

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION

Petitioner

v.

BiTMICRO LLC,

Patent Owner.

IPR2023-00781

U.S. Patent No. 7,826,243

**DECLARATION OF SCOTT THOMPSON, PH.D.
IN SUPPORT OF INTER PARTES REVIEW OF U.S. 7,826,243**

TABLE OF CONTENTS

I.	Introduction	1
A.	Qualifications and Expertise	2
B.	Understanding of Relevant Legal Principles.....	7
II.	The '243 Patent.....	10
A.	Technical Background.....	10
1.	Integrated Circuits (ICs).....	11
2.	Inter-chip Connection.....	14
3.	Packaging	16
4.	Moore's Law	24
5.	Multichip Module (MCM)	26
6.	IC Testing.....	29
B.	'243 Patent Summary	34
1.	The '243 Patent's Stacking Technique	34
2.	The '243 Patent's Routing Technique	37
C.	Prosecution History	39
D.	Level of Ordinary Skill in the Art	40
E.	Claim Construction.....	41
1.	<i>"a plurality of modules each comprising"</i> [1A].....	42
2.	<i>"passive port"</i> [1C].....	43
III.	GROUND 1: Claims 1, 2, 11 and 12 are Obvious Over the Combination of Hosomi and Sato	44
A.	Combination Overview	44
1.	Hosomi	44
2.	Sato.....	47
3.	Motivation to Combine	54
B.	Independent Claim 1	61
1.	Preamble [1P] and <i>"Plurality of Modules"</i> [1A].....	61
2.	<i>"One or More Active Ports"</i> [1B].	62
3.	<i>"Passive Port"</i> [1C].....	72

4.	<i>“First Serial Chain Route”</i> [1D].	75
5.	<i>“Second Serial Chain Route”</i> [1E] and <i>“Control Circuit”</i> [1F].	86
C.	Claim 2	98
D.	Claims 11 and 12	99
IV.	GROUND 2: Claims 1, 2, 11 and 12 are Obvious Over the Combination of Sung and Watanabe	100
A.	Combination Overview	100
1.	Sung	100
2.	Watanabe	110
3.	Combination of Sung and Watanabe	114
B.	Independent Claim 1	124
1.	Preamble [1P] and <i>“Plurality of Modules”</i> [1A].	124
2.	<i>“One or More Active Ports”</i> [1B].	130
3.	<i>“Passive Port”</i> [1C].	133
4.	<i>“First Serial Chain Route”</i> [1D].	141
5.	<i>“Second Serial Chain Route”</i> [1E] and <i>“Control Circuit”</i> [1F].	146
C.	Claim 2	161
D.	Claims 11 and 12	162
V.	Conclusion	169
	ATTACHMENT A	170

I. Introduction

I, Scott E. Thompson, Ph.D., declare as follows:

1. I have been retained by Perkins Coie LLP on behalf of Intel Corporation (“Petitioner”), to provide this Declaration concerning technical subject matter relevant to the petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 7,826,243 to Bruce et al. (“the ’243 patent”). It is my understanding that the ’243 patent is currently assigned to BiTMICRO LLC (“Patent Owner”).

2. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

3. I have reviewed and am familiar with the specification and the claims of the ’243 patent. In general, I will cite to the specification of a United States Patent using the following formats: (Patent No., Col:Line Number(s)) or (Patent No., Paragraph Number(s)). For example, the citation (’243 patent, 1:1-10) points to the ’243 patent specification at column 1, lines 1-10. Also, for convenience, I use italics to denote limitations from the challenged claims.

4. All of the opinions contained in this Declaration are based on the documents I have reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, I have reviewed the documents listed in the exhibit list of Attachment A to this Declaration. I have also reviewed and am familiar with the other materials referred to in this Declaration. To the best

of my knowledge, the documents listed above are true and accurate copies of what they purport to be and are the kinds of materials that an individual with expertise in this field at the relevant time period would reasonably rely on in formulating opinions, such as those set forth in this declaration.

5. I have been asked to provide my technical opinions regarding how a person of ordinary skill in the art (“POSITA”) would have understood the claims of the ’243 patent at the time of the alleged invention. For purposes of whether the teachings of the prior art render the claims of the ’243 patent obvious, I have been asked to assume the date of December 29, 2005, the filing date of the ’243 patent, for the analysis in this document. I have also been asked to provide my technical opinions on how concepts in the ’243 patent specification relate to claim limitations of the ’243 patent. In reaching the opinions provided herein, I have considered the ’243 patent, its prosecution history, and the references cited in Attachment A, and have drawn as appropriate on my own education, training, research, knowledge, and personal and professional experience.

A. Qualifications and Expertise

6. In formulating my opinions, I have relied on my knowledge, training, and experience in the relevant field, which I will summarize briefly. A more detailed summary of my background, education, experience, and publications is set forth in my curriculum vitae (“CV”), which is provided as INTEL-1004.

7. I have personal knowledge of the facts and opinions set forth in this declaration and believe them to be true. If called upon to do so, I would testify competently thereto. I have been warned that willful false statements and the like are punishable by fine or imprisonment, or both.

8. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '243 patent.

9. I have worked in the fields of integrated circuit and semiconductor design and semiconductor manufacturing—including as an Intel Fellow, the highest technical level at Intel Corporation and Director—for over 30 years. I have also taught and researched in these fields since 2004 including receiving \$4M in research contracts.

10. I received my Bachelor of Electrical Engineering with Highest Honors from the University of Florida in 1987. I also received my Master of Science of Electrical Engineering in 1988 and my Ph.D. in Electrical Engineering in 1992, both from the University of Florida. My Ph.D. was funded by the Semiconductor Research Corporation. My Ph.D. dissertation studied CMOS integrated circuits,

and I did extensive measurements and fabrication CMOS test structures. My Ph.D. dissertation earned a best paper award from the Semiconductor Research Corporation and a Best Ph.D. award from the University of Florida.

11. In 1992, after receiving my Ph.D., I joined Intel working on research and development of CMOS integrated circuits. From 1992 to 2004, I worked in Integrated Circuit development and semiconductor manufacturing. During this time, I managed the development of several integrated circuit manufacturing technologies for Intel including a 90 nanometer¹ and 130 nanometer² technologies.

12. These semiconductor manufacturing technologies used CMOS transistors, Copper interconnects and ball/pad connections. I won several Intel Achievement Awards for this work (Intel's highest award).

13. In 2000, I was promoted to Director of Semiconductor Technology

¹ See S. Thompson et al., "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1T1R SRAM cell," Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 61-64, doi: 10.1109/IEDM.2002.1175779.

² See S. Thompson et al., "130nm Logic Technology Featuring 60nm Transistors, Low-K Dielectrics and Cu Interconnects" (<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=0691ee478ab78508ef236ccb63fc3a04660f2850>)

Development in the Technology and Manufacturing Group at Intel. In that role, I was responsible for current and next-generation technology for integrated circuits. In that role I managed different areas including transistor technology, interconnects, integrated circuit package integration, integrated circuit yield, in-line defect metrology, and strategic long ranges plans for semiconductor technology. The Intel Technology and Manufacturing Group manufactured billions of dollars of CMOS integrated circuits each year. In 2002, I was appointed to the position of Intel Fellow, which is the highest technical position at Intel, and awarded for outstanding technical achievement both within Intel and industry. In that Intel role, I managed the development and manufacturing of the most advanced CMOS integrated circuits in the semiconductor industry—from 2000 to 2004, Intel surpassed IBM in integrated circuit development and became the industry leader. My team and I presented this work at many international conferences and invited talks and short courses.

14. Since 2004, I have been a professor of electrical and computer engineering at the University of Florida. I was granted tenure and promoted to full professor in 2006. During my teaching career, I developed graduate level courses on advanced semiconductor chip design, semiconductor manufacturing, packaging technology (chip stacking). I also teach a graduate level course on the chip technology used for CPU, DRAM, GPU, image sensors, and 2D and 3D image

sensor processing. My current research areas include modeling and reliability integrated circuits. I currently have a Research Contract with Texas Instruments on how package balls and pads introduce mechanics stress and shift the electrical characteristics of integrated circuits. My research in advanced chip technology at the University of Florida has been funded by contracts worth \$4M. I have supervised approximately 20 Ph.D. candidates on topics related to CMOS integrated circuits and have won several University of Florida teaching awards.

15. In 2009, I founded SuVolta, a company that developed ultra-low power chip technology for image sensors, system-on-chip microchips, radio frequency integrated circuits, memory, CPUs, image sensors processors, and other chips. The technology developed by SuVolta was sold to Fujitsu in 2015 and was used in the commercial production of Milbeaut image sensor processors. The technology allowed Fujitsu to lower the power consuming of the image sensor processor by 50%. Working with Fujitsu, we also developed CMOS chips that operated at ultra-low power and operate at less than 0.5V power supply. SuVolta received several awards and honors: (1) 2011 EuroAsia IC Industry Award for start-ups; (2) 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology; and (3) 2014 TiE 50 Top Startup. SuVolta was granted about 80 patents directed to low power transistor structures and integrated circuits on which I am a named inventor.

16. In 2006, I was elected as an IEEE Fellow for Advancing Fabrication of nanoscale MOSFET. In 2008, I received the Semi Award North America for Development of Strained Silicon Transistors.

17. Since 2005, I have worked as a consultant for leading companies in the semiconductor and computer chip industry, including Applied Materials, Cypress Semiconductor, Qualcomm, SanDisk, and Taiwan Semiconductor. I am the author of over 60 papers and one book related to semiconductors and am a named inventor on over 100 granted patents directed to integrated circuits and transistor structures.

B. Understanding of Relevant Legal Principles

18. I am not a lawyer and will not provide any legal opinions. But I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

19. I understand that a patent claim is invalid if it is anticipated or obvious in view of the prior art, and that a claim can be unpatentable even if all of the requirements of the claim cannot be found in a single prior-art reference. I further understand that invalidity of a claim requires that the claim be anticipated or obvious from the perspective of a person of ordinary skill in the art at the time the invention was made.

20. I have been informed that a patent claim is invalid if it would have

been obvious to a person of ordinary skill in the art. In analyzing the obviousness of a claim, I understand the following factors may be taken into account: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art; and (4) any “secondary considerations” of non-obviousness if they are present. Such secondary considerations include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention as compared to the closest prior art; praise of the invention by an infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I am not aware of any evidence of secondary considerations of non-obviousness relevant to the '243 patent. I reserve the right to supplement this Declaration if Patent Owner introduces evidence of secondary considerations of non-obviousness.

21. I understand that to prove that prior art or a combination of prior art renders a patent obvious, it is necessary to:

- identify the particular references that, singly or in combination, make the patent obvious;
- specifically identify which elements of the patent claim appear in

each of the asserted references; and

- explain why a person of ordinary skill in the art would have combined the references, and how they would have done so, to create the invention(s) claimed in the patent.

22. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of known technique(s) to improve similar devices (methods or products) in the same way;
- applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- “obvious to try” – choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a person of ordinary skill in the art; and
- some teaching, suggestion, or motivating in the prior art that would have led a person of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

23. I have also been informed that, in considering obviousness, hindsight reasoning derived from the patent at issue itself may not be used.

II. The '243 Patent

24. The '243 patent, titled “MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES,” was filed on December 29, 2005 and issued on November 2, 2010. (INTEL-1001.) The '243 patent relates to “a method of using [a] multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.” (INTEL-1001, 1:10–12.) In this section, I first provide a brief technical background of chip stacking and testing techniques, a high-level overview of the '243 patent, a discussion of the prosecution history of the '243 patent, and a discussion of claim construction.

A. Technical Background

25. At a fundamental level, “a functional electrical circuit requires transistors, resistors, diodes, etc. and the electrical connections between them.” (INTEL-1012, 143.) These electronic components are used to build primitive logic gates that “can be connected together to build more complex functions which may, in turn, be used as building blocks in yet more sophisticated systems.” (INTEL-1012, 103.) Until the mid-twentieth century, “transistors and other electronic components were available only in individual packages.” (INTEL-1012, 143.) Electrical circuits at that time were formed by laying out the discrete components on a circuit board and hand connecting them using separate wires. (*Id.*) However,

one disadvantage of electrical circuits formed using the discrete components was lower device yield, because “every solder joint on a circuit board is a potential source of failure, which affects the reliability of the design.” (INTEL-1012, 155.)

1. Integrated Circuits (ICs)

26. With the advent of integrated circuits, all of the electronic components of a device or system could be “formed on the surface layer of a sliver, or chip, of a single piece of semiconductor.” (INTEL-1012, 143.) The tracks linking components inside an integrated circuit, referred to in the art as “traces”, are orders of magnitude smaller than tracks linking components on a circuit board. (INTEL-1012, 155.) The invention of integrated circuits not only drastically reduced the dimensions of electrical circuits, but also lowers their costs and improves reliability. (INTEL-1012, 143 (“In the 1950s...an electronic gate capable of storing a single binary bit of data cost more than \$2. By comparison, in the early 1990s, enough gates to store 5,000 bits of data cost less than a cent. This vast reduction in price was primarily due to the invention of the *integrated circuit (IC)*.”) (emphasis in original); INTEL-1012, 155 (“Integrated circuits reduce the number of solder joints and hence improve the reliability of the system.”).)

27. An integrated circuit has all the electronic components formed on the surface layer of a chip or a piece of semiconductor material. (INTEL-1012, 143.) The most common semiconductor material is silicon, hence integrated circuits are

also known as “silicon chips.” (*Id.*) For the ease of description, I will use the terms “integrated circuits” and “chips” interchangeably throughout this document.

28. The fabrication process of integrated circuits (or chips) starts with wafers, which are circular slices of semiconductor material with thicknesses that provide “sufficient mechanical strength to allow it to be handled without damage.” (INTEL-1012, 144.) During fabrication, “the wafer is often referred to as the *substrate*, meaning ‘base layer.’” (INTEL-1012, 145 (emphasis in original).) Multiple layers are created on the substrate to form electronic components (e.g., transistors). (*Id.*) An integrated circuit includes at least “three distinct levels of conducting material: the *diffusion* layer at the bottom, the *polysilicon* layers in the middle, and the *metalization* layers at the top.” (INTEL-1012, 149 (emphasis in original).)

29. The NMOS transistor illustrated in the following figures from Maxfield is an example of an electronic component formed using the multi-layer technique. The NMOS transistor is formed on a silicon substrate and includes (i) source and drain regions formed in the diffusion layer, (ii) a gate electrode region formed in the poly-crystalline silicon layer, and (iii) metal tracks formed in the metalization layer. (INTEL-1012, 148–149.) As the number of transistors increase, more and more metal tracking layers can be added to the integrated circuit. (INTEL-1012, 149-150.)

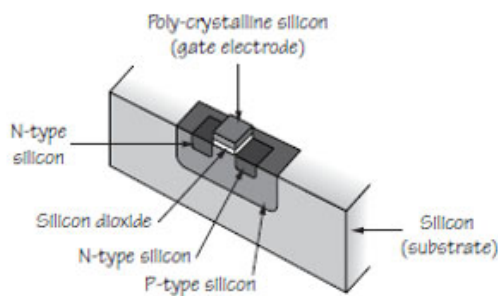


Figure 14-10. Add n-type diffusion regions and the gate electrode

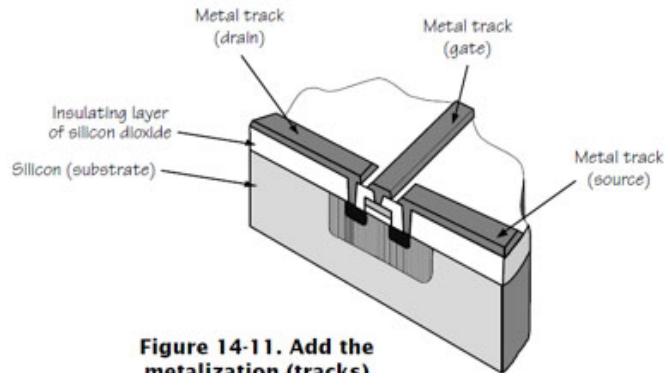


Figure 14-11. Add the metalization (tracks)

30. In general, “each layer requires its own unique mask.” (INTEL-1012, 145.) The patterns of each layer are formed through optical lithography, which is a common fabrication process that uses ultraviolet light (UV) and a photo-mask to project a pattern onto substrate. The patterns of ultraviolet light are subsequently used to form “corresponding structures in the silicon.” (INTEL-1012, 144.) The following figure from Maxfield depicts an “opto-lithographic step-and-repeat process” where “hundreds or thousands of identical integrated circuits” are formed on a single wafer by replicating the pattern across the whole wafer’s surface. (INTEL-1012, 144-145.)

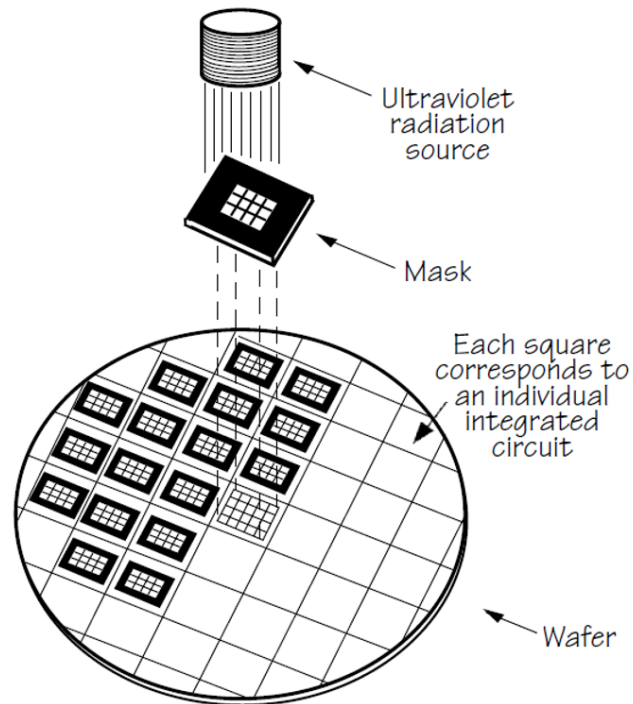


Figure 14-2. The opto-lithographic step-and-repeat process

2. Inter-chip Connection

31. After electronic circuit components are formed on the chips, each individual chip will need a way to communicate with external circuitry. This is achieved through conductive pads that “are constructed at the edges of each integrated circuit for testing and connection purposes. Some of the pads are used to supply power to the device, while the rest are used to provide input and output signals (Figure 14-12.)” (INTEL-102, 150.) “The pads can be connected to the internal components using the diffusion, polysilicon, or metalization layers.” (*Id.*) The tracks or “traces” interconnecting integrated circuit elements are formed of different layers of metalization that run along the surface of the chip. The

metalization layers form a hierarchy which ranges from lower metalization layers having thinner widths for interconnecting lower-level components to higher metalization layers having wider widths for interconnecting higher-level components.

32. The following annotated figure from Maxfield illustrates an array of identical chips formed on a single wafer. Each chip includes power and signal pads formed along the perimeter of an integrated circuit.

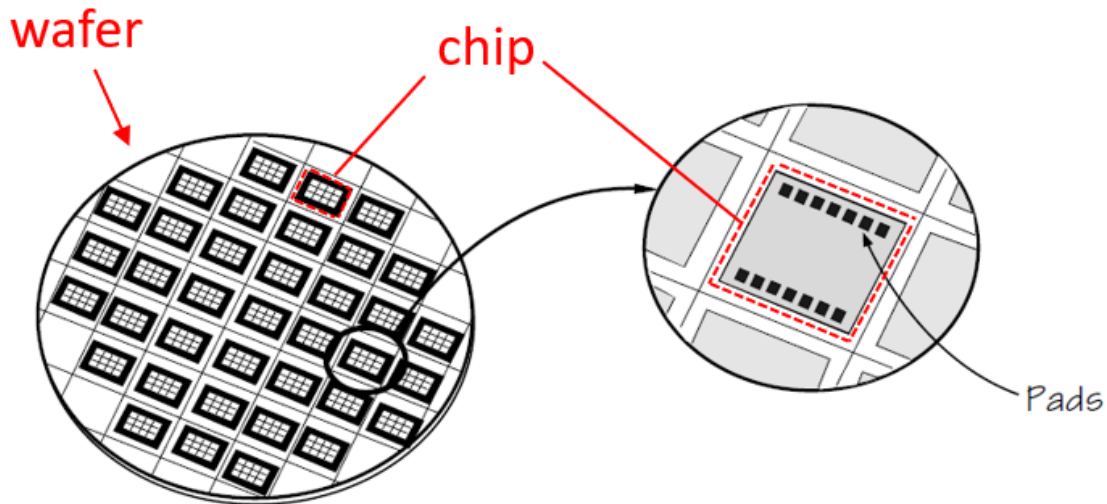


Figure 14-12. Power and signal pads

33. While the chips are still part of the wafer, each chip is individually tested for manufacturing defects, and chips that fail testing are rejected. (INTEL-102, 151.) Afterwards, “[t]he completed circuits, known as dies, are separated by marking the wafer with a diamond scribe and fracturing it along the scribed lines (much like cutting a sheet of glass or breaking up a Kit Kat® bar) (Figure 14-13).” (*Id.*) I have annotated and reproduced Figure 14-13 of Maxfield below. This die

separation process allows each die to be individually packaged for further processing using several packaging techniques, which I will discuss next.

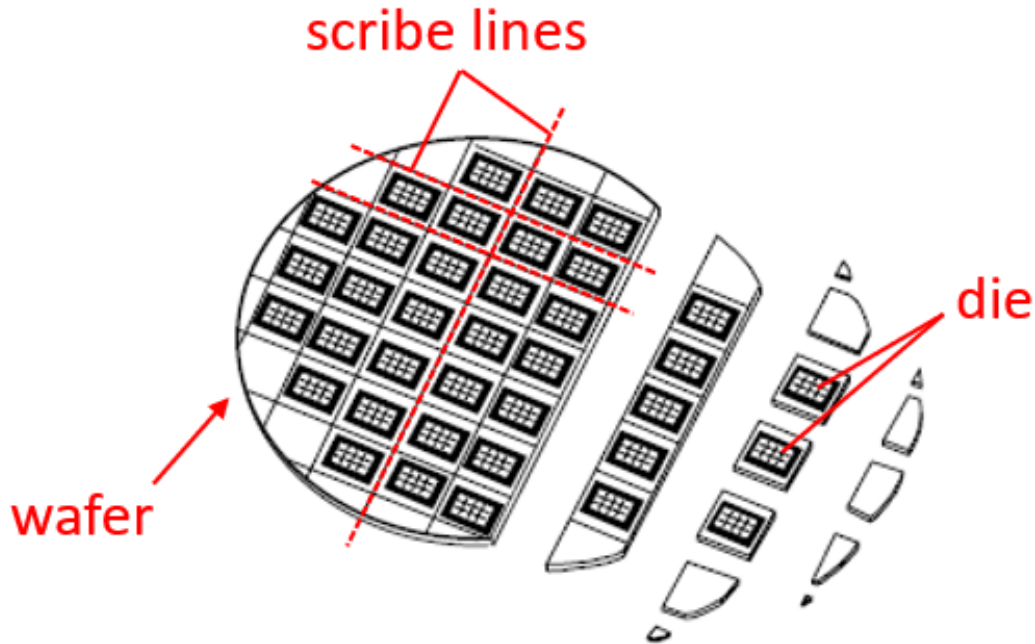


Figure 14-13. Die separation

3. Packaging

34. An electronic package, also referred to as a semiconductor package, may be defined as an integrated circuit's housing and interconnection. Electronic packages generally include (i) a structure to physically support the chip, (ii) a physical housing to protect the chip from the environment, (iii) a means of heat dissipation, and (iv) external electrical connections for routing signal and power to and from the chip. Packaging technology may be a factor in the determination of the price, performance, and reliability of a final semiconductor product. Examples of types of semiconductor packages include wire bonding, tape automated bonding

(TAB) and flip-chip solder bump bonding. (INTEL-1013, 267.) These connection alternatives are illustrated in Figure 7.12 of Blackwell, reproduced below.

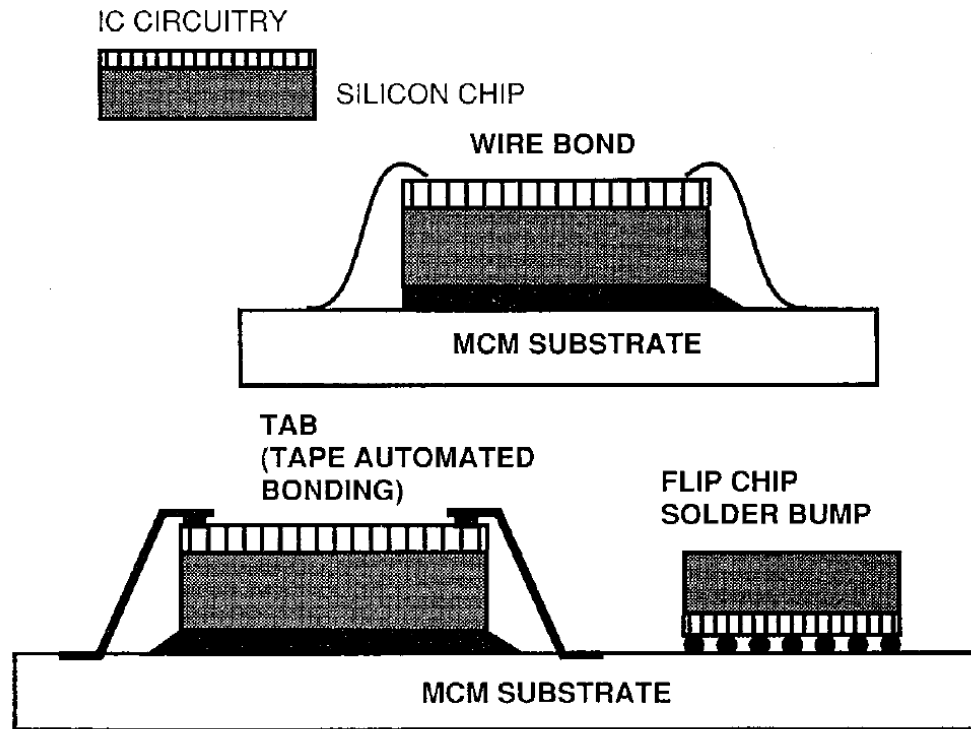


FIGURE 7.12 Chip attach options.

a) Wire Bonding

35. Wire bonding is “[a] relatively traditional process” of chip packaging that involves attaching a die to a metallic lead frame, connecting the pads of the die to leads on the frame through wire bonding, and encapsulating the assembly using plastic or epoxy. (INTEL-1012, 152.)

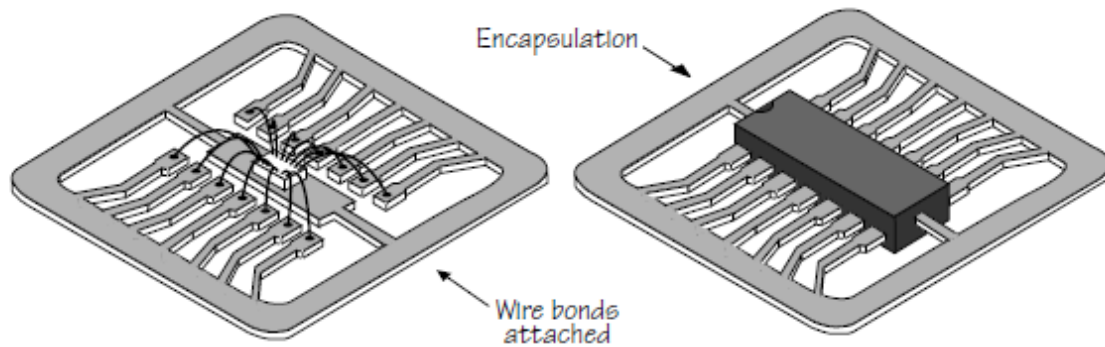


Figure 14-15. Wire bonding and encapsulation

“The unused parts of the lead frame are cut away and the device’s leads, or pins, are shaped as required.” (*Id.*)

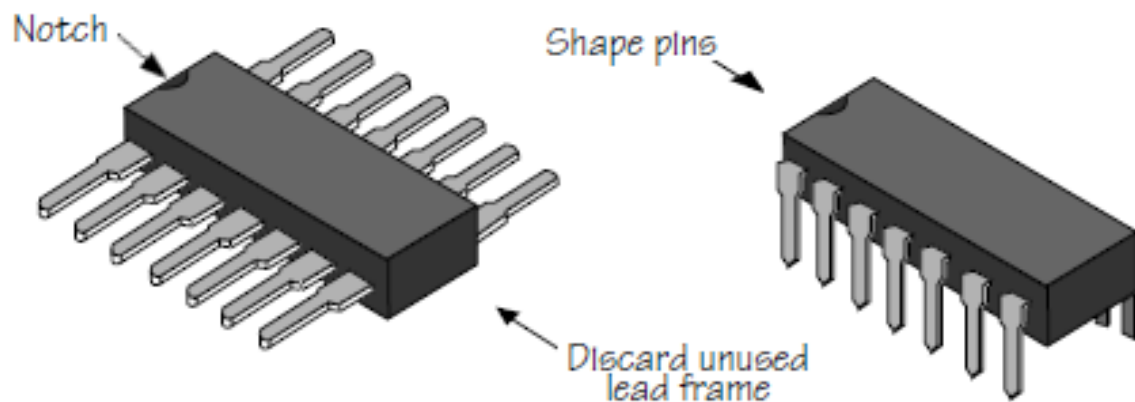


Figure 14-16. Discard unused lead frame and shape pins

The packaging technique described above has “pins that are intended to go all the way through the circuit board using a mounting technique called *lead through hole (LTH)*.” (INTEL-1012, 153 (emphasis in original).) However, the LTH mounting technique is best used for a device with very few pins. “By 2002, some integrated circuits had as many as 1,000 pins (with 2,000- and 4,000-pin devices on the horizon). This multiplicity of pins requires a very different approach.” (*Id.*)

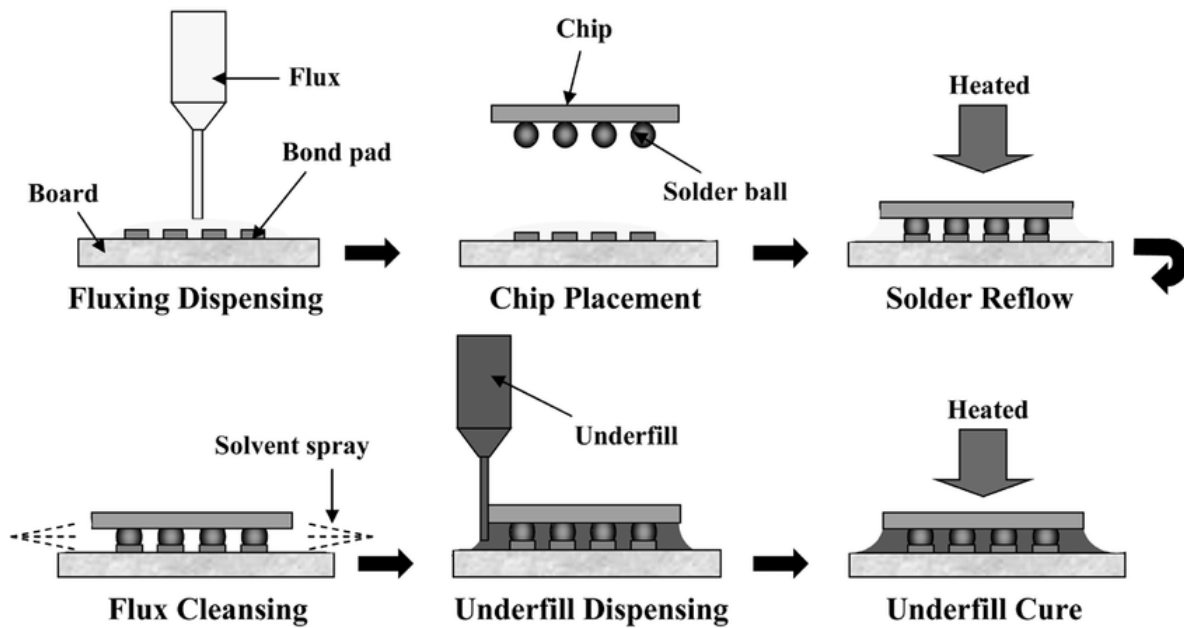
b) Solder Bump Bonding (Flip-Chip)

36. The solder bump bonding technique is one of many packaging technologies developed to accommodate the large number of pins. It is also referred to as a “flip-chip” technique, which includes placing bonding pads on the same surface of the chip upon which electronic devices are formed. The chip is then flipped upside-down to make electrical connections with a package substrate using solder balls that interconnect the bonding pads to bonding pads disposed on the package substrate.

[F]ace-bonded chips must have prepared bond pads suitable for direct placement and soldering to the substrate lands. The technique for pad preparation is known as *bumping*, since the end result is that each die bond pad has a solderable *bump* on it. Pad bumping is typically done with solder at each bond pad while the die are still in wafer form requiring special processing by the die manufacturer. ... For bumped die, the flip chip process begins with bumping the contact pads of the die. As noted previously bumping can be done several ways, but in most typical process results in tin-lead solder “bumps” being attached to each contact pad as shown in Fig. 4.4. ... This direct bonding to the substrate means the flip chip has real estate reductions compared to standard hybrid wire bonded die in much the same way that a ball grid array (BGA) has real estate reductions compared to a plastic leaded chip carrier (PLCC) or a quad flat pack (QFP). The real estate reduction is what gives flip chips their advantage in high-density circuits.

(INTEL-1013, 107–108 (emphasis in original).)

37. An exemplary flip chip manufacturing process is shown in the diagram below.



38. The flip-chip technique was first introduced commercially in the 1960s when IBM rolled out its “*controlled collapse chip connection (C4)*” technology for the System/360 to eliminate the expense, unreliability, and low productivity of manual wire bonding.” (INTEL-1013, 110 (emphasis in original).) In a flip-chip configuration, the power and signal pads of a chip are no longer restricted to the periphery like those implemented in the wire bonding technique, “but are instead located over the entire face of the die.” (INTEL-1012, 153.) “A minute ball of solder is then attached to each pad” to prepare the pads for subsequent bonding. (*Id.*)

39. As shown in the annotated Fig. 4.4 of Blackwell below, the most typical bumping process is attaching a tin-lead solder bump (shaded orange) to each contact pad (shaded dark green). (INTEL-1013, 108.)

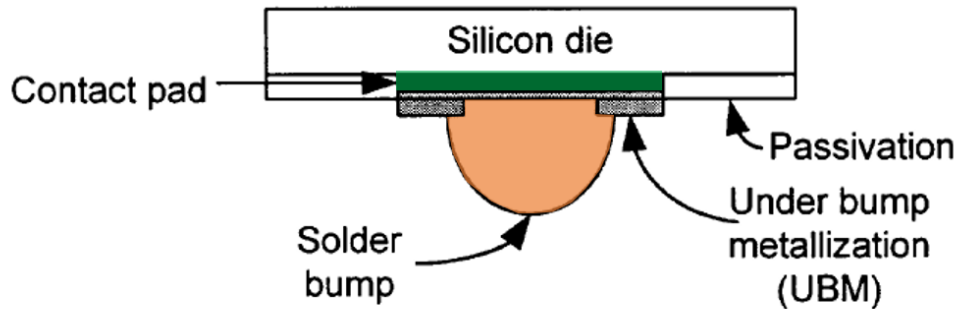


FIGURE 4.4 Typical solder bump.

The die is then flipped over and placed above a package substrate, with each solder ball aligned and in contact with a corresponding bonding pad on the package substrate. The “package-die combo is heated so as to melt the solder balls and form good electrical connections between the die and the substrate (Figure 14-17).”

(INTEL-1012, 153-154.)

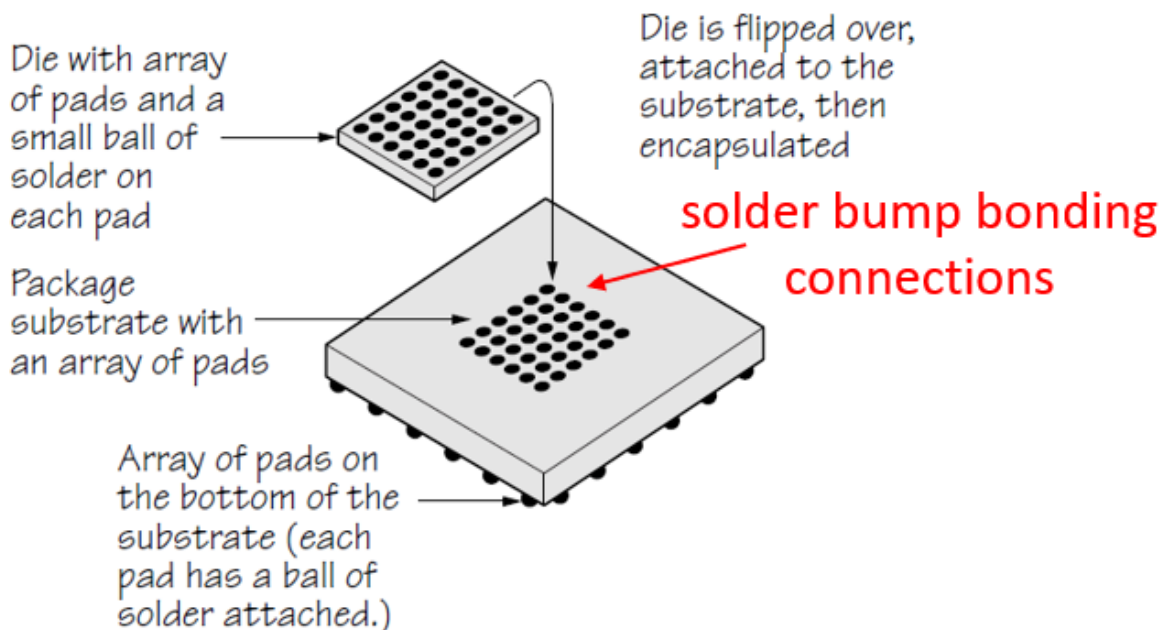


Figure 14-17. A solder bump bonded ball grid array packaging technique

These ball-to-pad (or “flip chip”) interconnections are “[t]he most popular attachment method” for making vertical interconnections in integrated circuits.

(INTEL-1014, 31.)

40. It should be noted that in integrated circuit packaging, a “bump” electrode is also known as a “ball” or “mound”. Each of these terms are synonymous and refer to small spherically-shaped balls of solder that are bonded (typically face-down) to contact pads of a semiconductor device or printed circuit board in order to provide vertical electrical connections. These electrical connections can be used, for example, to connect between a chip package and a printed circuit board, or between packages in a vertically stacked multichip module.

41. Flip chip connections have a number of advantages over other connection methods, including (i) reduced integrated circuit area and wiring length, resulting in high-density circuits with decreased parasitic capacitance and inductance, (ii) performance gains, especially at higher frequency operation, and (iii) simplified manufacturing process.

Flip chips are bare IC die placed on the board with bond pads down. Because of the reduction in ‘package’ size (there is none), and subsequent **reduction in electrical path length and associated parasitic capacitance and inductance, it is particularly suited for high-density, high-performance applications. ...**

(INTEL-1013, 106.)³ “The table below shows examples of the parasitics that exist in a variety of packages. **Flip chip advantages are obvious.**”

TABLE 4.1 Parasitics in Various Electronic Packages

Package type	Parasitic capacitance, pF	Parasitic Inductance, nH
Flip chip	0.1	0.01
Chip on board/wire bond	0.5	1–2
Pin grid array	1	2
Quad flat pack	1	1–6
Through-hole DIP	3	8–20

(INTEL-1013, 107.)

42. For example, compared to wire-bonded dies, the flip-chip technique not only reduces parasitic capacitance due to shortened electrical connection, but also provides “real estate reductions” that give flip chips their advantage in high-density circuits. (INTEL-1013, 108.) Flip chips can provide thousands of connections in a small area, resulting in a much greater connection density than wire bond connections. “For example, a 1-cm² chip could support 1600 solder bumps (at a conservative 250 μ m pitch) but only 533 wire bonds.” (INTEL-1013, 268.)

c) Vias

43. In electrical engineering, “vias” are “hole[s] filled or lined with a

³ All bold emphasis and annotations are added unless specifically noted otherwise.

conducting material, which [are] used to link two or more conducting layers.”

(INTEL-1012, 444; *see also* INTEL-1013, 607 (“*Via*. A plated-through hole that is used as an interlayer connection ...” (emphasis in original).) Vias are generally used to create three-dimensional integrated circuits and packages. There are different types of vias known in the art. For example, a “through-hole” via is a “via that extends completely through a substrate and is solder plated.” (INTEL-1013, 99.) Vias may include through-chip vias, interdie vias, through-package vias, etc.

44. The purpose of these various types of vias is to route electrical signals and power vertically up and down the stacked layers (as opposed to horizontal routing confined in planes formed by each layer). The vias route connections vertically between the layers, and in general it is a design decision to locate vertical routes in the chip(s) or in the substrate that the chip(s) are mounted on; or to even to use both types of vias. During the time frame of the '243 patent, due to common manufacturing methods, placing vias on the chip (versus the substrate) would generally results in higher cost. However, placing vias on the chip generally would allow for smaller and higher density of vias that enables higher overall module performance. Copper (a metal with very low resistance) would be a typical metal used inside the via independent of where it was placed.

4. Moore's Law

45. The ongoing goals of the computer industry include higher

performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits. It was Gordon Moore (co-founder of Intel Corporation) who first realized that new generations of memory devices were released approximately every 18 months, and that each new generation of devices contained roughly twice the memory capacity of its predecessor. (INTEL-1012, 161). “This observation subsequently became known as *Moore’s Law*.” (*Id.*, (emphasis in original).) In accordance with Moore’s law, the number of transistors that can be constructed in a certain area of silicon doubles approximately every 18 months.

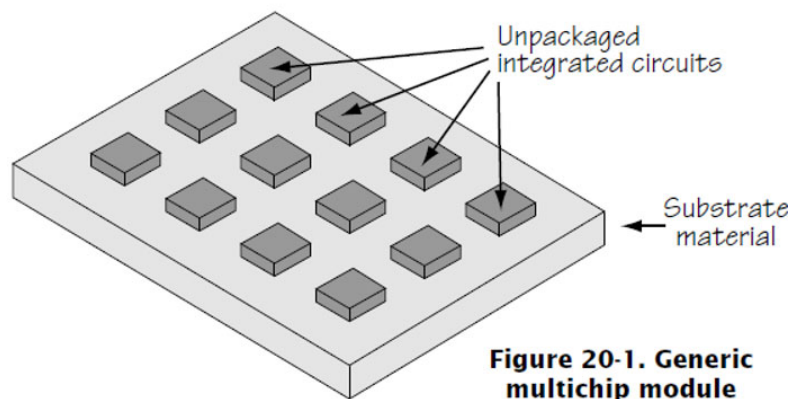
46. Moore’s law continued unabated for over 40 years, but transistor scaling has inevitably slowed as the scale of transistors approaches atomic dimensions. At such small sizes, transistor function begins to break down due to degradation of the conducting channel. (INTEL-1015, 22.) When transistor gate lengths are so small, the conducting channel begins to leak current even when the device is switched off. (*Id.*) Leakage power in modern transistors can be as high as 20-30 Watts (out of a total power budget of 100 Watts). (*Id.*)

47. As a result, electronic device performance can no longer be improved by transistor scaling alone. For this reason, chip developers have turned to other methods for producing smaller-footprint devices with improved functionality and processing power. Such techniques include integrating chips together in a

multichip module and using chip stacking techniques to further conserve area on the main circuit board.

5. Multichip Module (MCM)

48. Continuous advances in the speed and scale of integrated circuits have created a huge demand for high density packaging and reduced interconnection delays for improved performance. In order to conserve the amount of surface area consumed on a semiconductor substrate, various types of high-density packages have been developed. Included among these is the multi-chip module (MCM). Compared with single-chip packages, MCMs reduce circuit board area and improve performance. (INTEL-1012, 275.)



49. A MCM is generally an electronic assembly (such as a package with a number of conductor terminals) where multiple integrated circuits (ICs or “chips”), semiconductor dies and/or discrete components are integrated together, usually onto a unifying substrate. A “module” in a MCM comprises a packaged integrated circuit chip, and modules with multiple integrated circuit chips disposed on a

common substrate are MCMs. (See INTEL-1012, 275.) Packaging multiple chips into a MCM provides several benefits, including improved device yield, balanced heat distribution, reduced power consumption, and increased device density. The common substrate illustrated in Figure 20-1 (above) above essentially serves as a platform on which integrated circuit dies can be physically mounted using various techniques, such as “adhesive, eutectic, or flipped-chip techniques, and electrically connected using wire bonding, tape automated bonding, or solder bumping methodologies.” (INTEL-1012, 286.)

50. In general, a MCM module includes the following main physical components: (i) a substrate base that provides discrete circuit elements; (ii) a chip connection that transfers signals and power between the substrate and the chips; and (iii) a MCM package housing that surrounds the MCM and allows signals, power, and heat to be conducted to the outside world. (INTEL-1013, 262.) These components are illustrated in the following figure:

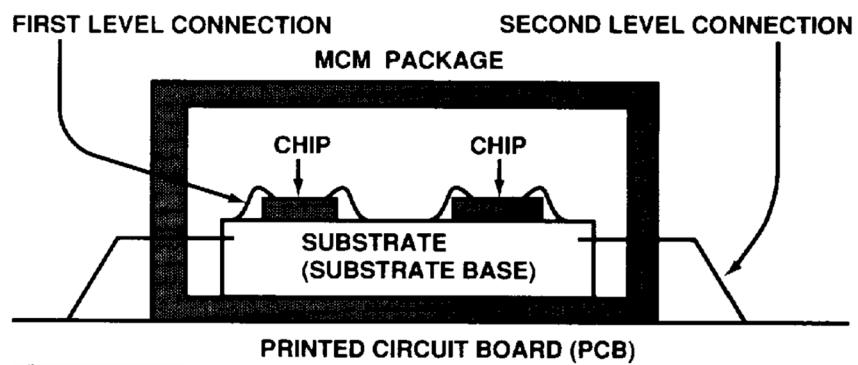


FIGURE 7.6 Physical technology components to an MCM.

(INTEL-1013, 263.) As shown, the chips are mounted on the substrate and electrically connected to the substrate through a wire bond chip-to-substrate connection.

51. Other types of multi-chip modules include assemblies of semiconductor devices that are stacked on top of one another. Since a stack of semiconductor devices consumes roughly the same amount of silicon real estate as a single-chip device or package, the amount of surface area that may be saved by stacking devices is readily apparent. In that sense, 3D integration provides a continuation of Moore's law beyond the stopping point of transistor scaling. It provides a path to further miniaturization through the reducing device footprint, increasing device density, and shortening interconnect lengths. The evolution of conventional 3D packaging is shown in the figure below. (See INTEL-1016, 5.)

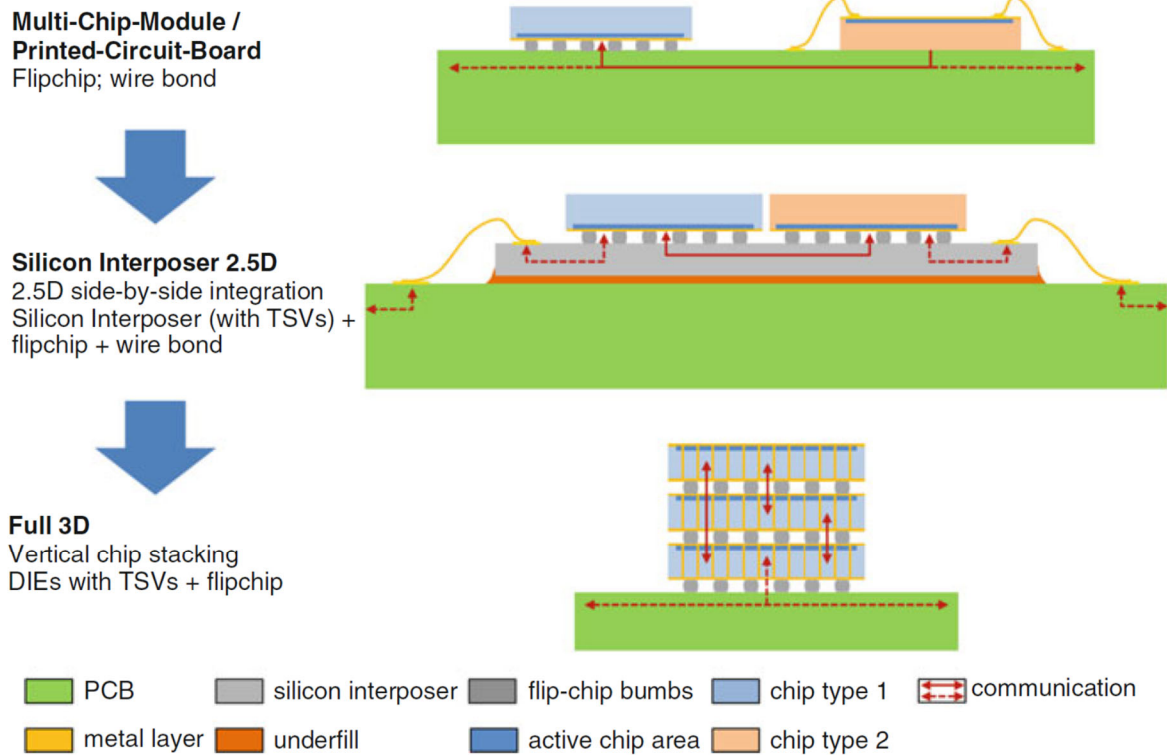


Fig. 1.2 Advancement towards 3D integration

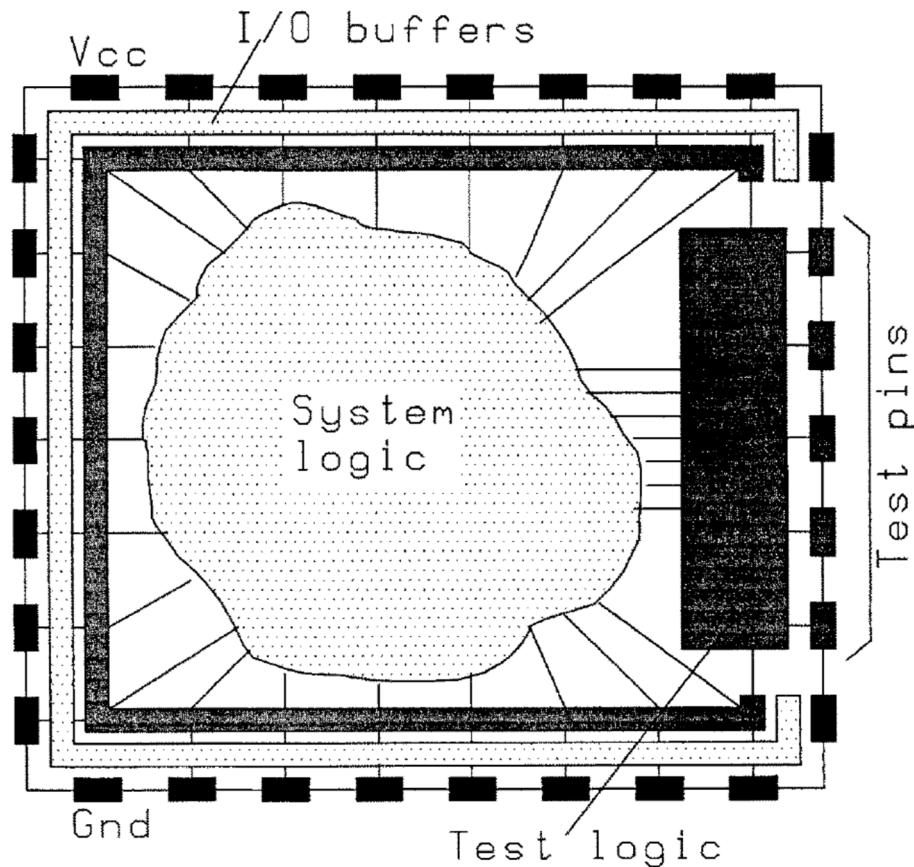
6. IC Testing

52. Despite the many advantages, MCMs were slow to penetrate high volume markets due to the unsatisfactory quality of the chips, low yield, high cost of manufacturing, and high complexity of testing and rework. (INTEL-1017, 1–2.) “Due to the increased complexity of digital ASICs having very high pin density packages, access to pins for defect isolation and diagnosis of device, mounted on multi-layer PCB or MCM **is extremely difficult by conventional bed-of-nails or probes method.**” (INTEL-1018, 130.) Indeed, a significant portion (25–30%) of the cost of an MCM is associated with its testing, diagnosis, and repair of faulty connections. (INTEL-1017, 2) Thus, “[t]o minimize the overall MCM cost, it is

also necessary to minimize the test cost of MCMs....” (INTEL-1017, 5).

53. Design For Testability (DFT) is a way to reduce the cost of testing and diagnosis of electronic circuits and has been used extensively over the decades preceding the '243 patent. (INTEL-1017, 5.) DFT involves building test circuitry directly into an integrated circuit design. Adding DFT to a circuit design costs very little in silicon real estate and can have immense benefits in manufacturing and testing. (INTEL-1019, 160.) Boundary Scan is among the most popular DFT technique. (INTEL-1017, 5.) Boundary Scan enables observability of test results on the circuit's primary input/output (I/O) pins. This allows input test data to be applied to the circuit without the burden of propagating test vectors through many levels of logic and enables immediate identification of defective components on the circuit board. (INTEL-1019, 159.)

54. As a result of efforts by the Joint Test Action Group (JTAG), Boundary Scan was standardized by the IEEE in 1991 in the IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture, which defines testability features that can be incorporated into digital circuit designs for testing. (See INTEL-1020.) An overall view of an IC design that conforms to the IEEE 1149.1 Standard is shown below.



(INTEL-1023, 28.) This circuitry includes system logic that performs the normal functions of the chip and test logic defined by the IEEE standard that performs the testing functions for the chip.

55. The JTAG Boundary Scan architecture “associates a memory cell with each input and output of a chip. These memory cells are connected serially to form a shift register” around the periphery of the circuit as shown in the diagram below. (INTEL-1017, 5-6.)

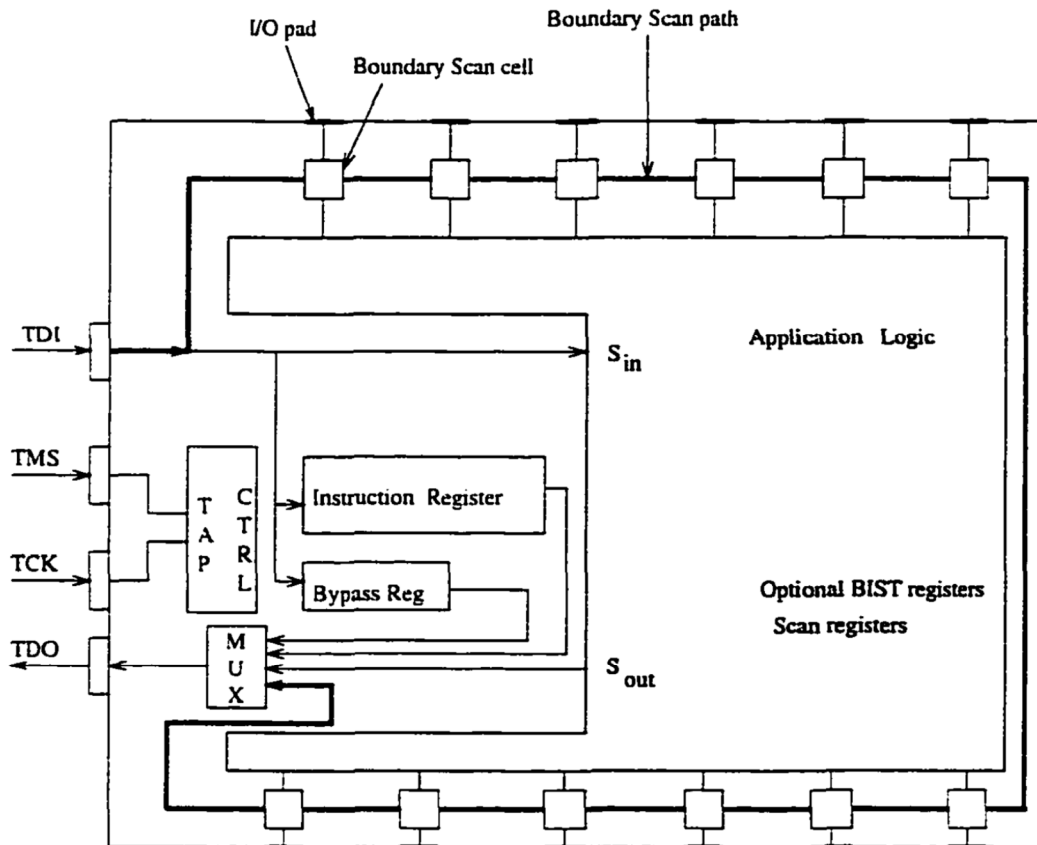


Figure 4: Chip supporting boundary scan standard IEEE 1149.1.

56. Boundary Scan includes a Test Access Port (TAP) which comprises four lines/ports, namely the test data in (TDI), the test data out (TDO), the test mode select (TMS), and the test clock (TCK). (INTEL-1017, 6.) These lines/ports are controlled by an external JTAG tester device mounted on the circuit board. In operation, test instructions and test data are input to the chip under test using the TDI line and the test results are output from the chip to an external JTAG tester using the TDO line. Once the tests are performed, the test results are shifted out of the shift register on the TDO line to the external tester, and the new test data is

shifted into the shift register on the TDI line as the results are shifted out. (See INTEL-1017, 6–7.)

57. Use of boundary scan in multichip modules provides a number of advantages such as enabling testing of connections between stacked modules without using external probes.

Complete prefabrication design verification is more critical when MCMs are being used, so more effort must be spent on logic and electrical simulation prior to fabrication. ... In a production module, you need to locate faulty die or wire bonds/solder bumps if faulty module is to be repaired (typically by replacing a die). **It is more difficult to physically probe lines on an MCM, however, than on a PCB.** ... The test plan must be able to isolate a fault to a single chip or chip-to-chip interconnection. **It is best to base such a plan on the use of chips with *boundary scan*** (Fig. 7.14). With boundary scan chips, test vectors $ca[n]$ be scanned in serially into registers around each chip. ... The results are used to determine which chip or interconnection has failed.

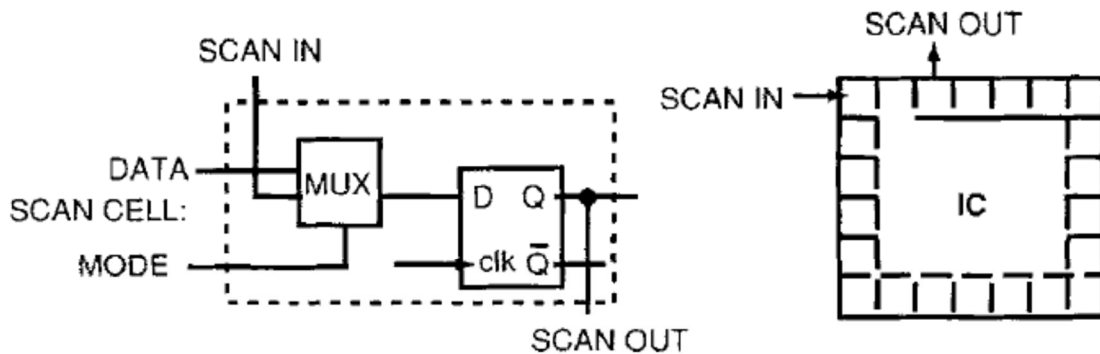


FIGURE 7.14 The use of boundary scan eases fault isolation in an MCM.

(INTEL-1013, 272.)

Using the JTAG/boundary-scan logic **minimizes the amount and complexity** of equipment for testing boards and for device

programming in design, manufacturing and service **as it removes the need for external probing and complex fixtures.**

(See INTEL-1021, 1.)

58. Boundary scan is an electrical testing technique that enables information about the state around the electronic component to be tested even though direct access to the internal circuitry is not possible. Therefore, testable designs of digital circuits and systems are essential for obtaining high reliability and boundary scan testing technology would have been the preferred choice for a POSITA conducting testing on MCMs and 3D stacked structures.

B. '243 Patent Summary

1. The '243 Patent's Stacking Technique

59. The '243 patent concerns “a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.” (INTEL-1001, 1:10–12.) The '243 patent explains that semiconductor devices such as disk drives “typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FEPROMs and the RAMs,” which the patent contends “limits the miniaturization of the entire storage device.” (INTEL-1001, 1:14–20.) According to the specification, stacking “maximizes the capacity in a limited area thus realizing the move to miniaturize the entire storage device.” (INTEL-1001, 1:21–24.)

60. The '243 patent describes using identical single chip or multichip modules at each layer of the stack. (INTEL-1001, 4:17-18 (“single and multiple chip modules are created to become the basic building blocks for the stacking technique”), 9:6-7 (“All SDRAM modules are identical”), 9:32–38 (“This way ensures four identical modules to be stacked”), 10:5–8 (“Since the modules are identical ...”).) According to the patent, this “modular approach is used in creating basic building blocks which can be tested individually and replaced easily prior to final packaging, making the technique reliable, and cost effective.” (INTEL-1001, 1:62–65.) In an exemplary embodiment of an SDRAM module, “three SDRAM dies 201 are placed in a single substrate 203 to become the SDRAM module which is one of the basic building blocks.” (INTEL-1001, 4:19–40.)

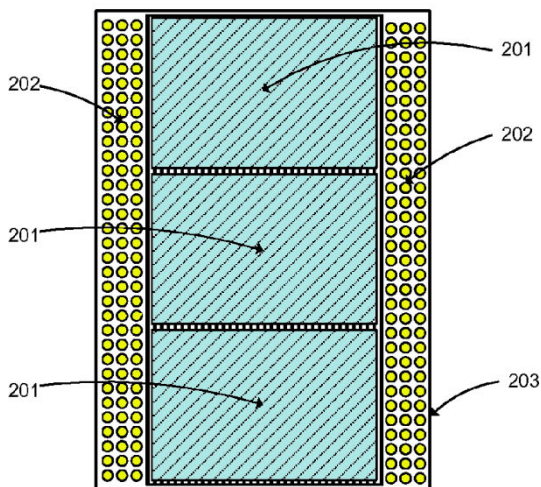


Figure 2a

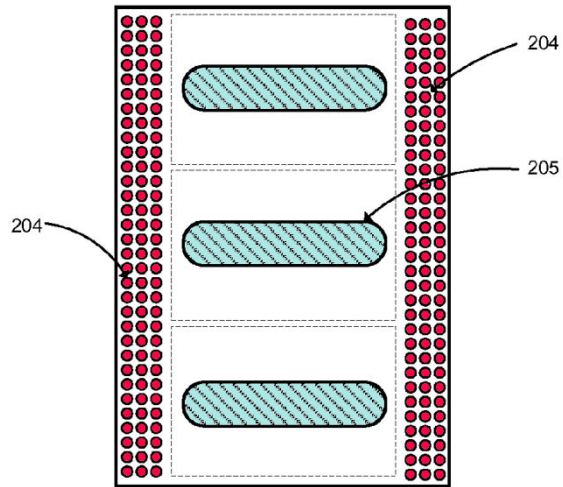


Figure 2b

'243 Patent, Annotated Figure 2a (Top View); Figure 2b (Bottom View)

The “[c]ombination of these modules and dies in a substrate creates a package with

a specific function or range of memory capacity. These packages are stacked to increase capacity or add functions.” (INTEL-1001, 1:32–38.)

61. “FIG. 2c is the stacked module cross sectional representation. Top pads 202 and bottom balls 204 act as the vertical interconnects between all SDRAM modules and to the controller module.” (INTEL-1001, 4:31–34.)

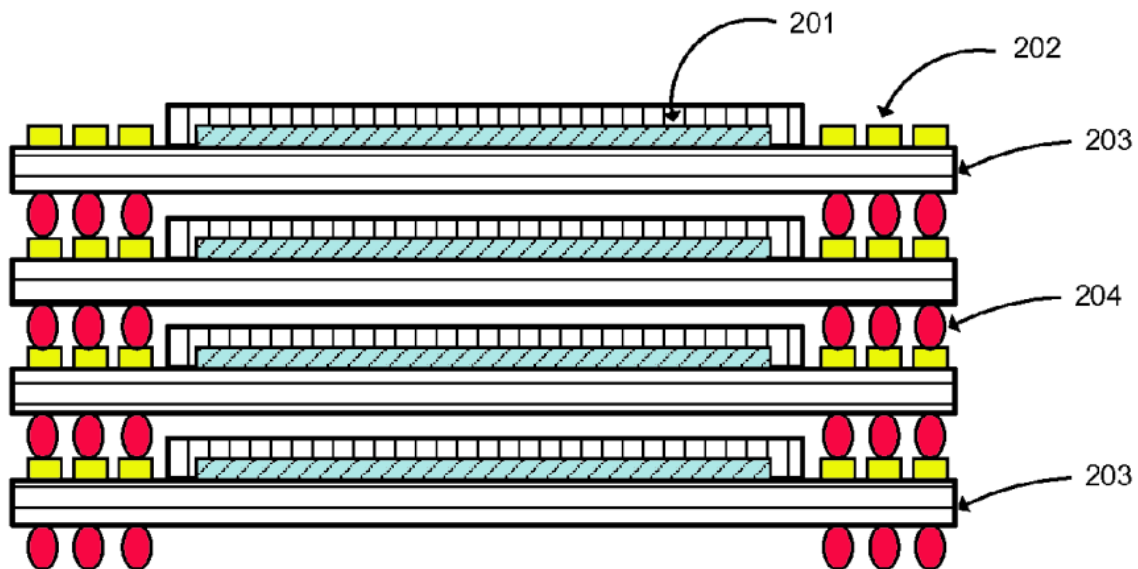


Figure 2c

'243 Patent, Annotated Figure 2c (Cross-Sectional View)

As shown, the solder ball connections (red) disposed on each module at each stacked layer are interconnected with corresponding bonding pads (yellow) disposed on the module below to form a repeating pattern of ball-to-pad interconnections.

62. However, stacking components such as dies and modules was well known before the '243 patent, a fact acknowledged by the patent itself when noting

that its embodiments “take[] advantage of the existing stacking technology both on the module and package level” such as “flip chip, wire bond, MCM, module stacking, advance packaging, etc., ... to accomplish highly reliable module to module and package to package interconnection and scalability.” (INTEL-1001, 1:38–42, 59–60; *see also*, §II.A.3.(b)–(c) (discussing prior art three-dimensional packaging).)

2. The '243 Patent's Routing Technique

63. The '243 patent further discloses several “pin assignment and signal routing techniques ... wherein internal and external signals are routed from [the] main board to various stacked modules.” (INTEL-1001, Abstract.) One example pin assignment and connection technique is shown in Figure 19 below. This configuration “enables a selection of specific module[s] in a multiple module stack.” (INTEL-1001, Abstract, 8:61–63.)

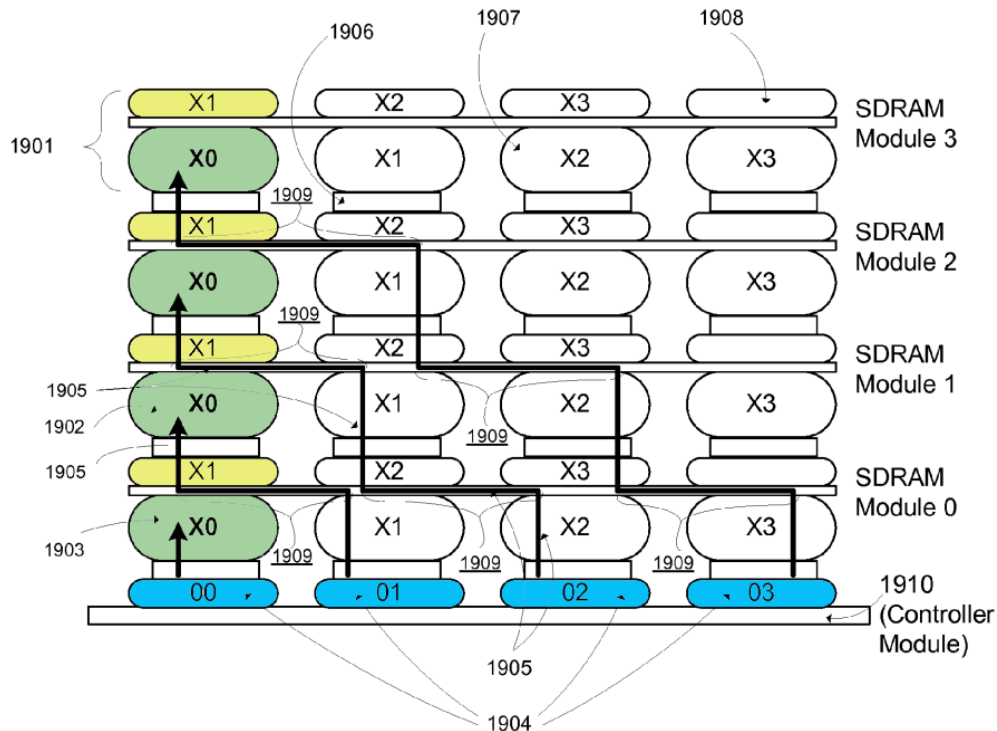


Figure 19

'243 Patent, Figure 19

64. The '243 patent, as modified by the amendment during prosecution which is reflected in the Certificate of Correction ("COC") further describes using "serial chain routes" in the stack. Figure 21b is the sole embodiment having the claimed "serial chain routes" coupled by a "control circuit" in an end module of the stack. (See INTEL-1001, 9:67.) The specific routing path illustrated in Figure 21b is, for example, a "JTAG TDI-TDO signal path." (INTEL-1001, 10:32–33.) JTAG boundary scan testing of interconnections was well-known and standardized by IEEE years before the '243 patent, as I discussed in the background section.

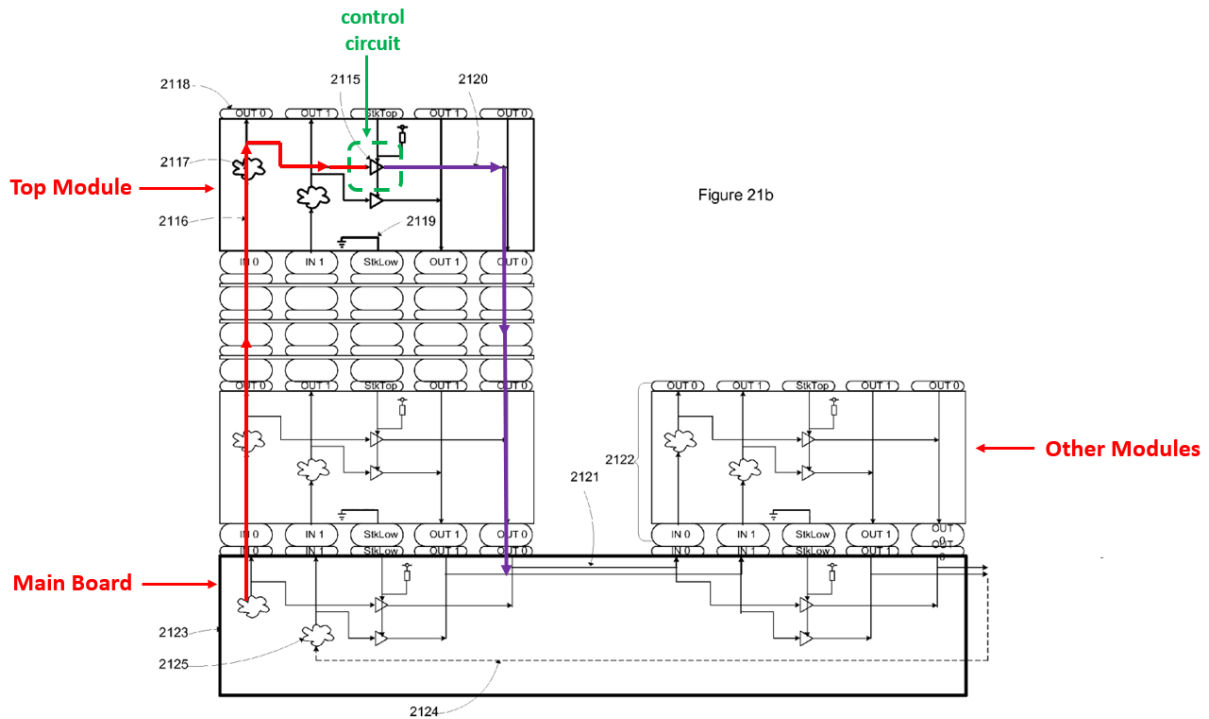


Figure 21b

'243 Patent, Annotated Figure 21b

C. Prosecution History

65. I have reviewed the prosecution history of the '243 patent and much of the subject matter of challenged independent claim 1 cannot be found in the specification as filed and was only inserted later by an amendment made late in prosecution. Early in prosecution, the Applicant sought patent protection for a broad claim directed to "A stacked module" with "one or more active port" and "one or more passive port." (INTEL-1002, 471.) The Examiner rejected this claim as anticipated and found the set of claim limitations, "one or more passive ports for passing through the one or more active signals", "one or more passive ball and one or more passive pad", and "one or more pair of daisy chain input port and daisy

chain output port”, were indefinite based on the then existing specification. (INTEL-1002, 449-456.) In its response of November 2009, the Applicant made extensive amendments to the specification adding over **40 lines** of new subject matter to the discussion of Figures 19 through 21. (*See* INTEL-1002, 403-408; INTEL-1005, 2-3; INTEL-1006.) For example, the Applicant added extensive discussion of serial chain routes including the concept of serial chain connections, circuits, inputs, and outputs. (INTEL-1002, 403-408; INTEL-1005, 1-3; INTEL-1006.) The Applicant also amended the claims to recite the newly added subject matter. (*See* INTEL-1002, 414-419.) Applicant characterized these amendments as “clerical” in nature, merely “correct[ing] **minor errors** noted in the Office Action.” (INTEL-1002, 423.) I do not agree with these characterizations made by the Applicant.

66. The Examiner allowed the claims based on these amendments in the second Office Action, finding a limitation based on the added subject matter, directed to connecting serial chain routes using a control circuit, patentable over the applied prior art. (INTEL-1002, 388.) However, the concept of connecting two routing paths in an integrated circuit using a control circuit was also well-known in the art, as discussed below.

D. Level of Ordinary Skill in the Art

67. I understand that certain issues relating to the validity of the ’243

patent must be judged from the perspective of a person of ordinary skill in the relevant art, as I discuss below. I have been asked to define the level of a “person of ordinary skill in the art” or “POSITA” at the time the alleged invention was made. In deciding the level of ordinary skill, I have considered the following factors, which I have been informed are relevant to the determination of ordinary skill in the art:

- the level of education and experience of persons working in the field;
- the types of problems encountered in the art;
- the prior art solutions to these problems;
- the rapidity with which innovations are made; and
- the sophistication of the technology.

68. In my opinion, a POSITA at the time of the '243 patent would have been someone with (1) a bachelor's degree in electrical engineering or similar discipline, and two to three years of work experience in semiconductor packaging or (2) a master's degree with one or more years of experience in those fields. My opinion below explains how a POSITA would have understood the technology described in the references identified in this declaration as of the priority date of the '243 patent.

E. Claim Construction

69. I understand that “claim construction” is the process of determining a

patent claim's meaning. I understand that the Patent Office applies the same claim construction standard used in district courts which seeks to give claim terms their plain and ordinary meaning to a POSITA at the time of the claimed invention in view of the claims, specification, and prosecution history. I also understand that if the patent applicant gave a term a special meaning in the specification or during prosecution, then the special meaning should control. In this section, I provide my opinion on the proper interpretation of claim terms "*a plurality of modules each comprising*" and "*passive port*"⁴.

1. "*a plurality of modules each comprising*" [1A].

70. The term "*a plurality of modules each comprising*" is not part of the preamble and should be construed as "each module in the stacked module comprising." Claim 1 recites "*A stacked module comprising a plurality of modules each comprising:*" In this claim, "*[a] stacked module comprising*" is the claim's preamble. The "*plurality of modules*" language follows the preamble and should be considered as part of the body of the claim.

71. A construction requiring the modifier "*each*" to apply to the modules in the "*plurality of modules*" and not to the entire "*stacked module*" as a whole is consistent with the specification which repeatedly describes a stacked module as having multiple **identical** modules. (See, e.g., INTEL-1001, 9:6–8 ("All SDRAM

⁴ Claim language is indicted with italics throughout.

modules are identical ...”); INTEL-1001, 3:29–33 (“FIG. 20a shows ... a rotational stacking orientation to allow stacking of **four identical modules**”); 9:32–38.) Moreover, the sole claimed embodiment of Figure 21 **requires** identical stacked modules. (INTEL-1001, 10:5–8 (“Since **the modules are identical**, this routed signal passes through ...”).) I also note that the final limitation in the body of the claim (“*the plurality of modules*”) depends on the term for antecedent basis.

72. I understand that Patent Owner (“PO”) has construed “*a plurality of modules each comprising*” in a co-pending district court litigation as part of the claim preamble and not a limitation of the claim. (See INTEL-1026, 15-18.)

2. “*passive port*” [1C].

73. The term “*passive port*” should be construed as a “connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module.” This construction is consistent with the definitional statement added by the Applicant to the specification during prosecution: “The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module ... **is named ‘passive port.’**” (INTEL-1001, 9:8 (as modified by COC); INTEL-1005, 2; INTEL-1002, 405, 425.)

74. I understand that Patent Owner (“PO”) contends a “*passive port*” is simply any “connection between a passive ball and a passive pad.” (See INTEL-

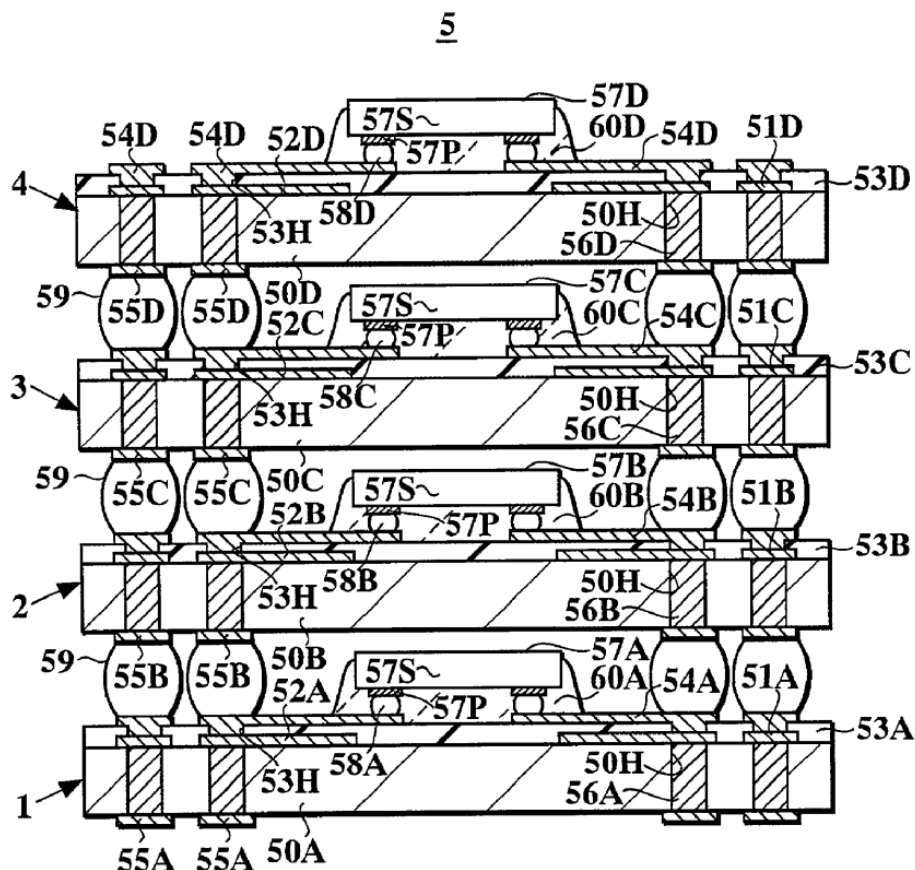
1026, 13-15.)

III. GROUND 1: Claims 1, 2, 11 and 12 are Obvious Over the Combination of Hosomi and Sato

A. Combination Overview

1. Hosomi

75. Hosomi discloses a semiconductor module 5, illustrated below, comprising four stacked semiconductor devices 1 to 4. (INTEL-1007, ¶89.) “A plurality of semiconductor devices are laid one over after another, thereby constituting a semiconductor module.” (INTEL-1007, Abstract.)



Hosomi, Figure 5

76. Semiconductor devices 2-4 “are substantially identical” to device 1 and “are three-dimensionally stacked one over” one another “on the semiconductor device 1.” (INTEL-1007, ¶89.) Each semiconductor device “includes at least a package substrate 50A, a semiconductor chip 57A mounted on the package substrate 50A by the flip-chip structure, and a protecting resin film 60A extending over the semiconductor chip 57A in order to protect it against surroundings.” (INTEL-1007, ¶95.) The substrate of each device “is provided with front electrodes 51A and rear electrodes 55A on the opposite surfaces thereof, and two wiring layers 52A and 54A on the front surface thereof.” (INTEL-1007, ¶96.) The front and rear electrodes are connected by vias 56. I note that Hosomi does not refer to connection 56 as a “via” but a POSITA would recognize it as such because it is a vertical conductive path through the substrate. A POSITA would further understand that Hosomi’s front and rear electrodes are conductive “pads” on the substrates because they are electrically connected to other components and are adapted for solder bumping. For example, rear electrode 55 “is electrically and mechanically connected, via a bump electrode 59” to a front electrode on an adjacent device. (INTEL-1007, ¶101.) In fact, conductive pads were well known interconnection elements often used with solder bumping for face-down interconnections.

[F]ace-bonded chips must have prepared bond pads suitable for direct placement and soldering to the substrate lands. The technique for pad

preparation is known as bumping, since the end result is that each die bond pad has a solderable bump on it. Pad bumping is typically done with solder at each bond pad while the die are still in wafer form requiring special processing by the die manufacturer. ... For bumped die, the flip chip process begins with bumping the contact pads of the die. As noted previously bumping can be done several ways, but in most typical process results in tin-lead solder “bumps” being attached to each contact pad as shown in Fig. 4.4. ... This direct bonding to the substrate means the flip chip has real estate reductions compared to standard hybrid wire bonded die in much the same way that a ball grid array (BGA) has real estate reductions compared to a plastic leaded chip carrier (PLCC) or a quad flat pack (QFP). The real estate reduction is what gives flip chips their advantage in high-density circuits.

(INTEL-1013, 107–108; *see also* §II.A.3.b.)

77. In integrated circuit packaging, a “bump” electrode (also known as a “ball” or “mound”) refers to small spherically-shaped balls of solder that are bonded (typically face-down) to contact pads (or regions) of a semiconductor device or printed circuit board in order to provide vertical electrical connections. (See §II.A.3.(b).) These electrical connections can be used, for example, to connect between a chip package and a printed circuit board, or between packages in a vertically stacked multichip module, such as the one disclosed by Hosomi.

78. Hosomi teaches using solder bump electrodes 59 in a “flip chip structure” between the stacked modules. Although Hosomi does not depict solder bumps (balls) coupled to electrodes 55 on the bottom surface of the bottom device, a POSITA would have understood that these would be included to attach the module to another component such as a printed circuit board. Indeed, prior to

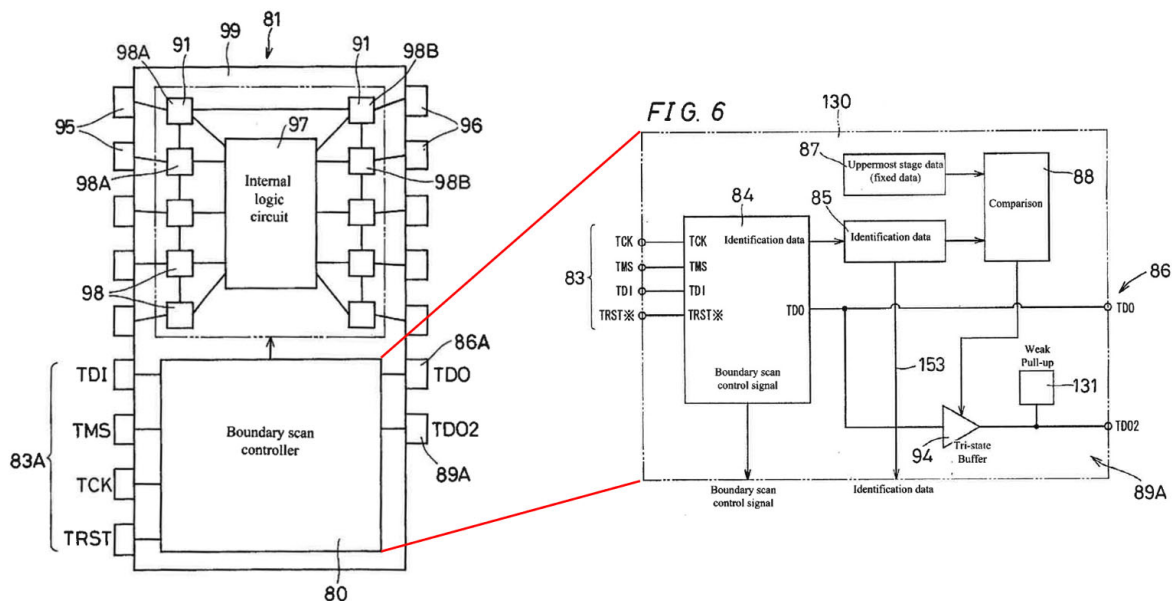
the '243 patent, solder bumping was the “most popular attachment method” for mounting a chip package such as Hosomi’s stacked module to a printed circuit board. (INTEL-1014, 31.)

2. Sato

79. Sato discloses “a boundary scan controller for testing connection states of input/output terminals of a plurality of semiconductor chips ... [in] a three dimensional multilayered LSI (Large Scale Integration).” (INTEL-1009, 1:9–12.). Sato’s boundary scan controller, illustrated below right, “operates in conformance to the standards of the JTAG (Joint European Test Action Group).” (INTEL-1009, 13:22–23.) The controller input has four signal lines: TCK (Test Clock) which “supplies input/out timings”, TMS (Test Mode Select) which “inputs the predetermined operation instruction”, TDI (Test Data input) which “serially inputs the identification data and the test data”, and TRST (Test Reset) which “inputs data for asynchronously initializing the controller.” (INTEL-1009, 14:1–11.) I note that TRST is an optional signal line in the standard and may not be included in JTAG implementations. (*See, e.g.*, INTEL-1009, 14:12-15.) These signal lines “are controlled by an external JTAG tester.” (INTEL-1009, 14:11–12.)

80. The controller is shown disposed in the semiconductor chip assembly
81 of Figure 2 (below left). The chip has standard IEEE test circuits added in a block called “Boundary scan controller.” Long before the '243 patent, these test

circuits were added to chips to support testing using the IEEE standard. One embodiment of the internal componentry of the controller is shown in Figure 6 (below right). Although Figure 2 includes controller 80 and Figure 6 includes controller 130, Sato teaches that the only difference between controllers 80 and 130 is “in the configuration of the data derivation part 89A.” (INTEL-1009, 25:11–18.) Therefore, Sato’s teachings regarding the common components of the controllers apply to both embodiments.



Sato, Figures 2 (left), 6 (right)

81. Control means 84 of the controller “set[s] test pattern data for performing the boundary scan test.” (INTEL-1009, 15:1–4.) For example, when an the “instruction of sending data is input to the control means 84,” the “various data which are input from the signal line TDI can be output from a signal line TDO ... through the shift registers.” (INTEL-1009, 15:4–7.) Sato performs JTAG boundary

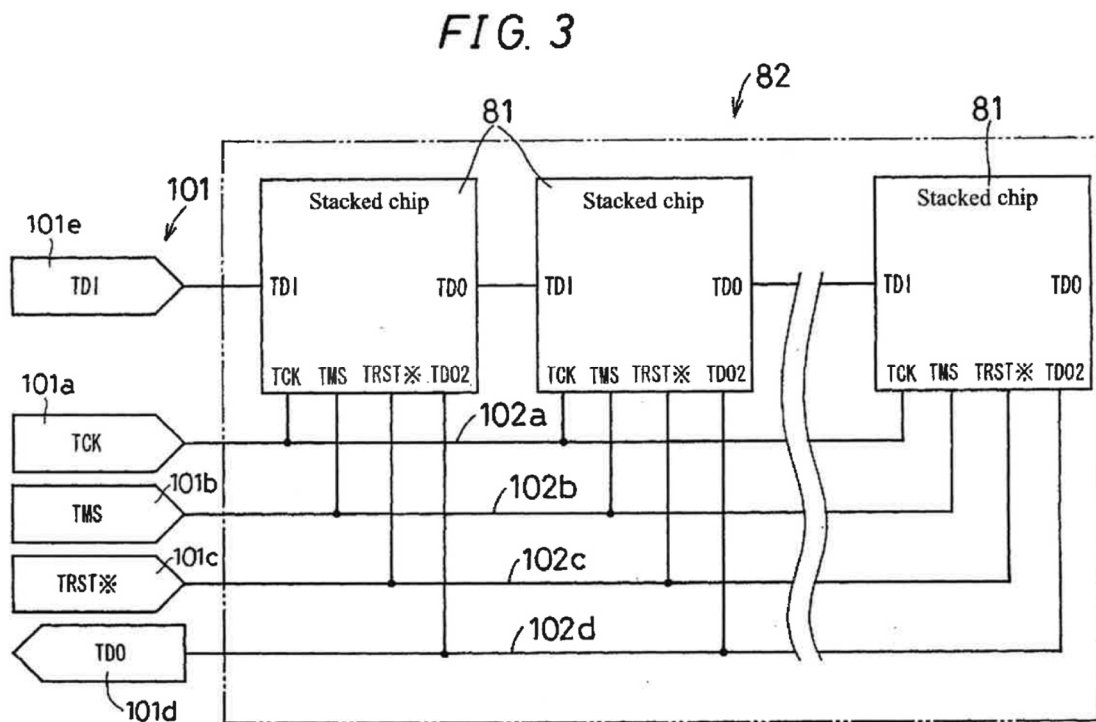
scan testing in this “daisy chain” manner wherein the output of a “controller of a lower stage” is connected to the input of a “controller of an upper stage.” (INTEL-1009, 8:5–8.) Thus, the TDO output data is the TDI input data during a boundary scan.

82. Fixed storage means 87 stores chip identification data loaded “when the semiconductor device 82 is configured.” (INTEL-1009, 16:1–4.) Storage means 85 stores the identification data received and “decoded by the control means 84” during operation. (INTEL-1009, 15:9.) Comparison means 88 determines “whether or not the identification data and the fixed data are matching, and outputs comparison result information.” (INTEL-1009, 16:12–15.)

83. Data derivation part 89A includes tri-state buffer 94 connected to comparison means 88. (INTEL-1009, 25:19–20.) If the comparison result from comparison means 88 “indicates matching between the identification data and fixed data, the tristate buffer 94 outputs the same data as the data from the output part 86” (e.g., TDO output data) on the TDO2 signal line. (INTEL-1009, 25:21–23.) If the comparison result indicates that the identification data and the fixed data do not match, “the tristate buffer 94 is prevented from outputting input data.” (INTEL-1009, 25:26–28.) In such cases, the routing path through the tristate buffer 94 is disabled.

84. In addition, Sato teaches that its boundary scan controller may be

disposed in **each** of the semiconductor chips in a vertically stacked multichip module and used for performing a boundary scan over all of the modules in the stack. (INTEL-1009, 10:21–23.) Sato’s semiconductor device 82 illustrated below in Figure 3, “is configured by stacking” semiconductor circuit chip assemblies 81. (INTEL-1009, 20:7–11.) Signal lines TCK of respective chips “are connected to the same bus line 102a, and are interconnected with the corresponding TCK pin 101a of the connector 101.” (INTEL-1009, 20:18–20.) Similarly, signal lines TMS and TRST “are respectively connected to identical bus lines” 102b and 102c. (INTEL-1009, 20:20–23.)

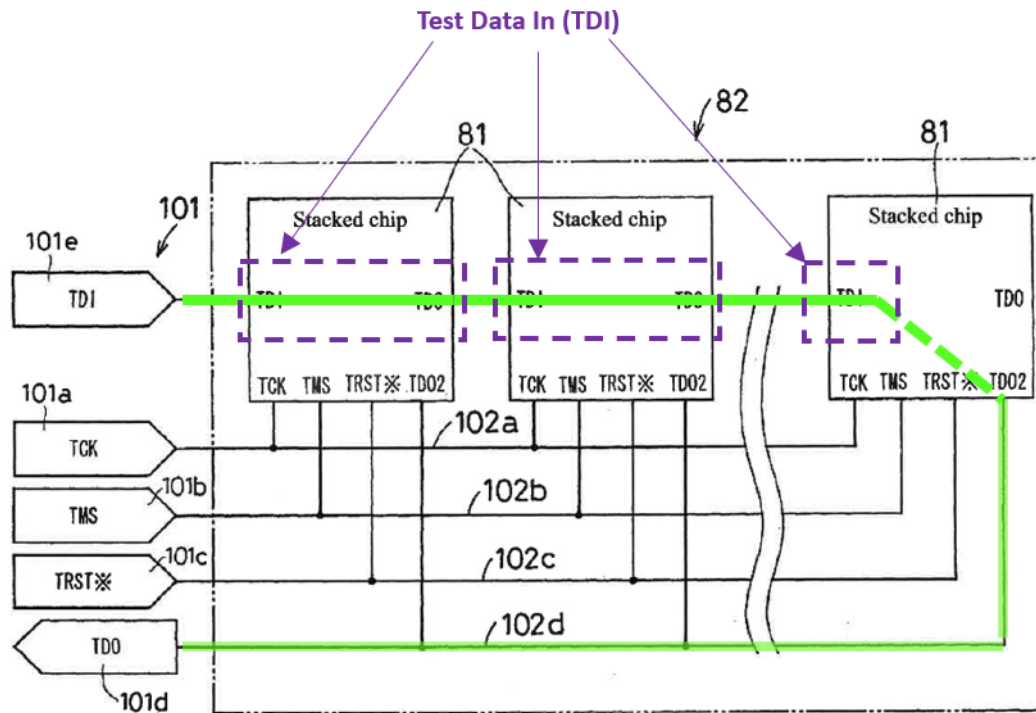


Sato, Figure 3

85. As illustrated above, the TDO output of the assemblies 81 “on the

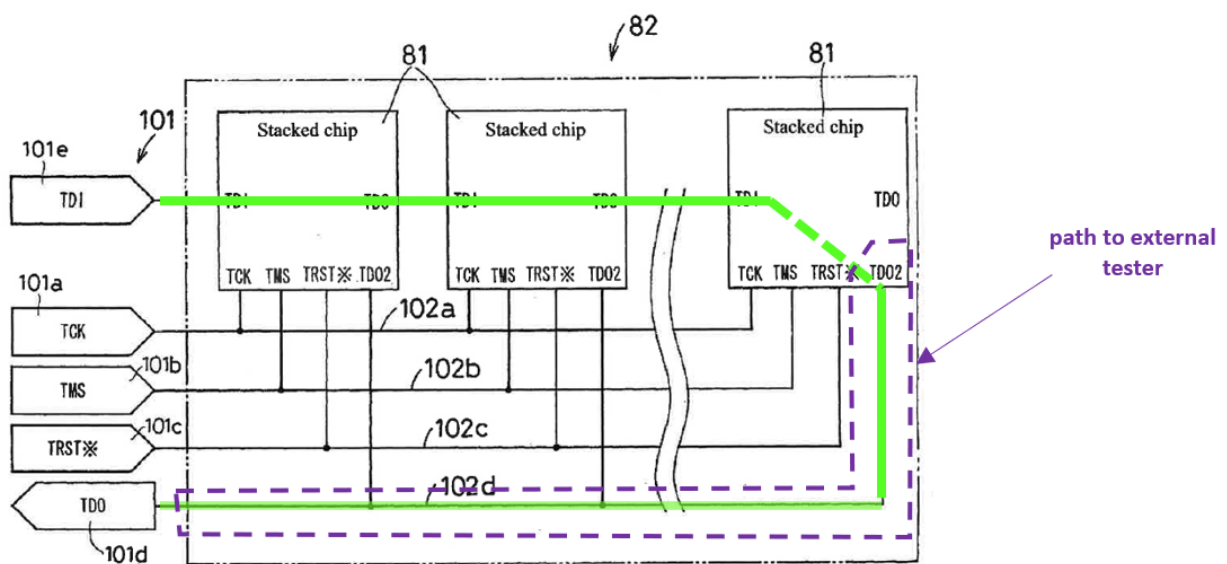
preceding stage sides are successively connected to the input part connection terminals 83A corresponding to the signal lines TDI of the semiconductor circuit chip assemblies 81 on the succeeding stage sides.” (INTEL-1009, 20:24–27.) In the top chip assembly 81, TDI is connected to TDO2 because no device is stacked above it. (INTEL-1009, 20:29–30, 22:26–32.) TDO2 is then passed to the external JTAG tester over bus 102d.

86. In this manner, individual controllers 80 “are connected in the shape of a chain” (referred to as a “daisy chain”) in the stacked module allowing all assemblies to be “simultaneously subjected to the boundary scan test.” (INTEL-1009, 20:31–21:1.) This “daisy chain” into and out of the stacked modules is shown in 2-dimensions in Figure 3 below. When the TDI signal reaches the uppermost module, it cannot be output on the TDO signal path because there is no module stacked above. Instead, the TDI signal is routed to the TDO2 contact pad. (INTEL-1009, 25:19–25.)



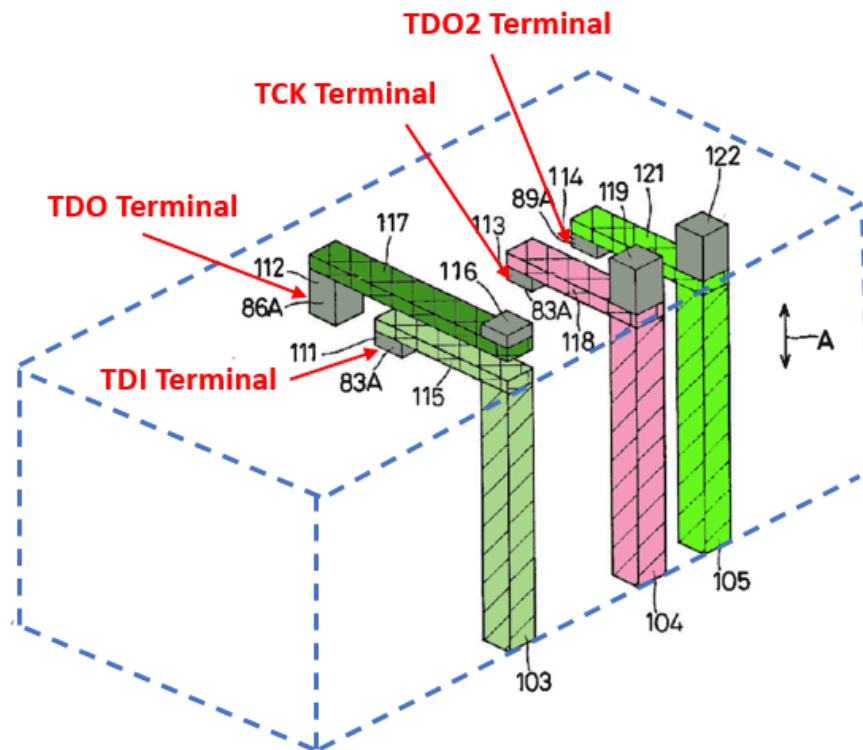
Sato, Annotated Figure 3

87. The TDO2 signal is then passed back down the stack to the external JTAG tester at the bottom (not shown).



Sato, Annotated Figure 3

88. In operation, the TDI signal enters each stacked module through a penetrating electrode, which provides vertical interconnections between the stacked modules. (INTEL-1009, Figure 5, 23:26–30.) I note that Sato uses the terminology “electrode” to refer to the vertical electrical path through its assembly. A POSITA would recognize this vertical connection as a “via” which I discussed in the background section. The daisy chain connection pattern for an individual assembly 81 is illustrated in Sato’s Figure 5 below, which I have annotated to outline a portion of the device substrate to provide context.



Sato, Annotated Figure 5

89. The electrodes 103-105 “penetrate through the semiconductor circuit

chip assembly, namely in the direction of arrow A.” (INTEL-1009, 23:12–15.) Terminal 111 is the input (83A) for signal line TDI and terminal 113 is the input (83A) for signal line TCK. (INTEL-1009, 23:20–23.) Terminal 114 is the connection (89A) for signal line TDO2. (INTEL-1009, 23:23–25.) Connection lines 115, 118, and 121 between electrodes 103-105 and terminals 111, 113, and 114 are “formed in one surface of the semiconductor circuit chip assembly.” (INTEL-1009, 23:27–28, 24:4–5, 24:22–23.) Terminal 112, the output (86A) of signal line TDO, is “interconnected with the first connection terminal 116 through the second connection line 117 which is stacked on the first connection line 115” with an “inter-layer insulating film interposed therebetween.” (INTEL-1009, 23:32–24:2.) Terminals 116, 119, and 122 are connected to the end of electrodes 103, 104, and 105 (respectively) of an adjacent assembly. (See INTEL-1009, 23:28–30, 24:5–7, 24:14–16.)

3. Motivation to Combine

90. A POSITA would have been motivated to incorporate Sato’s JTAG/boundary scan controller into each chip in each module⁵ of Hosomi’s

⁵ I refer to each of Hosomi’s semiconductor devices as a “module” because the device includes a chip coupled to substrate. I refer to the stack of devices in Hosomi as a “stacked module.”

91. There are numerous reasons a POSITA would have been motivated to combine Hosomi and Sato's teachings. First, Sato provides an express teaching that would have led a POSITA to incorporate Sato's boundary scan testing into Hosomi's stacked semiconductor module. Sato teaches that its boundary scan test "detect[s] the connection states of individual semiconductor circuit chip assemblies in a semiconductor device which is composed of a stack of semiconductor chip assemblies which are configured by **disposing the boundary scan controller in the semiconductor circuit chip.**" (INTEL-1009, 8:2–5; *see also*, 8:26–27 (the "device can be configured by stacking the **same semiconductor circuit chip assemblies which include the boundary scan controllers.**"); 13:18–19 (chip "configured by **disposing the boundary scan controller 80 in a semiconductor chip.**")).) And Hosomi teaches a low cost and highly reliable technique to route connections between the layers in the stack.

92. Second, a POSITA would have understood that testing was essential, if not required, for manufacturing stacked modules such as those taught by Hosomi and that boundary scan was the preferred and most widely used testing method. Boundary scan testing typically occurs at time of manufacture. For example, when the stacked module is an SDRAM memory module (as taught by Hosomi), the SDRAM module manufacturer would have been motivated to test the stack of modules to ensure each layer of memory is properly interconnected before

shipping the product to customers. A POSITA would have been motivated to use boundary scan testing for this purpose because boundary scan enables testing of the internal interconnections between devices in a stack without using external probes. (INTEL-1013, 272 (explaining that it is “more difficult to physically probe lines” and that “[i]t is best to base” a test plan “on the use of chips with boundary scan.”).)

93. As a result, a POSITA desiring to incorporate boundary scan into Hosomi’s stacked modules would have looked to the available options at the time and been led to Sato. Sato teaches a particular implementation that incorporates a boundary scan controller into **each** module in a stacked architecture such as Hosomi’s. Sato also teaches how to route the boundary scan for the top module or chip in a stack back to the JTAG testers for the technologically important case of stacking identical modules or chips. Boundary scan testing of Hosomi’s stacked identical modules would also require a control circuit for routing as taught by Sato. Thus, in order to efficiently test Hosomi’s stacked modules, a POSITA would have been motivated to implement Sato’s method which taught how to add the IEEE 1149.1 standard boundary scan architecture to stacked modules to support testing. For example, a POSITA would have been motivated to combine Sato’s boundary scan teachings into Hosomi’s stacked architecture to minimize the amount and complexity of equipment required for testing. (INTEL-1021, 1 (explaining that

“[u]sing the JTAG/boundary-scan logic minimizes the amount and complexity of equipment for testing boards ... [and] saves time and costs for your board test and programming systems ...”).) Even the '243 patent itself recognized JTAG/boundary scan would be used to test the stacked modules or chips in this time frame. (*See* INTEL-1001, 10:32-33.)

94. Further, at the time of the '243 patent, it was already standard practice to add pre-tested and validated IEEE 1149.1 boundary scan circuit blocks to integrated circuit chips such as Hosomi's. Indeed, by the time of the '243 patent, boundary scan technology was widely known and standardized for use in testing and validation of integrated circuits, including stacked multichip modules. Sato explicitly applies the standards of JTAG for boundary scan testing, referring throughout to an external “JTAG tester.” (INTEL-1009, 4:9–5:5, 14:6–18.) The JTAG boundary scan standard was adopted in 1990 by IEEE as the IEEE Standard 1149.1, over 15 years before the '243 patent. (INTEL-1020.) Moreover, boundary scan was described in textbooks many years before the '243 patent. (*See, e.g.*, INTEL-1013, 272-273.) Boundary scan technology was also in use before the '243 patent.

Design For Testability (DFT) techniques **have been extensively used over the last few decades** for testing electronic circuits as simple as integrated circuits (ICs) to very complex multi computer systems [23]. **Boundary Scan (BS) is among the most popular DFT technique employed for enhanced test and diagnosis of electronic systems** [24, 25]. To better address the problems of testing, the IEEE 1149.1 Test

Access Port and Boundary Scan Standard has been developed [26.27] for providing an efficient methodology to test chips, boards and systems.

(INTEL-1017, 5; *see also* §II.A.6.)

95. As a result of its popularity and wide use, it would have been obvious to a POSITA to incorporate boundary scan technology into Hosomi's stacked architecture, and a POSITA would have been motivated to do so because it was almost universally known that circuits of all types require testing during manufacture to confirm fault-free interconnections and that boundary scan provides a standardized way for conducting such testing.

96. Moreover, a POSITA would have combined these well-known elements of Hosomi and Sato (stacked chips) using well-known methods (JTAG boundary scan testing) to yield no more than predictable results (fault-free interconnections). As discussed above, JTAG boundary scan was standardized since the early 1990s and would have been well known to a POSITA by 2005. Groups, such as NASA, were integrating JTAG boundary scan into complex stacked multichip modules years before the '243 patent. (*See* INTEL-1022, 44–45.) IC testing has always been a significant cost point in the production cycle for integrated circuits. (*See, e.g.*, INTEL-1017, 2.) Thus, it was critical to implement JTAG boundary scan to test stacked modules because boundary scan reduces the overall cost and complexity of testing and does not require use of external probes.

A POSITA accordingly would have been motivated to and would have known how to implement boundary scan testing into a module.

97. In addition, the functions performed by the Hosomi and Sato references are the same in combination as they are separately. Hosomi acts as SDRAM separately and in the combination and Sato's boundary scan components and wiring operate the same way in combination with Hosomi as they do separately. Indeed, Sato teaches that its disclosed boundary scan technique is used with memory devices. (INTEL-1009, 10:29–11:10.) A POSITA would have further recognized the results of the combination were predictable and would have had a reasonable expectation of success because, as discussed above, use of boundary scan testing for IC assemblies was well-known, standardized, and in wide use before the '243 patent.

98. Finally, a POSITA would have understood the combination of Hosomi and Sato amounts to applying known techniques to a known device ready for improvement to yield predictable results. Hosomi discloses a "base" device—a stacked SDRAM module—upon which Sato's boundary scan architecture is directly applicable to provide testing capability without probes. A POSITA would have considered the combination to be an improvement to Hosomi because chips manufactured with built-in terminals that support boundary scan testing have the capability to be tested for faulty interconnections at the same time and using the

same test vectors with minimal extra design effort and cost. As a result, Sato disclosed a known technique—boundary scan for stacked chips/modules—that is directly applicable to Hosomi’s base device (stacked assembly). A POSITA would have recognized that this known technique would have yielded predictable results and resulted in an improved system free of interconnection faults.

B. Independent Claim 1

[1P] A stacked module comprising

[1A] a plurality of modules each comprising:

[1B] one or more active ports for carrying one or more active signal;

[1C] one or more passive ports for passing through the one or more active signals;

[1D] a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

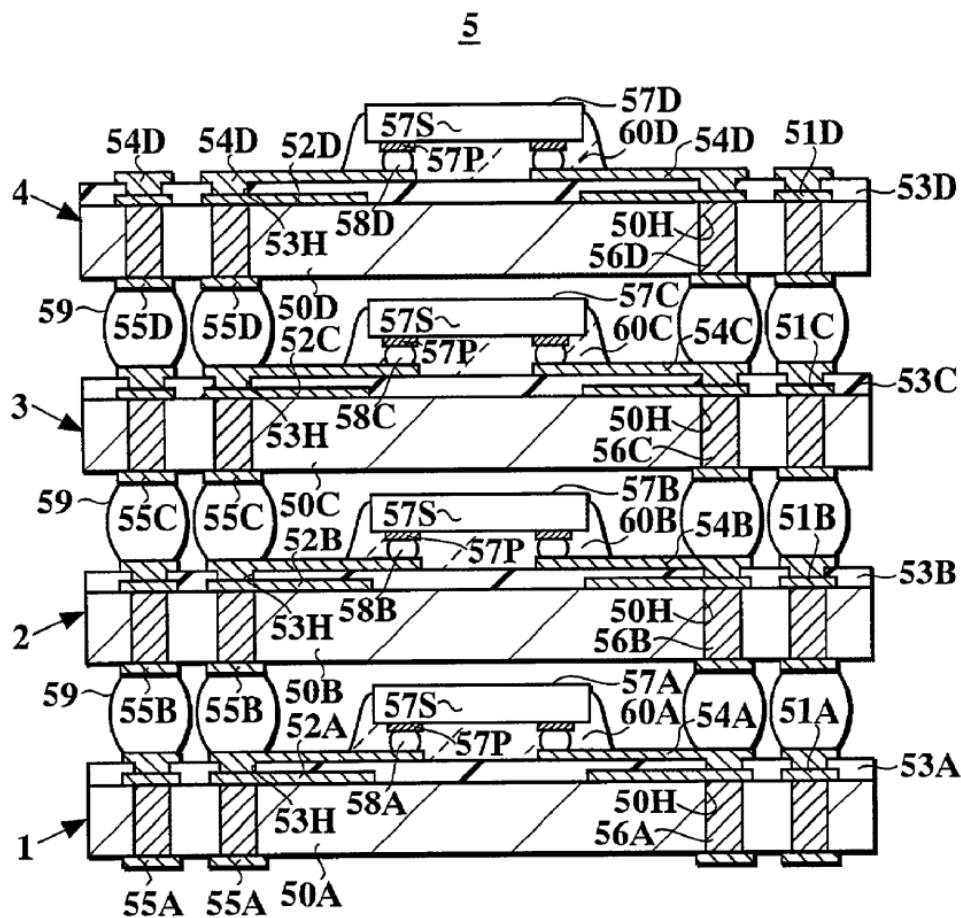
[1E] a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

[1F] said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

1. Preamble [1P] and “*Plurality of Modules*” [1A].

99. Hosomi discloses a semiconductor module 5, illustrated below, comprising a stack of semiconductor devices 1 to 4 (each device is referred to

herein as a module). (INTEL-1007, ¶89) Semiconductor devices (modules) 2 to 4 “are substantially identical” to semiconductor device (module) 1 and are each “constituted by an SDRAM system.” (INTEL-1007, ¶¶89, 74.) Semiconductor devices (modules) 1-4 are each a “*module*” of the stacked module 5 because each includes a chip connected to a substrate. Hosomi therefore discloses a “*stacked module*” [1P] that comprises “*a plurality of modules*” [1A].



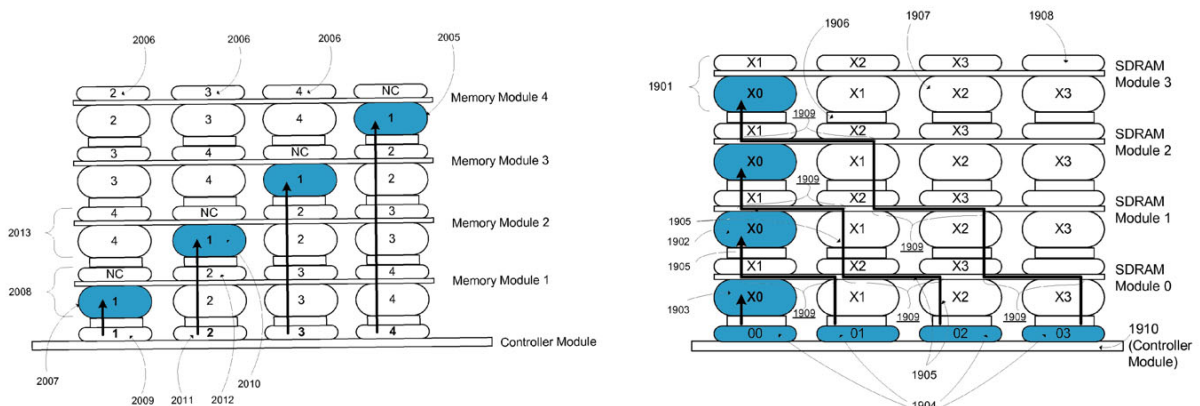
Hosomi, Figure 5

2. “One or More Active Ports” [1B].

100. The combination of Hosomi and Sato discloses “*one or more active*

ports for carrying one or more active signal” [1B]. The ’243 patent does not define the term “active port,” but the COC indicates “[a]n **active pad** may be also referred to herein as an ‘**active port**.’” (INTEL-1001, 9:2; INTEL-1005, 1.)

The ’243 patent also does not define the term “active signal.” In connection with Figure 20b, the ’243 patent describes Pins 1 (shaded blue) which receive signals at a module as “**active signal** pins for the module.” (See INTEL-1001, 9:47–49.) The COC added that an “active signal” is “applied at an **active pad**, such as active pad 02, shown with reference number 1904 [shaded blue] on controller module 1910” and “eventually reaches an active ball, such as [an] X0 ball [shaded blue].” (See INTEL-1001, 9:12 (as modified by COC); INTEL-1005, 2; *see also*, INTEL-1001, Figure 19 (below right).) Once an active signal is received, for example, at one of the ports X0 of Figure 19, it is distributed to the circuitry on that module. (See, *e.g.*, INTEL-1001, Figure 21b.)

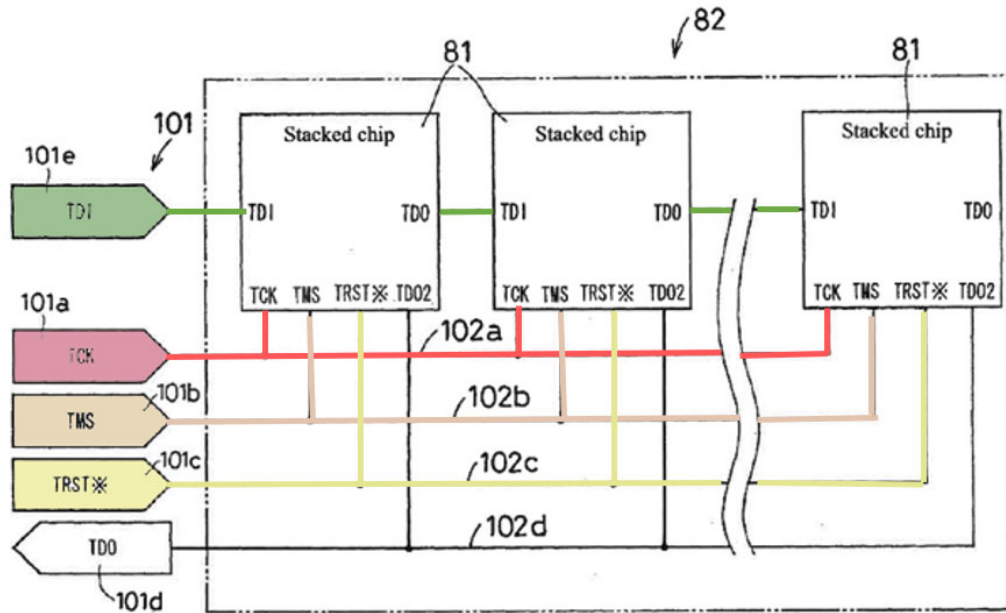


’243 Patent, Annotated Figures 20b (left), 19 (right)

101. The '243 patent therefore uses the term “port” broadly as either an entry or exit to/from a module or to/from a circuit or chip on the module. And an “*active signal*” as disclosed in the '243 patent encompasses a signal applied to the stack by an external source that is received at an “*active port*” of a module and distributed via an “*active port*” to circuitry on the module, which is consistent with the blue-shaded pads/ports shown in Figures 19 and 20b above.

102. Sato discloses numerous “*active signals*” carrying information and used by a boundary scan controller, including TDI (data input), TCK (clock), TMS (test mode select input), and TRST (test reset input). (*See* §II.A.6.) In the stacked module of the combination of Hosomi and Sato having a boundary scan controller in each module and using daisy-chain connections as taught by Sato, the TDI active signal (shaded green) is applied to the bottom controller (leftmost) by an external JTAG tester. (INTEL-1009, Figure 3 (below).) The TDO output of the bottom controller is connected to the TDI input of the controller in the next module in the stack. (INTEL-1009, 20:24–27.) The TDO output of that layer is in turn connected to the TDI input of the next module, and so on until the top controller (rightmost) is reached. Signal lines TCK (shaded red), TMS (shaded orange) and TRST (shaded yellow) are distributed through the stack to the controller in each module of the stack via identical bus lines 102a, 102b and 102c. (INTEL-1009,

20:20–23.) I discuss the TDI and TCK signal path in further detail in the next sections.



Sato, Annotated Figure 3

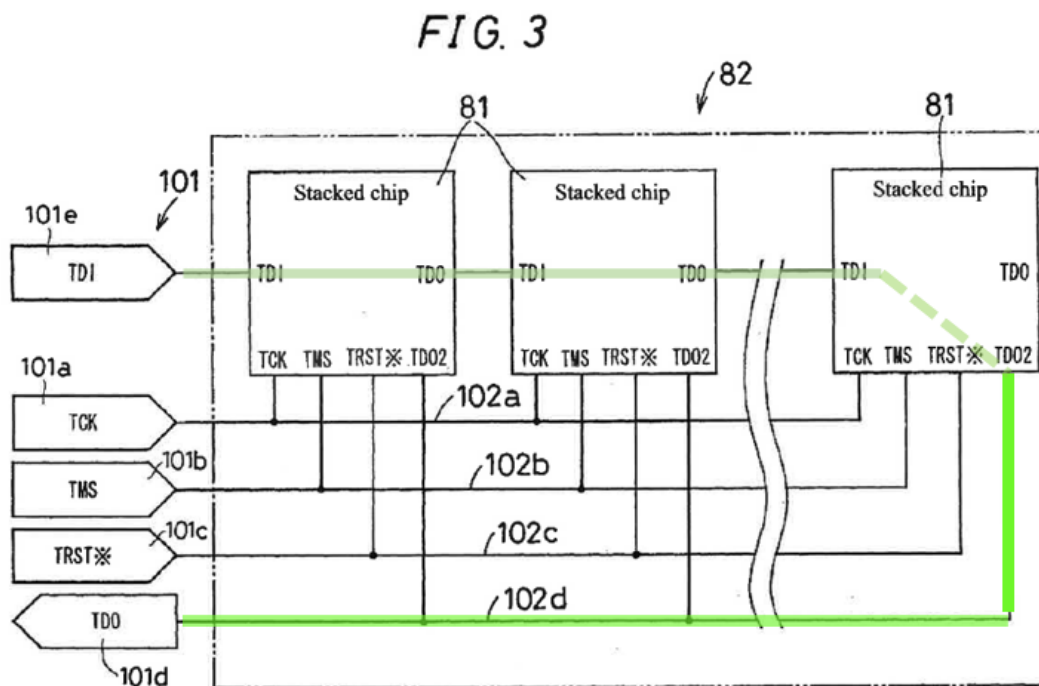
a) TDI Active Signal Path

103. With respect to the TDI daisy-chain connection shown below, Sato teaches that (i) the TDI signal is routed from an external JTAG tester (not shown) connected to the TDI pin 101e at the base of the stacked module through the daisy chain through the stack, and (ii) the TDO2 signal is routed from the top controller back down the stack to the external JTAG tester connected to TDO pin 101d at the bottom of the stack.

The semiconductor device 82 is configured by stacking the semiconductor circuit chip assemblies 81 as described above. In Fig. 3, the semiconductor circuit chip assemblies 81 which are indicated in a region enclosed in a phantom line are stacked. Hereinafter, stacked

semiconductor circuit chip assemblies 81 will be sometimes be referred to as a “multilayer module”. A connector 101 is disposed in the semiconductor device 82, and the JTAG tester is connected to the connector 101. The semiconductor circuit chip assemblies 81 which are stacked at the lowermost stage, middle stage and uppermost stage in succession from the left are illustrated in Fig. 3. ... The signal lines TCK of the respective semiconductor circuit chip assemblies 81 are connected to the same bus line 102a, and are interconnected with the corresponding TCK pin 101a of the connector 101. Similar to the signal lines TCK, the signal lines TMS, TRST and TDO2 are respectively connected to identical bus lines 102b, 102c and 102d and are mutually connected to the corresponding TMS pin 101b, TRST pin 101c and TDO2 pin 101d of the connector 101 in parallel.

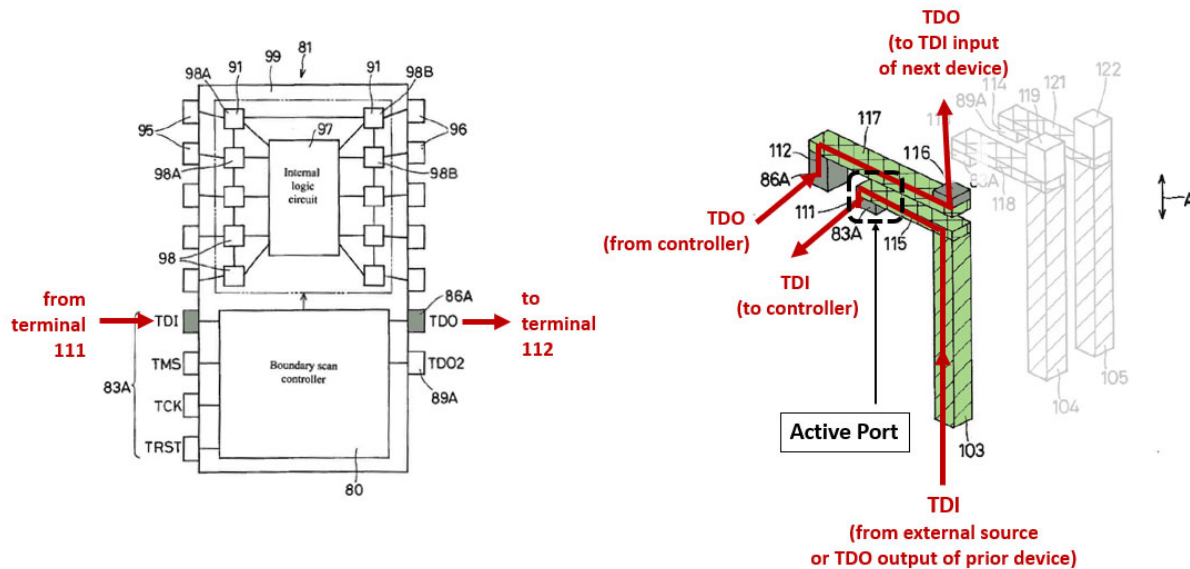
(See INTEL-1009, 20:7–23.)



Sato, Annotated Figure 3

104. In the TDI signal path of Sato’s daisy-chain connection illustrated in Figure 5 below, the TDI signal passes through electrode 103 (shaded green) to

terminal 111 via connection line 115 (shaded green). (INTEL-1009, 23:26–27; Figure 5 below right.) The active TDI signal is then communicated from terminal 111 (shaded gray) to the TDI input (83A) of the boundary scan controller via a connection line. (See INTEL-1009, Figure 2 below left.)



Sato, Figure 2 (left), Figure 5 (right)

105. A POSITA would have understood a “terminal” to be a conductive pad on the substrate that terminates a conductive path. Terminal 111 is an “*active port*” because it comprises a pad that distributes the TDI active signal to the boundary scan controller. (INTEL-1001, 9:3 (as modified by COC) (“An **active pad** may be also referred to as an ‘**active port**’”); INTEL-1005, 1.) The TDO output of the controller is provided to terminal 112 (86A) (shaded gray) which is

“interconnected with the first connection terminal 116 through the second communication line 117.” (INTEL-1009, 23:32–24:2.)

106. The diagram below illustrates application of Sato daisy chain connection of Figure 5 to the substrate of each module in the stacked module. (See INTEL-1009, 23:5–25:10.) As I discussed in §III.A.3, the daisy-chain connection is implemented (1) using Hosomi’s vias as vertical electrodes of Sato, Hosomi’s pads as Sato’s terminals, and Hosomi’s wiring layers to form Sato’s interconnections and (2) connecting modules using the pad and ball connections taught by Hosomi.

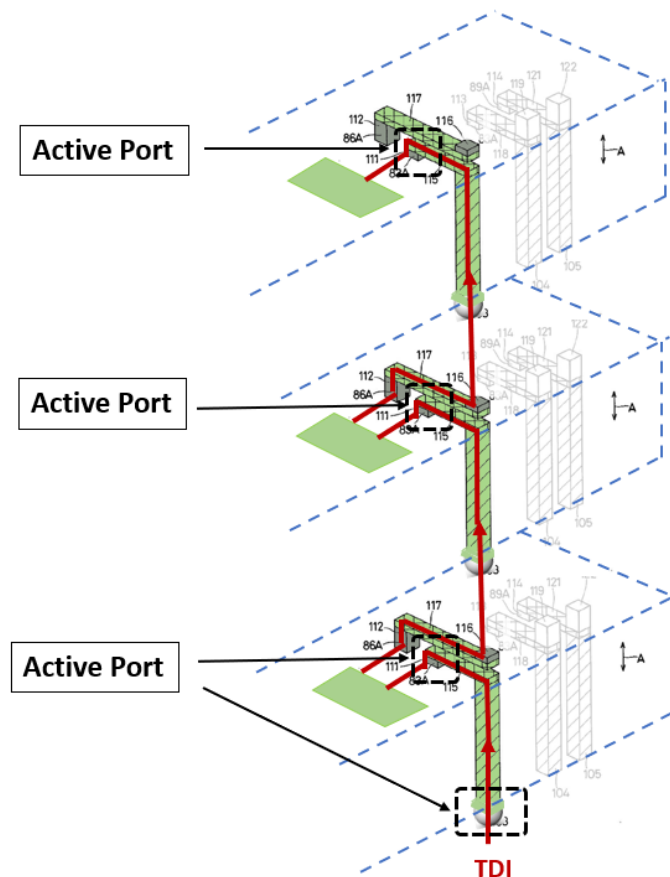


Figure A: Stacked Module of Hosomi and Sato—TDI Signal Path

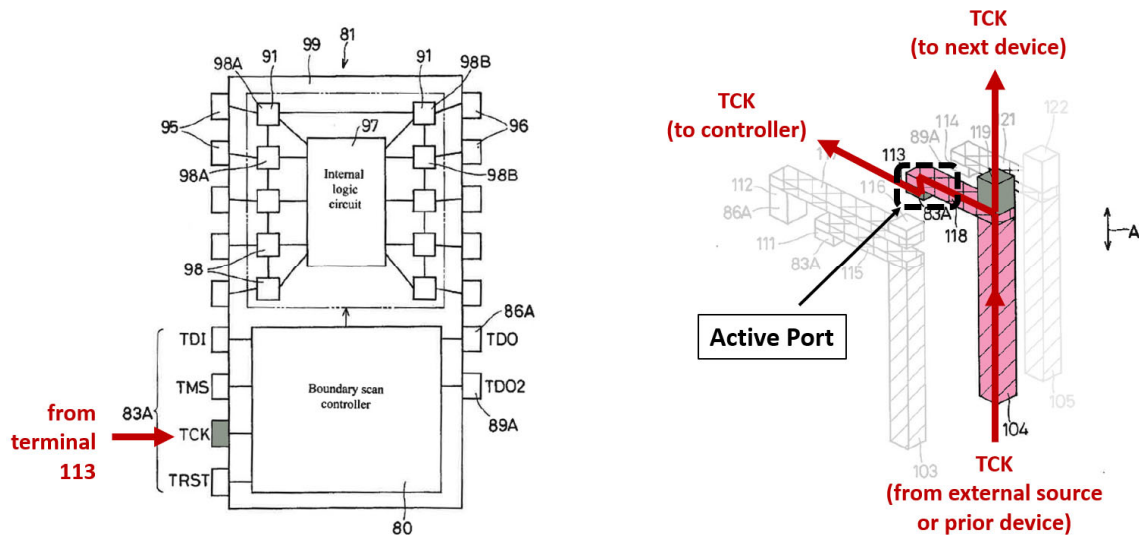
107. In the “*stacked module*” of the combination, the bottom module receives the TDI signal from an external JTAG tester. A POSITA would have understood that the “*stacked module*” is mounted to a circuit board. The JTAG testing signals are applied to the stacked module via connector 100 associated with the JTAG tester. Further, as discussed above, Hosomi utilizes solder bumping for making vertical interconnections between the stacked layers, which was the preferred and most popular method for implementing access point connections on a printed circuit board. (See §II.A.3(b).) A POSITA would have understood that using solder bumping’s pad-via-ball structure for this purpose provides a number of advantages over other packaging methods. For example, pad-via-ball connections can (i) accommodate a larger number of signal pins for high-density circuits, (ii) provide real estate reductions because signal pads can be placed over the entire face of the die, (iii) reduce wiring length, which reduces parasitic capacitance and inductance in the lines, and (iv) simplify the manufacturing process. Thus, a POSITA would have been motivated to utilize Hosomi’s solder bumps to connect the bottom module to a circuit board.

108. The pad/ball receiving the TDI signal at the bottom module is an “*active port*” because it receives the TDI signal from the external JTAG tester. As shown in the diagram above, TDI travels through the daisy-chain path of the bottom module to terminal (pad) 116 which is coupled to the pad/ball connection at

the end of electrode (via) 103 in the adjacent module in the stack. TDI continues up the stack through the daisy-chain connections at each module until it reaches the boundary scan controller in the top module. Terminal (pad) 111 in each module distributes TDI to the controller in that module. Therefore, each module includes an “*active port*” at terminal (pad) 111.

b) TCK Signal Path

109. In Sato, the TCK signal passes through electrode 104 and “is interconnected to the terminal 113 ... through the third connection line 118.” (INTEL-1009, 24:3–4; Figure 5 below right.) TCK is then provided from terminal 113 to the TCK input of the controller via a connection line. Terminal 113 is an “*active port*” because it comprises an active pad that distributes the active signal TCK via terminal 113 for use by the controller circuitry at each layer in the stack.



Sato, Figure 2 (left), Figure 5 (right)

111. TMS and TRST have similar signaling paths as TCK in the combined “*stacked module*.” Therefore, each module further includes a set of “*active ports*” carrying these signals.

112. Thus, for each of the above reasons, the combination of Hosomi and Sato discloses each module in the “*stacked module*” includes “*one or more active ports for carrying one or more active signal*” [1B], as required by Petitioner’s “*plurality of modules*” construction. The combination also discloses the “*stacked module*” includes “*one or more active ports for carrying one or more active signal*” [1B], as required by the PO’s construction.

3. “*Passive Port*” [1C].

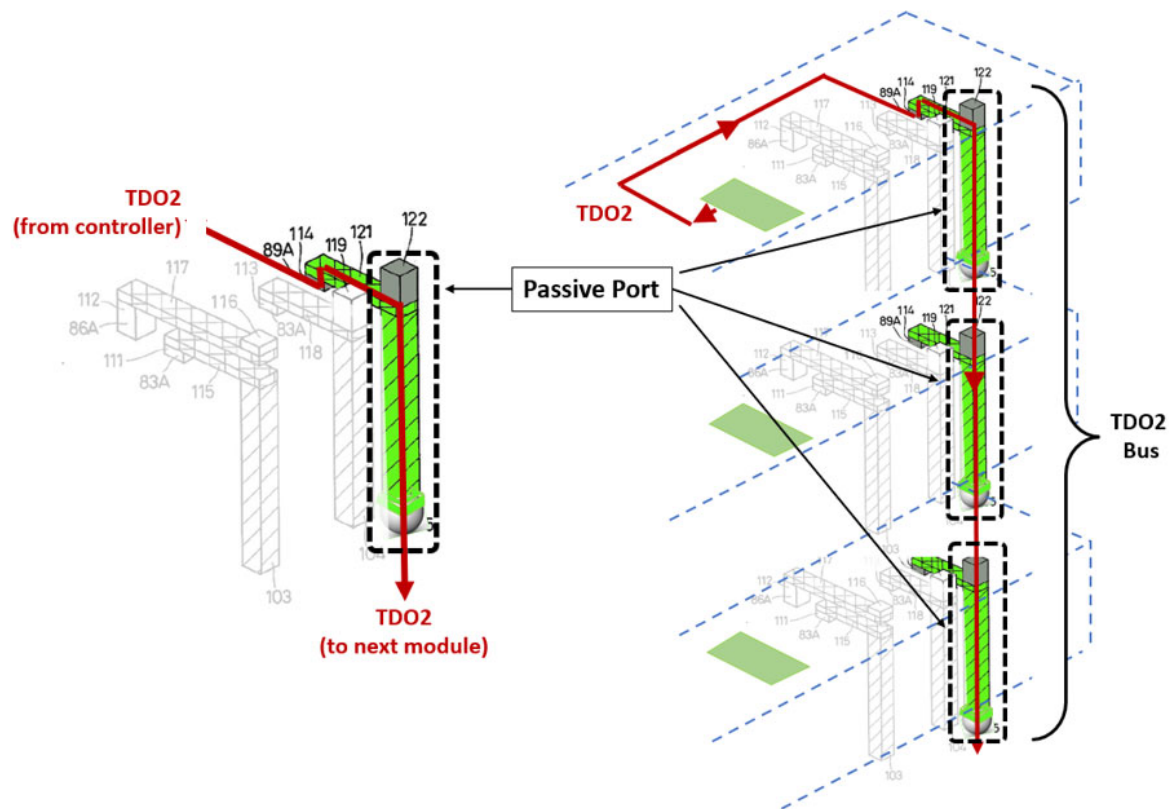
113. Limitation [1C] recites “*one or more passive ports for passing through the one or more active signals.*” As set forth below, the combination of Hosomi and Sato teaches multiple “*passive ports*” for passing through active signals such as TDI, TCK and TDO2. Petitioner contends the proper construction of a “*passive port*” is the “connection between a passive ball on one surface of an SDRAM module and a passive pad on another surface of the same SDRAM module.” (See §II.E.2.) The Patent Owner (“PO”), in contrast, contends a “*passive port*” is simply any “connection between a passive ball and a passive pad.” As set forth below, the combination of Hosomi and Sato discloses this limitation under

114. As shown in Figure 3 below, in the combination of Hosomi and Sato, the controller in the top SDRAM module in the stacked module outputs the TDO2 signal (shaded bright green) to bus 102d (“TDO2 bus”), which passes the TDO2 signal back down through the stack to the external JTAG tester connected to the connector 101. The TDO2 signal is an “*active signal*” because it carries the output data of boundary scan of the stacked module.



- 73 -

scan controller is transmitted to terminal 114 (89A), and in turn to terminal 122 through connection line 121. (INTEL-1009, 24:10–11.) The TDO2 signal then passes from terminal 122, through electrode 105, to the pad/ball structure at the bottom electrode, which is connected to terminal 122 of the next module lower in the stack, and so on. The path from terminal 122 in the top device down through the stack to a pad carrying TDO2 to the external JTAG tester is the TDO2 bus.



Sato, Annotated Figure 5, Top Device (left)
Figure C: Stacked Module of Hosomi and Sato-TDO2 (right)

116. The figure above at right includes the TDO2 portion of the daisy-chain connection in each module of the stacked module. As shown, TDO2 passes

from terminal (pad) 122, through electrode (via) 105, to the pad/ball structure at the bottom of the module which is connected to terminal (pad) 122 of the next module in the stack. This structure comprises a “*passive port*” under both constructions because it passes active TDO2 signals from a terminal (pad) to a ball on the opposite side of one of Hosomi’s stacked SDRAM chips, and subsequently to the next module in the stack (top/middle module) or to the external JTAG tester (bottom module) mounted on the main circuit board at the bottom of the stack.

117. Thus, the combination Hosomi and Sato discloses that each module in the “*stacked module*” includes “*one or more passive ports for passing through the one or more active signals*” [1C], as required by Petitioner’s “*plurality of modules*” construction. The combination also discloses the entire “*stacked module*” includes “*one or more passive ports for passing through the one or more active signals*” [1A], as required by PO’s construction.

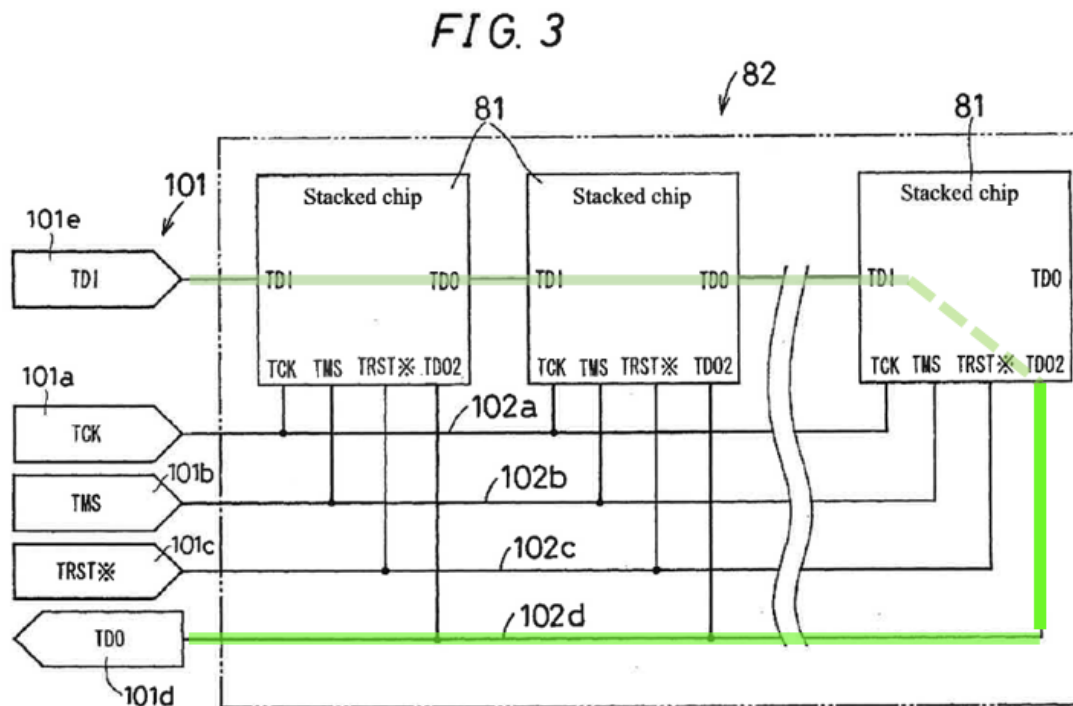
4. “*First Serial Chain Route*” [1D].

118. As set forth below, the daisy-chain path in the combination of Hosomi and Sato comprises “*a first serial chain route that includes at least one serial chain connection*” [1D]. Sato discloses a path for routing scan chain testing data through its stacked chips, which interconnects the boundary scan controllers 80 at each layer:

The output part connection terminals 86A of the semiconductor circuit chip assemblies 81 on the preceding stage sides are

successively connected to the input part connection terminals 83A corresponding to the signal lines TDI of the semiconductor circuit chip assemblies 81 on the succeeding stage sides. ... In this manner, the semiconductor device 82, the individual controllers 80 are connected **in the shape of a chain**. Hereinafter, **the chain-like connection is sometimes referred to as a ‘daisy chain’....**”

(INTEL-1009, 20:24–21:4, Fig. 3.)



Sato, Annotated Figure 3

119. In Sato’s daisy-chain path shown in Figure 3 above, test data is input to the TDI signal line of the bottom (leftmost) controller from an external JTAG tester coupled to connector 101. The TDO output of the controller in the bottom module is connected to the TDI input of the controller in the next module in the stack (e.g., the middle module). (INTEL-1009, 20:24–27; Figure 3 below.) The TDO output of that controller is connected to the TDI input of the controller of the

next module in the stack, and so on until the top (rightmost) controller is reached. (INTEL-1009, 20:24–27.) This path from the TDI input of the controller in the bottom module to the TDI input of the controller in the top module includes multiple “*serial chain connections*.”

a) “Serial Chain Connection”

120. The daisy chain path includes at least two “*serial chain connection[s]*” in each stacked module—a vertical serial chain connection and at least two horizontal serial chain connections. In particular, the combination of Hosomi and Sato discloses two alternative serial chain connections in each module in the stack: (i) a pad-via-ball vertical serial chain connection path formed in the TDI-TDO daisy chain between adjacent stacked modules; and (ii) horizontal serial chain connections formed through the boundary scan controller on each module in the stack.

121. **Vertical “Serial Chain Connection”:** The figure below illustrates Sato’s daisy chain connection applied to a module substrate of Hosomi. As shown, the TDI signal is applied to the pad/ball connection formed on the bottom surface of the module’s substrate and passes through electrode (via) 103 and the first connection line 115 to terminal 111 as shown below. (See INTEL-1009, 23:26–27.) In the bottom layer of the stack, the TDI signal is applied from an external JTAG tester by way of connector 101. (See INTEL-1009, 4:21–24.) In other

modules in the stack, the TDI signal is the TDO output of the preceding layer in the stack. (See INTEL-1009, 4:27–30.)

One surface of the semiconductor circuit chip assembly 81 is formed with the input part connection terminals 83A being the terminals of the input part 83 ... The input part connection terminals 83A are the terminal 111 of the signal line TDI and the terminal 113 of the signal line TCK. ... One end part of the first penetrating electrode 103 is interconnected to the terminal 111 of the signal line TDI through the first connection line 115. The first connection line 115 is formed in one surface of the semiconductor circuit chip assembly 81. ... By laying wiring lines in the manner, data which is input from the exterior of the semiconductor circuit chip assembly 81 is passed through the first penetrating electrode 103 and transmitted to the terminal 111 of the signal line TDI via the first connection line 115. ...

(INTEL-1009, 23:17–24:19)

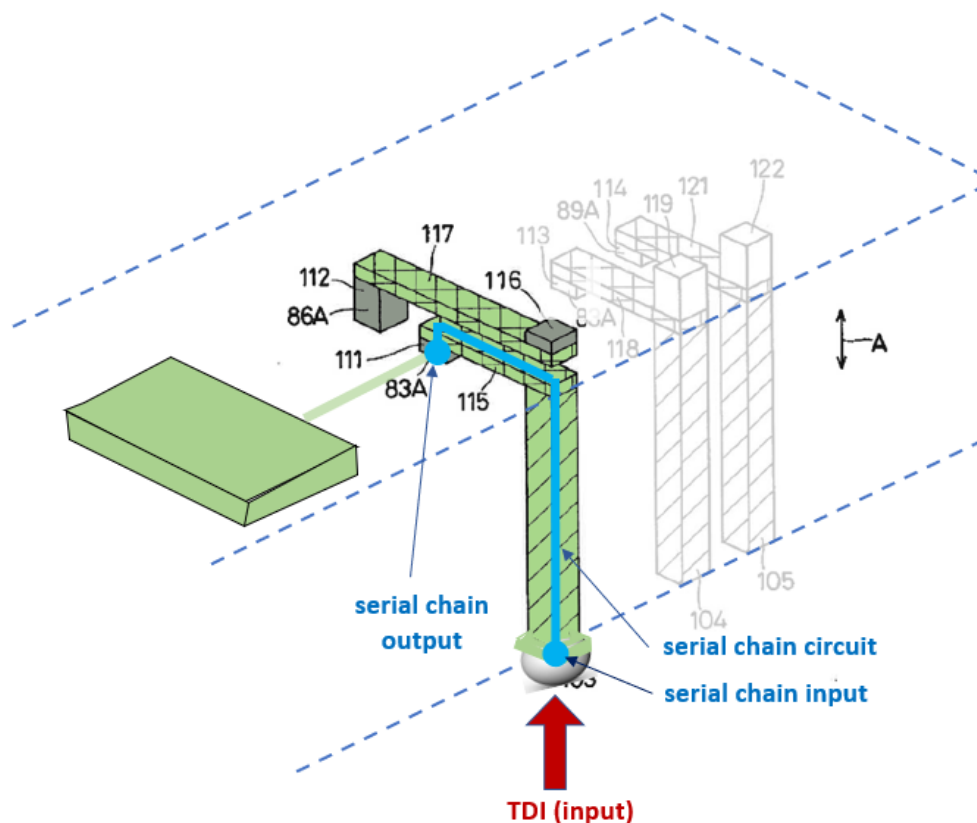


Figure D: Sato's Daisy Chain on Module Substrate

122. The pad-via-ball structure in each module is a vertical “*serial chain connection*” with the ball on the lower surface of the module substrate receiving TDI being a “*serial chain input*”, electrode (via) 103 being a “*serial chain circuit*”, and terminal (pad) 111 on the upper surface providing TDI to the controller (shaded green) being a “*serial chain output*.” (See INTEL-1005, 2 (“A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal”, “serial chain circuit coupl[es] a ball and pad”).) Thus, the combination demonstrates a “*first serial chain route*” as claimed.

123. **Horizontal “*Serial Chain Connection*”:** Each module in the “*stacked module*” of Hosomi and Sato also includes at least two “*serial chain connections*” in the horizontal direction. First, terminal (pad) 111 (shown in the figure below) is connected to the input of the boundary scan controller (shaded green) by way of a circuit trace or other connection line (shaded blue). This horizontal path is a “*serial chain connection*” with terminal (pad) 111 being the “*serial chain input*”, the circuit trace (connection line) being the “*serial chain circuit*”, and the input to the boundary scan controller being the “*serial chain output*.”

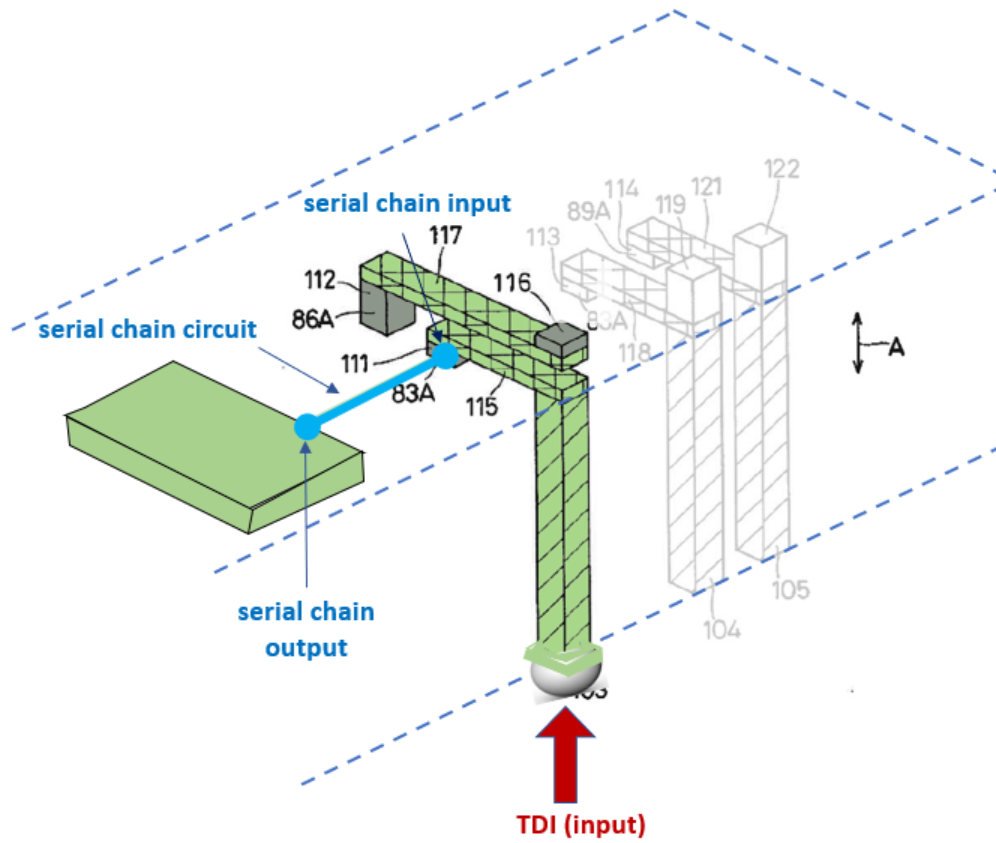


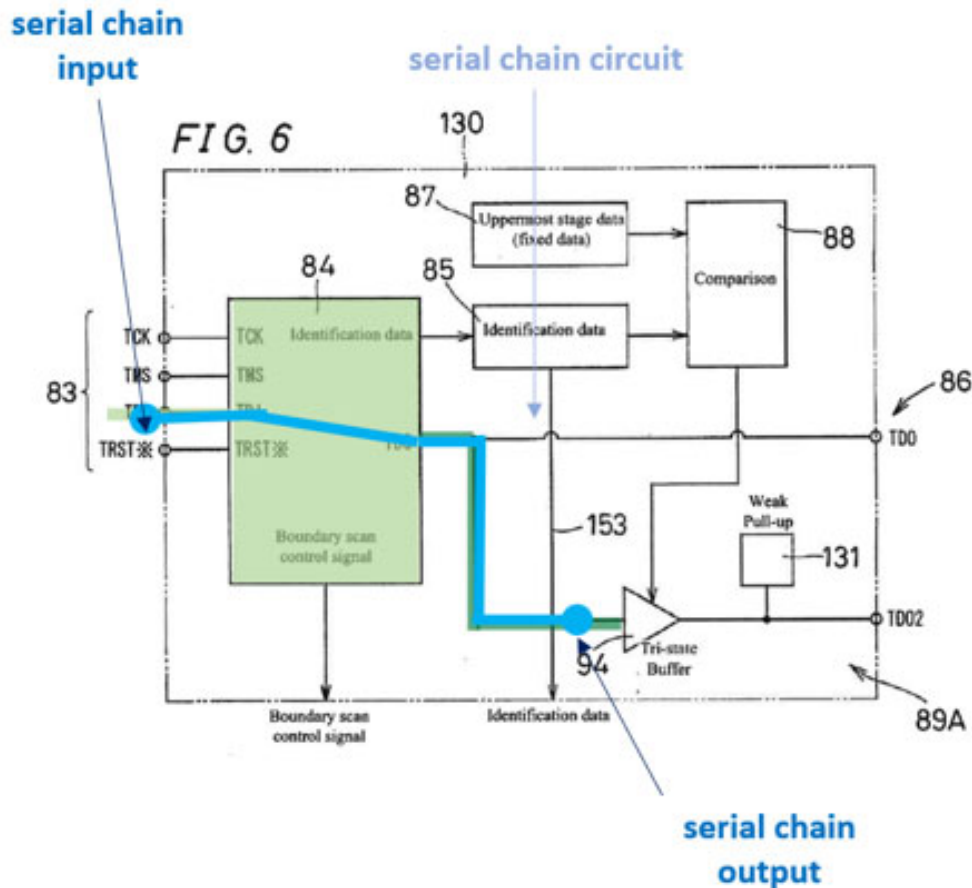
**Figure E: Horizontal “Serial Chain Connection”
Terminal (Pad) 111 to Controller**

124. Second, a horizontal “*serial chain connection*” exists within the boundary scan controller. As shown in Figure 6 (below left), test data input on TDI signal line is output from the TDO signal line through the shift registers (not shown) in control means 84. (See INTEL-1009, 15:4–7.) When the pre-configured identification data for a module matches identification data received during operation, the tristate buffer outputs TDO on signal line TDO2. (See INTEL-1009, 25:19-15.) During a boundary scan, a “match” condition occurs in the top module. Thus, in the top module as shown in Figure 6 (below), the horizontal path from the

TDI input of the controller to the buffer input is a “*serial chain connection*” with the TDI input of the controller being the “*serial chain input*”, the connection through the register of control means to input of the tri-state buffer being the “*serial chain circuit*” and the tri-state buffer input being the “*serial chain output*.”

Fig. 6 is a block diagram illustrating a boundary scan controller 130 in another embodiment of the present invention. The boundary scan controller 130 includes an input part 83, control means 84, storage means 85, an output part 86, fixed data holding means 87, comparison means 88, and a data derivation part 89A. ... If the comparison result information output from the comparison means 88 indicates matching between the identification data and fixed data, **the tristate buffer 94 outputs the same data as the data output from the output part 86.** The input terminal of the tristate buffer 94 is interconnected with the signal line TDO, and the output terminal thereof is interconnected with the signal line TDO2. On the other hand, if the comparison result information which is output from the comparison means 88 indicates mismatching between the identification data and the fixed data, **the tristate buffer 94 is prevented from outputting input data.**

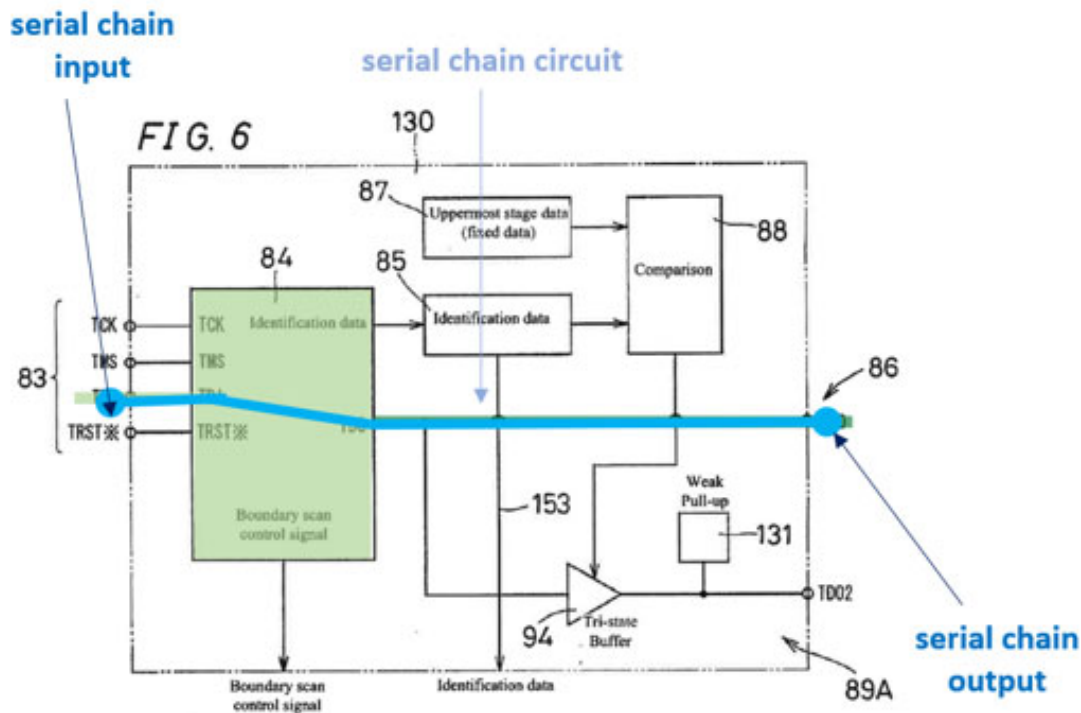
(INTEL-1009, 25:11–28.)



Sato, Annotated Figure 6—Top Module

125. However, when a mismatch condition occurs (*i.e.*, modules other than the top module), “the tristate buffer 94 is prevented from outputting input data.” (INTEL-1009, 25:26–28.) During a boundary scan, a mismatch condition occurs in each controller beneath the top module in the stack. (INTEL-1009, 9:24–26.) Therefore, in these modules, no data is output on signal line TDO2. Instead, the data is output on the TDO. Thus, in these modules as shown in Figure 6 both, the horizontal path from the TDI input of the controller to the TDO output of the

controller is also a “*serial chain connection*” with (i) the TDI input of the controller being the “*serial chain input*”, (ii) the connection through the registers and other circuitry of control means to the TDO output of the controller being the “*serial chain circuit*”, and (iii) the TDO output of the controller being the “*serial chain output*.”



Sato, Annotated Figure 6—Other Modules

b) “*First Serial Chain Route*” – Petitioner’s “*Plurality of Modules*” Construction

126. Petitioner’s “*plurality of modules*” construction requires that each module includes a “*first serial chain route*.” As claimed, the “*first serial chain route*” requires only “*one serial chain connection*.” As shown below, each stacked

module in the combined “*stacked module*” of Hosomi and Sato includes a vertical “*serial chain connection*” that is serially connected to two horizontal “*serial chain connections*.” Thus, the combination of Hosomi and Sato discloses that each module in the stack has “*a first serial chain route that includes at least one serial chain connection*” [1D] as illustrated below in the figure created to illustrate Sato’s boundary scan wiring superimposed on stacked device substrates.

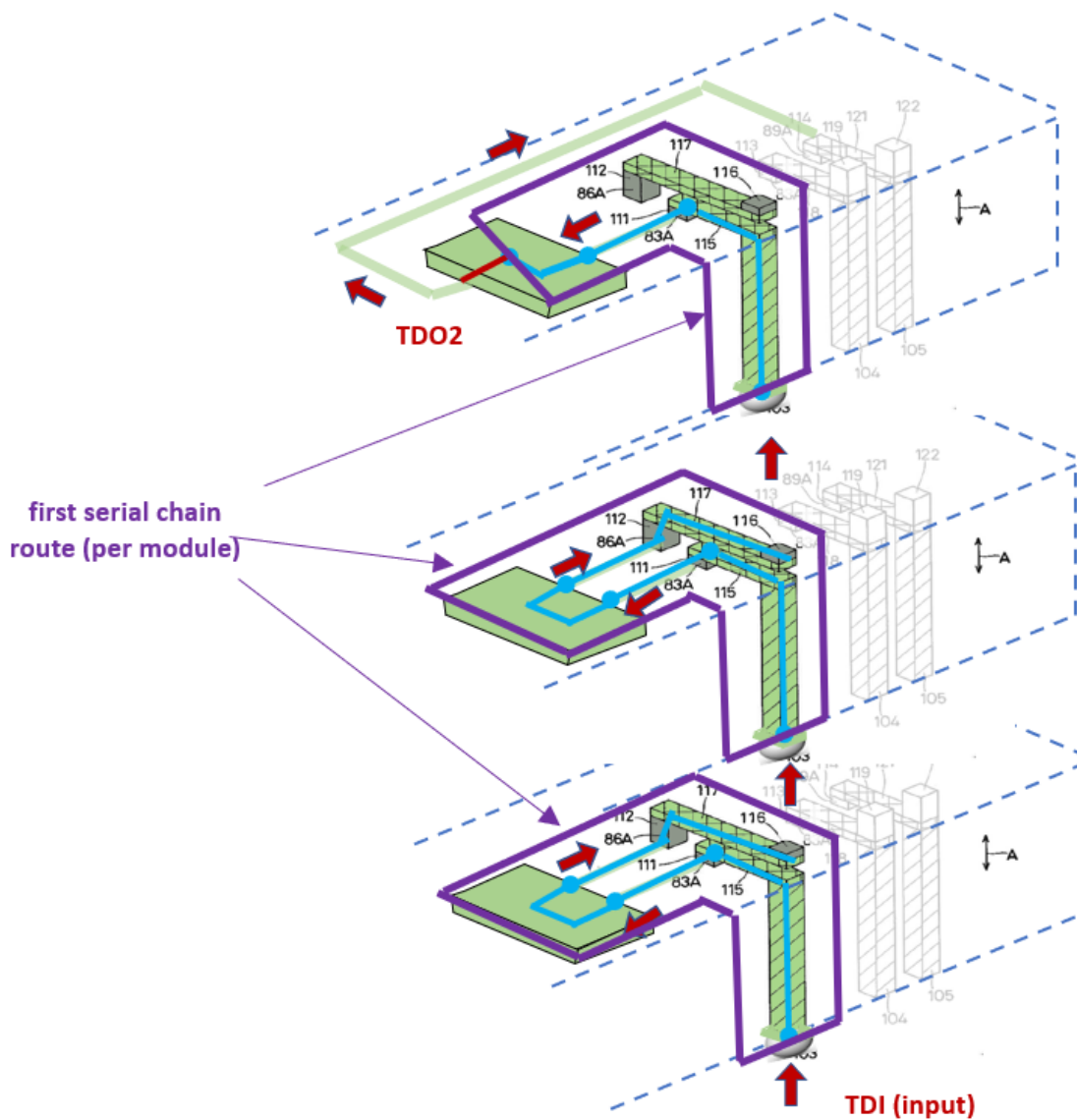


Figure F: Petitioner’s Construction

c) **“First Serial Chain Route”–PO’s “Plurality of Modules” Construction**

127. PO’s “*plurality of modules*” construction only requires the “*stacked module*” to include a “*first serial chain route*.” The “*stacked module*” includes multiple “*serial chain connections*” because each module includes a vertical and two horizontal “*serial chain connections*”, as discussed in §III.B.4(a), *supra*, which is shown in figure below created by Petitioner.

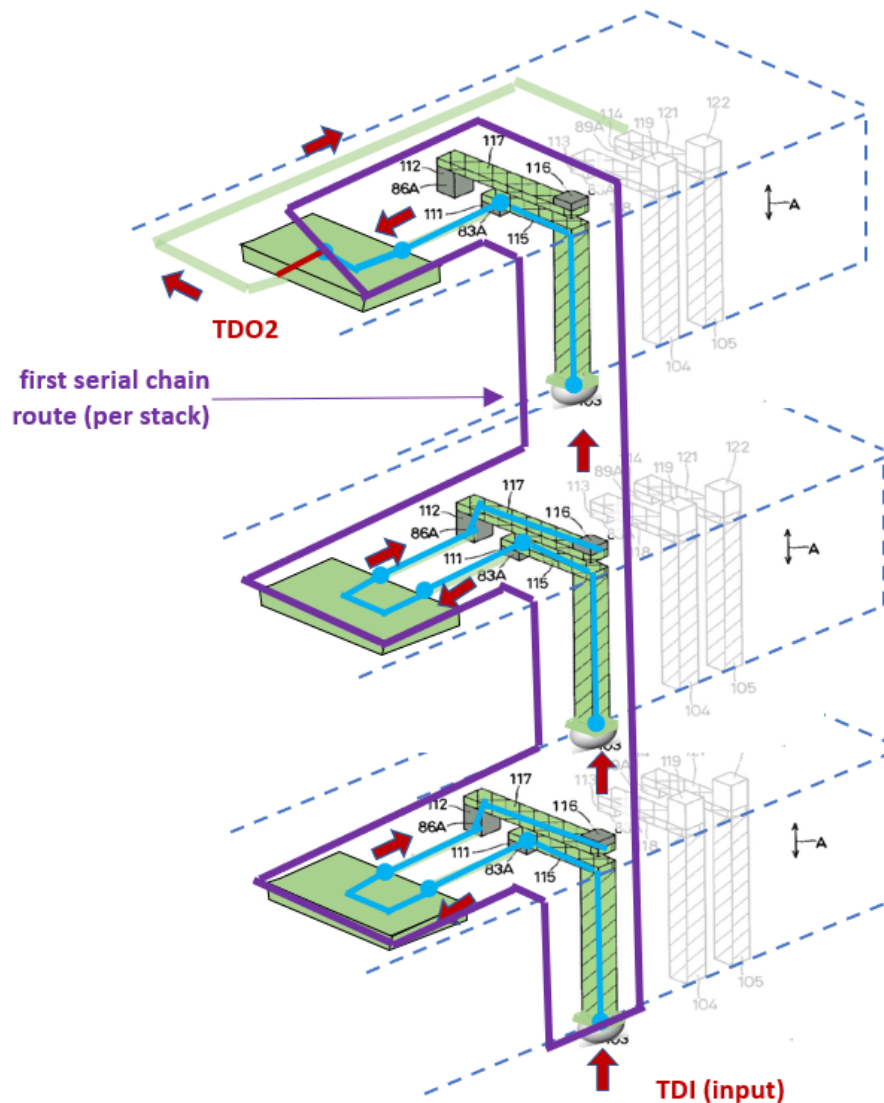


Figure G: PO’s Construction

128. Thus, the combination of Hosomi and Sato discloses that the “*stacked module*” includes “*a first serial chain route that includes at least one serial chain connection*” [1D] under PO’s construction.

5. “*Second Serial Chain Route*” [1E] and “*Control Circuit*” [1F].

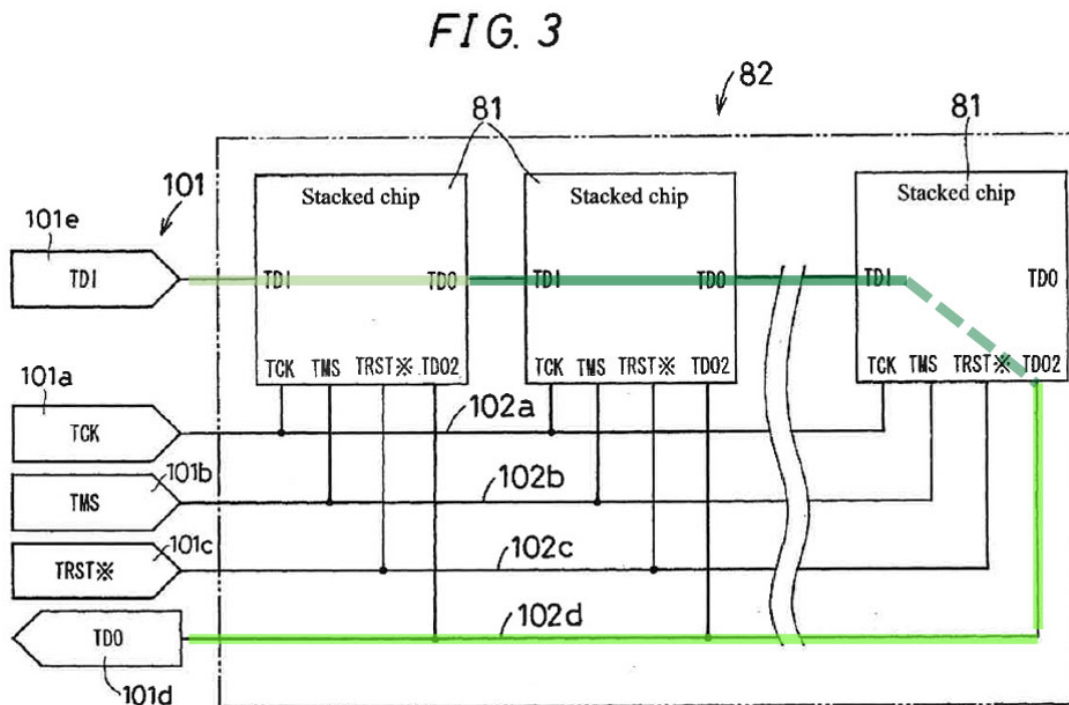
129. Petitioner’s construction requires that **each** of the stacked modules include the recited limitations. As set forth below, the combination of Hosomi and Sato discloses—at each stacked layer—a “*second serial chain route*” and a “*control circuit*” that enables a routing path connecting the first and second serial chain routes within the top module (“*end module*”) of the stack, in accordance with Petitioner’s construction.

a) “*Second Serial Chain Route*” [1E].

130. The combination of Hosomi and Sato discloses a “*second serial chain route.*” Unlike the “*first serial chain route*” [1D], the “*second serial chain route*” limitation [1E] does not recite that it includes “*at least one serial chain connection.*” Notwithstanding, the combination of Hosomi and Sato discloses a “*second serial chain route*” that includes one or more serial chain connections at each stacked layer in accordance with both parties’ “*plurality of modules*” construction.

131. During a boundary scan, illustrated in Figure 3 below, in the top (rightmost) controller, the TDI input data is output to the TDO2 signal line which

is connected to bus 102d (shaded bright green) and output to the external JTAG tester. (See Sato, 19:21–23, 20:20–23.)



Sato, Annotated Figure 3

132. **Petitioner’s “Plurality of Modules” Construction:** The TDO2 portion of the daisy chain connection in the combination of Hosomi and Sato is illustrated in Figure H created by Petitioner to illustrate the TDO2 path in the stacked module of the combination. As shown, in each module, the TDO2 signal passes through terminal (pad) 122, electrode (via) 105, and connecting ball to either the next module in the stack or to the external tester (not shown). As shown below, the pad-via-ball structure in each module in the combination of Hosomi and Sato comprises a “serial chain connection” and each device therefore has a

“second serial chain route” as required by Petitioner’s “plurality of modules” construction.

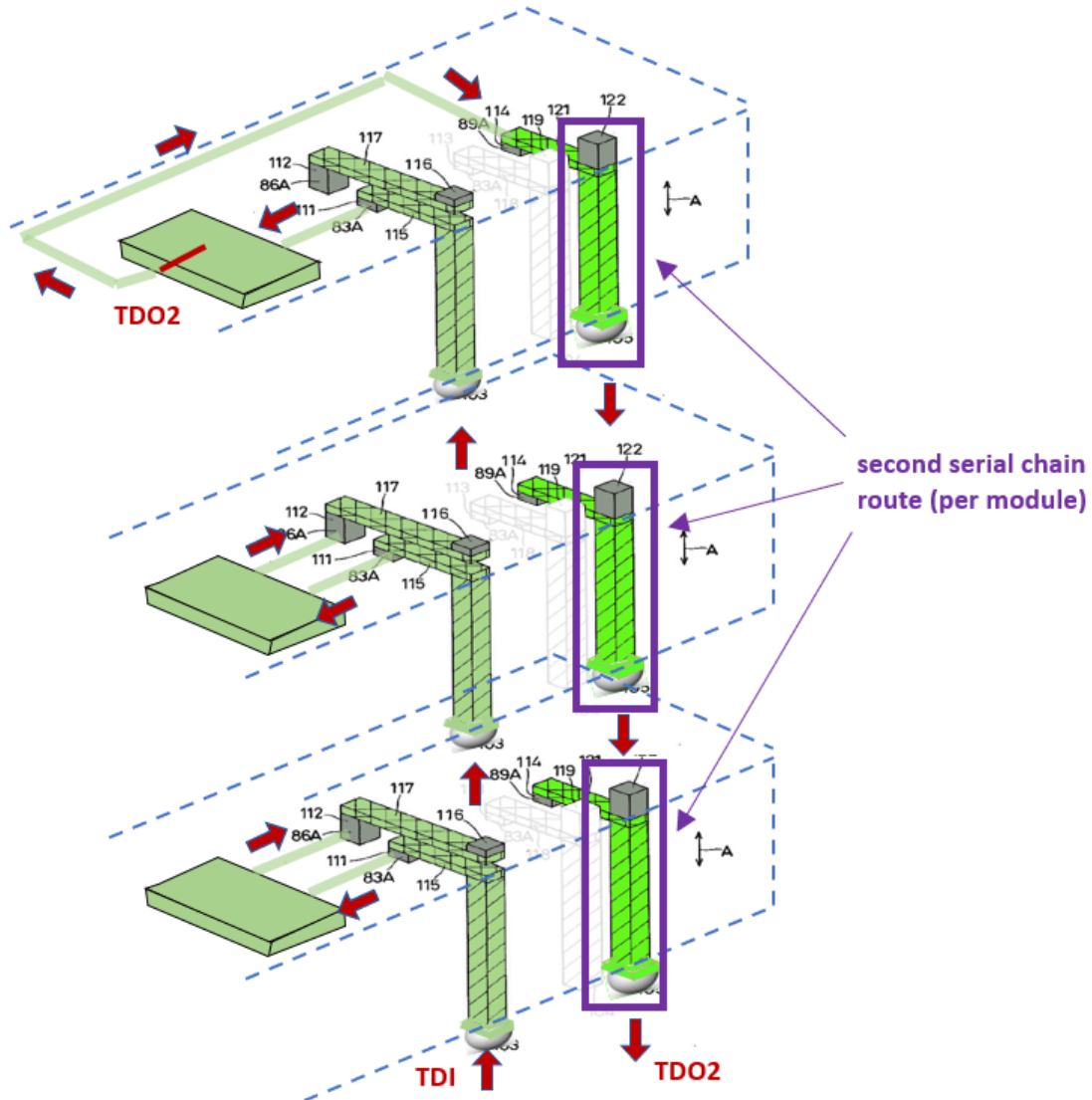


Figure H: Petitioner’s Construction

133. PO’s “*Plurality of Modules*” Construction: The “*stacked module*” includes a path for carrying TDO2 down the stack to the external tester comprising multiple “*serial chain connections*” (pad-via-ball structures), as shown below in

Figure I below created to illustrate the TDO2 portion of the daisy-chain connections in the combined stacked module.

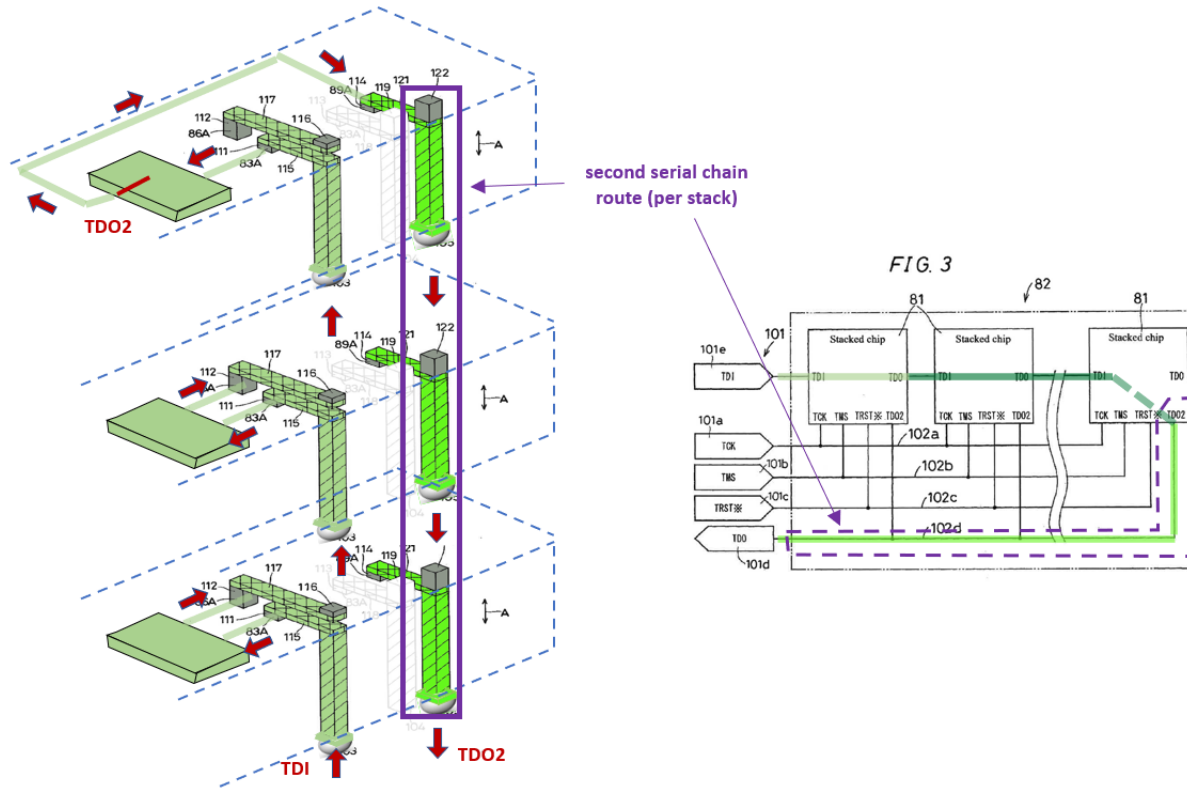


**Figure I (left): PO's Construction (left)
Sato, Annotated Figure 3 (right)**

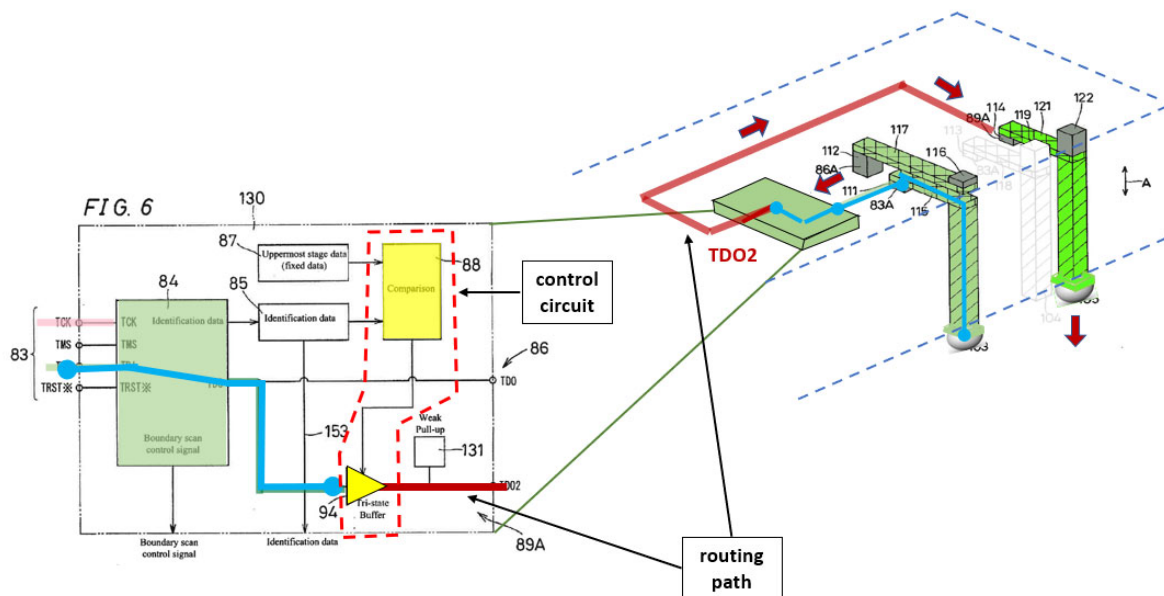
134. Thus, the combination of Hosomi and Sato discloses “a second serial chain route” under PO’s construction requiring a single “route” for the “stacked module” in accordance with PO’s “plurality of modules” construction.

b) Control Circuit Limitations

(1) “Control circuit”

135. The combination of Hosomi and Sato discloses “a control circuit for enabling a routing path” [1E]. The data derivation part 89A of the boundary scan

controller includes tristate buffer 94, pull-up means 131 and signal line TDO2. (INTEL-1009, 25:19–20; Figure 6 (below left).) The comparison means 88 and tristate buffer 94 (shaded yellow) in each controller are part of the “*control circuit*” because they coordinate to control the enabling/disabling of the tristate buffer, which determines whether a routing path is enabled to output data onto the TDO2 signal line.



Sato, Annotated Figure 6 (top module); Annotated Figure 5

136. Sato’s “*control circuit*” also indicates whether the module is the top module (“*end module*”) in the stack by comparing the fixed data stored in each layer of the stack with the identification data provided by over the TDI signal line during operation. The fixed data stored in each assembly is the identification data of the chip at the top layer of the stack:

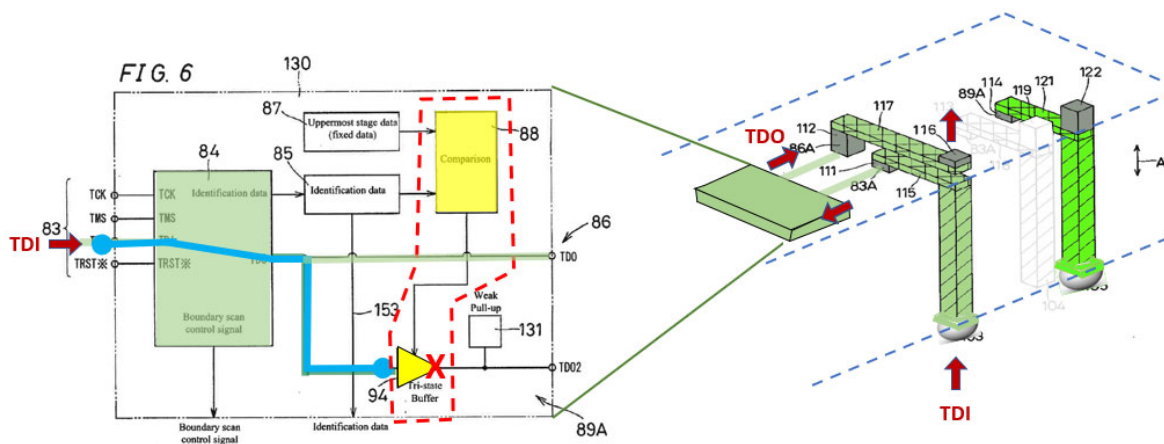
The fixed data holding means 87 holds fixed data. The fixed data is the identification data of the semiconductor circuit chip **which is provided at the uppermost stage when the semiconductor device 82 is configured** by stacking the plurality of semiconductor circuit chip assemblies 81, each configured with the controller 80 disposed in the semiconductor circuit chip. The semiconductor circuit chip which is provided at the uppermost stage is located at the furthest position from a circuit board when the semiconductor device 82 is mounted on the circuit board.

(INTEL-1009, 16:1–7.)

137. The comparison means 88 compares the identification data received during operation with fixed data 87 pre-configured for the module and outputs the comparison result, which is used as the control input to enable or disable the tristate buffer 94. (INTEL-1009, 16:12–15.) During a boundary scan, the identification data matches the fixed data only in the top module (*i.e.*, the “boundary” of the stack). (INTEL-1009, 9:24–26.) Thus, in the top module (an “*end module*” for the stack), the comparison results in a match that produces a control signal from the comparison means 88 that enables the tristate buffer, causing the TDO output of control means 84 (shaded blue in the diagram above) to be output onto signal line TDO2 (shaded red in the diagram above). (See INTEL-1009, 19:21–23.) When this happens, the signal line TDO2 from the controller connects to terminal (pad) 114 on the module substrate and then to terminal (pad) 122 through connection line 121. The path from the tristate buffer output to terminal (pad) 122 is a “*routing path*” for boundary scan data from the controller to

the TDO2 bus.

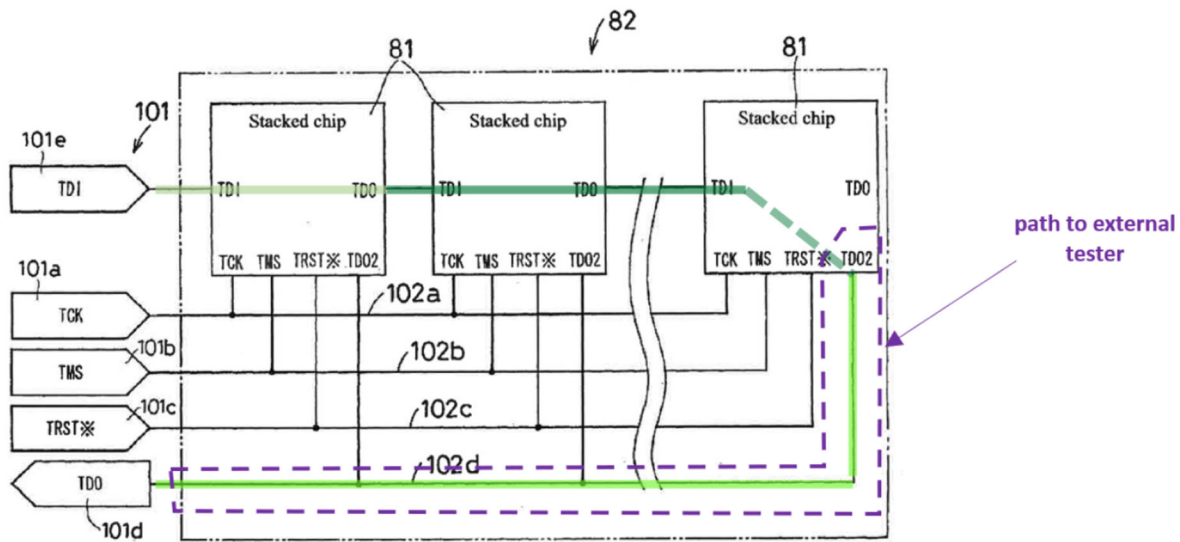
138. In the other modules, as illustrated below, the comparison result (mismatch condition) prevents tristate buffer 94 from outputting the TDI input data onto the signal line TDO2, and therefore prevents output of data on the path to terminal (pad) 122. (See INTEL-1009, 25:26–28.) The routing path is not enabled in modules other than the top module.



Sato, Annotated Figure 6 (other modules); Annotated Figure 5

139. Thus, when Sato's tri-state buffer 94 is turned "on" (*i.e.*, in the top module), the TDI input line is ultimately connected to the TDO2 output line as shown below, which enables an output path from TDO2 of the top module down to the external JTAG tester mounted on the main circuit board at the bottom of the stack. For all other modules, the tri-state buffer is turned "off" and the routing path is disconnected from the TDO2 output pin. The combination of Hosomi and Sato therefore discloses "*a control circuit for enabling a routing path ... within an end*

module.”



(2) “Connects the first serial chain route with the second serial chain route” [1E].

140. The combination of Hosomi and Sato discloses a “control circuit” that “connects the first serial chain route with the second serial chain route within an end module” [1E]. As discussed above, each module in the stack includes the claimed “control circuit” (tristate buffer 94 and comparison means 88) for enabling a “routing path” (TDI to TDO2) in response to a “control input signal” (from comparison means 88 to tristate buffer 94). (See §III.B.5(b)(1) (discussing Sato’s Figure 6 which depicts a control circuit disposed to enable a routing path in response to a control signal.))

141. **Petitioner’s “Plurality of Modules” Construction:** As shown below in the figure created to illustrate the combination of Hosomi and Sato, the match condition in the top module during a boundary scan test turns the tri-state buffer

“on” which causes the “*first serial route connection*” in the top module to be coupled to the “*second serial route connection*” in the top module. As a result, the combination of Hosomi and Sato discloses “*a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module*” [1E] under Petitioner’s “*plurality of modules*” construction, which requires a first and second “*serial route connection*” in each module.

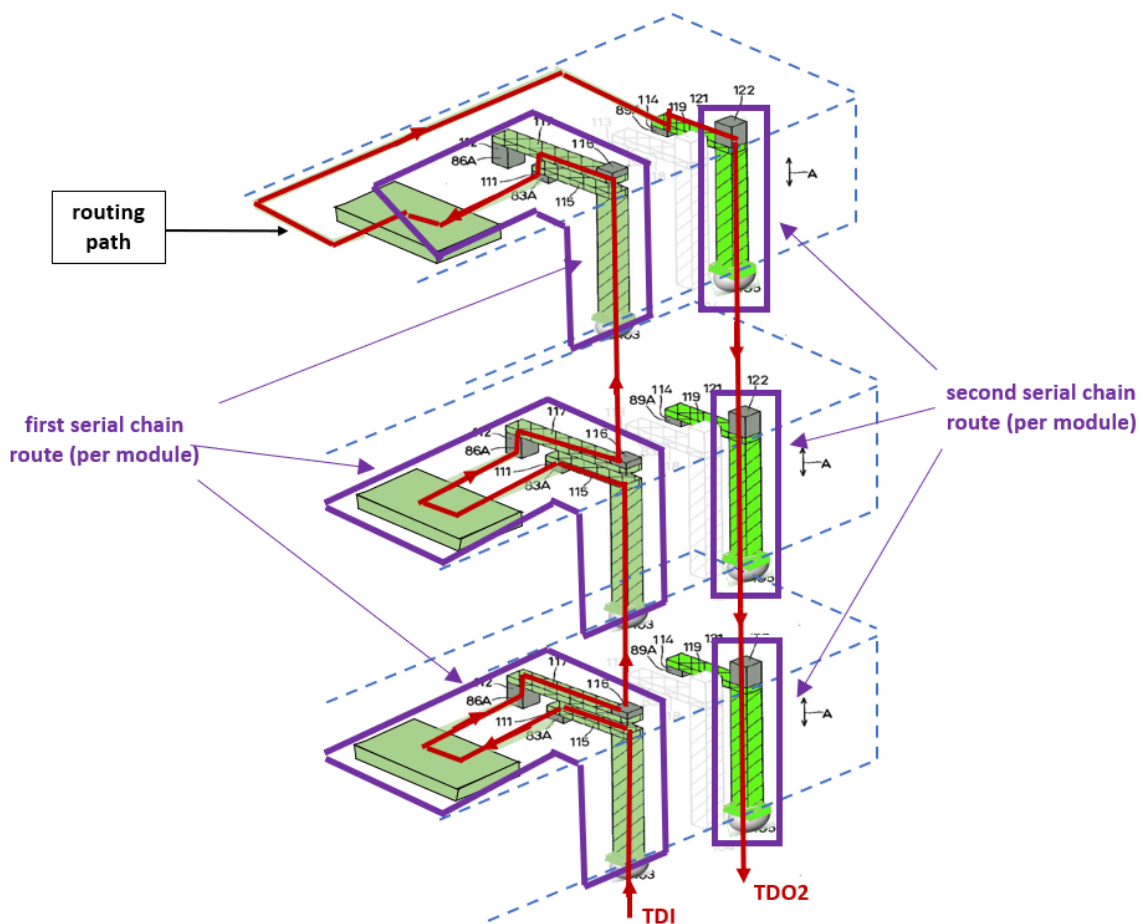


Figure J: Petitioner’s Construction

142. **PO’s “Plurality of Modules” Construction:** Similarly, as shown below, the match condition in the top module turns “on” the tri-state buffer

coupling the “*first serial route connection*” for the stack to the “*second serial route connection*” for the stack by way of the routing path in the top module. As a result, the combination of Hosomi and Sato discloses “*a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module*” [1E] under PO’s construction.

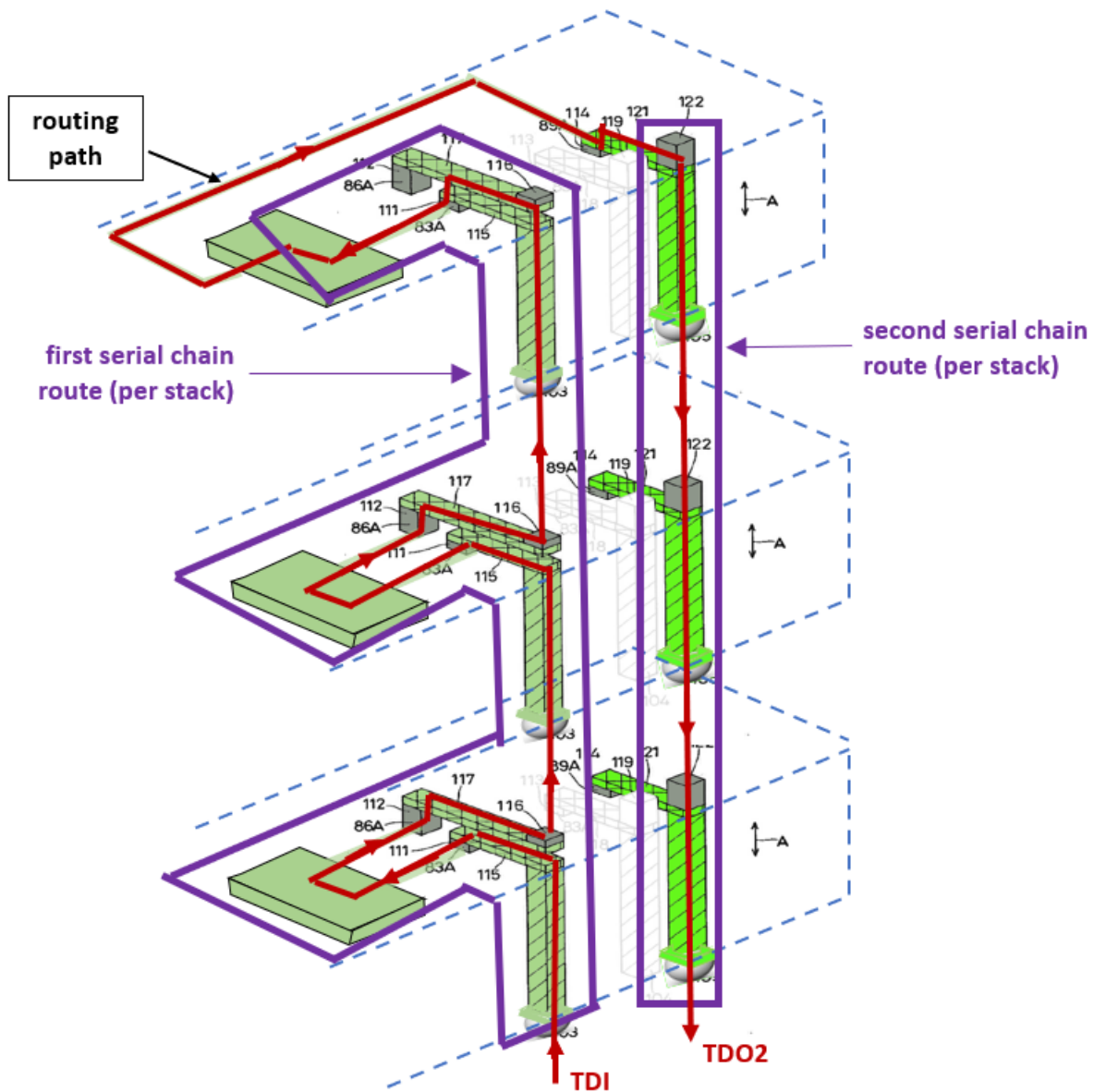


Figure K: PO’s Construction

(3) “Control input signal” [1F].

143. The comparison means, which controls the tristate buffer and is part of the “*control circuit*”, uses identification data input over the TDI signal line. (INTEL-1009, 14:9–10 (“The signal line TDI is a signal line which serially inputs the identification data”).) This identification data is a “*control input signal*” to the “*control circuit*” because it determines whether the comparison means 88 will turn on the tristate buffer 94 to enable the routing path from TDI to TDO2. The identification data provided by the external JTAG tester are routed on the TDI signal line up to the top module through the other modules in the stack, each of which comprise “*another module*” as recited in the claim limitation. As illustrated in Figure L below created by Petitioner to illustrate the combination, the identification data is routed up to the top module through the other modules in the stack by way of the daisy-chain path of TDI signal lines (discussed above), each of which comprise “*another module.*” Thus, the “*control input*” is “*receiving from another module.*” (*Id.*)

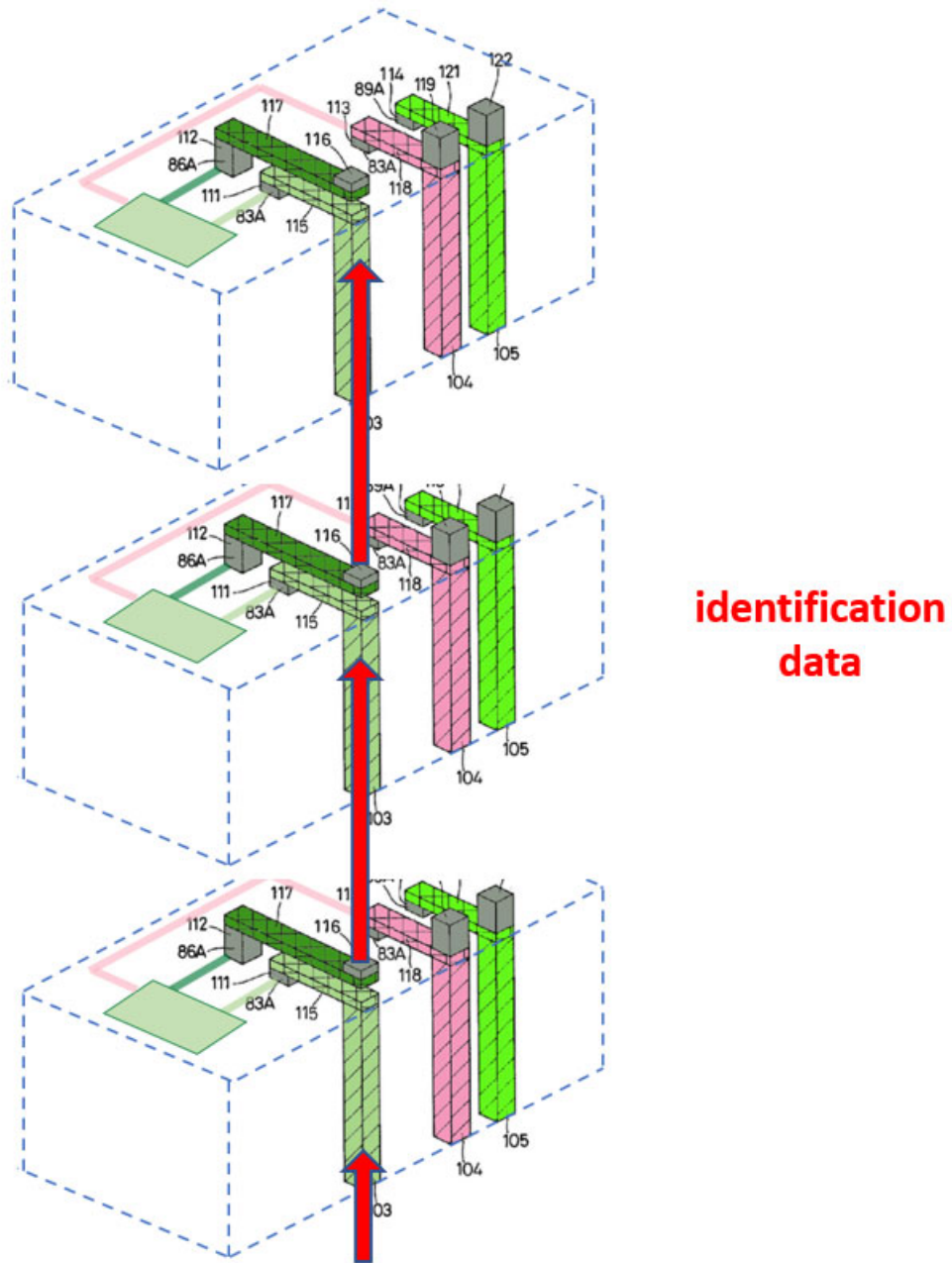


Figure L

144. Accordingly, the combination of Hosomi and Sato discloses “*said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module*” [1F].

C. Claim 2

145. For the reasons I discussed for limitation [1C] in §III.B.3., *supra*, the combination of Hosomi and Sato discloses “*the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module*” [2B]. Further, as shown below, the passive ports in the combination are configured to “*form[] a ladder like routing path*” [2A].

146. The passive ports form a ladder-like routing path because they create a series of “rungs” allowing a signal to pass horizontally in each module and to travel up or down the stack, as shown by Hosomi’s Figure 5 (right) and the Figure (left) created to depict the combination.

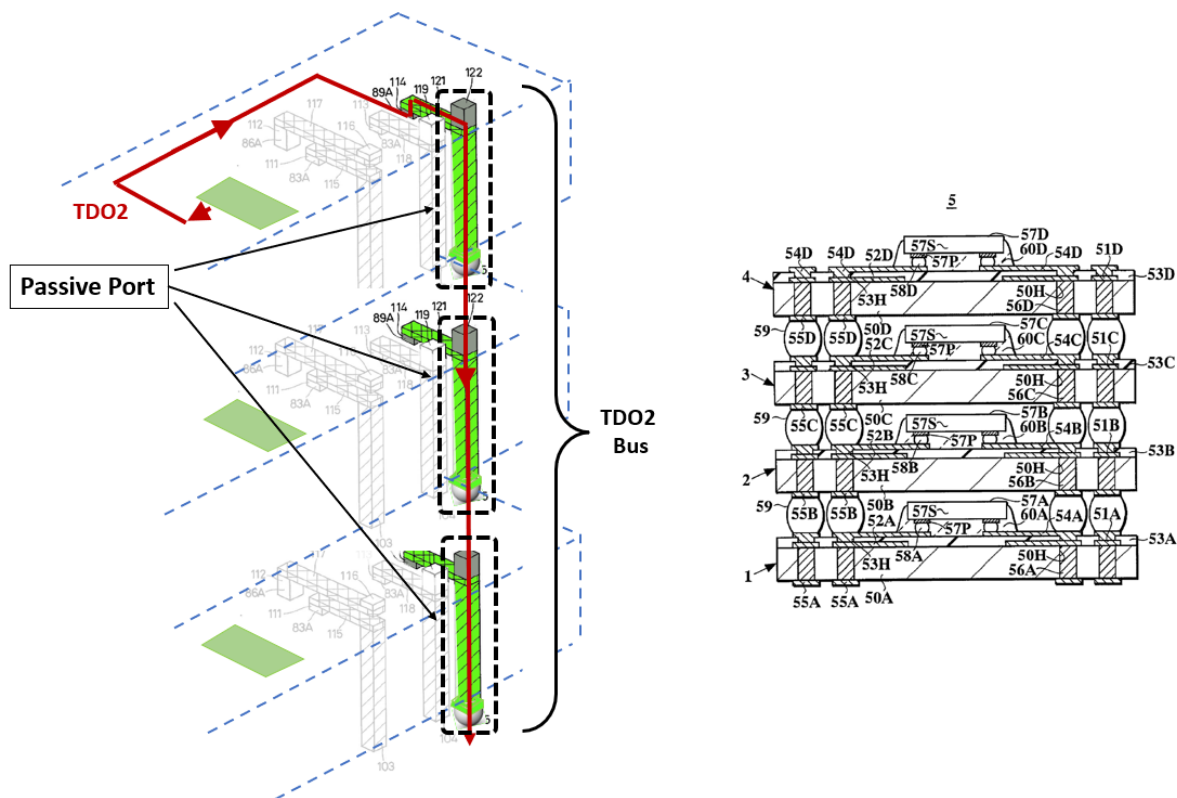


Figure M (left); Hosomi, Figure 5 (right)

D. Claims 11 and 12

147. The combination of Hosomi and Sato discloses that “*one or more of the plurality of modules includes a main board*” [11] and the “*one or more vertically stacked module is connected to the main board*” [12]. Hosomi discloses its memory units “may be mounted on a semiconductor chip together with logical units such as a central processing unit (CPU) and other units.” (INTEL-1007, ¶167.)

148. As discussed in §111.B.1, Hosomi discloses a semiconductor module comprising a plurality of stacked SDRAM modules. Hosomi discloses that the stacked memory module receives signals and transmits signals during memory read and write operations. (*See, e.g.*, INTEL-1007, ¶¶121–127.) Hosomi also discloses a proposal for mounting three-dimensional stacks of DRAM devices on a printed circuit board. (INTEL-1007, ¶7.) Sato also teaches that a stacked semiconductor module “is mounted on the circuit board.” (INTEL-1009, 16:5–7.)

149. As a result, a POSITA would have been motivated to mount Hosomi’s stacked SDRAM memory module having JTAG boundary scan testing functionality on a “*main board*” as taught by Sato. Hosomi further suggests the combination by describing prior art references that each mounted 3-dimensional stacked memory packages on a printed circuit board. (*See* INTEL-1007, ¶¶19–20; Figures 18–19.) Sato also suggests the combination by repeatedly referring to

receipt of external signals from an “external JTAG tester” and transmission of TDO output signals to the tester. (INTEL-1009, 4:21–23.) This teaching would have suggested coupling of the stacked module to a main board to receive signals from and transmit signals to the stacked module. Further, a POSITA would have been further motivated to mount the stacked memory module on a circuit board because it was well-known prior to the ’243 patent that memory modules were designed to be mounted on a main board for use in devices such as computers, smartphones, and other electronic appliances. (See INTEL-1022, 44 (“The MCMs are mounted on printed circuit boards stacked in three dimensions with elastomeric interconnections”).)

150. Further, when the “*stacked module*” is mounted on the main board, the main board is one of the modules of the package. Therefore, the combination of Hosomi and Sato discloses “*one or more of the plurality of modules includes a main board*” [11] and the “*vertically stacked module is connected to the main board*” [12].

IV. GROUND 2: Claims 1, 2, 11 and 12 are Obvious Over the Combination of Sung and Watanabe

A. Combination Overview

1. Sung

151. Like the stacked modules described in the ’243 patent, Sung describes “design methods” that “enable three-dimensional integrated circuit systems in

which all of the dies, in a vertically bonded stack of dies, are identical.” (INTEL-1010, Abstract.) Identical circuits are stacked at each layer “with little or no modification ... [and] while incurring no extra design effort.” (*Id.*) Sung’s method is focused on minimizing the design effort and mask costs associated with each die in a vertical stack. (INTEL-1010, Abstract, ¶¶4, 6, 25, 40-41.) According to Sung, the method can “increase processing power, chip integration and data storage density in the same planar integrated circuit area with small additional design effort ... [which] significantly reduce[s] the performance/productivity gap inherent with shrinking device geometries and increased system-on-chip integration.” (INTEL-1010, ¶42.)

152. To achieve communication between identical stacked components, Sung provides a system of die connectors 100, illustrated in annotated Figure 2 below, comprised of vertical conductors 2 (inter-die vias) situated equally between two terminators 4 (shaded blue). (*See* INTEL-1010, Figure 2, ¶¶43–44.) A POSITA would understand that terminators 4 are “pads”. (*See, e.g.*, INTEL-1012, 433 (“**Pad** – An area of metalization on a substrate used for probing or to connect to a via, plated through-hole, or an external interconnect”) (emphasis in original).) As shown, an electrical connection 102 “exists between each terminal 4.” A conditional electrical connection 104 (as shown by the dotted line on the right-hand-side of Figure 2) may also be used to interconnect one of the terminals 4

(shaded blue) and the pad (shaded green) coupled to the vertical conductor 2. (See INTEL-1010, ¶44, Figure 2.)

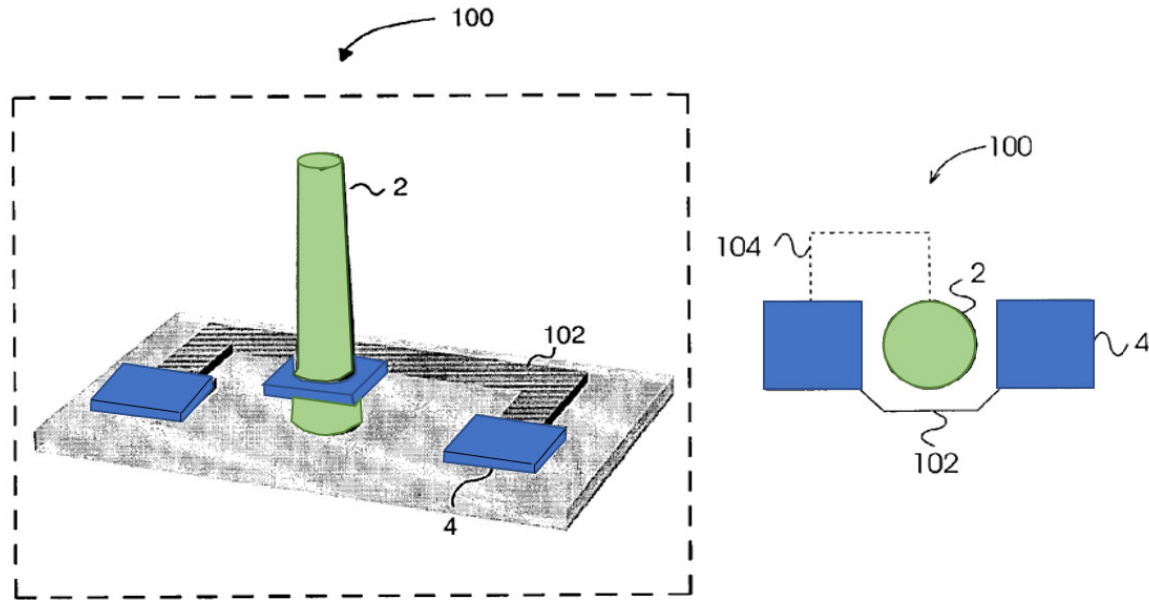


Figure 2: Model of a connector and associated symbol.

Sung, Annotated Figure 2

153. These die connectors 100 are the building blocks Sung uses to form vertical interconnections between adjacent dies in a stack. “Consider three stacked dies 110, 112, 114 with the connectors 100 aligned, as shown in FIG. 3.” (INTEL-1010, ¶44, Figure 3 below.)

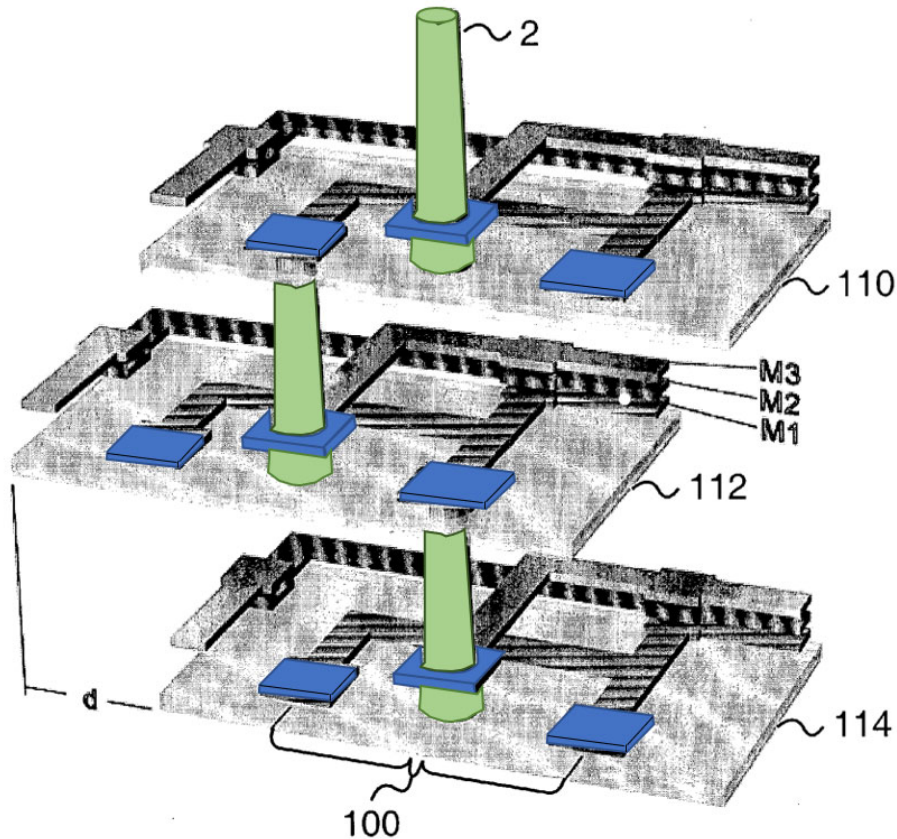


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

Sung, Annotated Figure 3

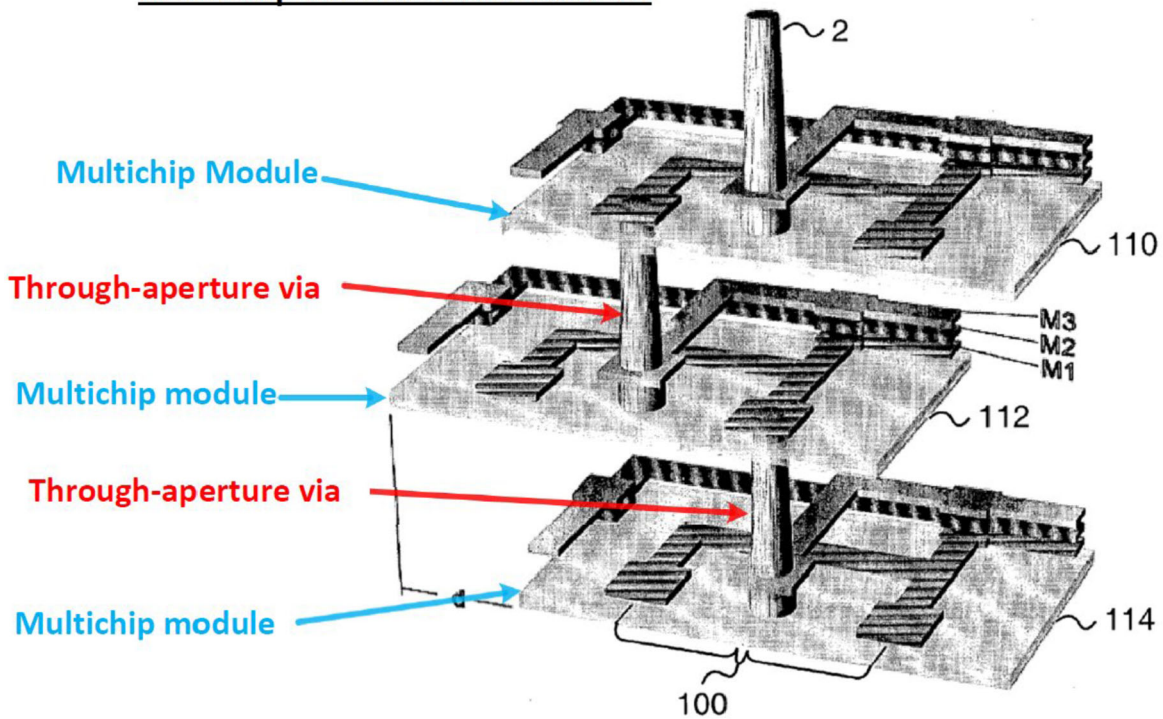
Connectors 100 are designed to permit “staggered alignment of alternating dies” which “facilitates the connection of signals from the current die to the die above, the die below or both dies.” (INTEL-1010, ¶44.) This staggered configuration of die connectors 100 enables using identical integrated circuits at each layer in the stack, while also proving a pathway for electrical signals to be communicated between layers.

154. Further, although Sung discusses stacked integrated circuit dies, Sung’s method “can be adapted to any stackable integrated circuit technology that

allows vertical interconnections between adjacent dies,” including “**stacked multi-chip modules, ... stacked system modules, ... or any other stacked three-dimensional array of electronic circuitry** where like electronic circuitry is used for each level of the stack.” (INTEL-1010, ¶¶43, 52; *see also* INTEL-1010, claims. 6, 13–15 (“6. The apparatus of claim 1 where the layers are comprised of **system modules**. ... 13. The apparatus of claim 1 where the layers are comprised of **multichip module substrates**. ... 15. The thin film structures of claim 14 where signals on adjacent module substrates are **electrically connected through vias formed through apertures that extend through the thickness of the thin film structure and the rigid support base.**”).)

155. In Sung’s multichip module embodiments, the “interdie vias” are replaced with “vias formed through apertures extending through the thickness of both the thin film structure and the rigid supporting base.” (INTEL-1010, claim 15.) These vias are referred to as “through-aperture vias” in the annotated diagram of Sung’s Figure 3 below. The electrical interconnections for a specific connector 100 are determined by the via interconnections of the metal layers on each die. (*See* INTEL-1010, ¶¶43, 47; Figures 1, 3.)

Multichip Module Embodiment



156. Sung further teaches techniques for routing signals among the stacked modules using a communications network for inter-module communications. For example, Sung's network may be used to implement "scan chains 290, inter-processor communication or pipelined computation where information is passed from ... one level of the stack to ... another level of the stack." (INTEL-1010, ¶49.) "In light of the fact that electrical signals can communicate among others: data information, control information, addressing information; it is an object of this invention to provide such a method for communicating externally to, externally from or communicating between, dies in the stack." (INTEL-1010, ¶18.) Indeed, Sung's connectors 100 provide generic building blocks for a variety of interlayer routing circuits in the vertical stack, including a broadcasting circuit 250,

a high current carrying connection 260, and a die identification circuit 270. (See INTEL-1010, ¶¶46–47; Fig. 6.)

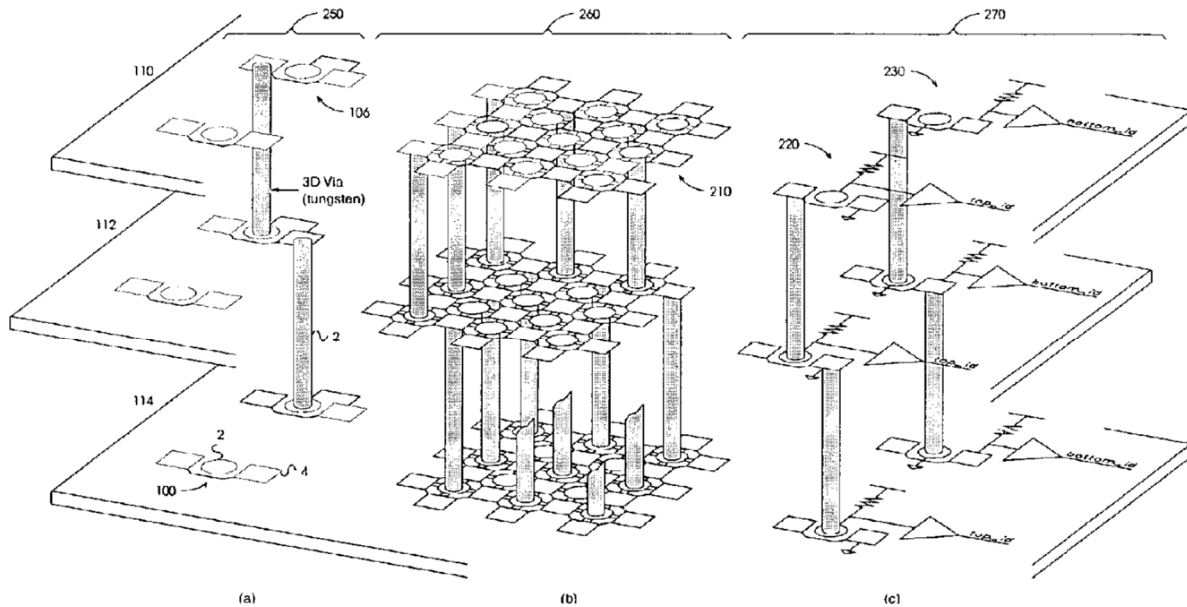


Figure 6: Inter-die communication circuits.

Sung, Figure 6

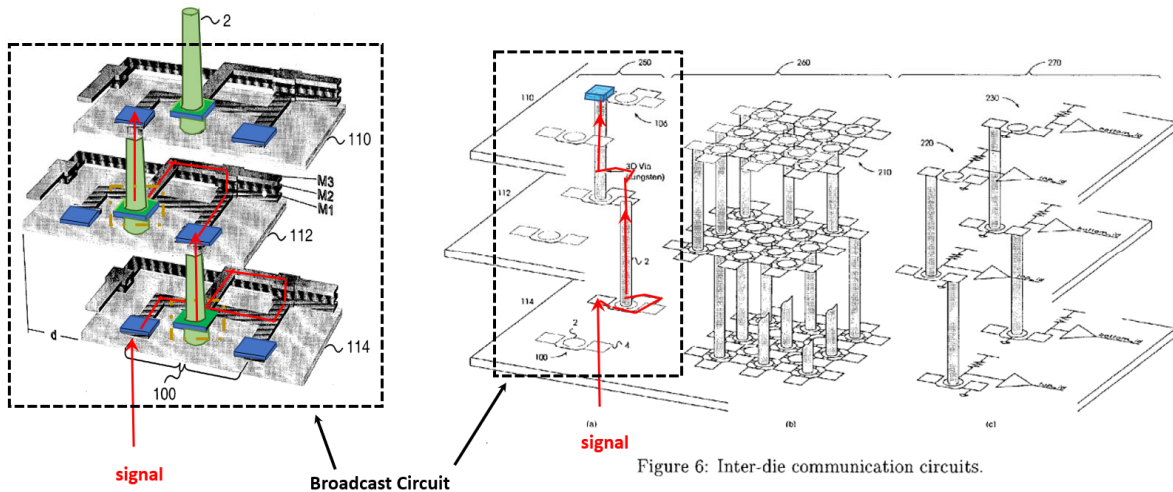
157. The data output by Sung’s inter-die networks may be provided to various system components (*e.g.*, processor, graphics controller, *etc.*) and may be used for functions such as boundary scan testing and validation. The specific circuits for broadcasting, boundary scan, and addressing are described further below.

a) Broadcast Circuit

158. In one example, Sung uses a stack of die connectors 100 to implement a broadcasting circuit 250, illustrated below, which “sends a signal to all dies within the stack.” (INTEL-1010, ¶47.) Examples of these broadcast signals

“include global clocks, addresses, and control signals.” (*Id.*) The broadcast signal travels up the stack when a signal is applied to the bottom stack layer.

Alternatively, the broadcast signal can travel down the stack when the signal is applied to the top stack layer.



Sung, Figure 3 (left), Figure 6 (right)

b) Boundary Scan Chain

159. As discussed in §II.A.6, boundary scan techniques were well-known and standardized before the '243 patent. An exemplary inter-die scan chain network 290 across three dies 110, 112, and 114 is depicted in Figure 10 below. (INTEL-1010, ¶49.) The scan chain path “relies upon the identification of both the top die 110 and bottom die 114 in the stack, to prevent data from flowing past the stack boundaries.” (*Id.*) In the boundary scan chain circuit, an external signal (“in”) is applied to an input pad (not shown in Figure 10) coupled to tri-state buffer 292 which “is controlled by the result (top_id) of the top die identifier circuit 220.”

(Id.)

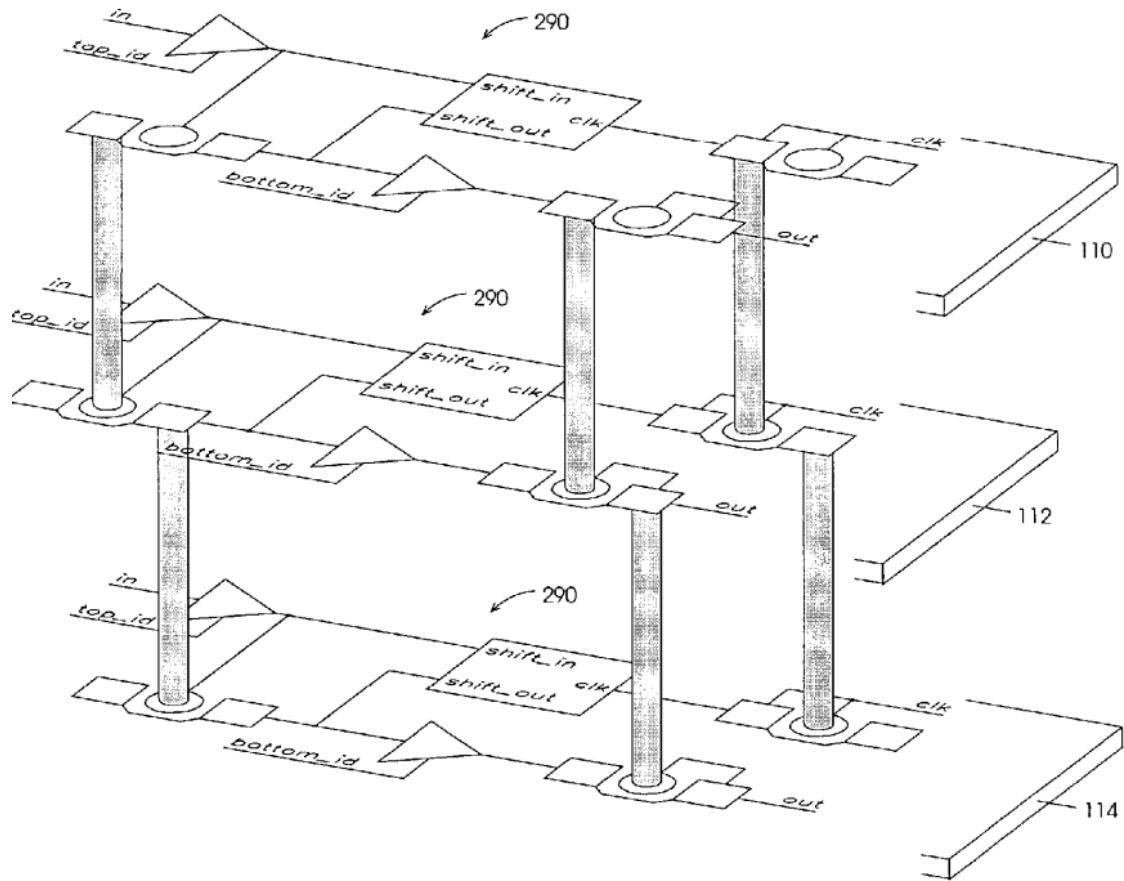


Figure 10: Inter-die communications chain for multiple dies.

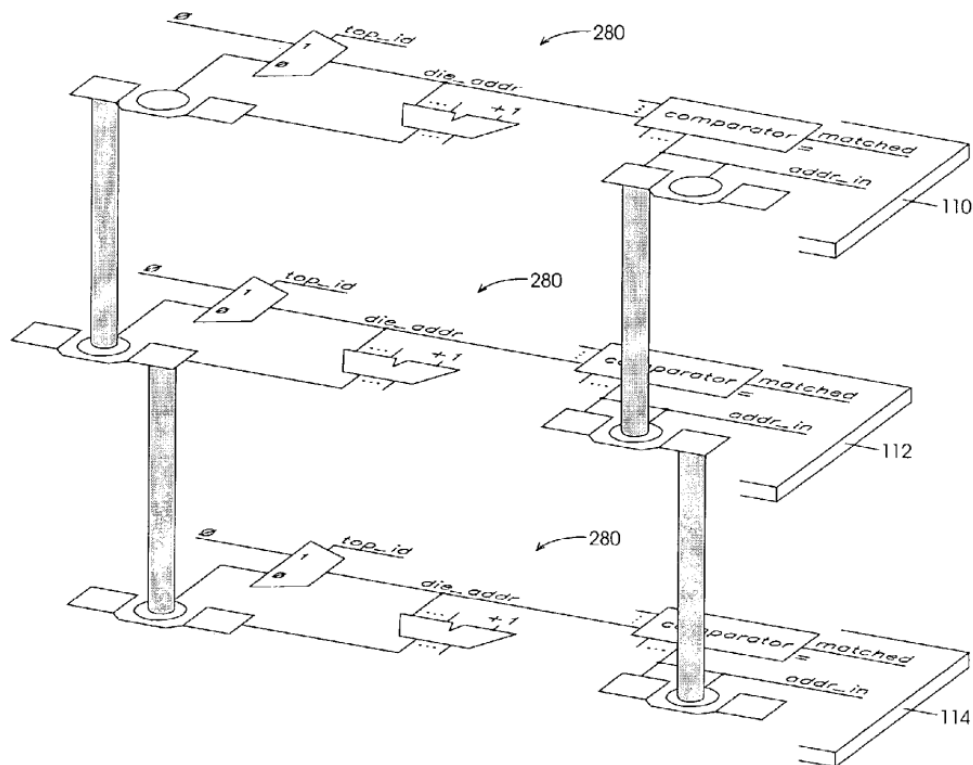
Sung, Figure 10

160. Because the die is at the top of the stack, the “in” signal is coupled by the tri-state buffer to shift_in of register 294. (See INTEL-1010, ¶49.) The shift_out signal “is coupled to the die below 112 through a connector 100.” (Id.) For middle die 112, “shift_in is coupled to the die above 110 through the connector 100 and shift_out is coupled to the die below 114 through the connector 100.” On bottom die 114, “shift_in is coupled to the die above 112 through the connector

100 and shift_out is coupled by a tristate buffer 296 to a broadcasting circuit 250 that conveys the data to the top of the stack 110 and then to a location external to the stack.” (*Id.*) Tristate buffer 296 on the bottom die “is controlled by the bottom_id signal generated by the bottom die identifier circuit 230.” (*Id.*)

c) Addressing Circuit

161. Sung further describes a method for “addressing one die in a vertical stack of like dies.” (INTEL-1010, ¶¶22–23.) Sung provides “a method for assigning each die, in a vertical stack of like dies, a unique address ... [and] addressing one die in a vertical stack of like dies.” (*Id.*) Sung’s addressing scheme enables individual selection of dies within the stack. (INTEL-1010, ¶48.)

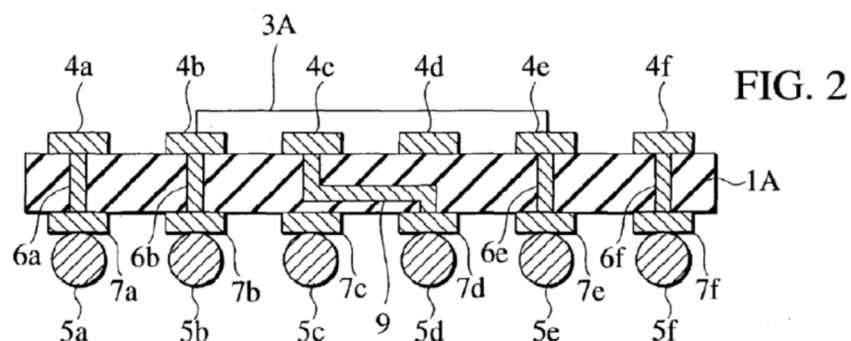


Sung, Figure 9

162. As shown in Figure 9, “the top die sets its address to zero, increments the address by one and passes it down.” (INTEL-1010, ¶48.) The middle die “make[s] the passed-in address its own, then increment[s] it and pass[es] it down.” (*Id.*) A die “respond[s] when the input broadcast address addr_in”, provided to each die by a broadcast circuit (not shown), “matches the die address die_addr.” (*Id.*)

2. Watanabe

163. Watanabe relates “to a semiconductor device packaging technology.” (INTEL-1011, 1:16–17.) Watanabe discloses stacking semiconductor modules referred to as “assemblies”. Watanabe’s stacked assemblies form a multichip module (MCM) comprising multiple thin-type mounting bases such as ball grid array (BGA) packages. (INTEL-1011, 1:16–25, 5:57–58.) Watanabe’s basic building blocks include a set of joint ball connections disposed on one surface of each mounting base that are vertically interconnected by “through-holes” to a corresponding set of “lands” disposed on the opposite surface as shown in Figure 2 below. (INTEL-1011, 3:40–4:26, Fig. 2.)

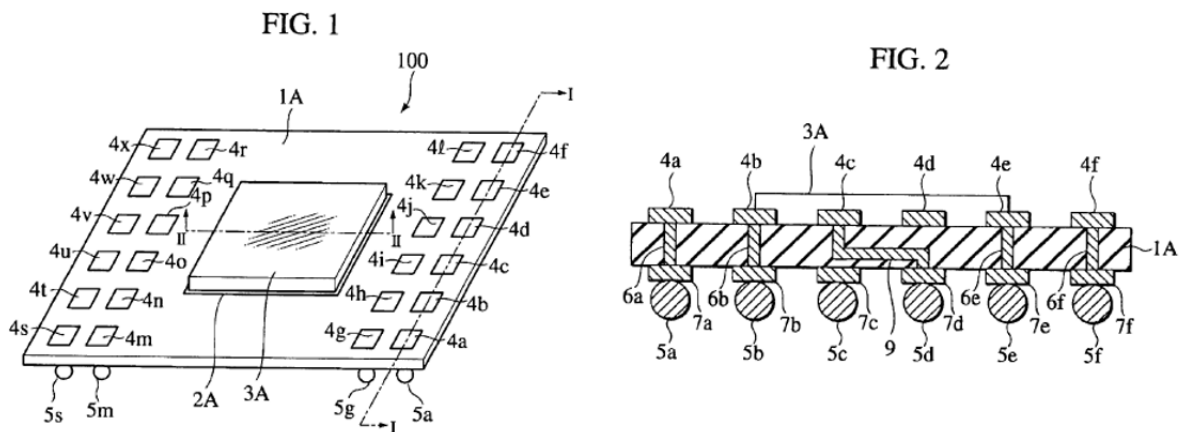


“Lands” are also commonly referred to as “pads”. (See INTEL-1013, 602, 604.)

Further, “solder balls are usable” for Watanabe’s joint balls 5a, 5b, 5c, ... , 5f.

(INTEL-1011, 5:32–33.) The second lands 4a, 4b, 4c, ... , 4f, ... , and the first lands 7a, 7b, 7c, ... , 7f, ... can be provided respectively on each of the first surface and the second surface with number of about 40 to 60 balls. (INTEL-1011, 5:33–37.)

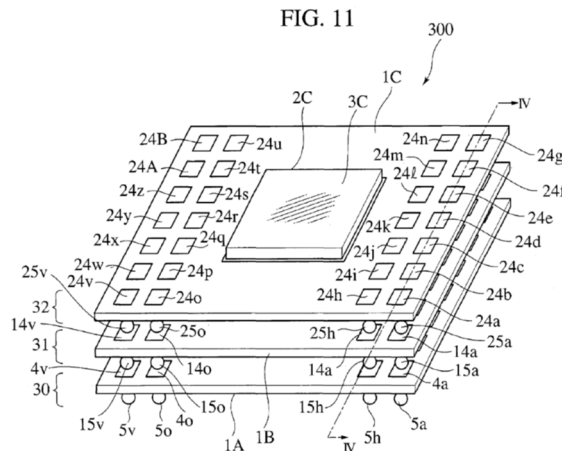
164. Watanabe explains that the “assembly of levels of electronic devices is classified into several packaging levels in a hierarchy.” (INTEL-1011, 3:27–28.) A “first level assembly” indicates an assembly “in which a semiconductor chip is mounted on a mounting base.” (INTEL-1011, 3:28–30.) Figure 1, below left, is an example of a one-layer first level assembly; and Figure 2, below right, is a side view from the I-I line of Figure 1. (See INTEL-1011, 2:35–40.)



165. As shown, the bottom first surface of mounting base 1A (referred to herein as “substrate 1A”) includes lands 7a-x on which balls are formed. (INTEL-1011, 3:43–44; 3:52–54.) A “mounting base” is commonly referred to as a

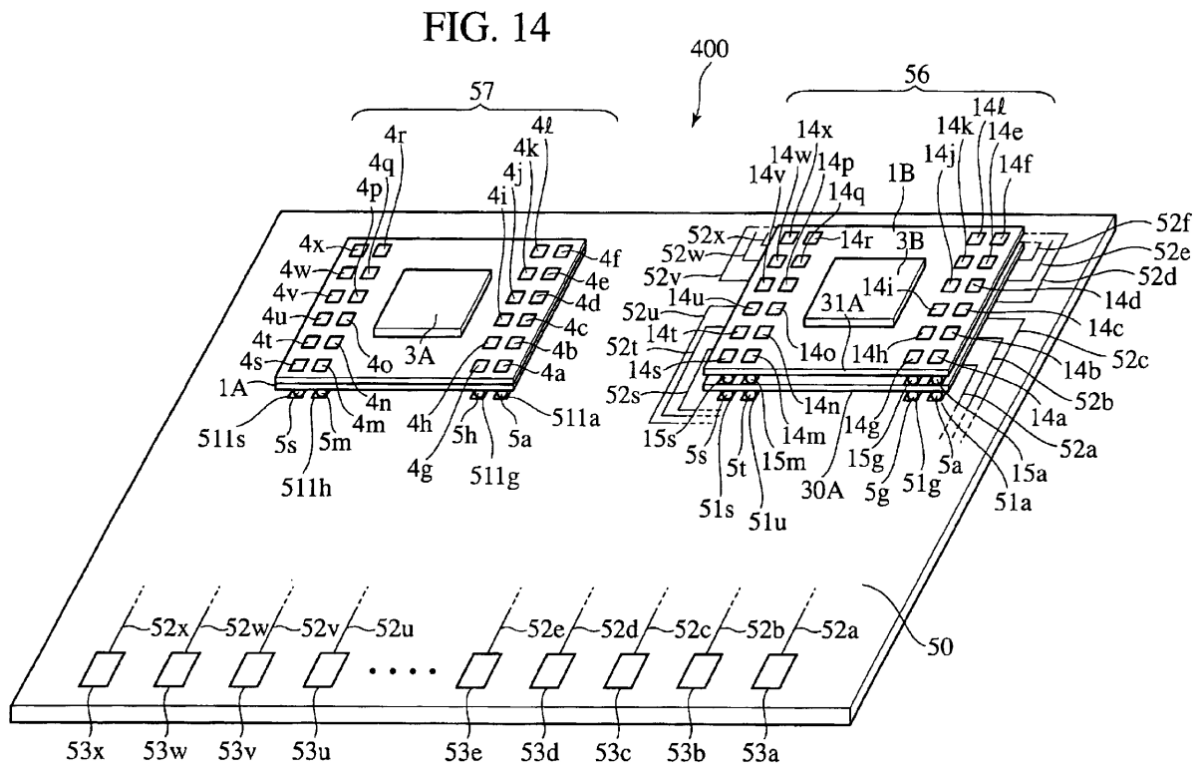
substrate. Second lands are disposed on the upper surface of substrate opposite the first lands and through-holes 6a-x are embedded in the substrate to connect first lands 7a-x to second lands 4a-x. (INTEL-1011, 3:45–50.) Through-holes filled with conductive material shown in Figure 2 are commonly known as “vias.” (See INTEL-1011, 4:23–26; *see also* INTEL-1012, 444 (“Via – A hole filled or lined with a conducting material, which is used to link two or more conducting layers in a substrate.”).) Thus, Watanabe’s pad-via-ball interconnections are configured to transfer signals from one surface of a module to the other.

166. Watanabe further discloses stacking memory structures such as “a DRAM, a flash memory, a SRAM, a mixed memory logic and the like” so that “the volume of the assembly can be made smaller.” (INTEL-1011, 8:7–8, 10:19–20.) For example, Watanabe teaches a “three-level stacked structure” shown in Figures 11 and 12 below.



In the embodiment shown in Figures 11 and 12, the first level assembly has multiple layers. Balls on the lower surface of the middle layer are coupled to pads on the upper surface of the bottom layer. Similarly, balls on the lower surface of the upper layer are coupled to pads on the upper surface of the middle layer. These connections allow a signal to be communicated between layers.

167. In a second level assembly, “the first level assembly is mounted on a board.” (INTEL-1011, 3:34–36.) Figure 14, reproduced below, illustrates a second level assembly having both single-layer and multi-layer first level assemblies 56, 57. (See INTEL-1011, 10:54–60.)



Watanabe, Figure 14

168. Terminals 53a-x on the board are configured for receiving external signals (e.g., addresses, input/output signals, voltage VDD, and ground) and are connected to the first assembly by signal wiring 52a-x, as shown. (See INTEL-1011, 11:9–57.) For example, Watanabe describes mounting the stacked structures on a main circuit board for supplying external signals such as input and output signals, address and power signals and the like:

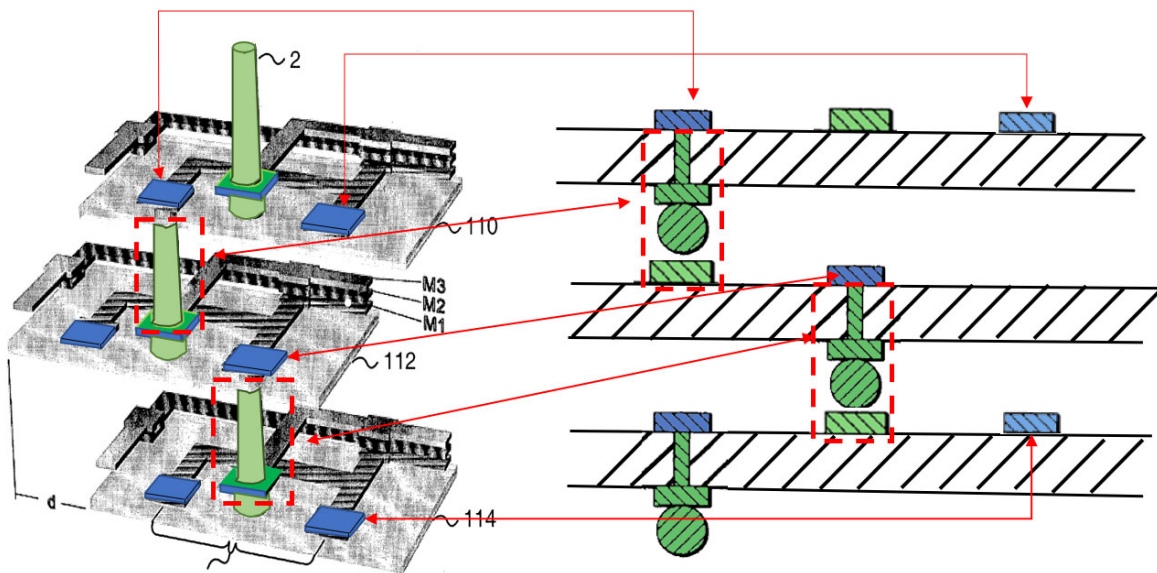
In the first connection terminals 51a, 51b, 51c, ..., 51x, ...disposed in the first substrate mounting area 51A ... included are: an ADD terminal 51a for supplying the address signal; an input and output terminal 51b for supplying the input and output signal; chip selection terminals 51c and 51d for selecting the semiconductor chips; a GND terminal 51e; and a VDD terminal 51f and the like.

(INTEL-1011, 11:25–31.) “[C]hip selection terminals” are also provided so that each stacked module may be operated independently. (See INTEL-1011, 7:54–57, 8:8–16, 10:16–27.)

3. Combination of Sung and Watanabe

169. A POSITA would have been motivated to use Watanabe’s pad-via-ball structure to implement connections between modules in Sung’s stacked module embodiments, as illustrated below for an exemplary broadcasting circuit (Sung’s Figure 3 left). Specifically, a POSITA would have been motivated to use Watanabe’s vias to provide bi-directional connection through a module substrate, like bi-directional vertical conductors of connector 100 provide connection through a die in Sung. (INTEL-1010, ¶44.) The use of vias is consistent with Sung which

claims its multichip module substrates include “vias formed through apertures that extend through the thickness of the thin film structures and the rigid support base.” (INTEL-1010, claim 15.) A POSITA would have further used a pad/ball on the bottom surface of each of Sung’s modules, connected to the via, for coupling with a pad on the upper surface, as taught by Watanabe. (See, e.g., INTEL-1012, 154 (explaining pad/ball connections are used on packages and chips and design for each implementation were understood).) An example of such a configuration is shown below.



Sung, Annotated Figure 3; Figure N

170. A POSITA would have been motivated to make the above combination for numerous reasons as set forth below. First, Sung describes embodiments in which its “design method” is used with “stacked multi-chip

modules”, “stacked system modules,” and “multichip module substrates.” (INTEL-1010, ¶52.) However, Sung lacks the particular implementation details for connecting such modules. A POSITA would have therefore been motivated to search for references describing the available types of interconnection techniques that are used for stacked modules and would have been led to Watanabe. Watanabe is in the same field of endeavor as Sung and the ’243 patent—*i.e.*, 3-dimensional packaging—and describes a stacking technique used to form multichip modules. (See INTEL-1010, ¶52; INTEL-1011, 5:57–58 (“mounting bases 1A such as BGA tape can be stacked into a multi chip module (MCM).”); *see also* INTEL-1001, 1:7–57.) Watanabe further teaches that its stacked modules are mounted onto a main board as shown in Figures 13 and 14 above. (See INTEL-1011, 3:32–38, 10:29–51.)

171. Both Sung and Watanabe are further reasonably pertinent to a problem addressed by the ’243 patent—maximizing “capacity in a limited area.” (INTEL-1001, 1:21–24.) Sung’s stacking technique is designed to “increase processing power, chip integration, operating speed and data storage density in the same planar area while minimizing global interconnect lengths,” while Watanabe’s stacking technique is aimed at realizing “high density packaging in thin-type semiconductor packages such as a BGA package.” (INTEL-1010, ¶6; INTEL-1011, 1:52–54.) These purposes are consistent with those of the ’243 patent, which

include “using [a] multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.”

172. Second, Sung provides express motivations that would have led a POSITA to use Watanabe’s pad-via-ball structure as the inter-module connection structure for Sung’s multichip module embodiments. Sung notes that “the design techniques presented in this invention can be adapted to any stackable integrated circuit technology that allows vertical interconnections between adjacent dies.” (See, INTEL-1010, ¶43.)

173. Sung further discloses use of different types of connections between components, and specifically teaches the use of “solder pads”, “solder bumps” and “solder mounds”:

New developments in manufacturing process technology allow wafers to be vertically stacked and fine-grained vertical conductors formed between circuits on adjacent dies [1, 2, 3, 4, 5, 6, 7]; U.S. Pat. No. 5,627,106; U.S. Pat. No. 5,877,034; U.S. Pat. No. 5,998,808; U.S. Pat. No. 6,185,122; U.S. Pat. No. 6,034,882. Alternatively, layers of transistor circuits may be interconnected with coarser grain conductors such as coaxial lines, (C-4) **solder pads, solder mounds, solder bumps**, wire bonds, wire interconnects or embedded wiring as in U.S. patent application Ser. No. 20010033030; U.S. patent application No. 20010033509; U.S. patent application Ser. No. 20010005059; U.S. Pat. No. 5,495,397; U.S. Pat. No. 5,544,017; U.S. Pat. No. 5,778,529.

(INTEL-1010, ¶3.) As discussed previously, a POSITA would have understood that the terms “solder balls”, “solder bumps” and “solder mounds” were used synonymously to refer to the same type of interconnection element. (See

II.A.3.(b).)

174. Sung teaches in its claims that its inter-die vertical conductors include “interconnection members such as solder mounds” and that the terminators may be “bonding pads” or “3D via pads.” (INTEL-1010, claims 36, 39, ¶29.) Bonding pads were well known interconnection elements often used with solder balls/bumps for forming vertical interconnections in integrated circuits:

[F]ace-bonded chips must have prepared bond pads suitable for direct placement and soldering to the substrate lands. The technique for pad preparation is known as *bumping*, since the end result is that each die bond pad has a solderable *bump* on it. Pad bumping is typically done with solder at each bond pad while the die are still in wafer form requiring special processing by the die manufacturer. ... For bumped die, the flip chip process begins with bumping the contact pads of the die. As noted previously bumping can be done several ways, but in most typical process results in tin-lead solder “bumps” being attached to each contact pad as shown in Fig. 4.4. ... This direct bonding to the substrate means the flip chip has real estate reductions compared to standard hybrid wire bonded die in much the same way that a ball grid array (BGA) has real estate reductions compared to a plastic leaded chip carrier (PLCC) or a quad flat pack (QFP). The real estate reduction is what gives flip chips their advantage in high-density circuits.

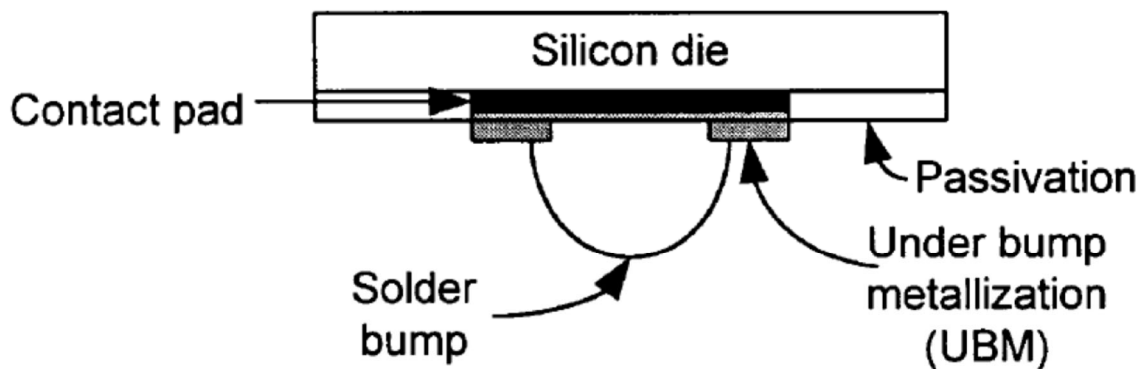


FIGURE 4.4 Typical solder bump.

(INTEL-1013, 107–108.) Based on these teachings, a POSITA would have been motivated to use solder balls (mounds) coupled to bonding pads to electrically connect signal paths in two adjacent modules, such as the ones taught by Watanabe.

175. Third, a POSITA would have been motivated to combine the teachings of Watanabe and Sung because the use of pad-ball interconnections and their advantages were well known long before the '243 patent. Pad-to-ball interconnections were pioneered by IBM in the 1960s and are still to this day “[t]he most popular attachment method” for making vertical interconnections. (INTEL-1014, 31.) For example, this interconnection technique has been used in “flip chip” packaging for decades. (INTEL-1013, 423 (definition of “Flipped-Chip”.) In flip chip bonding, pads are metalized on the surface of chip and a solder ball is deposited on each pad. The chip is then flipped and aligned with pads on the circuit board. Then the solder balls are essentially “remelted” to make the connection between the ball and the corresponding pad on the circuit board or substrate. (*See* §II.A.3.(b).)

176. A similar technique is used in 3-dimensional packaging to interconnect two modules as taught by Watanabe. It was well-known that flip chip connections had a number of other advantages over other connection methods, including (i) reduced integrated circuit area and wiring length, resulting in high-

density circuits with decreased parasitic capacitance and inductance, (ii) performance gains, especially at higher frequency operation, and (iii) simplified manufacturing process.

Flip chips are bare IC die placed on the board with bond pads down. Because of the reduction in ‘package’ size (there is none), and subsequent **reduction in electrical path length and associated parasitic capacitance and inductance, it is particularly suited for high-density, high performance applications.** ... The table below shows examples of the parasitics that exist in a variety of packages. **Flip chip advantages are obvious.”**

TABLE 4.1 Parasitics in Various Electronic Packages

Package type	Parasitic capacitance, pF	Parasitic Inductance, nH
Flip chip	0.1	0.01
Chip on board/wire bond	0.5	1–2
Pin grid array	1	2
Quad flat pack	1	1–6
Through-hole DIP	3	8–20

(INTEL-1013, 106–107.) “The most popular attachment method is to simply make the DCA⁶ bumps out of solder and reflow them to the substrate pads.” (INTEL-1014, 31.) Additionally, it was well known that pad-to-ball interconnections were

⁶ DCA and flip chip are nearly synonymous. DCA refers to “direct chip attach,” which is the general term for attaching an IC to a substrate or printed circuit board using solder balls/bumps. Direct chip attach is the general category focused on the attachment of balls to pads and may include chips that are flipped (flip chip) and those that are not flipped such as ball grid array (BGA).

easier to align than other types of connections (e.g., ball-to-ball), leading to lower manufacturing costs. These advantages of pad-ball interconnection would have been well-known to a POSITA.

177. Finally, the combination of Watanabe's pad-via-ball interconnection teachings with Sung is nothing more than the combination of familiar prior art elements according to known methods to yield predictable results. A POSITA would have understood how to combine the elements taught by Watanabe and Sung using known methods. As discussed above, use of solder balls and corresponding bonding pads to form flip-chip electrical interconnections was well-known and described in textbooks well before the '243 patent. (INTEL-1013, 106–108; INTEL-1014, 31; INTEL-1012, 153–154, 271–272, 423 and 440–441.)

Solder Bump Bonding – A flip-chip technique (also known as *Solder Bumping*) for attaching a die to a package substrate. A minute ball of solder is attached to each pad on the die, and the die is flipped over and attached to the package substrate. Each pad on the die has a corresponding pad on the package substrate and the package-die combo is heated so as to melt the solder balls and form good electrical connections between the die and the substrate.

(INTEL-1012, 440 (emphasis in original)).

178. Additionally, Sung and Watanabe both perform the same functions in the combination as they do separately. For example, Watanabe's pad-via-ball interconnections provide an electrical path through a module substrate and provides this same function in the combination. Sung provides techniques for

routing signals between modules in a stacked configuration. Sung's routing techniques operate the same using Watanabe's pad-via-ball signal path through a module in Sung's stacked module embodiment as they do in the stacked die embodiment.

179. A POSITA would therefore have recognized that the results of the combination were predictable and would have had a reasonable expectation of success in the combination. In fact, the stacking technology described in the '243 patent was nothing new at the time of the purported invention. Indeed, the '243 patent admits its module and package level stacking technology existed in the prior art: "[t]he present invention takes advantage of the **existing stacking technology both on the module and package level.**" (INTEL-1001, 1:59–60.) Sung similarly teaches that three-dimensional stacking of dies, including 3D memory stacks, existed. (See INTEL-1010, ¶¶4–14.) Thus, a POSITA would have understood how to implement these existing techniques to integrate pad-via-ball signal paths through modules and pad-to-ball connections between modules in Sung's stacked module embodiments.

180. Both Sung and Watanabe are focused on solving the same problems in the same manner—including (i) they are both focused on integrated circuit stacking techniques to increase circuit density per unit area, and (ii) they both provide a selection mechanism for uniquely accessing individual layers in the

stack. (See INTEL-1010, ¶¶5–6, 15, 22–23, 25, 40–42, 48; INTEL-1011, 1:23–26, 5:67–6:3, 6:17–22, 6:36–39, 8:8–16, 10:20–27.) These features are consistent with the description in the '243 patent which teaches “[s]tacking both on chip module and package level [to] maximize[] the capacity in a limited area thus realizing the move to miniaturize the entire storage device,” and a “connection technique that enables a selection of [a] specific module in a multiple module stack ... [and] that enables the controller module’s active pad to be routed to the desired specific module in the stack.” (INTEL-1001, 1:21–24, 8:61–9:12 (as modified by COC).) A POSITA would have recognized Watanabe’s interconnections to be advantageous in the multichip module implementations such as Sung’s because Watanabe furthers Sung’s objective of accessing each semiconductor die “independently.” (INTEL-1010, ¶¶22–23; INTEL-1011, 8:8–16, 10:20–27.)

181. Sung’s implementation uses identical integrated circuits at each layer of the stack and each of Watanabe’s modules are individually selectable, such that there would have been no need to modify Sung’s routing scheme to accommodate Watanabe’s technique.

182. Finally, it should also be noted that Watanabe’s structure is consistent with Sung’s. Sung teaches that its multichip module substrates include “vias formed through apertures that extend through the thickness of the thin film structures and the rigid support base.” (INTEL-1010, claim 15; *see also* claims 13–

14.) Watanabe similarly describes use of stacked integrated circuit structures that are vertically interconnected by way of through-hole vias between adjacent stacked layers. (See INTEL-1011, 3:40–62.)

B. Independent Claim 1

[1P] A stacked module comprising

[1A] a plurality of modules each comprising:

[1B] one or more active ports for carrying one or more active signal;

[1C] one or more passive ports for passing through the one or more active signals;

[1D] a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

[1E] a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

[1F] said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

1. Preamble [1P] and “Plurality of Modules” [1A].

183. The combination of Sung and Watanabe discloses a “*stacked module*” [1P] that comprises “*a plurality of modules*” [1A]. Sung discloses an “[s]calable electronic circuit system composed of **stacked layers of the same or similar circuitry.**” (INTEL-1010, ¶2.) “An object of this invention is to provide a method to reuse the same or similar integrated circuit design for each die in a vertically

bonded stack of dies, and have the entire stack of dies function as an interconnected system.” (INTEL-1010, ¶15.)

The methods described enable scalable integrated circuit systems in which circuits on different die, in a vertical three-dimensional stack of dies, are identical. Only one mask set is required for the entire stack. The system scales directly as the level of stacking is increased while incurring no extra design effort as the stack height increases.

(INTEL-1010, ¶25.) As discussed in §IV.A.6., *supra*, Sung teaches that its “stacked dies” are coupled together using “vertical connectors”.

184. Although Sung describes its techniques in the context of stacked dies or stacked integrated circuits, Sung’s “method of aligning and connecting together like wafers can be applied to: **stacked multi-chip modules ... stacked system modules**, stacked circuit subassemblies or any other stacked three-dimensional array of electronic circuitry.” (INTEL-1010, ¶52, *see also*, claim 6 (“layers are comprised of system modules”), claim 13 (“layers are comprised of multichip module substrates”).) Further, each module in Sung’s “*stacked module*” embodiments includes the same or substantially the same circuitry. One “object” of Sung is to provide a method “to reuse the **same or similar integrated circuit design for each die** in a vertically bonded stack of dies.” (INTEL-1010, ¶15; *see also*, ¶25 (“The methods described enable scalable integrated circuit systems in which **circuits on different die**, in a vertical three-dimensional stack of dies, **are identical**”); ¶52 (explaining technique applies to stacked modules “where like

electronic circuitry is used for each level in the stack”).)

185. Watanabe describes a stacked multichip module architecture where adjacent stacked layers are interconnected using flip chip connections. (*See* §II.A.3.(b).) Watanabe discloses a first level assembly 100 (corresponding to a “module”) that uses balls and pads to interconnect with other modules and components. Watanabe uses the term “lands.” “Lands” and “pads” are used synonymously in the art and may be defined as a “portion of a conductive pattern, usually, but not exclusively, used for the connection and/or attachment of components.” (INTEL-1013, 602, 604.) Lands may include, for example, bonding pads that are patterned on a printed circuit board. “Balls” are typically formed on the lands/pads as was well known in the art. (*See* §II.A.3.(b).) “Pad bumping is typically done with solder at each bond pad while the die are still in wafer form ... After individual dice are sliced from the wafer, the chip will be placed on the **board lands** and reflowed in a conventional reflow oven.” (INTEL-1013, 107.)

186. The stack of modules in the combined system of Sung and Watanabe is a “*stacked module*” [1P] which comprises “*a plurality of modules*” [1A]. Thus, the combination of Sung and Watanabe teaches a “*stacked module comprising a plurality of modules*” as claimed.

187. Further, the combination of Sung and Watanabe teaches or suggests

each module in the “*stacked module*” is an SDRAM module. Petitioner’s construction of “passive port” requires the modules to be SDRAM modules. (See §II.E.2.) Sung does not limit the applicability of the modules in its stack to a particular type of module. Instead, Sung suggests broad applicability to any stacked three-dimensional array of electronic circuitry.

Although the present invention pertains to stacked integrated circuits, the method of aligning and connecting together like wafers can be applied to: stacked multi-chip modules, stacked printed circuit boards, three-dimensional systems packaging, stacked system modules, stacked circuit subassemblies **or any other stacked three-dimensional array of electronic circuitry** where like electronic circuitry is used for each level of the stack.

(INTEL-1010, ¶52.)

188. Further, Sung teaches that its stacking technique increases “data storage density” and describes prior art “three-dimensional memories” which “stack separate layers of memory cells.” (INTEL-1010, ¶¶5–6, 42). But Sung does not explicitly teach that its memory modules comprise SDRAM modules.

189. Nonetheless, Watanabe suggests use of SDRAM memory modules. “The increase in density and the progress in large-scale integration have continued in semiconductor integrated circuits. **Especially in DRAM**, thin and small package such as ball grid array (BGA) package has been widely used.” (INTEL-1011, 1:23–26.) Watanabe’s stacked assemblies include stacked DRAM modules.

In addition, assuming that each of the first level assembly 30 and the upper level assembly 31 are semiconductor recording devices, the

(INTEL-1011, 7:67–8:8.) “FIG. 9 is a perspective view showing an example of a first level assembly having a two-level constitution according to a second embodiment of the present invention.” (INTEL-1011, 2:59–61, Fig. 9.)

- 128 -

Conventional DRAMs had an asynchronous interface to the memory controller, and hence every transfer involved overhead to synchronize with the controller. **The second major change was to add a clock signal to the DRAM interface**, so that the repeated transfers would not bear that overhead. **Synchronous DRAM (SDRAM) is the name of this optimization.**

(INTEL-1024, 313–314.)

SDRAM (Synchronous DRAM) – Until the latter half of the 1990s, DRAM-based computer memories were asynchronous, which means they weren't synchronized to a system clock. Over time, the industry migrated to synchronous DRAM (SDRAM), which is synchronized to the system clock and makes everyone's lives much easier. **Note that SDRAM is based on core DRAM concepts** – it's all in the way you tweak the chips and connect them together.

(INTEL-1012, 438.)

191. Thus, a POSITA would have been motivated to use SDRAM, which is synchronized to the system clock, as the DRAM in the stacked memory of the combination of Sung and Watanabe because SDRAM was easier to use than asynchronous DRAM and also because SDRAM was already widely deployed in devices such as desktop and laptop computers at the time. (See INTEL-1024, 338 (Figure 5.25) (reproduced below).)

192. A POSITA would have been motivated to stack SDRAM modules (as suggested by Watanabe) in Sung's architecture. Specifically, a POSITA would have been motivated to stack SDRAM modules to achieve higher memory capacity at lower cost. SDRAM provides the lowest cost per bit for readable/writeable memories because SDRAM only requires one transistor to store a bit in each

memory cell. (INTEL-1024, 312 (“To pack more bits per chip, DRAMs use only a single transistor to store a bit.”).)

ECC?	Modules		Dell XPS PCs					
	No ECC	ECC	No ECC			ECC		
Label	DIMM	RIMM	A	B	B – A	C	D	D – C
Memory or system?	DRAM		System		DRAM	System		DRAM
Memory size (MB)	256	256	128	512	384	128	512	384
SDRAM PC100	\$175	\$259	\$1519	\$2139	\$620	\$1559	\$2269	\$710
DDRDRAM PC700	\$725	\$826	\$1689	\$3009	\$1320	\$1789	\$3409	\$1620
Price ratio DRDRAM/SDRAM	4.1	3.2	1.1	1.4	2.1	1.1	1.5	2.3

Figure 5.25 Comparison of price of SDRAM versus DRDRAM in memory modules and in systems in 2000.

193. Finally, use of SDRAM modules in the “*stacked module*” of the combination of Sung and Watanabe amounts to no more than combining prior art elements (Watanabe’s DRAM/SDRAM with Sung’s modules) according to known methods to yield predictable results. Therefore, implementing a stacked memory module according to Sung’s architecture using SDRAM memory modules at each layer in the stack as suggested by Watanabe would have only required the application of ordinary skill.

2. “*One or More Active Ports*” [1B].

194. The combination of Sung and Watanabe discloses “*one or more active ports for carrying one or more active signal*” [1B]. The ’243 patent refers to an “active pad” as an “*active port*”:

The controller had four active pads such as 1904, one each for the four SDRAM modules such as 1901. **An active pad may be also referred to herein as an “active port.”** The controller module’s active pad 00

1904 is ultimately connected to X0 ball 1903 of SDRAM module 0, active pad 01 is connected to X0 ball 1902 of SDRAM module 1, and so on.

(INTEL-1001, 9:1–8 (COC additions indicated in underline); INTEL-1005, 2.) As I discussed in Ground 1, an “*active signal*” encompasses a signal applied to the stack by an external source that is distributed via an “*active port*” to circuitry on a module. Sung discloses numerous “*active signals*” carrying information, including the “in” signal of the boundary scan chain of Figure 10 (reproduced below with annotations). As shown, the external signal “in” is received as an input to a tri-state buffer on the top module of the stack. (See INTEL-1010, ¶49.) A POSITA would have understood the “in” signal is received at an active pad (shaded blue) on the upper surface of the top module (added by Petitioner to Figure 10 below). This active pad on the top module receiving the external “in” signal is an “*active port*.” (See INTEL-1001, 9:1–8; INTEL-1001, 9:2 (as modified by COC) (“An **active pad** may be also referred to as an ‘**active port**’”). Because the module receiving the external “in” signal is the top module in the stack, the tri-state buffer couples the “in” signal to shift_in of shift register 294. (See INTEL-1010, ¶49.) The active shift_out signal of the register is then “coupled to the die below 112 through a connector 100.” (*Id.*)

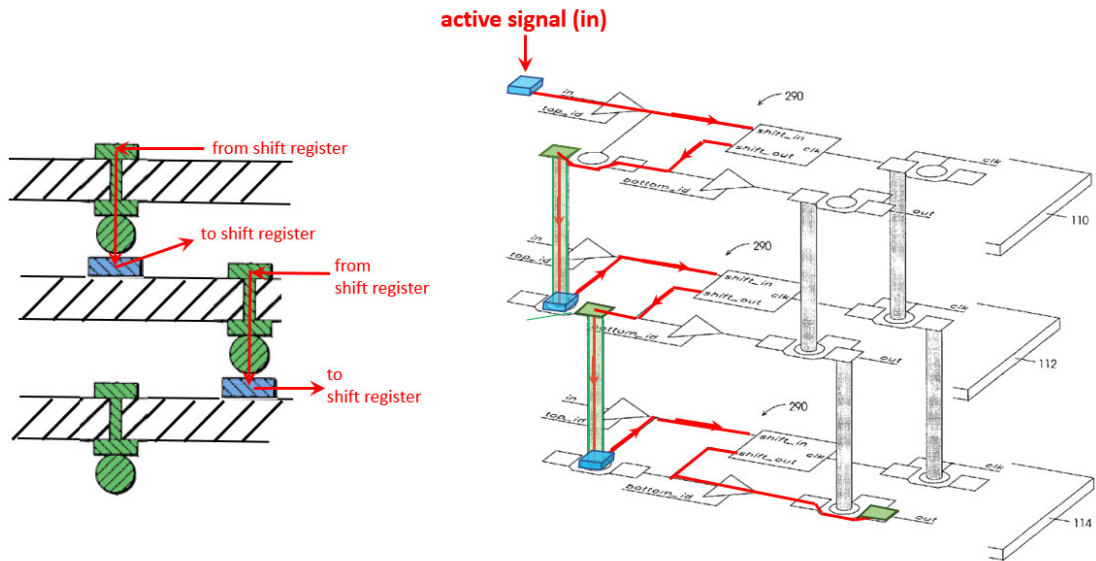


Figure O; Sung, Annotated Figure 10

195. Specifically, in the combination of Sung and Watanabe shown above having Sung’s vertical conductor 2 replaced with Watanabe’s pad-via-ball connection structure (as illustrated above), the shift_out signal is applied to a pad on the upper surface of the top module (shaded green) and traverses through a via to a ball (shaded green) on the lower surface of the top module. The ball on the lower surface of the top module is further coupled to a pad (shaded blue) on the upper surface of the middle module 112, which distributes the signal to shift_in of the shift register on the middle module. (See INTEL-1010, Figure 10.) Because the pad (shaded blue) on the upper surface of the middle module receives and distributes the active signal “in” to the middle module’s circuitry (*i.e.*, the shift register), the pad comprises an “active port” on the middle module.

196. The shift_out signal is then “coupled to the die below 114 through

connector 100.” (INTEL-1010, ¶49.) Specifically, like the top module, the shift_out signal from the shift register on the middle module is applied to a pad (shaded green) on the upper surface of the middle module and traverses through a via to a ball (shaded green) on the lower surface of the middle module. The ball on the lower surface of the middle module is coupled to a pad (shaded blue) on the upper surface of the bottom module 114, which distributes the “in” signal to shift_in of the shift register on the bottom module. (See INTEL-1010, Figure 10.) Because the pad (shaded blue) on the upper surface of the bottom module receives and distributes the active signal to the bottom module’s circuitry (i.e., the shift register), the pad comprises an “*active port*” on the bottom module.

197. Thus, the combination of Sung and Watanabe discloses that each module in its “*stacked module*” includes “*one or more active ports for carrying one or more active signal*” [1B], as required by Petitioner’s “*plurality of modules*” construction. The combination also discloses the “*stacked module*” includes “*one or more active ports for carrying one or more active signal*” [1B], as required by PO’s construction, which only requires “a connection between a passive ball and a passive pad” within the stacked module.

3. “*Passive Port*” [1C].

198. Limitation [1C] recites “*one or more passive ports for passing through the one or more active signals.*” As discussed in §II.E., *supra*, the

Petitioner’s construction of a “*passive port*” is the “connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module.” For the reasons set forth below, the combination of Sung and Watanabe discloses limitation [1C] under Petitioner’s construction, as well as under PO’s broader construction.

a) Petitioner’s Construction of “*Passive Port*”

199. The combination of Sung and Watanabe discloses “*one or more passive ports*” in **each** module. Sung discloses “passive ports” at each layer of the stacked module. As discussed in Sung (¶49) and illustrated in Sung’s Figure 10 (below right), on the top level of the scan chain communication circuit, the “shift_in” signal is coupled to an external “in” signal through a tri-state buffer controlled by the result of the die identifier circuit disclosed in Sung’s Figure 5 (not shown in the diagram below).

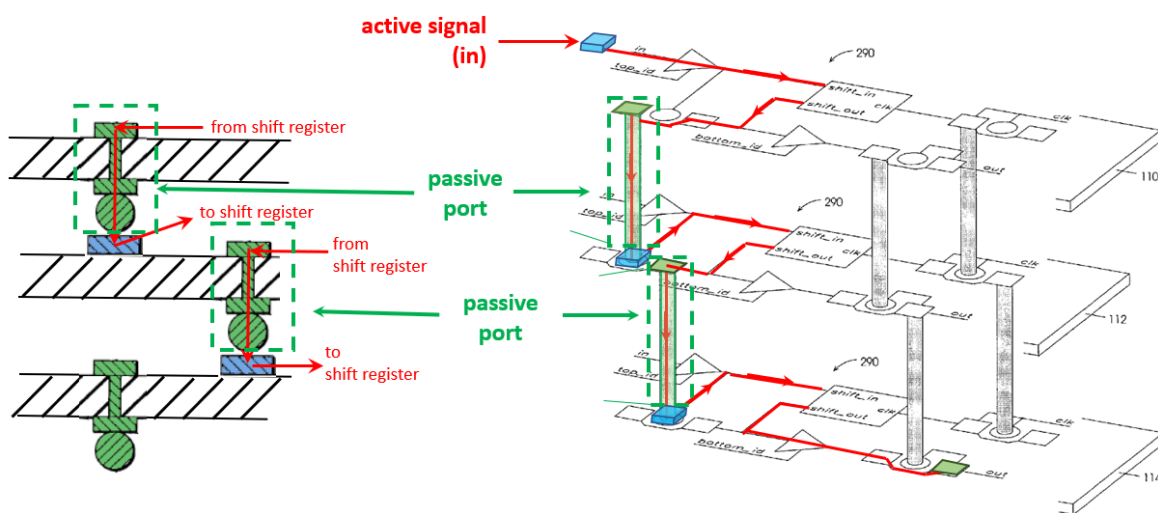


Figure P; Sung, Annotated Figure 10

200. As shown, the output of the shift register in the top and middle modules is coupled to the layer below through the connector 100, which may comprise a bonding pad on one surface of the module vertically interconnected with one of Watanabe's ball connections on the opposite surface by way of one of Watanabe's "through-hole" connections. The pads and balls on each of Sung's modules that pass through the signal from one level to the next are "*passive ports*." Thus, the top layer 110 and middle layer 112 each include a "*passive port*" in the communication circuit that passes signals through to the next lower module in the stack.

201. As shown above, the active shift_out signal from the top module's shift register is applied to a pad (shaded green) disposed on the upper surface of the top module and traverses down through a via such as one of Watanabe's vias shown above left (shaded green) to a ball (shaded green) disposed on a pad on the lower surface of the top module. That pad-via-ball connection through the top module which carries the active shift_out signal to an "*active port*" on the middle module is a "*passive port*" for the top module.

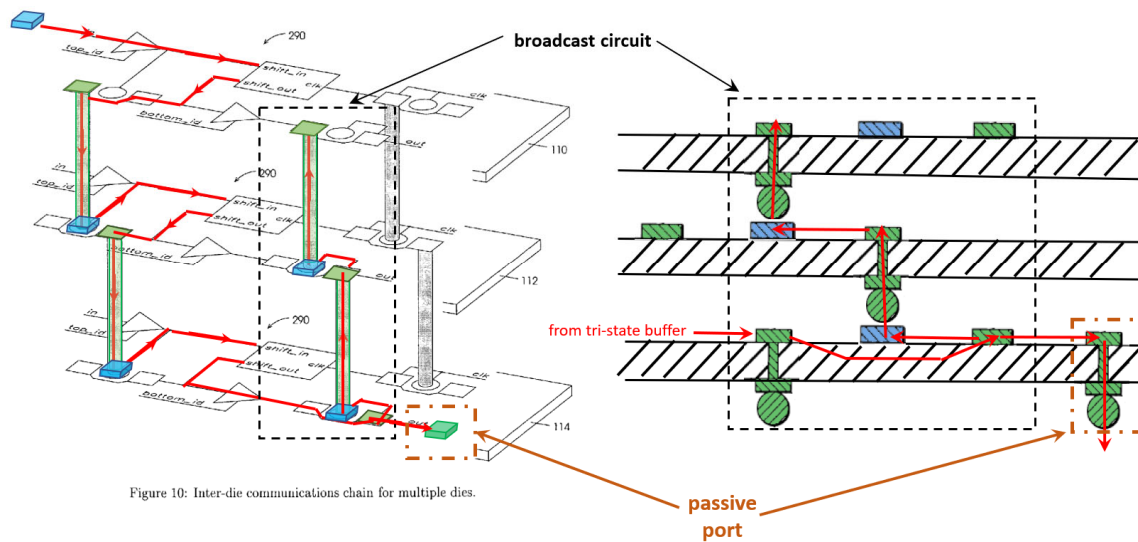
202. Similarly, the active shift_out signal from the middle module's shift register is applied to a pad (shaded green) on the upper surface of the middle module and traverses through a via (shaded green) to a ball (shaded green) disposed on a pad on the lower surface of the middle module. That pad-via-ball

connection through the middle module which carries the active shift_out signal to an “*active port*” on the bottom module is a “*passive port*” for the middle module. The ball on the lower surface of the middle module (part of the middle module’s “*passive port*”) is coupled to the “*active port*” (shaded blue) on the upper surface of the bottom module 114. The signal is then distributed through the bottom module’s shift register to a tristate buffer. (INTEL-1010, ¶49.) But because the module is a bottom (end) module, the tristate buffer couples the active shift_out signal to the module’s output pad (shaded green).

203. Under Petitioner’s constructions, **each** module must include a passive port; and while Sung’s Figure 10 above depicts passive ports associated with the top and middle modules, it does not explicitly show a passive port associated with the bottom module. But a POSITA would have appreciated that, in order for Sung’s stacked module to be integrated into a practical system, it would have been mounted on a main circuit board like the one disclosed in Watanabe in order to exchange external signals with the outside world, such as input and output signals, address and power signals, and the like. I discuss the mounting of the “*stacked module*” in the combination further in my analysis of claims 11 and 12.

204. Watanabe discloses that its main circuit board includes pad connections (terminals) for routing various external signals to and from the

illustrated in Figure Q (below right) created to illustrate the combination.



Sung, Annotated Figure 10 (left), Figure Q

206. As a result, a POSITA would have understood that the bottom layer in Sung’s stack also includes passive ports for exchanging signals with the main circuit board. The pad-via-ball interconnection in the bottom module carrying the active shift_out signal to a location external to the “*stacked module*” comprises a “*passive port*” for the bottom module.

207. Furthermore, **each** module in the “*stacked module*” of the combination of Sung and Watanabe may comprise an SDRAM module as discussed in §IV.B.1. Thus, the combination of Sung and Watanabe discloses that each module in its “*stacked module*” includes “*one or more passive ports for passing through the one or more active signals*” [1C], as required by Petitioner’s “*plurality of modules*” construction. The combination further discloses the

“*stacked module*” includes “*one or more passive ports for passing through the one or more active signals*” [1C] under PO’s “*plurality of modules*” construction.

b) PO’s Construction of “*Passive Port*”

208. Petitioner’s construction of “*passive port*” encompasses PO’s construction. Therefore, for the same reasons above, the combination of Sung and Watanabe teaches a “*passive port*” under PO’s construction. The broadcasting circuit 250 of Sung also includes “*one or more passive ports*” under PO’s construction of “*passive port*.”

209. However, the combination includes “*passive ports*” under PO’s construction for at least one additional reason. Sung’s broadcasting circuit, illustrated in Figure 3 (below right), “sends a signal to all dies within the stack.” (INTEL-1010, ¶47.) Exemplary broadcast signals “include global clocks, addresses, and control signals.” (*Id.*) For example, in the addressing circuit of Figure 9, a broadcast address signal is compared against the die address. (*See* INTEL-1010, ¶48; §IV.A.1(c).) In the combination of Sung and Watanabe shown below, the broadcast address signal (*e.g.*, an external address signal) is applied to the stacked module through a ball on the lower surface of the bottom module and communicated through a via to a pad on the upper surface of the bottom module.

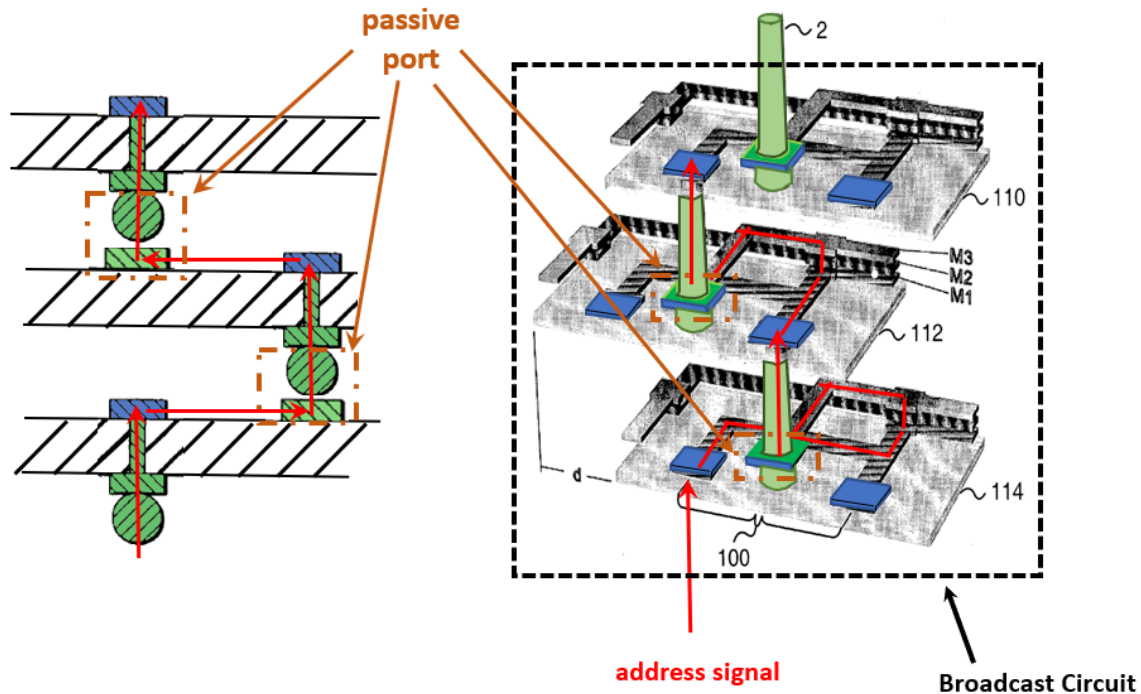


Figure R; Sung, Figure 3

210. The signal traverses a conditional connection as shown by the red line in Figure 3 to a pad (shaded green) on the upper surface of bottom module 114. In the combination, the pad on the upper surface of bottom module 114 is coupled to a ball on the lower surface of middle module 112 as discussed above. The pad (shaded green) on bottom module 114 and ball on middle module 112 is a “*passive port*” that carries the active address signal. A similar pad and ball connection exists between a pad (shaded green) on the upper surface of middle module 112 and a ball on the lower surface of upper module 110.

211. For this additional reason, the combination of Sung and Watanabe discloses the “*passive port*” limitation under PO’s construction for “*passive port*”

and “*plurality of modules*”.

4. “*First Serial Chain Route*” [1D].

212. The combination of Sung and Watanabe discloses “*a first serial chain route that includes at least one serial chain connection*” [1D].

a) “*Serial Chain Connection*”

213. The claim recites that a “*first serial chain route*” includes “*at least one serial chain connection,*” which comprises a serial chain circuit having an input and an output. The combination of Sung and Watanabe discloses two types of “*serial chain connection[s]*”—a vertical pad-via-ball serial chain connection and a horizontal serial connection through the shift register at each stacked layer.

214. **Vertical “*Serial Chain Connection*”:** In the inter-module scan chain circuit of the combination of Sung and Watanabe (illustrated in annotated Figure 10 and Figure S below created to illustrate the combination), the shift_out output signal of the shift register is passed to a pad on the upper surface of the top module and through a via to a ball on the lower surface of the top module. (See §IV.B.3.) The top module 110 provides the shift_out signal to a pad connection (green) on the module’s upper surface, which may be interconnected to one of Watanabe’s ball connections on the top module’s bottom surface by one of Watanabe’s through-hole vias, as shown in the diagram below. The middle module 112 and lower module 114 include similar connections as shown.

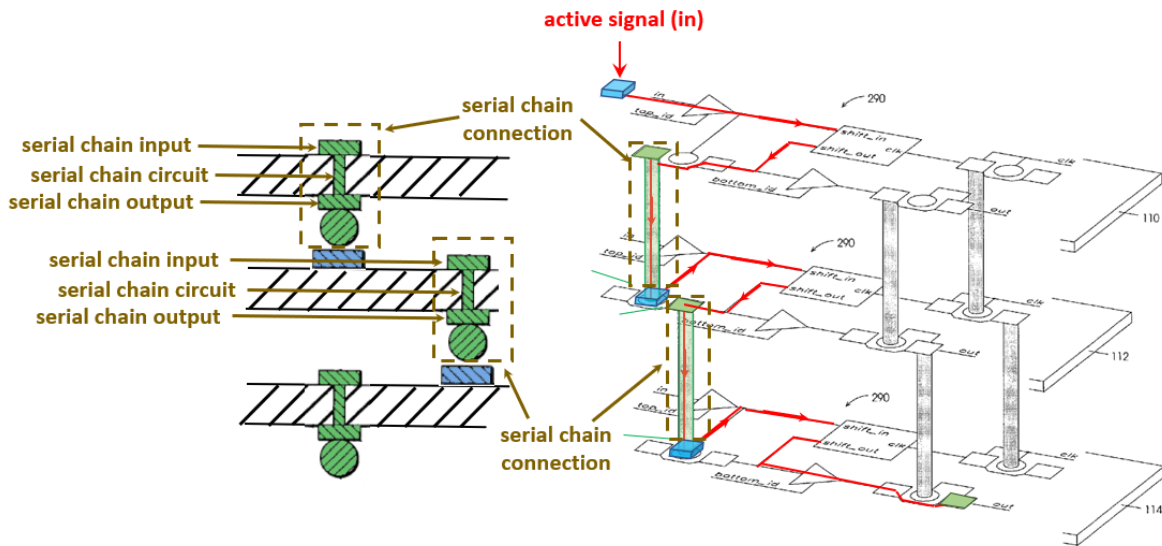
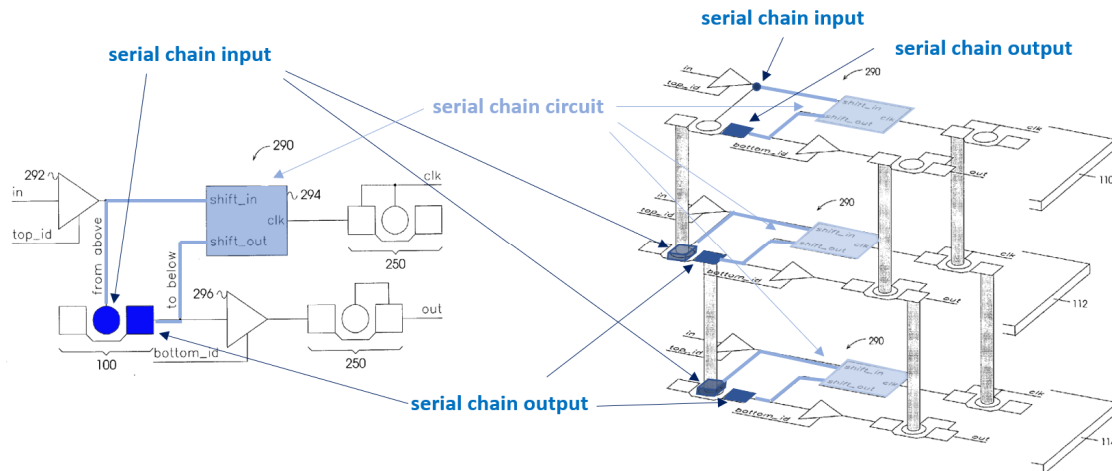


Figure S; Sung, Annotated Figure 10

215. The pad-via-ball structure in the top module is therefore a “*serial chain connection*” with the pad on the upper surface receiving the signal being a “*serial chain input*”, the via coupling the pad and ball being the “*serial chain circuit*”, and the ball on the lower surface providing the signal to the next module being the “*serial chain output*.” (INTEL-1001, 10:8 (as modified by COC); INTEL-1005, 2 (“A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal”/“serial chain circuit coupl[es] a[] ball and pad”).)

216. **Horizontal “*Serial Chain Connection*”:** Each module in the combined “*stacked module*” of Sung and Watanabe also includes a “*serial chain connection*” in the horizontal direction through the shift register as shown in annotated Figures 8 and 10 below.



Sung, Annotated Figures 8 and 10

217. Figure 8 illustrates a one-bit slice of a “communications chain that communicates data between storage elements on adjacent dies.” (INTEL-1010, ¶35.) In this circuit, “[o]n the top die 110, shift_in is coupled to in (an external signal) through a tristate buffer 292.” (INTEL-1010, ¶49.) The shift_in input on the top module is a “*serial chain input*.” The shift_out signal from the shift register is coupled to a pad on the upper surface of the top module. Thus, the connection from the shift_in input to the shift register, through the shift register to the pad is a “*serial chain circuit*” and the pad is the “*serial chain output*.” The “*serial chain input*”, “*serial chain circuit*” and “*serial chain output*” form the horizontal “*serial chain connection*.” (INTEL-1001, 10:8; INTEL-1005, 2 (“A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal”/“serial chain circuit coupl[es] a[] ball and pad”).) Each module in the “*stacked module*” of the combination of Sung and Watanabe includes a similar

horizontal “*serial chain connection*” as shown in annotated Figure 10 below right.

b) “First Serial Chain Route” – Petitioner’s “Plurality of Modules” Construction

218. Petitioner’s “*plurality of modules*” construction requires each module in the stack to include a “*first serial chain route*.” As discussed above, each module in the combined “*stacked module*” of the combination of Sung and Watanabe includes a horizontal “*serial chain connection*” in the scan chain circuit. Additionally, the top and middle modules include vertical “*serial chain connections*” in the scan chain circuit. Thus, the combination of Sung and Watanabe discloses “*a first serial chain route that includes at least one serial chain connection*” [1D] as illustrated in annotated Figure 10 below under Petitioner’s construction.

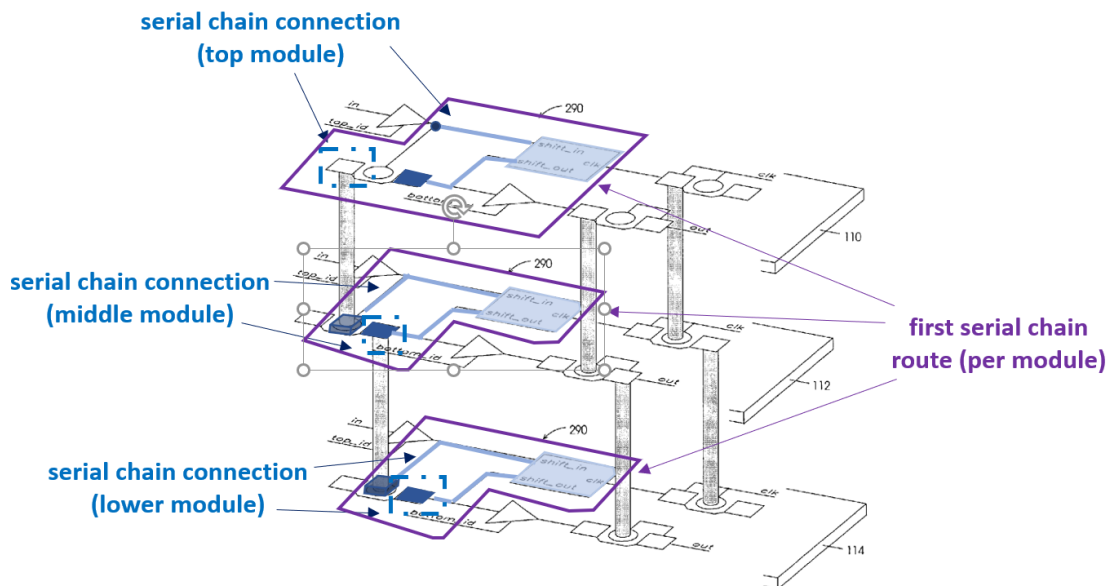
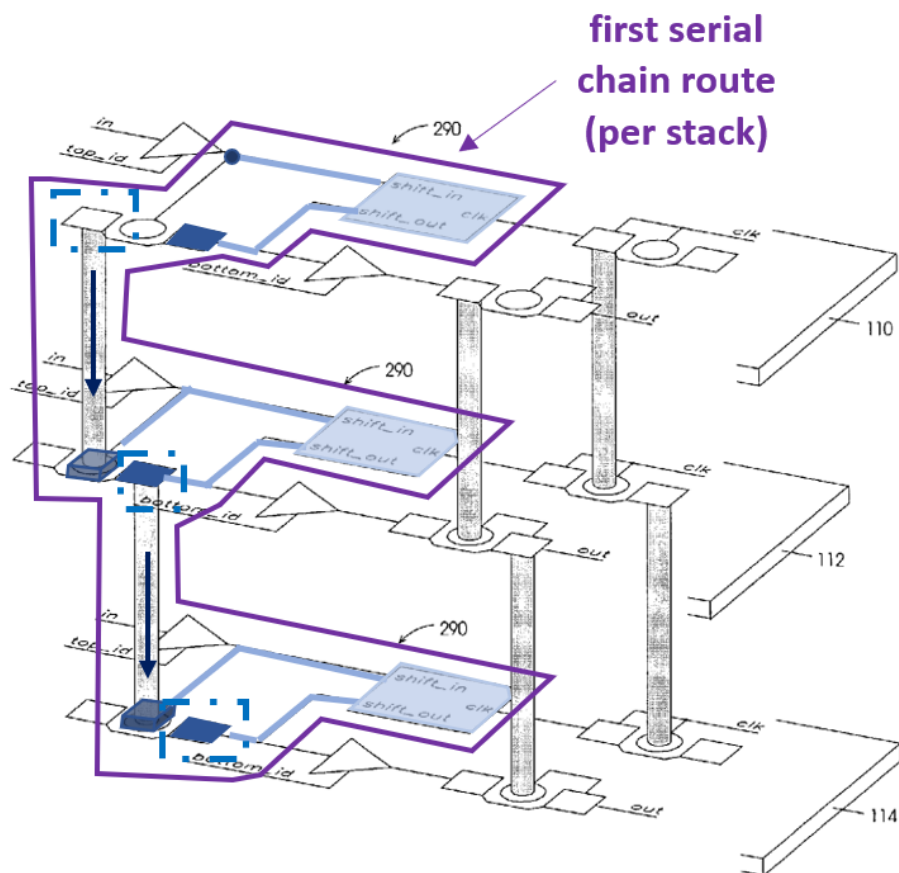


Figure 10: Inter-die communications chain for multiple dies.

Sung, Annotated Figure 10

c) **“First Serial Chain Route” – PO’s “Plurality of Modules” Construction**

219. PO’s “*plurality of modules*” construction requires the entire “*stacked module*” to include a “*first serial chain route*.” But as discussed above, the “*stacked module*” includes multiple “*serial chain connections*” because each stacked module includes both vertical and horizontal “*serial chain connection[s]*” as discussed in §IV.B.4(a). As depicted below in annotated Figure 10, the combination of Sung and Watanabe discloses “*a first serial chain route that includes at least one serial chain connection*” [1D] under PO’s construction.



Sung, Annotated Figure 10

5. “*Second Serial Chain Route*” [1E] and “Control Circuit” [1F].

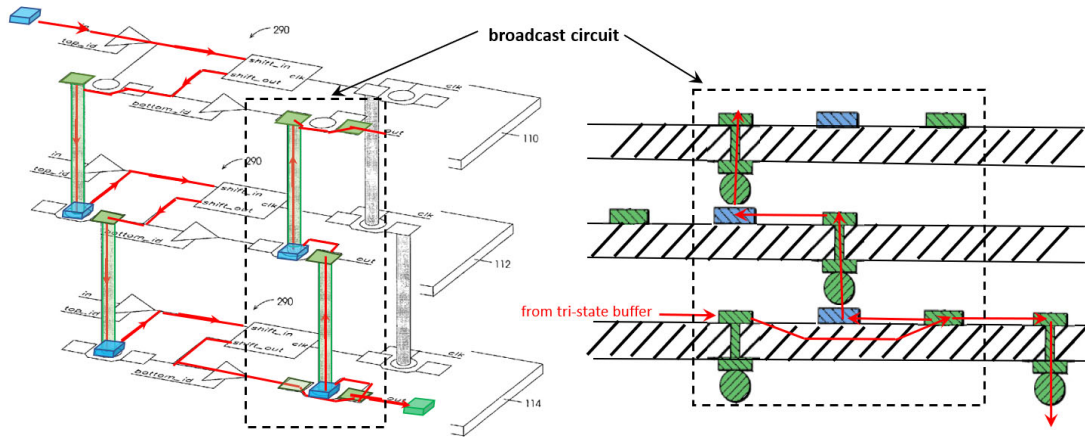
220. The combination of Sung and Watanabe discloses “*a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module* [1E], *said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module*” [1F].

a) “*Second Serial Chain Route*” - Petitioner’s Construction

221. The combination of Sung and Watanabe discloses a “*second serial chain route.*” Unlike the “*first serial chain route*” limitation [1D], the “*second serial chain route*” limitation does not recite that the route includes “*at least one serial chain connection.*” However, should PO contend the “*second serial chain route*” requires one or more “*serial chain connections*”, the combination of Sung and Watanabe satisfies the claim limitation for the reasons set forth below.

222. In the bottom module of Sung’s boundary scan chain circuit, illustrated in Figure 10 below (left), the shift_out signal from the shift register “is coupled by a tristate buffer 296 to a **broadcasting circuit 250** that conveys the data to the top of the stack 110 and then to a location external to the stack.”

(INTEL-1010, ¶49.)



Sung, Annotated Figure 10 (left); Figure T (right)

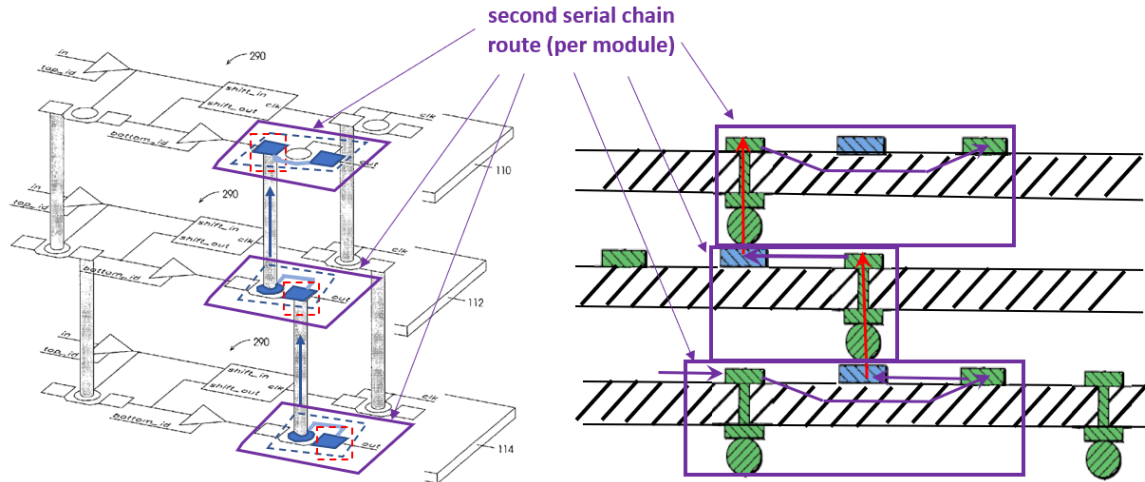
223. As shown, the shift_out signal enters the broadcast circuit on the bottom module at a connector pad (shaded green), is transmitted to a second connector pad (also shaded green) via substrate wiring, and then to the central connector pad (shaded blue) via substrate wiring where the signal is output to the next layer in the stack. This path, having an input, circuit (substrate wiring), and output, is a “*serial chain route*” through the module as well as a “*serial chain connection*.”

224. In the combination of Sung and Watanabe, the output signal from the bottom module is communicated to the middle module by the pad-via-ball connection of the middle module as illustrated in Figure T created to illustrate the combination (above right). This connection comprises a “*serial chain route*” through the middle module and a “*serial chain connection*.” In the middle module, the right connector pad (shaded green) transmits the signal to the central connector

pad (shaded blue) via substrate wiring. This path is also a “*serial chain route*” and “*serial chain connection*” in the middle module.

225. The output signal is communicated from the middle module to the top module by the pad-via-ball connection of the top module as illustrated in Figure T (above right). This connection is a “*serial chain route*” through the top module and a “*serial chain connection.*” In the top module, the left connector pad (shaded green) transmits the signal to the right connector pad (shaded green) and then to an output connection for the top module. This final path is also a “*serial chain route*” and a “*serial chain connection.*”

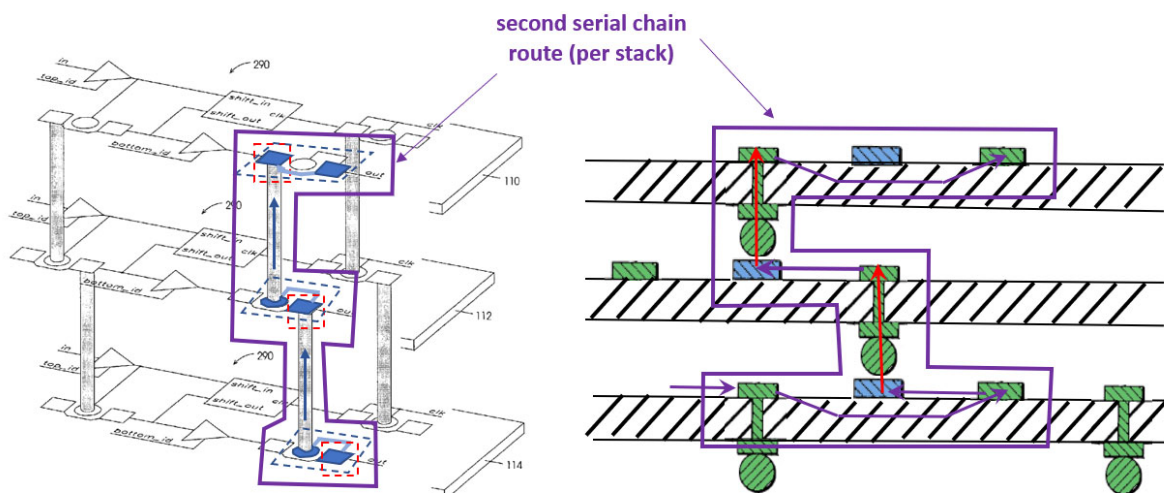
226. Petitioner’s “*plurality of modules*” construction requires *each* module in the stack to include a “*second serial chain route.*” Each module in the combined “*stacked module*” of Sung and Watanabe includes one or more “*second serial chain routes*” as illustrated below. Thus, the combination of Sung and Watanabe discloses “*a second serial chain route*” [1E] under Petitioner’s construction, as illustrated in Sung Figure 10 and Figure U created to illustrate the combination.



Sung, Annotated Figure 10 (left), Figure U (right)

(4) “Second Serial Chain Route” – PO’s “Plurality of Modules” Construction

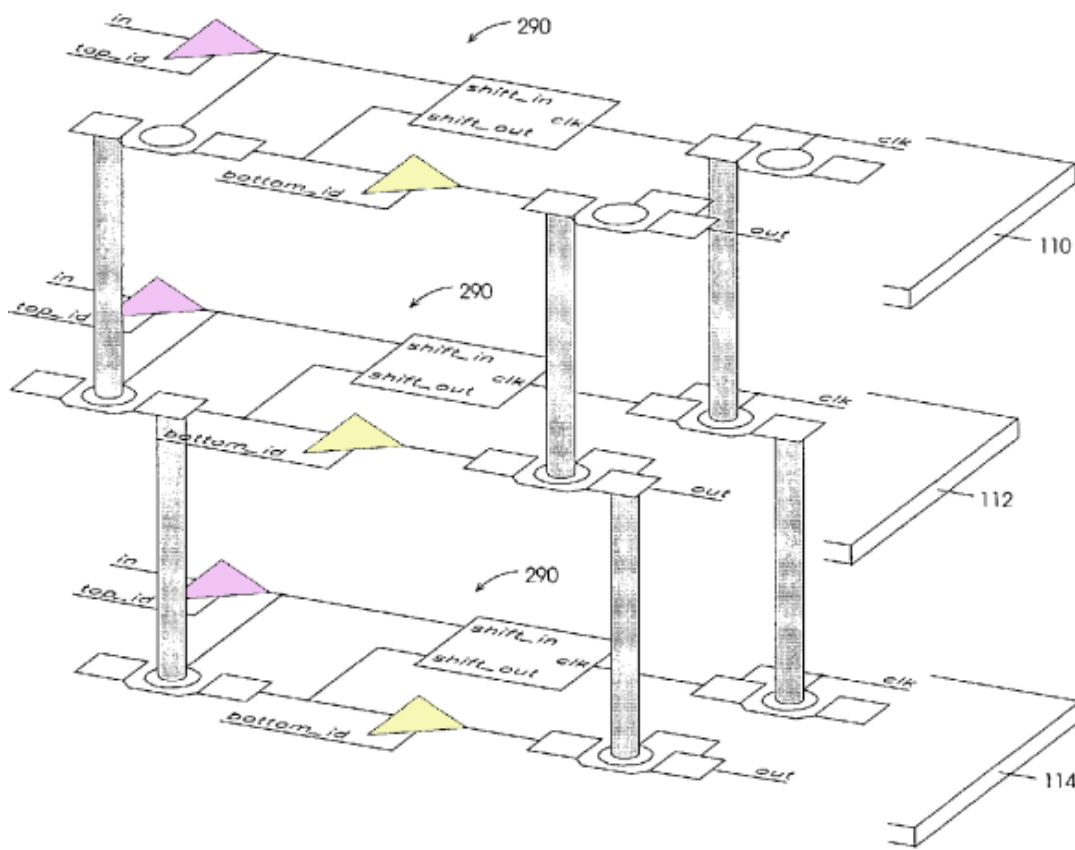
227. PO’s “*plurality of modules*” construction requires the entire “*stacked module*” to include a “*second serial chain route*.” The “*stacked module*” includes multiple second “*serial chain connections*” as discussed in §IV.B.5(a). Further, the combination of Sung and Watanabe discloses “*a second serial chain route*” under PO’s construction as illustrated below in Sung Figure 10 (left) and Figure V (right) created to illustrate the combination.



Sung, Annotated Figure 10 (left), Figure V (right)

b) “Control Circuit”

228. The combination of Sung and Watanabe also discloses “a control circuit for enabling a routing path” [1D]. Redirection of data within Sung’s inter-die scan chain network, illustrated in Figure 10 below, “relies upon the identification of both the top die 110 and bottom die 114.” (INTEL-1010, ¶49.) The top and bottom modules in the “*stacked module*” of Sung and Watanabe are each “*end modules*.” A first tri-state buffer in each layer (shaded pink) “is controlled by the result (top_id) of the top die identifier circuit 220.” (*Id.*) A second tri-state buffer in each layer (shaded yellow) “is controlled by the bottom_id signal generated by the bottom die identifier circuit 230.” (*Id.*) As a result, the first tri-state buffer is only enabled in the top die (module) and the second tri-state buffer is only enabled in the bottom die (module).

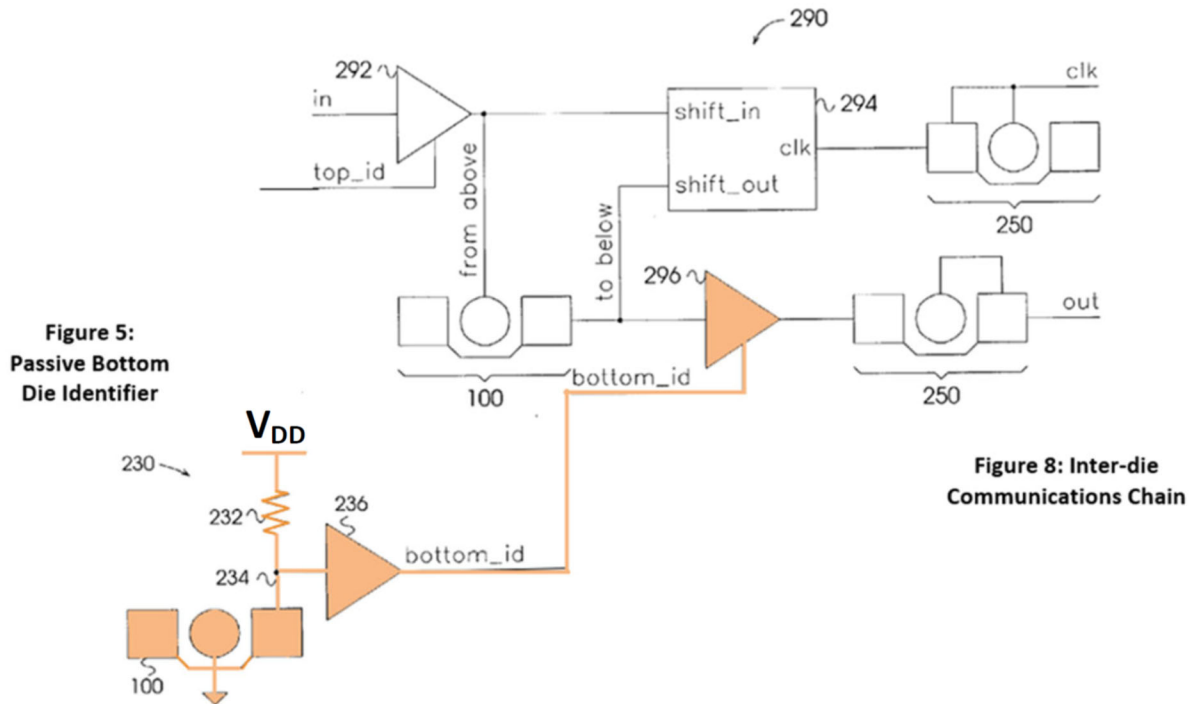


Sung, Annotated Figure 10

229. The diagram below integrates bottom die identifier circuit 230 of Sung’s Figure 5, which generates the bottom_id signal, with Figure 8 depicting a “one-bit slice of an inter-die scan chain 290.” (See INTEL-1010, ¶¶46, 49.) In the bottom die identifier circuit 230, the left and right terminals of connector 100 are coupled to a weak pull-up device 232. (See INTEL-1010, ¶46.) A POSITA would have understood that the weak pull-up device comprises a resistor (labeled 232) connected to a voltage source (labelled as voltage V_{DD} by Petitioner for exemplary purposes).

230. As shown, the center terminal of connector 100 (represented as an

orange circle) is coupled to ground but is not coupled to the left and right (square-shaped) terminals. In this configuration, the signal on node 234 is output by the tri-state buffer 236 to provide the signal “bottom_id” as the control input signal for enabling/disabling the tri-state buffer 296.



Sung, Partial Figure 5 and Figure 8 (Annotated)

231. The control input of tri-state buffer 296 tri-states the input when pulled low (when bottom_id is not asserted) to disable a routing path between the buffer input and output. When the control line is pulled high (bottom_id asserted), the tri-state buffer 296 enables the routing path from its input (*i.e.*, the shift_out output of the shift register 294) to its output (which is coupled to broadcast circuit 250). The combination (shaded orange in the diagram) of the bottom die

identification circuit 230 and tri-state buffer 296 comprises a “*control circuit*” that enables a “*routing path*” because it is the circuitry that controls the signal flow in the module by “*enabling (or disabling) a routing path*” [1E]. As discussed above, Sung discloses a “*control circuit*” which includes (i) a bottom die detector circuit 230 of Sung’s Figure 5 that asserts and de-asserts the bottom_id “*control input signal*,” and (ii) a tri-state buffer 296 shown of Figures 8 and 10 that enables or disables the routing path in response to the bottom_id “*control input signal*”.

232. The diagram below illustrates operation of the bottom die identifier circuits 230, illustrated in Figure 6 (left), with the scan chain circuit of Figure 10 in the stacked module (right). As shown, each module in the stack includes a “*control circuit*” that is either enabled or disabled. In the top module, the left connector terminal (shaded black) is grounded because it is coupled to the center connector terminal (shaded black) in the bottom die identifier circuit of the middle module, which is connected to ground (also black). Similarly, in the middle module, the right connector terminal (shaded black) in the bottom die identifier circuit is grounded because it is coupled to the center connector terminal (shaded black) in the bottom die identifier circuit of the bottom module, which is also connected to ground. Therefore, the top module receives “ground” from the middle module stacked below it and the middle module receives “ground” from the bottom

module stacked below it.

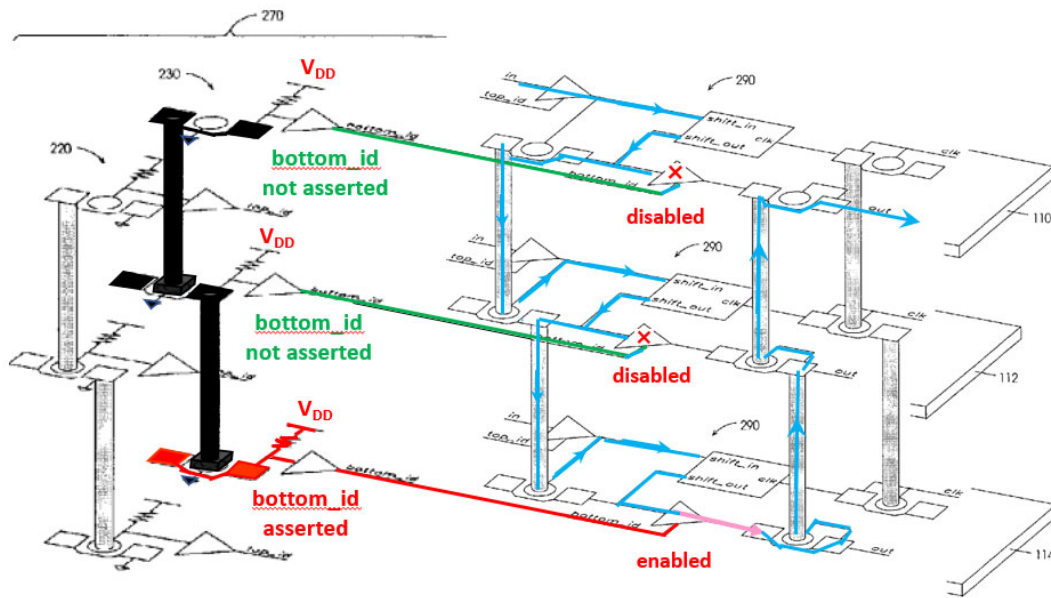


Figure 6: Die Identification Circuit

Figure 10: Inter-die communications chain for multiple dies.

Figure 10

Sung, Annotated Figures 6 and 10

233. A POSITA would have understood that when a ground connection is provided by the module stacked below in this manner, it overrides the weak pull-up on the tri-state buffer 296's control line provided by the resistor 232 coupled to voltage V_{DD} . Accordingly, when Sung's modules have another module stacked below—(i) the bottom_id identification circuit is grounded, (ii) the bottom_id control signal is not asserted, and (iii) the tristate buffer 296 in the scan chain circuit is disabled, which in turn disables its routing path from input to output. This is consistent with the operation of the '243 patent, discussed further below, in which connection of the StkLow ball to ground disables routing path 2120.

234. Thus, the routing path is enabled or disabled based on the presence or absence of the ground signal pulling down the control line “bottom_id” to the tri-state buffer 296, which, for the top and middle modules, is provided by another module in the stack when the modules are coupled together. As a result, for the top and middle modules, the “ground” signal is a “*control input signal received from another module from the plurality of modules,*” which pulls low the bottom_id control signal. The “*control circuit*” in those modules **disables** the “*routing path*” through the tri-state buffer 296 “*in response to a control input signal received from another module from the plurality of modules.*”

235. But Sung’s bottom module does not receive the ground signal from another module because there are no other modules stacked below to provide it. In the bottom module, which is an “*end module*”, the left and right terminals in the bottom die identification circuit are not connected to ground. As a result, the bottom_id “*control input signal*” to the tri-state buffer 296 on the bottom module is pulled high by the weak pull-up device 232 (*i.e.*, it is not overridden by ground). This enables the routing path (shaded pink) as shown in the diagram above connecting the input of the tristate buffer 296 to its output and further to the broadcast circuit 250. As discussed below, the voltage V_{DD} of the weak pull-up device 232 that pulls high the bottom_id control signal, is provided to the bottom module (“*end module*”) by “*another module*” in the stack by way of Sung’s high-

density, low-resistance, high-current carrying connection 260.

236. In particular, Sung discloses a connector array 210 which “provides a high-density, low-resistance, high current carrying connection 260.” (INTEL-1010, ¶47, Figure 6 (below).) Connection 260 “is suitable for routing fixed-potentials between dies.” (INTEL-1010, ¶47.) A POSITA would understand that a “fixed potential” in this context refers to a fixed electrical potential, or otherwise known as a fixed voltage such as V_{DD} or ground potential.

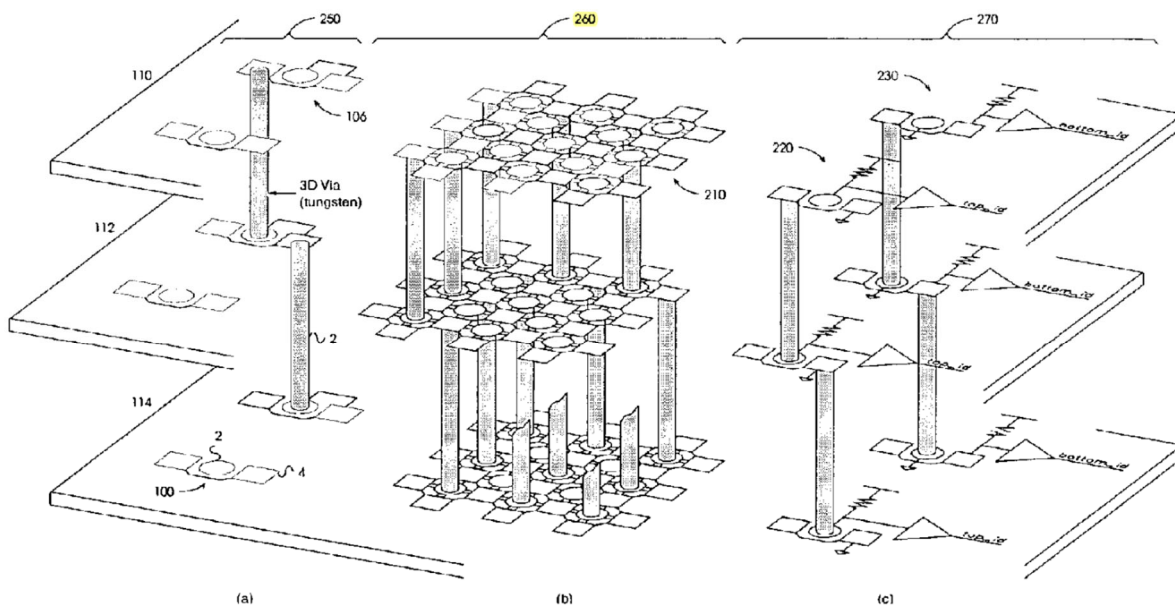


Figure 6: Inter-die communication circuits.

237. Thus, Sung’s connection 260 provides a pathway for routing fixed voltages between the layers in the stack. For example, the voltage V_{DD} (fixed voltage) comprises a “fixed potential” and is provided to each layer in the stack using connection 260. The same is true for ground potential, which a POSITA would understand is a fixed voltage of zero volts. Sung therefore teaches that fixed

voltages such as V_{DD} and ground may be routed throughout the stacked layers using connection 260.

238. Sung's connection 260 is configured to provide power and ground to each of the modules up and down the stack. For example, voltage V_{DD} may be provided throughout the stack using connection 260, which comprises conductors that conduct voltages such as V_{DD} from one staked layer to another. For example, connection 260 is configured to conduct V_{DD} from the top and middle modules ("*another module*") to the bottom module ("*end module*") and vice versa. This voltage V_{DD} provided to the bottom module by one of the other modules is the same voltage source that is used for the weak pull-up device 232 to pull high the "bottom_id" control input signal in bottom die self-identifier circuit 230, which enables the routing path in the bottom module's tri-state buffer 296.

239. Accordingly, the combination of Sung and Watanabe discloses that in the bottom module "*said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module*" [1F].

c) Connecting First and Second "*Serial Chain Routes*"

240. In addition, as shown in annotated Figure 10 below, when the routing path through the tristate buffer is enabled in the bottom module ("*end module*"), the "*first serial route connection*" in the bottom module is coupled to the "*second*

serial route connection” in the bottom module. Thus, the combination of Sung and Watanabe discloses “a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module” [1D] as required by Petitioner’s “*plurality of modules*” construction.

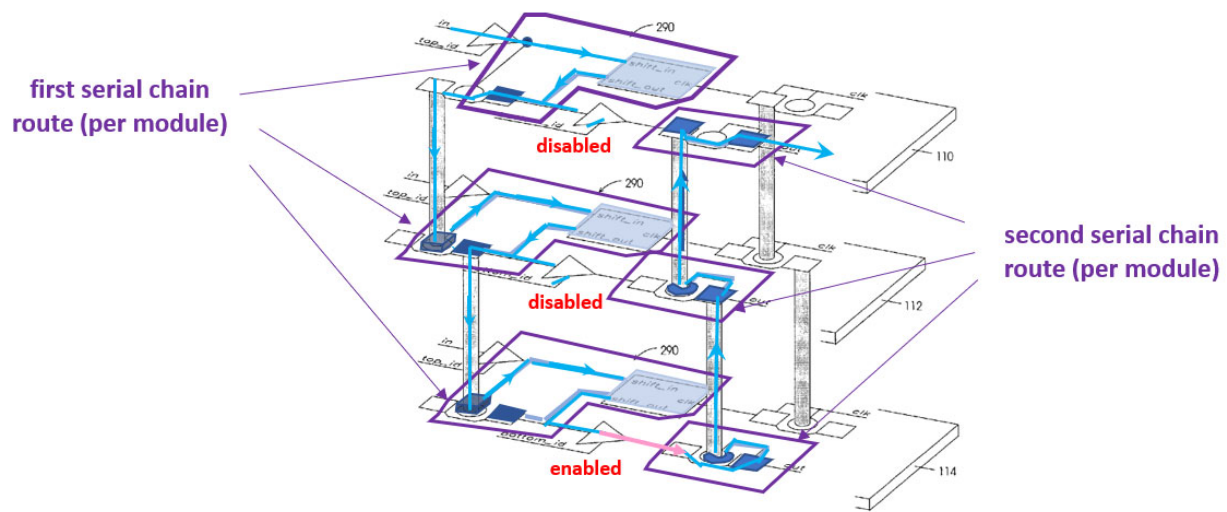


Figure 10: Inter-die communications chain for multiple dies.

Sung, Annotated Figure 10

241. Furthermore, as shown in annotated Figure 10 below, when the routing path through the tristate buffer is enabled in the bottom module (“*end module*”), the “*first serial route connection*” in the “*stacked module*” is coupled to the “*second serial route connection*” in “*stacked module.*” Thus, the combination of Sung and Watanabe discloses “a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module” [1D] as required by PO’s “*plurality of modules*” construction.

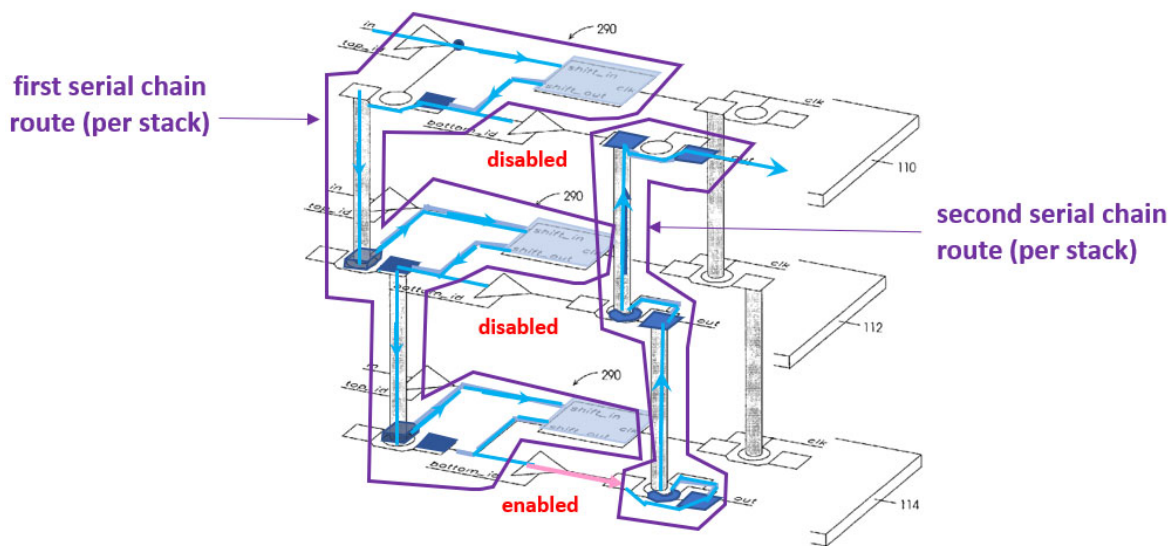


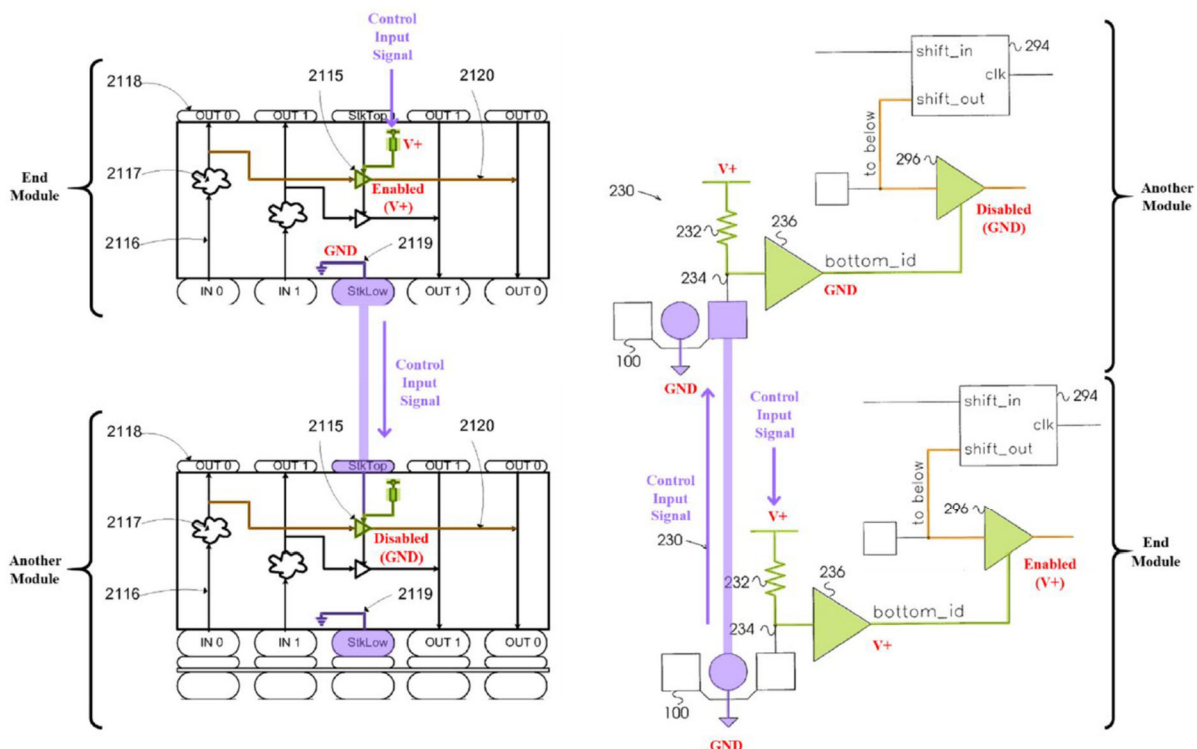
Figure 10: Inter-die communications chain for multiple dies.

Sung, Annotated Figure 10

d) Sung's Control Circuit Operates in Same Matter as Control Circuit of the '243 Patent

242. Sung's "*control circuit*" operates in the same manner as the control circuit described in the '243 patent, as highlighted by in the diagram below comparing two stacked modules excerpted from '243 patent's Figure 21b (below left) and Sung's Figures 5 and 8 (below right). The '243 patent's control circuit, illustrated in the excerpt from Figure 21b, includes "a selectable buffer 2115 that tri-states the input when pulled low." (INTEL-1001, 10:10–11.) As shown, the "SktTop" pad on the top module is not coupled to another module, so the control input to the tri-state buffer 2115 "is pulled high" by the voltage source which "let[s] the input signal branch out 2120 to the other pads, thus creating a

connection route or trace that loops back to the base module solder balls.” (INTEL-1001, 10:18–20.)



**'243 Patent, Annotated Excerpts from Figure 21b;
Sung, Annotated Excerpts from Figures 5 and 8**

244. In the corresponding disclosure in the Sung embodiment on the right-hand-side of the diagram, the ground signal is received from the modules stacked below for all modules except the bottom module, which is an “*end module*” because it does not have another module stacked below. The ground signal controls the tri-state buffer 296 that enables the routing path in Sung.

245. Therefore, Sung’s “*control circuit*” is disposed to enable a routing path in response to the bottom_id “*control input signal*” that is received from “*another module*” in the stack when the end module is “*coupled to the another module*” in exactly the same manner as the modules described in the ’243 patent.

246. The combination of Sung and Watanabe therefore renders obvious limitations [1E] and [1F].

C. Claim 2

247. As discussed in §IV.B.3., *supra*, the combination of Sung and Watanabe discloses “*the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module*” [2B]. As illustrated in Sung’s Figure 10 (right) and Figure W created to illustrate the combination, the passive ports in Sung’s scan chain circuit 290 are staggered forming a ladder-like

routing path through the stack. “This staggered alignment of alternating dies facilitates the connection of signals from the current die to the die above, the die below or both dies,” and thus forms a ladder-like routing path with both (i) vertical portions for routing signals along the direction of the vertical conductors, and (ii) horizontal portions for routing signals through the circuitry disposed on each of the stacked modules. (INTEL-1010, ¶44.) As a result, the combination also discloses “the one or more passive port forms a ladder like routing path” [2A].

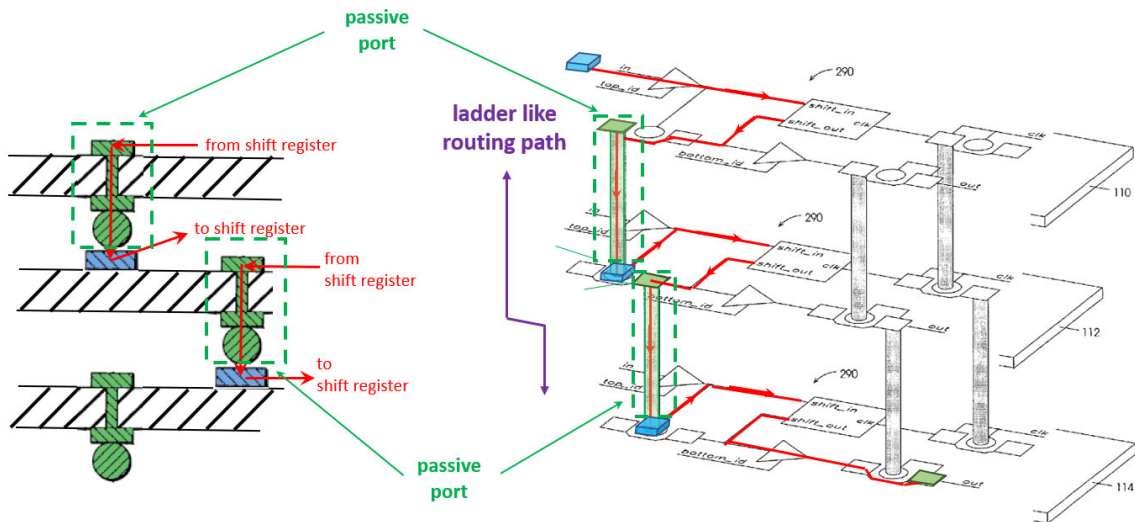


Figure W; Sung, Annotated Figure 10

D. Claims 11 and 12

248. The combination of Sung and Watanabe discloses that “one or more of the plurality of modules includes a main board” [11] and the “one or more vertically stacked module is connected to the main board” [12]. One object of Sung is to provide “a method for communicating **externally** to, **externally** from or

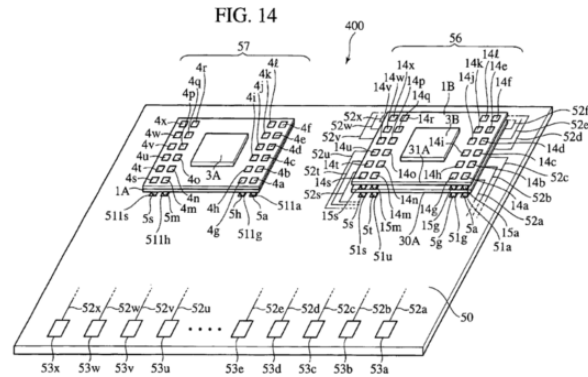
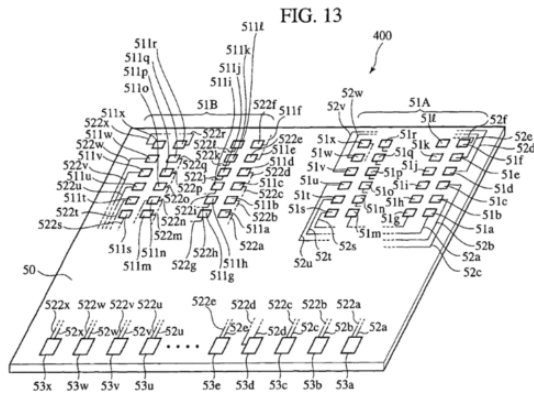
communicating between, dies in the stack.” (INTEL-1010, ¶18.) Sung repeatedly refers to receiving “external data input”, clocks, addresses, control signals and providing “external data output.” (INTEL-1010, ¶¶18, 47, claims 70–72.) Sung, however, does not provide any details for connecting its stacked module with an external component that provides signals to and/or receives signals from the stacked module.

249. But as a practical matter, a POSITA would understand that implementations of Sung’s stacked module would be mounted on a main circuit board to form an operational electronic device. Electronic systems include integrated circuit packages mounted on a printed circuit board in order to exchange external signals needed for operation, such as input/output signals, address and power signals, and the like.

250. Nonetheless, Watanabe discloses this feature. As illustrated in Figures 13 and 14 below, Watanabe discloses that its “second level assembly 400” includes a first level assembly that is “**mounted on a board.**” (referred to as “packaging substrate 50”).

A second level assembly in the hierarchy indicates an assembly in which the first level assembly is **mounted on a board**. The second level assembly in the hierarchy includes a second level assembly 400 as shown in FIG. 14.

(INTEL-1011, 3:32–36, Figures 13–14.)



Watanabe, Figures 13 and 14

251. Watanabe's packaging substrate 50 is a main board because it is adapted to exchange external signals, such as power and address signals, with the stacked module.

In the first connection terminals 51a, 51b, 51c, ..., 51x, ... disposed in the first substrate mounting area 51A ... included are: an ADD terminal 51a **for supplying the address signal**; an input and output terminal 51b **for supplying the input and output signal**; chip selection terminals 51c and 51d for selecting the semiconductor chips; a **GND terminal** 51e; and a **VDD terminal** 51f and the like.

(INTEL-1011, 11:25–37.)

252. This is consistent with the '243 patent's description: “[s]everal pin assignments and signal routing techniques are illustrated wherein internal an external signals are routed form [the] main board to various stacked modules.”

(INTEL-1001, Abstract (“internal and external signals are routed from main board to various stacked modules.”); *see also* INTEL-1001, 9:61–67.)

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. FIG. 21a shows how this

technique is implemented in the stacking method. The main board contains the input signals 2102 which will then be connected to IN ball 2104 of the base module 2103.

Therefore, Watanabe's packaging substrate 50 of the second level assembly 400 comprises a "*main board*" because it is a printed circuit board, and it is adapted to exchange external signals with the stacked module.

253. Based on the express suggestions in Sung discussed above, a POSITA would have been motivated to combine Sung's stacked module with Watanabe's teachings concerning a second level assembly mounted on a main board. For example, a POSITA would have been motivated to couple Sung's stacked module to the packaging substrate 50 of Watanabe's second level assembly.

254. Further, when the "*stacked module*" of SDRAM modules is mounted on the main board, as taught by Watanabe, the main board is one of the modules of the package. In Watanabe, the operational modules (first level assemblies) are mounted and functionally interconnected on a main board, which provides horizontal interconnections between the first level assemblies, as well as external connections for exchanging external signals. Therefore, the combination of Sung and Watanabe discloses "*one or more of the plurality of modules includes a main board*" [11] and the "*vertically stacked module is connected to the main board*" [12].

255. A POSITA would have been motivated to couple Sung's stacked

module to Watanabe's main board to form an operational electronic device. Sung teaches that its stacked modules include "storage elements" (*i.e.*, memory). (See INTEL-1010, ¶24.) A POSITA would have understood that in practical implementations, a stacked module, such as a memory module, would be used with a CPU (or other type of microcontroller) with a memory controller adapted to supply external electrical signals into a stacked memory module for performing operations such as reading and writing data. For example, a memory controller provides read enable signals, write enable signals, address signals such as column access strobe (CAS) signals and row access strobe (RAS) signals, chip select signals and the like, to memory module. (See §IV.A.3.)

As early DRAMs grew in capacity, the cost of a package with all the necessary address lines was an issue. The solution was to multiplex the address lines, thereby cutting the number of address pins in half. Figure 5.12 shows the basic DRAM organization. One-half of the address is sent first, called the row access strobe (RAS). The other half of the address, sent during the column access strobe (CAS), follows it. These names come from the internal chip organization, since the memory is organized as a rectangular matrix addressed by rows and columns.

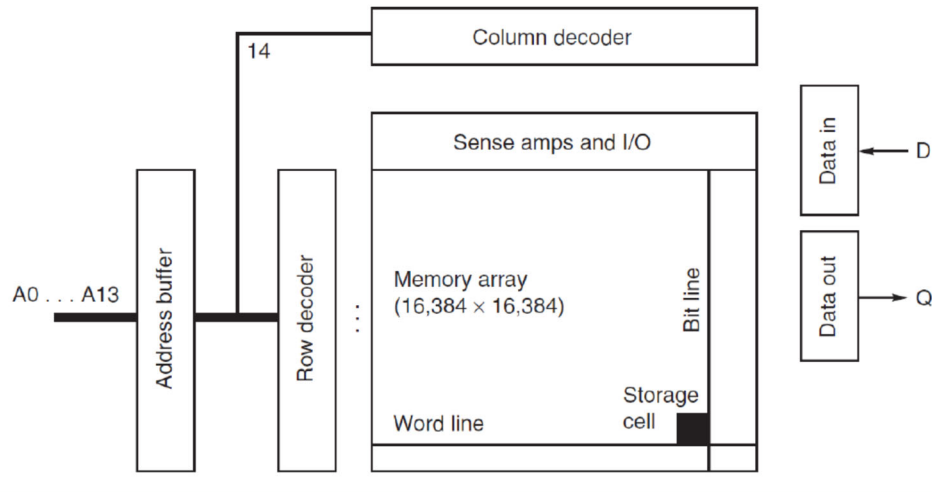


Figure 5.12 Internal organization of a 64M bit DRAM. DRAMs often use banks of memory arrays internally and select between them. For example, instead of one $16,384 \times 16,384$ memory, a DRAM might use 256 1024×1024 arrays or 16 2048×2048 arrays.

(INTEL-1024, 311.)

256. A POSITA would have understood that a common way to implement a device with CPU and memory stack is to mount both on a printed circuit board as taught by Watanabe. The integration of a module including a CPU into a stacked module was known prior to the '243 patent. For example, the NASA paper discussed above describes a stacked module mounted on a printed circuit board that includes a CPU at one level of the stack and a local memory module at another level of the stack. (See, e.g., INTEL-1022, 44–45, Figures 1–2.)

Figure 1 shows a block diagram of the space flight computer. The processor module (one slice of the stack), ... [t]he second module contains 400 Mbytes of local memory implemented with five 3D memory cubes of 16-Mbit DRAM chips stacked 40 high. ... The MCMs are mounted on printed circuit boards stacked in three dimensions with elastomeric interconnections. Figure 2 depicts the 3D MCM stack approach.

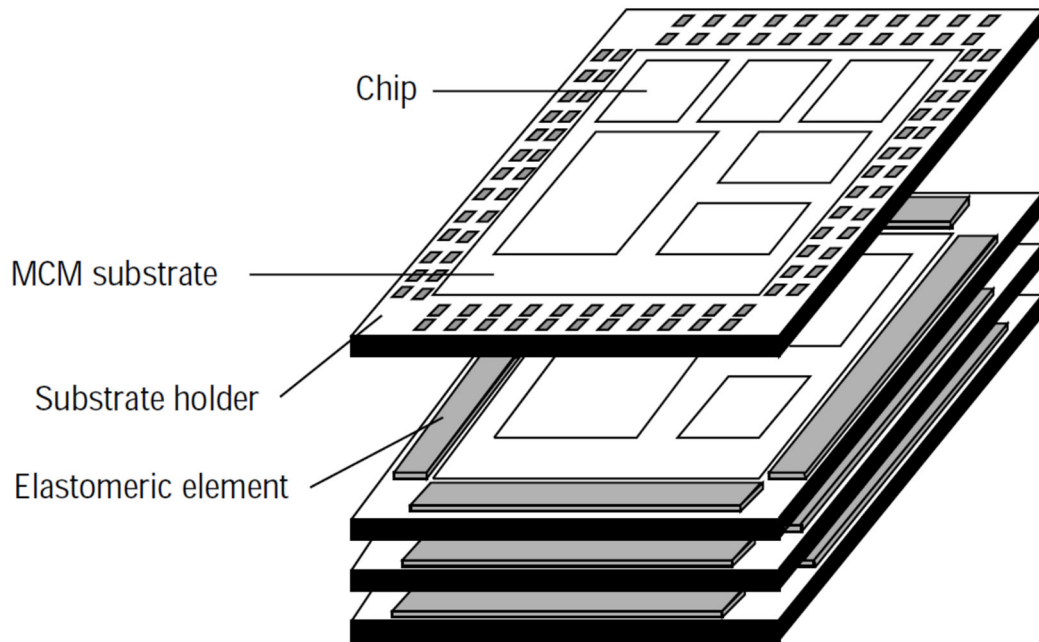


Figure 2. A 3D MCM stack.

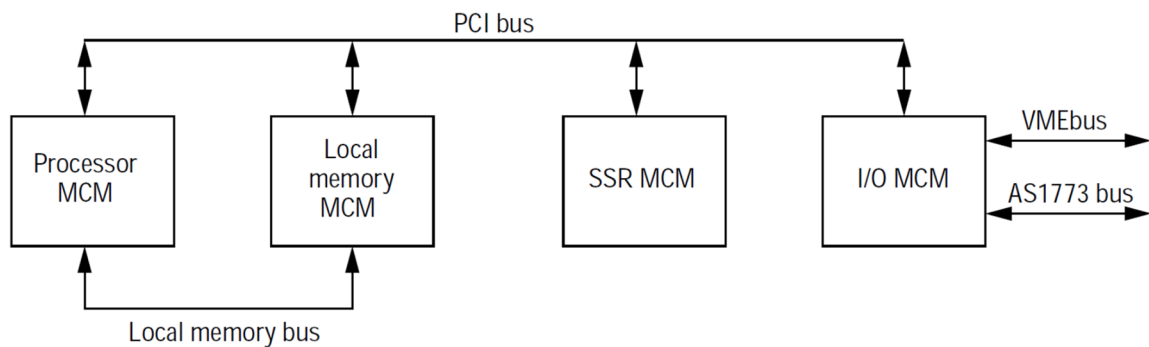


Figure 1. Block diagram of the 3D microavionics stack.

257. As taught by Watanabe, the operational modules (first level assemblies) are mounted and functionally interconnected on a main circuit board, which provides horizontal interconnections between the first level assemblies, as well as additional external connections for receiving electric power signals and the like.

V. Conclusion

In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 31st day of March in Gainesville, Florida.

Respectfully submitted,



ATTACHMENT A

Exhibit	Reference
1001	U.S. Patent No. 7,826,243 (“the ’243 patent”)
1002	File History of the ’243 patent
1005	Certificate of Correction for the ’243 patent
1006	Excerpt of the ’243 patent with Certificate of Correction language
1007	U.S. Patent Publication 2001/0028114 to Hosomi (“Hosomi”)
1009	Certified Translation of WO 2004/072667 (“Sato”)
1010	U.S. Patent Publication 2003/0178228 to Sung et al. (“Sung”)
1011	U.S. Patent 6,791,193 to Watanabe et al. (“Watanabe”)
1012	C. Maxfield, <i>Bebop to the Boolean Boogie</i> (2d. ed. 2003) (“Maxfield”)
1013	G. Blackwell, <i>The Electronic Packaging Handbook</i> (IEEE Press 2000) (“Blackwell”)
1014	K. Gilleo, <i>Area Array Packaging Handbook: Manufacturing and Assembly</i> (McGraw-Hill 2002) (“Gilleo”)
1015	S. Thompson et al., Moore’s law; the future of Si microelectronics, 22 (MaterialsToday, vol. 9, No. 6, June 2006) (“Thompson”)
1016	I. Elfadel, et al., 3D Stacked Chips: From Emerging Processes to Heterogeneous Systems, (Springer Int’l Publishing Switzerland 2016) (“Elfadel”)
1017	K. Sasidhar, <i>Parallel Test Techniques for Multi-chip Modules</i> (Doctoral Thesis, Georgia Institute of Technology, Aug. 1997) (“Sasidhar”)
1018	K. Satish, Tutorial on Design for Testability (DFT): An ASIC Design Philosophy for testability from Chips to Systems, (IEEE 1993) (“Satish”)
1019	J. Huber et al., Successful ASIC Design the First Time Through, 160 (Van Nostrand Reinhold 1991) (“Huber”)
1020	IEEE Standard 1149.1-1990

Exhibit	Reference
1021	www.jtag.com/what-is-jtag-boundary-scan (www.jtag.com)
1022	K. Sasidhar et al., <i>Testing NASA's 3D-Stack MCM Space Flight Computer</i> , (IEEE 1998) ("NASA")
1023	C. Maunder et al., An Introduction to the Boundary Scan Standard: ANSI/IEEE Std 1149.1, 28 (Journal of Electronic Testing 1991) ("Maunder")
1024	Hennessy and Patterson, <i>Computer Architecture: A Quantitative Approach</i> (4th ed. 2006) ("Hennessy and Patterson")
1026	Defendants' Opening Claim Construction Brief, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 33