Tutorial on Design For Testability (DFT)
"An ASIC Design Philosophy for testability from Chips to Systems"

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Abstract -- This is a comprehensive tutorial on DFT with emphasis on concepts of digital Application Specific Integrated Circuit (ASIC) testing incorporating boundary scan architecture in ASIC design. This tutorial covers discussion and features of Institute of Electrical and Electronics Engineers (IEEE) Standard 1149.1, Joint Test Action Group (JTAG) test technique, that can be implemented during design and development of digital ASIC and systems. These test techniques can be applied to test device mounted multi-layer Printed Circuit Board (PCB) and Multi Chip Module (MCM).

Introduction

Testable designs of digital ASIC's and systems are essential to obtain high reliability. Due to the increased complexity of digital ASIC's having very high pin density packages, access to pins for defect isolation and diagnosis of device, mounted on multi-layer PCB or MCM is extremely difficult by conventional bed-of-nails or probes method. Applying test stimulus by other chips to perform comprehensive in-circuit testing of a complex Integrated Circuit (IC) on a PCB or MCM is complex and expensive and also to maintain surrounding IC's not to be damaged by back-driving is difficult. Further, IC's offered by different manufacturers can interact with each other appropriately and predictably during testing of device mounted PCB is also important. The primary interface to apply test stimuli and to observe circuit response of a device mounted on PCB is through edge connector and access to the internal connections will be limited. These test problems were viewed with great concern and to address these, in 1985, several European and American companies joined together and formed a group called JTAG and conceived boundary scan technique. In early 1990 IEEE announced the industry standard 1149.1, "Test Access Port and Boundary Scan Architecture". This standard defines testability features that can be incorporated into digital devices and these features can be used in device testing, incoming inspection, device mounted PCB test, MCM test, system test, field maintenance and repair.

Following topics are discussed in the upcoming paragraphs a) DFT b) fault model used for test generation of digital logic c) boundary scan architecture that can be implemented in ASIC's and d) IEEE Std 1149.1.

What is DFT ?

In the past decade several circuit structures and design techniques have been developed to improve the testability of digital circuits. Most prominent among these have been scan-design, Linear-Feedback Shift Registers (LFSR) and Built-In-Self-Test (BIST) based around Built-In Logic Block Observer (BILBO). These techniques can be used at the chip level to guarantee testability and Automatic Test Pattern Generation (ATPG) tools can be used to generate tests that include stimuli to be applied and the expected response of the fault-free circuit. DFT is a technique aimed at simplifying testing by modifying a design to improve the Controllability, Observability and Predictability (COP) of internal signals of ASIC's and interconnections of devices on a PCB or MCM.

Controllability is defined as the ability to establish a specific signal logic value either low or high at each node in a circuit by setting values on the circuit's inputs. Observability is defined as the ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs. Predictability is the ability to obtain known output values in response to given input stimuli. Most DFT techniques deal with the ways for improving Controllability, Observability, Predictability and design efforts specifically employed to ensure that a device is testable [4].

Scan design is a DFT technique involving specialized flip-flop or latch that allows data to be scanned in for control and to be scanned out for observation and can be activated in scan mode for test purposes. The objective of DFT is to improve the reliability of hardware. Testability involves a design approach aimed at easing the detection of faults on the chip, on the board and in the system. By using DFT strategy in the early design process of ASIC's, one can simplify the test development effort and guarantee a high level of improved quality and system reliability. Testability is a property of a circuit, board, or system that enables non-destructive testing. These days design and test are no longer considered separate issues. DFT is a design characteristic that influences various costs associated with testing and by which, status of a device (normal, inoperable, degraded) can be determined and the isolation of faults within the device or in the system to be performed quickly, to reduce test time and cost. Methods of reducing the complexity of design, for test purposes and to keep the cost of test generation within reasonable bounds is referred to as DFT.

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DFT seeks to qualify the manufacturing of the design. DFT has to be applied at the design stage of an ASIC and is not considered as Test Design, but certainly can help Test Design to reduce test time and with known test structures to ease test generation.

What is Fault model ?

The basic assumptions regarding the nature of physical and logical faults in a combinatorial logic circuit are referred to as fault model. The most widely used fault model for digital logic circuits is that of a single node being permanently stuck at a logic value. This type of fault model is referred to as single stuck-at-fault model. The goal of test generation is to produce a complete fault detection test set (vector), that is, a set of tests that detect any detectable faults. By using stuck-at-fault model for combinatorial logic circuits and with algorithmic ATPG techniques, a high fault coverage test sets can be generated for testing ASIC's at different stages of test development like wafer, packaged device and in PCB or system level.

What is Boundary Scan ?

Boundary scan is a test technique using scan methodology, involving digital devices, designed with shift registers (scan flip flops) placed between each device pin and the internal logic. These shift registers can control and observe signal values present at each input and output pin and are connected together in serial fashion to form a data register chain, called Boundary Scan Registers. Figure 1 shows a generic boundary scan shift register with shift and update stages.

The update stage latch prevents output from rippling as data is shifted through the shift register during scan operation. Figure 2 shows how the boundary scan registers can be connected in an ASIC. Test sets generated by ATPG can be scanned into these boundary scan registers through scan in port such that test stimuli are applied in parallel, circuit response can be captured in parallel by boundary scan registers connected between internal logic and output pins and scanned out through scan out port. Each boundary scan register acts like a bed-of-nail test point.

JTAG IEEE Standard 1149.1

JTAG IEEE Standard 1149.1 defines a boundary scan architecture with Test Access Port (TAP). TAP is a general purpose port comprising 4 or 5 dedicated test signal pins - one test clock, one control, one serial data input pin, one serial data output pin, and one optional reset pin. TAP signal pins control a 16-state, finite state machine that operateS according to the state diagram as shown in figure 3.

The states whose names end with "-DR" will operate on one of the data register (Boundary Scan registers, optional test data registers, Bypass register, device Identification (ID) register), while those states whose names end with "-IR" will operate on Instruction Register. The instruction register is a shift-register based circuit with parallel output latch, which controls the operation of data register or the register to be accessed for a particular test or both (access and operation). In a minimum configuration, every device compliant to JTAG must contain a TAP controller, Boundary Scan registers, Instruction register and Bypass register. Optional registers are a) ID register, b) design specific test data registers. The primary reason for using Boundary Scan registers are to allow for efficient testing of board interconnect and to facilitate isolation and testing of devices by accessing through TAP. Figure 4 shows the architecture of JTAG boundary scan and TAP controller.

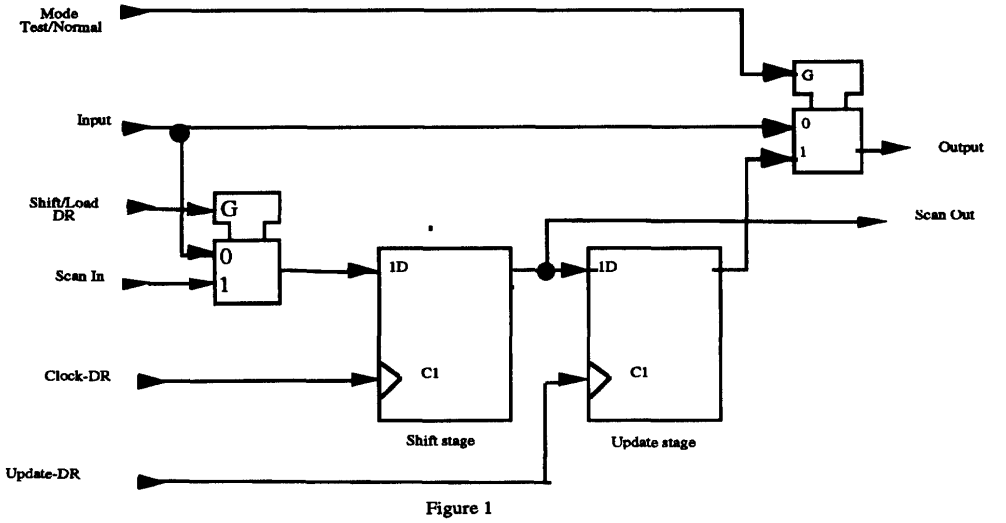


Figure 1

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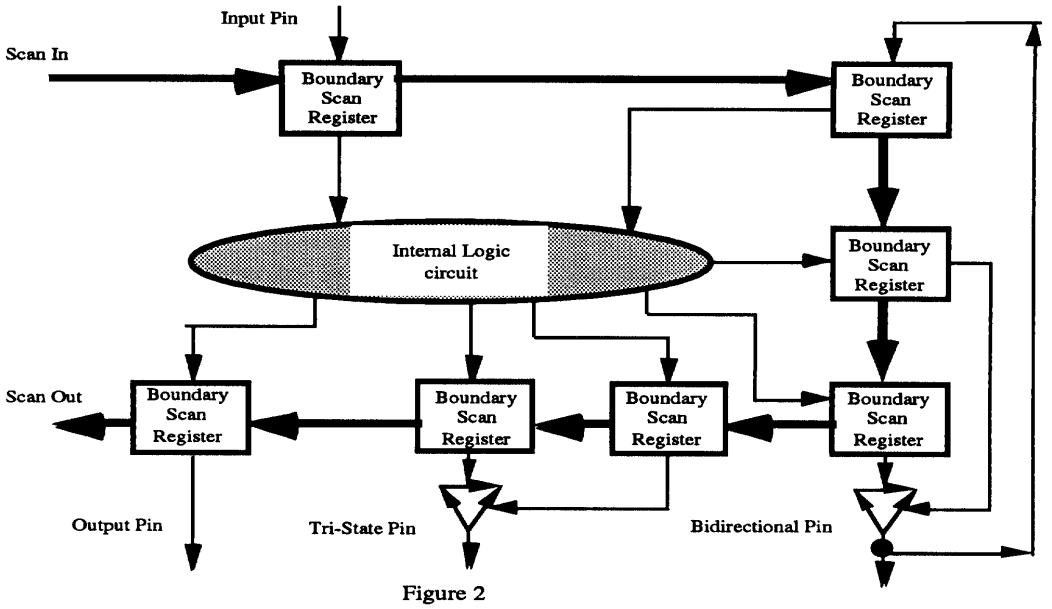


Figure 2

TAP controller signal pins

Test Reset input (TRST)
- Optional pin.
- Asynchronous reset signal.
- Low input signal will set the TAP controller state machine to the Test-Logic-Reset (TLR) state.
- Pull-up resistor assures a high level if unconnected.

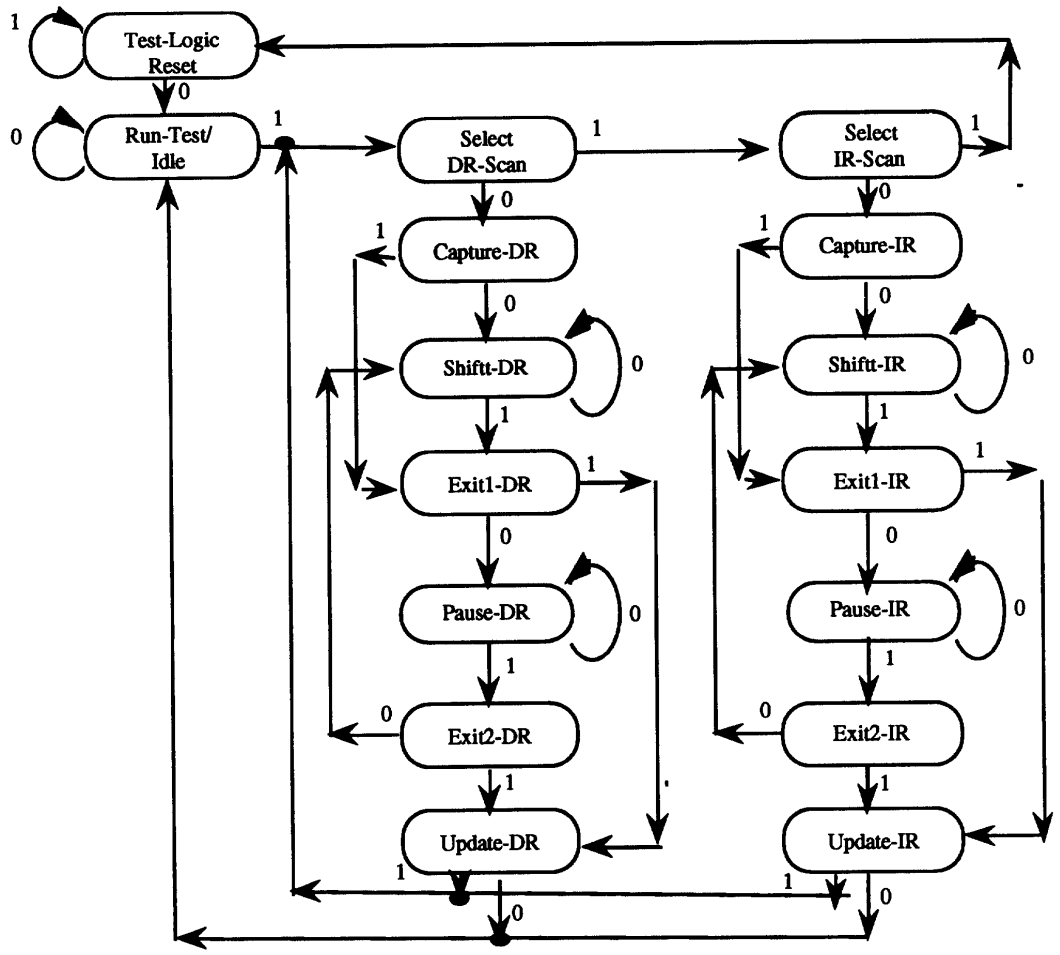
Test clock input (TCK)
- Low->high (0 - 1) transition causes -
  - The TAP controller to change state.
  - In Capture-IR state the shift register contained in the Instruction Register gets loaded with a fixed pattern logic value with two least significant bits assigned values 0 and 1 respectively.
  - In Shift-IR state, signal value at TDI input pin gets shifted into Instruction register shift stage.
  - In Capture-DR state data can be parallel-loaded into Boundary Scan registers or optional test data registers selected by current instruction. If a test data register selected by current instruction does not have a parallel input, or if capturing is not required for the selected test, the register retains its previous state.
- In Shift-DR state signal value at TDI input pin gets shifted into shift stage of data register which in-turn selected by current instruction.
- High->low (1 - 0) transition causes -
  - data from shift stage to load update stage of a) instruction register in Update -IR state or b) data register in Update-DR state.
  - In Shift-IR state, content of instruction register (shift stage) gets shifted out to TDO output pin.
  - In Shift-DR state, content of data register (shift stage) gets shifted out to TDO output pin.
- Independent of the system clock(s).

Test Mode Select input (TMS)
- Determines next state of the state machine based on the value when TCK goes low->high transition.
- According to the TAP state diagram, the state machine is such that, with TMS held high and with 5 or more TCK clocks the state machine resets to TLR state from any state. In TLR state the device operates in normal/system mode and test functions are disabled.
- Pull-up resistor assures a high level if unconnected.

Test Data Input (TDI)
- Input pin by which, data is serially shifted into either a) Instruction Register in Shift-IR state, or b) Data register in Shift-DR state.
- Pull-up resistor assures a high level if unconnected.

Test Data Output (TDO)
- Output pin by which data is serially shifted out of a) Instruction register in Shift-IR state, or b) Data register in Shift-DR state.
- Tri-state output, active only in Shift-DR and Shift-IR states.

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The value shown adjacent to each state transition represents the signal present at TMS at the time of a rising edge of TCK

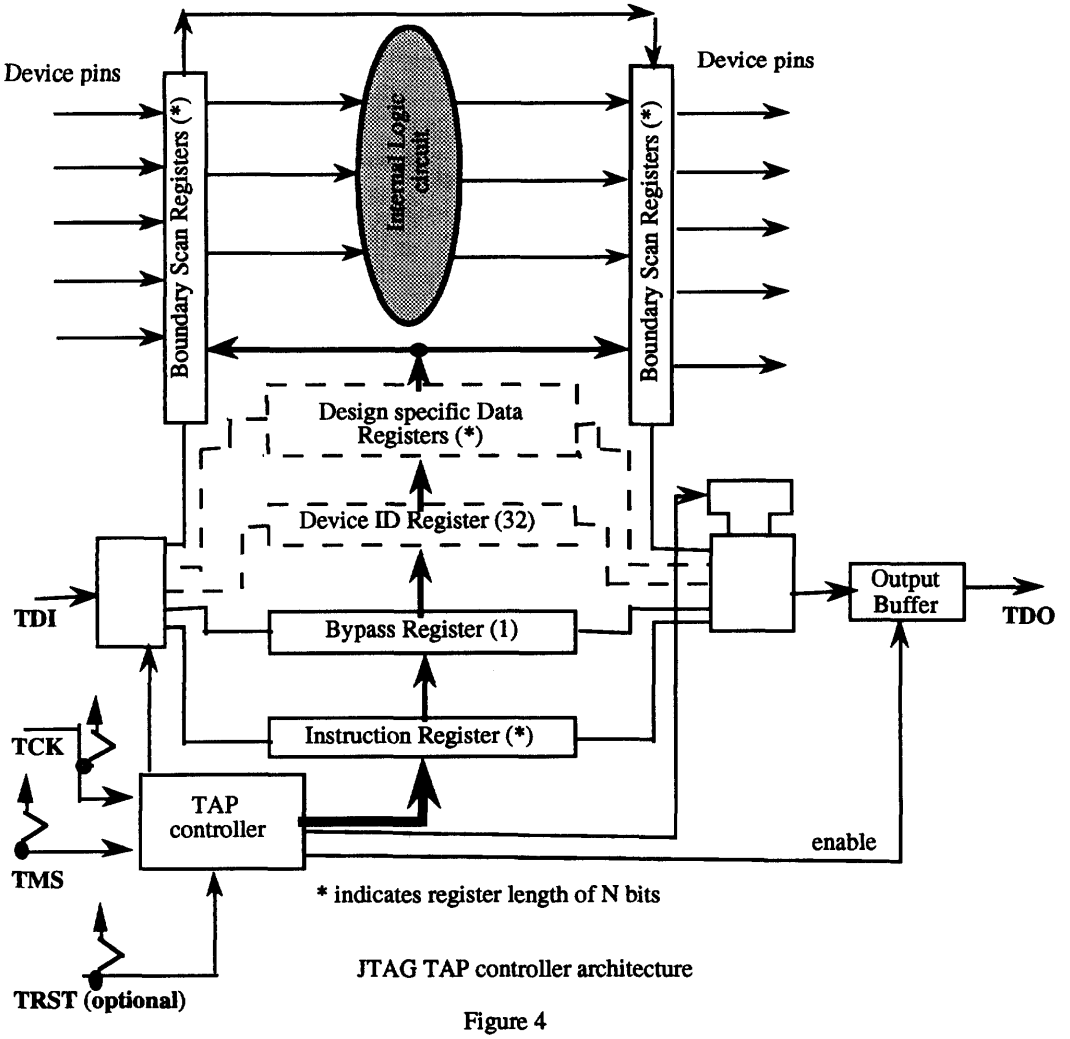
Figure 3

JTAG IEEE Std 1149.1 mandatory registers

Bypass Register
- 1 bit register.
- provides a single bit path through device TDI to TDO :
  - this allows quick access to any device on the PCB JTAG test bus.
  - if a system contains 100 devices on the JTAG test bus, each containing 100 bit long Boundary Scan registers it would take 1,000 TCK clocks to load the Boundary Scan registers of the last device in the PCB JTAG test bus. The Bypass register shortens this to 199 TCK clocks as each device not selected for test will require only one TCK clock to pass data through the Bypass register.
- Loads a 'b0 whenever this Bypass register is captured.

ID Register
- 32 bit long.
- Bit 0 is always 'b1.
- Bits 11-1 = Manufacturer's identification code and is set by Joint Electron Device Engineering Council (JEDEC), publication number JEP106-B.
- Bits 27-12 = Device part number.
- Bits 28-31 = Version number.

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JTAG TAP controller architecture

Figure 4

- Optionally, the ID register may also be designed to capture a different value when the USERCODE instruction is used. This applies only to programmable logic devices.
- If a device is initiated from TLR state to Shift-DR state the first bit shifted out will be 1 (if the device includes a ID register). If no ID register included in a device, Bypass register will be selected between TDI to TDO path and first bit shifted out will be 0.

31 28	27 12	11 1	0
Version 4 bits	Device Part Number 16 bits	Manufacturer's ID code 11 bits	1

Instruction Register (IR)

- At least 2 bits long.
- Each instruction register element comprises a shift register flip-flop and a parallel output latch. Latches hold the current instruction.
- Decodes instructions to determine which data register is connected between TDI and TDO path and controls the operation of data register.
- In TLR state, will be loaded with IDCODE instruction, (if the device contains ID register) or Bypass instruction.
- The two LSB's are loaded with 'b01 in Capture-IR state.
- With N bit IR length 2^N instructions can be decoded and test functions can be easily expanded by simply adding new instructions.

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JTAG IEEE Std 1149.1 mandatory instructions

BYPASS instruction

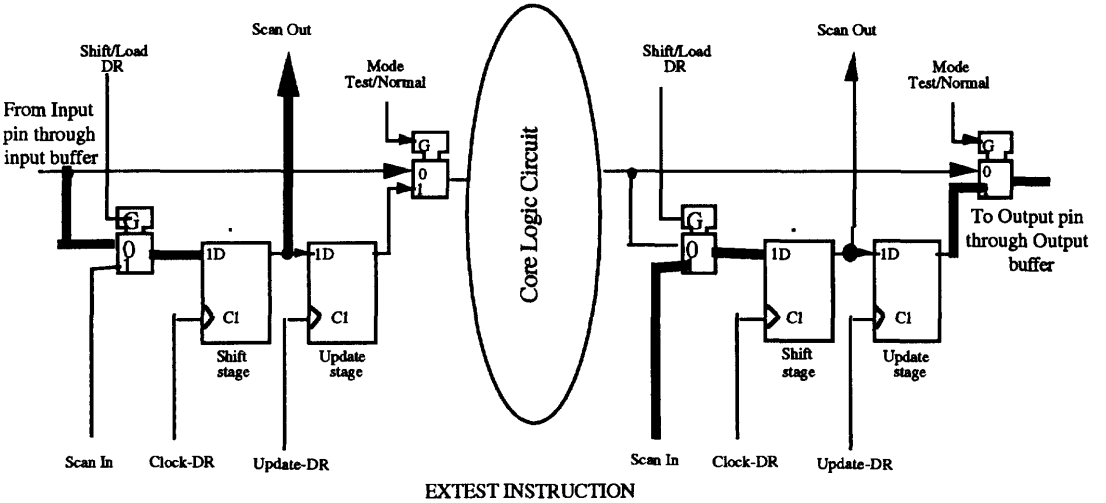
- Bypass register (single shift register) will be connected between TDI and TDO.
- The device will be in normal/system operation mode.
- IEEE standard 1149.1 requires a logic 1 be loaded into every instruction register element.
- Unused instruction codes can be decoded to execute BYPASS function.

EXTEST instruction

- Boundary scan registers will be connected between TDI and TDO.
- IEEE standard 1149.1 requires a logic 0 be loaded into every instruction register element.
- Following are the EXTEST functions
  - to test the connection between boundary register and PCB.
  - to test the interconnection between two boundary scan devices in a PCB.
  - to test non scan devices connected between two boundary scan devices.
- During EXTEST, all I/O pins are connected to the boundary scan registers and the core logic is isolated, data flows from input pin through input buffer to boundary scan register and output data will be driven out from boundary scan register to output pin through output buffer as shown in figure 5.
- Interconnection test can be performed by the following EXTEST sequence :
  - The instruction register in both devices are loaded with EXTEST instruction in Shift-IR state, then the TAP controller is moved to Shift-DR state and test stimuli is shifted into the 1st device boundary scan shift stage. After shifting the test stimuli the TAP controller is moved to Update-DR state and on the falling edge of TCK, the test stimuli in boundary scan shift stage of 1st device are loaded to update stage and will be driven out through the output interconnection pins of the device. The test results can be captured by the 2nd device connected to the 1st device by moving the TAP controller of 2nd device to Capture-DR state. TAP controller causes data to be captured by holding Shift/Load DR signal at 0 (refer to figure 1) and allowing TCK to propagate Clock-DR. Test results can be examined by moving back to Shift-DR controller state of the 2nd device. Figure 6 shows the JTAG compliant devices connected on a PCB JTAG test bus.

SAMPLE/PRELOAD instruction

- Boundary scan registers will be connected between TDI and TDO.
- Following are the SAMPLE/PRELOAD functions
  - A snap-shot of the data flowing through the device's output pins can be taken and this is called SAMPLE function. By shifting SAMPLE/PRELOAD instruction into Instruction register in Shift-IR state and then moving to Capture-DR state, data can be sampled on the rising edge of TCK. The captured data can be shifted out for examination in Shift-DR state.
  - Desired data can be shifted into the boundary scan registers without interfering with the normal flow of signals between input pins and core logic. This allows latched parallel outputs in boundary scan



EXTEST INSTRUCTION

Figure 5

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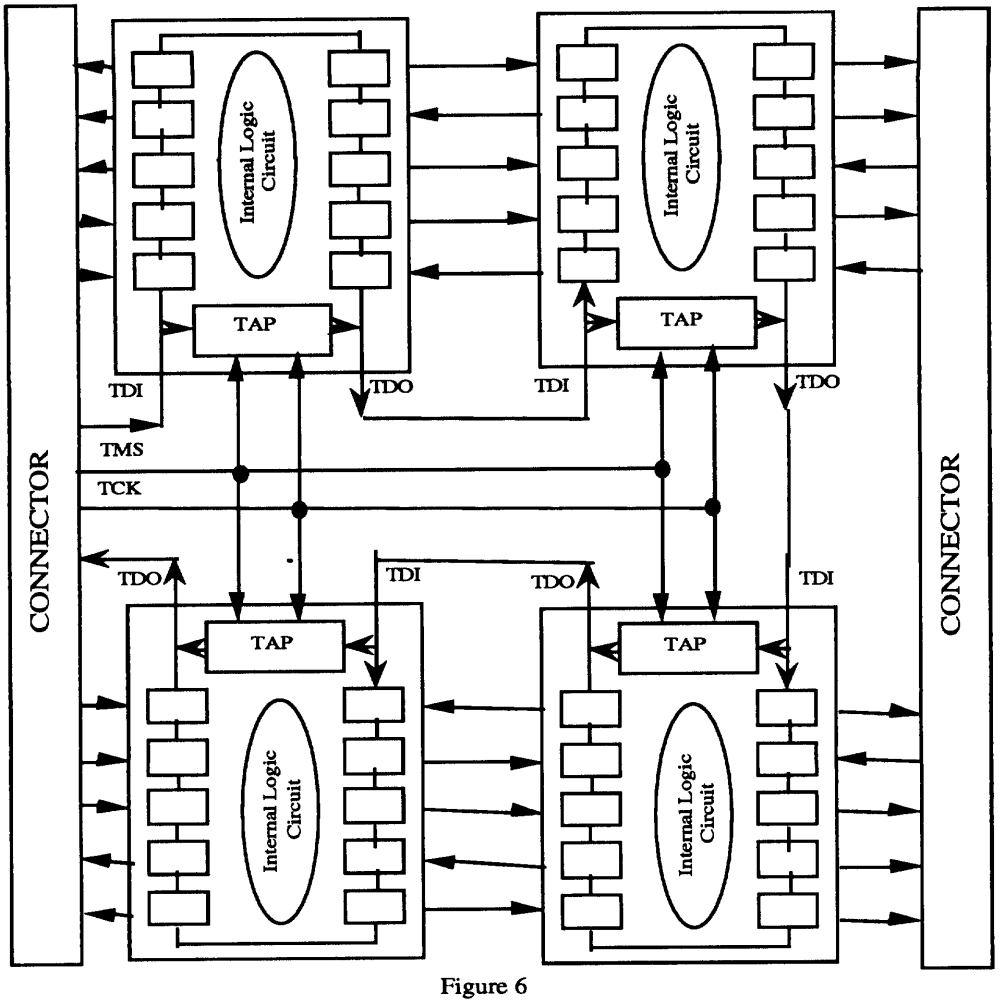


Figure 6

registers to be loaded with data before selecting another instruction that accesses boundary scan registers and this is called PRELOAD function. By shifting SAMPLE/PRELOAD instruction into IR in Shift-IR state and then moving to Shift-DR state, the desired data can be shifted into boundary scan registers and moving to Update-DR state causes latched parallel output stage of boundary scan registers to drive through the output pins.

- By loading suitable data when PRELOAD instruction is selected, it can be ensured that all signals driven out of the device are defined as soon as the EXTEST instruction is selected.

ITAG IEEE Std 1149.1 optional instructions

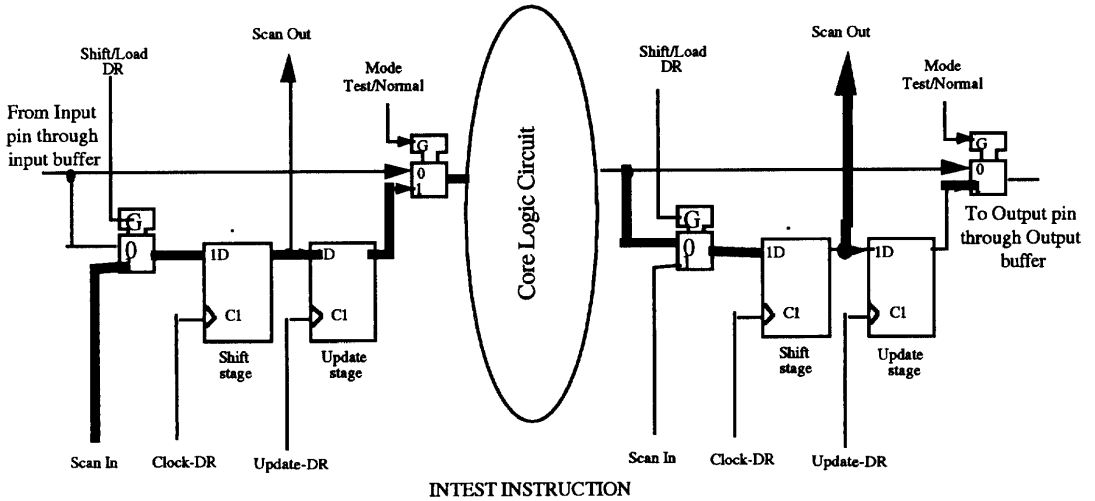
IDCODE Instruction (if ID register present in the device).

- ID register will be connected between TDI and TDO.
- First bit shifted out will be 1
- The pre-defined 32 bit data will be loaded into shift register stage in Capture-DR state and can be shifted out in Shift-DR state.

INTEST Instruction.

- Boundary scan registers will be connected between TDI and TDO.
- This instruction can be used to perform on-chip system logic test. ATPG generated test stimuli can be shifted to the input boundary scan registers in Shift-DR state and

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INTEST INSTRUCTION
Figure 7

is driven by the boundary scan register to the inputs of the on-chip logic following the falling edge of TCK in Update-DR state. The test is applied between Update-DR and Capture-DR states. For stored-state on-chip logic designs, this will require entry into the Run-Test/Idle state where appropriate clock transitions can be applied to the on-chip logic. On the rising edge of TCK in Capture-DR state the results are captured into the output pin boundary scan registers and can be shifted out in Shift-DR state for examination as shown in figure 7.

RUNBIST Instruction.

- Boundary scan registers will be connected between TDI and TDO.
- This instruction allows to run self-test of embedded structured logic built with LFSR's, signature analyzers or BILBO's. The required test stimuli can be shifted into the boundary scan registers and in Run-Test/Idle state self-test is executed and the results can be captured in Capture-DR state and shifted out in Shift-DR state for examination.

Proposed instructions supplement to IEEE Std 1149.1

HIGHZ instruction.

- Bypass register will be connected between TDI and TDO.
- All the output pins of the device (output pins, bi-directional pins and tri-state pins) are inactive.
- This instruction will be helpful for in-circuit PCB test, such that back-driving during in-circuit test can be avoided.

CLAMP instruction.

- Bypass register will be connected between TDI and TDO.
- The signal value driven out of the pins of the device will be the value that has been shifted into the boundary scan registers previously (for example the date shifted with SAMPLE/PRELOAD instruction).
- This instruction will be helpful for in-circuit PCB test.

Device wafer test

- At the wafer level, the device can be tested with limited probes on a probe card by accessing TAP controller pads, power pads, ground pads and system clock pad(s) (if the device has system clock), by using INTEST instruction and sequencing through the TAP state machine.

Package Device test

- At the package level, by using EXTEST instruction and sequencing through the TAP state machine DC parametrics of buffers can be measured by an Automatic Test Equipment (ATE).

Device interconnect test on PCB

- At the board level, interconnect test between JTAG IEEE Std 1149.1 compliant devices can be performed by using SAMPLE/PRELOAD and EXTEST instructions and sequencing through the TAP state machine.
- Figure 8 shows the interconnections of non-boundary scan device connected to boundary scan devices and the device can be tested through the boundary scan devices.

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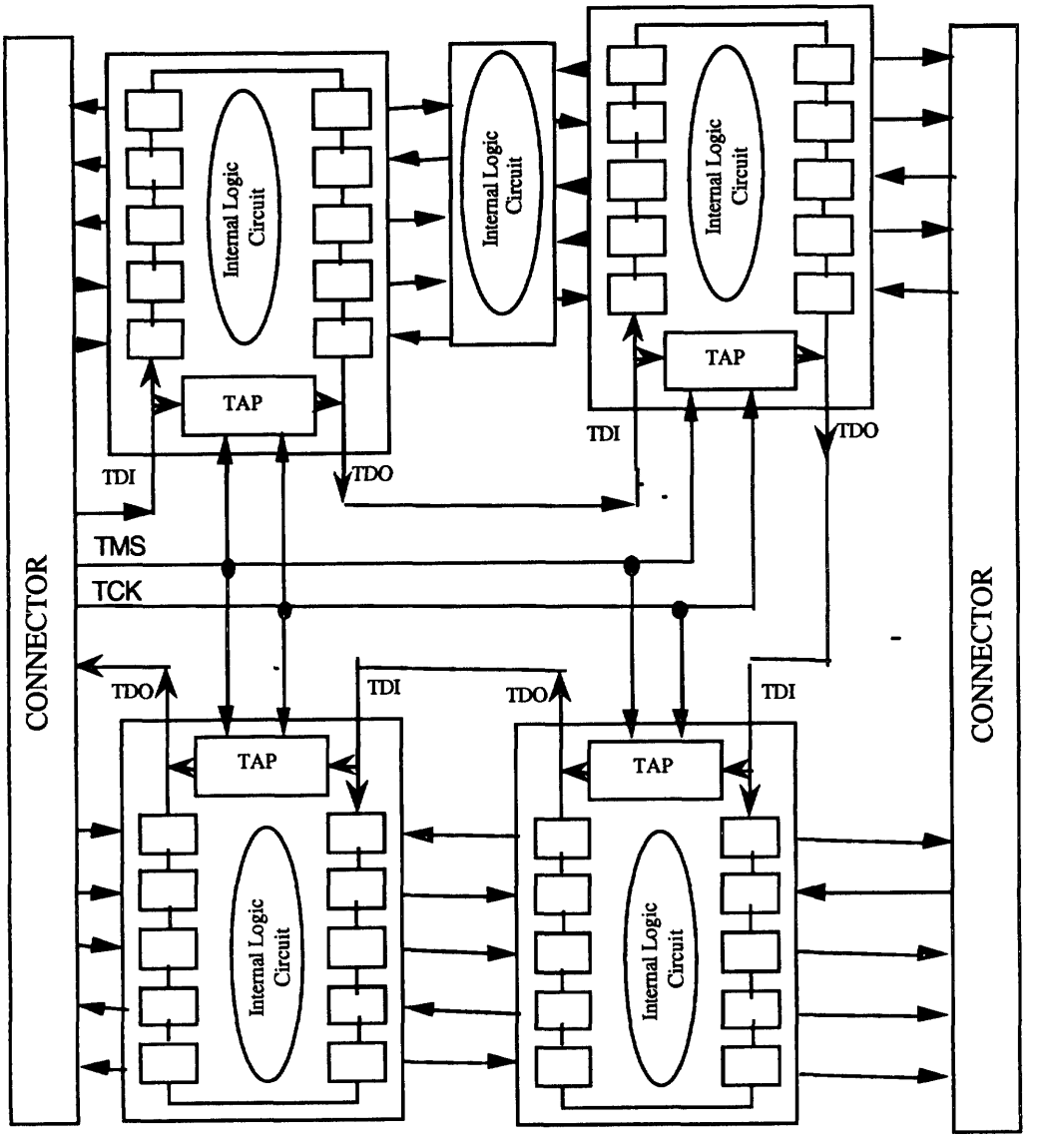


Figure 8

- JTAG test bus on the PCB can be extended to multiple PCBs in a system.

New developments

To describe boundary scan architecture, Boundary Scan Description Language (BSDL) has been proposed. BSDL can help in development of automatic test generation to test devices implemented with IEEE Std 1149.1. For further information please refer "HP Boundary-Scan Tutorial and BSDL Reference Guide", Hewlett Packard [3]

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Conclusion

Considering all the advantages that TAP and boundary scan architecture provides, IEEE Standard 1149.1 should be seriously considered as a test solution. While the capabilities gained are not free, the tradeoffs should be investigated. Advantages include increased Controllability and Observability, test set reuse, better fault detection, isolation of device for in-circuit PCB test, and consistent test methods across multiple test environments. Although IEEE Standard 1149.1 is suitable for all logic design sizes, implementing IEEE Standard 1149.1 is typically easier to justify on larger gate count and high density pin count package designs. Using the capabilities of IEEE Standard 1149.1 TAP and boundary scan will provide advantages that help to reduce the total cost of test generation, test development and system test.

Acknowledgments

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