

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

BiTMICRO LLC,

Plaintiff,

v.

KIOXIA AMERICA, INC.
And KIOXIA CORPORATION,

Defendants.

Case No. 6:22-cv-00331-ADA

BiTMICRO LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 6:22-cv-00335-ADA

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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Defendants KIOXIA America, Inc. and KIOXIA Corporation (together, “KIOXIA”) and Intel Corporation (“Intel”) (collectively, “Defendants”) hereby submit their Opening Claim Construction Brief for the disputed terms of U.S. Patent Nos. 6,496,939 (“the ’939 patent”), 8,010,740 (“the ’740 patent”), and 9,135,190 (“the ’190 patent”). Intel further submits its Opening Claim Construction Brief for the disputed terms of U.S. Patent Nos. 7,826,243 (“the ’243 patent”), 9,858,084 (“the ’084 patent”), and 10,120,694 (“the ’694 patent”).¹

I. LEGAL STANDARD

Claim terms are given their customary meaning as understood by a person of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005). To determine that meaning within the field of art, a court should look to “the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Id.* at 1314. A claim is invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2 when, read in light of the specification and the prosecution history, it “fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

II. ’939 PATENT

A. Technical Background

The ’939 patent relates to systems and methods for controlling data in a computer system when the computer system loses power. ’939 patent at 1:8-11. As the ’939 patent explains, computer systems typically comprise two types of memory: (1) volatile “cache” memory, which is erased when external power is shut down, and (2) non-volatile memory, which preserves data when external power is removed. *Id.* at 1:15-33. Since volatile cache memory is much faster than

¹ The ’243 patent, the ’084 patent, and the ’694 patent are not asserted against KIOXIA.

non-volatile memory, data is typically written to cache memory before being transferred to non-volatile memory. *Id.* However, when the computer system loses external power, there is insufficient time to transfer all newly written data from the volatile cache memory to the non-volatile memory, thereby creating a risk that data will be lost. *Id.* at 1:34-39. Accordingly, the '939 patent identifies an alleged need to ensure that all newly written data to the volatile memory is safely transferred to non-volatile memory when external power is lost. *Id.* at 2:13-16.

The '939 patent purports to address this need by disclosing the use of “super-capacitors”—which operate as a “short term power source”—to provide sufficient energy to allow data to be transferred from volatile memory to non-volatile memory before the computer system shuts down. *Id.* at 2:27-31; 3:3-5. To accomplish this function, the '939 patent explains that, upon loss of external power, the super capacitors are “activated” to maintain the internal power of the system. *Id.* at 5:8-11. Using this power supply, data is then transferred from the volatile memory to the non-volatile memory to ensure that it is preserved. *Id.* at 5:33-36. Once the super capacitors have discharged to a predetermined level—a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged—power is cut off from the super capacitors to the computer system. *Id.* at 5:39-43; 5:48-52; 6:49-53.

B. “predetermined level”

Patent	Plaintiff's Proposal	Defendants' Proposal
'939 patent: Claims 1, 10	Plain and ordinary meaning; not indefinite.	“a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged”

“[T]he specification is always highly relevant to the claim construction analysis.” *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). “Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Phillips*, 415 F.3d at 1315; *id.* at 1316

(“[T]he specification necessarily informs the proper construction of the claims.”); *Merck & Co. v. Teva Pharms. USA, Inc.*, 347 F.3d 1367, 1371 (Fed. Cir. 2003) (“[C]laims must be construed so as to be consistent with the specification, of which they are a part.”) (citations omitted). Here, Defendants’ proposed construction should be adopted because the specification makes clear that the “predetermined level” is “a preset minimum operating voltage that is necessary for proper operation, in which the super capacitors are not fully discharged.”

In particular, the specification explains that the “predetermined level” is a preset minimum operating voltage at which “the down-converter has *insufficient voltage differential to continue proper operation* and shuts down.” ’939 patent at 5:39-43 (emphasis added); *see also id.* at 6:40-44; 5:44-48 (explaining that voltage cannot be allowed to fall below “minimum operating voltage”); 5:48-52; 6:49-53 (explaining that super capacitors should not be “fully discharged”). The specification also demonstrates why these parameters are critically important, explaining that if the voltage “were allowed to *fall below the minimum operating voltage* of the computer system, the computer system could continue to run with *unpredictable and potentially serious results.*” *Id.* at 5:44-48 (emphases added); 6:45-49. This would seriously undermine the ’939 patent’s stated goals of ensuring that “a user is able to correctly store large amounts of newly written and modified data” and “rapidly and irretrievably erase data.” *Id.* at 2:33-41. Further, “by not fully discharging the super-capacitors they will take only a few seconds to recharge once the external system power is restored.” *Id.* at 5:48-52; 6:49-53.

The applicant also relied on these specific characteristics to distinguish the alleged invention during prosecution. As the applicant explained, “performance and reliability of the computer system are improved” by ensuring that the predetermined level is “set above the minimum operative voltage of the computer system, preventing the computer system from running

with unpredictable results.” *See* Ta Decl.,² Ex. I at 7 (amend. filed on May 8, 2002). The applicant further explained that, by setting the predetermined level “above a zero level of power for the computing system . . . it may take only a few seconds to recharge the super capacitors, rather than several minutes, rapidly providing protection against power loss.” *Id.* The applicant also distinguished the prior art based on these characteristics, emphasizing that “[a]ny combination of [the prior art] . . . would not deactivate super capacitors when the super capacitors are discharged to a predetermined level to cut off power to the computer system.” *Id.* at 8-9.

BiTMICRO’s argument that this term should be afforded a generic “plain and ordinary meaning” is incorrect. *Eon Corp. IP Holdings v. Silver Spring Networks, Inc.*, 815 F.3d 1314, 1321 (Fed. Cir. 2016) (“The question is not whether there is a settled ordinary meaning of the terms in some abstract sense of the words” since “[t]he only meaning that matters in claim construction is the meaning in the context of the patent.”). As explained above, the intrinsic evidence not only confirms that the patentee acted as its own lexicographer in giving this term a specific meaning, but also that the patentee relied on this specific meaning as the critical feature that differentiated the alleged invention from the prior art. As a result, the description of “predetermined level” in the intrinsic record, which is reflected in Defendants’ proposed construction, should be applied. *See, e.g., Kyocera Senco Indus. Tools Inc. v. Int’l Trade Comm’n*, 22 F.4th 1369, 1378 (Fed. Cir. 2022) (finding that the patentee acted as its own lexicographer in clearly defining a term); *Renishaw PLC v. Marposs Societa per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998) (“The construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.”).³

² All references to “Ta Decl.” are to the Declaration of Janice L. Ta in Support of this Brief.

³ BiTMICRO’s proposal also states that this term is “not indefinite.” Because Defendants do not contend that “predetermined level” is indefinite, Defendants do not address this assertion.

C. “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level”

Patent	Plaintiff’s Proposal	Defendants’ Proposal
’939 patent: Claim 10	Function: deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. Structure: Col. 3:3-12, 3:28-4:8, 4:20-35, 4:46-52, 4:64-5:5, 5:35-42, 6:37-44, Figs. 1, 3, 5, of the ’939 Patent, and equivalents thereof.	Indefinite under 35 U.S.C. § 112(6): Lacks corresponding structure.

A means plus function claim element “limits the scope of the functional term ‘to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof.’” *Dig. Retail Apps, Inc., v. H-E-B, LP*, No. 6-19-CV-00167-ADA, 2020 WL 376664, at *3 (W.D. Tex. Jan. 23, 2020) (citing *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347 (Fed. Cir. 2015)). Critically, however, “[a] ‘structure disclosed in the specification is ‘corresponding’ structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.”” *Id.* (citing *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001)). “The focus of the ‘corresponding structure’ inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is ‘clearly linked or associated with the [recited] function.”” *Id.* (citing *Medtronic*, 248 F.3d at 1311). In this case, the specification does not clearly link any structure to the recited function of “deactivating a plurality of super-capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to predetermined level.” As a result, this claim term is indefinite.

As an initial matter, all instances of “deactivating” described in the specification use generic functional language that simply states a result—*i.e.*, “deactivation” of a component—rather than describing a structure that achieves the result. *Id.* at 5:19-22 (stating that an up-converter “is deactivated”); 6:22-25 (same); Figs. 3 and 5 (same); 5:52-57 (stating that a down-converter “is deactivated”). On that basis alone, the specification fails to identify a sufficiently definite structure. *See Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1365 (Fed. Cir. 2012) (affirming indefiniteness where the “specification merely provides functional language” to describe a means plus function term); *Arendi S.A.R.L. v. LG Elecs., Inc.*, No. 12-1595-LPS, 2019 WL 3891150, at *14 (D. Del. Aug. 19, 2019) (holding that a means plus function term was indefinite where the “specification describes the ‘operation’ in terms of a functional result” and not an actual structure); *Pi-Net Int’l Inc. v. JPMorgan Chase & Co.*, No. 12-282-SLR, 2014 WL 1997039, at *9 (D. Del. May 14, 2014) (finding term indefinite where the specification “describes the [term] in functional language . . . [but] is devoid of any disclosure regarding **how** the [term] performs these various functions”).

More importantly, however, the specification does not disclose a structure that deactivates a plurality of super capacitors to cut off power to a computing engine. As explained above, the specification uses functional language to discuss “deactivation” of an up-converter and a down-converter. But annotated Figure 1, shown at right, establishes that the **up-converter** and **down-**

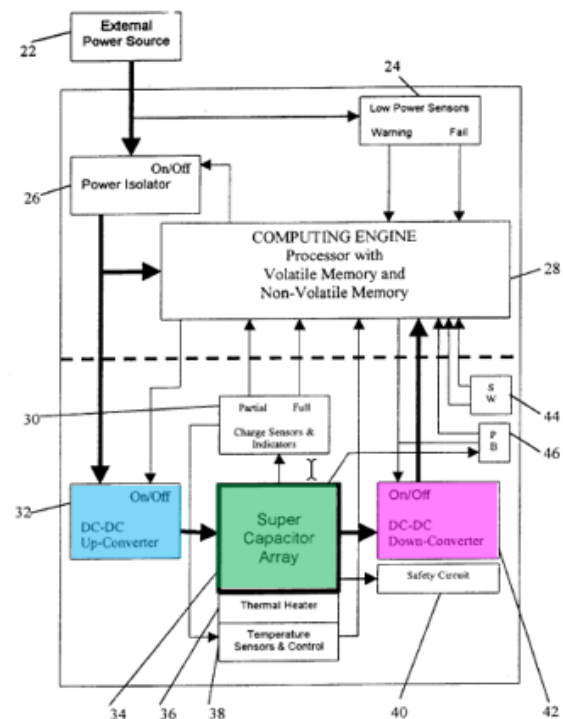


Figure 1

converter are separate and distinct from the **super capacitor array**. '939 patent, Fig. 1. Accordingly, the specification's discussion of deactivating an up-converter and down-converter does not identify a specific structure for deactivating a plurality of *super capacitors* as recited in the claim.

The specification also does not contain any link between the deactivation of the up-converter or down-converter and the deactivation of the super capacitors. For example, the specification states that an up-converter is deactivated when external power has fallen below a specific level. *Id.* at 5:19-22; 6:22-25; Figs. 3 and 5. Because the up-converter is simply a component that “up converts” external power to the voltage necessary to charge the super capacitors, however, it cannot itself deactivate the super capacitors and deactivation of up-converter will not cause deactivation of the super capacitors.⁴ *Id.* at 3:39-41. The only other mention of “deactivation” in the specification is a single sentence indicating that a “down-converter” can be deactivated once “the external power system is risen back to normal levels.” *Id.* at 5:52-57. However, this passage says nothing about deactivating the super capacitors themselves, much less doing so once the super capacitors have discharged to a predetermined level. To the contrary, this passage indicates that the down-converter is deactivated once the external power has turned back on—not when “the plurality of super capacitors discharge[] to a predetermined level” as required by the claim. Similarly, while other passages mention that that the down-converter may shut down when it has insufficient voltage differential, these passages are utterly silent regarding “deactivation” of the super capacitors. *See id.* at 5:39-43; 6:40-44. There is no

⁴ Notably, Figure 3 shows that the super capacitors only supply power *after the up-converter is deactivated*, establishing that deactivation of the up-converter does not—and cannot—deactivate the super-supercapacitors. *See* '939 patent, Fig. 3 (demonstrating that up-converter is deactivated in step 100, after which current is discharged from the super capacitors in steps 104-110).

indication at all that the down-converter's shutdown renders the super capacitors inactive. The claim recites something very specific—deactivating the super capacitors—and the patent does not describe whether or how super-capacitor deactivation occurs. At most, the patent states that the down converter shuts down. These passages fail to “clearly link” any structure to the recited function of “deactivating the plurality of super capacitors” as required for a means plus function element. *See Dig. Retail*, 2020 WL 376664, at *3.

Accordingly, because the specification of the '939 patent “does not contain an adequate disclosure of the structure that corresponds to the claimed function,” the patent “fail[s] to particularly point out and distinctly claim the invention as required by the second paragraph of section 112, which renders the claim invalid for indefiniteness.” *Id.*, at *7 (citing *In re Donaldson Co.*, 16 F. 3d 1189, 1195 (Fed. Cir. 1994)); *Ergo Licensing*, 673 F.3d at 1363 (“If an applicant does not disclose structure for a means-plus-function term, the claim is indefinite.”).

While BiTMICRO acknowledges that this is a means plus function term, BiTMICRO fails to identify a specific structure for performing the claimed function. Rather, BiTMICRO cites a laundry list of figures and paragraphs from the specification and contends that the allegedly corresponding structure is present *somewhere* in that collection. Such an “absurdly overinclusive designation fails to identify a sufficiently definite structure that corresponds to the claimed function.” *Bell N. Research, LLC v. Coolpad Techs., Inc.*, No. 18-CV-1783-CAB-BLM, 2019 WL 3766688, at *6 (S.D. Cal. Aug. 9, 2019). BiTMICRO would instead have Defendants and the Court speculate as to the allegedly corresponding structure by “scour[ing] the Plaintiff's submission to locate, or otherwise ascertain from the blanket proffer made by Plaintiff what structure . . . is disclosed to provide the function.” *Id.* This is improper.

BiTMICRO’s inability to identify a specific structure simply affirms that no such structure is disclosed. *See id.* (finding means plus function claim indefinite based, in part, on plaintiff’s failure to identify a specific structure). This is further confirmed by the portions of the specification cited by BiTMICRO, the majority of which make no mention of “deactivating” anything, much less a super capacitor. ’939 patent at 3:3-12, 3:28-4:8, 4:20-35, 4:46-52, 4:64-5:5, 5:35-42, 6:37-44. The remainder of BiTMICRO’s citations discuss deactivation of *different* components—such as an up-converter and down-converter—not a super capacitor, *as required by the claims*. *See, e.g., id.* at Figs. 3 and 5. As such, BiTMICRO’s inadequate and imprecise proposal underscores the indefiniteness of this claim element.

D. “reversing the flow of current between the computing engine and the plurality of super capacitors”

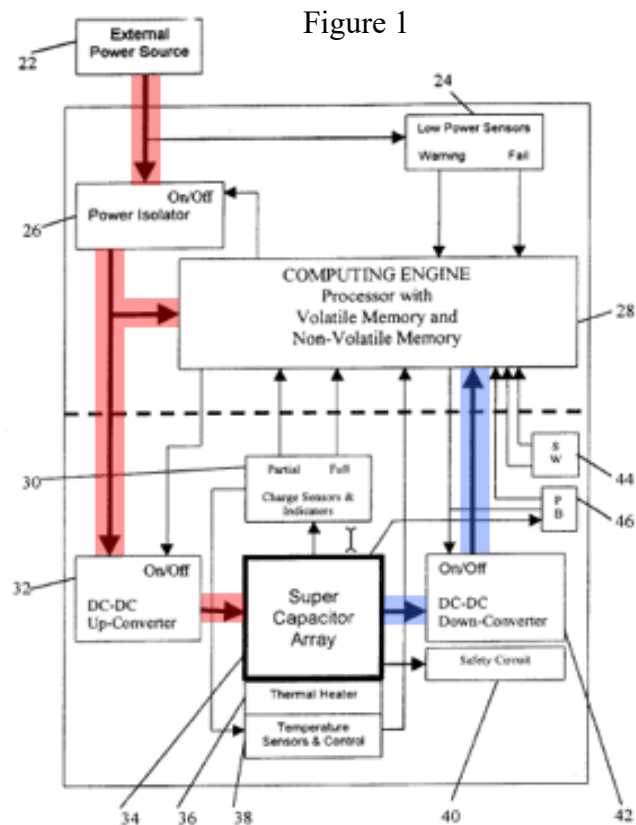
Patent	Plaintiff’s Proposal	Defendants’ Proposal
’939 patent: Claim 6	Plain and ordinary meaning; not indefinite.	Indefinite.

A claim element that is inconsistent with the description of the alleged invention in the specification is indefinite under 35 U.S.C. § 112(2). *See Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002) (finding that a claim requiring a plane to be “perpendicular” to another plane was indefinite where the recited orientation was inconsistent with the orientation disclosed in the specification); *see also In re Cohn*, 438 F.2d 989, 993 (C.C.P.A. 1971) (finding claims indefinite where “the description, definitions and examples appearing in appellant’s specification” were “inherently inconsistent” with the claims); *Ex Parte Gittleman*, 2008 WL 696137, at *4 (B.P.A.I. 2008) (“A claim also runs afoul of § 112, ¶ 2 when it is inherently inconsistent with what is described in the specification.”). In this case, the plain language of the claim requires a two-way flow of current between the computing engine (processor and memories)

and super capacitors such that current can be “reversed.” But the specification of the ’939 patent establishes that current only flows in one direction between the external power source, the super capacitors, and the computing engine. As a result, the requirement that current flow be “reversed” between the computing engine and the super capacitors upon activation of the super capacitors is both non-sensical and inconsistent with the specification, rendering this term indefinite.

As the specification explains, power is supplied to the computing engine from an external power source (“EPS”), in only one direction, during normal operation. ’939 patent at 3:32-35. The EPS also supplies current to charge the super capacitors in the same, singular direction. *Id.* at

3:39-41. Once external power has been lost, the super capacitors are activated to supply current to the computing engine. In that event, however, the flow of current between the super capacitors and the computing engine is still maintained in the same, singular direction. This is demonstrated in annotated Figure 1 at right, which illustrates (1) the unidirectional flow of current from the external power source to both the computing engine and super capacitors (highlighted in red), and (2) the unidirectional flow of current from the super capacitors to the



computing engine upon activation (highlighted in blue). The specification’s references to reversing current flow do not teach otherwise. In one passage, current flow reverses “between the

computer system and the super-capacitors.” *Id.* at 5:24-26 (emphasis added). Computer system 20 (represented by the whole of Figure 1) differs from and is much broader than the computing engine (processor and memories) recited in the claim. A second passage describes current flow that reverses “between the volatile memory and the super-capacitors.” *Id.* at 6:27-28. This statement is clearly an error: the patent nowhere suggests, let alone discloses, a current flow from the volatile memory within the computing engine to the super capacitors.

As annotated Figure 1 and its corresponding disclosure further confirm, current does not flow in two directions between the computing engine and the super capacitors. It only flows in one direction—it is not “reversed” upon activation of the super capacitors. In order for current reversal to occur, current from the external power source would need to flow *from the computing engine to the super capacitors* during normal operation, which is the exact opposite of the current flow that is illustrated and described in the specification. *See, e.g., id.*, Fig. 1 (demonstrating that current flows directly from the external power source to the super capacitors); 3:32-41 (same). Accordingly, because the claim’s requirement that current be reversed is inconsistent with the description in the specification, this term is indefinite. *Allen Eng’g*, 299 F.3d at 1349; *In re Cohn*, 438 F.2d at 993; *Ex Parte Gittleman*, 2008 WL 696137 at *4.

E. “means for reversing the flow of current between the computing engine and the plurality of super-capacitors”

Patent	Plaintiff’s Proposal	Defendants’ Proposal
’939 patent: Claim 15	Function: reversing the flow of current between the computing engine and the plurality of super capacitors. Structure: Col. 3:3-12, 3:28-4:8, 4:20-35, 4:64-5:5, 5:18-26, 6:22-28, Figs. 1, 3, 5, of the ’939 Patent, and equivalents thereof.	Indefinite under 35 U.S.C. § 112(6): Lacks corresponding structure.

As explained above, the specification does not teach “reversing” the flow of current

between the computing engine and super capacitors upon activation of the super capacitors. On that basis alone, this claim term is indefinite for failing to disclose the recited function. However, the specification also does not disclose a structure for performing the recited function. As Figure 1 makes clear, there is no structure that “reverses” current flow between the super capacitors and computing engine such that current flows in the opposite direction when the super capacitors are activated. *See* Section II.D, *supra*. As such, this claim element is indefinite for failure to disclose sufficient corresponding structure. *Dig. Retail*, 2020 WL 376664, at *7 (citing *In re Donaldson*, 16 F.3d at 1195); *Ergo Licensing*, 673 F.3d at 1363.

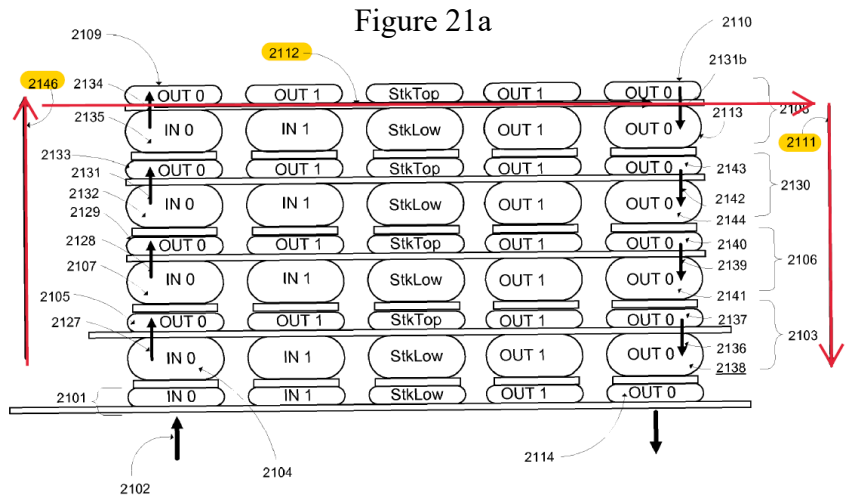
As with the other means plus function terms, BiTMICRO fails to identify a specific structure that allegedly corresponds to the recited “reversing” function, instead citing the same laundry list of figures and paragraphs from the specification that it cites for the other means plus function elements. This is both improper and confirms the lack of corresponding structure as discussed above. *See* Section II.C, *supra*; *Bell N.*, 2019 WL 3766688, at *6.

III. '243 PATENT

A. Technical Background

The '243 patent purports to “support miniaturization and memory scalability” by stacking and interconnecting multiple memory modules to form packages. *Id.* at 1:7-12, 32-42. Through this stacking technique, the patent states, “large capacity storage devices are implemented in a small package device, and larger form factors achieve bigger memory capacities.” *Id.* at 1:54-57.

The '243 patent describes several memory module stacking embodiments. Relevant here is the embodiment of Figures 21a-b, the sole embodiment that includes the “serial chain” and “control circuit” components recited by asserted claims 1, 2, 11, and 12. Figure 21a shows a first serial chain route 2146 that is connected to a second serial chain route 2111 via routing path 2112. *Id.* at 9:67 (as modified by Certificate of Correction), Fig. 21a (annotated at right). A control circuit in each memory



module determines how signals are routed between modules. *Id.* at 10:8-35, Fig. 21b. The patent states that “[s]ince the modules are identical,” a signal can be routed through “all modules in the stack” to the output of the main board for external access. *Id.* at 9:61-64, 10:5-8.

B. “passive port”

Patent	Plaintiff’s Proposal	Intel’s Proposal
'243 patent: Claims 1, 2	“connection between a passive ball and a passive pad”	“connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module.”

During prosecution, and in response to a rejection under 35 U.S.C. § 112, the applicants for the '243 patent amended their specification to add an express definition of “passive port”: “The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module . . . is named ‘passive port.’” '243 patent at 9:8 (as modified by Certificate of Correction); Ta Decl., Ex. F at 3, 22-23. This is an unambiguous definition of “passive port.” See *BookIT Oy v. Bank of Am. Corp.*, 817 F. App'x 990, 994 (Fed. Cir. 2020) (holding, where specification stated that “the mediator *is* a network based service,” that

“[t]here can be no clearer definition[]” of the disputed claim term) (emphasis added); *Sinorgchem Co., Shandong v. Int’l Trade Comm’n*, 511 F.3d 1132, 1136-37 (Fed. Cir. 2007) (observing that “the word ‘is,’ . . . used here in the specification, may signify that a patentee is serving as its own lexicographer”) (quotation omitted). This statement also operates as a clear and unambiguous disavowal of claim scope, given that the applicants chose to add it to the specification to overcome a rejection. *E.g., Tech. Properties Ltd. LLC v. Huawei Techs. Co.*, 849 F.3d 1349, 1358 (Fed. Cir. 2017) (holding that “statements made to overcome [the rejection]” during prosecution operated to disclaim claim scope, where they “were clear and unmistakable”).

To the extent there was ambiguity about the definitional nature of applicants’ statement, they *told the Patent Office expressly* that they were acting as “their own lexicographers”:

Applicants may be their own lexicographers. MPEP 2173.01. The Specification at p. 21, line 7 through p. 22, line 4, as amended in the “Amendments to the Specification” section above, recites in part:

. . . A **connection** between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named “passive port”, such as passive ports 1909 illustrated in Figure 19. (Emphasis added).

. . . ***Thus, “a connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module” is a “passive port”.***

Ta Decl., Ex. F at 23 (emphases added). Applicants also acknowledged to the Patent Office that this definition was consistent with the specification, which “shows [in Fig. 19] that a passive port 1909 **connects** ‘a passive ball’, such as passive ball X2, ‘on one surface of a SDRAM module’, . . . and a passive pad[], such as passive pad X3, ‘on another surface of the same SDRAM module.’” *Id.*

There is no more straightforward example of a “clearly express[ed] . . . intent to define the term”: not only did applicants use the word “lexicographers,” they pointed specifically to the

MPEP section discussing lexicography. *See GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014). The Federal Circuit has recognized that “[w]hen the patentee acts as its own lexicographer, that definition governs.” *Cont’l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 796 (Fed. Cir. 2019); *see also Kyocera*, 22 F.4th at 1378 (“Because the patentee clearly defined ‘driven position’ within the written description, that definition controls.”); *Biogen MA Inc. v. EMD Serono, Inc.*, 976 F.3d 1326, 1335-36 (Fed. Cir. 2020) (noting that patentee’s “argument fails to give effect to [the] explicit definition of ‘polypeptide’ in the specification. We must respect this lexicographic choice.”). This Court has also recognized that a patentee’s definition controls. *See Portus Singapore Pte. Ltd. v. Ecobee, Inc.*, No. 6:20-cv-00694-ADA, ECF No. 36, slip op. at 8-10 (W.D. Tex. Jul. 23, 2021) (holding that “the intrinsic record demonstrates the Patents provide a specific definition of the term [extranet],” where the specification stated that “[a]n extranet *is* a private network” with specific characteristics). And, by applicants’ own admission, their definition here is consistent with the specification. That definition should control.

C. “a plurality of modules each comprising”

Patent	Plaintiff’s Proposal	Intel’s Proposal
’243 patent: claim 1	Part of the preamble and not a limitation of the claim.	“each module in the stacked module comprises”

The disputed term “a plurality of modules each comprising” is part of the claim body, not the preamble. The preamble of claim 1 recites “[a] stacked module comprising.” The “plurality of modules each comprising” follows this preamble language and is thus a limitation. *See Nichia Corp. v. Document Sec. Sys., Inc.*, 2022 WL 1218036, *4 (Fed. Cir. Apr. 26, 2022) (where claim recited “[a] display comprising a plurality of plastic leaded chip carrier LEDs, the plastic leaded chip carrier LEDs each comprising:”, the preamble included only “[a] display comprising”).

As this term is part of the claim body, not the preamble, Intel's construction is consistent with the plain language—"each" means "each"—and the specification, which repeatedly describes a stacked module that includes multiple *identical* modules. For example, each of Figures 19 (shown at right), 20b, 21a, and 21b depicts a stacked module made up of identical modules with the same configuration. '243 patent at 9:6-

8 ("*All SDRAM modules are identical*, and in the example shown in FIG. 19 include the connections as follows: X1 ball is connected to X1 pad, X2 ball to X2 pad, and so on.") (as modified by Certificate of Correction); *id.* at 3:29-33 ("FIG. 20a shows . . . a rotational stacking orientation

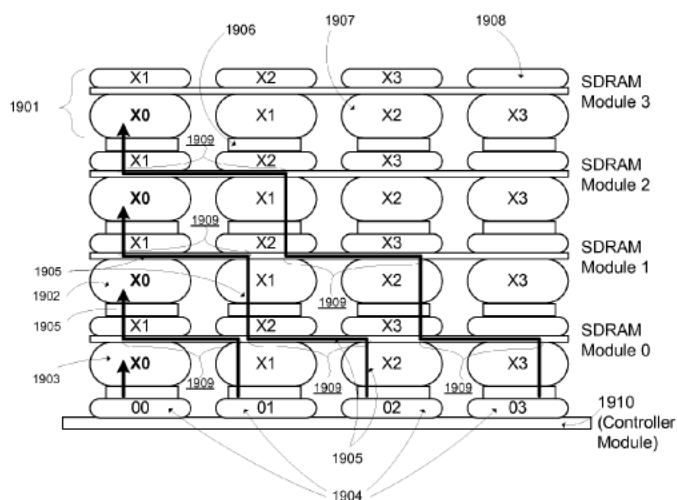


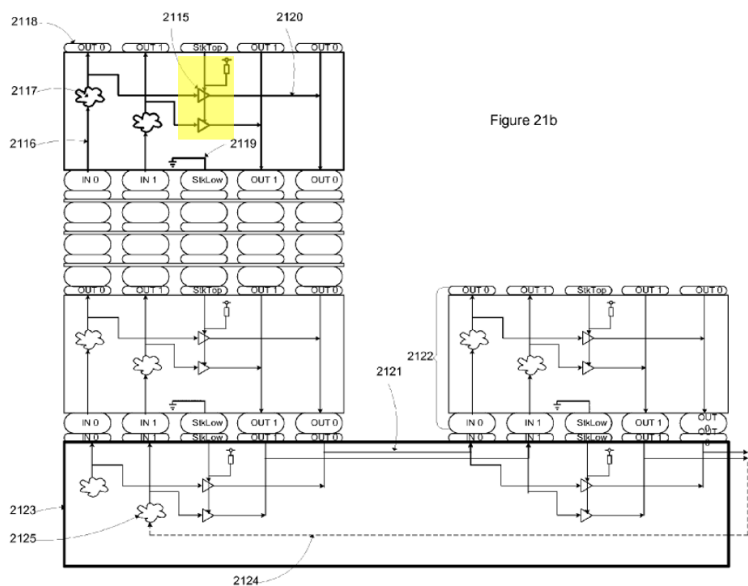
Figure 19

to allow stacking of *four identical modules*"). The specification states that the rotational stacking technique of certain embodiments is feasible only *because* the modules are identical. *Id.* at 9:32-38 ("*Since the stacked modules are identical*, we can use rotational stacking. . ."). Dependent claims also contemplate identical modules. *Id.* at cls. 3, 10 ("same location on one or more modules"), cl. 13 ("same location on the plurality of modules").

Further, the sole claimed embodiment *requires* identical stacked modules. The '243 patent describes the claimed "control circuit" and "control input signal" in connection with the embodiment of Figures 21a-b. *See id.* at 10:10-11 (as modified by Certificate of Correction). These illustrate a "connection technique . . . used for serial routing of all modules in the stack" that "allow[s] them to be externally accessible for horizontal expansion on a PCB." *Id.* at 9:61-64. The patent states that "*Since the modules are identical*," a routed signal can be passed through the

pads and balls of the stacked modules until it reaches an externally accessible “OUT pad.” *Id.* at 10:5-8. More specifically—and as shown in Figure 21b—“*All modules* have a control circuit that includes a selectable buffer 2115 that tri-states the input when pulled low.” *Id.* at 10:10-11 (as modified by Certificate of Correction), Fig. 21b (at right, with control circuit of top-left module highlighted). When a module is on top of the stack, the buffer 2115 control line is pulled high and

“let[s] the input signal branch out 2120 to the other pads, thus creating a connection route or trace that loops back to the base module solder balls.” *Id.* at 10:13-20; *supra* § III.A (annotated Fig. 21a showing serial chain routes connected via a routing path). Conversely, when a module is stacked below another



module, the buffer 2115 control line is pulled low and “disallow[s] the branching effect.” ’243 patent at 10:14-17, 20-24. This achieves “horizontal expansion” by routing the output signal to the OUT pads of the base module on the bottom of the stack. *Id.* at 10:24-26. But it is only *because* each module operates identically—with the same control circuit and the same tri-state buffer—that this arrangement works. *Id.* at 10:31-32 (“The tri-stated buffer technique is redundant to all locations.”).

Even if this Court determines that the disputed term is part of the preamble of claim 1, it is still limiting because the body of the claim depends on it for antecedent basis. *See In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019) (“We have repeatedly held a preamble limiting when it

serves as antecedent basis for a term appearing in the body of a claim.”). The last limitation of claim 1 recites “the plurality of modules.” ’243 patent at 10:59. This depends upon “a plurality of modules” for antecedent basis; there is no other mention of a “plurality of modules” in the claim.⁵ Additionally, because “a plurality of modules” is intertwined with “each comprising,” the entire phrase “a plurality of modules each comprising” is limiting. *See Bio-Rad Labs., Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1370-72 (Fed. Cir. 2020) (language intertwined with terms in preamble providing antecedent basis was also limiting). Further, as the discussion above shows, the “each comprising” aspect is “necessary to give life, meaning, and vitality” to the claimed module. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305-06 (Fed. Cir. 1999).

IV. ’740 PATENT

A. Technical Background

The ’740 patent is directed to purported solutions for optimizing memory operations by “optimally distribut[ing]” operational load across resources of the memory system, thereby “increasing operational efficiency, reducing memory operation latency or both.” ’740 patent at 1:16-24; 3:15-21.

The ’740 patent teaches a mapping table 9 (see Fig. 2 below) that maps LBA sets 40, 42, 44, and 45 from a host addressing system to PBAs 46, 48, 50, and 51 that can be used by an electronic storage device to

9

Logical Fields 26	PBA Fields 28			
	Access Parameter Fields 30			Memory Index Fields 32
	Bus Id Fields 34	FDE Id Fields 36	Group Id Fields 38	
40 LBAs 00-07	8-0	22-01	15-0	0x00 46
42 LBAs 08-15	8-0	22-02	15-1	0x08 48
44 LBAs 16-23	8-1	22-11	15-0	0x00 50
45 LBAs 24-31	8-1	22-12	15-1	0x08 51
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮

FIG. 2

⁵ The other references to “module” in claim 1 are to “[an / the] end module” (’243 patent at 10:55, 10:59-60), and “[another module / the another module] from the plurality of modules” (*id.* at 10:58-60). These refer to specific modules *within* the plurality, not to the plurality as a whole.

access the corresponding physical memory locations. *Id.* at 5:27-30. “LBA” refers to logical block addresses that “represent an address that is part of a logical addressing system . . . used by a host.” *Id.* at 6:37-54. LBA sets 40, 42, 44, and 45 “respectively represent consecutive LBAs used by host 18, such as LBAs 00 through 07, LBAs 08 through 15, LBAs 16 through 23, and LBAs 24-31.” *Id.* at 6:51-54.

“PBA” fields refer to physical block address fields that each represent a unique addressable physical memory location in a memory store, such as PBA fields 46, 48, 50 or 51. *Id.* For each PBA field, the physical memory location is represented by a set of access parameter fields 30 and memory index fields 32. *Id.* Each access parameter field 30 includes a Bus Id field 34, FDE Id field 36, and Group Id field 38, which essentially provide a path for accessing a specific physical memory location.

B. “optimized memory operations”

Patent	Plaintiff’s Proposal	Defendants’ Proposal
’740 patent: Claim 1	Plain and ordinary meaning; not indefinite.	Indefinite.

The phrase “optimized memory operations” in independent claim 1 of the ’740 patent is indefinite. Whether memory operations are within or outside the scope of the claim is impossible to decipher because the claim provides no criteria for assessing whether memory operations have been optimized. *Nautilus*, 572 U.S. at 901 (claim is indefinite when it “fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention.”). Nor does resort to the written description solve the problem. Although the written description includes one approach for optimizing memory transactions, constraining claim 1 to that example would render dependent claim 2 redundant and meaningless. Thus, claim 1 cannot be constrained to the illustration in the written description.

Asserted claim 1 requires a mapping table wherein, “in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform *optimized memory operations* on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.” ’740 patent, cl. 1 (emphasis added). The ’740 patent explains that “optimized memory operations” can be accomplished by “increasing the likelihood that, in response to an I/O transaction initiated by a host, the operational load will be ‘*optimally distributed*’ across different storage device resources, such as by interleaving or parallel memory operations, reducing memory operation latency, increasing operational device efficiency, or both.” *See id.* at 2:14-22 (emphasis added); *see also* 1:16-24, 3:12-21, 7:9-18, 9:19-25. The ’740 patent teaches only one way to “optimally distribute” operational load and thus optimize memory transactions—i.e., to map LBA sets to PBA fields such that memory transactions across multiple LBA sets can be conducted in parallel.

Figure 2 of the ’740 patent shows a mapping table in which LBA (logical block address) sets are associated with PBA (physical block address) fields consisting of access parameter fields 30 and memory index fields 32. ’740 2:14-22; 7:9-18, 9:19-25. For memory transactions across two or more LBA sets to be conducted in parallel, one or more of the access

Logical Fields 26	PBA Fields 28			
	Access Parameter Fields 30			Memory Index Fields 32
	Bus Id Fields 34	FDE Id Fields 36	Group Id Fields 38	
LBAs 00-07	8-0	22-01	15-0	0x00
LBAs 08-15	8-0	22-02	15-1	0x08
LBAs 16-23	8-1	22-11	15-0	0x00
LBAs 24-31	8-1	22-12	15-1	0x08
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮

FIG. 2

parameters associated with the LBA sets must be different. *Id.* As highlighted in red, the FDE

and Group ID access parameters associated with LBA sets 40 and 42 differ, which permits overlapping memory operations tied to those two LBA sets.

While claim 1 requires an I/O transaction to be associated with more than one LBA set, it does not require that the access parameters associated with said first and second LBA sets must be different as taught in the written description. *See* '740 patent, cl. 1 (“the I/O transaction request is associated with said first and second LBA sets”). Claim 2, which depends from claim 1, does require that difference. *See id.* at cl. 2 (“said first and second access parameters are different.”). Under the doctrine of claim differentiation, independent claim 1 presumptively has a broader scope from dependent claim 2. *See Phillips*, 415 F.3d at 1315. But interpreting “optimized memory operations” to mean the type of optimal distribution taught in the '740 patent would leave claim 1 and dependent claim 2 without any difference of scope, which is plainly not the correct reading of the claims. If on the other hand, claim 1 is given broader scope according to the ordinary meaning of “optimized memory operations,” claim 1 is indefinite because it fails to provide reasonably certain guidance about how to assess what is or is not optimal.

The court in *Chewy Inc. v. IBM Corp.*, 571 F. Supp. 3d 133, 153 (S.D.N.Y. 2021), addressed an analogous situation. There, the patentee argued that the term “on demand by said user” was not indefinite because the specification explained that “[f]or each search result item, a graphical user interface (GUI) selection is presented, allowing the user to select the GUI, on demand if so desired, to investigate related advertisement.” *Id.* Relying on this teaching in the specification, the patentee argued that “on demand by said user” is not indefinite and should be construed to mean “upon the user selecting a graphical user interface to investigate related advertisement.” *Id.* The court held that this interpretation failed as a matter of claim differentiation because another dependent claim recited the step of “displaying a graphical user interface to [the]

user.” *Id.* Because the patentee could not offer a construction that would render the disputed term meaningful without encroaching on the explicit language of another claim, the court found the disputed claim term to be indefinite. *Id.* As in *Chewy*, claim 1 is indefinite because there is no construction of claim 1 that would render the term “optimized memory operations” meaningful without encroaching on the explicit language of claim 2.

C. “optimally distributed”

Patent	Plaintiff’s Proposal	Defendants’ Proposal
’740 patent: Claim 32	Plain and ordinary meaning; not indefinite.	Indefinite.

The term “optimally distributed” as used in claim 32 of the ’740 patent is also indefinite for similar reasons as the term “optimized memory operations.” Claim 32 requires:

An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be ***optimally distributed*** across storage device resource ... wherein said mapping table increases the likelihood that that [sic] the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be ***optimally distributed*** across storage device resources.

’740 patent, cl. 32 (emphasis added).

Claim 32 describes “at least one difference between said first and second PBAs,” which is one of the predicate requirements for optimizing memory transactions (as described above), but it does not recite that the I/O transaction is associated with two LBA sets—the other predicate requirement. The latter requirement is part of claim 34, which depends from claim 32. *See id.* at cl. 34 (“wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA.”). Although claim 32 relates to two memory operations performed using two PBAs, that is the same as requiring an I/O transaction to be associated with two LBA sets because claim 32

requires that “a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA.” Again, claim differentiation suggests that claim 32 is broader than claim 34. *See Phillips*, 415 F.3d at 1315. It follows that claim 32 covers optimal distribution in the case where there is only a single set of LBAs. Here too, the patent provides no guidance as to how that is possible, leaving the scope of the claim indefinite.

D. “memory store”

Patent	Plaintiff’s Proposal	Defendants’ Proposal
’740 patent: Claims 1, 15, 32	“non-volatile, solid-state storage, e.g., flash”	Plain and ordinary meaning.

The term “memory store” should be given its plain and ordinary meaning, which is not limited to “non-volatile, solid-state storage, e.g., flash” memory as plaintiff suggests. For example, independent claim 1 recites a “memory store,” while claims 7, 8, and 15—each of which ultimately depends from claim 1—specifically recite that the memory store comprises either “a plurality of flash devices” or a “set of solid state memory devices.” Likewise, claim 17 recites a memory store that includes a first and second set of memory devices, while claim 19—which depends from claim 17—further recites that the first and second memory devices “include non-volatile solid state memory cells.” Under the doctrine of claim differentiation, “limitations stated in dependent claims are not to be read into the independent claim from which they depend.” *Nazomi Commc’ns, Inc. v. Arm Holdings, PLC*, 403 F.3d 1364, 1370 (Fed. Cir. 2005) (citations omitted); *Phillips*, 415 F.3d at 1314-15 (“[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.”). Accordingly, because the dependent claims expressly limit a “memory store” to solid state and flash devices (which reflect the outer boundaries of plaintiff’s proposed constructions), these limitations cannot be read into the broader construction of “memory device.”

This conclusion is further confirmed by asserted claims 15 and 32, which respectively state that the “memory store” “**includes** a set of solid state memory devices” and “**includes** a set of flash devices,” signifying an open-ended use of the term “memory store” that does not foreclose the inclusion of other types of memory devices. ’740 patent, cl. 15, 32 (emphases added); *see also*, *e.g.*, *In re Horvitz*, 168 F.2d 522, 525 (C.C.P.A. 1948) (holding that “comprises” is synonymous with “includes” and does not preclude the presence of other elements as part of the described structure). Indeed, construing a “memory store” to be limited to a solid state memory device or flash device would render the language in these claims redundant, further confirming that Plaintiff’s proposed construction is incorrect. *See Apple, Inc. v. Ameranth, Inc.*, 842 F.3d 1229, 1237 (Fed. Cir. 2016) (affirming that construction of a term should not include features “expressly recited in the claims” because “[c]onstruing a claim term to include features of that term already recited in the claims would make those expressly recited features redundant.”)

The specification also refutes Plaintiff’s proposed, narrow construction. As an initial matter, nothing in the specification expressly disclaims the use of devices other than solid-state storage devices. To the contrary, the specification states that “[m]emory store 6 **may be configured to include** a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs.” ’740 patent at 4:54-56 (emphasis added). Use of the phrase “may be configured to include” confirms that solid state memory devices are permitted but not required. The specification also states that “[t]he term ‘flash memory device,’” which constitutes one example of a memory store, “is intended to include **any form** of non-volatile memory, including those that use blocks of non-volatile memory cells, named flash blocks.” *Id.* at 4:59-62 (emphasis added). As a result, the specification establishes that the claims are not limited to solid-state storage devices.

BiTMICRO’s own Complaint demonstrates that BiTMICRO understands that the plain and ordinary meaning of the term “memory store” is not limited to non-volatile memory stores. For example, the Complaint, in discussing the ’190 patent, refers to Dynamic Random Access Memory (“DRAM”)—a volatile memory—as a type of memory store: “The Optane Persistent Memory product includes ‘a memory store.’ For example, the Optane Persistent Memory product *includes both DRAM memory* and persistent memory modules, *which separately* or in combination *are a memory store.*” No. 6:22-cv-00335-ADA, ECF No. 1 at ¶ 106 (emphases added). BiTMICRO’s proposed construction, which limits “memory store” to “non-volatile, solid-state storage, e.g., flash,” is inconsistent with even its own understanding of the plain and ordinary meaning of that term.

Since the intrinsic evidence alone is sufficient to rebut Plaintiff’s proposal, the Court need not consult extrinsic evidence. Nonetheless, Defendants’ extrinsic evidence confirms that the plain and ordinary meaning of “memory store” is not limited to “non-volatile, solid-state storage, e.g., flash” as BiTMICRO proposes. For example, the extrinsic illustrates the following:

- Definition of “memory”: “All of the addressable storage in a processing unit and other internal storage that is used to execute instructions.” Ta Decl., Ex. G, *The Authoritative Dictionary of IEEE Standards Terms* (7th ed.) at 684 (Inst. of Elec. & Electronics Engineers, Inc. 2000).
- Definition of “storage medium”: “Any device or recording medium into which data can be stored and held until some later time, and from which the entire original data can be obtained.” *Id.* at 1113.
- Definition of “memory”: “A device where information can be stored and retrieved.” Ta Decl., Ex. H, *Microsoft Computer Dictionary* (5th ed.) at 333 (Microsoft Corp.

2002).

- Definition of “storage”: “In computing, any device in or on which information can be kept. Microcomputers have two main types of storage: random access memory (RAM) and disk drives and other external storage media. Other types of storage include read-only memory (ROM) and buffers.” *Id.* at 498.

As the plain and ordinary meaning of “memory store” is well supported by the intrinsic and extrinsic record, the Court should reject BiTMICRO’s attempt to limit that term to “non-volatile, solid-state storage, e.g., flash” memory.

V. ’190 PATENT

A. Technical Background

The ’190 patent pertains to a “multi-profile memory controller” where memory locations are associated with different memory devices having different memory attributes. *See* ’190 patent at Abstract. The patent alleges that prior art memory controllers—components that control the flow of information going to and from a computer’s main memory—often managed memory devices that have the same memory device characteristics, e.g., flash memory devices that have the same large block size. *Id.* at 1:20-37. But in some instances, that shared characteristic might be undesirable: large block sizes may spawn latency and other issues. *Id.* at 1:38-43.

The ’190 patent is directed to memory controllers that “can perform memory transactions using different device profiles.” *Id.* at 3:61-63. The patent discloses that a memory store can include addressable memory locations associated with various memory attributes, such as the block size, the page size, the memory protocol, the memory device type, and the partial page size. *Id.* at 2:63-3:13. The memory attributes are organized into a “device profile.” *Id.* at 3:14-15. For example, in Figures 1 and 2B below, memory location 9 in memory store 4 may have a device profile 26 that includes attributes like “page size 28 associated with an attribute value of 1024

bytes, block size 30 associated with an attribute value of 2048 pages, a memory protocol 32 associated with an attribute type that represents the ONFi specification, a memory device type 34 associated with an attribute type that represents a NAND flash memory device, and a partial page size 36 associated with an attribute value of 512 bytes.” *Id.* at Fig. 1, 3:40-49. The patent further teaches that the alleged invention is not limited by the type of memory device or any number of innumerable attributes or device profiles. *Id.* at 3:61-64, 4:26-28. 5:4-6.

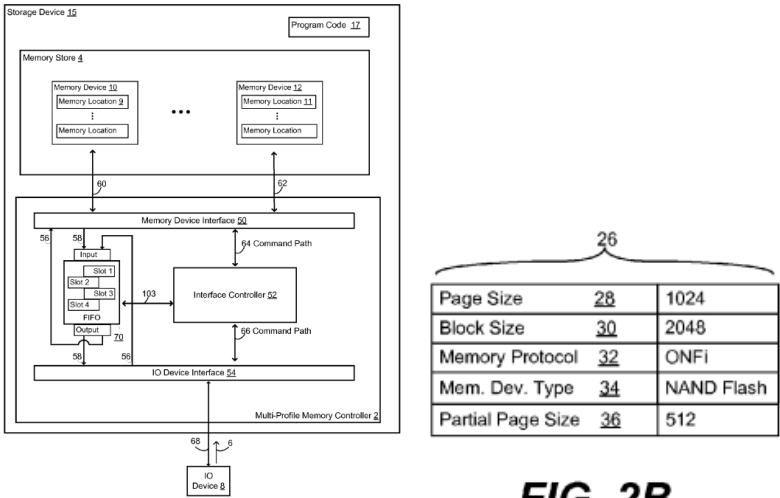


FIG. 1

FIG. 2B

B. “optimal”

Patent	Plaintiff’s Proposal	Defendants’ Proposal
’190 patent: Claims 1, 29, 45, 59, 80, 98	Plain and ordinary meaning; not indefinite.	Indefinite.

The term “optimal” as used in the ’190 patent to describe a “first device profile” is indefinite for failing to satisfy 35 U.S.C. § 112, ¶ 2. “[A] term of degree fails to provide sufficient notice of its scope if it depends on the unpredictable vagaries of any one person’s opinion.” *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014) (citation and internal quotation marks omitted). Here, the term “optimal” is a subjective term of degree, dependent on the characteristic sought to be optimized for any given device profile. *See, e.g., Intellectual*

Ventures I LLC v. T-Mobile USA, Inc., 902 F.3d 1372, 1381 (Fed. Cir. 2018) (“‘[O]ptimiz[ing] . . . QoS’ is a ‘term of degree’ that . . . is ‘purely subjective’ . . .”).

Asserted claims 1, 29, 45, 59, 80, and 98 each claim a “first device profile” that is “optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type.” ’190 patent at cl. 1, 29, 45, 59, 80, 98. Here, the specification notes that a “multi-profile” memory controller can “support[] memory locations that have different device profiles” that are optimal for different data types. *Id.* at 9:7-16. “One target memory location” “is optimal for the type of data subject to a memory transaction request,” while “another memory location” “is associated with another device profile that is optimal for the type of data subject to another memory transaction request.” *Id.* at 9:7-16. But it is unclear from the specification what criteria would make a device profile optimal for a particular data type.

At most, the specification provides three examples of device profiles that “may be desired” when a memory transaction request relates to a particular data type:

- (1) a device profile “that includes a block size attribute value that is the largest available from the other device profiles” when the data type is sequential (*id.* at 9:16-26);
- (2) a device profile “that includes a block size attribute value that is the smallest available from the other device profiles” when the data type is random (*id.* at 9:27-35); and
- (3) a device profile “that includes a partial page size attribute value” when the data type is random and “the data size of the data subject to the write transaction is at most equal to the partial page size attribute value” (*id.* at 9:35-43).

Despite these suggestions, the patent does not explain how to determine when one proposed approach would actually be desired and therefore “optimal.” Furthermore, the specification states that these three examples are not limiting (*see id.* at 9:43-44), and that the memory controller could

include code or use a map that “determines or causes” which memory locations are used for particular data types (*id.* at 9:44-48). The patent even states that “numerous implementation-specific decisions must be made to achieve [a] developer’s specific goals” and such “specific goals will vary from one implementation to another and from one developer to another.” *Id.* at 2:32-36. The patent fails to provide any explanation for how the memory device would select an optimal device profile based on the data type in any of those innumerable situations. The specification’s conclusory statements and three incomplete examples thus fail to provide the metes and bounds for when a particular device profile would be optimal for a particular data type, as required by the claim language.

A similar situation was present in *Intellectual Ventures I LLC v. T Mobile USA, Inc.*, No. 2:17-CV-00577-JRG, 2018 WL 5809267, at *4-5 (E.D. Tex. Nov. 6, 2018). There, the court found indefiniteness where the specification of the patent-at-issue provided two potential definitions for what would constitute “‘optimal’ performance in terms of handling communications in ways that depend on the types of data being communicated,” but failed to provide the metes and bounds of when performance would actually be considered optimal. In one example in *T Mobile*, optimal performance depended on the type of data being communicated—similar to how an optimal device profile for a given data type here may depend on block size, page size, or some other memory device attributes. *Id.* at 4. In another example recited in *T Mobile*, optimal performance “depend[ed] on how ‘the user defines it’”—a definition that is just as open-ended as the code or map implementation disclosed in the specification here. *Id.* at *5. As a result, the Court found that the specification failed to provide “sufficient ‘objective boundaries’ for those of skill in the art to understand the scope of the claims.” *Id.* at *5 (citation omitted).

Because the intrinsic record here fails to inform one of ordinary skill in the art with

reasonable certainty what objective boundaries and criteria are relevant to assessing an “optimal” device profile, the asserted claims should be found to be indefinite.

VI. '084 AND '694 PATENTS

A. Technical Background

The '084 and '694 patents describe techniques that use “a minimum amount of nonvolatile memory” to boot an embedded system through the use of a specialized data structure called a Power-On Reset (“POR”) Sequencer Descriptor. '084 patent at 2:23-25, 3:47-51.⁶ The embedded system of “[t]he present invention comprises . . . a Power-On Reset Sequencer which controls the overall boot process of the embedded system; nonvolatile memory and controller used to store data used by the Power-On Reset Sequencer in the boot process; [and] at least one direct memory access (DMA) controller which initiates and tracks data transfers.” *Id.* at 2:31-42. When the system powers up, the POR Sequencer and DMA controller are released from reset, and the POR Sequencer detects the POR Sequencer Descriptor in nonvolatile memory. *Id.* at 3:16-21. The

POR Sequencer Descriptor

includes information for configuring system registers and DMA descriptor information. *Id.* at 6:19-28,

Fig. 4 (annotated at right, with

register information in yellow and DMA descriptor information in green).

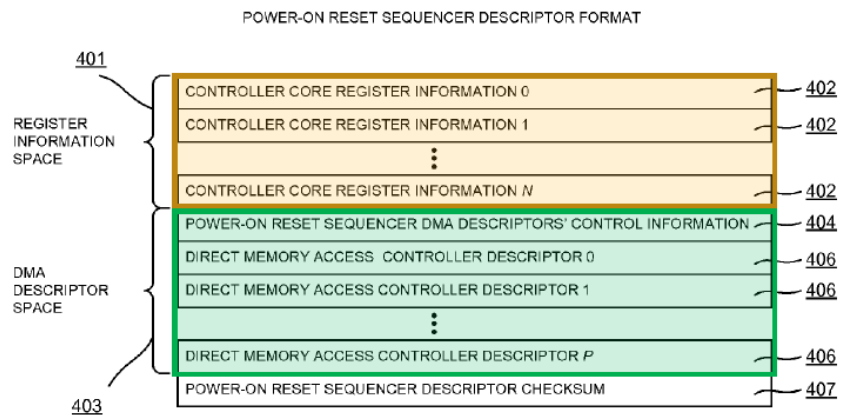


Figure 4

The POR Sequencer copies the POR Sequencer Descriptor to RAM and uses the register information to update the system’s configuration registers. *Id.* at 2:54-56, 3:28-34. Then it loads

⁶ The '084 and '694 patent specifications are nearly identical. Intel cites to the '084 patent specification for simplicity; the '694 patent contains parallel disclosure unless otherwise noted.

the DMA descriptors to the DMA controller. *Id.* at 2:56-58. If the DMA descriptor points to more register information, the DMA controller fetches that information and updates the POR Sequencer Descriptor; if the DMA descriptor points to firmware, the DMA controller copies that firmware to RAM. *Id.* at 3:35-45. When the DMA controller has finished copying all firmware, system CPU(s) are released from reset and execute the firmware to complete the boot process. *Id.* at 3:62-67.

B. “Direct Memory Access (DMA) descriptors” / “DMA controller descriptor”

Patent	Plaintiff’s Proposal	Intel’s Proposal
’084 Patent: Claims 1, 19 ’694 Patent: Claims 1, 6, 12	Plain and ordinary meaning; not indefinite.	“data structure including at least a source and destination address and byte count”

The ’084 patent independent claims recite a “POR sequencer descriptor” that includes “Direct Memory Access (DMA) descriptors used to fetch other POR sequencer descriptor fragments.” ’084 patent at 9:18-22, 10:56-60; *accord* ’694 patent at 9:31-32, 10:8-9, 10:60-61 (“POR sequencer descriptor includes . . . DMA controller descriptors”). Thus, while the claims plainly require that the POR sequencer descriptor includes DMA descriptors, it is not clear what type of information would qualify as a “DMA descriptor.”

Direct Memory Access, or DMA, is a technique for transferring data or code in a system without using the CPU. Alpert Decl. ¶ 15. DMA transfers are typically handled by a specialized device called a DMA controller. *Id.*; *see* ’084 patent at 2:31-42 (“The present invention comprises . . . at least one direct memory access (DMA) controller which initiates and tracks data transfers”). To perform a DMA transfer, a DMA controller requires, at a minimum, three pieces of information: the source location of the data/code to be transferred; the amount (*i.e.*, the length) of whatever is to be transferred; and the destination where the data/code is to be sent. Alpert Decl. ¶ 14. A DMA “descriptor” is a data structure that includes this basic information. *Id.* ¶¶ 15-16. DMA descriptors may have additional information as well, such as a pointer linking to another

DMA descriptor that describes a subsequent transfer operation. *Id.* ¶ 16; *see* '084 patent at Fig. 5, 6:44-46 (“The last DMA controller descriptor 506 . . . points to the next POR sequencer descriptor fragment 502.”).

The '084/'694 patents describe using DMA descriptors in precisely this way. Alpert Decl. ¶ 18. The POR Sequencer loads “DMA descriptors . . . to the DMA controllers of the system.” '084 patent at 2:56-58; *id.* at 7:29-32. The DMA controllers use the DMA descriptors to “initiate[] and track[] data transfers.” *Id.* at 5:3-4. A DMA controller processes each DMA descriptor depending on the information the descriptor “points to,” *i.e.*, what is stored at a particular source address. Specifically, “[i]f the DMA descriptor points to another set of register information,” the DMA controller transfers that information to RAM and updates the POR Sequencer Descriptor. *Id.* at 3:36-40; *id.* at 7:33-37, 7:41-45. “If the DMA descriptor points to a system firmware fragment,” the DMA controller “cop[ies] the system firmware fragments to the RAM.” *Id.* at 3:40-51.

The '084/'694 patents thus describe DMA descriptors as used to *fetch and transfer* data or firmware. *E.g.*, '084 at 7:47-50 (DMA descriptors are used “to fetch POR sequencer descriptor fragments . . . [and] also used to transfer system firmware . . . to the RAM”). The patents also repeatedly describe DMA descriptors as “pointing to” content to be fetched and transferred. *E.g.*, '084 patent at 3:36-42, 3:47-49, 3:54-60, 6:44-46, 6:52-55, 7:41-44, 7:63-66, 8:3-9. And to perform transfers, the DMA controller must know, at a minimum, where to find the content to be transferred (*i.e.*, the source location “pointed to” by the descriptor); the size of that content; and the destination where the content should be transferred. Alpert Decl. ¶¶ 15-18. Thus, a “DMA descriptor” or “DMA controller descriptor,” as used in the claims of the '084 and '694 patents, is a data structure that includes a source address, a byte count, and a destination address.

VII. CONCLUSION

Defendants respectfully request that the Court adopt their proposed constructions for the claim terms at issue.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

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