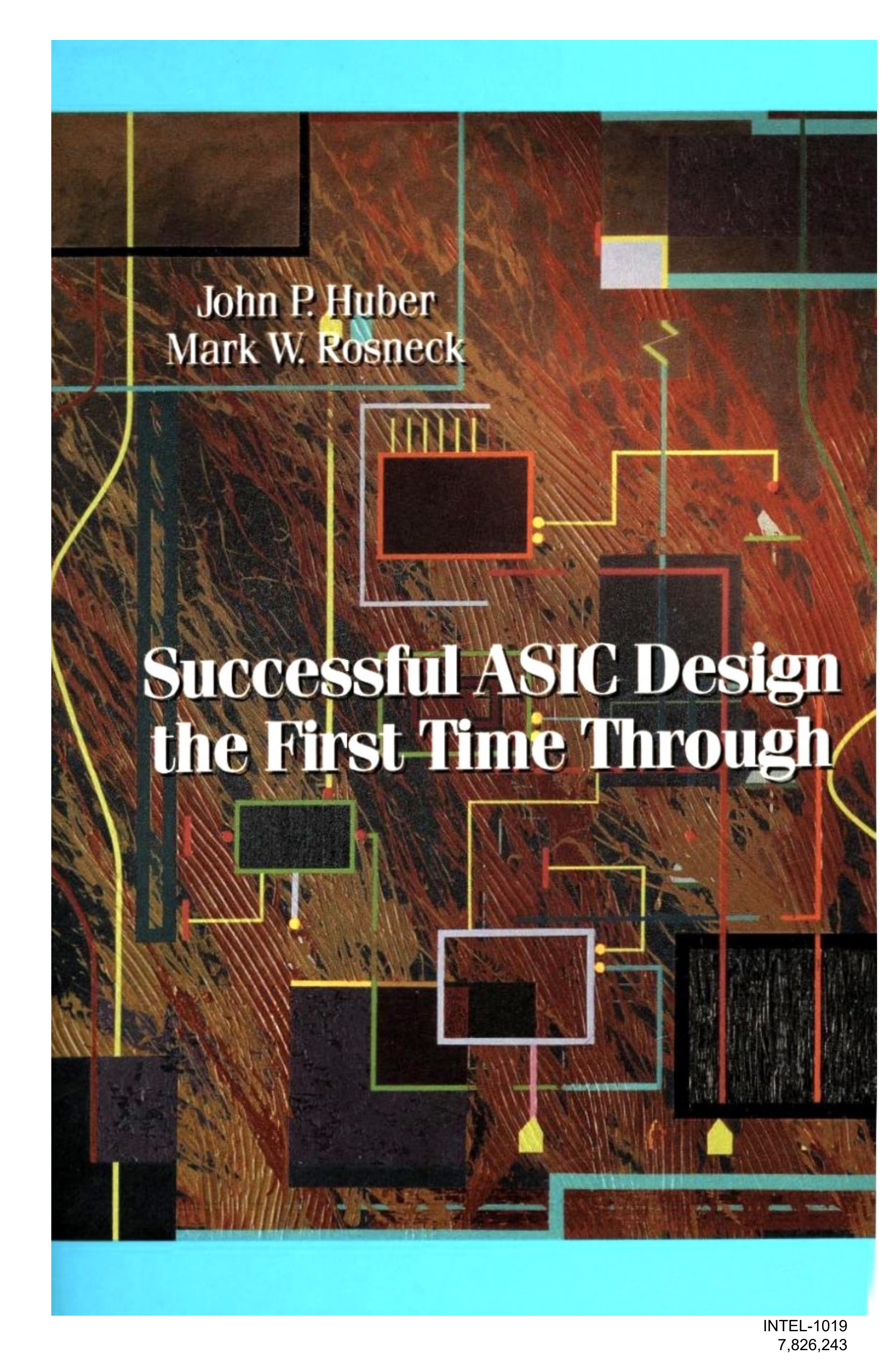




John P. Huber
Mark W. Rosneck

Successful ASIC Design the First Time Through

Successful ASIC Design the First Time Through

John P. Huber and
Mark W. Rosneck



Van Nostrand Reinhold
NEW YORK

Trademarks of the Mentor Graphics Corporation

QuickPath™ critical path analyzer
QuickSim II™ digital logic simulator
QuickFault II™ fault simulator
QuickGrade II™ fault grader
Design Architect™ design creation
NetEd™ Schematic drawing editor
SymEd™ Symbols drawing editor
System 1076™ VHDL design and simulation product
Genesil™ Silicon Compiler

Verilog is a registered trademark of **Cadence Design Systems**

Copyright © 1991 by Van Nostrand Reinhold

Library of Congress Catalog Card Number 90-49999
ISBN 0-442-00312-9

All rights reserved. No part of this work covered by the copyright hereon may be reproduced or used in any form by any means—graphic, electronic, or mechanical, including photocopying, recording, taping, or information storage and retrieval systems—without written permission of the publisher.

Printed in the United States of America

Van Nostrand Reinhold
115 Fifth Avenue
New York, New York 10003

Chapman and Hall
2-6 Boundary Row
London, SE1 8HN, England

Thomas Nelson Australia
102 Dodds Street
South Melbourne 3205
Victoria, Australia

Nelson Canada
1120 Birchmount Road
Scarborough, Ontario M1K 5G4, Canada

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

Library of Congress Cataloging-in-Publication Data

Huber, John P.

Successful ASIC design the first time through / John P. Huber & Mark W. Rosneck.

p. cm.

Includes index.

ISBN 0-442-00312-9

1. Application specific integrated circuits—Design and construction. 2. VHDL (Computer hardware description language)

I. Rosneck, Mark W. II. Title.

TK7874.H83 1991

621.39'5—dc20

90-49999

CIP

*To Terri and Debbie, who stood by us through
the late nights and long weekends to make this
book possible.*

Scan design synthesis may also be available. This turns a nonscan design into a scan design by replacing standard latches with scan cells, adding the scan clock circuitry, and connecting the scan cells into chains. It may be necessary to tune the synthesized design to meet timing criteria.

Design verification is still required to verify the functionality of the design. However, since scan designs are synchronous, zero delay simulation can be employed quite effectively. More efficient design verification is another added benefit of scan.

After successful design verification, the designer is ready to enter the test development phase. Often the design data will need to be optimized for use by the scan tools. After this new scan model is built, critical path analysis is normally utilized to provide timing verification.

An automatic test pattern generator (ATPG) program can then be run to create the scan patterns. This is the point where the benefits of scan are most readily apparent, since patterns can be created in hours that would require weeks or months to generate by hand. The fault coverage created by the ATPG program will be quite high, generally in excess of 99%. The scan patterns are normally then run through a test postprocessor to modify them for the specific syntax of the target scan tester.

Many designers feel that scan is an absolute imperative given the testing demands of today's ASIC designs, and the dramatically increasing popularity of scan is testimony to its effectiveness. However, should you decide to use scan, be certain that you adopt a total methodology that supports scan from schematic capture to testing the finished device on the tester. Failure to do so could result in the real estate used to implement scan going to waste because an adequate scan tester is unobtainable.

EMERGING TEST TECHNOLOGIES

As we have seen, the cost of generating tests for ASIC designs can be significant. However, the cost of inadequate testing can be disastrous. To meet the need for improved test techniques, a number of technologies have evolved, including built-in self-test (BIST), boundary scan, and embedded test matrix.

BIST

BIST is a scheme for generating test vectors within the ASIC and reporting a go/no-go result to a primary output. In general, the term BIST

encompasses a wide variety of test methods that meet these criteria. However, BIST is most often implemented through the use of a pseudo-random sequence generator that supplies a repeatable sequence of random data to a block of logic. Results from each test are combined with the result of the previous test through a technique known as signature analysis. After a known quantity of tests have been run against the logic block, a control signal is used to compare the computed signature with a signature programmed into the ASIC by the designer. A matching signature indicates that the logic block passed the test.

BIST is often used to test embedded RAM structures, since a great number of vectors are needed and these are difficult to create using any other technique. In addition, a random testing approach has been shown to be very effective with embedded RAM.

BIST should be designed with great care if it is to be effective. In general, BIST is most useful on extremely regular structures such as memories or purely combinational blocks. In any case, be very careful that only valid data are captured by the signature analysis registers since on the production line a single bit error will be sufficient to indict the device as defective.

Boundary Scan (JTAG)

Boundary scan is a specialized scan structure principally designed to aid with board-level test. Utilizing boundary scan implies the addition of logic to the design to allow the primary pins of the design to be electrically isolated. Data are input and output from the logic normally connected to these primary pins by shift registers, which are enabled by a dedicated test pin on the ASIC. In this way the ASIC is effectively isolated from the rest of the components on the circuit board, allowing test data to be applied to the ASIC without the burden of propagating test vectors through many levels of logic. An added benefit is the ability to identify a defective component on the circuit board immediately, without time-consuming guided fault analysis. In general, boundary scan can be a very effective technique for improving the manufacturability of complex printed circuit boards. Figures 8-8 and 8-9 demonstrate a scan path architecture.

Boundary scan has been highly promoted by an international consortium of companies known as the Joint Test Advisory Group (JTAG). Philips, Texas Instruments, British Telecom, AT&T, and IBM are among the major contributors to JTAG. JTAG has been very active in promoting

Device PIs and POs in boundary scan mode

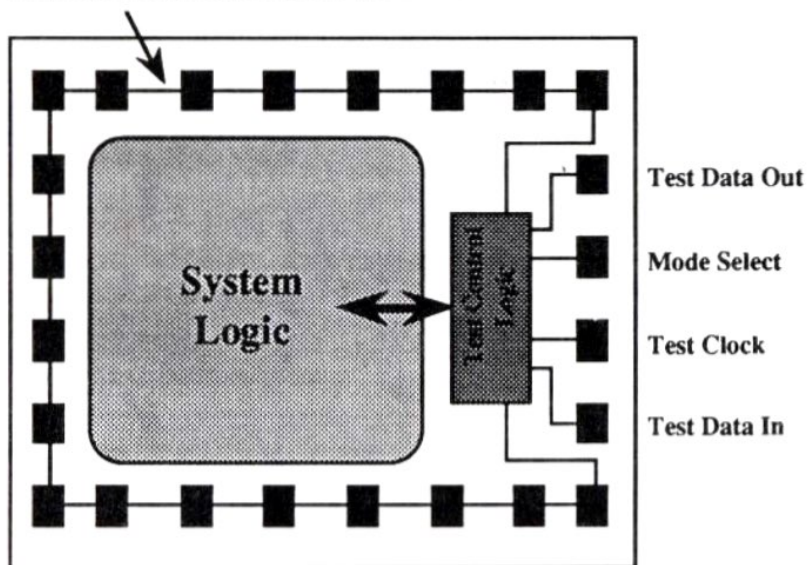


FIGURE 8-8. Boundary scan architecture.

standards in the test industry, particularly in the area of boundary scan. IEEE P1149.1 is a proposed standard for implementing a boundary scan architecture. P1149.1 describes a methodology for implementing boundary scan that minimizes real estate usage and performance degradation. The architecture consists of an instruction register to control switching between test and normal operating modes, a test access port (TAP) for applying test data, and a boundary scan register (BSR).

P1149.1 boundary scan is becoming very well known and popular in the industry as companies seek innovative ways to control test and manufacturing costs. The addition of boundary scan to an ASIC design will cost very little in real estate and can have immense benefits in manufacturing. However, the methodology *must* be consistently applied to the circuit board design to be of any use. Be certain to meet with the circuit board designer and test engineering to verify that the boundary scan design is completely carried through to the board design. It is most disheartening to see a well-implemented boundary scan ASIC mounted on a circuit board with the test circuitry hard-wired to power or ground. Additionally, be certain that the test circuitry cannot be accidentally enabled during normal operation of the circuit board *unless* the board has been specifically designed for self-diagnosis.

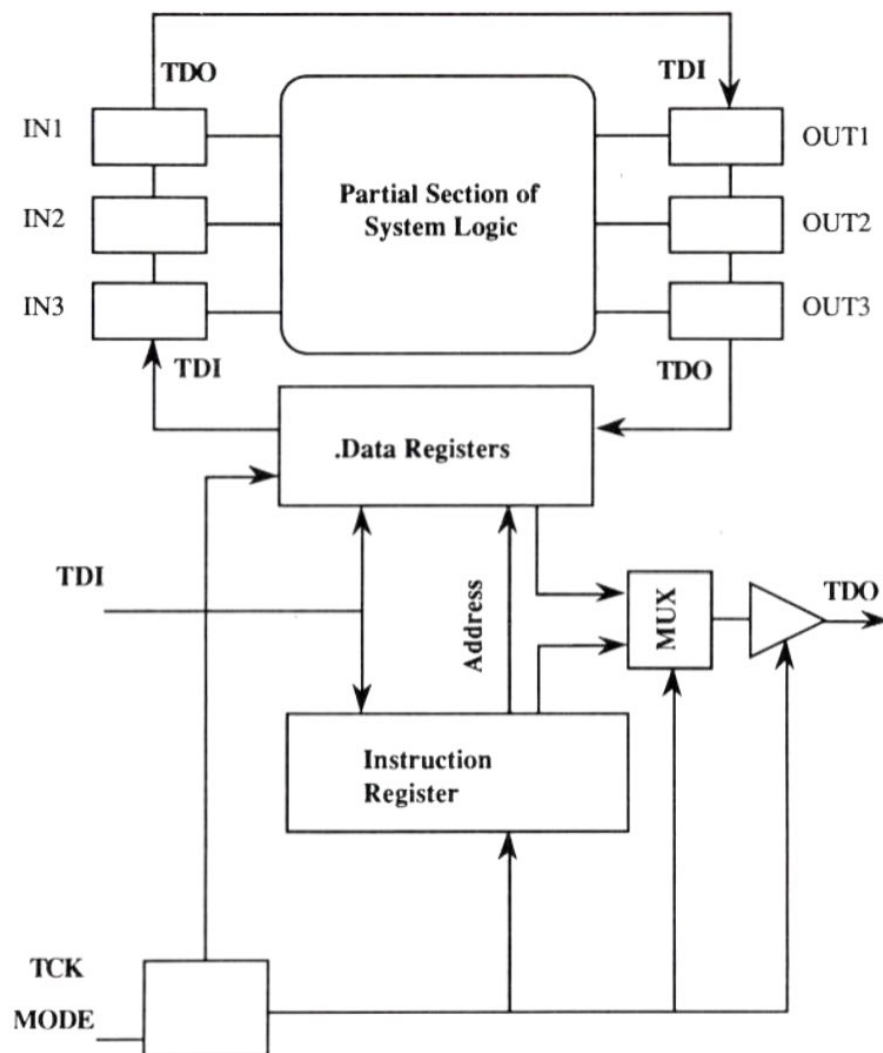


FIGURE 8-9. JTAG architecture.

Embedded Test Matrix

One of the most promising of the emerging test technologies is embedded test matrix, which is being developed by the CrossCheck corporation. This proprietary technology permits every node in the design to be completely observable, allowing for extremely high fault coverage with normal functional test techniques. Check with the ASIC vendor for