SCOTT EMMET THOMPSON

Prof. Electrical Engineering and Computer Science Department / Univ. of Florida
IEEE Fellow for contributions on advancing MOSFETs
Former Intel Corporation Fellow and Director of Computer Chip Technology

A. Education and Training

Education

1992 Ph.D. (Electrical Engineering), University of Florida
1988 Master of Science in Electrical Engineering, University of Florida
1987 Bachelor of Electrical Engineering with Highest Honors, University of Florida

B. Professional Experience

- Tenure Full Professor and Faculty/ Electrical and Computer Engineering, University of Florida (2/2004 to present).
- Founder and CTO of SuVolta (a low power chip company) (2009 - 2/2015).
    - Technology sold to Fujitsu and used in Mibeaut image sensor processor
- Researcher on advanced chip technology at University of Florida totaling $4M worth of research contracts.
    - 2019-2021 Research funding from Semiconductor Research Corporation (SRC)
- Consultant in semiconductor/computer chip industry (non litigation) last last 10 years: Cypress Semiconductor, Xperi Corporation, Intermolecular Inc, SuVolta, International Electron Device Meeting.
- **Intel Corporation** 1992 to 2004. Intel Fellow (highest technical level) and Director of computer chip technology (semiconductor manufacturing) including transferring and bringing up new manufacturing facilities worldwide.
- Intel Corporation experience and industry consulting on semiconductor manufacturing, semiconductor technology, yield and quality.
- Developed ultra low power chip technology for image sensors, SOC, RFIC, Memory, CPU, image sensors processors and other chips.
- Developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design and packaging technology (chip stacking) and computer chip technology including CPU, DRAM, GPU, image sensors, 2D and 3D image sensor processing.
- National Science Foundation Panel Reviewer for semiconductor/computer chip funding.

INTEL-1004
7,826,243

C. Legal cases (6 depositions and 3 time testimony at trial**)**

- Bold is the client
  - Amberwave v. **Intel Corporation** 2005-2006
  - Siliconix v. **Alpha Omega Semiconductor** 2007-2008
    - Exert report Jan, 2008 Judicial Arbitration and Mediation Service Ref 1110009946
    - Deposition Feb 6, 2008
    - Testimony at Trial Feb 2008
  - National Semiconductor v. **Alpha Omega Semiconductor** 2008-2009
  - **Intellectual Ventures** v. Canon
    - Expert report and deposition
    - Expert report: Oct 19, 2015 No. 1:11:00792-SLR - filed 9/9/2011
    - Deposition: United State district court for the District of Delaware, Nov 10th 2015 No. 11-792
  - **Round Rock Research, LLC** v. Nintendo Co., LTD and Ricoh Americas Corp
    - Declaration claims construction brief for Markman hearing
    - Declaration 01-21-2016 C. A. No. 1:14-cv-1491-SLR-SRF (D. Del.) - filed 12/17/2014
    - Supplemental Declaration 04-05-2016, C. A. No. 1:15-cv-157-SLR-SRF (D. Del.) - filed 2/13/2015
  - **Labaton Sucarow** /**Motley Rice LLP** v. Advanced Micro Devices, Inc.
    - Amended class action complaint, United States District Court Northern District of California, 05/23/14, No. 3:14-cv-00226-JD - filed 1/15/2014
    - Expert Report (Nov/2016), Rebuttal Report(Jan/2017) and Deposition (March/2017)
  - Godo Kaisha IP Bridge v/ **Xilinx**/**TSMC**
    - 7/2017 - 2018 Industry and expert witness
    - Case No. 2:17-CV-00100-JRG-RSP (E.D. Tex.) - filed 1/31/2017
  - KAIST IP v. **Apple**
    - 2018-2019 Industry and expert witness
    - Feb/2018 File report for Apple to Korea Trade Commission
    - May/2018 Supplemental Report to Korea Trade Commission
    - March /2019 Report to Intellectual Property Trial and Appeals board regarding Korean Patent No. 10-0458288
    - Case in Korea : Intellectual Property Trial and Appeal Board ("IPTAB") regarding Korean Patent No. 10-0458288 (hereinafter, "KR '288 patent").
  - IP Bridge, Inc. v. **NVIDIA** Godo Kaisha
    - NVIDIA Singapore Pte Ltd. as a technical expert in the customs proceeding initiated by petitioner Godo Kaisha IP Bridge 1

- Chinese Academy of Sciences v. **Intel**
    - IPR report Sept / 2018 in case IPR2018-01574 - filed 9/18/2018
    - IPR report Mar / 2019 in case IPR2019-00834 - filed 3/19/2019
    - Beijing Court Testimony IME vs Lenovo 11/21/2021
    - Beijing court Testimony IME vs Intel China 1/12/2022
- IFT v. **TSMC (**ITC case)
    - Case 1:19-cv-00308-UNA (D. Del.) - filed 2/13/2019
    - Inv. No. 337-TA-1149 - initial notice 4/3/2019
- NXP v. **Impinj**
    - 9,495,631, IPR2020-00543 - filed 2/10/2020
    - 9,633,302, IPR2020-00516 - filed 2/5/2020
    - 6,680,523, IPR2020-01630 - filed 9/17/2020
        - Deposition 7/7/2021
    - 7,538,444, IPR2021-00003 - filed 10/5/2020
    - Infringement Report 6/17/2022
        - Deposition Infringement Report 9/6/2022
    - Validity Report 8/16/2022
        - Deposition Validity Report 9/7/2022
- Ericsson v. **Apple** 2022
- Greenthread v. **Intel** 2022

Honors and Awards

- 100 granted US patents, 60 publications and 1 book on semiconductors
- Elected to **IEEE Fellow** in 2006 for Advancing Fabrication of nanoscale MOSFET
- Elected to Intel Fellow in 2003
- Thompson and co-workers were the first to publish at the International Electron Device Meeting (IEDM) in 2002 on a 90nm logic technology which introduced high levels of strain for significant mobility enhancement using SiGe
- 2008 SEMI award North American Recipient
- 2014 TiE 50: Top Startup (SuVolta)
- 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology: SuVolta
- 2011 EuroAsia IC Industry Award for start-up
- 2008 Semi Award North America (for Develop of Strained Silicon Transistors)

D. Publications/Patents

[1] T. A. Weingartner, C. -H. Kuo, A. Thomas, S. E. Thompson and M. E. Law, "Negative Impact of Compressive Biaxial Stress on High Precision Bipolar Devices," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, doi: 10.1109/TCPMT.2021.3095670.

[2] C.-H. Kuo, T. A. Weingartner, M. E. Law, S. E. Thompson, and A. Appaswamy, *Effect of Stress on Bipolar Transistor,* SRC TECHCON 2021

[3] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent 10,250,257, 2019.

[4] S. E. Thompson et al., "Advanced Transistors with Punch Through Suppression", US Patent US10325986B2, 2019.

[5] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10,217,668, 2019.

[6] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10224244B2, 2019.

[7] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent US20180248548A1, 2018.

[8] S.E. Thompson et.al., "Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof", US9865596B2, 2018.

[9] S.E. Thompson et al. "Integrated Circuit Devices and Methods", US Patent US9966130B2, 2018

[10] S.E. Thompson et al. "Buried Channel Deeply Depleted Channel Transistor, US Patent US9991300B2, 2018.

[11] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent US10074568B2, 2018

[12] S.E. Thompson et al., Transistor With Threshold Voltage Set Notch and Method of Fabrication Thereof" US Patent US9922977B2, 2018.

[13] S. E. Thompson et. al., "Buried Channel Deeply Depleted Channel Transistor," US 9,786,703 B2, 2017.

[14] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US 2017/0117366 A1, 2017.

[15] S. E. Thompson et. al., "Field Effect Transistor And Method For Producing The Same," JP2017055140A, 2017.

[16] S. E. Thompson et. al., "Advanced Transistors With Punch Through Suppression," US 2017/0040419 A1, 2017.

[17] S. E. Thompson et. al., "Digital Circuits Having Improved Transistor, and Methods Therefor," US 9,838,012 B2, 2017.

[18] S. E. Thompson et. al., "Low Power Semiconductor Transistor Structure And Method Of Fabrication Thereof," US 2017/0012044 A1, 2017.

[19] S. E. Thompson et. al., "Integrated Circuit Devices And Methods," US 9,741,428 B2, 2017.

[20] S. E. Thompson et. al., “Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof,” US 9,496,261, 2016.

[21] S. E. Thompson et. al., “CMOS Gate Stack Structures And Processes,” US 9,508,728 B2, 2016.

[22] S. E. Thompson et. al., “Integrated Circuit Devices and Methods,” US 9,362,291 B1, 2016.

[23] S. E. Thompson et. al., “Method For Fabricating A Transistor With Reduced Junction Leakage Current,” US 9,368,624 B2, 2016.

[24] S. E. Thompson et. al., “Advanced Transistors With Punch Through Suppression,” US 9,263,523 B2, 2016.

[25] S. E. Thompson et. al., “Analog Circuits Having Improved Transistors, And Methods Therefor,” US 9,231,541 B2, 2016.

[26] S. E. Thompson et. al., “Electronic Devices and Systems, and Methods for Making and Using the Same,” US 2016/0358918 A1, 2016.

[27] S. E. Thompson et. al., “Buried Channel Deeply Depleted Channel Transistor,” US 9,478,571 B1, 2016.

[28] S. E. Thompson et. al., “Transistor With Threshold Voltage Set Notch and Method of Fabrication Thereof,” US 9,418,987 B2, 2016.

[29] S. E. Thompson et. al., “Method For Fabricating Multiple Transistor Devices on a Substrate With Varying Threshold Voltages,” US 9,406,567 B1, 2016.

[30] S. E. Thompson et. al., “CMOS Structures and Processes Based On Selective Thinning,” US 9,391,076 B1, 2016.

[31] S. E. Thompson et. al., “Epitaxial Channel Transistor and Die With Diffusion Doped Channels,” US 2016/0211346 A1, 2016.

[32] S. E. Thompson et. al., “Digital Circuits Having Improved Transistors, and Methods Therefor,” US 2016/0020768 A1, 2016.

[33] S. E. Thompson et. al., “Analog Circuits Having Improved Transistors, And Methods Therefor,” US 2015/0015334 A1, 2015.

[34] S. E. Thompson et. al., “High Uniformity Screen And Epitaxial Layers For CMOS Devices,” US 9,196,727 B2, 2015.

[35] S. E. Thompson et. al., “Porting A Circuit Design From A First Semiconductor Process To A Second Semiconductor Process,” US 9,117,746 B1, 2015.

[36] S. E. Thompson et. al., “Digital Circuits Having Improved Transistors, And Methods Therefor,” US 9,184,750 B1, 2015.

[37] S. E. Thompson et. al., “Embedded Channel Type Deep Depletion Channel Transistor,” JP2015226059A, 2015.

[38] S. E. Thompson et. al., “Deeply Depleted MOS Transistors Having A Screening Layer And Methods Thereof,” US 9,041,126 B2, 2015.

[39] S. E. Thompson et. al., “Field Effect Transistor (FET) And Method For Fabricating The Same,” JP2015195403A, 2015.

[40] S. E. Thompson et. al., “Analog Transistor,” US 9,093,469 B2, 2015.

[41] S. E. Thompson et. al., “Semiconductor Devices Having Fin Structures and Fabrication Methods Thereof,” US 9,054,219 B1, 2015.

[42] S. E. Thompson et. al., “Field Effect Transistor and Methods for Producing The Same,” JP2015213200A, 2015.

[43] S. E. Thompson et. al., “Electronic Devices and Systems, And Methods For Making And Using The Same,” US 8,975,128 B2, 2015.

[44] S. E. Thompson, “Advanced CMOS Device Physics for 7nm and Beyond,” in Invited Short Course at International Electron Device Meeeting, Washington D.C., 2015.

[45] S. E. Thompson et. al., “Advanced Transistor With Punch Through Suppression,” US 2014/0167156 A1, 2014.

[46] S. E. Thompson et. al., “Analog Circuits Having Improved Transistors, And Methods Therefor,” US 8,847,684 B2, 2014.

[47] S. E. Thompson et. al., “Integrated Circuit Devices And Methods,” US 8,811,068 B1, 2014.

[48] S. E. Thompson et. al., “Transistor With Threshold Voltage Set Notch And Method Of Fabrication Thereof,” US 8,759,872 B2, 2014.

[49] S. E. Thompson et. al., “Monitoring And Measurement of Thin Film Layers,” US 8,796,048 B1, 2014.

[50] S. E. Thompson et. al., “Deeply Depleted MOS Transistors Having A Screening Layer And Methods Therof,” US 2014/0084385 A1, 2014.

[51] S. E. Thompson et. al., “Electronic Devices and Systems, And Methods For Making and Using the Same,” US 2014/0077312 A1, 2014.

[52] S. E. Thompson et. al., “Process For Manufacturing Of Integrated Circuits With Differents Channel Doping Transistors Architectures and Devices Thereform,” US 8,877,619 B1, 2014.

[53] S. E. Thompson et. al., “Transistor Having Reduced Junction Leakage And Methods of Forming Thereof,” US 8,883,600 B1, 2014.

[54] S. E. Thompson et. al., “Process For Manufacturing An Improved Analog Transistor,” US 8,748,270 B1, 2014.

[55] S. E. Thompson et. al., “CMOS Gate Stack Structures And Processes,” US 8,735,987 B1, 2014.

[56] S. E. Thompson et. al., “Porting A Circuit Design From A First Semiconductor Process To A Second Semiconductor Process,” US 8,645,878 B1, 2014.

[57] S. E. Thompson et. al., “Multiple Transistor Types Formed In A Common Epitaxial Layer By Differential Out-Diffusion From A Doped Underlayer,” US 8,629,016 B1, 2014.

[58] S. E. Thompson et. al., “Cmos Structures And Processes Based On Selective Thinning,” US 8,614,128 B1, 2013.

[59] S. E. Thompson et. al., “Low Power Semiconductor Transistors Structure and Method of Fabrication Thereof,” US 8,530,286 B2, 2013.

[60] S. E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making And

Using The Same," US 2013/0020639 A1, 2013.

[61] S. E. Thompson et. al., "Semiconductor Devices Having Fin Structures and Fabrication Methods Thereof," WO2013022753A2, 2013.

[62] S. E. Thompson et. al., "Analog Circuits Having Improved Transistors, And Methods Therefor," US 8,400,219 B2, 2013.

[63] S. E. Thompson et. al., "Advanced Transistors With Punch Through Suppression," US 8,421,162 B2, 2013.

[64] S. E. Thompson et. al., "Digital Circuits Having Improved Transistors, And Methods Therefor," US 8,461,875 B1, 2013.

[65] L. T. Clark, D. Zhao, T. Bakhishev, H. Ahn, E. Boling, M. Duane, K. Fujita, P. Gregory, T. Hoffmann, M. Hori, D. Kanai, D. Kidd, S. Lee, Y. Liu, J. Mitani, J. Nagayama, S. Pradhan, P. Ranade, R. Rogenmoser, L. Scudder, L. Shifren, Y. Torii, M. Wojko, Y. Asada, T. Ema, and S. Thompson, "A highly integrated 65-nm SoC process with enhanced power/performance of digital and analog circuits," in 2012 International Electron Devices Meeting, 2012, p. 14.4.1-14.4.4.

[66] M. O. Baykan, S. E. Thompson, and T. Nishida, "Size- and Orientation-Dependent Strain Effects on Ballistic Si p-Type Nanowire Field-Effect Transistors," IEEE Trans. Nanotechnol., vol. 11, no. 6, pp. 1231–1238, Nov. 2012.

[67] S.E. Thompson et. al., "Electronic Devices And Systems, And Methods For Making And Using The Same," US 8,273,617 B2, 2012.

[68] S. E. Thompson et. al., "Analog Circuits Having Improved Transistors, and Methods Therefor," US 2012/024209 A1, 2012.

[69] S. E. Thompson et. al., "Electronic Devices And Systems, And Methods For Making and Using The Same," EP2483915A1, 2012.

[70] K. Fujita, Y. Torii, M. Hori, J. Oh, L. Shifren, P. Ranade, M. Nakagawa, K. Okabe, T. Miyake, K. Ohkoshi, M. Kuramae, T. Mori, T. Tsuruta, S. Thompson, and T. Ema, "Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications," in 2011 International Electron Devices Meeting, 2011, p. 32.3.1-32.3.4.

[71] C. D. Young and M. O. Baykan and A. Agrawal and H. Madan and K. Akarvardar and C. Hobbs and I. Ok and W. Taylor and C. E. Smith and M. M. Hussain and T. Nishida and S. Thompson and P. Majhi and P. Kirsch and S. Datta, "Critical discussion on (100) and (110) orientation dependent transport: nMOS planar and FinFET," in VLSI Technology (VLSIT), 2011 Symposium on, 2011, pp. 18–19.

[72] S. E. Thompson et. al., "Electronic Devices And Systems, And Methods For Making And Using The Same," WO2011062788A1, 2011.

[73] S. E. Thompson et. al., "CMOS Fabrication Process Utilizing Special Transistor Orientation," US 7,888,710 B2, 2011.

[74] S. E. Thompson et. al., "Electronic Devices And Systems, And Methods For Making And Using The Same," US 2011/0074498 A1, 2011.

[75] S. E. Thompson et. al., "Low Power Semiconductor Transistor Structure And Method Of Fabrication Thereof," US 2011/0248352 A1, 2011.

[76] S. E. Thompson et. al., “Transistor With Threshold Voltage Set Notch And Method Of Fabrication Thereof,” US 2011/0309447 A1, 2011.

[77] S. E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making And Using The Same,” WO2011041109A1, 2011.

[78] D. J. Cummings, H. Park, S. E. Thompson, and M. E. Law, “An Adaptive Grid Scheme for Single-Event Upset Device Simulations,” IEEE Trans. Nucl. Sci., Dec. 2010.

[79] D. J. Cummings, A. F. Witulski, H. Park, R. D. Schrimpf, S. E. Thompson, and M. E. Law, “Mobility Modeling Considerations for Radiation Effects Simulations in Silicon,” IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 2318–2326, Aug. 2010.

[80] A. D. Koehler, A. Gupta, Min Chu, S. Parthasarathy, K. J. Linthicum, J. W. Johnson, T. Nishida, and S. E. Thompson, “Extraction of AlGaN/GaN HEMT Gauge Factor in the Presence of Traps,” IEEE Electron Device Lett., vol. 31, no. 7, pp. 665–667, Jul. 2010.

[81] S. E. Thompson, “Power, cost and circuit IP reuse: The real limiter to Moore’s Law over the next 10 years,” in Proceedings of 2010 International Symposium on VLSI Technology, System and Application, 2010, pp. 88–89.

[82] S. E. Thompson et. al., “Methods And Articles Incorporating Local Stress For Performanc Improvement of Strained Semiconductor Devices,” US 7,723,720 B2, 2010.

[83] H. Park, D. J. Cummings, R. Arora, J. A. Pellish, R. A. Reed, R. D. Schrimpf, D. McMorrow, S. E. Armstrong, U. Roh, T. Nishida, M. E. Law, and S. E. Thompson, “Laser-Induced Current Transients in Strained-Si Diodes,” IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3203–3209, Dec. 2009.

[84] U. Aghoram, J. Liu, M. Chu, A. D. Koehler, S. E. Thompson, S. Sridhar, R. Wise, S. Pendharkar, and M. Denison, “Effect of mechanical stress on LDMOSFETs: Dependence on orientation and gate bias,” in 2009 21st International Symposium on Power Semiconductor Devices & IC’s, 2009, pp. 220–223.

[85] Zhichao Lu, J. G. Fossum, Ji-Woon Yang, H. R. Harris, V. P. Trivedi, Min Chu, and S. E. Thompson, “A Simplified Superior Floating-Body/Gate DRAM Cell,” IEEE Electron Device Lett., vol. 30, no. 3, pp. 282–284, Mar. 2009.

[86] Y. Sun, S. E. Thompson, and T. Nishida, Strain Effect in Semiconductors: Theory and Device Applications. Springer Science, 2009.

[87] S. E. Thompson et. al., “Methods and Articles Incorporating Local Stress For Performance Improvement of Strained Semiconductor Devices,” US 2009/0072371 A1, 2009.

[88] Y. S. Choi, T. Numata, T. Nishida, R. Harris, and S. E. Thompson, “Impact of mechanical stress on gate tunneling currents of germanium and silicon p -type metal-oxide-semiconductor field-effect transistors and metal gate work function,” J. Appl. Phys., vol. 103, no. 6, pp. 1–6, 2008.

[89] H. Park, S. K. Dixit, Y. S. Choi, R. D. Schrimpf, D. M. Fleetwood, T. Nishida, and S. E. Thompson, “Total Ionizing Dose Effects on Strained HfO2 -Based nMOSFETs,” IEEE Trans. Nucl. Sci., vol. 55, no. 6, pp. 2981–2985, Dec. 2008.

[90] S. Suthram, Y. Sun, P. Majhi, I. Ok, H. Kim, H. R. Harris, N. Goel, S. Parthasarathy, A. Koehler, T. Acosta, T. Nishida, H.-H. Tseng, W. Tsai, J. Lee, R. Jammy, and S. E. Thompson,

"Strain additivity in III-V channels for CMOSFETs beyond 22nm technology node," in 2008 Symposium on VLSI Technology, 2008, pp. 182–183.

[91] S. Suthram, H. R. Harris, M. M. Hussain, C. Smith, C. D. Young, J.-W. Yang, K. Mathews, K. Freeman, P. Majhi, H. H.-H. Tseng, R. Jammy, and S. E. Thompson, "Understanding Strain Effects on Double-Gate FinFET Drive-Current Enhancement, Hot-Carrier Reliability and Ring-Oscillator Delay Performance via Uniaxial Wafer Bending Experiments," in 2008 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2008, pp. 163–164.

[92] S. Suthram, M. M. Hussain, H. R. Harris, C. Smith, H.-H. Cheng, R. Jammy, and S. E. Thompson, "Comparison of Uniaxial Wafer Bending and Contact-Etch-Stop-Liner Stress Induced Performance Enhancement on Double-Gate FinFETs," IEEE Electron Device Lett., vol. 29, no. 5, pp. 480–482, May 2008.

[93] A. M. Noori, M. Balseanu, P. Boelen, A. Cockburn, S. Demuynck, S. Felch, S. Gandikota, A. J. Gelatos, A. Khandelwal, J. A. Kittl, A. Lauwers, W.-C. Lee, J. Lei, T. Mandrekar, R. Schreutelkamp, K. Shah, S. E. Thompson, P. Verheyen, C.-Y. Wang, L.-Q. Xia, and R. Arghavani, "Manufacturable Processes for < 32-nm-node CMOS Enhancement by Synchronous Optimization of Strain-Engineered Channel and External Parasitic Resistances," IEEE Trans. Electron Devices, vol. 55, no. 5, pp. 1259–1264, May 2008.

[94] Y. S. Choi, T. Numata, T. Nishida, R. Harris, and S. E. Thompson, "Impact of mechanical stress on gate tunneling currents of germanium and silicon p -type metal-oxide-semiconductor field-effect transistors and metal gate work function," J. Appl. Phys., vol. 103, no. 6, pp. 1–6, 2008.

[95] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," J. Appl. Phys., vol. 102, no. 8, pp. 1–7, 2007.

[96] R. Arghavani, H. M'Saad, E. Yieh, G. Miner, S. Kuppurao, and S. Thompson, "Strain engineering push to the 32nm logic technology node," London, UK Semicond. Fabtech, pp. 2–6, 2007.

[97] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si/Si," Appl. Phys., no. figure 5, pp. 727–730, 2007.

[98] H. R. Harris, P. Kalra, P. Majhi, M. Hussain, D. Kelly, J. Oh, D. He, C. Smith, J. Barnett, P. D. Kirsch, G. Gebara, J. Jur, D. Lichtenwalner, A. Lubow, T. P. Ma, G. Sung, S. Thompson, B. H. Lee, H. H. Tseng, and R. Jammy, "Band-engineered low PMOS vT with high-K/metal gates featured in a dual channel CMOS integration scheme," Dig. Tech. Pap. - Symp. VLSI Technol., pp. 154–155, 2007.

[99] R. A. R. Arghavani, N. D. N. Derhacobian, V. B. V Banthia, M. B. M. Balseanu, N. I. N. Ingle, H. Ms. H. MSaad, S. V. S. Venkataraman, E. Y. E. Yieh, Z. Y. Z. Yuan, L. Q. X. L. Q. Xia, Z. K. Z. Krivokapic, U. A. U. Aghoram, K. M. K. MacWilliams, and S. E. T. S. E. Thompson, "Strain Engineering to Improve Data Retention Time in Nonvolatile Memory," IEEE Trans. Electron Devices, vol. 54, no. 2, pp. 362–365, 2007.

[100] S. Suthram, J. C. Ziegert, T. Nishida, and S. E. Thompson, "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (~1.5 GPa) channel stress," IEEE Electron Device Lett., vol. 28, no. 1, pp. 58–61, 2007.

[101] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si / Si 1-x Ge x / Si Quantum Wells with High- k / Metal Gate Stacks and Additive Uniaxial Strain for 22 nm Technology Node," pp. 727–730, 2007.

[102] Y. Sun, S. E. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors," J. Appl. Phys., vol. 101, no. 10, pp. 1–22, 2007.

[103] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," J. Appl. Phys., vol. 102, no. 8, pp. 1–8, 2007.

[104] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si/Si1-xGex/Si Quantum Wells with High-k/Metal Gate Stacks and Additive Uniaxial Strain for 22 nm Technology Node," in 2007 IEEE International Electron Devices Meeting, 2007, pp. 727–730.

[105] X. Yang, Y. Choi, T. Nishida, and S. E. Thompson, "Gate Direct Tunneling Currents in Uniaxial Stressed MOSFETs," in 2007 International Workshop on Electron Devices and Semiconductor Technology (EDST), 2007, pp. 149–152.

[106] H. R. Harris, S. E. Thompson, S. Krishnan, P. Kirsch, P. Majhi, C. E. Smith, M. M. Hussain, G. Sun, H. Adhikari, S. Suthram, B. H. Lee, H.-H. Tseng, and R. Jammy, "Flexible, simplified CMOS on Si(110) with metal gate / high k for HP and LSTP," in 2007 IEEE International Electron Devices Meeting, 2007, pp. 57–60.

[107] R. Arghavani, H. M'Saad, E. Yieh, G. Miner, S. Kuppurao, and S. Thompson, "Strain engineering push to the 32nm logic technology node," London, UK Semicond. Fabtech, pp. 2–6, 2007.

[108] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," J. Appl. Phys., vol. 102, no. 8, pp. 1–8, 2007.

[109] S. Suthram, J. C. Ziegert, T. Nishida, and S. E. Thompson, "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (~1.5 GPa) channel stress," IEEE Electron Device Lett., vol. 28, no. 1, pp. 58–61, 2007.

[110] H. R. Harris, P. Kalra, P. Majhi, M. Hussain, D. Kelly, J. Oh, D. He, C. Smith, J. Barnett, P. D. Kirsch, G. Gebara, J. Jur, D. Lichtenwalner, A. Lubow, T. P. Ma, G. Sung, S. Thompson, B. H. Lee, H. H. Tseng, and R. Jammy, "Band-engineered low PMOS vT with high-K/metal gates featured in a dual channel CMOS integration scheme," Dig. Tech. Pap. - Symp. VLSI Technol., pp. 154–155, 2007.

[111] R. A. R. Arghavani, N. D. N. Derhacobian, V. B. V Banthia, M. B. M. Balseanu, N. I. N. Ingle, H. Ms. H. MSaad, S. V. S. Venkataraman, E. Y. E. Yieh, Z. Y. Z. Yuan, L. Q. X. L. Q. Xia, Z. K. Z. Krivokapic, U. A. U. Aghoram, K. M. K. MacWilliams, and S. E. T. S. E. Thompson, "Strain Engineering to Improve Data Retention Time in Nonvolatile Memory," IEEE Trans. Electron Devices, vol. 54, no. 2, pp. 362–365, 2007.

[112] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," J. Appl. Phys., vol. 102, no. 8, pp. 1–7, 2007.

[113] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si/Si," Appl. Phys., no. figure 5, pp. 727–730, 2007.

[114] Y. Sun, S. E. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors," J. Appl. Phys., vol. 101, no. 10, pp. 1–22, 2007.

[115] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced Strained-Si: Extending the CMOS roadmap," IEEE Trans. Electron Devices, vol. 53, no. 5, pp. 1010–1020, 2006.

[116] S. E. Thompson and S. Parthasarathy, "Moore's law: the future of Si microelectronics," Mater. Today, vol. 9, no. 6, pp. 20–25, 2006.

[117] S. E. Thompson, S. Suthram, Y. Sun, G. Sun, S. Parthasarathy, M. Chu, and T. Nishida, "Future of Strained Si / Semiconductors in Nanoscale MOSFETs," Iedm, pp. 8–11, 2006.

[118] X. Yang, J. Lim, G. Sun, K. Wu, T. Nishida, and S. E. Thompson, "Strain-induced changes in the gate tunneling currents in p-channel metal-oxide-semiconductor field-effect transistors," Appl. Phys. Lett., vol. 88, no. 5, pp. 1–3, 2006.

[119] S. A. Krishnan, H. R. Harris, P. D. Kirsch, C. Krug, M. Quevedo-lopez, C. Young, H. Lee, R. Choi, N. Chowdhury, S. Suthram, S. Thompson, G. Bersuker, and R. Jammy, "High Performing pMOSFETs on Si (110) for Application to Hybrid Orientation Technologies – Comparison of HfO 2 and HfSiON," IEEE Electron Devices Meet., no. 110, pp. 8–11, 2006.

[120] Y. Sun, G. Sun, S. Parthasarathy, and S. E. Thompson, "Physics of process induced uniaxially strained Si," Mater. Sci. Eng. B Solid-State Mater. Adv. Technol., vol. 135, no. 3, pp. 179–183, 2006.

[121] S. E. Thompson, "Industry Examples at the State-of-the-Art: Intel's 90nm Logic Technologies," in Silicon heterostructure handbook : materials, fabrication, devices, circuits, and applications of SiGe and Si strained-layer epitaxy, CRC Taylor & Francis, 2006.

[122] S. E. Thompson, "Uniaxial Stressed Si MOSFET," in Silicon heterostructure handbook : materials, fabrication, devices, circuits, and applications of SiGe and Si strained-layer epitaxy, CRC Taylor & Francis, 2006.

[123] J.-S. Lim, X. Yang, T. Nishida, and S. E. Thompson, "Measurement of conduction band deformation potential constants using gate direct tunneling current in n-type metal oxide semiconductor field effect transistors under mechanical stress," Appl. Phys. Lett., vol. 89, no. 7, p. 73509, 2006.

[124] S. Thompson and G. Sun, "Strained Si and the Future Direction of CMOS," in 2006 International Symposium on VLSI Technology, Systems, and Applications, 2006, pp. 1–2.

[125] R. Arghavani, L. Xia, H. M'Saad, M. Balseanu, G. Karunasiri, A. Mascarenhas, and S. E. Thompson, "A reliable and manufacturable method to induce a stress of > 1 GPa on a P-channel MOSFET in high volume manufacturing," IEEE Electron Device Lett., vol. 27, no. 2, pp. 114–116, Feb. 2006.

[126] S. A. Krishnan, H. R. Harris, P. D. Kirsch, C. Krug, M. Quevedo-Lopez, C. Young, B. H. Lee, R. Choi, N. Chowdhury, S. Suthram, S. Thompson, G. Bersuker, and R. Jammy, "High

Performing pMOSFETs on Si(110) for Application to Hybrid Orientation Technologies -- Comparison of HfO2 and HfSiON," in 2006 International Electron Devices Meeting, 2006, pp. 1–4.

[127] I. Polishchuk, S. Levy, R. Kapre, O. Pohland, K. Ramkumar, N. Shah, and S. Thompson, "A Low-Cost Strained Silicon SRAM Technology with Reduced Contact Resistance," in 2006 64th Device Research Conference, 2006, pp. 263–264.

[128] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced Strained-Si: Extending the CMOS roadmap," IEEE Trans. Electron Devices, vol. 53, no. 5, pp. 1010–1020, 2006.

[129] S. E. Thompson and S. Parthasarathy, "Moore's law: the future of Si microelectronics," Mater. Today, vol. 9, no. 6, pp. 20–25, 2006.

[130] S. E. Thompson, S. Suthram, Y. Sun, G. Sun, S. Parthasarathy, M. Chu, and T. Nishida, "Future of Strained Si / Semiconductors in Nanoscale MOSFETs," Iedm, pp. 8–11, 2006.

[131] X. Yang, J. Lim, G. Sun, K. Wu, T. Nishida, and S. E. Thompson, "Strain-induced changes in the gate tunneling currents in p-channel metal-oxide-semiconductor field-effect transistors," Appl. Phys. Lett., vol. 88, no. 5, pp. 1–3, 2006.

[132] Y. Sun, G. Sun, S. Parthasarathy, and S. E. Thompson, "Physics of process induced uniaxially strained Si," Mater. Sci. Eng. B Solid-State Mater. Adv. Technol., vol. 135, no. 3, pp. 179–183, 2006.

[133] N. Mohta and S. E. Thompson, "Mobility enhancement," IEEE Circuits Devices Mag., vol. 21, no. 5, pp. 18–23, 2005.

[134] S. E. Thompson, R. S. Chau, T. Ghani, K. Mistry, S. Tyagi, and M. T. Bohr, "In search of 'forever,' continued transistor scaling one new material at a time," IEEE Trans. Semicond. Manuf., vol. 18, no. 1, pp. 26–35, 2005.

[135] S. E. Thompson, "Strained Si and the future direction of CMOS," in Fifth International Workshop on System-on-Chip for Real-Time Applications (IWSOC'05), 2005, pp. 14–16.

[136] S. E. Thompson, R. S. Chau, T. Ghani, K. Mistry, S. Tyagi, and M. T. Bohr, "In search of 'forever,' continued transistor scaling one new material at a time," IEEE Trans. Semicond. Manuf., vol. 18, no. 1, pp. 26–35, 2005.

[137] N. Mohta and S. E. Thompson, "Mobility enhancement," IEEE Circuits Devices Mag., vol. 21, no. 5, pp. 18–23, 2005.

[138] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key Differences For Process-induced Uniaxial vs . Substrate-induced Biaxial Stressed Si and Ge Channel MOSFETs," IEEE Electron Devices Meet., pp. 221–224, 2004.

[139] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained-silicon," IEEE Electron Device Lett., vol. 25, no. 4, pp. 191–193, 2004.

[140] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L.

Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, “A 90-nm logic technology featuring strained-silicon,” IEEE Trans. Electron Devices, vol. 51, no. 11, pp. 1790–1797, 2004.

[141] J. S. Lim, S. E. Thompson, and J. G. Fossum, “Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs,” IEEE Electron Device Lett., vol. 25, no. 11, pp. 731–733, 2004.

[142] C. H. Jan, N. Anand, C. Allen, J. Bielefeld, M. Buehler, V. Chikamane, K. Fischer, K. Jain, J. Jeong, S. Klopcic, T. Marieb, B. Miner, P. Nguyen, A. Schmitz, M. Nashner, T. Scherban, B. Schroeder, C. Ward, R. Wu, K. Zawadzki, S. Thompson, and M. Bohr, “A 90nm high volume manufacturing logic technology featuring Cu metallization and CDO low-k ILD interconnects on 300 mm wafers,” in Proceedings of the IEEE 2004 International Interconnect Technology Conference (IEEE Cat. No.04TH8729), 2004, pp. 205–207.

[143] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, “Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs,” in IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004., 2004, pp. 221–224.

[144] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson, and M. Bohr, “Delaying forever: Uniaxial strained silicon transistors in a 90nm CMOS technology,” in Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004., 2004, pp. 50–51.

[145] Scott. E. Thompson et. al., “Nitrogen Controlled Growth of Dislocations Loop In Stress Enhanced Transistors,” US 2004/0191975 A1, 2004.

[146] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, “A 90-nm logic technology featuring strained-silicon,” IEEE Trans. Electron Devices, vol. 51, no. 11, pp. 1790–1797, 2004.

[147] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, “A logic nanotechnology featuring strained-silicon,” IEEE Electron Device Lett., vol. 25, no. 4, pp. 191–193, 2004.

[148] J. S. Lim, S. E. Thompson, and J. G. Fossum, “Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs,” IEEE Electron Device Lett., vol. 25, no. 11, pp. 731–733, 2004.

[149] Scott. E. Thompson et. al., “Nitrogen Controlled Growth of Dislocations Loop In Stress Enhanced Transistors.” 2004.

[150] K. Zhang, U. Bhattacharya, L. Ma, Y. Ng, B. Zheng, M. Bohr, and S. Thompson, “A fully synchronized, pipelined, and re-configurable 50 Mb SRAM on 90 nm CMOS technology for logic applications,” in 2003 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No.03CH37408), 2003, pp. 253–254.

[151] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, “A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS

transistors," in IEEE International Electron Devices Meeting 2003, 2003, p. 11.6.1-11.6.3.

[152] S. E. Thompson et. al., "Structure and Process Flow For Fabrication of Dual Gate Floating Body Integrated MOS Transistors," US 6,624,032 B2, 2003.

[153] S. E. Thompson et. al., "Structure and Process Flow For Fabrication of Dual Gate Floating Body Integrated MOS Transistors." 2003.

[154] S. Vangal, M. A. Anders, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, J. W. Tschanz, Y. Ye, D. Somasekhar, B. A. Bloechel, G. E. Dermer, R. K. Krishnamurthy, K. Soumyanath, S. Mathew, S. G. Narendra, M. R. Stan, S. Thompson, V. De, and S. Borkar, "5-GHz 32-bit integer execution core in 130-nm dual-V/sub T/ CMOS," IEEE J. Solid-State Circuits, vol. 37, no. 11, pp. 1421–1432, Nov. 2002.

[155] M. Anders, S. Mathew, B. Bloechel, S. Thompson, R. Krishnamurthy, K. Soumyanath, and S. Borkar, "A 6.5GHz 130nm single-ended dynamic ALU and instruction scheduler loop," in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 2, pp. 332–534.

[156] M. Anders, S. Mathew, B. Bloechel, S. Thompson, R. Krishnamurthy, K. Soumyanath, and S. Borkar, "A 6.5 GHz 130 nm single-ended dynamic ALU and instruction-scheduler loop," in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 1, pp. 410–477.

[157] S. Vangal, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, M. Anders, J. Tschanz, Y. Ye, D. Somasekhar, B. Bloechel, G. Dermer, R. Krishnamurthy, S. Narendra, M. Stan, S. Thompson, V. De, and S. Borkar, "5GHz 32b integer-execution core in 130nm dual-V/sub T/ CMOS," in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 2, pp. 334–535.

[158] S. Vangal, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, M. Anders, J. Tschanz, Y. Ye, D. Somasekhar, B. Bloechel, G. Dermer, R. Krishnamurthy, S. Narendra, M. Stan, S. Thompson, V. De, and S. Borkar, "A 25 GHz 32 b integer-execution core in 130 nm dual-V/sub T/ CMOS," in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 1, pp. 412–478.

[159] S. E. Thompson et. al., "CMOS Fabrication Process Utilizing Special Transistor Orientation," US 2002/0063292 A1, 2002.

[160] T. Ghani, K. Mistry, P. Packan, M. Armstrong, S. Thompson, S. Tyagi, and M. Bohr, "Asymmetric source/drain extension transistor structure for high performance sub-50 nm gate length CMOS devices," in 2001 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.01 CH37184), 2001, pp. 17–18.

[161] S. Thompson, M. Alavi, R. Arghavani, A. Brand, R. Bigwood, J. Brandenburg, B. Crew, V. Dubin, M. Hussein, P. Jacob, C. Kenyon, E. Lee, B. Mcintyre, Z. Ma, P. Moon, P. Nguyen, M. Prince, R. Schweinfurth, S. Sivakumar, P. Smith, M. Stettler, S. Tyagi, M. Wei, J. Xu, S. Yang, and M. Bohr, "An enhanced 130 nm generation logic technology featuring 60 nm transistors optimized for high performance and low power at 0.7 - 1.4 V," in International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224), 2001, p. 11.6.1-11.6.4.

[162] Scott. E. Thompson et. al., "Method Of Fabricating A Supply Decoupling Capacitor," US

2001/0009785 A1, 2001.

[163] S. E. Thompson et. al., “Integrated Circuit With Borderless Contacts,” US 6,228,777 B1, 2001.

[164] K. Mistry, T. Ghani, M. Armstrong, S. Tyagi, P. Packan, S. Thompson, S. Yu, and M. Bohr, “Scalability revisited: 100 nm PD-SOI transistors and implications for 50 nm devices,” in 2000 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.00CH37104), 2000, pp. 204–205.

[165] S. Tyagi, M. Alavi, R. Bigwood, T. Bramblett, J. Brandenburg, W. Chen, B. Crew, M. Hussein, P. Jacob, C. Kenyon, C. Lo, B. McIntyre, Z. Ma, P. Moon, P. Nguyen, L. Rumaner, R. Schweinfurth, S. Sivakumar, M. Stettler, S. Thompson, B. Tufts, J. Xu, S. Yang, and M. Bohr, “A 130 nm generation logic technology featuring 70 nm transistors, dual Vt transistors and 6 layers of Cu interconnects,” in International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138), 2000, pp. 567–570.

[166] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, “Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors,” in 2000 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.00CH37104), 2000, pp. 174–175.

[167] S. E. Thompson et. al., “Channel Dopant Implantation With Automatic Compensation For Variation in Critical Dimensions,” US 6,020,244, 2000.

[168] S. E. Thompson et. al., “Process For Forming Doped Regions From Solid Phase Diffusion Source,” US 5,877,072, 1999.

[169] S. E. Thompson et. al., “Low Damage Doping Technique For Self-Aligned Source And Drain Regions,” US 5,976,939, 1999.

[170] S. E. Thompson et. al., “Two Step Source/Drain Anneal To Prevent Dopant Evaporation,” US 5,874,344, 1999.

[171] S. Thompson, P. Packan, T. Ghani, M. Stettler, M. Alavi, I. Post, S. Tyagi, S. Ahmed, S. Yang, and M. Bohr, “Source/drain extension scaling for 0.1 μm and below channel length MOSFETs,” in 1998 Symposium on VLSI Technology Digest of Technical Papers (Cat. No.98CH36216), 1998, pp. 132–133.

[172] P. Packan, S. Thompson, E. Andideh, S. Yu, T. Ghani, M. Giles, J. Sandford, and M. Bohr, “Modeling solid source boron diffusion for advanced transistor applications,” in International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), 1998, pp. 505–508.

[173] Thompson, Young, Greason, and Bohr, “Dual Threshold Voltages And Substrate Bias: Keys To High Performance, Low Power, 0.1 /spl mu/m Logic Designs,” in Symposium on VLSI Technology, 1997, pp. 69–70.

[174] P. Packan, H. Kennel, S. Thompson, S. Corcoran, and M. Taylor, “Understanding implant damage by implant channeling profile measurements,” in Proceedings of 11th International Conference on Ion Implantation Technology, 1996, pp. 539–542.

[175] S. E. Thompson, P. A. Packan, and M. T. Bohr, “Linear versus saturated drive current: tradeoffs in super steep retrograde well engineering,” in 1996 Symposium on VLSI Technology. Digest of Technical Papers, 1996, pp. 154–155.

[176] M. Bohr, S. S. Ahmed, S. U. Ahmed, M. Bost, T. Ghani, J. Greason, R. Hainsey, C. Jan, P. Packan, S. Sivakumar, S. Thompson, J. Tsai, and S. Yang, "A high performance 0.25 μm logic technology optimized for 1.8 V operation," in International Electron Devices Meeting. Technical Digest, 1996, pp. 847–850.

[177] M. Bohr, S. U. Ahmed, L. Brigham, R. Chau, R. Gasser, R. Green, W. Hargrove, E. Lee, R. Natter, S. Thompson, K. Weldon, and S. Yang, "A high performance 0.35 μm logic technology for 3.3 V and 2.5 V operation," in Proceedings of 1994 IEEE International Electron Devices Meeting, 1994, pp. 273–276.

[178] T. Nishida, S. E. Thompson, J. T. Kavalieros, Y. Lu, and M. K. Han, "Characterization of ULSI gate oxide reliability using substrate and channel electron injection stresses," in Proceedings Ninth Biennial University/Government/Industry Microelectronics Symposium, 1991, pp. 84–88.

[179] T. Nishida and S. E. Thompson, "Oxide field and temperature dependences of gate oxide degradation by substrate hot electron injection," in 29th Annual Proceedings Reliability Physics 1991, 1991, pp. 310–315.

[180] S. E. Thompson and F. A. Lindholm, "Influence of heavily doped contacts on photoconductive switch properties," IEEE Trans. Electron Devices, vol. 37, no. 12, pp. 2542–2553, 1990.

[181] *Strain Effects in Semiconductors: Theory and Device Applications,* S. Yongke, S.E. Thompson, and T. Nishida, Springer US, ISBN 978-1-4419-0551-2