

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner

v.

BiTMICRO LLC,

Patent Owner.

IPR 2023-00781

U.S. Patent No. 7,826,243

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,826,243**

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EXHIBIT LIST

Exhibit	Reference
1001	U.S. Patent No. 7,826,243 (“the ’243 patent”)
1002	File History of the ’243 patent
1003	Declaration of Dr. Scott Thompson in Support of Petition
1004	Curriculum Vitae of Dr. Scott Thompson
1005	Certificate of Correction for the ’243 patent
1006	Excerpt of the ’243 patent with Certificate of Correction language
1007	U.S. Patent Publication 2001/0028114 to Hosomi (“Hosomi”)
1008	International Publication No. WO 2004/072667
1009	Certified Translation of WO 2004/072667 (“Sato”)
1010	U.S. Patent Publication 2003/0178228 to Sung et al. (“Sung”)
1011	U.S. Patent 6,791,193 to Watanabe et al. (“Watanabe”)
1012	C. Maxfield, <i>Bebop to the Boolean Boogie</i> (2d. ed. 2003) (“Maxfield”)
1013	G. Blackwell, <i>The Electronic Packaging Handbook</i> (IEEE Press 2000) (“Blackwell”)
1014	K. Gilleo, <i>Area Array Packaging Handbook: Manufacturing and Assembly</i> (McGraw-Hill 2002) (“Gilleo”)
1015	S. Thompson et al., Moore’s law; the future of Si microelectronics, 22 (Materials Today, vol. 9, No. 6, June 2006) (“Thompson”)
1016	I. Elfadel, et al., 3D Stacked Chips: From Emerging Processes to Heterogeneous Systems, (Springer Int’l Publishing Switzerland 2016) (“Elfadel”)
1017	K. Sasidhar, <i>Parallel Test Techniques for Multi-chip Modules</i> (Doctoral Thesis, Georgia Institute of Technology, Aug. 1997) (“Sasidhar”)
1018	K. Satish, Tutorial on Design for Testability (DFT): An ASIC Design Philosophy for testability from Chips to Systems, (IEEE

Exhibit	Reference
	1993) (“Satish”)
1019	J. Huber et al., Successful ASIC Design the First Time Through, 160 (Van Nostrand Reinhold 1991) (“Huber”)
1020	IEEE Standard 1149.1-1990
1021	www.jtag.com/what-is-jtag-boundary-scan (www.jtag.com)
1022	K. Sasidhar et al., <i>Testing NASA’s 3D-Stack MCM Space Flight Computer</i> , (IEEE 1998) (“NASA”)
1023	C. Maunder et al., An Introduction to the Boundary Scan Standard: ANSI/IEEE Std 1149.1, 28 (Journal of Electronic Testing 1991) (“Maunder”)
1024	Hennessy and Patterson, <i>Computer Architecture: A Quantitative Approach</i> (4th ed. 2006) (“Hennessy and Patterson”)
1025	Summons and Proof of Service, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 9
1026	Defendants’ Opening Claim Construction Brief, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 33
1027	United States District Court – National Judicial Caseload Profile

I. INTRODUCTION

Intel Corporation (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1, 2, 11, and 12 of U.S. Patent 7,826,243 (“the ’243 patent”; INTEL-1001).

II. GROUNDS FOR STANDING

Petitioner certifies the ’243 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR. (*See*, INTEL-1025.)

III. IDENTIFICATION OF CHALLENGE

A. Prior Art

Each applied reference, listed below, was published before the filing date of the ’243 patent (December 29, 2005).

1. **U.S. Patent Publication 2001/0028114 to Hosomi** (“Hosomi”; INTEL-1007), published October 11, 2001, is prior art under §102(b).
2. **International Publication WO 2004/072667 to Sato** (INTEL-1008), published August 26, 2004, is prior art under §102(b). A certified translation is provided as INTEL-1009 (“Sato”).
3. **U.S. Patent Publication 2003/0178228 to Sung et al.** (“Sung”; INTEL-1010), published September 25, 2003, is prior art under §102(b).
4. **U.S. Patent 6,791,193 to Watanabe et al.**, (“Watanabe”; INTEL-1011), issued September 14, 2004, is prior art under §102(b).

B. Grounds For Challenge

Ground		Claims	
1	103	1, 2, 11, and 12	Hosomi and Sato
2	103	1, 2, 11, and 12	Sung and Watanabe

IV. '243 PATENT OVERVIEW

The '243 patent relates to a multiple chip module (MCM) and Package Stacking technique. (INTEL-1001, 1:10–12.) The '243 patent uses identical single or multichip modules for each stack layer. (INTEL-1001, 4:17-18 (“single and multiple chip modules are created to become the basic building blocks for the stacking technique”), 9:6-7 (“All SDRAM modules are identical”), 9:32-38, 10:5-8.) An exemplary SDRAM module, illustrated in Figures 2a-b below, includes one or more SDRAM dies “placed in a single substrate.” (INTEL-1001, 4:20-21.)

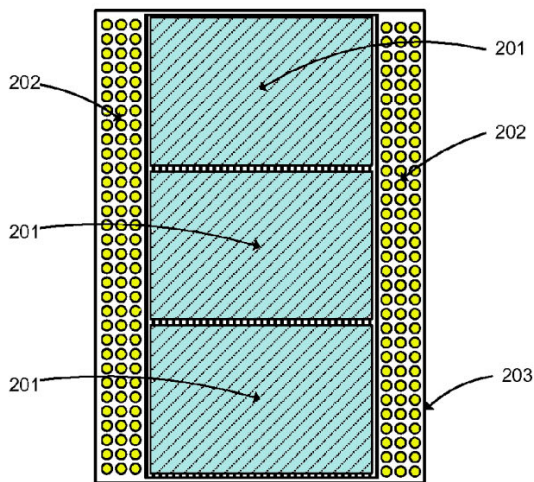


Figure 2a

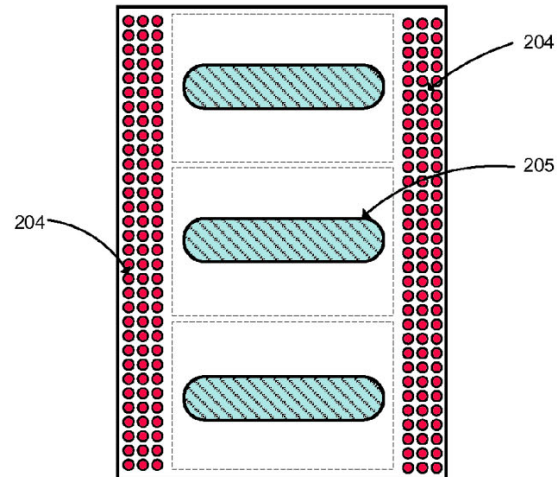


Figure 2b

'243 Patent, Annotated Figure 2a (Top View), Figure 2b (Bottom View)

The '243 patent acknowledges stacking components was known, noting its embodiments “take[] advantage of the existing stacking technology both on the module and package level.” (INTEL-1001, 1:59-60.) As shown in Figure 2c, when stacked, “[t]op pads 202 and bottom balls 204 act as the vertical interconnects between all SDRAM modules”. (INTEL-1001, 4:32-34.)

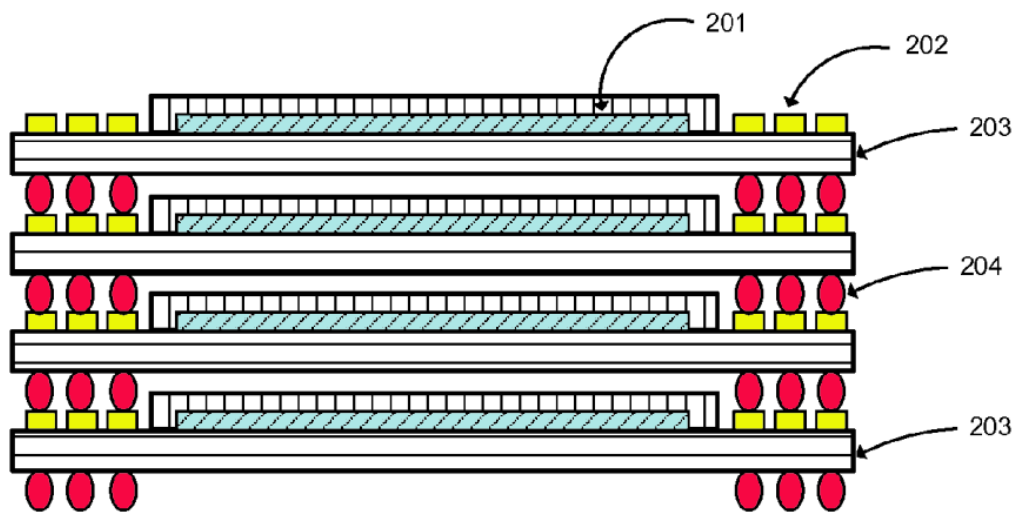
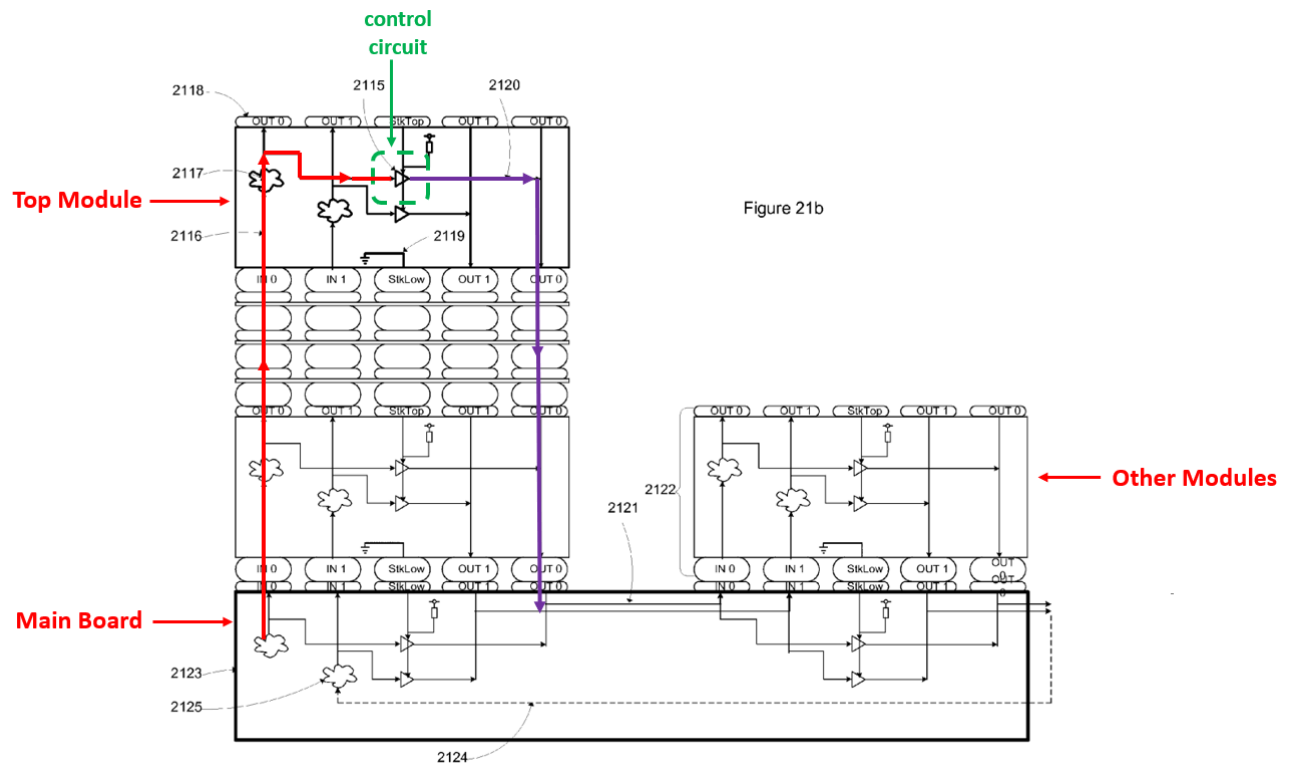


Figure 2c

'243 Patent, Annotated Figure 2c (Cross-Sectional View)

The embodiment of Figures 21b is the only embodiment having the claimed “serial chain routes” coupled by a “control circuit” in an end module. (See INTEL-1001, 9:67-10:10; INTEL-1005, 1-3.) The specific routing path is, for example, a “JTAG TDI-TDO signal” path. (INTEL-1001, 10:32-33.) Long before the '243 patent, JTAG (“Joint Test Action Group”) boundary scan testing was a standardized testing methodology widely used for all types of electronics. (See

INTEL-1003, ¶¶53-58.) Indeed, chips were designed (and are still) to incorporate testing functionality using this standard. (INTEL-1003, ¶¶55, 57-58.)



'243 Patent, Annotated Figure 21b

A. Prosecution History

Early in prosecution, Applicant sought a broad claim directed simply to a “stacked module” with active and passive ports. (INTEL-1002, 471.) The Examiner rejected this claim as anticipated and further found the passive port, daisy-chain input/output port and passive ball/pad limitations of the claims indefinite. (INTEL-1002, 449-456.) In response, Applicant made extensive

amendments to the specification adding over **40 lines** of new matter to the discussion of Figures 19-21. (*See* INTEL-1002, 403-408; INTEL-1005, 1-3; INTEL-1006.) Applicant characterized these amendments as “clerical” in nature, merely “correct[ing] **minor errors**¹ noted in the Office Action” and amended the claims to recite this new matter. (*See* INTEL-1002, 423; 414-419.)

The Examiner accepted the amendments and allowed the claims, finding a limitation based on the added matter, directed to connecting serial chain routes using a control circuit, patentable over the applied prior art. (INTEL-1002, 388.) However, the concept of connecting two routing paths using a control circuit was well-known in the prior art, as Petitioner establishes herein.

B. Level Of Ordinary Skill In The Art

A person of ordinary skill in the art (“POSITA”) at the time of the purported invention would have had (1) a bachelor’s degree in electrical engineering or similar discipline, and two to three years of work experience in semiconductor packaging or (2) a master’s degree with one or more years of experience in those fields. (INTEL-1003, ¶68.)

¹ Unless otherwise noted, all emphasis by bold added.

C. Claim Construction

The terms “*plurality of modules each comprising*”² and “*passive port*” require construction in this proceeding. Petitioner applies the plain and ordinary meaning for all other terms.

1. “*a plurality of modules each comprising*” [1A]

The term “*a plurality of modules each comprising*” is not part of the preamble and should be construed as “each module in the stacked module comprising.” Patent Owner (“PO”) contends in a co-pending litigation this term is “part of the preamble and not a limitation of the claim.” (INTEL-1026, 15-18.)

Claim 1 recites “*A stacked module comprising a plurality of modules each comprising:*” In this claim, “[*a*] stacked module comprising” is the claim’s preamble. The “*plurality of modules*” language follows this preamble and therefore should be considered as part of the body of the claim. *See Nichia Corp. v. Document Sec. Sys., Inc.*, No. 2020-2261, 2022 WL 1218036, *4 (Fed. Cir. Apr. 26, 2022)

Petitioner’s construction, requiring the modifier “*each*” to apply to the modules in the “*plurality of modules*” is consistent with the specification which repeatedly describes a stacked module as having multiple **identical** modules. (*See*,

² Claim language is indicated throughout with italics.

e.g., INTEL-1001, 9:6-8 (as amended by COC) (“All SDRAM modules are identical”), INTEL-1005, 1; *see also*, INTEL-1001, 3:29-33 (“FIG. 20a shows ... a rotational stacking orientation to allow stacking of **four identical modules**”; 9:32-38.) Moreover, the sole claimed embodiment shown in Figure 21 **requires** identical stacked modules. (INTEL-1001, 10:5-8 (“Since **the modules are identical**, [a] routed signal [can be] passe[d] through”).)

But even if it is determined this term is part of the preamble, Petitioner’s construction still applies because the body of the claim depends on it for antecedent basis. For example, the final limitation of claim 1 recites “*the plurality of modules.*”

2. “*passive port*”

The term “*passive port*” should be construed as a “connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module.” PO contends this term should be construed as a “connection between a passive ball and a passive pad.” (INTEL-1026, 13-15.)

Petitioner’s construction is consistent with the definitional statement added by Applicant to the specification: “The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module ... **is named ‘passive port.’**” (INTEL-1001, 9:8 (as modified by COC); INTEL-1005, 2; INTEL-1002, 405, 425.) To overcome the Examiner’s

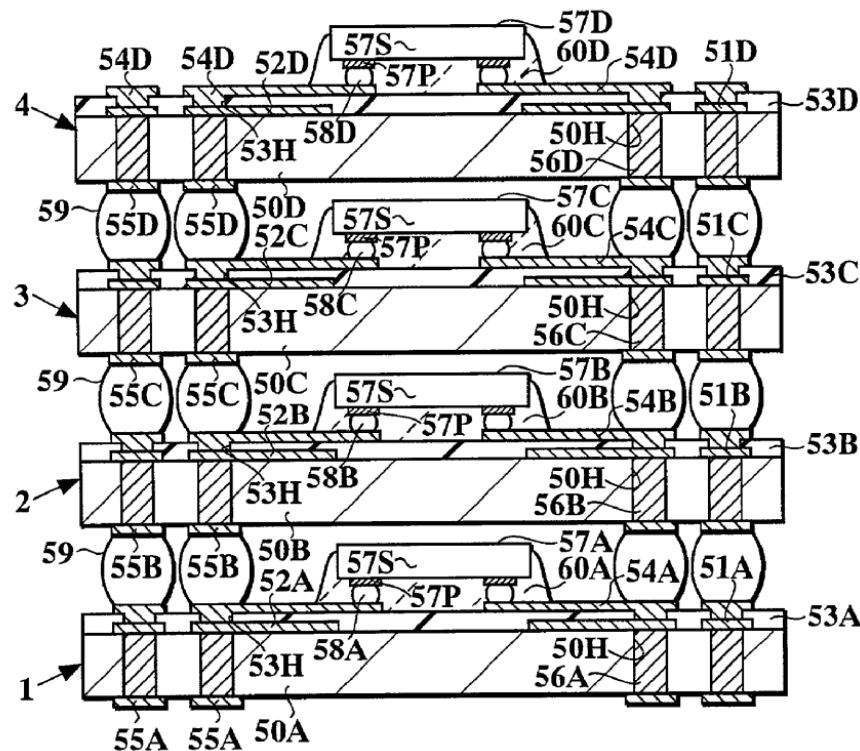
indefiniteness rejections, Applicant stressed it was acting as its “own lexicographer” and repeatedly relied on this added definitional language. (*See* INTEL-1002, 425, 427.) Applicant’s definition should control.

V. GROUND 1: Combination of Hosomi and Sato Renders Claims 1, 2, 11, and 12 Obvious

A. Combination Overview

1. Hosomi

Hosomi discloses a semiconductor module 5, illustrated below, comprising four stacked semiconductor devices 1 to 4. (INTEL-1007, ¶89.) Semiconductor devices 2-4 “are substantially identical” to device 1. (*Id.*)



Hosomi, Figure 5

The substrate of each device has electrodes³ 51A and two wiring layers 52A and 54A on its top surface and electrodes 55A on its bottom surface. (INTEL-1007, ¶96.) The front and rear electrodes are connected by via 56⁴. (INTEL-1003, ¶76.) Rear electrode 55 “is electrically and mechanically connected, via a bump electrode⁵ 59” to a front electrode on an adjacent device. (INTEL-1007, ¶101.)

2. Sato

Sato is directed to “a boundary scan controller for testing connection states of input/output terminals of a plurality of semiconductor circuit chips.” (INTEL-1009, 1:9-12.) Sato’s chip, illustrated in Figure 2 (below left), includes the

³ A POSITA would understand Hosomi’s electrodes are conductive “pads” on a substrate because they electrically connect to other components and are adapted for solder bumping. (INTEL-1003, ¶76, *citing* INTEL-1013, 107-108.)

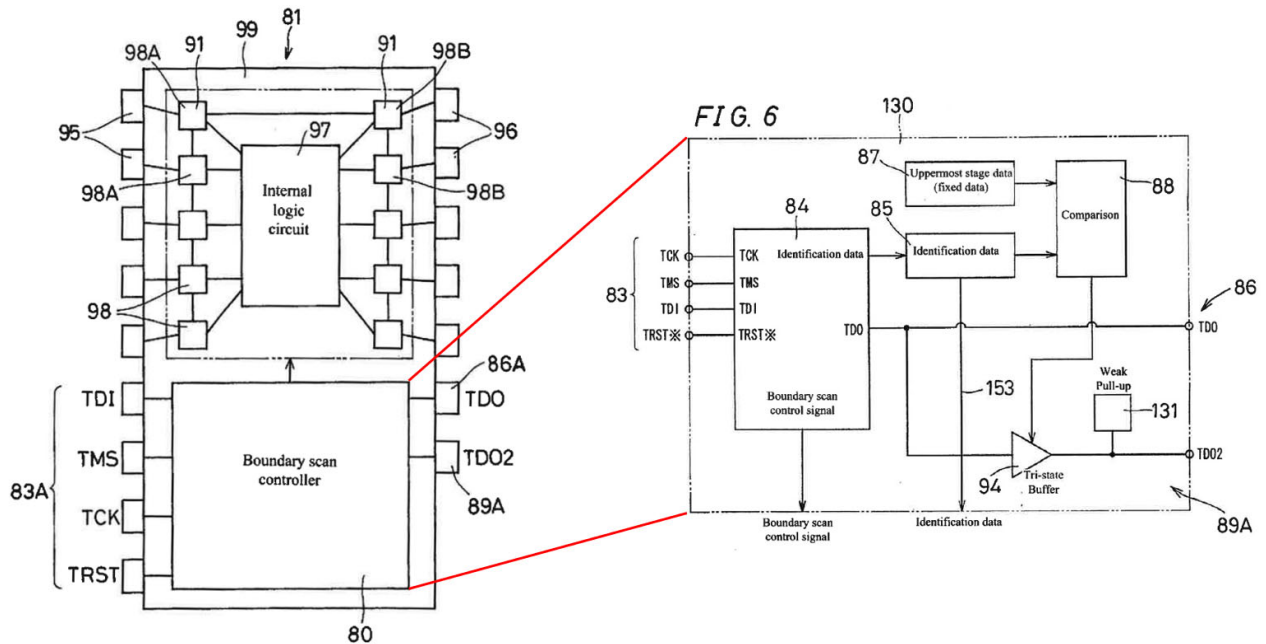
⁴ Connection 56 is a via because it routes connections vertically between layers. (INTEL-1003, ¶¶76, 43-44, *citing* INTEL-1012, 444, INTEL-1013, 607.)

⁵ A bump electrode is also known as a “ball.” (INTEL-1003, ¶¶76, 40.)

standard IEEE test circuit in a block labeled “boundary scan controller 80”⁶.

(INTEL-1003, ¶80.) Sato’s Figure 6 (right) illustrates an embodiment of a boundary scan controller which “operates in conformance to the standards of the JTAG.” (INTEL-1009, 13:22-23.) As such, the controller input has four signal lines: TCK (Test Clock) which supplies input/output timings, TMS (Test Mode Select) which inputs the operation instruction, TDI (Test Data input) which inputs identification and test data, and optional TRST (Test Reset). (INTEL-1009, 14:1-11.) These signal lines “are controlled by an external JTAG tester.” (INTEL-1009, 14:11-12.)

⁶ Although Figure 2 includes controller 80 and Figure 6 illustrates controller 130, the only difference between controllers 80 and 130 is “in the configuration of the data derivation part 89A.” (INTEL-1009, 25:11-18.)

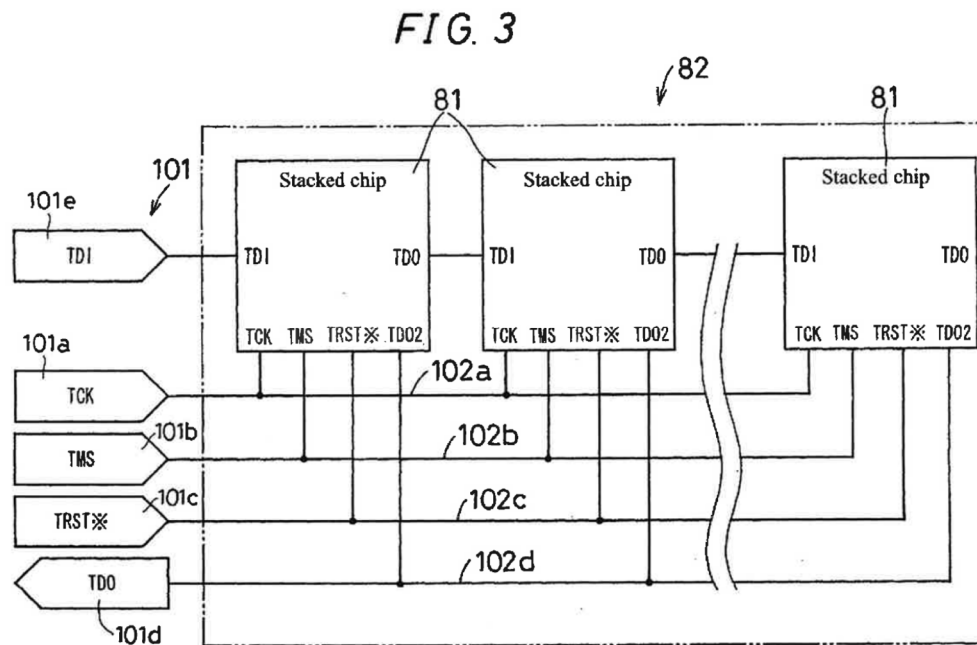


Sato, Figures 2 (right), 6 (left)

Control means 84 “set[s] test pattern data for performing the boundary scan test.” (INTEL-1009, 15:1-4.) For example, when a send data instruction is input, the “various data which are input from the signal line TDI can be output from a signal line TDO ... through the shift registers.” (INTEL-1009, 15:4-7.) Fixed data storage 87 stores chip identification data loaded “when the semiconductor device 82 is configured.” (INTEL-1009, 16:1-4.) Storage means 85 stores identification data received during operation. (Sato, 15:9.) Comparison means 88 determines whether the preconfigured identification data matches the data provided during operation. (INTEL-1009, 16:12-15.) If the result indicates a match, tristate buffer 94 in the data derivation part outputs TDO on the TDO2 signal line. (INTEL-1009,

25:19-25.) If the result indicates a mismatch, tristate buffer 94 “is prevented from outputting input data.” (INTEL-1009, 25:26-28.)

Sato’s semiconductor device 82, illustrated below, “is configured by stacking” semiconductor circuit chip assemblies 81. (INTEL-1009, 20:7-11.) Signal lines TCK of respective chips “are connected to the same bus line 102a.” (INTEL-1009, 20:18-20.) As illustrated below, a controller’s TDO output is connected to the TDI input of the next controller in the stack until the top controller is reached. In the top controller, TDI is connected to TDO2 because no device is stacked above it. (INTEL-1009, 20:29-30, 22:26-32.) TDO2 is then passed by the top controller to the external JTAG tester via bus 102d. In this manner, individual controllers 80 “are connected in the shape of a chain” (referred to as a “daisy chain”) in the stacked module allowing all assemblies to be “simultaneously subjected to the boundary scan test.” (INTEL-1009, 20:31-21:1.)



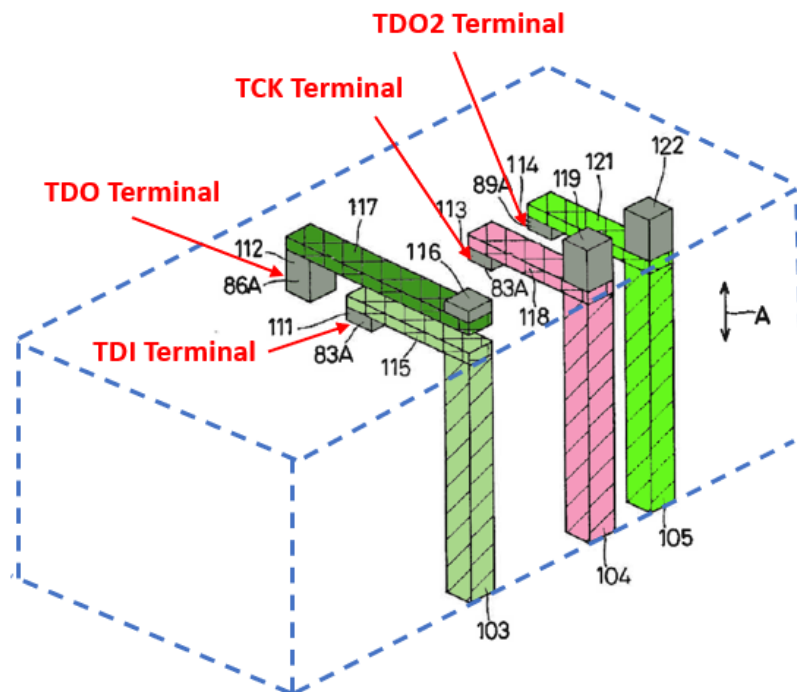
Sato, Figure 3

This daisy-chain connection for an individual assembly 81 is illustrated in Sato's Figure 5 which has been annotated to outline a portion of a device for context. Electrodes⁷ 103-105 "penetrate through the semiconductor circuit chip assembly, namely in the direction of arrow A." (INTEL-1009, 23:12-15.)

Terminals 111 and 113 are inputs for signal lines TDI and TCK respectively. (INTEL-1009, 23:20-23.) Terminals 112 and 114 are the output connection for

⁷ Although Sato uses the term "electrode" for its vertical connector, a POSITA would have understood this to be a "via" through the assembly. (INTEL-1003, ¶¶88, 43-44.)

signal lines TDO and TDO2, respectively. (INTEL-1009, 23:23-25.) Terminals 116, 119, and 122 connect to the end of electrodes 103, 104, and 105 (respectively) of an adjacent device to pass signals between the devices. (See INTEL-1009, 23:28-30, 24:5-7, 24:14-16.)

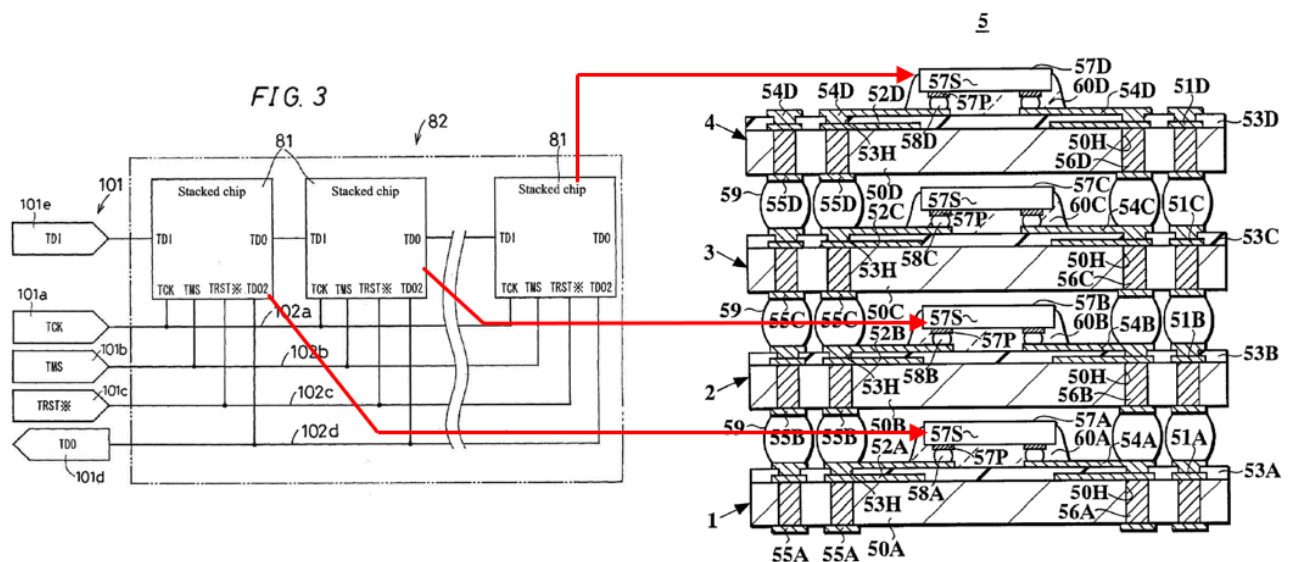


Sato, Annotated Figure 5

3. Motivation to Combine

A POSITA would have been motivated to incorporate Sato's boundary scan controller into a chip in each module of Hosomi's stacked module (as illustrated below) and would have been motivated to implement Sato's daisy-chain connections using the package routing structures of Hosomi. (INTEL-1003, ¶¶90-98.) Specifically, as taught by Sato, a boundary scan controller is incorporated into

the chip in each module of Hosomi's stack—the rightmost controller is disposed in the top module's chip (57D), the leftmost controller is disposed in the bottom module's chip (57A), and a middle controller is disposed in the middle modules' chips (57B and 57C). (INTEL-1003, ¶90.) A POSITA would have been motivated to implement Sato's daisy-chain connections (illustrated in Figure 5) in the combined system which stacks modules (each having a chip mounted on a substrate) using Hosomi's package routing structures including (1) implementing Sato's vertical electrodes using Hosomi's through-vias (*e.g.*, connection 56), Sato's terminals using Hosomi's electrodes 51 (pads), Sato's connection lines using Hosomi's wiring layers (*e.g.*, Figures 6A-6B), and (2) using Hosomi's pad and ball connections to connect adjacent modules. (*Id.*)



Sato, Figure 3 (left); Hosomi, Figure 5 (right)

A POSITA would have been motivated to make the above combination for numerous reasons. First, Sato provides an express teaching that would have led a POSITA to incorporate Sato's boundary scan controller and associated daisy-chain connection teachings into Hosomi's stacked module. (INTEL-1003, ¶91.) Sato teaches its boundary scan test "detect[s] the connection states of individual semiconductor circuit chip[s]" in a stack of semiconductor circuit chips "which are configured by **disposing the boundary scan controller in the semiconductor circuit chip.**" (INTEL-1009, 8:2-8; *see also*, 8:26-27 (device is configured "by stacking the **same semiconductor circuit chip assemblies which include the boundary scan controllers**"); 13:17-19 (chip "configured by disposing the boundary scan controller 80 in a semiconductor circuit chip").) And Hosomi teaches a low cost and reliable technique to route connections between layers in a stack. (INTEL-1003, ¶91.)

Second, a POSITA would have understood that testing was essential, if not required, for manufacturing vertically stacked modules such as those taught by Hosomi. (INTEL-1003, ¶¶92-93.) Boundary scan testing typically occurs at manufacture. (*Id.*) For example, when the stacked module is an SDRAM memory module (as taught by Hosomi), the SDRAM module manufacturer would have been motivated to test the stack of modules to ensure each layer of memory is properly interconnected. (*Id.*) A POSITA would have been motivated to use

boundary scan testing for this testing because boundary scan technology enables testing of connections between devices in a stack without external probes. (*Id.*; INTEL-1013, 272 (explaining it is “more difficult to physically probe lines” and “[i]t is best to base” a test plan “on the use of chips with *boundary scan*”).) A POSITA would have therefore been motivated to combine Sato’s boundary scan teachings into Hosomi to minimize the amount and complexity of equipment required for testing. (INTEL-1003, ¶93, *citing* INTEL-1021, 1 (“[u]sing the JTAG/boundary-scan logic minimizes the amount and complexity of equipment for testing boards JTAG/boundary-scan saves time and costs for your board test and programming systems”).) Even the ’243 itself acknowledged JTAG/boundary scan would be used to test the stacked modules or chips in this time frame. (INTEL-1001, 10:32-33.)

Third, a POSITA would have been motivated to combine the boundary scan teachings of Sato with Hosomi because boundary scan technology was widely known and standardized before the ’243 patent. (INTEL-1003, ¶¶94-95.) Sato explicitly applies JTAG boundary scan testing standards, referring throughout to an external “JTAG tester.” (INTEL-1009, 4:9-5:5, 14:6-18.) The IEEE JTAG boundary scan standard was adopted in 1990, 15 years before the ’243 patent. (INTEL-1003, ¶94, *citing* INTEL-1020.) Moreover, boundary scan testing techniques were described in textbooks many years before the ’243 patent. (*See*

INTEL-1013, 272-273.) Boundary scan technology was also widely used. (INTEL-1003, ¶¶94.) In fact, boundary scan was “the most popular” design for testability technique “employed for enhanced test and diagnosis of electronic systems” prior to the ’243 patent and remains popular today. (INTEL-1017, 5; *see also*, INTEL-1003, ¶¶53-58.)

Fourth, the combination of Hosomi and Sato is nothing more than the combination of prior art elements according to known methods to yield predictable results. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007); INTEL-1003, ¶¶96-97. A POSITA would have combined the well-known elements of Hosomi and Sato using well-known methods. (INTEL-1003, ¶96.) As discussed above, JTAG boundary scan was standardized since 1990 and would have been well known to a POSITA by 2005. (*Id.*) Groups, such as NASA, were integrating JTAG boundary scan into complex stacked multichip modules years before the ’243 patent. (*See* INTEL-1022, 44–45.) Indeed, because testing is so critical for devices, it was not uncommon prior to the ’243 patent that a device’s test cost is comparable to its manufacturing cost, further confirming a POSITA would have been motivated and understood how to include industry standard testing in Hosomi’s modules. (INTEL-1003, ¶96, *citing* INTEL-1017, 2.) Hosomi and Sato both perform the same function in combination as they do separately. (INTEL-1003, ¶97.) Hosomi acts as SDRAM separately and in the combination. (*Id.*) Sato’s

boundary scan components and daisy-chain connections operate the same way in the combination with Hosomi as they do separately. (*Id.*) A POSITA would have further recognized the results of the combination were predictable and would have had a reasonable expectation of success because, as discussed above, use of boundary scan testing for IC assemblies was well-known, standardized, and widely used before the '243 patent.

Finally, a POSITA would have understood the combination of Hosomi and Sato merely amounts to applying known techniques to a known device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 417; INTEL-1003, ¶98. Hosomi discloses a “base” device—a stacked SDRAM module—upon which Sato’s boundary scan architecture is directly applicable to provide the capability for testing without use of probes. (INTEL-1003, ¶98.) A POSITA would have considered the combination improvement to Hosomi because chips manufactured with built-in terminals that support boundary scan have the capability to be tested for faulty interconnections at the same time and using the same test vectors. (*Id.*) A POSITA would have recognized Sato’s known boundary scan technique would have yielded predictable results and would have resulted in an improved system free of interconnection faults for the reasons discussed in this section. (*Id.*)

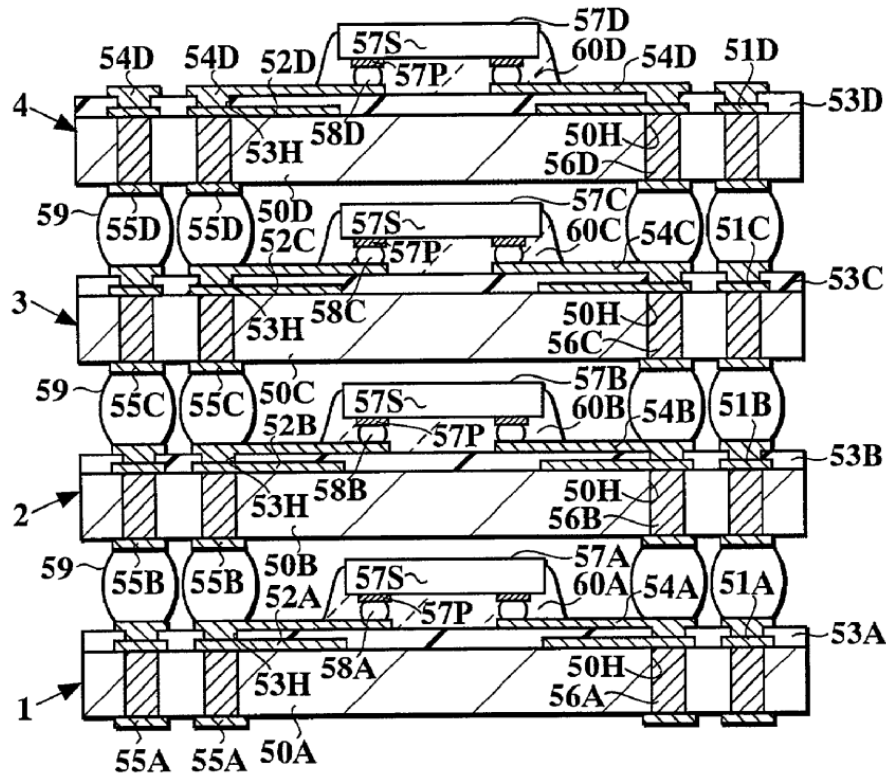
B. Independent Claim 1

1. Preamble [1P] and “*Plurality of Modules*” [1A].

Hosomi’s semiconductor module 5, illustrated below, comprises a stack of semiconductor devices 1 to 4. (INTEL-1007, ¶89) Semiconductor devices 2 to 4 “are substantially identical” to semiconductor device 1 and are each “constituted by an SDRAM system.” (INTEL-1007, ¶¶89, 74.) Semiconductor device 1-4⁸ are each a “*module*” of stacked semiconductor module 5 because each includes a chip connected to a substrate. (INTEL-1003, ¶99.) Hosomi therefore discloses a “*stacked module*” [1P] that comprises “*a plurality of modules*” [1A]. (*Id.*)

⁸ For ease of discussion, Petitioner refers to each of Hosomi’s semiconductor devices as a “module” and the stack as a “stacked module.”

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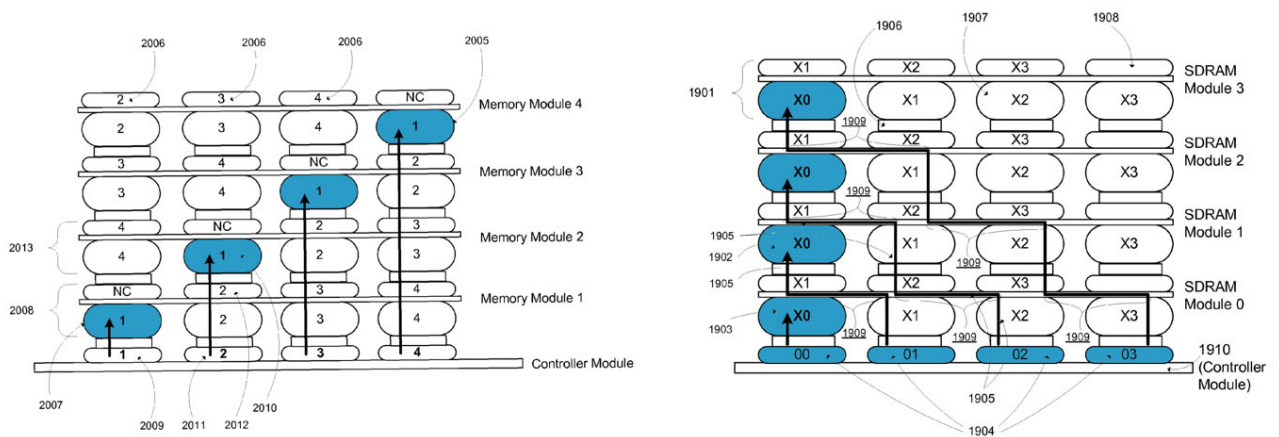
Hosomi, Figure 5

Petitioner establishes in §§ V.B.2.-5 that (1) each module includes limitations [1B]-[1F] as required by Petitioner’s construction of the “*plurality of modules comprising*” and (2) the “*stacked module*” includes these limitations as required by PO’s construction. (See §IV.C.1.)

2. “One or More Active Ports” [1B].

The combination of Hosomi and Sato discloses “*one or more active ports for carrying one or more active signal*” [1B]. (INTEL-1003, ¶¶100-112.) The ’243 patent does not define the term “*active port*,” but the COC indicates “[a]n **active**

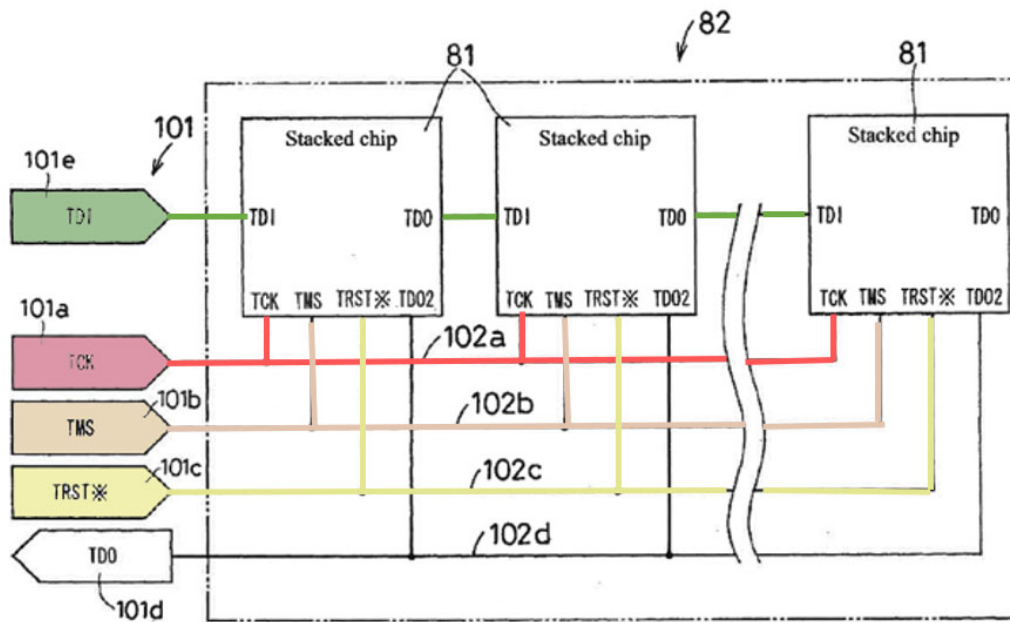
pad may be also referred to herein as an ‘active port.’” (INTEL-1001, 9:3; INTEL-1005, 1.) The ’243 patent similarly does not define the term “*active signal*.” In connection with Figure 20b, the ’243 patent describes Pins 1 (shaded blue) which receive signals at a module as “**active signal** pins for the module. (See INTEL-1001, 9:47-49.) The COC states an “active signal” is “applied at an **active pad**, such as **active pad** 02, shown with reference number 1904 [shaded blue] on controller module 1910” and “eventually reaches an active ball, such as [an] X0 ball [shaded blue].” (See INTEL-1005, 2; INTEL-1001, FIG 19 (below right).) When an active signal is received, for example, at port X0 of a module, it is distributed to the circuitry on that module. (INTEL-1003, ¶100; *see, e.g.*, INTEL-1001, Figure 21b.)



’243 Patent, Annotated Figures 20b (left), 19 (right)

The '243 patent therefore uses the term “port” broadly as either an entry to or exit from a module or circuit/chip on the module. (INTEL-1003, ¶101.) And, according to the '243 patent, an “*active signal*” encompasses a signal applied to the stack by an external source and distributed via an “*active port*” to circuitry on the module. (*Id.*)

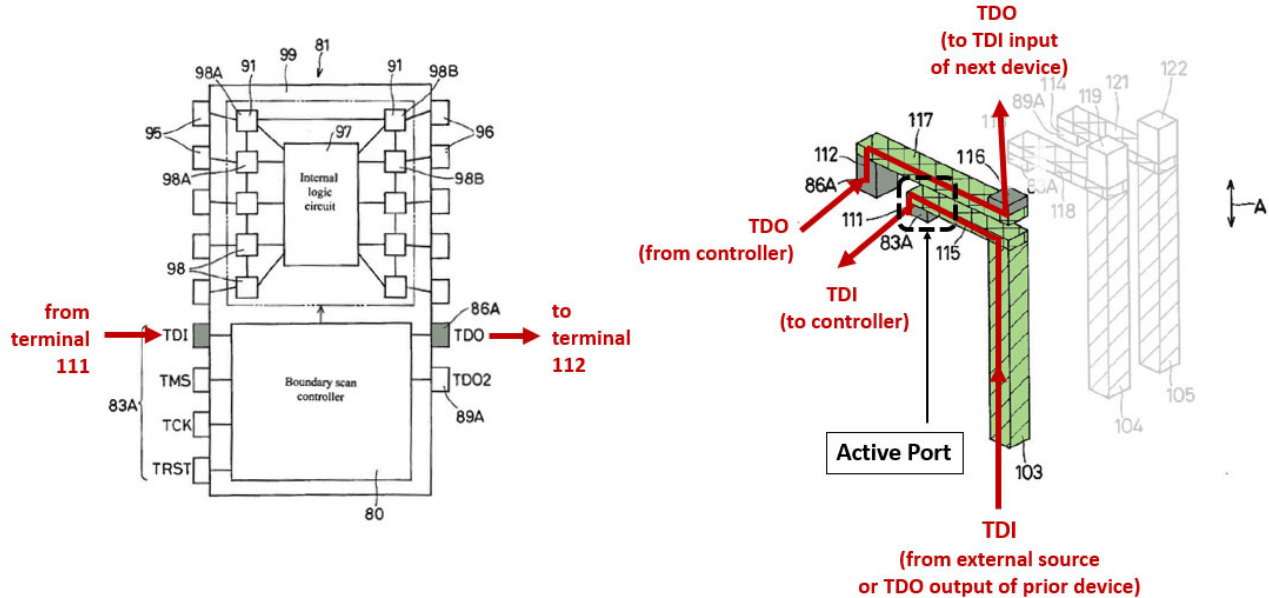
Sato discloses numerous “*active signals*” carrying information and used by a boundary scan controller including TDI (data input) and TCK (clock). In the stacked module of the combination of Hosomi and Sato (having a boundary scan controller in each module and using Sato’s daisy-chain connections), the TDI active signal (shaded green) is applied to the bottom controller (leftmost) by an external JTAG tester. (INTEL-1009, Figure 3 (below).) The TDO output of the bottom controller is connected to the TDI input of the controller in the next module in the stack. (INTEL-1009, 20:24-27.) The TDO output of that module is in turn connected to the TDI input of the next module and so on until the top controller (rightmost) is reached. The daisy-chain path propagates TDI through the stack. (INTEL-1003, ¶102.) Signal lines TCK (shaded red), TMS (shaded orange) and TRST (shaded yellow) are distributed through the stack to the controller in each module via identical bus lines 102a-c. (INTEL-1009, 20:20-23.)



Sato, Annotated Figure 3

a. TDI active signal path

In the TDI signal path of Sato’s daisy-chain connection, illustrated in Figure 5 below, TDI passes through electrode 103 (shaded green) to terminal 111 via connection line 115 (shaded green). (INTEL-1009, 23:26-27.) The active TDI signal is then communicated from terminal 111 (shaded gray) to the TDI input of the boundary scan controller. (See INTEL-1009, Figure 2 below; INTEL-1003, ¶104.) Terminal 111 distributes TDI to the boundary scan controller and is therefore an “*active port*.” (INTEL-1003, ¶¶104-105; INTEL-1005, 1.)



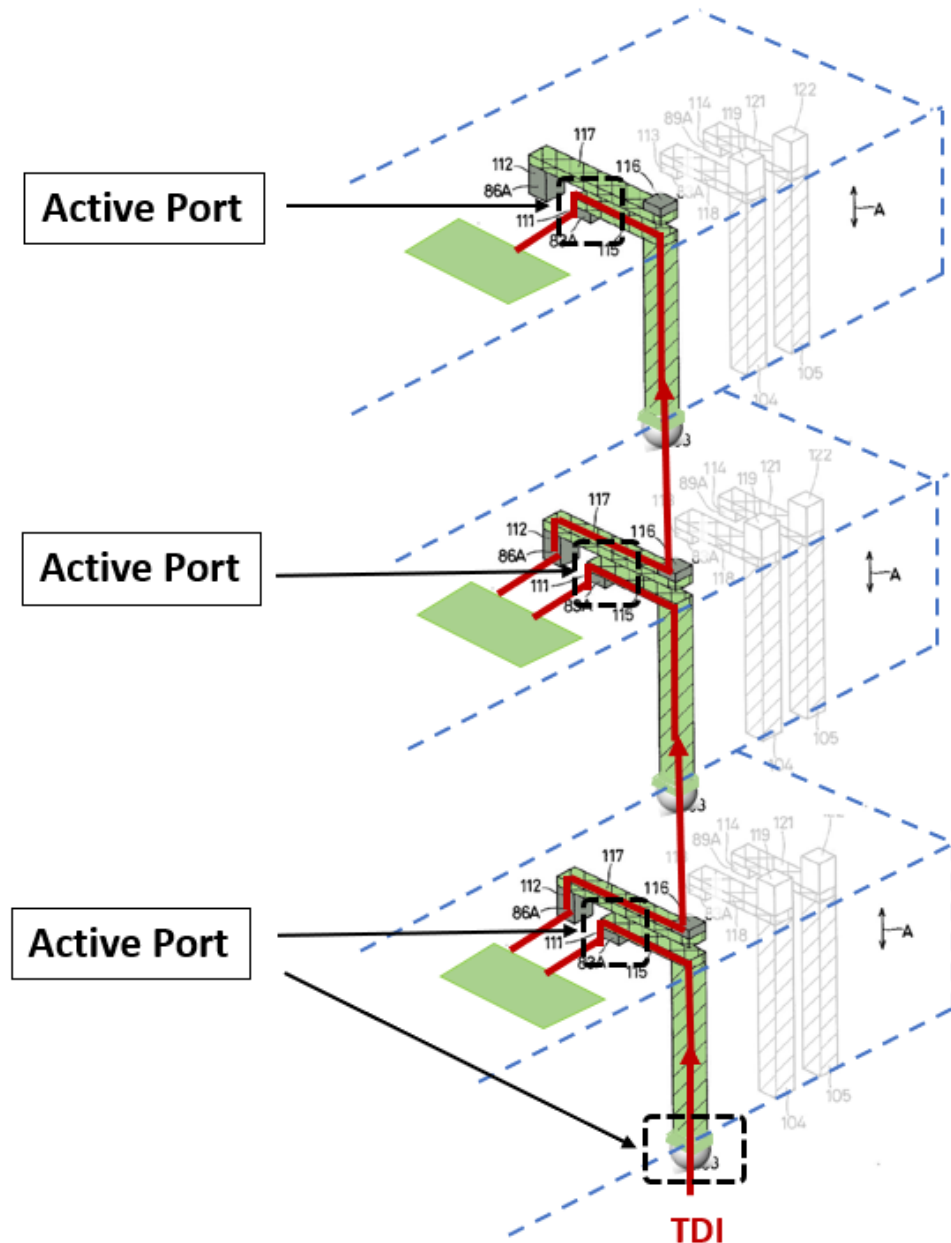
Sato, Annotated Figures 2 (left) and 5 (right)

In the combination of Hosomi and Sato, Sato's Figure 5 daisy-chain connection is integrated into the substrate of each stacked SDRAM semiconductor device of Hosomi as shown in Thompson⁹ Figure A. (See §V.A.3; INTEL-1009, 23:5-25:10.) As discussed in §V.A.3, the daisy-chain connection is implemented using Hosomi's vias as Sato's vertical electrodes, Hosomi's pads as Sato's terminals, Hosomi's wiring layers for Sato's connections, and the modules are connected using the pad/ball connections taught by Hosomi. As illustrated below,

⁹ All Figures labeled "Thompson Figure X" refer to Thompson Declaration Figures and were created by Petitioner to illustrate the combination.

the TDI signal is applied to the bottom module from an external JTAG tester.

(INTEL-1003, ¶106.) The pad/ball receiving the TDI signal at the bottom module is an “*active port*” because it receives TDI from an external source. (INTEL-1003, ¶¶107-108.)



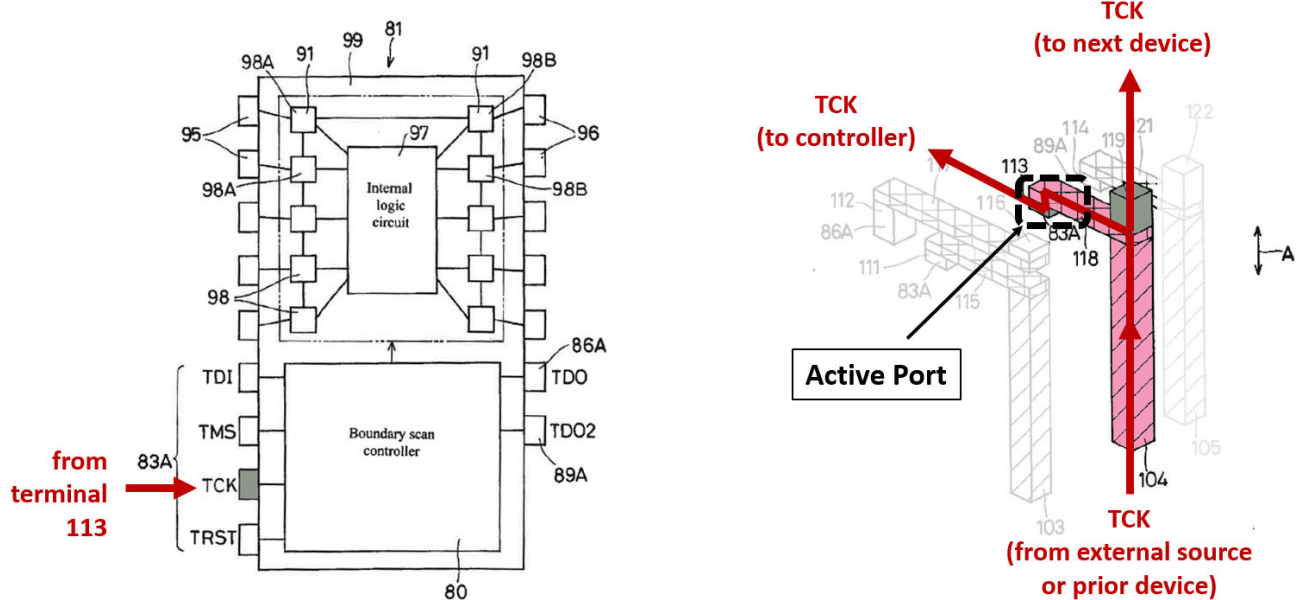
Thompson, Figure A: Hosomi and Sato—Stacked Module

TDI travels through the daisy-chain path of the bottom module to terminal (pad) 116 which is coupled to the pad/ball connection of the adjacent module coupled to electrode (via) 103. (INTEL-1003, ¶108.) TDI continues up the stack through the daisy chain in each module until it reaches the boundary scan controller in the top module. (*Id.*) As shown above, terminal (pad) 111 in each module distributes TDI to the controller for that module. Therefore, terminal (pad) 111 in each module is an “*active port*.” (*Id.*)

b. TCK signal path¹⁰

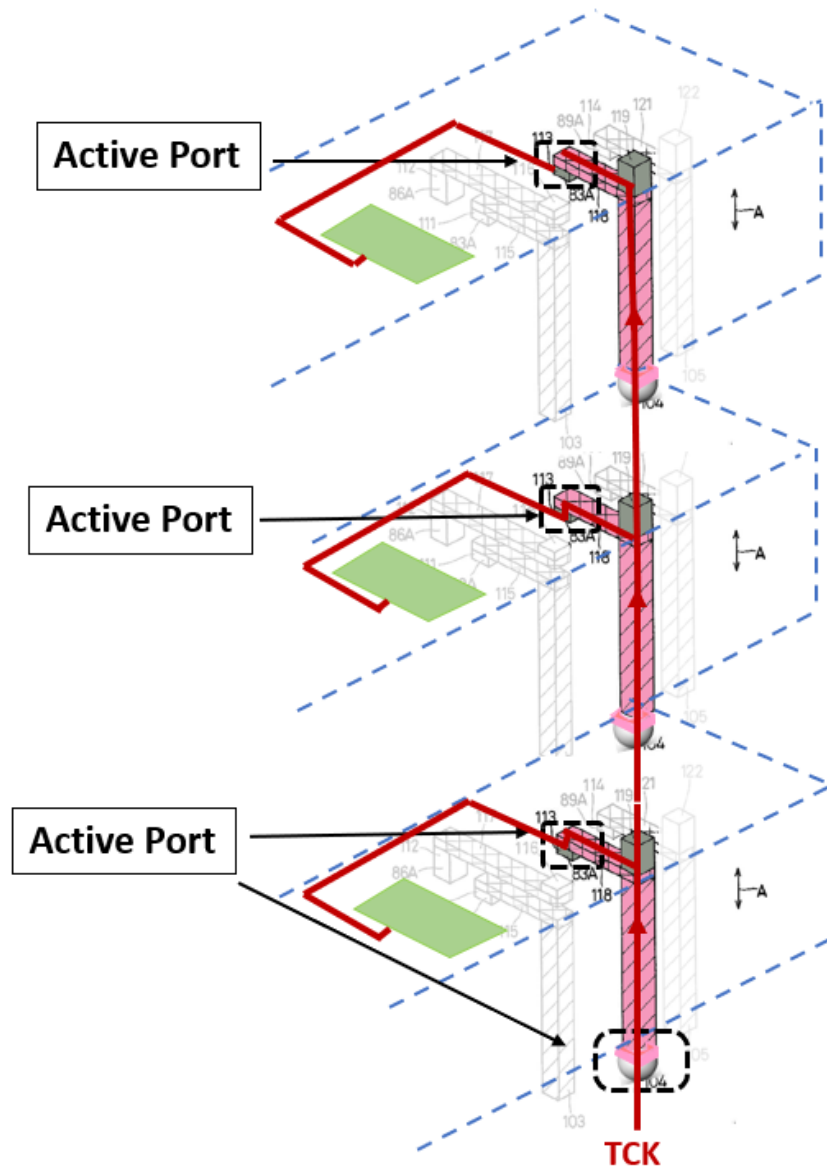
In Sato, TCK passes through electrode 104 and “is interconnected to the terminal 113” through connection line 118. (INTEL-1009, 24:3-4; Figure 5 below.) TCK is then provided from terminal 113 to the TCK input of the controller via a connection line. (INTEL-1003, ¶109.) Terminal 113 is an “*active port*” because it distributes active signal TCK to the controller. (INTEL-1003, ¶109.)

¹⁰ TMS and TRST have similar signaling paths as TCK and therefore would have a set of “*active ports*” carrying these signals for the same reasons discussed in this section. (INTEL-1003, ¶111.)



Sato, Annotated Figures 2 (left) and 5 (right)

In the “*stacked module*” of the combination of Hosomi and Sato illustrated in Thompson Figure B, TCK is applied to the bottom substrate from the external JTAG tester. The terminal (pad/ball) receiving TCK at the bottom module is an “*active port.*” (INTEL-1003, ¶110.) As shown, terminal (pad) 113 in each module distributes TCK and is therefore also an “*active port.*” (INTEL-1003, ¶110.)



Thompson, Figure B: Stacked Module of Hosomi and Sato—TCK Signal Path

* * *

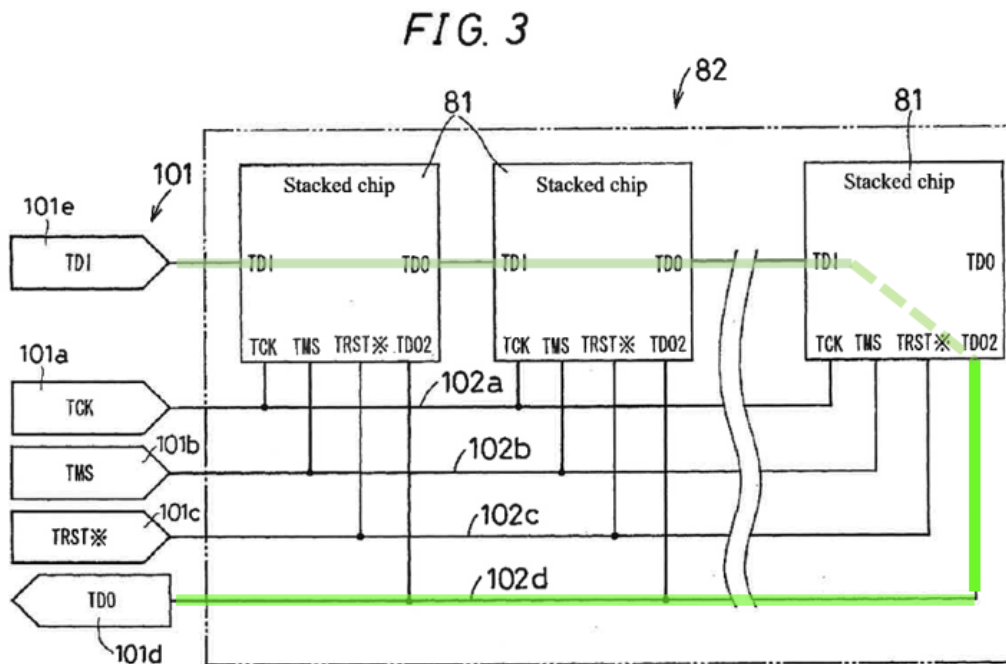
Thus, the combination of Hosomi and Sato discloses each module in its “*stacked module*” includes “*one or more active ports for carrying one or more active signal*” [1B], as required by Petitioner’s “*plurality of module*” construction.

(INTEL-1003, ¶¶100-112.) The combination therefore also discloses the entire “*stacked module*” includes this limitation, as required by PO’s construction. (*Id.*)

3. “*Passive Port*” [1C].

Limitation [1C] recites “*one or more passive ports for passing through the one or more active signals.*” Petitioner’s construction of “*passive port*” is the “connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module.” (*See* §IV.C.2.) PO contends a “*passive port*” is simply any “connection between a passive ball and a passive pad.” (*Id.*) The combination of Hosomi and Sato discloses multiple “*passive ports*” under both constructions. (INTEL-1003, ¶¶113-117.)

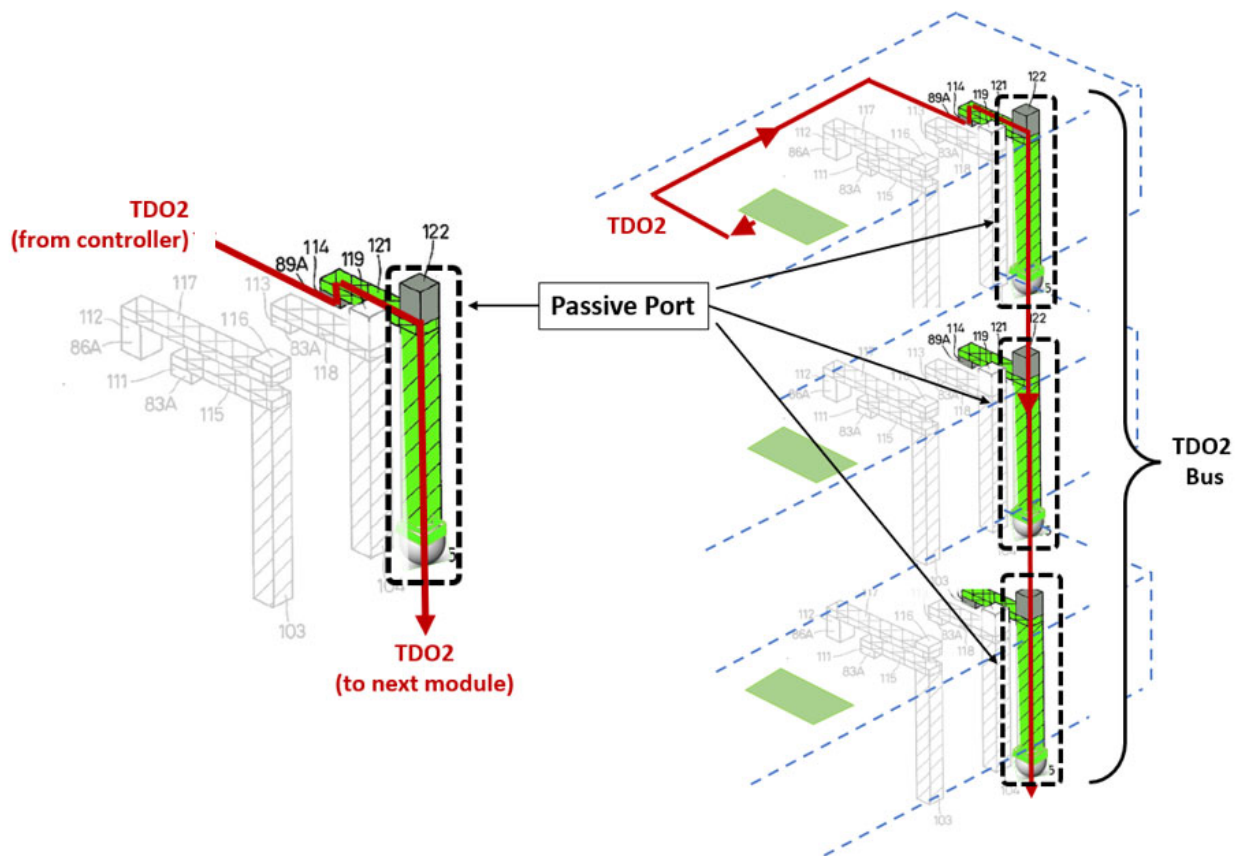
Each module in Hosomi’s stack is an SDRAM module. (§V.B.1; INTEL-1007, ¶¶89, 74.) As shown in Figure 3 below, the controller in the top SDRAM module in the stacked module of Hosomi and Sato outputs TDO2 (shaded neon green) to bus 102d (“TDO2 bus”) which passes TDO2 through the stack to the external JTAG tester. TDO2 is an “*active signal*” because it carries the output data of a boundary scan of the stacked module. (INTEL-1003, ¶114.)



Sato, Annotated Figure 3

The TDO2 bus is a path through the stack and includes a set of interconnected “*passive ports.*” (INTEL-1003, ¶115.) As illustrated in Figure 5 below left, in Sato’s daisy-chain path, TDO2 is output from the controller and transmitted to terminal 114 and then terminal 122 through connection line 121. (INTEL-1009, 24:10-11; INTEL-1003, ¶115.) The path from terminal 122 in the top module through the stack to the external JTAG tester is the TDO2 bus. (INTEL-1003, ¶115.) In the “*stacked module*” of the combination of Hosomi and Sato illustrated in Thompson Figure C below, TDO2 passes from terminal (pad) 122, through electrode (via) 105, to the pad/ball structure at the bottom of the module which is connected to terminal (pad) 122 of the next module in the stack.

Each module in the stack includes the TDO2 portion of the daisy-chain connection. (INTEL-1003, ¶116.) This structure is a “*passive port*” under both constructions because it passes the active TDO2 from a terminal (pad) to a ball on the opposite side of an SDRAM module and subsequently a pad in the adjacent module in the stack or to a pad carrying TDO 2 to an external JTAG tester. (INTEL-1003, ¶116.)



Sato, Annotated Figure 5, Top Device (left)

Thompson, Figure C: Stacked Module of Hosomi and Sato—TDO2 (right)

* * *

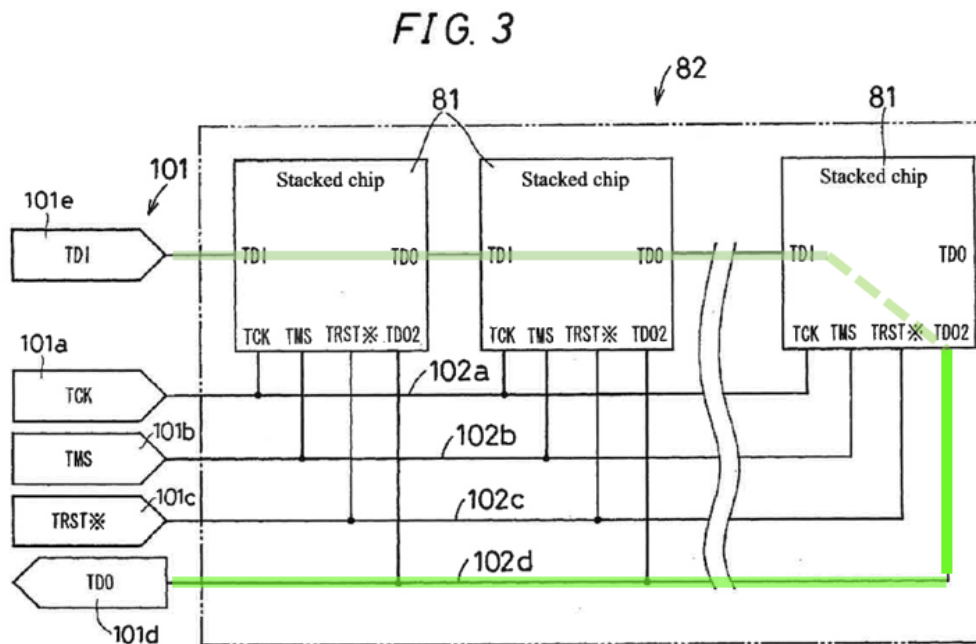
Thus, the combination of Hosomi and Sato discloses each module in its “*stacked module*” includes “*one or more passive ports for passing through the one*

or more active signals” [1C], as required by Petitioner’s “*plurality of modules*” construction. (INTEL-1003, ¶¶110-117.) The combination also discloses the entire “*stacked module*” includes this limitation, as required by PO’s construction. (*Id.*)

4. “*First Serial Chain Route*” Limitation [1D].

The daisy-chain boundary scan signal path in the combination of Hosomi and Sato has “*a first serial chain route that includes at least one serial chain connection*” [1D]. (INTEL-1003, ¶¶118-128.)

In the daisy-chain path, test data is input to the TDI signal line of the bottom controller (leftmost device) from an external source. TDI travels up the stack, passed from TDO output of one controller to TDI input of the next, until the top controller is reached. (INTEL-1009, 20:24-27; Figure 3 below; §V.A.2.) This path from the TDI input of the controller in the bottom module to the TDI input of the controller in the top module includes multiple “*serial chain connections.*” (INTEL-1003, ¶¶119-125.)



Sato, Annotated Figure 3

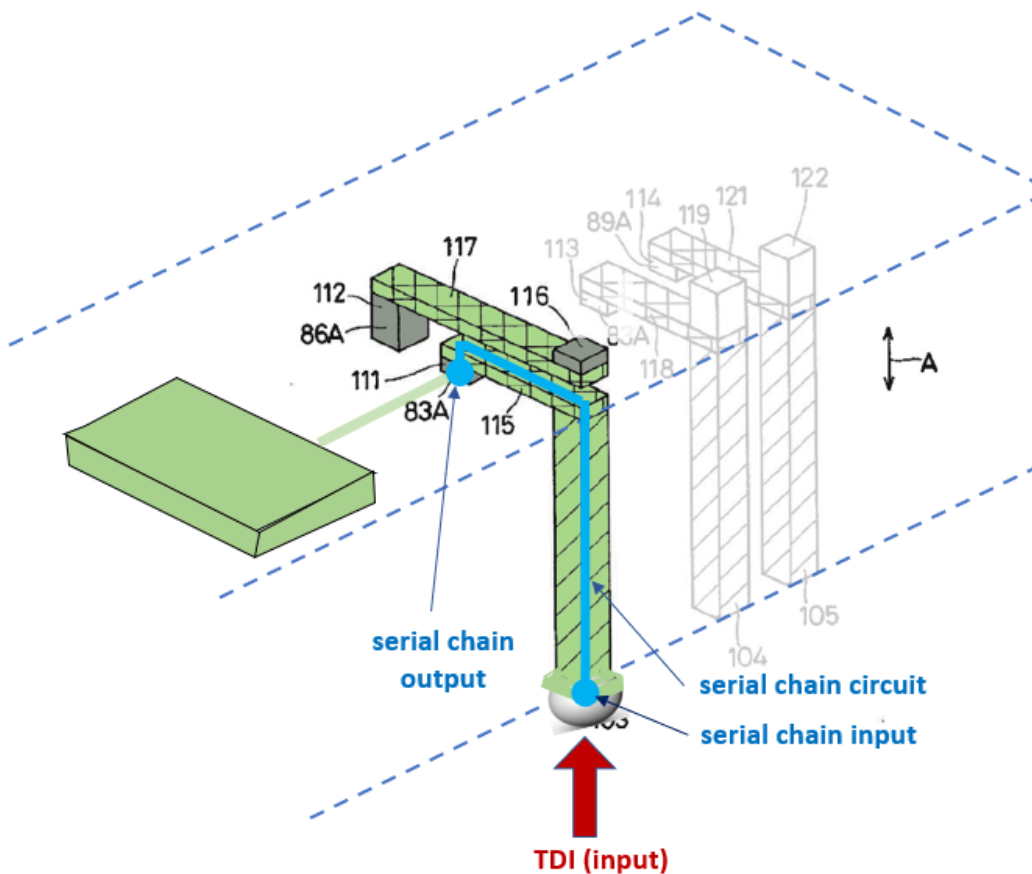
a. “Serial Chain Connection”

The daisy-chain path includes at least two “*serial chain connection[s]*” in each stacked module—a vertical connection and two horizontal connections.

(INTEL-1003, ¶¶120-125.)

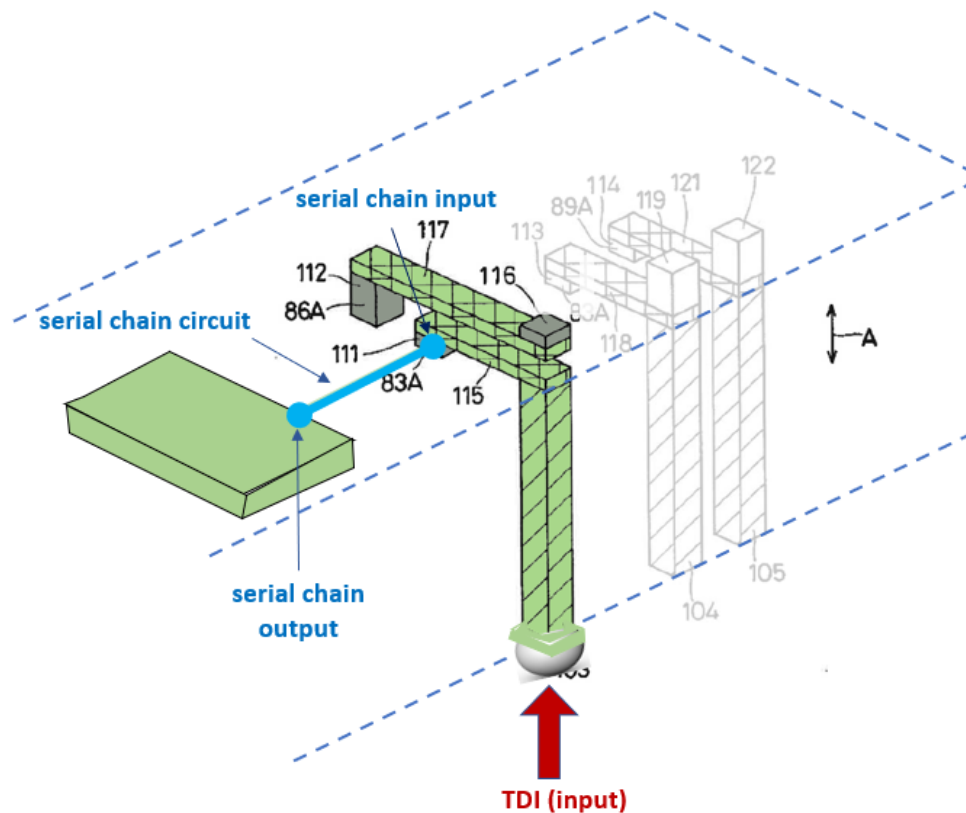
Vertical “Serial Chain Connection”: In the daisy-chain path of the combination of Hosomi and Sato, TDI is applied to the pad/ball at the bottom of the module and passes through electrode (via) 103 and connection line 115 to terminal (pad) 111 as shown below in Thompson Figure D. (See INTEL-1009, 23:26-27.) In the bottom module of the stack, TDI is applied from an external JTAG tester. (See INTEL-1009, Figure 3.) In other modules in the stack, TDI is the

TDO output of the preceding module. (See INTEL-1009, 20:24-27; INTEL-1003, ¶121.) The pad-via-ball structure in each module is a vertical “*serial chain connection*” with the ball on the lower surface of the module receiving TDI being a “*serial chain input*”, electrode (via) 103 being a “*serial chain circuit*”, and terminal (pad) 111 on the upper surface that provides TDI to the controller being a “*serial chain output*.” (INTEL-1003, ¶¶121-122; INTEL-1005, 2 (“A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal”), (“serial chain circuit coupl[es] a ball and pad”).)



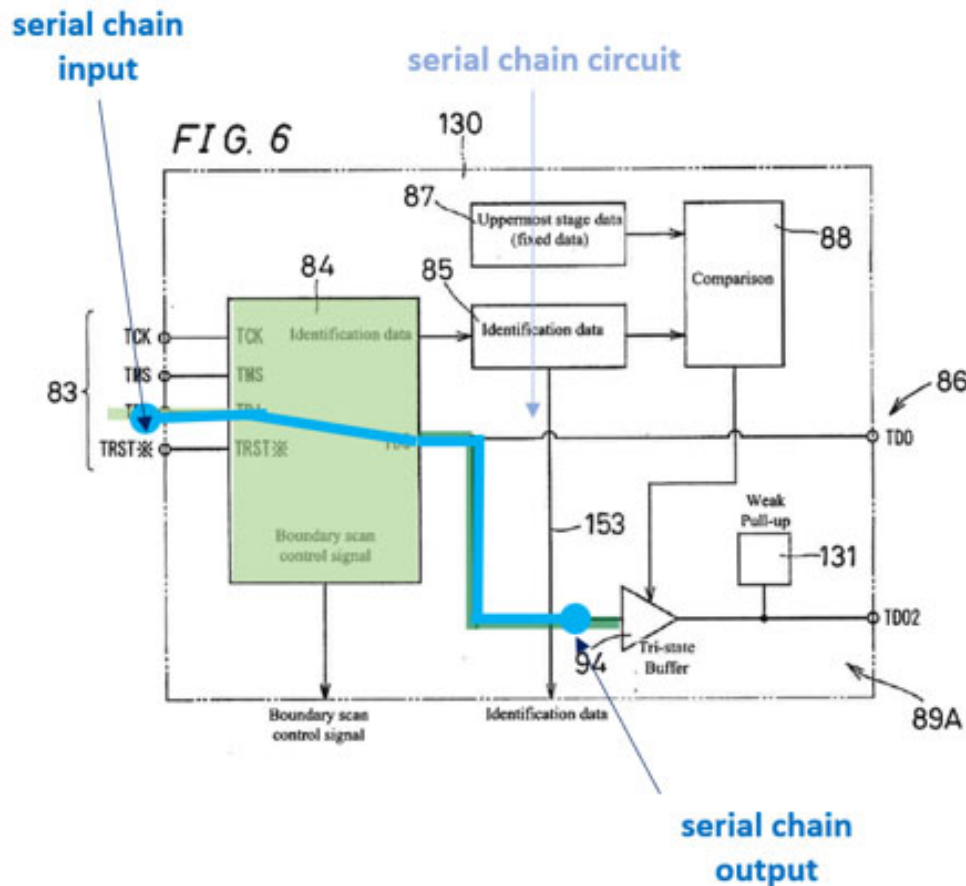
Thompson, Figure D: Sato’s Daisy Chain on Module Substrate

Horizontal “Serial Chain Connection”: Each module in the “*stacked module*” of Hosomi and Sato also includes at least two “*serial chain connections*” in the horizontal direction. (INTEL-1003, ¶¶123-135). First, terminal (pad) 111 is connected to the input of the boundary scan controller (shaded green) via a connection line. This horizontal path (shown in the figure below) is a “*serial chain connection*” with terminal (pad) 111 being the “*serial chain input*”, the connection line being the “*serial chain circuit*” and the boundary scan controller’s input being the “*serial chain output*.” (INTEL-1003, ¶123; Thompson, Figure E.)



**Thompson, Figure E: Horizontal “Serial Chain Connection”
Terminal (Pad) 111 to Controller**

Second, a horizontal “*serial chain connection*” exists inside the boundary scan controller. As discussed in §V.B.2, test data input on signal line TDI are output from signal line TDO through shift registers in control means 84. (See INTEL-1009, 15:4-7.) When the pre-configured identification data for a module matches identification data received during operation, a tristate buffer in the controller outputs TDO on signal line TDO2. (See INTEL-1009, 19:21-23.) During a boundary scan, a match condition occurs in the top module. (INTEL-1003, ¶124.) Thus, in the top module as shown in Figure 6 (below), the horizontal path from the controller’s TDI input to the buffer input is a “*serial chain connection*” with the controller’s TDI input being the “*serial chain input*”, the connection through the register of the control means to tri-state buffer’s input being the “*serial chain circuit*” and the tri-state buffer input’s being the “*serial chain output.*” (*Id.*)

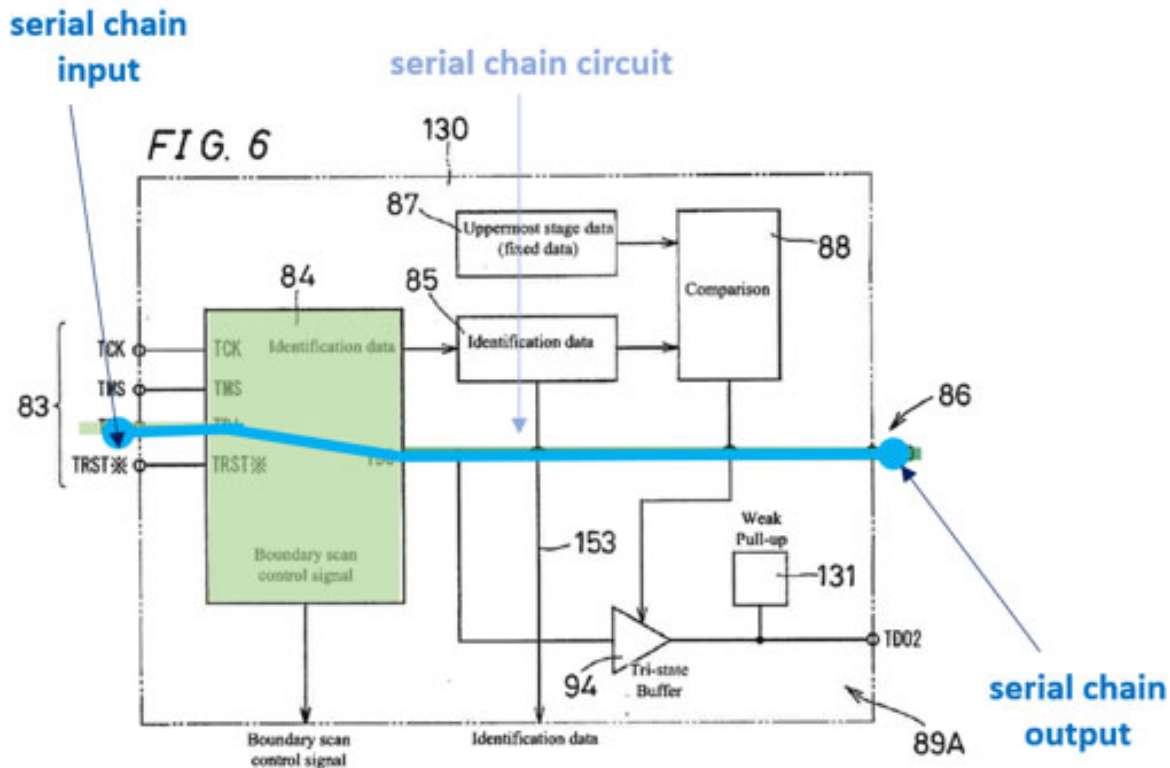


Sato, Annotated Figure 6—Top Module

When a mismatch condition occurs, as shown in Figure 6 below, “tristate buffer 94 is prevented from outputting input data.” (INTEL-1009, 25:26-28.)

During a boundary scan, a mismatch condition occurs in each controller beneath the top module in the stack. (INTEL-1003, ¶125.) Therefore, in these modules, no data is output on signal line TDO2 and signal line TDO outputs the data input on signal line TDI. (*Id.*) In these modules, the horizontal path from the controller’s TDI input to the controller’s TDO output is a “*serial chain connection*” with the

controller's TDI input the “*serial chain input*”, the connection through the register of the control means to the TDO output being the “*serial chain circuit*” and the TDO output being the “*serial chain output.*” (*Id.*)

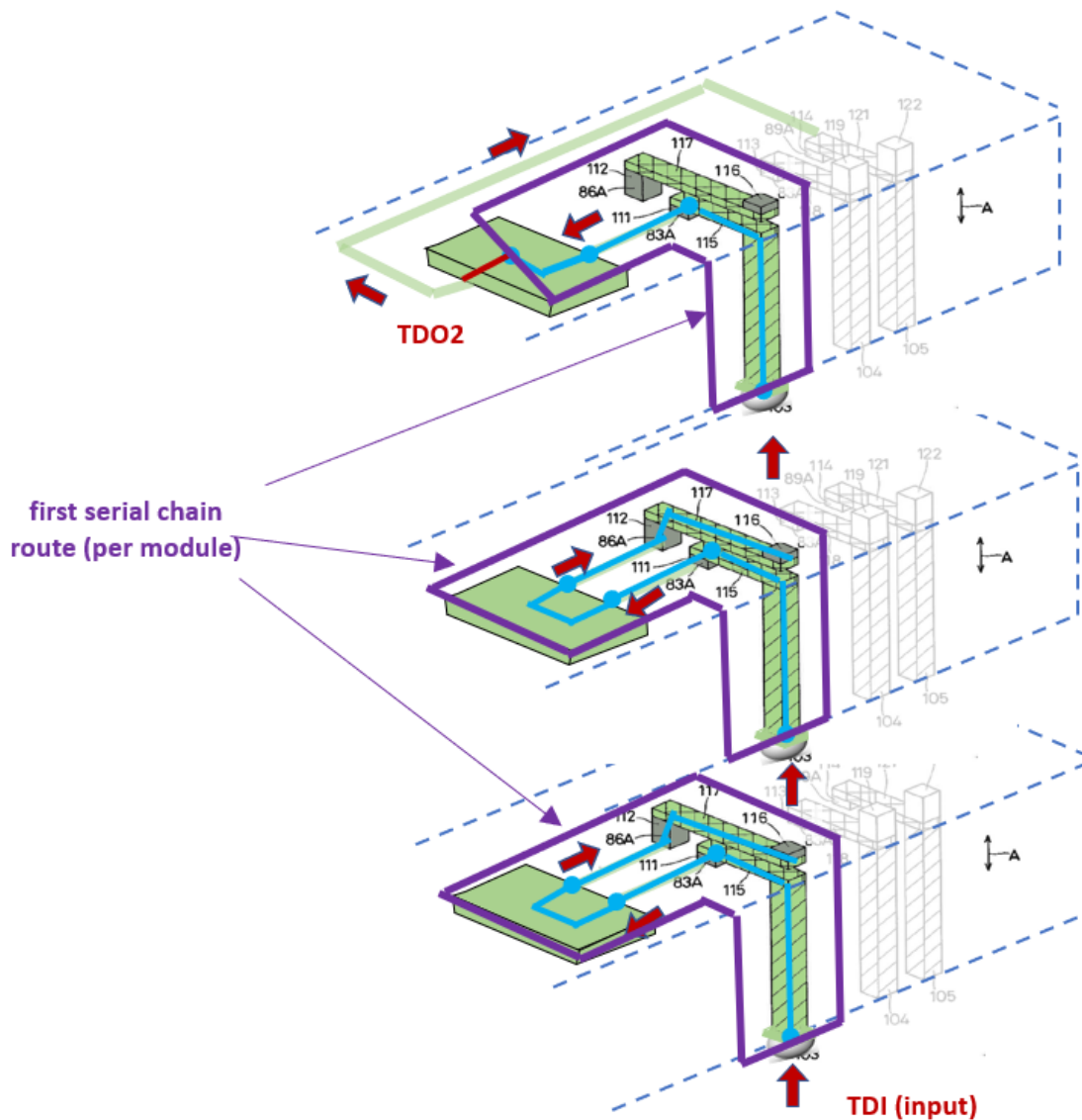


Sato, Annotated Figure 6—Other Modules

b. “First Serial Chain Route” - Petitioner’s “Plurality of Modules” Construction

Petitioner’s “*plurality of modules*” construction requires each module in the stack includes a “*first serial chain route*.” As claimed, the “*first serial chain route*” requires only “*one serial chain connection*.” Each module in the combined “*stacked module*” of Hosomi and Sato includes a vertical “*serial chain connection*”

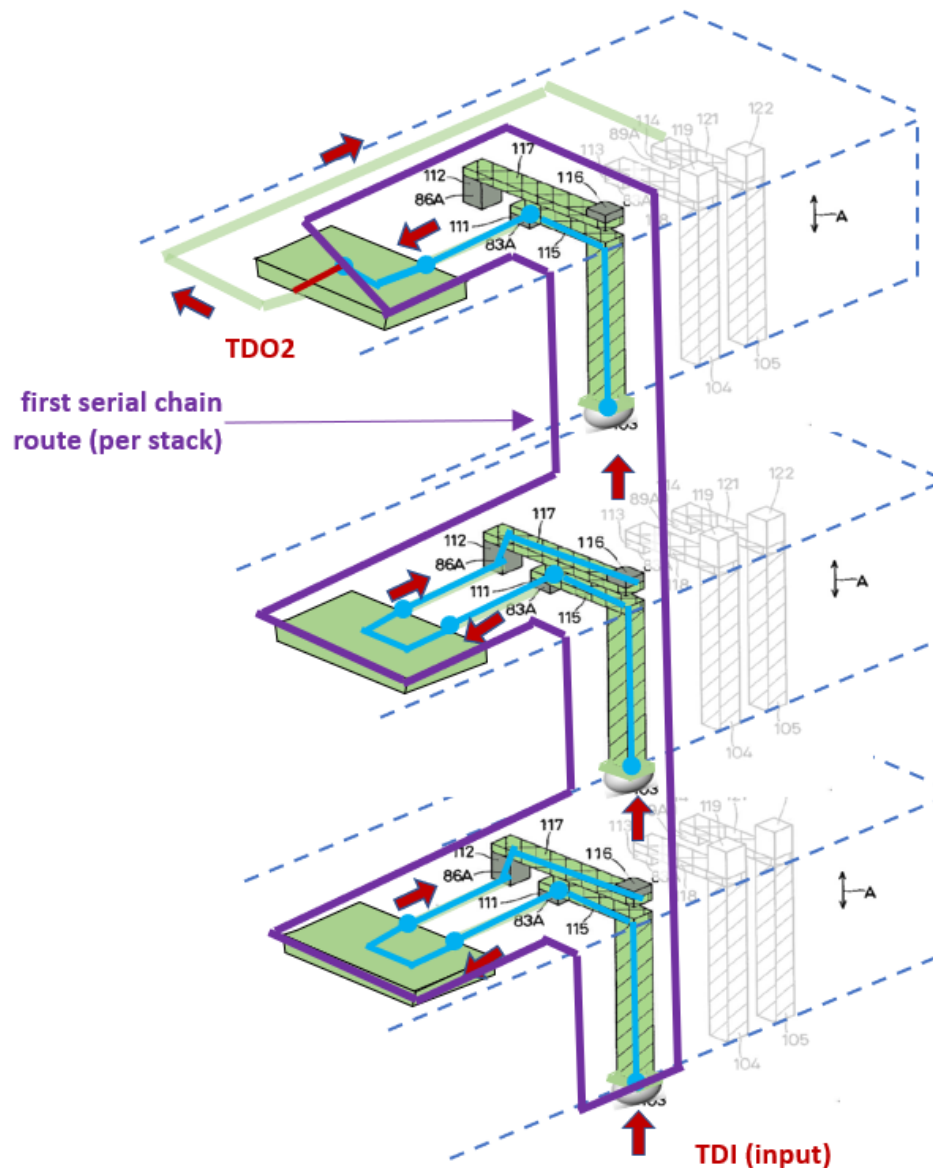
serially connected to two serial horizontal “*serial chain connections.*” (INTEL-1003, ¶126.) Thus, the combination of Hosomi and Sato discloses each module in the stack has “*a first serial chain route that includes at least one serial chain connection*” [1D] as illustrated in Thompson Figure F. (INTEL-1003, ¶126.)



Thompson, Figure F: Petitioner's Construction

**c. “*First Serial Chain Route*”—PO’s “*Plurality of Modules*”
Construction.**

PO’s “*plurality of modules*” construction requires the entire “*stacked module*” include a “*first serial chain route*.” The “*stacked module*” includes multiple “*serial chain connections*” because each module includes a vertical and two horizontal “*serial chain connections*.” Thus, the combination of Hosomi and Sato discloses that the “*stacked module*” includes this limitation, as illustrated in Thompson Figure G. (INTEL-1003, ¶127.)



Thompson, Figure G: PO's Construction

5. “*Second Serial Chain Route*” [1E] and “*Control Circuit*” [1F].

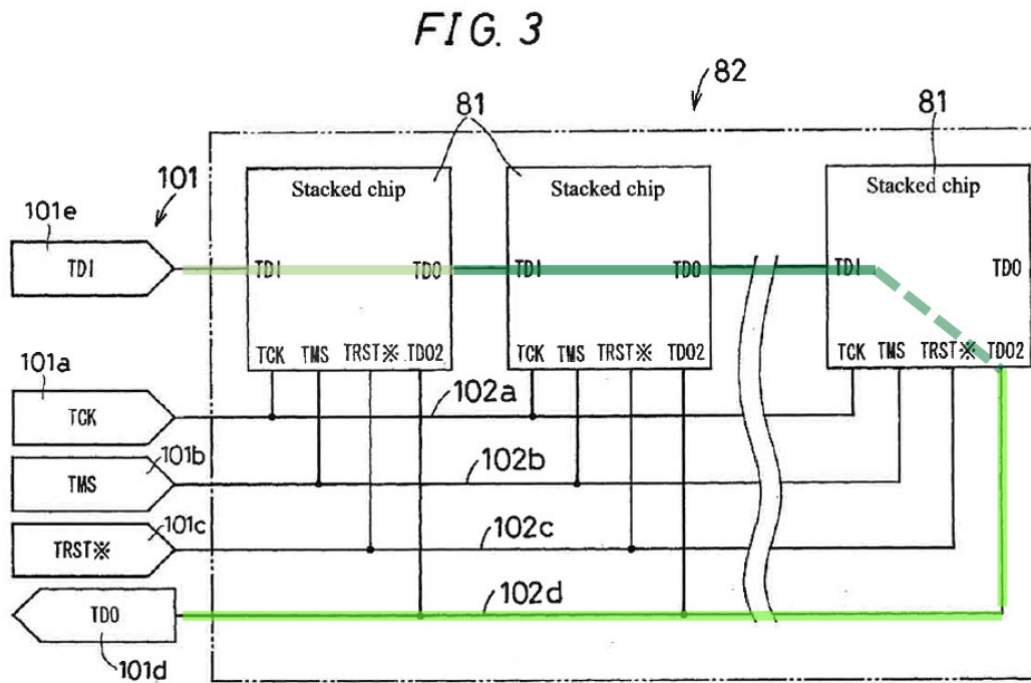
The combination of Hosomi and Sato discloses “*a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module [1E], said control circuit is disposed to enable the routing path in response to a control input signal*”

received from another module from the plurality of modules when the end module is coupled to the another module” [1F].

a. “Second Serial Chain Route” [1E]

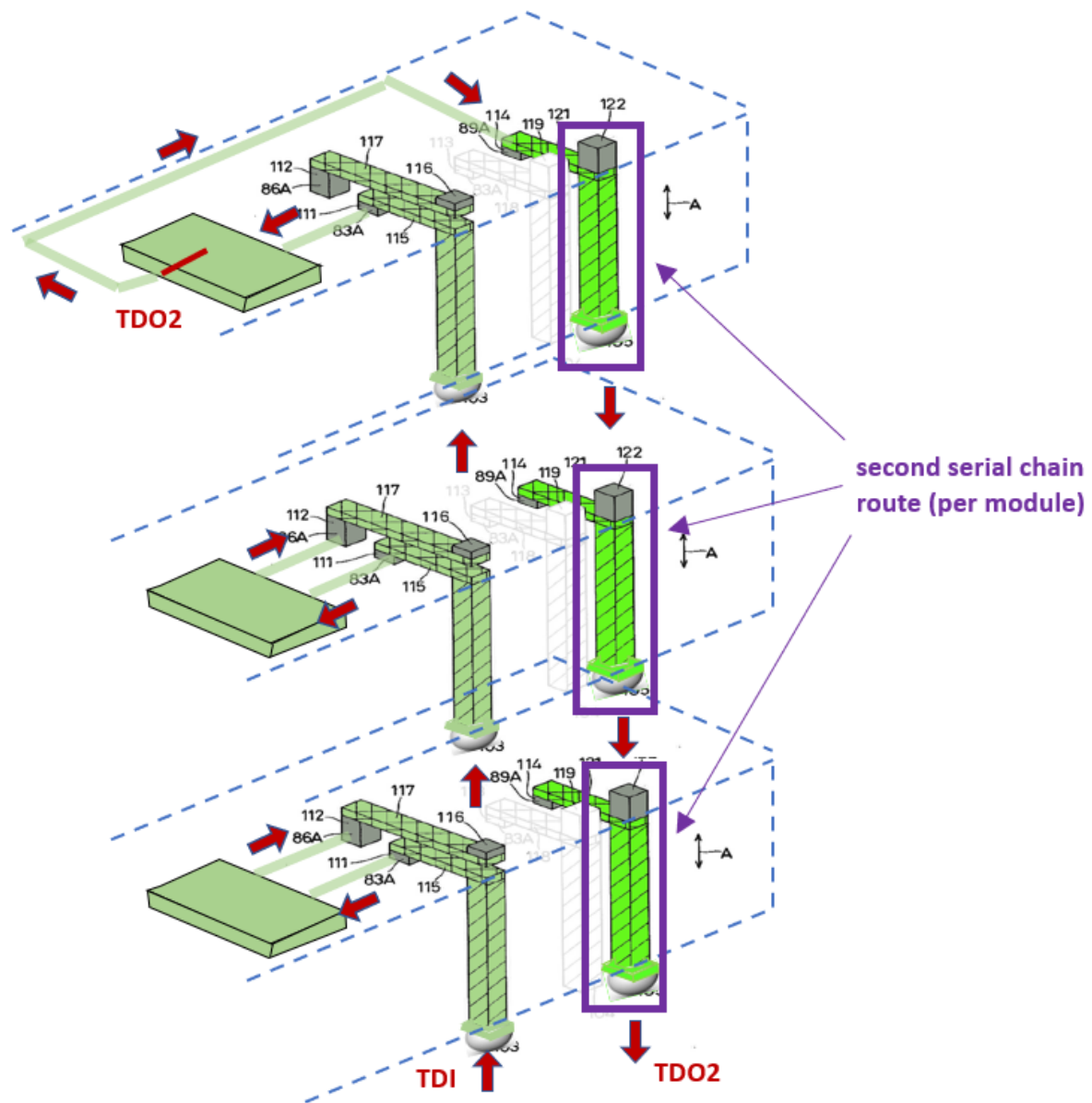
The combination of Hosomi and Sato discloses a “*second serial chain route.*” (INTEL-1003, ¶¶130-134.) Unlike the “*first serial chain route*” [1D], the “*second serial chain route*” does not require “*at least one serial chain connection.*” However, should PO contend the “*second serial chain route*” requires one or more “*serial chain connections*”, the combination of Hosomi and Sato meets the claim limitation for the reasons detailed below.

During a boundary scan, illustrated in Figure 3 below, in the top (rightmost) controller, TDI is output to the **TDO2** signal line which is connected to bus 102d and output to the external tester. (See INTEL-1009, 19:21-23, 20:20-23.)



Sato, Annotated Figure 3

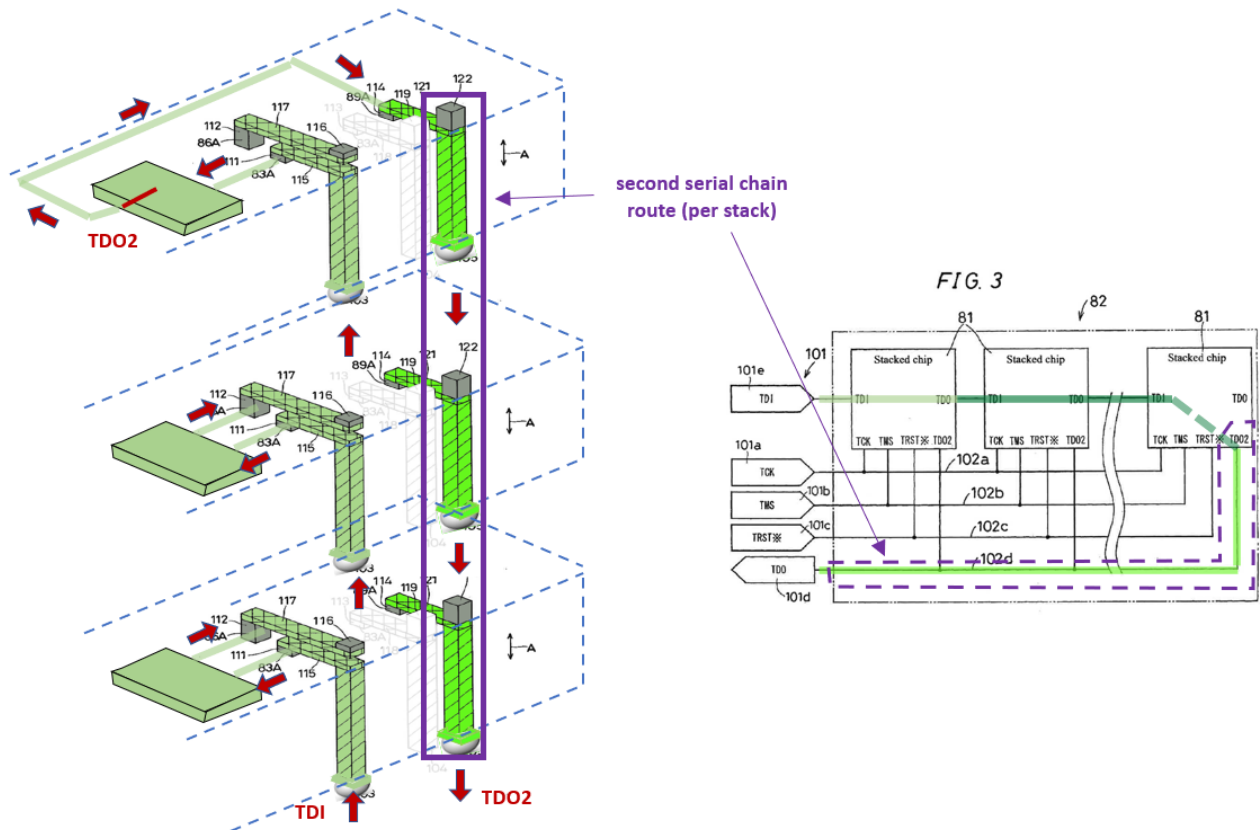
Petitioner’s “Plurality of Modules” Construction: The TDO2 portion of the daisy chain in the combination of Hosomi and Sato is illustrated in Thompson Figure H. As shown, in each module, the TDO2 signal passes through terminal (pad) 122, electrode (via) 105, and connecting pad/ball to either an adjacent module or the external tester. The pad-via-ball structure in each module in the combination of Hosomi and Sato is a “*serial chain connection*” and each device therefore has a “*second serial chain route*” as required by Petitioner’s “*plurality of modules*” construction. (INTEL-1003, ¶132.)



Thompson, Figure H: Petitioner's Construction

PO's “Plurality of Modules” Construction: The “*stacked module*” includes a path for carrying TDO2 down the stack to the external tester consisting of multiple “*serial chain connections*” (pad-via-ball structures) as shown below in Thompson Figure I. Thus, the combination of Hosomi and Sato discloses “a

second serial chain route” under PO’s construction requiring a single “*route*” for the entire stack. (INTEL-1003, ¶133.)



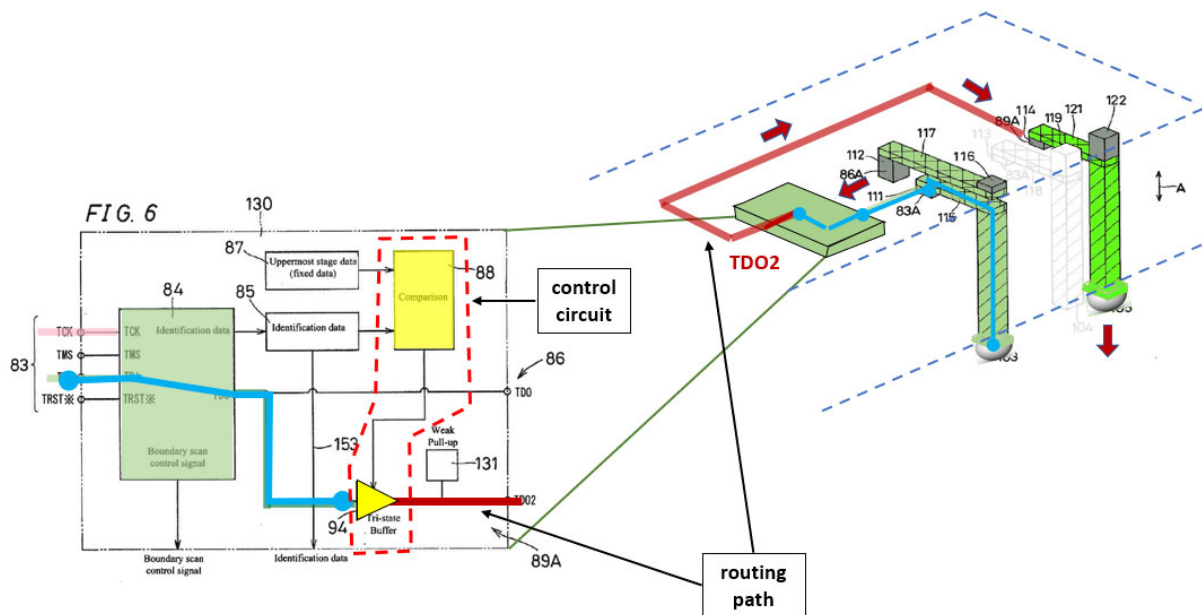
Thompson, Figure I (left): PO's Construction (left)
Sato, Annotated Figure 3 (right)

b. Control Circuit Limitations

(i) ***“Control Circuit”***

The combination of Hosomi and Sato also discloses “*a control circuit for enabling a routing path*” [1E]. (INTEL-1003, ¶135.) The data derivation part 89A of each boundary scan controller includes tristate buffer 94, pull-up means 131 and

signal line TDO2. (Sato, 25:19-20; Figure 6 (below left).) Comparison means 88 and tristate buffer 94 (shaded yellow) are part of “a control circuit” because they coordinate to control whether data is output on signal line TDO2, as discussed further below. (INTEL-1003, ¶¶135-139.)

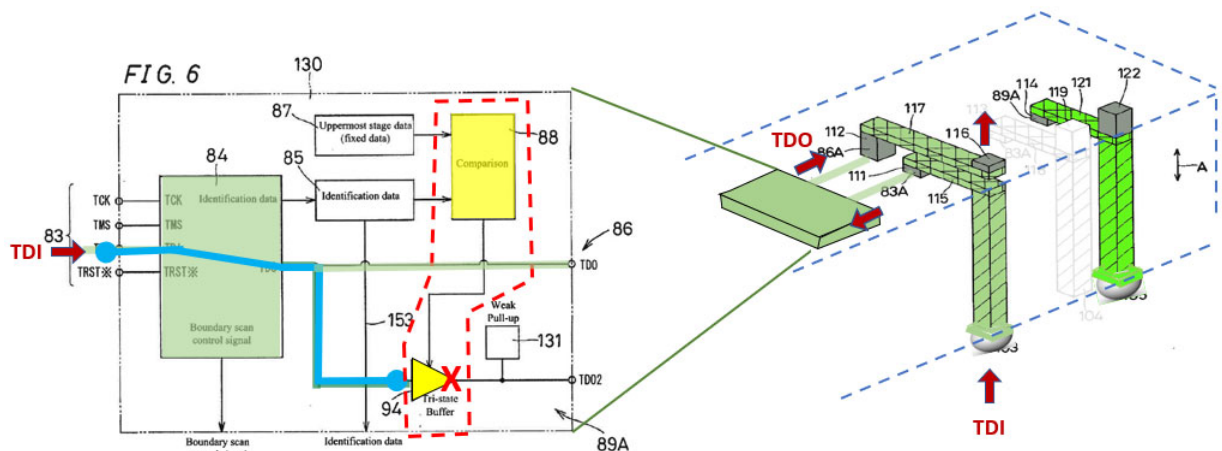


Sato, Annotated Figure 6 (top module); Annotated Figure 5

Specifically, comparison means 88 compares the received identification data with preconfigured identification data and outputs a result which is used as the control input of tristate buffer 94. (INTEL-1009, 16:12-15.) During a boundary scan, a match occurs only in the top module (the “boundary” of the stack). (INTEL-1003, ¶137.) Therefore, in the top module (an “end module” for the stack), the comparison result (match condition) turns on the tristate buffer causing the

output of control means 84 (TDO) to be output on signal line TDO2. (See INTEL-1009, 19:21-23.) In the combination, TDO2 from the controller connects to terminal (pad) 114 on the module substrate and then to terminal (pad) 122 through connection line 121. The path from the tristate buffer output to terminal 122 (shaded red above) is a “*routing path*” for boundary scan data from the controller to the TDO2 bus. (INTEL-1003, ¶137.) The combination of Hosomi and Sato therefore discloses “*a control circuit for enabling a routing path ... within an end module.*” (INTEL-1003, ¶¶137-139.)

In the other modules in the combined “*stacked module*”, as illustrated below, the comparison result (mismatch condition) prevents tristate buffer 94 from outputting input data on signal line TDO2 and therefore prevents output of data on the path to terminal (pad) 122. (See INTEL-1009, 25:26-28.) Thus, the routing path is not enabled in modules other than the top module. (INTEL-1003, ¶138.)

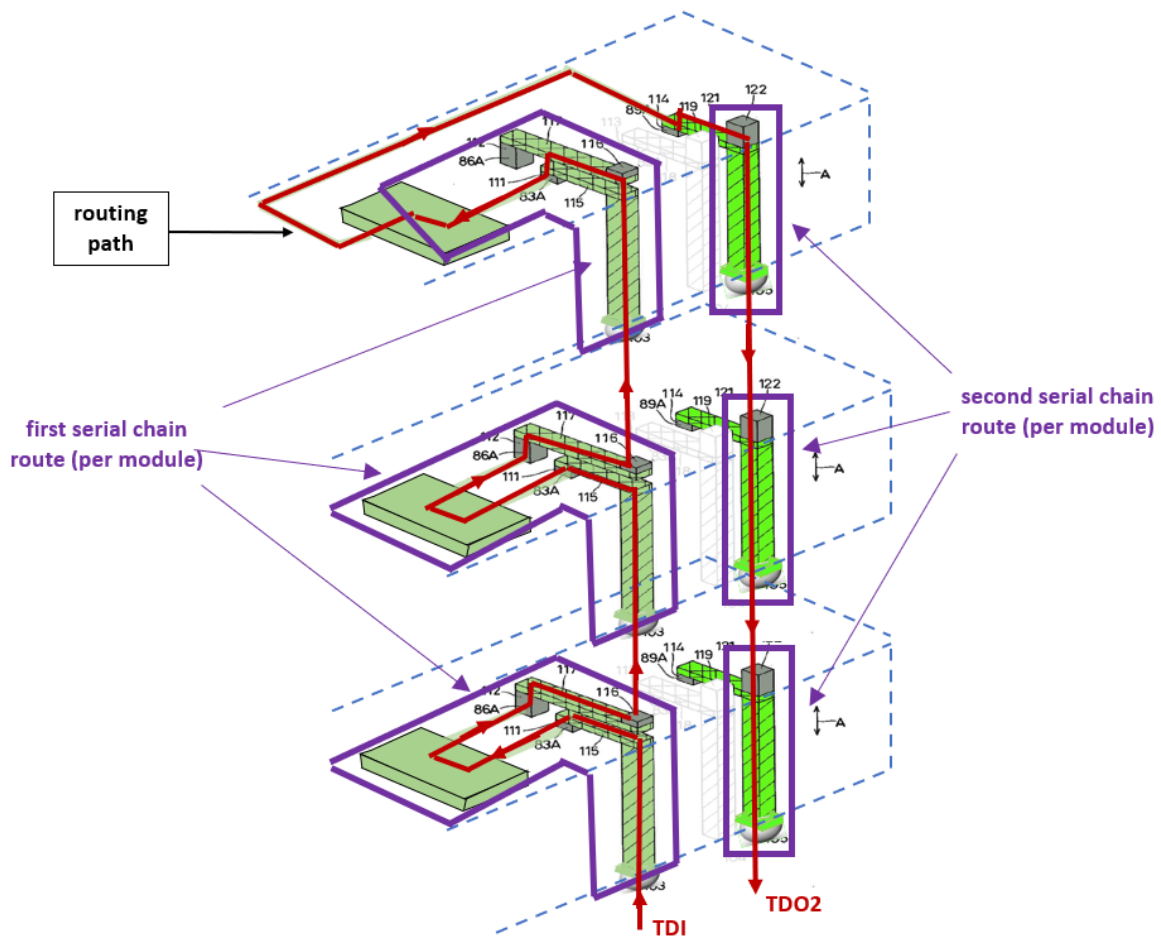


Sato, Annotated Figure 6 (other modules); Annotated Figure 5

(ii) ***“Connects the first serial chain route with second serial chain route”*** [1E].

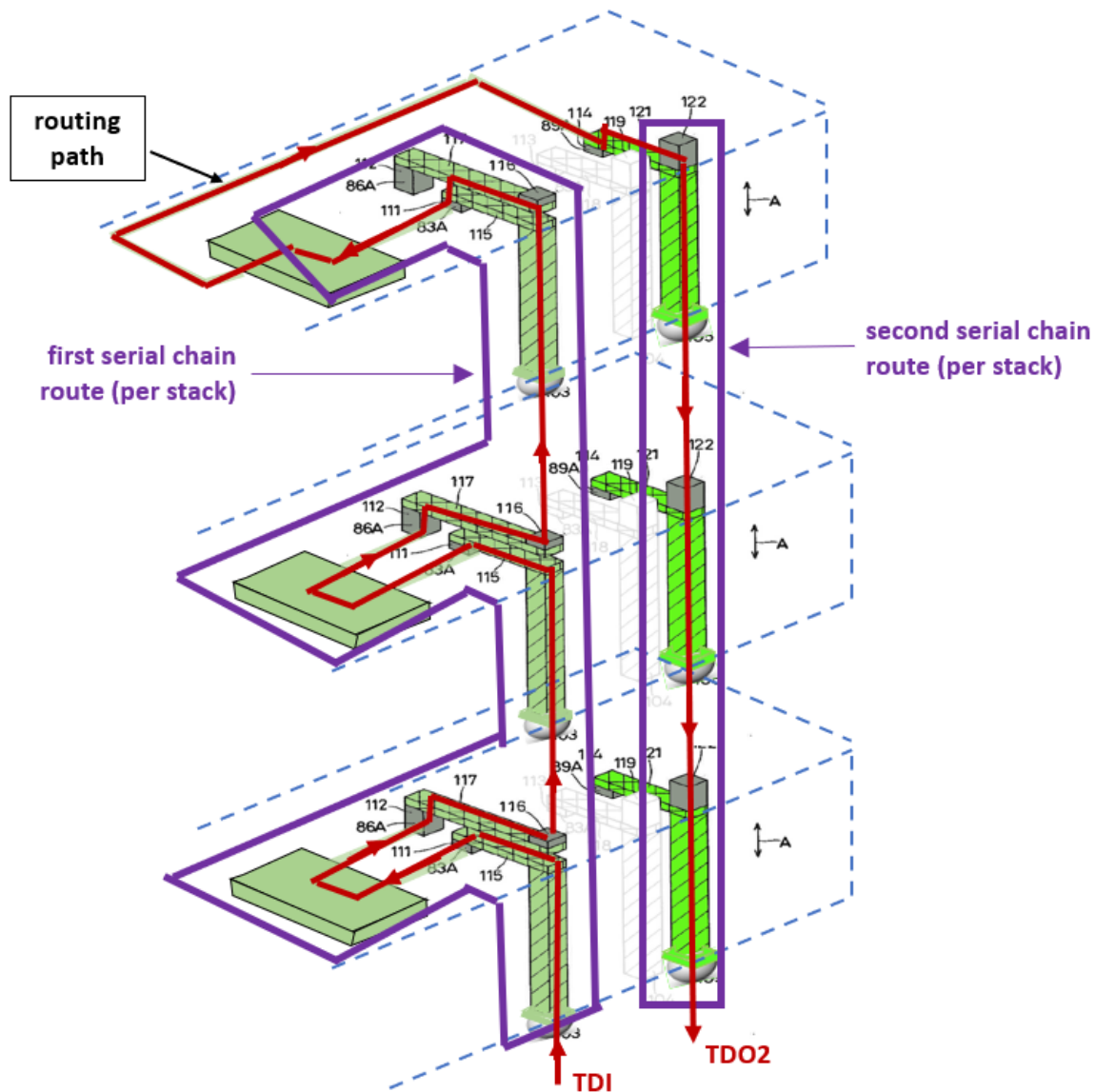
The combination of Hosomi and Sato discloses the “*control circuit*” “*connects the first serial chain route with the second serial chain route within an end module*” [1E]. (INTEL-1003, ¶¶140-144.)

Petitioner’s “*Plurality of Modules*” Construction: As shown in Thompson Figure J, a match condition in the top module during a boundary scan turns on the tri-state buffer (as discussed above) which causes the “*first serial route connection*” in the top module to be coupled to the “*second serial route connection*” in the top module. (INTEL-1003, ¶141.) Thus, the combination of Hosomi and Sato discloses “*a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module*” [1E] under Petitioner’s “*plurality of modules*” construction which requires a first and second “*serial route connection*” in each stacked device. (*Id.*)



Thompson, Figure J: Petitioner's Construction

PO's “Plurality of Modules” Construction: Similarly, as shown in Thompson Figure K, the match condition in the top module turns on the tri-state buffer coupling the “*first serial route connection*” for the stack to the “*second serial route connection*” for the stack via the routing path in the top device, meeting limitation [1E] under PO's construction requiring a single first and second serial route for the entire stack. (INTEL-1003, ¶142.)

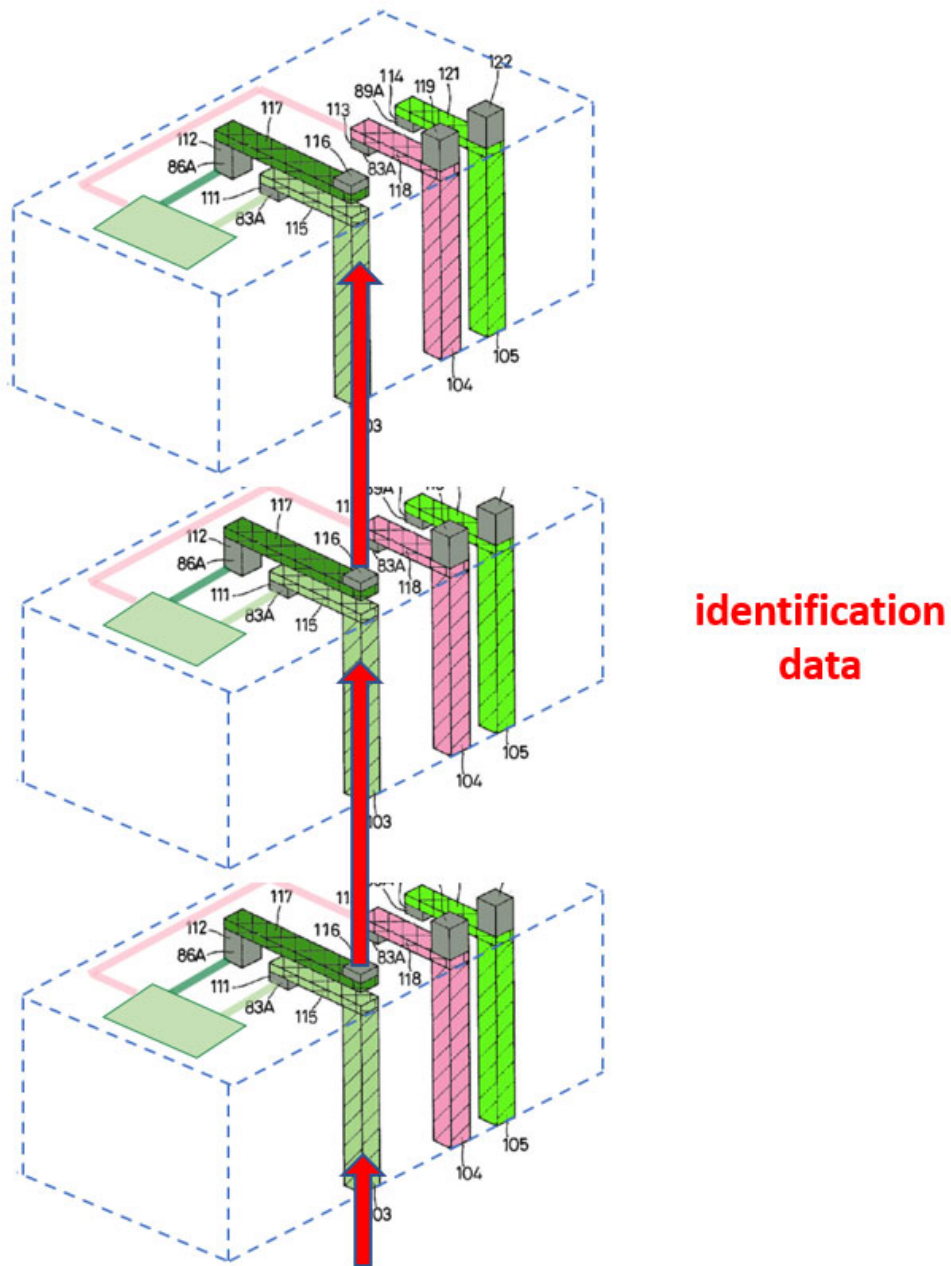


Thompson, Figure K: PO's Construction

(iii) “Control Input Signal” Limitation [1F].

The comparison means, which controls the tristate buffer and is part of the “control circuit”, uses identification data input via signal line TDI. (INTEL-1009, 14:9-10 (“The signal line TDI is a signal line which serially inputs the identification data”).) This identification data is a “control input signal” to the

“*control circuit*” because it determines whether the routing path from TDO to TDO2 is enabled in a module. (INTEL-1003, ¶143.) As illustrated below in Thompson Figure L, identification data are routed up to the top module through the other modules (each of which comprise “*another module*”) in the stack via the daisy-chain path of TDI signal lines (discussed above). (*Id.*) Thus, the “*control input signal*” is “*received from another module.*” (*Id.*)



Thompson, Figure L

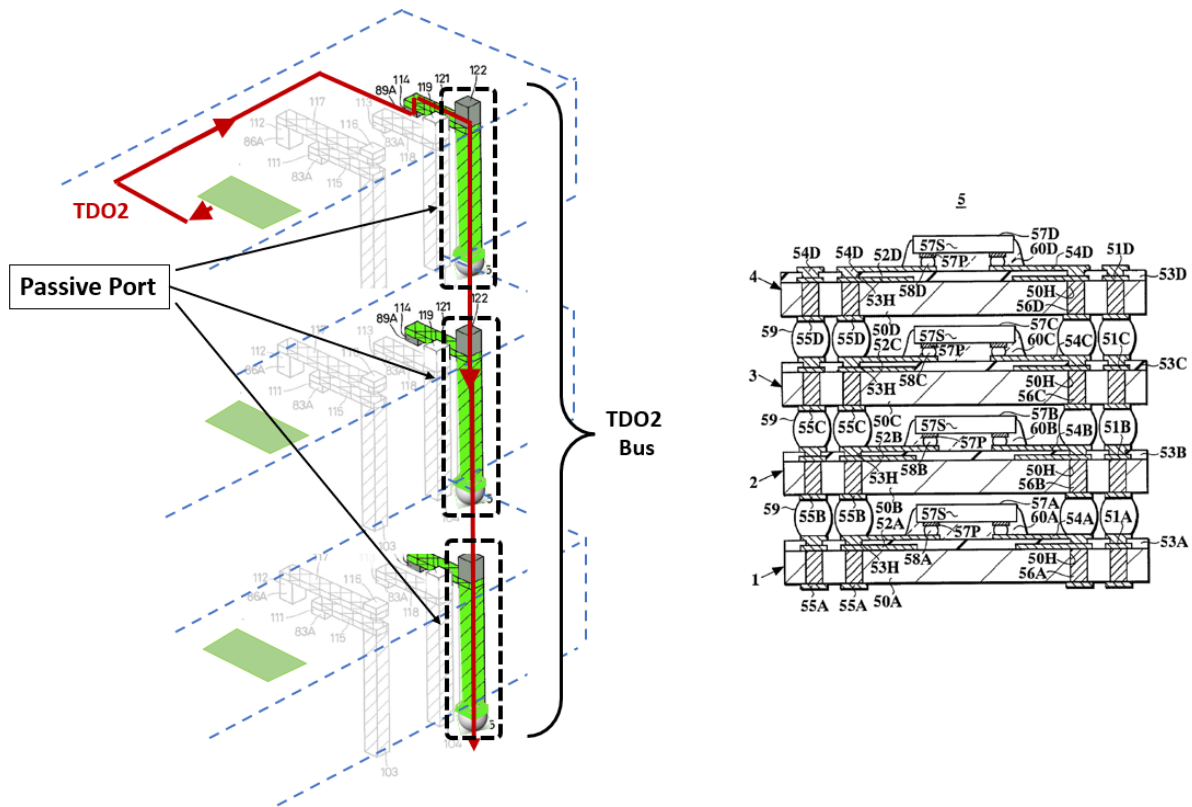
Accordingly, the combination of Hosomi and Sato discloses “*said control circuit is disposed to enable the routing path in response to a control input signal*”

received from another module from the plurality of modules when the end module is coupled to the another module” [1F]. (INTEL-1003, ¶¶143-144.)

C. Claim 2

For the reasons discussed in §V.B.3 for limitation [1C], the combination of Hosomi and Sato discloses “*the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module*” [2B]. (INTEL-1003, ¶145.)

The passive ports in the combination of Hosomi and Sato “*form[] a ladder like routing path*” [2A] because they create a series of “rungs” allowing a signal to pass horizontally in each module and to travel up or down the stack, as shown by Hosomi’s Figure 5 (right) and Thompson Figure M. (INTEL-1003, ¶146; *see also*, §V.B.3.)



Thompson, Figure M (left); Hosomi, Figure 5 (right)

D. Claims 11 and 12

The combination of Hosomi and Sato discloses that “one or more of the plurality of modules includes a main board” [11] and the “one or more vertically stacked module is connected to the main board” [12]. (INTEL-1003, ¶¶147-150.)

As discussed in §V.B.1, Hosomi discloses a stacked module having a plurality of SDRAM modules. Hosomi discloses this stacked memory module receives signals and transmits signals during memory read and write operations. (See, e.g., INTEL-1007, ¶¶121-127.) Hosomi does not explicitly disclose its

stacked module is mounted on a main board. Sato however explicitly teaches a stacked module “mounted on the circuit board.” (INTEL-1009, 16:6-7.)

A POSITA would have been motivated to mount the stacked SDRAM memory module having JTAG boundary scan functionality of the combination of Hosomi and Sato on a “*main board*” as taught by Sato. (INTEL-1003, ¶149.) Hosomi suggests this combination describing two prior art references that mounted 3-dimensional stacked memory packages on a printed circuit board. (See INTEL-1007, ¶¶19-20; FIGS. 18-19.) Sato also suggests the combination, repeatedly referring to receipt of external signals from an “external JTAG tester” and transmission of output signals to the tester, which would have indicated to a POSITA coupling of the stacked module to a main board carrying signals to and from the stacked module to the tester. (INTEL-1009, 14:11-12; 21:7-8; 8:10-12.) Further, a POSITA would have been further motivated to mount the stacked memory module on a circuit board because it was well-known prior to the ’243 patent that memory modules were designed to be mounted on a main board for use in devices such as computers, smartphones, and other electronic appliances. (INTEL-1003, ¶149, *citing* INTEL-1022, 44.)

When the “*stacked module*” is mounted on a main board, the main board is a “*module*” in the package. Therefore, the combination of Hosomi and Sato discloses “*one or more of the plurality of modules includes a main board*” [11] and the

“vertically stacked module is connected to the main board” [12]. (INTEL-1003, ¶¶147-150.)

VI. GROUND 2: Combination of Sung and Watanabe Renders Claims 1, 2, 11, and 12 Obvious.

A. Combination Overview

1. Sung

Sung’s describes “three-dimensional integrated circuit systems in which all of the dies, in a vertically bonded stack of dies, are identical.” (INTEL-1010, Abstract.) To achieve communication between identical stacked components, Sung provides connector 100. (*See* INTEL-1010, ¶¶43-44; Figure 2 below.) Connector 100 includes bi-directional vertical conductor 2 “situated equally between two terminators 4 [shaded blue].” (INTEL-1010, ¶44.) Electrical connection 102 “exist[s] between each terminal 4” and a conditional electrical connection 104 can exist between a pad coupled to vertical conductor 2 and a terminal 4. (*See Id.*)

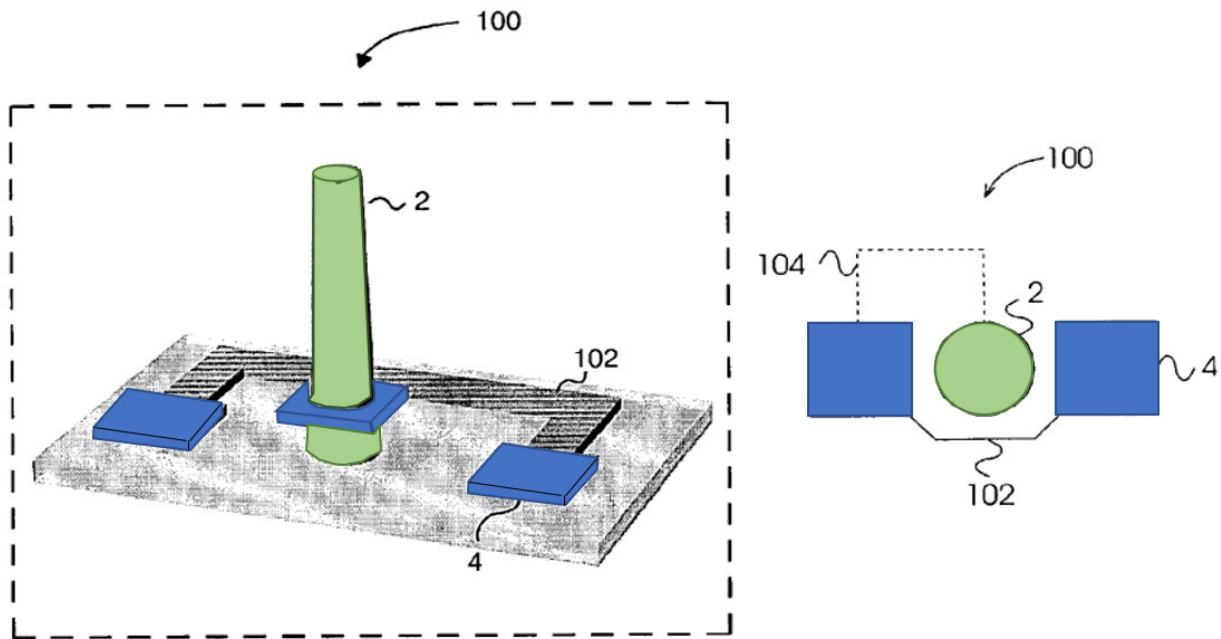


Figure 2: Model of a connector and associated symbol.

Sung, Annotated Figure 2

Connectors 100 permit “staggered alignment of alternating dies” which “facilitates the connection of signals from the current die to the die above, the die below or both dies.” (INTEL-1010, ¶44; Figure 3 (below).) The specific electrical interconnections are determined by the via interconnections of the metal layers present on each die. (See INTEL-1010, ¶¶43, 47; Figures 1, 3; INTEL-1003, ¶155.)

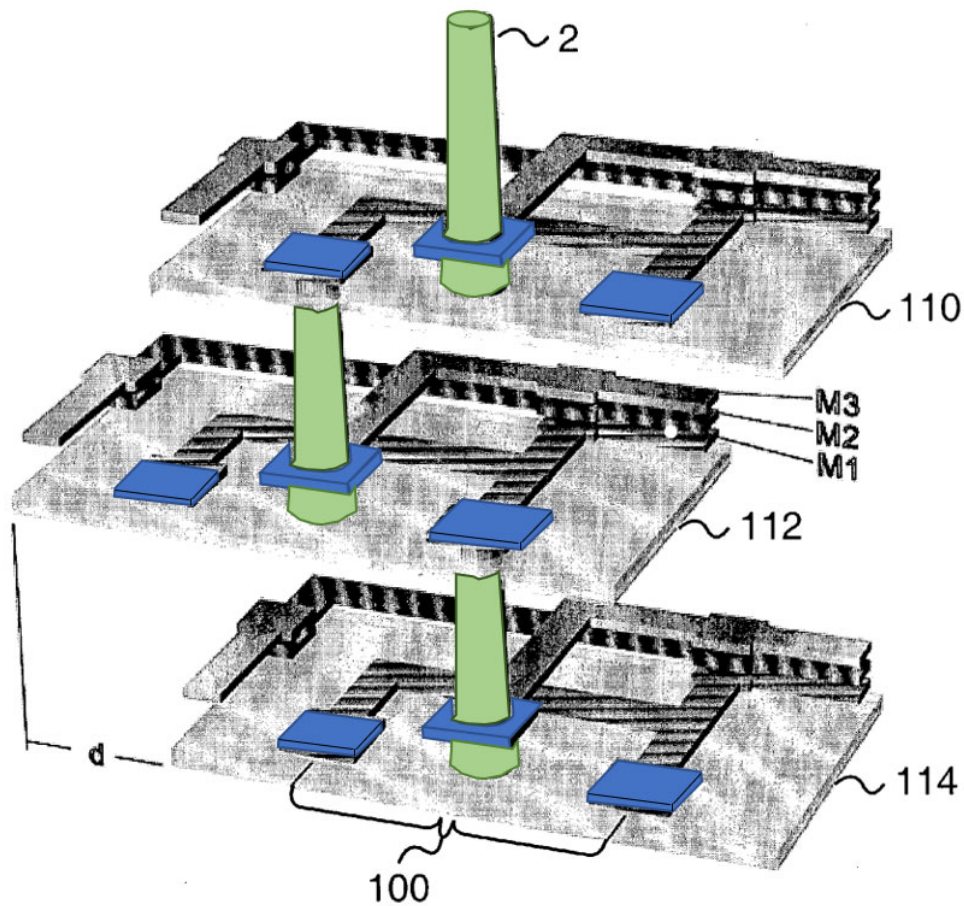


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

Sung, Annotated Figure 3

Connector 100 provides a generic building block to design a variety of interlayer routing circuits including broadcasting circuit 250 and die identification circuit group 270. (See INTEL-1010, ¶¶46-47; Figure 6 below.) Sung further discloses a communication network usable to implement scan chains 290. (INTEL-1010, ¶49.) The data output by these inter-die networks are provided to system components (e.g., processor, graphics controller, etc.) and are used by external

components for functions such as boundary scan testing and validation. (INTEL-1003, ¶157.)

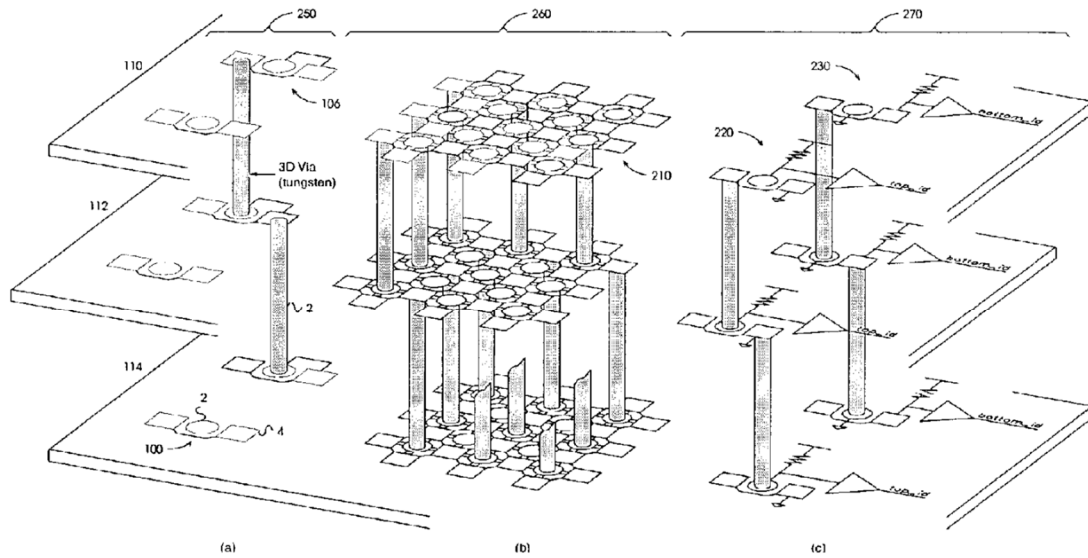
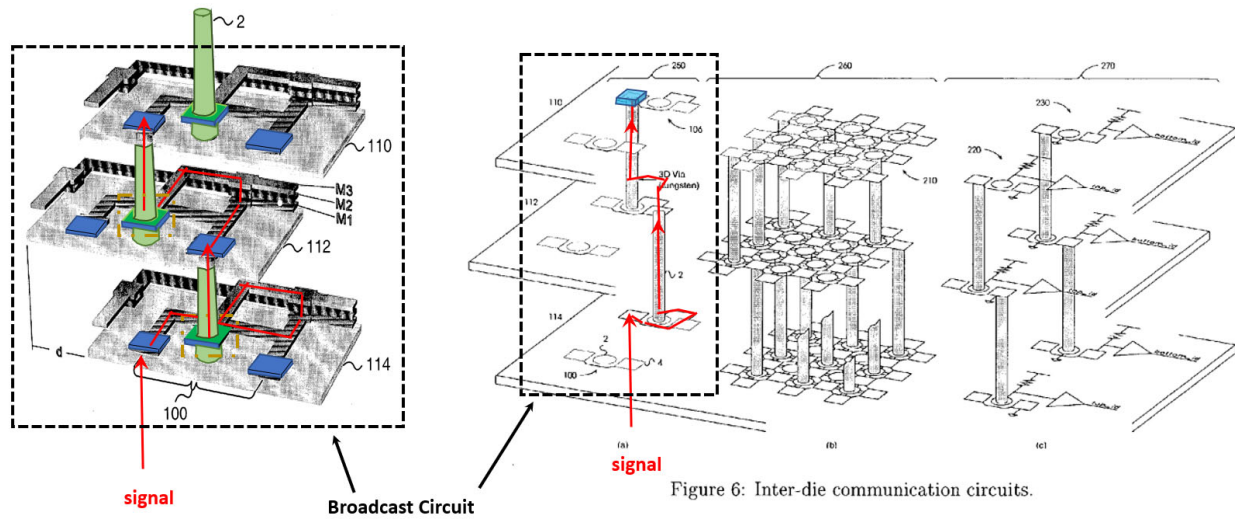


Figure 6: Inter-die communication circuits.

Sung, Figure 6

a. Broadcast Circuit

Broadcasting circuit 250, illustrated below right, “sends a signal to all dies within the stack” using connectors 100. (INTEL-1010, ¶47.) The broadcast signal travels up the stack when a signal is applied to the bottom stack layer. (INTEL-1003, ¶158.) Alternatively, the broadcast signal travels down the stack when the signal is applied to the top. (*Id.*)



Sung, Annotated Figures 3 (left) and 6 (right)

b. Boundary Scan Chain

An exemplary inter-die boundary scan network 290 across three dies 110, 112, and 114 is depicted in Figure 10 below. (INTEL-1010, ¶49.) The scan chain path “relies upon the identification of both the top die 110 and bottom die 114 in the stack, to prevent data from flowing past the stack boundaries.” (*Id.*)

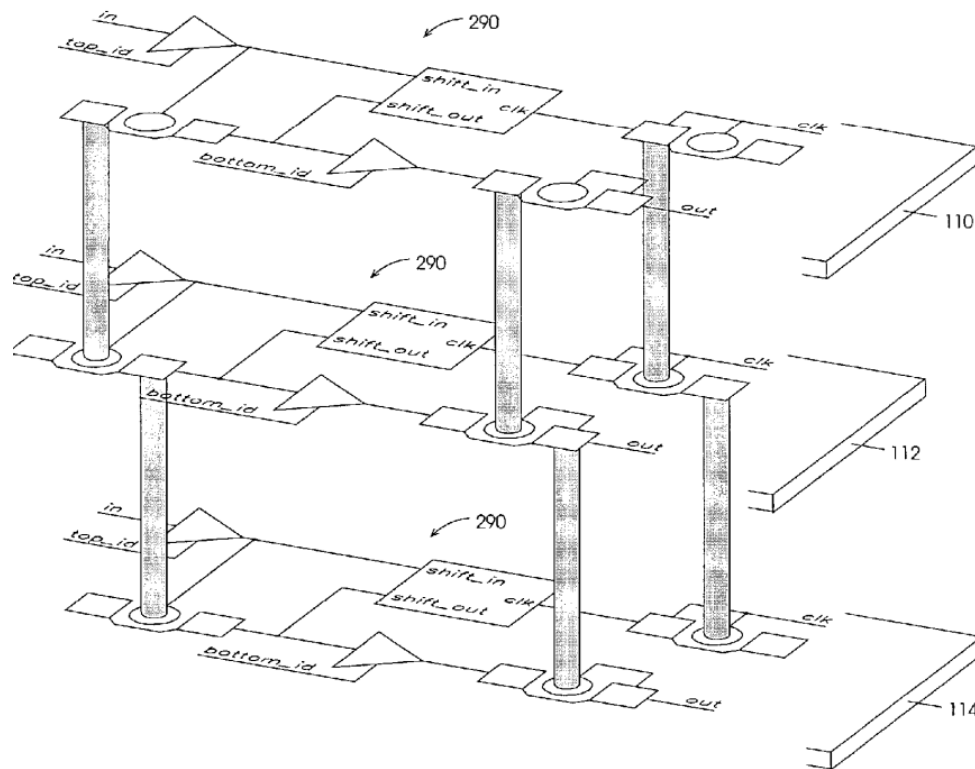


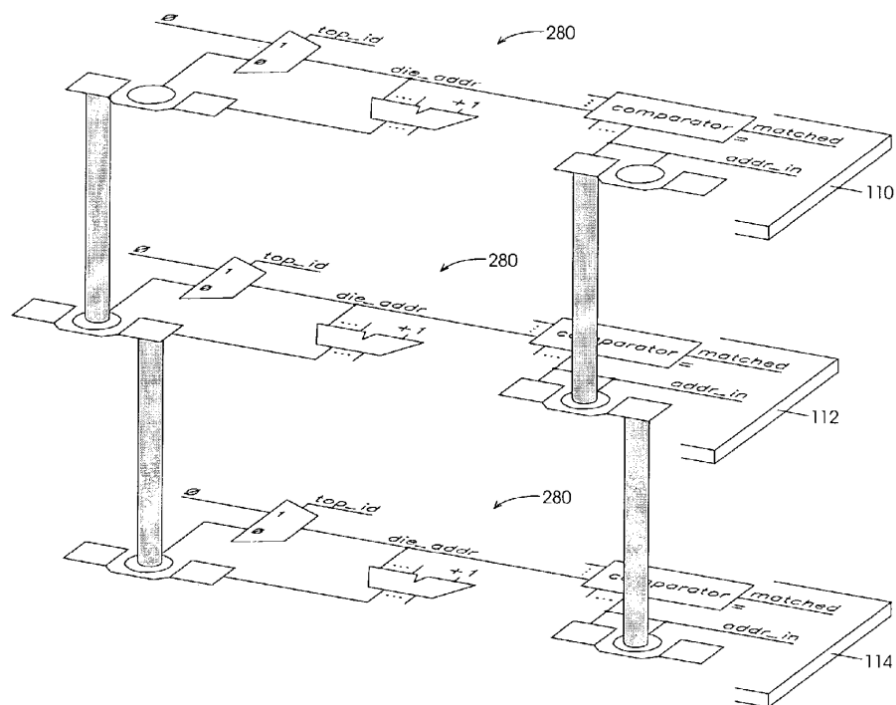
Figure 10: Inter-die communications chain for multiple dies.

Sung, Figure 10

In the boundary scan circuit, an external signal (“IN”) is applied to an input pad (not shown) coupled to tri-state buffer 292 which “is controlled by the result (top_id) of the top die identifier circuit 220.” (INTEL-1010, ¶49.) Because the die is at the top of the stack, the IN signal is coupled by the tri-state buffer to shift_in of register 294. (*See Id.*) Shift_out “is coupled to the die below 112 through a connector 100.” (*Id.*) In middle die 112, “shift_out is coupled to the die below 114 through the connector 100.” (*Id.*) On bottom die 114, shift_out is coupled by tristate buffer 296 to broadcasting circuit 250. (*Id.*)

c. Addressing Circuit

Sung further describes a method for “addressing one die in a vertical stack of like dies.” (INTEL-1010, ¶¶22-23.) As shown in Figure 9 (below), “the top die sets its address to zero, increments the address by one and passes it down.” (INTEL-1010, ¶48.) The middle die “make[s] the passed-in address its own, then increment[s] it and pass[es] it down.” (*Id.*) A die “respond[s] when the input broadcast address *addr_in*”, provided to each die by a broadcast circuit (not shown), “matches the die address *die_addr*.” (*Id.*)



Sung, Figure 9

2. Watanabe

Watanabe relates to “semiconductor device packaging technology.”

(INTEL-1011, 1:16-17.) Watanabe explains a “first level assembly” indicates an assembly “in which a semiconductor chip is mounted on a mounting base.”

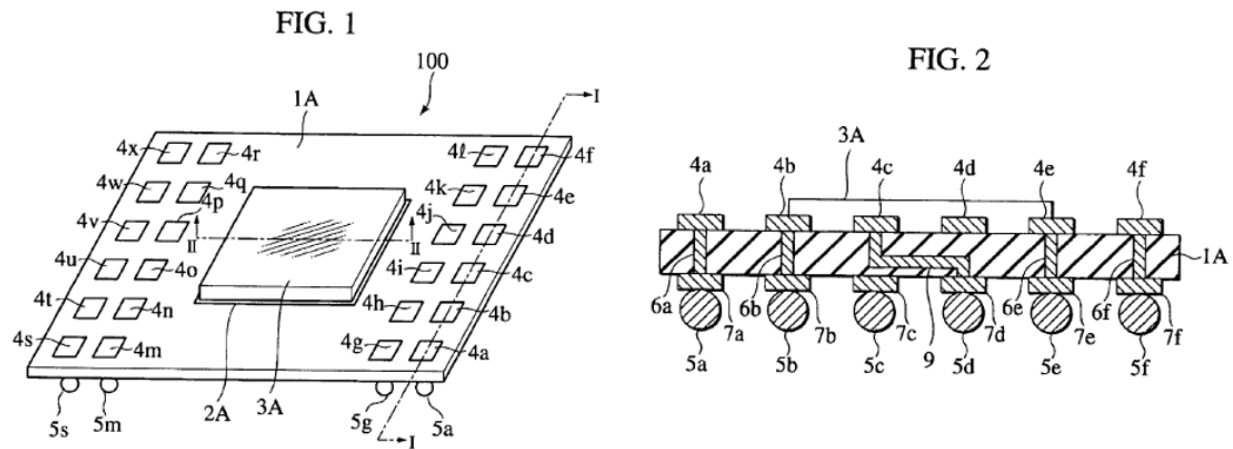
(INTEL-1011, 3:28-30.) Figure 1, below left, is an example of a one-layer first level assembly and Figure 2, below right, is a side view of the assembly from line I-I. (*See* INTEL-1011, 2:35-40.) The bottom surface of Watanabe’s mounting base¹¹ 1A includes lands¹² 7a-x on which balls are formed. (INTEL-1011, 3:43-44; 3:52-54.) Second lands are disposed on the upper surface of substrate opposite the first lands. (INTEL-1011, 3:45-47.) Through-holes¹³ 6a-x (referred to as “vias”) are embedded in the substrate to connect first lands 7a-x to second lands 4a-x.

¹¹ A “mounting base” is commonly referred to as a substrate. (INTEL-1003, ¶165.)

¹² Lands are commonly referred to as “pads.” (INTEL-1003, ¶163, *citing* INTEL-1013, 602, 604.)

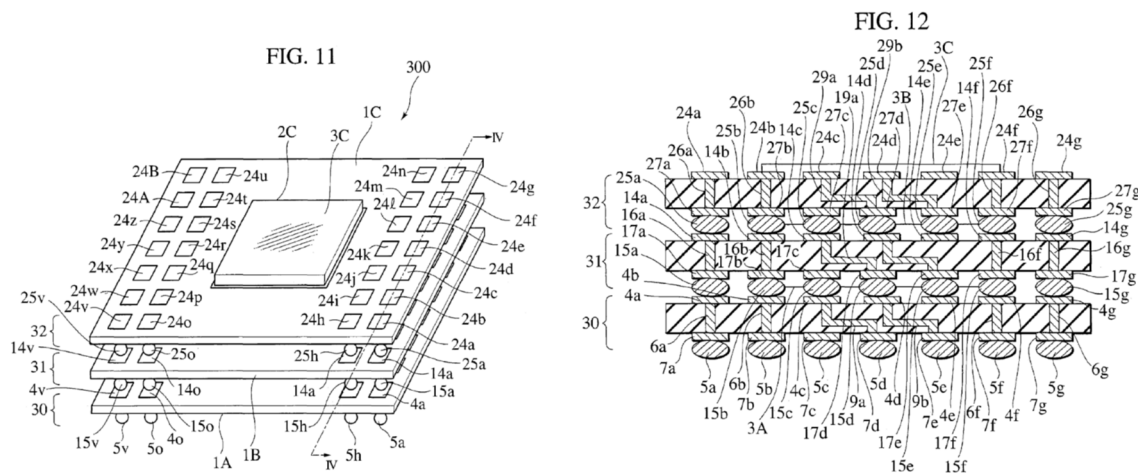
¹³ Through-holes filled with conductive material, shown in Figure 2, are commonly known as “vias.” (INTEL-1003, ¶¶165, 43-44, *citing* INTEL-1012, 444; INTEL-1013, 607.)

(INTEL-1011, 3:47-50.) Thus, the pad-via-ball configuration of Watanabe transfers a signal from one surface of a module to the opposite surface. (INTEL-1003, ¶165.)



Watanabe, Figures 1 and 2

The first level assembly of Figures 11 and 12 has multiple layers. As shown, balls on the lower surface of the middle layer are coupled to pads on the upper surface of the bottom layer. (INTEL-1003, ¶166.) Similarly, balls on the lower surface of the upper layer are coupled to pads on the upper surface of the middle layer. (*Id.*) These connections allow a signal to be communicated between layers. (*Id.*)

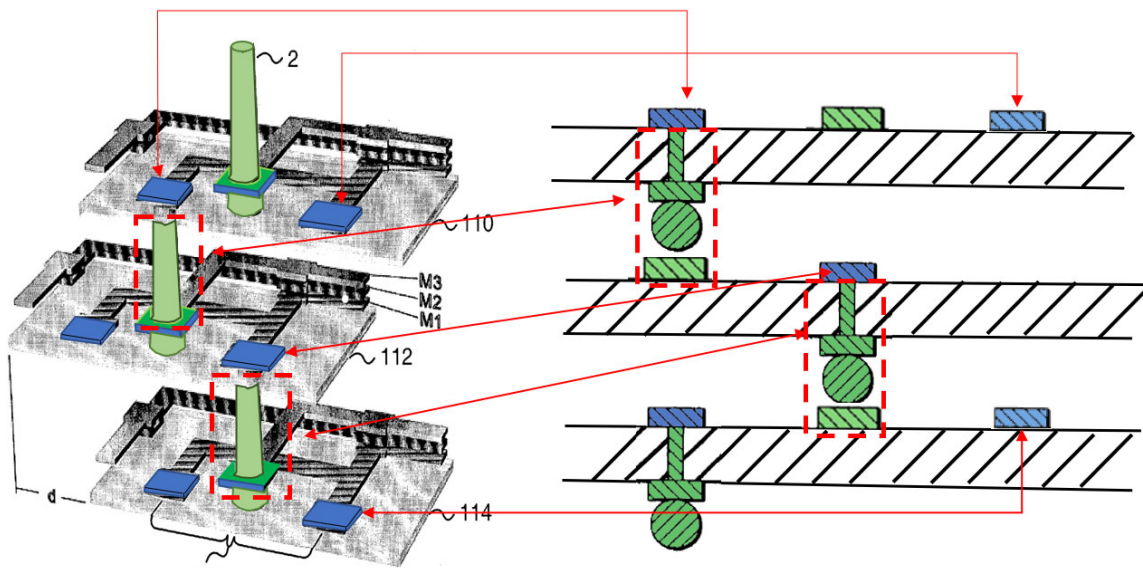


Watanabe, Figures 11 and 12

B. Combination of Sung and Watanabe

A POSITA would have been motivated to use Watanabe's pad-via-ball structure to implement connections between modules in Sung's stacked module, as illustrated below for an exemplary broadcasting circuit (Sung's Figure 3 left). (INTEL-1003, ¶¶169-182.) Specifically, a POSITA would have been motivated to use Watanabe's vias to provide bi-directional connection through a module substrate, like bi-directional vertical conductors of connector 100 provide connection through a die. (INTEL-1003, ¶169; *see also*, INTEL-1010, ¶44.) The use of vias is consistent with Sung which claims its multichip module substrates include "vias formed through apertures that extend through the thickness of the thin film structures and the rigid support base." (INTEL-1010, claim 15.) A POSITA would have further used a pad/ball on the bottom surface of Sung's module, connected to a via, for coupling with a pad on the upper surface of an

adjacent module, as taught by Watanabe, and shown below right in Thompson Figure N. (INTEL-1003, ¶169, *citing* INTEL-1012, 154 (explaining pad/ball connections used on packages and chips).)



Sung, Annotated Figure 3; Thompson, Figure N

A POSITA would have been motivated to make the above combination for numerous reasons. First, Sung teaches embodiments in which its teachings are applied to “stacked multi-chip modules”, “stacked system modules,” and “multichip module substrates.” (INTEL-1010, ¶52; claims 13-15.) However, Sung provides minimal details regarding how to interconnect such modules. (INTEL-1003, ¶170.) A POSITA would have therefore been motivated to search for references describing interconnection techniques for stacked modules and would have been led to Watanabe, which is in the same field of endeavor as Sung and

the '243 patent—3-dimensional packaging. (*See* INTEL-1010, ¶52; INTEL-1011, 5:57-58; INTEL-1001, 1:32-45.) Both Sung and Watanabe are further reasonably pertinent to a problem addressed by the '243 patent—maximizing “capacity in a limited area.” (INTEL-1001, 1:21-24; INTEL-1003, ¶171.) Sung’s stacking technique is designed to increase “data storage density” while Watanabe’s stacking technique is aimed at realizing “high density packaging.” (INTEL-1010 ¶6; INTEL-1011, 1:52–54.)

Second, Sung provides express motivations that would have led a POSITA to use Watanabe’s pad-via-ball structure as the inter-module connection structure. (INTEL-1003, ¶¶172-174.) Sung notes the techniques presented “can be adapted to any stackable integrated circuit technology that allows vertical interconnections between adjacent dies.” (*See*, INTEL-1010, ¶43.) Sung further teaches existing manufacturing technology utilized “solder mounds” and “solder bumps”¹⁴ for interconnecting “layers of transistor circuits.” (*See* INTEL-1010, ¶3.) Sung further

¹⁴ A POSITA would have understood the terms “solder balls”, “solder bumps” and “solder mounds” were used prior to the '243 patent (and today) synonymously by POSITAs and refer to the same type of interconnection element. (INTEL-1003, ¶¶40, 173.)

teaches in its claims that inter-die vertical conductors include “interconnection members such as solder mounds” and the terminators are “3D via pads.” (INTEL-1010, claims 36, 39, ¶29.) A POSITA would have understood “via pads” were well known interconnection elements often used with solder balls/bumps for forming vertical interconnections in integrated circuits prior to the ’243 patent. (INTEL-1003, ¶174, *citing* INTEL-1013, 107-108; *see also*, INTEL-1012, 154.) A POSITA would have therefore been motivated based on these suggestions to use solder balls (equivalent to solder mounds) to electrically couple signal paths in two adjacent modules as taught by Watanabe. (INTEL-1003, ¶¶172-174.)

Third, a POSITA would have been motivated to combine the teachings of Watanabe and Sung as discussed above because the use of pad-ball interconnections and their advantages were well known long before the ’243 patent. (INTEL-1003, ¶¶175-176.) Pad-ball interconnections were pioneered by IBM in the 1960s and were “[t]he most popular attachment method” for making vertical interconnections. (INTEL-1003, ¶175, *citing* INTEL-1014, 31.) For example, this interconnection technique has been used in “flip chip” packaging for decades. (INTEL-1003, ¶175, *citing* INTEL-1012, 423.) In flip chip bonding, pads are metalized on a chip’s surface and a solder ball is deposited on each pad. (INTEL-1003, ¶175.) The chip is then flipped and aligned with pads on the board. (*Id.*) The balls are “remelted” to connect the ball to the pad on the board. (*Id.*) A

similar technique is used in 3-dimensional packaging to interconnect two modules, as taught by Watanabe. (INTEL-1003, ¶176.)

The advantages of pad-ball interconnection would have been well-known to a POSITA. (INTEL-1003, ¶176.) For example, because of the reduction in electrical path length and reduction of parasitic capacitance and inductance, pad-ball interconnections are well suited for high-density, high-performance applications. (*Id.*, citing INTEL-1013, 106-107.) Additionally, it was well known that pad-ball interconnections were easier to align than other types of connections (e.g., ball-to-ball), leading to lower manufacturing costs. (INTEL-1003, ¶176.)

Finally, the combination of Watanabe's pad-via-ball interconnection teachings with Sung is nothing more than the combination of prior art elements according to known methods to yield predictable results. *See KSR*, 550 U.S. at 416; INTEL-1003, ¶¶177-182. A POSITA would have understood how to combine the elements taught by Watanabe and Sung using known methods. (INTEL-1003, ¶177.) As discussed above, use of solder balls and corresponding bonding pads to form electrical interconnections was well-known and described in textbooks long before the '243 patent. (*Id.*, citing INTEL-1013, 106-108; INTEL-1014, 31; INTEL-1012, 153-154, 271-272, 423, 440-441.) Further, Sung and Watanabe both perform the same functions in the combination as they do separately. (INTEL-1003, ¶178.) For example, Watanabe's pad-via-ball interconnections provide an

electrical path through a module substrate and provide this same function in the combination. Sung provides techniques for routing signals between modules in a stacked configuration. Sung's routing techniques operate the same using Watanabe's pad-via-ball signal path as they do in Sung's stacked die embodiment. (INTEL-1003, ¶178.)

A POSITA would have recognized the results of the combination were predictable and would have had a reasonable expectation of success in the combination. (INTEL-1003, ¶¶179-182.) In fact, the '243 patent admits its module and package level stacking technology existed in the prior art: "[t]he present invention takes advantage of the **existing stacking technology both on the module and package level.**" (INTEL-1001, 1:59–60.) Thus, a POSITA would have understood how to use these existing techniques to integrate pad-via-ball signal paths through a module and pad-ball connections between modules into Sung's stacked module embodiment. (INTEL-1003, ¶¶179-182.)

C. Independent Claim 1

1. Preamble [1P] and "*Plurality of Modules*" [1A].

The combination of Sung and Watanabe discloses a "*stacked module*" [1P] that comprises "*a plurality of modules*" [1A]. (INTEL-1003, ¶¶183-193.)

Sung discloses a "[s]calable electronic circuit system composed of **stacked layers of the same or similar circuitry.**" (INTEL-1010, ¶2.) Although Sung

describes its techniques in the context of stacked dies or stacked integrated circuits, Sung’s “method of aligning and connecting together like wafers can be applied to: **stacked multi-chip modules ... stacked system modules**, stacked circuit subassemblies or any other stacked three-dimensional array of electronic circuitry.” (INTEL-1010, ¶52, *see also*, claim 6 (“layers are comprised of system modules”), claim 13 (“layers are comprised of multichip module substrates”).) The stack of modules in the combined system of Sung and Watanabe is the “*stacked module*” [1P] and comprises “*a plurality of modules*” [1A]. (INTEL-1003, ¶¶183-186.)

Each module in Sung’s “*stacked module*” includes the same or substantially the same circuitry. (INTEL-1003, ¶184.) One “object” of Sung is “to reuse the **same or similar integrated circuit design for each die** in a vertically bonded stack of dies.” (INTEL-1010, ¶15; *see also*, ¶25 (“The methods described enable scalable integrated circuit systems in which **circuits on different die**, in a vertical three-dimensional stack of dies, **are identical**”); ¶52.)

Additionally, the combination of Sung and Watanabe teaches or suggests each module in the “*stacked module*” is an SDRAM module¹⁵. (INTEL-1003,

¹⁵ Petitioner’s construction of “*passive port*” requires the modules to be SDRAM modules. (See §IV.C.2.)

¶¶187-193.) Sung does teach its stacking technique increases “data storage density” (¶42) and describes prior art “three-dimensional memories” which “stack separate layers of memory cells”(¶¶5–6). Watanabe discloses a stacked memory including multiple DRAM modules: “as the first level assembly 30 and the upper level assembly 31 shown in FIG. 9, **a DRAM ... the like are applicable.**” (See INTEL-1011, 7:67-8:8.) A POSITA would have understood that Watanabe’s reference to “DRAM” encompasses SDRAM. (INTEL-1003, ¶190.) DRAM is a type of memory that can be synchronous (i.e., SDRAM) or asynchronous. (INTEL-1003, ¶¶190-191.) A POSITA would have been motivated to use SDRAM as the DRAM in the stacked memory of Sung and Watanabe because SDRAM was easier to use than asynchronous DRAM and was widely deployed in devices such as desktop and laptop computers before the ’243 patent. (See INTEL-1012, 438; INTEL-1024, 338; INTEL-1003, ¶191.)

Additionally, a POSITA would have been motivated to stack SDRAM modules in a memory device to achieve higher memory capacity at lower cost. (INTEL-1003, ¶192.) Specifically, SDRAM provides the lowest cost per bit for a readable/writeable memory because it only requires one transistor to store a bit in each memory cell. (*Id.*, citing INTEL-1024, 312.) Finally, the use of SDRAM modules in the “*stacked module*” of Sung and Watanabe is merely the combination of prior art elements (Watanabe’s DRAM/SDRAM with Sung’s modules)

according to known methods to yield predictable results. *KSR*, 550 U.S. at 416; INTEL-1003, ¶193.

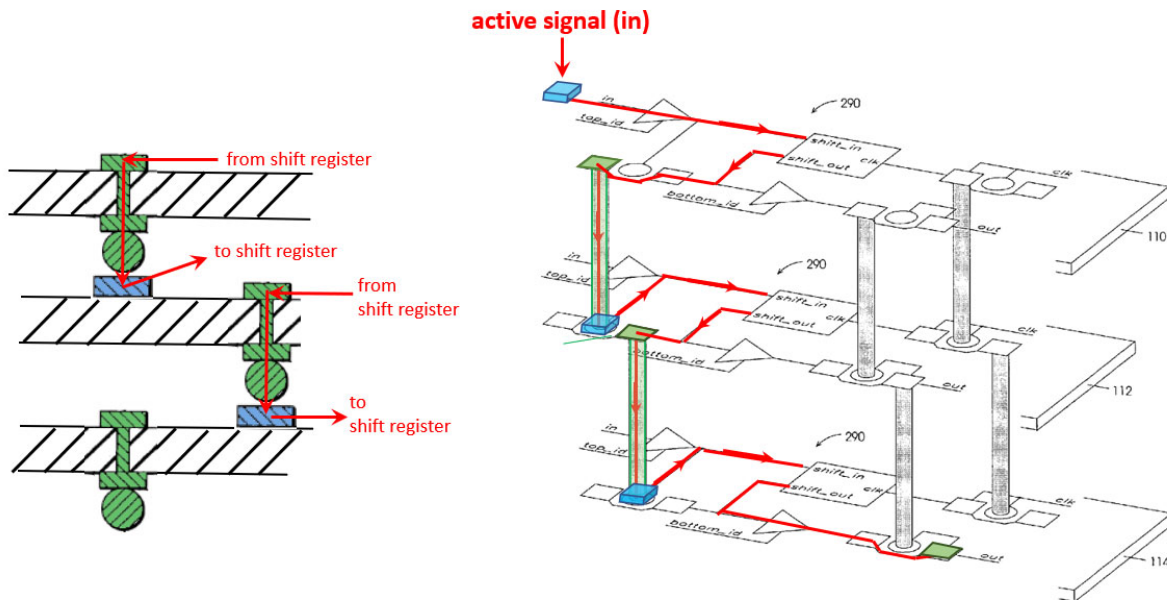
Petitioner establishes in §§IV.B.2.-5 that (1) each module includes the elements recited in limitations [1B]-[1F] as required by Petitioner’s construction of “*plurality of modules*” and (2) the “*stacked module*” includes these limitations as required by PO’s construction. (See §IV.C.1.)

2. “*One or More Active Ports*” [1B].

As discussed in §V.B.2, an “*active signal*” encompasses a signal applied to the stack by an external source and distributed via an “*active port*” (e.g., an “*active pad*”) to circuitry on a module. (INTEL-1003, ¶¶100-101, 194.) The combination of Sung and Watanabe discloses “*one or more active ports for carrying one or more active signal*” [1B]. (INTEL-1003, ¶¶194-197.)

Sung discloses numerous “*active signals*” carrying information, including the IN signal of the boundary scan chain of Figure 10 (below). As shown, the external IN signal is received as an input to a tri-state buffer on the top module of the stack. (See INTEL-1010, ¶49.) A POSITA would have understood the IN signal is received at a pad on the upper surface of the top module (added by Petitioner to Figure 10 below). (INTEL-1003, ¶194.) The pad on the top module receiving the external “IN” signal is an “*active port.*” (See INTEL-1001, 9:1-8;

INTEL-1005, 1 (“An **active pad** may be also referred to herein as an ‘**active port**’”); INTEL-1003, ¶194.)



Thompson, Figure O; Sung, Annotated Figure 10

Because the module receiving the external IN signal is the top module, the tri-state buffer couples the IN signal to shift_in of shift register 294. (See INTEL-1010, ¶49.) The active shift_out signal of the register is then “coupled to the die below 112 through a connector 100.” (*Id.*) Specifically, in the combination of Sung and Watanabe illustrated in Thompson Figure O and Sung’s Figure 10, the shift_out signal is applied to a pad on the upper surface of the top module (shaded green) and traverses through a via to a ball on the lower surface of the top module which is coupled to a pad (shaded blue) on the upper surface of the middle module

112. This pad receives and distributes the active signal to shift_in of the shift register on the middle module and is therefore an “*active port*” on the middle module. (INTEL-1003, ¶195.)

The shift_out signal is then “coupled to the die below 114 through connector 100.” (INTEL-1010, ¶49.) Specifically, like the top module, the shift_out signal from the shift register on the middle module is applied to a pad (shaded green) on the upper surface of the middle module and traverses through a via to a ball on the lower surface which is coupled to a pad (shaded blue) on the upper surface of the bottom module 114. This pad receives and distributes the signal to shift_in of the shift register and is therefore an “*active port*” on the bottom module. (INTEL-1003, ¶196.)

Thus, the combination of Sung and Watanabe discloses that each module in its “*stacked module*” includes “*one or more active ports for carrying one or more active signal*” [1B], as required by Petitioner’s “*plurality of modules*” construction. (INTEL-1003, ¶197.) The combination also discloses the “*stacked module*” includes this limitation, as required by PO’s construction. (INTEL-1003, ¶¶194-197.)

3. “*Passive Port*” [1C].

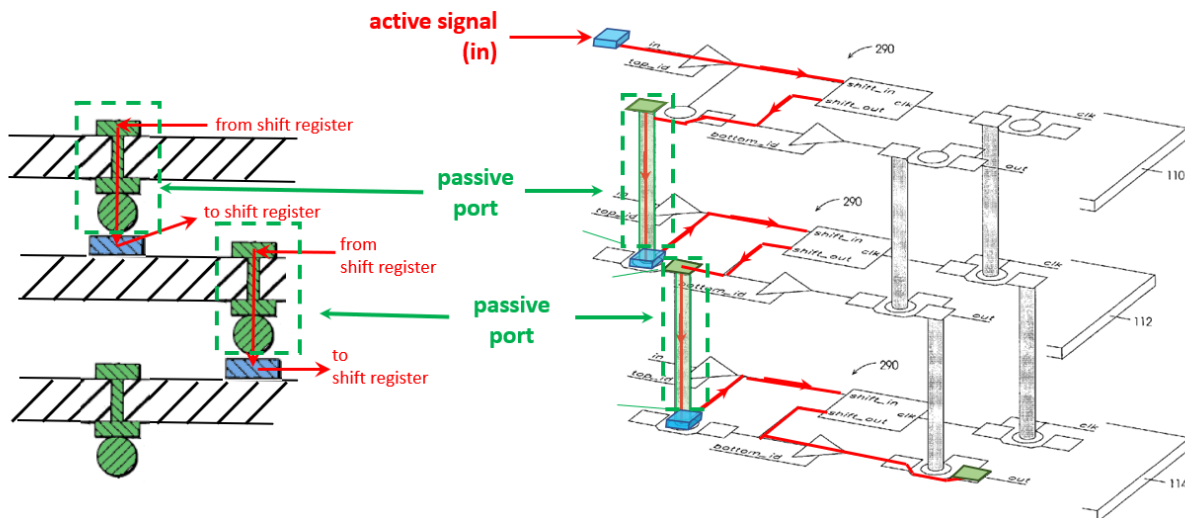
Limitation [1C] recites “*one or more passive ports for passing through the one or more active signals.*” The combination of Sung and Watanabe discloses

limitation [1C] under both Petitioner’s and PO’s constructions of “*passive port*”.

(See §IV.C.2.; INTEL-1003, ¶¶198-211.)

a. Petitioner’s “*Passive Port*” Construction.

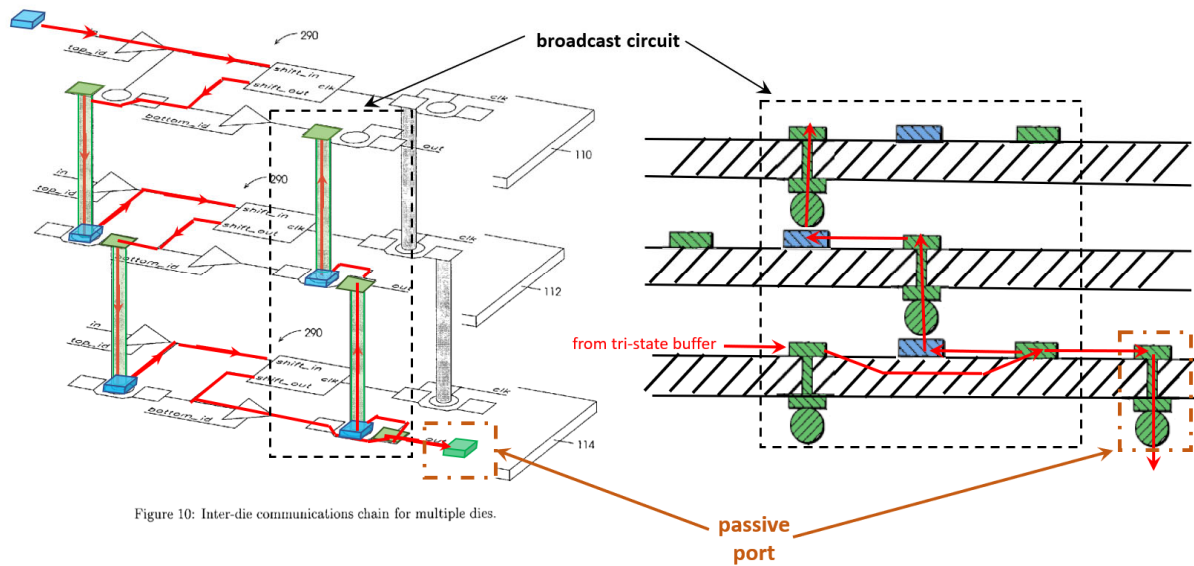
The combination of Sung and Watanabe discloses “*one or more passive ports*” in each module. (INTEL-1003, ¶¶199-207.) As illustrated in the figures below, in the scan chain communication circuit of the combination of Sung and Watanabe, the active shift_out signal from the top module’s shift register is applied to a pad on the upper surface of the top module (shaded green) and traverses through a via to a ball on the lower surface of the top module. (INTEL-1003, ¶¶200-201.) The pad-via-ball of the top module which carries the active shift_out signal to the middle module is a “*passive port*” on the top module. (INTEL-1003, ¶201.)



Thompson, Figure P; Sung, Annotated Figure 10

Similarly, the active shift_out signal from the middle module's shift register is applied to a pad on the upper surface of the middle module (shaded green) and traverses through a via to a ball on the lower surface of the middle module. (INTEL-1003, ¶202.) The pad-via-ball of the middle module which carries the active shift_out signal to the bottom module is a “*passive port*” on the middle module. (*Id.*)

On the bottom module, the signal is distributed through the shift register to a tristate buffer. (INTEL-1010, ¶49.) Because the module is a bottom (end) module, the tristate buffer couples the active shift_out signal to the module output. (*See* INTEL-1010, Figure 10.) Although not shown in Figure 10, a POSITA would have understood the output of the bottom module is coupled to a pad-via-ball structure which carries the active signal to an output terminal on a main board coupled to the “*stacked module*.” (*See* INTEL-1011, 11:25-27; Figures 13-14 (describing terminals on a main board carrying signals to/from a stacked assembly); INTEL-1003, ¶¶203-206, 248-257; *see also*, §VI.E (discussing connection of stacked module to main board in the combination).) The pad-via-ball interconnection in the bottom module carrying the active shift_out signal to a location external to the “*stacked module*” is a “*passive port*” on the bottom module. (INTEL-1003, ¶206.)



Sung, Annotated Figure 10 (left), Thompson, Figure Q

Each module in the “*stacked module*” of the combination is an SDRAM module as discussed in §VI.B.1.

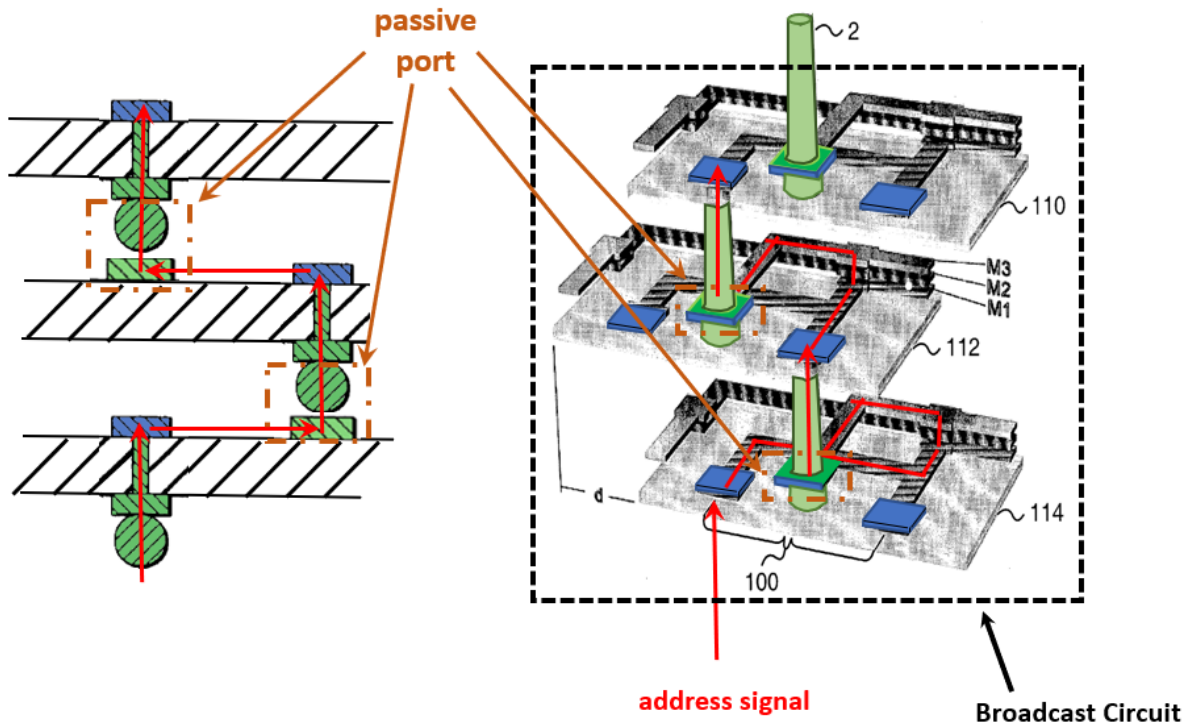
Thus, the combination of Sung and Watanabe discloses each module in its “*stacked module*” includes “*one or more passive ports for passing through the one or more active signals*” [1C], as required by Petitioner’s “*plurality of modules*” construction. (INTEL-1003, ¶¶199-207.) The combination of Sung and Watanabe also discloses the “*stacked module*” includes this limitation under PO’s construction. (*Id.*)

b. PO's Construction of "*Passive Port*"

Petitioner's construction of "*passive port*" encompasses PO's construction. Therefore, for the same reasons above, the combination of Sung and Watanabe teaches "*passive port*" under PO's construction.

Sung's broadcasting circuit 250 includes additional "*passive ports*" under PO's construction. (INTEL-1003, ¶¶209-211.) Sung's broadcasting circuit, illustrated Figure 3 (below), sends a signal (*e.g.*, an addressing signal) to all dies within the stack." (INTEL-1010, ¶47.) In the addressing circuit of Figure 9, the broadcast address signal is compared against the die address. (*See* INTEL-1010, ¶48.) In the combination of Sung and Watanabe, the external addressing signal is applied to the stacked module through a ball on the bottom module and communicated through a via to a pad on the upper surface of the bottom module, as illustrated in the figures below. (INTEL-1003, ¶209.) The signal traverses a conditional connection as shown by the red line in Figure 3 to a pad (shaded green) on the upper surface of bottom module 114. (INTEL-1003, ¶210.) In the combination, the pad on the upper surface of bottom module 114 is coupled to a ball on the lower surface of middle module 112. (*Id.*) The pad (shaded green) on bottom module 114 and ball on middle module 112 is a "*passive port*" that carries the active address signal. (*Id.*) A similar pad and ball connection exists between a

pad on the upper surface of middle module 112 and a ball on the lower surface of upper module 110. (*Id.*)



Thompson, Figure R; Sung, Annotated Figure 3

For this additional reason, the combination of Sung and Watanabe discloses the “*passive port*” limitation under PO’s construction of “*passive port*” and “*plurality of modules*”. (INTEL-1003, ¶¶209-211.)

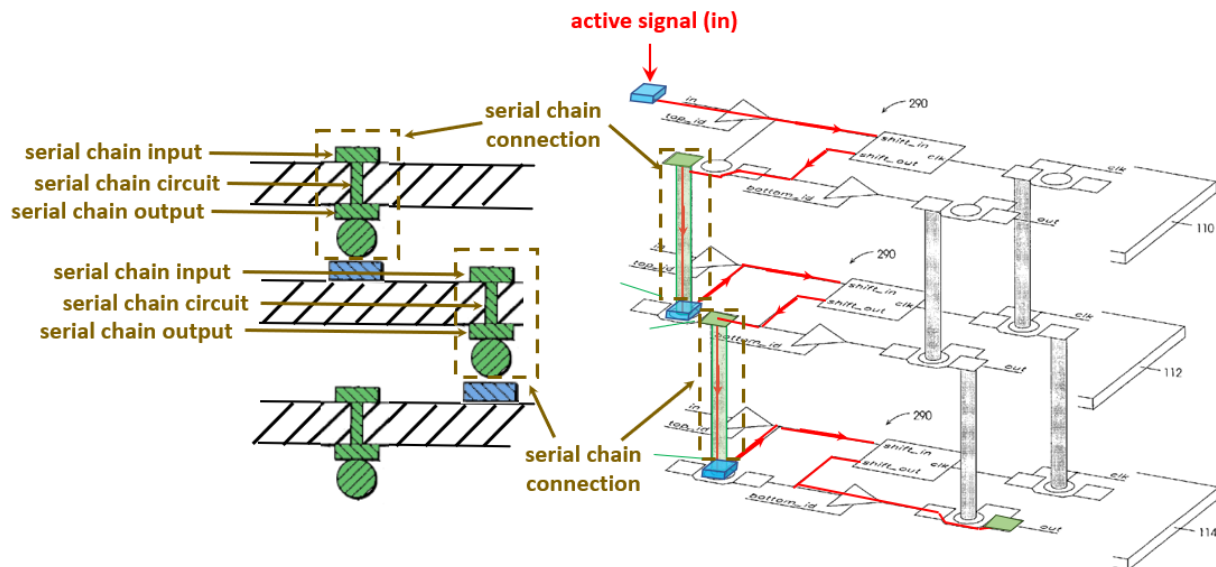
4. “*First Serial Chain Route*” Limitation [1D].

The combination of Sung and Watanabe discloses “*a first serial chain route that includes at least one serial chain connection*” [1D]. (INTEL-1003, ¶¶212-219.)

a. ***“Serial Chain Connection”***

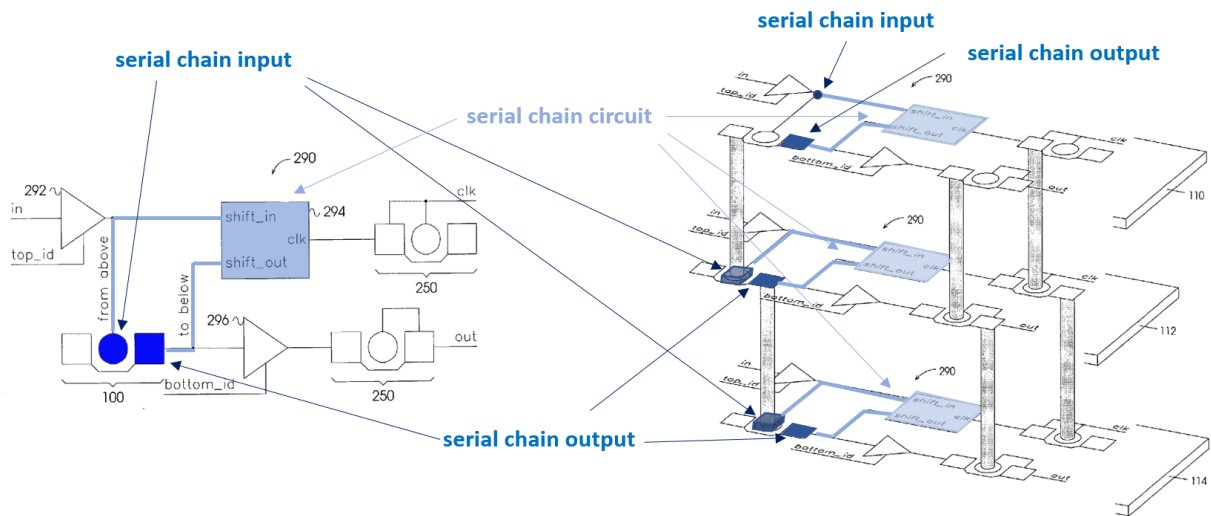
The combination of Sung and Watanabe discloses vertical and horizontal “*serial chain connection[s]*.” (INTEL-1003, ¶¶213-217.)

Vertical “*Serial Chain Connection*”: In the inter-module scan chain circuit of the combination of Sung and Watanabe (illustrated in Figure 10 and Thompson Figure S below), the shift_out output signal is passed to a pad on the upper surface of the top module and through a via to a ball on the lower surface of the module. (See §V.B.4.a.) The pad-via-ball structure in the top module is a “*serial chain connection*” with the pad on the upper surface receiving the signal being a “*serial chain input*”, the via coupling the pad and ball being the “*serial chain circuit*”, and the ball on the lower surface providing the signal to the next module being the “*serial chain output*.” (INTEL-1003, ¶¶214-215; INTEL-1005, 2,3.)



Thompson, Figure S; Sung, Annotated Figure 10

Horizontal “Serial Chain Connection”: Each module in the combined “*stacked module*” of Sung and Watanabe includes a “*serial chain connection*” in the horizontal direction through the shift register as shown in annotated Figures 8 and 10 below. (INTEL-1003, ¶¶216-127.) Figure 8 illustrates a one-bit slice of a “chain that communicates data between storage elements on adjacent dies.” (INTEL-1010, ¶35.) In this circuit, “[o]n the top die 110, shift_in is coupled to in (an external signal) through a tristate buffer 292.” (INTEL-1010, ¶49.) The shift_in input on the top module is a “*serial chain input*.” (INTEL-1003, ¶217.) The shift_out signal from the shift register is coupled to a pad on the upper surface of the top module. The connection from the shift_in input to the shift register, through the shift register to the pad is a “*serial chain circuit*” and the pad is the “*serial chain output*.” (*Id.*) The “*serial chain input*”, “*serial chain circuit*” and “*serial chain output*” form the horizontal “*serial chain connection*.” (*Id.*) Each module in the “*stacked module*” of Sung and Watanabe includes a similar horizontal “*serial chain connection*” as shown in annotated Figure 10 below right. (*Id.*)



Sung, Annotated Figure 8 (left), Figure 10 (right)

b. “First Serial Chain Route” - Petitioner’s “Plurality of Modules” Construction

As discussed above, each module in the combined “*stacked module*” of Sung and Watanabe includes a horizontal “*serial chain connection*” and the top and middle modules include vertical “*serial chain connections.*” (INTEL-1003, ¶218.) Thus, the combination of Sung and Watanabe discloses “*a first serial chain route that includes at least one serial chain connection*” [1D] under Petitioner’s construction. (*Id.*; Figure 10 below.)

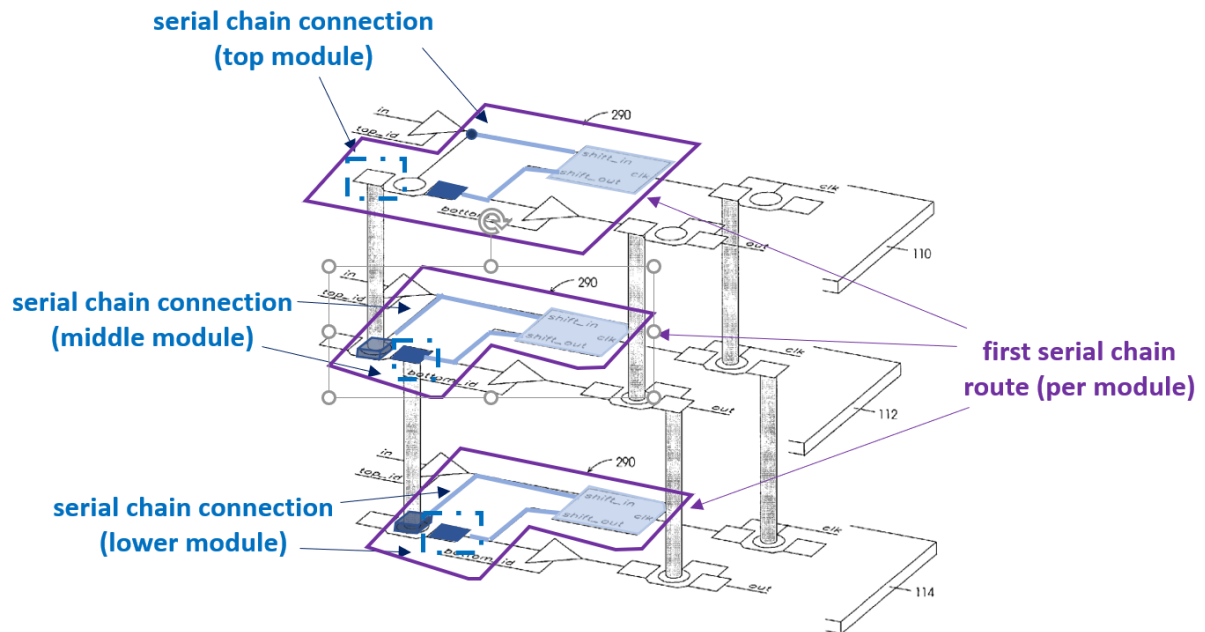
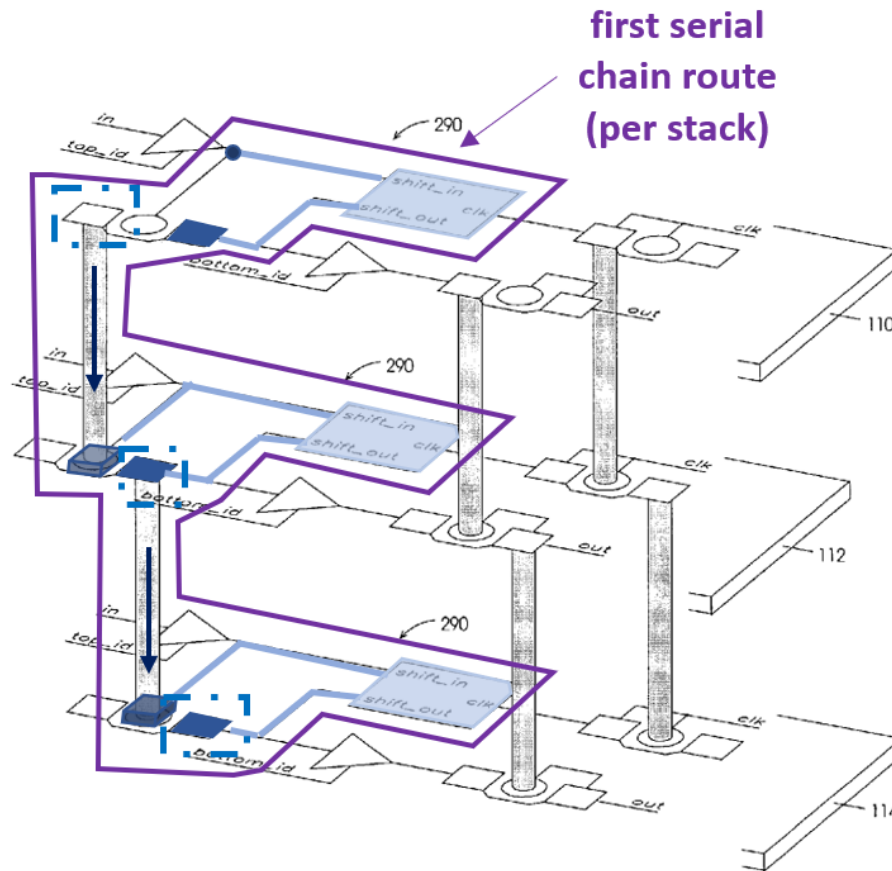


Figure 10: Inter-die communications chain for multiple dies.

Sung, Annotated Figure 10

c. “First Serial Chain Route” - PO’s “Plurality of Modules” Construction

The “*stacked module*” includes multiple “*serial chain connections*” because each stacked module includes a horizontal “*serial chain connection*” and the stack includes two vertical “*serial chain connection*.” Thus, the combination of Sung and Watanabe discloses this limitation as illustrated in Figure 10 under PO’s construction. (INTEL-1003, ¶219.)



Sung, Annotated Figure 10

5. “Second Serial Chain Route”/“Control Circuit” Limitations [1E]-[1F].

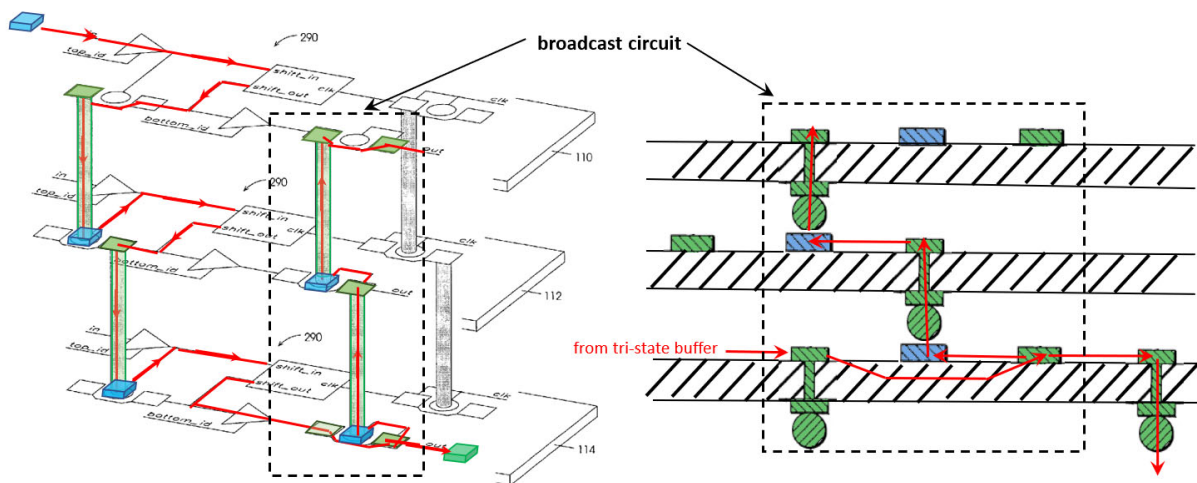
The combination of Sung and Watanabe discloses limitations [1E] and [1F].
(INTEL-1003, ¶¶220-246.)

a. “Second Serial Chain Route” - Petitioner’s Construction

The combination of Sung and Watanabe discloses a “*second serial chain route*.” (INTEL-1003, ¶¶221-227.) In Sung’s boundary scan circuit, illustrated in Figure 10 below, in the bottom module, the shift_out signal from the shift register

is coupled by tristate buffer 296 to **broadcasting circuit 250** “that conveys the data to the top of the stack 110 and then to a location external to the stack.”

(INTEL-1010, ¶49.) As illustrated in Figure 10, the shift_out signal enters the broadcast circuit on the bottom module at a connector pad (shaded green), is transmitted to a second connector pad (shaded green) via substrate wiring, and then to the central connector pad (shaded blue) via substrate wiring where the signal is output to the next layer in the stack. (INTEL-1003, ¶¶222-223.) This path, having an input, circuit (substrate wiring), and output, is a “*serial chain route*” through the module as well as a “*serial chain connection*.” (INTEL-1003, ¶223.)



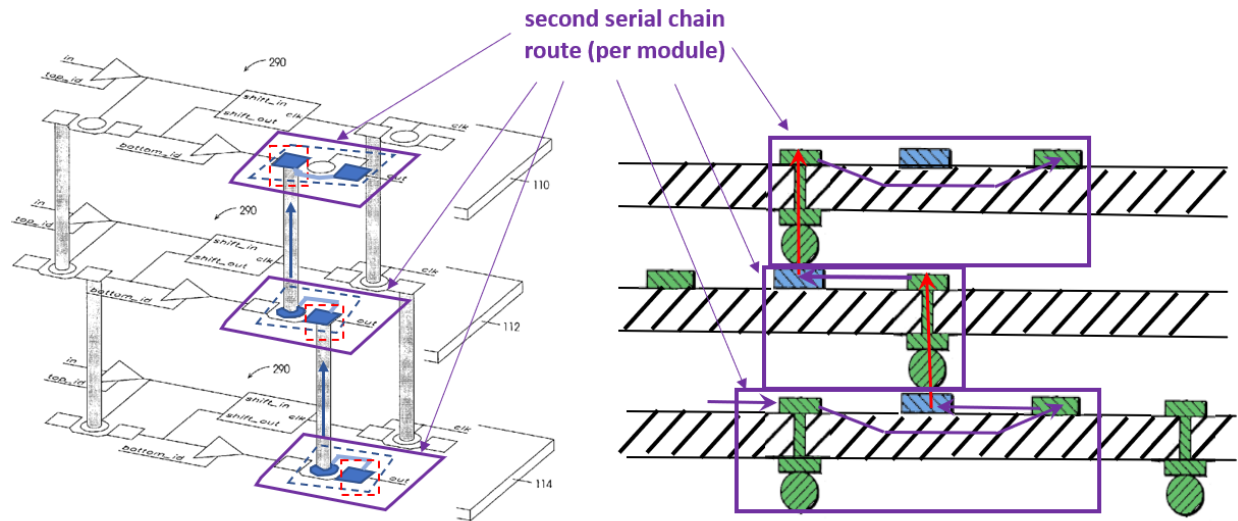
Sung, Annotated Figure 10 (left); Thompson, Figure T (right)

In the combination of Sung and Watanabe, the output signal from the bottom module is communicated to the middle module by the pad-via-ball connection of the middle module as illustrated in Thompson Figure T (above). (INTEL-1003,

¶224.) In the middle module, the right connector pad (shaded green) transmits the signal to the central connector pad (shaded blue) via substrate wiring. (*Id.*) These paths are each a “*serial chain route*” and “*serial chain connection*” in the middle module. (*Id.*)

The output signal is communicated from the middle module to the top module by the pad-via-ball connection of the top module as illustrated in Thompson Figure T (above). In the top module, the left connector pad (shaded green) transmits the signal to the right connector pad (shaded green) and then to an output connection for the top module. These paths are each a “*serial chain route*” and a “*serial chain connection*” in the top module (INTEL-1003, ¶225.)

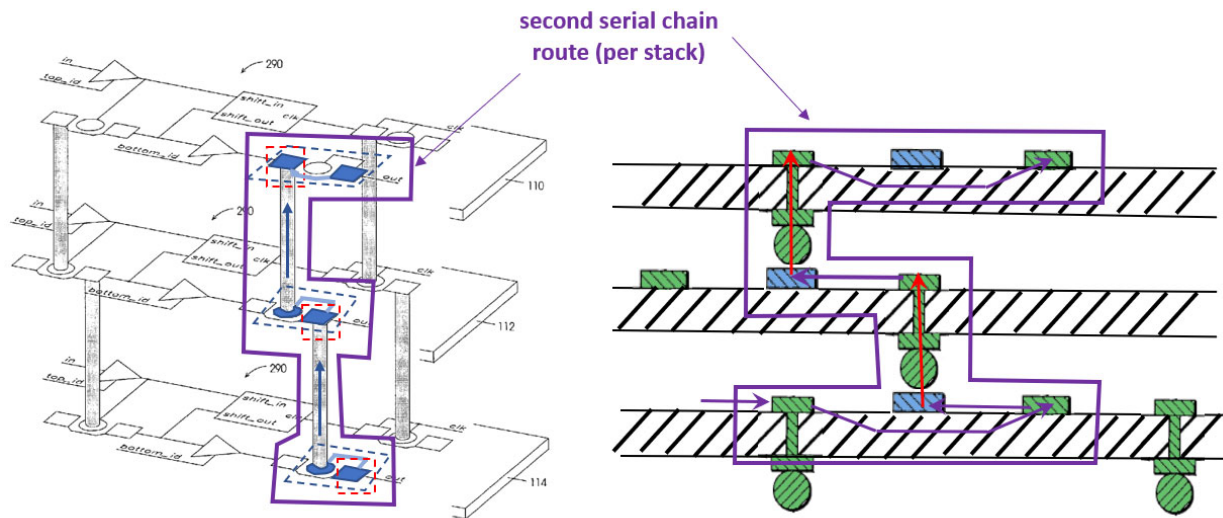
Thus, the combination of Sung and Watanabe discloses “*a second serial chain route*” [1E] under Petitioner’s “*plurality of modules*” construction as illustrated in Figure 10 below (left) and Thompson Figure U. (INTEL-1003, ¶226.)



Sung, Annotated Figure 10 (left), Thompson, Figure U (right)

b. “Second Serial Chain Route”—PO’s “Plurality of Modules” Construction

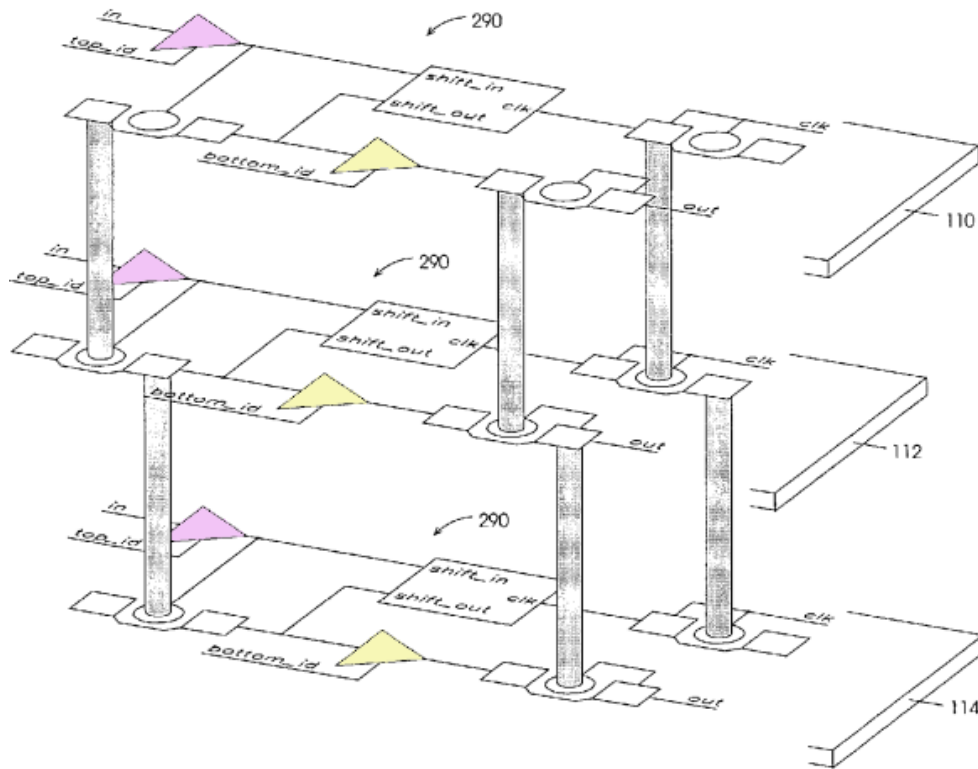
The “*stacked module*” includes multiple second “*second serial chain connections*” as discussed above. Thus, the combination of Sung and Watanabe discloses “*a second serial chain route*” under PO’s construction as illustrated in the figures below. (INTEL-1003, ¶227.)



Sung, Annotated Figure 10 (left), Thompson, Figure V (right)

c. “Control Circuit”

The combination of Sung and Watanabe also discloses “a control circuit for enabling a routing path” [1E]. (INTEL-1003, ¶¶228-239.) Redirection of data within Sung’s inter-die scan chain network, illustrated in Figure 10 below, “relies upon the identification of both the top die 110 and bottom die 114.” (INTEL-1010, ¶49.) The top and bottom modules in the “stacked module” of Sung and Watanabe are each “end modules.” (INTEL-1003, ¶228.)

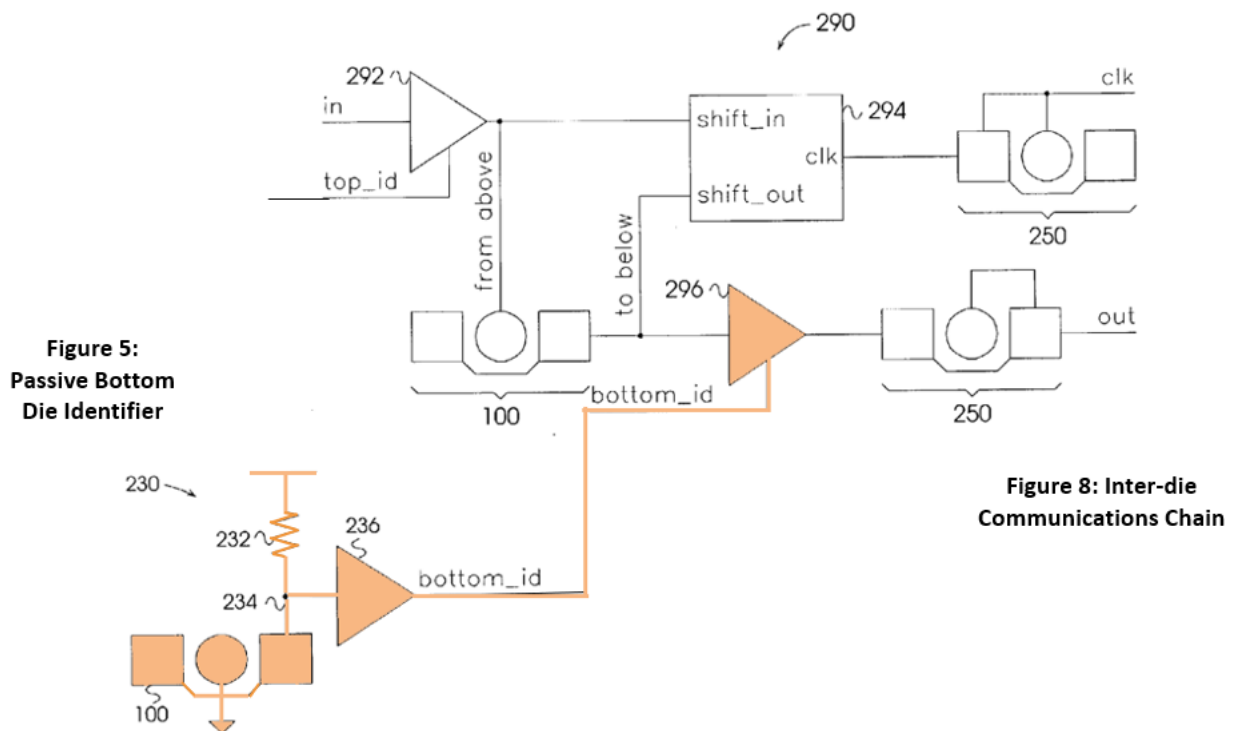


Sung, Annotated Figure 10

Specifically, a first tri-state buffer in each layer (shaded pink) “is controlled by the result (*top_id*) of the top die identifier circuit 220.” (INTEL-1010, ¶49.) A second tri-state buffer in each layer (shaded yellow) “is controlled by the *bottom_id* signal generated by the bottom die identifier circuit 230.” (*Id.*, ¶49.) The first tristate buffer is only enabled in the top die (module) and the second tristate buffer is only enabled in the bottom die (module). (INTEL-1003, ¶228.)

The following figure integrates the bottom die identifier circuit 230 of Figure 5, which generates the *bottom_id* signal, with Figure 8. (See INTEL-1010, ¶¶46, 49.) In the *bottom_id* circuit 230, the left and right terminals of connector

100 are coupled to a weak pull-up device 232. (INTEL-1003, ¶229; *See* INTEL-1010, ¶46.) Although not shown in Figure 5, a POSITA would have understood pull-up device 232 is also connected to a voltage (V_{DD}). (INTEL-1003, ¶229.) The center terminal (represented as a circle) is coupled to ground but is not coupled to the left and right terminals. (INTEL-1003, ¶230.) Node 234 is output by buffer 236 to provide bottom_id as the control input for tristate buffer 296. (*Id.*)



Sung, Partial Figure 5 and Figure 8 (Annotated)

The control input of tristate buffer 296 tri-states the input when pulled low (bottom_id not asserted) to disable a routing path between the tristate buffer input and output. (INTEL-1003, ¶231.) When the control line is pulled high (bottom_id

asserted), tristate buffer enables a routing path from its input (i.e., the output of the shift register) to its output which is coupled to broadcast circuit 250. (*Id.*) Bottom die identification circuit 230 and tristate buffer 296 (shaded orange) are the recited “*control circuit*” because they control the direction of data flow in a module by “*enabling (or disabling) a routing path*” [1E]. (*Id.*)

The following figure illustrates operation of bottom_id circuits 230 in each module, illustrated in Figure 6 (left), with Figure 10’s scan chain circuit. Each module in the stack includes a “*control circuit.*” (INTEL-1003, ¶232.) As illustrated in this figure, in the top module, the left connector terminal (shaded black) is grounded because it is coupled to the center connector terminal (shaded black) in the bottom_id circuit of the middle module which is connected to ground. (*Id.*) Similarly, in the middle module, the right connector terminal (shaded black) in the bottom_id circuit is grounded because it is coupled to the center connector terminal (shaded black) in the bottom_id circuit of the bottom module which is connected to ground. (*Id.*)

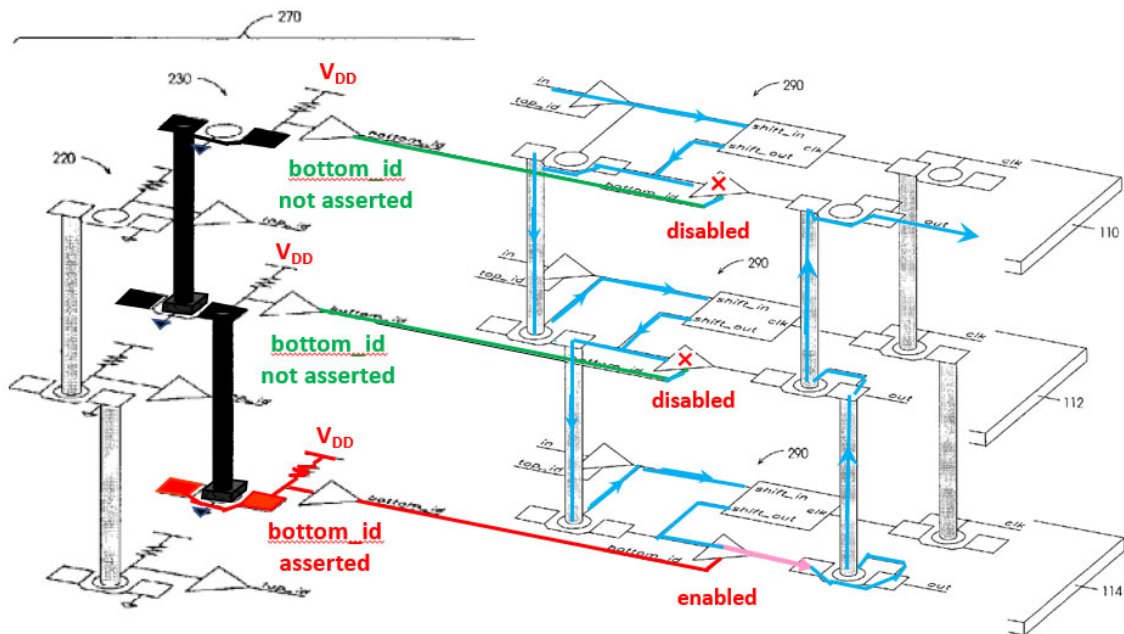


Figure 6: Die Identification Circuit

Figure 10: Inter-die communications chain for multiple dies.

Figure 10

Sung, Annotated Figures 6 and 10

The top module therefore receives “ground” from the middle module stacked below it and the middle module receives “ground” from the bottom module stacked below it. (INTEL-1003, ¶¶232-234.) The “ground” signal is a “control input signal received from another module from the plurality of modules.” (INTEL-1003, ¶234.) When Sung’s module has another module below it in the stack, the bottom_id circuit is grounded, the bottom_id signal is not asserted, and tristate buffer 296 in the scan chain circuit is disabled. (INTEL-1003, ¶¶233-234.) This is consistent with the operation of the ’243 patent, discussed further below, in which connection of the StkLow ball to ground disables path 2120. (See INTEL-

1001, 10:14-20.) Thus, the “*control circuit*” in the top and middle modules in the combination of Sung and Watanabe **disables** “*a routing path*” through the tristate buffer “*in response to a control input signal received from another module from the plurality of modules.*” (INTEL-1003, ¶¶233-234.)

In the bottom module, which is an “*end module*”, the left and right terminals in the bottom_id circuit are not connected to ground. (INTEL-1003, ¶235.)

Therefore, the bottom_id signal is pulled high by a voltage bias from the weak pull-up device which is connected to a voltage (labeled V_{DD}). (*Id.*) Because the control input to the tristate buffer (bottom_id signal) is asserted in the bottom end module, the tristate buffer enables a routing path (pink) connecting the input of buffer 296 to the input of broadcast circuit 250. (INTEL-1003, ¶235.)

Sung further discloses a high current carrying connection 260. (INTEL-1010, ¶47.) Connection 260 “is suitable for routing fixed-potentials between dies.” (*Id.*) A POSITA would understand that voltage V_{DD} (fixed voltage) is a “fixed potential” and is provided to each layer in the stack using a connection like connection 260. (INTEL-1003, ¶236.) Accordingly, voltage is provided through the stack such that the middle module provides the voltage to the bottom module. (INTEL-1003, ¶238.) Thus, in the bottom module, the combination of Sung and Watanabe discloses that “*said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the*

plurality of modules when the end module is coupled to the another module” [1F].

(INTEL-1003, ¶¶236-239.)

d. Connecting first and second “serial chain route[s]”

As shown in annotated Figure 10 below, when the routing path through tristate buffer 296 is enabled in the bottom module (“end module”), the “first serial route connection” in the bottom module is coupled to the “second serial route connection” in the bottom module. (INTEL-1003, ¶240.) Thus, the combination of Sung and Watanabe discloses “a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module” [1E] as required by Petitioner’s “plurality of modules” construction. (INTEL-1003, ¶240.)

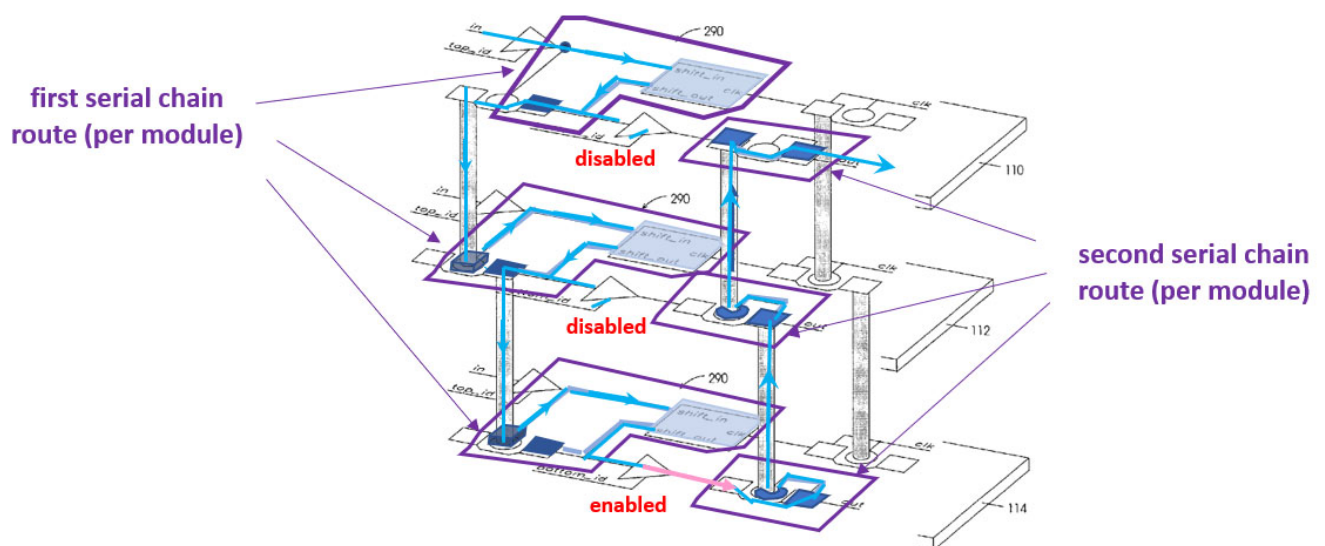


Figure 10: Inter-die communications chain for multiple dies.

Sung, Annotated Figure 10

As shown in annotated Figure 10 below, when the routing path through tristate buffer 296 is enabled in the bottom module (“*end module*”), the “*first serial route connection*” in the “*stacked module*” is coupled to the “*second serial route connection*” in “*stacked module*,” meeting this limitation under PO’s construction. (INTEL-1003, ¶241.)

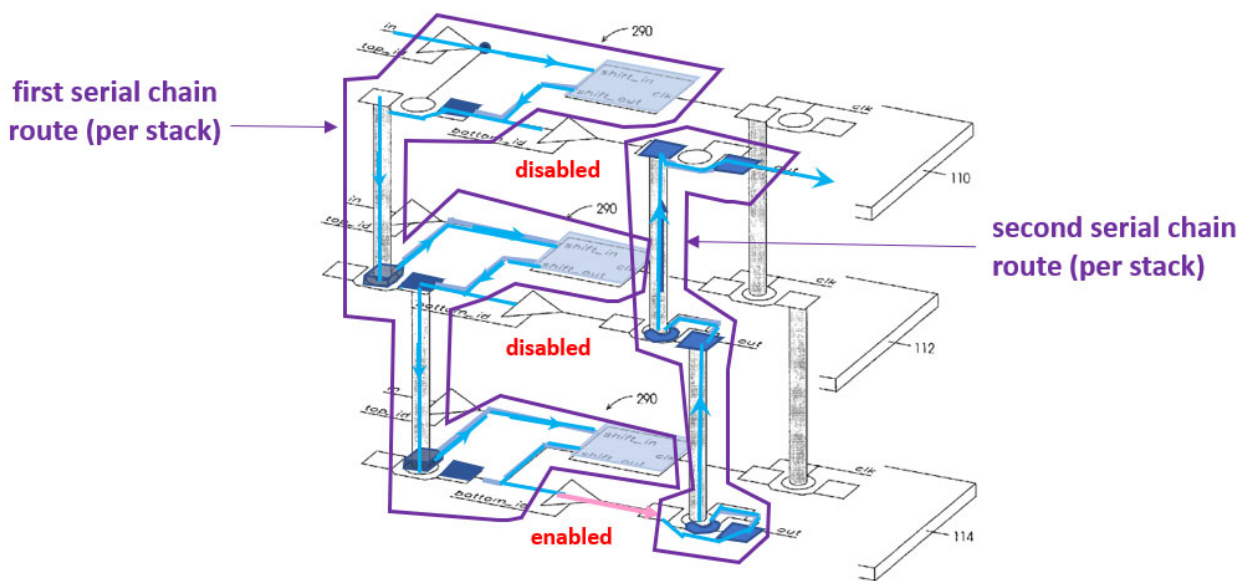


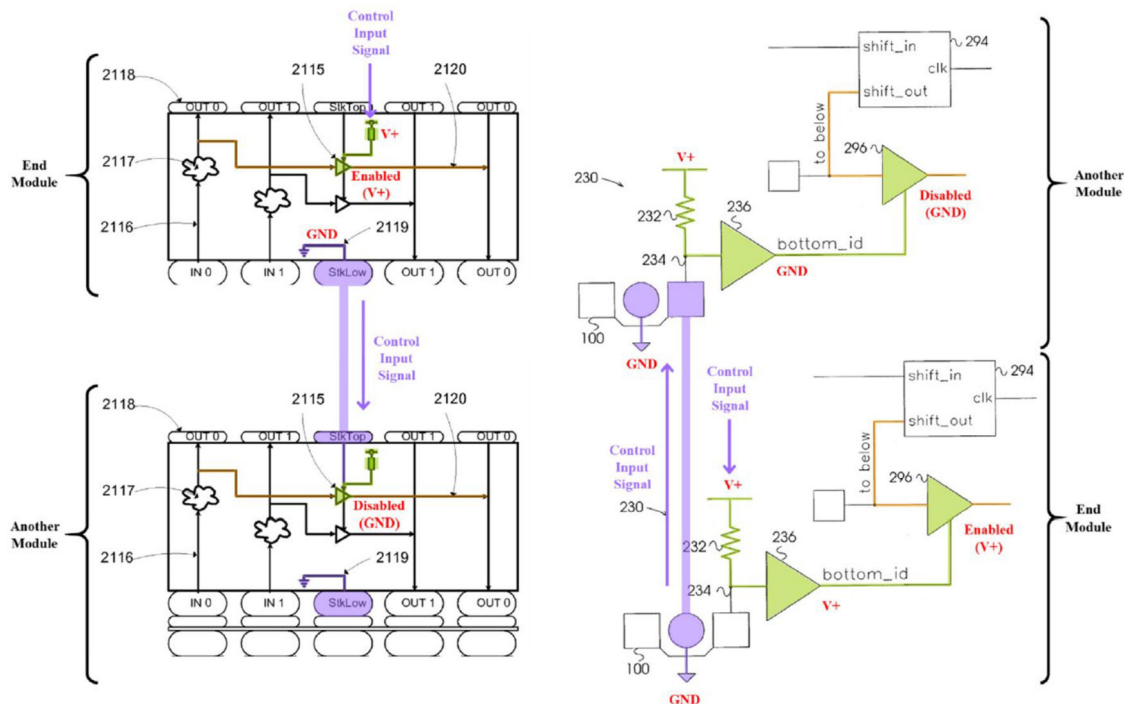
Figure 10: Inter-die communications chain for multiple dies.

Sung, Annotated Figure 10

e. Sung’s Control Circuit is Consistent with the ’243 Patent.

Sung’s “*control circuit*” operates in the same way as the control circuit of the ’243 patent, as highlighted by the below figure comparing two stacked modules excerpted from ’243 patent’s Figure 21b (left) and Sung’s control circuit shown in excerpts from Figures 5 and 8. (INTEL-1003, ¶¶242-245.) The ’243 patent’s

control circuit “includes a selectable buffer 2115 that tri-states the input when pulled low” (INTEL-1001, 10:10-11; INTEL-1005, 3.) As shown in Figure 21b, the “SktTop” pad in the top module is not coupled to another component so the control input of tristate buffer 2115 “is pulled high” by the voltage source which “let[s] the input signal branch out 2120 to the other pads, thus creating a connection route or trace that loops back to the base module solder balls.” (INTEL-1001, 10:17-20.) In each module, the “SktLow” ball “is connected internally to GND 2119.” (INTEL-1001, 10:14-15.) When a module is stacked below another module, the “SktLow” ball of the upper module couples to the “SktTop” pad of the module “pulling down the buffer control line” for the tristate buffer 2115 of the module. (INTEL-1001, 10:14-16.) This connection “tri-stat[es] the input signal and disallow[s] the branching effect.” (INTEL-1001, 10:20-24.) Sung operates in the same manner as discussed above.



**'243 Patent, Annotated Excerpts from Figure 21b;
Sung, Annotated Excerpts from Figures 5 and 8**

* * *

The combination of Sung and Watanabe discloses limitations [1E] and [1F] obvious. (INTEL-1003, ¶¶220-246.)

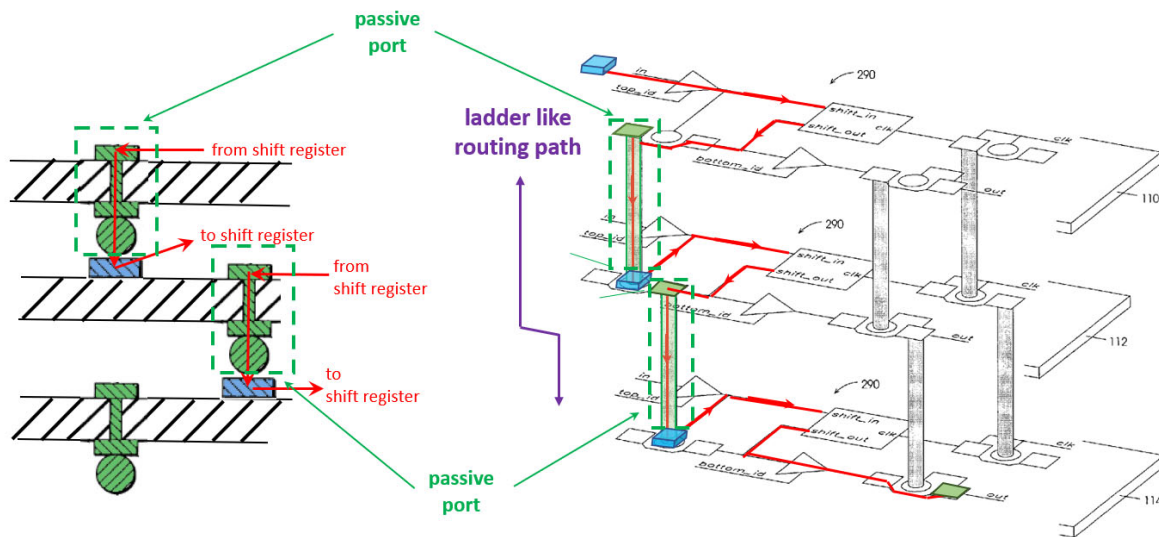
D. Claim 2

For the reasons discussed in §VI.B.3, the combination of Sung and Watanabe discloses “the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module” [2B]. (INTEL-1003, ¶247.)

The passive ports in Sung’s scan chain communications circuit 290 are staggered, forming a ladder-like routing path through the stack, as illustrated in

Sung's Figure 10 (right) and Thompson Figure W (left). (INTEL-1003, ¶247.)

Thus, the combination of Sung and Watanabe discloses “*the one or more passive port forms a ladder like routing path*” [2A]. (*Id.*)



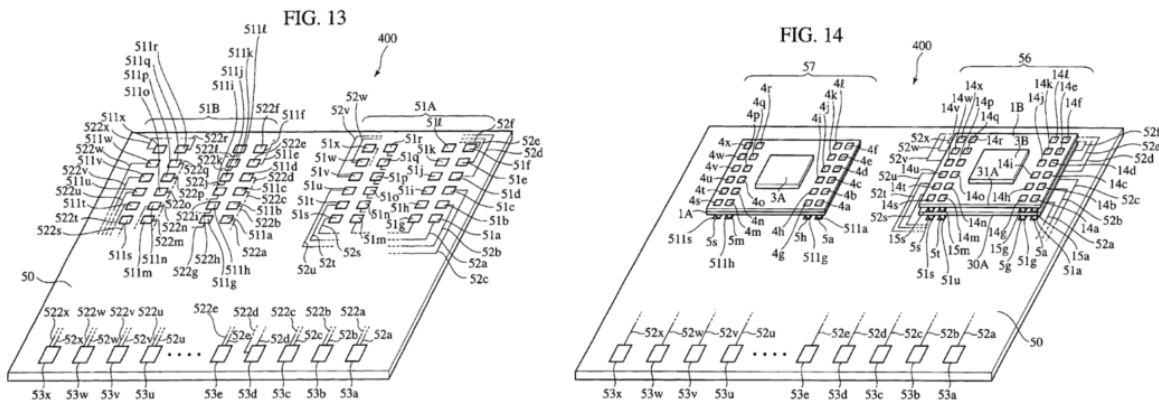
Thompson, Figure W; Sung, Annotated Figure 10

E. Claims 11 and 12

The combination of Sung and Watanabe discloses “*one or more of the plurality of modules includes a main board*” [11] and the “*one or more vertically stacked module is connected to the main board*” [12]. (INTEL-1003, ¶¶248-257.)

Sung provides “a method for communicating **externally** to, **externally** from or communicating between, dies in the stack.” (INTEL-1010, ¶18.) Sung repeatedly refers to receiving “external data input”, clocks, addresses, control signals and providing “external data output.” (INTEL-1010, ¶¶18, 47, claims 70-72.) Sung,

however, does not provide any details for connecting its stacked module with an external component that provides signals to and/or receives signals from the stacked module. Watanabe discloses its second level assembly includes a first level assembly “**mounted on a board**” (“packaging substrate 50”), as illustrated in Figures 13 and 14 below (INTEL-1011, 3:32-34; 10:29-32.) Watanabe’s packaging substrate is a main board because it supplies signals to be input to the stacked module and receives signals output from the stacked module. (INTEL-1003, ¶¶250-252, *citing* INTEL-1001, Abstract (“internal and external signals are routed from main board to various stacked modules”), 9:65-67.)



Watanabe, Figures 13 and 14

Based on the express suggestions in Sung discussed above, a POSITA would have been motivated to connect Sung's stacked module to the main board of a second level assembly, as taught by Watanabe. (INTEL-1003, ¶253.) When the "stacked module" of SDRAM modules is mounted on the main board, as taught by

Watanabe, the main board is a “*module*” in the package. Therefore, the combination of Sung and Watanabe discloses “*one or more of the plurality of modules includes a main board*” [11] and the “*vertically stacked module is connected to the main board*” [12]. (INTEL-1003, ¶254.)

A POSITA would have been motivated to couple the stacked module to a main board to form an operational electronic device. (INTEL-1003, ¶255.) Sung teaches its stacked modules include “storage elements” (i.e., memory). (See INTEL-1010, ¶24.) A POSITA would have understood that in practical implementations, a stacked module, such as a memory module, would be used with a CPU (or other type of microcontroller) that includes a memory controller adapted to supply external electrical signals into a stacked memory module for performing operations such as reading and writing data. (INTEL-1003, ¶255, *citing* INTEL-1024, 311, Figure 5.12.) A POSITA would have understood one common way to implement a device with CPU and memory stack is to mount both on a main circuit board as taught by Watanabe. (INTEL-1003, ¶256, *citing* INTEL-1022, 44-45.) As taught by Watanabe, the operational modules (first level assemblies) are mounted and functionally interconnected on a main circuit board, which provides horizontal interconnections between the first level assemblies, as well as additional external connections for receiving electric power signals and the like. (INTEL-1003, ¶257.)

VII. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. 35 U.S.C. §314(a)

1. Parallel Litigation

In addition to the compelling merits of the Petition, the *Fintiv* factors weigh heavily against discretionary denial. The '243 patent was asserted against Intel in the Western District of Texas in early April 2022. The case was transferred to the Northern District of California ("NDCA") in February 2023. The median-time-to-trial of all civil cases in NDCA is 32.9 months. (*See* INTEL-1027, 66.) Assuming that timing from the original filing date, the NDCA trial date is February 2025, over 2 months after the final written decision. Moreover, the co-pending district court litigation is in its early stages. The court has not issued a scheduling order and claim construction, expert discovery, summary judgment and trial all remain in the future.

2. Prior Petition

The '243 patent was challenged in a prior IPR proceeding, IPR2018-01720 (the '1720 IPR), by Samsung Electronics America, Inc., Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc. and SK Hynix America Inc., SK Hynix Inc. The Board instituted trial on April 5, 2019. The parties settled and terminated the proceeding in June 2019.

The *General Plastic* factors weigh heavily against discretionary denial. This

is Intel’s first Petition, filed in response to a recent infringement complaint asserting the ’243 patent. Intel has no significant relationship with the prior petitioners and therefore Factor 1 weighs heavily against denial. *Cf. Valve Corp. v. Electronic Scripting Products, Inc.*, IPR2019-00062, Paper 11, 9 (April 2, 2019) (precedential).

The remaining factors similarly weigh against denial. Factors 2 and 4 relate to prior art withheld from the first petition. Because Intel did not file the ’1720 petition, these factors are inapplicable, weighing against denial. Factor 5 also weighs against denial because Intel had no reason to file this Petition until it was served with a complaint—over **two years** after the ’1720 IPR was settled. Regarding Factor 3, while there is some overlap in applied references, Intel’s obviousness grounds are different than those in the ’1720 IPR and address claim construction positions not raised in the ’1720 IPR. Factors 6 and 7 also weigh against denial because the ’1720 IPR was settled shortly after institution, long before Final Written Decision (“FWD”), and no other proceeding is pending challenging the ’243 patent. *See Microsoft Corp. v. Dareltech, LLC*, IPR2020-00483, Paper 11 (September 16, 2020) (instituting trial of an IPR petition presenting same art and arguments as prior terminated IPR).

B. 35 U.S.C. §325(d)

None of the applied references in the present IPR were cited or discussed during the original prosecution of the '243 patent. The '1720 IPR was instituted for the challenged claims finding a reasonable likelihood of prevailing on 5 grounds: Obviousness over Sato alone or in combination with Gaynes or Eide and Obviousness over Sung alone or in combination with Matsui. The '1720 IPR settled before FWD. Therefore, the Office never issued a final ruling on patentability in the '1720 IPR based on any combination of references. Moreover, although Sato and Sung are used in the present IPR, the Office has not considered the grounds presented in this Petition based on Hosomi and Sato and Sung and Watanabe. Moreover, the present IPR addresses claim construction positions not raised in the '1720 IPR. Part 1 of the *Advanced Bionics* framework has not been satisfied.

Part 2 of the *Advanced Bionics* framework has also not been satisfied. No final determination on patentability of the Sato and Sung grounds issued from the Office due to the settlement between the parties. The evidence and facts presented in the Petition therefore warrant consideration of the Petition because, like the settled '1720 IPR, this Petition presents a compelling case of unpatentability based on claim constructions never considered by the Office.

VIII. MANDATORY NOTICES

A. Real Party In Interest Under 37 C.F.R. §42.8(b)(1)

Petitioner is the sole real party in interest.

B. Related Matters Under 37 C.F.R. §42.8(b)(2)

To the best of Petitioner's knowledge, the '243 patent is involved in the following district court litigations:

- *BiTMICRO LLC v. Intel Corp.*, 6-22-cv-00335 (WDTX)

C. Notice Of Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints **Lori A. Gordon** (Reg. No. 50,633) at the address of Perkins Coie LLP, 700 Thirteenth Street, N.W., Suite 800, Washington, DC 2005-3960, telephone number (202) 654-6200, as lead counsel; and **Christina J. McCullough** (Reg. No. 58,720) at the address of Perkins Coie LLP, 1201 Third Avenue, Suite 4900, Seattle, Washington 98101-3099, telephone number (206) 359-6897, **Matthew W. Hindman** (Reg. No. 57,396) and **Yuanfeng Gao** (Reg. No. 79,573) at the address of 3150 Porter Drive, Palo Alto, CA 94304-1212, telephone number (650) 838-4300, as backup counsel.

Petitioner consents to electronic service by email at the email addresses: gordon-ptab@perkinscoie.com, mccullough-ptab@perkinscoie.com, hindman-ptab@perkinscoie.com, and gao-ptab@perkinscoie.com.

IX. CONCLUSION

Inter Partes Review is respectfully requested.

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon (Reg. No. 50,633)
Lead Counsel, Petitioner

PERKINS COIE LLP
700 Thirteenth Street, NW, Suite 800
Washington, DC 2005

Date: March 31, 2023

LISTING OF ASSERTED CLAIMS

[1P] A stacked module comprising

[1A] a plurality of modules each comprising:

[1B] one or more active ports for carrying one or more active signal;

[1C] one or more passive ports for passing through the one or more active signals;

[1D] a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

[1E] a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

[1F] said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

2. The stacked module of claim 1 **[2A]** wherein the one or more passive port forms a ladder like routing path, and **[2B]** the passive port

connects a passive ball on one surface of a module to a passive pad on another surface of the module.

11. The stacked module of claim 1 wherein one or more of the plurality of modules includes a main board.

12. The stacked module of claim 11 wherein one or more vertically stacked module is connected to the main board.

CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(d)

Petitioner hereby certifies that this Petition complies with the type-volume requirements of 37 C.F.R. §42.24(a). The word processing program used to prepare this Petition indicates that it contains 13,988 words, excluding the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any listing of the claims.

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon
Attorney for Intel

Date: March 31, 2023

CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of the Petition for *Inter Partes* Review of U.S. Patent No. 7,826,243 and supporting materials (Exhibits and Power of Attorney) were served via overnight delivery on the Patent Owner at the correspondence address of record as listed on PAIR:

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and via email to the attorneys of record for Plaintiff in the concurrent *BiTMICRO LLC v. Intel Corp.*, 6-22-cv-00335 litigation:

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