

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BiTMICRO, LLC,
Patent Owner.

Case IPR2023-00781
Patent 7,826,243

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	1
A.	The ’243 Patent Discloses Connection Techniques for Memory Modules	2
B.	The Challenged Claims and Petitioner’s Challenges	6
II.	THE BOARD NEED NOT REACH ANY CLAIM CONSTRUCTION ISSUES TO DENY THE PETITION.....	9
III.	PETITIONER’S CHALLENGES FAIL ON THE MERITS	12
A.	Ground 1 Based on Hosomi in View of Sato Fails	12
i.	Petitioner’s Proposed Reason for Combining Hosomi and Sato is Driven By Hindsight-based Reasoning.....	12
ii.	Petitioner’s Proposed Combination of Hosomi and Sato Fails to Identify any “Passive Port[s]” as Claimed.....	15
iii.	Petitioner’s Proposed Combination of Hosomi and Sato Fails to Disclose a “First Serial Chain Route” of Independent Claim 1	19
iv.	Petitioner’s Proposed Combination of Hosomi and Sato Also Fails to Disclose a “Control Input Signal” of Independent Claim 1	22
v.	Ground 1’s Challenge Fails to Establish the Unpatentability of Claim 1.....	24
vi.	Petitioner’s Proposed Combination of Hosomi and Sato Also Fails to Disclose Every Feature of Dependent Claim 2.....	25
B.	Ground 2 Based on Sung in View of Watanabe Also Fails	28
i.	Petitioner’s Proposed Combination of Sung and Watanabe Fails to Disclose a “First Serial Chain Route” of Independent Claim 1	28

ii.	Petitioner’s Proposed Combination of Sung and Watanabe Also Fails to Disclose a “Control Input Signal” of Independent Claim 1	31
iii.	Ground 2’s Challenge Fails to Establish the Unpatentability of Claim 1	36
iv.	Petitioner’s Proposed Combination of Sung and Watanabe Also Fails to Disclose Every Feature of Dependent Claim 2	36
IV.	CONCLUSION.....	38

TABLE OF AUTHORITIES

Cases

<i>Samsung Electronics Co., Ltd. v. Rightquestion, LLC</i> , IPR2022-00251, Paper 17 (PTAB June 9, 2022)	14
---	----

Statutes

35 U.S.C. § 311(b)	34
--------------------------	----

Rules

37 C.F.R. § 42.107	1
37 C.F.R. § 42.120(a).....	1

Pursuant to 37 C.F.R. § 42.107, Patent Owner BiTMICRO, LLC (“BiTMICRO” or “Patent Owner”) files this preliminary response to the Petition, setting forth reasons why the Petition for *inter partes* review (“IPR”) of claims 1, 2, 11, and 12 of U.S. Patent No. 7,826,243 (the “’243 Patent”), as requested by Intel Corporation (“Petitioner”), should be denied.¹

I. INTRODUCTION

The ’243 Patent, entitled “Multiple Chip Module And Package Stacking For Storage Devices,” relates to chip module stacking and routing techniques “to support miniaturization and memory scalability.” ’243 Pat., 1:9–12. The ’243 Patent describes exemplary stacked modules where the semiconductor dies are mounted in a module and then “stacked to create the desired memory capacity and different packages are stacked to create [the] desired function.” ’243 Pat., 1:47–49. The stacked modules may be identical, or they may be different from each other. *See, e.g.*, ’243 Pat., 4:15-19, 6:44-7, 8:63-64. The ’243 Patent discloses multiple configurations for pin assignment and connection techniques to enable “a selection of a specific module in a multiple module stack.” ’243 Pat., 8:66-10:35.

¹ By submitting this Preliminary Response, no waiver of any argument is intended by Patent Owner. Patent Owner will have a right to file a complete response to the Petition, should the Board institute *inter partes* review. 37 C.F.R. § 42.120(a).

A. The '243 Patent Discloses Connection Techniques for Memory Modules

One connection technique is illustrated in Figure 19 through an exemplary stack of memory modules on a controller module. '243 Pat., 8:66-9:22; *see also* Ex. 1002, 404-06; Ex. 1005. Figure 19 illustrates a controller module at the bottom of the SDRAM module stack, and the controller module has four active pads, or active ports (pads 00, 01, 02, and 03). '243 Pat., 8:66-9:22; Ex. 1002, 404-06; Ex. 1005. Each of these active ports is connected to a respective active ball X0 to access an associated SDRAM Module through a ladder-like routing path, as shown below:

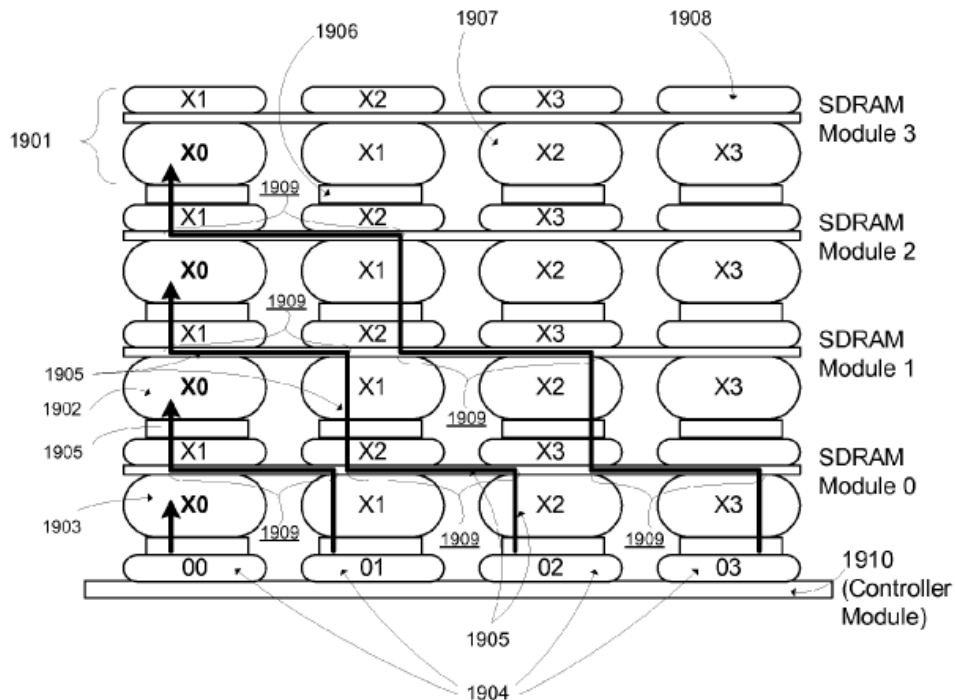


Figure 19

The balls and pads, labeled X1, X2, and X3 in the above image, are “passive” balls and pads. ’243 Pat., 8:66-9:22; Ex. 1002, 404-06; Ex. 1005. These active ports (also referred in the ’243 Patent to as “active pads”) are coupled to the respective X0 balls “through at least one passive port connecting a passive ball and passive pad.” ’243 Pat., 8:66-9:22; Ex. 1002, 404-06; Ex. 1005. These passive ports are used in a “technique [that] enables the controller module’s active pad to be routed to the desired specific module in the stack.” ’243 Pat., 8:66-9:22; Ex. 1002, 404-06; Ex. 1005. For example, as shown in Figure 19, a signal from active pad 02 is routed through three passive ports between a passive ball and passive pad before reaching ball X0.

A related pin assignment and connection technique, shown in Figure 21a, involves the “serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board.” ’243 Pat., 9:61-10:8; Ex. 1002, 406-08; Ex. 1005. The embodiment describing this technique is not limited to SDRAM modules; indeed, many different types of modules (such as Flash, FEPROM, memory and controller modules) can be used with these stacking and connection techniques. This second technique involves a module at the bottom of the stack with an input signal connected to the “IN ball” of the base module. ’243 Pat., 9:61-10:8; Ex. 1002, 406-08; Ex. 1005. Additional modules are stacked on the base module, with each module having “a ball and pad

that are coupled together by a serial chain circuit.” ’243 Pat., 9:61-10:8; Ex. 1002, 406; Ex. 1005. In this embodiment, the serial chain circuits couple IN balls with OUT pads, as shown by the small/short black arrows on the left side of the figure below (such as 2127). Similarly, serial chain circuits couple OUT pads with OUT balls, as shown by the small/short black arrows on the right side of the figure below (such as 2136):

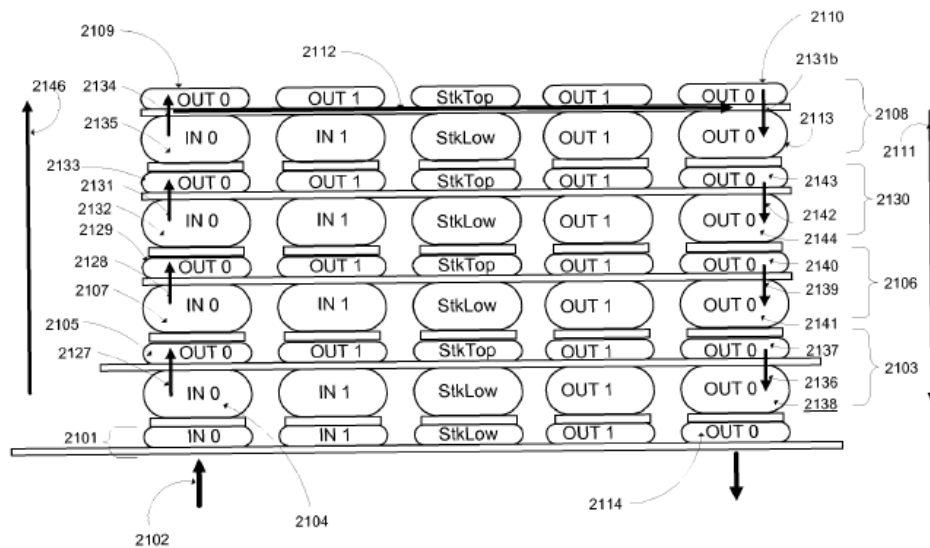


Figure 21a

In this embodiment, a signal route that includes a serial chain circuit connecting a ball and a pad creates a “serial chain connection,” with two or more “serial chain connections” constituting a “serial chain route.” Ex. 1002, 406-07; Ex. 1005 (defining “serial chain connection” and “serial chain route”). In this embodiment, when a serial chain route 2146 reaches a top pad, the signal is routed internally, with connection 2112, to another pad, such as OUT pad 2110, which is

connected directly to the ball underneath, such as OUT ball 2113. '243 Pat., 9:61-10:8; Ex. 1002, 406-08; Ex. 1005. In this embodiment, this routed signal then “passes through another set of serial chain connections that comprise another serial chain route, such as serial chain route 2111 for the stack until it reaches OUT pad 2114 of the main board for external access.” '243 Pat., 9:61-10:8; Ex. 1002, 406-08; Ex. 1005.

Similar to Figure 21a, Figure 21b illustrates a control circuit included in each module in the stack. '243 Pat., 10:10-11. The control circuit includes a selectable buffer 2115 that is controlled by a control input signal applied via a buffer control line, and “will let the input signal branch out 2120 to the other pads, thus creating a connection route or trace that loops back to the base module solder balls” via the OUT serial chain route. '243 Pat., 10:10-20.

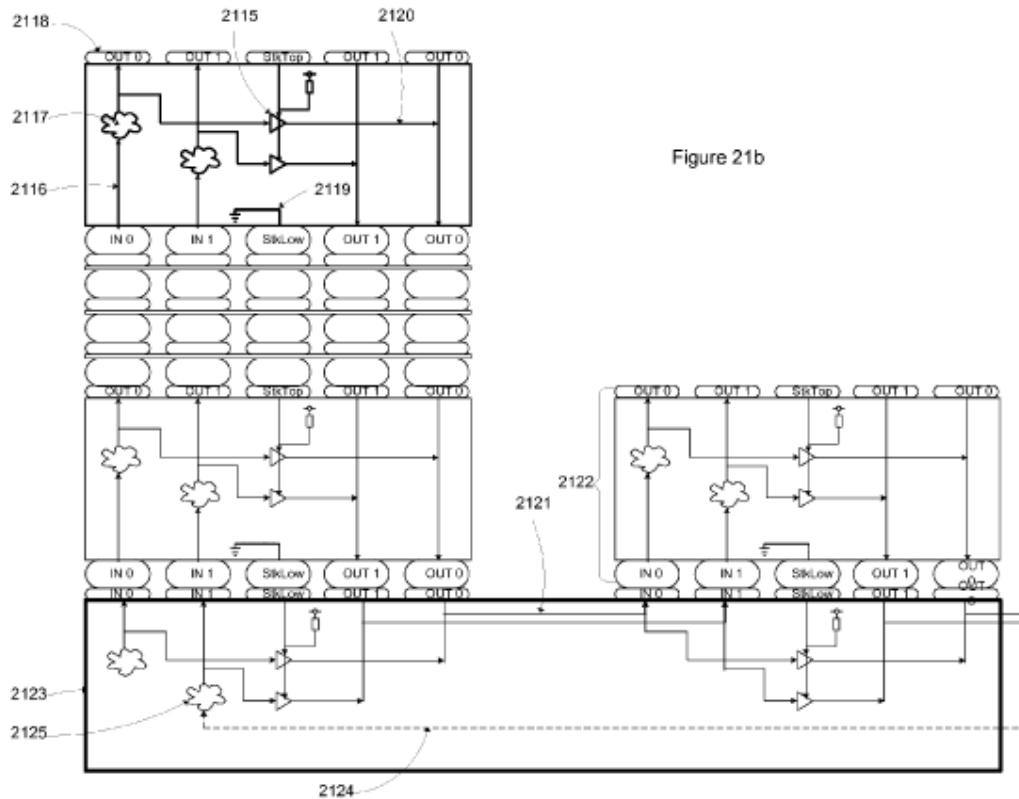


Figure 21b

B. The Challenged Claims and Petitioner's Challenges

Consistent with this disclosure, the challenged claims are directed generally to a stacked module of memory modules. Claim 1, the sole independent claim at issue in this proceeding, is reproduced below:

1. A stacked module comprising a plurality of modules each comprising:
 - one or more active ports for carrying one or more active signal;
 - one or more passive ports for passing through the one or more active signals;
 - a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain

circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

'243 Pat., 10:42-60. Petitioner asserts two obviousness-based grounds against claim 1 and the additional challenged dependent claims, claims 2, 11, and 12. In Ground 1, Petitioner contends that challenged claims 1, 2, 11, and 12 are obvious over the Hosomi² reference in view of the Sato³ reference. In Ground 2, Petitioner contends that challenged claims 1, 2, 11, and 12 are obvious over the Sung⁴ reference in view of the Watanabe⁵ reference. However, Petitioner's challenges fail for numerous reasons.

First, Petitioner advances a nonsensical construction of claim 1 that would require each module in a stacked module to include each claimed element,

² U.S. Patent Application Publication No. 2001/0028114 to Hosomi ("Hosomi").

³ Certified Translation of International Publication No. WO 2004/072667 ("Sato").

⁴ U.S. Patent Application Publication No. 2003/0178228 to Sung *et al.* ("Sung").

⁵ U.S. Patent 6,791,193 to Watanabe *et al.* ("Watanabe").

including both structural and functional features. This is wrong, as the '243 Patent makes clear that the claimed “first serial chain route” requires two serial chain circuits in series, each serial chain circuit coupling a ball and pad, and a serial chain route spans more than one module. Additionally, only a single control circuit in a stacked module “enable[s] the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.” Petitioner erroneously contorts the claim language and disclosures of the prior art while trying, unsuccessfully, to establish each of the claim elements in *each* module of the asserted combinations of references.

Second, each asserted combination lacks a number of claimed features. Petitioner fails to establish a “first serial chain route” in any combination, and no combination enables any “routing path in response to a control input signal received from another module from the plurality of modules.”

Third, Petitioner's proposed combination in the first challenge is driven solely by impermissible hindsight. Petitioner recognizes that Sato lacks any passive pad/passive ball connections, and Petitioner looks to Hosomi to incorporate certain circuit elements into Sato to remedy this shortcoming. But the support for Petitioner's proposed reason to modify Sato is predicated on a single conclusory sentence in the Petition. Even Dr. Thompson's declaration (Ex. 1003)

substantially parrots this sentence without providing any further explanation or reasoning supporting the combination, and should therefore be disregarded as improperly conclusory. Only impermissible hindsight bias exists to support this proposed modification of Sato.

Finally, without disclaiming the independent patentability of any other dependent claim, at least dependent claim 2 is independently patentable over Petitioner's asserted challenges. No reference discloses a ladder-shaped routing path formed by a passive port that connects a passive ball on one surface of a module to a passive pad on another surface of the same module. Petitioner's arguments to the contrary are incorrect even under Petitioner's own characterizations of the asserted combinations.

For these reasons, as more fully explained below, both Grounds presented in the Petition are deficient. The Petition should be denied without institution.

II. THE BOARD NEED NOT REACH ANY CLAIM CONSTRUCTION ISSUES TO DENY THE PETITION

In the Petition, Petitioner contends that two claim terms "require construction," and sets forth the following competing constructions for these terms.

Term	Petitioner’s Proposed Construction	Patent Owner’s Proposed Construction
Claim 1: “a plurality of modules each comprising” (appearing in the preamble of claim 1)	“each module in the stacked module comprising”	This term is part of the preamble and not a limitation of the claim
Claim 1: “passive port”	“connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module”	“connection between a passive ball and a passive pad”

See Pet., 6-8.

As introduced above and explained below, Petitioner’s proposed construction of the preamble term, “a plurality of modules each comprising” is nonsensical, and importantly results in multiple failures in Petitioner’s challenges. Petitioner incorrectly argues that the effect of its proposed construction means that each module in a stacked module must be identical in structure. Pet., 6-7. This proposed construction is irreconcilable deficient, as Petitioner’s proposed construction requires each module in a stacked module to possess every claimed feature. In addition to structural features, claim 1 also recites certain interactions

between the claimed structural elements, and Petitioner's interpretation of the preamble term would require these interactions to also be present in each module.

For example, as discussed in Section III.A.iv below, Petitioner's proposed construction of the preamble would require each module in a stacked module to include a claimed "control circuit ... disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module." This is facially unreasonable, and Petitioner never even attempts to establish that a control circuit in any module other than the top module of the Sato-Hosomi combination controls that top module's routing path. Indeed, under Petitioner's proposed combination of Hosomi and Sato, only the top module enables or disables the output of a signal onto the TDO2 signal line, which Petitioner relies upon to disclose the claimed "routing path." The Sung-Watanabe combination includes a similar deficiency, as only the bottom module controls the bottom module's routing path. If Petitioner's construction of the claim 1 preamble is decided by the Board to be correct, then it necessarily follows that Petitioner has failed to show at least this claimed feature in each module of the plurality of modules.

However, the Petition's failures extend beyond the natural results of Petitioner's proposed constructions for these two terms. For example, as discussed in Section III.A.iv and Section III.B.ii below, Petitioner's proposed combinations

in both Grounds fail to disclose or suggest the claimed “said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.” This element is absent from both challenges, and is dispositive in establishing that both Grounds fail, without asking the Board to also undertake an unnecessary claim construction exercise.

Thus, without expressly agreeing to Petitioner’s constructions, and without waiving its right to submit its proposed constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction. For the reasons presented in Section III below, Petitioner’s Grounds each include fundamental flaws and fail to establish the obviousness of any challenged claim.

III. PETITIONER’S CHALLENGES FAIL ON THE MERITS

A. Ground 1 Based on Hosomi in View of Sato Fails

i. Petitioner’s Proposed Reason for Combining Hosomi and Sato is Driven By Hindsight-based Reasoning

Petitioner argues that a POSITA “would have been motivated to incorporate Sato’s boundary scan controller into a chip in each module of Hosomi’s stacked module (as illustrated below) and would have been motivated to implement Sato’s daisy-chain connections using the package routing structures of Hosomi.” Pet., 14.

In particular, Petitioner proposes to incorporate a “boundary scan controller” from Sato into “each module of Hosomi’s stack.” Pet., 14-15.

Importantly, Petitioner also recognizes that Sato fails to disclose any passive ball/passive pad connections as required under either construction of “passive port,” and proposes “(1) implementing Sato’s vertical electrodes using Hosomi’s through-vias (*e.g.*, connection 56), Sato’s terminals using Hosomi’s electrodes 51 (pads), Sato’s connection lines using Hosomi’s wiring layers (*e.g.*, Figures 6A-6B), and (2) using Hosomi’s pad and ball connections to connect adjacent modules” in Sato. Pet., 15. This proposed implementation of Hosomi’s “package routing structures” “to implement Sato’s daisy-chain connections” fails, however, for lack of motivation.

Petitioner’s alleged reasons for the proposed combination of Sato and Hosomi, as enumerated in pp. 16-19 of the Petition, focus almost exclusively on the asserted reasons for incorporating Sato’s boundary scanning test into Hosomi, with almost no mention for why a POSITA would have been “motivated to implement Sato’s daisy-chain connections (illustrated in Figure 5) in the combined system which stacks modules (each having a chip mounted on a substrate) using Hosomi’s package routing structures” See Pet., 15. The sole reason presented for this modification to the electrode structure of Sato occurs at the end of the first

paragraph on page 16. There, Petitioner asserts that “Hosomi teaches a low cost and reliable technique to route connections between layers in a stack.” Pet., 16.

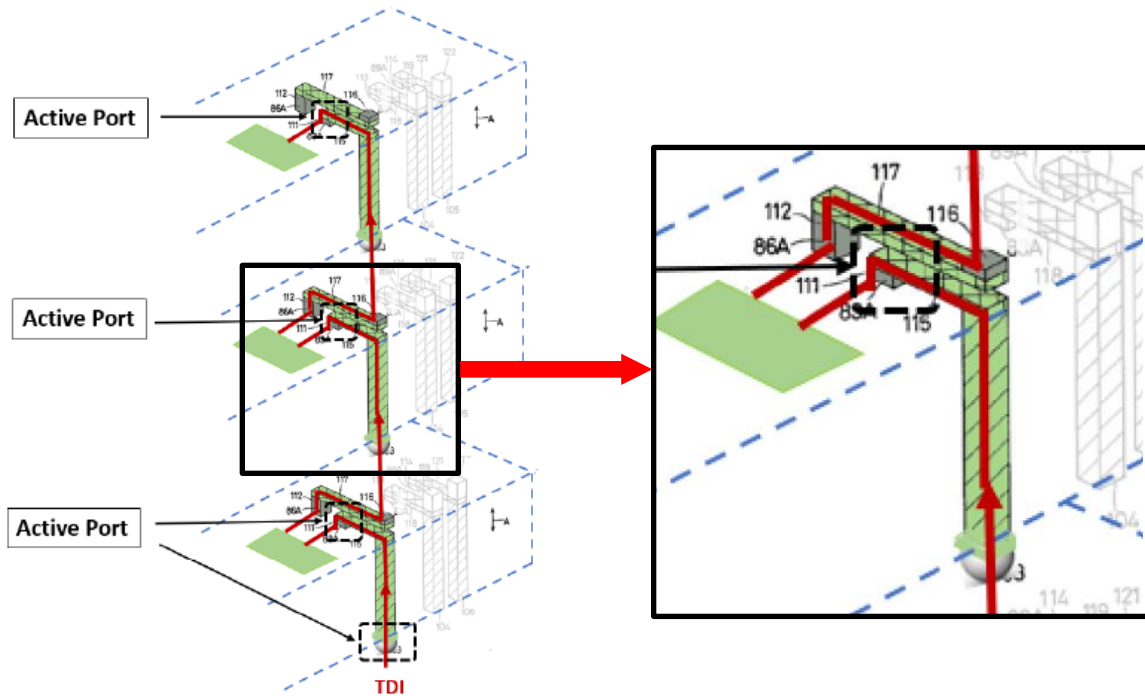
But this alleged reason to modify Sato’s electrode structure is unsupported by any evidence other than a single conclusory statement of Dr. Thompson. Pet., 16 (citing Ex. 1003, ¶91). Indeed, without any further citation to evidence, support, or explanation, Dr. Thompson’s Declaration substantially parrots the Petition, also stating “Hosomi teaches a low cost and highly reliable technique to route connections between the layers in the stack.” Ex. 1003, ¶91. This statement does nothing more than mirror the conclusory assertions in the Petition and should be disregarded. *See* 37 C.F.R. § 42.65(a); *Samsung Electronics Co., Ltd. v. Rightquestion, LLC*, IPR2022-00251, Paper 17 at 25 (PTAB June 9, 2022) (declining to credit testimony where “declarant makes these same statements verbatim, without more, and with no additional citations to evidence”). There is no evidence to conclude that Hosomi’s package routing structure is low cost or reliable, and there is no evidence that these unsupported allegations would have served as a POSITA’s motivation to modify Sato. Without evidence to establish a motivation for Petitioner’s proposed modification of Sato, this modification is unsupported.⁶

⁶ During prosecution, the examiner’s statement of reasons for allowance also noted a lack of motivation to combine the prior art in the manner recited by the claims that issued in the ’243 Patent. Ex. 1002, 388.

ii. Petitioner's Proposed Combination of Hosomi and Sato Fails to Identify any "Passive Port[s]" as Claimed

Claim 1 recites, in relevant part, "one or more passive ports for passing through the one or more active signals." The Petition fails to establish that these features are present or suggested by Petitioner's proposed combination of Hosomi and Sato.

Notwithstanding the lack of motivation for Petitioner's combination of Hosomi and Sato, Petitioner implements its combination "using Hosomi's vias as Sato's vertical electrodes, Hosomi's pads as Sato's terminals, Hosomi's wiring layers for Sato's connections, and the modules are connected using the pad/ball connections taught by Hosomi." Petitioner illustrates this implementation at p. 26 of the Petition:

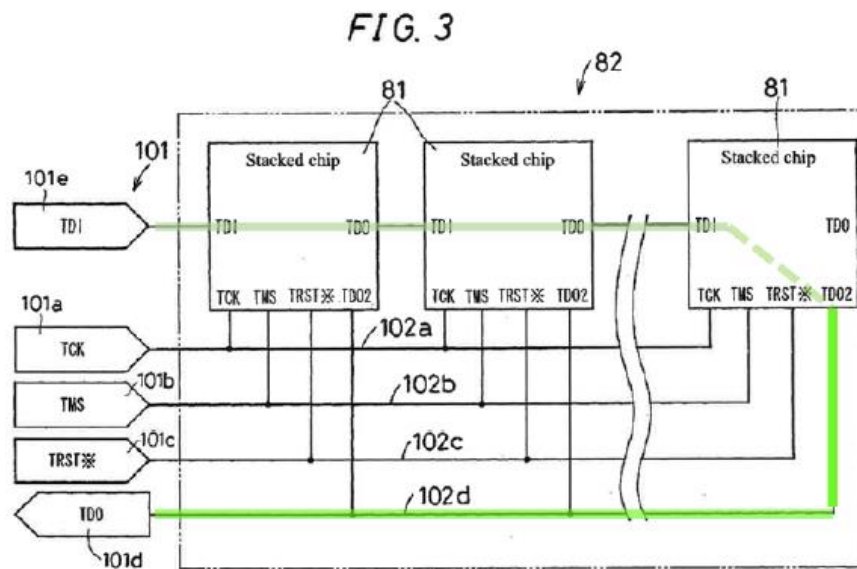


Thompson, Figure A: Hosomi and Sato—Stacked Module

Petitioner's proposed construction for "passive port" is the "connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module." However, as shown above, Petitioner's proposed combination of Hosomi and Sato does not result in a "passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module." Rather, the vertical electrode through the module connects to a wire 115, and pad 116 is arranged on a different layer above the module, insulated from wire 115. Thus, under Petitioner's proposed construction of "passive port," the Hosomi-Sato stacked module's TDI-TDO signal path leading to the top module does not disclose or suggest a "passive ball on one surface of a SDRAM module and a passive pad on another surface of the same

SDRAM module,” and therefore does not disclose a “passive port” under Petitioner’s construction.

Petitioner tacitly concedes this shortcoming of its Hosomi-Sato combination by looking solely to the TDO2 bus descending from the top module as the claimed “passive port.” Petitioner argues that “the controller in the top SDRAM module in the stacked module of Hosomi and Sato outputs TDO2 (shaded neon green) to bus 102d (‘TDO2 bus’) which passes TDO2 through the stack to the external JTAG tester.” Pet., 30.



Sato, Annotated Figure 3

Pet., 31. However, this argument and reliance on signal line TDO2 for the claimed “passive port” includes a logical gap that is never addressed or reconciled by Petitioner. Specifically, claim 1 requires that the claimed “one or more passive

ports [are] for passing through the one or more active signals,” and Petitioner fails to establish that the signal on TDO2 bus is an “active signal.”

In its analysis of the “passive port” term, Petitioner argues that “TDO2 is an ‘active signal’ because it carries the **output data** of a boundary scan of the stacked module.” Pet., 30 (citing Ex. 1003, ¶114) (emphasis added). But this is directly inconsistent with Petitioner’s prior interpretation of “active signal,” which addresses only signals applied *to* circuitry on a module, not any signals output from circuitry.

Earlier in the Petition, Petitioner evaluates the term, “active signal” in the ’243 Patent, and concludes that an “‘active signal’ encompasses a signal **applied to the stack** by an external source and **distributed** via an ‘active port’ **to circuitry on the module.**” Pet., 23 (emphasis added). Applying this interpretation, Petitioner contends that “Sato discloses numerous ‘active signals’ carrying information and used by a boundary scan controller including TDI (data input) and TCK (clock).” Pet., 23. Petitioner continues by characterizing the signals on signal lines TDI, TCK, TMS, and TRST, all of which are distributed *to* the boundary scan controller, as active signals. But Petitioner never contends that the signal on signal line TDO2 is an active signal. Specifically, Petitioner never asserts that an output of the boundary scan controller onto signal line TDO2 is also an “active signal.” Indeed, the output of the boundary scan controller onto signal line TDO2 is never

distributed to circuitry on any module. Reinforcing Petitioner’s failure here, Petitioner only contends that the Hosomi-Sato combination includes “active ports” upstream of the top module’s boundary scan controller. *See* Pet., 25, 26, 28, 29. Petitioner never identifies any “active port[s]” on signal line TDO2. *Id.*

Thus, the signal on signal line TDO2 does not match Petitioner’s own interpretation of “active signal,” and the Petition’s focus on signal line TDO2 for the claimed “one or more passive ports for passing through the one or more active signals” fails.

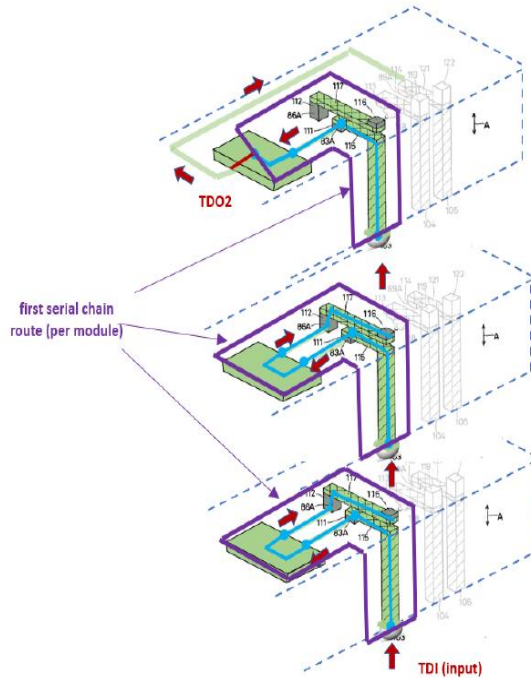
iii. Petitioner’s Proposed Combination of Hosomi and Sato Fails to Disclose a “First Serial Chain Route” of Independent Claim 1

Petitioner also fails to substantiate its contention that its proposed combination of Hosomi and Sato discloses any “first serial chain route” of claim 1. In particular, whether looking at an individual module or a stack of modules, Petitioner has no basis to contend that Hosomi in view of Sato discloses any “first serial chain route,” as claimed.

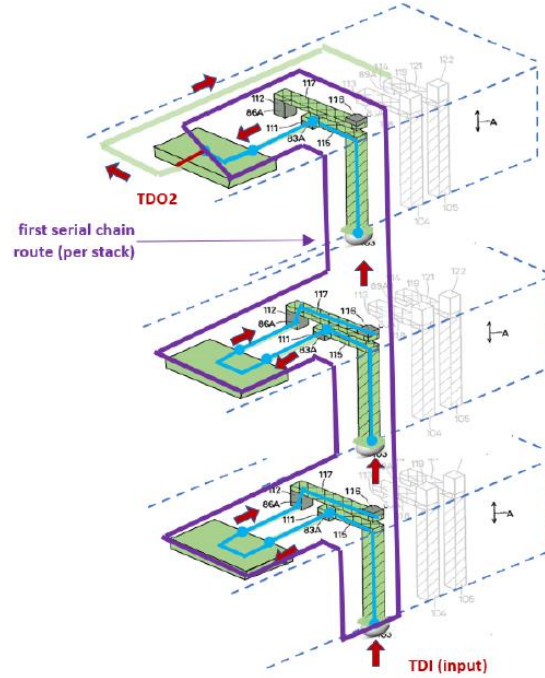
According to claim 1, the “stacked module” comprises in relevant part, “a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit.” Further, the ’243 Patent defines a “serial chain connection” as

follows: “A signal route that includes a serial chain circuit coupling [a] ball and pad is herein after referred to as a ‘serial chain connection’, and at least two serial chain connections connected in series are herein after referred to as a ‘serial chain route’, such as serial chain route 2146 or 2111.” Ex. 1002, 406-07; Ex. 1005 (defining “serial chain connection” and “serial chain route”).

The Petition alleges that the proposed combination of Hosomi and Sato has the claimed “first serial chain route.” Pet., 33. Petitioner states that “test data is input to the TDI signal line of the bottom controller (leftmost device) from an external source. TDI travels up the stack, passed from TDO output of one controller to TDI input of the next, until the top controller is reached.” Pet., 33. Petitioner concludes that “[t]his path from the TDI input of the controller in the bottom module to the TDI input of the controller in the top module includes multiple ‘serial chain connections.’” Pet., 33. Petitioner contends that the proposed combination of Hosomi and Sato discloses the claimed “first serial chain route” per module according to Petitioner’s construction of the preamble, and also per stack according to Patent Owner’s construction of the preamble. Petitioner’s annotations illustrating this “path” per stack and per module are reproduced from the Petition below:



Thompson, Figure F: Petitioner's Construction. (See Pet., 40)



Thompson, Figure G: PO's Construction. (See Pet., 42)

However, applying the '243 Patent's definition of a "serial chain route" and "serial chain connection," a "first serial chain route" of claim 1 must have at least "two serial chain connections connected in series," with each of the two serial chain connections being a "serial chain circuit coupling [a] ball and pad."

Petitioner fails to establish a first "serial chain route" having "at least two serial chain connections [or serial chain circuit coupling a ball and a pad] connected in series" in the proposed combination of Hosomi and Sato under either interpretation of claim 1's preamble. Specifically, as can be seen by each annotation above, the signal chain is interrupted on each module by a stacked chip circuit including the boundary scan controller 80 having a control means 84 and additional circuitry.

See also Ex. 1009, FIG. 1, FIG. 2. Indeed, control means 84 “includes an instruction register and a test data register,” which are each implemented as shift registers. Ex. 1009, 14:29-15:4. This disclosure indicates that the boundary scan controller 80 does not simply serve as a pass-through for data transmitted on the TDI signal line (to be output on the TDO signal line), but rather waits for an “instruction of sending data [that] is input to the control means” 84 to therefore output stored data “through the shift registers.” Ex. 1009, 15:4-8. Petitioner fails to establish that a TDI signal line and TDO signal line are “connected in series” where the lines are not directly connected. Instead, the signal path on each module is interrupted by circuitry and discontinuous, and Petitioner therefore fails to establish any two serial chain circuits coupling a ball and a pad “connected in series” sufficient to establish a “first serial chain route” as claimed.

iv. Petitioner's Proposed Combination of Hosomi and Sato Also Fails to Disclose a “Control Input Signal” of Independent Claim 1

Petitioner's proposed combination of Hosomi and Sato also fails to disclose any “control input signal” as recited in claim 1. Claim 1 recites, in relevant part, “said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.”

Petitioner contends that the identification data in Sato, which is the data being evaluated by comparison means, is a “‘control input signal’ to the ‘control circuit’ because it determines whether the routing path from TDO to TDO2 is enabled in a module.” Pet., 51-52 (emphasis omitted). This incorrect characterization fails, however. Sato is clear that only comparison means 88 in the top module of Petitioner’s proposed combination serves as an input to determine the output of tristate buffer 94 in Fig. 6. See Ex. 1009, 25:19-25. Specifically, the only signal that determines whether there is an output on TDO2 via tristate buffer 94 is the output of comparison means 88. The output of comparison means is not “received from another module from the plurality of modules,” as required by claim 1. Instead, comparison means 88 “makes a comparison as to whether the identification data and the fixed data are matching, and outputs comparison result information.” Ex. 1009, 16:12-18.

No “control input signal” is received from “another module” “to enable the routing path” in Petitioner’s proposed combination of Hosomi and Sato. The combination necessarily fails to disclose or suggest every claimed feature, and claim 1 survives Petitioner’s challenge.

Moreover, Petitioner overlooks that Petitioner’s proposed construction of the preamble would require each module to possess a “control circuit *for enabling a routing path* that connects the first serial chain route with the second serial chain

route within an end module” “in response to a control input signal received from another module.” (emphasis added). But nothing in any control circuit at the bottom or middle module in Petitioner’s proposed Sato-Hosomi combination “enabl[es] a routing path” within the top module. Petitioner concedes as much, stating that “in the top module ... the comparison result (match condition) turns on the tristate buffer causing the output of control means 84 (TDO) to be output on signal line TDO2.” Pet., 47-48. As previously noted, Sato is clear that only comparison means 88 in the top module of Petitioner’s proposed combination serves as an input to determine the output of tristate buffer 94 in Fig. 6. *See* Ex. 1009, 25:19-25.

Under these facts, Petitioner fails to explain how each claimed feature is satisfied under Petitioner’s proposed construction of “plurality of modules,” which would require each module to include a “control circuit for enabling a routing path ... within an end module” “in response to a control input signal received from another module.” At most, Petitioner describes the operation of the top module and concludes that this feature is met for each module. Pet., 49. This is wrong.

v. Ground 1’s Challenge Fails to Establish the Unpatentability of Claim 1

For all of the reasons presented above, Petitioner’s proposed combination of Sato and Hosomi is unsupported by the requisite motivation and, as combined, fails to disclose or suggest every claimed feature of claim 1. Therefore, claim 1

survives Petitioner’s Ground 1 challenge. Further, for these same reasons, dependent claims 2, 11, and 12 also survive Petitioner’s Ground 1 challenge.

vi. Petitioner’s Proposed Combination of Hosomi and Sato Also Fails to Disclose Every Feature of Dependent Claim 2

Without disclaiming the independent patentability of any other dependent claim, Petitioner’s proposed combination of Hosomi and Sato also fails to disclose every feature of claim 2 under any construction of “passive port.”

Claim 2 depends from claim 1 and further recites, in relevant part, “wherein the one or more passive port forms a ladder like routing path, and the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module.” An exemplary “ladder like routing path” is described in the ’243 Patent with reference to FIG. 19: “The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in FIG. 19, is named ‘passive port’, [such] as passive ports 1909 illustrated in FIG. 19. The technique involves using a ladder-like routing path, such as 1905 on the stacked modules.” Ex. 1002, 405; Ex. 1005. This exemplary ladder-like routing path 1905 is illustrated in Figure 19, also reproduced below.

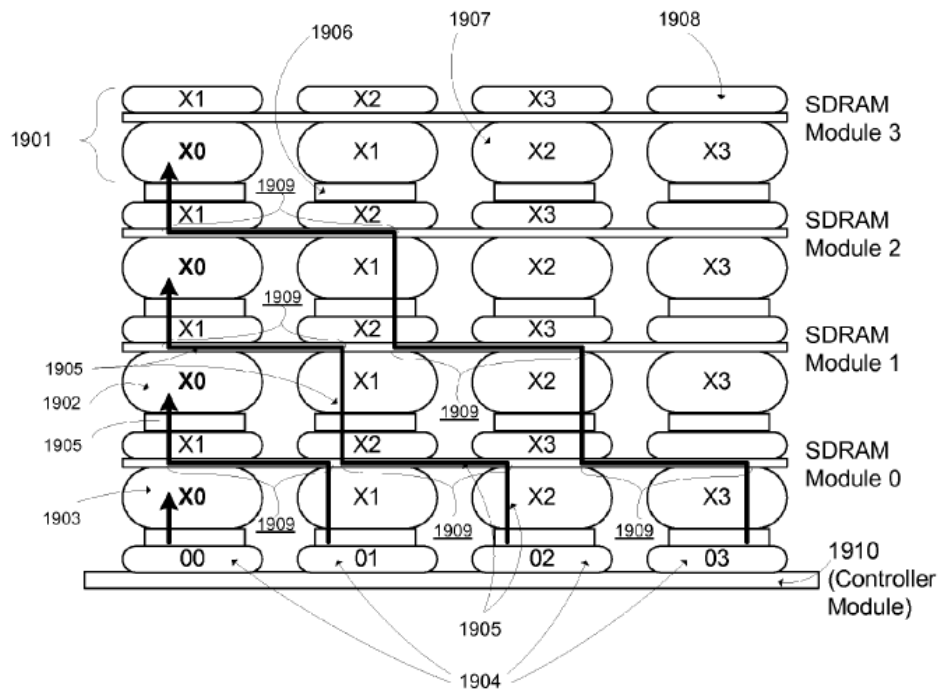
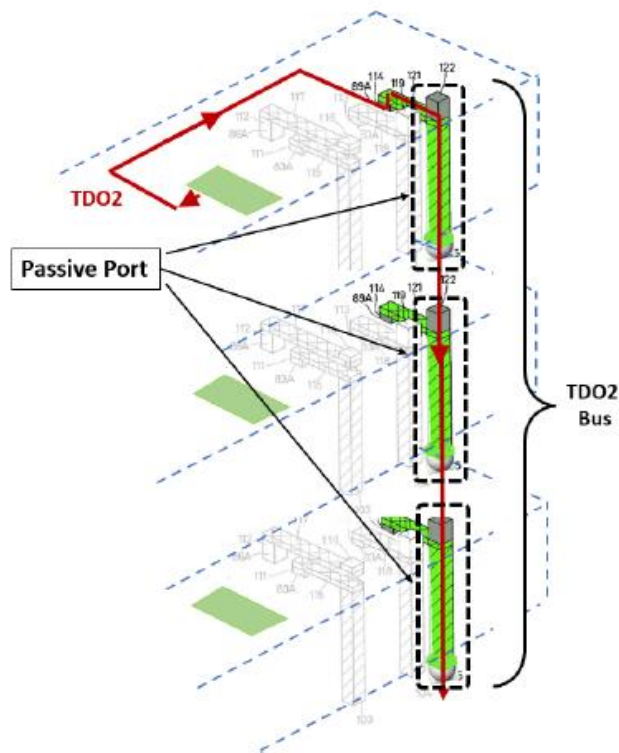


Figure 19

As shown, the exemplary ladder-like routing path of a passive port connects a ball X2 on one side of Module 0 and pad X2 on another side of Module 0. Similarly, the exemplary ladder-like routing path of a passive port connects a ball X1 on one side of Module 1 and pad X1 on another side of Module 1. As such, in the exemplary ladder-like routing path illustrated and described in the specification, a passive port forms the ladder like routing path, and the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module. These features are not disclosed in the Petitioner's asserted combination of references, however.

Petitioner contends that “passive ports in the combination of Hosomi and Sato ‘form[] a ladder like routing path’ [2A] because they create a series of ‘rungs’ allowing a signal to pass horizontally in each module and to travel up or down the stack” Pet., 54. But Petitioner’s illustration of the proposed combination tells a different story. Specifically, Petitioner provides an annotated version of the proposed combination that illustrates no “ladder like routing path” formed by any passive port “connect[ing] a passive ball on one surface of a module to a passive pad on another surface of the module,” as required by claim 2. As shown in Petitioner’s illustration below, there is only a descending signal path TDO2 associated with the alleged passive ports in the asserted combination.



Pet., 55 (citing Ex. 1003, ¶146). This illustration fails to disclose or suggest any ladder like routing path formed by a passive port. Petitioner's mention of a signal passing "horizontally in each module" is not explained, but to the extent that Petitioner intended to point to the stepped shape of the signal route in red, corresponding to wiring 119, this stepped shape is outside of the alleged passive ports in Petitioner's combination. As plainly shown in Petitioner's illustration, the stepped shape is not formed by any passive port "connect[ing] a passive ball on one surface of a module to a passive pad on another surface of the module." Petitioner's illustration of its proposed combination fails to disclose the express features of claim 2, and is also materially distinct from the exemplary signal path disclosed in Figure 19 of the '243 Patent, which discloses a connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, that forms a ladder-like routing path.

Petitioner's proposed combination of Hosomi and Sato fails to disclose or suggest the claimed features of claim 2.

B. Ground 2 Based on Sung in View of Watanabe Also Fails

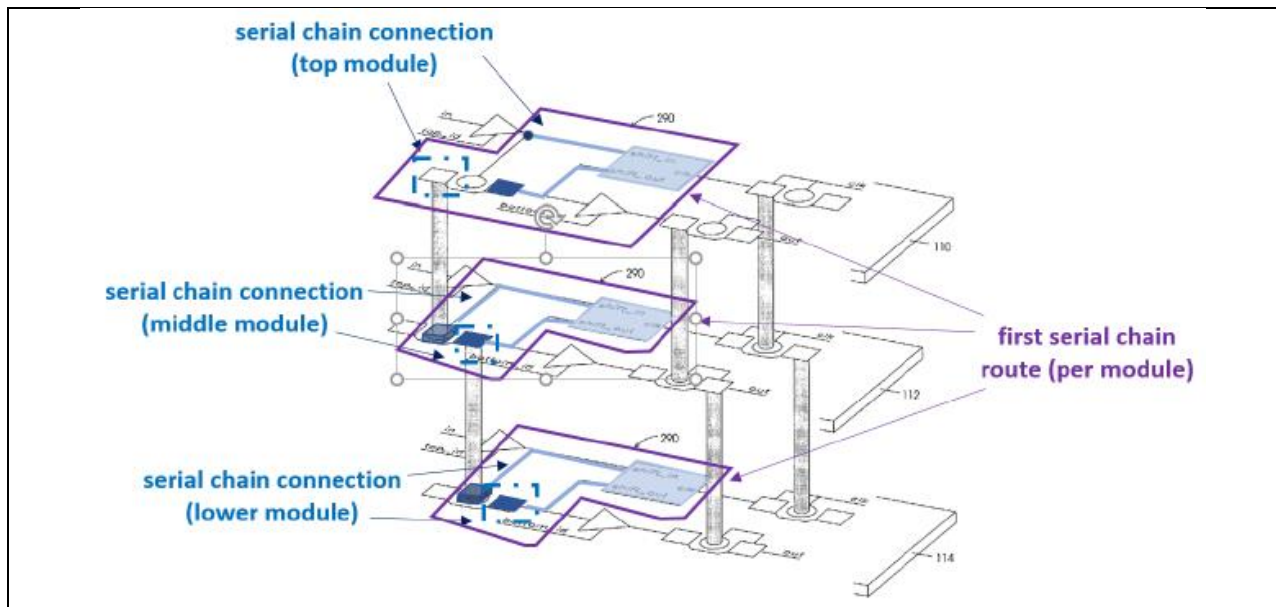
i. Petitioner's Proposed Combination of Sung and Watanabe Fails to Disclose a "First Serial Chain Route" of Independent Claim 1

Just as with Ground 1, Petitioner also fails to substantiate its contention that its proposed combination of Sung in view of Watanabe discloses any "first serial

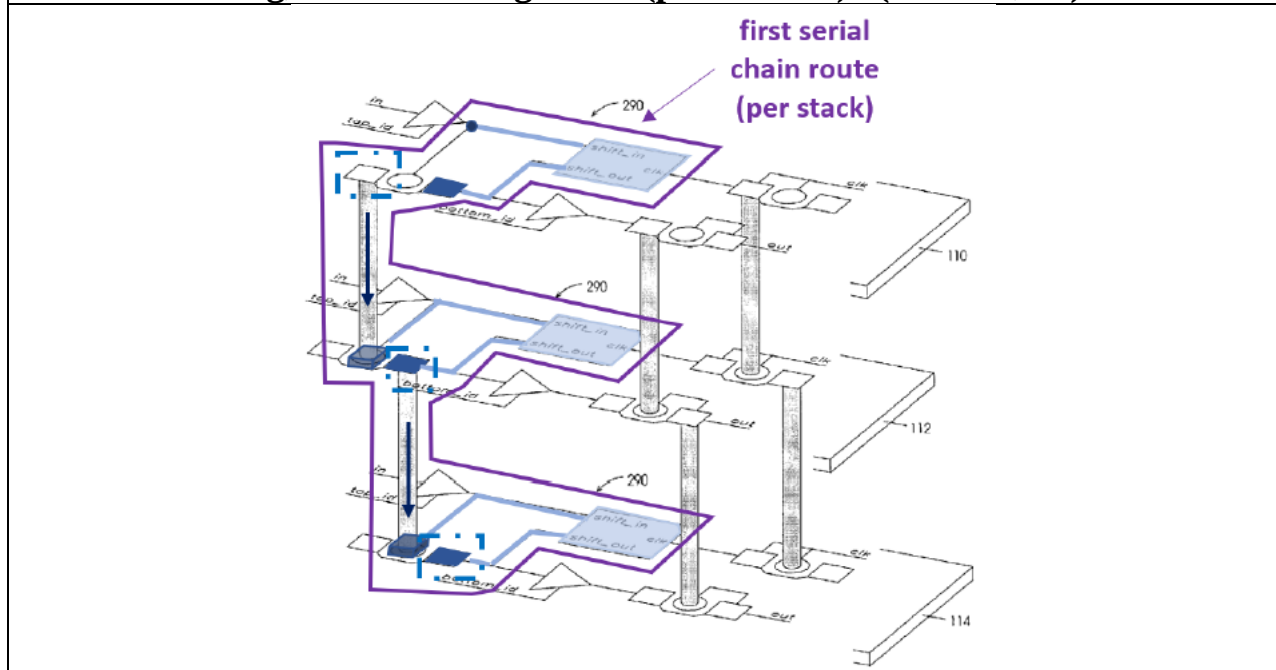
chain route” of claim 1. In particular, whether looking at an individual module or a stack of modules, Petitioner has no basis to contend that Sung in view of Watanabe discloses any “first serial chain route,” as claimed.

According to claim 1, the “stacked module” comprises in relevant part, “a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit.” Further, the '243 Patent defines a “serial chain connection” as follows: “A signal route that includes a serial chain circuit coupling [a] ball and pad is herein after referred to as a ‘serial chain connection’, and at least two serial chain connections connected in series are herein after referred to as a ‘serial chain route’, such as serial chain route 2146 or 2111.” Ex. 1002, 406-07; Ex. 1005 (defining “serial chain connection” and “serial chain route”).

The Petition alleges that Petitioner's proposed Sung-Watanabe combination has the claimed “first serial chain route.” See Pet., 82. Petitioner's annotations illustrating this “first serial chain route” per stack and per module are reproduced from the Petition below:



Sung, Annotated Figure 10 (per module). (See Pet., 85)



Sung, Annotated Figure 10 (per stack). (See Pet., 86)

However, applying the '243 Patent's definition of a "serial chain route" and "serial chain connection," a "first serial chain route" of claim 1 must have at least

“two serial chain connections connected in series,” with each of the two serial chain connections being a “serial chain circuit coupling [a] ball and pad.”

Petitioner fails to establish a first “serial chain route” having “at least two serial chain connections [or serial chain circuit coupling a ball and a pad] connected in series” in the proposed combination of Sung and Watanabe under either interpretation of claim 1’s preamble.

Specifically, as can be seen by each annotation above, the signal chain is interrupted on each module by the shift register. The shift register does not simply serve as a pass-through for data transmitted on the signal line. As Sung discloses, “information is passed from latches or registers 294 on one level of the stack to latches or registers on another level of the stack” according to a clock signal. Sung, [0049]. Petitioner fails to establish that two signal lines are “connected in series” where the signal lines are disconnected and separated by such circuitry, and therefore fails to establish any two serial chain circuits coupling a ball and a pad “connected in series” sufficient to establish a “first serial chain route” as claimed.

ii. Petitioner’s Proposed Combination of Sung and Watanabe Also Fails to Disclose a “Control Input Signal” of Independent Claim 1

Petitioner’s proposed combination of Sung and Watanabe also fails to disclose any “control input signal” as recited in claim 1. Claim 1 recites, in relevant part, “said control circuit is disposed to enable the routing path in response

to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.”

Petitioner contends that a ground signal in Sung is a “control input signal received from another module from the plurality of modules when the end module is coupled to the another module.” Pet., 94 (emphasis omitted). But the logic of Petitioner’s characterization is erroneous, as confirmed by Petitioner’s own discussion of Sung’s operation of tristate buffer 296. Per Sung, the tristate buffer 296 is only enabled when a bottom_id signal is “asserted,” or input to the tristate buffer 296. Sung, [0049] (“The tristate buffer 296 is controlled by the bottom_id signal generated by the bottom die identifier circuit 230.”). As Petitioner explains, “[w]hen Sung’s module has another module below it in the stack, the bottom_id circuit is grounded, the bottom_id signal is *not asserted*, and tristate buffer 296 in the scan chain circuit is *disabled*.” Pet., 94 (citing Ex. 1003, ¶233-234) (emphasis added). The only reason the bottom_id signal is asserted—or applied to the tristate buffer 296—in the bottom module of Sung is because there is no other module below that module. The bottom_id signal is not input to the tristate buffers in the middle and top modules, but even under Petitioner’s theory, the grounded connection *disables* the tristate buffers in modules other than an end module, and *does not enable* a routing path in the end module. Thus, Petitioner’s reliance on a

grounded connection as the claimed “control input signal” improperly turns claim 1 on its head.

Further, Petitioner does not contend that the `bottom_id` signal is received from another module. If they did, such a contention would be plainly wrong. Even under Petitioner's reworking of Sung to include an undisclosed V_{DD} voltage⁷ at each module, the V_{DD} voltage is applied at the bottom module in Petitioner's annotation.

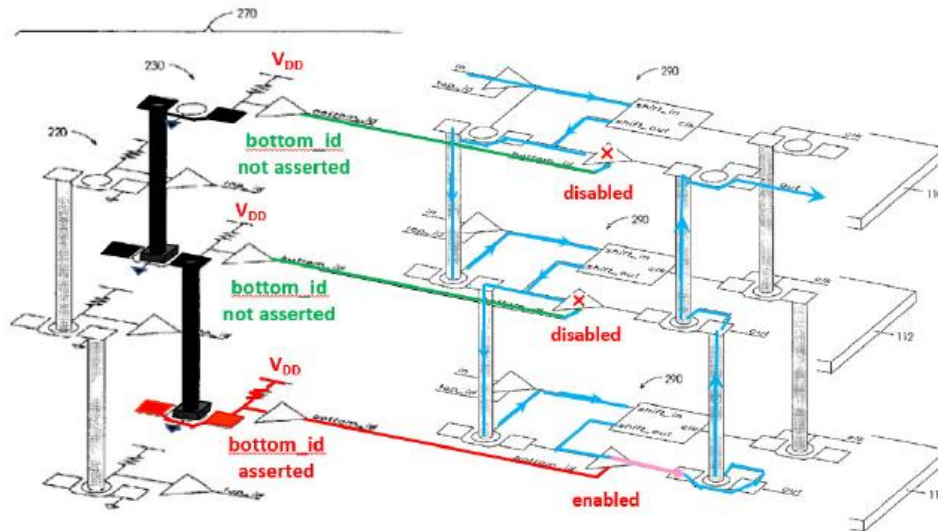


Figure 6: Die Identification Circuit

Figure 10: Inter-die communications chain for multiple dies.

Figure 10

Sung, Annotated Figures 6 and 10

Notably, in order to fabricate a “control input signal” in this Ground 2 challenge, Petitioner first creates an applied voltage V_{DD} that is not disclosed in

⁷ The voltage V_{DD} is an addition by Dr. Thompson, not in the disclosure of Sung. See Pet., 92 (“Although not shown in Figure 5, a POSITA would have understood ...”).

Sung, and then further creates a mechanism for transmitting voltage V_{DD} that first passes through a prior layer. Pet., 95-96. Thus, Petitioner’s challenge for this “control input signal” element is not based upon a patent or printed publication, but rather upon an expert’s testimony in violation of the controlling IPR statute. See 35 U.S.C. § 311(b).

No “control input signal” is received from “another module” “to enable the routing path” in Petitioner’s proposed combination of Sung and Watanabe. The bottom_id signal is applied to the tristate buffer 296 because no other module is connected to the bottom module in this stack of modules, and Petitioner points to no disclosure to the contrary.

Moreover, Petitioner once again overlooks the further claimed requirement of “a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module.” In Petitioner’s proposed construction of the preamble, each module would require a “control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module,” “in response to a control input signal received from another module.” But nothing in any control circuit at the top or middle module in the Sung-Watanabe combination “enabl[es] a routing path that connects” two serial chain routes within the bottom (or end) module. Petitioner concedes this failure by noting that only the bottom module’s shift_out signal is

responsible for conveying “data to the top of the stack 110 and then to a location external to the stack.” Pet., 86-87 (quoting Ex. 1010, ¶49). This is consistent with Petitioner’s Annotated Figures 6 and 10 from Sung, appearing on page 94 of the Petition and reproduced below:

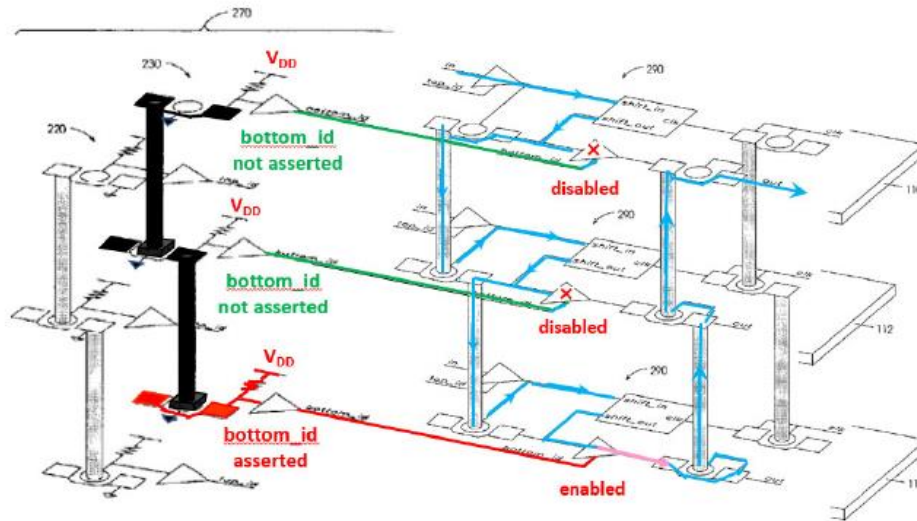


Figure 6: Die Identification Circuit

Figure 10: Inter-die communications chain for multiple dies.

Figure 10

Sung, Annotated Figures 6 and 10

As shown, only the bottom_id signal applied to the tristate buffer 296 on the bottom module controls whether the tristate buffer 296 on the bottom module enables a routing path up through the stack. Under these facts, this claimed “control circuit” requirement is not satisfied under Petitioner’s proposed construction of “plurality of modules,” which would require each module to include a “control circuit for enabling a routing path ... within an end module” “in response to a control input signal received from another module.”

The combination necessarily fails to disclose or suggest every claimed feature, and claim 1 survives Petitioner's Ground 2 challenge.

iii. Ground 2's Challenge Fails to Establish the Unpatentability of Claim 1

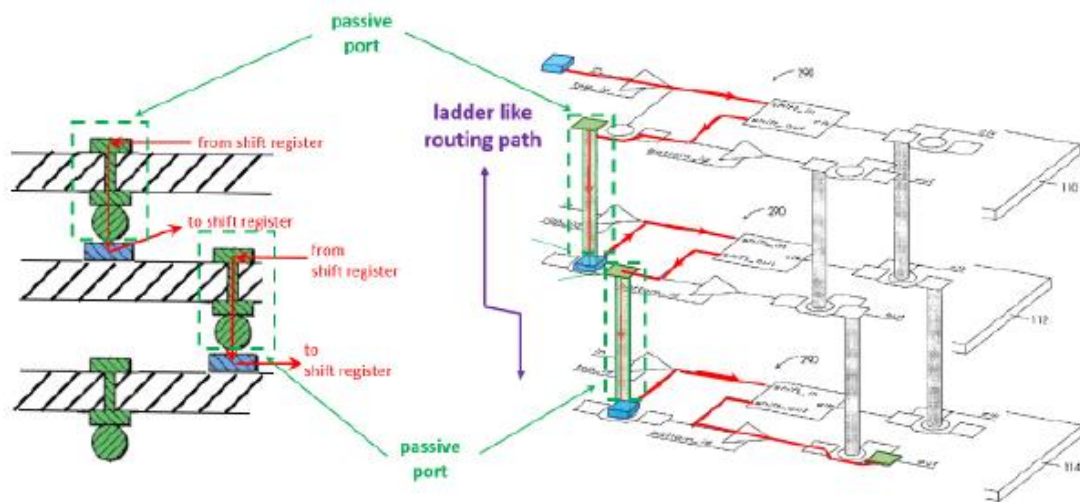
For all of the reasons presented above, Petitioner's proposed combination of Sung and Watanabe fails to disclose or suggest every claimed feature of claim 1. Therefore, claim 1 survives Petitioner's Ground 2 challenge. Further, for these same reasons, dependent claims 2, 11, and 12 also survive Petitioner's Ground 2 challenge.

iv. Petitioner's Proposed Combination of Sung and Watanabe Also Fails to Disclose Every Feature of Dependent Claim 2

Without disclaiming the independent patentability of any other dependent claim, Petitioner's proposed combination of Sung and Watanabe also fails to disclose every feature of claim 2 under any construction of "passive port." Claim 2 depends from claim 1 and further recites, in relevant part, "wherein the one or more passive port forms a ladder like routing path, and the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module."

Petitioner contends that "passive ports in Sung's scan chain communications circuit 290 are staggered, forming a ladder-like routing path through the stack." Pet., 99-100. However, Petitioner's annotated version of Sung's Figure 10

illustrates no “ladder like routing path” formed by any passive port “connect[ing] a passive ball on one surface of a module to a passive pad on another surface of the module,” as required by claim 2.



Pet., 100. This illustration fails to disclose or suggest any ladder like routing path formed by a passive port. For example, the angle in Petitioner’s purple arrow is not associated with any passive port. Any stepped shape due to the signal path passing through shift registers on each module is outside of the alleged passive ports in Petitioner’s combination. As plainly shown in Petitioner’s illustration, the stepped shape is not formed by any passive port “connect[ing] a passive ball on one surface of a module to a passive pad on another surface of the module.”

Petitioner’s illustration of its proposed combination fails to disclose the express features of claim 2, and is also materially distinct from the exemplary signal path disclosed in Figure 19 of the ’243 Patent, which discloses a connection

between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, that forms a ladder-like routing path.

Therefore, Petitioner's proposed combination of Sung and Watanabe also fails to disclose or suggest the claimed features of claim 2.

IV. CONCLUSION

For the reasons presented above, the Petition should be denied, and no *inter partes* review should be instituted.

Dated: July 26, 2023

/s/ Wayne M. Helge

Wayne M. Helge (Reg. No. 56,905)

NOSSAMAN, LLP

1401 New York Ave, NW

Suite 800

Washington, DC 20005

Telephone: (202) 887-1400

Email: whelge@nossaman.com

James T. Wilson (Reg. No. 41,439)

DAVIDSON BERQUIST JACKSON &

GOWDEY, LLP

8300 Greensboro Dr., Suite 500

McLean, VA 22102

Telephone: (571) 765-7700

Fax: (571) 765-7200

Email: jwilson@dbjg.com

Counsel for Patent Owner

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 7,037 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a).

By: /s/ Wayne M. Helge
Wayne M. Helge (Reg. No. 56,905)
Attorney for Patent Owner

CERTIFICATE OF SERVICE

I hereby certify that on July 26, 2023, a true and correct copy of the foregoing document was served via email, by consent, to Petitioner by serving the correspondence email addresses of record as follows:

Lori A. Gordon
Reg. No. 50,633
PERKINS COIE LLP
700 Thirteenth Street, N.W.,
Suite 800
Washington, DC 2005-3960
(202) 654-6200
gordon-ptab@perkinscoie.com

Christina J. McCullough
Reg. No. 58,720
PERKINS COIE LLP
1201 Third Avenue
Suite 4900
Seattle, Washington 98101-3099
(206) 359-6897
mccullough-ptab@perkinscoie.com

Matthew W. Hindman
Reg. No. 57,396
Yuanfeng Gao
Reg. No. 79,573
PERKINS COIE LLP
3150 Porter Drive
Palo Alto, CA 94304-1212
(650) 838-4300
hindman-ptab@perkinscoie.com
gao-ptab@perkinscoie.com

/s/ Wayne M. Helge
Wayne M. Helge (Reg. No. 56,905)
Attorney for Patent Owner