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Paper 7
Entered: October 24, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BITMICRO, LLC,
Patent Owner.

IPR2023-00781
Patent 7,826,243 B2

Before KEN B. BARRETT, KRISTINA M. KALAN, and KEVIN C. TROCK, *Administrative Patent Judges.*

TROCK, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 1, 2, 11, and 12 (the "challenged claims") of U.S. Patent No. 7,826,243 B2 (Ex. 1001, "the '243 patent"). BiTMICRO, LLC ("Patent Owner") filed a Preliminary Response (Paper 6, "Prelim. Resp.").

The Board has authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), we may not authorize an *inter partes* review unless the information in the petition and the preliminary response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. We therefore institute *inter partes* review as to all of the challenged claims of the '243 patent and all of the asserted grounds of unpatentability in the Petition.

II. BACKGROUND

A. Related Matters

The parties identify the following district court proceedings involving the '243 patent: *BiTMICRO LLC v. Intel Corp.,* Case No. 5:23-cv-00625 (N.D. Cal.) (transferred from the District Court for the Western District of Texas, Case No. 6-22-cv-00335). Pet. 106; Paper 4, 2. Patent Owner also identifies another related, terminated USPTO proceeding, IPR2018-01720 (PTAB), involving the '243 patent. Paper 4, 2.

B. Real Parties-in-Interest

Petitioner identifies Intel Corporation as the real party-in-interest. Pet. 106. Patent Owner identifies BiTMICRO, LLC, as the real party-in-interest. Paper 4, 2.

Based on the current record, we determine that Petitioner has established compliance with the statutory requirement under 35 U.S.C. § 312(a)(2) to identify all real parties in interest.

C. The '243 Patent

The '243 patent is entitled "Multiple Chip Module and Package Stacking for Storage Devices." Ex. 1001, code (54). The patent "relates to flash memory-based semiconductor disk drives and a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability." *Id.* at 1:8–12.

The '243 patent explains that "flash memory based semiconductor disk drive[s] typically use separate packages for the interface controller, the DMA [direct memory access] controller, the processor and separate packages for the Flash devices," but this "limits the miniaturization of the entire storage device." *Id.* at 1:14–19. Because "[s]tacking both on chip module and package level maximizes the capacity in a limited area," the patent proposes a "technique in stacking chip modules and packages strategically to support miniaturization and memory scalability in both vertical and horizontal orientation." *Id.* at 1:21–27.

The '243 patent explains that it uses a "combination of different existing technology such as flip chip, wire bond, MCM, module stacking, advance packaging, etc." *Id.* at 1:38–42. Figure 2c, reproduced below, shows a cross-sectional representation of stacked multiple SDRAM

(synchronous dynamic random-access memory) modules according to an embodiment of the '243 patent.

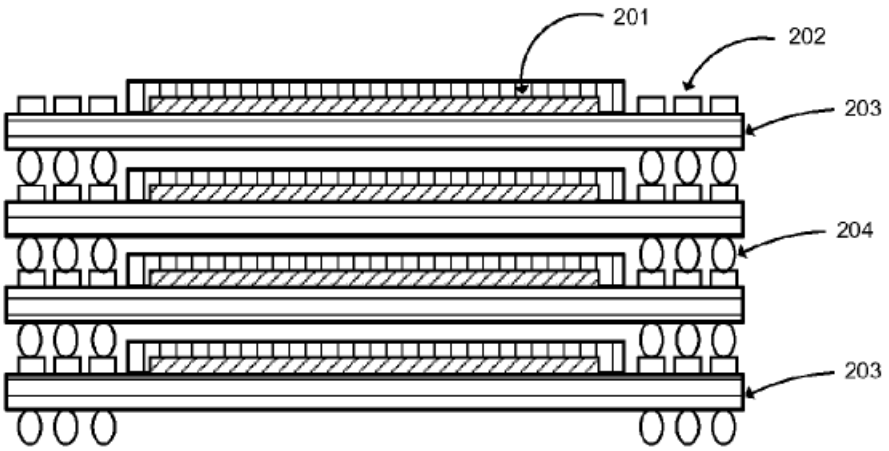


Figure 2c, above, shows SDRAM die 201, substrate 203, top pads 202, and bottom balls 204, where "[t]op pads 202 and bottom balls 204 act as the vertical interconnects between all SDRAM modules and to the controller module." *Id.* at 4:32–34.

The '243 patent also describes a connection technique used for serial routing of all modules in a stack that allows them to be externally accessible for horizontal expansion on a printed circuit board, such as a main board. Figure 21a, below, shows how this technique is implemented in the stacking method.

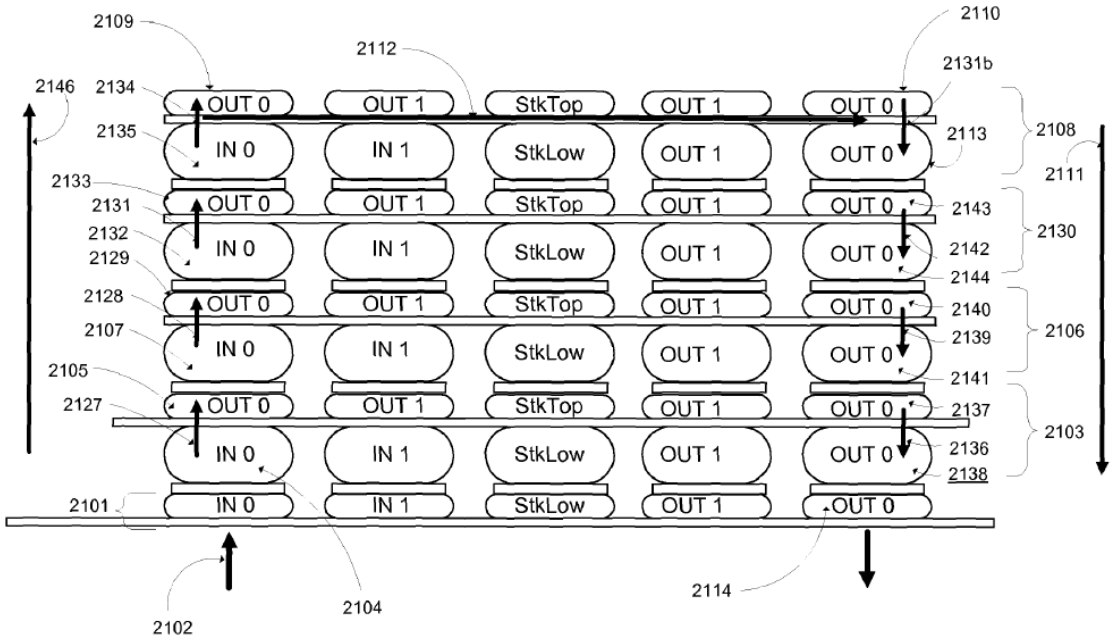


Figure 21a

In Figure 21a, above, main board 2101 receives the input signal 2102 which will then be connected to IN ball 2104 of the base module 2103. *Id.* at 9:65–68. The base module's OUT pad 2105 is connected to IN ball 2107 of the first stack module 2106, and so on. *Id.* at 9:68–10:2. The top module 2108 terminates the signal to the top pad 2109 and routes, with connection 2112, the signal internally to another pad 2110 which is connected directly to the ball 2113 underneath. *Id.* at 10:2–5. As the modules are identical, this routed signal passes through another set of serial chain connections that comprise another serial chain route, such as serial chain route 2111, until it reaches OUT pad 2114 of the main board for external access. *Id.* at 10:5–8; *see also* Ex. 1005, 2.

D. Illustrative Claim

The '243 patent has 15 claims. As noted, claims 1, 2, 11, and 12 are challenged in the Petition. Pet. 1. Claim 1 is the only independent claim. Claim 1 is illustrative of the claimed subject matter and is reproduced below:

> 1. A stacked module comprising a plurality of modules each comprising:
>
> one or more active ports for carrying one or more active signal;
>
> one or more passive ports for passing through the one or more active signals;
>
> a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;
>
> a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and
>
> said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Ex. 1001, 10:42–60.

E. Prior Art References and Other Evidence

Petitioner relies on the following references:

1. Hosomi, U.S. Patent Application Publication No. 2001/0028114 A1 (October 11, 2001), (Ex. 1007, "Hosomi").

2. Sato, International Patent Application Publication No. WO 2004/072667 A2 (August 26, 2004) (Ex. 1009, "Sato").[1]

3. Sung, et al., U.S. Patent Application Publication No. 2003/0178228 A1 (September 25, 2003) ("Sung," Ex. 1010).

4. Watanabe, et al., U.S. Patent No. 6,791,193 B2 (September 14, 2004) ("Watanabe," Ex. 1011).

In addition to these references, Petitioner relies on a Declaration of Scott E. Thompson, Ph.D. Ex. 1003 ("Thompson Decl.").

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 3.

Claim(s) Challenged	Basis 35 U.S.C. §	Reference(s)
1, 2, 11, 12	103(a)[2]	Hosomi, Sato
1, 2, 11, 12	103(a)	Sung, Watanabe

III. ANALYSIS OF THE CHALLENGED CLAIMS

A. Applicable Legal Standards

A claim is unpatentable as obvious under 35 U.S.C. § 103 "if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103 (2011). The

[1] Exhibit 1009 is a certified translation of the Japanese language application in Exhibit 1008.

[2] Because the application from which the '243 patent issued has an effective filing date before March 16, 2013 (Ex. 1001, (22)), citations to 35 U.S.C. § 103 are to the pre-AIA version. Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29.

question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) so-called "secondary considerations," including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

B. Level of Ordinary Skill in the Art

According to Petitioner, a person of ordinary skill in the pertinent art "would have had (1) a bachelor's degree in electrical engineering or similar discipline, and two to three years of work experience in semiconductor packaging or (2) a master's degree with one or more years of experience in those fields." Pet. 5 (citing Thompson Decl. ¶ 68).

Patent Owner does not address the level of skill of the ordinary artisan. *See generally* Prelim. Resp.

We regard Petitioner's definition as consistent with the '243 patent and the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Therefore, for the purpose of this decision, we adopt Petitioner's formulation.

C. Claim Construction

For this *inter partes* review, the Board applies the same claim construction standard as that applied in federal courts. *See* 37 C.F.R § 42.100(b) (2023). Under this standard, claim terms "are generally given their ordinary and customary meaning" as understood by a person of

ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc) (citations omitted). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–1317). Extrinsic evidence is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (citation omitted).

Petitioner contends that two terms require construction: "a plurality of modules each comprising," and "passive port." Pet. 6–8.

1. "a plurality of modules each comprising"

Petitioner contends this term "is not part of the preamble and should be construed as 'each module in the stacked module comprising.'" Pet. 6.

Patent Owner contends the term is part of the preamble and not a limitation of the claim. Prelim. Resp. 10. Patent Owner asserts that "Petitioner incorrectly argues that the effect of its proposed construction means that each module in a stacked module must be identical in structure," which "requires each module in a stacked module to possess every claimed feature." *Id.*

2. "passive port"

Petitioner contends "passive port" should be construed as "connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module." Pet. 7.

Patent Owner appears to indicate that the term may be construed as a "connection between a passive ball and a passive pad." Prelim. Resp. 10; *see also* Ex. 1026, 13–15.

Only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). For purposes of this Decision and based on this preliminary record, we determine that no claim terms require express construction at this stage of the proceeding.

D. Prior Art References

1. Hosomi (Ex. 1007)

Hosomi is a patent titled "Semiconductor Device Including Memory Unit and Semiconductor Module Including Memory Units." Ex. 1007, code (54). Hosomi "relates to a semiconductor device has at least one of memory unit which can lay over one after another and a semiconductor module has at least a plurality of memory units which can lay over one after another." *Id.* ¶ 3. Hosomi discloses a semiconductor device which comprises:

> a memory unit; a selecting signal terminal for receiving a memory unit selecting signal which is common to a plurality of memory units; and an identifying unit which includes at least a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal, and an identifier generating circuit for generating identifiers for other memory units on the basis of the identifier.

Id. ¶ 25.

Figure 5, reproduced below, shows a cross section of a semiconductor module in which a plurality of semiconductor devices of a flip chip structure are stacked. *Id.* ¶ 55.

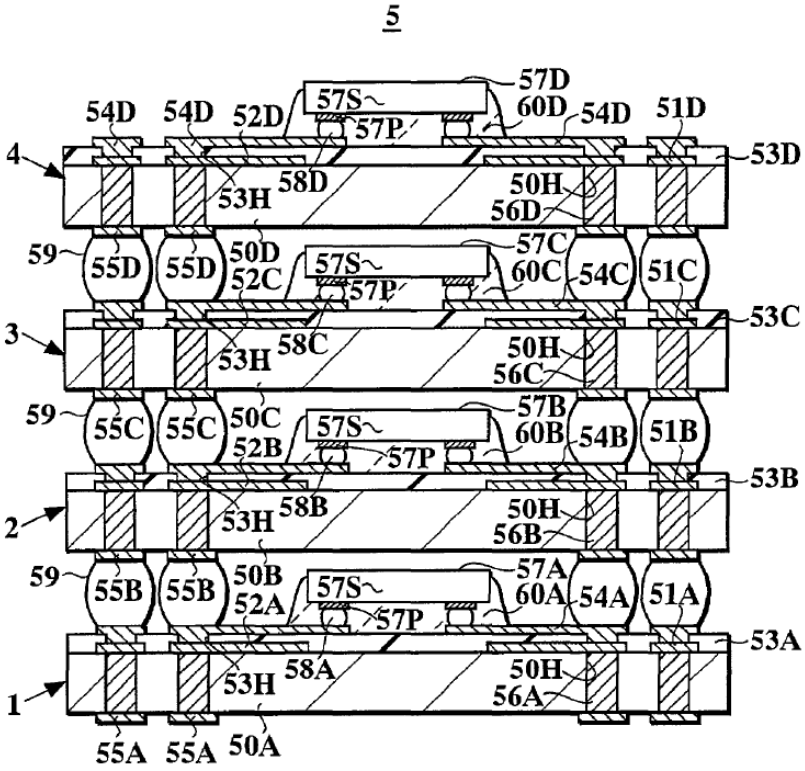


Figure 5 shows semiconductor devices 1 to 4 which are stacked one over another. *Id.* ¶ 94. With respect to Figure 5, Hosomi explains:

> The package substrate 50A is made of an insulating material such as epoxy resin or ceramics and so on, and is provided with front electrodes 51A and rear electrodes 55A on the opposite surfaces thereof, and two wiring layers 52A and 54A on the front surface thereof. The number of wiring layers is variable. The front and rear electrodes 51A and 55A are electrically connected via a connecting hole 50H in the package substrate 50A. The front electrode 51A and the first wiring layer 52A are flush with each other and are made of the same conductive material. The second wiring layer 54A is arranged on the first wiring layer 52A via an inter-layer insulating layer 53A, and is electrically connected to the first wiring layer 52A via a connecting hole 53H in the inter-layer insulating layer 53A. The

> front and rear electrodes 51A and 55A, and the first and second wiring layers 52A and 54A are made of conductive materials such as copper, copper alloy and so on.

Id. ¶ 96.

2. Sato (Ex. 1009)

Sato is an international patent application publication entitled "Boundary Scan Controller, Semiconductor Device, Method for Identifying Semiconductor Circuit Chip of Semiconductor Device, and Method for Controlling Semiconductor Circuit Chip of Semiconductor Device." Ex. 1009, code (54). Sato "relates to a boundary scan controller for testing connection states of input/output terminals of a plurality of semiconductor circuit chips which constitute a semiconductor device, for example, a three dimensional multilayered LSI (Large Scale Integration)." *Id.* at 1:9–12.

Sato describes that "[a]s demand for high density packaging of semiconductor circuit chips such as large scale integration (abbreviated to 'LSI') has increased, it has been proposed to enhance packaging density by stacking semiconductor circuit chips in a vertical direction." *Id.* at 1:14–16. Sato describes a need "to identify the individual chips of the chips to be stacked, similar to the case of the multilayered module of tape carrier packages." *Id.* at 2:12–14. "[I]n a semiconductor device for achieving high density packaging, there are mounted circuits for electrically testing whether or not the packaged chips are connected, that is, boundary scan controllers." *Id.* at 4:2–4.

Sato's boundary scan controller is described as including five signal lines: "TDI (Test Data input: data input part), TDO (Test Data Output: data output part), TCK (Test Clock input: clock input part), TMS (Test Mode Select input: test mode input part) and TRST (Test Reset input: test reset

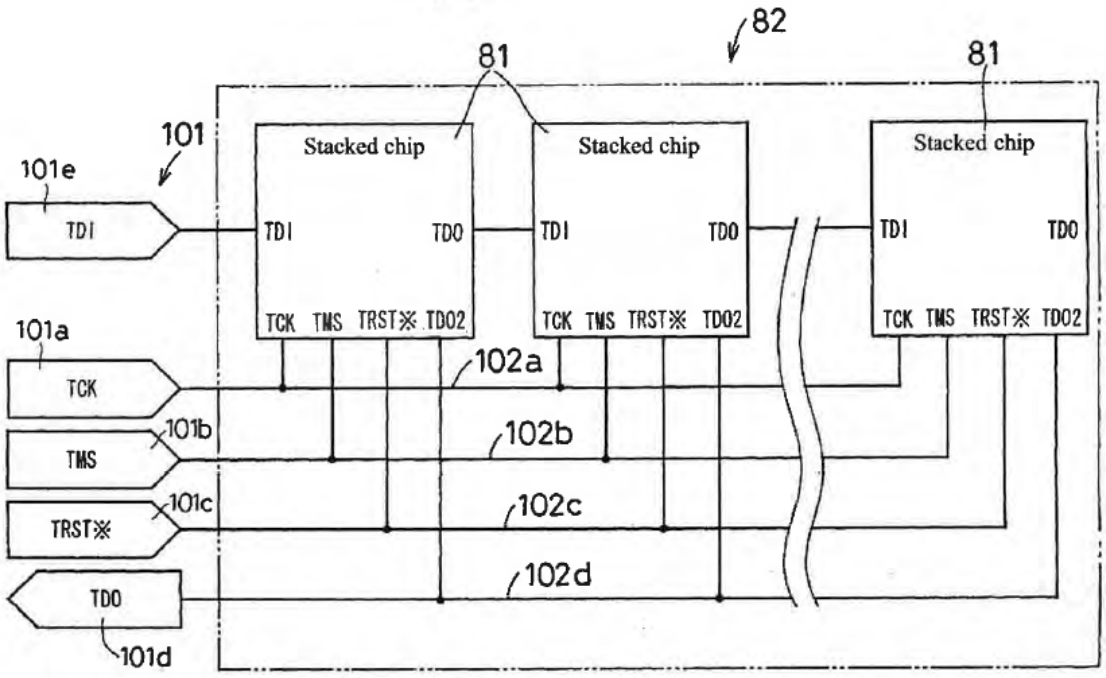
input part) for the standards of a boundary scan test," where the signal line TRST is optional. *Id.* at 4:5–8. Sato describes that "signal lines TDI and TDO of the boundary scan controller incorporated in the individual chips in the semiconductor device are connected in the shape of a chain." *Id.* at 4:10–14. Sato further describes that "the chain-like connection of the boundary scan controllers will be sometimes be referred to as a 'daisy chain,'" and "signal lines TCK, TMS, TDI and TRST are generally referred to as 'input parts'." *Id.* Sato explains that during a boundary scan test:

> In the daisy chain, the data output part of the boundary scan controller of a lower stage is connected to the data input part of the boundary scan controller of an upper stage. Furthermore, the test result data is derived from the data output part of the boundary scan controller disposed in the semiconductor circuit chip of the uppermost stage. In the boundary scan test, the inputs of the operation instruction, identification data and test data from each input part to the boundary scan controller, and the output data are detected by a JTAG tester.

Id. at 8:6–12.

Sato's Figure 3 is shown below.

FIG. 3



Sato's Figure 3, above, is a block diagram illustrating a semiconductor device 82 which is configured by stacking a plurality of semiconductor circuit chip assemblies 81. Ex. 1009, 12. With respect to Figure 3, Sato explains that the semiconductor circuit chip assemblies 81 are stacked at the lowermost stage, middle stage and uppermost stage in succession from the left. *Id.* at 20. A connector 101 is disposed in the semiconductor device 82, and the JTAG (Joint Test Action Group) tester is connected to the connector 101. *Id.* Similar to the signal lines TCK, the signal lines TMS, TRST and TDO2 are respectively connected to identical bus lines 102b, 102c and 102d and are mutually connected to the corresponding TMS pin 101b, TRST pin 101c and TDO2 pin 101d of the connector 101 in parallel. *Id.*

3. Sung (Ex. 1010)

Sung is titled "Method for Scalable Architectures in Stackable Three-Dimensional Integrated Circuits and Electronics." Ex. 1010, code (54). Sung relates to "design techniques or methods that enable scalable integrated circuit systems." *Id.* ¶ 40. Sung describes that "[n]ew developments in manufacturing process technology allow wafers to be vertically stacked and fine-grained vertical conductors formed between circuits on adjacent dies." *Id.* ¶ 3. Sung note that "[d]ie stacking has the potential to increase processing power, chip integration, operating speed and data storage density in the same planar area while minimizing global interconnect lengths," but "[a]s designs move to three dimensions, new design techniques are required to maximize performance while minimizing design effort." *Id.* ¶ 6.

Figure 3, reproduced below, shows a diagram of three stacked dies.

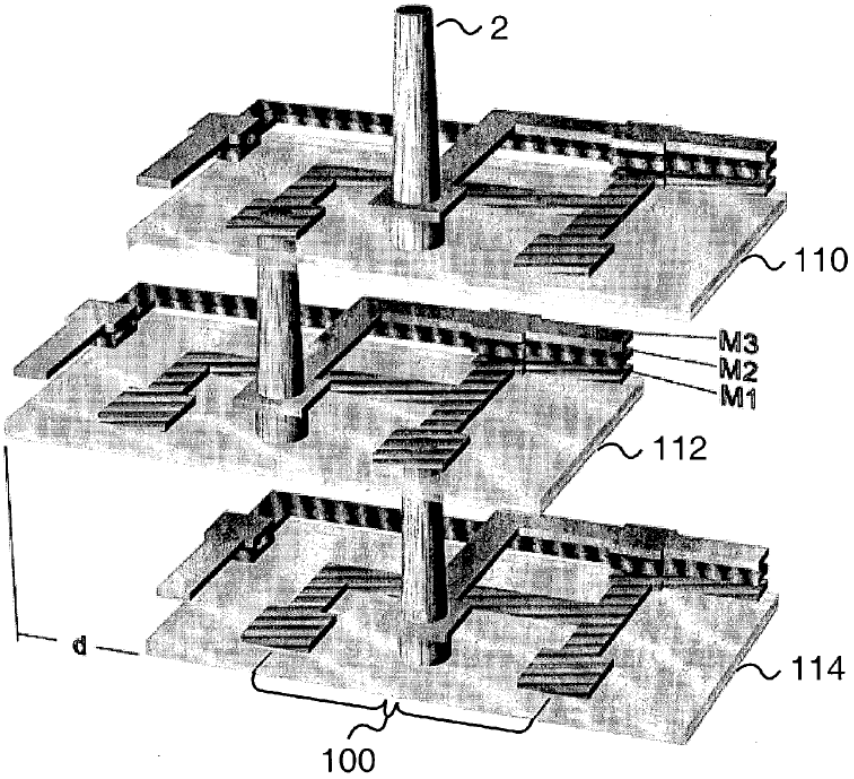


Figure 3 illustrates three stacked dies 110, 112, 114, aligned connectors 100, including vertical conductor 2 on middle die 112, which aligns with the left terminator 4 of the connector 100 on die 110 above it. *Id.* ¶ 44. Sung explains that "[c]ommunication between multiple dies can be accomplished by an inter-die network," where "[i]nter-die networks can be used to implement scan chains 290, inter-processor communication or pipelined computation where information is passed from latches or registers 294 on one level of the stack to latches or registers on another level of the stack." *Id.* ¶ 49.

4. Watanabe (Ex. 1011)

Watanabe is titled "Chip Mounting Substrate, First Level Assembly, and Second Level Assembly." Ex. 1011, code (54). Watanabe "relates to a semiconductor device packaging technology, more specifically to a chip mounting substrate, a first level assembly using the chip mounting substrate, and a second level assembly using the first level assembly." *Id.* at 1:16–20. Watanabe describes that the need for high density in semiconductor packaging has led to stacked semiconductors, but new packages are necessary. *Id.* at 1:42–55. To address this, Watanabe discloses:

> A first level assembly comprising: a mounting base defined by a first surface and a second surface opposite to the first surface; a plurality of first lands disposed on the first surface, being classified into first and second groups of the first lands; a plurality of second lands disposed on the second surface so as to face to the first lands, being classified into first and second groups of the second lands; a plurality of straight connection paths embedded in the mounting base so as to connect the first group of the first lands with the first group of the second lands just above the first group of the first lands; and a semiconductor chip mounted on a chip mounting area assigned adjacent to the second lands on the second surface.

Id. at 1:64–2:9.

Figure 1, reproduced below, is a perspective view showing an example of a first level assembly in Watanabe.

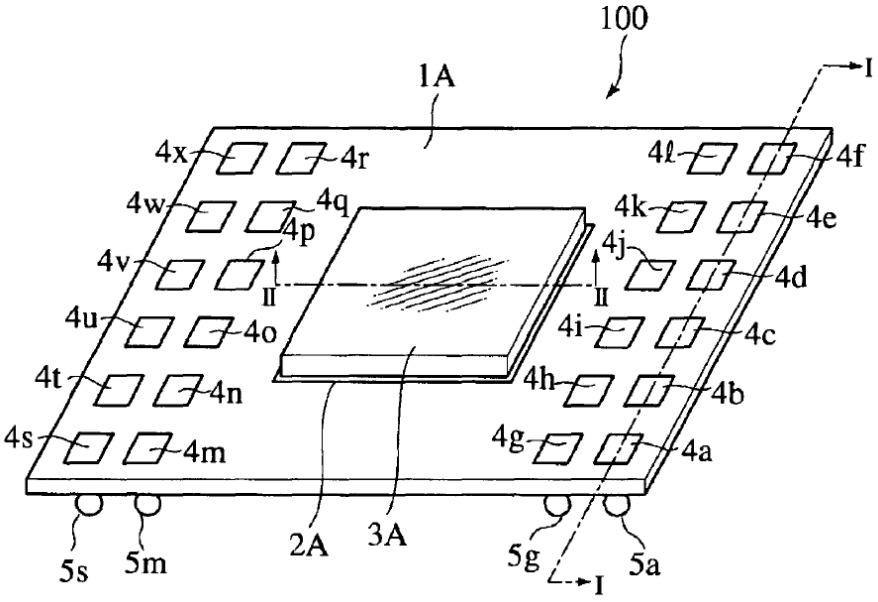


Figure 1 shows a mounting base 1A, second lands 4a, 4b, 4c, etc. on the top surface, joint balls 5a, 5b, 5c, etc., which are disposed on the first lands 7a, 7b, 7c, etc. (not shown), chip mounting area 2A, and semiconductor chip 3A. *Id.* at 3:40–62; 4:26–29. Figure 2, reproduced below, shows a side view of the assembly in Figure 1.

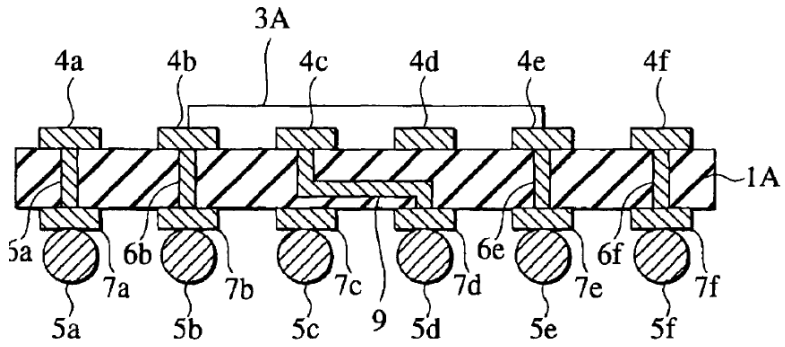


Figure 2 shows many of the features of Figure 1, and additionally shows which are opposite first lands 7a, 7b, 7c, etc., on the bottom surface, through-holes 6a, 6b, 6c, etc., and "bent through-hole 9 (bent connection

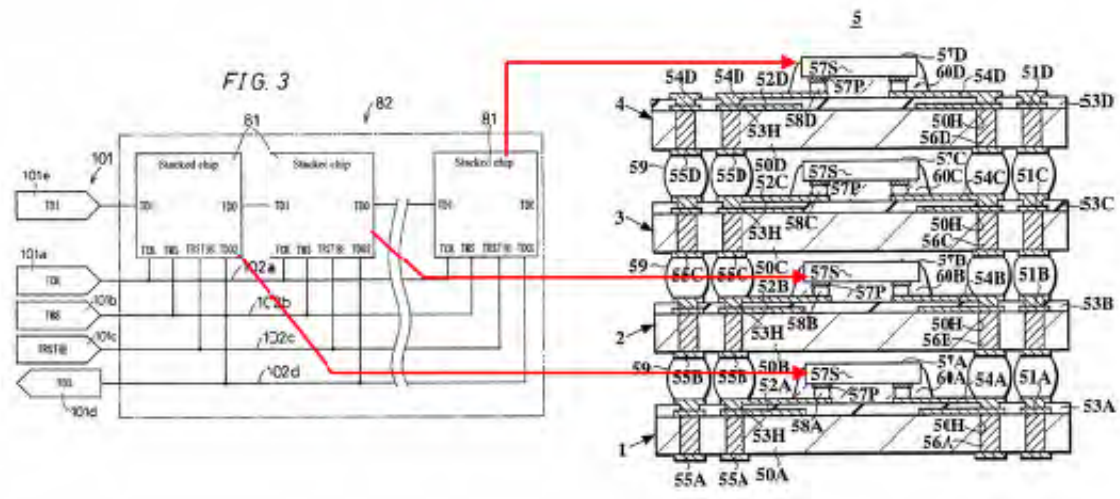
path), which has a stair-step shape and is embedded in the mounting base 1A." *Id.* at 4:29–35.

E. Asserted Obviousness Based on Hosomi and Sato

Petitioner contends that claims 1, 2, 11, and 12 would have been rendered obvious by the combination of Hosomi and Sato. Pet. 14–57. We discuss the evidence and the arguments provided by the parties with respect to independent claim 1 first. Petitioner provides a detailed claim analysis, supported by the testimony of Dr. Thompson. *See id.* at 14–54; Ex. 1003, 44–100. Patent Owner contests some of Petitioner's evidence and arguments with respect to claim 1, but does not provide any supporting testimony for its position. *See* Prelim. Resp. 12–28.

1. Rationale to Combine Hosomi and Sato

Petitioner contends that a person of ordinary skill in the art "would have been motivated to incorporate Sato's boundary scan controller into a chip in each module of Hosomi's stacked module (as illustrated below) and would have been motivated to implement Sato's daisy-chain connections using the package routing structures of Hosomi." Pet. 14 (citing Ex. 1003 ¶¶ 90–98). Petitioner illustrates this proposed combination using annotated versions of Sato's Figure 3 (below left) and Hosomi's Figure 5 (below right). Pet. 15.



Sato, Figure 3 (left); Hosomi, Figure 5 (right)

Petitioner's annotated versions of Sato's Figure 3, above at left, and Hosomi's Figure 5, above at right, show red lines between the two figures indicating incorporation of Sato's elements into Hosomi's stack. According to Petitioner, Sato's "boundary scan controller is incorporated into the chip in each module of Hosomi's stack—the rightmost controller is disposed in the top module's chip (57D), the leftmost controller is disposed in the bottom module's chip (57A), and a middle controller is disposed in the middle modules' chips (57B and 57C)." Pet. 14–15 (citing Ex. 1003 ¶ 90).

> Petitioner asserts that a person of ordinary skill in the art
>
> would have been motivated to implement Sato's daisy-chain connections (illustrated in Figure 5) in the combined system which stacks modules (each having a chip mounted on a substrate) using Hosomi's package routing structures including (1) implementing Sato's vertical electrodes using Hosomi's through-vias (*e.g.*, connection 56), Sato's terminals using Hosomi's electrodes 51 (pads), Sato's connection lines using Hosomi's wiring layers (*e.g.*, Figures 6A-6B), and (2) using Hosomi's pad and ball connections to connect adjacent modules. (*Id.*)

Pet. 15.

Petitioner argues that a person of ordinary skill in the art would have been motivated to make this combination for several reasons. "First," Petitioner argues, "Sato provides an express teaching that would have led a [person of ordinary skill in the art] to incorporate Sato's boundary scan controller and associated daisy-chain connection teachings into Hosomi's stacked module." Pet. 16 (citing Ex. 1003 ¶ 91; Ex. 1009, 8:2–8; *see also id.* at 8:26–27; 13:17–19).

"Second," Petitioner argues, a person of ordinary skill in the art "would have understood that testing was essential, if not required, for manufacturing vertically stacked modules such as those taught by Hosomi. Pet. 16 (citing Ex. 1003 ¶¶ 92–93). "For example," Petitioner argues, an "SDRAM module manufacturer would have been motivated to test the stack of modules to ensure each layer of memory is properly interconnected," and a person of ordinary skill in the art "would have been motivated to use boundary scan testing for this testing because boundary scan technology enables testing of connections between devices in a stack without external probes. Pet. 15–16 (citing Ex. 1013, 272 (explaining it is "more difficult to physically probe lines" and "[i]t is best to base" a test plan "on the use of chips with *boundary scan*")). Petitioner concludes that a person of ordinary skill in the art "would have therefore been motivated to combine Sato's boundary scan teachings into Hosomi to minimize the amount and complexity of equipment required for testing." Pet. 17 (citing Ex. 1003 ¶ 93, *citing* Ex. 1021, 1 ("[u]sing the JTAG/boundary-scan logic minimizes the amount and complexity of equipment for testing boards . . . JTAG/boundary-scan saves time and costs for your board test and programming systems")). Petitioner points out that "the '243 [patent] itself

acknowledged JTAG/boundary scan would be used to test the stacked modules or chips in this time frame." Pet. 17 (citing Ex. 1001, 10:32–33).

"Third," Petitioner argues, a person of ordinary skill in the art "would have been motivated to combine the boundary scan teachings of Sato with Hosomi because boundary scan technology was widely known and standardized before the '243 patent." Pet. 17 (citing Ex. 1003 ¶¶ 94–95). Petitioner points out that "Sato explicitly applies JTAG boundary scan testing standards, referring throughout to an external 'JTAG tester'" and that "[t]he IEEE JTAG boundary scan standard was adopted in 1990, 15 years before the '243 patent." Pet. 17 (citing Ex. 1009, 4:9–5:5, 14:6–18; Ex. 1003 ¶ 94).

"Fourth," Petitioner argues, "the combination of Hosomi and Sato is nothing more than the combination of prior art elements according to known methods to yield predictable results," and a person of ordinary skill in the art "would have combined the well-known elements of Hosomi and Sato using well-known methods." Pet. 18 (citing Ex. 1003 ¶¶ 96–97). Petitioner argues that "because testing is so critical for devices, it was not uncommon prior to the '243 patent that a device's test cost is comparable to its manufacturing cost, further confirming a [person of ordinary skill in the art] would have been motivated and understood how to include industry standard testing in Hosomi's modules." Pet. 18 (citing Ex. 1003 ¶ 96).

"Finally," Petitioner argues, a person of ordinary skill in the art "would have understood the combination of Hosomi and Sato merely amounts to applying known techniques to a known device ready for improvement to yield predictable results." Pet. 19 (citing Ex. 1003 ¶ 98). Petitioner argues that a person of ordinary skill in the art "would have

considered the combination improvement to Hosomi because chips manufactured with built-in terminals that support boundary scan have the capability to be tested for faulty interconnections at the same time and using the same test vectors." Pet. 19. According to Petitioner, a person of ordinary skill in the art "would have recognized Sato's known boundary scan technique would have yielded predictable results and would have resulted in an improved system free of interconnection faults." *Id.*

Patent Owner argues that "Petitioner's alleged reasons for the proposed combination of Sato and Hosomi . . . focus almost exclusively on the asserted reasons for incorporating Sato's boundary scanning test into Hosomi, with almost no mention for why [a person of ordinary skill in the art] would have been 'motivated to implement Sato's daisy-chain connections (illustrated in Figure 5) in the combined system which stacks modules (each having a chip mounted on a substrate) using Hosomi's package routing structures.'" *See* Prelim. Resp. 13. Patent Owner argues that Petitioner's "alleged reason to modify Sato's electrode structure is unsupported by any evidence other than a single conclusory statement of Dr. Thompson," and that this "statement does nothing more than mirror the conclusory assertions in the Petition and should be disregarded." *Id.* at 14 (citing Pet. 16; Ex. 1003 ¶ 91). Patent Owner argues that "[t]here is no evidence to conclude that Hosomi's package routing structure is low cost or reliable, and there is no evidence that these unsupported allegations would have served as a . . . motivation to modify Sato." Prelim. Resp. 14.

We disagree with Patent Owner. It is well established that a reason to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of

those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1355 (Fed. Cir. 1999) (citing *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)). Moreover, "any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418, 420 (2007). There is no requirement for Petitioner to articulate a separate rationale to combine every feature of the proposed combination of Hosomi and Sato, as Patent Owner's argument seems to imply.

Here, Petitioner articulates several reasons why a person of ordinary skill in the art would have combined Hosomi and Sato in the manner described by Petitioner, any one of which may be sufficient to support the proposed combination. Indeed, Petitioner even points out that the '243 patent discusses use of "the JTAG TDI-TDO signal." *See* Pet. 17 (citing Ex. 1001, 10:32–33). Petitioner's articulated rationale to combine is supported by the testimonial evidence of Dr. Thompson. *See* Ex. 1003 ¶¶ 90–98.

With regard to the rationale to combine Hosomi and Sato articulated by Petitioner, Petitioner's showing is supported by substantial, unrebutted testimony of Dr. Thompson (*see* Ex. 1003 ¶¶ 90–98). In contrast to Petitioner's supported showing of various rationales to combine Hosomi and Sato, Patent Owner relies on mere unsupported attorney argument and provides no testimonial evidence in support if its position. *See* Prelim. Resp. 12–15. As we have already mentioned, such unsupported attorney argument is entitled to little probative value. *See In re Geisler*, 116 F.3d 1465, 1470

(Fed. Cir. 1997); *In re De Blauwe*, 736 F.2d 699, 705 (Fed. Cir. 1984). The evidence at this stage favors Petitioner on the issue of rationale to combine.

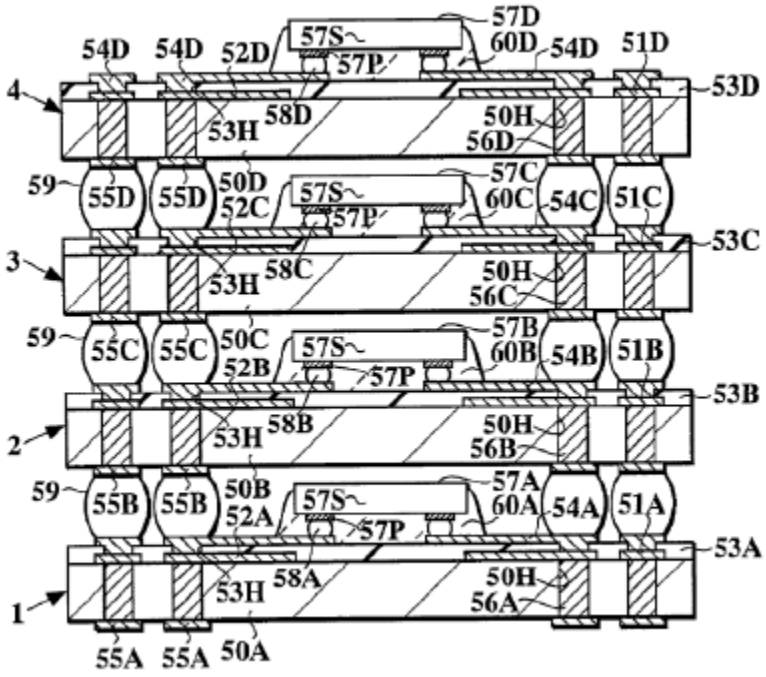
Based upon the current record, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that a person of ordinary skill in the art at the time of the invention would have had a reasoned basis for combining the teachings of Hosomi and Sato in the manner proffered and would have had a reasonable expectation of success in that endeavor.

2. Independent Claim 1

a) A stacked module comprising a plurality of modules each comprising:[3]

Petitioner contends that "Hosomi's semiconductor module 5, illustrated below, comprises a stack of semiconductor devices 1 to 4." Pet. 20 (citing Ex. 1007 ¶ 89). Petitioner explains that semiconductor devices 2 to 4 "are substantially identical" to semiconductor device 1 and are each "constituted by an SDRAM system." Pet. 20 (citing Ex. 1007 ¶¶ 89, 74). According to Petitioner, "semiconductor device[s] 1–4 are each a "*module*" of stacked semiconductor module 5 because each includes a chip connected to a substrate." Pet. 20 (citing Ex. 1003 ¶ 99). Hosomi's Figure 5 is shown below.

[3] Petitioner contends that the phrase "a plurality of modules each comprising" is not part of claim 1's preamble, but rather should be treated as a substantive limitation of claim 1. Pet. 6–7. Patent Owner disagrees. Prelim. Resp. 9–12. For purposes of this Decision and based on this preliminary record, we treat the contested phrase as part of the preamble. Because Petitioner has shown adequately that the prior art discloses or suggests the preamble, we need not determine whether it is limiting.



Hosomi's Figure 5, above, is a cross section of a semiconductor module in which a plurality of semiconductor devices 1–4 are stacked. Ex. 1007 ¶ 55. Semiconductor device 1 at the bottom includes package substrate 50A, semiconductor chip 57A mounted on the package substrate by the flip-chip structure, and protecting resin film 60A extending over semiconductor chip 57A in order to protect it against surroundings. *Id.* ¶ 95. Petitioner's arguments are supported by the testimony of Dr. Thompson. *See* Ex. 1003 ¶ 99.

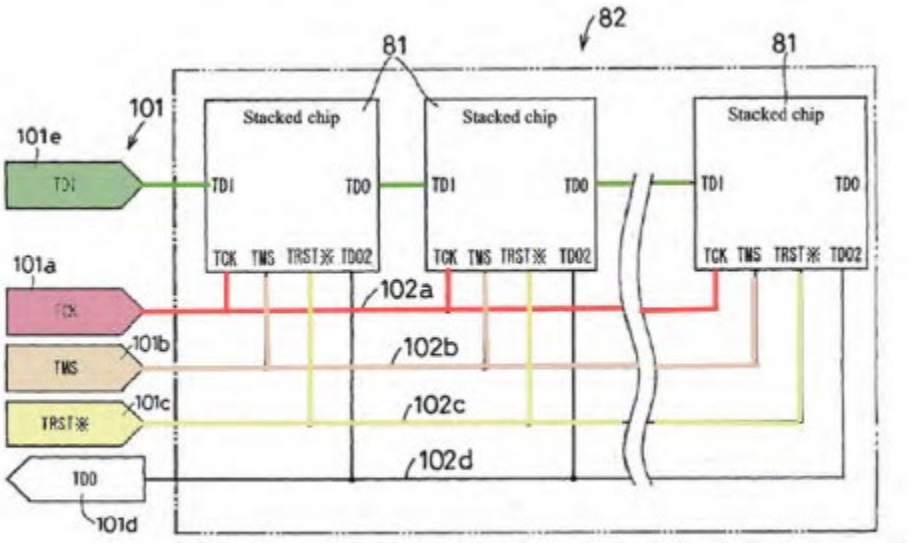
Patent Owner does not specifically contest Petitioner's evidence and arguments with respect to the preamble. *See* Prelim. Resp. 12–28.

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Hosomi's description of semiconductor module 5 comprising a stack of semiconductor devices 1 to 4 meets the recited "*stacked module comprising a plurality of modules*" of the preamble.

b) one or more active ports for carrying one or more active signal[s];

Petitioner contends that the combined teachings of Hosomi and Sato meet this limitation. Pet. 21 (citing Ex. 1003 ¶¶ 100–112). Petitioner asserts that "the '243 patent . . . uses the term 'port' broadly as either an entry to or exit from a module or circuit/chip on the module." Pet. 23 (citing Ex. 1003 ¶ 101). Petitioner also points out that "according to the '243 patent, an '*active signal*' encompasses a signal applied to the stack by an external source and distributed via an '*active port*' to circuitry on the module." *Id.*

According to Petitioner, "Sato discloses numerous '*active signals*' carrying information and used by a boundary scan controller including TDI (data input) and TCK (clock)." Pet. 23. To illustrate these active signals, Petitioner uses Sato's Figure 3, annotated by Petitioner, shown below.



Sato, Annotated Figure 3

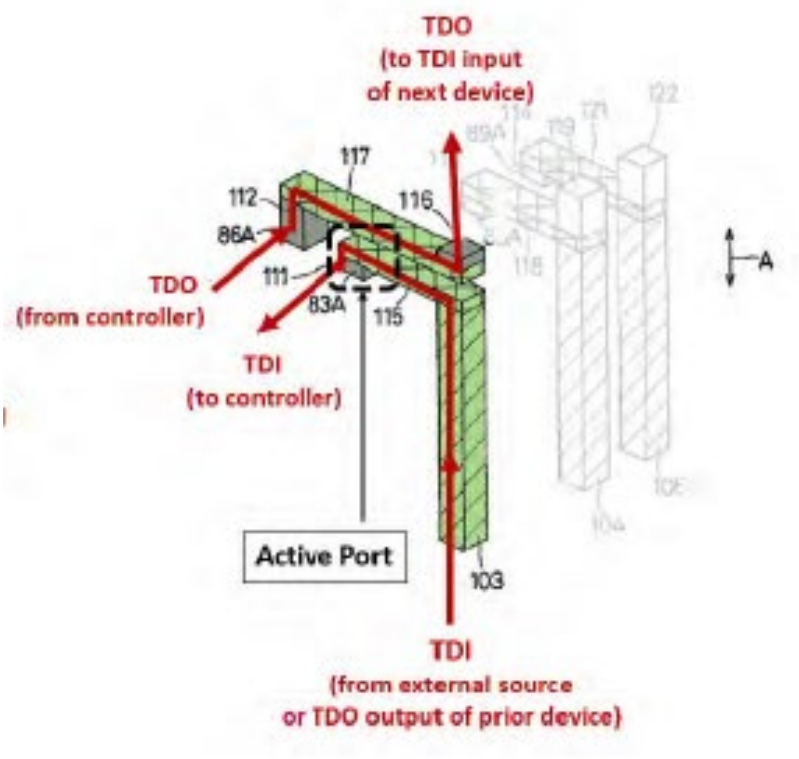
Sato's Figure 3, annotated by Petitioner shown above, is a block diagram illustrating semiconductor device 82, which is configured by

stacking a plurality of semiconductor circuit chip assemblies 81. Petitioner explains that

> [i]n the stacked module of the combination of Hosomi and Sato (having a boundary scan controller in each module and using Sato's daisy-chain connections), the TDI active signal (shaded green) is applied to the bottom controller (leftmost) by an external JTAG tester. ([Ex.] 1009, Figure 3 (below).) The TDO output of the bottom controller is connected to the TDI input of the controller in the next module in the stack. ([Ex.] 1009, 20:24-27.) The TDO output of that module is in turn connected to the TDI input of the next module and so on until the top controller (rightmost) is reached. The daisy-chain path propagates TDI through the stack. ([Ex.] 1003, ¶102.) Signal lines TCK (shaded red), TMS (shaded orange) and TRST (shaded yellow) are distributed through the stack to the controller in each module via identical bus lines 102a-c.

Pet. 23 (citing Ex. 1009, 20:20–23).

Petitioner also explains how a TDI active signal path moves through Sato's daisy-chain connection, as illustrated in Sato's Figure 5, annotated by Petitioner shown below. Pet. 25.



Sato's Figure 5, annotated by Petitioner shown above, is a perspective view illustrating part of the wiring pattern of semiconductor circuit chip assembly 81, which is formed by disposing controller 80 in the semiconductor circuit chip. Ex. 1009, 12. According to Petitioner, the TDI signal path passes through electrode 103 (shaded green) to terminal 111 via connection line 115 (shaded green). Pet. 24 (citing Ex. 1009, 23:26–27). Active TDI signal is then communicated from terminal 111 (shaded gray) to the TDI input of the boundary scan controller. Pet. 29 (citing Ex. 1009, Fig. 2; Ex. 1003 ¶ 104). Terminal 111 distributes TDI to the boundary scan controller and is therefore an "*active port*," in Petitioner's view. Pet. 29 (citing Ex. 1003 ¶¶ 104–105; Ex. 1005, 1).

Petitioner also explains how in its combination of Hosomi and Sato, Sato's Figure 5 daisy-chain connection is integrated into the substrate of each stacked SDRAM semiconductor device of Hosomi. Pet. 25–26.

Petitioner explains how "the daisy-chain connection is implemented using Hosomi's vias as Sato's vertical electrodes, Hosomi's pads as Sato's terminals, Hosomi's wiring layers for Sato's connections, and the modules are connected using the pad/ball connections taught by Hosomi." *Id.* at 25 (citing *id.* at Pet. § V.A.3; Ex. 1009, 23:5–25:10). In this combination, Petitioner asserts that "[t]he pad/ball receiving the TDI signal at the bottom module is an '*active port*' because it receives TDI from an external source." Pet. 26 (citing Ex. 1003 ¶¶ 107–108).

Petitioner's arguments are supported by the testimony of Dr. Thompson. *See* Ex. 1003 ¶¶ 100–112.

Patent Owner does not specifically contest Petitioner's evidence and arguments with respect to this limitation. *See* Prelim. Resp. 12–28.

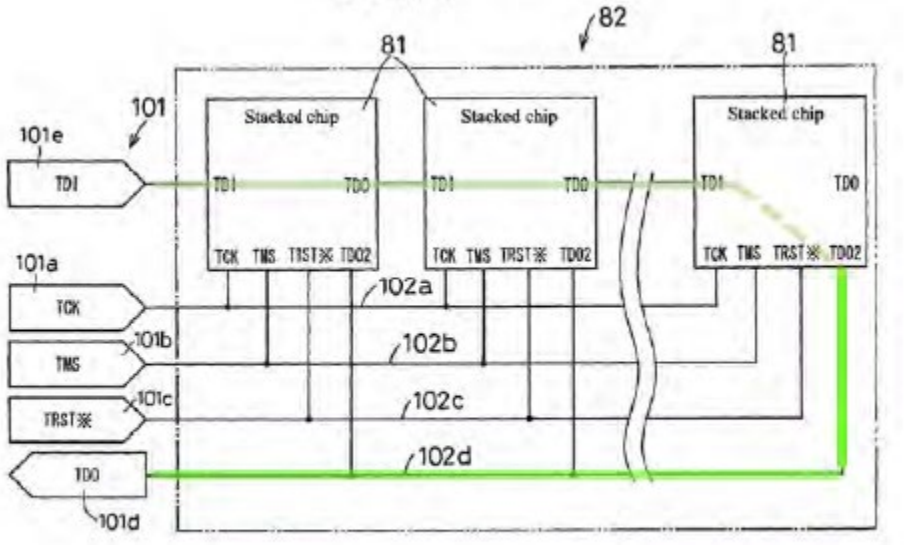
On this preliminary record, we find that Petitioner has shown sufficiently for purposes of institution that the combined teachings of Hosomi and Sato meet the recited limitation "*one or more active ports for carrying one or more active signal[s]*" of claim 1.

> *c) one or more passive ports for passing through the one or more active signals;*

Petitioner contends that the combined teachings of Hosomi and Sato disclose multiple "*passive ports*" and provide evidence and arguments directed to two different constructions.[4] Pet. 30–33. Petitioner explains that in its proposed combination, each module in Hosomi's stack is an SDRAM module and Sato's TDO2 signal "is an "*active signal*" because it carries the

[4] The parties appear to contest the meaning of "passive port" and support different constructions. We declined to adopt an express construction on this preliminary record and at this stage of the proceeding. *See* Section III.C above.

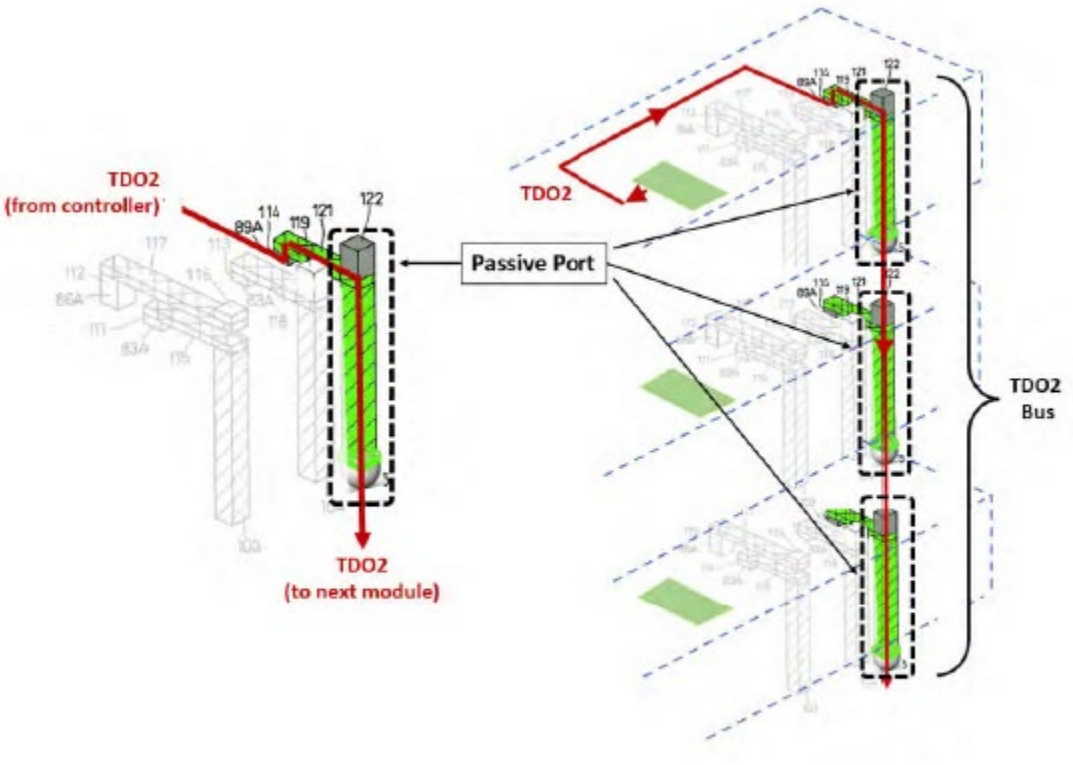
output data of a boundary scan of the stacked module. Pet. 30 (citing Ex. 1003 ¶ 114). Petitioner's annotation of Sato's Figure 3 is shown below. Pet. 31.



Sato, Annotated Figure 3

According to Petitioner, the controller in the top SDRAM module in the stacked module of Hosomi and Sato outputs TDO2 (shaded neon green) to bus 102d ("TDO2 bus") which passes TDO2 through the stack to the external JTAG tester. *Id.* at 30. Petitioner asserts that "the TDO2 bus is a path through the stack and includes a set of interconnected "*passive ports*". *Id.* at 31 (citing Ex. 1003 ¶ 115).

Petitioner also explains how TDO2 moves through passive ports in Sato's daisy-chain path. Petitioner's annotation of Sato's Figure 5 is shown below on the left, next to Thompson's Figure C below on the right.



Sato, Annotated Figure 5, Top Device (left)
Thompson, Figure C: Stacked Module of Hosomi and Sato—TDO2 (right)

Sato's Figure 5, annotated by Petitioner shown above left, is a perspective view illustrating part of the wiring pattern of semiconductor circuit chip assembly 81. Ex. 1009 12. Thompson's Figure C, above right, illustrates the stacked module configuration of Petitioner's combination of Hosomi and Sato. As illustrated in Petitioner's annotation of Sato's Figure 5, above left, TDO2 is output from the controller and transmitted to terminal 114 and then terminal 122 through connection line 121. Pet. 31 (citing Ex. 1009, 24:10–11; Ex. 1003 ¶ 115). The path from terminal 122 in the top module through the stack to the external JTAG tester is the TDO2 bus.

In the "stacked module" combination of Hosomi and Sato illustrated in Thompson Figure C above right, TDO2 passes from terminal (pad) 122, through electrode (via) 105, to the pad/ball structure at the bottom of the

module which is connected to terminal (pad) 122 of the next module in the stack. Pet. 31 (citing Ex. 1003 ¶ 115). Each module in the stack includes the TDO2 portion of the daisy-chain connection. Pet. 32 (citing Ex. 1003 ¶ 116). According to Petitioner, "[t]his structure is a '*passive port*' under both constructions because it passes the active TDO2 from a terminal (pad) to a ball on the opposite side of an SDRAM module and subsequently a pad in the adjacent module in the stack or to a pad carrying TDO 2 to an external JTAG tester. Pet. 32 (citing Ex. 1003 ¶ 116).

Patent Owner contests Petitioner's evidence, arguing that Petitioner's proposed combination of Hosomi and Sato does not result in the claimed "*passive port*" using Petitioner's proposed construction, because "the vertical electrode through the module connects to a wire 115, and pad 116 is arranged on a different layer above the module, insulated from wire 115." Prelim. Resp. 16 (referencing Thompson Figure A: Hosomi and Sato – Stacked Module). "Thus," Patent Owner argues, "under Petitioner's proposed construction of 'passive port,' the Hosomi-Sato stacked module's TDI-TDO signal path leading to the top module does not disclose or suggest a 'passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module' and does not disclose a '*passive port*' under Petitioner's construction." Prelim. Resp. 16–17.

Patent Owner also argues that Petitioner's identification of TDO2 as an "*active signal*" is also deficient because it is "directly inconsistent with Petitioner's prior interpretation of 'active signal,' which addresses only signals applied *to* circuitry on a module, not any signals output from circuitry." *Id.* at 18. Patent Owner asserts that "Petitioner never contends that the signal on signal line TDO2 is an active signal. Specifically,

Petitioner never asserts that an output of the boundary scan controller onto signal line TDO2 is also an 'active signal.'" *Id.*

We disagree with Patent Owner. First, Patent Owner does not respond directly to Petitioner's evidence. For example, Petitioner identifies "*passive ports*" in the stacked module combination illustrated in Dr. Thompson's Figure C, where "TDO2 passes from terminal (pad) 122, through electrode (via) 105, to the pad/ball structure at the bottom of the module which is connected to terminal (pad) 122 of the next module in the stack." *See* Pet. 31–32 (citing Ex. 1003 ¶ 116). In its argument, however, Patent Owner references Dr. Thompson's Figure A, which Dr. Thompson uses to identify "*active ports*" in the stacked module. Patent Owner argues that "the vertical electrode through the module connects to a wire 115, and pad 116 is arranged on a different layer above the module, insulated from wire 115," not addressing directly the particular structures and pathway identified by Dr. Thompson as a "*passive port*." *See* Prelim. Resp. 15–16.

Second, Patent Owner has not provided any declaration testimony to support its assertions. As a result, Patent Owner's assertions are founded principally on unsupported attorney argument, which has little probative value. The testimony of Dr. Thompson on this issue presently stands unrebutted. *See Icon Health & Fitness, Inc. v. Strava Inc.*, 849 F.3d 1034, 1046 (Fed. Cir. 2017) ("Attorney argument is not evidence or explanation in support of a conclusion."); *Invitrogen Corp. v. Clontech Lab., Inc.*, 429 F.3d 1052, 1068 (Fed. Cir. 2005) ("Unsubstantiated attorney argument regarding the meaning of technical evidence is no substitute for competent, substantiated expert testimony."); *In re Geisler*, 116 F.3d at 1470.

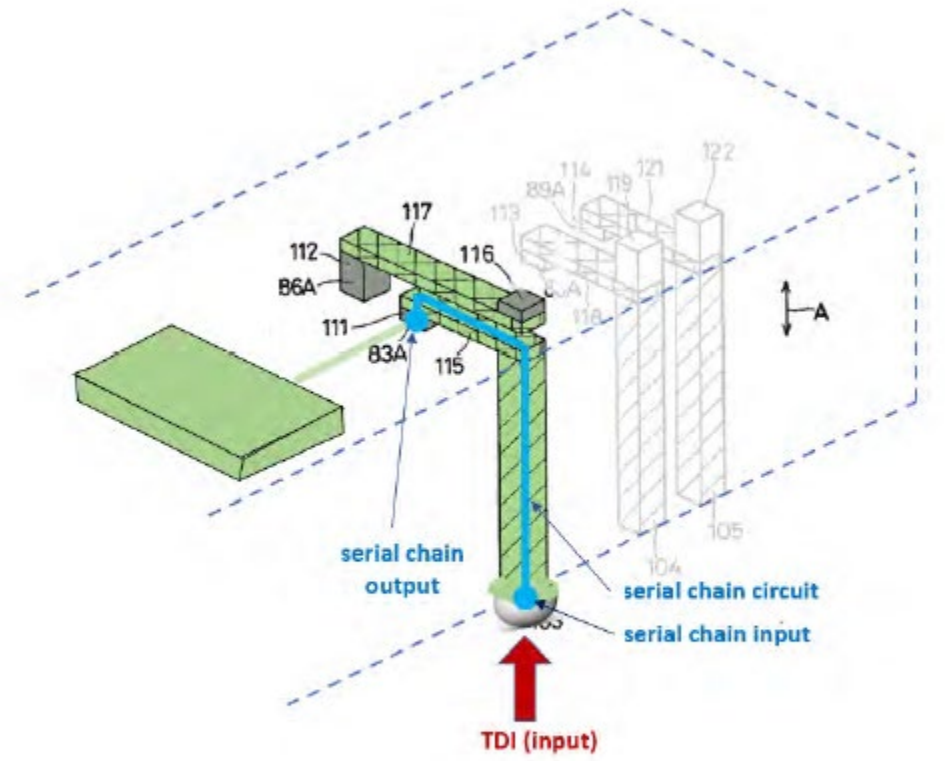
Third, Patent Owner argues that "Petitioner never contends that the signal on signal line TDO2 is an active signal" and "Petitioner never asserts that an output of the boundary scan controller onto signal line TDO2 is also an 'active signal.'" Prelim. Resp. 18. Yet, Petitioner clearly states that "TDO2 is an '*active signal'* because it carries the output data of a boundary scan of the stacked module." Pet. 30 (citing Ex. 1003 ¶ 114).

On this preliminary record, we find that Petitioner has shown sufficiently for purposes of institution that the combined teachings of Hosomi and Sato meet the recited limitation "*one or more passive ports for passing through the one or more active signals*" of claim 1.

> *d) a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;*

Petitioner contends that the combined teachings of Hosomi and Sato meet this limitation. Petitioner asserts that in the daisy-chain boundary scan signal path of its Hosomi/Sato combination, "the test data is input to the TDI signal line of the bottom controller (leftmost device) from an external source." Pet. 33. Petitioner explains that "TDI travels up the stack, passed from TDO output of one controller to TDI input of the next, until the top controller is reached." *Id.* (citing Ex. 1009, 20:24–27; Fig. 3). According to Petitioner, "[t]his path from the TDI input of the controller in the bottom module to the TDI input of the controller in the top module includes multiple '*serial chain connections.*'" Pet. 33 (citing Ex. 1003 ¶¶ 119–125). Petitioner asserts that "[t]he daisy-chain path includes at least two '*serial chain connection[s]*' in each stacked module—a vertical connection and two horizontal connections." Pet. 34 (citing Ex. 1003 ¶¶ 120–125).

Petitioner illustrates a vertical serial chain connection with Dr. Thompson's Figure D: Sato's Daisy Chain on Module Substrate, shown below.

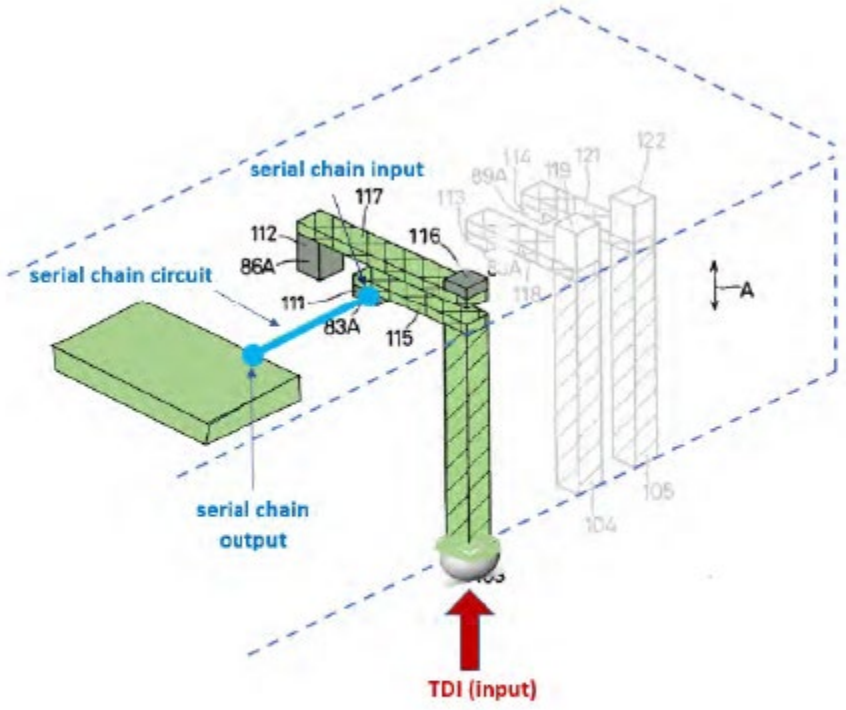


Thompson, Figure D: Sato's Daisy Chain on Module Substrate

Petitioner explains that in Figure D, above, "TDI is applied to the pad/ball at the bottom of the module and passes through electrode (via) 103 and connection line 115 to terminal (pad) 111." Pet. 34 (citing Ex. 1009, 23:26–27). "In the bottom module of the stack," Petitioner explains, "TDI is applied from an external JTAG tester." Pet. 34 (citing Ex. 1009, Fig. 3). "In other modules in the stack," Petitioner points out, "TDI is the TDO output of the preceding module. Pet. 34–35 (citing Ex. 1009, 20:24–27; Ex. 1003 ¶ 121). Petitioner asserts that "[t]he pad-via-ball structure in each module is a vertical '*serial chain connection*' with the ball on the lower surface of the

module receiving TDI being a '*serial chain input*,' electrode (via) 103 being a '*serial chain circuit*,' and terminal (pad) 111 on the upper surface that provides TDI to the controller being a '*serial chain output*.'" Pet. 35 (citing Ex. 1003 ¶¶ 121–122; Ex. 1005, 2).

Petitioner also provides an example of a horizontal serial chain connection using Dr. Thompson's Figure E, shown below.

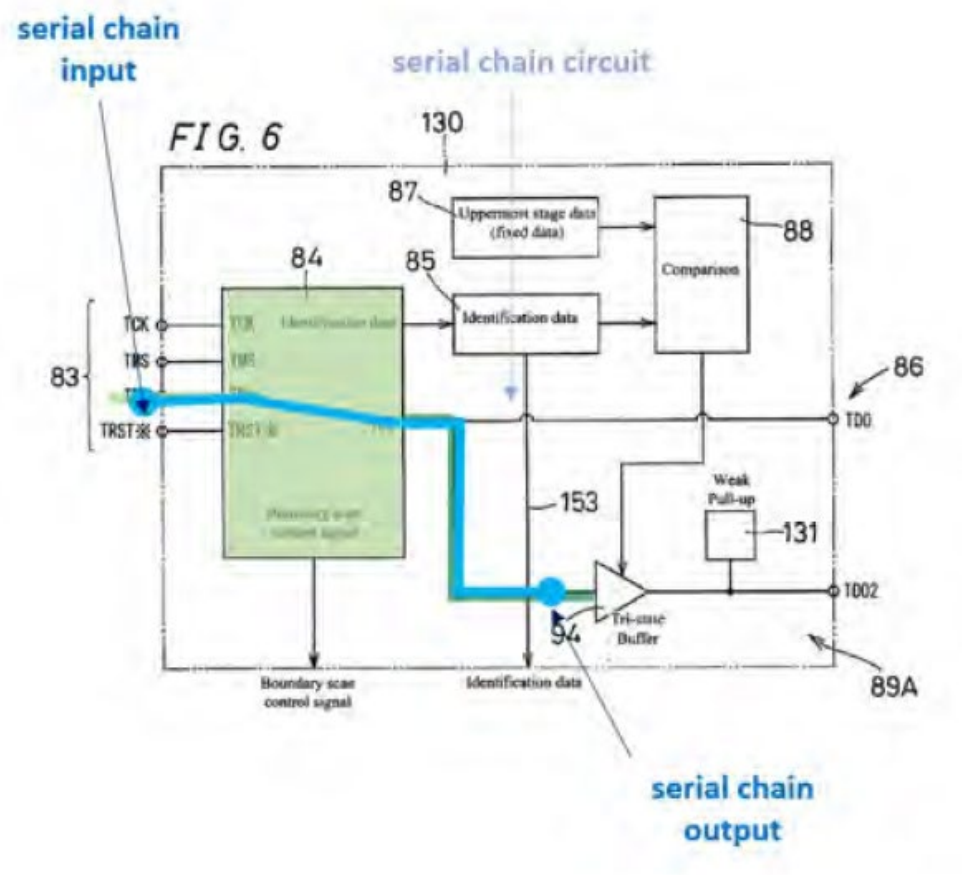


Thompson, Figure E: Horizontal "*Serial Chain Connection*" Terminal (Pad) 111 to Controller

> With respect to Figure E, above, Petitioner explains that
>
> terminal (pad) 111 is connected to the input of the boundary scan controller (shaded green) via a connection line. This horizontal path . . . is a "*serial chain connection*" with terminal (pad) 111 being the "*serial chain input*", the connection line being the "*serial chain circuit*" and the boundary scan controller's input being the "*serial chain output*."

Pet. 36 (citing Ex. 1003 ¶ 123).

Petitioner also asserts that a horizontal "*serial chain connection*" exists inside the boundary scan controller. Petitioner illustrates this connection using an annotated version of Sato's Figure 6, shown below. Pet. 38.



Sato, Annotated Figure 6—Top Module

Referring to Petitioner's annotated version of Sato's Figure 6, above, Petitioner explains that

> test data input on signal line TDI are output from signal line TDO through shift registers in control means 84. *See* [Ex.] 1009, 15:4-7. When the pre-configured identification data for a module matches identification data received during operation, a tristate buffer in the controller outputs TDO on signal line TDO2. *See* [Ex.] 1009, 19:21-23. During a boundary scan, a match condition occurs in the top module. [Ex.] 1003 ¶ 124. Thus, in the top

> module as shown in Figure 6 (below), the horizontal path from the controller's TDI input to the buffer input is a "*serial chain connection*" with the controller's TDI input being the "*serial chain input*", the connection through the register of the control means to tri-state buffer's input being the "*serial chain circuit*" and the tri-state buffer input's being the "*serial chain output*."

Pet. 37.

Petitioner further explains that

> [d]uring a boundary scan, a mismatch condition occurs in each controller beneath the top module in the stack. [Ex.] 1003 ¶ 125. Therefore, in these modules, no data is output on signal line TDO2 and signal line TDO outputs the data input on signal line TDI. (*Id.*) In these modules, the horizontal path from the controller's TDI input to the controller's TDO output is a "*serial chain connection*" with the controller's TDI input the "*serial chain input*", the connection through the register of the control means to the TDO output being the "*serial chain circuit*" and the TDO output being the "*serial chain output*." (*Id.*)

Pet. 38–39.

Patent Owner contends that "whether looking at an individual module or a stack of modules, Petitioner has no basis to contend that Hosomi in view of Sato discloses any 'first serial chain route,' as claimed." Prelim. Resp. 19. Patent Owner asserts that when "applying the '243 Patent's definition of a 'serial chain route' . . . a 'first serial chain route' of claim 1 *must have at least 'two serial chain connections* connected in series.'" Prelim. Resp. 21 (emphasis added). Patent Owner's assertion, however, appears inconsistent with the express language of claim 1, which recites "a first serial chain route that includes *at least one serial chain connection*." Ex. 1001, 10:48–49 (emphasis added). Patent Owner does not explain why we should ignore the express language of claim 1, and instead incorporate limitations from the specification into the claim. *See SuperGuide Corp. v.*

DirecTV Enters., Inc., 358 F.3d 870, 875 (Fed. Cir. 2004) ("Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim.").

Patent Owner also argues that

> Petitioner fails to establish that a TDI signal line and TDO signal line are "connected in series" where the lines are not directly connected. Instead, the signal path on each module is interrupted by circuitry and discontinuous, and Petitioner therefore fails to establish any two serial chain circuits coupling a ball and a pad "connected in series" sufficient to establish a "first serial chain route" as claimed.

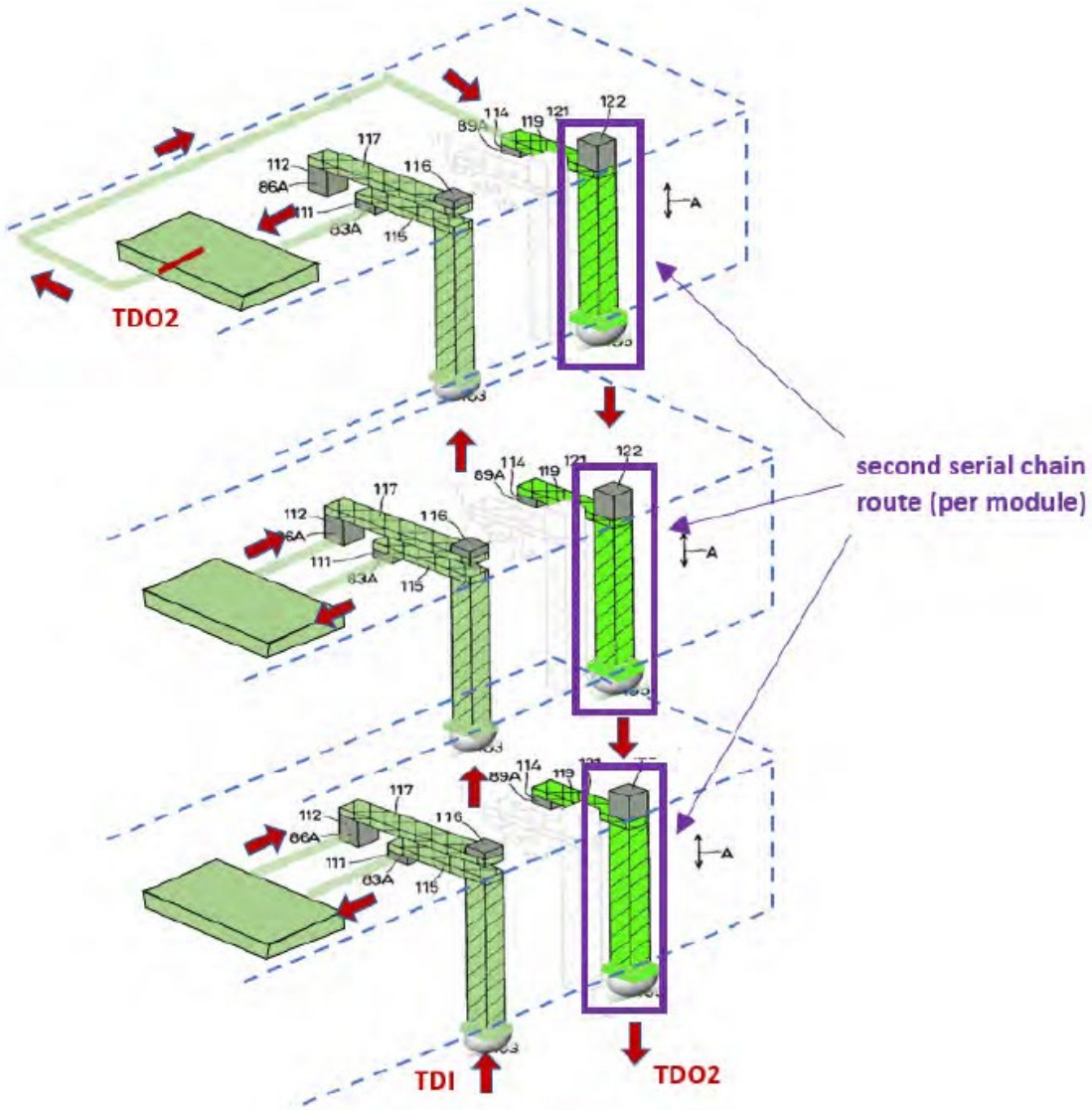
Prelim. Resp. 22. Patent Owner, however, does not explain how claim 1 requires a signal line "where the lines are . . . directly connected," or otherwise requires a "signal path on each module [that] is [not] interrupted by circuitry and discontinuous."

On this preliminary record, we find that Petitioner has shown sufficiently for purposes of institution that the combined teachings of Hosomi and Sato meet the recited limitation "*a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit*" of claim 1.

> *e) a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain*

route with the second serial chain route within an end module; and

Petitioner contends that the combined teachings of Hosomi and Sato meet this limitation. Petitioner illustrates a second serial chain route by referring to Dr. Thompson's Figure H, shown below. Pet. 44–45.



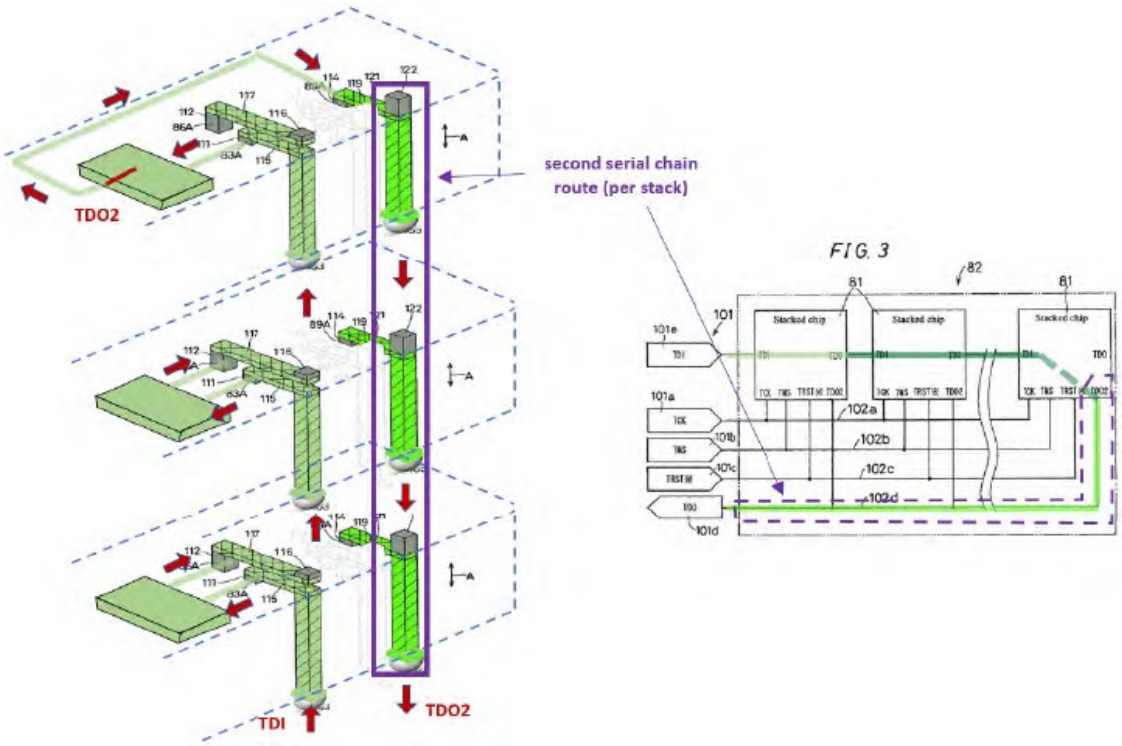
Thompson, Figure H: Petitioner's Construction

Figure H, above, depicts a second serial chain route through the TDO2 portion of the daisy chain connections in a combined stacked module. Pet. 44–45. With respect to Figure H, above, Petitioner explains that

> in each module, the TDO2 signal passes through terminal (pad) 122, electrode (via) 105, and connecting pad/ball to either an adjacent module or the external tester. The pad-via-ball structure in each module in the combination of Hosomi and Sato is a "serial chain connection" and each device therefore has a "second serial chain route" as required by Petitioner's "plurality of modules" construction.

Pet. 44 (citing Ex. 1003 ¶ 132).

Petitioner also provides an alternative example of a second serial chain route, using Dr. Thompson's Figure I (below left) and an annotated version of Sato Figure 3 (below right). Pet. 45–56.



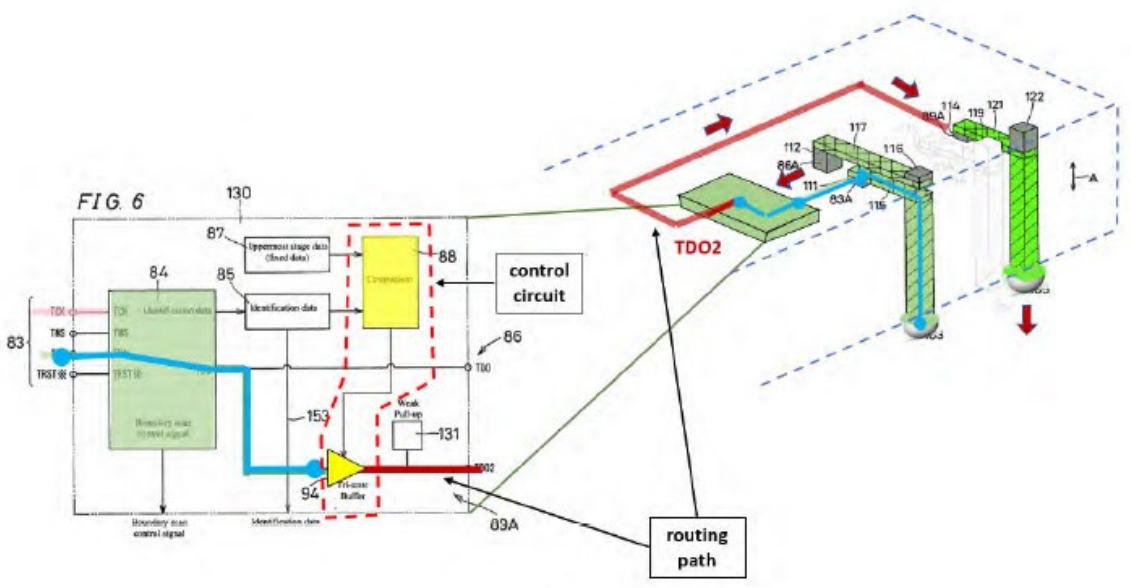
Thompson, Figure I (left): PO's Construction (left)
Sato, Annotated Figure 3 (right)

Figure I, above left, illustrates the TDO2 portion of the daisy-chain connections in a combined stacked module and Petitioner's annotated version of Sato's Figure 3, above right, shows the TDO2 signal line connected to bus 102(d). Ex. 1003 ¶ 133. With respect to these figures, Petitioner explains that

> [t]he "*stacked module*" includes a path for carrying TDO2 down the stack to the external tester consisting of multiple "*serial chain connections*" (pad-via-ball structures) as shown [above] in Thompson Figure I. Thus, the combination of Hosomi and Sato discloses "*a second serial chain route*" under [Patent Owner's] construction requiring a single "route" for the entire stack.

Pet. 45–46 (citing Ex. 1003 ¶ 133).

Petitioner illustrates the recited "*control circuit for enabling a routing path*" with reference to its annotated versions of Sato's Figures 5 and 6, shown below. Pet. 46–47 (citing Ex. 1003 ¶ 135).



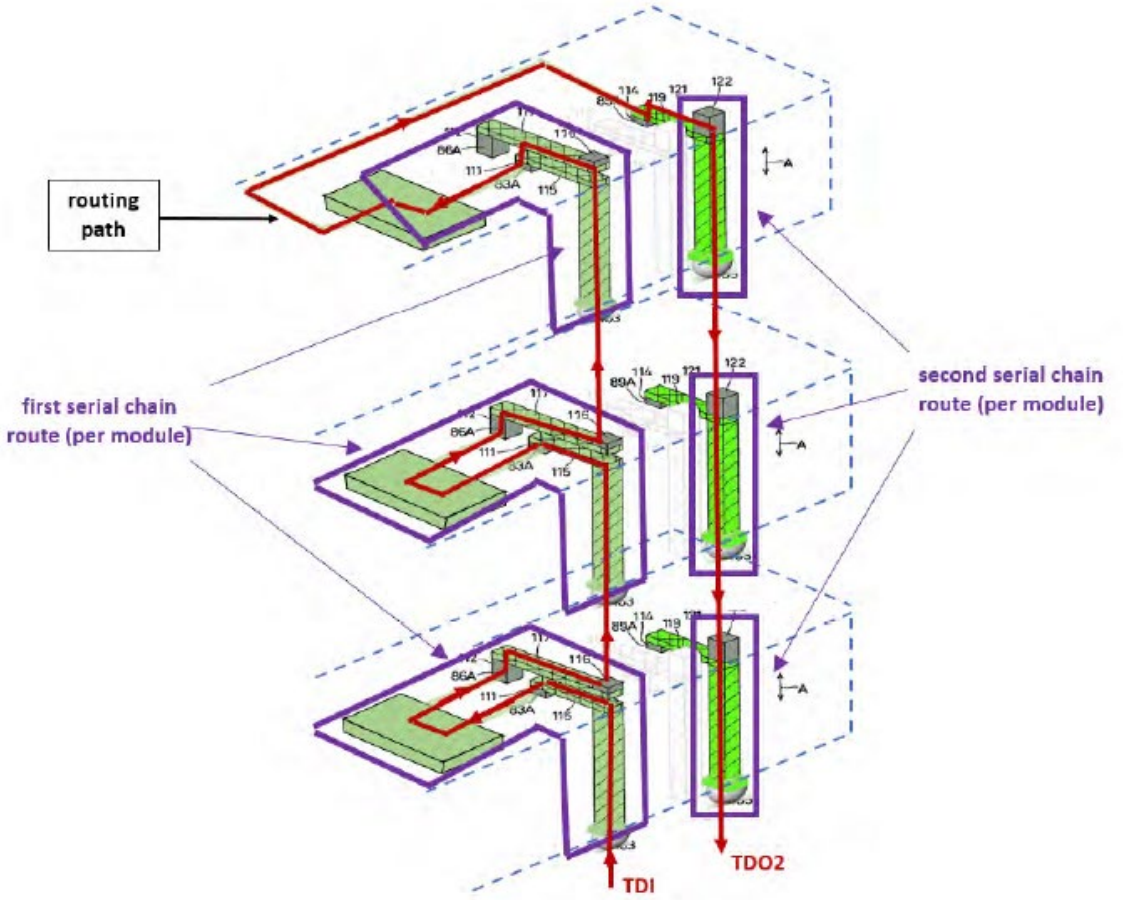
Sato, Annotated Figure 6 (top module); Annotated Figure 5

Sato's annotated Figure 6 on the left is a block diagram illustrating boundary scan controller 130, and Sato's annotated Figure 5 on the right is a perspective view illustrating part of the wiring pattern of semiconductor circuit chip assembly 82. Pet. 46–47; Ex. 1009, 12. Referring to Sato's annotated Figure 6, above left, Petitioner explains that "[t]he data derivation part 89A of each boundary scan controller includes tristate buffer 94, pull-up means 131 and signal line TDO2. Pet. 46–47 (citing Ex. 1009, 25:19–20). Petitioner asserts that "[c]omparison means 88 and tristate buffer 94 (shaded yellow) are part of "*a control circuit*" because they coordinate to control whether data is output on signal line TDO2." Pet. 47 (citing Ex. 1003 ¶¶ 135–139). Petitioner explains that "comparison means 88 compares the received identification data with preconfigured identification data and outputs a result which is used as the control input of tristate buffer 94." Pet. 47 (citing Ex. 1009, 16:12–15).

According to Petitioner, "[d]uring a boundary scan, a match occurs only in the top module (the 'boundary' of the stack)," and "[t]herefore, in the top module (an '*end module*' for the stack), the comparison result (match condition) turns on the tristate buffer causing the output of control means 84 (TDO) to be output on signal line TDO2." Pet. 47–48 (citing Ex. 1003 ¶ 137; Ex. 1009, 19:21–23). Petitioner asserts that "[t]he path from the tristate buffer output to terminal 122 (shaded red above) is a '*routing path*' for boundary scan data from the controller to the TDO2 bus. Pet. 48 (citing Ex. 1003 ¶ 137).

Petitioner uses Dr. Thompson's Figure J, shown below, to illustrate the "*control circuit . . . connects the first serial chain route with the second*

serial chain route within an end module." Pet. 49–50 (citing Ex. 1003, ¶¶140–144).



Thompson, Figure J: Petitioner's Construction

Figure J, above, illustrates the coupling of the first serial chain route and the second serial chain route through the daisy-chain connections of a combined stacked module. Pet. 49–50. With respect to Figure J, above, Petitioner explains that "a match condition in the top module during a boundary scan turns on the tri-state buffer . . . which causes the '*first serial route connection*' in the top module to be coupled to the '*second serial route connection*' in the top module. Pet. 49 (citing Ex. 1003 ¶ 141). This condition, Petitioner argues, shows that "the combination of Hosomi and

Sato discloses '*a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module*." Pet. 49.[5]

Petitioner's arguments are supported by the testimony of Dr. Thompson. *See* Ex. 1003 ¶¶ 129–142.

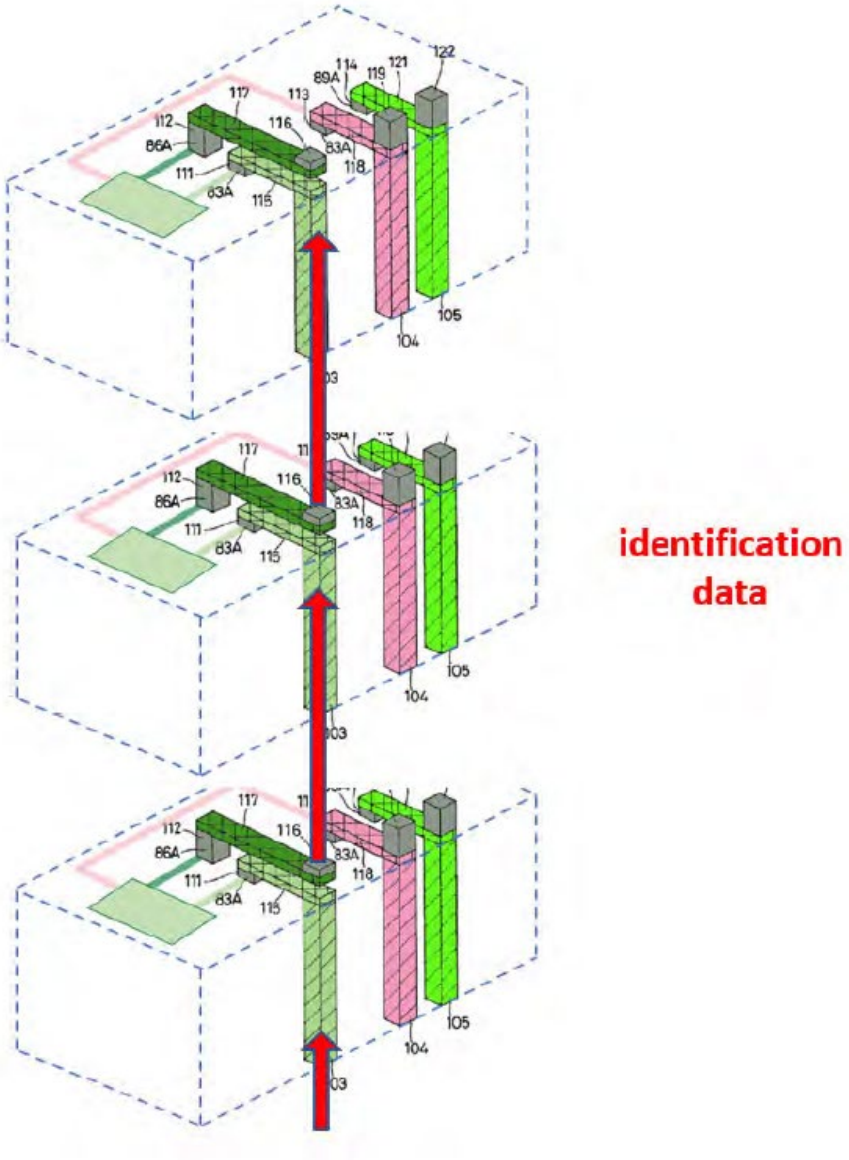
Patent Owner does not specifically contest Petitioner's evidence and arguments with respect to this limitation. *See* Prelim. Resp. 12–28.

On this preliminary record, we find that Petitioner has shown sufficiently for purposes of institution that the combined teachings of Hosomi and Sato meet the recited limitation "*a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module*" of claim 1.

> *f) said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.*

Petitioner contends that the combined teachings of Hosomi and Sato meet this limitation. To illustrate this limitation, Petitioner refers to Dr. Thompson's Figure L, shown below. Pet. 51–54.

[5] Petitioner also provides an alternative showing for this limitation using a construction "requiring a single first and second serial route for the entire stack." *See* Pet. 50–51 (citing Ex. 1003 ¶ 142).



Thompson, Figure L

Figure L, above, illustrates identification data being routed up to the top module through the other modules in a stack. Pet. 96–97. With respect to Figure L, Petitioner explains that "[t]he comparison means, which controls the tristate buffer and is part of the '*control circuit*,' uses identification data input via signal line TDI." Pet. 51 (citing Ex. 1009, 14:9–10) ("The signal line TDI is a signal line which serially inputs the

identification data."). "This identification data," Petitioner asserts, "is a '*control input signal*' to the '*control circuit*' because it determines whether the routing path from TDO to TDO2 is enabled in a module." Pet. 51–52 (citing Ex. 1003 ¶ 143). Petitioner explains that "identification data are routed up to the top module through the other modules (each of which comprise '*another module*') in the stack via the daisy-chain path of TDI signal lines . . . [t]hus, the '*control input signal*' is '*received from another module.*'" Pet. 52 (citing Ex. 1003 ¶¶ 143–144).

Patent Owner disagrees, arguing that

> the only signal that determines whether there is an output on TDO2 via tristate buffer 94 is the output of comparison means 88. The output of comparison means is not "received from another module from the plurality of modules," as required by claim 1. Instead, comparison means 88 "makes a comparison as to whether the identification data and the fixed data are matching, and outputs comparison result information." Ex. 1009, 16:12-18. No "control input signal" is received from "another module" "to enable the routing path."

Prelim. Resp. 23.

We disagree with Patent Owner. Patent Owner does not specifically address Petitioner's explanation that the comparison means "uses identification data input via signal line TDI," and that "[t]his identification data . . . is a '*control input signal*.'" *See* Pet. 51–52. Petitioner further explains that the "identification data are routed up to the top module through the other modules (each of which comprise '*another module*') in the stack via the daisy-chain path of TDI signal lines . . . [t]hus, the '*control input signal*' is '*received from another module.*'" Pet. 52.

Patent Owner instead argues that "the only signal that determines whether there is an output on TDO2 via tristate buffer 94 *is the output of*

comparison means 88. The output of comparison means is not 'received from another module from the plurality of modules,' as required by claim 1." Prelim. Resp. 23 (emphasis added). Patent Owner's argument, however, does not specifically address Petitioner's assertion that the recited "*control input signal*" is met by the "identification data input via signal line TDI" in Petitioner's combination of Hosomi and Sato.

Moreover, Patent Owner's assertions are founded principally on unsupported attorney argument, which, as we noted earlier, has little probative value. In contrast, Petitioner's showing with respect to this limitation is supported by the testimony of Dr. Thompson, which presently stands unrebutted. *See* Ex. 1003 ¶¶ 143–144. *See Icon Health & Fitness,* 849 F.3d at 1046 ("Attorney argument is not evidence or explanation in support of a conclusion."); *Invitrogen Corp.* 429 F.3d at 1068 ("Unsubstantiated attorney argument regarding the meaning of technical evidence is no substitute for competent, substantiated expert testimony."); *In re Geisler*, 116 F.3d at 1470.

On this preliminary record, we find that Petitioner has shown sufficiently for purposes of institution that the combined teachings of Hosomi and Sato meet the recited limitation "*said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module*" of claim 1.

3. Conclusion as to Independent Claim 1

We have considered Petitioner's evidence and arguments that the limitations of claim 1 are met by the combined teachings of Hosomi and Sato, as well as Patent Owner's evidence and arguments to the contrary.

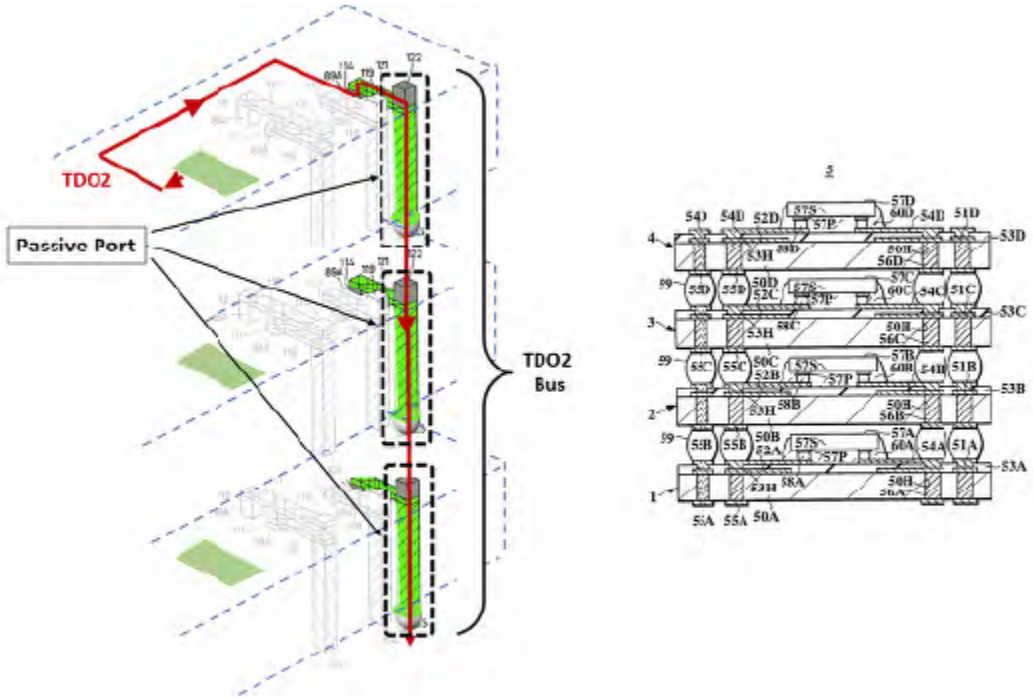
Based on the current record, and for the reasons given by Petitioner, and those summarized above, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that the combined teachings of Hosomi and Sato meet the limitations of independent claim 1 and that a person of ordinary skill in the art would have had sufficient reason to combine the art in the manner proffered by Petitioner.

4. Dependent Claims 2, 11, and 12

Petitioner contends that dependent claims 2, 11, and 12 would have been obvious over the combined teachings of Hosomi and Sato. Petitioner provides a claim-by-claim analysis for each of these dependent claims. *See* Pet. 54–57. Petitioner's analysis is supported by the testimony of Dr. Thompson. *See* Ex. 1003 ¶¶ 145–150.

Patent Owner specifically contests Petitioner's showing with respect to dependent claim 2, which recites "*[t]he stacked module of claim 1 wherein the one or more passive port forms a ladder like routing path, and the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module*."

Petitioner asserts that "[t]he passive ports in the combination of Hosomi and Sato "*form[] a ladder like routing path*" because they create a series of "rungs" allowing a signal to pass horizontally in each module and to travel up or down the stack, as shown by Hosomi's Figure 5 (right) and Thompson Figure M," shown below. Pet. 54–55 (citing Ex. 1003 ¶ 146).



Thompson, Figure M (left); Hosomi, Figure 5 (right)

Figure M, above left, shows the passive ports along TDO2 bus of a combined stacked module, and Hosomi's Figure 5, above right, is a cross section of a semiconductor module in which a plurality of semiconductor devices are stacked. Pet. 54–55; Ex. 1007 ¶ 55. With respect to Figure M, shown above, Patent Owner argues that "there is only a descending signal path TDO2 associated with the alleged passive ports in the asserted combination," and "the illustration fails to disclose or suggest any ladder like routing path formed by a passive port." Prelim. Resp. 27–28.

We note that Petitioner argues that the proposed combination of Hosomi and Sato allows "a signal *to pass horizontally* in each module and to travel up or down the stack." Pet. 54 (citing Ex. 1003 ¶ 146). We also note that Thompson Figure 5 illustrates a horizontal component of TDO2 that Patent Owner does not reference in its argument.

We have considered the evidence and arguments with respect to dependent claims 2, 11, and 12. Based upon the current record, we are persuaded that Petitioner has shown sufficiently for purposes of institution that the combined teachings of the cited art meet the recited limitations of these claims, and that a person of ordinary skill in the art at the time of the invention would have combined the references in the manner proffered and would have had a reasonable expectation of success in that endeavor.

F. Asserted Obviousness Based on Sung and Watanabe

Petitioner also contends that claims 1, 2, 11, and 12 are rendered obvious by the combination of Sung and Watanabe. Pet. 57–102. Petitioner provides a detailed claim analysis, supported by expert testimony. *Id.*; Ex. 1003 ¶¶ 151–257.

Patent Owner contests Petitioner's position with respect to these claims, and in particular, argues that Petitioner has failed to establish that its combination of Sung and Wantanabe discloses a "*first serial chain route*" or a "*control input signal*" as recited by independent claim 1. *See* Prelim. Resp. 28–36. Patent Owner also argues that Petitioner has failed to establish that its proposed combination discloses a "*ladder like routing path*" formed by a "*passive port*" as recited by dependent claim 2. *See* Prelim. Resp. 36–38.

We have considered Petitioner's and Patent Owner's evidence and arguments with respect to claims 1, 2, 11, and 12. However, because we determine that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge to claim 1 under 35 U.S.C. § 103(a) as obvious over the combined teachings of Hosomi and Sato, we institute *inter partes* review as to all other challenges in the Petition, including Petitioner's challenges to

claims 1, 2, 11, and 12 under 35 U.S.C. § 103(a) as obvious over the combined teachings of Sung and Wantanabe. *See PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018).

IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds asserted in the Petition.

V. ORDER

Upon consideration of the record before us, it is

ORDERED that *inter partes* review of claims 1, 2, 11, and 12 of the '243 patent is instituted on all grounds in the Petition;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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