

UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>	Attorney Docket No.	6005.007CIP
	First Inventor	ARCEDERA, Mark
	Title	Optimizing Memory Operations in ...
	Express Mail Label No.	

APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450										
<p>1. ☐ Fee Transmittal Form (e.g., PTO/SB/17)</p> <p>2. ☒ Applicant claims small entity status. <small>See 37 CFR 1.27.</small></p> <p>3. ☒ Specification [Total Pages <u>32</u>] <small>Both the claims and abstract must start on a new page (For information on the preferred arrangement, see MPEP 608.01(a))</small></p> <p>4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>2</u>]</p> <p>5. Oath or Declaration [Total Sheets <u>5</u>] a. ☒ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) <small>(for continuation/divisional with Box 18 completed)</small> i. ☐ DELETION OF INVENTOR(S) <small>Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).</small></p> <p>6. ☒ Application Data Sheet. See 37 CFR 1.76</p> <p>7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix) ☐ Landscape Table on CD</p> <p>8. Nucleotide and/or Amino Acid Sequence Submission <small>(if applicable, items a. – c. are required)</small> a. ☐ Computer Readable Form (CRF) b. Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies</p>	ACCOMPANYING APPLICATION PARTS <p>9. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee _____</p> <p>10. ☐ 37 CFR 3.73(b) Statement <small>(when there is an assignee)</small> ☐ Power of Attorney</p> <p>11. ☐ English Translation Document (if applicable)</p> <p>12. ☐ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached</p> <p>13. ☐ Preliminary Amendment</p> <p>14. ☐ Return Receipt Postcard (MPEP 503) <small>(Should be specifically itemized)</small></p> <p>15. ☐ Certified Copy of Priority Document(s) <small>(if foreign priority is claimed)</small></p> <p>16. ☐ Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.</p> <p>17. ☐ Other: _____</p>										
<p>18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:</p> <p>☐ Continuation ☐ Divisional ☒ Continuation-in-part (CIP) of prior application No.: _____</p> <p>Prior application information: Examiner <u>Hashem Farrokh</u> Art Unit: <u>2187</u></p>											
19. CORRESPONDENCE ADDRESS											
<p>☒ The address associated with Customer Number: 64180 OR ☐ Correspondence address below</p>											
<table border="1" style="width: 100%; border-collapse: collapse;"><tr><td colspan="2">Name</td></tr><tr><td colspan="2">Address</td></tr><tr><td>City</td><td>State</td></tr><tr><td>Country</td><td>Zip Code</td></tr><tr><td>Telephone</td><td>Email</td></tr></table>		Name		Address		City	State	Country	Zip Code	Telephone	Email
Name											
Address											
City	State										
Country	Zip Code										
Telephone	Email										
<table border="1" style="width: 100%; border-collapse: collapse;"><tr><td>Signature</td><td>/Stephen R. Uriarte/</td><td>Date</td><td>25 Nov 2008</td></tr><tr><td>Name (Print/Type)</td><td>Stephen R. Uriarte</td><td>Registration No. (Attorney/Agent)</td><td>40,854</td></tr></table>		Signature	/Stephen R. Uriarte/	Date	25 Nov 2008	Name (Print/Type)	Stephen R. Uriarte	Registration No. (Attorney/Agent)	40,854		
Signature	/Stephen R. Uriarte/	Date	25 Nov 2008								
Name (Print/Type)	Stephen R. Uriarte	Registration No. (Attorney/Agent)	40,854								

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)****Title of
Invention****OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE**

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ Application No. _____ filed on _____
- ☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

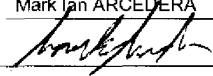
Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Mark Ian ARCEDERA

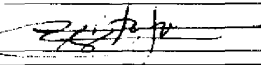
Date: Nov 26, 2008

Signature: 

Citizen of: Philippines

Inventor two: Ritchie BABAYLAN

Date: Nov 26, 2008

Signature: 

Citizen of: Philippines

☒ Additional inventors or a legal representative are being named on _____ ONE additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet
Page <u>1</u> of <u>1</u>	

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Reyjan		LANUZA	
Inventor's Signature <i>Reyjan C. Lanuza</i>		Date <i>11/25/08</i>	
Gen. T. De Leon Valenzuela City	State	Philippines	Philippines
Residence: City	State	Country	Citizenship
190D Policarpio Street			
Mailing Address			
Gen. T. De Leon Valenzuela City	State	1442	Philippines
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

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DECLARATION – Supplemental Priority Data Sheet

Foreign applications:

[illegible]

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
First Named Inventor/Applicant Name:		Mark Ian Arcedera		
Filer:		Stephen Radcliff Uriarte		
Attorney Docket Number:		6005.007CIP		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	82	82
Utility Search Fee	2111	1	270	270
Utility Examination Fee	2311	1	110	110
Pages:				
Claims:				
Claims in excess of 20	2202	20	26	520
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				982

Electronic Acknowledgement Receipt	
EFS ID:	4357691
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian Arcedera
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	25-NOV-2008
Filing Date:	
Time Stamp:	23:23:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 982
RAM confirmation Number	6564
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		6005_007CIP_SpecALL_20081124C.pdf	159070	yes	32
			b4f6284acfb316e8daac15a36d0c8297c92a1e93		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	19	
	Claims		20	31	
	Abstract		32	32	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	6005_007CIP_FIGS_20081125.pdf	203458	no	2
			1759a58d6b2548a5fcd7a36a7e0ec4fa8fcd591		
Warnings:					
Information:					
3	Application Data Sheet	6005_007CIP_ADS_20081125C.pdf	836613	no	5
			72a5f7ad5ae19155997e689165463b326905ad01		
Warnings:					
Information:					
4	Transmittal of New Application	6005_007CIP_AppnTL_20081125.pdf	278964	no	2
			f32ca37885ff06637e58086cb9fc27db8fb608bd		
Warnings:					
Information:					
5	Oath or Declaration filed	6005_007CIP_Decl_SignedAll_20081125B.pdf	193252	no	5
			8e5e7f63e78a05f85f4865135ab88da0cca7b2a7		
Warnings:					
Information:					
6	Fee Worksheet (PTO-06)	fee-info.pdf	36712	no	2
			38940f32637f99baca6f26a9d337cf2f980ea780		
Warnings:					
Information:					
Total Files Size (in bytes):			1708069		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

This patent application is submitted on behalf of Mark Ian Arcedera, Ritchie Babayan and Reyjan Lanuza, assignors to BiTMICRO Networks, Inc.

SPECIFICATION

Title of the Invention

OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Cross-Reference to Related Applications

[001] This application is a continuation in part application and claims the benefit of United States patent application, entitled "Optimized Placement Policy for Solid State Storage Devices, filed on 8 June 2006, and having Serial No.: 11/450,005 and attorney docket number 6005.007, and of United States patent application, entitled "Hybrid Multi-Tiered Caching Storage Systems", filed on 8 June 2006, and having Serial No.: 11/450,023 and attorney docket number 6005.006, which are incorporated herein as if fully set forth herein.

Field of Invention

[002] The present invention relates to solutions for optimizing memory operations in a memory system suitable for use in an electronic storage device. More particularly, the present invention relates to solutions for increasing the likelihood that the operational load imposed on the memory system by these memory operations, performed in response to an I/O transaction request, will be optimally distributed across resources used by the memory system, increasing operational efficiency, reducing memory operation latency or both.

Background

[003] Electronic storage devices that respectively employ a memory system that includes memory devices, memory chips, or modules that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices. The computer device industry has increased the adoption of these solid state storage devices due to certain advantages offered by these types of storage devices over other forms of storage devices, such as rotational drives. The adoption of solid state storage devices as enhancement or even a replacement to rotational drives is not without some difficulty because many conventional computer devices, sometimes referred to as "hosts", use host operating systems, file systems, or both that are optimized for use with rotational drives rather than solid state storage devices. For example, unlike rotational drives, solid state storage devices that use NAND flash memory, also referred to as "flash drives", suffer from write cycle limitations and to a certain degree, bad blocks. In addition, flash drives use block addressing rather than byte addressing, and these flash drives use block addresses that are usually much larger than the block address used by the host. Block addressing may impose an additional level of complexity and additional processing cycles when performing a write operation, and which in turn, may increase write operation latency. This additional level of complexity may include performing a read-modify-write transaction to complete the write operation.

[004] Many conventional host operating and file systems, however, do not employ mechanisms to solve these write cycle, bad block, or block level addressing issues. Consequently, flash drive manufacturers sometimes employ, at the storage device level, flash memory related techniques that include read-modify-write transactions,

wear leveling, bad block management or any combination of these to minimize or manage the write cycle limitation and bad blocks common to flash drives. Other host file systems, such as file systems that employ a write in place method, might use a "flash translation layer" to avoid excessive wear to a particular block of flash memory.

[005] The use of these flash memory related techniques at the storage device level, or a flash translation layer at the host level, however, may decrease storage device performance, increase transaction or memory operation latency, or render the storage device as a primary bottleneck to the processing efficiency of a host or a computing network. In response, some solid state storage device manufacturers have implemented "brute force" or active solutions that include using more complex algorithms and "faster" processing devices, such as CPUs, to handle and process these algorithms. These active solutions, however, increases device costs and in most cases, design complexity.

[006] Consequently, a need exists for a solution that optimizes memory operations performed by or in an electronic storage device with a relatively minimal increase in device complexity and costs. These optimizing memory operations include increasing the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources, such as by interleaving or parallel memory operations, reducing memory operation latency, increasing operational device efficiency, or both.

Summary

[007] Solutions for optimizing memory operations performed by or in an electronic storage device in response to receiving an I/O transaction request initiated by a host are disclosed. In one implementation, a mapping table is used and disposed to include: a set of logical fields, including a first logical field and a second logical field, with these logical fields respectively disposed for representing a plurality of LBA sets, including the first logical field disposed for representing a first LBA set and the second logical field disposed for representing a second LBA set, the first and second LBA sets each representing a set of consecutive LBAs. The mapping table further includes a set of PBA fields, including a first PBA field and a second PBA field, with these set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, with these PBAs each associated with a physical memory location in a memory store, and these set of logical fields and set of PBA fields disposed to associate the first and second LBA sets with the first and second PBAs; and wherein, in response to receiving the I/O transaction request, the mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with the first and second PBAs, if the I/O transaction request is associated with the first and second LBA sets.

Brief Description of Drawings

[008] FIG. 1 is a block diagram of an electronic storage device that includes a memory system which uses a memory table for increasing the likelihood that

optimized memory operations will be performed in accordance with one embodiment of the present invention.

[009] FIG. 2 is a mapping table for an electronic storage device, such as the electronic storage device illustrated in FIG. 1, in accordance with another embodiment of the present invention.

Detailed Description of the Invention

[0010] For clarity purposes, not all of the routine features of the embodiments described herein are shown or described. It is appreciated that in the development of any actual implementation of these embodiments, numerous implementation-specific decisions may be made to achieve a developer's specific goals. These specific goals will vary from one implementation to another and from one developer to another. This development effort might be complex and time-consuming but would nevertheless be a routine engineering undertaking for those of ordinary skill in the art having the benefit of this disclosure. In addition, the elements used in the embodiments described herein may be referred to using the variable symbol n , which is intended to reflect any number greater than one (1).

[0011] The various embodiments of the present invention disclosed herein relate to solutions for optimizing memory operations in a memory system suitable for use in an electronic storage device. More particularly, the present invention pertains to solutions that increase the likelihood which, in response to an I/O transaction initiated by a host, the operational load imposed on the memory system by these memory operations will be optimally distributed across resources used by the memory system, reducing memory operation latency, increasing operational device efficiency, or both.

This memory system, such as memory system 4, may be used with or implemented in an electronic storage device 2, in the manner illustrated in FIG. 1 in accordance with one embodiment of the present invention. Memory system 4 is coupled to a memory store 6 via a set of buses, such as buses 8-0 and 8-1, and uses a mapping table 9. Memory system 4 also includes a DMA controller 10 that includes a flash buffer controller 16 and a set of direct memory access engines, which are suitable for performing DMA operations on memory devices used by memory store 6.

[0012] When designed to operate with flash memory devices, these direct memory access engines may be also herein referred to as FDEs, and in the example shown in FIG. 1, are illustrated as FDEs 22-01, 22-02, 22-11 and 22-12. An FDE represents a device that is capable of controlling a flash memory device and performing DMA operations on the flash memory device in response to commands generated by storage device 2 through storage device controller 24. These DMA operations include facilitating high speed data transfers to and from memory devices that are included as part of memory store 6, such as flash memory devices 12-01 and 12-02. Buses 8-0 and 8-1 respectively function as a bus interface that is used by an FDE to control and communicate with selected flash memory devices in memory store 6. For example, bus 8-0 may be used by FDE 22-01 to control flash memory devices, such as flash memory devices 12-01, that are coupled to bus 8-0 and that have chip enables (not shown) which are controllable by FDE 22-01, while bus 8-1 may be used by FDE 22-11 to control flash memory devices, such as flash memory devices 12-01, that are coupled to bus 8-1 and that have chip enables (not shown) which are controllable by FDE 22-11. In another example, bus 8-0 may be used by FDE 22-02 to control flash memory devices, such as flash memory devices 12-02, that are coupled to bus 8-0

and that have chip enables which are controllable by FDE 22-02, while bus 8-1 may be used by FDE 22-12 to control flash memory devices, such as flash memory devices 12-02 in flash, that are coupled to bus 8-1 and that have chip enables which are controllable by FDE 22-12.

[0013] DMA controller 10 also includes a flash buffer controller 16. Flash buffer controller 16 is disposed to drive each bus utilized by memory system 4 and to translate command signals asserted by FDEs 22-0 through 22-12 into native memory device commands that are compatible with the memory device selected to receive these commands. In the example shown in FIG. 1, these memory device commands are in the form of native flash memory device commands. The number of buses, flash memory devices and FDEs shown in FIG. 1 are not intended to be limiting in any way and may be selected according to a variety of factors, such as the performance, cost, capacity and any combination of these which may be desired.

[0014] One of ordinary skill in the art having the benefit of this disclosure would readily recognize that DMA controller 10 may be implemented using a different configuration disclosed herein and may include other types of processors, DMA engines, or equivalent components. The term "host" means any device that can initiate an I/O transaction request which can be received by an electronic storage device that is targeted for receiving the I/O transaction request. For example, in FIG. 1, host 18 can initiate an I/O transaction request 20, which is received and processed by storage device 2 as described herein.

[0015] Storage device 2 represents any storage device that may be used with the optimized memory operation solutions and embodiments disclosed herein. For

example, storage device 2 may be further configured to include a processing unit, such as a CPU, a bus, a working memory, such as DRAM, and an I/O interface, which may be in the form of a SATA, iSCSI, SATA, Fibre Channel, USB, eSATA interfaces, a network adapter, a PCI or PCI-e bus bridge, or the like. These storage device components enable storage device 2 to execute an embedded operating system (not shown) necessary for processing I/O transactions that are initiated by a host through a suitable network, and that are eventually received and processed by storage device 2 through various device resources, including memory system 4, buses 8-0 and 8-1, and memory store 6. The processing unit, bus, DRAM, embedded operating system, and I/O interface are generally known, and thus, are hereinafter referred to and shown collectively in the form of a storage device controller 24 to avoid over complicating the herein disclosure. In addition, although DMA controller 10 is shown as a separate component device in FIG. 1, DMA controller 10 may be integrated with any other component employed by a storage device and thus, the form factor of DMA controller 10 is not intended to be limiting in any way. For example and although not shown in FIG. 1, DMA controller 10 may be part of or integrated within a storage device controller that has a function similar to storage device controller 24. In another example, DMA controller 10 may be implemented in the form of Flash DMA controller 109, which is part of hybrid storage controller 102, which are further disclosed in FIG. 1 of United States patent application, entitled "Hybrid Multi-Tiered Caching Storage Systems", filed on 8 June 2006, and having Serial No.: 11/450,023 and attorney docket number 6005.006.

[0016] Memory store 6 may be configured to include a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs. In

FIG. 1, these memory devices, buses, and FDEs are implemented in the form of flash memory devices 12-01 and 12-02; buses 8-0 and 8-1; and FDEs 22-01, 22-02, 22-11, and 22-12, respectively. The term "flash memory device" is intended to include any form of non-volatile memory, including those that use blocks of non-volatile memory cells, named flash blocks. Each memory cell may be single or multi-level. In FIG. 1, flash blocks 23-0 through 23-n are shown for each flash memory device illustrated. In addition, the number of flash memory devices, bus interfaces, and FDEs illustrated in FIG. 1 is not intended to be limiting in any way. Instead, the number of these devices may be increased or decreased, depending on the performance, cost and storage capacity desired.

[0017] A flash memory device permits memory operations, such as a write or read operation, to be performed on these flash blocks according to a protocol supported by the flash memory device. A flash memory device may be implemented using a flash memory device that complies with the Open NAND Flash Interface Specification, commonly referred to as ONFI Specification. The term "ONFI Specification" is a known device interface standard created by a consortium of technology companies, called the "ONFI Workgroup". The ONFI Workgroup develops open standards for NAND flash memory devices and for devices that communicate with these NAND flash memory devices. The ONFI Workgroup is headquartered in Hillsboro, Oregon. Using a flash memory device that complies with the ONFI Specification is not intended to limit the embodiment disclosed. One of ordinary skill in the art having the benefit of this disclosure would readily recognize that other types of flash memory devices employing different device interface protocols may be used, such as protocols compatible with the standards created through the Non-Volatile Memory Host

Controller Interface ("NVMHCI") working group. Members of the NVMHCI working group include Intel Corporation of Santa Clara, California, Dell Inc. of Round Rock, Texas and Microsoft Corporation of Redmond, Washington.

[0018] Mapping table 9 may be implemented in the manner shown in FIG. 2, which is discussed below in conjunction with FIG. 1. Mapping table 9 includes a set of fields, named logical fields 26, and a set of PBA fields 28. Each PBA field from set of PBA fields 28 is disposed to represent a unique addressable physical memory location, named "PBA, in memory store 6, such as PBA 46, 48, 50 or 51. For each PBA field, this physical memory location may be represented by using a set of access parameter fields 30 and a memory index field 32. The set of access parameters fields 30 includes a bus identifier field 34, a FDE identifier field 36, and a group identifier field 38.

[0019] Bus identifier field 34 is disposed to represent a bus identifier, which is an identifier that is used for representing a bus interface, such as bus 8-0 or 8-1. FDE identifier field 36 is disposed to represent a FDE identifier, which is an identifier for identifying one FDE from another FDE from a set of FDEs that are coupled to the same bus interface. The forms of the bus and FDE identifiers are not intended to be limiting in any way as long as the bus identifiers and FDE identifiers employed enable the selection of a specific bus from a set of buses, and the selection of a specific FDE from a set of FDEs that are coupled to the same bus via flash buffer controller 16. Flash memory devices coupled to the same bus may be hereinafter referred to as a flash array bank. For example, flash memory devices 12-01 and 12-02 that are coupled to bus 8-0 are in a flash array bank 14-0, while flash memory devices 12-01 and 12-02 that are coupled to bus 8-1 are in a flash array bank 14-1.

[0020] Flash memory devices that are controlled by the same FDE may be hereinafter referred to as a flash array bank interleave. For instance, in flash array bank 14-0, flash memory devices 12-01 are controlled by FDE 22-01 and are thus, in one flash array bank interleave 14-0-0, while flash memory devices 12-02 are controlled FDE 22-02 and are thus, in another flash array bank interleave, such as flash array bank interleave 14-0-1. Similarly, in flash array bank 14-1, flash memory devices 12-01 are controlled by FDE 22-11 and are thus, in flash array bank interleave 14-1-0, while flash memory devices 12-02 are controlled FDE 22-12 and are thus, in flash array bank interleave 14-1-1. Selection of a flash memory device may be provided by coupling the chip select line (not shown) of the flash memory device to a FDE.

[0021] Group identifier field 38 is disposed to represent a group identifier, which is an identifier for identifying one flash memory device from another flash memory device from a set of flash devices that are controlled by the same FDE. For example, in flash array bank interleave 14-0-0, since flash memory devices 12-01 are controlled by FDE 22-01, each of these flash memory devices are represented using different group identifiers, such as group identifiers 15-0 and 15-1.

[0022] Group identifiers are selected and assigned to flash memory devices so that no more than one flash memory device, which is within the same flash array bank interleave or which is controlled by the same FDE, is associated with the same group identifier. Flash memory devices may share the same group identifier as long as these flash memory devices are not controlled by the same FDE. In the example embodiment in FIG. 1, flash memory devices 12-01 and 12-02 share the same group

identifier, such as group identifier 15-0 or 15-1, because these flash devices are controlled by different FDEs, such as FDEs 22-01 or 22-02, respectively.

[0023] In FIG. 2, mapping table 9 reflects the embodiment disclosed in FIG. 1. PBA 46 and PBA 50 include access parameters that are associated with the same group identifier of 15-0 but pertain to physical memory locations within different flash memory devices in memory store 6. These access parameters are associated with different FDE identifiers, such as FDE identifiers 22-01 and 22-11 and with different bus identifiers 8-0 and 8-1, respectively. Using their respective access parameters, PBA 46 is associated with a physical memory location that is within a flash memory device 12-01 coupled to bus 8-0, controlled by FDE 22-01, and in group 15-0, while PBA 50 is associated with another physical memory location that is within a flash memory device 12-01 coupled to bus 8-1, controlled by FDE 22-11, and in group 15-0 in FIG. 1.

[0024] The term "LBA", which may also be referred to herein as a logical block address, is intended to represent an address that is part of a logical addressing system (not shown) used by a host, such as host 18, and this host may use one or more LBAs in an I/O transaction request, such as I/O transaction request 20. Mapping table 9 associates LBAs from this host logical addressing system to the device addressing system used by storage device 2. This device addressing system may include using a mapping table that includes the functionality described herein, such as mapping table 9. These LBAs may be grouped into sets of consecutive LBAs, named "LBA sets". These LBA sets may then be represented using logical fields 26 from mapping table 9, where each logical field in set of logical fields 26 is respectively disposed to represent a LBA set. For example, LBA sets 40, 42, 44, and 45 may be

used to respectively represent consecutive LBAs used by host 18, such as LBAs 00 through 07, LBAs 08 through 15, LBAs 16 through 23, and LBAs 24-31, respectively.

[0025] Logical fields in mapping table 9 may be initialized to represent LBA sets that are serially arranged in mapping table 9 so that LBAs from adjacent LBA sets are contiguous. In the example shown in FIG. 2, LBA sets 40, 42, 42, 44 and 45 represent serially arranged LBAs since the highest LBA in one LBA set is contiguous with the lowest LBA in an adjacent LBA set. Specifically, LBA sets 40 and 42 are disposed in adjacent rows and thus are adjacent to each other. These adjacent LBA sets are also contiguous because LBA 7, which corresponds to the highest LBA in LBA set 40, is contiguous with LBA 8, which is the lowest LBA in LBA set 42. Similarly, LBA sets 42 and 44 are also contiguous because LBA 15, which corresponds to the highest LBA in LBA set 42, is contiguous with LBA 16, which is the lowest LBA in LBA set 44. LBA set 44 is also contiguous with LBA set 45.

[0026] In addition, storage device 2 initializes mapping table 9 by creating an association between these LBA sets and PBAs so that adjacent LBA sets are mapped to PBAs, and any two adjacent PBAs differ by at least one access parameter. The term "two adjacent PBAs" is intended to include any two PBAs that are respectively mapped to adjacent LBAs in mapping table 9. This mapping association among LBA sets and PBAs increases the likelihood that memory operations resulting from an I/O transaction request will be optimized because if these memory operations involve data accesses associated with contiguous LBA sets these data accesses will in likelihood occur on different PBAs. This results in the likelihood that different storage resources will be used, such as different buses, different FDEs, different groups or any

combination of these, which provides a form of interleaving by bus, FDE, flash memory device group or any combination of these.

[0027] Each LBA set also includes a LBA set size, which is a function of the number of LBAs used in each LBA set and the LBA size of each LBA. For example, each LBA set may be associated with eight LBAs and if each LBA has an LBA size equal to 512 bytes, then LBA set 40 has an LBA set size of 4 Kilobytes (KB). If a flash block within a given flash memory device has a block size of 16KB, an LBA set size of 4KB would permit a maximum of four PBAs that can be mapped to this flash block. Similarly, if a flash block has a flash block size of 32KB, an LBA set size of 4KB would permit a maximum of eight PBAs that can be mapped to this flash block. In the example shown in FIG. 2, the LBA set size selected is set equal to a section size (not illustrated in figure). The term "section size" is the size of the minimum portion in which data may be transferred or relocated between physical memory locations in memory store 6. In addition, the section size may be limited to a size that is at least equal to the product of a positive integer multiplied by the native page size used by a flash block. For example, if the native page size for flash block 23-0 is 4KB, then the section sizes that may be used would be limited to 4KB, 8KB, 12K, and so on.

[0028] In an alternative embodiment, if a flash memory device supports more than one page write cycle that can be performed on a page before requiring an erase cycle to be performed on the flash block containing the page, then the section size may be set to a size that is at least equal to the quotient that results from dividing the native page size of the flash block by the number of page writes supported by the flash memory device. For example, if flash block 23-0 from flash memory device 12-01 supports two page writes on a page before requiring an erase cycle on flash block 23-

0 and the flash block 23-0 has a native page size of 4KB, then the section size may be set at least equal to 2KB. Since the LBA set size selected is equal to the section size, in this alternative embodiment, the LBA set used would have an LBA set size of 2KB.

[0029] Besides access parameter field 30, each PBA field also includes a memory index field 32, which may be used to represent a memory index, such as 0x00 or 0x08 in FIG. 2. Each memory index represents the starting address boundary of a physical memory location in a flash memory device in memory store 6, such as flash memory device 12-01 or 12-02. This physical memory location is used as the target physical memory location for reading or writing data that is associated with an LBA set that is mapped to the PBA associated with the memory index. A physical memory location is disposed to have a size, named "physical memory location size", that is at least equal to the LBA set size of this LBA set.

[0030] A physical memory location is comprised of one or more programmable portions. For example, if flash memory device 12-01 includes flash blocks that have programmable portions with a programming size of 512B, then each programmable portion may be associated with a unique memory index that represents the starting address boundary of each programmable portion in the flash memory device. A memory index of 0x00 may be used to represent the starting address boundary of a first 512B programmable portion, a memory index of 0x01 may be used to represent the starting boundary of a second 512B programmable portion, and so on until the last available programmable portion in a flash memory device is associated with a memory index. These programmable portions have a programming size that is equal to or less than the minimum erase size of a flash memory device. Since some flash memory devices are erasable by flash block, implementations that use flash memory

devices may be implemented with a programming size that is less than or equal to the flash block size.

[0031] In the embodiment shown in FIG. 2, memory index fields 32 are initialized to represent the memory indices of physical memory locations that are respectively comprised of more than one programmable portion, named portion set. Although more than one programmable portion comprises each physical memory location, a single memory index is used to represent each physical memory location in each memory index field 32. Each of these memory indices represents a starting address boundary of a programmable portion that is from a portion set associated with a physical memory location and that is the lowest of the other memory indices associated with the programmable portions in the portion set. The number of programmable portions comprising a physical memory location is a function of the programming size of these programmable portions and the LBA set size used. Each of these memory indices represented in memory index fields 32, respectively, are used to represent the starting boundary of a physical memory location that spans across the portion set comprising the physical memory location. For example, if LBA set 40 has an LBA set size of 4KB, and flash device 12-01 uses flash blocks having flash block sizes of 16KB and a programmable portion size of 512B, then the memory indices represented in memory index fields 32 would differ by at least by the size of the LBA set, such as 0x00, 0x08, 0x16, 0x24, and so on. Each of these memory indices represents the starting boundary of a physical memory location that spans across eight programmable portions. In effect, each of these memory indices functions as a physical memory address for a physical memory location that has a size equal to eight programmable portions.

[0032] In an alternative embodiment (not shown), if each physical memory location is comprised to have only one programmable portion, then each memory index that represents the starting address boundary of a physical memory location spans across only one programmable portion. Each memory index would differ by a single programmable portion size. For instance, if the programmable portion size is 512B, then each memory index represented by memory index fields 32 would differ by at least 512B, such as 0x00, 0x01, 0x02, and so on. In addition, mapping table 9 is initialized so that two different LBA sets are not mapped to the same PBA.

[0033] Assigning a single index for each starting address boundary of a programmable portion having a 512B programmable portion size is not intended to be limiting in any way. One of ordinary skill in the art after receiving the benefit of the herein disclosure would readily recognize that other indexing methods may be used. For instance, in yet another alternative embodiment (not shown), each index may be used to represent a byte of memory, which renders the flash memory devices in memory store 6 byte addressable in mapping table 9. This alternative approach results in indices, such as 0x0000, 0x1000, 0x2000 and so on, that have widths sufficient to represent the starting address boundaries of physical memory locations which have a physical memory location size sufficient to hold data represented by an LBA set size of 4K.

[0034] During operation and after initialization of mapping table 9, if storage device controller 22 receives an I/O transaction request 20 from host 18, storage device controller 22 processes I/O transaction request by transferring it to DMA controller 10. After receiving I/O transaction request 20, DMA controller 10 uses mapping table 9 to determine which PBAs are mapped to LBAs used in I/O transaction

request 20. DMA controller 10 uses the PBAs to determine which addressable physical memory locations to use when performing memory operations requested by host 18 through I/O transaction request 20. Mapping table 9 associates LBA sets to PBAs in a manner that increases the likelihood that memory operations resulting from I/O transaction request 20 will be optimized by distributing these memory operations across different storage device resources that are associated with these PBAs, such as across different FDEs, different buses, different flash memory devices, or any combination of these.

[0035] For example, still referring to FIGS. 1 and 2, I/O transaction request 20 may be in the form of a write transaction that targets LBAs 00-07 and 08-15. An I/O transaction that is associated with consecutive LBAs is sometimes referred to as a sequential I/O transaction. Since mapping table 9 has been initialized to map these LBAs 00-07 and LBAs 08-15 with LBA sets 40 and 42, respectively, DMA controller would more than likely be able to perform memory operations required by I/O transaction request 20 in an optimal manner by interleaving these memory operations across different buses, different FDEs, different flash memory devices, or any combination of these. Since in the example shown in FIG. 2, PBAs that are mapped to adjacent LBA sets have different Bus, FDE, flash device group identifiers or any combination of these, DMA controller 10 may interleave by Bus, FDE, or flash memory device. In one embodiment of the present invention, if interleaving may be performed through more than one access parameter, DMA controller 10 prioritizes interleaving first by Bus, then by FDE and then by flash memory device.

[0036] Using different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9, enables the interleaving of memory operations across flash devices

that are controlled by the same FDE. Stated another way, using different group identifiers enables interleaving memory operations across flash devices that belong to the same flash array bank interleave. Using different FDE identifiers in mapping table 9 enables interleaving memory operations across flash memory devices that are controlled by different FDEs, while using different bus identifiers enables interleaving memory operations across flash memory devices that are coupled to different flash bus interfaces.

[0037] While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments. Rather, the present invention should be construed according to the claims below.

We claim:

1. A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

2. The mapping table of claim 1, wherein:

said first and second LBA sets are adjacent LBA sets;

said first and second access parameters are different; and

said LBAs from said first and second LBA sets are logical block addresses used by the host for addressing said data.

3. The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

4. The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is not consecutive with an LBA having the highest LBA value from said first LBA set.

5. The mapping table of claim 1, wherein:

data stored at a first physical memory location, which is addressable using said first PBA, is transferred to a second physical memory location, which is addressable using said second PBA, said data transferred in portions equal to a section size.

6. The mapping table of claim 5, wherein:

said first and second LBA sets respectively have an LBA set size equal to said section size.

7. The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

8. The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that supports more than one page write that can be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said one of said flash blocks; and

said section size is at least equal to a quotient resulting from dividing said native page size by said more than one page write.

9. The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier.

10. The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.

11. The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers.

12. The mapping table of claim 1, wherein said first and second PBA include different bus identifiers.

13. The mapping table of claim 1, wherein said first and second PBA include different FDE identifiers.

14. The mapping table of claim 1, wherein said first and second PBAs respectively include a first group identifier and a second group identifier.

15. The mapping table of claim 1:

wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and

wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs.

16. The mapping table of claim 1, wherein:

said memory store includes a first set of memory devices controlled by a first FDE and a second set of memory devices controlled by a second FDE; and

said first and second sets of memory devices associated with a plurality of group identifiers in which no two of said group identifiers is the same, and each memory device from said first set of memory devices is respectively associated with different group identifiers from said plurality of group identifiers.

17. The mapping table of claim 1, wherein:

said electronic storage device includes a storage device controller, said memory store, and a memory system;

said memory system includes a flash buffer controller, a first set of FDEs, a second set of FDEs, and a set of buses that includes a first bus and a second bus;

said memory store includes a first set of memory devices and a second set of memory devices, said first and second set of memory devices respectively coupled to said first and second buses;

said first set of FDEs disposed to control said first set of memory devices through said flash buffer controller and said first bus, said first set of FDEs including a first FDE and a second FDE;

said second set of FDEs disposed to control said second set of memory devices through said flash buffer controller and said second bus, said second set of FDEs including a third FDE and a fourth FDE;

said first and second set of memory devices are associated with a plurality of memory device groups, including a first group and a second group;

wherein said first and second groups corresponding respectively to said first and second group identifiers; and

wherein said first and second PBAs respectively include said first and second group identifiers.

18. The mapping table of claim 17, wherein said first and third memory devices are associated with a first group identifier and said second and fourth memory devices are associated with a second group identifier.

19. The mapping table of claim 17, wherein said first and second memory devices include non-volatile solid state memory cells.

20. The mapping table of claim 17, wherein each memory device from said first set of memory devices are respectively associated with different group identifiers.

21. The mapping table of claim 1, wherein said first PBA further disposed to represent a memory index.

22. A memory system for optimizing memory operations in an electronic storage device responsive to an I/O transaction request initiated by a host, said electronic storage device including a memory store having a set of memory devices including a first memory device, a second memory device, a third memory device and a fourth memory device, said memory system comprising:

a flash buffer controller, a set of FDEs, and a set of buses, wherein said set of FDEs including a first FDE, a second FDE, a third FDE, and a fourth FDE and wherein said buses including a first bus and a second bus, said first bus coupled to the first and second memory devices, and the second bus coupled to said third and fourth memory devices;

said first and second FDEs coupled to said first bus through said first buffer controller, and said third and fourth FDEs coupled to said second bus through said first buffer controller;

said set of memory devices are partitioned into memory device groups, including a first group and a second group;

a mapping table that includes:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for holding a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory

locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.

23. The memory system of claim 22, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

24. The memory system of claim 22, wherein said first and third memory devices correspond to a first group identifier and said second and fourth memory devices correspond to a second group identifier.

25. The memory system of claim 22, wherein said optimized memory operations include a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

26. The memory system of claim 25, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier and a group identifier.

27. The memory system of claim 26, wherein said first and second PBAs respectively include said first and second group identifiers.

28. The memory system of claim 22, wherein said PBA further includes a memory index.

29. The memory system of claim 22, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

30. The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

31. The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

32. An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:

a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;

a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;

a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;

wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs; and

wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.

33. The electronic storage device of claim 32, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

34. The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

35. The memory system of claim 34, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier, and a group identifier.

36. The memory system of claim 35, wherein said first and second PBAs respectively include said first and second group identifiers.

37. The electronic storage device of claim 32, wherein said PBA further includes a memory index.

38. The electronic storage device of claim 32, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

39. The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

40. The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

Abstract

To optimize memory operations, a mapping table may be used that includes: logical fields representing a plurality of LBA sets, including first and second logical fields for representing respectively first and second LBA sets, the first and second LBA sets each representing a consecutive LBA set; PBA fields representing PBAs, including a first PBA disposed for representing a first access parameter set and a second PBA disposed for representing a second access parameter set, each PBA associated with a physical memory location in a memory store, and these logical fields and PBA fields disposed to associate the first and second LBA sets with the first and second PBAs; and, upon receiving an I/O transaction request associated with the first and second LBA sets, the mapping table causes optimized memory operations to be performed on memory locations respectively associated with the first and second PBAs.

OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Inventors: MARK ARCEDERA et al. Docket #: 6005.007CIP

1/2

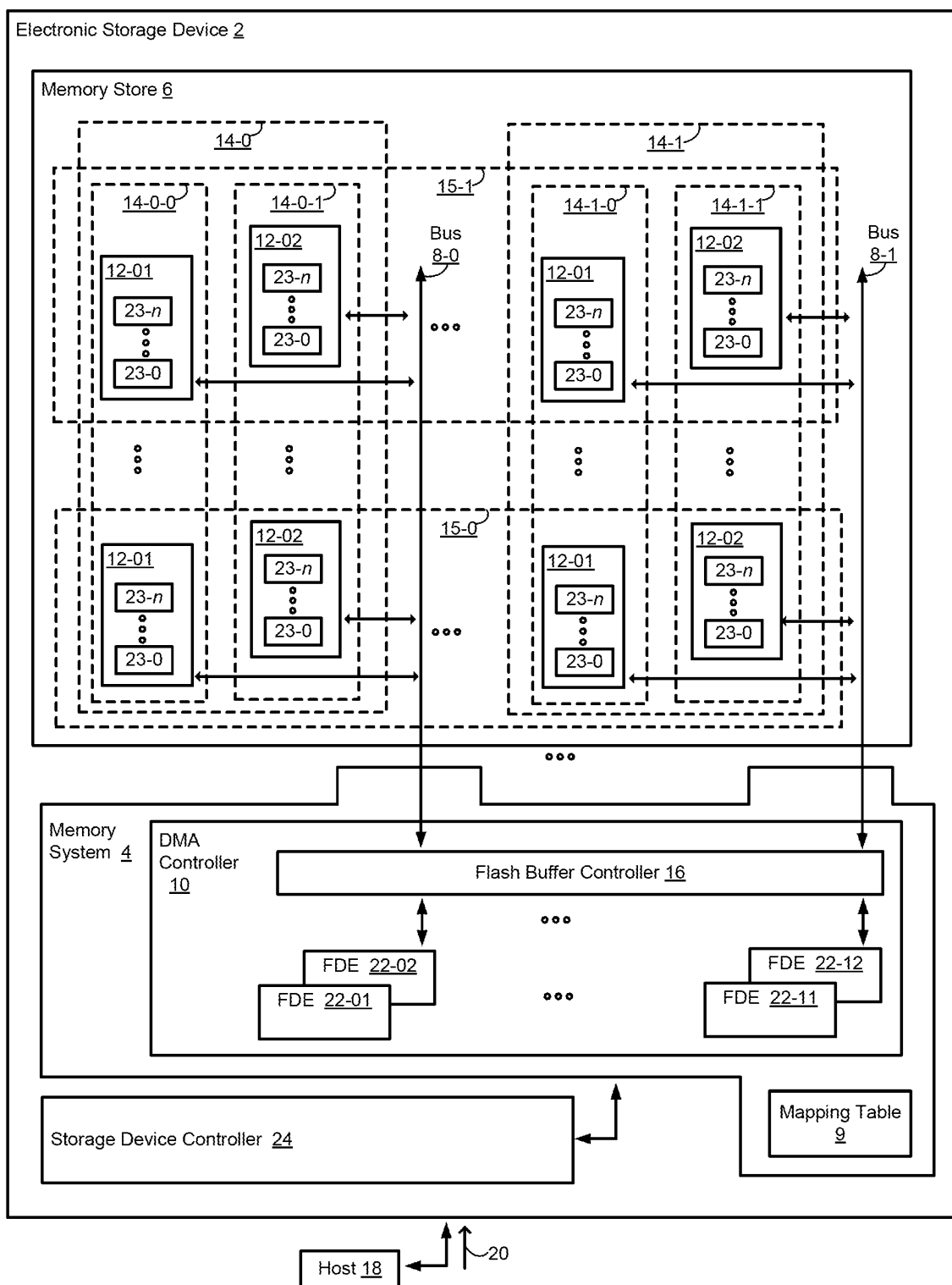


FIG. 1

OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Inventors: MARK ARCEDERA et al. Docket #: 6005.007CIP

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Logical Fields 26	PBA Fields 28			
	Access Parameter Fields 30			Memory Index Fields 32
	Bus Id Fields 34	FDE Id Fields 36	Group Id Fields 38	
40 LBAs 00-07	8-0	22-01	15-0	46 0x00
42 LBAs 08-15	8-0	22-02	15-1	48 0x08
44 LBAs 16-23	8-1	22-11	15-0	50 0x00
45 LBAs 24-31	8-1	22-12	15-1	51 0x08
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮

FIG. 2

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

- ☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Mark	Ian	ARCEDERA		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Paranaque City	Country Of Residenceⁱ	PH		
Citizenship under 37 CFR 1.41(b)ⁱ		PH			
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Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
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Citizenship under 37 CFR 1.41(b)ⁱ		PH			
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Applicant 3					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Reyjan		LANUZA		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Gen. T. De Leon Valenzuela City	Country Of Residenceⁱ	PH		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number		6005.007CIP	
		Application Number			
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE				
Citizenship under 37 CFR 1.41(b) i		PH			
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City	Gen. T. De Leon Valenzuela City			State/Province	
Postal Code	1442	Country	PH		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	64180		
Email Address	info@uriartelaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE				
Attorney Docket Number	6005.007CIP	Small Entity Status Claimed ☒			
Application Type	Nonprovisional				
Subject Matter	Utility				
Suggested Class (if any)		Sub Class (if any)			
Suggested Technology Center (if any)					
Total Number of Drawing Sheets (if any)	2	Suggested Figure for Publication (if any)	2		

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
Customer Number	64180		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	11450005	2006-06-06
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	11450023	2006-06-06
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee ¹				Remove
If the Assignee is an Organization check here. ☒				
Organization Name	BITMICRO Networks, Inc.			
Mailing Address Information:				
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Address 2				
City	Fremont	State/Province	CA	
Country ⁱ	US	Postal Code	94538	
Phone Number	510.623.2341	Fax Number	510.623.2342	
Email Address	info@bitmicro.com			
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Stephen R. Uriarte/			Date (YYYY-MM-DD)	2008-11-25
First Name	Stephen	Last Name	Uriarte	Registration Number	40854

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Filing Date: 11/25/08

Approved for use through 7/31/2006. OMB 0651-0032

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/323,461	
APPLICATION AS FILED – PART I						
(Column 1)		(Column 2)		SMALL ENTITY		OR
OTHER THAN SMALL ENTITY						
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	40	minus 20 = 20	x\$26		x\$52	1040
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *	x\$110		x\$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		390	
			TOTAL		TOTAL	2130
* If the difference in column 1 is less than zero, enter "0" in column 2.						
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY		OR
	Total (37 CFR 1.16(i))	*	Minus **	=	RATE (\$)	ADDITIONAL FEE (\$)
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X =	X =
	Application Size Fee (37 CFR 1.16(s))			X =	X =	X =
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			N/A	N/A	N/A
			TOTAL		TOTAL	
			ADD'T FEE		ADD'T FEE	
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY		OR
	Total (37 CFR 1.16(i))	*	Minus **	=	RATE (\$)	ADDITIONAL FEE (\$)
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X =	X =
	Application Size Fee (37 CFR 1.16(s))			X =	X =	X =
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			N/A	N/A	N/A
			TOTAL		TOTAL	
			ADD'T FEE		ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/323,461	11/25/2008	2189	982	6005.007CIP	40	3

CONFIRMATION NO. 7802

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FILING RECEIPT



OC000000033532314

Date Mailed: 12/10/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

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Assignment For Published Patent Application

BITMICRO NETWORKS, INC., Fremont, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 11/450,005 06/08/2006 *
and is a CIP of 11/450,023 06/08/2006 *

(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications

If Required, Foreign Filing License Granted: 12/09/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/323,461**

Projected Publication Date: 03/19/2009

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	)	Group Art Unit: 2189
	)	
Serial No.: 12/323,461	)	Examiner: Not Yet Assigned
	)	
Filed: 25 Nov 2008	)	
	)	
For: OPTIMIZING MEMORY OPERATIONS	)	
IN AN ELECTRONIC STORAGE DEVICE	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Examiner:

Please amend this Application as follows and consider the remarks set forth below.

The section entitled, "**Specification Amendments**" begins on page 2.

The section entitled, **Remarks** begins on page 3 of this paper.

Specification Amendments:

Please amend the Specification as follows.

In the Cross-Reference to Related Applications section, on page 1, please replace paragraph [001] with the following paragraph:

[001] This application is a continuation in part application and claims the benefit of United States patent application, entitled "Optimized Placement Policy for Solid State Storage Devices, filed on 8 June 2006, and having Serial No.: 11/450,005 and attorney docket number 6005.007, ~~and of United States patent application, entitled "Hybrid Multi-Tiered Caching Storage Systems", filed on 8 June 2006, and having Serial No.: 11/450,023 and attorney docket number 6005.006,~~ which are is hereby incorporated by reference herein as if fully set forth herein.

On page 8, please replace paragraph [0015] with the following paragraph:

[0015] In another example, DMA controller 10 may be implemented in the form of Flash DMA controller 109, which is part of hybrid storage controller 102, which are further disclosed in FIG. 1 of United States patent application, entitled "Hybrid Multi-Tiered Caching Storage System[[s]]", filed on 8 June 2006, and having Serial No.: 11/450,023 and attorney docket number 6005.006, which is hereby incorporated by reference as if fully set forth herein.

Remarks

The Specification has been amended to further particularly point out and distinctly claim subject matter regarded as the invention. The application has been amended to claim priority to a single parent application in which a common inventor is shared. The removal of the claim of priority for United States patent application, entitled "Hybrid Multi-Tiered Caching Storage Systems", filed on 8 June 2006, and having Serial No.: 11/450,023 and attorney docket number 6005.006, named "Other Application", does not preclude this application from complying with 35 U.S.C. Section 112.

The Specification has also been amended so that the incorporation by reference of the Other Application is perfected in compliance with 37 CFR 1.57(g) and MPEP 608.01(p).

The above amendments are not made to avoid the prior art and do not add "new matter".

Request for Allowance

It is believed that this Amendment places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 29 December 2008

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

The Uriarte Law Firm
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San Jose, CA 95126
Tel: 408.876.4470
Fax: 408.716.2651

Supplemental Application Data Sheet

Application Information

Title line One:: OPTIMIZING MEMORY OPERATIONS IN AN

Title Line Two:: ELECTRONIC STORAGE DEVICE

Application Number:: 12/323,461

Filing Date:: 11/25/08

Application Type:: Nonprovisional

Subject Matter:: Utility

Suggested classification::

Suggested Group Art Unit:: 2189

CD-ROM or CD-R?: None

Attorney Docket Number:: 6005.007CIP

Request for Early Publication?: No

Request for Non-Publication?: No

Suggested Drawing Figure:: 2

Total Drawing Sheets:: 2

Small Entity:: Yes

Petition included?: No

Petition Type::

Licensed US Govt. Agency::

Contract or Grant Numbers::

Secrecy Order in Parent Appl.?:: No

Applicant Information

Applicant Authority type:: Inventor
Primary Citizenship Country:: PH
Status:: Full Capacity
Inventor One Given Name:: Mark
Middle Initial:: I.
Family Name:: ARCEDERA
City of Residence:: Paranaque City
Country of Residence:: PH
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Sucat
City of mailing address:: Paranaque City
Postal or Zip Code of mailing address:: 1700

Applicant Authority type:: Inventor
Primary Citizenship Country:: PH
Status:: Full Capacity
Inventor Two Given Name:: Ritchie
Middle Initial::

Family Name:: BABAYLAN
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Subd.
Country of Residence:: PH
Street of mailing address:: 122 Kiamzon St., Phase XI-B Bahayang Pag-Asa
Subd.
Imus
City of mailing address:: Cavite
Postal or Zip Code of mailing address:: 4103

Applicant Authority type:: Inventor
Primary Citizenship Country:: PH
Status:: Full Capacity
Inventor Three Given Name:: Reyjan
Middle Initial::
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Phone number:: 408.244.2164 x111

Fax number:: 408.716.2651

E-Mail address:: info@uriartelaw.com

Representative Information

Representative Customer Number::	64180	
----------------------------------	-------	--

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
<u>This application is a</u>	Continuation in part of	11450005	[[2006-06-06]] <u>2006-06-08</u>
	Continuation in part of	11450023	[[2006-06-06]]

Foreign Priority Information

Country::	Application number::	Filing Date::	Priority Claimed::
			[[Yes]] <u>No</u>

Assignee Information

Assignee name:: BiTMICRO Networks, Inc.
Street of mailing address:: 47929 Fremont Blvd
City of mailing address:: Fremont
State or Province of mailing address:: CA
Country of mailing:: US
Postal or Zip Code of mailing address:: 94538

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	12/323,461	
	Filing Date	25 November 2008	
	First Named Inventor	ARCEDERA, Mark	
	Art Unit	2189	
	Examiner Name	Not Yet Assigned	
Total Number of Pages in This Submission	10	Attorney Docket Number	6005.007CIP

ENCLOSURES (Check all that apply)		
☐ Fee Transmittal Form ☐ Fee Attached ☐ Amendment/Reply ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/ Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): Preliminary Amendment (3 sheets) and Suppl. ADS (5 sheets).
<div>Remarks</div>		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	The Uriarte Law Firm		
Signature	/Stephen R. Uriarte/		
Printed name	Stephen R. Uriarte		
Date	30 December 2008	Reg. No.	40,854

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:			
Signature			
Typed or printed name		Date	

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	4540333
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	30-DEC-2008
Filing Date:	25-NOV-2008
Time Stamp:	19:53:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	6005_007CIP_PrelimAmd_Xref_Incorp_20081229.pdf	61659 b8b0530f5f9213a501cf76e18cd4729fe4930c7b	no	3

Warnings:

Information:

2	Application Data Sheet	6005_007CIP_SuppADS_20081229.pdf	55082 9efb3ddaa3922bfa3f12248f22ef65364786d9e7	no	5
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3	Miscellaneous Incoming Letter	6005_007CIP_TL_20081230.pdf	231876 b9817a686fb004bd30aaf197408266955e0ed21f	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			348617		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12323461
	Filing Date	2008-11-25
	First Named Inventor	Mark ARCEDERA
	Art Unit	2189
	Examiner Name	Not Yet Assigned
	Attorney Docket Number	6005.007CIP

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	2	20030217202	A1	2003-11-20	ZILBERMAN et al.	See ISR & WO (Entire Doc; abstract, para. 10, 22, 59, 60, 66, 112, 113)		
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		12323461
	Filing Date		2008-11-25
	First Named Inventor	Mark ARCEDERA	
	Art Unit	2189	
	Examiner Name	Not Yet Assigned	
	Attorney Docket Number	6005.007CIP	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Lee W. YOUNG, PCT/US07/70660 International Search Report (ISR), 18 Nov 2008, p. 2, International Searching Authority/US, Alexandria, Virginia	☐
	2	Lee W. YOUNG, PCT/US07/70660 Written Opinion (WO), 18 Nov 2008, Box V and Supplemental Box, International Searching Authority/US, Alexandria, Virginia	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12323461
	Filing Date	2008-11-25
	First Named Inventor	Mark ARCEDERA
	Art Unit	2189
	Examiner Name	Not Yet Assigned
	Attorney Docket Number	6005.007CIP

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Stephen R. Uriarte/	Date (YYYY-MM-DD)	2009-01-27
Name/Print	Stephen R. Uriarte	Registration Number	40,854

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	4687460
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	27-JAN-2009
Filing Date:	25-NOV-2008
Time Stamp:	21:09:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	6005_007CIP_IDS_1st_20090127_Acr9.pdf	609490 b39c0a2a0133355fc5856b1540cff35807daf66	no	4

Warnings:

Information:

2	NPL Documents	6005_007PCT_ISA.pdf	104012 4745beb89053ff40db494f0043603229d6981798	no	2
Warnings:					
Information:					
3	NPL Documents	6005_007PCT_WO.pdf	192753 f5044fc035413fc503d0156c381b0753d3d0744d	no	4
Warnings:					
Information:					
Total Files Size (in bytes):			906255		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP

CONFIRMATION NO. 7802

64180
URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051

PUBLICATION NOTICE



Title:OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Publication No.US-2009-0077306-A1

Publication Date:03/19/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802
64180	7590	10/25/2010	EXAMINER	
URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126			FARROKH, HASHEM	
			ART UNIT	PAPER NUMBER
			2187	
			NOTIFICATION DATE	DELIVERY MODE
			10/25/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com

Office Action Summary	Application No.	Applicant(s)	
	12/323,461	ARCEDERA ET AL.	
	Examiner	Art Unit	
	HASHEM FARROKH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 25 November 2008.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-40 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-40 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 25 November 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 01/27/09.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

The instant application having application No. 12/323,461 has a total of 40 claims pending in the application; there are 3 independent claim and 37 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING IDS:

The information disclosure statement (IDS) submitted on 01/27/09 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

1. *Lines 16-18 of the independent claim1 recite the limitation(s): "...said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA..." The*

specification does not describe how the mapping table causes the storage device to perform optimized memory operation on memory location in such a way that is understood by one having ordinary skill in the related art. The independent claims 22 and 32 recite a similar limitation(s) and are rejected based on the same ground of rejection. The dependent claims 2-21, 23-31, and 33-40 are rejected under 35 U.S.C. 112, first paragraph, by virtue of their dependency from their respected independent claims.

Conclusion

The prior art made of record and not relied upon are as follows:

- 1. U. S. Patent Publication No. 2009/0300318 A1 to Allen et al. describes ADDRESS CACHING STORED TRANSLATION.*
- 2. U. S. Patent Publication No. 2005/0114587 A1 to Chou et al. describes ExpressCard with On-Card Flash Memory with Shared Flash-Control Bus but Separate Ready Lines.*
- 3. U. S. Patent Publication No. 2003/0217202 A1 to Zilberman et al. describes Method for improving performance of a flash-based storage system using specialized flash controllers.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin L. Ellis can be reached on (571)272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*/Hashem Farrokh/
Examiner, Art Unit 2187*

Notice of References Cited	Application/Control No. 12/323,461	Applicant(s)/Patent Under Reexamination ARCEDERA ET AL.	
	Examiner HASHEM FARROKH	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0300318	12-2009	Allen et al.	711/206
*	B	US-2005/0114587 A1	05-2005	Chou et al.	711/103
*	C	US-2003/0217202 A1	11-2003	Zilberman et al.	710/22
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 12323461	Applicant(s)/Patent Under Reexamination ARCEDERA ET AL.
	Examiner HASHEM FARROKH	Art Unit 2187

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
PALM and EAST Inventor Search Conducted	10/19/2010	HF
EAST Text Search	10/19/2010	HF
IEEE Xplore Search Conducted	10/19/2010	HF
ACM Digital Library Search Conducted	10/19/2010	HF

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 12323461	Applicant(s)/Patent Under Reexamination ARCEDERA ET AL.
	Examiner HASHEM FARROKH	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	10/19/2010									
	1	✓									
	2	✓									
	3	✓									
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	33	✓									
	34	✓									
	35	✓									
	36	✓									

<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 12323461	Applicant(s)/Patent Under Reexamination ARCEDERA ET AL.
	Examiner HASHEM FARROKH	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	10/19/2010								
	37	✓								
	38	✓								
	39	✓								
	40	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(map\$4 or translat\$3 or conver\$4) near5 (((logical adj address) or LBA) near2 (set or group or cluster)) near5 (access\$3 near2 parameter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 21:58
L5	42	(map\$4 or translat\$3 or conver\$4) near5 (((logical adj address) or LBA) near2 (set or group or cluster)) near5 (((physical adj address) or PBA) near2 (set or group or cluster))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 22:04
L6	39	5 and (@ad<"20081125")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 22:04
L7	2	6 and (access\$3 near2 parameter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 22:04
L8	2	(((physical adj address) or PBA) near2 (set or group or cluster)) near5 (access\$3 near2 parameter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 22:18
S4	2	"20090077306"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 12:04
S5	7	"7613876"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 13:05

S6	6	"7506098"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 13:12
S7	4	"20050114587" "20030217202"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 13:36
S8	1	"12575480"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 14:09
S9	1	ARCEDERA-Mark-Ian.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 14:19
S10	3	BABAYLAN-Ritchie.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 14:20
S11	2	LANUZA-Reyjan.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 14:21
S12	1	((logical adj field) with ((logical adj block adj address) or LBA)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 14:42
S13	2	((logical adj field) with ((logical adj block adj address) or LBA))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 14:43

S14	1	((logical adj field) with ((logical adj block adj address) or LBA)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 14:43
S15	868	((logical adj block adj address) or LBA) near2 (set or group or cluster)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 14:46
S16	229	S15 and ((physical adj block adj address) or PBA)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 14:50
S17	6	((physical adj block adj address) or PBA) near3 (represent\$3 or identify\$3) near3 parameter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 14:51
S18	142	((physical adj block adj address) or PBA) near3 parameter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 14:52
S19	135	S18 and (@ad<"20081125")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 14:56
S20	10	S19 and "711"/\$.cls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 14:56
S21	1	S19 and "710"/\$.cls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 15:02

S22	1	S19 and "707"/\$.ocls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 15:03
S23	1	S19 and "709"/\$.ocls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/10/19 15:03
S24	1	(map\$4 or translat\$3 or conver\$4) with (((logical adj block adj address) or LBA) near2 (set or group or cluster)) with parameters	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 15:11
S25	125	(map\$4 or translat\$3 or conver\$4) with (((logical adj block adj address) or LBA) near2 (set or group or cluster))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 15:12
S26	142	((physical adj block adj address) or PBA) near3 parameter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 16:01
S27	3	((physical adj block adj address) or PBA) near3 (access\$3 near2 (parameter or characteristic or attribute))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 16:03
S28	32	((physical adj block adj address) or PBA) near3 (characteristic or attribute)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/19 16:05

10/19/2010 10:24:55 PM

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12323461
	Filing Date	2008-11-25
	First Named Inventor	Mark ARCEDERA
	Art Unit	2100 2187
	Examiner Name	Not Yet Assigned Hashem Farrokh
	Attorney Docket Number	6005.007CIP

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20050114587	A1	2005-05-26	CHOU et al.	See ISR & WO (Entire Doc; abstract, para. 27, 31-33, 38)		
	2	20030217202	A1	2003-11-20	ZILBERMAN et al.	See ISR & WO (Entire Doc; abstract, para. 10, 22, 59, 60, 66, 112, 113)		
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		12323461
	Filing Date		2008-11-25
	First Named Inventor	Mark ARCEDERA	
	Art Unit	2186 2187	
	Examiner Name	Not Yet Assigned Hashem Farrokh	
	Attorney Docket Number	6005.007CIP	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Lee W. YOUNG, PCT/US07/70660 International Search Report (ISR), 18 Nov 2008, p. 2, International Searching Authority/US, Alexandria, Virginia	☐
	2	Lee W. YOUNG, PCT/US07/70660 Written Opinion (WO), 18 Nov 2008, Box V and Supplemental Box, International Searching Authority/US, Alexandria, Virginia	☐

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EXAMINER SIGNATURE

Examiner Signature	/Hashem Farrokh/	Date Considered	10/19/2010
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	)	Group Art Unit: 2187
	)	
Serial No.: 12/323,461	)	Examiner: FARROKH, Hashem
	)	
Filed: 25 Nov 2008	)	
	)	
For: OPTIMIZING MEMORY OPERATIONS	)	
IN AN ELECTRONIC STORAGE DEVICE	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT TO FIRST OFFICE ACTION

Dear Examiner:

In response to the Office Action, mailed 25 Oct 2010, kindly amend this Application as follows and consider the remarks set forth below.

Amendments to the specification begin on page **2**;

A listing of original, amended and new claims begin on page **4**; and

Remarks begin on page **17** of this paper.

Amendment(s) to the Specification

In the Specification, please enter the amendments shown with respect to the replacement paragraphs identified below. Text in underline indicates new text, while text in strike-out format or between a pair of double brackets indicates deletion of text. No new matter has been added.

Please replace paragraph **[003]** on page 2 with the following replacement paragraph.

[0003] Electronic storage devices that respectively employ a memory system that includes memory devices, memory chips, or modules that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices. The computer device industry has increased the adoption of these solid state storage devices due to certain advantages offered by these types of storage devices over other forms of storage devices, such as rotational drives. The adoption of solid state storage devices as an enhancement or even as ~~replacements~~ ~~replacement~~ to rotational drives is not without some difficulty because many conventional computer devices, sometimes referred to as "hosts", use host operating systems, file systems, or both that are optimized for use with rotational drives rather than solid state storage devices. For example, unlike rotational drives, solid state storage devices that use NAND flash memory, also referred to as "flash drives", suffer from write cycle limitations and to a certain degree, bad blocks. In addition, flash drives use block addressing rather than byte addressing, and these flash drives use block addresses that are usually much larger than the block address used by the host. Block addressing may impose an

additional level of complexity and additional processing cycles when performing a write operation, and which in turn, may increase write operation latency. This additional level of complexity may include performing a read-modify-write transaction to complete the write operation.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (ORIGINAL) A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA

and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

2. (ORIGINAL) The mapping table of claim 1, wherein:

said first and second LBA sets are adjacent LBA sets;

said first and second access parameters are different; and

said LBAs from said first and second LBA sets are logical block addresses used by the host for addressing said data.

3. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

4. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is not consecutive with an LBA having the highest LBA value from said first LBA set.

5. (ORIGINAL) The mapping table of claim 1, wherein:

data stored at a first physical memory location, which is addressable using said first PBA, is transferred to a second physical memory location, which is addressable using said second PBA, said data transferred in portions equal to a section size.

6. (ORIGINAL) The mapping table of claim 5, wherein:

said first and second LBA sets respectively have an LBA set size equal to said section size.

7. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

8. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that supports more than one page write that can be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said one of said flash blocks; and

said section size is at least equal to a quotient resulting from dividing said native page size by said more than one page write.

9. (ORIGINAL) The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier.

10. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.

11. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers.

12. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different bus identifiers.

13. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different FDE identifiers.

14. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBAs respectively include a first group identifier and a second group identifier.

15. (ORIGINAL) The mapping table of claim 1:

wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and

wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs.

16. (ORIGINAL) The mapping table of claim 1, wherein:

said memory store includes a first set of memory devices controlled by a first FDE and a second set of memory devices controlled by a second FDE;
and

said first and second sets of memory devices associated with a plurality of group identifiers in which no two of said group identifiers is the same, and each memory device from said first set of memory devices is respectively associated with different group identifiers from said plurality of group identifiers.

17. (ORIGINAL) The mapping table of claim 1, wherein:

said electronic storage device includes a storage device controller, said memory store, and a memory system;

said memory system includes a flash buffer controller, a first set of FDEs, a second set of FDEs, and a set of buses that includes a first bus and a second bus;

said memory store includes a first set of memory devices and a second set of memory devices, said first and second set of memory devices respectively coupled to said first and second buses;

said first set of FDEs disposed to control said first set of memory devices through said flash buffer controller and said first bus, said first set of FDEs including a first FDE and a second FDE;

said second set of FDEs disposed to control said second set of memory devices through said flash buffer controller and said second bus, said second set of FDEs including a third FDE and a fourth FDE;

said first and second set of memory devices are associated with a plurality of memory device groups, including a first group and a second group;

wherein said first and second groups corresponding respectively to said first and second group identifiers; and

wherein said first and second PBAs respectively include said first and second group identifiers.

18. (ORIGINAL) The mapping table of claim 17, wherein said first and third memory devices are associated with a first group identifier and said second and fourth memory devices are associated with a second group identifier.

19. (ORIGINAL) The mapping table of claim 17, wherein said first and second memory devices include non-volatile solid state memory cells.

20. (ORIGINAL) The mapping table of claim 17, wherein each memory device from said first set of memory devices are respectively associated with different group identifiers.

21. (ORIGINAL) The mapping table of claim 1, wherein said first PBA further disposed to represent a memory index.

22. (ORIGINAL) A memory system for optimizing memory operations in an electronic storage device responsive to an I/O transaction request initiated by a host, said electronic storage device including a memory store having a set of memory devices including a first memory device, a second memory device, a third memory device and a fourth memory device, said memory system comprising:

a flash buffer controller, a set of FDEs, and a set of buses, wherein said set of FDEs including a first FDE, a second FDE, a third FDE, and a fourth FDE and wherein said buses including a first bus and a second bus, said first bus coupled to the first and second memory devices, and the second bus coupled to said third and fourth memory devices;

said first and second FDEs coupled to said first bus through said first buffer controller, and said third and fourth FDEs coupled to said second bus through said first buffer controller;

said set of memory devices are partitioned into memory device groups, including a first group and a second group;

a mapping table that includes:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for holding a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.

23. (ORIGINAL) The memory system of claim 22, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

24. (ORIGINAL) The memory system of claim 22, wherein said first and third memory devices correspond to a first group identifier and said second and fourth memory devices correspond to a second group identifier.

25. (ORIGINAL) The memory system of claim 22, wherein said optimized memory operations include a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

26. (ORIGINAL) The memory system of claim 25, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier and a group identifier.

27. (ORIGINAL) The memory system of claim 26, wherein said first and second PBAs respectively include said first and second group identifiers.

28. (ORIGINAL) The memory system of claim 22, wherein said PBA further includes a memory index.

29. (ORIGINAL) The memory system of claim 22, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

30. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

31. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

32. (ORIGINAL) An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:

a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;

a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;

a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;

wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs; and

wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of

the I/O transaction request will be optimally distributed across storage device resources.

33. (ORIGINAL) The electronic storage device of claim 32, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

34. (ORIGINAL) The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

35. (ORIGINAL) The memory system of claim 34, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier, and a group identifier.

36. (ORIGINAL) The memory system of claim 35, wherein said first and second PBAs respectively include said first and second group identifiers.

37. (ORIGINAL) The electronic storage device of claim 32, wherein said PBA further includes a memory index.

38. (ORIGINAL) The electronic storage device of claim 32, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

39. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

40. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

Remarks

The specification has been amended to correct minor errors, improve readability, or otherwise. These corrections are of a clerical nature and do not add "new matter".

The First Paragraph Section 112 Rejection

The Examiner rejects claims 1-40 under 35 USC §112, first paragraph, as allegedly failing to comply with the written description requirement. More particularly, the Examiner asserts that the "specification does not describe how the mapping table causes the storage device to perform optimized memory operations on a memory location". Applicants respectfully traverse this rejection because the Specification describes embodiment(s) of the present invention in a manner that allows one of ordinary skill in the art how to make and use without undue experimentation the invention as claimed. See, MPEP 2164.01.

Independent Claims 1, 22 and 32 Meet the Statutory Requirements

Claim 1

Claim 1 recites in part:

"wherein, in response to receiving the I/O transaction request, said mapping table **causes** the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets." (Emphasis Added.)

The above limitation in claim 1 is supported by the Specification because the Specification teaches how a “mapping table” causes a “storage device to perform optimized memory operations”. For example, paragraphs [0023]-[0025], [0034], and [0036] (see also, FIGS. 1-2) disclose a mapping table, that when used by a storage device, **causes** the storage device to perform optimized memory operations.

“[0023] In FIG. 2, mapping table 9 reflects the embodiment disclosed in FIG. 1. PBA 46 and PBA 50 include access parameters that are associated with the same group identifier of 15-0 but pertain to physical memory locations within different flash memory devices in memory store 6. ***These access parameters are associated with different FDE identifiers, such as FDE identifiers 22-01 and 22-11 and with different bus identifiers 8-0 and 8-1, respectively.*** (Emphasis added.) Using their respective access parameters, PBA 46 is associated with a physical memory location that is within a flash memory device 12-01 coupled to bus 8-0, controlled by FDE 22-01, and in group 15-0, while PBA 50 is associated with another physical memory location that is within a flash memory device 12-01 coupled to bus 8-1, controlled by FDE 22-11, and in group 15-0 in FIG. 1.

[0024] The term “LBA”, which may also be referred to herein as a logical block address, is intended to represent an address that is part of a logical addressing system (not shown) used by a host, such as host 18, and this host may use one or more LBAs in an I/O transaction request, such as I/O transaction request 20. Mapping table 9 associates LBAs from this host logical addressing system to the device addressing system used by storage

device 2. This device addressing system may include using a mapping table that includes the functionality described herein, such as mapping table 9. These LBAs may be grouped into ***sets of consecutive LBAs, named "LBA sets"***. (Emphasis added.) These LBA sets may then be represented using logical fields 26 from mapping table 9, where each logical field in set of logical fields 26 is respectively disposed to represent a LBA set. For example, LBA sets 40, 42, 44, and 45 may be used to respectively represent consecutive LBAs used by host 18, such as LBAs 00 through 07, LBAs 08 through 15, LBAs 16 through 23, and LBAs 24-31, respectively.

[0025] *Logical fields in mapping table 9 may be initialized to represent LBA sets that are serially arranged in mapping table 9 so that LBAs from adjacent LBA sets are contiguous.* (Emphasis added.)

In the example shown in FIG. 2, LBA sets 40, 42, 44 and 45 represent serially arranged LBAs since the highest LBA in one LBA set is contiguous with the lowest LBA in an adjacent LBA set. Specifically, LBA sets 40 and 42 are disposed in adjacent rows and thus are adjacent to each other. These adjacent LBA sets are also contiguous because LBA 7, which corresponds to the highest LBA in LBA set 40, is contiguous with LBA 8, which is the lowest LBA in LBA set 42. Similarly, LBA sets 42 and 44 are also contiguous because LBA 15, which corresponds to the highest LBA in LBA set 42, is contiguous with LBA 16, which is the lowest LBA in LBA set 44. LBA set 44 is also contiguous with LBA set 45.

[0034] During operation and after initialization of mapping table 9, if storage device controller 22 receives an I/O transaction request 20 from host 18, *storage device controller 22 processes I/O transaction request by*

transferring it to DMA controller 10. After receiving I/O transaction request 20, DMA controller 10 uses mapping table 9 to determine which PBAs are mapped to LBAs used in I/O transaction request 20. DMA controller 10 uses the PBAs to determine which addressable physical memory locations to use when performing memory operations requested by host 18 through I/O transaction request 20.

Mapping table 9 associates LBA sets to PBAs in a manner that increases the likelihood *that memory operations resulting from I/O transaction request 20 will be **optimized by distributing these memory operations across different storage device resources that are associated with these PBAs**, such as across **different FDEs, different buses, different flash** memory devices, or **any combination of these**.* (Emphasis added.)

[0036] Using different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9, enables the ***interleaving*** of memory operations across flash devices that are controlled by the same FDE. (Emphasis added.) Stated another way, using different group identifiers enables interleaving memory operations across flash devices that belong to the same flash array bank interleave. Using different FDE identifiers in mapping table 9 enables interleaving memory operations across flash memory devices that are controlled by different FDEs, while using different bus identifiers enables interleaving memory operations across flash memory devices that are coupled to different flash bus interfaces.”

Thus, by the example discussed above, the Specification describes “how the mapping table causes the storage device to perform optimized memory operations” (See, Office Action) in a manner that meets the requirements in Section 112, first

paragraph, rendering claim 1 and its respective dependent claims statutory.

Claim 22

Claim 22 recites in part:

“wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.”

The above limitation in claim 22 is also supported by the Specification because the Specification teaches how a “mapping table” causes a “storage device to perform optimized memory operations”. See, Specification at paragraphs [0023]-[0025], [0034], and [0036] and FIGS. 1-2. Thus, claim 22 also meets the requirements in 35 USC Section 112, first paragraph, rendering claim 22 and its respective dependent claims statutory.

Claim 32

Claim 32 recites in part:

“wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.”

The above limitation in claim 32 is supported by the Specification because the

Specification teaches how a “mapping table increases the likelihood that the operational load imposed on the storage apparatus”...“will be optimally distributed across storage device resources” as recited in claim 32. See for example, paragraphs [0034] and [0036] (see also, FIGS. 1-2) which disclose the following:

“[0034] During operation and after initialization of mapping table 9, if storage device controller 22 receives an I/O transaction request 20 from host 18, storage device controller 22 processes I/O transaction request by transferring it to DMA controller 10. *After receiving I/O transaction request 20, DMA controller 10 **uses mapping table 9 to determine which PBAs are mapped to LBAs used in I/O transaction request 20.** DMA controller 10 uses the PBAs to determine which addressable physical memory locations to use when performing memory operations requested by host 18 through I/O transaction request 20. Mapping table 9 associates LBA sets to PBAs in a manner that **increases the likelihood that memory operations resulting from I/O transaction request 20 will be optimized by distributing these memory operations across different storage device resources that are associated with these PBAs,** such as across **different FDEs, different buses, different flash** memory devices, or **any combination of these.** (Emphasis added.)*

[0036] Using different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9, **enables the *interleaving*** of memory operations across flash devices that are controlled by the same FDE. Stated another way, using different group identifiers enables interleaving memory operations across flash devices that belong to the same flash array bank interleave. Using different FDE identifiers in mapping table 9 enables interleaving

memory operations across flash memory devices that are controlled by different FDEs, while using different bus identifiers enables interleaving memory operations across flash memory devices that are coupled to different flash bus interfaces. (Emphasis added.)”

Thus, claim 32 also meets the requirements in 35 USC Section 112, first paragraph, rendering claim 32 and its respective dependent claims statutory.

Request for Allowance

It is believed that this Response places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 25 February 2011

/Stephen R. Uriarte/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	)	Group Art Unit: 2187
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Serial No.: 12/323,461	)	Examiner: FARROKH, Hashem
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Filed: 25 Nov 2008	)	
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IN AN ELECTRONIC STORAGE DEVICE	)	
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Commissioner for Patents
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[0003] Electronic storage devices that respectively employ a memory system that includes memory devices, memory chips, or modules that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices. The computer device industry has increased the adoption of these solid state storage devices due to certain advantages offered by these types of storage devices over other forms of storage devices, such as rotational drives. The adoption of solid state storage devices as an enhancement or even as ~~replacements~~ ~~replacement~~ to rotational drives is not without some difficulty because many conventional computer devices, sometimes referred to as "hosts", use host operating systems, file systems, or both that are optimized for use with rotational drives rather than solid state storage devices. For example, unlike rotational drives, solid state storage devices that use NAND flash memory, also referred to as "flash drives", suffer from write cycle limitations and to a certain degree, bad blocks. In addition, flash drives use block addressing rather than byte addressing, and these flash drives use block addresses that are usually much larger than the block address used by the host. Block addressing may impose an

additional level of complexity and additional processing cycles when performing a write operation, and which in turn, may increase write operation latency. This additional level of complexity may include performing a read-modify-write transaction to complete the write operation.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (ORIGINAL) A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA

and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

2. (ORIGINAL) The mapping table of claim 1, wherein:

said first and second LBA sets are adjacent LBA sets;

said first and second access parameters are different; and

said LBAs from said first and second LBA sets are logical block addresses used by the host for addressing said data.

3. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

4. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is not consecutive with an LBA having the highest LBA value from said first LBA set.

5. (ORIGINAL) The mapping table of claim 1, wherein:

data stored at a first physical memory location, which is addressable using said first PBA, is transferred to a second physical memory location, which is addressable using said second PBA, said data transferred in portions equal to a section size.

6. (ORIGINAL) The mapping table of claim 5, wherein:

said first and second LBA sets respectively have an LBA set size equal to said section size.

7. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

8. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that supports more than one page write that can be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said one of said flash blocks; and

said section size is at least equal to a quotient resulting from dividing said native page size by said more than one page write.

9. (ORIGINAL) The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier.

10. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.

11. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers.

12. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different bus identifiers.

13. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different FDE identifiers.

14. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBAs respectively include a first group identifier and a second group identifier.

15. (ORIGINAL) The mapping table of claim 1:

wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and

wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs.

16. (ORIGINAL) The mapping table of claim 1, wherein:

said memory store includes a first set of memory devices controlled by a first FDE and a second set of memory devices controlled by a second FDE;
and

said first and second sets of memory devices associated with a plurality of group identifiers in which no two of said group identifiers is the same, and each memory device from said first set of memory devices is respectively associated with different group identifiers from said plurality of group identifiers.

17. (ORIGINAL) The mapping table of claim 1, wherein:

said electronic storage device includes a storage device controller, said memory store, and a memory system;

said memory system includes a flash buffer controller, a first set of FDEs, a second set of FDEs, and a set of buses that includes a first bus and a second bus;

said memory store includes a first set of memory devices and a second set of memory devices, said first and second set of memory devices respectively coupled to said first and second buses;

said first set of FDEs disposed to control said first set of memory devices through said flash buffer controller and said first bus, said first set of FDEs including a first FDE and a second FDE;

said second set of FDEs disposed to control said second set of memory devices through said flash buffer controller and said second bus, said second set of FDEs including a third FDE and a fourth FDE;

said first and second set of memory devices are associated with a plurality of memory device groups, including a first group and a second group;

wherein said first and second groups corresponding respectively to said first and second group identifiers; and

wherein said first and second PBAs respectively include said first and second group identifiers.

18. (ORIGINAL) The mapping table of claim 17, wherein said first and third memory devices are associated with a first group identifier and said second and fourth memory devices are associated with a second group identifier.

19. (ORIGINAL) The mapping table of claim 17, wherein said first and second memory devices include non-volatile solid state memory cells.

20. (ORIGINAL) The mapping table of claim 17, wherein each memory device from said first set of memory devices are respectively associated with different group identifiers.

21. (ORIGINAL) The mapping table of claim 1, wherein said first PBA further disposed to represent a memory index.

22. (ORIGINAL) A memory system for optimizing memory operations in an electronic storage device responsive to an I/O transaction request initiated by a host, said electronic storage device including a memory store having a set of memory devices including a first memory device, a second memory device, a third memory device and a fourth memory device, said memory system comprising:

a flash buffer controller, a set of FDEs, and a set of buses, wherein said set of FDEs including a first FDE, a second FDE, a third FDE, and a fourth FDE and wherein said buses including a first bus and a second bus, said first bus coupled to the first and second memory devices, and the second bus coupled to said third and fourth memory devices;

said first and second FDEs coupled to said first bus through said first buffer controller, and said third and fourth FDEs coupled to said second bus through said first buffer controller;

said set of memory devices are partitioned into memory device groups, including a first group and a second group;

a mapping table that includes:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for holding a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.

23. (ORIGINAL) The memory system of claim 22, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

24. (ORIGINAL) The memory system of claim 22, wherein said first and third memory devices correspond to a first group identifier and said second and fourth memory devices correspond to a second group identifier.

25. (ORIGINAL) The memory system of claim 22, wherein said optimized memory operations include a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

26. (ORIGINAL) The memory system of claim 25, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier and a group identifier.

27. (ORIGINAL) The memory system of claim 26, wherein said first and second PBAs respectively include said first and second group identifiers.

28. (ORIGINAL) The memory system of claim 22, wherein said PBA further includes a memory index.

29. (ORIGINAL) The memory system of claim 22, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

30. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

31. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

32. (ORIGINAL) An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:

a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;

a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;

a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;

wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs; and

wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of

the I/O transaction request will be optimally distributed across storage device resources.

33. (ORIGINAL) The electronic storage device of claim 32, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

34. (ORIGINAL) The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

35. (ORIGINAL) The memory system of claim 34, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier, and a group identifier.

36. (ORIGINAL) The memory system of claim 35, wherein said first and second PBAs respectively include said first and second group identifiers.

37. (ORIGINAL) The electronic storage device of claim 32, wherein said PBA further includes a memory index.

38. (ORIGINAL) The electronic storage device of claim 32, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

39. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

40. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

Remarks

The specification has been amended to correct minor errors, improve readability, or otherwise. These corrections are of a clerical nature and do not add "new matter".

The First Paragraph Section 112 Rejection

The Examiner rejects claims 1-40 under 35 USC §112, first paragraph, as allegedly failing to comply with the written description requirement. More particularly, the Examiner asserts that the "specification does not describe how the mapping table causes the storage device to perform optimized memory operations on a memory location". Applicants respectfully traverse this rejection because the Specification describes embodiment(s) of the present invention in a manner that allows one of ordinary skill in the art how to make and use without undue experimentation the invention as claimed. See, MPEP 2164.01.

Independent Claims 1, 22 and 32 Meet the Statutory Requirements

Claim 1

Claim 1 recites in part:

"wherein, in response to receiving the I/O transaction request, said mapping table **causes** the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets." (Emphasis Added.)

The above limitation in claim 1 is supported by the Specification because the Specification teaches how a “mapping table” causes a “storage device to perform optimized memory operations”. For example, paragraphs [0023]-[0025], [0034], and [0036] (see also, FIGS. 1-2) disclose a mapping table, that when used by a storage device, **causes** the storage device to perform optimized memory operations.

“[0023] In FIG. 2, mapping table 9 reflects the embodiment disclosed in FIG. 1. PBA 46 and PBA 50 include access parameters that are associated with the same group identifier of 15-0 but pertain to physical memory locations within different flash memory devices in memory store 6. **These access parameters are associated with different FDE identifiers, such as FDE identifiers 22-01 and 22-11 and with different bus identifiers 8-0 and 8-1, respectively.** (Emphasis added.) Using their respective access parameters, PBA 46 is associated with a physical memory location that is within a flash memory device 12-01 coupled to bus 8-0, controlled by FDE 22-01, and in group 15-0, while PBA 50 is associated with another physical memory location that is within a flash memory device 12-01 coupled to bus 8-1, controlled by FDE 22-11, and in group 15-0 in FIG. 1.

[0024] The term “LBA”, which may also be referred to herein as a logical block address, is intended to represent an address that is part of a logical addressing system (not shown) used by a host, such as host 18, and this host may use one or more LBAs in an I/O transaction request, such as I/O transaction request 20. Mapping table 9 associates LBAs from this host logical addressing system to the device addressing system used by storage

device 2. This device addressing system may include using a mapping table that includes the functionality described herein, such as mapping table 9. These LBAs may be grouped into ***sets of consecutive LBAs, named "LBA sets"***. (Emphasis added.) These LBA sets may then be represented using logical fields 26 from mapping table 9, where each logical field in set of logical fields 26 is respectively disposed to represent a LBA set. For example, LBA sets 40, 42, 44, and 45 may be used to respectively represent consecutive LBAs used by host 18, such as LBAs 00 through 07, LBAs 08 through 15, LBAs 16 through 23, and LBAs 24-31, respectively.

[0025] *Logical fields in mapping table 9 may be initialized to represent LBA sets that are serially arranged in mapping table 9 so that LBAs from adjacent LBA sets are contiguous.* (Emphasis added.)

In the example shown in FIG. 2, LBA sets 40, 42, 44 and 45 represent serially arranged LBAs since the highest LBA in one LBA set is contiguous with the lowest LBA in an adjacent LBA set. Specifically, LBA sets 40 and 42 are disposed in adjacent rows and thus are adjacent to each other. These adjacent LBA sets are also contiguous because LBA 7, which corresponds to the highest LBA in LBA set 40, is contiguous with LBA 8, which is the lowest LBA in LBA set 42. Similarly, LBA sets 42 and 44 are also contiguous because LBA 15, which corresponds to the highest LBA in LBA set 42, is contiguous with LBA 16, which is the lowest LBA in LBA set 44. LBA set 44 is also contiguous with LBA set 45.

[0034] During operation and after initialization of mapping table 9, if storage device controller 22 receives an I/O transaction request 20 from host 18, *storage device controller 22 processes I/O transaction request by*

transferring it to DMA controller 10. After receiving I/O transaction request 20, DMA controller 10 uses mapping table 9 to determine which PBAs are mapped to LBAs used in I/O transaction request 20. DMA controller 10 uses the PBAs to determine which addressable physical memory locations to use when performing memory operations requested by host 18 through I/O transaction request 20.

Mapping table 9 associates LBA sets to PBAs in a manner that increases the likelihood *that memory operations resulting from I/O transaction request 20 will be **optimized by distributing these memory operations across different storage device resources that are associated with these PBAs**, such as across **different FDEs, different buses, different flash** memory devices, or **any combination of these**.* (Emphasis added.)

[0036] Using different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9, enables the ***interleaving*** of memory operations across flash devices that are controlled by the same FDE. (Emphasis added.) Stated another way, using different group identifiers enables interleaving memory operations across flash devices that belong to the same flash array bank interleave. Using different FDE identifiers in mapping table 9 enables interleaving memory operations across flash memory devices that are controlled by different FDEs, while using different bus identifiers enables interleaving memory operations across flash memory devices that are coupled to different flash bus interfaces.”

Thus, by the example discussed above, the Specification describes “how the mapping table causes the storage device to perform optimized memory operations” (See, Office Action) in a manner that meets the requirements in Section 112, first

paragraph, rendering claim 1 and its respective dependent claims statutory.

Claim 22

Claim 22 recites in part:

“wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.”

The above limitation in claim 22 is also supported by the Specification because the Specification teaches how a “mapping table” causes a “storage device to perform optimized memory operations”. See, Specification at paragraphs [0023]-[0025], [0034], and [0036] and FIGS. 1-2. Thus, claim 22 also meets the requirements in 35 USC Section 112, first paragraph, rendering claim 22 and its respective dependent claims statutory.

Claim 32

Claim 32 recites in part:

“wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.”

The above limitation in claim 32 is supported by the Specification because the

Specification teaches how a “mapping table increases the likelihood that the operational load imposed on the storage apparatus”...“will be optimally distributed across storage device resources” as recited in claim 32. See for example, paragraphs [0034] and [0036] (see also, FIGS. 1-2) which disclose the following:

“**[0034]** During operation and after initialization of mapping table 9, if storage device controller 22 receives an I/O transaction request 20 from host 18, storage device controller 22 processes I/O transaction request by transferring it to DMA controller 10. *After receiving I/O transaction request 20, DMA controller 10 **uses mapping table 9 to determine which PBAs are mapped to LBAs used in I/O transaction request 20.** DMA controller 10 uses the PBAs to determine which addressable physical memory locations to use when performing memory operations requested by host 18 through I/O transaction request 20. Mapping table 9 associates LBA sets to PBAs in a manner that **increases the likelihood that memory operations resulting from I/O transaction request 20 will be optimized by distributing these memory operations across different storage device resources that are associated with these PBAs,** such as across **different FDEs, different buses, different flash** memory devices, or **any combination of these.** (Emphasis added.)*

[0036] Using different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9, **enables the *interleaving*** of memory operations across flash devices that are controlled by the same FDE. Stated another way, using different group identifiers enables interleaving memory operations across flash devices that belong to the same flash array bank interleave. Using different FDE identifiers in mapping table 9 enables interleaving

memory operations across flash memory devices that are controlled by different FDEs, while using different bus identifiers enables interleaving memory operations across flash memory devices that are coupled to different flash bus interfaces. (Emphasis added.)”

Thus, claim 32 also meets the requirements in 35 USC Section 112, first paragraph, rendering claim 32 and its respective dependent claims statutory.

Request for Allowance

It is believed that this Response places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 25 February 2011

/Stephen R. Uriarte/

Stephen R. Uriarte, Reg. No. 40,854

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	)	Group Art Unit: 2187
	)	
Serial No.: 12/323,461	)	Examiner: FARROKH, Hashem
	)	
Filed: 25 Nov 2008	)	
	)	
For: OPTIMIZING MEMORY OPERATIONS	)	
IN AN ELECTRONIC STORAGE DEVICE	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR A ONE MONTH EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Dear Sir:

In conjunction with the Response to the Office Action, submitted on even date herewith, this is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows, indicated below:

Fees Paid:

<u>X</u>	One month (37 CFR 1.17(a)(1))	Fee (small entity: \$65.000)	<u>Paid</u>
<u> </u>	Two months (37 CFR 1.17(a)(2))	Fee (small entity: \$245.00)	<u>0.00</u>
<u> </u>	Three months (37 CFR 1.17(a)(3))	Fee (small entity: \$555.00)	<u>0.00</u>

Payment Method:

X Payment by credit card through EFS-web is provided.

Authorization to Charge/Credit Fees and Constructive Petition

X The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number: 50-4068. Please treat this authorization to charge all required fees under 37 CFR 1.17 as a constructive petition for an extension of time in accordance with 37 CFR 1.136(a)(3).

Sincerely,

Signature: /Stephen R. Uriarte/ Date: 25 February 2011
Name: Stephen R. Uriarte, Reg. No. 40,854

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Electronic Patent Application Fee Transmittal				
Application Number:		12323461		
Filing Date:		25-Nov-2008		
Title of Invention:		OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
First Named Inventor/Applicant Name:		Mark Ian ARCEDERA		
Filer:		Stephen Radcliff Uriarte		
Attorney Docket Number:		6005.007CIP		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	2251	1	65	65

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				65

Electronic Acknowledgement Receipt	
EFS ID:	9540274
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	25-FEB-2011
Filing Date:	25-NOV-2008
Time Stamp:	19:56:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$65
RAM confirmation Number	6316
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	6005_007CIP_Rsp21stOA_2011 0225_C.pdf	150204 b7388e90ee3290780b154d0f136109bc1fb 299ae	no	23
Warnings:					
Information:					
2	Extension of Time	6005_007CIP_Rsp21stOA_Ext_ 20110225_C.pdf	106906 2cf1d9f33aeaf307a706506f46035be2f69ba c12	no	2
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30363 d95d821ac757500de404e5c1e64235a5991 dc389	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			287473		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/323,461		Filing Date 11/25/2008		☐ To be Mailed				
APPLICATION AS FILED – PART I													
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY					
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A		OR		N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A		OR		N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A		OR		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =		OR		X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =		OR		X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.													
APPLICATION AS AMENDED – PART II										TOTAL			
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	02/25/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	* 40	Minus	** 40	= 0	X \$26 =	0	OR	X \$ =				
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$110 =	0	OR	X \$ =				
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
	TOTAL ADD'L FEE										0	OR	TOTAL ADD'L FEE
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =				
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =				
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
	TOTAL ADD'L FEE											OR	TOTAL ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

Legal Instrument Examiner:
/DORIS M. KING/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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NOTICE OF ALLOWANCE AND FEE(S) DUE

64180 7590 04/13/2011
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER

FARROKH, HASHEM

ART UNIT PAPER NUMBER

2187

DATE MAILED: 04/13/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802

TITLE OF INVENTION: OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	07/13/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 04/13/2011

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802
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TITLE OF INVENTION: OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	07/13/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2187	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802
64180	7590	04/13/2011	EXAMINER	
URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126			FARROKH, HASHEM	
			ART UNIT	PAPER NUMBER
			2187	

DATE MAILED: 04/13/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 242 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 242 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PART I **THE EXAMINER'S EVALUATION OF THE APPLICATION**

SECTION A **RELEVANT ART CITED BY THE EXAMINER**

1. U. S. Patent Publication No. 2009/0300318 A1 to Allen et al. describes ADDRESS CACHING STORED TRANSLATION.
2. U. S. Patent Publication No. 2005/0114587 A1 to Chou et al. describes Express Card with On-Card Flash Memory with Shared Flash-Control Bus but Separate Ready Lines.
3. U. S. Patent Publication No. 2003/0217202 A1 to Zilberman et al. describes Method for improving performance of a flash-based storage system using specialized flash controllers.

SECTION B **DISTINGUISHING FEATURES RECITED IN THE CLAIMS**

The following is an **Examiner's Statement of Reasons for Allowance** See MPEP 1302.14

4. The primary reasons for allowance of claims 1-31 in the instant application is the combination with the inclusion of the following limitations: **a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical**

fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and wherein, in response to receiving the I/O transaction request, said mapping table causes-the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

5. *The primary reasons for allowance of claims 32-40 in the instant application is the combination with the inclusion of the following limitations: **a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs; wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs; and wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of he I/O transaction request will be optimally distributed across storage device resources.***

The prior art of record including the disclosures of Allen et al. (2009/0300318 A1), Chou et al. (2005/0114587 A1), and Zilberman et al. (2003/0217202 A1) neither anticipates nor renders obvious the above-recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays should be clearly labeled "Comments on Statement of Reasons for Allowance"

SECTION C RESPONSE TO REMARKS

Applicant arguments regarding rejection of claims 1-40 under 35 U.S.C. 112, first paragraph is persuasive. Hence, rejection under 35 U.S.C. 112, first paragraph is withdrawn.

PART II THE ATTENTION OF FUTURE CORRESPONDENT

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571)272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*/HASHEM FARROKH/
Primary Examiner, Art Unit 2187*

Issue Classification 	Application/Control No. 12323461	Applicant(s)/Patent Under Reexamination ARCEDERA ET AL.
	Examiner HASHEM FARROKH	Art Unit 2187

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
711		103				G	0	6	F	12 / 00 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
711	203																	

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33										
	2		18		34										
	3		19		35										
	4		20		36										
	5		21		37										
	6		22		38										
	7		23		39										
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	9		25												
	10		26												
	11		27												
	12		28												
	13		29												
	14		30												
	15		31												
	16		32												

NONE		Total Claims Allowed:	
		40	
(Assistant Examiner)	(Date)		
/HASHEM FARROKH/ Primary Examiner.Art Unit 2187	03/25/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

<i>Search Notes</i> 	Application/Control No. 12323461	Applicant(s)/Patent Under Reexamination ARCEDERA ET AL.
	Examiner HASHEM FARROKH	Art Unit 2187

SEARCHED			
Class	Subclass	Date	Examiner
711	103	3/25/2011	HF
771	203	3/25/2011	HF

SEARCH NOTES		
Search Notes	Date	Examiner
PALM and EAST Inventor Search Conducted	10/19/2010	HF
EAST Text Search	10/19/2010	HF
IEEE Xplore Search Conducted	10/19/2010	HF
ACM Digital Library Search Conducted	10/19/2010	HF
PALM and EAST Inventor Search Updated	3/25/2011	HF
EAST Text Search Updated	3/25/2011	HF

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
711	103	3/25/2011	HF
711	203	3/25/2011	HF

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BIB DATA SHEET

CONFIRMATION NO. 7802

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/323,461	11/25/2008	711	2187	6005.007CIP		
RULE						
APPLICANTS Mark Ian ARCEDERA, Paranaque City, PHILIPPINES; Ritchie BABAYLAN, Cavite, PHILIPPINES; Reyjan LANUZA, Gen. T. De Leon Valenzuela City, PHILIPPINES; ** CONTINUING DATA ***** Yes /HF/ 03-25-2011 This application is a CIP of 11/450,005 06/08/2006 PAT 7,506,098 * and is a CIP of 11/450,023 06/08/2006 PAT 7,613,876 * (*)Data provided by applicant is not consistent with PTO records. ** FOREIGN APPLICATIONS ***** No /HF/ 03-25-2011 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED *** SMALL ENTITY ** 12/09/2008						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /HASHIM FARROKH/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY PHILIPPINES	SHEETS DRAWINGS 2	TOTAL CLAIMS 40	INDEPENDENT CLAIMS 3
ADDRESS URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126 UNITED STATES						
TITLE OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE						
FILING FEE RECEIVED 982	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4944	711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 21:33
L2	1637	711/203.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/25 21:39
S37	1	ARCEDERA-Mark-Ian.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:05
S38	3	BABAYLAN-Ritchie.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:05
S39	2	LANUZA-Reyjan.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:05
S40	2	((logical adj field) with ((logical near2 address) or LBA)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/25 17:07
S41	143	((physical adj block adj address) or PBA) near3 parameter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/25 17:08

S42	135	S41 and (@ad<"20081125")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:08
S43	10	S42 and "711"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:08
S44	1	S42 and "710"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:09
S45	1	S42 and "707"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:09
S46	1	S42 and "709"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/25 17:10
S47	399	((physical adj address) or PBA) and (parameter or arguments)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/25 17:11
S48	29	S47 and 711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/25 17:11
S49	20	S47 and 711/203.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/25 17:14

3/ 25/ 2011 10:24:11 PM

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URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126



**Courtesy Reminder for
Application Serial No: 12/323,461**

Attorney Docket No: 6005.007CIP
Customer Number: 64180
Date of Electronic Notification: 04/13/2011

This is a courtesy reminder that new correspondence is available for this application. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com

Please verify that these email addresses are correct.

To view your correspondence online or update your email addresses, please visit us anytime at **<https://sportal.uspto.gov/secure/myportal/privatepair>**. If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802

64180	7590	06/01/2011
URIARTE LAW		
Attn: Stephen R. Uriarte		
2021 The Alameda		
Suite 225		
San Jose, CA 95126		

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
06/01/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com



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Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 12323461
Applicant : Arcedera
Filing Date : 11/25/2008
Date Mailed : 06/01/2011

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 1 month(s) from the mail date of this Notice within which to respond.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED. **This period for reply is NOT extendable under 37 CFR 1.136(a).**

See attachment(s).

*A copy of this notice **MUST** be returned with the reply. Please address response to
"Mail Stop Issue Fee, Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450".*

/Kevin Danemark/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 12323461

IDENTIFICATION OF APPLICATION DEFICIENCIES

- ☐ Applicant must provide legible text for the following item(s).
- ☐ Specification filed , page(s) .
 - ☐ Claims filed , claim(s) .
 - ☐ Oath/declaration filed .
 - ☐ Other: .
- ☐ Applicant must provide missing information on the following page(s) of the specification by amending the specification to add the missing text. No new matter may be added.
- ☐ Applicant must provide an Abstract of the Disclosure.
- ☐ Applicant has submitted a DECLARATION (37 CFR 1.63) FOR A UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) (e.g., form PTO/SB/01A). The Application Data Sheet, however, is not present with the filed application. Applicant must submit an Application Data Sheet or file a new oath or declaration (e.g., PTO/SB/01) executed by the inventors and containing the information required in 37 CFR 1.63.
- ☐ Applicant must provide an executed declaration.
- ☐ Applicant must provide a declaration signed by inventor(s) .
- ☒ The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date may be required. See MPEP §§ 602.01 and 602.02. The oath or declaration is defective because:
- ☒ It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either an application data sheet or a supplemental oath or declaration.
 - ☐ The oath or declaration for the patent application was filed prior to December 1, 1997, and applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.
 - ☐ It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.
- ☐ Per 37 CFR § 1.63(a)(2), applicant must provide at least one given name without abbreviation for inventor(s) .



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 7802

SERIAL NUMBER 12/323,461	FILING OR 371(c) DATE 11/25/2008 RULE	CLASS 711	GROUP ART UNIT 2187	ATTORNEY DOCKET NO. 6005.007CIP	
APPLICANTS Mark Ian ARCEDERA, Paranaque City, PHILIPPINES; Ritchie BABAYLAN, Cavite, PHILIPPINES; Reyjan LANUZA, Gen. T. De Leon Valenzuela City, PHILIPPINES; ** CONTINUING DATA ***** This application is a CIP of 11/450,005 06/08/2006 PAT 7,506,098 * (*)Data provided by applicant is not consistent with PTO records. ** FOREIGN APPLICATIONS ***** IF REQUIRED, FOREIGN FILING LICENSE GRANTED** SMALL ENTITY ** ** 12/09/2008					
Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions ☐ yes ☐ no ☐ Met after met Allowance Verified and Acknowledged Examiner's Signature _____ Initials _____		STATE OR COUNTRY PHILIPPINES	SHEETS DRAWING 2	TOTAL CLAIMS 40	INDEPENDENT CLAIMS 3
ADDRESS 64180					
TITLE OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE					
FILING FEE RECEIVED 982	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	) Group Art Unit: 2187
	)
Serial No.: 12/323,461	) Examiner: FARROKH, Hashem
	)
Filed: 25 Nov 2008	)
	)
For: OPTIMIZING MEMORY OPERATIONS	)
IN AN ELECTRONIC STORAGE DEVICE	)
	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Dear Sir:

In response to the Notice to File Corrected Application Papers, mailed on 1 June 2011 and named the "Notice", please consider the remarks presented below.

In the Notice, it is asserted that "the oath or declaration is defective because it does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either an application data sheet (ADS) or a supplemental oath or declaration."

On 25 Nov 2008 the Applicants submitted via EFS-Web a fully executed Declaration For Utility or Design Application Using an Application Data Sheet and a corresponding ADS that lists the city and foreign country of residence for each inventor listed in the Declaration. The USPTO issued an electronic acknowledgment receipt showing receipt of these items.

In addition, on 30 Dec 2008 the Applicants also previously submitted a supplemental ADS that includes the city and foreign country of residence for each inventor. The copies of the original ADS and supplemental ADS are available on PAIR. Moreover, on 10 Dec 2008, the USPTO issued an Official Filing Receipt that reflects the city and foreign country of residence of

each joint inventor.

Electronic copies of these documents, which total 21 sheets, are filed concurrently with this paper:

1. Declaration (5 sheets);
2. ADS (5 sheets);
3. A USPTO Electronic Filing Receipt, dated 25 Nov 2008, showing receipt of the Declaration and ADS (3 sheets);
4. Supplemental ADS (5 sheets); and
5. Official Filing Receipt (3 sheets).

If the above remarks are deemed insufficient, please accept the city and foreign country of residence listed in the attached ADS or the supplemental ADS for each joint inventor listed in the Declaration.

Sincerely,

Signature: /Stephen R. Uriarte/ Date: 30 June 2011
Name: Stephen R. Uriarte, Reg. No.: 40,854

Uriarte Law
2021 The Alameda, Suite 225
San Jose, CA 95126
Tel: 408.244.2164
Fax: 408.716.2651
Email: mail@uriartelaw.com

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
-----------------------	--

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ Application No. _____ filed on _____
- ☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

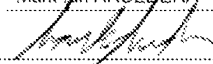
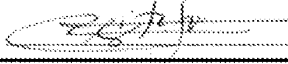
I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)	
Inventor one: Mark Ian ARCEDERA	Date: Nov 26, 2004
Signature: 	Citizen of: Philippines
Inventor two: Ritchie BABAYLAN	Date: Nov 26, 2004
Signature: 	Citizen of: Philippines
☒ Additional inventors or a legal representative are being named on _____ ONE additional form(s) attached hereto.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DECLARATION**ADDITIONAL INVENTOR(S)**
Supplemental SheetPage 1 of 1

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Reyjan		LANUZA	
Inventor's Signature <i>Reyjan C. Lanuza</i>		Date <i>11/25/08</i>	
Gen. T. De Leon Valenzuela City	State	Philippines	Philippines
Residence: City		Country	Citizenship
190D Policarpio Street			
Mailing Address			
Gen. T. De Leon Valenzuela City	State	1442	Philippines
City		Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION – Supplemental Priority Data Sheet[illegible]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1				
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117
				☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Mark	Ian	ARCEDERA	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Paranaque City	Country Of Residence	PH	
Citizenship under 37 CFR 1.41(b)		PH		
Mailing Address of Applicant:				
Address 1	30 Topaz St., Greenheights			
Address 2	Sucat			
City	Paranaque City	State/Province		
Postal Code	1700	Country	PH	
Applicant 2				
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117
				☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Ritchie		BABAYLAN	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Cavite	Country Of Residence	PH	
Citizenship under 37 CFR 1.41(b)		PH		
Mailing Address of Applicant:				
Address 1	122 Kiamzon St., Phase XI-B Bahayang Pag-Asa Subd.			
Address 2	Imus			
City	Cavite	State/Province		
Postal Code	4103	Country	PH	
Applicant 3				
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117
				☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Reyjan		LANUZA	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Gen. T. De Leon Valenzuela City	Country Of Residence	PH	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP	
		Application Number		
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE			
Citizenship under 37 CFR 1.41(b)		PH		
Mailing Address of Applicant:				
Address 1	190D Policarpio St.			
Address 2				
City	Gen. T. De Leon Valenzuela City		State/Province	
Postal Code	1442	Country	PH	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	64180		
Email Address	info@uriartelaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
Attorney Docket Number	6005.007CIP	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	2	Suggested Figure for Publication (if any)	2

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
Customer Number	64180		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	11450005	2006-06-06
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	11450023	2006-06-06
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

			Remove
Application Number	Country ¹	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1			
If the Assignee is an Organization check here. ☒			
Organization Name	BiTMICRO Networks, Inc.		
Mailing Address Information:			
Address 1	47929 Fremont Blvd		
Address 2			
City	Fremont	State/Province	CA
Country	US	Postal Code	94538
Phone Number	510.623.2341	Fax Number	510.623.2342
Email Address	info@bitmicro.com		
Additional Assignee Data may be generated within this form by selecting the Add button.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Stephen R. Uriarte/			Date (YYYY-MM-DD)	2008-11-25
First Name	Stephen	Last Name	Uriarte	Registration Number	40854

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	4357691
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian Arcedera
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	25-NOV-2008
Filing Date:	
Time Stamp:	23:23:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$982
RAM confirmation Number	6564
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:
Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		6005_007CIP_SpecALL_20081124C.pdf	159070 646224a2d8316a803ac15a3660c6297c23a1e93	yes	32
Multipart Description/PDF files in .zip description					
	Document Description		Start		End
	Specification		1		19
	Claims		20		31
	Abstract		32		32
Warnings:					
Information:					
2	Drawings-only black and white line drawings	6005_007CIP_FIGS_20081125C.pdf	203458 175fa25d9db7548a3fcd7230a7e6ec4a6fcd591	no	2
Warnings:					
Information:					
3	Application Data Sheet	6005_007CIP_ADS_20081125C.pdf	836613 72a577ad5ae19155997a689165463b326905ad01	no	5
Warnings:					
Information:					
4	Transmittal of New Application	6005_007CIP_AppnTL_20081125.pdf	278964 f32ca37885f05637e53089c90fc27db8f96c8bd	no	2
Warnings:					
Information:					
5	Oath or Declaration filed	6005_007CIP_Decl_SignedAll_20081125B.pdf	193252 9e5e7863e79a058f5fa8601334a98830c3d7b2a7	no	5
Warnings:					
Information:					
6	Fee Worksheet (PTO-06)	fee-info.pdf	36712 38940f5253799b6ac6f26a9c1337c72f989c8bc	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1708069		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/323,461	11/25/2008	2189	982	6005.007CIP	40	3

CONFIRMATION NO. 7802

64180
URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051

FILING RECEIPT



OC000000033532314

Date Mailed: 12/10/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Mark Ian ARCEDERA, Paranaque City, PHILIPPINES;
Ritchie BABAYLAN, Cavite, PHILIPPINES;
Reyjan LANUZA, Gen. T. De Leon Valenzuela City, PHILIPPINES;

Assignment For Published Patent Application

BITMICRO NETWORKS, INC., Fremont, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 11/450,005 06/08/2006 *
and is a CIP of 11/450,023 06/08/2006 *

(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications

If Required, Foreign Filing License Granted: 12/09/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/323,461**

Projected Publication Date: 03/19/2009

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Supplemental Application Data Sheet

Application Information

Title line One:: OPTIMIZING MEMORY OPERATIONS IN AN

Title Line Two:: ELECTRONIC STORAGE DEVICE

Application Number:: 12/323,461

Filing Date:: 11/25/08

Application Type:: Nonprovisional

Subject Matter:: Utility

Suggested classification::

Suggested Group Art Unit:: 2189

CD-ROM or CD-R?: None

Attorney Docket Number:: 6005.007CIP

Request for Early Publication?: No

Request for Non-Publication?: No

Suggested Drawing Figure:: 2

Total Drawing Sheets:: 2

Small Entity:: Yes

Petition included?: No

Petition Type::

Licensed US Govt. Agency::

Contract or Grant Numbers::

Secrecy Order in Parent Appl.?: No

Applicant Information

Applicant Authority type:: Inventor
Primary Citizenship Country:: PH
Status:: Full Capacity
Inventor One Given Name:: Mark
Middle Initial:: I.
Family Name:: ARCEDERA
City of Residence:: Paranaque City
Country of Residence:: PH
Street of mailing address:: 30 Topaz St., Greenheights
Sucat
City of mailing address:: Paranaque City
Postal or Zip Code of mailing address:: 1700

Applicant Authority type:: Inventor
Primary Citizenship Country:: PH
Status:: Full Capacity
Inventor Two Given Name:: Ritchie
Middle Initial::

Family Name:: BABAYLAN
City of Residence:: 122 Kiamzon St., Phase XI-B Bahayang Pag-Asa
Subd.
Country of Residence:: PH
Street of mailing address:: 122 Kiamzon St., Phase XI-B Bahayang Pag-Asa
Subd.
Imus
City of mailing address:: Cavite
Postal or Zip Code of mailing address:: 4103

Applicant Authority type:: Inventor
Primary Citizenship Country:: PH
Status:: Full Capacity
Inventor Three Given Name:: Reyjan
Middle Initial::
Family Name:: LANUZA
City of Residence:: Gen. T. De Leon Valenzuela City
Country of Residence:: PH
Street of mailing address:: 190D Policarpio St.
City of mailing address:: Gen. T. De Leon Valenzuela City
Postal or Zip Code of mailing address:: 1442

Correspondence Information

Correspondence Customer Number:: 64180

Phone number:: 408.244.2164 x111

Fax number:: 408.716.2651

E-Mail address:: info@uriartelaw.com

Representative Information

Representative Customer Number::	64180	
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Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
<u>This application is a</u>	Continuation in part of	11450005	[[2006-06-06]] <u>2006-06-08</u>
	Continuation in part of	11450023	[[2006-06-06]]

Foreign Priority Information

Country::	Application number::	Filing Date::	Priority Claimed::
			[[Yes]] <u>No</u>

Assignee Information

Assignee name:: BiTMICRO Networks, Inc.
Street of mailing address:: 47929 Fremont Blvd
City of mailing address:: Fremont
State or Province of mailing address:: CA
Country of mailing:: US
Postal or Zip Code of mailing address:: 94538

Electronic Acknowledgement Receipt	
EFS ID:	10442273
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	01-JUL-2011
Filing Date:	25-NOV-2008
Time Stamp:	16:35:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	6005_007CIP_Rsp2_Communication_ALL_20110701d.pdf	21331697 7f92907b5d36456416c07f16f815d8188561435c	no	23

Warnings:

Information:

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	)	Group Art Unit: 2187
	)	
Serial No.: 12/323,461	)	Examiner: FARROKH, Hashem
	)	
Filed: 25 Nov 2008	)	
	)	
For: OPTIMIZING MEMORY OPERATIONS	)	
IN AN ELECTRONIC STORAGE DEVICE	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE (SUPPLEMENTAL) TO NOTICE TO FILE CORRECTED APPLICATION
PAPERS

Dear Sir:

A prior response, which is responsive to the Notice to File Corrected Application Papers having a 1 June 2011 mail date and named Notice", was previously submitted with the USPTO on 1 July 2011. This prior response, however, did not include a copy of the Notice. Consequently, please replace the prior response with this supplemental response to the Notice as amended and restated below.

In response to the Notice to File Corrected Application Papers, mailed on 1 June 2011 and named the "Notice", please consider the remarks presented below.

In the Notice, it is asserted that "the oath or declaration is defective because it does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either an application data sheet (ADS) or a supplemental oath or declaration."

On 25 Nov 2008 the Applicants submitted via EFS-Web a fully executed Declaration For Utility or Design Application Using an Application Data Sheet and a corresponding ADS that

lists the city and foreign country of residence for each inventor listed in the Declaration. The USPTO issued an electronic acknowledgment receipt showing receipt of these items.

In addition, on 30 Dec 2008 the Applicants also previously submitted a supplemental ADS that includes the city and foreign country of residence for each inventor. The copies of the original ADS and supplemental ADS are available on PAIR. Moreover, on 10 Dec 2008, the USPTO issued an Official Filing Receipt that reflects the city and foreign country of residence of each joint inventor.

Electronic copies of the above documents, which total **24** sheets excluding the prior response, are filed concurrently with this paper:

1. Declaration (5 sheets);
2. ADS (5 sheets);
3. A USPTO Electronic Filing Receipt, dated 25 Nov 2008, showing receipt of the Declaration and ADS (3 sheets);
4. Supplemental ADS (5 sheets);
5. Official Filing Receipt (3 sheets); and
6. Copy of the Notice to File Corrected Application Papers (3 sheets).

If the above remarks are deemed insufficient, please accept the city and foreign country of residence listed in the attached ADS or the supplemental ADS for each joint inventor listed in the Declaration.

Sincerely,

Signature:	<u>/Stephen R. Uriarte/</u>	Date:	<u>1 July 2011</u>
Name:	Stephen R. Uriarte, Reg. No.: 40,854		

Uriarte Law
2021 The Alameda, Suite 225
San Jose, CA 95126
Tel: 408.244.2164
Fax: 408.716.2651
Email: mail@uriartelaw.com

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
-----------------------	--

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ Application No. _____ filed on _____
- ☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

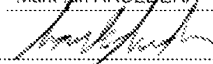
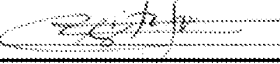
I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)	
Inventor one: Mark Ian ARCEDERA	Date: Nov 26, 2004
Signature: 	Citizen of: Philippines
Inventor two: Ritchie BABAYLAN	Date: Nov 26, 2004
Signature: 	Citizen of: Philippines
☒ Additional inventors or a legal representative are being named on _____ ONE additional form(s) attached hereto.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet
Page <u>1</u> of <u>1</u>	

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Reyjan		LANUZA	
Inventor's Signature <i>Reyjan C. Lanuza</i>		Date <i>11/25/08</i>	
Gen. T. De Leon Valenzuela City	State	Philippines Country	Philippines Citizenship
190D Policarpo Street			
Mailing Address			
Gen. T. De Leon Valenzuela City	State	1442 Zip	Philippines Country
City		Country	
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION – Supplemental Priority Data Sheet[illegible]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1				
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117
				☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Mark	Ian	ARCEDERA	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Paranaque City	Country Of Residence	PH	
Citizenship under 37 CFR 1.41(b)		PH		
Mailing Address of Applicant:				
Address 1	30 Topaz St., Greenheights			
Address 2	Sucat			
City	Paranaque City	State/Province		
Postal Code	1700	Country	PH	
Applicant 2				
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117
				☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Ritchie		BABAYLAN	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Cavite	Country Of Residence	PH	
Citizenship under 37 CFR 1.41(b)		PH		
Mailing Address of Applicant:				
Address 1	122 Kiamzon St., Phase XI-B Bahayang Pag-Asa Subd.			
Address 2	Imus			
City	Cavite	State/Province		
Postal Code	4103	Country	PH	
Applicant 3				
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117
				☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Reyjan		LANUZA	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Gen. T. De Leon Valenzuela City	Country Of Residence	PH	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP	
		Application Number		
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE			
Citizenship under 37 CFR 1.41(b)		PH		
Mailing Address of Applicant:				
Address 1	190D Policarpio St.			
Address 2				
City	Gen. T. De Leon Valenzuela City		State/Province	
Postal Code	1442	Country	PH	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	64180		
Email Address	info@uriartelaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
Attorney Docket Number	6005.007CIP	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	2	Suggested Figure for Publication (if any)	2

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
Customer Number	64180		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	11450005	2006-06-06
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	11450023	2006-06-06
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove			
Application Number	Country ¹	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1			
If the Assignee is an Organization check here. ☒			
Organization Name	BiTMICRO Networks, Inc.		
Mailing Address Information:			
Address 1	47929 Fremont Blvd		
Address 2			
City	Fremont	State/Province	CA
Country	US	Postal Code	94538
Phone Number	510.623.2341	Fax Number	510.623.2342
Email Address	info@bitmicro.com		
Additional Assignee Data may be generated within this form by selecting the Add button.			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	6005.007CIP
		Application Number	
Title of Invention	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Stephen R. Uriarte/			Date (YYYY-MM-DD)	2008-11-25
First Name	Stephen	Last Name	Uriarte	Registration Number	40854

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Electronic Acknowledgement Receipt

EFS ID:	4357691
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian Arcedera
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	25-NOV-2008
Filing Date:	
Time Stamp:	23:23:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$982
RAM confirmation Number	6564
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:
Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		6005_007CIP_SpecALL_20081124C.pdf	159070 646224a08316a803ac15a3660c6297c23a7e93	yes	32
Multipart Description/PDF files in .zip description					
	Document Description		Start		End
	Specification		1		19
	Claims		20		31
	Abstract		32		32
Warnings:					
Information:					
2	Drawings-only black and white line drawings	6005_007CIP_FIGS_20081125C.pdf	203458 17f9c5d9d9b754a833fd7230a7e6ec84a6f0f591	no	2
Warnings:					
Information:					
3	Application Data Sheet	6005_007CIP_ADS_20081125C.pdf	836613 72a577ad5ae19125997e689165463b3299015ad01	no	5
Warnings:					
Information:					
4	Transmittal of New Application	6005_007CIP_AppnTL_20081125.pdf	278964 f32cc257885f05637e530886c90fc27db8b9c78bd	no	2
Warnings:					
Information:					
5	Oath or Declaration filed	6005_007CIP_Decl_SignedAll_20081125B.pdf	193252 8e5e7f63e79a058f5f4860133a6b88d30e87b2a7	no	5
Warnings:					
Information:					
6	Fee Worksheet (PTO-06)	fee-info.pdf	36712 3d940f52537f99b6ac6f26a9c137cf2f980a78d	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1708069		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/323,461	11/25/2008	2189	982	6005.007CIP	40	3

CONFIRMATION NO. 7802

64180
URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051

FILING RECEIPT



OC000000033532314

Date Mailed: 12/10/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Mark Ian ARCEDERA, Paranaque City, PHILIPPINES;
Ritchie BABAYLAN, Cavite, PHILIPPINES;
Reyjan LANUZA, Gen. T. De Leon Valenzuela City, PHILIPPINES;

Assignment For Published Patent Application

BITMICRO NETWORKS, INC., Fremont, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 11/450,005 06/08/2006 *
and is a CIP of 11/450,023 06/08/2006 *

(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications

If Required, Foreign Filing License Granted: 12/09/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/323,461**

Projected Publication Date: 03/19/2009

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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Supplemental Application Data Sheet

Application Information

Title line One:: OPTIMIZING MEMORY OPERATIONS IN AN

Title Line Two:: ELECTRONIC STORAGE DEVICE

Application Number:: 12/323,461

Filing Date:: 11/25/08

Application Type:: Nonprovisional

Subject Matter:: Utility

Suggested classification::

Suggested Group Art Unit:: 2189

CD-ROM or CD-R?:: None

Attorney Docket Number:: 6005.007CIP

Request for Early Publication?:: No

Request for Non-Publication?:: No

Suggested Drawing Figure:: 2

Total Drawing Sheets:: 2

Small Entity:: Yes

Petition included?:: No

Petition Type::

Licensed US Govt. Agency::

Contract or Grant Numbers::

Secrecy Order in Parent Appl.?: No

Applicant Information

Applicant Authority type:: Inventor
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Representative Information

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Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
<u>This application is a</u>	Continuation in part of	11450005	[[2006-06-06]] <u>2006-06-08</u>
	Continuation in part of	11450023	[[2006-06-06]]

Foreign Priority Information

Country::	Application number::	Filing Date::	Priority Claimed::
			[[Yes]] <u>No</u>

Assignee Information

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State or Province of mailing address:: CA
Country of mailing:: US
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802

64180 7590 06/01/2011
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER

FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
06/01/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Application No. : 12323461
Applicant : Arcedera
Filing Date : 11/25/2008
Date Mailed : 06/01/2011

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 1 month(s) from the mail date of this Notice within which to respond.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED. **This period for reply is NOT extendable under 37 CFR 1.136(a).**

See attachment(s).

*A copy of this notice **MUST** be returned with the reply. Please address response to
"Mail Stop Issue Fee, Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450".*

/Kevin Danemark/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 12323461

IDENTIFICATION OF APPLICATION DEFICIENCIES

- ☐ Applicant must provide legible text for the following item(s).
- ☐ Specification filed , page(s) .
 - ☐ Claims filed , claim(s) .
 - ☐ Oath/declaration filed .
 - ☐ Other: .
- ☐ Applicant must provide missing information on the following page(s) of the specification by amending the specification to add the missing text. No new matter may be added.
- ☐ Applicant must provide an Abstract of the Disclosure.
- ☐ Applicant has submitted a DECLARATION (37 CFR 1.63) FOR A UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) (e.g., form PTO/SB/01A). The Application Data Sheet, however, is not present with the filed application. Applicant must submit an Application Data Sheet or file a new oath or declaration (e.g., PTO/SB/01) executed by the inventors and containing the information required in 37 CFR 1.63.
- ☐ Applicant must provide an executed declaration.
- ☐ Applicant must provide a declaration signed by inventor(s) .
- ☒ The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date may be required. See MPEP §§ 602.01 and 602.02. The oath or declaration is defective because:
- ☒ It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either an application data sheet or a supplemental oath or declaration.
 - ☐ The oath or declaration for the patent application was filed prior to December 1, 1997, and applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.
 - ☐ It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.
- ☐ Per 37 CFR § 1.63(a)(2), applicant must provide at least one given name without abbreviation for inventor(s) .

Electronic Acknowledgement Receipt	
EFS ID:	10443213
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	01-JUL-2011
Filing Date:	25-NOV-2008
Time Stamp:	17:40:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	6005_007CIP_Suppl_Rsp2_Comm_ALL_20110701_B.pdf	23911485 62a2418bd623d01056c415439273ebc3547a644f	no	26

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007C1P	7802
64180	7590	07/05/2011		
URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126			EXAMINER FARROKH, HASHEM	
			ART UNIT 2187	PAPER NUMBER
			NOTIFICATION DATE 07/05/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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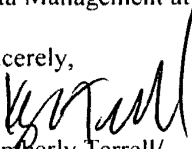
In re Application of :
Mark Ian Arcedera, et al :
Application No. 12323461 :
Filed: 11/25/2008 :
Attorney Docket No. **6005.007CIP** :

To Whom It May Concern:

The USPTO mailed a Notice to File Corrected Application Papers to your office on 06/01/2011. This notice was sent in error as the application contains the city and country of residence for each inventor in the Application Data Sheet filed with the application on November 25, 2008. Therefore, the requirement to respond to this notice within 1 month is waived and no response is required.

Telephone inquiries relating to this decision may be directed to the undersigned in the Office of Data Management at 571-272-4200.

Sincerely,


/Kimberly Terrell/
Manager
Office of Data Management
Publications Branch

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	)	Group Art Unit: 2187
	)	
Serial No.: 12/323,461	)	Examiner: FARROKH, Hashem
	)	
Filed: 25 Nov 2008	)	
	)	
For: OPTIMIZING MEMORY OPERATIONS	)	
IN AN ELECTRONIC STORAGE DEVICE	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER ALLOWANCE

Dear Examiner:

Please amend this Application as follows and consider the remarks set forth below.

Amendments to the specification begin on page **2**;

A listing of claims begin on page **3**; and

Remarks begin on page **17** of this paper.

Amendment(s) to the Specification

In the Specification, please enter the amendments shown with respect to the replacement paragraphs identified below. Text in underline indicates new text, while text in strike-out format or between a pair of double brackets indicates deletion of text. No new matter has been added.

In the Cross-Reference to Related Applications section on page 1 of the Specification, please replace paragraph [001] with the following paragraph:

[001] This application is a continuation in part application and claims the benefit of United States patent application no. 11/450,005, filed 8 June 2006, entitled "Optimized Placement Policy for Solid State Storage Devices, ~~filed on 8 June 2006,~~ and having Serial No.: ~~11/450,005 and attorney docket number 6005.007~~ now United States Patent 7,506,098, which is hereby incorporated by reference as if fully set forth herein.

On page 8, please replace paragraph [0015] with the following paragraph:

[0015] In another example, DMA controller 10 may be implemented in the form of Flash DMA controller 109, which is part of hybrid storage controller 102, which are further disclosed in FIG. 1 of United States patent application no. 11/450,023, filed 8 June 2006, entitled "Hybrid Multi-Tiered Caching Storage System", ~~filed on 8 June 2006,~~ and having Serial No.: ~~11/450,023 and attorney docket number 6005.006~~ now United States Patent 7,613,876, which is hereby incorporated by reference as if fully set forth herein.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (CURRENTLY AMENDED) A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes[[the storage]]the electronic storage device to perform optimized

memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

2. (ORIGINAL) The mapping table of claim 1, wherein:

said first and second LBA sets are adjacent LBA sets;

said first and second access parameters are different; and

said LBAs from said first and second LBA sets are logical block addresses used by the host for addressing said data.

3. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

4. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is not consecutive with an LBA having the highest LBA value from said first LBA set.

5. (ORIGINAL) The mapping table of claim 1, wherein:

data stored at a first physical memory location, which is addressable using said first PBA, is transferred to a second physical memory location, which is

addressable using said second PBA, said data transferred in portions equal to a section size.

6. (ORIGINAL) The mapping table of claim 5, wherein:

said first and second LBA sets respectively have an LBA set size equal to said section size.

7. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

8. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that supports more than one page write that can be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said one of said flash blocks; and

said section size is at least equal to a quotient resulting from dividing said native page size by said more than one page write.

9. (ORIGINAL) The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier.
10. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.
11. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers.
12. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different bus identifiers.
13. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different FDE identifiers.
14. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBAs respectively include a first group identifier and a second group identifier.
15. (ORIGINAL) The mapping table of claim 1:

wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and

wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs.

16. (ORIGINAL) The mapping table of claim 1, wherein:

said memory store includes a first set of memory devices controlled by a first FDE and a second set of memory devices controlled by a second FDE; and

said first and second sets of memory devices associated with a plurality of group identifiers in which no two of said group identifiers is the same, and each memory device from said first set of memory devices is respectively associated with different group identifiers from said plurality of group identifiers.

17. (ORIGINAL) The mapping table of claim 1, wherein:

said electronic storage device includes a storage device controller, said memory store, and a memory system;

said memory system includes a flash buffer controller, a first set of FDEs, a second set of FDEs, and a set of buses that includes a first bus and a second bus;

said memory store includes a first set of memory devices and a second set of memory devices, said first and second set of memory devices respectively coupled to said first and second buses;

said first set of FDEs disposed to control said first set of memory devices through said flash buffer controller and said first bus, said first set of FDEs including a first FDE and a second FDE;

said second set of FDEs disposed to control said second set of memory devices through said flash buffer controller and said second bus, said second set of FDEs including a third FDE and a fourth FDE;

said first and second set of memory devices are associated with a plurality of memory device groups, including a first group and a second group;

wherein said first and second groups corresponding respectively to said first and second group identifiers; and

wherein said first and second PBAs respectively include said first and second group identifiers.

18. (ORIGINAL) The mapping table of claim 17, wherein said first and third memory devices are associated with a first group identifier and said second and fourth memory devices are associated with a second group identifier.

19. (ORIGINAL) The mapping table of claim 17, wherein said first and second memory devices include non-volatile solid state memory cells.

20. (ORIGINAL) The mapping table of claim 17, wherein each memory device from said first set of memory devices are respectively associated with different group identifiers.

21. (ORIGINAL) The mapping table of claim 1, wherein said first PBA further disposed to represent a memory index.

22. (ORIGINAL) A memory system for optimizing memory operations in an electronic storage device responsive to an I/O transaction request initiated by a host, said electronic storage device including a memory store having a set of memory devices including a first memory device, a second memory device, a third memory device and a fourth memory device, said memory system comprising:

a flash buffer controller, a set of FDEs, and a set of buses, wherein said set of FDEs including a first FDE, a second FDE, a third FDE, and a fourth FDE and wherein said buses including a first bus and a second bus, said first bus coupled to the first and second memory devices, and the second bus coupled to said third and fourth memory devices;

said first and second FDEs coupled to said first bus through said first buffer controller, and said third and fourth FDEs coupled to said second bus through said first buffer controller;

said set of memory devices are partitioned into memory device groups, including a first group and a second group;

a mapping table that includes:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for holding a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.

23. (ORIGINAL) The memory system of claim 22, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

24. (ORIGINAL) The memory system of claim 22, wherein said first and third memory devices correspond to a first group identifier and said second and fourth memory devices correspond to a second group identifier.

25. (ORIGINAL) The memory system of claim 22, wherein said optimized memory operations include a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

26. (ORIGINAL) The memory system of claim 25, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier and a group identifier.

27. (ORIGINAL) The memory system of claim 26, wherein said first and second PBAs respectively include said first and second group identifiers.

28. (ORIGINAL) The memory system of claim 22, wherein said PBA further includes a memory index.

29. (ORIGINAL) The memory system of claim 22, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

30. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

31. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

32. (ORIGINAL) An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:

a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;

a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;

a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;

wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs; and

wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.

33. (ORIGINAL) The electronic storage device of claim 32, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

34. (ORIGINAL) The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

35. (ORIGINAL) The memory system of claim 34, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier, and a group identifier.

36. (ORIGINAL) The memory system of claim 35, wherein said first and second PBAs respectively include said first and second group identifiers.

37. (ORIGINAL) The electronic storage device of claim 32, wherein said PBA further includes a memory index.

38. (ORIGINAL) The electronic storage device of claim 32, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

39. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

40. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

Remarks

Specification Amendments

The Cross-Reference to Related Applications section of the specification has been amended by replacing the reference to the attorney docket number with the patent number for the parent application and by rearranging the contents of the paragraph to improve readability.

Paragraph [0015] has been amended by replacing the attorney docket number with the patent number of the United States patent application referred to in the amended paragraph and by rearranging the contents of the paragraph to improve readability.

These amendments are of a clerical nature and do not add "new matter".

The Listing of Claims

Claim 1 is amended to provide proper antecedent basis by adding the term "electronic" before the term "storage device". The preamble to claim 1 introduced the term "electronic storage device" but the previous version of claim 1 in the claim elements used the term "storage device". This amendment is readily ascertainable from claim 1 and thus, does not add new matter or require a new search.

Claim 1 is also amended by removing the dash symbol "-" after between "the" and "storage device". The inclusion of the dash was an inadvertent typographical error and its removal does not change the scope or meaning of claim 1. Consequently, this amendment also does not add new matter or necessitate a new search.

Request for Entry of Amendment

It is believed that this Amendment After Allowance renders the Application in a condition for issuance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 12 July 2011

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

Uriarte Law
2021 The Alameda, Suite 225
San Jose, CA 95126
Tel: 408.244.2164 x111
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Email: mail@uriartelaw.com

Electronic Acknowledgement Receipt	
EFS ID:	10505279
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	12-JUL-2011
Filing Date:	25-NOV-2008
Time Stamp:	22:01:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	6005_007CIP_AmendAftAllow_20110712B.pdf	110471 4b4208421ad4c45789f058c1b13b0e6390aded63	no	18

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 04/13/2011
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 Attn: Stephen R. Uriarte
 2021 The Alameda
 Suite 225
 San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802
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TITLE OF INVENTION: OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	07/13/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2187	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Stephen R. Uriarte

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

BitMICRO Networks, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Fremont, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached. Via EFS-Web
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 504068 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☒ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Stephen R. Uriarte/

Date 13 July 2011

Typed or printed name Stephen R. Uriarte

Registration No. 40,854

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PART B - FEE(S) TRANSMITTAL

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Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 04/13/2011
URIARTE LAW
 Attn: Stephen R. Uriarte
 2021 The Alameda
 Suite 225
 San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802
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TITLE OF INVENTION: OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	07/13/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2187	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Stephen R. Uriarte
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

BitMICRO Networks, Inc.

Fremont, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
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☐ A check is enclosed.
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☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 504068 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☒ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Stephen R. Uriarte/

Date 13 July 2011

Typed or printed name Stephen R. Uriarte

Registration No. 40,854

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:		12323461		
Filing Date:		25-Nov-2008		
Title of Invention:		OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE		
First Named Inventor/Applicant Name:		Mark Ian ARCEDERA		
Filer:		Stephen Radcliff Uriarte		
Attorney Docket Number:		6005.007CIP		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	755	755
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1055

Electronic Acknowledgement Receipt	
EFS ID:	10514504
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.007CIP
Receipt Date:	13-JUL-2011
Filing Date:	25-NOV-2008
Time Stamp:	18:42:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1055
RAM confirmation Number	7583
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	6005_007CIP_Reply2Allowance _EFS_20110713C.pdf	1754607	no	2
			b37d76875defe236c49a1e4c96884a7a708 96136		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31685	no	2
			d74f302304f2a59d86ce85135a9703a57a68 52f2		
Warnings:					
Information:					
Total Files Size (in bytes):			1786292		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.	)	Group Art Unit: 2187
	)	
Serial No.: 12/323,461	)	Examiner: FARROKH, Hashem
	)	
Filed: 25 Nov 2008	)	
	)	
For: OPTIMIZING MEMORY OPERATIONS	)	
IN AN ELECTRONIC STORAGE DEVICE	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER ALLOWANCE

Dear Examiner:

Please amend this Application as follows and consider the remarks set forth below.

Amendments to the specification begin on page **2**;

A listing of claims begin on page **3**; and

Remarks begin on page **17** of this paper.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007CIP	7802
64180	7590	07/28/2011	EXAMINER	
URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126			FARROKH, HASHEM	
			ART UNIT	PAPER NUMBER
			2187	
			NOTIFICATION DATE	DELIVERY MODE
			07/28/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com

Response to Rule 312 Communication	Application No. 12/323,461	Applicant(s) ARCEDERA ET AL.
	Examiner Hashem Farrokh	Art Unit 2188
<p align="center">-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --</p> <p>1. ☒ The amendment filed on <u>12 July 2011</u> under 37 CFR 1.312 has been considered, and has been:</p> <p>a) ☐ entered.</p> <p>b) ☒ entered as directed to matters of form not affecting the scope of the invention.</p> <p>c) ☐ disapproved because the amendment was filed after the payment of the issue fee. Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.</p> <p>d) ☐ disapproved. See explanation below.</p> <p>e) ☒ entered in part. See explanation below.</p> <p>The Applicant has not expressly stated that the after final amendment filed on 07/12/2011 is under 35 CFR 1.312, However, since amendment(s) has directed to the matter(s) that not affect or change the scope of claim(s), the Examiner has considered the amendment(s) to be under 35 CFR 1.312.</p>		
/Hashem Farrokh/ Primary Examiner, Art Unit 2188		



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	08/30/2011	8010740	6005.007CIP	7802

64180 7590 08/10/2011
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 181 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Mark Ian ARCEDERA, Paranaque City, PHILIPPINES;
Ritchie BABAYLAN, Cavite, PHILIPPINES;
Reyjan LANUZA, Gen. T. De Leon Valenzuela City, PHILIPPINES;

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ARCEDERA et al.)
Serial #: 12/323,461)
Patent #: **8,010,740**)
Issue Date: **30 AUG 2011**)
Confirmation Number: 7802)
Application Filing Date: 25 Nov. 2008)
For: OPTIMIZING MEMORY OPERATIONS IN)
AN ELECTRONIC STORAGE DEVICE)

Certificate of EFS-Web Transmission

I hereby certify that this correspondence is being transmitted via the U.S. Patent and Trademark Office(USPTO) electronic filing system (EFS-Web) to the USPTO on **12 September 2014.**

Certificate Signer: Arnold de Guzman
Signature: /Arnold de Guzman/
Registration Number: 39,955

Director of the United States Patent & Trademark Office
Attn: Maintenance Fee
2051 Jamieson Avenue, Suite 300
Alexandria, VA 22314

Notification of Loss of Entitlement to Small Entity Status

Dear Sir/Madam:

Entity Status Change from Small to Large Entity:

X In accordance with 37 CFR 1.27 and 1.33(b), please accept this paper as notice of a *loss of entitlement to small entity status for the above-referred issued U.S. patent.*

Thank you for your assistance.

Sincerely,

Signature: /Arnold de Guzman/
Name: Arnold de Guzman

Date: 12 September 2014
USPTO Reg. #: 39,955

Bitmicro Networks, Inc.
47929 Fremont Blvd
Fremont, CA 94538
Tel: 510.743.3173
Fax: 510.623.2342

Electronic Acknowledgement Receipt	
EFS ID:	20118967
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.007CIP
Receipt Date:	12-SEP-2014
Filing Date:	25-NOV-2008
Time Stamp:	08:56:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Notification of loss of entitlement to small entity status	6005_007CIP_EntitlementLoss Notice.pdf	50491 c035c16e2dec303cd206d01b9b9b1079ca7a3362	no	1

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT4586333

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
BITMICRO NETWORKS, INC.		06/30/2017
RECEIVING PARTY DATA		
Name:	BITMICRO LLC	
Street Address:	1620 N. WACCAMAW DRIVE	
Internal Address:	SUITE 109	
City:	MURRELLS INLET	
State/Country:	SOUTH CAROLINA	
Postal Code:	29576	
PROPERTY NUMBERS Total: 34		
Property Type	Number	
Patent Number:	6496939	
Patent Number:	9372755	
Patent Number:	6970890	
Patent Number:	7729370	
Patent Number:	7826243	
Patent Number:	8093103	
Patent Number:	6317330	
Patent Number:	9423457	
Patent Number:	9552848	
Patent Number:	6744635	
Patent Number:	7716389	
Patent Number:	8165301	
Patent Number:	7620748	
Patent Number:	9400617	
Patent Number:	9672178	
Patent Number:	9043669	
Patent Number:	7613876	
Patent Number:	8032700	
Patent Number:	9430386	

Property Type	Number
Patent Number:	9734067
Patent Number:	6000006
Patent Number:	5822251
Patent Number:	9099187
Patent Number:	8560804
Patent Number:	9484103
Patent Number:	8010740
Patent Number:	7506098
Patent Number:	8447908
Patent Number:	8788725
Application Number:	14297628
Patent Number:	6529416
Patent Number:	5956743
Patent Number:	9135190
Patent Number:	6757845

CORRESPONDENCE DATA

Fax Number: (512)391-2173

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 512.236.2023

Email: rdewanipdocket@jw.com

Correspondent Name: JACKSON WALKER L.L.P.

Address Line 1: 100 CONGRESS AVENUE

Address Line 2: SUITE 1100

Address Line 4: AUSTIN, TEXAS 78701

NAME OF SUBMITTER:	HEATHER BUCEK
SIGNATURE:	/heather bucek/
DATE SIGNED:	09/08/2017
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 8

source=BitMicro Recordable Assignment#page1.tif

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RECORDABLE ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **BITMICRO Networks, Inc.**, a California company having offices at 47929 Fremont Blvd., Fremont, CA 94538 ("**Assignor**") and **BITMICRO LLC**, a Delaware Company having offices at 1620 N. Waccamaw Drive, Suite 109, Murrells Inlet, SC 29576 does hereby sell, assign, transfer, and convey unto (hereafter "**Assignee**") all its right, title, and interest in and to any and all of the following (collectively, the "**Patent Rights**"):

(a) the patent applications and patents listed in the table below and any issued patent or patent application that directly or indirectly claims or is amended to claim priority to any of the above, in whole or in part (the "**Patents**");

(b) to the extent not included in Section (a) above, all issued patents, rights to inventions and pending and future applications for patents under U.S. law or regulation or any foreign country with respect to the patentable inventions from which such Patents arise, including without limitation, utility patents, utility models, design patents, invention certificates, provisional, reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications, requests for continuing examinations, divisionals, renewals, and registrations in all countries of the world, as well as any patents and patent applications to which any of the Patents or the foregoing directly or indirectly claim priority, in whole or in part;

(c) all related patent filing and prosecution documents;

(d) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any of the Patents and the inventions, invention disclosures, and discoveries therein;

(e) all inventions and discoveries described in any of the Patents or subject matter capable of being reduced to a patent claim in any of the Patents based on the specification of any of the Patents;

(f) priority rights in any and all patent filings available from and/or through the Patents; and

(g) causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of any of the Patents or of any patent that issues from any of the Patents, including, without limitation, all causes of action and other enforcement rights for (1) damages, (2) injunctive relief, and (3) any other remedies of any kind for past, current and future infringement and all of the proceeds from the foregoing, that are accrued and unpaid or that are hereafter accruing;

(h) rights to collect royalties or other payments under or on account of any of the Patents and/or any of the foregoing categories (a) through (g); and

(i) rights of cooperation assigned or granted by any third party under or on account of any of the Patents and/or any of the foregoing categories (a) through (h).

Assignor represents, warrants and covenants that:

Assignor has the full power and authority, and has obtained all third-party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at

Fremont, CA on 30 JUNE 2017

Assignor:

BITMICRO Networks, Inc.

By: 

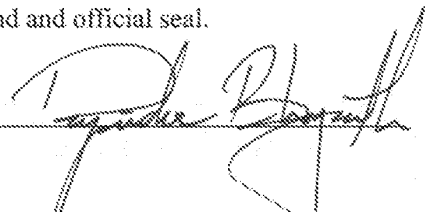
Name: Stephen R. Urmate

Title: President & General Counsel

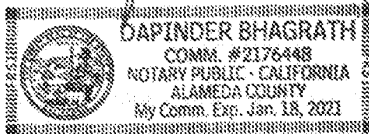
STATE OF CALIFORNIA)
) ss.
COUNTY OF Alameda)

On June 30th, 2017, before me, DAPINDER BHAGRATH, Notary Public in and for said State, personally appeared STEPHEN R. URMATE, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

Signature 

(Seal)



Group No. 1: PowerGuard and Data Recovery				NVM-only. (Volatile RAM + NVM) Solutions
Group No.	Country	Patent Number	Issue/Priority	Title
1	(A) US	6496939**	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System in the event of a power failure
1	(A) Taiwan	189445	2004-02-20 / 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) Canada	2,388,496	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) EP	App. No: 00961417.3	Filed 2002- 04-18 / Priority 1999- 09-21	Method and System for Controlling data in a Computer System
1	(B) US	9,372,755	2106-06-21/ 2011-10-05	Adaptive power cycle sequences for data recovery
1	(B) US	App. No. 15/176,156	Filed 2016- 06-08 / Priority 2011- 10-05	Adaptive power cycle sequences for data recovery
1	US	6,970,890	2005-11-29/ 2000-12-20	Method and apparatus for data recovery

(A & B) Identifies Different Priority Families; All Others Are Single Patents

Group No. 2: Networking+ Flash				Networked-attached Storage Devices (Filesystem / Block IO)
Group No.	Country	Patent Number	Issue/Priority	
2	US	6981070**	2005-12-27/ 2000-07-12 (+552 PTA)	Network storage device having solid-state non-volatile memory
2	US	7,729,370	2010-06-01/ 2005-08-19 (+861 PTA)	Apparatus for networking devices having fibre channel node functionality

Group No. 3: Casings, PCB, and ASIC				SSD/Acceleration Devices/ASIC design
Group No.	Country	Patent Number	Issue/Priority	
3	(C) US	7826243**	2010-11-2 / 2005-12-29 (+747 PTA)	Multiple chip module and package stacking for storage devices
3	(C) US	8093103	2012-1-10 / 2005-12-29	Multiple chip module and package stacking for storage devices
3	(C) Taiwan	I332701853	2010-11-1 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Korea	10-1391068	2014-4-24 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,745,730	2015-04-27 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,859,181	2015-12-08 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) China	101375391B	2010-12-28 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(D) US	6317330	2001-11-13 / 2000-2-15	Printed circuit board assembly
3	(D) China	CN 1423917	2006-02-08 / 2000-2-15	Printed circuit board assembly
3	(D) Israel	151278	2007-06-01 / 2000-2-15	Printed circuit board assembly
3	(D) Taiwan	I228211	2005-02-21 / 2000-2-15	Printed circuit board assembly
3	(D) Japan	4,397,143	2009-10-30 / 2000-2-15	Printed circuit board assembly
3	(E) US	9,423,457	2016-8-23 / 2013-3-14 (+102 PTA)	Self-Test Solution For Delay Locked Loops
3	(E) US	App. No. 15/232,801	Filed 2016- 08-09 / priority 2013- 3-14	Self-Test Solution For Delay Locked Loops
3	(F) US	8665601	2014-3-4 / 2009-9-4 (+500 PTA)	Solid state drive with improved enclosure assembly
3	(F) US	9,552,848	Filed 2014--2- 18 / priority 2010-9-4	Solid state drive with improved enclosure assembly

3	(F) US	App. No. 15/414,504	Filed 2017--1- 24 / priority 2010-9-4	Solid state drive with improved enclosure assembly
3	US	6,744,635	2004-6-1 / 2000-2-15	Removable Visual Indication Structure For A Printed Circuit Board

(C thru F) Identifies Different Priority Families; All Others Are Single Patents

Group No. 4: DMA and Security			Performance, Hardware Acceleration, Security for NVM and Non-NVM	
Group No.	Country	Patent Number	Issue/Priority	
4	US	7716389	2010-05-11 / 2006-03-17	Direct memory access controller with encryption and decryption for non-blocking high bandwidth I/O transactions
4	US	8165301	2012-04-24 / 2006-04-04	Input-output device and storage controller handshake protocol using key exchange for data security
4	US	7620748	2009-11-17 / 2006-04-06	Hardware assisted non-volatile memory-to-input/output direct memory access (DMA) transfer
4	(G) US	9400617	2016-07-26 / 2013-03-15	Hardware-assisted DMA transfer with dependency table configured to permit-in parallel-data drain from cache without processor intervention when filled or drained
4	(G) US	App. No. 15/217,947	Filed 2016-07- 22 / Priority 2013-03-15	Hardware-Assisted DMA Transfer with Dependency
4	(G) US	9672178	2017-06-06 / Priority 2013- 03-15	Bit-Mapped Dependency Table
4	(G) US	App. No. 15/603,434	Filed 2017-05- 23 / Priority 2013-03-15	Bit-Mapped Dependency Table

(G) Identifies A Priority Family; All Others Are Single Patents

Group No. 5: Flash-and-ECC related Patents			SSDs / FlashDevices (Flash, Profile, ECC, Firmware)	
Group No.	Country	Patent Number	Issue/Priority	
5	(H) US	9043669++	2015-05-26 / 2012-05-18	Distributed ECC engine for storage media
5	(H) US	App. No. 14/708,246	Filed 2015- 05-09 / Priority 2012- 05-18	Storage System With Distributed ECC Capability
5	(I) US	8959307++	2015-02-17 / 2007-11-16	Reduced latency memory read transactions in storage devices

5	(I) US	App. No. 14/616,700	Filed 2015-02-02 / Priority 2007-11-16	Memory Transaction With Reduced Latency
5	(I) US	App. No. 14/866,946	Filed 2015-09-26 / Priority 2007-11-16	Reduced latency memory read transactions in storage devices
5	(I) US	App. No. 15/268,533	Filed 2016-09-16 / Priority 2007-11-16	Memory Interface With An Expandable Architecture That Provides Reduced Latency
5	(I) US	App. No. 15/268,536	Filed 2016-09-16 / Priority 2007-11-16	Multi-Dimensional Memory
5	(I) US	App. No. 15/368,598	Filed 2016-12-03 / Priority 2006-11-16	Computer Storage System With Reduced Latency
5	(J) US	7613876++	2009-11-03 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
5	(J) US	8032700++	2011-10-04 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
5	(J) Taiwan	I438628	2014-05-21 / 2006-06-08	DATA STORAGE SYSTEM AND DATA STORAGE MEDIUM
5	(J) Taiwan	I525431	Filed 2014-02-17 / 2006-06-08	Data Storage System, Data Structure and Data Storage Method
5	(N) Taiwan	I420307	2013-12-21 / 2006-06-08	Optimized placement policy for solid state storage devices
5	(N) Taiwan	I540430	2016-07-01 / 2005-06-08	Method for data storage
5	(K) US	9430386++	2016-08-30 / 2013-03-15	Multi-leveled cache management in a hybrid storage system
5	(K) US	App. No. 15/249,475	Filed 2016-08-29 / Priority 2013-03-15	Multi-leveled cache management in a hybrid storage system
5	(K) US	App. No. 14/689,045	Filed 2015-04-16 / Priority 2013-03-15	Write Buffering
5	(L) US	6000006	1999-12-07 / 1997-08-25	UNIFIED RE-MAP AND CACHE-INDEX TABLE WITH DUAL WRITE-COUNTERS FOR WEAR-LEVELING OF NON-VOLATILE FLASH RAM MASS STORAGE

5	(L) US	5822251	1998-10-13 / 1997-09-29	Expandable flash-memory mass-storage using shared buddy lines and intermediate flash-bus between device-specific buffers and flash-intelligent DMA controllers
5	(M) US	9099187	2015-08-04 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
5	(M) US	8560804	2013-10-15 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
5	(M) US	9484103	2016-11-1 / 2009-09-14	Electronic Storage Device
5	(M) US	App. No. 15/269,967	Filed 2016- 09-19 / priority 2009- 09-14	Electronic Storage Device
5	(N) US	8010740	2011-08-30 / 2008-11-25	Optimizing memory operations in an electronic storage device
5	(N) US	7506098	2009-03-17 / 2006-06-08	Optimized placement policy for solid state storage devices
5	(O) US	8447908	2013-04-21 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
5	(O) US	8788725	2014-7-22 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
5	(O) US	App. No. 14/297,628	2014-06-06 / 2009-09-07	Multilevel memory bus system
5	US	6529416	2003-03-04 / 2000-11-30	Parallel erase operations in memory systems
5	US	5956743	1999-09-21 / 1997-09-29	TRANSPARENT MANAGEMENT AT HOST INTERFACE OF FLASH-MEMORY OVERHEAD-BYTES USING FLASH-SPECIFIC DMA HAVING PROGRAMMABLE PROCESSOR-INTERRUPT OF HIGH-LEVEL OPERATIONS
5	US	9135190	2015-09-15 / 2009-09-04	Multi-profile memory controller for computing devices
5	US	6757845	2004-06-29 / 2000-11-30	Method and apparatus for testing a storage device
5	US	Appl. No. 15/482,684	Filed 2017- 04-07	Multi-Dimensional Computer Storage System Note: this application was decided to be filed without any priority claim; option available for this application to be a continuation application that claims benefit to 15/268,536 and/or 15/268,533 (family (I))

(H thru O) Identifies Different Priority Families; All Others Are Single Patents

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	8010740
	Issue Date	08/30/2011
	First Named Inventor	Mark Ian Arcodera
	Title	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
	Attorney Docket No.	150962.00001

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

67942

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

--

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

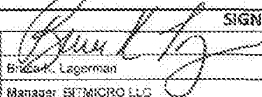
I am the:

☐ Inventor, having ownership of the patent.

OR

☒ Patent owner.

☒ Statement under 37 CFR 3.75(c) (Form PTO/SB/96) submitted herewith or filed on

SIGNATURE of Inventor or Patent Owner		Date	9-30-17
Signature		Date	9-30-17
Name	Brian Lagerman	Telephone	
Title and Company	Manager, BITMICRO LLC		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Bitmicro LLCApplication No./Patent No.: 8010740Filed/Issue Date: 08/30/2011Titled: OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

Bitmicro LLC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: Bitmicro Networks, Inc.The document was recorded in the United States Patent and Trademark Office at
Reel 026574, Frame 0906, or for which a copy thereof is attached.2. From: Bitmicro Networks, Inc. To: Bitmicro, LLCThe document was recorded in the United States Patent and Trademark Office at
Reel 043536, Frame 0407, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Bruce K. Lagerman

Printed or Typed Name

Date

Manager

Title or Registration Number

[Page 2 of 2]

Electronic Acknowledgement Receipt	
EFS ID:	30553200
Application Number:	12323461
International Application Number:	
Confirmation Number:	7802
Title of Invention:	OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE
First Named Inventor/Applicant Name:	Mark Ian ARCEDERA
Customer Number:	64180
Filer:	Raman N. Dewan/Heather Bucek
Filer Authorized By:	Raman N. Dewan
Attorney Docket Number:	6005.007CIP
Receipt Date:	03-OCT-2017
Filing Date:	25-NOV-2008
Time Stamp:	15:11:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		8010740_POA.pdf	3804008	yes	3
			694ed9a95c54a147a06f42b44af3863869e25ea2		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		3804008	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/323,461	11/25/2008	Mark Ian ARCEDERA	150962.00001

CONFIRMATION NO. 7802

POA ACCEPTANCE LETTER

67942
JACKSON WALKER L.L.P.
ATTN: INTELLECTUAL PROPERTY DEPARTMENT
100 CONGRESS AVENUE
SUITE 1100
AUSTIN, TX 78701



Date Mailed: 10/10/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/Itaba/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
12/323,461	11/25/2008	Mark Ian ARCEDERA	150962.00059	70455

Acknowledgement of Change to Small Entity Status

The entity status change request below filed through Private PAIR on 08/24/2018 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

× Applicant asserting small entity status. See 37 CFR 1.27.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
12/323,461	11/25/2008	Mark Ian ARCEDERA	150962.00059	148587

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 09/27/2021 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

☒ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947



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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
12/323,461	8010740	2187	149252

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 183214 on 10/05/2021 via Private PAIR in view of the certification copied below that authorized the change.

- Correspondence Address

The address for Customer Number 183214 is:

183214

Jackson Walker LLP

Bitmicro / Oyster Optics

100 CONGRESS AV

STE 1100

AUSTIN, TX 78701

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947



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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
12/323,461	8010740	2187	149252

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 183214 on 10/05/2021 via Private PAIR in view of the certification copied below that authorized the change.

- Maintenance Fee Address

The address for Customer Number 183214 is:

183214

Jackson Walker LLP

Bitmicro / Oyster Optics

100 CONGRESS AV

STE 1100

AUSTIN, TX 78701

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:22-cv-331	DATE FILED	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF BITMICRO LLC		DEFENDANT KIOXIA AMERICA, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,135,190	9/15/2015	BITMICRO LLC
2 8,010,740	8/30/2011	BITMICRO LLC
3 6,496,939	12/17/2002	BITMICRO LLC
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AF-128 (Rev. 08/16)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court **Western District of Texas** on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

Docket No. 6:22-cv-335	Date Filed 3/30/2022	U.S. District Court Western District of Texas
PLAINTIFF BITMICRO LLC		DEFENDANT INTEL CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,826,243	11/2/2010	BITMICRO LLC
2 9,135,190	9/15/2015	BITMICRO LLC
3 8,010,740	3/30/2011	BITMICRO LLC
4 9,858,084	1/2/2013	BITMICRO LLC
5 10,120,694	11/6/2018	BITMICRO LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY		
	☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
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5			

In the above—entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/16)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.)

DOCKET NO. 6:22-cv-335	DATE FILED 3/30/2022	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF BITMICRO LLC		DEFENDANT INTEL CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6 6,496,939	12/17/2002	BITMICRO LLC
2		
3		
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5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY		
	☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
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3			
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy