Carl Sechen

Professor
Dept. of Electrical Engineering
University of Texas at Dallas
carl.sechen@utdallas.edu
972-835-1611

Research Interests

My research interests center primarily on the design and computer-aided design of digital and analog integrated circuits. Ongoing projects include fast, accurate simulation-based timing analysis. Also, the design of secure ICs that cannot be reverse engineered. One aspect of this is the design of novel types of embeddable field-programmable circuits for design obfuscation. We are also working on reverse engineering of PCBs that are damaged and/or discarded.

Education

Ph.D., Electrical Engineering, University of California, Berkeley, 1986
Thesis: *Placement and Global Routing of Integrated Circuits Using Simulated Annealing*
Advisor: Prof. Alberto Sangiovanni-Vincentelli
M.S., Electrical Engineering, Massachusetts Institute of Technology, 1977
Advisor: Prof. Stephen Senturia
B.E.E., Electrical Engineering, University of Minnesota, 1975

Employment history

Professor, University of Texas at Dallas August 15, 2005 – present
Professor, University of Washington July 1999 – August 14, 2005
Associate Professor, University of Washington July 1992 – June 1999
Associate Professor, Yale University July 1990 – June 1992
Assistant Professor, Yale University July 1986 – June 1990

University Administrative Positions

Director of ECS Tech Support Services, UTD, June 2012 – February 2014

Honors and Awards

- *Best Paper Award* at the 2017 IEEE PhD Research in Microelectronics and Electronics Conference (PRIME), for the paper "Improved Lagrangian Relaxation-based Gate Size and VT Assignment for Very Large Circuits", Bariloche, Argentina, February 2017.
- Nominated for a *Best Paper Award* for: "A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic Reconfiguration", *Proc. of Design Automation and Test in Europe (DATE) Conference*, March 27-31, 2017, Lausanne, Switzerland.
- Nominated for UTD's President's Teaching Excellence Award for Graduate/Professional Instruction, 2020.
- Received the *Distinguished Teaching Award* for the Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2014.
- Received the *Distinguished Teacher of the Year* Award, Dept. of Electrical Engineering, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2008.
- Elected *IEEE Fellow* in 2002
- Received the *Outstanding Research Advisor* Award, Department of Electrical Engineering, University of Washington, 2002.

- Received the *Best Project Award*, NSF Center for the Design of Digital and Analog ICs (CDADIC), July 2002.
- Received the Semiconductor Research Corporation's 2001 *SRC Inventor's Recognition Award*
- Received the Semiconductor Research Corporation's 1994 *SRC Technical Excellence Award*
- Received the Semiconductor Research Corporation's 1988 *SRC Inventor's Recognition Award*

Litigation Support Experience

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Latham Watkins
Case Name:	Cannot disclose
Services Provided:	
Disposition:	pending
Date:	Started August 2021

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Orrick, Herrington, and Sutcliffe
Case Name:	Cannot disclose
Services Provided:	
Disposition:	pending
Date:	Started August 2020

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Anova Law Group, PLLC
Case Name:	Cannot disclose
Services Provided:	
Disposition:	pending
Date:	Started August 2021

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Perkins Coie
Case Name:	Cannot disclose
Services Provided:	
Disposition:	pending
Date:	Started October 2021

Expert Engagement

Type of Matter:	Patent ligitation
Law Firm:	Wilmer Cutler Pickering Hale and Dorr LLP ("WilmerHale")
Case Name:	Civil Action No. 6:19-cv-404-ADA FLASH-CONTROL, LLC, Plaintiff, v. IN-TEL CORPORATION; IN THE UNITED STATES DISTRICT COURT FOR THE WESTERN DISTRICT OF TEXAS AUSTIN DIVISION
Services Provided:	Expert consultation on behalf of Intel
Disposition:	pending
Date:	Started January 2020

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	*Arigna Technology Limited v. Volkswagen AG et al.,* Case No. 2:21-cv-00054-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation and testimony
Disposition:	Pending
Date:	Started 12/06/2020

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	*Arigna Technology Limited v. Bayerische Motoren Werke AG et al.,* Case No. 2:21-cv-00172-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Pending
Date:	Started 12/06/2020

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	*Arigna Technology Limited v. Porsche AG, et al.,* Case No. 2:21-cv-00173-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Pending
Date:	Started 12/06/2020

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	*Arigna Technology Limited v. General Motors Company, et al.,* Case No. 2:21-cv-00174-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Pending
Date:	Started 12/06/2020

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	*Arigna Technology Limited v. Daimler AG, et al.,* Case No. 2:21-cv-00175-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Pending
Date:	Started 12/06/2020

Expert Engagement

Type of Matter:	ITC Investigation
Law Firm:	Susman Godfrey LLP
Case Name:	*In The Matter of Certain Power Inverters and Converters, Vehicles Containing the Same and Components Thereof,* Inv. No. 337-TA-1267 (ITC)
Services Provided:	Expert consultation and testimony
Disposition:	Pending
Date:	Started 12/06/2020

Expert Engagement

Type of Matter:	IPR filing
Law Firm:	Kirkland & Ellis LLP
Case Name:	Case 1:19-cv-01006-UNA IPR PACT XPP Schweiz AG v. Intel Corporation IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE
Services Provided:	Expert consultation toward the filing of an IPR on behalf of Intel
Disposition:	pending
Date:	Started December 2019

Expert Engagement

Type of Matter:	IPR filing
Law Firm:	Wilmer Cutler Pickering Hale and Dorr LLP (WilmerHale)
Case Name:	VLSI Technology, LLC v. Intel Corporation, No. 3:17-cv-05671-BLF (N.D. Cal.), VLSI Technology, LLC v. Intel Corporation, No. 1:18-cv-00966-CFC-CJB (D. Del.) VLSI Technology, LLC v. Intel Corporation, No. 6:19-cv-00256-ADA (W.D. Tex.)
Services Provided:	Two declarations in support of an Intel IPR and two depositions
Disposition:	pending
Date:	Started May 1, 2019, ended July 30, 2020

Expert Engagement

Type of Matter:	Patent infringement and associated IPR filing
Law Firm:	Baker Botts (DC case) and Sterne, Kessler, Goldstein & Fox P.L.L.C. (IPR case)
Case Name:	Case No. 1:18-cv-555-LY UNITED STATES DISTRICT COURT WESTERN DISTRICT OF TEXAS AUSTIN DIVISION POLARIS INNOVATIONS, LTD., an Ireland limited company, Plaintiff, v. ADVANCED MICRO DEVICES, INC
Services Provided:	Filing a declaration in support of the IPR and planning for the district court case
Disposition:	Case dissolved

Date:	Started Febrary 2019; ended May 2020

Expert Engagement

Type of Matter:	Trade secret case before an Arbitration Panel
Law Firm:	Anova Law Group
Case Name:	TVL International LLC v. Zhejiang Shenghui Lighting Co., Ltd. Case No. 01-17-0004-7802 AMERICAN ARBITRATION ASSOCIATION CHARLOTTE, NORTH CAROLINA *In the matter of arbitration between* TVL INTERNATIONAL LLC, Claimant, v . ZHEJIANG SHENGHUI LIGHTING CO., LTD. and SENGLED USA, INC.
Services Provided:	Three expert reports completed, and testimony before the Arbitration Panel
Disposition:	Ended with TVL declared the winner
Date:	April 9, 2018 through August 31, 2018.

Expert Engagement

Type of Matter:	Challenge of Patent Validity
Law Firm:	Weil, Gotshal and Manges; but in the future: Orrick, Herrington & Sutcliffe
Case Name:	North Star Innovations, Inc. v Micron Technology, Inc., et al., Case 17-cv-506-LPS-CJB, D. Del.
Services Provided:	Research in support of an IPR regarding Patent 5,943,274 on behalf of Micron
Disposition:	In progress but no work performed to date
Date:	March 5, 2018 through present

Expert Engagement

Type of Matter:	Challenge of Patent Validity
Law Firm:	Baker Botts
Case Name:	Advanced Micro Devices v. Broadcom
Services Provided:	One declaration in support of an IPR regarding Patent 7,472,151 Case No. Unassigned Patent 7,472,151 _____ DECLARATION OF DR. CARL SECHEN IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,472,151
Disposition:	Settled not long after the IPR was filed
Date:	December 3, 2016 through March 27, 2017

Expert Engagement:

Type of Matter:	Trade Secret Misappropriation
Law Firm:	Wilson Sonsini Goodrich & Rosati

Case Name:	GSI Technology, Inc. v. United Memories, Inc. and Integrated Silicon Solution, Inc.; Case No. 5:13-cv-1081-PSG in the United States District Court for the Northern District of California, San Jose Division
Services Provided:	One declaration on behalf of ISSI, one deposition and one trial testimony before a jury
Disposition:	ISSI was victorious at trial and upon appeal
Date:	May 2014 through November 2015

Expert Engagement:

Type of Matter:	Patent validity – PTO re-examination proceedings
Law Firm:	Bruce Itchkawitz, Knobbe Martens Olson & Bear; Rich Kim, Mehran Arjomand, and David Kim, Morrison & Foerster LLP
Case Name:	Netlist, Inc. vs. Google, Inphi Corp., and Smart Modular Technologies Individual cases in the last 5 years: 1. *Inter Partes* Review No. IPR2017-00667 2. *Inter Partes* Review No. IPR2017-00549 3. *Inter Partes* Review No. IPR2017-00692 4. *Inter Partes* Review No. IPR2017-00562 5. *Inter Partes* Review No. IPR2017-00561 6. *Inter Partes* Review No. IPR2017-00587 7. *Inter Partes* Review No. IPR2017-00560 8. Appeal No. 2015-006849 9. Appeal No. 2015-007761 10. *Inter Partes* Review No. 2015-01021 11. Reexamination Control No.: 95/001,337 12. *Inter Partes* Review No. IPR2014-0097 13. *Inter Partes* Review No. IPR2014-00970 14. *Inter Partes* Review No. IPR2014-01011 15. *Inter Partes* Review No. IPR2014-00883 16. *Inter Partes* Review No. IPR2014-00883 17. Appeal No. 2013-009044
Services Provided:	25 declarations, 5 depositions on behalf of Netlist, Inc., filed July 2011 through May 2015 supporting patent validity challenges before the PTO Worked on 6 separate IPR's, each involved writing an expert report and giving a deposition.
Disposition:	Pending
Date:	June 28, 2011 through March 2018

Expert Engagement:

Type of Matter:	Patent invalidity and patent non-infringement
Law Firm:	Wilson Sonsini Goodrich & Rosati (representing the defendant)
Case Name:	HSM Portfolio, LLC, Technology Properties Limited, LLC v. Advanced Micro Devices (defendant) Case: 1:11-cv-00770-RGA (D. Del.)
Services Provided:	Work toward declaration on patent non-infringement
Disposition:	Settled in defendant's favor
Date:	April 2013 through December 2013

Expert Engagement:

Type of Matter:	Patent non-infringement
Law Firm:	Jones Day (representing the defendant)
Case Name:	Intellectual Ventures v. Xilinx (defendant) IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, Plaintiffs, v. ALTERA CORPORATION, MICROSEMI CORPORATION, LATTICE SEMICONDUCTOR CORPORATION and XILINX, INC., Defendants. C.A. No. 10-1065 (LPS) (CONSOLIDATED)
Services Provided:	One declaration on patent non-infringement; one deposition
Disposition:	Settled in defendants' favor
Date:	February 2013 through April 2014

Expert Engagement:

Type of Matter:	Patent non-infringement
Law Firm:	Morrison Foerster (representing the defendant)
Case Name:	Intellectual Ventures v. Altera (defendant) IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, Plaintiffs, v. ALTERA CORPORATION, MICROSEMI CORPORATION, LATTICE SEMICONDUCTOR CORPORATION and XILINX, INC., Defendants. C.A. No. 10-1065 (LPS) (CONSOLIDATED)
Services Provided:	One declaration on patent non-infringement; one deposition
Disposition:	Settled in defendant's favor
Date:	February 2013 through December 2013

Expert Engagement:

Type of Matter:	Patent validity and patent infringement
Law Firm:	Antonelli, Harrington & Thompson LLP
Case Name:	Guardian Media Technologies, Ltd., Plaintiff, v. Acer America Corp, et al., Defendants.

	Cases: CIVIL ACTION NO. 6:10-CV-597-LED Case No. 2:13-CV-08369 PSG (PLAx)
Services Provided:	One declaration on patent validity and two declarations on patent infringement
Disposition:	Settled in Plaintiff's favor
Date:	February 2013 through March 2015

Expert Engagement:

Type of Matter:	Patent infringement
Law Firm:	Winston & Strawn (Nanya)
Case Name:	On Technologies vs. Nanya
Services Provided:	Work on claim term definitions
Disposition:	Case was transferred from East. Dis. Texas to No. Calif. in late 2010; then settled
Date:	March 2010 through October 2010

Expert Engagement:

Type of Matter:	Patent infringement
Law Firm:	White and Case (Panasonic)
Case Name:	Freescale Semiconductor vs. Panasonic
Services Provided:	Invalidity and non-infringement expert reports filed November 2010; deposition December 2, 2010
Disposition:	ITC case settled January 2011
Date:	April 2010 through January 2011

Expert Engagement:

Type of Matter:	Patent infringement
Law Firm:	Weil, Gotshal and Manges (Samsung)
Case Name:	Rambus vs. Samsung
Services Provided:	One Declaration, One Deposition, and one trial testimony for Samsung **Declaration:** This report overviewed Rambus technology and patents, their alleged "steering" of patent claims, and Samsung's subsequent DDR products. **Deposition:** Dr. Sechen was asked to consider whether Samsung's subsequent DDR products, DDR2, DDR3, GDDR, GDDR2, GDDR3, and GDDR4 fell within the scope of their 2000 license agreement with Rambus. Representing attorney: Matt Antonelli. **Trial Testimony:** Dr. Sechen testified before Judge Ronald Whyte, San Jose, CA, that Samsung's subsequent DDR products, DDR2, DDR3, GDDR, GDDR2, GDDR3, and GDDR4 fell within the scope of their 2000 license agreement with Rambus. Representing attorney: Matt Antonelli.
Disposition:	Dr. Sechen's involvement completed on 30 September 2008 with the conclusion of the trial.

Date:	May 2008 through September 2008

Expert Engagement:

Type of Matter:	Patent infringement
Law Firm:	O'Melveny & Myers (Magma)
Case Name:	Synopsys vs. Magma Design Automation
Services Provided:	Two Declarations, One Supplemental Declaration and Two Depositions for Magma **Declaration**: June 10, 2005: Dr. Sechen illustrated that the material in the Synopsys patents (originally patented by Magma, but awarded to Synospys by the court) were put into the public domain by Magma. In addition, he illustrated that the material in the Synopsys patents were generally in the public domain prior to the patents. **Declaration**: Dr. Sechen wrote a declaration supporting Magma's proposed claim constructions for the two patents involved on July 21, 2005. **Supplemental Declaration**: July 13, 2005 Dr. Sechen had a supplemental declaration showing that Synopsys' expert report in fact was consistent and in agreement with his first declaration. **Deposition**: Aug. 10, 2005: Dr. Sechen was deposed on the July 21, 2005 declaration. Representing attorney: Mark Miller. **Deposition**: Dec. 16, 2005: Dr. Sechen was deposed on the June 10, 2005 declaration and on the supplemental declaration of July 13, 2005. Representing attorney: Mark Miller.
Disposition:	Settled after court made several rulings in Magma's favor
Date:	Started January 2005; Ended January 2006

Expert Engagement:

Type of Matter:	Trade Secret Misappropriation and Patent Enforcement
Law Firm:	Susman Godfrey
Case Name:	UniRAM Technology vs. Monolithic System Technology and TSMC
Services Provided:	3 Expert Reports, 1 Declaration and 2 Depositions, and 2 trial testimonies for UniRAM. **Expert Report**: May 19, 2005: Expert report covered claim construction issues **Declaration**:

	May 19, 2005: Declaration in support of plaintiff UniRAM's response to TSMC's motion for summary judgment of inequitable conduct. (Subject of the 2nd trial testimony.) **Expert Report**: May 31, 2007: Expert report that concluded that the UniRAM trade secrets were not and are not generally known, and that the UniRAM trade secrets created significant value for the defendants. **Expert Rebuttal Report**: Expert rebuttal report filed on June 13, 2007. **Deposition**: June 21, 2005: Deposition concerning expert report of May 19, 2005. Representing attorney: Russ Chorush. **Deposition**: June 28, 2007: Deposition regarding expert report of May 31, 2007 and to a lesser degree the May 19, 2005 declaration. Representing attorney: Russ Chorush. **Trial Testimony**: September 2007 trial concerning Dr. Sechen's expert report of May 31, 2007. Representing attorneys: Russ Chorush (Heim, Payne and Chorush) and Joseph Grinstein (Susman Godfrey). **Trial Testimony**: January 2008 regarding my declaration of May 19, 2005. Representing attorneys: Russ Chorush (Heim, Payne and Chorush) and Joseph Grinstein (Susman Godfrey). The presiding judge specifically commented on Dr. Sechen's credibility in his final judgment.
Disposition:	$32 million judgment for UniRAM
Date:	Started February 2005; Ended January 15, 2008

Expert Engagement:

Type of Matter:	Patent validity and infringement (both to PTO and trial)
Law Firm:	Squire, Sanders and Dempsey (Hitachi)
Case Name:	Translogic vs. Hitachi
	4 expert reports, 2 declarations, 1 deposition and trial testimony for Hitachi **Expert Disclosure Statement**: Expert disclosure statement of July 25, 2003. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively "Hitachi") to compare claims of U.S. Patent No. 5,162,666 ("the '666 Patent") with certain technical references which were prior art to the

	‘666 Patent. Plaintiff Translogic Technology, Inc. (“Translogic”) asserted claims of the ‘666 Patent against Hitachi. **Supplemental Expert Disclosure**: Supplemental expert disclosure statement of September 19, 2003. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively “Hitachi”) to compare claims of U.S. Patent No. 5,162,666 with certain technical references which were prior art. Dr. Sechen supplemented the Expert Disclosure Statement he previously submitted in this case based on his review of the Report and Recommendation of Special Master Regarding Claim Construction. **Expert Disclosure Statement**: Expert disclosure statement of February 9, 2004. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively “Hitachi”) to analyze certain circuits in Hitachi microprocessors that Translogic Technology, Inc. (“TTI”) accuses of infringing Patent No. 5,162,666 (“the ‘666 Patent”). Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products. **Supplemental and Restated Expert Disclosure Statement:** Supplemental and restated expert disclosure statement of September 20, 2004. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively “Hitachi”) to analyze certain circuits in Hitachi microprocessors that Translogic Technology, Inc. (“TTI”) accuses of infringing Patent No. 5,162,666 (“the ‘666 Patent”). Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products. This report supplements my earlier expert disclosure statement, however, it is written as a substitute for that earlier report. This revision now uses the multiplexer drawing convention used by Hitachi, which is different from the standard U.S. convention. **Declaration in Opposition to Plaintiff’s Motion for Summary Judgment**: Declaration in opposition to plaintiff’s motion for summary judgment, April 2004. Dr. Sechen was asked to analyze certain circuits in Hitachi microprocessors that Translogic Technology accused of infringing their patent No. 5,162,666. Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products. **Second Declaration in Opposition to Plaintiff’s Motion for Summary Judgment**: Second declaration in opposition to plaintiff’s motion for summary judgment, September 20, 2004. Dr. Sechen was asked to analyze certain circuits in Hitachi microprocessors that Translogic Technology accused of infringing their patent No. 5,162,666. Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products. **Deposition**:

	Aug. 18, 2003: Dr. Sechen was deposed on all of the above-mentioned expert disclosures and declarations. Representing attorneys: Nathan Lane and David Elkins of Squire, Sanders and Dempsey, as well as Alan Loudermilk of Loudermilk Associates. **Trial Testimony**: January 2004: Representing attorneys: Nathan Lane and David Elkins of Squire, Sanders and Dempsey, as well as Alan Loudermilk of Loudermilk Associates.
Disposition:	Concluded, PTO ruled in favor of Hitachi but court ruled in favor of Translogic.
Date:	July 2003 to September 2004

Expert Engagement:

Type of Matter:	Trade Secret Theft
Law Firm:	Keker and Van Ness (Cadence)
Case Name:	Cadence vs. Avanti
Services Provided:	Two Declarations and One Deposition for Cadence **Declaration**: Short declaration that verified and substantiated the findings of other Cadence experts. **Declaration**: Dr. Sechen submitted a very long reply declaration that compared an Avanti software product to a Cadence software product, and showing that the products were not in the public domain. **Deposition**: Deposition focused primarily on the reply declaration. Representing attorney: Michael Page.
Disposition:	Concluded
Date:	July 1995 to July 1996

Graduated Ph.D. Students

1. Kai-Win Lee (Yale May 1990) "Global Routing of Row-Based Integrated Circuits".
2. Dahe Chen (Yale May 1992) "Mickey: A Graph-Based Macro-Cell Global Router".
3. Mark Chiang (Yale May 1992) "A Perturbation Approach to the Symbolic Analysis of Analog Circuits".
4. William Swartz (Yale May 1993) "Automatic Layout of Analog and Digital Mixed Macro/Standard Cell Integrated Circuits".
5. Ted Stanion (Yale May 1994) "Boolean Algorithms for Combinational Synthesis and Test Generation".
6. Kalapi Roy (University of Washington June 1994) "A Timing-Driven Multi-Way Partitioning System for Integrated Circuits and Multi-Chip Systems".
7. Jer-Jaw Hsu (University of Washington December 1994) "Fully Symbolic Analysis of Large Analog Integrated Circuits".
8. Wern-Jieh Sun (University of Washington December 1994) "Effective and Efficient Placement for Very Large Integrated Circuits".
9. Qicheng Yu (University of Washington March 1995) "Approximate Symbolic Analysis of Large Analog Integrated Circuits".
10. Bingzhong David Guan (University of Washington August 1996) "Automatic Layout Generation of Static CMOS Combinational Cells and Blocks".
11. Eugene Liu (University of Washington, December 1997) "Global Routing and Pin Assignment for Multi-layer Chip-level Layout".
12. Hsiao-Ping Tseng (University of Washington, December 1997) "Detailed Routing Algorithms for VLSI Circuits".
13. Gin Yee (University of Washington, June 1999) "Dynamic Logic Design and Synthesis Using Clock-Delayed Domino".
14. Tyler Thorp (University of Washington, December 1999), "Design and Synthesis of Dynamic Circuits".
15. Tatjana Serdar (University of Washington, December 2000), "Automatic Datapath Tile Placement and Routing".
16. Jovanka Ciric (University of Washington, August 2001), "Boolean Matching and Level-Based Technology Mapping".
17. Yi Han (University of Washington, December 2004), "A High-Performance CMOS Programmable Logic Core for System-on-Chip Applications".
18. Hiran Tennakoon (University of Washington, August 2005), "Efficient and Accurate Gate Sizing With Piecewise Convex Delay Models".
19. Miodrag Vujkovic (University of Washington, March 2006), "Efficient Fully-Automated, Refinement-Based Power-Delay Optimization Design Flow for Standard Cell Designs".
20. Kian Hour (Alfred) Chong (University of Washington, June 2006), "Self-Calibrating Differential Output Prediction Logic".
21. Xinyu (Sunny) Guo (University of Washington, June 2006), " A High-Throughput Divider Based on Output Prediction Logic".
22. Sheng Sun (University of Washington, August 2006), "High Performance and Energy Efficient Adder Design".
23. Mohammad Rahman (UT-Dallas, December 2011), "Power and Leakage Minimization for Digital ICs".
24. Chiu-Wei Pan (UT-Dallas, August 2012), "High Speed and Power Efficient Compression of Partial Products".
25. Zhao Wang (UT-Dallas, October 2012), "Accurate Wire Endpoint Delay Estimation".
26. Akshay Sridharan (UT-Dallas, October 2015), "STARK: Synchronous to Asynchronous Redesign Kit".
27. Anitha Yella (UT-Dallas, January 2016), "Power Optimization in ICs".

28. Meisam Roshan (UT-Dallas, September 2016), "A MEMS-Assisted Dual-Resonator Temperature-to-Digital Converter".
29. Huihua (Helen) Huang (UT-Dallas, May 2018), "A 0.1ps Resolution Coarse-Fine Time-to-Digital Converter with 2.21ps Single-Shot Precision".
30. Jingxiang (Amelie) Tian (UT-Dallas, December 2019), "Transistor-level Programmable Fabric".
31. Bo Hu (UT-Dallas, March 2021), "Thermal-Aware Placement and High Level Synthesis For Hardware Security".
32. Lubaba Nahar, (UT-Dallas, July 2022), "CAD Tools for PCB Reverse Engineering and IC Interconnect".
33. Qiongdan (Olivia) Huang, (UT-Dallas, July 2022), "Toward Accurate Timing Analysis of Transistor-Level Programmable Fabric".
34. Xiangyu Xu, (UT-Dallas December 2022), "Routing Methods for Transistor-level Programmable Fabrics".

Current Ph.D. Students

1. Vibhav Kumarswami Salimath, Ph.D. expected 12/23
2. Apurva Jain, Ph.D. expected 12/23
3. Thomas Broadfoot, Ph.D. expected 12/23
4. Jinkun Feng, Ph.D. expected 06/26
5. Amir Hossein Torabi, Ph.D. expected 05/27

Teaching Activities

Yr	*Qtr*	*Course*	*Brief Title, Credits, #students*	*Stud. Opin. Survey*
1992	Aut	EE538	Auto Layout, 4 credits, 20 students	4.38/4.08
1993	Win	EE356	Analog ICs, 4 credits, 55 students	3.21/3.00
1993	Spr	EE535	VLSI Design, 4 credits, 25 students	4.27/4.47
1993	Sum	EE332	Analog ICs, 5 credits, 35 students	3.57/3.48
1993	Aut	EE538	Auto Layout, 4 credits, 15 students	3.60/3.50
1993	Aut	EE332	Analog ICs, 5 credits, 40 students	3.93/3.90
1994	Win	EE433	Analog MOS ICs, 4 credits, 65 students	3.96/4.08
1994	Spr	EE476	Digital ICs, 5 credits, 55 students	3.89/3.89
1994	Aut	EE538	Auto Layout, 4 credits, 15 students	3.63/3.63
1994	Aut	EE433	Analog MOS ICs, 4 credits, 55 students	4.32/4.30
1995	Win	EE476	Digital ICs, 5 credits, 85 students	3.75/3.85
1995	Spr	EE473	Adv. Analog MOS, 5 credits, 45 students	3.53/3.59
1995	Aut	EE476	Digital ICs, 5 credits, 85 students	4.40/4.20
1996	Win	EE535	VLSI Design, 4 credits, 55 students	4.10/4.00
1996	Spr	EE538	Auto Layout, 4 credits, 15 students	4.30/4.50
1996	Aut	EE476	Digital ICs, 5 credits, 125 students	3.40/3.40
1997	Win	EE477	Custom Dig ICs, 4 credits, 45 students	4.30/4.10
1997	Win	EE541	Auto Layout, 4 credits, 20 students	4.70/4.70

1997	Spr	EE535	VLSI Design, 4 credits, 20 students	3.83/4.00
1997	Aut	EE476	Digital ICs, 5 credits, 60 students	3.88/3.89
1998	Win	EE477	Custom Dig ICs, 4 credits, 60 students	3.66/3.61
1998	Spr	EE476	Digital ICs, 5 credits, 60 students	3.39/3.50
1998	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.57/3.94
1998	Aut	EE476	Digital ICs, 5 credits, 35 students	4.15/4.50
1999	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.00/3.94
1999	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.79/4.13
1999	Aut	EE476	Digital ICs, 5 credits, 50 students	4.70/4.70
2000	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.53/4.27
2000	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	4.35/4.44
2000	Aut	EE476	Digital ICs, 5 credits, 125 students	4.20/4.19
2001	Win	EE477	VLSI II, 5 credits, 75 students	4.30/4.37
2001	Win	EE525	VLSI II, 5 credits, 25 students	4.25/4.50
2001	Spr	EE526	VLSI III, 4 credits, 50 students	4.35/4.50
2001	Aut	EE476	VLSI I, 5 credits, 150 students	4.1/4.2
2002	Win	EE477	VLSI II, 5 credits, 75 students	4.1/4.1
2002	Win	EE525	VLSI II, 5 credits, 25 students	4.1/4.1
2002	Spr	EE526	VLSI III, 4 credits, 50 students	3.6/3.3
2002	Aut	EE476	VLSI I, 5 credits, 150 students	3.7/3.6
2003	Win	EE477	VLSI II, 5 credits, 55 students	3.4/3.8
2003	Win	EE525	VLSI II, 5 credits, 25 students	3.6/3.3
2003	Spr	EE526	VLSI III, 4 credits, 32 students	3.3/3.5
2003	Aut	EE476	VLSI I, 5 credits, 30 students	4.5/4.6
2004	Win	EE477	VLSI II, 5 credits, 12 students	3.2/3.7
2004	Win	EE525	VLSI II, 5 credits, 7 students	2.2/2.2
2004	Spr	EE526	VLSI III, 4 credits, 12 students	3.2/3.2
2004	Aut	EE476	VLSI I, 5 credits, 65 students	3.8/3.9
2005	Fall	EE6325	VLSI Design, 3 units, 42 students	4.4/4.6
2006	Spr	EE7325	Advanced VLSI Design, 3 units, 20 students	4.5/4.3
2006	Fall	EE6325	VLSI Design, 3 units, 66 students	4.4/4.2
2007	Spr	EE7325	Advanced VLSI Design, 3 units, 15 students	4.5/4.2
2007	Fall	EE6325	VLSI Design, 3 units, 40 students	4.8/4.6
2008	Spr	EE4325	Introduction to VLSI Design, 40 students	3.5/3.4
2008	Spr	EE7325	Advanced VLSI Design, 3 units, 19 students	4.6/4.4
2008	Sum	EE6325	VLSI Design, 3 units, 36 students	4.0/3.7
2008	Fall	EE6325	VLSI Design, 3 units, 40 students	4.1/4.1
2009	Spr	EE4325	Introduction to VLSI Design, 22 students	4.2/3.9
2009	Spr	EE7325	Advanced VLSI Design, 3 units, 37 students	3.7/3.6
2009	Sum	EE6325	VLSI Design, 3 units, 17 students	4.1/4.0
2009	Fall	EE6325	VLSI Design, 3 units, 67 students	4.3/4.0
2010	Spr	EE4325	Introduction to VLSI Design, 25 students	4.6/4.5
2010	Spr	EE7325	Advanced VLSI Design, 3 units, 35 students	4.4/4.4
2010	Sum	EE6325	VLSI Design, 3 units, 17 students	4.7/4.5
2010	Sum	EE3320	Digital Circuits, 3 units, 17 students	4.1/3.8
2010	Fall	EE6325	VLSI Design, 3 units, 77 students	4.4/4.2
2011	Spr	EE4325	Introduction to VLSI Design, 37 students	4.0/4.1
2011	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.2/4.2
2011	Sum	EE6325	VLSI Design, 3 units, 16 students	4.14
2011	Sum	EE3320	Digital Circuits, 3 units, 26 students	4.13
2011	Fall	EE6325	VLSI Design, 3 units, 91 students	4.73

2012	Spr	EE4325	Introduction to VLSI Design, 27 students	4.25
2012	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.90
2012	Sum	EE6325	VLSI Design, 3 units, 35 students	4.46
2012	Sum	EE3311	Electronic Circuits, 3 units, 22 students	3.62
2012	Fall	EE6325	VLSI Design, 3 units, 144 students	4.76
2013	Spr	EE6325	VLSI Design, 3 units, 41 students	4.85
2013	Spr	EE4325	Introduction to VLSI Design, 7 students	4.75
2013	Sum	EE7325	Advanced VLSI Design, 3 units, 67 students	4.38
2013	Sum	EE3311	Electronic Circuits, 3 units, 46 students	4.58
2013	Fall	EE6325	VLSI Design, 3 units, 129 students	4.64
2014	Spr	EE4325	Introduction to VLSI Design, 25 students	4.69
2014	Sum	EE7325	Advanced VLSI Design, 3 units, 74 students	4.53
2014	Sum	EE3311	Electronic Circuits, 3 units, 40 students	4.75
2014	Fall	EE6325	VLSI Design, 3 units, 139 students	4.79
2015	Spr	EE4325	Introduction to VLSI Design, 25 students	4.72
2015	Sum	EE7325	Advanced VLSI Design, 3 units, 49 students	4.25
2015	Sum	EE3311	Electronic Circuits, 3 units, 25 students	4.80
2015	Fall	EE6325	VLSI Design, 3 units, 142 students	4.73
2016	Spr	EE4325	Introduction to VLSI Design, 25 students	3.67
2016	Sum	EE7325	Advanced VLSI Design, 3 units, 70 students	4.77
2016	Sum	EE3311	Electronic Circuits, 3 units, 35 students	4.88
2016	Fall	EE6325	VLSI Design, 3 units, 140 students	4.79
2017	Spr	EE4325	Introduction to VLSI Design, 32 students	4.10
2017	Sum	EE7325	Advanced VLSI Design, 3 units, 30 students	4.88
2017	Sum	EE3311	Electronic Circuits, 3 units, 32 students	4.50
2017	Fall	EE6325	VLSI Design, 3 units, 80 students	4.82
2018	Spr	EE4325	Introduction to VLSI Design, 32 students	4.63
2018	Sum	EE7325	Advanced VLSI Design, 3 units, 30 students	4.88
2018	Fall	EE6325	VLSI Design, 3 units, 80 students	4.88
2019	Spr	EE4325	Introduction to VLSI Design, 43 students	4.33
2019	Sum	EE3311	Electronic Circuits, 3 units, 61 students	4.23
2019	Fall	EE6325	VLSI Design, 3 units, 60 students	4.84
2020	Spr	EE4325	Introduction to VLSI Design, 33 students	4.75
2020	Sum	EE3311	Electronic Circuits, 3 units, 29 students	4.30
2020	Fall	EE6325	VLSI Design, 3 units, 43 students	4.65
2020	Fall	EE7325	Advanced VLSI Design, 3 units, 16 students	4.17
2021	Spr	EE4325	Introduction to VLSI Design, 41 students	3.40
2021	Sum	EE3311	Electronic Circuits, 3 units, 29 students	4.20
2021	Fall	EE6325	VLSI Design, 3 units, 72 students	4.75
2022	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.17
2022	Spr	EE4325	Introduction to VLSI Design, 46 students	4.13
2022	Sum	EE3311	Electronic Circuits, 3 units, 29 students	-----
2022	Fall	EE6325	VLSI Design, 3 units, 111 students	4.20

Course Development

U. of Washington: EE 541 Automatic Layout of Integrated Circuits (first offering: Fall 1992)
U. of Washington: EE 477 Custom Digital CMOS Circuit Design (first offering: Win 1997)
U. of Washington: EE 476 Digital Integrated Circuit Design (first offering: Spr 1994)

Yale University: EE 880 Automatic Layout of Integrated Circuits.

Yale University: EE 877 Introduction to VLSI CAD Tools
Yale University: EE 878 Introduction to VLSI Synthesis
Yale University: EE 988 Analog Integrated Circuits II

Journal Publications

1. Roshan, C. Sechen, *et al*., "A MEMS-Assisted Temperature Sensor with 20μK Resolution, Conversion Rate of 200S/s and FOM of 0.04pJK", *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 185-197, January 2017.
2. Z. Wang, X. He, and C. Sechen, "A New Approach for Gate-Level Delay-Insensitive Asynchronous Logic", *Journal of Circuits, Systems & Signal Processing*, October 2014.
3. Z. Wang, C. Pan, Y. Song, and C. Sechen, "High-Throughput Digital IIR Filter Design", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 2, pp. 15-27, April 2014.
4. C. Pan, Z. Wang and C. Sechen, "High Speed and Power Efficient Compression of Partial Products and Vectors," *Journal of Algorithms and Optimization (JAO)*, Vol. 1, No. 1, pp. 39-54, October 2013.
5. Z. Wang and C. Sechen, "A New Algorithm for Accurate Wire Endpoint Delay Estimation", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 1, pp. 30-43, Jan. 2014.
6. M. Rahman, H. Tennakoon, and C. Sechen, "Library-Based Cell-Size Selection using Extended Logical Effort", *IEEE Trans. on Computer-Aided Design*, July 2013.
7. H. Tennakoon and C. Sechen, "Non-convex Gate Delay Modeling and Delay Optimization," *IEEE Trans. on Computer-Aided Design*, Vol. 27, No. 9, September 2008, pp. 1583-1594.
8. Don Bouldin, Warren Snapp, Paul Haug, Dave Sunderland, Roger Brees, Carl Sechen, and Wayne Dai, "Automated Design of Digital Signal Processing ASICs," *IEEE Circuits and Devices*, vol. 20, n. 4, pp. 17-21, July 2004.
9. J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *IEEE Trans. on Computer-Aided Design*, Vol. 22, No. 5, May 2003, pp. 535-544.
10. T. Thorp and C. Sechen, "Design and Synthesis of Dynamic Circuits," *IEEE Transactions on VLSI Systems*, Vol. 11, No. 1, February 2003, pp. 141-149.
11. G. Hoyer, G. Yee and C. Sechen, "Locally-Clocked Pipelines and Dynamic Logic," *IEEE Transactions on VLSI Systems*, Vol. 10, No. 1, February 2002, pp. 58-62.
12. H. P. Tseng, L. Scheffer and C. Sechen, "Timing- and Crosstalk-Driven Area Routing," *IEEE Transactions on Computer Aided Design*, vol. 20, no. 4, pp. 528-544, April 2001.
13. G. Yee and C. Sechen, "Clock-Delayed Domino for Dynamic Circuit Design," *IEEE Transactions on VLSI Systems*, Vol. 8, No. 4, August 2000, pp. 425-431.
14. L. Liu and C. Sechen, "Multi-layer Chip-level Global Routing Using an Efficient Graph-based Steiner Tree Heuristic," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
15. L. Liu and C. Sechen, "Multi-layer Pin Assignment for Macro Cell Circuits", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
16. H. P. Tseng and C. Sechen, "A Gridless Multi-Layer Router for Standard Cell Circuits using CTM Cells," *IEEE Transactions on Computer Aided Design*, Vol. 18, No. 10, October 1999.

17. W. Sun and C. Sechen, “A Parallel Standard Cell Placement Algorithm,” *IEEE Transactions on Computer Aided Design*, vol. 16, no. 11, November 1997, pp. 1342-1357.
18. Q. Yu and C. Sechen, “Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms,” *IEEE Transactions on Computer Aided Design*, vol. 16, no. 10, October 1997, pp. 1073-1081.
19. Q. Yu and C. Sechen, “Generation of Color-Constrained Spanning Trees with Application in Symbolic Analysis,” *Int. Journal of Circuit Theory and Applications*, Vol. 24, No. 5, pp. 597-603, 1996.
20. Q. Yu and C. Sechen, “A Unified Approach to the Approximate Symbolic Analysis of Large Analog Integrated Circuits,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 43, No. 8, pp. 656-669, August 1996.
21. K. Roy and C. Sechen, “A Timing-Driven Partitioning System for Multiple FPGAs,” *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 309-328, 1996.
22. K. Roy, D. Guan and C. Sechen, “A Sea-of-Gates Style FPGA Placement Algorithm,” *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 293-307, 1996.
23. T. Stanion, D. Bhattacharya, and C. Sechen, “An Efficient Method for Generating Exhaustive Test Sets,” *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 12, December 1995.
24. W. Sun and C. Sechen, “Efficient and Effective Placement for Very Large Circuits,” *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 3, pp. 349-359, March 1995.
25. J. J. Hsu and C. Sechen, “DC Small Signal Symbolic Analysis of Large Analog Integrated Circuits,” *IEEE Transactions on Circuits and Systems I*, Vol. 41, No. 12, pp. 817-828, December 1994.
26. T. Stanion and C. Sechen, “Boolean Division and Factorization Using Binary Decision Diagrams,” *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 9, September 1994, pp. 1179-1184.
27. C. Sechen, “Chip-Planning, Placement, and Global Routing of Macro Cell Integrated Circuits Using Simulated Annealing,” *Int. J. Computer-Aided VLSI Design*, vol. 2, no. 2, 1990, pp. 127-158.
28. C. Sechen, D. Braun, and A. Sangiovanni-Vincentelli, “ThunderBird: A Complete Standard Cell Layout Package,” *IEEE J. of Solid State Circuits*, vol. 23, n. 2, pp. 410- 420, April 1988.
29. C. Sechen and A. Sangiovanni-Vincentelli, “The TimberWolf Placement and Routing Package,” *IEEE J. of Solid State Circuits*, vol. 20, n. 2, April 1985, pp. 510-522.
30. C. Sechen, “An Improved Lock Layer Transistor,” *Solid State Electronics*, Vol. 21, No. 6, June 1978, pp. 911-913.
31. S. Senturia and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Transactions on Electron Devices,* vol.24, no.9, p.1207, September 1977.
32. S. Senturia, C. Sechen, and J. Wishneusky, “The Charge-Flow Transistor: A New MOS Device,” *Applied Physics Letters*, Vol. 30, No. 2, Jan. 1977, p. 106-108.

Fully Refereed Conference Proceedings

1. A. Jain, T. Broadfoot, Y. Makris, and C. Sechen, "Quo Vadis Signal? Automated Directionality Extraction for Post-Programming Verification of a Transistor-Level Programmable Fabric", *Proc. Design Automation and Test in Europe (DATE) Conference*, Antwerp, Belgium, April 17-19, 2023.
2. V. Salimath and C. Sechen, "Essential Standard Cell Library Composition", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022),* June 17-19, 2022, Dallas, TX.
3. L. Nahar, J. Rajendran, Y. Makris and C. Sechen, "MTBoM: Metal Trace to Bill of Materials Generation for PCB Reverse Engineering", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022),* June 17-19, 2022, Dallas, TX.
4. Q. Huang, J. Tian, T. Broadfoot, X. Xu, B. Hu, M. Shihab, A. Jain, V. Salimath, Y. Makris and C. Sechen", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022),* June 17-19, 2022, Dallas, TX.
5. M. Shihab, J. Tian, G. Reddy, B. Hu, W. Swartz Jr., B. Schaefer, C. Sechen and Y. Makris, "CASPER: CAD Framework for a Novel Transistor-Level Programmable Fabric", *Proc. IEEE International Symposium on Circuits & Systems (ISCAS)*, May 17-20, 2020, Seville, Spain.
6. V. Salimath and C. Sechen, "Optimal Standard Cell Library Composition for 7nm", *Proc. IEEE International Symposium on Circuits & Systems (ISCAS)*, May 17-20, 2020, Seville, Spain.
7. M. Shihab, B. Ramanidharan, S. Tellakula, G. Reddy, J. Tian, C. Sechen, and Y. Makris, "ATTEST: Application-Agnostic Testing of a Novel Transistor-Level Programmable Fabric", *Proc. 8th IEEE VLSI Test Symposium (VTS'20)*, April 5-8, 2020, San Diego, CA.
8. M. Shihab, J. Tian, G. Reddy, B. Hu, W. Swartz Jr., B. Schaefer, C. Sechen and Y. Makris, "A Transistor-Level Fabric for Design Obfuscation", *Proc. Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, March 16-19, 2020, San Diego, CA.
9. B. Hu, M. Shihab, Y. Makris, B. Schaefer and C. Sechen, "An Efficient MILP-Based Aging-Aware Floorplanner for Multi-Context Coarse-Grained Runtime Reconfigurable FPGAs", *Proc. Design Automation in Europe Conference (DATE)*, March 9-13, 2020, Grenoble, France.
10. B. Hu, M. Shihab, Y. Makris, B. Schaefer and C. Sechen, "Extending the Lifetime of Coarse-grained Runtime Reconfigurable FPGAs by Balancing Processing Element Usage", *2019 International Conference on Field-Programmable Technology (FPT'19*), December 9-13, 2019 Tianjin, China.
11. S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, *et al*., "Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project", *Proc. ACM/IEEE Design Automation Conference (DAC)*, June 4-6, 2019, Las Vegas, NV.
12. B. Hu, J. Tian, M. Shihab, G. Reddy, W. Swartz, Y. Makris, B. Schaefer, and C. Sechen, "Functional Obfuscation of Hardware Accelerators through Selective Partial Design Extraction onto an Embedded FPGA", *Proc. Great Lakes Symposium on VLSI (GLSVLSI)*, Washington, D.C., USA, May 9-11, 2019.
13. S. Sapatnekar, L. Saul, C. Sechen, *et al*., "OpenROAD: Toward a Self-Driving, Open-Source Digital Layout Implementation Tool Chain", *Proc. Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, March 25-28, 2019, Albuquerque, NM, pp. 1105-1110.
14. M. Shihab, G. Reddy, J. Tian, B. Hu, W. Swartz, B. Carrion Schaefer, C. Sechen, Y. Makris, "Design Obfuscation through Selective Post-Fabrication Transistor-Level Programming," *Proc. of Design Automation and Test in Europe (DATE) Conference*, March 25-29, 2019, Florence, Italy.

15. A. Yella, S. Gunturi and C. Sechen, "Are Standalone Gate Size and VT Optimization Tools Useful?", *Proc. IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE), Devices, Circuits, and Systems Track*, Windsor, ON, Canada, April 30 - May 3, 2017.
16. T. Broadfoot, C. Sechen and J. Rajendran, "On Designing Optimal Camouflaged Layouts", *Proc. IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, May 1-4, 2017, McLean, VA.
17. A. Yella and C. Sechen, "Improved Lagrangian Relaxation-based Gate Size and VT Assignment for Very Large Circuits, *Proc. IEEE PhD Research In Microelectronics and Electronics Conference Latin America (PRIME),* Bariloche, Argentina, February 20-23, 2017. **BEST PAPER AWARD**
18. J. Tian, G. Reddy, J. Wang, W. Swartz, Y. Makris and C Sechen, "A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic Reconfiguration", *Proc. of Design Automation and Test in Europe (DATE) Conference*, March 27-31, 2017, Lausanne, Switzerland. **NOMINATED FOR BEST PAPER AWARD**
19. M. Roshan, C. Sechen, *et al*., "Dual-MEMS Resonator Temperature-to-Digital Converter with 39μK Resolution and a FoM of 0.11pJK^2", *Proc. Int. Solid-State Circuits Conf. (ISSCC),* Feb. 2016, San Francisco, CA.
20. M. Jain and C. Sechen, "Chip Design: Matrix Multiplier Based on Systolic Architecture", *IEEE Computer Society 6th International Conference on Computing, Communications and Networking Technologies (ICCCNT)*, July 13-15, 2015, Dallas, TX.
21. Z. Wang, X. He and C. Sechen, "TonyChopper: A Desynchronization Package", *Proc. Int. Conf. on Computer Aided Design (ICCAD),* Nov. 2-6, 2014, San Jose, CA. (20% accepted)
22. H. Huang and C. Sechen, "A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS", *2014 Dallas Circuits and Systems Conference (DCAS)*, Oct 12-13, 2014, Dallas, TX.
23. A. Sridharan and C. Sechen, "Minimum Energy Operation using Robust Asynchronous Logic with Sleep Transistors", *Proc. Dallas Circuits and Systems Conference (DCAS)*, Oct 12-13, 2014, Dallas, TX.
24. Yashaswini Prathivadi, Carl Sechen, and Roozbeh Jafari, "A Swarm of Wearable Sensors at the Edge of the Cloud for Robust Activity Recognition", *Proc. First International Workshop on the Swarm at the Edge of the Cloud (SEC'13)*, Sept. 29, 2013, Montreal, Canada.
25. Mohammad-Mahdi Bidmeshki, Carl Sechen, and Roozbeh Jafari, "Low Power Programmable Architecture for Periodic Activity Monitoring", *Proc. SRC Techcon*, 2013, Austin, TX.
26. Thomas Broadfoot, Jingxiang Tian, HeeEun Choi, Mohammad-Mahdi Bidmeshki, Roozbeh Jafari, and Carl Sechen, "Platform Design for Swarm Wearable Computing", *Proc. First International Workshop on the Swarm at the Edge of the Cloud (SEC'13),* Sept. 29, 2013, Montreal, Canada.
27. A. Sridharan, C. Sechen, and R. Jafari, "Low-Voltage Low-Overhead Asynchronous Logic", *Int. Symp. on Low Power Electronics and Design (ISLPED)*, Beijing, China, Sept. 4-6, 2013. (25% accepted)
28. M. M. Bidmeshki, C. Sechen and R. Jafari, "Low Power Programmable Architecture for Periodic Activity Monitoring," *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, 8 March 2013, Round Top, Texas.
29. Hee-Eun Choi, C. Sechen and R. Jafari, "24kb, 11T Subthreshold SRAM for Ultra-Low Power Medical and Health Monitoring Embedded Systems," *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, 8 March 2013, Round Top, Texas.
30. M. Rahman, and C. Sechen, "Post-Synthesis Leakage Power Minimization", *Design Automation and Test in Europe (DATE) Conference*, March 12-16, 2012, Dresden, Germany.

31. M. Rahman, H. Tennakoon, R. Afonso and C. Sechen, "Power Reduction via Separate Synthesis and Physical Libraries", *Proc. Design Automation Conference (DAC)*, June 2011, San Diego, CA.
32. C. Pan and C. Sechen, "Power Efficient Partial Product Compression", *Proc. Great Lakes Symposium on VLSI*, Lausanne, May 2-4, 2011, Switzerland.
33. M. Rahman, H. Tennakoon, and C. Sechen, "Power Reduction via Near-Optimal Library-Based Cell-Size Selection", *Design Automation and Test in Europe (DATE) Conference*, March 14-18, 2011, Grenoble, France.
34. M. Rahman, H. Tennakoon, R. Afonso, and C. Sechen, October 17-18, "Design Automation Tools and Libraries for Low Power Digital Design", *Proc. IEEE Dallas Circuits and Systems Conference (DCAS)*, Oct. 17-18, 2010, Richardson, TX.
35. M. Rahman, H. Tennakoon, and C. Sechen, "Near Optimal Power Efficiency Through Gate Sizing", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC),* Oct. 26-27, 2009, Austin, TX.
36. H. Huang and C. Sechen, "A 22mW 227Msps 11b Self-Tuning ADC Based on Time-to-Digital Conversion", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC),* Oct. 26-27, 2009, Austin, TX.
37. E. Kiefer, W. Swartz, and C. Sechen, "Low Skew Automated Clock Tree Generation", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC),* Oct. 26-27, 2009, Austin, TX.
38. R. Afonso, M. Rahman, H. Tennakoon, and C. Sechen, "Power Efficient Standard Cell Library Design", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.
39. C.W. Pan, Y. Song, Z. Wang, and C. Sechen, "DSP Power Reduction through Generalized Carry-Save Arithmetic", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.
40. R. Afonso, M. Rahman, H. Tennakoon, and C. Sechen, "Power Efficient Standard Cell Library Design", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC),* Oct. 26-27, 2009, Austin, TX.
41. C.W. Pan, Y. Song, Z. Wang, and C. Sechen, "DSP Power Reduction through Generalized Carry-Save Arithmetic", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC),* Oct. 26-27, 2009, Austin, TX.
42. E. Kiefer, W. Swartz, and C. Sechen, "Low Power Automated Clock Tree Generation", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.
43. H. Huang and C. Sechen, "A 22mW 227Msps 11b Self-Tuning ADC Based on Time-to-Digital Conversion", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.
44. S. Sun and C. Sechen, "Post-Layout Comparison of High Performance 64b Static Adders in Energy-Delay Space," *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, Lake Tahoe, CA, October 2007.
45. M. Rahman, H. Tennakoon, and C. Sechen, "Optimal Area-versus-Delay Circuit Sizing Using Extended Logical Effort", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC),* May 14-15, 2007, Austin, TX.
46. K. H. Chong, L. McMurchie and C. Sechen, "A 64b Adder Using Self-calibrating Differential Output Prediction Logic," *Proc. Int. Solid-State Circuits Conference (ISSCC)*, February 2006, San Francisco, CA.
47. J. Zhang, M. Vujkovic, D. Wadkins, and C. Sechen, "Post-Layout Energy-Delay Analysis of Parallel Multipliers," *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, May 2006, Greece.
48. M. Vujkovic, D. Wadkins and C. Sechen, "Efficient Post-Layout Power-Delay Curve Generation," *Prof. 15th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 21-23 September 2005, Leuven, Belgium. In: *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and*

Simulation, Series: Lecture Notes in Computer Science, Vol. 3728 Paliouras, Vassilis; Vounckx, Johan; Verkest, Diederik (Eds.) 2005, XV, 753 p., Softcover ISBN: 3-540-29013-3.

49. X. Guo and C. Sechen, "High Throughput Divider Using Output Prediction Logic," *Proc. PRIME (Ph.D. Research in Microelectronics) Conf., July 25-28, 2005, Lausanne, Switzerland.*
50. X. Guo and C. Sechen, "A High Throughput Divider Implementation," *Proc. Custom Integrated Circuits Conference (CICC)*, 18-21 September 2005, San Jose, CA.
51. H. Tennakoon and C. Sechen, "Efficient and Accurate Gate Sizing with Piecewise Convex Delay Models," *Proc. Design Automation Conference (DAC)*, Anaheim, CA, June 13-17, 2005.
52. S. Sun, Y. Han, X. Guo, K. Chong, L. McMurchie and C. Sechen, "409ps 4.7 FO4 64b Adder Based on Output Prediction Logic in 0.18um CMOS," *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 11-12, 2005, Tampa, FL.
53. X. Guo and C. Sechen, "High Speed Redundant Adder and Divider in Output Prediction Logic," *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 11-12, 2005, Tampa, FL.
54. J. Kim, L. McMurchie and C. Sechen, "Mitigation of Single- and Multiple-Cycle-Duration SETs using Double-Mode Redundancy (DMR) in Time", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 5-12, 2005.
55. J. Lan, D. Lam, L. McMurchie, and C. Sechen, "SEE-Hardened-by-Design Area-Efficient SRAMs", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 5-12, 2005.
56. Y. Han, L. McMurchie and C. Sechen, "A High Performance CMOS Programmable Logic Core," *Proc. Custom Integrated Circuits Conference (CICC)*, October 3-6, 2004, Orlando, FL.
57. V. Tang, J. Lan, D. Lam, L. McMurchie, and C. Sechen, "High-Performance SEE-Hardened Programmable DSP Array," Proc. 2004 Military and Aerospace Programmable Logic Device (MAPLD) Conference, Washington, DC, Sept. 8-10, 2004.
58. D. Lam, J. Lan, L. McMurchie, and C. Sechen, "Radiation-Hardened-by-Design Area-Efficient SRAMs," Proc. Hardness by Design (HBD) Workshop, Albuquerque, NM, August 24-25, 2004.
59. M. Vujkovic, D. Wadkins, B. Swartz and C. Sechen, "Efficient Timing Closure Without Timing Driven Placement and Routing," *Proc. Design Automation Conference (DAC),* San Diego, CA, June 7-11, 2004.
60. Y. Lam, L. McMurchie, and C. Sechen, "SEU Hardening of Peripheral Circuitry in Self-Scrubbing SRAMs," *Proc. Single Event Effects Symposium*, Manhattan Beach, CA, April 27-29, 2004.
61. V. Tang, J. Lan, D. Lam, L. McMurchie and C. Sechen, "Low-Overhead SEE-Hardened Programmable DSP Array," *Proc. Single Event Effects Symposium*, Manhattan Beach, CA, April 27-29, 2004.
62. L. McMurchie and C. Sechen, "RADAR -- Reconfigurable Analog and Digital Array for Radiation-Hardened Circuits", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 6-13, 2004.
63. Y. Han and C. Sechen, "A Novel High Speed FPGA Architecture, *Proc. SRC Techcon*, Dallas, TX, Aug. 25 – 28, 2003.
64. C. Sechen, "The End of Libraries as We Know Them," *Proc. 40th Design Automation Conference (DAC)*, pp. 642-643, 2003.
65. S. Kio, K. Chong, and C. Sechen, "A Low Power Delayed-Clock Generation and Distribution System," *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, May 25-28, 2003, Bangkok, Thailand.

66. Warren Snapp, Paul Haug, Dave Sunderland, Roger Brees Don Bouldin, Wayne Dai, and Carl Sechen, "MSP Liberator ASIC Design Flow Produces Full Custom Performance Required for Next Generation Military Electronics*," Proc. Government Microelectronics and Applications Conference (GOMAC)*, April 1-3, 2003, Tampa, FL.
67. H. Tennakoon and C. Sechen, "Gate Sizing Using Lagrangian Relaxation Combined with a Fast Gradient-Based Preprocessing Step," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.
68. M. Vujkovic and C. Sechen, "Optimized Power-Delay Curve Generation for Standard Cell ICs," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.
69. L. McMurchie and C. Sechen, "WTA – Waveform-Based Timing Analysis for Deep Submicron Circuits," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.
70. M. Vujkovic and C. Sechen, "Optimized Power-Delay Curve Generation for Standard Cell ICs," *Proc. Int. Workshop on Logic Synthesis (IWLS)*, June 4-7, 2002, New Orleans, LA.
71. Yi Han, Larry McMurchie, Jovanka Ciric, and Carl Sechen, "Giga hertz-Speed FPGA Architecture based on Output Prediction Logic", *Tenth ACM/SIGDA International Symposium on Field Programmable Gate Arrays* (FPGA 2002).
72. J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *Proc. of IEEE Int. Conf. on Comp. Aided Design (ICCAD)*, San Jose, CA, November 5-7, 2001.
73. R. Rutenbar, M. Baron, T. Daniel, R. Jayaraman, Z. Or-Bach, J. Rose and C. Sechen, "When Will FPGAs Kill ASICs?" *Proc. Design Automation Conference (DAC)*, June 18-22, 2001, Las Vegas, NV.
74. J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *Proc. of IEEE Int. Workshop on Logic Synthesis*, Lake Tahoe, CA, June 12-15, 2001.
75. S. Kio, L. McMurchie, and C. Sechen, "Application of Output Prediction Logic to Differential CMOS," *Proc. of IEEE Computer Society Annual Workshop on VLSI*, Orlando, FL, April 19-20, 2001.
76. S. Sun, L. McMurchie, and C. Sechen, "A High-Performance 64-bit Adder Implemented in Output Prediction Logic," *Proc. 19th Conference on Advanced Research in VLSI*, March 14-16, 2001, Salt Lake City, UT.
77. T. Serdar and C. Sechen, "Automatic Datapath Tile Placement and Routing," *Proc. of the Design, Automation and Test in Europe (DATE) Conference*, March 13-16, 2001, Munich, Germany.
78. S. Kio, L. McMurchie, and C. Sechen, "Output Prediction Logic", *Proc. SRC Techcon*, September 21-23, 2000, Phoenix, AZ.
79. M. Vujkovic, G. Yee, and C. Sechen, "Post-Fabrication Automatically Tunable Programmable Delay Elements for Clock-Delayed Domino Logic," *Proc. SRC Techcon*, September 21-23, 2000, Phoenix, AZ.
80. G. Hoyer and C. Sechen, "A Locally-Clocked Dynamic Logic Serial/Parallel Multiplier," *Proc. SRC Techcon*, September 21-23, 2000, Phoenix, AZ.
81. L. McMurchie, S. Kio, G. Yee, T. Thorp and C. Sechen, "Output Prediction Logic: A High Performance CMOS Design Technique", *Proc. Int. Conf. On Computer Design (ICCD)*, September 17-20, 2000, Austin, TX.
82. G. Hoyer and C. Sechen, "A Locally-Clocked Dynamic Logic Serial/Parallel Multiplier", *Proc. of Custom Integrated Circuits Conference (CICC)*, May 21-25, 2000, Orlando, FL.
83. Gin Yee, Ron Christopherson, Tyler Thorp, Ban P. Wong, and Carl Sechen, "An automated shielding algorithm and tool for dynamic circuits," *Proc. Intl. Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 20-22, 2000.

84. J. Ciric, G. Yee, C. Sechen, "Delay Minimization and Technology Mapping of Two-Level Structures and Implementation Using Clock-Delayed Domino Logic," *Proc. Design Automation & Test in Europe (DATE2000)*, 27-30 March 2000, Paris, France.
85. T. Serdar and C. Sechen, "AKORD: Transistor Level and Mixed Transistor/Gate Level Placement Tool for Digital Data Paths," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, San Jose, CA, November 1999.
86. T. Thorp, G. Yee and C. Sechen, "Monotonic Static CMOS and Dual Vt Technology," *Proc. Int. Symp. on Low Power Electronics and Design (ISPLED)*, San Diego, CA, August 16-17, 1999.
87. T. Thorp, G. Yee and C. Sechen, "Monotonic Logic and Dual Vt Technology", *Proc. of Int. Conf. on Computer Design (ICCD)*, Austin, TX, October 1999.
88. G. Hoyer, G. Yee and C. Sechen, "SEU Tolerant Locally-Clocked Dynamic Logic, *Proc. Government Microelectronics and Applications Conference (GOMAC)*, March 1999, Monterey, CA.
89. T. Thorp and C. Sechen, "Domino logic synthesis using complex static gates", *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 9-11, 1998, San Jose, CA.
90. H. Tennakoon and C. Sechen, "Linear Time Heuristic for Timing Optimization", *Proc. SRC TECHCON Conf.*, Sept. 9-11, 1998, Las Vegas, NV.
91. G. Hoyer, G. Yee and C. Sechen, "Locally-clocked Dynamic Logic", *Proc. Midwest Conf. On Circuits and Systems*, Aug. 10-12, 1998, Notre Dame, IN.
92. J. Ciric and C. Sechen, "Clock-delayed Domino Synthesis Using Decomposition into Two-level Structures", *Proc. SRC TECHCON Conf.*, Sept. 9-11, 1998, Las Vegas, NV.
93. G. Hoyer and C. Sechen, "Locally-clocked Dynamic Logic", *Proc. SRC TECHCON Conf.*, Sept. 9-11, 1998, Las Vegas, NV.
94. H. P. Tseng, L. Liu and C. Sechen, "Chip-level Area Routing", *Proc. International Symposium on Physical Design (ISPD)*, April 1998, Monterey, CA.
95. H. P. Tseng, L. Scheffer and C. Sechen, "Timing and Crosstalk Driven Area Routing," *Proc. IEEE Design Automation Conference (DAC)*, June 1998, San Francisco, CA.
96. T. Thorp, G. Yee and C. Sechen, "Dynamic Logic Synthesis using Alternating Dynamic and Static Gates," *Proc. Int. Workshop on Logic Synthesis*, June 1998, Lake Tahoe, CA.
97. G. Yee, R. Chandra, H. Ganesan, and C. Sechen, "Wire Delay in the Presence of Crosstalk," *ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems,* Dec. 4-5, 1997, Austin, Texas.
98. M. Lefebvre, D. Marple and C. Sechen, "The Future of Custom Cell Generation in Physical Synthesis," *Proc. Design Automation Conference (DAC)*, Anaheim, CA, June 1997, pp. 446-451.
99. G. Yee and C. Sechen, "Dynamic Logic Synthesis," *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, May 5-8, 1997, Santa Clara, CA, pp. 345-348.
100. H. P. Tseng and C. Sechen, "Multi-layer Over-the-Cell Routing with Obstacles," *Proc. IEEE Custom Integrated Circuits Conference*, May 5-8, 1997, Santa Clara, CA, pp. 565-568.
101. L. Liu and C. Sechen, "Multi-layer Chip-Level Global Routing Using an Efficient Graph-based Steiner Tree Heuristic," *Proc. European Design and Test Conference (EDTC)*, March 18-20, 1997, Paris, France.
102. H. P. Tseng and C. Sechen, "A Gridless Multi-layer Router for Standard Cell Circuits Using Central Terminal Model Cells," *Proc. European Design and Test Conference (EDTC)*, March 18-20, 1997, Paris, France.
103. B. Guan and C. Sechen, "Large Standard Cell Libraries and Their Impact on Layout Area and Circuit Performance," *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, October 7-9, 1996, Austin, TX.
104. G. Yee and C. Sechen, "Clock-delayed Domino for Adder and Random Logic Design," *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, October 7-9, 1996, Austin, TX.

105. G. Yee and C. Sechen, "Low voltage and low power: how low can you go?," *Proceedings International Conference on Computer Design. VLSI in Computers and Processors*, 1996, pp. 342-, doi: 10.1109/ICCD.1996.563576.
106. B. Guan and C. Sechen, "ASIC Automatic Layout Generation Using Large Standard Cell Libraries," *Proc. International Conference on ASIC (ASICON)*, October 21-24, 1996, Shanghai, China.
107. B. Guan and C. Sechen, "Efficient Standard Cell Generation When Diffusion Strapping Is Required," *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, May 1996, San Diego, CA.
108. Q. Yu and C. Sechen, "Approximate Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the European Conference on Circuit Theory and Design (ECCTD)*, August 27-31, 1995, Istanbul, Turkey.
109. W. Swartz and C. Sechen, "Timing Driven Placement for Large Circuits," *Proc. 1995 Design Automation Conference (DAC)*, San Francisco, CA, June 1995.
110. T. Stanion and C. Sechen, "A Method for Finding Good Ashenhurst Decompositions and Its Application for FPGA Synthesis," *Proc. 1995 Design Automation Conference (DAC)*, San Francisco, CA, June 1995.
111. B. Guan and C. Sechen, "An Area Minimizing Layout Generator for Random Logic Blocks," *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, May 1-4, 1995, Santa Clara, CA.
112. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *Proc. of the IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 1-3, 1995, Seattle, WA.
113. J. Hsu and C. Sechen, "Simplified Symbolic Pole and Zero Expressions from the Sifting Approach to Symbolic Analysis," *Proc. of the IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 1-3, 1995, Seattle, WA.
114. T. Stanion and C. Sechen, "Quasi-Algebraic Decomposition of Switching Functions," *Proc. 16th Conference on Advanced Research in VLSI*, March 27-29, 1995, Chapel Hill, NC, pp. 358-367.
115. K. Roy and C. Sechen, "Multiple FPGA Partitioning with Performance Optimization," *Proc. of the IEEE/ACM International Symposium on FPGAs*, March 12-14, Monterrey, CA, 1995, pp. 146-152.
116. W. Sun and C. Sechen, "A Loosely Coupled Parallel Algorithm for Standard Cell Placement," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 6-10, 1994, Santa Clara, CA, pp. 137-144.
117. Q. Yu and C. Sechen, "Approximate Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 6-10, 1994, Santa Clara, CA, pp. 664-671.
118. J. J. Hsu and C. Sechen, "Fully Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Custom Integrated Circuits Conference (CICC)*, May 2-4, 1994, San Diego, CA, pp. 457-460.
119. Q. Yu and C. Sechen, "Generation of Color-Constrained Spanning Trees with Application in Symbolic Analysis," *Fourth Great Lakes Symposium on VLSI*, March 4-5, 1994, Notre Dame, IN, pp. 252-255.
120. K. Roy and C. Sechen, "A Timing Driven N-Way Chip and Multi-Chip Partitioner," *Proc. SRC TECHCON Conference*, September 28-30, 1993, Atlanta, GA.
121. W. Swartz and C. Sechen, "Precise Timing Driven Placement for Large Circuits," *Proc. SRC TECHCON Conference*, September 28-30, 1993, Atlanta, GA.
122. W. Swartz and C. Sechen, "A New Generalized Row-Based Global Router," *Proc. of the SRC TECHCON Conference*, September 28-30, 1993, Atlanta, GA.

123. T. Stanion and C. Sechen, “Maximum Projections of Don't Care Conditions in a Boolean Network,” *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA, pp. 674-679.
124. W. Sun and C. Sechen, “Efficient and Effective Placement for Very Large Circuits,” *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA, pp. 170-177.
125. K. Roy and C. Sechen, “A Timing Driven N-Way Chip and Multi-Chip Partitioner,” *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA, 240- 247.
126. W. Swartz and C. Sechen, “A New Generalized Row-Based Global Router,” *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA, pp. 491- 498.
127. K. Roy, B. Guan and C. Sechen, “A Sea-of-Gates Style FPGA Placement Algorithm,” *Int. Conf. on VLSI Design*, January 5-8, 1994, Calcutta, India.
128. J. J. Hsu and C. Sechen, “Low-Frequency Symbolic Analysis of Large Analog Integrated Circuits,” *IEEE Custom Integrated Circuits Conference (CICC)*, May 9-12, 1993, San Diego, CA, pp. 14.7.1-14.7.5.
129. T. Stanion and C. Sechen, “Boolean Division and Factorization Using Binary Decision Diagrams,” *IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS '92)*, Dec. 8-11, 1992, Sydney, Australia.
130. K. W. Lee and C. Sechen, “A Global Router for Sea-of-Gates Circuits,” *Proc. European Design Automation Conference*, Amsterdam, The Netherlands, February 26-28, 1991, pp. 242-247.
131. D. Chen and C. Sechen, “Mickey: A Macro Cell Global Router”, *Proc. European Design Automation Conference*, Amsterdam, The Netherlands, February 26-28, 1991, pp. 248- 252.
132. W. Swartz and C. Sechen, “New Algorithms for the Placement and Routing of Macro Cells,” *Proc. Int. Conf. on Comp. Aided Design (ICCAD)*, Santa Clara, CA, November 11-15, 1990, pp. 336-339.
133. D. Chen and C. Sechen, “Mickey: A New Macro Cell Global Router,” *Proc. SRC Techcon Conference*, San Jose, CA, October 16-18, 1990, pp. 241-244.
134. W. Swartz and C. Sechen, “New Algorithms for the Placement and Routing of Macro Cells,” *Proc. SRC Techcon Conference*, San Jose, CA, October 16-18, 1990, pp. 233-236.
135. K. W. Lee and C. Sechen, “A New Global Router for Sea-of-Gates Circuits,” *Proc. 9th Australian Microelectronics Conference*, Adelaide, S. Australia, July 2-4, 1990, pp. 233-244.
136. K. W. Lee and C. Sechen, “A New Global Router for Row-Based Layout,” *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 7-10, 1988, Santa Clara, CA, pp. 180-183.
137. C. Sechen and D. Chen, “An Improved Objective Function for Mincut Circuit Partitioning,” *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 7-10, 1988, Santa Clara, CA, pp. 502-505.
138. C. Sechen, “Chip-Planning, Placement, and Global Routing of Macro/Custom Cell Circuits Using Simulated Annealing,” *Proc. of the 25th Design Automation Conference (DAC)*, June 1988, Anaheim, CA, pp. 73-80.
139. C. Sechen and K. W. Lee, “An Improved Simulated Annealing Algorithm for Row-Based Placement,” *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 9-13, 1987, Santa Clara, CA, pp. 478-481.
140. C. Sechen, “Average Interconnection Length Estimation for Random and Optimized Placements,” *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 9-13, 1987, Santa Clara, CA, pp. 190-193.
141. J. Burns, A. Casotto, M. Igusa, F. Marron, F. Romeo, A. Sangiovanni-Vincentelli, C. Sechen, H. Shin, G. Srinath, and H. Yaghutiel, “Mosaico: An Integrated Macro-Cell Layout System,” in C. Sequin, editor, *Proc. of VLSI '87*, Vancouver, Canada, August, 1987.

142. C. Sechen and A. Sangiovanni-Vincentelli, "TimberWolf3.2: A New Standard Cell Placement and Global Routing Package," *Proc. 23rd Design Automation Conference (DAC)*, June 29-July 2, 1986, Las Vegas, NV, pp. 432-439.
143. D Braun, C. Sechen, and A. Sangiovanni-Vincentelli, "ThunderBird: A Complete Standard Cell Layout Package," *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1986, Rochester, NY.
144. F. Romeo, C. Sechen, and A. Sangiovanni-Vincentelli, "Simulated Annealing Research at Berkeley," *Proc. Int. Conf. on Computer Design (ICCD)*, October 1984, Rye Brook, NY.
145. C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1984, Rochester, NY.
146. M. Huberman, S. Senturia, and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Device Research Conference (DRC)*, Cornell University, June 1977.
147. S. Senturia and C. Sechen, "The Charge-Flow Transistor," *IEEE Int. Electron Devices Meeting (IEDM)*, Washington DC, Dec. 1976.
148. L. Liu and C. Sechen, "A Multi-Layer Chip-Level Global Router," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
149. L. Liu and C. Sechen, "Multi-Layer Pin Assignment for Macro Cell Circuits," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
150. G. Yee and C. Sechen, "Clock-Delayed Domino for Adder and Combinatorial Logic Design," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
151. B. Guan and C. Sechen, "Efficient Standard Cell Generation When Diffusion Strapping is Required," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
152. H. P. Tseng and C. Sechen, "A Gridless Multi-Layer Channel Router Based on a Combined Constraint Graph and Tile Expansion Approach," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
153. J. J. Hsu and C. Sechen, "The Sifting Approach to Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 211-230.
154. Q. Yu and C. Sechen, "Approximate Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 241-259.
155. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 261-277.
156. T. Stanion and C. Sechen, "Maximum Projections of Don't Care Conditions in a Boolean Network," *Proc. of the International Workshop on Logic Synthesis*, Lake Tahoe, CA, May 23-26, 1993.
157. W. Sun, K. Roy, and C. Sechen, "Fast, High-Quality Placement for Large Circuits," *Proc. of the 4th ACM/SIGDA Physical Design Workshop*, Lake Arrowhead, CA, April 19-21, 1993.
158. K. Roy, D. Guan and C. Sechen, "FPGA MCM Partitioning and Placement," *Proc. of the 4th ACM/SIGDA Physical Design Workshop*, Lake Arrowhead, CA, April 19-21, 1993.
159. T. Stanion and C. Sechen, "Incremental and Simultaneous Computation of Satisfiability and Observability Don't Cares," *Proc. IEEE/ACM Winter VLSI Workshop*, Jan. 25-27, 1993, Asilomar, CA.
160. R. Weier and C. Sechen, "TimberWolfAR: An Arbitrary Design Rule Multi-Layer Area Router," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.

161. W. Swartz and C. Sechen, "A Generalized Row-Based Global Router for FPGAs," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.
162. K. Roy and C. Sechen, "A Timing Driven N-Way Chip Partitioner," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.
163. K. W. Lee and C. Sechen, "A Global Router for Sea-of-Gates Circuits," *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.
164. D. Chen and C. Sechen, "Mickey: A New Macro Cell Global Router", *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.
165. W. Swartz and C. Sechen, "New Algorithms for the Placement and Routing of Macro Cells," *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.
166. C. Sechen, "TimberWolfSG: A Sea-of-Gates Layout Package," *Proc. of SRC Workshop on Sea-of-Gates Design*, Sept. 22-23, 1988, Berkeley, CA.
167. C. Sechen, "A Global Router for the Sea-of-Gates Environment," *Proc. IFIP Workshop on Physical Design of Sea-of-Gates VLSI*, August 11-12, 1988, Lenggries, Germany.
168. J. Lam, J. M. Delosme, and C. Sechen, "A New Simulated Annealing Schedule for Row-Based Placement," *Proc. IEEE International Workshop on Placement and Routing*, May 10-13, 1988, Research Triangle Park, NC.
169. F. Romeo, C. Sechen, and A. Sangiovanni-Vincentelli, "Some Theoretical Results on Simulated Annealing and TimberWolf: A Placement and Routing Package for the Layout of Integrated Circuits," *Proc. Workshop on Statistical Physics in Engineering and Biology*, IBM T.J. Watson Research Center, Yorktown Heights, NY, April 1984.

Books Authored

Carl Sechen, **Placement and Global Routing of Integrated Circuits Using Simulated Annealing**, 278 pages, Kluwer Academic Publishers, Boston, MA, 1988.

Patents

C. Sechen, Y. Makris, T. Broadfoot, "Field Programmable Transistor Arrays", US Patent 11,362,662 issued June 14, 2022. (New patent relative to the below two.)

C. Sechen, Y. Makris, G. Reddy, J. Tian, "Field Programmable Transistor Arrays", US Patent 10,855,285 B2, issued 1 December 2020. (New patent relative to the 2019 one.)

C. Sechen, Y. Makris, G. Reddy, J. Tian, "Field Programmable Transistor Arrays", US Patent No. 10,511,308, issued December 17, 2019.

C. Sechen, L. McMurchie, G. Yee and T. Thorp, "Output Prediction Logic", US Patent No. 6,549,038 issued March 2003.

Research Funding

- NSF Proposal: SaTC: TTP: Medium: Hardware Intellectual Property Protection through Hybrid ASIC/TRAP Integrated Circuit Design, awarded, 8/15/22-7/31/26, $900,000 (PI: Y. Makris, co-PI: C. Sechen).

- "CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)", Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer, ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, $150,000. NSF CHEST I/UCRC. March 1, 2022 – February 28, 2023.

- "CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)", Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer, Dr. William Swartz Jr., ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, $150,000. NSF CHEST I/UCRC. March 1, 2021 – February 28, 2022.

- IBM / NSWC CW3085860, "Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities (RAMP)," 10/8/20-3/20/21, $143,576 (PI: Y. Makris, co-PI: C. Sechen)

- "DEFENSEWERX-Advanced Microelectronics Design & Prototype Challenge", Benjamin Carrion Schaefer, Yiorgos Makris, Carl Sechen, William Swartz Jr., InertialWave/Defensewerks/Air Force, August 1, 2020 – November 30, 2020, $200,000.

- "CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)", Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer, Dr. William Swartz Jr., ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, $100,000. NSF CHEST I/UCRC. March 1, 2020 – February 28, 2021.

- "TRAP-based Circuit Obfuscation Development and Evaluation", PIs: Y. Makris, B. Schaefer, W. Swartz and C. Sechen, The Boeing Company, $149,914, February 1, 2020 – August 31, 2020.

- "DEFENSEWERX-Advanced Microelectronics Design & Prototype Challenge", Benjamin Carrion Schaefer, Yiorgos Makris, Carl Sechen, William Swartz Jr., InertialWave/Defensewerks/Air Force, Nov. 15, 2019 – Mar. 15, 2020, $87,980.

- "OpenROAD: Foundations and Realizations of Open, Accessible Design", co-PIs Carl Sechen and William Swartz, Defense Advanced Research Products Agency (DARPA) IDEA Program, May 1, 2018 through April 30, 2019, $287,341.

- CSR: "Small: Host-Assisted Software-Defined Solid-State Disk", PI: Carl Sechen, October 1, 2014 – September 30, 2019, $265,067.

- TerraSwarms Research Center, DARPA/SRC FCRP research center based at UC Berkeley, Jan. 15, 2013 – Jan. 14, 2014, co-PI: Carl Sechen portion: $100,000.

- "Optimal Gate Size and Vt Selector, and Innovative Approach to Path-Based Timing Analysis", PI: Carl Sechen, Texas Instruments, Jan. – Dec., 2012, $50,000. Current status: completed.

- "Optimal Gate Size and Vt Selection", Texas Instruments, Wireless Division, Jan. – Dec., 2011, $50,000, PI: Carl Sechen.

- "Power Minimization Research", Texas Instruments, ASIC Division, Jan. – Dec., 2011, $50,000, PI: Carl Sechen.

- "Power Minimization Research", Texas Instruments, ASIC Division, Jan. – Dec., 2010, $75,000, PI: Carl Sechen.

- "Low Power HD Video Decoder Research", Texas Instruments, Wireless Division, Jan. – Dec., 2010, $50,000, PI: Carl Sechen.

- "Power Minimization Research", Texas Instruments, ASIC Division, Jan. – Dec., 2009, $50,000, PI: Carl Sechen.

- "Low Power HD Video Decoder Research", Texas Instruments, Wireless Division, Jan. – Dec., 2009, $50,000, PI: Carl Sechen.

- "Power Optimization and Circuit Hardening", MARCO Focus Center Research Program (C2S2), $155,000, September 2005 – August 2008.

- "Ultra High Performance Digital Circuit Design and Synthesis", National Science Foundation (NSF), $80,000, (Jan. 2006 – Dec., 2008).

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $80,000, Jan. – Dec., 2008.

- "Power Minimization Research", Carl Sechen, Texas Instruments, ASIC Division, $37,000, Jan. – Dec., 2008.

- "Power Minimization and Yield Optimization in Digital IC's", Carl Sechen, Semiconductor Research Corporation TxACE, $150,000, August 2007 – July 2010.

- "Analog-to-Digital Converter based on Time-to-Digital Conversion", Carl Sechen, Texas Instruments, $40,000, Sep. 2007 – Aug. 2008.

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $45,000, Jan. – Dec., 2007.

- "Three-Transistor Memory Cell Research", Carl Sechen, Texas Instruments, $35,000, Jan. – Dec., 2007.

- "Power Minimization Research", Carl Sechen, Texas Instruments, ASIC Division, $37,000, Jan. – Dec., 2007.

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $30,000, Sept. – Dec., 2006.

- “DRAM-Density SRAM”, Carl Sechen, Honeywell, $105,000, January 2006 – April 2007.

- “RADHARD by Design,” DARPA/Boeing, Phase I, $45,000 (co-PI, my portion), November 2004 – August 2005).

- “CLASS: Clockless Logic, Analysis, Synthesis, and Systems,” DARPA/Boeing, Phase II/III, $709,000 (co-PI, my portion), (Sept. 2004 – August 2006).

- “MSP Phase 2: Digital IC Optimization Techniques,” DARPA/Boeing, $285,000 (co-PI, my portion), (September 2004 – August 2006).

- “Power Optimization and Circuit Hardening,” MARCO FCRP C2S2 Center, $100,000, PI (Oct. 04 – Sep. 05).

- “High Speed and Low Power Digital IC Design,” NSF ITR, $350,000 (my portion) co-PI, (Sept. 00 – Aug. 05).

- “Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits,” Air Force Research Lab, $110,000, PI (Sep 04 – Aug 05).

- “High Speed & Low Power Digital Circuit Synthesis and Design,” MARCO FCRP C2S2 Center, $100,000, PI (Oct. 03 – Sep. 04), full indirect.

- “CLASS: Clockless Logic, Analysis, Synthesis, and Systems,” DARPA/Boeing, Phase I, $135,000 (co-PI, my portion), (Oct. 2003 – May 2004).

- “Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits,” Air Force Research Lab, $105,000, PI (Sep 03 – Aug 04), full indirect.

- “Low Power Digital IC Design,” NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000, PI (Sep 03 – Aug 04), no indirect.

- “Reconfigurable RF, Analog and Digital Array for Radiation-Hardened Wireless Communication Circuits,” DARPA/SPAWAR, $150,000, PI (April 03 – May 04), full indirect.

- “Development of Pulse-Based Logic,” DARPA, $100,000, PI (March 03 – May 04), full indirect.

- “High Performance and Power Efficient Digital IC Optimization Techniques,” MSP Phase 1: Boeing/DARPA, $400,000, PI (April 02 – August 03), full indirect.

- Unrestricted grant, Intel Corporation, $60,000, PI (May 03 – April 04).

- “High Performance Digital IC Design,” MARCO/DARPA C2S2 Center, $170,000, PI (Jan. 01 – Aug. 03), full indirect.

- “Ultra High Performance Digital Circuit Design and Synthesis,” National Science Foundation, $180,000, PI, (Sep 02 – Aug 05).

- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, $95,000, PI (Sep 02 – Aug 03), full indirect.

- "PLL Design, Clock Generation and High-Speed/Low-Power DSP-block Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000, PI (Sep 02 – Aug 03), no indirect.

- Unrestricted grant, Intel Corporation, $60,000, PI (Mar 02 – Feb 03), no indirect.

- "High Performance Digital IC Design," Semiconductor Research Corporation (SRC), June 1, 2000 – May 31, 2003, $525,000 (full indirect).

- "High Performance Digital IC Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $60,000 (no indirect), PI (Sep. 00 - Aug. 01).

- Unrestricted grant, Intel Corporation, $60,000, PI (Mar 01 – Feb 02).

- Unrestricted grant, Sun Microsystems, $30,000, PI (Feb 00 – Mar 01).

- Unrestricted grant, Compaq Computer Corp., $25,000, PI (Oct. 99 – Sep. 00).

- Unrestricted grant, Cadabra, Inc., $20,000, PI (Feb. 00 – Mar 01).

- "Ultra High Speed Digital Circuit Synthesis and Layout NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000 (no indirect), PI (Sep. 99-Aug. 00).

- "Ultra High Speed Digital Circuit Synthesis and Layout", National Science Foundation, $255,000 (full indirect), PI (Sep 99 – Aug 02).

- "Ultra High Speed Digital Circuit Synthesis and Layout", Semiconductor Research Corporation, $154,000 (full indirect), PI (Mar 99-Mar 00).

- "Ultra High Speed Digital Circuit Synthesis and Layout", , Semiconductor Research Corporation, $154,000 (full indirect), PI (Mar 99-Mar 00).

- "Synthesis of Ultra High Speed Random Logic Blocks", Semiconductor Research Corporation, $132,000, PI (Mar 98-Feb 99).

- "Ultra High Speed Digital Circuit Synthesis and Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $65,000, PI (Sep. 98-Aug. 99).

- "Radiation-hard High Speed Digital Circuit Synthesis", Boeing, $35,000, PI (Sep. 98-Aug. 99).

- "Datapath Cell Layout", Compaq/Digital Equipment, $25,000, PI (Sep. 98 – Aug. 99).

- Unrestricted grant, Sun Microsystems, $8,000, PI (June 99 – May 00).

- Unrestricted grant, Compaq Computer Corp., $25,000, PI (Oct. 98 – Sep. 99).

- Unrestricted grant, Sun Microsystems, $30,000, PI (Jan. 99 – Dec. 99).
- Unrestricted grant, TimberWolf Systems, Inc., $20,000, PI (Apr. 98 – Mar. 99).
- Unrestricted grant, Sun Microsystems, Inc., $8,000, PI (June 98 – May 99).
- Various industrial gifts, $65,000, PI (Sep 97-Aug 98).
- "High Speed Digital Circuit Design", NSF Center for the Design of Analog and Digital ICs (CDADIC), $50,000, PI (Sep. 97-Aug. 98).
- "Automatic Layout Research", Semiconductor Research Corporation, $132,000, PI (Mar 97-Feb 98).
- Various industrial gifts, $112,000, PI (Sep 96-Aug 97).
- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $50,000, PI (Sep. 96-Aug. 97).
- "Symbolic Analysis of Large Analog Circuits", National Science Foundation, $90,000, PI (Sep 94-Aug 97).
- "Automatic Layout Research", Semiconductor Research Corporation, $132,000, PI (Mar 96-Feb 97).
- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 95-Aug. 96).
- Various industrial gifts, $117,000, PI (Sep 95-Aug 96).
- "Automatic Layout Research", Semiconductor Research Corporation, $132,000, PI (Mar 95-Feb 96).
- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 94-Aug. 95).
- Various industrial gifts, $208,000, PI (Sep 94-Aug 95).
- "Automatic Layout Research", Semiconductor Research Corporation, $144,000, PI (Mar 94-Feb 95).
- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 93-Aug. 94).
- Various industrial gifts, $343,000, PI (Sep 93-Aug 94).
- "Automatic Layout Research", Semiconductor Research Corporation, $140,000, PI (Mar 93-Feb 94).

- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 92-Aug. 93).

- Various industrial gifts, $312,000, PI (Sep 92-Aug 93).

- “Automatic Layout Research”, Semiconductor Research Corporation, $140,000, PI (Mar 92-Feb 93).

- Various industrial gifts, $306,000, PI (Sep 91-Aug 92).

- Yale University, Various Industrial Gifts, $1.65 million, PI (1986-1992).

Conference Service Activities

- Session Chairman for the Design Automation and Test in Europe Conference, 2012-2014.
- Session Chairman for the IEEE Design Automation Conference, 1987, 1990, 1991, 1997.
- Session Chairman for the International Symposium on Physical Design, 1997, 1998.
- Session Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1988, 89, 90, 91, 92.
- Session Chairman for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989, 1990, 1991, 1992, 1993, 1998.
- Elected Chairman for the Placement and Floorplanning sub-committee for the 2004 Design Automation Conference (DAC), 2004.
- Elected to the Placement and Floorplanning sub-committee for the 2003 Design Automation Conference (DAC), 2003.
- Elected Program Chair for the 2000 ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU).
- Elected chairman of the placement and floorplanning committee of the 2001 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 2000 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and routing committee of the 1999 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 1998 Int. Conf. On Computer Aided Design (ICCAD).
- Elected Program Chairman of the ACM Physical Design Workshop, Lake Arrowhead, CA, April 1993.
- Elected Chairman of the 1992 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- Elected Chairman of the 1990 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- CAD Track Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1991.

Service as a Referee

- Technical Program Committee for the Design Automation Conference, 2014, 2015.
- Technical Program Committee for the Design Automation and Test in Europe Conference, 2012-2014.
- Technical Program Committee for the IEEE Int. Symposium on VLSI Design, 2010-2011.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989-93, 98.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Design (ICCD), 1987-97.
- Technical Program Committee for the European Design and Test Conference (EDTC), 1995, 96, 97, 98.
- Technical Program Committee for the Design Automation and Test in Europe (DATE) Conference, 1998, 99, 00, 01, 02, 03.
- Technical Program Committee for ACM International Physical Design Workshop, 1996.
- Technical Program committee for the International Symposium on Physical Design, 1997, 98.
- Technical Program Committee for the International Workshop on Layout Synthesis, 1988, 90, 92.
- IEEE/ACM Design Automation Conference, 1986-1998.
- National Science Foundation, 1986-present.

- IEEE Transactions on Computer Aided Design, 1986-present.
- IEEE Transactions on VLSI Systems, 1992-present.
- ACM Transactions on Design Automation of Electronic Systems, 1995-present.

University Service

UTD

Director of ECS Tech Support Services, June 2012 – February 2014
Information Technology Planning and Policy Committee, Sept. 1, 2016 – August 31, 2019

UW

Faculty Council on Research, 1994-1997
Faculty Senate, 2002-2004

Department Service

UTD

Chair of the Computer Resources Committee, ECE Dept., 2007-2021
Advisory Committee to TxACE (SRC Texas Analog Center of Excellence) 2008-2009
Chair of the Analog Search Sub-Committee, EE Dept., 2007-2008
Faculty Search Committee (computer engineering) 2010-11
Teaching Assistant (TA) Selection Committee, 2021-23

UW

Faculty Search Committee, 2005-2006
Group Chair, VLSI and Digital Systems Group, 1997-2005
Faculty Search Committee, 98-99.
Graduate Studies and Research Committee, 1992-93, 96-97, 97-98.
Group Chair, Electronics, 94-95.
Graduate Admissions Committee, Electrical Engineering Dept., 1992-93.
Qualifying Examination Subcommittee, 1992-93.
Computer Resources Committee, 1992-93.

Outside University Service

Selected by the NSF to serve as a panelist for (invited) full proposals submitted to the CISE Expeditions in Computing (Expeditions) program, NSF 08-568, April 6-7, 2010.

Selected by the NSF to serve on the 2008 proposal review panel (April 14-15, 2008) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2009 funding.

Selected by the NSF to serve on the 2007 proposal review panel (January 8-9, 2007) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2008 funding.

Selected by the NSF to serve on the 2005 proposal review panel (October 20-21, 2005) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2006 funding.

Selected by the NSF to serve on the 2004 proposal review panel (May 5-6, 2004) to review a number of proposals that have been submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2004 funding.

Selected by the NSF to serve on the 2002 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Selected by the NSF to serve on the 1999 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Co-Director of the NSF Center for the Design of Analog and Digital ICs (CDADIC), 1997-2005; this center provides about $450,000 annually to the University of Washington.

Professional Society Memberships

Eta Kappa Nu
Tau Beta Pi
Sigma Xi
IEEE Fellow
ACM