UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BiTMICRO, LLC,
Patent Owner.

Case IPR2023-00782
Patent 8,010,740

PATENT OWNER'S PRELIMINARY RESPONSE

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Pursuant to 37 C.F.R. § 42.107, Patent Owner BiTMICRO, LLC ("BiTMICRO" or "Patent Owner") files this preliminary response to the Petition, setting forth reasons why the Petition for *inter partes* review ("IPR") of claims 1, 9-15, 32, and 34 of U.S. Patent No. 8,010,740 (the "'740 Patent"), as requested by Intel Corporation ("Petitioner"), should be denied.[1]

I. INTRODUCTION

The '740 Patent is entitled "OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE" and relates to "solutions for optimizing memory operations in a memory system suitable for use in an electronic storage device." *See* '740 Pat., 1:16–18. As an example of such a solution, the '740 Patent describes and claims an improved "mapping table" that increases "the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources" by "interleaving or [performing] parallel memory operations, reducing memory operation latency, increasing operational device efficiency," or a combination thereof. '740 Pat., 2:14–21.

[1] By submitting this Preliminary Response, no waiver of any argument is intended by Patent Owner. Patent Owner will have a right to file a complete response to the Petition, should the Board institute *inter partes* review. 37 C.F.R. § 42.120(a).

A. The '740 Patent Discloses a Mapping Table Designed to Correlate Sets of Consecutive Logical Block Addresses and Physical Block Addresses

The '740 Patent illustrates an exemplary "mapping table for an electronic storage device" in FIG. 2, also reproduced below. '740 Pat., 2:58-61.

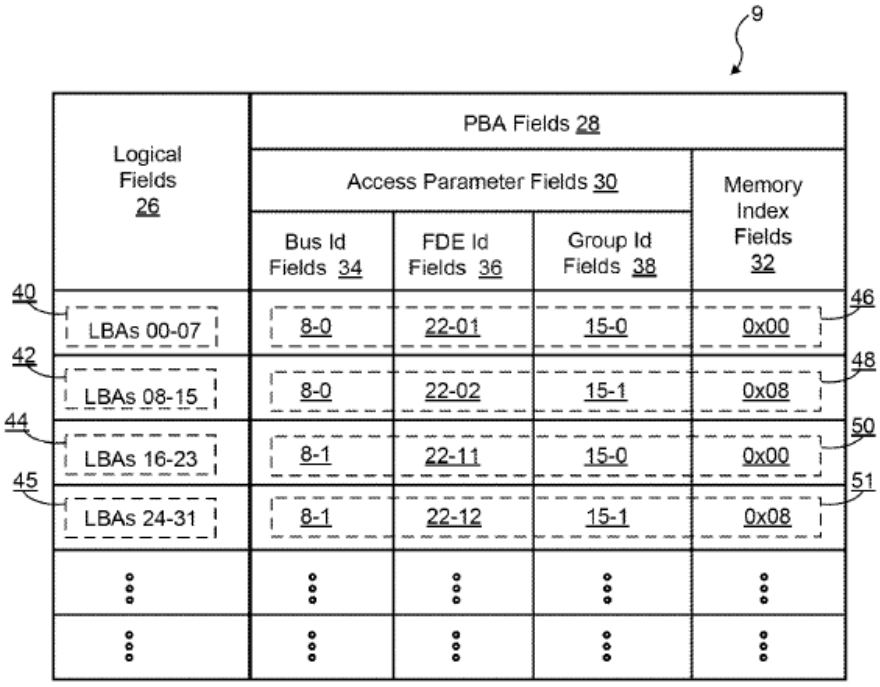

FIG. 2

As illustrated, the mapping table of FIG. 2 correlates sets of consecutive logical block addresses (LBAs) with physical block addresses (PBA). The PBA Fields 28 illustrated in the mapping table of FIG. 2 include Access Parameter Fields 30 and Memory Index Fields 32. The illustrated Access Parameter Fields 30 include Bus ID Fields 34, FDE ID Fields 36, and Group ID Fields 38. These Access Parameter Fields 30 illustrated in the mapping table of FIG. 2 are explained

further with reference to FIG. 1, which illustrates an exemplary electronic storage device using the mapping table of FIG. 2. This electronic storage device of FIG. 1 is reproduced below:

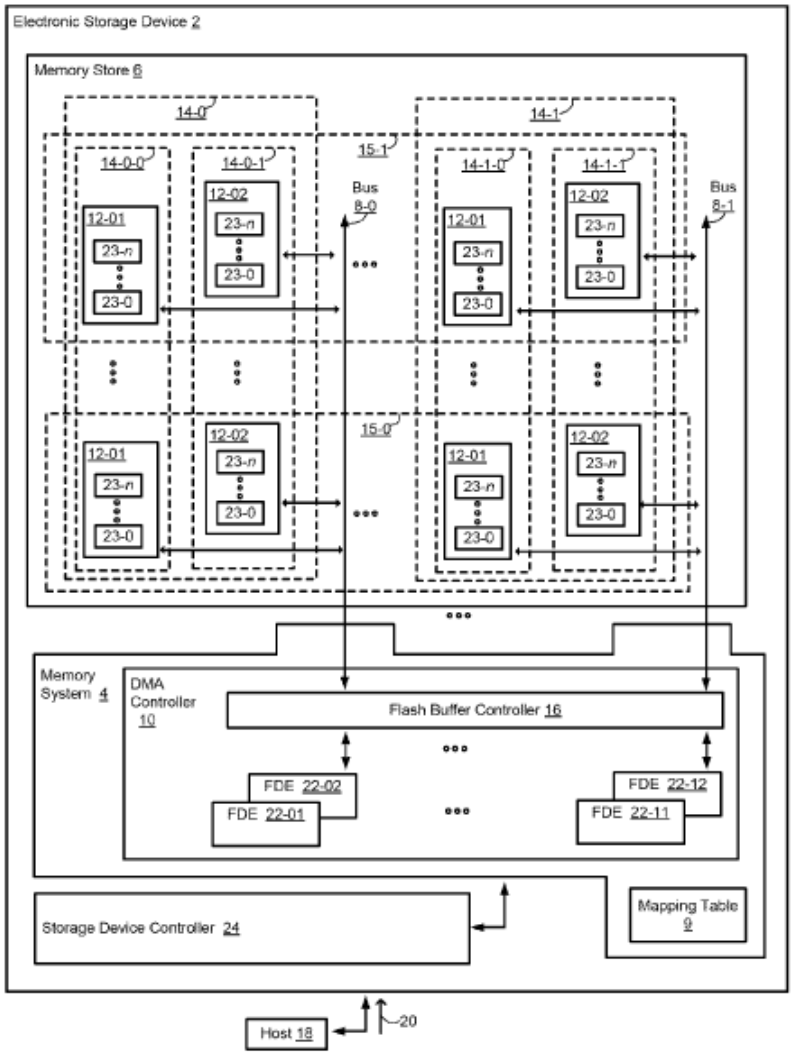

FIG. 1

The electronic storage device 2 of FIG. 1 includes direct memory access engines (FDEs) 22-01, 22-02, 22-11, and 22-12 to control flash memory devices 12-01 and 12-02 and perform DMA (direct memory access) operations on the flash

memory devices 12-01 and 12-02. Flash memory devices 12-01 and 12-02 are arranged into flash array banks 14-0 and 14-1, and also into flash array bank interleaves 14-0-0, 14-0-1, 14-1-0, and 14-1-1. FDEs 22-01 and 22-02 control and communicate with selected flash array bank interleaves 14-0-0 and 14-0-1 of flash array bank 14-0 via bus 8-0. Similarly, FDEs 22-11 and 22-12 control and communicate with selected flash array bank interleaves 14-1-0 and 14-1-1 of flash array bank 14-1 via bus 8-1. As shown in FIG. 1, the '740 Patent also assigns different group identifiers 15-0 and 15-1 to flash memory devices 12-01 and 12-02. As the '740 Patent explains, two flash memory devices 12-01 and 12-02 accessed via a common bus, such as bus 8-0, can share a common group number 15-0 or 15-1 if "these flash devices are controlled by different FDEs, such as FDEs 22-01 or 22-02, respectively." '740 Pat., 6:15-21.

Returning to the mapping table of FIG. 2, the Access Parameter Fields 30, including Bus ID Fields, FDE ID Fields, and Group ID Fields, associate sets of consecutive LBAs with corresponding PBAs. By mapping sets of consecutive LBAs to adjacent PBAs that "differ by at least one access parameter," the mapping table of FIG. 2 "increases the likelihood that memory operations resulting from an I/O transaction request will be optimized because if these memory operations involve data accesses associated with contiguous LBA sets these data accesses will in likelihood occur on different PBAs." '740 Pat., 7:3-15. For example, a memory

operation resulting from an I/O transaction request and involving data accesses associated with sets 40 and 42 of consecutive LBAs from FIG. 2 would access different memory devices in different FDE ID Fields and different Group ID Fields, as shown below.

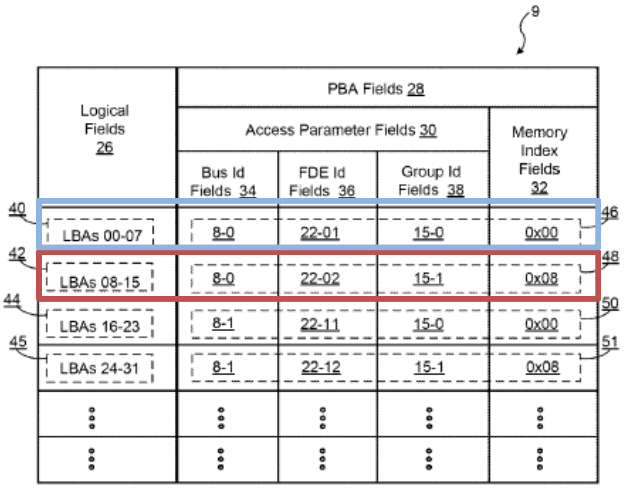

FIG. 2

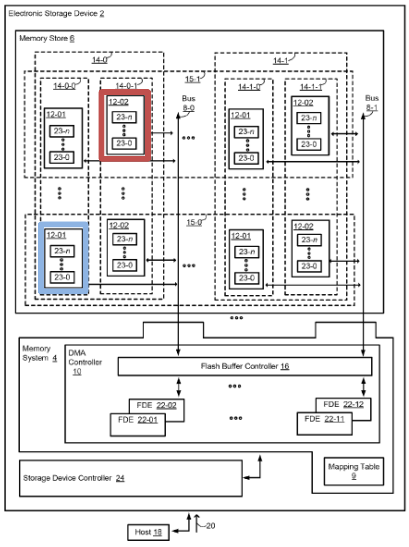

FIG. 1

B. Introduction to the Challenged Claims and Petitioner's Deficient Challenges

Consistent with this disclosure, the challenged claims each recite in relevant part a "mapping table" having first and second logical fields, respectively representing first and second LBA sets that each represent a set of consecutive LBAs. The challenged claims also recite additional features and relationships consistent with those described in the '740 Patent specification and discussed above. Independent claim 1 is specifically directed to a "mapping table for optimizing memory operations performed by an electronic storage device," while

independent claim 32 is directed to an "electronic storage device" comprising, *inter alia*, a "mapping table" having specifically claimed features. Claim 1 recites in full:

1. A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

'740 Pat., 9:63-10:24. Challenged claims 9-15 each depend directly or indirectly from claim 1. Independent claim 32 recites in full:

> 32. An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:
>
> a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;
>
> a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;
>
> a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;
>
> wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs;
>
> and wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.

'740 Pat., 13:29-14:5. Challenged claim 34 depends from claim 32.

Petitioner assert four grounds against these challenged claims 1, 9-15, 32, and 34. In Ground 1, Petitioner contends that challenged claims 1 and 14 are obvious over the Bruce-006[2] reference alone. In Ground 2, Petitioner contends that challenged claims 1 and 14 are obvious over Bruce-006 in view of the SBC[3] reference. In Ground 3, Petitioner contends that challenged claims 1, 9-15, 32, and 34 are obvious over Bruce-006 in view of the Bruce-251[4] reference. Finally, in Ground 4, Petitioner contends that challenged claims 1, 9-15, 32, and 34 are obvious over Bruce-006 in view of the Bruce-251, further in view of SBC.

However, in each challenge, Petitioner incorrectly relies upon Bruce-006 to disclose the claimed "said first and second *LBA sets* each representing *a set of consecutive LBAs*" in the claimed "mapping table" of claim 1. (emphasis added). Bruce-006 fails to disclose this feature, as Bruce-006 uses a single LBA for an entire block, and then uses a second offset address that is not part of Bruce-006's re-map table to identify a page within a flash block or byte within a page for a memory transaction. Bruce-006 therefore fails to disclose an LBA sets, much less sets of consecutive LBAs as claimed, and Petitioner fails to establish any "LBA set" even under Petitioner's own proposed construction of this term. Claim 32

[2] U.S. Patent No. 6,000,006 to Bruce *et al*. ("Bruce-006").

[3] "*American National Standard for Information Technology - SCSI-3 Block Commands (SBC)*" (hereinafter, "SBC").

[4] U.S. Patent No. 5,822,251 to Bruce *et al*. ("Bruce-251").

recites substantially similar features as claim 1 ("a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs") and Bruce-006 fails to disclose or suggest these features as well for the same reason.

While this reason alone is sufficient to defeat the Petition, Petitioner's challenges include other fatal shortcomings. For example, claim 1 also recites in relevant part, "in response to receiving the I/O transaction request, said mapping table *causes* the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, *if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets*." (emphasis added). However, any alleged "optimized memory operations" occurring in any of the asserted references are not "cause[d]" by Bruce-006's re-map table. Bruce-006 additionally fails to disclose any I/O transaction request from a host that is associated with first and second LBAs or first and second LBA sets. While Petitioner adds the SBC reference to Grounds 2 and 4 to include large data transfers, these challenges still include the defect that any alleged "optimized memory operations" occurring in those proposed combinations are not "cause[d]" by the Bruce-006 re-map table. Thus, each proposed combination includes fatal shortcomings.

For these reasons, and as discussed in more detail in Section III below, each ground presented in the Petition is deficient.

II. THE BOARD NEED NOT RESOLVE ANY CLAIM CONSTRUCTION DISPUTES TO DENY THE PETITION

Petitioner contends that the following two terms have been defined in the '740 Patent:

Term	Petitioner's Proposed Construction
Claims 1 and 32: "LBA" (logical block address)	"The term 'LBA', which may also be referred to herein as a logical block address, is intended to represent an address that is part of a logical addressing system (not shown) used by a host." Pet., 6 (citing '740 Pat., 6:37-40).
Claims 1 and 32: "LBA set"	"These LBAs may be grouped into sets of consecutive LBAs, named 'LBA sets.'" Pet., 6 (citing '740 Pat., 6:46-48).

Without expressly agreeing to Petitioner's constructions, and without waiving its right to submit its proposed constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction. For the reasons presented in Section III below, Petitioner fails to

establish any "LBA set" under Petitioner's own proposed construction of this term, and fails to establish any "LBA sets each representing a set of consecutive LBAs" as required by the challenged claims. As a result, Petitioner fails to establish the unpatentability of every challenged claim.

III. PETITIONER'S CHALLENGES FAIL ON THE MERITS

A. Petitioner's Ground 1 based on Bruce-006 Fails to Disclose or Suggest Every Feature Including LBA Sets Each Representing a Set of Consecutive LBAs, as Recited in Claim 1

Petitioner asserts that Bruce-006 renders claim 1 obvious. Pet., 6-27. However, Bruce-006 fails to disclose or suggest every claimed feature of claim 1. This challenge fails.

Claim 1 recites, in relevant part, "said first and second *LBA sets* each representing *a set of consecutive LBAs*," and also "in response to receiving the I/O transaction request, said mapping table *causes* the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, *if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets*." (emphasis added).

The Petition contends that Bruce-006's "logical address" term corresponds to the claimed "LBA" in the '740 Patent, and argues that "an LBA entry in Bruce-006's re-map table corresponds to and represents the grouping of logical addresses

for the consecutive pages in the re-mapped physical block." Pet., 16 (citing Bruce-006, 6:19-20). Based on this, Petitioner contends that "the Bruce-006 LBAs qualify as the claimed LBA sets (or groupings of consecutive logical addresses)." Pet., 16.

This argument misunderstands Bruce-006's disclosure, which does not disclose or suggest any "LBA sets" "representing a set of consecutive LBAs," as claimed. Bruce-006 confirms that an LBA in Bruce-006's re-map table is not an "LBA set" as claimed because Bruce-006 discloses that the "re-map table includes a physical block address (PBA) for *each* possible logical block address." Bruce-006, 5:42-43 (emphasis added). This re-map table arrangement requires that every logical block address in Bruce-006 includes its own entry in the re-map table. Bruce-006 also states that "host requests contain a logical address which includes a logical-block address (LBA) and an offset address that identifies a page within a flash block and perhaps a byte within a page for a read access." Bruce-006, 6:13-17. As such, to identify a page within a flash block or even a byte within a page, a host request in Bruce-006 identifies an LBA, and then uses a separate offset address not included within Bruce-006's LBA to pinpoint the desired page or byte.[5] The offset address used by Bruce-006 identifies a physical relationship and

[5] As an analogy, Bruce-006's LBA is like an interstate exit number, while the offset address is comparable to the directions to an address off the exit.

does not disclose a logical LBA "set." Further, the offset address is not included within Bruce-006's re-map table. Bruce-006's LBA (which Petitioner relies upon to disclose a claimed "LBA set") is not an LBA set, and does not include any sets of LBAs, much less a set of consecutive LBAs.

Petitioner also misrepresents what is disclosed in Bruce-006's column 6, lines 19-20. As noted above, Petitioner cites to this disclosure of Bruce-006 as support for arguing that "an LBA entry in Bruce-006's re-map table corresponds to and represents the grouping of logical addresses for the consecutive pages in the re-mapped physical block." Pet., 16. But Bruce-006's col. 6, lines 19-20 says nothing about "consecutive pages." Instead, it states that "Unified re-map table 20 contains entries preferably for all LBA's." Bruce-006, 6:19-20. This simply reinforces that a re-map table 20 includes an entry for each LBA used by the system, and does not support Petitioner's argument that "the Bruce-006 LBAs qualify as the claimed LBA sets (or groupings of consecutive logical addresses)." Pet., 16.

Further, Petitioner's argument incorrectly blurs the difference between "consecutive pages" in a "physical block" with the concept of "consecutive LBAs," which are not physical but rather logical. Per claim 1, an LBA set represents a "set of *consecutive* LBAs," whereas Bruce-006's LBA is not a "set." Bruce-006's re-map table uses a single LBA entry to identify a physical block

having multiple pages, and does not use any "LBA set" or "set of consecutive LBAs." Bruce-006's LBA entry in the re-map table identifies a block, nothing more. *See* Bruce-006, 8:35 ("This block is currently allocated to LBA 010."). As such, Bruce-006's LBA fails to disclose any LBA set "representing a set of consecutive LBAs" as claimed.

In addition to Bruce-006's failure to disclose any LBA set as claimed, Bruce-006 also fails to disclose or suggest an I/O transaction request initiated by a host being "associated with … first and second LBA sets." Petitioner argues that Bruce-006 teaches "combining the re-map table with block interleaving," and also that "Bruce-006 teaches that it is the re-map table that causes the optimized memory operations to be performed in response to a single I/O transaction request initiated by a host." Pet., 17, 24, 26-27. But Bruce-006 is clear that a host request is only associated with a single LBA, not first and second LBA sets. Bruce-006 discloses that a host request "contain[s] a logical address which includes a logical-block address (LBA) and an offset address that identifies a page within a flash block." Bruce-006, 6:12-17; *see also id*., 2:63-64 ("An entry is selected by a logical address from a host system."), 7:26-27 ("An entry 50 from the unified re-map table is selected by a logical block address (LBA)."), 14:7-9 ("an entry in the plurality of entries selected by a logical address from a host system … ."). In each instance of a host request, Bruce-006 discloses only a single LBA identified by the

host request, and certainly not "first and second LBA sets" each "representing a set of consecutive LBAs" as claimed.

Even when Bruce-006 performs wear-leveling involving more than one PBA, wear-leveling is triggered by the total writes for a single block, which is only associated with a single LBA as explained above. Bruce-006 discloses that "[t]o determine when wear-leveling is required, the total writes for this physical block in flash memory 24 is read from total-write-counter field 46 and compared by comparator 66 to the total-write threshold programmed into register 62." Bruce-006, 7:34-38. Similarly, the "incremental writes since the block's allocation or last wear-leveling is read from incremental-write-counter field 48" and evaluated. Bruce-006, 7:38-42. When these values both exceed a threshold for a single physical block associated with a single LBA, the wear-level controller 70 "then performs a wear-leveling operation to swap the logical address to a different, less-used physical flash block … ." Bruce-006, 7:51-57. Petitioner incorrectly points to Bruce-006's wear-leveling operation as a transaction "associated with … first and second LBA sets" because Bruce-006's wear-leveling operation involves two physical blocks. But the challenged claim requires more, namely that the "transaction request" that is initiated by the host "is associated with said first and second LBA sets." Bruce-006 does not disclose or suggest any host request "associated with said first and second LBA sets."

Finally, Bruce-006 includes another significant deficiency related to the claimed feature of "in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets." Petitioner asserts that "Bruce-006 discloses combining the re-map table with block-interleaving." Pet., 24. But the challenged claim requires more than the possibility that block-interleaving can occur in a system that also includes a re-map table. Rather, as claimed, the "mapping table *causes* the electronic storage device to perform optimized memory operations on memory locations … ." (emphasis added).

Here, Bruce-006's re-map does not "cause[]" interleaving, as required by claim 1. According to Bruce-006, "[i]nterleaving is accomplished by altering the physical address bits assigned to decoders for the flash devices and the physical address bits assigned to decode blocks and pages within a flash device." Bruce-006, 11:22-26. This altering of physical address bits has not been shown by Petitioner to be related to Bruce-006's re-map table in any way. Thus, the claimed condition of "said mapping table causes the electronic storage device to perform optimized memory operations … , if the I/O transaction request [initiated by a

host] is associated with said first and second LBA sets" is not disclosed or suggested by Bruce-006.

For at least these reasons, Petitioner has failed to establish that Bruce-006 discloses or suggests these features of claim 1, and therefore has failed to show that Bruce-006 renders claim 1 obvious. Further, because dependent claim 14 depends from claim 1, Petitioner has failed to show that Bruce-006 renders claim 14 obvious for these same reasons.

B. Ground 2 Based on Bruce-006 and SBC Also Fails to Disclose or Suggest Every Claimed Feature

In Ground 2, Petitioner again relies on Bruce-006 to disclose the claimed "said first and second LBA sets each representing a set of consecutive LBAs," in claim 1. *See* Pet., 35 ("As explained above (p.14-18 and p.18-22), Bruce-006 discloses and renders these claim limitations obvious."). But Bruce-006 fails to disclose these features as recited in claim 1 for the same reasons addressed above in Ground 1. Further, Petitioner does not rely on SBC to remedy the above-discussed shortcoming of Bruce-006. Thus, Petitioner's Ground 2 fails for the same reason presented above for Ground 1.

The asserted combination of Bruce-006 and SBC includes another significant deficiency related to the claimed feature of "in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively

associated with said first PBA and said second PBA, if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets."

Petitioner asserts that "POSITAs would have been motivated to combine Bruce-006 with SBC to use SCSI interface commands like READ(10) and WRITE(10) to achieve large data transfers to or from Bruce-006's flash-memory system." Pet., 36. Petitioner also relies on SBC to teach a READ(10) or WRITE(10) command that "use[s] two or more sequential LBA entries in Bruce-006's re-map table." Pet., 37. However, even in this combination of Bruce-006 and SBC asserted by Petitioner, the process of wear-leveling with interleaving in Bruce-006 is not triggered by the number of blocks identified by any READ(10) or WRITE(10) command. Rather, as explained above, wear-leveling in Bruce-006 is triggered by the total writes for a single block's table entry. Thus, the claimed condition of "said mapping table causes the electronic storage device to perform optimized memory operations … , if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets" is not satisfied in this proposed combination. Namely, any interleaving that may occur in Bruce-006 is unrelated to the number of blocks identified by any READ(10) or WRITE(10) command based on SBC, and is not "cause[d]" by Bruce-006's re-map table for the same reasons explained for Ground 1.

For at least these reasons, Petitioner fails to establish that Bruce-006 and SBC, whether considered alone or in combination, discloses or suggests these features of claim 1, and therefore has failed to show that the asserted combination renders claim 1 obvious. Further, because dependent claim 14 depends from claim 1, Petitioner has failed to show that the asserted combination renders claim 14 obvious for these same reasons.

C. Ground 3 Also Warrants Denial Because the Proposed Combination of Bruce-006 and Bruce-251 Fails to Disclose or Suggest Every Claimed Feature

In Ground 3, Petitioner again relies on Bruce-006 to disclose the claimed "said first and second LBA sets each representing a set of consecutive LBAs," in claim 1. *See* Pet., 49 ("As in ground 1 (p.14-27), Bruce-006 alone discloses and renders the remaining claim limitations obvious."). But Bruce-006 fails to disclose these features as recited in claim 1 for the same reasons addressed above in Ground 1. Further, Petitioner does not rely on Bruce-251 to remedy this above-discussed shortcoming of Bruce-006. Thus, Petitioner's Ground 3 against claim 1 fails for the same reason presented above for Ground 1.

Additionally, claim 32 recites substantially similar features, namely "a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs." Petitioner relies on its Bruce-006 analysis from pp. 14-22 of

the Petition to address this claimed feature, but Patent Owner has established that Bruce-006 fails to disclose or suggest these features. Thus, Petitioner's Ground 3 challenge against claim 32 also fails for these same reasons.

As with Grounds 1 and 2, the asserted combination of Bruce-006 and Bruce-251 in Ground 3 includes another significant deficiency related to the claimed feature of "in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets" as recited in claim 1.

Petitioner asserts that Bruce-251 discloses data "interleaved among the four banks for each flash buffer chip, and also interleaved among chips connected to the two flash busses." Pet., 41 (quoting Bruce-251, 6:57-60). But Bruce-251 discloses that any interleaving that occurs is a result of each DMA controller 12, 16 having "four state machines 40, one for each of four banks of flash-memory chips." Bruce-251, 6:51-61. Further, in Petitioner's proposed combination of Bruce-006 and Bruce-251, Petitioner does not modify the operation of Bruce-251's access of the flash-memory chips using four state machines 40. *See* Pet., 41-46. As such, the claimed condition of "said mapping table causes the electronic storage device to perform optimized memory operations … , if the I/O transaction request

[initiated by a host] is associated with said first and second LBA sets" is not satisfied in this proposed combination. Namely, any interleaving that may occur in the combination of Bruce-006 and Bruce-251 is unrelated to Bruce-006's re-map table, and is not "cause[d]" by Bruce-006's re-map table.

For these same reasons, the asserted combination of Bruce-006 and Bruce-251 fails to disclose or suggest comparable features of claim 32, namely "wherein said mapping table increases the likelihood that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources." As established by both Bruce-006 and Bruce-251, any interleaving that occurs in those references depends on other factors, and is unrelated to Bruce-006's re-map table.

Finally, because Petitioner's Ground 3 challenge against independent claims 1 and 32 fails, Petitioner's Ground 3 also fails to establish the unpatentability of any challenged dependent claim 9-15 and 34.

D. Ground 4 based on Bruce-006, Bruce-251, and SBC Includes the Same Fatal Flaws Addressed Above in Prior Grounds

In Ground 4, Petitioner again relies on Bruce-006 to disclose the claimed "said first and second LBA sets each representing a set of consecutive LBAs," in claim 1. *See* Pet., 76 ("As in ground 1, Bruce-006 alone discloses and renders these claim limitations obvious."). Bruce-006 fails to disclose these features as recited in claim 1 for the same reasons addressed above in Ground 1. Further,

Petitioner does not rely on Bruce-251 or SBC to remedy this above-discussed shortcoming of Bruce-006. Thus, Petitioner's Ground 4 against claim 1 fails for the same reason presented above for Ground 1.

Additionally, claim 32 recites substantially similar features, namely "a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs." Petitioner relies on its prior Bruce-006 analysis from pp. 14-22 of the Petition to address this claimed feature, but Patent Owner has established that Bruce-006 fails to disclose or suggest these features. Thus, Petitioner's Ground 4 challenge against claim 32 also fails for these same reasons.

Moreover, the addition of SBC to the combination of Bruce-006 and Bruce-251 is not asserted to remedy the deficiencies noted above in Patent Owner's response to Ground 3. Thus, for the same reasons presented above with respect to Ground 3, the asserted combination of Bruce-006, Bruce-251, and SBC fails to disclose or suggest "in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets" as recited in claim 1, and "wherein said mapping table increases the likelihood that that the operational load imposed on

the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources," as recited in claim 32. As established by both Bruce-006 and Bruce-251, any interleaving that occurs in those references depends on other factors, and is unrelated to Bruce-006's re-map table.

Finally, because Petitioner's Ground 4 challenge against independent claims 1 and 32 fails, Petitioner's Ground 4 also fails to establish the unpatentability of any challenged dependent claim 9-15 and 34.

IV. CONCLUSION

For the reasons presented above, each Ground fails to establish the unpatentability of any challenged claim, and no *inter partes* review should be instituted.

Dated: August 15, 2023

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 4,864 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a).

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I hereby certify that on August 15, 2023, a true and correct copy of the foregoing document was served via email, by consent, to Petitioner by serving the correspondence email addresses of record as follows:

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