

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

BiTMICRO LLC,

Plaintiff,

v.

KIOXIA AMERICA, INC.
And KIOXIA CORPORATION,

Defendants.

Case No. 6:22-cv-00331-ADA

BiTMICRO LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 6:22-cv-00335-ADA

DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

	Page
I. '939 PATENT	1
A. "predetermined level"	1
B. "means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level"	3
C. "reversing the flow of current between the computing engine and the plurality of super capacitors"	5
D. "means for reversing the flow of current between the computing engine and the plurality of super-capacitors"	7
II. '243 PATENT	7
A. "passive port"	8
B. "a plurality of modules each comprising"	10
III. '740 PATENT	11
A. "optimized memory operations"	11
B. "optimally distributed"	13
C. "memory store"	14
IV. '190 PATENT - "optimal"	15
V. '084 AND '694 PATENTS - "Direct Memory Access (DMA) descriptors" / "DMA controller descriptor"	16
VI. CONCLUSION	17

TABLE OF AUTHORITIES

	Page(s)
CASES	
<i>Acumed LLC v. Stryker Corp.</i> , 483 F.3d 800 (Fed. Cir. 2007).....	2
<i>Allen Eng’g Corp. v. Bartell Indus., Inc.</i> , 299 F.3d 1336 (Fed. Cir. 2002).....	7
<i>Apple, Inc. v. Ameranth, Inc.</i> , 842 F.3d 1229 (Fed. Cir. 2016).....	15
<i>Aristocrat Techs. Austl. Pty. Ltd v. Int’l Game Tech.</i> , 521 F.3d 1328 (Fed. Cir. 2008).....	4
<i>B. Braun Med., Inc., v. Abbott Labs.</i> , 124 F.3d 1419 (Fed. Cir. 1997).....	4
<i>Bd. of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.</i> , 533 F.3d 1362 (Fed. Cir. 2008).....	5
<i>Capital Sec. Sys., Inc. v. NCR Corp.</i> , No. 1:14-cv-1516-WSD, 2016 WL 3517595 (N.D. Ga. June 28, 2016)	5
<i>Catalina Marketing International, Inc. v. Coolsavings.com, Inc.</i> , 289 F.3d 801 (Fed. Cir. 2002).....	10, 11
<i>CCS Fitness, Inc. v. Brunswick Corp.</i> , 288 F.3d 1359 (Fed. Cir. 2002).....	1, 2
<i>Cont’l Circuits LLC v. Intel Corp.</i> , 915 F.3d 788 (Fed. Cir. 2019).....	14
<i>Data Retrieval Tech., LLC v. Sybase, Inc.</i> , No. C 08-5481 VRW, 2010 WL 11586656 (N.D. Cal. Nov. 8, 2010)	16
<i>Digit. Retail Apps, Inc. v. H-E-B, LP</i> , No. 6-19-CV-00167-ADA, 2020 WL 376664 (W.D. Tex. Jan. 23, 2020)	3
<i>Ex Parte Gittleman</i> , 2008 WL 696137 (B.P.A.I. 2008).....	7
<i>In re Cohn</i> , 438 F.2d 989 (C.C.P.A. 1971)	7

TABLE OF AUTHORITIES
(continued)

	Page(s)
<i>Intamin Ltd. v. Magnetar Techs., Corp.</i> , 483 F.3d 1328 (Fed. Cir. 2007).....	9
<i>Interval Licensing LLC v. AOL, Inc.</i> , 766 F.3d 1364 (Fed. Cir. 2014).....	13
<i>Kaufman v. Microsoft Corp.</i> , 34 F.4th 1360 (Fed. Cir. 2022)	9
<i>Luminara Worldwide, LLC v. Liown Elecs. Co.</i> , 814 F.3d 1343 (Fed. Cir. 2016).....	9
<i>Meds. Co. v. Mylan, Inc.</i> , 853 F.3d 1296 (Fed. Cir. 2017).....	9
<i>Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.</i> , 248 F.3d 1303 (Fed. Cir. 2001).....	4
<i>Moleculon Research Corp. v. CBS, Inc.</i> , 793 F.2d 1261 (Fed. Cir. 1986).....	13
<i>Nabors Drilling Techs. USA, Inc. v. Helmerich & Payne Int’l Drilling Co.</i> , No. 3:20-CV-03126-M, 2022 WL 1689444 (N.D. Tex. May 26, 2022)	16
<i>Nautilus, Inc. v. Biosig Instruments, Inc.</i> , 134 S. Ct. 2120 (2014).....	11
<i>Nichia Corp. v. Document Sec. Sys.</i> , No. 2020-2261, 2022 WL 1218036 (Fed. Cir. Apr. 26, 2022)	10, 11
<i>Noah Sys., Inc. v. Intuit Inc.</i> , 675 F.3d 1302 (Fed. Cir. 2012).....	5
<i>Nystrom v. TREX Co.</i> , 424 F.3d 1136 (Fed. Cir. 2005).....	2
<i>Pall Corp. v. Hemasure Inc.</i> , 181 F.3d 1305 (Fed. Cir. 1999).....	15
<i>Pisony v. Commando Constr., Inc.</i> , No. W-17-CV-00055-ADA, 2019 WL 928406 (W.D. Tex. Jan. 23, 2019)	15
<i>Qcue, Inc. v. Digonex Techs., Inc.</i> , No. A-12-CA-484-SS, 2013 WL 4784120 (W.D. Tex. Sept. 5, 2013).....	2

TABLE OF AUTHORITIES
(continued)

	Page(s)
<i>Seachange Int’l, Inc. v. C-COR, Inc.</i> , 413 F.3d 1361 (Fed. Cir. 2005).....	10
<i>Thorner v. Sony Computer Ent. Am. LLC</i> , 669 F.3d 1362 (Fed. Cir. 2012).....	1
<i>Toro Co. v. White Consol. Indus., Inc.</i> , 199 F.3d 1295 (Fed. Cir. 1999).....	1, 2
<i>Verint Sys. Inc. v. Red Box Recorders Ltd.</i> , 166 F. Supp. 3d 364 (S.D.N.Y. 2016).....	5
<i>Versata Software, Inc. v. Zoho Corp.</i> , 213 F. Supp. 3d 829 (W.D. Tex. 2016).....	12

KIOXIA America, Inc., KIOXIA Corporation, and Intel Corporation (collectively, “Defendants”) hereby submit their Reply Claim Construction Brief.

I. ’939 PATENT

A. “predetermined level”

BiTMICRO does not contest any of the salient claim arguments made by Defendants for this claim term. For example, BiTMICRO does not dispute that the ’939 patent specification describes a “predetermined level” as a preset minimum operating voltage at which “the down-converter has insufficient voltage differential to continue proper operation and shuts down.” Case No. 6:22-cv-00331, Dkt. 36 (“Opening Br.”) at 3 (citing ’939 patent at 5:39-43). Nor does BiTMICRO contest that the specification establishes the importance of setting the predetermined level at a voltage necessary for proper operation, explaining that if the voltage “were allowed to fall below the minimum operating voltage of the computer system, the computer system could continue to run with unpredictable and potentially serious results.” *Id.* (citing ’939 patent at 5:44-48, 6:45-49). BiTMICRO does not even dispute that a threshold set below a minimum operating voltage necessary for proper operation would fatally undermine the ’939 patent’s stated goals of ensuring that “a user is able to correctly store large amounts of newly written and modified data” and “rapidly and irretrievably erase data.” *Id.* (citing ’939 patent at 2:33-41).

In view of these undisputed facts, it is evident the patentee acted as its own lexicographer by not only “clearly set[ting] forth a definition” of “predetermined level,” but also “clearly express[ing] an intent to define the term.” *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). In addition, it is well-established that the scope of a claim term is limited where the specification describes a particular aspect “as important to the invention.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366-67 (Fed. Cir. 2002); *Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1301 (Fed. Cir. 1999) (limiting the meaning of a claim term based in

part on statements in the specification describing a particular structure as “important to the invention”). Here, the fact that the specification establishes the critical importance of having the predetermined level fixed at a preset minimum operating voltage necessary for proper operation confirms Defendants’ proposed construction. ’939 patent at 5:44-48, 6:45-49; *see also CCS*, 288 F.3d at 1366-67; *Toro*, 199 F.3d at 1301. Accordingly, BiTMICRO’s assertion that Defendants’ construction imports a limitation from the specification lacks merit. *See* Case No. 6:22-cv-00331, Dkt. 38 (“Resp. Br.”) at 5.

Aside from the requirements in the specification, BiTMICRO also acknowledges that the applicant expressly “*distinguish[ed]* a reference (Manson) cited by the examiner” at least in part on this basis. Resp. Br. 4-5 (emphasis added). The scope of a claim term is limited where “the patentee *distinguished that term from prior art* on the basis of a particular embodiment.” *CCS*, 288 F.3d at 1366-67 (emphasis added). Accordingly, BiTMICRO’s admission regarding the prosecution history further confirms the accuracy of Defendants’ proposed construction.

Finally, BiTMICRO’s reference to different patents, from different inventors, with different written descriptions and claims has no relevance to the proper construction of “predetermined level.” A patentee “is not entitled to a claim construction divorced from the context of the written description and prosecution history” of the asserted patent. *Nystrom v. TREX Co.*, 424 F.3d 1136, 1144-45 (Fed. Cir. 2005). Thus, how a claim term may be used in unrelated patents “merits little consideration.” *Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 809 (Fed. Cir. 2007); *Qcue, Inc. v. Digonex Techs., Inc.*, No. A-12-CA-484-SS, 2013 WL 4784120, at *10 (W.D. Tex. Sept. 5, 2013) (“[A]ll claims are not created equal, and the mere fact [a term] has been used in other patents does not make [it] any more meaningful in the context of the [asserted] [p]atent”).

B. “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level”

BiTMICRO’s brief illustrates why this claim element is indefinite for lack of corresponding structure. BiTMICRO states that “it does not make any sense” to identify a “specific structure” for this term. Resp. Br. 8-9. But it is black letter law that the specification *must* not only disclose a corresponding structure for a means-plus-function term, but *must* also “clearly link[] or associate[] that structure to the function recited in the claim.” *Digit. Retail Apps, Inc. v. H-E-B, LP*, No. 6-19-CV-00167-ADA, 2020 WL 376664, at *3 (W.D. Tex. Jan. 23, 2020). Because the ’939 patent does not meet this requirement, it is indefinite as a matter of law.

BiTMICRO’s arguments expose the absence of corresponding structure in the specification of the ’939 patent. BiTMICRO begins its brief by block-quoting a portion of the specification discussing an up-converter, down-converter, and various circuitry. Resp. Br. 6-7 (citing ’939 patent at 3:28-3:48, 3:49-4:8, Fig. 1). But these excerpts make no mention of deactivating any component, much less “deactivating a plurality of super capacitors to cut off power to the computing engine.” *See id.* BiTMICRO then block-quotes a different portion of the specification, *id.* at 7-8 (citing ’939 patent at 5:17-43), that also discloses nothing about “deactivating a plurality of supercapacitors.” Indeed, it is unclear from the specification what actions deactivating supercapacitors requires. BiTMICRO itself seems unsure whether it “mean[s] the capacitors are unable to take a charge again” or “something else.” Resp. Br. 9. While raising these questions in the context of Defendants’ position, BiTMICRO never explains what “deactivating a plurality of supercapacitors” means. The reason for that is simple. The patent does not address this issue, and thus BiTMICRO cannot identify any structure that performs the function.

Structures that BiTMICRO vaguely suggests as candidates for corresponding structure are not clearly linked to the claimed function. BiTMICRO underlines the charge level sensors, but

there is nothing to indicate the sensors “deactivate” the super-capacitors. Resp. Br. 7-8. The sensors simply “inform the computer system that the super-capacitor voltage has fallen below the fully charged and partially charged levels.” ’939 patent at 5:36-39, 6:37-40. Likewise, BiTMICRO underlines the down-converter that is eventually “shut down,” but there is also nothing to indicate that the down-converter “deactivates” the super-capacitors. In any event, relying on the down-converter is illogical. As its name implies, a down-converter simply converts a high voltage signal to a lower voltage one. ’939 patent at 3:46-48. It does not deactivate any type of structure, as the specification makes clear. Further, BiTMICRO invokes generic “circuitry” or “elements of the circuitry” that it admits are “not expressly stated” in the specification but would allegedly be “obvious to laypersons and POSITAs alike.” Resp. Br. 8. Such alleged structure is immaterial: “It is not enough for the patentee simply to state or later argue that persons of ordinary skill in the art would know what structures to use to accomplish the claimed function.” *Aristocrat Techs. Austl. Pty. Ltd v. Int’l Game Tech.*, 521 F.3d 1328, 1337 (Fed. Cir. 2008).

Accordingly, BiTMICRO does not point to any structure that is ***clearly linked*** to “deactivating the plurality of super capacitors,” as it must to identify corresponding structure. *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311-12 (Fed. Cir. 2001) (finding a means plus function term indefinite because “there is no clear link or association between the disclosed structures and the function recited” in the claim); *B. Braun Med., Inc., v. Abbott Labs.*, 124 F.3d 1419, 1425 (Fed. Cir. 1997) (confirming that a claim term was indefinite because “neither the specification nor the prosecution history contains any indication that the [structure] corresponds to the recited function.”). Thus, the claim is indefinite.

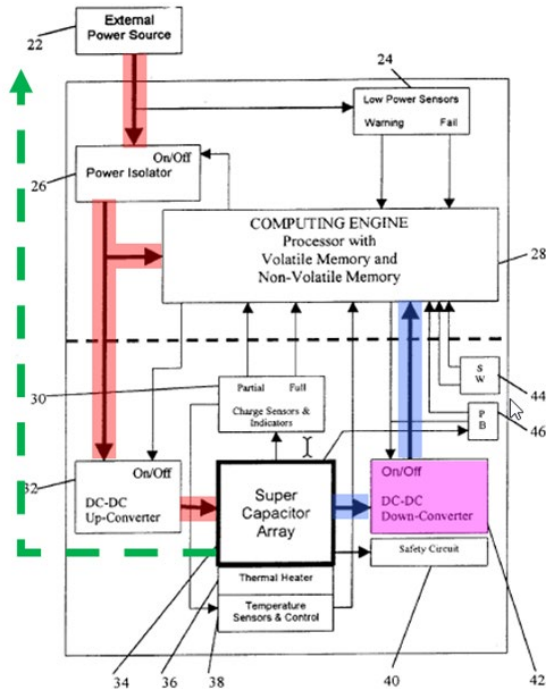
Likewise, BiTMICRO’s attempt to equate the “means for activating” and the “means for deactivating” is fundamentally flawed. See Resp. Br. 6. “Different claim terms are presumed to

have different meanings.” *Bd. of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008). Here, this difference is underscored by the fact that claim element 10[a] recites specific functionality for activating the super capacitors “based upon *power being removed from the computer system*,” while claim element 10[c] recites functionality for deactivating the capacitors “based upon the plurality of *super capacitors discharging to a predetermined level*.” ’939 patent, Cl. 10. This distinct functionality, which BiTMICRO omits from its discussion of the claim terms, negates BiTMICRO’s contention that the claim elements are “mirror images.”¹ This is underscored by the fact that BiTMICRO’s brief emphasizes different supposed structures for these two claim elements. *See* Resp. Br. 7-8.

Finally, BiTMICRO’s suggestion that expert testimony is necessary to invalidate the claim for indefiniteness (Resp. Br. 8), “misstates the applicable law.” *Verint Sys. Inc. v. Red Box Recorders Ltd.*, 166 F. Supp. 3d 364, 378 (S.D.N.Y. 2016). “[T]he Federal Circuit has . . . made clear that expert testimony is not a per se requirement and that when a specification is devoid of structure—as [Defendants] contend[]—the skilled artisan is unnecessary to find the claim indefinite.” *Id.*; *Capital Sec. Sys., Inc. v. NCR Corp.*, No. 1:14-cv-1516-WSD, 2016 WL 3517595, at *10 & n.9 (N.D. Ga. June 28, 2016) (same); *Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1318-19 (Fed. Cir. 2012) (affirming indefiniteness finding for a means-plus-function term without expert testimony). None of BiTMICRO’s cited cases purport to state a different rule of law. Resp. Br. 8.

C. “reversing the flow of current between the computing engine and the plurality of super capacitors”

¹ Notably, the applicant added the “means for deactivating” limitation during prosecution to overcome an anticipation rejection over a prior art reference, which taught the “means for activating” claim element. Ta Decl., Ex. I at 6-7. Accordingly, if the “means for deactivating” limitation is nothing more than a mirror image of the “means for activating,” as BiTMICRO now contends, the claim is invalid over the prior art. Such an interpretation would also render the applicant’s statement to the Patent Office meaningless.



BiTMICRO’s arguments for this term are directly contradicted by the specification of the ’939 patent. As explained in Defendants’ Opening Brief—and illustrated again in annotated Figure 1 to the left—the specification makes clear that current *flows in only one direction* from the external power source to the capacitors, and also *flows in only one direction* from the capacitors to the computing engine. Opening Br. 10-11. Notwithstanding this fact,

BiTMICRO divines an entirely different *current flow* that requires movement in the *opposite* direction—i.e., from the capacitors “to the shared power plane of the EPS, Power Isolator and CE.” Resp. Br. 11. BiTMICRO identifies nothing in either the specification or prosecution history supporting such a current flow. Accordingly, BiTMICRO’s attempt to rewrite the ’939 patent’s specification to fit its litigation-based theory should be rejected.

Regardless, BiTMICRO’s attorney argument is irrelevant. The plain claim language requires the flow of current to be reversed between the *computing engine* and the *super capacitors*—not between the super capacitors and the power isolator, the external power source, or a so-called “power plane.” And as the specification makes clear, current flows in *only one direction* from the super capacitors, through a *down-converter*, to the computing engine.² For this

² This is apparent from both the specification’s description and Figure 1, shown above. *See, e.g.,* ’939 patent at 3:46-48 (noting that voltage from the capacitors must flow through a down-converter to convert it to a voltage that usable by the computing engine); Figs. 3 & 5 (explaining that voltage must be discharged “through the down converter”).

to fulfill the requirement of “reversing the flow of current between the computing engine and the . . . super capacitors” upon activation, current would need to flow in the opposite direction during normal operation. That is, current would need to flow from the computing engine to the super capacitors along the same pathway. But as BiTMICRO expressly acknowledges, the “*external power supply* (EPS)” —not the computing engine— “supplies current to the . . . *capacitor*” during normal operation. Resp. Br. 11. Thus, activation of the super capacitors cannot “revers[e] the flow of current between the computing engine and the plurality of super capacitors” as recited in the claim. Accordingly, this claim term is indefinite. *See Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002); *In re Cohn*, 438 F.2d 989, 993 (C.C.P.A. 1971); *Ex Parte Gittleman*, 2008 WL 696137, at *4 (B.P.A.I. 2008); *see also* Opening Br. 9-11.

D. “means for reversing the flow of current between the computing engine and the plurality of super-capacitors”

BiTMICRO’s argument consists of two sentences, alleging that this claim is not indefinite “for the same reasons as discussed with respect to the previous term.” Resp. Br. 12. But as illustrated in both the previous section and Defendants’ Opening Brief, the ’939 patent does not teach any functionality for “reversing the flow of current between the computing engine and the plurality of super capacitors.” Opening Br. 11-12; *supra* § I.C. On that basis alone, this claim term is indefinite. Regardless, BiTMICRO also makes no attempt to identify any structure for the recited function beyond a single sentence referencing generic “circuitry” in “the cited passages of the specification.” Resp. Br. 12. As Defendants have explained, however, the ’939 patent does not teach any component, circuitry, structure, or other mechanism that reverses the flow of current between the computing engine and the super capacitors. Opening Br. 11-12; *supra* § I.C. Accordingly, this term is indefinite for lack of corresponding structure.

II. ’243 PATENT

A. “passive port”

BiTMICRO’s argument that applicants did not define “passive port” strains credulity. As explained (Opening Br. 13-15), during prosecution the examiner rejected pending claim 14 as indefinite due to the term “passive port” (Ta Decl., Ex. F at 22-23)—which did not appear anywhere in the specification. To overcome this rejection, applicants added “passive port” to the specification and expressly defined it: “The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module . . . *is named ‘passive port.’*” *Id.* at 3. Applicants told the examiner that “Applicants may be their own lexicographers” specifically in connection with this amendment and repeated their definition. *Id.* at 23 (excerpted above). Defendants’ construction tracks this language verbatim.

MPEP 2173.02. Applicants may be their own lexicographers. MPEP 2173.01. The Specification at p. 21, line 7 through p. 22, line 4, as amended in the “Amendments to the Specification” section above, recites in part:

...A **connection** between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named “passive port”, such as passive ports 1909 illustrated in Figure 19. (*Emphasis added*).

The above description should be read in conjunction with amended Figure 19, which shows that a passive port 1909 **connects** “a passive ball”, such as passive ball X2, “on one surface of a SDRAM module”, such as SDRAM module 0, and a passive pad”, such as passive pad X3, “on another surface of the same DRAM module”, such as SDRAM module 0. Thus, “a connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module” is a “passive port”. The above amendments render moot the First 35 USC § 112,

To avoid the consequences of “their own lexicograph[y],” BiTMICRO argues, incorrectly, that Defendants mischaracterize the prosecution history. It claims (Resp. Br. at 16) that because applicants’ remarks to the examiner bolded the word “connection,” the Court should construe “passive port” as merely a connection. But applicants did not say that “passive port” was *any* connection between a passive ball and pad—they unambiguously defined the term as a *specific type* of connection, one “between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module.” Ta Decl., Ex. F at 3, 23. BiTMICRO then asserts (Resp. Br. at 16) that applicants’ remarks merely identified “example connections,” because applicants used the phrase “such as.” To the contrary, applicants used “such as” to show how their

overall definition applied to the specific embodiment of Figure 19. Ta Decl., Ex. F at 23 (“such as passive ports 1909 illustrated in Figure 19”). BiTMICRO then notes that lexicography is an “exacting” standard (Resp. at 16)—but neither of its cited cases involves the situation here, where applicants *affirmatively represented* that they were acting as “their own lexicographers” when providing a definition. Further, in each case, the Federal Circuit *limited* claims based on the specification. *See Meds. Co. v. Mylan, Inc.*, 853 F.3d 1296, 1308-09 (Fed. Cir. 2017) (construing “efficient mixing” term “to require using the efficient mixing conditions of Example 5,” where this was “the specification’s only clear delineation of what ‘efficient mixing’ is”); *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353-54 (Fed. Cir. 2016) (construing claims to require chaotic pivoting where “the specification disclaims non-chaotic pivoting”).

BiTMICRO argues (Resp. Br. 14) that Intel’s construction excludes embodiments, pointing to Figure 19. This is incorrect; applicants told the examiner explicitly that Figure 19 was consistent with their definition. Ta Decl., Ex. F at 3, 23 (“The above description should be read in conjunction with amended Figure 19[.]”). The only other embodiment that involves “passive port” is depicted in Figure 21a-b. ’243 patent at 10:8 (as modified by Certificate of Correction) (“In effect, each of these serial chain circuits functions as a passive port.”); Ta Decl., Ex. F at 5. That a serial chain circuit *functions in effect* as a passive port does not mean that it is *the same as* a passive port. To the extent other disclosed embodiments are broader than the “passive port” claims—for example, because they include modules other than SDRAM—a “patentee may draft different claims to cover different embodiments.” *Intamin Ltd. v. Magnetar Techs., Corp.*, 483 F.3d 1328, 1337 (Fed. Cir. 2007). *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022) is not applicable because the construction there was not supported by any definitional statements and was inconsistent with the sole embodiment. In contrast, the applicants here specifically defined “passive port” and

confirmed to the Patent Office that embodiments (*e.g.*, Fig. 19) were consistent with that definition.

Finally, BiTMICRO argues (Resp. Br. 15) that claim differentiation weighs against Defendants' construction because claim 2 recites a limitation consistent with applicants' definition. However, claim 2 also recites a new limitation, "wherein the one or more passive port forms a ladder like routing path," and thus is already different in scope from claim 1. Further, claim differentiation "is not a hard and fast rule" and "will be overcome by a contrary construction dictated by the written description or prosecution history." *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005) (citations omitted).

B. "a plurality of modules each comprising"

BiTMICRO fails to rebut Intel's showing that the plain and ordinary meaning of this term should control. The preamble of claim 1 is "[a] stacked module comprising." Accordingly, "a plurality of modules *each* comprising" is a limitation. BiTMICRO is wrong that a preamble must include all words that appear before the first colon; the Federal Circuit has held otherwise. *Nichia Corp. v. Document Sec. Sys.*, No. 2020-2261, 2022 WL 1218036, at *4 (Fed. Cir. Apr. 26, 2022) (holding, for a claim reciting "[a] display **comprising** a plurality of plastic leaded chip carrier LEDs, the plastic leaded chip carrier LEDs **each comprising**," that only "[a] display comprising" was the preamble and the remaining text before the second "comprising" was a limitation). BiTMICRO's cited case of *Application of Dean*, 291 F.2d 947, 949 (C.C.P.A. 1961) is not applicable, because *Dean* did not involve a claim that recited "comprising" twice before a colon.

As Intel explained previously (Opening Br. 17-18), even if this Court determines that the disputed term is part of the preamble of claim 1, it is still limiting because a term in the claim body depends on it for antecedent basis. *Catalina Marketing International, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801 (Fed. Cir. 2002), relied upon by BiTMICRO, actually supports Intel: there, unlike here, a preamble *not* repeated in the claim body was not limiting (*Id.* at 807-08, 810), and a

preamble *repeated in the claim body* (as in '243 patent claim 1) *was* limiting. *Id.* at 810-11.

The specification contradicts BiTMICRO's assertion (Resp. Br. 19) that only the topmost module in Figure 21a can contain a control circuit. Rather, the specification states that Figures 21a and 21b—which BiTMICRO ignores—describe aspects of the *same embodiment*: “FIG. 21a shows how this [connection] technique is implemented in the stacking method ... Regarding the top module [of Figure 21a], the serial chain termination and branching to other pads is shown in FIG. 21b.” '243 patent at 9:61-10:10 (as modified by Certificate of Correction). In the embodiment of Figures 21a-b, all modules are identical and each includes a control circuit: “Since **the modules are identical** [in Fig. 21a], this routed signal passes through ... the stack until it reaches the OUT pad 2114 of the main board for external access ... **All modules** [in Fig. 21b] **have a control circuit** that includes a selectable buffer 2115 that tri-states the input when pulled low.” *Id.* at 10:5-32 (as modified by Certificate of Correction) (emphasis added). Thus, the specification expressly discloses that the control circuit in the topmost module in Figures 21a and 21b is included in *every module in the stack*. And it is only *because* the modules are identical that the embodiment can function as described. *See* Opening Br. 16-17.

III. '740 PATENT

A. “optimized memory operations”

Assigning an alleged “plain meaning” to “optimized memory operations” would improperly guarantee that *no one* will understand the scope of claim 1 and its dependents with reasonable certainty. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). Even the dictionary definition BiTMICRO urges shows why: “optimization” can refer to “maximiz[ing] or minimize[ing] *some* performance index.” Resp. Br. 21 (emphasis added). The claim language provides no performance index and no hint of objective criteria against which to assess memory operations. It is indefinite.

BiTMICRO's arguments regarding the file history also fail. BiTMICRO cites *Aladdin Manufacturing Corp. v. Brumlow Mills, Inc.*, but the file history in that case specifically addressed an indefiniteness issue. No. 4:19-cv-00058-WMR, 2020 WL 9594314, at *8 (N.D. Ga. June 25, 2020). The file history of the '740 patent, in contrast, addresses a *written description rejection*, not indefiniteness, and thus *Aladdin* is inapposite. Ex. 9 at 17-23. Moreover, the '740 patent file history arguments all point to Figure 2 and its associated text—which is the only disclosed example of a mapping table that “increases the likelihood that memory operations . . . will be optimized.” '740 at 7:9-11. As the court concluded in *Versata Software, Inc. v. Zoho Corp.*, 213 F. Supp. 3d 829, 836-37 (W.D. Tex. 2016), mere written description examples are insufficient to demarcate the indefinite scope of otherwise unbounded claim terms with reasonable certainty.

BiTMICRO's attempt to create multiple disclosed optimizations (Resp. Br. 22) is also mistaken. Claim 1 requires memory operations—not the mapping table—to be optimized. “Contiguous arrangement of LBA sets,” “adjacency between LBA sets,” and “adjacent PBAs differing by at least one access parameter,” referenced by BiTMICRO are all aspects of Figure 2's mapping table that together increase the likelihood of optimized memory operations as explained in the '740 patent at 7:3-11:

“[S]torage device 2 initializes mapping table 9 by creating an association between these LBA sets and PBAs so that adjacent LBA sets are mapped to PBAs, and any two adjacent PBA differ by at least one access parameter. . . . This mapping association among LBA sets and PBAs increases the likelihood that memory operations resulting from an I/O transaction request will be optimized.”

As explained in the Opening Brief, restricting claim 1 to the Figure 2 example would make dependent claim 2 redundant and meaningless because both claims would require two LBA sets with differing access parameters. Opening Br. 21. In response, BiTMICRO argues erroneously that non-adjacent LBA sets 40 and 45 (red in BiTMICRO's brief) could be an example of claim 1

but not claim 2, which recites “adjacent LBA sets.” Resp. Br. 23. But Figure 2 also has LBA sets 40 and 42 (blue) which are adjacent as recited in claim 2. Moreover, any mapping table like Figure 2 with two or more LBA sets as recited in claim 1 will necessarily have adjacent LBA sets, even if it also has non-adjacent LBA sets, as will be true whenever there are three or more LBA sets in the table. BitMICRO next argues that claim 2 has differing scope because it recites that the LBA sets “are logical block addresses used by the host for addressing said data.” Yet, that is how “LBA” is defined in the written description. *See* ’740 at 6:37-40 (“The term ‘LBA’. . . is intended to represent an address that is part of a logical addressing system . . . used by a host.”). Thus, neither the “adjacent” limitation nor the host “logical addressing system” limitation can distinguish claim 2 from claim 1 if claim 1 is limited to the Figure 2 embodiment in the written description. Resort to the specification fails to remedy the indefinite scope of “optimized memory operations.”³

B. “optimally distributed”

Regarding indefiniteness of claim 32’s “optimally distributed” limitation, BiTMICRO’s reliance on the file history and other examples of “optimized memory operations” fails for the reasons explained in the previous section. BiTMICRO’s remaining argument misstates the Opening Brief’s explanation. Defendants are not arguing that claim 32 would cover a mapping table with just one LBA set. The claim requires at least two LBA sets: “a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA.” The problem is that claim 32 does not limit, and therefore extends, its reach to “I/O transaction request[s]” with memory operations that use just one PBA. It is dependent claim 34 that adds the requirement of memory operations using both the first and second PBAs. Claim 32 requires that the mapping table

³ Contrary to BiTMICRO’s suggestion (Resp. Br. 24), expert testimony is not required to prove indefiniteness. *See, e.g., Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 n. (Fed. Cir. 2014); *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1270 (Fed. Cir. 1986).

“increase[] the likelihood that an operational load” “will be optimally distributed across storage device resources.” The ’740 patent explains how the Figure 2 embodiment accomplished the function when memory operations use two PBAs. But the ’740 patent (including claim 32) says nothing about how to achieve that outcome with an I/O transaction using just one PBA, leaving the scope of the “optimally distributed” limitation indefinite.⁴

C. “memory store”

BiTMICRO seeks to limit “memory store” to “non-volatile, solid-state storage, e.g., flash,” but the patent does not support that position or clearly disavow other types of memory store.⁵ The specification provides an exemplary instance of a “[m]emory store” that “*may be configured* to include a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs.” ’740 patent, 4:54-56 (emphasis added). BiTMICRO interprets “may be configured” to refer to the manner in which the solid state memory device may be coupled to a set of buses, rather than as permitting non-SSD memory devices. Resp. Br. 26. But that passage refers to a memory store that “may be configured to *include* a set of solid state memory devices” and is not focused on the manner of coupling. *Id.* (emphasis added). BiTMICRO also argues that the ’740 patent equates “memory store” with non-volatile, solid state storage, but the specification belies that notion. For example, independent claim 1 recites a “memory store,” while dependent claims 7, 8, and 15 recite that the memory store comprises either “a plurality of flash memory devices” or a “set of solid state memory devices.” BiTMICRO is wrong that the presumption of claim differentiation does not apply simply because some of the dependent claims have additional

⁴ As discussed previously (*supra* FN 3), expert testimony is not required to show indefiniteness.

⁵ Disclosure of one exemplary method “does not automatically lead to finding a clear disavowal of claim scope.” *Cont’l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019); *Phillips*, 415 F.3d at 1323 (“[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.”).

limitations. *See, e.g., Pisony v. Commando Constr., Inc.*, No. W-17-CV-00055-ADA, 2019 WL 928406, at *3 (W.D. Tex. Jan. 23, 2019) (crediting claim differentiation argument despite additional elements in dependent claim). If “memory store” were limited to a solid state memory or flash device, dependent claim 15 would not need to redundantly recite “wherein said memory store includes a set of ~~solid state memory devices~~ [memory stores] that are coupled to a set of buses....” *See Apple, Inc. v. Ameranth, Inc.*, 842 F.3d 1229, 1237 (Fed. Cir. 2016). BiTMICRO further argues that the following statement equates “solid state storage” with “non-volatile memory”: “Electronic storage devices that respectively employ a memory system that includes memory devices, memory chips, or modules that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices.” Resp. Br. 26; ’740 patent, 1:28-32. But that statement does not equate “non-volatile memory” with “solid state storage devices.” Rather, it points to particular “electronic storage devices” “that use non-volatile memory cells” and notes that those devices can “sometimes” be referred to as “solid state storage devices.” A non-volatile memory device need not be a solid-state drive. Indeed, claim 19, which recites “wherein said first and second memory devices include *non-volatile solid state memory cells*,” specifically identifies memory cells that are both “non-volatile” and “solid-state,” demonstrating that the applicant does not use those terms interchangeably. “Memory store” should be given its plain and ordinary meaning.⁶

IV. ’190 PATENT - “optimal”

⁶ BiTMICRO’s Complaint demonstrates that the plain and ordinary meaning of “memory store” can include even volatile memory stores. *See* Opening Br. 30. That those statements were allegedly made without the benefit of discovery into “the operation of Intel’s accused products” (Resp. Br. 26) is immaterial because claim construction “is independent of the device charged with infringement.” *Pall Corp. v. Hemasure Inc.*, 181 F.3d 1305, 1308 (Fed. Cir. 1999). BiTMICRO’s understanding of “memory store,” on the other hand, is relevant to the term’s plain and ordinary meaning and demonstrates the inconsistency in limiting that term to non-volatile memory stores.

The term “optimal”—as used in the ’190 patent to describe a “first device profile” for a “data type”—is indefinite. The patent does not explain how a memory device would select an optimal device profile based on a data type in the innumerable situations the device might encounter. BiTMICRO relies entirely on a few optimization examples in the specification, but these examples do not address the full scope of the claims, which extend to device profile optimization in all events. Resp. Br. 28. The patent does not specify the criteria for such broad optimization.⁷ *Data Retrieval Technology, LLC v. Sybase, Inc.* is instructive. No. C 08-5481 VRW, 2010 WL 11586656, at *4–5 (N.D. Cal. Nov. 8, 2010). There, the court found claims indefinite despite example embodiments in the specification demonstrating how a database might be “optimized” because there were potentially hundreds of database characteristics that could be improved and the process of optimization could result in tradeoffs that increase performance in some areas but diminish performance in others. *Id.* By focusing on examples in the specification, the plaintiff “fail[ed] to grasp ‘the distinction between using the specification to interpret the meaning of a claim and importing limitations from the specification into the claim.’” *Id.* Indeed, while examples in a specification can help define unclear claim terms, they do not limit the claims. *Id.* Here, the limited specification examples do not define the criteria for what is “optimal” or provide the metes and bounds of that indefinite term.⁸ *See id.*

V. ’084 AND ’694 PATENTS - “Direct Memory Access (DMA) descriptors” / “DMA controller descriptor”

Intel and BiTMICRO agree that “DMA descriptor” should be given its plain and ordinary

⁷ *See, e.g., Nabors Drilling Techs. USA, Inc. v. Helmerich & Payne Int’l Drilling Co.*, No. 3:20-CV-03126-M, 2022 WL 1689444, at *14–16 (N.D. Tex. May 26, 2022) (“[T]here is no support in the specification establishing any particular criteria—such as efficiency, speed, or length—as optimization parameters” unlike cases where “the characteristic to be optimized was defined or known, or the specification provided guidance on relevant criteria to evaluate”).

⁸ As discussed previously (*supra* FN 3), expert testimony is not required to rule on indefiniteness.

meaning. But while BiTMICRO asserts no construction is necessary (Resp. Br. 30), this term would not be known to laypersons. The meaning this term has to a POSITA should be made clear.

Significantly, BiTMICRO does not argue that Intel’s construction is *inconsistent* with how the term is used by the specification and claims, nor does it dispute that a DMA controller needs each piece of information to perform a DMA transfer. Instead, BiTMICRO picks at aspects of the construction without disputing the fundamental premise. BiTMICRO argues (Resp. Br. 32) that the “byte count” aspect of the construction is too narrow, because other groupings of data (word, sector, or “chunk” count) could specify the size of the data or code to be transferred—but it does not dispute the larger point, that a DMA controller must know the size of what is to be transferred to perform DMA transfers.’084 patent at 2:56-58, 3:51-54. Various groupings of data are possible in the context of the claimed DMA descriptors (which, being used in an embedded system, will ultimately relate to bytes); but regardless of the grouping, the descriptor must convey a size. Alpert Decl. ¶ 15. BiTMICRO also argues that source and destination addresses do not *both* need to be included, pointing to specialized scenarios where a source or destination has been pre-set or fixed. Resp. Br. 32-33. BiTMICRO’s examples confirm that a DMA controller must know both source and destination locations to perform a DMA transfer. *E.g.*, Resp. Br. Ex. 16 (Alpert Dep. Tr. (rough)) at 30:6-15. And the patents do not describe any scenario in which a DMA controller *already has* source or destination information—to the contrary, the DMA descriptor is the only vehicle for providing DMA controllers with information relating to a DMA transfer. *See* ’084 patent at 3:47-61, 7:29-39, 7:52-66, 8:3-24, Figs. 7-8. BiTMICRO has thus failed to rebut the showing that a DMA controller requires *each of* a source, destination, and size to perform a transfer, and the patents do not describe any way to provide this information apart from the DMA descriptor.

VI. CONCLUSION

Defendants respectfully request that the Court adopt their proposed constructions.

Dated: December 14, 2022

Respectfully submitted,

/s/ Chad S. Campbell

Chad S. Campbell
CSCampbell@perkinscoie.com
Tyler Bowen (*admitted pro hac vice*)
tbowen@perkinscoie.com
PERKINS COIE LLP
2901 North Central Avenue, Suite 2000
Phoenix, AZ 85012
Tel: (602) 351-8000
Fax: (602) 648-7000

Christina J. McCullough, WA 47147
cmccullough@perkinscoie.com
PERKINS COIE LLP
1201 Third Avenue, Suite 4900
Seattle, WA 98101-3099
Tel: (206) 359-6897
Fax: (206) 359-7897

Nancy Cheng (*admitted pro hac vice*)
ncheng@perkinscoie.com
PERKINS COIE LLP
3150 Porter Drive
Palo Alto, CA 94304
Tel: (650) 838-4325
Fax: (650) 838-4525

Janice L. Ta, Texas 24075138
JTa@perkinscoie.com
PERKINS COIE LLP
405 Colorado St., Suite 1700
Austin, TX 78701
Tel: (737) 256-6100
Fax: (737) 256-6300

Counsel for Defendant Intel Corporation

/s/ Douglas F. Stewart

Douglas F. Stewart
WA State Bar # 34068
Jared D. Schuettenhelm
WA State Bar # 46181
Patrick J. Connolly

WA State Bar # 46767
Bracewell LLP
701 5th Avenue, Suite 6200
Seattle, WA 98104
Telephone: (206) 204-6200
Facsimile: (800) 404-3970
doug.stewart@bracewell.com
jared.schuettenhelm@bracewell.com
patrick.connolly@bracewell.com

David J. Ball
NY State Bar # 4315099
Bracewell LLP
31 W 52nd Street, Suite 1900
New York, NY 10019-0019
Telephone: (212) 508-6100
Facsimile: (800) 404-3970
david.ball@bracewell.com

Timothy R. Geiger
Texas State Bar No. 24078552
Bracewell LLP
711 Louisiana Street, Suite 2300
Houston, Texas 77002-2781
Telephone: (713) 223-2300
Facsimile: (800) 404-3970
tim.geiger@bracewell.com

*Counsel for KIOXIA America, Inc. and
KIOXIA Corporation*

CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that, on December 14, 2022, all counsel of record who have appeared in this case are being served with a copy of the foregoing DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF via the Court's CM/ECF system.

Dated: December 14, 2022

Respectfully submitted,

/s/ Chad S. Campbell