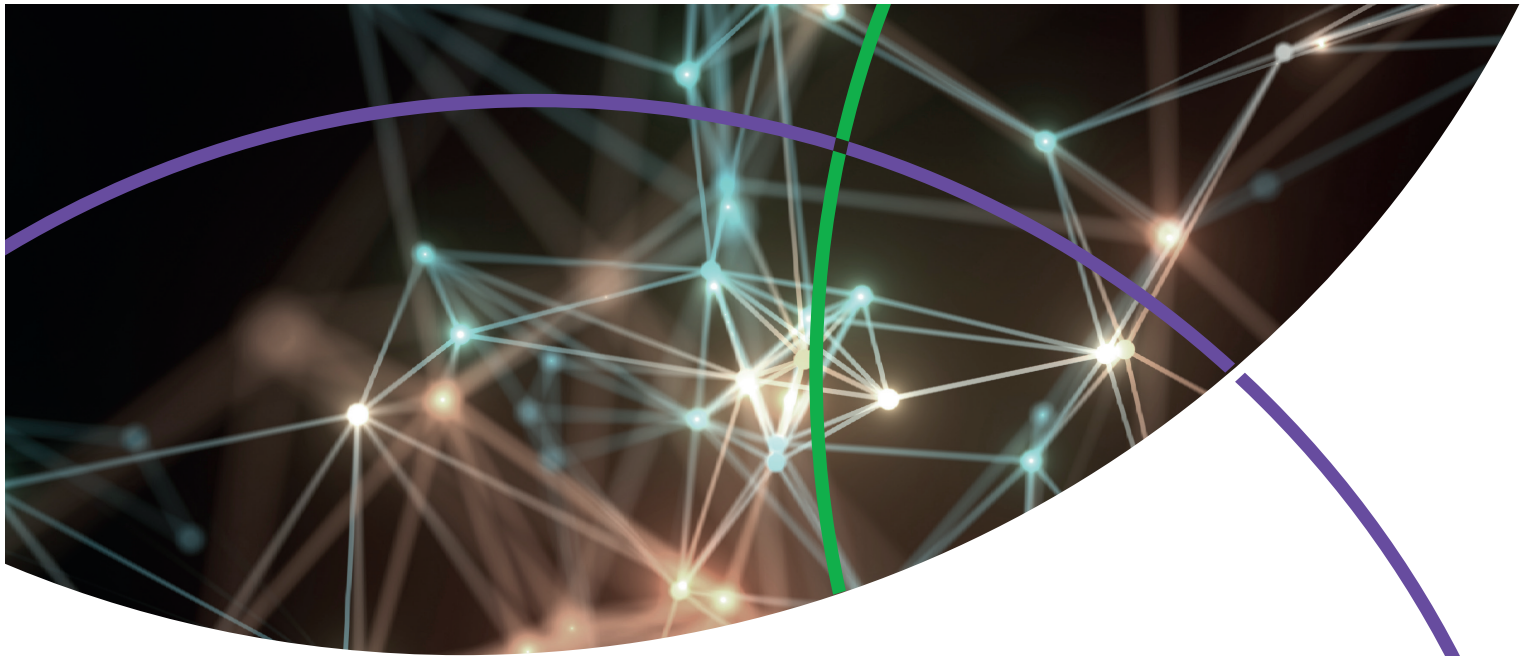




File Histories

The world's leading IP decision makers turn to us for one reason. Trust.

Good decisions require reliable intelligence. That's why more IP decision makers rely on us.

We empower companies to build and protect their valuable assets with services that span the full IP lifecycle. Our blend of global expertise, resources, and technology translates to results you can rely on with certainty. In any language, we're the name you can trust.

IP Services from Clarivate Analytics

Patent search and analytics

- Prior art search
- Patent watch
- Patent profiles

Patent licensing

- Patent-to-product mapping
- Standards mapping
- Licensing opportunity analysis
- Patent acquisition analysis
- Claims charting

Patent preparation and prosecution

- Patent drafting
- Prosecution services

IP analytics

- Technology landscaping
- Patent portfolio audit
- Competitive portfolio assessment

IP management

- Data validation services
- IP payments
- IP docketing
- IP management consulting
- Paralegal services
- Proofreading

Translation services and file histories

For more information, call us at +1-800-445-9760 or email fhservice@clarivate.com

Alexandria

+1 800 445 9760 (US)
+1 703 916 1500 (International)
filehistories.clarivate.com

IP 1702 300
07.2017
© 2017 Clarivate Analytics

clarivate.com



Petitioner Intel Corp., Ex. 1015
IPR2023-00783, Pg. 1

FILE HISTORY

US 5,608,684

PATENT: 5,608,684

INVENTORS: REASONER KELLY J
WILLIAMS ERIC E

TITLE: System and method for RAM power and data
backup utilizing a capacitor and ROM

APPLICATION NO: US1994322808A

FILED: 13 OCT 1994

ISSUED: 04 MAR 1997

COMPILED: 13 JUN 2022

365-258

08/322808

Class

Subclass

ISSUE CLASSIFICATION

UTILITY SERIAL NUMBER 08/322808

PATENT DATE MAR 04 1997

PATENT NUMBER

5608684

5608684

SERIAL NUMBER 08/322,808

FILING DATE 10/13/94

CLASS 365

SUBCLASS 228

GROUP ART UNIT 2511

EXAMINER

APPLICANTS

KELLY J. REASONER, FT. COLLINS, CO; ERIC E. WILLIAMS, FT. COLLINS, CO.

CONTINUING DATA***

VERIFIED None

OK

FOREIGN/PCT APPLICATIONS***

VERIFIED None

OK

FOREIGN FILING LICENSE GRANTED 11/20/94

Foreign priority claimed 35 USC 119 conditions met ☐ yes ☒ no

AS FILED

STATE OR COUNTRY CO

SHEETS DRWS. 4

TOTAL CLAIMS 13

INDEP. CLAIMS 3

FILING FEE RECEIVED \$730.00

ATTORNEY'S DOCKET NO. 10944581

Verified and Acknowledged OK

Examiner's Initials

ADDRESS

RECORDS MANAGER
LEGAL DEPARTMENT-2080
HEWLETT-PACKARD COMPANY
P/O, BOX 10301
PALO ALTO CA 94303-0890

Hewlett-Packard Company
IP Administration, M/S 2080

TITLE

SYSTEM AND METHOD FOR RAM POWER AND DATA BACKUP UTILIZING A CAPACITOR AND ROM

U.S. DEPT. of COMM.-Pat. & TM Office-PTO-436L (rev. 10-78)

PARTS OF APPLICATION FILED SEPARATELY

NOTICE OF ALLOWANCE/MAILED 6-21-96

ISSUE FEE
Amount Due \$1250.00
Date Paid MA 9/20/96

Label Area

Assistant Examiner

DO HYUN YOO
PRIMARY EXAMINER
GROUP 2500

Primary Examiner

PREPARED FOR ISSUE

CLAIMS ALLOWED
Total Claims 4
Print Claim 1

DRAWING
Sheets Drwg. 4
Figs. Drwg. 4
Print Fig. 1

ISSUE BATCH NUMBER B29

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code, Title 35, Sections 422, 424 and 428, or otherwise outside the U.S. Patent & Trademark Office

Form PTO-436A (Rev. 8/92)

Form 08322808
1439F RET 269341300-000001 RT ID: VI
M -A3-01-1-03-0033-1-02-08 0103267588
SKP:RF058974541-00002 CUST:RF058974541
5608684
Srv: 05/25 1:00pm EDT For: Richard
RECORDS MANAGEMENT
R

5,608,684

SYSTEM AND METHOD FOR RAM POWER AND DATA BACKUP
UTILIZING A CAPACITOR AND ROM

Transaction History

Date	Transaction Description
12-07-1994	Application Captured on Microfilm
02-09-1995	Case Docketed to Examiner in GAU
03-10-1995	Case Docketed to Examiner in GAU
03-27-1995	Restriction/Election Requirement
04-05-1995	Mail Restriction Requirement
05-05-1995	Response to Election / Restriction Filed
05-09-1995	Date Forwarded to Examiner
05-15-1995	Non-Final Rejection
05-24-1995	Mail Non-Final Rejection
08-14-1995	Response after Non-Final Action
08-22-1995	Date Forwarded to Examiner
10-20-1995	Non-Final Rejection
10-25-1995	Mail Non-Final Rejection
01-16-1996	Response after Non-Final Action
01-25-1996	Date Forwarded to Examiner
04-01-1996	Final Rejection
04-08-1996	Mail Final Rejection (PTOL - 326)
05-23-1996	Interview Summary Record
06-07-1996	Response after Final Action
06-13-1996	Date Forwarded to Examiner
06-21-1996	Mail Notice of Allowance
06-21-1996	Notice of Allowance Data Verification Completed
09-20-1996	Issue Fee Payment Verified
09-20-1996	Mailroom Date of Drawing(s)
09-30-1996	Drawing(s) Received at Publications
10-02-1996	Drawing(s) Matched to Application
10-07-1996	Drawing(s) Processing Completed
01-27-1997	Issue Notification Mailed
03-04-1997	Recordation of Patent Grant Mailed

08/322808

6/27/96 D93 AC
PATENT APPLICATION



APPROVED FOR LICENSE
NOV 0 1994

INITIALS _____

Date
Entered
or
Counted

CONTENTS

Date
Received
or
Mailed

DEC 12 1994

	1. Application	4 1 papers.	
8/13-27-95	2. Prior Art		10/13/94
5-9-95	3. Associate P/A		9/13/95
8/5-15-95	3. Restriction (30 days)		
8-22-95	4. Election		5-5-95
10-20-95	5. Re: (3)		5-24-95
1-25-96	6. Amndt A		8-14-95
8/4-1-96	7. Non-Final Re: (3)		10-25-95 ^{R2}
5-23-96	8. Amndt B		1-16-96
6/13/96	9. F. Re: (3)		1-8-96
6/21/96	10. PTOL-443 (Interview Summary Record)		5-23-96
10/2/96	11. Amndt A ^{R2}		6/7/96
	12. PTOL-37(=) / Examiner's Amendment D		6-21-96
	13. Formal Drawings 4 (shs) 121		9/20/96
	14. PTO Grant MAK 0 4 1997		
	15.		
	16.		
	17.		
	18.		
	19.		
	20.		
	21.		
	22.		
	23.		
	24.		
	25.		
	26.		
	27.		
	28.		
	29.		
	30.		
	31.		
	32.		

(FRONT)

Staple Issue Slip Here

POSITION		ID NO.	DATE
CLASSIFIER		21	11/1/94
EXAMINER		350	11/27/94
TYPIST		350	11/30
VERIFIER		314	11-30-94
CORPS CORR.			
SPEC. HAND			
FILE MAINT.			
DRAFTING			

INDEX OF CLAIMS

Claim		Date	
Final	Original		
1	1	11/1/94	
2	2	11/27/94	
3	3	11/30/94	
4	4	11/30/94	
5	5	11/30/94	
6	6	11/30/94	
7	7	11/30/94	
8	8	11/30/94	
9	9	11/30/94	
10	10	11/30/94	
11	11	11/30/94	
12	12	11/30/94	
13	13	11/30/94	
14	14	11/30/94	
15	15	11/30/94	
16	16	11/30/94	
17	17	11/30/94	
18	18	11/30/94	
19	19	11/30/94	
20	20	11/30/94	
21	21	11/30/94	
22	22	11/30/94	
23	23	11/30/94	
24	24	11/30/94	
25	25	11/30/94	
26	26	11/30/94	
27	27	11/30/94	
28	28	11/30/94	
29	29	11/30/94	
30	30	11/30/94	
31	31	11/30/94	
32	32	11/30/94	
33	33	11/30/94	
34	34	11/30/94	
35	35	11/30/94	
36	36	11/30/94	
37	37	11/30/94	
38	38	11/30/94	
39	39	11/30/94	
40	40	11/30/94	
41	41	11/30/94	
42	42	11/30/94	
43	43	11/30/94	
44	44	11/30/94	
45	45	11/30/94	
46	46	11/30/94	
47	47	11/30/94	
48	48	11/30/94	
49	49	11/30/94	
50	50	11/30/94	

SYMBOLS
✓ Rejected
= Allowed
- (Through numeral) Canceled
+ Restricted
N Non-elected
I Interference
A Appeal
O Objected

Claim		Date	
Final	Original		
51	51		
52	52		
53	53		
54	54		
55	55		
56	56		
57	57		
58	58		
59	59		
60	60		
61	61		
62	62		
63	63		
64	64		
65	65		
66	66		
67	67		
68	68		
69	69		
70	70		
71	71		
72	72		
73	73		
74	74		
75	75		
76	76		
77	77		
78	78		
79	79		
80	80		
81	81		
82	82		
83	83		
84	84		
85	85		
86	86		
87	87		
88	88		
89	89		
90	90		
91	91		
92	92		
93	93		
94	94		
95	95		
96	96		
97	97		
98	98		
99	99		
100	100		

(LEFT INSIDE)

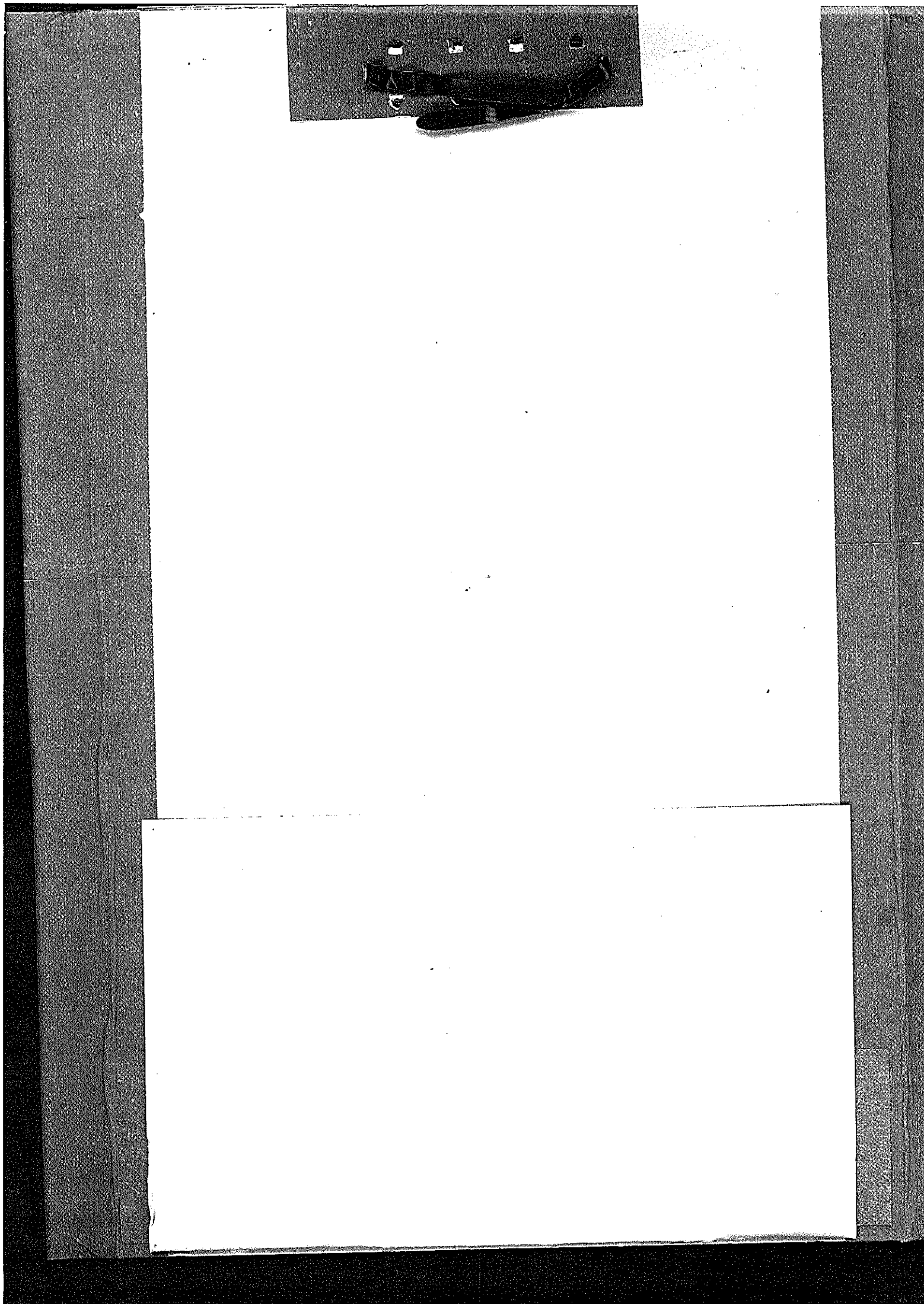
PATENT NUMBER	ORIGINAL CLASSIFICATION					
	CLASS 365			SUBCLASS 228		
APPLICATION SERIAL NUMBER 08/322808	CROSS REFERENCE(S)					
APPLICANT'S NAME (PLEASE PRINT) <i>Reasoner et al.</i>	CLASS 365	SUBCLASS (ONE SUBCLASS PER BLOCK)				
IF REISSUE, ORIGINAL PATENT NUMBER	149	154	226			
INTERNATIONAL CLASSIFICATION						
A I C	7/00					
	GROUP ART UNIT 2511	ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME) DO HYUN YOO PRIMARY EXAMINER				
		PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				
ISSUE CLASSIFICATION SLIP GROUP 2500						

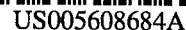
SEARCHED			
Class	Sub.	Date	Exmr.
365	226 102 149 222	5/12/95 ↓	DHT ↓
365 updated	228 228 104 above	10/18/95 ↓	DHT ↓
updated	above	3/27/96	DHT
updated	above	6/20/96	DHT

SEARCH NOTES		
	Date	Exmr.

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
385	102-154 228-128	6/24/46 ↓	D.H.P. ↓

Petitioner Intel Corp., Ex. 1015
IPR2023-00783, Pg. 8





[11] Patent Number: 5,608,684

[45] **Date of Patent:** Mar. 4, 1997

- ## OTHER PUBLICATIONS

- NEC Document No. CEP-1004G, "Supercap" User's Manual, published Jun. 1992.

- Primary Examiner*—Do Hyun Yoo

- [57]
- ABSTRACT**

- A system and method for permanently backing up RAM memory devices. The present invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The present invention also utilizes a ROM as a secondary backup device for backing up and restoring valid RAM data when the duration of power loss is greater than that for which the capacitor can supply backup power. Thus, the integrity of RAM data is guaranteed for all types of power fluctuations, interruptions, and failures. The ROM includes two storage areas for separately storing two copies of RAM data. The processor first determines whether the data stored in the RAM is valid. If the present RAM data is valid, the processor backs up the present RAM data by replacing the oldest or invalid copy in the ROM with the present RAM data. If the present RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM.

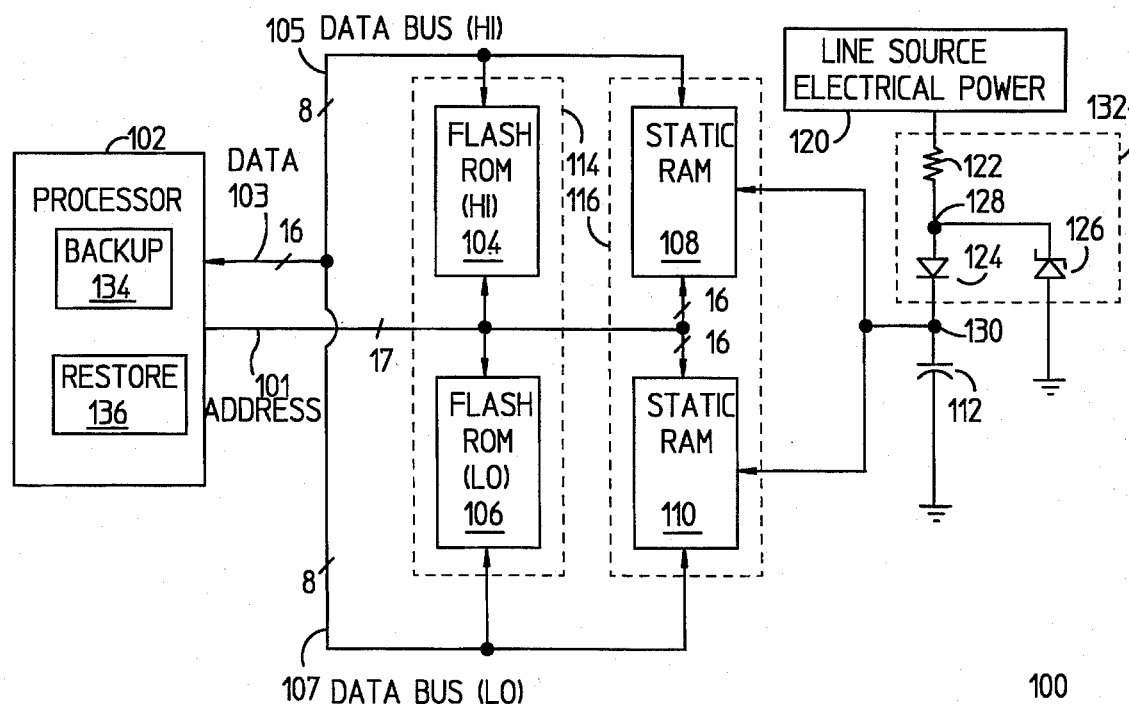
- ### 4 Claims, 4 Drawing Sheets

- [58] **Field of Search** 365/226, 102,
365/149, 222, 228, 154

- [56]
- References Cited**

U.S. PATENT DOCUMENTS

4,348,729	9/1982	Sasayama et al.	365/228	X
4,399,524	8/1983	Muguruma et al.	365/228	X
4,874,960	10/1989	Cybela	307/64	
5,175,842	12/1992	Totani	365/228	X
5,206,938	4/1993	Fujioka	365/228	X
5,243,577	9/1993	Ueda et al.	365/228	X
5,375,246	12/1994	Kimura et al.	365/226	X



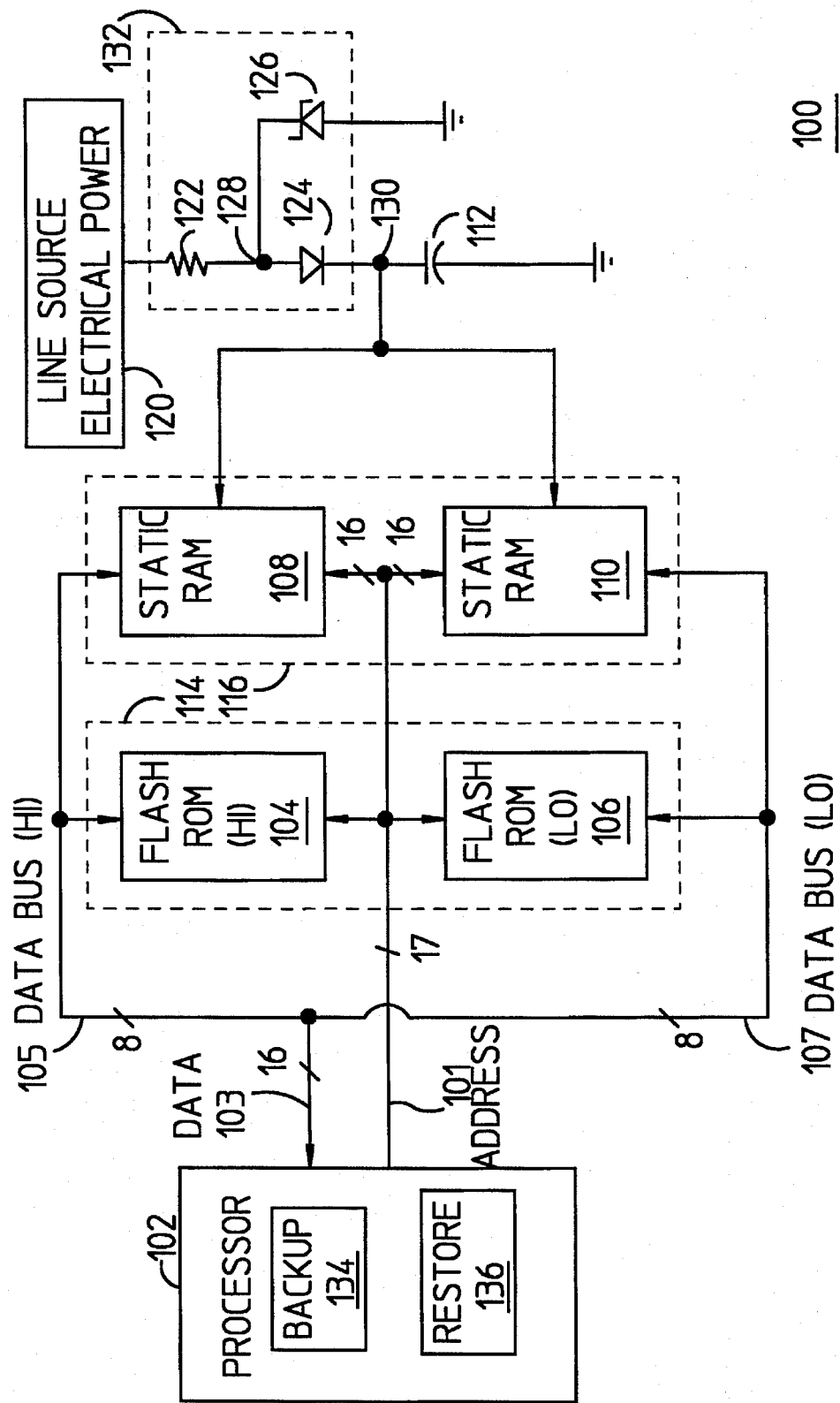


FIG 1

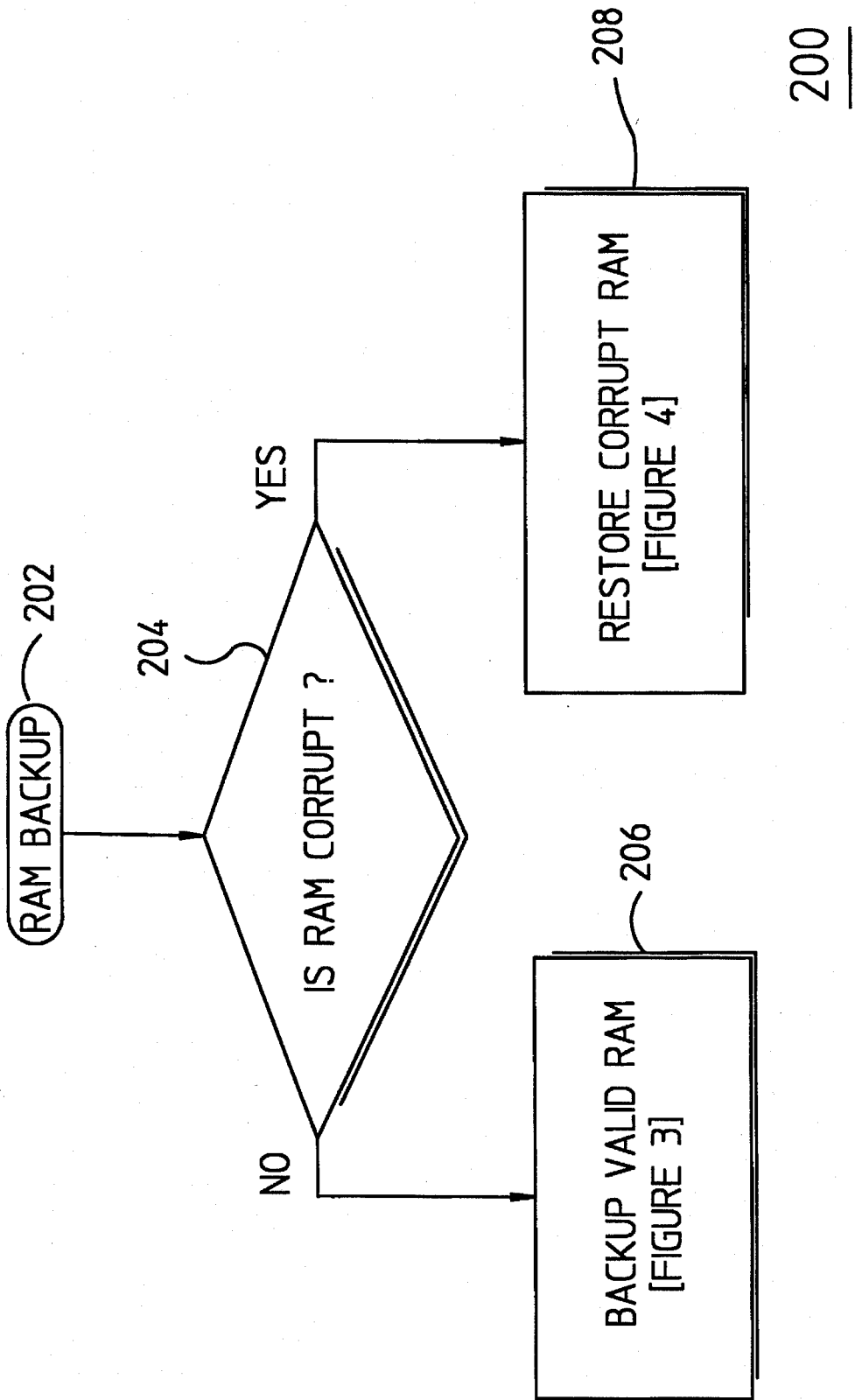


FIG 2

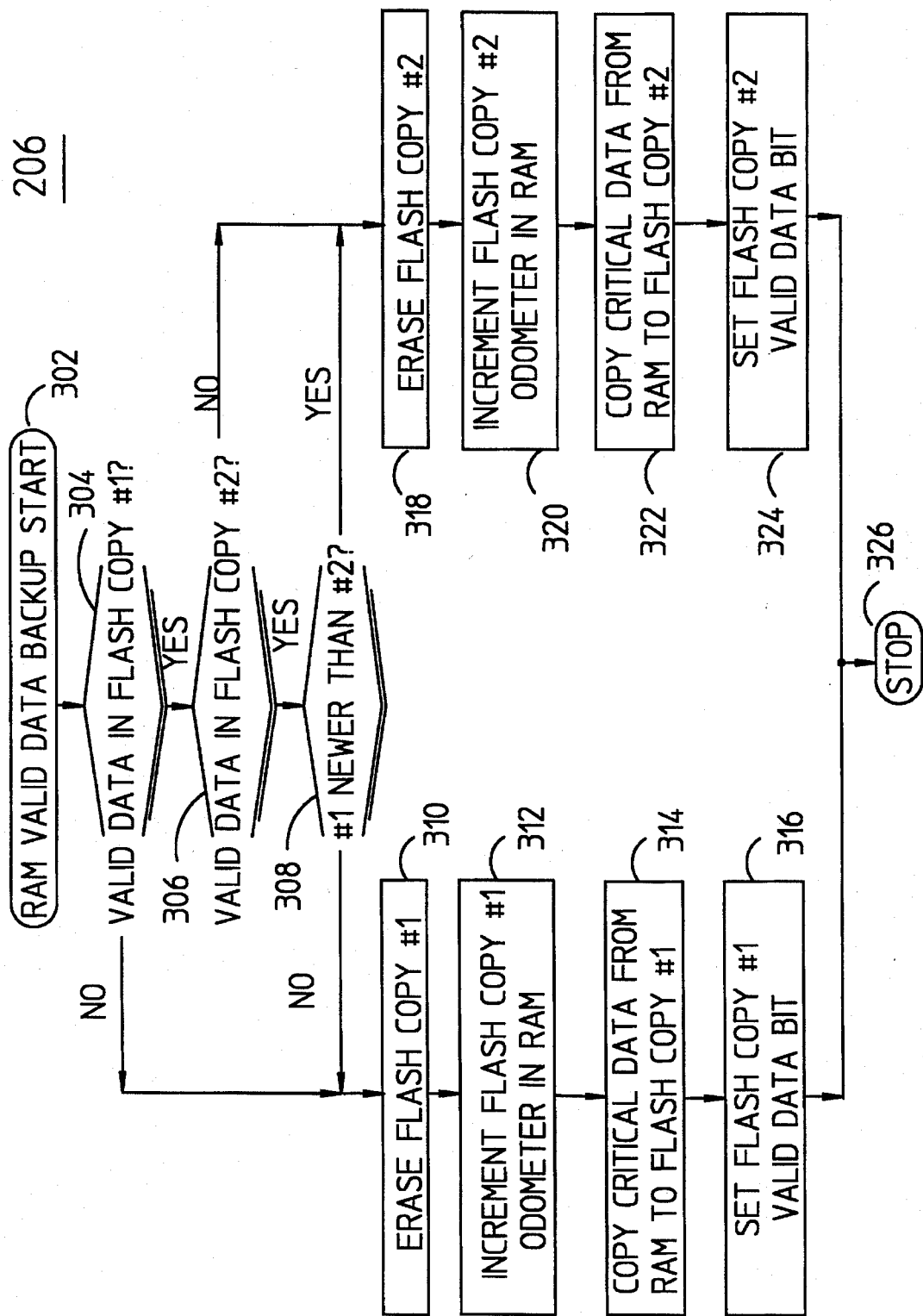


FIG 3

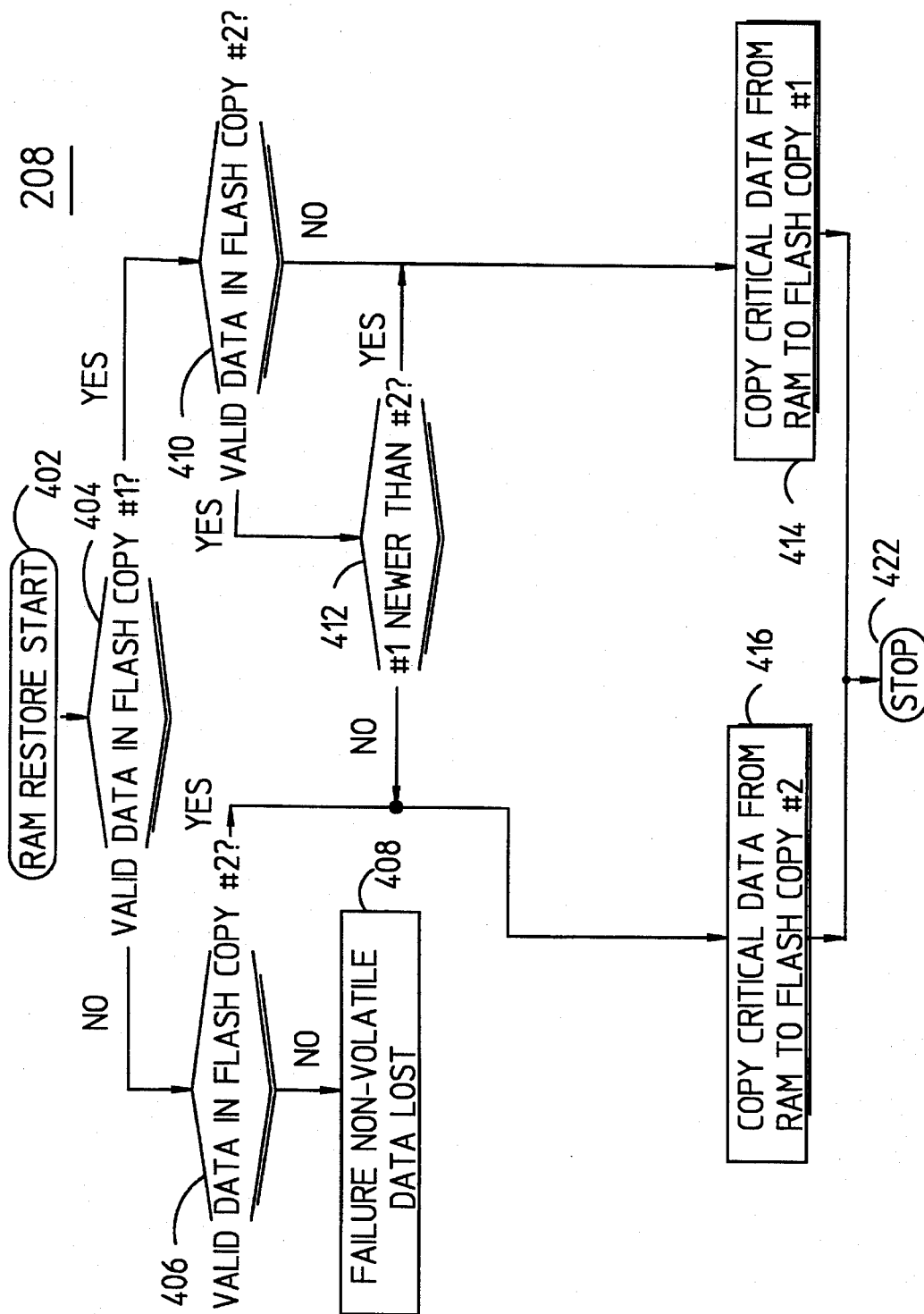


FIG 4

SYSTEM AND METHOD FOR RAM POWER AND DATA BACKUP UTILIZING A CAPACITOR AND ROM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to maintaining a supply of electrical power to electronic components normally furnished from a line supply of electrical power, and more particularly, to maintaining data stored in volatile memory components for which electrical power has been interrupted or lost.

2. Related Art

Volatile memory components such as a random access memory (RAM) must receive electrical power continuously to maintain the information stored in their memory cells. The bit content of the memory is typically lost whether electric power to the RAM is momentarily interrupted, fluctuates, or is lost.

There are many situations where backup power is required to maintain data in RAM. For example, service interruptions to the line source of power by natural phenomenon, operational problems in the power system, etc. These conditions generally result in a power interruption for a short period of time, perhaps one hour or less. Power backup is also required for momentary power fluctuations which may occur when, for example, heavy loads such as motors, buzzers, or displays are driven. Under such conditions, the backup power source is necessary to maintain a stable source of power. Other situations include providing backup power when the primary power source is turned off. Under these conditions, backup power may be required for an extended period of time, such as one month.

Recently, various approaches have been taken towards providing power backup capability to RAMs to achieve a nonvolatile memory, isolated from the above power interruptions and fluctuations. One of the more common backup power supply arrangements has been to combine a RAM with a dedicated backup battery. Some of these battery backup devices also include a circuit which senses power supply voltage. If this voltage drops below a predetermined battery voltage level, the circuit switches the RAM from receiving power from the line source of power to receiving power from the backup battery. These circuits generally allow current to be drawn from the battery only in the event of a loss of AC power.

There are a number of problems with the above approaches. First, the circuits normally exhibit a time delay before the backup battery is connected to the RAM. This time delay is a result of the turn-on time of the transistors in the circuit. While the delay time is relatively short, the RAM can be exposed to a low supply voltage condition before the battery is connected. This exposure to low supply voltage may cause a loss of data. Some systems have incorporated a capacitor to supply a temporary source of power to the RAM during the switching of power from line voltage to battery.

Another disadvantage of a battery backup power supply is that the charge remaining in nonrechargeable batteries to handle a power outage of unknown duration are difficult to determine. In addition, rechargeable batteries must have a controlled charge rate to limit current to the battery, and periodically requires replacement. This increases the maintenance cost of the system. In addition, the capacitor can supply the necessary voltage for only a limited period of

time. Thus, there may be a loss of data should the battery not be replaced at the proper time or is defective for a period longer than the discharge time of the capacitor.

Another disadvantage of battery backup systems relates to the environmental concerns of used battery disposal. Battery backup systems require the implementation of procedures for removing and discharging the battery prior to disposal. Although the use of a capacitor alone to provide backup power would alleviate this environmental problem, capacitors can supply power for only a relatively short period of time, making them ineffective as a long term backup power source.

What is needed, therefore, is a means for backing up volatile memory devices for long periods of time without incurring the problems associated with the use of batteries.

SUMMARY OF THE INVENTION

The present invention is system and method for indefinitely backing up RAM memory devices. The present invention utilizes a capacitor as the primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The present invention utilizes a ROM as a secondary backup device for backing up and replacing valid RAM data when the loss of line power supply is of a duration greater than that for which the capacitor can supply backup power. Thus, the present invention guarantees the integrity of RAM data for all types of primary power fluctuations, interruptions, and failures.

More specifically, the present invention includes a RAM configured to store binary data, a capacitor configured to provide the RAM with a voltage for a first period of time sufficient for the RAM to maintain the data stored in its memory cells, a ROM configured to store multiple backup copies of RAM data, and a processor for controlling the data transfers and copies stored in the RAM and ROM.

The processor first determines if the data presently stored in the RAM is valid. Typically, the RAM data is valid unless the line source power supply has been unavailable for a time which is greater than a discharge time of the capacitor. If the data stored in the RAM is valid, the processor backs up (copies) the RAM data to ROM. The ROM includes two storage areas for storing copies of RAM data. In the back up process of the present invention, the processor determines which of the copies of RAM data is the most recent and valid copy. The processor then replaces the older or invalid copy with the data presently stored in the RAM. If the RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM. This restoring process includes first determining which copy of RAM data stored in ROM is the most recent valid copy. Then the processor replaces the corrupted data stored in the RAM with the most recent valid copy of RAM data stored in ROM.

One advantage of the present invention is that it completely eliminates the use of a battery as a source of backup power to volatile RAM.

Another advantage of the present invention is that it uses a capacitor to provide relatively short term backup power. This enables the present invention to respond quickly to power interruptions. In addition, the capacitor protects against power fluctuations, thereby achieving greater circuit stability.

Another advantage of the present invention is that it utilizes an extremely high capacitance capacitor in conjunc-

tion with a ROM data backup system. The ROM provides long term data backup power for conditions in which the capacitor cannot maintain the necessary voltage output. The use of a high capacitance capacitor with a RAM enables the ROM to be used only in the rare circumstances wherein the power is removed from the system for long periods of time. This results in the ROM not being written to often, thereby preserving the ROM and enabling the present invention to guarantee RAM data indefinitely.

Further features and advantages of the present invention as well as the structure and operation of various embodiments of the present invention are described in detail below with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit of a reference number identifies the drawings in which the reference number first appears.

BRIEF DESCRIPTION OF THE FIGURES

The invention is best understood by reference to the Figures wherein references with like reference numbers indicate identical or functionally similar elements. In addition, the left-most digits refer to the figure in which the reference first appears in the accompanying drawings in which:

FIG. 1 is a circuit block diagram of a preferred embodiment of the RAM power and data backup system of the present invention;

FIG. 2 is a high level flowchart of the operation of the RAM data backup process of the present invention;

FIG. 3 is a flowchart of the portion of the RAM data backup process which copies valid RAM data to ROM; and

FIG. 4 is a flowchart of the portion of the RAM data backup process which copies previously stored RAM data from ROM back to RAM to replace data which has been found to be invalid.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

I. Introduction

The present invention is a system and method for permanently backing up RAM memory devices. The present invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and short-duration power failures. The present invention utilizes a ROM as a secondary backup device for backing up valid RAM data and replacing invalid RAM data. For instance, when the loss of line source power is for a time greater than that for which the capacitor can supply backup power, RAM data will be lost. Thus, the present invention guarantees the integrity of RAM data for all types of line source power fluctuations, interruptions, and failures.

II. System Architecture

FIG. 1 illustrates a circuit block diagram of a preferred embodiment of the memory backup system of the present invention. Referring now to FIG. 1, a memory backup system 100 of the present invention principally comprises a processor 102, a ROM 114, a RAM 116, a capacitor 112, and a power supply circuit 132. These components work in conjunction with each other to permanently maintain and backup data stored in RAM 116.

As will be discussed in detail below, ROM 114 consists of two separate ROM devices 104 and 106 to accommodate the multiple "flash copy" approach of the present invention. The two ROM devices 104 and 106 are addressed by processor 102 via address bus 101. Address bus 101 has 17 address lines, all of which are used to address ROM device 104 and ROM device 106. Processor 102 transfers data to and from ROM 114 over data bus 103. Data bus 103 has 16 data lines as illustrated in FIG. 1. The 16 data lines of data bus 103 are divided into 8 high order data lines, represented by high data bus 105, and 8 low order data lines, represented by low data bus 107. The 8 high order data lines are used to transfer data to and from ROM device 104. The 8 low order data lines are used to transfer data to and from ROM 106.

RAM 116 interfaces with processor 102 in a manner similar to ROM 114. RAM 116 consists of two separate RAM devices 108 and 110. However, as will be discussed in detail below, this division of RAM 116 is of little consequence in the present invention. In any event, the two RAM devices 108 and 110 are addressed via 16 of the 17 address lines of address bus 101. Processor 102 and RAM device 108 transfer data over high data bus 105. Processor 102 and RAM device 110 transfer data over low data bus 107.

RAM 116 receives power from a line power source 120 through power supply circuit 132. In the preferred embodiment of the present invention, RAM devices 108 and 110 are complimentary metal oxide silicon (CMOS) random access memory (RAM) components. These CMOS RAM components operate at 5 volts and retain stored information for extended periods of time at voltages down to 2 volts. Line power source 120 is a 12 volt source of power. Power supply circuit 132 receives the 12 volt line power, and converts that 12 volt power to 5 volts. Power supply 120 provides power to RAM 116 through resistor 122 and diode 124. A zener diode 126 is coupled to the power source side of diode 124. Zener diode 126 is employed as a voltage reference, maintaining a voltage of 5.6 volts at junction 128. Since the voltage drop across diode 124 is 0.6 volts, the voltage at junction 130 is maintained at 5 volts. Resistor 122, diode 124, and zener diode 126 are collectively and generally referred to as power supply circuit 132. The preferred embodiment of the present invention is implemented in a system having a 12 volt line voltage. Thus, power supply circuit 132 is directed towards reducing the 12 volt line voltage to the 5 volts required by CMOS RAM devices 108 and 110. However, as one skilled in the relevant art would find apparent, the configuration of power supply circuit 132 depends upon supply 120 and the power requirements of RAM 116, and may accordingly take on different configurations.

Coupled to power supply circuit 132 and RAM 116 at junction 130 is a capacitor 112. Capacitor 112 is charged by voltage source 120 through resistor 122 and diode 124. Capacitor 112 discharges when the voltage at junction 130 drops below 5 volts. Diode 124 prevents the charge stored in capacitor 112 from flowing to voltage source 120 when discharging to drive the remaining portions of the system (not shown). Thus, capacitor 112 supplies power only to RAM 116.

Further details regarding the system architecture and components are discussed with respect to the operation of the present invention. As introduced above, the present invention provides both power backup as well as data backup for RAM 116. Each of these processes and associated components are discussed below.

A. Power Backup Components

The components associated with the power backup feature of the present invention are now described in further

detail. These components include power supply circuit 132 and capacitor 112.

As described above, normal line power is supplied by line source power supply 120 through power supply circuit 132. In addition, power supply 120 simultaneously charges capacitor 112 while providing power to RAM 116. In the event of a loss or interruption of normal line power at line source 120, capacitor 112 will discharge to supply the necessary voltage to enable RAM 116 to maintain data stored in its memory cells.

As introduced above and discussed in detail below, the power backup feature of the present invention is utilized in conjunction with a ROM. However, the ROM components cannot be written too often (also discussed below). Thus, it is desired for capacitor 112 to have the capability to maintain the necessary voltage at junction 130 for RAM 116 to maintain the stored data for as long as possible.

In the preferred embodiment of the present invention, capacitor 112 is a 0.22F SUPERCAP, available from NEC Electronics, Inc., Mountain View, Calif., U.S.A. Due to its large capacity of 0.22F, capacitor 112 has a discharge time of a minimum of 10 days when supplying power to CMOS RAM 116. Thus, when there is a power interruption or failure for 10 or more days, capacitor 112 will supply the necessary power to preserve data in RAM 116, and ROM 114 will not have to be utilized. Further details regarding the NEC SUPERCAP capacitor 112 may be found in SUPERCAP User Manual, Document No. DEP-10046 (also available from NEC Electronics, Inc., Mountain View, Calif., U.S.A.), herein incorporated by reference in its entirety.

As introduced above, in the preferred embodiment of the present invention, capacitor 112 is a 0.22F SUPERCAP available from NEC. However, as one skilled in the relevant art would find apparent, any high capacitance capacitor may be used which is compatible with the anticipated duration of power interruptions which may occur. If the capacitance of capacitor 112 is too low, then ROM 114 will be utilized more often. Thus, if there are few long-term power interruptions, ROM 116 will still not be utilized often.

B. Data Backup Components

The system components directed to the backup and restoration of valid RAM data are now discussed. In particular, ROM 114 with ROM device 104 and ROM device 106 are provided to store copies of valid RAM data in the event that power is removed for a time greater than that for which capacitor 112 can supply backup power. The copying of RAM data and the transferring of data between processor 102 and RAM 116 and ROM 114 is performed by processor 102. More specifically, there are two functional components of processor 102 associated with the present invention: a backup subprocessor 134 and a restoration subprocessor 136. Backup subprocessor 134 backs up valid RAM data by copying it to ROM. A restoration subprocessor 136 restores RAM data which was previously backed up by backup subprocessor 134 to replace corrupted data stored in RAM 116.

As introduced above, ROM 114 is comprised of two ROM devices 104 and 106. Each of these are configured to store a copy of RAM data, referred to as a "flash copy." Thus, in the preferred embodiment, two copies of RAM data are maintained in ROM 114.

ROM 114, like all read-only memory components, is limited in the number of write cycles that it can support. This is typically on the order of a hundred thousand times. Thus, to extend the life of ROM 114, the present invention writes RAM data to ROM only at particular times and under certain conditions. Specifically, RAM data is copied to ROM 114 at

power up when the validity of the RAM data has been verified. One copy is the latest copy of RAM data as of the time that the system receives line power from line source power supply 120. The other copy is an older version of RAM data which is held for the unlikely event of a power interruption during the copying of data into ROM 114. Under such conditions, the more recent backup copy which was in the process of being copied to ROM 114 may have become corrupted or may be incomplete. The flash copy which is the older version of RAM data may then be used as a backup copy.

In the preferred embodiment of the present invention, flash ROM devices 104 and 106 are Intel 28F001BX-T/-B CMOS Flash Memory, available from Intel Corp., Santa Clara, Calif., U.S.A. CMOS flash ROM device 104 and CMOS flash ROM device 106 are nonvolatile flash memory comprised of four separately erasable blocks. In addition, each block is capable of being reprogrammed separately to ensure data integrity. The blocking scheme allows logical segmentation of the embedded software, with an 8 Kbyte block for boot code, a 112 Kbyte block and a 4 Kbyte block, combined to store the code associated with backup subprocessor 134 and restore subprocessor 136, and another 4 Kbyte block for storing critical data. In the preferred embodiment of the present invention, the critical data is parametric data, such as odometers, configurations, and identify bits. Thus, ROM 114 is capable of separately storing two copies of RAM data, one in CMOS flash ROM device 104 and one in CMOS flash ROM device 106. However, as one skilled in the relevant art would find apparent, other types of read only memory may be used which have the capability of separately storing multiple copies of RAM data.

ROM devices 104 and 106 also comprise a powerdown mode to lock out erase or write operations during system power up or power loss to provide absolute data protection. Thus, after an initial powerup or after return from a long-term powerdown situation, ROM devices 104 and 106 function as standard read only memories. In addition, the blocking scheme of ROM devices 104 and 106 allows updates in the main and parameter blocks while providing recovery code in a boot block in the unlikely event of a power failure during update. Further features of ROM 114 may be found in Intel product literature for Pat. No. 28F001BX-T/28F001BX-B 1M (128K X 8) CMOS FLASH MEMORY, order no. 290406-002, available from Intel Corporation, Santa Clara, Calif., U.S.A.

In the preferred embodiment of the present invention, processor 102 is 68000 series Motorola processor. However, as one skilled in the relevant art would find apparent, any other processor may be used which is configured to interface with ROM 114 and RAM 116 and which can perform the processing described below.

III. Data Backup Operation

FIGS. 2 through 4 are a flowchart of the RAM data backup and restoration process of the present invention. Referring to FIGS. 2-4, a preferred embodiment of the RAM data backup and restoration process is now discussed. The RAM data backup and restoration process 200 is invoked at start 202 when the system in which the present invention is implemented initially receives power.

First, in step 204, RAM 116 is verified to determine if it is corrupted. In the preferred embodiment of the present invention, this verification of the RAM data is accomplished by invoking a well known checksum operation. However, as one skilled in the relevant art would find apparent, other

memory verification procedures may be used, depending on the particular application. Typically, in the present invention, RAM 116 would only be corrupted when backup capacitor 112 has discharged to a point beyond which it can no longer supply the minimum voltage of +2 volts to RAM 116.

If RAM 116 is not corrupt, then the RAM data backup and restoration process 200 continues at block 206 wherein a RAM backup subprocess 206 is performed. RAM backup subprocess 206 copies the contents of RAM 116 into ROM 114. This process is illustrated in FIG. 3 and discussed in detail below. If RAM 116 is found to be corrupted in step 204, then processing continues at block 208 with a RAM restoration subprocess 208. RAM restoration subprocess 208 replaces this invalid data by restoring RAM 116 with valid data which has been previously stored in ROM 114. This process is illustrated in FIG. 4 and discussed in detail below.

A. Backup of Valid RAM

Referring to FIG. 3, the RAM backup subprocess 206 of the present invention is now discussed. As discussed above, in the preferred embodiment of the present invention, RAM 116 is comprised of two separate RAM devices 108 and 110. As discussed above, this separation of RAM 116 is inconsequential to the design of the present invention and was chosen due to the availability of components presently existing in the system in which the present invention is implemented. Thus, RAM 116 contains data, the integrity of which is to be guaranteed. This data is referred to as critical data, and is stored in both RAM device 108 and RAM device 110.

RAM backup subprocess 206 begins at start block 302, at which point RAM 116 has been verified as containing valid data which is to be copied to ROM 114.

As discussed above, in the preferred embodiment of the present invention, ROM 114 is comprised of two separate ROM devices 104 and 106, each of which stores a copy of the critical data. As will be discussed in detail below, the flash copy which is stored in one ROM device is not the same as the flash copy stored in the other ROM device. For ease of description, the copy of RAM data stored in ROM device 104 will be referred to as flash copy 1 and the copy of RAM data stored in ROM device 106 will be referred to as flash copy 2. As noted above, ROM 116 may be comprised of a single ROM device. In such a case, the ROM device must have separately controllable portions, one configured to store flash copy 1 and the other configured to store flash copy 2. Other configurations of ROM 114 are considered to be within the purview of one skilled in the relevant art.

One function of RAM backup subprocess 206 is to determine which flash copy to replace with the data stored in the RAM. Another function of RAM backup subprocess 206 is to copy the critical RAM data from RAM 116 to the ROM device containing the selected flash copy which is to be replaced. Also, the present invention updates the status of the selected flash copy to indicate the changed status of the data contained in the ROM component which stores that flash copy.

First, in step 304, flash copy 1, located on ROM device 104, is checked to determine if it contains valid data. This is performed by checking an associated validity bit stored in one of the parameter blocks of the associated ROM device 104. If flash copy 1 does not contain valid data, then data which is stored in RAM 116 may be stored in ROM device 104 in place of the invalid data presently stored as flash copy 1 in ROM device 104. Thus, in step 310, flash copy 1 is erased. The odometer associated with flash copy 1 is incre-

mented to indicate the processing point at which the RAM data is stored as flash copy 1. This is performed in step 312. After the data in flash copy 1 is erased and the odometer is incremented, the critical data stored in RAM 116 is copied to flash copy 1 in step 314. Finally, in step 316, a valid data bit associated with flash copy 1 is set to indicate that flash copy 1 now contains valid data.

If in step 304 it is determined that flash copy 1 contained valid data, then the above process of erasing flash copy 1 and replacing it with RAM data does not occur. Instead, processing continues at decision block 306, wherein a similar verification process is performed on flash copy 2.

If flash copy 2 does not contain valid data, then data which is stored in RAM 116 may be stored in place of flash copy 2. Thus, in step 318, flash copy 2 is erased. The odometer associated with flash copy 2 is incremented to indicate the processing point at which the RAM data is stored as flash copy 2. This is performed in step 320. After the data in flash copy 2 is erased and the odometer is incremented, the critical data stored in RAM 116 is copied to flash copy 2 in step 322. Finally, in step 324, a valid data bit associated with flash copy 2 is set to indicate that flash copy 2 now contains valid data.

If flash copy 1 and flash copy 2 both contain valid data, then the RAM data is copied to the flash copy containing the oldest version of data. Thus, since there are two separate flash ROMs to which RAM data may be copied, the RAM backup process 206 writes the copy of the critical data to the ROM device containing the oldest data.

In step 308 the backup subprocess 206 determines which flash copy contains the most recent version of RAM data. This step is performed by reading the associated odometers for each flash copy. If flash copy 2 is newer than flash copy 1, then flash copy 1 is erased and replaced with the critical data from RAM 116. This process was discussed above with reference to steps 310, 312, 314, and 316. Likewise, if flash copy 1 is newer than flash copy 2, then flash copy 2 is erased and replaced with the critical data from RAM 116. This process was discussed above with reference to steps 318, 320, 322, and 324.

Once the critical RAM data has been copied to ROM 114, the RAM backup subprocess 206 completes at block 326.

B. Restoration of Corrupted RAM

Referring to FIG. 4, the RAM restoration subprocess 208 is now discussed. RAM restoration subprocess 208 begins at start block 402, at which point RAM 116 has been verified as containing invalid data in step 204. Essentially, during RAM restoration subprocess 208 the latest valid flash copy stored in ROM 114 is copied to RAM 116 to replace corrupted data.

First, in step 404, the validity of the RAM data stored as flash copy 1 in ROM device 104 is verified. This is accomplished by reading an associated valid bit stored in a parameter block of ROM device 104. If flash copy 1 does not contain valid data, then that data cannot be used to replace the corrupted data presently stored in RAM 116. Thus, the validity of the RAM data stored as flash copy 2 is then verified in step 406. If flash copy 2 also does not contain valid RAM data, then there is no valid data available to replace the invalid RAM data. Processing continues at block 408 where a failure is indicated due to the loss of nonvolatile data.

If in step 404 restore subprocess 136 determines that flash copy 1 contains valid data, then processing continues at decision block 410 wherein the same verification process is performed on flash copy 2. If flash copy 2 does not contain valid data, then the critical RAM data stored as flash copy 1 in ROM device 104 is copied to RAM 116 in step 414.

If in step 404 restore subprocess 136 determines that flash copy 1 contains valid data and in step 410 restore subprocess 136 determines that flash copy 2 also contains valid data, then the most recent flash copy is selected to replace the corrupted data stored in RAM 116. Thus, in step 412, the odometer associated with flash copy 1 is compared with the odometer associated with flash copy 2 to determine which flash copy contains the oldest version of RAM data. If flash copy 1 is newer than flash copy 2, then processing proceeds to step 414 wherein the RAM data is copied to flash copy 1. Alternatively, if flash copy 2 is newer than flash copy 1, then processing proceeds to step 416 wherein RAM data is copied to flash copy 2. That is, restoration subprocess 206 of processor 102 copies the oldest flash copy of RAM data stored in ROM device 104 or 106 to RAM 116.

Thus, the present invention is capable of restoring the critical data stored in RAM 116 when it becomes corrupted. By maintaining two copies of the critical data in ROM 114, the present invention will restore the RAM with an older version of data which was backed up prior to the more recent version. Thus, the RAM will be restored to a known processing point from which the processing can be recovered.

Thus, the present invention maximizes the use of ROM 114 and capacitor 112 in their associated range of capabilities. Capacitor 112 is utilized often for "short term" (at least 10 days) power backup since it has the ability to be recharged repeatedly. ROM 114, on the other hand, is only utilized for the rare instances where "long term" data backup is required. In other words, there is a dual backup feature for maintaining valid RAM data; the first (capacitor) maintains the necessary RAM voltage to avoid the loss of data, and the second (ROM) restores the lost data when the capacitor fails to maintain the RAM voltage level.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that those of ordinary skill in the relevant art will recognize a variety of additional applications and appropriate modifica-

tions within the spirit of the invention and the scope of the claims.

What is claimed is:

1. A random access memory (RAM) backup system, comprising:

a RAM, configured to store binary data, including a supply voltage input adapted to receive a supply voltage thereon;

a capacitor, electrically coupled to said voltage input of said RAM, configured to provide said RAM with a voltage for a period of time, said voltage sufficient for said RAM to maintain said storage of said data;

a read only memory (ROM) having separate locations for concurrently storing multiple copies of said data stored in said RAM; and

processing means, coupled to said RAM and said ROM, for transferring said copies of said data between said RAM and said ROM.

2. The system of claim 1, wherein said ROM stores a first copy and a second copy of said data stored in said RAM, and further wherein said ROM enables said first copy of said data to be stored and erased separately from said second copy of said data.

3. The system of claim 2, further comprising: a power supply circuit, interposed between said RAM and a line power source having a line voltage, configured to convert and maintain said line voltage to said supply voltage.

4. The system of claim 3, wherein said processing means comprises:

a backup processing means for copying said first copy and said second copy of said data in said RAM to said ROM; and

a restore processing means for copying said first copy and said second copy of said data stored in said ROM to said RAM.

* * * * *

PATENT APPLICATION SERIAL NO. 08/322808

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

TW11066 10/26/94 08322808

08-2025 110 101

730.0000 1094458-1

PTO-1556
(5/87)



HEWLETT-PACKARD COMPANY
Legal Department, 2080
P.O. Box 10301
Palo Alto, California 94303-0890

00/322808
PATENT APPLICATION

ATTOR. DOCKET NO. 1094458-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is a(n): ☒ original patent application. ☒ Utility ☐ Design
☐ continuation-in-part application,
☐ continuation or divisional application under 37 CFR 1.53(b) of:

INVENTOR(S): Kelly J. Reasoner and Eric E. Williams

TITLE: System And Method For RAM Power And Data Backup
Utilizing A Capacitor And ROM

Enclosed are:

☒ The Declaration and Power of Attorney. ☒ signed ☐ unsigned or partially signed

☒ 4 sheets of ☐ formal drawings ☒ Informal drawings (one set)

☒ Information Disclosure Statement and Form PTO-1449 ☒ Associate Power of Attorney

☐ Priority document(s) ☐ (fee \$)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	13 — 20	0	X \$ 22	\$ 0
INDEPENDENT CLAIMS	3 — 3	0	X \$ 74	\$ 0
ANY MULTIPLE DEPENDENT CLAIMS			\$ 230	\$ 0
BASIC FEE: Design (\$290.00); Utility (\$710.00)				\$ 730.00
TOTAL FILING FEE				\$ 730.00
OTHER FEES				\$ 0
TOTAL CHARGES TO DEPOSIT ACCOUNT				\$ 730.00

Charge \$ 730.00 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Express Mail label no. TB65894828XUS

Date of Deposit 10/13/94

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

By Valerie A. Bakes

Typed Name: Valerie A. Bakes

By William W. Cochran II

Attorney/Agent for Applicant(s)
Reg. No. 26,652

Date: 10/13/94

Telephone No.: (303) 229-7239



78/322808

A

**System and Method For RAM Power And Data
Backup Utilizing A Capacitor And ROM**

**Inventors: Kelly J. Reasoner
Eric E. Williams**

5

Background of the Invention

Field of the Invention

10

The present invention relates generally to maintaining a supply of electrical power to electronic components normally furnished from a line supply of electrical power, and more particularly, to maintaining data stored in volatile memory components for which electrical power has been interrupted or lost.

Related Art

15

Volatile memory components such as a random access memory (RAM) must receive electrical power continuously to maintain the information stored in their memory cells. The bit content of the memory is typically lost whether electric power to the RAM is momentarily interrupted, fluctuates, or is lost.

20

There are many situations where backup power is required to maintain data in RAM. For example, service interruptions to the line source of power by natural phenomenon, operational problems in the power system, etc. These conditions generally result in a power interruption for a short period of time, perhaps one hour or less. Power backup is also required for momentary power fluctuations which may occur when, for example, heavy loads such as motors, buzzers, or displays are driven. Under such conditions, the backup power source is necessary to maintain a stable source of power. Other

25

situations include providing backup power when the primary power source is

turned off. Under these conditions, backup power may be required for an extended period of time, such as one month.

5 Recently, various approaches have been taken towards providing power backup capability to RAMs to achieve a nonvolatile memory, isolated from the above power interruptions and fluctuations. One of the more common backup power supply arrangements has been to combine a RAM with a dedicated backup battery. Some of these battery backup devices also include a circuit which senses power supply voltage. If this voltage drops below a predetermined battery voltage level, the circuit switches the RAM from
10 receiving power from the line source of power to receiving power from the backup battery. These circuits generally allow current to be drawn from the battery only in the event of a loss of AC power.

15 There are a number of problems with the above approaches. First, the circuits normally exhibit a time delay before the backup battery is connected to the RAM. This time delay is a result of the turn-on time of the transistors in the circuit. While the delay time is relatively short, the RAM can be exposed to a low supply voltage condition before the battery is connected. This exposure to low supply voltage may cause a loss of data. Some systems have incorporated a capacitor to supply a temporary source of power to the
20 RAM during the switching of power from line voltage to battery.

25 Another disadvantage of a battery backup power supply is that the charge remaining in nonrechargeable batteries to handle a power outage of unknown duration are difficult to determine. In addition, rechargeable batteries must have a controlled charge rate to limit current to the battery, and periodically requires replacement. This increases the maintenance cost of the system. In addition, the capacitor can supply the necessary voltage for ^{only} a limited period of time. Thus, there may be a loss of data should the battery

not be replaced at the proper time or is defective for a period longer than the discharge time of the capacitor.

Another disadvantage of battery backup systems relates to the environmental concerns of used battery disposal. Battery backup systems require the implementation of procedures for removing and discharging the battery prior to disposal. Although the use of ~~only~~ a capacitor ^{alone} to provide backup power would alleviate this environmental problem, capacitors can supply power for ^{only} a relatively short period of time, making them ineffective as a long term backup power source.

What is needed, therefore, is a means for backing up volatile memory devices for long periods of time without incurring the problems associated with the use of batteries.

Summary of the Invention

The present invention is system and method for indefinitely backing up RAM memory devices. The present invention utilizes a capacitor as the primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The present invention utilizes a ROM as a secondary backup device for backing up and replacing valid RAM data when the loss of line power supply is of a duration greater than that ^{for} which the capacitor can supply backup power. Thus, the present invention guarantees the integrity of RAM data for all types of primary power fluctuations, interruptions, and failures.

More specifically, the present invention includes a RAM configured to store binary data, a capacitor configured to provide the RAM with a voltage for a first period of time sufficient for the RAM to maintain the data stored in its memory cells, a ROM configured to store multiple backup copies of

RAM data, and a processor for controlling the data transfers and copies stored in the RAM and ROM.

5 The processor first determines if the data presently stored in the RAM is valid. Typically, the RAM data is valid unless the line source power supply has been unavailable for a time which is greater than a discharge time of the capacitor. If the data stored in the RAM is valid, the processor backs up (copies) the RAM data to ROM. The ROM includes two storage areas for storing copies of RAM data. In the back up process of the present invention, the processor determines which of the copies of RAM data is the most recent and valid copy. The processor then replaces the older or invalid copy with the data presently stored in the RAM. If the RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM. This restoring process includes first determining which copy of RAM data stored in ROM is the most recent valid copy. Then the processor replaces the corrupted data stored in the RAM with ^{the most recent valid copy of RAM} ~~a previously stored copy~~ of the data stored in ROM.

One advantage of the present invention is that it completely eliminates the use of a battery as a source of backup power to volatile RAM.

20 Another advantage of the present invention is that it uses a capacitor to provide relatively short term backup power. This enables the present invention to respond quickly to power interruptions. In addition, the capacitor protects against power fluctuations, thereby achieving greater circuit stability.

25 Another advantage of the present invention is that it utilizes an extremely high capacitance capacitor in conjunction with a ROM data backup system. The ROM provides long term data backup power for conditions in which the capacitor cannot maintain the necessary voltage output. The use of a high capacitance capacitor with a RAM enables the ROM to be used only in

the rare circumstances wherein the power is removed from the system for long periods of time. This results in the ROM not being written to often, thereby preserving the ROM and enabling the present invention to guarantee RAM data indefinitely.

5 Further features and advantages of the present invention as well as the structure and operation of various embodiments of the present invention are described in detail below with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit of a reference number identifies the
10 drawings in which the reference number first appears.

Brief Description of the Figures

The invention is best understood by reference to the Figures wherein references with like reference numbers indicate identical or functionally similar elements. In addition, the left-most digits refer to the figure in which the
15 reference first appears in the accompanying drawings in which:

Figure 1 is a circuit block diagram of a preferred embodiment of the RAM power and data backup system of the present invention;

Figure 2 is a high level flowchart of the operation of the RAM data backup process of the present invention;

20 Figure 3 is a flowchart of the portion of the RAM data backup process which copies valid RAM data to ROM; and

Figure 4 is a flowchart of the portion of the RAM data backup process which copies previously stored RAM data from ROM back to RAM to replace data which has been found to be invalid.

Detailed Description of the Preferred Embodiments

I. Introduction

5 The present invention is a system and method for permanently backing up RAM memory devices. The present invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and short-duration power failures. The present invention utilizes a ROM as a secondary backup device for backing up valid RAM data and replacing invalid RAM data. For instance, when the loss of line source power is for a time greater than that^{for} which the capacitor can supply backup power, RAM data will be lost. Thus, the present invention guarantees the integrity of RAM data for all types of line source power fluctuations, interruptions, and failures.

II. System Architecture

15 Figure 1 illustrates a circuit block diagram of a preferred embodiment of the memory backup system of the present invention. Referring now to Figure 1, a memory backup system 100 of the present invention principally comprises a processor 102, a ROM 114, a RAM 116, a capacitor 112, and a power supply circuit 132. These components work in conjunction with each other to permanently maintain and backup data stored in RAM 116.

20 As will be discussed in detail below, ROM 114 consists of two separate ROM devices 104 and 106 to accommodate the multiple "flash copy" approach of the present invention. The two ROM devices 104 and 106 are addressed by processor 102 via address bus 101. Address bus 101 has 17 address lines, all of which are used to address ROM device 104 and ROM device 106. Processor 102 transfers data to and from ROM 114 over data bus 103. Data bus 103 has 16 data lines as illustrated in Figure 1. The 16 data lines of data

bus 103 are divided into 8 high order data lines, represented by high data bus 105, and 8 low order data lines, represented by low data bus 107. The 8 high order data lines are used to transfer data to and from ROM device 104. The 8 low order data lines are used to transfer data to and from ROM 106.

5 RAM 116 interfaces with processor 102 in a manner similar to ROM 114. RAM 116 consists of two separate RAM devices 108 and 110. However, as will be discussed in detail below, this division of RAM 116 is of little consequence in the present invention. In any event, the two RAM devices 108 and 110 are addressed via 16 of the 17 address lines of address
10 bus 101. Processor 102 and RAM device 108 transfer data over high data bus 105. Processor 102 and RAM device 110 transfer data over low data bus 107.

 RAM 116 receives power from a line power source 120 through power supply circuit 132. In the preferred embodiment of the present invention, RAM devices 108 and 110 are complimentary metal oxide silicon (CMOS)
15 random access memory (RAM) components. These CMOS RAM components operate at 5 volts and retain stored information for extended periods of time at voltages down to 2 volts. Line power source 120 is a 12 volt source of power. Power supply circuit 132 receives the 12 volt line power, and converts that 12 volt power to 5 volts. Power supply 120 provides power to
20 RAM 116 through resistor 122 and diode 124. A zener diode 126 is coupled to the power source side of diode 124. Zener diode 126 is employed as a voltage reference, maintaining a voltage of 5.6 volts at junction 128. Since the voltage drop across diode 124 is 0.6 volts, the voltage at junction 130 is maintained at 5 volts. Resistor 122, diode 124, and zener diode 126 are
25 collectively and generally referred to as power supply circuit 132. The preferred embodiment of the present invention is implemented in a system having a 12 volt line voltage. Thus, power supply circuit 132 is directed towards reducing the 12 volt line voltage to the 5 volts required by CMOS RAM devices 108 and 110. However, as one skilled in the relevant art would

find apparent, the configuration of power supply circuit 132 depends upon supply 120 and the power requirements of RAM 116, and may accordingly take on different configurations.

5 Coupled to power supply circuit 132 and RAM 116 at junction 130 is a capacitor 112. Capacitor 112 is charged by voltage source 120 through resistor 122 and diode 124. Capacitor 112 discharges when the voltage at junction 130 drops below 5 volts. Diode 124 prevents the charge stored in capacitor 112 from flowing to voltage source 120 when discharging to drive the remaining portions of the system (not shown). Thus, capacitor 112
10 supplies power only to RAM 116.

Further details regarding the system architecture and components are discussed with respect to the operation of the present invention. As introduced above, the present invention provides both power backup as well as data backup for RAM 116. Each of these processes and associated components are
15 discussed below.

A. Power Backup Components

The components associated with the power backup feature of the present invention are now described in further detail. These components include power supply circuit 132 and capacitor 112.

20 As described above, normal line power is supplied by line source power supply 120 through power supply circuit 132. In addition, power supply 120 simultaneously charges capacitor 112 while providing power to RAM 116. In the event of a loss or interruption of normal line power at line source 120, capacitor 112 will discharge to supply the necessary voltage to
25 enable RAM 116 to maintain data stored in its memory cells.

As introduced above and discussed in detail below, the power backup feature of the present invention is utilized in conjunction with a ROM. However, the ROM components cannot be written too often (also discussed below). Thus, it is desired for capacitor 112 to have the capability to maintain the necessary voltage at junction 130 for RAM 116 to maintain the stored data for as long as possible.

In the preferred embodiment of the present invention, capacitor 112 is a .22F SUPERCAP, available from NEC Electronics, Inc., Mountain View, California, U.S.A. Due to its large capacity of .22F, capacitor 112 has a discharge time of a minimum of 10 days when supplying power to CMOS RAM 116. Thus, when there is a power interruption or failure for 10 or more days, capacitor 112 will supply the necessary power to preserve data in RAM 116, and ROM 114 will not have to be utilized. Further details regarding the NEC SUPERCAP capacitor 112 may be found in SUPERCAP User Manual, Document No. DEP-10046 (also available from NEC Electronics, Inc., Mountain View, California, U.S.A.), herein incorporated by reference in its entirety.

As introduced above, in the preferred embodiment of the present invention, capacitor 112 is a .22F SUPERCAP available from NEC. However, as one skilled in the relevant art would find apparent, any high capacitance capacitor may be used which is compatible with the anticipated duration of power interruptions which may occur. If the capacitance of capacitor 112 is too low, then ROM 114 will be utilized more often. Thus, if there are few long-term power interruptions, ROM 116 will still not be utilized often.

B. Data Backup Components

2 The system components directed to the backup and restoration of valid
RAM data^{are} is now discussed. In particular, ROM 114 with ROM device 104
and ROM device 106 are provided to store copies of valid RAM data in the
a 5 event that power is removed for a time greater than that^{for} which capacitor 112
can supply backup power. The copying of RAM data and the transferring of
data between processor 102 and RAM 116 and ROM 114 is performed by
processor 102. More specifically, there are two functional components of
processor 102 associated with the present invention: a backup subprocessor
10 134 and a restoration subprocessor 136. Backup subprocessor 134 backs up
valid RAM data by copying it to ROM. A restoration subprocessor 136
restores RAM data which was previously backed up by backup subprocessor
134 to replace corrupted data stored in RAM 116.

15 As introduced above, ROM 114 is comprised of two ROM devices 104
and 106. Each of these are configured to store a copy of RAM data, referred
to as a "flash copy." Thus, in the preferred embodiment, two copies of RAM
data are maintained in ROM 114.

20 ROM 114, like all read-only memory components, is limited in the
number of write cycles that it can support. This is typically on the order of
a hundred thousand times. Thus, to extend the life of ROM 114, the present
invention writes RAM data to ROM only at particular times and under certain
conditions. Specifically, RAM data is copied to ROM 114 at power up when
the validity of the RAM data has been verified. One copy is the latest copy
of RAM data as of the time that the system receives line power from line
25 source power supply 120. The other copy is an older version of RAM data
which is held for the unlikely event of a power interruption during the copying
of data into ROM 114. Under such conditions, the more recent backup copy
which was in the process of being copied to ROM 114 may have become

corrupted or may be incomplete. The flash copy which is the older version of RAM data may then be used as a backup copy.

In the preferred embodiment of the present invention, flash ROM devices 104 and 106 are Intel 28F001BX-T/-B CMOS Flash Memory, available from Intel Corp., Santa Clara, California, U.S.A. CMOS flash ROM device 104 and CMOS flash ROM device 106 are nonvolatile flash memory comprised of four separately erasable blocks. In addition, each block is capable of being reprogrammed separately to ensure data integrity. The blocking scheme allows logical segmentation of the embedded software, with an 8 Kbyte block for boot code, a 112 Kbyte block and a 4 Kbyte block, combined to store the code associated with backup subprocess 134 and restore subprocess 136, and another 4 Kbyte block for storing critical data. In the preferred embodiment of the present invention, the critical data is parametric data, such as odometers, configurations, and identify bits. Thus, ROM 114 is capable of separately storing two copies of RAM data, one in CMOS flash ROM device 104 and one in CMOS flash ROM device 106. However, as one skilled in the relevant art would find apparent, other types of read only memory may be used which have the capability of separately storing multiple copies of RAM data.

ROM devices 104 and 106 also comprise a powerdown mode to lock out erase or write operations during system power up or power loss to provide absolute data protection. Thus, after an initial powerup or after return from a long-term powerdown situation, ROM devices 104 and 106 function as standard read only memories. In addition, the blocking scheme of ROM devices 104 and 106 allows updates in the main and parameter blocks while providing recovery code in a boot block in the unlikely event of a power failure during update. Further features of ROM 114 may be found in Intel product literature for Pat. No. 28F001BX-T/28F001BX-B 1M (128K X 8)

CMOS FLASH MEMORY, order no. 290406-002, available from Intel Corporation, Santa Clara, California, U.S.A.

In the preferred embodiment of the present invention, processor 102 is 68000 series Motorola processor. However, as one skilled in the relevant art would find apparent, any other processor may be used which is configured to interface with ROM 114 and RAM 116 and which can perform the processing described below.

III. Data Backup Operation

Figures 2 through 4 are a flowchart of the RAM data backup and restoration process of the present invention. Referring to Figures 2-4, a preferred embodiment of the RAM data backup and restoration process is now discussed. The RAM data backup and restoration process 200 is invoked at start 202 when the system in which the present invention is implemented initially receives power.

First, in step 204, RAM 116 is verified to determine if it is corrupted. In the preferred embodiment of the present invention, this verification of the RAM data is accomplished by invoking a well known checksum operation. However, as one skilled in the relevant art would find apparent, other memory verification procedures may be used, depending on the particular application. Typically, in the present invention, RAM 116 would only be corrupted when backup capacitor 112 has discharged to a point beyond which it can no longer supply the minimum voltage of +2 volts to RAM 116.

If RAM 116 is not corrupt, then the RAM data backup and restoration process 200 continues at block 206 wherein a RAM backup subprocess 206 is performed. RAM backup subprocess 206 copies the contents of RAM 116 into ROM 114. This process is illustrated in Figure 3 and discussed in detail

below. If RAM 116 is found to be corrupted in step 204, then processing continues at block 208 with a RAM restoration subprocess 208. RAM restoration subprocess 208 replaces this invalid data by restoring RAM 116 with valid data which has been previously stored in ROM 114. This process is illustrated in Figure 4 and discussed in detail below.

A. Backup of Valid RAM

Referring to Figure 3, the RAM backup subprocess 206 of the present invention is now discussed. As discussed above, in the preferred embodiment of the present invention, RAM 116 is comprised of two separate RAM devices 108 and 110. As discussed above, this separation of RAM 116 is inconsequential to the design of the present invention and was chosen due to the availability of components presently existing in the system in which the present invention is implemented. Thus, RAM 116 contains data, the integrity of which is to be guaranteed. This data is referred to as critical data, and is stored in both RAM device 108 and RAM device 110.

RAM backup subprocess 206 begins at start block 302, at which point RAM 116 has been verified as containing valid data which is to be copied to ROM 114.

As discussed above, in the preferred embodiment of the present invention, ROM 114 is comprised of two separate ROM devices 104 and 106, each of which stores a copy of the critical data. As will be discussed in detail below, the flash copy which is stored in one ROM device is not the same as the flash copy stored in the other ROM device. For ease of description, the copy of RAM data stored in ROM device 104 will be referred to as flash copy 1 and the copy of RAM data stored in ROM device 106 will be referred to as flash copy 2. As noted above, ROM 116 may be comprised of a single ROM device. In such a case, the ROM device must have separately controllable

portions, one configured to store flash copy 1 and the other configured to store flash copy 2. Other configurations of ROM 114 are considered to be within the purview of one skilled in the relevant art.

One function of RAM backup subprocess 206 is to determine which flash copy to replace with the data stored in the RAM. Another function of RAM backup subprocess 206 is to copy the critical RAM data from RAM 116 to the ROM device containing the selected flash copy which is to be replaced. Also, the present invention updates the status of the selected flash copy to indicate the changed status of the data contained in the ROM component which stores that flash copy.

First, in step 304, flash copy 1, located on ROM device 104, is checked to determine if it contains valid data. This is performed by checking an associated validity bit stored in one of the parameter blocks of the associated ROM device 104. If flash copy 1 does not contain valid data, then data which is stored in RAM 116 may be stored in ROM device 104 in place of the invalid data presently stored as flash copy 1 in ROM device 104. Thus, in step 310, flash copy 1 is erased. The odometer associated with flash copy 1 is incremented to indicate the processing point at which the RAM data is stored as flash copy 1. This is performed in step 312. After the data in flash copy 1 is erased and the odometer is incremented, the critical data stored in RAM 116 is copied to flash copy 1 in step 314. Finally, in step 316, a valid data bit associated with flash copy 1 is set to indicate that flash copy 1 now contains valid data.

If in step 304 it is determined that flash copy 1 contained valid data, then the above process of erasing flash copy 1 and replacing it with RAM data does not occur. Instead, processing continues at decision block 306, wherein a similar verification process is performed on flash copy 2.

If flash copy 2 does not contain valid data, then data which is stored in RAM 116 may be stored in place of flash copy 2. Thus, in step 318, flash copy 2 is erased. The odometer associated with flash copy 2 is incremented to indicate the processing point at which the RAM data is stored as flash copy 2. This is performed in step 320. After the data in flash copy 2 is erased and the odometer is incremented, the critical data stored in RAM 116 is copied to flash copy 2 in step 322. Finally, in step 324, a valid data bit associated with flash copy 2 is set to indicate that flash copy 2 now contains valid data.

If flash copy 1 and flash copy 2 both contain valid data, then the RAM data is copied to the flash copy containing the oldest version of data. Thus, since there are two separate flash ROMs to which RAM data may be copied, the RAM backup process 206 writes the copy of the critical data to the ROM device containing the oldest data.

In step 308 the backup subprocess 206 determines which flash copy contains the most recent version of RAM data. This step is performed by reading the associated odometers for each flash copy. If flash copy 2 is newer than flash copy 1, then flash copy 1 is erased and replaced with the critical data from RAM 116. This process was discussed above with reference to steps 310, 312, 314, and 316. Likewise, if flash copy 1 is newer than flash copy 2, then flash copy 2 is erased and replaced with the critical data from RAM 116. This process was discussed above with reference to steps 318, 320, 322, and 324.

Once the critical RAM data has been copied to ROM 114, the RAM backup subprocess 206 completes at block 326.

B. Restoration of Corrupted RAM

Referring to Figure 4, the RAM restoration subprocess 208 is now discussed. RAM restoration subprocess 208 begins at start block 402, at which point RAM 116 has been verified as containing invalid data in step 204. Essentially, during RAM restoration subprocess 208 the latest valid flash copy stored in ROM 114 is copied to RAM 116 to replace corrupted data.

First, in step 404, the validity of the RAM data stored as flash copy 1 in ROM device 104 is verified. This is accomplished by reading an associated valid bit stored in a parameter block of ROM device 104. If flash copy 1 does not contain valid data, then that data cannot be used to replace the corrupted data presently stored in RAM 116. Thus, the validity of the RAM data stored as flash copy 2 is then verified in step 406. If flash copy 2 also does not contain valid RAM data, then there is no valid data available to replace the invalid RAM data. Processing continues at block 408 where a failure is indicated due to the loss of nonvolatile data.

If in step 404 restore subprocess 136 determines that flash copy 1 contains valid data, then processing continues at decision block 410 wherein the same verification process is performed on flash copy 2. If flash copy 2 does not contain valid data, then the critical RAM data stored as flash copy 1 in ROM device 104 is copied to RAM 116 in step 414.

If in step 404 restore subprocess 136 determines that flash copy 1 contains valid data and in step 410 restore subprocess 136 determines that flash copy 2 also contains valid data, then the most recent flash copy is selected to replace the corrupted data stored in RAM 116. Thus, in step 412, the odometer associated with flash copy 1 is compared with the odometer associated with flash copy 2 to determine which flash copy contains the oldest version of RAM data. If flash copy 1 is newer than flash copy 2, then

processing proceeds to step 414 wherein the RAM data is copied to flash copy 1. Alternatively, if flash copy 2 is newer than flash copy 1, then processing proceeds to step 416 wherein RAM data is copied to flash copy 2. That is, restoration subprocess 206 of processor 102 copies the oldest flash copy of RAM data stored in ROM device 104 or 106 to RAM 116.

Thus, the present invention is capable of restoring the critical data stored in RAM 116 when it becomes corrupted. By maintaining two copies of the critical data in ROM 114, the present invention will restore the RAM with an older version of data which was ^{backed} ~~backup~~ up prior to the more recent version. Thus, the RAM will be restored to a known processing point from which the processing can be recovered.

Thus, the present invention maximizes the use of ROM 114 and capacitor 112 in their associated range of capabilities. Capacitor 112 is utilized often for "short term" (at least 10 days) power backup since it has the ability to be recharged repeatedly. ROM 114, on the other hand, is only utilized for the rare instances where "long term" data backup is required. In other words, there is a dual backup feature for maintaining valid RAM data; the first (capacitor) maintains the necessary RAM voltage to avoid the loss of data, and the second (ROM) restores the lost data when the capacitor fails to maintain the RAM voltage level.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that those of ordinary skill in the relevant art will recognize a variety of additional applications and appropriate modifications within the spirit of the invention and the scope of the claims.

What Is Claimed Is:

1. A random access memory (RAM) backup system, comprising:
a RAM, configured to store binary data, including a voltage input adapted to receive a ^{supply} voltage thereon;
a capacitor, electrically coupled to said voltage input of said RAM, configured to provide said RAM with a voltage for a first period of time, said voltage sufficient for said RAM to maintain said storage of said data;
a read only memory (ROM) configured to store multiple copies of said data stored in said RAM; and
processing means, coupled to said RAM and said ROM, for transferring said ^{copies} copy of said data stored in said RAM to said ROM.

2. The system of claim 1, wherein said ROM ^{stores} is configured to store a first copy and a second copy of said data stored in said RAM, and further wherein said ROM ^{enables} is configured to enable said first copy of said data to be ^{stored} store and erased separately from said second copy of said data.

3. The system of claim 2, further comprising:
a power supply circuit, interposed between a line power source and said RAM, configured to convert and maintain said line voltage to a specified supply voltage associated with said RAM.

4. The system of claim 3, wherein said ^{processing} processor means comprises:

a backup processing means for copying said first copy and said second copy of said data in said RAM to said ROM; and

a restore processing means for restoring ^{the} ~~a most valid and~~ ^{valid copy} most recent ^{copies} of said first and second copy of said data stored in said ROM to said RAM.

1 5. A method for backing up data presently stored in a RAM,
2 comprising the steps of:

- 3 (1) determining if said present RAM data is valid;
4 (2) backing up said present RAM data to a ROM when said present
5 RAM data is valid; and
6 (3) restoring the contents of said RAM with valid RAM data
7 previously stored in said ROM when said present RAM data is invalid.

1 6. The method of claim 5, wherein said ROM comprises a first
2 storage region configured to store a first flash copy of RAM data and a second
3 storage region configured to store a second flash copy of RAM data, and
4 further wherein said step (2) comprises the steps of:

- 5 (a) determining which of said first flash copy and said second flash
6 copy is a most recent valid copy of said RAM data and an invalid copy of said
7 RAM data; and
8 (b) replacing said invalid copy of said RAM data with said present
9 RAM data.

1 7. The method of claim 6, wherein said step (2)(a) comprises the
2 steps of:

- 3 (i) verifying the validity of said first flash copy stored in said first
4 storage area of said ROM;
5 (ii) after said step (i), verifying the validity of said second flash
6 copy stored in said second storage area of said ROM if said first flash copy
7 is valid; and
8 (iii) determining which of said first flash copy and said second flash
9 copy is said most recent copy of said RAM data.

1 8. The method of claim 7, wherein said step (2)(b) comprises the
2 steps of:

3 (i) erasing said first flash copy of said RAM data if said first flash
4 copy is invalid; and

5 (ii) after said step (2)(i), copying said present RAM data to said
6 first storage area of said ROM.

1 9. The method of claim 7, wherein said step (2)(b) comprises the
2 steps of:

3 (i) erasing said second flash copy of said RAM data if said second
4 flash copy is invalid; and

5 (ii) after said step (2)(i), copying said present RAM data to said
6 second storage area of said ROM.

1 10. The method of claim 8, wherein said step (2)(b) further
2 comprises the steps of:

3 (iii) incrementing an odometer associated with said first storage area
4 of said ROM to indicate said first flash copy contains said present RAM data;
5 and

6 (iv) setting a validity bit associated with said first storage area of
7 said ROM to indicate said present RAM data stored in said first flash copy is
8 valid.

1 11. The method of claim 9, wherein said step (2)(b) further
2 comprises the steps of:

3 (iii) incrementing an odometer associated with said second storage
4 area of said ROM to indicate said second flash copy contains said present
5 RAM data; and

6 (iv) setting a validity bit associated with said second storage area of
7 said ROM to indicate said present RAM data stored in said second flash copy
8 is valid.

12. The method of claim 5, wherein said ROM comprises a first storage region configured to store a first flash copy of RAM data and a second storage region configured to store a second flash copy of RAM data, and further wherein said step (3) comprises the steps of:

(a) determining whether said first flash copy and said second flash copy is a most recent valid copy of said RAM data;

(b) replacing said present RAM data with said most recent valid copy of said RAM data stored in said ROM; and

(c) indicating said RAM data cannot be restored if said first flash copy and said second flash copy are not valid.

13. A power and data backup method for providing backup power and data presently stored in a RAM having a voltage input adapted to receive a voltage thereon, utilizing a ROM having a first storage region configured to store a first flash copy of RAM data and a second storage region configured to store a second flash copy of RAM data, comprising the steps of:

(1) providing a voltage from a capacitor to said voltage input of said RAM when a normal power source is interrupted for a first time duration;

(2) determining if said present RAM data is valid, said RAM data being invalid when said first time duration is greater than a discharge time of said capacitor;

(3) backing up said present RAM data to a ROM when said present RAM data is valid, including the steps of:

(a) determining which of said first flash copy and said second flash copy is a most recent valid copy of said RAM data and an invalid copy of said RAM data, and

(b) replacing said invalid copy of said RAM data with said present RAM data; and

(4) restoring the contents of said RAM with valid RAM data previously stored in said ROM when said present RAM data is invalid, including the steps of:

- 21 (a) determining whether said first flash copy and said
22 second flash copy is a most recent valid copy of said RAM data,
23 (b) replacing said present RAM data with said most recent
24 valid copy of said RAM data stored in said ROM, and
25 (c) indicating said RAM data cannot be restored if said first
26 flash copy and said second flash copy are not valid.
-

08/322808

**System and Method For RAM Power And Data
Backup Utilizing A Capacitor And ROM**

Abstract

5
10
15
A system and method for permanently backing up RAM memory devices. The present invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The present invention also utilizes a ROM as a secondary backup device for backing up and restoring valid RAM data when the duration of power loss is greater than that which the capacitor can supply backup power. Thus, the integrity of RAM data is guaranteed for all types of power fluctuations, interruptions, and failures. The ROM includes two storage areas for separately storing two copies of RAM data. The processor first determines whether the data stored in the RAM is valid. If the present RAM data is valid, the processor backs up the present RAM data by replacing the oldest or invalid copy in the ROM with the present RAM data. If the present RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM.

A287-02.WP5

092794

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION	ATTORNEY DOCKET NO. 1094458
---	-----------------------------

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

System And Method For RAM Power And Data Backup
Utilizing A Capacitor and ROM
the specification of which

☒ is attached hereto. (Leave blank in response to Notice of Missing Parts)
☐ was filed on _____ as Application Serial No. _____
☐ was amended by the preliminary amendment filed with the original application papers.

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above and that I have disclosed the best mode for carrying out the invention as of the effective filing date of this application. I acknowledge the duty to disclose all information which is material to the examination of this application in accordance with Title 37, CFR 1.56. If this is a continuation-in-part application, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior (priority) application and the National or PCT international filing date of this continuation-in-part application.

☒ In compliance with this duty there is attached an Information Disclosure Statement (37 CFR 1.97).

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: _____ NO: _____
			YES: _____ NO: _____
			YES: _____ NO: _____

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the attorney(s) and/or agent(s) listed below to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Jeffrey B. Fromm, Reg. 30,558; Edward L. Miller, Reg. 29,331; William W. Cochran, II, Reg. 26,652; Guy J. Kelley, Reg. 32,905; Karl E. Bring, Reg. 31,591; Augustus W. Winfield, Reg. 34,046.

Send Correspondence to: Records Manager Legal Department, 2080 HEWLETT-PACKARD COMPANY P.O. Box 10301 Palo Alto, California 94303-0890	Direct Telephone Calls To: William W. Cochran, II, Esq. (303) 229-7239
---	--

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Kelly J. Reasoner 1-00 Citizenship: U.S.A.

Residence/Post Office Address: 2442 Yorkshire Street
Ft. Collins, Colorado 80526

Inventor's Signature

Date

Rev 4/92 (Form 3.02)

(Use Page Two For Additional Inventor(s) Signature(s))

Page 1 of 2

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 1094458

Full Name of #2 Joint Inventor: Eric E. Williams 2-00 Citizenship: U.S.A.

Residence/Post Office Address: 6361 Buchanan Street
Ft. Collins, Colorado 80525

Inventor's Signature Eric E. Williams Date 10/5/94

Full Name of # 1 Joint Inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

Inventor's Signature _____ Date _____

Full Name of # 2 Joint Inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

Inventor's Signature _____ Date _____

Full Name of # 3 Joint Inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

Inventor's Signature _____ Date _____

Full Name of # 4 Joint Inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

Inventor's Signature _____ Date _____

Full Name of # 5 Joint Inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

Inventor's Signature _____ Date _____

Full Name of # 6 Joint Inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

Inventor's Signature _____ Date _____

(Use Next Page For Additional Inventor(s) Signature(s))

43-395 NO RECYCLED WASTE 2 SQUARE
43-396 ELECTRONICALLY RECYCLED
43-398 100% RECYCLED WHITE SQUARE
MADE IN U.S.A.

08/322808

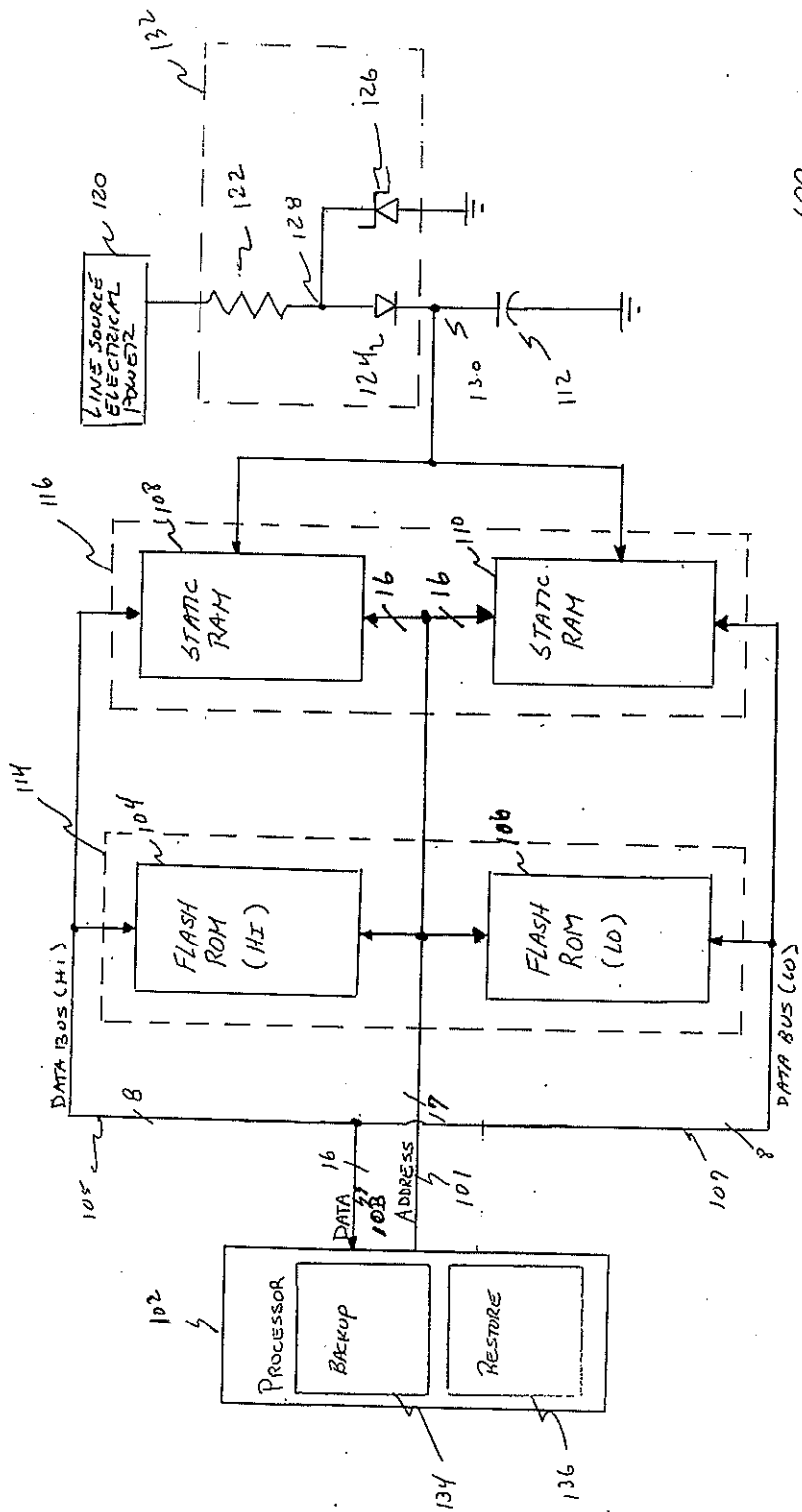


Figure 1

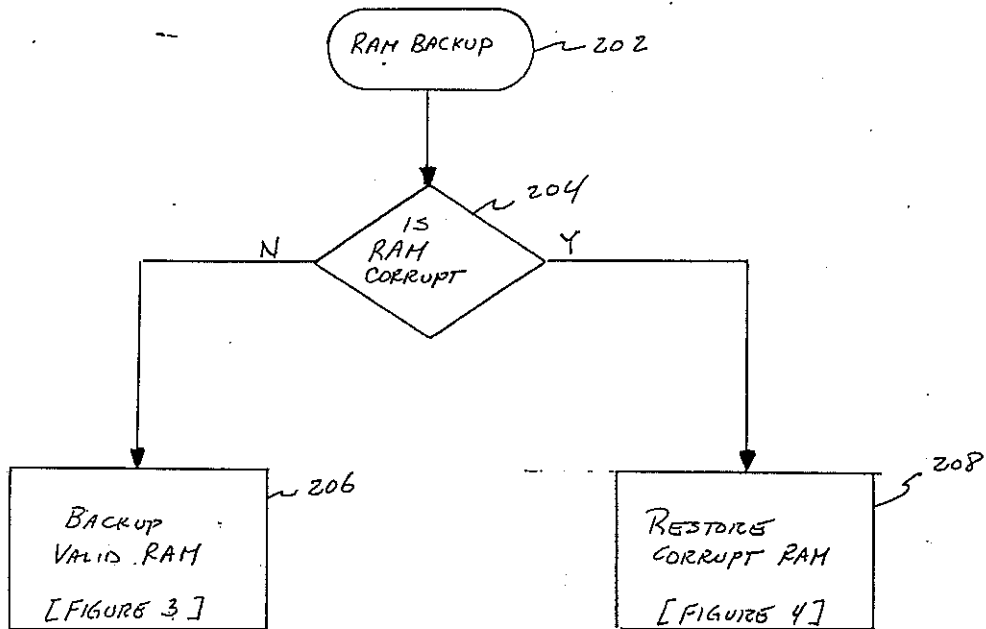


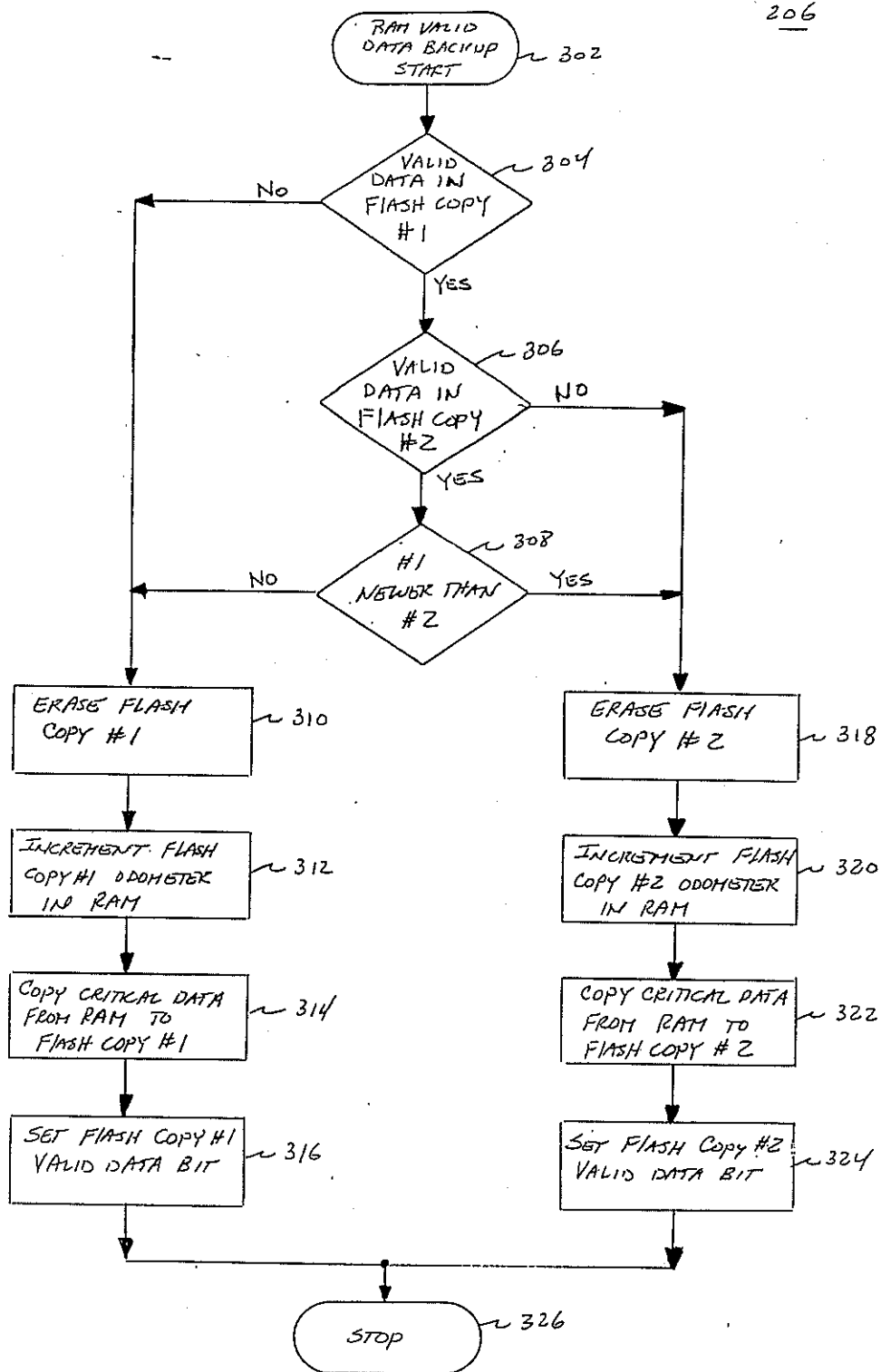
FIGURE 2

200

42-509 20 SHEETS ENCLAVE 5 SQUARE
42-509 100 RECYCLED WHITE 5 SQUARE
42-509 200 RECYCLED WHITE 5 SQUARE
42-509 200 RECYCLED WHITE 5 SQUARE

RECYCLED PAPER
42-509 200 RECYCLED WHITE 5 SQUARE

FIGURE 3



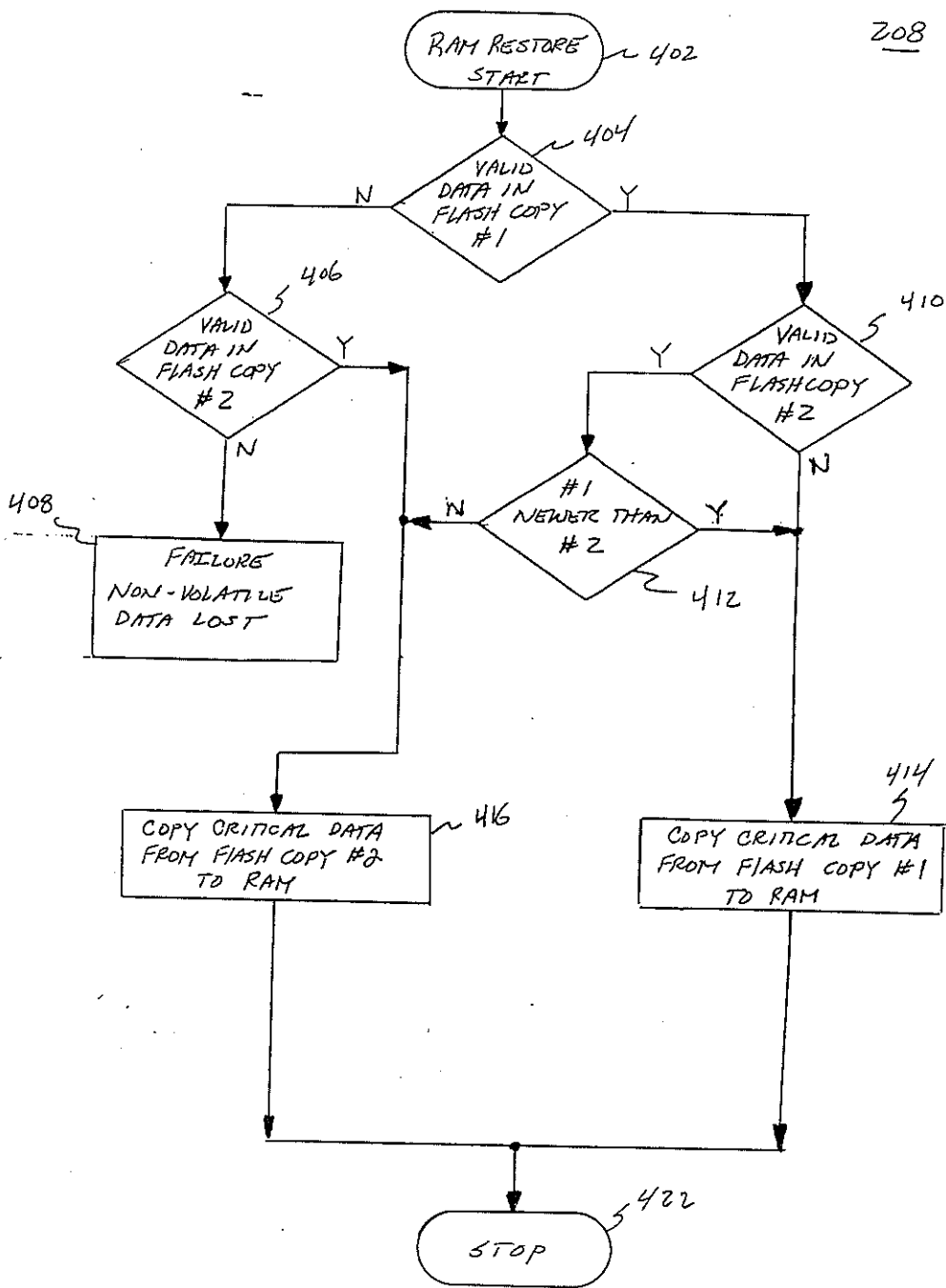


FIGURE 4

42-300 200 SHEETS PER CASE 5 SQUARE
42-302 100 RECYCLED WHITE 5 SQUARE
42-306 200 RECYCLED WHITE 5 SQUARE
MAY 2010 U.S.A.



08/322808

74-348 100% RECYCLED GLASS 3 SQUARE
42-396 100% RECYCLED WHITE 5 SQUARE
MADE IN U.S.A.

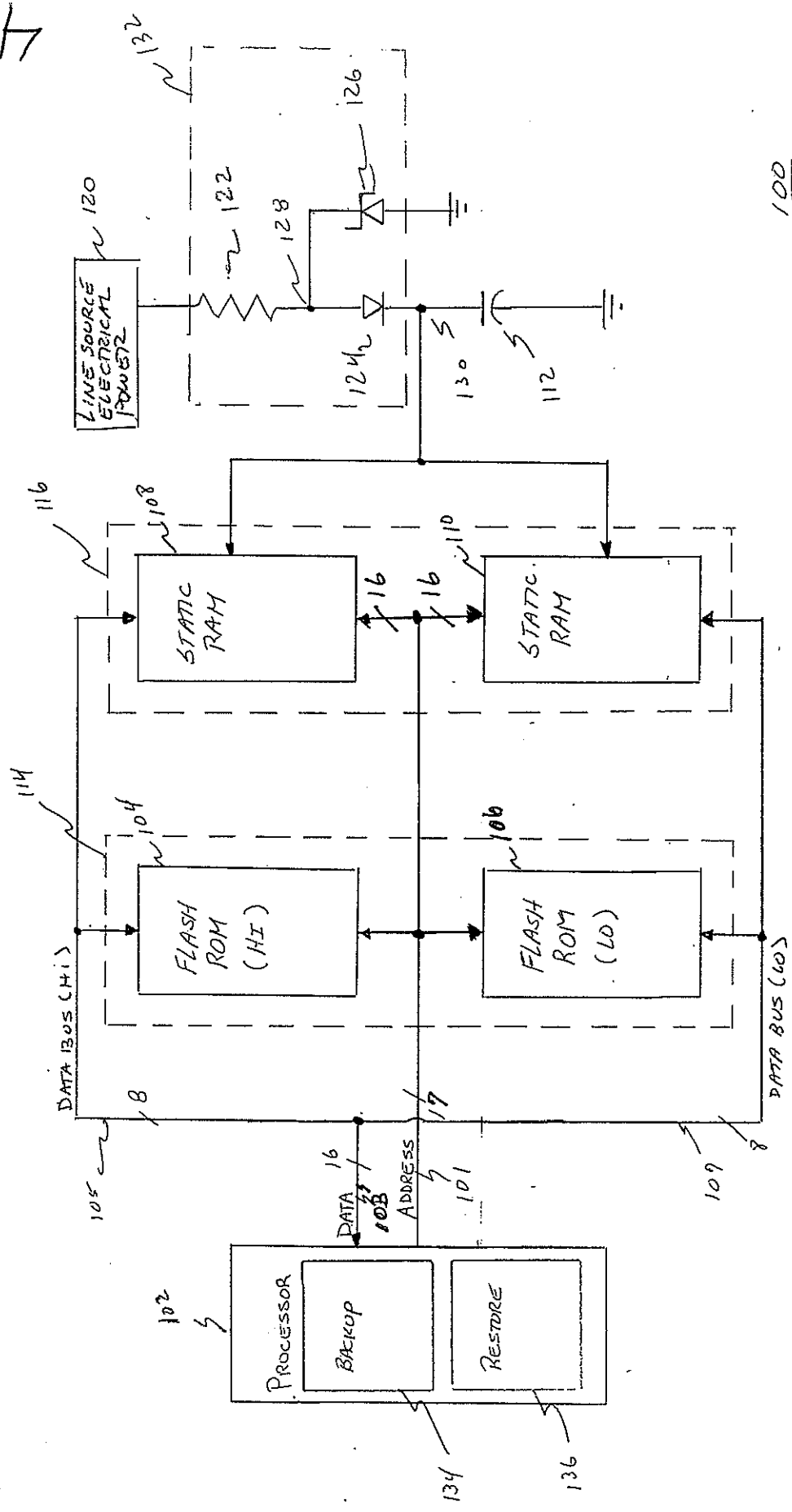


FIGURE 1

444555-III



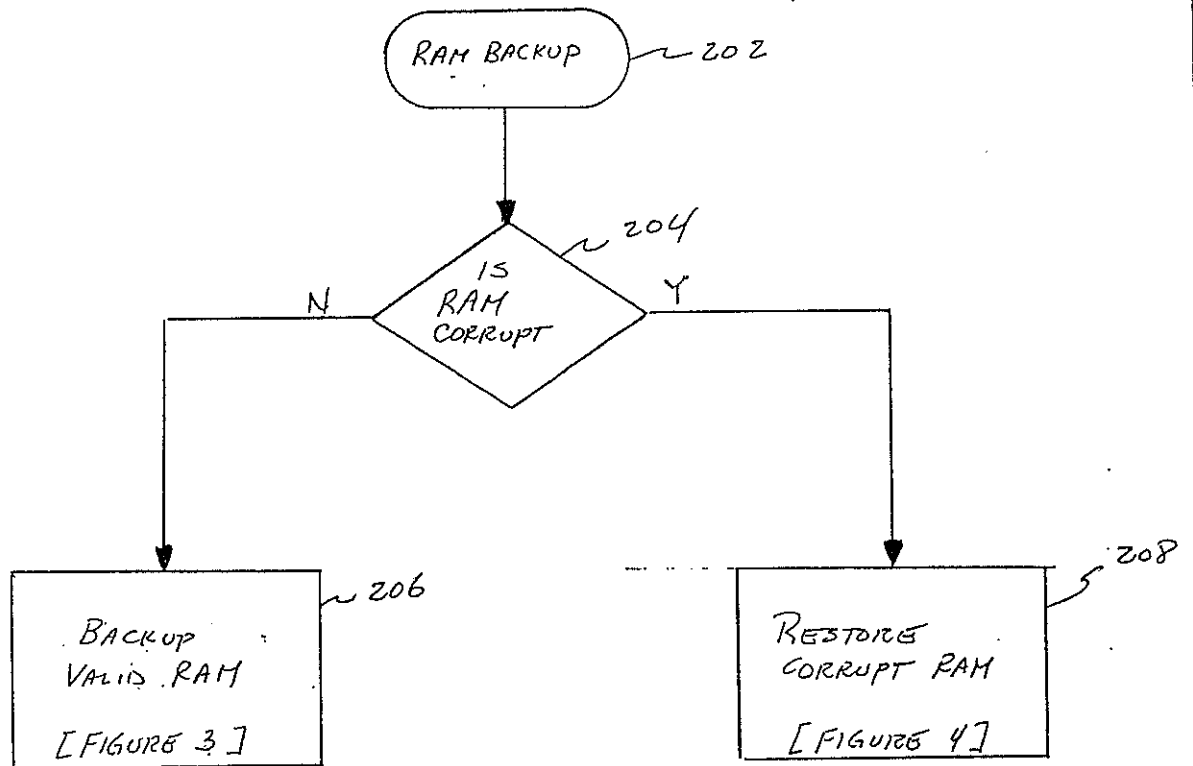


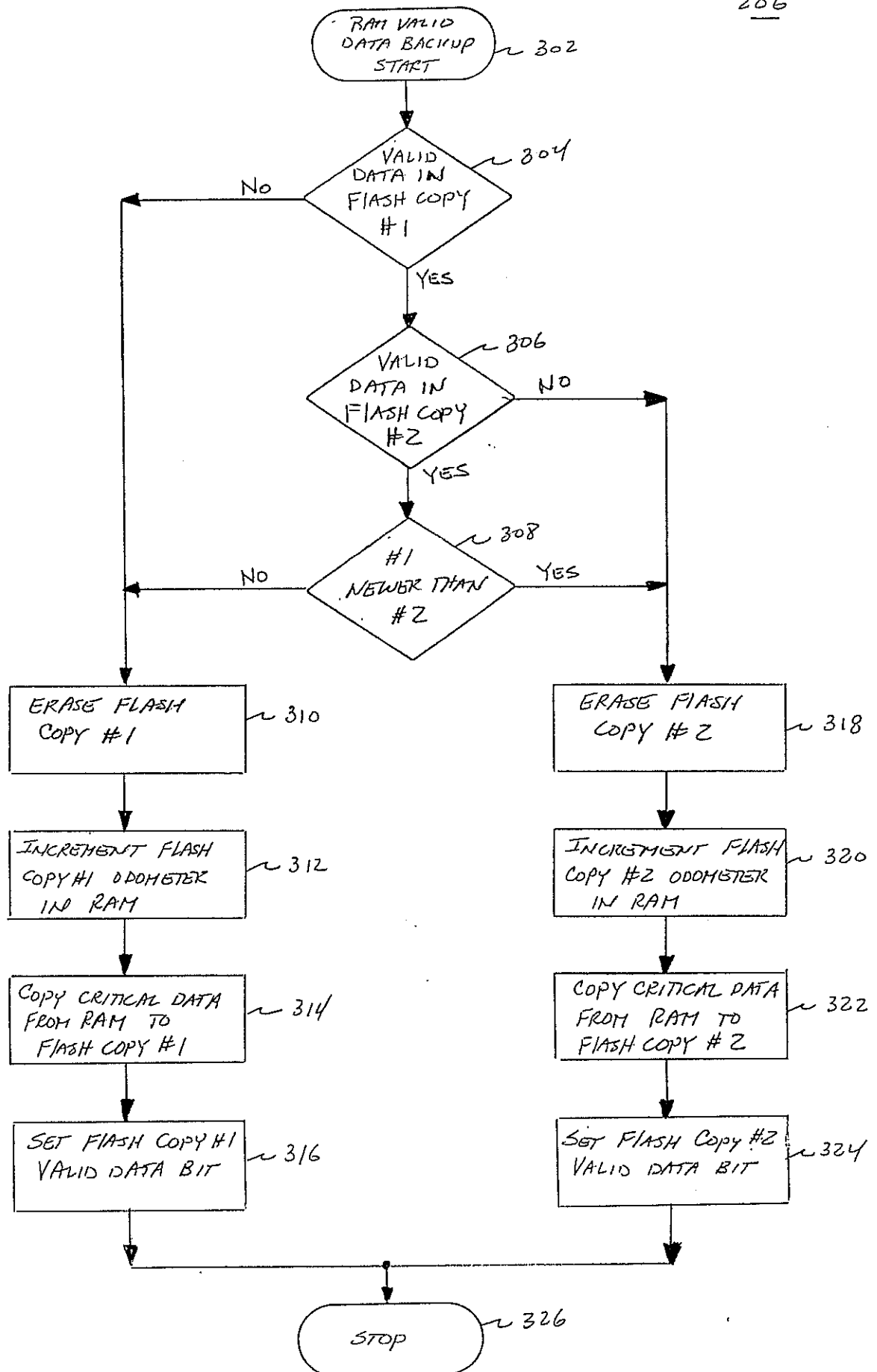
FIGURE 2

200

008881-00



206



808350-01



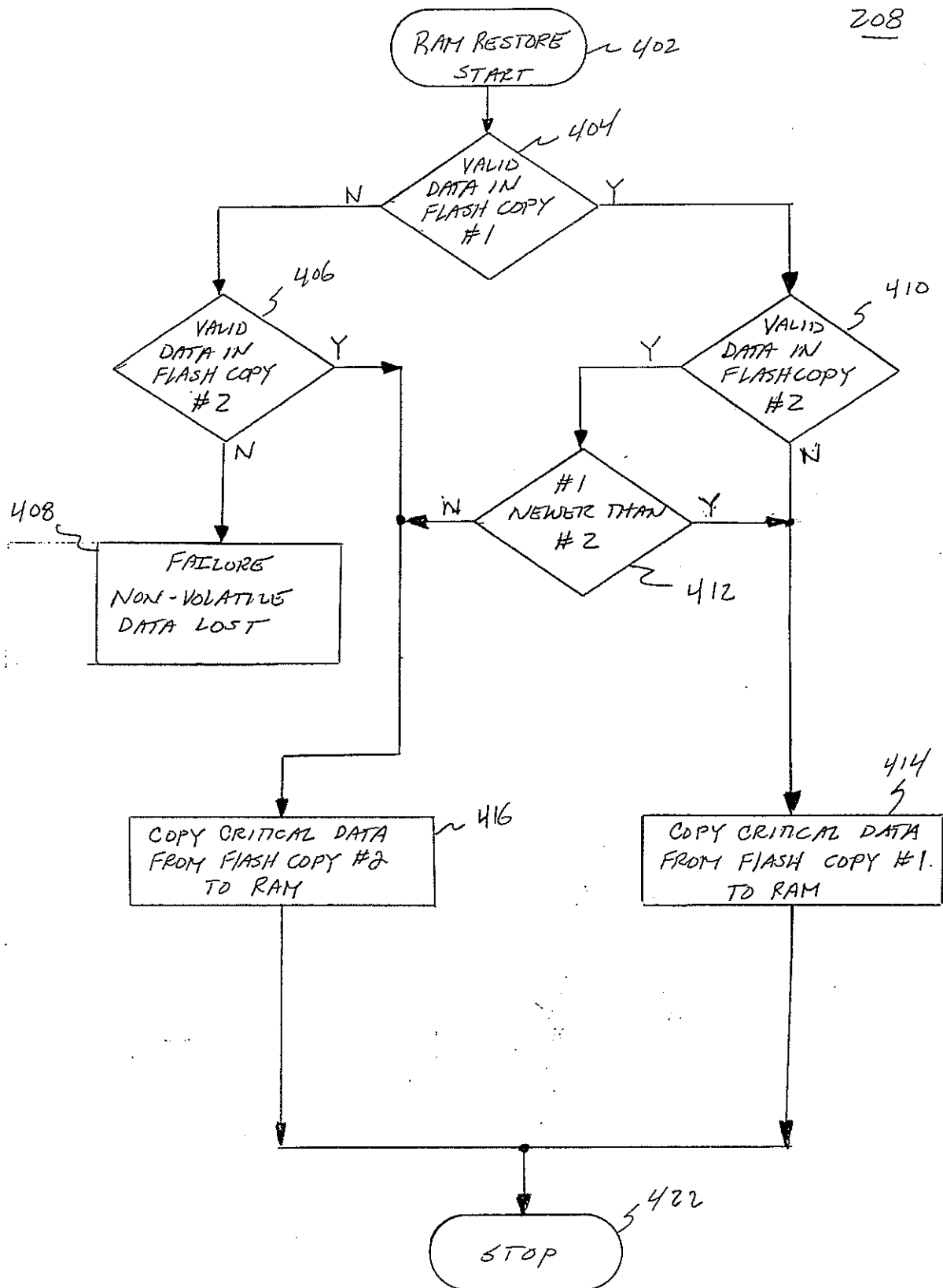


FIGURE 4



A handwritten signature in black ink, consisting of a large, stylized 'A' followed by a cursive 'C' and a long horizontal stroke.

HEWLETT-PACKARD COMPANY
Legal Department, 2080
P. O. Box 10301
Palo Alto, California 94303-0890

PATENT APPLICATION

ATTORNEY DOCKET NO. 1094458

08/322808



IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) Reasoner et al.

Serial No. (to be assigned)

Examiner: (to be assigned)

Filing Date: (herewith)

Group Art Unit: (to be assigned)

Title: System And Method For RAM Power And Data Backup
Utilizing A Capacitor And ROM

THE COMMISSIONER OF PATENTS & TRADEMARKS
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- (x) under 37 CFR 1.97 (b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)
- () under 37 CFR 1.97 (c) together with either a:
 - () Certification under 37 CFR 1.97(e), or
 - () a \$210.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- () under 37 CFR 1.97 (d) together with a:
 - () Certification under 37 CFR 1.97 (e), and
 - () a petition under 37 CFR 1.97 (d)(2)(ii), and
 - () a \$130.00 petition fee set forth in 37 CFR 1.17 (i)(1).
(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Please charge to Deposit Account 08-2025 the sum of _____. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

() A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

Respectfully submitted,

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Date of Deposit: October 13, 1994

Typed Name: Valerie Bakes

Signature: Valerie Bakes

Rev 10/94 (Form 3.05A)

By

Daniel N. Yannuzzi

Attorney/Agent for Applicant(s)
Reg. No. 36,727

Date: October 12, 1994

Telephone No.: (202) 371-2643

(Use several sheets if necessary)

SERIAL NO.
(to be assigned)
58 / 32808

FILING DATE 10/13/94
(to be assigned)

GROUP 2571
~~(to be assigned)~~

U.S. PATENT DOCUMENTS

[illegible][illegible]

047	APR	NEC Document No. CEP-1004G, "Supercap" User's Manual, published 6/92.
EXAMINER	Do Hyun Yoo	DATE CONSIDERED 5/12/95

Petitioner Intel Corp., Ex. 1015
IPR2023-00783, Pg. 61

USER'S MANUAL

NEC

"SUPERCAP"

(Electric Double-Layer Capacitors)

"SUPERCAP"

(Electric Double-Layer Capacitors)

UP TO 2 200 000 MICROFARAD, SMALL, BATTERY-LIKE CAPACITORS THAT CAN PROTECT CIRCUITS AGAINST TEMPORARY POWER SHUT-DOWNS

The expanding use of digital processing with its associated memory is driving the need for a standby power source to maintain the contents of volatile memories or to continue processing function during AC power outages. Historically, this standby function has been a choice between primary or secondary batteries.

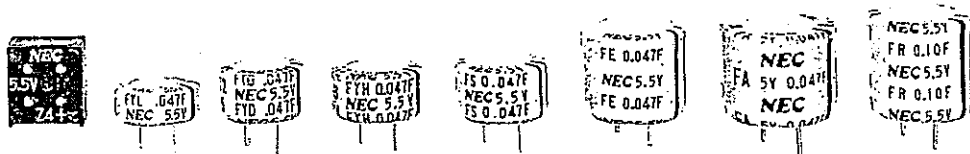
The use of nonrechargeable (primary) batteries, such as Lithium, may be risky since there is no way to determine how much charge is still available to handle a power outage of unknown duration. Rechargeable batteries, such as Ni-Cd must have a controlled charge rate to limit current to battery, and must be periodically replaced.

More recently, the use of CMOS and other low power drain technologies in processor and memory IC's has drastically reduced the total standby power requirements. This coupled with the fact that most power outages last only a short period of time (order of several hours) has opened the door for the **SUPERCAP** as a third alternative standby power source.

SUPERCAP is a completely innovative type of capacitor providing a volumetric efficiency (capacitance per unit volume of a given voltage) of 10 to 50 times that of conventional aluminum electrolytic capacitors. The high capacitance (2 200 000 microfarads) and low leakage current makes the **SUPERCAP** an efficient, reliable, and cost effective energy storage device. **SUPERCAP** can be used as standby power sources for CMOS memories and microcomputers up to several weeks during power outages.

The **SUPERCAP** can be assembled on printed circuit boards by conventional soldering processes together with all other components. The **SUPERCAP** can be charged and discharged at both high and low current rates; i.e., microamps to amps.

This brochure tells the **SUPERCAP** story.



CONTENTS

1. FEATURES	1
1.1 Extremely High Volumetric Efficiency	1
1.2 Simple Installation and Maintenance Free	1
1.3 Wide Operating Temperature Range	1
1.4 "Open" Failure Mode	1
1.5 Long Life	1
2. ORDERING INFORMATION	2
2.1 Catalog Numbering System	2
2.2 Outline Drawing	2
2.3 Taping Specification	4
3. STANDARD PRODUCTS	5
3.1 FA Series	5
3.2 FE Series	5
3.3 FS Series	6
3.4 FR Series	6
3.5 FY Series	7
3.6 3.5 V, 6.5 V Series	8
3.7 FM Series	8
4. TECHNICAL DATA	10
4.1 Specifications	10
4.2 Measuring Method	12
4.3 Charge/Discharge Characteristics	13
4.4 Life Test Data	15
4.5 Environmental Test Data	19
5. APPLICATION NOTES	22
5.1 Major Power Interruptions	22
5.2 Power Backup Design	23
5.3 Backup Time Capability	24
5.4 Capacitance Selection Method	25
5.5 Backup Circuit	30
5.6 Typical Applications	33
5.7 Series/Parallel Connection	34
5.8 General Hints and Suggestions	34
6. PRINCIPLE AND STRUCTURE	35
6.1 Operating Principle	35
6.2 Product Structure	36
6.3 Manufacturing Process and Quality Control	38

1. FEATURES

1.1 Extremely High Volumetric Efficiency

The capacitance per unit area of the electric double layer is estimated as high as 20 to 40 $\mu\text{F}/\text{cm}^2$. The surface area of the activated carbon is around 10,000,000 cm^2 per gram. Consequently, one gram of activated carbon particles can be calculated to provide 200 to 400 F of capacitance.

This is why **SUPERCAP** has extremely high capacitance value in such a small package.

1.2 Simple Installation and Maintenance Free

As the **SUPERCAP** is a capacitor, there is no problem with charging/discharging no matter how quickly or how frequently it is conducted. Unlike Ni-Cd batteries, there need neither specific charging circuit nor troublesome charging conditions.

1.3 Wide Operating Temperature Range

The operating temperature range of **SUPERCAP** is wider than battery's. (FR: -40°C to $+85^\circ\text{C}$, FE: -40°C to $+70^\circ\text{C}$, others: -25°C to $+70^\circ\text{C}$)

Operation at higher temperature on continuous basis will result in a decrease in capacitance. That means the backup time capability will be reduced.

1.4 "Open" Failure Mode

The failure mode of conventional capacitors is generally characterized by "short", but in case of **SUPERCAP**, it becomes "open" only when excess voltage and/or temperature has been impressed for a long time period, resulting in gassing from electrolyte and losing electrical contact between carbon particles and electroconductive rubber. Explosion by gassing can not happen because of very low content of electrolyte in unit cells.

1.5 Long Life

On top of its low content of electrolyte, the simple product structure and the hermeticity of unit cells promise a longer life for **SUPERCAP** in comparison with conventional aluminum electrolytic capacitors.

1.6 Taping Package for Automatic Assembly

Resin molded type has been developed as the FM series which is deliverable with the taping package for automatic assembly.

1.7 Extension to Specific Range of Rated Voltages for Specific Applications

In pursuit of total performance of the circuit, other line-up in specific rated voltages have been required very often for a few years.

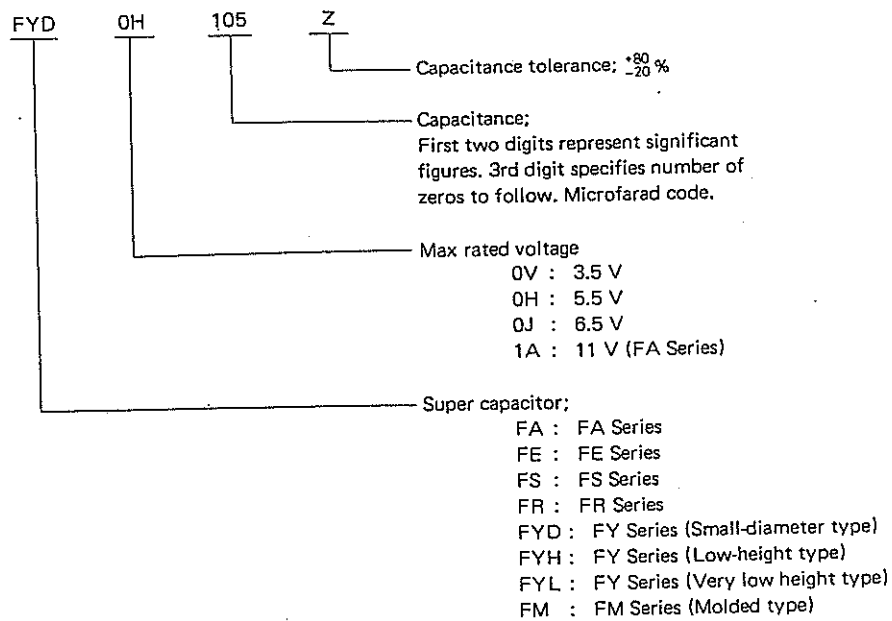
For responding to those requirements, NEC has standardized the 3.5 V and 6.5 V series as the extension to new direction.

NEC's line-up in rated voltage, therefore, consists of 3.5 V, 5.5 V, 6.5 V and 11 V.

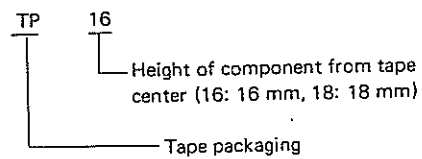
With the features mentioned above, the **SUPERCAP** can be ranked as a device between a battery and a capacitor. Once **SUPERCAP** is designed in, you can be free from power interruptions or battery maintenance in your systems with microcomputers/C MOS memories.

2. ORDERING INFORMATION

2.1 Catalog Numbering System

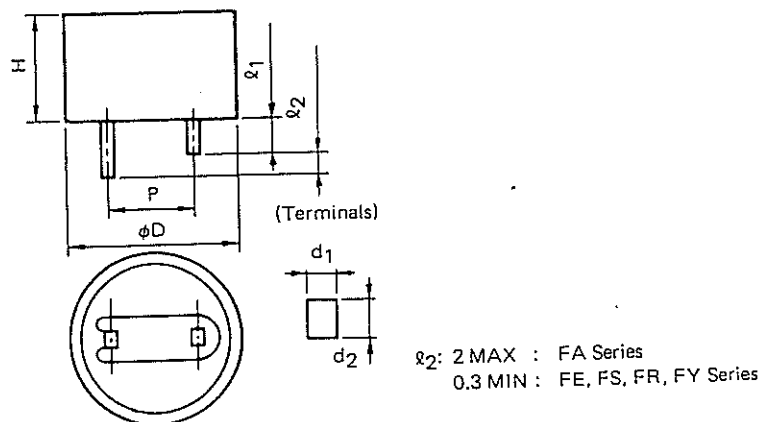


Following on this catalog numbering in bulk, taping specification numbering for FM series is undermentioned.

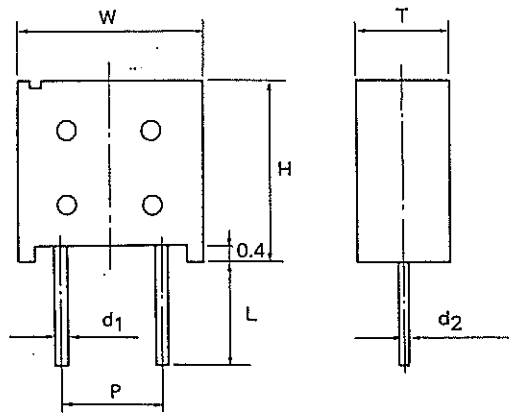


2.2 Outline Drawing (unit in mm)

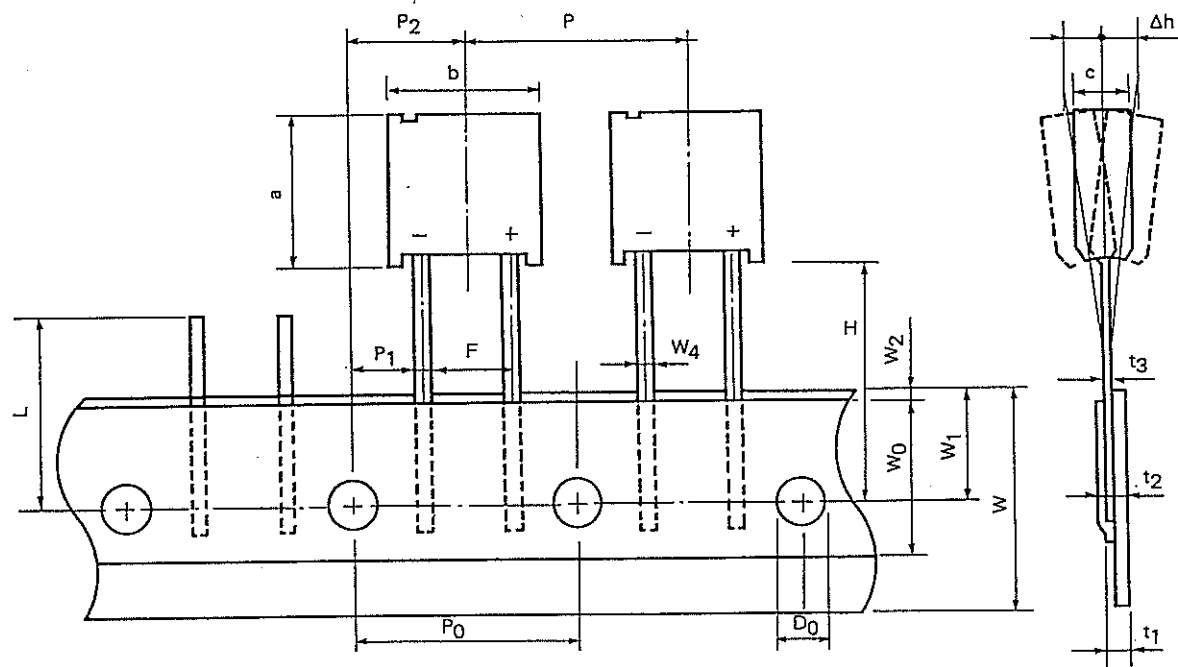
- Can Case Type (FA, FE, FS, FR, FY Series)



- Molded Type (FM Series)



2.3 Taping Specification (Ammo pack, Applicable only for FM Series)



Unit in mm

Item	Symbol	Value	Tolerance	Remarks
Component Height	a	11.5	± 0.5	
Component Width	b	10.5	± 0.5	
Component Thickness	c	*	± 0.5	* 5.0 for 0.01 F to 0.047 F, 6.5 for 0.1 F
Lead-wire Width	W4	0.5	± 0.1	
Lead-wire Thickness	t3	0.4	± 0.1	
Pitch of Component	P	12.7	± 1.0	
Sprocket pitch	P0	12.7	± 0.3	
Sprocket hole center to lead	P1	3.85	± 0.7	
Sprocket hole to component center	P2	6.35	± 1.3	
Lead spacing	F	5.0	± 0.5	
Component Alignment	Δh	2.0 MAX.	—	
Tape width	W	18.0	+ 1.0 - 0.5	
Hold-down tape width	W0	12.5 MIN.	—	
Sprocket hole position	W1	9.0	± 0.5	
Hold-down tape position	W2	3.0 MAX.	—	
Height of component from tape center	H	16.0	± 0.5	
		18.0	± 0.5	
Sprocket hole diameter	D0	φ4.0	± 0.2	
Total tape thickness	t1	0.7	± 0.2	
	t2	1.5 MAX.	—	
Length of shipped lead	L	11 MAX.	—	

3. STANDARD PRODUCTS

3.1 FA Series

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. Ia	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	D ± 0.5	H MAX.	P ± 0.3	d1 ± 0.1	d2 ± 0.1	ℓ1 MAX.	g (oz)
FA0H473Z	0.047	5.5	20	0.071	16.0 (0.630)	15.5 (0.610)	5.1 (0.2)	0.4 (0.016)	1.2 (0.047)	5.0 (0.197)	6.2 (0.219)
FA0H104Z	0.1	5.5	8	0.15	21.5 (0.846)	15.5 (0.610)	7.6 (0.3)	0.6 (0.024)	1.2 (0.047)	5.5 (0.217)	12 (0.423)
FA0H224Z	0.22	5.5	5	0.33	28.5 (1.122)	16.5 (0.650)	10.2 (0.4)	0.6 (0.024)	1.4 (0.055)	9.5 (0.374)	25 (0.882)
FA0H474Z	0.47	5.5	3.5	0.71	36.5 (1.437)	16.5 (0.650)	15 (0.591)	0.6 (0.024)	1.7 (0.067)	9.5 (0.374)	42 (1.482)
FA0H105Z	1.0	5.5	2.5	1.5	44.5 (1.752)	18.5 (0.728)	20 (0.787)	1.0 (0.039)	1.4 (0.055)	9.5 (0.374)	65 (2.293)
FA1A223Z	0.022	11	20	0.066	16.0 (0.630)	25.0 (0.984)	5.1 (0.2)	0.4 (0.016)	1.2 (0.047)	5.0 (0.197)	7.5 (0.265)
FA1A104Z	0.1	11	8	0.3	28.5 (1.122)	25.5 (1.004)	10.2 (0.4)	0.6 (0.024)	1.4 (0.055)	9.5 (0.374)	32 (1.129)
FA1A224Z	0.22	11	6	0.66	36.5 (1.437)	27.5 (1.083)	15 (0.591)	1.0 (0.039)	1.4 (0.055)	9.5 (0.374)	55 (1.940)
FA1A474Z	0.47	11	4	1.41	44.5 (1.752)	28.5 (1.122)	20 (0.787)	1.0 (0.039)	1.4 (0.055)	9.5 (0.374)	83 (2.928)

Note 1) Capacitance tolerance: +80 %, −20 %; 2) Weight is typical.

3.2 FE Series

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. Ia	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	D ± 0.5	H MAX.	P ± 0.5	d1 ± 0.1	d2 ± 0.1	ℓ1 MIN.	g (oz)
FE0H473Z	0.047	5.5	14	0.071	14.5 (0.57)	14.0 (0.55)	5.1 (0.2)	0.4 (0.016)	1.2 (0.047)	2.2 (0.087)	1.2 (0.042)
FE0H104Z	0.1	5.5	6.5	0.15	16.5 (0.65)	14.0 (0.55)	5.1 (0.2)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	5 (0.177)
FE0H224Z	0.22	5.5	3.5	0.33	21.5 (0.85)	15.5 (0.61)	7.6 (0.3)	0.6 (0.024)	1.2 (0.047)	3.0 (0.118)	9.5 (0.336)
FE0H474Z	0.47	5.5	1.8	0.71	28.5 (1.12)	16.5 (0.65)	10.2 (0.4)	0.6 (0.024)	1.4 (0.055)	6.1 (0.240)	16 (0.565)
FE0H105Z	1.0	5.5	1.0	1.5	36.5 (1.44)	18.5 (0.73)	15.0 (0.59)	0.6 (0.024)	1.7 (0.067)	6.1 (0.240)	38 (1.343)
FE0H155Z	1.5	5.5	0.6	2.3	44.5 (1.75)	18.5 (0.73)	20.0 (0.79)	1.0 (0.039)	1.4 (0.055)	6.1 (0.240)	72 (2.544)

Note 1) Capacitance tolerance: +80 %, −20 %; 2) Weight is typical.

3.3 FS Series

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. I _a	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	D ± 0.5	H MAX.	P ± 0.5	d ₁ ± 0.1	d ₂ ± 0.1	ℓ ₁ MIN.	g (oz)
FS0H223Z	0.022	5.5	60	0.033	11.5 (0.453)	8.5 (0.335)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	1.6 (0.057)
FS0H473Z	0.047	5.5	40	0.071	13.0 (0.512)	8.5 (0.335)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.2 (0.087)	2.6 (0.092)
FS0H104Z	0.1	5.5	25	0.15	16.5 (0.650)	8.5 (0.335)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	4.1 (0.145)
FS0H224Z	0.22	5.5	25	0.33	16.5 (0.650)	13.0 (0.512)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	5.3 (0.187)
FS0H474Z	0.47	5.5	13	0.71	21.5 (0.846)	13.0 (0.512)	7.62 (0.300)	0.6 (0.024)	1.2 (0.047)	3.0 (0.118)	10 (0.353)
FS0H105Z	1.0	5.5	7	1.5	28.5 (1.122)	14.0 (0.551)	10.16 (0.400)	0.6 (0.024)	1.4 (0.055)	6.1 (0.240)	18 (0.635)

Note 1) Capacitance tolerance: +80 %, -20 %; 2) Weight is typical.

3.4 FR Series

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. I _a	MIN. SD	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	(V)	D ± 0.5	H MAX.	P ± 0.5	d ₁ ± 0.1	d ₂ ± 0.1	ℓ ₁ MIN.	g (oz)
FR0H223Z	0.022	5.5	220	0.033	4.2	11.5 (0.453)	14.0 (0.551)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	2.3 (0.081)
FR0H473Z	0.047	5.5	110	0.071	4.2	14.5 (0.571)	14.0 (0.551)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.4 (0.095)	3.9 (0.138)
FR0H104Z	0.1	5.5	150	0.15	4.2	14.5 (0.571)	15.5 (0.610)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.4 (0.095)	4.3 (0.152)
FR0H224Z	0.22	5.5	180	0.33	4.2	14.5 (0.571)	21.0 (0.827)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.4 (0.095)	5.3 (0.187)
FR0H474Z	0.47	5.5	100	0.71	4.2	16.5 (0.650)	21.5 (0.846)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	7.5 (0.265)
FR0H105Z	1.0	5.5	60	1.5	4.2	21.5 (0.850)	22.0 (0.866)	7.62 (0.200)	0.6 (0.024)	1.4 (0.047)	3.0 (0.118)	13.3 (0.470)

Note 1) Capacitance tolerance: +80 %, -20 %; 2) Weight is typical.
3) SD: voltage holding characteristic.

3.5 FY Series

• FYD type: Small diameter

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. I _a	MIN. SD	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	(V)	D ± 0.5	H MAX.	P ± 0.5	d ₁ ± 0.1	d ₂ ± 0.1	ℓ ₁ MIN.	g (oz)
FYD0H223Z	0.022	5.5	220	0.033	4.2	11.5 (0.453)	8.5 (0.335)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	1.6 (0.056)
FYD0H473Z	0.047	5.5	220	0.071	4.2	11.5 (0.453)	8.5 (0.335)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	1.65 (0.058)
FYD0H104Z	0.1	5.5	100	0.15	4.2	13.0 (0.512)	8.5 (0.335)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.2 (0.087)	2.4 (0.085)
FYD0H224Z	0.22	5.5	120	0.33	4.2	14.5 (0.571)	15.0 (0.591)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.4 (0.095)	4.3 (0.152)
FYD0H474Z	0.47	5.5	65	0.71	4.2	16.5 (0.65)	15.0 (0.591)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	6.0 (0.212)
FYD0H105Z	1.0	5.5	35	1.5	4.2	21.5 (0.85)	16.0 (0.629)	7.62 (0.300)	0.6 (0.024)	1.2 (0.047)	3.0 (0.118)	11.0 (0.388)
FYD0H145Z	1.4	5.5	45	2.1	4.2	21.5 (0.85)	19.0 (0.748)	7.62 (0.300)	0.6 (0.024)	1.2 (0.047)	3.0 (0.118)	12.0 (0.424)
FYD0H225Z	2.2	5.5	35	3.3	4.2	28.5 (1.122)	22.0 (0.866)	10.16 (0.400)	0.6 (0.024)	1.4 (0.055)	6.1 (0.240)	22.9 (0.809)

Note 1) Capacitance tolerance: +80 %, −20 %; 2) Weight is typical. 3) SD: voltage holding characteristic.

• FYH type: Low height

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. I _a	MIN. SD	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	(V)	D ± 0.5	H MAX.	P ± 0.5	d ₁ ± 0.1	d ₂ ± 0.1	ℓ ₁ MIN.	g (oz)
FYH0H223Z	0.022	5.5	200	0.033	4.2	11.5 (0.453)	7.0 (0.276)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	1.5 (0.053)
FYH0H473Z	0.047	5.5	100	0.071	4.2	13.0 (0.512)	7.0 (0.276)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.2 (0.087)	2.2 (0.078)
FYH0H104Z	0.1	5.5	50	0.15	4.2	16.5 (0.65)	7.5 (0.295)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	3.4 (0.120)
FYH0H224Z	0.22	5.5	60	0.33	4.2	16.5 (0.65)	9.5 (0.374)	5.08 (0.200)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	3.6 (0.127)
FYH0H474Z	0.47	5.5	35	0.71	4.2	21.5 (0.85)	10.0 (0.394)	7.62 (0.300)	0.6 (0.024)	1.2 (0.047)	3.0 (0.118)	7.2 (0.255)
FYH0H105Z	1.0	5.5	20	1.5	4.2	28.5 (1.122)	11.0 (0.433)	10.16 (0.400)	0.6 (0.024)	1.4 (0.055)	6.1 (0.240)	13.9 (0.491)

Note 1) Capacitance tolerance: +80 %, −20 %; 2) Weight is typical. 3) SD: voltage holding characteristic.

• FYL type: Very low height

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. I _a	MIN. SD	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	(V)	D ± 0.5	H ± 0.5	P ± 0.5	d ₁ ± 0.1	d ₂ ± 0.1	ℓ ₁ MIN.	g (oz)
FYL0H103Z	0.01	5.5	300	0.015	4.2	11.0 (0.43)	5.0 (0.197)	5.08 (0.200)	0.2 (0.016)	1.2 (0.047)	2.7 (0.106)	0.9 (0.032)
FYL0H223Z	0.022	5.5	200	0.033	4.2	11.0 (0.43)	5.0 (0.197)	5.08 (0.200)	0.2 (0.016)	1.2 (0.047)	2.7 (0.106)	1.0 (0.035)
FYL0H473Z	0.047	5.5	200	0.071	4.2	12.0 (0.47)	5.0 (0.197)	5.08 (0.200)	0.2 (0.016)	1.2 (0.047)	2.2 (0.087)	1.2 (0.042)

Note 1) Capacitance tolerance: +80 %, −20 %; 2) Weight is typical. 3) SD: voltage holding characteristic.

3.6 3.5 V, 6.5 V Series

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. Ia	Dimensions mm (inch)						Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	D ± 0.5	H MAX.	P ± 0.5	d1 ± 0.1	d2 ± 0.1	ℓ1 MIN.	g (OZ)
FSH0V433Z	0.043	3.5	50	0.039	11.0 (0.413)	5.2 (0.205)	5.08 (0.2)	0.2 (0.008)	1.2 (0.047)	2.7 (0.106)	1.0 (0.035)
FYD0V563Z	0.056	3.5	150	0.050	11.0 (0.413)	5.2 (0.205)	5.08 (0.2)	0.2 (0.008)	1.2 (0.047)	2.7 (0.106)	1.0 (0.035)
FSH0J223Z	0.022	6.5	60	0.040	11.5 (0.453)	8.5 (0.355)	5.08 (0.2)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	1.7 (0.060)
FYD0J273Z	0.027	6.5	200	0.049	11.5 (0.453)	8.5 (0.355)	5.08 (0.2)	0.4 (0.016)	1.2 (0.047)	2.7 (0.106)	1.6 (0.056)

Note 1) Capacitance: +80 %, -20 %; 2) Weight is typical.

3.7 FM Series (Molded type)

Catalog NBR	Cap.	MAX. Rated Voltage	MAX. ESR	MAX. Ia	MIN. SD	Dimensions mm (inch)							Weight
	(Farad)	(V. DC)	(Ω at 1 kHz)	(mA)	(V)	W ± 0.5	H ± 0.5	T ± 0.5	P ± 0.3	L ± 1.0	d1 ± 0.1	d2 ± 0.1	g (OZ)
FM0H103Z	0.01	5.5	300	0.015	4.2	10.5 (0.413)	11.5 (0.453)	5.0 (0.197)	5.0 (0.197)	5.0 (0.197)	0.5 (0.020)	0.4 (0.016)	1.3 (0.046)
FM0H223Z	0.022	5.5	200	0.033	4.2	10.5 (0.413)	11.5 (0.453)	5.0 (0.197)	5.0 (0.197)	5.0 (0.197)	0.5 (0.020)	0.4 (0.016)	1.3 (0.046)
FM0H473Z	0.047	5.5	200	0.071	4.2	10.5 (0.413)	11.5 (0.453)	5.0 (0.197)	5.0 (0.197)	5.0 (0.197)	0.5 (0.020)	0.4 (0.016)	1.3 (0.046)
FM0H104Z	0.1	5.5	100	0.15	4.2	10.5 (0.413)	11.5 (0.453)	6.5 (0.256)	5.0 (0.197)	5.0 (0.197)	0.5 (0.020)	0.4 (0.016)	1.6 (0.056)

Note 1) Capacitance: +80 %, -20 %; 2) Weight is typical; 3) SD: Voltage holding characteristic.

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 1994-10-13
Document Title - Non-Patent Literature
Page(s) - 9

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

4. TECHNICAL DATA

4.1 Specification

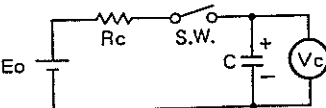
Item		Series	FA		FE		FS			
Operating Temperature Range			-25 °C ~ +70 °C		-40 °C ~ +70 °C		-25 °C ~ +70 °C			
Rated Voltage			5.5 V, 11 V		5.5 V		5.5 V			
Capacitance Range			5.5 V: 0.047 F ~ 1 F 11 V: 0.022 F ~ 0.47 F		0.047 F ~ 1.5 F		0.022 F ~ 1.0 F			
Capacitance Tolerance			+80 %, -20 %		+80 %, -20 %		+80 %, -20 %			
ESR			See table in 3.1		See table in 3.1		See table in 3.1			
Current at 30 min			See table in 3.1		See table in 3.1		See table in 3.1			
Surge Voltage Test	Capacitance	—		more than 90 % of the initial requirement		more than 90 % of the initial requirement				
	ESR	—		less than 120 % of the initial requirement		less than 120 % of the initial requirement				
	Current	—		less than 120 % of the initial requirement		less than 120 % of the initial requirement				
Temperature Characteristics Test	Capacitance	-25 °C	more than 70 % of the initial value		-40 °C	more than 40 % of the initial value		-25 °C	more than 50 % of the initial value	
	ESR		less than 300 % of the initial value			less than 400 % of the initial value			less than 300 % of the initial value	
	Capacitance	—		—		—				
	ESR									
	Capacitance	+70 °C	less than 150 % of the initial value		+70 °C	less than 200 % of the initial value		+70 °C	less than 150 % of the initial value	
	ESR		Shall meet the initial requirement.			Shall meet the initial requirement.			Shall meet the initial requirement.	
	Current		Less than 1.5 CV (mA)			Less than 1.5 CV (mA)			Less than 1.5 CV (mA)	
	Capacitance	+25 °C	within ±20 % of the initial value		+25 °C	within ±20 % of the initial value		+25 °C	within ±20 % of the initial value	
	ESR		Shall meet the initial requirement.			Shall meet the initial requirement.			Shall meet the initial requirement.	
	Current		Shall meet the initial requirement.			Shall meet the initial requirement.			Shall meet the initial requirement.	
Vibration Test	Capacitance	Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				
	ESR									
	Current									
Solderability			At least 75 % covered by continuous new solder coating.		At least 75 % covered by continuous new solder coating.		At least 75 % covered by continuous new solder coating.			
Soldering Heat Resistance	Capacitance	Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				
	ESR									
	Current									
Temperature Cycling	Capacitance	Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				
	ESR									
	Current									
Moisture Resistance	Capacitance	more than 90 % of the initial value		within ±20 % of the initial value		more than 90 % of the initial requirement				
	ESR	less than 120 % of the initial requirement		less than 120 % of the initial requirement		less than 120 % of the initial requirement				
	Current	less than 120 % of the initial requirement		less than 120 % of the initial requirement		less than 120 % of the initial requirement				
Load Life	Capacitance	more than 85 % of the initial requirement		within ±30 % of the initial value		more than 85 % of the initial requirement				
	ESR	less than 120 % of the initial requirement		less than 300 % of the initial requirement		less than 200 % of the initial requirement				
	Current	less than 200 % of the initial requirement		less than 200 % of the initial requirement		less than 200 % of the initial requirement				
Voltage Holding Characteristics			—		—		—			

FY (FYD, FYH, FYL), FM		FR		3.5 V and 6.5 V series				Test Conditions	
-25 °C ~ +70 °C		-40 °C ~ +85 °C		-25 °C ~ +70 °C					
5.5 V		5.5 V		3.5 V		6.5 V			
FYD: 0.022 F ~ 2.2 F FYH: 0.022 F ~ 1.0 F FYL: 0.01 F ~ 0.047 F FMM: 0.01F ~ 0.1 F		0.022 F ~ 1.0 F		0.043 F	0.056 F	0.022 F	0.027 F	Refer to Measuring Method (P.12)	
+80 %, -20 %		+80 %, -20 %		+80 %, -20 %				Refer to Measuring Method (P.12)	
See table in 3.1		See table in 3.1		See table in 3.1					
See table in 3.1		See table in 3.1		See table in 3.1					
more than 90 % of the initial requirement		more than 90 % of the initial requirement		more than 90 % of the initial requirement				Surge Voltage: 6.3 V, Temperature: 70 ± 2 °C (FR Series 85 ± 2 °C) 1000 cycles Charge: 30 sec. Discharge: 9 min 30 sec.	
less than 120 % of the initial requirement		less than 120 % of the initial requirement		less than 120 % of the initial requirement					
less than 120 % of the initial requirement		less than 120 % of the initial requirement		less than 120 % of the initial requirement					
-25 °C	more than 50 % of the initial value	-25 °C	more than 50 % of the initial value	-25 °C	more than 50 % of the initial value				
	less than 400 % of the initial value		less than 400 % of the initial value		less than 400 % of the initial value				
-		-40 °C	more than 30 % of the initial value	-					
			less than 700 % of the initial value						
+70 °C	less than 200 % of the initial value	+85 °C	less than 200 % of the initial value	+70 °C	less than 200 % of the initial value				
	Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				
	Less than 1.5 CV (mA)		Less than 1.5 CV (mA)		Less than 1.5 CV (mA)				
+25 °C	within ±20 % of the initial value	+25 °C	within ±20 % of the initial value	+25 °C	within ±20 % of the initial value				
	Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				
	Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				
Shall meet the initial requirement		Shall meet the initial requirement.		Shall meet the initial requirement.				Frequency: 10 ~ 55 Hz/min. Time: 2 hours each for 3 directions (total 6 hours)	
At least 75 % covered by continuous new solder coating		At least 75 % covered by continuous new solder coating		At least 75 % covered by continuous new solder coating				Temperature: 230 ± 5 °C Time: 5 ± 0.5 sec immersing the 1.6 mm (FA series: 2.5 mm) of lead terminal.	
Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				Temperature: 260 ± 10 °C Time: 10 ± 1 sec immersing the 1.6 mm (FA series: 2.5 mm) of lead terminal.	
Shall meet the initial requirement.		Shall meet the initial requirement.		Shall meet the initial requirement.				Temperature: -25 °C (FR·FE: -40 °C) +70 °C (FR: +85 °C) 5 cycles	
within ±20 % of the initial value		within ±20 % of the initial value		within ±20 % of the initial value				Temperature: 40 ± 2 °C Relative Humidity: 90 ~ 95 % Time: 240 hours	
less than 120 % of the initial requirement		less than 120 % of the initial requirement		less than 200 % of the initial requirement					
less than 120 % of the initial requirement		less than 120 % of the initial requirement		less than 120 % of the initial requirement					
within ±30 % of the initial value		within ±30 % of the initial value		within ±30 % of the initial value				Temperature: 70 ± 2 °C (FR: 85 °C ± 2 °C) Applied Voltage: Rated Voltage Series Resistance: 0 Ω Time: 1000 hours	
less than 200 % of the initial requirement		less than 200 % of the initial requirement		less than 300 % of the initial requirement					
less than 200 % of the initial requirement		less than 200 % of the initial requirement		less than 200 % of the initial requirement					
Voltage between terminal leads shall be higher than 4.2 V.		Voltage between terminal leads shall be higher than 4.2 V.		Voltage between terminal leads shall be higher than 4.2 V.				Charge	Applied Voltage: 5 V Time: 24 hours
								Discharge	Time: 24 hours

4.2 Measuring Method

(1) Capacitance

Capacitance can be calculated using the formula in Fig. 1 by using the charging time constant (τ) being measured from the circuit diagram.

$$C = \frac{\tau}{R_c} \text{ (F)}$$


Eo : 3.0 V. DC for Rated Voltage Code 0V (3.5 V)
: 5.0 V. DC for Rated Voltage Code 0H (5.5 V)
: 6.0 V. DC for Rated Voltage Code 0J (6.5 V)
: 10.0 V. DC for Rated Voltage Code 1A (11 V)
r : Time period (sec) to reach Vc = 0.632 Eo
Rc :

Series Cap	FA	FE	FS	FY			FM	FR	3.5 V, 6.5 V
				FYD	FYH	FYL			
0.01F	—	—	—	—	—	5 kΩ	5 kΩ	—	0.022 F ~ 0.056 F 2 kΩ
0.022F	1 kΩ	—	1 kΩ	2 kΩ	2 kΩ	2 kΩ	2 kΩ	2 kΩ	
0.047F	1 kΩ	1 kΩ	1 kΩ	2 kΩ	1 kΩ	2 kΩ	2 kΩ	1 kΩ	—
0.1F	510 Ω	510 Ω	510 Ω	1 kΩ	510 Ω	—	1 kΩ	1 kΩ	—
0.22F	200 Ω	200 Ω	200 Ω	510 Ω	510 Ω	—	—	510 Ω	—
0.47F	100 Ω	100 Ω	100 Ω	200 Ω	200 Ω	—	—	200 Ω	—
1.0F	51 Ω	51 Ω	100 Ω	100 Ω	100 Ω	—	—	100 Ω	—
1.4F	—	—	—	200 Ω	—	—	—	—	—
1.5F	—	51 Ω	—	—	—	—	—	—	—
2.2F	—	—	—	100 Ω	—	—	—	—	—

Fig. 1 Capacitance Measurement

(2) Equivalent series resistance (ESR)

A measuring circuit and formula are shown in Fig. 2.

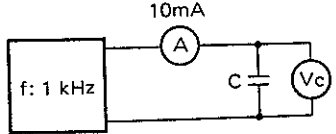
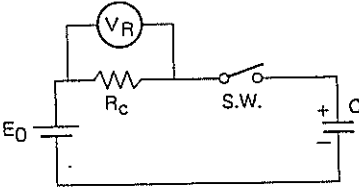
$$ESR = \frac{V_c}{10^{-2}} \text{ (}\Omega\text{)}$$


Fig. 2 ESR Measurement

(3) Current (at 30 minutes after charging)

A measuring circuit and formula are shown in Fig. 3.
Current shall be calculated from the equation below.
Prior to measurement, both lead terminals must be short-circuited for a minimum of 30 minutes.
The lead terminal connected to the metal can case is connected to the negative side of the power supply.

E0 : The same as 4.2 (1) above
Rc : 0.01F to 0.056F 1,000 Ω
0.10 to 0.47F 100 Ω
1.0F to 2.2F 10 Ω



$$\text{Current} = \frac{V_R}{R_c} \times 10^3 \text{ (mA)}$$

Fig. 3 Current Measurement

4.3 Charge/Discharge Characteristics

(1) Charging characteristics

Charging characteristics of 5 V, 0.047F is shown in Fig. 4.

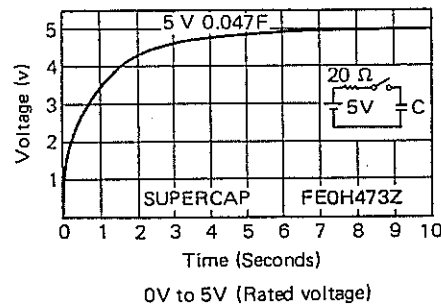


Fig. 4 Charging Characteristics

SUPERCAP, as a battery, has excellent charging characteristics since it can be charged within seconds.

(2) Charging Current

Fig. 5 shows a typical charging current, which reaches very low current level (i.e. leakage current) long hours after the charging started.

The power dissipation in keeping the rated voltage applied to the **SUPERCAP** can be roughly estimated by this ultimate leakage current.

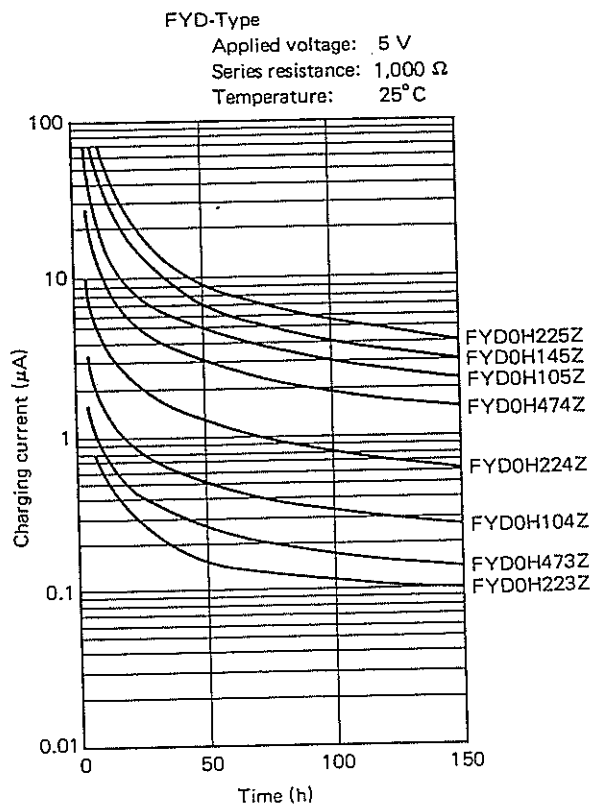


Fig. 5 Charging Current

(3) Discharge Characteristics

Only a figure for discharge characteristics of FYD0H473Z is mentioned typically here in this section, however many figures for all the types are necessary and very useful for the capacitance selection in circuit design. All of those figures are mentioned in later section of Capacitance Selection Method.

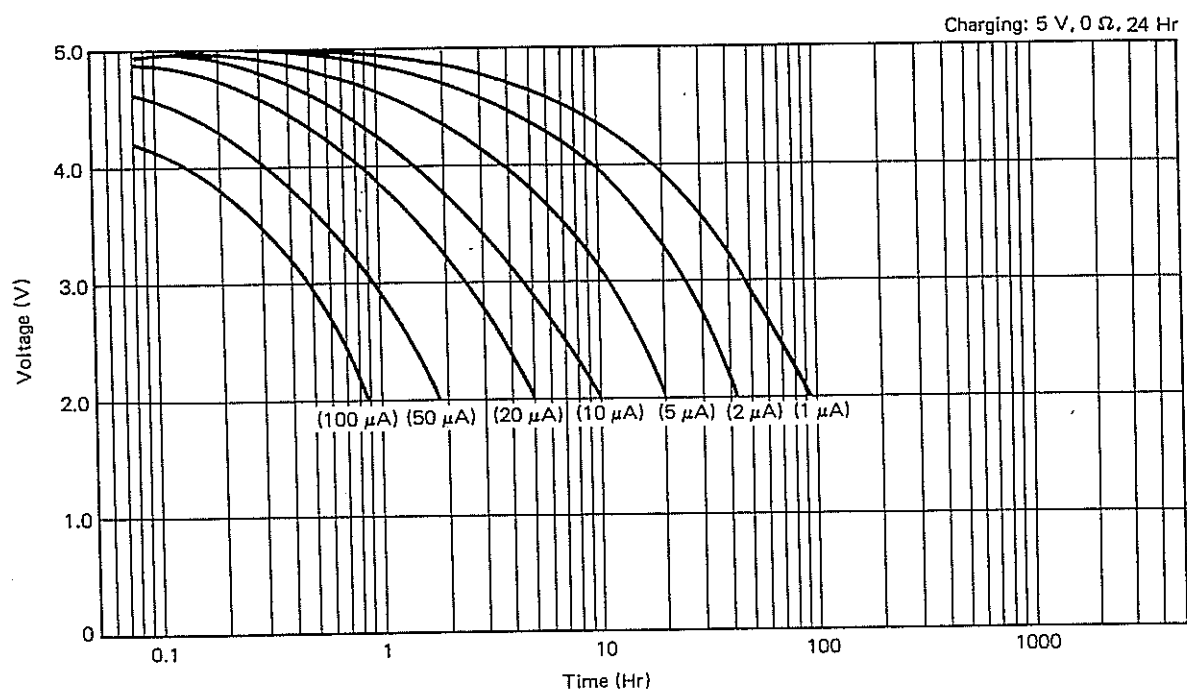


Fig. 6 Load Discharge Characteristics of FYD0H473Z

(4) Self discharge characteristics

Self discharge characteristics shown in Fig. 7.

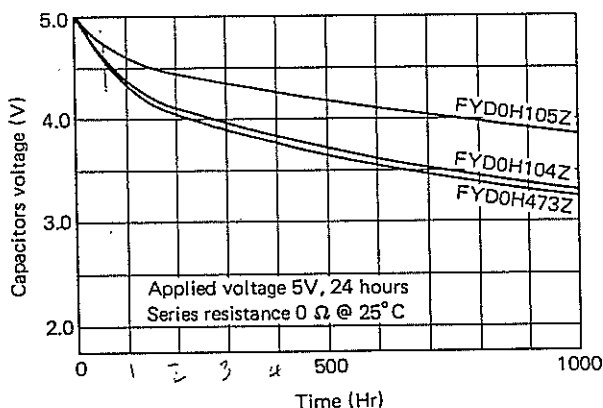


Fig. 7 Voltage Holding Characteristics of FYD Series

4.4 Life Test Data

The following information is reference data and not guaranteed specifications.

(1) Charge/discharge cycles

Fig. 8 shows capacitance and ESR change during 15,000 charge/discharge cycle life test.

The time period is 30 sec on charge and 30 sec on discharge with no series resistors connected.

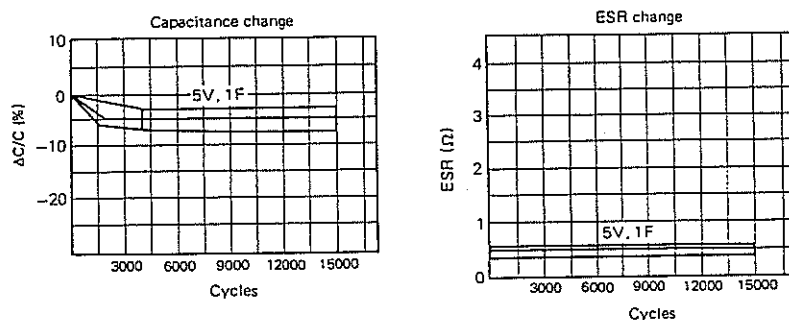


Fig. 8 Charge/Discharge Cycle Test Data

The test conditions are more severe than NEC guarantee specification.

Charging and discharging SUPERCAP is limitless in repetition because the mechanism is based on physical phenomena which gives no damage to SUPERCAP at all.

While since a Ni-Cd battery makes use of a chemical reaction, it can not be repeated more than a few hundred cycles.

- (2) Life test at maximum operating temperature
 Capacitance and ESR change at life test, are typically shown in Fig. 9, Fig. 10 and 11.
 The test conditions are more severe than NEC guarantee specification.

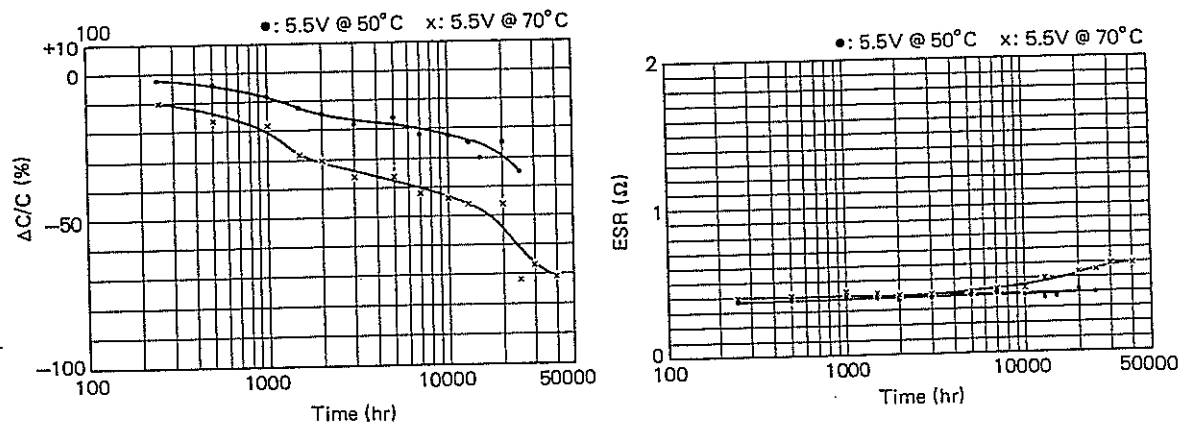


Fig. 9 Life Test Data (FA0H105Z)

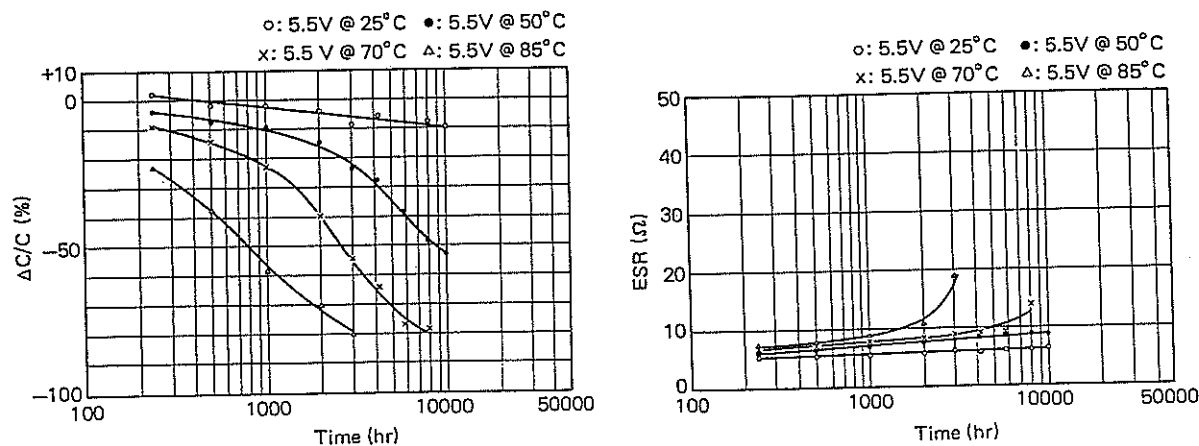


Fig. 10 Life Test Data (FS0H473Z)

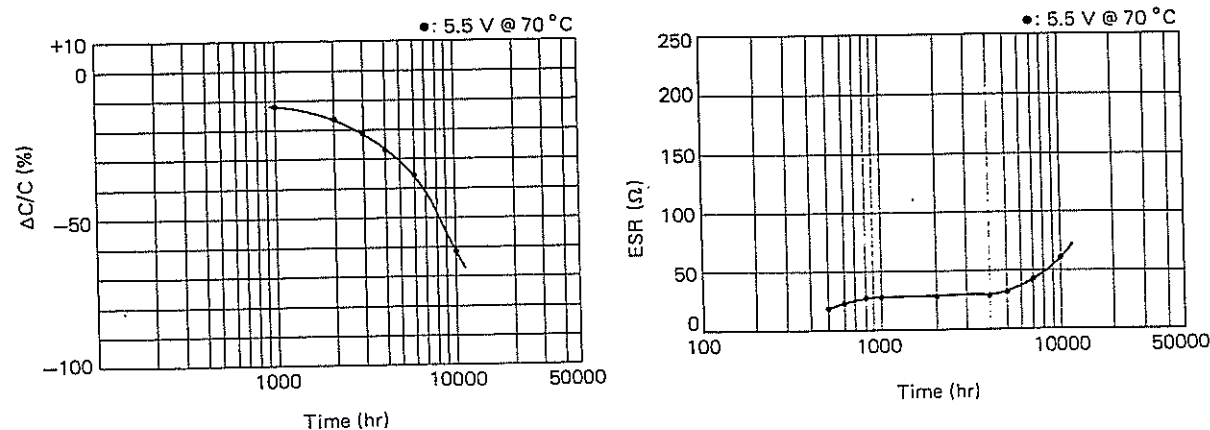


Fig. 11 Life Test Data (FYD0H474Z)

(3) Storage life at high/low temperature
Fig. 12, 13 and Fig. 14, 15 are typical storage life test data at 85 °C for 1,000 h and -40 °C for 500 h respectively.
The test conditions are more severe than NEC guarantee specification.

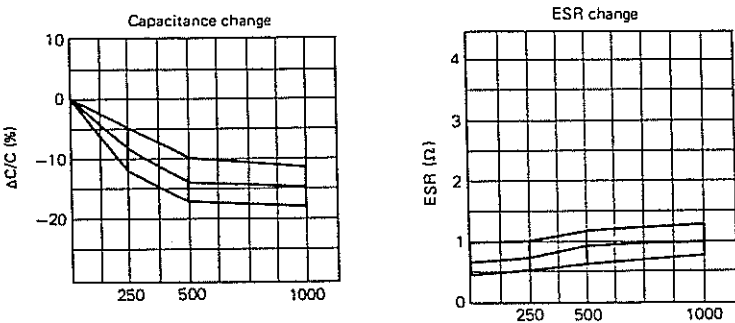


Fig. 12 Storage Life Test Data; at 85 °C (FA0H105Z)

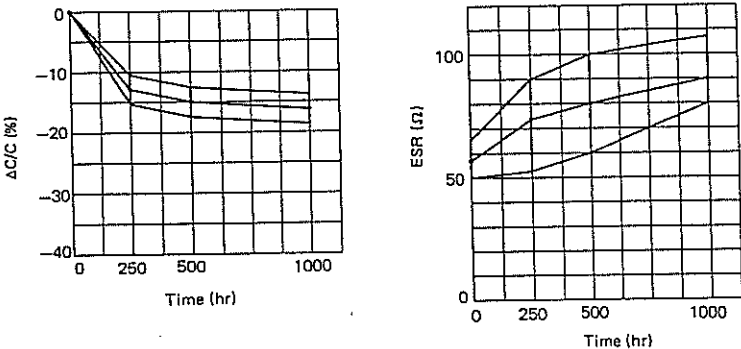


Fig. 13 Storage Life Test Data; at 85 °C (FYH0H473Z)

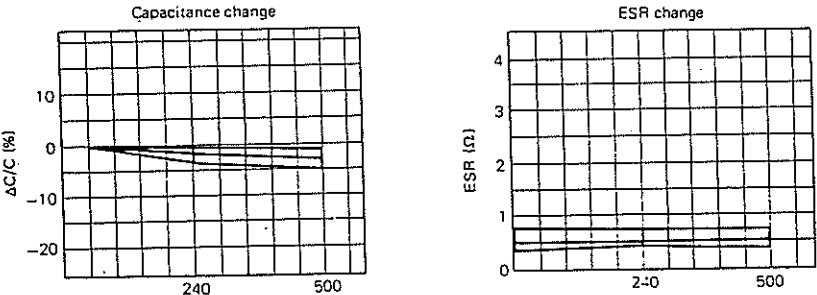


Fig. 14 Storage Life Test Data; at -40 °C (FA0H105Z)

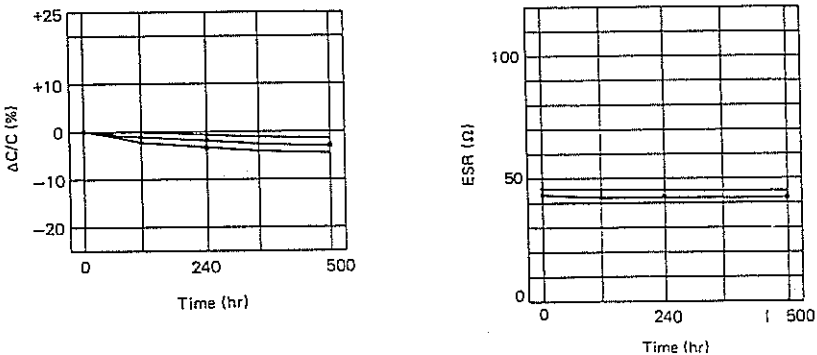


Fig. 15 Storage Life Test Data; at -40 °C (FYH04H473Z)

(4) Moisture Resistance

Fig. 16 and Fig. 17 are Moisture Resistance test data at 40 °C, 90 to 95 % relative humidity, with no voltage applied, for 500 h.

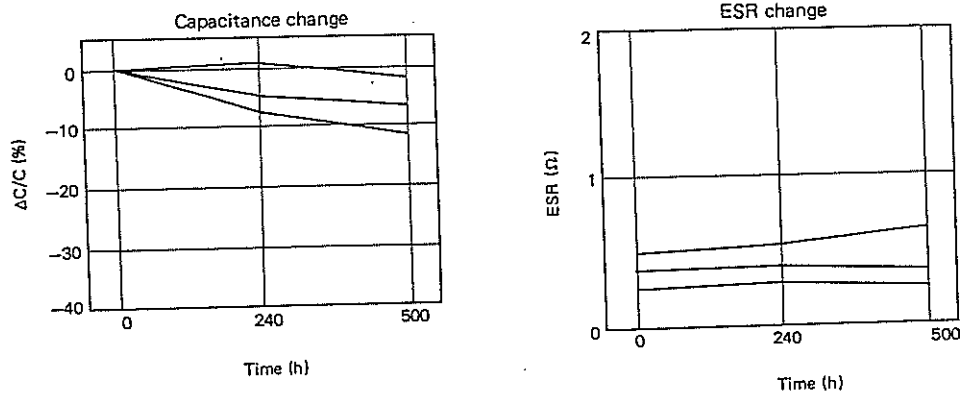


Fig. 16 Moisture Resistance Test Data (FA0H105Z)

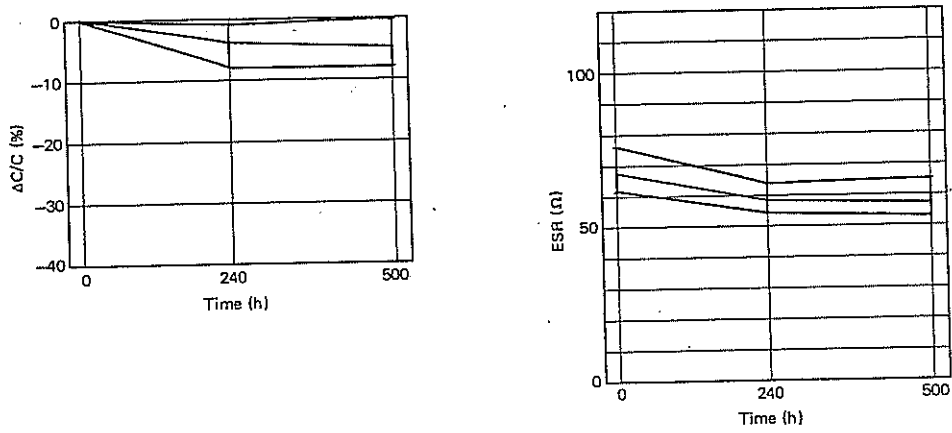


Fig. 17 Moisture Resistance Test Data (FYD0H473Z)

4.5 Environmental Test Data

The following information is reference data and not guaranteed specifications.

(1) Temperature characteristics

Fig. 18 and Fig. 19 show typical changes with temperature in capacitance and ESR over the operating temperature range of -25 °C to +70 °C.

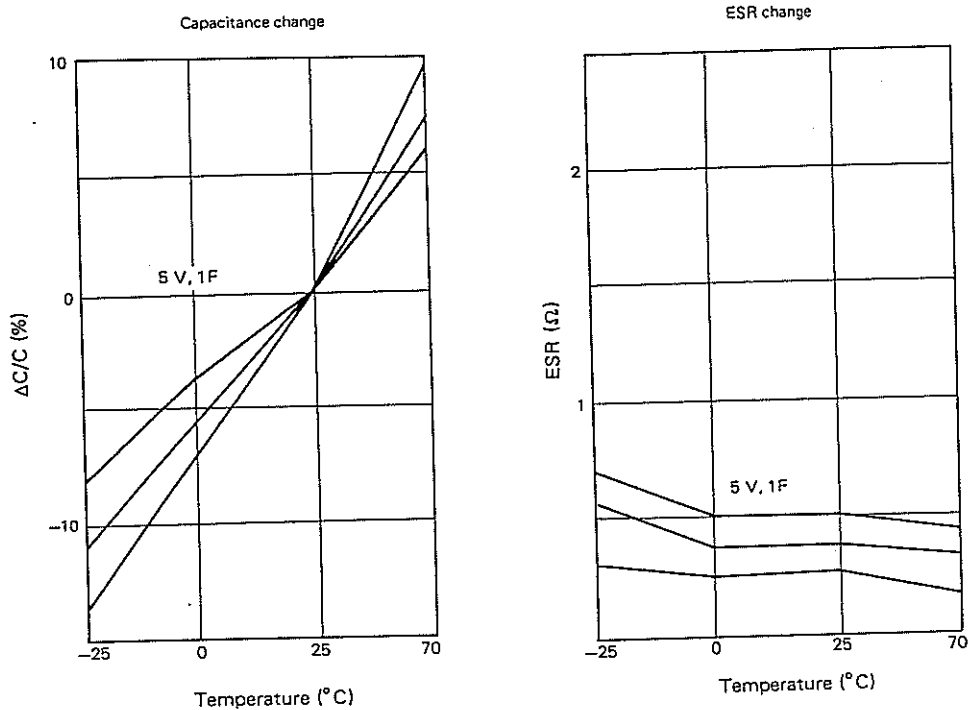


Fig. 18 Temperature Characteristics (FA0H105Z)

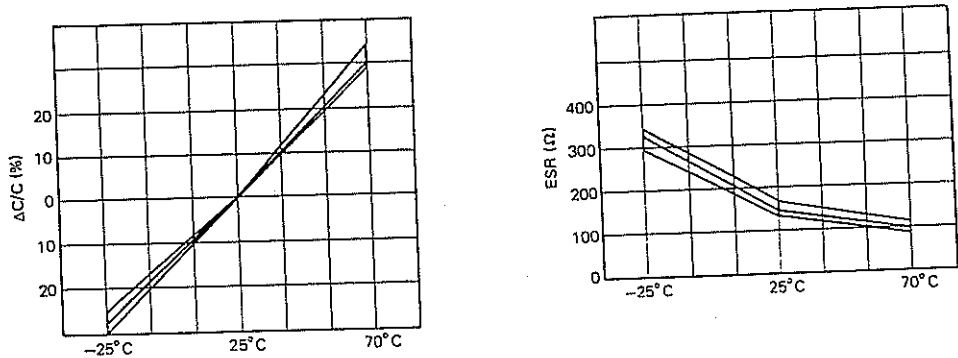


Fig. 19 Temperature characteristics (FYD0H473Z)

(2) Thermal cycling test

Capacitance and ESR of **SUPERCAP** shall be within the initial requirements after 5 thermal cycles, which consists of 30 min. each successive exposure at -25°C , $+25^{\circ}\text{C}$, $+70^{\circ}\text{C}$ and $+25^{\circ}\text{C}$ per each cycle. **Fig. 20** and **Fig. 21** typically show more extensive test result from 10 cycles of -30°C to $+85^{\circ}\text{C}$ (test A) and 10 cycles of -30°C to $+100^{\circ}\text{C}$ (test B). No degradation was found in these tests.

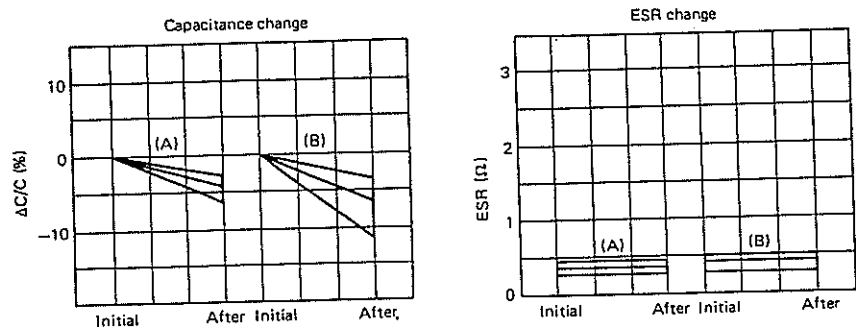


Fig. 20 Thermal Cycling Test Data; 10 Cycles (FA0H105Z)

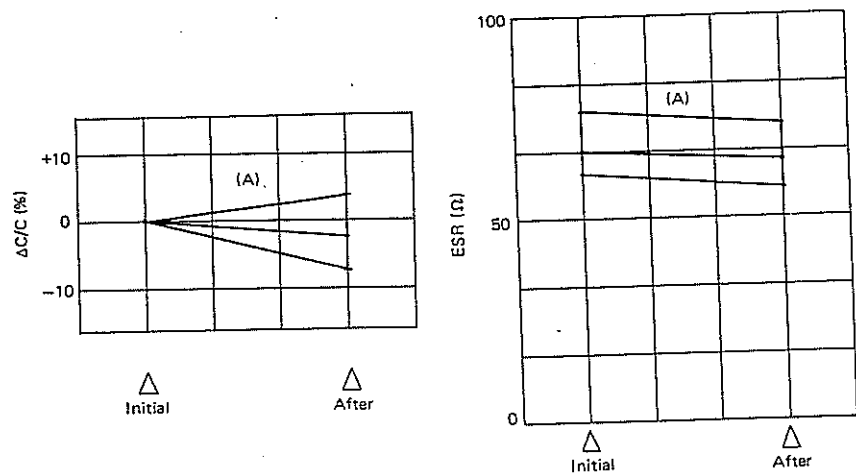


Fig. 21 Thermal Cycling Test Data; 10 Cycles (FYD0H473Z)

(3) Vibration/Mechanical shock test

Typical change in capacitance and ESR after the tests are shown in Fig. 22, 23 and Fig. 24.

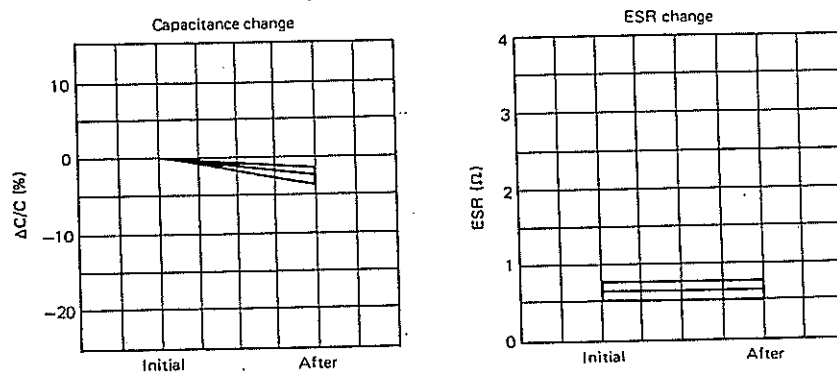


Fig. 22 Vibration Test; 10 Hz to 55 Hz, 6 Hours (FA0H105Z)

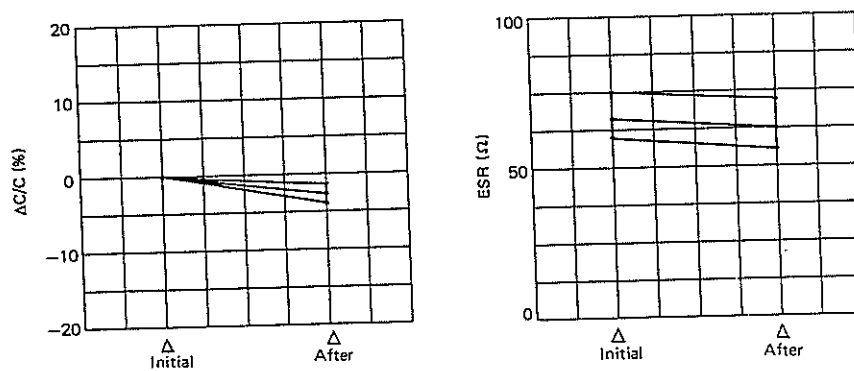


Fig. 23 Vibration Test; 10 Hz to 55 Hz, 6 Hours (FYD0H473Z)

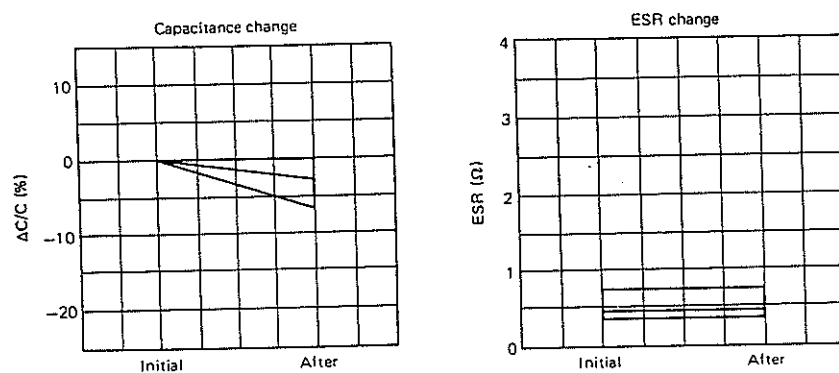


Fig. 24 Mechanical Shock Test; MIL-STD-202E, Method 205 (FA0H105Z)

5. APPLICATION NOTES

5.1 Major Power Interruptions

Major power interruptions are illustrated in the table below. Among them, the most frequent power outages range less than a few minutes.

Major Power Interruptions

TIME PERIOD	CAUSES OF INTERRUPTION	FREQUENCY
Second(s)	<ul style="list-style-type: none">• Service interruption (Natural phenomena, trouble in power system)• Disconnect (Accidental)• Main Power Voltage Drop• Intermittent contact	Very frequent
Minute(s)	<ul style="list-style-type: none">• Battery replacement• Disconnect (Accidental)• Service interruption (Natural phenomena, construction)• Removal of apparatus (Indoor)	Frequent
Hour(s)	<ul style="list-style-type: none">• Service interruption (Natural phenomena, construction)• Removal of the apparatus (Indoor)• Trouble repair of apparatus• Car battery replacement	Infrequent
Day(s)	<ul style="list-style-type: none">• House-moving (long distance)• Weekends	Infrequent Frequent
Week(s)	<ul style="list-style-type: none">• Stoppage of power supply during holidays and summer vacations	1 ~ 2 times/year

5.2 Power Backup Design

Certain parameters must be considered in defining the type of energy source required for standby power. These include the following:

- Voltage level (minimum to retain memory or standby conditions)
- Current requirements (minimum to retain memory or standby conditions)
- Duration of power outages expected (or time on "Standby power")
- Shelf and operational life expected (or the needs for maintenance)
- Storage and operating range, and other environmental considerations
- Device size, reliability and safety, plus consideration to simple P.C. board assembly
- Cost (Not only device cost, but overall installation cost for related circuits, assembly, etc.)

Once these parameters are well defined, in many instances, it will become apparent that **SUPERCAP** provides a reliable, maintenance free, and cost effective standby power source.

It is suggested that FA, FE, FS, FR, FY, and FM Series **SUPERCAP** should be selectively used as follows:
(See Fig. 25)

FA and FE Series: Medium to large current (50 milliamperes or more) for short time backup applications.

FS Series: Small current (less than 50 milliamperes) for several minutes backup applications.

FR, FY, and FM Series: Very small current (less than 500 μA) for several weeks backup applications.

This selection guideline is recommended due to the difference of max ESR specifications. (See Fig. 26 (a), (b), 27, 28 for detailed backup time capability.)

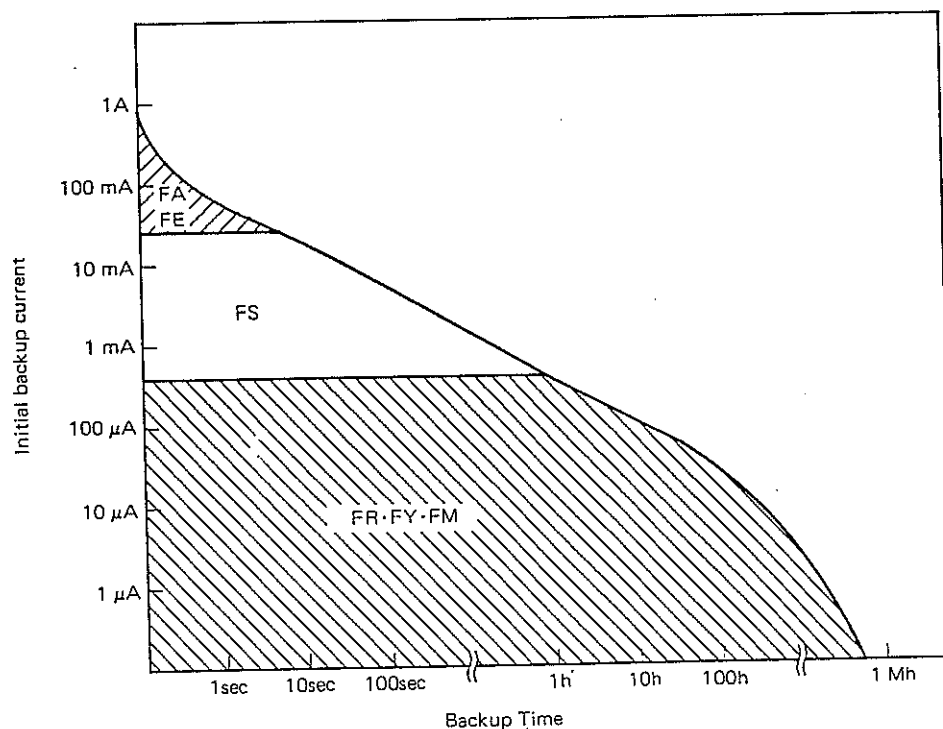


Fig. 25

5.3 Backup Time Capability

Relation between backup current and backup time period is given in Fig. 26, Fig. 27 and Fig. 28.

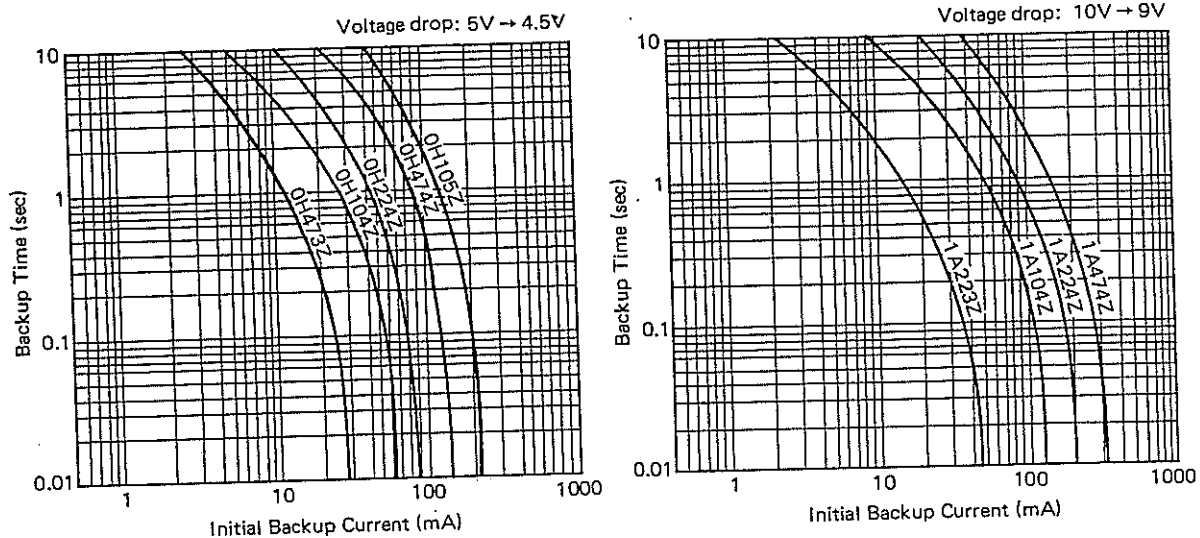


Fig. 26 (a), (b) FA and FE Series Typical Backup Time Capability (for Microcomputers)

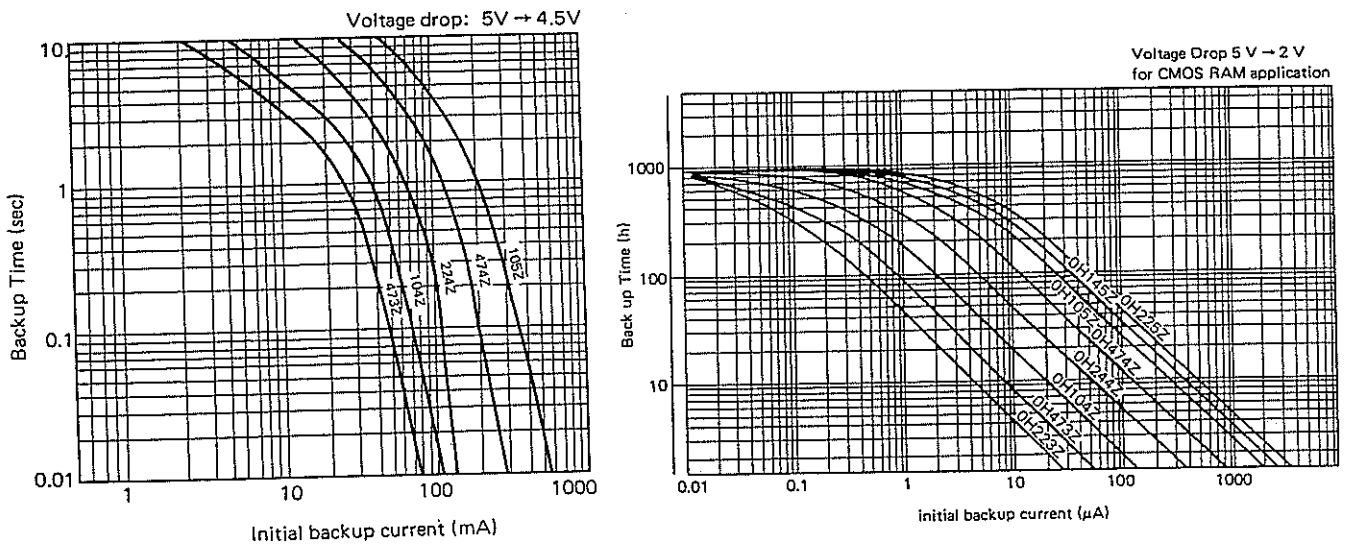
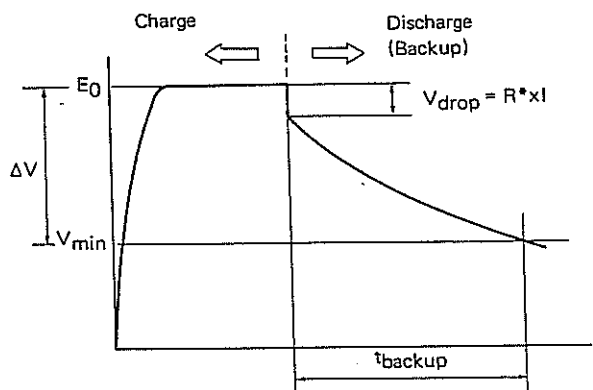


**Fig. 27 FS Series Typical Backup Time Capability
(for CMOS Microcomputers)**

Fig. 28 FR, FY and FM Series Typical Backup Time Capability (for CMOS RAMs)

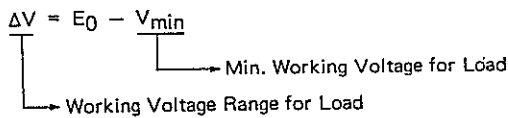
5.4 Capacitance Selection Method

- (1) To obtain the capacitance for the initial backup current from several μA to several hundred μA , use Fig. 29 to Fig. 32 of FY, FR and FM series.
Discharge characteristics on page 25 to 28.
- (2) For the backup current from several hundred to 1 A, use the following Formula (1) below to determine the capacitance.
This is applicable for FA, FE and FS series.



$$\text{Cap} = \frac{I \times t_{\text{backup}}}{\Delta V - V_{\text{drop}}} \quad [\text{F}] - (1)$$

where



- I : Backup current [A]
- t_{backup} : Backup time [sec]
- E₀ : Charged voltage [V]
- V_{drop} = R × I [V]

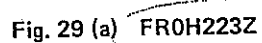
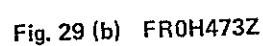
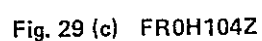
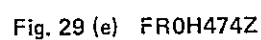
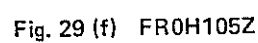
* The following is value for R.

Catalog NBR	R (TYP.) (Ω)
FA0H473Z	13
FA0H104Z	4
FA0H224Z	3
FA0H474Z	2
FA0H105Z	1
FA1A223Z	20
FA1A104Z	4
FA1A224Z	1.7
FA1A474Z	1.2

FE's value is equal to FA's.

Catalog NBR	R (TYP.) (Ω)
FS0H473Z	9
FS0H104Z	5
FS0H224Z	7
FS0H474Z	3.5
FS0H105Z	2

- FR Series



● FYH Series

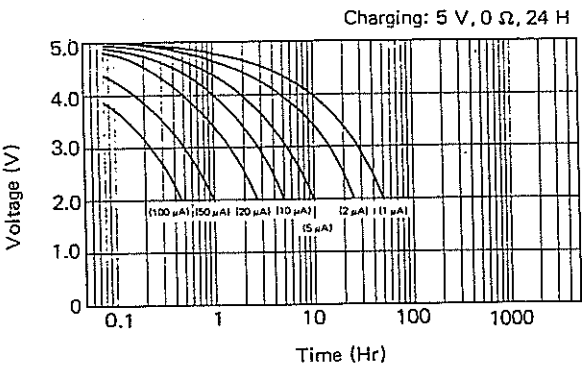


Fig. 30 (a) FYH0H223Z ,022

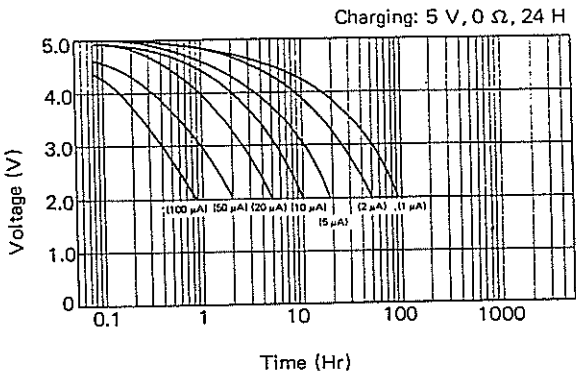


Fig. 30 (b) FYH0H473Z

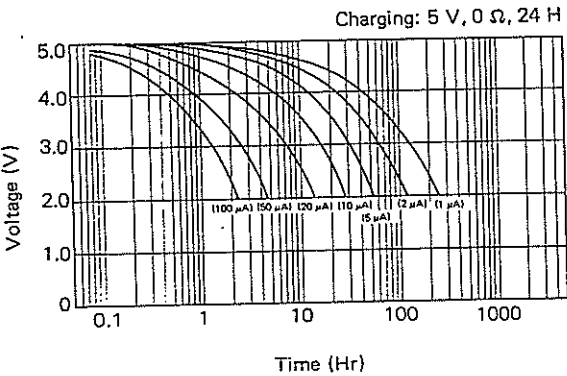


Fig. 30 (c) FYH0H104Z

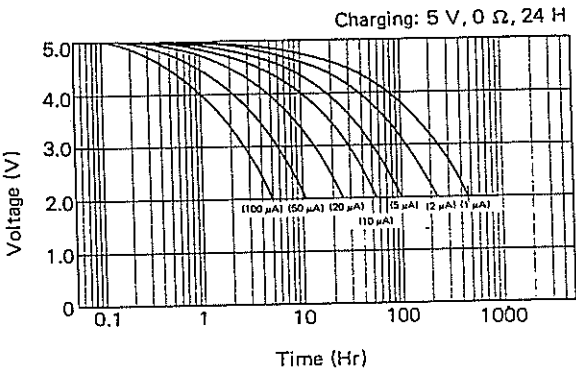


Fig. 30 (d) FYH0H224Z ,22
450

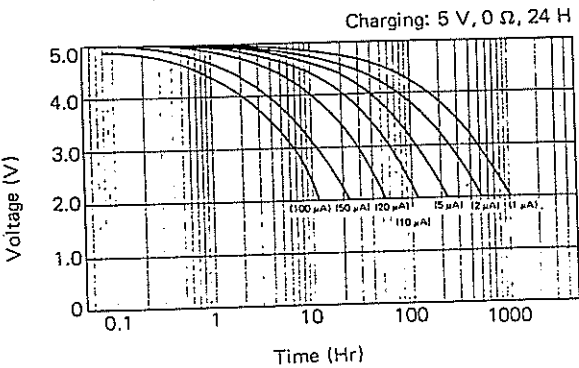


Fig. 30 (e) FYH0H474Z

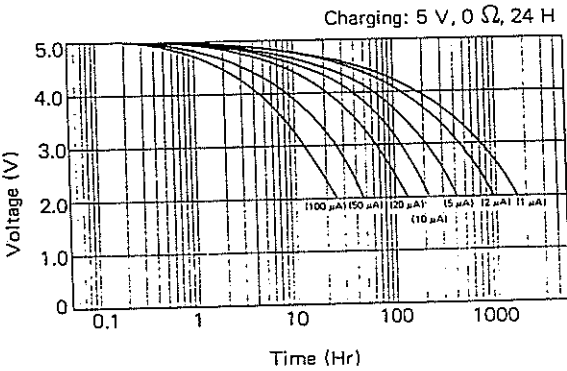


Fig. 30 (f) FYH0H105Z

• FYD Series

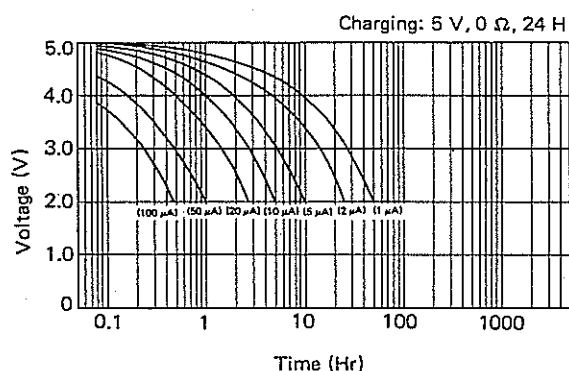


Fig. 31 (a) FYD0H223Z

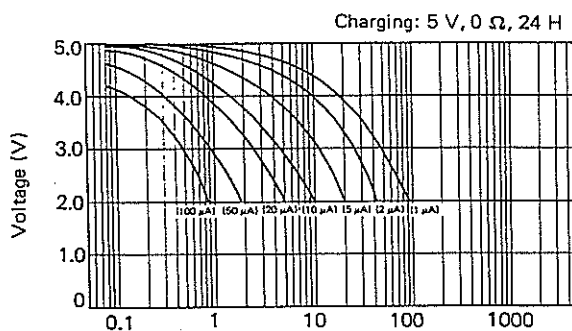


Fig. 31 (b) FYD0H473Z

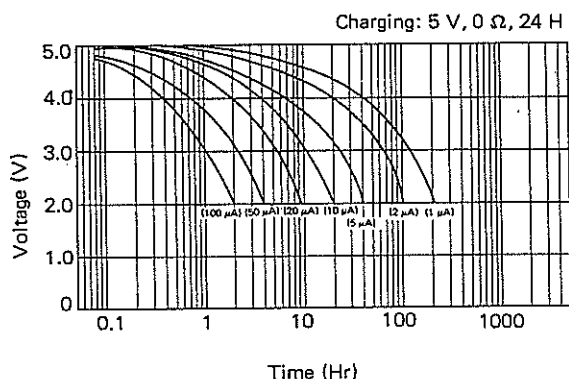


Fig. 31 (c) FYD0H105Z

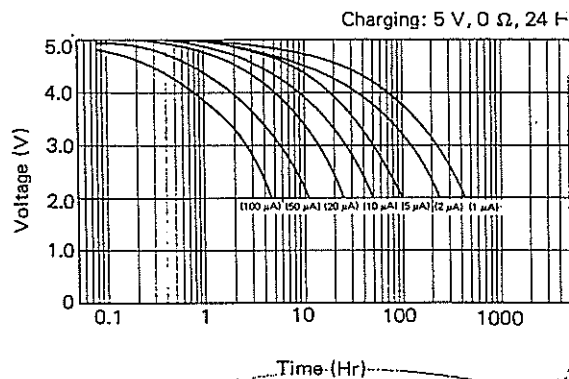


Fig. 31 (d) FYD0H224Z

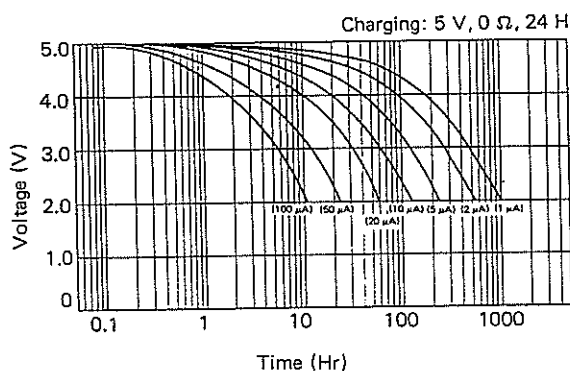


Fig. 31 (e) FYD0H474Z

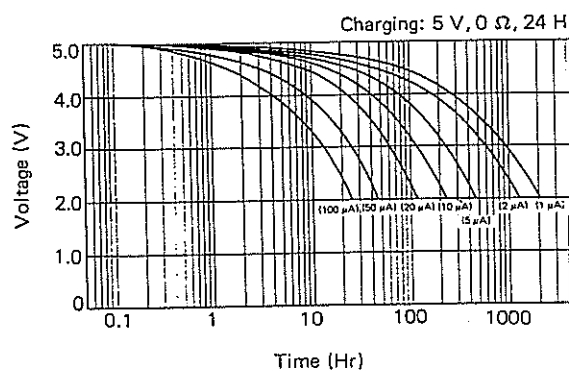


Fig. 31 (f) FYD0H105Z

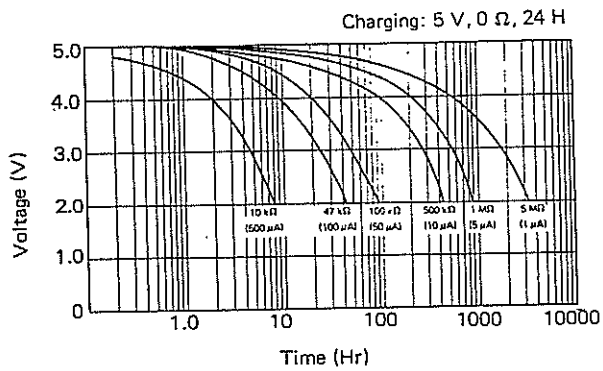


Fig. 31 (g) FYD0H225Z

● FM Series

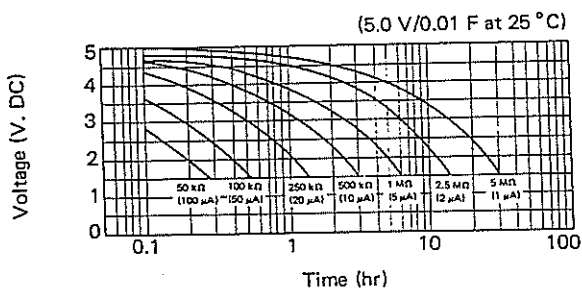


Fig. 32 (a) FM0H103Z

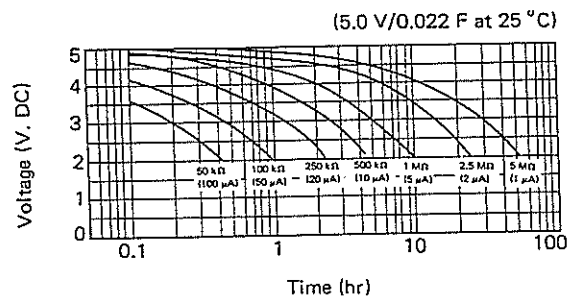


Fig. 32 (b) FM0H223Z

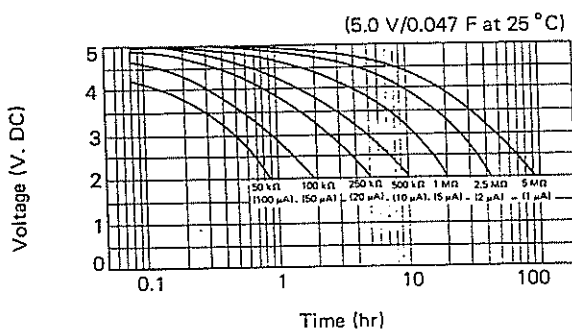


Fig. 32 (c) FM0H473Z

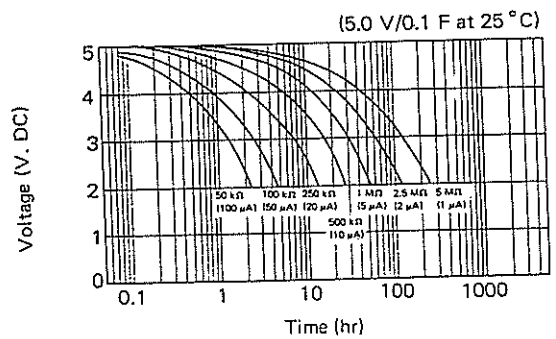


Fig. 32 (d) FM0H104Z

5.5 Backup Circuit

Basic circuit diagram in use of the SUPERCAP is shown in Fig. 33.

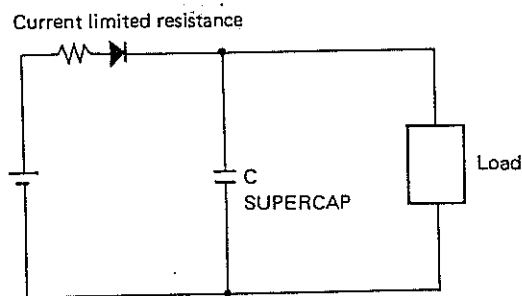


Fig. 33 SUPERCAP Basic Circuit

The diode shall be placed to isolate the primary power supply from the SUPERCAP during power interruption.

The backup time capability of the SUPERCAP depends on the current magnitude of the load circuit. For the purpose of retaining data during power outages, it is suggested that SUPERCAP should be placed as close as possible to CMOS RAMs or microcomputers, then the stored charges in the SUPERCAP will be most effectively utilized.

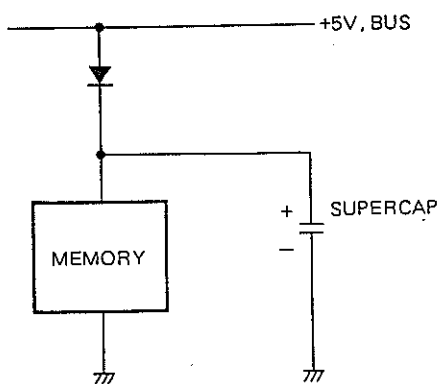


Fig. 34 Possible Backup Configuration (A)

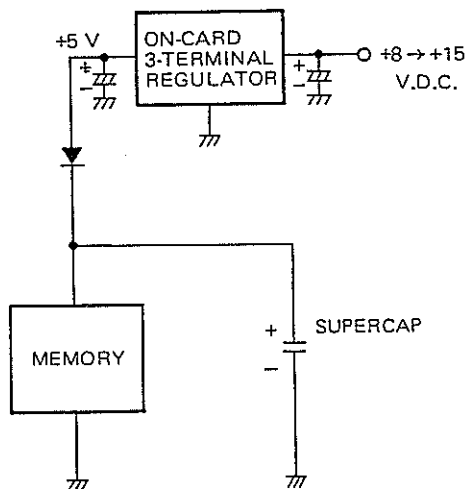
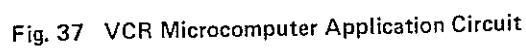


Fig. 35 Possible Backup Configuration (B)

Fig. 36 Memory Backup Circuit Diagram



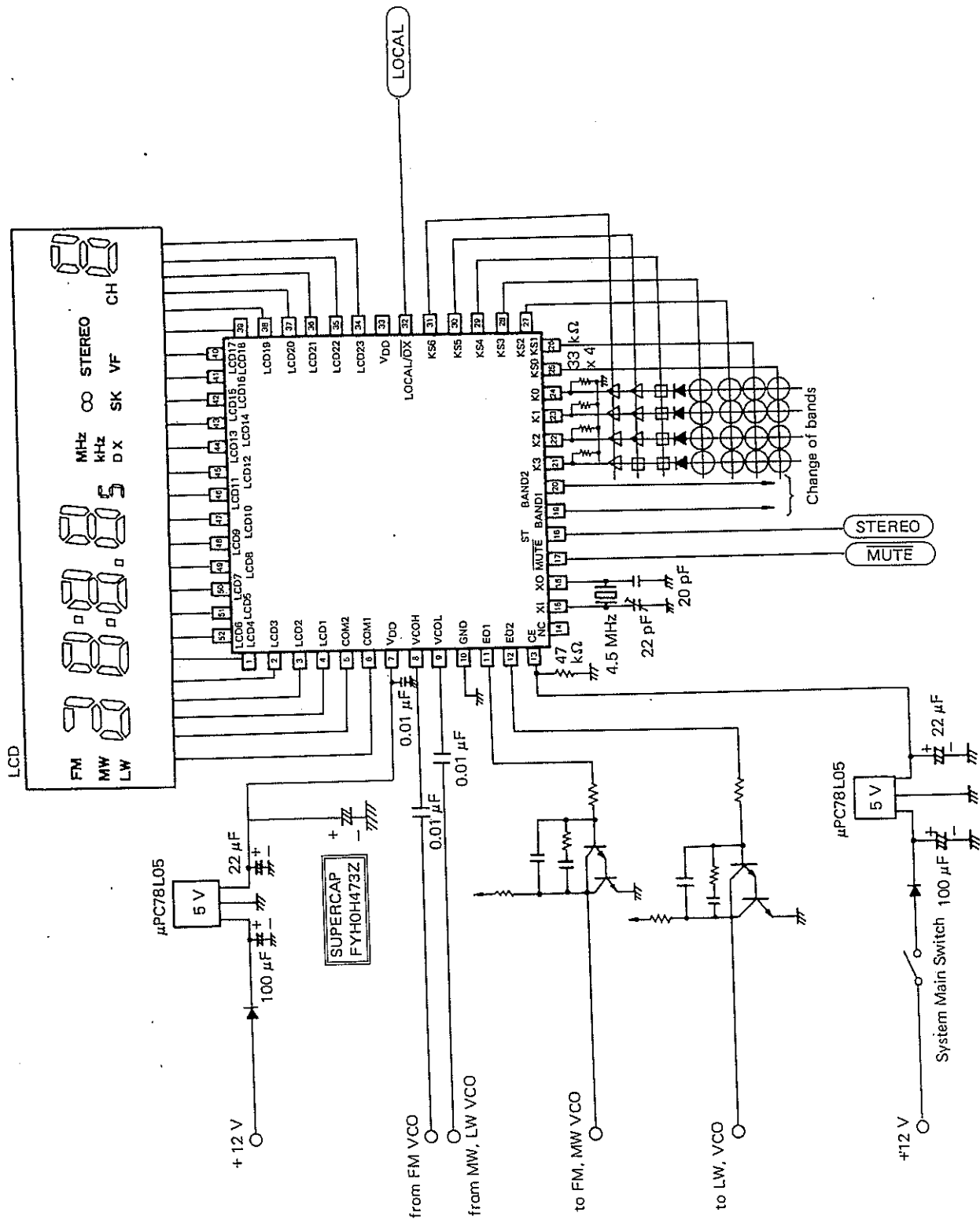


Fig. 38 PLL Frequency Synthesizer/Controller for LW, MW, FM Digital Tuner Application Circuit

5.6 Typical Applications

Typical applications categorized by the functions and the magnitude of backup current required are shown in the table below.

Typical Applications for SUPERCAP

FUNCTIONS	BACKUP CURRENT	APPLICATIONS	EQUIPMENT	ADEQUATE SERIES
Large current supply	Up to 1 A	Actuator applications (Large current in a short period)	Actuators Relay/Solenoid starter Igniters	FA and FE Series
		Primary power supply for LED displays, toys, electric buzzer etc.	Handheld toys Displays, Smoke detectors, Alarm devices, Emergency display	
Medium capacity power supply	Up to 50 mA	Secondary power source for undesirable voltage drops	Car radio back-up at the engine start, etc.	FS Series 3.5 V-6.5 V Series (FSH)
		Motor Start	VCR, Video disk Record player	
Power backup for primary power outages	Less than 500 μ A	CMOS Microcomputers	Phones (Memory dial, Auto-answering) Electric cash registers Electric typewriters Computer terminals Automatic measuring instruments etc.	FY Series (FYD Type) (FYH Type) (FYL Type) 3.5 V-6.5 V Series (FYD) FM Series
		CMOS RAMs ICs for Clocks	Digital tuning audio system (LW-MW-FM Radio, Car Radio, Stereo, etc.) Programmable consumer electronic products (VCR, Microwave oven, Games, etc.)	
		<ul style="list-style-type: none">CMOS RAMs ICs for ClocksHigh operating temperature (85 °C)	Measuring instruments Automatic control Communications Car	FR Series
(Other Possible Applications) Programmable thermostat, Medical Electronics, Copiers, Vending machines, Automatic Electricity Counters, Traffic signals, Taxi Meters, Fuel Management Systems, Process Monitoring or Control, Satellite Communications, Military Electronics, Avionics, Intercom, Portable "Battery" Operated Equipment, Fare collection System, POS Terminals, Mail Sorters, Scale, Flow metering, Electronic Slot Machines, Water Heat Controllers.				

Typical test results for the actual backup time capability are listed in the table below.

SUPERCAP BACKUP TIME (TYPICAL TEST RESULTS at 25 °C)

NEC ICs (Description)	Actual current	SUPERCAP tested	Backup Time (Test Results)
μPD43256AC-LL (256K bit CMOS RAM)	1.2 μA or less	FYH0H473Z	50 hours
μPD1708C (CMOS LSI for PLL Tuner)	10 μA or less (without clock)	FYH0H224Z	40 hours
μPD75216A (CMOS Microcomputer)	8 μA or less (stop mode)	FYH0H473Z	7 hours

5.7 Series/Parallel Connections

When higher rated voltage or greater capacitance (i.e., longer backup time) is required, it can be obtained by connecting **SUPERCAP** in series or in parallel respectively.

(1) Series Connection

The voltage needs to be equally distributed to the capacitors. Practically, the same production lot number capacitors shall "only" be connected in series.

Series connection of different **SUPERCAP** part numbers may cause imbalanced voltage distribution to each capacitors, resulting that excess voltage may be kept applied to a specific capacitor.

(2) Parallel Connection

No major caution is suggested. Parallel connection with different part number capacitors is allowable.

5.8 General Hints and Suggestions

- (1) Due to relatively high ESR, it is not recommended to apply **SUPERCAP** in AC or filtering applications.
- (2) Do not apply the voltage beyond the maximum working voltage.
- (3) Do not disassemble the capacitor, as dilute sulfuric acid is moisturized to the activated carbon.
- (4) Although **SUPERCAP** has no polarity, it is suggested to take the longer lead as a negative porality, since the longer lead is electrically connected to the metal can case.
- (5) Grinding leads will decrease solderability.
- (6) At the cleaning process after P.C board soldering, **SUPERCAP** should not be completely dipped into the solvent. Ultrasonic cleaning should also be avoided.
Solvent immersion into the **SUPERCAP** may leave undesirable solder flux residue inside the capacitors, resulting in possible ESR increase. Solvent shower or partial dipping to solvent is allowable.

6. PRINCIPLE AND STRUCTURE

6.1 Operating Principle

At every interface, an array of charged particles and induced charges is thought to exist. This array is known as an electric double layer. The large capacitance of an electric double layer capacitor arises from the charge stored at the interface by the changing electric field between two available phases. In the **SUPERCAP**, one phase is the activated carbon particle. The other phase is sulfuric acid solution, as an ionically conducting electrolyte.

The charge distribution at the interface is illustrated in **Fig. 39 (a)**, **Fig. 39 (b)** shows that with electric field applied.

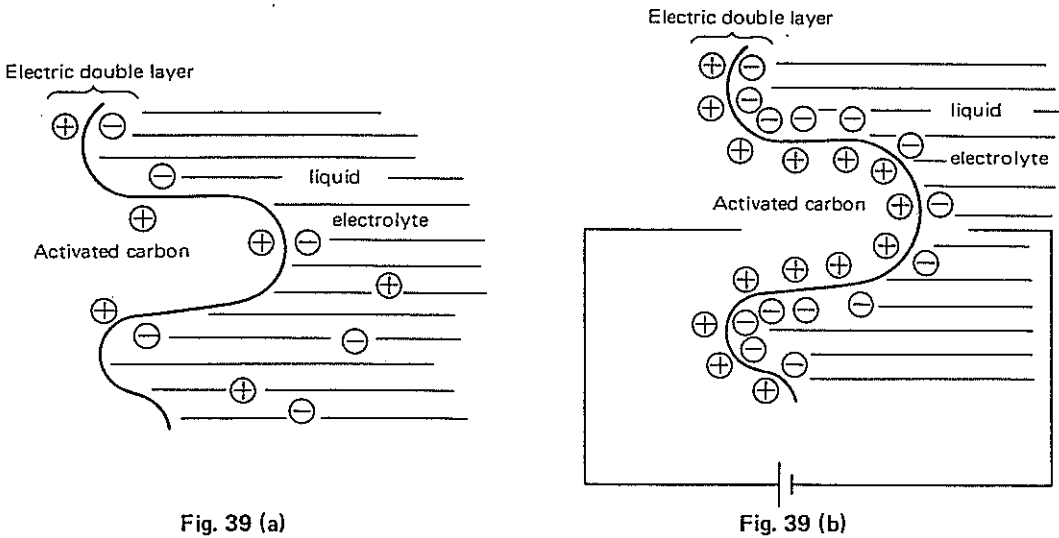


Fig. 39 (a)

Fig. 39 (b)

Fig. 39 Electric Double Layer

The basic model of **SUPERCAP** is shown in **Fig. 40**.

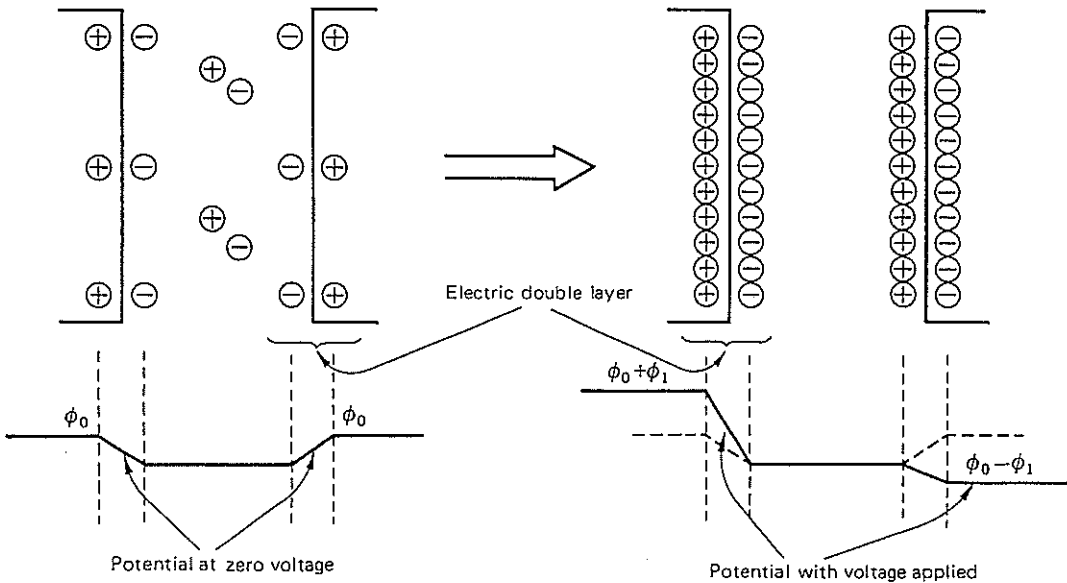


Fig. 40 Basic Model of SUPERCAP

The charges per unit area 'N' is calculated by the formula (4), where 'd' represents a dielectric constant, δ signifies the distance from a solid surface to the center of ions and ' ϕ ' represents the electric potential of double layer.

$$N = \frac{d}{4 \pi \delta} \times \phi \dots\dots\dots (4)$$

In Fig. 40 if ' ϕ ' at the time of no-voltage is ' ϕ_0 ' then, ' N_0 ' is shown in formula (5).

$$N_0 = \frac{d}{4 \pi \delta} \times \phi_0 \dots\dots\dots (5)$$

When the external electric field is applied, electrical charges are accumulated at the interface. As a result, ' ϕ_0 ' becomes ' ϕ_1 ' and the charges increase to ' N_1 ' as shown in formula (6).

$$N_1 = \frac{d}{4 \pi \delta} \times (2\phi_1 - \phi_0) \dots\dots\dots (6)$$

In other words;

$$N_1 = 2N_0 \frac{\phi_1}{\phi_0} \quad (\phi_1 \gg \phi_0) \dots\dots\dots (7)$$

Since the order of ϕ_0 is a few milli-volt, the external voltage (a few volt) can dramatically increase the charges. This is one of the reasons why **SUPERCAP** can achieve extremely high capacitance in a small package.

6.2 Product Structure

The cross section of a unit cell is shown in Fig. 41. The activated carbon particles moisturized (not in real liquid state) by diluted sulfuric acid electrolyte are segregated by a porous, ion permeable separator, and packaged inside by electroconductive rubber and nonconductive rubber gasket.

The unit cell is hermetically sealed by the electroconductive rubber and nonconductive rubber gasket, both of which are vulcanized together at the same time. No adhesive glue is used for the seal.

The breakdown voltage of the unit cell can be as low as 1.2 volt. This is the decomposition voltage of aqueous electrolyte solution. Therefore, several unit cells are stacked in series to get the required rated voltage.

Fig. 42 and 43 illustrate the cross section of the **SUPERCAP**.

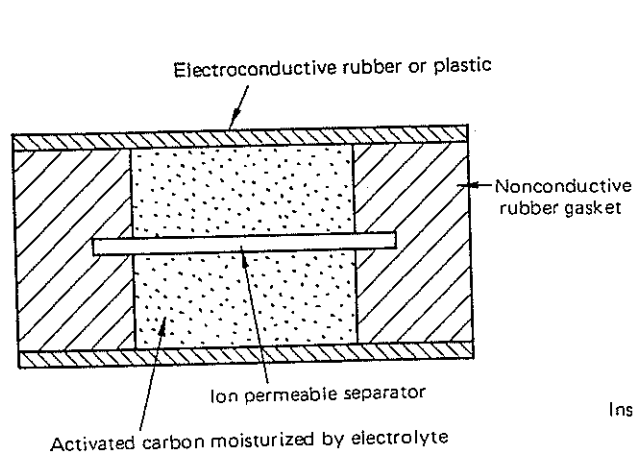


Fig. 41 SUPERCAP Unit Cell

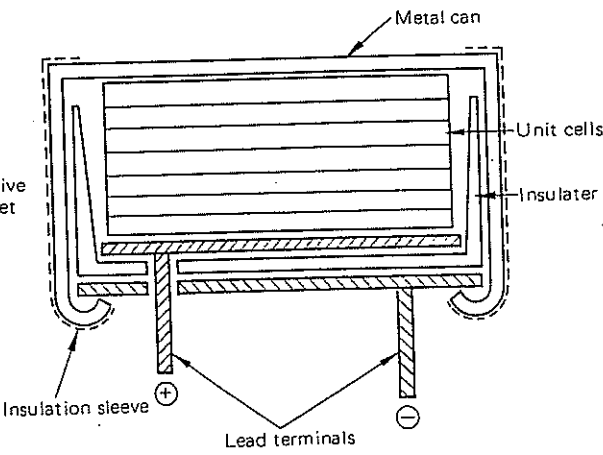


Fig. 42 Cross Section of the Can Case Type

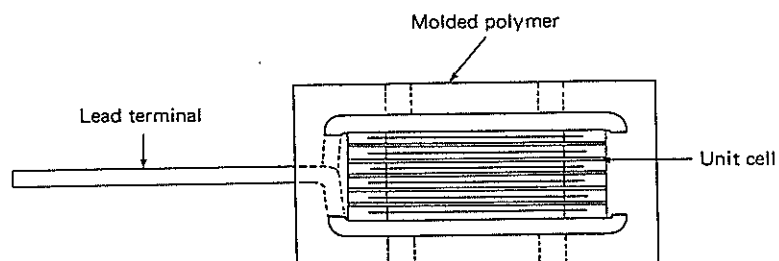
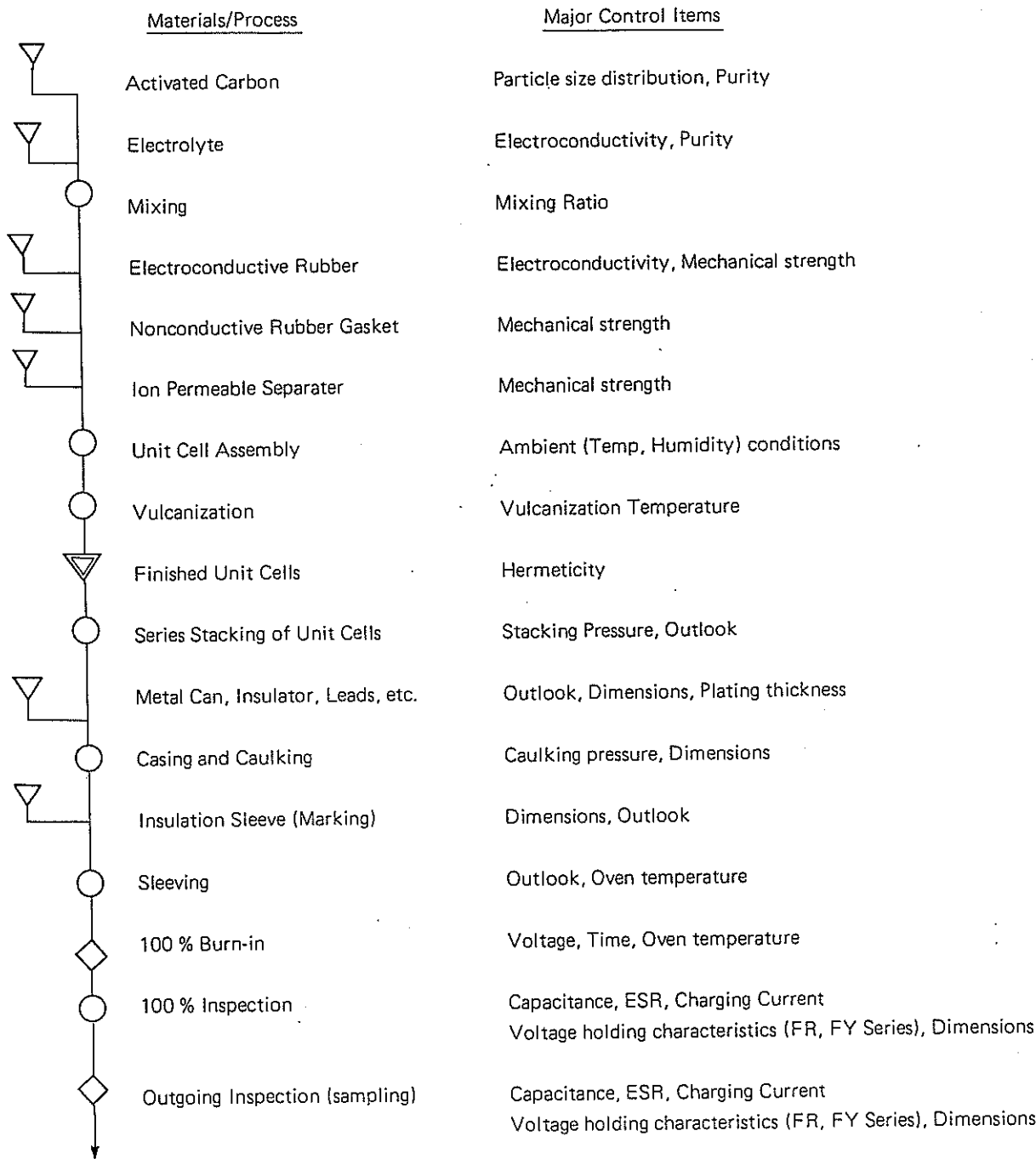


Fig. 43 Cross Section of the Molded Type (FM Series)

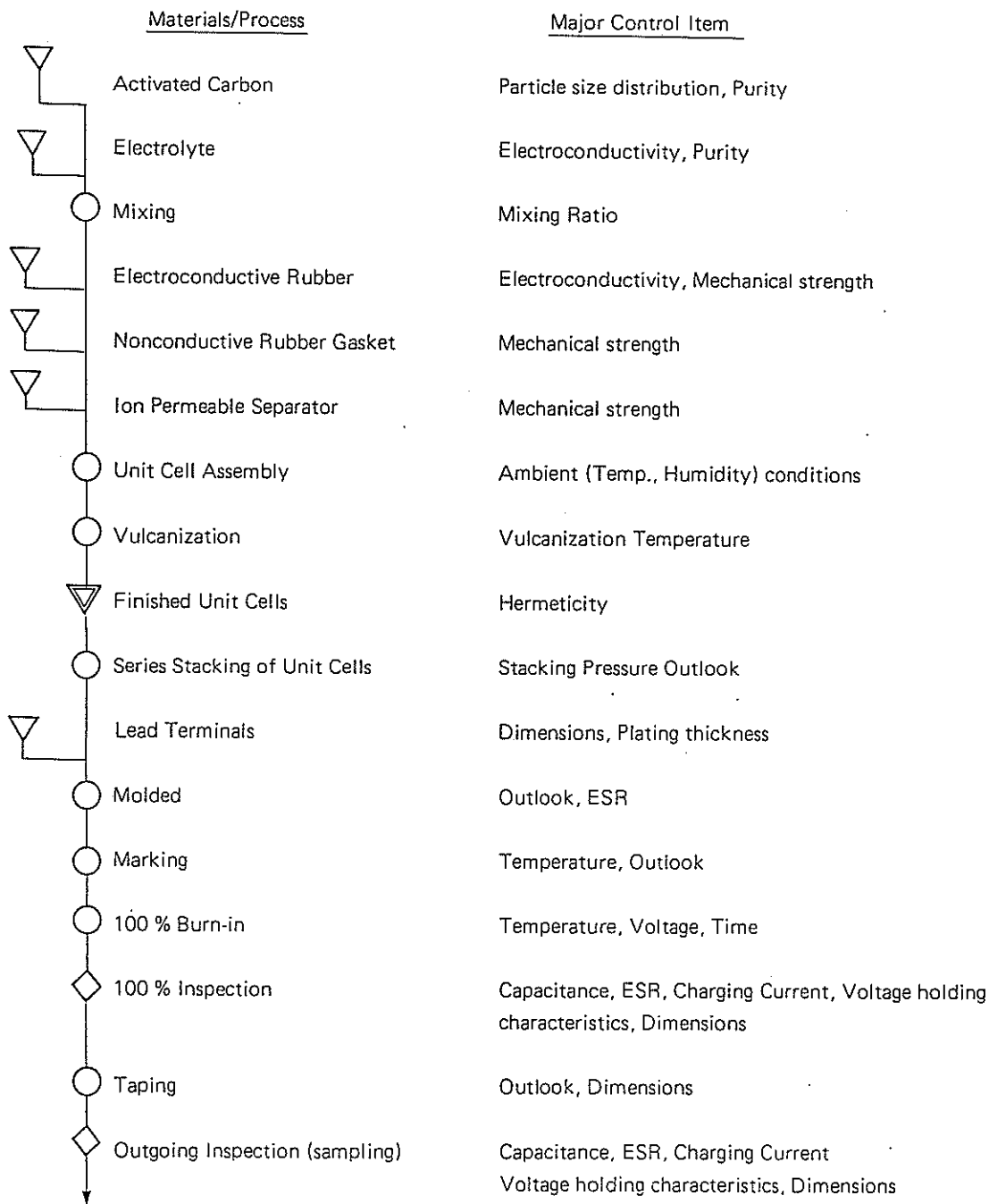
[Note] Activated carbon is specially processed carbon to achieve very high porosity, so that its surface area is greatly increased. This feature is widely utilized as an odor absorption material. **SUPERCAP** also utilizes its wide surface area for the high capacitance electrode.

6.3 Manufacturing Process and Quality Control

• Can Case Type



● Molded Type (FM Series)





#216
2/8/95
T.M.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Reasoner *et al.* :
Serial No. (to be assigned) : Date: 10/05/94
Filed: (herewith) : Art Unit: (to be assigned)
For: System And Method For : Examiner: (to be assigned)
RAM Power and Data :
Backup Utilizing A :
Capacitor And ROM :

APPOINTMENT OF ASSOCIATE ATTORNEY

The Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

The undersigned attorney, who has been appointed as an attorney in the Combined Declaration and Power of Attorney for the above-identified application, hereby appoints Robert Greene Sterne, Esq. (Registration No. 28,912) and Edward J. Kessler, Esq. (Registration No. 25,688), of Sterne, Kessler, Goldstein & Fox, 1100 New York Avenue, NW, Washington, D.C. 20036, (202) 371-2600 his associate attorneys to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith.

Respectfully submitted,

By: William W. Cochran II
William W. Cochran II
Registration No. 26,652
Telephone No.: (303) 229-7239

HEWLETT-PACKARD COMPANY
Legal Department, 20B0
P.O. Box 10301
Palo Alto, California 94303-0890



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
---------------	-------------	----------------------	---------------------

08/322,808 10/13/94 REASONER

25M1/0405

RECORDS MANAGER
LEGAL DEPARTMENT 2080
HEWLETT-PACKARD COMPANY
P O BOX 10301
PALO ALTO CA 94303-0890

K	10944581
EXAMINER	
YOO, D	
ART UNIT	PAPER NUMBER

2511
DATE MAILED: 04/05/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire _____ month(s), 30 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- | | |
|---|---|
| 1. ☐ Notice of References Cited by Examiner, PTO-892. | 2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948. |
| 3. ☐ Notice of Art Cited by Applicant, PTO-1449. | 4. ☐ Notice of Informal Patent Application, PTO-152. |
| 5. ☐ Information on How to Effect Drawing Changes, PTO-1474. | 6. ☐ _____ |

Part II SUMMARY OF ACTION

1. ☒ Claims 1-13 are pending in the application.
Of the above, claims nine are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☐ Claims _____ are rejected.
5. ☐ Claims _____ are objected to.
6. ☒ Claims 1-13 are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

Serial Number: 322,808

Art Unit: 2511

Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 1-4, drawn to a random access memory backup system utilizing a RAM, a capacitor, a read only memory, and processing means, classified in Class 365, subclass 149.

II. Claims 5-13, drawn to a method for backing up utilizing the steps of determining, backing up, and restoring, classified in Class 365, subclass 226.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I (claim 1-4) and Group II (claims 5-13) are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (M.P.E.P. § 806.05(h)). In the instant case the process as claimed can be practiced with another materially different product such as one not requiring processing means. Alternatively, the product as claimed can be used in a materially different process such as one requiring a step related to processing means.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by

Serial Number: 322,808

-3-

Art Unit: 2511

their different classification restriction for examination purposes as indicated is proper.

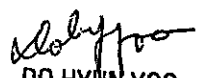
Applicant is advised that the response to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 C.F.R. § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 C.F.R. § 1.48(b) and by the fee required under 37 C.F.R. § 1.17(h).

Any inquiry concerning this communication should be directed to Do H. Yoo at telephone number (703) 308-4908.

Yoo/tj 047

March 30, 1995


DO HYUN YOO
PRIMARY EXAMINER
GROUP 2500



CA
2571

ROBERT GREENE STERNE
EDWARD J. KESSLER
JORGE A. GOLDSTEIN
SAMUEL L. FOX
DAVID K.S. CORNWELL
ROBERT W. ESMOND
TRACY-GENE G. DURKIN
MICHELE A. CIMBALA
MICHAEL B. RAY
ROBERT E. SOKOHL
WILLIAM C. ALLISON V
MICHAEL Q. LEE
EVELYN H. MCCONATHY
ERIC K. STEFFE
ANDREA G. REISTER
DANIEL N. YANNUZZI
BRADFORD G. ADDISON
CONO A. CARRANO*
G. KEVIN TOWNSEND*
JOHN M. COVERT*
ANNE BROWN
MICHELE A. VAN PATTEN*
LINDA E. ALCORN
BRADLEY J. OLSON

JAMES L. LEWIS*
OF COUNSEL

*BAR OTHER THAN D.C.

STERNE, KESSLER, GOLDSTEIN & FOX

ATTORNEYS AT LAW

SUITE 600

1100 NEW YORK AVENUE, N.W.
WASHINGTON, D.C. 20005-3934

(202) 371-2600

RECEIVED

MAY 11 1995

GROUP 2500

TELEFAX: (202) 371-2540

INTERNET: skgf@capcon.net

BALTIMORE

INNER HARBOR CENTER
EAST PRATT STREET, SUITE 800
BALTIMORE, MARYLAND 21202
(410) 659-7570

DONALD J. FEATHERSTONE
ROBERT A. MILLMAN
STEVEN R. LUDWIG
LAWRENCE B. BUGAISKY
RAZ E. FLESHNER
KAREN R. MARKOWICZ
DREW GRANSTON
GREGORY P. EINHORN
MICHAEL V. MESSINGER
DAVID C. ISAACSON

REGISTERED
PATENT AGENTS

WRITER'S DIRECT NUMBER:

(202) 371-2550

May 5, 1995

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: U.S. Utility Patent Application
Appl. No. 08/322,808; Filed: October 13, 1994
For: System And Method For RAM Power And Data Backup Utilizing A
Capacitor And ROM
Inventors: Reasoner *et al.*
Our Ref : 1094458

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Response to Restriction Requirement; and
2. Three Return Post Cards.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents and returned to our courier.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

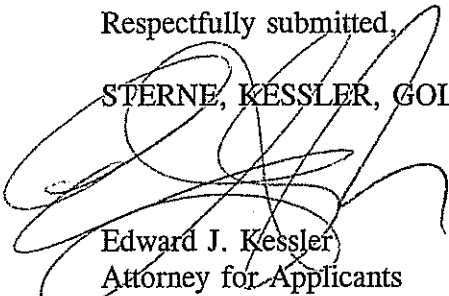
STERNE, KESSLER, GOLDSTEIN & FOX

Assistant Commissioner for Patents
May 5, 1995
Page 2

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to Hewlett Packard's Deposit Account No. 08-2025. A duplicate copy of this letter is enclosed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX



Edward J. Kessler
Attorney for Applicants
Registration No. 25,688

EJK:alw
C:\EJK\1245183.CVR



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#4
5/9/95
J Proctor

In re application of:

Reasoner *et al.*

Appl. No. 08/322,808

Filed: October 13, 1994

For: **System And Method For RAM
Power And Data Backup
Utilizing A Capacitor And ROM**

Art Unit: 2511

Examiner: Yoo, D.

Atty. Docket: 1094458

Response To Restriction Requirement

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated **April 5, 1995**, requesting an election of one invention to prosecute in the above-referenced patent application, Applicant hereby provisionally elects to prosecute the invention of Group I, represented by claims 1-4. This election is made without prejudice to or disclaimer of the other claims or inventions disclosed.

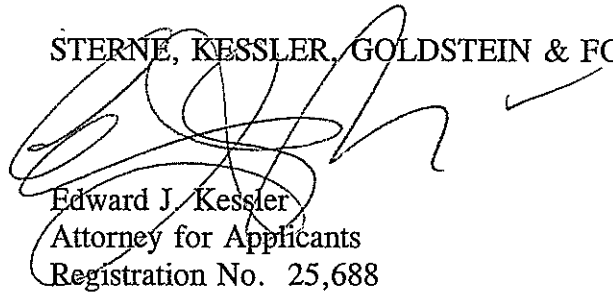
This election is made without traverse.

It is not believed that extensions of time are required, beyond those that may otherwise be provided for in accompanying documents. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of

time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor are hereby authorized to be charged to Hewlett Packard's Deposit Account No. 08-2025.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX



Edward J. Kessler
Attorney for Applicants
Registration No. 25,688

Date: 5/5/95

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005
(202) 371-2600

EJK:alw
C:\EJK\1245183.REQ



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
---------------	-------------	----------------------	---------------------

08/322,808 10/13/94 REASONER

K 10944581

EXAMINER

YOO, D

ART UNIT

PAPER NUMBER

2511

DATE MAILED:

05/24/95

RECORDS MANAGER
LEGAL DEPARTMENT 2080
HEWLETT-PACKARD COMPANY
P O BOX 10301
PALO ALTO CA 94303-0890

25M1/0524

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined

☒ Responsive to communication filed on 5-5-95

☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- ☒ Notice of References Cited by Examiner, PTO-892.
- ☒ Notice of Draftsman's Patent Drawing Review, PTO-948.
- ☒ Notice of Art Cited by Applicant, PTO-1449.
- ☐ Notice of Informal Patent Application, PTO-152.
- ☐ Information on How to Effect Drawing Changes, PTO-1474.
- ☐

Part II SUMMARY OF ACTION

- ☒ Claims 1-13 are pending in the application.
Of the above, claims 5-13 are withdrawn from consideration.
- ☐ Claims — have been cancelled.
- ☐ Claims — are allowed.
- ☒ Claims 1-4 are rejected.
- ☐ Claims — are objected to.
- ☒ Claims 5-13 are subject to restriction or election requirement.
- ☒ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
- ☐ Formal drawings are required in response to this Office action.
- ☐ The corrected or substitute drawings have been received on —. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
- ☐ The proposed additional or substitute sheet(s) of drawings, filed on —, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
- ☐ The proposed drawing correction, filed —, has been ☐ approved; ☐ disapproved (see explanation).
- ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. —; filed on —.
- ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
- ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

Serial Number: 322,808
Art Unit: 2511

-2-

Applicant's election without traverse of Group I (claims 1-4) in Paper No. 4 is acknowledged.

The disclosure is objected to because of the following informalities: Claim 1, line 10, "copy" should be replaced by --copies--. Claim 2, line 4, "store" should be replaced by --stored--. Claim 4, line 1, "processor" should be replaced by --processing--. Line 6, --copy-- should be replaced by --copies-. Appropriate correction is required.

Claims 3-4 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, "said line voltage" (line 3) lacks positive antecedent basis.

In claim 4, "a most valid and most recent" is indefinite.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. § 102(b) as being anticipated by NEC Document ("Supercap" User's Manual).

NEC Document shows all the limitations of the claimed RAM backup system, comprising a RAM (RAM), a capacitor (Supercap), a ROM (ROM), and processing means (CPU). Refer to figs. 33-37.

Serial Number: 322,808
Art Unit: 2511

-3-

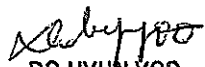
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kimura et al. show back-up power supply apparatus for protection of stored data.

Any inquiry concerning this communication should be directed to Do H. Yoo at telephone number (703) 308-4908.

Yoo/tj b17

May 17, 1995


DO HYUN YOO
PRIMARY EXAMINER
GROUP 2500

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

FORM PTO-892 (REV. 3-78)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 08/322808		GROUP/ART UNIT 2511		ATTACHMENT TO PAPER NUMBER 5						
NOTICE OF REFERENCES CITED				APPLICANT(S) Reasoner et al.										
U.S. PATENT DOCUMENTS														
*		DOCUMENT NO.						DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE		
	A	5	3	7	5	2	4	6	12/20/94	Kimura et al.	365	226 X	8/26/91	
	B													
	C													
	D													
	E													
	F													
	G													
	H													
	I													
	J													
	K													
FOREIGN PATENT DOCUMENTS														
*		DOCUMENT NO.						DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
	L													
	M													
	N													
	O													
	P													
	Q													
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)														
	R													
	S													
	T													
	U													
EXAMINER								DATE						
Do Hyun Too								5/12/95						
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)														

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

PTO Draftpersons review all originally filed drawings regardless of whether they are designated as formal or informal. Additionally, patent Examiners will review the drawings for compliance with the regulations. Direct telephone inquiries concerning this review to the Drawing Review Branch, 703-305-8404.

The drawings filed (insert date) 11/13/94, are
 A. ☒ not objected to by the Draftsperson under 37 CFR 1.84 or 1.152.
 B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this Notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:

- Black ink. Color.
☐ Not black solid lines. Fig(s) _____
☐ Color drawings are not acceptable until petition is granted.

2. PHOTOGRAPHS. 37 CFR 1.84(b)

- ☐ Photographs are not acceptable until petition is granted.

3. GRAPHIC FORMS. 37 CFR 1.84(d)

- ☐ Chemical or mathematical formula not labeled as separate figure. Fig(s) _____
☐ Group of waveforms not presented as a single figure, using common vertical axis with time extending along horizontal axis. Fig(s) _____
☐ Individuals waveform not identified with a separate letter designation adjacent to the vertical axis. Fig(s) _____

4. TYPE OF PAPER. 37 CFR 1.84(e)

- ☐ Paper not flexible, strong, white, smooth, nonshiny, and durable. Sheet(s) _____
☐ Erasures, alterations, overwritings, interlineations, cracks, creases, and folds not allowed. Sheet(s) _____

5. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable paper sizes:

- 21.6 cm. by 35.6 cm. (8 1/2 by 14 inches)
 21.6 cm. by 33.1 cm. (8 1/2 by 13 inches)
 21.6 cm. by 27.9 cm. (8 1/2 by 11 inches)
 21.0 cm. by 29.7 cm. (DIN size A4)

- ☐ All drawing sheets not the same size. Sheet(s) _____
☐ Drawing sheet not an acceptable size. Sheet(s) _____

6. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Paper size			
21.6 cm. X 35.6 cm. (8 1/2 X 14 inches)	21.6 cm. X 33.1 cm. (8 1/2 X 13 inches)	21 cm. X 27.9 cm. (8 1/2 X 11 inches)	21 cm. X 29.7 cm. (DIN Size A4)
T 5.1 cm. (2")	2.5 cm. (1")	2.5 cm. (1")	2.5 cm.
L .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	2.5 cm.
R .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.5 cm.
B .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.0 cm.

Margins do not conform to chart above.

Sheet(s) _____
☐ Top (T) ☐ Left (L) ☐ Right (R) ☐ Bottom (B)

7. VIEWS. 37 CFR 1.84(h)

REMINDER: Specification may require revision to correspond to drawing changes.

- ☐ All views not grouped together. Fig(s) _____
☐ Views connected by projection lines. Fig(s) _____
☐ Views contain center lines. Fig(s) _____

Partial views. 37 CFR 1.84(h)(2)

- ☐ Separate sheets not linked edge to edge. Fig(s) _____
☐ View and enlarged view not labeled separately. Fig(s) _____

- ☐ Long view relationship between different parts not clear and unambiguous. 37 CFR 1.84(h)(2)(ii) Fig(s) _____

Sectional views. 37 CFR 1.84(h)(3)

- ☐ Hatching not indicated for sectional portions of an object. Fig(s) _____
☐ Hatching of regularly spaced oblique parallel lines not spaced sufficiently. Fig(s) _____
☐ Hatching not at substantial angle to surrounding axes or principal lines. Fig(s) _____
☐ Cross section not drawn same as view with parts in cross section with regularly spaced parallel oblique strokes. Fig(s) _____
☐ Hatching of juxtaposed different elements not angled in a different way. Fig(s) _____

Alternate position. 37 CFR 1.84(h)(4)

- ☐ A separate view required for a moved position. Fig(s) _____

Modified forms. 37 CFR 1.84(h)(5)

- ☐ Modified forms of construction must be shown in separate views. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

- ☐ View placed upon another view or within outline of another. Fig(s) _____
☐ Words do not appear in a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____

9. SCALE. 37 CFR 1.84(k)

- ☐ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____
☐ Indication such as "actual size" or "scale 1/2" not permitted. Fig(s) _____
☐ Elements of same view not in proportion to each other. Fig(s) _____

10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)

- ☒ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (except for color drawings). Fig(s) 1-4

11. SHADING. 37 CFR 1.84(m)

- ☐ Shading used for other than shape of spherical, cylindrical, and conical elements of an object, or for flat parts. Fig(s) _____
☐ Solid black shading areas not permitted. Fig(s) _____

12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)

- ☐ Numbers and reference characters not plain and legible. 37 CFR 1.84(p)(i) Fig(s) _____
☐ Numbers and reference characters used in conjunction with brackets, inverted commas, or enclosed within outlines. 37 CFR 1.84(p)(i) Fig(s) _____
☐ Numbers and reference characters not oriented in same direction as the view. 37 CFR 1.84(p)(i) Fig(s) _____
☐ English alphabet not used. 37 CFR 1.84(p)(2) Fig(s) _____
☒ Numbers, letters, and reference characters do not measure at least .32 cm. (1/8 inch) in height. 37 CFR(p)(3) Fig(s) _____

13. LEAD LINES. 37 CFR 1.84(q)

- ☐ Lead lines cross each other. Fig(s) _____
☐ Lead lines missing. Fig(s) _____
☐ Lead lines not as short as possible. Fig(s) _____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)

- ☐ Number appears in top margin. Fig(s) _____
☐ Number not larger than reference characters. Fig(s) _____
☐ Sheets not numbered consecutively, and in Arabic numerals, beginning with number 1. Sheet(s) _____

15. NUMBER OF VIEWS. 37 CFR 1.84(u)

- ☐ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____
☐ View numbers not preceded by the abbreviation Fig. Fig(s) _____
☐ Single view contains a view number and the abbreviation Fig. Fig(s) _____
☐ Numbers not larger than reference characters. Fig(s) _____

16. CORRECTIONS. 37 CFR 1.84(w)

- ☐ Corrections not durable and permanent. Fig(s) _____

17. DESIGN DRAWING. 37 CFR 1.152

- ☐ Surface shading shown not appropriate. Fig(s) _____
☐ Solid black shading not used for color contrast. Fig(s) _____

ATTACHMENT TO PAPER NO. 5REVIEWER [Signature]DATE 12/1/94

REMINDER

Drawing changes may also require changes in the specification, e.g., if Fig. 1 is changed to Fig. 1A, Fig. 1B, Fig. 1C, etc., the specification, at the Brief Description of the Drawings, must likewise be changed. Please make such changes by 37 CFR 1.312 Amendment at the time of submitting drawing changes.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Review Branch.

2. Timing of Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable correction resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon as possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO 948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

HEWLETT-PACKARD COMPANY
Legal Department, 2080
P.O. Box 10301
Folsom, California 94303-0890

PATENT APPLICATION
ATTORNEY DOCKET NO. 1094458-1



IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Reasoner, et al.

Serial No.: 08/322,808

Examiner: Yoo, D.

Filing Date: October 13, 1994

Group Art Unit: 2511

Title: System And Method For RAM Power And Data Backup
Utilizing A Capacitor And ROM

THE COMMISSIONER OF PATENTS & TRADEMARKS
Washington, D.C. 20231

RECEIVED

AUG 22 1995

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

GROUP 230

Sir:

Transmitted herewith is/are the following in the above-identified application:

- ☒ Response/Amendment ☐ Petition to extend time to respond
☐ New fee as calculated below ☐ Supplemental Declaration
☐ No additional fee (Address envelope to "Box Non-Fee Amendments")
☒ Other: New Abstract

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	4	MINUS	20	=	X \$ 22	\$ 0
INDEP. CLAIMS	1	MINUS	3	=	X \$ 76	\$ 0
[] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ \$240	\$ 0
EXTENSION FEE	1ST MONTH \$110.00	2ND MONTH \$370.00	3RD MONTH \$870.00	4TH MONTH \$1360.00		\$ 0
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	\$ 0

Charge \$ 0.00 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

By A. W. Winfield

Augustus W. Winfield
Attorney/Agent for Applicant(s)
Reg. No. 34,046

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Date of Deposit: August 10, 1995

Date: August 10, 1995

Typed Name: Laura A. Schutze

Signature: Laura A. Schutze

Telephone No.: (303) 229-3800



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Reasoner *et al.*

Appl. No.: 08/322,808

Filed: October 13, 1994

For: **System and Method for RAM
Power and Data Backup Utilizing a
Capacitor and ROM**

Art Unit: 2511

Examiner: Yoo, D.

Atty Docket: 1094458-1

6/a
fl
RECEIVED
AUG 22 1995
GROUP 2511

RESPONSE AND AMENDMENT UNDER 37 CFR § 1.111

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Office Action dated May 24, 1995 (PTO paper no. 5), Applicants submit the following Amendments and Remarks.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account, No. 19-0036.

Kindly enter the following amendments:

A

Amendments

In the Abstract

Please replace the abstract of the invention with the new abstract attached hereto.

In The Specification

Page 2, line 25, delete "requires" and insert therefor --require--; and
line 26, after "for", insert --only--.

Page 3, line 6, delete "only";
after "capacitor", insert --alone--;
line 8, after "for", insert --only--; and
line 20, after "that", insert --for--.

Page 4, lines 15-16, delete "a previously stored copy of the" and insert therefor --the
most recent valid copy of RAM--.

Page 6, line 9, after "that", insert --for--.

Page 10, line 3, delete "is" and insert therefor --are--; and
line 5, before "which", insert --for--.

Page 14, line 5, after "function", insert --of--.

Page 17, line 9, delete "backup" and insert therefor --backed--.

In The Claims

Please amend the claims as follows:

Claim 1, line 2, after "RAM" insert --,--,
line 3, before "voltage" insert --supply--,
line 5, delete "first", and
line 10, change "copy" to --copies--.
Claim 2, line 4, change "store" to --stored--.

1 3. The system of claim 2, further comprising:
2 a power supply circuit, interposed between said RAM and a line power source having
3 a line voltage [and said RAM], configured to convert and maintain said line voltage to said [a
4 specified] supply voltage [associated with said RAM].

Claim 4, line 1, change "processor" to --processing--,
line 5, delete "a most valid and" and insert therefor --the--,
after "recent", insert --valid copy--, and
line 6, change "copy" to --copies--.

Remarks

Claims 1-4 are now pending in the application. Claim 1 is independent. By the foregoing Amendment, claims 1-4 are sought to be amended.

The specification has been amended to correct minor typographical errors.

The foregoing amendments are believed not to introduce new matter and their entry is respectfully requested. Based on the foregoing amendments and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

I. Rejections under 35 U.S.C. § 112

The Examiner has rejected claims 3-4 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. In light of the foregoing amendments to claims 3-4, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

II. Rejections under 35 U.S.C. § 102(b)

The Examiner has rejected claims 1-4 under 35 U.S.C. § 102(b) as allegedly being anticipated by NEC Document ("Supercap" User's Manual). Based on the following remarks, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Applicants' claimed invention is directed to a system and method for permanently backing up RAM memory devices. The invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The invention also utilizes a ROM as a secondary backup device for backing up and restoring valid RAM data when the duration of power loss is greater than that for which the capacitor can supply backup power. Thus, the integrity of RAM data is guaranteed for all types of power fluctuations, interruptions, and failures. The ROM includes two storage areas for separately storing two copies of RAM data. The processor first determines whether the data stored in the RAM is valid. If the present RAM data is valid, the processor backs up the present RAM data by replacing the oldest or invalid copy in the ROM with the present RAM data. If the present RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM.

The "Supercap" User's Manual is a user's manual for an electric double-layer capacitor. While the figures cited by the Examiner (Figures 33-37) disclose some typical applications for the capacitor, it is respectfully submitted that none of the figures anticipate Applicants' claimed invention.

In a rejection under 35 U.S.C. § 102, each and every claimed element must be present in the applied reference. However, as will be explained below, the cited reference does not anticipate the recitations and the language of independent claim 1. Therefore, it is respectfully requested that the rejection be reconsidered and withdrawn.

Of the figures cited by the Examiner, the most relevant is Figure 36 - Memory Backup Circuit Diagram. However, Figure 36 fails to teach the fourth element of independent claim 1, reproduced in full below.

processing means, coupled to said RAM and said ROM, for transferring said copy of said data stored in said RAM to said ROM.

Figure 36 is found in section 5.5.1 of the "Supercap" User's Manual, entitled "Example Application of Supercap"; no descriptive text accompanies the figure. The figure depicts four RAM chips and a decoder chip; the power supply inputs of the chips are fed by a 5-volt power supply in parallel with a "Supercap" capacitor. The decoder receives address bits from a CPU (not depicted) and decodes the address bits to select one of the four depicted RAM chips or one of four other ROM or RAM chips (not depicted).

The clear purpose of Figure 36 is to depict a circuit whereby a "Supercap" capacitor is used to provide temporary backup power to the depicted chips in the event of a temporary outage of the 5-volt power source. Figure 36 teaches nothing else. Because no means of data transfer, such as a data bus, are depicted, no data transfer operation, such as that claimed by Applicants, is taught. Thus the "Supercap" User's Manual fails to teach the fourth element of Applicants' independent claim 1.

Applicants' claims 2-4 depend directly or indirectly from claim 1. The rejection of claim 1 was traversed above; therefore the rejection of dependent claims 2-4 is similarly traversed.

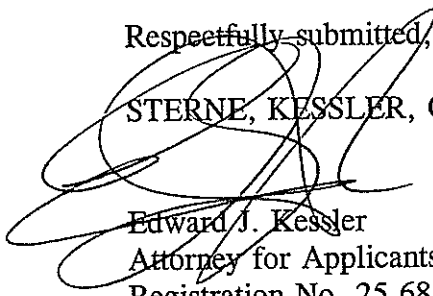
For at least these reasons, Applicants respectfully request that the Examiner's rejection of claims 1-4 under 35 U.S.C. § 102(b) be withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections, and that they be withdrawn. The Examiner is invited to telephone the undersigned representative if it is believed that an interview might be useful for any reason.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX


Edward J. Kessler
Attorney for Applicants
Registration No. 25,688

Date: August 9, 1995

1100 New York Avenue, N.W.
Washington, D.C. 20005
(202) 371-2600

System and Method For RAM Power And Data Backup Utilizing A Capacitor And ROM

Abstract

5 A system and method for permanently backing up RAM memory
devices. The present invention utilizes a capacitor as a primary backup device
for supplying the necessary backup power for power fluctuations, power
interruptions, and other short-duration power failures. The present invention
also utilizes a ROM as a secondary backup device for backing up and
restoring valid RAM data when the duration of power loss is greater than that
10 for which the capacitor can supply backup power. Thus, the integrity of
RAM data is guaranteed for all types of power fluctuations, interruptions, and
failures. The ROM includes two storage areas for separately storing two
copies of RAM data. The processor first determines whether the data stored
in the RAM is valid. If the present RAM data is valid, the processor backs
15 up the present RAM data by replacing the oldest or invalid copy in the ROM
with the present RAM data. If the present RAM data is not valid, the
processor restores the RAM data with the most recent valid data previously
stored in the ROM.



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
---------------	-------------	----------------------	---------------------

08/322,808 10/13/94 REASONER

K 10944581

EXAMINER

YOU, D

25M1/1025

ART UNIT

PAPER NUMBER

7

RECORDS MANAGER
LEGAL DEPARTMENT 2080
HEWLETT-PACKARD COMPANY
P O BOX 10301
PALO ALTO CA 94303-0890

2511

DATE MAILED:

10/25/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 8-14-95 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- | | |
|---|---|
| 1. ☒ Notice of References Cited by Examiner, PTO-892. | 2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948. |
| 3. ☐ Notice of Art Cited by Applicant, PTO-1449. | 4. ☐ Notice of Informal Patent Application, PTO-152. |
| 5. ☐ Information on How to Effect Drawing Changes, PTO-1474. | 6. ☐ |

Part II SUMMARY OF ACTION

1. ☒ Claims 1-13 are pending in the application.

Of the above, claims none are withdrawn from consideration.

2. ☐ Claims have been cancelled.

3. ☐ Claims are allowed.

4. ☒ Claims 1-4 are rejected.

5. ☐ Claims are objected to.

6. ☒ Claims 5-13 are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on . Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on , has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed , has been ☐ approved; ☐ disapproved (see explanation).

12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. ; filed on .

13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

Serial Number: 322,808
Art Unit: 2511

-2-

Claim 4 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, "the most recent valid copy" (line 5) lacks positive antecedent basis.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sasayama et al.

Sasayama et al. show all the limitations of the claimed RAM backup system in Figs. 1-11, comprising a RAM 112, a capacitor 134, a ROM 120, and processing means 108 and 114. Further, refer to columns 5-6.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ueda et al., Fujioka, Totani, and Muguruma et al. show a RAM back up system.

Any inquiry concerning this communication should be directed to Do H. Yoo at telephone number (703) 308-4908.

Yoo/tj DHY

Oct. 23, 1995


DO HYUN YOO
PRIMARY EXAMINER
GROUP 2500

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

FORM PTO-892 (REV. 2-92)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 081322808		GROUP/ART UNIT 2511		ATTACHMENT TO PAPER NUMBER 7						
NOTICE OF REFERENCES CITED				APPLICANT(S) Reasoner et al.										
U.S. PATENT DOCUMENTS														
*		DOCUMENT NO.						DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE		
	A	5	2	4	3	5	7	7	9/17/93	Ueda et al.	365	228 X		
	B	5	2	0	6	9	3	8	4/27/93	Fujioka	365	228 X		
	C	5	1	7	5	8	4	2	12/29/92	Totani	365	228 X		
	D	4	3	9	9	5	2	4	8/16/83	Muguruma et al.	365	228 X		
	E	4	3	4	8	7	2	9	9/17/82	Sasayama et al.	365	228 X		
	F													
	G													
	H													
	I													
	J													
	K													
FOREIGN PATENT DOCUMENTS														
*		DOCUMENT NO.						DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
	L													
	M													
	N													
	O													
	P													
	Q													
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)														
	R													
	S													
	T													
	U													
EXAMINER Do Hyun Yoo								DATE 10/19/95						
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)														

HEWLETT-PACKARD COMPANY
Legal Department, 2080
P. O. Box 10301
Palo Alto, California 94303-0890

PATENT APPLICATION

ATTORNEY DOCKET NO. 1094458-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Reasoner et al.

Serial No.: 08/322,808

Examiner: Yoo, D.

Filing Date: October 13, 1994

Group Art Unit: 2511

Title: System and Method For RAM Power and Data Backup Utilizing
A Capacitor and ROM

THE COMMISSIONER OF PATENTS & TRADEMARKS
Washington, D.C. 20231

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- ☒ Response/Amendment ☐ Petition to extend time to respond
☐ New fee as calculated below ☐ Supplemental Declaration
☐ No additional fee (Address envelope to "Box Non-Fee Amendments")
☐ Other: _____

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	4	MINUS	20	= 0	X \$ 22	\$ 0
INDEP. CLAIMS	1	MINUS	3	= 0	X \$ 76	\$ 0
[] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ \$240	\$ 0
EXTENSION FEE	1ST MONTH \$110.00	2ND MONTH \$370.00	3RD MONTH \$870.00	4TH MONTH \$1360.00	\$ 0	
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	\$ 0

Charge \$ 0.00 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

Respectfully submitted,
Kelly J. Reasoner, et al.

By A. W. Winfield
Augustus W. Winfield
Attorney/Agent for Applicant(s)
Reg. No. 34,046

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Date of Deposit: Jan. 11, 1996

Typed Name: Laura A. Schutze

Date: Jan. 11, 1996

Signature: Laura A. Schutze

Telephone No.: (303) 229-3800



THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Reasoner *et al.*

Appl. No.: 08/322,808

Filed: October 13, 1994

For: **System and Method for RAM Power
and Data Backup Utilizing a
Capacitor and ROM**

Art Unit: 2511

Examiner: Yoo, D.

Atty Docket: 1094458-1

8/B
jcl
1-25-96
RECEIVED
JAN 25 1996
GROUP 2511

Response and Amendment under 37 C.F.R. § 1.111

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Office Action dated October 25, 1995 (PTO paper no. 7), Applicants submit the following Amendments and Remarks.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account, No. 19-0036.

Kindly enter the following amendments:

B

- 2 -

Amendments

In The Claims

Please amend the claims as follows:

Claim 2, line 1, change "is configured to store" to --stores--, and
line 4, change "is configured to enable" to --enables--.

-
- 1 4. (Twice Amended) The system of claim 3, wherein said processing means comprises:
2 a backup processing means for copying said first copy and said second copy of said data in
3 said RAM to said ROM; and
4 a restore processing means for copying [restoring the most recent valid copy of] said first
5 copy and said second copy [copies] of said data stored in said ROM to said RAM.
-

Remarks

Claims 1-4 are now pending in the application. Claim 1 is independent. By the foregoing Amendment, claims 2 and 4 are sought to be amended.

The foregoing amendments are believed not to introduce new matter and their entry is respectfully requested. Based on the foregoing amendments and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

I. Rejections under 35 U.S.C. § 112

The Examiner has rejected claim 4 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. In light of the foregoing amendment to claim 4, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

II. Rejections under 35 U.S.C. § 102(b)

The Examiner has rejected claims 1-4 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 4,348,729 (Sasayama *et al.*). Based on the following remarks, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Applicants' claimed invention is directed to a system and method for permanently backing up RAM memory devices. The invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The invention also utilizes a ROM as a secondary backup device for backing up and restoring valid RAM data when the duration of power loss is greater than that for which the capacitor can supply backup power. Thus, the integrity of RAM data is guaranteed for all types of power fluctuations, interruptions, and failures. The ROM includes two storage areas for separately storing two copies of RAM data. The processor first determines whether the data stored in the RAM is valid. If the present RAM data is valid, the processor backs up the present RAM data by replacing the oldest or invalid copy in the ROM with the present RAM data. If the present RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM.

Sasayama *et al.* discloses a method and system for engine control wherein a control factor is calculated and stored in RAM. The control factor stored in RAM is transferred to a non-volatile memory under predetermined conditions. The correction factor stored in non-volatile memory is transferred back to RAM upon restoration of normal supply voltage at the RAM.

In a rejection under 35 U.S.C. § 102, each and every claimed element must be present in the applied reference. However, as will be explained below, the cited reference does not contain all of the elements recited in the claims presented here. Therefore, it is respectfully requested that the rejection be reconsidered and withdrawn.

Referring first to rejected claim 1, Sasayama *et al.* does not disclose the third element of that claim, to wit:

"a read only memory (ROM) configured to store multiple copies of said data stored in said RAM"

Claim 1, lines 7-8.

In a preferred embodiment of Applicants' claimed invention, a ROM is configured to store two copies (also known as "flash copies") of the RAM data.

"One copy is the latest copy of RAM data as of the time that the system receives line power from line source power supply 120. The other copy is an older version of RAM data which is held for the unlikely event of a power interruption during the copying of data into ROM 114. Under such conditions, the more recent backup copy which was in the process of being copied to ROM 114 may have become corrupted or may be incomplete. The flash copy which is the older version of RAM data may then be used as a backup copy."

Applicants' specification, page 10, line 23 through page 11, line 2.

Thus the use of multiple flash copies is more than a mere repetition of parts; it results in a significant advantage: the ability to recover from power interruptions that occur during the backup process.

Sasayama *et al.* does not teach or suggest the use of multiple backup copies. Therefore, it cannot be employed to recover from power interruptions that occur during the backup process. Because Sasayama *et al.* does not teach or suggest this element of Applicants' independent claim 1, a rejection under 35 U.S.C. § 102 is improper.

For at least these reasons, Applicants respectfully request that the Examiner's rejection of claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Turning to rejected claim 2, Sasayama *et al.* fails to disclose the feature of claim 2, that "said ROM enables said first copy of said data to be stored and erased separately from said second copy of said data."

Applicants' claimed invention maintains two backup copies of the RAM data, which may be stored separately and erased separately. Because Sasayama *et al.* does not teach or suggest this feature, a rejection under 35 U.S.C. § 102 is improper.

For at least these reasons, Applicants respectfully request that the Examiner's rejection of claim 2 under 35 U.S.C. § 102(b) be withdrawn.

Applicants' claims 3-4 depend directly or indirectly from claim 1. The rejection of claim 1 was traversed above; therefore the rejection of dependent claims 3-4 is similarly traversed.

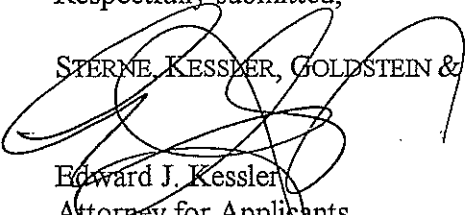
For at least these reasons, Applicants respectfully request that the Examiner's rejection of claims 1-4 under 35 U.S.C. § 102(b) be withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections, and that they be withdrawn. The Examiner is invited to telephone the undersigned representative if it is believed that an interview might be useful for any reason.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX, P.L.L.C.



Edward J. Kessler
Attorney for Applicants
Registration No. 25,688

Date: January 10, 1996

1100 New York Avenue, N.W.
Washington, D.C. 20005
(202) 371-2600



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
US/222,209	10/12/94	READOWER	

EXAMINER	ART UNIT	PAPER NUMBER
10944501		9

25N1/0400

RECORDS MANAGER
LEGAL DEPARTMENT 2050
HEWLETT-PACKARD COMPANY
P O BOX 10001
PALO ALTO CA 94300-0890

2511
DATE MAILED: 04/08/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 3-16-96 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- | | |
|---|---|
| 1. ☐ Notice of References Cited by Examiner, PTO-892. | 2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948. |
| 3. ☐ Notice of Art Cited by Applicant, PTO-1449. | 4. ☐ Notice of Informal Patent Application, PTO-152. |
| 5. ☐ Information on How to Effect Drawing Changes, PTO-1474. | 6. ☐ |

Part II SUMMARY OF ACTION

1. ☒ Claims 1-13 are pending in the application.
Of the above, claims 5-13 are withdrawn from consideration.
2. ☐ Claims have been cancelled.
3. ☐ Claims are allowed.
4. ☒ Claims 1-4 are rejected.
5. ☐ Claims are objected to.
6. ☒ Claims 5-13 are subject to restriction or election requirement.
7. ☐ This application has been filed with Informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. ; filed on .
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

Serial Number: 322,808
Art Unit: 2511

-2-

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sasayama et al.

Sasayama et al. show all the limitations of the claimed RAM back up system in Figs. 1-11, comprising a RAM 112, a capacitor 134, a ROM 120, and processing means 108 and 114. Further, refer to columns 5-6.

Applicant's arguments filed 1-16-96 have been fully considered but they are not deemed to be persuasive.

Applicant's argue that Sasayama et al. does not show a ROM configured to store multiple copies of the data stored in said RAM, as recited in claim 1. In response to this argument, Sasayama et al. clearly shows a ROM 120 configured to store multiple copies of the data stored in the RAM 112. It is respectfully requested to note that the term "multiple copies of said data" is not defined in claim 1 so that it might be broadly interpreted (for example, multiple data, words, and so on).

In addition, note that Sasayama et al. teaches multiple data transferring from RAM 112 to ROM 120 (columns 5-6).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

Serial Number: 322,808
Art Unit: 2511

-3-

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Any inquiry concerning this communication should be directed to Do H. Yoo at telephone number (703) 308-4908.

Yoo/tj *DHY*

April 3, 1996

Do Hyun Yoo
DO HYUN YOO
PRIMARY EXAMINER
GROUP 2500



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKETT NO.
---------------	-------------	-----------------------	----------------------

EXAMINER

ART UNIT	PAPER NUMBER
----------	--------------

10

DATE MAILED:

EXAMINER INTERVIEW SUMMARY RECORD

All participants (applicant, applicant's representative, PTO personnel):

- (1) Mr. Edward J. Kessler (applicant's representative) (3) Do Hyun Yoo (PTO)
- (2) Mr. Eric Manning (applicant's representative) (4)

Date of interview 5/23/96

Type: ☐ Telephonic ☒ Personal (copy is given to ☐ applicant ☒ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No. If yes, brief description: _____

Agreement ☐ was reached with respect to some or all of the claims in question. ☐ was not reached.

Claims discussed: 1

Identification of prior art discussed: Sasayama et al. reference (U.S. Patent No. 4378729)

Description of the general nature of what was agreed to if an agreement was reached, or any other comments: _____

Tried to discuss and clarify "store multiple copies of said data"
as recited in claim 1, which is the only issue in the instant application
The Examiner has reserved the final comments until the Examiner
receives the response and/or amendment.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.)

☒ 1. It is not necessary for applicant to provide a separate record of the substance of the interview.

Unless the paragraph below has been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW (e.g., items 1-7 on the reverse side of this form). If a response to the last Office action has already been filed, then applicant is given one month from this interview date to provide a statement of the substance of the interview.

☐ 2. Since the examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action. Applicant is not relieved from providing a separate record of the substance of the interview unless box 1 above is also checked.

[Signature]
Examiner's Signature

PTOL-413 (REV. 2-93)

ORIGINAL FOR INSERTION IN RIGHT HAND FLAP OF FILE WRAPPER

HEWLETT-PACKARD COMPANY
Legal Department, 2080
P.O. Box 10301
Palo Alto, California 94303-0890

MAILED
JUN 13 1996
60
UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

A. JOURNEY DOCKET NO. 1094458-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Reasoner et al.

Serial No.: 08/322,808

Examiner: Yoo, D.

Filing Date: October 13, 1994

Group Art Unit:

Title: System And Method For RAM Power And
Data Backup Utilizing A Capacitor And ROM

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

ATTN: BOX AF

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- (x) Response/Amendment () Petition to extend time to respond
() New fee as calculated below () Supplemental Declaration
(x) No additional fee
() Other: _____

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	4	MINUS	20	= 0	x \$22	\$ 0.00
INDEP. CLAIMS	1	MINUS	3	= 0	x \$78	\$ 0.00
[] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+	\$ 0.00
EXTENSION FEE	1ST MONTH	2ND MONTH	3RD MONTH	4TH MONTH	\$ 0.00	
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	\$ 0.00

Charge \$ 0.00 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231.

Date of Deposit: June 3, 1996

Typed Name: Laura A. Schutze

Signature: Laura A. Schutze

By A. W. Winfield
Augustus W. Winfield

Attorney/Agent for Applicant(s)
Reg. No. 34,046

Date: June 3, 1996

Telephone No.: (970) 229-3800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

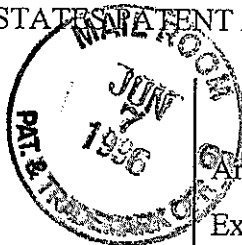
In re application of:

Reasoner *et al.*

Appl. No.: 08/322,808

Filed: October 13, 1994

For: **System and Method for RAM Power
and Data Backup Utilizing a
Capacitor and ROM**



Art Unit: 2511

Examiner: Yoo, D.

Atty Docket: 1094458-1

RECEIVED

JUN 13 1996

GROUP 2500

Response and Amendment under 37 C.F.R. § 1.116

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Office Action dated April 8, 1996 (PTO paper no. 9), Applicants submit the following Amendments and Remarks.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to the Hewlett-Packard Deposit Account, No. 08-2025.

Kindly enter the following amendments:

Amendments

In The Claims

Please amend claim 1 as follows:

1 1. A random access memory (RAM) backup system, comprising:
2 a RAM, configured to store binary data, including a supply voltage input adapted to
3 receive a supply voltage thereon;
4 a capacitor, electrically coupled to said voltage input of said RAM, configured to provide
5 said RAM with a voltage for a period of time, said voltage sufficient for said RAM to maintain
6 said storage of said data;
7 a read only memory (ROM) having separate locations for concurrently storing
8 [configured to store] multiple copies of said data stored in said RAM; and
9 processing means, coupled to said RAM and said ROM, for transferring said copies of
10 said data between [stored in] said RAM and [to] said ROM.

Remarks

Claims 1-4 are now pending in the application. Claim 1 is independent. By the foregoing
Amendment, claim 1 is sought to be amended.

23

The foregoing amendments are believed not to introduce new matter or raise new issues requiring further search or consideration. Their entry is therefore respectfully requested. Based on the foregoing amendments and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

The Examiner has rejected claims 1-4 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 4,348,729 (Sasayama *et al.*). Based on the following remarks, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Examiner Interview

The Applicants' representatives acknowledge and express their appreciation for the interview that Examiner Yoo accorded them on May 23, 1995 (see Examiner Interview Summary Record, PTO Paper No. 10). During the interview the Applicants' representatives discussed the differences between Applicants' claimed invention and the Sasayama *et al.* reference and presented proposed amendments. The Examiner indicated that Applicants' invention is conceptually different from the disclosure of Sasayama *et al.*

Rejection under 35 U.S.C. § 102(b)

Applicants' claimed invention is directed to a system and method for permanently backing up RAM memory devices. The invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The invention also utilizes a ROM as a secondary backup device for backing up and restoring valid RAM data when the duration of power loss is greater than that for which the capacitor can supply backup power. Thus, the integrity of RAM data is guaranteed

for all types of power fluctuations, interruptions, and failures. The ROM includes at least two storage areas for separately and concurrently storing at least two copies of RAM data. The processor first determines whether the data stored in the RAM is valid. If the present RAM data is valid, the processor backs up the present RAM data by replacing the oldest or invalid copy in the ROM with the present RAM data. If the present RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM.

Sasayama *et al.* discloses a method and system for engine control wherein a control factor is calculated and stored in RAM. The control factor stored in RAM is transferred to a non-volatile memory under predetermined conditions. The correction factor stored in non-volatile memory is transferred back to RAM upon restoration of normal supply voltage at the RAM.

In a rejection under 35 U.S.C. § 102, each and every claimed element must be present in the applied reference. However, as will be explained below, the cited reference does not contain all of the elements recited in the claims presented here. Therefore, it is respectfully requested that the rejection be reconsidered and withdrawn.

Referring first to amended claim 1, Sasayama *et al.* does not disclose the third element of that claim, to wit:

"a read only memory (ROM) having separate locations for concurrently storing multiple copies of said data stored in said RAM"

Claim 1, lines 7-8.

In a preferred embodiment of Applicants' claimed invention, a ROM is configured to concurrently store two copies of the RAM data at separate locations.

"As introduced above, ROM 114 is comprised of two ROM devices 104 and 106. Each of these are configured to store a copy of RAM data, referred to as a 'flash copy.' Thus, in the preferred embodiment, two copies of RAM data are maintained in ROM 114."

Applicants' specification, page 10, lines 17-18.

As explained during the Examiner interview, Sasayama *et al.* stores only one copy of RAM data in ROM at one location. Thus, when a copy of the RAM data is stored in ROM, it overwrites the previously stored copy.

Further, the maintenance of multiple copies of RAM data in ROM is more than a mere repetition of parts; it results in a significant advantage: the ability to recover from power interruptions that occur during the backup process.

"One copy is the latest copy of RAM data as of the time that the system receives line power from line source power supply 120. The other copy is an older version of RAM data which is held for the unlikely event of a power interruption during the copying of data into ROM 114. Under such conditions, the more recent backup copy which was in the process of being copied to ROM 114 may have become corrupted or may be incomplete. The flash copy which is the older version of RAM data may then be used as a backup copy."

Applicants' specification, page 10, line 23 through page 11, line 2.

Sasayama *et al.* does not teach or suggest the use of multiple concurrent backup copies. Therefore, it cannot be employed to recover from power interruptions that occur during the backup process. Because Sasayama *et al.* does not teach or suggest this element of Applicants' independent claim 1, a rejection under 35 U.S.C. § 102 is improper.

During the Examiner interview, the Examiner referred to columns 5 and 6 of Sasayama *et al.* as teaching "multiple transfers of data." Applicants have therefore again reviewed those columns, and can find no such teachings. However, even if Sasayama *et al.* contains such teachings, Applicants respectfully submit that the concept of "multiple *transfers* of data" differs significantly from the concept of concurrently storing multiple *copies* of data of the claimed invention.

For at least these reasons, Applicants respectfully request that the Examiner's rejection of claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Turning to rejected claim 2, Sasayama *et al.* fails to disclose the feature of claim 2, that "said ROM enables said first copy of said data to be stored and erased separately from said second copy of said data."

Applicants' claimed invention maintains two backup copies of the RAM data, which may be stored separately and erased separately. Because Sasayama *et al.* does not teach or suggest this feature, a rejection under 35 U.S.C. § 102 is improper.

For at least these reasons, Applicants respectfully request that the Examiner's rejection of claim 2 under 35 U.S.C. § 102(b) be withdrawn.

Applicants' claims 3-4 depend indirectly from claim 1. The rejection of claim 1 was traversed above; therefore the rejection of dependent claims 3-4 is similarly traversed.

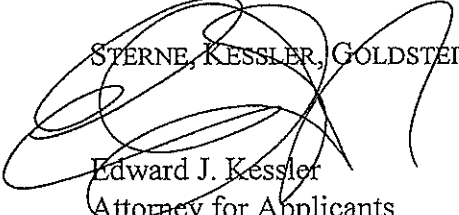
For at least these reasons, Applicants respectfully request that the Examiner's rejection of claims 1-4 under 35 U.S.C. § 102(b) be withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections, and that they be withdrawn. The Examiner is invited to telephone the undersigned representative if it is believed that an interview might be useful for any reason.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX, P.L.L.C.



Edward J. Kessler
Attorney for Applicants
Registration No. 25,688

Date: May 23, 1996

1100 New York Avenue, N.W.
Washington, D.C. 20005
(202) 371-2600



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
---------------	-------------	-----------------------	---------------------

08/322,808 10/13/94 REASONER

K 10944581

EXAMINER

YOO, D

25M1/0621

RECORDS MANAGER
LEGAL DEPARTMENT 2080
HEWLETT-PACKARD COMPANY
P O BOX 10301
PALO ALTO CA 94303-0890

ART UNIT PAPER NUMBER

2511

12

DATE MAILED: 06/21/96

NOTICE OF ALLOWABILITY

PART I.

- ☒ This communication is responsive to an amendment filed on 6-7-96.
- ☒ All the claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
- ☒ The allowed claims are 1-5.
- ☐ The drawings filed on _____ are acceptable.
- ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has [] been received, [] not been received. [] been filed in parent application Serial No. _____, filed on _____.
- ☒ Note the attached Examiner's Amendment. below
- ☐ Note the attached Examiner Interview Summary Record, PTOL-413.
- ☐ Note the attached Examiner's Statement of Reasons for Allowance.
- ☐ Note the attached NOTICE OF REFERENCES CITED, PTO-892.
- ☐ Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II.

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

- ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
- ☒ APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
 - ☒ Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No. 5. CORRECTION IS REQUIRED.
 - ☐ The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED.
 - ☐ Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
 - ☒ Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:

- ☒ Examiner's Amendment below
- ☐ Examiner Interview Summary Record, PTOL-413
- ☐ Reasons for Allowance
- ☐ Notice of References Cited, PTO-892
- ☐ Information Disclosure Citation, PTO-1449
- ☐ Notice of Informal Application, PTO-152
- ☐ Notice re Patent Drawings, PTO-948
- ☐ Listing of Bonded Draftsmen
- ☐ Other

Please note the following Examiner's Amendment.

this application is in condition for allowance except for the presence of claims 5-13 (Group II) neglected without traverse. Accordingly, claims 5-13 have been cancelled.

DO HYUN YOO
DO HYUN YOO
PRIMARY EXAMINER
GROUP 2500



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: Box ISSUE FEE
COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

RECEIVED MAIL ROOM
JUL 21 1996
PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231

NOTICE OF ALLOWANCE
AND ISSUE FEE DUE

- ☐ Note attached communication from the Examiner.
- ☐ This notice is issued in view of applicant's communication filed _____

SERIES CODE/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
First Named Applicant	06/21/96	1	06/21/96	06/21/96

TITLE OF INVENTION: SYSTEM AND METHOD FOR DATA PROCESSING AND DATA STORAGE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
10000000	01/00	00000000	UTILITY	NO	\$12,000.00	09/21/96

THE APPLICATION IDENTIFIES ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- I. Review the SMALL ENTITY Status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
 - A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the patent and Trademark Office of the change in status, or
 - B. If the Status is the same, pay the FEE DUE shown above.
- If the SMALL ENTITY is shown as NO:
 - A. Pay FEE DUE shown above, or
 - B. File verified statement of Small Entity Status before, or with, pay of 1/2 the FEE DUE shown above.
- II. Part B of this notice should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B should be completed and returned. If you are charging the ISSUE FEE to your deposit account, Part C of this notice should also be completed and returned.
- III. All communications regarding this application must give series code (or filing date), serial number and batch number. Please direct all communication prior to issuance to Box ISSUE FEE unless advised to contrary.

IMPORTANT REMINDER: Patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

OPM

H13HM

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.
Date of Deposit: September 16, 1996
By: Laura A. Schutze
Signature:

Laura A. Schutze

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
Publishing Division

SEP 20 1996

01

APPLICANT: Kelly J. Reasoner, et al.

SERIAL NO: 08/322,808

EXAMINER: D. Yoo

FILED: 10/12/94

ART UNIT: 2511

FOR: SYSTEM AND METHOD FOR RAM POWER AND DATA BACKUP UTILIZING A CAPACITOR AND ROM

DRAWING TRANSMITTAL LETTER
**THE COMMISSIONER OF PATENTS
AND TRADEMARKS
WASHINGTON, D.C. 20231**

SIR:

In response to the Notice of Allowance mailed on June 21, 1996, enclosed herewith are four (4) pages of formal drawings showing figures 1,2,3,4.

Respectfully submitted,
Kelly J. Reasoner, et al.

by A. W. Winfield
Augustus W. Winfield
Reg. No: 34,046

AWW:las
September 16, 1996
Fort Collins, CO
(970) 229-3142

(i:\dept\pto_draw) (11/18/94)

5608684

322808

APPROVED	0.9.110.1
BY	CLASS
DATE	365
REVISION	228

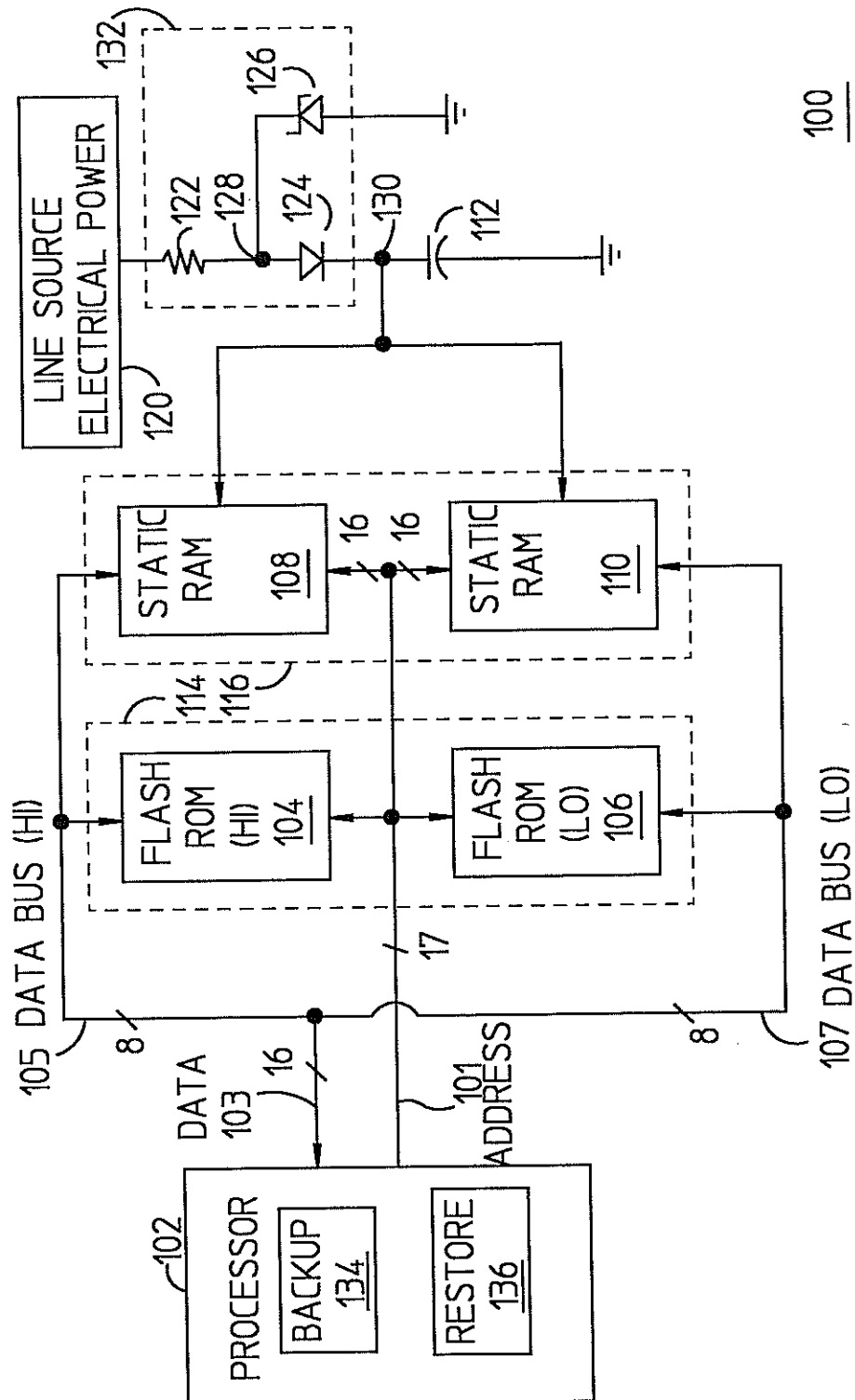


FIG 1

Hewlett-Packard Company
U.S. Serial Number: 08/322,808
Filing Date: 10/13/94
Inventor(s): Kelly J. Reasoner, et al.
Page 1 of 4

Hewlett-Packard Company
U.S. Serial Number: 08/322,808
Filing Date: 10/13/94
Inventor(s): Kelly J. Reasoner, et al.
Page 2 of 4

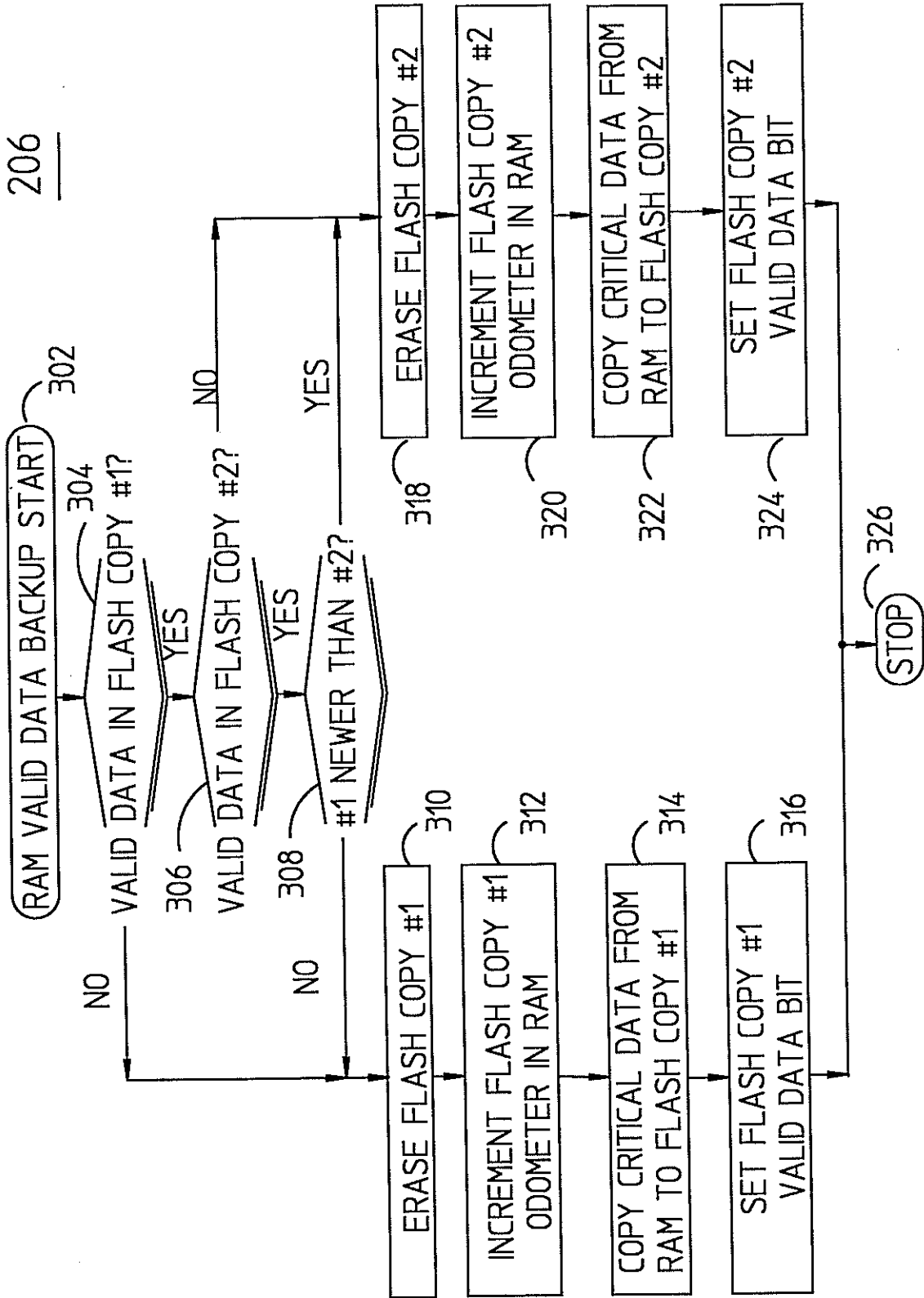


FIG 3

Hewlett-Packard Company
U.S. Serial Number: 08/322,808
Filing Date: 10/13/94
Inventor(s): Kelly J. Reasoner, et al.
Page 3 of 4

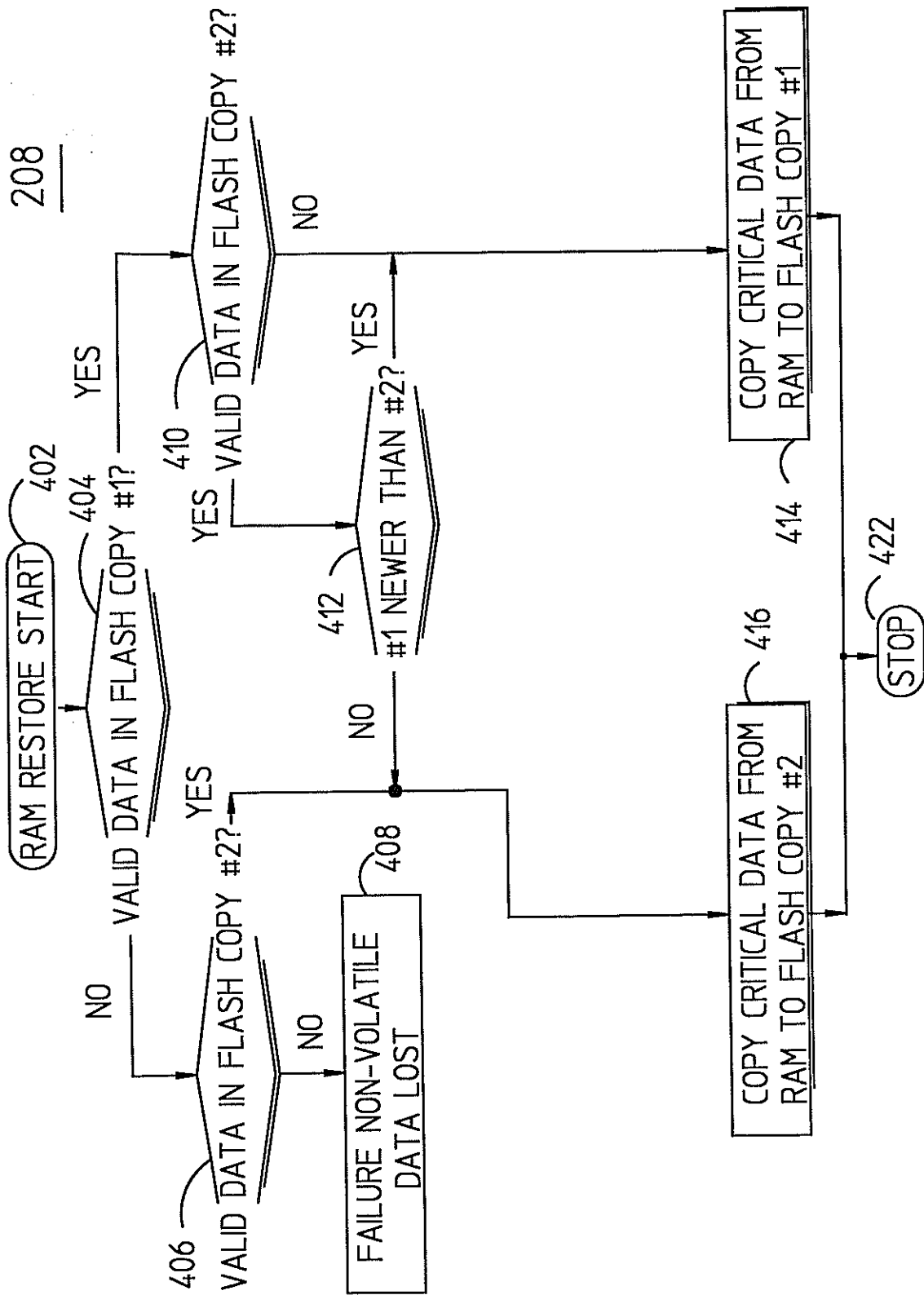


FIG 4

Hewlett-Packard Company
U.S. Serial Number: 08/322,808
Filing Date: 10/13/94
Inventor(s): Kelly J. Reasoner, et al.
Page 4 of 4

RECEIVED
Publishing Division
SEP 20 1996
01

Hewlett-Packard Company
Legal Department
3404 E. Harmony Road
Ft. Collins, CO 80525
Mail Stop 79



Phone: (970) 229-3800
Fax: (970) 229-7247

TO: George Pinderlin
OF: Publication Branch of PTO
FAX NO: 703-305-8755
1 of 3 pages

DATE: 12-11-96
TIME: 2:10PM (MST)

☐ Cynthia Baan	229-3012	☐ Jodi Juskie	229-2212
☐ Valerie Bakes	229-6967	☐ Guy Kelley	229-6970
☐ Kathy Bettinghouse	229-7246	☐ Ed Miller	229-7240
☐ Laurita Bostic	229-7660	☐ Patrick Murphy	229-6968
☐ Karl Bring	229-7244	☐ Alex Neudeck	229-4931
☐ Lynette DeBrey-Cota	229-7243	☐ Craig Pace	229-2733
☐ Linda Depperschmidt	229-4956	☐ Tom Perkins	229-6287
☐ Jeff Fromm	229-7241	☐ Jeannie McGrew	229-7245
☐ Izah Gallagher	229-4587	☒ Laurie Schutze	229-4919
☐ Kevin Hart	229-7057	☐ Gus Winfield	229-3142

COMMENTS:

Per your request of today to our Outside Counsel, please
find attached the front + back copies of Form PTO 85B
for Serial No: 08/322,808. This form was mailed to
the PTO on Sept. 16, 1996. Please call if you require anything
further.

Warning: This message is intended only for use of the individual or entity to which it is addressed and may contain information which is privileged, confidential, and exempt from disclosure under applicable law. If you are not the intended recipient, you are hereby notified that any use, dissemination, distribution, or copying of this communication is strictly prohibited. If you have received this communication in error, please notify us immediately by telephone, and return this original message to us at the above address via the U.S. Postal Service. Thank you.

SENT BY: HEWLETT-PACKARD CO.

12-11-96 : 4:20PM : FORT COLLINS LEGAL

703 305 8755: # 2

MAILING INSTRUCTIONS: This form should be completed and submitted with the ISSUE FEE. Blocks 2 through 6 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to addressee entered in Block 1 unless you direct otherwise, by: (a) specifying a new correspondence address in Block 3 below; or (b) providing the PTO with a separate "FEE ADDRESS" for maintenance fee notifications with the payment of Issue Fee or thereafter. See reverse for Certificate of Mailing.

1. CORRESPONDENCE ADDRESS	2. INVENTOR(S) ADDRESS CHANGE (Complete only if there is a change)
RECORDS MANAGER LEGAL DEPARTMENT 2080 HEWLETT-PACKARD COMPANY P O BOX 10301 PALO ALTO CA 94303-0890	INVENTOR'S NAME
	Street Address
	City, State and ZIP Code
	CO-INVENTOR'S NAME
	Street Address
	City, State and ZIP Code
	☐ Check if additional changes are on reverse side

SERIES CODE/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/322,808	10/13/94	004	YOO, D	2511 06/21/96

TITLE OF INVENTION: REASONER, KELLY J.
SYSTEM AND METHOD FOR RAM POWER AND DATA BACKUP UTILIZING A CAPACITOR AND ROM

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 10944581	365-228,000	B29	UTILITY	NO	\$1250.00	09/23/96

1. Correspondence address change (Complete only if there is a change)	4. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR, alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will be printed.
Hewlett-Packard Company IP Administration, M/S 20 BN P.O. Box 10301 Palo Alto, CA 94303-0890	1 _____ 2 _____ 3 _____

D 820 1 082025 82308 960920 960927 142 1250.00	DO NOT USE THIS SPACE
D 820 1 082025 82308 960920 960927 561 36.00	

ASSIGNMENT DATA TO BE PRINTED ON THE PATENT (print or type)	
(1) NAME OF ASSIGNEE: Hewlett-Packard Company	8a. The following fees are enclosed: ☐ Issue Fee ☐ Advance Order - # of Copies _____
(2) ADDRESS: (CITY & STATE OR COUNTRY) Palo Alto, California, USA	8b. The following fees should be charged to: DEPOSIT ACCOUNT NUMBER 08-2025 (ENCLOSE PART C) ☒ Issue Fee ☒ Advance Order - # of Copies 12 ☒ Any Deficiencies in Enclosed Fees
☐ This application is NOT assigned. ☒ Assignment previously submitted to the Patent and Trademark Office. ☐ Assignment is being submitted under separate cover. Assignments should be directed to Box ASSIGNMENTS. PLEASE NOTE: Unless an assignee is identified in Block 6, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.	The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified above. (Authorized Signature) <u>A. W. Wimpfelf</u> (Date) 09/16/96 NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

TRANSMIT THIS FORM WITH FEE-CERTIFICATE OF MAILING ON REVERSE

PTOL-858 (REV. 4-94) (0851-0033)

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Box ISSUE FEE
Commissioner of Patents and Trademarks
Washington, D.C. 20231

RECEIVED
SEP 16 1996
U.S. PATENT & TRADEMARK OFFICE
WASHINGTON, D.C. 20503

on September 16, 1996
(Date)

Laura A. Schutze
(Name of person making deposit)

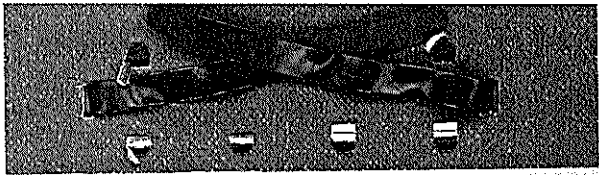
(Signature)

(Date)

Note: If this certificate of mailing is used, it can only be used to transmit the Issue Fee.

This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Burden Hour Statement: This form is estimated to take .2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Office of Information Systems, Patent and Trademark Office, Washington, D.C. 20231, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, (Project 0651-0033), Washington, D.C. 20503. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks, Box Issue Fee, Washington, DC 20231.



PTO UTILITY GRANT
Paper Number 14

The Commissioner of Patents
and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

Bruce Lehman
Commissioner of Patents and Trademarks

Melvinia Gary
Attest

Form PTO-1584 (Rev. 5/96)

(RIGHT INSIDE)

FPI-LGM



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

CHANGE OF ADDRESS/POWER OF ATTORNEY

LOCATION 9200 SERIAL NUMBER 08322808 PATENT NUMBER 5608684

THE CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 22879

THE PRACTITIONERS OF RECORD HAVE BEEN CHANGED TO CUSTOMER # 22879

ON 02/07/00 THE ADDRESS OF RECORD FOR CUSTOMER NUMBER 22879 IS:

HEWLETT PACKARD COMPANY
INTELLECTUAL PROPERTY ADMINISTRATION
3404 E HARMONY ROAD
P O BOX 272400
FORT COLLINS CO 80528-9599

AND THE PRACTITIONERS OF RECORD FOR CUSTOMER NUMBER 22879 ARE:

22944	23035	24266	26762	26978	27091	27196	28614	28910	30405
30558	30581	31183	31267	31591	32057	32490	32905	33472	34046
35185	35186	35592	35675	35931	36199	36241	36618	36771	36823
37079	37157	37721	39043	39779	39819	40231	40952	41220	41314
42206	42846	42919	43133	43955	44395	44652			

PTO INSTRUCTIONS: PLEASE TAKE THE FOLLOWING ACTION WHEN THE
CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER NUMBER:
RECORD, ON THE NEXT AVAILABLE CONTENTS LINE OF THE FILE JACKET,
'ADDRESS CHANGE TO CUSTOMER NUMBER'. LINE THROUGH THE OLD
ADDRESS ON THE FILE JACKET LABEL AND ENTER ONLY THE 'CUSTOMER
NUMBER' AS THE NEW ADDRESS. FILE THIS LETTER IN THE FILE JACKET.
WHEN ABOVE CHANGES ARE ONLY TO FEE ADDRESS AND/OR PRACTITIONERS
OF RECORD, FILE LETTER IN THE FILE JACKET.

PATENT APPLICATION FEE DETERMINATION RECORD Effective October 1, 1995					Application or Docket Number	
CLAIMS AS FILED - PART I						
		(Column 1)	(Column 2)			
FOR		NUMBER FILED		NUMBER EXTRA		
BASIC FEE						
TOTAL CLAIMS			minus 20 =			
INDEPENDENT CLAIMS			minus 3 =			
MULTIPLE DEPENDENT CLAIM PRESENT						
* If the difference in column 1 is less than zero, enter "0" in column 2						
CLAIMS AS AMENDED - PART II						
		(Column 1)	(Column 2)	(Column 3)		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total	* 13	Minus	** 20	=	
	Independent	* 3	Minus	*** 3	=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total	* 13	Minus	** 20	=	
	Independent	* 3	Minus	*** 3	=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					
AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total	*	Minus	**	=	
	Independent	*	Minus	***	=	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					
				SMALL ENTITY	OR	OTHER THAN SMALL ENTITY
				RATE	FEE	RATE
				x\$11=		x\$22=
				x39=		x78=
				+125=		+250=
				TOTAL		TOTAL
				SMALL ENTITY	OR	OTHER THAN SMALL ENTITY
				RATE	ADDITIONAL FEE	RATE
				x\$11=		x\$22=
				x39=		x78=
				+125=		+250=
				TOTAL ADDIT. FEE		TOTAL ADDIT. FEE
				SMALL ENTITY	OR	OTHER THAN SMALL ENTITY
				RATE	ADDITIONAL FEE	RATE
				x\$11=		x\$22=
				x39=		x78=
				+125=		+250=
				TOTAL ADDIT. FEE		TOTAL ADDIT. FEE

*** If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875

PATENT APPLICATION FEE DETERMINATION RECORD Effective October 1, 1994						Application or Docket Number <div>322 808</div>					
CLAIMS AS FILED - PART I						SMALL ENTITY		OR	OTHER THAN SMALL ENTITY		
		(Column 1)			(Column 2)	RATE	FEE		RATE	FEE	
FOR		NUMBER FILED		NUMBER EXTRA			365.00	OR		730.00	
BASIC FEE						x\$11=		OR	x\$22=		
TOTAL CLAIMS		13 minus 20 =		*		x38=		OR	x76=		
INDEPENDENT CLAIMS		3 minus 3 =		*		+120=		OR	+240=		
MULTIPLE DEPENDENT CLAIM PRESENT						TOTAL		OR	TOTAL	730	
* If the difference in column 1 is less than zero, enter "0" in column 2											
CLAIMS AS AMENDED - PART II						SMALL ENTITY		OR	OTHER THAN SMALL ENTITY		
		(Column 1)			(Column 2)	(Column 3)	RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA						
	Total	*	Minus	**	=	x\$11=		OR	x\$22=		
	Independent	*	Minus	***	=	x38=		OR	x76=		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+120=		OR	+240=		
		(Column 1)			(Column 2)	(Column 3)	TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA						
	Total	*	Minus	**	=	x\$11=		OR	x\$22=		
	Independent	*	Minus	***	=	x38=		OR	x76=		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+120=		OR	+240=		
		(Column 1)			(Column 2)	(Column 3)	TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	
AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA						
	Total	*	Minus	**	=	x\$11=		OR	x\$22=		
	Independent	*	Minus	***	=	x38=		OR	x76=		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+120=		OR	+240=		
		(Column 1)			(Column 2)	(Column 3)	TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20." *** If the Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3." The Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office										1ST EXAMINER <i>R. Quetz</i>		DATE <i>11/29/94</i>	
Form PTO-1130 (REV 2/94)										2ND EXAMINER		DATE	
PACE DATA ENTRY CODING SHEET													
APPLICATION NUMBER <i>08/322808</i>		TYPE APPL <i>1</i>	FILING DATE MONTH DAY YEAR <i>10 13 94</i>			SPECIAL HANDLING <i>0</i>	GROUP ART UNIT <i>2511</i>		CLASS <i>365</i>	SHEETS OF DRAWING <i>1-4</i>			
TOTAL CLAIMS <i>13</i>		INDEPENDENT CLAIMS <i>3</i>	SMALL ENTITY? <i>0</i>	FILING FEE <i>730</i>		FOREIGN LICENSE <i>Y</i>	ATTORNEY DOCKET NUMBER <i>10947581</i>						
CONTINUITY DATA													
CONT STATUS CODE		PARENT APPLICATION SERIAL NUMBER		PCT APPLICATION SERIAL NUMBER		PARENT PATENT NUMBER		PARENT FILING DATE MONTH DAY YEAR					
				P C T /									
				P C T /									
				P C T /									
				P C T /									
				P C T /									
PCT/FOREIGN APPLICATION DATA													
FOREIGN PRIORITY CLAIMED		COUNTRY CODE		PCT/FOREIGN APPLICATION SERIAL NUMBER		FOREIGN FILING DATE MONTH DAY YEAR							

Derwent Innovation Patent Export, 2022-06-13 01:16:30 +0000

Search results for: PNS=(US5608684);

Collections searched: DWPI; ARIPO grant; Argentina UM; Argentina app; Armenia grant; Australia UM; Australia app; Australia grant; Austria UM; Austria app; Austria grant; Belarus UM; Belarus grant; Belgium app; Belgium grant; Brazil UM; Brazil app; Brazil grant; Bulgaria UM; Bulgaria app; Bulgaria grant; Canada app; Canada grant; China, Mainland UM; China, Mainland app; China, Mainland grant; Colombia app; Costa Rica UM; Costa Rica app; Croatia UM; Croatia app; Croatia grant; Cuba app; Cuba grant; Czech Republic UM; Czech Republic app; Czech Republic grant; Czechoslovakia grant; Denmark UM; Denmark app; Denmark grant; Estonia UM; Estonia app; Estonia grant; Eurasian (EAPO) grant; Europe (EP) app; Europe (EP) grant; Finland app; Finland grant; France app; France grant; Georgia grant; German Democratic Republic app; German Democratic Republic grant; Germany UM; Germany app; Germany grant; Greece app; Greece grant; Gulf Cooperation Council grant; Hong Kong UM; Hong Kong app; Hong Kong grant; Hungary grant; Iceland grant; India app; India grant; Indonesia UM; Indonesia app; Ireland UM; Ireland app; Ireland grant; Israel grant; Italy grant; Italy grant; Italy grant; Italy grant; Japan UM; Japan app; Japan grant; Korea UM; Korea app; Korea grant; Latvia grant; Lithuania grant; Luxembourg app; Luxembourg grant; Malaysia app; Malaysia grant; Mexico app; Mexico grant; Moldova UM; Moldova grant; Monaco grant; Mongolia UM; Mongolia grant; Morocco app; Morocco grant; Netherlands app; Netherlands grant; New Zealand grant; Norway app; Norway grant; OAPI grant; PCT (WO) app; Philippines UM; Philippines app; Philippines grant; Poland UM; Poland grant; Portugal UM; Portugal app; Portugal grant; Romania UM; Romania app; Romania granted; Russia UM; Russia app; Russia grant; Serbia UM; Serbia app; Serbia grant; Singapore app; Singapore grant; Slovakia UM; Slovakia app; Slovakia grant; Slovenia UM; Slovenia grant; South Africa app; Spain UM; Spain app; Spain grant; Sweden app; Sweden grant; Switzerland app; Switzerland grant; Taiwan UM; Taiwan appl; Taiwan grant; Thailand UM; Thailand app; Thailand grant; Tunisia app; Turkey UM; Turkey app; Turkey grant; UK app; UK grant; USSR grant; Ukraine UM; Ukraine grant; United States app; United States grant; Uruguay app; Vietnam UM; Vietnam app; Vietnam grant; Other

Table of Contents

- 1. US5608684A System and method for RAM power and data backup utilizing a capacitor and ROM

Family 1/1
1 record(s) per family

Record 1/1 US5608684A System and method for RAM power and data backup utilizing a capacitor and ROM

Title: System and method for RAM power and data backup utilizing a capacitor and ROM
Title - DWPI: System for permanently backing up RAM memory device has capacitor as primary device for supplying back=up power, and ROM for backing up and restoring valid RAM data when duration of power loss is greater than that for which capacitor can supply power

Priority Number: US1994322808A
Priority Date: 1994-10-13
Application Number: US1994322808A
Application Date: 1994-10-13
Publication Date: 1997-03-04

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
G11C000514	G	G11	G11C	G11C0005	G11C000514
G11C001100	G	G11	G11C	G11C0011	G11C001100

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
G11C000700 (IPC 1-7)	G	G11	G11C	G11C0007	G11C000700 (IPC 1-7)

Assignee/Applicant: Hewlett Packard Company,Palo Alto,CA,US
JP F Terms:
JP FI Codes:
Assignee - Original: Hewlett Packard Company
Any CPC Table:

Type	Invention	Additional	Version	Office
Current	G11C 5/141	-	20130101	EP; US

Current	G11C 11/005		20130101	EP; US
Original	G11C 5/141	-	20130101	US
Original	G11C 11/005		20130101	US

ECLA: G11C000514B | G11C001100C

Abstract:

A system and method for permanently backing up RAM memory devices. The present invention utilizes a capacitor as a primary backup device for supplying the necessary backup power for power fluctuations, power interruptions, and other short-duration power failures. The present invention also utilizes a ROM as a secondary backup device for backing up and restoring valid RAM data when the duration of power loss is greater than that for which the capacitor can supply backup power. Thus, the integrity of RAM data is guaranteed for all types of power fluctuations, interruptions, and failures. The ROM includes two storage areas for separately storing two copies of RAM data. The processor first determines whether the data stored in the RAM is valid. If the present RAM data is valid, the processor backs up the present RAM data by replacing the oldest or invalid copy in the ROM with the present RAM data. If the present RAM data is not valid, the processor restores the RAM data with the most recent valid data previously stored in the ROM.

Language of Publication: EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2011-09-22	AS	-
Description: ASSIGNMENT HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P., TEXAS ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:HEWLETT-PACKARD COMPANY; REEL/FRAME:026945/0699 2003-01-31		
2008-09-08	REMI	-
Description: MAINTENANCE FEE REMINDER MAILED		
2008-09-04	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 12		
2004-09-07	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 8		
2001-01-16	AS	-

Description: ASSIGNMENT HEWLETT-PACKARD COMPANY, COLORADO MERGER; ASSIGNOR:HEWLETT-PACKARD COMPANY; REEL/FRAME:011523/0469 1998-05-20		
2000-09-01	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 4		
1997-02-21	STCF	-
Description: INFORMATION ON STATUS: PATENT GRANT PATENTED CASE		
1995-07-24	AS	-
Description: ASSIGNMENT HEWLETT-PACKARD COMPANY, CALIFORNIA ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNORS:REASONER, KELLY J.; WILLIAMS, ERIC E.; REEL/FRAME:007557/0777 1994-10-05		

Post-Issuance (US):

Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
HEWLETT-PACKARD DEVELOPMENT COMPANY L.P.,HOUSTON,TX,US	HEWLETT-PACKARD COMPANY	2003-01-31	026945/0699	2011-09-22
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: HEWLETT-PACKARD COMPANY 3404 E. HARMONY ROAD MS 35 INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80528				
HEWLETT-PACKARD COMPANY,FORT COLLINS,CO,US	HEWLETT-PACKARD COMPANY	1998-05-20	011523/0469	2001-01-16
Conveyance: MERGER (SEE DOCUMENT FOR DETAILS).				
Corresponent: HEWLETT-PACKARD COMPANY VALERIE BAKES INTELLECTUAL PROPERTY ADMINISTRATION P.O. BOX 272400 FORT COLLINS, CO 80527-2400				
HEWLETT-PACKARD COMPANY,PALO ALTO,CA,US	REASONER, KELLY J.	1994-10-05	007557/0777	1995-07-24
	WILLIAMS, ERIC E.	1994-10-05	-	-
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: HEWLETT-PACKARD COMPANY CARRIE E. LEWIS LEGAL DEPARTMENT, M/S 79 3404 E. HARMONY ROAD FT. COLLINS, CO 80525				

Maintenance Status (US):

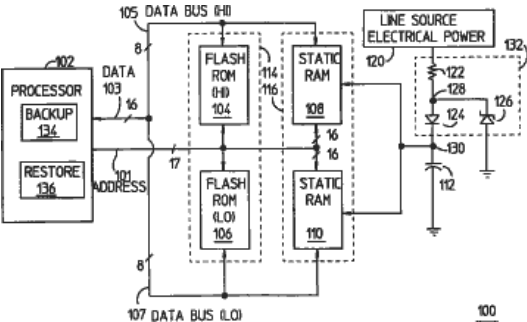
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Priority Number - DWPI: US1994322808A

Priority Date - DWPI: 1994-10-13

Assignee - Current US: HEWLETT-PACKARD DEVELOPMENT COMPANY L.P.



United States Patent and Trademark Office
Office of the Commissioner for Patents

SYSTEM AND METHOD FOR RAM POWER AND DATA BACKUP UTILIZING A CAPACITOR AND ROM

PATENT # 5608684 APPLICATION # 08322808 FILING DATE 10/13/1994 ISSUE DATE 03/04/1997

Payment Window Status

WINDOW				STATUS		FEES		No maintenance fees are due.
11.5 Year				Closed		Paid		
Window	First Day to Pay	Surcharge Starts	Last Day to Pay	Status	Fees			
3.5 Year	03/04/2000	09/06/2000	03/05/2001	Closed	Paid			
7.5 Year	03/04/2004	09/08/2004	03/04/2005	Closed	Paid			
11.5 Year	03/04/2008	09/05/2008	03/04/2009	Closed	Paid			

Patent Holder Information

Customer #	204
Entity Status	UNDISCOUNTED
Phone Number	3014248890
Address	COMPUTER PACKAGES, INC. 414 HUNGERFORD DRIVE ROCKVILLE, MD 20850 UNITED STATES