HOROWITZ and HILL

THE ART OF ELECTRONICS

SECOND EDITION

CAMBRIDGE

THE ART OF ELECTRONICS

PAUL HOROWITZ
WINFIELD HILL

SECOND EDITION

This is the thoroughly revised and updated second edition of the hugely successful *The Art of Electronics*. Widely accepted as *the* single authoritative text and reference on electronic circuit design, both analog and digital, the original edition sold over 125,000 copies worldwide and was translated into eight languages. The book revolutionized the teaching of electronics by emphasizing the methods actually used by circuit designers – a combination of some basic laws, rules of thumb, and a large bag of tricks. The result was, and is, a largely nonmathematical treatment that encourages circuit intuition, brainstorming, and simplified calculation of circuit values and performance.

This completely new edition responds to the breakneck pace of change in electronics with totally rewritten chapters on microcomputers and microprocessors, substantially revised chapters on digital electronics, on op-amps and precision design, and on construction techniques. Every table has been revised, and many new ones have been added.

The new *Art of Electronics* retains the feeling of informality and easy access that helped make the first edition so successful and popular. It is an ideal first textbook on electronics for scientists and engineers and an indispensable reference for anyone, professional or amateur, who works with electronic circuits.

The Art of Electronics covers the full range of subjects normally treated in electronics books, as well as a rich complement of important but neglected topics:

- useful subcircuits such as followers, switches, current sources, current mirrors, differential amplifiers, push-pull, cascode
- JFETs and MOSFETs, FET vs. bipolar design, ESD, amplifier design aids, analog switching
- active rectifiers, logarithmic converters, peak detectors, dielectric absorption, single-supply op-amps
- design of constant-Q and constant-BW filters, switched capacitor filters, zero-offset LPFs, single-control tunable notch, oscillators
- discrete and integrated regulators, SOA, thermal design and heat sinking, switching supplies, crowbars
- precision linear design, autonulling amplifiers, isolation amplifiers
- noise generation, measurement, and low-noise design; shielding and grounding
- timing, runt pulses, clocking skew, monostable multivibrators
- phase-locked loops, optoelectronics, driving buses, capacitive loads, cables, signal interfacing
- IBM-PC and the Intel family, RS-232 cables, serial ports, ASCII, modems, SCSI, IPI, GPIB, parallel ports, local-area networks
- 68000-family microprocessors, peripheral LSI chips, memory, instrument design with programming
- protyping methods, printed-circuit and wire-wrap design, schematic capture, instrument construction
- modular RF components, simplified design of high frequency amplifiers and high-speed switching circuits
- batteries, solar cells; micropower regulators, op-amps, microprocessors
- bandwidth-narrowing methods, signal averaging, multichannel scaling, lock-in amplifiers, pulse-height analysis

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Paul Horowitz HARVARD UNIVERSITY

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TO CAROL, JACOB, MISHA, AND GINGER

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PREFACE

Electronics, perhaps more than any other field of technology, has enjoyed an explosive development in the last four decades. Thus it was with some trepidation that we attempted, in 1980, to bring out a definitive volume teaching the art of the subject. By "art" we meant the kind of mastery that comes from an intimate familiarity with real circuits, actual devices, and the like, rather than the more abstract approach often favored in textbooks on electronics. Of course, in a rapidly evolving field, such a nuts-and-bolts approach has its hazards – most notably a frighteningly quick obsolescence.

The pace of electronics technology did not disappoint us! Hardly was the ink dry on the first edition before we felt foolish reading our words about "the classic [2Kbyte] 2716 EPROM ... with a price tag of about $25." They're so classic you can't even get them anymore, having been replaced by EPROMs 64 times as large, and costing less than half the price! Thus a major element of this revision responds to improved devices and methods – completely rewritten chapters on microcomputers and microprocessors (using the IBM PC and the 68008) and substantially revised chapters on digital electronics (including PLDs, and the new HC and AC logic families), on op-amps and precision design (reflecting the availability of excellent FET-input op-amps), and on construction techniques (including CAD/CAM). Every table has been revised, some substantially; for example, in Table 4.1 (operational amplifiers) only 65% of the original 120 entries survived, with 135 new op-amps added.

We have used this opportunity to respond to readers' suggestions and to our own experiences using and teaching from the first edition. Thus we have rewritten the chapter on FETs (it was too complicated) and repositioned it before the chapter on op-amps (which are increasingly of FET construction). We have added a new chapter on low-power and micropower design (both analog and digital), a field both important and neglected. Most of the remaining chapters have been extensively revised. We have added many new tables, including A/D and D/A converters, digital logic components, and low-power devices, and throughout the book we have expanded the number of figures. The book now contains 78 tables (available separately as *The Horowitz and Hill Component Selection Tables*) and over 1000 figures.

Throughout the revision we have strived to retain the feeling of informality and easy access that made the first edition so successful and popular, both as reference and text. We are aware of the difficulty students often experience when approaching electronics for the first time: The field is densely interwoven, and there is no path of learning that takes you, by logical steps, from neophyte to broadly competent designer. Thus we have added extensive cross-referencing throughout the text; in addition, we have expanded the separate *Laboratory Manual* into a *Student Manual* (*Student Manual for The Art of Electronics*, by Thomas C. Hayes and Paul Horowitz),

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complete with additional worked examples of circuit designs, explanatory material, reading assignments, laboratory exercises, and solutions to selected problems. By offering a student supplement, we have been able to keep this volume concise and rich with detail, as requested by our many readers who use the volume primarily as a reference work.

We hope this new edition responds to all our readers' needs – both students and practicing engineers. We welcome suggestions and corrections, which should be addressed directly to Paul Horowitz, Physics Department, Harvard University, Cambridge, MA 02138.

In preparing this new edition, we are appreciative of the help we received from Mike Aronson and Brian Matthews (AOX, Inc.), John Greene (University of Cape Town), Jeremy Avigad and Tom Hayes (Harvard University), Peter Horowitz (EVI, Inc.), Don Stern, and Owen Walker. We thank Jim Mobley for his excellent copyediting, Sophia Prybylski and David Tranah of Cambridge University Press for their encouragement and professional dedication, and the never-sleeping typesetters at Rosenlaui Publishing Services, Inc. for their masterful composition in TEX.

Finally, in the spirit of modern jurisprudence, we remind you to read the legal notice here appended.

Paul Horowitz
Winfield Hill

March 1989

LEGAL NOTICE

In this book we have attempted to teach the techniques of electronic design, using circuit examples and data that we believe to be accurate. However, the examples, data, and other information are intended solely as teaching aids and should not be used in any particular application without independent testing and verification by the person making the application. Independent testing and verification are especially important in any application in which incorrect functioning could result in personal injury or damage to property.

For these reasons, we make no warranties, express or implied, that the examples, data, or other information in this volume are free of error, that they are consistent with industry standards, or that they will meet the requirements for any particular application. THE AUTHORS AND PUBLISHER EXPRESSLY DISCLAIM THE IMPLIED WARRANTIES OF MERCHANTABILITY AND OF FITNESS FOR ANY PARTICULAR PURPOSE, even if the authors have been advised of a particular purpose, and even if a particular purpose is indicated in the book. The authors and publisher also disclaim all liability for direct, indirect, incidental, or consequential damages that result from any use of the examples, data, or other information in this book.

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PREFACE TO FIRST EDITION

This volume is intended as an electronic circuit design textbook and reference book; it begins at a level suitable for those with no previous exposure to electronics and carries the reader through to a reasonable degree of proficiency in electronic circuit design. We have used a straightforward approach to the essential ideas of circuit design, coupled with an in-depth selection of topics. We have attempted to combine the pragmatic approach of the practicing physicist with the quantitative approach of the engineer, who wants a thoroughly evaluated circuit design.

This book evolved from a set of notes written to accompany a one-semester course in laboratory electronics at Harvard. That course has a varied enrollment – undergraduates picking up skills for their eventual work in science or industry, graduate students with a field of research clearly in mind, and advanced graduate students and postdoctoral researchers who suddenly find themselves hampered by their inability to "do electronics."

It soon became clear that existing textbooks were inadequate for such a course. Although there are excellent treatments of each electronics specialty, written for the planned sequence of a four-year engineering curriculum or for the practicing engineer, those books that attempt to address the whole field of electronics seem to suffer from excessive detail (the handbook syndrome), from oversimplification (the cookbook syndrome), or from poor balance of material. Much of the favorite pedagogy of beginning textbooks is quite unnecessary and, in fact, is not used by practicing engineers, while useful circuitry and methods of analysis in daily use by circuit designers lie hidden in application notes, engineering journals, and hard-to-get data books. In other words, there is a tendency among textbook writers to represent the theory, rather that the art, of electronics.

We collaborated in writing this book with the specific intention of combining the discipline of a circuit design engineer with the perspective of a practicing experimental physicist and teacher of electronics. Thus, the treatment in this book reflects our philosophy that electronics, as currently practiced, is basically a simple art, a combination of some basic laws, rules of thumb, and a large bag of tricks. For these reasons we have omitted entirely the usual discussions of solid-state physics, the *h*-parameter model of transistors, and complicated network theory, and reduced to a bare minimum the mention of load lines and the *s*-plane. The treatment is largely nonmathematical, with strong encouragement of circuit brainstorming and mental (or, at most, back-of-the-envelope) calculation of circuit values and performance.

In addition to the subjects usually treated in electronics books, we have included the following:

- an easy-to-use transistor model
- extensive discussion of useful subcircuits, such as current sources and current mirrors
- single-supply op-amp design
- easy-to-understand discussions of topics on which practical design information is often difficult to find: op-amp frequency

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compensation, low-noise circuits, phase-locked loops, and precision linear design
- simplified design of active filters, with tables and graphs
- a section on noise, shielding, and grounding
- a unique graphical method for streamlined low-noise amplifier analysis
- a chapter on voltage references and regulators, including constant current supplies
- a discussion of monostable multivibrators and their idiosyncrasies
- a collection of digital logic pathology, and what to do about it
- an extensive discussion of interfacing to logic, with emphasis on the new NMOS and PMOS LSI
- a detailed discussion of A/D and D/A conversion techniques
- a section on digital noise generation
- a discussion of minicomputers and interfacing to data buses, with an introduction to assembly language
- a chapter on microprocessors, with actual design examples and discussion – how to design them into instruments, and how to make them do what you want
- a chapter on construction techniques: prototyping, printed circuit boards, instrument design
- a simplified way to evaluate high-speed switching circuits
- a chapter on scientific measurement and data processing: what you can measure and how accurately, and what to do with the data
- bandwidth narrowing methods made clear: signal averaging, multichannel scaling, lock-in amplifiers, and pulse-height analysis
- amusing collections of "bad circuits," and collections of "circuit ideas"
- useful appendixes on how to draw schematic diagrams, IC generic types, *LC* filter design, resistor values, oscilloscopes, mathematics review, and others
- tables of diodes, transistors, FETs, op-amps, comparators, regulators, voltage references, microprocessors, and other devices, generally listing the characteristics of both the most popular and the best types

Throughout we have adopted a philosophy of naming names, often comparing the characteristics of competing devices for use in any circuit, and the advantages of alternative circuit configurations. Example circuits are drawn with real device types, not black boxes. The overall intent is to bring the reader to the point of understanding clearly the choices one makes in designing a circuit – how to choose circuit configurations, device types, and parts values. The use of largely nonmathematical circuit design techniques does not result in circuits that cut corners or compromise performance or reliability. On the contrary, such techniques enhance one's understanding of the real choices and compromises faced in engineering a circuit and represent the best approach to good circuit design.

This book can be used for a full-year electronic circuit design course at the college level, with only a minimum mathematical prerequisite, namely, some acquaintance with trigonometric and exponential functions, and preferably a bit of differential calculus. (A short review of complex numbers and derivatives is included as an appendix.) If the less essential sections are omitted, it can serve as the text for a one-semester course (as it does at Harvard).

A separately available laboratory manual, *Laboratory Manual for the Art of Electronics* (Horowitz and Robinson, 1981), contains twenty-three lab exercises, together with reading and problem assignments keyed to the text.

To assist the reader in navigation, we have designated with open boxes in the margin those sections within each chapter that we feel can be safely passed over in an abbreviated reading. For a one-semester course it would probably be wise

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to omit, in addition, the materials of Chapter 5 (first half), 7, 12, 13, 14, and possibly 15, as explained in the introductory paragraphs of those chapters.

We would like to thank our colleagues for their thoughtful comments and assistance in the preparation of the manuscript, particularly Mike Aronson, Howard Berg, Dennis Crouse, Carol Davis, David Griesinger, John Hagen, Tom Hayes, Peter Horowitz, Bob Kline, Costas Papaliolios, Jay Sage, and Bill Vetterling. We are indebted to Eric Hieber and Jim Mobley, and to Rhona Johnson and Ken Werner of Cambridge University Press, for their imaginative and highly professional work.

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FOUNDATIONS

CHAPTER 1

INTRODUCTION

Developments in the field of electronics have constituted one of the great success stories of this century. Beginning with crude spark-gap transmitters and "cat's-whisker" detectors at the turn of the century, we have passed through a vacuum-tube era of considerable sophistication to a solid-state era in which the flood of stunning advances shows no signs of abating. Calculators, computers, and even talking machines with vocabularies of several hundred words are routinely manufactured on single chips of silicon as part of the technology of large-scale integration (LSI), and current developments in very large scale integration (VLSI) promise even more remarkable devices.

Perhaps as noteworthy is the pleasant trend toward increased performance per dollar. The cost of an electronic microcircuit routinely decreases to a fraction of its initial cost as the manufacturing process is perfected (see Fig. 8.87 for an example). In fact, it is often the case that the panel controls and cabinet hardware of an instrument cost more than the electronics inside.

On reading of these exciting new developments in electronics, you may get the impression that you should be able to construct powerful, elegant, yet inexpensive, little gadgets to do almost any conceivable task – all you need to know is how all these miracle devices work. If you've had that feeling, this book is for you. In it we have attempted to convey the excitement and know-how of the subject of electronics.

In this chapter we begin the study of the laws, rules of thumb, and tricks that constitute the art of electronics as we see it. It is necessary to begin at the beginning – with talk of voltage, current, power, and the components that make up electronic circuits. Because you can't touch, see, smell, or hear electricity, there will be a certain amount of abstraction (particularly in the first chapter), as well as some dependence on such visualizing instruments as oscilloscopes and voltmeters. In many ways the first chapter is also the most mathematical, in spite of our efforts to keep mathematics to a minimum in order to foster a good intuitive understanding of circuit design and behavior.

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Once we have considered the foundations of electronics, we will quickly get into the "active" circuits (amplifiers, oscillators, logic circuits, etc.) that make electronics the exciting field it is. The reader with some background in electronics may wish to skip over this chapter, since it assumes no prior knowledge of electronics. Further generalizations at this time would be pointless, so let's just dive right in.

VOLTAGE, CURRENT, AND RESISTANCE

1.01 Voltage and current

There are two quantities that we like to keep track of in electronic circuits: voltage and current. These are usually changing with time; otherwise nothing interesting is happening.

Voltage (symbol: V, or sometimes E). The voltage between two points is the cost in energy (work done) required to move a unit of positive charge from the more negative point (lower potential) to the more positive point (higher potential). Equivalently, it is the energy released when a unit charge moves "downhill" from the higher potential to the lower. Voltage is also called *potential difference* or *electromotive force* (EMF). The unit of measure is the *volt*, with voltages usually expressed in volts (V), kilovolts ($1\text{kV} = 10^{3}\text{V}$), millivolts ($1\text{mV} = 10^{-3}\text{V}$), or microvolts ($1\mu\text{V} = 10^{-6}\text{V}$) (see the box on prefixes). A joule of work is needed to move a coulomb of charge through a potential difference of one volt. (The coulomb is the unit of electric charge, and it equals the charge of 6×10^{18} electrons, approximately.) For reasons that will become clear later, the opportunities to talk about nanovolts ($1\text{nV} = 10^{-9}\text{V}$) and megavolts ($1\text{MV} = 10^{6}\text{V}$) are rare.

Current (symbol: I). Current is the rate of flow of electric charge past a point. The unit of measure is the ampere, or amp, with currents usually expressed in amperes (A), milliamperes ($1\text{mA} = 10^{-3}\text{A}$), microamperes ($1\mu\text{A} = 10^{-6}\text{A}$), nanoamperes ($1\text{nA} = 10^{-9}\text{A}$), or occasionally picoamperes ($1\text{pA} = 10^{-12}\text{A}$). A current of one ampere equals a flow of one coulomb of charge per second. By convention, current in a circuit is considered to flow from a more positive point to a more negative point, even though the actual electron flow is in the opposite direction.

Important: Always refer to voltage *between* two points or *across* two points in a circuit. Always refer to current *through* a device or connection in a circuit.

To say something like "the voltage through a resistor ... " is nonsense, or worse. However, we do frequently speak of the voltage *at a point* in a circuit. This is always understood to mean voltage between that point and "ground," a common point in the circuit that everyone seems to know about. Soon you will, too.

We *generate* voltages by doing work on charges in devices such as batteries (electrochemical), generators (magnetic forces), solar cells (photovoltaic conversion of the energy of photons), etc. We *get* currents by placing voltages across things.

At this point you may well wonder how to "see" voltages and currents. The single most useful electronic instrument is the oscilloscope, which allows you to look at voltages (or occasionally currents) in a circuit as a function of time. We will deal with oscilloscopes, and also voltmeters, when we discuss signals shortly; for a preview, see the oscilloscope appendix (Appendix A) and the multimeter box later in this chapter.

In real circuits we connect things together with wires, metallic conductors, each of which has the same voltage on it everywhere (with respect to ground, say). (In the domain of high frequencies or low impedances, that isn't strictly true, and we will have more to say about this later. For now, it's a good approximation.) We mention this now so that you will realize

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that an actual circuit doesn't have to look like its schematic diagram, because wires can be rearranged.

Here are some simple rules about voltage and current:

1. The sum of the currents into a point in a circuit equals the sum of the currents out (conservation of charge). This is sometimes called Kirchhoff's current law. Engineers like to refer to such a point as a *node*. From this, we get the following: For a series circuit (a bunch of two-terminal things all connected end-to-end) the current is the same everywhere.

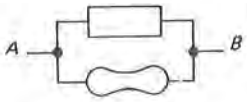


Figure 1.1

2. Things hooked in parallel (Fig. 1.1) have the same voltage across them. Restated, the sum of the "voltage drops" from A to B via one path through a circuit equals the sum by any other route equals the voltage between A and B. Sometimes this is stated as follows: The sum of the voltage drops around any closed circuit is zero. This is Kirchhoff's voltage law.

3. The power (work per unit time) consumed by a circuit device is

$$P = VI$$

This is simply (work/charge) $\times$ (charge/time). For V in volts and I in amps, P comes out in watts. Watts are joules per second (1W = 1J/s).

Power goes into heat (usually), or sometimes mechanical work (motors), radiated energy (lamps, transmitters), or stored energy (batteries, capacitors). Managing the heat load in a complicated system (e.g., a computer, in which many kilowatts of electrical energy are converted to heat, with the energetically insignificant by-product of a few pages of computational results) can be a crucial part of the system design.

PREFIXES

These prefixes are universally used to scale units in science and engineering.

Multiple	*Prefix*	*Symbol*
10^{12}	tera	T
10^{9}	giga	G
10^{6}	mega	M
10^{3}	kilo	k
10^{-3}	milli	m
10^{-6}	micro	μ
10^{-9}	nano	n
10^{-12}	pico	p
10^{-15}	femto	f

When abbreviating a unit with a prefix, the symbol for the unit follows the prefix without space. Be careful about upper-case and lower-case letters (especially m and M) in both prefix and unit: 1mW is a milliwatt, or one-thousandth of a watt; 1MHz is 1 million hertz. In general, units are spelled with lower-case letters, even when they are derived from proper names. The unit name is not capitalized when it is spelled out and used with a prefix, only when abbreviated. Thus: hertz and kilohertz, but Hz and kHz; watt, milliwatt, and megawatt, but W, mW, and MW.

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Soon, when we deal with periodically varying voltages and currents, we will have to generalize the simple equation $P = VI$ to deal with *average* power, but it's correct as a statement of *instantaneous* power just as it stands.

Incidentally, don't call current "amperage"; that's strictly bush-league. The same caution will apply to the term "ohmage" when we get to resistance in the next section.

1.02 Relationship between voltage and current: resistors

This is a long and interesting story. It is the heart of electronics. Crudely speaking, the name of the game is to make and use gadgets that have interesting and useful I-versus-V characteristics. Resistors (I simply proportional to V), capacitors (I proportional to rate of change of V), diodes (I flows in only one direction), thermistors (temperature-dependent resistor), photoresistors (light-dependent resistor), strain gauges (strain-dependent resistor), etc., are examples. We will gradually get into some of these exotic devices; for now, we will start with the most mundane (and most widely used) circuit element, the resistor (Fig. 1.2).



Figure 1.2

Resistance and resistors

It is an interesting fact that the current through a metallic conductor (or other partially conducting material) is proportional to the voltage across it. (In the case of wire conductors used in circuits, we usually choose a thick enough gauge of wire so that these "voltage drops" will be negligible.) This is by no means a universal law for all objects. For instance, the current through a neon bulb is a highly nonlinear function of the applied voltage (it is zero up to a critical voltage, at which point it rises dramatically). The same goes for a variety of interesting special devices – diodes, transistors, light bulbs, etc. (If you are interested in understanding why metallic conductors behave this way, read sections 4.4–4.5 in the *Berkeley Physics Course*, Vol. II, see Bibliography). A resistor is made out of some conducting stuff (carbon, or a thin metal or carbon film, or wire of poor conductivity), with a wire coming out each end. It is characterized by its resistance:

$$R = V/I$$

R is in ohms for V in volts and I in amps. This is known as Ohm's law. Typical resistors of the most frequently used type (carbon composition) come in values from 1 ohm (1Ω) to about 22 megohms (22MΩ). Resistors are also characterized by how

RESISTORS

Resistors are truly ubiquitous. There are almost as many types as there are applications. Resistors are used in amplifiers as loads for active devices, in bias networks, and as feedback elements. In combination with capacitors they establish time constants and act as filters. They are used to set operating currents and signal levels. Resistors are used in power circuits to reduce voltages by dissipating power, to measure currents, and to discharge capacitors after power is removed. They are used in precision circuits to establish currents, to provide accurate voltage ratios, and to set precise gain values. In logic circuits they act as bus and line terminators and as "pull-up" and "pull-down" resistors. In high-voltage circuits they are used to measure voltages and to equalize leakage currents among diodes or capacitors connected in series. In radiofrequency circuits they are even used as coil forms for inductors.

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Resistors are available with resistances from 0.01 ohm through 10^{12} ohms, standard power ratings from 1/8 watt through 250 watts, and accuracies from 0.005% through 20%. Resistors can be made from carbon-composition moldings, from metal films, from wire wound on a form, or from semiconductor elements similar to field-effect transistors (FETs). But by far the most familiar resistor is the 1/4 or 1/2 watt carbon-composition resistor. These are available in a standard set of values ranging from 1 ohm to 100 megohms with twice as many values available for the 5% tolerance as for the 10% types (see Appendix C). We prefer the Allen-Bradley type AB (1/4 watt, 5%) resistor for general use because of its clear marking, secure lead seating, and stable properties.

Resistors are so easy to use that they're often taken for granted. They're not perfect, though, and it is worthwhile to look at some of their defects. The popular 5% composition type, in particular, although fine for nearly all noncritical circuit applications, is not stable enough for precision applications. You should know about its limitations so that you won't be surprised someday. Its principal defects are variations in resistance with temperature, voltage, time, and humidity. Other defects may relate to inductance (which may be serious at high frequencies), the development of thermal hot spots in power applications, or electrical noise generation in low-noise amplifiers. The following specifications are worst-case values; typically you'll do better, but don't count on it!

SPECIFICATIONS FOR ALLEN-BRADLEY AB SERIES TYPE CB

Standard tolerance is ±5% under nominal conditions. Maximum power for 70°C ambient temperature is 0.25 watt, which will raise the internal temperature to 150°C. The maximum applied voltage specification is $(0.25R)^{1/2}$ or 250 volts, whichever is less. They mean it! (See Fig. 6.53.) A single 5 second overvoltage to 400 volts can cause a permanent change in resistance by 2%.

	Resistance change		*Permanent?*
	(R = 1k)	(R = 10M)	
Soldering (350°C at 1/8 inch)	±2%	±2%	yes
Load cycling (500 ON/OFF cycles in 1000 hours)	+4%–6%	+4%–6%	yes
Vibration (20*g*) and shock (100*g*)	±2%	±2%	yes
Humidity (95% relative humidity at 40°C)	+6%	+10%	no
Voltage coefficient (10V change)	−0.15%	−0.3%	no
Temperature (25°C to −15°C)	+2.5%	+4.5%	no
Temperature (25°C to 85°C)	+3.3%	+5.9%	no

For applications that require any real accuracy or stability a 1% metal-film resistor (see Appendix D) should be used. They can be expected to have stability of better than 0.1% under normal conditions and better than 1% under worst-case treatment. Precision wire-wound resistors are available for the most demanding applications. For power dissipation above about 0.1 watt, a resistor of higher power rating should be used. Carbon-composition resistors are available with ratings up to 2 watts, and wire-wound power resistors are available for higher power. For demanding power applications, the conduction-cooled type of power resistor delivers better performance. These carefully designed resistors are available at 1% tolerance and can be operated at core temperatures up to 250°C with dependable long life. Allowable resistor power dissipation depends on air flow, thermal conduction via the resistor leads, and circuit density; thus, a resistor's power rating should be considered a rough guideline. Note also that resistor power ratings refer to *average* power dissipation and may be substantially exceeded for short periods of time (a few seconds or more, depending on the resistor's "thermal mass").

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much power they can safely dissipate (the most commonly used ones are rated at 1/4 watt) and by other parameters such as tolerance (accuracy), temperature coefficient, noise, voltage coefficient (the extent to which R depends on applied V), stability with time, inductance, etc. See the box on resistors and Appendixes C and D for further details.

Roughly speaking, resistors are used to convert a voltage to a current, and vice versa. This may sound awfully trite, but you will soon see what we mean.

Resistors in series and parallel

From the definition of R, some simple results follow:



Figure 1.3

1. The resistance of two resistors in series (Fig. 1.3) is

$$R = R_1 + R_2$$

By putting resistors in series, you always get a *larger* resistor.

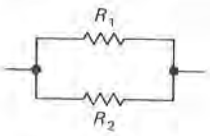


Figure 1.4

2. The resistance of two resistors in parallel (Fig. 1.4) is

$$R = \frac{R_1 R_2}{R_1 + R_2} \quad \text{or} \quad R = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}}$$

By putting resistors in parallel, you always get a *smaller* resistor. Resistance is measured in ohms (Ω), but in practice we frequently omit the Ω symbol when referring to resistors that are more than 1000Ω (1kΩ). Thus, a 10kΩ resistor is often referred to as a 10k resistor, and a 1MΩ resistor as a 1M resistor (or 1 meg). On schematic diagrams the symbol Ω is often omitted altogether. If this bores you, please have patience – we'll soon get to numerous amusing applications.

EXERCISE 1.1

You have a 5k resistor and a 10k resistor. What is their combined resistance (a) in series and (b) in parallel?

EXERCISE 1.2

If you place a 1 ohm resistor across a 12 volt car battery, how much power will it dissipate?

EXERCISE 1.3

Prove the formulas for series and parallel resistors.

EXERCISE 1.4

Show that several resistors in parallel have resistance

$$R = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \cdots}$$

A trick for parallel resistors: Beginners tend to get carried away with complicated algebra in designing or trying to understand electronics. Now is the time to begin learning intuition and shortcuts.

Shortcut no. 1 A large resistor in series (parallel) with a small resistor has the resistance of the larger (smaller) one, roughly.

Shortcut no. 2 Suppose you want the resistance of 5k in parallel with 10k. If you think of the 5k as two 10k's in parallel, then the whole circuit is like three 10k's in parallel. Because the resistance of n equal resistors in parallel is $1/n$th the resistance of the individual resistors, the answer in this case is 10k/3, or 3.33k. This trick is handy because it allows you to analyze circuits quickly in your head, without distractions. We want to encourage mental designing, or at least "back of the envelope" designing, for idea brainstorming.

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Some more home-grown philosophy: There is a tendency among beginners to want to compute resistor values and other circuit component values to many significant places, and the availability of inexpensive calculators has only made matters worse. There are two reasons you should try to avoid falling into this habit: (a) the components themselves are of finite precision (typical resistors are ±5%; the parameters that characterize transistors, say, frequently are known only to a factor of two); (b) one mark of a good circuit design is insensitivity of the finished circuit to precise values of the components (there are exceptions, of course). You'll also learn circuit intuition more quickly if you get into the habit of doing approximate calculations in your head, rather than watching meaningless numbers pop up on a calculator display.

In trying to develop intuition about resistance, some people find it helpful to think about *conductance*, $G = 1/R$. The current through a device of conductance G bridging a voltage V is then given by $I = GV$ (Ohm's law). A small resistance is a large conductance, with correspondingly large current under the influence of an applied voltage.

Viewed in this light, the formula for parallel resistors is obvious: When several resistors or conducting paths are connected across the same voltage, the total current is the sum of the individual currents. Therefore the net conductance is simply the sum of the individual conductances, $G = G_1 + G_2 + G_3 + \cdots$, which is the same as the formula for parallel resistors derived earlier.

Engineers are fond of defining reciprocal units, and they have designated the unit of conductance the siemens ($\mathrm{S} = 1/\Omega$), also known as the mho (that's ohm spelled backward, given the symbol ℧). Although the concept of conductance is helpful in developing intuition, it is not used widely; most people prefer to talk about resistance instead.

Power in resistors

The power dissipated by a resistor (or any other device) is $P = IV$. Using Ohm's law, you can get the equivalent forms $P = I^2R$ and $P = V^2/R$.

EXERCISE 1.5

Show that it is not possible to exceed the power rating of a 1/4 watt resistor of resistance greater than 1k, no matter how you connect it, in a circuit operating from a 15 volt battery.

EXERCISE 1.6

Optional exercise: New York City requires about 10^{10} watts of electrical power, at 110 volts (this is plausible: 10 million people averaging 1 kilowatt each). A heavy power cable might be an inch in diameter. Let's calculate what will happen if we try to supply the power through a cable 1 foot in diameter made of pure copper. Its resistance is $0.05\mu\Omega$ (5×10^{-8} ohms) per foot. Calculate (a) the power lost per foot from "I^2R losses," (b) the length of cable over which you will lose all 10^{10} watts, and (c) how hot the cable will get, if you know the physics involved ($\sigma = 6 \times 10^{-12}\mathrm{W/^\circ K^4 cm^2}$).

If you have done your computations correctly, the result should seem preposterous. What is the solution to this puzzle?

Input and output

Nearly all electronic circuits accept some sort of applied *input* (usually a voltage) and produce some sort of corresponding *output* (which again is often a voltage). For example, an audio amplifier might produce a (varying) output voltage that is 100 times as large as a (similarly varying) input voltage. When describing such an amplifier, we imagine measuring the output voltage for a given applied input voltage. Engineers speak of the *transfer function* H, the ratio of (measured) output divided by (applied) input; for the audio amplifier above, H is simply a constant (H = 100). We'll get to amplifiers soon enough, in the next chapter. However, with just resistors we can already look at a very important circuit fragment, the *voltage divider* (which you might call a "de-amplifier").

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1.03 Voltage dividers

We now come to the subject of the voltage divider, one of the most widespread electronic circuit fragments. Show us any real-life circuit and we'll show you half a dozen voltage dividers. To put it very simply, a voltage divider is a circuit that, given a certain voltage input, produces a predictable fraction of the input voltage as the output voltage. The simplest voltage divider is shown in Figure 1.5.

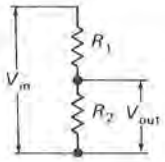


Figure 1.5. Voltage divider. An applied voltage V_{in} results in a (smaller) output voltage V_{out}.

What is V_{out}? Well, the current (same everywhere, assuming no "load" on the output) is

$$I = \frac{V_{in}}{R_1 + R_2}$$

(We've used the definition of resistance and the series law.) Then, for R_2,

$$V_{out} = IR_2 = \frac{R_2}{R_1 + R_2} V_{in}$$

Note that the output voltage is always less than (or equal to) the input voltage; that's why it's called a divider. You could get amplification (more output than input) if one of the resistances were negative. This isn't as crazy as it sounds; it is possible to make devices with negative "incremental" resistances (e.g., the tunnel diode) or even true negative resistances (e.g., the negative-impedance converter that we will talk about later in the book). However, these applications are rather specialized and need not concern you now.

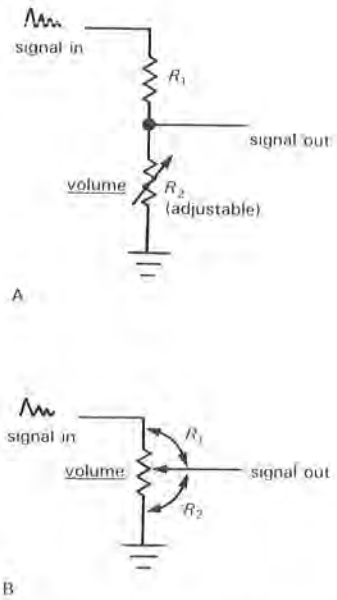


Figure 1.6. An adjustable voltage divider can be made from a fixed and variable resistor, or from a potentiometer.

Voltage dividers are often used in circuits to generate a particular voltage from a larger fixed (or varying) voltage. For instance, if V_{in} is a varying voltage and R_2 is an adjustable resistor (Fig. 1.6A), you have a "volume control"; more simply, the combination R_1R_2 can be made from a single variable resistor, or *potentiometer* (Fig. 1.6B). The humble voltage divider is even more useful, though, as a way of *thinking* about a circuit: the input voltage and upper resistance might represent the output of an amplifier, say, and the lower resistance might represent the input of the following stage. In this case the voltage-divider equation tells you how much signal gets to the input of that last stage. This will all become clearer after you know about a remarkable fact (Thévenin's theorem) that will be discussed later. First, though, a short aside on voltage sources and current sources.

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1.04 Voltage and current sources

A perfect voltage source is a two-terminal *black box* that maintains a fixed voltage drop across its terminals, regardless of load resistance. For instance, this means that it must supply a current $I = V/R$ when a resistance R is attached to its terminals. A real voltage source can supply only a finite maximum current, and in addition it generally behaves like a perfect voltage source with a small resistance in series. Obviously, the smaller this series resistance, the better. For example, a standard 9 volt alkaline battery behaves like a perfect 9 volt voltage source in series with a 3 ohm resistor and can provide a maximum current (when shorted) of 3 amps (which, however, will kill the battery in a few minutes). A voltage source "likes" an open-circuit load and "hates" a short-circuit load, for obvious reasons. (The terms "open circuit" and "short circuit" mean the obvious: An open circuit has nothing connected to it, whereas a short circuit is a piece of wire bridging the output.) The symbols used to indicate a voltage source are shown in Figure 1.7.

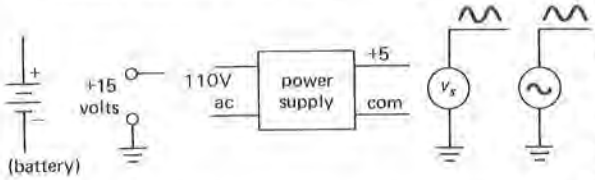


Figure 1.7. Voltage sources can be either steady (dc) or varying (ac).

A perfect current source is a two-terminal black box that maintains a constant current through the external circuit, regardless of load resistance or applied voltage. In order to do this it must be capable of supplying any necessary voltage across its terminals. Real current sources (a much-neglected subject in most textbooks) have a limit to the voltage they can provide (called the *output voltage compliance*, or just *compliance*), and in addition they do not provide absolutely constant output current. A current source "likes" a short-circuit load and "hates" an open-circuit load. The symbols used to indicate a current source are shown in Figure 1.8.

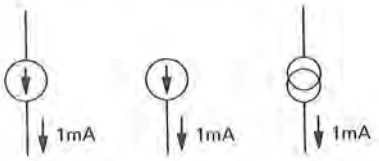


Figure 1.8. Current-source symbols.

A battery is a real-life approximation of a voltage source (there is no analog for a current source). A standard D-size flashlight cell, for instance, has a terminal voltage of 1.5 volts, an equivalent series resistance of about 1/4 ohm, and total energy capacity of about 10,000 watt-seconds (its characteristics gradually deteriorate with use; at the end of its life, the voltage may be about 1.0 volt, with an internal series resistance of several ohms). It is easy to construct voltage sources with far better characteristics, as you will learn when we come to the subject of feedback. Except in devices intended for portability, the use of batteries in electronic devices is rare. We will treat the interesting subject of low-power (battery-operated) design in Chapter 14.

MULTIMETERS

There are numerous instruments that let you measure voltages and currents in a circuit. The oscilloscope (see Appendix A) is the most versatile; it lets you "see" voltages versus time at one or more points in a circuit. Logic probes and logic analyzers are special-purpose instruments for troubleshooting digital circuits. The simple multimeter provides a good way to measure voltage,

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current, and resistance, often with good precision; however, it responds slowly, and thus it cannot replace the oscilloscope where changing voltages are of interest. Multimeters are of two varieties: those that indicate measurements on a conventional scale with a moving pointer, and those that use a digital display.

The standard VOM (volt-ohm-milliammeter) multimeter uses a meter movement that measures current (typically 50μA full scale). (See a less-design-oriented electronics book for pretty pictures of the innards of meter movements; for our purposes, it suffices to say that it uses coils and magnets.) To measure voltage, the VOM puts a resistor in series with the basic movement. For instance, one kind of VOM will generate a 1 volt (full-scale) range by putting a 20k resistor in series with the standard 50μA movement; higher voltage ranges use correspondingly larger resistors. Such a VOM is specified as 20,000 ohms/volt, meaning that it looks like a resistor whose value is 20k multiplied by the full-scale voltage of the particular range selected. Full scale on any voltage range is 1/20,000, or 50μA. It should be clear that one of these voltmeters disturbs a circuit less on a higher range, since it looks like a higher resistance (think of the voltmeter as the lower leg of a voltage divider, with the Thévenin resistance of the circuit you are measuring as the upper resistor). Ideally, a voltmeter should have infinite input resistance.

Nowadays there are various meters with some electronic amplification whose input resistance may be as large as 10^9 ohms. Most digital meters, and even a number of analog-reading meters that use FETs (field-effect transistors, see Chapter 3), are of this type. Warning: Sometimes the input resistance of FET-input meters is very high on the most sensitive ranges, dropping to a lower resistance for the higher ranges. For instance, an input resistance of 10^9 ohms on the 0.2 volt and 2 volt ranges, and 10^7 ohms on all higher ranges, is typical. Read the specifications carefully! For measurements on most transistor circuits, 20,000 ohms/volt is fine, and there will be little loading effect on the circuit by the meter. In any case, it is easy to calculate how serious the effect is by using the voltage-divider equation. Typically, multimeters provide voltage ranges from a volt (or less) to a kilovolt (or more), full scale.

A VOM can be used to measure current by simply using the bare meter movement (for our preceding example, this would give a range of 50μA full scale) or by shunting (paralleling) the movement with a small resistor. Because the meter movement itself requires a small voltage drop, typically 0.25 volt, to produce a full-scale deflection, the shunt is chosen by the meter manufacturer (all you do is set the range switch to the range you want) so that the full-scale current will produce that voltage drop through the parallel combination of the meter resistance and the shunt resistance. Ideally, a current-measuring meter should have zero resistance in order not to disturb the circuit under test, since it must be put in series with the circuit. In practice, you tolerate a few tenths of a volt drop (sometimes called "voltage burden") with both VOMs and digital multimeters. Typically, multimeters provide current ranges from 50μA (or less) to an amp (or more), full scale.

Multimeters also have one or more batteries in them to power the resistance measurement. By supplying a small current and measuring the voltage drop, they measure resistance, with several ranges to cover values from an ohm (or less) to 10 megohms (or more).

Important: Don't try to measure "the current of a voltage source," for instance by sticking the meter across the wall plug; the same applies for ohms. This is the leading cause of blown-out meters.

EXERCISE 1.7

What will a 20,000 ohms/volt meter read, on its 1 volt scale, when attached to a 1 volt source with an internal resistance of 10k? What will it read when attached to a 10k–10k voltage divider driven by a "stiff" (zero source resistance) 1 volt source?

EXERCISE 1.8

A 50μA meter movement has an internal resistance of 5k. What shunt resistance is needed to convert it to a 0–1 amp meter? What series resistance will convert it to a 0–10 volt meter?

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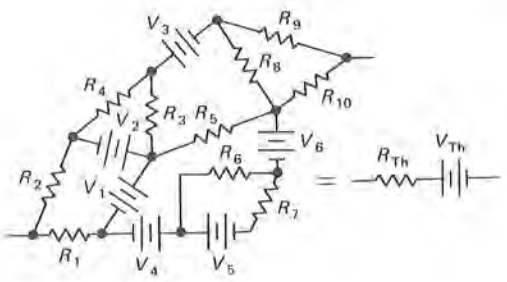


Figure 1.9

1.05 Thévenin's equivalent circuit

Thévenin's theorem states that any two-terminal network of resistors and voltage sources is equivalent to a single resistor R in series with a single voltage source V. This is remarkable. Any mess of batteries and resistors can be mimicked with one battery and one resistor (Fig. 1.9). (Incidentally, there's another theorem, Norton's theorem, that says you can do the same thing with a current source in parallel with a resistor.)

How do you figure out the Thévenin equivalent R_{Th} and V_{Th} for a given circuit? Easy! V_{Th} is the open-circuit voltage of the Thévenin equivalent circuit; so if the two circuits behave identically, it must also be the open-circuit voltage of the given circuit (which you get by calculation, if you know what the circuit is, or by measurement, if you don't). Then you find R_{Th} by noting that the short-circuit current of the equivalent circuit is $V_{\text{Th}}/R_{\text{Th}}$. In other words,

$$V_{\text{Th}} = V \text{ (open circuit)}$$

$$R_{\text{Th}} = \frac{V \text{ (open circuit)}}{I \text{ (short circuit)}}$$

Let's apply this method to the voltage divider, which must have a Thévenin equivalent:

1. The open-circuit voltage is

$$V = V_{\text{in}} \frac{R_2}{R_1 + R_2}$$

2. The short-circuit current is

$$V_{\text{in}}/R_1$$

So the Thévenin equivalent circuit is a voltage source

$$V_{\text{Th}} = V_{\text{in}} \frac{R_2}{R_1 + R_2}$$

in series with a resistor

$$R_{\text{Th}} = \frac{R_1 R_2}{R_1 + R_2}$$

(It is not a coincidence that this happens to be the parallel resistance of R_1 and R_2. The reason will become clear later.)

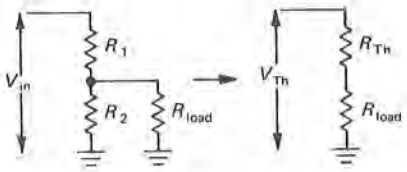


Figure 1.10

From this example it is easy to see that a voltage divider is not a very good battery, in the sense that its output voltage drops severely when a load is attached. As an example, consider Exercise 1.9. You now know everything you need to know to calculate exactly how much the output will drop for a given load resistance: Use the Thévenin equivalent circuit, attach a load, and calculate the new output, noting that the new circuit is nothing but a voltage divider (Fig. 1.10).

EXERCISE 1.9

For the circuit shown in Figure 1.10, with $V_{\text{in}} =$ 30V and $R_1 = R_2 =$ 10k, find (a) the output voltage with no load attached (the open-circuit voltage); (b) the output voltage with a 10k load (treat as voltage divider, with R_2 and R_{load} combined into a single resistor); (c) the Thévenin equivalent circuit; (d) the same as in part b, but using the Thévenin equivalent circuit (again, you wind up with a voltage divider; the answer should agree with the result in part b); (e) the power dissipated in each of the resistors.

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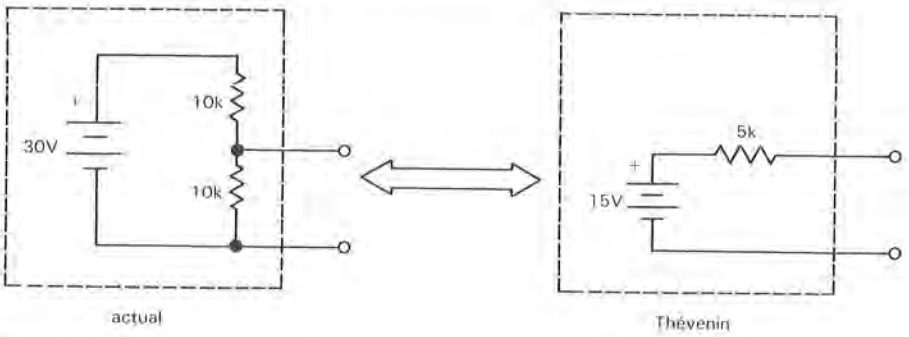


Figure 1.11

Equivalent source resistance and circuit loading

As you have just seen, a voltage divider powered from some fixed voltage is equivalent to some smaller voltage source in series with a resistor; for example, the output terminals of a 10k–10k voltage divider driven by a perfect 30 volt battery are precisely equivalent to a perfect 15 volt battery in series with a 5k resistor (Fig. 1.11). Attaching a load resistor causes the voltage divider's output to drop, owing to the finite *source resistance* (Thévenin equivalent resistance of the voltage divider output, viewed as a source of voltage). This is often undesirable. One solution to the problem of making a stiff voltage source ("stiff" is used in this context to describe something that doesn't bend under load) might be to use much smaller resistors in a voltage divider. Occasionally this brute-force approach is useful. However, it is usually best to construct a voltage source, or power supply, as it's commonly called, using active components like transistors or operational amplifiers, which we will treat in Chapters 2–4. In this way you can easily make a voltage source with internal (Thévenin equivalent) resistance measured in milliohms (thousandths of an ohm), without the large currents and dissipation of power characteristic of a low-resistance voltage divider delivering the same performance. In addition, with an active power supply it is easy to make the output voltage adjustable.

The concept of equivalent internal resistance applies to all sorts of sources, not just batteries and voltage dividers. Signal sources (e.g., oscillators, amplifiers, and sensing devices) all have an equivalent internal resistance. Attaching a load whose resistance is less than or even comparable to the internal resistance will reduce the output considerably. This undesirable reduction of the open-circuit voltage (or signal) by the load is called "circuit loading." Therefore, you should strive to make $R_{\text{load}} \gg R_{\text{internal}}$, because a high-resistance load has little attenuating effect on the source (Fig. 1.12). You will see numerous circuit examples in the chapters ahead. This high-resistance condition ideally

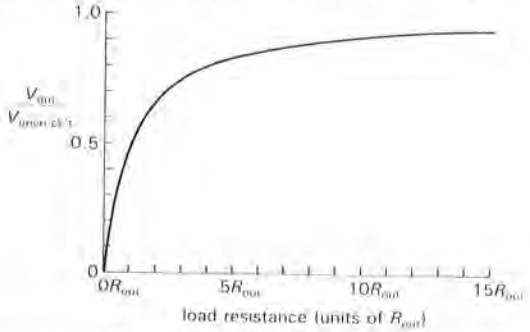


Figure 1.12. To avoid attenuating a signal source below its open-circuit voltage, keep the load resistance large compared with the output resistance.

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characterizes measuring instruments such as voltmeters and oscilloscopes. (There are exceptions to this general principle; for example, we will talk about transmission lines and radiofrequency techniques, where you must "match impedances" in order to prevent the reflection and loss of power.)

A word on language: You frequently hear things like "the resistance looking into the voltage divider," or "the output sees a load of so-and-so many ohms," as if circuits had eyes. It's OK (in fact, it's a rather good way to keep straight which resistance you're talking about) to say what part of the circuit is doing the "looking."

Power transfer

Here is an interesting problem: What load resistance will result in maximum power being transferred to the load for a given source resistance? (The terms *source resistance, internal resistance,* and *Thévenin equivalent resistance* all mean the same thing.) It is easy to see that both $R_{\text{load}} = 0$ and $R_{\text{load}} = \infty$ result in zero power transferred, because $R_{\text{load}} = 0$ means that $V_{\text{load}} = 0$ and $I_{\text{load}} = V_{\text{source}}/R_{\text{source}}$, so that $P_{\text{load}} = V_{\text{load}}I_{\text{load}} = 0$. But $R_{\text{load}} = \infty$ means that $V_{\text{load}} = V_{\text{source}}$ and $I_{\text{load}} = 0$, so that $P_{\text{load}} = 0$. There has to be a maximum in between.

EXERCISE 1.10

Show that $R_{\text{load}} = R_{\text{source}}$ maximizes the power in the load for a given source resistance. Note: Skip this exercise if you don't know calculus, and take it on faith that the answer is true.

Lest this example leave the wrong impression, we would like to emphasize again that circuits are ordinarily designed so that the load resistance is much greater than the source resistance of the signal that drives the load.

1.06 Small-signal resistance

We often deal with electronic devices for which I is not proportional to V; in such cases there's not much point in talking about resistance, since the ratio V/I will depend on V, rather than being a nice constant, independent of V. For these devices it is useful to know the slope of the V–I curve, in other words, the ratio of a small change in applied voltage to the resulting change in current through the device, $\Delta V/\Delta I$ (or dV/dI). This quantity has the units of resistance (ohms) and substitutes for resistance in many calculations. It is called the small-signal resistance, incremental resistance, or dynamic resistance.

Zener diodes

As an example, consider the *zener diode*, which has the V–I curve shown in Figure 1.13. Zeners are used to create a constant voltage inside a circuit somewhere, simply by providing them with a (roughly constant) current derived from a higher voltage within the circuit. For example, the zener diode in Figure 1.13 will convert an applied current in the range shown to a corresponding (but narrower) range of voltages. It is important to know how the resulting zener voltage will change with applied current; this is a measure of its "regulation" against changes in the driving current provided to it. Included in the specifications of a zener will be its dynamic resistance, given at a certain current. (Useful fact: the dynamic resistance of a zener diode varies roughly in inverse proportion to current.) For example, a zener might have a dynamic resistance of 10 ohms at 10mA, at its zener voltage of 5 volts. Using the definition of dynamic resistance, we find that a 10% change in applied current will therefore result in a change in voltage of

$$\Delta V = R_{\text{dyn}}\Delta I = 10 \times 0.1 \times 0.01 = 10\text{mV}$$

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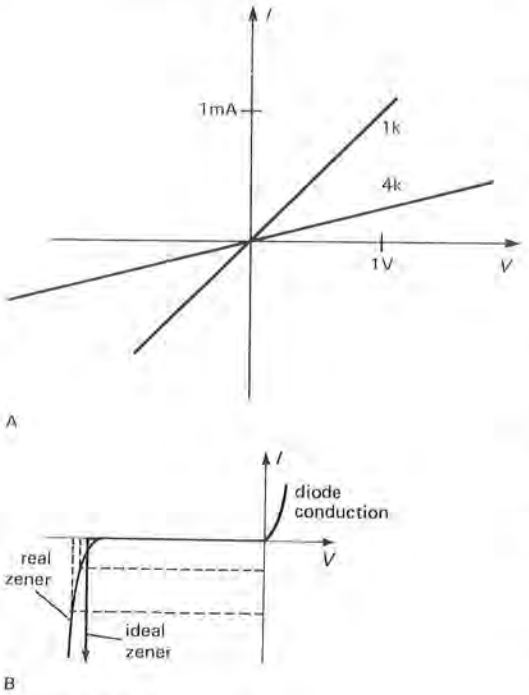


Figure 1.13. *V–I* curves.
A. Resistor (linear).
B. Zener diode (nonlinear).

or

$$\Delta V/V = 0.002 = 0.2\%$$

thus demonstrating good voltage-regulating ability. In this sort of application you frequently get the zener current through a resistor from a higher voltage available somewhere in the circuit, as in Figure 1.14.

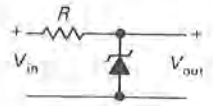


Figure 1.14. Zener regulator.

Then,

$$I = \frac{V_{\text{in}} - V_{\text{out}}}{R}$$

and

$$\Delta I = \frac{\Delta V_{\text{in}} - \Delta V_{\text{out}}}{R}$$

so

$$\Delta V_{\text{out}} = R_{\text{dyn}}\Delta I = \frac{R_{\text{dyn}}}{R}(\Delta V_{\text{in}} - \Delta V_{\text{out}})$$

and finally

$$\Delta V_{\text{out}} = \frac{R_{\text{dyn}}}{R + R_{\text{dyn}}}\Delta V_{\text{in}}$$

Thus, for *changes* in voltage, the circuit behaves like a voltage divider, with the zener replaced by a resistor equal to its dynamic resistance at the operating current. This is the utility of incremental resistance. For instance, suppose in the preceding circuit we have an input voltage ranging between 15 and 20 volts and use a 1N4733 (5.1V 1W zener diode) in order to generate a stable 5.1 volt power supply. We choose $R = 300$ ohms, for a maximum zener current of 50mA: (20 − 5.1)/300. We can now estimate the output voltage regulation (variation in output voltage), knowing that this particular zener has a specified maximum dynamic impedance of 7.0 ohms at 50mA. The zener current varies from 50mA to 33mA over the input voltage range; this 17mA change in current then produces a voltage change at the output of $\Delta V = R_{\text{dyn}}\Delta I$, or 0.12 volt. You will see more of zeners in Sections 2.04 and 6.14.

In real life, a zener will provide better regulation if driven by a current source, which has, by definition, $R_{\text{incr}} = \infty$ (same current regardless of voltage). But current sources are more complex, and therefore in practice we often resort to the humble resistor.

Tunnel diodes

Another interesting application of incremental resistance is the *tunnel diode*, sometimes called the Esaki diode. Its *V–I* curve is shown in Figure 1.15. In the region from *A* to *B* it has *negative* incremental resistance. This has a remarkable consequence: A voltage *divider* made with a resistor and

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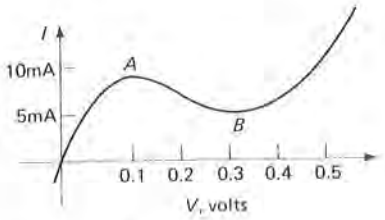


Figure 1.15

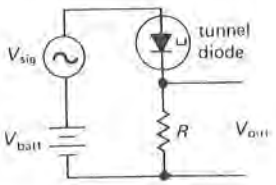


Figure 1.16

a tunnel diode can actually be an *amplifier* (Fig. 1.16). For a wiggly voltage v_{sig}, the voltage divider equation gives us

$$v_{\text{out}} = \frac{R}{R + r_t} v_{\text{sig}}$$

where r_t is the incremental resistance of the tunnel diode at the operating current, and the lower-case symbol v_{sig} stands for a small-signal variation, which we have been calling ΔV_{sig} up to now (we will adopt this widely used convention from now on). The tunnel diode has $r_{t(\text{incr})} < 0$. That is,

$$\Delta V/\Delta I \quad (\text{or } v/i) \quad < \quad 0$$

from A to B on the characteristic curve. If $r_{t(\text{incr})} \approx R$, the denominator is nearly zero, and the circuit amplifies. V_{batt} provides the steady current, or *bias*, to bring the operating point into the region of negative resistance. (Of course, it is always necessary to have a source of power in any device that amplifies.)

A postmortem on these fascinating devices: When tunnel diodes first appeared, late in the 1950s, they were hailed as the solution to a great variety of circuit problems. Because they were fast, they were supposed to revolutionize computers, for instance. Unfortunately, they are difficult devices to use; this fact, combined with stunning improvements in transistors, has made tunnel diodes almost obsolete.

The subject of negative resistance will come up again later, in connection with active filters. There you will see a circuit called a negative-impedance converter that can produce (among other things) a pure negative resistance (not just incremental). It is made with an operational amplifier and has very useful properties.

SIGNALS

A later section in this chapter will deal with capacitors, devices whose properties depend on the way the voltages and currents in a circuit are *changing*. Our analysis of dc circuits so far (Ohm's law, Thévenin equivalent circuits, etc.) still holds, even if the voltages and currents are changing in time. But for a proper understanding of alternating-current (ac) circuits, it is useful to have in mind certain common types of *signals*, voltages that change in time in a particular way.

1.07 Sinusoidal signals

Sinusoidal signals are the most popular signals around; they're what you get out of the wall plug. If someone says something like "take a 10 microvolt signal at 1 megahertz," he means a sine wave. Mathematically, what you have is a voltage described by

$$V = A \sin 2\pi f t$$

where A is called the amplitude, and f is the frequency in cycles per second, or hertz. A sine wave looks like the wave shown in Figure 1.17. Sometimes it is important to know the value of the signal at some arbitrary time $t = 0$, in which case you may see a *phase* ϕ in the expression:

$$V = A \sin(2\pi f t + \phi)$$

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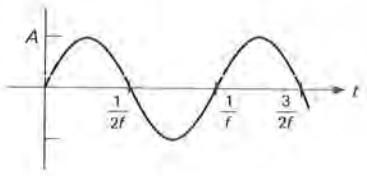


Figure 1.17. Sine wave of amplitude A and frequency f.

The other variation on this simple theme is the use of *angular frequency*, which looks like this:

$$V = A \sin \omega t$$

Here, ω is the angular frequency in radians per second. Just remember the important relation $\omega = 2\pi f$ and you won't go wrong.

The great merit of sine waves (and the cause of their perennial popularity) is the fact that they are the solutions to certain linear differential equations that happen to describe many phenomena in nature as well as the properties of linear circuits. A linear circuit has the property that its output, when driven by the sum of two input signals, equals the sum of its individual outputs when driven by each input signal in turn; i.e., if $O(A)$ represents the output when driven by signal A, then a circuit is linear if $O(A + B) = O(A) + O(B)$. A linear circuit driven by a sine wave always responds with a sine wave, although in general the phase and amplitude are changed. No other signal can make this statement. It is standard practice, in fact, to describe the behavior of a circuit by its *frequency response*, the way it alters the amplitude of an applied sine wave as a function of frequency. A high-fidelity amplifier, for instance, should be characterized by a "flat" frequency response over the range 20Hz to 20kHz, at least.

The sine-wave frequencies you will usually deal with range from a few hertz to a few megahertz. Lower frequencies, down to 0.0001Hz or lower, can be generated with carefully built circuits, if needed. Higher frequencies, e.g., up to 2000MHz, can be generated, but they require special transmission-line techniques. Above that, you're dealing with microwaves, where conventional wired circuits with lumped circuit elements become impractical, and exotic waveguides or "striplines" are used instead.

1.08 Signal amplitudes and decibels

In addition to its amplitude, there are several other ways to characterize the magnitude of a sine wave or any other signal. You sometimes see it specified by *peak-to-peak amplitude* (pp amplitude), which is just what you would guess, namely, twice the amplitude. The other method is to give the *root-mean-square amplitude* (rms amplitude), which is $V_{\text{rms}} = (1/\sqrt{2})A = 0.707A$ (this is for sine waves only; the ratio of pp to rms will be different for other waveforms). Odd as it may seem, this is the usual method, because rms voltage is what's used to compute power. The voltage across the terminals of a wall socket (in the United States) is 117 volts rms, 60Hz. The *amplitude* is 165 volts (330 volts pp).

Decibels

How do you compare the relative amplitudes of two signals? You could say, for instance, that signal X is twice as large as signal Y. That's fine, and useful for many purposes. But because we often deal with ratios as large as a million, it is easier to use a logarithmic measure, and for this we present the decibel (it's one-tenth as large as something called a bel, which no one ever uses). By definition, the ratio of two signals, in decibels, is

$$\text{dB} = 20 \log_{10} \frac{A_2}{A_1}$$

where A_1 and A_2 are the two signal amplitudes. So, for instance, one signal of twice the amplitude of another is +6dB relative

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to it, since $\log_{10}2 = 0.3010$. A signal 10 times as large is +20dB; a signal one-tenth as large is −20dB. It is also useful to express the ratio of two signals in terms of power levels:

$$\text{dB} = 10 \log_{10} \frac{P_2}{P_1}$$

where P_1 and P_2 represent the power in the two signals. As long as the two signals have the same kind of waveform, e.g., sine waves, the two definitions give the same result. When comparing unlike waveforms, e.g., a sine wave versus "noise," the definition in terms of power (or the amplitude definition, with rms amplitudes substituted) must be used.

Although decibels are ordinarily used to specify the ratio of two signals, they are sometimes used as an absolute measure of amplitude. What is happening is that you are assuming some reference signal amplitude and expressing any other amplitude in decibels relative to it. There are several standard amplitudes (which are unstated, but understood) that are used in this way; the most common references are (a) dBV; 1 volt rms; (b) dBm; the voltage corresponding to 1mW into some assumed load impedance, which for radiofrequencies is usually 50 ohms, but for audio is often 600 ohms (the corresponding 0dBm amplitudes, when loaded by those impedances, are then 0.22V rms and 0.78V rms); and (c) the small noise voltage generated by a resistor at room temperature (this surprising fact is discussed in Section 7.11). In addition to these, there are reference amplitudes used for measurements in other fields. For instance, in acoustics, 0dB SPL is a wave whose rms pressure is 0.0002μbar (a bar is 10^6 dynes per square centimeter, approximately 1 atmosphere); in communications, levels can be stated in dBrnC (relative noise reference weighted in frequency by "curve C"). When stating amplitudes this way, it is best to be specific about the 0dB reference amplitude; say something like "an amplitude of 27 decibels relative to 1 volt rms," or abbreviate "27 dB re 1V rms," or define a term like "dBV."

EXERCISE 1.11

Determine the voltage and power ratios for a pair of signals with the following decibel ratios: (a) 3dB, (b) 6dB, (c) 10dB, (d) 20dB.

1.09 Other signals

The ramp is a signal that looks like the signal shown in Figure 1.18. It is simply a voltage rising (or falling) at a constant rate. That can't go on forever, of course, even in science fiction movies. It is sometimes approximated by a finite ramp (Fig. 1.19) or by a periodic ramp, or sawtooth (Fig. 1.20).

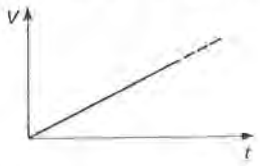


Figure 1.18. Voltage ramp waveform.

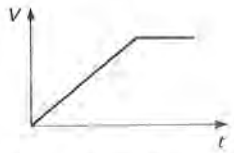


Figure 1.19. Ramp with limit.

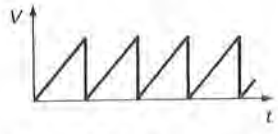


Figure 1.20. Sawtooth wave.

Triangle

The triangle wave is a close cousin of the ramp; it is simply a symmetrical ramp (Fig. 1.21).

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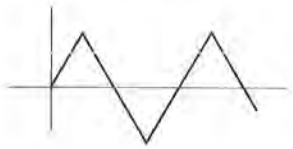


Figure 1.21. Triangle wave.



Figure 1.22. Noise.

Noise

Signals of interest are often mixed with *noise*; this is a catchall phrase that usually applies to random noise of thermal origin. Noise voltages can be specified by their frequency spectrum (power per hertz) or by their amplitude distribution. One of the most common kinds of noise is *band-limited white Gaussian noise*, which means a signal with equal power per hertz in some band of frequencies and a Gaussian (bell-shaped) distribution of amplitudes if large numbers of instantaneous measurements of its amplitude are made. This kind of noise is generated by a resistor (Johnson noise), and it plagues sensitive measurements of all kinds. On an oscilloscope it appears as shown in Figure 1.22. We will study noise and low-noise techniques in some detail in Chapter 7. Sections 9.32–9.37 deal with noise-generation techniques.

Square waves

A square wave is a signal that varies in time as shown in Figure 1.23. Like the sine wave, it is characterized by amplitude and frequency. A linear circuit driven by a square wave rarely responds with a square wave. For a square wave, the rms amplitude equals the amplitude.

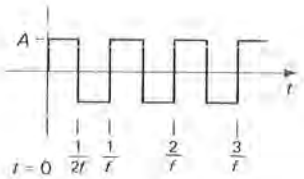


Figure 1.23. Square wave.

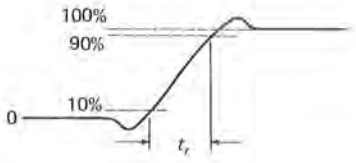


Figure 1.24. Rise time of a step waveform.

The edges of a square wave are not perfectly square; in typical electronic circuits the rise time t_r ranges from a few nanoseconds to a few microseconds. Figure 1.24 shows the sort of thing usually seen. The rise time is defined as the time required for the signal to go from 10% to 90% of its total transition.

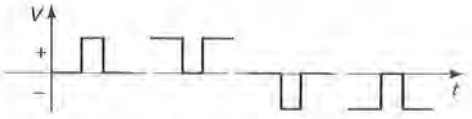


Figure 1.25. Positive- and negative-going pulses of both polarities.

Pulses

A pulse is a signal that looks as shown in Figure 1.25. It is defined by amplitude and pulse width. You can generate a train of periodic (equally spaced) pulses, in which case you can talk about the frequency, or pulse repetition rate, and the "duty cycle," the ratio of pulse width to repetition period (duty cycle ranges from zero to 100%). Pulses can have positive or negative polarity; in addition, they can be "positive-going" or "negative-going." For instance, the second pulse in Figure 1.25

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is a negative-going pulse of positive polarity.



Figure 1.26

Steps and spikes

Steps and spikes are signals that are talked about a lot but are not often used. They provide a nice way of describing what happens in a circuit. If you could draw them, they would look something like the example in Figure 1.26. The step function is part of a square wave; the spike is simply a jump of vanishingly short duration.

1.10 Logic levels

Pulses and square waves are used extensively in digital electronics, where predefined voltage levels represent one of two possible states present at any point in the circuit. These states are called simply HIGH and LOW and correspond to the 0 (false) and 1 (true) states of Boolean logic (the algebra that describes such two-state systems).

Precise voltages are not necessary in digital electronics. You need only to distinguish which of the two possible states is present. Each digital logic family therefore specifies legal HIGH and LOW states. For example, the "74HC" digital logic family runs from a single +5 volt supply, with output levels that are typically 0 volts (LOW) and 5 volts (HIGH), and an input decision threshold of 2.5 volts. Actual outputs can be as much as a volt from ground or +5 volts without malfunction, however. We'll have much more to say about logic levels in Chapters 8 and 9.

1.11 Signal sources

Often the source of a signal is some part of the circuit you are working on. But for test purposes a flexible signal source is invaluable. They come in three flavors: signal generators, pulse generators, and function generators.

Signal generators

Signal generators are sine-wave oscillators, usually equipped to give a wide range of frequency coverage (50kHz to 50MHz is typical), with provision for precise control of amplitude (using a resistive divider network called an *attenuator*). Some units let you *modulate* the output (see Chapter 13). A variation on this theme is the *sweep generator*, a signal generator that can sweep its output frequency repeatedly over some range. These are handy for testing circuits whose properties vary with frequency in a particular way, e.g., "tuned circuits" or filters. Nowadays these devices, as well as many test instruments, are available in configurations that allow you to program the frequency, amplitude, etc., from a computer or other digital instrument.

A variation on the signal generator is the *frequency synthesizer*, a device that generates sine waves whose frequencies can be set precisely. The frequency is set digitally, often to eight significant figures or more, and is internally synthesized from a precise standard (a quartz-crystal oscillator) by digital methods we will discuss later (Sections 9.27–9.31). If your requirement is for no-nonsense accurate frequency generation, you can't beat a synthesizer.

Pulse generators

Pulse generators only make pulses, but what pulses! Pulse width, repetition rate, amplitude, polarity, rise time, etc., may all be adjustable. In addition, many units allow you to generate pulse pairs, with settable spacing and repetition rate, or even coded pulse trains. Most modern pulse

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generators are provided with logic-level outputs for easy connection to digital circuitry. Like signal generators, these come in the programmable variety.

Function generators

In many ways function generators are the most flexible signal sources of all. You can make sine, triangle, and square waves over an enormous frequency range (0.01 Hz to 10 MHz is typical), with control of amplitude and dc offset (a constant dc voltage added to the signal). Many of them have provision for frequency sweeping, often in several modes (linear or logarithmic frequency variation versus time). They are available with pulse outputs (although not with the flexibility you get with a pulse generator), and some of them have provision for modulation.

Like the other signal sources, function generators come in programmable versions and versions with digital readout of frequency (and sometimes amplitude). The most recent addition to the function-generator family is the synthesized function generator, a device that combines all the flexibility of a function generator with the stability and accuracy of a frequency synthesizer. An example is the HP 8116A, with sine, square, and triangle waves (as well as pulses, ramps, haversines, etc.) from 0.001Hz to 50MHz. Frequency and amplitude (10mV to 16V pp) are programmable, as are linear and logarithmic frequency sweeps. This unit also provides trigger, gate, burst, FM, AM, pulse-width modulation, voltage-controlled frequency, and single cycles. For general use, if you can have only one signal source, the function generator is for you.

CAPACITORS AND AC CIRCUITS

Once we enter the world of changing voltages and currents, or signals, we encounter two very interesting circuit elements that are useless in dc circuits: capacitors and inductors. As you will see, these humble devices, combined with resistors, complete the triad of passive linear circuit elements that form the basis of nearly all circuitry. Capacitors, in particular, are essential in nearly every circuit application. They are used for waveform generation, filtering, and blocking and bypass applications. They are used in integrators and differentiators. In combination with inductors, they make possible sharp filters for separating desired signals from background. You will see some of these applications as we continue with this chapter, and there will be numerous interesting examples in later chapters.

Let's proceed, then, to look at capacitors in detail. Portions of the treatment that follows are necessarily mathematical in nature; the reader with little mathematical preparation may find Appendix B helpful. In any case, an understanding of the details is less important in the long run than an understanding of the results.



Figure 1.27. Capacitor.

1.12 Capacitors

A capacitor (Fig. 1.27) (the old-fashioned name was *condenser*) is a device that has two wires sticking out of it and has the property

$$Q = CV$$

A capacitor of C farads with V volts across its terminals has Q coulombs of stored charge on one plate, and $-Q$ on the other.

To a first approximation, capacitors are devices that might be considered simply frequency-dependent resistors. They allow you to make frequency-dependent voltage dividers, for instance. For some applications (bypass, coupling) this is

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almost all you need to know, but for other applications (filtering, energy storage, resonant circuits) a deeper understanding is needed. For example, capacitors cannot dissipate power, even though current can flow through them, because the voltage and current are 90° out of phase.

Taking the derivative of the defining equation above (see Appendix B), you get

$$I = C\frac{dV}{dt}$$

So a capacitor is more complicated than a resistor; the current is not simply proportional to the voltage, but rather to the rate of change of voltage. If you change the voltage across a farad by 1 volt per second, you are supplying an amp. Conversely, if you supply an amp, its voltage changes by 1 volt per second. A farad is very large, and you usually deal in microfarads (μF) or picofarads (pF). (To make matters confusing to the uninitiated, the units are often omitted on capacitor values specified in schematic diagrams. You have to figure it out from the context.) For instance, if you supply a current of 1mA to 1μF, the voltage will rise at 1000 volts per second. A 10ms pulse of this current will increase the voltage across the capacitor by 10 volts (Fig. 1.28).

Capacitors come in an amazing variety of shapes and sizes; with time, you will come to recognize their more common incarnations. The basic construction is simply two conductors near each other (but not touching); in fact, the simplest capacitors are just that. For greater capacitance, you need more area and closer spacing; the usual approach is to plate some conductor onto a thin insulating material (called a dielectric), for instance, aluminized Mylar film rolled up into a small cylindrical configuration. Other popular types are thin ceramic wafers (disc ceramics), metal foils with oxide insulators (electrolytics), and metallized mica. Each of these types has unique properties; for a brief rundown, see the box on capacitors. In general, ceramic and Mylar types are used for most noncritical circuit applications; tantalum capacitors are used where greater capacitance is needed, and electrolytics are used for power-supply filtering.

Capacitors in parallel and series

The capacitance of several capacitors in parallel is the sum of their individual capacitances. This is easy to see: Put voltage V across the parallel combination; then

$$\begin{aligned} C_{\text{total}}V = Q_{\text{total}} &= Q_1 + Q_2 + Q_3 + \dots \\ &= C_1V + C_2V + C_3V + \dots \\ &= (C_1 + C_2 + C_3 + \dots)V \end{aligned}$$

or

$$C_{\text{total}} = C_1 + C_2 + C_3 + \dots$$

For capacitors in series, the formula is like that for resistors in parallel:

$$C_{\text{total}} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \dots}$$

or (two capacitors only)

$$C_{\text{total}} = \frac{C_1C_2}{C_1 + C_2}$$

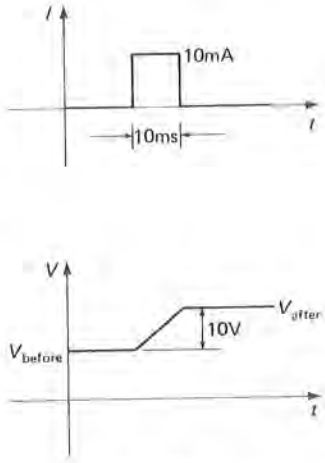


Figure 1.28. The voltage across a capacitor changes when a current flows through it.

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CAPACITORS

There is wide variety among the capacitor types available. This is a quickie guide to point out their major advantages and disadvantages. Our judgments should be considered somewhat subjective:

Type	Capacitance range	Maximum voltage	Accuracy	Temperature stability	Leakage	Comments
Mica	1pF–0.01μF	100–600	Good		Good	Excellent; good at RF
Tubular ceramic	0.5pF–100pF	100–600		Selectable		Several tempcos (including zero)
Ceramic	10pF–1μF	50–30,000	Poor	Poor	Moderate	Small, inexpensive, very popular
Polyester (Mylar)	0.001μF–50μF	50–600	Good	Poor	Good	Inexpensive, good, popular
Polystyrene	10pF–2.7μF	100–600	Excellent	Good	Excellent	High quality, large; signal filters
Polycarbonate	100pF–30μF	50–800	Excellent	Excellent	Good	High quality, small
Polypropylene	100pF–50μF	100–800	Excellent	Good	Excellent	High quality, low dielectric absorption
Teflon	1000pF–2μF	50–200	Excellent	Best	Best	High quality, lowest dielectric absorption
Glass	10pF–1000pF	100–600	Good		Excellent	Long-term stability
Porcelain	100pF–0.1μF	50–400	Good	Good	Good	Good long-term stability
Tantalum	0.1μF–500μF	6–100	Poor	Poor		High capacitance; polarized, small; low inductance
Electrolytic	0.1μF–1.6F	3–600	Terrible	Ghastly	Awful	Power-supply filters; polarized; short life
Double layer	0.1F–10F	1.5–6	Poor	Poor	Good	Memory backup; high series resistance
Oil	0.1μF–20μF	200–10,000			Good	High-voltage filters; large, long life
Vacuum	1pF–5000pF	2000–36,000			Excellent	Transmitters

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EXERCISE 1.12
Derive the formula for the capacitance of two capacitors in series. Hint: Because there is no external connection to the point where the two capacitors are connected together, they must have equal stored charges.

The current that flows in a capacitor during charging ($I = CdV/dt$) has some unusual features. Unlike resistive current, it's not proportional to voltage, but rather to the rate of change (the "time derivative") of voltage. Furthermore, unlike the situation in a resistor, the power (V times I) associated with capacitive current is not turned into heat, but is stored as energy in the capacitor's internal electric field. You get all that energy back when you discharge the capacitor. We'll see another way to look at these curious properties when we talk about *reactance*, beginning in Section 1.18.

1.13 *RC* circuits: *V* and *I* versus time

When dealing with ac circuits (or, in general, any circuits that have changing voltages and currents), there are two possible approaches. You can talk about V and I versus time, or you can talk about amplitude versus signal frequency. Both approaches have their merits, and you find yourself switching back and forth according to which description is most convenient in each situation. We will begin our study of ac circuits in the time domain. Beginning with Section 1.18, we will tackle the frequency domain.

What are some of the features of circuits with capacitors? To answer this question, let's begin with the simple RC circuit (Fig. 1.29). Application of the capacitor rules gives

$$C\frac{dV}{dt} = I = -\frac{V}{R}$$

This is a differential equation, and its solution is

$$V = Ae^{-t/RC}$$

So a charged capacitor placed across a resistor will discharge as in Figure 1.30.

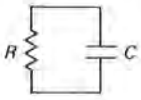


Figure 1.29

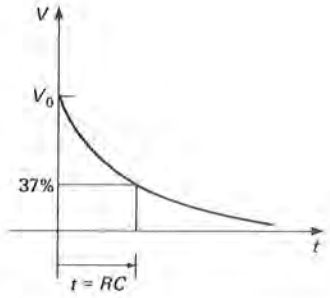


Figure 1.30. RC discharge waveform.

Time constant

The product RC is called the *time constant* of the circuit. For R in ohms and C in farads, the product RC is in seconds. A microfarad across 1.0k has a time constant of 1ms; if the capacitor is initially charged to 1.0 volt, the initial current is 1.0mA.

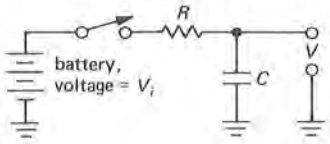


Figure 1.31

Figure 1.31 shows a slightly different circuit. At time $t = 0$, someone connects the battery. The equation for the circuit is then

$$I = C\frac{dV}{dt} = \frac{V_i - V}{R}$$

with the solution

$$V = V_i + Ae^{-t/RC}$$

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(Please don't worry if you can't follow the mathematics. What we are doing is getting some important results, which you should remember. Later we will use the results often, with no further need for the mathematics used to derive them.) The constant A is determined by initial conditions (Fig. 1.32): $V = 0$ at $t = 0$; therefore, $A = -V_i$, and

$$V = V_i(1 - e^{-t/RC})$$

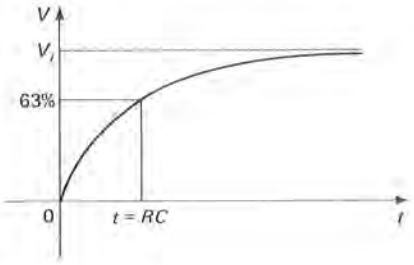


Figure 1.32

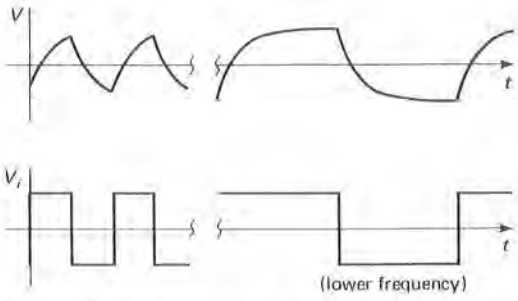


Figure 1.33. Output (top waveform) across a capacitor, when driven by square waves through a resistor.

Decay to equilibrium

Eventually (when $t \gg RC$), V reaches V_i. (Presenting the "$5RC$ rule of thumb": a capacitor charges or decays to within 1% of its final value in 5 time constants.) If we then change V_0 to some other value (say, 0), V will decay toward that new value with an exponential $e^{-t/RC}$. For example, a square-wave input for V_0 will produce the output shown in Figure 1.33.

EXERCISE 1.13

Show that the rise time (the time required to go from 10% to 90% of its final value) of this signal is $2.2RC$.

You might ask the obvious next question: What about $V(t)$ for arbitrary $V_i(t)$? The solution involves an inhomogeneous differential equation and can be solved by standard methods (which are, however, beyond the scope of this book). You would find

$$V(t) = \frac{1}{RC}\int_{-\infty}^{t} V_i(\tau)e^{-(t-\tau)/RC}d\tau$$

That is, the RC circuit averages past history at the input with a weighting factor

$$e^{-\Delta t/RC}$$

In practice, you seldom ask this question. Instead, you deal in the *frequency domain* and ask how much of each frequency component present in the input gets through. We will get to this important topic soon (Section 1.18). Before we do, though, there are a few other interesting circuits we can analyze simply with this time-domain approach.

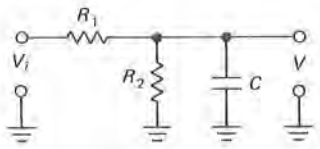


Figure 1.34

Simplification by Thévenin equivalents

We could go ahead and analyze more complicated circuits by similar methods, writing down the differential equations and trying to find solutions. For most purposes it simply isn't worth it. This is as complicated an RC circuit as we will need. Many other circuits can be reduced to it (e.g., Fig. 1.34). By just using the Thévenin equivalent of the voltage divider formed by R_1 and R_2, you can find the output

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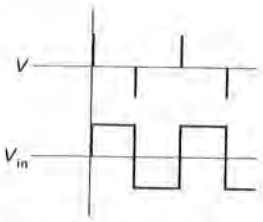


Figure 1.37. Output waveform (top) from differentiator driven by a square wave.

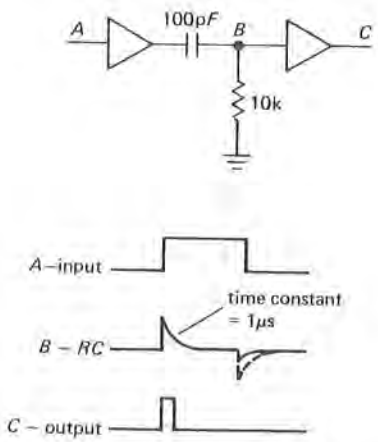


Figure 1.38. Leading-edge detector.

Differentiators are handy for detecting *leading edges* and *trailing edges* in pulse signals, and in digital circuitry you sometimes see things like those depicted in Figure 1.38. The *RC* differentiator generates spikes at the transitions of the input signal, and the output buffer converts the spikes to short square-topped pulses. In practice, the negative spike will be small because of a diode (a handy device discussed in Section 1.25) built into the buffer.

Unintentional capacitive coupling

Differentiators sometimes crop up unexpectedly, in situations where they're not welcome. You may see signals like those shown in Figure 1.39. The first case is caused by a square wave somewhere in the circuit coupling capacitively to the signal line you're looking at; that might indicate a missing resistor termination on your signal line. If not, you must either reduce the source resistance of the signal line or find a way to reduce capacitive coupling from the offending square wave. The second case is typical of what you might see when you look at a square wave, but have a broken connection somewhere, usually at the scope probe. The very small capacitance of the broken connection combines with the scope input resistance to form a differentiator. *Knowing that you've got a differentiated "something" can help you find the trouble and eliminate it.*

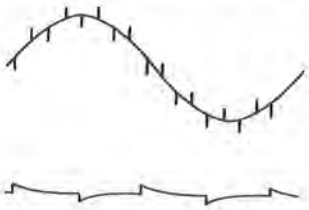


Figure 1.39

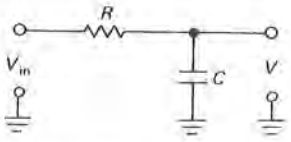


Figure 1.40

1.15 Integrators

Take a look at the circuit in Figure 1.40. The voltage across R is $V_{\text{in}} - V$, so

$$I = C\frac{dV}{dt} = \frac{V_{\text{in}} - V}{R}$$

If we manage to keep $V \ll V_{\text{in}}$, by keeping the product RC large, then

$$C\frac{dV}{dt} \approx \frac{V_{\text{in}}}{R}$$

or

$$V(t) = \frac{1}{RC}\int^{t} V_{\text{in}}(t)\,dt + \text{constant}$$

We have a circuit that performs the integral over time of an input signal! You can

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$V(t)$ produced by a step input for V_0.

EXERCISE 1.14

$R_1 = R_2 = 10\text{k}$, and $C = 0.1\mu\text{F}$ in the circuit shown in Figure 1.34. Find $V(t)$ and sketch it.

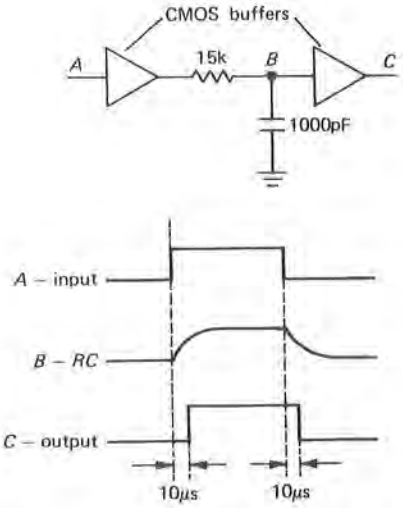


Figure 1.35. Producing a delayed digital waveform with the help of an RC.

Example: time-delay circuit

We have already mentioned logic levels, the voltages that digital circuits live on. Figure 1.35 shows an application of capacitors to produce a delayed pulse. The triangular symbols are "CMOS buffers." They give a HIGH output if the input is HIGH (more than one-half the dc power-supply voltage used to power them), and vice versa. The first buffer provides a replica of the input signal, but with low source resistance, and prevents input loading by the RC (recall our earlier discussion of circuit loading in Section 1.05). The RC output has the characteristic decays and causes the output buffer to switch 10μs after the input transitions (an RC reaches 50% output in $0.7RC$). In an actual application you would have to consider the effect of the buffer input threshold deviating from one-half the supply voltage, which would alter the delay and change the output pulse width. Such a circuit is sometimes used to delay a pulse so that something else can happen first. In designing circuits you try not to rely on tricks like this, but they're occasionally handy.

1.14 Differentiators

Look at the circuit in Figure 1.36. The voltage across C is $V_{\text{in}} - V$, so

$$I = C\frac{d}{dt}(V_{\text{in}} - V) = \frac{V}{R}$$

If we choose R and C small enough so that $dV/dt \ll dV_{\text{in}}/dt$, then

$$C\frac{dV_{\text{in}}}{dt} \approx \frac{V}{R}$$

or

$$V(t) = RC\frac{d}{dt}V_{\text{in}}(t)$$

That is, we get an output proportional to the rate of change of the input waveform.

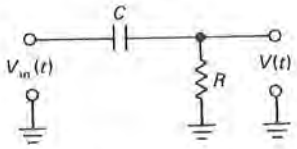


Figure 1.36

To keep $dV/dt \ll dV_{\text{in}}/dt$, we make the product RC small, taking care not to "load" the input by making R too small (at the transition the change in voltage across the capacitor is zero, so R is the load seen by the input). We will have a better criterion for this when we look at things in the frequency domain. If you drive this circuit with a square wave, the output will be as shown in Figure 1.37.

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see how the approximation works for a square-wave input: $V(t)$ is then the exponential charging curve we saw earlier (Fig. 1.41). The first part of the exponential is a ramp, the integral of a constant; as we increase the time constant RC, we pick off a smaller part of the exponential, i.e., a better approximation to a perfect ramp.

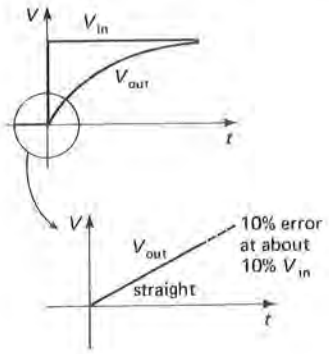


Figure 1.41

Note that the condition $V \ll V_{in}$ is just the same as saying that I is proportional to V_{in}. If we had as input a *current* $I(t)$, rather than a voltage, we would have an exact integrator. A large voltage across a large resistance approximates a current source and, in fact, is frequently used as one.

Later, when we get to operational amplifiers and feedback, we will be able to build integrators without the restriction $V_{out} \ll V_{in}$. They will work over large frequency and voltage ranges with negligible error.

The integrator is used extensively in analog computation. It is a useful subcircuit that finds application in control systems, feedback, analog/digital conversion, and waveform generation.

Ramp generators

At this point it is easy to understand how a ramp generator works. This nice circuit is extremely useful, for example in timing circuits, waveform and function generators, oscilloscope sweep circuits, and analog/digital conversion circuitry. The circuit uses a constant current to charge a capacitor (Fig. 1.42). From the capacitor equation $I = C(dV/dt)$, you get $V(t) = (I/C)t$. The output waveform is as shown in Figure 1.43. The ramp stops when the current source "runs out of voltage," i.e., reaches the limit of its compliance. The curve for a simple RC, with the resistor tied to a voltage source equal to the compliance of the current source, and with R chosen so that the current at zero output voltage is the same as that of the current source, is also drawn for comparison. (Real current sources generally have output compliances limited by the power-supply voltages used in making them, so the comparison is realistic.) In the next chapter, which deals with transistors, we will design some current sources, with some refinements to follow in the chapters on operational amplifiers (op-amps) and field-effect transistors (FETs). Exciting things to look forward to!

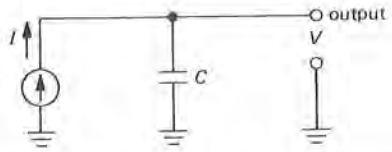


Figure 1.42. A constant current source charging a capacitor generates a ramp voltage waveform.

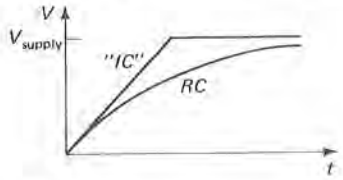


Figure 1.43

EXERCISE 1.15

A current of 1mA charges a 1μF capacitor. How long does it take the ramp to reach 10 volts?

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INDUCTORS AND TRANSFORMERS

1.16 Inductors

If you understand capacitors, you won't have any trouble with inductors (Fig. 1.44). They're closely related to capacitors; the rate of current change in an inductor depends on the voltage applied across it, whereas the rate of voltage change in a capacitor depends on the current through it. The defining equation for an inductor is

$$V = L\frac{dI}{dt}$$

where L is called the *inductance* and is measured in henrys (or mH, μH, etc.). Putting a voltage across an inductor causes the current to rise as a ramp (for a capacitor, supplying a constant current causes the voltage to rise as a ramp); 1 volt across 1 henry produces a current that increases at 1 amp per second.

Figure 1.44. Inductor.

As with capacitive current, inductive current is not simply proportional to voltage. Furthermore, unlike the situation in a resistor, the power associated with inductive current (V times I) is not turned into heat, but is stored as energy in the inductor's magnetic field. You get all that energy back when you interrupt the inductor's current.

The symbol for an inductor looks like a coil of wire; that's because, in its simplest form, that's all it is. Variations include coils wound on various core materials, the most popular being iron (or iron alloys, laminations, or powder) and ferrite, a black, nonconductive, brittle magnetic material. These are all ploys to multiply the inductance of a given coil by the "permeability" of the core material. The core may be in the shape of a rod, a toroid (doughnut), or even more bizarre shapes, such as a "pot core" (which has to be seen to be understood; the best description we can think of is a doughnut mold split horizontally in half, if doughnuts were made in molds).

Inductors find heavy use in radio-frequency (RF) circuits, serving as RF "chokes" and as parts of tuned circuits (see Chapter 13). A pair of closely coupled inductors forms the interesting object known as a transformer. We will talk briefly about them in the next section.

An inductor is, in a real sense, the opposite of a capacitor. You will see how that works out in the next few sections of this chapter, which deal with the important subject of *impedance*.

1.17 Transformers

A transformer is a device consisting of two closely coupled coils (called primary and secondary). An ac voltage applied to the primary appears across the secondary, with a voltage multiplication proportional to the turns ratio of the transformer and a current multiplication inversely proportional to the turns ratio. Power is conserved. Figure 1.45 shows the circuit symbol for a laminated-core transformer (the kind used for 60Hz ac power conversion).

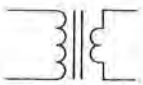


Figure 1.45. Transformer.

Transformers are quite efficient (output power is very nearly equal to input power); thus, a step-up transformer gives higher voltage at lower current. Jumping ahead for a moment, a transformer of turns ratio n increases the impedance by n^2. There is very little primary current if the secondary is unloaded.

Transformers serve two important functions in electronic instruments: They

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change the ac line voltage to a useful (usually lower) value that can be used by the circuit, and they "isolate" the electronic device from actual connection to the power line, because the windings of a transformer are electrically insulated from each other. *Power transformers* (meant for use from the 110V power line) come in an enormous variety of secondary voltages and currents: outputs as low as 1 volt or so up to several thousand volts, current ratings from a few milliamps to hundreds of amps. Typical transformers for use in electronic instruments might have secondary voltages from 10 to 50 volts, with current ratings of 0.1 to 5 amps or so.

Transformers for use at audiofrequencies and radiofrequencies are also available. At radiofrequencies you sometimes use tuned transformers, if only a narrow range of frequencies is present. There is also an interesting class of transmission-line transformer that we will discuss briefly in Section 13.10. In general, transformers for use at high frequencies must use special core materials or construction to minimize core losses, whereas low-frequency transformers (e.g., power transformers) are burdened instead by large and heavy cores. The two kinds of transformers are in general not interchangeable.

IMPEDANCE AND REACTANCE

Warning: This section is somewhat mathematical; you may wish to skip over the mathematics, but be sure to pay attention to the results and graphs.

Circuits with capacitors and inductors are more complicated than the resistive circuits we talked about earlier, in that their behavior depends on frequency: A "voltage divider" containing a capacitor or inductor will have a frequency-dependent division ratio. In addition, circuits containing these components (known collectively as *reactive* components) "corrupt" input waveforms such as square waves, as we just saw.

However, both capacitors and inductors are *linear* devices, meaning that the amplitude of the output waveform, whatever its shape, increases exactly in proportion to the input waveform's amplitude. This linearity has many consequences, the most important of which is probably the following: *The output of a linear circuit, driven with a sine wave at some frequency* f, *is itself a sine wave at the same frequency (with, at most, changed amplitude and phase).*

Because of this remarkable property of circuits containing resistors, capacitors, and inductors (and, later, linear amplifiers), it is particularly convenient to analyze any such circuit by asking how the output voltage (amplitude and phase) depends on the input voltage, *for sine-wave input at a single frequency*, even though this may not be the intended use. A graph of the resulting *frequency response*, in which the ratio of output to input is plotted for each sine-wave frequency, is useful for thinking about many kinds of waveforms. As an example, a certain "boom-box" loudspeaker might have the frequency response shown in Figure 1.46, where the "output" in this case is of course sound pressure, not voltage. It is desirable for a speaker to have a "flat" response, meaning that the graph of sound pressure versus frequency is constant over the band of audible frequencies. In this case the speaker's deficiencies can be corrected by introducing a passive filter with the inverse response (as shown) into the amplifiers of the radio.

As we will see, it is possible to generalize Ohm's law, replacing the word "resistance" with "impedance," in order to describe any circuit containing these linear passive devices (resistors, capacitors, and inductors). You could think of the subject of impedance and reactance as Ohm's law for circuits that include capacitors and inductors. Some important terminology: Impedance is the "generalized resistance"; inductors

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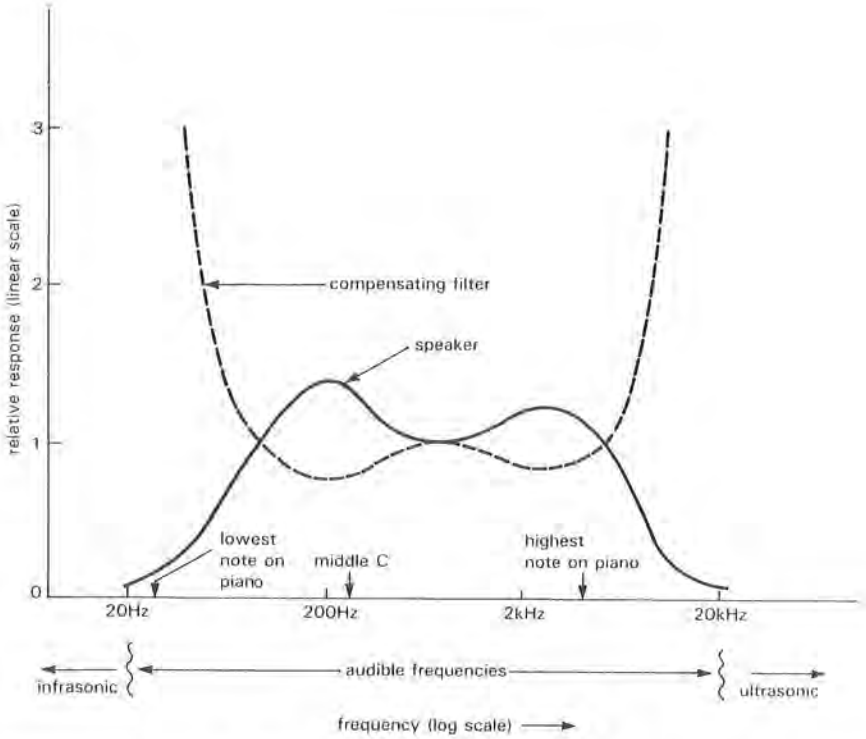


Figure 1.46. Example of frequency analysis: "boom box" loudspeaker equalization.

and capacitors have *reactance* (they are "reactive"); resistors have *resistance* (they are "resistive"). In other words, impedance = resistance + reactance (more about this later). However, you'll see statements like "the impedance of the capacitor at this frequency is ... " The reason you don't have to use the word "reactance" in such a case is that impedance covers everything. In fact, you frequently use the word "impedance" even when you know it's a resistance you're talking about; you say "the source impedance" or "the output impedance" when you mean the Thévenin equivalent resistance of some source. The same holds for "input impedance."

In all that follows, we will be talking about circuits driven by sine waves at a single frequency. Analysis of circuits driven by complicated waveforms is more elaborate, involving the methods we used earlier (differential equations) or decomposition of the waveform into sine waves (Fourier analysis). Fortunately, these methods are seldom necessary.

1.18 Frequency analysis of reactive circuits

Let's start by looking at a capacitor driven by a sine-wave voltage source (Fig. 1.47). The current is

$$I(t) = C\frac{dV}{dt} = C\omega V_0 \cos \omega t$$

i.e., a current of amplitude I, with the phase leading the input voltage by 90°. If we consider amplitudes only, and disregard phases, the current is

$$I = \frac{V}{1/\omega C}$$

(Recall that $\omega = 2\pi f$.) It behaves like a frequency-dependent resistance $R = 1/\omega C$, but in addition the current is 90° out of phase with the voltage (Fig. 1.48).

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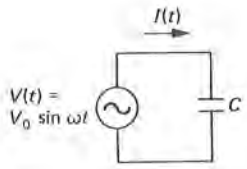


Figure 1.47

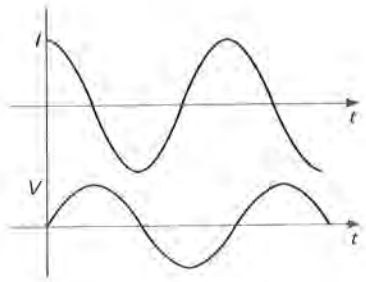


Figure 1.48

For example, a 1μF capacitor put across the 110 volt (rms) 60Hz power line draws a current of rms amplitude

$$I = \frac{110}{1/(2\pi \times 60 \times 10^{-6})} = 41.5\text{mA (rms)}$$

Note: At this point it is necessary to get into some complex algebra; you may wish to skip over the math in some of the following sections, taking note of the results as we derive them. A knowledge of the detailed mathematics is not necessary in order to understand the remainder of the book. Very little mathematics will be used in later chapters. The section ahead is easily the most difficult for the reader with little mathematical preparation. Don't be discouraged!

Voltages and currents as complex numbers

As you have just seen, there can be phase shifts between the voltage and current in an ac circuit being driven by a sine wave at some frequency. Nevertheless, as long as the circuit contains only *linear* elements (resistors, capacitors, inductors), the magnitudes of the currents everywhere in the circuit are still proportional to the magnitude of the driving voltage, so we might hope to find some generalization of voltage, current, and resistance in order to rescue Ohm's law. Obviously a single number won't suffice to specify the current, say, at some point in the circuit, because we must somehow have information about both the magnitude and phase shift.

Although we can imagine specifying the magnitudes and phase shifts of voltages and currents at any point in the circuit by writing them out explicitly, e.g., $V(t) = 23.7\sin(377t + 0.38)$, it turns out that our requirements can be met more simply by using the algebra of complex numbers to *represent* voltages and currents. Then we can simply add or subtract the complex number representations, rather than laboriously having to add or subtract the actual sinusoidal functions of time themselves. Because the actual voltages and currents are real quantities that vary with time, we must develop a rule for converting from actual quantities to their representations, and vice versa. Recalling once again that we are talking about a single sine-wave frequency, ω, we agree to use the following rules:

1. Voltages and currents are *represented* by the complex quantities $\mathbf{V}$ and $\mathbf{I}$. The voltage $V_0\cos(\omega t+\phi)$ is to be represented by the complex number $V_0e^{j\phi}$. Recall that $e^{j\theta} = \cos\theta + j\sin\theta$, where $j = \sqrt{-1}$.

2. *Actual* voltages and currents are obtained by multiplying their complex number representations by $e^{j\omega t}$ and then taking the real part: $V(t) = \mathcal{R}e(\mathbf{V}e^{j\omega t})$, $I(t) = \mathcal{R}e(\mathbf{I}e^{j\omega t})$

In other words,

circuit voltage versus time		complex number representation
$V_0\cos(\omega t + \phi)$	multiply by $e^{j\omega t}$ and take real part	$V_0e^{j\phi} = a + jb$

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(In electronics, the symbol j is used instead of i in the exponential in order to avoid confusion with the symboi i meaning current.) Thus, in the general case the actual voltages and currents are given by

$$\begin{aligned} V(t) &= \mathcal{R}e(\mathbf{V}e^{j\omega t}) \\ &= \mathcal{R}e(\mathbf{V})\cos\omega t - \mathcal{I}m(\mathbf{V})\sin\omega t \\ I(t) &= \mathcal{R}e(\mathbf{I}e^{j\omega t}) \\ &= \mathcal{R}e(\mathbf{I})\cos\omega t - \mathcal{I}m(\mathbf{I})\sin\omega t \end{aligned}$$

For example, a voltage whose complex representation is

$$\mathbf{V} = 5j$$

corresponds to a (real) voltage versus time of

$$\begin{aligned} V(t) &= \mathcal{R}e[5j\cos\omega t + 5j(j)\sin\omega t] \\ &= -5\sin\omega t \text{ volts} \end{aligned}$$

Reactance of capacitors and inductors

With this convention we can apply complex Ohm's law to circuits containing capacitors and inductors, just as for resistors, once we know the reactance of a capacitor or inductor. Let's find out what these are. We have

$$V(t) = \mathcal{R}e(V_0e^{j\omega t})$$

For a capacitor, using $I = C(dV/dt)$, we obtain

$$\begin{aligned} I(t) = -V_0C\omega\sin\omega t &= \mathcal{R}e\left(\frac{V_0e^{j\omega t}}{-j/\omega C}\right) \\ &= \mathcal{R}e\left(\frac{V_0e^{j\omega t}}{X_C}\right) \end{aligned}$$

i.e., for a capacitor

$$X_C = -j/\omega C$$

X_C is the reactance of a capacitor at frequency ω. As an example a 1μF capacitor has a reactance of $-2653j$ ohms at 60Hz and a reactance of $-0.16j$ ohms at 1MHz. Its reactance at dc is infinite.

If we did a similar analysis for an inductor, we would find

$$X_L = j\omega L$$

A circuit containing only capacitors and inductors always has a purely imaginary impedance, meaning that the voltage and current are always 90° out of phase – it is purely reactive. When the circuit contains resistors, there is also a real part to the impedance. The term "reactance" in that case means the imaginary part only.

Ohm's law generalized

With these conventions for representing voltages and currents, Ohm's law takes a simple form. It reads simply

$$\mathbf{I} = \mathbf{V}/\mathbf{Z}$$
$$\mathbf{V} = \mathbf{IZ}$$

where the voltage represented by $\mathbf{V}$ is applied across a circuit of impedance $\mathbf{Z}$, giving a current represented by $\mathbf{I}$. The complex impedance of devices in series or parallel obeys the same rules as resistance:

$$\mathbf{Z} = \mathbf{Z}_1 + \mathbf{Z}_2 + \mathbf{Z}_3 + \cdots \quad \text{(series)}$$
$$\mathbf{Z} = \frac{1}{\frac{1}{\mathbf{Z}_1} + \frac{1}{\mathbf{Z}_2} + \frac{1}{\mathbf{Z}_3} + \cdots} \quad \text{(parallel)}$$

Finally, for completeness we summarize here the formulas for the impedance of resistors, capacitors, and inductors:

$$\mathbf{Z}_R = R \quad \text{(resistor)}$$
$$\mathbf{Z}_C = -j/\omega C = 1/j\omega C \quad \text{(capacitor)}$$
$$\mathbf{Z}_L = j\omega L \quad \text{(inductor)}$$

With these rules we can analyze many ac circuits by the same general methods we used in handling dc circuits, i.e., application of the series and parallel formulas and Ohm's law. Our results for circuits such as voltage dividers will look nearly the same as before. For multiply connected

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networks we may have to use Kirchhoff's laws, just as with dc circuits, in this case using the complex representations for V and I: The sum of the (complex) voltage drops around a closed loop is zero, and the sum of the (complex) currents into a point is zero. The latter rule implies, as with dc circuits, that the (complex) current in a series circuit is the same everywhere.

EXERCISE 1.16

Use the preceding rules for the impedance of devices in parallel and in series to derive the formulas (Section 1.12) for the capacitance of two capacitors (a) in parallel and (b) in series. Hint: In each case, let the individual capacitors have capacitances C_1 and C_2. Write down the impedance of the parallel or series combination; then equate it to the impedance of a capacitor with capacitance C. Find C.

Let's try out these techniques on the simplest circuit imaginable, an ac voltage applied across a capacitor, which we considered just previously. Then, after a brief look at power in reactive circuits (to finish laying the groundwork), we'll analyze some simple but extremely important and useful RC filter circuits.

Imagine putting a 1μF capacitor across a 110 volt (rms) 60Hz power line. What current flows? Using complex Ohm's law, we have

$$\mathbf{Z} = -j/\omega C$$

Therefore, the current is given by

$$\mathbf{I} = \mathbf{V}/\mathbf{Z}$$

The phase of the voltage is arbitrary, so let us choose $\mathbf{V} = A$, i.e. $V(t) = A\cos\omega t$, where the amplitude $A = 110\sqrt{2} \approx 156$ volts. Then

$$\mathbf{I} = j\omega CA \approx 0.059\sin\omega t$$

The resulting current has an amplitude of 59mA (41.5mA rms) and leads the voltage by 90°. This agrees with our previous calculation. Note that if we just wanted to know the magnitude of the current, and didn't care what the relative phase was, we could have avoided doing any complex algebra: If

$$\mathbf{A} = \mathbf{B}/\mathbf{C}$$

then

$$A = B/C$$

where A, B, and C are the magnitudes of the respective complex numbers; this holds for multiplication, also (see Exercise 1.17). Thus, in this case,

$$I = V/Z = \omega CV$$

This trick is often useful.

Surprisingly, there is no power dissipated by the capacitor in this example. Such activity won't increase your electric bill; you'll see why in the next section. Then we will go on to look at circuits containing resistors and capacitors with our complex Ohm's law.

EXERCISE 1.17

Show that if $\mathbf{A}=\mathbf{BC}$, then $A=BC$, where A, B, and C are magnitudes. Hint: Represent each complex number in polar form, i.e., $\mathbf{A}=Ae^{i\theta}$.

Power in reactive circuits

The instantaneous power delivered to any circuit element is always given by the product $P = VI$. However, in reactive circuits where V and I are not simply proportional, you can't just multiply them together. Funny things can happen; for instance, the sign of the product can reverse over one cycle of the ac signal. Figure 1.49 shows an example. During time intervals A and C, power is being delivered to the capacitor (albeit at a variable rate), causing it to charge up; its stored energy is increasing (power is the rate of change of energy). During intervals B and D, the power delivered to the capacitor is negative; it is discharging. The average power over a whole cycle for this example is in fact exactly zero, a statement that is always true for any purely reactive circuit element (inductors, capacitors, or any combination

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thereof). If you know your trigonometric integrals, the next exercise will show you how to prove this.

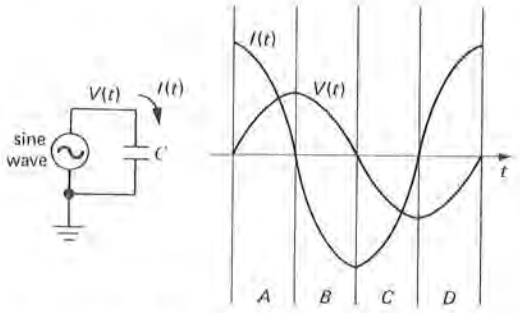


Figure 1.49. When driven by a sine wave, the current through a capacitor leads the voltage by 90°.

EXERCISE 1.18

Optional exercise: Prove that a circuit whose current is 90° out of phase with the driving voltage consumes no power, averaged over an entire cycle.

How do we find the average power consumed by an arbitrary circuit? In general, we can imagine adding up little pieces of VI product, then dividing by the elapsed time. In other words,

$$P = \frac{1}{T}\int_0^T V(t)I(t)\,dt$$

where T is the time for one complete cycle. Luckily, that's almost never necessary. Instead, it is easy to show that the average power is given by

$$P = \mathcal{R}e(\mathbf{V}\mathbf{I}^*) = \mathcal{R}e(\mathbf{V}^*\mathbf{I})$$

where $\mathbf{V}$ and $\mathbf{I}$ are complex rms amplitudes.

Let's take an example. Consider the preceding circuit, with a 1 volt (rms) sine wave driving a capacitor. We'll do everything with rms amplitudes, for simplicity. We have

$$\mathbf{V} = 1$$

$$\mathbf{I} = \frac{\mathbf{V}}{-j/\omega C} = j\omega C$$

$$P = \mathcal{R}e(\mathbf{V}\mathbf{I}^*) = \mathcal{R}e(-j\omega C) = 0$$

That is, the average power is zero, as stated earlier.

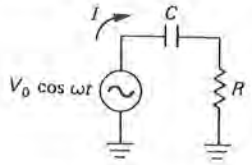


Figure 1.50

As another example, consider the circuit shown in Figure 1.50. Our calculations go like this:

$$\mathbf{Z} = R - \frac{j}{\omega C}$$

$$\mathbf{V} = V_0$$

$$\mathbf{I} = \frac{\mathbf{V}}{\mathbf{Z}} = \frac{V_0}{R - (j/\omega C)} = \frac{V_0[R + (j/\omega C)]}{R^2 + (1/\omega^2 C^2)}$$

$$P = \mathcal{R}e(\mathbf{V}\mathbf{I}^*) = \frac{V_0^2 R}{R^2 + (1/\omega^2 C^2)}$$

(In the third line we multiplied numerator and denominator by the complex conjugate of the denominator, in order to make the denominator real.) This is less than the product of the magnitudes of $\mathbf{V}$ and $\mathbf{I}$. In fact, the ratio is called the *power factor*:

$$|\mathbf{V}|\,|\mathbf{I}| = \frac{V_0^2}{[R^2 + (1/\omega^2 C^2)]^{1/2}}$$

$$\text{power factor} = \frac{\text{power}}{|\mathbf{V}|\,|\mathbf{I}|} = \frac{R}{[R^2 + (1/\omega^2 C^2)]^{1/2}}$$

in this case. The power factor is the cosine of the phase angle between the voltage and the current, and it ranges from 0 (purely reactive circuit) to 1 (purely resistive). A power factor less than 1 indicates some component of reactive current.

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EXERCISE 1.19

Show that all the average power delivered to the preceding circuit winds up in the resistor. Do this by computing the value of V_R^2/R. What is that power, in watts, for a series circuit of a 1μF capacitor and a 1.0k resistor placed across the 110 volt (rms), 60Hz power line?

Power factor is a serious matter in large-scale electrical power distribution, because reactive currents don't result in useful power being delivered to the load, but cost the power company plenty in terms of I^2R heating in the resistance of generators, transformers, and wiring. Although residential users are only billed for "real" power $[\mathcal{R}e(\mathbf{VI}^*)]$, the power company charges industrial users according to the power factor. This explains the capacitor yards that you see behind large factories, built to cancel the inductive reactance of industrial machinery (i.e., motors).

EXERCISE 1.20

Show that adding a series capacitor of value $C = 1/\omega^2 L$ makes the power factor equal 1.0 in a series RL circuit. Now do the same thing, but with the word "series" changed to "parallel."

Voltage dividers generalized

Our original voltage divider (Fig. 1.5) consisted of a pair of resistors in series to ground, input at the top and output at the junction. The generalization of that simple resistive divider is a similar circuit in which either or both resistors are replaced by a capacitor or inductor (or a more complicated network made from R, L, and C), as in Figure 1.51. In general, the division ratio $V_{\text{out}}/V_{\text{in}}$ of such a divider is not constant, but depends on frequency. The analysis is straightforward:

$$\mathbf{I} = \frac{\mathbf{V}_{\text{in}}}{\mathbf{Z}_{\text{total}}}$$

$$\mathbf{Z}_{\text{total}} = \mathbf{Z}_1 + \mathbf{Z}_2$$

$$\mathbf{V}_{\text{out}} = \mathbf{I}\,\mathbf{Z}_2 = \mathbf{V}_{\text{in}}\frac{\mathbf{Z}_2}{\mathbf{Z}_1 + \mathbf{Z}_2}$$

Rather than worrying about this result in general, let's look at some simple, but very important, examples.

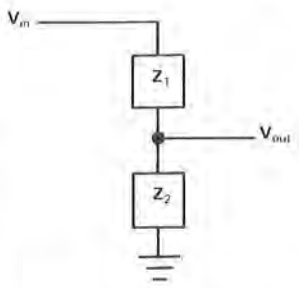


Figure 1.51. Generalized voltage divider: a pair of arbitrary impedances.

1.19 *RC* filters

By combining resistors with capacitors it is possible to make frequency-dependent voltage dividers, owing to the frequency dependence of a capacitor's impedance $\mathbf{Z}_C = -j/\omega C$. Such circuits can have the desirable property of passing signal frequencies of interest while rejecting undesired signal frequencies. In this section you will see examples of the simplest such RC filters, which we will be using frequently throughout the book. Chapter 5 and Appendix H describe filters of greater sophistication.

High-pass filters

Figure 1.52 shows a voltage divider made from a capacitor and a resistor. Complex Ohm's law gives

$$\mathbf{I} = \frac{\mathbf{V}_{\text{in}}}{\mathbf{Z}_{\text{total}}} = \frac{\mathbf{V}_{\text{in}}}{R - (j/\omega C)}$$
$$= \frac{\mathbf{V}_{\text{in}}[R + (j/\omega C)]}{R^2 + 1/\omega^2 C^2}$$

(For the last step, multiply top and bottom by the complex conjugate of the denominator.) So the voltage across R is just

$$\mathbf{V}_{\text{out}} = \mathbf{I}\,\mathbf{Z}_R = \mathbf{I}\,R = \frac{\mathbf{V}_{\text{in}}[R + (j/\omega C)]R}{R^2 + (1/\omega^2 C^2)}$$

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Most often we don't care about the phase of V_{out}, just its amplitude:

$$\mathbf{V}_{out} = (\mathbf{V}_{out}\mathbf{V}^*_{out})^{1/2}$$
$$= \frac{R}{[R^2 + (1/\omega^2C^2)]^{1/2}}V_{in}$$

Note the analogy to a resistive divider, where

$$V_{out} = \frac{R_1}{R_1 + R_2}V_{in}$$

Here the impedance of the series RC combination (Fig. 1.53) is as shown in Figure 1.54. So the "response" of this circuit, ignoring phase shifts by taking magnitudes of the complex amplitudes, is given by

$$V_{out} = \frac{R}{[R^2 + (1/\omega^2C^2)]^{1/2}}V_{in}$$
$$= \frac{2\pi fRC}{[1 + (2\pi fRC)^2]^{1/2}}V_{in}$$

and looks as shown in Figure 1.55. We could have gotten this result immediately by taking the ratio of the *magnitudes* of impedances, as in Exercise 1.17 and the example immediately preceding it; the numerator is the magnitude of the impedance of the lower leg of the divider (R), and the denominator is the magnitude of the impedance of the series combination of R and C.

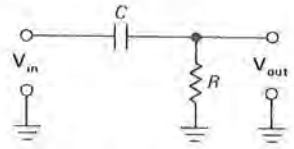


Figure 1.52. High-pass filter.

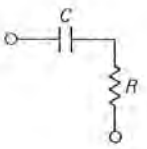


Figure 1.53

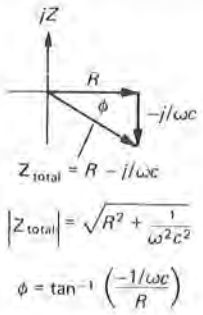


Figure 1.54

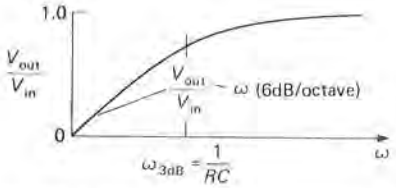


Figure 1.55. Frequency response of high-pass filter.

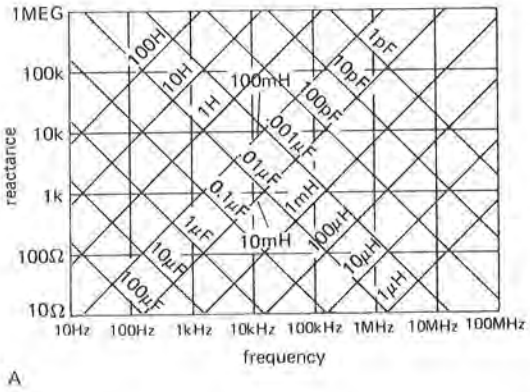
You can see that the output is approximately equal to the input at high frequencies (how high? $\gtrsim 1/RC$) and goes to zero at low frequencies. This is a very important result. Such a circuit is called a high-pass filter, for obvious reasons. It is very common. For instance, the input to the oscilloscope (Appendix A) can be switched to ac coupling. That's just an RC high-pass filter with the bend at about 10Hz (you would use ac coupling if you wanted to look at a small signal riding on a large dc voltage). Engineers like to refer to the −3dB "breakpoint" of a filter (or of any circuit that behaves like a filter). In the case of the simple RC high-pass filter, the −3dB breakpoint is given by

$$f_{3dB} = 1/2\pi RC$$

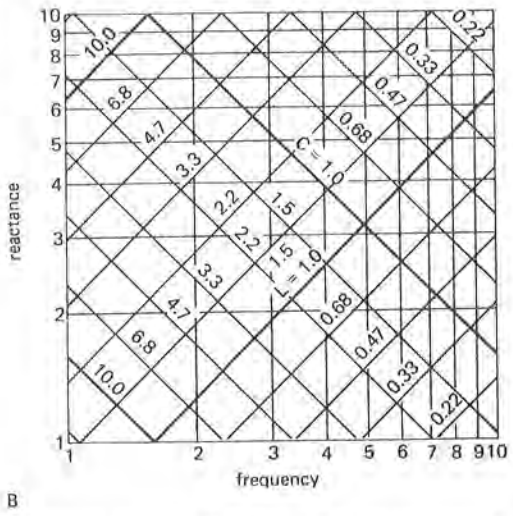
Note that the capacitor lets no steady current through ($f = 0$). This use as a dc *blocking capacitor* is one of its most frequent applications. Whenever you need to couple a signal from one amplifier to another, you almost invariably use a capacitor. For instance, every hi-fi audio

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amplifier has all its inputs capacitively coupled, because it doesn't know what dc level its input signals might be riding on. In such a coupling application you always pick R and C so that all frequencies of interest (in this case, 20Hz–20kHz) are passed without loss (attenuation).



A



B

Figure 1.56. A. Reactance of inductors and capacitors versus frequency; all decades are identical, except for scale.
B. A single decade from part A expanded, with standard 20% component values shown.

You often need to know the impedance of a capacitor at a given frequency (e.g., for design of filters). Figure 1.56 provides a very useful graph covering large ranges of capacitance and frequency, giving the value of $|Z| = 1/2\pi fC$.

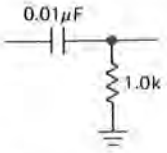


Figure 1.57

As an example, consider the filter shown in Figure 1.57. It is a high-pass filter with the 3dB point at 15.9kHz. The impedance of a load driven by it should be much larger than 1.0k in order to prevent circuit loading effects on the filter's output, and the driving source should be able to drive a 1.0k load without significant attenuation (loss of signal amplitude) in order to prevent circuit loading effects by the filter on the signal source.

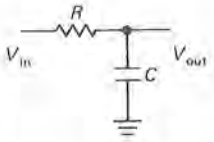


Figure 1.58. Low-pass filter.

Low-pass filters

You can get the opposite frequency behavior in a filter by interchanging R and C (Fig. 1.58). You will find

$$V_{\text{out}} = \frac{1}{(1+\omega^2R^2C^2)^{1/2}}V_{\text{in}}$$

as seen in Figure 1.59. This is called a low-pass filter. The 3dB point is again at a frequency

$$f = 1/2\pi RC$$

Low-pass filters are quite handy in real life. For instance, a low-pass filter can be used to eliminate interference from nearby radio and television stations (550kHz–800MHz), a problem that plagues audio

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amplifiers and other sensitive electronic equipment.

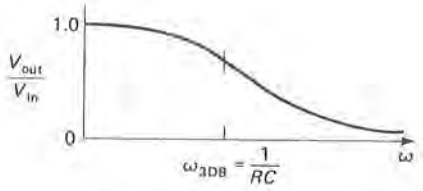


Figure 1.59. Frequency response of low-pass filter.

EXERCISE 1.21

Show that the preceding expression for the response of an RC low-pass filter is correct.

The low-pass filter's output can be viewed as a signal source in its own right. When driven by a perfect ac voltage (zero source impedance), the filter's output looks like R at low frequencies (the perfect signal source can be replaced by a short, i.e., by its small-signal source impedance, for the purpose of impedance calculations). It drops to zero impedance at high frequencies, where the capacitor dominates the output impedance. The signal driving the filter sees a load of R plus the load resistance at low frequencies, dropping to R at high frequencies.

In Figure 1.60, we've plotted the same low-pass filter response with *logarithmic* axes, which is a more usual way of doing it. You can think of the vertical axis as decibels, and the horizontal axis as octaves (or decades). On such a plot, equal distances correspond to equal ratios. We've also plotted the phase shift, using a linear

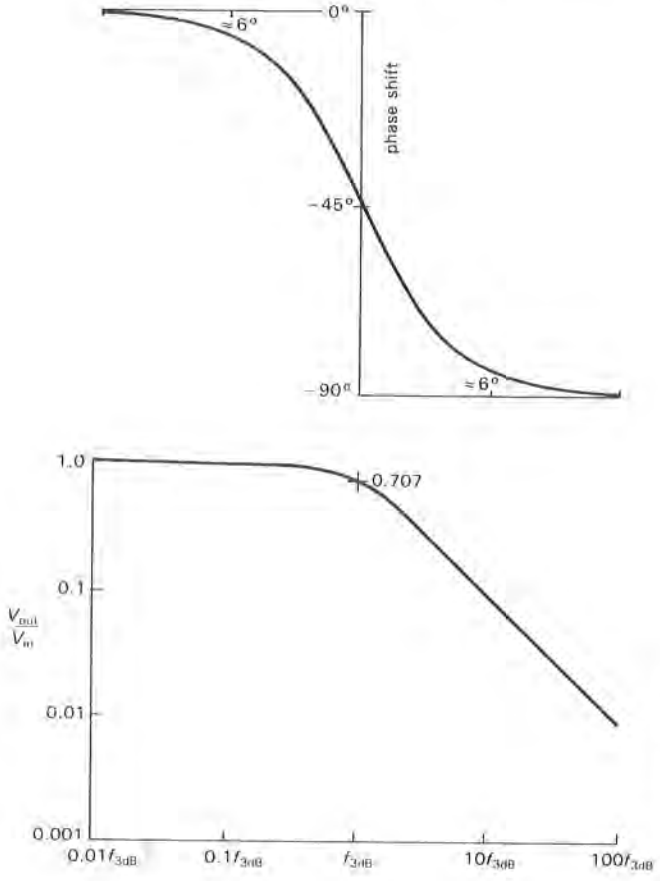


Figure 1.60. Frequency response (phase and amplitude) of low-pass filter, plotted on logarithmic axes. Note that the phase shift is 45°at the 3dB point and is within 6° of its asymptotic value for a decade of frequency change.

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vertical axis (degrees) and the same logarithmic frequency axis. This sort of plot is good for seeing the detailed response even when it is greatly attenuated (as at right); we'll see a number of such plots in Chapter 5, when we treat active filters. Note that the filter curve plotted here becomes a straight line at large attenuations, with a slope of −20dB/decade (engineers prefer to say "−6dB/octave"). Note also that the phase shift goes smoothly from 0° (at frequencies well below the breakpoint) to 90° (well above it), with a value of 45° at the −3dB point. A rule of thumb for single-section RC filters is that the phase shift is $\approx 6°$ from its asymptotic value at $0.1f_{3dB}$ and $10f_{3dB}$.

EXERCISE 1.22
Prove the last assertion.

An interesting question is the following: Is it possible to make a filter with some arbitrary specified amplitude response and some other specified phase response? Surprisingly, the answer is no: The demands of causality (i.e., that response must follow cause, not precede it) force a relationship between phase and amplitude response of realizable analog filters (known officially as the Kramers-Kronig relation).

RC differentiators and integrators in the frequency domain

The RC differentiator that we saw in Section 1.14 is exactly the same circuit as the high-pass filter in this section. In fact, it can be considered as either, depending on whether you're thinking of waveforms in the time domain or response in the frequency domain. We can restate the earlier time-domain condition for its proper operation ($V_{out} \ll V_{in}$) in terms of the frequency response: For the output to be small compared with the input, the signal frequency (or frequencies) must be well below the 3dB point. This is easy to check. Suppose we have the input signal

$$V_{in} = \sin \omega t$$

Then, using the equation we obtained earlier for the differentiator output,

$$V_{out} = RC\frac{d}{dt}\sin \omega t = \omega RC \cos \omega t$$

and so $V_{out} \ll V_{in}$ if $\omega RC \ll 1$, i.e., $RC \ll 1/\omega$. If the input signal contains a range of frequencies, this must hold for the highest frequencies present in the input.

The RC integrator (Section 1.15) is the same circuit as the low-pass filter; by similar reasoning, the criterion for a good integrator is that the lowest signal frequencies must be well above the 3dB point.

Inductors versus capacitors

Inductors could be used, instead of capacitors, in combination with resistors to make low-pass (or high-pass) filters. In practice, however, you rarely see RL low- or high-pass filters. The reason is that inductors tend to be more bulky and expensive and perform less well (i.e., they depart further from the ideal) than capacitors. If you have a choice, use a capacitor. One exception to this general statement is the use of ferrite beads and chokes in high-frequency circuits. You just string a few beads here and there in the circuit; they make the wire interconnections slightly inductive, raising the impedance at very high frequencies and preventing "oscillations," without the added resistance you would get with an RC filter. An RF "choke" is an inductor, usually a few turns of wire wound on a ferrite core, used for the same purpose in RF circuits.

□ 1.20 Phasor diagrams

There's a nice graphic method that can be very helpful when trying to understand reactive circuits. Let's take an example, namely the fact that an RC filter attenuates 3dB at a frequency $f = 1/2\pi RC$,

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which we derived in Section 1.19. This is true for both high-pass and low-pass filters. It is easy to get a bit confused here, because at that frequency the reactance of the capacitor equals the resistance of the resistor; so you might at first expect 6dB attenuation. That is what you would get, for example, if you were to replace the capacitor by a resistor of the same impedance (recall that 6dB means half voltage). The confusion arises because the capacitor is reactive, but the matter is clarified by a phasor diagram (Fig. 1.61). The axes are the real (resistive) and imaginary (reactive) components of the impedance. In a series circuit like this, the axes also represent the (complex) voltage, because the current is the same everywhere. So for this circuit (think of it as an R–C voltage divider) the input voltage (applied across the series R–C pair) is proportional to the length of the hypotenuse, and the output voltage (across R only) is proportional to the length of the R leg of the triangle. The diagram represents the situation at the frequency where the magnitude of the capacitor's reactance equals R, i.e., $f = 1/2\pi RC$, and shows that the ratio of output voltage to input voltage is $1/\sqrt{2}$, i.e., -3dB.

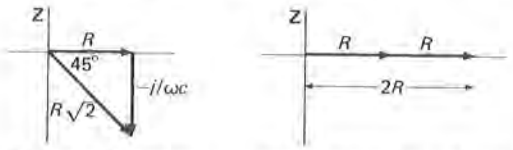


Figure 1.61

The angle between the vectors gives the phase shift from input to output. At the 3dB point, for instance, the output amplitude equals the input amplitude divided by the square root of 2, and it leads by 45° in phase. This graphic method makes it easy to read off amplitude and phase relationships in RLC circuits. For example, you can use it to get the response of the high-pass filter that we previously derived algebraically.

EXERCISE 1.23

Use a phasor diagram to derive the response of an RC high-pass filter:

$$V_{\text{out}} = \frac{R}{[R^2 + (1/\omega^2 C^2)]^{1/2}} V_{\text{in}}$$

EXERCISE 1.24

At what frequency does an RC low-pass filter attenuate by 6dB (output voltage equal to half the input voltage)? What is the phase shift at that frequency?

EXERCISE 1.25

Use a phasor diagram to obtain the low-pass filter response previously derived algebraically.

In the next chapter (Section 2.08) you will see a nice example of phasor diagrams in connection with a constant-amplitude phase-shifting circuit.

1.21 "Poles" and decibels per octave

Look again at the response of the RC low-pass filter (Fig. 1.59). Far to the right of the "knee" the output amplitude is dropping proportional to $1/f$. In one octave (as in music, one octave is twice the frequency) the output amplitude will drop to half, or -6dB; so a simple RC filter has a 6dB/octave falloff. You can make filters with several RC sections; then you get 12dB/octave (two RC sections), 18dB/octave (three sections), etc. This is the usual way of describing how a filter behaves beyond the cutoff. Another popular way is to say a "3-pole filter," for instance, meaning a filter with three RC sections (or one that behaves like one). (The word "pole" derives from a method of analysis that is beyond the scope of this book and that involves complex transfer functions in the complex frequency plane, known by engineers as the "s-plane.")

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A caution on multistage filters: You can't simply cascade several identical filter sections in order to get a frequency response that is the concatenation of the individual responses. The reason is that each stage will load the previous one significantly (since they're identical), changing the overall response. Remember that the response function we derived for the simple RC filters was based on a zero-impedance driving source and an infinite-impedance load. One solution is to make each successive filter section have much higher impedance than the preceding one. A better solution involves active circuits like transistor or operational amplifier (op-amp) interstage "buffers," or active filters. These subjects will be treated in Chapters 2 through 5.

1.22 Resonant circuits and active filters

When capacitors are combined with inductors or are used in special circuits called active filters, it is possible to make circuits that have very sharp frequency characteristics (e.g., a large peak in the response at a particular frequency), as compared with the gradual characteristics of the RC filters we've seen so far. These circuits find applications in various audiofrequency and radiofrequency devices. Let's now take a quick look at LC circuits (there will be more on them, and active filters, in Chapter 5 and Appendix H).

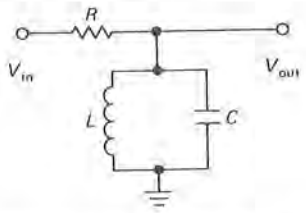


Figure 1.62. LC resonant circuit: bandpass filter.

First, consider the circuit shown in Figure 1.62. The reactance of the LC combination at frequency f is just

$$\frac{1}{\mathbf{Z}_{LC}} = \frac{1}{\mathbf{Z}_L} + \frac{1}{\mathbf{Z}_C} = \frac{1}{j\omega L} - \frac{\omega C}{j}$$
$$= j\left(\omega C - \frac{1}{\omega L}\right)$$

i.e.,

$$\mathbf{Z}_{LC} = \frac{j}{(1/\omega L) - \omega C}$$

In combination with R it forms a voltage divider; because of the opposite behaviors of inductors and capacitors, the impedance of the parallel LC goes to infinity at the *resonant frequency* $f_0 = 1/2\pi\sqrt{LC}$ (i.e., $\omega_0 = 1/\sqrt{LC}$), giving a peak in the response there. The overall response is as shown in Figure 1.63.

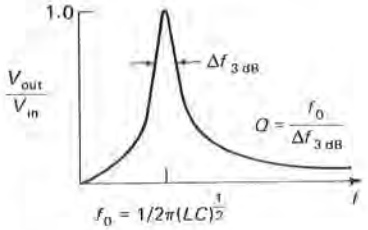


Figure 1.63

In practice, losses in the inductor and capacitor limit the sharpness of the peak, but with good design these losses can be made very small. Conversely, a Q-spoiling resistor is sometimes added intentionally to reduce the sharpness of the resonant peak. This circuit is known simply as a parallel LC resonant circuit or a tuned circuit and is used extensively in radiofrequency circuits to select a particular frequency for amplification (the L or C can be variable, so you can tune the resonant frequency). The higher the driving impedance, the sharper the peak; it is not uncommon to drive them with something approaching a current source, as you will see later. The *quality factor* Q is a measure of the sharpness of the peak. It equals the resonant frequency divided by the width

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at the −3dB points. For a parallel RLC circuit, $Q = \omega_0 RC$.

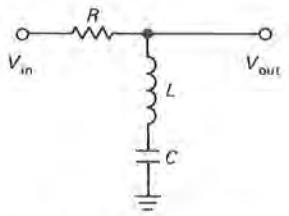


Figure 1.64. LC notch filter ("trap").

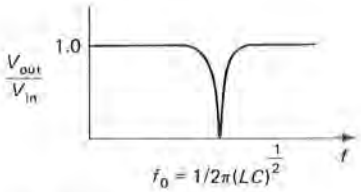


Figure 1.65

Another variety of LC circuit is the series LC (Fig. 1.64). By writing down the impedance formulas involved, you can convince yourself that the impedance of the LC goes to zero at resonance $[f_0 = 1/2\pi(LC)^{1/2}]$; such a circuit is a "trap" for signals at or near the resonant frequency, shorting them to ground. Again, this circuit finds application mainly in radiofrequency circuits. Figure 1.65 shows what the response looks like. The Q of a series RLC circuit is $Q = \omega_0 L/R$.

EXERCISE 1.26
Find the response (V_{out}/V_{in} versus frequency) for the series LC trap circuit in Figure 1.64.

1.23 Other capacitor applications

In addition to their uses in filters, resonant circuits, differentiators, and integrators, capacitors are needed for several other important applications. We will treat these in detail later in the book, mentioning them here only as a preview.

Bypassing

The impedance of a capacitor goes down with increasing frequency. This is the basis of another important application: bypassing. There are places in circuits where you want to allow a dc (or slowly varying) voltage, but don't want signals present. Placing a capacitor across that circuit element (usually a resistor) will help to kill any signals there. You choose the capacitor value so that its impedance at signal frequencies is small compared with what it is bypassing. You will see much more of this in later chapters.

Power-supply filtering

Power-supply filtering is really a form of bypassing, although we usually think of it as energy storage. The dc voltages used in electronics are usually generated from the ac line voltage by a process called *rectification* (which will be treated later in this chapter); some residue of the 60Hz input remains, and this can be reduced as much as desired by means of bypassing with suitably large capacitors. These capacitors really are large – they're the big shiny round things you see inside most electronic instruments. You will see how to design power supplies and filters later in this chapter and again in Chapter 6.

Timing and waveform generation

A capacitor supplied with a constant current charges up with a ramp waveform. This is the basis of ramp and sawtooth generators, used in function generators, oscilloscope sweep circuits, analog/digital converters, and timing circuits. RC circuits are also used for timing, and they form the basis of digital delay circuits (monostable multivibrators). These timing and waveform applications are important in many areas of electronics and will be covered in Chapters 3, 5, 8, and 9.

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TABLE 1.1. DIODES

Type	$V_{R(max)}$[a] (V)	$I_{R(max)}$[b] (μA)	Continuous V_F @ I_F		Peak V_F @ I_F		Reverse recovery (ns)	Capacitance (10V) (pF)	Class	Comments
			(V)	(mA)	(V)	(A)				
PAD-1	45	1pA@20V	0.8	5	–	–	–	0.8	lowest I_R	Siliconix
FJT1100	30	0.001	–	–	1.1	0.05	–	1.2	very low I_R	1pA@5V, 10pA@15V
ID101	30	10pA@10V	0.8	1	1.1	0.03	–	0.8	very low I_R	Intersil; dual
1N3595	150	3	0.7	10	<1.0	0.2	3000	8.0	low I_R	1nA@125V
1N914	75	5	0.75	10	1.1	0.1	4	1.3	gen purp sig diode	indus std; same as 1N4148
1N6263	60	10	0.4	1	0.7	0.01	0	1.0	Schottky: low V_F	
1N3062	75	50	<1.0	20[b]	–	–	2	0.6	low cap, sig diode	1pF at 0 volts
1N4305	75	50	0.6	1	–	–	4	1.5	controlled V_F	
1N4002	100	50	0.9	1000	2.3	25	3500	15	1-amp rect	indus std; 7-member fam
1N4007	1000	50	0.9	1000	2.3	25	5000	10		
1N5819	40	10000	0.4	1000	1.1	20	–	50	pwr Schottky	lead mounted
1N5822	40	20000	0.45	3000	1.3	50	–	180	pwr Schottky	lead mounted
1N5625	400	50	1.1	5000	2.0	50	2500	45	5-amp rect	lead mounted
1N1183A	50	1000	1.1	40000	1.3	100	–	–	high curr rect	1N1183RA reverse

(a) $V_{R(max)}$ is repetitive peak reverse voltage, 25°C, 10μA leakage. (b) $I_{R(max)}$ is reverse leakage current at V_R and 100°C ambient temperature.

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1.24 Thévenin's theorem generalized

When capacitors and inductors are included, Thévenin's theorem must be restated: Any two-terminal network of resistors, capacitors, inductors, and signal sources is equivalent to a single complex impedance in series with a single signal source. As before, you find the impedance and the signal source from the open-circuit output voltage and the short-circuit current.

DIODES AND DIODE CIRCUITS

1.25 Diodes

The circuit elements we've discussed so far (resistors, capacitors, and inductors) are all *linear*, meaning that a doubling of the applied signal (a voltage, say) produces a doubling of the response (a current, say). This is true even for the reactive devices (capacitors and inductors). These devices are also *passive*, meaning that they don't have a built-in source of power. And they are all two-terminal devices, which is self-explanatory.



Figure 1.66. Diode.

The diode (Fig. 1.66) is a very important and useful two-terminal passive *nonlinear* device. It has the *V–I* curve shown in Figure 1.67. (In keeping with the general philosophy of this book, we will not attempt to describe the solid-state physics that makes such devices possible.)

The diode's arrow (the anode terminal) points in the direction of forward current flow. For example, if the diode is in a circuit in which a current of 10mA is flowing from anode to cathode, then (from the graph) the anode is approximately 0.5 volt more positive than the cathode; this is called the "forward voltage drop." The reverse current, which is measured in the nanoamp range for a general-purpose diode (note the different scales in the graph for forward and reverse current), is almost never of any consequence until you reach the reverse breakdown voltage (also called the peak inverse voltage, PIV), typically 75 volts for a general-purpose diode like the 1N914. (Normally you never subject a diode to voltages large enough to cause reverse breakdown; the exception is the zener diode we mentioned earlier.) Frequently, also, the forward voltage drop of about 0.5 and 0.8 volt is of little concern, and the diode can be treated as a good approximation to an ideal one-way conductor. There are other important characteristics that distinguish the thousands of diode types available, e.g., maximum forward current, capacitance, leakage current, and reverse recovery time (see Table 1.1 for characteristics of some typical diodes).

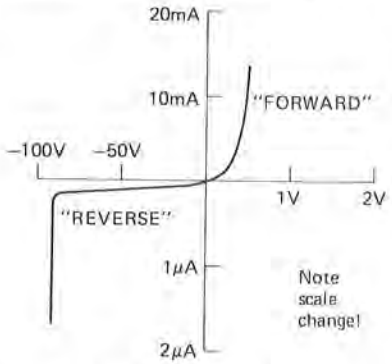


Figure 1.67. Diode *V–I* curve.

Before jumping into some circuits with diodes, we should point out two things: (a) A diode doesn't actually have a resistance (it doesn't obey Ohm's law). (b) If you put some diodes in a circuit, it won't have a Thévenin equivalent.

1.26 Rectification

A rectifier changes ac to dc; this is one of the simplest and most important applications of diodes (diodes are sometimes

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called rectifiers). The simplest circuit is shown in Figure 1.68. The "ac" symbol represents a source of ac voltage; in electronic circuits it is usually provided by a transformer, powered from the ac power line. For a sine-wave input that is much larger than the forward drop (about 0.6V for silicon diodes, the usual type), the output will look like that in Figure 1.69. If you think of the diode as a one-way conductor, you won't have any trouble understanding how the circuit works. This circuit is called a *half-wave rectifier*, because only half of the input waveform is used.

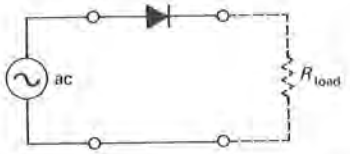


Figure 1.68. Half-wave rectifier.

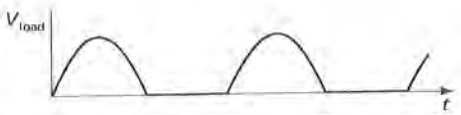


Figure 1.69

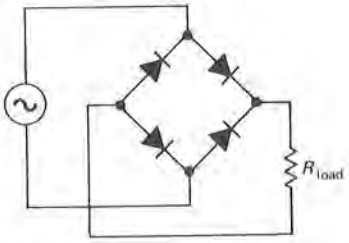


Figure 1.70. Full-wave bridge rectifier.

Figure 1.70 shows another rectifier circuit, a full-wave bridge. Figure 1.71 shows the voltage across the load for which the whole input waveform is used. The gaps at zero voltage occur because of the diodes' forward voltage drop. In this circuit, two diodes are always in series with the input; when you design low-voltage power supplies, you have to remember that.

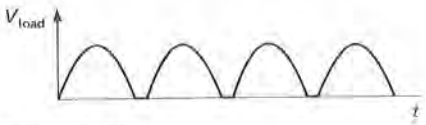


Figure 1.71

1.27 Power-supply filtering

The preceding rectified waveforms aren't good for much as they stand. They're dc only in the sense that they don't change polarity. But they still have a lot of "ripple" (periodic variations in voltage about the steady value) that has to be smoothed out in order to generate genuine dc. This we do by tacking on a low-pass filter (Fig. 1.72). Actually, the series resistor is unnecessary and is always omitted (although you sometimes see a very small resistor used to limit the peak rectifier current). The reason is that the diodes prevent flow of current back out of the capacitors, which are really serving more as energy-storage devices than as part of a classic low-pass filter. The energy stored in a capacitor is $U = \frac{1}{2}CV^2$. For C in farads and V in volts, U comes out in joules (watt-seconds).

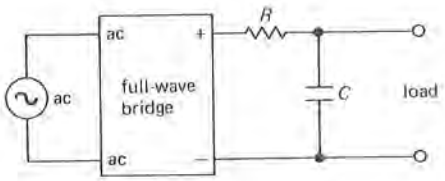


Figure 1.72

The capacitor value is chosen so that

$$R_{load}C \gg 1/f$$

(where f is the ripple frequency, here 120Hz) in order to ensure small ripple, by making the time constant for discharge much longer than the time between recharging. We will make this vague statement clearer in the next section.

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Calculation of ripple voltage

It is easy to calculate the approximate ripple voltage, particularly if it is small compared with the dc (see Fig. 1.73). The load causes the capacitor to discharge somewhat between cycles (or half cycles, for full-wave rectification). If you assume that the load current stays constant (it will, for small ripple), you have

$$\Delta V = \frac{I}{C}\Delta t \qquad \left(\text{from } I = C\frac{dV}{dt}\right)$$

Just use $1/f$ (or $1/2f$ for full-wave rectification) for Δt (this estimate is a bit on the safe side, since the capacitor begins charging again in less than a half cycle). You get

$$\Delta V = \frac{I_{\text{load}}}{fC} \qquad \text{(half wave)}$$

$$\Delta V = \frac{I_{\text{load}}}{2fC} \qquad \text{(full wave)}$$

(While teaching electronics we've noticed that students love to memorize these equations! An informal poll of the authors showed that two out of two engineers don't memorize them. Please don't waste brain cells that way – instead, learn how to derive them.)

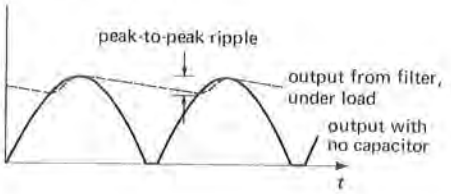


Figure 1.73. Power-supply ripple calculation.

If you wanted to do the calculation without any approximation, you would use the exact exponential discharge formula. You would be misguided in insisting on that kind of accuracy, though, for two reasons:

1. The discharge is an exponential only if the load is a resistance; many loads are not. In fact, the most common load, a *voltage regulator,* looks like a constant-current load.

2. Power supplies are built with capacitors with typical tolerances of 20% or more. Realizing the manufacturing spread, you design conservatively, allowing for the worst-case combination of component values.

In this case, viewing the initial part of the discharge as a ramp is in fact quite accurate, especially if the ripple is small, and in any case it errs in the direction of conservative design – it overestimates the ripple.

EXERCISE 1.27

Design a full-wave bridge rectifier circuit to deliver 10 volts dc with less than 0.1 volt (pp) ripple into a load drawing up to 10mA. Choose the appropriate ac input voltage, assuming 0.6 volt diode drops. Be sure to use the correct ripple frequency in your calculation.

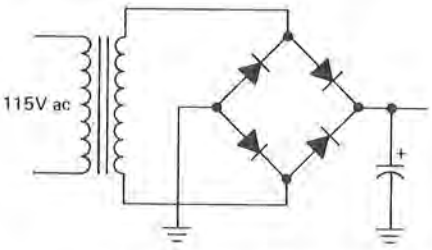


Figure 1.74. Bridge rectifier circuit. The polarity marking and curved electrode indicate a polarized capacitor, which must not be allowed to charge with the opposite polarity.

1.28 Rectifier configurations for power supplies

Full-wave bridge

A dc power supply using the bridge circuit we just discussed looks as shown in Figure 1.74. In practice, you generally buy the bridge as a prepackaged module. The smallest ones come with maximum current ratings of 1 amp average, with breakdown voltages going from 100 volts to 600 volts,

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or even 1000 volts. Giant bridge rectifiers are available with current ratings of 25 amps or more. Take a look at Table 6.4 for a few types.

Center-tapped full-wave rectifier

The circuit in Figure 1.75 is called a center-tapped full-wave rectifier. The output voltage is half what you get if you use a bridge rectifier. It is not the most efficient circuit in terms of transformer design, because each half of the secondary is used only half the time. Thus the current through the winding during that time is twice what it would be for a true full-wave circuit. Heating in the windings, calculated from Ohm's law, is I^2R, so you have four times the heating half the time, or twice the average heating of an equivalent full-wave bridge circuit. You would have to choose a transformer with a current rating 1.4 (square root of 2) times as large, as compared with the (better) bridge circuit; besides costing more, the resulting supply would be bulkier and heavier.

EXERCISE 1.28

This illustration of I^2R heating may help you understand the disadvantage of the center-tapped rectifier circuit. What fuse rating (minimum) is required to pass the current waveform shown in Figure 1.76, which has 1 amp average current? Hint: A fuse "blows out" by melting (I^2R heating) a metallic link, for steady currents larger than its rating. Assume for this problem that the thermal time constant of the fusible link is much longer than the time scale of the square wave, i.e., that the fuse responds to the value of I^2 averaged over many cycles.

Split supply

A popular variation of the center-tapped full-wave circuit is shown in Figure 1.77. It gives you split supplies (equal plus and minus voltages), which many circuits need. It is an efficient circuit, because both halves of the input waveform are used in each winding section.

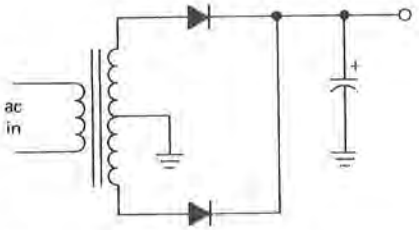


Figure 1.75. Full-wave rectifier using center-tapped transformer.

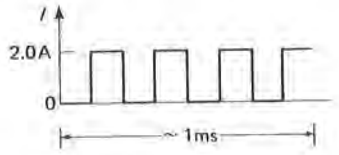


Figure 1.76

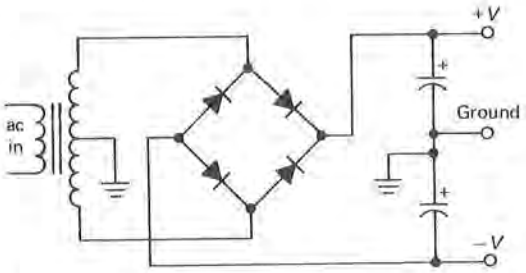


Figure 1.77. Dual-polarity (split) supply.

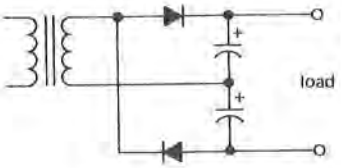


Figure 1.78. Voltage doubler.

□ *Voltage multipliers*

The circuit shown in Figure 1.78 is called a voltage doubler. Think of it as two half-wave rectifier circuits in series. It is officially a full-wave rectifier circuit, since

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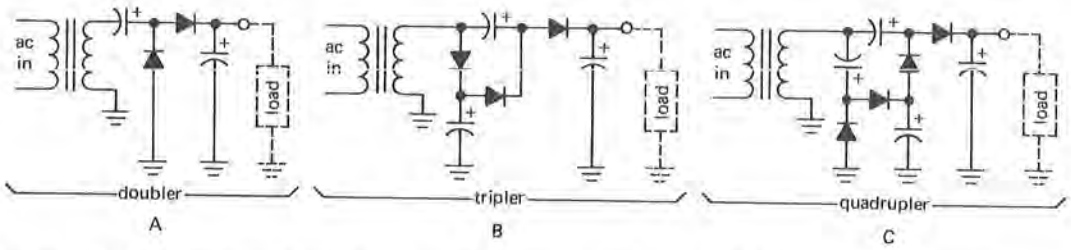


Figure 1.79. Voltage multipliers; these configurations don't require a floating voltage source.

both halves of the input waveform are used – the ripple frequency is twice the ac frequency (120Hz for the 60Hz line voltage in the United States).

Variations of this circuit exist for voltage triplers, quadruplers, etc. Figure 1.79 shows doubler, tripler, and quadrupler circuits that let you ground one side of the transformer.

1.29 Regulators

By choosing capacitors that are sufficiently large, you can reduce the ripple voltage to any desired level. This brute-force approach has two disadvantages:

1. The required capacitors may be prohibitively bulky and expensive.

2. Even with the ripple reduced to negligible levels, you still have variations of output voltage due to other causes, e.g., the dc output voltage will be roughly proportional to the ac input voltage, giving rise to fluctuations caused by input line voltage variations. In addition, changes in load current will cause the output voltage to change because of the finite internal resistances of the transformer, diode, etc. In other words, the Thévenin equivalent circuit of the dc power supply has $R > 0$.

A better approach to power-supply design is to use enough capacitance to reduce ripple to low levels (perhaps 10% of the dc voltage), then use an active *feedback circuit* to eliminate the remaining ripple. Such a feedback circuit "looks at" the output, making changes in a controllable series resistor (a transistor) as necessary to keep the output constant (Fig. 1.80).

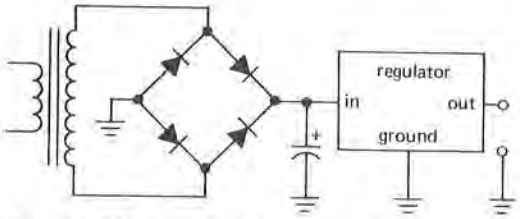


Figure 1.80. Regulated dc power supply.

These voltage regulators are used almost universally as power supplies for electronic circuits. Nowadays complete voltage regulators are available as inexpensive integrated circuits (priced under one dollar). A power supply built with a voltage regulator can be made easily adjustable and self-protecting (against short circuits, overheating, etc.), with excellent properties as a voltage source (e.g., internal resistance measured in milliohms). We will deal with regulated dc power supplies in Chapter 6.

1.30 Circuit applications of diodes

Signal rectifier

There are other occasions when you use a diode to make a waveform of one polarity only. If the input waveform isn't a sine wave, you usually don't think of it as a rectification in the sense of a power supply. For instance, you might want a train of pulses corresponding to the rising edge of a square wave. The easiest way is to rectify

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the differentiated wave (Fig. 1.81). Always keep in mind the 0.6 volt (approximately) forward drop of the diode. This circuit, for instance, gives no output for square waves smaller than 0.6 volt pp. If this is a problem, there are various tricks to circumvent this limitation. One possibility is to use *hot carrier diodes* (Schottky diodes), with a forward drop of about 0.25 volt (another device called a *back diode* has nearly zero forward drop, but its usefulness is limited by very low reverse breakdown voltage).

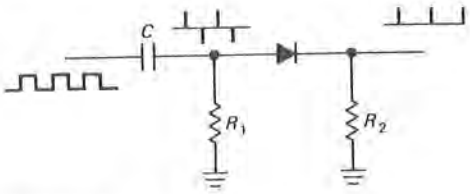


Figure 1.81

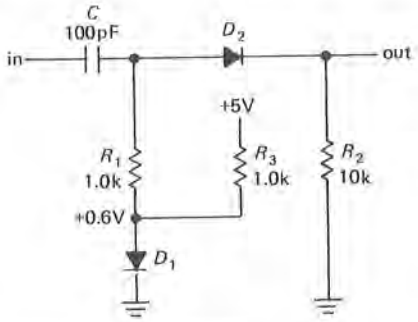


Figure 1.82. Compensating the forward voltage drop of a diode signal rectifier.

A possible circuit solution to this problem of finite diode drop is shown in Figure 1.82. Here D_1 compensates D_2's forward drop by providing 0.6 volt of *bias* to hold D_2 at the threshold of conduction. Using a diode (D_1) to provide the bias (rather than, say, a voltage divider) has several advantages: There is nothing to adjust, the compensation will be nearly perfect, and changes of the forward drop (e.g., with changing temperature) will be compensated properly. Later we will see other instances of matched-pair compensation of forward drops in diodes, transistors, and FETs: it is a simple and powerful trick.

Diode gates

Another application of diodes, which we will recognize later under the general heading of *logic*, is to pass the higher of two voltages without affecting the lower. A good example is *battery backup*, a method of keeping something running (e.g, a precision electronic clock) that must not stop when there is a power failure. Figure 1.83 shows a circuit that does the job. The battery does nothing until the power fails; then it takes over without interruption.

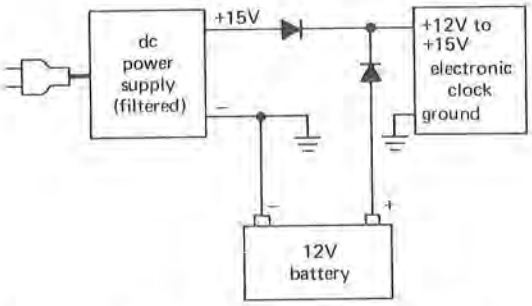


Figure 1.83. Diode OR gate: battery backup.

EXERCISE 1.29

Make a simple modification to the circuit so that the battery is charged by the dc supply (when power is on, of course) at a current of 10mA (such a circuit is necessary to maintain the battery's charge).

Diode clamps

Sometimes it is desirable to limit the range of a signal (i.e., prevent it from exceeding certain voltage limits) somewhere in a circuit. The circuit shown in Figure 1.84 will accomplish this. The diode prevents the output from exceeding about +5.6 volts,

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with no effect on voltages less than that (including negative voltages); the only limitation is that the input must not go so negative that the reverse breakdown voltage of the diode is exceeded (e.g., −70V for a 1N914). Diode clamps are standard equipment on all inputs in the CMOS family of digital logic. Without them, the delicate input circuits are easily destroyed by static electricity discharges during handling.

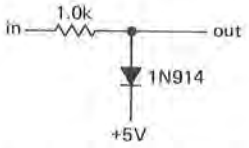


Figure 1.84. Diode voltage clamp.

EXERCISE 1.30

Design a symmetrical clamp, i.e., one that confines a signal to the range −5.6 volts to +5.6 volts.

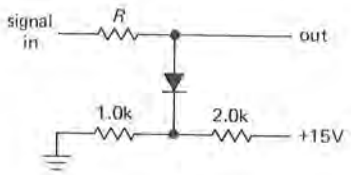


Figure 1.85

A voltage divider can provide the reference voltage for a clamp (Fig. 1.85). In this case you must ensure that the impedance looking into the voltage divider (R_{vd}) is small compared with R, because what you have looks as shown in Figure 1.86 when the voltage divider is replaced by its Thévenin equivalent circuit. When the diode conducts (input voltage exceeds clamp voltage), the output is really just the output of a voltage divider, with the Thévenin equivalent resistance of the voltage reference as the lower resistor (Fig. 1.87). So, for the values shown, the output of the clamp for a triangle-wave input would look as shown in Figure 1.88. The problem is that the voltage divider doesn't provide a stiff reference, in the language of electronics. A stiff voltage source is one that doesn't bend easily, i.e., it has low internal (Thévenin) impedance.

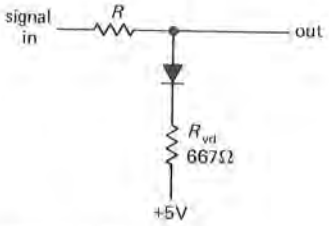


Figure 1.86

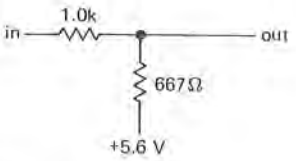


Figure 1.87

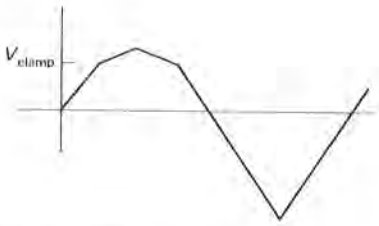


Figure 1.88

A simple way to stiffen the clamp circuit of Figure 1.85, at least for *high-frequency* signals, is to add a bypass capacitor across the 1k resistor. For example, a 15μF capacitor to ground reduces the impedance seen looking into the divider below 10 ohms for frequencies above 1kHz. (You could similarly add a bypass capacitor across D_1 in Fig. 1.82.) Of course, the effectiveness of this trick drops at low frequencies, and it does nothing at dc.

In practice, the problem of finite impedance of the voltage-divider reference can be easily solved using a transistor or

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operational amplifier (op-amp). This is usually a better solution than using very small resistor values, because it doesn't consume large currents, yet it provides impedances of a few ohms or less. Furthermore, there are other ways to construct a clamp, using an op-amp as part of the clamp circuit. You will see these methods in Chapter 4.

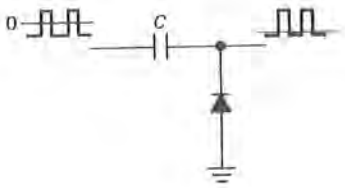


Figure 1.89. dc restoration.

One interesting clamp application is "dc restoration" of a signal that has been ac-coupled (capacitively coupled). Figure 1.89 shows the idea. This is particularly important for circuits whose inputs look like diodes (e.g., a transistor with grounded emitter); otherwise an ac-coupled signal will just fade away.

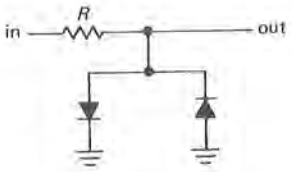


Figure 1.90. Diode limiter.

Limiter

One last clamp circuit is shown in Figure 1.90. This circuit limits the output "swing" (again, a common electronics term) to one diode drop, roughly 0.6 volt. That might seem awfully small, but if the next stage is an amplifier with large voltage amplification, its input will always be near zero volts; otherwise the output is in "saturation" (e.g., if the next stage has a gain of 1000 and operates from ± 15V supplies, its input must stay in the range ± 15mV in order for its output not to saturate). This clamp circuit is often used as input protection for a high-gain amplifier.

Diodes as nonlinear elements

To a good approximation the forward current through a diode is proportional to an exponential function of the voltage across it at a given temperature (for a discussion of the exact law, see Section 2.10). So you can use a diode to generate an output voltage proportional to the logarithm of a current (Fig. 1.91). Because V hovers in the region of 0.6 volt, with only small voltage changes that reflect input current variations, you can generate the input current with a resistor if the input voltage is much larger than a diode drop (Fig. 1.92).

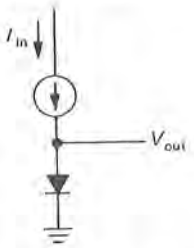


Figure 1.91. Exploiting the diode's nonlinear V–I curve: logarithmic converter.

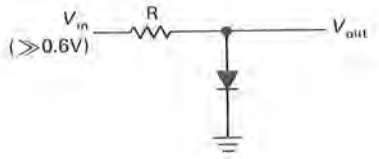


Figure 1.92

In practice, you may want an output voltage that isn't offset by the 0.6 volt diode drop. In addition, it would be nice to have a circuit that is insensitive to changes in temperature. The method of diode drop compensation is helpful here (Fig. 1.93). R_1 makes D_2 conduct, holding point A at about -0.6 volt. Point B is then near ground (making I_{in} accurately proportional

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to V_{in}, incidentally). As long as the two (identical) diodes are at the same temperature, there is good cancellation of the forward drops, except, of course, for the difference owing to input current through D_1, which produces the desired output. In this circuit, R_1 should be chosen so that the current through D_2 is much larger than the maximum input current, in order to keep D_2 in conduction.

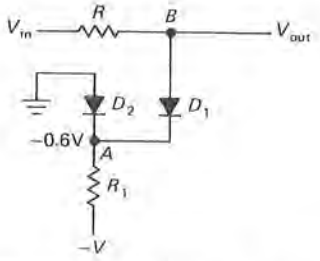


Figure 1.93. Diode drop compensation in the logarithmic converter.

In the chapter on op-amps we will examine better ways of constructing logarithmic converter circuits, along with careful methods of temperature compensation. With such methods it is possible to construct logarithmic converters accurate to a few percent over six decades or more of input current. A better understanding of diode and transistor characteristics, along with an understanding of op-amps, is necessary first. This section is meant to serve only as an introduction for things to come.

1.31 Inductive loads and diode protection

What happens if you open a switch that is providing current to an inductor? Because inductors have the property

$$V = L\frac{dI}{dt}$$

it is not possible to turn off the current suddenly, since that would imply an infinite voltage across the inductor's terminals. What happens instead is that the voltage across the inductor suddenly rises and keeps rising until it forces current to flow. Electronic devices controlling inductive loads can be easily damaged, especially the component that "breaks down" in order to satisfy the inductor's craving for continuity of current. Consider the circuit in Figure 1.94. The switch is initially closed, and current is flowing through the inductor (which might be a relay, as will be described later). When the switch is opened, the inductor "tries" to keep current flowing from A to B, as it had been. That means that terminal B goes positive relative to terminal A. In a case like this it may go 1000 volts positive before the switch contact "blows over." This shortens the life of the switch and also generates impulsive interference that may affect other circuits nearby. If the switch happens to be a transistor, it would be an understatement to say that its life is shortened; its life is ended!

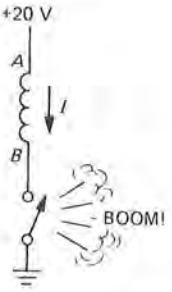


Figure 1.94. Inductive "kick."

The best solution is to put a diode across the inductor, as in Figure 1.95. When the switch is on, the diode is back-biased (from the dc drop across the inductor's winding resistance). At turn-off the diode goes into conduction, putting the switch terminal a diode drop above the positive supply voltage. The diode must be able to handle the initial diode current, which equals the steady current that had been flowing through the inductor; something like a 1N4004 is fine for nearly all cases.

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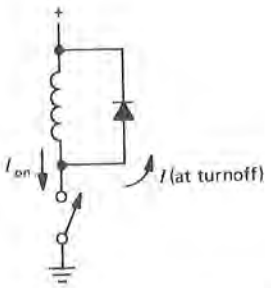


Figure 1.95. Blocking inductive kick.

The only disadvantage of this protection circuit is that it lengthens the decay of current through the inductor, since the rate of change of inductor current is proportional to the voltage across it. For applications where the current must decay quickly (high-speed impact printers, high-speed relays, etc.), it may be better to put a resistor across the inductor, choosing its value so that $V_{supply} + IR$ is less than the maximum allowed voltage across the switch. (For fastest decay with a given maximum voltage, a zener could be used instead, giving a ramp-down of current rather than an exponential decay.)

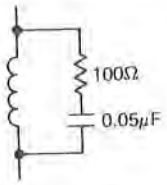


Figure 1.96. RC "snubber" for suppressing inductive kick.

For inductors driven from ac (transformers, ac relays), the diode protection just described will not work, since the diode will conduct on alternate half cycles when the switch is closed. In that case a good solution is an RC "snubber" network (Fig. 1.96). The values shown are typical for small inductive loads driven from the ac power line. Such a snubber should be included in all instruments that run from the ac power line, since a transformer is inductive. An alternative protection device is a metal-oxide varistor, or transient suppressor, an inexpensive device that looks something like a disc ceramic capacitor and behaves electrically like a bi-directional zener diode. They are available at voltage ratings from 10 to 1000 volts and can handle transient currents up to thousands of amperes (see Section 6.11 and Table 6.2). Putting a transient suppressor across the ac power-line terminals makes good sense in a piece of electronic equipment, not only to prevent inductive spike interference to other nearby instruments but also to prevent occasional large power-line spikes from damaging the instrument itself.

OTHER PASSIVE COMPONENTS

In the following sections we would like to introduce briefly an assortment of miscellaneous but essential components. If you are experienced in electronic construction, you may wish to proceed to the next chapter.

1.32 Electromechanical devices

Switches

These mundane but important devices seem to wind up in most electronic equipment. It is worth spending a few paragraphs on the subject. Figure 1.97 shows some common switch types.

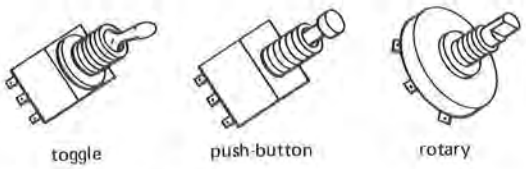


Figure 1.97. Panel switches.

Toggle switches. The simple toggle switch is available in various configurations, depending on the number of poles; Figure 1.98 shows the usual ones (SPDT

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indicates a single-pole double-throw switch, etc.). Toggle switches are also available with "center OFF" positions and with up to 4 poles switched simultaneously. Toggle switches are always "break before make," e.g., the moving contact never connects to both terminals in an SPDT switch.

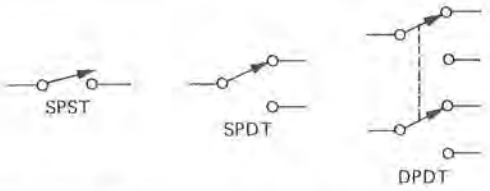


Figure 1.98. Fundamental switch types.

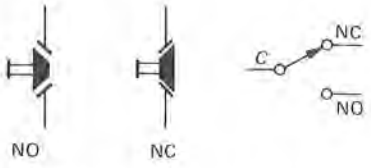


Figure 1.99. Momentary-contact (push-button) switches.

Push-button switches. Push-button switches are useful for momentary-contact applications; they are drawn schematically as shown in Figure 1.99 (NO and NC mean normally open and normally closed). For SPDT momentary-contact switches, the terminals must be labeled NO and NC, whereas for SPST types the symbol is self-explanatory. Momentary-contact switches are always "break before make." In the electrical (as opposed to electronic) industry, the terms form A, form B, and form C are used to mean SPST (NO), SPST (NC), and SPDT, respectively.

Rotary switches. Rotary switches are available with many poles and many positions, often as kits with individual wafers and shaft hardware. Both shorting (make before break) and nonshorting (break before make) types are available, and they can be mixed on the same switch. In many applications the shorting type is useful to prevent an open circuit between switch positions, because circuits can go amok with unconnected inputs. Nonshorting types are necessary if the separate lines being switched to one common line must not ever be connected to each other.

Other switch types. In addition to these basic switch types, there are available various exotic switches such as Hall-effect switches, reed switches, proximity switches, etc. All switches carry maximum current and voltage ratings; a small toggle switch might be rated at 150 volts and 5 amps. Operation with inductive loads drastically reduces switch life because of arcing during turn-off.

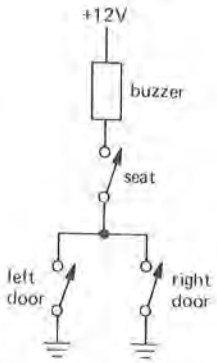


Figure 1.100

Switch examples. As an example of what can be done with simple switches, let's consider the following problem: Suppose you want to sound a warning buzzer if the driver of a car is seated and one of the car doors is open. Both doors and the driver's seat have switches, all normally open. Figure 1.100 shows a circuit that does what you want. If one OR the other door is open (switch closed) AND the seat switch is closed, the buzzer sounds. The words OR and AND are used in a logic sense here, and we will see this example again in Chapters 2 and 8 when we talk about transistors and digital logic.

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Figure 1.101 shows a classic switch circuit used to turn a ceiling lamp on or off from a switch at either of two entrances to a room.

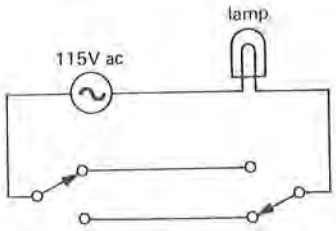


Figure 1.101. Electrician's "three-way" switch wiring.

EXERCISE 1.31

Although few electronic circuit designers know how, every *electrician* can wire up a light fixture so that any of N switches can turn it on or off. See if you can figure out this generalization of Figure 1.101. It requires two SPDT switches and $N-2$ DPDT switches. (Hint: First figure out how to use a DPDT switch to crisscross a pair of wires.)

Relays

Relays are electrically controlled switches. In the usual type, a coil pulls in an armature when sufficient coil current flows. Many varieties are available, including "latching" and "stepping" relays; the latter provided the cornerstone for telephone switching stations, and they're still popular in pinball machines. Relays are available for dc or ac excitation, and coil voltages from 5 volts up to 110 volts are common. "Mercury-wetted" and "reed" relays are intended for high-speed (~1ms) applications, and giant relays intended to switch thousands of amps are used by power companies. Many previous relay applications are now handled with transistor or FET switches, and devices known as solid-state relays are now available to handle ac switching applications. The primary uses of relays are in remote switching and high-voltage (or high-current) switching. Because it is important to keep electronic circuits electrically isolated from the ac power line, relays are useful to switch ac power while keeping the control signals electrically isolated.

Connectors

Bringing signals in and out of an instrument, routing signal and dc power around between the various parts of an instrument, providing flexibility by permitting circuit boards and larger modules of the instrument to be unplugged (and replaced) – these are the functions of the connector, an essential ingredient (and usually the most unreliable part) of any piece of electronic equipment. Connectors come in a bewildering variety of sizes and shapes.

Single-wire connectors. The simplest kind of connector is the simple pin jack or banana jack used on multimeters, power supplies, etc. It is handy and inexpensive, but not as useful as the shielded-cable or multiwire connectors you often need. The humble binding post is another form of single-wire connector, notable for the clumsiness it inspires in those who try to use it.

Shielded-cable connectors. In order to prevent capacitive pickup, and for other reasons we'll go into in Chapter 13, it is usually desirable to pipe signals around from one instrument to another in shielded coaxial cable. The most popular connector is the BNC ("baby N" connector) type that adorns most instrument front panels. It connects with a quarter-turn twist and completes both the shield (ground) circuit and inner conductor (signal) circuit simultaneously. Like all connectors used to mate a cable to an instrument, it comes in both panel-mounting and cable-terminating varieties (Fig. 1.102).

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Figure 1.102. BNC connectors are the most popular type for use with shielded (coaxial) cable. From left to right: A male connector on a length of cable, a standard panel-mounted female connector, two varieties of insulated panel-mounted female connectors, and a BNC "T," a handy device to have in the laboratory.

Among the other connectors for use with coaxial cable are the TNC (a close cousin of the BNC, but with threaded outer shell), the high-performance but bulky type N, the miniature SMA, the subminiature LEMO and SMC, and the MHV, a high-voltage version of the standard BNC connector. The so-called phono jack used in audio equipment is a nice lesson in bad design, because the inner conductor mates before the shield when you plug it in; furthermore, the design of the connector is such that both shield and center conductor tend to make poor contact. You've undoubtedly *heard* the results! Not to be outdone, the television industry has responded with its own bad standard, the type F coax "connector," which uses the unsupported inner wire of the coax as the pin of the male plug, and a shoddy arrangement to mate the shield.

Multipin connectors. Very frequently electronic instruments demand multiwire cables and connectors. There are literally dozens of different kinds. The simplest example is a 3-wire line cord connector. Among the more popular are the excellent type D subminiature, the Winchester MRA series, the venerable MS type, and the flat ribbon-cable mass-termination connectors (Fig. 1.103).



Figure 1.103. A selection of popular multipin connectors. From left to right: *D* subminiature type, available in panel- and cable-mounting versions, with 9, 15, 25, 37, or 50 pins; the venerable MS-type connector, available in many (too many!) pin and mounting configurations, including types suitable for shielded cables; a miniature rectangular connector (Winchester MRA type) with integral securing jackscrews, available in several sizes; a circuit-board-mounting mass-termination connector with its mating female ribbon connector.

Beware of connectors that can't tolerate being dropped on the floor (the miniature hexagon connectors are classic) or that don't provide a secure locking mechanism (e.g., the Jones 300 series).

Card-edge connectors. The most common method used to make connection to printed-circuit cards is the card-edge connector, which mates to a row of gold-plated contacts at the edge of the card. Card-edge connectors may have from 15 to 100 pins, and they come with different lug styles according to the method of connection. You can solder them to a "motherboard" or "backplane," which is itself just another printed-circuit board containing the interconnecting wiring between the individual circuit cards. Alternatively, you may want to use edge connectors with standard solder-lug terminations, particularly in a system with only a few cards (see Chapter 12 for some photographs).

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1.33 Indicators

Meters

To read out the value of some voltage or current, you have a choice between the time-honored moving-pointer type of meter and digital-readout meters. The latter are more expensive and more accurate. Both types are available in a variety of voltage and current ranges. There are, in addition, exotic panel meters that read out such things as VU (volume units, an audio dB scale), expanded-scale ac volts (e.g., 105 to 130 volts), temperature (from a thermocouple), percentage motor load, frequency, etc. Digital panel meters often provide the option of logic-level outputs, in addition to the visible display, for internal use by the instrument.

Lamps and LEDs

Flashing lights, screens full of numbers and letters, eerie sounds – these are the stuff of science fiction movies, and except for the latter, they form the subject of lamps and displays (see Section 9.10). Small incandescent lamps used to be standard for front-panel indicators, but they have been replaced by light-emitting diodes (LEDs). The latter behave electrically like ordinary diodes, but with a forward voltage drop in the range of 1.5 to 2.5 volts. When current flows in the forward direction, they light up. Typically, 5mA to 20mA produces adequate brightness. LEDs are cheaper than incandescent lamps, they last forever, and they are even available in three colors (red, yellow, and green). They come in convenient panel-mounting packages; some even provide built-in current limiting.

LEDs are also used for digital displays, most often the familiar 7-segment numeric display you see in calculators. For displaying letters as well as numbers (alphanumeric display), you can get 16-segment displays or dot-matrix displays. For low power or outdoor use, liquid-crystal displays are superior.

1.34 Variable components

Resistors

Variable resistors (also called volume controls, potentiometers, pots, or trimmers) are useful as panel controls or internal adjustments in circuits. The most common panel type is known as a 2 watt type AB potentiometer; it uses the same basic material as the fixed carbon-composition resistor, with a rotatable "wiper" contact. Other panel types are available with ceramic or plastic resistance elements, with improved characteristics. Multiturn types (3, 5, or 10 turns) are available, with counting dials, for improved resolution and linearity. "Ganged" pots (several independent sections on one shaft) are also manufactured, although in limited variety, for applications that demand them.

For use inside an instrument, rather than on the front panel, *trimmer pots* come in single-turn and multiturn styles, most intended for printed-circuit mounting. These are handy for calibration adjustments of the "set-and-forget" type. Good advice: Resist the temptation to use lots of trimmers in your circuits. Use good design instead.

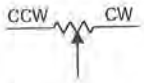


Figure 1.104. Potentiometer (3-terminal variable resistor).

The symbol for a variable resistor, or pot, is shown in Figure 1.104. Sometimes the symbols CW and CCW are used to indicate clockwise and counterclockwise.

One important point about variable resistors: Don't attempt to use a potentiometer as a substitute for a precise resistor value somewhere within a circuit. This is tempting, because you can trim the resistance to the value you want. The trouble is that potentiometers are not as stable as good (1%) resistors, and in addition

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they may not have good resolution (i.e., they can't be set to a precise value). If you must have a precise and settable resistor value somewhere, use a combination of a 1% (or better) precision resistor and a potentiometer, with the fixed resistor contributing most of the resistance. For example, if you need a 23.4k resistor, use a 22.6k (a 1% value) 1% fixed resistor in series with a 2k trimmer pot. Another possibility is to use a series combination of several precision resistors, choosing the last (and smallest) resistor to give the desired series resistance.

As you will see later, it is possible to use FETs as voltage-controlled variable resistors in some applications. Transistors can be used as variable-gain amplifiers, again controlled by a voltage. Keep an open mind when design brainstorming.



Figure 1.105. Variable capacitor.

Capacitors

Variable capacitors are primarily confined to the smaller capacitance values (up to about 1000pF) and are commonly used in radiofrequency (RF) circuits. Trimmers are available for in-circuit adjustments, in addition to the panel type for user tuning. Figure 1.105 shows the symbol for a variable capacitor.

Diodes operated with applied reverse voltage can be used as voltage-variable capacitors; in this application they're called varactors, or sometimes varicaps or epicaps. They're very important in RF applications, especially automatic frequency control (AFC), modulators, and parametric amplifiers.

Inductors

Variable inductors are usually made by arranging to move a piece of core material in a fixed coil. In this form they're available with inductances ranging from microhenrys to henrys, typically with a 2:1 tuning range for any given inductor. Also available are rotary inductors (coreless coils with a rolling contact).

Transformers

Variable transformers are very handy devices, especially the ones operated from the 115 volt ac line. They're usually "autoformers," which means that they have only one winding, with a sliding contact. They're also commonly called Variacs, and they are made by Technipower, Superior Electric, and others. Typically they provide 0 to 135 volts ac output when operated from 115 volts, and they come in current ratings from 1 amp to 20 amps or more. They're good for testing instruments that seem to be affected by power-line variations, and in any case to verify worst-case performance. Warning: Don't forget that the output is not electrically isolated from the power line, as it would be with a transformer!

ADDITIONAL EXERCISES

(1) Find the Norton equivalent circuit (a current source in parallel with a resistor) for the voltage divider in Figure 1.106. Show that the Norton equivalent gives the same output voltage as the actual circuit when loaded by a 5k resistor.

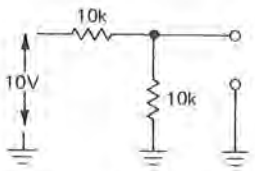


Figure 1.106

(2) Find the Thévenin equivalent for the circuit shown in Figure 1.107. Is it the

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same as the Thévenin equivalent for exercise 1?

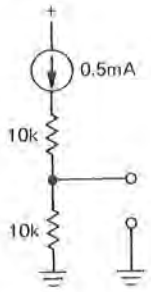


Figure 1.107

(3) Design a "rumble filter" for audio. It should pass frequencies greater than 20Hz (set the −3dB point at 10Hz). Assume zero source impedance (perfect voltage source) and 10k (minimum) load impedance (that's important so that you can choose R and C such that the load doesn't affect the filter operation significantly).

(4) Design a "scratch filter" for audio signals (3dB down at 10kHz). Use the same source and load impedances as in exercise 3.

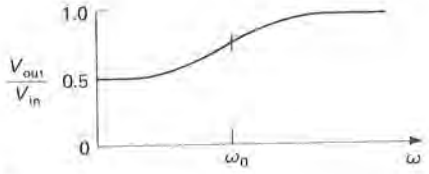


Figure 1.108

(5) How would you make a filter with Rs and Cs to give the response shown in Figure 1.108?

(6) Design a bandpass RC filter (as in Fig. 1.109); f_1 and f_2 are the 3dB points. Choose impedances so that the first stage isn't much affected by the loading of the second stage.

(7) Sketch the output for the circuit shown in Figure 1.110.

(8) Design an oscilloscope "×10 probe"

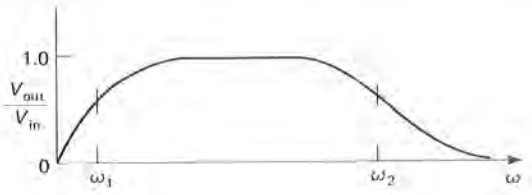


Figure 1.109

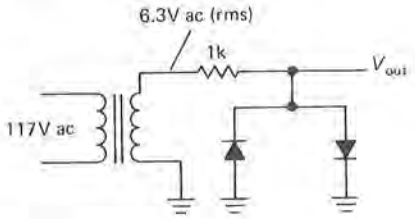


Figure 1.110

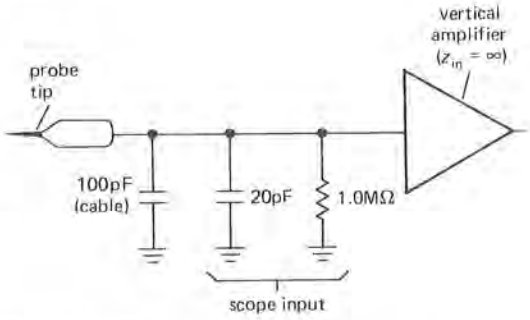


Figure 1.111

(see Appendix A) to use with a scope whose input impedance is 1MΩ in parallel with 20pF. Assume that the probe cable adds an additional 100pF and that the probe components are placed at the tip end (rather than at the scope end) of the cable (Fig. 1.111). The resultant network should have 20dB (×10) attenuation at all frequencies, including dc. The reason for using a ×10 probe is to increase the load impedance seen by the circuit under test, which reduces loading effects. What input impedance (R in parallel with C) does your ×10 probe present to the circuit under test, when used with the scope?

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TRANSISTORS

CHAPTER 2

INTRODUCTION

The transistor is our most important example of an "active" component, a device that can amplify, producing an output signal with more power in it than the input signal. The additional power comes from an external source of power (the power supply, to be exact). Note that voltage amplification isn't what matters, since, for example, a step-up transformer, a "passive" component just like a resistor or capacitor, has voltage gain but no power gain. Devices with power gain are distinguishable by their ability to make oscillators, by feeding some output signal back into the input.

It is interesting to note that the property of power amplification seemed very important to the inventors of the transistor. Almost the first thing they did to convince themselves that they had really invented something was to power a loudspeaker from a transistor, observing that the output signal sounded louder than the input signal.

The transistor is the essential ingredient of every electronic circuit, from the simplest amplifier or oscillator to the most elaborate digital computer. Integrated circuits (ICs), which have largely replaced circuits constructed from discrete transistors, are themselves merely arrays of transistors and other components built from a single chip of semiconductor material.

A good understanding of transistors is very important, even if most of your circuits are made from ICs, because you need to understand the input and output properties of the IC in order to connect it to the rest of your circuit and to the outside world. In addition, the transistor is the single most powerful resource for interfacing, whether between ICs and other circuitry or between one subcircuit and another. Finally, there are frequent (some might say too frequent) situations where the right IC just doesn't exist, and you have to rely on discrete transistor circuitry to do the job. As you will see, transistors have an excitement all their own. Learning how they work can be great fun.

Our treatment of transistors is going to be quite different from that of many other books. It is common practice to use the h-parameter model and equivalent

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circuit. In our opinion that is unnecessarily complicated and unintuitive. Not only does circuit behavior tend to be revealed to you as something that drops out of elaborate equations, rather than deriving from a clear understanding in your own mind as to how the circuit functions; you also have the tendency to lose sight of which parameters of transistor behavior you can count on and, more important, which ones can vary over large ranges.

In this chapter we will build up instead a very simple introductory transistor model and immediately work out some circuits with it. Soon its limitations will become apparent; then we will expand the model to include the respected Ebers-Moll conventions. With the Ebers-Moll equations and a simple 3-terminal model, you will have a good understanding of transistors; you won't need to do a lot of calculations, and your designs will be first-rate. In particular, they will be largely independent of the poorly controlled transistor parameters such as current gain.

Some important engineering notation should be mentioned. Voltage at a transistor terminal (relative to ground) is indicated by a single subscript (C, B, or E): V_C is the collector voltage, for instance. Voltage between two terminals is indicated by a double subscript: V_{BE} is the base-to-emitter voltage drop, for instance. If the same letter is repeated, that means a power-supply voltage: V_{CC} is the (positive) power-supply voltage associated with the collector, and V_{EE} is the (negative) supply voltage associated with the emitter.

2.01 First transistor model: current amplifier

Let's begin. A transistor is a 3-terminal device (Fig. 2.1) available in 2 flavors (*npn* and *pnp*), with properties that meet the following rules for *npn* transistors (for *pnp* simply reverse all polarities):

1. The collector must be more positive than the emitter.

2. The base-emitter and base-collector circuits behave like diodes (Fig. 2.2). Normally the base-emitter diode is conducting and the base-collector diode is reverse-biased, i.e., the applied voltage is in the opposite direction to easy current flow.

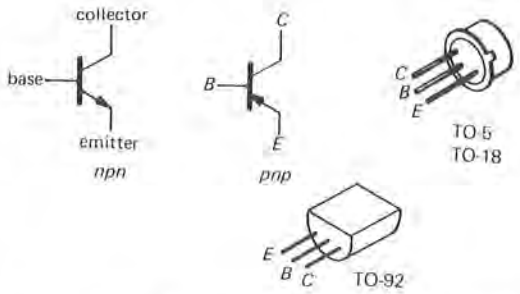


Figure 2.1. Transistor symbols, and small transistor packages.

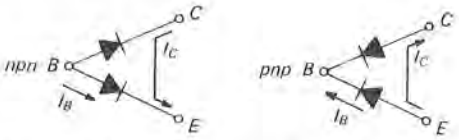


Figure 2.2. An ohmmeter's view of a transistor's terminals.

3. Any given transistor has maximum values of I_C, I_B, and V_{CE} that cannot be exceeded without costing the exceeder the price of a new transistor (for typical values, see Table 2.1). There are also other limits, such as power dissipation ($I_C V_{CE}$), temperature, V_{BE}, etc., that you must keep in mind.

4. When rules 1–3 are obeyed, I_C is roughly proportional to I_B and can be written as

$$I_C = h_{FE} I_B = \beta I_B$$

where h_{FE}, the current gain (also called beta), is typically about 100. Both I_C and I_E flow to the emitter. Note: The collector current is not due to forward conduction of the base-collector diode;

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that diode is reverse-biased. Just think of it as "transistor action."

Property 4 gives the transistor its usefulness: A small current flowing into the base controls a much larger current flowing into the collector.

Warning: h_{FE} is not a "good" transistor parameter; for instance, its value can vary from 50 to 250 for different specimens of a given transistor type. It also depends upon the collector current, collector-to-emitter voltage, and temperature. *A circuit that depends on a particular value for h_{FE} is a bad circuit.*

Note particularly the effect of property 2. This means you can't go sticking a voltage across the base-emitter terminals, because an enormous current will flow if the base is more positive than the emitter by more than about 0.6 to 0.8 volt (forward diode drop). This rule also implies that an operating transistor has $V_B \approx V_E + 0.6$ volt ($V_B = V_E + V_{BE}$). Again, polarities are normally given for *npn* transistors; reverse them for *pnp*.

Let us emphasize again that you should not try to think of the collector current as diode conduction. It isn't, because the collector-base diode normally has voltages applied across it in the reverse direction. Furthermore, collector current varies very little with collector voltage (it behaves like a not-too-great current source), unlike forward diode conduction, where the current rises very rapidly with applied voltage.

SOME BASIC TRANSISTOR CIRCUITS

2.02 Transistor switch

Look at the circuit in Figure 2.3. This application, in which a small control current enables a much larger current to flow in another circuit, is called a transistor switch. From the preceding rules it is easy to understand. When the mechanical switch is open, there is no base current. So, from

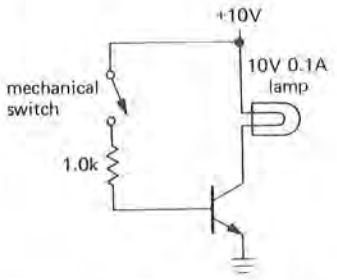


Figure 2.3. Transistor switch example.

rule 4, there is no collector current. The lamp is off.

When the switch is closed, the base rises to 0.6 volt (base-emitter diode is in forward conduction). The drop across the base resistor is 9.4 volts, so the base current is 9.4mA. Blind application of rule 4 gives $I_C = 940$mA (for a typical beta of 100). That is wrong. Why? Because rule 4 holds only if rule 1 is obeyed; at a collector current of 100mA the lamp has 10 volts across it. To get a higher current you would have to pull the collector below ground. A transistor can't do this, and the result is what's called saturation – the collector goes as close to ground as it can (typical saturation voltages are about 0.05–0.2V, see Appendix G) and stays there. In this case, the lamp goes on, with its rated 10 volts across it.

Overdriving the base (we used 9.4mA when 1.0mA would have barely sufficed) makes the circuit conservative; in this particular case it is a good idea, since a lamp draws more current when cold (the resistance of a lamp when cold is 5 to 10 times lower than its resistance at operating current). Also transistor beta drops at low collector-to-base voltages, so some extra base current is necessary to bring a transistor into full saturation (see Appendix G). Incidentally, in a real circuit you would probably put a resistor from base to ground (perhaps 10k in this case) to make sure the base is at ground with the switch open. It wouldn't affect the

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"on" operation, because it would sink only 0.06mA from the base circuit.

There are certain cautions to be observed when designing transistor switches:
1. Choose the base resistor conservatively to get plenty of excess base current, especially when driving lamps, because of the reduced beta at low V_{CE}. This is also a good idea for high-speed switching, because of capacitive effects and reduced beta at very high frequencies (many megahertz). A small "speedup" capacitor is often connected across the base resistor to improve high-speed performance.
2. If the load swings below ground for some reason (e.g., it is driven from ac, or it is inductive), use a diode in series with the collector (or a diode in the reverse direction to ground) to prevent collector-base conduction on negative swings.
3. For inductive loads, protect the transistor with a diode across the load, as shown in Figure 2.4. Without the diode the inductor will swing the collector to a large positive voltage when the switch is opened, most likely exceeding the collector-emitter breakdown voltage, as the inductor tries to maintain its "on" current from V_{CC} to the collector (see the discussion of inductors in Section 1.31).

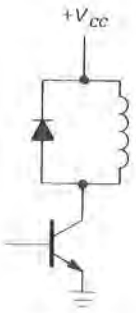


Figure 2.4. Always use a suppression diode when switching an inductive load.

Transistor switches enable you to switch very rapidly, typically in a small fraction of a microsecond. Also, you can switch many different circuits with a single control signal. One further advantage is the possibility of remote *cold switching*, in which only dc control voltages snake around through cables to reach front-panel switches, rather than the electronically inferior approach of having the signals themselves traveling through cables and switches (if you run lots of signals through cables, you're likely to get capacitive pickup as well as some signal degradation).

"Transistor man"

Figure 2.5 presents a cartoon that will help you understand some limits of transistor

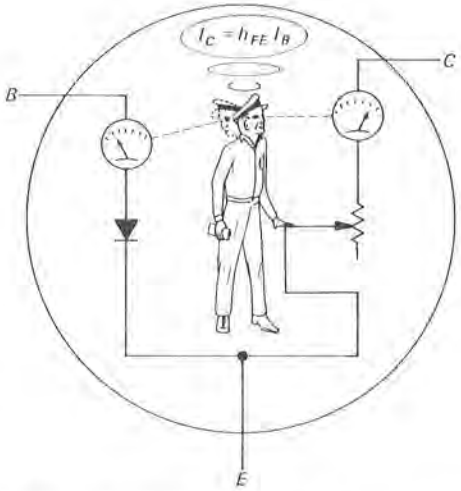


Figure 2.5. "Transistor man" observes the base current, and adjusts the output rheostat in an attempt to maintain the output current h_{FE} times larger.

behavior. The little man's perpetual task in life is to try to keep $I_C = h_{FE}I_B$; however, he is only allowed to turn the knob on the variable resistor. Thus he can go from a short circuit (saturation) to an open circuit (transistor in the "off" state), or anything in between, but he isn't allowed to use batteries, current sources, etc. One warning is in order here: Don't think that the collector of a transistor

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looks like a resistor. It doesn't. Rather, it looks approximately like a poor-quality constant-current sink (the value of current depending on the signal applied to the base), primarily because of this little man's efforts.

Another thing to keep in mind is that, at any given time, a transistor may be (a) cut off (no collector current), (b) in the active region (some collector current, and collector voltage more than a few tenths of a volt above the emitter), or (c) in saturation (collector within a few tenths of a volt of the emitter). See Appendix G on transistor saturation for more details.

2.03 Emitter follower

Figure 2.6 shows an example of an *emitter follower*. It is called that because the output terminal is the emitter, which follows the input (the base), less one diode drop:

$V_E \approx V_B - 0.6$ volt

The output is a replica of the input, but 0.6 to 0.7 volt less positive. For this circuit, V_{in} must stay at +0.6 volt or more, or else the output will sit at ground. By returning the emitter resistor to a negative supply voltage, you can permit negative voltage swings as well. Note that there is no collector resistor in an emitter follower.

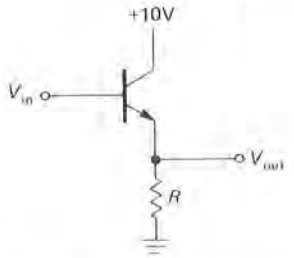


Figure 2.6. Emitter follower.

At first glance this circuit may appear useless, until you realize that the input impedance is much larger than the output impedance, as will be demonstrated shortly. This means that the circuit requires less power from the signal source to drive a given load than would be the case if the signal source were to drive the load directly. Or a signal of some internal impedance (in the Thévenin sense) can now drive a load of comparable or even lower impedance without loss of amplitude (from the usual voltage-divider effect). In other words, an emitter follower has current gain, even though it has no voltage gain. It has power gain. Voltage gain isn't everything!

Impedances of sources and loads

This last point is very important and is worth some more discussion before we calculate in detail the beneficial effects of emitter followers. In electronic circuits, you're always hooking the output of something to the input of something else, as suggested in Figure 2.7. The signal source might be the output of an amplifier stage (with Thévenin equivalent series impedance Z_{out}), driving the next stage or perhaps a load (of some input impedance Z_{in}). In general, the loading effect of the following stage causes a reduction of signal, as we discussed earlier in Section 1.05. For this reason it is usually best to keep $Z_{out} \ll Z_{in}$ (a factor of 10 is a comfortable rule of thumb).

In some situations it is OK to forgo this general goal of making the source stiff compared with the load. In particular, if the load is always connected (e.g., within a circuit) and if it presents a known and constant Z_{in}, it is not too serious if it "loads" the source. However, it is always nicer if signal levels don't change when a load is connected. Also, if Z_{in} varies with signal level, then having a stiff source ($Z_{out} \ll Z_{in}$) assures linearity, where otherwise the level-dependent voltage divider would cause distortion.

Finally, there are two situations where $Z_{out} \ll Z_{in}$ is actually the wrong thing to

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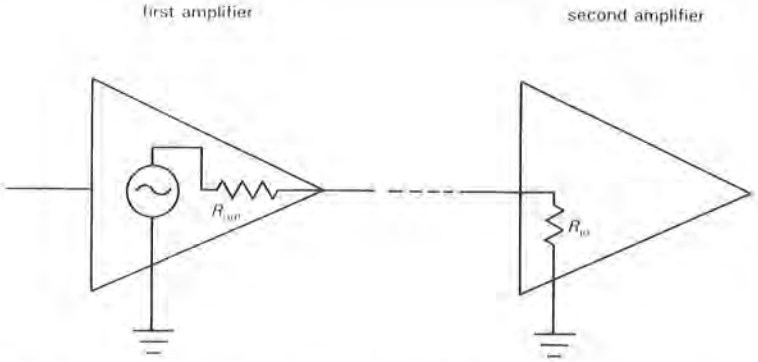


Figure 2.7. Illustrating circuit "loading" as a voltage divider.

do: In radiofrequency circuits we usually *match* impedances ($Z_{\text{out}} = Z_{\text{in}}$), for reasons we'll describe in Chapter 14. A second exception applies if the signal being coupled is a *current* rather than a voltage. In that case the situation is reversed, and one strives to make $Z_{\text{in}} \ll Z_{\text{out}}$ ($Z_{\text{out}} = \infty$, for a current source).

Input and output impedances of emitter followers

As you have just seen, the emitter follower is useful for changing impedances of signals or loads. To put it bluntly, that's the whole point of an emitter follower.

Let's calculate the input and output impedances of the emitter follower. In the preceding circuit we will consider R to be the load (in practice it sometimes is the load; otherwise the load is in parallel with R, but with R dominating the parallel resistance anyway). Make a voltage change ΔV_B at the base; the corresponding change at the emitter is $\Delta V_E = \Delta V_B$. Then the change in emitter current is

$$\Delta I_E = \Delta V_B / R$$

so

$$\Delta I_B = \frac{1}{h_{fe}+1}\Delta I_E = \frac{\Delta V_B}{R(h_{fe}+1)}$$

(using $I_E = I_C + I_B$). The input resistance is $\Delta V_B / \Delta I_B$. Therefore

$$r_{\text{in}} = (h_{fe}+1)R$$

The transistor beta (h_{fe}) is typically about 100, so a low-impedance load looks like a much higher impedance at the base; it is easier to drive.

In the preceding calculation, as in Chapter 1, we have used lower-case symbols such as h_{fe} to signify small-signal (incremental) quantities. Frequently one concentrates on the *changes* in voltages (or currents) in a circuit, rather than the steady (dc) values of those voltages (or currents). This is most common when these "small-signal" variations represent a possible signal, as in an audio amplifier, riding on a steady dc "bias" (see Section 2.05). The distinction between dc current gain (h_{FE}) and small-signal current gain (h_{fe}) isn't always made clear, and the term beta is used for both. That's alright, since $h_{fe} \approx h_{FE}$ (except at very high frequencies), and you never assume you know them accurately, anyway.

Although we used resistances in the preceding derivation, we could generalize to complex impedances by allowing ΔV_B, ΔI_B, etc., to become complex numbers. We would find that the same

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transformation rule applies for impedances: $Z_{in} = (h_{fe} + 1)Z_{load}$.

We could do a similar calculation to find that the output impedance Z_{out} of an emitter follower (the impedance looking into the emitter) driven from a source of internal impedance Z_{source} is given by

$$Z_{out} = \frac{Z_{source}}{h_{fe} + 1}$$

Strictly speaking, the output impedance of the circuit should also include the parallel resistance of R, but in practice Z_{out} (the impedance looking into the emitter) dominates.

EXERCISE 2.1

Show that the preceding relationship is correct. Hint: Hold the source voltage fixed, and find the change in output current for a given change in output voltage. Remember that the source voltage is connected to the base through a series resistor.

Because of these nice properties, emitter followers find application in many situations, e.g., making low-impedance signal sources within a circuit (or at outputs), making stiff voltage references from higher-impedance references (formed from voltage dividers, say), and generally isolating signal sources from the loading effects of subsequent stages.

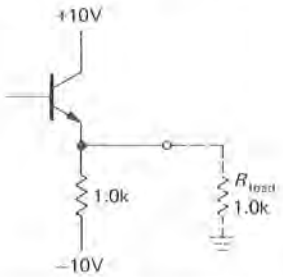


Figure 2.8. An *npn* emitter follower can source plenty of current through the transistor, but can sink limited current only through its emitter resistor.

EXERCISE 2.2

Use a follower with base driven from a voltage divider to provide a stiff source of +5 volts from an available regulated +15 volt supply. Load current (max) = 25mA. Choose your resistor values so that the output voltage doesn't drop more than 5% under full load.

Important points about followers

1. Notice (Section 2.01, rule 4) that in an emitter follower the *npn* transistor can only "source" current. For instance, in the loaded circuit shown in Figure 2.8 the output can swing to within a transistor saturation voltage drop of V_{CC} (about +9.9V), but it cannot go more negative than −5 volts. That is because on the extreme negative swing, the transistor can do no more than turn off, which it does at −4.4 volts input (−5V output). Further negative swing at the input results in backbiasing of the base-emitter junction, but no further change in output. The output, for a 10 volt amplitude sine-wave input, looks as shown in Figure 2.9.

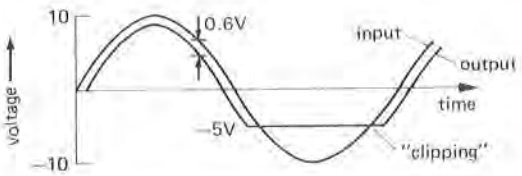


Figure 2.9. Illustrating the asymmetrical current drive capability of the *npn* emitter follower.

Another way to view the problem is to say that the emitter follower has low small-signal output impedance. Its large-signal output impedance is much larger (as large as R_E). The output impedance changes over from its small-signal value to its large-signal value at the point where the transistor goes out of the active region (in this case at an output voltage of -5V). To put this point another way, a low value of small-signal output impedance doesn't

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necessarily mean that the circuit can generate large signal swings into a low-resistance load. Low small-signal output impedance doesn't imply large output current capability.

Possible solutions to this problem involve either decreasing the value of the emitter resistor (with greater power dissipation in resistor and transistor), using a *pnp* transistor (if all signals are negative only), or using a "push-pull" configuration, in which two complementary transistors (one *npn*, one *pnp*), are used (Section 2.15). This sort of problem can also come up when the load of an emitter follower contains voltage or current sources of its own. This happens most often with regulated power supplies (the output is usually an emitter follower) driving a circuit that has other power supplies.

2. Always remember that the base-emitter reverse breakdown voltage for silicon transistors is small, quite often as little as 6 volts. Input swings large enough to take the transistor out of conduction can easily result in breakdown (with consequent degradation of h_{FE}) unless a protective diode is added (Fig. 2.10).

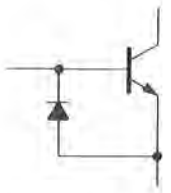


Figure 2.10. A diode prevents base-emitter reverse voltage breakdown.

3. The voltage gain of an emitter follower is actually slightly less than 1.0, because the base-emitter voltage drop is not really constant, but depends slightly on collector current. You will see how to handle that later in the chapter, when we have the Ebers-Moll equation.

2.04 Emitter followers as voltage regulators

The simplest regulated supply of voltage is simply a zener (Fig. 2.11). Some current must flow through the zener, so you choose

$$\frac{V_{\text{in}} - V_{\text{out}}}{R} > I_{\text{out}}\ (\text{max})$$

Because V_{in} isn't regulated, you use the lowest value of V_{in} that might occur for this formula. This is called worst-case design. In practice, you would also worry about component tolerances, line-voltage limits, etc., designing to accommodate the worst possible combination that would ever occur.

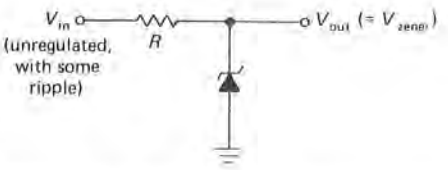


Figure 2.11. Simple zener voltage regulator.

The zener must be able to dissipate

$$P_{\text{zener}} = \left(\frac{V_{\text{in}} - V_{\text{out}}}{R} - I_{\text{out}}\right) V_{\text{zener}}$$

Again, for worst-case design, you would use V_{in} (max), R_{min}, and I_{out} (min).

EXERCISE 2.3

Design a +10 volt regulated supply for load currents from 0 to 100mA; the input voltage is +20 to +25 volts. Allow at least 10mA zener current under all (worst-case) conditions. What power rating must the zener have?

This simple zener-regulated supply is sometimes used for noncritical circuits, or circuits using little supply current. However, it has limited usefulness, for several reasons:

1. V_{out} isn't adjustable, or settable to a precise value.

2. Zener diodes give only moderate ripple rejection and regulation against changes of

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input or load, owing to their finite dynamic impedance.

3. For widely varying load currents a high-power zener is often necessary to handle the dissipation at low load current.

By using an emitter follower to isolate the zener, you get the improved circuit shown in Figure 2.12. Now the situation is much better. Zener current can be made relatively independent of load current, since the transistor base current is small, and far lower zener power dissipation is possible (reduced by as much as $1/h_{FE}$). The collector resistor R_C can be added to protect the transistor from momentary output short circuits by limiting the current, even though it is not essential to the emitter follower function. Choose R_C so that the voltage drop across it is less than the drop across R for the highest normal load current.

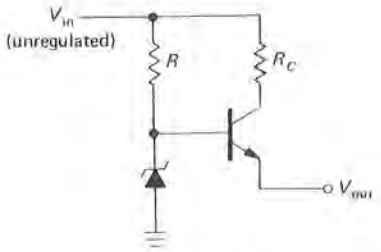


Figure 2.12. Zener regulator with follower, for increased output current. R_C protects the transistor by limiting maximum output current.

EXERCISE 2.4

Design a +10 volt supply with the same specifications as in Exercise 2.3. Use a zener and emitter follower. Calculate worst-case dissipation in transistor and zener. What is the percentage change in zener current from the no-load condition to full load? Compare with your previous circuit.

A nice variation of this circuit aims to eliminate the effect of ripple current (through R) on the zener voltage by supplying the zener current from a current source, which is the subject of Section 2.06. An alternative method uses a low-pass filter in the zener bias circuit (Fig. 2.13). R is chosen to provide sufficient zener current. Then C is chosen large enough so that $RC \gg 1/f_{\text{ripple}}$. (In a variation of this circuit, the upper resistor is replaced by a diode.)

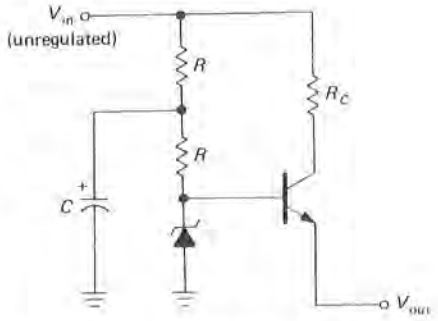


Figure 2.13. Reducing ripple in the zener regulator.

Later you will see better voltage regulators, ones in which you can vary the output easily and continuously, using feedback. They are also better voltage sources, with output impedances measured in milliohms, temperature coefficients of a few parts per million per degree centigrade, etc.

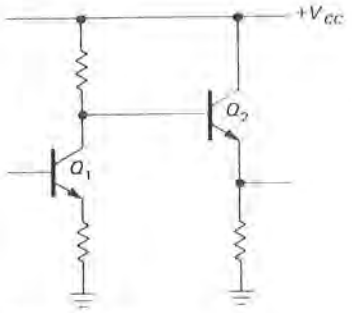


Figure 2.14

2.05 Emitter follower biasing

When an emitter follower is driven from a preceding stage in a circuit, it is usually OK to connect its base directly to the

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previous stage's output, as shown in Figure 2.14.

Because the signal on Q_1's collector is always within the range of the power supplies, Q_2's base will be between V_{CC} and ground, and therefore Q_2 is in the active region (neither cut off nor saturated), with its base-emitter diode in conduction and its collector at least a few tenths of a volt more positive than its emitter. Sometimes, though, the input to a follower may not be so conveniently situated with respect to the supply voltages. A typical example is a capacitively coupled (or ac-coupled) signal from some external source (e.g., an audio signal input to a high-fidelity amplifier). In that case the signal's average voltage is zero, and direct coupling to an emitter follower will give an output like that in Figure 2.15.

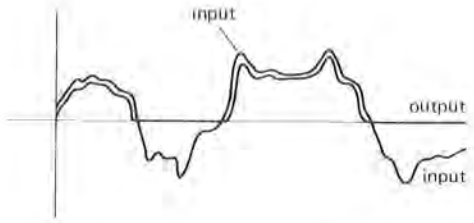


Figure 2.15. A transistor amplifier powered from a single positive supply cannot generate negative voltage swings at the transistor output terminal.

It is necessary to *bias* the follower (in fact, any transistor amplifier) so that collector current flows during the entire signal swing. In this case a voltage divider is the simplest way (Fig. 2.16). R_1 and R_2 are chosen to put the base halfway between ground and V_{CC} with no input signal, i.e., R_1 and R_2 are approximately equal. The process of selecting the operating voltages in a circuit, in the absence of applied signals, is known as setting the *quiescent point*. In this case, as in most cases, the quiescent point is chosen to allow maximum symmetrical signal swing of the output waveform without *clipping* (flattening of the top or bottom of the waveform). What values should R_1 and R_2 have? Applying our general principle (Section 1.05), we make the impedance of the dc bias source (the impedance looking into the voltage divider) small compared with the load it drives (the dc impedance looking into the base of the follower). In this case,

$$R_1 \| R_2 \ll h_{FE} R_E$$

This is approximately equivalent to saying that the current flowing in the voltage divider should be large compared with the current drawn by the base.

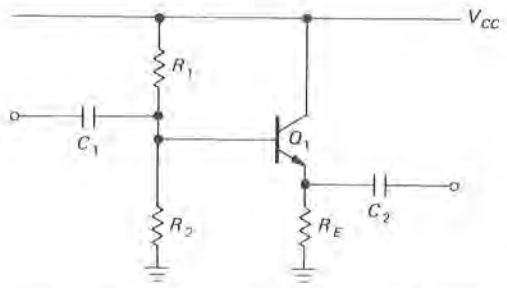


Figure 2.16. An ac-coupled emitter follower. Note base bias voltage divider.

Emitter follower design example

As an actual design example, let's make an emitter follower for audio signals (20Hz to 20kHz). V_{CC} is +15 volts, and quiescent current is to be 1mA.

Step 1. Choose V_E. For the largest possible symmetrical swing without clipping, $V_E = 0.5V_{CC}$, or +7.5 volts.

Step 2. Choose R_E. For a quiescent current of 1mA, $R_E = 7.5$k.

Step 3. Choose R_1 and R_2. V_B is V_E+ 0.6, or 8.1 volts. This determines the ratio of R_1 to R_2 as 1:1.17. The preceding loading criterion requires that the parallel resistance of R_1 and R_2 be about 75k or less (one-tenth of 7.5k times h_{FE}).

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Suitable standard values are $R_1 = 130\text{k}$, $R_2 = 150\text{k}$.

Step 4. Choose C_1. C_1 forms a high-pass filter with the impedance it sees as a load, namely the impedance looking into the base in parallel with the impedance looking into the base voltage divider. If we assume that the load this circuit will drive is large compared with the emitter resistor, then the impedance looking into the base is $h_{FE}R_E$, about 750k. The divider looks like 70k. So the capacitor sees a load of about 63k, and it should have a value of at least $0.15\mu\text{F}$ so that the 3dB point will be below the lowest frequency of interest, 20Hz.

Step 5. Choose C_2. C_2 forms a high-pass filter in combination with the load impedance, which is unknown. However, it is safe to assume that the load impedance won't be smaller than R_E, which gives a value for C_2 of at least $1.0\mu\text{F}$ to put the 3dB point below 20Hz. Because there are now two cascaded high-pass filter sections, the capacitor values should be increased somewhat to prevent large attenuation (reduction of signal amplitude, in this case 6dB) at the lowest frequency of interest. $C_1 = 0.5\mu\text{F}$ and $C_2 = 3.3\mu\text{F}$ might be good choices.

Followers with split supplies

Because signals often are "near ground," it is convenient to use symmetrical positive and negative supplies. This simplifies biasing and eliminates coupling capacitors (Fig. 2.17).

Warning: You must always provide a dc path for base bias current, even if it goes only to ground. In the preceding circuit it is assumed that the signal source has a dc path to ground. If not (e.g., if the signal is capacitively coupled), you must provide a resistor to ground (Fig. 2.18). R_B could be about one-tenth of $h_{FE}R_E$, as before.

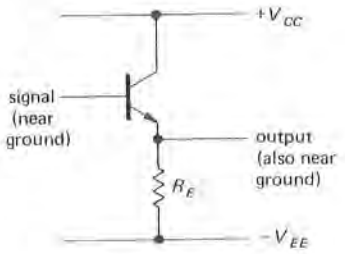


Figure 2.17. A dc-coupled emitter follower with split supply.

EXERCISE 2.5

Design an emitter follower with ±15 volt supplies to operate over the audio range (20Hz–20kHz). Use 5mA quiescent current and capacitive input coupling.

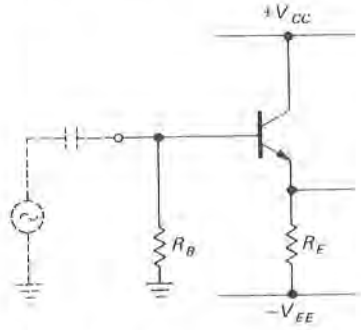


Figure 2.18

Bad biasing

Unfortunately, you sometimes see circuits like the disaster shown in Figure 2.19. R_B was chosen by assuming a particular value for h_{FE} (100), estimating the base current, and then hoping for a 7 volt drop across R_B. This is a bad design; h_{FE} is not a good parameter and will vary considerably. By using voltage biasing with a stiff voltage divider, as in the detailed example presented earlier, the quiescent point is insensitive to variations in transistor beta. For instance, in the previous design example the emitter voltage will increase by only 0.35 volt (5%) for a transistor with $h_{FE} = 200$ instead of the nominal

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$h_{FE} = 100$. As with this emitter follower example, it is just as easy to fall into this trap and design bad transistor circuits in the other transistor configurations (e.g., the common-emitter amplifier, which we will treat later in this chapter).

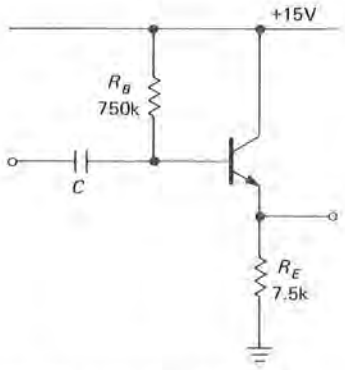


Figure 2.19. Don't do this!

2.06 Transistor current source

Current sources, although often neglected, are as important and as useful as voltage sources. They often provide an excellent way to bias transistors, and they are unequaled as "active loads" for super-gain amplifier stages and as emitter sources for differential amplifiers. Integrators, sawtooth generators, and ramp generators need current sources. They provide wide-voltage-range pull-ups within amplifier and regulator circuits. And, finally, there are applications in the outside world that require constant current sources, e.g., electrophoresis or electrochemistry.

Resistor plus voltage source

The simplest approximation to a current source is shown in Figure 2.20. As long as $R_{\text{load}} \ll R$ (in other words, $V_{\text{load}} \ll V$), the current is nearly constant and is approximately

$$I = V/R$$

The load doesn't have to be resistive. A capacitor will charge at a constant rate, as long as $V_{\text{capacitor}} \ll V$; this is just the first part of the exponential charging curve of an RC.

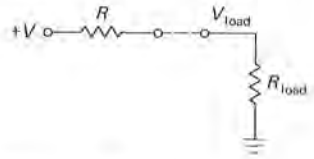


Figure 2.20

There are several drawbacks to a simple resistor current source. In order to make a good approximation to a current source, you must use large voltages, with lots of power dissipation in the resistor. In addition, the current isn't easily *programmable*, i.e., controllable over a large range via a voltage somewhere else in the circuit.

EXERCISE 2.6

If you want a current source constant to 1% over a load voltage range of 0 to +10 volts, how large a voltage source must you use in series with a single resistor?

EXERCISE 2.7

Suppose you want a 10mA current in the preceding problem. How much power is dissipated in the series resistor? How much gets to the load?

Transistor current source

Fortunately, it is possible to make a very good current source with a transistor (Fig. 2.21). It works like this : Applying V_B to the base, with $V_B > 0.6$ volt, ensures that the emitter is always conducting:

$$V_E = V_B - 0.6 \text{ volt}$$

So

$$I_E = V_E/R_E = (V_B - 0.6 \text{ volt})/R_E$$

But, since $I_E \approx I_C$ for large h_{FE},

$$I_C \approx (V_B - 0.6 \text{ volt})/R_E$$

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independent of V_C, as long as the transistor is not saturated ($V_C > V_E + 0.2$ volt).

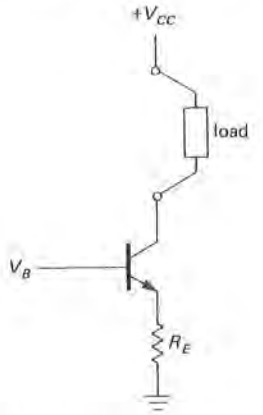


Figure 2.21. Transistor current source: basic concept.

Current-source biasing

The base voltage can be provided in a number of ways. A voltage divider is OK, as long as it is stiff enough. As before, the criterion is that its impedance should be much less than the dc impedance looking into the base ($h_{FE}R_E$). Or you can use a zener diode, biased from V_{CC}, or even a few forward-biased diodes in series from base to the corresponding emitter supply. Figure 2.22 shows some examples. In the last example (Fig. 2.22C), a *pnp* transistor *sources* current to a load returned to ground. The other examples (using *npn* transistors) should properly be called current *sinks*, but the usual practice is to call all of them current sources. ["Sink" and "source" simply refer to the direction of current flow: If a circuit *supplies* (positive) current to a point, it is a *source*, and vice versa.] In the first circuit, the voltage-divider impedance of ~1.3k is very stiff compared with the impedance looking into the base of about 100k (for $h_{FE} = 100$), so any changes in beta with collector voltage will not much affect the output current by causing the base voltage to change. In the other two circuits the biasing resistors are chosen to provide several milliamps to bring the diodes into conduction.

Compliance

A current source can provide constant current to the load only over some finite range of load voltage. To do otherwise would be equivalent to providing infinite power. The output voltage range over which a current source behaves well is called its output *compliance*. For the preceding transistor current sources, the compliance is set by the requirement that

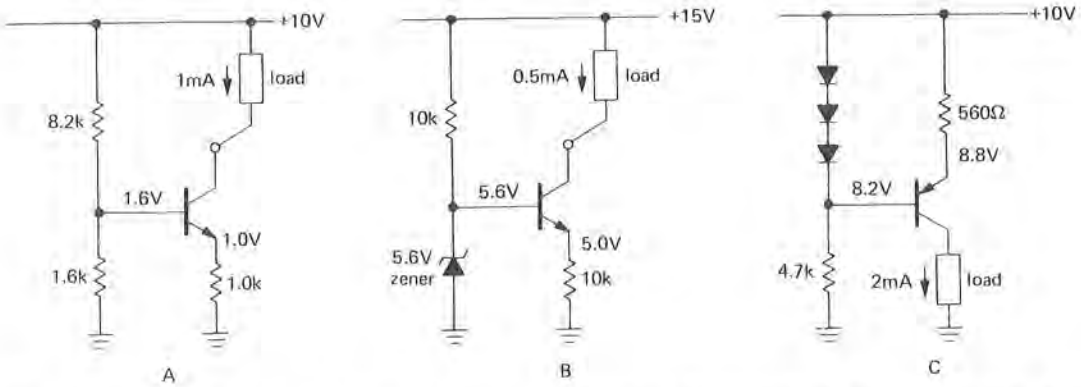


Figure 2.22. Transistor–current–source circuits, illustrating three methods of base biasing; *npn* transistors *sink* current, whereas *pnp* transistors *source* current. The circuit in C illustrates a load returned to ground.

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the transistors stay in the active region. Thus in the first circuit the voltage at the collector can go down until the transistor is almost in saturation, perhaps +1.2 volts at the collector. The second circuit, with its higher emitter voltage, can sink current down to a collector voltage of about +5.2 volts.

In all cases the collector voltage can range from a value near saturation all the way up to the supply voltage. For example, the last circuit can source current to the load for any voltage between zero and about +8.6 volts across the load. In fact, the load might even contain batteries or power supplies of its own, carrying the collector beyond the supply voltage. That's OK, but you must watch out for transistor breakdown (V_{CE} must not exceed BV_{CEO}, the specified collector-emitter breakdown voltage) and also for excessive power dissipation (set by $I_C V_{CE}$). As you will see in Section 6.07, there is an additional safe-operating-area constraint on power transistors.

EXERCISE 2.8

You have +5 and +15 volt regulated supplies available in a circuit. Design a 5mA *npn* current source (sink) using the +5 volts on the base. What is the output compliance?

A current source doesn't have to have a fixed voltage at the base. By varying V_B you get a voltage-programmable current source. The input signal swing v_{in} (remember, lower-case symbols mean *variations*) must stay small enough so that the emitter voltage never drops to zero, if the output current is to reflect input voltage variations smoothly. The result will be a current source with variations in output current proportional to the variations in input voltage, $i_{\text{out}} = v_{\text{in}}/R_E$.

□ *Deficiencies of current sources*

To what extent does this kind of current source depart from the ideal? In other words, does the load current vary with voltage, i.e., have a finite ($R_{Th} < \infty$) Thévenin equivalent resistance, and if so why? There are two kinds of effects:

1. Both V_{BE} (Early effect) and h_{FE} vary slightly with collector-to-emitter voltage at a given collector current. The changes in V_{BE} produced by voltage swings across the load cause the output current to change, because the emitter voltage (and therefore the emitter current) changes, even with a fixed applied base voltage. Changes in h_{FE} produce small changes in output (collector) current for fixed emitter current, since $I_C = I_E - I_B$; in addition, there are small changes in applied base voltage produced by the variable loading of the nonzero bias source impedance as h_{FE} (and therefore the base current) changes. These effects are small. For instance, the current from the circuit in Figure 2.22A varied about 0.5% in actual measurements with a 2N3565 transistor. In particular, for load voltages varying from zero to 8 volts, the Early effect contributed 0.5%, and transistor heating effects contributed 0.2%. In addition, variations in h_{FE} contributed 0.05% (note the stiff divider). Thus these variations result in a less-than-perfect current source: The output current depends slightly on voltage and therefore has less than infinite impedance. Later you will see methods that get around this difficulty.

2. V_{BE} and also h_{FE} depend on temperature. This causes drifts in output current with changes in ambient temperature; in addition, the transistor junction temperature varies as the load voltage is changed (because of variation in transistor dissipation), resulting in departure from ideal current source behavior. The change of V_{BE} with ambient temperature can be compensated with a circuit like that shown in Figure 2.23, in which Q_2's base-emitter drop is compensated by the drop in emitter follower Q_1, with similar temperature dependence. R_3, incidentally, is a

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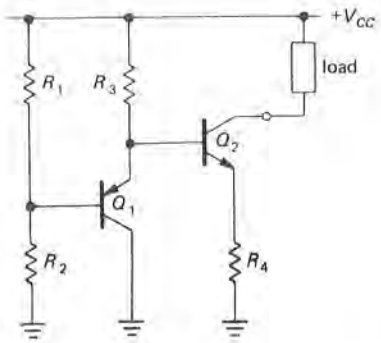


Figure 2.23. One method of temperature-compensating a current source.

pull-up resistor for Q_1, since Q_2's base sinks current, which Q_1 cannot source.

□ *Improving current-source performance*

In general, the effects of variability in V_{BE}, whether caused by temperature dependence (approximately $-2\text{mV}/^\circ\text{C}$) or by dependence on V_{CE} (the Early effect, given roughly by $\Delta V_{BE} \approx -0.0001\,\Delta V_{CE}$), can be minimized by choosing the emitter voltage to be large enough (at least 1V, say) so that changes in V_{BE} of tens of millivolts will not result in large fractional changes in the voltage across the emitter resistor (remember that the *base* voltage is what is held constant by your circuit). For instance, choosing $V_E = 0.1$ volt (i.e., applying about 0.7V to the base) would cause 10% variations in output current for 10mV changes in V_{BE}, whereas the choice $V_E = 1.0$ volt would result in 1% current variations for the same V_{BE} changes. Don't get carried away, though. Remember that the lower limit of output compliance is set by the emitter voltage. Using a 5 volt emitter voltage for a current source running from a +10 volt supply limits the output compliance to slightly less than 5 volts (the collector can go from about V_E+ 0.2V to V_{CC}, i.e., from 5.2V to 10V).

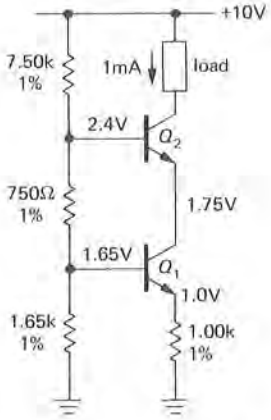


Figure 2.24. Cascode current source for improved current stability with load voltage variations.

Figure 2.24 shows a circuit modification that improves current-source performance significantly. Current source Q_1 functions as before, but with collector voltage held fixed by Q_2's emitter. The load sees the same current as before, since Q_2's collector and emitter currents are nearly equal (large h_{FE}). But with this circuit the V_{CE} of Q_1 doesn't change with load voltage, thus eliminating the small changes in V_{BE} from Early effect and dissipation-induced temperature changes. Measurements with 2N3565s gave 0.1% current variation for load voltages from 0 to 8 volts; to obtain performance of this accuracy it is important to use stable 1% resistors, as shown. (Incidentally, this circuit connection also finds use in high-frequency amplifiers, where it is known as the "cascode.") Later you will see current source techniques using op-amps and feedback that circumvent the problem of V_{BE} variation altogether.

The effects of variability of h_{FE} can be minimized by choosing transistors with large h_{FE}, so that the base current contribution to the emitter current is relatively small.

Figure 2.25 shows one last current source, whose output current doesn't

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depend on supply voltage. In this circuit, Q_1's V_{BE} across R_2 sets the output current, independent of V_{CC}:

$$I_{\text{out}} = V_{BE}/R_2$$

R_1 biases Q_2 and holds Q_1's collector at two diode drops below V_{CC}, eliminating Early effect as in the previous circuit. This circuit is not temperature-compensated; the voltage across R_2 decreases approximately 2.1mV/°C, causing the output current to decrease approximately 0.3%/°C.

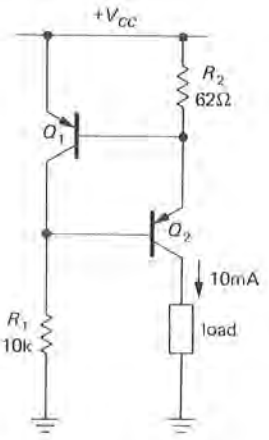


Figure 2.25. Transistor V_{BE}-referenced current source.

2.07 Common-emitter amplifier

Consider a current source with a resistor as load (Fig. 2.26). The collector voltage is

$$V_C = V_{CC} - I_C R_C$$

We could capacitively couple a signal to the base to cause the collector voltage to vary. Consider the example in Figure 2.27. C is chosen so that all frequencies of interest are passed by the high-pass filter it forms in combination with the parallel resistance of the base biasing resistors (the

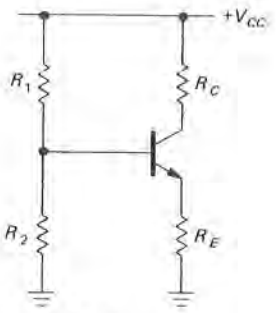


Figure 2.26

impedance looking into the base itself will usually be much larger because of the way the base resistors are chosen, and it can be ignored); that is,

$$C \geq \frac{1}{2\pi f(R_1 \| R_2)}$$

The quiescent collector current is 1.0mA because of the applied base bias and the 1.0k emitter resistor. That current puts the collector at +10 volts (+20V, minus 1.0mA through 10k). Now imagine an applied wiggle in base voltage v_B. The emitter follows with $v_E = v_B$, which causes a wiggle in emitter current

$$i_E = v_E/R_E = v_B/R_E$$

and nearly the same change in collector current (h_{fe} is large). So the initial wiggle in base voltage finally causes a collector voltage wiggle

$$v_C = -i_C R_C = -v_B(R_C/R_E)$$

Aha! It's a *voltage amplifier*, with a voltage amplification (or "gain") given by

$$\text{gain} = v_{\text{out}}/v_{\text{in}} = -R_C/R_E$$

In this case the gain is −10,000/1000, or −10. The minus sign means that a positive wiggle at the input gets turned into a negative wiggle (10 times as large) at the output. This is called a *common-emitter amplifier* with emitter degeneration.

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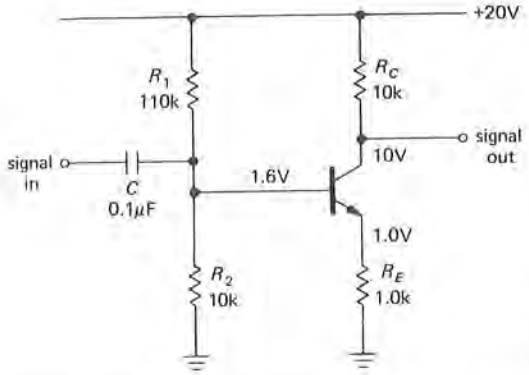


Figure 2.27. An ac common-emitter amplifier with emitter degeneration. Note that the output terminal is the collector, rather than the emitter.

Input and output impedance of the common-emitter amplifier

We can easily determine the input and output impedances of the amplifier. The input signal sees, in parallel, 110k, 10k, and the impedance looking into the base. The latter is about 100k (h_{fe} times R_E), so the input impedance (dominated by the 10k) is about 8k. The input coupling capacitor thus forms a high-pass filter, with the 3dB point at 200Hz. The signal driving the amplifier sees 0.1μF in series with 8k, which to signals of normal frequencies (well above the 3dB point) just looks like 8k.

The output impedance is 10k in parallel with the impedance looking into the collector. What is that? Well, remember that if you snip off the collector resistor, you're simply looking into a current source. The collector impedance is very large (measured in megohms), and so the output impedance is just the value of the collector resistor, 10k. It is worth remembering that the impedance looking into a transistor's collector is high, whereas the impedance looking into the emitter is low (as in the emitter follower). Although the output impedance of a common-emitter amplifier will be dominated by the collector load resistor, the output impedance of an emitter follower will not be dominated by the emitter load resistor, but rather by the impedance looking into the emitter.

2.08 Unity-gain phase splitter

Sometimes it is useful to generate a signal and its inverse, i.e., two signals 180° out of phase. That's easy to do – just use an emitter-degenerated amplifier with a gain of −1 (Fig. 2.28). The quiescent collector voltage is set to $0.75V_{CC}$, rather than the usual $0.5V_{CC}$, in order to achieve the same result – maximum symmetrical output swing without clipping at either output. The collector can swing from $0.5V_{CC}$ to V_{CC}, whereas the emitter can swing from ground to $0.5V_{CC}$.

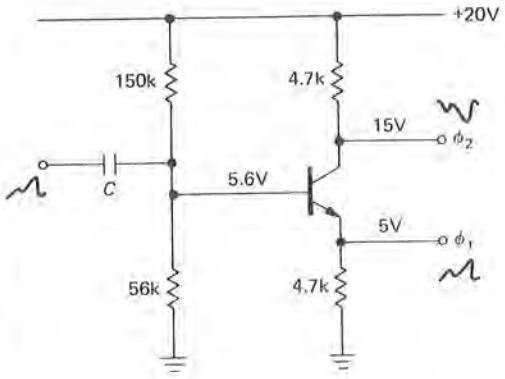


Figure 2.28. Unity-gain phase splitter.

Note that the phase-splitter outputs must be loaded with equal (or very high) impedances at the two outputs in order to maintain gain symmetry.

Phase shifter

A nice use of the phase splitter is shown in Figure 2.29. This circuit gives (for a sine wave input) an output sine wave of adjustable phase (from zero to 180°), but with constant amplitude. It can be best understood with a phasor diagram of voltages (see Chapter 1); representing the input signal by a unit vector along

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the real axis, the signals look as shown in Figure 2.30.

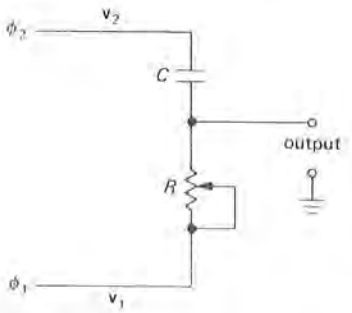


Figure 2.29. Constant-amplitude phase shifter.

Signal vectors v_R and v_C must be at right angles, and they must add to form a vector of constant length along the real axis. There is a theorem from geometry that says that the locus of such points is a circle. So the resultant vector (the output voltage) always has unit length, i.e., the same amplitude as the input, and its phase can vary from nearly zero to nearly 180° relative to the input wave as R is varied from nearly zero to a value much larger than Z_C at the operating frequency. However, note that the phase shift also depends on the frequency of the input signal for a given setting of the potentiometer R. It is worth noting that a simple RC high-pass (or low-pass) network could also be used as an adjustable phase shifter. However, its output amplitude would vary over an enormous range as the phase shift was adjusted.

An additional concern here is the ability of the phase-splitter circuit to drive the RC phase shifter as a load. Ideally, the load should present an impedance that is large compared with the collector and emitter resistors. As a result, this circuit is of limited utility where a wide range of phase shifts is required. You will see improved phase-splitter techniques in Chapter 4.

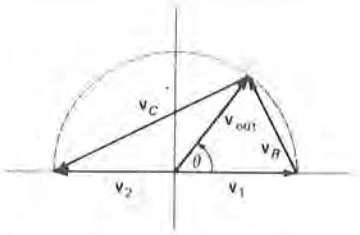


Figure 2.30. Phasor diagram for phase shifter.

2.09 Transconductance

In the preceding section we figured out the operation of the emitter-degenerated amplifier by (a) imagining an applied base voltage swing and seeing that the emitter voltage had the same swing, then (b) calculating the emitter current swing; then, ignoring the small base current contribution, we got the collector current swing and thus (c) the collector voltage swing. The voltage gain was then simply the ratio of collector (output) voltage swing to base (input) voltage swing.

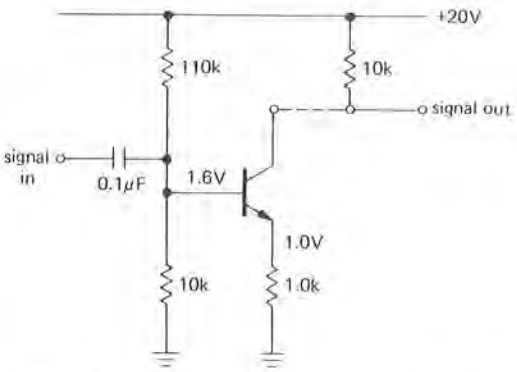


Figure 2.31. The common-emitter amplifier is a transconductance stage driving a (resistive) load.

There's another way to think about this kind of amplifier. Imagine breaking it apart, as in Figure 2.31. The first part is a voltage-controlled current source, with quiescent current of 1.0mA and gain

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of -1mA/V. Gain means the ratio output/input; in this case the gain has units of current/voltage, or 1/resistance. The inverse of resistance is called *conductance* (the inverse of reactance is *susceptance*, and the inverse of impedance is *admittance*) and has a special unit, the *siemens*, which used to be called the *mho* (ohm spelled backward). An amplifier whose gain has units of conductance is called a *transconductance* amplifier; the ratio $I_{\text{out}}/V_{\text{in}}$ is called the transconductance, g_m.

Think of the first part of the circuit as a transconductance amplifier, i.e., a voltage-to-current amplifier with transconductance g_m (gain) of 1mA/V (1000μS, or 1mS, which is just $1/R_E$). The second part of the circuit is the load resistor, an "amplifier" that converts current to voltage. This resistor could be called a *transresistance* amplifier, and its gain (r_m) has units of voltage/current, or resistance. In this case its quiescent voltage is V_{CC}, and its gain (transresistance) is 10kV/A (10kΩ), which is just R_C. Connecting the two parts together gives you a voltage amplifier. You get the overall gain by multiplying the two gains. In this case $G = g_m R_C = R_C/R_E$, or -10, a unitless number equal to the ratio (output voltage)/(input voltage).

This is a useful way to think about an amplifier, because you can analyze performance of the sections independently. For example, you can analyze the transconductance part of the amplifier by evaluating g_m for different circuit configurations or even different devices, such as field-effect transistors (FETs). Then you can analyze the transresistance (or load) part by considering gain versus voltage swing trade-offs. If you are interested in the overall voltage gain, it is given by $G_V = g_m r_m$, where r_m is the transresistance of the load. Ultimately the substitution of an active load (current source), with its extremely high transresistance, can yield one-stage voltage gains of 10,000 or more. The *cascode* configuration, which we will discuss later, is another example easily understood with this approach.

In Chapter 4, which deals with operational amplifiers, you will see further examples of amplifiers with voltages or currents as inputs or outputs; voltage amplifiers (voltage to voltage), current amplifiers (current to current), and transresistance amplifiers (current to voltage).

Turning up the gain: limitations of the simple model

The voltage gain of the emitter-degenerated amplifier is $-R_C/R_E$, according to our model. What happens as R_E is reduced toward zero? The equation predicts that the gain will rise without limit. But if we made actual measurements of the preceding circuit, keeping the quiescent current constant at 1mA, we would find that the gain would level off at about 400 when R_E is zero, i.e., with the emitter grounded. We would also find that the amplifier would become significantly nonlinear (the output would not be a faithful replica of the input), the input impedance would become small and nonlinear, and the biasing would become critical and unstable with temperature. Clearly our transistor model is incomplete and needs to be modified in order to handle this circuit situation, as well as others we will talk about shortly. Our fixed-up model, which we will call the transconductance model, will be accurate enough for the remainder of the book.

EBERS-MOLL MODEL APPLIED TO BASIC TRANSISTOR CIRCUITS

2.10 Improved transistor model: transconductance amplifier

The important change is in property 4 (Section 2.01), where we said earlier that $I_C = h_{FE} I_B$. We thought of the transistor

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as a current amplifier whose input circuit behaved like a diode. That's roughly correct, and for some applications it's good enough. But to understand differential amplifiers, logarithmic converters, temperature compensation, and other important applications, you must think of the transistor as a *transconductance* device – collector current is determined by base-to-emitter *voltage*.

Here's the modified property 4:

4. When rules 1–3 (Section 2.01) are obeyed, I_C is related to V_{BE} by

$$I_C = I_S\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right]$$

where $V_T = kT/q = 25.3\text{mV}$ at room temperature (68°F, 20°C), q is the electron charge (1.60×10^{-19} coulombs), k is Boltzmann's constant (1.38×10^{-23} joules/°K), T is the absolute temperature in degrees Kelvin (°K = °C + 273.16), and I_S is the saturation current of the particular transistor (depends on T). Then the base current, which also depends on V_{BE}, can be approximated by

$$I_B = I_C/h_{FE}$$

where the "constant" h_{FE} is typically in the range 20 to 1000, but depends on transistor type, I_C, V_{CE}, and temperature. I_S represents the reverse leakage current. In the active region $I_C \gg I_S$, and therefore the -1 term can be neglected in comparison with the exponential.

The equation for I_C is known as the Ebers-Moll equation. It also approximately describes the current versus voltage for a diode, if V_T is multiplied by a correction factor m between 1 and 2. For transistors it is important to realize that the collector current is accurately determined by the base-emitter voltage, rather than by the base current (the base current is then roughly determined by h_{FE}), and that this exponential law is accurate over an enormous range of currents, typically from nanoamps to milliamps. Figure 2.32 makes the point graphically. If you measure the base current at various collector currents, you will get a graph of h_{FE} versus I_C like that in Figure 2.33.

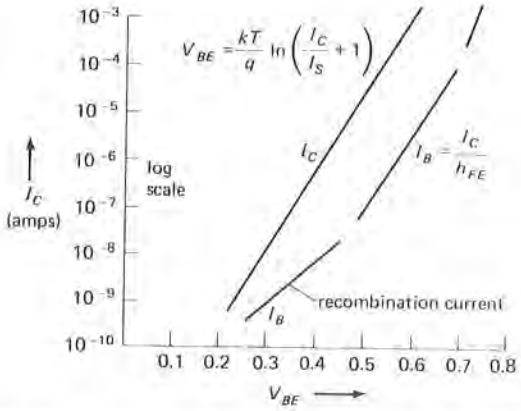


Figure 2.32. Transistor base and collector currents as functions of base-to-emitter voltage V_{BE}.

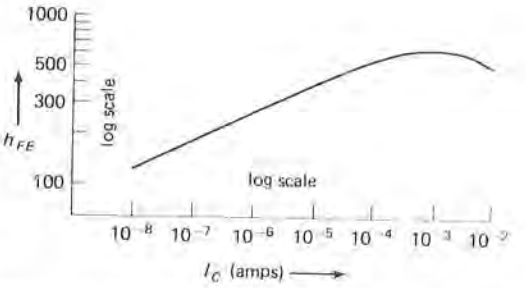


Figure 2.33. Typical transistor current gain (h_{FE}) versus collector current.

Although the Ebers-Moll equation tells us that the base-emitter voltage "programs" the collector current, this property may not be directly usable in practice (biasing a transistor by applying a base voltage) because of the large temperature coefficient of base-emitter voltage. You will see later how the Ebers-Moll equation provides insight and solutions to this problem.

Rules of thumb for transistor design

From the Ebers-Moll equation we can get

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several important quantities we will be using often in circuit design:

1. The steepness of the diode curve. How much do we need to increase V_{BE} to increase I_C by a factor of 10? From the Ebers-Moll equation, that's just $V_T \log_e 10$, or 60mV at room temperature. *Base voltage increases 60mV per decade of collector current.* Equivalently, $I_C = I_{C0}e^{\Delta V/25}$, where ΔV is in millivolts.

2. The small-signal impedance looking into the emitter, for the base held at a fixed voltage. Taking the derivative of V_{BE} with respect to I_C, you get

$$r_e = V_T/I_C = 25/I_C \text{ ohms}$$

where I_C is in milliamps. The numerical value $25/I_C$ is for room temperature. This *intrinsic* emitter resistance, r_e, acts as if it is in series with the emitter in all transistor circuits. It limits the gain of a grounded emitter amplifier, causes an emitter follower to have a voltage gain of slightly less than unity, and prevents the output impedance of an emitter follower from reaching zero. Note that the transconductance of a grounded emitter amplifier is $g_m = 1/r_e$.

3. The temperature dependence of V_{BE}. A glance at the Ebers-Moll equation suggests that V_{BE} has a positive temperature coefficient. However, because of the temperature dependence of I_S, V_{BE} *decreases* about 2.1mV/°C. It is roughly proportional to $1/T_{\text{abs}}$, where T_{abs} is the absolute temperature.

There is one additional quantity we will need on occasion, although it is not derivable from the Ebers-Moll equation. It is the Early effect we described in Section 2.06, and it sets important limits on current-source and amplifier performance, for example:

4. Early effect. V_{BE} varies slightly with changing V_{CE} at constant I_C. This effect is caused by changing effective base width, and it is given, approximately, by

$$\Delta V_{BE} = -\alpha \Delta V_{CE}$$

where $\alpha \approx 0.0001$.

These are the essential quantities we need. With them we will be able to handle most problems of transistor circuit design, and we will have little need to refer to the Ebers-Moll equation itself.

2.11 The emitter follower revisited

Before looking again at the common-emitter amplifier with the benefit of our new transistor model, let's take a quick look at the humble emitter follower. The Ebers-Moll model predicts that an emitter follower should have nonzero output impedance, even when driven by a voltage source, because of finite r_e (item 2, above). The same effect also produces a voltage gain slightly less than unity, because r_e forms a voltage divider with the load resistor.

These effects are easy to calculate. With fixed base voltage, the impedance looking back into the emitter is just $R_{\text{out}} = dV_{BE}/dI_E$; but $I_E \approx I_C$, so $R_{\text{out}} \approx r_e$, the intrinsic emitter resistance [$r_e = 25/I_C(\text{mA})$]. For example, in Figure 2.34A, the load sees a driving impedance of $r_e = 25$ ohms, since $I_C = 1$mA. (This is paralleled by the emitter resistor R_E, if used; but in practice R_E will always be much larger than r_e.) Figure 2.34B shows a more typical situation, with finite source resistance R_S (for simplicity we've omitted the obligatory biasing components – base divider and blocking capacitor – which are shown in Fig. 2.34C). In this case the emitter follower's output impedance is just r_e in series with $R_s/(h_{fe}+ 1)$ (again paralleled by an unimportant R_E, if present). For example, if $R_s = 1$k and $I_C = 1$mA, $R_{\text{out}} = 35$ ohms (assuming $h_{fe} = 100$). It is easy to show that the intrinsic emitter r_e also figures into an emitter follower's *input* impedance, just as if it were in series with the load (actually, parallel combination of load resistor and

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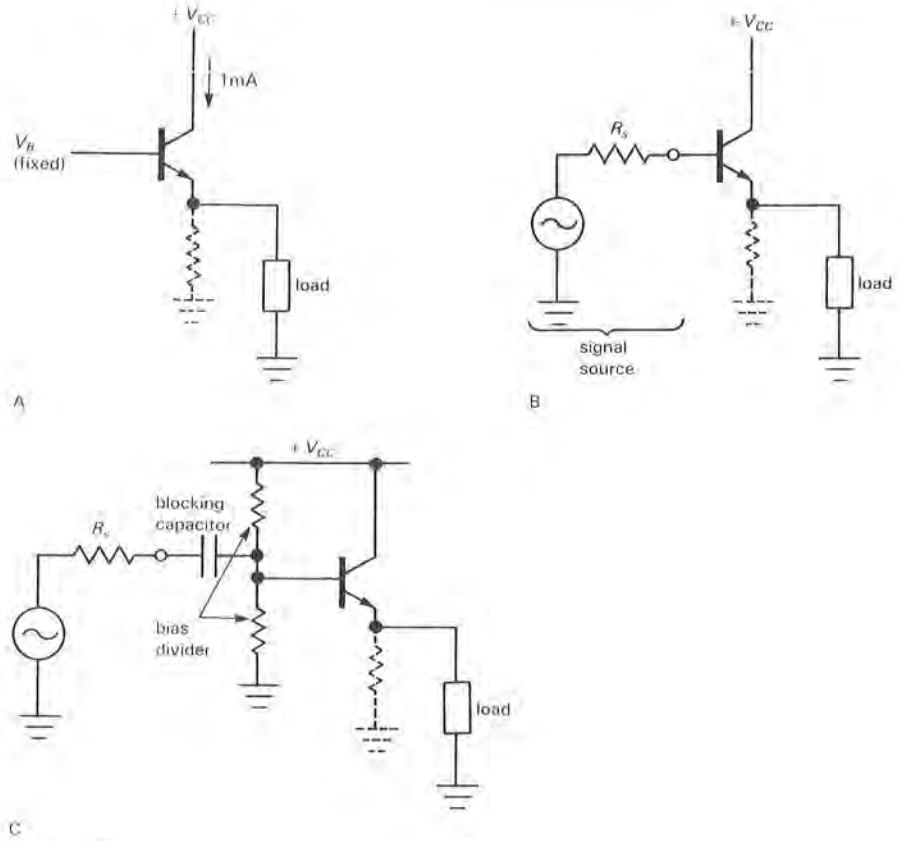


Figure 2.34

emitter resistor). In other words, for the emitter follower circuit the effect of the Ebers–Moll model is simply to add a series emitter resistance r_e to our earlier results.

The voltage gain of an emitter follower is slightly less than unity, owing to the voltage divider produced by r_e and the load. It is simple to calculate, because the output is at the junction of r_e and R_{load}: $G_V = v_{\text{out}}/v_{\text{in}} = R_L/(r_e + R_L)$. Thus, for example, a follower running at 1mA quiescent current, with 1k load, has a voltage gain of 0.976. Engineers sometimes like to write the gain in terms of the transconductance, to put it in a form that holds for FETs also (see Section 3.07); in that case (using $g_m = 1/r_e$) you get $G_V = R_L g_m/(1 + R_L g_m)$.

2.12 The common-emitter amplifier revisited

Previously we got wrong answers for the voltage gain of the common-emitter amplifier with emitter resistor (sometimes called emitter degeneration) when we set the emitter resistor equal to zero. The problem is that the transistor has $25/I_C(\text{mA})$ ohms of built-in (intrinsic) emitter resistance r_e that must be added to the actual external emitter resistor. This resistance is significant only when small emitter resistors (or none at all) are used. So, for instance, the amplifier we considered previously will have a voltage gain of $-10\text{k}/r_e$, or -400, when the external emitter resistor is zero. The input

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impedance is not zero, as we would have predicted earlier ($h_{fe}R_E$); it is approximately $h_{fe}r_e$, or in this case (1mA quiescent current) about 2.5k.

The terms "grounded emitter" and "common emitter" are sometimes used interchangeably, and they can be confusing. We will use the phrase "grounded emitter amplifier" to mean a common-emitter amplifier with $R_E = 0$. A common-emitter amplifier stage may have an emitter resistor; what matters is that the emitter circuit is common to the input circuit and the output circuit.

Shortcomings of the single-stage grounded emitter amplifier

The extra voltage gain you get by using $R_E = 0$ comes at the expense of other properties of the amplifier. In fact, the grounded emitter amplifier, in spite of its popularity in textbooks, should be avoided except in circuits with overall negative feedback. In order to see why, consider Figure 2.35.

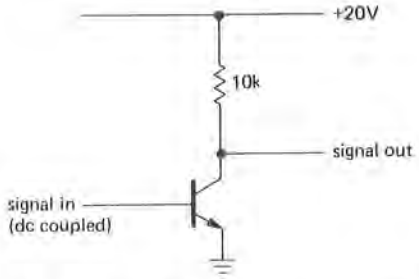


Figure 2.35. Common-emitter amplifier without emitter degeneration.

*1. **Nonlinearity.*** The gain is $G = -g_m R_C = -R_C/r_e = -R_C I_C(\text{mA})/25$, so for a quiescent current of 1mA, the gain is -400. But I_C varies as the output signal varies. For this example, the gain will vary from -800 ($V_{\text{out}} = 0$, $I_C = 2\text{mA}$) down to zero ($V_{\text{out}} = V_{CC}$, $I_C = 0$). For a triangle-wave input, the output will look like that in Figure 2.36. The amplifier has high distortion, or poor linearity. The grounded emitter amplifier without feedback is useful only for small signal swings about the quiescent point. By contrast, the emitter-degenerated amplifier has gain almost entirely independent of collector current, as long as $R_E \gg r_e$, and can be used for undistorted amplification even with large signal swings.

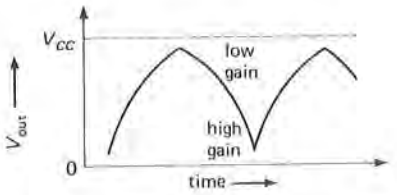


Figure 2.36. Nonlinear output waveform from grounded emitter amplifier.

*2. **Input impedance.*** The input impedance is roughly $Z_{\text{in}} = h_{fe}r_e = 25\ h_{fe}/I_C(\text{mA})$ ohms. Once again, I_C varies over the signal swing, giving a varying input impedance. Unless the signal source driving the base has low impedance, you will wind up with nonlinearity due to the nonlinear variable voltage divider formed from the signal source and the amplifier's input impedance. By contrast, the input impedance of an emitter-degenerated amplifier is constant and high.

*3. **Biasing.*** The grounded emitter amplifier is difficult to bias. It might be tempting just to apply a voltage (from a voltage divider) that gives the right quiescent current according to the Ebers-Moll equation. That won't work, because of the temperature dependence of V_{BE} (at fixed I_C), which varies about $2.1\text{mV}/^\circ\text{C}$ (it actually decreases with increasing T because of the variation of I_S with T; as a result, V_{BE} is roughly proportional to $1/T$, the absolute temperature). This means that the collector current (for fixed V_{BE}) will increase by a factor of 10 for a 30°C rise

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in temperature. Such unstable biasing is useless, because even rather small changes in temperature will cause the amplifier to saturate. For example, a grounded emitter stage biased with the collector at half the supply voltage will go into saturation if the temperature rises by 8°C.

EXERCISE 2.9

Verify that an 8°C rise in ambient temperature will cause a base-voltage-biased grounded emitter stage to saturate, assuming that it was initially biased for $V_C = 0.5V_{CC}$.

Some solutions to the biasing problem will be discussed in the following sections. By contrast, the emitter-degenerated amplifier achieves stable biasing by applying a voltage to the base, most of which appears across the emitter resistor, thus determining the quiescent current.

Emitter resistor as feedback

Adding an external series resistor to the intrinsic emitter resistance r_e (emitter degeneration) improves many properties of the common-emitter amplifier, at the expense of gain. You will see the same thing happening in Chapters 4 and 5 , when we discuss *negative feedback*, an important technique for improving amplifier characteristics by feeding back some of the output signal to reduce the effective input signal. The similarity here is no coincidence; the emitter-degenerated amplifier itself uses a form of negative feedback. Think of the transistor as a transconductance device, determining collector current (and therefore output voltage) according to the voltage applied between the base and emitter; but the input to the amplifier is the voltage from base to ground. So the voltage from base to emitter is the input voltage, *minus a sample of the output* ($I_E R_E$). That's negative feedback, and that's why emitter degeneration improves most properties of the amplifier (improved linearity and stability and increased input impedance; also the output impedance would be reduced if the feedback were taken directly from the collector). Great things to look forward to in Chapters 4 and 5!

2.13 Biasing the common-emitter amplifier

If you must have the highest possible gain (or if the amplifier stage is inside a feedback loop), it is possible to arrange successful biasing of a common-emitter amplifier. There are three solutions that can be applied, separately or in combination: bypassed emitter resistor, matched biasing transistor, and dc feedback.

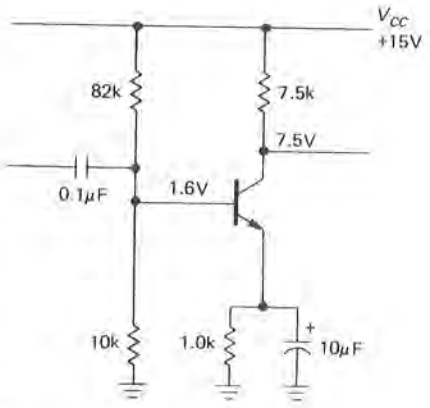


Figure 2.37. A bypassed emitter resistor can be used to improve the bias stability of a grounded emitter amplifier.

Bypassed emitter resistor

Use a bypassed emitter resistor, biasing as for the degenerated amplifier, as shown in Figure 2.37. In this case R_E has been chosen about $0.1R_C$, for ease of biasing; if R_E is too small, the emitter voltage will be much smaller than the base-emitter drop, leading to temperature instability of the quiescent point as V_{BE} varies with temperature. The emitter bypass capacitor is chosen by making its impedance small

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compared with r_e (not R_E) at the lowest frequency of interest. In this case its impedance is 25 ohms at 650Hz. At signal frequencies the input coupling capacitor sees an impedance of 10k in parallel with the base impedance, in this case h_{fe} times 25 ohms, or roughly 2.5k. At dc, the impedance looking into the base is much larger (h_{fe} times the emitter resistor, or about 100k), which is why stable biasing is possible.

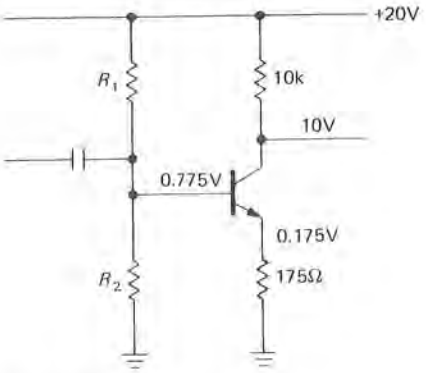


Figure 2.38

A variation on this circuit consists of using two emitter resistors in series, one of them bypassed. For instance, suppose you want an amplifier with a voltage gain of 50, quiescent current of 1mA, and V_{CC} of +20 volts, for signals from 20Hz to 20kHz. If you try to use the emitter-degenerated circuit, you will have the circuit shown in Figure 2.38. The collector resistor is chosen to put the quiescent collector voltage at $0.5V_{CC}$. Then the emitter resistor is chosen for the required gain, including the effects of the r_e of $25/I_C$(mA). The problem is that the emitter voltage of only 0.175 volt will vary significantly as the ~0.6 volt of base-emitter drop varies with temperature (−2.1mV/°C, approximately), since the base is held at constant voltage by R_1 and R_2; for instance, you can verify that an increase of 20°C will cause the collector current to increase by nearly 25%.

The solution here is to add some bypassed emitter resistance for stable biasing, with no change in gain at signal frequencies (Fig. 2.39). As before, the collector resistor is chosen to put the collector at 10 volts ($0.5V_{CC}$). Then the unbypassed emitter resistor is chosen to give a gain of 50, including the intrinsic emitter resistance $r_e = 25/I_C$(mA). Enough bypassed emitter resistance is added to make stable biasing possible (one-tenth of the collector resistance is a good rule). The base voltage is chosen to give 1mA of emitter current, with impedance about one-tenth the dc impedance looking into the base (in this case about 100k). The emitter bypass capacitor is chosen to have low impedance compared with 180+25 ohms at the lowest signal frequencies. Finally, the input coupling capacitor is chosen to have low impedance compared with the *signal-frequency* input impedance of the amplifier, which is equal to the voltage divider impedance in parallel with $(180 + 25)h_{fe}$ ohms (the 820Ω is bypassed, and looks like a short at signal frequencies).

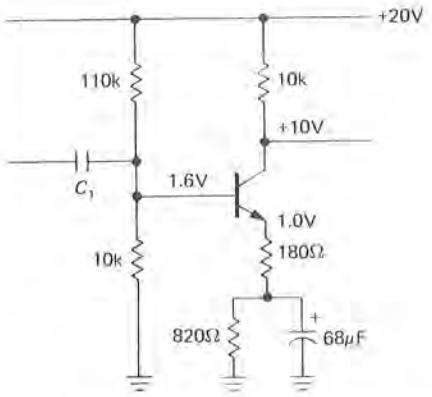


Figure 2.39. A common-emitter amplifier combining bias stability, linearity, and large voltage gain.

An alternative circuit splits the signal and dc paths (Fig. 2.40). This lets you vary the gain (by changing the 180Ω resistor) without bias change.

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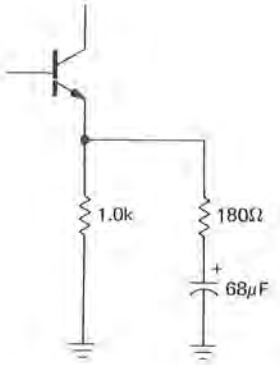
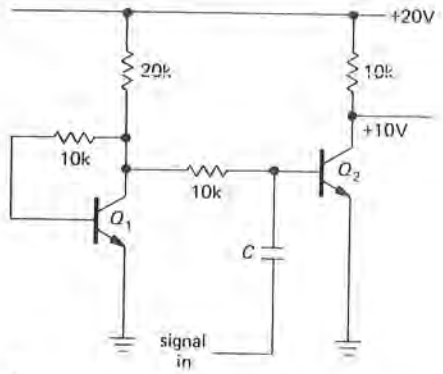
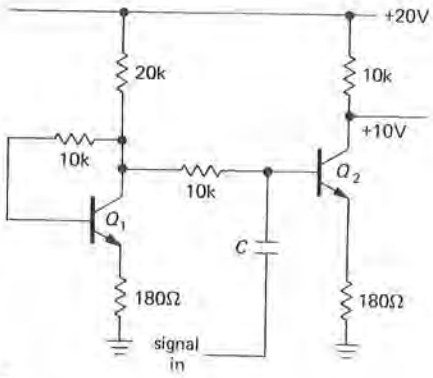


Figure 2.40. Equivalent emitter circuit for Figure 2.39.



A



B

Figure 2.41. Biasing scheme with compensated V_{BE} drop.

☐ *Matched biasing transistor*

Use a matched transistor to generate the correct base voltage for the required collector current; this ensures automatic temperature compensation (Fig. 2.41). Q_1's collector is drawing 1mA, since it is guaranteed to be near ground (about one V_{BE} drop above ground, to be exact); if Q_1 and Q_2 are a matched pair (available as a single device, with the two transistors on one piece of silicon), then Q_2 will also be biased to draw 1mA, putting its collector at +10 volts and allowing a full ±10 volt symmetrical swing on its collector. Changes in temperature are of no importance, as long as both transistors are at the same temperature. This is a good reason for using a "monolithic" dual transistor.

Feedback at dc

Use dc feedback to stabilize the quiescent point. Figure 2.42 shows one method. By taking the bias voltage from the collector, rather than from V_{CC}, you get some measure of bias stability. The base sits one diode drop above ground; since its bias comes from a 10:1 divider, the collector is at 11 diode drops above ground, or about 7 volts. Any tendency for the transistor

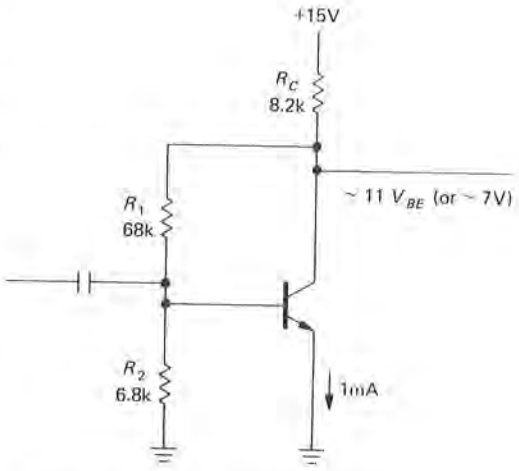


Figure 2.42. Bias stability is improved by feedback.

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to saturate (e.g., if it happens to have unusually high beta) is stabilized, since the dropping collector voltage will reduce the base bias. This scheme is acceptable if great stability is not required. The quiescent point is liable to drift a volt or so as the ambient (surrounding) temperature changes, since the base-emitter voltage has a significant temperature coefficient. Better stability is possible if several stages of amplification are included within the feedback loop. You will see examples later in connection with feedback.

A better understanding of feedback is really necessary to understand this circuit. For instance, feedback acts to reduce the input and output impedances. The input signal sees R_1's resistance effectively reduced by the voltage gain of the stage. In this case it is equivalent to a resistor of about 300 ohms to ground. In Chapter 4 we will treat feedback in enough detail so that you will be able to figure the voltage gain and terminal impedance of this circuit.

Note that the base bias resistor values could be increased in order to raise the input impedance, but you should then take into account the non-negligible base current. Suitable values might be $R_1 =$ 220k and $R_2 =$ 33k. An alternative approach might be to bypass the feedback resistance in order to eliminate feedback (and therefore lowered input impedance) at signal frequencies (Fig. 2.43).

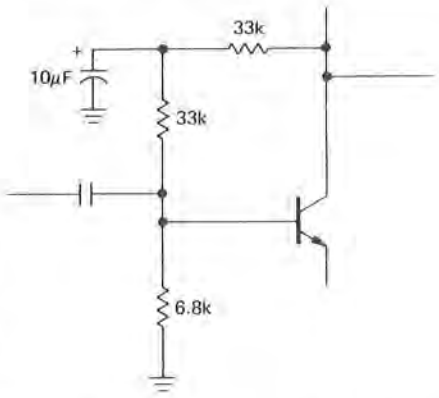


Figure 2.43. Eliminating feedback at signal frequencies.

Comments on biasing and gain

One important point about grounded emitter amplifier stages: You might think that the voltage gain can be raised by increasing the quiescent current, since the intrinsic emitter resistance r_e drops with rising current. Although r_e does go down with increasing collector current, the smaller collector resistor you need to obtain the same quiescent collector voltage just cancels the advantage. In fact, you can show that the small-signal voltage gain of a grounded emitter amplifier biased to $0.5V_{CC}$ is given by $G = 20V_{CC}$, independent of quiescent current.

EXERCISE 2.10
Show that the preceding statement is true.

If you need more voltage gain in one stage, one approach is to use a current source as an *active load.* Since its impedance is very high, single-stage voltage gains of 1000 or more are possible. Such an arrangement cannot be used with the biasing schemes we have discussed, but must be part of an overall dc feedback loop, a subject we will discuss in the next chapter. You should be sure such an amplifier looks into a high-impedance load; otherwise the gain obtained by high collector load impedance will be lost. Something like an emitter follower, a field-effect transistor (FET), or an op-amp presents a good load.

In radiofrequency amplifiers intended for use only over a narrow frequency range, it is common to use a parallel LC circuit as a collector load; in that case very high voltage gain is possible, since the LC circuit has high impedance (like a current source) at the signal frequency, with low impedance at dc. Since the LC

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is "tuned," out-of-band interfering signals (and distortion) are effectively rejected. Additional bonuses are the possibility of peak-to-peak output swings of $2V_{CC}$ and the use of transformer coupling from the inductor.

EXERCISE 2.11

Design a tuned common-emitter amplifier stage to operate at 100kHz. Use a bypassed emitter resistor, and set the quiescent current at 1.0mA. Assume $V_{CC} = +15$ volts and $L = 1.0$mH, and put a 6.2k resistor across the LC to set $Q = 10$ (to get a 10% bandpass; see Section 1.22). Use capacitive input coupling.

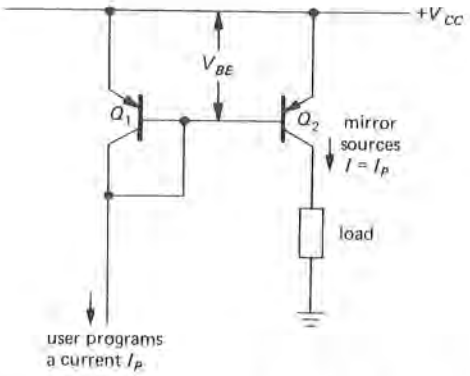


Figure 2.44. Classic bipolar-transistor matched-pair current mirror. Note the common convention of referring to the positive supply as V_{CC}, even when *pnp* transistors are used.

2.14 Current mirrors

The technique of matched base-emitter biasing can be used to make what is called a *current mirror* (Fig. 2.44). You "program" the mirror by sinking a current from Q_1's collector. That causes a V_{BE} for Q_1 appropriate to that current at the circuit temperature and for that transistor type. Q_2, matched to Q_1 (a monolithic dual transistor is ideal), is thereby programmed to source the same current to the load. The small base currents are unimportant.

One nice feature of this circuit is voltage compliance of the output transistor current source to within a few tenths of a volt of V_{CC}, since there is no emitter resistor drop to contend with. Also, in many applications it is handy to be able to program a current with a current. An easy way to generate the control current I_P is with a resistor (Fig. 2.45). Since the bases are a diode drop below V_{CC}, the 14.4k resistor produces a control current, and therefore an output current, of 1mA. Current mirrors can be used in transistor circuits whenever a current source is needed. They're very popular in integrated circuits, where (a) matched transistors abound and (b) the designer tries to make circuits that will work over a large range of supply voltages. There are even resistorless integrated circuit op-amps in which the operating current of the whole amplifier is set by one external resistor, with all the quiescent currents of the individual amplifier stages inside being determined by current mirrors.

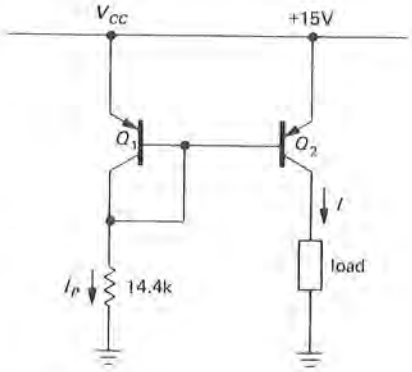


Figure 2.45

Current mirror limitations due to Early effect

One problem with the simple current mirror is that the output current varies a bit with changes in output voltage, i.e., the output impedance is not infinite. This is because of the slight variation of V_{BE} with collector voltage at a given current in Q_2 (due to Early effect); in other words, the

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curve of collector current versus collector-emitter voltage at a fixed base-emitter voltage is not flat (Fig. 2.46). In practice, the

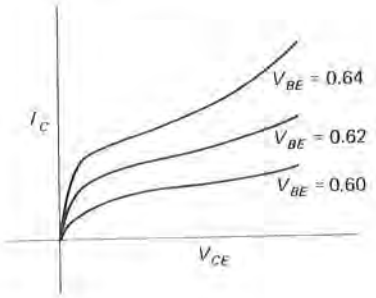


Figure 2.46

current might vary 25% or so over the output compliance range – much poorer performance than the current source with emitter resistor discussed earlier.

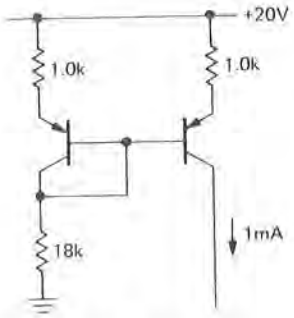


Figure 2.47. Improved current mirror.

One solution, if a better current source is needed (it often isn't), is the circuit shown in Figure 2.47. The emitter resistors are chosen to have at least a few tenths of a volt drop; this makes the circuit a far better current source, since the small variations of V_{BE} with V_{CE} are now negligible in determining the output current. Again, matched transistors should be used.

Wilson mirror

Another current mirror with very constant current is shown in the clever circuit of Figure 2.48. Q_1 and Q_2 are in the usual mirror configuration, but Q_3 now keeps Q_1's collector fixed at two diode drops

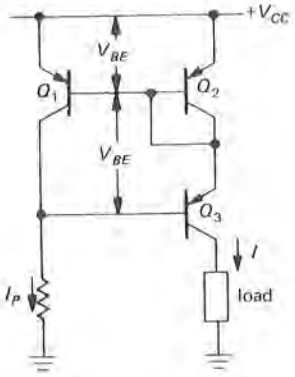


Figure 2.48. Wilson current mirror. Good stability with load variations is achieved through cascode transistor Q_3, which reduces voltage variations across Q_1.

below V_{CC}. That circumvents the Early effect in Q_1, whose collector is now the programming terminal, with Q_2 now sourcing the output current. Q_3 does not affect the balance of currents, since its base current is negligible; its only function is to pin Q_1's collector. The result is that both current-determining transistors (Q_1 and Q_2) have fixed collector-emitter drops; you can think of Q_3 as simply passing the output current through to a variable-voltage load (a similar trick is used in the cascode connection, which you will see later in the chapter). Q_3, by the way, does not have to be matched to Q_1 and Q_2.

Multiple outputs and current ratios

Current mirrors can be expanded to source (or sink, with *npn* transistors) current to several loads. Figure 2.49 shows the idea. Note that if one of the current source transistors saturates (e.g., if its load is disconnected), its base robs current from the shared base reference line, reducing the other output currents. The situation is

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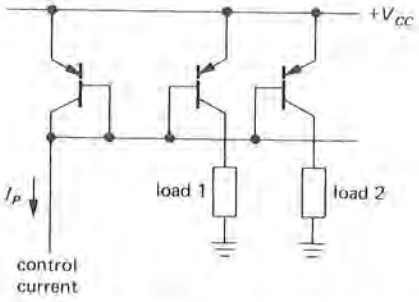


Figure 2.49. Current mirror with multiple outputs. This circuit is commonly used to obtain multiple programmable current sources.

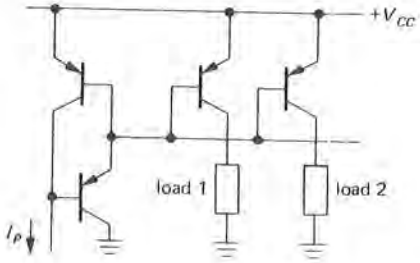


Figure 2.50

rescued by adding another transistor (Fig. 2.50).

Figure 2.51 shows two variations on the multiple-mirror idea. These circuits mirror twice (or half) the control current. In the design of integrated circuits, current mirrors with any desired current ratio can be made by adjusting the size of the emitter junctions appropriately.

Texas Instruments offers complete monolithic Wilson current mirrors in convenient TO-92 transistor packages. Their TL011 series includes 1:1, 1:2, 1:4, and 2:1 ratios, with output compliance from 1.2 to 40 volts. The Wilson configuration gives good current source performance – at constant programming current the output current increases by only 0.05% per volt – and they are very inexpensive (50 cents or less). Unfortunately, these useful devices are available in *npn* polarity only.

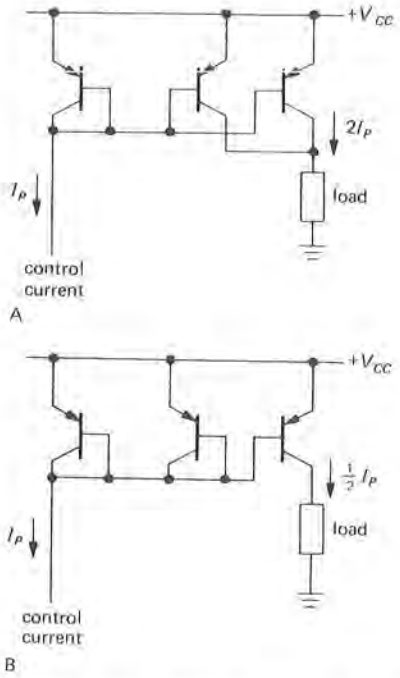


Figure 2.51. Current mirrors with current ratios other than 1:1.

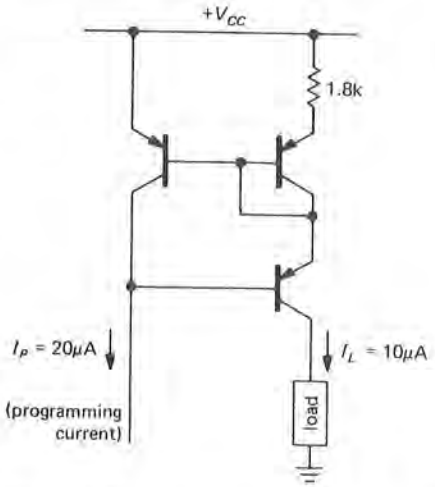


Figure 2.52. Modifying current-source output with an emitter resistor. Note that the output current is no longer a simple multiple of the progamming current.

Another way to generate an output current that is a fraction of the programming

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current is to add a resistor in the emitter circuit of the output transistor (Fig. 2.52). In any circuit where the transistors are operating at different current densities, the Ebers-Moll equation predicts that the difference in V_{BE} depends only on the ratio of the current densities. For matched transistors, the ratio of collector currents equals the ratio of current densities. The graph in Figure 2.53 is handy for determining the difference in base-emitter drops in such a situation. This makes it easy to design a "ratio mirror."

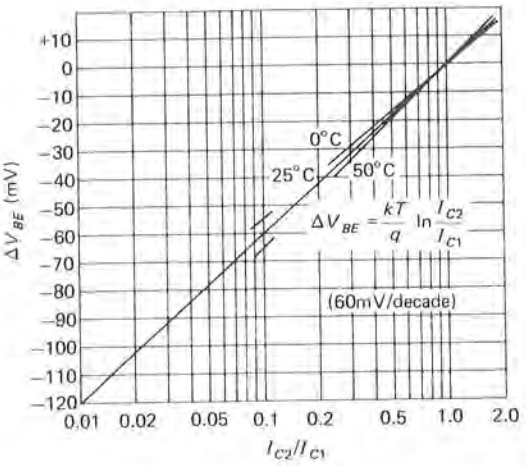


Figure 2.53. Collector current ratios for matched transistors as determined by the difference in applied base-emitter voltages.

EXERCISE 2.12
Show that the ratio mirror in Figure 2.52 works as advertised.

SOME AMPLIFIER BUILDING BLOCKS

□ 2.15 Push-pull output stages

As we mentioned earlier in the chapter, an *npn* emitter follower cannot sink current, and a *pnp* follower cannot source current. The result is that a single-ended follower operating between split supplies can drive a ground-returned load only if a high quiescent current is used (this is sometimes called a class A amplifier). The quiescent current must be at least as large as the maximum output current during peaks of the waveform, resulting in high quiescent power dissipation. For instance, Figure 2.54 shows a follower circuit to drive an 8 ohm load with up to 10 watts of audio. The *pnp* follower Q_1 is included to reduce drive requirements and to cancel Q_2's V_{BE} offset (zero volts input gives zero volts output). Q_1 could, of course, be omitted for simplicity. The hefty current source in Q_1's emitter load is used to ensure that there is sufficient base drive to Q_2 at the top of the signal swing. A resistor as emitter load would be inferior because it would have to be a rather low value (50Ω or less) in order to guarantee at least 50mA of base drive to Q_2 at the peak of the swing, when load current would be maximum and the drop across the resistor would be minimum; the resultant quiescent current in Q_1 would be excessive.

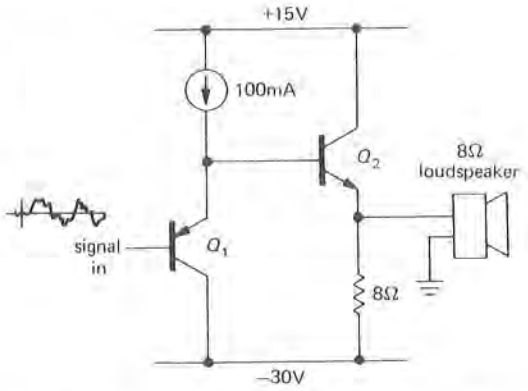


Figure 2.54. A 10 watt loudspeaker amplifier, built with a single-ended emitter follower, dissipates 165 watts of quiescent power!

The output of this example circuit can swing to nearly ±15 volts (peak) in both

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directions, giving the desired output power (9V rms across 8Ω). However, the output transistor dissipates 55 watts with no signal, and the emitter resistor dissipates another 110 watts. Quiescent power dissipation many times greater than the maximum output power is characteristic of this kind of class A circuit (transistor always in conduction); this obviously leaves a lot to be desired in applications where any significant amount of power is involved.

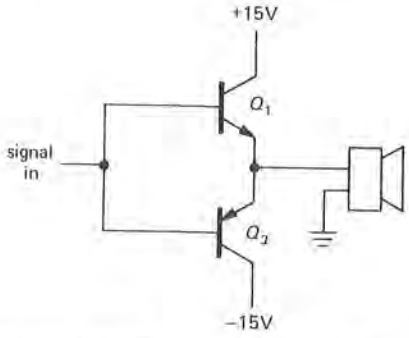


Figure 2.55. Push-pull emitter follower.

Figure 2.55 shows a push-pull follower to do the same job. Q_1 conducts on positive swings, Q_2 on negative swings. With zero input voltage, there is no collector current and no power dissipation. At 10 watts output power there is less than 10 watts dissipation in each transistor.

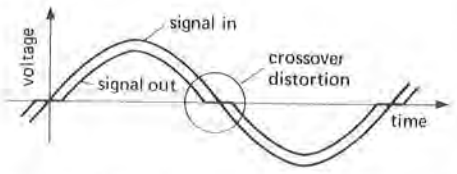


Figure 2.56. Crossover distortion in the push-pull follower.

□ *Crossover distortion in push-pull stages*

There is a problem with the preceding circuit as drawn. The output trails the input by a V_{BE} drop; on positive swings the output is about 0.6 volt less positive than the input, and the reverse for negative swings. For an input sine wave, the output would look as shown in Figure 2.56. In the language of the audio business, this is called crossover distortion. The best cure (feedback offers another method, although it is not entirely satisfactory) is to bias the push-pull stage into slight conduction, as in Figure 2.57.

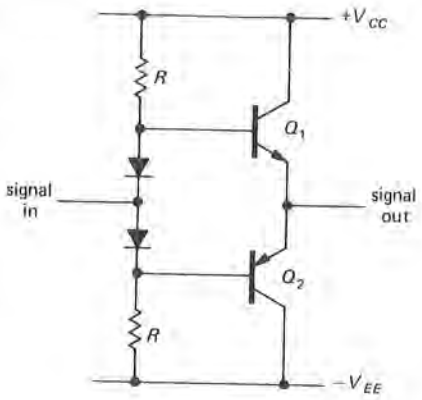


Figure 2.57. Biasing the push-pull follower to eliminate crossover distortion.

The bias resistors R bring the diodes into forward conduction, holding Q_1's base a diode drop above the input signal and Q_2's base a diode drop below the input signal. Now, as the input signal crosses through zero, conduction passes from Q_2 to Q_1; one of the output transistors is always on. R is chosen to provide enough base current for the output transistors at the peak output swing. For instance, with ±20 volt supplies and an 8 ohm load running up to 10 watts sine-wave power, the peak base voltage is about 13.5 volts, and the peak load current is about 1.6 amps. Assuming a transistor beta of 50 (power transistors generally have lower current gain than small-signal transistors), the 32mA of necessary base current will require base resistors of about 220 ohms (6.5V from V_{CC} to base at peak swing).

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Thermal stability in class B push-pull amplifiers

The preceding amplifier (sometimes called a class B amplifier, meaning that each transistor conducts over half the cycle) has one bad feature: It is not thermally stable. As the output transistors warm up (and they will get hot, because they are dissipating power when signal is applied), their V_{BE} drops, and quiescent collector current begins to flow. The added heat this produces causes the situation to get worse, with the strong possibility of what is called *thermal runaway* (whether it runs away or not depends on a number of factors, including how large a "heat sink" is used, how well the diode temperature tracks the transistor, etc.). Even without runaway, better control over the circuit is needed, usually with the sort of arrangement shown in Figure 2.58.

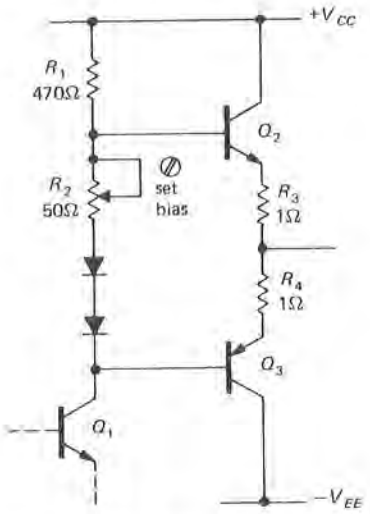


Figure 2.58. Small emitter resistors improve thermal stability in the push-pull follower.

For variety, the input is shown coming from the collector of the previous stage; R_1 now serves the dual purpose of being Q_1's collector resistor and providing current to bias the diodes and bias-setting resistor in the push-pull base circuit. Here R_3 and R_4, typically a few ohms or less, provide a "cushion" for the critical quiescent current biasing: The voltage between the bases of the output transistors must now be a bit greater than two diode drops, and you provide the extra with adjustable biasing resistor R_2 (often replaced by a third series diode). With a few tenths of a volt across R_3 and R_4, the temperature variation of V_{BE} doesn't cause the current to rise very rapidly (the larger the drop across R_3 and R_4, the less sensitive it is), and the circuit will be stable. Stability is improved by mounting the diodes in physical contact with the output transistors (or their heat sinks).

You can estimate the thermal stability of such a circuit by remembering that the base-emitter drop decreases by about 2.1mV for each 1°C rise and that the collector current increases by a factor of 10 for every 60mV increase in base-emitter voltage. For example, if R_2 were replaced by a diode, you would have three diode drops between the bases of Q_2 and Q_3, leaving about one diode drop across the series combination of R_3 and R_4. (The latter would then be chosen to give an appropriate quiescent current, perhaps 50mA for an audio power amplifier.) The worst case for thermal stability occurs if the biasing diodes are not thermally coupled to the output transistors.

Let us assume the worst and calculate the increase in output-stage quiescent current corresponding to a 30°C temperature rise in output transistor temperature. That's not a lot for a power amplifier, by the way. For that temperature rise, the V_{BE} of the output transistors will decrease by about 63mV at constant current, raising the voltage across R_3 and R_4 by about 20% (i.e., the quiescent current will rise by about 20%). The corresponding figure for the preceding amplifier circuit without emitter resistors (Fig. 2.57) will be a factor of 10 rise in quiescent current (recall that

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I_C increases a decade per 60mV increase in V_{BE}), i.e., 1000%. The improved thermal stability of this biasing arrangement is evident.

This circuit has the additional advantage that by adjusting the quiescent current, you have some control over the amount of residual crossover distortion. A push-pull amplifier biased in this way to obtain substantial quiescent current at the crossover point is sometimes referred to as a class AB amplifier, meaning that both transistors conduct simultaneously during a portion of the cycle. In practice, you choose a quiescent current that is a good compromise between low distortion and excessive quiescent dissipation. Feedback, the subject of the next chapter, is almost always used to reduce distortion still further.

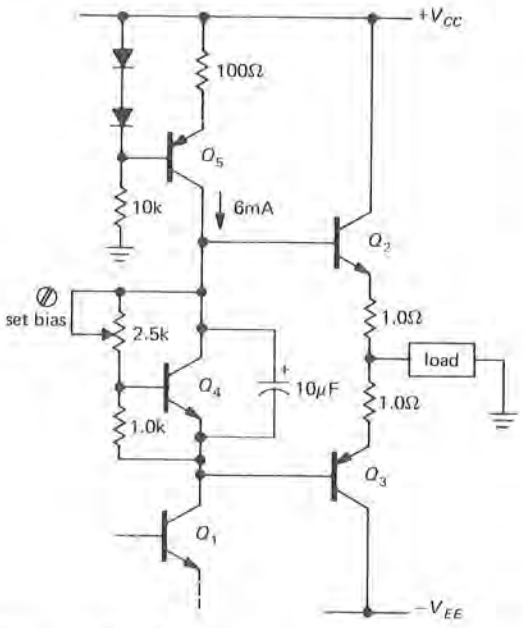


Figure 2.59. Biasing a push-pull output stage for low crossover distorion and good thermal stability.

An alternative method for biasing a push-pull follower is shown in Figure 2.59. Q_4 acts as an adjustable diode: The base resistors are a divider, and therefore Q_4's collector-emitter voltage will stabilize at a value that puts 1 diode drop from base to emitter, since any greater V_{CE} will bring it into heavy conduction. For instance, if both resistors were 1k, the transistor would turn on at 2 diode drops, collector to emitter. In this case, the bias adjustment lets you set the push-pull interbase voltage anywhere from 1 to 3.5 diode drops. The 10μF capacitor ensures that both output transistor bases see the same signal; such a bypass capacitor is a good idea for any biasing scheme you use. In this circuit, Q_1's collector resistor has been replaced by current source Q_5. That's a useful circuit variation, because with a resistor it is sometimes difficult to get enough base current to drive Q_2 near the top of the swing. A resistor small enough to drive Q_2 sufficiently results in high quiescent collector current in Q_1 (with high dissipation), and also reduced voltage gain (remember that $G = -R_{\text{collector}}/R_{\text{emitter}}$). Another solution to the problem of Q_2's base drive is the use of *bootstrapping*, a technique that will be discussed shortly.

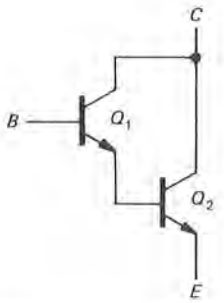


Figure 2.60. Darlington transistor configuration.

2.16 Darlington connection

If you hook two transistors together as in Figure 2.60, the result behaves like a single transistor with beta equal to the

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product of the two transistor betas. This can be very handy where high currents are involved (e.g., voltage regulators or power amplifier output stages), or for input stages of amplifiers where very high input impedance is necessary.

For a Darlington transistor the base-emitter drop is twice normal, and the saturation voltage is at least one diode drop (since Q_1's emitter must be a diode drop above Q_2's emitter). Also, the combination tends to act like a rather slow transistor because Q_1 cannot turn off Q_2 quickly. This problem is usually taken care of by including a resistor from base to emitter of Q_2 (Fig. 2.61). R also prevents leakage current through Q_1 from biasing

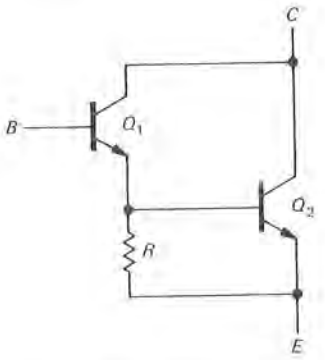


Figure 2.61. Improving turn-off speed in a Darlington pair.

Q_2 into conduction; its value is chosen so that Q_1's leakage current (nanoamps for small-signal transistors, as much as hundreds of microamps for power transistors) produces less than a diode drop across R and so that R doesn't sink a large proportion of Q_2's base current when it has a diode drop across it. Typically R might be a few hundred ohms in a power transistor Darlington, or a few thousand ohms for a small-signal Darlington.

Darlington transistors are available as single packages, usually with the base-emitter resistor included. A typical example is the *npn* power Darlington 2N6282, with current gain of 2400 (typically) at a collector current of 10 amps.

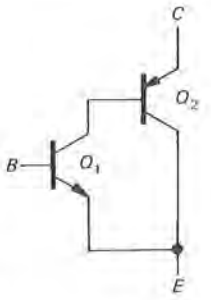


Figure 2.62. Sziklai connection ("complementary Darlington").

Sziklai connection

A similar beta-boosting configuration is the Sziklai connection, sometimes referred to as a complementary Darlington (Fig. 2.62). This combination behaves like an *npn* transistor, again with large beta. It has only a single base-emitter drop, but it also cannot saturate to less than a diode drop. A small resistor from base to emitter of Q_2 is advisable. This connection is common in push-pull power output stages where the designer wishes to use one polarity of output transistor only. Such a circuit is shown in Figure 2.63. As before, R_1 is Q_1's collector resistor. Darlington Q_2Q_3 behaves like a single *npn* transistor with high current gain. The Sziklai connected pair Q_4Q_5 behaves like a single high-gain *pnp* power transistor. As before, R_3 and R_4 are small. This circuit is sometimes called a pseudocomplementary push-pull follower. A true complementary stage would use a Darlington-connected *pnp* pair for Q_4Q_5.

Superbeta transistor

The Darlington connection and its near relatives should not be confused with the so-called superbeta transistor, a device

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with very high h_{FE} achieved through the manufacturing process. A typical superbeta transistor is the 2N5962, with a guaranteed minimum current gain of 450 at collector currents from 10μA to 10mA; it belongs to the 2N5961–2N5963 series; with a range of maximum V_{CE}s of 30 to 60 volts (if you need higher collector voltage, you have to settle for lower beta). Superbeta matched pairs are available for use in low-level amplifiers that require matched characteristics, a topic we will discuss in Section 2.18. Examples are the LM394 and MAT-01 series; these provide high-gain *npn* transistor pairs whose V_{BE}s are matched to a fraction of a millivolt (as little as 50μV in the best versions) and whose h_{FE}s are matched to about 1%. The MAT-03 is a *pnp* matched pair.

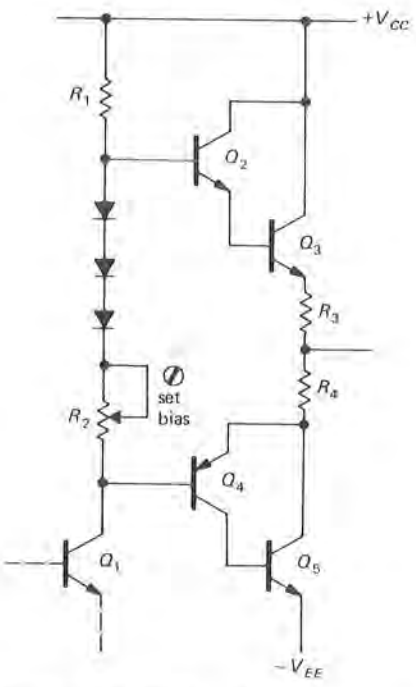


Figure 2.63. Push-pull power stage using only *npn* output transistors.

It is possible to combine superbeta transistors in a Darlington connection. Some commercial devices (e.g., the LM11 and LM316 op-amps) achieve base bias currents as low as 50 *pico*amps this way.

□ 2.17 Bootstrapping

When biasing an emitter follower, for instance, you choose the base voltage divider resistors so that the divider presents a stiff voltage source to the base, i.e., their parallel impedance is much less than the impedance looking into the base. For this reason the resulting circuit has an input impedance dominated by the voltage divider – the driving signal sees a much lower impedance than would otherwise be necessary. Figure 2.64 shows an example. The input

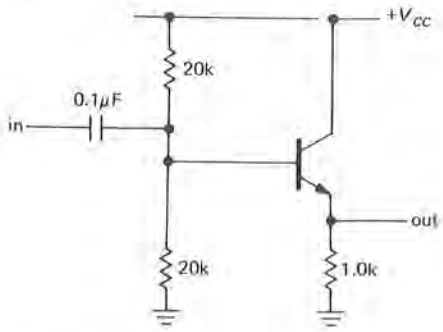


Figure 2.64

resistance of about 9k is mostly due to the voltage-divider impedance of 10k. It is always desirable to keep input impedances high, and anyway it's a shame to load the input with the divider, which, after all, is only there to bias the transistor. Bootstrapping is the colorful name given to a technique that circumvents this problem (Fig. 2.65). The transistor is biased by the divider R_1R_2 through series resistor R_3. C_2 is chosen to have low impedance at signal frequencies compared with the bias resistors. As always, bias is stable if the dc impedance seen from the base (in this case 9.7k) is much less than the dc impedance looking into the base (in

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this case approximately 100k). But now the signal-frequency input impedance is no longer the same as the dc impedance. Look at it this way: An input wiggle v_{in} results in an emitter wiggle $v_E \approx v_{in}$. So the change in current through bias resistor R_3 is $i = (v_{in} - v_E)/R_3 \approx 0$, i.e., Z_{in} (due to bias string) $= v_{in}/i_{in} \approx$ infinity. We've made the loading (shunt) impedance of the bias network very large *at signal frequencies.*

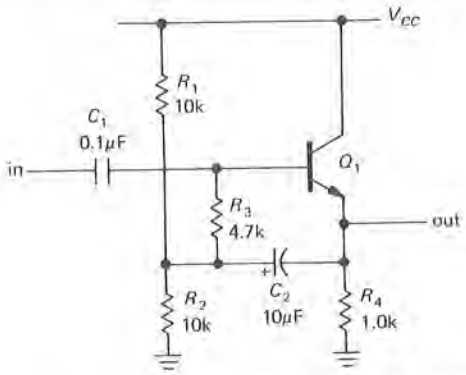


Figure 2.65. Raising the input impedance of an emitter follower at signal frequencies by bootstrapping the base bias divider.

Another way of seeing this is to notice that R_3 always has the same voltage across it at signal frequencies (since both ends of the resistor have the same voltage changes), i.e., it's a current source. But a current source has infinite impedance. Actually, the effective impedance is less than infinity because the gain of a follower is slightly less than 1. That is so because the base-emitter drop depends on collector current, which changes with the signal level. You could have predicted the same result from the voltage-dividing effect of the impedance looking into the emitter [$r_e = 25/I_C$(mA) ohms] combined with the emitter resistor. If the follower has voltage gain A ($A \approx 1$), the effective value of R_3 at signal frequencies is

$$R_3/(1 - A)$$

In practice the value of R_3 is effectively increased by a hundred or so, and the input impedance is then dominated by the transistor's base impedance. The emitter-degenerated amplifier can be bootstrapped in the same way, since the signal on the emitter follows the base. Note that the bias divider circuit is driven by the low-impedance emitter output at signal frequencies, thus isolating the input signal from this usual task.

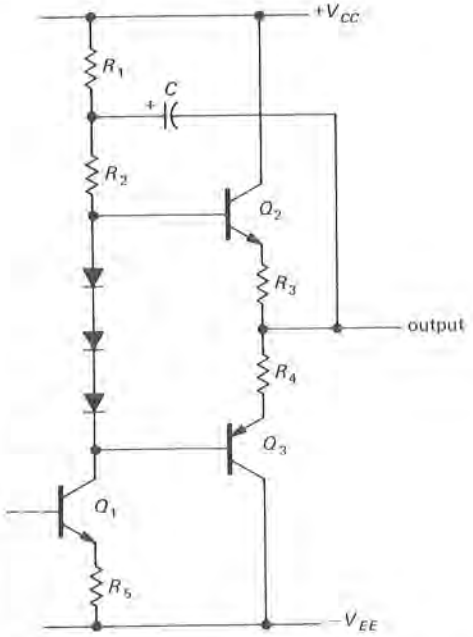


Figure 2.66. Bootstrapping driver-stage collector load resistor in a power amplifier.

□ *Bootstrapping collector load resistors*

The bootstrap principle can be used to increase the effective value of a transistor's collector load resistor, if that stage drives a follower. That can increase the voltage gain of the stage substantially [recall that $G_V = -g_m R_C$, with $g_m = 1/(R_E + r_e)$]. Figure 2.66 shows an example of a bootstrapped push-pull output stage similar to the push-pull follower circuit we saw earlier. Because the output follows Q_2's base

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signal, C bootstraps Q_1's collector load, keeping a constant voltage across R_2 as the signal varies (C must be chosen to have low impedance compared with R_1 and R_2 at all signal frequencies). That makes R_2 look like a current source, raising Q_1's voltage gain and maintaining good base drive to Q_2, even at the peaks of the signal swing. When the signal gets near V_{CC}, the junction of R_1 and R_2 actually rises above V_{CC} because of the stored charge in C. In this case, if $R_1 = R_2$ (not a bad choice) the junction between them rises to 1.5 times V_{CC} when the output reaches V_{CC}. This circuit has enjoyed considerable popularity in commercial audio amplifier design, although a simple current source in place of the bootstrap is superior, since it maintains the improvement at low frequencies and eliminates the undesirable electrolytic capacitor.

2.18 Differential amplifiers

The differential amplifier is a very common configuration used to amplify the difference voltage between two input signals. In the ideal case the output is entirely independent of the individual signal levels – only the difference matters. When both inputs change levels together, that's a *common-mode* input change. A differential change is called *normal mode*. A good differential amplifier has a high *common-mode rejection ratio* (CMRR), the ratio of response for a normal-mode signal to the response for a common-mode signal of the same amplitude. CMRR is usually specified in decibels. The common-mode input range is the voltage level over which the inputs may vary.

Differential amplifiers are important in applications where weak signals are contaminated by "pickup" and other miscellaneous noise. Examples include digital signals transferred over long cables (usually twisted pairs of wires), audio signals (the term "balanced" means differential, usually 600Ω impedance, in the audio business), radiofrequency signals (twin-lead cable is differential), electrocardiogram voltages, magnetic-core memory readout signals, and numerous other applications. A differential amplifier at the receiving end restores the original signal if the common-mode signals are not too large. Differential amplifiers are universally used in operational amplifiers, which we will come to soon. They're very important in dc amplifier design (amplifiers that amplify clear down to dc, i.e., have no coupling capacitors) because their symmetrical design is inherently compensated against thermal drifts.

Figure 2.67 shows the basic circuit. The output is taken off one collector with respect to ground; that is called a *single-ended output* and is the most common configuration. You can think of this amplifier as a device that amplifies a difference signal and converts it to a single-ended signal so that ordinary subcircuits (followers, current sources, etc.) can make use of the output. (If, instead, a differential output is desired, it is taken between the collectors.)

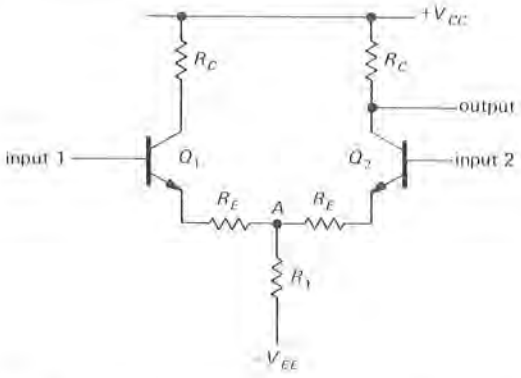


Figure 2.67. Classic transistor differential amplifier.

What is the gain? That's easy enough to calculate: Imagine a symmetrical input signal wiggle, in which input 1 rises by

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v_{in} (a small-signal variation) and input 2 drops by the same amount. As long as both transistors stay in the active region, point A remains fixed. The gain is then determined as with the single transistor amplifier, remembering that the input change is actually twice the wiggle on either base: $G_{diff} = R_C/2(r_e + R_E)$. Typically R_E is small, 100 ohms or less, or it may be omitted entirely. Differential voltage gains of a few hundred are typical.

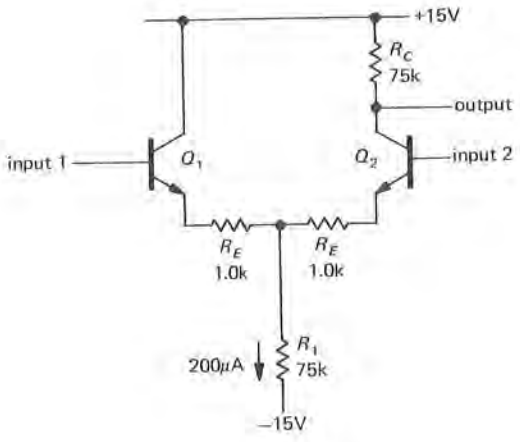
The common-mode gain can be determined by putting identical signals v_{in} on both inputs. If you think about it correctly (remembering that R_1 carries both emitter currents), you'll find $G_{CM} = -R_C/(2R_1 + R_E)$. Here we've ignored the small r_e, because R_1 is typically large, at least a few thousand ohms. We really could have ignored R_E as well. The CMRR is roughly $R_1/(r_e + R_E)$. Let's look at a typical example (Fig. 2.68) to get some familiarity with differential amplifiers.

R_C is chosen for a quiescent current of 100μA. As usual, we put the collector at $0.5V_{CC}$ for large dynamic range. Q_1's collector resistor can be omitted, since no output is taken there. R_1 is chosen to give total emitter current of 200μA, split equally between the two sides when the (differential) input is zero. From the formulas just derived, this amplifier has a differential gain of 30 and a common-mode gain of 0.5. Omitting the 1.0k resistors raises the differential gain to 150, but drops the (differential) input impedance from about 250k to about 50k (you can substitute Darlington transistors in the input stage to raise the impedance into the megohm range, if necessary).

Remember that the maximum gain of a single-ended grounded emitter amplifier biased to $0.5V_{CC}$ is $20V_{CC}$. In the case of a differential amplifier the maximum differential gain ($R_E = 0$) is half that figure, or (for arbitrary quiescent point) 20 times the voltage across the collector resistor. The corresponding maximum CMRR (again with $R_E = 0$) is equal to 20 times the voltage across R_1.

EXERCISE 2.13
Verify that these expressions are correct. Then design a differential amplifier to your own specifications.

The differential amplifier is sometimes called a "long-tailed pair," because if the length of a resistor symbol indicated its magnitude, the circuit would look like Figure 2.69. The long tail determines the



$$G_{diff} = \frac{v_{out}}{v_1 - v_2} = \frac{R_C}{2(R_E + r_e)}$$

$$G_{CM} = -\frac{R_C}{2R_1 + R_E + r_e}$$

$$CMRR \approx \frac{R_1}{R_E + r_e}$$

Figure 2.68. Calculating differential amplifier performance.

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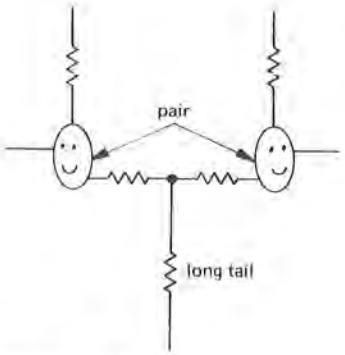


Figure 2.69

common-mode gain, and the small inter-emitter resistance (including intrinsic emitter resistance r_e) determines the differential gain.

Current-source biasing

The common-mode gain of the differential amplifier can be reduced enormously by substituting a current source for R_1. Then R_1 effectively becomes very large, and the common-mode gain is nearly zero. If you prefer, just imagine a common-mode input swing; the emitter current source maintains a constant total emitter current, shared equally by the two collector circuits, by symmetry. The output is therefore unchanged. Figure 2.70 shows an example. The CMRR of this circuit, using an LM394 monolithic transistor pair for Q_1 and Q_2 and a 2N5963 current source is 100,000:1 (100dB). The common-mode input range for this circuit goes from -12 volts to $+7$ volts; it is limited at the low end by the compliance of the emitter current source and at the high end by the collector's quiescent voltage.

Be sure to remember that this amplifier, like all transistor amplifiers, must have a dc bias path to the bases. If the input is capacitively coupled, for instance, you must have base resistors to ground. An additional caution for differential amplifiers,

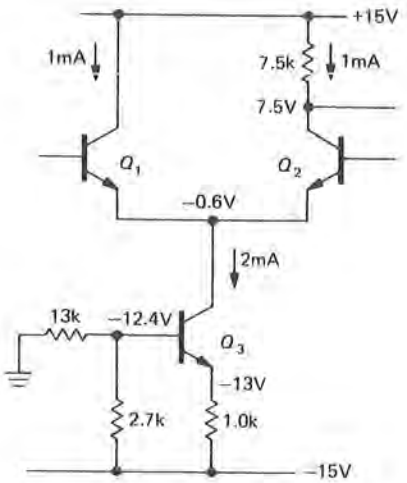


Figure 2.70. Improving CMRR of the differential amplifier with a current source.

particularly those without inter-emitter resistors: Bipolar transistors can tolerate only 6 volts of base-emitter reverse bias before breakdown; thus, applying a differential input voltage larger than this will destroy the input stage (if there is no inter-emitter resistor). An inter-emitter resistor limits the breakdown current and prevents destruction, but the transistors may be degraded (in h_{fe}, noise, etc.). In either case the input impedance drops drastically during reverse conduction.

Use in single-ended dc amplifiers

A differential amplifier makes an excellent dc amplifier, even for single-ended inputs. You just ground one of the inputs and connect the signal to the other (Fig. 2.71). You might think that the "unused" transistor could be eliminated. Not so! The differential configuration is inherently compensated for temperature drifts, and even when one input is at ground that transistor is still doing something: A temperature change causes both V_{BE}s to change the same amount, with no change in balance or output. That is, changes in V_{BE} are not amplified by G_{diff} (only by G_{CM},

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which can be made essentially zero). Furthermore, the cancellation of V_{BE}s means that there are no 0.6 volt drops at the input to worry about. The quality of a dc amplifier constructed this way is limited only by mismatching of input V_{BE}s or their temperature coefficients. Commercial monolithic transistor pairs and commercial differential amplifier ICs are available with extremely good matching (e.g., the MAT-01 *npn* monolithic matched pair has a typical drift of V_{BE} between the two transistors of 0.15μV/°C and 0.2μV per month).

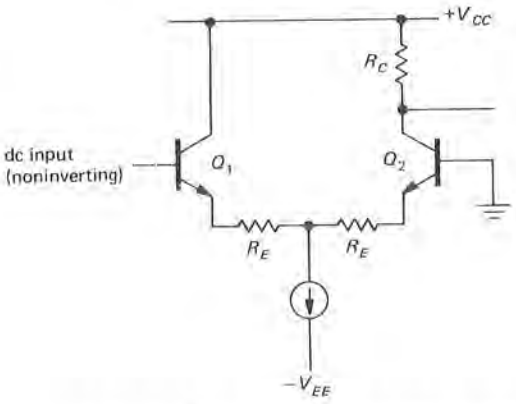


Figure 2.71. A differential amplifier can be used as a precision single-ended dc amplifier.

Either input could have been grounded in the preceding circuit example. The choice depends on whether or not the amplifier is supposed to invert the signal. (The configuration shown is preferable at high frequencies, however, because of *Miller effect*; see Section 2.19.) The connection shown is noninverting, and so the inverting input has been grounded. This terminology carries over to op-amps, which are simply high-gain differential amplifiers.

Current mirror active load

As with the simple grounded emitter amplifier, it is sometimes desirable to have a single-stage differential amplifier with very high gain. An elegant solution is a current mirror active load (Fig. 2.72). Q_1Q_2 is the differential pair with emitter current source. Q_3 and Q_4, a current mirror, form the collector load. The high effective collector load impedance provided by the mirror yields voltage gains of 5000 or more, assuming no load at the amplifier's output. Such an amplifier is usually used only within a feedback loop, or as a comparator (discussed in the next section). Be sure to load such an amplifier with a high impedance, or the gain will drop enormously.

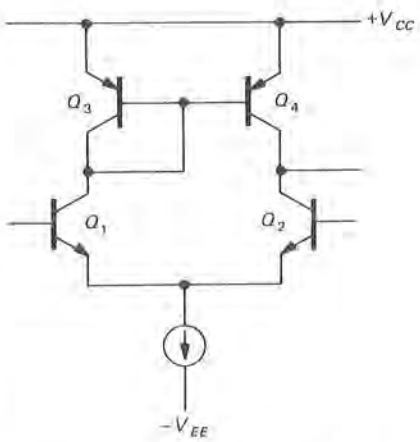


Figure 2.72. Differential amplifier with active current mirror load.

Differential amplifiers as phase splitters

The collectors of a symmetrical differential amplifier generate equal signal swings of opposite phase. By taking outputs from both collectors, you've got a phase splitter. Of course, you could also use a differential amplifier with both differential inputs and differential outputs. This differential output signal could then be used to drive an additional differential amplifier stage, with greatly improved overall common-mode rejection.

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Differential amplifiers as comparators

Because of its high gain and stable characteristics, the differential amplifier is the main building block of the *comparator*, a circuit that tells which of two inputs is larger. They are used for all sorts of applications: switching on lights and heaters, generating square waves from triangles, detecting when a level in a circuit exceeds some particular threshold, class D amplifiers and pulse-code modulation, switching power supplies, etc. The basic idea is to connect a differential amplifier so that it turns a transistor switch on or off, depending on the relative levels of the input signals. The linear region of amplification is ignored, with one or the other of the two input transistors cut off at any time. A typical hookup is illustrated in the next section by a temperature-controlling circuit that uses a resistive temperature sensor (thermistor).

2.19 Capacitance and Miller effect

In our discussion so far we have used what amounts to a dc, or low-frequency, model of the transistor. Our simple current amplifier model and the more sophisticated Ebers-Moll transconductance model both deal with voltages, currents, and resistances seen at the various terminals. With these models alone we have managed to go quite far, and in fact these simple models contain nearly everything you will ever need to know to design transistor circuits. However, one important aspect that has serious impact on high-speed and high-frequency circuits has been neglected: the existence of capacitance in the external circuit and in the transistor junctions themselves. Indeed, at high frequencies the effects of capacitance often dominate circuit behavior; at 100 MHz a typical junction capacitance of 5pF has an impedance of 320 ohms!

We will deal with this important subject in detail in Chapter 13. At this point we would merely like to state the problem, illustrate some of its circuit incarnations, and suggest some methods of circumventing the problem. It would be a mistake to leave this chapter without realizing the nature of this problem. In the course of this brief discussion we will encounter the famous *Miller effect* and the use of configurations such as the cascode to overcome it.

Junction and circuit capacitance

Capacitance limits the speed at which the voltages within a circuit can swing ("slew rate"), owing to finite driving impedance or current. When a capacitance is driven by a finite source resistance, you see RC exponential charging behavior, whereas a capacitance driven by a current source leads to slew-rate-limited waveforms (ramps). As general guidance, reducing the source impedances and load capacitances and increasing the drive currents within a circuit will speed things up. However, there are some subtleties connected with feedback capacitance and input capacitance. Let's take a brief look.

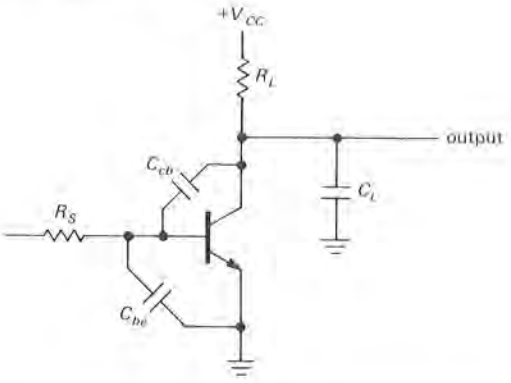


Figure 2.73. Junction and load capacitances in a transistor amplifier.

The circuit in Figure 2.73 illustrates most of the problems of junction capacitance. The output capacitance forms a

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time constant with the output resistance R_L (R_L includes both the collector and load resistances, and C_L includes both junction and load capacitances), giving a rolloff starting at some frequency $f = 1/2\pi R_L C_L$. The same is true for the input capacitance in combination with the source impedance R_S.

Miller effect

C_{cb} is another matter. The amplifier has some overall voltage gain G_V, so a small voltage wiggle at the input results in a wiggle G_V times larger (and inverted) at the collector. This means that the signal source sees a current through C_{cb} that is $G_V + 1$ times as large as if C_{cb} were connected from base to ground; i.e., for the purpose of input rolloff frequency calculations, the feedback capacitance behaves like a capacitor of value $C_{cb}(G_V + 1)$ from input to ground. This effective increase of C_{cb} is known as the Miller effect. It often dominates the rolloff characteristics of amplifiers, since a typical feedback capacitance of 4pF can look like several hundred picofarads to ground.

There are several methods available to beat the Miller effect. It is absent altogether in a grounded base stage. You can decrease the source impedance driving a grounded emitter stage by using an emitter follower. Figure 2.74 shows two other possibilities. The differential amplifier circuit (with no collector resistor in Q_1) has no Miller effect; you can think of it as an emitter follower driving a grounded base amplifier. The second circuit is the famous cascode configuration. Q_1 is a grounded emitter amplifier with R_L as its collector resistor. Q_2 is interposed in the collector path to prevent Q_1's collector from swinging (thereby eliminating the Miller effect) while passing the collector current through to the load resistor unchanged. V_+ is a fixed bias voltage, usually set a few volts above Q_1's emitter voltage to pin Q_1's

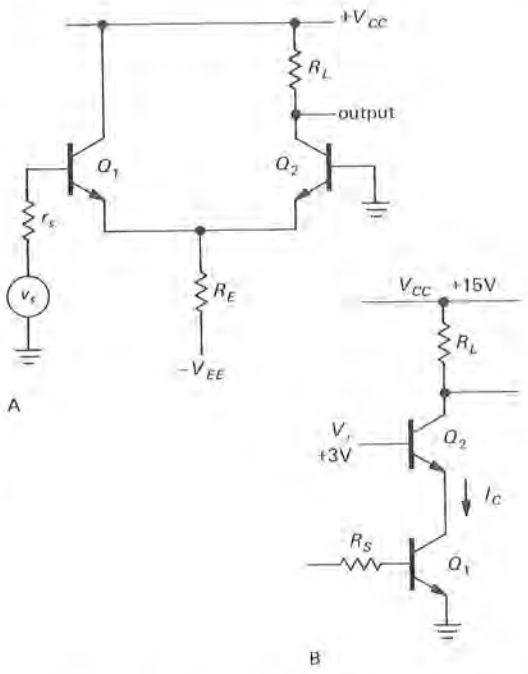


Figure 2.74. Two circuit configurations that avoid Miller effect. Circuit B is the cascode.

collector and keep it in the active region. This fragment is incomplete as shown; you could either include a bypassed emitter resistor and base divider for biasing (as we did earlier in the chapter) or include it within an overall loop with feedback at dc. V_+ might be provided from a divider or zener, with bypassing to keep it stiff at signal frequencies.

EXERCISE 2.14

Explain in detail why there is no Miller effect in either transistor in the preceding differential amplifier and cascode circuits.

Capacitive effects can be somewhat more complicated than this brief introduction might indicate. In particular: (a) The rolloffs due to feedback and output capacitances are not entirely independent; in the terminology of the trade there is pole splitting, an effect we will explain in the next chapter. (b) The input capacitance still

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has an effect, even with a stiff input signal source. In particular, current that flows through C_{be} is not amplified by the transistor. This base current "robbing" by the input capacitance causes the transistor's small-signal current gain h_{fe} to drop at high frequencies, eventually reaching unity at a frequency known as f_T. (c) To complicate matters, the junction capacitances depend on voltage. C_{be} changes so rapidly with base current that it is not even specified on transistor data sheets; f_T is given instead. (d) When a transistor is operated as a switch, effects associated with charge stored in the base region of a saturated transistor cause an additional loss of speed. We will take up these and other topics having to do with high-speed circuits in Chapter 13.

2.20 Field-effect transistors

In this chapter we have dealt exclusively with *bipolar junction transistors* (BJTs), characterized by the Ebers-Moll equation. BJTs were the original transistors, and they still dominate analog circuit design. However, it would be a mistake to continue without a few words of explanation about the other kind of transistor, the field-effect transistor (FET), which we will take up in detail in the next chapter.

The FET behaves in many ways like an ordinary bipolar transistor. It is a 3-terminal amplifying device, available in both polarities, with a terminal (the *gate*) that controls the current flow between the other two terminals (*source* and *drain*). It has a unique property, though: The gate draws no current, except for leakage. This means that extremely high input impedances are possible, limited only by capacitance and leakage effects. With FETs you don't have to worry about providing substantial base current, as was necessary with the BJT circuit design of this chapter. Input currents measured in *pico*amperes are commonplace. Yet the FET is a rugged and capable device, with voltage and current ratings comparable to those of bipolar transistors.

Most of the available devices fabricated with transistors (matched pairs, differential and operational amplifiers, comparators, high-current switches and amplifiers, radiofrequency amplifiers, and digital logic) are also available with FET construction, often with superior performance. Furthermore, microprocessors and memory (and other large-scale digital electronics) are built almost exclusively with FETs. Finally, the area of micropower design is dominated by FET circuits.

FETs are so important in electronic design that we will devote the next chapter to them, before treating operational amplifiers and feedback in Chapter 4. We urge the reader to be patient with us as we lay the groundwork in these first three difficult chapters; that patience will be rewarded many times over in the succeeding chapters, as we explore the enjoyable topics of circuit design with operational amplifiers and digital integrated circuits.

SOME TYPICAL TRANSISTOR CIRCUITS

To illustrate some of the ideas of this chapter, let's look at a few examples of circuits with transistors. The range of circuits we can cover is necessarily limited, since real-world circuits often use negative feedback, a subject we will cover in Chapter 4.

2.21 Regulated power supply

Figure 2.75 shows a very common configuration. R_1 normally holds Q_1 on; when the output reaches 10 volts, Q_2 goes into conduction (base at 5V), preventing further rise of output voltage by shunting base current from Q_1's base. The supply can be made adjustable by replacing R_2 and R_3

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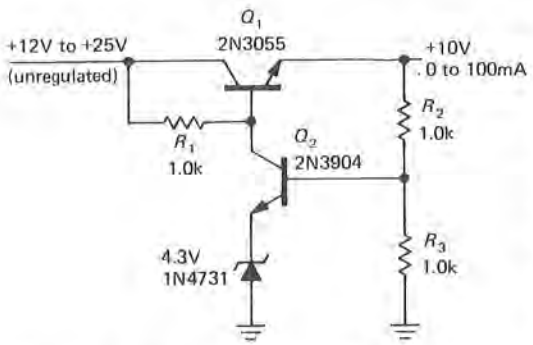


Figure 2.75. Feedback voltage regulator.

by a potentiometer. This is actually an example of negative feedback: Q_2 "looks at" the output and does something about it if the output isn't at the right voltage.

2.22 Temperature controller

The schematic diagram in Figure 2.76 shows a temperature controller based on a *thermistor* sensing element, a device that changes resistance with temperature. Differential Darlington $Q_1 - Q_4$ compares the voltage of the adjustable reference divider R_4–R_6 with the divider formed from the thermistor and R_2. (By comparing *ratios* from the same supply, the comparison becomes insensitive to supply variations; this particular configuration is called a Wheatstone bridge.) Current mirror Q_5Q_6 provides an active load to raise the gain, and mirror Q_7Q_8 provides emitter current. Q_9 compares the differential amplifier output with a fixed voltage, saturating Darlington $Q_{10}Q_{11}$, which supplies power to the heater, if the thermistor is too cold. R_9 is a current-sensing resistor that turns on protection transistor Q_{12} if the output current exceeds about 6 amps; that removes base drive from $Q_{10}Q_{11}$, preventing damage.

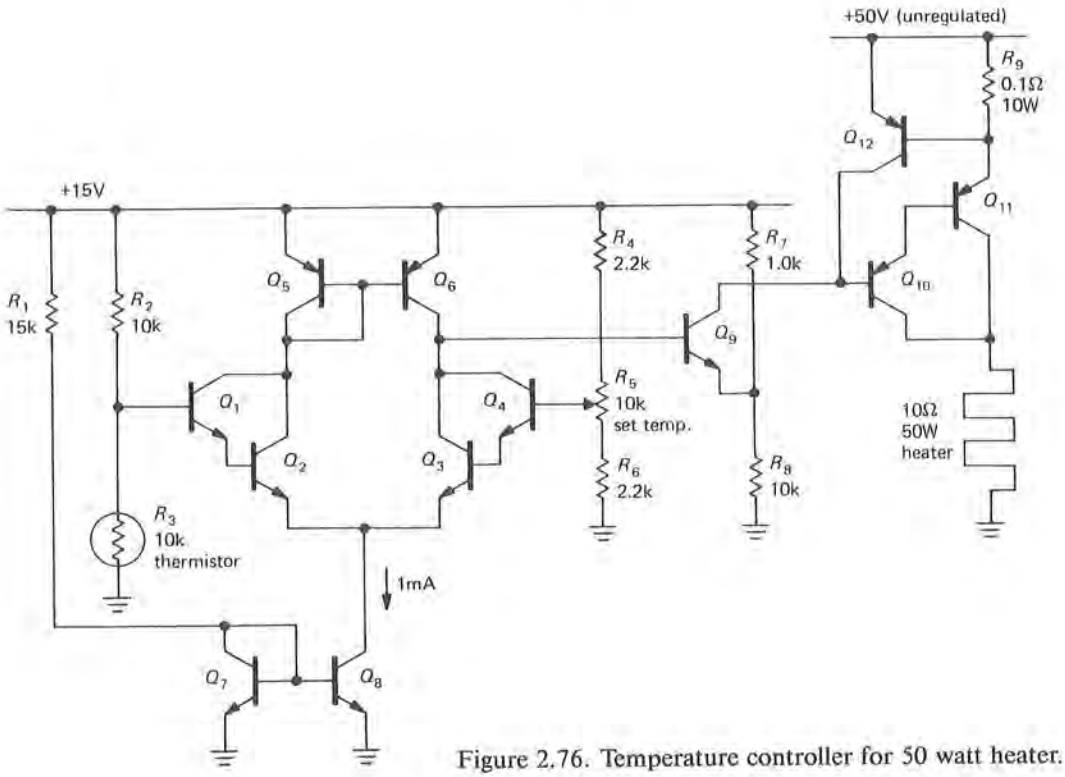


Figure 2.76. Temperature controller for 50 watt heater.

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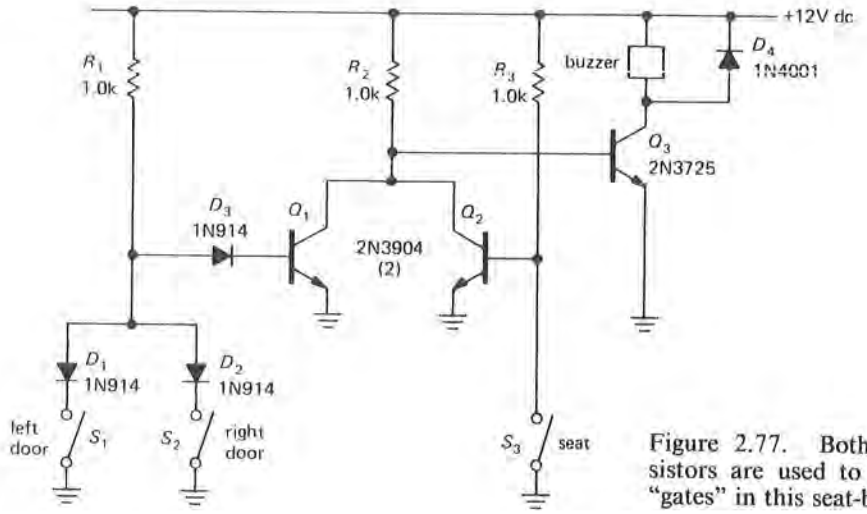


Figure 2.77. Both diodes and transistors are used to make digital logic "gates" in this seat-belt buzzer circuit.

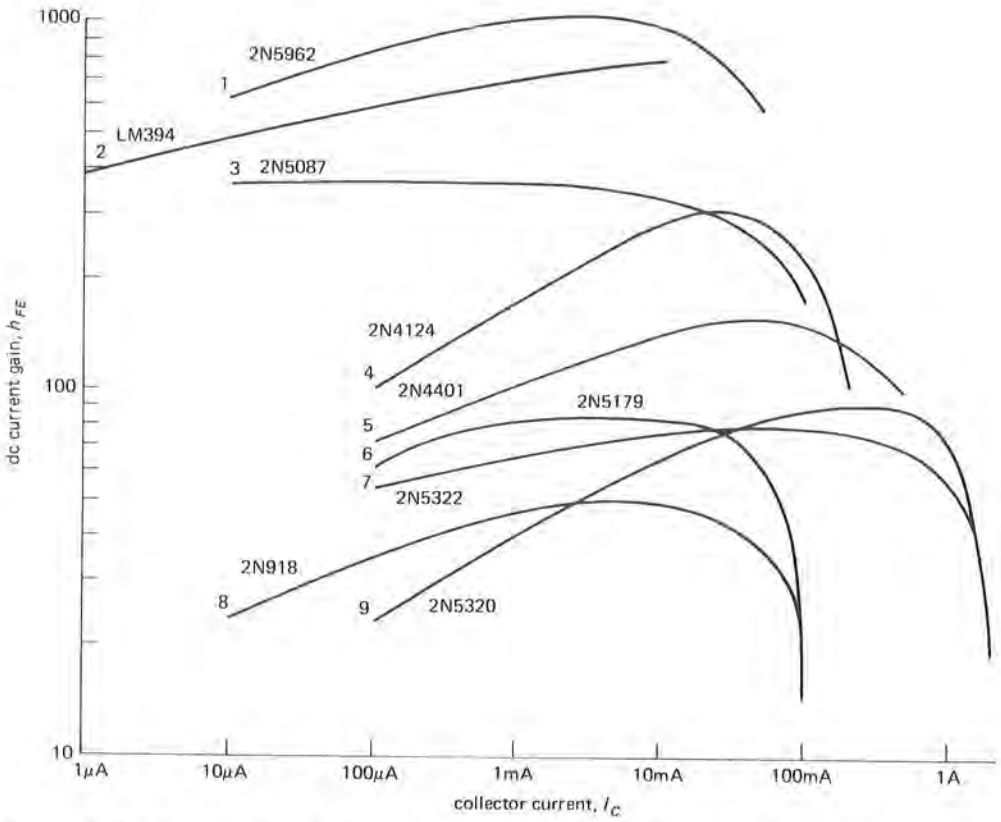


Figure 2.78. Curves of typical transistor current gain, h_{FE}, for a selection of transistors from Table 2.1. These curves are taken from manufacturers' literature. You can expect production spreads of +100%, −50% from the "typical" values graphed.

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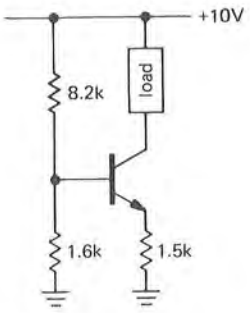


Figure 2.79

2.23 Simple logic with transistors and diodes

Figure 2.77 shows a circuit that performs a task we illustrated in Section 1.32: sounding a buzzer if either car door is open and the driver is seated. In this circuit the transistors all operate as switches (either off or saturated). Diodes D_1 and D_2 form what is called an OR gate, turning off Q_1 if either door is open (switch closed). However, the collector of Q_1 stays near ground, preventing the buzzer from sounding unless switch S_3 is also closed (driver seated); in that case R_2 turns Q_3 on, putting 12 volts across the buzzer. D_3 provides a diode drop so that Q_1 is off with S_1 or S_2 closed, and D_4 protects Q_3 from the buzzer's inductive turn-off transient. In Chapter 8 we will discuss logic circuitry in detail.

Table 2.1 presents a selection of useful and popular small-signal transistors; Figure 2.78 shows corresponding curves of current gain. See also Appendix K.

SELF-EXPLANATORY CIRCUITS

2.24 Good circuits

Figure 2.80 shows a couple of circuit ideas that use transistors.

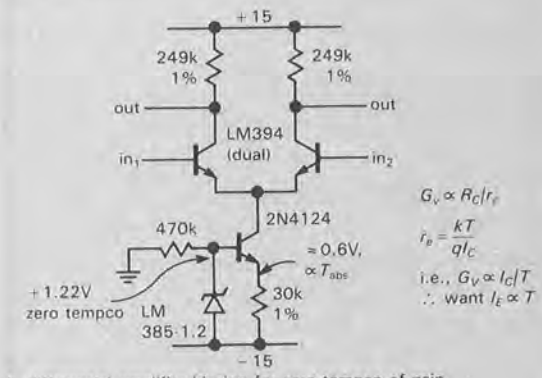
2.25 Bad circuits

A lot can be learned from your own mistakes or someone else's mistakes. In this section we present a gallery of blunders (Fig. 2.81). You can amuse yourself by thinking of variations on these bad circuits, and then avoiding them!

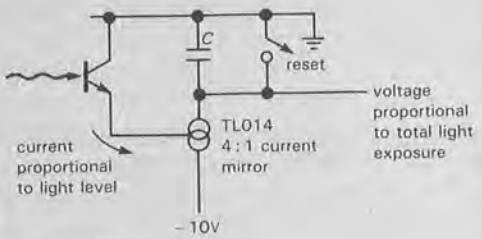
ADDITIONAL EXERCISES

(1) Design a transistor switch circuit that allows you to switch two loads to ground via saturated *npn* transistors. Closing switch A should cause both loads to be powered, whereas closing switch B should power only one load. Hint: Use diodes.

Circuit ideas



A. differential amplifier biasing for zero tempco of gain

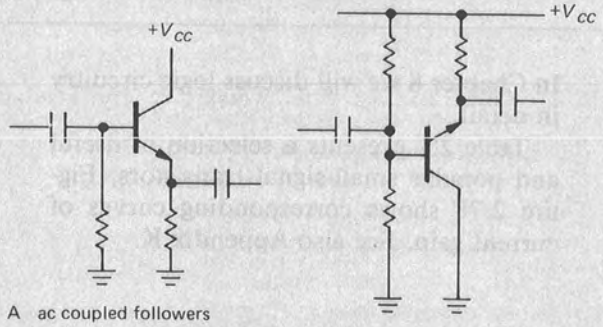


B. light integrator

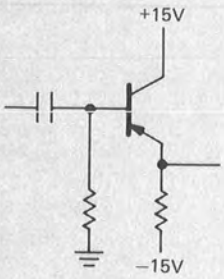
Figure 2.80

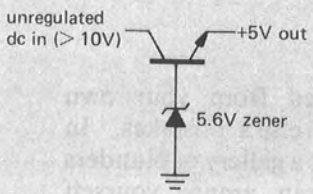
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Bad circuits

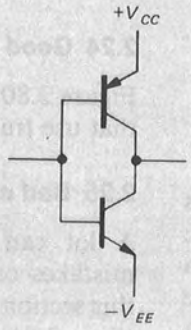


A ac coupled followers

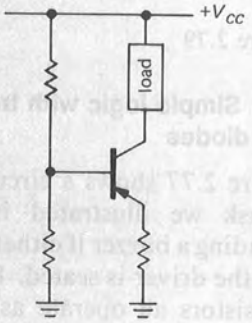




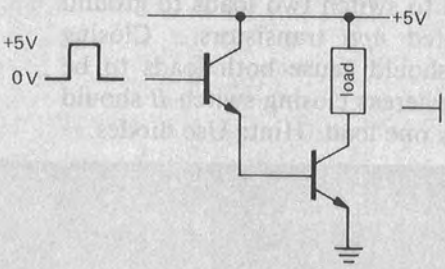
B +5V regulator



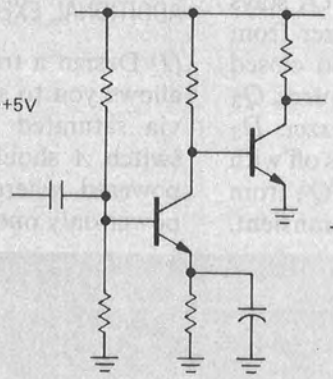
C push-pull follower



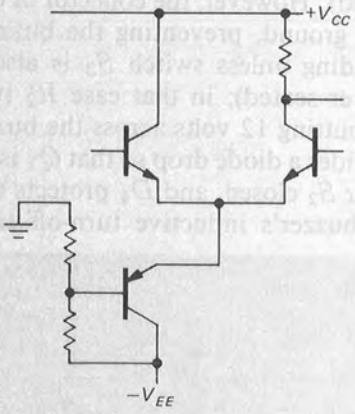
D current source



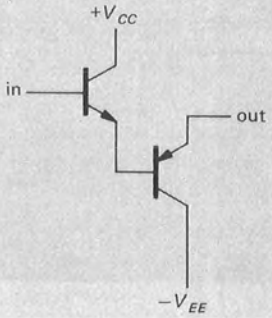
E high-current switch



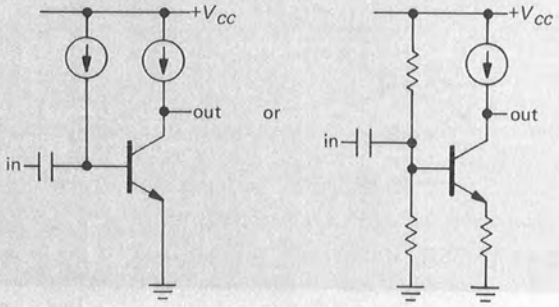
F two-stage amplifier



G differential amplifier



H zero-offset follower



I high-gain ac amplifier

Figure 2.81

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TABLE 2.1. SELECTED SMALL-SIGNAL TRANSISTORS[a]

	V_{CEO} (V)	I_C max (mA)	h_{FE} typ[b]	I_C (mA)	C_{cb} typ[c] (pF)	f_T typ[d] (MHz)	Gain curve	Metal				Plastic	
								TO-5[e]		TO-18[f]		TO-92[h]	
								npn	pnp	npn	pnp	npn	pnp
General purpose	20	500	100	150	16	200		–	–	–	–	–	–
	25	200	200	2	1.8-2.8	300	4	–	–	–	–	4124	4126
	40	200	200	10	1.8-2.8	300		–	–	3947	3251	3904	3906
High gain, low noise	25	50	300	10	2-7	150		–	–	–	–	3391A[h],3707[h]	4058[h]
	25	300	250	50	4	300		–	–	–	–	6008[h]	6009[h]
	25	50	500	5	1.5-4	500		–	–	–	–	5089	–
	40	20	700	1	14	200	2	LM394	–	–	–	–	–
	45	50	1000	10	1.5	300	1	–	–	–	–	5962	–
	50	50	350	5	1.8	400	3	–	–	2848	3965	4967,5210	4965,5087
High current	30-60	600	150	150	5	300	5	2219	2905	2222	2907,3251	4401	4403
	50	1000	100	200	7	450		3725	5022	4014	–	–	–
	60	1000	70	80	15	100		2102,3107	4036	–	–	–	–
	75	2000	70	500	20	60	7,9	5320	5322	–	–	–	–
High voltage	150	600	100	10	3-6	250		–	4929	–	–	5550	5401
	300	1000	50	50	10	50		3439	5416	–	–	–	–
High speed	12	50	80	3	0.7	1500	6	–	–	5179	–	3662[h]	–
	12	100	50	8	1.5	900	8	–	–	918	4208	5770	–
	12	200	75	25	3	500		–	–	2369	2894	5769	5771

[a] all transistors are 2Nxxx numbers, except for the LM394 dual transistor. Devices listed on a single row are similar in characteristics and in some cases are electrically identical. [b] see figure 2.76. [c] at V_{CB}=10V. [d] see figure 13.4. [e] or TO-39. [f] or TO-72, TO-46. [h] TO-92 and its variants have two basic pinouts: EBC and ECB. Transistors with superscript *h* are ECB; all others are EBC.

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(2) Consider the current source in Figure 2.79. ***(a)*** What is I_{load}? What is the output compliance? Assume V_{BE} is 0.6 volt. ***(b)*** If h_{FE} varies from 50 to 100 for collector voltages within the output compliance range, how much will the output current vary? (There are two effects here.) ***(c)*** If V_{BE} varies according to $\Delta V_{BE} = -0.0001\,\Delta V_{CE}$ (Early effect), how much will the load current vary over the compliance range? ***(d)*** What is the temperature coefficient of output current assuming that h_{FE} does not vary with temperature? What is the temperature coefficient of output current assuming that h_{FE} increases from its nominal value of 100 by 0.4%/°C?

(3) Design a common-emitter *npn* amplifier with voltage gain of 15, V_{CC} of +15 volts, and I_C of 0.5mA. Bias the collector at $0.5V_{CC}$, and put the low-frequency 3dB point at 100Hz.

(4) Bootstrap the circuit in the preceding problem in order to raise the input impedance. Choose the rolloff of the bootstrap appropriately.

(5) Design a dc-coupled differential amplifier with voltage gain of 50 (to a single-ended output) for input signals near ground, supply voltages of ±15 volts, and quiescent currents of 0.1mA in each transistor. Use a current source in the emitter and an emitter follower output stage.

(6) In this problem you will ultimately design an amplifier whose gain is controlled by an externally applied voltage (in Chapter 3 you will see how to do the same thing with FETs). ***(a)*** Begin by designing a long-tailed pair differential amplifier with emitter current source and no emitter resistors (undegenerated). Use ±15 volt supplies. Set I_C (each transistor) at 1mA, and use $R_C = 1.0\text{k}$. Calculate the voltage gain from a single-ended input (other input grounded) to a single-ended output. ***(b)*** Now modify the circuit so that an externally applied voltage controls the emitter current source. Give an approximate formula for the gain as a function of controlling voltage. (In a real circuit you might arrange a second set of voltage-controlled current sources to cancel the quiescent-point shift that gain changes produce in this circuit, or a differential-input second stage could be added to your circuit.)

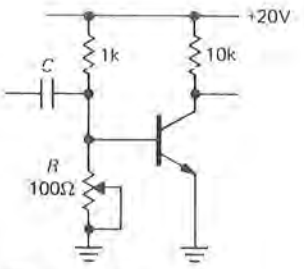


Figure 2.82

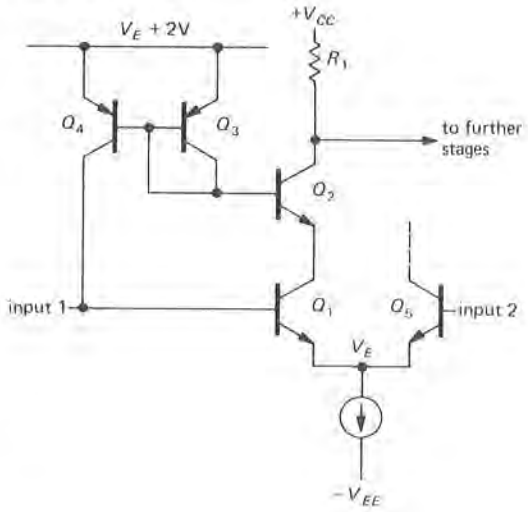


Figure 2.83. Base-current cancellation scheme, commonly used in high-quality operational amplifiers.

(7) Disregarding the lessons of this chapter, a disgruntled student builds the amplifier shown in Figure 2.82. He adjusts R until the quiescent point is $0.5V_{CC}$. ***(a)*** What is Z_{in} (at high frequencies where $Z_C \approx 0$)? ***(b)*** What is the small-signal voltage gain? ***(c)*** What rise in ambient temperature (roughly) will cause the transistor to saturate?

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(8) Several commercially available precision op-amps (e.g., the venerable OP-07 and the recent LT1012) use the circuit in Figure 2.83 to cancel input bias current (only half of the symmetrical-input differential amplifier is shown in detail; the other half works the same way). Explain how the circuit works. Note: Q_1 and Q_2 are a beta-matched pair. Hint: It's all done with mirrors.

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FIELD-EFFECT TRANSISTORS

CHAPTER 3

INTRODUCTION

Field-effect transistors (FETs) are different from the ordinary transistors (sometimes called "bipolar transistors," "bipolar junction transistors," or BJTs, to distinguish them from FETs) that we talked about in the last chapter. Broadly speaking, however, they are similar devices, which we might call *charge-control devices*: In both cases we have a 3-terminal device in which the conduction between two electrodes depends on the availability of charge carriers, which is controlled by a voltage applied to a third *control electrode*.

Here's how they differ: In an *npn* BJT the collector-base junction is back-biased, so no current normally flows. Forward-biasing the base-emitter junction by $\approx$0.6 volts overcomes its diode "contact potential barrier," causing electrons to enter the base region, where they are strongly attracted to the collector; although some base current results, most of these "minority carriers" are captured by the collector. This results in a collector current, controlled by a (smaller) base current. The collector current is proportional to the rate of injection of minority carriers into the base region, which is an exponential function of the *BE* potential difference (the Ebers–Moll equation). You can think of a bipolar transistor as a current amplifier (with roughly constant current gain, h_{FE}) or as a transconductance device (Ebers–Moll).

In a FET, as the name suggests, conduction in a *channel* is controlled by an *electric field*, produced by a voltage applied to the *gate* electrode. There are no forward-biased junctions, so the gate draws no current; this is perhaps the most important advantage of the FET. As with BJTs, there are two polarities, *n-channel* FETs (conduction by electrons) and *p-channel* FETs (conduction by holes). These two polarities are analogous to the familiar *npn* and *pnp* bipolar transistors, respectively. In addition, however, FETs tend to be confusing at first because they can be made with two different kinds of gates (thus JFETs and MOSFETs), and with two different kinds of channel doping (leading to *enhancement* and *depletion* modes). We'll sort out these possibilities shortly.

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First, though, some motivation and perspective: The FET's nonexistent gate current is its most important characteristic. The resulting high input impedance (which can be greater than $10^{14}\Omega$) is essential in many applications, and in any case it makes circuit design simple and fun. For applications like analog switches and amplifiers of ultrahigh input impedance, FETs have no equal. They can be easily used by themselves or combined with bipolar transistors to make integrated circuits: In the next chapter we'll see how successful that process has been in making nearly perfect (and wonderfully easy to use) *operational amplifiers*, and in Chapters 8–11 we'll see how digital electronics has been revolutionized by MOSFET integrated circuits. Because many FETs using very low current can be constructed in a small area, they are especially useful for large-scale integration (LSI) digital circuits such as calculator chips, microprocessors, and memories. In addition, high-current MOSFETs (30A or more) of recent design have been replacing bipolar transistors in many applications, often providing simpler circuits with improved performance.

3.01 FET characteristics

Beginners sometimes become catatonic when directly confronted with the confusing variety of FET types (see, for example, the first edition of this book!), a variety that arises from the combined choices of polarity (*n-channel* or *p-channel*), form of gate insulation (semiconductor *junction* [JFET] or oxide *insulator* [MOSFET]), and channel doping (*enhancement* or *depletion* mode). Of the eight resulting possibilities, six *could* be made, and five actually are. Four of those five are of major importance.

It will aid understanding (and sanity), however, if we begin with one type only, just as we did with the *npn* bipolar transistor. Once comfortable with FETs, we'll have little trouble with their family tree.

FET V–I curves

Let's look first at the n-channel enhancement-mode MOSFET, which is analogous to the *npn* bipolar transistor (Fig. 3.1). In normal operation the drain (~collector) is more positive than the source (~emitter). No current flows from drain to source unless the gate (~base) is brought positive with respect to the source. Once the gate is thus "forward-biased" there will be drain current, all of which flows to the source. Figure 3.2 shows how the drain current I_D varies with drain-source voltage V_{DS}, for a few values of controlling gate-source voltage V_{GS}. For comparison, the corresponding "family" of curves of I_C versus V_{BE} for an ordinary *npn* bipolar transistor is shown. Obviously threre are a lot of similarities between n-channel MOSFETs and *npn* bipolar transistors.

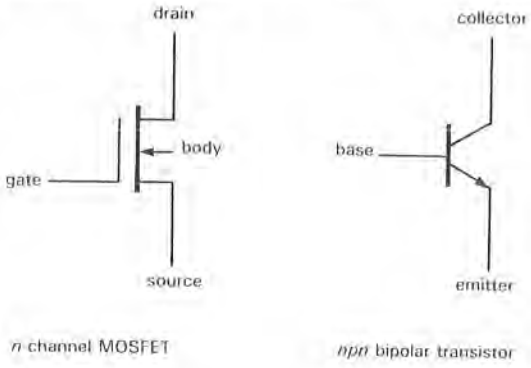


Figure 3.1

Like the *npn* transistor, the FET has a high incremental drain impedance, giving roughly constant current for V_{DS} greater than a volt or two. By an unfortunate choice of language, this is called the "saturation" region of the FET and corresponds to the "active" region of the bipolar transistor. Analogous to the bipolar transistor, larger gate-to-source bias produces larger drain current. If anything, FETs behave more nearly like ideal transconductance devices (constant drain current for constant gate-source voltage) than do bipolar

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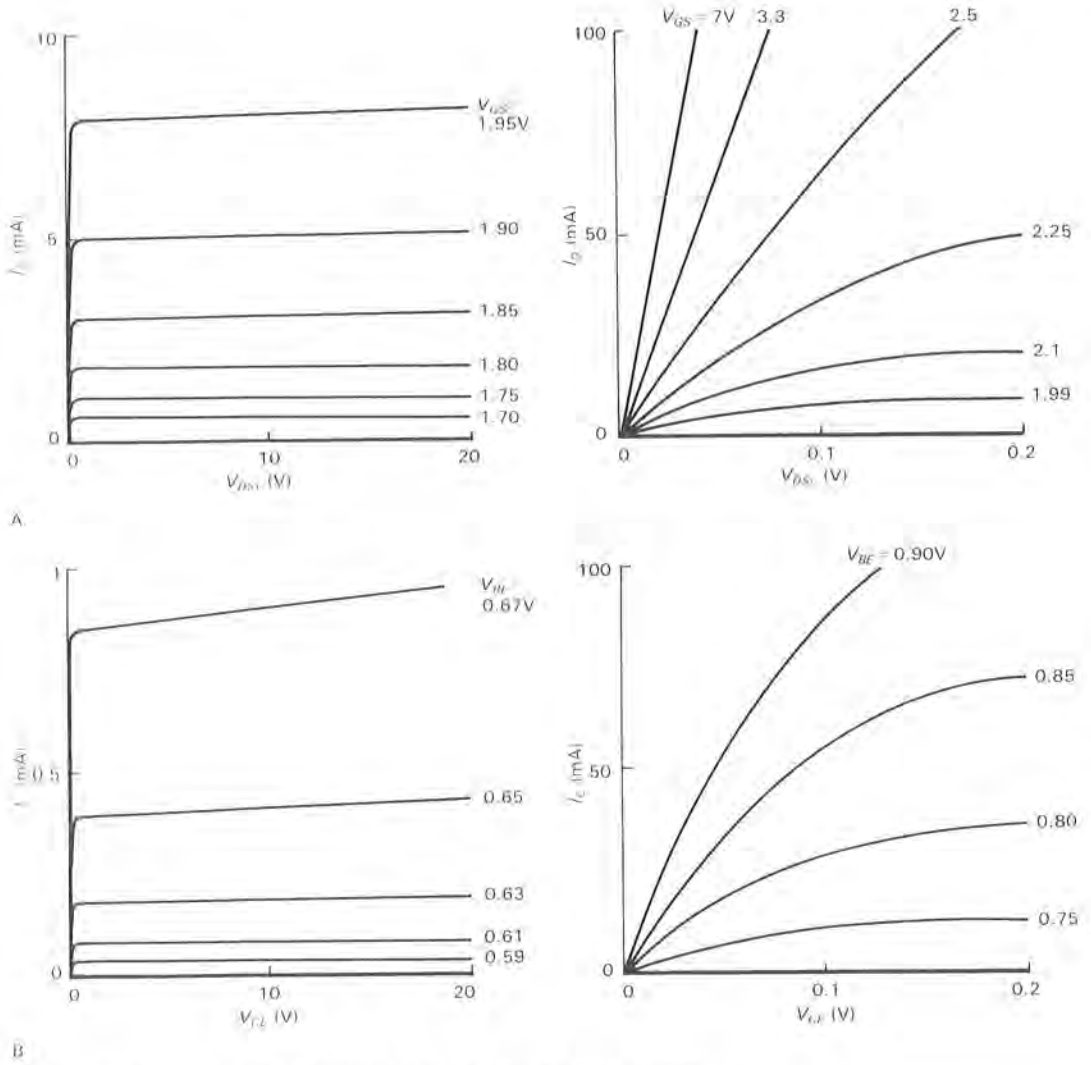


Figure 3.2. Measured MOSFET/transistor characteristic curves.
A. VN0106 n-channel MOSFET: I_D versus V_{DS} for various values of V_{GS}.
B. 2N3904 *npn* bipolar transistor: I_C versus V_{CE} for various values of V_{BE}.

transistors; the Ebers-Moll equation predicts perfect transconductance characteristics for bipolar transistors, but that ideal behavior is degraded by the Early effect (Section 2.10).

So far, the FET looks just like the *npn* transistor. Let's look closer, though. For one thing, over the normal range of currents the saturation drain current increases rather modestly with increasing gate voltage (V_{GS}). In fact, it is proportional to $(V_{GS}-V_T)^2$, where V_T is the "gate threshold voltage" at which drain current begins ($V_T \approx 1.63$V for the FET in Fig. 3.2); compare this mild quadratic law with the steep exponential transistor law, as given to us by Ebers and Moll. Second, there is *zero* dc gate current, so you mustn't think of the FET as a device with current gain (which would be infinite). Instead, think

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of the FET as a transconductance device, with gate-source voltage programming the drain current, as we did with the bipolar transistor in the Ebers-Moll treatment; recall that the transconductance g_m is simply the ratio i_d/v_{gs} (recall the convention of using lower-case letters to indicate "small-signal" changes in a parameter; e.g., $i_d/v_{gs} = \delta I_d/\delta V_{gs}$). Third, the gate of a MOSFET is truly insulated from the drain-source channel; thus, unlike the situation for bipolar transistors (or JFETs, as we'll see), you can bring it positive (or negative) at least 10 volts or more without worrying about diode conduction. Finally, the FET differs from the bipolar transistor in the so-called linear region of the graph, where it behaves rather accurately like a resistor, *even for negative* V_{DS}; this turns out to be quite useful because the equivalent drain-source resistance is, as you might guess, programmed by the gate-source voltage.

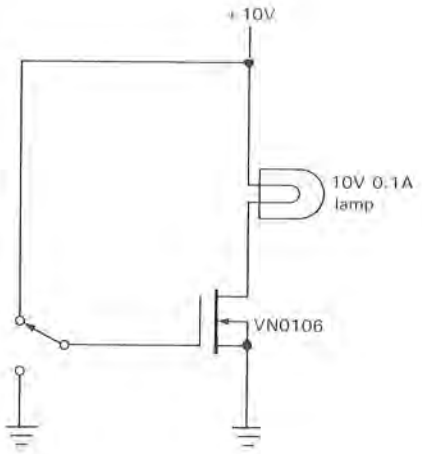


Figure 3.3. MOSFET switch.

Two examples

FETs have more surprises in store for us. Before getting into more details, though, let's look at two simple switching applications. Figure 3.3 shows the MOSFET equivalent of Figure 2.3, our first saturated transistor switch. The FET circuit is even simpler, because we don't have to concern ourselves with the inevitable compromise of providing adequate base drive current (considering worst-case minimum h_{FE} combined with the lamp's cold resistance) without squandering excessive power. Instead, we just apply a full-swing dc voltage drive to the cooperative high-impedance gate. As long as the switched-on FET behaves like a resistance small compared with the load, it will bring its drain close to ground; typical power MOSFETs have $R_{ON} < 0.2$ ohm, which is fine for this job.

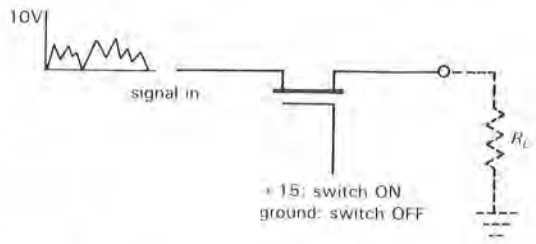


Figure 3.4

Figure 3.4 shows an "analog switch" application, which cannot be done at all with bipolar transistors. The idea here is to switch the conduction of a FET from open-circuit (gate reverse-biased) to short-circuit (gate forward-biased), thus blocking or passing the analog signal (we'll see plenty of reasons to do this sort of thing later). In this case we just arrange for the gate to be driven more negative than any input signal swing (switch *open*), or a few volts more positive than any input signal swing (switch *closed*). Bipolar transistors aren't suited to this application, because the base draws current and forms diodes with the emitter and collector, producing awkward clamping action. The MOSFET is delightfully simple by comparison, needing only a voltage swing into the (essentially open-circuit) gate. Warning:

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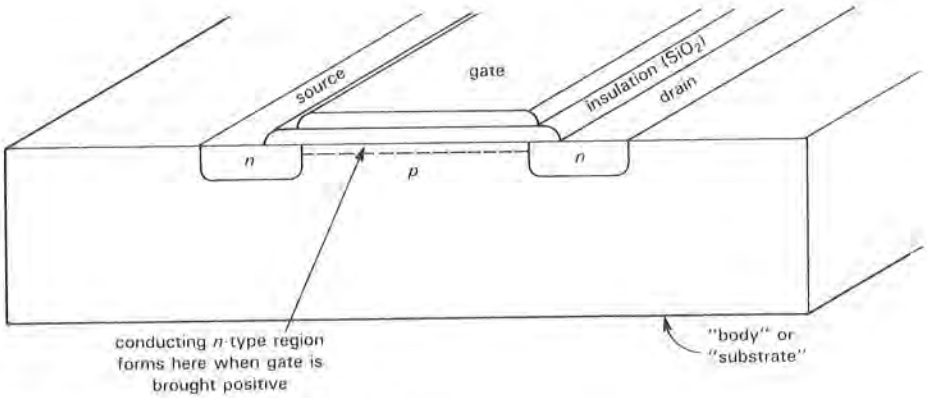


Figure 3.5. An n-channel MOSFET.

It's only fair to mention that our treatment of this circuit has been somewhat simplistic, for instance ignoring the effects of gate-channel capacitance and the variation of R_{ON} with signal swing. We'll have more to say about analog switches later.

3.02 FET types

n-channel, p-channel

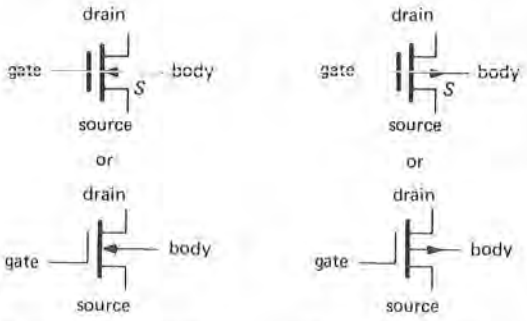
Now for the family tree. First of all, FETs (like BJTs) can be fabricated in both polarities. Thus, the mirror twin of our n-channel MOSFET is a *p-channel* MOSFET. Its behavior is symmetrical, mimicking *pnp* transistors: The drain is normally negative with respect to the source, and drain current flows if the gate is brought at least a volt or two negative with respect to the source. The symmetry isn't perfect because the carriers are holes, rather than electrons, with lower "mobility" and "minority carrier lifetime." These are semiconductor parameters of importance in transistor performance. The consequence is worth remembering – p-channel FETs usually have poorer performance, manifested as higher gate threshold voltage, higher R_{ON}, and lower saturation current.

MOSFET, JFET

In a MOSFET ("Metal-Oxide-Semiconductor Field-Effect Transistor") the gate region is separated from the conducting channel by a thin layer of SiO_2 (glass) grown onto the channel (Fig. 3.5). The gate, which may be either metal or doped silicon, is truly insulated from the source-drain circuit, with characteristic input resistance $>10^{14}$ ohms. It affects channel conduction purely by its electric field. MOSFETs are sometimes called *insulated-gate* FETs, or IGFETs. The gate insulating layer is quite thin, typically less than a wavelength of light, and can withstand gate voltages up to ± 20 volts or more. MOSFETs are easy to use because the gate can swing either polarity relative to the source without any gate current flowing. They are, however, quite susceptible to damage from static electricity; you can destroy a MOSFET device literally by touching it.

The symbols for MOSFETs are shown in Figure 3.6. The extra terminal is the "body," or "substrate," the piece of silicon in which the FET is fabricated (see Fig. 3.5). Because the body forms a diode junction with the channel, it must be held at a nonconducting voltage. It can be tied to the source, or to a point in the

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A. n-channel MOSFET B. p-channel MOSFET

Figure 3.6

circuit more negative (positive) than the source for n-channel (p-channel) MOSFETs. It is common to see the body terminal omitted; furthermore, engineers often use the symbol with the symmetrical gate. Unfortunately, with what's left you can't tell source from drain; worse still, you can't tell n-channel from p-channel! We will use the lower set of schematic symbols exclusively in this book to avoid confusion, although we will often leave the body pin unconnected.

In a JFET ("Junction Field-Effect Transistor") the gate forms a semiconductor junction with the underlying channel. This has the important consequence that *a JFET gate should not be forward biased with respect to the channel, to prevent gate current*. For example, diode conduction will occur as the gate of an n-channel JFET approaches +0.6 volt with respect to the more negative end of the channel (which is usually the source). The gate is therefore operated reverse-biased with respect to the channel, and no current (except diode leakage) flows in the gate circuit. The circuit symbols for JFETs are shown in Figure 3.7. Once again, we favor the symbol with offset gate, to identify the source. As we'll see later, FETs (both JFET and MOSFET) are nearly symmetrical, but the gate-drain capacitance is usually designed to be less than the gate-source capacitance, making the drain the preferred output terminal.

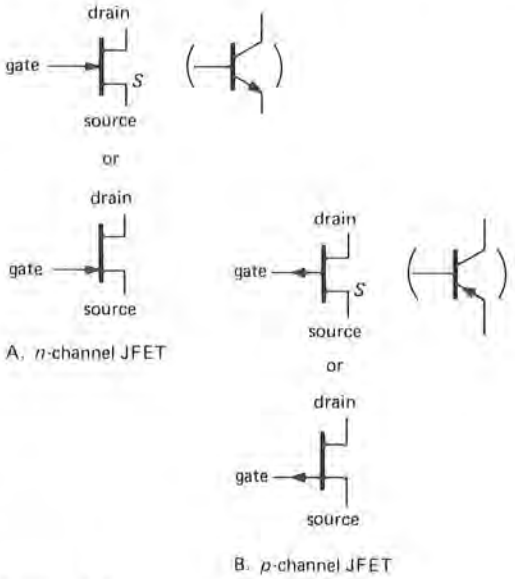


Figure 3.7

Enhancement, depletion

The n-channel MOSFETs with which we began the chapter were nonconducting, with zero (or negative) gate bias, and were driven into conduction by bringing the gate positive with respect to the source. This kind of FET is known as *enhancement mode*. The other possibility is to manufacture the n-channel FET with the channel semiconductor "doped" so that there is plenty of channel conduction even with zero gate bias, and the gate must be reverse-biased a few volts to cut off the drain current. Such a FET is known as *depletion mode*. MOSFETs can be made in either variety, since there is no restriction on gate polarity. But JFETs permit only reverse gate bias and therefore can be made only in depletion mode.

A graph of drain current versus gate-source voltage, at a fixed value of drain voltage, may help clarify this distinction (Fig. 3.8). The enhancement-mode device draws no drain current until the gate

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is brought positive (these are n-channel FETs) with respect to the source, whereas the depletion-mode device is operating at nearly its maximum value of drain current when the gate is at the same voltage as the source. In some sense the two categories are artificial, because the two curves are identical except for a shift along the V_{GS} axis. In fact, it is possible to manufacture "in-between" MOSFETs. Nevertheless, the distinction is an important one when it comes to circuit design.

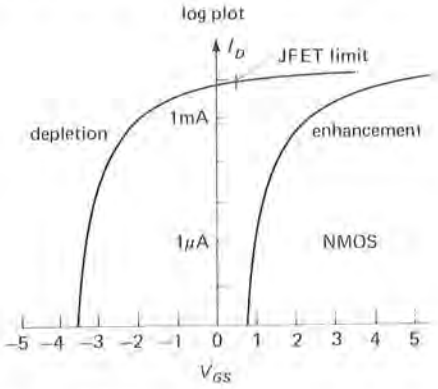


Figure 3.8

Note that JFETs are always depletion-mode devices and that the gate cannot be brought more than about 0.5 volt more positive (for n-channel) than the source, since the gate-channel diode will conduct. MOSFETs *could* be either enhancement or depletion, but in practice you rarely see depletion-mode MOSFETs (the exceptions being n-channel GaAs FETs and "dual-gate" cascodes for radiofrequency applications). For all practical purposes, then, you have to worry only about (a) depletion-mode JFETs and (b) enhancement-mode MOSFETs; they both come in the two polarities, n-channel and p-channel.

3.03 Universal FET characteristics

A family tree (Fig. 3.9) and a map (Fig. 3.10) of input/output voltage (source grounded) may help simplify things. The different devices (including garden-variety *npn* and *pnp* bipolar transistors) are drawn in the quadrant that characterizes their input and output voltages when they are in the active region with source (or emitter) grounded. You don't have to remember the properties of the five kinds of FETs, though, because they're all basically the same.

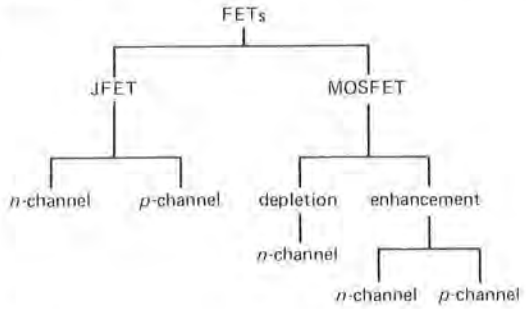


Figure 3.9

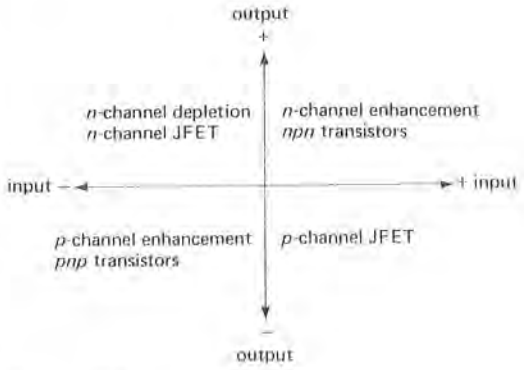


Figure 3.10

First, with the source grounded, a FET is turned on (brought into conduction) by bringing the gate voltage "toward" the active drain supply voltage. This is true for all five types of FETs, as well as the bipolar transistors. For example, an n-channel JFET (which is automatically depletion-mode) uses a positive drain supply, as do all n-type devices. Thus a positive-going gate voltage tends to turn on the JFET.

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The subtlety for depletion-mode devices is that the gate must be (negatively) back-biased for zero drain current, whereas for enhancement-mode devices zero gate voltage is sufficient to give zero drain current.

Second, because of the near symmetry of source and drain, either terminal can act as the effective source (exception: not true for power MOSFETs, where the body is internally connected to the source). When thinking of FET action, and for purposes of calculation, the effective source terminal is always the one most "away" from the active drain supply. For example, suppose a FET is used to switch a line to ground, and both positive and negative signals are present on the switched line, which is usually selected to be the FET drain. If the switch is an n-channel MOSFET (therefore enhancement), and a negative voltage happens to be present on the (turned-off) drain terminal, then that terminal is actually the "source" for purposes of gate turn-on voltage calculation. Thus a negative gate voltage larger than the most negative signal, rather than ground, is needed to ensure turn-off.

The graph in Figure 3.11 may help you sort out all these confusing ideas. Again, the difference between enhancement and depletion is merely a question of displacement along the V_{GS} axis – i.e., whether there is a lot of drain current or no drain current at all when the gate is at the same potential as the source. The n-channel and p-channel FETs are complementary in the same way as *npn* and *pnp* bipolar transistors.

In Figure 3.11 we have used standard symbols for the important FET parameters of saturation current and cutoff voltage. For JFETs the value of drain current with gate shorted to source is specified on the data sheets as I_{DSS} and is nearly the maximum drain current possible. (I_{DSS} means current from *d*rain to *s*ource with the gate *s*horted to the source. Throughout the chapter you will see this notation, in which the first two subscripted letters designate the pair of terminals, and the third specifies the condition.) For enhancement-mode MOSFETs the analogous specification is $I_{D(ON)}$, given at some forward gate voltage ("I_{DSS}" would be zero for any enhancement-mode device).

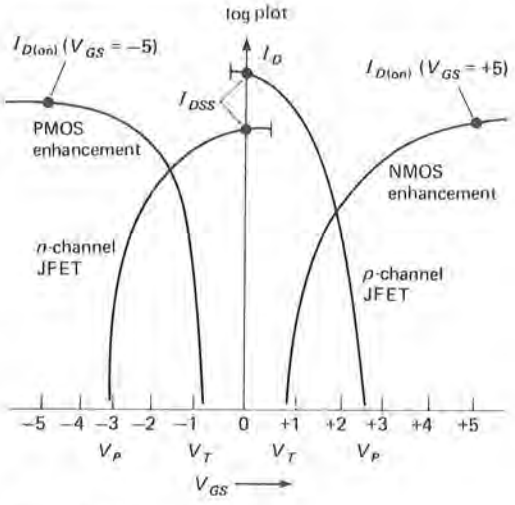


Figure 3.11

For JFETs the gate-source voltage at which drain current approaches zero is called the "gate-source cutoff voltage," $V_{GS(OFF)}$, or the "pinch-off voltage," V_P, and is typically in the range of -3 to -10 volts (positive for p-channel, of course). For enhancement-mode MOSFETs the analogous quantity is the "threshold voltage," V_T (or $V_{GS(th)}$), the gate-source voltage at which drain current begins to flow. V_T is typically in the range of 0.5 to 5 volts, in the "forward" direction, of course. Incidentally, don't confuse the MOSFET V_T with the V_T in the Ebers-Moll equation that describes bipolar transistor collector current; they have nothing to do with each other.

With FETs it is easy to get confused about polarities. For example, n-channel devices, which usually have the drain

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positive with respect to the source, can have positive or negative gate voltage, and positive (enhancement) or negative (depletion) threshold voltages. To make matters worse, the drain can be (and often is) operated negative with respect to the source. Of course, all these statements go in reverse for p-channel devices. In order to minimize confusion, we will always assume n-channel devices unless explicitly stated otherwise. Likewise, because MOSFETs are nearly always enhancement-mode, and JFETs are always depletion-mode, we'll omit those designations from now on.

3.04 FET drain characteristics

In Figure 3.2 we showed a family of curves of I_D versus V_{DS} that we measured for a VN0106, an n-channel enhancement-mode MOSFET. (The VN01 comes in various voltage ratings, indicated by the last two digits of the part number. For example, a VN0106 is rated at 60V.) We remarked that FETs behave like pretty good transconductance devices over most of the graph (i.e., I_D nearly constant for a given V_{GS}), except at small V_{DS}, where they approximate a resistance (i.e., I_D proportional to V_{DS}). In both cases the applied gate-source voltage controls the behavior, which can be well described by the FET analog of the Ebers-Moll equation. Let's look at these two regions a bit more closely.

Figure 3.12 shows the situation schematically. In both regions the drain current depends on $V_{GS} - V_T$, the amount by which the applied gate-source voltage exceeds the threshold (or pinch-off) voltage. The linear region, in which drain current is approximately proportional to V_{DS}, extends up to a voltage $V_{DS(\text{sat})}$, after which the drain current is approximately constant. The slope in the linear region, I_D/V_{DS}, is proportional to the gate bias, $V_{GS} - V_T$. Furthermore, the drain voltage at which the curves enter the "saturation region," $V_{DS(\text{sat})}$, equals $V_{GS} - V_T$, making the saturation drain current, $I_{D(\text{sat})}$, proportional to $(V_{GS} - V_T)^2$, the quadratic law we mentioned earlier. For reference, here are the universal FET drain-current formulas:

$$I_D = 2k[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2] \quad \text{(linear region)}$$

$$I_D = k(V_{GS} - V_T)^2 \quad \text{(saturation region)}$$

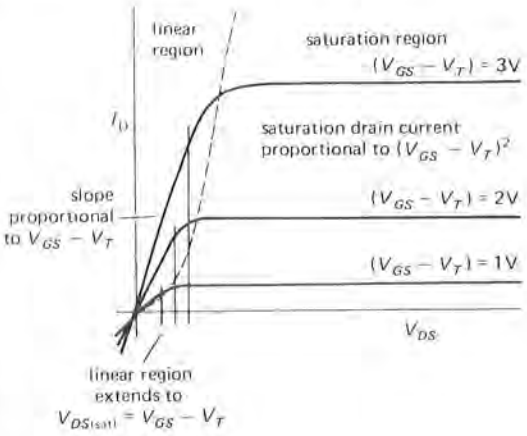


Figure 3.12

If we call $V_{GS} - V_T$ (the amount by which the gate-source voltage exceeds the threshold) the "gate drive," the important results are that (a) the resistance in the linear region is inversely proportional to gate drive, (b) the linear region extends to a voltage equal to the gate drive, and (c) saturation drain current is proportional to the square of the gate drive. These equations assume that the body is connected to the source. Note that the "linear region" is not really linear, because of the V_{DS}^2 term; we'll show a clever circuit fix later.

The scale factor k depends on particulars such as the geometry of the FET, oxide capacitance, and carrier mobility. It has a temperature dependence $k \propto T^{-3/2}$, which alone would cause I_D to decrease

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with increasing temperature. However, V_T also depends slightly on temperature (2–5mV/°C); the combined effect produces the curve of drain current versus temperature shown in Figure 3.13.

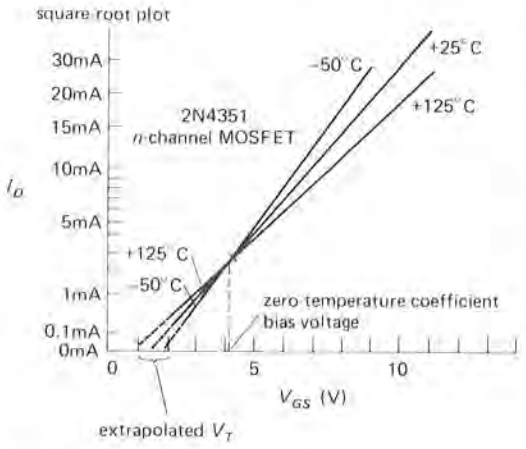


Figure 3.13

At large drain currents the negative temperature coefficient of k causes the drain current to decrease with increasing temperature – goodbye thermal runaway! As a consequence, FETs of a given type can be paralleled without the external current-equalizing ("emitter-ballasting") resistors that you must use with bipolar transistors (see Section 6.07). This same negative coefficient also prevents thermal runaway in local regions of the junction (an effect known as "current hogging"), which severely limits the power capability of large bipolar transistors, as we'll see when we discuss "second breakdown" and "safe operating area" in Chapter 6.

At small drain currents (where the temperature coefficient of V_T dominates), I_D has a positive tempco, with a point of zero temperature coefficient at some drain current in between. This effect is exploited in FET op-amps to minimize temperature drift, as we'll see in the next chapter.

Subthreshold region

Our expression given earlier for saturation drain current does not apply for very small drain currents. This is known as the "subthreshold" region, where the channel is below the threshold for conduction, but some current flows anyway because of a small population of thermally energetic electrons. If you've studied physics or chemistry, you probably know in your bones that the resulting current is exponential:

$$I_D = k \exp(V_{GS} - V_T)$$

We measured some MOSFETs over 9 decades of drain current (1nA to 1A) and plotted the result as a graph of I_D versus V_{GS} (Fig. 3.14). The region from 1nA to 1mA is quite precisely exponential; above this subthreshold region the curves enter the normal saturation region. For the n-channel MOSFET (type VN01) we checked out a sample of 20 transistors (from four different manufacturing runs spread over 2 years), plotting the extreme range to give you an idea of the variability (see next section). Note the somewhat poorer characteristics (V_T, $I_{D(ON)}$) of the "complementary" VP01.

3.05 Manufacturing spread of FET characteristics

Before we look at some circuits, let's take a look at the range of FET parameters (such as I_{DSS} and V_T), as well as their manufacturing "spread" among devices of the same nominal type, in order to get a better idea of the FET. Unfortunately, many of the characteristics of FETs show much greater process spread than the corresponding characteristics of bipolar transistors, a fact that the designer must keep in mind. For example, the VN01 (a typical n-channel MOSFET) has a specified V_T of 0.8 to 2.4 volts (I_D = 1mA), compared with the analogous V_{BE} spread of

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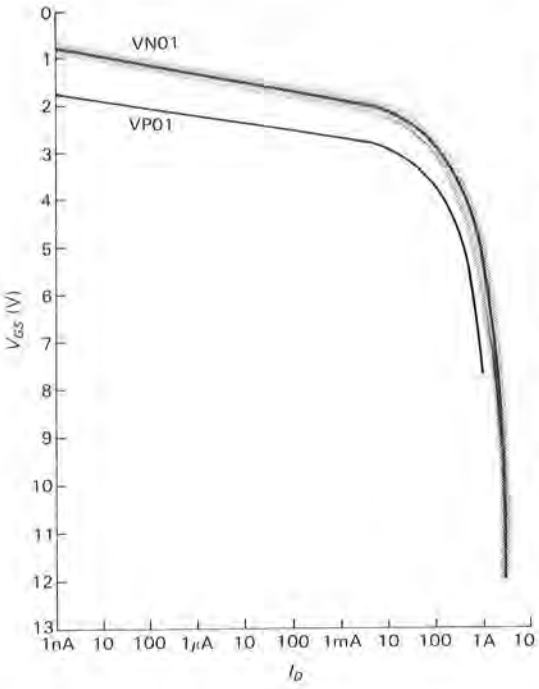


Figure 3.14. Measured MOSFET drain current versus gate-source voltage.

0.63 to 0.83 volt (also at $I_C = 1$mA) for an *npn* bipolar transistor. Here's what you can expect:

Characteristic	*Available range*	*Spread*
I_{DSS}, $I_{D(ON)}$	1mA to 100A	×5
$R_{DS(ON)}$	0.05Ω to 10k	×5
g_m @ 1mA	500–3000μS	×5
V_P (JFETs)	0.5–10V	5V
V_T (MOSFETs)	0.5–5V	2V
$BV_{DS(OFF)}$	6–1000V	
$BV_{GS(OFF)}$	6–125V	

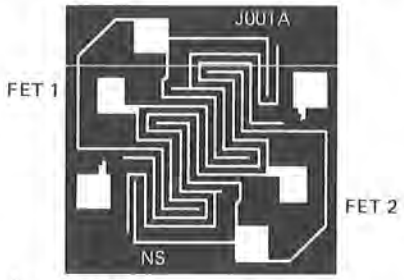
$R_{D(ON)}$ is the drain-source resistance (linear region, i.e., small V_{DS}) when the FET is conducting fully, e.g., with the gate grounded in the case of JFETs or with a large applied gate-source voltage (usually specified as 10V) for MOSFETs. I_{DSS} and $I_{D(ON)}$ are the saturation-region (large V_{DS}) drain currents under the same turned-on gate drive conditions. V_P is the pinch-off voltage (JFETs), V_T is the turn-on gate threshold voltage (MOSFETs), and the BVs are breakdown voltages. As you can see, a JFET with grounded source may be a good current source, but you can't predict very well what the current will be. Likewise, the V_{GS} needed to produce some value of drain current can vary considerably, in contrast to the predictable (≈0.6V) V_{BE} of bipolar transistors.

Matching of characteristics

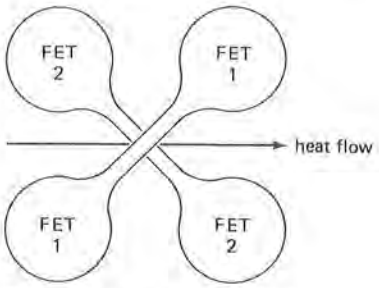
As you can see, FETs are inferior to bipolar transistors in V_{GS} predictability, i.e., they have a large spread in the V_{GS} required to produce a given I_D. Devices with a large process spread will, in general, have larger offset (voltage unbalance) when used as differential pairs. For instance, typical run-of-the-mill bipolar transistors might show a spread in V_{BE} of 50mV or so, at some collector current, for a selection of off-the-shelf transistors. The comparable figure for MOSFETs is more like 1 volt! Because FETs have some very desirable characteristics otherwise, it is worthwhile putting in some extra effort to reduce these offsets in specially manufactured matched pairs. IC designers use techniques like interdigitation (two devices sharing the same general piece of IC real estate) and thermal-gradient cancellation schemes to improve performance (Fig. 3.15).

The results are impressive. Although FET devices still cannot equal bipolar transistors in V_{GS} matching, their performance is adequate for most applications. For example, the best available matched FET has a voltage offset of 0.5mV and tempco of 5μV/°C (max), whereas the best bipolar pair has values of 25μV and 0.6μV/°C (max), roughly 10 times better. Operational amplifiers (the universal high-gain differential amplifiers we'll see in the next chapter) are available in both flavors; you would generally choose one with bipolar innards for high precision (because of its

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A. interdigitation



B. temperature-gradient cancellation

Figure 3.15

close input-transistor V_{BE} matching), whereas a FET-input op-amp is the obvious choice for high-impedance applications (because its inputs – FET gates – draw no current). For example, the inexpensive JFET-input LF411 that we will use as our all-around op-amp in the next chapter has a typical input current of 50pA and costs $0.60; the popular MOSFET-input TLC272 costs about the same and has a typical input current of only 1pA! Compare this with a common bipolar op-amp, the μA741, with typical input current of 80,000pA (80nA).

Tables 3.1–3.3 list a selection of typical JFETs (both single and dual) and small-signal MOSFETs. Power MOSFETs, which we will discuss in Section 3.14, are listed in Table 3.5.

BASIC FET CIRCUITS

Now we're ready to look at FET circuits. You can usually find a way to convert a circuit that uses BJTs into one using FETs. However, the new circuit may not be an improvement! For the remainder of the chapter we'd like to illustrate circuit situations that take advantage of the unique properties of FETs, i.e., circuits that work better with FETs, or that you can't build at all with bipolar transistors. For this purpose it may be helpful to group FET applications into categories; here are the most important, as we see it:

High-impedance/low-current. Buffers or amplifiers for applications where the base current and finite input impedance of BJTs limit performance. Although you *can* build such circuits with discrete FETs, current practice favors using integrated circuits built with FETs. Some of these use FETs as a high-impedance front-end for an otherwise bipolar design, whereas others use FETs throughout.

Analog switches. MOSFETs are excellent voltage-controlled analog switches, as we hinted in Section 3.01. We'll look briefly at this subject. Once again, you should generally use dedicated "analog switch" ICs, rather than building discrete circuits.

Digital logic. MOSFETs dominate microprocessors, memory, and most high-performance digital logic. They are used exclusively in micropower logic. Here, too, MOSFETs make their appearance in integrated circuits. We'll see why FETs are preferable to BJTs.

Power switching. Power MOSFETs are often preferable to ordinary bipolar power transistors for switching loads, as we suggested in our first circuit of the chapter. For this application you use *discrete* power FETs.

Variable resistors; current sources. In the "linear" region of the drain curves, FETs behave like voltage-controlled resistors; in the "saturation" region they are voltage-controlled current sources. You can exploit this intrinsic behavior of FETs in your circuits.

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TABLE 3.1. JFETs

Type	BV_{GSS} (V)	I_{DSS} min (mA)	I_{DSS} max (mA)	$V_{GS(OFF)}, V_P$ min (V)	$V_{GS(OFF)}, V_P$ max (V)	C_{iss} max (pF)	C_{rss} max (pF)	Comments
n-channel								
2N4117A-	40	0.03	0.09	0.6	1.8	3	1.5	low leakage: 1pA (max)
2N4119A	40	0.24	0.6	2	6	4	1.5	
2N4338	50	0.2	0.6	0.3	1	6	2	0.5fA/√Hz @ 100Hz
2N4416	30	5	15	2.5	6	4	0.8	VHF low noise: <2dB@100MHz
2N4867A-	40	0.4	1.2	0.7	2	25	5	low freq, low noise:
2N4869A	40	2.5	7.5	1.8	5	25	5	10nV/√Hz(max)@10Hz
2N5265-	60	0.5	1	–	3	7	2	series of 6, tight I_{DSS} spec;
2N5270	60	7	14	–	8	7	2	2N5358-64 p-chan complement
2N5432	25	150	–	4	10	30	15	switch: R_{ON}=5Ω(max)
2N5457-	25	1	5	0.5	6	7	3	general purpose;
2N5459	25	4	16	2	8	7	3	2N5460-2 p-chan complement
2N5484-	25	1	5	0.3	3	5	1	low noise RF; inexpensive
2N5486	25	8	20	2	6	5	1	
2SK117	50	0.6	14	0.2	1.5	13[t]	3[t]	ultra low noise: 1nV/√Hz
2SK147	40	5	30	0.3	1.2	75[t]	15[t]	ultra low noise: 0.7nV/√Hz
p-channel								
2N5114	30	30	90	5	10	25	7	switch: R_{ON}=75Ω(max)
2N5358-	40	0.5	1	0.5	3	6	2	series of 7, tight I_{DSS} spec;
2N5364	40	9	18	2.5	8	6	2	2N5265-70 n-chan complement
2N5460-	40	1	5	0.75	6	7	2	general purpose;
2N5462	40	4	16	1.8	9	7	2	2N5457-9 n-chan complement
2SJ72	25	5	30	0.3	2	185[t]	55[t]	ultra low noise: 0.7nV/√Hz

[t] typical.

Generalized replacement for bipolar transistors. You can use FETs in oscillators, amplifiers, voltage regulators, and radio-frequency circuits (to name a few), where bipolar transistors are also normally used. FETs aren't *guaranteed* to make a better circuit – sometimes they will, sometimes they won't. You should keep them in mind as an alternative.

Now let's look at these subjects. We'll adopt a slightly different order, for clarity.

3.06 JFET current sources

JFETs are used as current sources within integrated circuits (particularly op-amps), and also sometimes in discrete designs. The simplest JFET current source is shown in Figure 3.16; we chose a JFET, rather than a MOSFET, because it needs no gate bias (it's depletion mode). From a graph of FET drain characteristics (Fig. 3.17) you can see that the current will be reasonably

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TABLE 3.2. SELECTED MOSFETs

Type	Mfg[a]	Gate protect	$R_{DS(on)}$ max @V_{GS} (Ω)	(V)	$V_{GS(th)}$ min (V)	$V_{GS(th)}$ max (V)	$I_{D(on)}$ (V_{DS}=10V) min (mA)	C_{rss} max (pF)	BV_{DS} (V)	BV_{GS} (V)	I_{GSS} (nA)	Comments
n-channel												
3SK38A	TO	•	500	3	–	–	10	2.5	20	12	25	
3N170	IL	–	200	10	1.0	2	10	1.3	25	35	0.01	
SD210	SI	–	45	10	0.5	2	–	0.5	30	40	0.1	low R_{ON}
SD211	SI	•	45	10	0.5	2	–	0.5	30	15	10	low R_{ON}
VN1310	ST	–	8	10	0.8	2.4	500	5	100	20	0.1	small VMOS; D-S diode
IT1750	IL	–	50	20	0.5	3	10	1.6	25	25	0.01	
VN2222L	SI	–	8	5	0.6	2.5	750	5	60	40	0.1	small VMOS; D-S diode
CD3600	RC	•	500	10	1.5[t]	–	1.3	0.4	15	15	0.01	equiv to 4007 array
2N3796	MO	–	–	–	-4	–	14	0.8	25	10	0.001	depletion; I_{DSS}=1.5mA
2N4351	MO+	–	300	10	1.5	5	3	2.5	25	35	0.01	popular
p-channel												
3N163	IL	–	250	20	2	5	5	0.7	40	40	0.01	
VP1310	ST	–	25	10	1.5	3.5	250	5	100	20	0.1	small VMOS; D-S diode
IT1700	IL	–	400	10	2	5	2	1.2	40	40	0.01	
CD3600	RC	•	500	10	1.8[t]	–	1.3	0.8	15	15	0.02	equiv to 4007 array
2N4352	MO+	–	600	10	1.5	6	2	2.5	25	35	0.01	popular
3N172	IL	•	250	20	2	5	5	1	40	40	0.2	popular

[a] see footnotes to Table 4.1. [t] typical.

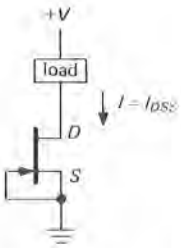


Figure 3.16

constant for V_{DS} larger than a couple of volts. However, because of I_{DSS} spread, the current is unpredictable. For example, the 2N5484 (a typical n-channel JFET) has a specified I_{DSS} of 1mA to 5mA. Still, the circuit is attractive because of the simplicity of a two-terminal constant-current device. If that appeals to you, you're in luck. You can buy "current-regulator diodes" that are nothing more than JFETs with gate tied to source, sorted according to current. They're the current analog of a zener (voltage regulator) diode. Here are the characteristics of the 1N5283–1N5314 series:

Currents available	0.22mA to 4.7mA
Tolerance	10%
Temperature coefficient	±0.4%/°C
Voltage range	1V–2.5V min, 100V max
Current regulation	5% typical
Impedance	1M typical (for 1mA device)

We plotted I versus V for a 1N5294 (rated at 0.75mA); Figure 3.18A shows

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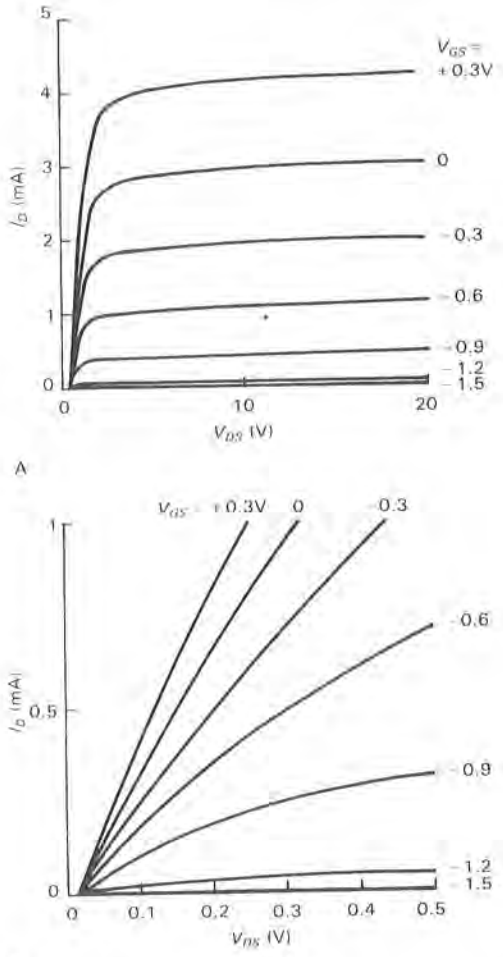


Figure 3.17. Measured JFET characteristic curves. 2N5484 n-channel JFET: I_D versus V_{DS} for various values of V_{GS}.

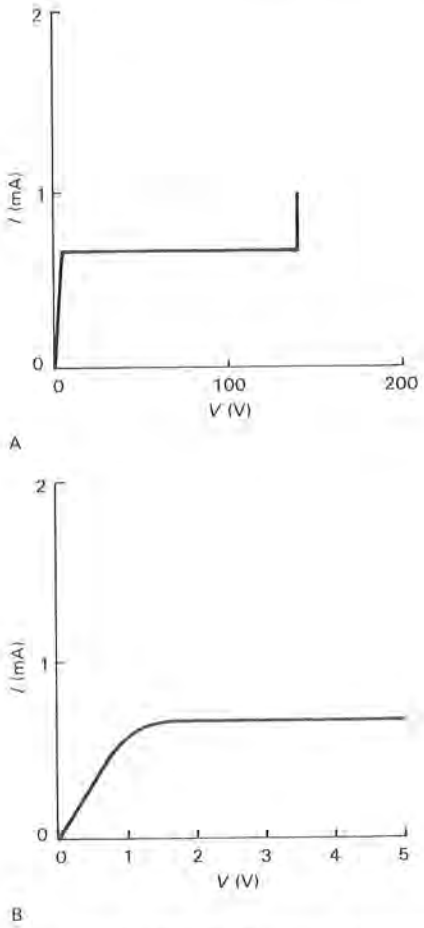


Figure 3.18. 1N5294 "current regulator diode."

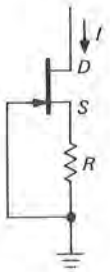


Figure 3.19

good constancy of current up to the breakdown voltage (140V for this particular specimen), whereas Figure 3.18B shows that the device reaches full current with somewhat less than 1.5 volts across it. We'll show how to use these devices to make a cute triangle-wave generator in Section 5.13. Table 3.4 is a partial listing of the 1N5283 series.

Source self-biasing

A variation of the previous circuit (Fig. 3.19) gives you an adjustable current source. The self-biasing resistor R back-biases the gate by $I_D R$, reducing I_D and bringing the JFET closer to pinch-off. You can calculate R from the drain curves for the particular JFET. This circuit allows you

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TABLE 3.3. DUAL MATCHED n-CHANNEL JFETs

Type	V_{os} max (mV)	Drift max (μV/°C)	I_{GSS} (V_{DG}=20V) max (pA)	CMRR min (dB)	$V_{GS(OFF)}$, V_P min (V)	$V_{GS(OFF)}$, V_P max (V)	e_n (10Hz) max (nV/√Hz)	C_{rss} (V_{DG}=10V) max (pF)	Comments
U421	10	10	0.2	90	0.4	2	50	1.5	Siliconix
2N3954A	5	5	100	–	1	3	150[a]	1.2	gen purp, low drift
2N3955	5	25	100	–	1	4.5	150[a]	1.2	popular
2N3958	25	–	100	–	1	4.5	150[a]	1.2	
2N5196	5	5	15	–	0.7	4	20[b]	2	
2N5520	5	5	100	100	0.7	4	15	5	
2N5906	5	5	2	90[t]	0.6	4.5	70[t]	1.5	low gate leakage
2N5911	10	20	100	–	1	5	20[c]	1.2	low noise at high freq
2N6483	5	5	100	100	0.7	4	10	3.5	low noise at low freq
NDF9406	5	5	5	120	0.5	4	30	0.1	cascode: low C_{rss}
2N5452	5	5	100[d]	–	1	4.5	20[b]	1.2[e]	
2SK146	20	–	1000[d]	–	0.3	1.2	1.3	15[t]	ultra low noise

[a] at 100Hz. [b] at 1kHz. [c] at 10kHz. [d] at 30V. [e] at 20V. [t] typical.

to set the current (which must be less than I_{DSS}), as well as to make it more predictable. Furthermore, the circuit is a better current source (higher impedance) because the source resistor provides "current-sensing feedback" (which we'll learn about in Section 4.07), and also because FETs tend to be better current sources anyway when the gate is back-biased (as can perhaps be seen from the flatness of the lower drain-current curves in Figs. 3.2 and 3.17). Remember, though, that actual curves of I_D for some value of V_{GS} obtained with a real FET may differ markedly from the values read from a set of published curves, owing to manufacturing spread. You may therefore want to use an adjustable source resistor, if it is important to have a specific current.

EXERCISE 3.1

Use the 2N5484 measured curves in Figure 3.17 to design a JFET current source to deliver 1mA. Now ponder the fact that the specified I_{DSS} of a 2N5484 is 1mA (min), 5mA (max).

A JFET current source, even if built with source resistor, shows some variation of output current with output voltage; i.e., it has finite output impedance, rather than the desirable infinite Z_{out}. The measured curves of Figure 3.17, for example, suggest that over a drain voltage range of 5 to 20 volts, a 2N5484 shows a drain current variation of 5% when operated with gate tied to source (i.e., I_{DSS}). This might drop to 2% or so if you use a source resistor. The same trick used in Figure 2.24 can be used with JFET current sources and is shown in Figure 3.20. The idea (as with BJTs) is to use a second JFET to hold constant the drain-source voltage of the current source. Q_1 is an ordinary JFET current source, shown in this case with a source resistor. Q_2 is a JFET of larger I_{DSS}, connected "in series" with the current source. It passes Q_1's (constant) drain current through to the load, while holding Q_1's drain at a fixed voltage – namely the gate-source voltage that makes Q_2 operate at the same current as Q_1. Thus Q_2 shields Q_1 from voltage swings

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TABLE 3.4. CURRENT-REGULATOR DIODES[a]

Type	I_P (mA)	Impedance (25V) min (MΩ)	V_{min} ($I > 0.8\ I_P$) (V)
1N5283	0.22	25	1.0
1N5285	0.27	14	1.0
1N5287	0.33	6.6	1.0
1N5288	0.39	4.1	1.1
1N5290	0.47	2.7	1.1
1N5291	0.56	1.9	1.1
1N5293	0.68	1.4	1.2
1N5294	0.75	1.2	1.2
1N5295	0.82	1.0	1.3
1N5296	0.91	0.9	1.3
1N5297	1.0	0.8	1.4
1N5299	1.2	0.6	1.5
1N5302	1.5	0.5	1.6
1N5304	1.8	0.4	1.8
1N5305	2.0	0.4	1.9
1N5306	2.2	0.4	2.0
1N5308	2.7	0.3	2.2
1N5309	3.0	0.3	2.3
1N5310	3.3	0.3	2.4
1N5312	3.9	0.3	2.6
1N5314	4.7	0.2	2.9

[a] all operate to 100V and 600mW, and look like diodes in the reverse direction

at its output; since Q_1 doesn't see drain voltage variations, it just sits there and provides constant current. If you look back at the Wilson mirror (Fig. 2.48), you'll see that it uses this same voltage clamping idea.

You may recognize this JFET circuit as the "cascode," which is normally used to circumvent Miller effect (Section 2.19). A JFET cascode is simpler than a BJT cascode, however, because you don't need a bias voltage for the gate of the upper FET: Because it's depletion-mode, you can simply ground the upper gate (compare with Fig. 2.74).

EXERCISE 3.2

Explain why the upper JFET in a cascode must have higher I_{DSS} than the lower JFET. It may help to consider a JFET cascode with no source resistor.

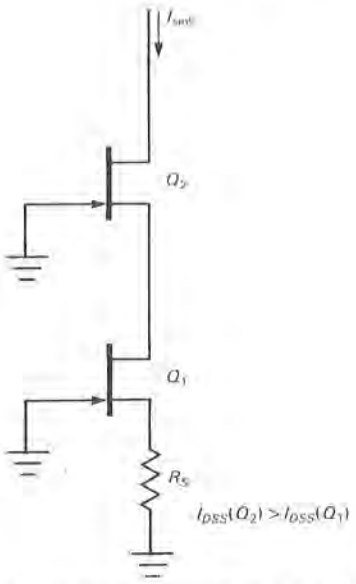


Figure 3.20. Cascode JFET current sink.

It is important to realize that a good bipolar transistor current source will give far better predictability and stability than a JFET current source. Furthermore, the op-amp-assisted current sources we'll see in the next chapter are better still. For example, a FET current source might vary 5% over a typical temperature range and load voltage variation, even after being set to the desired current by trimming the source resistor, whereas an op-amp/transistor (or op-amp/FET) current source is predictable and stable to better than 0.5% without great effort.

3.07 FET amplifiers

Source followers and common-source FET amplifiers are analogous to the emitter followers and common-emitter amplifiers made with bipolar transistors that we talked about in the last chapter. However, the absence of dc gate current makes

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it possible to realize very high input impedances. Such amplifiers are essential when dealing with the high-impedance signal sources encountered in measurement and instrumentation. For some specialized applications you may want to build followers or amplifiers with discrete FETs; most of the time, however, you can take advantage of FET-input op-amps. In either case it's worth knowing how they work.

With JFETs it is convenient to use the same self-biasing scheme as with JFET current sources (Section 3.06), with a single gate-biasing resistor to ground (Fig. 3.21); MOSFETs require a divider from the drain supply, or split supplies, just as we used with BJTs. The gate-biasing resistors can be quite large (a megohm or more), because the gate leakage current is measured in nanoamps.

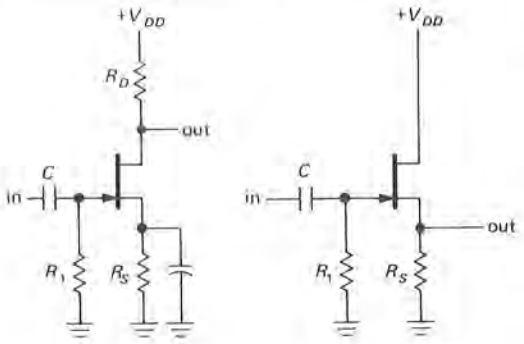


Figure 3.21

Transconductance

The absence of gate current makes *transconductance* (the ratio of output current to input voltage: $g_m = i_{\text{out}}/v_{\text{in}}$) the natural gain parameter for FETs. This is in contrast to bipolar transistors in the last chapter, where we at first flirted with the idea of current gain ($i_{\text{out}}/i_{\text{in}}$), then introduced the transconductance-oriented Ebers-Moll model: It's useful to think of BJTs either way, depending on the application.

FET transconductance can be estimated from the characteristic curves, either by looking at the increase in I_D from one gate-voltage curve to the next on the family of curves (Fig. 3.2 or 3.17), or, more simply, from the slope of the I_D–V_{GS} "transfer characteristics" curve (Fig. 3.14). The transconductance depends on drain current (we'll see how, shortly) and is, of course,

$$g_m(I_D) = i_d/v_{gs}$$

(Remember that lower-case letters indicate quantities that are small-signal variations.) From this we get the voltage gain

$$G_{\text{voltage}} = v_d/v_{gs} = -R_D i_d/v_{gs}$$
$$= -g_m R_D$$

just the same as the bipolar transistor result in Section 2.09, with load resistor R_C replaced by R_D. Typically, FETs have transconductances of a few thousand microsiemens (micromhos) at a few milliamps. Because g_m depends on drain current, there will be some variation of gain (nonlinearity) over the waveform as the drain current varies, just as we have with grounded emitter amplifiers (where $g_m = 1/r_e$, proportional to I_C). Furthermore, FETs in general have considerably lower transconductance than bipolar transistors, which makes them less suitable as amplifiers and followers. Let's look at this a little further.

Transconductance of FETs versus BJTs

To make our last remark quantitative, consider a JFET and a BJT, each operating at 1mA. Imagine they are connected as common source (emitter) amplifiers, with a drain (collector) resistor of 5k to a +10 volt supply (Fig. 3.22). Let's ignore details of biasing and concentrate on the gain. The BJT has an r_e of 25 ohms, hence a g_m of 40 mS, for a voltage gain of −200 (which you could have calculated directly as $-R_C/r_e$). A typical JFET (e.g., a

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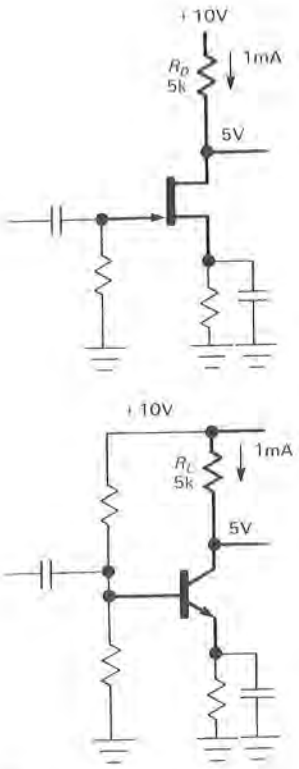


Figure 3.22

2N4220) has a g_m of 2mS at a drain current of 1mA, giving a voltage gain of -10. This seems discouraging by comparison. The low g_m also produces a relatively large Z_{out} in a follower configuration (Fig. 3.23): The JFET has

$$Z_{\text{out}} = 1/g_m$$

which in this case equals 500 ohms (independent of signal source impedance), to be compared with the BJT, which has

$$Z_{\text{out}} = R_s/h_{fe} + r_e = R_s/h_{fe} + 1/g_m$$

equal to R_s/h_{fe}+ 25 ohms (at 1mA). For typical transistor betas, say $h_{fe} = 100$, and reasonable signal sources, say with $R_s < 5k$, the BJT follower is an order of magnitude stiffer ($Z_{\text{out}} = 25\Omega$ to 75Ω). Note, however, that for $R_s > 50$k the JFET follower will be better.

To see what is happening, let's look back at the expressions for FET drain current versus gate-source voltage and compare with the equivalent expression (Ebers-Moll) for BJT collector current versus base-emitter voltage.

BJT: The Ebers-Moll equation,

$$I_C = I_S\{\exp(V_{BE}/V_T) - 1\},$$
$$\text{with } V_T = kT/q = 25\,\text{mV}$$

predicts $g_m = dI_C/dV_{BE} = I_C/V_T$ for collector currents large compared with "leakage" current I_S. This is our familiar result $r_e(\text{ohms}) = 25/I_C(\text{mA})$, since $g_m = 1/r_e$.

FET: In the "subthreshold" region of very low drain current,

$$I_D \propto \exp(V_{GS})$$

which, being exponential like Ebers-Moll, also gives a transconductance proportional

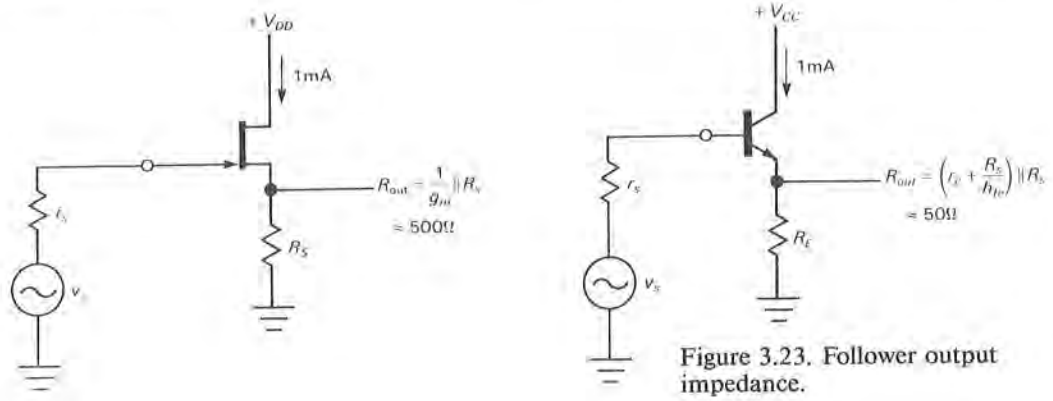


Figure 3.23. Follower output impedance.

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to current. However, for real-world values of k (which is determined by FET geometry, carrier mobility, etc.) the FET's transconductance is somewhat lower than the BJT's, about $I/40\text{mV}$ for p-channel MOSFETs and $I/60\text{mV}$ for n-channel MOSFETs, as compared with $I/25\text{mV}$ for BJTs. As the current is increased, the FET enters the normal "saturation" region, where

$$I_D = k(V_{GS} - V_T)^2$$

which gives $g_m = 2(kI_D)^{1/2}$. That is, the transconductance increases only as the square root of I_D and is well below the transconductance of a bipolar transistor at the same operating current; see Figure 3.24. Increasing the constant k in our preceding equations (by raising the width/length ratio of the channel) increases the transconductance (and the drain current, for a given V_{GS}) in the region above threshold, but the transconductance still remains less than that of a bipolar transistor at the same current.

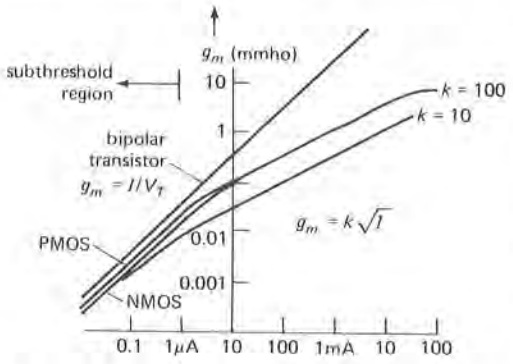


Figure 3.24. Comparison of g_m for bipolar transistors and FETs.

EXERCISE 3.3

Derive the foregoing expressions for g_m by differentiating I_{out} with respect to V_{in}.

The problem of low voltage gain in FET amplifiers can be circumvented by resorting to a current-source (active) load, but once again the bipolar transistor will be better in the same circuit. For this reason you seldom see FETs used as simple amplifiers, unless it's important to take advantage of their unique input properties (extremely high input resistance and low input current).

Note that FET transconductance in the saturation region is proportional to $V_{GS} - V_T$; thus, for example, a JFET with gate operated halfway to pinch-off has a transconductance approximately half that shown on the data sheet (where it is always given for $I_D = I_{DSS}$, i.e., $V_{GS} = 0$).

Differential amplifiers

Matched FETs can be used to construct high-input-impedance front-end stages for bipolar differential amplifiers, as well as the important op-amps and comparators we'll meet in the next chapter. As we mentioned earlier, the substantial V_{GS} offsets of FETs will generally result in larger input voltage offsets and offset drifts than with a comparable amplifier constructed entirely with bipolar transistors, but of course the input impedance will be raised enormously.

Oscillators

In general, FETs have characteristics that make them useful substitutes for bipolar transistors in almost any circuit that can benefit from their uniquely high input impedance and low bias current. A particular instance is their use in high-stability LC and crystal oscillators; we'll show examples in Sections 5.18, 5.19, and 13.11.

Active load

Just as with BJT amplifiers, it is possible to replace the drain-load resistor in a FET amplifier with an active load, i.e., a current

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source. The voltage gain you get that way can be very large:

$$G_V = -g_m R_D$$

(with a drain resistor as load)

$$G_V = -g_m R_0$$

(with a current source as load)

where R_0 is the impedance looking into the drain (called "g_{oss}"), typically in the range of 100k to 1M.

One possibility for an active load is a current mirror as the drain load for a differential FET pair (see Section 2.18); the circuit is not bias-stable, however, without overall feedback. The current mirror can be constructed with either FETs or BJTs. This configuration is often used in FET op-amps, as we'll see in the next chapter. You will see another nice example of the active load technique in Section 3.14 when we discuss the CMOS linear amplifier.

3.08 Source followers

Because of the relatively low transconductance of FETs, it's often better to use a FET "source follower" (analogous to an emitter follower) as an input buffer to a conventional BJT amplifier, rather than trying to make a common-source FET amplifier directly. You still get the high input impedance and zero dc input current of the FET, and the BJT's large transconductance lets you achieve high single-stage gain. Furthermore, discrete FETs (i.e., those that are not part of an integrated circuit) tend to have higher interelectrode capacitance than BJTs, leading to greater Miller effect (Section 2.19) in common-source amplifiers; the source follower configuration, like the emitter follower, has no Miller effect.

FET followers, with their high input impedance, are commonly used as input stages in oscilloscopes as well as other measuring instruments. There are many applications in which the signal source impedance is intrinsically high, e.g., capacitor microphones, pH probes, charged-particle detectors, or microelectrode signals in biology and medicine. In these cases a FET input stage (whether discrete or part of an integrated circuit) is a good solution. Within circuits there are situations where the following stage must draw little or no current. Common examples are analog "sample-and-hold" and "peak detector" circuits, in which the level is stored on a capacitor and will "droop" if the next amplifier draws significant input current. In all these applications the negligible input current of a FET is more important than its low transconductance, making source followers (or even common-source amplifiers) attractive alternatives to the bipolar emitter follower.

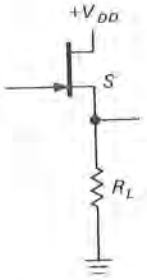


Figure 3.25

Figure 3.25 shows the simplest source follower. We can figure out the output amplitude, as we did for the emitter follower in Section 2.11, using the transconductance. We have

$$v_s = R_L i_d$$

since i_g is negligible; but

$$i_d = g_m v_{gs} = g_m(v_g - v_s)$$

so

$$v_s = \left[\frac{R_L g_m}{(1 + R_L g_m)}\right] v_g$$

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For $R_L \gg 1/g_m$ it is a good follower ($v_s \approx v_g$), with gain approaching, but always less than, unity.

Output impedance

The preceding equation for v_s is precisely what you would predict if the source follower's output impedance were equal to $1/g_m$ (try the calculation, assuming a source voltage of v_g in series with $1/g_m$ driving a load of R_L). This is exactly analogous to the emitter follower situation, where the output impedance was $r_e = 25/I_C$, or $1/g_m$. It can be easily shown explicitly that a source follower has output impedance $1/g_m$ by figuring the source current for a signal applied to the output with grounded gate (Fig. 3.26). The drain current is

$$i_d = g_m v_{gs} = g_m v$$

so

$$r_{\text{out}} = v/i_d = 1/g_m$$

typically a few hundred ohms at currents of a few milliamps. As you can see, FET source followers aren't nearly as stiff as emitter followers.

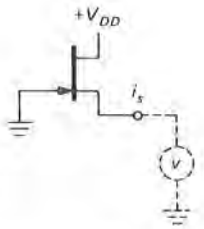


Figure 3.26

There are two drawbacks to this circuit:
1. The relatively high output impedance means that the output swing may be significantly less than the input swing, even with high load impedance, because R_L alone forms a divider with the source's output impedance. Furthermore, because the drain current is changing over the signal waveform, g_m and therefore the output impedance will vary, producing some nonlinearity (distortion) at the output. The situation is improved if FETs of high transconductance are used, of course, but a combination FET–bipolar follower is often a better solution.
2. Because the V_{GS} needed to produce a certain operating current is a poorly controlled parameter in FET manufacture, a source follower has an unpredictable dc offset, a serious drawback for dc-coupled circuits.

Active load

The addition of a few components improves the source follower enormously. Let's take it in stages:

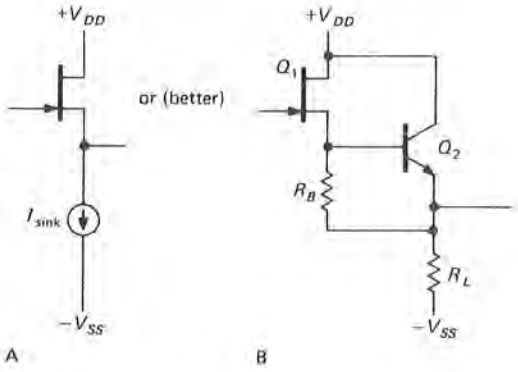


Figure 3.27

First, replace R_L with a (pull-down) current source (Fig. 3.27). The constant source current makes V_{GS} approximately constant, thus reducing nonlinearities. You can think of this as the previous case with infinite R_L, which is what a current source is. The circuit on the right has the advantage of providing low output impedance, while still providing a (roughly) constant source current of V_{BE}/R_B. We still have the problem of unpredictable (and therefore nonzero) offset voltage (from input to output) of V_{GS} ($V_{GS} + V_{BE}$ for

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the circuit on the right). Of course, we could simply adjust I_{sink} to the particular value of I_{DSS} for the given FET (in the first circuit) or adjust R_B (in the second). This is a poor solution, for two reasons: (a) It requires individual adjustment for each FET. (b) Even so, I_D may vary by a factor of two over the normal operating temperature range for a given V_{GS}.

A better circuit uses a matched FET pair to achieve zero offset (Fig. 3.28). Q_1 and Q_2 are a matched pair, on a single chip of silicon. Q_2 sinks a current exactly appropriate to the condition $V_{GS} = 0$. So, for both FETs, $V_{GS} = 0$, and Q_1 is therefore a follower with zero offset. Because Q_2 tracks Q_1 in temperature, the offset remains near zero independent of temperature.

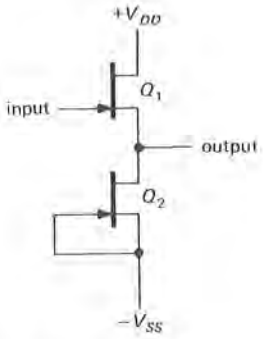


Figure 3.28

You usually see the preceding circuit with source resistors added (Fig. 3.29). A little thought should convince you that R_1 is necessary and that $R_1 = R_2$ guarantees that $V_{\text{out}} = V_{\text{in}}$ if Q_1 and Q_2 are matched. This circuit modification gives better I_D predictability, allows you to set the drain current to some value less than I_{DSS}, and gives improved linearity, since FETs are better current sources when operated below I_{DSS}. This follower circuit is popular as the input stage for oscilloscope vertical amplifiers.

For the utmost in performance you can add circuitry to bootstrap the drain (eliminating input capacitance) and use a bipolar output stage for low output impedance. That same output signal can then be used to drive an inner "guard" shield in order to effectively eliminate the effects of shielded-cable capacitance, which would otherwise be devastating for the high source impedances that you might see with this sort of high-impedance input buffer amplifier.

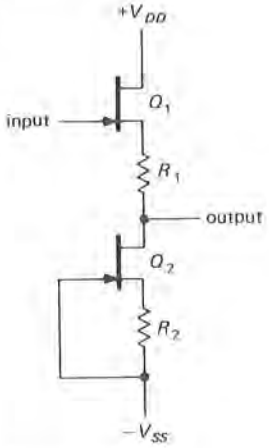


Figure 3.29

3.09 FET gate current

We said at the outset that FETs in general, and MOSFETs in particular, have essentially zero gate current. This is perhaps the most important property of FETs, and it was exploited in the high-impedance amplifiers and followers in the previous sections. It will prove essential, too, in applications to follow – most notably analog switches and digital logic.

Of course, at *some* level of scrutiny we might expect to see some gate current. It's important to know about gate current, because a naive zero-current model is guaranteed to get you in trouble sooner or later. In fact, finite gate current arises from

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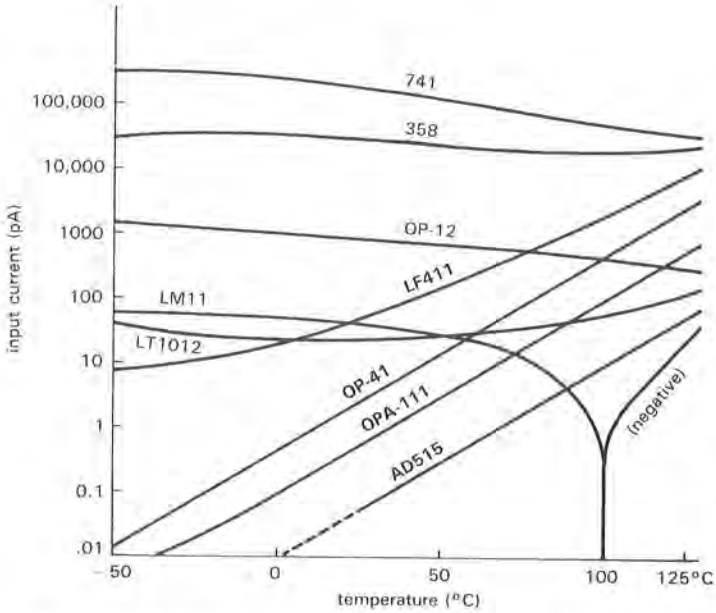


Figure 3.30. The input current of a FET amplifier is gate leakage, which doubles every 10°C.

several mechanisms: Even in MOSFETs the silicon dioxide gate insulation is not perfect, leading to leakage currents in the picoampere range. In JFETs the gate "insulation" is really a back-biased diode junction, with the same impurity and junction leakage current mechanisms as ordinary diodes. Furthermore, JFETs (n-channel in particular) suffer from an additional effect known as "impact-ionization" gate current, which can reach astounding levels. Finally, both JFETs and MOSFETs have *dynamic* gate current, caused by ac signals driving the gate capacitance; this can cause Miller effect, just as with bipolar transistors.

In most cases gate input currents are negligible in comparison with BJT base currents. However, there are situations in which a FET may actually have *higher* input current! Let's look at the numbers.

Gate leakage

The low-frequency input impedance of a FET amplifier (or follower) is limited by gate leakage. JFET data sheets usually specify a breakdown voltage, BV_{GSS}, defined as the voltage from gate to channel (source and drain connected together) at which the gate current reaches 1μA. For smaller applied gate-channel voltages, the gate leakage current, I_{GSS}, again measured with the source and drain connected together, is considerably smaller, dropping quickly to the picoampere range for gate-drain voltages well below breakdown. With MOSFETs you must never allow the gate insulation to break down; instead, gate leakage is specified as some maximum leakage current at a specified gate-channel voltage. Integrated circuit amplifiers with FETs (e.g., FET op-amps) use the misleading term "input bias current," I_B, to specify input leakage current; it's usually in the picoampere range.

The good news is that these leakage currents are in the picoampere range at room temperature. The bad news is that they increase rapidly (in fact, exponentially) with temperature, roughly doubling every 10°C. By contrast, BJT base currents aren't leakage, and in fact tend to *decrease* slightly with increasing temperature. The comparison is shown graphically in Figure 3.30, a plot of input current versus temperature for several IC amplifiers (op-amps).

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The FET-input op-amps have the lowest input currents at room temperature (and below), but their input current rises rapidly with temperature, crossing over the curves for amplifiers with carefully designed BJT input stages like the LM11 and LT1012. These BJT op-amps, along with "premium" low-input-current JFET op-amps like the OPA111 and AD549, are fairly expensive. However, we also included everyday "jellybean" op-amps like the bipolar 358 and JFET LF411 in the figure to give an idea of input currents you can expect with inexpensive (less than a dollar) op-amps.

□ JFET impact-ionization current

In addition to conventional gate leakage effects, n-channel JFETs suffer from rather large gate leakage currents when operated with substantial V_{DS} and I_D (the gate leakage specified on data sheets is measured under the unrealistic conditions $V_{DS} = I_D = 0$!). Figure 3.31 shows what happens. The gate leakage current remains near the I_{GSS} value until you reach a critical drain-gate voltage, at which point it rises precipitously. This extra "impact-ionization" current is proportional to drain current, and it rises exponentially with voltage and temperature. The onset of this current occurs at drain-gate voltages of about 25% of BV_{GSS}, and it can reach gate currents of a microamp or more. Obviously a "high-impedance buffer" with a microamp of input current is worthless. That's what you would get if you used a 2N4868A as a follower, running 1mA of drain current from a 40 volt supply.

This extra gate leakage current afflicts primarily n-channel JFETs, and it occurs at higher values of drain-gate voltage. Some cures are to (a) operate at low drain-gate voltage, either with a low-voltage drain supply or with a cascode, (b) use a p-channel JFET, where the effect is much smaller, or (c) use a MOSFET. The most important thing is to be aware of the effect so that it doesn't catch you by surprise.

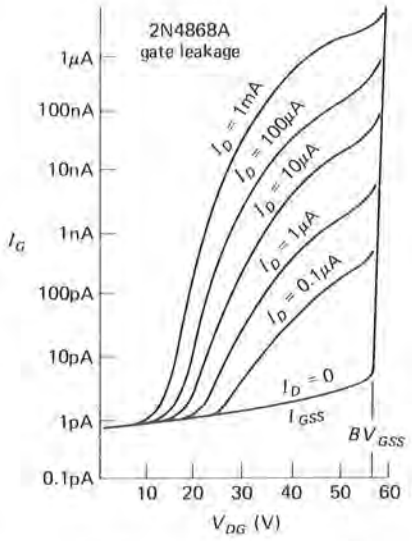


Figure 3.31. JFET gate leakage increases disastrously at higher drain-gate voltages and is proportional to drain current.

□ Dynamic gate current

Gate leakage is a dc effect. Whatever is driving the gate must also supply an *ac* current, because of gate capacitance. Consider a common-source amplifier. Just as with bipolar transistors, you can have the simple effect of input capacitance to ground (called C_{iss}), and you can have the capacitance-multiplying Miller effect (which acts on the feedback capacitance C_{rss}). There are two reasons why capacitive effects are more serious in FETs than in bipolar transistors: First, you use FETs (rather than BJTs) because you want very low input current; thus the capacitive currents loom relatively larger for the same capacitance. Second, FETs often have considerably larger capacitance than equivalent bipolar transistors.

To appreciate the effect of capacitance, consider a FET amplifier intended for a signal source of 100k source impedance.

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At dc there's no problem, because the picoampere currents produce only microvolt drops across the signal source's internal impedance. But at 1MHz, say, an input capacitance of 5pF presents a shunt impedance of about 30k, seriously attenuating the signal. In fact, *any* amplifier is in trouble with a high-impedance signal at high frequencies, and the usual solution is to operate at low impedance (50Ω is typical) or use tuned LC circuits to resonate away the parasitic capacitance. The point to understand is that the FET amplifier doesn't look like a 10^{12} ohm load at signal frequencies.

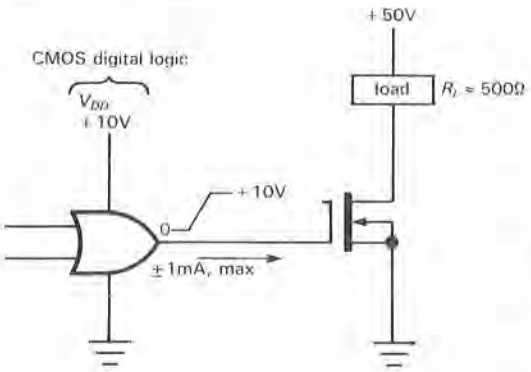


Figure 3.32

As another example, imagine switching a 10 amp load with a power MOSFET (there aren't any power JFETs), in the style of Figure 3.32. One might naively assume that the gate could be driven from a digital logic output with low current-sourcing capability, for example the so-called CMOS logic, which can supply output current on the order of 1mA with a swing from ground to +10 volts. In fact, such a circuit would be a disaster, since with 1mA of gate drive the 350pF feedback capacitance of the 2N6763 would stretch the output switching speed to a leisurely 20μs. Even worse, the dynamic gate currents ($I_{\text{gate}} = CdV_D/dt$) would force currents back into the logic device's output, possibly destroying it via a perverse effect known as "SCR latchup" (more of which in Chapters 8 and 9). Bipolar power transistors turn out to have comparable capacitances, and therefore comparable dynamic input currents; but when you design a circuit to drive a 10-amp power BJT, you're *expecting* to provide 500mA or so of base drive (via a Darlington or whatever), whereas with a FET you tend to take low input current for granted. In this example, once again, the ultra-high-impedance FET has lost some of its luster.

EXERCISE 3.4

Show that the circuit of Figure 3.32 switches in about 20μs, assuming 1mA of available gate drive.

3.10 FETs as variable resistors

Figure 3.17 showed the region of JFET characteristic curves (drain current versus V_{DS} for a small family of V_{GS} voltages), both in the normal ("saturated") regime and in the "linear" region of small V_{DS}. We showed the equivalent pair of graphs for a MOSFET at the beginning of the chapter (Fig. 3.2). The I_D-versus-V_{DS} curves are approximately straight lines for V_{DS} smaller than $V_{GS} - V_T$, and they extend in both directions through zero, i.e., the device can be used as a voltage-controlled resistor for small signals of either polarity. From our equation for I_D versus V_{GS} in the linear region (Section 3.04) we easily find the ratio (I_D/V_{DS}) to be

$$\frac{1}{R_{DS}} = 2k\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right]$$

The last term represents a nonlinearity, i.e., a departure from resistive behavior (resistance shouldn't depend on voltage). However, for drain voltages substantially less than the amount by which the gate is above threshold ($V_{DS} \rightarrow 0$), the last

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term becomes unimportant, and the FET behaves approximately like a resistance:

$$R_{DS} \approx 1/[2k(V_{GS} - V_T)]$$

Because the device-dependent parameter k isn't a quantity you are likely to know, it's more useful to write R_{DS} as

$$R_{DS} \approx R_0(V_{G0} - V_T)/(V_G - V_T)$$

where the resistance R_{DS} at any gate voltage V_G is written in terms of the (known) resistance R_0 at some gate voltage V_{G0}.

EXERCISE 3.5
Derive the preceding "scaling" law.

From either formula you can see that the conductance ($= 1/R_{DS}$) is proportional to the amount by which the gate voltage exceeds threshold. Another useful fact is that $R_{DS} = 1/g_m$, i.e., the channel resistance in the *linear* region is the inverse of the transconductance in the *saturated* region. This is a handy thing to know, because g_m is a parameter nearly always specified on FET data sheets.

EXERCISE 3.6
Show that $R_{DS} = 1/g_m$ by finding the transconductance from the saturation drain-current formula in Section 3.04.

Typically, the values of resistance you can produce with FETs vary from a few tens of ohms (as low as 0.1Ω for power MOSFETs) all the way up to an open circuit. A typical application might be an automatic-gain-control (AGC) circuit in which the gain of an amplifier is adjusted (via feedback) to keep the output within the linear range. In such an AGC circuit you must be careful to put the variable-resistance FET at a place in the circuit where the signal swing is small, preferably less than 200mV or so.

The range of V_{DS} over which the FET behaves like a good resistor depends on the particular FET and is roughly proportional to the amount by which the gate voltage exceeds V_P (or V_T). Typically, you might have nonlinearities of about 2% for $V_{DS} < 0.1(V_{GS} - V_P)$, and perhaps 10% nonlinearity for $V_{DS} \approx 0.25(V_{GS} - V_P)$. Matched FETs make it easy to design a ganged variable resistor to control several signals at once. JFETs intended for use as variable resistors are available (Siliconix VCR series) with resistance tolerances of 30%, specified at some V_{GS}.

It is possible to improve the linearity, and simultaneously the range of V_{DS} over which a FET behaves like a resistor, by a simple compensation scheme. We'll illustrate with an application.

□ *Linearizing trick: electronic gain control*

By looking at the preceding equation for $1/R_{DS}$, you can see that the linearity will be nearly perfect if you can add to the gate voltage a voltage equal to one-half the drain-source voltage. Figure 3.33 shows two circuits that do exactly that. In the first, the JFET forms the lower half of a resistive voltage divider, thus forming a voltage-controlled attenuator (or "volume control"). R_1 and R_2 improve the linearity by adding a voltage of $0.5V_{DS}$ to V_{GS}, as just discussed. The JFET shown has an ON resistance (gate grounded) of 60 ohms (max), giving the circuit an attenuation range of 0 to 40dB.

The second circuit uses a MOSFET as a variable emitter resistance in an emitter-degenerated ac amplifier. Note the use of a constant-dc-current emitter pulldown (Wilson mirror or FET current-regulator diode); this (a) looks like a very high impedance at signal frequencies, thus letting the variable-resistance FET set the gain over a wide range (including $G_V \ll 1$), and (b) provides simple biasing. By using a blocking capacitor, we've arranged the circuit so that the FET affects only the

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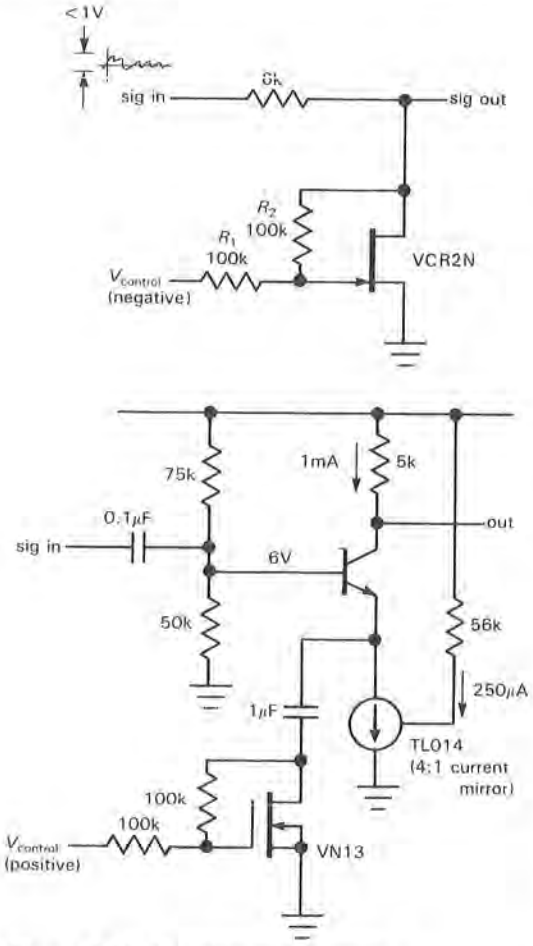


Figure 3.33. Variable-gain circuits.

ac (signal) gain. Without the capacitor, the transistor biasing would vary with FET resistance.

EXERCISE 3.7

The VN13 has an ON resistance ($V_{GS} = +5V$) of 15 ohms (max). What is the range of amplifier gain in the second circuit (assume that the current sink looks like 1MΩ)? What is the low-frequency 3dB point when the FET is biased so that the amplifier gain is (a) 40dB or (b) 20dB?

The linearization of R_{DS} with a resistive gate divider circuit, as above, is remarkably effective. In Figure 3.34 we've compared actual measured curves of I_D versus V_{DS} in the linear (low-V_{DS}) region for FETs with and without the linearizing circuit. The linearizing circuit is essential for low-distortion applications with signal swings of more than a few millivolts.

When considering FETs for an application requiring a gain control, e.g., an AGC or "modulator" (in which the amplitude of a high-frequency signal is varied at an audio rate, say), it is worthwhile to look also at "analog-multiplier" ICs. These are high-accuracy devices with good dynamic range that are normally used to form the product of two voltages. One of the voltages can be a dc control signal, setting the multiplication factor of the device for the other input signal, i.e., the gain. Analog multipliers exploit the g_m-versus-I_C characteristic of bipolar transistors [$g_m = I_C$(mA)/25 siemens], using matched arrays to circumvent problems of offsets and bias shifts. At very high frequencies (100MHz and above), passive "balanced mixers" (Section 13.12) are often the best devices to accomplish the same task.

It is important to remember that a FET in conduction at low V_{DS} behaves like a good resistance all the way down to zero volts from drain to source (there are no diode drops or the like to worry about). We will see op-amps and digital logic families (CMOS) that take advantage of this nice property, giving outputs that saturate cleanly to the power supplies.

FET SWITCHES

The two examples of FET circuits that we gave at the beginning of the chapter were both *switches*: a logic-switching application and a linear signal-switching circuit. These are among the most important FET applications and take advantage of the FET's unique characteristics: high gate impedance and bipolarity resistive conduction clear down to zero volts. In practice

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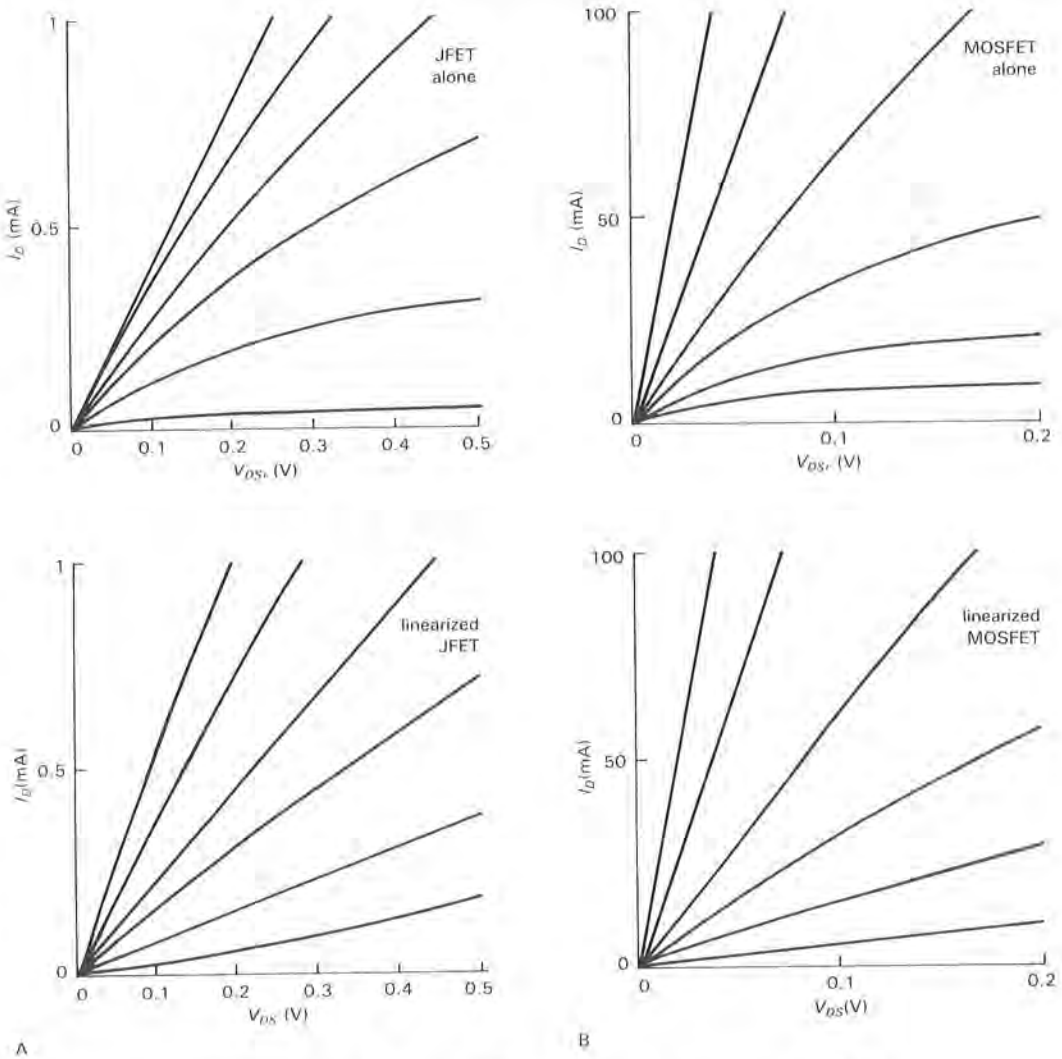


Figure 3.34. Measured curves of I_D versus V_{DS} for bare and linearized FETS.
A. 2N5484 JFET
B. VN0106 MOSFET

you usually use MOSFET integrated circuits (rather than discrete transistors) in all digital logic and linear switch applications, and it is only in power switching applications that you resort to discrete FETs. Even so, it is essential (and fun!) to understand the workings of these chips; otherwise you're almost guaranteed to fall prey to some mysterious circuit pathology.

3.11 FET analog switches

A common use of FETs, particularly MOSFETs, is as analog switches. Their combination of low ON resistance (all the way to zero volts), extremely high OFF resistance, low leakage currents, and low capacitance makes them ideal as voltage-controlled switch elements for analog signals. An ideal analog, or linear, switch behaves like

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a perfect mechanical switch: In the ON state it passes a signal through to a load without attenuation or nonlinearity; in the OFF state it is an open circuit. It should have negligible capacitance to ground and negligible coupling to the signal of the switching level applied to the control input.

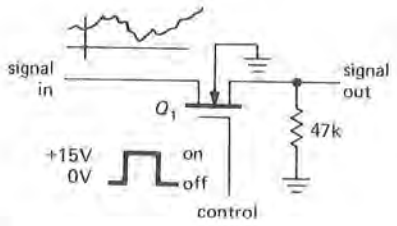


Figure 3.35

Let's look at an example (Fig. 3.35). Q_1 is an n-channel enhancement-mode MOSFET, and it is nonconducting when the gate is grounded or negative. In that state the drain-source resistance (R_{OFF}) is typically more than 10,000M, and no signal gets through (though at high frequencies there will be some coupling via drain-source *capacitance*; more on this later). Bringing the gate to +15 volts puts the drain-source channel into conduction, typically 25 to 100 ohms (R_{ON}) in FETs intended for use as analog switches. The gate signal level is not at all critical, as long as it is sufficiently more positive than the largest signal (to maintain R_{ON} low), and it could be provided from digital logic circuitry (perhaps using a FET or BJT to generate a full-supply swing) or even from an op-amp (whose ±13V output swing would do nicely, since gate breakdown voltages in MOSFETs are typically 20V or more). Swinging the gate negative (as from an op-amp output) doesn't hurt, and in fact has the added advantage of allowing the switching of analog signals of either polarity, as will be described later. Note that the FET switch is a bidirectional device; signals can go either way through it. Ordinary mechanical switches work that way, too, so it should be easy to understand.

The circuit as shown will work for positive signals up to about 10 volts; for larger signals the gate drive is insufficient to hold the FET in conduction (R_{ON} begins to rise), and negative signals would cause the FET to turn on with the gate grounded (it would also forward bias the channel-body junction; see Section 3.02). If you want to switch signals that are of both polarities (e.g., signals in the range −10V to +10V), you can use the same circuit, but with the gate driven from −15 volts (OFF) to +15 volts (ON); the body should then be tied to −15 volts.

With any FET switch it is important to provide a load resistance in the range of 1k to 100k in order to reduce capacitive feedthrough of the input signal that would otherwise occur during the OFF state. The value of the load resistance is a compromise: Low values reduce feedthrough, but they begin to attenuate the input signal because of the voltage divider formed by R_{ON} and the load. Because R_{ON} varies over the input signal swing (from changing V_{GS}), this attenuation also produces some undesirable nonlinearity. Excessively low load resistance appears at the switch input, of course, loading the signal source as well. Several possible solutions to this problem (multiple-stage switches, R_{ON} cancellation) are shown in Sections 3.12 and 4.30. An attractive alternative is to use a second FET switch section to connect the output to ground when the series FET is off, thus effectively forming an SPDT switch (more on this in the next section).

CMOS linear switches

Frequently it is necessary to switch signals that may go nearly to the supply voltages. In that case the simple n-channel switch circuit just described won't work, since the gate is not forward-biased at the

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peak of the signal swing. The solution is to use paralleled complementary MOSFET ("CMOS") switches (Fig. 3.36). The triangular symbol is a digital inverter, which we'll discuss shortly; it inverts a HIGH input to a LOW output, and vice versa. When the control input is high, Q_1 is held ON for signals from ground to within a few volts of V_{DD} (where R_{ON} starts increasing dramatically). Q_2 is likewise held ON (by its grounded gate) for signals from V_{DD} to within a few volts of ground (where its R_{ON} increases dramatically). Thus, signals anywhere between V_{DD} and ground are passed through with low series resistance (Fig. 3.37). Bringing the control signal to ground turns off both FETs, providing an open circuit. The result is an analog switch for signals between ground and V_{DD}. This is the basic construction of the 4066 CMOS "transmission gate." It is bidirectional, like the switches described earlier; either terminal can be the input.

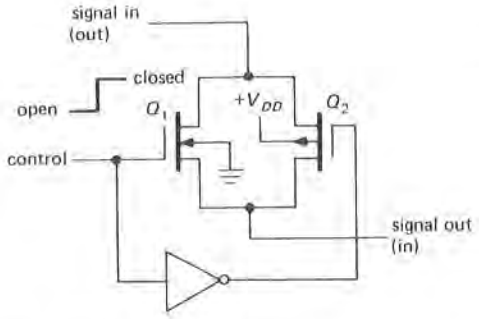


Figure 3.36. CMOS analog switch.

There is a variety of integrated circuit CMOS analog switches available, with various switch configurations (e.g., several independent sections with several poles each). The 4066 is the classic 4000-series CMOS "analog transmission gate," just another name for an analog switch for signals between ground and a single positive supply. The IH5040 and IH5140 series from Intersil and Harris and the DG305 and DG400 series from Siliconix are very convenient to use; they accept logic-level (0V = LOW, > 2.4V = HIGH) control signals, they will handle analog signals to ±15 volts (compared with only ±7.5V for the 4000 series), they come in a variety of configurations, and they have relatively low ON resistance (25Ω for some members of these families). Analog Devices, Maxim, and PMI also manufacture nice analog switches.

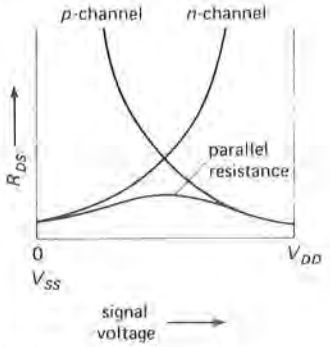


Figure 3.37

Multiplexers

A nice application of FET analog switches is the "multiplexer" (or MUX), a circuit that allows you to select any of several inputs, as specified by a digital control signal. The analog signal present on the selected input will be passed through to the (single) output. Figure 3.38 shows the basic scheme. Each of the switches SW0 through SW3 is a CMOS analog switch. The "select logic" decodes the address and *enables* (jargon for "turns on") the addressed switch only, disabling the remaining switches. Such a multiplexer is usually used in conjunction with digital circuitry that generates the appropriate addresses. A typical situation might involve a data-acquisition instrument in which a number of analog input voltages must be sampled in turn, converted to digital quantities, and used as input to some computation.

Because analog switches are bidirectional, an analog multiplexer such as this is

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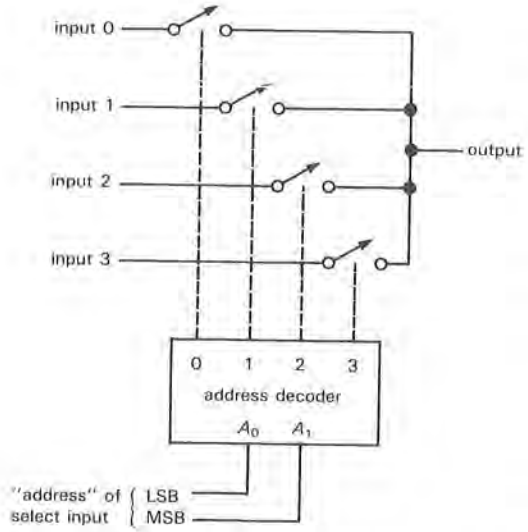


Figure 3.38. Analog multiplexer.

also a "demultiplexer": A signal can be fed into the "output" and will appear on the selected "input." When we discuss digital circuitry in Chapters 8 and 9, you will see that an analog multiplexer such as this can also be used as a "digital multiplexer/demultiplexer," because logic levels are, after all, nothing but voltages that happen to be interpreted as binary 1's and 0's.

Typical of analog multiplexers are the DG506–509 series and the IH6108 and 6116 types, 8- or 16-input MUX circuits that accept logic-level address inputs and operate with analog voltages up to ±15 volts. The 4051-4053 devices in the CMOS digital family are analog multiplexers/demultiplexers with up to 8 inputs, but with 15 volt pp maximum signal levels; they have a V_{EE} pin (and internal level shifting) so that you can use them with bipolarity analog signals and unipolarity (logic-level) control signals.

Other analog switch applications

Voltage-controlled analog switches form essential building blocks for op-amp circuits we'll see in the next chapter – integrators, sample-and-hold circuits, and peak detectors. For example, with op-amps we will be able to build a "true" integrator (unlike the approximation to an integrator we saw in Section 1.15): A constant input generates a linear ramp output (not an exponential), etc. With such an integrator you must have a method to reset the output; a FET switch across the integrating capacitor does the trick. We won't try to describe these applications here; because op-amps form essential parts of the circuits, they fit naturally into the next chapter. Great things to look forward to!

3.12 Limitations of FET switches

Speed

FET switches have ON resistances R_{ON} of 25 to 200 ohms. In combination with substrate and stray capacitances, this resistance forms a low-pass filter that limits operating speeds to frequencies of the order of 10MHz or less (Fig. 3.39). FETs with lower R_{ON} tend to have larger capacitance (up to 50pF with some MUX switches), so no gain in speed results. Much of the rolloff is due to protection components – current-limiting series resistance, and capacitance of shunt diodes. There are a few "RF/video" analog switches that obtain higher speeds, probably by eliminating some protection. For example, the

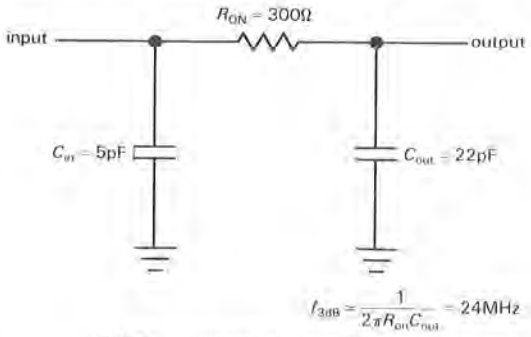


Figure 3.39

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IH5341 and IH5352 switches handle analog signals over the usual ±15 volt range and have a bandwidth of 100MHz; the 74HC4051-53 series of "high-speed" CMOS multiplexers also provide a 3dB analog bandwidth of 100MHz, but handle signals only to ±5 volts. The MAX453–5 from Maxim combine a video multiplexer with an output video amplifier, so you can drive low-impedance cables or loads (usually 75Ω) directly; they have 50MHz typical bandwidth and are intended for ±1 volt low-impedance video signals.

ON resistance

CMOS switches operated from a relatively high supply voltage (15V, say) will have low R_{ON} over the entire signal swing, because one or the other of the transmission FETs will have a forward gate bias at least half the supply voltage. However, when operated with lower supply voltages, the switch's R_{ON} value will rise, the maximum occurring when the signal is about halfway between the supply and ground (or halfway between the supplies, for dual-supply voltages). Figure 3.40 shows why. As V_{DD} is reduced, the FETs begin to have significantly higher ON resistance (especially near $V_{GS} = V_{DD}/2$), since for enhancement-mode FETs V_T is at least a few volts, and a gate-source voltage of as much as 5 to 10 volts is required to achieve low R_{ON}. Not only will the parallel resistances of the two FETs rise for signal voltages between the supply voltage and ground, but also the peak resistance (at half V_{DD}) will rise as V_{DD} is reduced, and for sufficiently low V_{DD} the switch will become an open circuit for signals near $V_{DD}/2$.

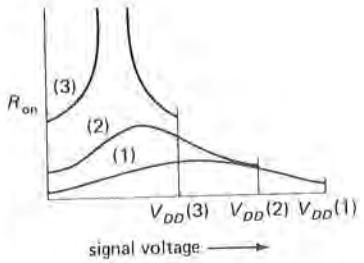


Figure 3.40

There are various tricks used by the designers of analog switch ICs to keep R_{ON} low, and approximately constant (for low distortion), over the signal swing. For example, the original 4016 analog switch used the simple circuit of Figure 3.36, producing R_{ON} curves that look like those in Figure 3.41. In the improved 4066 switch the designers added a few extra FETs so that the n-channel body voltage follows the signal voltage, producing the R_{ON} curves of Figure 3.42. The "volcano" shape, with

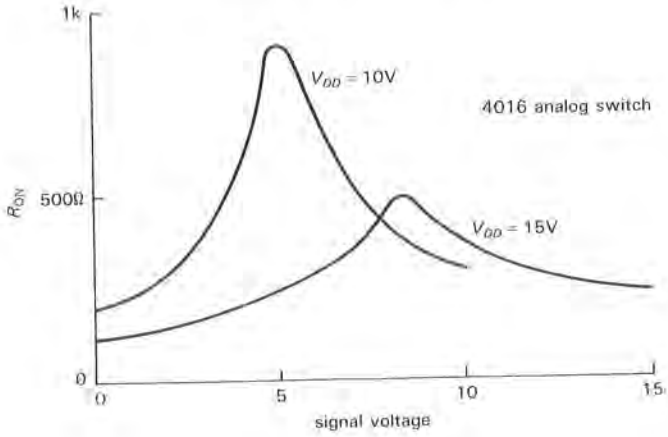


Figure 3.41. ON resistance for 4016 CMOS switch.

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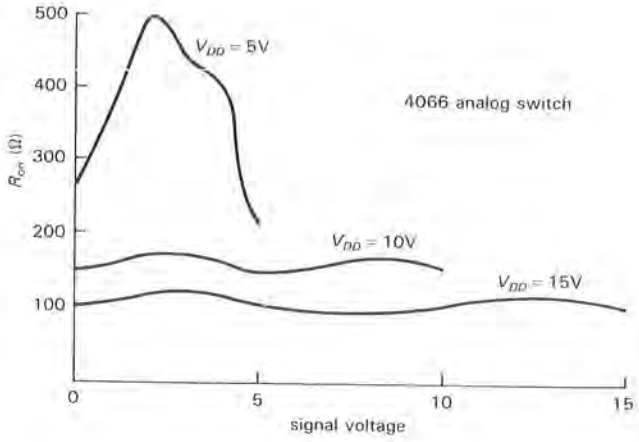


Figure 3.42. ON resistance for the improved 4066 CMOS switch; note change of scale from previous figure.

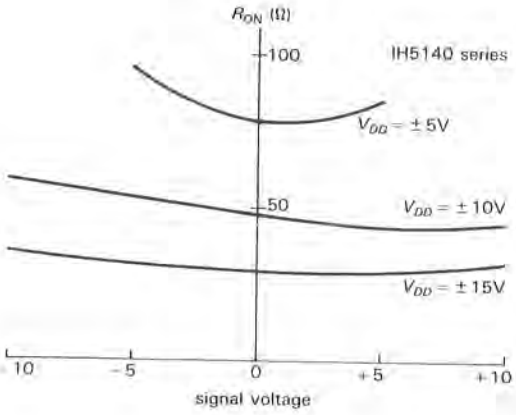


Figure 3.43. ON resistance for the IH5140-series bipolarity analog switches; note vertical scale.

its depressed central R_{ON}, replaces the "Everest" shape of the 4016. Sophisticated switches like the IH5140 series (or AD7510 series), intended for serious analog applications, succeed even better, with gentle R_{ON} curves like those shown in Figure 3.43. The recent DG400 series from Siliconix achieves an excellent R_{ON} of 20 ohms, at the expense of increased "charge transfer" (see the later section on *glitches*); this switch family (like the IH5140 series) has the additional advantage of zero quiescent current.

Capacitance

FET switches exhibit capacitance from input to output (C_{DS}), from channel to ground (C_D, C_S), from gate to channel, and from one FET to another within one IC package (C_{DD}, C_{SS}); see Figure 3.44. Let's look at the effects:

C_{DS}: Capacitance from input to output. Capacitance from input to output causes signal coupling in an OFF switch, rising at high frequencies. Figure 3.45 shows the effect for the IH5140 series. Note the use

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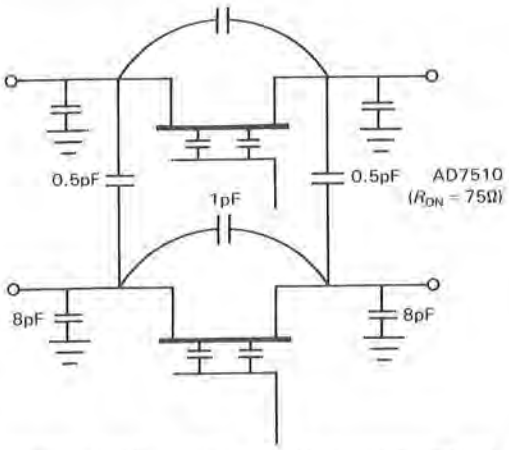


Figure 3.44. Analog switch capacitances – AD7510 4-channel switch.

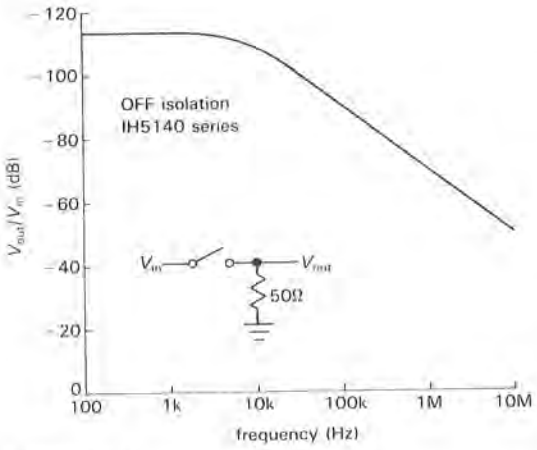


Figure 3.45

of a stiff 50 ohm load, common in radiofrequency circuits, but much lower than normal for low-frequency signals, where a typical load impedance is 10k or more. Even with a 50 ohm load, the feedthrough becomes significant at high frequencies (at 30MHz 1pF has a reactance of 5k, giving −40dB of feedthrough). And, of course, there is significant attenuation (and nonlinearity) driving a 50 ohm load, since R_{ON} is typically 30 ohms (75Ω worst-case). With a 10k load the feedthrough situation is much worse, of course.

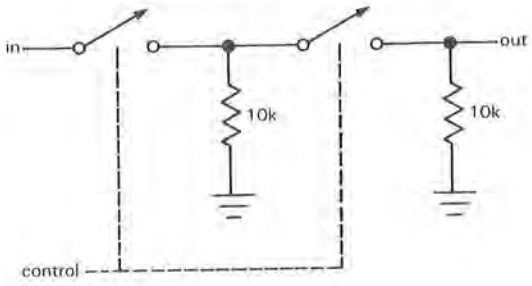


Figure 3.46

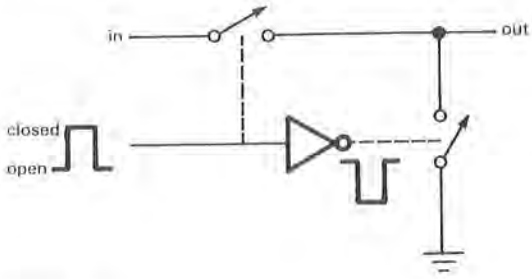


Figure 3.47

EXERCISE 3.8
Calculate the feedthrough into 10k at 1MHz, assuming $C_{DS} = 1$pF.

In most low-frequency applications capacitive feedthrough is not a problem. If it is, the best solution is to use a pair of cascaded switches (Fig. 3.46) or, better still, a combination of series and shunt switches, enabled alternately (Fig. 3.47). The series cascade doubles the attenuation (in decibels), at the expense of additional R_{ON}, whereas the series-shunt circuit (effectively an SPDT configuration) reduces feedthrough by dropping the effective load resistance to R_{ON} when the series switch is off.

EXERCISE 3.9
Recalculate switch feedthrough into 10k at 1MHz, assuming $C_{DS} = 1$pF and $R_{ON} = 50$ ohms, for the configuration of Fig. 3.47.

CMOS SPDT switches with controlled break-before-make are available commercially in single packages; in fact, you can

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get a pair of SPDT switches in a single package. Examples are the DG188 and IH5142, as well as the DG191, IH5143, and AD7512 (dual SPDT units). Because of the availability of such convenient CMOS switches, it is easy to use this SPDT configuration to achieve excellent performance. The RF/video switches mentioned earlier use a series-shunt circuit internally.

C_D, C_S: Capacitance to ground. Shunt capacitance to ground leads to the high frequency rolloff mentioned earlier. The situation is worst with a high-impedance signal source, but even with a stiff source the switch's R_{ON} combines with the shunt capacitance at the output to make a low-pass filter. The following problem shows how it goes.

EXERCISE 3.10

An AD7510 (here chosen for its complete capacitance specifications, shown in Fig. 3.44) is driven by a signal source of 10k, with a load impedance of 100k at the switch's output. Where is the high-frequency −3dB point? Now repeat the calculation, assuming a perfectly stiff signal source, and a switch R_{ON} of 75 ohms.

Capacitance from gate to channel. Capacitance from the controlling gate to the channel causes a different effect, namely the coupling of nasty little transients into your signal when the switch is turned on or off. This subject is worth some serious discussion, so we'll defer it to the next section on glitches.

C_{DD}, C_{SS}: Capacitance between switches. If you package several switches on a single piece of silicon the size of a kernel of corn, it shouldn't surprise you if there is some coupling between channels ("cross-talk"). The culprit, of course, is cross-channel capacitance. The effect increases with frequency and with signal impedance in the channel to which the signal is coupled. Here's a chance to work it out for yourself:

EXERCISE 3.11

Calculate the coupling, in decibels, between a pair of channels with $C_{DD} = C_{SS} = 0.5$pF (Fig. 3.44) for the source and load impedances of the last exercise. Assume that the interfering signal is 1MHz. In each case calculate the coupling for (a) OFF switch to OFF switch, (b) OFF switch to ON switch, (c) ON switch to OFF switch, and (d) ON switch to ON switch.

It should be obvious from this example why most broadband radiofrequency circuits use low signal impedances, usually 50 ohms. If cross-talk is a serious problem, don't put more than one signal on one chip.

Glitches

During turn-on and turn-off transients, FET analog switches can do nasty things. The control signal being applied to the gate(s) can couple capacitively to the channel(s), putting ugly transients on your signal. The situation is most serious if the signal is at high impedance levels. Multiplexers can show similar behavior during transitions of the input address, as well as momentary connection between inputs if turn-off delay exceeds turn-on delay. A related bad habit is the propensity of some switches (e.g., the 4066) to short the input to ground momentarily during changes of state.

Let's look at this problem in a bit more detail. Figure 3.48 shows a typical waveform you might see at the output of an n-channel MOSFET analog switch circuit similar to Figure 3.35, with an input

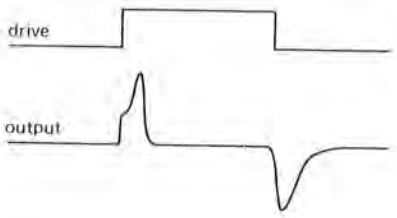


Figure 3.48

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signal level of zero volts and an output load consisting of 10k in parallel with 20pF, realistic values for an analog switch circuit. The handsome transients are caused by charge transferred to the channel, through the gate-channel capacitance, at the transitions of the gate. The gate makes a sudden step from one supply voltage to the other, in this case between ±15 volt supplies, transferring a slug of charge

$$Q = C_{GC}[V_G(\text{finish}) - V_G(\text{start})]$$

C_{GC} is the gate-channel capacitance, typically around 5pF. Note that the amount of charge transferred to the channel depends only on the total voltage change at the gate, not on its rise time. Slowing down the gate signal gives rise to a smaller-amplitude glitch of longer duration, with the same total area under its graph. Low-pass filtering of the switch's output signal has the same effect. Such measures may help if the peak amplitude of the glitch must be kept small, but in general they are ineffective in eliminating gate feedthrough. In some cases the gate-channel capacitance may be predictable enough for you to cancel the spikes by coupling an inverted version of the gate signal through a small adjustable capacitor.

The gate-channel capacitance is distributed over the length of the channel, which means that some of the charge is coupled back to the switch's input. As a result, the size of the output glitch depends on the signal source impedance and is smallest when the switch is driven by a voltage source. Of course, reducing the size of the load impedance will reduce the size of the glitch, but this also loads the source and introduces error and nonlinearity due to finite R_{ON}. Finally, all other things being equal, a switch with smaller gate-channel capacitance will introduce smaller switching transients, although you pay a price in the form of increased R_{ON}.

Figure 3.49 shows an interesting comparison of gate-induced charge transfers for three kinds of analog switches, including JFETs. In all cases the gate signal is making a full swing, i.e., either 30 volts or the indicated supply voltage for MOSFETs, and a swing from −15 volts to the signal level for the n-channel JFET switch. The JFET switch shows a strong

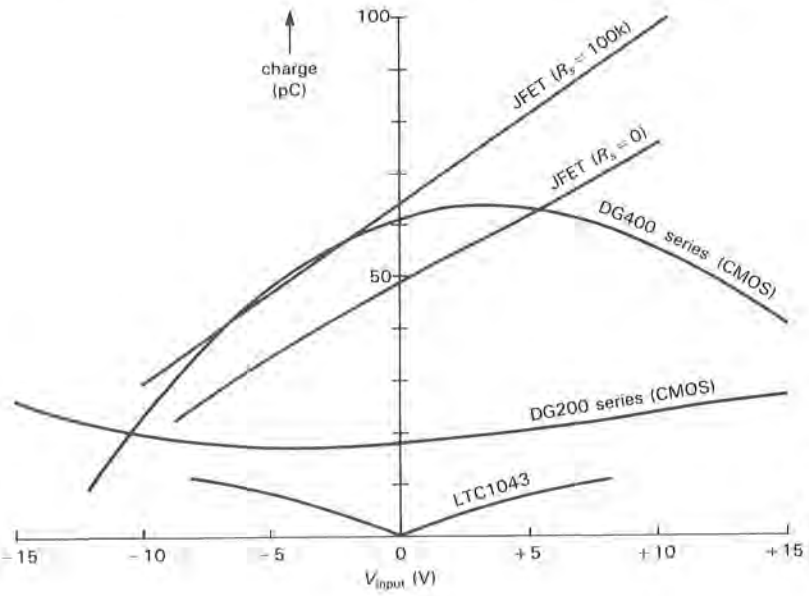


Figure 3.49. Charge transfer for various FET linear switches as a function of signal voltage.

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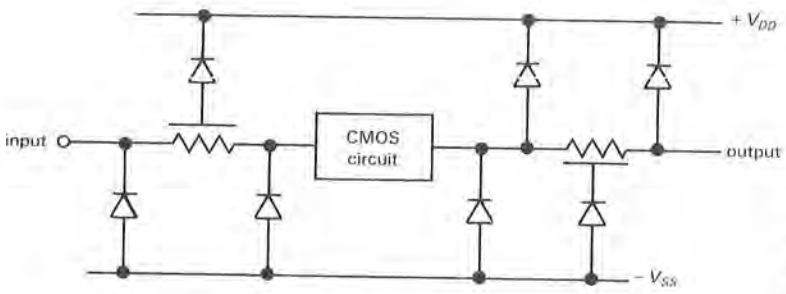


Figure 3.50. CMOS input/output protection networks. The series resistor at the output is often omitted.

dependence of glitch size on signal, because the gate swing is proportional to the level of the signal above −15 volts. Well-balanced CMOS switches have relatively low feedthrough because the charge contributions of the complementary MOSFETs tend to cancel out (one gate is rising while the other is falling). Just to give scale to these figures, it should be pointed out that 30pC corresponds to a 3mV step across a 0.01μF capacitor. That's a rather large filter capacitor, and you can see that this is a real problem, since a 3mV glitch is pretty large when dealing with low-level analog signals.

Latchup and input current

All CMOS integrated circuits have some form of input protection circuit, because otherwise the gate insulation is easily destroyed (see the later section on handling precautions). The usual protection network is shown in Figure 3.50: Although it may use distributed diodes, the network is equivalent to clamping diodes to V_{SS} and to V_{DD}, combined with resistive current limiting. If you drive the inputs (or outputs) more than a diode drop beyond the supply voltages, the diode clamps go into conduction, making the inputs (or outputs) look like a low impedance to the respective supplies. Worse still, the chip can be driven into "SCR latchup," a terrifying (and destructive) condition we'll describe in more detail in Section 14.16. For now, all you need to know about it is that you don't want it! SCR latchup is triggered by input currents (through the protection network) of roughly 20mA or more. Thus, you must be careful not to drive the analog inputs beyond the rails. This means, for instance, that you must be sure the power supply voltages are applied before any signals that have significant drive current capability. Incidentally, this prohibition goes for *digital* CMOS ICs as well as the analog switches we have been discussing.

The trouble with diode-resistor protection networks is that they compromise switch performance, by increasing R_{ON}, shunt capacitance, and leakage. With clever chip design (making use of "dielectric isolation") it is possible to eliminate SCR latchup without the serious performance compromises inherent in traditional protection networks. Many of the newer analog switch designs are "fault protected"; for example, Intersil's IH5108 and IH5116 analog multiplexers claim you can drive the analog inputs to ±25 volts, even with the supply at zero (you pay for this robustness with an R_{ON} that is four times higher than that of the conventional IH6108/16). Watch out, though, because there are plenty of analog switch ICs around that are not forgiving!

You can get analog switches and multiplexers built with n-channel JFETs rather than complementary MOSFETs. They perform quite well, improving on CMOS switches in several characteristics. In particular, the series of JFET switches from PMI has superior constancy of R_{ON} versus analog voltage, complete absence of

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latchup, and low susceptibility to electrostatic damage.

Other switch limitations

Some additional characteristics of analog switches that may or may not be important in any given application are switching time, settling time, break-before-make delay, channel leakage current (both ON and OFF; see Section 4.15), R_{ON} matching, temperature coefficient of R_{ON}, and signal and power supply ranges. We'll show unusual restraint by ending the discussion at this point, leaving the reader to look into these details if the circuit application demands it.

3.13 Some FET analog switch examples

As we indicated earlier, many of the natural applications of FET analog switches are in op-amp circuits, which we will treat in the next chapter. In this section we will show a few switch applications that do not require op-amps, to give a feeling for the sorts of circuits you can use them in.

Switchable RC low-pass filter

Figure 3.51 shows how you could make a simple RC low-pass filter with selectable 3dB points. We've used a multiplexer to select one of four preset resistors, via a 2-bit (digital) address. We chose to put the switch at the input, rather than after the resistors, because there is less charge injection at a point of lower signal impedance. Another possibility, of course, is to use FET switches to select the *capacitor*. To generate a very wide range of time constants you might have to do that, but the switch's finite R_{ON} would limit attenuation at high frequencies, to a maximum of R_{ON}/R_{series}. We've also indicated a unity-gain buffer, following the filter, since the output impedance is high. You'll see how to make "perfect" followers (precise gain, high Z_{in}, low Z_{out}, and no V_{BE} offsets, etc.) in the next chapter. Of course, if the amplifier that follows the filter has high input impedance, you don't need the buffer.

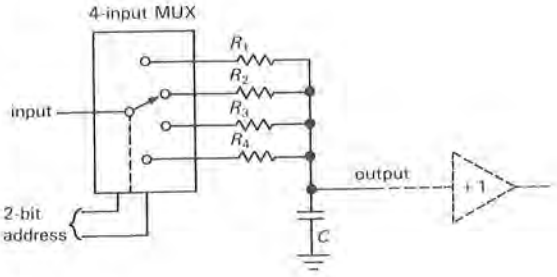


Figure 3.51

Figure 3.52 shows a simple variation in which we've used four independent switches, rather than a 4-input multiplexer. With the resistors scaled as shown, you can generate 16 equally spaced 3dB frequencies by turning on binary combinations of the switches.

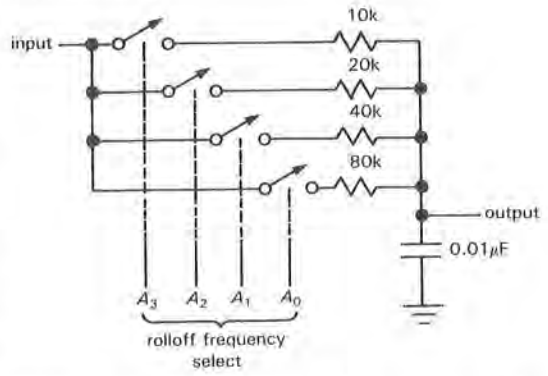


Figure 3.52. RC low-pass filter with choice of 15 equally spaced time constants.

EXERCISE 3.12
What are the 3dB points for this circuit?

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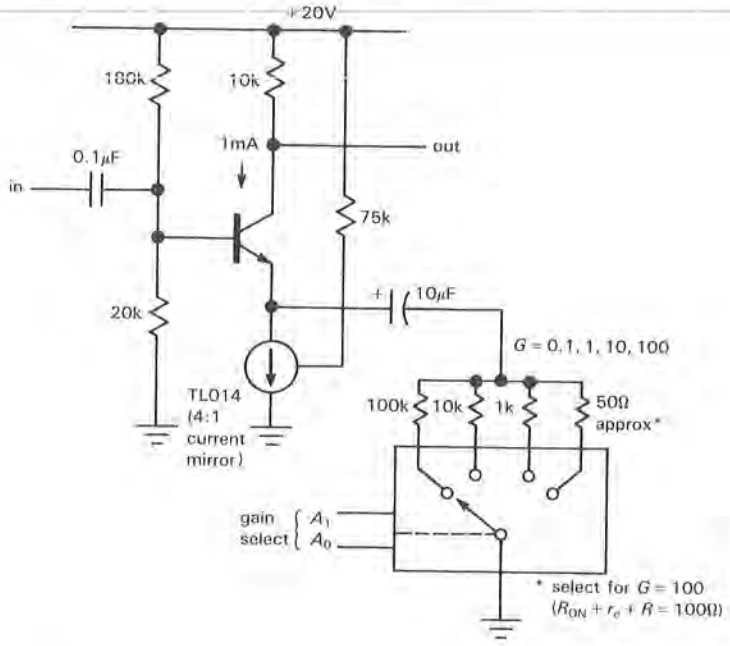


Figure 3.53. An analog multiplexer selects appropriate emitter degeneration resistors to achieve decade-switchable gain.

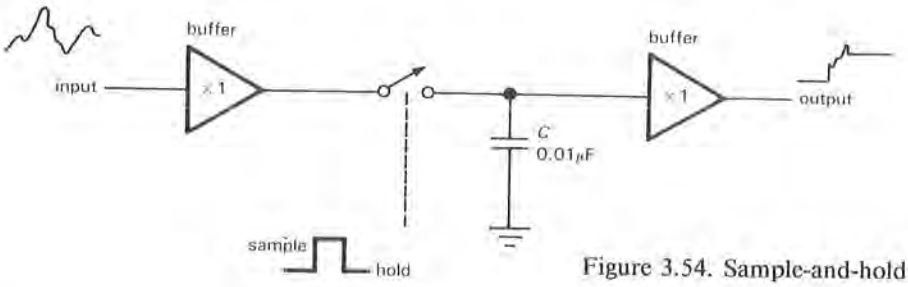


Figure 3.54. Sample-and-hold.

Switchable gain amplifier

Figure 3.53 shows how you can apply the same idea of switching resistors to produce an amplifier of selectable gain. Although this idea is a natural for op-amps, we can use it with the emitter-degenerated amplifier. We used a constant-current sink as emitter load, as in an earlier example, to permit gains much less than unity. We then used the multiplexer to select one of four emitter resistors. Note the blocking capacitor, needed to keep the quiescent current independent of gain.

Sample-and-hold

Figure 3.54 shows how to make a "sample-and-hold" circuit, which comes in handy when you want to convert an analog signal to a stream of digital quantities ("analog-to-digital conversion") – you've got to hold each analog level steady while you figure out how big it is. The circuit is simple: A unity-gain input buffer generates a low-impedance copy of the input signal, forcing it across a small capacitor. To hold the analog level at any moment, you simply open the switch. The high input impedance of the second buffer (which

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should have FET input transistors, to keep input current near zero) prevents loading of the capacitor, so it holds its voltage until the FET switch is again closed.

EXERCISE 3.13

The input buffer must supply current to keep the capacitor following a varying signal. Calculate the buffer's peak output current when the circuit is driven by an input sine wave of 1 volt amplitude at 10kHz.

Flying-capacitor voltage converter

Here's a nice way (Fig. 3.55) to generate a needed negative power-supply voltage in a circuit that is powered by a single positive supply. The pair of FET switches on the left connects C_1 across the positive supply, charging it to V_{in}, while the switches on the right are kept open. Then the input switches are opened, and the switches on the right are closed, connecting charged C_1 across the output, transferring some of its charge onto C_2. The switches are diabolically arranged so that C_1 gets turned upside down, generating a *negative* output! This particular circuit is available as the 7662 voltage converter chip, which we'll talk about in Sections 6.22 and 14.07. The device labeled "inverter" turns a HIGH voltage into a LOW voltage, and vice versa. We'll show you how to make one in the next section (and we'll really get you up to speed on them in Chapters 8–11!).

3.14 MOSFET logic and power switches

The *other* kinds of FET switch applications are *logic* and *power switching* circuits. The distinction is simple: In analog signal switching you use a FET as a series switch, passing or blocking a signal that has some range of analog voltage. The analog signal is usually a low-level signal, at insignificant power levels. In logic switching, on the other hand, MOSFET switches open and close to generate full swings between the power supply voltages. The "signals" here are really digital, rather than analog—they swing between the power supply voltages, representing the two states HIGH and LOW. In-between voltages are not useful or desirable; in fact, they're not even legal! Finally, "power switching" refers to turning on or off the power to a load such as a lamp, relay coil, or motor winding; in these applications, both voltages and currents tend to be large. We'll take logic switching first.

Logic switching

Figure 3.56 shows the simplest kind of logic switching with MOSFETs: Both circuits use a resistor as load and perform the logical function of *inversion* – a HIGH

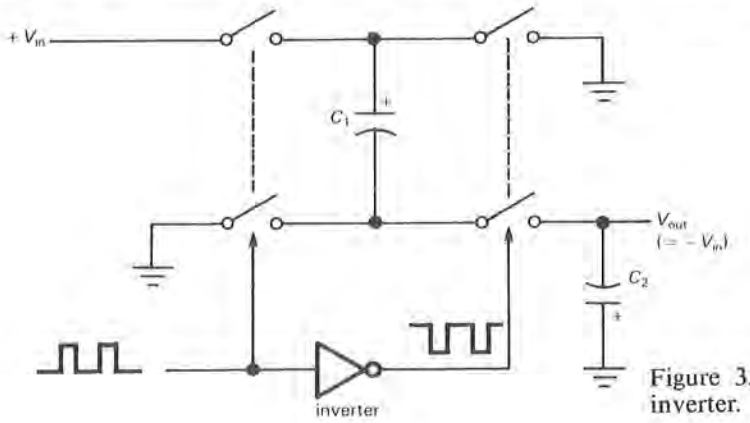


Figure 3.55. Flying-capacitor voltage inverter.

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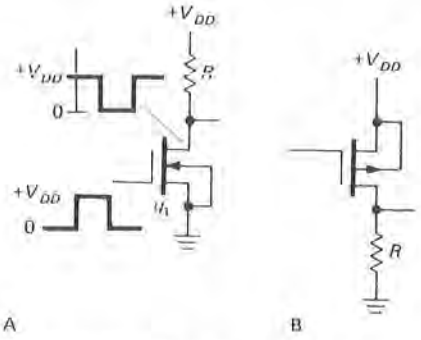


Figure 3.56. NMOS and PMOS logic inverters.

input generates a LOW output, and vice versa. The n-channel version pulls the output to ground when the gate goes HIGH, whereas the p-channel version pulls the resistor HIGH for grounded (LOW) input. Note that the MOSFETs in these circuits are used as common-source inverters, rather than as source followers. In digital logic circuits like these we are usually interested in the output voltage ("logic level") produced by a certain input voltage; the resistor serves merely as a passive drain load, to make the output swing to the drain supply when the FET is off. If, on the other hand, we replace the resistor by a light bulb, relay, printhead hammer, or some other hefty load, we've got a power-switching application (Fig. 3.3). Although we're using the same "inverter" circuit, in the power switching application we're interested instead in turning the load on and off.

CMOS inverter

The NMOS and PMOS inverters of the preceding circuits have the disadvantage of drawing current in the ON state and having relatively high output impedance in the OFF state. You can reduce the output impedance (by reducing R), but only at the expense of increased dissipation, and vice versa. Except for current sources, of course, it's never a good idea to have high output impedance. Even if the intended load is high impedance (another MOSFET gate, for example), you are inviting capacitive noise pickup problems, and you will suffer reduced switching speeds for the ON-to-OFF ("trailing") edge (because of stray loading capacitance). In this case, for example, the NMOS inverter with a compromise value of drain resistor, say 10k, would produce the waveform shown in Figure 3.57.

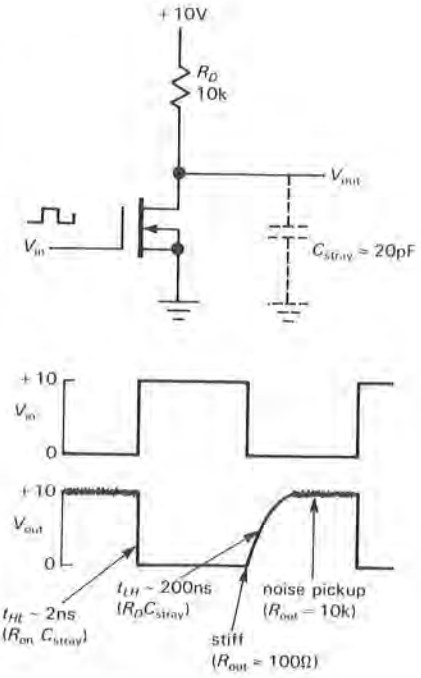


Figure 3.57

The situation is reminiscent of the single-ended emitter follower in Section 2.15, in which quiescent power dissipation and power delivered to the load were involved in a similar compromise. The solution there – the push-pull configuration – is particularly well suited to MOSFET switching. Look at Figure 3.58, which you might think of as a push-pull switch: Input grounded cuts off the bottom transistor and turns on the top transistor, pulling the output HIGH. A HIGH input ($+V_{DD}$) does the reverse, pulling the output to ground. It's an inverter with low output

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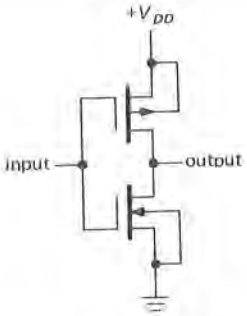


Figure 3.58. CMOS logic inverter.

impedance in *both* states, and no quiescent current whatsoever. It's called a CMOS (complementary MOS) inverter, and it is the basic structure of all digital CMOS logic, the logic family that has become dominant in large-scale integrated circuits (LSI), and seems destined to replace earlier logic families (with names like "TTL") based on bipolar transistors. Note that the CMOS inverter is two complementary MOSFET switches *in series*, alternately enabled, while the CMOS analog switch (treated earlier in the chapter) is two complementary MOSFET switches *in parallel*, enabled simultaneously.

EXERCISE 3.14

The complementary MOS transistors in the CMOS inverter are both operating as common-source inverters, whereas the complementary bipolar transistors in the push-pull circuits of Section 2.15 are (non-inverting) emitter followers. Try drawing a "complementary BJT inverter," analogous to the CMOS inverter. Why won't it work?

We'll be seeing much more of digital CMOS in the chapters on digital logic and microprocessors (Chapters 8-11). For now, it should be evident that CMOS is a low power logic family (with *zero* quiescent power) with high-impedance inputs, and with stiff outputs that swing the full supply range. Before leaving the subject, however, we can't resist the temptation to show you one additional CMOS circuit (Fig. 3.59). This is a logic *NAND gate*, whose output goes LOW only if input A AND input B are both HIGH. The operation is surprisingly easy to understand: If A and B are both HIGH, series NMOS switches Q_1 and Q_2 are both ON, pulling the output stiffly to ground; PMOS switches Q_3 and Q_4 cooperate by being OFF; thus, no current flows. However, if either A or B (or both) is LOW, the corresponding PMOS transistor is ON, pulling the output HIGH; since one (or both) of the series chain Q_1Q_2 is OFF, no current flows.

This is called a "NAND" gate because it performs the logical AND function, but

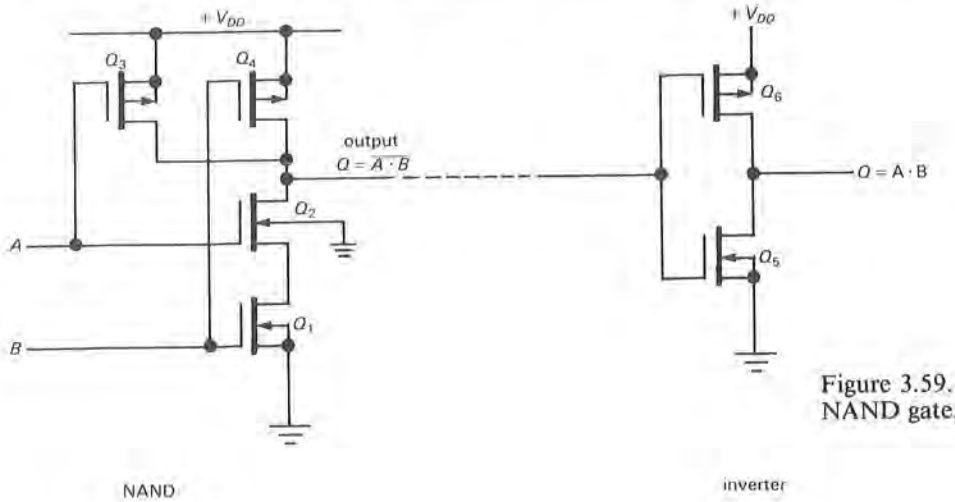


Figure 3.59. CMOS NAND gate, AND gate.

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with inverted ("NOT") output – it's a NOT-AND, abbreviated NAND. Although gates and their variants are properly a subject for Chapter 8, you will enjoy trying your hand at the following problems.

EXERCISE 3.15
Draw a CMOS AND gate. Hint: AND = NOT-NAND.

EXERCISE 3.16
Now draw a NOR gate: The output is LOW if either A OR B (or both) is HIGH.

EXERCISE 3.17
You guessed it – draw a CMOS OR gate.

EXERCISE 3.18
Draw a 3-input CMOS NAND gate.

The CMOS digital logic we'll be seeing later is constructed from combinations of these basic gates. The combination of very low power dissipation and stiff rail-to-rail output swing makes CMOS logic the family of choice for most digital circuits, accounting for its popularity. Furthermore, for micropower circuits (such as wristwatches and small battery-powered instruments) it's the only game in town.

Lest we leave the wrong impression, however, it's worth noting that CMOS logic is not *zero*-power. There are two mechanisms of current drain: During transitions, a CMOS output must supply a transient current $I = CdV/dt$ to charge any capacitance it sees (Fig. 3.60). You get load capacitance both from wiring ("stray" capacitance) and from the input capacitance of additional logic that you are driving. In fact, because a complicated CMOS chip contains many internal gates, each driving some on-chip internal capacitance, there is some current drain in any CMOS circuit that is making transitions, even if the chip is not driving any external load. Not surprisingly, this "dynamic" current drain is proportional to the rate at which transitions take place. The second mechanism of CMOS current drain is shown in Figure 3.61: As the input jumps between the supply voltage and ground, there is a region where both MOSFETs are conducting, resulting in large current spikes from V_{DD} to ground. This is sometimes called "class-A current" or "power supply crowbarring." You will see some consequences of this in Chapters 8, 9, and 14. As long as we're dumping on CMOS, we should mention that an additional disadvantage of CMOS (and, in fact, of all MOSFETs) is its vulnerability to damage from static electricity. We'll have more to say about this in Section 3.15.

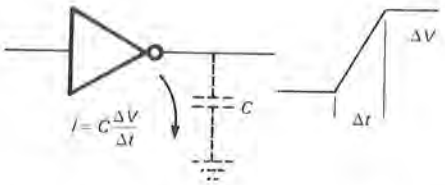


Figure 3.60. Capacitive charging current.

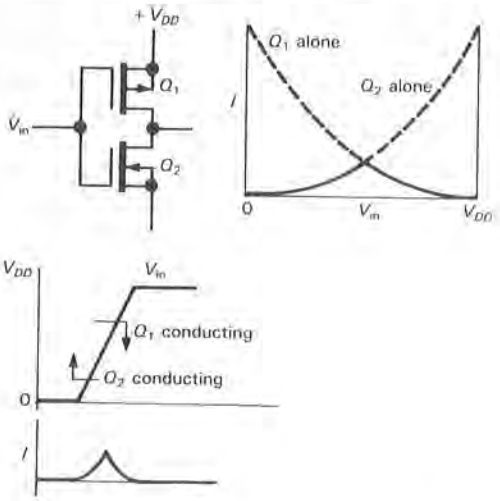


Figure 3.61. Class-A CMOS conduction.

☐ *CMOS linear amplifier*

CMOS inverters – and indeed all CMOS digital logic circuits – are intended to be

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used with digital signal levels. Except during transitions between states, therefore, the inputs and outputs are close to ground or V_{DD} (usually +5V). And except during those transitions (with typical durations of a few nanoseconds), there is no quiescent current drain.

The CMOS inverter turns out to have some interesting properties when used with *analog* signals. Look again at Figure 3.61. You can think of Q_1 as an active (current-source) load for inverting amplifier Q_2, and vice versa. When the input is near V_{DD} or ground, the currents are grossly mismatched, and the amplifier is in saturation (or "clipping") at ground or V_{DD}, respectively. This is, of course, the normal situation with digital signals. However, when the input is near half the supply voltage, there is a small region where the drain currents of Q_1 and Q_2 are nearly equal; in this region the circuit is an inverting linear amplifier with high gain. Its transfer characteristic is shown in Figure 3.62. The variation of R_{load} and g_m with drain current is such that the highest voltage gain occurs for relatively low drain currents, i.e., at low supply voltages (say 5V).

This circuit is not a good amplifier; it has the disadvantage of very high output impedance (particularly when operated at low voltage), poor linearity, and unpredictable gain. However, it is simple and inexpensive (CMOS inverters are available 6 to a package for under half a dollar), and it is sometimes used to amplify small input signals whose waveforms aren't important. Some examples are proximity switches (which amplify 60Hz capacitive pickup), crystal oscillators, and frequency-sensing input devices whose output is a frequency that goes to a frequency counter (see Chapter 15).

To use a CMOS inverter as a linear amplifier, it's necessary to bias the input so that the amplifier is in its active region. The usual method is with a large-

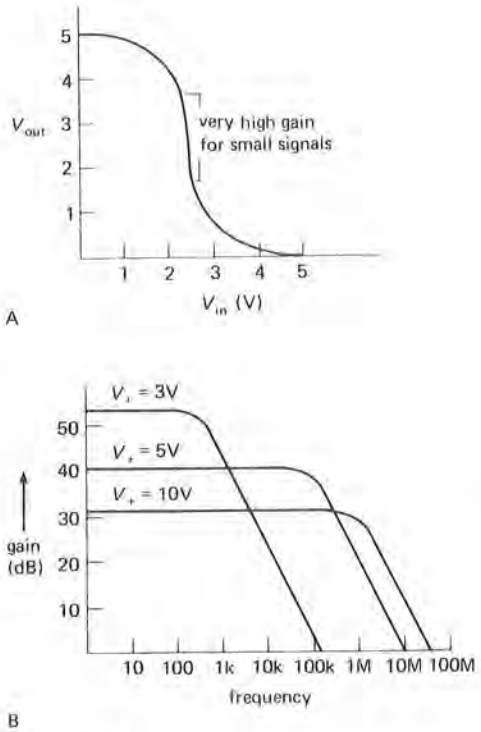


Figure 3.62

value resistor from output to input (which we'll recognize as "dc feedback" in the next chapter), as shown in Figure 3.63. That puts us at the point $V_{\text{out}} = V_{\text{in}}$ in Figure 3.62. As we'll learn later, such a connection (circuit A) also acts to lower the input impedance, through "shunt feedback," making circuit B desirable if a high input impedance at signal frequencies is important. The third circuit is the classic CMOS crystal oscillator, discussed in Section 5.13. Figure 3.64 shows a variant of circuit A, used to generate a clean 10MHz full-swing square wave (to drive digital logic) from an input sine wave. The circuit works well for input amplitudes from 50mV rms to 5 volts rms. This is a good example of an "I don't know the gain, and I don't care" application. Note the input-protection network, consisting of a current-limiting series resistor and clamping diodes.

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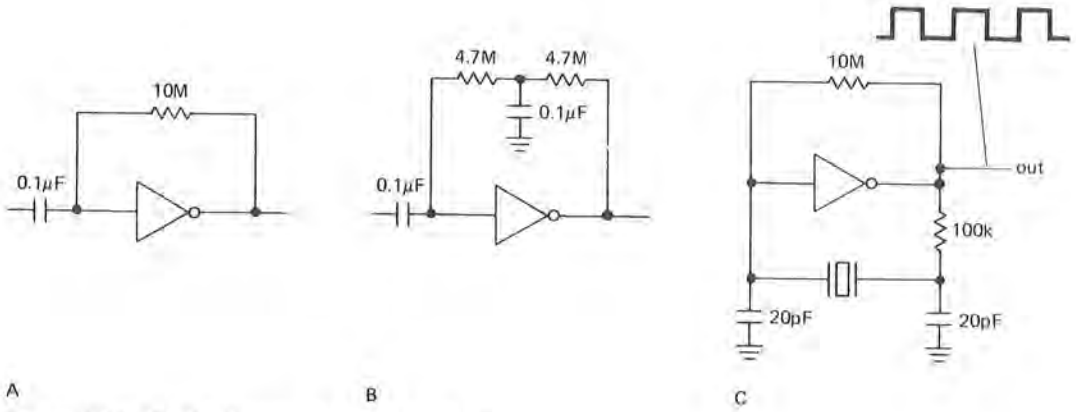


Figure 3.63. CMOS linear amplifier circuits.

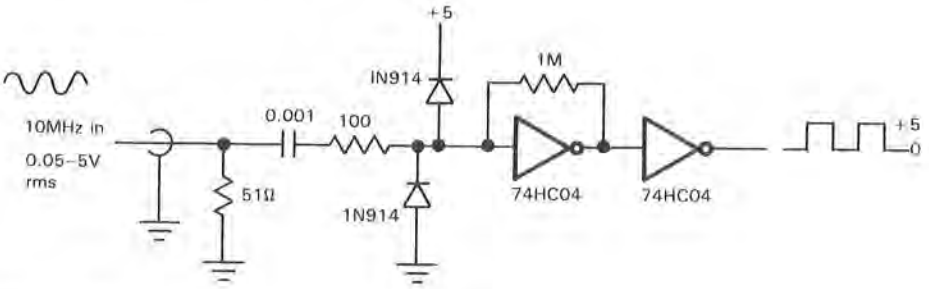


Figure 3.64

Power switching

MOSFETs work well as saturated switches, as we suggested with our simple circuit in Section 3.01. Power MOSFETs are now available from many manufacturers, making the advantages of MOSFETs (high input impedance, easy paralleling, absence of "second breakdown") applicable to power circuits. Generally speaking, power MOSFETs are easier to use than conventional bipolar power transistors. However, there are some subtle effects to consider, and cavalier substitution of MOSFETs in switching applications can lead to prompt disaster. We've visited the scenes of such disasters and hope to avert their repetition. Read on for our handy guided tour.

Power MOSFETs. FETs were feeble low-current devices, barely able to run more than a few tens of milliamps, until the late 1970s, when the Japanese introduced "vertical-groove" MOS transistors. Power MOSFETs are now manufactured by all the manufacturers of discrete semiconductors (e.g, GE, IR, Motorola, RCA, Siliconix, Supertex, TI, along with European companies like Amperex, Ferranti, Siemens, and SGS, and many of the Japanese companies), with names like VMOS, TMOS, vertical DMOS, and HEXFET. They can handle surprisingly high voltages (up to 1000V), and peak currents to 280 amps (continuous currents to 70A), with R_{ON} as low as 0.02 ohm. Small power MOSFETs sell for much less than a dollar, and they're available in all the usual transistor packages, as well as multiple transistors packaged in the convenient DIP (dual in-line package) that most integrated

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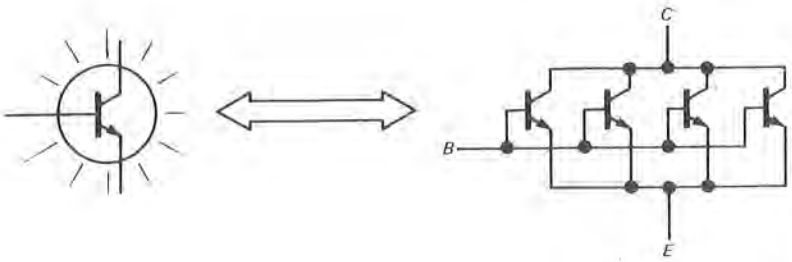


Figure 3.65. A large-junction-area transistor can be thought of as many paralleled small-area transistors.

circuits come in. Ironically, it is now discrete *low-level* MOSFETs that are hard to find, there being no shortage of power MOSFETs. See Table 3.5 for a listing of representative power MOSFETs.

High impedance, thermal stability. The two important advantages of the power MOSFET, compared with the bipolar power transistor, are its high input impedance (but watch out for high input capacitance, particularly with high-current devices; see below) and its complete absence of thermal runaway and second breakdown. This latter effect is very important in power circuits and is worth understanding: The large junction area of a power transistor (whether BJT or FET) can be thought of as a large number of small junctions in parallel (Fig. 3.65), all with the same applied voltages. In the case of a bipolar power transistor, the positive temperature coefficient of collector current at fixed V_{BE} (approximately +9%/°C, see Section 2.10) means that a local hot spot in the junction will have a higher current density, thus producing additional heating. At sufficiently high V_{CE} and I_C, this "current hogging" can cause local thermal runaway, known as *second breakdown*. As a result, bipolar power transistors are limited to a "safe operating area" (on a plot of collector current versus collector voltage) smaller than that allowed by transistor power dissipation alone (we'll see more of this in Chapter 6). The important point here is that the *negative* temperature coefficient of MOS drain current (Fig. 3.13) prevents these junction hot spots entirely. MOSFETs have no second breakdown, and their safe operating area (SOA) is limited only by power dissipation (see Fig. 3.66, where we've compared the SOAs of an *npn* and an NMOS power transistor of the same I_{max}, V_{max}, and P_{diss}). For the same reason, MOSFET power amplifiers don't have the nasty runaway tendencies that we've all grown to love in bipolar transistors (see Section 2.15), and as an added bonus, power MOSFETs can be paralleled without the current-equalizing "emitter-ballasting" resistors that are necessary with bipolar transistors (see Section 6.07).

Power switching examples and cautions. You often want to control a power MOSFET from the output of digital logic. Although there are logic families that generate swings of 10 volts or more ("4000-series CMOS"), the most common logic families use levels of +5 volts ("high-speed CMOS") or +2.4 volts ("TTL"). Figure 3.67 shows how to switch loads from these three logic families. In the first circuit, the +10 volt gate drive will fully turn on any MOSFET, so we chose the VN0106, an inexpensive transistor that specifies $R_{ON} < 5$ ohms at $V_{GS} = 5$ volts. The diode protects against inductive spike (Section 1.31); the series gate resistor, though not essential, is a good idea, because MOSFET drain-gate capacitance can couple the load's inductive transients back to the delicate CMOS logic (more on this soon). In the second circuit we have 5 volts of gate drive, still fine for the VN01/VP01 series; for variety we've

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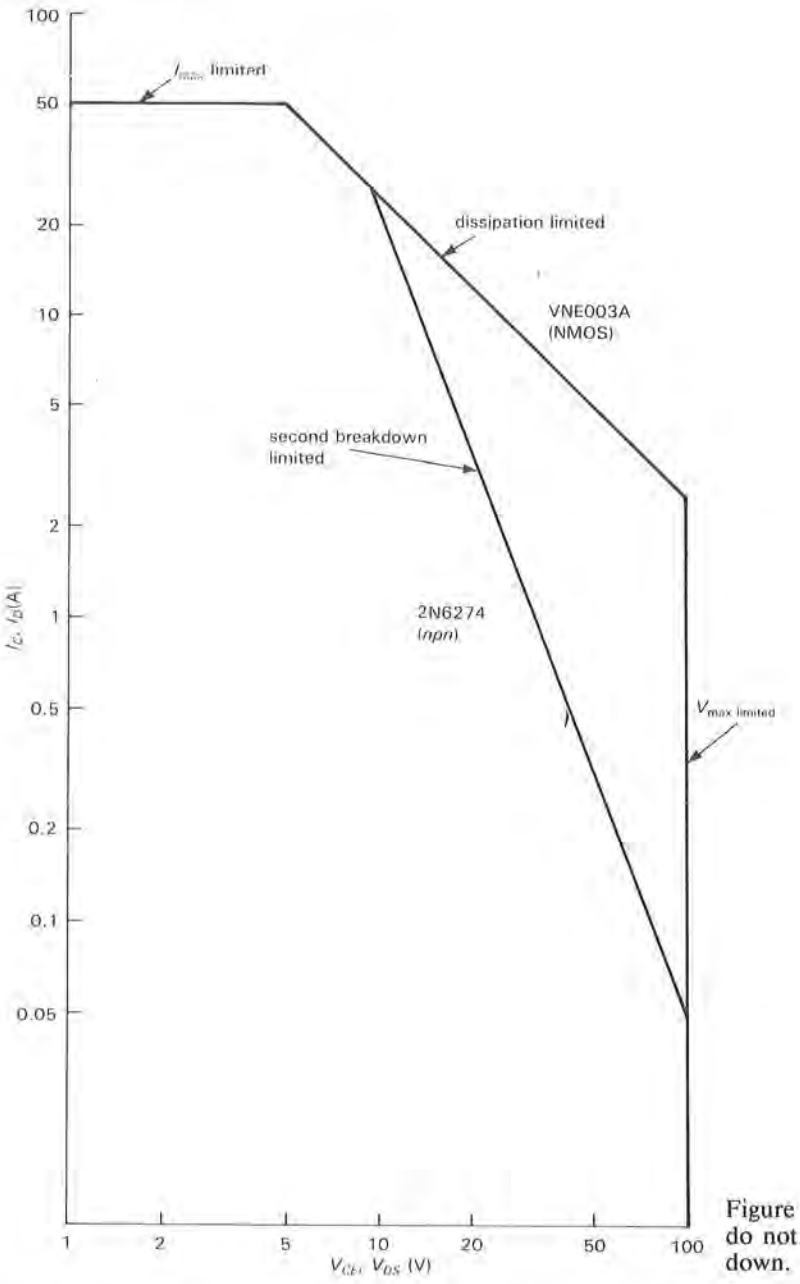


Figure 3.66. Power MOSFETs do not suffer from second breakdown.

used a *p*-channel MOSFET, driving a load returned to ground.

The last two circuits show two ways to handle the +2.4 volt (worst-case; it's usually around +3.5V) HIGH output from TTL digital logic: We can use a pullup resistor to +5 volts to generate a full +5 volt swing from the TTL output, which then drives a normal MOSFET; alternatively, we can use something like the TN0106, a "low-threshold" MOSFET designed for logic-level drive. Watch out, though, for misleading specifications. For example, the TN01 specifies "$V_{GS(\text{th})}$ =

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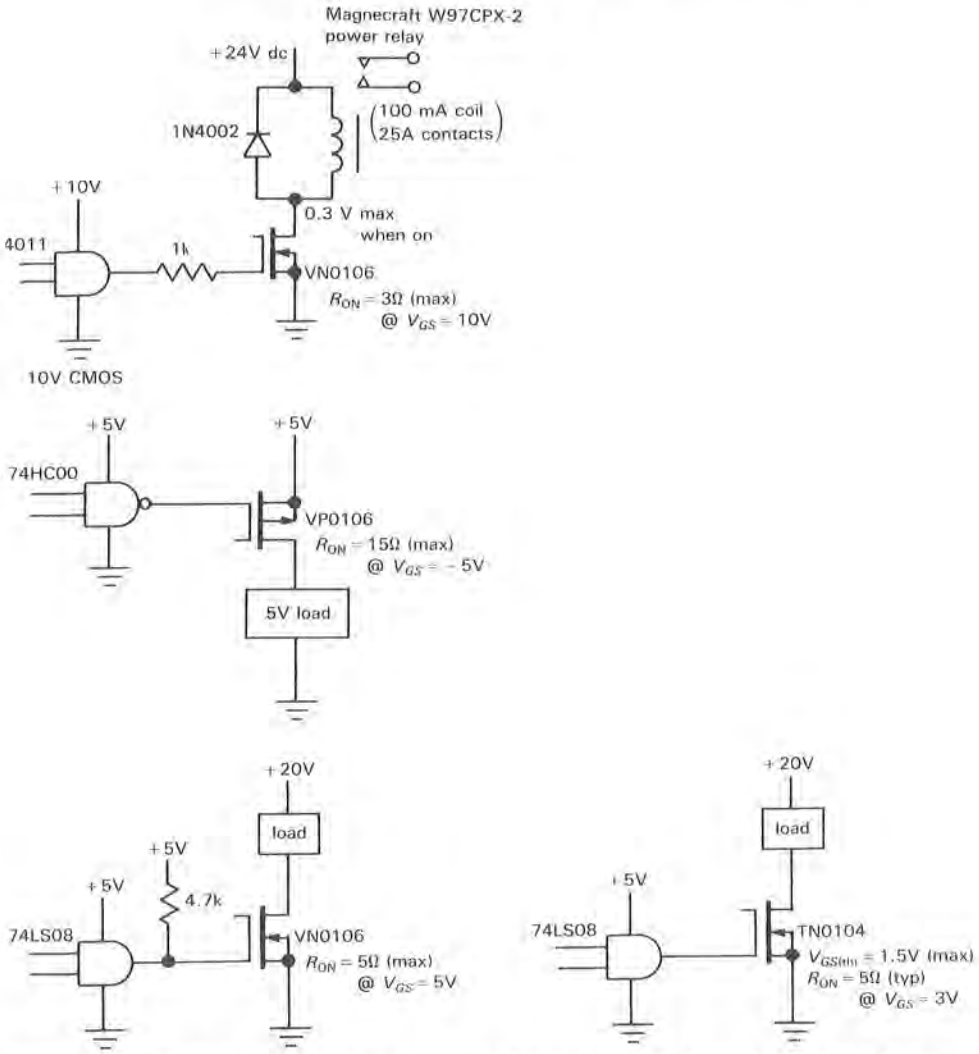


Figure 3.67. MOSFETs can switch power loads when driven from digital logic levels.

1.5 volts (max)," which sounds fine until you read the fine print ("at I_D = 1mA"). It takes considerably more gate voltage than $V_{GS(\text{th})}$ to turn the MOSFET on fully (Fig. 3.68). However, the circuit will probably work OK, because (a) a HIGH TTL output is rarely less than +3 volts, and typically more like +3.5 volts, and (b) the TN01 further specifies "R_{ON}(typ) = 5Ω at V_{GS} = 3V."

This example illustrates a frequent designer's quandary, namely a choice between a complicated circuit that meets the strict worst-case design criterion, and is therefore *guaranteed* to work, and a simple circuit that doesn't meet worst-case specifications, but is overwhelmingly likely to function without problems. There are times when you will find yourself choosing the latter, ignoring the little voice whispering into your ear.

□ *Capacitance.* In the preceding examples we put a resistor in series with the gate when there was an inductive load. As we mentioned earlier in the chapter (Section

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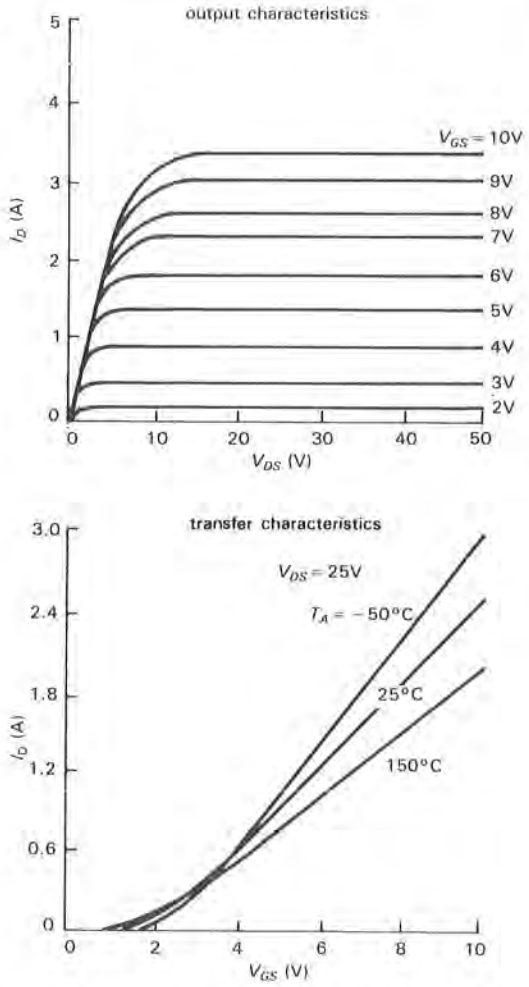


Figure 3.68. Drain characteristics of an *n*-channel low-threshold MOSFET (type TN0104).

3.09), MOSFETs have essentially infinite gate *resistance*, but finite *impedance* owing to gate-channel capacitance. With high-current MOSFETs the capacitance can be staggering: Compared with 45pF of input capacitance for the 1 amp VN01, the 10 amp IRF520 has $C_{\text{in}} = 450\text{pF}$, and the macho 70 amp SMM70N05 from Siliconix has $C_{\text{in}} = 4300\text{pF}$! A rapidly-changing drain voltage can produce milliamps of transient gate current, enough to overdrive (and even damage, via "SCR crowbarring") delicate CMOS driver chips.

The series resistance is a compromise between speed and protection, with values of 100 ohms to 10k being typical. Even without inductive loads there is dynamic gate current, of course: The capacitance to ground, C_{iss}, gives rise to $I = C_{iss}dV_{GS}/dt$, while the (smaller) feedback capacitance, C_{rss}, produces an input current $I = C_{rss}dV_{DG}/dt$. The latter may dominate in a common-source switch, because ΔV_{DG} is usually much larger than the ΔV_{GS} gate drive (Miller effect).

EXERCISE 3.19

An IRF520 MOSFET controlling a 2 amp load is switched off in 100ns (by bringing the gate from +10V to ground), during which the drain goes from 0 to 50 volts. What is the average gate current during the 100ns, assuming C_{GS} (also called C_{iss}) is 450pF, and C_{DG} (also called C_{rss}) is 50pF?

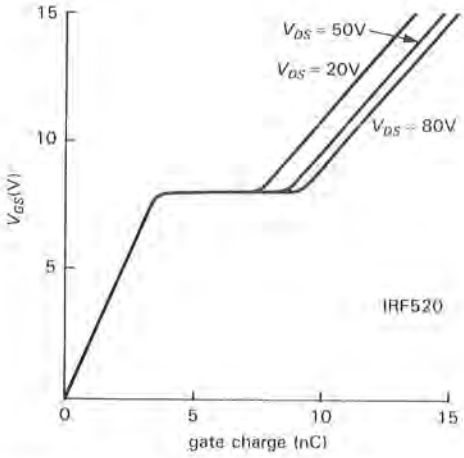


Figure 3.69. Gate charge versus V_{GS}.

In a common-source switch, the Miller-effect contribution to gate current occurs entirely during the drain transitions, whereas the gate-source capacitance causes current whenever the gate voltage is changing. These effects are often plotted as a graph of "gate charge versus gate-source voltage," as in Figure 3.69. The horizontal portion occurs at the turn-on voltage, where the rapidly falling drain forces the

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gate driver to supply additional charge to C_{rss} (Miller effect). If the feedback capacitance were independent of voltage, the horizontal portion would be proportional to drain voltage, after which the curve would continue at the previous slope. In fact, feedback capacitance C_{rss} rises rapidly at low voltage (Fig. 3.70), which means that most of the Miller effect occurs during the low-voltage portion of the drain waveform. This explains the change in slope of the gate charge curve, as well as the fact that the horizontal portion is almost independent of drain voltage.

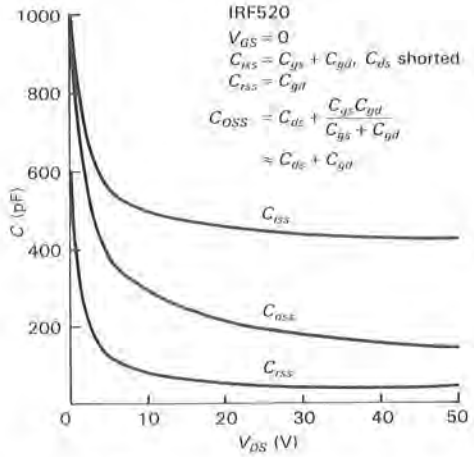


Figure 3.70. Power MOSFET capacitances.

EXERCISE 3.20

How does the voltage dependence of C_{rss} explain the change in slope of the gate charge curves?

Other cautions. Power MOSFETs have some additional idiosyncrasies you should know about. All manufacturers of power MOSFETs seem to connect the body internally to the source. Because the body forms a diode with the channel, this means that there is an effective diode from drain to source (Fig. 3.71); some manufacturers even draw the diode explicitly in their MOSFET symbol so that you won't forget. This means that you cannot use power MOSFETs bidirectionally, or at least not with more than a diode drop of reverse drain-source voltage. For example, you couldn't use a power MOSFET to zero an integrator driven with a bipolarity signal, and you couldn't use a power MOSFET as an analog switch for bipolarity signals. This problem does not occur with *integrated circuit* MOSFETs (analog switches, for example), where the body is connected to the most negative power-supply terminal.

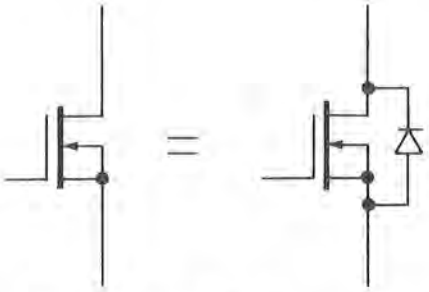


Figure 3.71. Power MOSFETs connect body to source, forming a drain-source diode.

Another trap for the unwary is the fact that gate-source breakdown voltages (±20V is a common figure) are lower than drain-source breakdown voltages (which range from 20V to 1000V). This doesn't matter if you're driving the gate from the small swings of digital logic, but you get into trouble immediately if you think you can use the drain swings of one MOSFET to drive the gate of another.

Finally, the issue of *gate protection*: As we discuss in the final section of this chapter, all MOSFET devices are extremely susceptible to gate oxide breakdown, caused by electrostatic discharge. Unlike JFETs or other junction devices, in which junction avalanche current can safely discharge the overvoltage, MOSFETs are damaged irreversibly by a single instance of gate breakdown. For this reason it is a very good idea to use gate series resistors of 1k–10k, particularly when the gate signal

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comes from another circuit board. This greatly reduces the chances of damage; it also prevents circuit loading if the gate is damaged, because the most common symptom of a damaged MOSFET is substantial dc gate current. Another precaution is to make sure you don't leave MOSFET gates unconnected, because they are much more susceptible to damage when floating (there is then no *circuit* path for

TABLE 3.5. POWER MOSFETs

BV_{DS}[a] (V)	Cont drain curr max (A)	$R_{DS(on)}$ max (Ω)	@V_{GS} (V)	$V_{GS(th)}$ max (V)	C_{iss} typ (pF)	C_{rss} typ (pF)	Turn-on charge typ (nC)	Case[b]	Type/Comments[c]
n-channel									
30	0.8	1.8	5	2.5	110	35	-	DIP-14	VQ3001J[1]; 2N, 2P in DIP
40	4	2.5	5	1.5	60	5	0.8	TO-92	TN0104N3; low threshold
60	0.2	6	5	2.5	60	5	-	TO-92	VN0610L[3]; gate protec; sim to VN2222
60	0.4	5	5	2.5	60	10	-	DIP-14	VQ1004J[1]; quad in DIP
60	15	0.14	5	2	900	180	-	TO-220	RFP15N06L[2]; low threshold
100	0.25	15	5	2.4	27	3	0.6	TO-92	VN1310N3, BSS100
100	0.8	2.5	5	2.4	70	12	2.6	TO-92	VN0210N3
100	1.3	0.3	10	4	450	50	11	DIP-4	IRFD120
100	2	1	5	2	200	20	-	TO-220	RFP2N10L[2]; low threshold
100	4	0.6	10	4	180	15	5	TO-220	IRF510, MTP4N10, VN1110N5, 2SK295
100	8	0.25	10	4	350	24	10	TO-220	IRF520, BUZ72A, 2SK383, VN1210N5
100	25	0.08	10	4	1500	90	39	TO-220	IRF540, MTP25N10
100	40	0.06	10	4	2000	350	63	TO-3	IRF150, 2N6764
100	65	0.04	10	5	5200	640	-	TO-3	VNE003A[1]
120	0.2	10	2.5	2	125	20	-	TO-92	VN1206L[1]; low threshold
200	0.1	40	5	3.5	25	3	0.5	TO-92	VN1320N3
200	0.1	24	10	2	40	5	-	TO-92	VN2020L[1], BS107
200	0.25	15	5	3	40	5	1.0	TO-92	VN0120N3, BSS101
200	0.4	8	5	3	75	7	2.5	TO-92	VN0220N3, BSS89
200	3	1.5	10	4	140	9	6	TO-220	IRF610, VN1220N5
200	5	0.8	10	4	450	40	11	TO-220	IRF620, MTP5N20, BUZ30, 2SK440
200	9	0.4	10	4	600	80	19	TO-220	IRF630, MTP8N20, BUZ32
200	18	0.18	10	4	1300	93	43	TO-220	IRF640
200	30	0.09	10	4	2600	150	80	TO-3	IRF250, 2N6766, MTM40N20
500	0.05	85	5	4	45	2	-	TO-92	VN0550N3
500	0.2	20	5	4	75	10	-	TO-92	VN0650N3
500	2.5	3	10	4	350	10	13	TO-220	IRF820, BUZ74, MTP3N50
500	4	1.5	10	4	610	18	21	TO-220	IRF830, BUZ41A, VN5001D[1], MTP4N50
500	8	0.85	10	4	1300	45	42	TO-220	IRF840, MTP8N50, 2SK555[4]
500	12	0.4	10	4	2700	75	86	TO-3	IRF450, 2N6770, 2SK560[4]
500	20	0.3	10	5	4500	100	-	TO-3	VNP006A[1]
1000	1	10	10	4.5	1200[m]	80[m]	33	TO-220	MTP1N100, BUZ50B
1000	5	3	10	4.5	2600[m]	200[m]	110	TO-3	MTM5N100, BUZ54, IRFAG50

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BV_{DS}[a] (V)	Cont drain curr max (A)	$R_{DS(on)}$ max (Ω)	@V_{GS} (V)	$V_{GS(th)}$ max (V)	C_{iss} typ (pF)	C_{rss} typ (pF)	Turn-on charge typ (nC)	Case[b]	Type/Comments[c]
p-channel									
30	0.6	2	12	4.5	150	60	-	DIP-14	VQ3001J[1]; 2N, 2P in DIP
60	0.4	5	10	4.5	150	20	-	DIP-14	VQ2004J[1]; quad in DIP
100	0.15	40	5	3.5	20	3	0.4	TO-92	VP1310N3
100	0.4	8	5	3.5	90	15	3	TO-92	VP0210N3, VP1008L[1]
100	1	0.6	10	4	300	50	16	DIP-4	IRFD9120
100	6	0.6	10	4	300	50	16	TO-220	IRF9520, VP1210N5, MTP8P10
100	19	0.2	10	4	1100	250	70	TO-220	IRF9540, MTP12P10
200	0.06	100	5	3.5	35	2	0.5	TO-92	VP1320N3
200	0.1	40	5	3.5	50	5	1	TO-92	VP0120N3, BSS92
200	3.5	4	5	3.5	600	20	10	TO-220	VP1220N5, IRF9622
200	11	0.5	10	4	1100	150	70	TO-220	IRF9640
500	0.07	150	5	5	35	3	-	TO-92	VP0550N3
500	0.1	25	5	4	75	10	-	TO-92	VP0650N3
500	1	9	5	4.5	550	20	-	TO-220	VP0350N5
500	2	6	10	4.5	1000[m]	80[m]	20	TO-220	MTP2P50

(a) BV_{GS} is ±20V, except (1) ±40V, (2) ±10V, (3) +15, -0.3V, and (4) ±15V
(b) Θ_{JA}: DIP-4=120°C/W; DIP-14=100°C/W; TO-92=200°C/W; Θ_{JC}: TO-220=2.5°C/W; TO-3=0.8°C/W.
P_{diss} @ T_{amb}=75°C: DIP-4=0.6W; DIP-14=0.8W; TO-92=0.3W; P_{diss} @ T_{case}=75°C: TO-220=30W; TO-3=90W.
(c) expect variations in characteristics between manufacturers; those shown are typical. (m) maximum.

static discharge, which otherwise provides a measure of safety). This can happen unexpectedly if the gate is driven from another circuit board. The best practice is to connect a pulldown resistor (say 100k to 1M) from gate to source of any MOSFETs whose gates are driven from an off-card signal source.

□ *MOSFETs versus BJTs as high-current switches.* Power MOSFETs are attractive alternatives to conventional power BJTs most of the time. They currently cost somewhat more, for the same capability; but they're simpler to drive, and they don't suffer from second breakdown and consequently reduced safe-operating-area (SOA) constraints (Fig. 3.66).

Keep in mind that an ON MOSFET behaves like a small resistance, rather than a saturated bipolar transistor, for small values of drain voltage. This can be an advantage, because the "saturation voltage" goes clear to zero for small drain currents. There is a general perception that MOSFETs don't saturate as well at high currents, but our research shows this to be largely false. In Table 3.6 we've chosen comparable pairs (*npn* versus *n*-channel MOSFET), for which we've looked up the specified $V_{CE(\mathrm{sat})}$ or $R_{DS(\mathrm{on})}$. The *low-current* MOSFET makes a poor showing when compared with its "small-signal" *npn* cousin, but in the range of 10–50 amps, 0–100 volts, the MOSFET does better. Note particularly the enormous base currents

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TABLE 3.6. BJT-MOSFET COMPARISON

Class	Type	I_C, I_D	V_{sat}(max) (25°C) (V)	V_{sat}(max) (125°C) (V)	I_B, V_{GS}	C_{out} (10V) max	Price (100 pc)
60V, 0.5A	NPN – 2N4400	0.5A	0.75	0.8	50mA	8pF	$0.09
	NMOS – VN0610	0.5A	2.5	4.5	10V	25pF	$0.43
60V, 10A	NPN – 2N3055	10A	3	–	3.3A	600pF	$0.65
	NMOS – MTP3055A	10A	1.5	2.3	10V	300pF	$0.57
100V, 50A	NPN – 2N6274	20A	1	1.4	2A	600pF	$11.00
	NMOS – VNE003A	20A	0.7	1.1	10V	3000pF	$12.50
400V, 15A	NPN – 2N6547	15A	1.5	2.5	2A	500pF	$4.00
	NMOS – IRF350	15A	3	6	10V	900pF	$12.60

needed to bring the bipolar power transistor into good saturation – 10% or more of the collector current (!) – compared with the (zero-current) 10 volt bias at which MOSFETs are usually specified. Note also that high-voltage MOSFETs (say, $BV_{DS} >$ 200V) tend to have larger $R_{DS(on)}$, with larger temperature coefficients, than the lower-voltage units. Along with saturation data, we've listed capacitances in the table, because power MOSFETs often have more capacitance than BJTs of the same rated current; in some applications (particularly if switching speed is important) you might want to consider the product of capacitance and saturation voltage as a figure of merit.

Remember that power MOSFETs can be used as BJT substitutes for linear power circuits, for example audio amplifiers and voltage regulators (we'll treat the latter in Chapter 6). Power MOSFETs are also available as p-channel devices, although there tends to be a greater variety available among the (better performing) n-channel devices.

Some MOSFET power switching examples. Figure 3.72 shows three ways to use a MOSFET to control the dc power to some sub-circuit that you want to turn on and off. If you have a battery-operated instrument that needs to make some measurements occasionally, you might use circuit A to switch the power-hungry microprocessor off except during those intermittent measurements. Here we've used a PMOS switch, turned on by a 5 volt logic swing to ground. The "5V logic" is micropower CMOS digital circuitry, kept running even when the microprocessor is shut off (remember, CMOS logic has zero static dissipation). We'll have much more to say about this sort of "power-switching" scheme in Chapter 14.

In the second circuit (B), we're switching dc power to a load that needs +12 volts, at considerable current; maybe it's a radio transmitter, or whatever. Because we have only a 5 volt logic swing available, we've used a small n-channel switch to generate a full 12 volt swing, which then drives the PMOS gate. Note the high-value NMOS drain resistor, perfectly adequate here because the PMOS gate draws no dc current (even a beefy 10A brute), and we don't need high switching speed in an application like this.

The third circuit (C) is an elaboration of circuit B, with short-circuit current limiting via the *pnp* transistor. That's always a good idea in power supply design, because it's easy to slip with the oscilloscope probe. In this case, the current limiting

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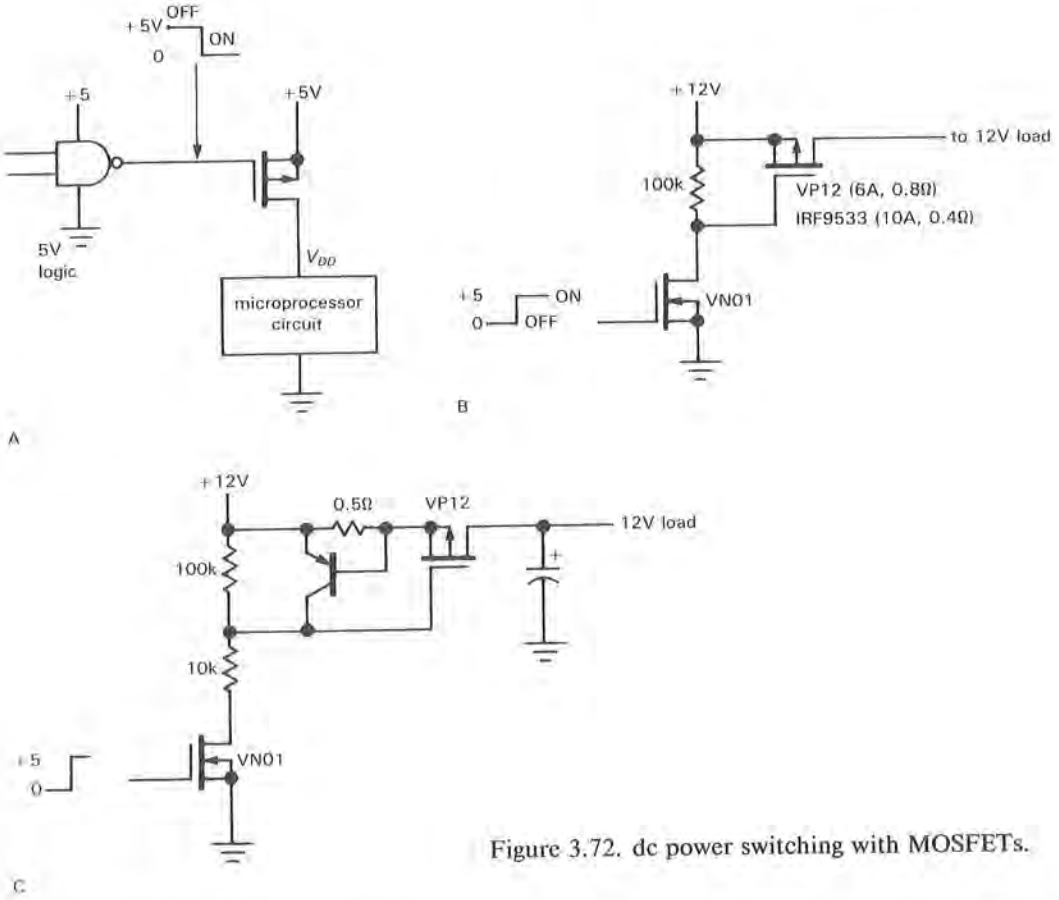


Figure 3.72. dc power switching with MOSFETs.

also prevents momentary short-circuiting of the +12 volt supply by the initially uncharged bypass capacitor. See if you can figure out how the current limiting circuit works.

EXERCISE 3.21

How does the current limiting circuit work? How much load current does it allow? Why is the NMOS drain resistor split in two?

The limited gate breakdown voltages of MOSFETs (usually ±20V) would create a real problem here if you attempted to operate the circuit from higher supply voltage. In that case you could replace the 100k resistor with 10k (allowing operation to 40V), or other appropriate ratio, always keeping the VP12 gate drive less than 20 volts.

Figure 3.73A shows a simple MOSFET switching example, one that takes advantage of the high gate impedance. You might want to turn on exterior lighting automatically at sunset. The photoresistor has low resistance in sunlight, high resistance in darkness. You make it part of a resistive divider, driving the gate directly (no dc loading!). The light goes on when the gate voltage reaches the value that produces enough drain current to close the relay. Sharp-eyed readers may have noticed that this circuit is not particularly precise or stable; that's OK, because the photoresistor undergoes an enormous change in resistance (from 10k to 10M, say) when it gets dark. The circuit's lack of a precise and stable threshold just means that the light may turn on a few minutes early or

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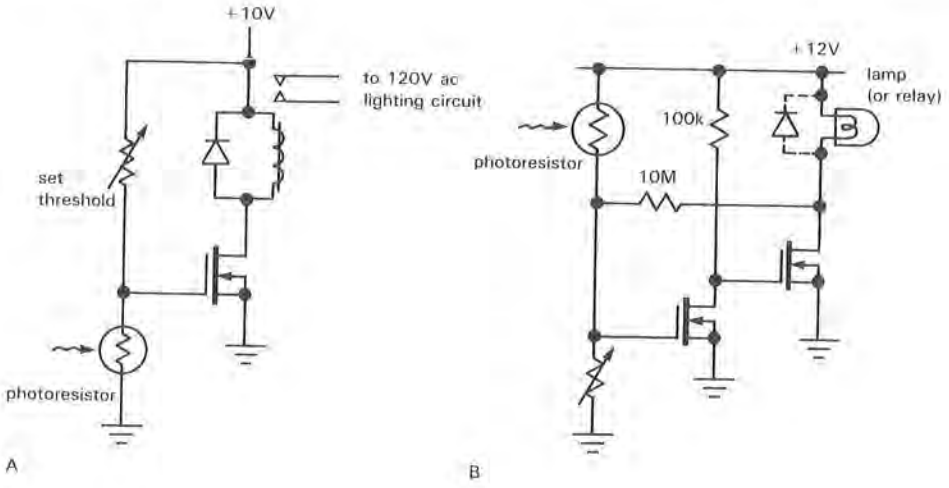


Figure 3.73. Ambient-light-controlled power switch.

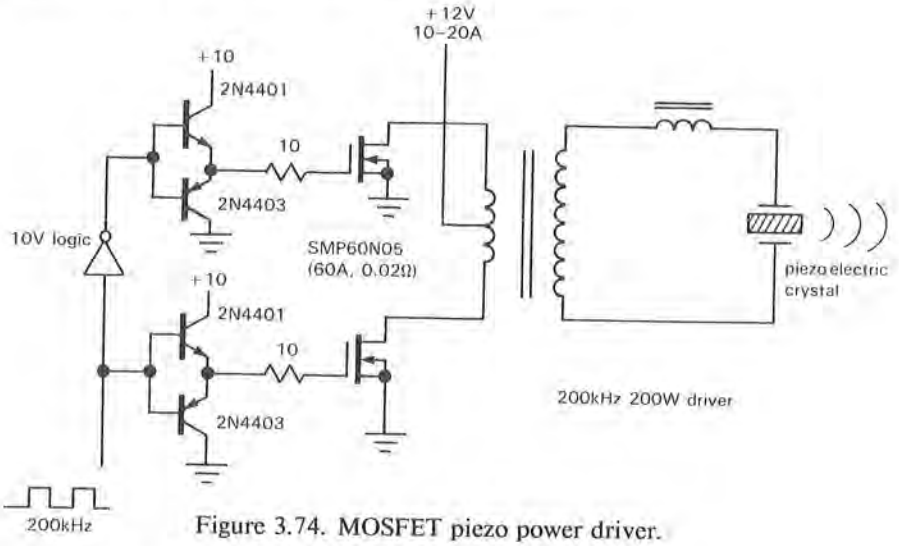


Figure 3.74. MOSFET piezo power driver.

late. Note that the MOSFET may have to dissipate some power during the time the gate bias is inching up, since we're operating in the linear region. That problem is remedied in Figure 3.73B, where a pair of cascaded MOSFETs delivers much higher gain, augmented by some positive feedback via the 10M resistor; the latter causes the circuit to snap on regeneratively as it reaches threshold.

Figure 3.74 shows a real power MOSFET job: A 200 watt amplifier to drive a piezoelectric underwater transducer at 200kHz. We've used a pair of hefty NMOS transistors, driven alternately to create ac drive in the (high-frequency) transformer primary. The bipolar push-pull gate drivers, with small gate resistors, are needed to overcome capacitive loading, since the FETs must be turned on fully in something less than a microsecond.

Finally, in Figure 3.75 we show a *linear* circuit example with power MOSFETs. Ceramic *piezoelectric* transducers are often used in optical systems to produce controlled small motions; for example,

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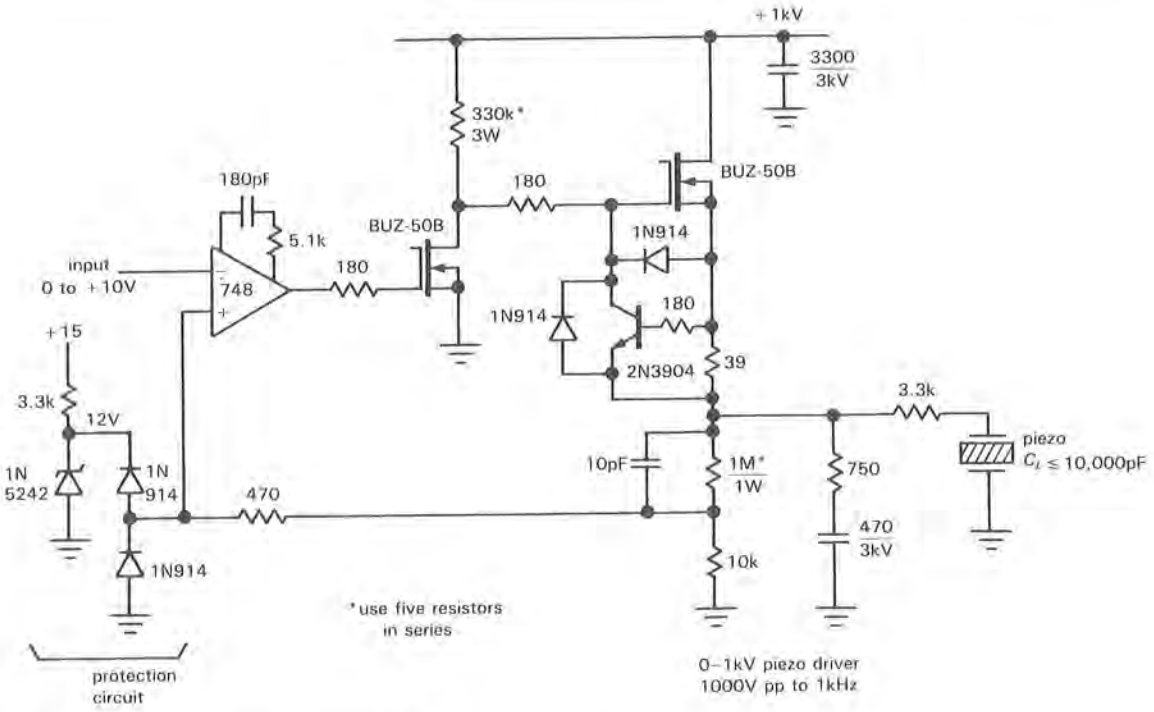


Figure 3.75. 1kV low-power piezo driver.

in *adaptive optics* you might use a piezoelectrically controlled "rubber mirror" to compensate for local variations in the index of refraction of the atmosphere. Piezo transducers are nice to use, because they're very stiff. Unfortunately, they require a kilovolt or more of voltage to produce significant motions. Furthermore, they're highly capacitive – typically 0.01μF or more – and have mechanical resonances in the kilohertz range, thus presenting a nasty load. We needed dozens of such driver amplifiers, which for some reason cost a few thousand dollars apiece if you buy them commercially. We solved our problem with the circuit shown. The BUZ-50B is an inexpensive ($4) MOSFET, good for 1kV and 2 amps. The first transistor is a common-source inverting amplifier, driving a source follower. The *npn* transistor is a current-limiter and can be a low-voltage unit, since it floats on the output. One subtle feature of the circuit is the fact that it's actually push-pull, even though it looks single-ended: You need plenty of current to push 10,000pF around at 2 volts per microsecond (how much?); the output transistor can *source* current, but the pull-down resistor can't sink enough (look back to Section 2.15, where we motivated push-pull with the same problem). In this circuit the driver transistor is the pulldown, via the gate-source diode! The rest of the circuit involves feedback (with an op-amp), a forbidden subject until the next chapter; in this case the magic of feedback makes the overall circuit linear (100V of output per volt of input), whereas without it the output voltage would depend on the (nonlinear) I_D-versus-V_{GS} characteristic of the input transistor.

3.15 MOSFET handling precautions

The MOSFET gate is insulated by a layer of glass (SiO_2) a few thousand angstroms (1Å = 0.1nm) thick. As a result it has very high resistance, and no resistive or

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junction-like path that can discharge static electricity as it is building up. In a classic situation you have a MOSFET (or MOSFET integrated circuit) in your hand. You walk over to your circuit, stick the device into its socket, and turn on the power, only to discover that the FET is dead. You killed it! You should have grabbed onto the circuit board with your other hand before inserting the device. This would have discharged your static voltage, which in winter can reach thousands of volts. MOS devices don't take kindly to "carpet shock," which is officially called *electrostatic discharge* (ESD). For purposes of static electricity, you are equivalent to 100pF in series with 1.5k; in winter your capacitor may charge to 10kV or more with a bit of shuffling about on a fluffy rug, and even a simple arm motion with shirt or sweater can generate a few kilovolts (see Table 3.7).

TABLE 3.7.
TYPICAL ELECTROSTATIC VOLTAGES[a]

Action	Electrostatic voltage 10%-20% humidity (V)	Electrostatic voltage 65%-90% humidity (V)
walk on carpet	35,000	1,500
walk on vinyl floor	12,000	250
work at bench	6,000	100
handle vinyl envelope	7,000	600
pick up poly bag	20,000	1,200
shift position on foam chair	18,000	1,500

[a] adapted from Motorola Power MOSFET Data Book.

Although any semiconductor device can be clobbered by a healthy spark, MOS devices are particularly susceptible because the energy stored in the gate-channel capacitance, when it has been brought up to breakdown voltage, is sufficient to blow a hole through the delicate gate oxide insulation. (If the spark comes from your finger, your additional 100pF only adds to the injury.) Figure 3.76 (from a series of ESD tests on a power MOSFET) shows the sort of mess this can make. Calling this "gate breakdown" gives the wrong idea; the colorful term "gate *rupture*" is closer to the mark!



high power (X1200)

Figure 3.76. Scanning electron micrograph of a 6 amp MOSFET destroyed by 1kV charge on "human body equivalent" (1.5k in series with 100pF) applied to its gate. (Courtesy of Motorola, Inc.)

The electronics industry takes ESD very seriously. It is probably the leading cause of nonfunctional semiconductors in instruments fresh off the assembly line. Books are published on the subject, and you can takes courses on it. MOS devices, as well as other susceptible semiconductors (which includes just about everything; e.g., it takes about 10 times as much voltage to zap a BJT), should be shipped in conductive foam or bags, and you have to be careful about voltages on soldering irons, etc., during fabrication. It is best to ground soldering irons, table tops, etc., and use conductive wrist straps. In addition, you can get "antistatic" carpets, upholstery, and even

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clothing (e.g., antistatic smocks containing 2% stainless steel fiber). A good antistatic workstation includes humidity control, air ionizers (to make the air slightly conductive, which keeps things from charging up), and educated workers. In spite of all this, failure rates increase dramatically in winter.

Once a semiconductor device is safely soldered into its circuit, the chances for damage are greatly reduced. In addition, most small-geometry MOS devices (e.g., CMOS logic devices, but not power MOSFETs) have protection diodes in the input gate circuits. Although the internal protection networks of resistors and clamping diodes (or sometimes zeners) compromise performance somewhat, it is often worthwhile to choose those devices because of the greatly reduced risk of damage by static electricity. In the case of unprotected devices, for example power MOSFETs, small-geometry (low current) devices tend to be the most troublesome, because their low input capacitance is easily brought to high voltage when it comes in contact with a charged 100pF human. Our personal experience with the small-geometry VN13 MOSFET has been so dismal in this regard that we no longer use it in production instruments.

It is hard to overstate the problem of gate damage due to breakdown in MOSFETs. Luckily, MOSFET designers realize the seriousness of the problem and are responding with new designs with higher BV_{GS}; for example, Motorola's new "TMOS IV" series features ±50 volt gate-source breakdown.

SELF-EXPLANATORY CIRCUITS

3.16 Circuit ideas

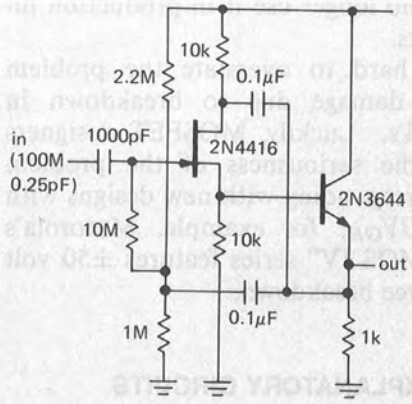
Figure 3.77 presents a sampling of FET circuit ideas.

3.17 Bad circuits

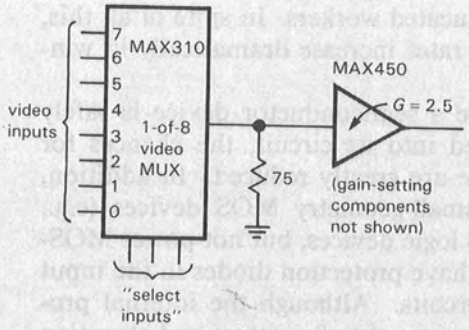
Figure 3.78 presents a collection of bad ideas, some of which involve a bit of subtlety. You'll learn a lot by figuring out why these circuits won't work.

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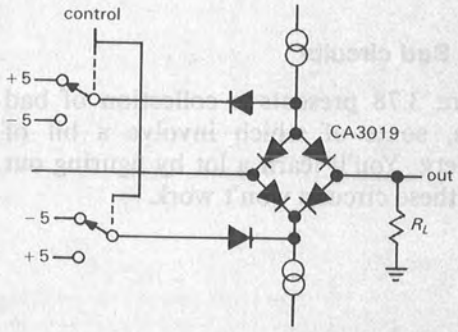
Circuit ideas



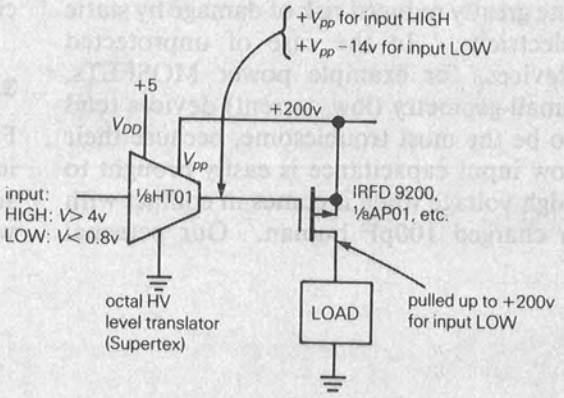
A. high-input-impedance follower



B. MOSFET video MUX with amplifier to compensate R_{on} losses.



C. signal switching using a diode bridge; alternative to FETs.



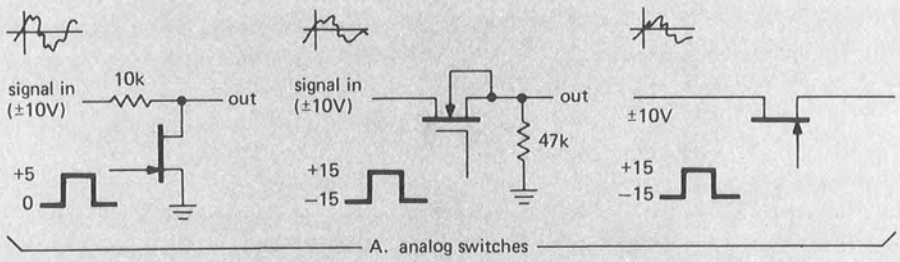
D. logic-level to *p*-channel HV switch

Figure 3.77

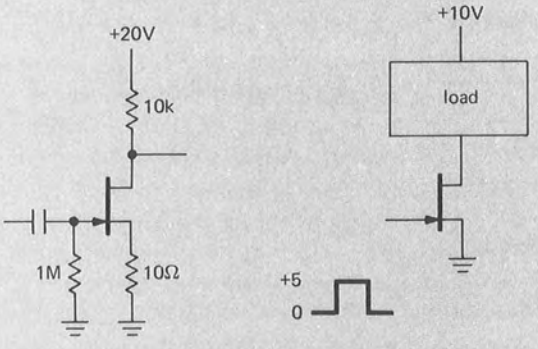
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Bad circuits

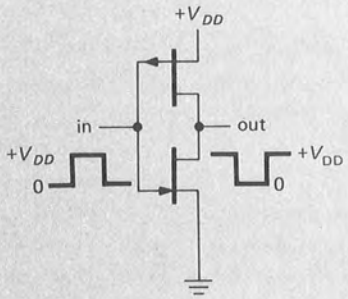


A. analog switches

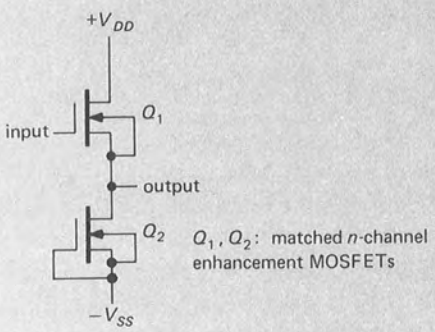


B. X1000 amplifier

C. logic switch



D. complementary JFET inverter



E. zero-offset follower

Figure 3.78

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FEEDBACK AND OPERATIONAL AMPLIFIERS

CHAPTER 4

INTRODUCTION

Feedback has become such a well-known concept that the word has entered the general vocabulary. In control systems, feedback consists in comparing the output of the system with the desired output and making a correction accordingly. The "system" can be almost anything: for instance, the process of driving a car down the road, in which the output (the position and velocity of the car) is sensed by the driver, who compares it with expectations and makes corrections to the input (steering wheel, throttle, brake). In amplifier circuits the output should be a multiple of the input, so in a feedback amplifier the input is compared with an attenuated version of the output.

4.01 Introduction to feedback

Negative feedback is the process of coupling the output back in such a way as to cancel some of the input. You might think that this would only have the effect of reducing the amplifier's gain and would be a pretty stupid thing to do. Harold S. Black, who attempted to patent negative feedback in 1928, was greeted with the same response. In his words, "Our patent application was treated in the same manner as one for a perpetual-motion machine." (See the fascinating article in *IEEE Spectrum*, December 1977.) True, it does lower the gain, but in exchange it also improves other characteristics, most notably freedom from distortion and nonlinearity, flatness of response (or conformity to some desired frequency response), and predictability. In fact, as more negative feedback is used, the resultant amplifier characteristics become less dependent on the characteristics of the open-loop (no-feedback) amplifier and finally depend only on the properties of the feedback network itself. Operational amplifiers are typically used in this *high-loop-gain* limit, with *open-loop* voltage gain (no feedback) of a million or so.

A feedback network can be frequency-dependent, to produce an equalization amplifier (with specific gain-versus-frequency characteristics, an example being the famous RIAA phono amplifier

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characteristic), or it can be amplitude-dependent, producing a nonlinear amplifier (a popular example is a logarithmic amplifier, built with feedback that exploits the logarithmic V_{BE} versus I_C of a diode or transistor). It can be arranged to produce a current source (near-infinite output impedance) or a voltage source (near-zero output impedance), and it can be connected to generate very high or very low input impedance. Speaking in general terms, the property that is sampled to produce feedback is the property that is improved. Thus, if you feed back a signal proportional to the output current, you will generate a good current source.

Feedback can also be *positive*; that's how you make an oscillator, for instance. As much fun as that may sound, it simply isn't as important as negative feedback. More often it's a nuisance, since a negative-feedback circuit may have large enough phase shifts at some high frequency to produce positive feedback and oscillations. It is surprisingly easy to have this happen, and the prevention of unwanted oscillations is the object of what is called *compensation*, a subject we will treat briefly at the end of the chapter.

Having made these general comments, we will now look at a few feedback examples with operational amplifiers.

4.02 Operational amplifiers

Most of our work with feedback will involve operational amplifiers, very high gain dc-coupled differential amplifiers with single-ended outputs. You can think of the classic long-tailed pair (Section 2.18) with its two inputs and single output as a prototype, although real op-amps have much higher gain (typically 10^5 to 10^6) and lower output impedance and allow the output to swing through most of the supply range (you usually use a split supply, most often ± 15V). Operational amplifiers are now available in literally hundreds of types, with the universal symbol shown in Figure 4.1, where the (+) and (−) inputs do as expected: The output goes positive when the noninverting input (+) goes more positive than the inverting input (−), and vice versa. The (+) and (−) symbols don't mean that you have to keep one positive with respect to the other, or anything like that; they just tell you the relative phase of the output (which is important to keep negative feedback negative). Using the words "noninverting" and "inverting," rather than "plus" and "minus," will help avoid confusion. Power-supply connections are frequently not displayed, and there is no ground terminal. Operational amplifiers have enormous voltage gain, and they are *never* (well, hardly ever) used without feedback. Think of an op-amp as fodder for feedback. The open-loop gain is so high that for any reasonable closed-loop gain, the characteristics depend only on the feedback network. Of course, at some level of scrutiny this generalization must fail. We will start with a naive view of op-amp behavior and fill in some of the finer points later, when we need to.

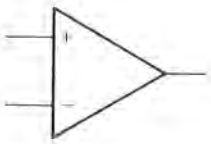


Figure 4.1

There are literally hundreds of different op-amps available, offering various performance trade-offs that we will explain later (look ahead to Table 4.1 if you want to be overwhelmed by what's available). A very good all-around performer is the popular LF411 ("411" for short), originally introduced by National Semiconductor. Like all op-amps, it is a wee beastie packaged in the so-called mini-DIP (dual in-line package), and it looks

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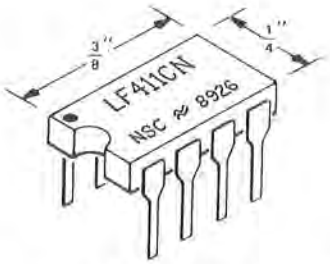


Figure 4.2. Mini-DIP integrated circuit.

as shown in Figure 4.2. It is inexpensive (about 60 cents) and easy to use; it comes in an improved grade (LF411A) and also in a mini-DIP containing two independent op-amps (LF412, called a "dual" op-amp). We will adopt the LF411 throughout this chapter as our "standard" op-amp, and we recommend it as a good starting point for your circuit designs.

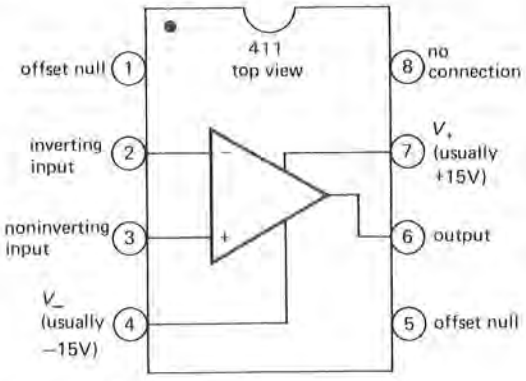


Figure 4.3

Inside the 411 is a piece of silicon containing 24 transistors (21 BJTs, 3 FETs), 11 resistors, and 1 capacitor. The pin connections are shown in Figure 4.3. The dot in the corner, or notch at the end of the package, identifies the end from which to begin counting the pin numbers. As with most electronic packages, you count pins counterclockwise, viewing from the top. The "offset null" terminals (also known as "balance" or "trim") have to do with correcting (externally) the small asymmetries that are unavoidable when making the op-amp. You will learn about this later in the chapter.

4.03 The golden rules

Here are the simple rules for working out op-amp behavior with external feedback. They're good enough for almost everything you'll ever do.

First, the op-amp voltage gain is so high that a fraction of a millivolt between the input terminals will swing the output over its full range, so we ignore that small voltage and state golden rule I:

I. The output attempts to do whatever is necessary to make the voltage difference between the inputs zero.

Second, op-amps draw very little input current (0.2nA for the LF411; picoamps for low-input-current types); we round this off, stating golden rule II:

II. The inputs draw no current.

One important note of explanation: Golden rule I doesn't mean that the op-amp actually changes the voltage at its *inputs*. It can't do that. (How could it, and be consistent with golden rule II?) What it does is "look" at its input terminals and swing its output terminal around so that the external feedback network brings the input differential to zero (if possible).

These two rules get you quite far. We will illustrate with some basic and important op-amp circuits, and these will prompt a few cautions listed in Section 4.08.

BASIC OP-AMP CIRCUITS

4.04 Inverting amplifier

Let's begin with the circuit shown in Figure 4.4. The analysis is simple, if you remember your golden rules:

1. Point B is at ground, so rule I implies that point A is also.

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2. This means that (a) the voltage across R_2 is V_{out} and (b) the voltage across R_1 is V_{in}.

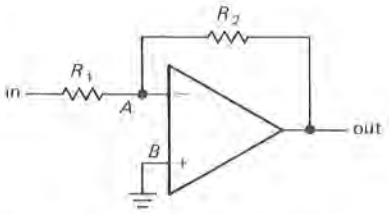


Figure 4.4. Inverting amplifier.

3. So, using rule II, we have

$$V_{out}/R_2 = -V_{in}/R_1$$

In other words,

$$\text{voltage gain} = V_{out}/V_{in} = -R_2/R_1$$

Later you will see that it's often better not to ground B directly, but through a resistor. However, don't worry about that now.

Our analysis seems almost too easy! In some ways it obscures what is actually happening. To understand how feedback works, just imagine some input level, say +1 volt. For concreteness, imagine that R_1 is 10k and R_2 is 100k. Now, suppose the output decides to be uncooperative, and sits at zero volts. What happens? R_1 and R_2 form a voltage divider, holding the inverting input at +0.91 volt. The op-amp sees an enormous input unbalance, forcing the output to go negative. This action continues until the output is at the required −10.0 volts, at which point both op-amp inputs are at the same voltage, namely ground. Similarly, any tendency for the output to go more negative than −10.0 volts will pull the inverting input below ground, forcing the output voltage to rise.

What is the input impedance? Simple. Point A is always at zero volts (it's called a *virtual ground*). So $Z_{in} = R_1$. At this point you don't yet know how to figure the output impedance; for this circuit, it's a fraction of an ohm.

Note that this analysis is true even for dc – it's a dc amplifier. So if you have a signal source offset from ground (collector of a previous stage, for instance), you may want to use a coupling capacitor (sometimes called a blocking capacitor, since it blocks dc but couples the signal). For reasons you will see later (having to do with departures of op-amp behavior from the ideal), it is usually a good idea to use a blocking capacitor if you're only interested in ac signals anyway.

This circuit is known as an *inverting amplifier*. Its one undesirable feature is the low input impedance, particularly for amplifiers with large (closed-loop) voltage gain, where R_1 tends to be rather small. That is remedied in the next circuit (Fig. 4.5).

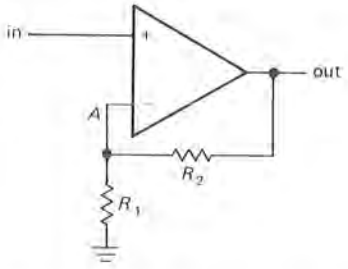


Figure 4.5. Noninverting amplifier.

4.05 Noninverting amplifier

Consider Figure 4.5. Again, the analysis is simplicity itself:

$$V_A = V_{in}$$

But V_A comes from a voltage divider:

$$V_A = V_{out}R_1/(R_1 + R_2)$$

Set $V_A = V_{in}$, and you get

$$\text{gain} = V_{out}/V_{in} = 1 + R_2/R_1$$

This is a *noninverting amplifier*. In the approximation we are using, the input impedance is infinite (with the 411 it would be $10^{12}\Omega$ or more; a bipolar op-amp

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will typically exceed $10^8\Omega$). The output impedance is still a fraction of an ohm. As with the inverting amplifier, a detailed look at the voltages at the inputs will persuade you that it works as advertised.

Once again we have a dc amplifier. If the signal source is ac-coupled, you must provide a return to ground for the (very small) input current, as in Figure 4.6. The component values shown give a voltage gain of 10 and a low-frequency 3dB point of 16Hz.

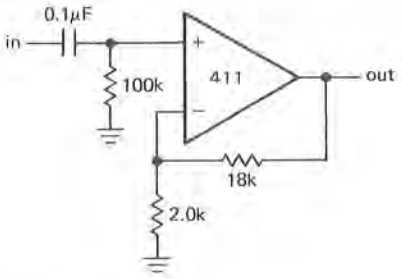


Figure 4.6

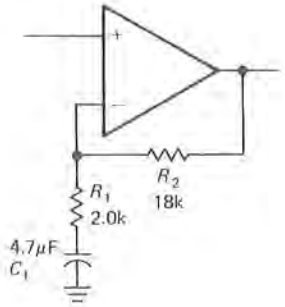


Figure 4.7

An ac amplifier

Again, if only ac signals are being amplified, it is often a good idea to "roll off" the gain to unity at dc, especially if the amplifier has large voltage gain, in order to reduce the effects of finite "input offset voltage." The circuit in Figure 4.7 has a low-frequency 3dB point of 17Hz, the frequency at which the impedance of the capacitor equals 2.0k. Note the large capacitor value required. For noninverting amplifiers with high gain, the capacitor in this ac amplifier configuration may be undesirably large. In that case it may be preferable to omit the capacitor and trim the offset voltage to zero, as we will discuss later (Section 4.12). An alternative is to raise R_1 and R_2, perhaps using a T network for the latter (Section 4.18).

In spite of its desirable high input impedance, the noninverting amplifier configuration is not necessarily to be preferred over the inverting amplifier configuration in all circumstances. As we will see later, the inverting amplifier puts less demand on the op-amp and therefore gives somewhat better performance. In addition, its virtual ground provides a handy way to combine several signals without interaction. Finally, if the circuit in question is driven from the (stiff) output of another op-amp, it makes no difference whether the input impedance is 10k (say) or infinity, because the previous stage has no trouble driving it in either case.

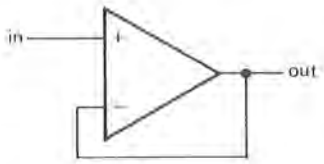


Figure 4.8. Follower.

4.06 Follower

Figure 4.8 shows the op-amp version of an emitter follower. It is simply a noninverting amplifier with R_1 infinite and R_2 zero (gain = 1). There are special op-amps, usable only as followers, with improved characteristics (mainly higher speed), e.g., the LM310 and the OPA633, or with simplified connections, e.g., the TL068 (which comes in a 3-pin transistor package).

An amplifier of unity gain is sometimes called a *buffer* because of its isolating

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properties (high input impedance, low output impedance).

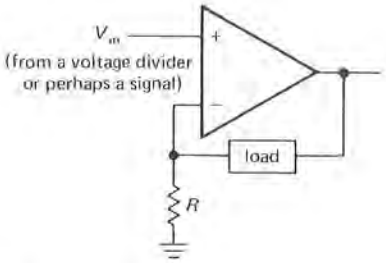


Figure 4.9

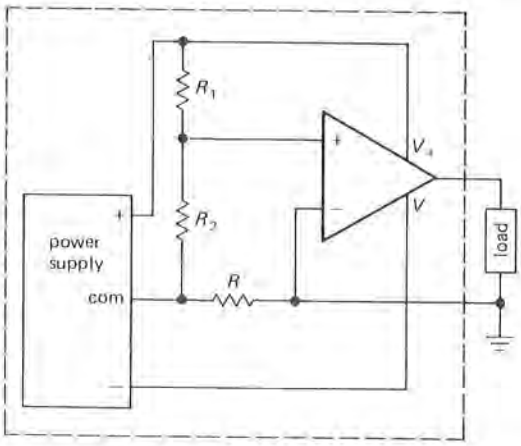


Figure 4.10. Current source with grounded load and floating power supply.

4.07 Current sources

The circuit in Figure 4.9 approximates an ideal current source, without the V_{BE} offset of a transistor current source. Negative feedback results in V_{in} at the inverting input, producing a current $I = V_{\text{in}}/R$ through the load. The major disadvantage of this circuit is the "floating" load (neither side grounded). You couldn't generate a usable sawtooth wave with respect to ground with this current source, for instance. One solution is to float the whole circuit (power supplies and all) so that you can ground one side of the load (Fig. 4.10).

The circuit in the box is the previous current source, with its power supplies shown explicitly. R_1 and R_2 form a voltage divider to set the current. If this circuit seems confusing, it may help to remind yourself that "ground" is a relative concept. Any one point in a circuit could be called ground. This circuit is useful for generating currents into a load that is returned to ground, but it has the disadvantage that the control input is now floating, so you cannot program the output current with an input voltage referenced to ground. Some solutions to this problem are presented in Chapter 6 in the discussion of constant-current power supplies.

Current sources for loads returned to ground

With an op-amp and external transistor it is possible to make a simple high-quality current source for a load returned to ground; a little additional circuitry makes it possible to use a programming input referenced to ground (Fig. 4.11). In the first circuit, feedback forces a voltage $V_{CC} - V_{\text{in}}$ across R, giving an emitter current (and therefore an output current) $I_E = (V_{CC} - V_{\text{in}})/R$. There are no V_{BE} offsets, or their variations with temperature, I_C, V_{CE}, etc., to worry about. The current source is imperfect (ignoring op-amp errors: I_b, V_{os}) only insofar as the small base current may vary somewhat with V_{CE} (assuming the op-amp draws no input current), not too high a price to pay for the convenience of a grounded load; a Darlington for Q_1 would reduce this error considerably. This error comes about, of course, because the op-amp stabilizes the *emitter* current, whereas the load sees the *collector* current. A variation of this circuit, using a FET instead of a bipolar transistor, avoids this problem altogether, since FETs draw no gate current.

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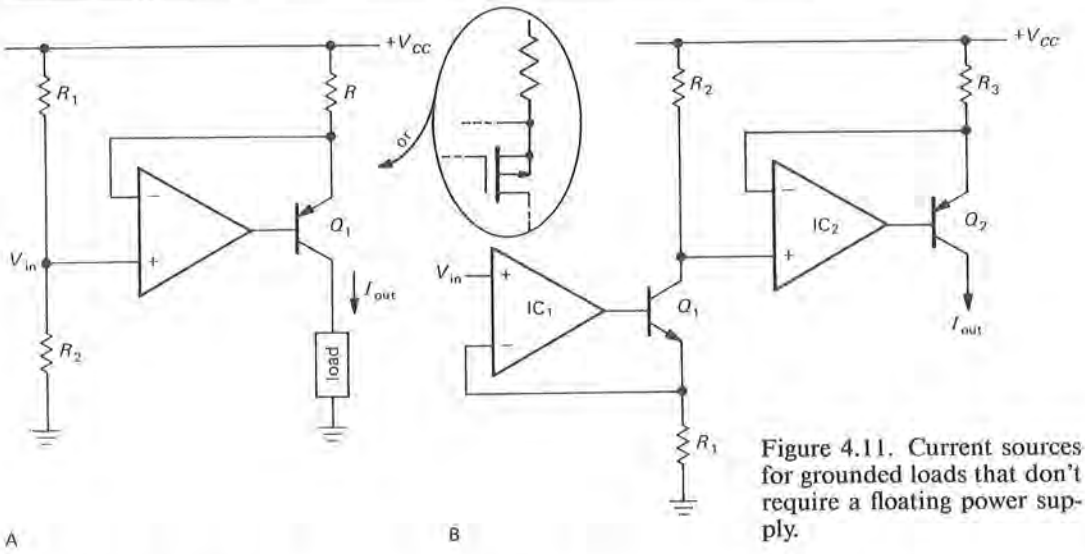


Figure 4.11. Current sources for grounded loads that don't require a floating power supply.

With this circuit the output current is proportional to the voltage drop below V_{CC} applied to the op-amp's noninverting input; in other words, the programming voltage is referenced to V_{CC}, which is fine if V_{in} is a fixed voltage generated by a voltage divider, but an awkward situation if an external input is to be used. This is remedied in the second circuit, in which a similar current source with *npn* transistor is used to convert an input voltage (referenced to ground) to a V_{CC}-referenced input to the final current source. Op-amps and transistors are inexpensive. Don't hesitate to use a few extra components to improve performance or convenience in circuit design.

One important note about the last circuit: The op-amp must be able to operate with its inputs near or at the positive supply voltage. An op-amp like the 307, 355, or OP-41 is good here. Alternatively, the op-amp could be powered from a separate V_+ voltage higher than V_{CC}.

EXERCISE 4.1

What is the output current in the last circuit for a given input voltage V_{in}?

Figure 4.12 shows an interesting variation on the op-amp/transistor current source. It has the advantage of zero base current error, which you get with FETs, without being restricted to output currents less than $I_{DS(\text{ON})}$. In this circuit (actually a current *sink*), Q_2 begins to conduct when Q_1 is drawing about 0.6mA drain current. With Q_1's minimum I_{DSS}

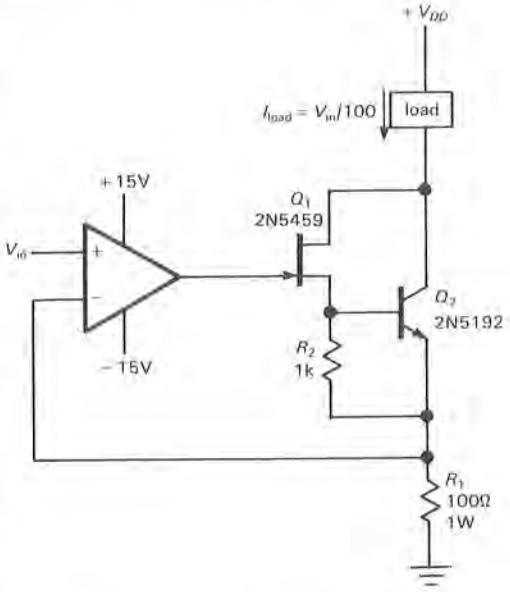


Figure 4.12. FET/bipolar current source suitable for high currents.

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of 4mA and a reasonable value for Q_2's beta, load currents of 100mA or more can be generated (Q_2 can be replaced by a Darlington for much higher currents, and in that case R_1 should be reduced accordingly). We've used a JFET in this particular circuit, although a MOSFET would be fine; in fact, it would be better, since with a JFET (which is a depletion-mode device) the op-amp must be run from split supplies to ensure a gate voltage range sufficient for pinch-off. It's worth noting that you can get plenty of current with a simple power MOSFET ("VMOS"); but the high interelectrode capacitances of power FETs may cause problems that you avoid with the hybrid circuit here.

Howland current source

Figure 4.13 shows a nice "textbook" current source. If the resistors are chosen so that $R_3/R_2 = R_4/R_1$, then it can be shown that $I_{\text{load}} = -V_{\text{in}}/R_2$.

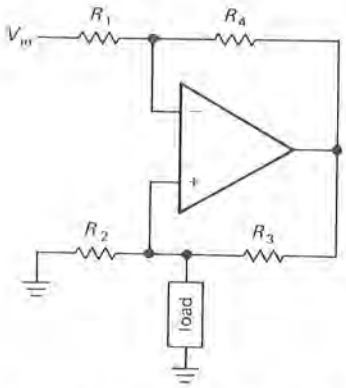


Figure 4.13. Howland current source.

EXERCISE 4.2
Show that the preceding result is correct.

This sounds great, but there's a hitch: The resistors must be matched exactly; otherwise it isn't a perfect current source. Even so, its performance is limited by the CMRR of the op-amp. For large output currents, the resistors must be small, and the compliance is limited. Also, at high frequencies (where the loop gain is low, as we'll learn shortly) the output impedance can drop from the desired value of infinity to as little as a few hundred ohms (the op-amp's open-loop output impedance). As clever as it looks, the Howland current source is not widely used.

4.08 Basic cautions for op-amp circuits

1. In all op-amp circuits, golden rules I and II (Section 4.03) will be obeyed only if the op-amp is in the active region, i.e., inputs and outputs not saturated at one of the supply voltages.

For instance, overdriving one of the amplifier configurations will cause output clipping at output swings near V_{CC} or V_{EE}. During clipping, the inputs will no longer be maintained at the same voltage. The op-amp output cannot swing beyond the supply voltages (typically it can swing only to within 2V of the supplies, though certain op-amps are designed to swing all the way to one supply or the other). Likewise, the output compliance of an op-amp current source is set by the same limitation. The current source with floating load, for instance, can put a maximum of $V_{CC} - V_{\text{in}}$ across the load in the "normal" direction (current in the same direction as applied voltage) and $V_{\text{in}} - V_{EE}$ in the reverse direction (the load could be rather strange, e.g., it might contain batteries, requiring the reverse sense of voltage to get a forward current; the same thing might happen with an inductive load driven by changing currents).

2. The feedback must be arranged so that it is negative. This means (among other things) that you must not mix up the inverting and noninverting inputs.

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3. There must always be feedback at dc in an op-amp circuit. Otherwise the op-amp is guaranteed to go into saturation.

For instance, we were able to put a capacitor from the feedback network to ground in the noninverting amplifier (to reduce gain at dc to 1, Fig. 4.7), but we could not similarly put a capacitor in series between the output and the inverting input.

4. Many op-amps have a relatively small maximum differential input voltage limit. The maximum voltage difference between the inverting and noninverting inputs might be limited to as little as 5 volts in either polarity. Breaking this rule will cause large input currents to flow, with degradation or destruction of the op-amp.

We will take up some more issues of this type in Section 4.11 and again in Section 7.06 in connection with precision circuit design.

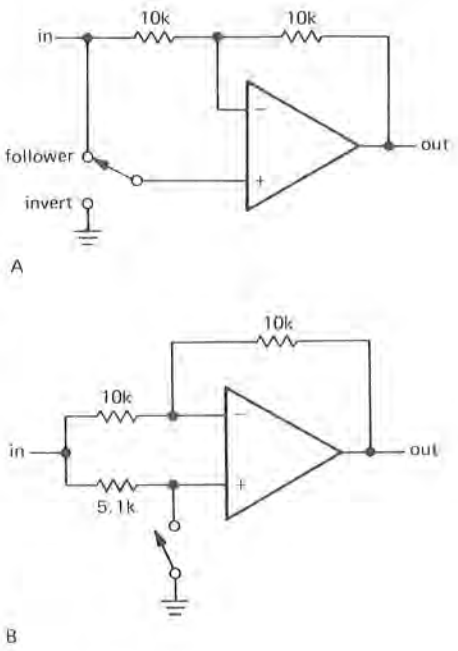


Figure 4.14

AN OP-AMP SMORGASBORD

In the following examples we will skip the detailed analysis, leaving that fun for you, the reader.

4.09 Linear circuits

Optional inverter

The circuits in Figure 4.14 let you invert, or amplify without inversion, by flipping a switch. The voltage gain is either +1 or −1, depending on the switch position.

EXERCISE 4.3
Show that the circuits in Figure 4.14 work as advertised.

Follower with bootstrap

As with transistor amplifiers, the bias path can compromise the high input impedance you would otherwise get with an op-amp,

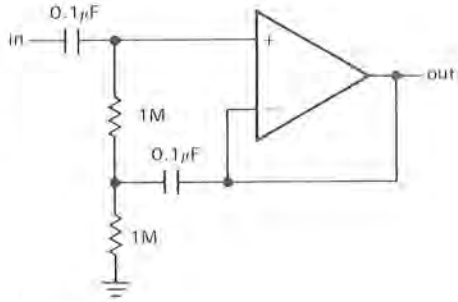


Figure 4.15

particularly with ac-coupled inputs, where a resistor to ground is mandatory. If that is a problem, the bootstrap circuit shown in Figure 4.15 is a possible solution. As in the transistor bootstrap circuit (Section 2.17), the 0.1μF capacitor makes the upper 1M resistor look like a high-impedance current source to input signals. The low-frequency rolloff for this circuit will begin at about 10Hz, dropping at 12dB per octave for frequencies somewhat below this. Note: You might be tempted to

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reduce the input coupling capacitor, since its load has been bootstrapped to high impedance. However, this can generate a peak in the frequency response, in the manner of an active filter (see Section 5.06).

Ideal current-to-voltage converter

Remember that the humble resistor is the simplest I-to-V converter. However, it has the disadvantage of presenting a nonzero impedance to the source of input current; this can be fatal if the device providing the input current has very little compliance or does not produce a constant current as the output voltage changes. A good example is a *photovoltaic cell*, a fancy name for a sun battery. Even the garden-variety signal diodes you use in circuits have a small photovoltaic effect (there are amusing stories of bizarre circuit behavior finally traced to this effect). Figure 4.16 shows the good way to convert current

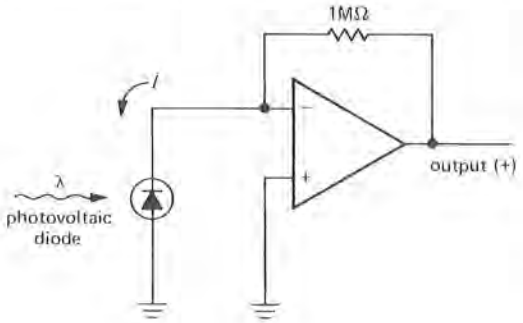


Figure 4.16

to voltage while holding the input strictly at ground. The inverting input is a virtual ground; this is fortunate, since a photovoltaic diode can generate only a few tenths of a volt. This particular circuit has an output of 1 volt per microamp of input current. (With BJT-input op-amps you sometimes see a resistor connected between the noninverting input and ground; its function will be explained shortly in connection with op-amp shortcomings.)

Of course, this *transresistance* configuration can be used equally well for devices that source their current via some positive excitation voltage, such as V_{CC}. Photomultiplier tubes and phototransistors (both devices that source current from a positive supply when exposed to light) are often used this way (Fig. 4.17).

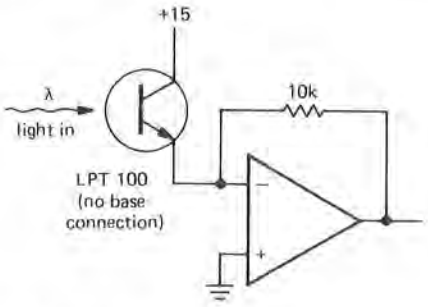


Figure 4.17

EXERCISE 4.4

Use a 411 and a 1mA (full scale) meter to construct a "perfect" current meter (i.e., one with zero input impedance) with 5mA full scale. Design the circuit so that the meter will never be driven more than ±150% full scale. Assume that the 411 output can swing to ±13 volts (±15V supplies) and that the meter has 500 ohms internal resistance.

Differential amplifier

The circuit in Figure 4.18 is a differential amplifier with gain R_2/R_1. As with the current source that used matched resistor ratios, this circuit requires precise resistor matching to achieve high common-mode rejection ratios. The best procedure is to stock up on a bunch of 100k 0.01% resistors next time you have a chance. All your differential amplifiers will have unity gain, but that's easily remedied with further (single-ended) stages of gain. We will treat differential amplifiers in more detail in Chapter 7.

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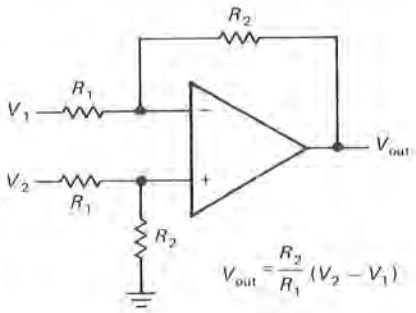


Figure 4.18. Classic differential amplifier.

Summing amplifier

The circuit shown in Figure 4.19 is just a variation of the inverting amplifier. Point X is a virtual ground, so the input current is $V_1/R + V_2/R + V_3/R$. That gives $V_{out} = -(V_1 + V_2 + V_3)$. Note that the inputs can be positive or negative. Also, the input resistors need not be equal; if they're unequal, you get a weighted sum. For instance, you could have four inputs, each of which is +1 volt or zero, representing binary values 1, 2, 4, and 8. By using input resistors of 10k, 5k, 2.5k, and 1.25k you will get an output in volts equal to the binary count input. This scheme can be easily expanded to several digits. It is the basis of digital-to-analog conversion, although a different input circuit (an $R-2R$ ladder) is usually used.

EXERCISE 4.5

Show how to make a two-digit digital-to-analog converter by appropriately scaling the input resistors in a summing amplifier. The digital input represents two digits, each consisting of four lines that represent the values 1, 2, 4, and 8 for the respective digits. An input line is either at +1 volt or at ground, i.e., the eight input lines represent 1, 2, 4, 8, 10, 20, 40, and 80. Because op-amp outputs generally cannot swing beyond ±13 volts, you will have to settle for an output in volts equal to one-tenth the value of the input number.

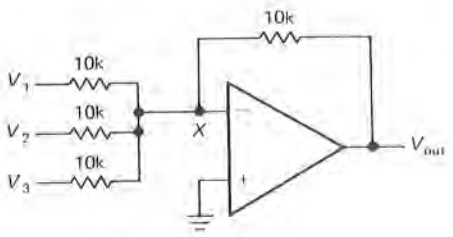


Figure 4.19

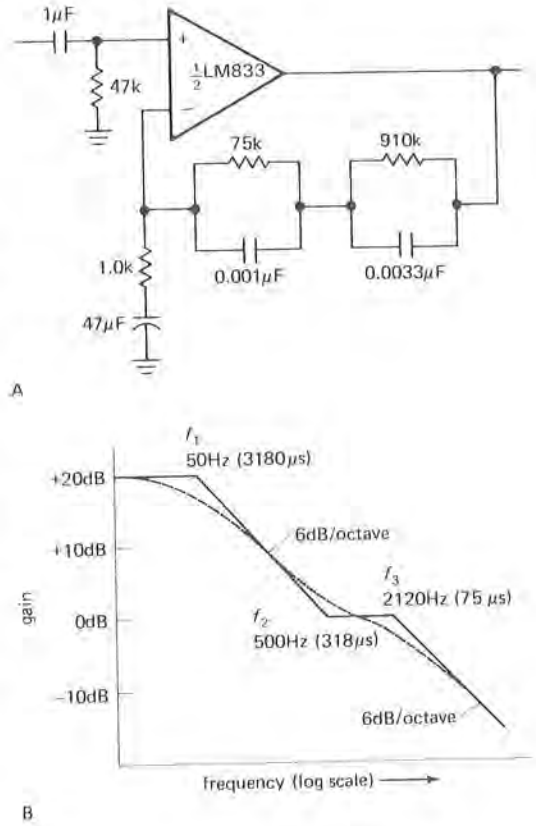


Figure 4.20. Op-amp RIAA phono playback amplifier.

RIAA preamp

The RIAA preamp is an example of an amplifier with a specifically tailored frequency response. Phonograph records are cut with approximately flat amplitude characteristics; magnetic pickups, on the other hand, respond to velocity, so a playback amplifier with rising bass response is required.

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The circuit shown in Figure 4.20 produces the required response. The RIAA playback amplifier frequency response (relative to 0dB at 1kHz) is shown in the graph, with the breakpoints given in terms of time constants. The 47μF capacitor to ground rolls off the gain to unity at dc, where it would otherwise be about 1000; as we have hinted earlier, the reason is to avoid amplification of dc input "offsets." The LM833 is a low-noise dual op-amp intended for audio applications (a "gold-plated" op-amp for this application is the ultra-low-noise LT1028, which is 13dB quieter, and 10dB more expensive, than the 833!).

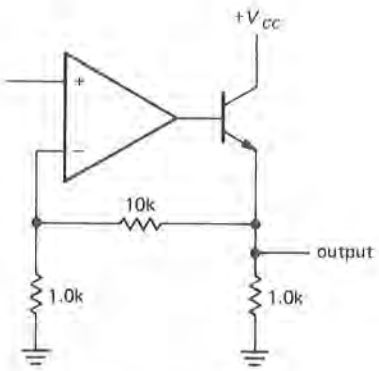


Figure 4.21

Power booster

For high output current, a power transistor follower can be hung on an op-amp output (Fig. 4.21). In this case a noninverting amplifier has been drawn; the follower can be added to any op-amp configuration. Notice that feedback is taken from the emitter; thus, feedback enforces the desired output voltage in spite of the V_{BE} drop. This circuit has the usual problem that the follower output can only *source* current. As with transistor circuits, the remedy is a push-pull booster (Fig. 4.22). You will see later that the limited speed with which the op-amp can move its output (slew rate) seriously limits the speed

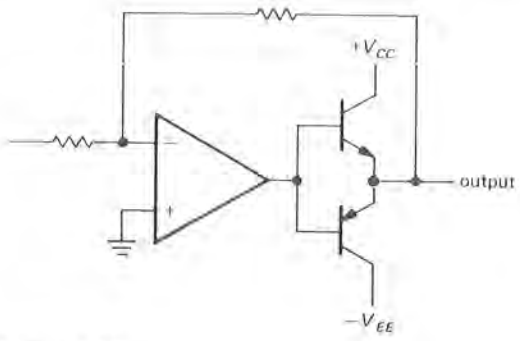


Figure 4.22

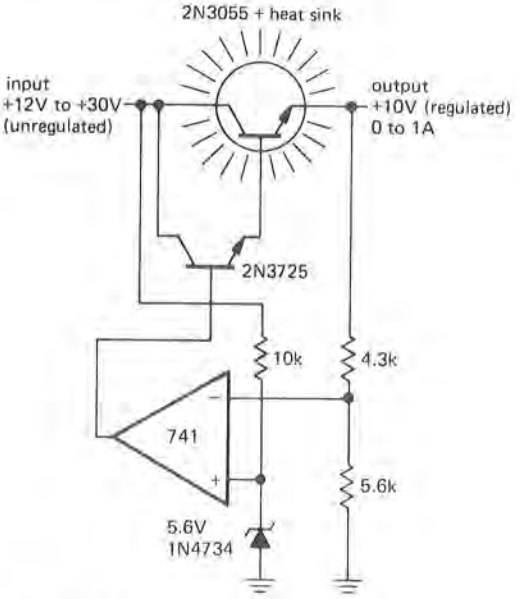


Figure 4.23

of this booster in the crossover region, creating distortion. For slow-speed applications you don't need to bias the push-pull pair into quiescent conduction, because feedback will take care of most of the crossover distortion. Commercial op-amp power boosters are available, e.g., the LT1010, OPA633, and 3553. These are unity-gain push-pull amplifiers capable of 200mA of output current and operation to 100MHz and above. You can include them inside the feedback loop without any worries (See Table 7.4).

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Power supply

An op-amp can provide the gain for a feedback voltage regulator (Fig. 4.23). The op-amp compares a sample of the output with the zener reference, changing the drive to the Darlington "pass transistor" as needed. This circuit supplies 10 volts regulated, at up to 1 amp load current. Some notes about this circuit:

1. The voltage divider that samples the output could be a potentiometer, for adjustable output voltage.

2. For reduced ripple at the zener, the 10k resistor should be replaced by a current source. Another approach is to bias the zener from the output; that way you take advantage of the regulator you have built. Caution: When using this trick, you must analyze the circuit carefully to be sure it will start up when power is first applied.

3. The circuit as drawn could be damaged by a temporary short circuit across the output, because the op-amp would attempt to drive the Darlington pair into heavy conduction. Regulated power supplies should always have circuitry to limit "fault" current (see Section 6.05 for more details).

4. Integrated circuit voltage regulators are available in tremendous variety, from the time-honored 723 to the convenient 3-terminal adjustable regulators with internal current limit and thermal shutdown (see Tables 6.8–6.10). These devices, complete with temperature-compensated internal zener reference and pass transistor, are so easy to use that you will almost never use a general-purpose op-amp as a regulator. The exception might be to generate a stable voltage within a circuit that already has a stable power-supply voltage available.

In Chapter 6 we will discuss voltage regulators and power supplies in detail, including special ICs intended for use as voltage regulators.

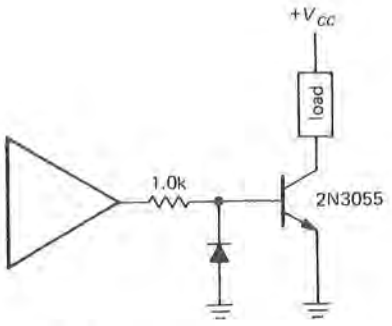


Figure 4.24

4.10 Nonlinear circuits

Power-switching driver

For loads that are either on or off, a switching transistor can be driven from an op-amp. Figure 4.24 shows how. Note the diode to prevent reverse base-emitter breakdown (op-amps easily swing more than −5V). The 2N3055 is everyone's power transistor for noncritical high-current applications. A Darlington (or power MOSFET) can be used if currents greater than about 1 amp need to be driven.

Active rectifier

Rectification of signals smaller than a diode drop cannot be done with a simple diode-resistor combination. As usual, op-amps come to the rescue, in this case by putting a diode in the feedback loop (Fig. 4.25). For V_{in} positive, the diode provides negative feedback; the output follows the input, coupled by the diode, but without a V_{BE} drop. For V_{in} negative, the op-amp goes into negative saturation and V_{out} is at ground. R could be chosen smaller for lower output impedance, with the tradeoff of higher op-amp output current. A better solution is to use an op-amp follower at the output, as shown, to produce very low output impedance regardless of the resistor value.

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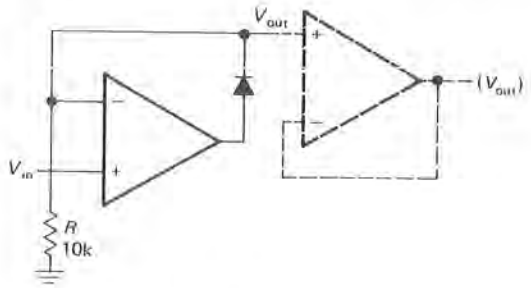


Figure 4.25. Simple active rectifier.

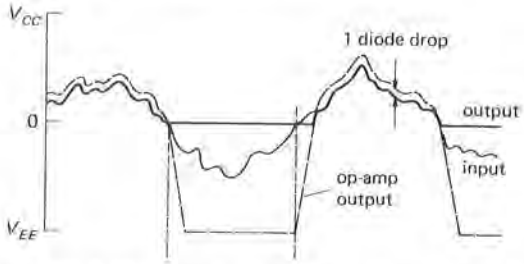


Figure 4.26. Effect of finite slew rate on the simple active rectifier.

There is a problem with this circuit that becomes serious with high-speed signals. Because an op-amp cannot swing its output infinitely fast, the recovery from negative saturation (as the input waveform passes through zero from below) takes some time, during which the output is incorrect. It looks something like the curve shown in Figure 4.26. The output (heavy line) is an accurate rectified version of the input (light line), except for a short time interval after the input rises through zero volts. During that interval the op-amp output is racing up from saturation near $-V_{EE}$, so the circuit's output is still at ground. A general-purpose op-amp like the 411 has a *slew rate* (maximum rate at which the output can change) of 15 volts per microsecond; recovery from negative saturation therefore takes about 1μs, which may introduce significant output error for fast signals. A circuit modification improves the situation considerably (Fig. 4.27).

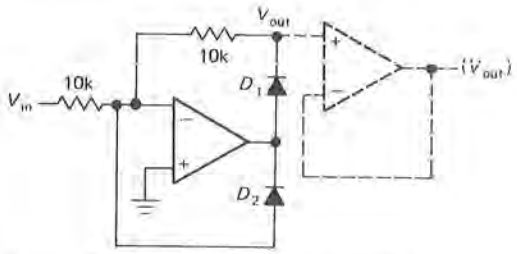


Figure 4.27. Improved active rectifier.

D_1 makes the circuit a unity-gain inverter for negative input signals. D_2 clamps the op-amp's output at one diode drop below ground for positive inputs, and since D_1 is then back-biased, V_{out} sits at ground. The improvement comes because the op-amp's output swings only two diode drops as the input signal passes through zero. Since the op-amp output has to slew only about 1.2 volts instead of V_{EE} volts, the "glitch" at zero crossings is reduced more than tenfold. This rectifier is inverting, incidentally. If you require a noninverted output, attach a unity-gain inverter to the output.

The performance of these circuits is improved if you choose an op-amp with a high slew rate. Slew rate also influences the performance of the other op-amp applications we've discussed, for instance the simple voltage amplifier circuits. At this point it is worth pausing for a while to see in what ways real op-amps depart from the ideal, since that influences circuit design, as we have hinted on several occasions. A good understanding of op-amp limitations and their influence on circuit design and performance will help you choose your op-amps wisely and design with them effectively.

A DETAILED LOOK AT OP-AMP BEHAVIOR

Figure 4.28 shows the schematic of the 741, a very popular op-amp. Its circuit is

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relatively straightforward, in terms of the kinds of transistor circuits we discussed in the last chapter. It has a differential input stage with current mirror load, followed by a common-emitter *npn* stage (again with active load) that provides most of the voltage gain. A *pnp* emitter follower drives the push-pull emitter follower output stage, which includes current-limiting circuitry. This circuit is typical of many op-amps now available. For many applications the properties of these amplifiers approach ideal op-amp performance characteristics. We will now take a look at the extent to which real op-amps depart from the ideal, what the consequences are for circuit design, and what to do about it.

4.11 Departure from ideal op-amp performance

The ideal op-amp has these characteristics:
1. Input impedance (differential or common mode) = infinity
2. Output impedance (open loop) = 0
3. Voltage gain = infinity
4. Common-mode voltage gain = 0
5. $V_{out} = 0$ when both inputs are at the same voltage (zero "offset voltage")
6. Output can change instantaneously (infinite slew rate)

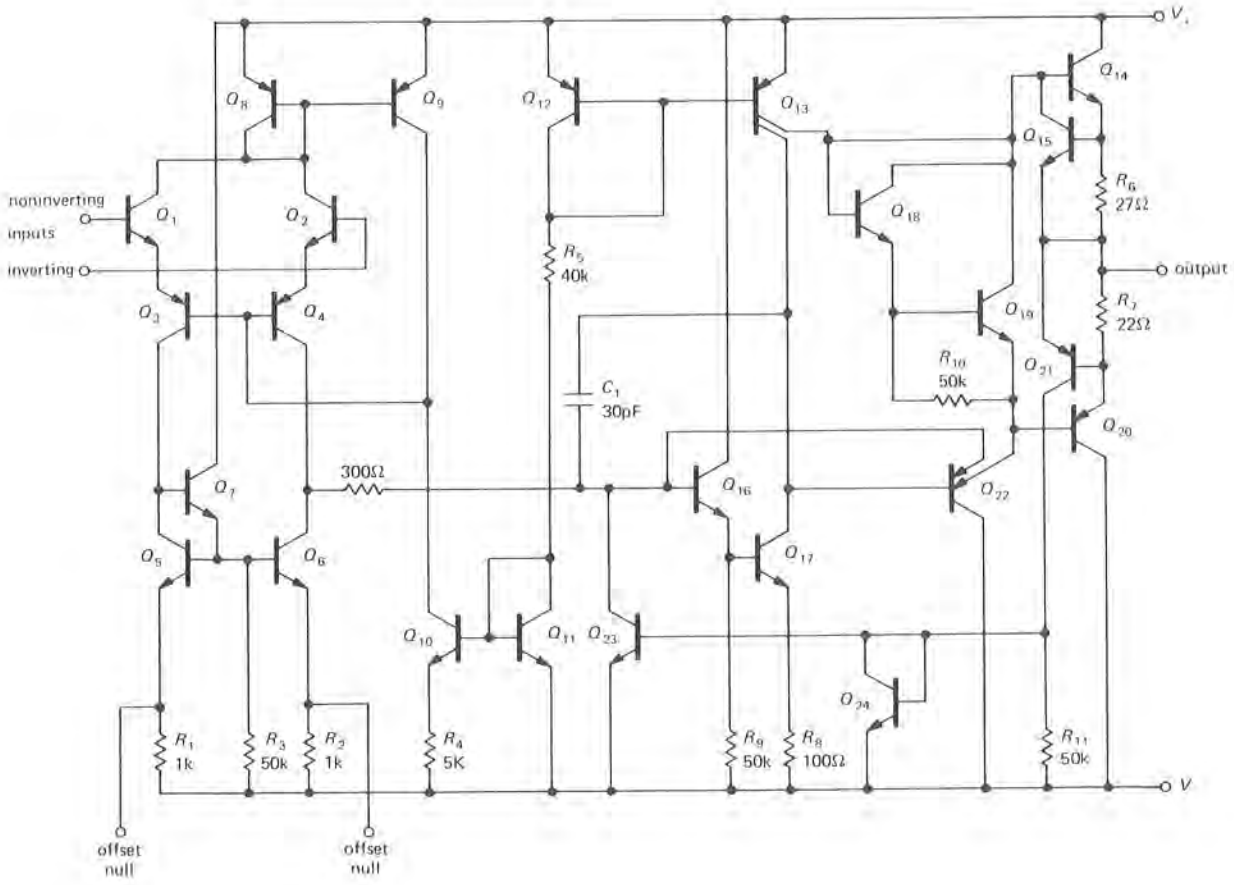


Figure 4.28. Schematic of the 741 op-amp. (Courtesy of Fairchild Camera and Instrument Corp.)

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All of these characteristics are independent of temperature and supply voltage changes.

Real op-amps depart from these characteristics in the following ways (see Table 4.1 for some typical values).

Input current

The input terminals sink (or source, depending on the op-amp type) a small current called the input bias current, I_B, which is defined as half the sum of the input currents with the inputs tied together (the two input currents are approximately equal and are simply the base or gate currents of the input transistors). For the JFET-input 411 the bias current is typically 50pA at room temperature (but as much as 2nA at 70°C), while a typical BJT-input op-amp like the OP-27 has a typical bias current of 15nA, varying little with temperature. As a rough guide, BJT-input op-amps have bias currents in the tens of nanoamps, while FET-input op-amps have input currents in the tens of picoamps (i.e., 1000 times lower). Generally speaking, you can ignore input current with FET op-amps, but not with bipolar-input op-amps.

The significance of input bias current is that it causes a voltage drop across the resistors of the feedback network, bias network, or source impedance. How small a resistor this restricts you to depends on the dc gain of your circuit and how much output variation you can tolerate. You will see how this works later.

Op-amps are available with input bias currents down to a nanoamp or less for (bipolar) transistor-input circuit types or down to a few picoamps ($10^{-6}\mu$A) for FET-input circuit types. The very lowest bias currents are typified by the superbeta Darlington LM11, with a maximum input current of 50pA, the AD549, with an input current of 0.06pA, and the MOSFET ICH8500, with an input current of 0.01pA. In general, transistor op-amps intended for high-speed operation have higher bias currents.

Input offset current

Input offset current is a fancy name for the difference in input currents between the two inputs. Unlike input bias current, the offset current, I_{os}, is a result of manufacturing variations, since an op-amp's symmetrical input circuit would otherwise result in identical bias currents at the two inputs. The significance is that even when it is driven by identical source impedances, the op-amp will see unequal voltage drops and hence a difference voltage between its inputs. You will see shortly how this influences design.

Typically, the offset current is one-half to one-tenth the bias current. For the 411, $I_{\text{offset}} = 25$pA, typical.

□ *Input impedance*

Input impedance refers to the differential input resistance (impedance looking into one input, with the other input grounded), which is usually much less than the common-mode resistance (a typical input stage looks like a long-tailed pair with current source). For the FET-input 411 it is about 10^{12} ohms, while for BJT-input op-amps like the 741 it is about 2MΩ. Because of the input bootstrapping effect of negative feedback (it attempts to keep both inputs at the same voltage, thus eliminating most of the differential input signal), Z_{in} in practice is raised to very high values and usually is not as important a parameter as input bias current.

□ *Common-mode input range*

The inputs to an op-amp must stay within a certain voltage range, typically less than the full supply range, for proper operation. If the inputs go beyond this range, the gain of the op-amp may change drastically, even reversing sign! For a 411 operating

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from ±15 volt supplies, the guaranteed common-mode input range is ±11 volts minimum. However, the manufacturer claims that the 411 will operate with common-mode inputs all the way to the positive supply, though performance may be degraded. Bringing either input down to the negative supply voltage causes the amplifier to go berserk, with symptoms like phase reversal and output saturation to the positive supply.

There are op-amps available with common-mode input ranges down to the negative supply, e.g., the LM358 (a good dual op-amp) or the LM10, CA3440, or OP-22, and up to the positive supply, e.g., the 301, OP-41, or the 355 series. In addition to the *operating* common-mode range, there are maximum allowable input voltages beyond which damage will result. For the 411 they are ±15 volts (but not to exceed the negative supply voltage, if it is less).

Differential input range

Some bipolar op-amps allow only a limited voltage between the inputs, sometimes as small as ±0.5 volt, although most are more forgiving, permitting differential inputs nearly as large as the supply voltages. Exceeding the specified maximum can degrade or destroy the op-amp.

□ *Output impedance; output swing versus load resistance*

Output impedance R_0 means the op-amp's intrinsic output impedance *without feedback*. For the 411 it is about 40 ohms, but with some low-power op-amps it can be as high as several thousand ohms (see Fig. 7.16). Feedback lowers the output impedance into insignificance (or raises it, for a current source); so what usually matters more is the maximum output current, with typical values of 20mA or so. This is frequently given as a graph of output voltage swing V_{om} as a function of load resistance, or sometimes just a few values for typical load resistances. Many op-amps have asymmetrical output drive capability, with the ability to sink more current than they can source (or vice versa). For the 411, output swings to within about 2 volts of V_{CC} and V_{EE} are possible into load resistances greater than about 1k. Load resistances significantly less than that will permit only a small swing. Some op-amps can produce output swings all the way down to the negative supply (e.g., the LM358), a particularly useful feature for circuits operated from a single positive supply, since output swings all the way to ground are then possible. Finally, op-amps with MOS transistor outputs (e.g., the CA3130, 3160, ALD1701, and ICL761*x*) can swing all the way to both rails. The remarkable bipolar LM10 shares this property, without the limited supply voltage range of the MOS op-amps (usually ±8V max).

□ *Voltage gain and phase shift*

Typically the voltage gain A_{vo} at dc is 100,000 to 1,000,000 (often specified in decibels), dropping to unity gain at a frequency (called f_T) of 1MHz to 10MHz. This is usually given as a graph of open-loop voltage gain as a function of frequency. For *internally compensated* op-amps this graph is simply a 6dB/octave rolloff beginning at some fairly low frequency (for the 411 it begins at about 10Hz), an intentional characteristic necessary for stability, as you will see in Section 4.32. This rolloff (the same as a simple *RC* low-pass filter) results in a constant 90° lagging phase shift from input to output (open-loop) at all frequencies above the beginning of the rolloff, increasing to 120° to 160° as the open-loop gain approaches unity. Since a 180° phase shift at a frequency where the voltage gain equals 1 will result in positive feedback (oscillations), the term "phase margin" is used to specify the difference between the phase shift at f_T and 180°.

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Input offset voltage

Op-amps don't have perfectly balanced input stages, owing to manufacturing variations. If you connect the two inputs together for zero input signal, the output will usually saturate at either V_{CC} or V_{EE} (you can't predict which). The difference in input voltages necessary to bring the output to zero is called the input offset voltage V_{os} (it's as if there were a battery of that voltage in series with one of the inputs). Usually op-amps make provision for trimming the input offset voltage to zero. For a 411 you use a 10k pot between pins 1 and 5, with the wiper connected to V_{EE}.

Of greater importance for precision applications is the drift of the input offset voltage with temperature and time, since any initial offset can be trimmed to zero. A 411 has a typical offset voltage of 0.8mV (2mV maximum), with temperature coefficient ("tempco") of 7μV/°C and unspecified coefficient of offset drift with time. The OP-77, a precision op-amp, is laser-trimmed for a typical offset of 10 *micro*volts, with temperature coefficient TCV_{os} of 0.2μV/°C and long-term drift of 0.2μV/month.

Slew rate

The op-amp "compensation" capacitance (discussed further in Section 4.32) and small internal drive currents act together to limit the rate at which the output can change, even when a large input unbalance occurs. This limiting speed is usually specified as *slew rate* or slewing rate (SR). For the 411 it is 15V/μs; low-power op-amps typically have slew rates less than 1V/μs, while a high-speed op-amp might slew at 100V/μs, and the LH0063C "damn fast buffer" slews at 6000V/μs. The slew rate limits the amplitude of an undistorted sine-wave output swing above some critical frequency (the frequency at which the full supply swing requires the maximum slew rate of the op-amp, Fig. 4.29), thus explaining the "output voltage swing as a function of frequency" graph. A sine wave of frequency f hertz and amplitude A volts requires a minimum slew rate of $2\pi Af$ volts per second.

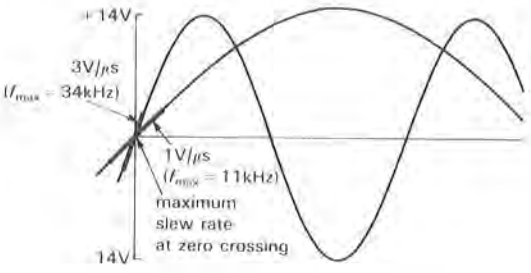


Figure 4.29. Slew-rate-induced distortion.

For externally compensated op-amps the slew rate depends on the compensation network used. In general, it will be lowest for "unity gain compensation," increasing to perhaps 30 times faster for ×100 gain compensation. This is discussed further in Section 4.32.

Temperature dependence

All these parameters have some temperature dependence. However, this usually doesn't make any difference, since small variations in gain, for example, are almost entirely compensated by feedback. Furthermore, the variations of these parameters with temperature are typically small compared with the variations from unit to unit.

The exceptions are input offset voltage and input offset current. This will matter, particularly if you've trimmed the offsets approximately to zero, and will appear as drifts in the output. When high precision is important, a low-drift "instrumentation" op-amp should be used, with external loads kept above 10k to minimize

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the horrendous effects on input-stage performance caused by temperature gradients. We will have much more to say about this subject in Chapter 7.

For completeness, we should mention here that op-amps are also limited in common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), input noise voltage and current (e_n, i_n), and output crossover distortion. These become significant limitations only in connection with precision circuits and low-noise amplifiers, and they will be treated in Chapter 7.

4.12 Effects of op-amp limitations on circuit behavior

Let's go back and look at the inverting amplifier with these limitations in mind. You will see how they affect performance, and you will learn how to design effectively in spite of them. With the understanding you will get from this example, you should be able to handle other op-amp circuits. Figure 4.30 shows the circuit again.

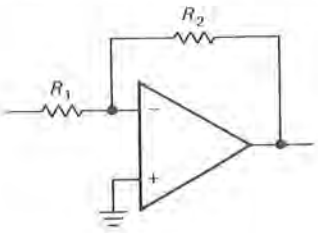


Figure 4.30

Open-loop gain

Because of finite open-loop gain, the voltage gain of the amplifier with feedback (closed-loop gain) will begin dropping at a frequency where the open-loop gain approaches R_2/R_1 (Fig. 4.31). For garden-variety op-amps like the 411, this means that you're dealing with a relatively low frequency amplifier; the open-loop gain is down to 100 at 50kHz, and f_T is 4MHz. Note that the closed-loop gain is always less than the open-loop gain; this means, for instance, that a ×100 amplifier built with a 411 will show a noticeable falloff of gain for frequencies approaching 50kHz. Later in the chapter (Section 4.25), when we deal with transistor feedback circuits with finite open-loop gains, we will have a more accurate statement of this behavior.

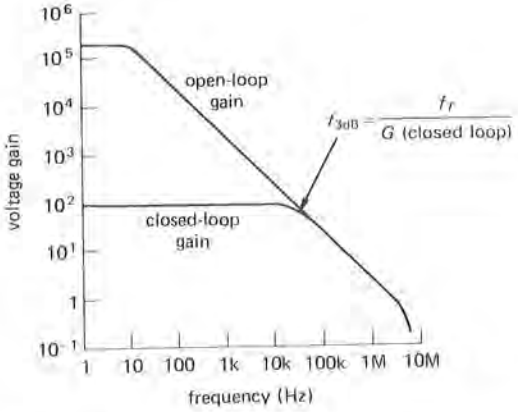


Figure 4.31. LF411 gain versus frequency ("Bode plot").

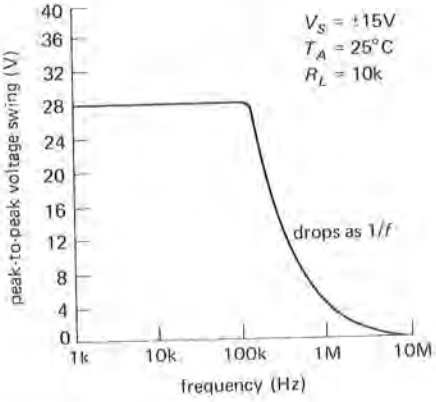


Figure 4.32. Output swing versus frequency (LF411).

Slew rate

Because of limited slew rate, the maximum undistorted sine-wave output swing drops above a certain frequency. Figure 4.32 shows the curve for a 411, with its 15V/μs

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slew rate. For slew rate S, the output amplitude is limited to $A(\text{pp}) \leq S/\pi f$ for a sine wave of frequency f, thus explaining the $1/f$ dropoff of the curve. The flat portion of the curve reflects the power-supply limits of output voltage swing.

As an aside, the slew-rate limitation of op-amps can be usefully exploited to filter sharp noise spikes from a desired signal, with a technique known as *nonlinear low-pass filtering*: By deliberately limiting the slew rate, the fast spikes can be dramatically reduced without any distortion of the underlying signal.

Output current

Because of limited output current capability, an op-amp's output swing is reduced for small load resistances. Figure 4.33 shows the graph for a 411. For precision applications it is a good idea to avoid large output currents in order to prevent on-chip thermal gradients produced by excessive power dissipation in the output stage.

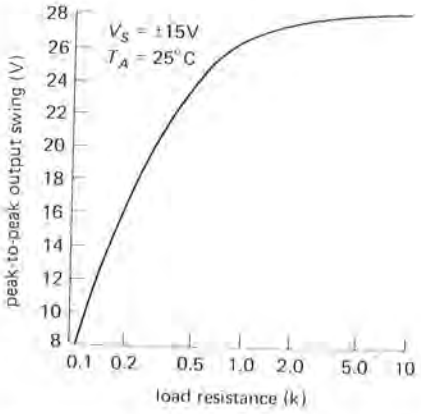


Figure 4.33. Output swing versus load (LF411).

Offset voltage

Because of input offset voltage, a zero input produces an output of $V_{\text{out}} = G_{dc}V_{os}$. For an inverting amplifier with voltage gain of 100 built with a 411, the output could be as large as ± 0.2 volt when the input is grounded ($V_{os} = 2$mV max). Solutions: (a) If you don't need gain at dc, use a capacitor to drop the gain to unity at dc, as in Figure 4.7, as well as the RIAA amplifier circuit (Fig. 4.20). In this case you could do that by capacitively coupling the input signal. (b) Trim the voltage offset to zero using the manufacturer's recommended trimming network. (c) Use an op-amp with smaller V_{os}. (d) Trim the voltage offset to zero using an external trimming network as described in Section 7.06 (Fig. 7.5).

Input bias current

Even with a perfectly trimmed op-amp (i.e., $V_{os} = 0$), our inverting amplifier circuit will produce a non-zero output voltage when its input terminal is connected to ground. That is because the finite input bias current, I_B, produces a voltage drop across the resistors, which is then amplified by the circuit's voltage gain. In this circuit the inverting input sees a driving impedance of $R_1 \parallel R_2$, so the bias current produces a voltage $V_{\text{in}} = I_B(R_1 \parallel R_2)$, which is then amplified by the gain at dc, $-R_2/R_1$.

With FET-input op-amps the effect is usually negligible, but the substantial input current of bipolar op-amps can cause real problems. For example, consider an inverting amplifier with $R_1 = 10$k and $R_2 = 1$M; these are reasonable values for an inverting stage, where we might like to keep Z_{in} at least 10k. If we chose the low-noise bipolar LM833, the output (for grounded input) could be as large as $100 \times 1000\text{nA} \times 9.9\text{k}$, or 0.99 volt ($G_{dc}I_B R_{\text{unbalance}}$), which is unacceptable. By comparison, for our jellybean LF411 (JFET-input) op-amp the corresponding worst-case output (for grounded input) is 0.2mV; for most applications this is negligible, and in any case is dwarfed by the

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V_{os}-produced output error (200mV, worst-case untrimmed, for the LF411).

There are several solutions to the problem of bias-current errors. If you must use an op-amp with large bias current, it is a good idea to ensure that both inputs see the same dc driving resistance, as in Figure 4.34. In this case, 9.1k is chosen as the parallel resistance of 10k and 100k. In addition, it is best to keep the resistance of the feedback network small enough so that bias current doesn't produce large offsets; typical values for the resistance seen from the op-amp inputs are 1k to 100k or so. A third cure involves reducing the gain to unity at dc, as in the RIAA amplifier earlier.

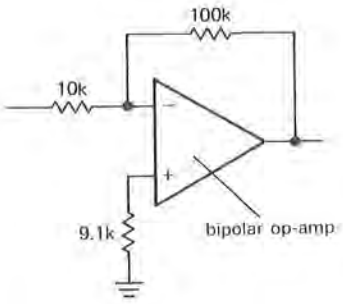


Figure 4.34. With bipolar op-amps, use a compensation resistor to reduce errors caused by input bias current.

In most cases, though, the simplest solution is to use op-amps with negligible input current. Op-amps with JFET or MOSFET input stages generally have input currents in the picoamp range (watch out for its rapid rise versus temperature, though, roughly doubling every 10°C), and many modern bipolar designs use superbeta transistors or bias-cancellation schemes to achieve bias currents nearly as low, *decreasing* slightly with temperature. With these op-amps, you can have the advantages of bipolar op-amps (precision, low noise) without the annoying problems caused by input current. For example, the precision low-noise bipolar OP-27 has I_B =10nA (typ), the inexpensive bipolar LM312 has I_B =1.5nA (typ), and its improved bipolar cousins (the LT1012 and LM11) have I_B = 30pA (typ). Among inexpensive FET op-amps, the JFET LF411 has I_B = 50pA (typ), and the MOSFET TLC270 series, priced under a dollar, have I_B = 1pA (typ).

Input offset current

As we just described, it is usually best to design circuits so that circuit impedances, combined with op-amp bias current, produce negligible errors. However, occasionally it may be necessary to use an op-amp with high bias current, or to deal with signals of extraordinarily high Thévenin impedances. In that case the best you can do is to balance the dc driving resistances seen by the op-amp at its input terminals. There will still be some error at the output ($G_{dc}I_{\text{offset}}R_{\text{source}}$), due to unavoidable asymmetry in the op-amp input currents. In general, I_{offset} is smaller than I_{bias} by a factor of 2 to 20 (with bipolar op-amps generally showing better matching than FET op-amps).

In the preceding paragraphs we have discussed the effects of op-amp limitations, taking the example of the simple inverting voltage amplifier circuit. Thus, for example, op-amp input current caused a *voltage* error at the output. In a different op-amp application you may get a different effect; for example, in an op-amp integrator circuit, finite input current produces an output *ramp* (rather than a constant) with zero applied input. As you become familiar with op-amp circuits you will be able to predict the effects of op-amp limitations in a given circuit and therefore choose which op-amp to use in a given application. In general, there is no "best" op-amp (even when price is no object): For example,

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TABLE 4.1. OPERATIONAL AMPLIFIERS

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
BIPOLAR, PRECISION																	
OP-07A	PM+	•	A	–	•	–	1	6	44	4	0.01	0.025	0.2	0.6	2	2	9.6
OP-07E	PM+	•	A	–	•	–	1	6	44	4	0.03	0.08	0.3	1.3	4	3.8	9.6
OP-21A	PM	•	A	A	•	–	1	5	36	0.3	0.04	0.1	0.5	1	100	4	21
OP-27E	PM+	•	A	A	•	–	1	8	44	5	0.01	0.025	0.2	0.6	40	35	3.0
OP-27G	PM+	•	A	A	•	–	1	8	44	6	0.03	0.1	0.4	1.8	80	75	3.2
OP-37E	PM+	•	A	–	•	–	5	8	44	5	0.01	0.025	0.2	0.6	40	35	3.0
OP-50E	PM	•	–	–	•	•	5	10	36	4	0.01	0.025	0.15	0.3	5	1	4.5
OP-77E	PM	•	A	A	•	–	1	6	44	2	0.01	0.025	0.1	0.3	2	1.5	9.6
OP-90E	PM	•	A	A	•	–	1	1.6	36	0.02	0.05	0.15	0.3	2	15	3	60
OP-97E	PM	•	–	–	•	–	1	4.5	40	0.6	0.01	0.025	0.2	0.6	0.1	0.1	14
MAX400M	MA	•	–	–	•	–	1	6	44	4	0.004	0.01	0.2	0.3	2	2	9.6
LM607A	NS	•	–	–	•	•	1	6	44	1.5	0.015	0.025	0.2	0.3	2	2	6.5
AD707C	AD	•	A	–	•	–	1	6	36	3	0.005	0.015	0.03	0.1	1	1	9.6
AD846B	AD	•	–	–	–	•	2	10	36	6.5	0.025	0.075	0.8	3.5	250	(k)	2
LT1001A	LT	•	A	–	•	–	1	6	44	3.3	0.01	0.025	0.2	0.6	4	4	9.6
LT1007A	LT	•	–	–	•	–	1	5	44	4	0.01	0.025	0.2	0.6	35	30	2.5
LT1012C	LT+	•	A	–	•	•	1	4	40	0.6	0.01	0.05	0.2	1.5	0.15	0.15	14
LT1028A	LT	•	–	–	•	•	1	8	44	9.5	0.01	0.04	0.2	0.8	90	50	0.9
LT1037A	LT	•	–	–	•	–	5	5	44	4.5	0.01	0.025	0.2	0.6	35	30	2.5
RC4077A	RA	•	–	–	•	–	1	6	44	1.7	0.004	0.01	0.1	0.3	2	1.5	9.6
HA5134A	HA	–	–	•	–	–	1	10	40	8	0.05	0.1	0.3	1.2	25	25	7
HA5135	HA	•	–	–	•	–	1	8	40	1.7	0.01	0.08	0.4	1.3	4	4	9
HA5147A	HA	•	–	–	•	–	10	8	44	4	0.01	0.025	0.2	0.6	40	35	3.0
BIPOLAR, LOW-BIAS (see also "bipolar, precision")																	
OP-08E	PM	•	–	–	–	•	U	10	40	0.5	0.07	0.15	0.5	2.5	2	0.2	20
LM10	NS+	•	–	–	•	–	1	1	45	0.4	0.3	2	2	-	20	0.7	47
LM11	NS+	•	–	–	•	•	1	5	40	0.6	0.1	0.3	1	3	50pA	10pA	150
OP-12E	PM+	•	–	–	–	–	1	10	40	0.5	0.07	0.15	0.5	2.5	2	0.2	20
LM308	NS+	•	A	–	–	•	U	10	36	0.8	2	7.5	6	30	7	1	35
LM312	NS+	•	–	–	•	•	1	10	40	0.8	2	7.5	6	30	7	1	35
LP324	NS	–	–	•	–	–	1	4	32	0.25	2	4	10	-	10	2	-
BIPOLAR, SINGLE-SUPPLY																	
324A	NS+	A	A	•	–	–	1	3	32	3	2	3	7	30	100	30	-
LP324	NS	–	–	•	–	–	1	4	32	0.25	2	4	10	-	10	2	-
LT1013C	LT	–	•	A	–	–	1	4	44	1	0.06	0.3	0.4	2.5	50	2	22
HA5141A	HA	•	A	A	–	–	1	2	40	0.07	0.5	2	3	-	75	10	20
BIPOLAR, SINGLE-SUPPLY PRECISION																	
LT1006A	LT	•	–	–	•	–	1	2.7	44	0.5	0.02	0.05	0.2	1.3	15	0.5	22
LT1013A	LT	–	•	A	–	–	1	4	44	1	0.04	0.15	0.4	2	35	1.3	22

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Type	Slew rate[e] typ (V/μs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	Swing to supplies?[g] In −	Swing to supplies?[g] Out +	Swing to supplies?[g] Out −	Comments
OP-07A	0.17	0.6	110	100	110	10	30[h]	–	–	–	–	
OP-07E	0.17	0.6	106	94	106	10	30[h]	–	–	–	–	
OP-21A	0.25	0.6	100	104	120	-	30	–	–	–	–	low power
OP-27E	2.8	8	114	100	120	20	0.5	–	–	–	–	low noise
OP-27G	2.8	8	100	94	117	20	0.5	–	–	–	–	cheap grade
OP-37E	17	63	114	100	120	20	0.5	–	–	–	–	low noise, decomp OP-27
OP-50E	3	25	126	126	140	70	10[h]	–	–	–	–	high current, low noise
OP-77E	0.3	0.6	120	110	134	12	30[h]	–	–	–	–	improved OP-07
OP-90E	0.01	0.02	100	104	117	6	36	–	•	–	•	micropower
OP-97E	0.2	0.9	114	114	110	10	0.5	–	–	–	–	low power OP-77
MAX400M	0.3	0.6	114	100	114	12	30	–	–	–	–	lowest non-chopper V_{os}
LM607A	0.7	1.8	124	100	134	10	0.5	–	–	–	–	
AD707C	0.3	0.9	130	120	138	12	44	–	–	–	–	improved OP-07; dual = 708
AD846B	450	310	110	110	-	50	18	–	–	–	–	current feedback; fast
LT1001A	0.25	0.8	114	110	113	30	30	–	–	–	–	
LT1007A	2.5	8	117	110	137	20	0.5	–	–	–	–	low noise, ~OP-27
LT1012C	0.2	0.8	110	110	106	12	1	–	–	–	–	improved 312; dual = 1024
LT1028A	15	75	114	117	137	20	1	–	–	–	–	ultra low noise
LT1037A	15	60	117	110	137	20	0.5	–	–	–	–	decomp 1007, ~OP-37
RC4077A	0.25	0.8	120	110	128	15	30	–	–	–	–	lowest non-chopper V_{os}
HA5134A	1	4	94	100	108	20	40	–	–	–	–	quad, low noise
HA5135	0.8	2.5	106	94	120	20	15[h]	–	–	–	–	
HA5147A	35	140	114	80	120	15	0.5	–	–	–	–	low noise, high speed, uncomp
OP-08E	0.12	0.8	104	104	98	5	0.5	–	–	–	–	precision 308
LM10	0.12	0.1	93	90	102	20	40	–	•	•	•	1V op-amp; precision; volt. ref.
LM11	0.3	0.5	110	100	100	2	0.5	–	–	–	–	precision; lowest bias bipolar
OP-12E	0.12	0.8	104	104	98	5	0.5	–	–	–	–	precision 312
LM308	0.15	0.3	80	80	88	5	0.5	–	–	–	–	original low-bias (superbeta)
LM312	0.15	0.3	80	96	88	5	0.5	–	–	–	–	compensated 308
LP324	0.05	0.1	80	90[t]	94	5	32	–	•	–	•	low power, single supply
324A	0.5	1	65	65	88	20	30	–	•	–	•	a classic; dual=358A
LP324	0.05	0.1	80	90[t]	94	5	32	–	•	–	•	low power, low bias
LT1013C	0.4	0.8	97	100	122	25	30	–	•	–	•	improved 358/324; quad = 1014
HA5141A	1.5	0.4	80	94	94	1	7	–	•	–	•	micropower
LT1006A	0.4	1	100	106	120	20	30	–	•	–	•	optional I_s = 90μA
LT1013A	0.4	0.8	100	103	124	25	30	–	•	–	•	improved 358/324; quad = 1014

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
BIPOLAR, HIGH-SPEED																	
OP-62E	PM	•	–	–	•	•	1	16	36	7	-	0.2	-	-	300	100	2.5
OP-63E	PM	•	–	–	•	•	1	16	36	7	-	0.75	-	-	300	100	7
OP-64E	PM	•	–	–	•	•	5	16	36	7	-	0.75	-	-	300	100	7
OP-65E	PM	•	–	–	•	–	1	9	14	25	-	2	-	-	3μA	1μA	-
CLC400	CL	•	–	–	•	–	1	-	7	15	2	5.5	20	40	25μA	(k)	12
AD509K	AD	•	–	–	•	•	3	10	40	6	4	8	-	40	200	25	19
SL541B	PL	•	–	–	•	–	10	-	24	21	-	5	15	-	25μA	10	-
VA705L	VT	•	A	A	•	–	1	8	12	10	1	2	20	-	900	25	-
VA706K	VT	•	A	A	•	–	1	8	12	10	4	10	20	-	1μA	120	-
VA707K	VT	•	A	A	•	–	12	8	12	10	3	6	20	-	1μA	120	-
LM837	NS	–	–	•	–	–	1	8	36	15	0.3	5	2	-	1μA	200	4.5
AD840K	AD	•	–	–	•	–	10	10	36	12	0.1	0.3	3	-	5μA	200	4
AD841K	AD	•	–	–	•	–	1	10	36	12	0.5	1	35	20	5μA	200	13
AD847J	AD	•	–	–	•	–	1	9	36	5.6	0.5	1	15	-	7μA	50[t]	15[i]
AD848J	AD	•	–	–	•	–	5	9	36	5.6	0.5	1	2	10	5μA	15[t]	4[i]
AD849J	AD	•	–	–	•	–	25	9	36	5.6	0.5	1	1	10	5μA	15[t]	4[i]
HA2539	HA	•	–	–	–	–	10	10	35	25	8	15	20	-	20μA	6μA	6
SL2541B	PL	•	–	–	•	–	1	14	30	25[t]	10	-	20	-	20μA	-	-
HA2541	HA	•	–	–	•	–	1	10	35	45	-	2	20	-	35μA	7μA	10
HA2542	HA	•	–	–	•	•	2	10	35	40	-	10	20	-	35μA	7μA	10
HA2544	HA	•	–	–	•	•	1	10	33	10	6	15	10	-	15μA	2μA	-
CA3450	RC	•	–	–	•	•	1	10	14	35	8	15	-	-	350	150	-
HA5101	HA	•	A	A	•	–	1	4	40	6	0.5	3	3	-	200	75	3.3
HA5111	HA	•	A	A	•	•	10	4	40	6	0.5	3	3	-	200	75	3.3
HA5147A	HA	•	–	–	•	–	10	8	44	4	0.01	0.025	0.2	0.6	40	35	3.0
HA5195	HA	•	–	–	–	–	5	20	35	25	3	6	20	-	15μA	4μA	6
LM6361	NS	•	–	–	•	–	1	5	36	6.5	5	20	10	-	5μA	2μA	15
LM6364	NS	•	–	–	•	–	5	5	36	6.5	2	9	6	-	5μA	2μA	8
LM6365	NS	•	–	–	•	–	25	5	36	6.8	1	6	3	-	5μA	2μA	5
BIPOLAR, OTHER																	
OP-20B	PM	•	A	A	•	–	1	4	36	0.08	0.06	0.25	0.75	1.5	25	1.5	58
LM833	NS	–	•	–	–	–	1	10	36	8	0.3	5	2	-	1μA	200	4.5
CA3193A	RC	•	–	–	•	–	1	7	36	3.5	0.14	0.2	1	3	20	5	24
XR4560	XR	–	•	–	–	–	1	8	36	2	0.5	6	-	-	500	200	8
HA5151	HA	•	A	A	–	–	1	2	40	0.25	2	3	3	-	150	30	15
NE5534	SN+	•	A	–	•	•	3	6	44	8	0.5	4	-	-	2μA	300	4
MC33078	MO	–	•	A	–	–	1	10	36	5	0.15	2	2	-	750	150	4.5
MC33171	MO	•	A	A	•	–	1	3	44	0.25	2	4.5	10	-	100	20	32
MC34071A	MO	•	A	A	•	–	1	3	44	2.5	0.5	1.5	10	-	500	50	32

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Type	Slew rate[e] typ (V/µs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-62E	15	50	110	105	111	20	5	–	–	–	–	precision
OP-63E	50	50	110	105	100	20	5	–	–	–	–	
OP-64E	200	200	110	105	100	20	5	–	–	–	–	
OP-65E	200	150	85	90	100	50	5	–	–	–	–	
CLC400	700	280	40	40	-	50	-	–	–	–	–	transimpedance; decomp=401
AD509K	120	20	80	80	80	-	15	–	–	–	–	fast
SL541B	175	100	60	46	46	6.5	9	–	–	–	–	fast, video
VA705L	35	25	60	60	80	50	9	–	–	–	–	video, drives 50Ω; fast settle
VA706K	42	25	60	60	66	50	9	–	–	–	–	video, drives 50Ω; fast settle
VA707K	105	300	60	60	74	50	9	–	–	–	–	decomp, fast, 50Ω
LM837	10	25	80	120	90	40	30	–	–	–	–	low noise, low distortion
AD840K	400	400	100	94	104	50	6	–	–	–	–	decomp 841; 842 has G>2
AD841K	300	40	90	90	88	50	6	–	–	–	–	fast settle; decomp versions
AD847J	300	50	78	75	70	20	6	–	–	–	–	fast settle; decomp versions
AD848J	300	250	104[t]	104[t]	82	25	6	–	–	–	–	decomp 847
AD849J	300	725	110[t]	100[t]	90	25	6	–	–	–	–	uncomp 847
HA2539	600	600	60	85	80	10	6	–	–	–	–	low noise, sim to 2540
SL2541B	900	800	47	40[t]	45	10	10	–	–	–	–	has uncommitted unity gain buf
HA2541	280	40	70	60	80	10	6	–	–	–	–	fast settle, low distortion
HA2542	375	120	70	70	80	100	6	–	–	–	–	fast settle, decomp
HA2544	150	33	75	70	70	35	6	–	–	–	–	video
CA3450	420	190	50	60	96	75	5	–	–	–	–	video amp/line driver
HA5101	10	10	100[t]	80	136[t]	30	7	–	–	–	–	low noise
HA5111	50	100	100[t]	100[t]	136[t]	30	7	–	–	–	–	low noise, uncomp
HA5147A	35	140	114	80	120	15	0.7	–	–	–	–	low noise, precision, uncomp
HA5195	200	150	74	70	80	25	6	–	–	–	–	Elantec EL2195 = improved
LM6361	300	50	70	72	52	30	8	–	–	–	–	vertical PNP
LM6364	300	160	102[t]	70	66[t]	30	8	–	–	–	–	vertical PNP
LM6365	300	725	80	104[t]	75	30	8	–	–	–	–	vertical PNP
OP-20B	0.05	0.1	96	100	114	0.5	30	–	•	–	–	accurate low power
LM833	7	15	80	80	90	10	30	–	–	–	–	low noise, low distortion
CA3193A	0.25	1.2	110	100	110	7	5	–	–	–	–	
XR4560	4	10	70	76	86	100	30	–	–	–	–	intended for audio
HA5151	4.5	1.3	80	80	94	3	7	–	–	–	•	low power
NE5534	6	10	70	80	88	20	0.5	–	–	–	–	low noise, intended for audio
MC33078	7	16	80	80	90	20	36	–	–	–	–	low noise, low distortion
MC33171	2.1	1.8	80	80	94	4	44	–	•	–	–	
MC34071A	10	4.5	80	80	94	25	44	–	•	–	–	drives 0.01µF

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1 2 4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage: Offset typ (mV)	Voltage: Offset max (mV)	Voltage: Drift typ (μV/°C)	Voltage: Drift max (μV/°C)	Current: Bias max (nA)	Current: Offset max (nA)	e_n @1kHz typ nV/√Hz
BIPOLAR, OBSOLESCENT															
OP-01E	PM	• – –	•	–	1	10	44	3	1	2	3	10	50	5	-
OP-02E	PM	• A –	•	–	1	10	44	2	0.3	0.5	2	8	30	2	21
OP-05E	PM+	• A –	•	–	1	6	44	4	0.2	0.5	0.7	2	4	3.8	9.6
OP-11E	PM	– – •	–	–	1	10	44	6	0.3	0.5	2	10	300	20	12
307	NS+	• – –	–	–	1	10	44	2.5	2	7.5	6	30	250	50	16
LM318	NS+	• – –	•	•	1	10	40	10	4	10	-	-	500	200	14
349	NS	– – •	–	–	5	10	36	4.5	1	6	-	-	200	50	60
AD517L	AD	• – –	•	–	1	10	36	3	-	0.025	-	0.5	1	0.25	20
AD518J	AD	• – –	•	•	1	10	40	10	4	10	10	-	500	200	-
NE530	SN	• A –	•	–	1	10	36	3	2	5	6	-	150	40	30
NE531	SN	• – –	•	•	U	12	44	10	2	6	-	-	2μA	200	-
NE538	SN	• A –	•	–	5	10	36	2.8	2	5	6	-	150	40	18
μA725	FA+	• – –	•	•	U	6	44	3	0.5	1	2	5	100	20	-
μA739	FA	– • –	–	•	U	8	36	14	1	6	-	-	2μA	10μA	-
741C	FA+	• A A	•	–	1	10	36	2.8	2	6	-	-	500	200	-
748C	FA+	• – –	•	•	U	10	36	3.3	2	6	-	-	500	200	-
μA749	FA	– • –	–	•	U	8	36	10	1	3	3	-	750	400	-
1435	TP	• – –	•	•	10	24	32	30	2	5	5	25	20μA	-	-
1456	MO	• – –	•	–	1	10	36	3	5	10	-	-	30	10	45
HA2505	HA	• – –	•	•	1	20	40	6	4	8	20	-	250	50	-
HA2515	HA	• – –	•	•	1	20	40	6	5	10	30	-	250	50	-
HA2525	HA	• – –	•	•	3	20	40	6	5	10	30	-	250	50	-
HA2605	HA	• – –	•	•	1	10	45	4	3	5	10	-	25	25	-
HA2625	HA	• – –	•	•	5	10	45	4	3	5	10	-	25	25	-
CA3100	RC	• – –	•	•	10	13	36	11	1	5	-	-	2μA	400	-
4558	RA+	– • –	–	–	1	8	36	5.6	2	6	-	-	500	200	43
NE5535	SN	A • –	•	–	1	10	36	2.8	2	5	6	-	150	40	17
5539	SI+	• – –	–	•	7	6	24	15	2.5	5	5	10	20μA	-	4
JFET, PRECISION															
OP-41E	PM	• – –	•	–	1	10	36	1	0.2	0.25	2.5	5	0.005	0.001	32
OP-43E	PM	• – –	•	–	1	10	36	1	0.2	0.25	2.5	5	0.005	0.001	32
OPA101B	BB	• – –	•	–	1	10	40	8	0.05	0.25	3	5	0.01	4pA	8
OPA111B	BB	• A –	•	–	1	10	36	3.5	0.05	0.25	0.5	1	1pA	0.7pA	7
AD547L	AD	• A –	•	–	1	5	36	1.5	-	0.25	-	1	0.025	2pA[1]	30
AD548C	AD	• A –	•	–	1	9	36	0.2	0.1	0.25	-	2	0.01	0.005	30
OPA627B	BB	• – –	•	–	1	9	36	8	0.04	0.1	0.5	0.8	0.02	0.02	5.2
AD711C	AD	• A A	•	–	1	9	36	2.8	0.1	0.25	2	3	0.025	0.01	18
AD845K	AD	• – –	•	–	1	9.5	36	12	0.1	0.25	1.5	5	1	0.1	25
LT1055A	LT	• – –	•	–	1	10	40	4	0.05	0.15	1.2	4	0.05	0.01	14
HA5170	HA	• – –	•	–	1	9	44	2.5	0.1	0.3	2	5	0.1	0.06	10

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Type	Slew rate[e] typ (V/μs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-01E	18	2.5	80	80	94	6	30	–	–	–	–	fast, precision
OP-02E	0.5	1.3	90	90	100	6	30	–	–	–	–	precision, low current
OP-05E	0.17	0.6	110	94	106	10	30[h]	–	–	–	–	
OP-11E	1	2	110	90	100	6	30	–	–	–	–	precision quad
307	0.5	1	70	70	84	10	30	•	–	–	–	a classic; uncomp=301
LM318	70	15	70	65	86	10	0.5	–	–	–	–	was popular
349	2	4	70	77	88	15	36	–	–	–	–	decomp 348 (quad 741)
AD517L	0.1	0.25	110	96	120	10	30	–	–	–	–	
AD518J	70	12	70	65	88	15	-	–	–	–	–	
NE530	35	3	70	76	94	10	30	•	–	–	–	fast; dual=5530
NE531	35	1	70	76	86	-	15	•	–	–	–	
NE538	60	5	70	76	94	10	30	•	–	–	–	fast; dual=5538
μA725	0.005	0.08	110	100	108	15	5	–	–	–	–	original precision op-amp
μA739	1	6	70	85[t]	76	1.5	5	–	–	–	•	low noise, intended for audio
741C	0.5	1.2	70	76	86	20	30	–	–	–	–	old classic; dual=1458, quad=348
748C	0.5	1.2	70	76	94	15	30	–	–	–	–	uncomp 741
μA749	2	6	70	74	86	1.5	5	–	–	–	•	sim to 739
1435	300	1GHz	80	75[t]	80	10	2	–	–	–	–	fast settle
1456	2.5	1	70	74	97	5	40	–	–	–	–	
HA2505	30	12	74	74	84	10	15	•	–	–	–	
HA2515	60	12	74	74	78	10	15	•	–	–	–	
HA2525	120	20	74	74	78	10	15	•	–	–	–	
HA2605	7	12	74	74	98	10	12	–	–	–	–	
HA2625	35	100	74	74	98	10	12	–	–	–	–	
CA3100	25	30	76	60	58	15	12	–	–	–	–	
4558	1	2.5	70	74	86	15	30	–	–	–	–	fast 1458
NE5535	15	1	70	76	94	10	30	•	–	–	–	fast
5539	600	1200	70	66	46	40	10	–	–	–	•	small output swing
OP-41E	1.3	0.5	100	92	120	15	20	•	–	–	–	low bias, low dist; OP-43 faster
OP-43E	6	2.4	100	92	120	15	20	•	–	–	–	low bias, low dist; OP-41 stabler
OPA101B	7	20	80	86	96	45	20	–	–	–	–	low noise; decomp = OPA102
OPA111B	2	2	100	100	120	10	36	–	–	–	–	low noise, low bias
AD547L	3	1	80	80	108	20	20	–	–	–	–	dual = AD642, 647
AD548C	1.8	1	86	86	110	20	20	–	–	–	–	improved LF441; dual = AD648
OPA627B	55	16	106	106	110	30	-	–	–	–	–	fast
AD711C	20	4	86	86	106	20	20	–	–	–	–	improved LF411/2
AD845K	100	16	94	95	108	30	36	–	–	–	–	fast
LT1055A	13	5	86	90	104	30	40	–	–	–	–	LT1056 is 20% faster
HA5170	8	8	90	74	110	10	30	•	–	–	–	low noise

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage: Offset typ (mV)	Voltage: Offset max (mV)	Voltage: Drift typ (μV/°C)	Voltage: Drift max (μV/°C)	Current: Bias max (nA)	Current: Offset max (nA)	e_n @1kHz typ nV/√Hz
JFET, HIGH-SPEED																	
OP-42E	PM	•	–	–	•	–	1	15	40	6.5	0.3	0.75	4	10	0.2	0.04	13
OP-44E	PM	•	–	–	•	–	3	16	40	6	0.03	0.75	4	10	0.2	40pA	13
357B	NS+	•	–	–	•	–	5	10	36	7	3	5	5	-	100pA	0.02	12
AD380K	AD	•	–	–	•	•	U	12	40	15	-	1	-	10	0.1	5pA[t]	15
LF401A	NS	•	–	–	•	•	1	15	36	12	-	0.2	-	-	0.2	0.1	23
OPA404B	BB	–	–	•	–	–	1	10	36	10	0.26	0.75	3	-	0.004	4pA	15
LF457B	NS	•	–	–	•	–	5	10	36	10	0.18	0.4	3	4	50pA	20pA	10
OPA602C	BB	•	–	–	•	–	1	10	36	4	0.1	0.25	1	2	1pA	1pA	13
OPA605K	BB	•	–	–	•	•	50	10	40	9	0.25	0.5	-	5	0.035	2pA[t]	20
OPA606L	BB	•	–	–	•	–	1	10	36	9.5	0.1	0.5	3	5	0.01	5pA	13
AD744C	AD	•	A	–	•	•	2	9	36	4	0.1	0.25	2	3	0.05	0.02	18
AD843B	AD	•	–	–	•	–	1	9	36	12	0.5	1	15	-	1	0.1	13
AD845K	AD	•	–	–	•	–	1	9.5	36	10.2	0.1	0.25	1.5	3	0.4	0.05	25
LT1022A	LT	•	–	–	•	–	1	20	40	7	0.08	0.25	1.3	5	0.05	0.01	14
HA5160	HA	•	–	–	–	•	U	14	40	10	1	3	20	-	0.05	0.01	35
MC34080A	MO	•	A	A	•	–	2	6	44	3.4	0.3	0.5	10	-	0.2	0.1	30
MC34081A	MO	•	A	A	•	–	1	6	44	3.4	0.3	0.5	10	-	0.2	0.1	30
JFET, OTHER																	
TL031C	TI	•	A	A	•	–	1	10	36	0.28	0.5	1.5	6	-	0.2	0.1	41
TL051C	TI	•	A	A	•	–	1	10	36	3.2	0.6	1.5	8	-	0.2	0.1	18
TL061C	TI+	•	A	A	•	–	1	4	36	0.25	3	15	10	-	0.4	0.2	42
TL071C	TI+	•	A	A	•	–	1	7	36	2.5	3	10	10	-	0.2	0.05	18
TL081B	TI+	•	A	A	•	–	1	7	36	2.8	2	3	10	-	0.2	0.01	18
OPA121	BB	•	–	–	•	–	1	10	36	4	0.5	2	3	10	0.005	4pA	8
OPA128L	BB	•	–	–	•	–	1	10	36	1.5	0.14	0.5	-	5	75fA	30fA[t]	27
LF351	NS+	•	A	A	•	–	1	10	36	3.4	5	10	10	-	0.2	0.1	25
355B	NS+	•	–	–	•	–	1	10	36	4	3	5	5	-	100pA	0.02	20
356B	NS+	•	–	–	•	–	1	10	36	7	3	5	5	-	100pA	0.02	12
LF411	NS+	•	A	–	•	–	1	10	36	3.4	0.8	2	7	20	0.2	0.1	25
LF*nnn*	NS	–	•	–	–	–	1	6	36	25	1	-	-	-	100pA	50pA	3.5
LF441	NS	•	A	A	•	–	1	10	36	0.25	1	5	10	20	0.1	0.05	35
LF455B	NS	•	–	–	•	–	1	10	36	4	0.18	0.4	3	4	50pA	20pA	12
LF456B	NS	•	–	–	•	–	1	10	36	8	0.18	0.4	3	4	50pA	20pA	10
AD549L	AD	•	–	–	•	–	1	10	36	0.7	0.3	0.5	5	10	60fA	20fA[t]	35
AD611K	AD	•	–	–	•	–	1	10	36	2.5	0.25	0.5	5	10	0.05	0.025	18
LT1057A	LT	–	•	A	–	–	1	20	40	3.8	0.15	0.45	1.8	7	0.05	0.04	13
HA5180	HA	•	–	–	•	–	1	10	40	1	0.1	0.5	5	-	0.001	200fA	70
MC34001A	MO	•	A	A	•	–	1	8	36	2.5	1	2	10	-	0.1	0.05	25
MC34181	MO	•	A	A	•	–	1	3	36	0.2	0.5	2	10	-	0.1	0.05	38

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Type	Slew rate[e] typ (V/μs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-42E	58	10	88	86	114	25	40	–	–	–	–	low Z_{out}
OP-44E	120	16	88	90	114	15	40	–	–	–	–	
357B	50	20	85	85	94	20	30	•	–	–	–	decomp 356
AD380K	330	300	60	60	92	60	20	–	–	–	–	hybrid, fast, 50Ω
LF401A	30	16	90	80	100	50	32	–	–	–	–	accurate
OPA404B	35	6.4	92	86	92	10	36	–	–	–	–	accurate quad
LF457B	50	20	86	86	106	100[l]	40	•	–	–	–	low noise; drives 0.01μF
OPA602C	35	6.5	92	86	92	20	36	–	–	–	–	low bias, fast settle
OPA605K	94	20	80	74	104[t]	30	20	–	–	–	–	uncomp
OPA606L	35	13	85	90	100	10	36	–	–	–	–	improved LF356
AD744C	75	13	86	92	108	20	36	–	–	–	–	very low dist (3ppm); fast settle
AD843B	250	35	100	95	88	50	-	–	–	–	–	fast settle
AD845K	100	16	94	98	106	25	20	–	–	–	–	fast settle
LT1022A	26	8.5	86	88	104	10	40	–	–	–	–	
HA5160	120	100	74	108	98	22	40	–	–	–	–	low bias
MC34080A	50	16	75	75	94	20	44	–	–	–	–	$V_{in} > V_-+4V$; decomp 34081
MC34081A	25	8	75	75	94	20	44	–	–	–	–	$V_{in} > V_-+4V$
TL031C	3	1	75	75	74	8	30	•	–	–	–	low power; improved TL061
TL051C	24	3	75	75	94	30	30	•	–	–	–	low dist; improved TL071/081
TL061C	3.5	1	70	70	70	5	30	–	–	–	–	low power
TL071C	13	3	70	70	88	10	30	–	–	–	–	lower noise
TL081B	13	3	80	80	94	10	30	–	–	–	–	
OPA121	2	2	86	86	110	10	36	–	–	–	–	low noise
OPA128L	3	1	90	90	110	10	36	–	–	–	–	very low bias
LF351	13	4	70	70	88	10	30	•	–	–	–	353=dual, 347=quad
355B	5	2.5	85	85	94	20	30	•	–	–	–	popular
356B	12	5	85	85	94	20	30	•	–	–	–	faster 355
LF411	15	4	70	70	88	20	30	•	–	–	–	jellybean
LF*nnn*	20	10	80	80	100	15	2	•	–	–	–	lowest noise JFET
LF441	1	1	70	70	88	4	30	•	–	–	–	low current jellybean
LF455B	5	3	86	86	106	100[l]	40	•	–	–	–	low noise; drives 0.01μF
LF456B	12.5	5	86	86	106	100[l]	40	•	–	–	–	low noise; drives 0.01μF
AD549L	3	1	90	90	110	10	36	–	–	–	–	electrometer; guard pin
AD611K	13	2	80	80	94	20	20	–	–	–	–	low dist, gen purp JFET
LT1057A	13	5	86	88	104	10	40	–	–	–	–	accurate dual/quad JFET
HA5180	7	2	90	90	106	15	40	–	–	–	–	very low bias over temp; noisy
MC34001A	13	4	80	80	94	20	30	•	–	–	–	
MC34181	10	4	70	70	88	8	36	–	–	–	–	low power, fast, low dist.

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[c]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
JFET, OBSOLESCENT																	
OP-15E	PM+	•	A	–	•	–	1	10	44	4	0.2	0.5	2	5	0.05	0.01	15
OP-16E	PM+	•	–	–	•	–	1	10	44	7	0.2	0.5	2	5	0.05	0.01	15
AD515L	AD	•	–	–	•	–	1	10	36	1.5	0.4	1	-	25	80fA	80fA	50
AD542L	AD	•	–	–	•	–	1	10	36	1.5	-	0.5	-	5	0.025	2pA[t]	30
AD544L	AD	•	–	–	•	–	1	10	36	2.5	-	0.5	-	5	0.05	0.5pA[t]	18
AD545L	AD	•	–	–	•	–	1	10	36	1.5	-	0.5	-	5	0.001	-	35
ICH8500A	IL	•	–	–	•	–	1	16	36	2.5	-	50	-	-	10fA	10fA	40
MOSFET																	
OP-80E	PM	•	–	–	•	–	1	4.5	16	0.2	0.4	1	-	-	60fA	10fA[t]	70
TLC27L2A	TI	A	•	A	–	–	1	3	18	0.04	-	5	0.7	-	1pA[t]	1pA[t]	70
TLC27M2A	TI	A	•	A	–	–	1	3	18	0.6	-	5	2	-	1pA[t]	1pA[t]	38
TLC272A	TI	A	•	A	–	–	1	3	18	4	-	5	5	-	1pA[t]	1pA[t]	25
TLC279C	TI	–	–	•	–	–	1	3	18	8	0.4	1.2	2	-	0.7pA[t]	0.1pA[t]	25
LMC660A	NS	–	–	•	–	–	1	5	16	2.2	1	2	1.3	5	20pA	20pA	22
TLC1078C	TI	–	•	A	–	–	1	1.4	16	0.05	0.18	0.6	1	-	0.7pA[t]	0.1pA[t]	68
ALD1701	AL	•	–	–	–	–	1	2	12	0.25	-	4.5	7	-	0.03	0.025	-
ALD1702	AL	•	–	–	–	–	1	2	12	2	-	4.5	7	-	0.03	0.025	100
CA3140A	RC	•	A	–	•	–	1	4	44	6	2	5	6	-	0.04	0.02	40
CA3160A	RC	•	A	–	•	•	1	5	16	15	2	5	10	-	0.03	0.02	72
CA3410A	RC	–	–	•	–	–	1	4	36	10	3	8	10	-	0.03	0.01	40
CA3420A	RC	•	–	–	•	•	1	2	22	1	2	5	4	-	0.005	0.004	62
CA5160A	RC	•	A	–	•	•	1	5	15	0.4	1.5	4	-	-	0.01	0.005	-
CA5420A	RC	•	–	–	•	•	1	2	20	0.5	1	5	-	-	0.001	0.5pA	-
CA5422	RC	•	–	–	•	–	1	2	20	0.7	1.8	10	20	-	0.005	0.004	-
ICL7612B	IL+	•	–	–	–	–	1	3	18	2.5	-	5	5	-	0.05	0.03	100
ICL7641B	IL+	A	A	•	–	–	1	1	18	2.5	-	5	5	-	0.05	0.03	100
CHOPPER STABILIZED																	
MAX420E	MA	•	–	–	–	–	1	6	33	2	0.001	0.005	0.02	0.05	0.03	0.06	1.1[j]
MAX422E	MA	•	–	–	–	–	1	6	33	0.5	0.001	0.005	0.02	0.05	0.03	0.06	1.1[j]
LMC668A	NS	•	–	–	–	–	1	5	16	3.5	0.001	0.005	0.05	-	0.06	-	2[j]
TSC900A	TS	•	–	–	–	–	1	4.5	16	0.2	-	0.005	0.02	0.05	0.05	0.5pA[t]	4[j]
TSC901	TS	•	A	A	–	–	1	5	32	0.6	0.007	0.015	0.05	0.15	0.05	0.1	5[j]
TSC911A	TS	•	A	A	–	–	1	4	16	0.6	0.005	0.015	0.05	0.15	0.07	0.02	11[j]
TSC915	TS	•	–	–	–	–	1	7	32	1.5		0.01	0.01	0.1	0.1	0.1	0.8[j]
TSC918	TS	•	–	–	–	–	1	4.5	16	0.8	-	0.05	0.4	0.8	0.1	0.5pA[t]	4[j]
LTC1050	LT	•	–	–	–	–	1	4.8	16	1.5	0.5μV	0.005	0.01	0.05	0.03	0.06	1.6[j]
LTC1052	LT	•	–	–	–	–	1	4.8	16	2	0.5μV	0.005	0.01	0.05	0.03	0.03	1.5[j]
ICL7650	IL+	•	–	–	–	–	1	4.5	16	3.5	0.002	0.005	0.1	-	0.01	5pA[t]	2[j]
ICL7650S	IL	•	–	–	–	–	1	4.5	16	3	0.7μV	0.005	0.02	0.1	0.01	0.02	2[j]
ICL7652	IL+	•	–	–	–	–	1	5	16	3.5	0.002	0.005	0.1	-	0.03	25pA[t]	0.7[j]
ICL7652S	IL	•	–	–	–	–	1	5	16	2.5	0.7μV	0.005	0.01	0.06	0.03	0.04	0.7[j]
TSC76HV52	TS	•	–	–	–	–	1	7	32	1.5	-	0.01	-	0.3	0.1	0.1	0.8[j]

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Type	Slew rate[e] typ (V/µs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-15E	17	6	86	86	100	15	40	−	−	−	−	precision fast 355
OP-16E	25	8	86	86	100	20	40	−	−	−	−	precision fast 356 (OP-17=decomp)
AD515L	1	0.4	70	74	94	10	20	−	−	−	−	very low bias, precision
AD542L	3	1	80	80	110	10	20	−	−	−	−	precision
AD544L	13	2	80	80	94	15	20	−	−	−	−	precision, low noise
AD545L	1	0.7	76	74[t]	92	10	20	−	−	−	−	precision
ICH8500A	0.5	0.5	60	80[t]	100[t]	10	0.5	−	−	−	−	ultra low bias
OP-80E	0.4	0.3	60	60	100	10	16	−	•	−	•	electrometer; I_b<20pA @ 125°C
TLC27L2A	0.04	0.1	70	70	90	10	18	−	•	−	•	CMOS jellybeans
TLC27M2A	0.6	0.7	70	70	86	10	18	−	•	−	•	CMOS jellybeans
TLC272A	4.5	2.3	70	65	80	10	18	−	•	−	•	CMOS jellybeans
TLC279C	4.5	2.3	65	65	80	10	18	−	•	−	•	best V_{os} of 272-series
LMC660A	1.7	1.5	72	80	112	15	16	−	•	•	•	quad CMOS jellybean
TLC1078C	0.05	0.11	75	75	114	15	16	−	•	−	•	low offset
ALD1701	0.7	0.7	65	65	90	0.5	12	•	•	•	•	rail-to-rail; specs @ +5V supply
ALD1702	2.1	1.5	65	65	94	2	12	•	•	•	•	rail-to-rail; specs @ +5V supply
CA3140A	7	3.7	70	76	86	+10,-1	8	−	•	−	•	
CA3160A	10	4	80	76	94	12	8	−	•	•	•	MOS in/out (3130=uncomp)
CA3410A	10	5.4	80	80	86	6	16	−	•	−	−	high speed 324-type replacement
CA3420A	0.5	0.5	60	70	86	2	15	−	•	•	•	low I_b, good input protec.
CA5160A	10	4	-	-	90	1	?	−	•	•	•	CMOS output
CA5420A	0.5	0.5	-	-	85	0.5	15	−	•	•	•	similar to 3420
CA5422	1	1	60	60	80	2	15	−	•	•	•	unusual 2-section design
ICL7612B	1.6	1.4	60	70	80	5[m]	18	•	•	•	•	programmable; in/out to both rails
ICL7641B	1.6	1.4	60	70	80	5[m]	18	•	−	•	•	gen purp, low voltage
MAX420E	0.5	0.5	120	120	120	+2,-15	33	−	•	•	•	±15V V_s; 0.1µV/mo; 430 has C_{int}
MAX422E	0.13	0.13	120	120	120	+0.2,-8	33	−	•	•	•	±15V V_s; 0.1µV/mo; 432 has C_{int}
LMC668A	2.5	1	120	120	120	+5,-15	16	−	•	•	•	
TSC900A	0.2	0.7	110	120	120	2.5	16	−	•	−	•	low power
TSC901	2	0.8	120	120	120	-	36	−	•	−	•	±15V supply; int caps
TSC911A	2.5	1.5	110	112	116	3.5	16	−	•	−	•	int caps, noisy
TSC915	0.5	0.5	120	120	120	10	36	−	•	−	•	±15V supply
TSC918	0.2	0.7	98	105	100	-	16	−	•	−	•	inexpensive
LTC1050	4	2.5	120	125	130	+3,-20	16	−	•	•	•	int caps; 50nV/√month
LTC1052	4	1.2	120	120	120	+5,-15	16	−	•	•	•	improved 7652; 0.1µV/month
ICL7650	2.5	2	110	120	120	+5,-20	16	−	•	•	•	0.1µV/month
ICL7650S	2.5	2	120	120	136	+4,-20	16	−	•	•	•	improved 7650; 0.1µV/month
ICL7652	0.5	0.4	110	110	120	+5,-20	16	−	−	•	•	0.15µV/month
ICL7652S	1	0.5	120	120	136	+4,-20	16	−	−	•	•	improved 7652; 0.15µV/month
TSC76HV52	0.5	0.5	120	120	120	10	32	−	−	•	•	±15V supply

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
HIGH VOLTAGE																	
LM343	NS	•	–	–	•	–	1	10	68	5	2	8	-	-	40	10	35
LM344	NS	•	–	–	•	•	U	10	68	5	2	8	-	-	40	10	35
OPA445B	BB	•	–	–	•	–	1	20	100	4.5	1	3	10	-	0.05	0.01	16
1436	MO+	•	–	–	•	–	1	10	80	5	5	10	-	-	40	10	50
HA2645	HA	•	–	–	•	•	1	20	80	4.5	2	6	15	-	30	30	30
3580	BB	•	–	–	•	–	1	30	70	10	-	10	-	30	0.05	-	15
3581	BB	•	–	–	•	–	1	64	150	8	-	3	-	25	0.02	0.02	25
3582	BB	•	–	–	•	–	1	140	300	6.5	-	3	-	25	0.02	-	25
3583	BB	•	–	–	•	–	1	100	300	8.5	-	3	-	25	0.1	0.1	50
3584	BB	•	–	–	•	•	U	140	300	6.5	-	3	-	25	0.1	0.1	50
MONOLITHIC POWER																	
LM12	NS	•	–	–	–	–	1	20	80	80	2	7	-	50	300	100	90
OPA541B	BB	•	–	–	–	–	1	20	80	25	0.1	1	15	30	0.05	0.03	50
LM675	NS	•	–	–	–	–	10	16	60	50	1	10	25	-	2μA	500	-
SG1173	SG	•	–	–	–	–	1	10	50	20	2	4	-	30	500	150	-

[a] manufacturers are as follows (a "+" suffix designates multiple sources):

AD - Analog Devices
AL - Advanced Linear Devices
AM - Advanced Micro Devices
AN - Analogic
AP - Apex
BB - Burr-Brown
BT - Brooktree
CL - Comlinear
CR - Crystal Semiconductor
CY - Cypress
DA - Datel
EL - Elantec
FA - Fairchild (National)
FE - Ferranti
GE - General Electric
GI - General Instrument
HA - Harris
HI - Hitachi
HO - Honeywell
HS - Hybrid Systems
ID - Integrated Device Technology
IL - GE/Intersil
IN - Intel
IR - International Rectifier
KE - M.S.Kennedy Corp
LT - Linear Technology Corp
MA - Maxim
MN - Micro Networks
MO - Motorola
MP - Micro Power Systems
NE - NEC
NS - National Semiconductor
OE - Optical Electronics Inc
PL - Plessey
PM - Precision Monolithics
RA - Raytheon
RC - GE/RCA
RO - Rockwell
SG - Silicon General
SI - Siliconix
SN - Signetics
SO - Sony
ST - Supertex
TI - Texas Instruments
TM - Telmos
TO - Toshiba
TP - Teledyne Philbrick
TQ - TriQuint
TR - TRW
TS - Teledyne Semiconductor
VT - VTC
XI - Xicor
XR - Exar
ZI - Zilog

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Type	Slew rate[e] typ (V/μs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
LM343	2.5	1	70	74	97	10	68	–	–	–	–	monolithic
LM344	30	10	70	74	97	10	68	–	–	–	–	uncomp 343
OPA445B	10	2	80	80	100	15	80	–	–	–	–	low-bias, monolithic
1436	2	1	70	80	97	10	80	–	–	–	–	monolithic
HA2645	5	4	74	74	100	10	37	–	–	–	–	monolithic
3580	15	5	86[t]	87[t]	106[t]	60	70	–	–	–	–	hybrid
3581	20	5	110[t]	105[t]	112[t]	30	150	–	–	–	–	hybrid
3582	20	5	110[t]	105[t]	118[t]	15	300	–	–	–	–	hybrid
3583	30	5	110[t]	84[t]	94	75	300	–	–	–	–	fast JFET, hybrid
3584	150	20	110[t]	84[t]	100	15	300	–	–	–	–	uncomp JFET, hybrid
LM12	9	0.7	75	80	94	10A	80	–	–	–	–	full output protection
OPA541B	10	1.6	95	100	90	10A	80	–	–	–	–	isolated case; no int. protec.
LM675	8	5.5	70	70	70	3000	60	–	–	–	–	full output protection
SG1173	0.8	1	76	80	92	3500	50	–	–	–	–	thermal shutdown

[b] the symbol • indicates the number of op-amps per package for the part number shown; an "A" indicates the availability of other quantities of op-amps per package from the same manufacturer; some electrical characteristics (particularly offset voltage) may be degraded somewhat in multiple packages.
[c] pins are provided for external compensation.
[d] a number gives the minimum closed-loop gain without instability. Op-amps with pins for external compensation can generally be operated at lower gain, if an appropriate ext comp network is used. The letter U means that the op-amp is uncompensated – external capacitance is necessary for any small value of closed-loop gain.
[e] at minimum stable closed-loop gain (usually unity gain), unless otherwise noted.
[f] the maximum value without damage to the chip; not to exceed the total supply voltage used, if that is less.
[g] a dot in an IN column means that the input operating common-mode range includes that supply rail; a dot in an OUT column means that the op-amp can swing its output all the way to the corresponding supply rail.
[h] resistor-diode network draws input current for input differential greater than ±1V.
[j] μV pp, 0.1-10Hz.
[k] current-sensing inverting input ("current feedback" configuration); the bias currents at the two inputs may differ widely. The listed bias current is for the non-inverting input.
[l] "raw" output (no current limit) available at pin 8, in addition to the conventional (protected) output at pin 6; the latter is limited to ±15mA.
[m] min/max (worst case).
[t] typical.

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TABLE 4.2. RECOMMENDED OP-AMPS

Type	Mfg[a]	Amps per package[b] 1	2	4	Offset voltage max (mV)	Offset drift max (μV/°C)	Input curr max (nA)	Total supply voltage min (V)	Total supply voltage max (V)	Supply curr max (mA)	e_n, typ 10Hz (nV/√Hz)	e_n, typ 1kHz (nV/√Hz)	Slew rate typ (V/μs)	f_T typ (MHz)	Comments
LF411	NS	•	A	–	2	20	0.2	10	36	3.4	50	25	15	4	general purpose jellybean
AD711K	AD	•	A	–	0.5	10	0.05	9	36	3	45	18	20	4	improved LF411
LM358A	NS+	–	•	A	3	20	100	3	32	1.2	–	–	0.5	1	single supply jellybean
TLC27M2A	TI	A	•	A	5	2[t]	0.001[t]	3	18	0.6	–	–	0.6	0.7	CMOS jellybean
OP-27E	PM+	•	A	A	0.025	0.6	40	8	44	5	3.5	3.0	2.8	8	precision, low-noise
OP-37E	PM+	•	A	–	0.025	0.6	40	8	44	5	3.5	3.0	17[h]	63[h]	ditto, faster (decomp. min. gain = 5)
HA5147A	HA	•	–	–	0.025	0.6	40	8	44	4	3.5	3.0	35[c]	140[c]	ditto, still faster (min. gain = 10)
OP-77E	PM	•	A	A	0.025	0.3	2	6	44	2	10.3	9.6	0.3	0.6	precision
LT1028A	LT	•	–	–	0.04	0.8	90	8	44	9.5	1.0	0.85	15	75	precision ultra-low-noise
LT1013A	LT	–	•	A	0.15	2	35	4	44	1	24	22	0.4	0.8	precision single-supply
LT1055A	LT	•	–	–	0.15	4	0.05	10	40	4	28	14	13	5	precision JFET
LT1012C	LT+	•	A	–	0.05	1.5	0.15	4	40	0.6	17	14	0.2	0.8	precision low-bias
OPA111B	BB	•	A	–	0.25	1	0.001	10	36	3.5	30	7	2	2	precision low-bias JFET
AD744K	AD	•	–	–	0.5	10	0.1	9	36	4	45	18	75[f]	13[f]	ultra low dist, stable, fast settle
LTC1052	IL+	•	–	–	0.005	0.05	0.03	4.8	16	2	–	–	4	1.2	chopper
OP-90E	PM	•	A	A	0.15	2	15	1.6	36	0.02	60	60	0.012	0.02	precision micropower
CA3440A	RC	•	–	–	5	4[t]	0.04	4	15	(d)	250	110	0.003[e]	0.005[e]	nanopower (programmable)
AD549L	AD	•	–	–	0.5	10	60fA	10	36	0.7	90	35	3	1	ultra low input current JFET
LM10	NS+	•	–	–	2	2[t]	20	1.1	40	0.4	50	46	0.1	0.4	low supply voltage, rail-to-rail output

[a] see footnotes to Table 4.1. [b] • = this part number; A = available. [c] G>10. [d] programmable 0.02μA–10μA. [e] at I_S=1μA. [f] G>2. [h] G>5.
[m] min/max. [t] typical.

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op-amps with the very lowest input currents (MOSFET types) generally have poor voltage offsets, and vice versa. Good circuit designers choose their components with the right trade-offs to optimize performance, without going overboard on unnecessary "gold-plated" parts.

Limitations imply trade-offs

The limitations of op-amp performance we have talked about will have an influence on component values in nearly all circuits. For instance, the feedback resistors must be large enough so that they don't load the

"Here Yesterday, Gone Today"

In its untiring quest for better and fancier chips, the semiconductor industry can sometimes cause you great pain. It might go something like this: You've designed and prototyped a wonderful new gadget; debugging is complete, and you're ready to go into production. When you try to order the parts, you discover that a crucial IC has been discontinued by the manufacturer! An even worse nightmare goes like this: Customers have been complaining about late delivery on some instrument that you've been manufacturing for many years. When you go to the assembly area to find out what's wrong, you discover that a whole production run of boards is built, except for one IC that "hasn't come in yet." You then ask purchasing why they haven't expedited the order; turns out they have, just haven't received it. Then you learn from the distributor that the part was discontinued six months ago, and that none is available!

Why does this happen, and what do you do about it? We've generally found four reasons that ICs are discontinued:

1. *Obsolescence:* Much better parts come along, and it doesn't make much sense to keep making the old ones. This has been particularly true with digital memory chips (e.g., small static RAMs and EPROMs, which are superseded by denser and faster versions each year), though linear ICs have not entirely escaped the purge. In these cases there is often a pin-compatible improved version that you can plug into the old socket.
2. *Not selling enough:* Perfectly good ICs sometimes disappear. If you are persistent enough, you may get an explanation from the manufacturer – "there wasn't enough demand," or some such story. You might characterize this as a case of "discontinued for the convenience of the manufacturer." We've been particularly inconvenienced by Harris's discontinuation of their splendid HA4925 – a fine chip, the fastest quad comparator, now gone, with no replacement anything like it. Harris also discontinued the HA2705 – another great chip, the fastest low-power op-amp, now gone without a trace! Sometimes a good chip is discontinued when the wafer fabrication line changes over to a larger wafer size (e.g., from the original 3″ diameter wafer to a 5″ or 6″ wafer). We've noticed that Harris has a particular fondness for discontinuing excellent and unique chips; Intersil and GE have done the same thing.
3. *Lost schematics:* You might not believe it, but sometimes the semiconductor house loses track of the schematic diagram of some chip and can't make any more! This apparently happened with the Solid State Systems SSS-4404 CMOS 8-stage divider chip.
4. *Manufacturer out of business:* This also happened to the SSS-4404!

If you're stuck with a board and no available IC, you've got several choices. You can redesign the board (and perhaps the circuit) to use something that is available. This is probably best if you're going into production with a new design or if you are running a large production of an existing board. A cheap and dirty solution is to make a little "daughterboard" that plugs into the empty IC socket and includes whatever it takes to emulate the nonexistent chip. Although this latter solution isn't terribly elegant, it gets the job done.

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output significantly, but they must not be so large that input bias current produces sizable offsets. High impedances in the feedback network also increase susceptibility to capacitive pickup of interfering signals and increase the loading effects of stray capacitance. These trade-offs typically dictate resistor values of 2k to 100k with general-purpose op-amps.

Similar sorts of trade-offs are involved in almost all electronic design, including the simplest circuits constructed with transistors. For instance, the choice of quiescent current in a transistor amplifier is limited at the high end by device dissipation, increased input current, excessive supply current, and reduced current gain, whereas the lower limit of operating current is limited by leakage current, reduced current gain, and reduced speed (from stray capacitance in combination with the high resistance values). For these reasons you typically wind up with collector currents in the range of a few tens of microamps to a few tens of milliamps (higher for power circuits, sometimes a bit lower in "micropower" applications), as mentioned in Chapter 2.

In the next three chapters we will look more carefully at some of these problems in order to give you a good understanding of the trade-offs involved.

EXERCISE 4.6

Draw a dc-coupled inverting amplifier with gain of 100 and $Z_{\text{in}} = 10\text{k}$. Include compensation for input bias current, and show offset voltage trimming network (10k pot between pins 1 and 5, wiper tied to V_-). Now add circuitry so that $Z_{\text{in}} \geq 10^8$ ohms.

4.13 Low-power and programmable op-amps

For battery-powered applications there is a popular group of op-amps known as "programmable op-amps," because all of the internal operating currents are set by an externally applied current at a bias programming pin. The internal quiescent currents are all related to this bias current by current mirrors, rather than by internal resistor-programmed current sources. As a consequence, such amplifiers can be programmed to operate over a wide range of supply currents, typically from a few

POPULAR OP-AMPS

Sometimes a new op-amp comes along at just the right time, filling a vacuum with its combination of performance, convenience, and price. Several companies begin to manufacture it (it becomes "second-sourced"), designers become familiar with it, and you have a hit. Here is a list of some popular favorites of recent times:

301 First easy-to-use op-amp; first use of "lateral *pnp*." External compensation. National.

741 The industry standard for many years. Internal compensation. Fairchild.

1458 Motorola's answer to the 741; two 741s in a mini-DIP, with no offset pins.

308 National's precision op-amp. Low power, superbeta, guaranteed drift specifications.

324 Popular quad op-amp (358=dual, mini-DIP). Single-supply operation. National.

355 All-purpose bi-FET op-amp (356, 357 faster). Practically as precise as bipolar, but faster and lower input current. National. (Fairchild tried to get the FET ball rolling with their 740, which flopped because of poor performance. Would you believe 0.1V input offset?)

TL081 Texas Instruments' answer to the 355 series. Low-cost comprehensive series of singles, duals, quads; low power, low noise, many package styles.

LF411 National's improved bi-FET series. Low offset, low bias, fast, low distortion, high output current, low cost. Dual (LF412) and low-power variants (LF441/2/4).

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microamps to a few milliamps. The slew rate, gain-bandwidth product f_T, and input bias current are all roughly proportional to the programmed operating current. When programmed to operate at a few microamps, programmable op-amps are extremely useful in battery-powered circuits. We will treat micropower design in detail in Chapter 14.

The 4250 was the original programmable op-amp, and it is still a good unit for many applications. Developed by Union Carbide, this classic is now "second-sourced" by many manufacturers, and it even comes in duals and triples (the 8022 and 8023, respectively). As an example of the sort of performance you can expect for operation at low supply currents, let's look at the 4250 running at 10μA. To get that operating current, we have to supply a bias current of 1.5μA with an external resistor. When it is operated at that current, f_T is 75kHz, the slew rate is 0.05V/μs, and the input bias current I_B is 3nA. At low operating currents the output drive capability is reduced considerably, and the open-loop output impedance rises to astounding levels, in this case about 3.5k. At low

THE 741 AND ITS FRIENDS

Bob Widlar designed the first really successful monolithic op-amp back in 1965, the Fairchild μA709. It achieved great popularity, but it had some problems, in particular the tendency to go into a latch-up mode when the input was overdriven and its lack of output short-circuit protection. It also required external frequency compensation (two capacitors and one resistor) and had a clumsy offset trimming circuit (again requiring three external components). Finally, its differential input voltage was limited to 5 volts.

Widlar moved from Fairchild to National, where he went on to design the LM301, an improved op-amp with short-circuit protection, freedom from latch-up, and a 30-volt differential input range. Widlar didn't provide internal frequency compensation, however, because he liked the flexibility of user compensation. The 301 could be compensated with a single capacitor, but because there was only one unused pin remaining, it still required three external components for offset trimming.

Meanwhile, over at Fairchild the answer to the 301 (the now-famous 741) was taking shape. It had the advantages of the 301, but Fairchild engineers opted for internal frequency compensation, freeing two pins to allow simplified offset trimming with a single external trimmer. Since most circuit applications don't require offset trimming (Widlar was right), the 741 in normal use requires no components other than the feedback network itself. The rest is history – the 741 caught on like wildfire and became firmly entrenched as the industry standard.

There are now numerous 741-type amps, essentially similar in design and performance, but with various features such as FET inputs, dual or quad units, versions with improved specifications, decompensated and uncompensated versions, etc. We list some of them here for reference and as a demonstration of man's instinct to clutch onto the coattails of the famous (see Table 4.1 for a more complete listing).

Single units		*Dual units*		*Quad units*	
741S	fast (10V/μs)	747	dual 741	MC4741	quad 741(alias 348)
MC741N	low noise	OP-04	precision	OP-11	precision
OP-02	precision	1458	mini-DIP package	4136	fast (3MHz)
4132	low power (35μA)	4558	fast (15V/μs)	HA4605	fast (4V/μs)
LF13741	FET low input current	TL082	FET, fast (similar to LF353)	TL084	FET, fast (similar to LF347)
748	uncompensated				
NE530	fast (25V/μs)	LF412	FET, fast		
TL081	FET, fast (similar to LF351)				
LF411	FET, fast				

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operating currents the input noise voltage rises, while the input noise current drops (see Chapter 7). The 4250 specifications claim that it can run from as little as 1 volt total supply voltage, but the claimed minimum supply voltages of op-amps may not be terribly relevant in an actual circuit, particularly where any significant output swing or drive capability is needed.

The 776 (or 3476) is an upgraded 4250, with better output-stage performance at lower currents. The 346 is a nice quad programmable op-amp, with three sections programmed by one of the programming inputs, and the fourth programmed by the other. Some other programmable op-amps constructed with ordinary bipolar transistors are the OP-22, OP-32, HA2725, and CA3078. Programmable CMOS op-amps include the ICL7612, TLC251, MC14573, and CA3440. These feature operation at very low supply voltage (down to 1V for the TLC251) and, for the astounding 3440, operation at quiescent currents down to 20 *nano*amps. The 7612 and 251 use a variation of the usual programming scheme; their quiescent current is pin-selectable (10μA, 100μA, or 1mA), according to whether the programming pin is connected to V_+ or V_- or is left open.

In addition to these op-amps, there are several nonprogrammable op-amps that have been designed for low supply currents and low-voltage operation and should be considered for low-power applications. Notable among these is the outstanding bipolar LM10, an op-amp that is fully specified at 1 volt total supply voltage (±0.5V, for example). This is extraordinary, considering that V_{BE} increases with decreasing temperature and is close to 1 volt at −55°C, the lower limit of the LM10's operating range. Some other excellent "micropower" op-amps (and their operating currents) are the precision OP-20 (40μA), OP-90 (12μA), and LT1006 (90μA), the inexpensive quad LP324 (20μA per amplifier), the JFET LF441/2/4 (150μA per amplifier), and the MOSFET TLC27L4 (10μA per amplifier).

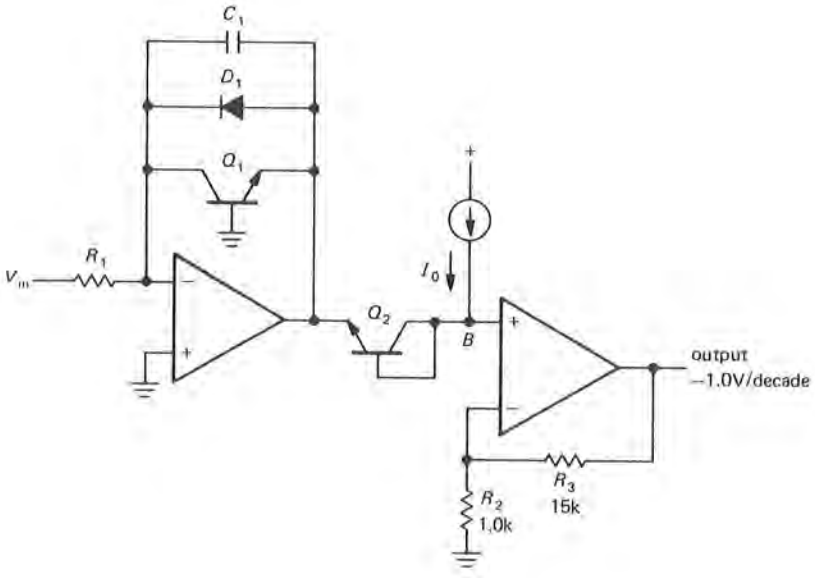


Figure 4.35. Logarithmic converter. Q_1 and Q_2 compose a monolithic matched pair.

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TABLE 4.3. HIGH-VOLTAGE OP-AMPS

Type	Mfg[a]	Total supply min (V)	Total supply max (V)	Diff'l input[b] max (V)	FET	Ext comp	Trim	f_T typ (MHz)	Slew rate typ (V/μs)	Output current max (mA)	P_{diss} (50°C) max (W)	Therm lim	Case[c]	Comments
LM675	NS	20	60	60	–	–	–	5.5	8	3000	40	•	TO-220	monolithic pwr op-amp
LM343	NS	10	68	68	–	–	•	1	2	20	0.6	–	TO-99	superbeta
LM344	NS	10	68	68	–	•	–	1	30[d]	20	0.6	–	TO-99	superbeta
3580	BB	30	70	70	•	–	•	5	15	60	4.5	•	TO-3I	
LM12	NS	20	80	80	–	–	–	0.7	9	10000	90	•	TO-3	monolithic high-power
PA19	AP	30	80	40	•	•	–	100[e]	650[d]	5000	70	•	TO-3I	VMOS output
OPA541	BB	20	80	80	•	–	–	2	10	10000	90	–	TO-3I	monolithic high-pwr
MC1436	MO	10	80	80	–	–	•	1	2	10	0.6	–	TO-99	original, still good
1460	TP	30	80	6	–	•	•	1000[e]	300[e]	150	2.5	–	TO-3	VMOS output
1461	TP	30	80	25	•	•	•	1000[e]	1200[e]	750		–	P-DIP	VMOS output
1463	TP	30	80	25	•	–	•	17	165	1000	40	–	TO-3	fast unity-gain comp
HA2645	HA	20	80	74	–	•	•	4	5	10	0.6	•	TO-99	same as Philbrick 1332
OPA445	BB	20	100	80	•	–	•	2	10	15	0.6	–	TO-99	monolithic; miniDIP also
1481	TP	30	150	150	•	–	•	4.5	25	80	15	–	TO-3	current limit
3581	BB	65	150	150	•	–	•	5	20	30	4.5	•	TO-3I	
PA04	AP	30	200	20	•	•	–	2	50	20000	160	–	P-DIP	VMOS output; curr lim
1480	TP	30	300	450	•	–	•	20	100	80		•	TO-3	
3582	BB	140	300	300	•	–	•	5	20	15	4.5	•	TO-3I	
3583	BB	80	300	300	•	–	•	5	30	75	10	•	TO-3	
3584	BB	140	300	300	•	•	•	20[e]	150[e]	15	4.5	•	TO-3	
PA08V	AP	30	340	50	•	–	•	5	30	150	18	•	TO-3I	low V_{os}, low e_n
PA88	AP	30	450	25	•	•	–	1[d]	30[e]	100	12	•	TO-3I	low I_O, V_{os}, e_n, VMOS
PA85	AP	30	450	25	•	•	–	20[d]	1000[e]	200	28	•	TO-3I	low V_{os}, low e_n, VMOS

[a] see notes to Table 4.1. [b] not to exceed total supply voltage. [c] "I" = isolated. [d] when comp for G>10. [e] when comp for G>100.

A DETAILED LOOK AT SELECTED OP-AMP CIRCUITS

The performance of the next few circuits is affected significantly by the limitations of op-amps; we will go into a bit more detail in their description.

4.14 Logarithmic amplifier

The circuit shown in Figure 4.35 exploits the logarithmic dependence of V_{BE} on I_C to produce an output proportional to the logarithm of a positive input voltage. R_1 converts V_{in} to a current, owing to the virtual ground at the inverting input. That current flows through Q_1, putting its emitter one V_{BE} drop below ground, according to the Ebers-Moll equation. Q_2, which operates at a fixed current, provides a diode drop of correction voltage, which is essential for temperature compensation. The current source (which can be a resistor, since point B is always within a few tenths of a volt of ground) sets the input current at which the output voltage is zero. The second op-amp is a noninverting amplifier with a voltage gain of 16, in order to give an output voltage of -1.0 volt per decade of input current (recall that V_{BE} increases 60mV per decade of collector current).

Some further details: Q_1's base could have been connected to its collector, but the base current would then have caused an error (remember that I_C is an accurate exponential function of V_{BE}). In this

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TABLE 4.4. POWER OP-AMPS

Type	Mfg[a]	monolithic	FET	Trim?	Pkg[b]	I_{out} (A)	$\pm V_{supply}$ min (V)	$\pm V_{supply}$ max (V)	P_{diss} (W)	SR typ (V/µs)	f_T typ (MHz)	pwr BW (kHz)	V_{os}(max) (mV)	V_{os}(max) (µV/°C)	V_{os}(max) (µV/W)
PA03	AP	–	•	•	PD	30	15	75	500	10	5	70	3	30	20[t]
PA04A	AP	–	•	–	PD	20	15	100	200	50	2	90	5	30	10[t]
OPA512	BB	–	–	–	3I	15	10	50	125	4	4	20	3	40	20[t]
LM12	NS	•	–	–	3	10	10	40	90	9	0.7	60	7	50	50
OPA501	BB	–	–	–	3I	10	10	40	80	1.4[m]	1	16	5	40	35[t]
OPA512B	BB	–	–	–	3I	10	10	50	125	4	4	20	6	65	20[t]
OPA541B	BB	•	•	–	3I	10	10	40	90	10	2	55	2	30	60
1468	TP	–	–	–	3	10	10	50	125	4	4	20	6	65	20[t]
PA19A	AP	–	•	–	3I	5	15	40	70	900	100	3500	0.5	10	20[t]
OPA511	BB	–	–	–	3I	5	10	30	67	1.8	1	23	10	65	20[t]
PA09A	AP	–	•	•	3I	4	10	40	78	400	75	2500	0.5	10	
SG1173	SG	•	–	–	220	3.5	5	25	20	0.8	1		4	30	-
LM675	NS	•	–	–	220	3	8	30	40	8	5.5		10	25[t]	25[t]
LH0101	NS	–	•	–	3	2	5	20	62	10	5	300	3	10[t]	150[t]
3572	BB	–	•	–	3I	2	15	40	60	3	0.5	16	2	40	20[t]
3573	BB	–	–	–	3I	2	10	34	45	1.5	1	23	10	65	
LH0021	NS	–	–	–	3	1	5	15	23	3	1	20	3	25	15
MSK792	KE	–	–	•	3	1	5	22	5	2	1	11	0.1	2	-
1463	TP	–	•	•	3	1	15	40	40	165	17		5	20[t]	
1461	TP	–	•	•	PD	0.75	15	40		1200[u]	1000[u]		5	50	-
LH0061	NS	–	–	•	3	0.5	-	15	20	70	-	1000	4	5[t]	5[t]
WA01A	AP	–	–	•	3I	0.4	12	16	10	4000	1000	150000	5	25	10[t]
CLC203	CL	–	–	–	PD	0.2	9	20		6000	5000	60000	1.5	15	
1460	TP	–	–	•	3	0.15	15	40	2.5	300[u]	1000[u]	1500	5	50	-
3554B	BB	–	•	•	3I	0.15	5	18	5	1200	100	19000	1	15	-
HA2542	HA	•	–	•	D	0.1	5	15	1.6	375	120	4700[m]	10[m]	20	-
LH4101	NS	–	•	•	D	0.1	-	15	4	250	28	-	15	25[t]	-
LH4104	NS	–	•	•	C	0.1	-	15	2.5	40	18	-	5	20[t]	-
1480	TP	–	•	•	3	0.08	15	150		100	20	120	3	100	-
1481	TP	–	•	•	3	0.08	15	75	15	25	4.5	50	3	25	-
CA3450	RC	•	–	•	D	0.08	-	7	1.5	420	190	10000	15	-	-
3583	BB	–	•	•	3I	0.08	40	140	10	30	5	60	3	23	-
OP-50E	PM	•	–	•	D	0.07	5	18	0.5	3	25	20	0.03	0.3	-
3580	BB	–	•	•	3I	0.06	15	35	4.5	15	5	100	10	30	-
AMP-01E	PM	•	–	•	D	0.05	5	15	0.5	4.5	1	20	0.05	0.3	-
3581	BB	–	•	•	3I	0.03	32	75	4.5	20	5	60	3	25	-
3582/4	BB	–	•	•	3I	0.02	70	150	4.5	20/150	7	30/135	3	25	-

[a] see Table 4.1 notes. [b] 3 – TO-3; 220 – TO-220; PD – power DIP; D – DIP; I – isolated; C – metal can.
[c] current limit: T – thermal limit; E – external adjust. [m] min or max. [t] typical. [u] uncompensated.

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Type	I_b (max) @ 25°C (nA)	I_b (max) @ T_{max} (nA)	V_{sat} (V)	V_{sat} @ (A)	t_s (typ) (µs)	t_s (typ) to (%)	I_{lim}[c] (A)	Thermal limit	Comments
PA03	0.05	50	7	30	2	0.1	T	•	a mighty brute
PA04A	0.02	-	7.5	15	2.5	0.1	E	–	high voltage brute
OPA512	20	15	7	15	2	0.1	E	–	PA-12 similar
LM12	300	150	8	10			13	•	
OPA501	20	15	7	10			E	–	PA-51 similar
OPA512B	30	-	6	10	2	0.1	E	–	
OPA541B	0.05	40	4.5	5	2	0.1	E	–	monolithic JFET
1468	30	-	6	10	2	0.1	E	–	
PA19A	0.05	50	5	4	1.2	0.01	E	•	VMOS output, wideband, prec
OPA511	40	30	8	5	2	0.1	E	–	PA-01 similar
PA09A	0.02	20	8	2	0.3	0.1	4.5	•	fast
SG1173	500	300	6	2			3.5	•	
LM675	2µA		10	3.5			4	•	
LH0101	0.3	300	5	2	2	0.01	E	–	PA-02 similar
3572	0.1	100	5	2			E	•	PA-07 similar; 3571 to 1A
3573	40	30	5	2			E	–	PA-73 similar
LH0021	100	35	4	1	4	0.1	E	–	ext comp
MSK792	100	100	3.5	1			E	–	
1463	0.2	200	8	1	0.25	0.1	E	–	VMOS output
1461	0.1	100	9	0.5	0.4	0.1	E	–	VMOS output; ext comp
LH0061	100	35	5	0.5	0.8	0.1	E	–	ext comp
WA01A	10µA		5	0.4	0.02	0.1			
CLC203	20µA	20µA	4	0.2	15ns	0.2	E	–	fast settle, wideband, prec
1460	10µA	-	6	0.15	1	0.1	0.25	–	VMOS output; ext comp
3554B	0.05	50	5	0.1	0.2	0.01	0.15	–	fast
HA2542	35µA	-	-	-	0.1	0.1	-	–	decomp (G>2)
LH4101	0.5	500	-	-	0.3	0.1	-	–	
LH4104	0.6	25	5	0.1	0.5	0.01	-	–	LH4105 has V_{os}<0.5mV
1480	0.2	200	10	0.08	1.5	0.01	0.13	–	high voltage
1481	0.1	100	5	0.08	7.5	0.1	0.13	–	
CA3450	350	-	2	0.08	35ns	0.1	-	–	video amp
3583	0.02	20	10	0.08	12	0.1	0.1	•	high voltage
OP-50E	5	7[f]	2	0.03	30	0.01	0.06	•	low noise, precision
3580	0.05	50	5	0.06	12	0.1	0.1	•	
AMP-01E	3	10[f]	2	0.03	15	0.01	0.06	•	low noise, prec inst amp
3581	0.02	20	5	0.03	12	0.1	0.05	•	
3582/4	0.02	20	5	0.02	12	0.1	0.03	•	high voltage

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circuit the base is at the same voltage as the collector because of the virtual ground, but there is no base-current error. Q_1 and Q_2 should be a matched pair, thermally coupled (a matched monolithic pair like the LM394 or MAT-01 is ideal). This circuit will give accurate logarithmic output over seven decades of current or more (1nA to 10mA, approximately), providing that low-leakage transistors and a low-bias-current input op-amp are used. An op-amp like the 741 with 80nA of bias current is unsuitable, and a FET-input op-amp like the 411 is usually required to achieve the full seven decades of linearity. Furthermore, in order to give good performance at low input currents, the input op-amp must be accurately trimmed for zero offset voltage, since V_{in} may be as small as a few tens of microvolts at the lower limit of current. If possible, it is better to use a current input to this circuit, omitting R_1 altogether.

The capacitor C_1 is necessary to stabilize the feedback loop, since Q_1 contributes voltage gain inside the loop. Diode D_1 is necessary to prevent base-emitter breakdown (and destruction) of Q_1 in the event the input voltage goes negative, since Q_1 provides no feedback path for positive op-amp output voltage. Both these minor problems are avoided if Q_1 is wired as a diode, i.e., with its base tied to its collector.

Temperature compensation of gain

Q_2 compensates changes in Q_1's V_{BE} drop as the ambient temperature changes, but the changes in the slope of the curve of V_{BE} versus I_C are not compensated. In Section 2.10 we saw that the "60mV/decade" is proportional to absolute temperature. The output voltage of this circuit will look as shown in Figure 4.36. Compensation is perfect at an input current equal to I_0, Q_2's collector current. A change in temperature of 30°C causes a

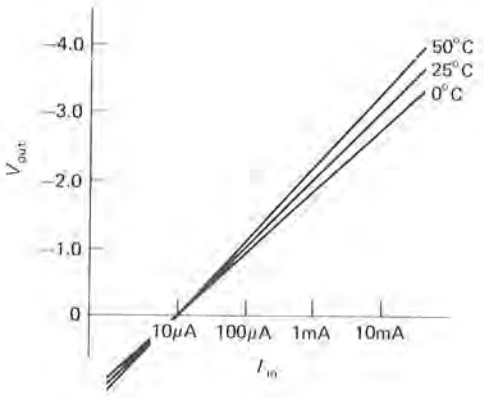


Figure 4.36

10% change in slope, with corresponding error in output voltage. The usual solution to this problem is to replace R_2 with a series combination of an ordinary resistor and a resistor of positive temperature coefficient. Knowing the temperature coefficient of the resistor (e.g., the TG 1/8 type manufactured by Texas Instruments has a coefficient of +0.67%/°C) allows you to calculate the value of the ordinary resistor to put in series in order to effect perfect compensation. For instance, with the 2.7k TG 1/8 type "sensistor" just mentioned, a 2.4k series resistor should be used.

There are several logarithmic converter modules available as complete integrated circuits. These offer very good performance, including internal temperature compensation. Some manufacturers are Analog Devices, Burr–Brown, Philbrick, Intersil, and National Semiconductor.

EXERCISE 4.7

Finish up the log converter circuit by (a) drawing the current source explicitly and (b) using a TG 1/8 resistor (+0.67%/°C tempco) for thermal slope compensation. Choose values so that $V_{out} = +1$ volt per decade, and provide an output offset control so that V_{out} can be set to zero for any desired input current (do this with an inverting amplifier offset circuit, not by adjusting I_0).

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4.15 Active peak detector

There are numerous applications in which it is necessary to determine the peak value of some input waveform. The simplest method is a diode and capacitor (Fig. 4.37). The highest point of the input waveform charges up C, which holds that value while the diode is back-biased.

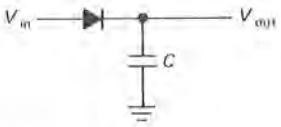


Figure 4.37

This method has some serious problems. The input impedance is variable and is very low during peaks of the input waveform. Also, the diode drop makes the circuit insensitive to peaks less than about 0.6 volt and inaccurate (by one diode drop) for larger peak voltages. Furthermore, since the diode drop depends on temperature and current, the circuit's inaccuracies depend on the ambient temperature and on the rate of change of output; recall that $I = C(dV/dt)$. An input emitter follower would improve the first problem only.

Figure 4.38 shows a better circuit, using feedback. By taking feedback from the voltage at the capacitor, the diode drop doesn't cause any problems. The sort of output waveform you might get is shown in Figure 4.39.

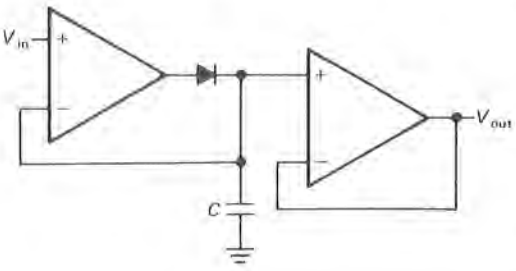


Figure 4.38. Op-amp peak detector.

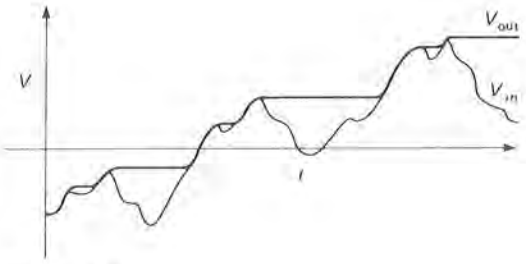


Figure 4.39

Op-amp limitations affect this circuit in three ways: (a) Finite op-amp slew rate causes a problem, even with relatively slow input waveforms. To understand this, note that the op-amp's output goes into negative saturation when the input is less positive than the output (try sketching the op-amp voltage on the graph; don't forget about diode forward drop). So the op-amp's output has to race back up to the output voltage (plus a diode drop) when the input waveform next exceeds the output. At slew rate S, this takes roughly $(V_0 - V_-)/S$, where V_- is the negative supply voltage and V_0 is the output voltage. (b) Input bias current causes a slow discharge (or charge, depending on the sign of the bias current) of the capacitor. This is sometimes called "droop," and it is best avoided by using op-amps with very low bias current. For the same reason, the diode must be a low-leakage type (e.g., the FJT1100, with less than 1pA reverse current at 20V, or a "FET diode" such as the PAD-1 from Siliconix or the ID101 from Intersil), and the following stage must also present high impedance (ideally it should also be a FET or FET-input op-amp). (c) The maximum op-amp output current limits the rate of change of voltage across the capacitor, i.e., the rate at which the output can follow a rising input. Thus, the choice of capacitor value is a compromise between low droop and high output slew rate.

For instance, a 1μF capacitor used in this circuit with the common 741 (which

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would be a poor choice because of its high bias current) would droop at $dV/dt = I_B/C = 0.08\text{V/s}$ and would follow input changes only up to $dV/dt = I_{\text{output}}/C = 0.02\text{V}/\mu s$. This maximum follow rate is much less than the op-amp's slew rate of $0.5\text{V}/\mu\text{s}$, being limited by the maximum output current of 20mA driving $1\mu\text{F}$. By decreasing C you could achieve greater output slewing rate at the expense of greater droop. A more realistic choice of components would be the popular LF355 FET-input op-amp as driver and output follower (30pA typical bias current, 20mA output current) and a value of $C = 0.01\mu\text{F}$. With this combination you would get a droop of only 0.006V/s and an overall circuit slew rate of $2\text{V}/\mu\text{s}$. For better performance, use a FET op-amp like the OPA111 or AD549, with input currents of 1pA or less. Capacitor leakage may then limit performance even if unusually good capacitors are used, e.g., polystyrene or polycarbonate (see Section 7.05).

□ *A circuit cure for diode leakage*

Quite often a clever circuit configuration can provide a solution to problems caused by nonideal behavior of circuit components. Such solutions are aesthetically pleasing as well as economical. At this point we yield to the temptation to take a closer look at such a high-performance design, rather than delaying until Chapter 7, where we treat such subjects under the heading of precision design.

Suppose we want the best possible performance in a peak detector, i.e., highest ratio of output slew rate to droop. If the lowest-input-current op-amps are used in a peak-detector circuit (some are available with bias currents as low as 0.01pA), the droop will be dominated by diode leakage; i.e., the best available diodes have higher leakage currents (see Table 1.1) than the op-amps' bias currents. Figure 4.40 shows a clever circuit solution. As before, the voltage on the capacitor follows a rising input waveform: IC_1 charges the capacitor through both diodes and is unaffected by IC_2's output. When the input drops below the peak value, IC_1 goes into negative saturation, but IC_2 holds point X at the capacitor voltage, eliminating leakage altogether in D_2. D_1's small leakage current flows through R_1, with negligible drop across the resistor. Of course, both op-amps must have low bias current. The OPA111B is a good choice here, with its combination of precision ($V_{os} = 250\mu\text{V}$, max) and low input current (1pA, max). This circuit is analogous to the so-called guard circuits used for high-impedance or small-signal measurements.

Note that the input op-amps in both peak-detector circuits spend most of their time in negative saturation, only popping up when the input level exceeds the peak voltage previously stored on the capacitor. However, as we saw in the active rectifier circuit (Section 4.10), the journey from negative saturation can take a while (e.g., $1\mu\text{s}$–$2\mu\text{s}$ for the LF411). This may restrict your choice to high-slew-rate op-amps.

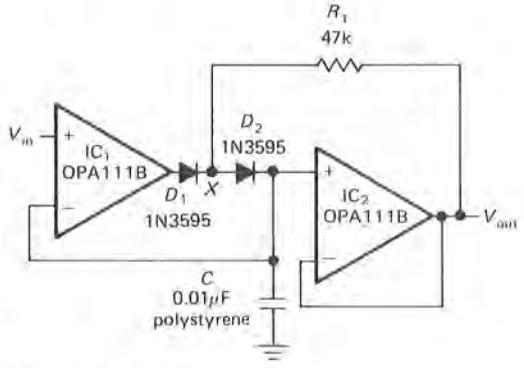


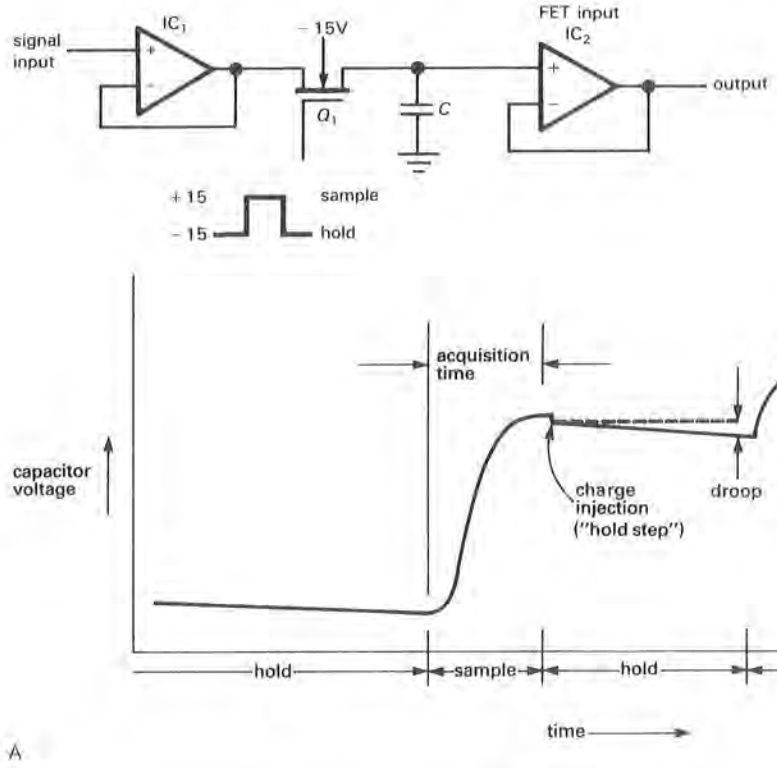
Figure 4.40

□ *Resetting a peak detector*

In practice it is usually desirable to reset the output of a peak detector in some way.

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One possibility is to put a resistor across the output so that the circuit's output decays with a time constant RC. In this way it holds only the most recent peak values. A better method is to put a transistor switch across C; a short pulse to the base then zeros the output. A FET switch is often used instead. For example, in Figure 4.38 you could connect an n-channel MOSFET across C; bringing the gate momentarily positive then zeros the capacitor voltage.



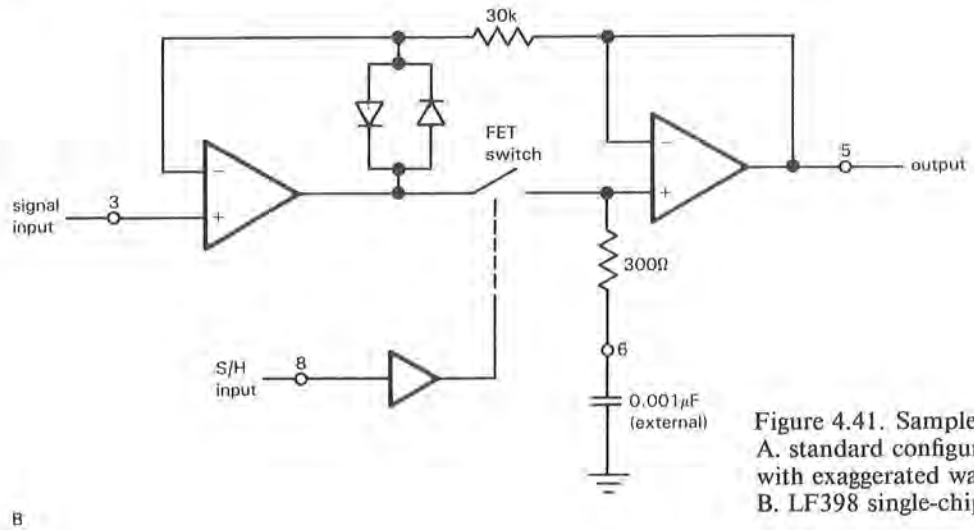


Figure 4.41. Sample-and-hold. A. standard configuration, with exaggerated waveform. B. LF398 single-chip S/H.

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4.16 Sample-and-hold

Closely related to the peak detector is the "sample-and-hold" (S/H) circuit (sometimes called "follow-and-hold"). These are especially popular in digital systems, where you want to convert one or more analog voltages to numbers so that a computer can digest them: The favorite method is to grab and hold the voltage(s), then do the digital conversion at your leisure. The basic ingredients of a S/H circuit are an op-amp and a FET switch; Figure 4.41A shows the idea. IC_1 is a follower to provide a low-impedance replica of the input. Q_1 passes the signal through during "sample" and disconnects it during "hold." Whatever signal was present when Q_1 was turned OFF is held on capacitor C. IC_2 is a high-input-impedance follower (FET inputs), so that capacitor current during "hold" is minimized. The value of C is a compromise: Leakage currents in Q_1 and the follower cause C's voltage to "droop" during the hold interval, according to $dV/dt = I_{\text{leakage}}/C$. Thus C should be large to minimize droop. But Q_1's ON resistance forms a low-pass filter in combination with C, so C should be small if high-speed signals are to be followed accurately. IC_1 must be able to supply C's charging current $I = CdV/dt$ and must have sufficient slew rate to follow the input signal. In practice, the slew rate of the whole circuit will usually be limited by IC_1's output current and Q_1's ON resistance.

EXERCISE 4.8

Suppose IC_1 can supply 10mA of output current, and $C = 0.01\mu F$. What is the maximum input slew rate the circuit can accurately follow? If Q_1 has 50 ohms ON resistance, what will be the output error for an input signal slewing at 0.1V/μs? If the combined leakage of Q_1 and

□ DIELECTRIC ABSORPTION

Capacitors are not perfect. The most commonly appreciated shortcomings are leakage (parallel resistance), series resistance and inductance, and nonzero temperature coefficient of capacitance. A more subtle problem is *dielectric absorption*, an effect that manifests itself clearly as follows: Take a large-value tantalum capacitor that is charged up to 10 volts or so, and rapidly discharge it by momentarily putting a 100 ohm resistor across it. Remove the resistor, and watch the capacitor's voltage on a high-impedance voltmeter. You will be amazed to see the capacitor *charge back up*, reaching perhaps a volt or so after a few seconds!

The origins of dielectric absorption (or dielectric *soakage*, dielectric *memory*) are not entirely understood, but the phenomenon is believed to be related to remnant polarization trapped on dielectric interfaces; mica, for example, with its layered structure, is particularly poor in this regard. From a circuit point of view, this extra polarization behaves like a set of additional series RCs across the capacitor (Fig. 4.42A), with time constants generally in the range of $\approx$100μs to several seconds. Dielectrics vary widely in their susceptibility to dielectric absorption; Figure 4.42B shows data for several high-quality dielectrics, plotted as voltage memory versus time after a 10 volt step of 100μs duration.

Dielectric absorption can cause significant errors in integrators and other analog circuits that rely on the ideal characteristics of capacitors. In the case of a sample/hold followed by precision analog-to-digital conversion, the effect can be devastating. In such situations the best approach is to choose your capacitors carefully (Teflon dielectric seems to be best), retaining a healthy skepticism until proven wrong. In extreme cases you may have to resort to tricks such as compensation networks that use carefully trimmed RCs to electrically cancel the capacitor's internal dielectric absorption. This approach is used in some high-quality sample/hold modules made by Hybrid Systems.

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IC_2 is 1nA, what is the droop rate during the "hold" state?

For both the sample/hold circuit and the peak detector, an op-amp drives a capacitive load. When designing such circuits, make sure you choose an op-amp that is stable at unity gain when loaded by the capacitor C. Some op-amps, (e.g., the LF355/6) are specifically designed to drive large (0.01μF) capacitive loads directly. Some other tricks you can use are discussed in Section 7.07 (see Fig. 7.17).

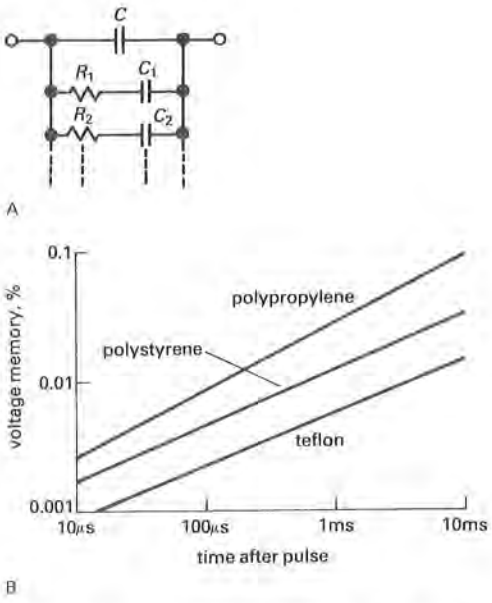


Figure 4.42. Dielectric absorption in capacitors. A. model B. measured properties for several dielectrics. (After Hybrid Systems HS9716 data sheet.)

You don't have to design S/H circuits from scratch, because there are nice monolithic ICs that contain all the parts you need except for the capacitor. National's LF398 is a popular part, containing the FET switch and two op-amps in an inexpensive ($2) 8-pin package. Figure 4.41B shows how to use it. Note how feedback closes the feedback loop around *both* op-amps. There are plenty of fancy S/H chips

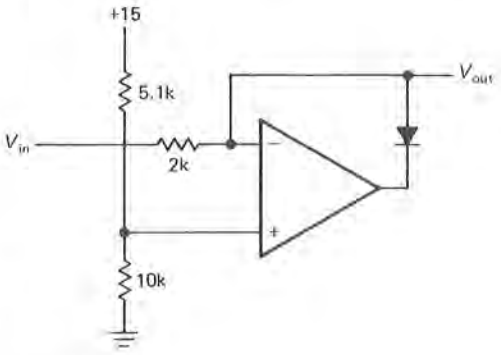


Figure 4.43

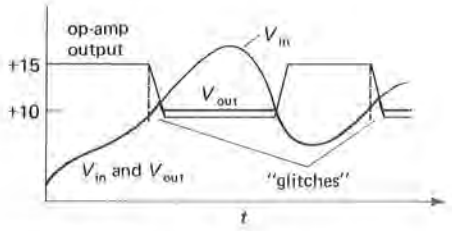


Figure 4.44

available, if you need better performance than the LF398 offers; for example, the AD585 from Analog Devices includes an internal capacitor and guarantees a maximum acquisition time of 3μs for 0.01% accuracy following a 10 volt step.

□ 4.17 Active clamp

Figure 4.43 shows a circuit that is an active version of the clamp function we discussed in Chapter 1. For the values shown, $V_{in} < +10$ volts puts the op-amp output at positive saturation, and $V_{out} = V_{in}$. When V_{in} exceeds +10 volts the diode closes the feedback loop, clamping the output at 10 volts. In this circuit, op-amp slew-rate limitations allow small glitches as the input reaches the clamp voltage from below (Fig. 4.44).

□ 4.18 Absolute-value circuit

The circuit shown in Figure 4.45 gives a positive output equal to the magnitude of

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the input signal; it is a full-wave rectifier. As usual, the use of op-amps and feedback eliminates the diode drops of a passive full-wave rectifier.

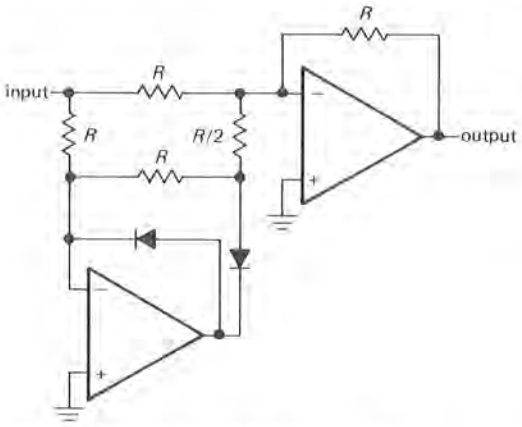


Figure 4.45. Active full-wave rectifier.

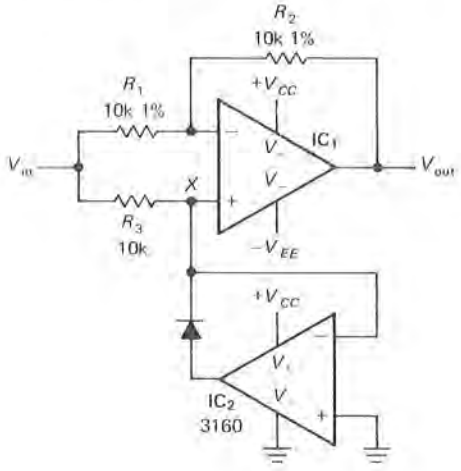


Figure 4.46

EXERCISE 4.9

Figure out how the circuit in Figure 4.45 works. Hint: Apply first a positive input voltage, and see what happens; then do negative.

Figure 4.46 shows another absolute-value circuit. It is readily understandable as a simple combination of an optional inverter (IC_1) and an active clamp (IC_2). For positive input levels the clamp is out of the circuit, with its output at negative saturation, making IC_1 a unity-gain inverter. Thus the output is equal to the absolute value of the input voltage. By running IC_2 from a single positive supply, you avoid problems of slew-rate limitations in the clamp, since its output moves over only one diode drop. Note that no great accuracy is required of R_3.

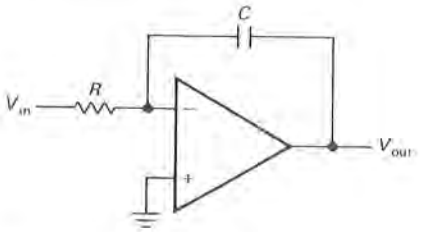


Figure 4.47. Integrator.

4.19 Integrators

Op-amps allow you to make nearly perfect integrators, without the restriction that $V_{out} \ll V_{in}$. Figure 4.47 shows how it's done. Input current V_{in}/R flows through C. Because the inverting input is a virtual ground, the output voltage is given by

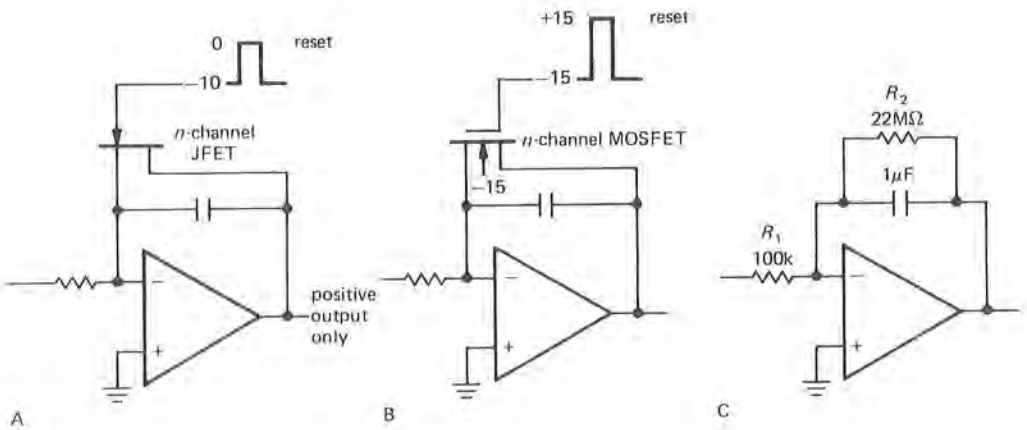
$$V_{in}/R = -C(dV_{out}/dt)$$

or

$$V_{out} = \frac{1}{RC}\int V_{in}\,dt + \text{constant}$$

The input can, of course, be a current, in which case R will be omitted. One problem with this circuit as drawn is that the output tends to wander off, even with the input grounded, due to op-amp offsets and bias current (there's no feedback at dc, which violates rule 3 in Section 4.08). This problem can be minimized by using a FET op-amp for low input current and offset, trimming the op-amp input offset voltage, and using large R and C values. In addition, in many applications the integrator is zeroed periodically by closing a

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4.48. Op-amp integrators with reset switches.

switch placed across the capacitor (usually a FET), so only the drift over short time scales matters. As an example, an inexpensive FET op-amp like the LF411 (25pA typical bias current) trimmed to a voltage offset of 0.2mV and used in an integrator with $R = 10\text{M}\Omega$ and $C = 10\mu\text{F}$ will produce an output drift of less than 0.003 volt in 1000 seconds.

If the residual drift of the integrator is still too large for a given application, it may be necessary to put a large resistor R_2 across C to provide dc feedback for stable biasing. The effect is to roll off the integrator action at very low frequencies, $f < 1/R_2C$. Figure 4.48 shows integrators with FET zeroing switch and with resistor bias stabilization. The feedback resistor may become rather large in this sort of application. Figure 4.49 shows a trick for producing the effect of a large feedback resistor using smaller values. In this case the feedback network behaves like a single 10MΩ resistor in the standard inverting amplifier circuit giving a voltage gain of −100. This technique has the advantage of using resistors of convenient values without the problems of stray capacitance, etc., that occur with very large resistor values. Note that this "T-network" trick may increase the effective input offset voltage, if used in a transresistance configuration (Section 4.09). For example, the circuit of Figure 4.49, driven from a high-impedance source (e.g., the current from a photodiode, with the input resistor omitted), has an output offset of 100 times V_{os}, whereas the same circuit with a 10MΩ feedback resistor has an output equal to V_{os} (assuming the offset due to input current is negligible).

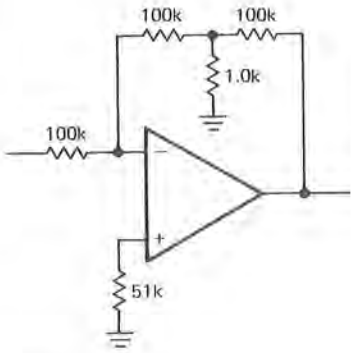


Figure 4.49

□ *A circuit cure for FET leakage*

In the integrator with a FET reset switch (Fig. 4.48), drain-source leakage sources a small current into the summing junction even when the FET is OFF. With an ultra-low-input-current op-amp and low-leakage

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capacitor, this can be the dominant error in the integrator. For example, the excellent AD549 JFET-input "electrometer" op-amp has a maximum input current of 0.06pA, and a high-quality 0.01μF metallized Teflon or polystyrene capacitor specifies leakage resistance as 10^7 *meg*ohms, minimum. Thus the integrator, exclusive of reset circuit, keeps stray currents at the summing junction below 1pA (for a worst-case 10V full-scale output), corresponding to an output dV/dt of less than 0.01mV/s. Compare this with the leakage contribution of a MOSFET such as the popular 2N4351 (enhancement mode), which specifies a maximum leakage current of 10nA at $V_{DS} = 10$V and $V_{GS} = 0$V! In other words, the FET contributes 10,000 times as much leakage as everything else combined.

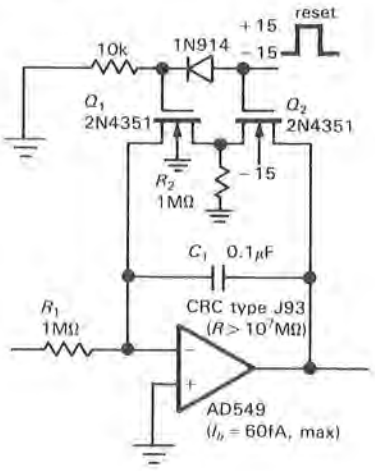


Figure 4.50

Figure 4.50 shows a clever circuit solution. Although both n-channel MOSFETs are switched together, Q_1 is switched with gate voltages of zero and +15 volts so that gate leakage (as well as drain-source leakage) is entirely eliminated during the OFF state (zero gate voltage). In the ON state the capacitor is discharged as before, but with twice R_{ON}. In the OFF state, Q_2's small leakage passes to ground through R_2 with negligible drop. There is no leakage current at the summing junction because Q_1's source, drain, and substrate are all at the same voltage. Compare this circuit with the zero-leakage peak-detector circuit of Figure 4.40.

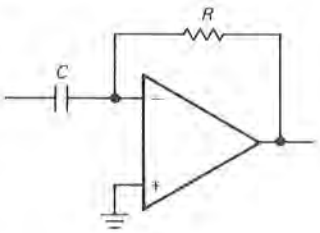


Figure 4.51

□ 4.20 Differentiators

Differentiators are similar to integrators, but with R and C reversed (Fig. 4.51). Since the inverting input is at ground, the rate of change of input voltage produces a current $I = C(dV_{in}/dt)$ and hence an output voltage

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Differentiators are bias-stable, but they generally have problems with noise and instabilities at high frequencies because of the op-amp's high gain and internal phase shifts. For this reason it is necessary to roll off the differentiator action at some maximum frequency. The usual method is shown in Figure 4.52. The choice of the rolloff components R_1 and C_2 depends on the noise level of the signal and the bandwidth of the op-amp. At high frequencies this circuit becomes an integrator, due to R_1 and C_2.

□ OP-AMP OPERATION WITH A SINGLE POWER SUPPLY

Op-amps don't *require* ±15 volt regulated supplies. They can be operated from split

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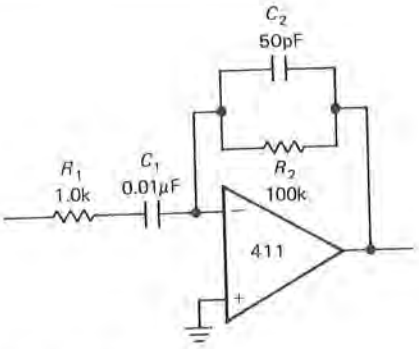


Figure 4.52

supplies of lower voltages, or from unsymmetrical supply voltages (e.g, +12 and −3), as long as the total supply voltage ($V_+ - V_-$) is within specifications (see Table 4.1). Unregulated supply voltages are often adequate because of the high "power-supply rejection ratio" you get from negative feedback (for the 411 it's 90dB typ). But there are many occasions when it would be nice to operate an op-amp from a single supply, say +12 volts. This can be done with ordinary op-amps by generating a "reference" voltage above ground, if you are careful about minimum supply voltages, output swing limitations, and maximum common-mode input range. With some of the more recent op-amps whose input and output ranges include the negative supply (i.e., ground, when run from a single positive supply), single-supply operation is attractive because of its simplicity. Keep in mind, though, that operation with symmetrical split supplies remains the usual technique for nearly all applications.

□ 4.21 Biasing single-supply ac amplifiers

For a general-purpose op-amp like the 411, the inputs and output can typically swing to within about 1.5 volts of either supply. With V_- connected to ground, you can't have either of the inputs or the output at ground. Instead, by generating a reference voltage (e.g., $0.5V_+$) you can bias the op-amp for successful operation (Fig. 4.53). This circuit is an audio amplifier with 40dB gain. $V_{ref} = 0.5V_+$ gives an output swing of about 17 volts pp before onset of clipping. Capacitive coupling is used at the input and output to block the dc level, which equals V_{ref}.

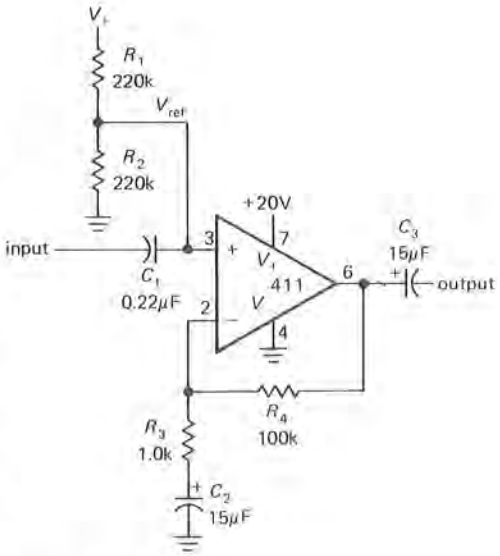


Figure 4.53

□ 4.22 Single-supply op-amps

There is a class of op-amps that permit simplified operation with a single positive supply, because they permit input voltages all the way down to the negative rail (normally tied to ground). They can be further divided into two types, according to the capability of the output stage: One type can swing all the way down to V_-, and the other type can swing all the way to *both* rails:

1. The LM324(quad)/LM358 (dual), LT1013, and TLC270 types. These have input common-mode ranges all the way down to 0.3 volt *below* V_-, and the output can swing down to V_-. Both inputs and output can go to within 1.5 volts of V_+. If

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instead you need an input range up to V_+, use something like an LM301/307, OP-41, or a 355; an example is illustrated in Section 6.24 in the discussion of constant-current supplies. In order to understand some of the subtleties of this sort of op-amp, it is helpful to look at the schematic (Fig. 4.54). It is a reasonably straightforward differential amplifier, with current mirror active load on the input stage and push-pull complementary output stage with current limiting. The special things to remember are these (calling V_- ground):

Inputs: The *pnp* input structure allows swings of 0.3 volt below ground; if that is exceeded by either input, weird things happen at the output (it may go negative, for instance).

Output: Q_{13} pulls the output down and can sink plenty of current, but it goes only to within a diode drop of ground. Outputs below that are provided by the 50μA current sink, which means you can't drive a load that sources more than 50μA and get closer than a diode drop above ground. Even for "nice" loads (an open circuit, say), the current source won't bring the output lower than a saturation voltage (0.1V) above ground. If you want the output to go clear down to ground, the load should sink a small current to ground; it could be a resistor to ground, for instance. Recent additions to the family of *pnp*-input single-supply op-amps include the precision LT1006 and LT1014 (single and quad, respectively) and the micropower OP-20 and OP-90 (both single), and LP324 (quad).

We will illustrate the use of these op-amps with some circuits, after mentioning the other kind of op-amp that lends itself well to single-supply operation.

2. The LM10 (bipolar) or CA5130/5160 (MOSFET) complementary-output-stage op-amps. When saturated, they look like a small resistance from the output to the supply (V_+ or V_-). Thus the output can swing all the way to either supply. In addition, the inputs can go 0.5 volt below V_-. Unlike the LM10, the CA5130

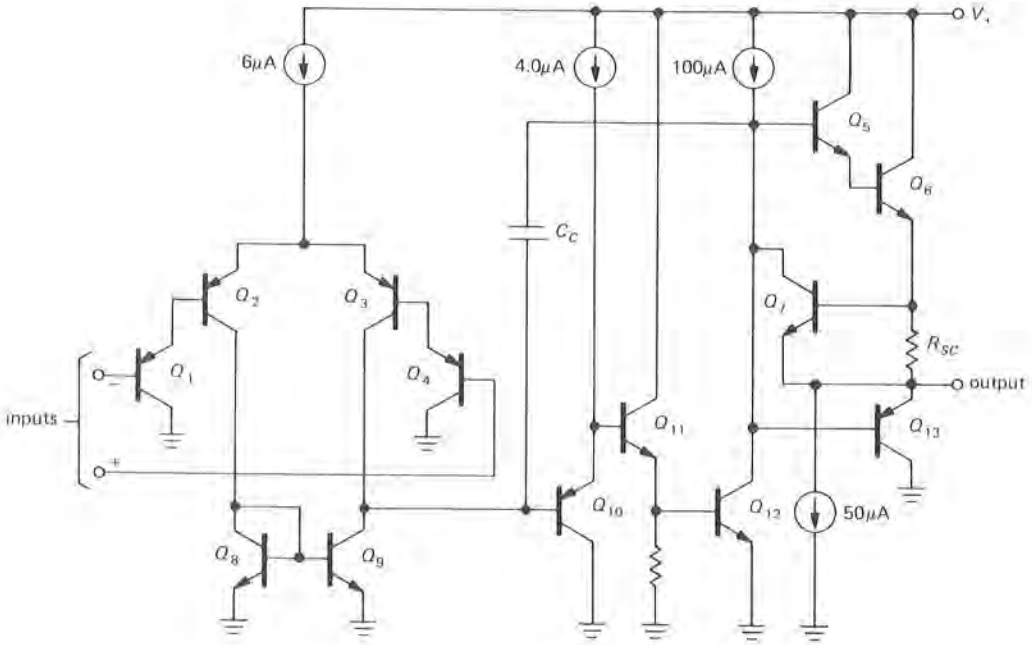


Figure 4.54. Schematic of the popular 324 and 358 op-amps. (National Semiconductor Corp.)

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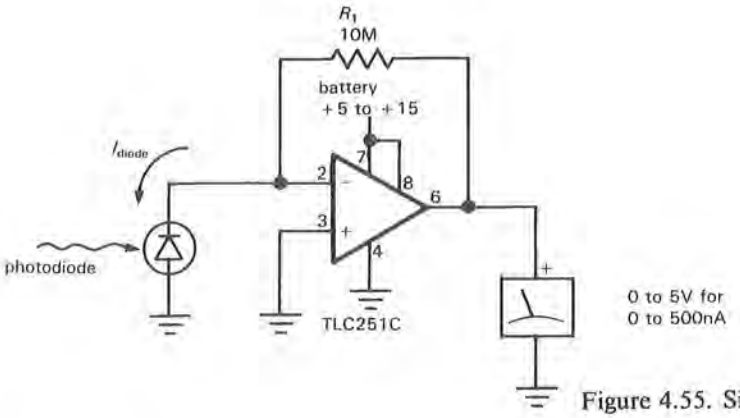


Figure 4.55. Single-supply photometer.

and 5160 are limited to 16 volts (max) total supply voltage and ±8 volts differential input voltage. Although most CMOS op-amps permit rail-to-rail output swings, watch out for some varieties that can only swing all the way to one rail; also note that the input common-mode range of most CMOS op-amps, like ordinary bipolar op-amps, includes at most one power-supply rail. For example, the popular TLC27*xx* series from TI has input and output capability to the negative rail only, whereas the LMC660 from National, along with the Intersil ICL76*xx* series and RCA's CMOS op-amps, has output swing to both rails (but input common-mode range only to the negative rail). Unique among op-amps are the CMOS ICL7612 and ALD1701/2, which claim both input and output operation to *both* rails.

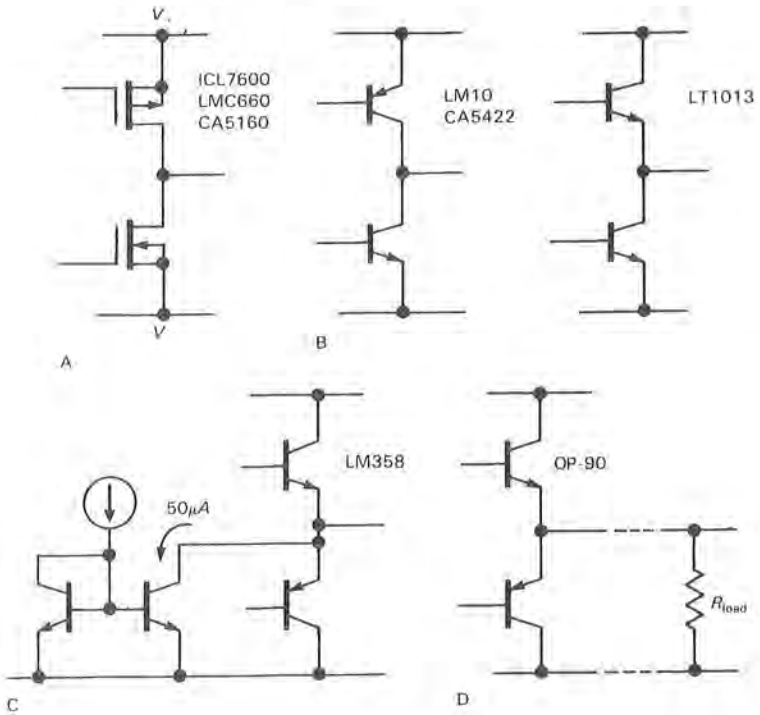


Figure 4.56. Output stages used in single-supply op-amps.

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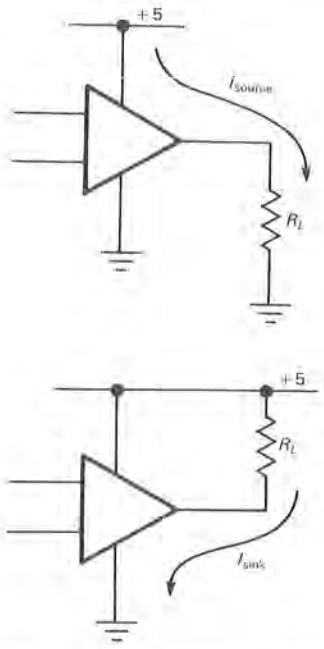


Figure 4.57. Connecting a load to a single-supply op-amp. All single-supply types (A–D) can swing all the way to ground while sourcing current. Some types (A and B) can swing nearly to ground while sinking moderate or substantial currents; type C can sink up to 50μA, and type D requires a load resistor returned to ground to operate near ground.

□ *Example: single-supply photometer*

Figure 4.55 shows a typical example of a circuit for which single-supply operation is convenient. We discussed a similar circuit earlier under the heading of current-to-voltage converters. Since a photocell circuit might well be used in a portable light-measuring instrument, and since the output is known to be positive only, this is a good candidate for a battery-operated single-supply circuit. R_1 sets the full- scale output at 5 volts for an input photocurrent of 0.5μA. No offset voltage trim is needed in this circuit, since the worst-case untrimmed offset of 10mV corresponds to a negligible 0.2% of full-scale meter indication. The TLC251 is an inexpensive micropower (10μA supply current) CMOS op-amp with input and output swings to the negative rail. Its low input current (1pA, typ, at room temperature) makes it good for low-current applications like this. Note that if you choose a bipolar op-amp for an application like this, better performance at low light levels results if the photodiode is connected as in the circuit shown in Figure 4.94J.

When using "single-supply" op-amps, watch out for misleading statements about output swing to the negative rail (ground). There are really four different kinds of output stages, all of which "swing down to ground," but they have very different properties (Fig. 4.56): (a) Op-amps with complementary MOS output transistors give true rail-to-rail swing; such a stage is

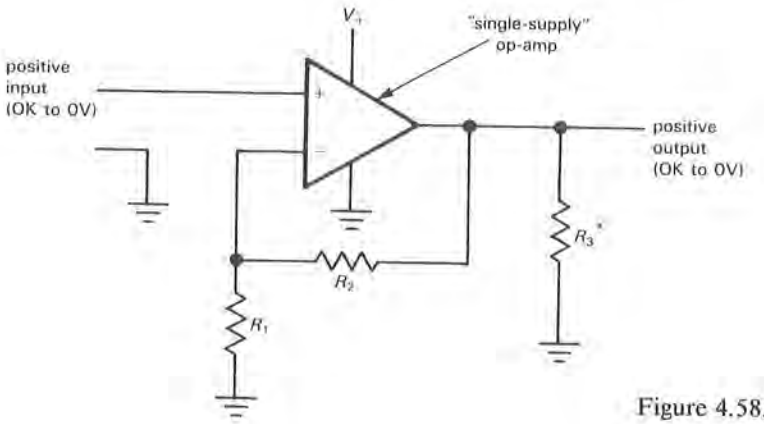


Figure 4.58. Single-supply dc amplifier.

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capable of pulling its output to ground, *even when sinking moderate current*. Some examples are the ICL76*xx*, the LMC660, and CA5160. (b) Op-amps with an *npn* common-emitter transistor to ground behave similarly, i.e., they can pull their output to ground even while sinking current. Examples are the LM10, CA5422, and LT1013/14. Both kinds of output stages can, of course, handle an open circuit or a load that *sinks* current to ground. (c) Some op-amps, notably the 358 and 324, use a *pnp* follower to ground (which can only pull down to within a diode drop of ground), in parallel with an *npn* current sink (with compliance clear to ground). In the 358, the internal current sink is set at 50μA. Such a circuit can swing clear down to ground as long as it doesn't have to sink more than 50μA from the load. If the load sources more current, the output only works to within a diode drop of ground. As before, this kind of output circuit is happy *sourcing* current to a load that is returned to ground (as in the photometer example earlier). (d) Finally, some single-supply op-amps (e.g., the OP-90) use a *pnp* follower to ground, without the parallel current sink. Such an output stage can swing to ground only if the load helps out by sinking current, i.e., by being returned to ground. If you want to use such an op-amp with a load that sources current, you have to add an external resistor to ground (Fig. 4.57).

A note of caution: Don't make the mistake of assuming that you can make any op-amp's output work down to the negative rail simply by providing an external current sink. In most cases the circuitry driving the output stage does not permit that. Look for explicit permission in the data sheet!

Example: single-supply dc amplifier

Figure 4.58 shows a typical single-supply noninverting amplifier to amplify an input signal of known positive polarity. The input, output, and positive supply are all referenced to ground, which is the negative supply voltage for the op-amp. The output "pulldown" resistor may be needed with what we called type-1 amplifiers to ensure output swing all the way to ground; the feedback network or the load itself could perform this function. An important point: Remember that the output cannot go negative; thus you cannot use this amplifier with, say, ac-coupled audio signals.

Single-supply op-amps are indispensable in battery-operated equipment. We'll have more to say about this in Chapter 14.

COMPARATORS AND SCHMITT TRIGGER

It is quite common to want to know which of two signals is larger, or to know when a given signal exceeds a predetermined value. For instance, the usual method of generating triangle waves is to supply positive or negative currents into a capacitor, reversing the polarity of the current when the amplitude reaches a preset peak value. Another example is a digital voltmeter. In order to convert a voltage to a number, the unknown voltage is applied to one input of a comparator, with a linear ramp (capacitor + current source) applied to the other. A digital counter counts cycles of an oscillator while the ramp is less than the unknown voltage and displays the result when equality of amplitudes is reached. The resultant count is proportional to the input voltage. This is called single-slope integration; in most sophisticated instruments a dual-slope integration is used (see Section 9.21).

4.23 Comparators

The simplest form of comparator is a high-gain differential amplifier, made either with transistors or with an op-amp (Fig. 4.59). The op-amp goes into positive or

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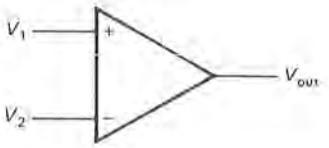


Figure 4.59

negative saturation according to the difference of the input voltages. Because the voltage gain typically exceeds 100,000, the inputs will have to be equal to within a fraction of a millivolt in order for the output not to be saturated. Although an ordinary op-amp can be used as a comparator (and frequently is), there are special integrated circuits intended for use as comparators. Some examples are the LM306, LM311, LM393, NE527, and TLC372. These chips are designed for very fast response and aren't even in the same league as op-amps. For example, the high-speed NE521 slews at several thousand volts per microsecond. With comparators, the term "slew rate" isn't usually used; you talk instead about "propagation delay versus input overdrive."

Comparators generally have more flexible output circuits than op-amps. Whereas an ordinary op-amp uses a push-pull output stage to swing between the supply voltages (±13V, say, for a 411 running from ±15V supplies), a comparator chip usually has an "open-collector" output with grounded emitter. By supplying an external "pullup" resistor (that's accepted terminology, believe it or not) connected to a voltage of your choice, you can have an output swing from +5 volts to ground, say. You will see later that logic circuits have well-defined voltages they like to operate between; the preceding example would be ideal for driving a TTL circuit, a popular type of digital logic. Figure 4.60 shows the circuit. The output switches from +5 volts to ground when the input signal goes negative. This use of a comparator is really an example of analog-to-digital conversion.

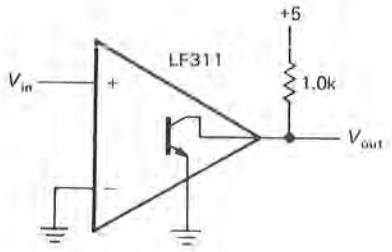


Figure 4.60

This is the first example we have presented of an *open-collector* output; this is a common configuration in logic circuits, as you will see throughout Chapters 8–11. If you like, you can think of the external pullup resistor as completing the comparator's internal circuit by providing a collector load resistor for an *npn* output transistor. Since the output transistor operates as a saturated switch, the resistor value is not at all critical, with values typically between a few hundred ohms and a few thousand ohms; small values yield improved switching speed and noise immunity at the expense of increased power dissipation. Incidentally, in spite of their superficial resemblance to op-amps, comparators are never used with negative feedback because they would not be stable (see Sections 4.32–4.34). However, some *positive* feedback is often used, as you will see in the next section.

Comments on comparators

Some points to remember: (a) Because there is no negative feedback, golden rule I is not obeyed. The inputs are not at the same voltage. (b) The absence of negative feedback means that the (differential) input impedance isn't bootstrapped to the high values characteristic of op-amp circuits. As a result, the input signal sees a changing load and changing (small) input current as the comparator switches; if the driving impedance is too high,

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strange things may happen. (c) Some comparators permit only limited differential input swings, as little as ±5 volts in some cases. Check the specs! See Table 9.3 and the discussion in Section 9.07 for the properties of some popular comparators.

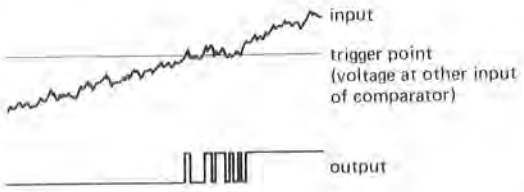


Figure 4.61

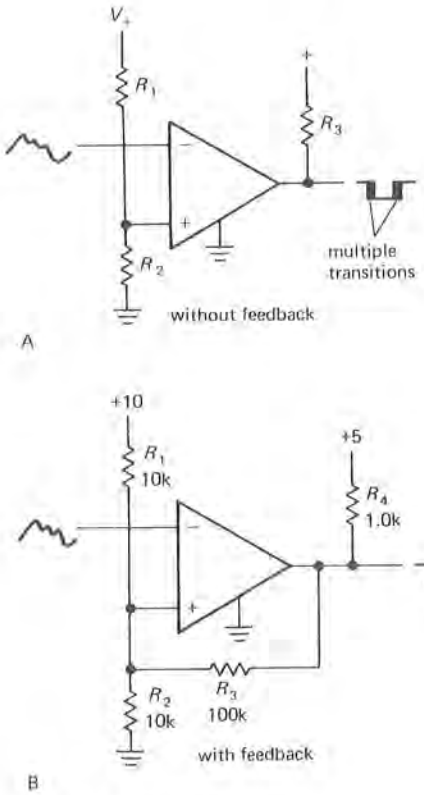


Figure 4.62

4.24 Schmitt trigger

The simple comparator circuit in Figure 4.60 has two disadvantages. For a very slowly varying input, the output swing can be rather slow. Worse still, if the input is noisy, the output may make several transitions as the input passes through the trigger point (Fig. 4.61). Both these problems can be remedied by the use of *positive* feedback (Fig. 4.62). The effect of R_3 is to make the circuit have two thresholds, depending on the output state. In the example shown, the threshold when the output is at ground (input high) is 4.76 volts, whereas the threshold with the output at +5 volts is 5.0 volts. A noisy input is less likely to produce multiple triggering (Fig. 4.63). Furthermore, the positive feedback ensures a rapid output transition, regardless of the speed of the input waveform. (A small "speedup" capacitor of 10–100pF is often connected across R_3 to enhance switching speed still further.) This configuration is known as a Schmitt trigger. (If an op-amp were used, the pullup would be omitted.)

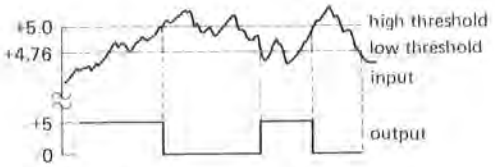


Figure 4.63

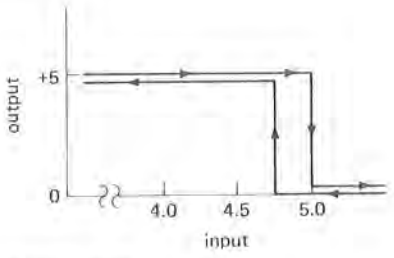


Figure 4.64

The output depends both on the input voltage and on its recent history, an effect called *hysteresis*. This can be illustrated with a diagram of output versus input, as in Figure 4.64. The design procedure

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is easy for Schmitt triggers that have a small amount of hysteresis. Use the circuit of Figure 4.62B. First choose a resistive divider (R_1, R_2) to put the threshold at approximately the right voltage; if you want the threshold near ground, just use a single resistor from noninverting input to ground. Next, choose the (positive) feedback resistor R_3 to produce the required hysteresis, noting that the hysteresis equals the output swing, attenuated by a resistive divider formed by R_3 and $R_1 \| R_2$. Finally, choose an output pullup resistor R_4 small enough to ensure nearly full supply swing, taking account of the loading by R_3. For the case where you want thresholds symmetrical about ground, connect an offsetting resistor of appropriate value from the noninverting input to the negative supply. You may wish to scale all resistor values in order to keep the output current and impedance levels within a reasonable range.

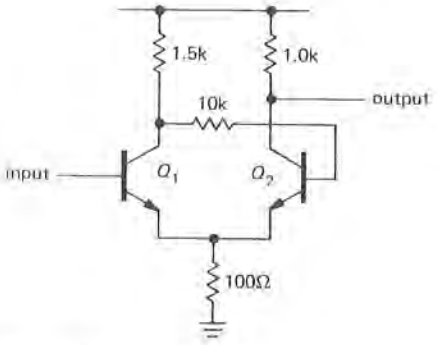


Figure 4.65

Discrete-transistor Schmitt trigger

A Schmitt trigger can also be made simply with transistors (Fig. 4.65). Q_1 and Q_2 share an emitter resistor. It is essential that Q_1's collector resistor be larger than Q_2's. In that way the threshold to turn on Q_1, which is one diode drop above the emitter voltage, rises when Q_1 is turned off, since the emitter current is higher with Q_2 conducting. This produces hysteresis in the trigger threshold, just as in the preceding integrated circuit Schmitt trigger.

EXERCISE 4.10

Design a Schmitt trigger using a 311 comparator (open-collector output) with thresholds at +1.0 volt and +1.5 volts. Use a 1.0k pullup resistor to +5 volts, and assume that the 311 is powered from ±15 volt supplies.

FEEDBACK WITH FINITE-GAIN AMPLIFIERS

We mentioned in Section 4.12 that the finite open-loop gain of an op-amp limits its performance in a feedback circuit. Specifically, the closed-loop gain can never exceed the open-loop gain, and as the open-loop gain approaches the closed-loop gain, the amplifier begins to depart from the ideal behavior we have come to expect. In this section we will quantify these statements so that you will be able to predict the performance of a feedback amplifier constructed with real (less than ideal) components. This is important also for feedback amplifiers constructed entirely with discrete components (transistors), where the open-loop gain is usually much less than with op-amps. In these cases the output impedance, for instance, will not be zero. Nonetheless, with a good understanding of feedback principles you will be able to achieve the performance required in any given circuit.

4.25 Gain equation

Let's begin by considering an amplifier of finite voltage gain, connected with feedback to form a noninverting amplifier (Fig. 4.66). The amplifier has open-loop voltage gain A, and the feedback network subtracts a fraction B of the output voltage from the input. (Later we will generalize

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things so that inputs and outputs can be currents or voltages.) The input to the gain block is then $V_{in} - BV_{out}$. But the output is just the input times A:

$$A(V_{in} - BV_{out}) = V_{out}$$

In other words,

$$V_{out} = \frac{A}{1 + AB} V_{in}$$

and the closed-loop voltage gain, V_{out}/V_{in}, is just

$$G = \frac{A}{1 + AB}$$

Some terminology: The standard designations for these quantities are as follows: G = closed-loop gain, A = open-loop gain, AB = loop gain, $1 + AB$ = return difference, or desensitivity. The feedback network is sometimes called the beta network (no relation to transistor beta, h_{fe}).

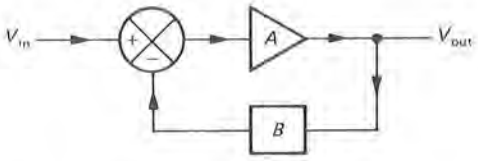


Figure 4.66

4.26 Effects of feedback on amplifier circuits

Let's look at the important effects of feedback. The most significant are predictability of gain (and reduction of distortion), changed input impedance, and changed output impedance.

Predictability of gain

The voltage gain is $A/(1 + AB)$. In the limit of infinite open-loop gain A, $G = 1/B$. We saw this result in the noninverting amplifier configuration, where a voltage divider on the output provided the signal to the inverting input (Fig. 4.69). The closed-loop voltage gain was just the inverse of the division ratio of the voltage divider. For finite gain A, feedback still acts to reduce the effects of variations of A (with frequency, temperature, amplitude, etc.). For instance, suppose A depends on frequency as in Figure 4.67. This

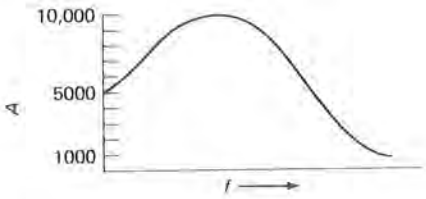


Figure 4.67

will surely satisfy anyone's definition of a poor amplifier (the gain varies over a factor of 10 with frequency). Now imagine we introduce feedback, with $B = 0.1$ (a simple voltage divider will do). The closed-loop voltage gain now varies from 1000/[1 +(1000×0.1)], or 9.90, to 10,000/[1 + (10,000×0.1)], or 9.99, a variation of just 1% over the same range of frequency! To put it in audio terms, the original amplifier is flat to ±10dB, whereas the feedback amplifier is flat to ±0.04dB. We can now recover the original gain of 1000 with nearly this linearity by just cascading three such stages. It was for just this reason (namely, the need for extremely flat telephone repeater amplifiers) that negative feedback was invented. As the inventor, Harold Black, described it in his first open publication on the invention (*Electrical Engineering*, 53:114, 1934), "by building an amplifier whose gain is made deliberately, say 40 decibels higher than necessary (10,000-fold excess on energy basis) and then feeding the output back to the input in such a way as to throw away the excess gain, it has been found possible to effect extraordinary improvement in constancy of amplification and freedom from nonlinearity."

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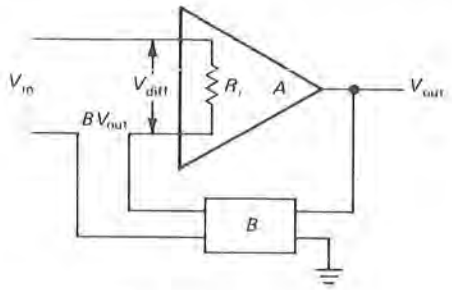


Figure 4.68

It is easy to show, by taking the partial derivative of G with respect to A ($\partial G/\partial A$), that relative variations in the open-loop gain are reduced by the desensitivity:

$$\frac{\Delta G}{G} = \frac{1}{1+AB}\frac{\Delta A}{A}$$

Thus, for good performance the loop gain AB should be much larger than 1. That's equivalent to saying that the open-loop gain should be much larger than the closed-loop gain.

A very important consequence of this is that nonlinearities, which are simply gain variations that depend on signal level, are reduced in exactly the same way.

Input impedance

Feedback can be arranged to subtract a voltage or a current from the input (these are sometimes called *series feedback* and *shunt feedback*, respectively). The noninverting op-amp configuration, for instance, subtracts a sample of the output voltage from the differential voltage appearing at the input, whereas in the inverting configuration a current is subtracted from the input. The effects on input impedance are opposite in the two cases: Voltage feedback multiplies the open-loop input impedance by $1 + AB$, whereas current feedback reduces it by the same factor. In the limit of infinite loop gain the input impedance (at the amplifier's input terminal) goes to infinity or zero, respectively. This is easy to understand, since voltage feedback tends to subtract signal from the input, resulting in a smaller change (by the factor AB) across the amplifier's input resistance; it's a form of bootstrapping. Current feedback reduces the input signal by bucking it with an equal current.

Let's see explicitly how the effective input impedance is changed by feedback. We will illustrate the case of voltage feedback only, since the derivations are similar for the two cases. We begin with an op-amp model with (finite) input resistance as shown in Figure 4.68. An input V_{in} is reduced by BV_{out}, putting a voltage $V_{diff} = V_{in} - BV_{out}$ across the inputs of the amplifier. The input current is therefore

$$I_{in} = \frac{V_{in} - BV_{out}}{R_i} = \frac{V_{in}\left(1 - B\frac{A}{1+AB}\right)}{R_i} = \frac{V_{in}}{(1+AB)R_i}$$

giving an effective input resistance

$$R_i' = V_{in}/I_{in} = (1+AB)R_i$$

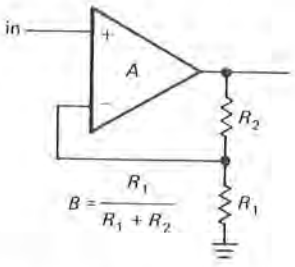


Figure 4.69

The classic op-amp noninverting amplifier is exactly this feedback configuration, as shown in Figure 4.69. In this circuit, $B = R_1/(R_1 + R_2)$, giving the usual voltage-gain expression $G_v = 1 + R_2/R_1$ and an infinite input impedance for the ideal case of infinite open-loop voltage gain

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A. For finite loop gain, the equations as previously derived apply.

The op-amp *inverting* amplifier circuit is different from the noninverting circuit and has to be analyzed separately. It's best to think of it as a combination of an input resistor driving a shunt feedback stage (Fig. 4.70). The shunt stage alone has its input at the "summing junction" (the inverting input of the amplifier), where the currents from feedback and input signals are combined (this amplifier connection is really a "transresistance" configuration; it converts a current input to a voltage output). Feedback reduces the impedance looking into the summing junction, R_2, by a factor of $1 + A$ (see if you can prove this). In cases of very high loop gain (e.g, an op-amp) the input impedance is reduced to a fraction of an ohm, a good characteristic for a current-input amplifier. Some good examples are the photometer amplifier in Section 4.22 and the logarithmic converter in Section 4.14.

The classic op-amp inverting amplifier connection is a combination of a shunt feedback transresistance amplifier and a series input resistor, as in the figure. As a result, the input impedance equals the sum of R_1 and the impedance looking into the summing junction. For high loop gain, R_{in} approximately equals R_1.

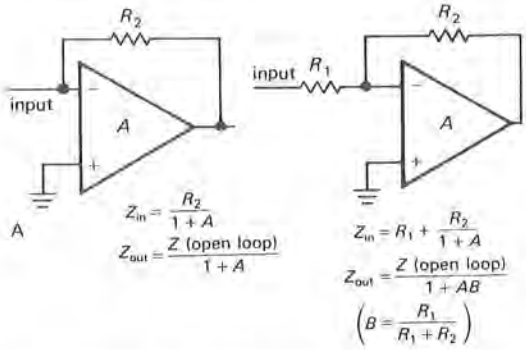


Figure 4.70. Input and output impedances for (A) transresistance amplifier and (B) inverting amplifier.

It is a straightforward exercise to derive an expression for the closed-loop voltage gain of the inverting amplifier with finite loop gain. The answer is

$$G = -A(1 - B)/(1 + AB)$$

where B is defined as before, $B = R_1/(R_1 + R_2)$. In the limit of large open-loop gain A, $G = -1/B + 1$ (i.e., $G = -R_2/R_1$).

EXERCISE 4.11

Derive the foregoing expressions for input impedance and gain of the inverting amplifier.

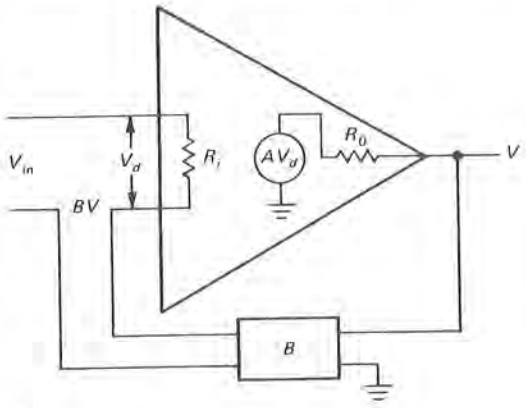


Figure 4.71

Output impedance

Again, feedback can extract a sample of the output voltage or the output current. In the first case the open-loop output impedance will be reduced by the factor $1 + AB$, whereas in the second case it will be increased by the same factor. We will illustrate this effect for the case of voltage sampling. We begin with the model shown in Figure 4.71. This time we have shown the output impedance explicitly. The calculation is simplified by a trick: Short the input, and apply a voltage V to the output; by calculating the output current I, we get the output impedance $R_0' = V/I$. Voltage V at the output

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puts a voltage $-BV$ across the amplifier's input, producing a voltage $-ABV$ in the amplifier's internal generator. The output current is therefore

$$I = \frac{V-(-ABV)}{R_0} = \frac{V(1+AB)}{R_0}$$

giving an effective output impedance

$$R_0' = V/I = R_0/(1+AB)$$

If feedback is connected instead to sample the output current, the expression becomes

$$R_0' = R_0(1+AB)$$

It is possible to have multiple feedback paths, sampling both voltage and current. In the general case the output impedance is given by Blackman's impedance relation

$$R_0' = R_0\frac{1+(AB)_{SC}}{1+(AB)_{OC}}$$

where $(AB)_{SC}$ is the loop gain with the output shorted to ground and $(AB)_{OC}$ is the loop gain with no load attached. Thus, feedback can be used to generate a desired output impedance. This equation reduces to the previous results for the usual situation in which feedback is derived from either the output voltage or the output current.

□ *Loading by the feedback network*

In feedback computations, you usually assume that the beta network doesn't load the amplifier's output. If it does, that must be taken into account in computing the open-loop gain. Likewise, if the connection of the beta network at the amplifier's input affects the open-loop gain (feedback removed, but network still connected), you must use the modified open-loop gain. Finally, the preceding expressions assume that the beta network is unidirectional, i.e., it does not couple signal from the input to the output.

□ 4.27 Two examples of transistor amplifiers with feedback

Figure 4.72 shows a transistor amplifier with negative feedback.

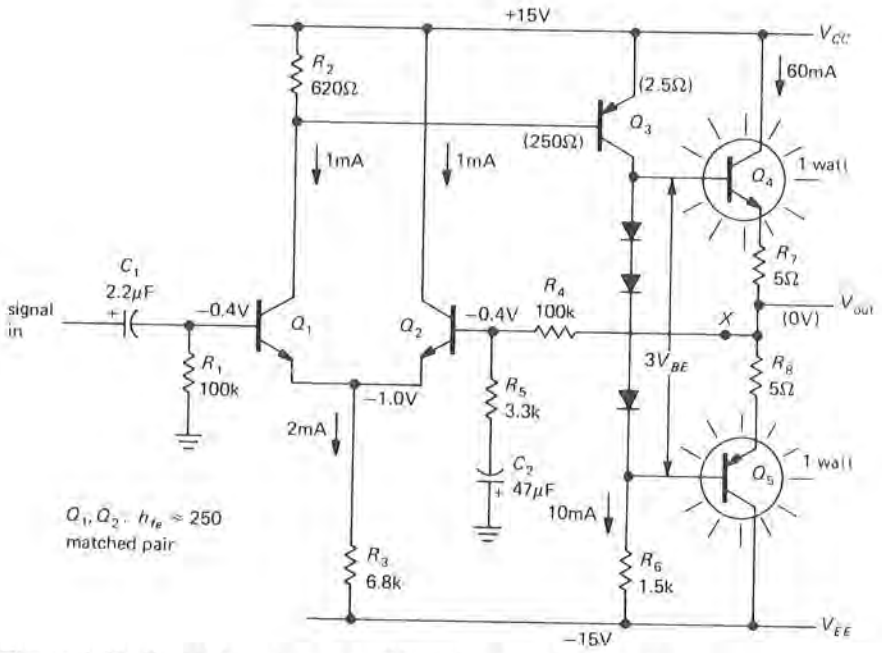


Figure 4.72. Transistor power amplifier with negative feedback.

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□ ***Circuit description***

It may look complicated, but it is extremely straightforward in design and is relatively easy to analyze. Q_1 and Q_2 form a differential pair, with common-emitter amplifier Q_3 amplifying its output. R_6 is Q_3's collector load resistor, and push-pull pair Q_4 and Q_5 form the output emitter follower. The output voltage is sampled by the feedback network consisting of voltage divider R_4 and R_5, with C_2 included to reduce the gain to unity at dc for stable biasing. R_3 sets the quiescent current in the differential pair, and since overall feedback guarantees that the quiescent output voltage is at ground, Q_3's quiescent current is easily seen to be 10mA (V_{EE} across R_6, approximately). As we have discussed earlier (Section 2.15), the diodes bias the push-pull pair into conduction, leaving one diode drop across the series pair R_7 and R_8, i.e., 60mA quiescent current. That's class AB operation, good for minimizing crossover distortion, at the cost of 1 watt standby dissipation in each output transistor.

From the point of view of our earlier circuits, the only unusual feature is Q_1's quiescent collector voltage, one diode drop below V_{CC}. That is where it must sit in order to hold Q_3 in conduction, and the feedback path ensures that it will. (For instance, if Q_1 were to pull its collector closer to ground, Q_3 would conduct heavily, raising the output voltage, which in turn would force Q_2 to conduct more heavily, reducing Q_1's collector current and hence restoring the status quo.) R_2 was chosen to give a diode drop at Q_1's quiescent current in order to keep the collector currents in the differential pair approximately equal at the quiescent point. In this transistor circuit the input bias current is not negligible (4μA), resulting in a 0.4 volt drop across the 100k input resistors. In transistor amplifier circuits like this, in which the input currents are considerably larger than in op-amps, it is particularly important to make sure that the dc resistances seen from the inputs are equal, as shown (a Darlington input stage would probably be better here).

□ ***Analysis***

Let's analyze this circuit in detail, determining the gain, input and output impedances, and distortion. To illustrate the utility of feedback, we will find these parameters for both the open-loop and closed-loop situations (recognizing that biasing would be hopeless in the open-loop case). To get a feeling for the linearizing effect of the feedback, the gain will be calculated at +10 volts and −10 volts output, as well as the quiescent point (zero volts).

□ *Open loop.* Input impedance: We cut the feedback at point X and ground the right side of R_4. The input signal sees 100k in parallel with the impedance looking into the base. The latter is h_{fe} times twice the intrinsic emitter resistance plus the impedance seen at Q_2's emitter due to the feedback network at Q_2's base. For $h_{fe} \approx 250$, $Z_{\text{in}} \approx 250\times[(2\times25)+(3.3\text{k}/250)]$; i.e., $Z_{\text{in}} \approx 16\text{k}$.

Output impedance: Since the impedance looking back into Q_3's collector is high, the output transistors are driven by a 1.5k source (R_6). The output impedance is about 15 ohms ($h_{fe} \approx 100$) plus the 5 ohm emitter resistance, or 20 ohms. The intrinsic emitter resistance of 0.4 ohm is negligible.

Gain: The differential input stage sees a load of R_2 paralleled by Q_3's base resistance. Since Q_3 is running 10mA quiescent current, its intrinsic emitter resistance is 2.5 ohms, giving a base impedance of about 250 ohms (again, $h_{fe} \approx 100$). The differential pair thus has a gain of

$$\frac{250\|620}{2\times25\Omega} \quad \text{or} \quad 3.5$$

The second stage, Q_3, has a voltage gain of 1.5k/2.5ohms, or 600. The overall voltage

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gain at the quiescent point is 3.5 × 600, or 2100. Since Q_3's gain depends on its collector current, there is substantial change of gain with signal swing, i.e., nonlinearity. The gain is tabulated in the following section for three values of output voltage.

□ *Closed loop.* Input impedance: This circuit uses series feedback, so the input impedance is raised by (1 + loop gain). The feedback network is a voltage divider with $B = 1/30$ at signal frequencies, so the loop gain AB is 70. The input impedance is therefore 70 × 16k, still paralleled by the 100k bias resistor, i.e., about 92k. The bias resistor now dominates the input impedance.

Output impedance: Since the output *voltage* is sampled, the output impedance is reduced by (1 + loop gain). The output impedance is therefore 0.3 ohm. Note that this is a small-signal impedance and does not mean that a 1 ohm load could be driven to nearly full swing, for instance. The 5 ohm emitter resistors in the output stage limit the large signal swing. For instance, a 4 ohm load could be driven only to 10 volts pp, approximately.

Gain: The gain is $A/(1+AB)$. At the quiescent point, that equals 30.84, using the exact value for B. In order to illustrate the gain stability achieved with negative feedback, the overall voltage gain of the circuit with and without feedback is tabulated at three values of output level at the end of this paragraph. It should be obvious that negative feedback has brought about considerable improvement in the amplifier's characteristics, although in fairness it should be pointed out that the amplifier could have been designed for better open-loop performance, e.g., by using a current source for Q_3's collector load and degenerating its emitter, by using a current source for the differential-pair emitter circuit, etc. Even so, feedback would still make a large improvement.

	Open loop			*Closed loop*		
V_{out}	−10	0	+10	−10	0	+10
Z_{in}	16k	16k	16k	92k	92k	92k
Z_{out}	20Ω	20Ω	20Ω	0.3Ω	0.3Ω	0.3Ω
Gain	1360	2100	2400	30.60	30.84	30.90

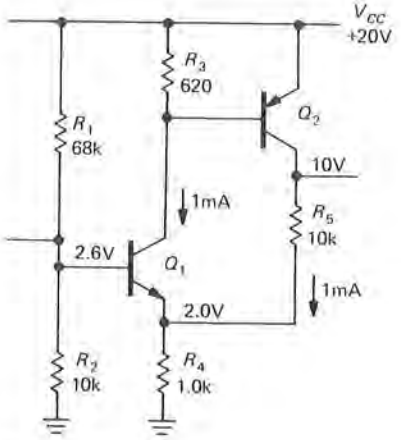


Figure 4.73

□ ***Series feedback pair***

Figure 4.73 shows another transistor amplifier with feedback. Thinking of Q_1 as an amplifier of its base-emitter voltage drop (thinking in the Ebers-Moll sense), the feedback samples the output voltage and subtracts a fraction of it from the input signal. This circuit is a bit tricky because Q_2's collector resistor doubles as the feedback network. Applying the techniques we used earlier, you should be able to show that G(open loop) ≈ 200, loop gain ≈ 20, Z_{out}(open loop) ≈10k, Z_{out}(closed loop) ≈ 500 ohms, and G(closed loop) ≈ 9.5.

SOME TYPICAL OP-AMP CIRCUITS

4.28 General-purpose lab amplifier

Figure 4.74 shows a dc-coupled "decade amplifier" with settable gain, bandwidth, and wide-range dc output offset. IC_1 is a FET-input op-amp with noninverting gain from unity (0dB) to ×100 (40dB) in

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accurately calibrated 10dB steps; a vernier is provided for variable gain. IC_2 is an inverting amplifier; it allows offsetting the output over a range of ±10 volts, accurately calibrated via R_{14}, by injecting current into the summing junction. $C_2 - C_4$ set the high-frequency rolloff, since it is often a nuisance to have excessive bandwidth (and noise). IC_5 is a power booster for driving low-impedance loads or cables; it can provide ±150mA output current.

Some interesting details: A 10MΩ input resistor is small enough, since the bias current of the 411 is 25pA (0.3mV error with open input). R_2, in combination with D_1 and D_2, limits the input voltage at the op-amp to the range V_- to $V_+ + 0.7$. D_3 is used to generate a clamp voltage at $V_- + 0.7$, since the input common mode range extends only to V_- (exceeding V_- causes the output to reverse phase). With the protection components shown, the input can go to ±150 volts without damage.

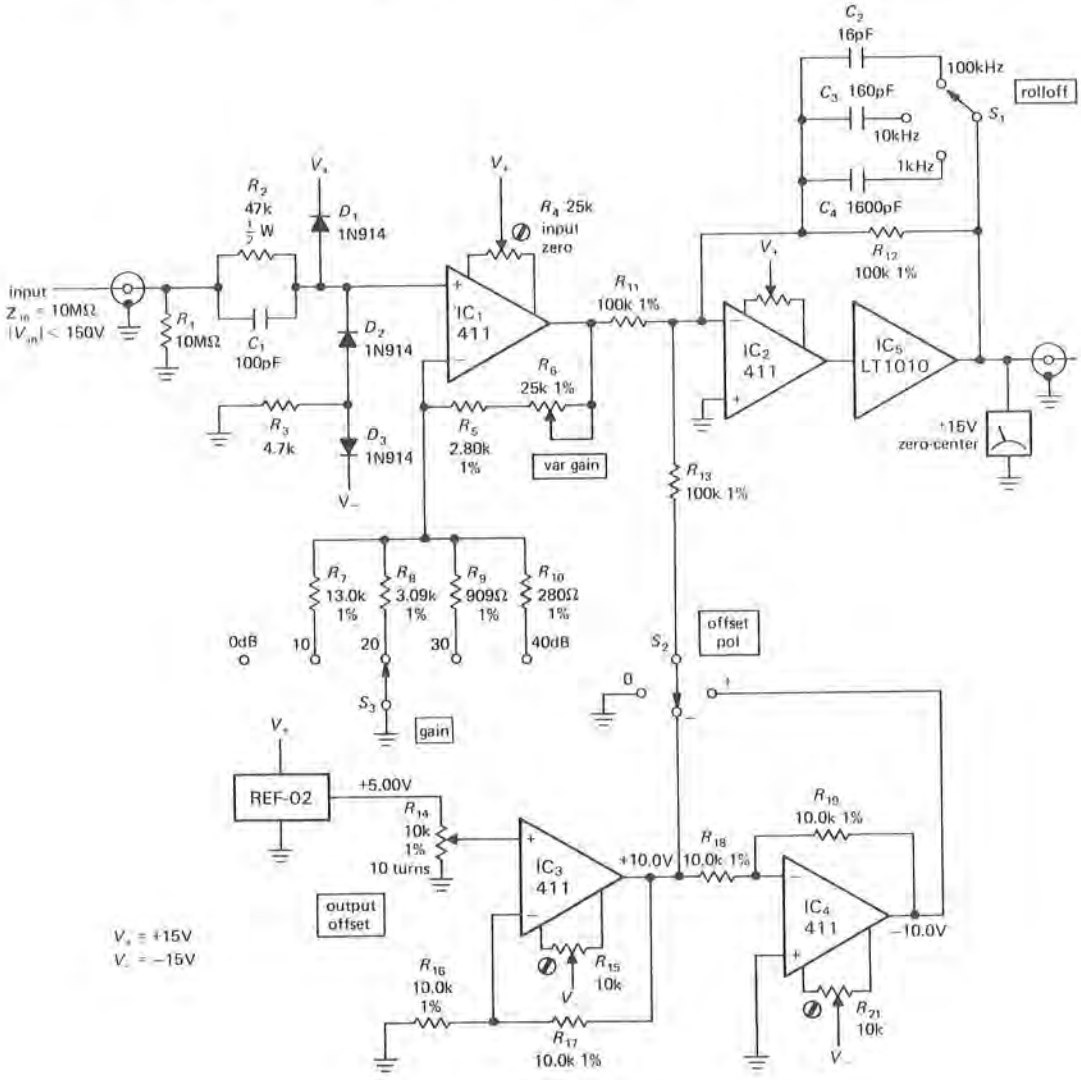


Figure 4.74. Laboratory dc amplifier with output offset.

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EXERCISE 4.12

Check that the gain is as advertised. How does the variable offset circuitry work?

4.29 Voltage-controlled oscillator

Figure 4.75 shows a clever circuit, borrowed from the application notes of several manufacturers. IC_1 is an integrator, rigged up so that the capacitor current (V_{in}/200k) changes sign, but not magnitude, when Q_1 conducts. IC_2 is connected as a Schmitt trigger, with thresholds at one-third and two-thirds of V_+. Q_1 is an n-channel MOSFET, used here as a switch; it is simpler to use than bipolar transistors in this sort of application, but an alternative circuit using *npn* transistors is shown in addition. In either case, the bottom side of R_4 is pulled to ground when the output is HIGH and open-circuited when the output is LOW.

An unusual feature of this circuit is its operation from a single positive supply. The 3160 (internally compensated version of the 3130) has FETs as output transistors, guaranteeing a full swing between V_+ and ground at the output; this ensures that the thresholds of the Schmitt don't drift, as they would with an op-amp of conventional output-stage design, with its ill-defined limits of output swing. In this case this means that the frequency and amplitude of the triangle wave will be stable. Note that the frequency depends on the ratio V_{in}/V_+; this means that if V_{in} is generated from V_+ by a resistive divider (made from some sort of resistive transducer, say), the output frequency won't vary with V_+, only with changes in resistance.

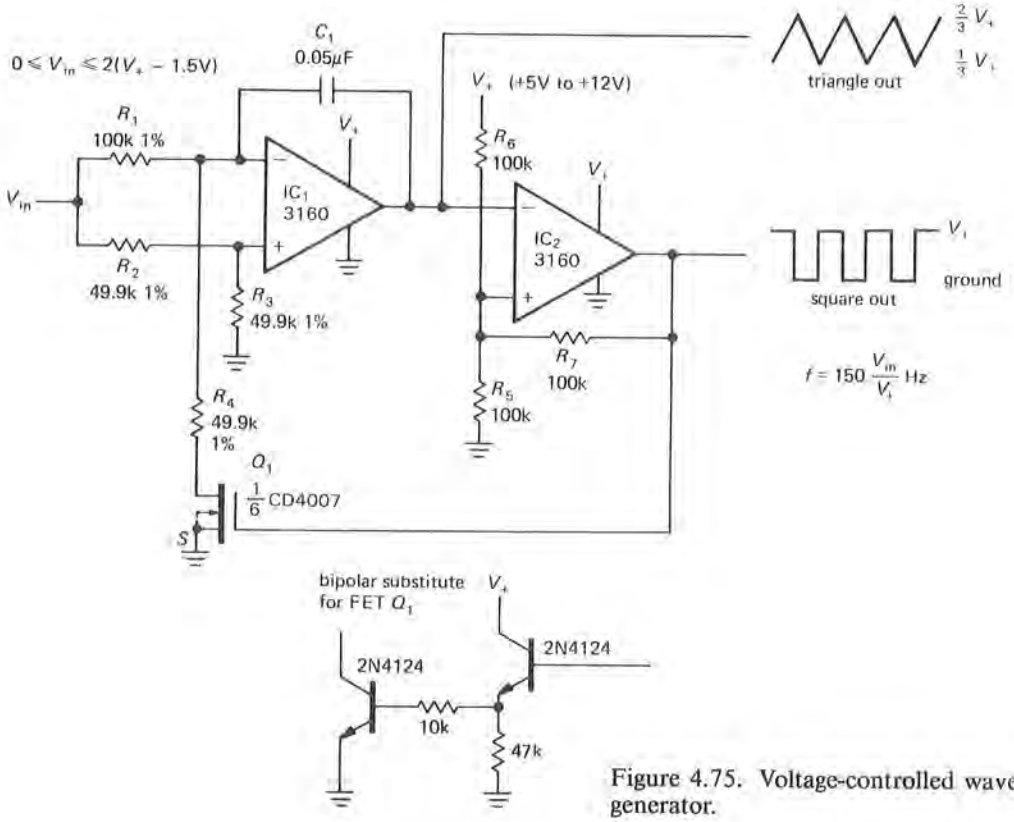


Figure 4.75. Voltage-controlled waveform generator.

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EXERCISE 4.13

Show that the output frequency is given by $f(\text{Hz}) = 150V_{in}/V_+$. Along the way, verify that the Schmitt thresholds and integrator currents are as advertised.

□ 4.30 JFET linear switch with R_{ON} compensation

In Chapter 3 we considered MOSFET linear switches in some detail. It is also possible to use JFETs as linear switches. However, you have to be more careful about gate signals so that gate conduction doesn't occur. Figure 4.76 shows a typical arrangement. The gate is held well below ground to keep the JFET pinched off. This means that if the input signals go negative, the gate must be held at least V_P below the most negative input swing. To bring the FET into conduction, the control input is brought more positive than the most positive input excursion. The diode is then reverse-biased, and the gate rides at source voltage via the 1M resistor.

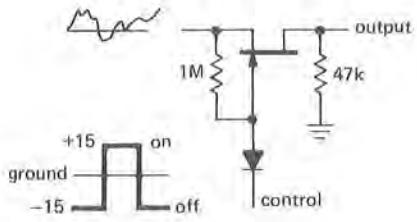


Figure 4.76

The awkwardness of this circuit probably accounts for much of the popularity of MOSFETs in linear switch applications. However, it is possible to devise an elegant JFET linear switch circuit if you use an op-amp, since you can tie the JFET source to the virtual ground at the summing junction of an inverting amplifier. Then you simply bring the gate to ground potential to turn the JFET on. This arrangement has the added advantage of providing a method of canceling precisely the errors caused by finite R_{ON} and its nonlinearity. Figure 4.77 shows the circuit.

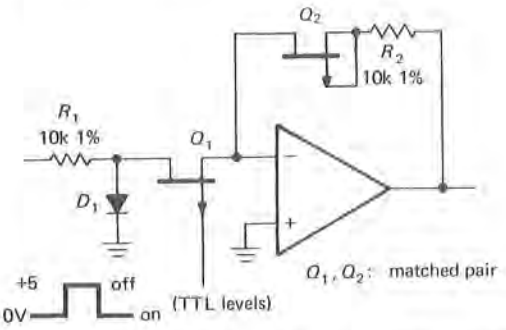


Figure 4.77. JFET-switched amplifier with R_{ON} cancellation.

There are two noteworthy features of this circuit: (a) When Q_1 is ON (gate grounded), the overall circuit is an inverter with identical impedances in the input and feedback circuits. That results in the cancellation of any effects of finite or nonlinear ON resistance, assuming the FETs are matched in R_{ON}. (b) Because of the low pinch-off voltage of JFETs, the circuit will work well with a control signal of zero to +5 volts, which is what you get with standard digital logic circuits (see Chapters 8 and 9). The inverting configuration, with Q_1's source connected to a virtual ground (the summing junction), simplifies circuit operation, since there are no signal swings on Q_1's source in the ON state; D_1 prevents FET turn-on for positive input swings when Q_1 is OFF, and it has no effect when the switch is closed.

There are p-channel JFETs with low pinch-off voltages available in useful configurations at low prices. For example, the IH5009–IH5024 family includes devices with four input FETs and one cancellation FET in a single DIP package, with R_{ON} of 100 ohms and a price less than two dollars. Add an op-amp and a few resistors and you've got a 4-input multiplexer. Note that the same R_{ON} cancellation trick can be used with MOSFET switches.

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□ 4.31 TTL zero-crossing detector

The circuit shown in Figure 4.78 generates an output square wave for use with TTL logic (zero to +5V range) from an input wave of any amplitude up to 100 volts. R_1, combined with D_1 and D_2, limits the input swing to −0.6 volt to +5.6 volts, approximately. Resistive divider R_2R_3 is necessary to limit negative swing to less than 0.3 volt, the limit for a 393 comparator. R_5 and R_6 provide hysteresis, with R_4 setting the trigger points symmetrically about ground. The input impedance is nearly constant, because of the large R_1 value relative to the other resistors in the input attenuator. A 393 is used because its inputs can go all the way to ground, making single-supply operation simple.

EXERCISE 4.14
Verify that the trigger points are at ±25mV at the input signal.

□ 4.32 Load-current-sensing circuit

The circuit shown in Figure 4.79 provides a voltage output proportional to load current, for use with a current regulator, metering circuit, or whatever. The voltage across the 4-terminal resistor R_S goes from zero to 0.1 volt, with probable common-mode offset due to the effects of resistance in the ground lead (note that the power supply is grounded at the output). For that reason the op-amp is wired as a differential amplifier, with gain of 100. Voltage offset is trimmed externally with R_8, since the LT1013 doesn't have internal trimming circuitry (the single LT1006 does, however). A zener reference with a few percent stability is adequate for trimming, since the trimming is itself a small correction (you hope!). The venerable 358 could have been chosen because both inputs and output also go all the way to ground. V_+ could be unregulated, since the power-supply rejection of the op-amp is more than adequate, 100dB (typ) in this case.

FEEDBACK AMPLIFIER FREQUENCY COMPENSATION

If you look at a graph of open-loop voltage gain versus frequency for several op-amps,

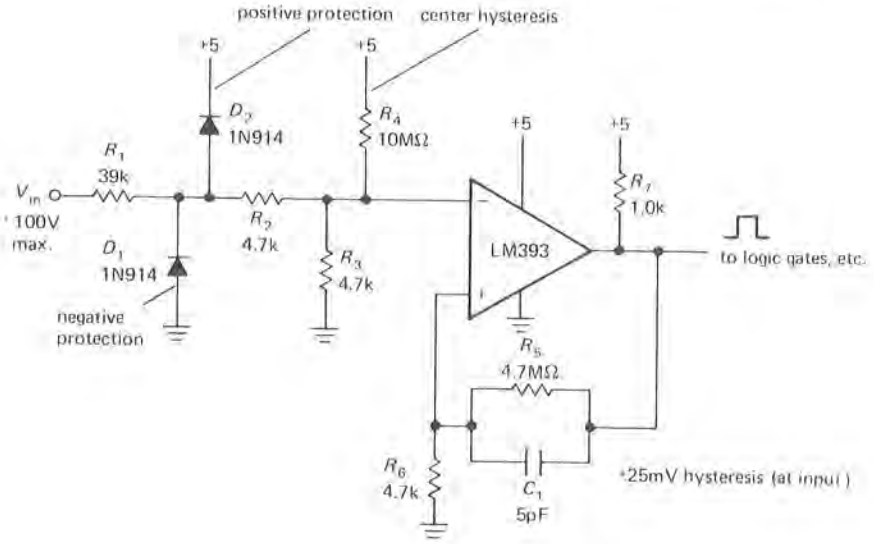


Figure 4.78. Zero-crossing level detector with input protection.

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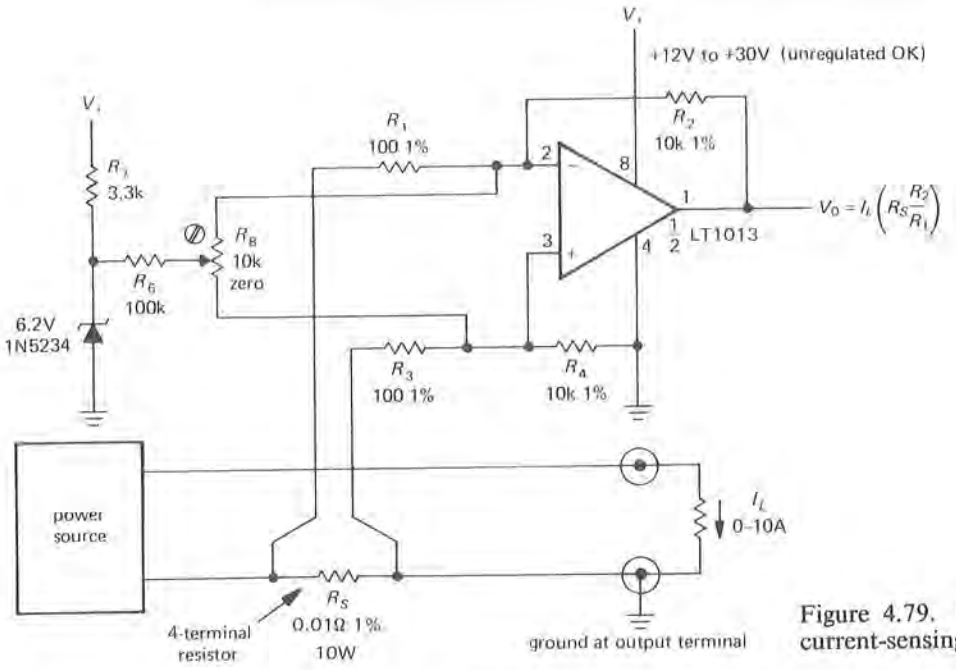


Figure 4.79. High-power current-sensing amplifier.

you'll see something like the curves in Figure 4.80. From a superficial look at such a *Bode plot* (a log-log plot of gain

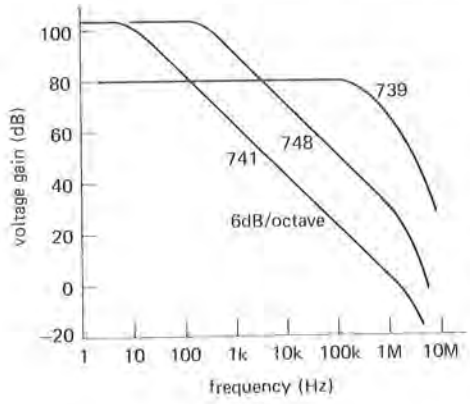


Figure 4.80

and phase versus frequency) you might conclude that the 741 is an inferior op-amp, since its open-loop gain drops off so rapidly with increasing frequency. In fact, that rolloff is built into the op-amp intentionally and is recognizable as the same −6db/octave curve characteristic of an *RC* low-pass filter. The 748, by comparison, is identical with the 741 except that it is *uncompensated* (as is the 739). Op-amps are generally available in internally compensated varieties and uncompensated varieties; let's take a look at this business of frequency compensation.

4.33 Gain and phase shift versus frequency

An op-amp (or, in general, any multistage amplifier) will begin to roll off at some frequency because of the low-pass filters formed by signals of finite source impedance driving capacitive loads within the amplifier stages. For instance, it is common to have an input stage consisting of a differential amplifier, perhaps with current mirror load (see the LM358 schematic in Fig. 4.54), driving a common-emitter second stage. For now, imagine that the capacitor labeled C_C in that circuit is removed. The high output impedance of the input stage, in combination with

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junction capacitance C_{ie} and feedback capacitance C_{cb} (Miller effect, see Sections 2.19 and 13.04) of the following stage, forms a low-pass filter whose 3dB point might fall somewhere in the range of 100Hz to 10kHz.

The decreasing reactance of the capacitor with increasing frequency gives rise to the characteristic 6db/octave rolloff: At sufficiently high frequencies (which may be below 1kHz), the capacitive loading dominates the collector load impedance, resulting in a voltage gain $G_V = g_m X_C$, i.e., the gain drops off as $1/f$. It also produces a 90° lagging phase shift at the output relative to the input signal. (You can think of this as the tail of an RC low-pass filter characteristic, where R represents the equivalent source impedance driving the capacitive load. However, it is not necessary to have any actual resistors in the circuit.)

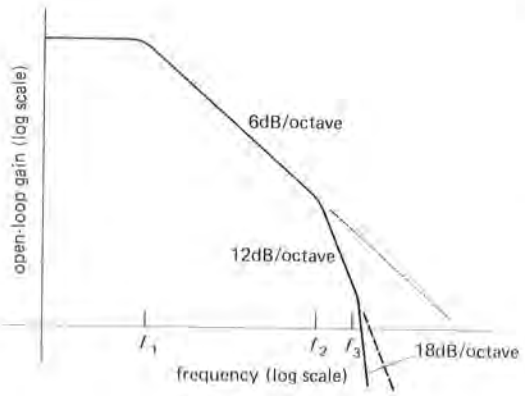


Figure 4.81

In a multistage amplifier there will be additional rolloffs at higher frequencies, caused by low-pass filter characteristics in the other amplifier stages, and the overall open-loop gain will look something like that shown in Figure 4.81. The open-loop gain begins dropping at 6dB/octave at some low frequency f_1, due to capacitive loading of the first-stage output. It continues dropping off with that slope until an internal RC of another stage rears its ugly head at frequency f_2, beyond which the rolloff goes at 12dB/octave, and so on.

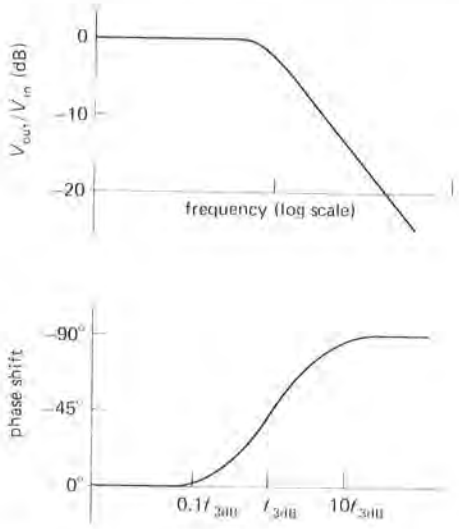


Figure 4.82. Bode plot: gain and phase versus frequency.

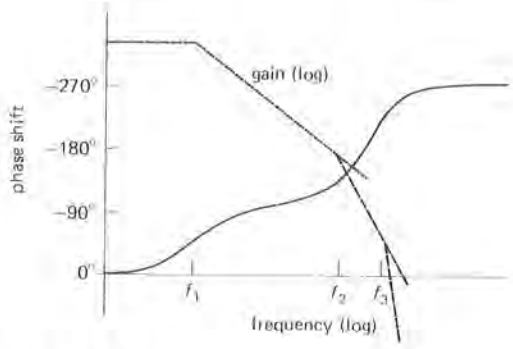


Figure 4.83

What is the significance of all this? Remember that an RC low-pass filter has a phase shift that looks as shown in Figure 4.82. Each low-pass filter within the amplifier has a similar phase-shift characteristic, so the overall phase shift of the hypothetical amplifier will be as shown in Figure 4.83.

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Now here's the problem: If you were to connect this amplifier as an op-amp follower, for instance, it would oscillate. That's because the open-loop phase shift reaches 180° at some frequency at which the gain is still greater than 1 (negative feedback becomes positive feedback at that frequency). That's all you need to generate an oscillation, since any signal whatsoever at that frequency builds up each time around the feedback loop, just like a public address system with the gain turned up too far.

Stability criterion

The criterion for stability against oscillation for a feedback amplifier is that its open-loop phase shift must be less than 180° at the frequency at which the loop gain is unity. This criterion is hardest to satisfy when the amplifier is connected as a follower, since the loop gain then equals the open-loop gain, the highest it can be. Internally compensated op-amps are designed to satisfy the stability criterion even when connected as followers; thus they are stable when connected for any closed-loop gain with a simple resistive feedback network. As we hinted earlier, this is accomplished by deliberately modifying an existing internal rolloff in order to put the 3dB point at some low frequency, typically 1Hz to 20Hz. Let's see how that works.

4.34 Amplifier compensation methods

Dominant-pole compensation

The goal is to keep the open-loop phase shift much less than 180° at all frequencies for which the loop gain is greater than 1. Assuming that the op-amp may be used as a follower, the words "loop gain" in the last sentence can be replaced by "open-loop gain." The easiest way to do this is to add enough capacitance at the point in the circuit that produces the initial 6dB/octave rolloff, so that the open-loop gain drops to unity at about the 3dB frequency of the next "natural" RC filter. In this way the open-loop phase shift is held at a constant 90° over most of the passband, increasing toward 180° only as the gain approaches unity. Figure 4.84 shows the idea. Without compensation the open-loop gain drops toward 1, first at 6dB/octave, then at 12dB/octave, etc., resulting in phase shifts of 180° or more before the gain has reached 1. By moving the first rolloff down in frequency (forming a "dominant pole"), the rolloff is controlled so that the phase shift begins to rise above 90° only as the open-loop gain approaches unity. Thus, by sacrificing open-loop gain, you buy stability. Since the natural rolloff of lowest frequency is usually caused by Miller effect in the stage driven by the input differential amplifier, the usual method of dominant-pole compensation consists simply of adding additional feedback capacitance around the second-stage transistor, so that the combined voltage gain of

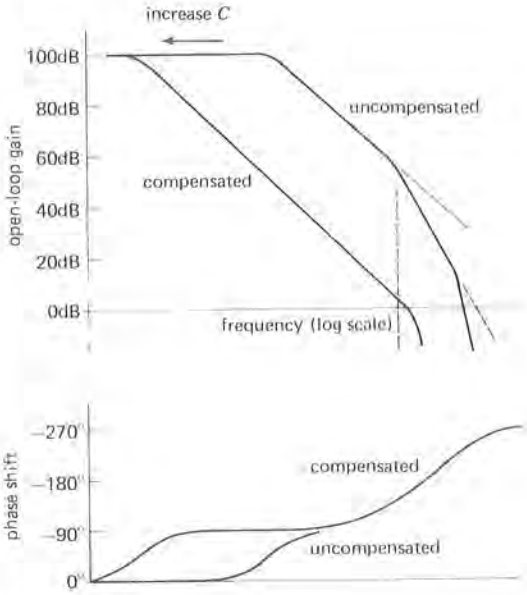


Figure 4.84

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the two stages is $g_m X_C$ or $g_m/2\pi f C_{\text{comp}}$ over the compensated region of the amplifier's frequency response (Fig. 4.85). In practice, Darlington-connected transistors would probably be used for both stages.

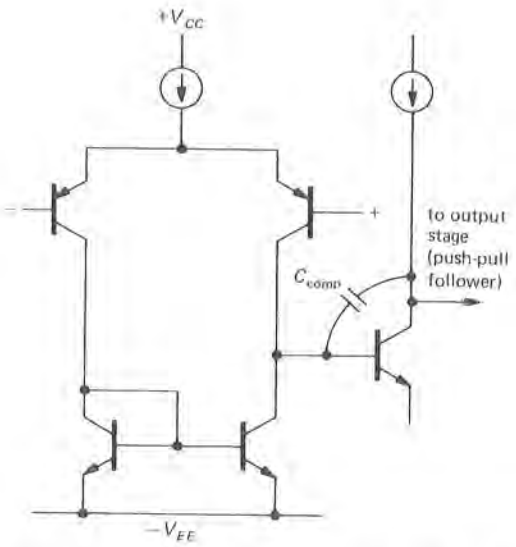


Figure 4.85. Classic op-amp input stage with compensation.

By putting the dominant-pole unity-gain crossing at the 3dB point of the next rolloff, you get a phase margin of about 45° in the worst case (follower), since a single RC filter has a 45° lagging phase shift at its 3dB frequency, i.e., the phase margin equals 180° − (90° + 45°), with the 90° coming from the dominant pole.

An additional advantage of using a Miller-effect pole for compensation is that the compensation is inherently insensitive to changes in voltage gain with temperature, or manufacturing spread of gain: Higher gain causes the feedback capacitance to look larger, moving the pole downward in frequency in exactly the right way to keep the unity-gain crossing frequency unchanged. In fact, the actual 3dB frequency of the compensation pole is quite irrelevant; what matters is the point at which it intersects the unity-gain axis (Fig. 4.86).

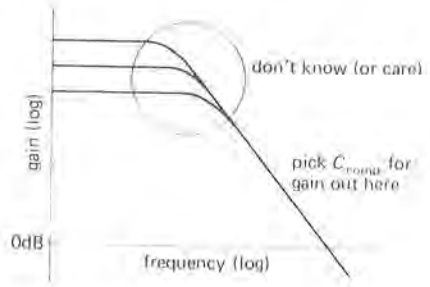


Figure 4.86

Uncompensated op-amps

If an op-amp is used in a circuit with closed-loop gain greater than 1 (i.e., not a follower), it is not necessary to put the pole (the term for the "corner frequency" of a low-pass filter) at such a low frequency, since the stability criterion is relaxed because of the lower loop gain. Figure 4.87 shows the situation graphically.

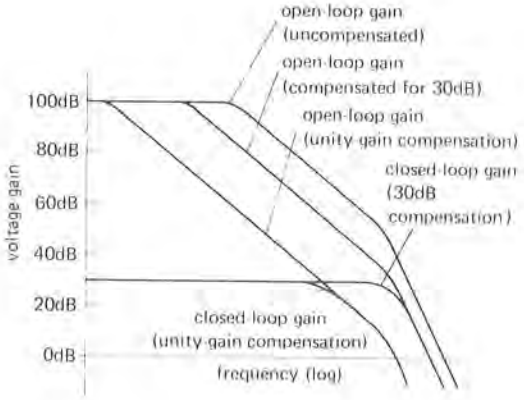


Figure 4.87

For a closed-loop gain of 30dB, the loop gain (which is the ratio of the open-loop gain to the closed-loop gain) is less than for a follower, so the dominant pole can be placed at a higher frequency. It is chosen

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so that the open-loop gain reaches 30dB (rather than 0dB) at the frequency of the next natural pole of the op-amp. As the graph shows, this means that the open-loop gain is higher over most of the frequency range, and the resultant amplifier will work at higher frequencies. Some op-amps are available in uncompensated versions [e.g., the 748 is an uncompensated 741; the same is true for the 308 (312), 3130 (3160), HA5102 (HA5112), etc.], with recommended external capacitance values for a selection of minimum closed-loop gains. They are worth using if you need the added bandwidth and your circuit operates at high gain. An alternative is to use "decompensated" (a better word might be "undercompensated") op-amps, such as the 357, which are internally compensated for closed-loop gains greater than some minimum ($A_V > 5$ in the case of the 357).

□ *Pole-zero compensation*

It is possible to do a bit better than with dominant-pole compensation by using a compensation network that begins dropping (6dB/octave, a "pole") at some low frequency, then flattens out again (it has a "zero") at the frequency of the second natural pole of the op-amp. In this way the amplifier's second pole is "canceled," giving a smooth 6dB/octave rolloff up to the amplifier's third pole. Figure 4.88 shows a frequency response plot. In practice, the zero is chosen to cancel the amplifier's second pole; then the position of the first pole is adjusted so that the overall response reaches unity gain at the frequency of the amplifier's third pole. A good set of data sheets will often give suggested component values (an R and a C) for pole-zero compensation, as well as the usual capacitor values for dominant-pole compensation.

As you will see in Section 13.06, moving the dominant pole downward in frequency actually causes the second pole of the amplifier to move upward somewhat in frequency, an effect known as "pole splitting." The frequency of the canceling zero will be chosen accordingly.

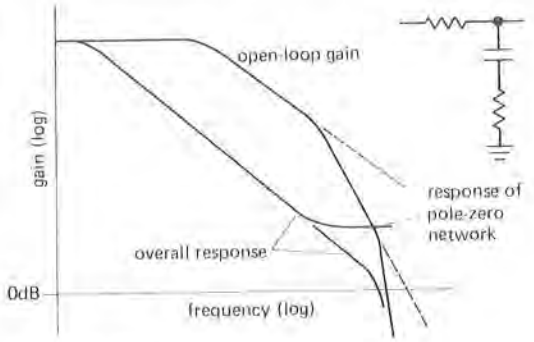


Figure 4.88

□ 4.35 Frequency response of the feedback network

In all of the discussion thus far we have assumed that the feedback network has a flat frequency response; this is usually the case, with the standard resistive voltage divider as a feedback network. However, there are occasions when some sort of equalization amplifier is desired (integrators and differentiators are in this category) or when the frequency response of the feedback network is modified to improve amplifier stability. In such cases it is important to remember that the Bode plot of loop gain versus frequency is what matters, rather than the curve of open-loop gain. To make a long story short, the curve of ideal closed-loop gain versus frequency should intersect the curve of open-loop gain, with a difference in slopes of 6dB/octave. As an example, it is common practice to put a small capacitor (a few picofarads) across the feedback resistor in the usual inverting or noninverting amplifier. Figure 4.89 shows the circuit and Bode plot.

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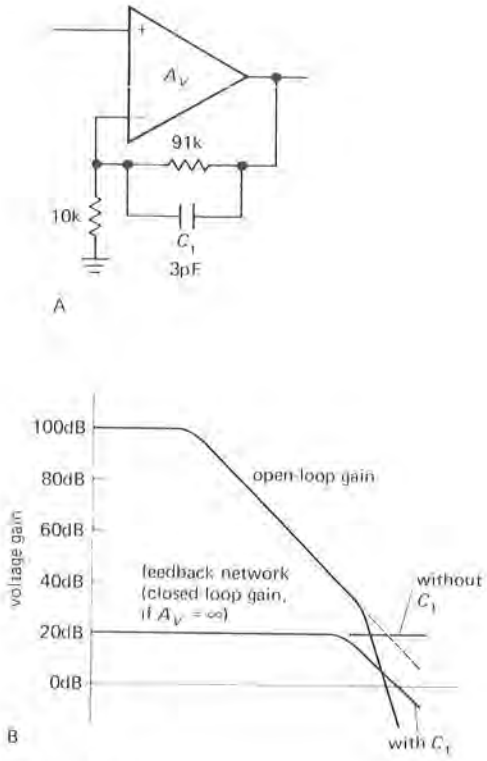


Figure 4.89

The amplifier would have been close to instability with a flat feedback network, since the loop gain would have been dropping at nearly 12dB/octave where the curves meet. The capacitor causes the loop gain to drop at 6dB/octave near the crossing, guaranteeing stability. This sort of consideration is very important when designing differentiators, since an ideal differentiator has a closed-loop gain that rises at 6dB/octave; it is necessary to roll off the differentiator action at some moderate frequency, preferably going over to a 6dB/octave rolloff at high frequencies. Integrators, by comparison, are very friendly in this respect, owing to their 6dB/octave closed-loop rolloff. It takes real talent to make a low-frequency integrator oscillate!

What to do

In summary, you are generally faced with the choice of internally compensated or uncompensated op-amps. It is simplest to use the compensated variety, and that's the usual choice. You might consider the internally compensated LF411 first. If you need greater bandwidth or slew rate, look for a faster compensated op-amp (see Table 4.1 or 7.3 for many choices). If it turns out that nothing is suitable, and the closed-loop gain is greater than unity (as it usually is), you can use an uncompensated op-amp, with an external capacitor as specified by the manufacturer for the gain you are using.

A number of op-amps offer another choice: a "decompensated" version, requiring no external compensation components, but only usable at some minimum gain greater than unity. For example, the popular OP-27 low-noise precision op-amp (unity-gain-compensated) is available as the decompensated OP-37 (minimum gain of 5), offering roughly seven times the speed, and also as the decompensated HA-5147 (minimum gain of 10), with 15 times the speed.

□ Example: 60Hz power source

Uncompensated op-amps also give you the flexibility of overcompensating, a simple solution to the problem of additional phase shifts introduced by other stuff in the feedback loop. Figure 4.90 shows a nice example. This is a low-frequency amplifier designed to generate a 115 volt ac power output from a variable 60Hz low-level sine-wave input (it goes with the 60Hz synthesizer circuit described in Section 8.31). The op-amp, together with R_2 and R_3, forms a $\times 100$ gain block; this is then used as the relatively low "open-loop gain" for overall feedback. The op-amp output drives the push-pull output stage, which in turn drives the transformer primary. Low-frequency feedback is taken from the transformer output via R_{10}, in order to generate low distortion and a stable output voltage under load variations. Because of

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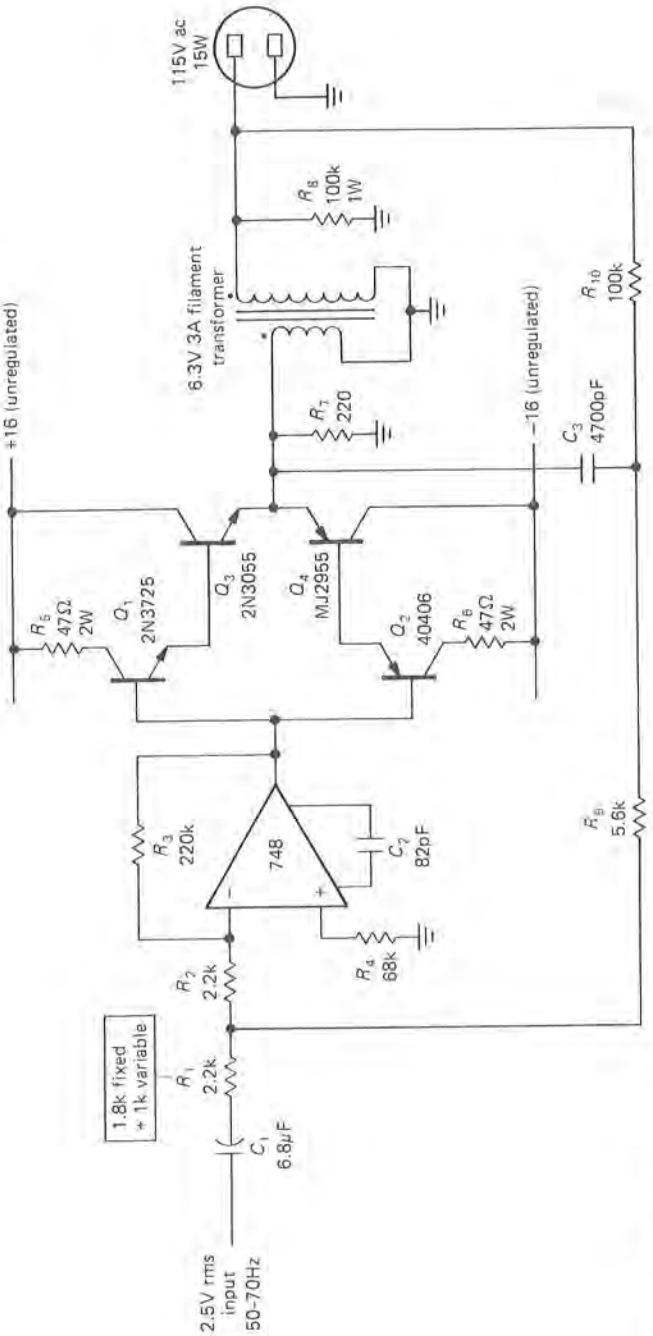


Figure 4.90. Output amplifier for 60Hz power source.

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the unacceptably large phase shifts of such a transformer at high frequencies, the circuit is rigged up so that at higher frequencies the feedback comes from the low-voltage input to the transformer, via C_3. The relative sizes of R_9 and R_{10} are chosen to keep the amount of feedback constant at all frequencies. Even though high-frequency feedback is taken directly from the push-pull output, there are still phase shifts associated with the reactive load (the transformer primary) seen by the transistors. In order to ensure good stability, even with reactive loads at the 115 volt output, the op-amp has been overcompensated with an 82pF capacitor (30pF is the normal value for unity gain compensation). The loss of bandwidth that results is unimportant in a low-frequency application like this.

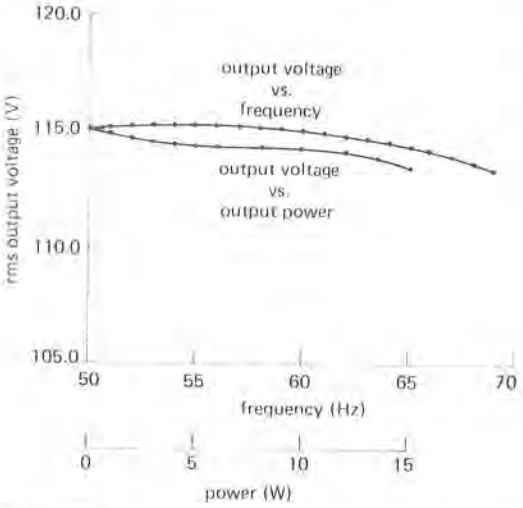


Figure 4.91

An application such as this represents a compromise, since ideally you would like to have plenty of loop gain to stabilize the output voltage against variations in load current. But a large loop gain increases the tendency of the amplifier to oscillate, especially if a reactive load is attached. This is because the reactive load, in combination with the transformer's finite output impedance, causes additional phase shifts within the low-frequency feedback loop. Since this circuit was built to derive a telescope's synchronous driving motors (highly inductive loads), the loop gain was intentionally kept low. Figure 4.91 shows a graph of the ac output voltage versus load, which illustrates good (but not great) regulation.

Motorboating

In ac-coupled feedback amplifiers, stability problems can also crop up at very low frequencies, due to the accumulated *leading* phase shifts caused by several capacitively coupled stages. Each blocking capacitor, in combination with the input resistance due to bias strings and the like, causes a leading phase shift that equals 45° at the low-frequency 3dB point and approaches 90° at lower frequencies. If there is enough loop gain, the system can go into a low-frequency oscillation picturesquely known as "motorboating." With the widespread use of dc-coupled amplifiers, motorboating is almost extinct. However, old-timers can tell you some good stories about it.

SELF-EXPLANATORY CIRCUITS

4.36 Circuit ideas

Some interesting circuit ideas, mostly lifted from manufacturers' data sheets, are shown in Figure 4.94.

4.37 Bad circuits

Figure 4.95 presents a zoo of intentional (mostly) blunders to amuse, amaze, and educate you. There are a few real howlers here this time. These circuits are guaranteed not to work. Figure out why. All op-amps run from ±15 volts unless shown otherwise.

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ADDITIONAL EXERCISES

(1) Design a "sensitive voltmeter" to have $Z_{in} = 1M\Omega$ and full-scale sensitivities of 10mV to 10V in four ranges. Use a 1mA meter movement and an op-amp. Trim voltage offsets if necessary, and calculate what the meter will read with input open, assuming **(a)** $I_B = 25pA$ (typical for a 411) and **(b)** $I_B = 80nA$ (typical for a 741). Use some form of meter protection (e.g., keep its current less than 200% of full scale), and protect the amplifier inputs from voltages outside the supply voltages. What do you conclude about the suitability of the 741 for low-level high-impedance measurements?

(2) Design an audio amplifier, using an OP-27 op-amp (low noise, good for audio), with the following characteristics: gain = 20dB, $Z_{in} = 10k$, $-3dB$ point = 20Hz. Use the noninverting configuration, and roll off the gain at low frequencies in such a way as to reduce the effects of input offset voltage. Use proper design to minimize the effects of input bias current on output offset. Assume that the signal source is capacitively coupled.

(3) Design a unity-gain phase splitter (see Chapter 2) using 411s. Strive for high input impedance and low output impedances. The circuit should be dc-coupled. At roughly what maximum frequency can you obtain full swing (27V pp, with $\pm 15V$ supplies), owing to slew rate limitations?

(4) El Cheapo brand loudspeakers are found to have a treble boost, beginning at 2kHz (+3dB point) and rising 6dB/octave. Design a simple RC filter, buffered with AD611 op-amps (another good audio chip) as necessary, to be placed between preamp and amplifier to compensate this rise. Assume that the preamp has $Z_{out} = 50k$ and that the amplifier has $Z_{in} = 10k$, approximately.

(5) A 741 is used as a simple comparator, with one input grounded; i.e., it is a zero-crossing detector. A 1 volt amplitude sine wave is fed into the other input (frequency1kHz). What voltage(s) will the input be when the output passes through zero volts? Assume that the slew rate is $0.5V/\mu s$ and that the op-amp's saturated output is ± 13 volts.

(6) The circuit in Figure 4.92 is an example of a "negative-impedance converter." **(a)** What is its input impedance? **(b)** If the op-amp's output range goes from V_+ to V_-, what range of input voltages will this circuit accommodate without saturation?

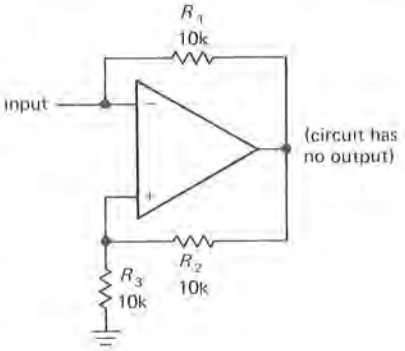


Figure 4.92

(7) Consider the circuit in the preceding problem as the 2-terminal black box (Fig. 4.93). Show how to make a dc amplifier with a gain of -10. Why can't you make a dc amplifier with a gain of $+10$? (Hint: The circuit is susceptible to a latchup condition for a certain range of source resistances. What is that range? Can you think of a remedy?)

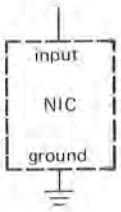
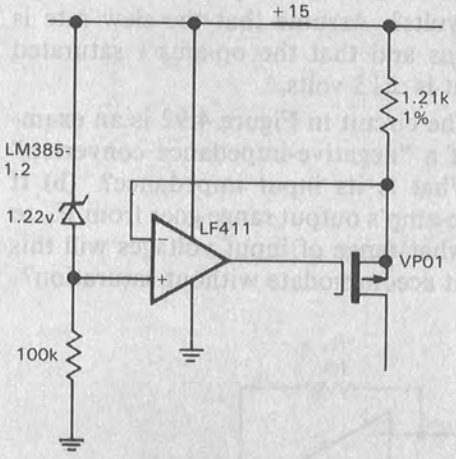


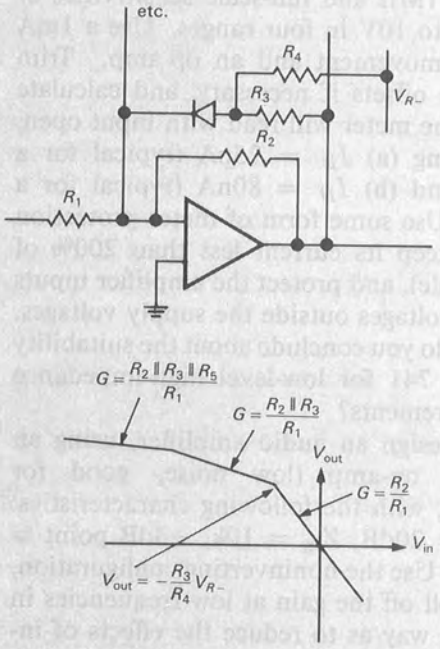
Figure 4.93

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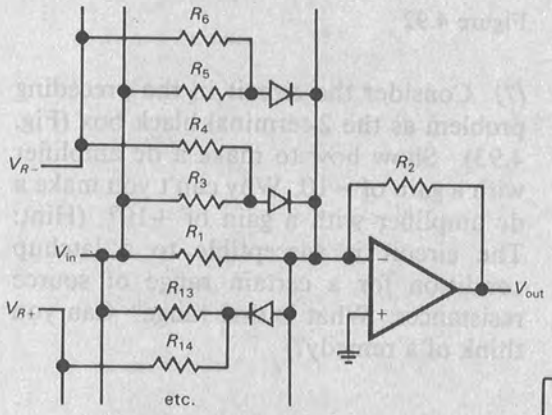


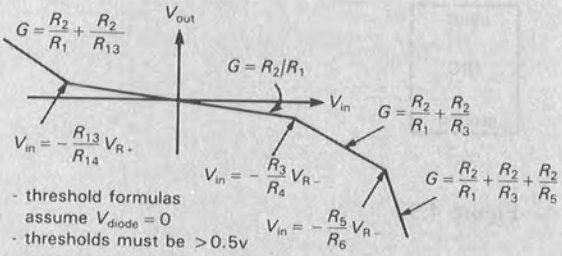
current source using PMOS FET

A. precision current source



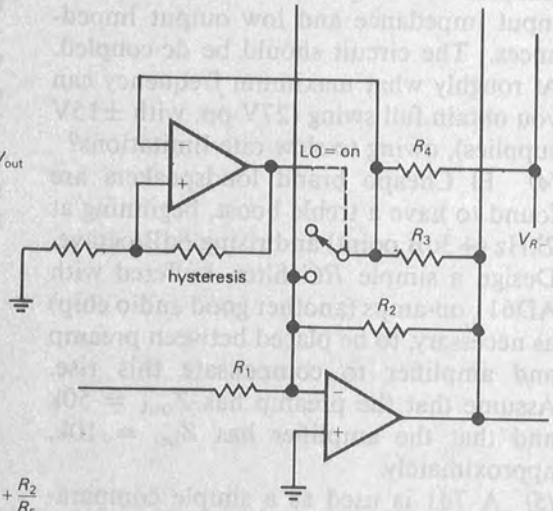
C. as in B, but gain decreases for outputs above threshold





- threshold formulas assume $V_{diode} = 0$
- thresholds must be $> 0.5v$

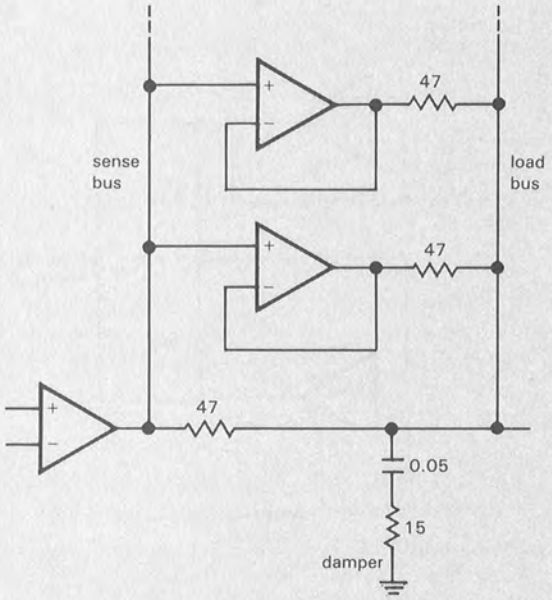
B. inverting piecewise-linear curve amplifier
G increases for inputs above threshold



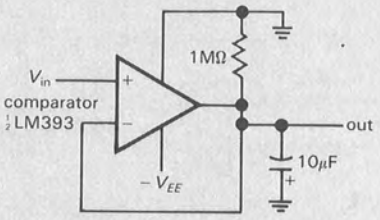
D. as in C, but with comparator and switch, acting as a "perfect" diode ($V_D = 0$)

Figure 4.94

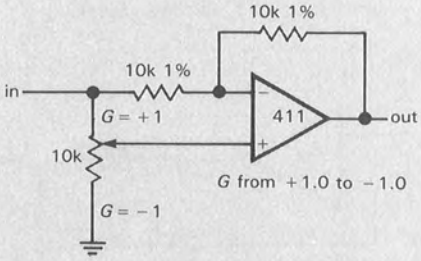
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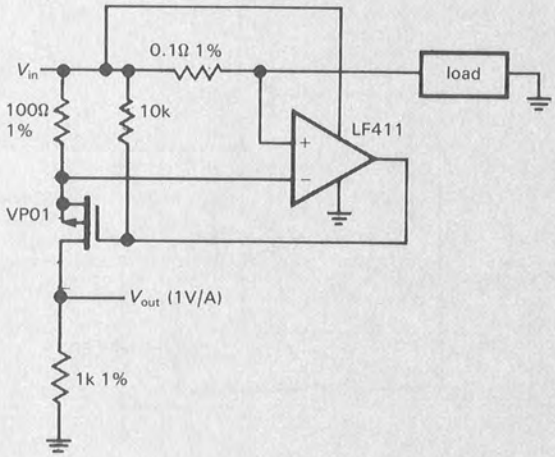
E. higher output current from additional op-amp sections; watch for excess heating



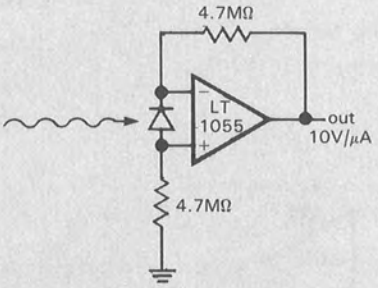
H. negative peak detector



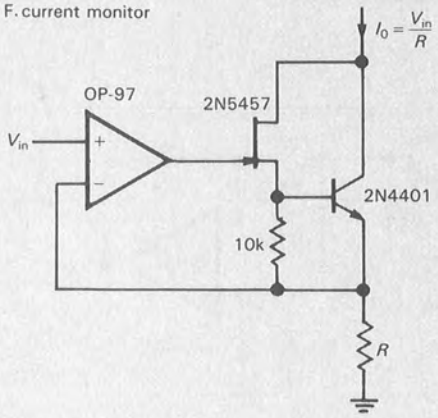
I. continuously variable gain



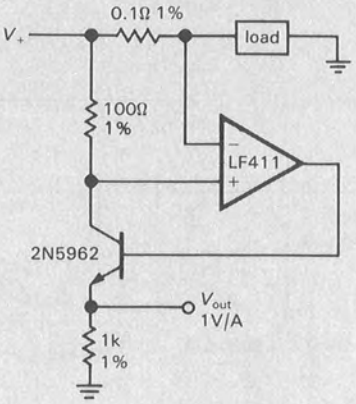
F. current monitor



J. photodiode amplifier



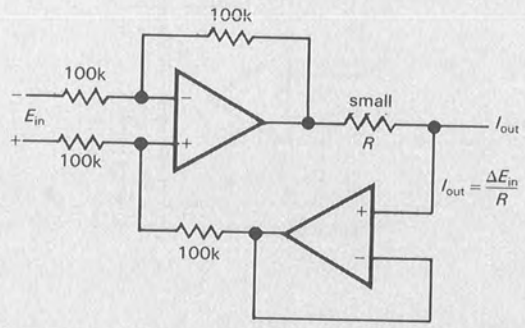
G. precision current sink



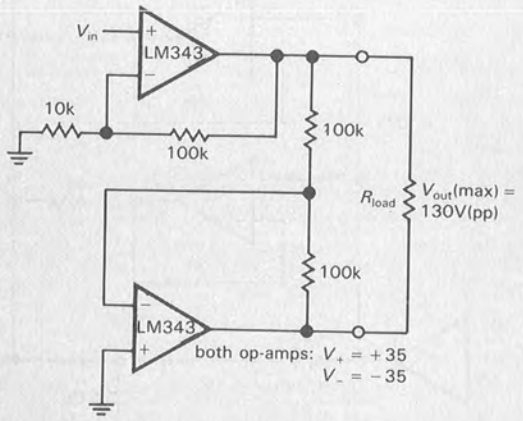
K. current monitor

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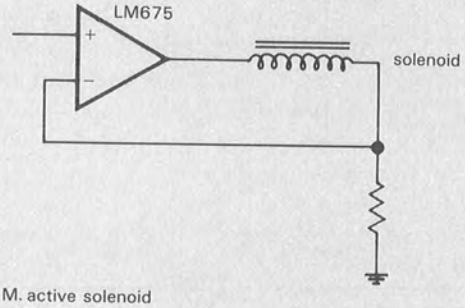
Circuit ideas (*cont.*)



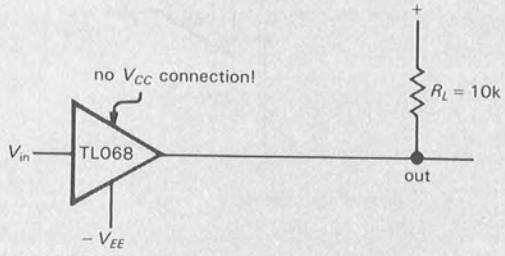
L. precision bipolarity current source



P. high-voltage (bridge) drive to floating load (gain = 22)

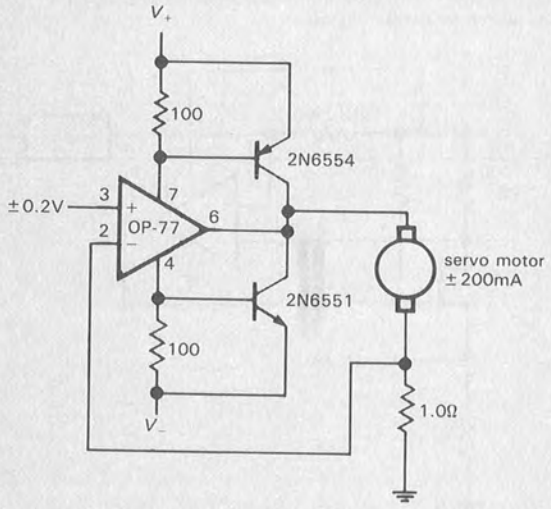


M. active solenoid

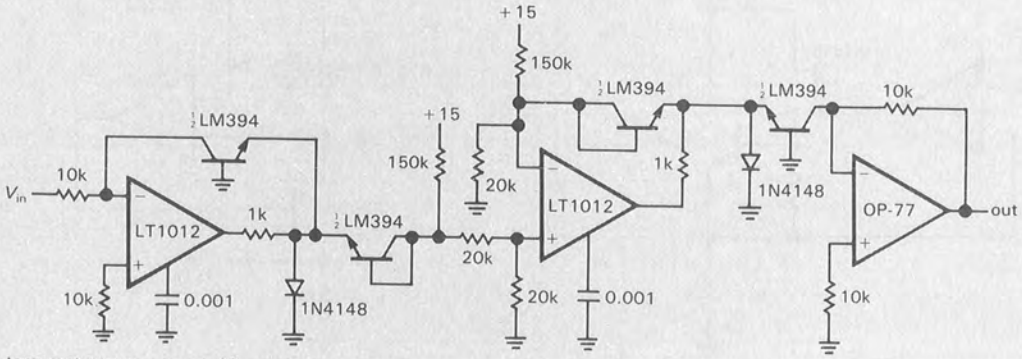


$V_{EE} + 3V < V_{in} < 30V$

N. unusual 3-pin JFET follower

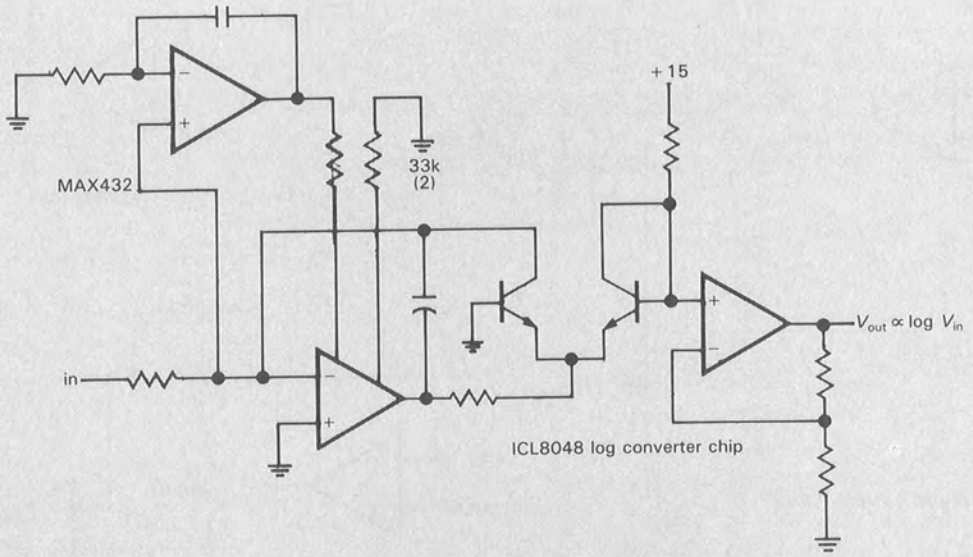


Q. 0.2A servo-motor amplifier

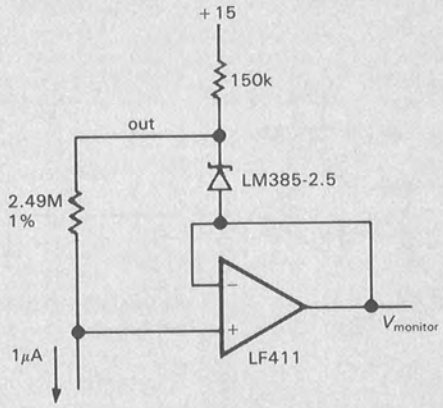


O. temperature-compensated log converter

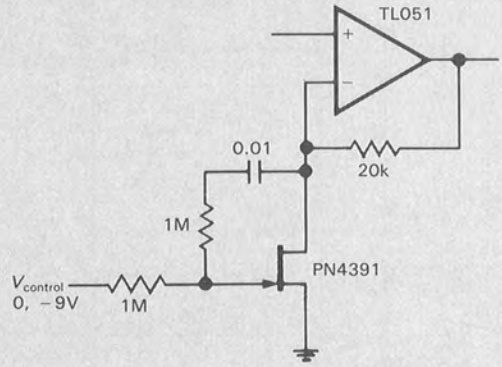
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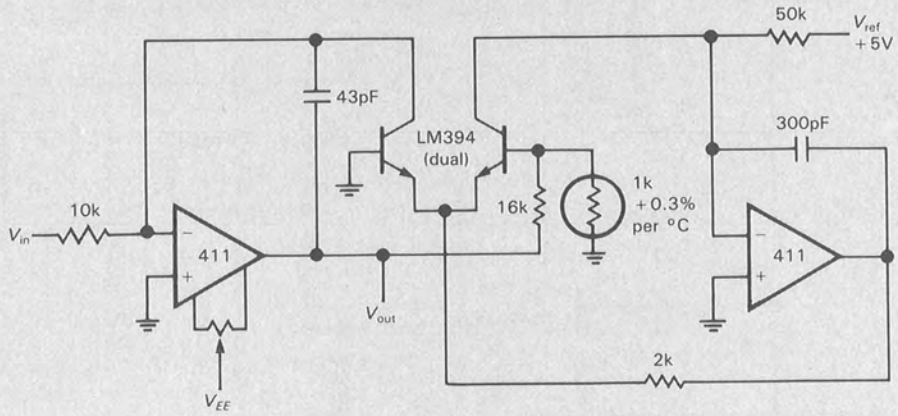
R. log converter with wide input range due to automatic nulling with a chopper amplifier



S. current source

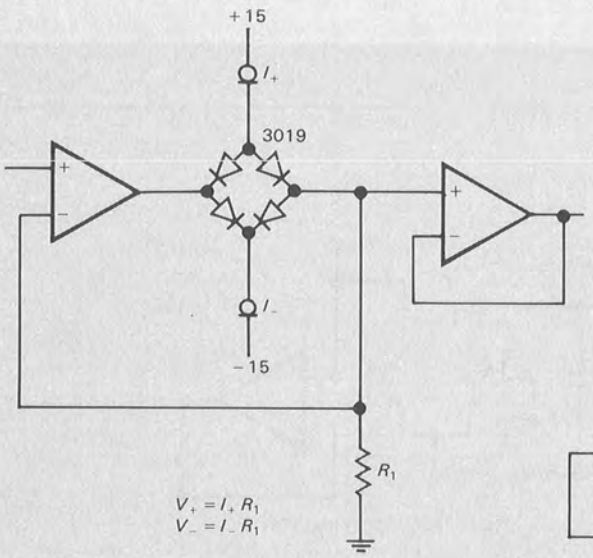


U. low-distortion variable-gain amplifier

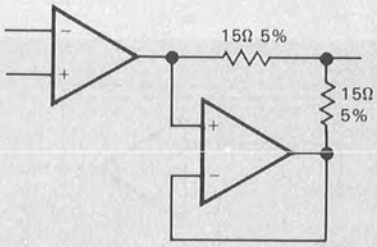


T. fast logarithmic converter

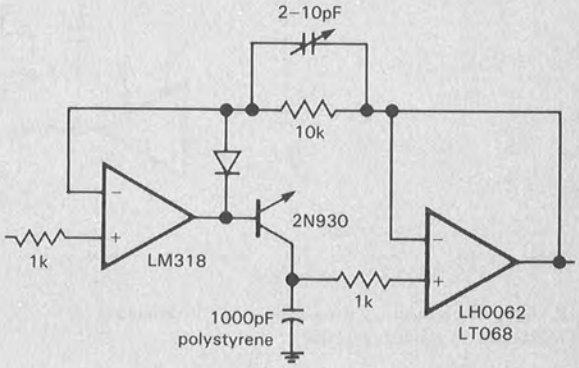
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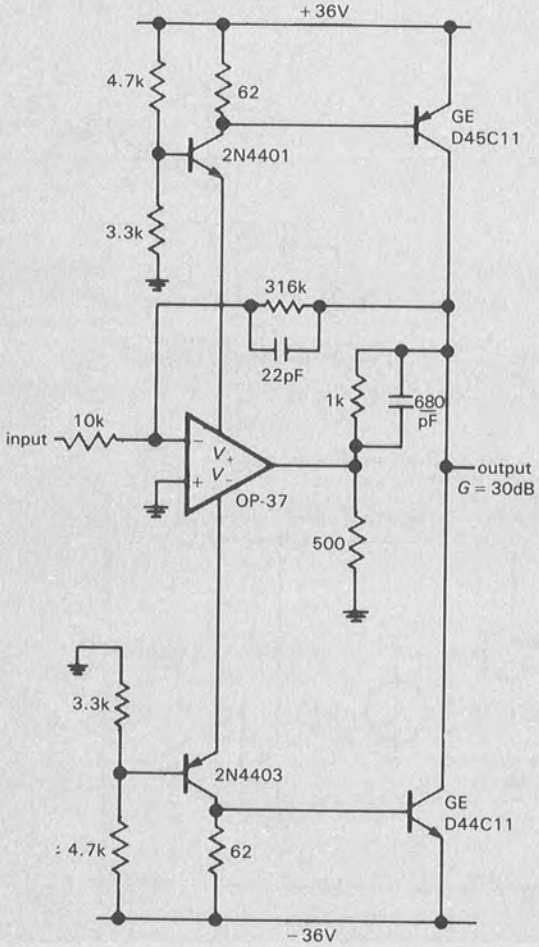
V. precision bipolarity limiter



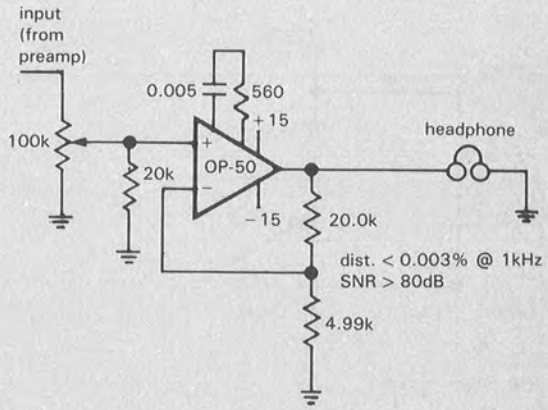
X. obtaining 2× output capability from a dual op-amp



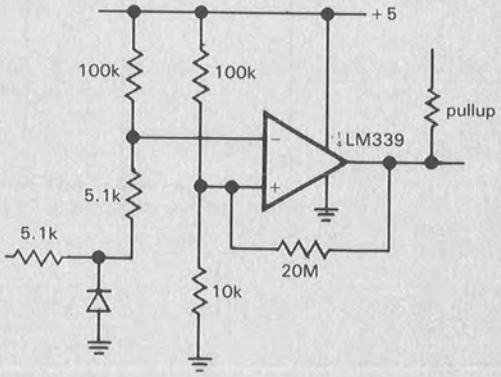
Y. high-speed peak detector



W. low-noise high-voltage op-amp (from PMI App. Note 106)

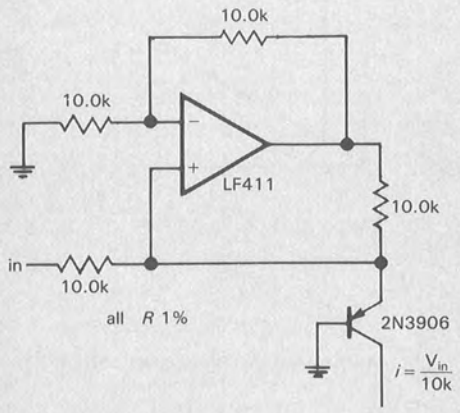


Z. low-distortion headphone amp (from PMI App. Note 106)

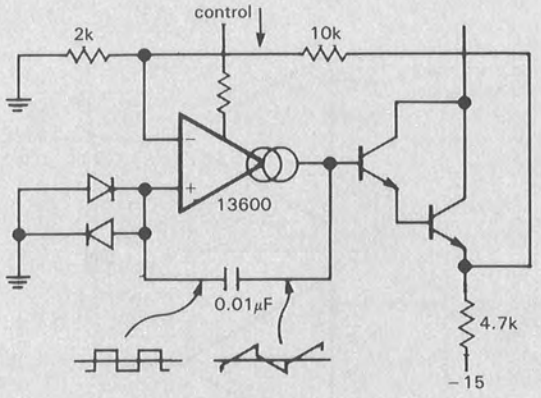


AA. zero-crossing detector, single supply

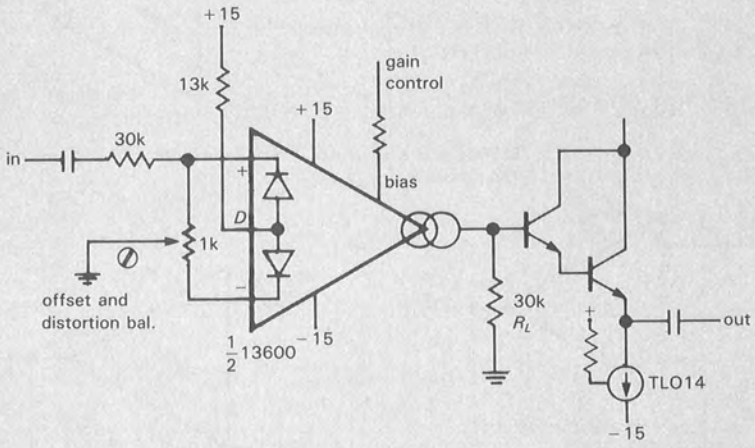
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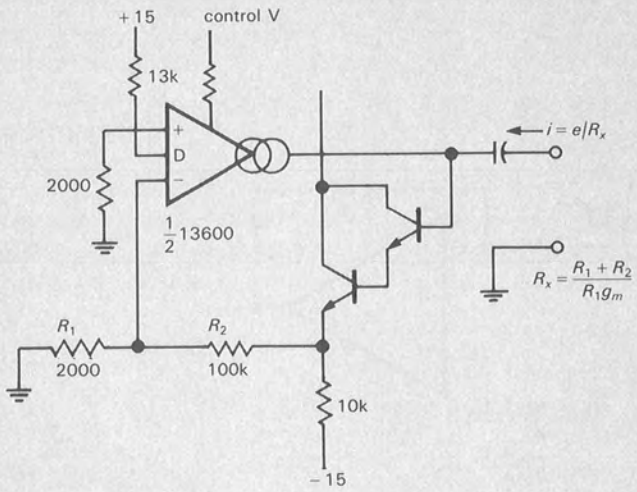
BB. Howland-style current source for transconductance voltage-current control circuits (1μA to 1mA)



EE. voltage-contolled oscillator with transconductance amplifier

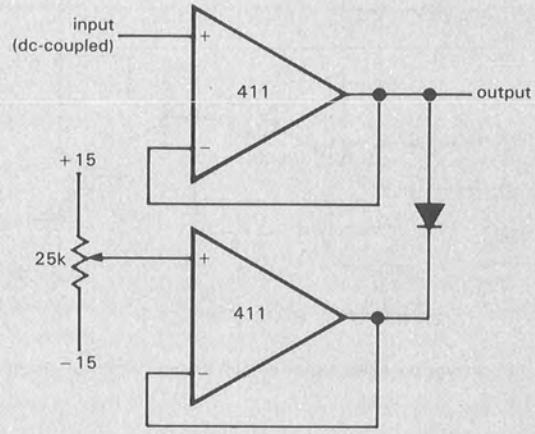


CC. transconductance linearized voltage-controlled amplifier (VCA)

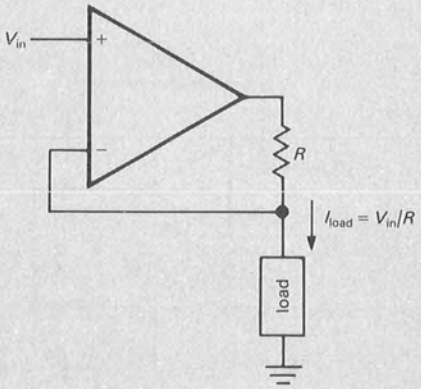


DD. voltage-controlled AC load resistor

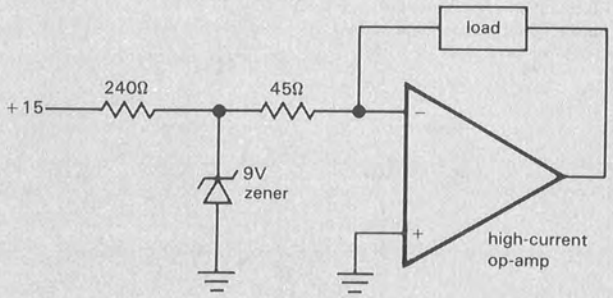
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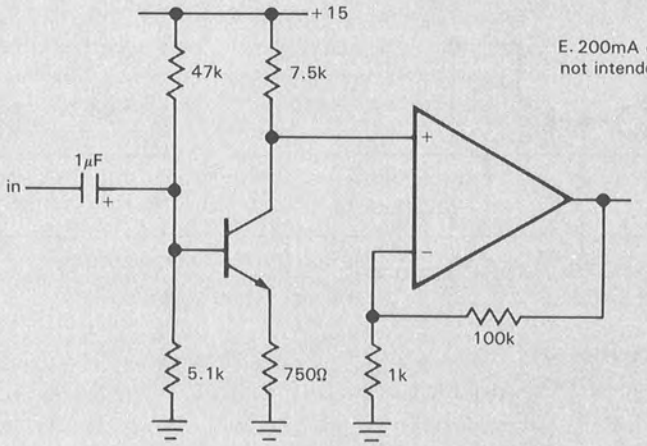
A. adjustable clamp



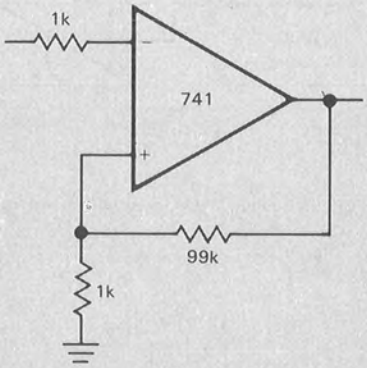
D. current source (voltage-programmed)



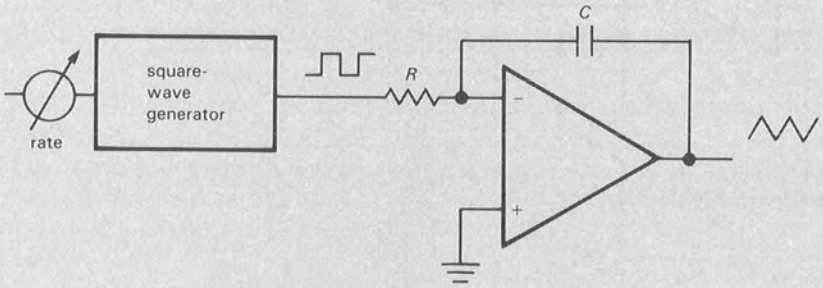
E. 200mA current source (from Diefenderfer, not intended as a "bad circuit")



B. × 100 op-amp output stage for audio amplifier



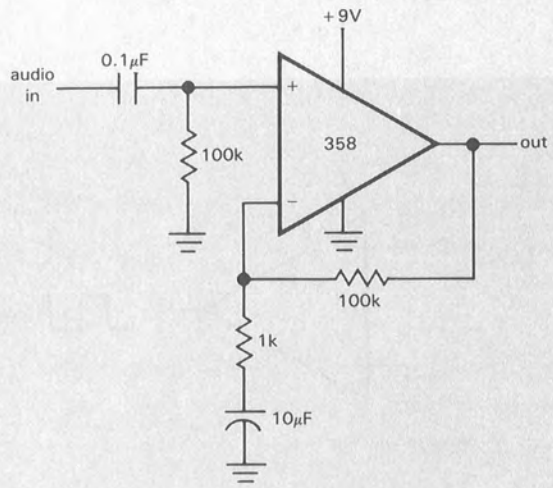
F. dc amplifier (× 100)



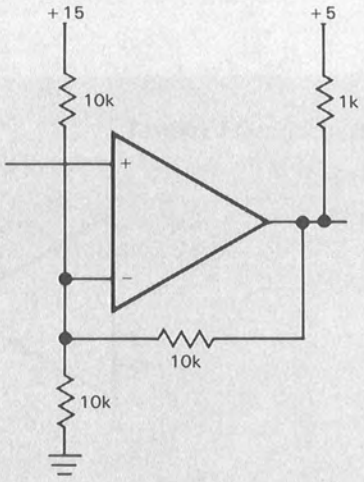
C. triangle wave-generator

Figure 4.95

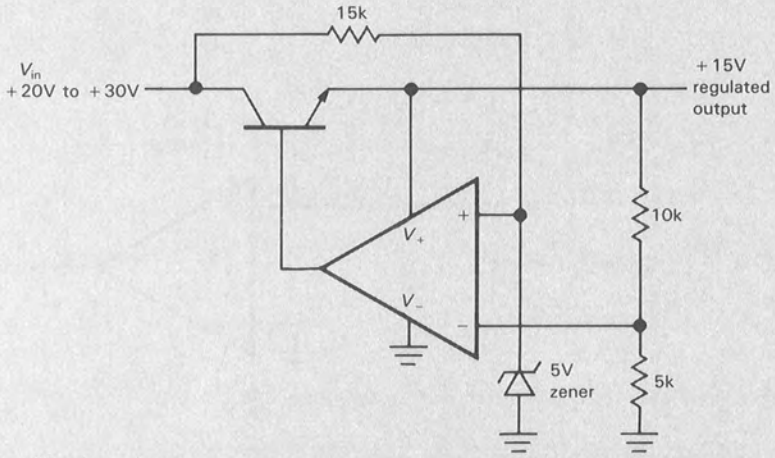
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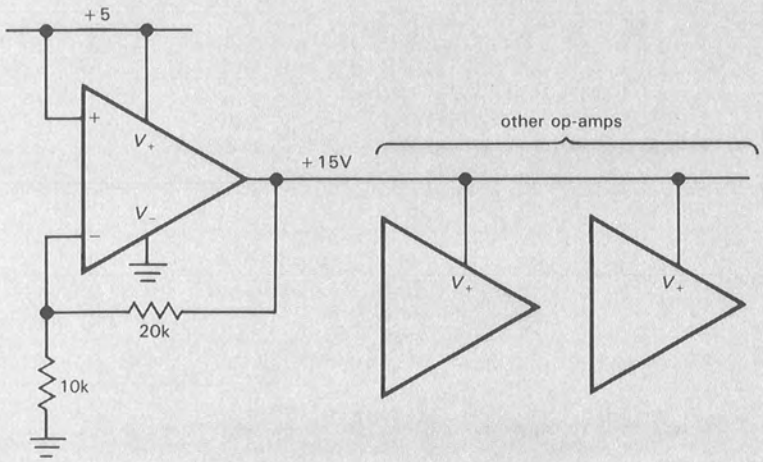
G. × 100 audio amplifier (single supply)



J. Schmitt trigger



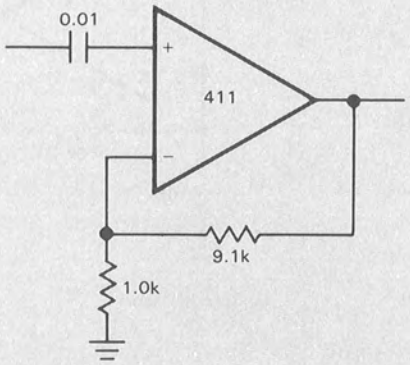
H. +15 volt regulator



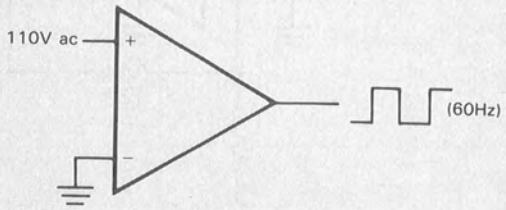
I. op-amp as +15V regulator

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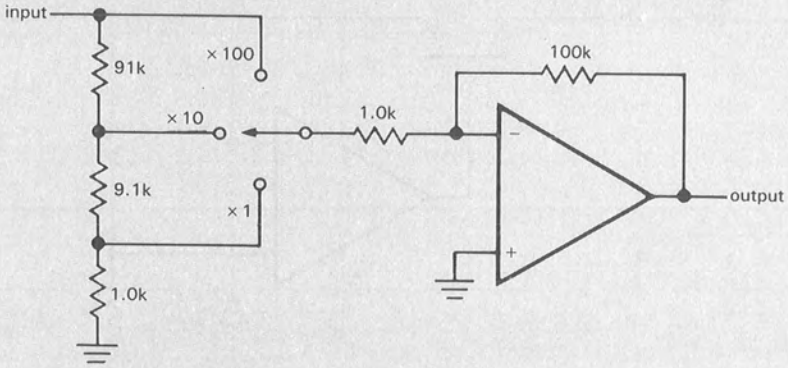
Bad circuits (*cont.*)



K. ac-coupled ×10 amplifier



M. zero-crossing detector



L. dc amplifier, selectable gains (×1 to ×100)

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