

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner

v.

BiTMICRO LLC,
Patent Owner.

IPR2023-00783
U.S. Patent No. 6,496,939

**DECLARATION OF DR. CARL SECHEN, PH.D.
IN SUPPORT OF INTER PARTES REVIEW OF U.S. 6,496,939**

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I. Introduction

1. My name is Carl Sechen, and I have been retained by Perkins Coie LLP on behalf of Intel Corporation (“Intel” or “Petitioner”), to provide this Declaration concerning technical subject matter relevant to the petition for *Inter Partes* Review (“Petition”) of U.S. Pat. No. 6,496,939 to Portman (“the ’939 patent”). It is my understanding that the ’939 patent is currently assigned to BiTMICRO LLC (“BiTMICRO” or “Patent Owner”).

2. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

3. I have reviewed and am familiar with the specification and the claims of the ’939 patent. In general, I will cite to the specification of a United States patent using the following formats: (Patent No., Col:Line Number(s)) or (Patent No., Paragraph Number(s)). For example, the citation (’939 patent, 1:1-10 (INTEL-1001)) points to the ’939 patent specification at column 1, lines 1-10. Also, for convenience, I use italics to denote limitations from the challenged claims, which are claims 1-3, 6, 10-12, and 15.

4. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, I reviewed the documents listed in the Exhibit list of Attachment A to this Declaration. I have also reviewed and am

familiar with the other materials referred to in this Declaration. To the best of my knowledge, the documents listed above are true and accurate copies of what they purport to be and are the kinds of materials that an individual with expertise in this field at the relevant time period would reasonably rely on in formulating opinions, such as those set forth in this Declaration. In citing documents below, I have added emphasis to some words and phrases. Unless stated otherwise, I added any emphasis that appears in the quotations.

5. I have been asked to provide my technical opinions regarding how a person of ordinary skill in the art (“POSITA”) would have understood the claims of the ’939 patent at the time of the alleged invention. For purposes of whether the teachings of the prior art render the claims of the ’939 patent obvious, I have been asked to use September 21, 1999, the filing date of the ’939 patent for the analysis in this Declaration. I have also been asked to provide my technical opinions on how concepts in the ’939 patent specification relate to claim limitations of the ’939 patent. In reaching the opinions provided herein, I have considered the ’939 patent, its prosecution history, and the references cited above and have drawn as appropriate on my own education, training, research, knowledge, and personal and professional experience.

A. Qualifications and Expertise

6. In formulating my opinions, I have relied on my knowledge, training, and experience in the relevant field, which I will summarize briefly. A more detailed summary of my background, education, experience, and publications is set forth in my curriculum vitae (“CV”), which is provided as exhibit INTEL-1004. My CV also includes a list of my litigation support experience.

7. I earned a B.E.E. in Electrical Engineering from the University of Minnesota in 1975, followed by a M.S. in Electrical Engineering from the Massachusetts Institute of Technology in 1977. I earned a Ph.D. in Electrical Engineering from the University of California, Berkeley in 1986.

8. I have been a Professor of Electrical Engineering for 36 years. Since August 15, 2005, I have been a Professor of Electrical and Computer Engineering at the University of Texas at Dallas. From July 1992 to August 14, 2005, I served as a Professor of Electrical Engineering at the University of Washington. From July 1986 through June 1992, I served as an Assistant Professor and then an Associate Professor of Electrical Engineering at Yale University.

9. Over the course of my academic career, my research has focused on the design and computer-aided design of digital integrated circuits, including computer architecture, and the design of dynamic random-access memory (“DRAM”) and static random-access memory (“SRAM”) modules. I also have

designed several chips that included various types of embedded DRAM (“eDRAM”). In this research work, I have designed multiple sense amplifier circuits for the various DRAMs, eDRAMs, and SRAMs. I have authored or co-authored over 200 papers and one book, the majority of which concern digital integrated circuit design and memory design.

10. During my undergraduate education at Minnesota and my master’s degree work at MIT, I fabricated multiple fully-functional semiconductor circuits. I designed and fabricated circuits comprising depletion mode transistors that included buried-channels and buried layers. I also designed and fabricated circuits comprising enhancement mode (or surface channel) transistors in this work.

11. As a professor, I have developed and taught numerous courses, including several courses that teach Very Large Scale Integration (“VLSI”) circuit design, computer architecture and memory design, as well as analog and mixed signal IC design. I have taught these courses continuously for the past 27 years. I have taught digital integrated circuit design and memory design to undergraduate and graduate students at the University of Washington and at the University of Texas at Dallas. The design and use of SRAM, DRAM and Flash memories are covered in these courses, as is the design of sense amplifier circuits for various types of memory. In these courses I teach the details of the structures and functions of computer systems and the use of digital tools to design memory circuits. Also

covered are the design of basic power management circuits. I have designed power management circuits for several research projects.

12. In 2002, I was elected a Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”) for contributions to placement and routing of application-specific integrated circuits. IEEE is the leading professional association for electrical engineers. The Board of Directors of the IEEE awards the rank of “Fellow” to individuals with an extraordinary record of accomplishments in any of the IEEE fields of interest. The total number of IEEE members who can be named Fellows in any one year cannot exceed one-tenth of one percent of the total voting IEEE membership.

13. I received several research and teaching awards during my career. I received the Semiconductor Research Corporation’s Inventor’s Recognition Award in 1988 and in 2001. I also received the Technical Excellence Award from the Semiconductor Research Corporation in 1994. While serving as a Professor at the University of Washington, I received the Outstanding Research Advisor Award from the Department of Electrical Engineering in 2002. In 2008, I received the Distinguished Teacher of the Year Award from the Department of Electrical Engineering at the University of Texas at Dallas. I also received the Distinguished Teaching Award for the Erik Johnson School of Engineering and Computer Science in 2014.

14. Over the years, I also have received extensive funding to conduct research in computer circuits and memory designs, including area-efficient and reliable eDRAM and SRAM design. Together with my graduate students, I have designed and fabricated various types of computational VLSI chips.

15. I am the lead inventor on four issued patents. Three of the patents concern extremely dense transistor-level field programmable logic.

B. Compensation

16. I am being compensated for my time in connection with this *inter partes* review (“IPR”) proceeding at my standard consulting rate of \$400 an hour. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or in any litigation involving the ’939 patent.

C. Materials Considered and Basis of Opinions

17. In forming the opinions set forth in this Declaration, I have considered and relied upon my education, experience, and knowledge of the relevant fields. I have also reviewed and considered the documents and materials cited in the body, including exhibits in the IPR such as the ’939 patent and its file history.

18. In forming the opinions set forth in this Declaration, I have considered and relied upon my education, experience, and knowledge of the relevant fields. I have also reviewed and considered the documents, schematics, and publicly available articles and books cited in the body and exhibits to this Declaration.

19. I reserve the right to supplement this Declaration and rely upon any additional information, deposition testimony, documents, or materials that may be provided to me or that are relied upon by any of Patent Owner's experts or witnesses.

20. I also reserve my right to supplement this Declaration and rely upon additional information that becomes available to me.

21. I may rely on visual aids and demonstratives to demonstrate the bases of my opinions, such as claim charts, patent drawings, excerpts from patent specifications, file histories, interrogatory responses, deposition transcripts and exhibits, as well as charts, diagrams, videos and animated or computer-generated video. The demonstrative exhibits I may use to accompany any testimony I may give may also include documents, testimony, and other evidence cited in my Declaration, portions of such evidence, and other portions of my Declaration and the attached exhibits.

D. Understanding of Relevant Legal Principles

22. I am not a lawyer and will not provide any legal opinions. Although I am not a lawyer, I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

23. I understand that a patent claim is invalid if it is anticipated or obvious in view of the prior art, and that a claim can be unpatentable even if all of the requirements of the claim cannot be found in a single prior-art reference. I further understand that invalidity of a claim requires that the claim be anticipated or obvious from the perspective of a person of ordinary skill in the art at the time the invention was made.

24. I have been informed that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art. In analyzing the obviousness of a claim, I understand the following factors may be taken into account: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art; and (4) any so called “secondary considerations” of non-obviousness if they are present. Such secondary considerations include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results

achieved by the invention as compared to the closest prior art; praise of the invention by the infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I am not aware of any evidence of secondary considerations of non-obviousness relevant to the '939 patent. I reserve the right to supplement this Declaration if Patent Owner introduces evidence of secondary considerations of non-obviousness.

25. I understand that to prove that prior art or a combination of prior art renders a patent obvious, it is necessary to:

- (1) identify the particular references that, singly or in combination, make the patent obvious;
- (2) specifically identify which elements of the patent claim appear in each of the asserted references; and
- (3) explain why a person of ordinary skill in the art would have combined the references, and how they would have done so, to create the inventions claimed in the patent. I further understand that exemplary rationales that may support a conclusion of obviousness include:
 - combining prior art elements according to known methods to yield predictable results;

- simple substitution of one known element for another to obtain predictable results;
- use of known technique(s) to improve similar devices (methods or products) in the same way;
- applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- “obvious to try” – choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a person of ordinary skill in the art; and
- some teaching, suggestion, or motivating in the prior art that would have led a person of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

26. I have been informed that, in considering obviousness, hindsight reasoning derived from the patent at issue may not be used.

II. The '939 Patent

27. The '939 patent provides “a method and system for controlling data in a computer system when the computer system loses power.” ('939 patent, Abstract (INTEL-1001).) The system described in the '939 patent “activat[es] a plurality of

super capacitors to supply power to the computing engine based upon power being removed from the computer system and reconfiguring the data in the computing engine.” (’939 patent, Abstract (INTEL-1001).) In the event of a sudden external power loss, “a user is able to correctly store large amounts of newly written and modified data from the volatile memory to the non-volatile memory” or “rapidly and irretrievably erase data from the non-volatile memory automatically.” (’939 patent, 2:32-43 (INTEL-1001).) In this section, I first provide a brief technical background of power storage for memory systems, a high-level overview of the ’939 patent, a discussion of the prosecution history of the ’939 patent, and a discussion of claim construction.

A. Technical Background

1. Computer Memory System Overview

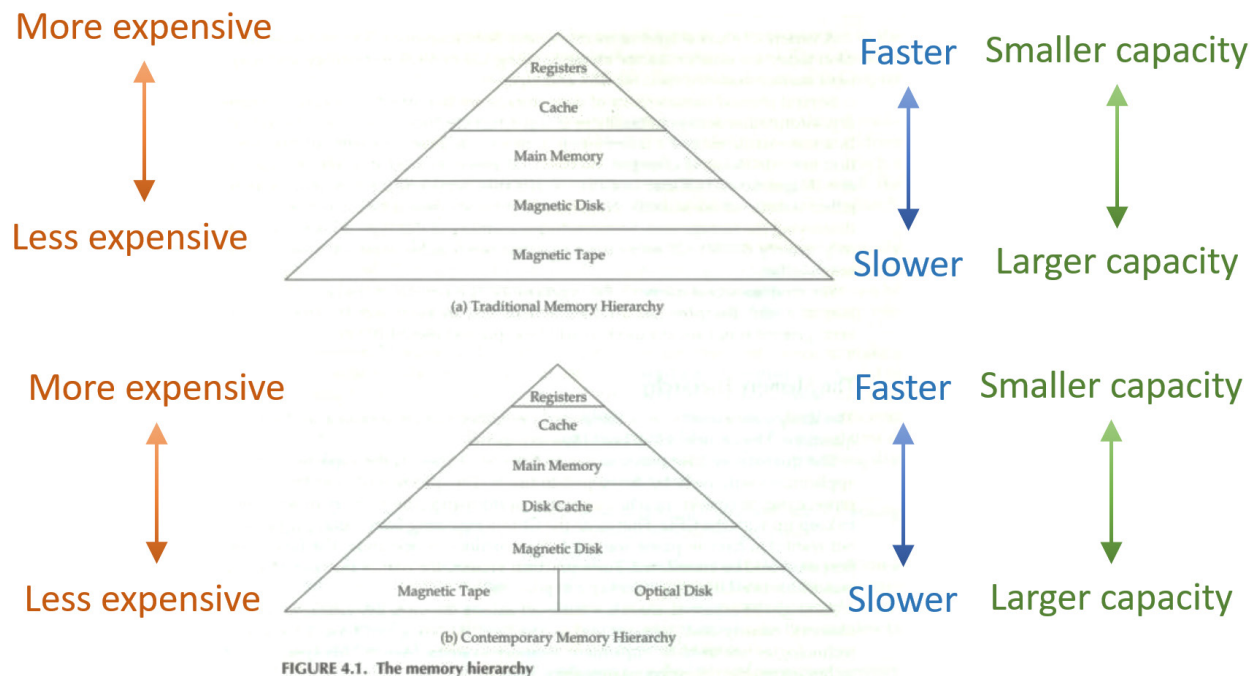
28. Computer memory is a fundamental structure of a computer system: “[a]t a top level, a computer consists of CPU, memory, and I/O components, with one or more modules of each type. These components are interconnected in some fashion to achieve the basic function of the computer, which is to execute programs.” (“Computer Organization and Architecture,” 4th Edition, 1996 by Stallings (“Stallings”), 49 (INTEL-1039).) The process of executing programs involves the CPU executing “a set of instructions stored in memory.” (Stallings, 52 (INTEL-1039).) “The simplest point of view” for understanding program

execution “is to consider instruction processing as consisting of two steps: The CPU reads (**fetches**) instructions from memory one at a time, and it executes each instruction.” (Stallings, 52 (INTEL-1039) (emphasis in original).)

29. Computer memory provides both short-term and long-term data storage solutions for the computer system. For example, “[a] cache is an area of memory which serves as a temporary storage area for the device (such as computer memory or a disk drive).” (U.S. Pat. No. 5,519,831 (“Holzhammer”), 1:27-30 (INTEL-1036).) In contrast, an erasable programmable read-only memory (EPROM) “holds its data virtually indefinitely.” (Stallings, 110 (INTEL-1039).) The design process of a computer’s memory system is guided by three major considerations: storage capacity, data access speed, and cost. A memory system designer often faces a tradeoff of those factors: faster access time requires higher cost per bit, while memories with greater storage capacity tend to have slower access time. (Stallings, 103-104 (INTEL-1039).)

30. The solution is not to rely on a single type of memory, but to employ a memory hierarchy that includes a combination of different types of memory devices. As a result, the memory component of a computer system “exhibits perhaps the widest range of type, technology, organization, performance, and cost of any feature of a computer system.” (Stallings, 100 (INTEL-1039).) Fortunately, the computer does not need to access all data at the same frequency or speed.

Smaller, faster, and more expensive memories are supplemented by larger, slower, and less expensive memories to fulfill the different needs and access requests of the computer system. The figure below illustrates a typical memory hierarchy that shows different levels of memory devices in a computer system. (Stallings, 101 (INTEL-1039).) I have annotated the figure to show that “[a]s one goes down the hierarchy, the following occur: (a) decreasing cost per bit; (b) increasing storage capacity; (c) increasing access time; and (d) decreasing frequency of access of the memory by the processor.” (Stallings, 100 (INTEL-1039).)



(Stallings, 104 (INTEL-1039).)

31. One of the memories in the hierarchy is the main memory, which is “the principal internal memory system of the computer.” (Stallings, 107 (INTEL-

1039).) Main memories are often constructed using semiconductor technology.

“Today, the use of semiconductor chips for main memory is almost universal.”

(Stallings, 109 (INTEL-1039).) The table below lists some major types of semiconductor memory used in computer systems.

Memory Type	Category	Erase	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Flash memory		Electrically, block-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		

(Stallings, 109 (INTEL-1039).)

32. The most basic and essential element of a semiconductor memory is the memory cell. Each memory cell can exhibit two stable states “which can be used to represent binary 1 and 0.” (Stallings, 111 (INTEL-1039).) A memory cell is “capable of being written into (at least once), to set the state” and “being read to sense the state.” (Stallings, 111 (INTEL-1039).) To achieve the aforementioned functionality, a memory cell is usually equipped with “three functional terminals capable of carrying an electrical signal,” including (i) a select terminal that “selects a memory cell for a read or write operation”; (ii) a control terminal that “indicates read or write”; and (iii) a data terminal that sets the state of the cell during a

writing operation or sensing the state of the cell during a reading operation.

(Stallings, 111 (INTEL-1039).) The figure below is an abstract illustration that depicts the operation of a memory cell.

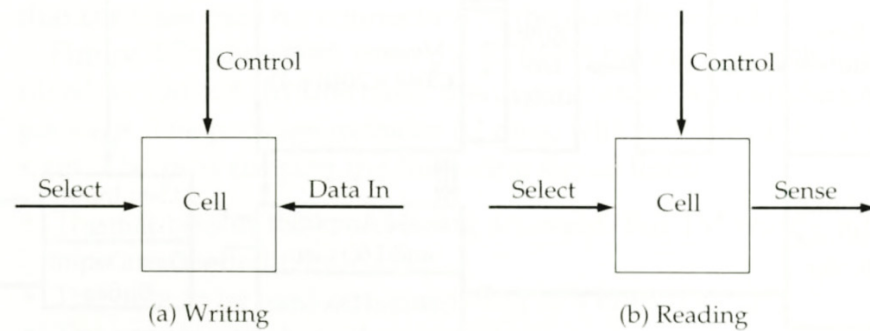


FIGURE 4.5. Memory cell operation

(Stallings, 111 (INTEL-1039).)

33. Memory devices **require an electrical power supply** to perform these operations. For example, “both the reading and writing are accomplished through the use of electrical signals.” (Stallings, 109 (INTEL-1039).) Based on whether a memory device retains data when power is removed, memory devices can be largely divided into two types: volatile memory devices and non-volatile memory devices.

2. Types of Semiconductor Memory

a) Volatile Memory

34. Volatile memory devices must receive continuous electrical power supply to maintain the information stored in their memory cells and would “lose stored data if the power supplying the computer is interrupted, even momentarily.”

(U.S. Pat. No. 4,559,616 (“Bruder”), 1:23-25 (INTEL-1034).). Volatile memory devices are vital components of a computer system and used as “a temporary storage”. (Stallings, 109 (INTEL-1039).) “All computers have some fast random-access memory called RAM.... RAM is always *volatile*, which means that its information evaporates when power is removed.” (“The Art of Electronics,” 2nd Edition, 1989 by Horowitz, et al. (“Horowitz”), 675 (INTEL-1037).) Specifically, the bit content in a volatile RAM device is “typically lost whether electric power to the RAM is momentarily interrupted, fluctuates, or is lost.” (U.S. Pat. No. 5,608,684 (“Reasoner”), 1:15-20 (INTEL-1030).)

35. The two forms of RAM commonly used in computers are DRAM and SRAM. DRAM and SRAM devices utilize different circuit configurations that make them best suited for different data-storing applications. In general, DRAM has nearly an order of magnitude more cells per unit area and is “less expensive than a corresponding static RAM,” and on the other hand, “static RAMs are generally somewhat faster than DRAMs.” (Stallings, 110 (INTEL-1039).)

b) Non-Volatile Memory

36. Non-volatile memory devices are read and write accessible memory devices that retain information even when the power supply is lost. (U.S. Pat. No. 4,974,167 (“Anderson”), 1:23-28 (INTEL-1031).)

37. Some non-volatile memory is read-only memory (“ROM”) that contains a “permanent pattern of data that cannot be changed.” (Stallings, 110 (INTEL-1039).) Data is wired into these types of ROM devices either during chip fabrication or later using special equipment, and “it is not possible to write new data into it.” (Stallings, 110 (INTEL-1039).) While there are many applications suitable for ROM devices (e.g., micro-programming), non-volatile memory devices with the capability of being written into without using special equipment are versatile and can be “useful for applications in which read operations are far more frequent than write operations but for which nonvolatile storage is required.” (Stallings, 110 (INTEL-1039).)

38. Non-volatile memory devices that have the capability of being written into multiple times are referred to as “read-mostly memory.” (Stallings, 110 (INTEL-1039).) “There are three common forms of read-mostly memory: EPROM, EEPROM, and flash memory.” (Stallings, 110 (INTEL-1039).)

39. “[E]rasable programmable read-only memory (EPROM) is read and written electrically.” (Stallings, 110 (INTEL-1039).) EPROM requires that “storage cells must be erased to the same initial state” before a write operation can be performed. (Stallings, 110 (INTEL-1039).) “This erasure process can be performed repeatedly.” (Stallings, 110 (INTEL-1039).)

40. Electrically erasable programmable read-only memory (“EEPROM”) has the advantage over EPROM due to the capability of being “written into at any time without erasing prior contents.” (Stallings, 110-111 (INTEL-1039).)

41. Flash memory was “[f]irst introduced in the mid-1980s” and “is intermediate between EPROM and EEPROM in both cost and functionality.” (Stallings, 111 (INTEL-1039).) Flash memory got its name because of “the speed with which it can be reprogrammed.” (Stallings, 111 (INTEL-1039).) The erasure operation can be completed “in one or a few seconds, which is much faster than EPROM.” (Stallings, 111 (INTEL-1039).)

3. Protecting Data During a Power Outage

42. Problems in the power supply, such as power fluctuations and power interruptions, can cause errors in data stored in volatile memory devices. These errors are often referred to as soft errors: “[a] soft error is a random, non-destructive event that alters the contents of one or more memory cells, without damaging the memory. **Soft errors can be caused by power supply problems** or alpha particles.” (Stallings, 116 (INTEL-1039).)

43. Vital information in volatile memories may be destroyed due to lost or corrupt data caused by problems in the power supply. To prevent such a catastrophic outcome, it was well known to equip computer systems with “memory backup” capabilities that enable the computer to transfer data from volatile

memories to non-volatile memories upon detecting a power interruption. The following paragraphs describe several examples of patents and patent application publications that were published before September 1999 and described computer systems with memory backup capabilities.

44. Japanese Patent Application Publication No. JPH05-108505 (“Nishida”) was published on April 30, 1993 and “relates to computer systems with memory backup functions.” (Nishida, ¶1 (INTEL-1006).) Nishida’s computer system includes “a CPU, a volatile main recording memory, a non-volatile external recording device.” (Nishida, claim 1 (INTEL-1006).) In the event of a power outage, **“the data on the main memory is urgently transferred to a non-volatile external recording device** using the power supply for the backup to protect data.” (Nishida, ¶2 (INTEL-1006); *see also* ¶¶3, 4, 15.)

45. U.S. Pat. No. 4,965,828 (“Ergott”) was issued on October 23, 1990 and described “a system that utilizes a volatile SRAM and a non-volatile backup store implemented by means of E²PROMs in which **data is transferred from the SRAMs to the E²PROMs when the power is turned off or interrupted** by using high voltage energy stored in a backup capacitor to provide operating power for at least a long enough period of time to effectuate reliable transfer of data from the SRAM to the E²PROM.” (Ergott, 3:2-10 (INTEL-1008).)

46. Bruder was issued on December 17, 1985 and described a memory system that includes a semiconductor volatile RAM memory and a non-volatile memory for backing up the volatile memory. (Bruder, Abstract (INTEL-1034).) Whenever there is a power failure, “the entire contents of CMOS 41 [the volatile memory] is transferred to non-volatile bubble memory 42.” (Bruder, 7:57-60 (INTEL-1034).)

47. U.S. Pat. No. 4,327,410 (“Patel”) was issued on April 27, 1982 and described financial terminals that include a “system for preserving data associated with a memory unit.” (Patel, Abstract (INTEL-1035).) When normal operation power is available, the volatile RAM memory stores Terminal Processor (TP) data such as “teller totals, accumulators, transaction counters, supervisory codes, and terminal sign-in information.” (Patel, 4: 21-40 (INTEL-1035).) When there is an impending power failure, **the data in the volatile RAM memory is transferred to the non-volatile memory.** (Patel, 4: 21-40 (INTEL-1035).)

48. Holzhammer was issued on May 21, 1996 and described a method used in a computer system for saving data from a volatile cache memory during a power loss. (Holzhammer, Abstract (INTEL-1036).) Specifically, a control logic “copies the data contained in the volatile cache memory to the non-volatile memory upon detection of the power loss.” (Holzhammer, Abstract (INTEL-1036).)

4. Backup Power Supplies

49. To support data transfer during a power outage, a backup power supply is required for delivering the power needed to the volatile memory, the non-volatile memory, and/or the control circuitry that carries out the data transfer process. Common backup power supplies for computer systems at the time included batteries and capacitors, both of which contain a finite amount of stored energy. Nishida disclosed that both batteries and capacitors are options for the backup power supply: “storage batteries, supercapacitors, lithium primary batteries, etc.” (Nishida, ¶2 (INTEL-1006).) Ergott used “high voltage energy stored in a backup capacitor to provide operating power for at least a long enough period of time to effectuate reliable transfer of data from the SRAM to the E²PROM.” (Ergott, 3:7-10 (INTEL-1008).) Holzhammer relied on batteries for powering the volatile memory, the microcontroller, and the non-volatile memory “when computer system power is lost.” (Holzhammer, 5:28-47 (INTEL-1036).) The memory system in Bruder is a “bank of energy storage capacitors” that supplies “enough energy to maintain the voltage supply lines” of the volatile RAM memory, the non-volatile memory, and other circuitry “within a predetermined voltage range long enough to allow this transfer of data to be accomplished.” (Bruder, 7-60-66 (INTEL-1034).)

50. Although batteries were widely used to store electrical energy, they suffered from numerous problems, such as safety issues, maintenance costs, charging rate limitations, and the need for continuous replacements. In contrast, capacitors, especially large-capacitance capacitors, were “considered preferable to a battery for present energy storage uses for reasons of size, weight, reliability and decreased maintenance requirements, and [were] now readily available as commercial products.” (U.S. Pat. No. 5,914,542 (“Weimer”), 2:19-41 (INTEL-1032).) Commercial high-capacitance products, such as a SUPERCAP developed before September 1999 by Nippon Electric Corporation (NEC), provided backup time from “several minutes” to “several weeks,” depending on the application. (File History of Reasoner including “SUPERCAP” (Electric Double-Layer Capacitors) User’s Manual (“Supercap Manual”), 87 (INTEL-1015).)

5. Capacitors as Backup Power Supplies

a) Capacitor Fundamentals

51. Capacitors are passive electronic components that store electrical energy by virtue of accumulating electric charges on two surfaces that are insulated from each other. Capacitors are fundamental elements of electrical circuits and have been used for hundreds of years. “The beginning of capacitor technology is generally attributed to the invention in October 1745 of the Leyden jar by the German Ewald Georg von Kleist.” (“Historical Introduction to Capacitor

Technology,” IEEE Electrical Insulation Magazine, Vol. 26, Issue 1, January 2010, by Ho, et al. (“Ho”), 20 (INTEL-1041).)

52. The most general form of a capacitor includes two conductive terminals (e.g., metal plates) separated by an insulating material called a dielectric. The schematic symbol for a general capacitor is illustrated in the figure below:

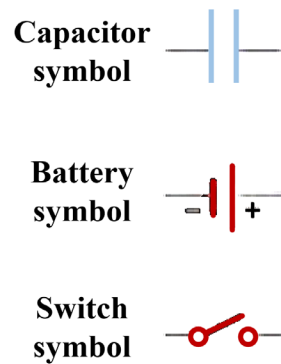


Figure 20.20 Circuit symbols for Capacitors, batteries, and switches. Note that capacitors are in blue, And batteries and switches are in red.

(“Principles of Physics,” 2nd Edition, 1998 by Serway (“Serway”), 576 (INTEL-1038).)

53. Three important characteristics of a capacitor are its capacitance (C), the amount of charge it holds (Q), and the voltage (ΔV) across the two conductive terminals of the capacitor. “The capacitance, C , of a capacitor is defined as the ratio of the magnitude of the charge on either conductor to the magnitude of the

potential difference between them.” (Serway, 573 (INTEL-1038).) The relationship between capacitance, charge, and voltage is shown in the equation below:

$$C \equiv \frac{Q}{\Delta V}$$

(Serway, 573 (INTEL-1038).)

54. “[T]he capacitance of a device is a measure of its ability to store charge and **electrical potential energy**.” (Serway, 573 (INTEL-1038).) The unit of capacitance is the farad (F). A farad is the capacitance value that allows the capacitor to store one coulomb of charge when one volt is applied across the plates of the capacitor. A farad is a very large value, so other common units of capacitance include microfarads (μF) or picofarads (pF), which equals to one millionth (10^{-6}) and one trillionth (10^{-12}) of a farad, respectively. (Serway, 573 (INTEL-1038).)

55. Multiple capacitors can be connected in parallel or in series to meet different circuitry needs. Capacitors are connected in parallel when both of its terminals are connected to each terminal of another capacitor, as illustrated by capacitors C_1 and C_2 in the figure below:

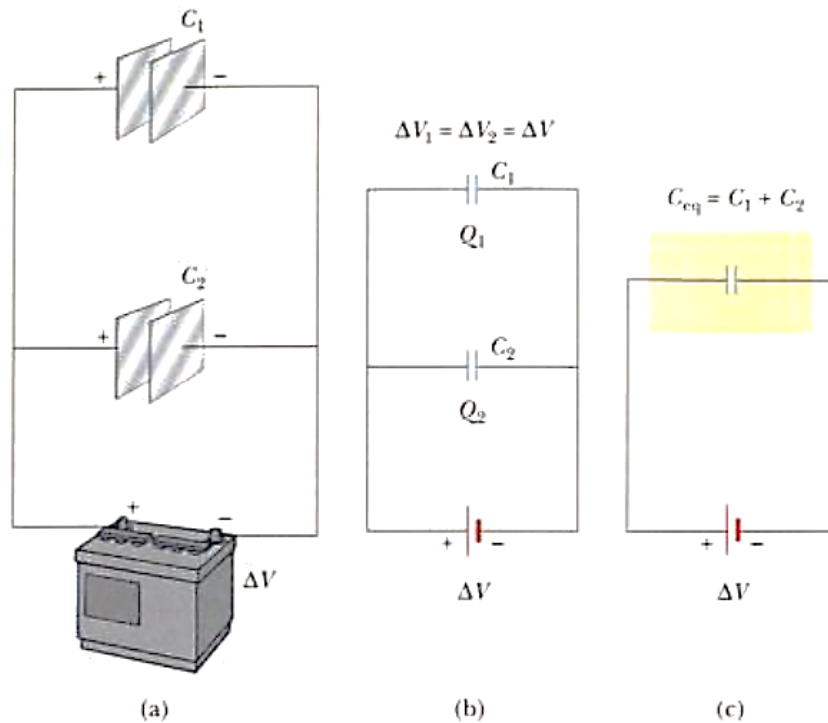


Figure 20.21 (a) A parallel combination of two capacitors. (b) The circuit diagram for the parallel combination. (c) The potential difference is the same across each capacitor, and the equivalent capacitance is $C_{eq} = C_1 + C_2$.

(Serway, 577 (INTEL-1038).)

56. The equivalent capacitance for capacitors connected in parallel is the sum of their individual capacitance, as stated in the description within the figure above. In addition, “[i]f we extend this treatment to three or more capacitors connected in parallel, the equivalent capacitance is $C_{eq} = C_1 + C_2 + C_3 + \dots$ ” (Serway, 577 (INTEL-1038).) Therefore, capacitors are connected in parallel to achieve a higher total capacitance, which in turn provides longer backup times: [w]hen higher rated voltage or greater capacitance (i.e., longer backup time) is

required, it can be obtained by connecting SUPERCAP in series or in parallel respectively.” (Supercap Manual, 98 (INTEL-1015).)

57. On the other hand, capacitors are connected in series when they are daisy chained together in a single line, as illustrated by capacitors C_1 and C_2 in the figure below:

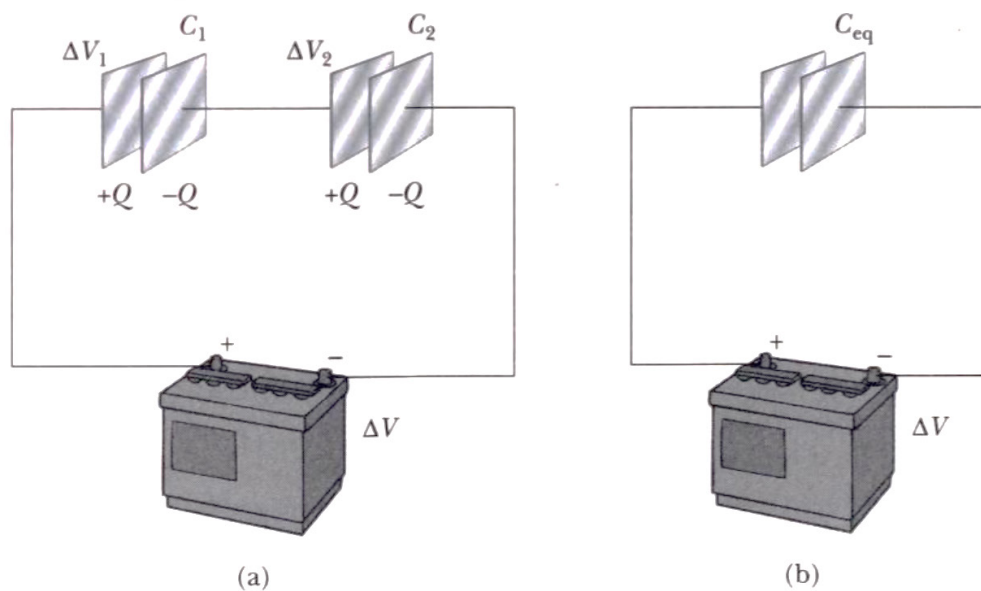


Figure 20.22 A series combination of two capacitors. The charge on each capacitor is the same, and the equivalent capacitance can be calculated from the relationship $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$.

(Serway, 578 (INTEL-1038).)

58. For three or more capacitors connected in series, the equivalent capacitance is:

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \dots$$

(Serway, 579 (INTEL-1038).)

59. In a fully discharged state, the two conductor plates of the capacitor are electrically neutral because there are as many positive as negative charges on each of the two plates. The equation $C = Q/\Delta V$ discussed in ¶53 can be rearranged into $\Delta V = Q/C$. According to the equation $\Delta V = Q/C$, the capacitor voltage is directly proportional to the charge stored. Therefore, the voltage across the two conductor plates is zero when the capacitor is fully discharged.

60. I will use the parallel combination of capacitors discussed in ¶55 as an example to describe the capacitor charging process. The parallel combination of capacitors is illustrated again below:

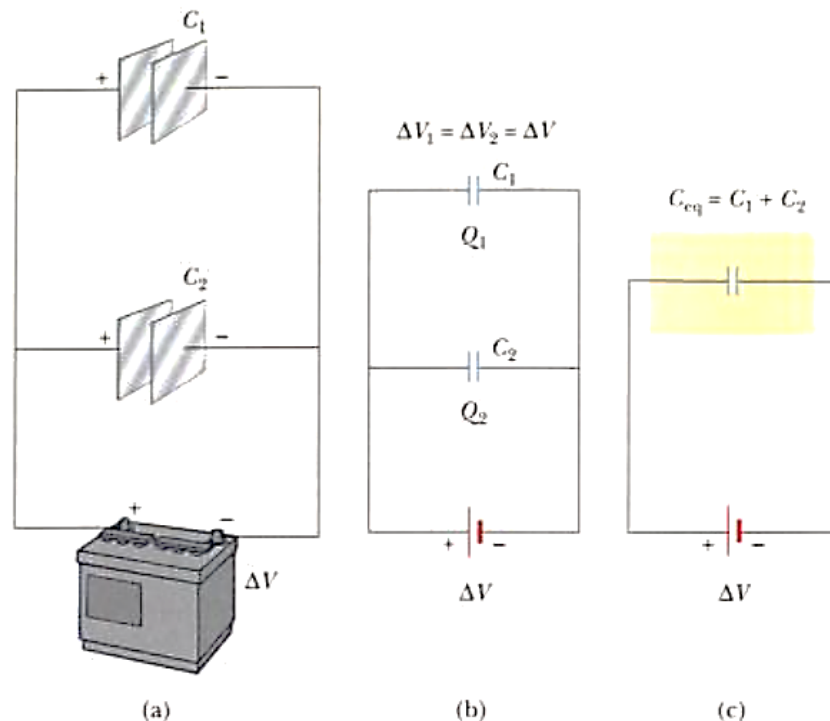


Figure 20.21 (a) A parallel combination of two capacitors. (b) The circuit diagram for the parallel combination. (c) The potential difference is the same across each capacitor, and the equivalent capacitance is $C_{eq} = C_1 + C_2$.

(Serway, 577 (INTEL-1038).) “When the capacitors are first connected in the circuit, electrons are transferred through the battery from the left plates to the right plates, leaving the left plates positively charged and the right plates negatively charged. The energy source for this charge transfer is the internal chemical energy stored in the battery, which is converted to electric potential energy. The flow of charge ceases when the voltage across the capacitors is equal to that of the battery.” (Serway, 576 (INTEL-1038).)

61. In the example shown in the figure below, the charging circuit includes a battery (with output voltage V_i) connected in series to a resistor (with resistance R) and a capacitor (with capacitance C).

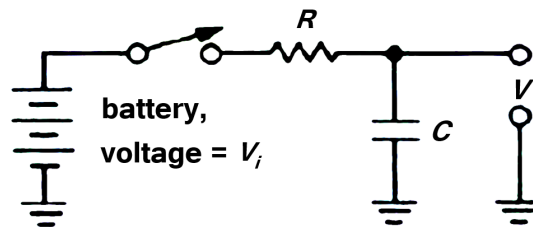


Figure 1.31

(Horowitz, 23 (INTEL-1037).) The voltage of the capacitor verses time during the charging process obeys the following equation:

$$V = V_i(1 - e^{-\frac{t}{RC}})$$

(Horowitz, 23 (INTEL-1037).) According to the above equation the voltage across the capacitor does not rise in a linear fashion during the charging process. Rather,

it is said to rise in an exponential fashion. This can be visualized using the capacitor voltage verses time diagram below:

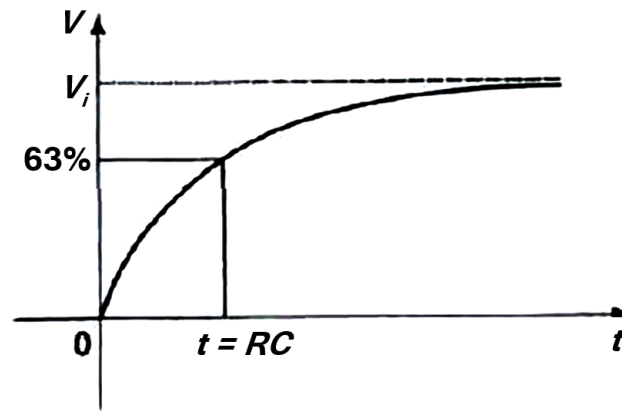


Figure 1.32

(Horowitz, 24 (INTEL-1037).) Because very few of the charges can cross between the plates, the capacitor will remain in the charged state even if the battery is removed.

62. If a conductor or a load is placed across the plates, electrons will find a path back to the positively charged plate through the conductor and the load, and eventually the charges will be neutralized again. This process is referred to as a capacitor discharging process.

63. The equation discussed in ¶59 illustrates that the capacitor voltage is directly proportional to the capacitor charges. Therefore, as the amount of charges on the capacitor plates decrease during the discharging process, the voltage across the capacitor also decreases. We can use a simple resistor-capacitor (RC) circuit to

analyze the voltage behavior of the capacitor during the discharge process. The RC circuit consists of a resistor connected in parallel with a charged capacitor, as shown in the figure below:

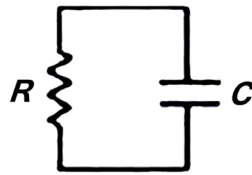


Figure 1.29

(Horowitz, 23, 24 (INTEL-1037).)

64. When a charged capacitor C is inserted into the circuitry above, the voltage drop across the capacitor verses time is illustrated in the graph below:

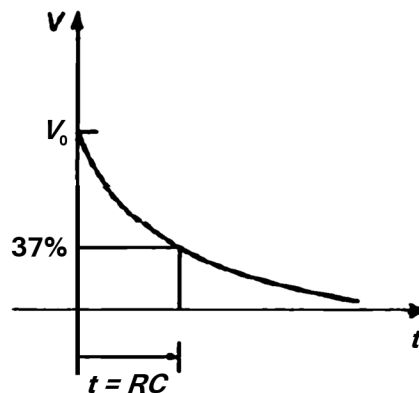


Figure 1.30. RC discharge waveform.

(Horowitz, 23 (INTEL-1037).) As seen from the graph above, the capacitor voltage gradually decreases in a non-linear (decreasing exponential) fashion. “The product RC is called the time constant of the circuit.” (Horowitz, 23 (INTEL-1037) (emphasis in original).) The larger the resistance, the greater the RC value and the

longer it takes for the capacitor to discharge. The energy stored in the capacitor eventually dissipates through the resistor.

65. As briefly discussed in ¶¶53 and 59, “the capacitance of a device is a measure of its ability to store charge and electrical potential energy.” (Serway, 573 (INTEL-1038).) The energy (U) stored in a capacitor is represented by the following equation:

$$U = \frac{Q^2}{2C} = \frac{1}{2} Q \Delta V = \frac{1}{2} C (\Delta V)^2$$

“This [equation] applies to **any** capacitor, regardless of its geometry.” (Serway, 581 (INTEL-1038) (emphasis in original).) The equation above indicates that energy stored in a capacitor is directionally proportional to the square of the voltage across the capacitor. Therefore, as seen from the equation above, there are two ways to increase the energy (U) stored in the capacitor: increase the capacitor voltage (ΔV) and/or increase the capacitance value (C).

66. Since the stored energy is directionally proportional to the square of the voltage across the capacitor, the above equation indicates that increasing the capacitor voltage will result in exponential increase in stored energy. For example, doubling the capacitor voltage can lead to a four-fold increase in the stored energy. Therefore, many circuits incorporating capacitors as backup power supplies also implemented voltage-up converters to increase the capacitor charging voltage and

voltage-down converters to reduce the capacitor supply voltage level to a suitable level for the circuitry components. Here are a few examples of patents issued before the September 1999 filing date of the '939 patent that describe using voltage-up and voltage-down converters in conjunction with capacitor backup power supplies:

67. Ergott used “**high voltage energy stored in a backup capacitor** to provide operating power for at least a long enough period of time to effectuate reliable transfer of data from the SRAM to the E²PROM.” (Ergott, 3:6-10 (INTEL-1008).) Ergott’s **up-converter “boost[s]” an external power supply** of five volts to charge up “backup capacitor 43 to approximately 100 volts.” (Ergott, 6:62-68 (INTEL-1008).) After a power interruption, “voltage down converter circuit discharge[s] current from the backup capacitor to supply the internal power supply voltage.” (Ergott, Claim 2 (INTEL-1008).)

68. Bruder utilized a high voltage capacitor bank to provide backup power for the memory devices and control circuitry. “[T]emporary power is supplied to the CMOS memory and to the bubble memory system, and also to a low power control circuit **by means of a high voltage capacitor bank** which is gradually discharged into a down voltage converter that produces a constant, regulated output voltage to the control circuitry, the CMOS memory, and the bubble memory system.” (Bruder, 2:35-42 (INTEL-1034).) Bruder incorporated “[a] **“voltage up”**

converter circuit 51 [to] boost[] the normal operating voltage on main power bus 52 to produce the 100 volts needed to charge up capacitor bank 49 and thereby store enough energy in case of a power failure.” (Bruder, 8:31-34 (INTEL-1034).) When there is a power interruption on the main power supply line, “the voltage and energy stored on the capacitors in capacitor bank 49 is coupled by means of conductor 48 to voltage down converter circuit 47. **Voltage down converter circuit 47 maintains the proper operating voltages** on conductors 45 and 46 to permit complete transfer of data in CMOS RAM 41 to bubble memory 42.” (Bruder, 8:4-10 (INTEL-1034).)

69. Another way to increase energy stored in the capacitor is to increase the capacitance of the capacitors. One example of large-capacitance capacitors is the electric double-layer capacitors, which were patented by General Electric in 1957 and commercialized in the late 1970s. (Ho, 21 (INTEL-1041).) These double-layer capacitors were used as battery substitutes to provide backup power in computer systems, as further described below.

b) Super-capacitors

70. Since the electric double-layer capacitor was patented by General Electric in 1957, double-layer capacitor designs were subsequently developed and patented by other companies as well, such as Standard Oil of Ohio. (Ho, 22 (INTEL-1041).) This led to the commercial product introduction in 1978 by

Nippon Electric Corporation (“NEC”). (Ho, 22 (INTEL-1041).) NEC’s products were called “Supercapacitors” or “SUPERCAP” and had capacitance values up to 1F, which is orders of magnitude greater than typical capacitors used in circuits. These super-capacitors “were used as battery substitutes to provide backup power for volatile CMOS computer memory.” (Ho, 22 (INTEL-1041).) Typical applications for NEC’s SUPERCAP products include being used as backup power for CMOS Microcomputers and CMOS RAMS, among others:

Typical Applications for SUPERCAP

FUNCTIONS	BACKUP CURRENT	APPLICATIONS	EQUIPMENT	ADEQUATE SERIES
Large current supply	Up to 1 A	Actuator applications (Large current in a short period)	Actuators Relay/Solenoid starter Igniters	FA and FE Series
		Primary power supply for LED displays, toys, electric buzzer etc.	Handheld toys Displays, Smoke detectors, Alarm devices, Emergency display	
Medium capacity power supply	Up to 50 mA	Secondary power source for undesirable voltage drops	Car radio back-up at the engine start, etc.	FS Series 3.5 V-6.5 V Series (FSH)
		Motor Start	VCR, Video disk Record player	
Power backup for primary power outages	Less than 500 μ A	CMOS Microcomputers	Phones (Memory dial, Auto-answering) Electric cash registers Electric typewriters Computer terminals Automatic measuring instruments etc.	FY Series (FYD Type) (FYH Type) (FYL Type) 3.5 V-6.5 V Series (FYD) FM Series
		CMOS RAMs ICs for Clocks	Digital tuning audio system (LW-MW-FM Radio, Car Radio, Stereo, etc.) Programmable consumer electronic products (VCR, Microwave oven, Games, etc.)	
		- CMOS RAMs ICs for Clocks - High operating temperature (85 °C)	Measuring instruments Automatic control Communications Car	FR Series
(Other Possible Applications) Programmable thermostat, Medical Electronics, Copiers, Vending machines, Automatic Electricity Counters, Traffic signals, Taxi Meters, Fuel Management Systems, Process Monitoring or Control, Satellite Communications, Military Electronics, Avionics, Intercom, Portable "Battery" Operated Equipment, Fare collection System, POS Terminals, Mail Sorters, Scale, Flow metering, Electronic Slot Machines, Water Heat Controllers.				

((Supercap Manual, 97 (INTEL-1015).))

71. The capacitors developed by NEC were widely used in the industry (as I will discuss later in this section) and often referred to as super-capacitors.

72. Using super-capacitors as backup power supplies offered several advantages, especially compared to nonrechargeable and rechargeable batteries. First, rechargeable batteries “must have a controlled charge rate to limit current to [the] battery, and must be periodically replaced.” (Supercap Manual, 63 (INTEL-1015).) Using nonrechargeable batteries “may be risky since there is no way to determine how much charge is still available to handle a power outage of unknown duration.” (Supercap Manual, 63 (INTEL-1015).) Second, the super-capacitors offered wider operating temperature range (e.g., from -40°C to $+85^{\circ}\text{C}$) than their battery counterparts. (Supercap Manual, 65 (INTEL-1015).) Third, super-capacitors have no problem with how fast or frequent charging/discharging is conducted. For example, unlike nickel-cadmium rechargeable batteries, supercapacitors do not need to avoid troublesome charging conditions. (Supercap Manual, 65 (INTEL-1015).)

73. Super-capacitors were widely used as backup power supplies in computer systems before the September 1999 filing date of the '939 patent. Here are a few examples of patents issued before the September 1999 filing date of the

'939 patent that describe using super-capacitors, including NEC's super-capacitors, as backup power supply in computer and memory systems:

74. Reasoner was issued on March 4, 1997 and described “a system and method for permanently backing up RAM memory devices.” (Reasoner, 3:44-45 (INTEL-1030).) “In the preferred embodiment of the present invention, capacitor 112 is a **0.22F SUPERCAP, available from NEC Electronics, Inc., Mountain View, Calif., U.S.A.** Due to its large capacity of 0.22F, capacitor 112 has a discharge time of a minimum of 10 days when supplying power to CMOS RAM 116.” (Reasoner, 5:18-23 (INTEL-1030).) In fact, the specification of Reasoner explicitly stated that “[f]urther details regarding the NEC SUPERCAP capacitor 112 may be found in **SUPERCAP User Manual**, Document No. DEP-10046 (also available from NEC Electronics, Inc., Mountain View, Calif., U.S.A.), herein incorporated by reference in its entirety.” (Reasoner, 5:26-30 (INTEL-1030).)

75. U.S. Pat. No. 5,444,378 (“Rogers”) was issued on August 22, 1995 and described a charge monitoring circuit with “a large capacitance element having the capability to store charge for long periods of time, so that the integration can be performed along the same curve even if power to the integrating circuit is interrupted during continuous or intermittent use.” (Rogers, Abstract (INTEL-1033).) “The large capacitance device C1 is preferably a **super capacitor, for example, product number FYHOH105Z manufactured by NEC Corporation,**

which is capable of storing a charge for up to three years.” (Rogers, 6:12-16 (INTEL-1033).)

76. U.S. Pat. No. 5,959,926 (“Jones”) was issued on September 28, 1999 and filed on April 13, 1998. The patent described “large capacitors” that were known as “super caps.” (Jones, 4:56-59 (INTEL-1045); *see also* 10:23-27.) Jones further taught using a “super capacitor” as a “second power source.” (Jones, 9:59-62 (INTEL-1045); *see also* 3:43-36.) “Super caps” were an example of a “rechargeable energy source ... to be used for a backup supply.” (Jones, 13:62-67 (INTEL-1045).)

6. Power Monitoring and Management Circuitry

a) Voltage Detection Circuitry

77. Computer systems with memory backup functions can include circuitry components that monitor power levels of the main and backup power supplies, such that certain operations (e.g., transferring data from volatile to non-volatile memories) are initiated when the computer system detects a power interruption.

78. For example, Nishida’s computer system with memory backup functions includes “**power supply monitoring means 107 [that] constantly monitors the supply voltage of the external power supply 106.**” (Nishida, ¶3 (INTEL-1006).) “[W]hen this supply voltage deviates from a predetermined range”

the power supply monitoring means “instructs the transfer means 109 to transfer the contents of main recording memory 102 to external recording device 103.” (Nishida, ¶3 (INTEL-1006).) Nishida also includes means for monitoring the power levels of the backup power supply. For example, Nishida’s “computer system comprises a power amount monitoring means 114 that **monitors the amount of power that can be supplied from the storage battery 110.**” (Nishida, Summary (INTEL-1006).)

79. As another example, Ergott disclosed a “[c]omparator 93 [that] generates a ‘Input Power Okay’ signal $\bar{P}_{INOK}$ on conductor 94 by **sensing the input supply voltage** on conductor 10 by means of a resistive divider circuit that applies a voltage to the non-inverting input of comparator 93.” (Ergott, 8:11-17 (INTEL-1008).) Ergott further disclosed that “[t]he **energy stored in the backup capacitor is monitored**, and at a time when just enough energy plus a safety factor remains to download all of the data from the SRAM to the E²PROM, a controller effectuates downloading of all the data in the SRAM to the E²PROM backup memory.” (Ergott, 3:16-21 (INTEL-1008).)

b) Power Distribution Circuitry

80. Computer systems may also include devices that control the distribution of power within the system.

81. Nishida's computer system includes a switch that connects either the main power supply or the backup power supply to the computer system: Nishida's power switching switch "switches the supply of power" to the computer unit "between the external power supply 106 and the storage battery 110." (Nishida, ¶3 (INTEL-1006).) "If the supply voltage of the external power supply 106 deviates from a predetermined range, the power supply monitoring means 107 **immediately switches the power switching switch 108 to the storage battery 110**, and this computer system is operated by power from the storage battery 110." (Nishida, ¶4 (INTEL-1006).)

B. '939 Patent Summary

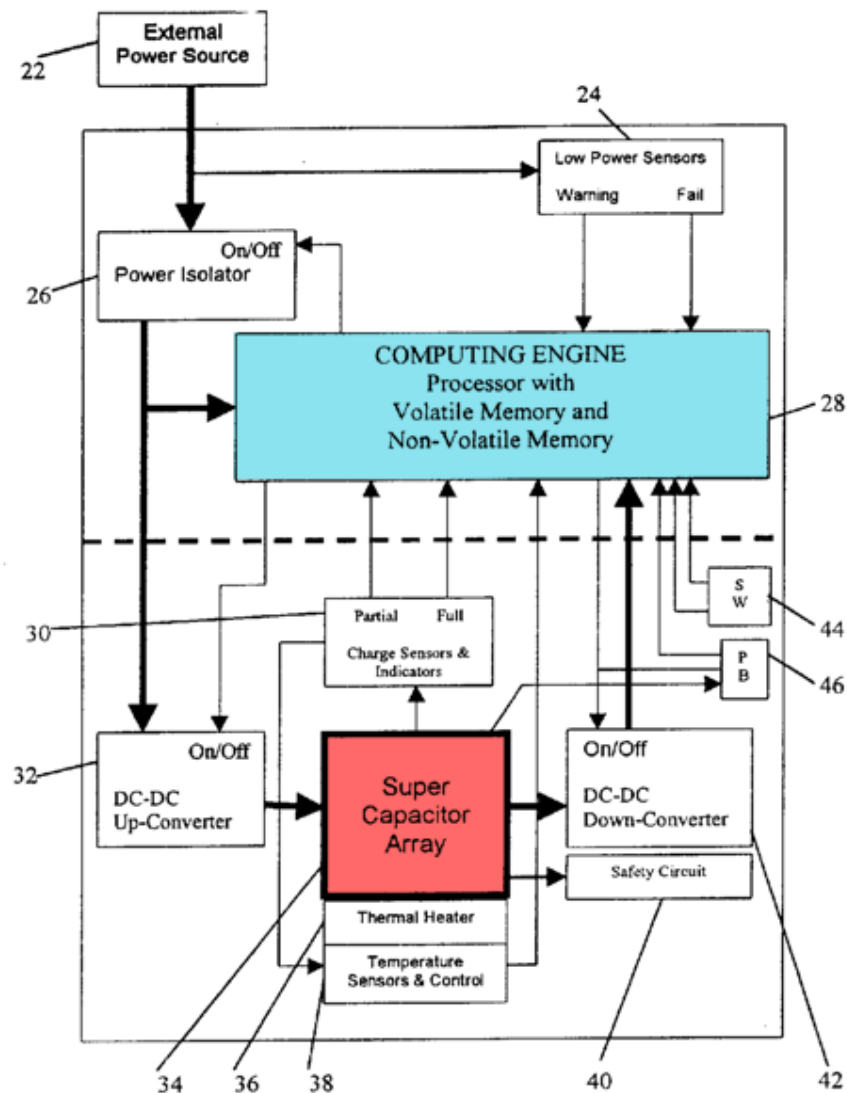
1. Overview of the Specification

82. The '939 patent is directed to "[a] method and system for controlling data in a computer system when the computer system loses power." ('939 patent, Abstract (INTEL-1001).) According to the specification, "a user is able to correctly store large amounts of newly written and modified data from the volatile memory to the non-volatile memory in the event of a sudden external power loss." ('939 patent, 2:33-37 (INTEL-1001).)

83. The system described in the '939 patent includes a "computing engine CE 28 containing the processor, volatile and non-volatile memory." ('939 patent, 3:33-34 (INTEL-1001).) When external power is available, the computing engine

CE 28 receives “power from the external power source EPS 22.” (’939 patent, 3:33-34 (INTEL-1001).) When external power is removed from the computer system, “a plurality of super capacitors [are activated] to supply power to the computing engine.” (’939 patent, Abstract (INTEL-1001).)

84. I have annotated Figure 1 of the ’939 patent to show “super-capacitors SC 34” in red and “computing engine CE 28” in blue.



2. The '939 Patent's Modes of Operation

a) Save Mode

85. The '939 patent describes a save mode in which “all data is automatically transferred from volatile memory to the non-volatile memory in the event of a sudden power loss from the external power source.” ('939 patent, 4:37-41 (INTEL-1001).) “If a system is in ‘save mode’ and is subsequently subjected to a sudden power loss, first, the super-capacitors are activated to maintain the internal power of the system, via step 50. **Finally, data from the volatile memory is transferred to the non-volatile memory, via step 52.**” ('939 patent, 5:6-13 (INTEL-1001).) The save mode is illustrated by Figure 2 of the '939 patent, which I have reproduced below:

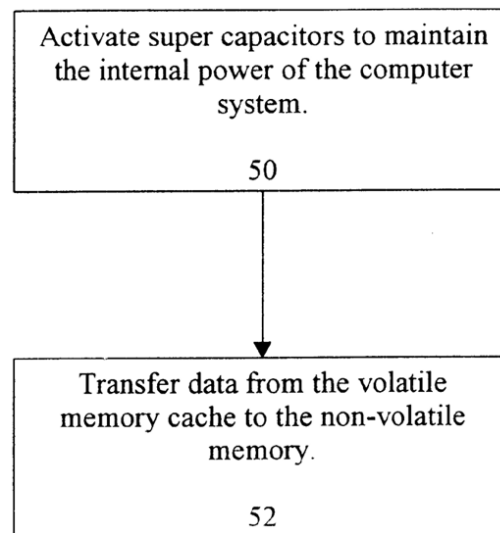


FIGURE 2

b) Erase Mode

86. The '939 patent also describes an erase mode in which the computer system “securely erase[s] all data even in event of a sudden power loss.” ('939 patent, 5:65-67 (INTEL-1001).) The '939 patent’s purported method and system “has the ability to irretrievably erase the entire contents of a large non-volatile memory hundreds of times faster than a conventional rotational hard disk drive.” ('939 patent, 6:1-4 (INTEL-1001).) When the system is subjected to a sudden power loss, “the super-capacitors are activated to maintain the internal power of the system” and “an erase command is executed until completed.” ('939 patent, 6:9-15 (INTEL-1001).) The erase mode is illustrated by Figure 4 of the '939 patent, which I have reproduced below:

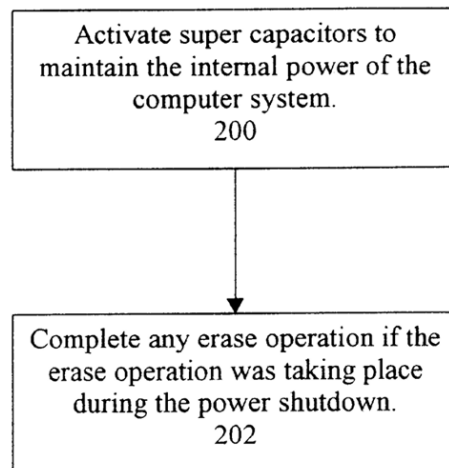


FIGURE 4

c) Standby Mode

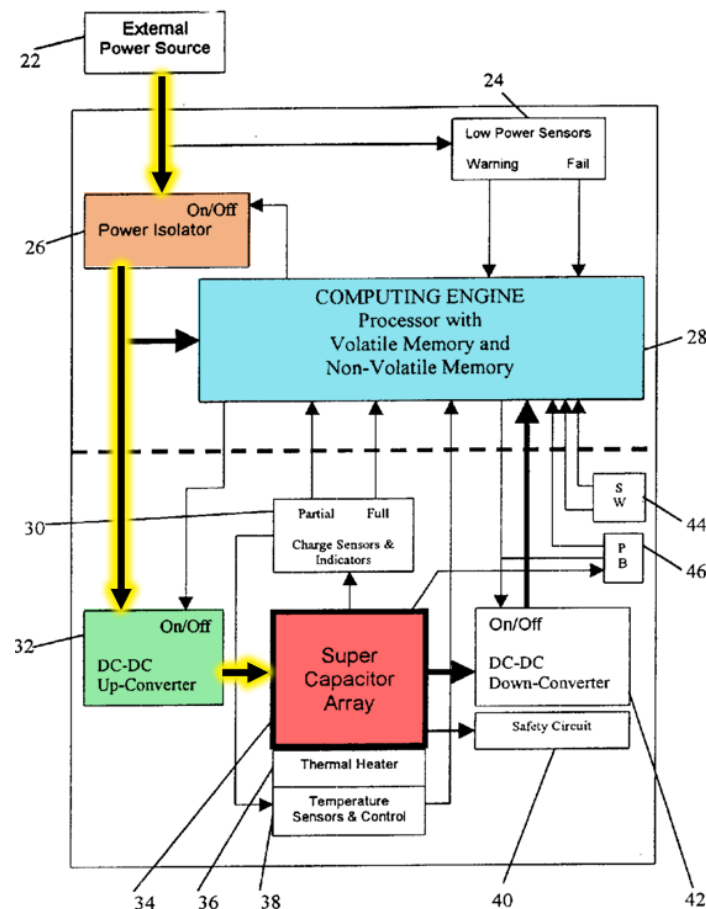
87. The '939 patent also describes a “‘standby mode’ which provides the ability to erase data manually while the system is removed from the system.” ('939 patent, 6:54-57 (INTEL-1001).) Specifically, “if a system containing sensitive data is being transported, the erase command can be activated by depressing the external pushbutton connected to the system, at which time the system will be powered up and the entire contents of the non-volatile memory will be rapidly and irretrievably erased.” ('939 patent, 6:61-67 (INTEL-1001).)

3. The '939 Patent's Backup Power Supply Structure

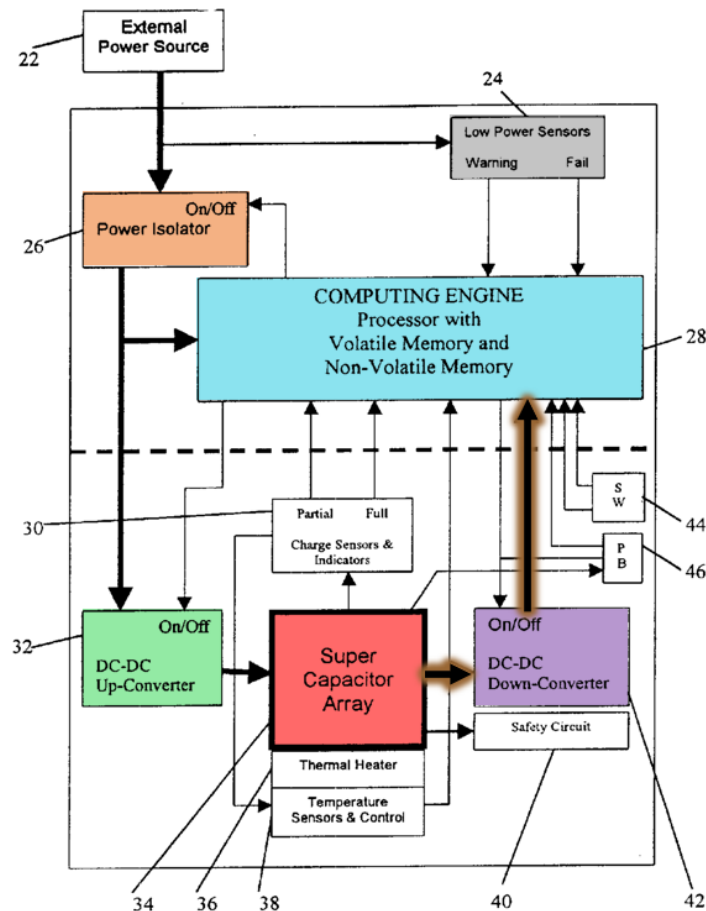
88. The '939 patent incorporates “super-capacitors as a short term power source.” ('939 patent, 3:3-5 (INTEL-1001).) The '939 patent acknowledges that “[w]ith the advent of low cost super-capacitors available in values to over 10 Farads, large amounts of energy can be affordably stored internally in a very small space to use as a short term power source to extend operations well beyond a detected loss of external system power.” ('939 patent, 3:5-10 (INTEL-1001).)

89. The '939 patent also incorporates a DC-DC up-converter 32 to “convert the voltage supplied by EPS 22” and a DC-DC down-converter 42 to “convert the voltage from the SC 34 to supply power to the [computing engine] CE 28.” ('939 patent, 3:39-48, (INTEL-1001).) When external power is available, “CE 28 ... is supplied power from the external power source EPS 22 through the power

isolator PI 26.” (’939 patent, 3:32-35 (INTEL-1001).) The up-converter 32 “convert[s] the voltage supplied by the EPS 22 and charge[s] the super-capacitors 34.” (’939 patent, 3:39-41 (INTEL-1001).) Therefore, the current from external power source EPS 22 passes through DC-DC up-converter 32 and to super-capacitors SC 34. I have annotated Figure 1 of the ’939 patent below to show power isolator 26 in orange, super-capacitors SC 34 in red, DC-DC up-converter 32 in green, and current that flows through the power isolator and up-converter into the super-capacitors in yellow. I have also shown computing engine 28 in blue.



90. When low power sensors detect that external power falls “below a certain threshold amount,” “the up-converter is deactivated, ... [and] the down-converter is activated.” (’939 patent, 5:6-24, (INTEL-1001).) Super-capacitors 34 “then begin to slowly discharge current to the computer system through the down-converter.” (’939 patent, 5:26-28 (INTEL-1001).) I have annotated Figure 1 of the ’939 patent below to show the low power sensors 24 in grey, power isolator 26 in orange, super-capacitors SC 34 in red, DC-DC up-converter 32 in green, DC-DC down-converter 42 in purple, computing engine 28 in blue, and the path of current flow through the down-converter to the computing engine is in brown.



91. When the system is in save mode, as the super-capacitors discharge, “data is transferred from the volatile memory to the non-volatile memory.” (’939 patent, 5:33-35 (INTEL-1001).) The ’939 patent incorporates “charge level sensors [to] inform the computer system that the super-capacitor voltage has fallen below the fully charged and partially charged levels.” (’939 patent, 5:36-48 (INTEL-1001).) “[O]nce the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system” (’939 patent, 5:39-42 (INTEL-1001).)

C. Prosecution History

92. I have reviewed the prosecution history of the ’939 patent. The application for the ’939 patent was filed on September 21, 1999. (File History of ’939 patent, 2, 20, 50 (INTEL-1002).) The originally filed application included claims 1-18, with claims 1 and 10 being the independent claims. (File History of ’939 patent, 36-39 (INTEL-1002).) Originally filed claim 1 included is reproduced below:

1. *A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:*

(a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; and

(b) reconfiguring the data in the computing engine.

(File History of '939 patent, 36 (INTEL-1002).) Originally filed claim 10 recited similar limitations. As seen above, originally filed claim 1 included the “activating” (step (a)) and “reconfiguring” (step (b)) limitations. The Examiner rejected the originally filed independent claims 1 and 10 as well as dependent claims 2-4, 6, 7, 11-13, 15, and 16 as being anticipated by U.S. Pat. No. 5,542,042 (“Manson”). (File History of '939 patent, 56-57 (INTEL-1002); Manson (INTEL-1022).) The Examiner also rejected dependent claims as being obvious over Manson in view of U.S. Pat. No. 5,768,208 (“Bruwer”). (File History of '939 patent, 58 (INTEL-1002); Bruwer (INTEL-1023).)

93. The applicant amended originally filed independent claims 1 and 10 to include the “deactivating” limitation (step (c) that appears in issued and challenged independent claims 1 and 10) and argued that Manson and Bruwer failed to teach that limitation. (File History of '939 patent, 69, 75-77, 82-83 (INTEL-1002).) In response, the Examiner allowed the challenged claims without providing a Statement of Reasons for Allowance. (File History of '939 patent, 92-95 (INTEL-1002).)

D. Level of Ordinary Skill in the Art

94. I understand that certain issues relating to the validity of the '939 patent must be judged from the perspective of a person of ordinary skill in the relevant art, as I discuss below. I have been asked to define the level of a “person of ordinary skill in the art” or “POSITA” at the time the alleged invention as claimed was made. In ¶¶ 82-91, I provided an overview of the '939 patent. In deciding the level of ordinary skill, I have considered the following factors, which I have been informed are relevant to the determination of ordinary skill in the art:

- the levels of education and experience of persons working in the field;
- the types of problems encountered in the art;
- the prior art solutions to these problems;
- the rapidity with which innovations are made; and
- the sophistication of the technology.

95. In my opinion, a POSITA would have been someone with at least a bachelor's degree in electrical engineering, physics, or a related scientific field, and approximately two years of experience working on computer system architecture and power management circuits, or an equivalent combination of education and experience.

96. I explain below how a POSITA would have understood the technology described in the references I have identified in this Declaration as of the priority date of the '939 patent.

E. Claim Construction

97. I understand that claim construction is the process of determining a patent claim's meaning. I also understand that the Patent Office applies the same claim construction standard used in district courts which seeks to give claim terms their plain and ordinary meaning to a POSITA at the time of the claimed invention in view of the claims, specification, and prosecution history.

98. I understand that a "means-plus-function" claim term is a term that recites a particular function but does not recite a specific structure for performing that function. I understand that means-plus-function terms are limited to the function recited in the claim(s) and the specific structure disclosed in the patent's specification for performing that function, as well as structures equivalent to the disclosed structures.

99. In this section, I identify claim constructions or identifications of structure that I have been asked to consider in this Declaration for the following means-plus-function limitations: "means for activating" (claim 10), "means for reconfiguring" (claim 10), "means for deactivating" (claim 10), "means for allowing" (claim 12), "means for reversing" (claim 15), and "means for

discharging” (claim 15). For other claim terms, I give the terms their plain and ordinary meaning to a POSITA unless otherwise noted. I am aware that a district court has construed some terms of the challenged claims and, when analyzing the prior art below, consider the court’s constructions and Petitioner’s and Patent Owner’s proposed constructions to the district court. (Claim Construction Order and Memorandum in Support Thereof, 10-26, 46-47 (INTEL-1018).)

1. “*means for activating*” (claim 10)

100. I understand the claimed function is “*activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system.*”

101. I also understand that, for purposes of the Petition, the Petitioner identifies the corresponding structure for the term “*means for activating*” as an up-converter and a down-converter (and equivalents). I further understand that the Patent Owner contends that power sensors and a power isolator are also required corresponding structure. (BiTMICRO LLC’s Responsive Claim Construction Brief, 17 (INTEL-1011).) I have considered these constructions when analyzing the prior art below.

2. “*means for reconfiguring*” (claim 10)

102. I understand the claimed function is “*reconfiguring the data in the computing engine.*”

103. I also understand that, for purposes of this IPR, the Petitioner identifies the corresponding structure for the term “*means for reconfiguring*” as non-volatile memory and volatile memory (and equivalents). I have considered this structure when analyzing the prior art below.

3. “*means for deactivating*” (claim 10)

104. I understand the claimed function is “*deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.*”

105. I am aware that the district court concluded that “*deactivating*” means “that the capacitor is electrically disconnected such that it not discharging current to a load.” (Claim Construction Order and Memorandum in Support Thereof, 19 (INTEL-1018).) That is similar to what the Patent Owner argued to the court. (BiTMICRO LLC’s Sur-Reply Claim Construction Brief, 3 (INTEL-1019).) I understand that, for purposes of this IPR, the Petitioner identifies “*deactivating*” as having the meaning provided by the court. I have considered this when analyzing the prior art below.

106. I also understand that, for purposes of this IPR, the Petitioner identifies the corresponding structure for the term “*means for deactivating*” as a down-converter (and equivalents), and as potentially including switches, transistors, gates, etc. that are generally known in the art. This is consistent with

the district court's construction of corresponding structure for the "*deactivating*" limitation. (Claim Construction Order and Memorandum in Support Thereof, 20 (INTEL-1018).) In addition to a down-converter, I understand that the Patent Owner identified super-capacitor charge level sensors, an up-converter, and a power isolator as corresponding structure. (BiTMICRO LLC's Responsive Claim Construction Brief, 7-8 (INTEL-1011); BiTMICRO LLC's Sur-Reply Claim Construction Brief, 4 (INTEL 1019).) I have considered these structures when analyzing the prior art below.

4. "*means for allowing*" (claim 12)

107. I understand the claimed function is "*allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.*"

108. I understand that, for purposes of the Petition, Petitioner identifies the corresponding structure for the term "*means for deactivating*" as volatile and non-volatile memory (and equivalents). I have considered this structure when analyzing the prior art below.

5. "*means for reversing*" (claim 15)

109. I understand the claimed function is "*reversing the flow of current between the computing engine and the plurality of super capacitors.*"

110. I further understand that, for purposes of this IPR, the Petitioner identifies the corresponding structure for the term “*means for reversing*” as a down-converter and an up-converter (and equivalents). I also understand that the Patent Owner has suggested that power sensors and a power isolator, as well as the corresponding structures required for the “*means for deactivating*,” are additional required corresponding structure for the “*means for reversing*” limitation. (BiTMICRO LLC’s Responsive Claim Construction Brief, 10-12 (INTEL-1011).) I have considered these structures when analyzing the prior art below.

6. “*means for discharging*” (claim 15)

111. I understand the claimed function is “*discharging current from the plurality of super capacitors to the computing engine.*”

112. I also understand that, for purposes of this IPR, the Petitioner identifies the corresponding structure for the term “*means for discharging*” as an up-converter and a down-converter (and equivalents). I further understand that the Patent Owner may argue that power sensors and a power isolator are additional required corresponding structure for the “*means for discharging*” limitation. I have considered these structures when analyzing the prior art below.

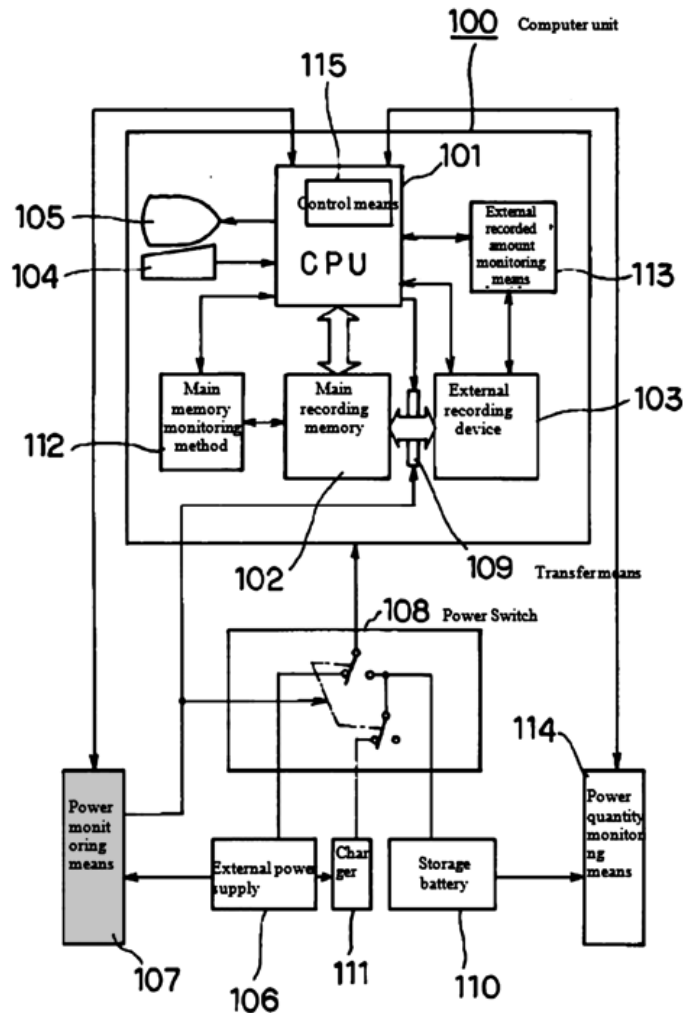
III. Claims 1-3, and 6 would have been obvious over the combination of Nishida and Nakao (including in further combination with Harari)

A. Claim 1

- 1. 1.pre: “*A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:*”**

113. Nishida combined with U.S. Pat. No. 5,535,328 (“Harari”) rendered the preamble to claim 1 obvious. Turning to the “*computer system*” limitation, Nishida disclosed a “**computer system**” that includes “computer unit 100 and a power supply part.” (Nishida, ¶3 (INTEL-1006).) Figure 1 annotated and reproduced below “is a block diagram illustrating a configuration of **a computer system** with a memory backup guaranteed amount display function.” (Nishida, ¶10 (INTEL-1006).) In addition, the system of Nishida’s Figure 1 incorporates the system of Nishida’s Figure 2: “This computer system [Figure 1] ... is configured with the above-mentioned conventional computer system [Figure 2].” (Nishida, ¶¶10-11 (INTEL-1006).) The overlap between the two figures is also apparent given that they both use the same reference numbers to refer to system components.

【Figure 1】



114. Nishida taught that the computer system “loses power” when there is an external power supply outage. Nishida disclosed that its “power supply portion consists of an external power supply 106, such as a commercial power supply” and “the power supply monitoring means 107 constantly monitors the supply voltage of the external power supply 106, warns CPU 101 when **this supply voltage deviates from a predetermined range.**” (Nishida, ¶3 (INTEL-1006).) According to Nishida, generally when a computer system’s power supply “is interrupted due to a

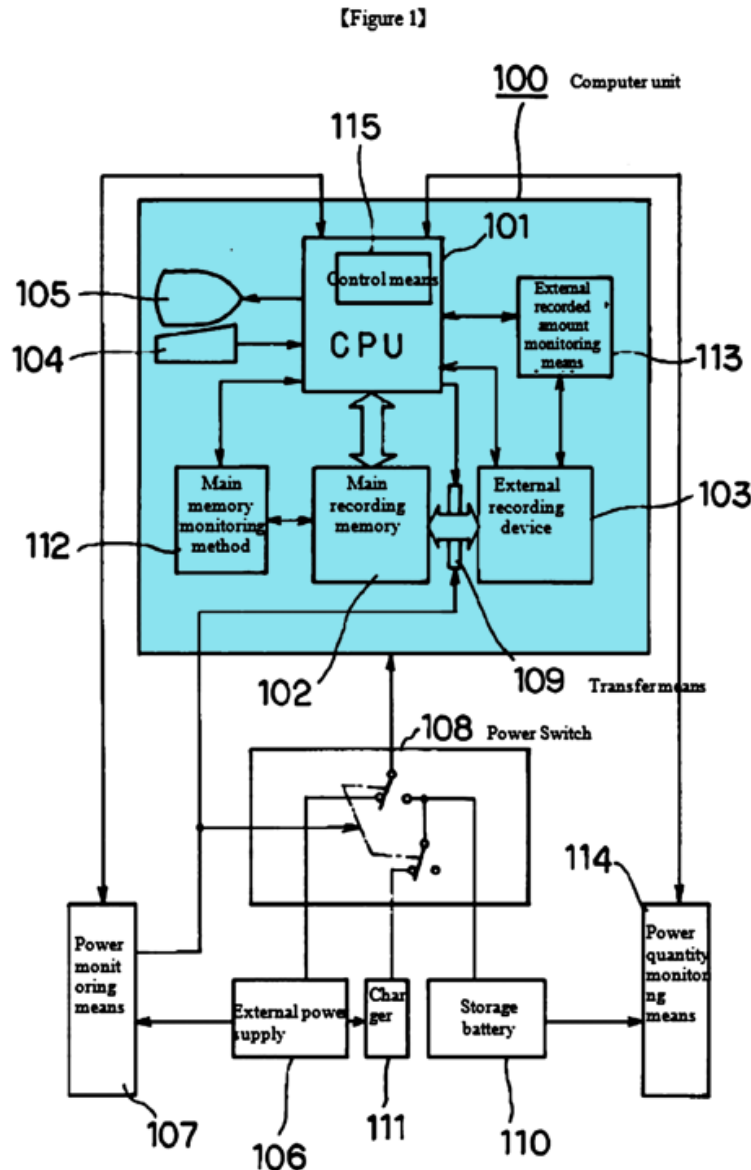
power outage, data stored in the main memory in the computer system will disappear.” (Nishida, ¶2 (INTEL-1006).) To prevent the loss of data and provide a “back up” of “the main memory,” Nishida taught that “if an abnormality is detected in the supply voltage from the external power supply, the data on the main memory is urgently transferred to a non-volatile external recording device using the power supply for the backup to protect data.” (Nishida, ¶2 (INTEL-1006).) The power outage can manifest as a “deviat[ion] from a predetermined range.” (Nishida, ¶¶3, 4, 7, 15 (INTEL-1006).) Power supply monitoring means 107 “constantly monitors the supply voltage of the external power supply 106” so that it can detect any power outage. (Nishida, ¶¶2-3 (INTEL-1006).) Annotated Figure 1 of Nishida reproduced above shows the power supply monitoring means 107 in gray.

115. If a power outage occurs, the computer system performs “*a method for controlling data*.” Nishida disclosed controlling data by transferring data from main recording memory 102 to non-volatile external recording device 103. When a power outage is detected, “the data on the main memory is urgently **transferred** to a non-volatile external recording device using the power supply for the backup to protect data.” (Nishida, ¶2 (INTEL-1006); *see also* ¶¶3, 4, 15.) Nishida disclosed that its main recording memory 102 is “volatile”: “The computer unit 100 consists of ... **a volatile main recording memory 102** that is directly accessed from the

CPU 101.” (Nishida, ¶3 (INTEL-1006).) As discussed in ¶¶34-41, volatile memory loses data when its supply power is not available and non-volatile memory stores data even when the power supply is lost. Therefore, transferring data to non-volatile external recording device 103 “protect[s]” the data from “disappear[ing]” in the event of an external power loss. (Nishida, ¶2 (INTEL-1006).) Nishida’s teachings closely resemble the ’939 patent’s disclosures of the save mode used when external power is interrupted. (’939 patent, 4:37-41, 5:19-28, 5:34-36 (INTEL-1001).) As discussed in ¶¶42-48, computer systems with memory backup capabilities were well known before the September 1999 filing date of the ’939 patent.

116. Nishida also taught multiple alternatives of the “*computing engine*” that is recited in the preamble to claim 1. First, Nishida’s computer system includes computer unit 100. (Nishida, ¶¶3, 11 (INTEL-1006).) “The computer unit 100 consists of a CPU (central processing unit) 101,” as well as other components. ((Nishida, ¶3 (INTEL-1006).) It is apparent from Nishida’s disclosures that computer unit 100 performs “computing” and is therefore a “computing engine.” For example, the computer unit “computes the amount of backup memory

possible” (Nishida, Summary (INTEL-1006)) and “calculates [a] maximum amount of data (memory backupable amount) that can be transferred.” (Nishida, ¶14 (INTEL-1006); *see also* ¶¶8, 11, 16). Both of those functions involve computations based on data available to the computer system. Annotated and Figure 1 of Nishida reproduced below shows computer unit 100 in blue.



117. In the alternative, computer unit 100's "CPU (central processing unit) 101," "volatile main recording memory 102," and "non-volatile external recording device 103" are another example of a "*computing engine*" as claimed in the preamble to claim 1. (Nishida, ¶3 (INTEL-1006).) All three of these structures are engaged in functions that relate to "computing." CPU 101 uses data available in the computer system to "calculate[] a memory backup possible amount, which is the amount of data that can be transferred from the main recording memory 102 to the external recording device 103, based on the amount of power that can be supplied from the storage battery 110 monitored by the power amount monitoring means 114." (Nishida, Summary, ¶¶8, 11, 14, 16 (INTEL-1006).) Those calculations are computations and CPU 101 is therefore a "computing engine." Main recording memory 102 and external recording means 103 "exchange[]" data and instructions for use by computer unit 100 and CPU 101. (Nishida, ¶3 (INTEL-1006); *see also* ¶¶2, 4, 11, 14-15.) For example, computer systems like the one described in Nishida involve the process of executing programs in which the CPU executes "a set of instructions stored in memory." (Stallings, 52 (INTEL-1039).) "The CPU reads (**fetches**) instructions from memory one at a time, and it executes each instruction." (Stallings, 52 (INTEL-1039) (emphasis in original).) Thus, memory plays an important role in computing. As shown in the annotated Figure 1

of Nishida reproduced above, CPU 101, main recording memory 102, and external recording device 103 are within computer unit 100.

118. External recording device 103 is a memory because it receives and “protect[s]” data transferred from memory 102 (Nishida ¶2 (INTEL-1006); *see also* Summary, ¶¶3, 15). That involves storing the data. External recording device 103 also provides a “memory backup function” when it stores and protects the data transferred from main recording memory 102 during a power outage: “the data on the main memory is urgently transferred to a non-volatile external recording device using the power supply for the backup to protect data.” (Nishida ¶2 (INTEL-1006); *see also* Summary, ¶¶1, 5, 11, 16.)

119. In addition, the general term “device” as used in “recording device 103” would have been understood by a POSITA to include a “memory.” In the field of electronics, a “device” is “[a] simple or complex discrete electronic component.” (“The Illustrated Dictionary of Electronics,” 5th Edition, 1990 by Turner (“Turner”), 157 (INTEL-1042).) External recording device 103 in Nishida fits this description. It was also understood that a “memory” was a known “device” that records data: “[a] **memory is a device** made so that a unique address (input) will give a unique output” (U.S. Pat. No. 3,854,226 (“Divine”), 3:38-40 (INTEL-1025)); “[a] **flash memory is a device** providing erasable programmable read only memory containing many sectors, each sector containing a number of bytes, where

each sector is separately erasable” (U.S. Pat. No. 6,629,317 (“Kirschner”), 1:34-37 (INTEL-1026).) Recognizing this fact, Nishida often referred to main memory 102 as a “recording memory.” (Nishida, Summary ¶¶3-4, 7-8, 11, 14-16 (INTEL-1006).) Nishida’s CPU and volatile and non-volatile memories are similar to the “computing engine” described in the ’939 patent, which includes a “processor,” “volatile memory,” and “non-volatile memory.” (’939 patent, 3:33-36 (INTEL-1001); *see also* Fig. 1.)

120. A POSITA would have been motivated to use EEPROM as an implementation of the non-volatile external recording device 103 disclosed in Nishida. First, Nishida does not provide details about the composition of non-volatile external recording device 103. There were many types of non-volatile memories to choose from before the September 1999 filing date of the ’939 patent. For example, as discussed in ¶¶36-41, non-volatile memory device options included at least ROM, EPROM, EEPROM, and flash memory devices. A POSITA desiring a non-volatile memory device would have investigated these available options at the time to discover Harari, which described “[a] system of Flash EEprom memory chips with controlling circuits serv[ing] as non-volatile memory.” (Harari, Abstract (INTEL-1024).)

121. Harari disclosed “an array of electrically erasable programmable read only memories (EEprom’s) integrated circuit chips.” (Harari, 3:48-58 (INTEL-

1024).) A POSITA would have had a reasonable expectation of success because Harari's EEPROM would have been used for its intended purpose of non-volatile data storage, which would have stored data even when the power supply is not available. Harari disclosed that EEPROMs are "nonvolatile, and retain their memory even after power is shut down." (Harari, 1:35-36 (INTEL-1024).) This is same functionality required by Nishida's external recording device 103. Harari further disclosed that EEPROMs "are typically used in applications where semi-permanent storage of data or program is required but with a limited need for reprogramming." (Harari, 1:40-43 (INTEL-1024).)

122. Second, Harari taught that using EEPROM as a non-volatile memory storage device provided many advantages to a computer system. For example, EEPROM provides non-volatility "without sacrificing ease of erasing and rewriting data into the memory, speed of access, low cost and reliability" and "requir[es] less power to operate" and "[is] lighter in weight than a hard disk drive magnetic memory." (Harari, 3:48-58 (INTEL-1024).) It was known at the time of the alleged invention that EEPROM "combines the advantage of nonvolatility with the flexibility of being updatable in place, using ordinary bus control, address, and data lines." (Stallings, 110, 111 (INTEL-1039).) Using EEPROM as recording device 103 would have provided these advantages to Nishida's computer system.

123. Furthermore, Nishida's computer unit 100 relies on the finite energy stored in storage battery 110—the backup power supply that can be configured as super-capacitors instead—for executing the data transfer process from main recording memory 102 to external recording device 103 in the event of a power outage. Harari's EEPROMs “requiring less power to operate” would have reduced energy consumption, which would have conserved the energy available in the backup power supply. (Harari, 3:48-58 (INTEL-1024).)

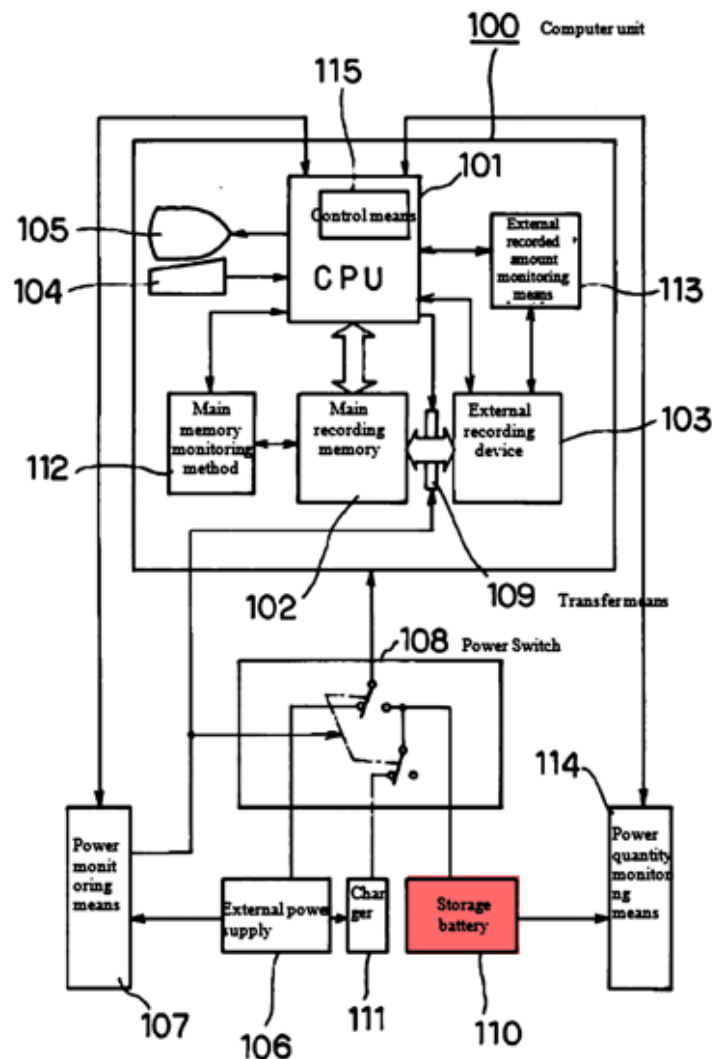
2. **1.a: “(a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;”**

124. As required by limitation 1.a, Nishida disclosed supplying backup power to the computer system “*upon power being removed from the computer system*” using a “*plurality of supercapacitors*.” Nishida taught “a backup power supply consisting of storage batteries, **supercapacitors**, lithium primary batteries, etc.” for use when a “power outage” occurs in the “computer system.” (Nishida, ¶2 (INTEL-1006).) As disclosed in Nishida, any one of the structures identified in the list above can be the backup power supply for the computer system. As discussed in ¶¶49-50, common backup power supplies for computer systems at the time of the alleged invention included batteries and capacitors. The examples discussed in ¶¶44-48 used “high voltage energy stored in a backup capacitor” (Ergott, 3:7-10 (INTEL-1008)), batteries for powering the volatile memory, the microcontroller,

and the non-volatile memory “when computer system power is lost” (Holzhammer, 5:28-47 (INTEL-1036)), and a “bank of energy storage capacitors” to supply “enough energy to maintain the voltage supply lines” of the volatile RAM memory, the non-volatile memory, and other circuitry” (Bruder, 7-60-66 (INTEL-1034)).

125. Annotated Figure 1 reproduced below illustrates one example of a backup power supply disclosed in Nishida: storage battery 110. (Nishida, ¶3

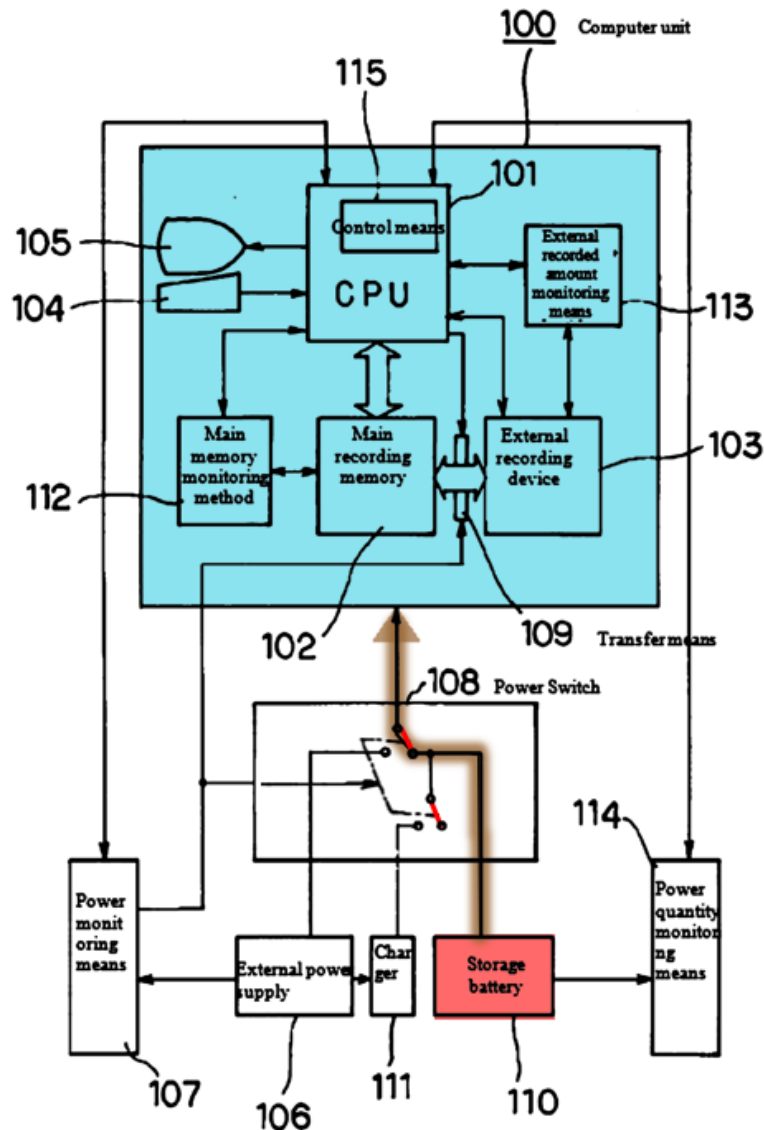
【Figure 1】



(INTEL-1006).) The figure shows storage battery 110 in red. In the remainder of this Declaration, I will refer to backup power supply 110 as super-capacitors 110 based on Nishida's teachings that super-capacitors are another structure that was used as the backup power supply. (Nishida, ¶2 (INTEL-1006).)

126. Nishida also disclosed "*activating [the] super capacitors to supply power to the computing engine*" as required by limitation 1.a. Nishida's computer system includes power switching switch 108, which in response to an outage of external power, "switches the supply of power to computer unit 100" to super-capacitors 110. (Nishida, ¶¶3, 4, 15 (INTEL-1006).) Super-capacitors 110 are shown in red in annotated Figure 1 reproduced below. The annotated figure also includes red lines in the upper and lower switches that comprise power switching switch 108. Both switches have been oriented to the backup power supply side on the right. (Nishida, ¶3, 4, 15 (INTEL-1006).) That action creates an electrical connection between super-capacitors 110 and computer unit 100 (blue) by creating a transmission path between the two. Once this electrical connection is established, the super-capacitors are "*activat[ed]*" and begin providing power along the path indicated with a brown arrow so "computer system is operated by power from" super-capacitors 110. (Nishida, ¶3, 4, 15 (INTEL-1006).) The electrical connection provides a discharge path for the super-capacitors to provide power to a load (computer unit 100).

【Figure 1】



127. In addition to providing power to computer unit 100, super-capacitors 110 supply power to the individual components within computer unit 100, such as CPU 101, main recording memory 102, and external recording device 103. Because of the backup power supply, computer unit 100 and its individual components continue to operate even though the external power supply has been

interrupted. “If the supply voltage of the external power supply 106 deviates from a predetermined range, the power supply monitoring means 107 immediately switches the power switching switch 108 to the storage battery 110, and **this computer system is operated by power from the storage battery 110.**”

(Nishida, ¶4 (INTEL-1006); *see also* ¶5.) As explained in ¶¶116-117 regarding limitation 1.pre, the “*computing engine*” of Nishida’s system is computer unit 100 or CPU 101, main recording memory 102, and external recording device 103.

Those are structures that receive power when super-capacitors 110 are activated.

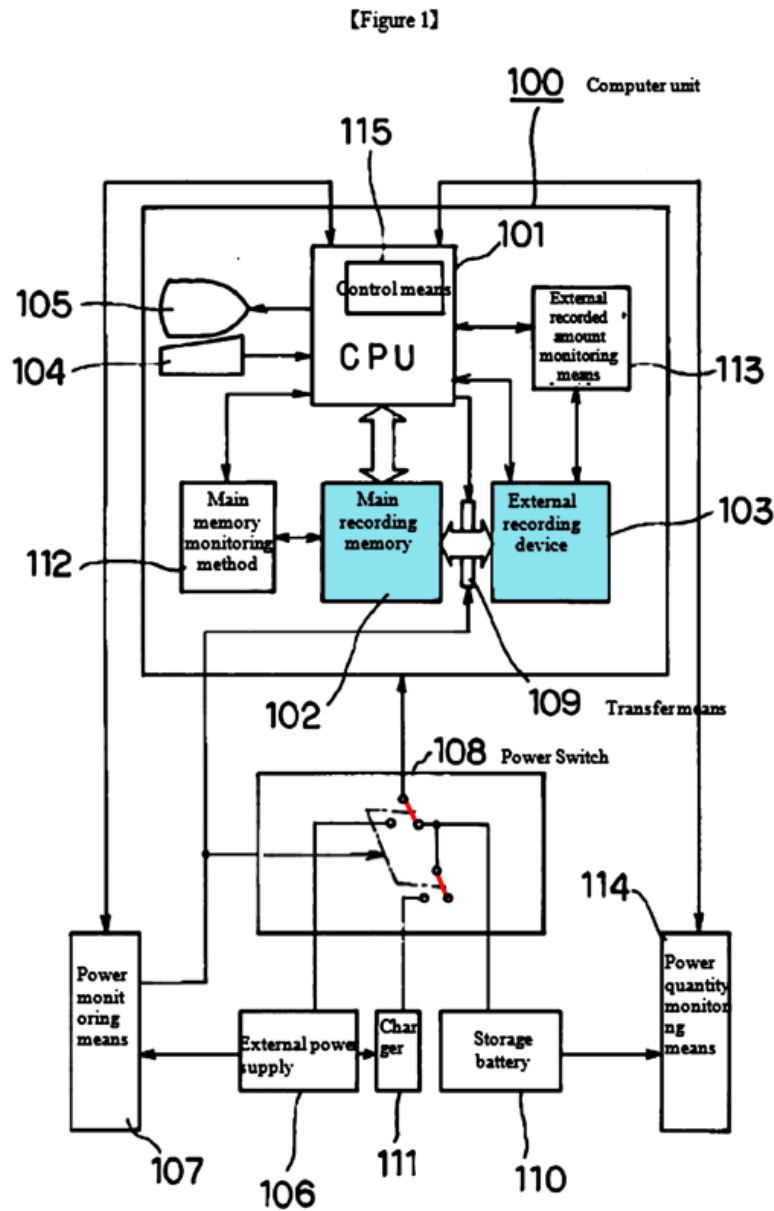
3. 1.b: “(b) reconfiguring the data in the computing engine; and”

128. Nishida disclosed this limitation, and the combination of Nishida and Harari rendered it obvious. Nishida taught that after a power outage was detected by the computer system, “data on the main recording memory 102 is **completely evacuated** to the external recording device 103.” (Nishida, ¶15 (INTEL-1006).)

Nishida also described the evacuation process as a “transfer” from “main recording memory 102 to the external recording device 103.” (Nishida, Summary (INTEL-1006).) Nishida disclosed that “power supply monitoring means 107 constantly monitors the supply voltage of the external power supply 106, warns CPU 101 when this supply voltage deviates from a predetermined range, switches power supply switching switch 108 to the storage battery 110 side, and instructs the

transfer means 109 to **transfer the contents of main recording memory 102 to external recording device 103.**” (Nishida, ¶3 (INTEL-1006); *see also* ¶¶2, 4, 7-9, 14-15.)

129. Nishida described the volatility characteristics of main recording memory 102 and external recording device 103—the former is “volatile” while the latter is “non-volatile.” (Nishida, ¶2, 3, 7 (INTEL-1006).) As explained in ¶¶116-123 regarding limitation 1.pre, (i) external recording device 103 is a memory, (ii) a POSITA would have been motivated to use Harari’s EEPROM as Nishida’s external recording device, and (iii) main recording memory 102 and external recording device 103 constitute a portion of a “*computing engine*” (whether that component is computer unit 100 or CPU 101, main recording memory 102, and external recording memory 103). Annotated Figure 1 of Nishida reproduced below shows main recording memory 102 and external recording device 103 in blue. There is a double-headed arrow between the two structures that signifies the transfer of information between them as described in Nishida. Power switching switch 108 has been configured to the backup power supply side on the right, as indicated with two red lines, which happens once a power outage is detected. (Nishida, ¶3, 4, 15 (INTEL-1006).)



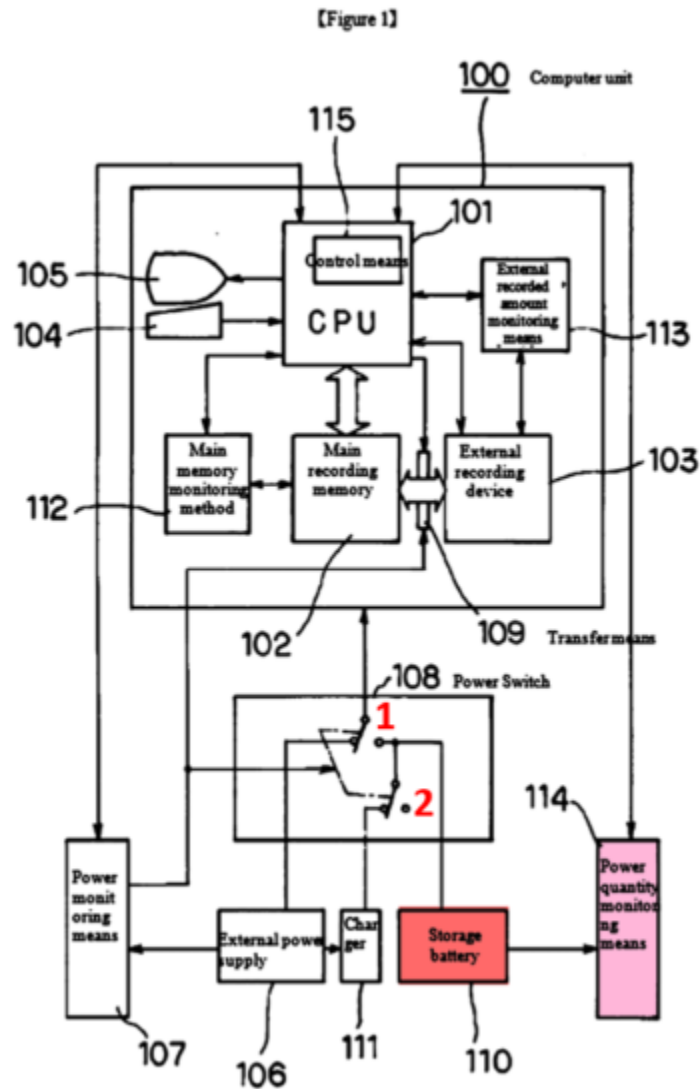
130. The data transfer taught in Nishida is like the data transfer that is disclosed in the '939 patent. The patent discloses “transfer[ring] all data from volatile memory to non-volatile memory” where each of the memories is included in the computing engine that also includes a “processor.” ('939 patent, 5:13-16 (INTEL-1001); *see also* 4:37-41, 5:33-36, Fig. 1.)

4. **1.c: “(c) *deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.*”**

131. Nishida, and the combination of Nishida and Harari, further in combination with Nakao rendered limitation 1.c obvious. As explained in ¶¶124-127 regarding limitation 1.a, Nishida disclosed a “*computing engine*” that receives a power supply from a “*plurality of super capacitors.*” Nishida taught that super-capacitors 110 store a finite amount of energy, which necessitates shutting down the computer system after a power outage: “[b]ecause there is a limited amount of charge in the storage battery 110, it is necessary to shut down the computer system, so at the same time as switching to the storage battery 110 side, the CPU 101 initiates a shutdown process effected by a warning from the power supply monitoring means 107, and the transfer means 109 initiates the transfer of the contents of the main recording memory 102 to the external recording device 103.” (Nishida, ¶2 (INTEL-1006); *see also* ¶4.) Nishida’s system also provides real-time monitoring of the energy stored in super-capacitors 110: “power monitoring means 114 [] monitor[s] the current charge amount of the storage battery 110 and report it to the CPU 101.” (Nishida, ¶11 (INTEL-1006); *see also* ¶14.)

132. Power switching switch 108 is positioned between computer unit 100 (above the switch) and external power supply 106 and super-capacitor 110 (below the switch) and operates by “switch[ing] the supply of power to the computer unit

100 between the external power supply 106” and super-capacitors 110. (Nishida, ¶3 (INTEL-1006); *see also* ¶¶4, 15.) As shown in annotated Figure 1 of Nishida reproduced below, super-capacitors 110 are connected to external power supply 106 through a lower switch (labeled “2”). In this configuration, super-capacitors 110 are being “charged by the charger 111.” (Nishida, ¶13 (INTEL-1006).) The super-capacitors are not supplying power to computer unit 100 because the upper switch (labeled “1”) is switched to the external power supply side on the left, which disconnects the current path between computer unit 100 and super-capacitors 110. The disconnection precludes the super-capacitors from providing power to computer unit 100. Instead, the “computer system is operated with power from the external power supply 106.” (Nishida, ¶13 (INTEL-1006).) Annotated Nishida’s Figure 1 reproduced below shows super-capacitors 110 in red and power quantity monitoring means 114 in pink.

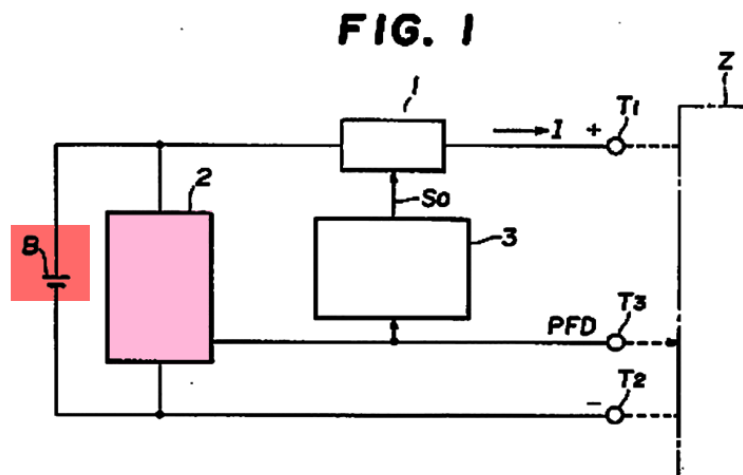


a) The teachings of Nakao

133. Nakao described a technique for “preventing over-discharge” in power storage elements, including for example a “secondary battery, primary battery and large-scale capacitors, etc.” (Nakao, 1:5-8 (INTEL-1007).) Nakao disclosed numerous examples, each of which involves the basic steps of first detecting that large-scale capacitors have reached a particular voltage level and

second sending signals to orient a switch to cut off the power supply from the capacitors to the rest of the computer system.

134. The first embodiment described by Nakao is shown in annotated Figure 1 reproduced below. The embodiment includes the following structures: electric storage element B, switching portion 1, voltage detector 2, discharge controller 3, and external apparatuses and instruments Z. (Nakao, 2:14-25, 2:40-42, 2:66-3:31 (INTEL-1007).) Annotated Figure 1 shows storage element B (which is described as a battery) in red and voltage detector 2 in pink. Nakao also disclosed that other structures can be used as electric storage elements, including for example “large-scaled capacitors.” (Nakao, 2:40-42 (INTEL-1007).) The external apparatuses and instruments Z “are connected to each of the connectors T1, T2, T3 of the battery package.” (Nakao, 3:17-19 (INTEL-1007).)



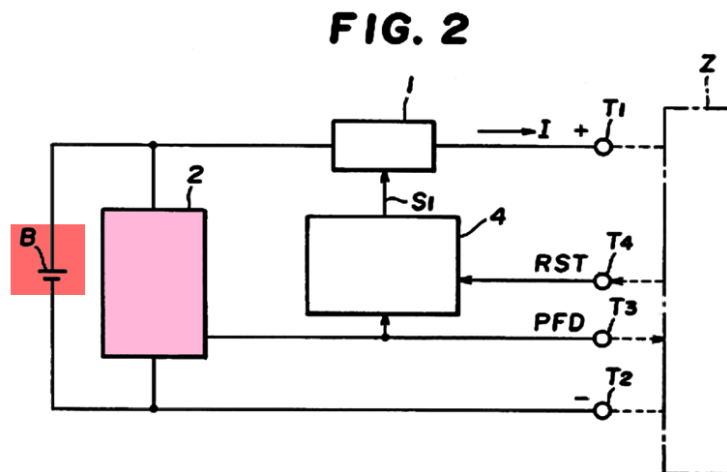
135. The embodiment shown in Figure 1 of Nakao operates as follows.

First, “when the external apparatuses and instruments Z are connected to each of the connectors T1, T2, T3 of the battery package, discharge of the battery B starts.” (Nakao, 3:17-21 (INTEL-1007).) If the voltage level of storage element B “is above the discharge finishing voltage VL (that is, a limited voltage for finishing the discharge), the voltage detector 2 maintains its inoperative state, and the switching portion 1 is turned into its ON-state by its output so that **a discharge current I is supplied to the external apparatuses and instruments Z through the terminals T1, and T2.**” (Nakao, 3:20-30 (INTEL-1007).)

136. As the storage element B continues to discharge, the voltage level “gradually” reduces. (Nakao, 3:31-32 (INTEL-1007).) When the voltage level of the storage element B “becomes lower” than a “discharge finishing voltage VL”, voltage detector 2 “output[s] a discharge finishing signal PFD.” (Nakao, 3:33-35 (INTEL-1007).) “When the external apparatuses and instruments receive an ON-state of the discharge finishing signal PFD,” they “judge the battery to be in a used-up consumed [] state and therefore begin stopping ... operation.” (Nakao, 3:35-40 (INTEL-1007).) Discharge controller 3 waits for a brief period of time and then sends “signal S0” to “make the switching portion 1 ... change to an OFF state.” (Nakao, 3:41-63 (INTEL-1007).) When “the switching portion 1 of the next

stage change to an OFF state” and “the electric power supply to the external apparatuses and instruments Z is stopped.” (Nakao, 3:41-63 (INTEL-1007).)

137. The second embodiment described in Nakao is shown in annotated Figure 2 reproduced below and includes components that are the same as or resemble the components used in the first embodiment shown in Figure 1. The Figure 2 embodiment uses a controller that operates differently, however. “When the discharge is continued to the point where the battery voltage is lower than the discharge finishing voltage VL,” voltage detector 2 “transmit[s] [a] discharge finishing signal PFD.” (Nakao, 4:47-52 (INTEL-1007).) Annotated Figure 2 of Nakao reproduced below shows storage element B in red and voltage detector 2 in pink.

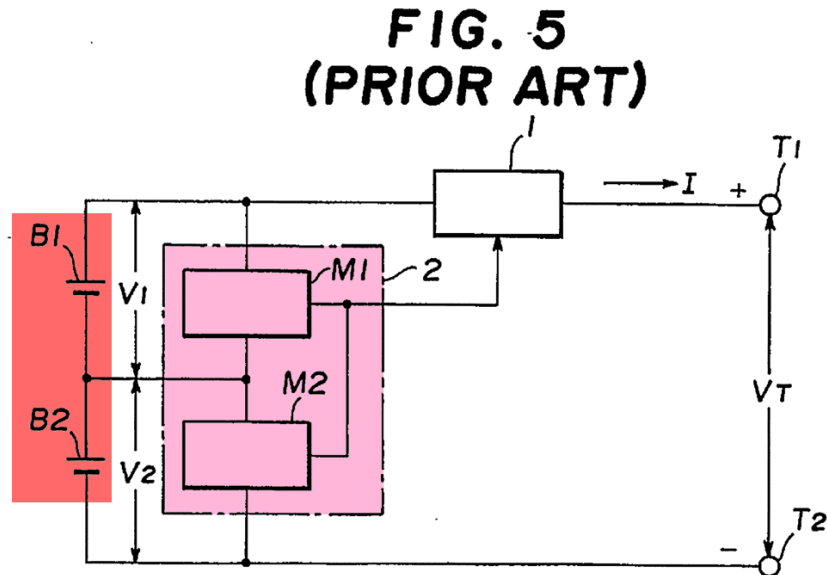


138. Once the external apparatuses and instruments Z “recognize the discharge-finish” signal PFD, “a predetermined stop operation (data-save

operation, etc.) is executed.” (Nakao, 4:53-59 (INTEL-1007).) After that, apparatuses and instruments Z transmit “a power cut-out signal RST.” (Nakao, 4:53-59 (INTEL-1007).) “When the power cut-out signal RST is input to the remote controller 4, an OFF output signal S1 is output from the output side to the switching portion 1 so that the power supply to the external apparatuses and instruments Z is stopped.” (Nakao, 4:59-63 (INTEL-1007).)

139. Nakao also disclosed a “conventional prior art structure of a battery package provided with the conventional over-discharge prevention apparatus.” (Nakao, 2:57-59 (INTEL-1007).) The conventional prior art structure shown in annotated Figure 5 reproduced below also includes some of the same components used in the first and second embodiments illustrated in Figures 1 and 2—storage elements, a voltage detector, and a switching portion. (Nakao, 1:23-29, 2:57-59 (INTEL-1007).) The conventional prior art structure does not include a controller. In the convention prior art structure, “[w]hen the battery voltage falls below a discharge extinction voltage, the voltage detector 2 is driven to switch OFF the switching portion 1 to thereby stop the electric supply to electronic apparatuses and instruments.” (Nakao, 1:29-32 (INTEL-1007).) “The electric apparatuses and instruments have been provided with a power source detection mechanism so that the remaining battery remanent Voltage is assumed from a voltage value VT of the power source in the battery package to judge in advance the state of battery

consumption, and then an operation of the electronic apparatuses and instruments are accurately stopped before the battery output is cut off.” (Nakao, 1:38-46 (INTEL-1007).) Annotated Figure 5 of Nakao reproduced below shows storage element B in red and voltage detector 2 in pink.



140. Nakao’s two embodiments (the Figure 1 and Figure 2 embodiments), and conventional prior art structure (the Figure 5 example) each include an over-discharge prevention circuit that detects the voltage across storage element B and generates a signal to stop the discharge from storage element B once the element discharges to an extinction or finishing voltage, also referred to as VL. (Nakao, 1:29-46, 3:33-47, 4:47-63 (INTEL-1007).)

141. Nakao’s teachings disclosed the claimed “*deactivating*” under the district court’s construction requiring “electrically disconnect[ing]” a power supply

(e.g., capacitor) so that it is “not discharging current to a load.” (Claim Construction Order and Memorandum in Support Thereof, 19 (INTEL-1018).) In the two embodiments and the conventional prior art structure, configuring switching portion 1 to an off position electrically disconnects power electronic apparatuses and instruments Z from storage elements B because turning the switch to the off position interrupts the current flow in the circuit between those two sets of components. That configuration “stop[s]” or “cut[s] off” the power being supplied from storage elements B (the power supply) to electronic apparatuses and instruments Z (the load that receives power).

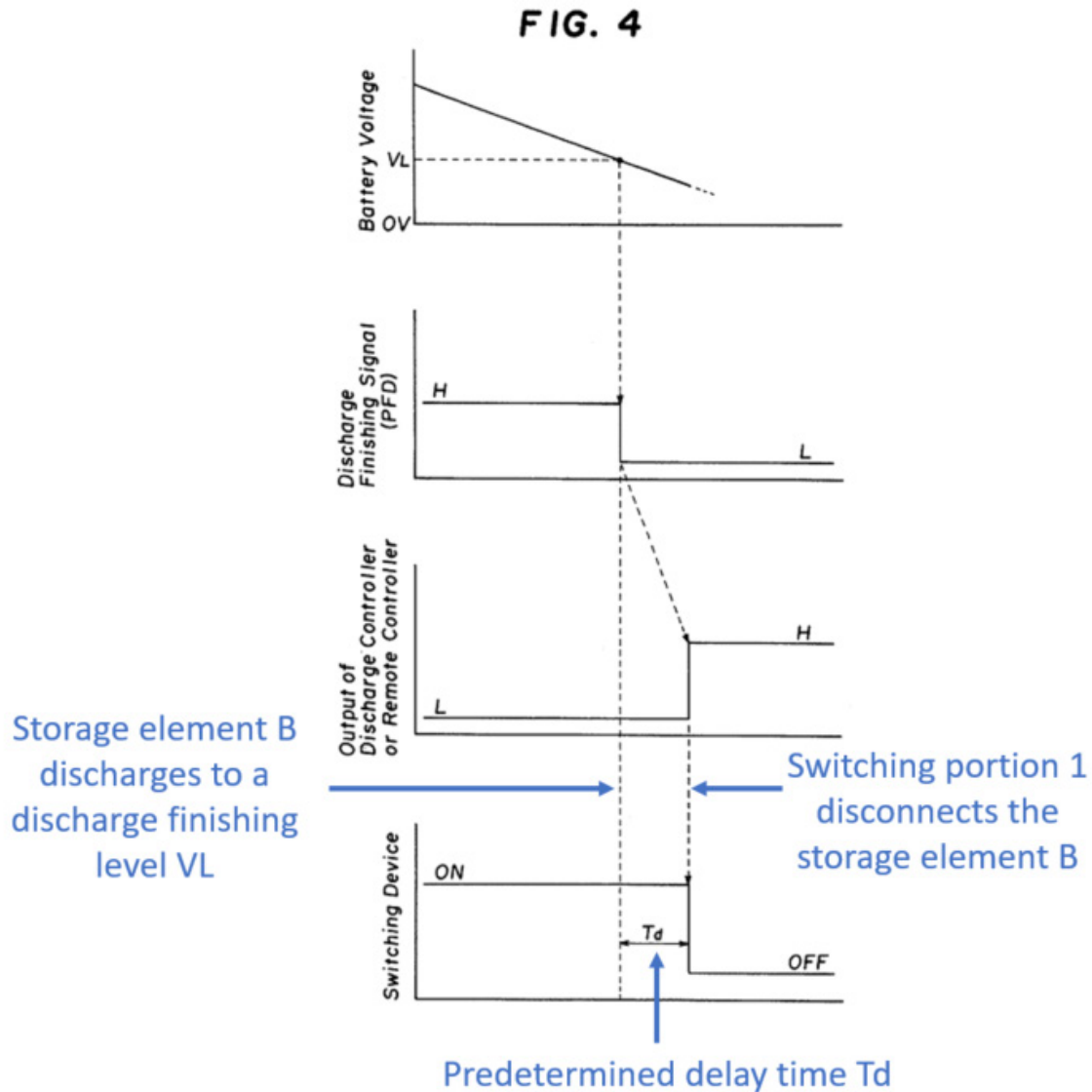
142. For example, regarding the conventional prior art over-discharge prevention mechanisms described in Figure 5, “when the battery voltage falls below a discharge extinction voltage, the voltage detector 2 is driven to switch OFF the switching portion 1 to **thereby stop the electric supply to electronic apparatuses and instruments.**” (Nakao, 1:29-32 (INTEL-1007); *see also* 1:38-46, 1:55-62, 3:41-47, 5:47-53, claim 2.) As another example, when the switching portion 1 has been switched to the “OFF” state, “an OFF output signal S1 is output from the output side to the switching portion 1 so that the power supply to the external apparatuses and instruments Z is stopped.” (Nakao, 4:60-63 (INTEL-1007).) Nakao’s two embodiments and conventional prior art structure electrically disconnect electronic apparatuses and instruments Z from storage elements B using

switching portion 1 and therefore prevent storage elements B from discharging current to the load (electronic apparatuses and instruments Z).

143. In Nakao, the “*deactivating*” is “*based on*” the storage elements (e.g., capacitors) gradually losing voltage until they reach a “*predetermined level*” that causes power cutoff. When the storage elements discharge to discharge extinction or finishing voltage VL, they are disconnected from external apparatuses and instruments Z and therefore “*deactivat[ed]*.” Based on these teachings, VL corresponds to the claimed “*predetermined level*.”

144. I will use Nakao’s first embodiment shown in Figure 1 as an example to explain how Nakao’s power cutoff process is based on a predetermined voltage level of the storage elements (e.g., capacitors). First, voltage detector 2 detects the voltage level of “electric storage element (B) and **output[s] a discharge finishing signal (PFD) when a discharge extinction voltage (VL) is detected.**” (Nakao, Abstract (INTEL-1007).) Next, discharge controller 3 receives the PFD signal and sends an “output signal S0” to switching portion 1 after a “predetermined delay time Td.” (Nakao, 3:31-47 (INTEL-1007).) The predetermined delay time Td is measured from the time when discharge controller 3 receives the PFD signal, as illustrated in annotated Figure 4 of Nakao reproduced below. Lastly, switching portion 1 changes to an “OFF state and then the electric power supply to the

external apparatuses and instruments Z is stopped after the predetermined delay time T_d from the over-discharge detection.” (Nakao, 3:41-47 (INTEL-1007).)

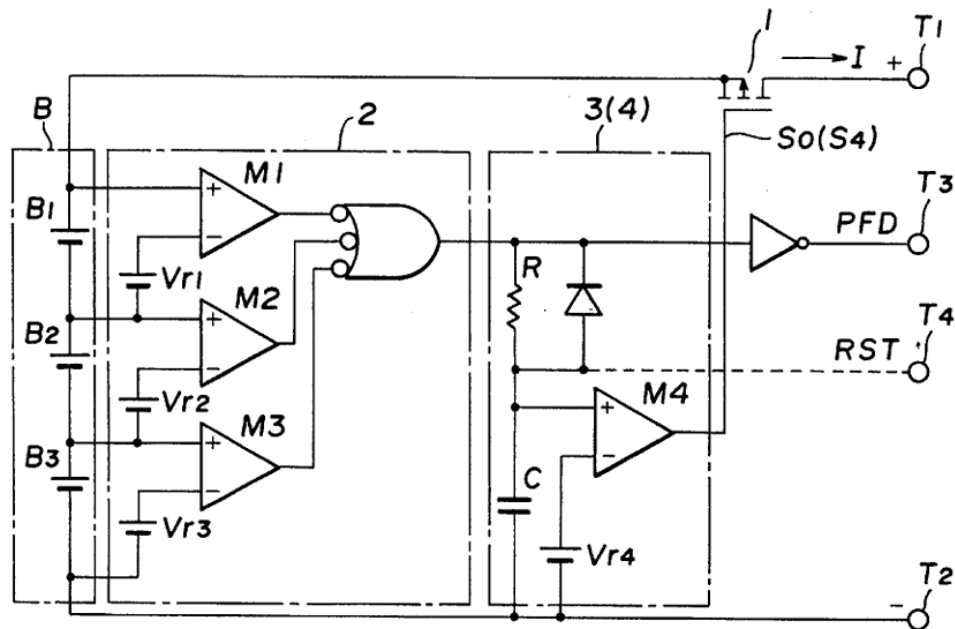


145. I understand the district court construed “*predetermined level*” to have its “plain-and-ordinary meaning.” (Claim Construction Order and Memorandum in Support Thereof, 15 (INTEL-1018).) Under that construction, Nakao disclosed a “*predetermined level*” because the discharge finishing voltage V_L is a pre-set

(“*predetermined*”) voltage limit (“*level*”). Nakao disclosed that discharge finishing voltage VL is “a limited voltage for finishing the discharge” (Nakao, 3:17-26 (INTEL-1007)) and “can be set to a usage limitation value.” (Nakao, 4:4-8 (INTEL-1007).) The specific voltage limit corresponds to a voltage level. The limit is also determined or set in advance before any over-discharge occurs.

146. For example, in Figure 3 reproduced below, Nakao shows a “specific electric circuit” having a battery package with “a battery B composed of three cells B1, B2, and B3 which are connected together in series.” (Nakao, 5:6-9 (INTEL-1007).) “Reference voltages Vr1, Vr2, Vr3 of the comparators M1, M2, M3 **are set in accordance with discharge finishing voltages** of the battery cells B1, B2 and B3.” (Nakao, 5:17-19 (INTEL-1007).) Nakao further disclosed that voltage Vr4 is a “predetermined reference voltage” for comparator M4. (Nakao, 5:20-26 (INTEL-1007); *see also* Fig. 3.) Reference voltages Vr1, Vr2, Vr3 are similarly predetermined reference voltages. This is apparent because Nakao uses the same circuit symbol for reference voltages Vr1, Vr2, Vr3, and Vr4. (Nakao, Figure 3 (INTEL-1007).)

FIG. 3



b) The motivation for combining Nakao with Nishida (including in further combination with Harari)

147. Based on Nakao's explicit teachings, a POSITA would have been motivated to incorporate Nakao's techniques for deactivating power storage elements into Nishida or the combination of Nishida and Harari. As taught by Nakao, "[w]hen the battery voltage falls below a discharge extinction voltage, the voltage detector 2 is driven to switch OFF the switching portion 1 to thereby stop the electric supply to electronic apparatuses and instruments." (Nakao, 1:29-32 (INTEL-1007).) Tracking Nakao's teachings described above, when power quantity monitoring means 114 of Nishida detected a discharge finishing voltage, it would have configured power switching switch 108 to the external power supply

side on the left to electrically disconnecting super-capacitors 110 from computer unit 100. A POSITA would have been motivated to pursue this combination for the reasons set forth below.

148. First, Nakao provides express teachings of over-discharge prevention that would have led a POSITA to modify Nishida's system or the combined system of Nishida and Harari. Nakao explicitly taught the advantages of preventing over-discharge in power storage elements as reflected in Nakao's two embodiments and conventional prior art example. Nakao described "preventing over-discharge in various kinds of accumulator elements such as a secondary battery, primary battery and large-scale capacitors, etc." (Nakao, 1:5-13 (INTEL-1007).) Nakao's over-discharge prevention is based on a straightforward approach that initially uses a voltage detector to sense that power storage elements have discharged to a set extinction or finishing voltage and subsequently uses a controller or detector to transmit signals that configure a switch to an off position, cutting off the power supply provided by the power storage elements. (Nakao, 1:23-37, 3:31-63, 4:45-63 (INTEL-1007).) Nakao's two embodiments and conventional prior art example each involve this approach, though the details differ.

149. To obtain the explicit advantage of over-discharge protection, a POSITA would have implemented any one of Nakao's first embodiment (Figure 1), second embodiment (Figure 2), or convention prior art example (Figure 5) in

Nishida's system or the combined system of Nishida and Harari. The resulting combination would have prevented over-discharge for Nishida's super-capacitors 110 that supply power during a power outage. Further, Nakao described using its over-discharge protection approach on "large-scale capacitors." (Nakao, 1:5-13, 2:40-42 (INTEL-1008).) Nishida's super-capacitors fit in that category. In addition, Nakao's disclosure of plural "large-scale capacitors" would have at least suggested to a POSITA to use multiple super-capacitors in Nishida's system, to the extent Nishida did not disclose multiple super-capacitors. Nakao taught that its over-discharge prevention mechanism was intended for such a design. As explained in ¶56, it was known in the state of the art that using multiple capacitors increased the amount of backup power and lengthened backup time. Nishida does not address the issue of over-discharging super-capacitors 110 or provide any way to prevent it. Given Nishida's silence on the issue, a POSITA would have looked for solutions in the prior art. Nakao provides several ways to prevent over-discharging the power storage element, including for large capacitors.

150. Second, a POSITA would have incorporated the over-discharge prevention approach of any one of Nakao's two embodiments or conventional prior art example into Nishida's system or the combined system of Nishida and Harari because Nishida did not teach how to safely shut down its computer system as backup power continues to discharge toward exhaustion. Both Nishida and Nakao

disclosed computer systems that rely on batteries or capacitors as backup power sources. (Nishida, ¶2 (INTEL-1006); Nakao, 2:66-3:3 (INTEL-1007).) As discussed in ¶49, a POSITA would have recognized that both batteries and capacitors have a finite amount of stored energy, and that the stored energy would eventually be depleted if the external power supply is not reestablished. Nishida acknowledged this fact, noting that “there is limited amount of charge” in super-capacitors 110. (Nishida, ¶4 (INTEL-1006).) Nishida further taught that because backup power is limited, “it is necessary to shut down the computer system” following a power outage. (Nishida, ¶4 (INTEL-1006).) Accordingly, Nishida’s CPU 101 “initiates a shutdown process” when the computer system switches to backup power after an outage. (Nishida, ¶4, 15 (INTEL-1006).) Although Nishida disclosed the initiation of system shutdown, it does not disclose how to successfully finish the shutdown process.

151. Nakao’s two embodiments and conventional prior art example each involve an over-discharge protection approach that provides for a stopping period to allow the computer system to shut down in a controlled and predictable fashion. Referring to the embodiment shown in Figure 1 of Nakao, the over-discharge prevention approach protects “processing data and information [] before the power supply is stopped” and allows for the execution of “**other suitable and necessary emergency processing.**” (Nakao, 6:4-14 (INTEL-1007).) Referring to the

embodiment shown in Figure 2 of Nakao, the over-discharge prevention approach allows “[t]he period of time from over-discharge detection to stop of discharge [to] be controlled freely by the external apparatus and instruments. Consequently, especially in a network system using personal computers or workstations, **serious problems of system-shutdown can be prevented by a suitable power cutting-out sequence.**” (Nakao, 4:64-5:5, 6:20-29 (INTEL-1007).) Referring to the prior art example shown in Figure 5 of Nakao, the over-discharge prevention approach allows “an operation of the electronic apparatuses and instruments [to be] **accurately stopped before the battery output is cut off.**” (Nakao, 1:38-46 (INTEL-1007).)

152. Third, combining Nakao with Nishida’s system or the combined system of Nishida and Harari would have applied a known technique to improve a similar system in the same way as described in Nakao. Nakao disclosed processes for shutting down a computer system when that system is being powered by storage elements with a finite amount of stored energy, such as batteries or large-scale capacitors. (Nakao, 1:23-46, 4:64-5:5, 6:4-29 (INTEL-1007).) Nishida’s system, and the combined system of Nishida and Harari, are similar to Nakao’s system. Nishida addressed the same problem of shutting down a computer system after a power outage while being supplied with backup power from a finite energy source, such as batteries or super-capacitors. (Nishida, ¶¶2, 4 (INTEL-1006).) In

addition, Nishida's system and Nakao's system had the same objective of ensuring the safety and reliability of data despite a power outage. (Nishida, ¶¶2, 5 (INTEL-1006); Nakao, 1:38-46, 5:2-5, 6:4-29 (INTEL-1007).) A POSITA would have looked to Nakao's approaches for accomplishing that objective because Nakao taught "over-discharge prevention" mechanisms that "prevent erroneous (wrong) operation, that is, malfunction" at the time when backup power runs out. (Nakao, 1:5-13 (INTEL-1007).)

153. Nakao's two embodiments and conventional prior art example each involve improving data security by stopping power discharge once power storage elements reach a pre-set discharge extinction or finishing voltage level. Referring to the embodiment shown in Figure 1 of Nakao, the over-discharge protection allows "the discharge [to be] stopped after a predetermined period of time ... **to thereby improve the safety and reliability of the data.**" (Nakao, 6:4-14, 3:48-51 (INTEL-1007).) Referring to the embodiment shown in Figure 2 of Nakao, as a result of the over-discharge protection, the "cut-out timing of the output after the over-discharge detection can be controlled by the external apparatuses and instruments Z and a suitable stopping operation period Td.... Thus, **a serious problem of system-shutdown in a network system such as personal computers, work stations, etc. can be prevented thereby improving the reliability of the entire system.**" (Nakao, 4:55-5:5 (INTEL-1007).) Referring to the conventional

prior art example shown in Figure 5 of Nakao, the over-discharge protection allows “operation of the electronic apparatuses and instruments [to be] accurately stopped before the battery output is cut off **so that the data and information are reliably saved and protected.**” (Nakao, 1:38-46 (INTEL-1007).)

154. The approaches of the embodiments and conventional prior art example of Nakao would have improved data safety and reliability in Nishida’s system or the combined system of Nishida and Harari. For example, Nishida disclosed that “when the supply voltage of the external power supply 106 is within a predetermined range,” if “the sum [of the amount of data on the main recording memory] exceeds the memory backup possible amount, the control means 115 causes the display device 105 to display an alarm.” (Nishida, ¶¶13-14 (INTEL-1006).) Even if the alarm is displayed and available to the operator, the operator may decide that “the data transfer may be performed as is.” (Nishida, ¶14 (INTEL-1006).) Nishida’s system proceeds to execute the data transfer when the “alarm by the control means 115 is ignored and the data transfer instructions are enforced.” (Nishida, ¶15 (INTEL-1006).) In this case, the data transfer is incomplete as Nishida’s super-capacitors 110 run low on, and eventually lose, power. As taught in Nakao, this type of over-discharge leads to “erroneous (wrong) operation” and “malfunction.” (Nakao, 1:5-13 (INTEL-1007).) A POSITA would have been motivated to incorporate Nakao’s shutdown procedures into Nishida’s system or

the combined system of Nishida and Harari to enable the computer system to be “accurately stopped before the [super-capacitors’] output is cut off **so that the data and information are reliably saved and protected.**” (Nakao, 1:38-46 (INTEL-1007).) That would have allowed Nishida’s computer system to shut down operation before super-capacitor power depleted to a level that risked errors and malfunction in the data transfer.

155. This advantage would have been the same regardless of which embodiment or example a POSITA applied to Nishida’s system or the combined system of Nishida and Harari. Nakao’s first embodiment (Figure 1) and second embodiment (Figure 2) implement a stopping period that occurs after the discharge extinction or finishing voltage is detected. Nakao’s conventional prior art example includes a stopping period that occurs because the discharge extinction or finishing voltage is detected. In either case, a stopping period is provided to allow the computer system to sufficiently protect data and avoid improper operation that may result in errors.

156. Fourth, the combination of Nakao with Nishida’s system or the combined system of Nishida and Harari would have applied a known technique to resolve a known problem recognized in Nishida. Nishida described that protecting and preserving data during a power outage and system shutdown was a known problem. Nishida disclosed that after a power outage “the data on the main

memory is urgently transferred to a non-volatile external recording device using the power supply for the backup to protect data.” (Nishida, ¶2 (INTEL-1006).)

Nishida also taught that “if the charged amount of the storage battery is insufficient to transfer all of the data of the main memory, there is a problem that only a portion of the data of the main memory is backed up.” (Nishida, ¶5 (INTEL-1006).) Nishida further disclosed that “[b]ecause there is a limited amount of charge in the storage battery 110, it is necessary to shut down the computer system.” (Nishida, ¶4 (INTEL-1006).) Nishida’s backup data transfer process may be executed even if the amount of data to be transferred exceeds the memory backup possible amount. (Nishida, ¶15 (INTEL-1006).) Nakao’s over-discharge protection approaches provide a viable implementation that assures an orderly shutdown of the computer system, as required by Nishida, while protecting and preserving data, and maintaining its reliability, by imposing a stopping period before shutdown that avoids errors and malfunctions as the backup power decreases toward an insufficient level and later to zero. (Nakao, 1:5-13 (INTEL-1007).)

157. Fifth, a POSITA would have been motivated to combine Nakao with Nishida’s system or the combined system of Nishida and Harari to substitute Nishida’s computer system shutdown process initiated at the time of a power outage with Nakao’s approach based on detecting power supply discharge levels.

Nishida's and Nakao's teachings establish that both approaches were known. The proposed substitution would have had the foreseeable result that a computer system shutdown in Nishida's system, or the combined system of Nishida and Harari, would have begun based on detecting the output level of the power supply, Nishida's super-capacitors 110. It would have been straightforward to use Nakao's approach. Nishida includes power amount monitoring means 114 that "monitor[s] the current charge amount" of super-capacitors 110 and "report[s] it to the CPU 101." (Nishida, ¶11 (INTEL-1006).) A POSITA would have used the power measurements from power amount monitoring means 114 to detect the output voltage of super-capacitors 110 and begin the shutdown process as described in Nakao's two embodiments (based on detecting a discharge finishing voltage VL) and conventional prior art example (based on detecting the remaining voltage in the power supply). (Nakao, 1:38-46, 3:41-47, 5:47-53 (INTEL-1007).)

c) The reasonable expectation of success in combining Nakao with Nishida (including in further combination with Harari)

158. A POSITA would have also expected success in combining Nakao with Nishida or the combined system of Nishida and Harari. The combination would have yielded predictable results. As explained in ¶¶131, 152, and 133-140, the Nishida system and Nakao system shared many similarities: both are concerned with protecting data in computers; both utilize a backup power supply with a finite

amount of stored energy; and both monitor the decreasing discharge voltage of power supplies. Moreover, both Nishida and Nakao use power monitoring mechanisms to detect energy remaining in the backup power supply. Nishida's power amount monitoring means 114 monitors the current charge amount in its super-capacitors 110. (Nishida, ¶11 (INTEL-1006).) Like Nishida's power amount monitoring means 114, a voltage detector 2 is used by Nakao to monitor the voltage level of the backup power supply. (Nakao, 3:15-63, 4:37-5:5, 6:4-29 (INTEL-1007).) Further, both Nishida and Nakao used switches that electrically connect and disconnect the backup power supply from the load. For example, in Nishida, when power switching switch 108 is configured to the external power supply side on the left, super capacitors 110 are disconnected from computer unit 100, and when power switching switch 108 is switched to the backup power supply side on the right, super capacitors 110 are connected to computer unit 100. (Nishida, ¶¶3-4, 13, 15, Figure 1 (INTEL-1006).) In Nakao, when switching portion 1 is switched to ON, it electrically connects the electric supply to battery B, and when switching portion 1 is switched to OFF, it electrically disconnects the electric supply from battery B. (Nakao, 1:23-32, 3:17-47, 4:21-29, 4:59-63.)

159. A POSITA would have used any of Nakao's over-discharge protection approaches from the first embodiment, the second embodiment, or the prior art example in Nishida's computer system based on existing structures

disclosed in Nishida. Nishida's power amount monitoring means 114 would have been used in the same manner as Nakao's voltage detector 2 to monitor the discharge level of the backup power supply, super-capacitors 110. Nishida's power switching switch 108 would have been used to discontinue the supply of power to computer unit 100 (the load for super-capacitors 110) in a manner similar to Nakao's switching portion 1, which stops the supply of power to electronic apparatuses and instruments Z. In addition, a POSITA would have implemented a controller like Nakao's the controllers associated with the first and second embodiments in Nishida to send and receive signals relating to Nishida's power amount monitoring means 114 (the component that monitors backup power supply discharge) and CPU 101 (the component that can signal the controller to turn off the switch and discontinue power, as described in Nakao's second embodiment). The combinations of Nishida's system, or the combined system of Nishida and Harari, with Nakao's first embodiment, second embodiment, and prior art example are described in further detail below.

160. A POSITA would have had a reasonable expectation of success in incorporating aspects of Nakao's conventional prior art example shown in Figure 5 in Nishida or the combined system of Nishida and Harari. Annotated and modified Figure 1 from Nishida reproduced below shows an example of the combination between Nishida's computer system and Nakao's conventional prior art example.

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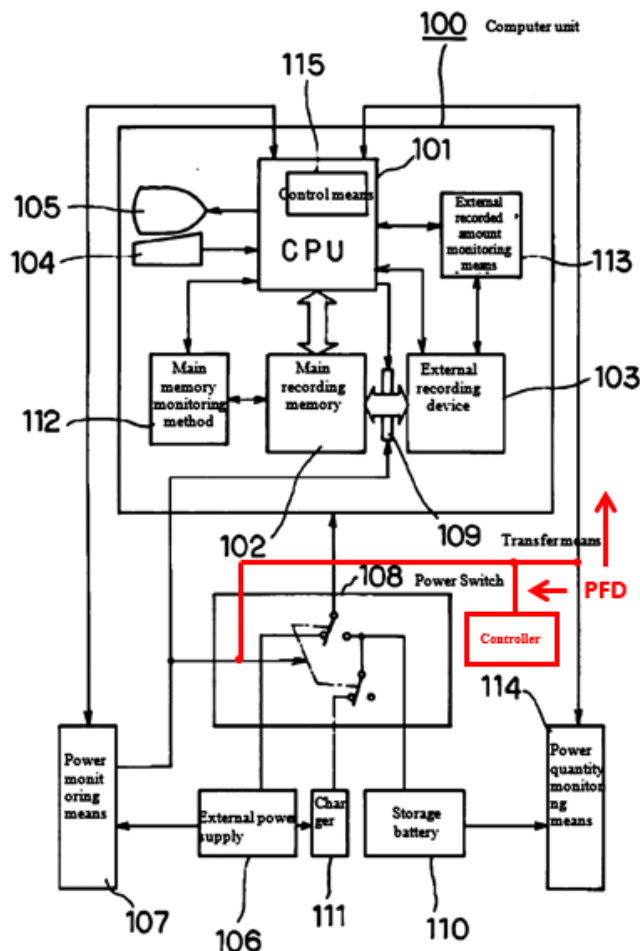


means 114 to detect a discharge extinction or finishing voltage VL as super-capacitors 110 discharge power to computer unit 100. Power amount monitoring means 114 would have then signaled power switching switch 108 to move to the external power supply side on the left, resulting in the super-capacitors being electrically disconnected from computer unit 100.

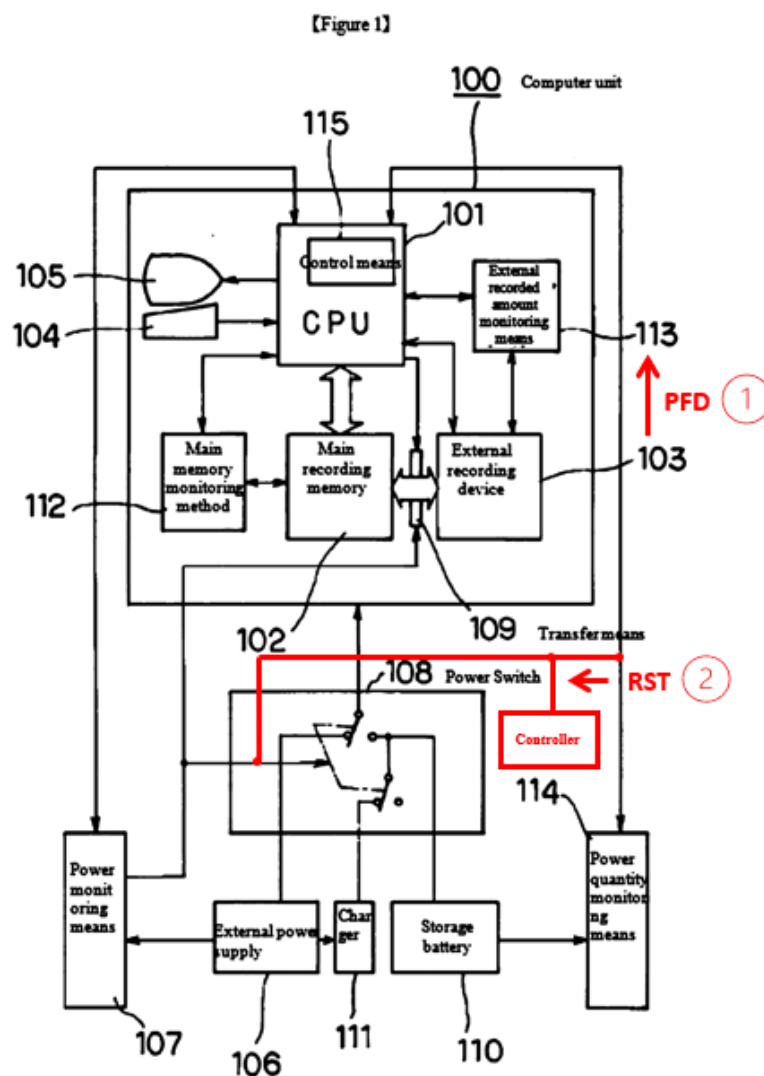
161. A POSITA also would have had a reasonable expectation of success when applying teachings relating to Nakao's first embodiment shown in Figure 1 to Nishida's computer system. I have annotated and modified Figure 1 from Nishida and reproduced below to show an exemplary combination. A red signal line connecting power amount monitoring means 114, CPU 101, and power switching switch 108 and a controller and a related red signal line have been added to the figure. Referring to the first embodiment, Nakao disclosed that "[w]hen the battery voltage becomes lower than the discharge finishing voltage VL, the voltage detector 2 is driven to output a discharge finishing signal PFD.... [T]he over-discharge detection output is delayed for the predetermined time Td at the discharge controller 3 and its delay output signal S0 will make the switching portion 1 of the next stage change to an OFF state and then the electric power supply to the external apparatuses and instruments Z is stopped after the predetermined delay time Td from the over-discharge detection." (Nakao, 3:32-47 (INTEL-1007).) Based on those disclosures, a POSITA would have used power

amount monitoring means 114 to detect a discharge extinction or finishing voltage VL from the output of super capacitors 110. Power amount monitoring means 114 would have transmitted a PFD signal to CPU 101 along the existing connection between power amount monitoring means 114 and CPU 101. The signal also would have been sent to the controller. The signals and directions of transmission are represented with red arrows. Next, the controller would have instructed power switching switch 108 to move to the external power supply side on the left, which would have electrically disconnected computer unit 100 and super-capacitors 110.

【Figure 1】



162. A POSITA would have had a reasonable expectation of success in combining features from Nakao's second embodiment shown in Figure 2 with Nishida's computer system. Annotated and modified Figure 1 from Nishida reproduced below shows one potential way to combine Nakao's second embodiment and Nishida's computer system. Nakao's first (Figure 1) and second



(Figure 2) embodiments are similar. Like the combination involving Nakao's first embodiment, the combination based on Nakao's second embodiment includes the

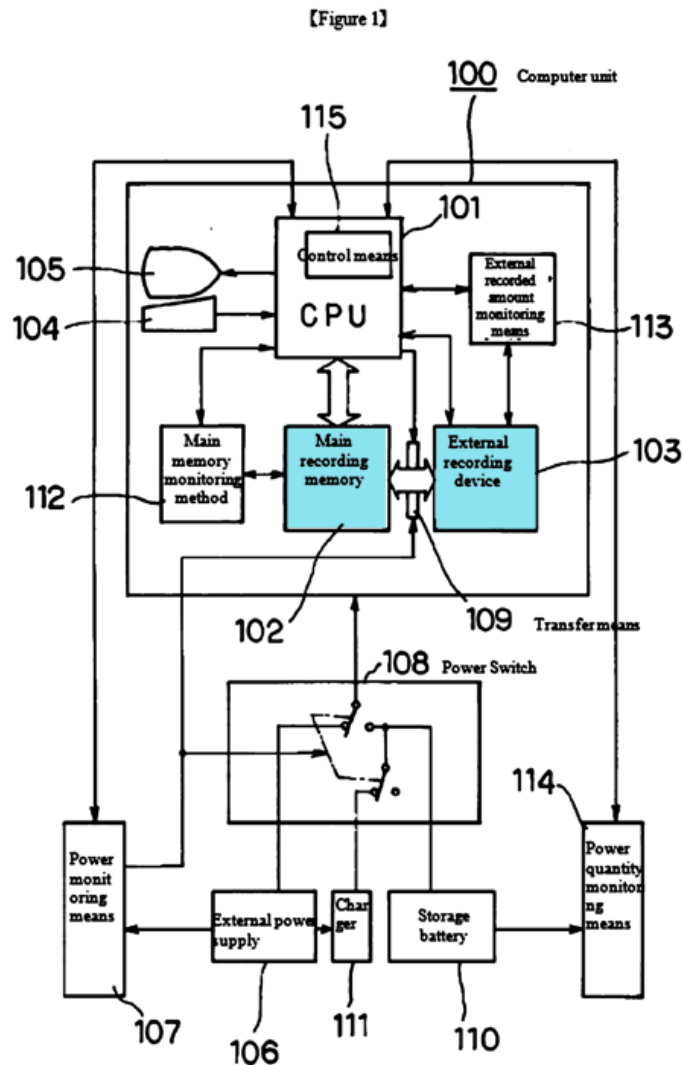
addition of signal lines and a controller, which are shown in red. Regarding the second embodiment, Nakao disclosed “[w]hen the discharge is continued to the point where the battery voltage is lower than the discharge finishing voltage VL, the voltage detector 2 is driven to transmit the discharge finishing signal PFD to thereby require the external apparatuses and instruments to stop the power supply.... When the external apparatuses and instruments recognize the discharge-finish of the battery B, a predetermined stop operation (data-save operation, etc.) is executed and thereafter a power cut-out signal RST is transmitted to the battery, package. When the power cut-out signal RST is input to the remote controller 4, an OFF output signal S1 is output from the output side to the switching portion 1 so that the power supply to the external apparatuses and instruments Z is stopped.” (Nakao, 4:47-63 (INTEL-1007).)

163. Based on these disclosures, a POSITA would have used power amount monitoring means 114 in Nishida to detect a discharge extinction or finishing voltage VL being provided from super-capacitors 110. Power amount monitoring means 114 would have then transmitted a PFD signal to CPU 101 through the existing connection between the two components. As shown in the figure above, the PFD signal is labeled “1” and is sent to CPU 101. After receiving the PFD signal, CPU 101 would have prepared for shutdown and sent an RST signal to the controller once preparations were complete. The RST signal is labeled

“2” in the figure above and is shown as sent to the controller. The RST signal would have caused the controller to provide a signal to power switching switch 108 to orient the switch to the external power supply side on the left, resulting in the electrical disconnection of super-capacitors 110 and computer unit 100.

B. Claim 2: “*The method of claim 1 wherein the computing engine comprises a[t] least one volatile memory and at least one non-volatile memory.*”

164. As for claim 1, the combined system of Nishida and Nakao (including in further combination with Harari) rendered claim 2 obvious. As discussed in ¶¶115-117 regarding limitation 1.pre, Nishida’s computer system includes a “*computing engine*” with “*volatile memory*.” Nishida disclosed that “[t]he computer unit 100 consists of ... a volatile main recording memory 102.” (Nishida, ¶3 (INTEL-1006).) As also discussed in ¶¶116-123 regarding limitation 1.pre, Nishida disclosed a “*non-volatile memory*” in the form of non-volatile external recording device 102 and also rendered “*non-volatile memory*” obvious when combined with Harari. (Nishida, ¶¶3, 7, 15 (INTEL-1006); Harari, 1:35-36 (INTEL-1024).) Annotated Figure 1 of Nishida reproduced below shows volatile main recording memory 102 and non-volatile external recording device 103 (which also would have been implemented as Harari’s EEPROM) in blue.



C. **Claim 3:** *“The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”*

165. Similar to claim 2, the combined system of Nishida and Nakao (including in further combination with Harari) rendered claim 3 obvious. As explained in ¶¶128-129 regarding limitation 1.b, Nishida disclosed that “if an abnormality is detected in the supply voltage from the external power supply, **the**

data on the main memory is urgently transferred to a non-volatile external recording device using the power supply for the backup to protect data.” (Nishida, ¶2 (INTEL-1006).) Nishida also taught that this data transfer involved “**completely evacuat[ing]**” the data from volatile main recording memory 103 to non-volatile external recording memory 103 (which would also have been implemented as Harari’s EEPROM).

D. Claim 6: “*The method of claim 3 wherein the activating step (a) further comprises: (a1) reversing the flow of current between the computing engine and the plurality of super capacitors; and (a2) discharging current from the plurality of super capacitors to the computing engine.*”

166. The combined system of Nishida and Nakao (including in further combination with Harari) rendered claim 6 obvious. As discussed in ¶¶124-127 regarding limitation 1.a, Nishida taught the “*activating step*” that is claimed in limitation 1.a. The claim limitation of claim 6 includes two sub-steps that are part of the “*activating step*”: (1) “*reversing the flow of current between the computing engine and the plurality of super capacitors*” (sub-step (a1)) and (2) “*discharging current from the plurality of super capacitors to the engine*” (sub-step (a2)).

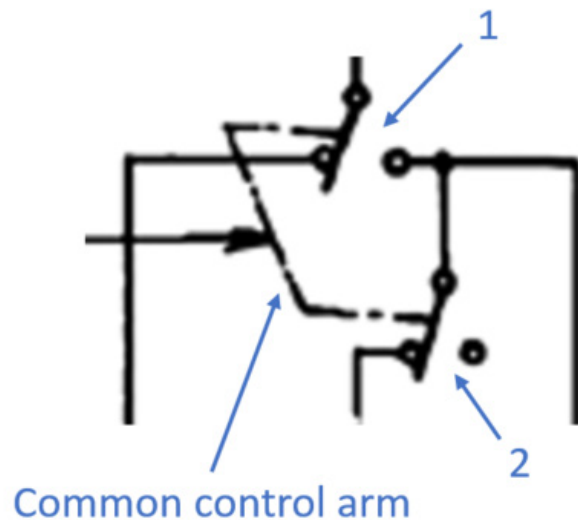
167. I understand that the district court gave sub-step (a1) its “plain-and-ordinary meaning.” (Claim Construction Order and Memorandum in Support Thereof, 24 (INTEL-1018).) Patent Owner proposed that construction to the court. (Claim Construction Order and Memorandum in Support Thereof, 46 (INTEL-

1018).) I further understand that Patent Owner argued that “*reversing*” means a change in flow of current between “when power is supplied by the [external power supply] to the computing engine and **to the capacitors** to charge them” and “when power is supplied **from the capacitors** to the computer engine.” (BiTMICRO LLC’s Responsive Claim Construction Brief, 11 (INTEL-1011).) Patent Owner further explained that in the first scenario current goes “toward the capacitors” while in the second scenario current flows “from” the capacitors. (BiTMICRO LLC’s Responsive Claim Construction Brief, 11 (INTEL-1011) (emphasis in original).)

168. Under Patent Owner’s construction of “*reversing*,” the combination of Nishida and Nakao (including in further combination with Harari) rendered sub-step (a1) obvious. Nishida disclosed two potential power supplies for providing power to computer unit 100: external power supply 106 and backup power supply 110. (Nishida, ¶¶2-4 (INTEL-1006).) Nishida also taught power switching switch 108 connected to external power supply 106, backup power supply 110, and computer unit 100. (Nishida, ¶¶3-4, 13, 15, Figure 1 (INTEL-1006).)

169. Nishida’s power switching switch 108 consists of two switches (upper switch and lower switch) that are connected by a common control arm. (Nishida, Figure 1 (INTEL-1006).) The annotated and enlarged portion of Figure 1 of Nishida reproduced below shows the upper switch (labeled “1”), the lower switch

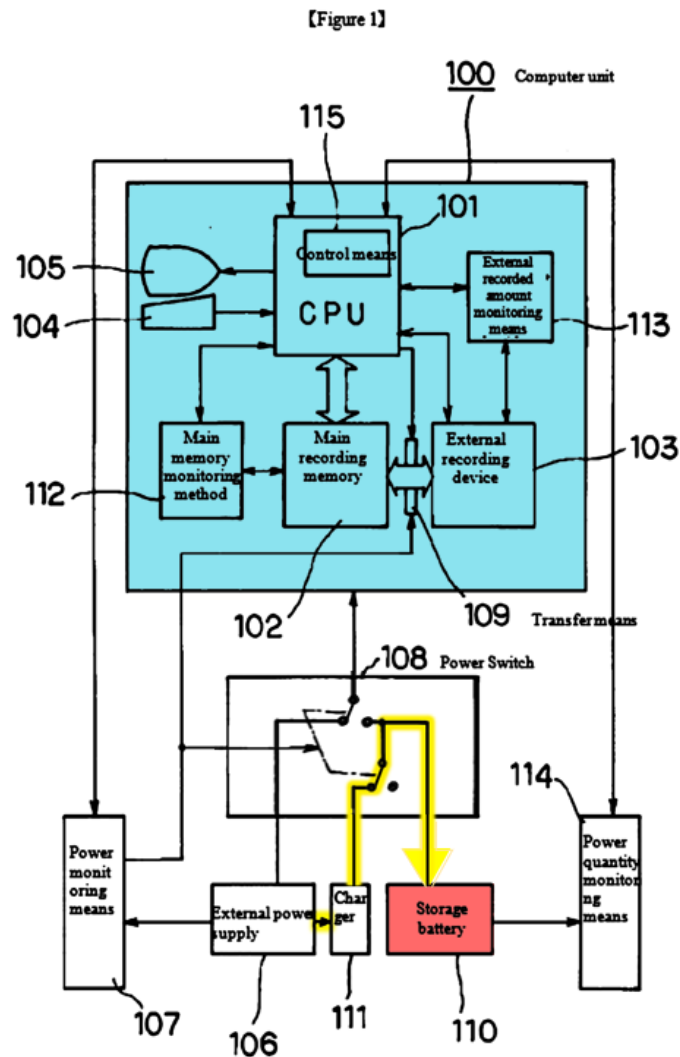
(labeled “2”), and the C-shaped common control arm of power switching switch 108. The common control arm controls both the upper switch and the lower switch at the same time, causing both switches to move together to the left or to the right. The upper and lower switches must therefore be operated in unison. Nishida’s design does not allow the upper and lower switches to be separately controlled. There is no scenario in which one switch is set to the terminal on one side (e.g., the left-side terminal) and the other switch is switched to the terminal on the opposite side (e.g., the right-side terminal). Current flows through the upper and lower switches but not through the common control arm.



170. As shown in Figure 1 of Nishida, the top of power switching switch 108 is connected to computer unit 100 and the bottom of power switching switch 108 is connected to the two types of power supplies, external power supply 106 and backup power supply 110 through charger 111. Nishida disclosed that “power switching switch 108 switches the supply of power to the computer unit 100 between the external power supply 106 and the [backup power supply] 110.” (Nishida, ¶3 (INTEL-1006).) “[T]he computer system is normally operated with

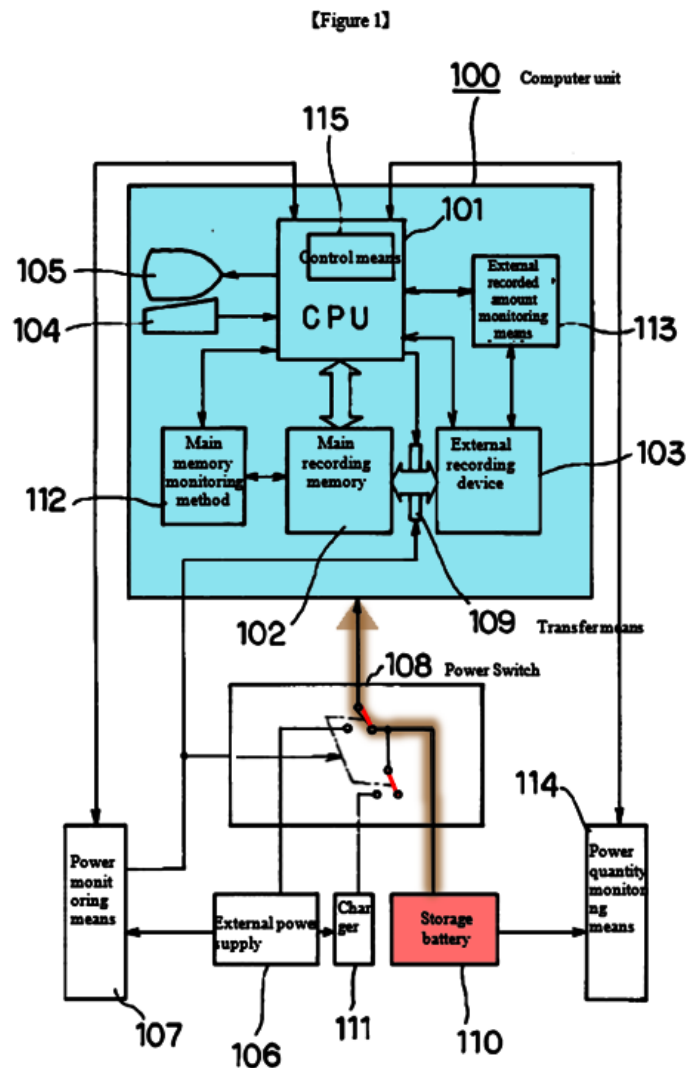
power from the external power supply 106.” (Nishida, ¶4 (INTEL-1006).) In that case, “power switching switch 108 is switched to the external power supply 106 side” (Nishida, ¶13 (INTEL-1006).) The upper and lower switches within power switching switch 108 are configured to their left-side terminals. As a result, computer unit 100 receives power from external power supply 106 through the current path established by power switching switch 108.

171. Nishida disclosed that backup power supply 110 can be super-capacitors. (Nishida, ¶2 (INTEL-1006).) In that implementation, super-capacitors 110 are “maintained in a charged stated by the charger 111.” (INTEL-1006 ¶4; *see also* ¶13.) Nishida’s “charger 111 [is] for charging the [backup power supply] 110 by power from the external power supply 106.” (Nishida, ¶3 (INTEL-1006).) As shown in annotated Figure 1 of Nishida reproduced below, charger 111 is connected in series between external power supply 106 and super-capacitors 110. When power switching switch 108 is switched to the external power supply side on the left, current flows from external power supply 106 to charger 111 and then into super-capacitors 110. The current flow is indicated with a yellow arrow. Current moves **toward** super-capacitors 110. Annotated Figure 1 of Nishida reproduced below shows computer unit 100 in blue and super-capacitors 110 in red.



172. Nishida disclosed that “if the supply of power from external power sources is interrupted due to a power outage” (Nishida, ¶2 (INTEL-1006)), power switching switch 108 “switches to the [backup power supply] side” on the right. (Nishida, ¶3 (INTEL-1006).) Annotated and modified Figure 1 of Nishida reproduced below shows the power switching switch 108 configured to the backup power supply side on the right. The reconfigured switches are indicated with two red lines. In this configuration, super-capacitors 110 supply “power to the

computer unit 100” (Nishida, ¶3 (INTEL-1006); *see also* ¶¶4, 7, 15.) Current flows **away from** super-capacitors 110 and toward computer unit 100. The direction of current flow is marked in brown in the modified and annotated Figure 1 of Nishida reproduced below. These teachings disclosed the “*reversing*” sub-step under Patent Owner’s construction because, during normal operation, current flows toward super-capacitors 110, but during a power outage, current flows away from super-capacitors 110.



173. The current flows in Nishida are like the current flows disclosed in the '939 patent. The '939 patent discloses that external power source 22 “charges the super-capacitors 34” using current that flows from external power source 22 to power isolator 26 to DC-DC up-converter 32 and eventually into super-capacitors 34. ('939 patent, 3:39-46 (INTEL-1001).) Current also flows from external power source 22 to power isolator 26 and into computing engine 28. Annotated Figure 1 reproduced below shows super-capacitors 34 in red and computing engine 28 in blue. The current flows from external power source 22 **toward** super-capacitors 34

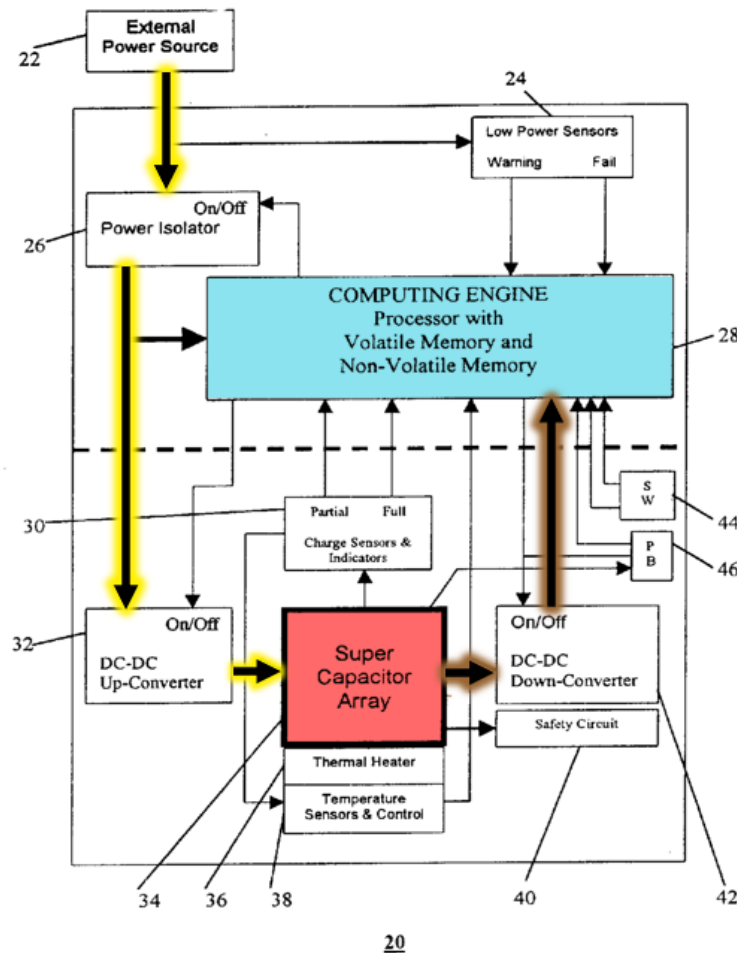


FIGURE 1

when super-capacitors 34 are being charged by external power source 22 through DC-DC up-converter 32. The figure shows the current flow from external power source 22 to supercapacitors 34 using arrows with yellow outlining.

174. When the computer system in the '939 patent “detects that the external system power has fallen below a certain threshold amount,” “the up-converter is deactivated” and “the down-converter is activated.” ('939 patent, 6:20-27 (INTEL-1001).) At that point, “super-capacitors then begin to slowly discharge current to the computer system through the down-converter.” ('939 patent, 6:28-31 (INTEL-1001).) The '939 patent refers to this process as “revers[ing] the flow of current between the computer system and the super-capacitors.” ('939 patent, 6:27-28 (INTEL-1001).) Annotated Figure 1 of the '939 patent reproduced above shows current flow after a power interruption. Current flows **from** super-capacitors 34 to down-converter 42 and eventually into computing engine 28. The figure shows the current flow from super-capacitors 34 to computing engine 28 using arrows with brown outlining.

175. The combination of Nishida's system, or the combined system of Nishida and Harari, and Nakao also rendered “*discharging*” sub-step (a2) obvious. As discussed in ¶¶116-117 and 124-125 regarding limitations 1.pre and 1.a, Nishida's system includes both a “*computing engine*” and “*a plurality of super capacitors,*” as required by sub-step (a2). Nishida further disclosed that “if the

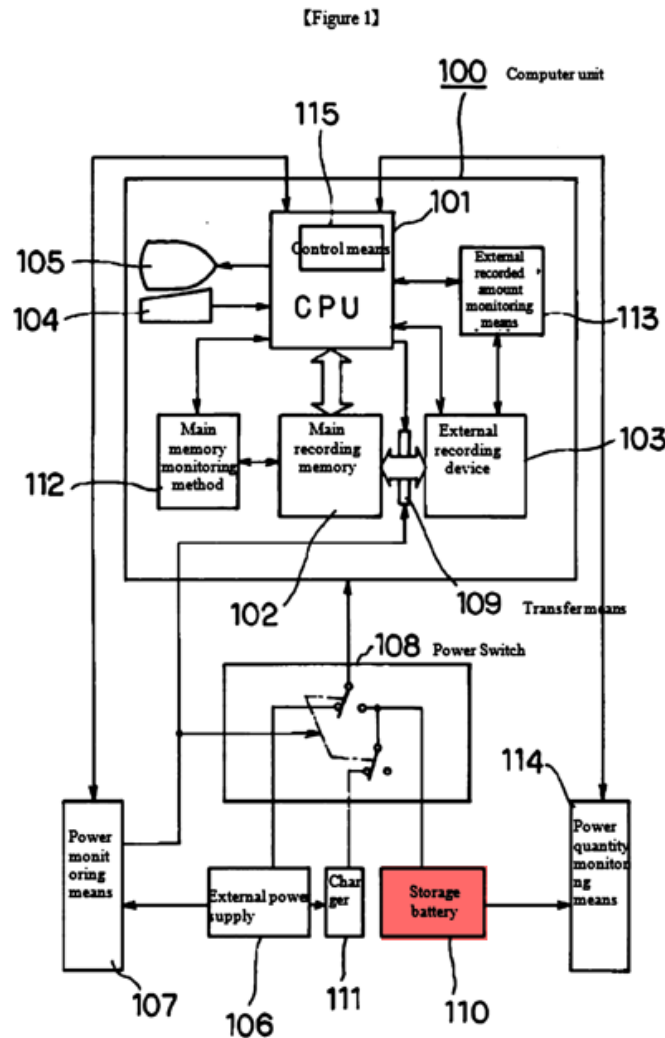
supply of power from external power sources is interrupted due to a power outage,” power switching switch 108 is configured to the backup power supply side on the right. (Nishida, ¶3-4, 7, 15 (INTEL-1006).) Changing the switch’s orientation creates an electrical connection that allows backup super-capacitors 110 to discharge current and provide power to computer unit 100. Computer unit 100 corresponds to, or includes structures (CPU 101, main recording memory 102, and external recording memory 103 or Harari’s EEPROM) that correspond to, the claimed “*computing engine*.”

IV. Claims 1-3, 6, 10-12, and 15 would have been obvious over the combination of Nishida, Ergott, and Pilukaitis (including in further combination with Harari)

A. The combination of Ergott and Nishida (including in further combination with Harari)

176. As discussed in ¶65, the equation $U = \frac{1}{2} C (\Delta V)^2$ (Serway, 581 (INTEL-1038)) determined that energy (U) stored in capacitors is directly related to the square of the voltage (ΔV) across the capacitors, and one way to increase the energy stored is to increase the voltage across the capacitors. As further discussed in ¶¶66-68, many circuits that incorporated capacitors as backup power supplies also implemented voltage up-converters to increase the capacitor voltage and voltage down-converters to reduce the capacitor supply voltage level to be suitable for computer circuits. Nishida described a backup power supply 110 that

“consist[s] of ... supercapacitors.” (Nishida, ¶2 (INTEL-1006).) Charger 111 charges those super-capacitors. (Nishida, ¶¶3, 13 (INTEL-1006).) A POSITA would have been motivated to include an up-converter and a down-converter in the Nishida system (including as combined with Harari) to increase the energy available in Nishida’s super-capacitors 110. Annotated Figure 1 from Nishida reproduced below shows super-capacitors 110 in red and charger 111, which is connected to super-capacitors 110.

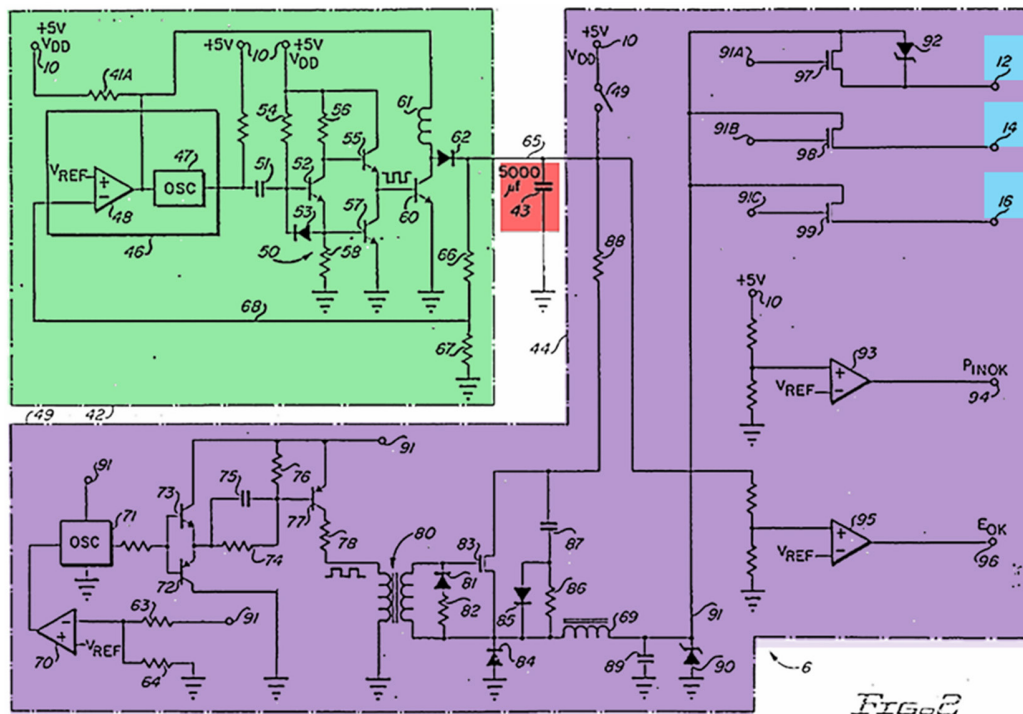


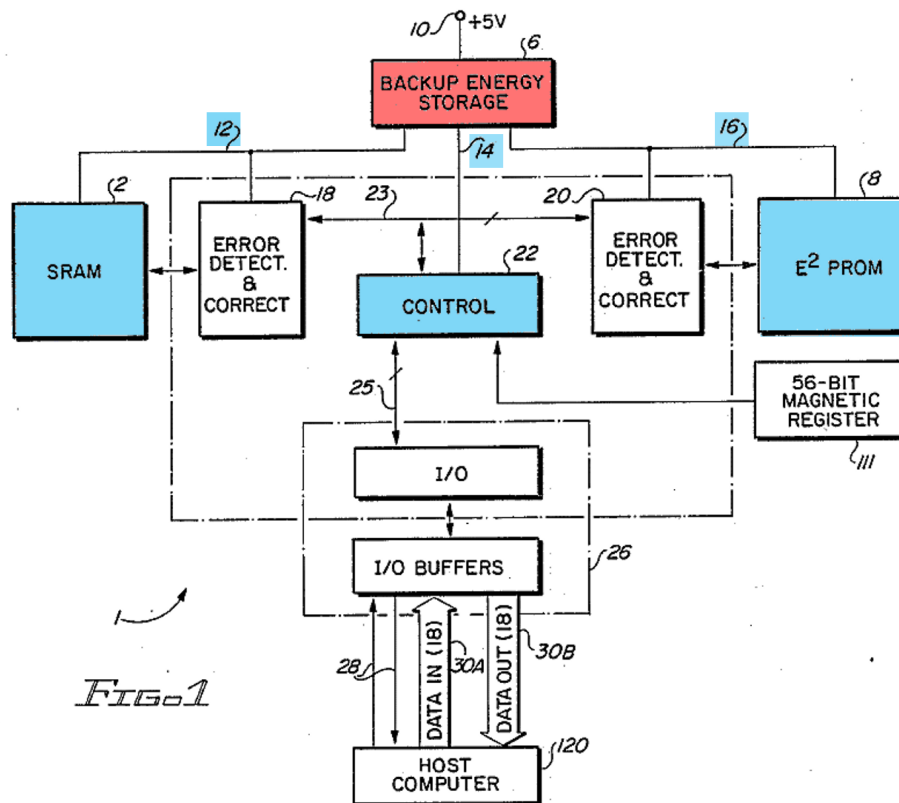
1. The teachings of Ergott

177. Ergott described a memory system that “utilizes a **volatile SRAM and a non-volatile backup store** implemented by means of E²PROMs in which data is transferred from the SRAMs to the E²PROMs when the power is turned off or interrupted by **using high voltage energy stored in a backup capacitor to provide operating power** for at least a long enough period of time to effectuate reliable transfer of data from the SRAM to the E²PROM.” (Ergott, 3:1-10 (INTEL-1008).)

178. Ergott taught using a voltage up-converter to boost the voltage of the backup capacitor and a voltage down-converter to convert the boosted capacitor voltage into a suitable voltage level (e.g., 5 volts) for the components of the system. When external power is available, “**a voltage up converter 42 []** performs the function of **boosting the external 5 volt power supply voltage** on conductor 10 **to charge up a 1,000 to 5,000 microfarad backup capacitor 43** to approximately 100 volts to provide a backup voltage on backup capacitor terminal 65 to power the non-volatile memory system 1.” (Ergott, 6:2-68 (INTEL-1008).) When external power is interrupted, the “100 volts produced on conductor 65 ... is converted back down to the internal 5 volt supply voltage.” (Ergott, 7:1-6 (INTEL-1008); *see also* 5:7-13.) Ergott relies on down converter 44 to perform that conversion: “discharging current from the backup capacitor by means of a

voltage down converter circuit to supply the internal supply voltage.” (Ergott, claims 2, 12 (INTEL-1008); *see also* 7:48-8:10.) Annotated Figure 2 of Ergott reproduced below shows backup capacitor 43 in red, up-converter 42 in green, and down-converter 44 in purple. The “100 volts produced on conductor 65 by backup capacitor 43” feeds into down converter 44 which converts that voltage into “the internal 5 volt supply on conductor 91” distributed “to conductors 12, 14, and 16, respectively.” (Ergott, 7:6-11 (INTEL-1008).) Conductors 12, 14, and 16 appear in blue. Conductors 12, 14, and 16 are connected to SRAM 2, control 14, and E²PROM 8, respectively, as shown in annotated Figure 1 of Ergott further reproduced below. In that figure, backup energy storage 6 appears in red and conductors 12, 14, and 16, SRAM 2, control 14, and E²PROM 8 all appear in blue.





2. The motivation to combine Ergott with Nishida (including in further combination with Harari)

179. A POSITA would have been motivated to modify Nishida's system (including in combination with Harari) to incorporate a voltage up-converter and a voltage down-converter. Ergott taught substantial advantages provided by an up-converter and a down-converter. Ergott disclosed that using an up-converter "increase[s] the amount of backup energy storage." (Ergott, claims 2, 12 (INTEL-1008).) The up-converter 42 "boost[s]" an external power supply of five volts to charge up "backup capacitor 43 to approximately 100 volts." (Ergott, 6:62-68 (INTEL-1008).) This boosting technique increases the backup voltage in the

capacitors by 20x. That increase in voltage also increases the amount of energy storage in the capacitor for use when backup power is needed. As discussed in ¶¶65-66, it was known that “potential energy stored in the capacitor” is calculated using the following equation:

$$U = \frac{Q^2}{2C} = \frac{1}{2} Q \Delta V = \frac{1}{2} C (\Delta V)^2$$

(Serway, 581 (INTEL-1038).) In the equation above, C is the capacitor capacitance and ΔV is the capacitor voltage. Since the potential energy stored in the capacitor is directly proportional to the square of the capacitor voltage, the 20x increase in backup capacitor voltage provided by voltage up-converter 42 results in a significant 400x increase ($20^2 = 400$) in the energy stored in backup capacitor 43.

180. Ergott further disclosed that when an external power interruption occurs, the capacitor “slowly discharg[es]” from a peak of 100 volts, and voltage down-converter 44 reduces that gradually decreasing output voltage of backup capacitor 43 “back down to the internal 5 volt supply voltage.” (Ergott, 7:1-6 (INTEL-1008); *see also* 7:48-8:10, claims 2, 12.) Ergott explicitly taught the advantage of using high-voltage energy storage: “high voltage energy stored in a backup capacitor [] **provide[s] operating power for at least a long enough period of time to effectuate reliable transfer of data from the [volatile] SRAM to the [non-volatile] E²PROM.**” (Ergott, 3:1-10 (INTEL-1008).) Based on the

specific advantages identified in Ergott, a POSITA would have used a voltage up-converter to charge Nishida's super-capacitors to a higher voltage level to obtain an increase in stored energy.

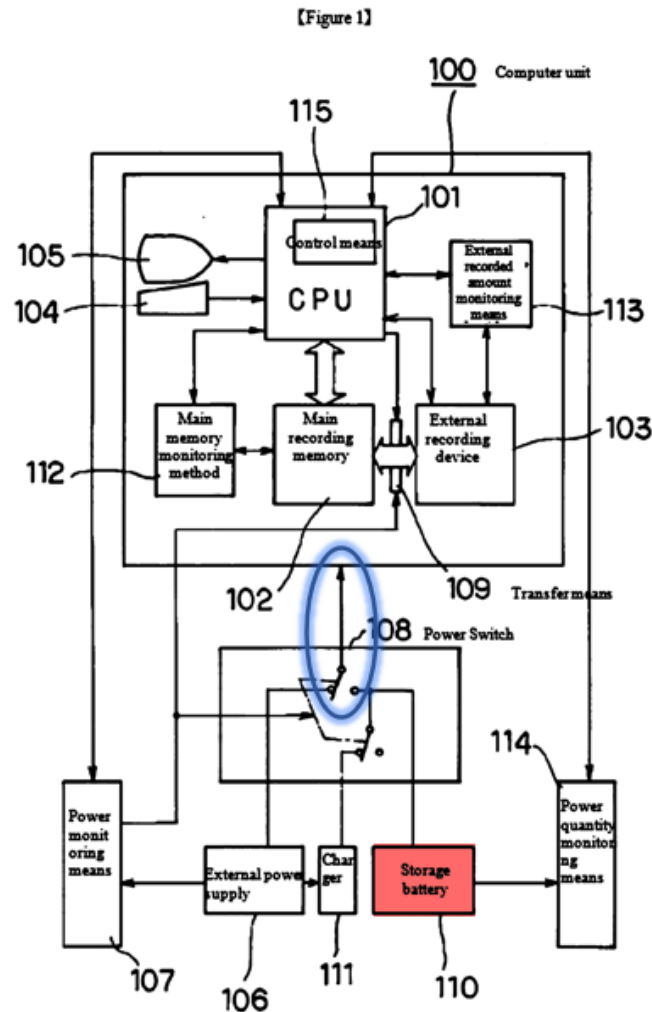
181. Nishida identified problems caused by insufficient backup power. If backup power runs low, data will only partially be backed up after an outage of external power: “[i]n the conventional computer system with memory backup function described above, **if the charged amount of the storage battery is insufficient to transfer all of the data of the main memory, there is a problem that only a portion of the data of the main memory is backed up.**” (Nishida, ¶¶2, 5 (INTEL-1006).) By contrast, when there is sufficient backup energy, data is completely evacuated from volatile to non-volatile storage, which prevents loss of data. For example, Nishida's computer system “calculates the maximum amount of data (memory backupable amount) that can be transferred from the main recording memory 102 to the external recording device 103 by using only the power from the storage battery 110 when a memory backup must be performed.” (Nishida, ¶14 (INTEL-1006).) Then, if “the amount of data on the main recording memory 102 is less than or equal to the amount of memory backup possible... the data on the main recording memory 102 is completely evacuated to the [non-volatile] external recording device 103.” (Nishida, ¶15 (INTEL-1006).) As such, any transferred data is “protect[ed].” (Nishida, ¶2 (INTEL-1006).) A POSITA reading Nishida would

have understood that backup energy storage limits the amount of data that can be safely transferred. Increasing the backup energy storage would have made it possible to safely transfer more data.

182. Therefore, a POSITA would have sought ways to increase the amount of energy stored in the backup power supply. That would have improved the likelihood of transferring all data from volatile to non-volatile storage in the event of an external power loss. Using a voltage up-converter paired with a voltage down-converter, which is what Ergott disclosed, would have accomplished that objective. The voltage up-converter would have increased the amount of available backup power by boosting the voltage stored in super-capacitors 110.

183. The voltage down-converter also would have been necessary to convert the boosted high voltage level (e.g., 100 V) supplied by the backup super-capacitors into the input voltage level (e.g., 5 V) for use by the components of Nishida's computer system. As discussed in ¶60, the capacitor charging process ceases when the voltage across the capacitor equals the voltage level of the power source. Therefore, absent a voltage up-converter for super-capacitors 110, the fully charged super-capacitors would have the same voltage as external power source 106. Therefore, Nishida taught that both external power supply 100 and super-capacitors 110 supply the same voltage to computer unit 100. Annotated Figure 1 from Nishida reproduced below illustrates that super-capacitors 110 receive power

through charger 111 from external power supply 106, and external power supply 100 and super-capacitors 110 share a common supply line to computer unit 100 that is connected to the top of the upper switch in power switching switch 108. The common supply line is shown within the blue oval.



184. As discussed in ¶162, the upper switch of power switching switch 108 determines whether external power supply 100 or super-capacitors 110 supply power to computer unit 100. (Nishida, ¶¶3-4 (INTEL-1006).) The choice is limited

to one of those options and only one power supply can provide power to computer unit 100 using the common supply line and input of computer unit 100. If the upper switch is configured to the left terminal, external power supply 106 provides power to computer unit 100. If the upper switch is configured to the right terminal, super-capacitors 110 provide power to computer unit 100 at the same input of computer unit 100. Because the two power supplies use the same supply line and the same input into computer unit 100, and there is no indication in Nishida that the power level is altered, the supply provided by super-capacitors 110 must be the same as the supply provided by external power supply 106. In each case, the power supplies provide the input voltage that is required by computer unit 100. As a result, if an up-converter is used to boost the input voltage for super-capacitors 110, a down-converter would also have been used to reduce that voltage to the same voltage super-capacitors 110 would have supplied to computer unit 100 without the up-conversion. That voltage is equal to the voltage that external power supply 106 supplies to computer unit 100.

185. It was known in the art that a computer system has a single voltage input, and five volts was a common value for the voltage input. For example, Ergott disclosed that “SRAM 2 and all of control circuitry 22 are supplied by the normal 5 volt levels.” (Ergott, 13:19-22 (INTEL-1008).) In another example, one of the most prominent microprocessors at the time of the alleged invention, the

Intel 8085 microprocessor, required a “+5 V power supply” for its V_{CC} terminal (the power input). (Stallings, 519 (INTEL-1039).)

186. Further, applying Ergott’s teaching of using an up-converter and a down-converter to Nishida’s system (including in further combination with Harari) would have used a known technique, as reflected in Ergott’s disclosures, to improve a similar system—the system based on Nishida—in the same way that Ergott described. Ergott taught a known technique of using an up-converter to increase the energy stored in a backup capacitor (Ergott, claims 2, 12 (INTEL-1008)) and a down-converter to convert the increased voltage provided to the backup capacitor down to the supply voltage for the computer system (Ergott, 7:48-8:10 (INTEL-1008)).

187. Ergott’s system is also structurally and functionally similar to the Nishida’s system (including in further combination with Harari). The table below summarizes the structural similarities. (Nishida, ¶¶2-3, Fig. 1 (INTEL-1006); Ergott, 4:63-67, 6:20-23 (INTEL-1008).)

Structure	Ergott	Nishida (+ Harari)
Volatile Memory	SRAM 2	Main recording memory 102
Non-Volatile Memory	E ² PROM 8	External recording device 103 EEPROM (Harari)

Structure	Ergott	Nishida (+ Harari)
Backup Power Source	Backup capacitor 43	Super-capacitor 110
Main Control Circuitry	Control circuitry 22	CPU 101

188. Ergott's system is functionally similar to Nishida's system (including in further combination with Harari) because both provide power from backup capacitors to achieve transferring data from a volatile memory to a non-volatile memory. (Nishida, ¶2, (INTEL-1006); Ergott, 5:45-56, 6:62-67 (INTEL-1008).) In addition, Ergott's system and Nishida's system (including in further combination with Harari) are both aimed at ensuring that data in volatile memory is protected during a power outage by reliably transferring all the data in the volatile memory into a non-volatile memory storage. (Nishida, ¶2, (INTEL-1006); Ergott, 3:1-10 (INTEL-1008).) As explained in ¶¶66-68, an up-converter and down-converter pair, as described in Ergott, was a known and implementable technique for increasing backup power and processing time to address the known problem of protecting data jeopardized by a loss of external power. More backup power resolved the issue by provided a longer period of time to transfer data to non-volatile storage after a power loss.

189. A POSITA also would have been motivated to implement an up-converter and down-converter—the approach described in Ergott—in Nishida's

system (or further in combination with Harari) because the combination involved a simple substitution. Nishida's system (or further in combination with Harari) includes charger 111, which provides power to super-capacitors 110 but lacks up-conversion capability. (Nishida, ¶¶3-4, 13 (INTEL-1006).) The system also lacks a down-converter. A POSITA would have substituted the charger 111 with an up-converter and added a corresponding down-converter on the discharge end of super-capacitors 110. Ergott establishes that this approach was known. The implementation adding an up-converter and a down-converter would have accomplished the same functions as Nishida's charger by providing a boosted charge to super-capacitors 110. (Ergott, 6:62-68 (INTEL-1008).) Adding the down-converter would have allowed for reducing the discharge voltage of super-capacitors 110 to the input voltage of computer unit 100. The proposed substitution also would have had the foreseeable results of increasing backup energy and obtaining longer operation time for the system after an external power interruption.

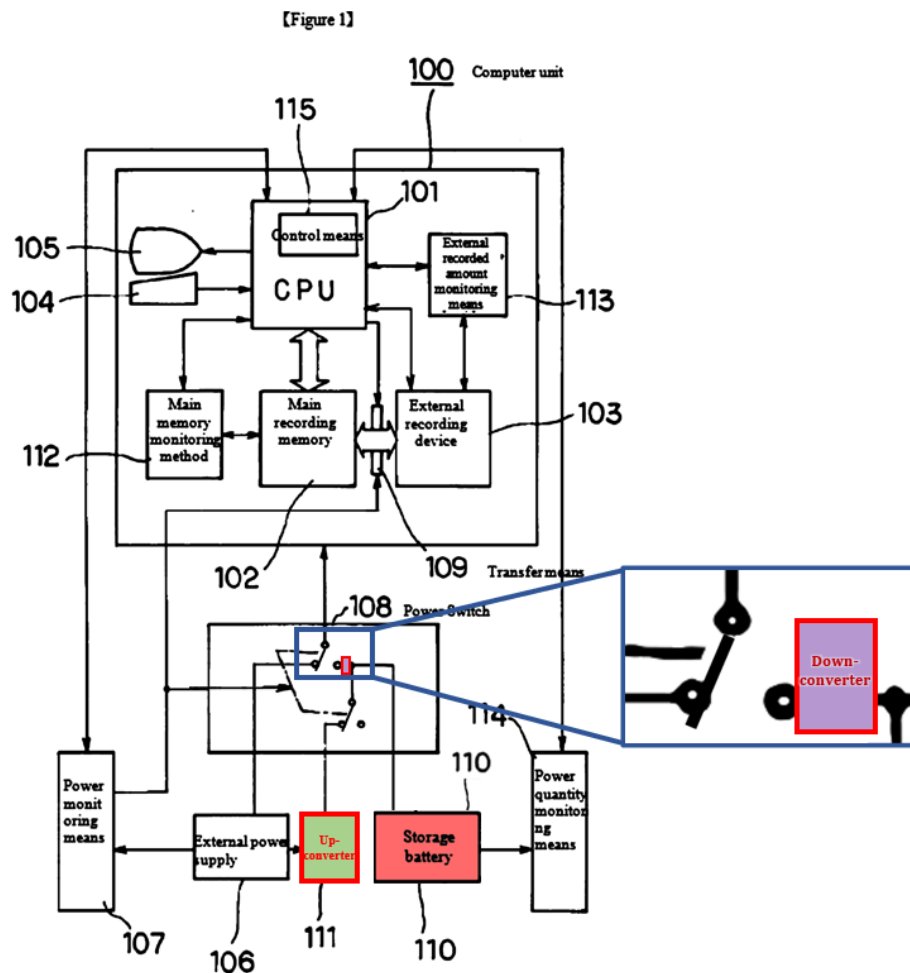
3. The reasonable expectation of success for combining Ergott with Nishida (including in further combination with Harari)

190. Ergott disclosed the known technique of using an up-converter to increase the energy stored in a backup capacitor (Ergott, claims 2, 12 (INTEL-1008)) and a down-converter to convert the voltage from the backup capacitor down to a supply voltage used by computer components (Ergott, 7:48-8:10

(INTEL-1008)). A POSITA would have had a reasonable expectation of success with predictable results when incorporating an up-converter and down-converter into Nishida's system (or further in combination with Harari). For instance, Ergott provided one example of a similar system that implements both an up-converter and down-converter to provide increased capacity for data backup when external power is interrupted. Ergott's system also includes volatile and non-volatile memories, which resembles the computer system of Nishida (including in further combination with Harari). As explained in ¶68, Bruder provides a second example of using an up-converter and down-converter in a system that backs up data after a power loss.

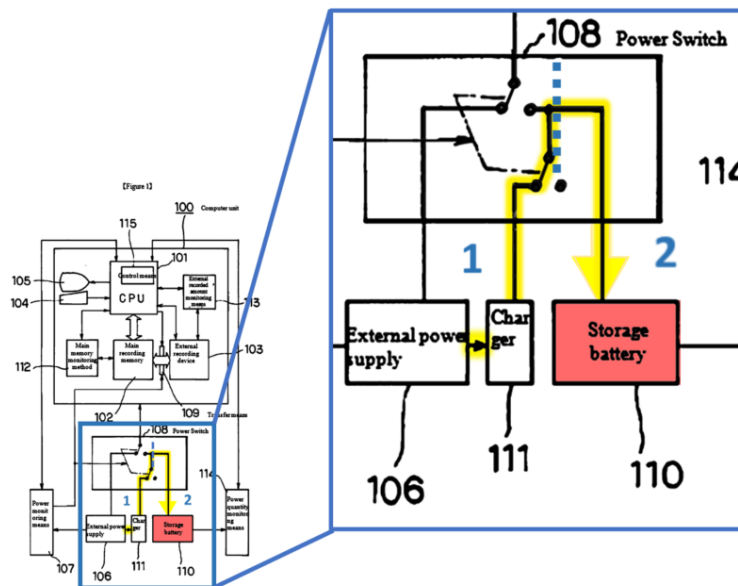
191. Based on these teachings, a POSITA would have understood how to modify Nishida's system (including in further combination with Harari) to add an up-converter and down-converter. First, a POSITA would have replaced charger 111 in Nishida's system (or further in combination with Harari) with an up-converter. The up-converter provides the same charging function but also boosts the voltage of super-capacitors 110 to a higher voltage level. (Ergott, 6:62-68 (INTEL-1008).) In the modified system, the voltage up-converter would have been placed upstream of super-capacitors 110 in the same position previously occupied by charger 111. Second, a POSITA would have added a voltage down-converter between super-capacitors 110 and computer unit 100 to reduce the boosted voltage

level of the super-capacitors to an internal power supply voltage for computer unit 100. The voltage down-converter is positioned downstream from super-capacitors 110. Annotated and modified Figure 1 from Nishida reproduced below shows the voltage up-converter in green, the super-capacitors 110 in red, and the voltage down-converter in purple.



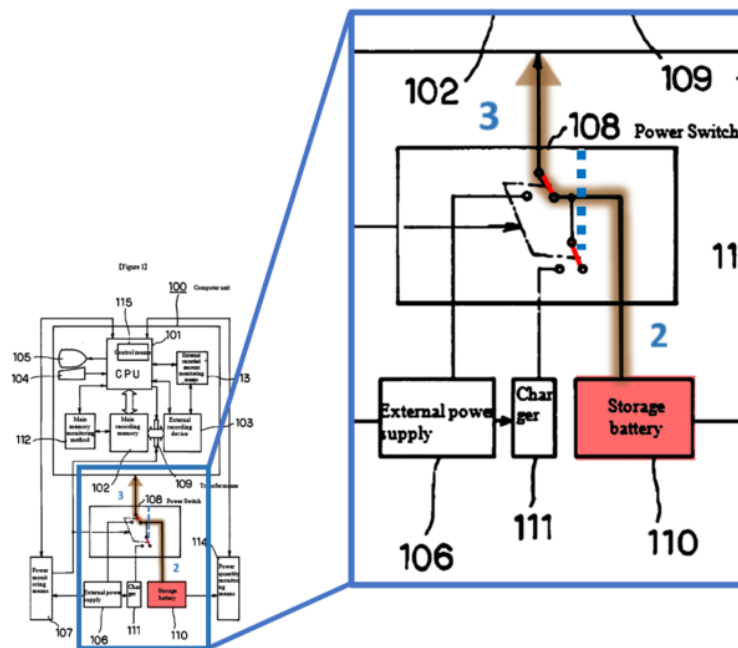
192. The voltage down-converter in Nishida would have been placed as indicated above for a reason. As discussed in ¶171, when Nishida's power switching switch 108 is switched to the external power supply side on the left,

current flows from external power supply 106 to charger 111 and then into super-capacitors 110. Annotated and modified Figure 1 from Nishida reproduced below shows a yellow arrow that indicates the current flow. Super-capacitors 110 appear in red. The path from charger 111 to super-capacitors 110 has two segments. For illustration purposes only, the two segments are separated by a blue dotted line. The first segment (labeled “1”) carries current through the lower switch of power switching switch 108 and toward super-capacitors 110. The second segment (labeled “2”) carries current to supercapacitors 110.



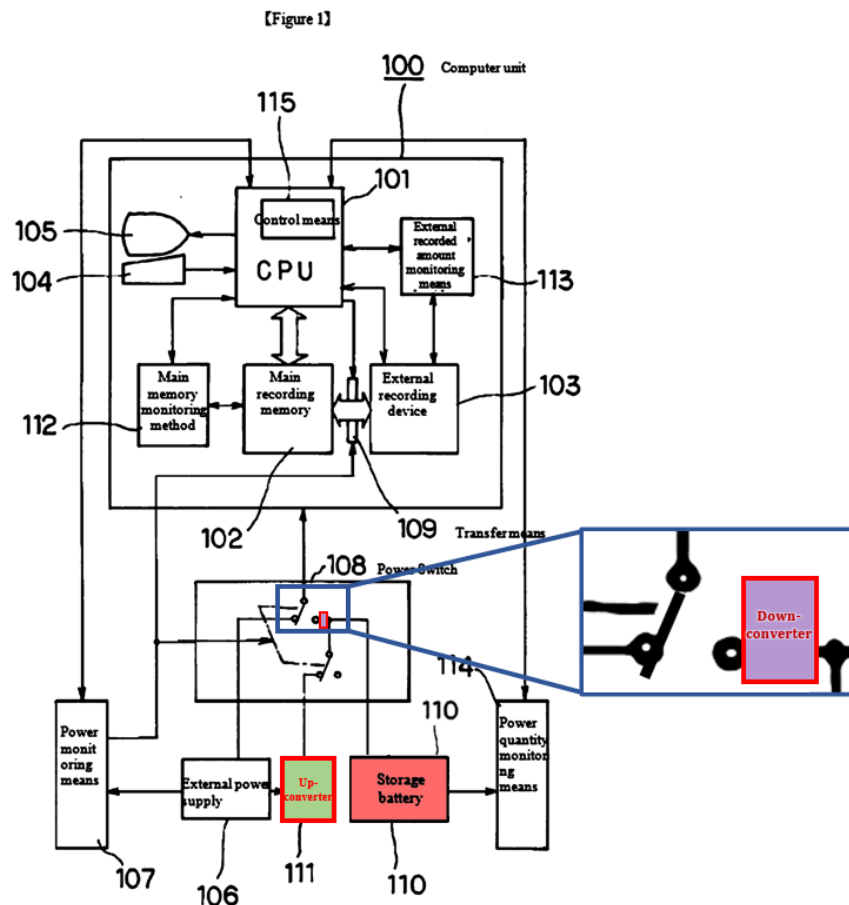
193. Also, as discussed in ¶172, when power switching switch 108 is switched to the backup power supply side on the right, super-capacitors 110 discharge power to computer unit 100. Annotated and modified Figure 1 from Nishida reproduced below shows a brown arrow that represents this current flow.

Super-capacitors 110 again appear in red. The discharge path for super-capacitors 110 has two segments. For illustration purposes only, the two segments are separated by a blue dotted line. The lower segment (labeled “2”) is the same as the second segment used when charging the super-capacitors. The upper segment (labeled “3”) includes a portion to the right of the upper switch of power switching switch 108 and before the blue dotted line that is unique to the super-capacitor discharge path.



194. A POSITA would have placed the voltage down-converter in the portion of segment “3” unique to Nishida’s super-capacitor discharge path. That discharge transmission line carries current towards computer unit 100, and the down-converter would have operated solely on the up-converted super-capacitor discharge voltage. This positioning also would have avoided the external power

transmission line that leaves power switching switch 108 above the upper switch. That transmission line is used by external power supply 106 to supply power to computer unit 100 when power switching switch 108 is configured to the left side. Putting the down-converter on that transmission line would not have made sense because power supplied by external power supply 106 is not converted up to a higher voltage so there is no need for down-conversion. The positioning for the down-converter illustrated in annotated and modified Figure 1 from Nishida reproduced below would have affected only power provided at a high voltage from super-capacitors 110 to computer unit 100, as intended.



B. The combination of Pilukaitis and the combined system of Nishida and Ergott (including in further combination with Harari)

1. The teachings of Pilukaitis

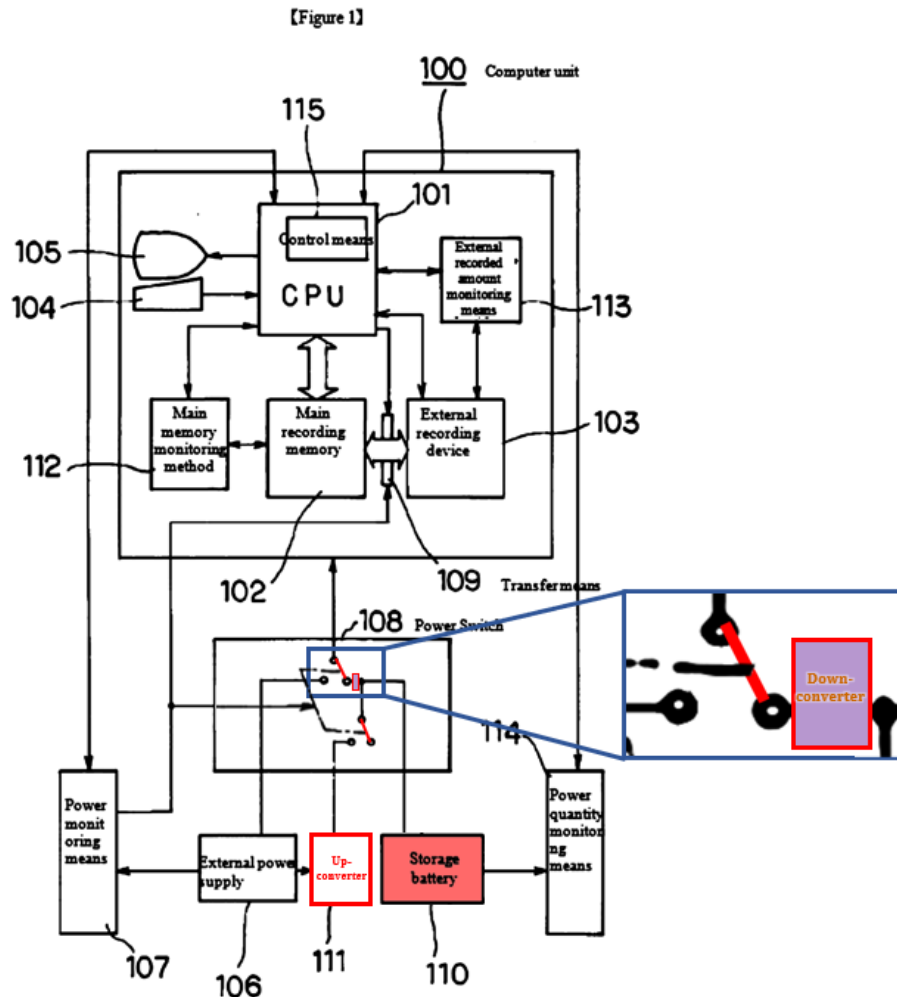
195. Pilukaitis disclosed “an integrated protection circuit for a power converter and method of operation thereof.” (Pilukaitis, 1:7-10 (INTEL-1014).) Pilukaitis established that there were several circuits available at the time of the alleged invention for realizing undervoltage lockout. For example, that functionality can be “provided by a **dedicated undervoltage circuit** or by a pulse width modulator (PWM) integrated circuit (IC) controller.” (Pilukaitis, 1:24-26 (INTEL-1014).) In either case, “as the input voltage drops from a normal operating input voltage to zero volts, **the undervoltage lockout circuit will turn the power converter off when the input voltage falls below a predetermined threshold.**” (Pilukaitis, 1:26-34 (INTEL-1014).) In one implementation, the protection circuit “includes: (1) a sensor that senses an actual input voltage of the power converter and (2) an isolation circuit, coupled to the first comparator, that selectively decouples the first comparator from the second comparator, the second comparator causing the controller to **disable the power converter when the actual input voltage falls below a threshold input voltage thereby allowing the protection circuit to provide both overcurrent and undervoltage protection.**” (Pilukaitis, 2:34-43 (INTEL-1014).)

196. I understand that the district court construed the claimed “*predetermined level*” of limitation 1.c to have its “plain-and-ordinary meaning.” (Claim Construction Order and Memorandum in Support Thereof, 15 (INTEL-1018).) Under that construction, the “predetermined threshold” disclosed in Pilukaitis is a “*predetermined level*.” The two phrases share the term “predetermined.” Further, Pilukaitis taught that the “threshold” represents a level of voltage that will result in shutdown if the power converter input falls beneath it. (Pilukaitis, 1:26-34 (INTEL-1014).)

2. Motivation to combine Pilukaitis with the combined system of Nishida and Ergott (including in further combination with Harari)

197. As explained in ¶191, the combined system of Nishida and Ergott (including in further combination with Harari) includes super-capacitors 110 and a voltage down-converter. The voltage down-converter is placed downstream of super-capacitors 110 (i.e., current flows from super-capacitors 110 to the voltage down-converter). The down-converter only receives power from super-capacitors 110 when power switching switch 108 is configured to the backup power supply side on the right, which is the side that includes super-capacitors 110. (Nishida, ¶¶3, 4, 15 (INTEL-1006).) Annotated and modified Figure 1 of Nishida reproduced below shows the modified switch position within power switching switch 108

using two red lines, super-capacitors 110 in red, and the voltage down-converter in purple.



198. Pilukaitis described advantages associated with the use of an undervoltage lockout circuit together with a power converter. First, “[t]he undervoltage lockout function is desirable since the input current to the power converter tends to increase as the input voltage decreases.” (Pilukaitis, 1:35-37 (INTEL-1014).) High current has the potential to cause serious problems, including “internal or external component failure” in the “power supply (e.g.,

power converter)” and “excessive heating in those failed components.” (Pilukaitis, 1:17-23 (INTEL-1014).) Second, an undervoltage lockout circuit “can prevent voltage drop and overcurrent shutdown in circuits with maximum duty cycle limiting.” (Pilukaitis, 1:38-40 (INTEL-1014).) To avoid those issues, Pilukaitis’s undervoltage lockout “function can effectively limit that current.” (Pilukaitis, 1:35-38 (INTEL-1014).)

199. Pilukaitis further disclosed that an undervoltage lockout circuit can be used together with several conventional converter devices: “even though only one type of power converter was referenced above, other converter topologies including, without limitation, a push-push converter, **a buck converter** and a flyback converter, are also within the broad scope of the present invention.” (Pilukaitis, 8:55-60 (INTEL-1014).) It was known to a POSITA that a “buck converter” is another name for a voltage down-converter: “[t]he current-mode switching regulator is designed as a step-down converter (buck converter).” (U.S. Pat. No. 6,222,356 (“Taghizadeh-Kaschani”), 7:58-59 (INTEL-1029).)

200. A POSITA would have used Pilukaitis’s undervoltage lockout circuit in the combined system of Nishida and Ergott (including in further combination with Harari) to obtain the known advantages described in Pilukaitis, which include preventing circuit damage and sudden and undesired shutdown. Pilukaitis also expressly suggests using the undervoltage lockout circuit with a down-converter,

such as the one included in the combined system of Nishida and Ergott (including in further combination with Harari).

201. A POSITA would have modified the combined system of Nishida and Ergott (including in further combination with Harari) based on the teachings of Pilukaitis because doing so would have applied a known technique, as described in Pilukaitis, to improve a similar system based on Nishida and Ergott in the same way taught in Pilukaitis. Pilukaitis established that using an undervoltage lockout circuit together with a power converter was a known approach. (Pilukaitis, 1:7-10 (INTEL-1014).) Undervoltage lockout circuits had been in use for “more than a decade.” (Pilukaitis, 1:13-15 (INTEL-1014).) Similar to the system in Pilukaitis, the combined system of Nishida and Ergott (including in further combination with Harari) includes a power converter in the form of a voltage down-converter.

202. Applying Pilukaitis’s teachings of an undervoltage lockout circuit to the combined system of Nishida and Ergott (including in further combination with Harari) would have prevented known problems associated with undervoltage being supplied to a power converter, as described in Pilukaitis. Incorporating the undervoltage lockout circuit of Pilukaitis into the combined system of Nishida and Ergott (including in further combination with Harari) would have worked the same way as Pilukaitis intended by turning off the voltage down-converter in the combined system of Nishida and Ergott (including in further combination with

Harari) when its input voltage drops below a threshold value to avoid the negative consequences of supplying undervoltage to the power converter.

203. A POSITA also would have modified the combined system of Nishida and Ergott (including in further combination with Harari) to include an undervoltage lockout circuit, as taught in Pilukaitis, because the modification would have involved a simple substitution of known elements. Pilukaitis described that the undervoltage lockout circuit was known, including for use with power supplies such as power converters. (Pilukaitis, 1:7-23 (INTEL-1014).) The down-converter of the combined system of Nishida and Ergott (including in further combination with Harari), which lacks undervoltage protection, was also a known component. A POSITA would have substituted the voltage down-converter of the combined system of Nishida and Ergott (including in further combination with Harari) that has no undervoltage protection for a power converter (such as a buck converter or down-converter) that includes undervoltage protection in the form of an undervoltage lockout circuit that controls power converter shutdown as taught in Pilukaitis. (Pilukaitis, 1:13-43, 8:55-60 (INTEL-1014).) The substitution would have been a straightforward replacement with predictable results. Pilukaitis's undervoltage lockout circuit would have protected the down-converter in the combined system of Nishida and Ergott (including in further combination with Harari) from the adverse effects of supplying undervoltage to the power converter.

204. I understand that the Petitioner proposed a claim construction of the “*predetermined level*” limitation of limitation 1.c to the district court. Under the claim construction proposed by the Petitioner, a “*predetermined level*” is “a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged.” (Defendant’s Opening Claim Construction Brief, 2 (INTEL-1012).)

205. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered the “*predetermined level*” limitation obvious under Petitioner’s proposed claim construction. Pilukaitis taught a “predetermined threshold” voltage that causes an undervoltage lockout circuit to shut down a power converter once the voltage falls below the threshold. (Pilukaitis, 1:31-34 (INTEL-1014).) Petitioner’s proposed construction required that the voltage be “preset.” Pilukaitis’s predetermined threshold is preset because it is a value known before the operation of the undervoltage lockout circuit and that value “can be set higher than” other voltages. (Pilukaitis, 8:7-37 (INTEL-1014).)

206. Pilukaitis’s predetermined threshold is also a “minimum operating voltage necessary for proper operation,” as required by Petitioner’s proposed construction. In Pilukaitis, “as the input voltage drops from a normal operating input voltage to zero volts, the undervoltage lockout circuit will turn the power converter off when the input voltage falls below a predetermined threshold.”

(Pilukaitis, 1:26-34 (INTEL-1014).) Pilukaitis disclosed that this power converter shutdown feature is necessary for proper operation of the converter because “the undervoltage lockout function can prevent voltage drop and overcurrent shutdown.” (Pilukaitis, 1:37-40 (INTEL-1014).) Pilukaitis further taught that an overcurrent condition, which is linked to low input voltage, can cause other impediments to proper operation, including “internal and external component failure” and “excessive heating in those failed components” (Pilukaitis, 1:21-23, 1:37-40, (INTEL-1014).)

207. As discussed in ¶¶63-64 and 193-194, Nishida’s super-capacitors 110 begin to discharge when they are activated to provide power to computer unit 100 through the voltage down-converter and the discharged voltage across super-capacitors 110 gradually decreases over time. Based on Pilukaitis’s teachings, in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), under some circumstances super-capacitors 110 would not have been fully discharged when the down-converter reached its predetermined threshold voltage prompting the undervoltage lockout circuit to turn off the converter. (Pilukaitis, 1:31-34 (INTEL-1014); *see also* 1:34-43.)

208. Pilukaitis taught that the undervoltage lockout voltage—“the input voltage ... at which the undervoltage lockout circuit will turn the power supply” off—is set higher than certain other voltages. Pilukaitis, 8:26-37 (INTEL-1014).)

The “undervoltage lockout voltage V_{inuv} can be set higher than the minimum input voltage V_{inmin} but lower than the input threshold voltage $V_{inturnon}$, which can be expressed as the following: $V_{inturnon} > V_{inuv} > V_{inmin} \dots V_{inmin}$ is the input voltage corresponding to minimum voltage which keeps the output voltage within the desired boundaries.” (Pilukaitis, 8:26-37(INTEL-1014).) In that case, the undervoltage lockout voltage (which corresponds to the input voltage received from super-capacitors 110 in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari)) is positive for any value of the minimum input voltage because the lockout voltage must be greater than the minimum input voltage. That remains true even if the minimum input voltage is equal to zero. According to the equation $\Delta V = Q/C$ discussed in ¶¶53 and 59, a positive input voltage (ΔV) indicates super-capacitors 110 still have remaining charge because Q (or stored energy) must be positive for the input voltage to be positive. Super-capacitors therefore are not fully discharged under these circumstances.

209. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) also rendered obvious portions of “*deactivating*” limitation 1.c other than the “*predetermined level*.” As discussed in ¶¶116-117 and 124-127 regarding limitations 1.pre and 1.a, Nishida taught a “*plurality of super capacitors*” that provides power to a “*computing engine*.” In the combined system

of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), super-capacitors 110 would have discharged voltage and the level of that voltage would have decreased to reduce the “input voltage” to the down-converter until it “fell below a predetermined threshold” causing Pilukaitis’s undervoltage protection circuit to “turn ... off” the voltage down-converter. (Pilukaitis, 1:31-34 (INTEL-1014).) This functionality corresponds to the portion the claim limitation that requires “*deactivating*” to occur “*based upon the plurality of super capacitors discharging to a predetermined level.*” In the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), super-capacitors 110 would have discharged to the predetermined threshold.

210. I am aware that the district court construed “*deactivating*” to mean “disconnect[ing]” a capacitor “such that it is not discharging current to a load.” (Claim Construction Order and Memorandum in Support Thereof, 19 (INTEL-1018); BiTMICRO LLC’s Sur-Reply Claim Construction Brief, 3 (INTEL-1019).) Under that construction, shutting down the voltage down-converter in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) would have disconnected super-capacitors 110 from computer unit 100. “[T]urn[ing] ... off” the voltage down-converter would have terminated the output voltage supplied by the down-converter to computer unit 100—the load that ultimately receives power produced by super-capacitors 110).

(Pilukaitis, 1:31-34 (INTEL-1014).) As Pilukaitis taught, the down-converter would have been “disabled,” and “reactivated” only once the input voltage recovers and “rises above the reference voltage.” (Pilukaitis, 4:64-67 (INTEL-1014); *see also* claim 1.) Down-converter shutdown would have, in turn, electrically disconnected super-capacitors 110 from computer unit 100 by cutting off the discharge path of super-capacitors 110 because any power discharged by super-capacitors 110, which must pass through the disabled and inactive down-converter to reach computer unit 100, cannot do so. Computer unit 100 corresponds to the “*computing engine*” and contains other components like CPU 101, main recording memory 102, and external recording memory 103 (potentially implemented as Harari’s EEPROM) that alternatively correspond to the “*computing engine*.” Therefore, turning off the down-converter would have “*cut off power to the computing engine*.”

211. The operation of the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) to cut off power to computer unit 100 resembles the “save mode” disclosed in the ’939 patent. When the computer system of the ’939 patent is operating in “save mode,” “once the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 110.” (’939 patent, 5:39-43

(INTEL-1001).) The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) similarly includes a down-converter that receives a super-capacitor voltage that may decrease below a threshold, and if it does so, results in the down-converter shutting down, which turns off the power supply to the remainder of the system.

3. The reasonable expectation of success for the combination of Pilukaitis with Nishida and Ergott (including in further combination with Harari)

212. A POSITA would have had a reasonable expectation of success in modifying the combined system of Nishida and Ergott (including in further combination with Harari). Pilukaitis demonstrated that a POSITA would have been aware of methods for implementing an undervoltage lockout circuit for a voltage down-converter. (Pilukaitis, 1:13-37 (INTEL-1014).) Pilukaitis noted that “undervoltage ... protection circuit have been separately used for power supplies for more than a decade.” (Pilukaitis, 1:13-15 (INTEL-1014).) Further, Pilukaitis directed a POSITA to use its teachings of an undervoltage lockout circuit in a buck converter, also known as a down-converter, which is the type of power converter used in the combined system of Nishida and Ergott (including in further combination with Harari). (Pilukaitis, 8:55-60 (INTEL-1014).)

213. The undervoltage lockout circuit of Pilukaitis would have been used for its intended purpose of “turn[ing] the power converter off when the input

voltage falls below a predetermined threshold.” (Pilukaitis, 1:30-33 (INTEL-1014).) A POSITA would have applied Pilukaitis’s teachings by substituting the down-converter without undervoltage protection in the combined system of Nishida and Ergott (including in further combination with Harari) with a down-converter that was subject to control by an undervoltage lockout circuit, as disclosed in Pilukaitis. A POSITA would have connected the input of the down-converter having undervoltage protection to the output of super-capacitors 110 and would have connected the output of the down-converter having undervoltage protection to the input of computer unit 100. These are the same input and output connections used for the down-converter in the combined system of Nishida and Ergott (including in further combination with Harari).

214. For limitations of claim 1 other than 1.c and for claims 2-3 and 6, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) would have rendered those limitations and claims obvious for the reasons explained above regarding the combined system of Nishida and Nakao (including in further combination with Harari).

C. Claim 10

1. **10.pre:** “*A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:*”

215. As explained in ¶¶113-123 regarding limitation 1.pre, Nishida disclosed the preamble to claim 1 or rendered it obvious in combination with Harari. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) also rendered obvious the preamble to claim 10. The preamble to claim 10 recites a “*system for controlling data in a computer system.*” The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) is based on Nishida’s “computer system” (Nishida, Summary, ¶¶2-7, 10-11, 13-16, Fig. 1 (INTEL-1006)) and includes a “*system for controlling data*” as described below in relation to limitations 10.a, 10.b, and 10.c.

216. The preamble to claim 10 recites a “*computer engine.*” The ’939 patent describes using the term “engine” to describe a single structure—“computing engine CE 28,” which “contain[s] the processor” and “volatile and non-volatile memory.” (’939 patent, 3:33-36 (INTEL-1001).) The ’939 patent does not describe any differences between a “*computer engine*” and a “*computing engine.*” As explained in ¶¶116-117 regarding limitation 1.pre, Nishida taught a “*computing engine*” and therefore also disclosed a “*computer engine.*” Those

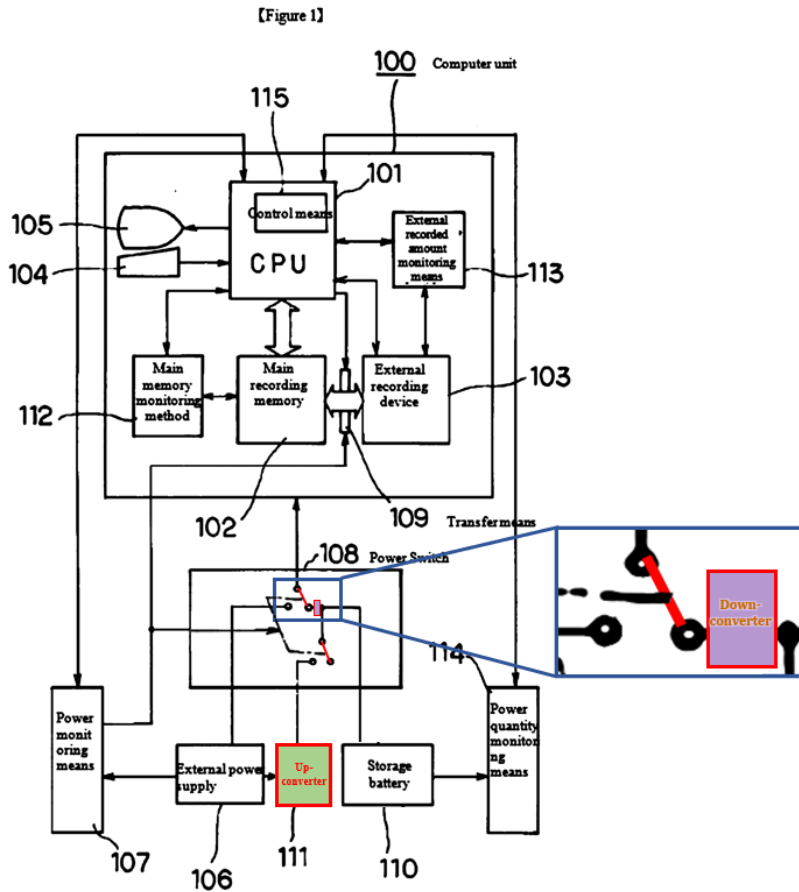
teachings are also part of the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari).

2. 10.a: “means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system”

217. As explained in ¶¶124-127 regarding limitation 1.a, Nishida disclosed the “*activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system.*” I have been asked to consider two potential sets of corresponding structure relating to limitation 10.a. The combined system of Nishida, Harari, Ergott, and Pilukaitis rendered the structures obvious.

a) Petitioner’s identified structure

218. As described in ¶101, I understand that the Petitioner identifies an up-converter and a down-converter (and equivalents) as corresponding structure for limitation 10.a. As described in ¶¶190-191, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) includes an up-converter and a down-converter. Annotated and modified Figure 1 from Nishida reproduced below shows the voltage up-converter in green and the voltage down-converter in purple.



219. In the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), when “the supply voltage of the external power supply 106 deviates from a predetermined range,” which indicates a power outage, the voltage up-converter would have been electrically disconnected from super-capacitors 110 when the lower switch of power switching switch 108 immediately switched to the backup power supply side on the right and away from the external power supply side on the left. (Nishida, ¶¶2-4 (INTEL-1006).) The resulting switch configurations for power switching switch 108 are shown as red lines in the figure reproduced above for the upper and lower switches inside power

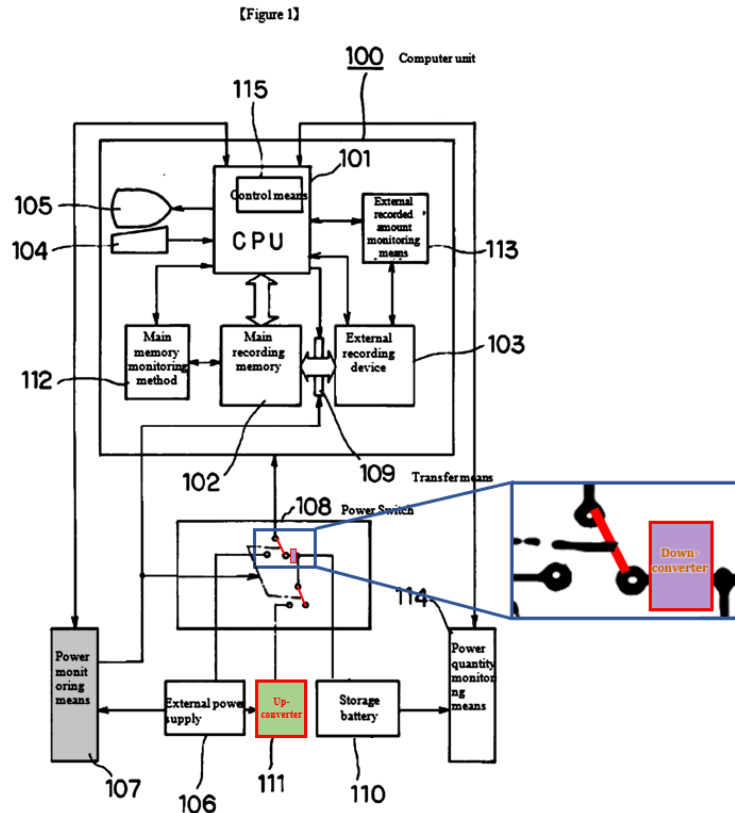
switching switch 108. Since the voltage up-converter is electrically disconnected from external power supply 106, which is the source of its power, the up-converter is deactivated and no longer provides power to super-capacitors 110 or any other components.

220. When the upper switch of power switching switch 108 is configured to activate the backup power supply by moving to the right side, the down-converter would have been electrically connected to computer unit 100 by means of the upper switch of power switching switch 108. (Nishida, ¶¶2-4, 15 (INTEL-1006).) Because the upper switch provides an electrical transmission line from the voltage down-converter to the computer unit 100, configuring the upper switch to the right activates the voltage down-converter to start the discharging process of super-capacitors 110. An active voltage down-converter allows super-capacitors 110 to “*activat[e]*” and discharge power. Super-capacitors 110 begin the discharge process in which current flows from super-capacitors 110 through the serially connected (and now activated) down-converter and arrives at the “*computing engine*” of the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). That “*computing engine*” is either computer unit 100 or CPU 101, main recording memory 102, and external recording device 103 (potentially Harari’s EEPROM).

b) Patent Owner's construction

221. I have also been asked to consider Patent Owner's construction of the corresponding structure of the "*means for activating*" limitation to require power sensors and a power isolator (and equivalents) in addition to an up-converter and a down-converter. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered power sensors and a power isolator obvious.

222. If the "*means for activating*" limitation requires a single power sensor as corresponding structure, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered a sensor obvious. Power monitoring means 107 is a power sensor. Power supply monitoring means 107 is configured to "constantly monitor[] the supply voltage of the external power supply 106, warn[] CPU 101 when this supply voltage deviates from a predetermined range, [and] switch[] power supply switching switch 108" to the backup power supply side on the right. (Nishida, ¶3 (INTEL-1006); *see also* ¶¶2, 4, 15.) Annotated and modified Nishida's Figure 1 reproduced below shows power monitoring means 107 in gray, the voltage up-converter in green, the voltage down-converter in purple, and the positioning on the right of the upper and lower switches of power switching switch 108 using two red lines.



223. Power supply monitoring means 107 operates to detect the voltage of external power supply 106. (Nishida, ¶¶3, 4, and 15 (INTEL-1006).) The '939 patent similarly describes that the power sensors detect whether “the external system power has fallen below a certain threshold amount.” ('939 patent, 5:19-22 (INTEL-1001).) Power supply monitoring means 107 is like the described power sensors.

224. Furthermore, a POSITA would have understood the power supply monitoring means 107 disclosed in Nishida as a sensor. The two terms were used interchangeably to describe measuring a target's characteristics. For example, “[a] set of sensors (monitoring means) is used to gather information The monitoring

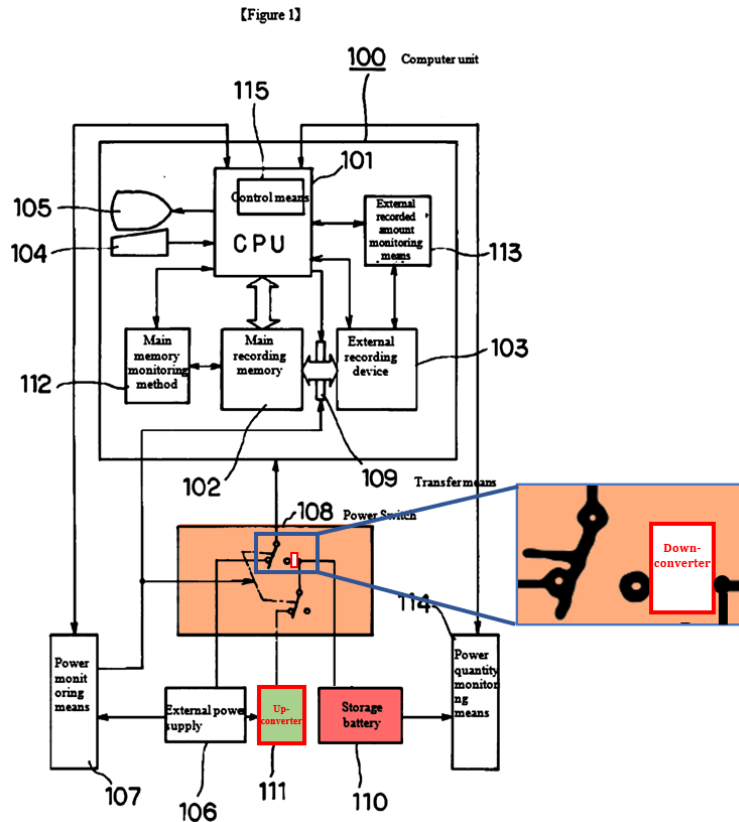
means include the respiration sensor ... for detecting chest wall movement ... the ECG electrodes [] to monitor the surface electrocardiogram and a reference ECG electrode ... to establish a ‘common’ potential for electrodes.” (U.S. Pat. No. 5,078,134 (“Heilman”), 8:5-16 (INTEL-1028).)

225. If the “*means for activating*” requires multiple sensors as corresponding structure, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) also rendered a set of sensors obvious. Nishida’s “power supply monitoring means 107 constantly monitors the supply voltage of the external power supply 106 [and] **warns CPU 101 when this supply voltage deviates from a predetermined range.**” (Nishida, ¶3 (INTEL-1006).) A POSITA would have understood that the predetermined range of external power supply 106 would have included a lower voltage limit but also an upper voltage limit. Tracking a predetermined range that included an upper limit was a known technique and allowed prevention against a circuit being exposed to overvoltage: “[o]vercurrent, undervoltage and **overvoltage protection circuits have been** separately **used for power supplies for more than a decade.**” (Pilukaitis, 1:13-15 (INTEL-1014).) The detection of the predetermined range disclosed in Nishida would have required two separate voltage sensing circuits, such as sensor and comparator pairs. One pair would have been used to check the lower limit of the range. It was known at the time of the alleged invention to use a

sensor for detecting a voltage level and an associated comparator to produce an output signal that depends on its comparison between the voltage level and a single reference voltage level. For example, Pilukaitis disclosed a “sensor (e.g., a resistor divider network including third and fourth resistors 460, 465)” (Pilukaitis, 6:16-18 (INTEL-1014)) for sensing an input voltage level (V_{in}) and comparator 430 for providing an output signal based on its comparison of the sensed input voltage level and a single “primary reference voltage V_{refl} ” (Pilukaitis, 6:19-33 (INTEL-1014)). Similarly, a second sensor/comparator pair would have been used to check the upper limit of the range.

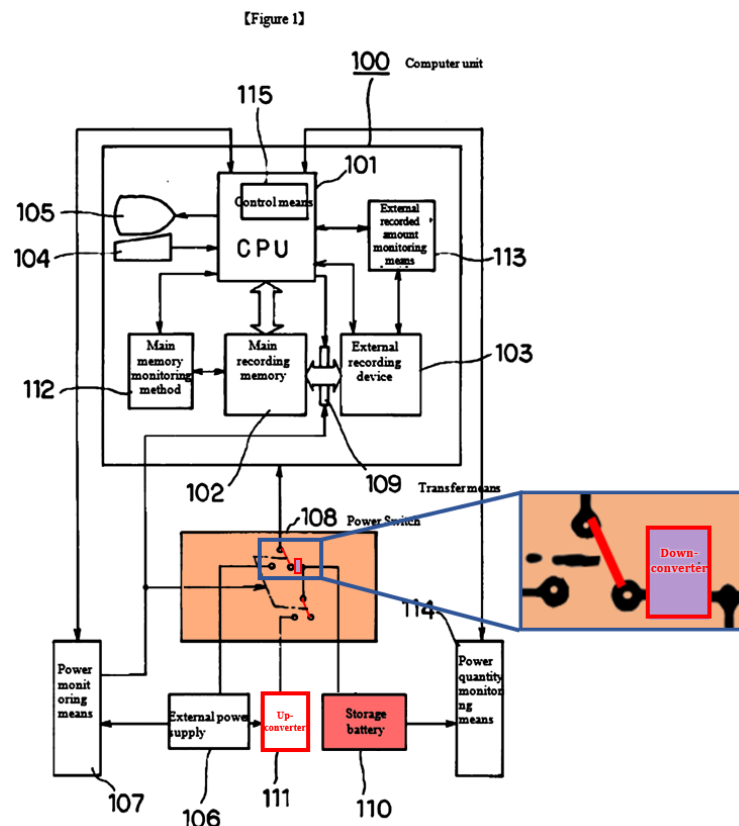
226. If a power isolator is corresponding structure for the “*means for activating*,” the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered a power isolator obvious. Nishida’s power switching switch 108 “switches the supply of power to the computer unit 100 between the external power supply 106” and super-capacitors 110. (Nishida, ¶3 (INTEL-1006); *see also* ¶¶4, 15.) When the upper and lower switches of power switching switch 108 are configured to the external power supply side on the left, indicating for example that external power supply 106 is operating within a predetermined range, external power 106 provides power to computer unit 100 and charges super-capacitors 110 through the voltage up-converter. (Nishida, ¶¶3, 4, 13 (INTEL-1006).) Annotated and modified Figure 1 from Nishida reproduced below

shows power supply switching switch 108 in orange, voltage up-converter in green, and super-capacitors 110 in red.



227. When “the supply voltage of the external supply 106 deviates from a predetermined range, the power supply monitoring means 107 immediately switches the power switching switch 108” to the backup power supply side on the right. (Nishida, ¶4 (INTEL-1006).) Annotated and modified Figure 1 from Nishida reproduced below shows the upper and lower switches of power switching switch 108 configured to the right side using two red lines in the upper and lower switches. The figure shows power switching switch 108 in orange, voltage down-converter in purple, and super-capacitors 110 in red. When power switching switch

108 is configured to the right, super-capacitors 110 are disconnected from the up-converter and external power supply 106 because the lower switch disconnects the current transmission line between super-capacitors 110 and the voltage up-converter. The upper switch establishes a current transmission line between the down-converter and computer unit 100, which causes current to begin flowing to computer unit 100 from super-capacitors 110 through the voltage down-converter. The upper and lower switches of power switching switch 108 disconnect, and therefore isolate, external power supply 106 from several of the other structures in the computer system, including computer unit 100, the voltage down-converter, and super-capacitors 110.



228. Nishida's power switching switch 108 is similar to the '939 patent's power isolator 26. The '939 patent discloses that power isolator 26 "isolates [computing engine] 28 from [external power source] 22." ('939 patent, 3:36-37 (INTEL-1001).) According to the '939 patent, isolation "prevents any contention between the external power source and the down-converter." ('939 patent, 5:28-31 (INTEL-1001); *see also* 6:31-33.) In the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), when power switching switch 108 is configured to the right to allow current to flow from super-capacitors 110 to computer unit 100, super-capacitors 110, the down-converter, and computer unit 100 are isolated from external power supply 106.

229. That isolation prevents contention between the down-converter and external power supply 106. For example, once power switching switch 108 is configured to the backup power supply side on the right, current only flows along one path from super-capacitors 110 through the down-converter to computer unit 100. Super-capacitors 110 do not supply power to external power supply 106 or the voltage up-converter. The lower switch of power switching switch 108 prevents current flow in that manner because it disconnects the transmission line between super-capacitors 110 and the voltage up-converter and external power supply 106.

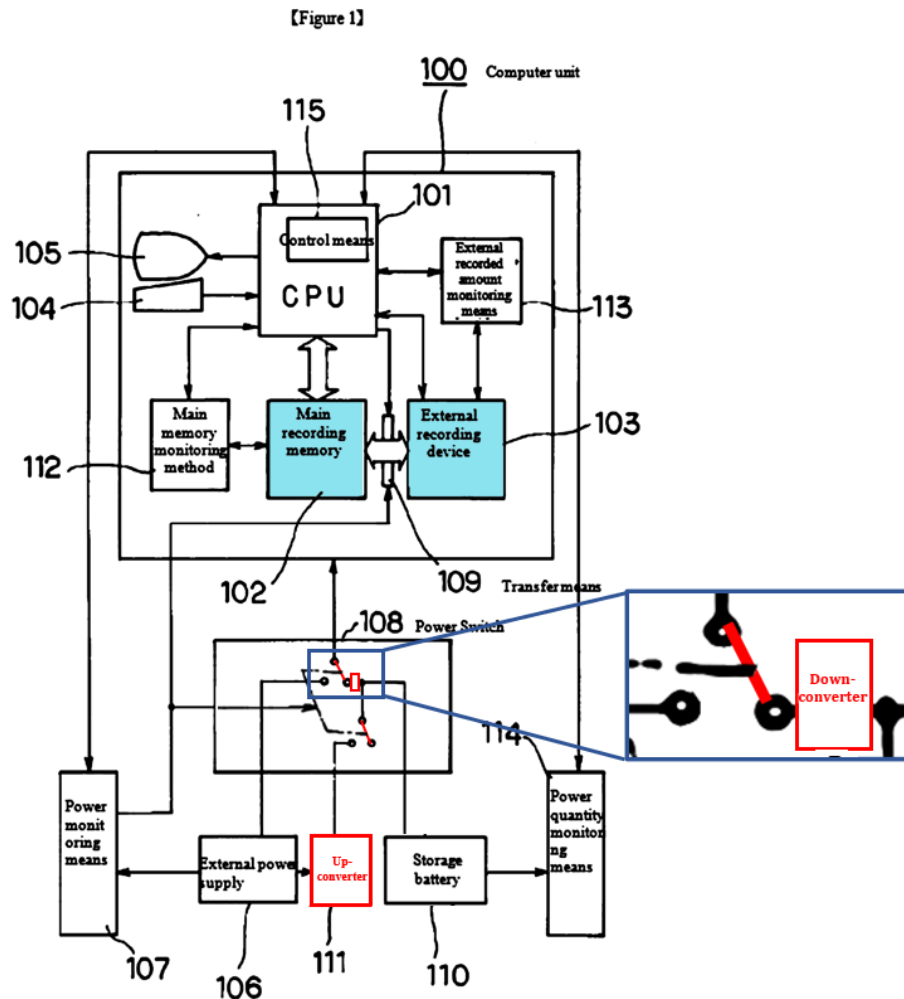
3. **10.b: “means for reconfiguring the data in the computing engine; and”**

230. As explained in ¶¶128-130 regarding limitation 1.b, Nishida disclosed the “*reconfiguring the data in the computing engine.*” Nishida taught transferring data when “the supply voltage of the external power 106 deviates from a predetermined range,” which indicates that the external power supply is interrupted. (Nishida, ¶¶3, 4 (INTEL-1006).) Based on those teachings regarding the operation of Nishida’s computer system, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) disclosed data transfer. I have been asked to consider whether the prior art taught Petitioner’s proposed construction for the corresponding structure for this limitation: a non-volatile memory and volatile memory (and equivalents). The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) includes non-volatile memory and volatile memory and they perform the data transfer described in Nishida.

231. As explained in ¶115, Nishida described “a **volatile** main recording memory.” (Nishida, ¶¶2, 3, 7 (INTEL-1006).) Nishida also disclosed a non-volatile memory, or in combination with Harari, rendered a non-volatile memory obvious. Nishida taught a “**non-volatile** external recording device.” (Nishida, ¶¶2, 3, 7 (INTEL-1006).) As explained in ¶¶118-119 regarding limitation 1.pre, a POSITA

would have understood external recording device 103 to be a memory. And as discussed in ¶¶120-123 regarding limitation 1.pre, it would also have been obvious to use Harari's EEPROM as external recording device 103 in Nishida's system.

232. Annotated and modified Figure 1 from Nishida reproduced below represents the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) and shows volatile main recording memory 102 and the non-volatile memory (which is either external recording device 103 or Harari's EEPROM) in blue. When the voltage supply of external power supply 106 deviates from a predetermined range, power switching switch 108 is configured to the backup power supply side on the right, which electrically connects super-capacitors 110 and computer unit 100. The switch configuration is represented by two red lines that appear in the upper and lower switches of power switching switch 108. If super-capacitors 110 have sufficient power to support the operation, "the data on the main recording memory 102 is completely evacuated" to the non-volatile memory. (Nishida, ¶15 (INTEL-1006).) Nishida described this operation as a data "transfer": "when this supply voltage deviates from a predetermined range," that results in a "**transfer** the contents of main recording memory 102 to external recording device 103." (Nishida, ¶3 (INTEL-1006); *see also* ¶¶2, 4, 7-9, 14-15.)



233. The '939 patent similarly describes using volatile and non-volatile memory to transfer data. For example, “[i]f the system is operating in save mode, ... all data is automatically transferred from volatile memory to the non-volatile memory in the event of a sudden power loss from the external power source.” ('939 patent, 4:37-41 (INTEL-1001).) The '939 patent also discloses that “data from the volatile memory is transferred to the non-volatile memory, via step 52.” ('939 patent, 5:11-28 (INTEL-1001).) The '939 patent further discloses “[w]hile the computer system is receiving current from the super-capacitors, data is

transferred from the volatile memory to the non-volatile memory, via step 106.”

(’939 patent, 5:33-36 (INTEL-1001); *see also* BiTMICRO LLC’s Responsive Claim Construction Brief, 7 (INTEL-1011).)

4. 10.c: “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.”

234. As explained in ¶¶196 and 204-210 regarding limitation 1.c, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious the “*deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level*” function. I have been asked to analyze the prior art based on the district court’s construction and Patent Owner’s construction of the corresponding structure. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered this claim limitation obvious under both claim constructions.

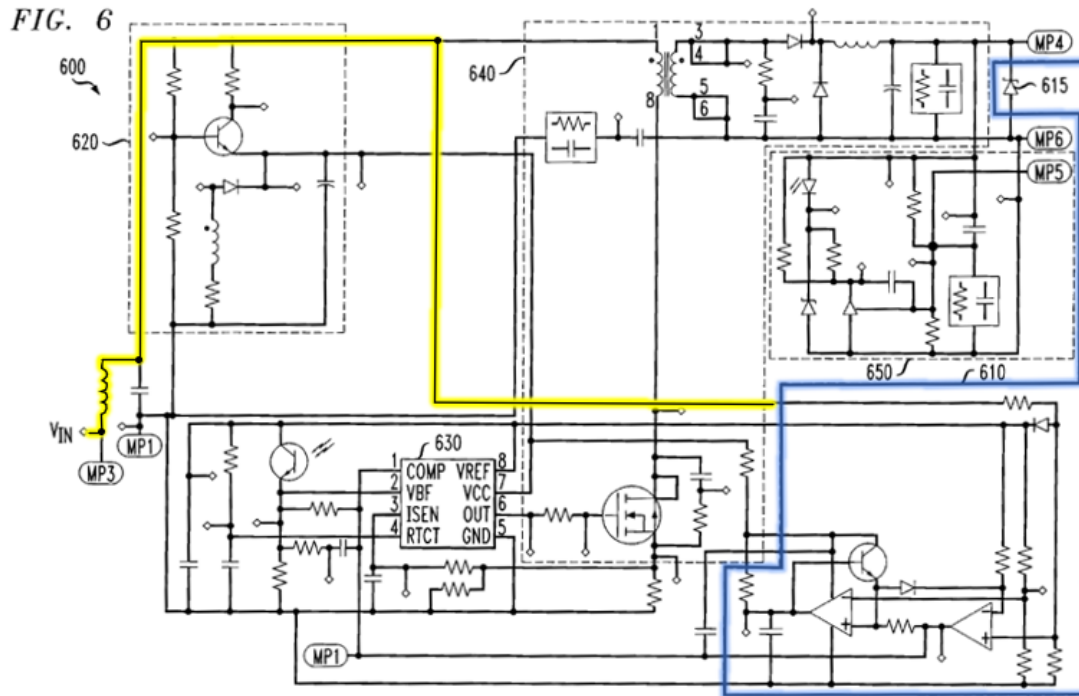
a) District court’s construction

235. I have been asked to consider the district court’s construction that a down-converter (and equivalents) is corresponding structure and that “other circuit elements, *e.g.*, switches, transistors, gates, *etc.*, could be corresponding structure.” (Claim Construction Order and Memorandum in Support Thereof, 20 (INTEL-1018).) The combined system of combined system of Nishida, Ergott, and

Pilukaitis (including in further combination with Harari) rendered obvious a down-converter and the “other circuit elements.”

236. As explained in ¶¶196, 204-210, and 212-213 regarding limitation 1.c, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) would have performed “*deactivating*” using Pilukaitis’s **undervoltage lockout circuit**. Pilukaitis taught that a “power converter” is an example of a “power supply”: “[t]he advantages of the overcurrent protection circuits are that they are very simple, can completely shut-off the **power supply (e.g., a power converter)**.” (Pilukaitis, 1:17-21 (INTEL-1014).) Pilukaitis also disclosed that its “power supply,” which can be a power converter, incorporates an undervoltage lockout circuit. For example, Pilukaitis taught that “[t]he **power supply 600 employs an integrated** overcurrent, **undervoltage** and overvoltage **protection circuit 610** constructed according to the principles of the present invention.” (Pilukaitis, 7:54-57 (INTEL-1014).) Annotated Figure 6 of Pilukaitis reproduced below shows an **integrated** overcurrent, undervoltage, and overvoltage protection circuit 610 outlined in blue that is an integral part of and included within power supply 600. Protection circuit 610 is integrated within power supply 600 at least because a single input voltage (V_{IN}) terminal of power supply 600 provides input voltage to several circuitry components within power supply 600, including

protection circuit 610. The transmission path connecting the input voltage (V_{IN}) terminal to protection circuit 610 is highlighted in yellow.

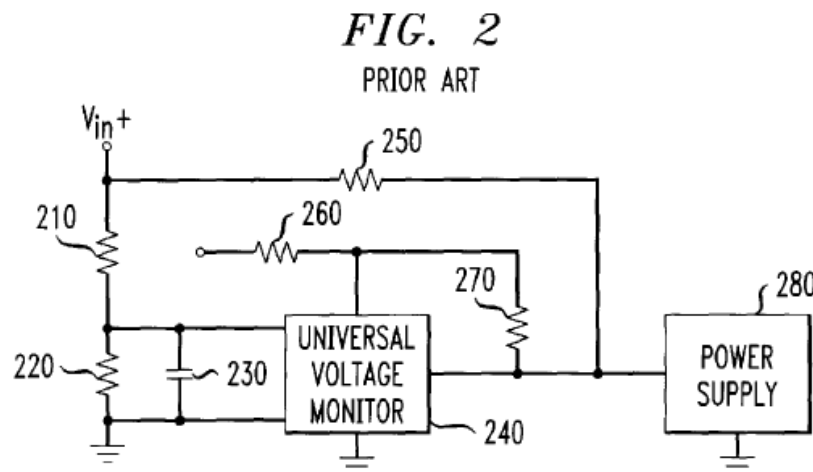


237. Pilukaitis disclosed that its teachings apply to other converter topologies: “those skilled in the art are aware that even though only one type of power converter was referenced above, other converter topologies including, without limitation, a push-push converter, **a buck converter** and a flyback converter, are also within the broad scope of the present invention.” (Pilukaitis, 8:55-60 (INTEL-1014).) A POSITA would have understood that a “buck converter” is another way to describe a down-converter: “[t]he current-mode switching regulator is designed as a step-down converter (buck converter).” (Taghizadeh-Kaschani, 7:58-59 (INTEL-1029).) Based on these disclosures, a

POSITA would have added Pilukaitis's undervoltage lockout circuit as an integrated component of the **voltage down-converter** in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). Pilukaitis expressly taught that approach. The resulting down-converter of the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) would have included the undervoltage lockout circuitry for "*deactivating*" super-capacitors 110 by turning off the down-converter. In this configuration, the down-converter contained the circuits needed to perform "*deactivating*," which taught the required corresponding structure of a down-converter under the district court's construction.

238. Alternatively, Pilukaitis described that the undervoltage lockout circuit as a structure separate from the voltage down-converter, and that configuration would also meet the district court's construction of corresponding structure. Pilukaitis disclosed a prior art implementation with "a prior art undervoltage lockout circuit 200" that is structural distinct from although "coupled to a power supply 280." (Pilukaitis, 4:48-67 (INTEL-1014); *see also* Fig. 2.) In this prior art implementation disclosed by Pilukaitis, a "universal voltage monitor (UVM) 240 [] monitors undervoltage conditions" and if "the input voltage V_{in} is lower than a reference voltage" "the output of the UVM 240 drops to zero, [and] the power supply 280 will be disabled." (Pilukaitis, 4:48-67 (INTEL-1014).)

Following these disclosures, instead of integrating the undervoltage lockout circuit into the down-converter, a POSITA would have positioned Pilukaitis's undervoltage protection circuit (e.g., universal voltage monitor (UVM) and its peripheral circuitry from the prior art implementation) as a distinct structure from the voltage down-converter in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). Figure 2 of Pilukaitis relating to the prior art implementation is reproduced below.



239. This modified approach for the combination meets the district court's construction of corresponding structure because that construction allows that "other circuit elements," whether part of or distinct from the voltage down-converter, could be corresponding structure. In this case, Pilukaitis's undervoltage lockout circuit would have been incorporated separately from the down-converter and the separate circuit would have been involved in "*deactivating*." That covers

both the down-converter and “other circuit elements” mentioned in the district court’s construction.

240. It also would have been obvious to a POSITA to try incorporating Pilukaitis’s undervoltage lockout circuit using either implementation option, integrating the undervoltage lockout circuit into the down-converter or adding it as a separate component. As evidenced by Pilukaitis, there are a finite number of ways to implement an undervoltage lockout circuit that affects a power converter. A designer has two basic options: (i) integrating the undervoltage detection circuit into the power converter (e.g., the embodiment illustrated in Figure 6 of Pilukaitis) or (ii) connect an undervoltage lockout circuit as a separate structure to a power converter (e.g., the prior art implementation embodiment illustrated in Figure 2 of Pilukaitis). The former option would have positioned the undervoltage lockout circuit **inside** the down-converter. The latter option would have positioned the undervoltage lockout circuit **outside** the down-converter.

241. A POSITA would have had a reasonable expectation of success in exploring those two options because both were known. Pilukaitis disclosed implementations based on both approaches. In addition, U.S. Pat. No. 5,627,460 (“Bazinet”) taught integrating an undervoltage lockout circuit into a voltage down-converter. Bazinet is directed to “switching converters and more particularly, to Buck, or step-down converters having a bootstrapped high side driver.” (Bazinet,

1:6-8 (INTEL-1040).) The “Buck” or “step-down converter 10” converts input DC voltage to a lower DC output voltage. (Bazinet 2:55-60 (INTEL-1040).) Therefore, the “step-down converter” is configured to provide the same function (converting a higher DC input voltage into a lower DC output voltage) as Ergott’s voltage down-converter and the buck converter disclosed by Pilukaitis. (Pilukaitis, 8:55-60, claims 15-21 (INTEL-1014); Ergott, 7:6-11, 8:3-10 (INTEL-1008).) Both Pilukaitis and Bazinet use the same term (buck converter) when referring to their voltage down-converters. (Pilukaitis, 8:55-60 (INTEL-1014); Bazinet 2:55-60 (INTEL-1040).)

242. Figure 1 of Bazinet reproduced below shows step-down converter 10 incorporating control circuit 30. Figure 5 of Bazinet reproduced further below shows “additional features of the control circuit 30 of FIG. 1.” (Bazinet, 7:11-12 (INTEL-1040).) Control circuit 30 of step-down converter 10 contains comparator 136 and inverter 142 (shown in Figure 5 of Bazinet) that “provide[s] an **under voltage lockout feature** to inhibit the gate drive signals 38, 40 until the input voltage V_{IN} has reached a level necessary for regulated operation.” (Bazinet, 7:17-24, 7:38-42, Fig. 1 (INTEL-1040); *see also* 2:49-50, 7:11-13.) Control circuit 30 is an integral part of step-down converter 10: “[p]referably, the control circuit 30 and linear regulator 42 are provided **in a monolithic integrated circuit**.” (Bazinet, 3:53-54 (INTEL-1040).)

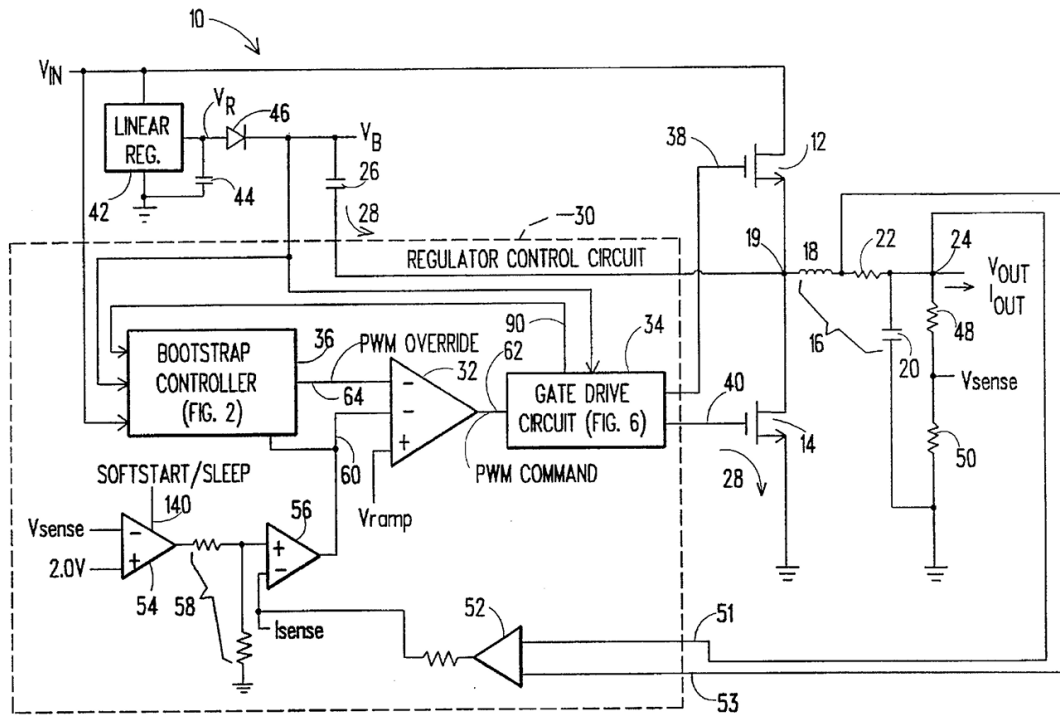


FIG. 1

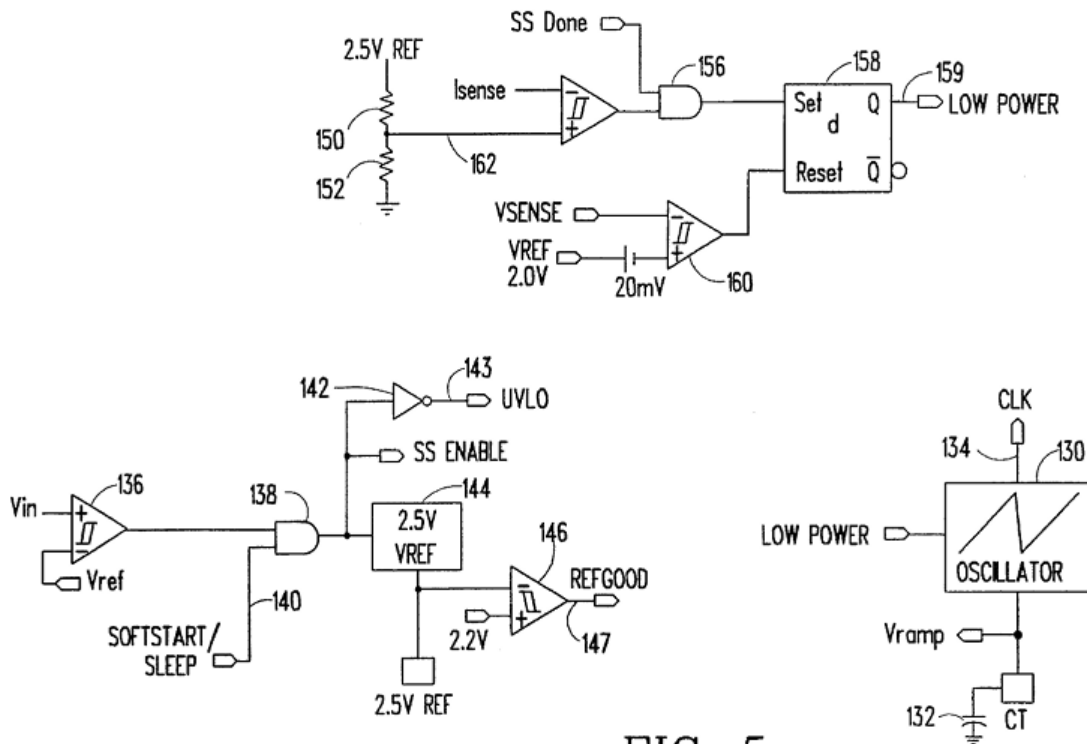


FIG. 5

b) Patent Owner's construction

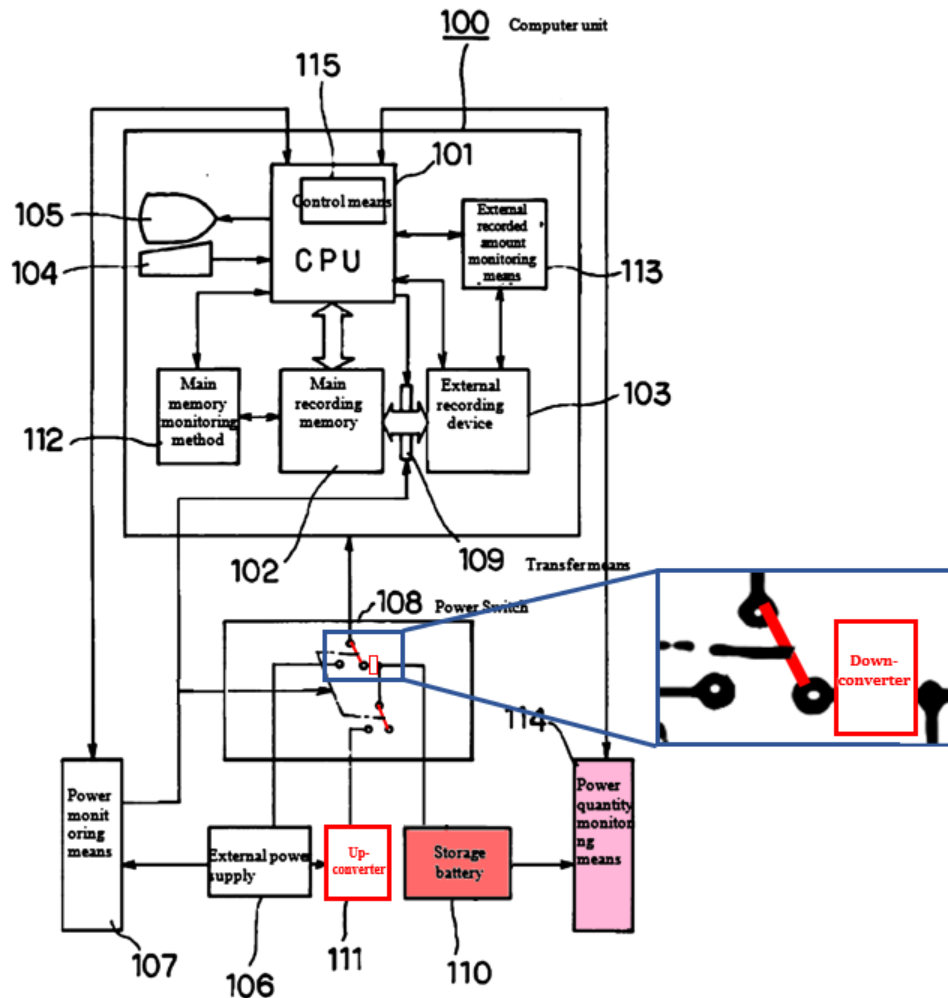
243. I understand that Patent Owner construes the “*means for deactivating*” of limitation 10.c to require a down-converter, up-converter, charge level sensors, and a power isolator (and equivalents) as corresponding structure. As explained in ¶¶236-237 and 240-242 regarding the district court’s corresponding structure for limitation 10.c, a POSITA would have implemented the undervoltage lockout circuit of Pilukaitis as part of the down-converter in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). In addition, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious the up-converter, charge level sensors, and power isolator that are included in Patent Owner’s construction.

244. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) includes an up-converter. During normal operation, such as when “external power supply 106 is within a predetermined range, the power supply switching switch is switched to the external power supply 106 side [on the left], and th[e] computer system is operated with power from the external power supply 106, and the [backup power supply, e.g., super-capacitors] 100 is charged by the charger 111.” (Nishida, ¶13 (INTEL-1006); *see also* ¶¶3-4.) In the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), an up-converter replaces charger 111. Electrically

connecting the up-converter to super-capacitors 110 by configuring power switching switch to the left side would have activated the up-converter to “boost[]” the power supply provided by external power supply 106 to supply power to and “charge up” super-capacitors 110 to a high voltage. (Ergott, 6:62-67 (INTEL-1008).) The ’939 patent similarly describes an up-converter that activates to charge super-capacitors using power from an external power system: “the computer system is reconnected to the external power system, ... the up-converter is activated to recharge the super-capacitors.” (’939 patent, 5:52-57 (INTEL-1001); *see also* 3:39-41.)

245. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) also includes charge level sensors. If only one charge level sensor is required as corresponding structure, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered a charge level sensor obvious. Nishida’s computer system includes power amount monitoring means 114 for “monitor[ing] the current charge amount” of the backup power supply (e.g., super-capacitors 110) and “report[ing] it to the CPU 101.” (Nishida, ¶11 (INTEL-1001); *see also* Summary, ¶14.) Annotated and modified Figure 1 reproduced below shows power amount monitoring means 114 in pink and super-capacitors 110 in red.

【Figure 1】



246. When power amount monitoring means 114 monitors the backup power supply voltage, it senses or detects that voltage so it can report its measurements to CPU 101. As explained in ¶224 regarding limitation 10.a, a POSITA also would have understood a “monitoring means” to refer to a sensor.

247. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) includes a second charge level sensor in the form of Pilukaitis’s undervoltage lockout circuit. Pilukaitis disclosed that the circuit

includes “a sensor that senses an actual input voltage of [a] power converter.” (Pilukaitis, 2:34-43, claims 1, 15 (INTEL-1014); *see also* 2:48-67, 6:19-23.) As part of the combination, super-capacitors 110 would have provided power to the voltage down-converter. Thus, sensing the input voltage for the voltage down-converter is the same as sensing the output voltage for super-capacitors 110. The voltage measurements would have indicated super-capacitor output voltage and down-converter input voltage at the same time.

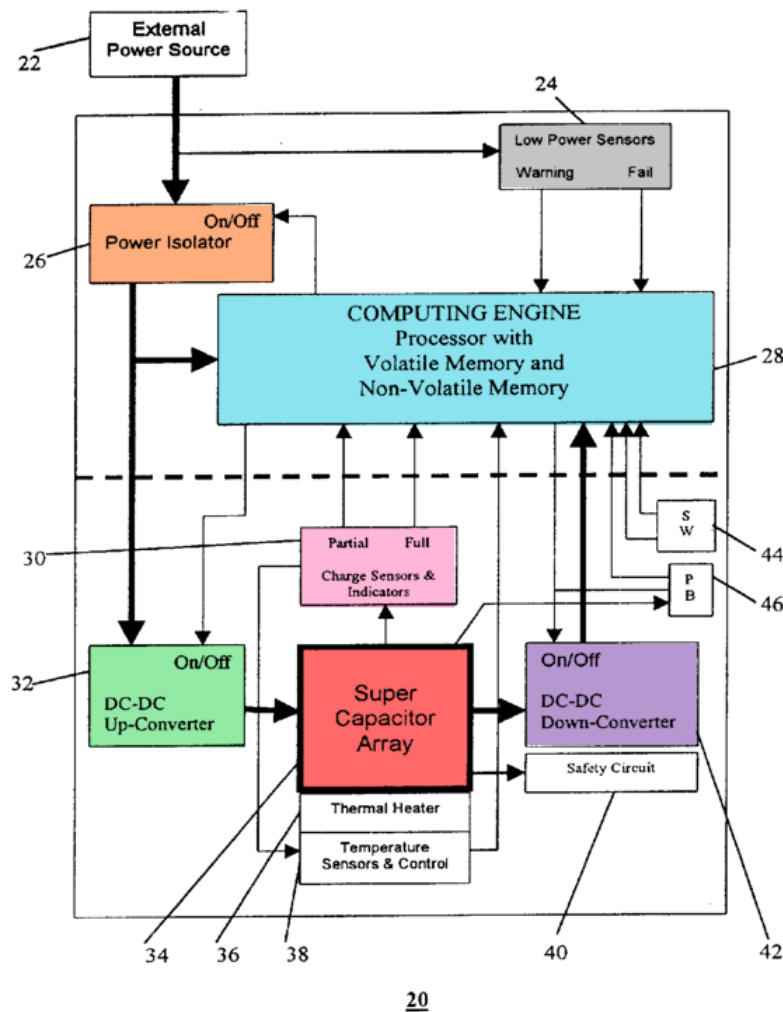
248. Nishida’s power amount monitoring means 114 and Pilukaitis’s undervoltage lockout circuit resemble the charge level sensors disclosed in the ’939 patent that detect whether the super-capacitors are “partially and fully charged.” (Nishida, 3:41-43 (INTEL-1001); *see also* 5:36-39.) Power amount monitoring means 114 monitors the charge amount of super-capacitors 110 at all times, including when they are fully and partially discharged. (Nishida, ¶11 (INTEL-1006).) The undervoltage lockout circuit of Pilukaitis would have detected when super-capacitors 110 provides an input voltage to the down-converter that “falls below a predetermined threshold.” (Pilukaitis, 1:31-34 (INTEL-1014).) As explained in ¶¶207-208, in some instances detecting that threshold would have sensed a partial discharge level of super-capacitors 110.

249. If more than one charge level sensor is required as corresponding structure for the “*means for deactivating*” limitation, the combined system of

Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered that obvious. Nishida's power amount monitoring means 114 and Pilukaitis's undervoltage lockout circuit each qualify as a charge level sensor for super-capacitors 110.

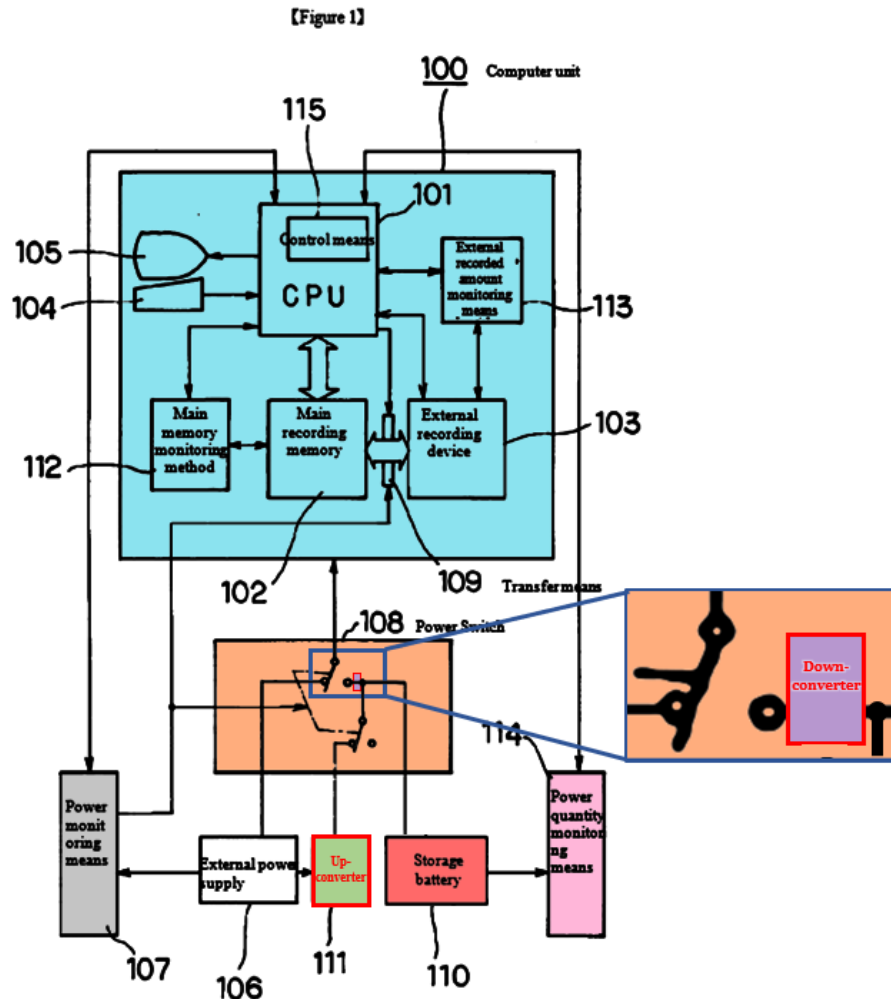
250. As explained in ¶¶226-229, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious a power isolator. Power switching switch 108 is like power isolator 26 disclosed in the '939 patent.

251. Overall, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) shares many structural similarities with the computer system disclosed in the '939 patent. The two systems include many of the same structural components. Annotated Figure 1 from the '939 patent reproduced below shows computing engine 28 (which includes a "processor," "volatile memory," and "non-volatile memory) in blue, power isolator 26 in orange, power sensors 24 in gray, charge sensors 30 in pink, up-converter 32 in green, supercapacitors 34 in red, and down-converter 42 in purple.



252. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) includes the same components. Annotated and modified Figure 1 from Nishida reproduced below shows computer unit 100 (which includes CPU 101, memory 102, and recording device 103) in blue, power switching switch 108 in orange, power supply monitoring means 107 in gray, power amount monitoring means 114 in pink, an up-converter in green, super-

capacitors 110 in red, and a down-converter in purple. The figure does not depict Pilukaitis's undervoltage lockout circuit that protects the down-converter.



D. Claim 11: “*The system of claim 10 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.*”

253. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered claim 11 obvious for the reasons explained in ¶164 regarding claim 2. The two claims recite the same additional limitation.

- E. **Claim 12:** “*The system of claim 11 wherein the reconfiguring means further comprises: means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.*”

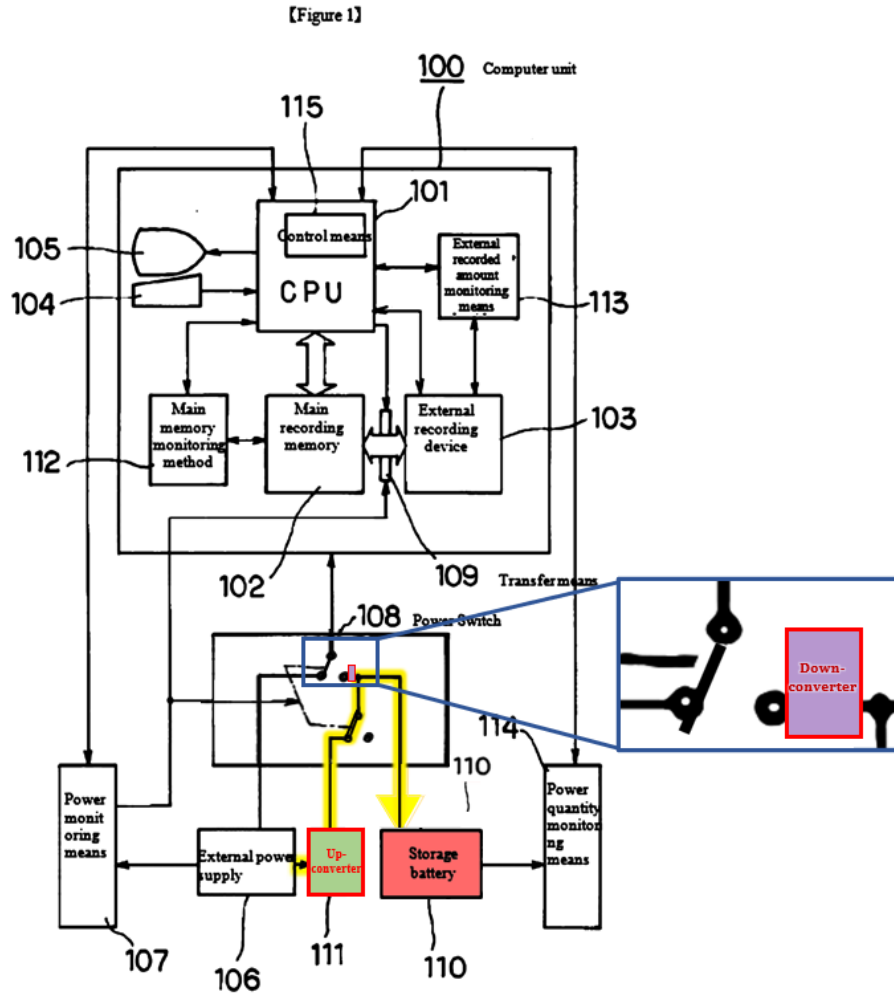
254. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered claim 12 obvious for the reasons explained in ¶¶128-130 regarding limitation 10.b. I understand that Petitioner identifies the corresponding structure for the “*means for allowing*” to be the same as its proposed corresponding structure for the “*means for reconfiguring*” of limitation 10.b. That structure is a volatile memory and a non-volatile memory (and equivalents) and is included in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). In the case of a power outage in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), when super-capacitors 110 have charge adequate to support a complete data transfer, “the data on the main recording memory 102 is **completely evacuated**” to the non-volatile memory. (Nishida, ¶15 (INTEL-1006).)

- F. **Claim 15:** “*The system of claim 12 wherein the activating means further comprises: means for reversing the flow of current between the computing engine and the plurality of super capacitors; and means for discharging current from the plurality of super capacitors to the computing engine.*”

255. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered claim 15 obvious.

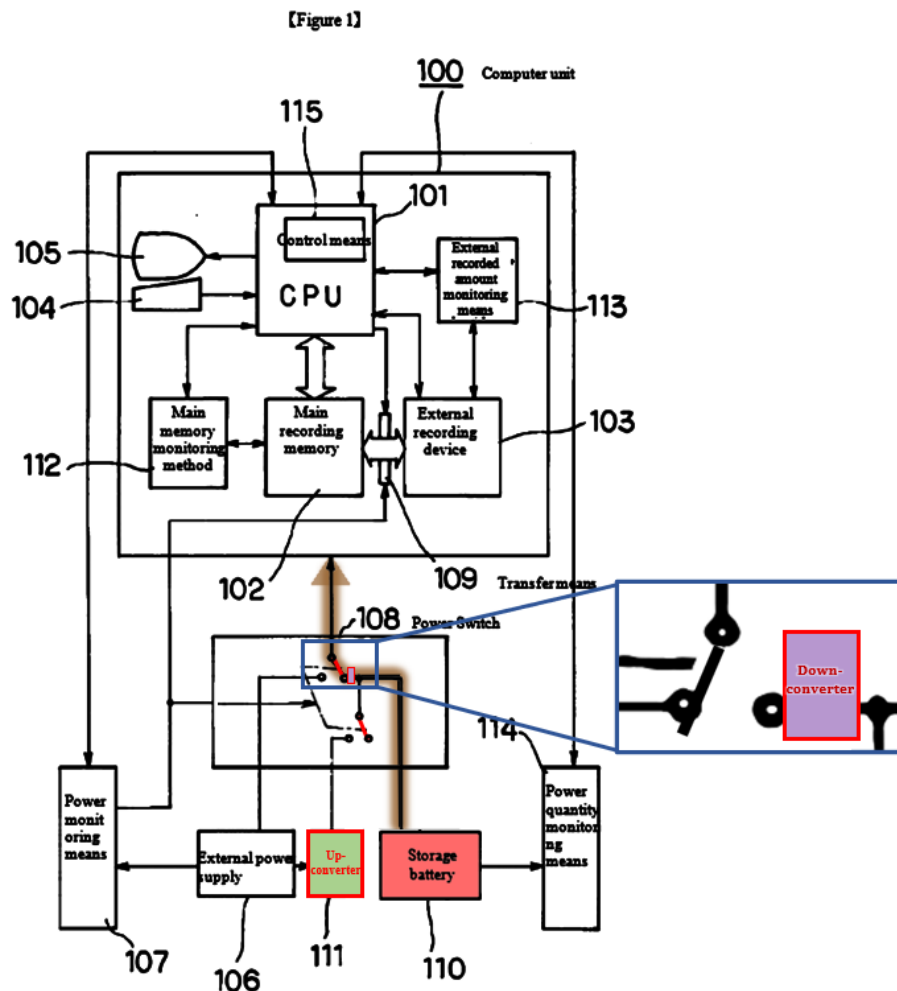
256. As to the “*means for reversing*,” the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered “*reversing the flow of current between the computing engine and the plurality of super capacitors*” obvious for the reasons explained in ¶¶166-175 regarding claim 6.

257. I understand that Petitioner identifies the “*means for reversing*” limitation as having the corresponding structure of a voltage up-converter and a voltage down-converter (and equivalents). The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious the voltage up-converter and voltage down-converter. Annotated and modified Figure 1 from Nishida reproduced below represents the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). The figure shows super-capacitors 110 in red, the up-converter in green, and the down-converter in purple. The figure also shows a yellow arrow that indicates the path and direction of current flow from external power supply 106 **toward** super-capacitors 110 when the computer system is not experiencing a power outage.



258. Annotated and modified Figure 1 from Nishida reproduced below also represents the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). This iteration also shows super-capacitors 110 in red, the up-converter in green, and the down-converter in purple. Here, however, a brown arrow shows the path and direction of current flow **from** super-capacitors 110 into the down-converter and then to computer unit 100. This is the current flow in the computer system of the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) when the external power

supply is interrupted. As explained in ¶227 regarding limitation 10.a, the configuration of power switching switch 108 to the backup power supply side on the right that follows a power outage results in the deactivation of the voltage up-converter and the activation of the voltage down-converter, altering the current flow in the computer system. The altered current flow, which shifts from current that flows toward the super-capacitors to current that flows away from the super-capacitors, is “reversing” under Patent Owner’s construction of that term, as explained in ¶¶167-172 regarding claim 6.



259. I understand that Patent Owner's construction of corresponding structure for the "*means for reversing*" limitation goes beyond a voltage up-converter and a voltage down-converter to include the following additional structures: power sensors, a power isolator, and the structures that Patent Owner construes as corresponding structure for the "*means for deactivating*" limitation. As explained in ¶¶218-229 and 234-250 regarding limitations 10.a and 10.c, the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious power sensors, a power isolator, and the structures that Patent Owner construes as corresponding structure for the "*means for deactivating*" limitation.

260. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious the "*means for discharging*" limitation. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious the recited function of "*discharging current from the plurality of super capacitors to the computing engine*" for the reasons explained in ¶175 regarding claim 6. I understand that both Petitioner and Patent Owner address the corresponding structure for this limitation by referring to the corresponding structure they have identified or proposed for the "*means for activating*" of limitation 10.a. The combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) rendered obvious the

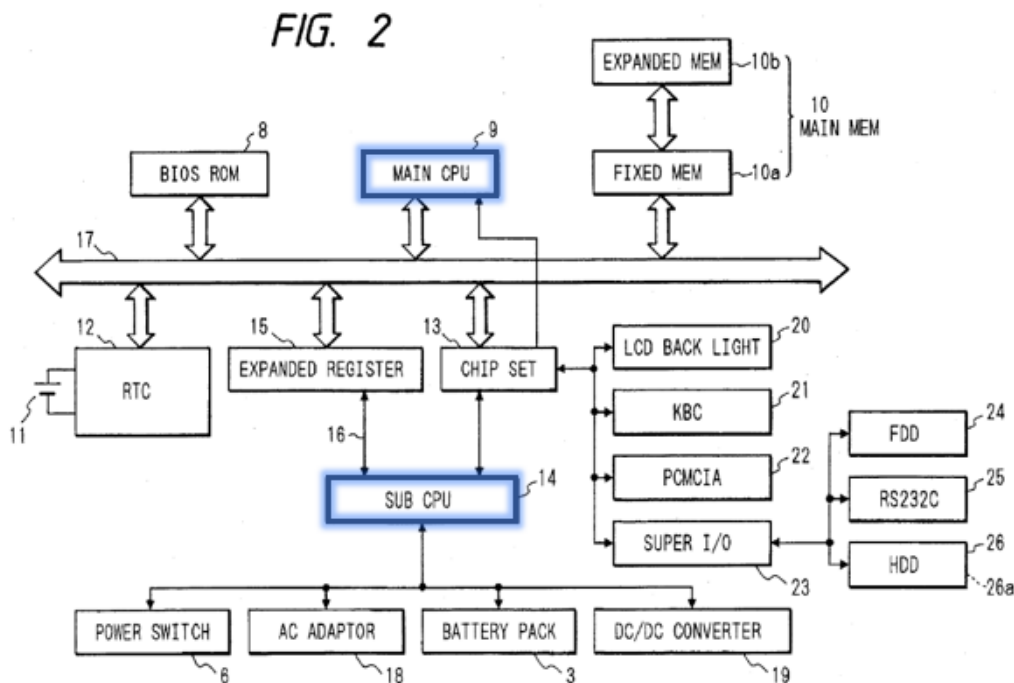
corresponding structures identified or proposed by the parties for limitation 10.a for the reasons explained in ¶¶218-229 regarding limitation 10.a.

V. Claims 10-12 and 15 would have been obvious over the combination of Nishida, Harari, Ergott, Pilukaitis, and Nakamura

261. I have been asked to consider a claim construction of the corresponding structure for the six means-plus-function limitations recited in claims 10 (three means-plus-function limitations), claim 12 (one means-plus-function limitation), and claim 15 (two means-plus-function limitations) that includes a computing engine or processor. As described below, under that claim construction, a POSITA would have combined U.S. Pat. No. 5,710,931 (“Nakamura”) with the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) described above in this Declaration. The combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari) would have rendered obvious the means-plus-function limitations of claims 10, 12, and 15 to the extent they require a computing engine or processor as corresponding structure. The combination also would have rendered obvious the other limitations of those claims, as well as claim 11, for the reasons explained above relating to the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari).

A. The teachings of Nakamura

262. Nakamura is entitled “suspension state control for information processing devices such as battery powered computers.” (Nakamura, Title (INTEL-1027).) Nakamura described a “notebook personal computer ... “that has a suspension function that temporarily halts the supply of power as needed, and a resume function that, when power is again supplied, immediately places the computer in the state in which it was before it was halted.” (Nakamura, 1:10-17 (INTEL-1027).) Annotated Figure 2 reproduced below “is a block diagram illustrating the internal arrangement of the notebook personal computer.” (Nakamura, 5:7-8 (INTEL-1027).) Main CPU 9 and sub-CPU 14 are outlined in blue.



263. Sub-CPU 14 “mainly controls [the] power supply system” and “exchange[s] data” with main CPU 9. (Nakamura, 6:45-58 (INTEL-1027).) Sub-CPU 14 dictates whether power is supplied or halted: “Under the control of the sub-CPU 14, the DC/DC converter 19 converts an input voltage from the battery pack 3 into a desirable output voltage and both supplies power to the main CPU 9 and halts the supply of power.” (Nakamura, 6:67-7:4 (INTEL-1027).) Nakamura further taught that main CPU 9 can control the operations of the power supply system. “[W]hen a main CPU 9 that has a sufficiently high processing speed is employed, the main CPU 9 can take the place of the sub-CPU 14 to perform one or all of the controls, such as power characteristic determination processing, that are performed by the sub-CPU 14.” (Nakamura, 18:1-8 (INTEL-1027).)

B. The motivation for combining Nakamura with the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari)

264. A POSITA would have been motivated to use Nakamura’s teachings about power supply control by a CPU in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari). Using a CPU to control power supply functions, as taught in Nakamura, was a known technique. The combinations based on Nishida involved a similar system that required control of whether power is supplied to computer unit 100 using external power supply 106 or backup power supply 110 (e.g., batteries, super-capacitors) and related

functions such as detecting an outage in the external power supply and transferring data in volatile memory to prevent its erasure. (Nishida, ¶¶2-4, 13, 15 (INTEL-1006).) Nishida's teachings reflect that controlling power supply functions was a known issue and necessary to facilitate system shutdown operations in the case of a power outage, including protecting data when an external power supply is interrupted. (Nishida, ¶¶2-4, 15 (INTEL-1006).)

265. Applying Nakamura's technique would have improved the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) by using a CPU, as disclosed in Nishida (computer unit 100 or CPU 101), to control power supply functions and ensure system operations after a power outage with minimal, if any, data loss. Nakamura's disclosures confirm that power supply control by a CPU was a workable option that satisfied the need for power supply control recognized by Nishida.

266. A POSITA also would have been motivated to apply Nakamura's teachings of power supply control using a CPU in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) because it would have been a simple substitution of known elements. Nakamura's CPU-based power supply control was known. (Nakamura, 6:45-58, 6:67-7:4, 18:1-8 (INTEL-1027).) Nishida's power supply control relied on other components such as power supply monitoring means 114 to perform some control functions, such as switching

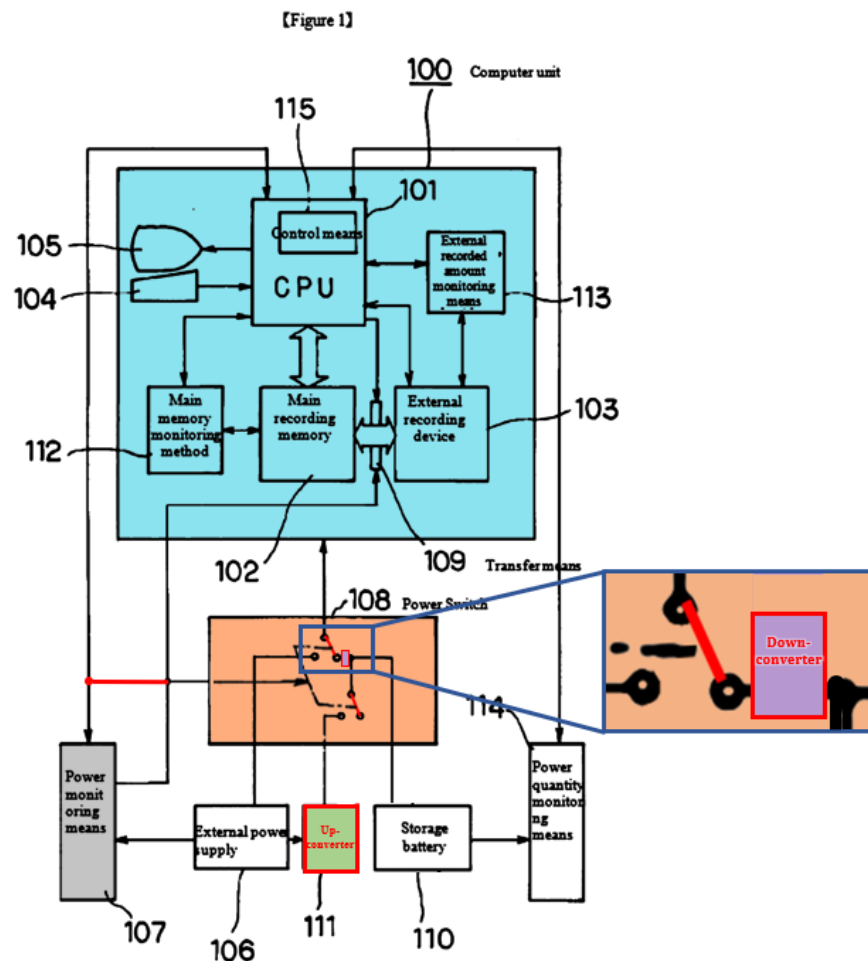
power switching switch 108 when a power outage is detected and providing instructions for a data transfer. (Nishida, ¶¶3-4, 15 (INTEL-1006).) It would have been apparent to a POSITA to substitute Nishida’s power control that relies on components other than a CPU with Nakamura’s technique based on power supply control using a CPU. Nishida’s computer system includes computer unit 100, which contains CPU 101. (Nishida, ¶¶3-4, 11, 15-16 (INTEL-1006).) Using Nishida’s or Nakamura’s power supply control approach would have achieved the same result of providing control over power supply functions.

267. In combining Nakamura with the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), a POSITA would have had a reasonable expectation of success. The combination also would have provided predictable results. Nakamura described a known way to provide power supply control at the time of the alleged invention—having a CPU handle control operations. (Nakamura, 6:45-58, 6:67-7:4, 18:1-8 (INTEL-1027).) Nakamura also described that CPU control was effective when addressing operations that “suppl[y] power” and “halt the supply of power.” (Nakamura, 6:45-7:4 (INTEL-1027).) A POSITA would have followed these teachings and applied Nakamura’s known methods of CPU-based power system control in Nishida’s system, which requires control over when a computer system uses an external power supply or, alternatively, a backup power supply. (Nishida, ¶¶2-4, 7, 13, 15 (INTEL-1006).)

268. To implement Nakamura's teachings of CPU-based power supply control in the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari), a POSITA would have used Nishida's computer unit 100 or CPU 101 in the same manner that Nakamura taught using sub-CPU 14 or main CPU 9. The result would have been CPU-based power supply control.

C. “means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system” (limitation 10.a)

269. Annotated and modified Figure 1 from Nishida reproduced below shows the combined system of Nishida, Ergott, Pilukaitis, and Nakamura



(including in further combination with Harari). The figure includes annotations for computer unit 100 (including CPU 101) in blue, power supply monitoring means 107 in gray, power switching switch 108 in orange, the up-converter in green, and the down-converter in purple.

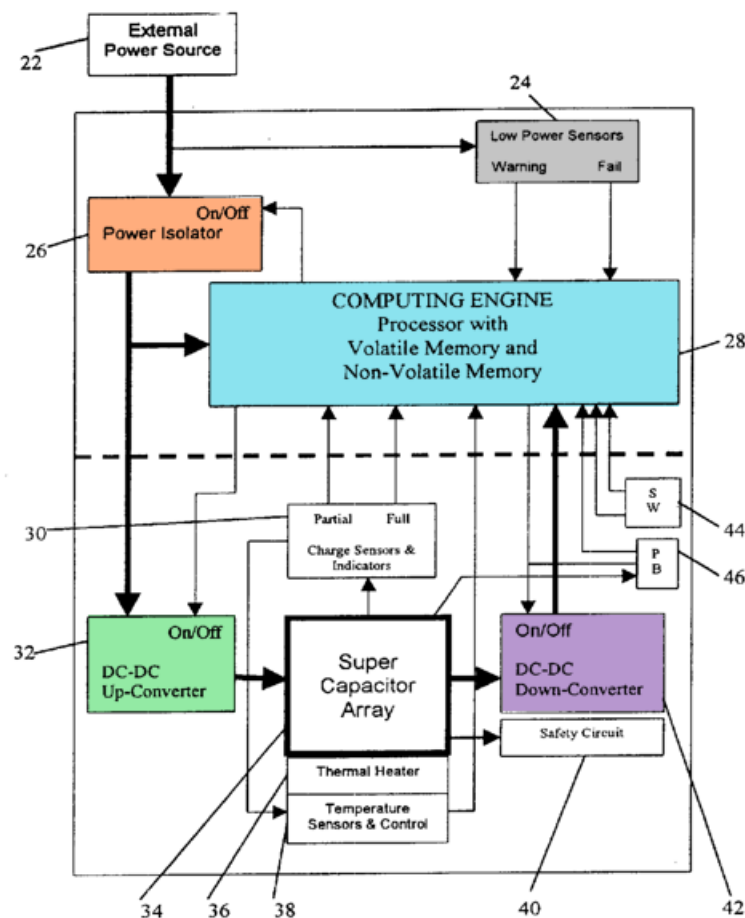
270. As explained in ¶¶116-117 regarding limitation 1.pre, computer unit 100 and CPU 101 are computing engines because each performs computing functions. Computer unit 100 and CPU 101 are also each a processor. Nishida described CPU 101 as a “central **processing** unit.” (Nishida, ¶3 (INTEL-1006).) As just one example of processing, a CPU handles and executes program instructions. (Stallings, 52 (INTEL-1039).) Computer unit 100 qualifies as a processor because it contains CPU 101.

271. In the implementation shown in the figure reproduced above, power supply monitoring means 107 is connected to computer unit 100 and CPU 101 via the signal line between them. In the combination with Nakamura, a POSITA would have controlled the power supply system in Nishida using computer unit 100 and CPU 101. To allow for that control, a signal line between power switching switch 108 and computer unit 100 and CPU 101 would have been added to provide a way for computer unit 100 and CPU 101 to communicate with and therefore control the switches within power switching switch 108. The added signal line

appears in red and connects the common control arm of power switching switch 108 to a signal line that runs to computer unit 100 and CPU 101.

272. In the event of an external power supply interruption, Nishida taught that power supply monitoring means 107 “warns CPU 101,” and computer unit 100 that contains the CPU, “when this supply voltage deviates from a predetermined range” and “switches power supply switching means 108 to the [external power supply] side” on the right. (Nishida, ¶3 (INTEL-1006); *see also* ¶¶4, 15.) The figure reproduced above shows this configuration using two red lines inside power supply switching means 108. Rather than having power supply monitoring means 107 warn computer unit 100 and CPU 101 and then configure power switching switch 108, as part of the combination with Nakamura, computer unit 100 and CPU 101 would have received the warning message and controlled the operation to “switch[] power supply switching means 108 to the [backup power supply] 110 side” on the right. (Nishida, ¶3 (INTEL-1006); *see also* ¶¶4, 15.) As discussed in ¶227, orienting power switching switch 108 to the backup power supply side on the right causes the up-converter to deactivate and the down-converter to activate and electrically connects super-capacitors 110 to a load (computer unit 100), causing the super-capacitors to begin supplying power to the unit. As discussed in ¶227, this configuration of power switching switch 108 to the backup power supply side also isolates the up-converter and external power supply 106.

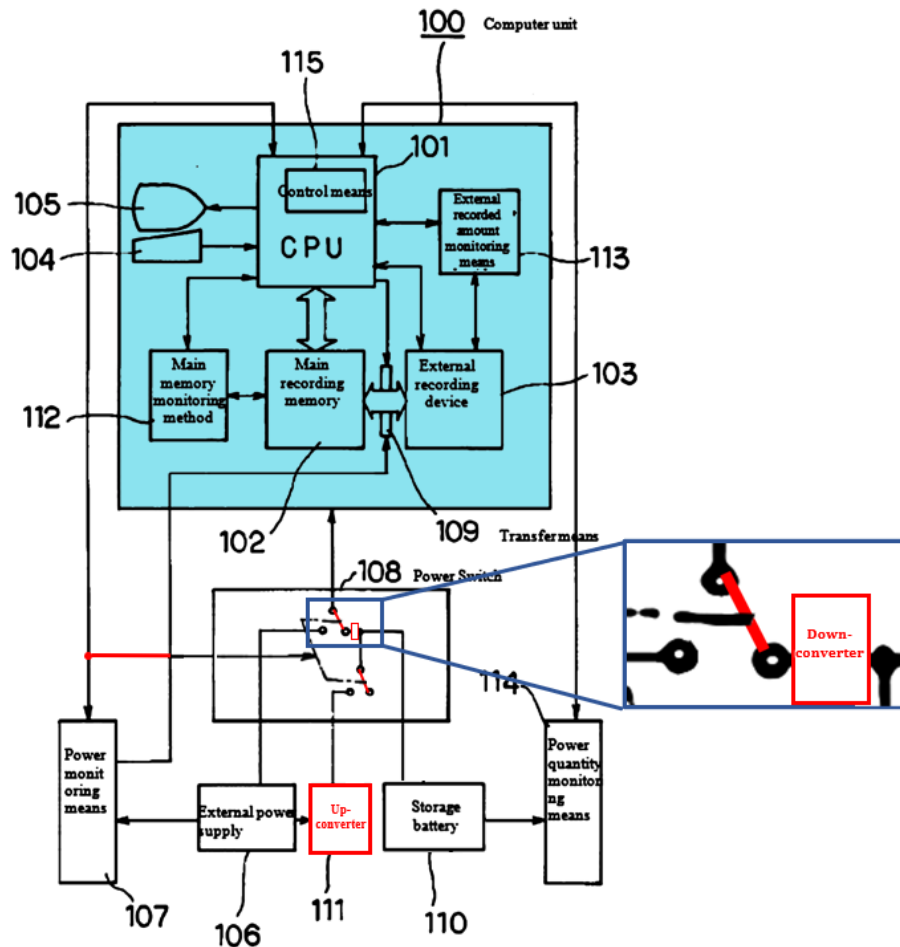
273. The components present in the combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari), as shown in the annotated and modified figure reproduced above, are the same as structures disclosed in the '939 patent. Annotated Figure 1 from the '939 patent reproduced below, shows that the computer system includes computing engine 28 in blue, low power sensors 24 in gray, power isolator 26 in orange, up-converter 32 in green, and down-converter 42 in purple. ('939 patent, 3:29-48 (INTEL-1001).)



**D. “means for reconfiguring the data in the computing engine; and”
(limitation 10.b)**

274. Annotated and modified Figure 1 from Nishida reproduced below shows the combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari). The figure is annotated to show computer unit 100 and CPU 101 in blue.

【Figure 1】



275. As explained in ¶270 regarding limitation 10.a, computer unit 100 and CPU 101 are each a computing engine and a processor. Transfer means 109 “for

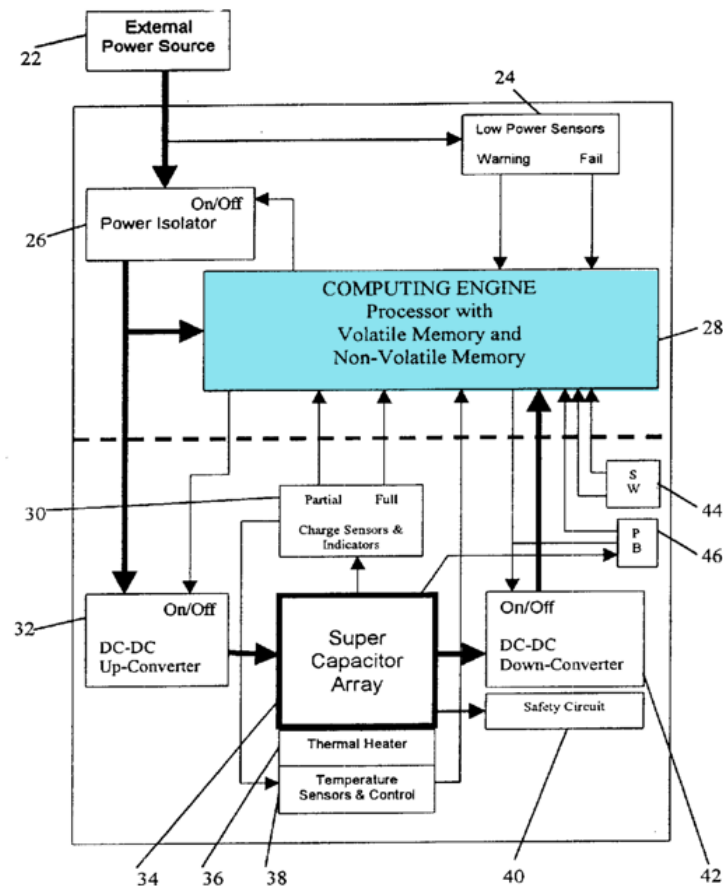
transferring data between the main recording memory 102 and the external recording device 103” is positioned within computer unit 100. (Nishida, ¶3 (INTEL-1006); *see also* ¶¶4, 15.) Transfer means 109 is “instruct[ed]” “to transfer the contents of main recording memory 102 to external recording device 103.” (Nishida, ¶3 (INTEL-1006); *see also* ¶¶4, 15.) All data is transferred. (Nishida, ¶15 (INTEL-1006) (“completely evacuated”).) The data transfer happens after an outage of external power supply 106 has been detected. (Nishida, ¶¶2-4, 15 (INTEL-1006).) Thus, computer unit 100 performs the claimed “*reconfiguring*” of data by transferring data.

276. In the combination with Nakamura, a POSITA would have controlled the power supply system in Nishida using CPU 101. Instead of having transfer means 109 perform the data transfer after an external power supply outage, CPU 101 would have controlled that operation. Nishida disclosed that power supply monitoring means 107 “warns CPU 101 when [the external power supply] deviates from a predetermined range.” (Nishida, ¶¶2-3, 15 (INTEL-1006); *see also* ¶4.) Having received that warning, in the combination with Nakamura, CPU 101 would have responded by initiating a complete data transfer from volatile main recording memory 102 to external recording device 103 (or Harari’s EEPROM).

277. As shown in the annotated and modified figure reproduced above, volatile main recording memory 102 exchanges information with CPU 101. This is

illustrated in the figure using a double-headed arrow between the two structures. Similarly, external recording device 103 (or Harari's EEPROM) is connected to CPU 101 using a signal line. Using these connections, CPU 101 would have initiated a transfer by informing both structures of the transfer operation and by instructing main recording memory 102 to execute the transfer data to external recording device 103 (or Harari's EEPROM). The transfer operation is described in Nishida and the annotated and modified figure reproduced above shows a double-headed arrow between main recording memory 102 and external recording device 103, which indicates the exchange of information between the two structures. (Nishida, ¶3 (INTEL-1006).) As explained in ¶¶118-119, a POSITA would have understood external recording device 103 to include a memory. The use of Harari's EEPROM as an obvious implementation of external recording device 103 is explained in ¶¶120-123 regarding limitation 1.pre.

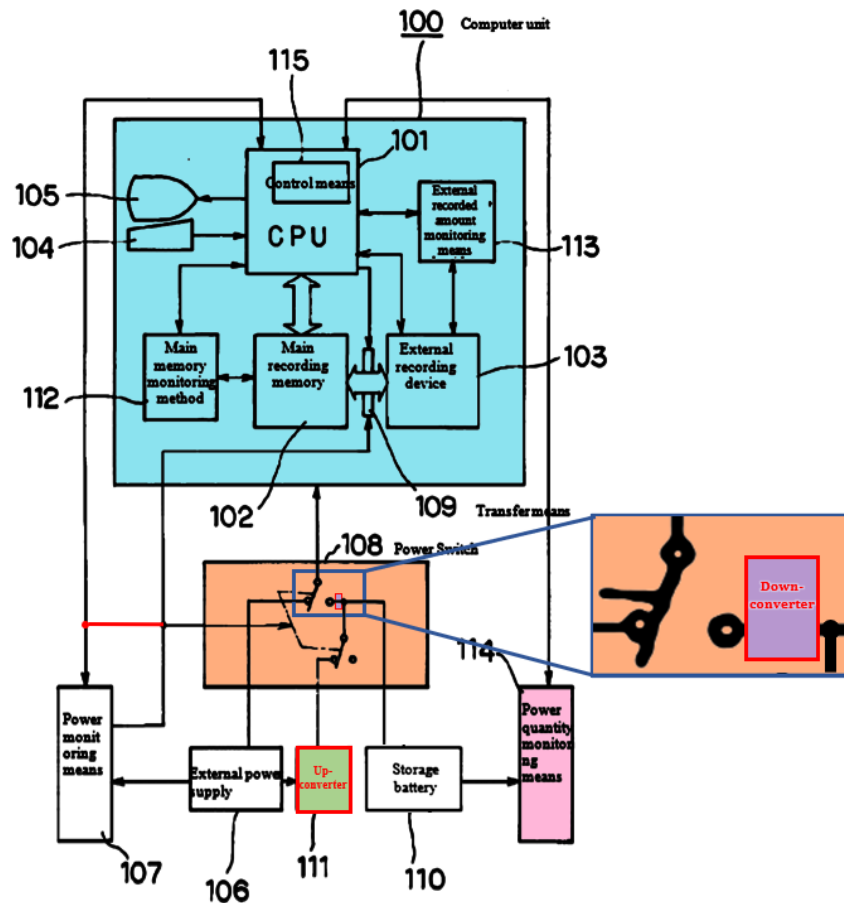
278. The components present in the combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari), as shown in the annotated and modified figure reproduced above, are the same as structures disclosed in the '939 patent. Annotated Figure 1 from the patent reproduced below shows computing engine 28 in blue. Similar to Nishida's computer unit 100, which contains CPU 101, computing engine 28 contains a "processor." ('939 patent, 3:29-36 (INTEL-1001).)



E. *“means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level” (limitation 10.c)*

279. Annotated and modified Figure 1 from Nishida reproduced below shows the combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari). The figure includes annotations for computer unit 100 and CPU 101 in blue, power amount monitoring means 114 in pink, power switching switch 108 in orange, the up-converter in green, and the down-converter in purple.

【Figure 1】



280. As explained in ¶270 regarding limitation 10.a, computer unit 100 and CPU 101 are each a computing engine and a processor. As explained in ¶¶197-203 and 212-213 regarding limitation 1.c, a POSITA would have been motivated to use the undervoltage lockout circuit disclosed in Pilukaitis in a combined system based on the teachings of Nishida and Ergott (including in further combination with Harari). The circuit described in Pilukaitis would have shut down the computer system's voltage down-converter at the point when the input voltage for the voltage down-converter fell below a threshold level.

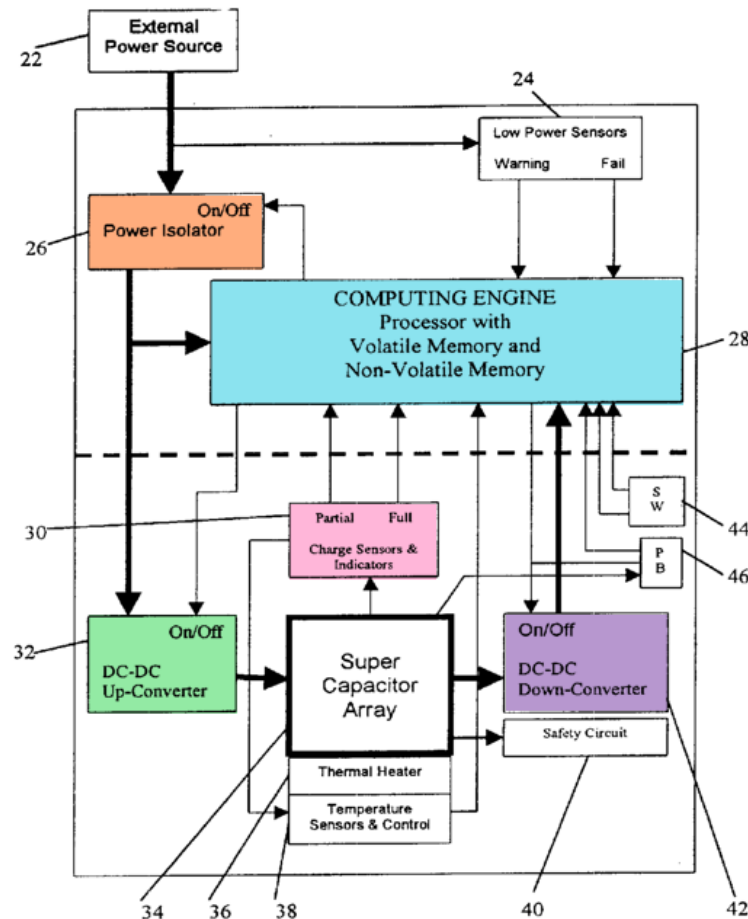
281. As part of the combination between the combined system of Nishida, Ergott, and Pilukaitis (including in further combination with Harari) and Nakamura, a POSITA would have performed that power supply system control function using computer system 100 and CPU 100. The combination based on Nishida includes power amount monitoring means 114. Nishida taught that power amount monitoring means 114 “monitor[s] the current charge amount” of super-capacitors 110 “and report[s] it to the CPU 101” contained in computer unit 100. (Nishida, ¶11 (INTEL-1006); *see also* Summary, ¶14.) As a result of the reporting, computer unit 100 and CPU 101 are informed of the voltage level of the discharging super-capacitors 110, which corresponds to the input voltage of the down-converter. When the down-converter’s input voltage fell below the threshold level, computer unit 100 and CPU 100 would have received that information from power amount monitoring means 114.

282. As discussed in ¶¶271-272 regarding limitation 10.a, a POSITA would have used computer unit 100 and CPU 100 to control the configuration of Nishida’s power switching switch 108 in the combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari). To prevent issues with the down-converter receiving too little voltage from super-capacitors 110, a POSITA would have electrically disconnected super-capacitors 110 from computer unit 100 (the load that receives the power supply from the

super-capacitors). That would have been achieved by configuring power switching switch 108 to the external power supply side on the left, as shown in the annotated and modified figure reproduced above. In this manner, computer unit 100 and CPU 101 would have controlled the power supply system to avoid the consequences of a down-converter input voltage that was low enough to cause malfunctions.

283. As explained in ¶¶226 and 244 regarding limitations 10.a and 10.c, configuring power switching switch 108 to the external power supply side on the left would have resulted in the activation of the up-converter to charge super-capacitors 110 and would have removed the isolation between the voltage up-converter and external power supply 106. The voltage up-converter is not isolated from external power supply 106 because power is supplied to the super-capacitors from external power supply 106 through the voltage up-converter. In addition, the voltage down-converter is deactivated as part of this configuration because it has been electrically disconnected from computer unit 100, which is the load for power discharge when super-capacitors 110 are activated. Once the upper switch of power switching switch 108 is moved to the left side, neither super-capacitors 110 nor the down-converter is electrically connected to computer unit 100. Due to that lack of electrical connection, super-capacitors 110 will not discharge power to the voltage down-converter, and the voltage down-converter will not supply power to computer unit 100.

284. The components present in the combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari), as shown in the annotated and modified figure reproduced above, are the same as structures disclosed in the '939 patent. Annotated Figure 1 from the '939 patent reproduced below shows computing engine 28 in blue, charge level sensors 30 in pink, power isolator 26 in orange, up-converter 32 in green, and down-converter 42 in purple. ('939 patent, 3:29-48 (INTEL-1001).)



F. “means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory” (claim 12)

285. The combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari) rendered the “*means for allowing*” obvious for the reasons explained in ¶¶128-130 regarding limitation 10.b. Computer unit 100 and CPU 101 would have been used by a POSITA to perform a complete transfer of data from volatile main recording memory 102 to external recording device 103 (or Harari’s EEPROM).

G. “means for reversing the flow of current between the computing engine and the plurality of super capacitors” and “means for discharging current from the plurality of super capacitors to the computing engine” (claim 15)

286. The combined system of Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari) rendered the “*means for reversing*” and the “*means for discharging*” limitations obvious for the reasons explained in ¶¶269-273 and 279-284 regarding limitations 10.a and 10.c.

287. A POSITA would have used computer unit 100 and CPU 101 to control the configuration of power switching switch 108 in the combination that includes Nakamura. That would have included orienting the power switching switch 108 (i) to the external power supply side on the left to allow charging of super-capacitors 110 by external power supply 106 or (ii) to the backup power supply side on the right to allow super-capacitors 110 to discharge backup power

to computer unit 100 after an interruption of external power supply 106. In the first mode of operation, current flows **toward** super-capacitors 110. In the second mode of operation, current flows **from** super-capacitors 110. As explained in ¶¶168-172 regarding claim 6, this functionality for the combination that involves Nakamura taught “*reversing*” under the Patent Owner’s construction of that term.

288. Using the computer unit 100 and CPU 101 to control power switching switch 108 also would have rendered the “*means for discharging*” obvious. In the combination that involves Nakamura, when power switching switch 108 is positioned by computer unit 100 or CPU 101 to the backup power supply side on the right, super-capacitors 110 are electrically connected to computer unit 100, which provides the load for super-capacitor discharge. Due to that connection, super-capacitors 110 begin “*discharging current ... to the computing engine*” (either computer unit 100 or CPU 100 in the combination that involves Nakamura), as required by the limitation.

VI. Combinations based on Supercap Manual

289. As explained above, the combination of Nishida, Harari, and Nakao rendered claims 1-3 and 6 obvious; the combination of Nishida, Harari, Ergott, and Pilukaitis rendered claims 1-3, 6, 10-12, and 15 obvious; and the combination of Nishida, Harari, Ergott, Pilukaitis, and Nakamura rendered claims 10-12 and 15 obvious. Adding Supercap Manual to each of these combinations would have

rendered the same claims obvious. Each of the resulting combinations are based on the same reasoning explained above, except that to the extent Nishida does not teach “*a plurality of super-capacitors*” as required by limitations 1.a, 1.c, 10.a, and 10.c and claims 6 and 15, a POSITA would have used more than one super-capacitor in each of the combined systems based on the teachings of the Supercap Manual.

290. Supercap Manual described “high capacitance” capacitors that were designated by NEC as “SUPERCAPs.” (File History of Reasoner including Supercap Manual), 63 (INTEL-1015).) In a section relating to “ordering information,” Supercap Manual identified eight separate series of “super capacitor products.” (File History of Reasoner including Supercap Manual, 66 (INTEL-1015).) Supercap Manual further taught that the super-capacitors known as “SUPERCAPs” “can be used as standby power sources for CMOS memories and microcomputers ... during power outages.” (File History of Reasoner including Supercap Manual), 63 (INTEL-1015).)

291. Supercap Manual provides examples of using super-capacitors to facilitate memory backup. For example, annotated Figure 36 of Supercap Manual reproduced below shows a “memory backup circuit diagram” that includes a decoder with signaling connections to a CPU, four separate blocks of RAM, and a super-capacitor labeled “SUPERCAP.” (File History of Reasoner including

Supercap Manual), 95 (INTEL-1015).) The super-capacitor is shown in red.

Supercap Manual described that “[w]hen higher rated voltage or **greater capacitance (i.e., longer backup time)** is required, it can be obtained by **connecting SUPERCAP in series or in parallel** respectively.” (File History of Reasoner including Supercap Manual), 98 (INTEL-1015).) The teachings of Supercap Manual are straightforward. Connecting super-capacitors in parallel provides higher capacitance and thus increases backup time for a system that receives power from the super-capacitors. As explained in ¶56, increasing capacitance was a known way at the time of the alleged invention to augment the energy stored in a capacitor or group of capacitors.

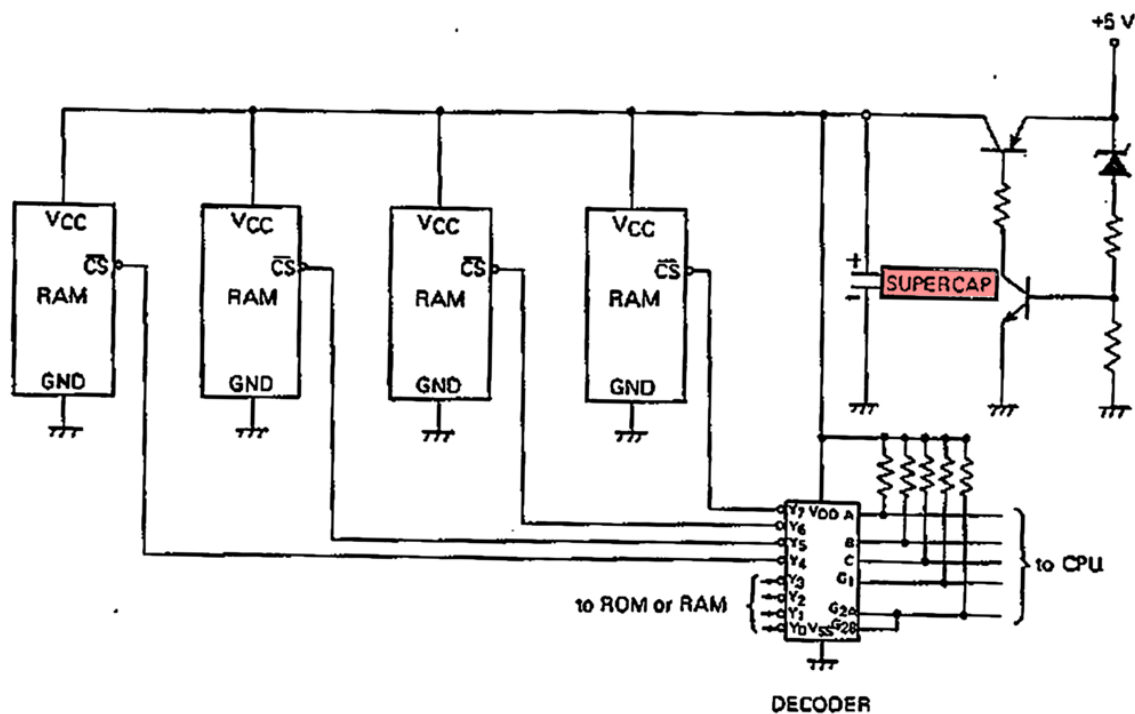


Fig. 36 Memory Backup Circuit Diagram

292. One of the primary objectives of Nishida’s computer system was to detect a “power outage” and rely on a “backup power supply.” (Nishida, ¶2 (INTEL-1006).) “[U]sing the power supply for the backup,” “the data on the main memory is urgently transferred to a non-volatile external recording device.” (Nishida, ¶2 (INTEL-1006).) But if the “charged amount” of the backup power supply “is insufficient to transfer all of the data of the main memory, there is a problem that only a portion of the data of the main memory is backed up.” (Nishida, ¶5 (INTEL-1006).)

293. Supercap Manual described a solution to the problem of partial data transfer due to insufficient backup power supply. A parallel connection of two or more super-capacitors led to greater overall “capacitance” and, as a consequence of increased capacitance, “longer backup time” when a system reliant on the super-capacitors lost external power. (File History of Reasoner including Supercap Manual), 98 (INTEL-1015).) These express teachings in Supercap Manual would have directed a POSITA to use a parallel connection of multiple super-capacitors as the backup power supply in the combinations of Nishida, Harari, and Nakao; Nishida, Harari, Ergott, and Pilukaitis; and Nishida, Harari, Ergott, Pilukaitis, and Nakamura. Applying the technique described in Supercap Manual would have increased both capacitance and backup time in these various systems.

294. The combinations based on Supercap Manual involve using a known technique disclosed in Supercap Manual to improve a similar system based on Nishida in the same way taught in Supercap Manual. Supercap Manual described using two or more super-capacitors in a parallel configuration. (File History of Reasoner including Supercap Manual), 98 (INTEL-1015).) That design for a backup power supply provided known improvements of “greater capacitance” and “longer backup time.” (File History of Reasoner including Supercap Manual, 98 (INTEL-1015).) Similar to Supercap Manual, the combined systems based on Nishida each involved a “backup power supply” that allowed for a transfer of data from volatile memory to non-volatile storage “to protect data.” (Nishida, ¶2 (INTEL-1006).) Nishida sought to avoid partial data transfers when backup power “is insufficient to transfer all of the data.” (Nishida, ¶5 (INTEL-1006).) Supercap Manual’s parallel super-capacitor approach would have improved the combinations based on Nishida by providing more backup time, as taught in Supercap Manual, which would have decreased the likelihood of an incomplete data transfer by providing more capacitance and backup time in which to transfer all data. (Nishida, ¶¶8-9, 14 (INTEL-1006).)

295. A POSITA would have expected to succeed in combining Supercap Manual with the combinations based on Nishida and obtain predictable results. Supercap Manual taught that connecting super-capacitors in a parallel

configuration provided “greater capacitance” and “more backup time.” (File History of Reasoner including Supercap Manual, 98 (INTEL-1015).) Carrying out those teachings in the combinations based on Nishida would have used super-capacitors connected in parallel for their intended purpose disclosed in Supercap Manual of improving a backup power supply by increasing capacitance and backup time.

296. In addition, super-capacitors were known structures at the time of the alleged invention. Supercap Manual catalogued the features of dozens of different SUPERCAPs or “super capacitors.” (File History of Reasoner including Supercap Manual), 66, 69-72 (INTEL-1015).) As explained in ¶¶70-76, other prior art references mentioned super-capacitors, such as NEC’s SUPERCAPs, as known structures. Further, it was known at the time of the alleged invention to connect capacitors in parallel. One reference refers to the voltage characteristics of capacitors connected in parallel: “It was well known to those skilled in the electronic arts that in a dc circuit, ... capacitors coupled in parallel have equal voltages.” (U.S. Pat. No. 5,914,869 (“Troiano”), 3:54-58 (INTEL-1016).) It was also known at the time of the alleged invention that connecting capacitors in parallel provided an increase in capacitance: “Each of the parallel capacitor circuits have a total capacitance and a total temperature compensating value across its terminals.” (U.S. Pat. No. 4,939,779 (“Hitchcock”), 4:17-33 (INTEL-1017).) For

these reasons, a POSITA would have predicted that applying Supercap Manual's teachings in combination based on Nishida would have provided the promised improvements using conventional techniques.

VII. Conclusion

297. In my opinion, the challenged claims of the '939 patent are obvious based on at least the following combinations of prior art references.

- Nishida and Nakao (including in further combination with Harari) (claims 1-3 and 6)
- Nishida, Ergott, and Pilukaitis (including in further combination with Harari) (claims 1-3, 6, 10-12, 15)
- Nishida, Ergott, Pilukaitis, and Nakamura (including in further combination with Harari) (claims 10-12 and 15)
- Nishida, Nakao, and Supercap Manual (including in further combination with Harari) (claims 1-3 and 6)
- Nishida, Ergott, Pilukaitis, and Supercap Manual (including in further combination with Harari) (claims 1-3, 6, 10-12, 15)
- Nishida, Ergott, Pilukaitis, Nakamura, and Supercap Manual (including in further combination with Harari) (claims 10-12 and 15)

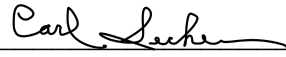
298. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of

the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted for cross-examination.

299. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 1st day of April in Allen, Texas.

Respectfully submitted,

A handwritten signature in cursive script, appearing to read "Carl Sechen", written over a horizontal line.

Dr. Carl Sechen

ATTACHMENT A

EXHIBIT LIST

Exhibit	Reference
INTEL-1001	U.S. Patent No. 6,496,939 (“the ’939 patent”)
INTEL-1002	File History of the ’939 patent
INTEL-1004	CV of Dr. Carl Sechen, Ph.D.
INTEL-1005	Japanese Patent Application Publication No. JPH05-108505 (“Nishida Japanese”)
INTEL-1006	Certified English translation of Japanese Patent Application Publication No. JPH05-108505 (“Nishida”)
INTEL-1007	U.S. Patent No. 5,929,603 (“Nakao”)
INTEL-1008	U.S. Patent No. 4,965,828 (“Ergott”)
INTEL-1009	Plaintiff’s Preliminary Disclosure of Asserted Claims and Infringement Contentions Appendix H, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.)
INTEL-1010	Plaintiff’s Preliminary Disclosure of Asserted Claims and Infringement Contentions Appendix G, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.)
INTEL-1011	Plaintiff BiTMICRO LLC’s Responsive Claim Construction Brief, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 44
INTEL-1012	Defendants’ Opening Claim Construction Brief, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 33
INTEL-1013	Defendants’ Reply Claim Construction Brief, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 43
INTEL-1014	U.S. Patent No. 5,926,383 (“Pilukaitis”)
INTEL-1015	File History of U.S. Patent No. 5,608,684 (“Reasoner”) consisting of “SUPERCAP” (Electric Double-Layer Capacitors) User’s Manual (“Supercap Manual”)
INTEL-1016	U.S. Patent No. 5,914,869 (“Troiano”)
INTEL-1017	U.S. Patent No. 4,939,779 (“Hitchcock”)

Exhibit	Reference
INTEL-1018	Claim Construction Order and Memorandum in Support Thereof, <i>BiTMICRO LLC v. Kioxia Am., Inc.</i> , No. 6:22-cv-00331-ADA (W.D. Tex.), Dkt. 54
INTEL-1019	Plaintiff BiTMICRO LLC's Sur-Reply Claim Construction Brief, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 47
INTEL-1020	U.S. Patent No. 5,705,919 ("Wilcox")
INTEL-1021	Case transfer notice, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 5:23-cv-00625 (W.D. Tex.), Dkt. 56
INTEL-1022	U.S. Patent No. 5,542,042 ("Manson")
INTEL-1023	U.S. Patent No. 5,768,208 ("Bruwer")
INTEL-1024	U.S. Patent No. 5,535,328 ("Harari")
INTEL-1025	U.S. Patent No. 3,854,226 ("Divine")
INTEL-1026	U.S. Patent No. 6,629,317 ("Kirschner")
INTEL-1027	U.S. Patent No. 5,710,931 ("Nakamura")
INTEL-1028	U.S. Patent No. 5,078,134 ("Heilman")
INTEL-1029	U.S. Patent No. 6,222,356 ("Taghizadeh-Kaschani")
INTEL-1030	U.S. Patent No. 5,608,684 ("Reasoner")
INTEL-1031	U.S. Patent No. 4,974,167 ("Anderson")
INTEL-1032	U.S. Patent No. 5,914,542 ("Weimer")
INTEL-1033	U.S. Patent No. 5,444,378 ("Rogers")
INTEL-1034	U.S. Patent No. 4,559,616 ("Bruder")
INTEL-1035	U.S. Patent No. 4,327,410 ("Patel")
INTEL-1036	U.S. Patent No. 5,519,831 ("Holzhammer")
INTEL-1037	"The Art of Electronics," 2nd Edition, 1989 by Horowitz, et al. ("Horowitz")
INTEL-1038	"Principles of Physics," 2nd Edition, 1998 by Serway ("Serway")
INTEL-1039	"Computer Organization and Architecture," 4th Edition, 1996 by Stallings ("Stallings")

Exhibit	Reference
INTEL-1040	U.S. Patent No. 5,627,460 (“Bazinet”)
INTEL-1041	“Historical Introduction to Capacitor Technology,” IEEE Electrical Insulation Magazine, Vol. 26, Issue 1, January 2010, by Ho, et al. (“Ho”)
INTEL-1042	“The Illustrated Dictionary of Electronics,” 5th Edition, 1990 by Turner, et al., 157.
INTEL-1043	Summon with Proof of Service, <i>BiTMICRO LLC v. Intel Corp.</i> , No. 6:22-cv-00335-ADA (W.D. Tex.), Dkt. 9
INTEL-1044	United States District Court — National Judicial Caseload Profile
INTEL-1045	U.S. Patent No. 5,959,926 (“Jones”)