

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BITMICRO, LLC,
Patent Owner.

IPR2023-00783
Patent 6,496,939 B2

Before KEN B. BARRETT, TERRENCE W. MCMILLIN, and
KEVIN C. TROCK, *Administrative Patent Judges*.

TROCK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–3, 6, 10–12, and 15 (the “challenged claims”) of U.S. Patent No. 6,496,939 B2 (Ex. 1001, “the ’939 patent”). BiTMICRO, LLC (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”). With our approval, Petitioner filed a Preliminary Reply addressing the prior art status of one of the asserted references. Paper 7 (“Prelim. Reply”). Patent Owner filed a Preliminary Sur-reply addressing the same issue. Paper 8 (“Prelim. Sur-reply”).

The Board has authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), we may not authorize an *inter partes* review unless the information in the petition and the preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one of the challenged claims. We therefore institute *inter partes* review as to all of the challenged claims of the ’939 patent on all of the asserted grounds of unpatentability in the Petition.

II. BACKGROUND

A. *Related Matters*

The parties identify the following district court proceedings involving the ’939 patent: *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, No. 6:22-cv-00331 (W.D. Tex. 2022); *BiTMICRO LLC v. Intel Corp.*, No. 5:23-cv-00625 (N.D. Cal.). Pet. 90–91; Paper 3, 2. The parties also identify a related

USPTO proceeding: IPR2023-00743 (PTAB),¹ involving the '939 patent.
Pet. 91; Paper 3, 2.

B. Real Parties-in-Interest

Petitioner identifies itself, Intel Corporation, as real party-in-interest.
Pet. 90. Patent Owner identifies itself, BitMicro, LLC, as the real party-in-interest. Paper 3, 2.

Based on the current record, we determine that Petitioner has established compliance with the statutory requirement under 35 U.S.C. § 312(a)(2) to identify all real parties in interest.

C. The '939 Patent

The '939 patent is entitled “Method and System for Controlling Data in a Computer System in the Event of a Power Failure.” Ex. 1001, code (54). According to the '939 patent, when there is a sudden loss of external power to a computer system there is insufficient time to safely write all the newly written and modified data from the computer's volatile memory to the computer's data storage mechanism before the computer system shuts down. *Id.* at 1:34–38. The '939 patent explains that in accordance with the invention, “if a system is in ‘save mode’ and is subsequently subjected to a sudden power loss, first, the super-capacitors are activated to maintain the internal power of the system.” *Id.* at 5:8–11. The '939 patent goes on to explain that “data from the volatile memory is transferred to the non-volatile memory . . . [so that] a user is able to quickly and correctly transfer all data from volatile memory to non-volatile memory in the event of a sudden power loss.” *Id.* at 5:11–16.

¹ IPR2023-00743 was terminated on November 14, 2023. IPR2023-00743, Paper 12.

Figure 1, reproduced below, shows a schematic of the '939 patent's system.

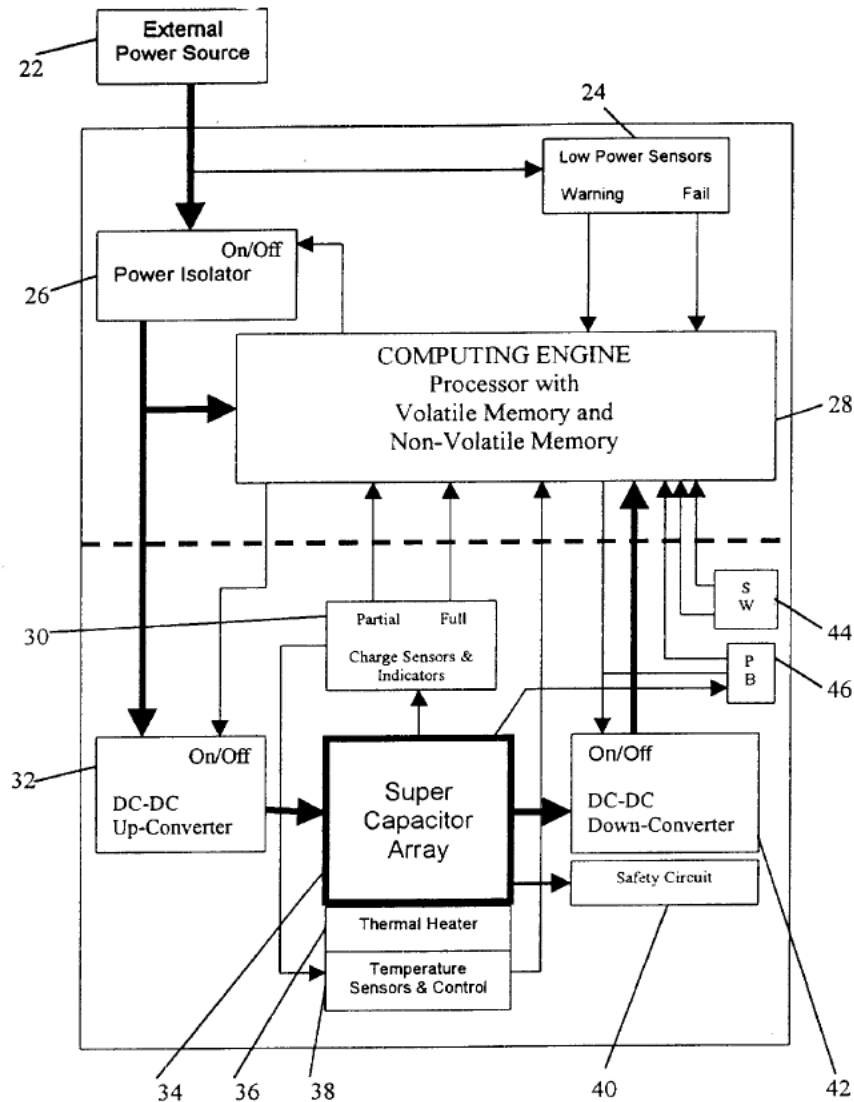


Figure 1, above, shows computing engine 28 comprising a processor with volatile memory and non-volatile memory, external power source 22, power isolator 26, DC-DC up-converter 32, DC-DC down-converter 42, and super capacitor array 34. *Id.* at 3:33–41.

The '939 patent explains that “[w]hile the computer system is receiving current from the super-capacitors, data is transferred from the volatile memory to the non-volatile memory,” but “once the super-capacitors

discharge to a pre-determined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system.” *Id.* at 5:33–43.

The ’939 patent explains that this shut down has two positive side effects. “First,” the patent explains, “if the output voltage from the down-converter were allowed to fall below the minimum operating voltage of the computer system, the computer system could continue to run with unpredictable and potentially serious results.” *Id.* at 5:44–48. Second, “by not fully discharging the super-capacitors they will take only a few seconds to recharge once the external system power is restored, whereas the initial charge of super-capacitors may take up to 5 minutes.” *Id.* at 5:48–52.

D. Illustrative Claim

The ’939 patent has 28 claims. As noted, claims 1–3, 6, 10–12, and 15 are challenged in the Petition. Pet. 1. Claim 1, a method claim, and claim 10, a system claim, are independent. Ex. 1001, 7:20–10:34. Claim 1 is illustrative of the claimed subject matter and is reproduced below:²

1. [1.pre] A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

[1.a] activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;

[1.b] reconfiguring the data in the computing engine; and

[1.c] deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

² Paragraph references in brackets proposed by Petitioner. *See* Pet. 15–23.

Ex. 1001, 7:20–31.

E. Prior Art References and Other Evidence

Petitioner relies on the following references:

1. Nishida, Japanese Patent Appl. Pub. No. JPH05-108505 (April 30, 1993), (Ex. 1006, “Nishida”)³.
2. Harari, U.S. Patent No. 5,535,328 (July 9, 1996) (Ex. 1024, “Harari”).
3. Nakao, U.S. Patent No. 5,929,603 (July 27, 1999) (Ex. 1007, “Nakao”).
4. Ergott, U.S. Patent No. 4,965,828 (October 23, 1990) (Ex. 1008, “Ergott”).
5. Pilukaitis, U.S. Patent No. 5,926,383 (July 20, 1999) (Ex. 1014, “Pilukaitis”).
6. Nakamura, U.S. Patent No. 5,710,931 (January 20, 1998) (Ex. 1027, “Nakamura”).
7. “SUPERCAP” (Electric Double-Layer Capacitors) User’s Manual (bearing a 1985 copyright date) (Ex. 1015, “Supercap”).

In addition to these references, Petitioner relies on a Declaration of Dr. Carl Sechen. Ex. 1003.

³ This is a certified translation of the original Japanese-language version that is Exhibit 1005.

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 3.

Claim(s) Challenged	Basis 35 U.S.C. §	Reference(s)
1–3, 6	103(a) ⁴	Nishida, Harari, Nakao
1–3, 6, 10–12, 15	103(a)	Nishida, Harari, Ergott, Pilukaitis
10–12, 15	103(a)	Nishida, Harari, Ergott, Pilukaitis, Nakamura
1–3, 6	103(a)	Nishida, Harari, Nakao, Supercap
1–3, 6, 10–12, 15	103(a)	Nishida, Harari, Ergott, Pilukaitis, Supercap
10–12, 15	103(a)	Nishida, Harari, Ergott, Pilukaitis, Nakamura, Supercap

III. ANALYSIS OF THE CHALLENGED CLAIMS

A. Applicable Legal Standards

A claim is unpatentable as obvious under 35 U.S.C. § 103 “if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103 (2011). The question of obviousness is resolved on the basis of underlying factual

⁴ Because the application from which the ’939 patent issued has an effective filing date before March 16, 2013 (Ex. 1001, code (22)), citations to 35 U.S.C. § 103 are to the pre-AIA version. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29.

determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

B. Level of Ordinary Skill in the Art

According to Petitioner, a person of ordinary skill in the pertinent art “would have had at least a bachelor’s degree in electrical or computer engineering and two years of experience working on computer system architecture and power management circuits, or an equivalent combination of education and experience.” Pet. 7 (citing Ex. 1003 ¶ 90).

Patent Owner does not address the level of skill of the ordinary artisan. *See generally* Prelim. Resp.

We regard Petitioner’s definition as consistent with the ’939 patent and the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Therefore, for the purpose of this decision, we adopt Petitioner’s formulation.

C. Claim Construction

For this *inter partes* review, the Board applies the same claim construction standard as that applied in federal courts. *See* 37 C.F.R. § 42.100(b) (2019). Under this standard, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v.*

AWH Corp., 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc) (citations omitted). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Extrinsic evidence is “less significant than the intrinsic record in determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317 (citation omitted).

Only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Some of the challenged claims make use of “means-plus-function” claiming. *See* 35 U.S.C. § 112 ¶ 6. Means-plus-function claiming occurs when a claim term is drafted in a manner that invokes 35 U.S.C. § 112 ¶ 6, which states:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

See 35 U.S.C. § 112 ¶ 6; *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347 (Fed. Cir. 2015) (en banc).

On the record before us, we have not been directed to any dispute between the parties that § 112 ¶ 6 does not apply to the “means for” clauses

recited in the challenged claims. Where claim language may be construed according to 35 U.S.C. § 112(f) (or its predecessor, § 112 ¶ 6), a petitioner must provide a construction that includes both the claimed function and the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function. 37 C.F.R. § 42.104(b)(3).

In accordance with these requirements, Petitioner provides constructions for all the means-plus-function clauses in the challenged claims. *See* Pet. 7–15. Where applicable, Petitioner asserts its proposed constructions are consistent with constructions made by the district court in related litigation. *Id.*; *see also* Ex. 1018.

Patent Owner contends “the Board need not engage in any pre-institution claim construction,” does not substantively address or contest Petitioner’s proposed claim constructions, and does not propose any constructions itself. *See* Prelim. Resp. 8–10.

Based on the record before us, we adopt, for purposes of this Decision, Petitioner’s unopposed claim constructions. This initial claim construction determination does not preclude the parties from arguing their proposed constructions of the claims during trial. Indeed, the parties are hereby given notice that claim construction, in general, is an issue to be addressed at trial. Claim construction will be determined at the close of all the evidence and after any hearing. The parties should assert all their claim construction arguments and evidence in the Petition, Patent Owner’s Response, or otherwise during trial, as permitted by our rules.

1. “*means for activating*” (*claim 10*)

Petitioner proposes that this term, recited in claim 10, should be construed as means-plus-function, with a recited function being “activating a

plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system,” and the corresponding structure being “an up-converter and a down-converter (and equivalents).” Pet. 8–9.

Patent Owner does not provide a construction or any specific arguments directed to this limitation. *See* Prelim. Resp. 8–10.

2. *“means for reconfiguring” (claim 10)*

Petitioner proposes that this term, recited in claim 10, should be construed as means-plus-function, with a recited function being “reconfiguring the data in the computing engine,” and the corresponding structure being a “non-volatile memory and volatile memory (and equivalents).” Pet. 9–10.

Petitioner explains that the ’939 patent describes a method and system for “controlling data . . . when the computer system loses power,” which includes “reconfiguring the data in the computing engine.” *Id.* at 10 (citing Ex. 1001, 2:25–32; *see also id.* at 3:33–35 (“Computing engine CE 28 contain[s]” “volatile and non-volatile memory”), 4:9–28, 4:42–46, 4:37–41, 5:6–16, 5:33–36, 6:54–67).

Patent Owner does not provide a construction or any specific arguments directed to this limitation. *See* Prelim. Resp. 8–10.

3. *“means for deactivating” (claim 10)*

Petitioner proposes that this term, recited in claim 10, should be construed consistent with the district court construction as means-plus-function, with the recited function being “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level” and the

corresponding structure as “a down-converter (and equivalents), and switches, transistors, gates, etc. that are generally known in the art.” Pet. 10–12.

Patent Owner does not provide a construction or any specific arguments directed to this limitation. *See* Prelim. Resp. 8–10.

4. *“means for allowing” (claim 12)*

Petitioner proposes that this term, recited in claim 12, should be construed as means-plus-function with the recited function being “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory” and the corresponding structure being a “volatile and non-volatile memory (and equivalents).” Pet. 12–13.

Patent Owner does not provide a construction or any specific arguments directed to this limitation. *See* Prelim. Resp. 8–10.

5. *“means for reversing” (claim 15)*

Petitioner proposes that this term, recited in claim 15, should be construed as means-plus-function with the recited function being “reversing the flow of current between the computing engine and the plurality of super capacitors” and the corresponding structure being “a down-converter and an up-converter (and equivalents).” Pet. 13–14.

Patent Owner does not provide a construction or any specific arguments directed to this limitation. *See* Prelim. Resp. 8–10.

6. *“means for discharging” (claim 15)*

Petitioner contends that this term, recited in claim 15, should be construed as means-plus-function, with the recited function being “discharging current from the plurality of super capacitors to the computing

engine,” and the corresponding structure being “an up-converter and a down-converter (and equivalents).” Pet. 14–15.

Patent Owner does not provide a construction or any specific arguments directed to this limitation. *See* Prelim. Resp. 8–10.

D. Prior Art References

1. Nishida (Ex. 1005)

Nishida is a Japanese, unexamined patent application publication titled “Computer system with memory backup guaranteed amount display function.” Ex. 1006, code (54). Nishida “relates to computer systems with memory backup functions.” *Id.* ¶ 1. Nishida seeks to “provide the computer system equipped with a memory backup function which can previously recognize whether backup can be completely executed or not, and raises an alarm when the backup can not be completely executed.” *Id.* at code (57).

Figure 1, reproduced below, is a block diagram of Nishida’s computer system.

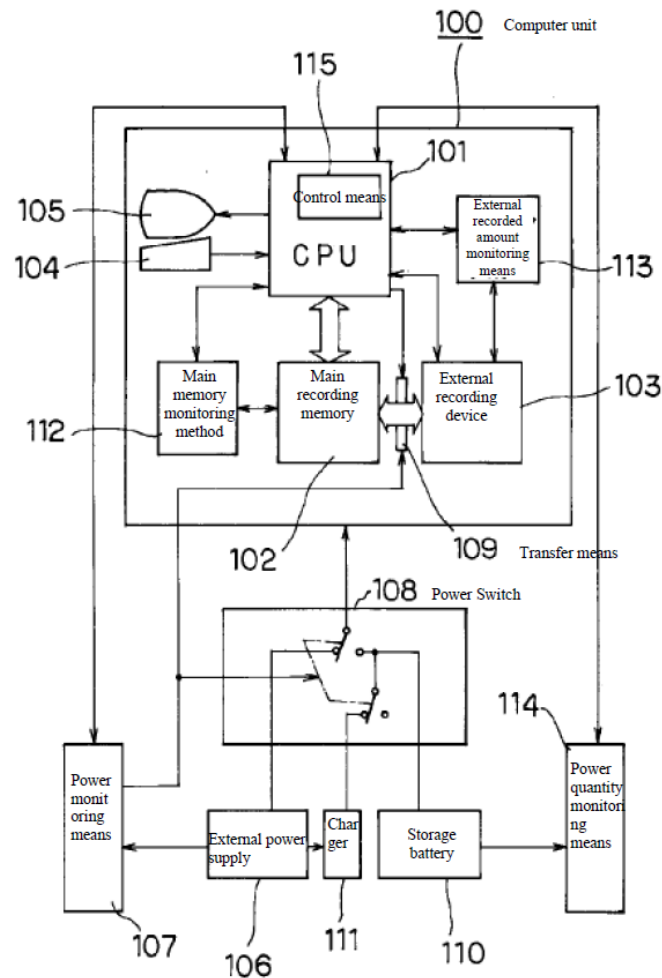


Figure 1 illustrates computer system 100, including CPU 101, main memory 102, recording device 103, power supply 106, charger 111, power monitor 114, battery 110, and main memory monitor 112. *Id.* ¶¶ 11–14.

Nishida’s system “calculates the maximum amount of data (memory backupable amount) that can be transferred from the main recording memory 102 to the external recording device 103 by only the power from the storage battery 110 when a memory backup must be performed.” *Id.* ¶ 14. However, if the amount of data to be transferred “exceeds the memory backup possible amount, the control means 115 causes the display device 105 to display an alarm and interrupts the execution of data transfer

instructions from the external recording device 103 to the main recording memory 102 until there is a predetermined input.” *Id.*

Nishida further discloses:

if the supply voltage of the external power supply 106 deviates from the predetermined range, the power supply switching switch 108 is immediately switched to the storage battery 110 side by means of the power supply monitoring means 107, and this computer system is activated by power from the storage battery 110. At the same time, the CPU 101 initiates a shutdown process by warning from the power supply monitoring means 107, and the transfer means 109 initiates the transfer of the contents of the main recording memory 102 to the external recording device 103.

Id. ¶ 15.

2. *Harari (Ex. 1024)*

Harari is a patent titled “Non-Volatile Memory System Card with Flash Erasable Sectors of EEPROM Cells Including a Mechanism for Substituting Defective Cells.” Ex. 1024, code (54). Harari “relates generally to semiconductor electrically erasable programmable read only memories (EEPROM), and specifically to a system of integrated circuit Flash EEPROM chips.” *Id.* at 1:18–21.

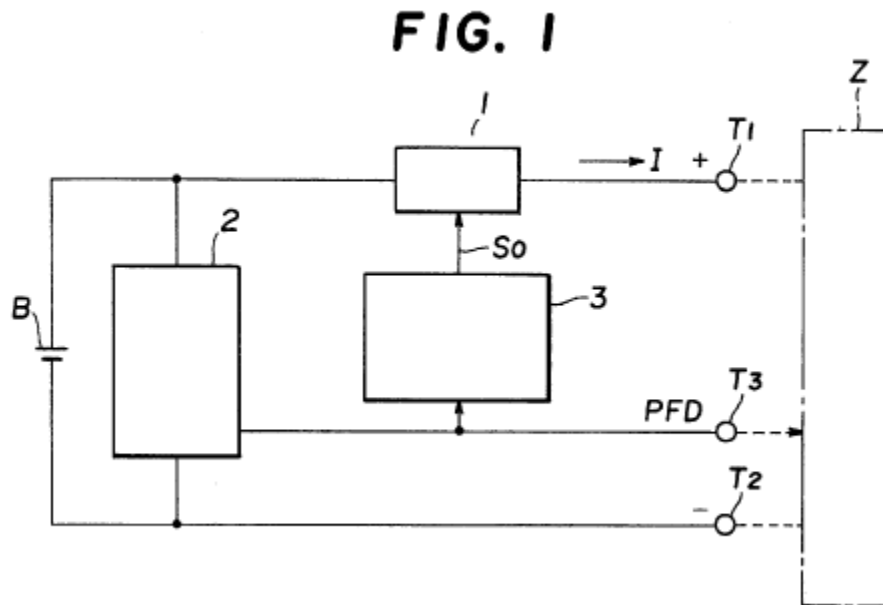
Harari describes “it is an object of the present invention to provide a Flash EEPROM memory system with enhanced performance and which remains reliable after enduring a large number of write/erase cycles,” and “to provide an improved Flash EEPROM system which can serve as non-volatile memory in a computer system.” *Id.* at 1:44–50. Harari discloses using “an array of electrically erasable programmable read only memories (EEPROM’s) integrated circuit chips. This type of memory has additional advantages of requiring less power to operate, and of being lighter in weight

than a hard disk drive magnetic media memory, thereby being especially suited for battery operated portable computers.” *Id.* at 3:52–58.

3. *Nakao (Ex. 1007)*

Nakao is titled “Apparatus for Preventing Over-Discharge.” Ex. 1007, code (54). Nakao “relates to an apparatus for preventing over-discharge in various kinds of accumulator elements such as a secondary battery, primary battery and large-scale capacitors, etc.” *Id.* at 1:4–13. Nakao seeks “to provide a new and reliable over-discharge prevention apparatus which permits safety of the data and information of external electronic apparatuses and instruments at the time of an extinction voltage of the batteries and, improvements in utilization efficiency of the batteries.” *Id.* at 2:6–11.

Nakao’s Figure 1 is shown below.



Nakao’s Figure 1, above, is a block diagram of a typical structure of a battery package provided with an over-discharge prevention apparatus

comprising secondary battery B mounted within a battery package with positive electrode (+) connected through switching portion 1 to source terminal T1, and negative electrode (-) connected to ground terminal T2 such that electric power is provided to external apparatuses and instruments Z. Ex. 1007, 2:45–48, 2:66–3:15. Voltage detector 2 is provided for detecting voltage of battery B. An output side of voltage detector 2 is connected with discharge controller 3 and also connected with terminal T3 as an electric line for a discharge finishing signal PFD for the external apparatuses and instruments Z. *Id.* at 3:5–10.

If the battery voltage is above a discharge finishing voltage VL (that is, a limited voltage for finishing the discharge), voltage detector 2 maintains its inoperative state, and switching portion 1 is turned into its ON-state so that discharge current I is supplied to the external apparatuses and instruments Z through the terminals T1, and T2. *Id.* at 3:15–26. External apparatuses and instruments Z always monitor the state and conditions of the battery via the electric line for the discharge finishing signal PFD transmitted through the terminal T3. *Id.* at 3:26–30.

When the battery voltage becomes lower than the discharge finishing Voltage VL, voltage detector 2 is driven to output a discharge finishing signal PFD. *Id.* at 3:32–34. When the external apparatuses and instruments receive an ON-state of the discharge finishing signal PFD, the external apparatuses and instruments judge the battery to be in a used-up consumed state and therefore begin stopping the operation of the external apparatuses and instruments. *Id.* at 3:34–40. “[T]he over-discharge detection output . . . at the discharge controller 3 . . . will make the switching portion 1 of the

next stage change to an OFF state and then the electric power supply to the external apparatuses and instruments Z is stopped.” *Id.* at 3:40–45.

4. *Ergott (Ex. 1008)*

Ergott, titled “Non-Volatile Semiconductor Memory with Scram Hold Cycle Prior to Scram-to-E²PROM Backup Transfer,” “relates to non-volatile semiconductor memory systems including a volatile high speed SRAM (static random access memory), a non-volatile E²PROM (electrically erasable programmable read only memory) backup memory, and circuitry for transferring the contents of the SRAM to the E²PROM in response to onset of a power interruption or failure.” Ex. 1014, code (54), 1:7–13.

Ergott describes “an unmet need for a non-volatile memory system which includes a volatile semiconductor RAM and a non-volatile backup memory to which data in the RAM is downloaded during power interruptions and from which data is uploaded into the RAM after power interruptions.” *Id.* at 2:28–37.

To address this, Ergott describes a memory system where “[i]f there is a power interruption or failure, non-volatile energy system 1 acts as a backup memory that contains all of the data in SRAM 2 immediately before the interruption of input power 10.” *Id.* at 5:26–29. Ergott discloses that “downloading is initiated if the voltage stored on the backup capacitor falls below the pre-defined threshold, typically about 80% below the nominal backup energy level.” *Id.* at 5:45–48. Ergott’s “controller circuit 22 applies full power from the energy storage circuit 6 to all or nearly all of the circuitry.” *Id.* at 5:48–52. Ergott’s energy storage circuitry “includes a voltage up converter that boosts the external 5 volt power supply voltage to charge up a 1,000 to 5,000 microfarad backup capacitor to approximately

100 volts.” *Id.* at 6:62–68. The 100 volts is converted back down to the internal 5 volt supply voltage whenever the external 5 volt level is interrupted, by slowly discharging the energy stored in the backup capacitor. *Id.* at 7:1–6.

5. *Pilukaitis (Ex. 1014)*

Pilukaitis, titled “Integrated Protection Circuit for a Power Converter and Method of Operation Thereof,” “provides for use with a controller, couplable to a network of first and second comparators, that disables a power converter an actual output current thereof exceeds a threshold output current, an integrated protection circuit and method of operating the same.” Ex. 1014, code (54), 2:29–34.

Pilukaitis describes that “[o]vercurrent, undervoltage and overvoltage protection circuits have been separately used for power supplies for more than a decade.” *Id.* at 1:13–15. Pilukaitis describes a need for “a circuit that combines at least overcurrent and undervoltage protections in an integrated fashion.” *Id.* at 2:21–25.

Pilukaitis’ integrated protection circuit includes:

(1) a sensor that senses an actual input voltage of the power converter and (2) an isolation circuit, coupled to the first comparator, that selectively decouples the first comparator from the second comparator, the second comparator causing the controller to disable the power converter when the actual input voltage falls below a threshold input voltage thereby allowing the protection circuit to provide both overcurrent and undervoltage protection.

Id. at 2:34–43.

6. *Nakamura (Ex. 1027)*

Nakamura is titled “Suspension State Control for Information Processing Devices such as Battery Powered Computers.” Ex.1027, code

(54). Nakamura relates to “a notebook personal computer (hereafter referred to a ‘notebook PC’), that has a suspension function that temporarily halts the supply of power as needed and a resume function that, when power is again supplied, immediately places the computer in the state in which it was before it was halted.” *Id.* at 1:9–16.

Figure 2, reproduced below, is a block diagram illustrating a control system within the notebook PC.

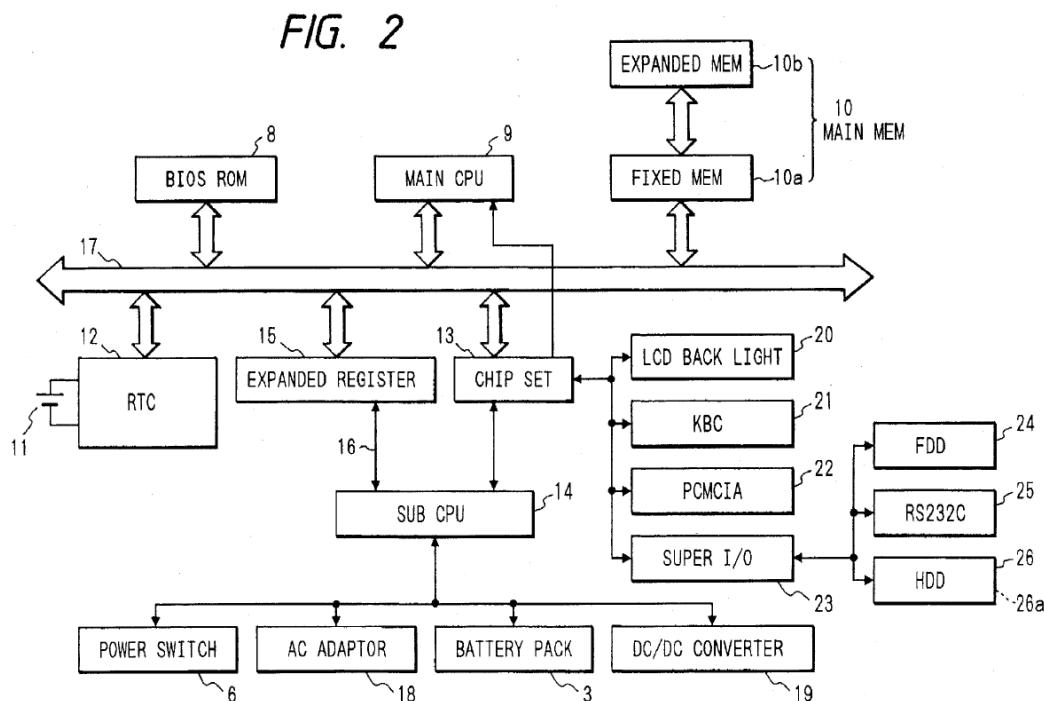


Figure 2 illustrates BIOS ROM 8, main CPU 9, main memory 10, battery 11 (part of RTC 12), chip set 13 for controlling I/O units, sub-CPU 14 for controlling a power supply system, and register 15 for exchanging data between sub-CPU 14 and the main CPU 9. *Id.* at 6:46–58.

7. Supercap (Ex. 1015)

“Supercap” (Electric Double-Layer Capacitors) is an NEC “User’s Manual” bearing an NEC Corporation 1985 copyright date. Ex. 1015, 62. The manual explains:

SUPERCAP is a completely innovative type of capacitor providing a volumetric efficiency (capacitance per unit volume of a given voltage) of 10 to 50 times that of conventional aluminum electrolytic capacitors. The high capacitance (2 200 000 microfarads) and kagecurrentmakes the SUPERCAP an efficient, reliable, and cost effective energy storage device. SUPERCAP can be used as standby power sources for CMOS memories and microcomputers up to several weeks during power outages.

Id. at 63. The manual also describes that “[w]hen higher rated voltage or greater capacitance (i.e., longer backup time) is required, it can be obtained by connecting SUPERCAP in series or in parallel respectively.” *Id.* at 98 (§ 5.7).

a) Prior Art Status of Supercap

Petitioner explains that the asserted prior art combinations for Grounds 4–6 “are identical to those described above in Grounds 1–3 except that, in addition to Nishida’s teachings of multiple ‘supercapacitors’” a person of ordinary skill in the art “also would have been motivated to use multiple super-capacitors based on Supercap Manual’s teachings.” Pet. 83–84 (citing Ex. 1006 ¶ 2).

In its Preliminary Response, Patent Owner argues that “Petitioner fails to establish that the Supercap Manual is a printed publication constituting prior art.” Prelim. Resp. 21. Petitioner argues that “there is no showing that the Supercap Manual would have been sufficiently accessible to the public interested in the relevant art,” because 1) “Reasoner is not available online through the USPTO’s Patent Center,” 2) “Petitioner presents no testimony or other evidence that the Supercap Manual . . . would have been sufficiently accessible to the public interested in the art,” and 3) “there [is] absolutely no

evidence that the Supercap Manual was independently available as a ‘printed publication.’” *Id.* at 21–24.

We gave the parties leave to file supplemental briefing on this issue. *See* Papers 7, 8. After reviewing the parties briefing, we are concerned that neither party cited, or addressed, one of the Board’s precedential decisions directed to this issue, *Hulu, LLC v. Sound View Innovations, LLC*, Case IPR2018-01039, Paper 29 (PTAB December 20, 2019) (precedential).

Hulu determined that “[f]or institution of an *inter partes* review, a petitioner must establish a reasonable likelihood that a reference is a printed publication. If trial is instituted, the petitioner will ultimately have the burden to prove that the reference is a printed publication by a preponderance of the evidence.” *Hulu*, Paper 29 at 21.

In its briefing Patent Owner merely argues that “[i]t is Petitioner’s burden to establish that a document is a printed publication. *Nobel Biocare Servs. AG v. Instradent USA, Inc.*, 903 F.3d 1365, 1375 (Fed. Cir. 2018), *as amended* (Sept. 20, 2018). Petitioner has failed to meet this burden.” Prelim. Sur-reply 3. Petitioner, as far as we can tell, does not even address the appropriate burden of proof for printed publications at the preliminary proceeding stage. *See generally* Prelim. Reply.

Because we determine that Petitioner has shown sufficiently for purposes of institution that the combined teachings of Nishida, Harari, and Nakao meet the limitations of independent claim 1 under Ground 1, we do not reach the question of whether the Supercap reference qualifies as printed publication prior art at this stage of the proceeding. Nevertheless, we direct the parties to consider, as appropriate, our rules concerning the submission of evidence and the guidance set forth in *Hulu*, which explains that

We do not opine at this stage of the proceeding as to the ultimate determination of whether Petitioner will establish by a preponderance of the evidence—the standard to prevail at trial (35 U.S.C. § 316(e))—that Dougherty is a printed publication. Should trial be instituted, Patent Owner may challenge Petitioner’s evidence, and Petitioner may respond if appropriate, as indicated herein.

Hulu, Paper 29 at 21.

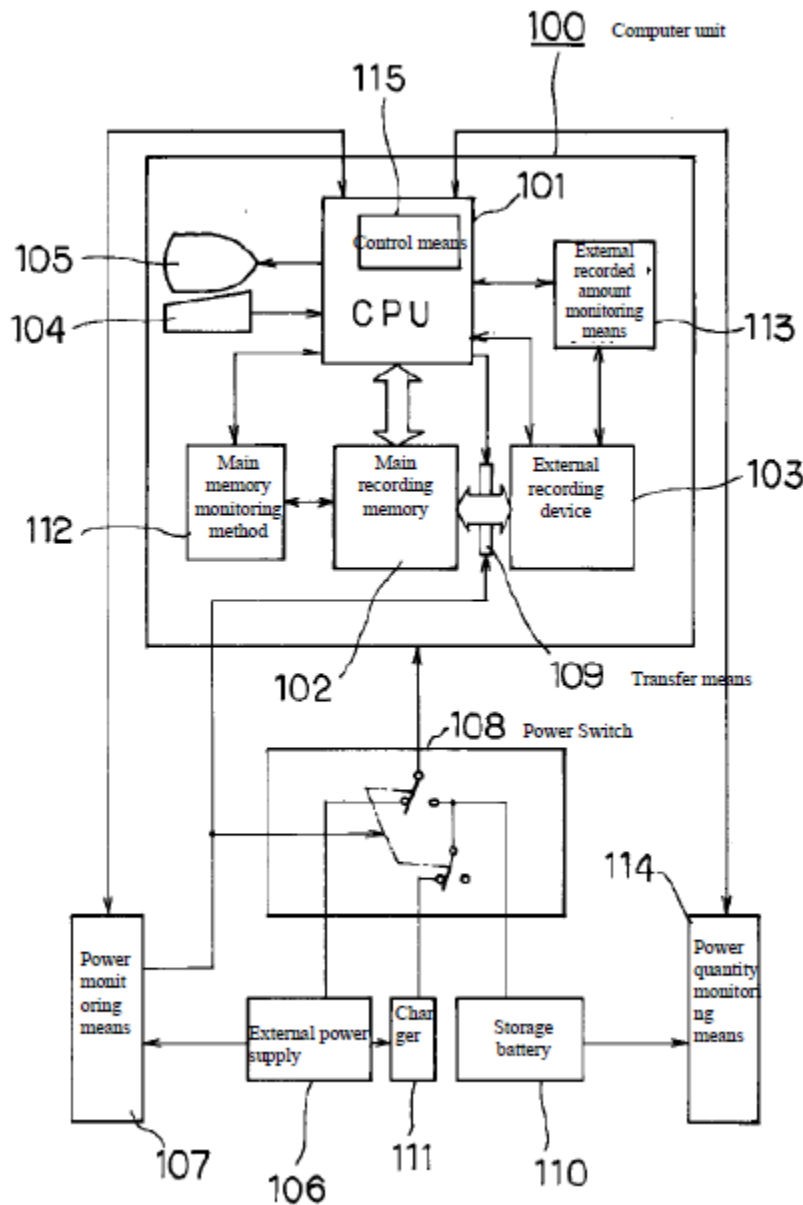
E. Obviousness Based on Nishida, Harari, Nakao (Ground 1)

Petitioner first asserts that claims 1–3 and 6 are rendered obvious by the combined teachings of Nishida, Harari, and Nakao. Pet. 15–40. Petitioner provides a detailed claim analysis, supported by declaration testimony. *Id.*; Ex. 1003 ¶¶ 113–175.

1. Claim 1

Preamble - “A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:”

Petitioner contends that “[i]f the preamble is limiting, Nishida disclosed it or rendered it obvious in combination with Harari.” Pet. 15. As for the recited “*computer system*,” Petitioner asserts that “Nishida disclosed a “computer system” that includes “computer unit 100 and a power supply part.” *Id.* (citing Ex. 1006 ¶ 3). Petitioner asserts that Nishida’s Figure 1, shown below, illustrates the recited “*computer system*.” Pet. 15–16 (citing Ex. 1006 ¶¶ 10–11).



Nishida's Figure 1, above, is a block diagram showing a configuration of a computer system with a memory backup comprising computer unit 100 with CPU 101, control means 115, main recording memory 102, external recording device 103 and transfer means 109. Ex. 1006, Fig. 1. Power switch 108 is connected to computer unit 100 and external power supply 106, power unit monitoring means 107, and storage battery 110, which is connected to power quantity monitoring means 114.

According to Petitioner, Nishida explains that the “computer system” is “generally operated by power from external power sources.” Pet. 16 (citing Ex. 1006 ¶ 2; *see also id.* ¶¶ 4, 6–7, 10–11, 13–15, claims 1–3). Nishida explains that when a computer system’s power supply “is interrupted due to a power outage, data stored in the main memory in the computer system will disappear,” and in order to avoid data loss and “back up . . . the main memory,” Nishida teaches detecting a power outage as an “abnormality” or “deviat[ion] from a predetermined range.” Pet. 16 (citing Ex. 1006 ¶¶ 2, 3; *see also id.* ¶¶ 4, 7, 15). Petitioner points out that Nishida has power supply monitoring means 107 that “constantly monitors the supply voltage of the external power supply 106.” Pet. 16–17 (citing Ex. 1006 ¶ 3).

Petitioner asserts that in Nishida, a power outage triggers “*a method for controlling data*,” because “when an outage is detected, ‘the data on the main memory is urgently transferred to a non-volatile external recording device using the power supply for the backup to protect data.’” Pet. 17 (citing Ex. 1006 ¶ 2; *see also id.* ¶¶ 3, 4, 15; Ex. 1003 ¶ 115). According to Petitioner, “[b]ecause main recording memory [102] is ‘volatile,’ data transfer to non-volatile external recording device [103] ‘protect[s]’ the data from ‘disappear[ing]’ in the event of a power loss.” Pet. 17 (citing Ex. 1006 ¶¶ 2, 3; Ex. 1003 ¶ 115).

Petitioner asserts that Nishida also teaches the recited “*computing engine*,” because “Nishida’s computer system includes computer unit 100,” which performs “*computing*,” such as “comput[ing] the amount of backup memory possible” and “calculate[ing] [a] maximum amount of data . . . that can be transferred.” Pet. 17 (citing Ex. 1006 ¶¶ 3, 11, 14; *see also id.* ¶¶ 8,

11, 16). Petitioner argues that “[a]lternatively, computer unit 100’s ‘CPU (central processing unit) 101,’ ‘volatile main recording memory 102,’ and ‘nonvolatile external recording device 103’ constitute a “*computing engine*.” Pet. 17 (citing Ex. 1006 ¶ 3).

Petitioner argues that “it would have been obvious to use EEPROM [electrically erasable programmable read only memories] as Nishida’s nonvolatile recording device 103,” because Harari teaches that “EEPROM provides nonvolatility ‘without sacrificing ease of erasing and rewriting data into the memory, speed of access, low cost and reliability,’ as well as ‘requiring less power to operate’ and ‘being lighter in weight than a hard disk drive magnetic memory,’” and that “[u]sing EEPROM as recording device 103 would have provided these benefits to Nishida’s system.” Pet. 19 (citing Ex. 1024, 3:48–58).

Patent Owner does not provide any arguments directed specifically to whether the asserted art meets the preamble (*see generally* Prelim. Resp.), but does provide argument contesting Petitioner’s rationale to combine the asserted art, which we consider in Section III.E.1.d.

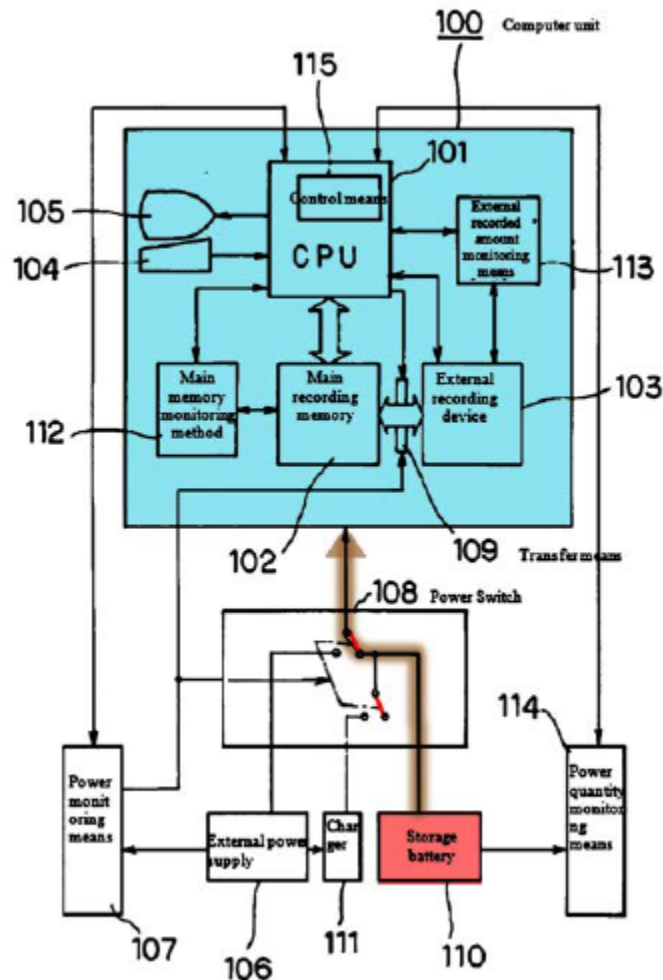
Based on this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that the asserted prior art meets the subject matter recited in the preamble of claim 1.

a) [1a] activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;

Petitioner contends that “Nishida disclosed a ‘*plurality of supercapacitors*’ that supply backup power ‘*upon power being removed from the computer system*.’” Pet. 20. Petitioner points out that “Nishida disclosed ‘a backup power supply consisting of storage batteries,

supercapacitors, lithium primary batteries, etc.’ to use upon a ‘power outage’ in the ‘computer system.’” *Id.* (citing Ex. 1006 ¶ 2). Petitioner asserts that “[a]ny of the listed structures can serve as the ‘backup power supply.’” Pet. 20 (citing Ex. 1003 ¶¶ 124–125). Petitioner relies on disclosed backup power supply 110 consisting of super-capacitors. Pet. 20.

Petitioner asserts that Nishida also disclosed “*activating [the] super capacitors to supply power to the computing engine.*” *Id.* Petitioner provides annotated Figure 1 from Nishida, shown below.



Petitioner’s annotated Figure 1 from Nishida is shown above. Petitioner explains that in Nishida, “[u]pon a power outage, switch 108

‘switches the supply of power to computer unit 100’ to super-capacitors 110 (red in annotated Figure 1 [above]) by changing to the backup power supply (right) side (indicated with red lines).” Pet. 20–21 (citing Ex. 1006 ¶ 3; *see also id.* ¶¶ 4, 15). Petitioner explains, “[t]hat electrically connects super-capacitors 110 with computer unit 100 (blue), ‘*activating*’ the super-capacitors so the ‘computer system is operated by power from’ super-capacitors 110 provided along the brown path.” Pet. 21 (citing Ex. 1006 ¶ 4; *see also id.* ¶¶ 3, 15). Petitioner asserts that “[i]n providing power to computer unit 100, the super-capacitors also supply power to CPU 101, memory 102, and recording device 103, all of which continue to function despite the power outage.” Pet. 21 (citing Ex. 1006 ¶¶ 4, 15; Ex. 1003 ¶¶ 126–127).

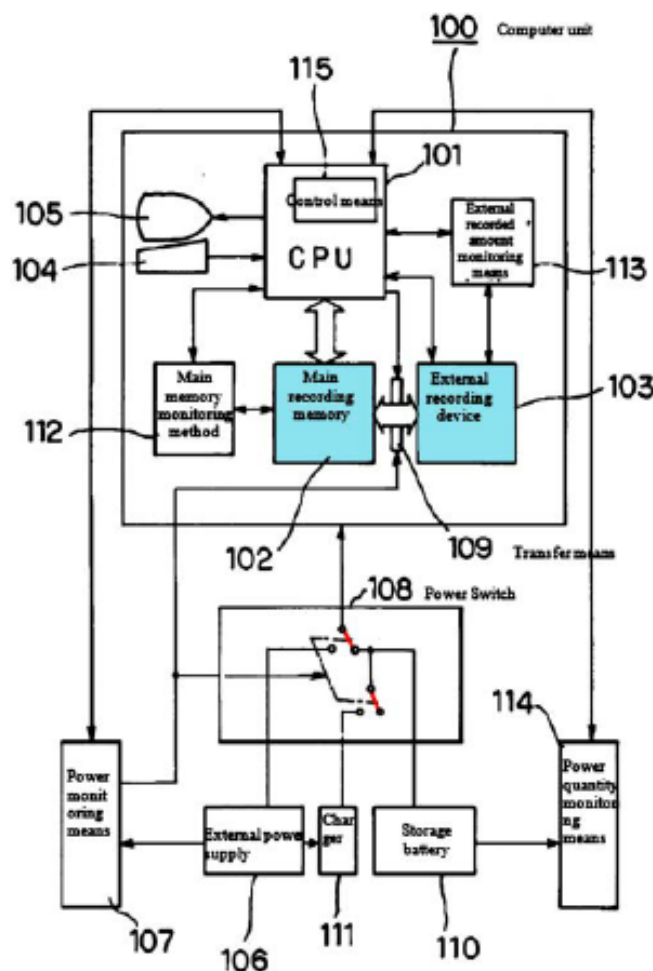
Patent Owner does not provide any arguments directed specifically to this limitation (*see generally* Prelim. Resp.), but does provide argument contesting Petitioner’s rationale to combine the asserted art, which we consider in Section III.E.1.d.

Based on this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that the asserted prior art meets the recited limitation “*activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system*” of claim 1.

b) [1b] *reconfiguring the data in the computing engine;*

Petitioner contends that its proffered Nishida/Harari system renders this limitation obvious. Petitioner explains that in this system, “[a]fter a power outage, ‘data on the main recording memory 102 is completely evacuated to the external recording device 103,’” and that this process “is

described as a ‘transfer.’” Pet. 22 (citing Ex. 1006 ¶¶ 3, 15; *see also id.*, ¶¶ 2, 4, 7–9, 14–15). Petitioner asserts that “[m]emory 102 is ‘volatile,’ and recording device 103 is ‘nonvolatile.’” Pet. 22 (citing Ex. 1006 ¶¶ 2–3, 7). Petitioner argues that “recording device 103 is (or would have been) a memory, and both memory 102 and recording device 103 are part of a ‘*computing engine.*’” Pet. 22. Petitioner provides annotated Figure 1 from Nishida, below.



Petitioner’s annotated Figure 1 of Nishida, shown above, shows memory 102 and recording device 103 (in blue) and a double-headed arrow between them that indicates data transfer. Pet. 22 (citing Ex. 1003 ¶¶ 128–129).

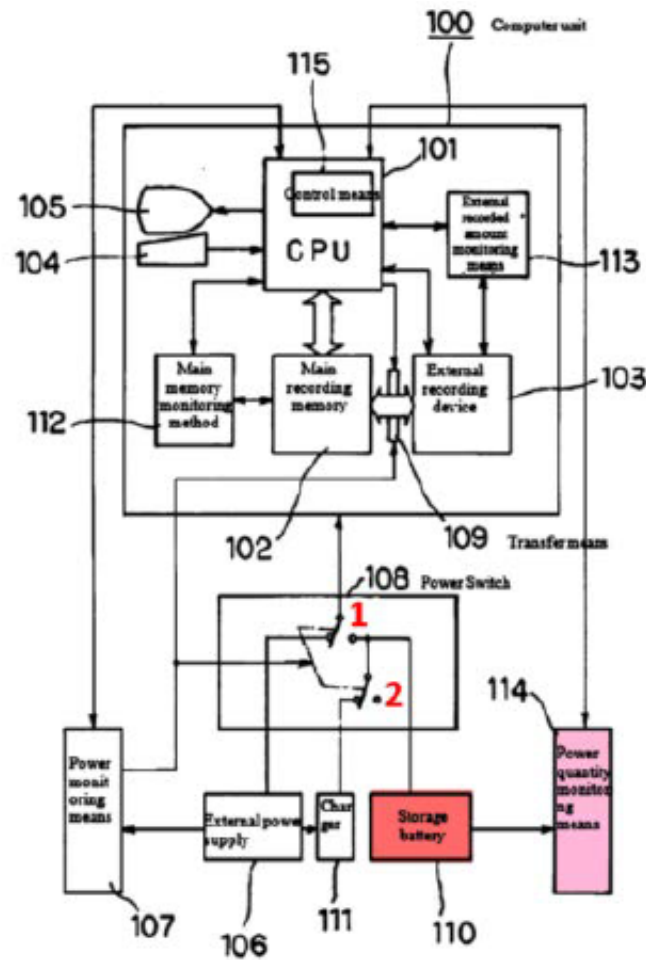
Patent Owner does not provide any arguments directed specifically to this limitation (*see generally* Prelim. Resp.), but does provide argument contesting Petitioner’s rationale to combine the asserted art, which we consider in Section III.E.1.d.

Based on this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that the asserted prior art meets the recited limitation “*reconfiguring the data in the computing engine*” of claim 1.

c) [1c] deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

Petitioner contends that the Nishida/Harari system in combination with Nakao renders this limitation obvious. Pet. 23. In addition to Nishida disclosing a “*plurality of super capacitors*” that provides power to a “*computing engine*,” Petitioner asserts that “Nishida further taught monitoring the power level of the super-capacitors and using a switch to ‘*deactivat[e]*’ them.” *Id.*

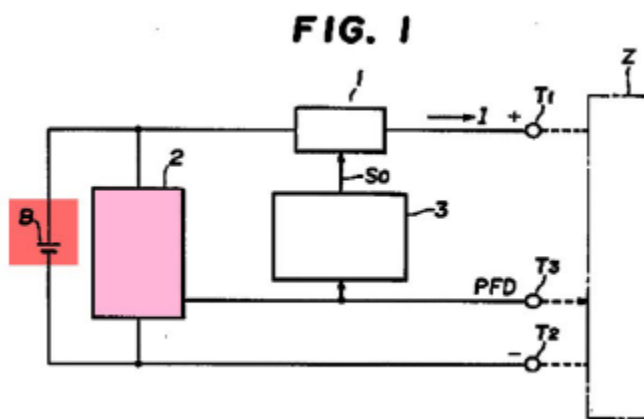
Petitioner provides an annotated version of Nishida’s Figure 1, shown below. *Id.*



According to Petitioner, “Nishida recognized that backup super-capacitors 110 (red in annotated Figure 1 [above]) have ‘a limited amount of charge.’” Pet. 23 (citing Ex. 1006 ¶ 4; *see also id.* ¶ 2). Petitioner explains that “[p]ower amount monitoring means 114 (pink) ‘monitors the current charge amount’ of super-capacitors 110,” and “[s]witch 108 ‘switches the supply of power to the computer unit 100 between the external power supply 106’ and super-capacitors 110.” Pet. 23–24 (citing Ex. 1006 ¶ 3; *see also id.* ¶¶ 4, 15). Annotated Figure 1, above, shows switch 108 configured to the external power supply (left) side. Pet. 24 (citing Ex. 1006 ¶ 13). Petitioner explains that “[i]n that configuration, super-capacitors 110 are disconnected

from and not supplying power to computer unit 100.” Pet. 24 (citing Ex. 1003 ¶¶ 131–132).

Petitioner asserts that “Nakao taught a device for ‘preventing over-discharge’ in power storage elements.” Pet. 24 (citing Ex. 1007, 1:5–8). According to Petitioner, “Nakao described several implementations that detect when large-scale capacitors reach a specific voltage and provide signals that configure a switch to stop the capacitors from supplying power.” Pet. 24. Petitioner provides annotated Figure 1 from Nakao, shown below.



As illustrated in Nakao’s annotated Figure 1, above, one embodiment includes battery B (red), switching portion 1, voltage detector 2 (pink), and controller 3. Pet. 24 (citing Ex. 1007, 3:6–14). Nakao explains that “large-scaled capacitors can form the electric storage elements (B),” and when the voltage of storage elements B “becomes lower” than V_L , detector 2 “output[s] a discharge finishing signal PFD.” Pet. 24 (citing Ex. 1007, 2:40–42, 3:33–35). “In response,” Petitioner explains, “external circuits Z ‘begin stopping . . . operation,’ [d]ischarge controller 3 delays before sending ‘signal S0’ to ‘make the switching portion 1 . . . change to an OFF state,’ [and] [t]he power supply to external circuits Z ‘is stopped.’” Pet. 25 (citing Ex. 1007, 3:35–63).

Petitioner describes similar implementations in Nakao with respect to Nakao’s Figures 2 and 5. *See* Pet. 25–26. Petitioner provides the chart below identifying Nakao’s disclosures in these three implementations with respect to a detected voltage and a signal to stop power. Pet. 26.

Implementation	Detect voltage	Signal to stop power
Figure 1	3:33-35	3:33-47
Figure 2	4:47-52	4:47-63
Figure 5	1:29-32	1:29-32, 1:38-46

Petitioner explains that

In each case, turning off switching portion 1 disconnects power storage elements from external circuits Z to “stop[]” or “cut off” (“*cut off*”) power to those circuits. (Ex. 1007, 1:29-32, 1:38-46, 1:55-62, 3:41-47, 4:55-63, 5:47-53; *see also id.*, claim 2 (“power **cut-off** signal RST”).) Nakao therefore disclosed “*deactivating*,” which Intel identifies as “electrically disconnect[ing]” power storage elements so they are “not discharging current to a load” (the district court’s interpretation). (Ex. 1018, 19; *see also* Ex. 1019, 3.) In Nakao, setting switching portion 1 to “OFF” breaks the electrical connection between the power storage elements and the external circuits, preventing the elements from discharging current to the external circuits (the load). (Ex. 1007, 4:25-29; Ex. 1003 ¶¶ 140-142.)

Pet. 26–27.

Petitioner argues that “[d]eactivating” happens “*based on*” the storage elements discharging to a discharge extinction or finishing voltage VL—which is a “*predetermined level*.” Pet. 27 (citing Ex. 1007, Abstract, 1:29–32, 3:31–47, 4:4–8, 4:45–52; Ex. 1003 ¶ 143). Petitioner explains that “VL is ‘a limited voltage’ (Ex. 1007, 3:17–26) and ‘can be set to a usage

limitation value’ (*id.* at 4:4–8), including based on reference voltages (*id.*, 5:10–19).” Pet. 27. Petitioner argues that “Nakao disclose[s] the limitation because VL is a pre-set voltage limit.” Pet. 27 (citing Ex. 1003 ¶¶ 143–146).

Patent Owner does not provide any arguments directed specifically to this limitation (*see generally* Prelim. Resp.), but does provide argument contesting Petitioner’s rationale to combine the asserted art, which we consider in Section III.E.1.d.

Based on this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that the asserted prior art meets the recited limitation “*deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level*” of claim 1.

d) Rationale to Combine

For purposes of a rationale to combine the asserted art, the Petition relies on Dr. Sechen’s testimony that a person of ordinary skill in the art “would have been motivated to use EEPROM as an implementation of the non-volatile external recording device 103 disclosed in Nishida,” because “Nishida does not provide details about the composition of nonvolatile external recording device 103.” Pet. 19 (quoting Ex. 1003 ¶ 120). Dr. Sechen testifies that a person of ordinary skill in the art “desiring a non-volatile memory device would have investigated . . . available options at the time to discover Harari, which described ‘[a] system of Flash EEprom memory chips with controlling circuits serv[ing] as non-volatile memory.’” Ex. 1003 ¶ 120 (citing Ex. 1024, Abstract).

Dr. Sechen also testifies that a person of ordinary skill in the art “would have had a reasonable expectation of success because Harari’s

EEPROM would have been used for its intended purpose of non-volatile data storage, which would have stored data even when the power supply is not available,” as “Harari disclosed that EEPROMs are ‘nonvolatile, and retain their memory even after power is shut down,’ which is the “same functionality required by Nishida’s external recording device 103.” Ex. 1003 ¶ 121 (citing Ex. 1024, 1:35–36).

Dr. Sechen further testifies that

Harari taught that using EEPROM as a non-volatile memory storage device provided many advantages to a computer system. For example, EEPROM provides non-volatility “without sacrificing ease of erasing and rewriting data into the memory, speed of access, low cost and reliability” and “requir[es] less power to operate” and “[is] lighter in weight than a hard disk drive magnetic memory.”

Ex. 1003 ¶ 122 (citing Ex. 1024, 3:48–58). Dr. Sechen testifies that “[u]sing EEPROM as recording device 103 would have provided these advantages to Nishida’s computer system.” Ex. 1003 ¶ 122.

According to Dr. Sechen, Nakao teaches that “[w]hen the battery voltage falls below a discharge extinction voltage, the voltage detector 2 is driven to switch OFF the switching portion 1 to thereby stop the electric supply to electronic apparatuses and instruments.” Ex. 1003 ¶ 147 (citing Ex. 1007, 1:29–32). “Tracking Nakao’s teachings,” Dr. Sechen testifies, “when power quantity monitoring means 114 of Nishida detected a discharge finishing voltage, it would have configured power switching switch 108 to the external power supply side on the left to electrically disconnecting super-capacitors 110 from computer unit 100.” Ex. 1003 ¶ 147.

Dr. Sechen testifies that a person of ordinary skill in the art would have been motivated to pursue this combination because “Nakao explicitly taught the advantages of preventing over-discharge in power storage elements,” and “Nakao described ‘preventing over-discharge in various kinds of accumulator elements such as a secondary battery, primary battery and large-scale capacitors, etc.’” *Id.* ¶ 148 (citing Ex. 1007, 1:5–13). According to Dr. Sechen, “[t]he resulting combination would have prevented over-discharge for Nishida’s super-capacitors 110 that supply power during a power outage.” Ex. 1003 ¶ 149.

Dr. Sechen also testifies that a person of ordinary skill in the art “would have incorporated the over-discharge prevention approach of any one of Nakao’s two embodiments or conventional prior art example into Nishida’s system or the combined system of Nishida and Harari because Nishida did not teach how to safely shut down its computer system as backup power continues to discharge toward exhaustion.” *Id.* ¶ 150. According to Dr. Sechen, a person of ordinary skill in the art “would have recognized that both batteries and capacitors have a finite amount of stored energy, and that the stored energy would eventually be depleted if the external power supply is not reestablished,” and “Nishida acknowledged this fact, noting that ‘there is limited amount of charge’ in supercapacitors 110.” *Id.* (citing Ex. 1006 ¶ 4).

Dr. Sechen testifies that “combining Nakao with Nishida’s system or the combined system of Nishida and Harari would have applied a known technique to improve a similar system in the same way as described in Nakao,” and the combination “would have improved data safety and reliability in Nishida’s system or the combined system of Nishida and

Harari.” Ex. 1003 ¶¶ 152, 154. According to Dr. Sechen, “the combination of Nakao with Nishida’s system or the combined system of Nishida and Harari would have applied a known technique to resolve a known problem recognized in Nishida.” *Id.* ¶ 156.

Patent Owner argues that “[c]onsidering the disclosures of these references in full, a [person of ordinary skill in the art] would not have been motivated to combine these references in the manner claimed.” Prelim. Resp. 13. Patent Owner argues that “Nishida’s ‘object’ is providing ‘a computer system that can know in advance whether a backup can be performed completely.’” *Id.* “On the other hand, Nakao expressly discloses that its mechanism serves as an *alternative* to ‘power source detection mechanisms,’ which were used to assume the ‘remaining battery remanent voltage . . . to judge in advance the state of the batter consumption.’” *Id.* at 14 (citing Ex. 1007, 1:39–46, 6:15–18). Patent Owner argues that “Nakao intentionally developed an *alternative* to the advanced computation of reserve battery power, such as disclosed in Nishida.” Prelim. Resp. 14.

“Given that even Nakao itself sought an alternative approach to Nishida’s advanced computation,” Patent Owner argues that a person of ordinary skill in the art “faced with the disclosures of Nishida and Nakao would not have been motivated to combine these references’ teachings in the manner claimed.” *Id.* at 15. Patent Owner argues that a person of ordinary skill in the art “would have had no reason to include Nishida’s power quantity monitoring means 114 to monitor the storage battery 110 into a system that uses Nakao’s mechanism for avoiding over-discharge.” *Id.* at 16. Patent Owner argues that “[t]hese references disclose different,

alternative solutions, and a [person of ordinary skill in the art] would not have been motivated to combine these solutions.” *Id.* at 17.

We disagree with Patent Owner. Petitioner provides a well-reasoned showing of various rationales for combining the teachings of Nishida, Harari, and Nakao. Petitioner’s arguments are supported by the unrebutted testimony of Dr. Sechen. *See* Ex. 1003 ¶¶ 120–123, 147–163. In contrast, Patent Owner provides only unsupported attorney argument to challenge Petitioner’s showing. *See* Prelim. Resp. 13–18. At this stage of the proceeding, Dr. Sechen’s testimony is unrebutted and the evidence is one-sided in favor of Petitioner on the issue of rationale to combine.

Based upon the current record, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that a person of ordinary skill in the art at the time of the invention would have had a reasoned basis for combining the teachings of Nishida, Harari, and Nakao in the manner proffered and would have had a reasonable expectation of success in that endeavor.

e) Conclusion as to Claim 1

We have considered the evidence and arguments with respect to independent claim 1. Based upon this preliminary record, we are persuaded that Petitioner has shown sufficiently for purposes of institution that the combined teachings of the cited art meet the limitations of independent claim 1, and that a person of ordinary skill in the art at the time of the invention would have combined the references in the manner proffered and would have had a reasonable expectation of success in that endeavor.

2. *Claims 2, 3 and 6*

These claims depend, directly or indirectly, from claim 1. Petitioner provides a claim-by-claim analysis for each of these claims in relation to Nishida, Harari, and Nakao, which is supported by the testimony of Dr. Sechen. *See* Pet. 35–40; Ex. 1003 ¶¶ 164–175.

Patent Owner does not provide any arguments directed specifically to these dependent claims (*see generally* Prelim. Resp.), but does provide argument contesting Petitioner’s rationale to combine the asserted art, which we consider in Section III.E.1.d.

We have considered the evidence and arguments with respect to dependent claims 2, 3, and 6. Based upon this preliminary record, we are persuaded that Petitioner has shown sufficiently for purposes of institution that the combined teachings of the cited art meet the recited limitations of these claims, and that a person of ordinary skill in the art at the time of the invention would have combined the references in the manner proffered and would have had a reasonable expectation of success in that endeavor.

F. Grounds 2–6

Petitioner also contends that claims 1–3, 6, 10–12, and 15 are unpatentable under 35 U.S.C. § 103 as obvious over the combined teachings of Nishida, Harari, Ergott, and Pilukaitis (Ground 2, Pet. 40–72); claims 10–12, and 15 over Nishida, Harari, Ergott, Pilukaitis, and Nakamura (Ground 3, Pet. 72–83); claims 1–3, and 6 over Nishida, Harari, Nakao, and Supercap (Ground 4, Pet. 83–86); claims 1–3, 6, 10–12, and 15 over Nishida, Harari, Ergott, Pilukaitis, and Supercap (Ground 5, Pet. 83–86); and claims 10–12, and 15 over Nishida, Harari, Ergott, Pilukaitis, Nakamura, and Supercap (Ground 6, Pet. 83–86). Petitioner provides evidence and arguments as to

how the art teaches or suggests each claim limitation. *See* Pet. 40–86.

Dr. Sechen provides supporting testimony for Petitioner’s contentions. *See* Ex. 1003, 54–198.

Patent Owner disputes some of Petitioner’s contentions and provides evidence and arguments as to how Petitioner has failed to demonstrate that the challenged claims are obvious over the asserted art, principally for failing to establish that a person of ordinary skill in the art would not have been motivated to combine the asserted prior art in the manner proposed by Petitioner. *See* Prelim. Resp. 10–20. Patent Owner also argues that Petitioner has failed to establish that the Supercap reference qualifies as printed publication prior art. *See* Prelim. Resp. 21–24. We address the Supercap prior art issue in Section III.D.7.a.

We have considered the parties evidence and arguments with respect to these grounds. However, because we determine that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge to independent claim 1 under 35 U.S.C. § 103(a) as obvious over the combined teachings of Nishida, Harari, and Nakao (*see* Section III.E) and we are instituting an *inter partes* review on that challenge, we must institute *inter partes* review as to all challenges in the Petition, including Petitioner’s challenges with respect to Grounds 2–6. *See PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018).

IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

V. ORDER

Upon consideration of the record before us, it is
ORDERED that *inter partes* review of claims 1–3, 6, 10–12, and 15
of the '939 patent is instituted on all grounds in the Petition; and
FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and
37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial
will commence on the entry date of this decision.

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