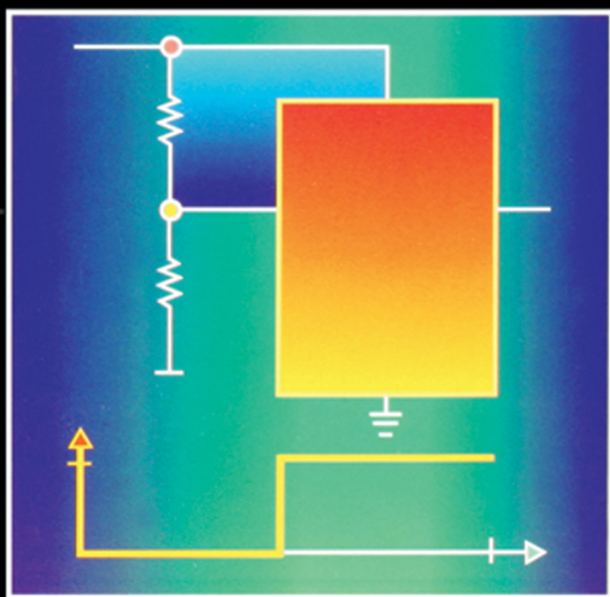


JOHN D. LENK

SIMPLIFIED DESIGN OF MICROPROCESSOR- SUPERVISORY CIRCUITS



EDN® SERIES FOR DESIGN ENGINEERS

Simplified Design of Microprocessor- Supervisory Circuits

John D. Lenk

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Greetings from the Villa Buttercup!

To my wonderful wife, Irene: Thank you for being by my side all these years!

To my lovely family: Karen, Tom, Brandon, Justin, and Michael.

And to our Lambie and Suzzie: Be happy wherever you are!

*And to my special readers: May good fortune find your doorway,
bringing good health and happy things. Thank you for buying my books!*

To Karen Speerstra, Jo Gilmore, Duncan Enright, Pam Boiros, Joan Dargan, Philip Shaw, Elizabeth McCarthy, Vickie Edwards, Pam Chester, the Newnes people, the UK people, and the EDN people: A special thanks for making me an international best seller, again (this is book 90).

Abundance!

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Preface

This book has something for everyone involved in electronics. No matter what your skill level, this book shows you how to design and experiment with microprocessor-supervisory circuits and interfaces.

For experimenters, students, and serious hobbyists, the book provides sufficient information to design and build microprocessor-supervisory circuits from scratch. The design approach is the one used in all my best-selling books on simplified and practical design.

If you are a working engineer responsible for designing microprocessor-supervisory circuits or selecting supervisory integrated circuits, the variety of circuit configurations described herein should generally simplify your task. The book describes supervisory circuit designs and covers the most popular forms of supervisory integrated circuits available. Throughout the book, you will find a wealth of information on supervisory integrated circuits and related components.

In this book, design problems start with circuits that can be put to immediate use as is and include guidelines for selecting components. By using the guideline values in experimental circuits, you can produce the desired results (such as microprocessor reset, memory protection, power-fail warning, battery backup, and watchdog) by varying the experimental component values, if necessary.

Chapter 1 is devoted to primary microprocessor-supervisory functions. Such functions are vital to all microprocessor-based systems because the functions include safeguards against system failure.

Chapter 2 discusses simplified design with supervisory integrated circuits used in 5-V digital systems.

Chapter 3 is devoted to simplified design with supervisory integrated circuits used in 3-V and 3.3-V digital systems.

Chapter 4 covers simplified design with supervisory integrated circuits that have on-board chip-enable functions.

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Chapter 5 is devoted to simplified design with low-cost supervisory integrated circuits that have a battery-backup function.

Chapter 6 discusses simplified design with low-cost supervisory integrated circuits that have a watchdog function.

Chapter 7 covers simplified design with low-cost supervisory integrated circuits that provide for voltage monitoring in the 3-V range.

Chapter 8 is devoted to simplified design with complete supervisory integrated circuits that provide all the functions discussed in Chapter 1.

Chapter 9 discusses simplified design with supervisory integrated circuits that provide most functions for both power-supply and watchdog monitoring in systems without battery backup as well as memory-write protection.

Finally, Chapter 10 is devoted to simplified design approaches for a cross section of microprocessor and microcontroller supervisory integrated circuits as well as a few discrete-component supervisory circuits. The circuits described can be put to immediate use. In many cases, you can alter the operating range and characteristics by changing component values or by making minor changes in circuit connections. The chapter ends with simplified design approaches for microprocessor interface circuits.

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And to Irene, my wife and super agent, I extend my thanks. Without her help, this book could not have been written.

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CHAPTER 1

The Microprocessor-Supervisory Functions

The primary microprocessor-supervisory functions are concerned with housekeeping required by microprocessors and digital systems. Such functions are vital to all microprocessor-based systems because the functions include safeguards against system failure. Some microprocessors provide the supervisory functions, but such microprocessors cannot always diagnose their own failures. To be most effective and reliable, the system and microprocessor must be monitored with external circuits.

It is possible to design supervisory circuits from scratch. However, all the basic functions are available in IC form, and it is generally easier and simpler to use such ICs. Considerable design effort and development time can be saved with ICs that contain both analog and digital supervisory functions. That is why we concentrate on such ICs in this simplified-design book.

The data sheets for supervisory ICs often show the connections required to convert the IC to a complete supervisory system. We describe many such examples throughout the book. In this chapter, we concentrate on the basic functions to help you understand the data-sheet information. In the remaining chapters, I describe internal operation of the ICs themselves and show how ICs are used.

It is assumed that you are already familiar with digital and microprocessor basics (such as number systems, logic elements, gates, microprocessors, and digital test equipment). If not, read *Lenk's Digital Handbook*, McGraw-Hill, 1992.

The most common microprocessor-supervisory functions include power-on-reset, low-voltage reset for glitch and brownout, memory-write protection, power-fail warning, battery backup switchover, and watchdog timer. These functions are not difficult to implement individually but can be a problem when they all must be included, especially if space is critical. The following review of these supervisory functions shows their relation to the overall microprocessor system.

1.1 Power-On Reset

When power is applied to a microprocessor, the internal registers “come up” in arbitrary states that contain random data. Applying a reset command to the microprocessor overcomes this chaos by resetting all internal circuits at a predictable starting point. To ensure proper startup, the RESET input must be held low for a typical 20 to 120 ms. Although simple, the external reset-timer circuit must keep the RESET signal low while the supply voltage (V_{CC}) is below the minimum level allowed for microprocessor operation.

For example, during startup the circuit initiates a reset-delay interval only when V_{CC} reaches that minimum level. If the timed interval begins early (at too low a voltage) or ends too soon, the reset might be overridden by arbitrary states in the digital circuitry while the supply voltage is rising toward the minimum operating level. Power-on reset-timer circuits therefore require a timer, a comparator, an accurate voltage reference, and a suitable means for driving the microprocessor RESET input.

1.2 Low-Voltage (Glitch/Brownout) Reset

Once operating, a microprocessor should continue as long as V_{CC} remains within the specified limits. To ensure reliable operation, the supervisory IC must monitor V_{CC} for low voltage or undervoltage (both short-term glitches and long-term brownout). These undervoltage conditions are seldom destructive, but they can cause unpredictable operation that leads to a system crash. During a crash, the system or computer loses its mind in a manner that no programming genius can cure. The microprocessor cannot be trusted to control its own reset, so the most reliable remedy is to reset the microprocessor with a signal that originates automatically in an external device.

The low-voltage and power-on sections of a typical supervisory IC share the same precision voltage-sensing circuit, and both respond when V_{CC} goes low. When V_{CC} returns to normal, the RESET output to the microprocessor remains low for a timed-delay interval, as is the case when power is first applied (during initial power on; see Section 1.1).

1.3 Memory-Write Protection

A typical system crash can lead to a potentially worse problem. During the crash, the microprocessor might write “garbage” into the permanent (nonvolatile) memory, causing data and program losses that cannot be restored with a simple reset. To prevent such losses, the system must intercept and disable the memory chip-enable (CE) signal during a supply-voltage glitch or brownout. This can be done by means of applying the CE signal and the output of a low-voltage comparator to a gate

and using the gate output to drive the memory CE input. However, the gate must operate reliably with a V_{CC} as low as 2 V (for a typical 5-V digital system).

1.4 Power-Fail Warning

Full protection for a digital system might require more than a simple low-voltage detection and reset. It might be necessary to provide other actions before reset. For example, the microprocessor might need to store the register contents in a non-volatile memory (such as a battery-backed CMOS RAM).

Power-fail warning circuits take advantage of the fact that power-supply regulators have large input-filter capacitors. In a typical 5-V supply, these capacitors charge to between 8 V and 10 V. This charge enables the regulator to continue operating for 50 to 100 ms after the primary power is lost (until the capacitor discharges to about 6.5 V, or less for low-dropout regulators).

The supervisory IC can be connected to monitor the filter-capacitor voltage. (On Maxim ICs, the power is monitored at a power-fail-in [PFI] input.) When the unregulated voltage from the filter capacitor falls below a given value (typically about 7.5 V), an internal comparator issues a power-fail-out (PFO) signal. This allows sufficient time for microprocessor housecleaning before the system initiates a reset.

The PFO signal normally is connected to the nonmaskable interrupt (NMI) of the microprocessor. This ensures top-priority response. In a supervisory IC, the PFI input drives one side of an internal CMOS comparator. The other side is driven by a fixed reference (typically 1.3 V). Two external resistors, which divide the capacitor voltage down to the 1.3-V reference, allow the trip point to be set for any desired filter-capacitor voltage.

1.5 Battery-Backup Switchover

CMOS RAM normally is powered by the 5-V supply of the microprocessor. When connected to a 3-V battery in the shutdown or backup mode, the RAM retains its contents but consumes very little power. Backup batteries can be small because the memory current drain (several milliamperes in normal operation) drops to a few microamperes in the backup mode.

The circuit that switches RAM from the main supply to the battery must “stay awake” to switch the RAM back when power is restored. As in the case of a RAM, this switchover circuit depends on the battery and therefore must operate on microamperes of current. Besides low power consumption, the switchover circuit must show reliable operation at low supply voltage when the backup battery discharges. The same is true for reset and write-protect circuits, which remain active in the backup mode.

1.6 Watchdog Timer

Software is usually written as a series of modules interconnected in a continuous loop. During execution, an unforeseen sequence of events can sometimes cause the program to stall within one module, endlessly performing some useless (or possibly harmful) function. A watchdog-timer circuit monitors the program execution and issues a reset command when the stall condition appears.

To use the watchdog, connect a port of the microprocessor to the timer-reset input of the watchdog circuit (which is normally free running), and configure the software to write data to the port several times a second. Because the circuit interprets missing instructions as a software problem, the watchdog issues a system reset whenever the free-running watchdog times out before receiving the next write instruction.

The optimum timeout depends on the system hardware and software. For example, a longer period at power up gives the microprocessor extra time to initialize the system before starting the main software loop. In some systems, the watchdog is activated only for certain applications.

1.7 Monitoring Multiple Power Supplies

In some digital systems, the supervisory IC must monitor more than one power supply. Figure 1–1 shows a typical supervisory IC (the Maxim 696/697) connected to monitor V_{CC} , +12 V and +15 V. The PFI monitors the +15-V supply, and the low-line input (LLIN) monitors both V_{CC} and +12 V simultaneously. In this particular IC, both inputs have very low leakage so high-resistance voltage dividers can be used. Because little current is drawn from the supplies, the use of low-leakage ICs has the advantage for monitoring a backup battery.

1.8 Manual Reset

In addition to the automatic reset provided by most supervisory ICs, some digital systems require a manual reset. Figure 1–2 shows the Maxim MAX690-695 series connected for manual reset. This circuit provides all normal reset delays plus a man-

Figure 1–1.
Multiple line monitor.
(Maxim New Releases
Data Book, 1992,
p. 5-10)

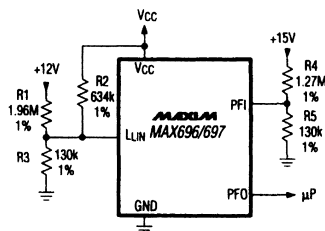
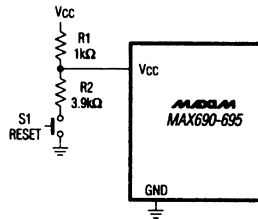


Figure 1-2.

Manual reset with de-bounced input. (Maxim New Releases Data Book, 1992, p. 5-10)

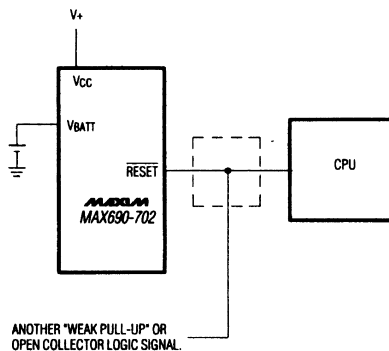


ual reset with debounced input. Various manual-reset configurations are described throughout the rest of this book.

1.9 Parallel Outputs

In some digital systems, the supervisory IC must provide outputs to the microprocessor and to other system components simultaneously, all on the same line. This can cause problems when there is a conflict on a particular line. Figure 1-3 shows ICs in the MAX690 series connected to the microprocessor (CPU) and to another open-collector logic-signal source, both on the same line. These Maxim ICs have unusual output structures that allow them to be paralleled with other logic as a wired-NOR gate or used with an external pull-up resistor to V_{OUT} .

In the circuit of Fig. 1-3, the RESET and $\overline{\text{RESET}}$ lines use what Maxim describes as a “weak pull up.” When the lines are high, the outputs source only about 1 mA (thus saving on power consumption). When the lines are low, the outputs can sink more than a milliampere to ground. As a result, if two of these outputs are connected, and one is pulled low, the other output also is pulled low. In effect, the outputs are in parallel NOR but without the use of an external gate.

**Figure 1-3.**

Paralleled NOR outputs. (Maxim New Releases Data Book, 1992, p. 5-10)

1.10 Detailed Description of Internal Circuits

The rest of this chapter is devoted to operation of internal circuits in typical microprocessor-supervisory ICs. Although it is not absolutely necessary for you to understand operation of the internal circuits for simplified design, it is usually most helpful.

Figure 1-4 is a block diagram of the MAX690/91/92/93/94/95 ICs. Figure 1-5 shows operation for the MAX696/697 ICs. These supervisory ICs are very similar in operation but are not identical. The following discussion describes both the differences and the similarities.

1.11 Battery-Switchover and V_{OUT} Circuit Operation

Figure 1-6 shows the battery-switchover circuits in block form. These circuits compare V_{CC} with the V_{BATT} input and connect V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50 mV greater than V_{BATT} as V_{CC} falls and when V_{CC} is 70 mV more than V_{BATT} when V_{CC} rises. The switchover comparator has 20 mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

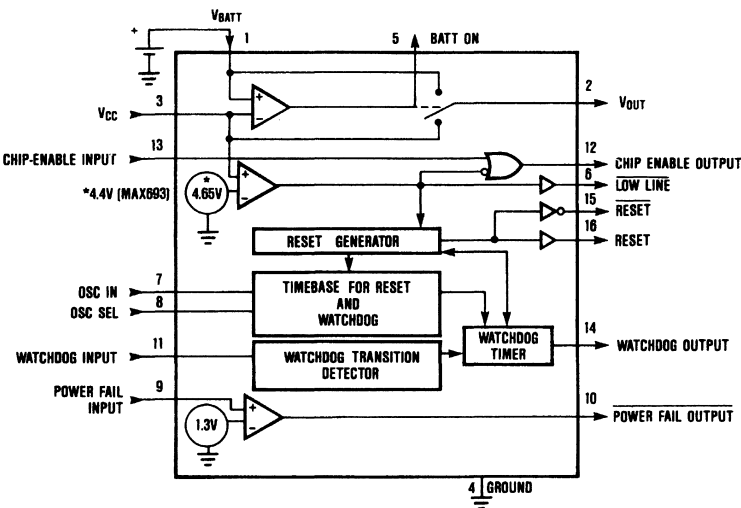


Figure 1-4. Block diagram of MAX690/91/92/93/94/95. (Maxim New Releases Data Book, 1992, p. 5-25)

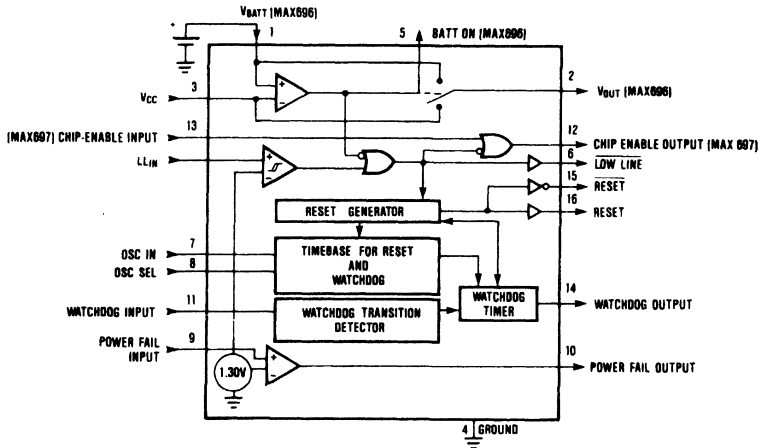


Figure 1-5. Block diagram of MAX696/97. (Maxim New Releases Data Book, 1992, p. 5-39)

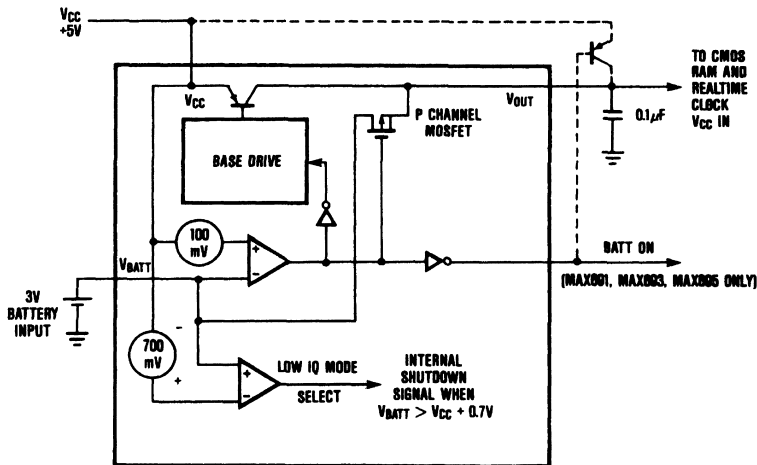


Figure 1-6. Typical battery-switchover circuits. (Maxim New Releases Data Book, 1992, p. 5-26)

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When V_{CC} is higher than V_{BATT} , V_{CC} is internally switched to V_{OUT} through a low-saturation PMOS. V_{OUT} has 50-mA output current capability. If the output current requirement at V_{OUT} exceeds 50 mA, use an external PNP pass transistor in parallel with the internal PMOS transistor, as shown by the dotted lines in Fig. 1–6. This same connection can be made if a lower V_{CC} - V_{OUT} voltage differential is required. The BATT ON output (MAX691/93/96 only) can drive the base of the external transistor directly.

These supervisory ICs need only supply the average current drawn by the CMOS RAM (if there is adequate filtering). Many RAM data sheets specify a 70-mA maximum supply current, but this peak-current spike lasts only 100 ns. A 0.1- μ F bypass capacitor at V_{OUT} supplies the high instantaneous current. As a result, V_{OUT} need only supply the average load current, which is typically much less. A capacitance of 0.1 μ F or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200-ohm MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has a very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low-power CMOS circuits. When V_{CC} equals V_{BATT} , the supply current is typically 12 μ A. When V_{CC} is between 0 V and ($V_{BATT} - 700$ mV), the typical supply current is 600 nA typical and 1 μ A maximum.

The MAX690/91/94/95 circuits operate with battery voltages from 2.0 V to 4.25 V. The MAX692/93 circuits operate with battery voltages from 2.0 V to 4.0 V. High-value capacitors, either standard electrolytic or farad-size double-layer capacitors, can be used for short-term memory backup. The charging resistor for both capacitors and rechargeable batteries should be connected V_{OUT} to eliminate the discharge path that exists if the resistor was connected to V_{CC} .

A small charging current of about 10 nA (0.1 μ A maximum) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} , but the charging-current polarity is such that the backup battery is always slightly charged (and never discharged when V_{CC} is in the operating-voltage range). This configuration extends the shelf life of the backup battery by compensating for the self-discharge current. The charging current poses no problem when lithium batteries are used for backup because the maximum charging current (1.0 μ A) is safe for even the smallest lithium cells. If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC} .

The battery-switchover circuit operation for the MAX696 (Fig. 1–5) is almost identical to that just described, with the following exceptions.

The MAX696 operates with battery voltages from 2.0 V to 4.25 V. The battery voltage should not be used with 0.5 V of V_{CC} , or switchover might occur. If capacitors are used in place of a backup battery, the capacitor charging voltage line should include a diode to limit the fully charged voltage to about 0.5 V less than V_{CC} . The maximum leakage current that flows from the V_{BATT} terminal is typically between 10 nA and a maximum of 20 nA.

1.12 Reset Output

Figure 1–7 shows the reset circuits in block form. Figure 1–8 shows reset timing. $\overline{\text{RESET}}$ is an active-low output that goes low whenever V_{CC} falls below 4.5 V (MAX690/91/94/95) or 4.25 V (MAX692/93). $\overline{\text{RESET}}$ remains low until V_{CC} rises above 4.75 V (MAX690/91/94/95) or 4.5 V (MAX692/93) for 50 ms (200 ms for MAX694/95).

The guaranteed minimum and maximum thresholds of the MAX690/91/94/95 circuits are 4.5 V and 4.75 V. The guaranteed thresholds for the MAX692/93 are 4.25 and 4.5 V. The MAX690/91/94/95 circuits are compatible with 5-V supplies with a +10%, –5% tolerance. The MAX692/93 are compatible with 5-V $\pm 10\%$ supplies. The reset threshold comparator has about 50 mV of hysteresis, with a nominal threshold of 4.65 V in the MAX690/91/94/95 circuit and 4.4 V in the MAX692/93 circuit.

The response time of the reset voltage comparator is about 100 μs . V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{\text{RESET}}$ output.

Reset also goes low if the watchdog timer is enabled and watchdog input (WDI) remains either high or low longer than the watchdog timeout period. RESET has an internal 3- μA pull up and can either connect to an open collector reset bus or drive a CMOS gate directly (without an external pull-up resistor).

The reset circuit operation for the MAX696 (Fig. 1–5) is somewhat different from that just described. For the MAX696, $\overline{\text{RESET}}$ is an active-low output that goes low whenever LL_{IN} falls below 1.3 V. $\overline{\text{RESET}}$ remains low until LL_{IN} rises above 1.312 V for 50 ms.

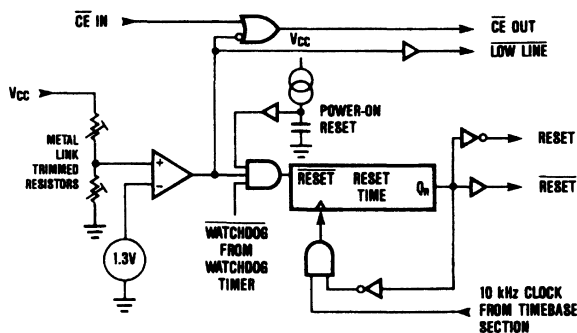


Figure 1–7. Typical reset circuits. (Maxim New Releases Data Book, 1992, p. 5-27)

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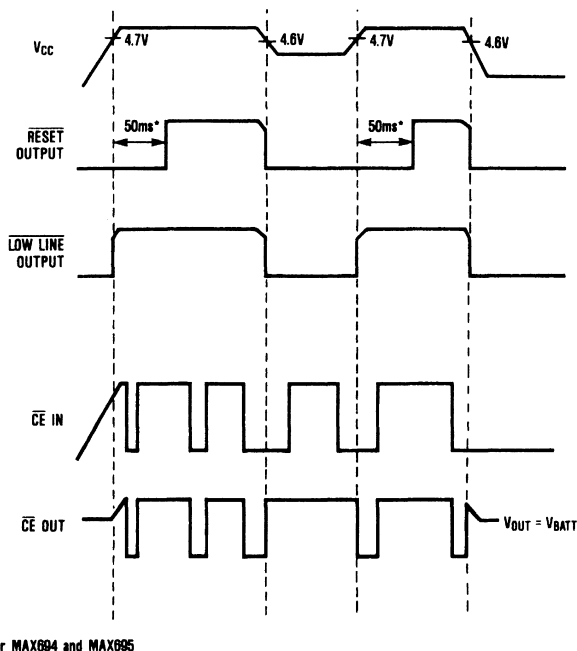


Figure 1-8. Typical reset timing. (Maxim New Releases Data Book, 1992, p. 5-27)

The guaranteed minimum and maximum low-line thresholds of the MAX696/697 circuit are 1.2 and 1.4 V. The LL_{IN} comparator has about 12 mV of hysteresis.

The response time of the reset voltage comparator is about 100 μ s. LL_{IN} should be bypassed to ensure that glitches do not activate the reset outputs.

1.13 Chip-Enable Gating and RAM Write Protection

The MAX691/93/95 circuits use two pins to control the chip-enable (CE) or write inputs of CMOS RAMs. When V_{CC} is +5 V, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN, with a 50-ns propagation delay. If V_{CC} falls below 4.65 V (4.5 V minimum, 4.75 V maximum) an internal gate forces $\overline{CE}$ OUT high, independent of $\overline{CE}$ IN. The MAX693 $\overline{CE}$ OUT goes high wherever V_{CC} is less than 4.4 V (4.25 V minimum, 4.5 V maximum). The $\overline{CE}$ output is forced high when V_{CC} is less than V_{BATT} .

$\overline{CE}$ OUT typically drives the $\overline{CE}$, $\overline{CS}$, or $\overline{WRITE}$ input of battery-backup CMOS RAM. This ensures the integrity of the data in memory by preventing write

operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}$ OUT to drive the STORE or WRITE inputs of an EEPROM, EAROM, or NOVRAM.

If the 50-ns (typical) propagation delay of $\overline{CE}$ OUT is too long, connect $\overline{CE}$ IN to GND and use the resulting $\overline{CE}$ OUT to control a high-speed external logic gate. A second alternative is to AND the LOW $\overline{LINE}$ output with the $\overline{CE}$ or $\overline{WR}$ signal. An external logic gate and the RESET output of the MAX690/92/94 can also be used for CMOS RAM write protection.

The MAX697 (Fig. 1-5) uses two pins to control the CHIP $\overline{ENABLE}$ or $\overline{WRITE}$ inputs of CMOS RAMs. When LL_{IN} is greater than 1.3 V, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN, with a 50-ns propagation delay. If the LL_{IN} input falls below 1.3 V (1.2 V minimum, 1.4 V maximum), an internal gate forces $\overline{CE}$ OUT high, independent of $\overline{CE}$ IN. The $\overline{CE}$ output also is forced high when V_{CC} is less than V_{BATT} .

1.14 1.3-V Comparator and Power-Fail Warning

The PFI is compared with an internal 1.3-V reference, as shown in Fig. 1-4. The $\overline{PFO}$ goes low when the voltage at PFI is less than 1.3 V. Typically, PFI is driven by an external voltage divider that senses either the unregulated DC input to the system 5-V regulator or the regulated 5-V output. The voltage divider ratio can be chosen so that the voltage at PFI falls below 1.3 V several milliseconds before the +5-V supply falls below 4.75 V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75 V and the RESET output goes low (4.5 V for MAX692/93).

The power-fail detector can monitor the backup battery to warn of a low-battery condition. To conserve battery power, the power-fail detector comparator is turned off and $\overline{PFO}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

The MAX696/67 (Fig. 1-5) power-fail detector operates in a similar manner to that just described except that the voltage-divider ratio is chosen so that the voltage at PFI falls below 1.3 V several milliseconds before the LL_{IN} falls below 1.3 V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before LL_{IN} falls below 1.3 V and the RESET goes low.

1.15 Watchdog Timer and Oscillator

Figure 1-9 shows the watchdog timer circuits in block form. These circuits monitor the activity of the microprocessors. If the microprocessor does not toggle the WDI within the selected timeout period, a 50-ms $\overline{RESET}$ pulse is generated. (The $\overline{RESET}$ for MAX694 is 200 ms.) Because many systems cannot service the watchdog timer immediately after a reset, the MAX691/93/95 circuit has a longer timeout period after a reset is issued.

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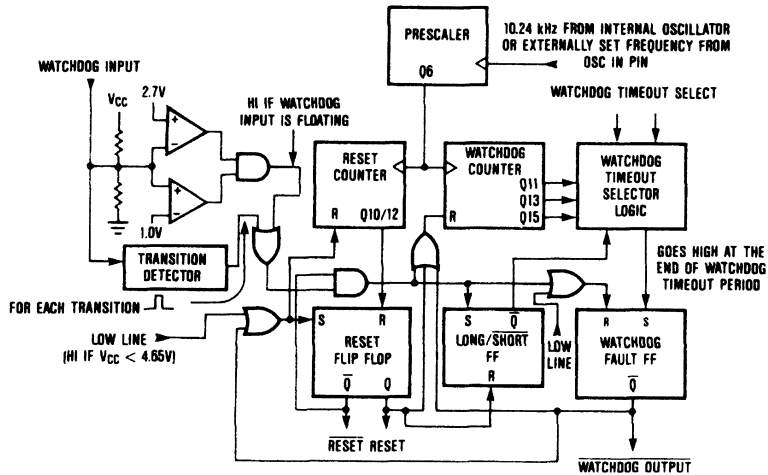


Figure 1-9. Typical watchdog timer and oscillator circuits. (Maxim New Releases Data Book, 1992, p. 5-28)

The normal timeout period for all microprocessor supervisors in this series becomes effective after the first transition of WDI after $\overline{\text{RESET}}$ has gone high. The watchdog timer is restarted at the end of reset, whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses are issued every 1.6 seconds. The watchdog monitor can be deactivated by means of floating the WDI.

The watchdog output (WDO) goes low if the watchdog timer times out and remains low until set high by the next transition on the watchdog input. WDO also is set high when V_{CC} goes below the reset threshold.

The internal oscillator is enabled when OSC SEL is floating. In this mode, OSC IN selects between the 1.6-s and 100-ms watchdog timeout periods. In either case, immediately after a reset, the timeout period is 1.6 s. This gives the microprocessor time to initialize the system.

If OSC IN is low, the 100-ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the input-output (I/O) port driving WDI is left in the power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog-timeout period of 70 ms.

For Further Information

When applicable, the source for each circuit or table is included in the circuit or table title, so that the reader may contact the original source for further information. To this end, the mailing address and telephone and facsimile number for each source is given in this section. When writing or calling, give complete information, including circuit title and description. All circuit diagrams and tables have been reproduced directly from the original source, without redrawing or resetting, with permission of the original publisher in each case.

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