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Application
For
10 *United States Non-Provisional Utility Patent*

Title:
15 Embedded System Boot from a Storage Device

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Inventors:

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Embedded System Boot from a Storage Device

CROSS-REFERENCE(S) TO RELATED APPLICATIONS

5 **[001]** This application claims the benefit of and priority
to U.S. Provisional Application 61/801,952, filed 15 March
2013. This U.S. Provisional Application 61/801,952 is
hereby fully incorporated herein by reference.

10

BACKGROUND

Field

The present invention relates generally to computers having a single or multiple
Central Processing Units (CPU), and more particularly, to a method and device for
15 booting such a system directly from a storage device.

Description of Related Art

An embedded system refers to an apparatus that is made up of a single or multiple
controller chips interconnected to each other on a printed circuit board. A controller chip
can have one or more central processing unit (CPU) that enables it to interpret and
20 execute code. When an embedded system has more than one processor it is already called
a multiprocessor system. The term embedded system will be used to refer to a single CPU
or a multiprocessor system in this paper.

A conventional embedded system contains a nonvolatile memory which is used to
store firmware that is read and executed by a CPU to initialize the system. The

nonvolatile memory can be a read-only memory (ROM), one-time programmable memory (OTP), programmable read only memory (PROM), electrically erasable PROM (EEPROM), or a flash PROM (FPROM). The nonvolatile memory can be internal (on-chip) or external (off-chip) to the controller chip. The firmware stored in the nonvolatile memory can be a boot code loader, a basic input/output system (BIOS), an operating system (OS), or an application firmware. The boot code loader is a small code executed by a CPU to do minimum initialization of the system. After initialization, the boot code loader copies the BIOS or OS or application firmware from a mass storage device external to the embedded system to the random access memory (RAM) of the system.

10 When the BIOS or OS or application firmware is already loaded in the RAM, the CPU reads and executes it to do exhaustive initialization and diagnostics before proceeding to normal system operation. A mass storage device can be a rotating disk drive or a solid-state drive which is made up of FPRAM devices. Though nonvolatile memory size can be reduced due to a small boot code loader, the boot code loader doesn't have the ability to

15 self check its integrity.

In an invention described in US Patent Application Publication number US 2005/0120146 A1, June 2 2005, an embedded system in FIG. 1 that does not have an on-chip nonvolatile memory such as a read only memory directly boots from flash block mass storage **106**. The flash block mass storage **106** is a collection of flash chips

20 interfaced to the flash memory controller **105**. The apparatus makes use of a Flash Programming Engine, embedded within a Flash memory controller **105**, the first device that is taken out of reset, to program a Direct Memory Access controller **104** to transfer a boot code loader from flash block mass storage **106** to an internal Random Access

Memory (RAM) **103**. When the transfer of the boot code loader to the RAM **103** is completed the internal Central Processing Unit **101** of the controller chip is taken out of reset to read and execute the boot code loader in the RAM **103**. The boot code loader performs initialization of the system, power-on self tests, and copies a much larger control program or application firmware from flash block mass storage **106** to the RAM **103**.

SUMMARY

The invention that is described in this document makes use of a minimum amount of non-volatile memory in order to boot an embedded system. Reduction in size of the nonvolatile memory brings about an advantage in terms of cost and complexity. The invention also allows the system to verify the integrity of data and code used in the boot process.

In some cases, the configuration registers of an embedded system may need to be initialized even before any of the CPU of the system is brought out of reset to begin execution of the system firmware. The invention presented in this paper will also address this issue of pre-initialization.

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The present invention provides a mechanism for booting up a system using a minimum amount of nonvolatile memory. This method also enables the embedded system to initialize all configuration registers even before any of the CPUs of the system

is brought out of reset. The embedded system consists of multiple controller chips or a single controller chip. The embedded system can have a single or multiple central processing units.

The present invention comprises of at least one Central Processing Unit (CPU) which reads and executes firmware; a random access memory (RAM) which is used to temporarily store firmware; a memory controller which provides interface to the RAM; a Reset Controller which maintains the reset states of all the devices of the embedded system; a Power-On Reset Sequencer which controls the overall boot process of the embedded system; nonvolatile memory and controller used to store data used by the Power-On Reset Sequencer in the boot process; at least one direct memory access (DMA) controller which initiates and tracks data transfers; a storage device controller which provides interface to the storage device; a CPU bus which interconnects the devices of the system; and a storage device which is used to store system firmware; a debug interface used to pre-program the nonvolatile memory and storage device with data and code.

The present invention describes the structure of the Power-On Reset (POR) Sequencer and its operation. The POR Sequencer makes use of a POR Sequencer Descriptor which is a preassembled descriptor that is stored in a nonvolatile memory of the system. The POR Sequencer descriptor contains register information and direct memory access (DMA) controller descriptors. The register information are read and used by the POR Sequencer to update the configuration registers of the system. The DMA descriptors are loaded by the POR Sequencer to the DMA controllers of the system. The

POR Sequencer facilitates the boot process and takes care of verifying the integrity of loaded data and code in the RAM.

The POR Sequencer Descriptor of the current invention is not limited to a single data structure. A linked-list of data structures is presented to increase the amount of register information and DMA descriptors available for processing by the POR Sequencer.

The present invention also provides a method of copying POR Sequencer Descriptor from nonvolatile memory to the RAM and verifying its integrity; a method of initializing the configuration registers by the POR Sequencer; a method of copying the system firmware from the storage device to the RAM; and a method of releasing the CPUs of the system from reset.

Initially, the system's nonvolatile memory and storage device contain nothing. When the system is powered up, no boot process occurs but the debug interface and a CPU are released from reset. The system integrator loads a program to the RAM via the debug interface. The program contains code to burn the POR Sequencer Descriptor in nonvolatile memory and to save a copy of the System Firmware in the storage device.

The method of copying POR Sequencer Descriptor from nonvolatile memory to RAM starts when the supply voltage of the system becomes stable after power-up. Then the Reset Controller, the POR Sequencer, the CPU Bus, the memory controllers, the DMA controllers, and the storage device controllers are released from reset. Then the POR Sequencer detects the presence of the POR Sequencer Descriptor in the nonvolatile memory. If the POR Sequencer Descriptor is not detected, then the debug interface and a CPU of the system are released from reset. If the POR Sequencer Descriptor is detected,

then the POR Sequencer copies the POR Sequencer Descriptor from nonvolatile memory to RAM. This step ends after the verification of the copied POR Sequencer Descriptor to the RAM completed without error.

5 The method of initializing the configuration registers of the system starts when the first register information of the POR Sequencer Descriptor is read. Then the register indicated by the register information is updated with a new set of configuration. This sequence is repeated until the last register information of the POR Sequencer Descriptor is read and processed. Then the step proceeds to the processing of the DMA descriptor. The type of the DMA descriptor is identified by the POR Sequencer. If the DMA
10 descriptor points to another set of register information then the DMA transfer will update the register information and DMA descriptor spaces of the current POR Sequence Descriptor in the RAM. If the DMA descriptor points to a system firmware fragment then this step is ended and the sequence proceeds to the next method.

The next method is the step where the system firmware stored in the external
15 storage device is copied to the RAM of the embedded system. The system firmware can be a boot code loader, a BIOS, an operating system, or a plain application firmware. This step starts when the POR Sequencer identifies that the DMA descriptor points to a system firmware fragment. The POR Sequencer loads the DMA or DMAs with the DMA Descriptors that will copy the system firmware fragments to the RAM. The POR
20 Sequencer waits for completion signals from all DMA controllers that have been loaded with DMA descriptors before proceeding in the process flow. If the last DMA descriptor of the current POR Sequencer Descriptor points to another set of DMA Descriptors then another set of system firmware fragments must be copied from the storage devices to the

RAM. If the last DMA descriptor of the current POR Sequencer Descriptor points to the last system firmware fragment then this step ends. The storage device refers to a single storage device or a plurality of storage devices of the same type.

The last step is the release of the CPUs of the embedded system from reset.

- 5 When the system has a single CPU, after the system firmware is loaded in the RAM, the POR Sequencer configures the reset controller to release the CPU from reset. Then the CPU starts reading and executing the system firmware. In a multi-CPU system, a CPU is released from reset. Then, the CPU reads and executes the system firmware in the RAM. The system firmware will have instructions to sequence the release of the other CPUs
- 10 from reset either one at a time or simultaneously.

BRIEF DESCRIPTION OF DRAWINGS

- So that the manner in which the above recited features, advantages and objects of the present invention
- 15 are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

- It is to be noted, however, that the appended
- 20 drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

FIG. 1 shows a prior art embedded system that implements a mechanism to directly boot from flash block mass storage.

FIG. 2 is a block diagram of an embedded system with a power-on reset sequencer that manages the initialization and boot up of the system.

5 FIG. 3 is a block diagram which presents the internal organization of the power-on reset sequencer and its interconnection to the RAM via a memory controller.

FIG. 4 shows the structure of the power-on reset sequencer descriptor.

FIG. 5 illustrates a linked-list data structure of the power-on reset sequencer descriptor.

10 FIG. 6 is a flow chart of the sequence used in copying the power-on reset sequencer descriptor from nonvolatile memory to the RAM.

FIG. 7 is a flow chart of the sequence used in the register initialization phase of the power-on reset sequencer.

15 FIG. 8 is a flow chart of the sequence used in copying the system firmware from the storage device to the RAM.

FIG. 9 is a flow chart of the sequence used in releasing the CPUs of the embedded system from their reset states.

DETAILED DESCRIPTION

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The present invention relates a method and device for booting up a system from a storage device and further relates a method for enabling a system to initialize all configuration registers even before any of the CPUs of the system is brought out of reset.

FIG. 2 is a block diagram showing a typical embodiment of the present invention. The figure shows an embedded system **200** comprising a CPU bus **202** interconnecting a single CPU **201** or a plurality of CPUs **201**, a single DMA controller **203** or a plurality of DMA controllers **203**, a reset controller **206**, a power-on reset (POR) sequencer **207**, a
5 RAM controller **205**, a nonvolatile memory controller **214**, a storage device controller **204**, and a debug interface **216**. Also comprising the system is an internal RAM **208**, a small nonvolatile memory **215** and a storage device **209**. A storage device type may be a mechanical disk drive, a mobile flash drive, or a solid-state drive.

The storage device controller **204** controls the storage device or devices **209**
10 connected to it. A storage device or a plurality of storage devices **209** are connected to the storage device controller **204** via an IO bus **210** for the case of interface standards such as IDE/ATA, Serial ATA, SCSI/SAS, PCI/PCI-X, USB, Firewire, Bluetooth, Fibre Channel and PCI Express. For a solid-state drive, a flash bus is used to connect to the storage device controller **204** which also called a flash controller. The reset controller
15 **206** handles the reset states of all the devices in the system. One or a plurality of DMA controllers **203** initiates and tracks data transfers. The storage device controller **204** provides interface to the storage device **209**. The storage device **209** is used to store system firmware **211** or a fragment of the system firmware **211**. When the POR sequencer descriptor exceeds the space of the nonvolatile memory, the descriptor is
20 divided into fragments **212**, **213** and distributed across the nonvolatile memory **215** and storage devices **209**.

The multi-port memory controller **205** interfaces the RAM **208** to the CPU bus **202** and to the POR sequencer **207**. The POR sequencer **207** processes the POR

sequencer descriptor which contains information to initialize configuration registers of the system and DMA descriptors used to fetch other POR sequencer descriptor fragments **213** and the system firmware **211**. The POR sequencer **207** takes care of loading the system firmware to the RAM and verifying its integrity. After the system firmware has
5 been loaded in the RAM and the system's configuration registers pre-initialized, the POR sequencer sequences the release of the CPUs from their reset states.

The nonvolatile memory **215** with its controller **214** is used to store the head of the POR sequencer descriptor **212** used by the POR sequencer **207** in the boot process. Initially, the system's nonvolatile memory and storage devices attached to the system are
10 empty. When the system is powered up the boot process exits to emulation mode since there are no POR sequencer descriptor to process and no system firmware to load and execute in memory. The system integrator which writes program for the system loads a firmware to the RAM of the system via the debug interface **216**. The firmware loaded in the RAM has a routine that writes the POR sequencer descriptor and system firmware to
15 the nonvolatile memory **215** and storage devices **209** attached to the system. After the POR sequencer descriptor and system firmware has been written to the nonvolatile memory and storage devices, the next time the system is powered up, the system doesn't exit to emulation mode instead it continues with the boot process until all CPUs **201** of the system are released from their reset states.

20 FIG. 3 is a schematic diagram that illustrates the structure and interconnection between the POR sequencer **300** and the multi-port memory controller **308**. For the POR sequencer **300**, data and control signals to and from the CPU bus **304** is managed by the bus master interface **303** while control signals to and from the RAM **311** is managed by

the memory controller port interface **302**. The POR sequencer state machine **301** utilizes the bus master interface **303** to perform data transfer to and from the CPU bus and the memory controller port interface **302** to do data transfer to and from the RAM **311**. The POR sequencer **300** combines the use of the bus master interface **303** and the memory
5 controller port interface **302** in order to control transfers to and from the RAM **311**.

The POR sequencer **300** transfers the POR sequencer descriptor from the nonvolatile memory or from the storage device to the RAM **311** before it is processed. When the POR sequencer descriptor is already loaded in the RAM **311**, the POR sequencer state machine reads a part of the descriptor from RAM to parse and interpret.
10 Depending on the content of the part of the POR sequencer descriptor, the POR sequencer state machine decides whether to get another part of the descriptor from RAM, transfer data from RAM to a device mapped on the CPU bus **304**, or to write data that it generated to the RAM or to a device mapped on the CPU bus **304**. Through the use of POR sequencer state machine **301**, memory controller port interface **302**, and bus master
15 interface **303** the POR sequencer **300** is able to do the following tasks: transfer of DMA controller descriptor to the DMA controller's configuration register space, activation of the DMA controller, initialization of configuration registers, and copy of data from storage device or nonvolatile memory to the RAM.

The multi-port memory controller **308** has several port interfaces. Port 1 interface
20 **307** provides devices on the CPU bus **304** access to the RAM **311**. Port 2 interface provides the POR sequencer **300** access to the RAM **311**. The data path multiplexers **309** route the read and write requests from the POR sequencer **300** and the CPU bus **304** to the RAM **311**. The controller **310** manages how the data path multiplexers **309** behave in

response to the read and write requests received from the POR sequencer **300** and CPU bus **304**.

FIG. **4** shows the POR sequencer descriptor format. The POR sequencer descriptor is comprised of the register information space **401**, the DMA descriptor space **403**, and an optional POR sequencer descriptor checksum **407**. The register information space consists of controller core register information **402** used by the POR sequencer to update the configuration registers of the system. The DMA descriptor space **403** on the other hand consists of the POR sequencer DMA descriptors' control information **404** and one or more DMA controller descriptors **406**. The DMA controller descriptors **406** are loaded by the POR Sequencer to the DMA controller's configuration register space. The POR sequencer DMA descriptors' control information **404** contains information about the DMA controller descriptors **406** of the current POR sequencer descriptor.

When the POR sequencer descriptor doesn't fit in the nonvolatile memory of the system, the descriptor is divided into fragments and distributed across the nonvolatile memory and storage devices attached to the system. FIG. **5** gives us an illustration of a fragmented POR sequencer descriptor. POR sequencer descriptor fragment 0 **501** is stored in the nonvolatile memory. Fragment 0 comprises of register information space **505**, DMA descriptor space **503**, and POR sequencer descriptor checksum **504**. The DMA descriptor space **503** is composed of DMA controller descriptors 0 to P. The last DMA controller descriptor **506** of the POR sequencer descriptor fragment **501**, **502** points to the next POR sequencer descriptor fragment **502**. POR sequencer fragment 1 to N **502** have only two parts, the register information space **505** and DMA descriptor space **503** in contrast to POR sequencer descriptor fragment 0 **501** which is made up of three

parts. The POR sequencer descriptor fragment **501** or **502** may or may not have a register information space **505**. The last DMA controller descriptor **507** of the last POR sequencer descriptor fragment points to the last fragment of the system firmware in the storage device.

5 FIG. 6 is a flowchart showing the process of transferring the POR sequencer descriptors **212**, **213** from nonvolatile memory **215** and storage device **209** to the RAM **208**. After the system is powered-up and the input power supply stabilizes in block **601**, the CPU bus **202**, reset controller **206**, DMA controller **203**, storage device controller **204**, RAM controller **205**, nonvolatile memory controller **214** and POR sequencer **207** are
10 brought out of reset in block **602**. The POR sequencer **207** then detects the presence of POR sequencer descriptor **212** in the nonvolatile memory in block **603**. If the first copy of the POR Sequencer descriptor **212** is detected, then POR sequencer **207** copies the POR sequencer descriptor **212** from the nonvolatile memory **215** to the RAM **208** in block **606**. POR sequencer **207** then checks the integrity of POR sequencer descriptor **212**
15 in block **606** by comparing the computed checksum to the POR sequencer descriptor checksum **507**. If no error is found then copying of POR sequencer descriptor **212** from nonvolatile memory **215** to the RAM **208** is completed. If an error is found, a POR sequencer error handler is activated in block **612**. If the first copy **212** is unsuccessfully detected in step **604**, in block **609**, the POR sequencer will try to detect a second copy of
20 the POR sequencer descriptor which is not shown in FIG. 2. If successful, the POR sequencer **207** will copy the backup copy of the POR sequencer descriptor from the nonvolatile memory **215** to the RAM **208** in block **605**. If not, the POR sequencer **207**

releases the debug interface **216** and a CPU **201** from reset to allow a system integrator from updating the nonvolatile memory **215** with a new POR sequencer descriptor **212**.

FIG. 7 illustrates the register initialization phase by the POR sequencer **207**.

Starting from block **701**, the POR sequencer **207** reads the first register information in the register information space **401** of the POR sequencer descriptor **212** from the RAM **208**.
The POR sequencer **207** then processes the register information and then updates the corresponding configuration register based on the contents of the register information in block **702**. Steps **701** and **702** are repeated for succeeding register information until the last register information of the current POR sequencer descriptor **212** is read and processed. After the last register information is read, the POR sequencer **207** writes the DMA controller descriptor **406** to the DMA controller's register space in block **704**. The POR sequencer **207** then activates the DMA controller **203** in block **705**. The DMA controller **203** then processes the DMA controller's descriptor **406** that it received and initiates transfer of data from the storage device **209** to the RAM **208** via the storage device controller **204** in block **706**. When the data transfer is finished, in block **707**, the DMA controller **203** informs the POR sequencer **207** that the data transfer has completed. The POR sequencer **207** then reads the POR sequencer DMA descriptor's control information **404** in block **608**. It then checks if the DMA controller descriptor **406** points to a new set of register information of another POR sequencer descriptor fragment **502** in block **709**. If the test is positive, the register initialization phase is repeated starting with block **701**. If the test is negative, then the register initialization phase has ended.

DMA controller descriptors **406** are not only used to fetch POR sequencer descriptor fragments **501**, **502**. They are also used to transfer system firmware **211** from

the storage device to the RAM **208**. In FIG. **8**, the copying of system firmware **211** from the storage device **209** to the RAM **208** is illustrated. The process starts with the POR sequencer **207** reading a DMA controller descriptor **406** from RAM **208** and then writing the DMA controller descriptor **406** to the configuration space of an available DMA
5 controller **203** in block **801**. The POR sequencer **207** then activates the DMA controller **203** in block **802**, which would then cause the DMA controller **203** to start the transfer of a system firmware fragment **211** from the storage device **209** to the internal RAM **208** via the storage device controller **204** in block **803**.

The POR sequencer **207** then reads the DMA descriptor control information **404**
10 from RAM **208** in block **804**. If the DMA descriptor **406** points to the last system firmware fragment, the POR sequencer **207** waits for all busy DMA controllers to complete their transfers in block **809**. The POR sequencer **207** then verifies the integrity of the copied system firmware in block **811**. If the system firmware is error free then the sequence completes. If an error is found, an error handling routine will be executed in
15 block **813**. In block **805**, if the DMA controller descriptor **406** does not point to the last system firmware fragment, which means there are succeeding system firmware fragments, then the POR sequencer **207** proceeds to block **806** to check if the said DMA controller descriptor **406** was the last descriptor of the current POR sequencer descriptor. If it is the last DMA controller descriptor **406** of the current frame, then POR sequencer
20 **207** waits for all the busy DMA controllers to complete their transfers in block **810**. The process is repeated starting from block **801** for the next POR sequencer descriptor which will be used to fetch the next system firmware fragment **211**.

In block **806**, if the DMA controller descriptor **406** of the current POR sequencer descriptor is not the last one, then the availability of a DMA controller **203** is determined in block **807**. If there is no available DMA controller, meaning, all the DMA controllers **203** are busy, then the POR sequencer **207** waits for a DMA controller **203** to complete its transfer in block **808** before proceeding to process the next DMA controller descriptor **406**. When a DMA controller becomes available the process goes back to block **801**.

FIG. **9** describes the process of releasing the CPUs **201** from their reset state. The POR sequencer **207** first configures the reset controller **206** to release a CPU **201** from reset in block **901**. This CPU is usually referred to as the bootstrap CPU. After coming out of reset, the bootstrap CPU reads and executes the system firmware from RAM **208** in block **902**. Then the bootstrap CPU performs full system initialization and diagnostics in block **903**. If the diagnostic failed, a system firmware error handling routine is executed in block **905**. If the system diagnostics is successful, the release of other CPUs, if present, proceeds. The system firmware instructs the reset controller **206** to release the next CPU from reset in block **908**. The next CPU is released from reset which then reads and executes a copy of the system firmware in block **909**. This process ends when all of the CPUs **203** have been brought out of reset. At this point, the system firmware exits system initialization phase and waits for service calls from the controller cores of the embedded system.

[002] Foregoing described embodiments of the invention are provided as illustrations and descriptions. They are not intended to limit the invention to precise form described. In particular, it is contemplated that functional implementation of invention described herein may be

implemented equivalently in hardware, software, firmware, and/or other available functional components or building blocks, and that networks may be wired, wireless, or a combination of wired and wireless.

5 **[003]** It is also within the scope of the present invention to implement a program or code that can be stored in a machine-readable or computer-readable medium to permit a computer to perform any of the inventive techniques described above, or a program or code that can be stored in
10 an article of manufacture that includes a computer readable medium on which computer-readable instructions for carrying out embodiments of the inventive techniques are stored. Other variations and modifications of the above-described embodiments and methods are possible in light of the
15 teaching discussed herein.

[004] The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments
20 of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

[005] These modifications can be made to the invention in
25 light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following

claims, which are to be construed in accordance with
established doctrines of claim interpretation.

IN THE CLAIMS

What is claimed is:

1. An apparatus, comprising:

- 5 one or more CPUs, a reset controller, a storage device controller, one or more
direct memory access controllers, a RAM and its controller, a ROM and its controller, a
debug interface and a power-on reset (POR) sequencer.

10

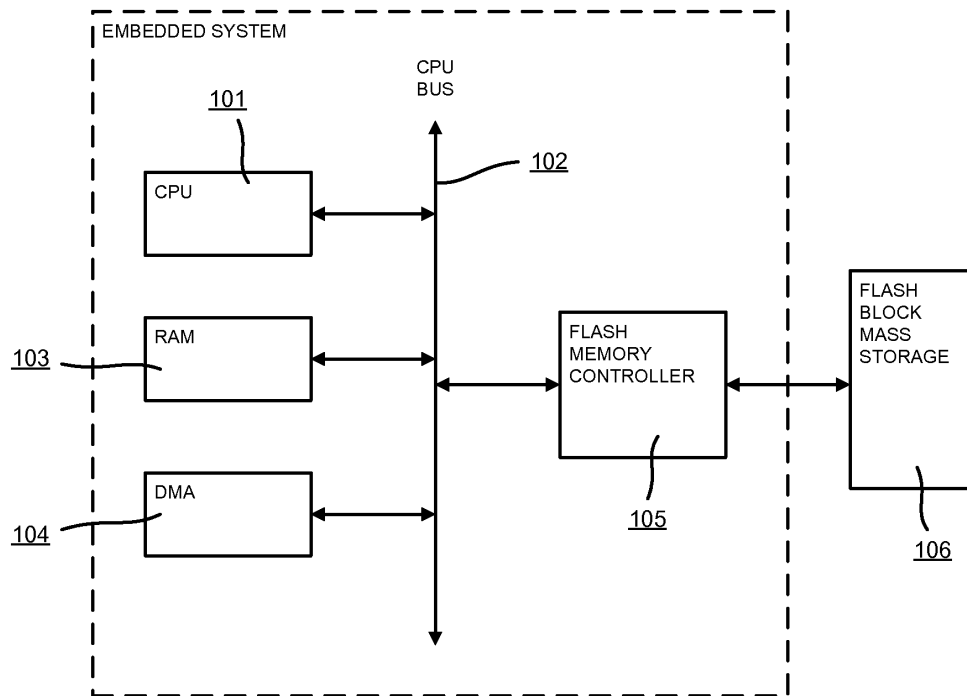
ABSTRACT

A mechanism of booting up a system directly from a storage device and a means of initializing an embedded system prior to activating a CPU is presented. The said system is comprised of one or more CPUs, a reset controller, a storage device controller, one or more direct memory access controllers, a RAM and its controller, a ROM and its controller, a debug interface and a power-on reset (POR) sequencer. The POR sequencer controls the overall boot process of the embedded system. Said sequencer uses descriptors (POR Sequencer descriptors) which are used to update the configuration registers of the system and to enable CPU-independent data transfers with the use of DMA controllers.

Using a minimal amount of non-volatile memory for booting up a system brings down costs associated with increased silicon real estate area and power consumption. Capability of pre-initializing the system even before a CPU is brought out of reset provides flexibility and system robustness. Through the use of the Power-On Reset Sequencer module, integrity of program code and user data used in the boot up process can be verified thus providing a resilient boot up sequence.

The present invention provides a mechanism for booting up a system using a minimum amount of nonvolatile memory. This method also enables the embedded system to initialize all configuration registers even before any of the CPUs of the system is brought out of reset. The embedded system consists of multiple controller chips or a

single controller chip. The embedded system can have a single or multiple central processing units.



PRIOR ART

FIG. 1

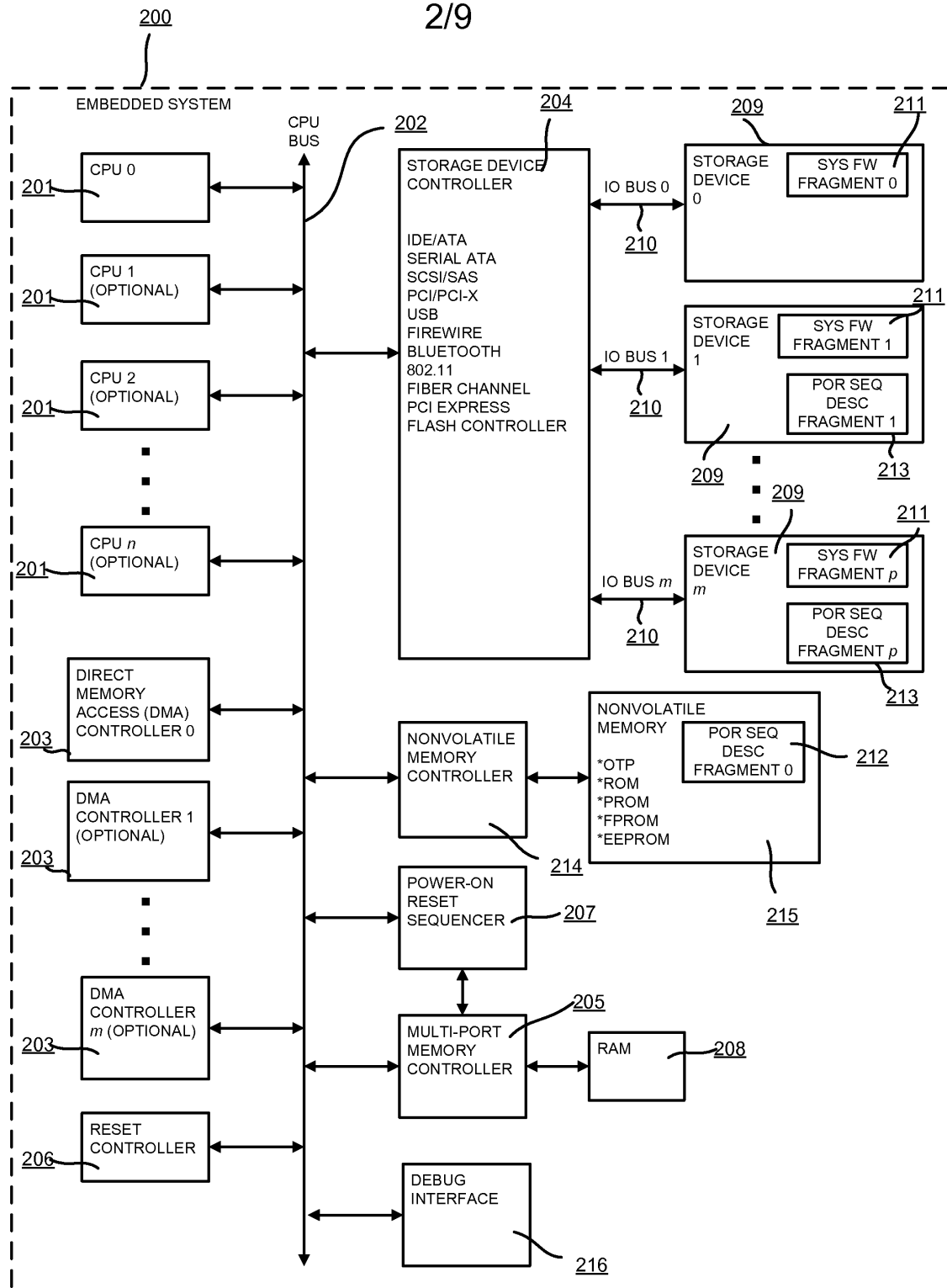


FIG. 2

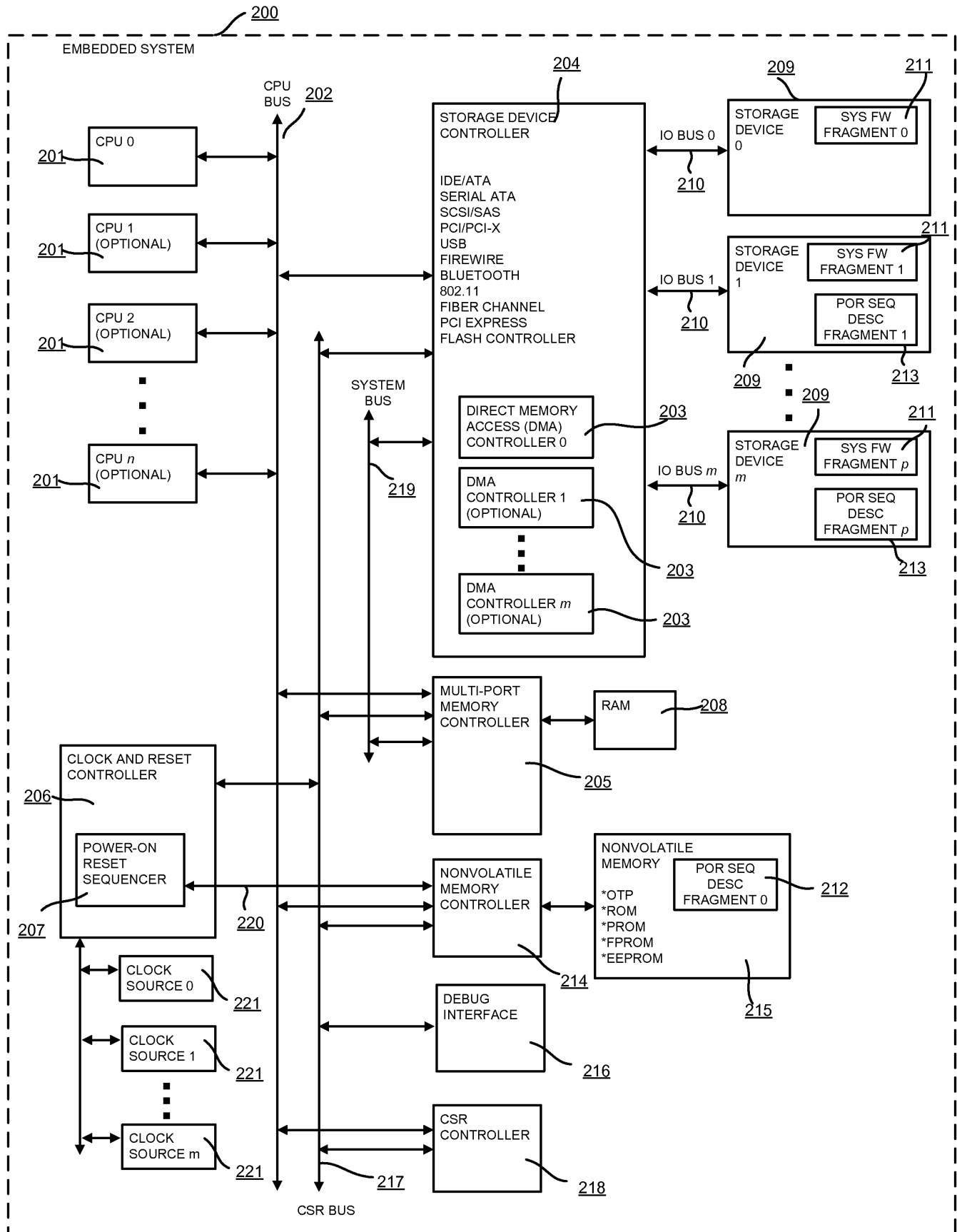


FIG. 2B

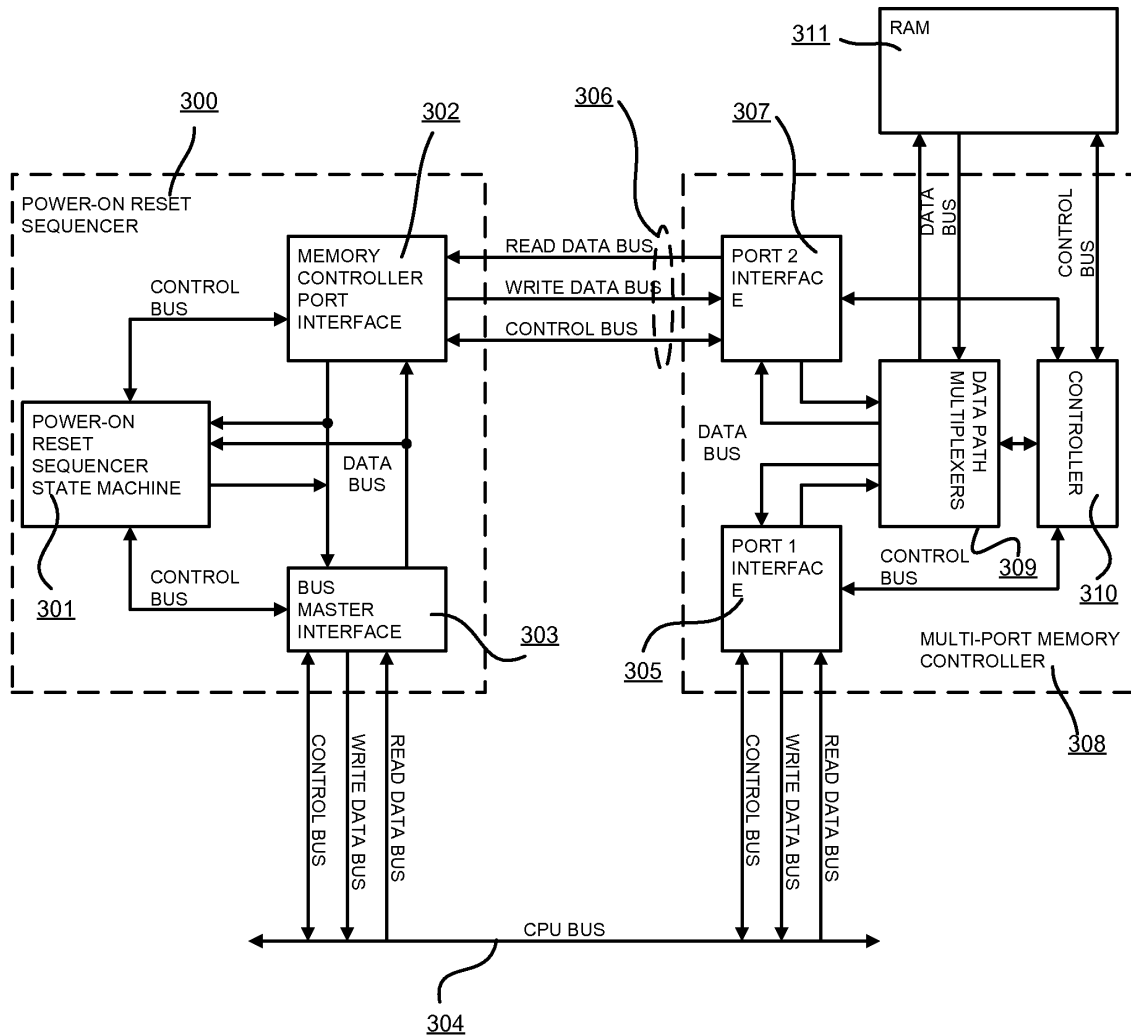


FIG. 3

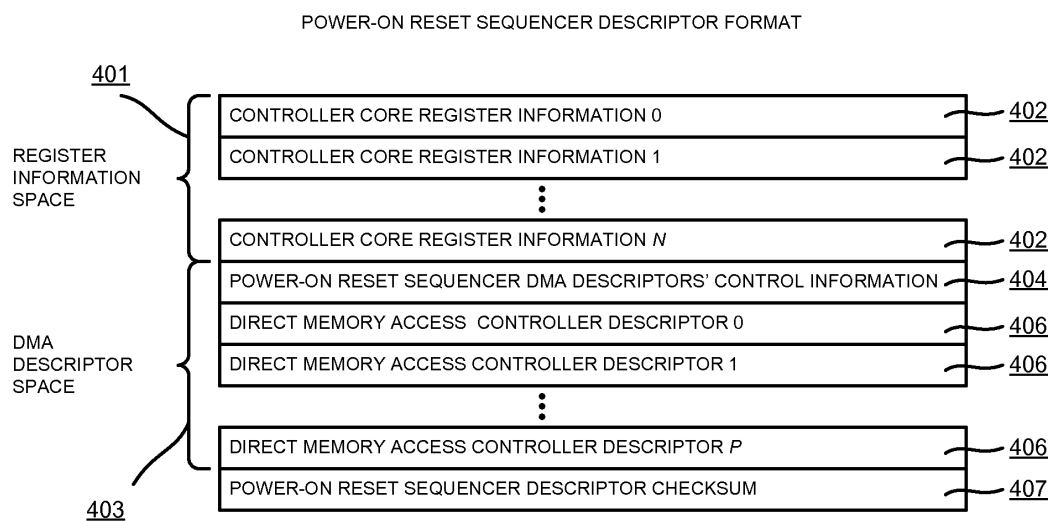
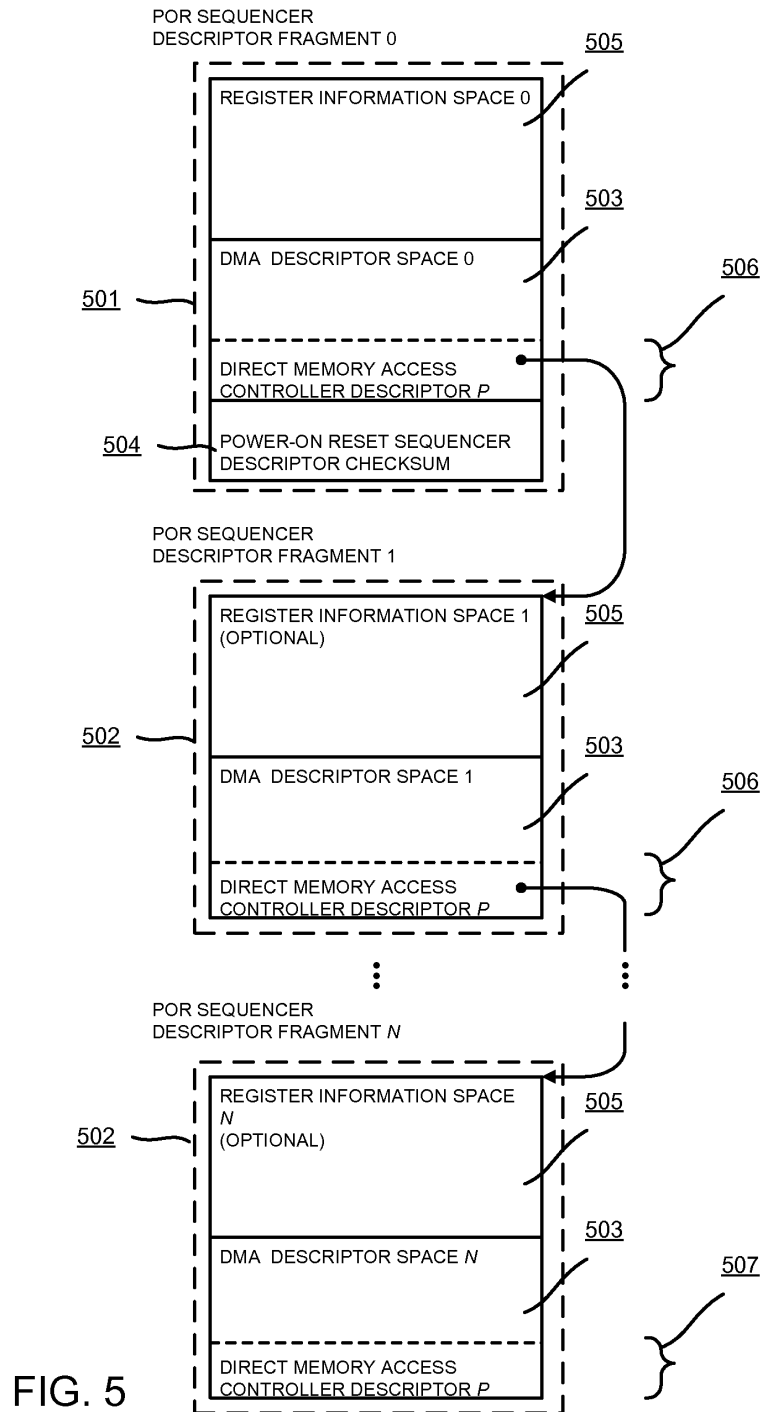


FIG. 4



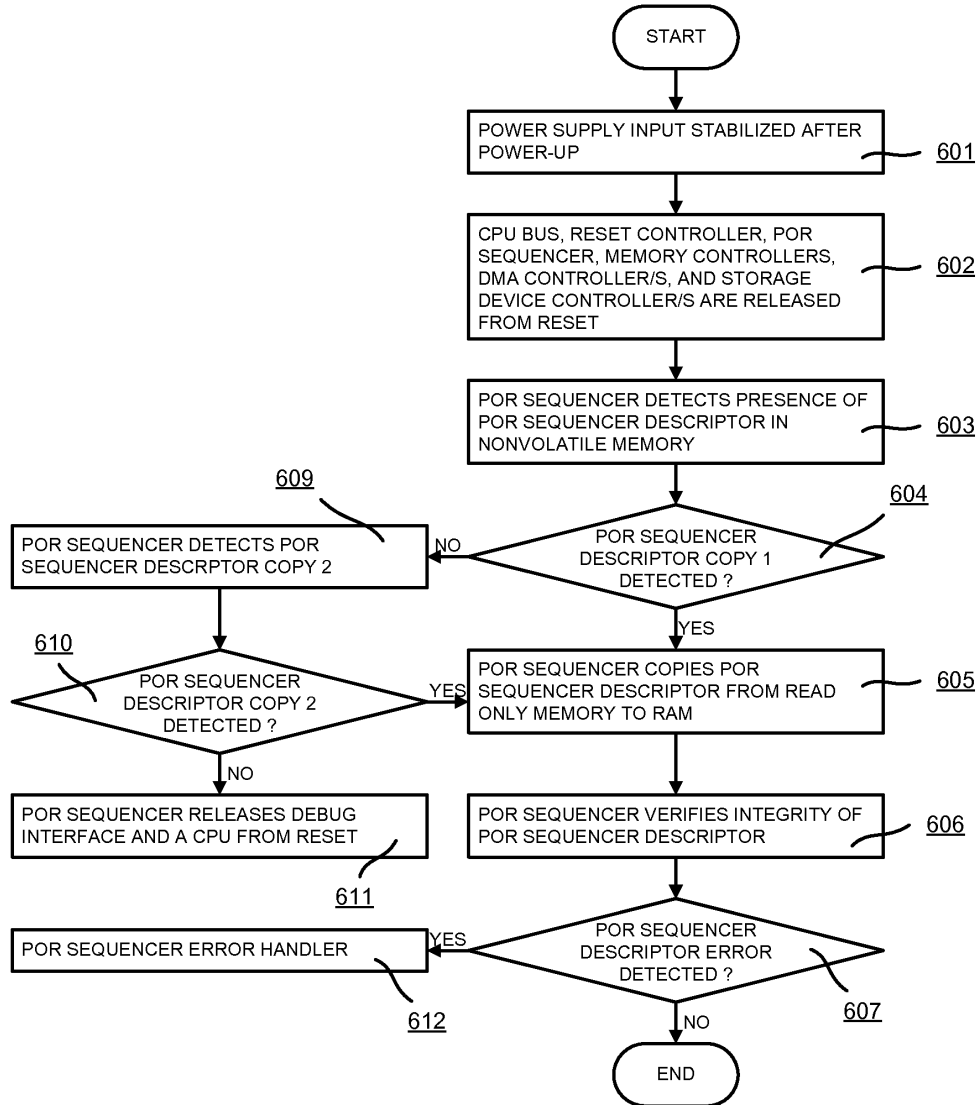


FIG. 6

7/9

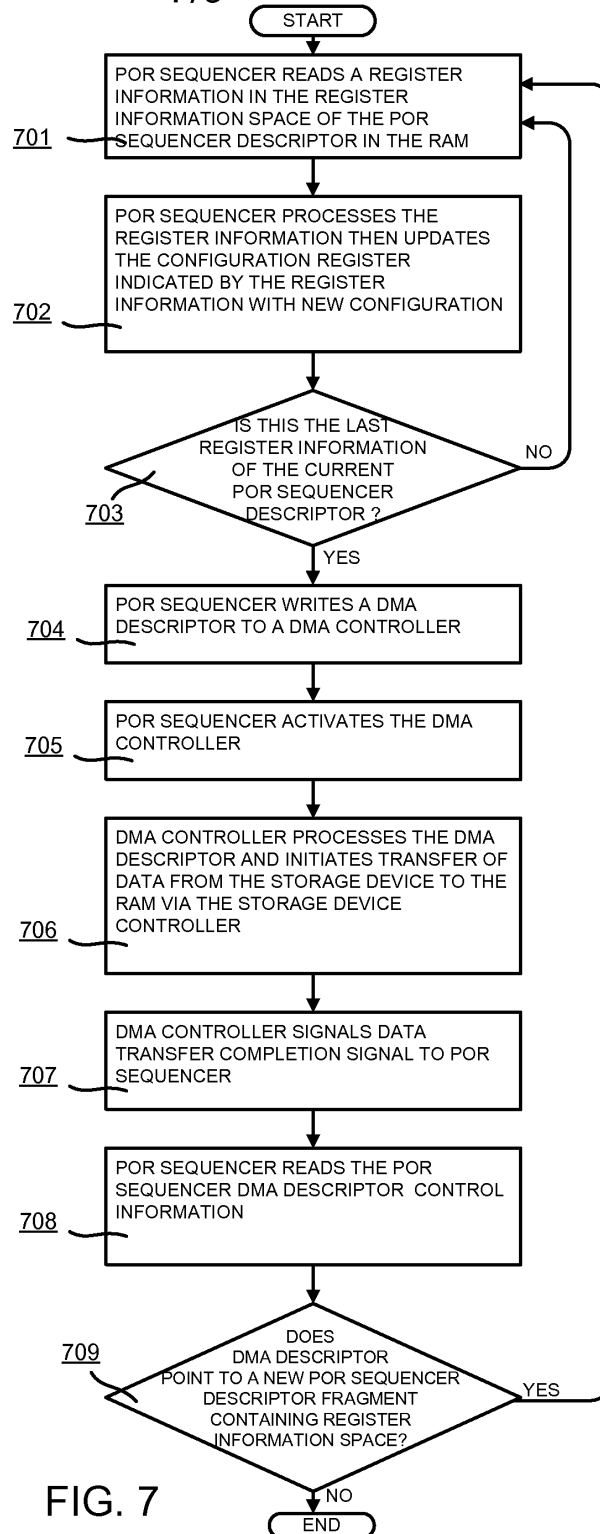


FIG. 7

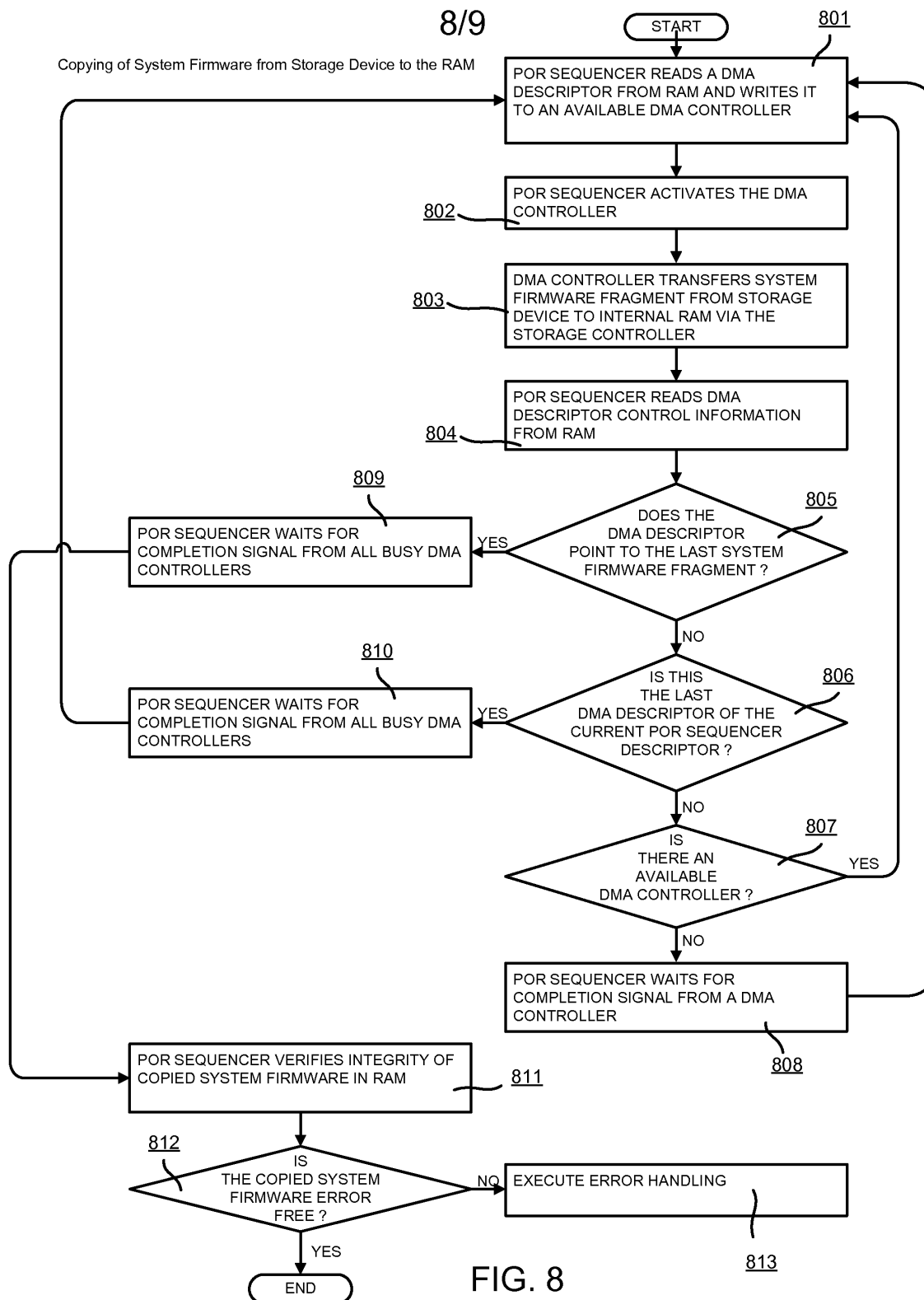


FIG. 8

Release of CPUs From Reset

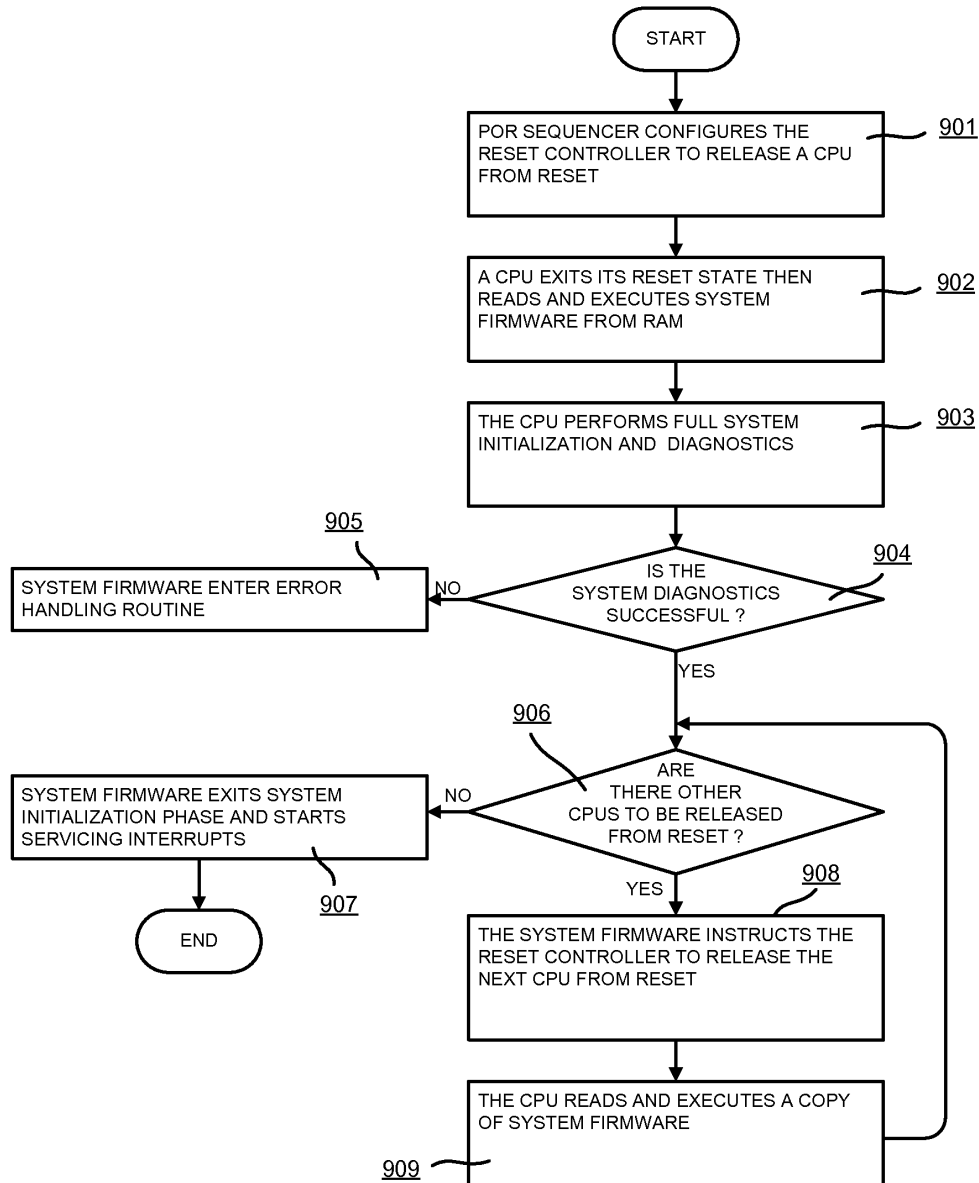


FIG. 9

Electronic Acknowledgement Receipt	
EFS ID:	18502210
Application Number:	14217365
International Application Number:	
Confirmation Number:	8249
Title of Invention:	Embedded System Boot from a Storage Device
First Named Inventor/Applicant Name:	Alvin Anonuevo Manlapat
Customer Number:	16428
Filer:	Arnold de Guzman
Filer Authorized By:	
Attorney Docket Number:	6005.018
Receipt Date:	17-MAR-2014
Filing Date:	
Time Stamp:	23:29:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	18spec.pdf	104687 c20d45a438064f16202bcb105a6c56041e45ab87	no	22

Warnings:

Information:

2	Drawings-only black and white line drawings	drawings_6005_018.pdf	81024 3097e1f8f6493553326b1d64759242ad526dffa8	no	10
Warnings:					
Information:					
Total Files Size (in bytes):			185711		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/217,365	03/17/2014	2115	0.00		1	1

CONFIRMATION NO. 8249

FILING RECEIPT



OC000000067684492

16428
BITMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

Date Mailed: 04/11/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Alvin Anonuevo Manlapat, Residence Not Provided;

Applicant(s)

Alvin Anonuevo Manlapat, Residence Not Provided;

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 04/09/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/217,365**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Embedded System Boot from a Storage Device

Preliminary Class

713

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/217,365			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720		
TOTAL CLAIMS (37 CFR 1.16(i))	1	minus 20 = *				x 80 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 420 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600		
APPLICATION AS AMENDED - PART II									
AMENDMENT A	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	OR OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		TOTAL ADD'L FEE	
AMENDMENT B	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	OR OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/217,365	03/17/2014	2115	1740	6005.018	1	1

CONFIRMATION NO. 8249

FILING RECEIPT



OC000000069167411*

16428
BITMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

Date Mailed: 06/25/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Alvin Anonuevo Manlapat, Residence Not Provided;

Applicant(s)

Alvin Anonuevo Manlapat, Residence Not Provided;

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

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If Required, Foreign Filing License Granted: 04/09/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/217,365**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Embedded System Boot from a Storage Device

Preliminary Class

713

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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NOT GRANTED

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SelectUSA

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249
16428	7590	02/18/2016	EXAMINER	
BiTMICRO Networks, Inc. ATTN: Patent Department 47929 Fremont Blvd Fremont, CA 94538			ELAMIN, ABDELMONIEM I	
			ART UNIT	PAPER NUMBER
			2116	
			NOTIFICATION DATE	DELIVERY MODE
			02/18/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

arnold@dcpatentlaw.com
bit-ip@bitmicro.com
mariedel.nolasco@bitmicro.com

Office Action Summary	Application No. 14/217,365	Applicant(s) MANLAPAT, ALVIN ANONUEVO	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2116	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 03/17/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☐ Claim(s) ____ is/are allowed.

7) ☐ Claim(s) ____ is/are rejected.

8) ☐ Claim(s) ____ is/are objected to.

9) ☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some** c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.

4) ☐ Other: ____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-9, drawn to an apparatus, comprising: an embedded system comprising one or more processors, a reset controller, ..., classified in class G06F 1/24.
 - II. Claims 10-20, drawn to a method of booting up an embedded system using a minimum amount of nonvolatile memory, classified in class G06F 9/4401.
3. The inventions are distinct, each from the other because of the following reasons:
4. Inventions I and II are directed to related inventions. The related inventions are distinct if: (1) the inventions as claimed are either not capable of use together or can have a materially different design, mode of operation, function, or effect; (2) the inventions do not overlap in scope, i.e., are mutually exclusive; and (3) the inventions as claimed are not obvious variants. See MPEP § 806.05(j). In the instant case, the inventions as claimed are different. Furthermore, the inventions as claimed do not encompass overlapping subject matter and there is nothing of record to show them to be obvious variants.
5. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) apply: Search for each invention can be made independently and sub class of each is different.

6. **Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.**

7. The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDELMONIEM ELAMIN whose telephone number is (571)272-3674. The examiner can normally be reached on MON - THUR 10:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ABDELMONIEM ELAMIN/
Primary Examiner, Art Unit 2116

February 11, 2016

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 8249
Alvin Anonuevo Manlapat et al.)	)
	) Examiner: not yet known
Serial No.: 14/216,627	) Telephone No.:
	)
Filing Date:	) Art Unit: 2115
March 17, 2014	)
	) Atty. Docket No.: 6005.018
Title: Embedded System Boot	)
From A Storage Device	) Customer No.: 16428
	)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO OFFICE ACTION
AND AMENDMENT**

Dear Sir:

The following is in response to the office action
mailed on 18 February 2016.

Amendments to the Claims are reflected in the listing of
claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) An apparatus, comprising:
 - an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and a power-on reset (POR) sequencer.
2. (previously presented) The apparatus of claim 1,
 - wherein the one or more processors reads and executes firmware;
 - wherein the reset controller maintains reset states of all devices of the embedded system;
 - wherein the storage device controller provides an interface to a storage device;
 - wherein the one or more direct memory access controllers initiates and tracks data transfers;
 - wherein the RAM is used to temporarily store firmware;
 - wherein the memory controller provides an interface to the RAM;
 - wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ROM controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

3. (previously presented) The apparatus of claim 1, wherein the POR sequencer uses a POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

4. (previously presented) The apparatus of claim 3, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

5. (previously presented) The apparatus of claim 4, wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

6. (previously presented) The apparatus of claim 1, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

7. (previously presented) The apparatus of claim 1, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

8. (previously presented) The apparatus of claim 1, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

9. (previously presented) The apparatus of claim 1, further comprising: a CPU bus in the embedded system.

10-20. (cancelled)

REMARKS/ARGUMENTS

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9.

II. Claims 10-20.

Applicant elects invention I to be examined. The election of invention I is made without traverse. Claims 1-9 are identified as claims encompassing the elected invention (invention I).

Applicant reserves the right to pursue any cancelled claims in a divisional or continuation application. Claims 10-20 are canceled without prejudice, waiver, or surrender of the subject matter contained therein. See e.g., *In re Tanaka*, No. 10-1262, (Fed. Cir. 2011); *In re Mostafazadeh*, No. 10-1260 (Fed. Cir. 2011).

The withdrawal of the rejections to claims is respectfully requested.

Favorable action is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicant is not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: 21 February 2016

Respectfully submitted,

/Arnold de Guzman/
 Arnold de Guzman
 Attorney for Applicant(s)
 Reg. No. 39,955

Please send correspondence to:
 Customer No. 16428

CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	21 February 2016
Express Mail Mailing Number (optional):			

Electronic Acknowledgement Receipt	
EFS ID:	24973413
Application Number:	14217365
International Application Number:	
Confirmation Number:	8249
Title of Invention:	Embedded System Boot from a Storage Device
First Named Inventor/Applicant Name:	Alvin Anonuevo Manlapat
Customer Number:	16428
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.018
Receipt Date:	21-FEB-2016
Filing Date:	17-MAR-2014
Time Stamp:	12:14:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	6005_018_response.pdf	33693 4cc8f2719183da9814f036c8c923f001ee912796	no	6

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249
16428	7590	03/02/2016	EXAMINER	
BiTMICRO Networks, Inc. ATTN: Patent Department 47929 Fremont Blvd Fremont, CA 94538			ELAMIN, ABDELMONIEM I	
			ART UNIT	PAPER NUMBER
			2116	
			NOTIFICATION DATE	DELIVERY MODE
			03/02/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

arnold@dcpatentlaw.com
bit-ip@bitmicro.com
mariedel.nolasco@bitmicro.com

Office Action Summary	Application No. 14/217,365	Applicant(s) MANLAPAT, ALVIN ANONUEVO	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2116	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on amendment filed on 02/21/2016.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) 1-9 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☒ Claim(s) 1,2 and 6-9 is/are rejected.

8) ☒ Claim(s) 3-5 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some** c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 02/15/2016

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

4) ☐ Other: _____

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

3. Claims 1-2, 6-9 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Chow et al, US. Patent No. 7,676,640.

4. Claims 1, Chow teaches an apparatus, comprising:

an embedded system [*see abstract, Fig. 3*] comprising one or more processors [*CPU 320 of Fig. 3*], a reset controller [*Power-on reset 354 of Fig. 3*], a storage device controller [*323 of Fig. 3*], one or more direct memory access controllers [*DMA logic 331 of Fig. 3*], a random access memory (RAM) and a memory controller [*Main memory (RAM) 352 of Fig. 3*], a nonvolatile memory and a nonvolatile memory controller [*Booting ROM 350 of Fig. 3*], a debug interface [*see CRC16 and CRC17 of Fig. 3*], and a power-on reset (POR) sequencer [*see col. 11, lines 2021-22*].

5. Claim 2, Chow teaches the one or more processors reads and executes firmware [*see CPU 320 of Fig. 3, col. 10, lines 41-47*]; wherein the reset controller maintains reset states of all devices of the embedded system [*col. 15, lines 44-57*]; wherein the storage device controller

Art Unit: 2116

provides an interface to a storage device [*provide an interface to the flash memory 204 of Fig. 3*]; wherein the one or more direct memory access controllers initiates and tracks data transfers [*see DMA 331 of Fig. 3, col. 11, lines 12-19*]; wherein the RAM is used to temporarily store firmware; wherein the memory controller provides an interface to the RAM [*see RAM 352 and related disclosure*]; wherein the nonvolatile memory comprises a read only memory (ROM) [*ROM 350 of Fig. 3*]; wherein the ROM controller is used to store data used by the POR sequencer in a boot process of the embedded system [*ROM 350 of Fig. 3 and related disclosure*]; wherein the debug interface is used to pre-program the ROM and the storage device with data and code [*see ECC of Fig. 3 and related disclosure*]; and wherein the POR sequencer controls the boot process of the embedded system [*see col. 11, lines 20-22*].

6. Claims 6, Chow teaches the POR sequencer loads DMA descriptors to the DMA controllers [*see DMA 331 and related disclosure*].

7. Claims 7, Chow teaches the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM [*see CRC16 and CRC17 of Fig. 3 and related disclosure*].

8. Claims 9, Chow teaches a CPU bus in the embedded system [*see Fig. 3*].

Allowable Subject Matter

9. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDELMONIEM ELAMIN whose telephone number is (571)272-3674. The examiner can normally be reached on MON - THUR 10:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ABDELMONIEM ELAMIN/
Primary Examiner, Art Unit 2116

February 24, 2016

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 8249
Alvin Anonuevo Manlapat	)
	) Examiner:
	) Abdelmoniem I. Elamin
Serial No.: 14/217,365	) Telephone No.: 571.272.3674
	)
Filing Date:	) Art Unit: 2116
March 17, 2014	)
	) Atty. Docket No.: 6005.018
Title: Embedded System Boot	)
From A Storage Device	) Customer No.: 16428
	)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO OFFICE ACTION
AND AMENDMENT**

The following is in response to the office action
dated on 02 March 2016.

Amendments to the Specification begin on page 2 of this
paper.

Amendments to the Claims are reflected in the listing of
claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 8 of this paper.

In the substitute specification, please replace paragraph from page 12, line 19 to page 13, line 2 with the following amended paragraph:

-- The multi-port memory controller 308 has several port interfaces. Port 1 interface ~~307~~ 305 provides devices on the CPU bus 304 access to the RAM 311. Port 2 interface 307 provides the POR sequencer 300 access to the RAM 311. The data path multiplexers 309 route the read and write requests from the POR sequencer 300 and the CPU bus 304 to the RAM 311. The controller 310 manages how the data path multiplexers 309 behave in response to the read and write requests received from the POR sequencer 300 and CPU bus 304.--

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM.

2. (previously presented) The apparatus of claim 1,

wherein the one or more processors reads and executes firmware;

wherein the reset controller maintains reset states of all devices of the embedded system;

wherein the storage device controller provides an interface to a storage device;

wherein the one or more direct memory access controllers initiates and tracks data transfers;

wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ROM controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

3. (currently amended) The apparatus of claim 1,

wherein the descriptor comprises a POR sequencer descriptor, and

wherein the POR sequencer uses [[a]] the POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

4. (previously presented) The apparatus of claim 3, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

5. (previously presented) The apparatus of claim 4, wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

6. (previously presented) The apparatus of claim 1, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

7. (previously presented) The apparatus of claim 1, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

8. (previously presented) The apparatus of claim 1, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

9. (previously presented) The apparatus of claim 1, further comprising: a CPU bus in the embedded system.

10-20. (cancelled)

21. (new) An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and a power-on reset (POR) sequencer, wherein the POR sequencer uses a POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

22. (new) The apparatus of claim 21,

wherein the one or more processors reads and executes firmware;

wherein the reset controller maintains reset states of all devices of the embedded system;

wherein the storage device controller provides an interface to a storage device;

wherein the one or more direct memory access controllers initiates and tracks data transfers;

wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ROM controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

23. (new) The apparatus of claim 21, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

24. (new) The apparatus of claim 23, wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

25. (new) The apparatus of claim 21, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

26. (new) The apparatus of claim 21, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

27. (new) The apparatus of claim 21, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

28. (new) The apparatus of claim 21, further comprising: a CPU bus in the embedded system.

REMARKS/ARGUMENTS

The specification is being amended to correct various minor clerical errors. No new matter is being added by virtue of the amendments to the specification. Applicant respectfully requests for the approval of these amendments.

Various claims are being amended as shown above. The amendments to the claims are being presented for enhancing a clarification of the recited elements and are not necessarily intended to limit the claimed invention.

Non-elected claims 10-20 were previously cancelled.

Claim rejections - 35 USC 102

Claims 1-2, and 6-9

Claims 1-2 and 6-9 are rejected under pre-AIA 35 U.S.C. 102(a) as allegedly being anticipated by U.S. Patent No. 7,676,640 to Chow et al. (hereinafter "Chow").

Applicant respectfully disagrees with this rejection, but to expedite an allowance of the claims, Applicant amends independent claim 1 herein to recite: a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM.

Support for the amendment in claim 1 is found in the substitute specification of the filed application in, for example, Figures 2, 5, 6, and 7 and accompanying text; page 5, lines 9 through 10; page 5, line 16 through page 6, line 2; page 6, line 17 through page 7, line 2; page 10, line 22 through page 11, line 3; and page 11, lines 7 through 8.

The Office avers that column 11 of Chow discloses a power-on reset (POR) sequencer in column 11. However, the Office does not identify a POR sequencer in column 11 and also does not identify a POR sequencer in the drawings. Therefore, Chow does not disclose "a power-on reset (POR) sequencer" as required in claim 1. Additionally, Chow does not disclose any element that can be equated to "a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM" as required in claim 1. Additionally, nowhere in Chow is even the term "POR sequencer" or "power-on reset sequencer" even used. Therefore, Chow does not disclose and does not teach the POR sequencer of claim 1. Based on at least the foregoing reasons, Chow does not disclose and does not teach all the limitations in claim 1.

Since Chow does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by Chow. Claim 1 is otherwise allowable.

Claims 2 and 6-9 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-2 and 6-9 is respectfully requested.

Applicant thanks the Examiner for identifying claims 3-5 as having allowable subject matter.

New claims 21-28

New claim 21 is being added and incorporates the limitations recited in claim 1 and claim 3. New claims 22, 23, 24, 25, 26, 27, and 28 are also being added and incorporate the limitations recited in claims 2, 4, 5, 6, 7, 8, and 9, respectively. Accordingly, claims 21 through 28 are in condition for allowance.

Favorable action is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Conclusion

The pending claims herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: 02 June 2016

Respectfully submitted,

/Arnold de Guzman/
Arnold de Guzman
Attorney for Applicant(s)
Reg. No. 39,955

Please send correspondence to:
Customer No. 16428

CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	02 June 2016
Express Mail Mailing Number (optional):			

Electronic Acknowledgement Receipt	
EFS ID:	25957094
Application Number:	14217365
International Application Number:	
Confirmation Number:	8249
Title of Invention:	Embedded System Boot from a Storage Device
First Named Inventor/Applicant Name:	Alvin Anonuevo Manlapat
Customer Number:	16428
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.018
Receipt Date:	02-JUN-2016
Filing Date:	17-MAR-2014
Time Stamp:	20:21:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	6005_018_response.pdf	48182 5c7c8380b54ccf6c17b68e8c40f1953fb303f057	no	12

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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NOTICE OF ALLOWANCE AND FEE(S) DUE

16428 7590 10/18/2016
BiTMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT

PAPER NUMBER

2116

DATE MAILED: 10/18/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249
TITLE OF INVENTION: Embedded System Boot from a Storage Device				

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	01/18/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

16428 7590 10/18/2016
BitMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249

TITLE OF INVENTION: Embedded System Boot from a Storage Device

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	01/18/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
ELAMIN, ABDELMONIEM I	2116	713-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

Notice of Allowability	Application No. 14/217,365	Applicant(s) MANLAPAT ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2116	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 06/02/2016.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-9 and 21-28. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>See Continuation Sheet</u> 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
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/ABDELMONIEM ELAMIN/ Primary Examiner, Art Unit 2116	
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Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 03/08/16, 03/23/16, 06/12/2016, 06/17/16, 07/03/16, 08/22/16.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 8249
Alvin Anonuevo Manlapat	)
	) Examiner:
	) Abdelmoniem I. Elamin
Serial No.: 14/217,365	) Telephone No.: 571.272.3674
	)
Filing Date:	) Art Unit: 2116
March 17, 2014	)
	) Atty. Docket No.: 6005.018
Title: Embedded System Boot	)
From A Storage Device	) Customer No.: 16428
	)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**AMENDMENT AND
REQUEST FOR CONTINUED EXAMINATION**

Please amend this application as shown below. A
Request For Continued Examination is being filed herewith.

Amendments to the Claims are reflected in the listing of
claims which begins on page 2 of this paper.

Remarks And Arguments begin on page 7 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access (DMA) controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and

a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM.

2. (currently amended) The apparatus of claim 1,

wherein the one or more processors reads and executes firmware;

wherein the reset controller maintains reset states of all devices of the embedded system;

wherein the storage device controller provides an interface to a storage device;

wherein the one or more direct memory access controllers initiates and tracks data transfers;

wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ~~ROM~~ nonvolatile memory controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

3. (previously presented) The apparatus of claim 1,

wherein the descriptor comprises a POR sequencer descriptor, and

wherein the POR sequencer uses the POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

4. (previously presented) The apparatus of claim 3, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

5. (previously presented) The apparatus of claim 4, wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

6. (previously presented) The apparatus of claim 1, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

7. (previously presented) The apparatus of claim 1, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

8. (previously presented) The apparatus of claim 1, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

9. (currently amended) The apparatus of claim 1, further comprising: a CPU (Central Processing Unit) bus in the embedded system.

10-20. (cancelled)

21. (currently amended) An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access (DMA) controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and

a power-on reset (POR) sequencer, wherein the POR sequencer uses a POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

22. (currently amended) The apparatus of claim 21,

wherein the one or more processors reads and executes firmware;

wherein the reset controller maintains reset states of all devices of the embedded system;

wherein the storage device controller provides an interface to a storage device;

wherein the one or more direct memory access controllers initiates and tracks data transfers;

wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ~~ROM~~ nonvolatile memory controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

23. (previously presented) The apparatus of claim 21, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

24. (previously presented) The apparatus of claim 23, wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

25. (previously presented) The apparatus of claim 21, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

26. (previously presented) The apparatus of claim 21, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

27. (previously presented) The apparatus of claim 21, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

28. (currently amended) The apparatus of claim 21, further comprising: a CPU (Central Processing Unit) bus in the embedded system.

REMARKS AND ARGUMENTS

Various claims are being amended as shown above. The amendments to the claims are being presented for enhancing a clarification of the recited elements and are not necessarily intended to limit the claimed invention.

No new matter is being added by virtue of the amendments to the claims.

Favorable action is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Conclusion

The pending claims herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: 18 January 2017

Respectfully submitted,

/Arnold de Guzman/
Arnold de Guzman
Attorney for Applicant(s)
Reg. No. 39,955

Please send correspondence to:
Customer No. 16428

CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	18 January 2017
Express Mail Mailing Number (optional):			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

16428 7590 02/10/2017
BiTMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT PAPER NUMBER

2115

DATE MAILED: 02/10/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249

TITLE OF INVENTION: Embedded System Boot from a Storage Device

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	05/10/2017

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HOW TO REPLY TO THIS NOTICE:

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BitMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
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Certificate of Mailing or Transmission

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249

TITLE OF INVENTION: Embedded System Boot from a Storage Device

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	05/10/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
ELAMIN, ABDELMONIEM I	2115	713-001000

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- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
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- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249
16428	7590	02/10/2017	EXAMINER	
BiTMICRO Networks, Inc. ATTN: Patent Department 47929 Fremont Blvd Fremont, CA 94538			ELAMIN, ABDELMONIEM I	
			ART UNIT	PAPER NUMBER
			2115	
DATE MAILED: 02/10/2017				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No. 14/217,365	Applicant(s) MANLAPAT ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2115	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to RCE filed on 01/18/2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-9 and 21-28. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>01/18/2017</u>	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/ABDELMONIEM ELAMIN/ Primary Examiner, Art Unit 2115	
---	--

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 8249
Alvin Anonuevo Manlapat	)
	) Examiner:
	) Abdelmoniem I. Elamin
Serial No.: 14/217,365	) Telephone No.: 571.272.3674
	)
Filing Date:	) Art Unit: 2115
March 17, 2014	)
	) Atty. Docket No.: 6005.018
Title: Embedded System Boot	)
From A Storage Device	) Customer No.: 16428
	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL LETTER

Dear Sir:

Applicant respectfully requests the Office to consider the following Information Disclosure Statement being filed herewith.

Filing of Information Disclosure Statement Under 37 C.F.R. 1.56, 37 C.F.R. 1.97, and 37 C.F.R. 1.98

Pursuant to the provisions of 37 CFR 1.56, 37 CFR 1.97, and 37 C.F.R. 1.98, enclosed herewith is form PTO/SB/08 listing references which may be material to the examination of this application, and with respect to which there may be a duty to disclose. The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of

In re Manlapat et al.
U.S. Appl. No. 14/217,365

1

references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

A copy of each listed reference is enclosed herewith, unless no such copy is required pursuant to 37 CFR 1.98(d).

Pursuant to 37 CFR 1.97, this Information Disclosure Statement is being submitted under the following section: 37 CFR 1.97(b)(4). An information disclosure statement shall be considered by the Office if filed by the applicant within any one of the following time periods: Before the mailing of a first office action after the filing of a request for continued examination under section 1.114.

Consideration of the listed references and favorable action are respectfully solicited.

Conclusion

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: 10 May 2017

Respectfully submitted,

/Arnold de Guzman/
 Arnold de Guzman
 Attorney for Applicant(s)
 Reg. No. 39,955

Please send correspondence to:
 Customer No. 16428

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Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	10 May 2017
Express Mail Mailing Number (optional):			



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249
16428	7590	08/23/2017	EXAMINER	
BiTMICRO Networks, Inc. ATTN: Patent Department 47929 Fremont Blvd Fremont, CA 94538			ELAMIN, ABDELMONIEM I	
			ART UNIT	PAPER NUMBER
			2115	
			NOTIFICATION DATE	DELIVERY MODE
			08/23/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

arnold@dcpatentlaw.com
bit-ip@bitmicro.com
mariedel.nolasco@bitmicro.com

Corrected Notice of Allowability	Application No. 14/217,365	Applicant(s) MANLAPAT ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2115	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

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☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-6,8,9 and 21-28. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
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Certified copies:
 a) ☐ All b) ☐ Some *c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
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Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____ .	5. ☒ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
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1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Arnold de Guzman (Reg. #39,955) on August 17, 2017.

The application has been amended as follows:

In the Claims

Please cancel claim 7.

Please amend claim 1 as follows:

1. An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access (DMA) controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and

a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM,

wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

Allowable Subject Matter

3. Claims 1-6, 8-9, 21-28 are allowed.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or fairly suggest the following:

a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

For these reasons, claim 1 is deemed to be allowable over the prior art of record and claims 2-6, 8-19 are allowed by dependency.

Also, the prior art of record does not teach or fairly suggest the following:

a power-on reset (POR) sequencer wherein the POR sequencer uses a POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

For these reasons, claim 21 is deemed to be allowable over the prior art of record and claims 22-28 are allowed by dependency.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDELMONIEM ELAMIN whose telephone number is (571)272-3674. The examiner can normally be reached on MON - FRI 10:00 AM - 6:30 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ABDELMONIEM ELAMIN/
Primary Examiner, Art Unit 2115

August 18, 2017

Notice of References Cited	Application/Control No. 14/217,365	Applicant(s)/Patent Under Reexamination MANLAPAT ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2007/0180223 A1	08-2007	Tanaka; Akira	G06F15/177	713/2
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 8249
Alvin Anonuevo Manlapat	)
	) Examiner:
	) Abdelmoniem I. Elamin
Serial No.: 14/217,365	) Telephone No.: 571.272.3674
	)
Filing Date:	) Art Unit: 2115
March 17, 2014	)
	) Atty. Docket No.: 6005.018
Title: Embedded System Boot	)
From A Storage Device	) Customer No.: 16428
	)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Dear Sir:

Please amend the above-identified patent application as shown below. A request for continued examination is being filed herewith.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Amendments to the Claims:

In re Manlapat et al.
U.S. Appl. No. 14/217,365

1

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) An apparatus, comprising:
an embedded system comprising one or more processors,
a reset controller, a storage device controller, one or
more direct memory access DMA controllers, a random access
memory (RAM) and a memory controller, a nonvolatile memory
and a nonvolatile memory controller, a debug interface, and
a power-on reset (POR) sequencer configured to detect,
in the nonvolatile memory, a descriptor used in a boot
process and configured to copy the descriptor from the
nonvolatile memory to the RAM,
wherein the POR sequencer facilitates a boot process
and verifies an integrity of loaded data and code in the
RAM.
2. (previously presented) The apparatus of claim 1,
wherein the one or more processors reads and executes
firmware;
wherein the reset controller maintains reset states of
all devices of the embedded system;
wherein the storage device controller provides an
interface to a storage device;
wherein the one or more direct memory access
controllers initiates and tracks data transfers;
wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ROM controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

3. (previously presented) The apparatus of claim 1,

wherein the descriptor comprises a POR sequencer descriptor, and

wherein the POR sequencer uses the POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

4. (previously presented) The apparatus of claim 3, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

5. (previously presented) The apparatus of claim 4, wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

6. (previously presented) The apparatus of claim 1, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

7. (cancelled)

8. (previously presented) The apparatus of claim 1, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

9. (previously presented) The apparatus of claim 1, further comprising: a CPU bus in the embedded system.

10-20. (cancelled)

21. (previously presented) An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and a power-on reset (POR) sequencer, wherein the POR sequencer uses a POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

22. (previously presented) The apparatus of claim 21,

wherein the one or more processors reads and executes firmware;

wherein the reset controller maintains reset states of all devices of the embedded system;

wherein the storage device controller provides an interface to a storage device;

wherein the one or more direct memory access controllers initiates and tracks data transfers;

wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ROM controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

23. (previously presented) The apparatus of claim 21, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

24. (previously presented) The apparatus of claim 23, wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

25. (previously presented) The apparatus of claim 21, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

26. (previously presented) The apparatus of claim 21, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

27. (previously presented) The apparatus of claim 21, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

28. (previously presented) The apparatus of claim 21, further comprising: a CPU bus in the embedded system.

29. (new) An article of manufacture, comprising:

 a non-transitory computer-readable medium having stored thereon instructions to permit an apparatus to perform a method comprising:

 detecting in a nonvolatile memory in the apparatus, by a power-on reset (POR) sequencer, a descriptor used in a boot process and copying, by the POR sequencer, the descriptor from the nonvolatile memory to a random access memory (RAM), and

 facilitating, by the POR sequencer, a boot process and verifying, by the POR sequencer, an integrity of loaded data and code in the RAM.

30. (new) The article of manufacture of claim 29,

 wherein the apparatus comprises an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access

DMA controllers, the random access memory (RAM) and a memory controller, the nonvolatile memory and a nonvolatile memory controller, a debug interface, and the POR sequencer;

wherein the one or more processors reads and executes firmware;

wherein the reset controller maintains reset states of all devices of the embedded system;

wherein the storage device controller provides an interface to a storage device;

wherein the one or more direct memory access controllers initiates and tracks data transfers;

wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ROM controller is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

31. (new) The article of manufacture of claim 29,

wherein the descriptor comprises a POR sequencer descriptor, and

wherein the POR sequencer uses the POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory.

32. (new) The article of manufacture of claim 31, wherein the POR sequencer descriptor includes register information and DMA controller descriptors.

REMARKS/ARGUMENTS

Various claims are being amended as shown above. The amendments to the claims are being presented for enhancing a clarification of the recited elements and are not necessarily intended to limit the claimed invention.

New claims 29-32 are being added and are supported in the filed application.

Non-elected claims 10-20 and claim 7 were previously cancelled. Claims 10 through 20 and 7 in this patent application are canceled without prejudice, waiver, or surrender of the subject matter contained therein. See, e.g., *In re Tanaka*, No. 10-1262, (Fed. Cir. 2011); *In re Mostafazadeh*, No. 10-1260 (Fed. Cir. 2011).

Favorable action is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Conclusion

The pending claims herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: October 23, 2017

Respectfully submitted,

/Arnold de Guzman/
Arnold de Guzman
Attorney for Applicant(s)
Reg. No. 39,955

Please send correspondence to:
Customer No. 16428

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Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	October 23, 2017
Express Mail Mailing Number (optional):			

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 8249
Alvin Anonuevo Manlapat	)
	) Examiner:
	) Abdelmoniem I. Elamin
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In re Manlapat et al.
U.S. Appl. No. 14/217,365

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Date: October 23, 2017

Respectfully submitted,

/Arnold de Guzman/
 Arnold de Guzman
 Attorney for Applicant(s)
 Reg. No. 39,955

Please send correspondence to:
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Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	October 23, 2017
Express Mail Mailing Number (optional):			



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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16428	7590	11/01/2017	EXAMINER	
BiTMICRO Networks, Inc. ATTN: Patent Department 47929 Fremont Blvd Fremont, CA 94538			ELAMIN, ABDELMONIEM I	
			ART UNIT	PAPER NUMBER
			2115	
			NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

arnold@dcpatentlaw.com
bit-ip@bitmicro.com
mariedel.nolasco@bitmicro.com

Office Action Summary	Application No. 14/217,365	Applicant(s) MANLAPAT ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2115	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 10/23/2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) 1-9 and 21-32 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☒ Claim(s) 1-9 and 21-32 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some** c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 10/23/2017

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

4) ☐ Other: _____

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

3. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

4. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).
5. Claims 1-6, 8-9, 21-32 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 14/217,399. Although the conflicting claims are not identical, they are not patentably distinct from each other because they recite means or steps that are substantially the same and that would have been obvious to one of ordinary skill in the art.
6. Claims 1-6, 8-9, 21-32, essentially repeat most of the features listed in claims 1-20 of copending Application No. 14/217,399.
7. The omission of an element with a corresponding loss of function is an obvious expedient. See *In re Karlson*, 136 USPQ 184 and *Ex parte Raina*, 168 USPQ 375.

Claim 1 of the Instant Application	Claims 1, 10 and 19 of 14/217,399
An embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access DMA controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded	An apparatus, comprising: <u>an embedded system</u> configured to release components of the embedded system from reset; wherein the embedded system comprises a <u>power-on reset (POR) sequencer configured to detect a POR sequencer descriptor in a nonvolatile memory, to copy the POR sequencer descriptor from the nonvolatile memory to a random access memory (RAM), to verify an integrity of the POR sequencer descriptor, and to detect any error in the POR sequencer descriptor; wherein the POR sequencer descriptor comprises information to initialize configuration registers of the embedded system, Direct Memory Access (DMA) descriptors used to fetch other POR</u>

data and code in the RAM	sequencer descriptor fragments, and a system firmware; wherein the POR sequencer comprises a bus master interface that manages data and control signals to and from a Central Processor Unit (CPU) bus, a memory controller port interface that manages control signals to and from the RAM, and a POR sequencer state machine that utilizes the
--------------------------	--

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-4, 6-7, 9, 21-23, 25-32 are rejected under 35 U.S.C. 103 as being unpatentable over Tanaka, Pub. No. US 2007/0180223 A1 in view of Holland et al, US. Pat. No. 7,921,237.

10. Claims 1, 6-7, 9, 25-26, 29, Tanaka teaches an embedded system comprising one or more processors [*CPU 10 and Sub-CPU 21 of Fig. 1*], a reset controller [*to detect reset events, see paragraphs 0078, 0087-0088*], a storage device controller [*inherent*], one or more direct memory access DMA controllers [*inherent*], a random access memory (RAM) and a memory controller [*subsystem memory 22*], a nonvolatile memory and a nonvolatile memory controller [*ROM 23*], a debug interface [*in order for development, the system inherently has a debug port for sending in the parameter values, see paragraph 0074*], and

a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory [*POR control program, see paragraphs 0067+*], a descriptor [*control values (script) stored in ROM*]

Art Unit: 2115

23] used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM [*POR control program with the control values (script) are stored in the ROM 23 and then copy to the subsystem RAM 22, see paragraphs 0067+*],

Tanaka fails to teach POR sequencer verifies an integrity of loaded data and code in the RAM.

Holland teaches a storage system includes a host computer coupled to a device to transfer a DMA descriptor between the host and the device. An integrity manager manages the integrity of the DMA descriptor between the host computer and the device. The integrity manager embeds a host-side DMA descriptor integrity value in the DMA descriptor and the device transfers the DMA descriptor to a device memory. The device generates a device-side DMA descriptor integrity value and compares it to the host-side DMA descriptor integrity value to determine if the descriptor is corrupted [*see abstract, col. 2, lines 6-16*].

It would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Tanaka to include POR sequencer verifies an integrity of loaded data and code in the RAM, because it helps determining whether the descriptor is corrupted or not [*see col. 2, lines 15-16*].

11. Claims 2, 22, 30, Tanaka teaches the one or more processors reads and executes firmware [*see paragraph 0015*]; wherein the reset controller maintains reset states of all devices of the embedded system [*The subsystem 2 recognizes the state of the main system from information recorded in the Mail Box 15. On the other hand, the main CPU 10 recognizes the state of the subsystem and gives event notification using the Mail Box 15, see paragraph, 0076.*]; wherein

Art Unit: 2115

the storage device controller provides an interface to a storage device [*inherent*]; wherein the one or more direct memory access controllers initiates and tracks data transfers [*typically direct memory access controller initiates and tracks data transfers*]; wherein the RAM is used to temporarily store firmware [*subsystem memory 22*]; wherein the memory controller provides an interface to the RAM; wherein the nonvolatile memory comprises a read only memory (ROM); wherein the nonvolatile memory controller is used to store data used by the POR sequencer in a boot process of the embedded system [*see ROM 23 and related disclosure*]; wherein the debug interface is used to pre-program the ROM and the storage device with data and code [*inherent*]; and wherein the POR sequencer controls the boot process of the embedded system [*see POR control program, paragraphs 0067+*].

12. Claims 3-4, 23, 31-32, Tanaka teaches the POR sequencer uses the POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory [*stored in subsystem ROM 23*].

13. Claims 9, 28, Tanaka teaches a CPU (Central Processing Unit) bus in the embedded system [*see Fig. 1*].

Allowable Subject Matter

14. Claims 5, 8, 24 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable:

- a. If the double patenting rejection is resolved; and
- b. If rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDELMONIEM ELAMIN whose telephone number is (571)272-3674. The examiner can normally be reached on MON - FRI 10:00 AM - 6:30 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ABDELMONIEM ELAMIN/
Primary Examiner, Art Unit 2115

October 28, 2017

Notice of References Cited	Application/Control No. 14/217,365	Applicant(s)/Patent Under Reexamination MANLAPAT ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2007/0180223 A1	08-2007	Tanaka; Akira	G06F9/4405	713/2
*	B	US-7,921,237 B1	04-2011	Holland; Thomas	G06F11/1004	710/22
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 8249
Alvin Anonuevo Manlapat	)
	) Examiner:
	) Abdelmoniem I. Elamin
Serial No.: 14/217,365	) Telephone No.: 571.272.3674
	)
Filing Date:	) Art Unit: 2115
March 17, 2014	)
	) Atty. Docket No.: 6005.018
Title: Embedded System Boot	)
From A Storage Device	) Customer No.: 16428
	)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO OFFICE ACTION
AND AMENDMENT**

Dear Sir:

The following is in response to the office action
dated on November 1, 2017.

Amendments to the Claims are reflected in the listing of
claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access (DMA) controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and

a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM,

wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM,

wherein the descriptor comprises a POR sequencer descriptor, and wherein the POR sequencer uses the POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory,

wherein the POR sequencer descriptor includes register information and DMA controller descriptors, and

wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

2. (currently amended) The apparatus of claim 1,
 wherein the one or more processors reads and executes
firmware;
 wherein the reset controller maintains reset states of
all devices of the embedded system;
 wherein the storage device controller provides an
interface to a storage device;
 wherein the one or more direct memory access
controllers initiates and tracks data transfers;
 wherein the RAM is used to temporarily store firmware;
 wherein the memory controller provides an interface to
the RAM;
 wherein the nonvolatile memory comprises a read only
memory (ROM);
 wherein the ROM ~~controller~~ is used to store data used
by the POR sequencer in a boot process of the embedded
system;
 wherein the debug interface is used to pre-program the
ROM and the storage device with data and code; and
 wherein the POR sequencer controls the boot process of
the embedded system.

3. (cancelled)

4. (cancelled)

5. (cancelled)

6. (previously presented) The apparatus of claim 1, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

7. (cancelled)

8. (previously presented) The apparatus of claim 1, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

9. (previously presented) The apparatus of claim 1, further comprising: a CPU bus in the embedded system.

10-20. (cancelled)

21. (currently amended) An apparatus, comprising:

an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access (DMA) controllers, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and

a power-on reset (POR) sequencer, wherein the POR sequencer uses a POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory,

wherein the POR sequencer descriptor includes register information and DMA controller descriptors, and

wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

22. (currently amended) The apparatus of claim 21,
 wherein the one or more processors reads and executes firmware;
 wherein the reset controller maintains reset states of all devices of the embedded system;
 wherein the storage device controller provides an interface to a storage device;
 wherein the one or more direct memory access controllers initiates and tracks data transfers;
 wherein the RAM is used to temporarily store firmware;
 wherein the memory controller provides an interface to the RAM;
 wherein the nonvolatile memory comprises a read only memory (ROM);
 wherein the ROM ~~controller~~ is used to store data used by the POR sequencer in a boot process of the embedded system;
 wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and
 wherein the POR sequencer controls the boot process of the embedded system.

23. (cancelled)

24. (cancelled)

25. (previously presented) The apparatus of claim 21, wherein the POR sequencer loads DMA descriptors to the DMA controllers.

26. (previously presented) The apparatus of claim 21, wherein the POR sequencer facilitates a boot process and verifies an integrity of loaded data and code in the RAM.

27. (previously presented) The apparatus of claim 21, wherein the POR sequencer processes a linked-list of data structures in order to increase an amount of register information and DMA descriptors that are processed by the POR sequencer.

28. (previously presented) The apparatus of claim 21, further comprising: a CPU bus in the embedded system.

29. (currently amended) An article of manufacture, comprising:

a non-transitory computer-readable medium having stored thereon instructions to permit an apparatus to perform a method comprising:

detecting in a nonvolatile memory in the apparatus, by a power-on reset (POR) sequencer, a descriptor used in a boot process and copying, by the POR sequencer, the descriptor from the nonvolatile memory to a random access memory (RAM), and

facilitating, by the POR sequencer, a boot process and verifying, by the POR sequencer, an integrity of loaded data and code in the RAM,

wherein the descriptor comprises a POR sequencer descriptor, and wherein the POR sequencer uses the POR sequencer descriptor which is a preassembled descriptor that is stored in the nonvolatile memory,

wherein the POR sequencer descriptor includes register information and DMA controller descriptors, and

wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system.

30. (currently amended) The article of manufacture of claim 29,

wherein the apparatus comprises an embedded system comprising one or more processors, a reset controller, a storage device controller, one or more direct memory access (DMA) controllers, the random access memory (RAM) and a memory controller, the nonvolatile memory and a nonvolatile memory controller, a debug interface, and the POR sequencer;

wherein the one or more processors reads and executes firmware;

wherein the reset controller maintains reset states of all devices of the embedded system;

wherein the storage device controller provides an interface to a storage device;

wherein the one or more direct memory access controllers initiates and tracks data transfers;

wherein the RAM is used to temporarily store firmware;

wherein the memory controller provides an interface to the RAM;

wherein the nonvolatile memory comprises a read only memory (ROM);

wherein the ROM ~~controller~~ is used to store data used by the POR sequencer in a boot process of the embedded system;

wherein the debug interface is used to pre-program the ROM and the storage device with data and code; and

wherein the POR sequencer controls the boot process of the embedded system.

31. (cancelled)

32. (cancelled)

REMARKS/ARGUMENTS

Various claims are being amended as shown above. The amendments to the claims are being presented for enhancing a clarification of the recited elements and are not necessarily intended to limit the claimed invention.

Claim rejections - Double Patenting

Claims 1-6, 8-9, and 21-32

Claims 1-6, 8-9, and 21-32 are provisionally rejected on the ground of non-statutory obviousness-type double patenting as allegedly being unpatentable over claims 1-20 of copending Patent Application No. 14/217,399.

While Applicant respectfully disagrees with this rejection, Applicant defers response to this non-statutory double patenting rejection until the claims are in condition for allowance. Applicant respectfully submits that no further action is required to be taken at this time. The withdrawal of the rejection to claims 1-6, 8-9, and 21-32 is respectfully requested.

Claim rejections - 35 USC § 103

Claims 1-4, 6-7, 9, 21-23, and 25-32

Claims 1-4, 6-7, 9, 21-23, and 25-32 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent Application Publication No. 2007/0180223 to Tanaka in view of U.S. Patent No. 7,921,237 to Holland et al. (hereinafter referred to as "Holland").

Although Applicant respectfully disagrees with this rejection, in order to expedite the allowance of the

claims, Applicant amends independent claims 1 and 21 herein to recite allowable subject matter in claims 5 and 24, respectively, and to recite any intervening claims. Claim 29 is also being amended to recite allowable subject matter as similarly recited in amended claim 1. Accordingly, claims 1, 21, and 29 are each patentable over Tanaka and Holland, considered individually or in combination. Claims 1, 21, and 29 are each otherwise allowable.

Claims 2, 6, and 9 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1. Claims 3-5 are being cancelled.

Claims 22 and 25-28 depend from allowable claim 21; as such, they are also allowable for at least the same reasons as claim 21. Claims 23-24 are being cancelled.

Claim 30 depends from allowable claim 29; as such, claim 30 also allowable for at least the same reasons as claim 29. Claims 31-32 are being cancelled.

The withdrawal of the rejections to claims 1, 2, 6, 9, 22, 25-28, and 29-30 is respectfully requested.

Non-elected claims 7 and 10-20 were previously cancelled. As also noted above, additional claims in this patent application are canceled without prejudice, waiver, or surrender of the subject matter contained therein. See, e.g., *In re Tanaka*, No. 10-1262, (Fed. Cir. 2011); *In re Mostafazadeh*, No. 10-1260 (Fed. Cir. 2011).

Favorable action is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Conclusion

The pending claims herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: February 1, 2018

Respectfully submitted,

/Arnold de Guzman/
Arnold de Guzman
Attorney for Applicant(s)
Reg. No. 39,955

Please send correspondence to:
Customer No. 16428

CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	February 1, 2018
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NOTICE OF ALLOWANCE AND FEE(S) DUE

16428 7590 06/14/2018
BiTMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT

PAPER NUMBER

2115

DATE MAILED: 06/14/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249
TITLE OF INVENTION: EMBEDDED SYSTEM BOOT FROM A STORAGE DEVICE				

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0	\$0	\$1000	09/14/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

16428 7590 06/14/2018
BitMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249

TITLE OF INVENTION: EMBEDDED SYSTEM BOOT FROM A STORAGE DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0	\$0	\$1000	09/14/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
ELAMIN, ABDELMONIEM I	2115	713-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	03/17/2014	Alvin Anonuevo Manlapat	6005.018	8249
16428	7590	06/14/2018	EXAMINER	
BiTMICRO Networks, Inc. ATTN: Patent Department 47929 Fremont Blvd Fremont, CA 94538			ELAMIN, ABDELMONIEM I	
			ART UNIT	PAPER NUMBER
			2115	
DATE MAILED: 06/14/2018				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

<i>Notice Requiring Inventor's Oath or Declaration</i>	Application No. 14/217,365	Applicant(s) Alvin Anonuevo Manlapat	
	Examiner ELAMIN, ABDELMONIEM I	Art Unit 2115	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) **MUST** be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Alvin Anonuevo Manlapat** and **Ian Victor Pasion Beleno**.

Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/217,365	Applicant(s) MANLAPAT ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2115	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 02/012018.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1,2,6,8,9,21,22 and 25-30. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____ . 5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.	
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/ABDELMONIEM ELAMIN/ Primary Examiner, Art Unit 2115	
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/217,365	11/06/2018	10120694	6005.018	8249

16428 7590 10/17/2018
BiTMICRO Networks, Inc.
ATTN: Patent Department
47929 Fremont Blvd
Fremont, CA 94538

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 63 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Alvin Anonuevo Manlapat, City of San Fernando, PHILIPPINES;
BiTMICRO Networks, Inc., Fremont, CA;
Ian Victor Pasion Beleno, Quezon city, PHILIPPINES;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.