UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	03/07/2017	9590582	5750/0265PUS1	1455

60601 7590 02/15/2017

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 7 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hsiao-Tsung YEN, Hsinchu, TAIWAN;
REALTEK SEMICONDUCTOR CORP., Hsinchu, TAIWAN;
Yuh-Sheng JEAN, Hsinchu, TAIWAN;
Ta-Hsun YEH, Hsinchu, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60601 7590 11/22/2016
Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, RAKESH BHASKARBHAI	2842	333-185000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Muncy, Geissler, Olds & Lowe, P.C.
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: REALTEK SEMICONDUCTOR CORP.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): HSINCHU, TAIWAN

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☒ Payment by credit card. ~~Form PTO-2038 is attached~~.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-3828 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date January 20, 2017

Typed or printed name Joe McKinney Muncy Registration No. 32,334

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	14338904
Filing Date:	23-Jul-2014
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Filer:	Joe McKinney Muncy/Tammy Jordan
Attorney Docket Number:	5750/0265PUS1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	28124369
Application Number:	14338904
International Application Number:	
Confirmation Number:	1455
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Customer Number:	60601
Filer:	Joe McKinney Muncy/Tammy Jordan
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	5750/0265PUS1
Receipt Date:	20-JAN-2017
Filing Date:	23-JUL-2014
Time Stamp:	16:41:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	012317INTEFSW16422500
Deposit Account	503828
Authorized User	Tammy Jordan
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2017-01-20_Issue-Fee-Transmittal.pdf	229006 4fca249aa77ded31e2883d71a4fa743504a540ff	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30599 5e74dd880de2fb266db2d8df0644381398fe3f05	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	259605		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60601 7590 11/22/2016
Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER
PATEL, RAKESH BHASKARBHAI

ART UNIT	PAPER NUMBER
2842	

DATE MAILED: 11/22/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/22/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60601 7590 11/22/2016
Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, RAKESH BHASKARBHAI	2842	333-185000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1002, p. 8 of 466

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

60601 7590 11/22/2016

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER	
PATEL, RAKESH BHASKARBHAI	
ART UNIT	PAPER NUMBER
2842	

DATE MAILED: 11/22/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/338,904	Applicant(s) YEN ET AL.	
	Examiner RAKESH PATEL	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE amendment dated 10/28/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-3 and 6-11*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *11/16/2016* .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/STEPHEN E. JONES/ Primary Examiner, Art Unit 2842	/R. P./ Examiner, Art Unit 2842

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with Scott Tulino, Registration No. 48,317 on November 16, 2016.

The following changes have been made to claim 6:

On lines 4-6 of claim 6, "wherein the capacitor component further comprises: a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction," has been deleted.

On lines 7-11 of claim 6, "; and a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments" has been deleted.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: As per claims 1 and 11, the closest prior art Jing et al. US Patent 9,270,247 (of record) discloses in Fig. 7 a semiconductor device with an LC resonant circuit comprising all of the limitations recited therein **EXCEPT** "wherein the plurality of connecting segments of the capacitor component are respectively overlapped with **the two extension-conductor segments**". Jing et al. discloses an inductor component 705 including legs or "extension-conductor segments" 715 and 720. The inductor 705 is connected to TWO separate finger capacitors or "capacitor components" 725 and 730. Each of the capacitor components overlaps with only a single one of the "extension-conductor segments" in a vertical direction and not both (i.e. "the two extension-conductor segments") as recited within the claims. Further, each of the finger capacitors or "capacitor components" 725 and 730 is its

own separate capacitor structure separated by switches 735 as shown in Fig. 7, and thus elements 725 and 730 together cannot be interpreted as "a capacitor component".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAKESH PATEL whose telephone number is (571)272-0961. The examiner can normally be reached on Monday-Friday 7:30 am-5:00 pm ET, ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. P./
Examiner, Art Unit 2842

/STEPHEN E. JONES/
Primary Examiner, Art Unit 2842

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	14/338,904	YEN ET AL.	
	Examiner	Art Unit	
	RAKESH PATEL	2842	

All participants (applicant, applicant's representative, PTO personnel):

(1) *RAKESH PATEL*. (3)_____.

(2) *Scott Tulino, Registration No. 48,317*. (4)_____.

Date of Interview: *16 November 2016*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *6*.

Identification of prior art discussed: _____.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

An agreement was reached to delete repetitive limitations recited within claim 6 which are redundant to limitations recited within amended claim 1. See Examiner's Amendment for a detailed description of the changes.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/RAKESH PATEL/ Examiner, Art Unit 2842	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

CPC- SEARCHED		
Symbol	Date	Examiner
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	9/18/2015	RP
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	3/7/2016	RP
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	7/12/2016	RP
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013, H01L23/5223, H01L23/5227	11/15/2016	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
333	175,177,185	9/18/2015	RP
336	200	9/18/2015	RP
333	175,177,185	3/7/2016	RP
336	200	3/7/2016	RP
333	175,177,185	7/12/2016	RP
336	200	7/12/2016	RP
333	175,177,185	11/15/2016	RP
336	200	11/15/2016	RP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Text Search	9/18/2015	RP
EAST Updated Text Search	3/7/2016	RP
Consulted Examiner, Gerald Stevens	3/7/2016	RP
Inventor Search	3/7/2016	RP
EAST Updated Text Search	7/12/2016	RP
Consulted Examiner, Gerald Stevens	7/12/2016	RP
EAST Updated Text Search	11/15/2016	RP

/R.P./ Examiner.Art Unit 2842	

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Inventor Search	11/15/2016	RP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
PGPUB Search and USPAT Search		11/15/2016	RP

/R.P./ Examiner.Art Unit 2842	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L26	1	L24 and (semiconductor and resona$4 and capacitor and inductor).clm.	US-PGPUB; USPAT; USOCR	OR	ON	2016/11/15 16:26
L25	0	L24 and (semiconductor and resona$4 and capacitor and inductor).clm.	USPAT; USOCR	OR	ON	2016/11/15 16:26
L24	210	(hsiao$tsung with yen) or (yuh$sheng with jean) or (ta$hsun with yeh)	US-PGPUB; USPAT; USOCR	OR	ON	2016/11/15 16:26
L23	0	L17 and L22	US-PGPUB; USPAT	OR	ON	2016/11/15 16:26
L22	1	(14/338904).APP.	US-PGPUB; USPAT	OR	OFF	2016/11/15 16:25
L21	16	L17 and (semiconductor and capacitor).clm.	USPAT; USOCR	OR	ON	2016/11/15 16:25
L20	48	L17 and (semiconductor).clm.	USPAT; USOCR	OR	ON	2016/11/15 16:25
L19	0	L17 and (semiconductor and resona$4 and capacitor and inductor).clm.	USPAT; USOCR	OR	ON	2016/11/15 16:25
L18	0	L17 and (LC and resona$4 and capacitor and inductor).clm.	USPAT; USOCR	OR	ON	2016/11/15 16:25
L17	86	(hsiao$tsung with yen) or (yuh$sheng with jean) or (ta$hsun with yeh)	USPAT; USOCR	OR	ON	2016/11/15 16:24
L16	274	(L7 or L8 or L9 or L10 or L11 or L12 or L13 or L14) and semiconductor and finger	USPAT; USOCR	OR	ON	2016/11/15 16:24
L15	220	(L7 or L8 or L9 or L10 or L11 or L12 or L13 or L14) and semiconductor and LC with resona$4	USPAT; USOCR	OR	ON	2016/11/15 16:24
L14	2453	(336/200).ccls.	USPAT; USOCR	OR	ON	2016/11/15 16:23
L13	2378	(333/175,177,185).ccls.	USPAT; USOCR	OR	ON	2016/11/15 16:23
L12	895	(H01F17/0013).cpc.	USPAT; USOCR	OR	ON	2016/11/15 16:23
L11	207	(H01F2027/2809).cpc.	USPAT; USOCR	OR	ON	2016/11/15 16:23
L10	787	(H01F27/2804).cpc.	USPAT; USOCR	OR	ON	2016/11/15 16:23
L9	1377	(H01L23/5227).cpc.	USPAT; USOCR	OR	ON	2016/11/15 16:23
L8	1463	(H01L23/5223).cpc.	USPAT; USOCR	OR	ON	2016/11/15 16:23
L7	836	(H03H7/0115).cpc.	USPAT; USOCR	OR	ON	2016/11/15 16:22
L6	1	(14/092241).APP.	USPAT;	OR	ON	2016/11/15

			USOCR			13:32
L5	1	("20150145615").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/15 11:06

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L28	21	(semiconductor and resona$4 and capacitor and inductor and lateral$3).clm.	US-PGPUB; USPAT	OR	ON	2016/11/15 16:27
L27	954	(semiconductor and resona$4 and capacitor and inductor).clm.	US-PGPUB; USPAT	OR	ON	2016/11/15 16:27

11/15/2016 4:30:00 PM
C:\Users\rpatel9\Documents\EAST\Workspaces\14338904.wsp

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1002, p. 18 of 466

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	**Art Unit**
	RAKESH PATEL	2842

CPC						
Symbol					**Type**	**Version**
H03H		7	/	0115	F	2013-01-01
H01L		23	/	66	I	2013-01-01
H01L		2223	/	6672	A	2013-01-01
H01L		23	/	5223	I	2013-01-01
H01L		23	/	5227	I	2013-01-01
H01L		28	/	10	A	2013-01-01
H01L		28	/	40	A	2013-01-01
H01L		2924	/	19011	A	2013-01-01
H01L		2924	/	19041	A	2013-01-01
H01L		2924	/	19042	A	2013-01-01
H01L		2924	/	0002	A	2013-01-01
			/			
			/			
			/			
			/			

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
H01L		2924	/	0002	A	1	1	2013-01-01
H01L		2924	/	00	A	1	2	2013-01-01

/RAKESH PATEL/ Examiner.Art Unit 2842 (Assistant Examiner)	11/15/2016 (Date)	**Total Claims Allowed:** 9	
/STEPHEN E JONES/ Primary Examiner.Art Unit 2842 (Primary Examiner)	11/16/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	**Art Unit**
	RAKESH PATEL	2842

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
333	185	H	0	3	H	7 / 01 (2006.0)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											
333	175											

/RAKESH PATEL/ Examiner.Art Unit 2842	11/15/2016	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	9	
/STEPHEN E JONES/ Primary Examiner.Art Unit 2842	11/16/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	**Art Unit**
	RAKESH PATEL	2842

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
	4														
	5														
6	6														
7	7														
8	8														
4	9														
5	10														
9	11														

/RAKESH PATEL/ Examiner.Art Unit 2842	11/15/2016	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	9	
/STEPHEN E JONES/ Primary Examiner.Art Unit 2842	11/16/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/338,904	Filing Date 07/23/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 10/28/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 9	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
RENEE HAWKINS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	14338904	Filing Date	2014-07-23	Docket Number (if applicable)	5750/0265PUS1	Art Unit	2842
First Named Inventor	Hsiao-Tsung YEN			Examiner Name	PATEL, RAKESH BHASKARBHAI		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☒ Other Request for non-entry of Amendment after final filed on 16 Sep 2016

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503828

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

X Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Joe McKinney Muncy/	Date (YYYY-MM-DD)	2016-10-28
Name	Joe McKinney Muncy	Registration Number	32334

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: YEN, Hsiao-Tsung Application No.: 14/338,904 Filed: 23 Jul 2014 Title: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT Attorney Docket No.: 5750/0265PUS1	Examiner: PATEL, Rakesh Bhaskarbhai Art Unit: 2842 Confirmation Number: 1455

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL UNDER 37 CFR 1.116

Dear Sir:

In response to the Final Office Action of 28 Jul 2016, and in view of the Request for Continued Examination being filed herewith, the following are provided:

Amendments to the Claims; and

Remarks.

Attachments: Request for Continued Examination

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,

wherein the capacitor component comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

2. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

3. (Original) The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

4. (Cancelled)

5. (Cancelled)

6. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a tap segment, electrically connected to the coil-conductor segment;

wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein one of the plurality of connecting segments is located below the tap segment and overlapped with the tap segment; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

7. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, wherein the coil-conductor segment has a pair of staggered parts, a second region is defined by outer sides of the pair of staggered parts, and the semiconductor device further comprises:

an electronic component, arranged corresponding to the second region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

8. (Original) The semiconductor device with an LC resonant circuit according to claim 7,

wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

9. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

10. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 9, wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment.

11. (New) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

REMARKS

Claims 1-3 and 6-11 are now present in this application.

Applicants request that the claim amendments filed on September 16, 2016 are not entered and the claims are instead herein amended. Claim 1 has been amended. Claim 11 has been added. Claims 4 and 5 have been cancelled without prejudice or disclaimer. Favorable consideration of the application, as amended, is respectfully requested.

Entry of Amendments

It is respectfully submitted that the foregoing amendments do not contain new matter. Specifically, claim 1 is amended to incorporate the features of original claims 4 and 5, and the features of original claims 1, 4 and 5 are combined to form new claim 11. As such, the Examiner is respectfully requested to enter the same.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication that claim 5 would be allowable if rewritten in independent form. Without conceding the appropriateness of the Examiner's rejection, claim 1 has been amended to include features from claims 4 and 5, and new claim 11 has been added to include the limitations of original claims 1, 4 and 5. Accordingly, claims 1 and 11 are now in condition for allowance. The pending dependent claims depend from allowable independent claims and are allowable for at least this reason.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

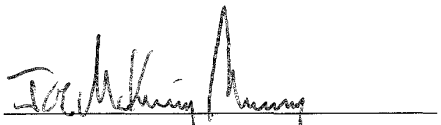
Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require action, it is respectfully requested that the Examiner telephone Joe McKinney Muncy, Applicants' Attorney, at 703.621.7140 so that such issues may be resolved as expeditiously as possible.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; in particular, extension of time fees.

Date: October 28, 2016

Respectfully submitted,

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road, Suite 310
Fairfax, VA 22033
Tel. 703.621.7140
mailroom@mg-ip.com



Joe McKinney Muncy
Attorney/Agent for Applicant(s)
Reg. No. 32334

Electronic Patent Application Fee Transmittal

Application Number:	14338904
Filing Date:	23-Jul-2014
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Filer:	Joe McKinney Muncy/Anita Paka
Attorney Docket Number:	5750/0265PUS1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1st Request	1801	1	1200	1200
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt	
EFS ID:	27358169
Application Number:	14338904
International Application Number:	
Confirmation Number:	1455
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Customer Number:	60601
Filer:	Joe McKinney Muncy/Anita Paka
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	5750/0265PUS1
Receipt Date:	28-OCT-2016
Filing Date:	23-JUL-2014
Time Stamp:	15:54:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	103116INTEFSW15551800
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	2016-10-28-RCE.pdf	697722 1fb538debeea2e6212e0618fba8b3f0db9dc03d1	no	3
Warnings:					
Information:					
2		2016-10-28-AmendmentAF-asfiled.pdf	552774 80fc53fca1bbab6710cd3997b9224051bfce610e	yes	6

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Response After Final Action	1	1
Claims	2	4
Applicant Arguments/Remarks Made in an Amendment	5	6

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30459 7b0a1aaa614c9a5b5fc980795dc53cbef5fb6dd1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1280955		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

60601 7590 09/30/2016

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER
PATEL, RAKESH BHASKARBHAI

ART UNIT	PAPER NUMBER
2842	

MAIL DATE	DELIVERY MODE
09/30/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	14/338,904	YEN ET AL.	
	Examiner	Art Unit	
	RAKESH PATEL	2842	

All participants (applicant, applicant's representative, PTO personnel):

(1) *RAKESH PATEL*. (3)_____.

(2) *Scott Tulino, Registration No. 48,317*. (4)_____.

Date of Interview: *26 September 2016*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Daley et al. (of record) and Jing et al. US 2015/0145615*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

The Examiner notified the Applicant that the amendment made to claim 1 (see Amended claims dated 9/16/2016) does not overcome the reference of record Daley et al. Further, a new search was conducted within the allotted time and the Examiner cites a new prior art that also reads on claim 1. Jing et al. discloses in Fig. 5 a semiconductor device with an LC circuit comprising the limitations recited within claim 1. The Examiner notified the Applicant that the amendment dated 9/16/2016 will not be entered. The Applicant acknowledged and stated that an RCE will most probably be submitted.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/RAKESH PATEL/ Examiner, Art Unit 2842	

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 14/338,904	**Applicant(s)** YEN ET AL.	
	Examiner RAKESH PATEL	**Art Unit** 2842	**AIA (First Inventor to File) Status** Yes

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 16 September 2016 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☒ Other: PTO-2323, PTO-413B dated 9/26/2016, and PTO-892 form.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: .
   Claim(s) objected to: 5.
   Claim(s) rejected: 1-4 and 6-10.
   Claim(s) withdrawn from consideration: .

/R. P./ Examiner, Art Unit 2842	/STEPHEN E. JONES/ Primary Examiner, Art Unit 2842

Continuation of 12. does NOT place the application in condition for allowance because: The amendment made to claim 1 does not overcome the prior art of record Daley et al. "Capacitor component" 16 has portions which are aligned with and not aligned with the "coil conductor" 50, 52 in a vertical direction, where the portion which substantially forms the capacitor does not vertically align with the "coil conductor". Further, the Examiner cites a new reference Jing et al. US 2015/0145615, where Fig. 6 therein discloses a semiconductor device comprising an LC resonant circuit including all of the limitations recited in claim 1.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	14/338,904	YEN ET AL.	
	Examiner	Art Unit	
	RAKESH PATEL	2842	

All participants (applicant, applicant's representative, PTO personnel):

(1) *RAKESH PATEL*. (3)_____.

(2) *Scott Tulino, Registration No. 48,317*. (4)_____.

Date of Interview: *26 September 2016*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Daley et al. (of record) and Jing et al. US 2015/0145615*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

The Examiner notified the Applicant that the amendment made to claim 1 (see Amended claims dated 9/16/2016) does not overcome the reference of record Daley et al. Further, a new search was conducted within the allotted time and the Examiner cites a new prior art that also reads on claim 1. Jing et al. discloses in Fig. 5 a semiconductor device with an LC circuit comprising the limitations recited within claim 1. The Examiner notified the Applicant that the amendment dated 9/16/2016 will not be entered. The Applicant acknowledged and stated that an RCE will most probably be submitted.

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Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/RAKESH PATEL/ Examiner, Art Unit 2842	

Notice of References Cited	Application/Control No. 14/338,904	Applicant(s)/Patent Under Reexamination YEN ET AL.	
	Examiner RAKESH PATEL	Art Unit 2842	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2015/0145615 A1	05-2015	Jing; Jing	H01L23/5227	333/174
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

DO NOT ENTER: /R.P./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: YEN, Hsiao-Tsung Application No.: 14/338,904 Filed: 23 Jul 2014 Title: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT Attorney Docket No.: 5750/0265PUS1	Examiner: PATEL, Rakesh Bhaskarbhai Art Unit: 2842 Confirmation Number: 1455

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL UNDER 37 CFR 1.116

Dear Sir:

In response to the Final Office Action of 28 Jul 2016, and in view of Request for Participation in the After Final Consideration Pilot Program being filed concurrently herewith, the following are provided:

Amendments to the Claims; and

Remarks.

AFCP 2.0 Decision	Application No.	Applicant(s)
	14/338,904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

This is in response to the After Final Consideration Pilot request filed 16 September 2016.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.

   ☐ Other:

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☐ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☒ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action. See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other:

   Examiner Note: Please attach an interview summary when necessary as described above.

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
5750/0265PUS1	14/338,904	07-23-2014
First Named Inventor:	**Title:**	
Hsiao-Tsung YEN	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:
   - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
   - The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
     - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
     - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
       - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
       - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
ROBERT F. GNUSE	09/16/2016
Name (Print/Typed) Joe McKinney Muncy Registration #27295	Practitioner Registration No. 32,334

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

[✓] * Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: YEN, Hsiao-Tsung Application No.: 14/338,904 Filed: 23 Jul 2014 Title: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT Attorney Docket No.: 5750/0265PUS1	Examiner: PATEL, Rakesh Bhaskarbhai Art Unit: 2842 Confirmation Number: 1455

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL UNDER 37 CFR 1.116

Dear Sir:

In response to the Final Office Action of 28 Jul 2016, and in view of Request for Participation in the After Final Consideration Pilot Program being filed concurrently herewith, the following are provided:

Amendments to the Claims; and

Remarks.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially vertically aligned ~~overlapped~~ with the coil-conductor segment.

2. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

3. (Original) The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

4. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

5. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 4, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction.

6. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a tap segment, electrically connected to the coil-conductor segment;

wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein one of the plurality of connecting segments is located below the tap segment and overlapped with the tap segment; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

7. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, wherein the coil-conductor segment has a pair of staggered parts, a second region is defined by outer sides of the pair of staggered parts, and the semiconductor device further comprises:

an electronic component, arranged corresponding to the second region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

8. (Original) The semiconductor device with an LC resonant circuit according to claim 7, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

9. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

10. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 9, wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment.

11. (New) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

REMARKS

Claims 1-11 are now present in this application.

Claim 1 has been amended. Claim 11 has been added. Favorable consideration of the application, as amended, is respectfully requested.

Shortened Statutory Period for Response

Since the present response is being filed within two (2) months of the mailing date of the final action, if an advisory action is not mailed until after the end of the three month shortened statutory period for response, then the shortened statutory period for response will expire on the day the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. However, it is believed that this application is in condition for allowance, and therefore no advisory action is expected.

Entry of Amendments

It is respectfully submitted that the foregoing amendments do not contain new matter. Specifically, the amendment to claim 1 is supported by Figures 2, 5, 8, 11, 15 and 17 and paragraph [0055] of original specification. As such, the Examiner is respectfully requested to enter the same.

Rejections under 35 USC 102

Claims 1-4 and 6-10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Daley, et al. (U.S. Patent Application Publication No. 2009/0322447; hereinafter "Daley"). This rejection is respectfully traversed.

Daley discloses: "The on-chip capacitor is positioned laterally within the at least one second metallization level such that **the on-chip capacitor is in a substantially vertical alignment with the on-chip inductor** in the at least one first metallization level." (see paragraph [0007]). Furthermore, Daley discloses: "**The on-chip capacitor 16 and the on-chip inductor 20 are arranged** laterally within the respective metallization levels and **in approximate vertical alignment** such that the on-chip capacitor 16 is disposed between the on-chip inductor 20 and the substrate 24." (see paragraph [0034]).

Daley teaches away from the claimed invention.

Independent claim 1 recites:

> "A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

> a first insulation layer;
> an inductor component, comprising:
> a coil-conductor segment, located on a surface of the first insulation layer; and
> two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and
> a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and **the capacitor component is <u>not</u> substantially vertically aligned with the coil-conductor segment**." (Emphasis added.)

Furthermore, the specification of the application discloses:

> "in the semiconductor device with an LC resonant circuit according to the present invention, an LC resonant circuit may be integrated on a semiconductor substrate by means of a 3D die stacking technology, and a resonant capacitor is arranged corresponding to an input/output part of an inductor component, so as to ***reduce generation of phase noise, arrangement of interconnecting wires, and an overall size***. In some embodiments, in the semiconductor device with an LC resonant circuit according to the present invention, other electronic components are arranged corresponding to the input/out part or a staggered part of the inductor component, so as to further ***reduce generation of phase noise, arrangement of interconnecting wires, parasitic RLC (Resistance- Inductance- Capacitance) and an overall size***."

Therefore, Daley fails to teach or suggest, "*the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and* ***the capacitor component is <u>not</u> substantially vertically aligned with the coil-conductor segment***," as recited in claim 1, and thus amended claim 1 is not anticipated or rendered obvious by Daley.

Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

<u>Allowable Subject Matter</u>

Applicants gratefully acknowledge the Examiner's indication that claim 5 would be allowable if rewritten in independent form. Without conceding the appropriateness of the Examiner's rejection, new claim 11 has been added to include the limitations of claims 1, 4 and

5. Accordingly, claim 11 is now in condition for allowance.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require action, it is respectfully requested that the Examiner telephone Joe McKinney Muncy, Applicants' Attorney, at 703.621.7140 so that such issues may be resolved as expeditiously as possible.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; in particular, extension of time fees.

Date: September 16, 2016

Respectfully submitted,

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Joe McKinney Muncy
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ROBERT F. GNUSE
Registration #27295

Electronic Acknowledgement Receipt

EFS ID:	26949423
Application Number:	14338904
International Application Number:	
Confirmation Number:	1455
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Customer Number:	60601
Filer:	Joe McKinney Muncy/Anita Paka
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	5750/0265PUS1
Receipt Date:	16-SEP-2016
Filing Date:	23-JUL-2014
Time Stamp:	14:02:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	After Final Consideration Program Request	2016-09-16-AFCP-pto.pdf	185557 f9e37f222994b37e9cc58d144beae392f10c0e98	no	1

Warnings:

Information:					
2		2016-09-16-AmendmentAF-asfiled.pdf	731182 1cc292ed8e829778bba51500c67050ab301aadf6	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	7

Warnings:	
Information:	
Total Files Size (in bytes):	916739

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/338,904	Filing Date 07/23/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	09/16/2016	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 11	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
MARCIA GORDON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

60601 7590 07/28/2016

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER
PATEL, RAKESH BHASKARBHAI

ART UNIT	PAPER NUMBER
2842	

MAIL DATE	DELIVERY MODE
07/28/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/338,904	Applicant(s) YEN ET AL.	
	Examiner RAKESH PATEL	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/17/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-4 and 6-10* is/are rejected.

8)☒ Claim(s) *5* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *6/17/2016*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. In the amendment dated 6/17/2016, the following has occurred: Claims 1, 5, and 7 have been amended.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-10 are pending.

Claim Rejections - 35 USC § 102

6. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Daley et al. US 2009/0322447 (of record).

As per claims 1-4 and 6-10, Daley et al. discloses in Figs. 1-2, 2a-2b, and 3 **a semiconductor device with an LC resonant circuit** (Fig. 1, BEOL wiring structure 10; As stated in Paragraph 2, structure 10 is a semiconductor device. As stated in Paragraph 33 lines 6-8, terminals 56, 58 (i.e. Fig. 1) are coupled with ports 25, 35 (i.e. Fig. 2) to form an LC resonator.)**, comprising:**

as per claims 1, 9, and 10, **a first insulation layer** (Fig. 2a, dielectric layer 18)**; an inductor component** (Fig. 1, on-chip inductor 20) **comprising a coil-conductor segment** (Figs. 1-2a, signal lines 50 and 52) **located on a surface of the first insulation layer** (Fig. 2a; As shown, signal lines 50 and 52 are located on a top surface of dielectric layer 18.)**, and two extension-conductor segments** (Annotated Fig. 1 below, the conductor segments annotated as A) **located on the surface of the first insulator layer, coupled to two ends**

of the coil-conductor segment respectively (Annotated Fig. 1 below, the ends annotated as B of signal line 50)**, arranged at an interval, and extending outwards relative to the coil-conductor segment** (Annotated Fig. 1 below; The conductor segments annotated as A are arranged at a distance apart (i.e., an interval) from one another and extend outward from the respective ends annotated as B.)**, wherein a first region is defined between the two extension-conductor segments and the coil-conductor segments** (Fig. 1, the enclosed circular area within inductor 20)**; and a capacitor component** (Fig. 1, on-chip capacitor 16)**, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer** (Fig. 2a; Capacitor 16 is embedded within wiring structure 10 directly below the "first region" on the opposite surface (i.e. bottom surface) of dielectric 18.)**, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment** (Annotated Fig. 1 below; As shown, each of four corners of capacitor 16 all extend outwards in respective directions annotated as W-Z from signal lines 50 and 52.)**, and the capacitor component is not substantially overlapped with the coil-conductor segment** ("Substantially" is defined as to a great or significant extent. As shown in Fig. 1, there are portions of on-chip capacitor 16 which both overlap and do not overlap signal lines 50 and 52 when viewing the structure in a vertical direction. Only the portion of capacitor 16 which is directly disposed underneath signal lines 50 and 52 is overlapped with capacitor 16. The remaining substantial portion of capacitor 16 (i.e. which includes at least the four corners of capacitor 16 and a center portion directly below the "first region") which substantially defines capacitor 16 is not overlapped with signal lines 50 and 52.)**;**

as per claims 2, 3, and 8, **a second insulation layer** (Fig. 2a, dielectric layer 12)**, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer** (Fig. 2a; Capacitor 16 is sandwiched between dielectric layers 18 and 12.)**; and a transistor component** (Paragraph 23 and Fig. 2a, field effect transistor 22a) **arranged corresponding to the first region in an embedded manner on the other surface, opposite to the capacitor component, of the second insulating layer** (Fig. 2a; FET 22a

is disposed on an opposite surface (i.e. bottom surface) of dielectric layer 12 which is opposite to a top surface of dielectric 12 that faces capacitor 16.)**;**

as per claims 4 and 6, **a tap segment** ("Tap" is defined as an electrical connection made to some point between the end terminals of a component. Vias 48 in Fig. 2 are "tap segments" disposed between input/outputs 25 and 35.)**, electrically connected to the coil-conductor segment; wherein the capacitor component comprises a plurality of connecting segments** (Fig. 2, conductive bars 26 and 28)**, extending corresponding to the two extension-conductor segments in a same direction** (As shown in the annotated Fig. 1 below, conductive bars 26 and 28 (not labeled) which are disposed on the left and right sides of capacitor 16 extend along the line annotated as C, which is the same line direction as which the extension-conductor segments annotated as A extend along.)**; and a plurality of electrode segments** (Fig. 2, electrodes 30 and 32) **located below the first region** (Fig. 1; Electrodes 30 and 32 in Fig. 2 are portions of capacitor 16 which is disposed underneath the enclosed circular area region within inductor 20.)**, wherein one end of each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments** (Paragraph 24 and Fig. 2; Electrodes 30 are directly connected with conductive bars 26 and electrodes 32 are directly connected with conductive tab 28. Each of the electrodes has an end that extends laterally or "toward" the side with the other conductive bar that the respective electrode is not connected to.)**; and**

as per claim 7, **wherein the coil-conductor segment has a pair of staggered parts** (Annotated Fig. 1 below; "Stagger" is defined as a cross-over section of the "coil-conductor segment" based on Fig. 9 and page 14 lines 18-20 of the instant specification. A portion of an outermost loop of the signal lines "crosses over" and connects with a portion of an inner loop of the signal lines within the sections annotated as D and E when viewing the structure in a vertical direction. Thus, signal lines 50 and 52 have a pair of crossover sections or "staggered parts" annotated as D and E.)**, a second region is defined by outer sides of the pair of staggered**

parts (Annotated Fig. 1 below; Left and right sides of each of the sections annotated as D and E necessarily form "a second portion" of the coil-conductor segment.).

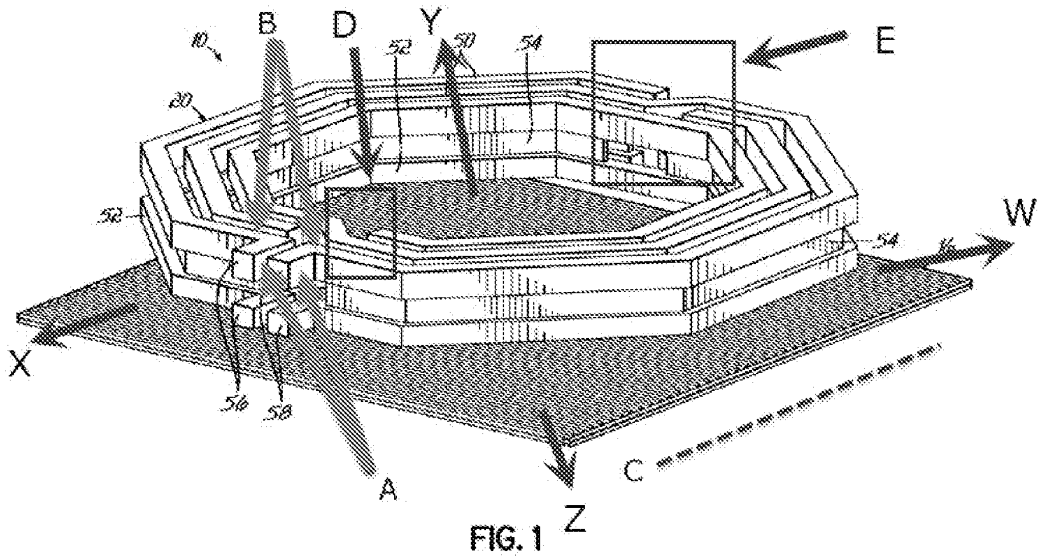


FIG. 1

Allowable Subject Matter

7. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. See reasons for allowance in Office action dated 9/30/2015.

Response to Arguments

8. Applicant's arguments filed 6/17/2016 have been fully considered but they are not persuasive.

On pages 5-6 of Applicant's Remarks dated 6/17/2016, the Applicant states that in Daley, the four corners of capacitor 16 are NOT arranged corresponding to the region defined by TWO conductor segments and the coil-conductor segment. Moreover, in order to operate as a Faraday shield and provide the isolation, the capacitor 16 of Daley BE overlapped with the coil-conductor segment of the inductor 20 of Daley. Thus, Daley fails to teach "a first region defined by the two extension-conductor segments and the coil-conductor segment", "a capacitor component, arranged corresponding to the first region", "the capacitor component is

correspondingly configured outwards related to the coil-conductor segment", and "the capacitor component is substantially un-overlapped with the coil-conductor segment", as recited in claim 1.

The Examiner respectfully disagrees with the Applicant. The claim merely recites "a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface". As explained above in the Office action, at least a portion of capacitor 16 of Daley is disposed directly below the defined "first region". The claim does not limit the entire capacitor to be disposed directly below the first region. The Examiner acknowledges the Applicant's arguments pertaining to Daley operating as a "Faraday shield". However, although a portion of capacitor 16 does indeed overlap with inductor 20, as clearly shown in Fig. 1 of Daley, a substantial portion of capacitor 16 DOES NOT overlap inductor 20 when viewing the structure in the vertical direction. Thus, Daley indeed teaches "a capacitor component", "a first region defined by the two-extension-conductor segments and the coil-conductor segment" as explained above. The rejections to claims 1-4 and 6-10 have been sustained and repeated above.

Conclusion

9. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAKESH PATEL whose telephone number is (571)272-0961. The examiner can normally be reached on Monday-Friday 7:30 am-5:00 pm ET, ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. P./
Examiner, Art Unit 2842

/ROBERT PASCAL/
Supervisory Patent Examiner, Art Unit 2842

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S35	750	S34 and resona$4	US-PGPUB; USPAT	OR	ON	2016/07/11 18:20
S28	2506	(333/175,177,185).ccls.	US-PGPUB; USPAT	OR	ON	2016/07/11 18:19
S29	3745	(336/200).ccls.	US-PGPUB; USPAT	OR	ON	2016/07/11 18:19
S30	1153	(H03H7/0115).cpc.	US-PGPUB; USPAT	OR	ON	2016/07/11 18:19
S31	1688	(H01F27/2804).cpc.	US-PGPUB; USPAT	OR	ON	2016/07/11 18:19
S32	524	(H01F2027/2809).cpc.	US-PGPUB; USPAT	OR	ON	2016/07/11 18:19
S33	1893	(H01F17/0013).cpc.	US-PGPUB; USPAT	OR	ON	2016/07/11 18:19
S34	1454	(S28 or S29 or S30 or S31 or S32 or S33) and semiconductor and inductor and capacitor	US-PGPUB; USPAT	OR	ON	2016/07/11 18:19

7/12/2016 10:59:03 AM
C:\Users\rpatel9\Documents\EAST\Workspaces\14338904.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/18/2015	03/07/2016	07/12/2016						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	O	O						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	✓	✓	✓						
	9	✓	✓	✓						
	10	✓	✓	✓						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

CPC- SEARCHED		
Symbol	Date	Examiner
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	9/18/2015	RP
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	3/7/2016	RP
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	7/12/2016	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
333	175,177,185	9/18/2015	RP
336	200	9/18/2015	RP
333	175,177,185	3/7/2016	RP
336	200	3/7/2016	RP
333	175,177,185	7/12/2016	RP
336	200	7/12/2016	RP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Text Search	9/18/2015	RP
EAST Updated Text Search	3/7/2016	RP
Consulted Examiner, Gerald Stevens	3/7/2016	RP
Inventor Search	3/7/2016	RP
EAST Updated Text Search	7/12/2016	RP
Consulted Examiner, Gerald Stevens	7/12/2016	RP

INTERFERENCE SEARCH

/R.P./ Examiner.Art Unit 2842	

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/R.P./ Examiner.Art Unit 2842	

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	14/338,904
Filing Date	Jul 23, 2014
First Named Inventor	YEN, Hsiao-Tsung
Art Unit	2842
Examiner Name	PATEL, Rakesh Bhaskarbhai
Attorney Docket Number	5750/0265PUS1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
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		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
/R.P./		TW 201206059 A1	02/01/2012	STATS ChipPAC, Ltd.		X
/R.P./		TW 201003883 A1	01/16/2010	Int'l Business Machines Corp.		X
/R.P./		TW 201232579 A1	08/01/2012	Nat'l Taiwan Univ. of Sci. and Tech.		X
/R.P./		TW 200943707	10/16/2009	STATS ChipPAC, Ltd.		X

Examiner Signature	/Rakesh Patel/	Date Considered	07/19/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional).[2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.[3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).[4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.[6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: YEN, Hsiao-Tsung Application No.: 14/338,904 Filed: 23 Jul 2014 Title: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT Attorney Docket No.: 5750/0265PUS1	Examiner: PATEL, Rakesh Bhaskarbhai Art Unit: 2842 Confirmation Number: 1455

MS AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Dear Sir:

In response to the Office Action of 18 Mar 2016, the following are provided:

Amendments to the Claims; and

Remarks.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.

2. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

3. (Original) The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

4. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

5. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 4, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction~~, respectively~~.

6. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a tap segment, electrically connected to the coil-conductor segment;

wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein one of the plurality of connecting segments is located below the tap segment and overlapped with the tap segment; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

7. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 1, wherein the [[-coil]]coil-conductor segment has a pair of staggered parts, a second region is defined by outer sides of the pair of staggered parts, and the semiconductor device further comprises:

an electronic component, arranged corresponding to the second region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

8. (Original) The semiconductor device with an LC resonant circuit according to claim 7, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

9. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

10. (Previously Presented) The semiconductor device with an LC resonant circuit according to claim 9, wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment.

REMARKS

Claims 1-10 remain present in this application.

Claims 1, 5 and 7 have been amended. Favorable consideration of the application, as amended, is respectfully requested.

Entry of Amendments

It is respectfully submitted that the foregoing amendments do not contain new matter. As such, the Examiner is respectfully requested to enter the same.

Objections to the Claims

The claims stand objected to for certain informalities. In view of the foregoing amendments, it is respectfully submitted that these informalities have been addressed. Reconsideration and withdrawal of any objection to the claims are respectfully requested.

Rejections under 35 USC 102

Claims 1-4 and 6-10 stand rejected under 35 USC 102(a)(1) as being anticipated by Daley, et al. (U.S. Patent Application Publication No. 2009/0322447; hereinafter "Daley"). This rejection is respectfully traversed.

Daley discloses:

> "**The on-chip capacitor 16 and the on-chip inductor 20 are arranged laterally** within the respective metallization levels and in approximate vertical alignment such that the on-chip capacitor 16 is disposed between the on-chip inductor 20 and the substrate 24. Specifically, **the outermost edges of the on-chip capacitor 16**, such as representative edges 90, 92 respectively visible in FIGS. 2A and 2B, **are approximately aligned, when viewed in a vertical direction, with the outermost edges of the on-chip inductor 20**, such as representative edges 94, 96 respectively visible in FIGS. 2A and 2B. In the representative embodiment, **the on-chip capacitor 16 effectively operates as a Faraday shield to enhance the inductor quality** by increasing the quality factor, Q, **of the on-chip inductor 20** and to **provide isolation between the active devices 22a, 22b on substrate 24 and the on-chip inductor 20**."

Figure 1 of Daley clearly recites that the capacitor 16 covers with the ***WHOLE*** of the inductor 20.

In other words, in Daley, the four corners of capacitor 16 are ***NOT*** **arranged corresponding to the region defined by *TWO* conductor segments** (annotated as A shown in following FIG. 1) **and the coil-conductor segment** (the signal line 50 shown in following FIG.

1).

Moreover, in order to operate as a Faraday shield and provide the isolation, the capacitor 16 of Daley ***BE*** **overlapped with** the coil-conductor segment of the inductor 20 of Daley.

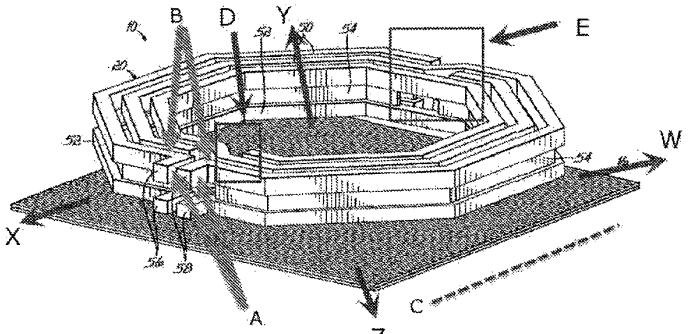


FIG. 1

In the present invention, the specification of the application discloses:

> "in the semiconductor device with an LC resonant circuit according to the present invention, an LC resonant circuit may be integrated on a semiconductor substrate by means of a 3D die stacking technology, and a resonant capacitor is arranged corresponding to an input/output part of an inductor component, so as to ***reduce generation of phase noise, arrangement of interconnecting wires, and an overall size***. In some embodiments, in the semiconductor device with an LC resonant circuit according to the present invention, other electronic components are arranged corresponding to the input/out part or a staggered part of the inductor component, so as to further ***reduce generation of phase noise, arrangement of interconnecting wires, parasitic RLC (Resistance-Inductance- Capacitance) and an overall size***."

Therefore, Daley fails to teach or suggest, "**a first region is *defined by the two extension-conductor segments* and the coil-conductor segment**" "**a capacitor component, *arranged corresponding to the first region***" "the capacitor component is correspondingly configured **outwards relative to the coil-conductor segment**" and "the capacitor component is substantially ***un-***overlapped with the coil-conductor segment," as recited in claim 1.

Therefore, Daley fails to anticipate the claimed invention. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Allowable Subject Matter

Applicants gratefully acknowledge that the Examiner considers claim 5 to contain allowable subject matter. In view of the foregoing amendments and/or remarks, it is respectfully submitted that all claims should be fully in condition for allowance.

Conclusion

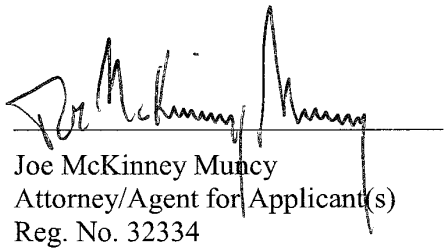
Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require action, it is respectfully requested that the Examiner telephone Joe McKinney Muncy, Applicants' Attorney, at 703.621.7140 so that such issues may be resolved as expeditiously as possible.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; in particular, extension of time fees.

Date: June 17, 2016

Respectfully submitted,



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Joe McKinney Muncy
Attorney/Agent for Applicant(s)
Reg. No. 32334

Search terms : (1) (201206059)@PN 【 印出 】

Patent/Publication Number	201206059
Title	Semiconductor device and method of forming RF balun having reduced capacitive coupling and high CMRR
Issued/Publication Date	2012/02/01
Application Date	2011/03/15
Application Number	100108685 Espacenet
IPC	H03H-011/32(2006.01)
Inventor	LIU, KAI CN; FRYE, ROBERT C. US
Applicant	STATS CHIPPAC, LTD.SG
Individual	F
Priority Number	20100330 US 20100750555
Abstract	A semiconductor device has an RF balun formed over a substrate. The RF balun includes a first conductive trace wound to exhibit inductive properties with a first end coupled to a first terminal of the semiconductor device and second end coupled to a second terminal of the semiconductor device. A first capacitor is coupled between the first and second ends of the first conductive trace. A second conductive trace is wound to exhibit inductive properties with a first end coupled to a third terminal of the semiconductor device and second end coupled to a fourth terminal of the semiconductor device. The first conductive trace is formed completely within the second conductive trace. The first conductive trace and second conductive trace can have an oval, circular, or polygonal shape separated by 50 micrometers. A second capacitor is coupled between the first and second ends of the second conductive trace.

Information on this system is for reference only, it cannot be used as grounds for approval or rejection.
In all instances of discrepancy, official publication from TIPO shall prevail and should be consulted.

(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201206059 A1
(43)公開日： 中華民國 101 (2012) 年 02 月 01 日

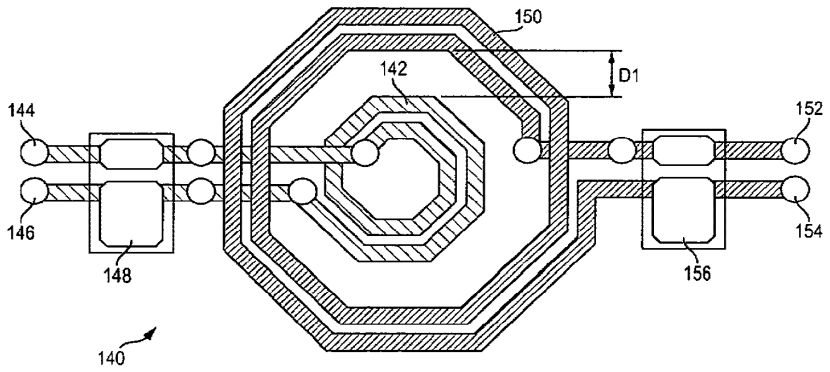
(21)申請案號：100108685 (22)申請日： 中華民國 100 (2011) 年 03 月 15 日
(51)Int. Cl.： *H03H11/32 (2006.01)*
(30)優先權：2010/03/30 美國 12/750,555
(71)申請人：史達晶片有限公司 (新加坡) STATS CHIPPAC, LTD. (SG)
新加坡
(72)發明人：劉凱 LIU, KAI (CN) ；富萊 羅勃特 C FRYE, ROBERT C. (US)
(74)代理人：閻啟泰；林景郁
申請實體審查：無 申請專利範圍項數：25 項 圖式數：9 共 38 頁

(54)名稱

半導體裝置和形成具有減少的電容性耦合和高ＣＭＲＲ的ＲＦ平衡－不平衡轉換器的方法
SEMICONDUCTOR DEVICE AND METHOD OF FORMING RF BALUN HAVING REDUCED CAPACITIVE COUPLING AND HIGH CMRR

(57)摘要

一種半導體裝置具有形成於一基板上的一射頻平衡-不平衡轉換器。該射頻平衡-不平衡轉換器包含捲繞的第一導線，以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性。一第一電容器係耦接於該第一導線的第一及第二末端之間。一第二導線被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性。該第一導線係完全地形成於該第二導線內。該第一導線及該第二導線可具有相隔 50 微米的橢圓形、圓形或多邊形外形。一第二電容器係耦接於該第二導線的第一及第二末端之間。



140：整合式射頻平衡-不平衡轉換器
142：導線或線圈
144：埠
146：埠
148：電容器
150：導線或線圈
152：埠
154：埠
156：電容器

(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201206059 A1
(43)公開日： 中華民國 101 (2012) 年 02 月 01 日

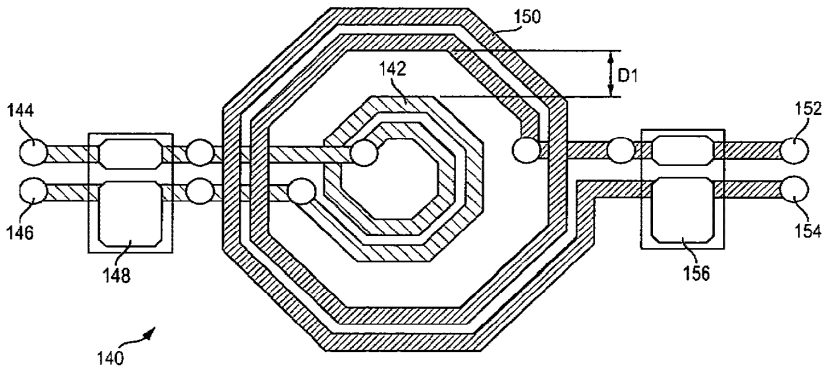
(21)申請案號：100108685 (22)申請日： 中華民國 100 (2011) 年 03 月 15 日
(51)Int. Cl.： *H03H11/32 (2006.01)*
(30)優先權：2010/03/30 美國 12/750,555
(71)申請人：史達晶片有限公司 (新加坡) STATS CHIPPAC, LTD. (SG)
新加坡
(72)發明人：劉凱 LIU, KAI (CN) ；富萊 羅勃特 C FRYE, ROBERT C. (US)
(74)代理人：閻啟泰；林景郁
申請實體審查：無 申請專利範圍項數：25 項 圖式數：9 共 38 頁

(54)名稱

半導體裝置和形成具有減少的電容性耦合和高ＣＭＲＲ的ＲＦ平衡－不平衡轉換器的方法
SEMICONDUCTOR DEVICE AND METHOD OF FORMING RF BALUN HAVING REDUCED CAPACITIVE COUPLING AND HIGH CMRR

(57)摘要

一種半導體裝置具有形成於一基板上的一射頻平衡-不平衡轉換器。該射頻平衡-不平衡轉換器包含捲繞的第一導線，以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性。一第一電容器係耦接於該第一導線的第一及第二末端之間。一第二導線被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性。該第一導線係完全地形成於該第二導線內。該第一導線及該第二導線可具有相隔 50 微米的橢圓形、圓形或多邊形外形。一第二電容器係耦接於該第二導線的第一及第二末端之間。



140：整合式射頻平衡-不平衡轉換器
142：導線或線圈
144：埠
146：埠
148：電容器
150：導線或線圈
152：埠
154：埠
156：電容器

六、發明說明：

【發明所屬之技術領域】

本發明大體上關於半導體裝置，且更特別地，關於一種半導體裝置和形成具有減少LC共振器間的電容性耦合及高共模拒斥比的射頻平衡-不平衡轉換器的方法。

【先前技術】

半導體裝置係普遍地見於現代電子產品中。半導體裝置隨著電性元件的數量和密度而改變。離散型半導體裝置大體上包含一電性元件類型，例如發光二極體(LED)、小訊號電晶體、電阻器、電容器、電感器及功率金屬氧化物半導體場效電晶體(MOSFET)。整合型半導體裝置大體上包含成千上萬的電性元件。整合型半導體裝置範例包含微控制器、微處理器、電荷耦合裝置(CCD)、太陽能電池和數位微型反射鏡裝置(DMD)。

半導體裝置執行各式各樣的功能，例如高速計算、收發電磁波訊號、控制電子裝置、轉換太陽光成為電力和替電視顯示器產生視覺投影。半導體裝置係見於娛樂、通訊、電力轉換、網路、電腦及消費品領域中。半導體裝置也見於軍事應用、航空、汽車、工業控制及辦公室設備中。

半導體裝置利用半導體材料的電性特性。半導體材料的原子結構允許它的導電性受到施加電場或基極電流或透過摻雜製程來操縱。摻雜技術將雜質引入該半導體材料中以操縱並控制該半導體裝置的導電性。

一半導體裝置包含主動和被動電性結構。包含雙載子電晶體及場效電晶體的主動結構控制電流的流動。藉由改變摻雜水準及施加一電場或基極電流，該電晶體不是增進就是壓制該電流流動。包含電阻器、電容器和電感器的被動結構建立執行各種電性功能所需電壓和電流間的關係。該些主動和被動結構係電性連接以形成致能該半導體裝置來執行高速計算和其它有用功能的電路。

半導體裝置大體上係使用例如前端製程和後端製程的二複雜製程來製造，每一個製程可能涉及數百種步驟。前端製程涉及在一半導體晶圓表面上形成複數個晶粒。每一個晶粒典型地係一模一樣且包含由電性連接主動和被動元件所形成的電路。後端製程涉及自已完成晶圓中單粒化個別晶粒並封裝該晶粒以提供結構性支撐和環境上隔離。

半導體製程的一目標係製造更小半導體裝置。較小裝置典型地耗用較少電力，具有較高執行效率並可更有效率地被製造。此外，較小半導體裝置具有可期待更小末端產品的較小佔用空間。一較小晶粒尺寸可藉由改善該前端製程而產生具有較小且較高密度的主動和被動元件而得。後端製程可藉由改善電性相連和封裝材料來產生具有較小佔用空間的半導體裝置封裝。

半導體製程的另一目標係產生較高執行效率的半導體裝置。裝置執行效率增加可藉由形成能夠操作於較高速度下的主動元件而得。例如在射頻(RF)無線通訊的高頻應用中，整合被動元件(IPD)常常被納入該半導體裝置內。整合

被動元件範例包含電阻器、電容器和電感器。一典型射頻系統在一或更多半導體封裝中需要多個整合被動元件以執行所需電性功能。

一射頻平衡-不平衡轉換器在無線通訊系統中係一重要元件。該射頻平衡-不平衡轉換器被用以利用適當的阻抗轉換公式將例如來自一功率放大器或收發器的差動訊號轉換成單端訊號。該平衡-不平衡轉換器壓抑電性雜訊，執行阻抗轉換及匹配，並透過電磁耦合來極小化共模(雜訊、隨機雜訊或其它電性干擾)。

一傳統平衡-不平衡轉換器 10 係示於圖 1，具有導線或線圈 12 互相捲繞或與導線或線圈 14 交錯以增加該些電感器間的交互耦合。導線 12 具有耦接至平衡埠 16 和 18 的第一和第二末端接頭。電容器 20 係耦接於埠 16 和 18 間。該電感器 12 和電容器 20 構成一第一 LC(電感器和電容器)共振器。導線 14 具有耦接至不平衡埠 24 和埠 26(接地端)的第一和第二末端接頭。電容器 28 係耦接於埠 24 和 26。該中心閥門 30 和導線 32 供應一直流偏壓至平衡埠 16 和 18。該電感器 14 和電容器 28 構成一第二電感電容共振器。

該射頻平衡-不平衡轉換器執行效率的優勢係共模拒斥比(CMRR)。一不當共模拒斥比導致電源供應調變和接收電路內例如該低雜訊放大器的自我混合。例如一功率放大器的電性裝置的諧波響應時常以共模形式存在。為了減少不要的諧波響應，在該射頻平衡-不平衡轉換器中期待一高共模拒斥比。

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一高共模拒斥比可能難以在圖 1 所示配置中得到，尤其是在較高頻下，部分起因於該電感電容共振器 12 和 20 及該電感電容共振器 14 和 28 間的電容性耦合之故。電感電容共振器中的電流係由共同電感所耦合。至該不平衡電感電容共振器的輸入訊號感應出該平衡電感電容共振器內的電流，反之亦然。理想上，施加至該平衡埠 16 和 18 的共模訊號引起相等但相反電流流入電感器 14，且沒有訊號被傳送至該不平衡埠 24。為了補償，該射頻平衡-不平衡轉換器尺寸被製造的相當大以提供強磁性耦合。該些電感電容共振器間的耦合係數典型地被製造與實際一樣大，例如，大於 0.6，以得到所需的磁性耦合。此外，該些電感電容共振器間的耦合被製造的大以提供較大頻寬。

然而，電感電容共振器間的寄生電容性耦合讓該共模訊號洩至該不平衡埠，尤其是在較高頻下。儘管具有交錯式導線的較大平衡-不平衡轉換器具有某些優勢，也就是製程變化上的穩健性以及改善的頻寬、帶通響應、匹配、載入品質、電阻性損失及插入損失，但它也消耗晶粒面積，其增加該製程的成本、減少平衡並增加電容性耦合而降低共模拒斥比。

【發明內容】

存在對具有減少電容性耦合和高共模拒斥比的射頻平衡-不平衡轉換器的需求。據此，在一實施例中，本發明係一種半導體裝置，該半導體裝置包括一基板和形成於該基

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板上的平衡-不平衡轉換器。該平衡-不平衡轉換器包含被捲繞以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性的一第一導線。一第一電容器係耦接於該第一導線的第一及第二末端之間。該平衡-不平衡轉換器進一步包含被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性的一第二導線。該第一導線係完全形成於該第二導線內。一第二電容器係耦接於該第二導線的第一及第二末端之間。

在另一實施例中，本發明係一種半導體晶粒，該半導體晶粒包括一基板和形成於該基板上且被捲繞以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性的一內部導線。一外部導線係形成於該基板上且被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性。該內部導線係形成於該外部導線內。

在另一實施例中，本發明係一種半導體裝置，該半導體裝置包括一基板和形成於該基板上的第一電感器。一第二電感器係形成於該基板上。該第一電感器係形成於該第二電感器內。

在另一實施例中，本發明係一種形成一半導體晶粒的方法，該方法包括下列步驟：提供一基板、在該基板上形成一捲繞的內部導線以展示具有耦接至該半導體裝置的第

一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性、及在該基板上形成一捲繞的外部導線以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性。該內部導線係形成於該外部導線內。

【實施方式】

本發明係描述於參考該些圖形進行下列說明的一或更多實施例中，其中，類似編號代表相同或類似構件。儘管本發明以就取得本發明目的的最佳模式做說明，然而熟知此項技術之人士要理解的是，想要涵蓋可能包含於下列揭示和圖式所支持的所附申請專利範圍和它們等效例所定義的本發明精神和範圍內的替代例、修改例及等效例。

半導體裝置大體上係使用二複雜製程來製造：前端製程和後端製程。前端製程涉及在一半導體晶圓表面上形成複數個晶粒。該晶圓上的每一個晶粒內含主動和被動電性元件，其係電性連接以形成功能性電性電路。如電晶體和二極體的主動電性元件具有控制電流流動的能力。如電容器、電感器、電阻器和變壓器的被動電性元件建立用以執行電性電路功能所需的電壓和電流間的關係。

被動和主動元件係由包含摻雜、沉積、微影成像、蝕刻和平坦化的一系列製程步驟來形成於該半導體晶圓表面上。摻雜藉由如離子植入或熱擴散的技術將雜質引入該半導體材料中。該摻雜製程改變主動裝置內的半導體材料的

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導電性，轉換該半導體材料成為一絕緣體、導體，或動態地改變該半導體材料導電性以回應一電場或基極電流。電晶體內含用以依據該電場或基極電流的應用來致能該電晶體以增進或限制電流流動所需而安排的不同摻雜類型和程度的區域。

主動和被動元件係由具有不同電性特性的材料層所形成。該些層可藉由以沉積材料類型所部分決定的各種沉積技術來形成。例如，薄膜沉積可涉及化學氣相沉積(CVD)、物理氣相沉積(PVD)、電鍍和無電鍍製程。每一層大體上被圖案化以形成主動元件、被動元件或元件間的電性連接的各部分。

該些層可使用微影成像技術來進行圖案化，其涉及將如光阻劑的感光材料沉積覆蓋在欲圖案化層上。使用光使一圖案自一光罩轉移至光阻劑。使用一溶劑將遇到光的光阻劑圖案部分移除，露出圖案化的下層部分。將剩餘光阻劑移除，留下一圖案化層。或者，一些材料類型係藉由使用例如無電鍍和電鍍技術將該材料直接沉積至前一沉積/蝕刻製程所形成的區域或孔隙中。

沉積一薄膜材料於一現存圖案上可擴大下面圖案並產生不均勻平坦表面。產生較小且更密地包裝的主動和被動元件需要一均勻平坦表面。平坦化可被使用以移除來自該晶圓表面的材料並產生一均勻平坦表面。平坦化涉及以一拋光片來拋光該晶圓表面。一研磨材料和腐蝕性化學藥品係於拋光期間添加至該晶圓表面。該化學藥品的研磨和腐

蝕動作的結合式機械動作移除任何不規擇拓樸，產生一均勻平坦表面。

後端製程指切割或單粒化該完成晶圓成為個別晶粒，接著封裝該晶粒以提供結構支撐和環境隔離。為了單粒化該晶粒，該晶圓係沿著所謂切割道或劃線的晶圓無功能區域來劃線並切斷。使用一雷射切割工具或鋸子來單粒化該晶圓。在單粒化後，該個別晶粒被安裝至包含接腳或接觸墊片以與其它系統元件互相連接的封裝基板。形成於該半導體晶粒上的接觸墊片接著被連接至該封裝內的接觸墊片。可利用銲接凸塊、短柱凸塊、導電膏或接線來製造該些電性連接。一密封劑或其它密封材料係沉積於該封裝上以提供物理性支撐和電性隔離。該完成封裝接著被插入至一電性系統中，且該半導體裝置的功能可由其它系統元件利用之。

圖 2 說明具有內含複數個半導體封裝安裝於它表面上的晶片載體基板或印刷電路板(PCB)52 的電子裝置 50。電子裝置 50 可具有一半導體封裝類型或多種半導體封裝類型，視應用而定。基於說明的目的，圖 2 顯示不同半導體封裝類型。

電子裝置 50 可為使用該些半導體封裝來執行一或更多電性功能的獨立系統。或者，電子裝置 50 可以是一較大系統的子元件。例如，電子裝置 50 可以是一圖形卡、網路介面卡或可插入至一電腦的其它訊號處理卡。該半導體封裝可包含微處理器、記憶體、特殊用途積體電路(ASIC)、邏輯

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電路、類比電路、射頻電路、離散裝置或其它半導體晶粒或電性元件。

在圖 2 中，印刷電路板 52 提供一總基板以提供安裝於該印刷電路板上的半導體封裝結構上的支撐和電性連接。訊號導線 54 係使用蒸鍍、電鍍、無電鍍、網印或其它合適金屬沉積製程來形成於一表面上或印刷電路板 52 的各層內。訊號導線 54 提供該些半導體封裝、安裝元件及其它外部系統元件的每一個間的電性通訊。導線 54 也提供電力和接地連接給該些半導體封裝中的每一個。

在一些實施例中，一半導體裝置具有二封裝層級。第一層級封裝係用於機械性及電性附接該半導體晶粒至一中間載體的技術。第二層級封裝涉及機械性及電性附接該中間載體至該印刷電路板上。在其它實施例中，一半導體裝置可以只具有該第一層級封裝，其中，該晶粒係機械性及電性地直接安裝至該印刷電路板上。

基於說明目的，包含打線封裝 56 及覆晶封裝 58 的一些第一層級封裝類型係示於印刷電路板上。此外，包含球狀柵格陣列(BGA)60、凸塊晶片載體(BCC)62、雙列式封裝(DIP)64、平面柵格陣列(LGA)66、多晶片模組(MCM)68、四邊扁平無接腳封裝(QFN)70 和四邊扁平封裝 72 的一些第二層級封裝類型係顯示安裝於印刷電路板 52 上。依據系統需求，可將利用任何第一和第二層級封裝型結合所架構的任何半導體封裝結合及其它電子元件連接至印刷電路板 52。在一些實施例中，電子裝置 50 包含單一附接半導體封

裝，而其它實施例需要多個互連封裝。藉由結合單一基板上的一或更多半導體封裝，製造商可整合預先製造元件至電子裝置和系統中。因為該些半導體封裝包含複雜功能、電子裝置可使用較便宜元件及有效率製程來製造之。產生的裝置較不會失敗且製造費用也較少，因而對於消費者而言產生一較低成本的結果。

圖 3a 至圖 3c 顯示示範性半導體封裝。圖 3a 說明安裝於印刷電路板 52 上的雙列式封裝 64 的進一步細節。半導體晶粒 74 包含一作用區，內含配置成形成於該晶粒內並根據該晶粒的電性設計來電性互連的主動裝置、被動裝置、導電層及介電層的類比或數位電路。例如，該電路可包含一或更多電晶體、二極體、電感器、電容器、電阻器和形成於該半導體晶粒 74 的作用區內的其它電路構件。接觸墊片 76 係例如鋁(Al)、銅(Cu)、錫(Sn)、鎳(Ni)、金(Au)或銀(Ag)的一或更多導電材料層，且被電性連接至形成於半導體晶粒 74 內的電路構件。在雙列式封裝 64 的組合其間，半導體晶粒 74 係使用一金矽共熔合金層或例如熱環氧化物或環氧樹脂的黏性材料來安裝至一中間載體 78。該封裝本體包含例如聚合物或陶瓷的絕緣封裝材料。導體接腳 80 或接線 82 提供半導體晶粒 74 及印刷電路板 52 間的電性互連。密封劑 84 係沉積覆蓋於該封裝上，藉由阻止濕氣及微粒進入該封裝並污染晶粒 74 和接線 82 而提供環境保護。

圖 3b 說明安裝於印刷電路板 52 上的凸塊晶片載體 62 的進一步細節。半導體晶粒 88 係使用一底膠或環氧樹脂黏

性材料 92 來安裝於載體 90 上。接線 94 提供接觸墊片 96 和 98 間的第一層級封裝內連線。密封化合物或密封劑 100 係沉積於半導體晶粒 88 和接線 94 上，以提供該裝置物理支撐和電性隔離。接觸墊片 102 係使用例如電鍍或無電鍍的合適金屬沉積製程來形成於印刷電路板的表面上，以阻止氧化作用。接觸墊片 102 係電性連接至印刷電路板 52 中的一或更多訊號導線 54。凸塊 104 係形成於凸塊晶片載體 62 的接觸墊片 98 及印刷電路板 52 的接觸墊片 102 之間。

在圖 3c 中，利用一覆晶型第一層級封裝技術將半導體晶粒 58 面向下地安裝至中間載體 106。半導體晶粒 58 的作用區 108 包含配置成根據該晶粒的電性設計所形成的主動裝置、被動裝置、導電層及介電層的類比或數位電路。例如，該電路可包含一或更多電晶體、二極體、電感器、電容器、電阻器和在作用區 108 內的其它電路構件。半導體晶粒 58 係透過凸塊 110 來電性且機械性地連接至載體 106。

球狀柵格陣列 60 係利用一球狀柵格陣列型第二層級封裝技術，使用凸塊 112 來電性且機械性地連接至印刷電路板 52。半導體晶粒 58 係透過凸塊 110、訊號線 114 和凸塊 112 來電性連接至印刷電路板 52 中的訊號導線 54。一密封化合物或密封劑 116 係沉積於半導體晶粒 58 和載體 106 上，以提供該裝置物理支撐和電性隔離。該覆晶半導體裝置提供自半導體晶粒 58 上的主動裝置至印刷電路板 52 上的導線的短導電路徑，用以減少訊號傳送距離、降低電容並改善整體電路執行效率。在另一實施例中，該半導體晶

粒 58 可使用覆晶型第一層級封裝技術而不使用中間載體 106 來機械性且電性地直接連接至印刷電路板 52。

與圖 2 和圖 3a-3c 有關的半導體晶粒或封裝 120 被顯示在圖 4 中，其具有如矽(Si)、鍺、砷化鎵(GaAs)、玻璃、低溫共燒陶瓷(LTCC)、印刷電路板的基底材料或其它主體半導體材料所製造的半導體基板 122 作為結構支撐。一作用區 124 係形成於該半導體基板 122 的頂部表面上。作用區 124 包含類比或數位電路，配置成形成於該晶粒內並根據該晶粒的電性設計和功能來電性互連的主動裝置、被動裝置、導電層及介電層。例如，該電路可包含一或更多電晶體、二極體、電感器、電容器、電阻器和形成於該半導體晶粒 74 的作用區內以配置類比電路或數位電路的其它電路構件。半導體晶粒 122 也包含例如薄膜電感器、電容器和電阻器的一或更多整合被動元件以提供射頻訊號處理。作用區 124 約佔用半導體晶粒 120 的整體厚度或高度 H1 的 5-10%。在一實施例中，半導體晶粒 120 佔用一 0.8 毫米(mm)乘 0.45 毫米的面積。可使用覆晶、打線或內連線接腳將半導體晶粒 120 電性連接至其它裝置。

內含複數個整合被動元件的半導體裝置可被使用於高頻應用中，例如，微波雷達、電信系統、無線收發器、電子開關和執行射頻電性功能的其它裝置。該些整合被動元件提供電性特性曲線給例如平衡-不平衡轉換器、共振器、高通濾波器、低通濾波器、帶通濾波器(BPF)、對稱性高品質共振變壓器、匹配網路、射頻耦合器和調諧電容器的電

路功能。例如，該些整合被動元件可充當前端無線射頻元件，其可被放置於該該天線及收發器之間。該平衡-不平衡轉換器抑制電性雜訊，提供自單端至差動埠的模式轉換，執行阻抗轉換及匹配，並透過電磁耦合來極小化共模雜訊。在一些應用中，多個平衡-不平衡轉換器係形成覆蓋於一共同基板上，以允許多頻帶操作。例如，二或更多平衡-不平衡轉換器被使用於行動電話或其它全球行動通訊系統的四頻帶中，每一個平衡-不平衡轉換器專供該四頻帶裝置的一頻帶操作使用。一典型射頻系統在一或更多半導體封裝中需要多個整合被動元件和其它高頻電路，以執行所需電性功能。該無線應用可為使用例如寬頻分碼多重存取(WCDMA)頻帶(個人通訊系統頻帶、IMT 頻帶、低頻帶)和全球行動通訊系統(GSM)頻帶(低頻帶及高頻帶)的多頻帶操作的蜂巢式電話。

圖 5 說明使用一射頻積體電路(RFIC)128 的無線通訊系統 126。射頻積體電路 128 包含一射頻平衡-不平衡轉換器充當整體整合於單一半導體晶粒 120 的基板 122 上的整合被動元件。該射頻平衡-不平衡轉換器可操作於各種頻率範圍，例如 1.71-1.91 或 5.15-5.83 千兆赫(GHz)。射頻積體電路 128 接收不平衡埠 130 上的射頻訊號並提供一平衡差動射頻訊號至埠 134 和 136 上的功率放大器(PA)和收發器 132。功率放大器和收發器 132 放大傳輸用的射頻訊號並以全雙工方式接收射頻訊號，再濾波和調整該些訊號以供進一步處理。

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隨著越來越重視無線消費品的小型化，不管是使用晶片上被動元件或是做為獨立的整合被動元件，都有將射頻平衡-不平衡轉換器變壓器整合至一共同封裝的趨勢。因其具有共同形式因素和低成本之故，將該些整合被動元件整合於射頻積體電路 128 內特別吸引人。該些整合被動元件也具有超過晶片上被動元件的執行效率優勢。

射頻積體電路 128 的進一步細節係示於具有使用電感電容共振器來配置的整合式射頻平衡-不平衡轉換器 140 的圖 6 中。一導線或線圈 142 被捲繞以展示電感特性，且包含耦接至埠 144 和埠 146 的第一和第二末端接頭。在一實施例中，埠 144 係一單端不平衡埠，且埠 146 係一接地端。或者，埠 146 係一單端不平衡埠，且埠 144 係該接地端。導線 142 係形成一多邊形、圓形或橢圓形外形，具有 20 微米(μm)線寬及 10 微米間距或空隔。一電感器 142 及電容器 148 構成一第一電感電容共振器。

另一導線或線圈 150 被捲繞以展示電感特性，且包含耦接至平衡埠 152 和 154 的第一和第二末端接頭。導線 150 係環繞著導線 142 而形成，以使導線 142(內部導線)主要或實際上係放置於導線 150(外部導線)內部，具有間隔 D1=50 微米以減少該些導線間的電感性耦合和電容性耦合兩者。換言之，導線 142 的捲繞部分的全部部件係完全放置於導線 150 的捲繞部分的全部部件內，如圖 6 所示。所形成的導線 150 可具有一多邊形、圓形或橢圓形外形及 20 微米線寬和 10 微米間距或空隔。一電容器 156 係耦接於平衡埠 152

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及 154 之間。該電感器 150 及電容器 156 構成一第二電感電容共振器。

圖 7 顯示具有電感器 142 和 150 及電容器 148 和 156 的射頻平衡-不平衡轉換器 140 的電性示意圖。該些電感器 142 和 150 被捲繞以於該些電感器之間產生用於一窄頻帶響應，例如耦合係數 k=0.2 至 0.45 的相當小的磁性耦合。該電感性耦合強度可藉由改變該二線圈間的距離 D1 來調整。

在另一實施例中，一整合射頻平衡-不平衡轉換器 170 係示於使用電感電容共振器所配置的圖 8 中。一導線或線圈 172 被捲繞以展示電感特性，且包含耦接至平衡埠 172 和 176 的第一和第二末端接頭。導線 172 係形成一多邊形、圓形或橢圓形外形，具有 20 微米(μm)線寬及 10 微米間距或空隔。一電容器 178 係耦接於平衡埠 174 及 176 之間。該中心閥門 180 提供透過電容器 178 至埠 174 和 176 的直流偏壓。該直流偏壓係由電源匯流排 182 所供應，經過導線 184 到達中心閥門 180。電容器 178 可被分割成連接至中心閥門 180 的兩部件。藉由使該二分割電容器輕微地不平衡，該平衡可被最佳化。該電感器 142 及電容器 148 構成一第一電感電容共振器。

另一導線或線圈 190 被捲繞以展示電感特性，且包含耦接至埠 192 和埠 194 的第一和第二末端接頭。在一實施例中，埠 192 係一單端不平衡埠，且埠 194 係一接地端。或者，埠 194 係一單端不平衡埠，且埠 192 係該接地端。導線 190 係形成於導線 172 內，以使導線 190(內部導線)主

要或實際上係放置於導線 172(外部導線)內部，具有間隔 D2=50 微米以減少該些導線間的電感性耦合和電容性耦合兩者。換言之，導線 190 的捲繞部分的全部部件係完全放置於導線 172 的捲繞部分的全部部件內，如圖 8 所示。所形成的導線 190 可具有一多邊形、圓形或橢圓形外形及 20 微米線寬和 10 微米間距或空隔。一電容器 196 係耦接於埠 192 及埠 194 之間。該電感器 190 及電容器 196 構成一第二電感電容共振器。

該射頻平衡-不平衡轉換器的價值指數可表示為該輸入及輸出反射損失、插入損失和該差動埠的平衡(振幅和相位)。在該射頻平衡-不平衡轉換器中的共模拒斥比高度相關於該平衡。在例如低雜訊放大器的接收器電路中，共模訊號產生電源供應調變和自我混合。在發射器中，偶階諧波典型地出現於該共模輸出中。可期待阻擋該些諧波以維持高線性和電磁相容性。

既然該共模偏壓連接並未理想地隔離，至該偏壓供應器的射頻耦合可在該平衡接頭處引入一共模成分。在較高輸出功率處，接近該放大器的壓抑點處，該輸出頻譜中的偶諧波成分也被引入該共模中。據此，一高共模拒斥比對於自該射頻平衡-不平衡轉換器中移除共模訊號係重要的。

該插入損失或差動模式增益係自該不平衡埠分散至該差動埠的功率測量值，如同公式(1)所給予。

$$DMG=S_{DU}=(S_{21}-S_{31})/\sqrt{2} \qquad (1)$$

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該射頻平衡-不平衡轉換器共模增益(反轉該共模拒斥比)係自該不平衡埠分散至該共模埠的功率測量值，如同公式(2)所給予。

$$CMG=S_{CU}=(S_{21}+S_{31})/\sqrt{2} \qquad (2)$$

該射頻平衡-不平衡轉換器的平衡特性曲線係以S參數表示。對於輸入至該不平衡埠的射頻輸入訊號而言，振幅及相位差係於該些平衡埠間進行測量並以來自公式(1)和(2)的共模和差動模增益而論的公式(3)和(4)來表示為：

$$S_{21}=(CMG+DMG)/\sqrt{2} \qquad (3)$$

$$S_{31}=(CMG-DMG)/\sqrt{2} \qquad (4)$$

由公式(3)及(4)中，在 S_{21} 接近 S_{31} 時，該共模增益接近零，也就是高共模拒斥比。該振幅平衡被最佳化且該二輸出間的相位差係 180 度。因此，高共模拒斥比係與最佳化振幅和相位平衡特性曲線直接有關。

表格 1 顯示說明習知圖 1 的射頻平衡-不平衡轉換器配置(交錯式導線)及圖 6 本發明實施例的射頻平衡-不平衡轉換器配置(內部和外部導線)間的差異的各種參數比較圖。

	圖 1	圖 6
耦合係數	0.65	0.44
頻寬(千兆赫)	3.85	1.90
插入損失(分貝)	0.75	0.94

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共模拒斥比(分貝)	25.9	36.8
振幅不平衡(分貝)	0.90	0.12
相位不平衡(度)	2.4	1.8

表格 1-圖 1 和圖 6 的參數比較

圖 9 顯示的是以分貝表示的共模增益相對於以千兆赫表示的頻率波形圖。針對圖 6 本發明實施例的射頻平衡-不平衡轉換器配置(內部和外部導線)，線 200 代表量測共模增益，而線 202 代表模擬共模增益。注意，例如 1.81 千兆赫的帶通中的共模拒斥比係約-35.0 分貝，其約高於習知圖 1 約射頻平衡-不平衡轉換器配置(交錯式導線)10 分貝。增加的共模拒斥比係部分貢獻於本發明配置中使用內部和外部導線而減少的電容性耦合。

儘管已詳述本發明一或更多實施例，然而熟習該項技術者將理解到，該些實施例的修改可被進行而不偏離下列申請專利範圍所述的本發明範圍。

【圖式簡單說明】

圖 1 係具有第一和第二互相捲繞線圈的傳統平衡-不平衡轉換器。

圖 2 說明具有不同類型封裝安裝於它表面的印刷電路板。

圖 3a 至圖 3c 說明安裝至該印刷電路板的代表性半導體封裝的進一步細節。

圖 4 說明具有形成於該作用表面上的整合被動元件的

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半導體晶粒。

圖 5 說明具有連接至功率放大器和收發器的整合射頻平衡-不平衡轉換器的無線通訊系統。

圖 6 說明該整合射頻平衡-不平衡轉換器的進一步細節。

圖 7 說明該射頻平衡-不平衡轉換器的示意電路圖。

圖 8 說明該整合射頻平衡-不平衡轉換器的另一實施例。

圖 9 係該整合射頻平衡-不平衡轉換器的共模增益對頻率的波形圖。

【主要元件符號說明】

10	射頻平衡-不平衡轉換器
12	導線或線圈
14	導線或線圈
16	埠
18	埠
20	電容器
24	埠
26	埠
28	電容器
30	中心閥門
32	導線
50	電子裝置

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52	印刷電路板
54	導線
56	打線封裝
58	覆晶封裝
60	球狀柵格陣列
62	凸塊晶片載體
64	雙列式封裝
66	平面柵格陣列
68	多晶片模組
70	四邊扁平無接腳封裝
72	四邊扁平封裝
74	半導體晶粒
76	接觸墊片
78	中間載體
80	導體接腳
82	接線
84	密封劑
88	半導體晶粒
90	載體
92	底膠或環氧樹脂黏性材料
94	接線
96	接觸墊片
98	接觸墊片
100	密封化合物或密封劑

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102	接觸墊片
104	凸塊
106	中間載體
108	作用區
110	凸塊
112	凸塊
114	訊號線
116	密封化合物或密封劑
120	半導體晶粒或封裝
122	半導體基板
124	作用區
126	無線通訊系統
128	射頻積體電路
130	埠
132	收發器
134	埠
136	埠
140	整合式射頻平衡-不平衡轉換器
142	導線或線圈
144	埠
146	埠
148	電容器
150	導線或線圈
152	埠

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154	埠
156	電容器
170	整合式射頻平衡-不平衡轉換器
172	導線
174	埠
176	埠
178	電容器
180	中心閥門
182	電源匯流排
184	導線
190	導線或線圈
192	埠
194	埠
196	電容器
200	代表量測共模增益的線
202	代表模擬共模增益的線

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201206059

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※申請案號：100108685

※申請日：100.3.15　※IPC分類：H03H 11/32 (2006.01)

一、發明名稱：（中文/英文）

半導體裝置和形成具有減少的電容性耦合和高 CMRR 的 RF 平衡-不平衡轉換器的方法

SEMICONDUCTOR DEVICE AND METHOD OF FORMING RF BALUN HAVING REDUCED CAPACITIVE COUPLING AND HIGH CMRR

二、中文發明摘要：

一種半導體裝置具有形成於一基板上的一射頻平衡-不平衡轉換器。該射頻平衡-不平衡轉換器包含捲繞的第一導線，以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性。一第一電容器係耦接於該第一導線的第一及第二末端之間。一第二導線被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性。該第一導線係完全地形成於該第二導線內。該第一導線及該第二導線可具有相隔 50 微米的橢圓形、圓形或多邊形外形。一第二電容器係耦接於該第二導線的第一及第二末端之間。

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三、英文發明摘要：

A semiconductor device has an RF balun formed over a substrate. The RF balun includes a first conductive trace wound to exhibit inductive properties with a first end coupled to a first terminal of the semiconductor device and second end coupled to a second terminal of the semiconductor device. A first capacitor is coupled between the first and second ends of the first conductive trace. A second conductive trace is wound to exhibit inductive properties with a first end coupled to a third terminal of the semiconductor device and second end coupled to a fourth terminal of the semiconductor device. The first conductive trace is formed completely within the second conductive trace. The first conductive trace and second conductive trace can have an oval, circular, or polygonal shape separated by 50 micrometers. A second capacitor is coupled between the first and second ends of the second conductive trace.

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七、申請專利範圍：

1.一種半導體裝置，包括：

一基板；及

一形成於該基板上的平衡-不平衡轉換器，該平衡-不平衡轉換器包含：

(a)被捲繞以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性的一第一導線，

(b)耦接於該第一導線的第一及第二末端之間的一第一電容器，

(c)被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性的一第二導線，該第一導線係完全形成於該第二導線內，及

(d)耦接於該第二導線的第一及第二末端之間的一第二電容器。

2.如申請專利範圍第1項之半導體裝置，其中，該第一導線及第二導線係相隔50微米。

3.如申請專利範圍第1項之半導體裝置，其中，該第一導線及第二導線每一個具有一橢圓形、圓形或多邊形外形。

4.如申請專利範圍第1項之半導體裝置，其中，該第一導線及第二導線具有介於0.2至0.45之間的一耦合係數。

5.如申請專利範圍第1項之半導體裝置，進一步包含：

一中心閥門，耦接於該第二導線的第一及第二末端之

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間；及

一直流偏壓，耦接至該中心閥門。

6.一種半導體裝置，包括：

一基板；

一內部導線，形成於該基板上且被捲繞以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性；及

一外部導線，形成於該基板上且被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性，該內部導線係形成於該外部導線內。

7.如申請專利範圍第6項之半導體裝置，進一步包含：

一第一電容器，形成於該基板上且耦接於該內部導線的第一及第二末端之間；及

一第二電容器，形成於該基板上且耦接於該外部導線的第一及第二末端之間；

8.如申請專利範圍第6項之半導體裝置，其中，該內部導線及外部導線係相隔50微米。

9.如申請專利範圍第6項之半導體裝置，其中，該內部導線及外部導線每一個具有一橢圓形、圓形或多邊形外形。

10.如申請專利範圍第6項之半導體裝置，進一步包含耦接於該外部導線的第一及第二末端之間的一中心閥門。

11.如申請專利範圍第10項之半導體裝置，進一步包含耦接至該中心閥門的一直流偏壓。

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12.一種半導體裝置，包括：

一基板；

一第一電感器，形成於該基板上；及

一第二電感器，形成於該基板上，該第一電感器係形成於該第二電感器內。

13.如申請專利範圍第12項之半導體裝置，其中，該第一電感器包含被捲繞以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性的一第一導線。

14.如申請專利範圍第13項之半導體裝置，其中，該第二電感器包含被捲繞以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性的一第二導線。

15.如申請專利範圍第14項之半導體裝置，其中，該第一導線及第二導線係相隔50微米。

16.如申請專利範圍第14項之半導體裝置，進一步包含：

一第一電容器，形成於該基板上且耦接於該第一導線的第一及第二末端之間；及

一第二電容器，形成於該基板上且耦接於該第二導線的第一及第二末端之間；

17.如申請專利範圍第14項之半導體裝置，其中，該第一導線及第二導線具有介於0.2至0.45之間的一耦合係數。

18.如申請專利範圍第14項之半導體裝置，其中，該第

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一導線及第二導線每一個具有一橢圓形、圓形或多邊形外形。

19.如申請專利範圍第 14 項之半導體裝置，進一步包含：

一中心閥門，耦接於該第二導線的第一及第二末端之間；及

一直流偏壓，耦接至該中心閥門。

20.一種形成一半導體裝置的方法，包括：

提供一基板；

在該基板上形成一捲繞的內部導線以展示具有耦接至該半導體裝置的第一接頭的第一末端及耦接至該半導體裝置的第二接頭的第二末端的電感特性；及

在該基板上形成一捲繞的外部導線以展示具有耦接至該半導體裝置的第三接頭的第一末端及耦接至該半導體裝置的第四接頭的第二末端的電感特性，該內部導線係形成於該外部導線內。

21.如申請專利範圍第 20 項之方法，進一步包含：

在該基板上形成耦接於該內部導線的第一及第二末端之間的一第一電容器；及

在該基板上形成耦接於該外部導線的第一及第二末端之間的一第二電容器；

22.如申請專利範圍第 20 項之方法，其中，該內部導線及外部導線係相隔 50 微米。

23.如申請專利範圍第 20 項之方法，其中，該內部導線

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及外部導線每一個具有一橢圓形、圓形或多邊形外形。

24.如申請專利範圍第 20 項之方法，進一步包含：

提供耦接於該外部導線的第一及第二末端之間的一中心閥門；及

連接一直流偏壓至該中心閥門。

25.如申請專利範圍第 20 項之方法，其中，該第一導線及第二導線具有介於 0.2 至 0.45 之間的一耦合係數。

八、圖式：

(如次頁)

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及外部導線每一個具有一橢圓形、圓形或多邊形外形。

24.如申請專利範圍第 20 項之方法，進一步包含：

提供耦接於該外部導線的第一及第二末端之間的一中心閥門；及

連接一直流偏壓至該中心閥門。

25.如申請專利範圍第 20 項之方法，其中，該第一導線及第二導線具有介於 0.2 至 0.45 之間的一耦合係數。

八、圖式：

(如次頁)

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1002, p. 108 of 466

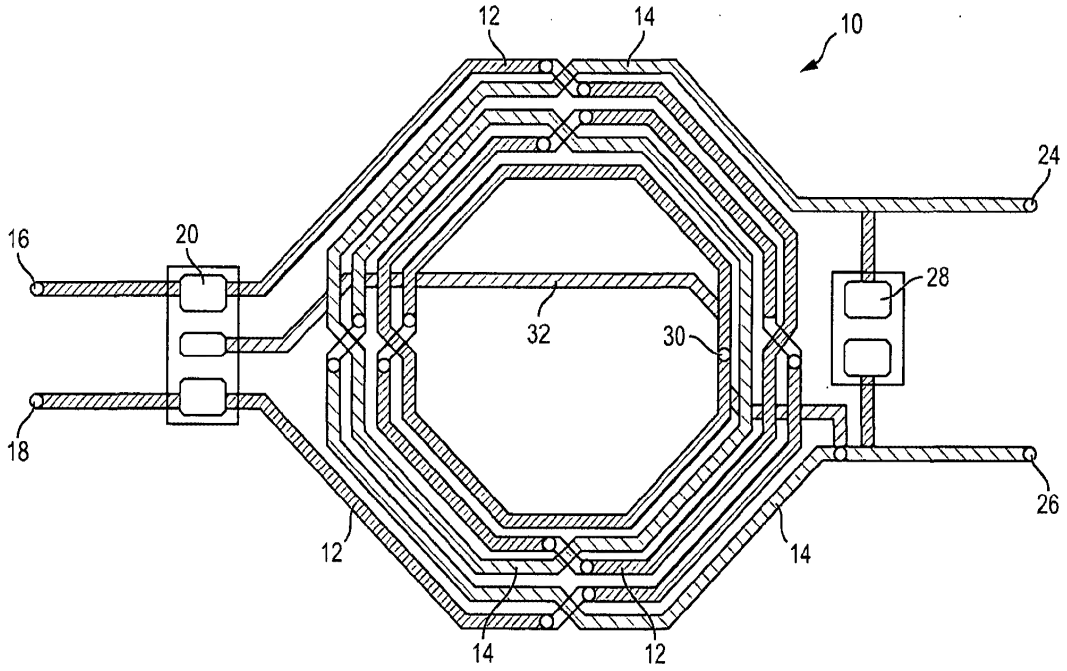


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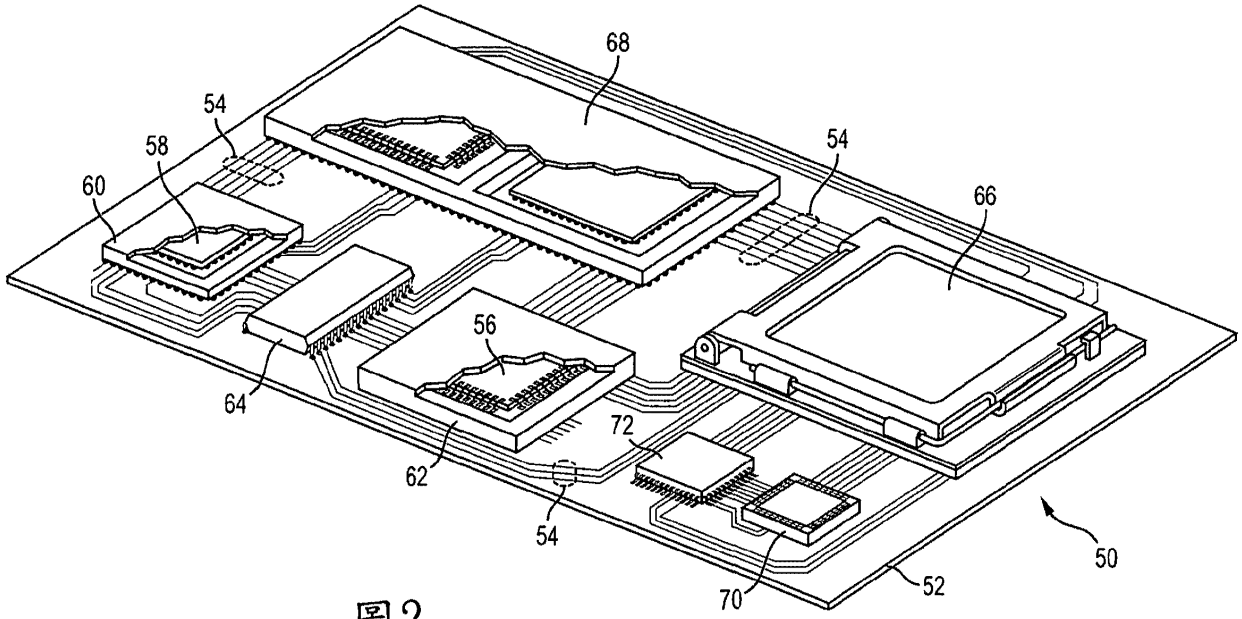


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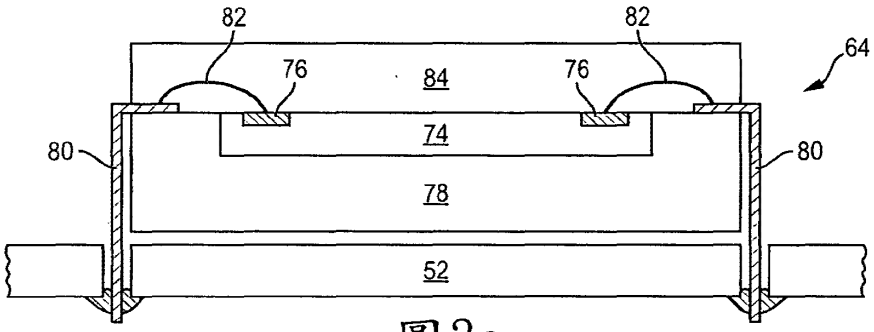

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圖3a

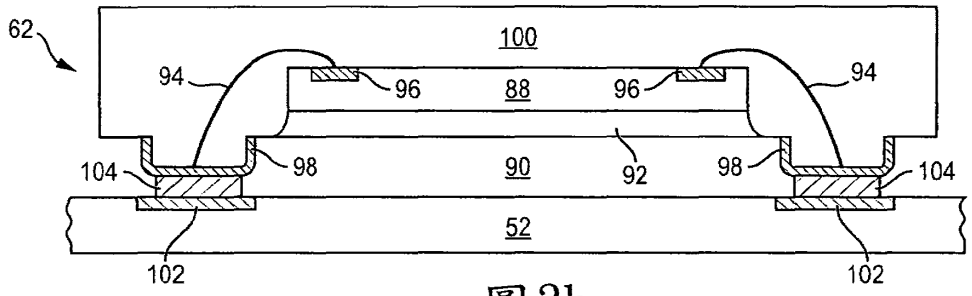

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圖3b

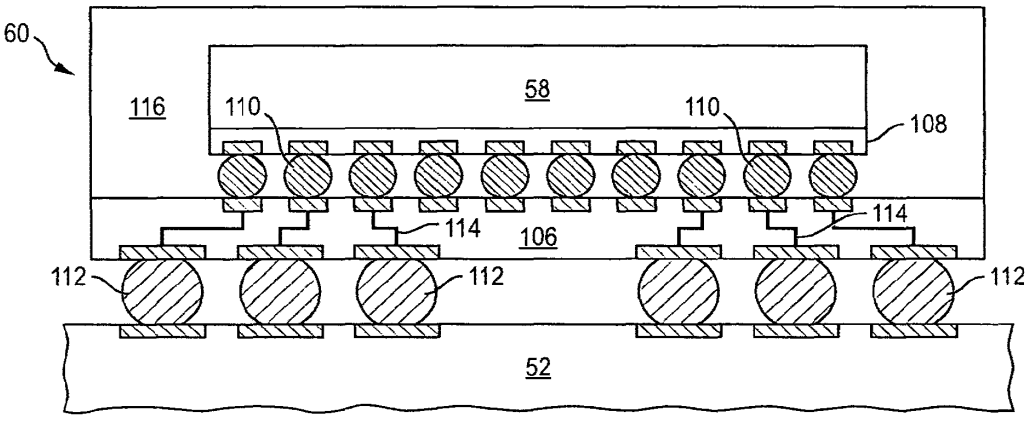

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圖3c

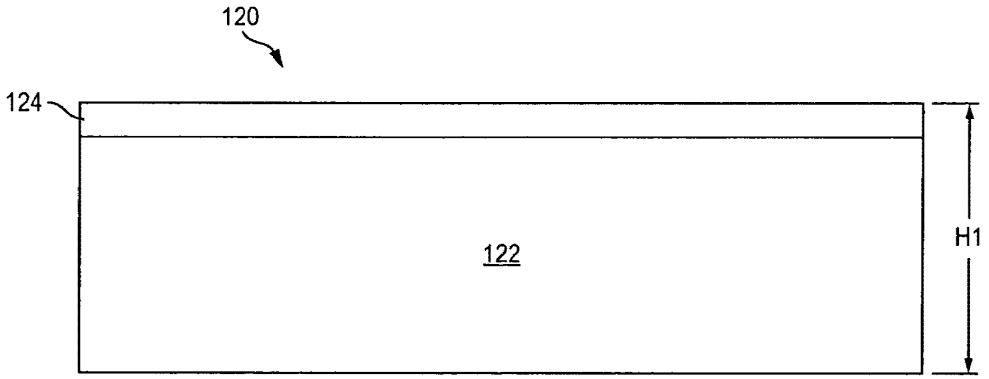

120
124
122
H1

圖4

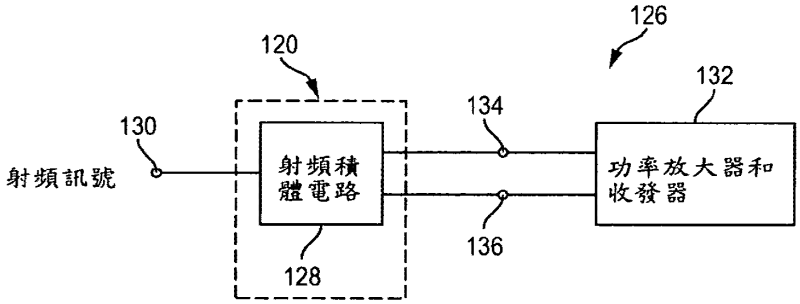

126
120
132
134
130
射頻訊號
射頻積體電路
功率放大器和收發器
136
128

圖5

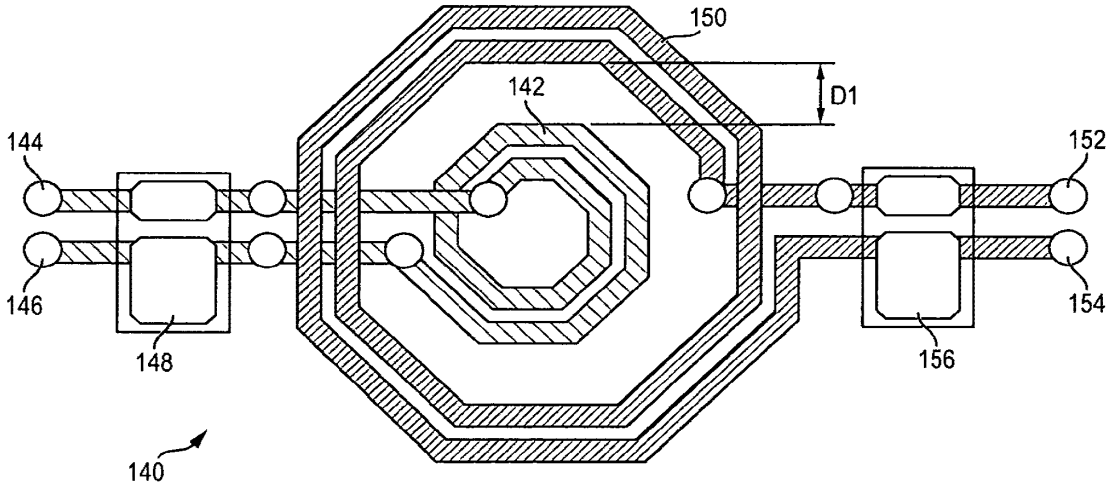

150
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圖6

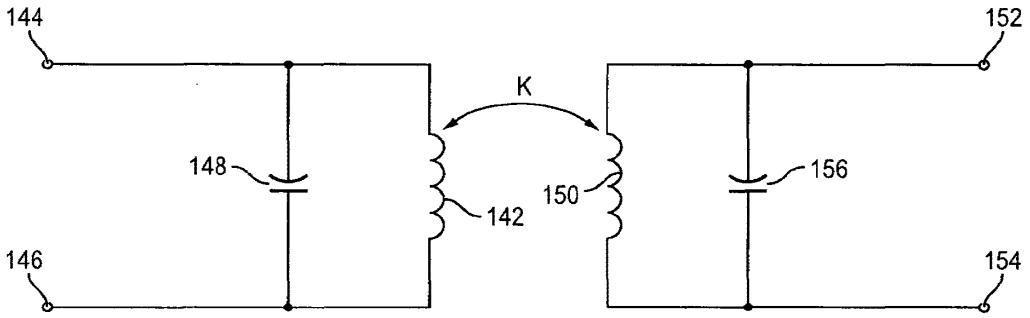

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圖7

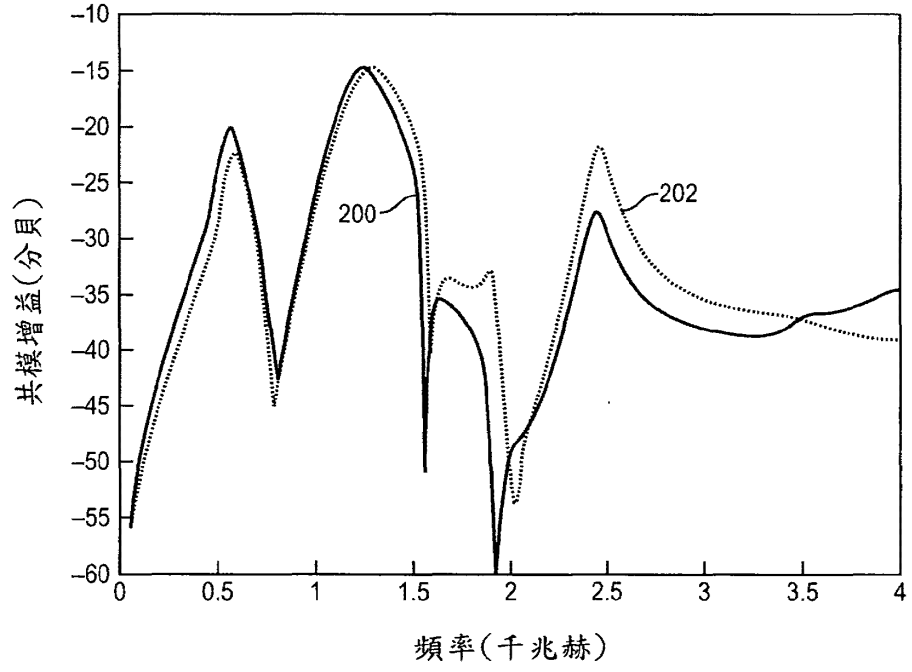

-10
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
共模增益(分貝)
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202
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0.5
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1.5
2
2.5
3
3.5
4
頻率(千兆赫)

圖9

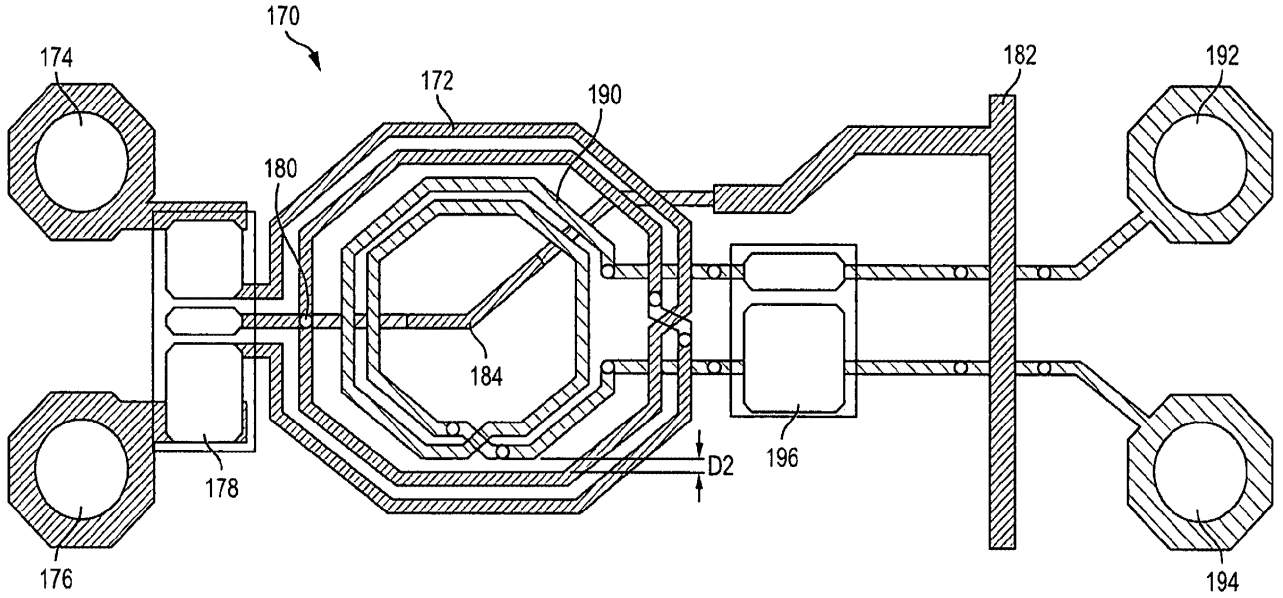


圖8

四、指定代表圖：

(一)本案指定代表圖為：圖6。

(二)本代表圖之元件符號簡單說明:

140	整合式射頻平衡-不平衡轉換器
142	導線或線圈
144	埠
146	埠
148	電容器
150	導線或線圈
152	埠
154	埠
156	電容器

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

Search terms：(1) (201003883)@PN 【 明細 】

Patent/Publication Number	201003883 Patent I473238
Title	On-chip integrated voltage-controlled variable inductor, methods of making and turning such variable inductors, and design structures integrating such variable inductors
Issued/Publication Date	2010/01/16
Application Date	2009/01/17
Application Number	098101836 Espacenet
IPC	H01L-023/58(2006.01)
Inventor	DING, HAN-YI CN; MINA, ESSAM F. US; WOODS, WAYNE H. US
Applicant	INTERNATIONAL BUSINESS MACHINES CORPORATIONUS
Individual	F
Priority Number	20080129 US 20080021339
Abstract	On-chip integrated variable inductors, methods of making and tuning an on-chip integrated variable inductor, and design structures embodying a circuit containing the on-chip integrated variable inductor. The inductor generally includes a signal line configured to carry an electrical signal, a ground line positioned in proximity to the signal line, and at least one control unit electrically coupled with the ground line. The at least one control unit is configured to open and close a current path connecting the ground line with a ground potential so as to change an inductance of the signal line.

Information on this system is for reference only, it cannot be used as grounds for approval or rejection.
In all instances of discrepancy, official publication from TIPO shall prevail and should be consulted.

(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201003883 A1
(43)公開日： 中華民國 99 (2010) 年 01 月 16 日

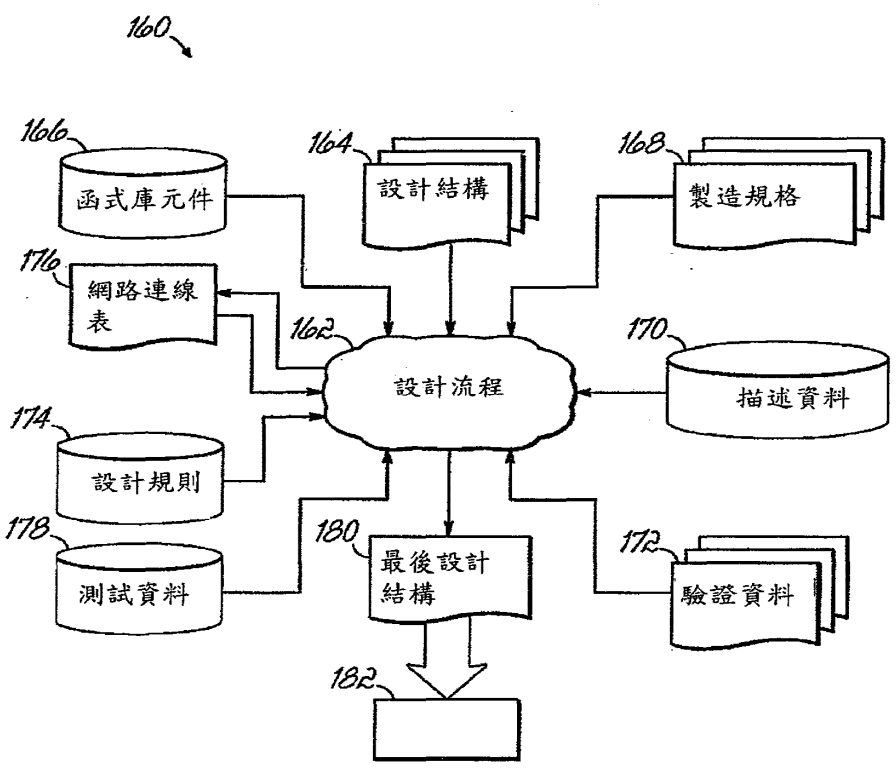
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(54)名稱

晶片整合之壓控可變電感，製造與調整此可變電感之方法，以及整合此可變電感之設計結構
ON-CHIP INTEGRATED VOLTAGE-CONTROLLED VARIABLE INDUCTOR, METHODS OF MAKING AND TURNING SUCH VARIABLE INDUCTORS, AND DESIGN STRUCTURES INTEGRATING SUCH VARIABLE INDUCTORS

(57)摘要

揭露關於晶片整合可變電感、製造與調整晶片整合可變電感之方法、以及實施一包含晶片整合可變電感之電路的設計結構。電感通常包括一經組態以裝載一電子信號之信號線、一位於靠近信號線處之接地線、以及經電氣耦接於接地線之至少一控制單元。至少一控制單元係經組態以斷接與接通將接地線連接於接地電位之電流路徑，以致於改變信號線之電感性。



160：設計流
162：設計流程
164：設計結構
166：函式庫元件
168：製造規格
170：描述資料
172：驗證資料
174：設計規則
176：網路連線表
178：測試資料檔案
180：最後設計結構
182：階段

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(12)發明說明書公開本 (11)公開編號：TW 201003883 A1
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揭露關於晶片整合可變電感、製造與調整晶片整合可變電感之方法、以及實施一包含晶片整合可變電感之電路的設計結構。電感通常包括一經組態以裝載一電子信號之信號線、一位於靠近信號線處之接地線、以及經電氣耦接於接地線之至少一控制單元。至少一控制單元係經組態以斷接與接通將接地線連接於接地電位之電流路徑，以致於改變信號線之電感性。

六、發明說明：

【發明所屬之技術領域】

本發明是有關於積體電路，更特定來說，是有關於積體電路之晶片整合可變電感，實施此晶片整合可變電感之設計結構，製造此晶片整合可變電感之方法，以及在電路運作期間調整晶片整合可變電感之方法。

【先前技術】

電感是見於許多積體電路之一被動電子裝置，積體電路包括射頻積體電路(RFIC)、多頻帶被動匹配網路、多頻帶壓控振盪器(VCO)儲槽電路、以及相位延遲單元。電感可被單獨用在積體電路中或是以成對方式配置為積體電路內之差動電感或變壓器。一般來說，電感是一反應性元件，其可儲存其磁場中的能量並傾向抵抗流經其之電流流動量的改變。電感的效能會顯著影響相關積體電路之整體效能，電感甚至可能成為一效能限制元件。晶片電感或是單片電感通常會在相同的基底(substrate)上製造以作為相關積體電路的其餘部份。電感可以一傳統的金屬氧化半導體(MOS)製程或是先進矽鍺(SiGe)製程來加以製造。

晶片電感的重要參數包括電感值、Q(品質因子)、共振頻率(電感與電容值)、以及晶片面積，在積體電路中所有的這些參數都需要被最佳化。品質因子 Q 是關於積體

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電路內之電感效能的一通常被接受之指標，並且代表了在電感內能量損失與能量儲存間之關係的量測。高數值的Q係反應出一低的基底損失與一低的串聯電阻值。

晶片電感可為一平面形式(包括直線種類與平面螺旋種類)或一螺旋形式，並具有固定或可變的電感值。混合信號與射頻應用通常會需要可變的反應性元件(例如電感或電容)來完成調整、頻帶切換、鎖相迴路功能等等。此等反應性元件通常被用在某些種類的電路內，在此電路內反應性元件係與其他的反應性元件共振。所欲之結果為一具有如下反應之共振電路：可動態地從一頻率調整到另一頻率。一達成之方法係在電路設計中建立將一額外長度之導體切換至晶片可變電感之信號線的能力。導體的額外長度可被串聯或並聯於導體的原本長度。電感信號線之加長會改變其電感值。然而，傳統的配置方式係需要可變電感之信號線內的某些切換，對於許多混合信號與射頻應用來說，會使得Q值惡化到一無法接受的低數值。

因此，晶片可變電感的改良結構被需要以克服而不具有傳統可變電感的此等缺點或其他缺點。

【發明內容】

在一實施例中，一晶片整合可變電感包含一經組態以裝載一電子信號之信號線、一位於靠近信號線處之接地

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線、以及被放置在一電流路徑上之至少一控制單元，該電流路徑係將接地線連接於接地電位。該至少一控制單元係經組態以選擇性地斷接與接通該電流路徑，以致於當該電流路徑被斷接時該信號線具有一第一電感值，以及當該電流路徑被接通以將該接地線耦接於該接地電位時該信號線具有一第二電感值。

該晶片整合可變電感之信號線係被電氣耦接於該晶片上所製造之一積體電路。該晶片整合可變電感之電感值可被修正而無需改變該信號路徑、加長該信號線、或是安裝一電感器至該信號線。反而是，當該晶片上之該積體電路被供電或運作時，藉由將被放置在靠近該信號線處之一或多接地線之接地，該可變電感之電感值可被修改或調整。

在另一實施例中，用以製造一晶片整合可變電感之一方法係被提供。該方法包含：在一晶片上製造一信號線，該信號線係電氣耦接於該晶片上之一積體電路。該方法另包含：製造一足夠靠近該信號線之接地線，以致於當該接地線在一電流路徑上耦接於一接地電位時該信號線具有一第一電感值，以及當該電流路徑被斷接時該信號線具有一第二電感值。該方法另包含：製造至少一控制單元，經組態以選擇性地斷接或接通該電流路徑。該接地線與該信號線可被放置在一共同金屬化層中，或可被放置在不同的金屬化層中。

又在另一實施例中，用以在經電氣耦接於該可變電感

之一積體電路的操作期間來調整一晶片整合可變電感之方法係被提供。該方法包含：自該積體電路引導一電子信號通過該可變電感之一信號線。該方法另包含：選擇性地將足夠靠近該信號線之該至少一接地線接地，以改變該信號線之一電感值。

又在另一實施例中，一設計結構係被提供，該設計結構係被實施在一機器可讀媒體內，用以設計與製造一電路。該電路包含一晶片整合可變電感，該晶片整合可變電感包括一信號線圈及一接地線，該信號線係經組態以裝載一電子信號，該接地線係位於靠近該信號線處。該電路另包含至少一控制單元，該至少一控制單元係被放置在一電流路徑上，該電流路徑係將該接地線連接於一接地電位。該至少一控制單元係被組態以選擇性地斷接與接通該電流路徑，以至於當該電流路徑被斷接時該信號線具有一第一電感值，以及當該電流路徑被接通以將該接地線耦接於該接地電位時該信號線具有一第二電感值。該電路與該電路結構係位於設計檔案內或設計結構內(例如 GDSII 檔案)，其可被轉換至設計公司、製造商、客戶、或其他第三方。

【實施方式】

請參照第 1A 圖至第 1B 圖，一晶片整合可變電感(被概括標示為參考編號 10)係由一信號線 12 所組成，信號線

12係以一條導電材料之一代表形式來呈現，此條導電材料被埋入一介電材料之一絕緣層 14(第 1B 圖)內或被絕緣層 14 所包圍。電感 10 係置於一基底 16 上，基底 16 包括在其上及(或)其內所形成之至少一積體電路，而積體電路帶有具零件(feature)(零件 18 與 20 為代表，其被接觸於信號線 12)之該等裝置。零件 18 與 20 可包含金屬化線、接點、半導體材料、及(或)先前已形成在基底 16 上面及(或)裡面的電路元件之零件。基底 16 通常是包含一小塊半導體晶圓(包含一整個積體電路之一晶片或晶粒(die)。

位於信號線 12 相反兩端之埠或端點 22 與 24 係藉由導電路徑 21 與 23(位於絕緣層 14 以及位於任何中間的介電層(例如像是介電層 25 與 27))來被電氣耦合於基底 16 上之零件 18 與 20。一電子信號係由基底 16 上之積體電路傳送至信號線 12。或者是，端點 22 與 24 可藉由在上面的金屬化層(未顯示)之導電路徑 21 與 23 來被耦合於基底 16 上之其他電路。

電感 10 之一接地線 26 係被放置在信號線 12 與基底 16 之間。接地線 26 係為直線條狀之導電材料，其被埋入絕緣層 25(第 1B 圖)並被絕緣層 25 所包圍。接地線 26(通常是在信號線 12 之下)係藉由至少絕緣層 14 與 25(其係提供電氣絕緣)之一部份的介電材料來與信號線 12 隔離。在代表的實施例中，電感 10 僅包括一信號線 12，且接地線 26 係被放置成實質平行於信號線 12。

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接地線的相反兩端係構成接點 28 與 30，接點 28 與 30 係以一種可選擇的方式分別藉由控制單元 32 與 34 來與接地端電氣耦合。控制單元 32 與 34(被顯示為存在於基底 16 上)係藉由在絕緣層 25 以及任何其他中間的介電層(例如像是絕緣層 27)內之導電路徑 31 與 33 來實體連接於接點 28 與 30。控制單元 32 與 34 可以是任何壓控裝置，但並未被限制於場效電晶體(例如像是一 p 型金屬氧化半導體(PMOS)電晶體或一 n 型金屬氧化半導體(NMOS)電晶體)與正－本－負(p-i-n)二極體(其具有熟知技藝人士所了解之結構)之中。當控制單元 32 與 34 兩者被適當的壓控信號所斷接(open)時，接地線 26 係代表一開路或為電子浮接。當控制單元 32 與 34 在斷接狀態時，接地線 26 的存在並不會顯著影響信號線 12 的電感值。當控制單元 32 與 34 兩者被適當的壓控信號接通(close)時，接地線 26 係處於一閉迴路，此閉迴路係由一短路電路耦接至接地電位。被接地的接地線 26 對於信號線 12 的靠近會造成電感 10 之電感值的改變，如同以下所另述。

在一替代實施例中，接地線 26 之接點 28 與 30 之一者可被一直綁在接地電位，並且只有接地線 26 之接點 28 與 30 之另一者進行切換以完成此閉迴路之接地動作。在另一替代實施例中，接地線 26 可被分段，並且額外的控制單元可被加入以選擇性地將該等片段耦接在一起以調整接地線 26 的有效長度。舉例來說，接地線 26 可包含一中央接點(未顯示)(此中央接點係靠近接點 28 與 30 之

一中間點)、以及對於此中央接點之一額外控制單元(未顯示),用以當不同的接點組合被選擇時讓電感 10 具有兩個以上的電感值狀態。

藉由將接地線 26 與接地端耦合,控制單元 32 與 34 的操作對於電感 10 之電感值改變是有效的。當控制單元 32 與 34 被接通以及接地線 26 係藉由導電路徑 31 與 33 來被電氣耦合於接地端時,接地線 26 對於信號線 12 的靠近會降低電感 10 的電感值。此電感值之降低是二元的,因為:當控制單元 32 與 34 被斷接時,電感 10 具有一第一電感值;當控制單元 32 與 34 被接通時,電感 10 具有一第二電感值(第二電感值係小於第一電感值)。當控制單元 32 與 34 被接通時,接地線 26 變回到電感 10。電感 10 係可藉由電壓信號來以電子方式做調整,因為在基底 16 上之積體電路的操作期間,控制單元 32 與 34 可被斷接與接通。

接地線 26 的寬度 w_1 可以大於信號線 12 的寬度 w_2(其可運作以降低與基底 16 的耦合)。在一實施例中,接地線 26 的寬度 w_1 可以等於信號線 12 的寬度 w_2 乘以在信號線 12 與接地線 26 間之間隔的兩倍。或者是,信號線 12 與接地線 26 可以具有近似於相等的寬度,或是接地線 26 可以比信號線 12 窄。當控制單元 32 與 34 被接通以將接地線 26 連接於接地端時,接地線 26 之寬度 w_1 的降低會減少電感值的降低。信號線 12 與接地線 26 係藉由一縱橫比(代表線厚度與線寬度之比率)來加以表示。

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一般來說，接地線 26 的厚度 t_1 係小於信號線 12 的厚度 t_2，此係導致接地線 26 相較於信號線 12 具有一較小的縱橫比。信號線 12 與接地線 26 的長度係為近似地相等。當設計關聯於電感 10 之積體電路時，信號線 12 與接地線 26 的維度係被選擇。

信號線 12 與接地線 26 係為在成層堆疊之該等互連金屬線與該等貫孔內之零件，其係藉由傳統的後段製程(BEOL)處理(例如像是金屬鑲嵌製程以及雙重金屬鑲嵌製程)與對於基底 16 之積體電路上的一互連結構之定義來被製造於基底 16 上。舉例來說，信號線 12 可以是一置於 M5 層或 M6 層之金屬線，而接地線 26 可以是一置於 M12 層(比起對於接地線 12 之金屬化層更靠近基底 16)之金屬線。結果，絕緣層 14 通常會藉由中間的絕緣層(未顯示)(中間的絕緣層亦包含互連結構之該等導電零件)來與絕緣層 25 分開。典型地，在上面的金屬化層上，由 BEOL 處理所形成之金屬化零件通常會比形成於較低金屬化層上之金屬化零件還要厚，此即意味著信號線 12 可能比接地線 26 還要厚。

在一典型的製造程序中，藉由傳統的前段製程(FEOL)處理(亦即關聯於積體電路之該等半導體裝置之製造的處理)，於製造裝置直到第一 M1 層為止的期間內，零件 18 與 20、以及控制單元 32 與 34、以及關聯於電感 10 之積體電路係被形成於基底 16 內與基底 16 上。BEOL 處理被用來形成覆蓋在 M1 層上的每一金屬化層(M2

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層、M3 層等等)。特別是，BEOL 處理被用來在一較低金屬化層形成信號線 12 以及在一較高金屬化層形成接地線 26，以及形成經金屬填充之貫孔與形成用來定義導電路徑 21、23、31、33 之導電線。

為達到此目的，絕緣層 27 係被 BEOL 處理所使用與處理以定義經金屬填充之貫孔與導電線，而某些導電線係參與了導電路徑 21、23、31、33 的定義。絕緣層 25 係被使用在絕緣層 27 上，貫孔與溝槽(包括接地線 26 之一溝槽)係使用已知的石版印刷術與蝕刻技術來被定義於絕緣層 25 內，而溝槽與貫孔則以一所需導體來填充。在填充步驟後剩餘的任何額外負擔的導體係被平面化處理所移除，例如像是藉由一化學機械研磨(CMP)程序。如果有任何中間的金屬化層，則中間的金屬化層係使用 BEOL 處理來被應用。絕緣層 14 係被應用，貫孔與溝槽(包括信號線 12 之一溝槽)係使用已知的石版印刷術與蝕刻技術來被定義於絕緣層 14 之內，而溝槽與貫孔係被一所需導體所填充。在填充步驟後剩餘的任何額外負擔的導體係被平面化處理所移除，例如像是藉由一 CMP 程序。如果有任何覆蓋在上面的金屬化層的話，則覆蓋在上面的金屬化層接著使用 BEOL 處理來被應用以完成互連結構。

在本發明之一替代實施例中，接地線 26 可在 FEOL 處理過程中被形成於 M1 層。接著，上面的金屬化層(包括含有信號線 12 之金屬化層)係被應用如上所述。

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絕緣層 14、25、27 可包含熟知技藝人士所了解之任何有機或無機之介電材料，其可藉由任何個數的已知習知技術來加以沈積，例如像是濺鍍、旋轉塗佈應用、化學氣相沈積(CVD)程序、或電漿促進 CVD(PECVD)程序。用於絕緣層 14、25、27 之候選無機介電材料可包括(但不限於)二氧化矽、氟化矽玻璃(FSG)、以及這些介電材料的組合。該些絕緣層 14、25、27 之介電材料可由小於二氧化矽之介電常數(大約是 3.9)之一相關介電係數或介電常數所特述。絕緣層 14、25、27 之候選低 k 介電材料包括(但不限於)多孔性與非滲透性旋轉塗佈有機低 k 介電質(例如像是旋轉塗佈熱固聚芳香樹脂)、滲透性與非滲透性無機低 k 介電質(例如像是有機矽酸鹽玻璃、氫添加之矽碳氧化物(SiCOH)、碳摻雜氧化物)、以及有機與無機介電質之混合。來自此等低 k 材料之絕緣層 14、25、27 的製造係可運作以降低熟知技藝人士所能理解之經完成互連架構的電容。

對於信號線 12 與接地線 26 之合適導電材料包括(但不限於)銅(Cu)、鋁(Al)、這些金屬的合金、以及其他類似的金屬。這些金屬可藉由傳統的沈積製程(包括但不限於一 CVD 製程以及一電化學製程(像是電鍍以及非電鍍))來被沈積。一障壁層(未顯示)可覆蓋信號線 12 與接地線 26 之一或多邊。舉例來說，障壁層可包含由傳統沈積製程所應用之鉭與氮化鉭之雙層、或鉭或氮化鉭之雙層。導電路徑 21、23、31、33 可由相同於信號線 12 與接地

線 26 的材料、以及被熟知技藝人士所了解之額外種類的材料(像是鎢(W)以及矽化金屬)所組成。

基底 16 可以是由半導體材料(包括但不限於矽(Si)、矽鍺(SiGe)、絕緣層上矽元件(SOI)層、以及其他類似之含有矽的半導體材料)所組成之一半導體晶圓。或者是，基底 16 可包含對於熟知技藝人士來說已知之陶瓷基底(例如像是一石英晶圓或一 Al2O3-TiC(Al2O3-TiC)晶圓)或是其他種類的基底(例如像是 III-V 族化合物之半導體基底)。

在使用中以及繼續參照第 1A 圖至第 1B 圖，當控制單元 32 與 34 被切換到斷接二將基地線 26 置於一電子浮接狀態時，電感 10 係具有一第一電感值。在關聯的積體電路(包含電感 10)之操作過程中以及依據電感 10 之電感值調整的一需要，積體電路在適當的控制線(未顯示)上將該等電壓信號傳送至控制單元 32 與 34。該等電壓信號係作用以造成控制單元 32 與 34 改變狀態並接通一目前路徑(其透過導電路徑 31 與 33 來將接地線 26 連接於接地端)。舉例來說，電壓信號可電子地偏壓一場效電晶體或一 p-i-n 二極體(運作為控制單元 32 與 34)以導通各別源極/汲極區域之間的電流，其在接通電流路徑上將接地線 26 連接於一接地電位。接地線 26 之接地係運作以將電感 10 之電感值降低至一第二電感值(第二電感值係低於第一電感值)。結果，當關聯之積體電路運作時，電感 10 的電感值可被有效地調整；因此，電感值的改變係為可編程的。

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參照第 2A 圖與第 2B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 38 係修正電感 10(第 1A 圖與第 1B 圖)之結構，藉由引入接地線 26 以外之接地線 40 與 42 來納入多條接地線。類似於接地線 26，接地線 40 與 42 為直線條狀之導電材料，其被埋入絕緣層 25，用以讓接地線 26 在一側有接地線 40，在另一側有接地線 42。接地線 40 與 42 亦被放置在信號線 12 與基底 16 之間，並與接地線 26 處於相同的金屬化層以及以上關於接地線 26 所述之方式所形成。

藉由絕緣層 14 之介電材料部分，接地線 40 與 42 係與彼此、接地線 26、以及信號線 12 電氣絕緣。接地線 40 與 42 亦由相同的 BEOL 製程技術所形成，並與接地線 26 來自相同的 BEOL 冶金術，並通常與接地線 26 一起形成。接地線 40 與 42 與信號線 12 之維度上的關係可類似於信號線 12 與接地線 26 之維度上的關係。然而，各別接地線 26、40、42 之寬度及(或)厚度可不相同。

接地線 26 的相反兩端係構成接點 28 與 30，接點 28 與 30 分別藉由控制單元 32 與 34 以一可選擇方式以電流路徑來被電氣耦合於接地端。控制單元 32 與 34(其被描述為位於基底 16 上)係藉由絕緣層 25 內與任何其他中間介電層(例如絕緣層 27)內之導電路徑 31 與 33 來被實體連接於接點 28 與 30。

接地線 40 的相反兩端係構成接點 44 與 46，接點 44

與46分別藉由控制單元48與50以一可選擇方式來被電氣耦合於接地端。接地線42的相反兩端係構成接點52與54，接點52與54分別藉由控制單元56與58以一可選擇方式來被電氣耦合於接地端。當控制單元48與50以及控制單元56與58(具有類似於控制單元32與34之一結構)被共同接通時，係以一類似於控制單元32與34關於接地線26操作之方式運作，以各別及絕緣的電流路徑來選擇性地將各別接地線40與42連接至接地端。控制單元48、50、56、58可位於基底16上，並藉由相似於導電路徑31與33(第1B圖)之導電路徑(未顯示)耦合於各別的接地線40與42。為簡潔說明起見，導電路徑21、23、31、33係省略於第2B圖。

控制單元32與34、48與50、56與58之操作係作用以藉由將接地線26、40、42各別耦合於接地端，或者是藉由將接地線26、40、42之不同組合耦合於接地端，來改變電感38的電感值。當一或多組控制單元32與34、48與50、或56與58被接通時，被接地之一或多接地線26、40、42對於信號線12的靠近會降低電感38的電感值。相較於電感10(第1A圖與第1B圖)的二元維持，電感值之不同降低量係正比於經切換接地線26、40、42之數量。舉例來說，三接地線26、40、42之可選擇接地係允許電感38有八個不同的電感值，這些不同的電感值可僅藉由斷接與接通控制單元32與34、控制單元48與50、控制單元56與58、與在此之組合來被選擇。

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參照第 3A 圖與第 3B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 60 包括接地線 62 與 64，而非見於電感 10(第 1A 圖與第 1B 圖)之接地線 26。類似於接地線 26，接地線 62 與 64 係由直線條狀之導電材料所組成，其被埋入絕緣層 14，用以讓信號線 12 在一側有接地線 62，在另一側有接地線 64。接地線 62 與 64 係位於和信號線 12 相同之金屬化層內。藉由部份的絕緣層 14，接地線 62 與 64 係彼此電氣絕緣、以及與信號線 12 電氣絕緣。接地線 62 與 64 亦藉由相同的 BEOL 製程技術所形成，並來自與信號線 12 相同的 BEOL 冶金術，並通常與信號線 12 一起形成。接地線 62、64 與信號線 12 之維度上的關係可類似於信號線 12 與接地線 26 之維度上的關係(第 1A 圖與第 1B 圖)。然而，接地線 62 與 64 之每一者係具有不同的寬度。

接地線 62 的相反兩端係構成接點 66 與 68，接點 66 與 68 係以一種可選擇的方式分別藉由控制單元 70 與 72 以一電流路徑來與接地端電氣耦合。接地線 64 的相反兩端係構成接點 74 與 76，接點 74 與 76 係以一種可選擇的方式分別藉由控制單元 78 與 80 以另一電流路徑來與接地端電氣耦合。當控制單元 70 與 72 以及控制單元 78 與 80(具有類似於控制單元 32 與 34 之一結構)被共同接通時，係以一類似於控制單元 32 與 34 關於接地線 26 操作之方式運作，以各別及絕緣的電流路徑來選擇性地將

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各別接地線 62 與 64 耦合至接地端。控制單元 70、72、78、80 可位於基底 16 上並且藉由類似於導電路徑 31 與 33(第 1B 圖)之導電路徑(未顯示)來與各別的接地線 62 與 64 耦合。為簡潔說明起見，導電路徑 21、23、31、33 係被忽略於第 3B 圖。

控制單元 70 與 72 以及控制單元 78 與 80 的操作係作用以藉由將接地線 62、64 各別耦合於接地端，或者是藉由將接地線 62、64 二者皆耦合於接地端，來改變電感 60 的電感值。當一或二組之控制單元 70 與 72、或 78 與 80 被接通時，被接地之接地線 62、64 對於信號線 12 的靠近會降低電感 60 的電感值。接地線 62 與 64 之可選擇接地係允許電感 60 有三種不同的電感值，這些不同的電感值可僅藉由斷接與接通控制單元 70 與 72、以及控制單元 78 與 80 來被選擇。

在一替代性實施例中，一電容屏(未顯示)可使用介於接地線 62 與 64 之一或兩者以及信號線 12 間之一串貫孔來定義。選擇性的電容屏係以類似於電容屏 106(第 6A 圖與第 6B 圖)之方式運作。

參照第 4A 圖與第 4B 圖(在此，相似的參考編號係代表在第 2A 圖與第 2B 圖中以及第 3A 圖與第 3B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 81 包括接地線 26、40、42(該等接地線係在與信號線 12 不同之金屬化層)以及接地線 62、64(該等接地線係在與信號線 12 相同之金屬化層)。因此，藉由連接不同的

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接地線 26、40、42、62、64 或排列或組合，電感 81 之電感值可被切換到正比於其個數之多個不同電感值。在一實施例中，接地線 26 可被切換到接地處，而其他的接地線 40、42、62、64 不是被單獨切換就是被一起切換，以調整電感 81。在此實施例中，電感 81 可垂直地與水平地調整。為簡潔說明起見，導電路徑 21、23、31、33 未省略於第 4B 圖中。

參照第 5A 圖與第 5B 圖(在此，相似的參考編號係代表相似於第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 82 係修正電感 10(第 1A 圖與第 1B 圖)之結構係藉由除了接地線 26 以外之接地線 84 與 86 的引入，來納入一堆疊之接地線。類似於接地線 26，接地線 84 與 86 係為直線條狀之導電材料，其被安置入絕緣層 83 與 85，用以讓接地線 84 介於接地線 26 與信號線 12 之間而接地線 26 則是介於接地線 84 與接地線 86 之間。絕緣層 83 與 85 係類似於絕緣層 14 與 25，並與絕緣層 25 一起堆疊。接地線 84 可位於一金屬化層，此金屬化層係介於包含信號線 12 與接地線 26 之該等金屬化層之間；而接地線 26 可位於一金屬化層，此金屬化層係介於包含接地線 84 與接地線 86 之該等金屬化層之間。舉例來說，信號線 12 可為一置於 M6 層之金屬線，接地線 86 可為一置於 M2 層之金屬線，接地線 26 可為一置於 M3 層之金屬線，以及接地線 84 可為一置於 M4 層之金屬線。

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至少藉由絕緣層 14、25、83、85 之部份，讓接地線 84 與 86 與彼此、接地線 26、以及信號線 12 電氣絕緣。該等接地線 84 與 86 亦可由相同的 BEOL 製程技術所形成，並與接地線 26 來自相同的 BEOL 冶金術。接地線 84、86 與信號線 12 之維度關係可類似於信號線 12 與接地線 26 間之維度關係；然而，如第 5A 圖與第 5B 圖所示，接地線 84、86、26 之每一者可具有不同的寬度及(或)厚度。

接地線 84 之相反兩端係構成接點 88 與 90，接點 88 與 90 係分別藉由控制單元 92 與 94 以一可選擇方式依一電流路徑來電氣耦接於接地端。接地線 86 之相反兩端係構成接點 96 與 98，接點 96 與 98 係分別藉由控制單元 100 與 102 以一可選擇方式依另一電流路徑來電氣耦接於接地端。當被致動時，控制單元 92、94 與控制單元 100、102(具有類似於控制單元 32、34 之結構)以一類似於控制單元 32、34 對於接地線 26 之操作方式來運作，以選擇性地將個別接地線 84、86 耦接於接地端。控制單元 92、94、100、102 可位於基底 16 上，並藉由類似於導電路徑 31、33(第 1B 圖)之導電路徑(未顯示)來與各別接地線 84、86 耦接。為簡潔說明起見，導電路徑 21、23、31、33 係被忽略於第 5B 圖。

藉由將接地線 84、86、26 分別與一接地電位耦接之方式，或者是藉由將接地線 84、86、26 之不同組合與接地電位耦接的替代方式，控制單元 32、34 與控制單元 92、

94及控制單元100、102之操作係有效改變電感82的電感值。當控制單元32、34與控制單元92、94及控制單元100、102之一或多組被接通時，經接地之接地線84、86、26之一或多組對於信號線12的靠近會降低電感82的電感值。電感值之不同降低的量係正比於經切換之接地線84、86、26的個數。舉例來說，接地線84、86、26之選擇性接地係允許電感82有一個不同的電感值，此等電感值可僅藉由斷接或接通該等單元32、34與控制單元92、94及控制單元100、102之方式以選擇。

當沒有任何接地線26、84、86被耦接至接地端時，電感82的電感值被最大化。接地線26、84、86之一或多者與接地端之耦接係運作以降低電感82之電感值。若最接近信號線12之接地線84耦接於接地端並且接地線84與下層接地線26與86之任一者亦耦接於接地端，則不論接地線26與86之任一者是否亦耦接於接地端，電感82之電感值係被最小化。

類似於電感38之接地線26、40、42(第2A圖與第2B圖)，電感82在與接地線26、84、86之一或多者相同的金屬化層內可另包括額外的接地線(未顯示)。或者是，類似於電感60之接地線62、64(第3A圖與第3B圖)，電感82在與信號線12相同的金屬化層內可另包括額外的接地線(未顯示)。

參照第6A圖與第6B圖(在此，相似的參考編號係代表在第1A圖與第1B圖中相似的零件)並根據本發明之一替

代實施例，亦類似於電感 10(第 1A 圖與第 1B 圖)的一晶片整合可變電感 104 係納入一電容屏 106。電容屏 106 係放置在介於信號線 12 與接地線 26 之間的絕緣層 83 內，因此處在介於該等含有信號線 12 與接地線 26 之金屬化層間的一金屬化層。舉例來說，信號線 12 可為置於 M6 層之一金屬線，電容屏 106 可為置於 M3 層之一金屬線，而接地線 26 可為置於 M2 層之一金屬線。藉由三少絕緣層 14、25、83 之該等部分，信號線 12、接地線 26、電容屏 106 係與彼此電氣絕緣。電容屏 106 亦由與形成信號線 12 與接地線 26 之相同 BEOL 製程技術所形成，並來自相同或類似的 BEOL 冶金術。為簡潔說明起見，導電路徑 21、23、31、33 係省略於第 6B 圖。

電容屏 106 包括複數個實質相同的片段 108，該等片段 108 係以一彎曲形狀來電子鏈結在一起。該等片段 108 係被建構與擺放以定義該等間隙，用以讓電容屏 106 不像一連續的接地平面或接地板，好讓接地線 26 之切換在電容屏 106 的存在下可影響信號線 12 之電感值。電容屏 106 係被一直綁在接地端，因此不是被選擇性地切換。

電容屏 106 係降低介於信號線 12 與基底 16 之間的電容性耦合，其賦予電感 104 對於接地線 26 之兩不同狀態有一相似的 Q 因子。此外，電容屏 106 幫助提供將電感 104 之信號線 12 隔離於基底 16 上之積體電路內的剩餘電路。在一替代實施例中，電容屏 106 可具有一梳子形狀。

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參照第 7A 圖與第 7B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 118 包括一螺旋形狀之信號線 120 以及一螺旋形狀之接地線 126，接地線 126 係置於信號線 120 與基底 16 之間。類似於信號線 12 與接地線 26(第 1A 圖與第 1B 圖)，信號線 120 以及接地線 126 每一者係形成於一平面條狀之導電材料。信號線 120 係被埋入絕緣層 14 並被絕緣層 14 所圍繞；類似地，接地線 126 係被埋入絕緣層 25 並被絕緣層 25 所圍繞。信號線 120 與接地線 126 之螺旋形狀係實質相同。埠或端點 123、124(位於信號線 120 之相反兩端)係藉由導電路徑 21、23 電氣耦接於基底 16 上之積體電路的零件 18、20。

藉由用以提供呈電氣絕緣之該等絕緣層 14、25 之部份，接地線 126(通常位於信號線 120 下方)係與信號線 120 隔開。如同在此對於信號線 12 與接地線 26 之描述(第 1A 圖與第 1B 圖)，信號線 120 與接地線 126 係藉由傳統的 BEOL 製程技術並自用於此等製程技術之傳統 BEOL 冶金術來形成於不同的金屬化層中。舉例來說，信號線 120 可置於 M5 層或 M6 層，而接地線 126 可置於靠近基底 16 之 M2 層。如同可被熟知技藝人士所了解，信號線 120 與接地線 126 可包括額外的共同中心排列之平面螺旋線(未顯示)與下拉貫孔及地下通道。信號線 120 與接地線 126 係以具有多邊形之方式描述於第 7A 圖，在代表

性實施例中則為一八邊形。然而，信號線 120 與接地線 126 可被替代地纏繞為一具有長方形、圓形、或橢圓形之螺旋形，或是一具有不同個數之邊的多邊形。

接地線 126 的相反兩端係構成接點 128 與 130，接點 128 與 130 係以一種可選擇的方式分別藉由控制單元 32 與 34 依一電流路徑來與接地端電氣耦合。接點 128 與 130 係藉由導電路徑 31 與 33 實質耦接於控制單元 32 與 34。當控制單元 32 與 34 兩者由適當的電壓控制信號切換至斷接時，接地線 126 係為一開路並為電子浮接。當控制單元 32 與 34 處於斷接狀態時，浮接的接地線 126 並不會顯著影響信號線 120 的電感性。當控制單元 32 與 34 兩者由適當的電壓控制信號接通時，接地線 126 係處於一閉迴路電流路徑，其由一短路電路耦接至一接地電位。在一替代實施例中，接地線 126 之接點 128、130 之一者可被持續綁在接地端，只有接地線 126 之接點 128、130 的另一者切換時完成至接地電位之此閉迴路電路。

藉由將接地線 126 選擇性耦接於接地電位，控制單元 32 與 34 的操作可有效改變電感 118 的電感值。當控制單元 32 與 34 被導通以及接地線 126 在電流路徑被電氣耦接於接地端時，接地線 126 對於信號線 120 的靠近會降低電感 118 的電感值。此降低係為二元的，因為：當控制單元 32 與 34 被切換至斷接時，電感 118 具有一第一電感值；當控制單元 32 與 34 被切換至接通時，電感 118 具有一小於第一電感值之第二電感值。當控制單元

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32 與 34 被接通時，接地線 126 不是在電感 118 之信號路徑上。電感 118 係為電子可調的，因為：在基底 16 上之積體電路的操作期間，控制單元 32 與 34 可被斷接與接通。

參照第 8A 圖與第 8B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，亦類似於電感 118(第 7A 圖與第 7B 圖)之一晶片整合可變電感 140 係納入一電容屏 142。電容屏 142 被放置在介於信號線 120 與接地線 126 間之一金屬化層內。電容屏 142 係被放置在介於信號線 120 與接地線 126 間之絕緣層 83 內，因此處在含有信號線 120 與接地線 126 之該等金屬化層之間的一金屬化層。舉例來說，信號線 120 可為置於 M6 層之一金屬線，電容屏 142 可為置於 M3 層之一金屬線，而接地線 126 可為置於 M2 層之一金屬線。藉由絕緣層 14、83、25 之部份，信號線 120、接地線 126、與電容屏 142 係與彼此電氣絕緣。電容屏 142 亦被形成信號線 120 與接地線 126 的相同 BEOL 製程技術所形成，並來自相同或相似的 BEOL 冶金術。為簡潔說明起見，導電路徑 21、23、31、33 係省略於第 8B 圖。

電容屏 142 包括以屏線 144、146 形式存在之複數個實質相同的平行線片段或條(其延伸自一中央橋 148 的相反兩邊緣)。每一鄰接對之屏線 144、146 係被一間隔隔開，用以讓電容屏 142 不會定義一連續接地平面或板，以及

用以讓接地線 126 之切換在電容屏 142 的存在下可影響信號線 120 的電感值。電容屏 142 係被持續綁在接地端。

電容屏 142 係降低介於信號線 120 與基底 16 之電容性耦合，以賦予電感 140 一最佳化的 Q 值。此外，電容屏 142 係主動提供將電感 140 之信號線 120 隔離於基底 16 上之積體電路內的剩餘電路。或者是，電容屏 142 可具有一不同樣式之導電零件，例如像是發現在一放射狀類型之屏蔽，其中是該等屏線被引導至垂直於信號線 120。

第 9 圖為一用以製造一積體電路之示範性設計流程 160 的方塊圖。設計流程 160 可依據被設計之積體電路的種類來改變。舉例來說，一用以建構一特定應用積體電路(ASIC)之設計流程 160 將不同於一用以建構一標準元件之設計流程 160。設計結構 164 係為設計流程 162 的一輸入，並可來自一智財(IP)供應商、一核心發展商、或其他設計公司。設計結構 164 包含以電路圖與佈局圖或硬體描述語言(HDL)(例如像是 VHDL 或是 Verilog)形式存在之一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140。由於 HDL 表示方式一般係定義要被一電路設計所執行之邏輯或功能，一積體電路之 HDL 表示方式在許多方面係類似於一軟體程式。如同在以下之第 10 圖內容中所描述，設計結構 164 可以位於一或多機器可讀媒體上。舉例來說，設計結構 164 可以是一積體電路(包括一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140)之一文字檔或一圖形表示方式。設計流程

162 將積體電路(包括一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140)合成(或轉換)為一網路連線表(netlist)176。舉例來說，網路連線表 176 係為粗線、電晶體、邏輯閘、控制電路、I/O、模型等等之一列表，並描述在一積體電路設計內與其他元件及電路的連接關係並被記錄在至少一機器可讀媒體上。

設計流程 162 包括各種製程之使用；舉例來說，來自函式庫元件 166(其可針對一特定製造技術(例如，不同技術節點、32nm、45 nm、90nm 等等)設置一組常用的元件、電路、以及裝置，包括模型、佈局、以及符號表示方式)之輸入、製造規格 168 之輸入、描述資料 170 之輸入、驗證資料 172 之輸入、設計規則 174 之輸入、以及測試資料檔案 178 之輸入(其可包括測試樣式與其他測試資訊)。舉例來說，設計流程 162 包括標準電路設計流程，例如像是時序分析、驗證工具、設計規則檢查器、配置與繞線工具等等。一熟知積體電路設計之技藝人士可明瞭可能的電子設計自動化工具與應用(可被用於設計流程 162 之替代實施例中)之範圍。

設計流程 162 最終將包括一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140 之電路與剩餘的積體電路設計(如果適用的話)轉換成一最後設計結構 180(例如儲存在一 GDS 儲存媒體內之資訊)。最後設計結構 180 可包括資訊，像是測試資料檔案、設計內容檔案、製造資料、佈局參數、線、金屬之層、貫孔、形狀、測

試資料、透過製造線之繞線資料、以及半導體製造器所需以製造一電路(含有一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140)的任何其他資料。最後設計結構 180 可接著進行到設計流 160 之階段 182；舉例來說，階段 182 是最後設計結構 180 進行到下線(tape-out)之處，階段 182 在此係被送去製造、被送到另一設計公司、或回到客戶手上。

第 10 圖接著說明一裝置 190，設計流程 160 之各種步驟可在裝置 190 內執行。在所述實施例中，裝置 190 係被實作為一伺服器或多使用者之電腦(其會透過網路 192 耦接於一或多客戶電腦 194)。為了本發明的目的，每一電腦 190、194 實際上可代表任何種類的電腦、電腦系統、或其他可編程電子裝置。此外，每一電腦 190、194 可利用一或多連成網路的電腦來實作，例如在一叢集或其他分散式電腦系統中。在替代方案中，電腦 190 可被實作在單一電腦中或其他可編程電子裝置(例如一桌上型電腦、一膝上型電腦、一手持電腦、一手機、一機上盒等等)中。

電腦 190 通常包括一中央處理單元(CPU)196；CPU 196 包括耦接於記憶體 198 之至少一微處理器；記憶體 198 可代表該等隨機存取記憶體(RAM)裝置，包含電腦 190 之主要儲存以及任何補充層級之記憶體(例如快取記憶體、非揮發或備份記憶體(例如可編程或快閃記憶體)、唯讀記憶體等等)。此外，記憶體 198 可被認為包括實際

上位於電腦 190 別處之記憶體儲存(例如在 CPU 196 之一處理器內的任何快取記憶體)以及被用來作為一虛擬記憶體之任何儲存容量(例如像是儲存在一大容量裝置 200 上，或是在耦接於電腦 190 之其他電腦上)。通常電腦 190 亦接收一些輸入與輸出，用以在外部對資訊進行通訊。為提供介面給使用者或操作者，電腦 190 通常包括一使用者介面 202，其納入一或多使用者輸入裝置(例如，一鍵盤、一滑鼠、一軌跡球、一搖桿、一觸控板、及(或)一麥克風、其他者)以及一顯示(例如，一 CRT 螢幕、一 LCD 顯示板、及(或)一喇叭、其他者)。除此之外，使用者之輸入可透過其他的電腦或終端來接收。

對於額外的儲存，電腦 190 亦可包括一或多大容量儲存裝置 200，例如一軟碟或其他可移除式碟機、一硬碟機、一直接存取儲存裝置(DASD)、一光碟機(例如，一 CD 碟機、一 DVD 碟機等等)、及(或)一磁帶機、其他者。此外，電腦 190 可包括與一或多網路 192(例如，一 LAN、一 WAN、一無線網路、及(或)網際網路、其他者)連接之一介面 204，以允許與其他電腦及電子裝置之資訊通訊。應理解到，如同在技藝中所知，在 CPU 196 與元件 198、200、202、204 每一者之間，電腦 190 通常包括合適的類比及(或)數位介面。其他的硬體環境係被考量於本發明之內容內。

如同將於其下所詳述，電腦 190 係運作在一作業系統 206 的控制之下並加以執行，或依靠各種電腦軟體應用

程式、元件、程式、物件、模組、資料結構等等。此外，各種應用程式、元件、程式、物件、模組等等亦可執行於透過網路 192(例如，在一分散式或主從架構之計算環境中)來耦接於電腦 190 之其他電腦的一或多處理器上，藉此用以實作電腦程式之該等功能所需的處理可被分配到網路上之多個電腦。

一般來說，不論是否被實作為一部份的作業系統或特定應用程式、元件、程式、物件、模組或一串指令、或甚至是在此之一子集合，經執行以實作本發明該等實施例之常式在此將代表「電腦程式碼」或僅為「程式碼」。程式碼通常包含一或多指令，該等指令有時常駐在一電腦內之各種記憶體與儲存裝置，當該等指令被電腦內之一或多處理器讀取或執行時，會造成此電腦執行該等必要的步驟來執行用以實施本發明各式態樣的步驟與元件。此外，儘管本發明具有並將於其後描述為全功能電腦與電腦系統之情境內，熟知技藝人士將理解到本發明之各式實施例能夠被分配為各種形式之一程式產品，並理解到不論被用來實際實作此分配之機器可讀媒體的特殊種類為何，本發明係平等地使用。機器可讀媒體的範例包括但不限於可觸碰、可記錄種類的媒體，例如像是揮發與非揮發記憶體裝置、軟碟與其他可移除碟、硬碟機、磁帶、光碟(例如 CD-ROM、DVD 等等)、其他者、以及傳送種類媒體(例如像是數位與類比通訊鏈結)。

此外，此後所述之各種程式碼可根據應用加以辨識(在

此應用內，程式碼係被實作在本發明之一特定實施例)。然而，應理解到，所採用之任何特定程式命名僅為方便之用，因此本發明不應被限制於僅在由此命名所辨識及(或)意味之任何特定應用。再者，給定通常不限個數的方法(在此，電腦程式可被組織為常式、程序、方法、模組、物件、及其相似者)以及各式方法(在此，程式功能可位在常駐於一典型電腦之各種軟體層(例如，作業系統、函式庫、API、應用、小程式等等)間)，應理解到本發明未被限制於在此所述之程式功能的特定組織與配置。

為了實作在第 9 圖之設計流程 162 內的各種活動，電腦 190 包括一些軟體工具，舉例來說，軟體工具包括一設計流程工具 208。與積體電路設計、驗證、及(或)測試所結合使用之其他工具亦可被用在電腦 190 內。此外，儘管設計流程工具 208 被顯示在單一電腦 190 中，具有快速揭露優勢之熟知技藝人士將理解到通常此等工具會被擺放在分離的電腦，特別是當多個個體參與一積體電路設計之邏輯設計、整合、與驗證時。因此，本發明之該等實施例並未被限於第 10 圖所描繪之單一電腦實作。

熟知技藝人士將理解到第 9 圖與第 10 圖所描繪之示範性環境並非意圖限制本發明之實施例。實際上，熟知技藝人士將理解到其他替代的硬體及(或)軟體環境係可被使用。

在此對於詞彙的參照(例如像是「垂直」、「水平」等等)

係作為範例而非限制之用，以建立參考之框架。此處所使用之詞彙「水平」係被定義為平行於一半導體基底之傳統平面的平面，而不論它實際的三維空間方向為何。如同所定義的，詞彙「垂直」係代表垂直於水平之一方向。該等詞彙(例如像是「上」、「以上」、「以下」、「邊」(像是在「側邊」中)、「上面」、「下面」、「上方」、「下方」、「下」係被定義為關於水平平面。可了解到，各種其他相對的參照可被用來描述本發明而不脫離本發明之精神與範疇。亦了解到，本發明之該等框架沒有必要在圖中被特別顯示。此外，對於用在詳細描述或是申請專利範圍中之詞彙「包括」、「具有」、「具」、「有」、或在此之變形的範圍，此等詞彙係意欲被含括在類似於詞彙「包含」之方式中。

雖然本發明已以各種實施例的描述所述並且該等實施例被相當詳細地描述，然申請者並非意圖將所附申請專利範圍限定或以任何方式限制在此等細節中。對於熟習技藝人士來說，將可輕易明白另外的優點與修正形式。因此在較廣態樣中之本發明並未被限制在被顯示與被描述之特定細節、代表裝置與方法、以及所述範例中。因此可分離於此等細節而不脫離申請者一般發明概念之精神和範圍。

【圖式簡單說明】

第 1A 圖係根據本發明一實施例由一信號線與一經切換接地線所組成之一晶片整合可變電感之透視圖，在此所包圍的介電材料為簡潔起見係省略。

第 1B 圖係第 1A 圖電感之一剖面圖。

第 2A 圖與第 2B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由一信號線與多經切換接地線所組成。

第 3A 圖與第 3B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由實質被放置在單一金屬化層之一信號線與多經切換接地線所組成。

第 4A 圖與第 4B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由實質被放置在不同金屬化層之一信號線與多經切換接地線所組成。

第 5A 圖與第 5B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由實質被放置在單一金屬化層之一信號線與該等經切換接地線之堆疊所組成。

第 6A 圖與第 6B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，在此一電容器係置於信號線與接地線之間。

第 7A 圖係根據本發明一實施例由一螺旋形信號線與一經切換螺旋形接地線所組成之一晶片整合可變電感之

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透視圖，在此所包圍的介電材料為簡潔起見係省略。

第 7B 圖係第 7A 圖電感之一剖面圖。

第 8A 圖與第 8B 圖係根據本發明一替代實施例之類似於第 7A 圖與第 7B 圖之晶片整合可變電感的透視圖與剖面圖，在此一電容屏係置於信號線與接地線之間。

第 9 圖係一示範性設計流的方塊圖。

第 10 圖係適於實作第 9 圖流程之一電腦系統內之該等主要硬體元件的一方塊圖。

【主要元件符號說明】

10、38、60、81、82、104、[illegible] 晶片整合可變電感

12、120	信號線
14、25、27、83、85、122	絕緣層
16	基底
18、20	零件
21、23、31、33	導電路徑
22、24、123、124	端點
26、40、42、62、64、84、86、126	接地線
28、30、44、46、52、54、66、68、74、76、88、90、96、98、128、130	接點
32、34、48、50、56、58、70、72、78、80、92、94、100、102	控制單元

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106、142	電容屏
108	片段
144、146	屏線
148	中央橋
160	設計流
162	設計流程
164	設計工具
166	函式庫元件
168	製造廠格
170	描述語言
172	驗證語言
174	設計檔案
176	網路連線表
178	測試語言檔案
180	最後設計結構
182	階段
190	裝置
192	網路
194	客戶電腦
196	中央處理單元
198	記憶體

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200	大容量裝置
202	使用者介面
204	網路介面
206	作業系統
208	設計流程工具

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201003883

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分電勿填寫；惟已有申請案號者請填寫）

※ 申請案號：98101836

※ 申請日期：2009 年 1 月 17 日　　※IPC 分類：H01L23/58(2006.01)

一、發明名稱：（中文/英文）

晶片整合之壓控可變電感，製造並調整此可變電感之方法，以及整合此可變電感之設計結構

ON-CHIP INTEGRATED VOLTAGE-CONTROLLED VARIABLE INDUCTOR, METHODS OF MAKING AND TUNING SUCH VARIABLE INDUCTORS, AND DESIGN STRUCTURES INTEGRATING SUCH VARIABLE INDUCTORS

二、中文發明摘要：

揭露關於晶片整合可變電感、製造與調整晶片整合可變電感之方法、以及實施一包含晶片整合可變電感之電路的設計結構。電感通常包括一經組態以接收一電子信號之信號線、一位於靠近信號線處之接地線、以及經電氣耦接於接地線之至少一控制單元。至少一控制單元係經組態以斷接與接通將接地線連接於接地電位之電流路徑，以致於改變信號線之電感性。

三、英文發明摘要：

On-chip integrated variable inductors, methods of making and tuning an on-chip integrated variable inductor, and design structures embodying a circuit containing the on-chip integrated variable inductor. The inductor generally

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includes a signal line configured to carry an electrical signal, a ground line positioned in proximity to the signal line, and at least one control unit electrically coupled with the ground line. The at least one control unit is configured to open and close a current path connecting the ground line with a ground potential so as to change an inductance of the signal line.

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七、申請專利範圍：

1. 一種晶片整合可變電感，至少包含：

一信號線，經組態以導通一電子信號；

一第一接地線，位於靠近該信號線之處；以及

至少一控制單元，放置在連接該第一接地線與一接地電位之一第一電流路徑上，該至少一控制單元係經組態以選擇性地斷接與接通該第一電流路徑，以致於當該第一電流路徑被斷接時該信號線具有一第一電感值，以及當該第一電流路徑被接通以將該第一接地線耦接於該接地電位時該信號線具有一第二電感值。

2. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一積體電路，電氣耦接於該信號線以用以與該電子信號通訊；以及

一晶片，裝載該第一接地線、該信號線、以及該積體電路，該第一接地線係位於該信號線以及該晶片之間。

3. 如申請專利範圍第 2 項所述之晶片整合可變電感，其中該至少一控制單元係製造在該晶片上。

4. 如申請專利範圍第 1 項所述之晶片整合可變電感，其中

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該信號線係一第一平面螺旋繞線，以及該第一接地線係位於該第一平面螺旋繞線下之一第二平面螺旋繞線。

5. 如申請專利範圍第 1 項所述之晶片整合可變電感，其中該信號線係一第一平面導線，以及該第一接地線係一第二平面導線，該第二平面導線係置於與該第一平面導線相關之一空間關係中。

6. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一介電材料，包圍該信號線與該第一接地線，一部份之該介電材料係置於該信號線與該第一接地線之間以避免該信號線與該第一接地線間之電子導通。

7. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一電容屏，置於該第一接地線與該信號線之間。

8. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一晶片，裝載該第一接地線與該信號線；以及

一積體電路，經裝載於該晶片上，該積體電路電氣耦接於該信號線以用以與該電子信號通訊。

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9. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一第二接地線，位於靠近該信號線之處，該第二接地線係經組態以在一第二電流路徑中選擇性地耦接於接地電位，該第二電流路徑係與該第一電流路徑電氣磁耦合，以及當該第二接地線耦接於該接地電位時該信號線具有一第三電感值。

10. 如申請專利範圍第 9 項所述之晶片整合可變電感，其中該第一接地線被含在一第一金屬化層中，該第二接地線被含在一第二金屬化層中，該信號線被含在一第三金屬化層中，以及該第一接地線、該第二接地線、以及該信號線具有一堆疊配置，在該堆疊配置中該第二金屬化層被放置在該第一金屬化層與該第三金屬化層之間。

11. 如申請專利範圍第 9 項所述之晶片整合可變電感，其中該第一接地線、該第二接地線、以及該信號線被含在一共同金屬化層，以及該信號線被放置在該第一接地線與該第二接地線之間。

12. 如申請專利範圍第 9 項所述之晶片整合可變電感，其中該第一接地線與該第二接地線被含在一第一金屬化層中，以及該信號線被含在不同於該第一金屬化層之一第二金屬化層中。

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13. 如申請專利範圍第 9 項所述之晶片整合可變電感，另包含：

一第三接地線，位在靠近該信號線之處，該第三接地線係經組態以在一第三電流路徑中選擇性地耦接於接地電位，該第三電流路徑係與該第一電流路徑與該第二電流路徑電氣無關，以及當該第三接地線耦接於該接地電位時該信號線具有一第四電感值。

14. 如申請專利範圍第 13 項所述之晶片整合可變電感，其中該第一接地線、該第二接地線、以及該信號線被含在一第一金屬化層，以及該第三接地線被放置在不同於該第一金屬化層之一第二金屬化層。

15. 一種製造一晶片整合可變電感之方法，該方法至少包含以下步驟：

在一晶片上製造一信號線，該信號線係電氣耦接於該晶片上之一積體電路；

製造一第一接地線，該第一接地線係足夠靠近該信號線，以致於當該第一接地線在一第一電流路徑中耦接於一接地電位時該信號線具有一第一電感值，以及當該第一電流路徑斷接時該信號線具有一第二電感值；以及

製造至少一控制單元，該控制單元係經組態以選

擇性地斷接或接通該第一電流路徑。

16. 如申請專利範圍第15項所述之方法，其中該第一接地線係被製造於一第一金屬化層上，以及該信號線係被製造在不同於該第一金屬化層之一第二金屬化層上。

17. 如申請專利範圍第15項所述之方法，其中該第一接地線以及該信號線係被製造在相同金屬化層上。

18. 如申請專利範圍第15項所述之方法，更包含以下步驟：

製造一第二接地線，該第二接地線係足夠靠近該信號線，以致於當該第二接地線在一第二電流路徑上耦接於該接地電位時該信號線具有一第三電感值，以及當該第二電流路徑斷接時該信號線具有一第四電感值；以及

製造至少一控制單元，該控制單元係經組態以選擇性地斷接與接通該第二電流路徑。

19. 一種於一積體電路之操作期間調整一晶片整合可變電感之方法，該積體電路係電氣耦接於該晶片整合可變電感，該方法至少包含以下步驟：

自該積體電路引導一電子信號通過該晶片整合可變電感之一信號線；以及

選擇性地將足夠靠近該信號線之至少一接地線接

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地，以改變該信號線之一電感值。

20. 如申請專利範圍第 19 項所述之方法，其中選擇性地將該至少一接地線接地之步驟另包含以下步驟：

操作至少一控制單元，以將該至少一接地線電氣耦接於一接地電位。

21. 如申請專利範圍第 20 項所述之方法，其中操作該至少一控制單元之步驟另包含以下步驟：

將一電壓信號傳送至該至少一控制單元，該至少一控制單元係有效以電氣耦接該至少一接地線至該接地電位。

22. 一種實施於一機器可讀媒體以用來設計與製造一電路之設計結構，該電路包含：

一晶片整合可變電感，該晶片整合可變電感包含一信號線以及一接地線，該信號線經組態以導通一電子信號，該接地線係位於靠近該信號線之處；以及

至少一控制單元，該至少一控制單元被放置在將該接地線連接到一接地電位之一電流路徑上，該至少一控制單元係經組態以選擇性地斷接與接通該電流路徑，以致於當該電流路徑被斷接時該信號線具有一第一電感值，以及當該電流路徑被接通以將該接地線耦接於該接地電位時該信號線具有一第二電感值。

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23. 如申請專利範圍第 22 項所述之設計結構，其中該信號線係一第一平面螺旋繞線，以及該接地線係一位於該第一平面螺旋繞線下方之一第二平面螺旋繞線。

24. 如申請專利範圍第 22 項所述之設計結構，其中該信號線係一第一平面導線，以及該接地線係一第二平面導線，該第二平面導線係置於與該第一平面導線相關之一空間關係中。

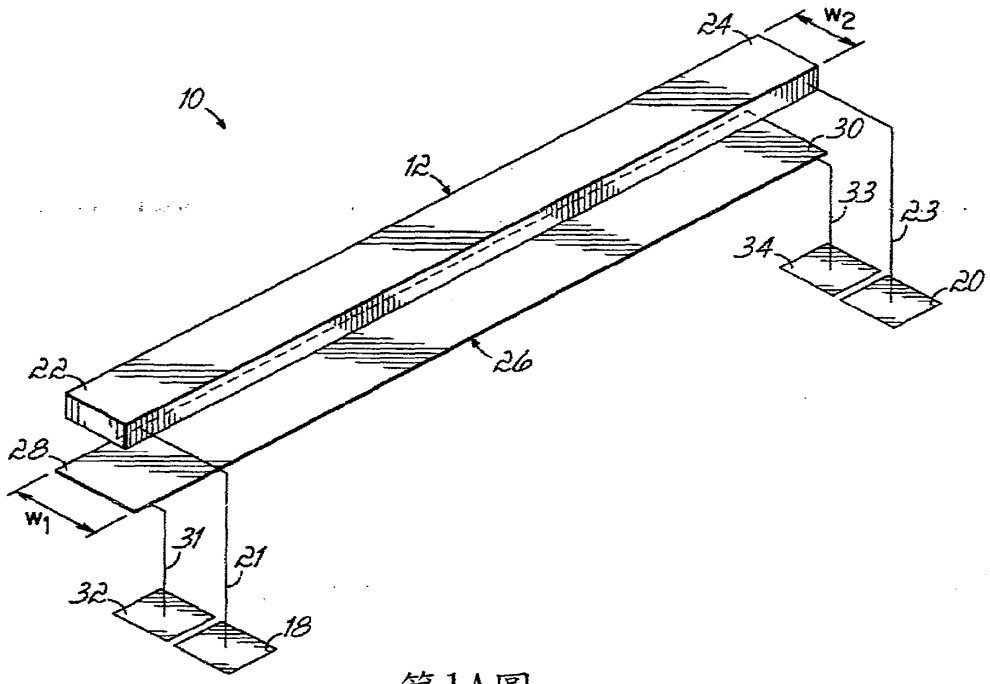
25. 如申請專利範圍第 22 項所述之設計結構，其中該電路另包含：

一電容屏，放置在該接地線與該信號線之間。

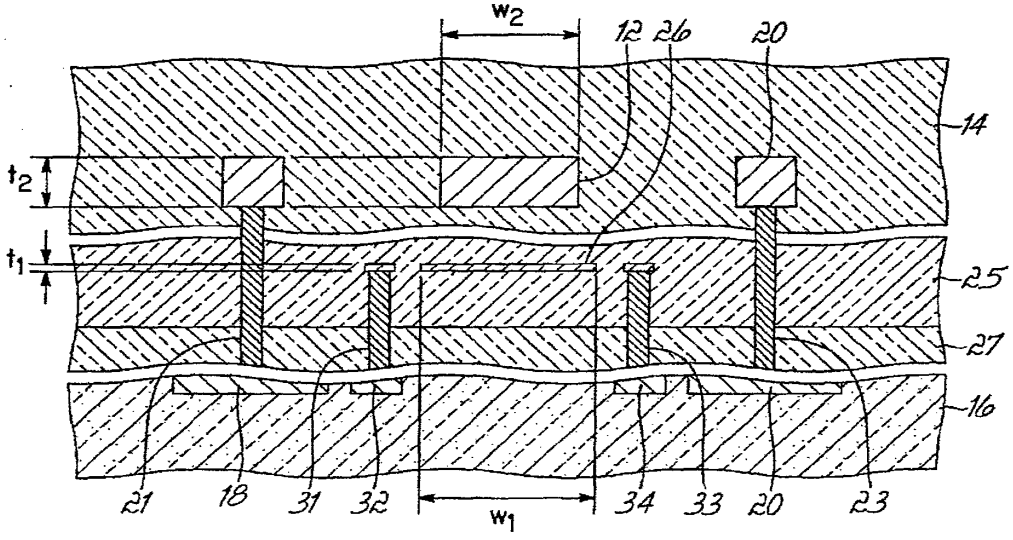
26. 如申請專利範圍第 22 項所述之設計結構，其中該至少一控制單元係經組態以運作在一控制電壓信號之接收，以選擇性地斷接與接通該電流路徑。

27. 如申請專利範圍第 22 項所述之設計結構，其中該至少一控制單元係選擇自場效電晶體、正－本－負二極體、以及在此之組合所組成之群組。

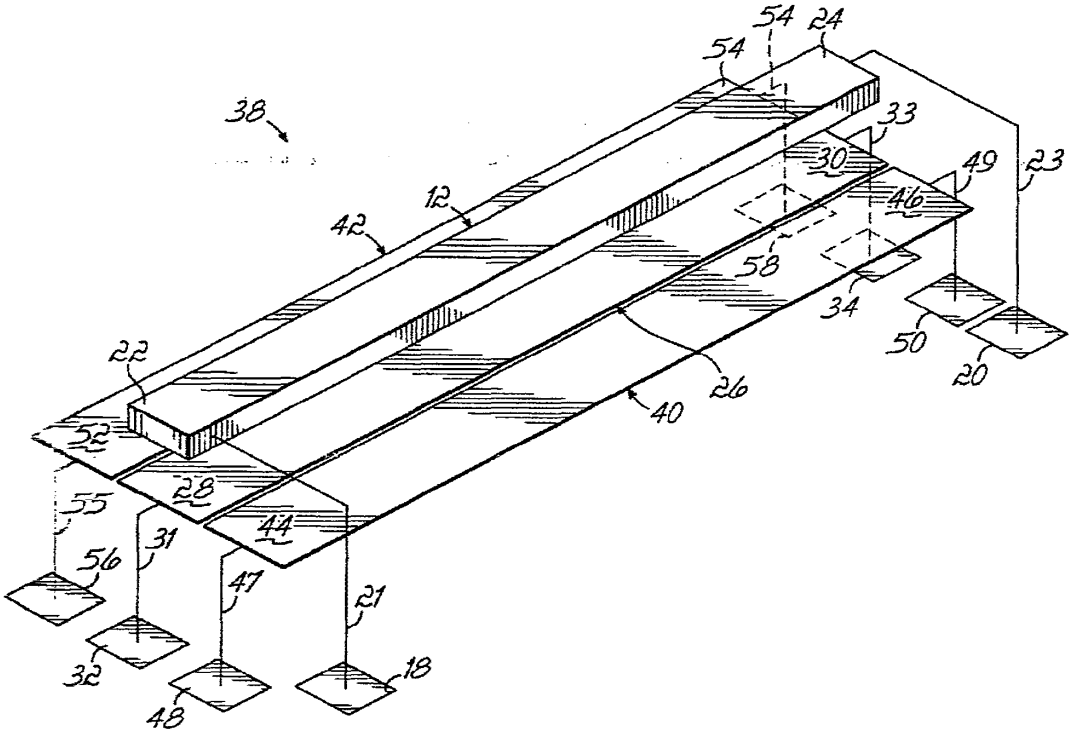
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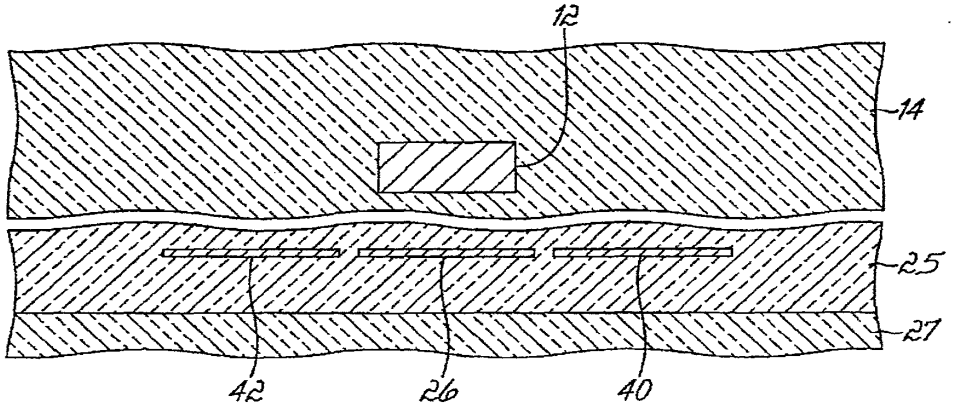
第1A圖


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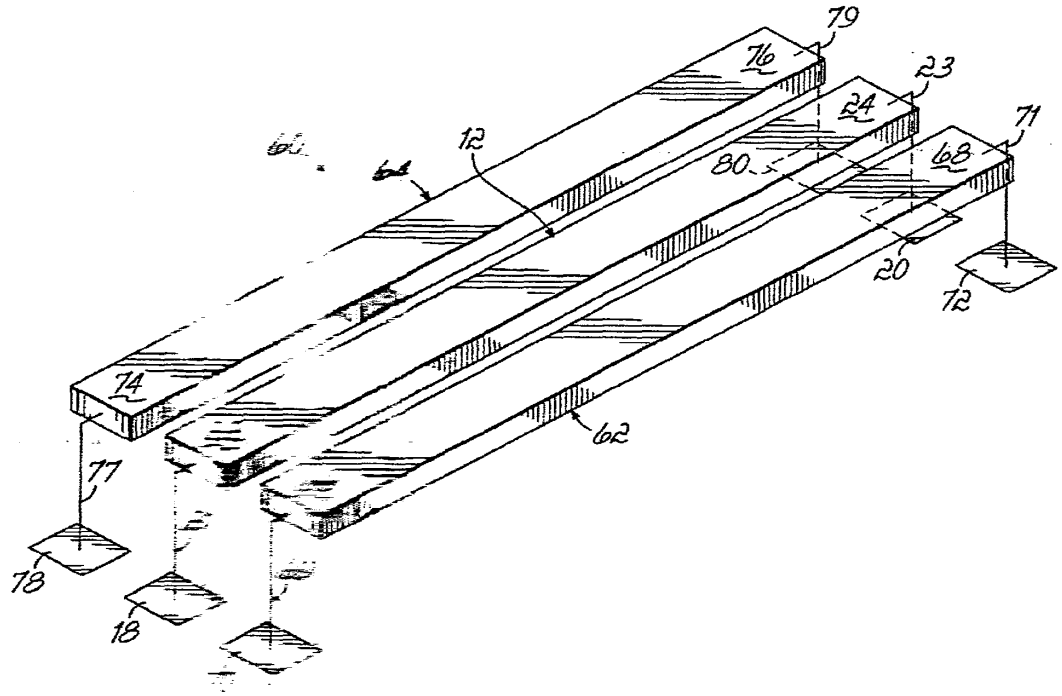
第1B圖


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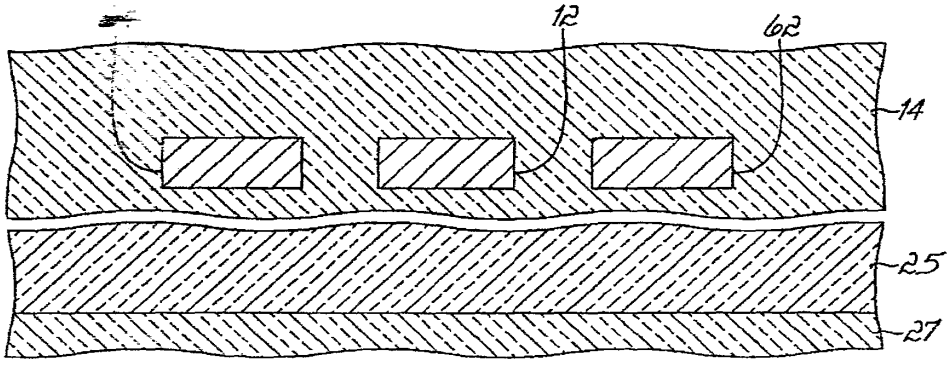
第2A圖


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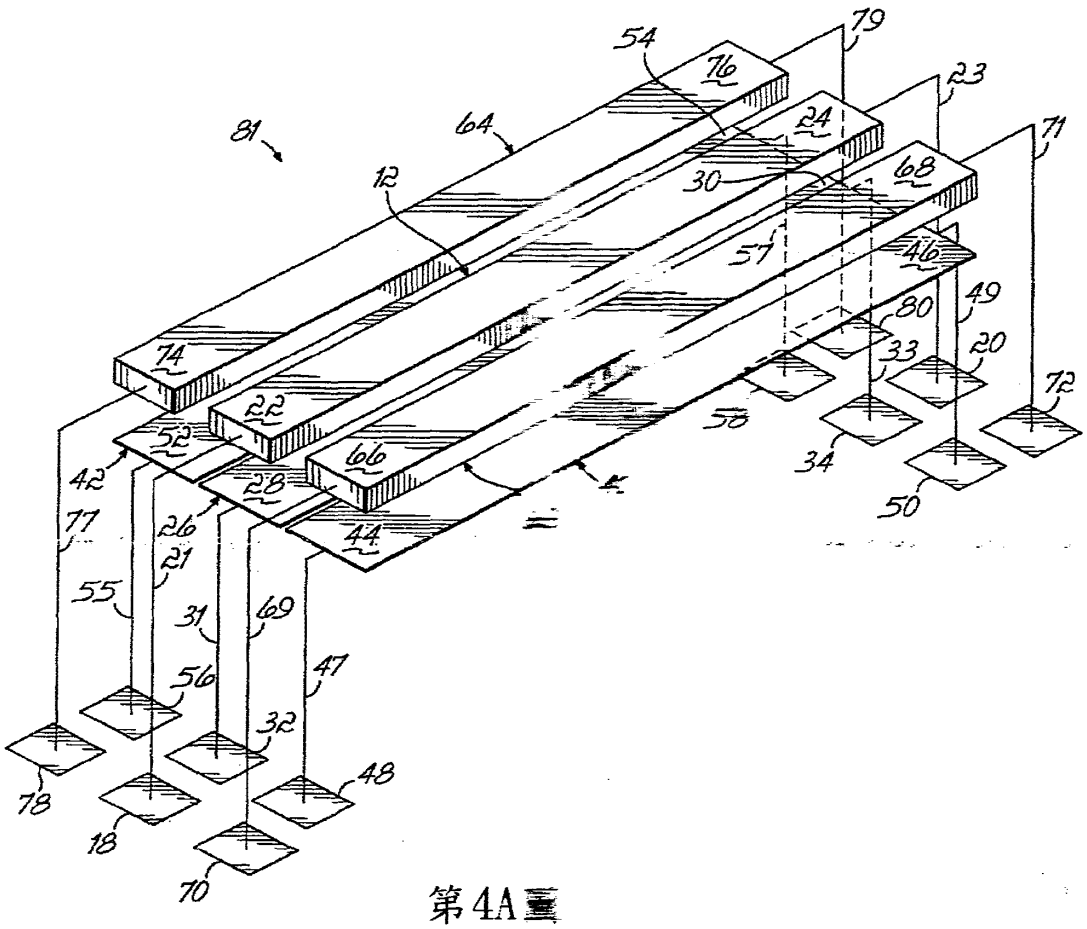
第2B圖



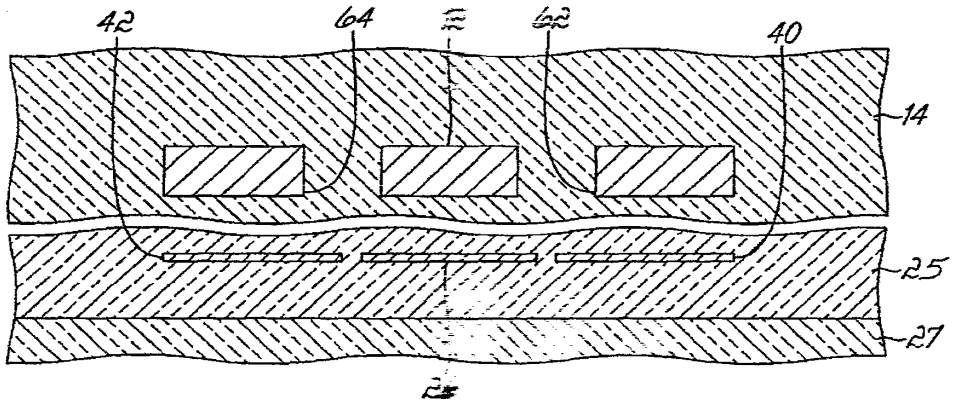
第3A圖



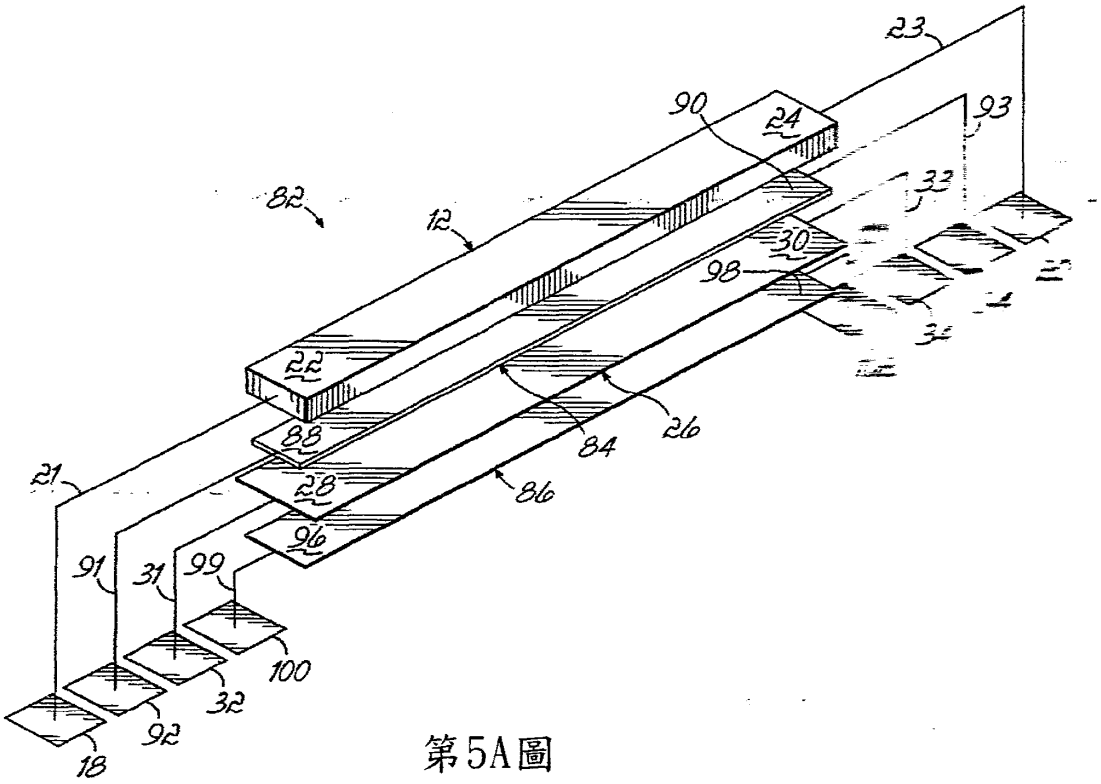
第3B圖


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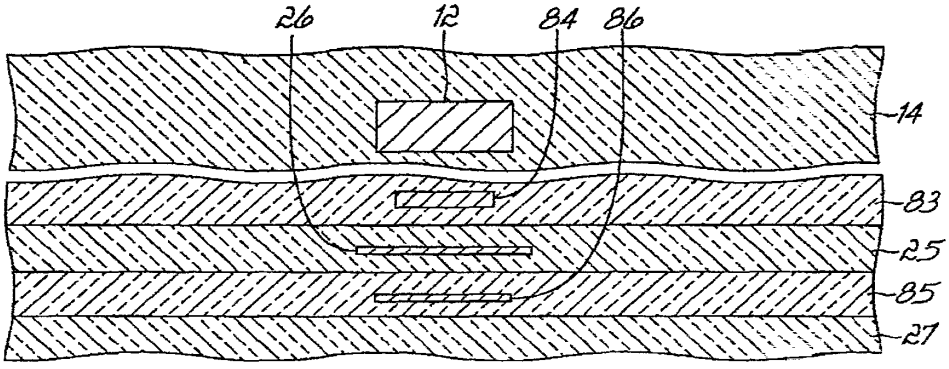
第4A圖


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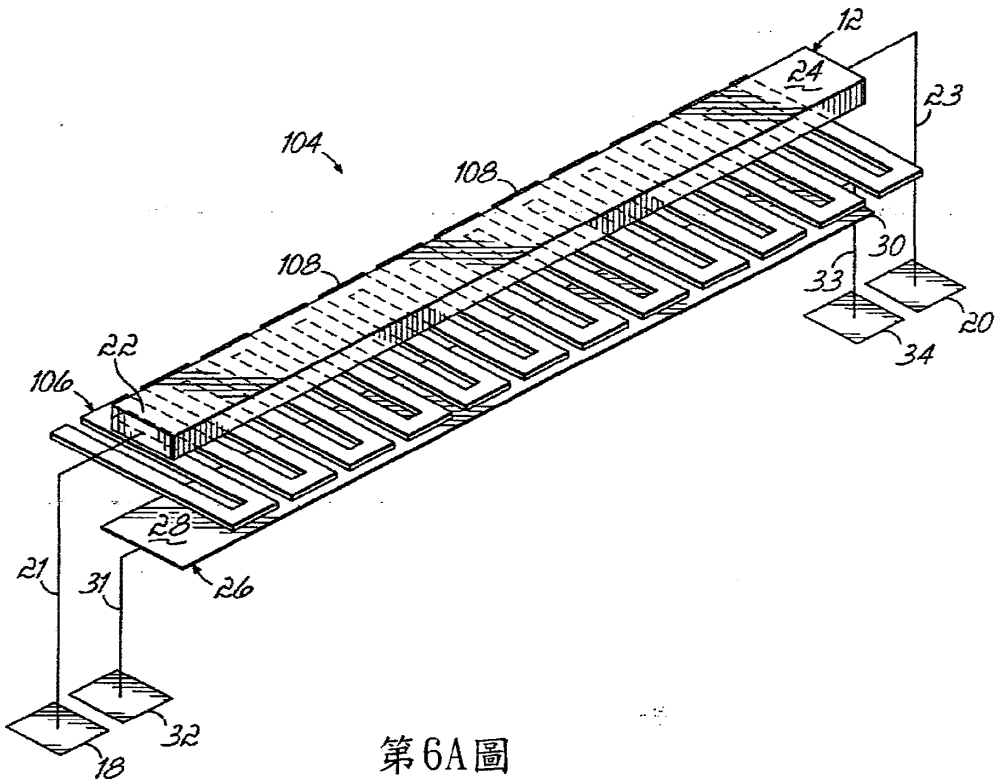
第4B圖


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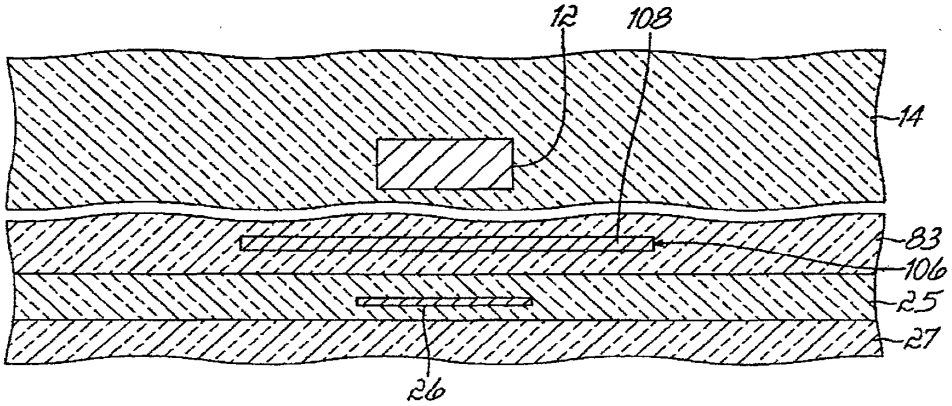
第5A圖


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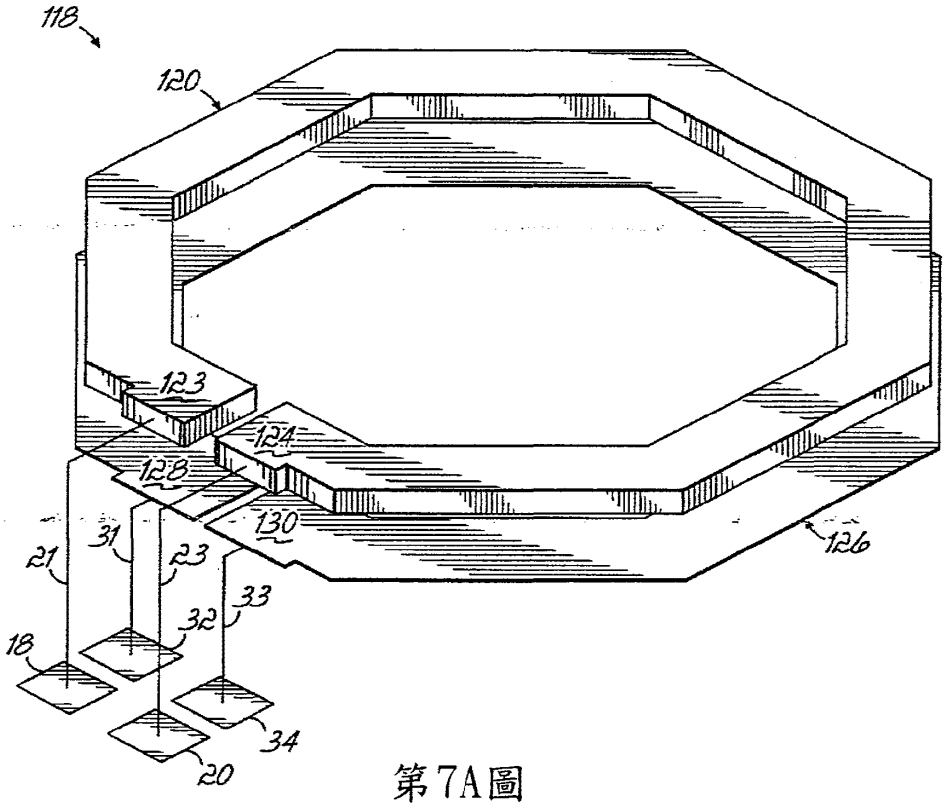
第5B圖


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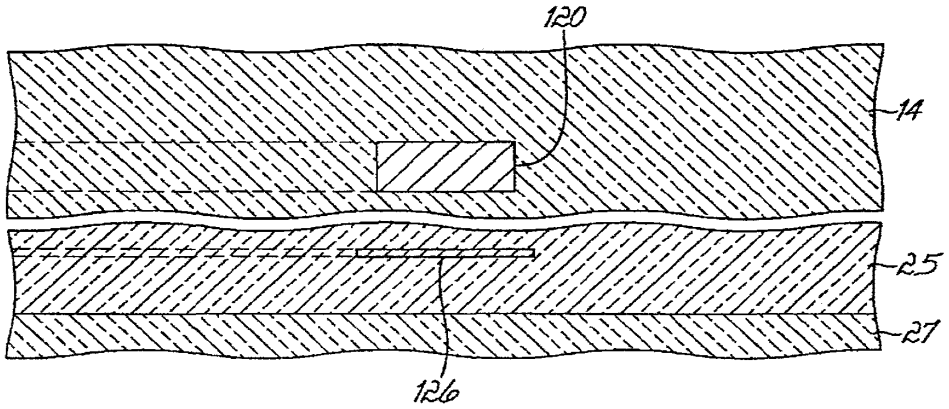
第6A圖


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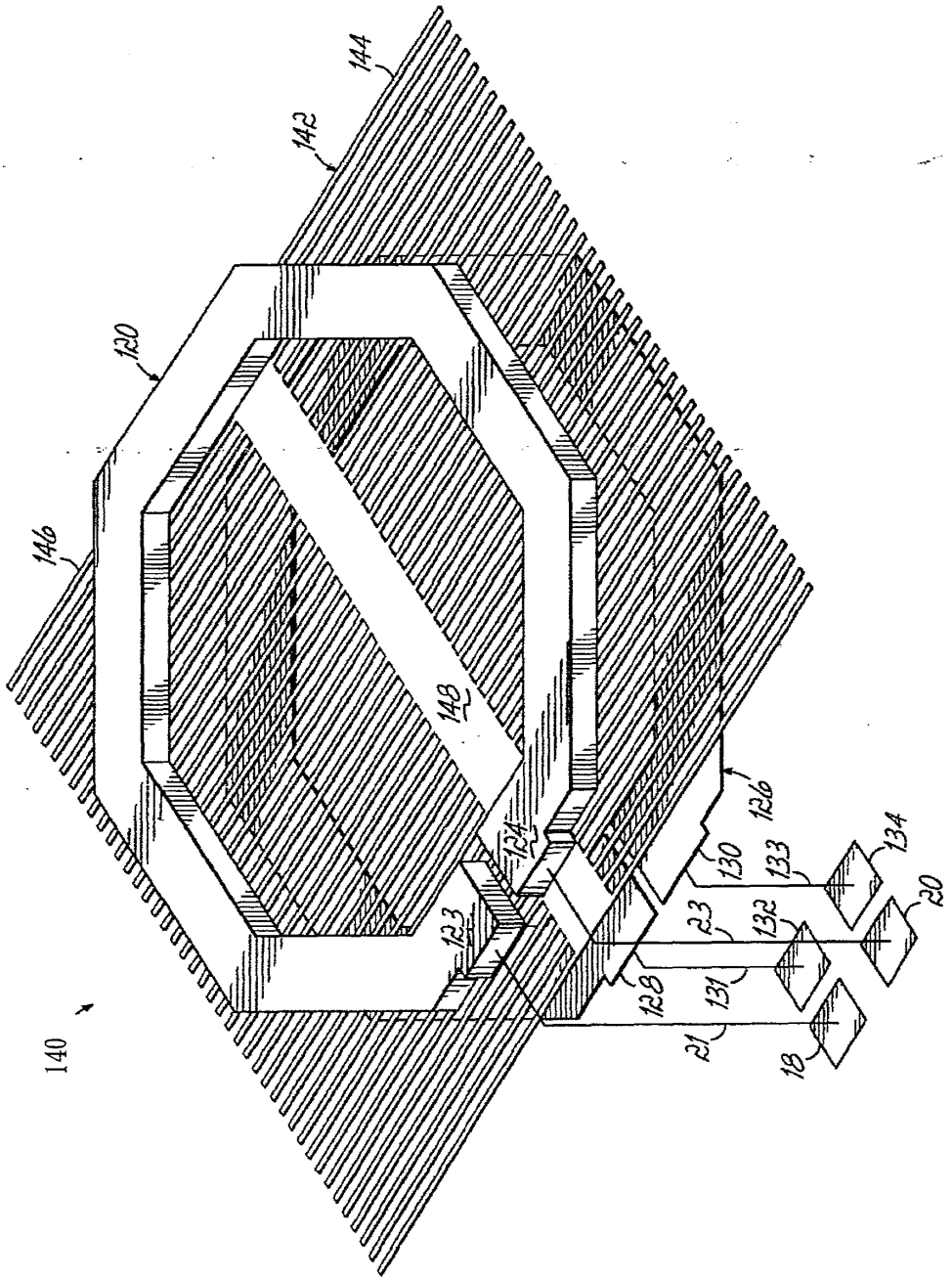
第6B圖



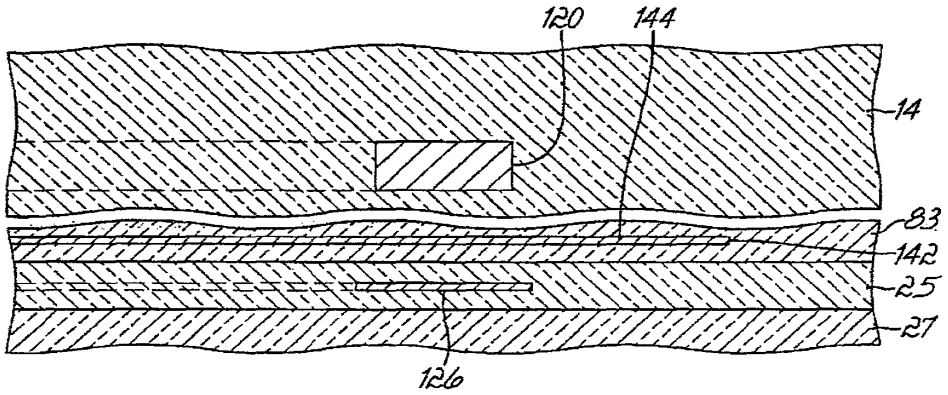
第7A圖



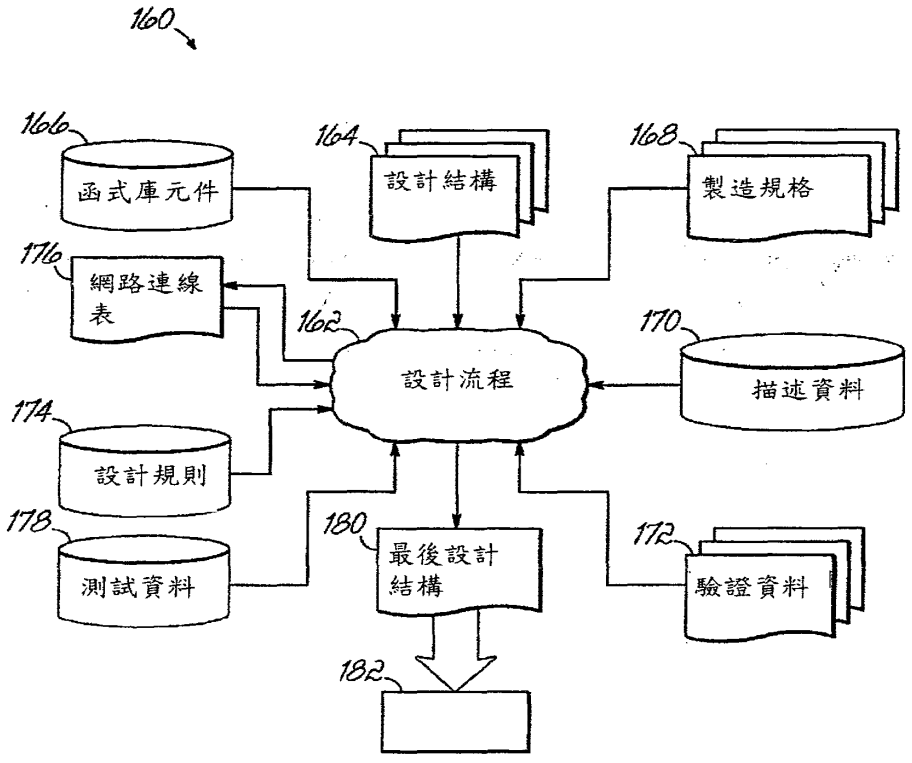
第7B圖


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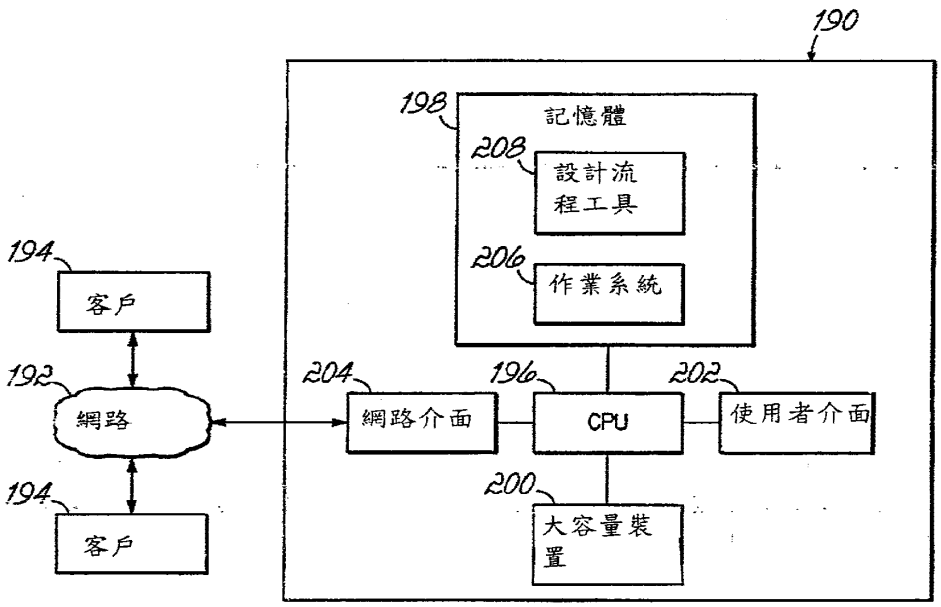
第8A圖


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第8B圖


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設計結構
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設計流程
170
描述資料
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設計規則
178
測試資料
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最後設計結構
172
驗證資料
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第9圖


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作業系統
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192
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網路介面
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客戶
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大容量裝置

第10圖

四、指定代表圖：

(一)本案指定代表圖為：第（ 9 ）圖。

(二)本代表圖之元件符號簡單說明:

160	設計流
162	設計流程
164	設計結構
166	函式庫元件
168	製造規格
170	描述資料
172	驗證資料
174	設計規則
176	網路連線表
178	測試資料檔案
180	最後設計結構
182	階段

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

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104.4.M 修正 補充

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫；惟已有申請案號者請填寫）

※ 申請案號：98101836

※ 申請日期：2009 年 1 月 17 日　　※IPC 分類：H01L23/58(2006.01)

一、發明名稱：（中文/英文）

晶片整合之壓控可變電感，製造與調整此可變電感之方法，以及整合此可變電感之設計結構

ON-CHIP INTEGRATED VOLTAGE-CONTROLLED VARIABLE INDUCTOR, METHODS OF MAKING AND TURNING SUCH VARIABLE INDUCTORS, AND DESIGN STRUCTURES INTEGRATING SUCH VARIABLE INDUCTORS

二、中文發明摘要：

揭露關於晶片整合可變電感、製造與調整晶片整合可變電感之方法、以及實施一包含晶片整合可變電感之電路的設計結構。電感通常包括一經組態以裝載一電子信號之信號線、一位於靠近信號線處之接地線、以及經電氣耦接於接地線之至少一控制單元。至少一控制單元係經組態以斷接與接通將接地線連接於接地電位之電流路徑，以致於改變信號線之電感性。

三、英文發明摘要：

On-chip integrated variable inductors, methods of making and tuning an on-chip integrated variable inductor, and design structures embodying a circuit containing the on-chip integrated variable inductor. The inductor generally

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六、發明說明：

【發明所屬之技術領域】

本發明是有關於積體電路，更特定來說，是有關於積體電路之晶片整合可變電感，實施此晶片整合可變電感之設計結構，製造此晶片整合可變電感之方法，以及在電路運作期間調整晶片整合可變電感之方法。

【先前技術】

電感是見於許多積體電路之一被動電子裝置，積體電路包括射頻積體電路(RFIC)、多頻帶被動匹配網路、多頻帶壓控振盪器(VCO)儲槽電路、以及相位延遲單元。電感可被單獨用在積體電路中或是以成對方式配置為積體電路內之差動電感或變壓器。一般來說，電感是一反應性元件，其可儲存其磁場中的能量並傾向抵抗流經其之電流流動量的改變。電感的效能會顯著影響相關積體電路之整體效能，電感甚至可能成為一效能限制元件。晶片電感或是單片電感通常會在相同的基底(substrate)上製造以作為相關積體電路的其餘部份。電感可以一傳統的金屬氧化半導體(MOS)製程或是先進矽鍺(SiGe)製程來加以製造。

晶片電感的重要參數包括電感值、Q(品質因子)、共振頻率(電感與電容值)、以及晶片面積，在積體電路中所有的這些參數都需要被最佳化。品質因子Q是關於積體

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電路內之電感效能的一通常被接受之指標，並且代表了在電感內能量損失與能量儲存間之關係的量測。高數值的Q係反應出一低的基底損失與一低的串聯電阻值。

晶片電感可為一平面形式(包括直線種類與平面螺旋種類)或一螺旋形式，並具有固定或可變的電感值。混合信號與射頻應用通常會需要可變的反應性元件(例如電感或電容)來完成調整、頻帶切換、鎖相迴路功能等等。此等反應性元件通常被用在某些種類的電路內，在此電路內反應性元件係與其他的反應性元件共振。所欲之結果為一具有如下反應之共振電路：可動態地從一頻率調整到另一頻率。一達成之方法係在電路設計中建立將一額外長度之導體切換至晶片可變電感之信號線的能力。導體的額外長度可被串聯或並聯於導體的原本長度。電感信號線之加長會改變其電感值。然而，傳統的配置方式係需要可變電感之信號線內的某些切換，對於許多混合信號與射頻應用來說，會使得Q值惡化到一無法接受的低數值。

因此，晶片可變電感的改良結構被需要以克服而不具有傳統可變電感的此等缺點或其他缺點。

【發明內容】

在一實施例中，一晶片整合可變電感包含一經組態以裝載一電子信號之信號線、一位於靠近信號線處之接地

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線、以及被放置在一電流路徑上之至少一控制單元，該電流路徑係將接地線連接於接地電位。該至少一控制單元係經組態以選擇性地斷接與接通該電流路徑，以致於當該電流路徑被斷接時該信號線具有一第一電感值，以及當該電流路徑被接通以將該接地線耦接於該接地電位時該信號線具有一第二電感值。

該晶片整合可變電感之信號線係被電氣耦接於該晶片上所裝載之一積體電路。該晶片整合可變電感之電感值可被修改而無需改變該信號路徑、加長該信號線、或是安裝一開關至該信號線。反而是，當該晶片上之該積體電路被供電或運作時，藉由將被放置在靠近該信號線處之一或多接地線之接地，該可變電感之電感值可被修改或調整。

在另一實施例中，用以製造一晶片整合可變電感之一方法係被提供。該方法包含：在一晶片上製造一信號線，該信號線係電氣耦接於該晶片上之一積體電路。該方法另包含：製造一足夠靠近該信號線之接地線，以致於當該接地線在一電流路徑上耦接於一接地電位時該信號線具有一第一電感值，以及當該電流路徑被斷接時該信號線具有一第二電感值。該方法另包含：製造至少一控制單元，經組態以選擇性地斷接或接通該電流路徑。該接地線與該信號線可被放置在一共同金屬化層中，或可被放置在不同的金屬化層中。

又在另一實施例中，用以在經電氣耦接於該可變電感

之一積體電路的操作期間來調整一晶片整合可變電感之方法係被提供。該方法包含：自該積體電路引導一電子信號通過該可變電感之一信號線。該方法另包含：選擇性地將足夠靠近該信號線之該至少一接地線接地，以改變該信號線之一電感值。

又在另一實施例中，一設計結構係被提供，該設計結構係被實施在一機器可讀媒體內，用以設計與製造一電路。該電路包含一晶片整合可變電感，該晶片整合可變電感包括一信號線以及一接地線，該信號線係經組態以裝載一電子信號，該接地線係位於靠近該信號線處。該電路另包含至少一控制單元，該至少一控制單元係被放置在一電流路徑上，該電流路徑係將該接地線連接於一接地電位。該至少一控制單元係被組態以選擇性地斷接與接通該電流路徑，以致於當該電流路徑被斷接時該信號線具有一第一電感值，以及當該電流路徑被接通以將該接地線耦接於該接地電位時該信號線具有一第二電感值。該電路與該電路結構係位於設計檔案內或設計結構內(例如 GDSII 檔案)，其可被轉換至設計公司、製造商、客戶、或其他第三方。

【實施方式】

請參照第 1A 圖與第 1B 圖，一晶片整合可變電感(被概括標示為參考編號 10)係由一信號線 12 所組成，信號線

12係以一條導電材料之一代表形式來呈現，此條導電材料被埋入一介電材料之一絕緣層 14(第 1B 圖)內或被絕緣層 14 所包圍。電感 10 係置於一基底 16 上，基底 16 包括在其上及(或)其內所形成之至少一積體電路，而積體電路帶有具零件(feature)(零件 18 與 20 為代表，其被接觸於信號線 12)之該等裝置。零件 18 與 20 可包含金屬化線、接點、半導體材料、及(或)先前已形成在基底 16 上面及(或)裡面的電路元件之零件。基底 16 通常是包含一小塊半導體晶圓(包含一整個積體電路)之一晶片或晶粒(die)。

位於信號線 12 相反兩端之埠或端點 22 與 24 係藉由導電路徑 21 與 23(位於絕緣層 14 以及位於任何中間的介電層(例如像是介電層 25 與 27))來被電氣耦合於基底 16 上之零件 18 與 20。一電子信號係由基底 16 上之積體電路傳送至信號線 12。或者是，端點 22 與 24 可藉由在上面的金屬化層(未顯示)之導電路徑 21 與 23 來被耦合於基底 16 上之其他電路。

電感 10 之一接地線 26 係被放置在信號線 12 與基底 16 之間。接地線 26 係為直線條狀之導電材料，其被埋入絕緣層 25(第 1B 圖)並被絕緣層 25 所包圍。接地線 26(通常是在信號線 12 之下)係藉由至少絕緣層 14 與 25(其係提供電氣絕緣)之一部份的介電材料來與信號線 12 隔離。在代表的實施例中，電感 10 僅包括一信號線 12，且接地線 26 係被放置成實質平行於信號線 12。

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接地線的相反兩端係構成接點 28 與 30，接點 28 與 30 係以一種可選擇的方式分別藉由控制單元 32 與 34 來與接地端電氣耦合。控制單元 32 與 34(被顯示為存在於基底 16 上)係藉由在絕緣層 25 以及任何其他中間的介電層(例如像是絕緣層 27)內之導電路徑 31 與 33 來實體連接於接點 28 與 30。控制單元 32 與 34 可以是任何壓控裝置，但並未被限制於場效電晶體(例如像是一 p 型金屬氧化半導體(PMOS)電晶體或一 n 型金屬氧化半導體(NMOS)電晶體)與正－本－負(p-i-n)二極體(其具有熟知技藝人士所了解之結構)之中。當控制單元 32 與 34 兩者被適當的壓控信號所斷接(open)時，接地線 26 係代表一開路並為電子浮接。當控制單元 32 與 34 在斷接狀態時，接地線 26 的存在並不會顯著影響信號線 12 的電感值。當控制單元 32 與 34 兩者被適當的壓控信號接通(close)時，接地線 26 係處於一閉迴路，此閉迴路係由一短路電路耦接至接地電位。被接地的接地線 26 對於信號線 12 的靠近會造成電感 10 之電感值的改變，如同以下所另述。

在一替代實施例中，接地線 26 之接點 28 與 30 之一者可被一直綁在接地電位，並且只有接地線 26 之接點 28 與 30 之另一者進行切換以完成此閉迴路之接地動作。在另一替代實施例中，接地線 26 可被分段，並且額外的控制單元可被加入以選擇性地將該等片段耦接在一起以校調接地線 26 的有效長度。舉例來說，接地線 26 可包括一中央接點(未顯示)(此中央接點係靠近接點 28 與 30 之

一中間點)、以及對於此中央接點之一額外控制單元(未顯示)，用以當不同的接點組合被選擇時讓電感 10 具有兩個以上的電感值狀態。

藉由將接地線 26 與接地端耦合，控制單元 32 與 34 的操作對於電感 10 之電感值改變是有效的。當控制單元 32 與 34 被接通以及接地線 26 係藉由導電路徑 31 與 33 來被電氣耦合於接地端時，接地線 26 對於信號線 12 的靠近會降低電感 10 的電感值。此電感值之降低是二元的，因為：當控制單元 32 與 34 被斷接時，電感 10 具有一第一電感值；當控制單元 32 與 34 被接通時，電感 10 具有一第二電感值(第二電感值係小於第一電感值)。當控制單元 32 與 34 被接通時，接地線 26 變回到電感 10。電感 10 係可藉由電壓信號來以電子方式做調整，因為在基底 16 上之積體電路的操作期間，控制單元 32 與 34 可被斷接與接通。

接地線 26 的寬度 w_1 可以大於信號線 12 的寬度 w_2(其可運作以降低與基底 16 的耦合)。在一實施例中，接地線 26 的寬度 w_1 可以等於信號線 12 的寬度 w_2 乘以在信號線 12 與接地線 26 間之間隔的兩倍。或者是，信號線 12 與接地線 26 可以具有近似於相等的寬度，或是接地線 26 可以比信號線 12 窄。當控制單元 32 與 34 被接通以將接地線 26 連接於接地端時，接地線 26 之寬度 w_1 的降低會減少電感值的降低。信號線 12 與接地線 26 係藉由一縱橫比(代表線厚度與線寬度之比率)來加以表示。

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一般來說，接地線 26 的厚度 t_1 係小於信號線 12 的厚度 t_2，此係導致接地線 26 相較於信號線 12 具有一較小的縱橫比。信號線 12 與接地線 26 的長度係為近似地相等。當設計關聯於電感 10 之積體電路時，信號線 12 與接地線 26 的維度係被選擇。

信號線 12 與接地線 26 係為在成層堆疊之該等互連金屬線與該等貫孔內之零件，其係藉由傳統的後段製程(BEOL)處理(例如像是金屬鑲嵌製程以及雙重金屬鑲嵌製程)與對於基底 16 之積體電路上的一互連結構之定義來被製造於基底 16 上。舉例來說，信號線 12 可以是一置於 M5 層或 M6 層之金屬線，而接地線 26 可以是一置於 M12 層(比起對於接地線 12 之金屬化層更靠近基底 16)之金屬線。結果，絕緣層 14 通常會藉由中間的絕緣層(未顯示)(中間的絕緣層亦包含互連結構之該等導電零件)來與絕緣層 25 分開。典型地，在上面的金屬化層上，由 BEOL 處理所形成之金屬化零件通常會比形成於較低金屬化層上之金屬化零件還要厚，此即意味著信號線 12 可能比接地線 26 還要厚。

在一典型的製造程序中，藉由傳統的前段製程(FEOL)處理(亦即關聯於積體電路之該等半導體裝置之製造的處理)，於製造裝置直到第一 M1 層為止的期間內，零件 18 與 20、以及控制單元 32 與 34、以及關聯於電感 10 之積體電路係被形成於基底 16 內與基底 16 上。BEOL 處理被用來形成覆蓋在 M1 層上的每一金屬化層(M2

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層、M3 層等等)。特別是，BEOL 處理被用來在一較低金屬化層形成信號線 12 以及在一較高金屬化層形成接地線 26，以及形成經金屬填充之貫孔與形成用來定義導電路徑 21、23、31、33 之導電線。

為達到此目的，絕緣層 27 係被 BEOL 處理所使用與處理以定義經金屬填充之貫孔與導電線，而某些導電線係參與了導電路徑 21、23、31、33 的定義。絕緣層 25 係被使用在絕緣層 27 上，貫孔與溝槽(包括接地線 26 之一溝槽)係使用已知的石版印刷術與蝕刻技術來被定義於絕緣層 25 內，而溝槽與貫孔則以一所需導體來填充。在填充步驟後剩餘的任何額外負擔的導體係被平面化處理所移除，例如像是藉由一化學機械研磨(CMP)程序。如果有任何中間的金屬化層，則中間的金屬化層係使用 BEOL 處理來被應用。絕緣層 14 係被應用，貫孔與溝槽(包括信號線 12 之一溝槽)係使用已知的石版印刷術與蝕刻技術來被定義於絕緣層 14 之內，而溝槽與貫孔係被一所需導體所填充。在填充步驟後剩餘的任何額外負擔的導體係被平面化處理所移除，例如像是藉由一 CMP 程序。如果有任何覆蓋在上面的金屬化層的話，則覆蓋在上面的金屬化層接著使用 BEOL 處理來被應用以完成互連結構。

在本發明之一替代實施例中，接地線 26 可在 FEOL 處理過程中被形成於 M1 層。接著，上面的金屬化層(包括含有信號線 12 之金屬化層)係被應用如上所述。

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絕緣層 14、25、27 可包含熟知技藝人士所了解之任何有機或無機之介電材料，其可藉由任何個數的已知習知技術來加以沈積，例如像是濺鍍、旋轉塗佈應用、化學氣相沈積(CVD)程序、或電漿促進 CVD(PECVD)程序。用於絕緣層 14、25、27 之候選無機介電材料可包括(但不限於)二氧化矽、氟化矽玻璃(FSG)、以及這些介電材料的組合。構成絕緣層 14、25、27 之介電材料可由小於二氧化矽之介電常數(大約是 3.9)之一相關介電係數或介電常數所描述。絕緣層 14、25、27 之候選低 k 介電材料包括(但不限於)滲透性與非滲透性旋轉塗佈有機低 k 介電質(例如像是旋轉塗佈熱固聚芳香樹脂)、滲透性與非滲透性無機低 k 介電質(例如像是有機矽酸鹽玻璃、氫添加之矽碳氧化物(SiCOH)、碳摻雜氧化物)、以及有機與無機介電質之組合。來自此等低 k 材料之絕緣層 14、25、27 的製造係可運作以降低熟知技藝人士所能理解之經完成互連架構的電容。

對於信號線 12 與接地線 26 之合適導電材料包括(但不限於)銅(Cu)、鋁(Al)、這些金屬的合金、以及其他類似的金屬。這些金屬可藉由傳統的沈積製程(包括但不限於一 CVD 製程以及一電化學製程(像是電鍍以及非電鍍))來被沈積。一障壁層(未顯示)可覆蓋信號線 12 與接地線 26 之一或多邊。舉例來說，障壁層可包含由傳統沈積製程所應用之鈦與氮化鈦之雙層、或鉭或氮化鉭之雙層。導電路徑 21、23、31、33 可由相同於信號線 12 與接地

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線 26 的材料、以及被熟知技藝人士所了解之額外種類的材料(像是鎢(W)以及矽化金屬)所組成。

基底 16 可以是由半導體材料(包括但不限於矽(Si)、矽鍺(SiGe)、絕緣層上矽元件(SOI)層、以及其他類似之含有矽的半導體材料)所組成之一半導體晶圓。或者是，基底 16 可包含對於熟知技藝人士來說已知之陶瓷基底(例如像是一石英晶圓或一 AlTiC(Al_2O_3-TiC)晶圓)或是其他種類的基底(例如像是 III-V 族化合物之半導體基底)。

在使用中以及繼續參照於第 1A 圖與第 1B 圖，當控制單元 32 與 34 被切換到斷接以將接地線 26 置於一電子浮接狀態時，電感 10 係具有一第一第感值。在關聯的積體電路(包含電感 10)之操作過程中以及依據電感 10 之電感值調整的一需要，積體電路在適當的控制線(未顯示)上將該等電壓信號傳送至控制單元 32 與 34。該等電壓信號係作用以造成控制單元 32 與 34 改變狀態並接通一目前路徑(其透過導電路徑 31 與 33 來將接地線 26 連接於接地端)。舉例來說，電壓信號可電子地偏壓一場效電晶體或一 p-i-n 二極體(運作為控制單元 32 與 34)以導通各別源極/汲極區域之間的電流，其在接通電流路徑上將接地線 26 連接於一接地電位。接地線 26 之接地係運作以將電感 10 之電感值降低至一第二電感值(第二電感值係低於第一電感值)。結果，當關聯之積體電路運作時，電感 10 的電感值可被有效地調整，因此，電感值的改變係為可編程的。

參照第 2A 圖與第 2B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 38 係修正電感 10(第 1A 圖與第 1B 圖)之結構，藉由引入接地線 26 以外之接地線 40 與 42 來納入多條接地線。類似於接地線 26，接地線 40 與 42 為直線條狀之導電材料，其被埋入絕緣層 25，用以讓接地線 26 在一側有接地線 40，在另一側有接地線 42。接地線 40 與 42 亦被放置在信號線 12 與基底 16 之間，並與接地線 26 處於相同的金屬化層以及以如上關於接地線 26 所述之方式所形成。

藉由絕緣層 14 之介電材料部分，接地線 40 與 42 係與彼此、接地線 26、以及信號線 12 電氣絕緣。接地線 40 與 42 亦由相同的 BEOL 製程技術所形成，並與接地線 26 來自相同的 BEOL 冶金術，並通常與接地線 26 一起形成。接地線 40 與 42 與信號線 12 之維度上的關係可類似於信號線 12 與接地線 26 之維度上的關係。然而，各別接地線 26、40、42 之寬度及(或)厚度可不相同。

接地線 26 的相反兩端係構成接點 28 與 30，接點 28 與 30 分別藉由控制單元 32 與 34 以一可選擇方式以電流路徑來被電氣耦合於接地端。控制單元 32 與 34(其被描述為位於基底 16 上)係藉由絕緣層 25 內與任何其他中間介電層(例如絕緣層 27)內之導電路徑 31 與 33 來被實體連接於接點 28 與 30。

接地線 40 的相反兩端係構成接點 44 與 46，接點 44

與46分別藉由控制單元48與50以一可選擇方式來被電氣耦合於接地端。接地線42的相反兩端係構成接點52與54，接點52與54分別藉由控制單元56與58以一可選擇方式來被電氣耦合於接地端。當控制單元48與50以及控制單元56與58(具有類似於控制單元32與34之一結構)被共同接通時，係以一類似於控制單元32與34關於接地線26操作之方式運作，以各別及絕緣的電流路徑來選擇性地將各別接地線40與42連接至接地端。控制單元48、50、56、58可位於基底16上，並藉由相似於導電路徑31與33(第1B圖)之導電路徑(未顯示)耦合於各別的接地線40與42。為簡潔說明起見，導電路徑21、23、31、33係省略於第2B圖。

控制單元32與34、48與50、56與58之操作係作用以藉由將接地線26、40、42各別耦合於接地端，或者是藉由將接地線26、40、42之不同組合耦合於接地端，來改變電感38的電感值。當一或多組控制單元32與34、48與50、或56與58被接通時，被接地之一或多接地線26、40、42對於信號線12的靠近會降低電感38的電感值。相較於電感10(第1A圖與第1B圖)的二元維持，電感值之不同降低量係正比於經切換接地線26、40、42之數量。舉例來說，三接地線26、40、42之可選擇接地係允許電感38有八個不同的電感值，這些不同的電感值可僅藉由斷接與接通控制單元32與34、控制單元48與50、控制單元56與58、與在此之組合來被選擇。

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參照第 3A 圖與第 3B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 60 包括接地線 62 與 64，而非見於電感 10(第 1A 圖與第 1B 圖)之接地線 26。類似於接地線 26，接地線 62 與 64 係由直線條狀之導電材料所組成，其被埋入絕緣層 14，用以讓信號線 12 在一側有接地線 62，在另一側有接地線 64。接地線 62 與 64 係位於和信號線 12 相同之金屬化層內。藉由部份的絕緣層 14，接地線 62 與 64 係彼此電氣絕緣、以及與信號線 12 電氣絕緣。接地線 62 與 64 亦藉由相同的 BEOL 製程技術所形成，並來自與信號線 12 相同的 BEOL 冶金術，並通常與信號線 12 一起形成。接地線 62、64 與信號線 12 之維度上的關係可類似於信號線 12 與接地線 26 之維度上的關係(第 1A 圖與第 1B 圖)。然而，接地線 62 與 64 之每一者係具有不同的寬度。

接地線 62 的相反兩端係構成接點 66 與 68，接點 66 與 68 係以一種可選擇的方式分別藉由控制單元 70 與 72 以一電流路徑來與接地端電氣耦合。接地線 64 的相反兩端係構成接點 74 與 76，接點 74 與 76 係以一種可選擇的方式分別藉由控制單元 78 與 80 以另一電流路徑來與接地端電氣耦合。當控制單元 70 與 72 以及控制單元 78 與 80(具有類似於控制單元 32 與 34 之一結構)被共同接通時，係以一類似於控制單元 32 與 34 關於接地線 26 操作之方式運作，以各別及絕緣的電流路徑來選擇性地將

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各別接地線 62 與 64 耦合至接地端。控制單元 70、72、78、80 可位於基底 16 上並且藉由類似於導電路徑 31 與 33(第 1B 圖)之導電路徑(未顯示)來與各別的接地線 62 與 64 耦合。為簡潔說明起見，導電路徑 21、23、31、33 係被忽略於第 3B 圖。

控制單元 70 與 72 以及控制單元 78 與 80 的操作係作用以藉由將接地線 62、64 各別耦合於接地端，或者是藉由將接地線 62、64 二者皆耦合於接地端，來改變電感 60 的電感值。當一或二組之控制單元 70 與 72、或 78 與 80 被接通時，被接地之接地線 62、64 對於信號線 12 的靠近會降低電感 60 的電感值。接地線 62 與 64 之可選擇接地係允許電感 60 有三種不同的電感值，這些不同的電感值可僅藉由斷接與接通控制單元 70 與 72、以及控制單元 78 與 80 來被選擇。

在一替代性實施例中，一電容屏(未顯示)可使用介於接地線 62 與 64 之一或兩者以及信號線 12 間之一串貫孔來定義。選擇性的電容屏係以類似於電容屏 106(第 6A 圖與第 6B 圖)之方式運作。

參照第 4A 圖與第 4B 圖(在此，相似的參考編號係代表在第 2A 圖與第 2B 圖中以及第 3A 圖與第 3B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 81 包括接地線 26、40、42(該等接地線係在與信號線 12 不同之金屬化層)以及接地線 62、64(該等接地線係在與信號線 12 相同之金屬化層)。因此，藉由連接不同的

接地線 26、40、42、62、64 或排列或組合，電感 81 之電感值可被切換到正比於其個數之多個不同電感值。在一實施例中，接地線 26 可被切換到接地處，而其他的接地線 40、42、62、64 不是被單獨切換就是被一起切換，以調整電感 81。在此實施例中，電感 81 可垂直地與水平地調整。為簡潔說明起見，導電路徑 21、23、31、33 係省略於第 4B 圖中。

參照第 5A 圖與第 5B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 82 係修正電感 10(第 1A 圖與第 1B 圖)之結構係藉由除了接地線 26 以外之接地線 84 與 86 的引入，來納入一堆疊之接地線。類似於接地線 26，接地線 84 與 86 係為直線條狀之導電材料，其被分別埋入絕緣層 83 與 85，用以讓接地線 84 介於接地線 26 與信號線 12 之間而接地線 26 則是介於接地線 84 與接地線 86 之間。絕緣層 83 與 85 係類似於絕緣層 14 與 25，並與絕緣層 25 一起堆疊。接地線 84 可位於一金屬化層，此金屬化層係介於包含信號線 12 與接地線 26 之該等金屬化層之間；而接地線 26 可位於一金屬化層，此金屬化層係介於包含接地線 84 與接地線 86 之該等金屬化層之間。舉例來說，信號線 12 可為一置於 M6 層之金屬線，接地線 86 可為一置於 M2 層之金屬線，接地線 26 可為一置於 M3 層之金屬線，以及接地線 84 可為一置於 M4 層之金屬線。

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至少藉由絕緣層 14、25、83、85 之部份，讓接地線 84 與 86 與彼此、接地線 26、以及信號線 12 電氣絕緣。該等接地線 84 與 86 亦可由相同的 BEOL 製程技術所形成，並與接地線 26 來自相同的 BEOL 冶金術。接地線 84、86 與信號線 12 之維度關係可類似於信號線 12 與接地線 26 間之維度關係。然而，如第 5A 圖與第 5B 圖所示，接地線 84、86、26 之每一者可具有不同的寬度及(或)厚度。

接地線 84 之相反兩端係構成接點 88 與 90，接點 88 與 90 係分別藉由控制單元 92 與 94 以一可選擇方式依一電流路徑來電氣耦接於接地端。接地線 86 之相反兩端係構成接點 96 與 98，接點 96 與 98 係分別藉由控制單元 100 與 102 以一可選擇方式依另一電流路徑來電氣耦接於接地端。當被同時接通時，控制單元 92、94 與控制單元 100、102(具有類似於控制單元 32、34 之結構)以一類似於控制單元 32、34 對於接地線 26 之操作方式來運作，以選擇性地將個別接地線 84、86 耦接於接地端。控制單元 92、94、100、102 可位於基底 16 上，並藉由類似於導電路徑 31、33(第 1B 圖)之導電路徑(未顯示)來與各別接地線 84、86 耦接。為簡潔說明起見，導電路徑 21、23、31、33 係被忽略於第 5B 圖。

藉由將接地線 84、86、26 分別與一接地電位耦接之方式，或者是藉由將接地線 84、86、26 之不同組合與接地電位耦接的替代方式，控制單元 32、34 與控制單元 92、

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94及控制單元100、102之操作係有效改變電感82的電感值。當控制單元32、34與控制單元92、94及控制單元100、102之一或多組被接通時，經接地之接地線84、86、26之一或多組對於信號線12的靠近會降低電感82的電感值。電感值之不同降低的個數係正比於經切換之接地線84、86、26的個數。舉例來說，接地線84、86、26之選擇性接地係允許電感82有八個不同的電感值，此等電感值可僅藉由斷接或接通該等控制單元32、34與控制單元92、94及控制單元100、102來加以選擇。

當沒有任何接地線26、84、86被耦接至接地端時，電感82的電感值被最大化。接地線26、84、86之一或多者與接地端之耦接係運作以降低電感82之電感值。若最接近信號線12之接地線84耦接於接地端並且接地線84與下層接地線26與86之任一者同寬或更寬，則不論接地線26與86之任一者是否亦耦接於接地端，電感82之電感值係被最小化。

類似於電感38之接地線26、40、42(第2A圖與第2B圖)，電感82在與接地線26、84、86之一或多者相同的金屬化層內可另包括額外的接地線(未顯示)。或者是，類似於電感60之接地線62、64(第3A圖與第3B圖)，電感82在與信號線12相同的金屬化層內可另包括額外的接地線(未顯示)。

參照第6A圖與第6B圖(在此，相似的參考編號係代表在第1A圖與第1B圖中相似的零件)並根據本發明之一替

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代實施例，亦類似於電感 10(第 1A 圖與第 1B 圖)的一晶片整合可變電感 104 係納入一電容屏 106。電容屏 106 係放置在介於信號線 12 與接地線 26 之間的絕緣層 83 內，因此處在介於該等含有信號線 12 與接地線 26 之金屬化層間的一金屬化層。舉例來說，信號線 12 可為置於 M6 層之一金屬線，電容屏 106 可為置於 M3 層之一金屬線，而接地線 26 可為置於 M2 層之一金屬線。藉由至少絕緣層 14、25、83 之該等部分，信號線 12、接地線 26、電容屏 106 係與彼此電氣絕緣。電容屏 106 亦由與形成信號線 12 與接地線 26 之相同 BEOL 製程技術所形成，並來自相同或類似的 BEOL 冶金術。為簡潔說明起見，導電路徑 21、23、31、33 係省略於第 6B 圖。

電容屏 106 包括複數個實質相同的片段 108，該等片段 108 係以一彎曲形狀來電子鏈結在一起。該等片段 108 係被建構與擺放以定義該等間隙，用以讓電容屏 106 不像一連續的接地平面或接地板，好讓接地線 26 之切換在電容屏 106 的存在下可影響信號線 12 之電感值。電容屏 106 係被一直綁在接地端，因此不是被選擇性地切換。

電容屏 106 係降低介於信號線 12 與基底 16 之間的電容性耦合，其賦予電感 104 對於接地線 26 之兩不同狀態有一相似的 Q 因子。此外，電容屏 106 幫助提供將電感 104 之信號線 12 隔離於基底 16 上之積體電路內的剩餘電路。在一替代實施例中，電容屏 106 可具有一梳子形狀。

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參照第 7A 圖與第 7B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，一晶片整合可變電感 118 包括一螺旋形狀之信號線 120 以及一螺旋形狀之接地線 126，接地線 126 係置於信號線 120 與基底 16 之間。類似於信號線 12 與接地線 26(第 1A 圖與第 1B 圖)，信號線 120 以及接地線 126 每一者係形成於一平面條狀之導電材料。信號線 120 係被埋入絕緣層 14 並被絕緣層 14 所圍繞；類似地，接地線 126 係被埋入絕緣層 25 並被絕緣層 25 所圍繞。信號線 120 與接地線 126 之螺旋形狀係實質相同。埠或端點 123、124(位於信號線 120 之相反兩端)係藉由導電路徑 21、23 電氣耦接於基底 16 上之積體電路的零件 18、20。

藉由用以提供呈電氣絕緣之該等絕緣層 14、25 之部份，接地線 126(通常位於信號線 120 下方)係與信號線 120 隔開。如同在此對於信號線 12 與接地線 26 之描述(第 1A 圖與第 1B 圖)，信號線 120 與接地線 126 係藉由傳統的 BEOL 製程技術並自用於此等製程技術之傳統 BEOL 冶金術來形成於不同的金屬化層中。舉例來說，信號線 120 可置於 M5 層或 M6 層，而接地線 126 可置於靠近基底 16 之 M2 層。如同可被熟知技藝人士所了解，信號線 120 與接地線 126 可包括額外的共同中心排列之平面螺旋線(未顯示)與下拉貫孔及地下通道。信號線 120 與接地線 126 係以具有多邊形之方式描述於第 7A 圖，在代表

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性實施例中則為一八邊形。然而，信號線 120 與接地線 126 可被替代地纏繞為一具有長方形、圓形、或橢圓形之螺旋形，或是一具有不同個數之邊的多邊形。

接地線 126 的相反兩端係構成接點 128 與 130，接點 128 與 130 係以一種可選擇的方式分別藉由控制單元 32 與 34 依一電流路徑來與接地端電氣耦合。接點 128 與 130 係藉由導電路徑 31 與 33 實質耦接於控制單元 32 與 34。當控制單元 32 與 34 兩者由適當的電壓控制信號切換至斷接時，接地線 126 係為一開路並為電子浮接。當控制單元 32 與 34 處於斷接狀態時，浮接的接地線 126 並不會顯著影響信號線 120 的電感性。當控制單元 32 與 34 兩者由適當的電壓控制信號接通時，接地線 126 係處於一閉迴路電流路徑，其由一短路電路耦接至一接地電位。在一替代實施例中，接地線 126 之接點 128、130 之一者可被持續綁在接地端，只有接地線 126 之接點 128、130 的另一者切換時完成至接地電位之此閉迴路電路。

藉由將接地線 126 選擇性耦接於接地電位，控制單元 32 與 34 的操作可有效改變電感 118 的電感值。當控制單元 32 與 34 被導通以及接地線 126 在電流路徑被電氣耦接於接地端時，接地線 126 對於信號線 120 的靠近會降低電感 118 的電感值。此降低係為二元的，因為：當控制單元 32 與 34 被切換至斷接時，電感 118 具有一第一電感值；當控制單元 32 與 34 被切換至接通時，電感 118 具有一小於第一電感值之第二電感值。當控制單元

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32 與 34 被接通時，接地線 126 不是在電感 118 之信號路徑上。電感 118 係為電子可調的，因為：在基底 16 上之積體電路的操作期間，控制單元 32 與 34 可被斷接與接通。

參照第 8A 圖與第 8B 圖(在此，相似的參考編號係代表在第 1A 圖與第 1B 圖中相似的零件)並根據本發明之一替代實施例，亦類似於電感 118(第 7A 圖與第 7B 圖)之一晶片整合可變電感 140 係納入一電容屏 142。電容屏 142 被放置在介於信號線 120 與接地線 126 間之一金屬化層內。電容屏 142 係被放置在介於信號線 120 與接地線 126 間之絕緣層 83 內，因此處在含有信號線 120 與接地線 126 之該等金屬化層之間的一金屬化層。舉例來說，信號線 120 可為置於 M6 層之一金屬線，電容屏 142 可為置於 M3 層之一金屬線，而接地線 126 可為置於 M2 層之一金屬線。藉由絕緣層 14、83、25 之部份，信號線 120、接地線 126、與電容屏 142 係與彼此電氣絕緣。電容屏 142 亦被形成信號線 120 與接地線 126 的相同 BEOL 製程技術所形成，並來自相同或相似的 BEOL 冶金術。為簡潔說明起見，導電路徑 21、23、31、33 係省略於第 8B 圖。

電容屏 142 包括以屏線 144、146 形式存在之複數個實質相同的平行線片段或條(其延伸自一中央橋 148 的相反兩邊緣)。每一鄰接對之屏線 144、146 係被一間隔隔開，用以讓電容屏 142 不會定義一連續接地平面或板，以及

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用以讓接地線 126 之切換在電容屏 142 的存在下可影響信號線 120 的電感值。電容屏 142 係被持續綁在接地端。

電容屏 142 係降低介於信號線 120 與基底 16 之電容性耦合，以賦予電感 140 一最佳化的 Q 值。此外，電容屏 142 係幫助提供將電感 140 之信號線 120 隔離於基底 16 上之積體電路內的剩餘電路。或者是，電容屏 142 可具有一不同樣式之導電零件，例如像是發現在一放射狀類型之屏，甚至於是該等屏線被引導至垂直於信號線 120。

第 9 圖顯示一用以製造一積體電路之示範性設計流 160 的方塊圖。設計流 160 可依據被設計之積體電路的種類來改變。舉例來說，一用以建構一特定應用積體電路(ASIC)之設計流 160 將不同於一用以建構一標準元件之設計流 160。設計結構 164 係為設計流程 162 的一輸入，並可來自一智財(IP)供應商、一核心發展商、或其他設計公司。設計結構 164 包含以電路圖與佈局圖或硬體描述語言(HDL)(例如像是 VHDL 或是 Verilog)形式存在之一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140。由於 HDL 表示方式一般係定義要被一電路設計所執行之邏輯或功能，一積體電路之 HDL 表示方式在許多方面係類似於一軟體程式。如同在以下之第 10 圖內容中所描述，設計結構 164 可以位於一或多機器可讀媒體上。舉例來說，設計結構 164 可以是一積體電路(包括一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140)之一文字檔或一圖形表示方式。設計流程

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162 將積體電路(包括一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140)合成(或轉換)為一網路連線表(netlist)176。舉例來說，網路連線表 176 係為粗線、電晶體、邏輯閘、控制電路、I/O、模型等等之一列表，並描述在一積體電路設計內與其他元件及電路的連接關係並被記錄在至少一機器可讀媒體上。

設計流程 162 包括各種輸入之使用；舉例來說，來自函式庫元件 166(其可針對一給定製造技術(例如，不同技術節點、32nm、45 nm、90nm 等等)放置一組常用的元件、電路、以及裝置，包括模型、佈局、以及符號表示方式)之輸入、製造規格 168 之輸入、描述資料 170 之輸入、驗證資料 172 之輸入、設計規則 174 之輸入、以及測試資料檔案 178 之輸入(其可包括測試樣式與其他測試資訊)。舉例來說，設計流程 162 另包括標準電路設計流程，例如像是時序分析、驗證工具、設計規則檢查器、配置與繞線工具等等。一熟知積體電路設計之技藝人士可明瞭可能的電子設計自動化工具與應用(可被用於設計流程 162 之替代實施例中)之範圍。

設計流程 162 最終將包括一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140 之電路與剩餘的積體電路設計(如果適用的話)轉換成一最後設計結構 180(例如儲存在一 GDS 儲存媒體內之資訊)。最後設計結構 180 可包括資訊，像是測試資料檔案、設計內容檔案、製造資料、佈局參數、線、金屬之層、貫孔、形狀、測

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試資料、透過製造線之繞線資料、以及半導體製造器所需以製造一電路(含有一或多晶片整合可變電感 10、38、60、81、82、104、118、或 140)的任何其他資料。最後設計結構 180 可接著進行到設計流 160 之階段 182；舉例來說，階段 182 是最後設計結構 180 進行到下線(tape-out)之處，階段 182 在此係被送去製造、被送到另一設計公司、或回到客戶手上。

第 10 圖接著說明一裝置 190，設計流程 162 的各種步驟可在裝置 190 內執行。在所述實施例中，裝置 190 係被實作為一伺服器或多使用者之電腦(其係透過網路 192 耦接於一或多客戶電腦 194)。為了本發明的目的，每一電腦 190、194 實際上可代表任何種類的電腦、電腦系統、或其他可編程電子裝置。此外，每一電腦 190、194 可利用一或多連成網路的電腦來實作，例如在一叢集或其他分散式電腦系統中。在替代方案中，電腦 190 可被實作在單一電腦中或其他可編程電子裝置(例如一桌上型電腦、一膝上型電腦、一手持電腦、一手機、一機上盒等等)中。

電腦 190 通常包括一中央處理單元(CPU)196；CPU 196 包括耦接於記憶體 198 之至少一微處理器；記憶體 198 可代表該等隨機存取記憶體(RAM)裝置，包含電腦 190 之主要儲存以及任何補充層級之記憶體(例如快取記憶體、非揮發或備份記憶體(例如可編程或快閃記憶體)、唯讀記憶體等等)。此外，記憶體 198 可被認為包括實際

上位於電腦 190 別處之記憶體儲存(例如在 CPU 196 之一處理器內的任何快取記憶體)以及被用來作為一虛擬記憶體之任何儲存容量(例如像是儲存在一大容量裝置 200 上，或是在耦接於電腦 190 之其他電腦上)。通常電腦 190 亦接收一些輸入與輸出，用以在外部對資訊進行通訊。為提供介面給使用者或操作者，電腦 190 通常包括一使用者介面 202，其納入一或多使用者輸入裝置(例如，一鍵盤、一滑鼠、一軌跡球、一搖桿、一觸控板、及(或)一麥克風、其他者)以及一顯示(例如，一 CRT 螢幕、一 LCD 顯示板、及(或)一喇叭、其他者)。除此之外，使用者之輸入可透過其他的電腦或終端來接收。

對於額外的儲存，電腦 190 亦可包括一或多大容量儲存裝置 200，例如一軟碟或其他可移除式碟機、一硬碟機、一直接存取儲存裝置(DASD)、一光碟機(例如，一 CD 碟機、一 DVD 碟機等等)、及(或)一磁帶機、其他者。此外，電腦 190 可包括與一或多網路 192(例如，一 LAN、一 WAN、一無線網路、及(或)網際網路、其他者)連接之一介面 204，以允許與其他電腦及電子裝置之資訊通訊。應理解到，如同在技藝中所知，在 CPU 196 與元件 198、200、202、204 每一者之間，電腦 190 通常包括合適的類比及(或)數位介面。其他的硬體環境係被考量於本發明之內容內。

如同將於其下所詳述，電腦 190 係運作在一作業系統 206 的控制之下並加以執行，或依靠各種電腦軟體應用

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程式、元件、程式、物件、模組、資料結構等等。此外，各種應用程式、元件、程式、物件、模組等等亦可執行於透過網路 192(例如，在一分散式或主從架構之計算環境中)來耦接於電腦 190 之其他電腦的一或多處理器上，藉此用以實作電腦程式之該等功能所需的處理可被分配到網路上之多個電腦。

一般來說，不論是否被實作為一部份的作業系統或特定應用程式、元件、程式、物件、模組或一串指令、或甚至是在此之一子集合，經執行以實作本發明該等實施例之常式在此將代表「電腦程式碼」或僅為「程式碼」。程式碼通常包含一或多指令，該等指令有時常駐在一電腦內之各種記憶體與儲存裝置，當該等指令被電腦內之一或多處理器讀取或執行時，會造成此電腦執行該等必要的步驟來執行用以實施本發明各式態樣的步驟與元件。此外，儘管本發明具有並將於其後描述為全功能電腦與電腦系統之情境內，熟知技藝人士將理解到本發明之各式實施例能夠被分配為各種形式之一程式產品，並理解到不論被用來實際實作此分配之機器可讀媒體的特殊種類為何，本發明係平等地使用。機器可讀媒體的範例包括但不限於可觸碰、可記錄種類的媒體，例如像是揮發與非揮發記憶體裝置、軟碟與其他可移除碟、硬碟機、磁帶、光碟(例如 CD-ROM、DVD 等等)、其他者、以及傳送種類媒體(例如像是數位與類比通訊鏈結)。

此外，此後所述之各種程式碼可根據應用加以辨識(在

此應用內，程式碼係被實作在本發明之一特定實施例)。然而，應理解到，所採用之任何特定程式命名僅為方便之用，因此本發明不應被限制於僅在由此命名所辨識及(或)意味之任何特定應用。再者，給定通常不限個數的方法(在此，電腦程式可被組織為常式、程序、方法、模組、物件、及其相似者)以及各式方法(在此，程式功能可位在常駐於一典型電腦之各種軟體層(例如，作業系統、函式庫、API、應用、小程式等等)間)，應理解到本發明未被限制於在此所述之程式功能的特定組織與配置。

為了實作在第 9 圖之設計流程 162 內的各種活動，電腦 190 包括一些軟體工具，舉例來說，軟體工具包括一設計流程工具 208。與積體電路設計、驗證、及(或)測試所結合使用之其他工具亦可被用在電腦 190 內。此外，儘管設計流程工具 208 被顯示在單一電腦 190 中，具有快速揭露優勢之熟知技藝人士將理解到通常此等工具會被擺放在分離的電腦，特別是當多個個體參與一積體電路設計之邏輯設計、整合、與驗證時。因此，本發明之該等實施例並未被限於第 10 圖所描繪之單一電腦實作。

熟知技藝人士將理解到第 9 圖與第 10 圖所描繪之示範性環境並非意圖限制本發明之實施例。實際上，熟知技藝人士將理解到其他替代的硬體及(或)軟體環境係可被使用。

在此對於詞彙的參照(例如像是「垂直」、「水平」等等)

係作為範例而非限制之用，以建立參考之框架。此處所使用之詞彙「水平」係被定義為平行於一半導體基底之傳統平面的平面，而不論它實際的三維空間方向為何。如同所定義的，詞彙「垂直」係代表垂直於水平之一方向。該等詞彙(例如像是「上」、「以上」、「以下」、「邊」(像是在「側邊」中)、「上面」、「下面」、「上方」、「下方」、「下」)係被定義為關於水平平面。可了解到，各種其他框架的參照可被用來描述本發明而不脫離本發明之精神與範圍。亦了解到，本發明之該等框架沒有必要在圖中被縮放顯示。此外，對於用在詳細描述或是申請專利範圍中之詞彙「包括」、「具有」、「具」、「有」、或在此之變形的範圍，此等詞彙係意欲被含括在類似於詞彙「包含」之方式中。

雖然本發明已以各種實施例的描述所述並且該等實施例被相當詳細地描述，然申請者並非意圖將所附申請專利範圍限定或以任何方式限制在此等細節中。對於熟習技藝人士來說，將可輕易明白另外的優點與修正形式。因此在較廣態樣中之本發明並未被限制在被顯示與被描述之特定細節、代表裝置與方法、以及所述範例中。因此可分離於此等細節而不脫離申請者一般發明概念之精神和範圍。

【圖式簡單說明】

第 1A 圖係根據本發明一實施例由一信號線與一經切換接地線所組成之一晶片整合可變電感之透視圖，在此所包圍的介電材料為簡潔起見係省略。

第 1B 圖係第 1A 圖電感之一剖面圖。

第 2A 圖與第 2B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由一信號線與多經切換接地線所組成。

第 3A 圖與第 3B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由實質被放置在單一金屬化層之一信號線與多經切換接地線所組成。

第 4A 圖與第 4B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由實質被放置在不同金屬化層之一信號線與多經切換接地線所組成。

第 5A 圖與第 5B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，其係由實質被放置在單一金屬化層之一信號線與該等經切換接地線之堆疊所組成。

第 6A 圖與第 6B 圖係根據本發明一替代實施例之類似於第 1A 圖與第 1B 圖之晶片整合可變電感的透視圖與剖面圖，在此一電容屏係置於信號線與接地線之間。

第 7A 圖係根據本發明一實施例由一螺旋形信號線與一經切換螺旋形接地線所組成之一晶片整合可變電感之

透視圖，在此所包圍的介電材料為簡潔起見係省略。

第 7B 圖係第 7A 圖電感之一剖面圖。

第 8A 圖與第 8B 圖係根據本發明一替代實施例之類似於第 7A 圖與第 7B 圖之晶片整合可變電感的透視圖與剖面圖，在此一電容屏係置於信號線與接地線之間。

第 9 圖係一示範性設計流的方塊圖。

第 10 圖係適於實作第 9 圖流程之一電腦系統內之該等主要硬體元件的一方塊圖。

【主要元件符號說明】

10、38、60、81、82、104、118、140	晶片整合可變電感
12、120	信號線
14、25、27、83、85、122	絕緣層
16	基底
18、20	零件
21、23、31、33	導電路徑
22、24、123、124	端點
26、40、42、62、64、84、86、126	接地線
28、30、44、46、52、54、66、68、74、76、88、90、96、98、128、130	接點
32、34、48、50、56、58、70、72、78、80、92、94、100、102	控制單元

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106、142	電容屏
108	片段
144、146	屏線
148	中央橋
160	設計流
162	設計流程
164	設計結構
166	函式庫元件
168	製造規格
170	描述資料
172	驗證資料
174	設計規則
176	網路連線表
178	測試資料檔案
180	最後設計結構
182	階段
190	裝置
192	網路
194	客戶電腦
196	中央處理單元
198	記憶體

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200	大容量裝置
202	使用者介面
204	網路介面
206	作業系統
208	設計流程工具

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發明專利說明書

補充

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫；惟已有申請案號者請填寫）

※ 申請案號：98101836

※ 申請日期：2009 年 1 月 17 日　　※IPC 分類：H01L23/58(2006.01)

一、發明名稱：（中文/英文）

晶片整合之壓控可變電感，製造與調整此可變電感之方法，以及整合此可變電感之設計結構

ON-CHIP INTEGRATED VOLTAGE-CONTROLLED VARIABLE INDUCTOR, METHODS OF MAKING AND TURNING SUCH VARIABLE INDUCTORS, AND DESIGN STRUCTURES INTEGRATING SUCH VARIABLE INDUCTORS

二、中文發明摘要：

揭露關於晶片整合可變電感、製造與調整晶片整合可變電感之方法、以及實施一包含晶片整合可變電感之電路的設計結構。電感通常包括一經組態以裝載一電子信號之信號線、一位於靠近信號線處之接地線、以及經電氣耦接於接地線之至少一控制單元。至少一控制單元係經組態以斷接與接通將接地線連接於接地電位之電流路徑，以致於改變信號線之電感性。

三、英文發明摘要：

On-chip integrated variable inductors, methods of making and tuning an on-chip integrated variable inductor, and design structures embodying a circuit containing the on-chip integrated variable inductor. The inductor generally

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includes a signal line configured to carry an electrical signal, a ground line positioned in proximity to the signal line, and at least one control unit electrically coupled with the ground line. The at least one control unit is configured to open and close a current path connecting the ground line with a ground potential so as to change an inductance of the signal line.

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七、申請專利範圍：

1. 一種晶片整合可變電感，至少包含：

一信號線，經組態以導通一電子信號；

一第一接地線，位於靠近該信號線之處；以及

至少一控制單元，放置在連接該第一接地線與一接地電位之一第一電流路徑上，該至少一控制單元係經組態以選擇性地斷接與接通該第一電流路徑，以致於當該第一電流路徑被斷接時該信號線具有一第一電感值，以及當該第一電流路徑被接通以將該第一接地線耦接於該接地電位時該信號線具有一第二電感值。

2. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一積體電路，電氣耦接於該信號線以用以與該電子信號通訊；以及

一晶片，裝載該第一接地線、該信號線、以及該積體電路，該第一接地線係位於該信號線以及該晶片之間。

3. 如申請專利範圍第 2 項所述之晶片整合可變電感，其中該至少一控制單元係製造在該晶片上。

4. 如申請專利範圍第 1 項所述之晶片整合可變電感，其中

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該信號線係一第一平面螺旋繞線，以及該第一接地線係位於該第一平面螺旋繞線下之一第二平面螺旋繞線。

5. 如申請專利範圍第 1 項所述之晶片整合可變電感，其中該信號線係一第一平面導線，以及該第一接地線係一第二平面導線，該第二平面導線係置於與該第一平面導線相關之一空間關係中。

6. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一介電材料，包圍該信號線與該第一接地線，一部份之該介電材料係置於該信號線與該第一接地線之間以避免該信號線與該第一接地線間之電子導通。

7. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一電容屏，置於該第一接地線與該信號線之間。

8. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一晶片，裝載該第一接地線與該信號線；以及

一積體電路，經裝載於該晶片上，該積體電路電氣耦接於該信號線以用以與該電子信號通訊。

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9. 如申請專利範圍第 1 項所述之晶片整合可變電感，另包含：

一第二接地線，位於靠近該信號線之處，該第二接地線係經組態以在一第二電流路徑中選擇性地耦接於接地電位，該第二電流路徑係與該第一電流路徑電氣絕緣，以及當該第二接地線耦接於該接地電位時該信號線係具有一第三電感值。

10. 如申請專利範圍第 9 項所述之晶片整合可變電感，其中該第一接地線被含在一第一金屬化層中，該第二接地線被含在一第二金屬化層中，該信號線被含在一第三金屬化層中，以及該第一接地線、該第二接地線、以及該信號線具有一堆疊配置，在該堆疊配置中該第二金屬化層被放置在該第一金屬化層與該第三金屬化層之間。

11. 如申請專利範圍第 9 項所述之晶片整合可變電感，其中該第一接地線、該第二接地線、以及該信號線被含在一共同金屬化層，以及該信號線被放置在該第一接地線與該第二接地線之間。

12. 如申請專利範圍第 9 項所述之晶片整合可變電感，其中該第一接地線與該第二接地線被含在一第一金屬化層中，以及該信號線被含在不同於該第一金屬化層之一第二金屬化層中。

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13. 如申請專利範圍第 9 項所述之晶片整合可變電感，另包含：

一第三接地線，位在靠近該信號線之處，該第三接地線係經組態以在一第三電流路徑中選擇性地耦接於接地電位，該第三電流路徑係與該第一電流路徑與該第二電流路徑電氣絕緣，以及當該第三接地線耦接於該接地電位時該信號線係具有一第四電感值。

14. 如申請專利範圍第 13 項所述之晶片整合可變電感，其中該第一接地線、該第二接地線、以及該信號線被含在一第一金屬化層，以及該第三接地線被放置在不同於該第一金屬化層之一第二金屬化層。

15. 一種製造一晶片整合可變電感之方法，該方法至少包含以下步驟：

在一晶片上製造一信號線，該信號線係電氣耦接於該晶片上之一積體電路；

製造一第一接地線，該第一接地線係足夠靠近該信號線，以致於當該第一接地線在一第一電流路徑中耦接於一接地電位時該信號線具有一第一電感值，以及當該第一電流路徑斷接時該信號線具有一第二電感值；以及

製造至少一控制單元，該控制單元係經組態以選

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擇性地斷接或接通該第一電流路徑。

16. 如申請專利範圍第15項所述之方法，其中該第一接地線係被製造於一第一金屬化層上，以及該信號線係被製造在不同於該第一金屬化層之一第二金屬化層上。

17. 如申請專利範圍第15項所述之方法，其中該第一接地線以及該信號線係被製造在相同金屬化層上。

18. 如申請專利範圍第15項所述之方法，另包含以下步驟：

製造一第二接地線，該第二接地線係足夠靠近該信號線，以致於當該第二接地線在一第二電流路徑上耦接於該接地電位時該信號線具有一第三電感值，以及當該第二電流路徑斷接時該信號線具有該第二電感值；以及

製造至少一控制單元，該控制單元係經組態以選擇性地斷接與接通該第二電流路徑。

19. 一種於一積體電路之操作期間調整一晶片整合可變電感之方法，該積體電路係電氣耦接於該晶片整合可變電感，該方法至少包含以下步驟：

自該積體電路引導一電子信號通過該晶片整合可變電感之一信號線；以及

選擇性地將足夠靠近該信號線之至少一接地線接

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地，以改變該信號線之一電感值。

20. 如申請專利範圍第 19 項所述之方法，其中選擇性地將該至少一接地線接地之步驟另包含以下步驟：

操作至少一控制單元，以將該至少一接地線電氣耦接於一接地電位。

21. 如申請專利範圍第 20 項所述之方法，其中操作該至少一控制單元之步驟另包含以下步驟：

將一電壓信號傳送至該至少一控制單元，該至少一控制單元係有效以電氣耦接該至少一接地線至該接地電位。

22. 一種實施於一機器可讀媒體以用來設計與製造一電路之設計結構，該電路包含：

一晶片整合可變電感，該晶片整合可變電感包含一信號線以及一接地線，該信號線經組態以導通一電子信號，該接地線係位於靠近該信號線之處；以及

至少一控制單元，該至少一控制單元被放置在將該接地線連接到一接地電位之一電流路徑上，該至少一控制單元係經組態以選擇性地斷接與接通該電流路徑，以致於當該電流路徑被斷接時該信號線具有一第一電感值，以及當該電流路徑被接通以將該接地線耦接於該接地電位時該信號線具有一第二電感值。

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23. 如申請專利範圍第 22 項所述之設計結構，其中該信號線係一第一平面螺旋繞線，以及該接地線係一位於該第一平面螺旋繞線下方之一第二平面螺旋繞線。

24. 如申請專利範圍第 22 項所述之設計結構，其中該信號線係一第一平面導線，以及該接地線係一第二平面導線，該第二平面導線係置於與該第一平面導線相關之一空間關係中。

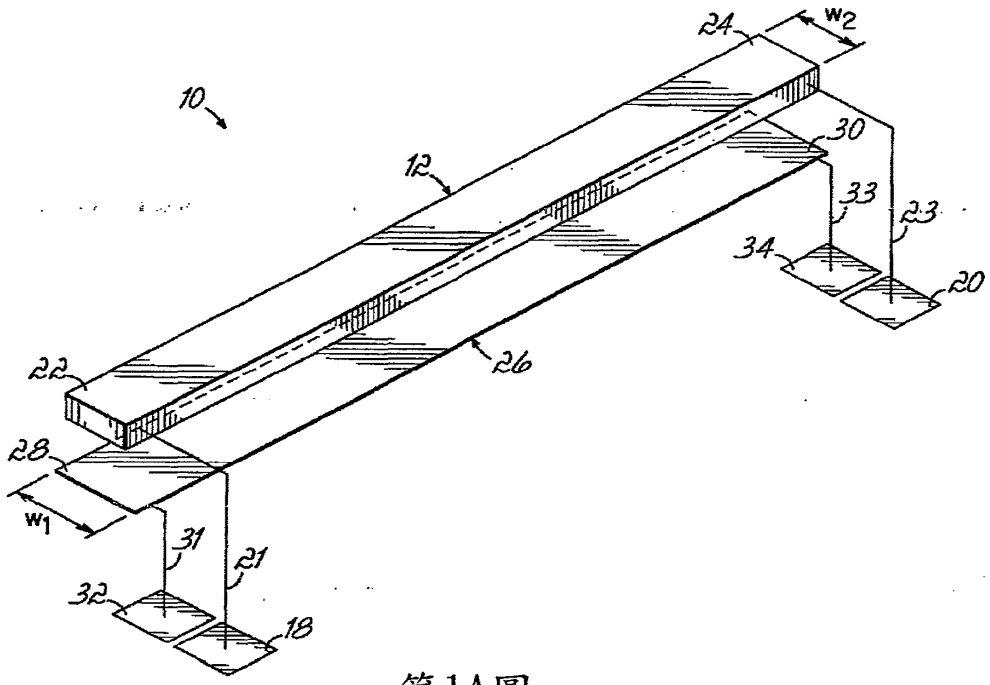
25. 如申請專利範圍第 22 項所述之設計結構，其中該電路另包含：

一電容屏，放置在該接地線與該信號線之間。

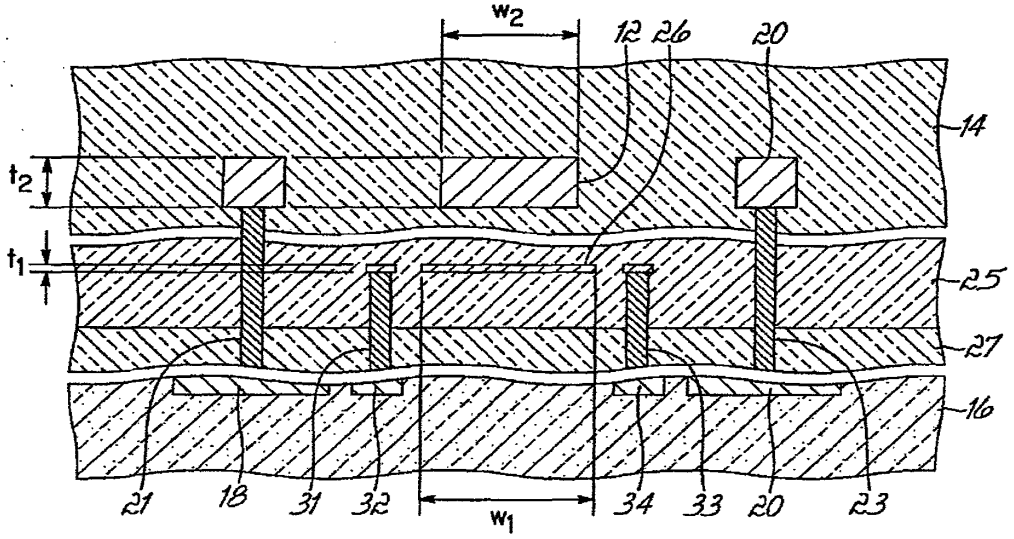
26. 如申請專利範圍第 22 項所述之設計結構，其中該至少一控制單元係經組態以運作在一控制電壓信號之接收，以選擇性地斷接與接通該電流路徑。

27. 如申請專利範圍第 22 項所述之設計結構，其中該至少一控制單元係選擇自場效電晶體、正－本－負二極體、以及在此之組合所組成之群組。

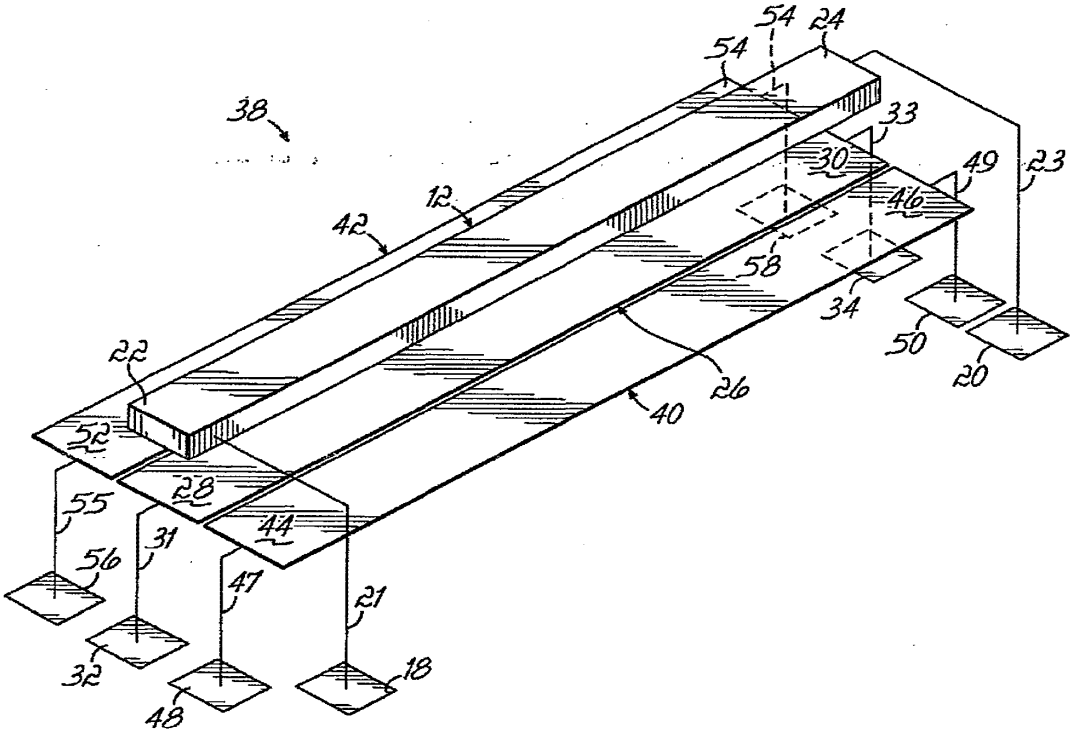
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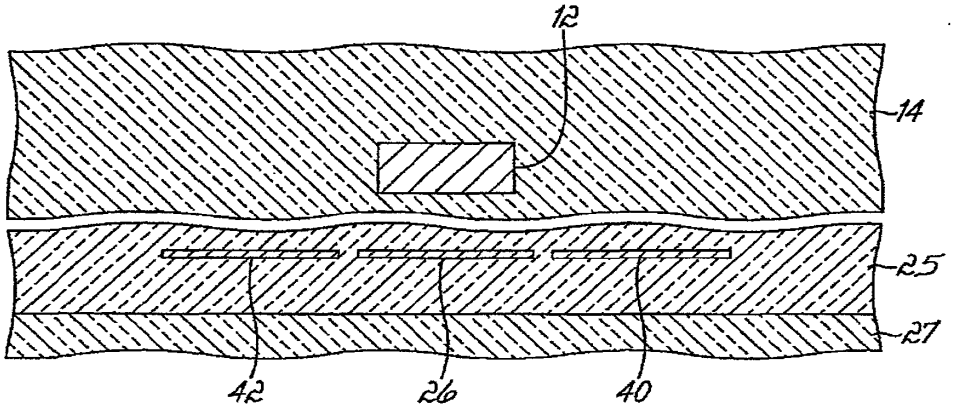
第1A圖


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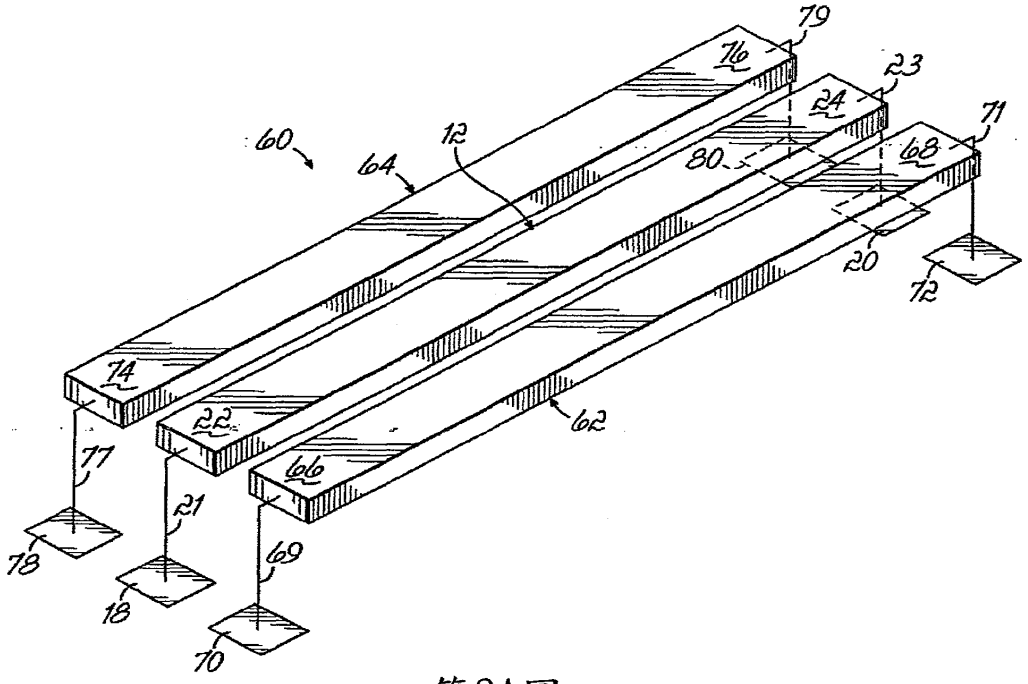
第1B圖


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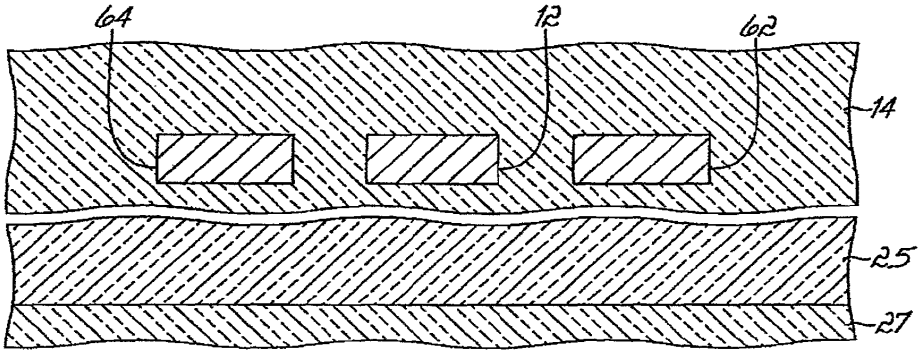
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第2B圖

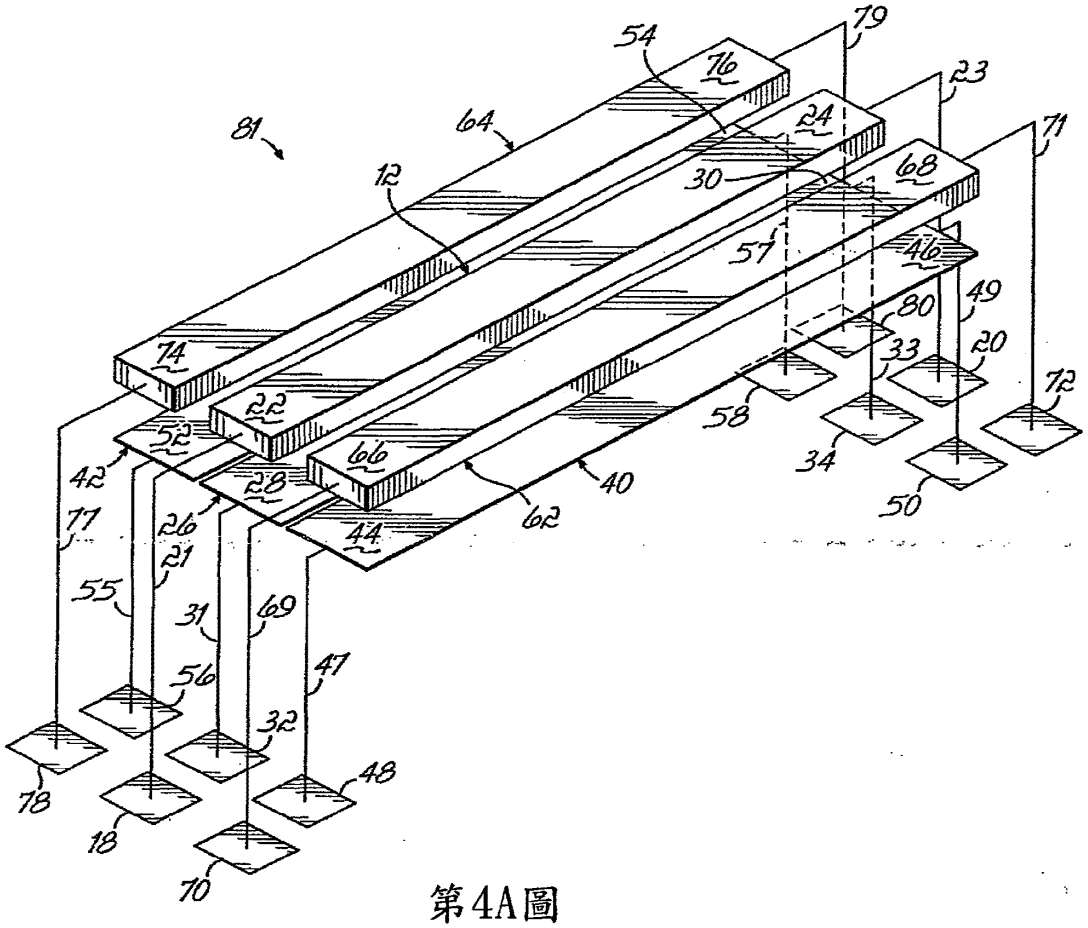


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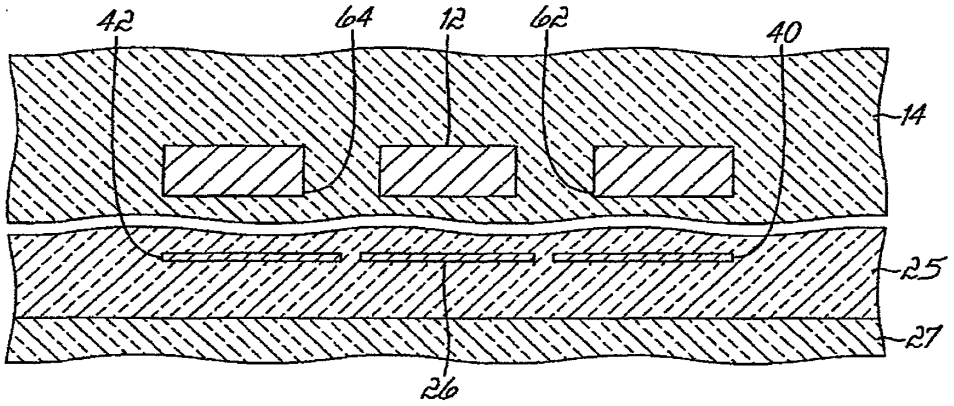


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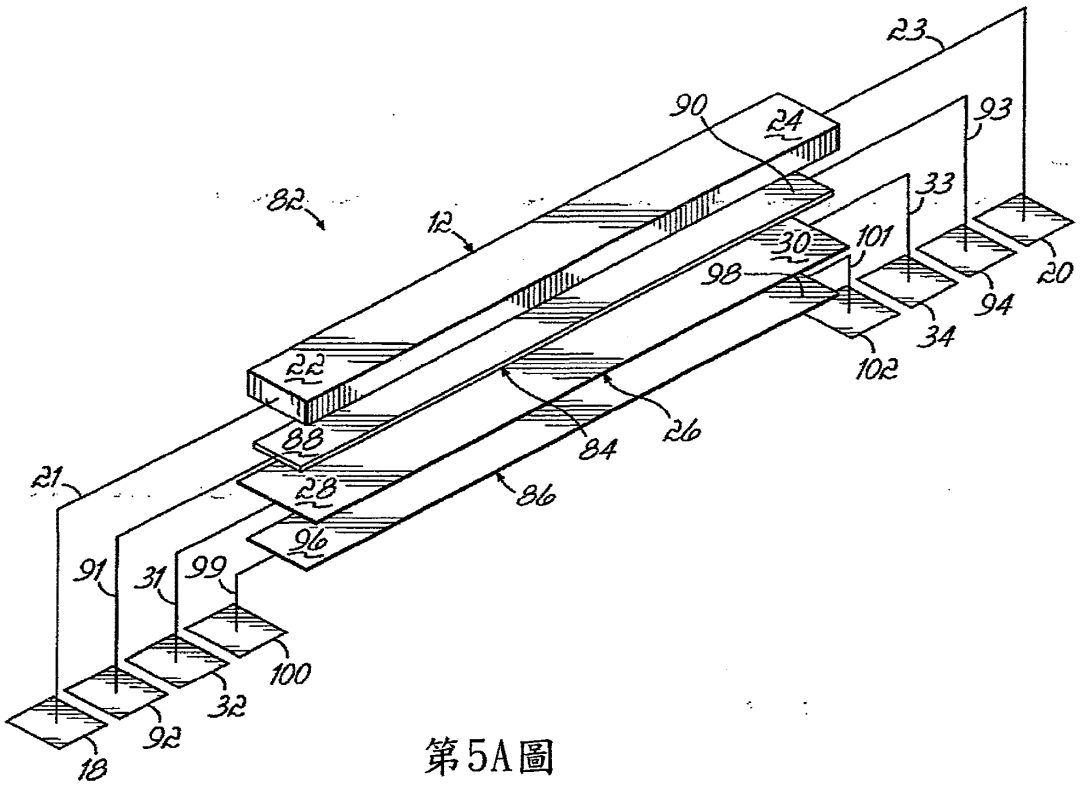
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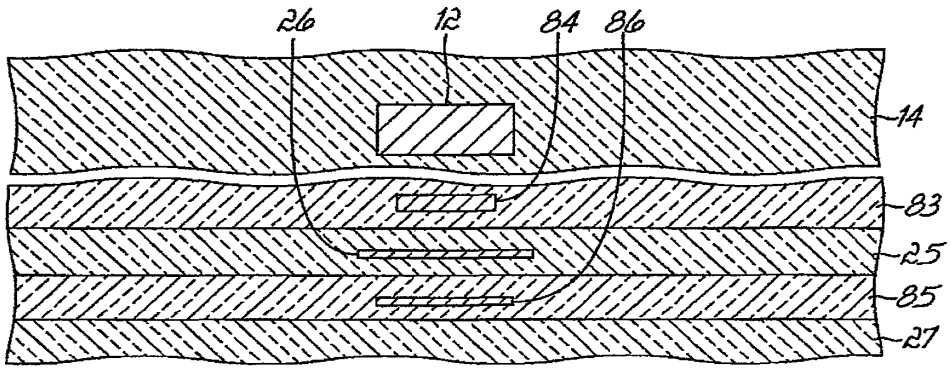
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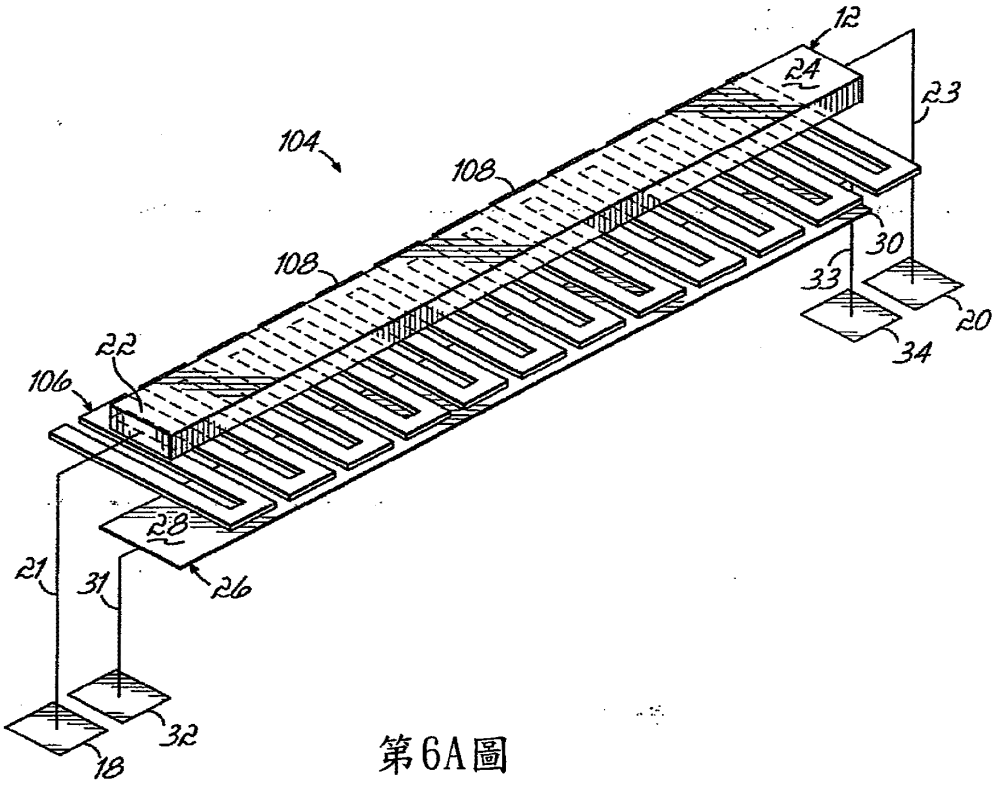
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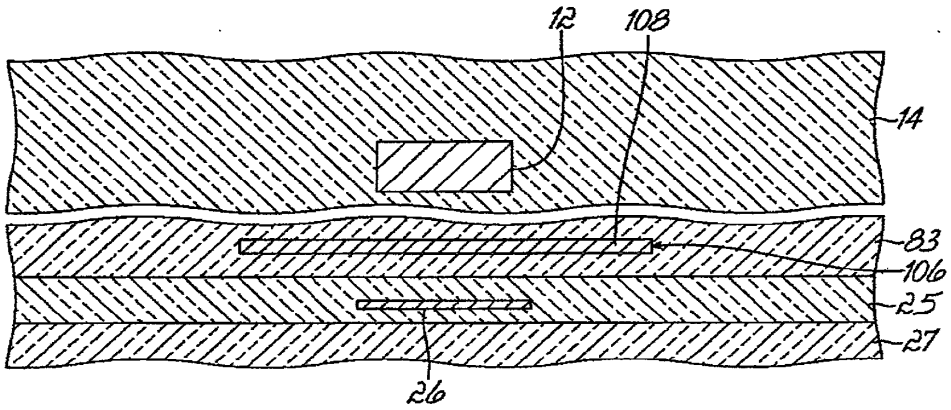
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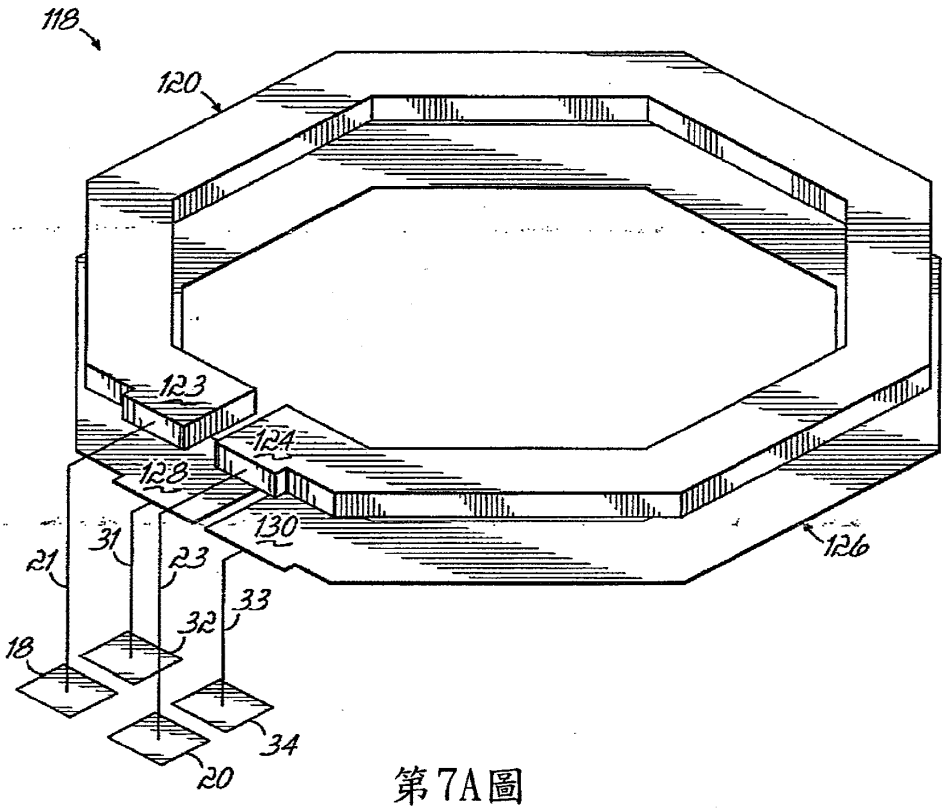
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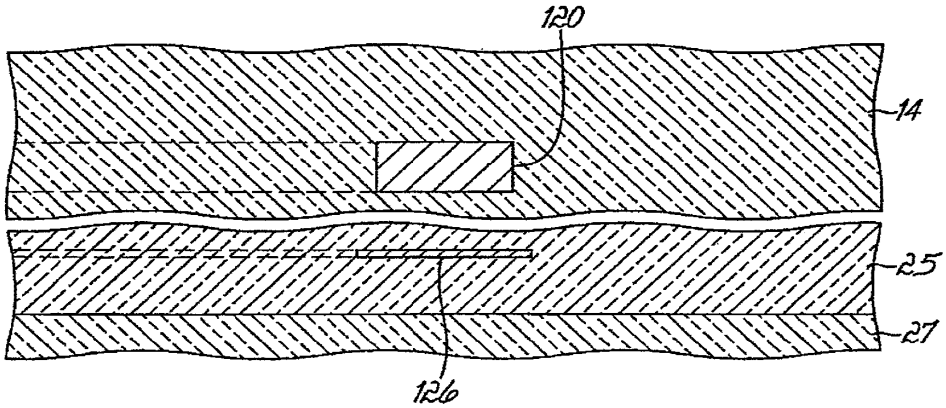
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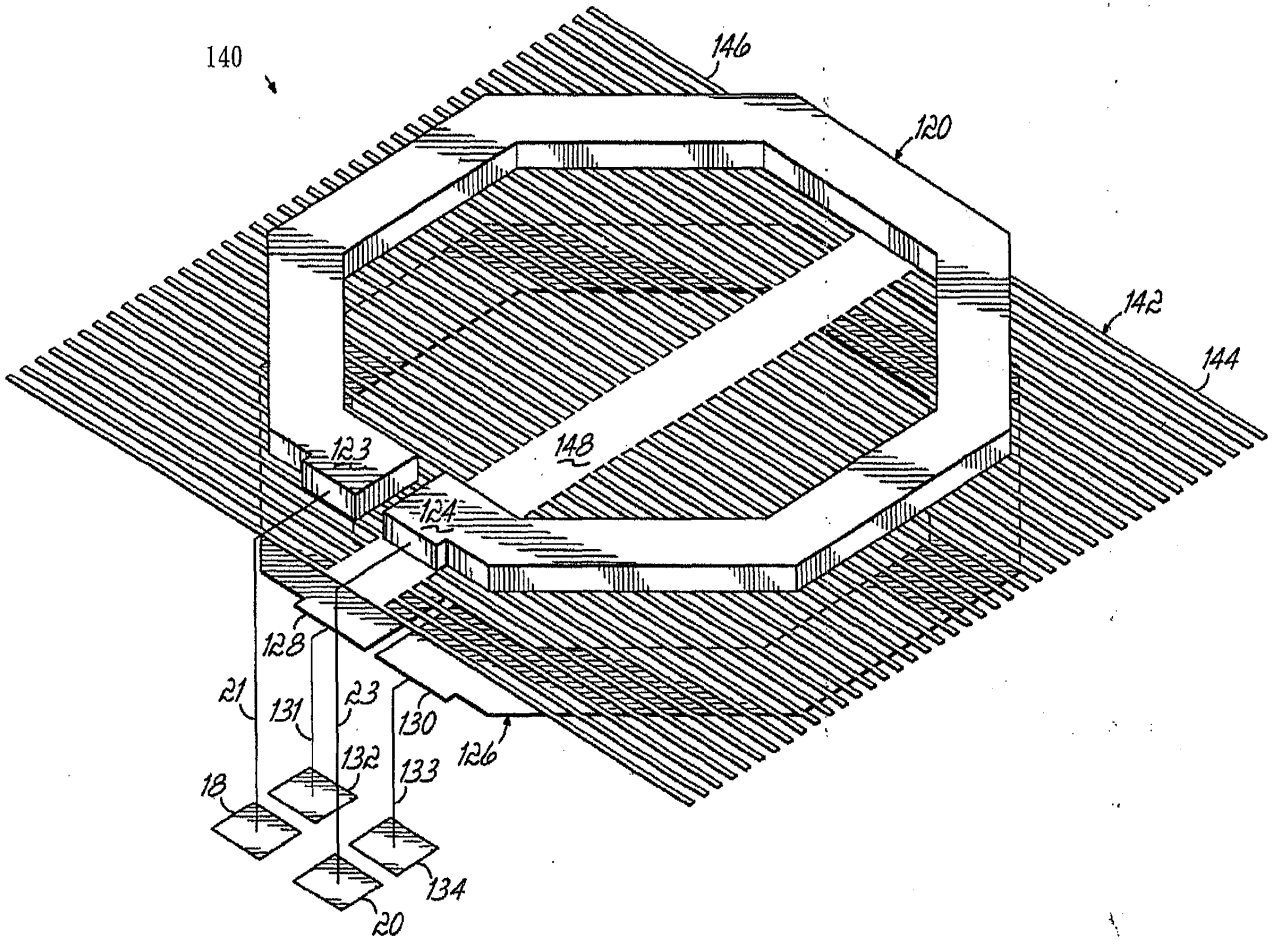
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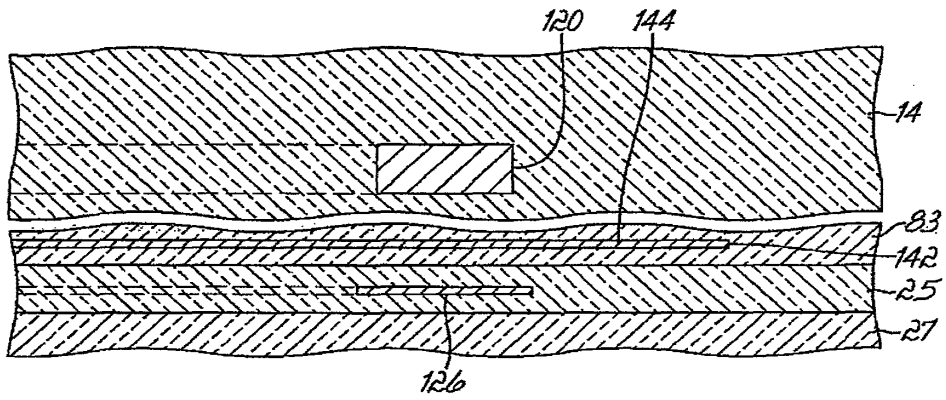
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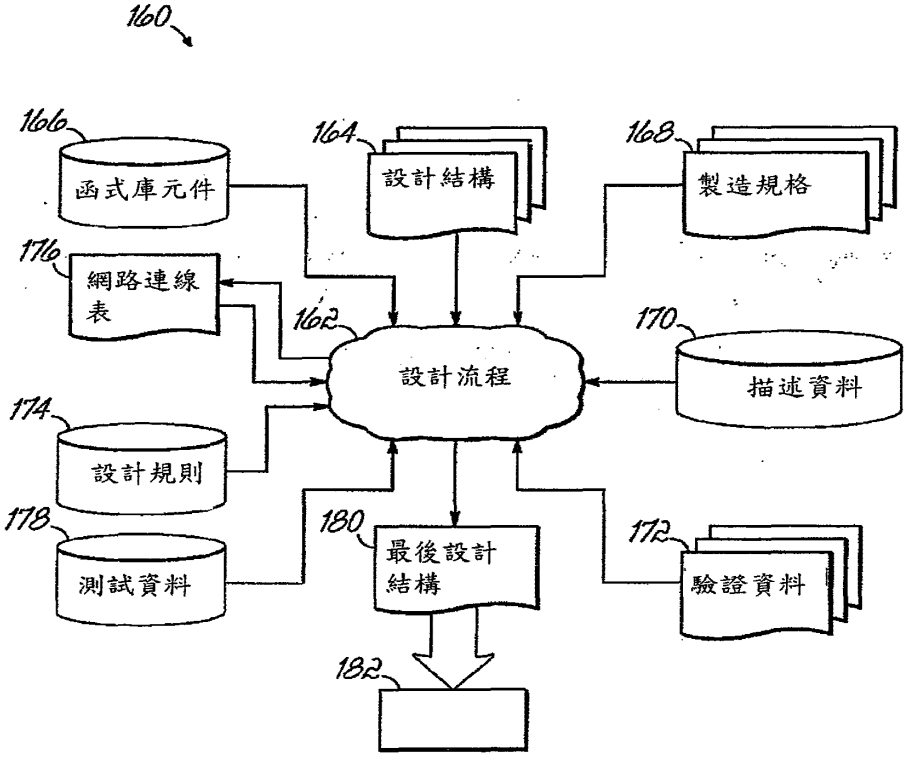
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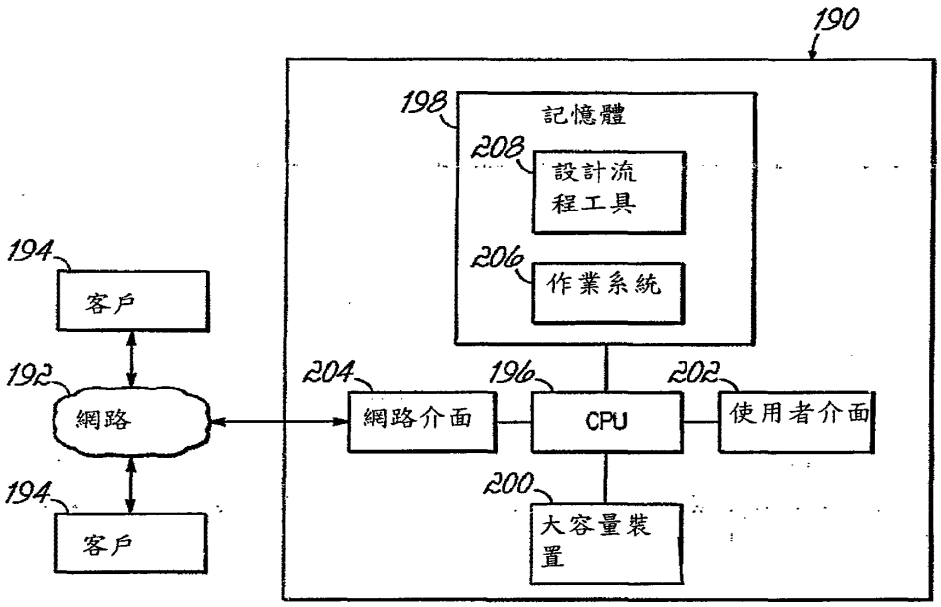
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四、指定代表圖：

(一)本案指定代表圖為：第（ 9 ）圖。

(二)本代表圖之元件符號簡單說明:

160	設計流
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170	描述資料
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五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

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Individual	F
Abstract	A planar ultra-capacitor including a substrate, a carbon nanotube (CNT) thin film and a transition metal oxide layer is provided. The CNT thin film with an interdigitated pattern is deposited on the substrate. The transition metal oxide layer with the same interdigitated pattern is deposited on the CNT thin film. The planar ultra-capacitor of the present invention is capable of incorporating to the micro-electromechanical (MEMS) system more easily than the conventional ultra-capacitor having parallel electrodes, so that the application thereof is not limited.

Information on this system is for reference only, it cannot be used as grounds for approval or rejection.
In all instances of discrepancy, official publication from TIPO shall prevail and should be consulted.

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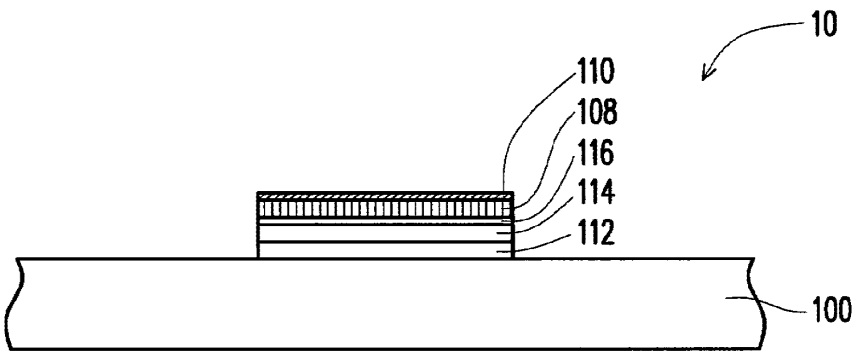
(54)名稱

平面超高電容器

PLANAR ULTRACAPACITOR

(57)摘要

一種平面超高電容器，包括基材、奈米碳管薄膜及過渡金屬之氧化物層。奈米碳管薄膜具有指叉圖案並沉積於基材上。過渡金屬之氧化物層具有相同指叉圖案並沉積於奈米碳管薄膜上。本發明之平面超高電容器較習知之具有平行電極之超高電容器更易於納入微機電系統中，其應用範圍不受限制。



10：平面超高電容器
100：基材
108：奈米碳管薄膜
110：過渡金屬之氧化物層
112：圖案化緩衝層
114：圖案化集電層
116：圖案化觸媒層

六、發明說明：

【發明所屬之技術領域】

本發明是與一種超高電容器有關，且特別是與一種微型平面超高電容器有關。

【先前技術】

在二十一世紀，人們對於電能的需求日益殷切，因此對於電化學儲能裝置的需求也隨之增加，其中電池（battery）及電化學電容（electrochemical capacitor）均是主要的電化學儲能裝置。

二次電池已存在於各式各樣的消費性電子產品、電動工具、電動車、國防軍事裝置中，以提供攜帶型的電力。但在電能驅動上，常遇見需要瞬時高功率輸出（pulse power output）場合，二次電池儘管擁有高能量密度，且所攜帶的能量容量廣為使用者接受，但因為它們需要進行電化學反應以獲得功率，受限於反應過程時的反應速率以及電極的反應活性位置有限，使得電池難以達到電路系統所要求的快速充/放電。此外，由於先天性的電活化表面腐蝕問題，也讓二次電池不合適做高速充/放電。

另一方面，電容器則相對適合於進行瞬時高功率輸出，因為電容器電極並未參與實質的電化學反應。其中，超高電容器 （supercapacitor；ultracapacitor）的儲存容量係高於一般電容器，同時於工作期間，電雙層電容（double layer capacitance）的界面吸/脫附，遠較電化學反應的應答

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快，因而適合於搭配電池的高儲存能量，以提供瞬時高功率，是一種具備反覆快速充/放電、瞬間高輸出功率能力的儲能元件，因此引起各界極大的研究興趣。

然而，一般超高電容器均設計係為平行電極結構。隨著元件之微小化的趨勢，此種平行電極結構之超高電容器與微機電系統（micro-electromechanical system；MEMS）的相容性不佳，導致其應用範圍受限制。

【發明內容】

有鑑於此，本發明提供一種具有指叉電極之平面超高電容器，其之製程簡單且易於納入微機電系統中，應用範圍不受限制。

本發明提供一種平面超高電容器，其包括基材、奈米碳管（carbon nanotubes；CNT）薄膜及過渡金屬之氧化物層。奈米碳管薄膜具有指叉圖案並係沉積於基材上。過渡金屬之氧化物層具有相同之指叉圖案並係沉積於奈米碳管薄膜上。

在本發明之一實施例中，上述過渡金屬之氧化物層的材料包括氧化錳、氧化錳鉬、氧化鎳鈷、氧化鎳、氧化鈷、氧化鉛或其等組合。

在本發明之一實施例中，上述過渡金屬之氧化物層僅係被電鍍於陽極上。

在本發明之一實施例中，上述過渡金屬之氧化物層係同時電鍍於陽極及陰極上。

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在本發明之一實施例中，上述奈米碳管薄膜包括多數個奈米碳管，且這些奈米碳管係實質上以垂直於基材的方式來排列。

在本發明之一實施例中，上述過渡金屬之氧化物層更沉積於這些奈米碳管的一部分或是全部側表面上。

在本發明之一實施例中，上述過渡金屬之氧化物層之單位面積的重量為奈米碳管薄膜之單位面積的重量的千分之一倍至十倍之間。

在本發明之一實施例中，上述平面超高電容器更包括具有指叉圖案之圖案化觸媒層，沉積於基材與奈米碳管薄膜之間。

在本發明之一實施例中，上述平面超高電容器更包括具有指叉圖案之圖案化集電層（current collector layer），其係沉積於基材與圖案化觸媒層之間。

在本發明之一實施例中，上述平面超高電容器更包括具有指叉圖案之圖案化緩衝層，沉積於基材與圖案化集電層之間。

基於上述，本發明之單晶片平面超高電容器所使用的材料包括具電雙層電容的奈米碳管薄膜，以及具擬電容（pseudocapacitance）的過渡金屬之氧化物（例如氧化錳）。具擬電容的過渡金屬之氧化物（例如氧化錳）價格低廉且耐腐蝕，將其應用於電容材料中具有降低成本及提高電容量之效果。此外，相較於一般電容的平行電極幾何形態，本發明之超高電容器的平面設計更易於納入微機電

系統中，應用範圍更廣，極具競爭優勢。

為讓本發明之上述特徵和優點能更明顯易懂，下文特舉實施例，並配合所附圖式作詳細說明如下。

【實施方式】

圖 1 為根據本發明一實施例所繪示之平面超高電容器的上視圖。圖 2 為圖 1 中沿 I-I'線的剖面示意圖。

請參照圖 1 及圖 2，本發明的平面超高電容器 10 包括基材 100、各別具有指叉圖案之奈米碳管薄膜 108 及過渡金屬之氧化物層 110。

基材 100 的材料包括矽。舉例來說，基材 100 可以例如是二氧化矽/矽晶片或 Eagle 2000 玻璃(或其它無鹼矽氧玻璃)基材。奈米碳管薄膜 108 係被沉積於基材 100 上。在一實施例中，奈米碳管薄膜 108 包括多數個奈米碳管，這些奈米碳管的高度約為 30~50 μm，且這些奈米碳管係實質上垂直於基材 100 排列。過渡金屬之氧化物層 110 係沉積於奈米碳管薄膜 108 上。過渡金屬之氧化物層 110 的材料包括氧化錳、氧化錳鉬、氧化鎳鈷、氧化鎳、氧化鈷、氧化鉛或其組合。在一實施例中，過渡金屬之氧化物層 110 的材料例如是氧化錳微粒，且氧化錳會隨著垂直的奈米碳管而出現直行的水滴式結構，並具有尺寸相當均一的顆粒。此外，過渡金屬之氧化物層 110 之單位面積的重量(通常以 mg/cm^2 表示）係為奈米碳管薄膜 108 之單位面積的重量之千分之一倍至十倍之間。

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特別要注意的是，圖 1 為繪示過渡金屬之氧化物層 110，被設置於奈米碳管薄膜 108 中的奈米碳管之頂表面上的示意圖，但本發明並不侷限於此。在本領域中具有通常知識者應可了解，過渡金屬之氧化物層 110 更可以被沉積於奈米碳管薄膜 108 中之奈米碳管的一部分或是全部側表面上（未繪示）。

本發明的平面超高電容器 10 可以分為「非對稱型」及「對稱型」兩種。在一實施例中，過渡金屬之氧化物層 110 僅被電鍍於陽極上，以形成具有非對稱型指叉式電極的平面超高電容器。在另一實施例中，過渡金屬之氧化物層 110 係被同時電鍍於陽極及陰極上，以形成具有對稱型指叉式電極的平面超高電容器。

此外，本發明的平面超高電容器 10 可以更包括各具有指叉圖案之圖案化觸媒層 116、圖案化集電層 114 及圖案化緩衝層 112。

圖案化觸媒層 116 係被配置於基材 100 與奈米碳管薄膜 108 之間，以加速奈米碳管薄膜 108 的成長。因此，圖案化觸媒層 116 也可以稱為奈米碳管之成長觸媒層，且奈米碳管薄膜 108 中的奈米碳管，係實質上垂直於圖案化觸媒層 116 而成長。圖案化觸媒層 116 的材料包括鋁及鐵（Al/Fe）。

圖案化集電層 114 係沉積於基材 100 與圖案化觸媒層 116 之間，以降低電極的內部阻抗。圖案化緩衝層 112 則係沉積於基材 100 與圖案化集電層 114 之間，以增加圖案

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化集電層 114 與基材 100 之間的附著性。在一實施例中，圖案化集電層 114 可以例如是金（Au）薄膜，而圖案化緩衝層 112 則可以例如是鈦（Ti）薄膜。

特別要注意的是，也可以省略形成圖案化緩衝層 112 及圖案化集電層 114 的步驟，而如圖 3 所示將圖案化觸媒層 116 直接沉積於基材 100 上。

基於上述說明，本發明之單晶片平面超高電容器所使用的材料，包括具電雙層電容的奈米碳管薄膜，以及具擬電容的過渡金屬之氧化物（例如氧化錳）。本發明藉著將此兩種材料結合運用，以發展出具有高電容值的超高電容器。此外，相較於一般電容的平行電極幾何形態，本發明之超高電容器的平面設計，使其更易於納入微機電系統中，進而使其之應用範圍更不受限制。

以下，將說明本發明之平面超高電容器的製作方法。圖 4A 至圖 4D 係為根據本發明一實施例所繪示之平面超高電容器之製作方法的剖面示意圖。

請參照圖 4A，於基材 100 上形成圖案化光阻層 101。基材 100 可以例如是二氧化矽/矽(100)晶片。形成圖案化光阻層 101 的方法，包括在基材 100 上塗佈光阻材料層（未繪示），然後對光阻材料層進行微影製程以形成圖案化光阻層 101。光阻材料層的材料可以為負型光阻劑或正型光阻劑。

接著，請參照圖 4B，於基材 100 上依序形成緩衝層 102 與集電層 104，以覆蓋圖案化光阻層 101。形成緩衝層

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102 與集電層 104 的方法包括有濺鍍法。緩衝層 102 可以例如是鈦薄膜。集電層 104 可以例如是金薄膜。之後，於集電層 104 上形成觸媒層 106。形成屬觸媒層 106 的方法包括蒸鍍法。觸媒層 106 可以例如是鐵/鋁觸媒層。

接著，請參照圖 4C，其利用剝膜劑來移除圖案化光阻層 101。剝膜劑可以例如是丙酮溶劑。於移除圖案化光阻層 101 的步驟中，也可以同時移除位於圖案化光阻層 101 上的緩衝層 102、集電層 104 及觸媒層 106，以形成各別具有指叉圖案之圖案化緩衝層 112、圖案化集電層 114 及圖案化觸媒層 116。

然後，請參照圖 4D，於圖案化觸媒層 116a 上形成奈米碳管薄膜 108。奈米碳管薄膜 108 包括多數個奈米碳管，而這些奈米碳管係排列成實質上垂直於圖案化觸媒層 116。本發明之奈米碳管薄膜 108 係由水平式長管爐來加以製備，其中反應氣體包括 C_2H_2，溫度約 750℃，壓力約 4 torr，時間約 2 分鐘。

接著，請繼續參照圖 4D，其係於奈米碳管薄膜 108 上形成過渡金屬之氧化物層 110。形成過渡金屬之氧化物層 110 的方法可以包括電鍍法。依製程需要，其可以僅將過渡金屬之氧化物層 110 電鍍於陽極上，或同時電鍍於陽極及陰極上，以形成「非對稱型」及/或「對稱型」之平面超高電容器。至此，便完成本發明之平面超高電容器 10 的製作。

在一實施例中，過渡金屬之氧化物層 110 例如是氧化

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錳層。形成氧化錳層的方法如下。首先，配製 0.2 M $MnSO_4 \cdot 5H_2O$ 電鍍液，並以 0.5 M H_2SO_4 與 0.1 M Na_2SO_4 來將 pH 值調整至約為 7.0。之後，將試片浸置於電鍍液中，在工作電極（陽極）下進行電鍍，先以固定電位在 1.2 V 下進行沉積 10 秒，再以定電流法（電流密度為 5mA cm^{-2}）做脈衝式電鍍 10 分鐘，過程中並配合循環式恆溫水槽，將電鍍溫度控制於 25 ℃。然後，將試片放置空氣下乾燥，再於空氣中以 50 ℃加熱 12 小時。

特別要說明的是，於形成奈米碳管薄膜 108 之後以及形成過渡金屬之氧化物層 110 之前，可以如圖 5A 至圖 5C 所示之進行試片的封裝。首先，請參照圖 5A，用銀膠 202 將銅線 200 黏著於元件的陰極、陽極上，再放入烘箱固定 20 分鐘。之後，請參照圖 5B，利用陶瓷膠 204 覆蓋住銀膠 202，使其穩固不會脫落，並放入烘箱內固定 30 分鐘。最後，請參照圖 5C，用絕緣黏膠（例如 Microstop）206 覆蓋住陶瓷膠 204，並包住所有浸於電解液之銅線 200 的導電表面。

在上述實施例之圖 4B 的步驟中，也可以省略形成緩衝層 102、集電層 104 的步驟，而將觸媒層 106 直接形成於基材 100 上並覆蓋圖案化光阻層 101。然後，繼續圖 4C 及 4D 的步驟，以完成本發明之平面超高電容器 10a（如圖 3）的製作。

接下來，將根據上述製造方法來製作多個平面超高電容器以驗證本發明的功效。

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實例 1

於二氧化矽/矽(100)晶片上依序形成各別具有指叉圖案之鐵/鋁觸媒層、CNT 薄膜及氧化錳層。在實例 1 之樣品中，氧化錳層僅被電鍍於陽極上，以形成無金之非對稱型平面超高電容器。

實例 2

於二氧化矽/矽(100)晶片上依序形成各別具有指叉圖案之鐵/鋁觸媒層、CNT 薄膜及氧化錳層。在實例 2 之樣品中，氧化錳層係被同時電鍍於陽極及陰極上，以形成無金之對稱型平面超高電容器。

實例 3

於二氧化矽/矽(100)晶片上依序形成各別具有指叉圖案之鈦薄膜（作為緩衝層）、金薄膜（作為集電層）、鐵/鋁觸媒層、CNT 薄膜及氧化錳層。在實例 3 之樣品中，氧化錳層僅被電鍍於陽極上，以形成有金之非對稱型平面超高電容器。

實例 4

於二氧化矽/矽(100)晶片上依序形成各別具有指叉圖案之鈦薄膜（作為緩衝層）、金薄膜（作為集電層）、鐵/鋁觸媒層、CNT 薄膜及氧化錳層。在實例 4 之樣品中，氧化錳層係被同時電鍍於陽極及陰極上，以形成有金之對稱型平面超高電容器。

實例 1~4 之平面超高電容器於 10、50、200、500 mV/s 掃描速率（sweep rate）下所計算出的比電容值係如表 1 所

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示。

表 1

	CNT (mg/cm^2)	MnO_2 (mg/cm^2)	比電容	掃描速率			
				10 mV/s	50 mV/s	200 mV/s	500 mV/s
實例 1（無金/非對稱型）	1.23	0.93	C (mF/cm^2)	365	159	52.1	21.9
			C ($F/g_{MnO2+CNT}$)	169	73.5	24.1	10.1
實例 2（無金/對稱型）	1.23	0.93	C (mF/cm^2)	148	63.3	22.2	13.0
			C ($F/g_{MnO2+CNT}$)	120	51.3	18.0	10.6
實例 3（有金/非對稱型）	0.31	0.93	C (mF/cm^2)	217	117	76.4	49.8
			C ($F/g_{MnO2+CNT}$)	209	113	73.8	48.1
實例 4（有金/對稱型）	0.31	0.93	C (mF/cm^2)	50.6	25.7	16.3	11.0
			C ($F/g_{MnO2+CNT}$)	41.1	20.8	13.2	8.9

請參照表 1，本發明之平面超高電容器於 10 mV/s 及 50 mV/s 的掃描速率下均可達到高電容值之功效，尤其無金之非對稱型平面超高電容器（實例 1），於 10 mV/s 掃描速率下的比電容值更可高達 365 mF/cm^2（169 F/g）。

如表 1 所示，非對稱型之平面超高電容器（實例 1、3）的比電容值，較對稱型之平面超高電容器（實例 2、4）的比電容值來得更高。詳而言之，無金之非對稱型平面超高電容器（實例 1）的比電容值（365 mF/cm^2；169 F/g），係較無金之對稱型平面超高電容器（實例 2）的比電容值（148 mF/cm^2；120 F/g）高出許多。此外，有金之非對稱型平面超高電容器（實例 3）的比電容值（217 mF/cm^2；209 F/g），

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亦較無金之對稱型平面超高電容器（實例 4）的比電容值（50.5 mF/cm^2；41.1 F/g）高出許多。推估這是因為非對稱性電極其內部阻抗較小，並能使用高比表面積之奈米碳管直接做相對電極，故能更有效地使用電容材料以提升其電容值。

圖 6~9 繪示實例 1~4 之平面超高電容器於不同定電流下的充/放電曲線圖。表 2 顯示實例 1~4 之平面超高電容器於不同放電電流下的比電容值。

表 2

	比電容	放電電流(μA)									
		10	20	30	40	50	60	70	80	90	100
實例 1（無金/非對稱型）	C (mF/cm^2)	-	-	357	341	343	293	287	272	257	237
	C ($F/g_{MnO2+CNT}$)	-	-	165	158	159	136	133	126	119	110
實例 2（無金/對稱型）	C (mF/cm^2)	105	77.9	69.8	39.2	22.7	10.3	-	-	-	-
	C ($F/g_{MnO2+CNT}$)	48.5	36.1	32.3	18.1	10.5	4.8	-	-	-	-
實例 3（有金/非對稱型）	C (mF/cm^2)	-	-	-	288	244	220	169	144	124	110
	C ($F/g_{MnO2+CNT}$)	-	-	-	233	197	162	137	116	100	88.8
實例 4（有金/對稱型）	C (mF/cm^2)	65.2	39.2	30.2	24.8	21.6	19.5	17.8	16.7	15.7	14.8
	C ($F/g_{MnO2+CNT}$)	52.8	31.8	24.4	20.1	17.5	15.8	14.4	13.5	12.7	12

由圖 6~9 中可看出，在電性表現上只有無金疊層之樣品（實例 1、2）會有氧化錳材料的阻抗影響，其於放電過程中會出現電壓降（IR drop）的情形，且隨著放電電流的提升其壓降範圍也會加大。反之，此種現象在有金疊層之樣品（實例 3、4）皆被改善了。

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此外，如表2顯示，可以發現隨著放電電流的提升，無金疊層之樣品（實例1、2）的電容值之衰退程度較大。反之，有金疊層之樣品（實例3、4）卻具有較小之電容值衰退。由此可知，在充/放電過程中內部阻抗所導致的電容損失，可以藉由導入作為集電層之金薄膜而降低。

綜上所述，本發明之平面超高電容器所使用的材料，包括具電雙層電容的奈米碳管薄膜，以及具擬電容的過渡金屬之氧化物（例如氧化錳）。奈米碳管的高表面積、低質量密度、優良的抗腐蝕及化學穩定性、高電子傳導能力等等特性，使其適合用於集積化元件。而氧化錳微粒的高擬電容值，價格低廉與耐腐蝕性，使其在應用於電容材料中可以具有低成本及高電容量之效果。本發明將此兩種材料結合運用，以發展出具有高電容值的超高電容器。此外，相較於一般電容的平行電極幾何形態，本發明之超高電容器的平面設計，使其更易於納入微機電系統中，其之應用範圍廣，極具競爭優勢。

另外，已知技術常使用具擬電容的二氧化釕（RuO_2）作為電極，其之結晶顆粒極小，且本身的電阻值相當低，具有良好導電性。然而儘管釕氧化物具有很高的電容值及幾近理想的循環充放電穩定性，但在商業上，因為地球釕礦藏量稀少，不容易取得，進而使得材料成本太過昂貴，實用性受到限制。相較之下，本發明使用市購容易取得且單價低的材料（例如氧化錳）來取代二氧化釕，因而使得本發明之平面超高電容器在成本及實用性上更具優勢。

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雖然本發明已以實施例揭露如上，然其並非用以限定本發明，任何所屬技術領域中具有通常知識者，在不脫離本發明之精神和範圍內，當可作些許之更動與潤飾，故本發明之保護範圍當視後附之申請專利範圍所界定者為準。

【圖式簡單說明】

圖 1 為根據本發明一實施例所繪示之平面超高電容器的上視圖。

圖 2 為圖 1 中沿 I-I'線的剖面示意圖。

圖 3 為根據本發明一實施例所繪示之平面超高電容器的局部剖面示意圖。

圖 4A 至圖 4D 根據本發明一實施例所繪示之平面超高電容器之製作方法的剖面示意圖。

圖 5A 至圖 5C 繪示本發明之平面超高電容器之試片封裝的上視圖。

圖 6~9 繪示實例 1~4 之平面超高電容器於不同定電流下的充/放電曲線圖。

【主要元件符號說明】

10、10a：平面超高電容器

100：基材

101：圖案化光阻層

102：緩衝層

104：集電層

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106：觸媒層
108：奈米碳管薄膜
110：過渡金屬之氧化物層
112：圖案化緩衝層
114：圖案化集電層
116：圖案化觸媒層
200：銅線
202：銀膠
204：陶瓷膠
206：絕緣黏膠

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發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※ 申請案號：100101999

※ 申請日：　　※IPC 分類：H01G 4/33 (2006.01) H01G 4/005 (2006.01)

一、發明名稱：

平面超高電容器 / PLANAR ULTRACAPACITOR

二、中文發明摘要：

一種平面超高電容器，包括基材、奈米碳管薄膜及過渡金屬之氧化物層。奈米碳管薄膜具有指叉圖案並沉積於基材上。過渡金屬之氧化物層具有相同指叉圖案並沉積於奈米碳管薄膜上。本發明之平面超高電容器較習知之具有平行電極之超高電容器更易於納入微機電系統中，其應用範圍不受限制。

三、英文發明摘要：

A planar ultra-capacitor including a substrate, a carbon nanotube (CNT) thin film and a transition metal oxide layer is provided. The CNT thin film with an interdigitated pattern is deposited on the substrate. The transition metal oxide layer with the same interdigitated pattern is deposited on the CNT thin film. The planar ultra-capacitor of the present invention is capable of incorporating to the micro-electromechanical (MEMS) system more easily than

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the conventional ultra-capacitor having parallel electrodes, so that the application thereof is not limited.

四、指定代表圖：

（一）本案之指定代表圖：圖 2

（二）本代表圖之元件符號簡單說明：

10：平面超高電容器

100：基材

108：奈米碳管薄膜

110：過渡金屬之氧化物層

112：圖案化緩衝層

114：圖案化集電層

116：圖案化觸媒層

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

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七、申請專利範圍：

1. 一種平面超高電容器，包括：

具有一指叉圖案之一奈米碳管薄膜，沉積於一基材上；以及

具有該指叉圖案之一過渡金屬之氧化物層，沉積於該奈米碳管薄膜上。

2. 如申請專利範圍第 1 項所述之平面超高電容器，其中該過渡金屬之氧化物層的材料包括氧化錳、氧化錳鉬、氧化鎳鈷、氧化鎳、氧化鈷、氧化鉛或其組合。

3. 如申請專利範圍第 1 項所述之平面超高電容器，其中該過渡金屬之氧化物層僅電鍍於陽極上。

4. 如申請專利範圍第 1 項所述之平面超高電容器，其中該過渡金屬之氧化物層同時電鍍於陽極及陰極上。

5. 如申請專利範圍第 1 項所述之平面超高電容器，其中該奈米碳管薄膜包括多數個奈米碳管，且該些奈米碳管實質上垂直於該基材排列。

6. 如申請專利範圍第 5 項所述之平面超高電容器，其中該過渡金屬之氧化物層更沉積於該些奈米碳管的一部分或是全部側表面上。

7. 如申請專利範圍第 1 項所述之平面超高電容器，其中該過渡金屬之氧化物層之單位面積的重量為該奈米碳管薄膜之單位面積的重量的千分之一倍至十倍之間。

8. 如申請專利範圍第 1 項所述之平面超高電容器，更包括具有該指叉圖案之一圖案化觸媒層，沉積於該基材與

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該奈米碳管薄膜之間。

9. 如申請專利範圍第 8 項所述之平面超高電容器，更包括具有該指叉圖案之一圖案化集電層，沉積於該基材與該圖案化觸媒層之間。

10. 如申請專利範圍第 9 項所述之平面超高電容器，更包括具有該指叉圖案之一圖案化緩衝層，沉積於該基材與該圖案化集電層之間。

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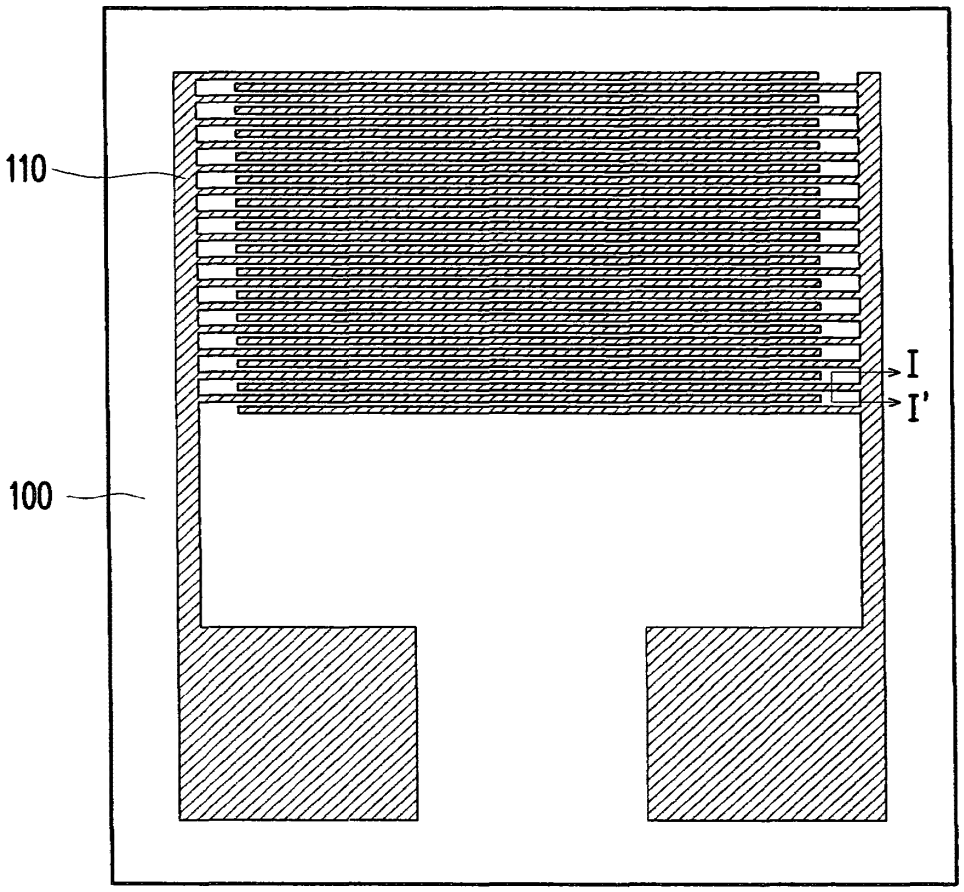


圖 1

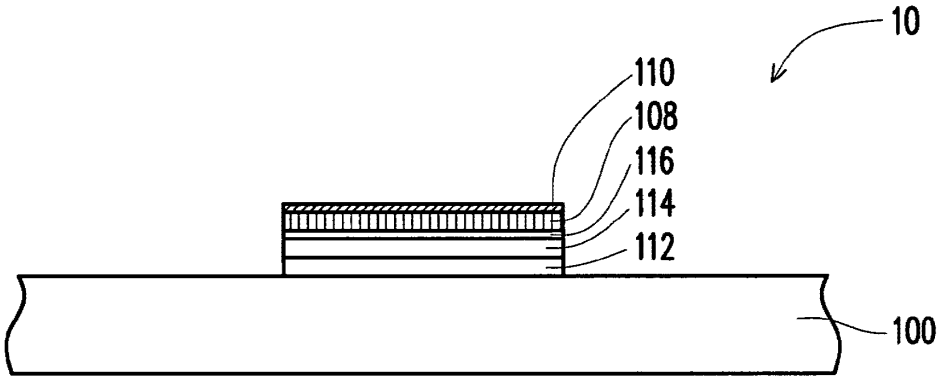


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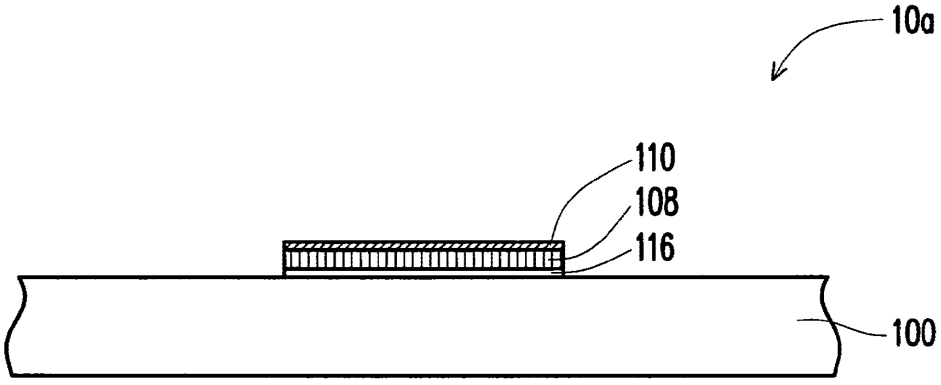


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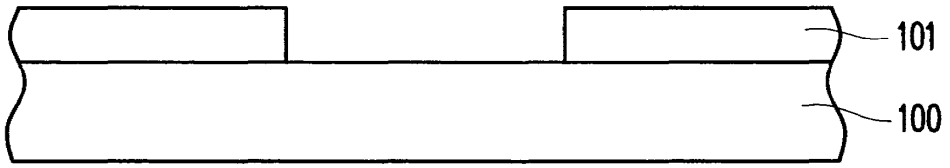


圖 4A

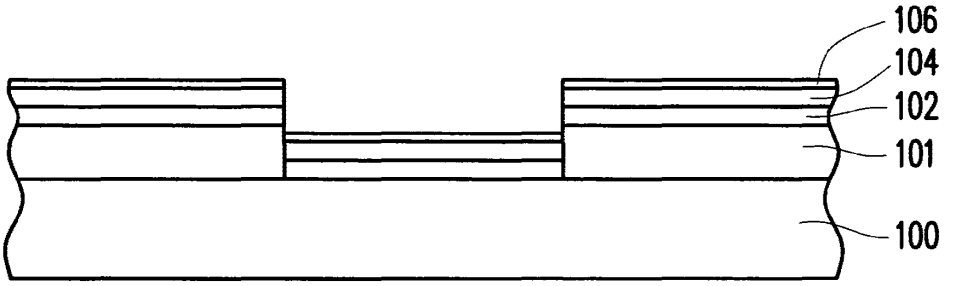


圖 4B

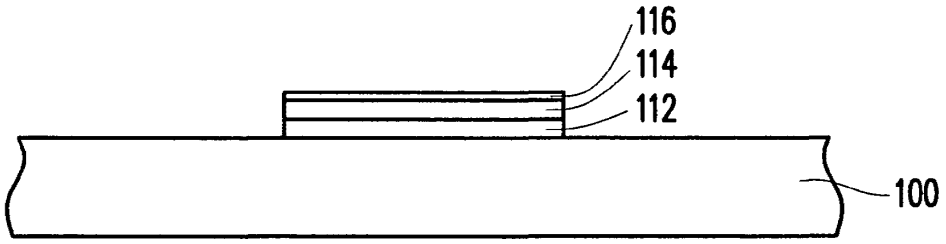


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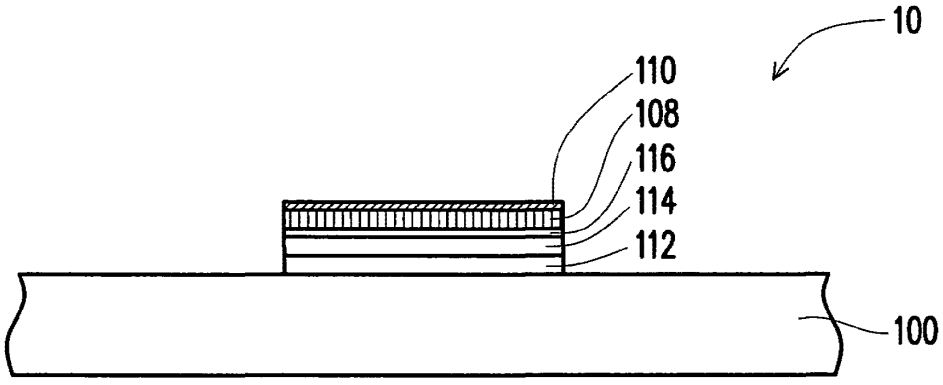


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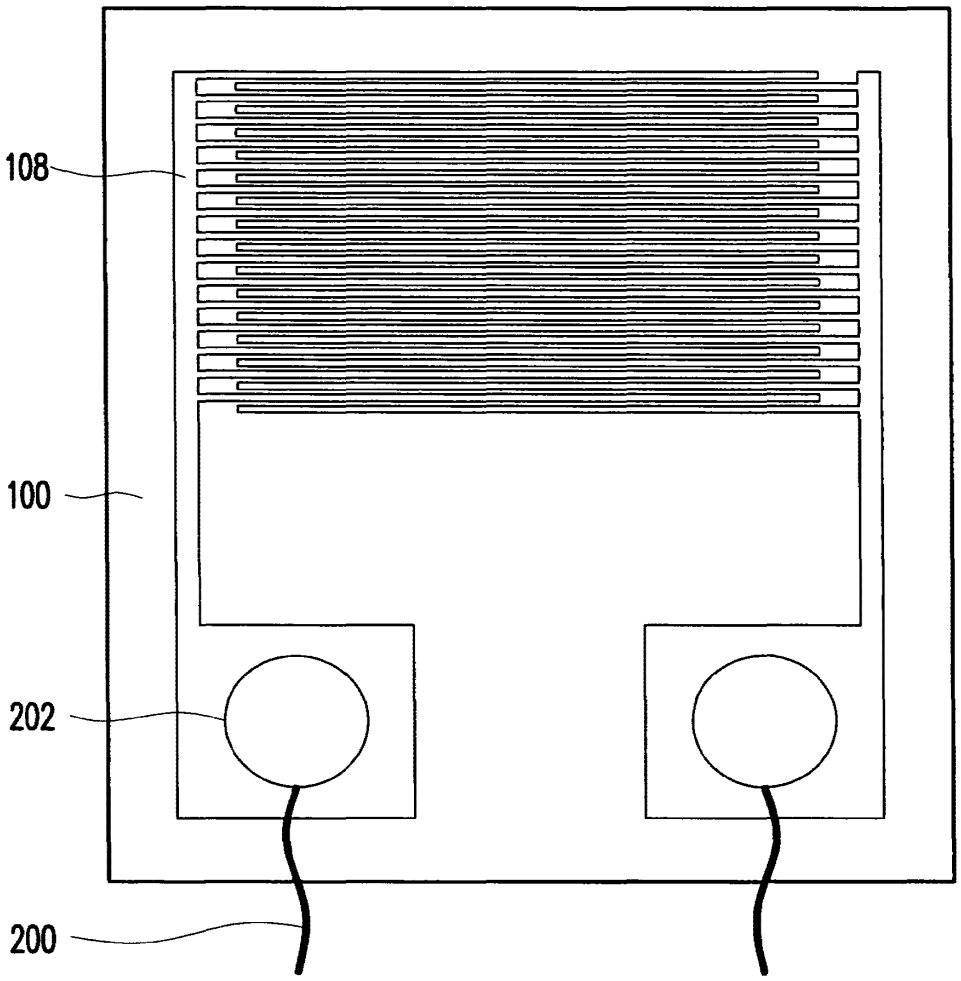


圖 5A

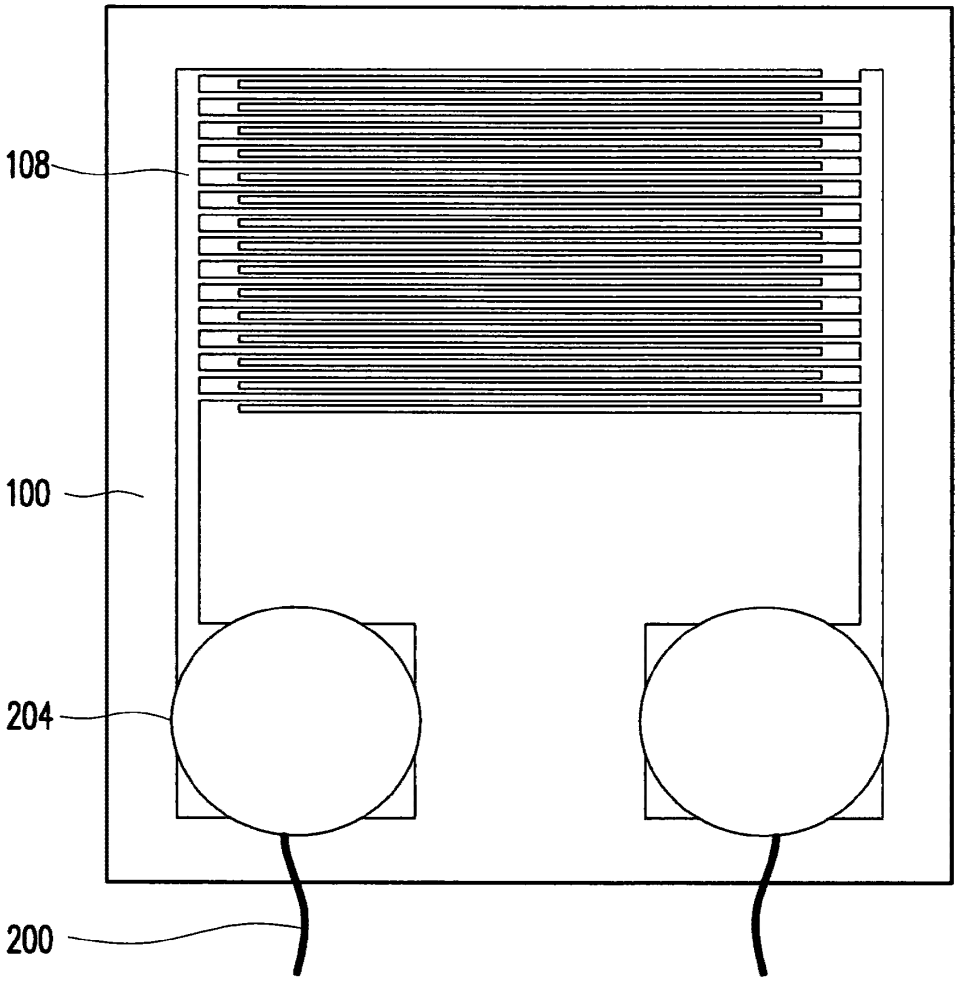


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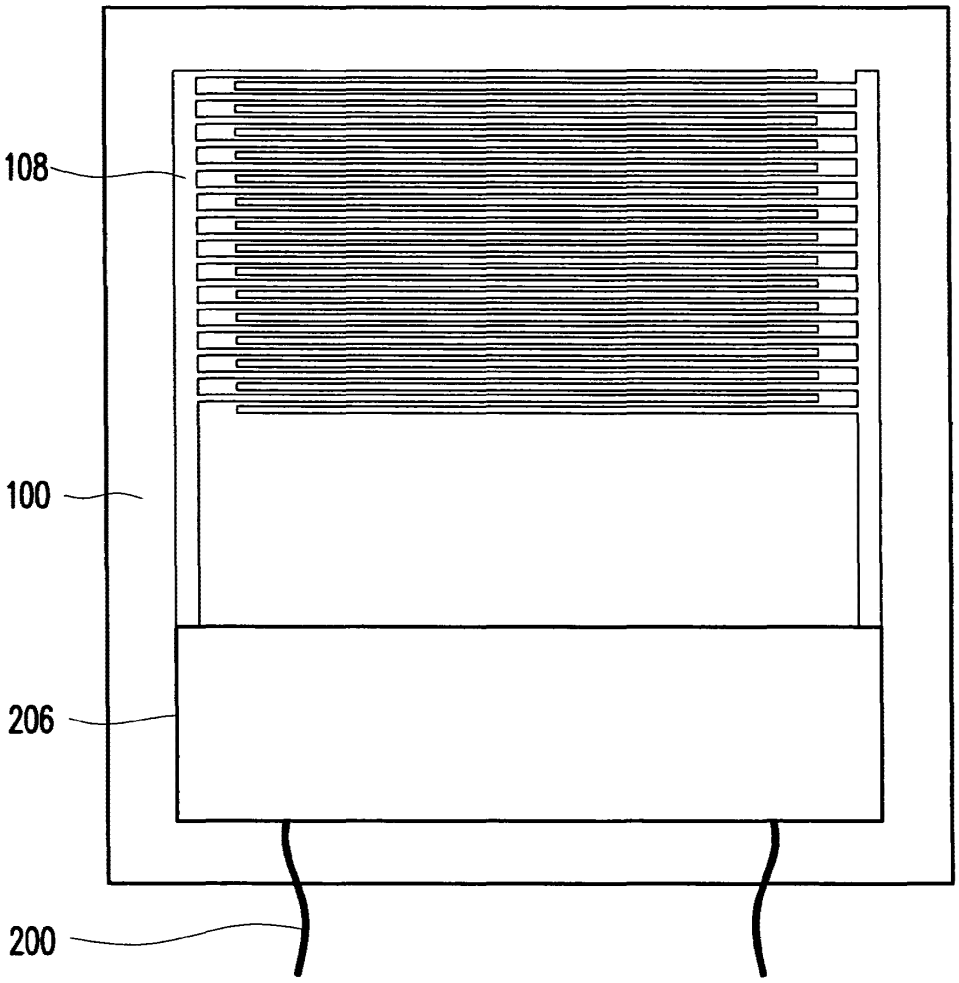


圖 5C

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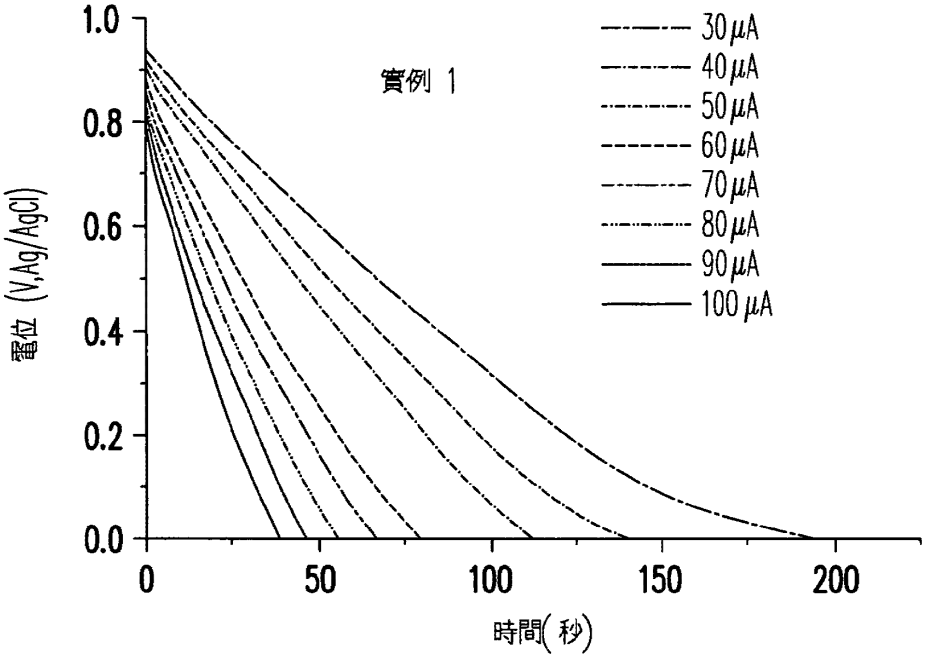


圖 6

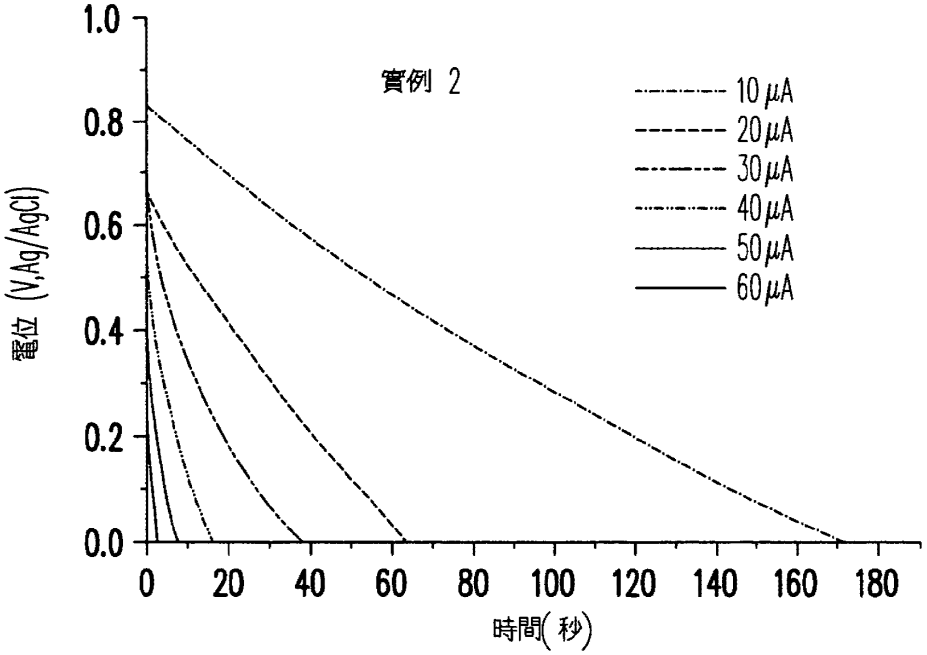


圖 7

37215TW_T

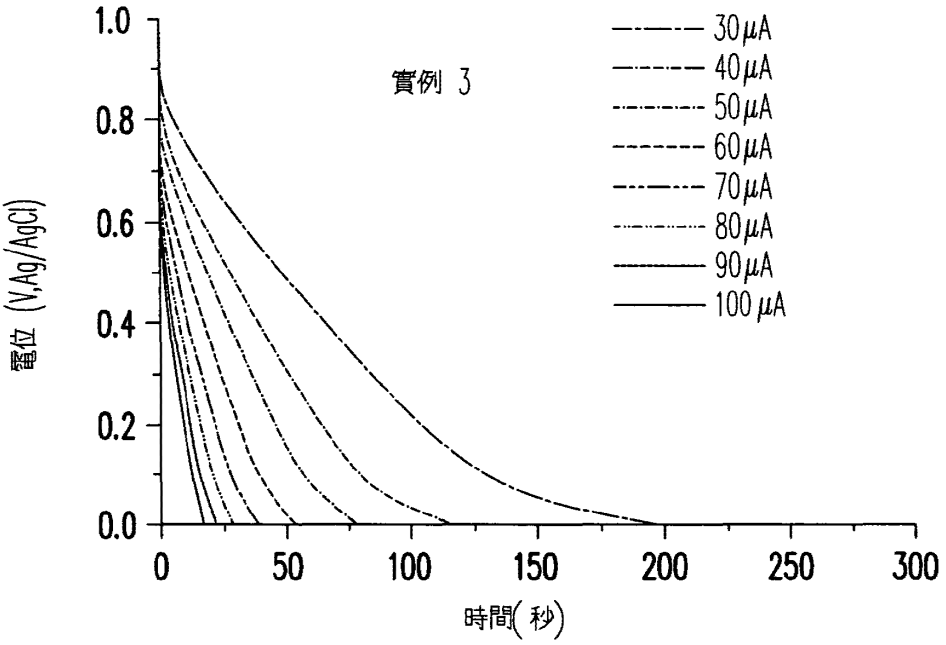


圖 8

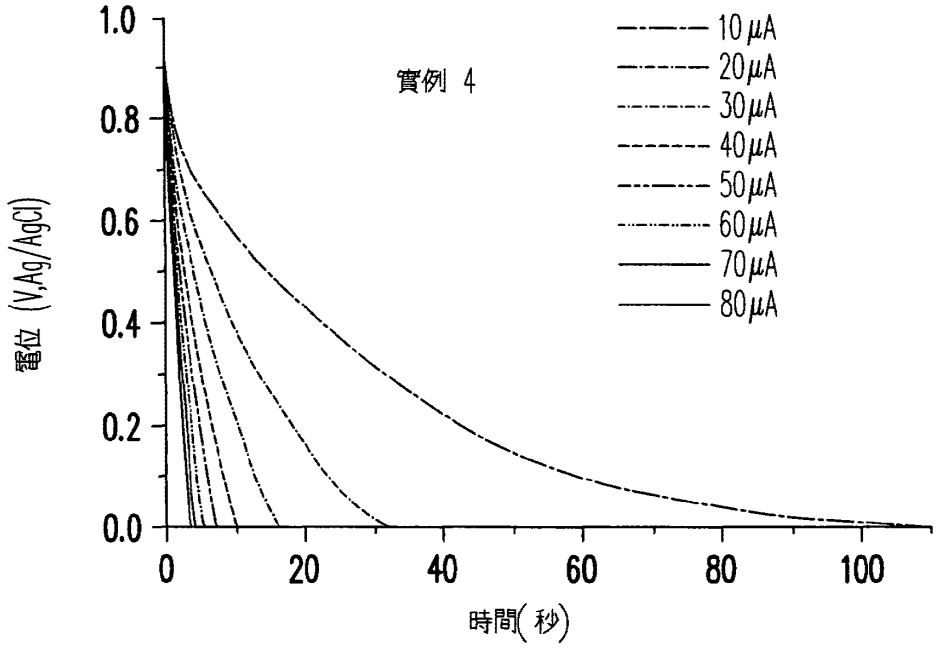


圖 9

the conventional ultra-capacitor having parallel electrodes, so that the application thereof is not limited.

四、指定代表圖：

（一）本案之指定代表圖：圖 2

（二）本代表圖之元件符號簡單說明：

10：平面超高電容器

100：基材

108：奈米碳管薄膜

110：過渡金屬之氧化物層

112：圖案化緩衝層

114：圖案化集電層

116：圖案化觸媒層

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

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Search terms : (1) (200943707)@PN 【 印出 】

Patent/Publication Number	200943707
Title	Semiconductor device having balanced band-pass filter implemented with LC resonators
Issued/Publication Date	2009/10/16
Application Date	2008/12/16
Application Number	097148898 Espacenet
IPC	H03H-007/01(2006.01);H03H-007/42(2006.01)
Inventor	LIU, KAI CN; FRYE, ROBERT C. US; LIN, YAO-JIAN CN
Applicant	STATS CHIPPAC, LTD.SG
Individual	F
Priority Number	20071228 US 20070017360P
Abstract	A band-pass filter has a plurality of frequency band channels each including a first inductor having a first terminal coupled to a first balanced port and a second terminal coupled to a second balanced port. A first capacitor is coupled between the first and second terminals of the first inductor. A second inductor has a first terminal coupled to a first unbalanced port and a second terminal coupled to a second unbalanced port. The second inductor is disposed within a first distance of the first inductor to induce magnetic coupling. A second capacitor is coupled between the first and second terminals of the second inductor. A third inductor is disposed within a second distance of the first inductor and within a third distance of the second inductor to induce magnetic coupling. A third capacitor is coupled between first and second terminals of the third inductor.

Information on this system is for reference only, it cannot be used as grounds for approval or rejection.
In all instances of discrepancy, official publication from TIPO shall prevail and should be consulted.

200943707

發明專利說明書

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※ 申請案號：97148898

※ 申請日期：97.12.16　　※IPC 分類：H03H 7/01 (2006.01)
H03H 7/42 (2006.01)

一、發明名稱：（中文/英文）

具有以 LC 共振器執行平衡式帶通濾波器之半導體裝置

SEMICONDUCTOR DEVICE HAVING BALANCED BAND-PASS FILTER IMPLEMENTED WITH LC RESONATORS

二、申請人：（共 1 人）

姓名或名稱：（中文/英文）

史達晶片有限公司 / STATS ChipPAC, Ltd.

代表人：（中文/英文）

陳勵勤 / TAN, LAY KOON

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新加坡 569059 科技重點區#05-17/20 安哥摩基歐街 10 號第 65 號公寓

國　籍：（中文/英文）

新加坡 / SINGAPORE

三、發明人：（共 3 人）

姓　名：（中文/英文）

1. 劉凱 / LIU, Kai
2. 羅勃特 D.　富萊 / FRYE, Robert D.
3. 林耀劍 / LIN, Yaojian

國　籍：（中文/英文）

1. 中國大陸 / China
2. 美國 / USA
3. 中國大陸 / China

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四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：　年　月　日。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

美國、2007.12.28、61/017,360

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

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九、發明說明：

【發明所屬之技術領域】

本發明概略有關於半導體裝置，並且尤其是有關於一種具有以LC共振器所執行之平衡式帶通濾波器的半導體裝置。

【先前技術】

半導體裝置常見於現代電子產品。半導體裝置在電子元件之數量及密度上會有所變化。離散半導體裝置通常含有某一類型的電氣元件，即如發光二極體(LED)、電晶體、電阻器、電容器、電感器及電力氧化金屬半導體場效電晶體(MOSFET)。整合式半導體裝置一般含有數百至數百萬個電氣元件。整合式半導體裝置的範例包含微控制器、微處理器、電荷耦接裝置(CCD)、太陽能電池及數位微映鏡(DMD)裝置。

半導體裝置可執行廣泛各種的功能，像是進行高速計算、傳送及接收電磁信號、控制電子裝置、將陽光轉換成電力以及產生用於電視顯示器的視覺投射。半導體裝置可見於娛樂、通訊傳播、發電、網路、電腦及消費性產品的領域中。半導體裝置亦常見於包含軍事、航空、汽車、工業用控制器及辦公室設備的電子產品裡。

半導體裝置運用半導體材料的電子性質。半導體材料的原子結構使得讓其導電性能夠藉由施加一電場或透過摻質製程而加以操縱。摻質處理可將不純物引入至該半導體材料內，藉此操縱並控制該半導體裝置的導電性。

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一半導體裝置含有主動及被動電氣結構。主動結構，包含電晶體在內，可控制電流的流注。藉由改變摻質程度及一電場的施加，該電晶體即可促進或禁制電流的流注。而被動結構，包含電阻器、二極體及電感器在內，可於電壓與電流之間產生一為執行各種電氣功能所必要的關係。該等被動及主動結構係經電氣連接以構成邏輯電路，如此讓該半導體裝置能夠執行高速計算作業以及其他的可用功能。

半導體裝置通常是利用兩類複雜的製程處理所製造，亦即前端製造及後端製造，而各者皆可能牽涉到數以百計的步驟。前端製造牽涉到在一半導體晶圓的表面上構成複數個晶粒。各晶粒通常為等同且含有藉由電氣連接主動及被動元件所構成的電路。後端製造則牽涉到自所完成晶圓單切個別晶粒，並且將該晶粒封裝以提供結構性支撐與環境隔離。

半導體製造之一目標即為產生較小的半導體裝置。較小的裝置通常耗用較少電力、具備較高效能並且可更有效率地生產。此外，較小的半導體裝置具有較小的廓跡，而此確為小型末端產品所欲者。可藉由改善前端製程以獲致擁有較小且較高密度之主動及被動元件的晶粒從而達到較小的晶粒尺寸。後端製程則可藉由改善電氣互連及封裝材料以獲致具較小廓跡的半導體裝置封裝。

半導體製造的另一目標在於產生較高效能的半導體裝置。可藉由構成能夠按較高速度運作的主動元件來提高裝

置效能。在像是射頻(RF)無線通訊的高頻率應用項目裡，經常會將整合式被動裝置(IPD)納入在該半導體裝置之內。IPD的範例包含電阻器、電容器及電感器。一典型RF系統需要在一或更多半導體封裝裡設置多個IPD，以利執行必要的電氣功能。

平衡-不平衡轉換器(Balun)及帶通濾波器(BPF)在無線通訊系統中為重要元件。許多先前技藝設計者利用離散、級聯之元件以達到平衡及過濾兩者功能。平衡-不平衡轉換器係經實作成一種分散式線路，而其中尺寸是與操作頻率成反比關係。操作頻率愈低，所需之平衡-不平衡轉換器即愈大。然消費者需要較小尺寸，這會使得在像是GSM行動電話的較低頻率應用項目中難以進行最小化。

【發明內容】

存在一種將用於RF信號處理電路之平衡-不平衡轉換器予以最小化的需要。從而，在一具體實施例裡，本發明為一帶通濾波器，其中含有複數個頻帶通道，各通道含有一第一及第二平衡式連接埠以及第一及第二不平衡式連接埠。各頻帶通道含有一第一電感器，此電感器的一第一終端係經耦接於該第一平衡式連接埠而一第二終端則經耦接於該第二平衡式連接埠。一第一電容器係經耦接於該第一電感器的第一及第二終端之間。一第二電感器具有一第一終端，此終端係經耦接於該第一不平衡式連接埠，以及一第二終端，此終端係經耦接於一第二不平衡式連接埠。該第二電感器係經設置在該第一電感器的一第一距離之內，

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藉以於該等第一與第二電感器之間感應磁性耦接。一第二電容器係經耦接於該第二電感器的第一及第二終端之間。一第三電感器係經設置在該第一電感器的一第二距離之內以及該第二電感器的一第三距離之內，藉以於該等第一、第二與第三電感器之間感應磁性耦接。一第三電容器係經耦接於該第三電感器的第一及第二終端之間。

在另一具體實施例裡，本發明為一帶通濾波器，其中含有複數個 LC 共振器，各共振器具有一第一及第二平衡式連接埠以及第一及第二不平衡式連接埠。該帶通濾波器含有一第一電感器，此電感器具有一第一終端，此終端係經耦接於該第一平衡式連接埠，以及一第二終端，此終端係經耦接於該第二平衡式連接埠。一第一電容器係經耦接於該第一電感器的第一及第二終端之間。一第二電感器具有一第一終端，此終端係經耦接於該第一不平衡式連接埠，以及一第二終端，此終端係經耦接於該第二不平衡式連接埠。一第二電容器係經耦接於該第二電感器的第一及第二終端之間。一第三電感器係經設置在鄰近於該等第一及第二電感器處，藉以於該等第一、第二與第三電感器之間感應磁性耦接。一第三電容器係經耦接於該第三電感器的第一及第二終端之間。

在另一具體實施例裡，本發明為一 LC 共振器電路，此電路中含有一具有第一及第二終端的第一電感器。一第一電容器係經耦接於該第一電感器的第一及第二終端之間。一第二電感器具有第一及第二終端。一第二電容器係經耦

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接於該第二電感器的第一及第二終端之間。一第三電感器係經設置在鄰近於該等第一及第二電感器處，藉以於該等第一、第二與第三電感器之間感應磁性耦接。一第三電容器係經耦接於該第三電感器的第一及第二終端之間。

在另一具體實施例裡，本發明為一積體電路封裝，其中承載有複數個 LC 共振器，並且具有第一、第二、第三及第四互連終端。該積體電路含有一第一電感器，此電感器具有一第一終端，此終端係經耦接於該第一互連終端，以及一第二終端，此終端係經耦接於該第二互連終端。一第一電容器係經耦接於該第一電感器的第一及第二終端之間。一第二電感器具有一第一終端，此終端係經耦接於該第一互連終端，以及一第二終端，此終端係經耦接於該第二互連終端。一第二電容器係經耦接於該第二電感器的第一及第二終端之間。一第三電感器係經設置在鄰近於該等第一及第二電感器處，藉以於該等第一、第二與第三電感器之間感應磁性耦接。一第三電容器係經耦接於該第三電感器的第一及第二終端之間。

【實施方式】

在後文說明中將參照隨附圖式以於一或更多具體實施例中描述本發明，而該等圖式中的類似編號代表相同或類似構件。本發明雖係按照為達到本發明目的之最佳模式所描述，然熟諳本項技藝之人士將能瞭解所欲者係涵蓋可經納入在由按本揭示及圖式所支持之後載申請專利範圍及其等同項目而定義的本發明精神與範疇內之替代、修改及等

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同物。

半導體裝置概為利用兩類複雜的製程處理所製造：前端製造及後端製造。前端製造牽涉到在一半導體晶圓的表面上構成複數個晶粒。該晶圓上的各晶粒含有許多主動及被動元件，此等係經電氣連接以構成功能性電路。主動電氣元件，像是電晶體，擁有控制電流流注的能力。而被動電氣元件，即如電容器、電感器、電阻器及變壓器，則是可在電壓與電流之間產生一為執行各種電路功能所必要的關係。

被動及主動元件係藉由一系列處理步驟而構成於該半導體晶圓的表面上，此等步驟包含摻質、沉積、光刻、蝕刻及平面化製程。摻質是藉由離子植入或熱性擴散的技術以將雜質引入至該半導體材料之內。該摻質製程可修改主動裝置內之半導體材料的導電性，將該半導體轉換成一永久絕緣體、永久導體，或是改變該半導體材料回應於一電場而在導電性方面變動的方式。電晶體含有多個具有不同類型及程度之摻質的範圍，此等範圍可視需要而加以排置，藉此當施加一電場時讓該電晶體能夠促進或禁制電流的流注。

主動及被動元件是由具不同電氣性質之材料的疊層所構成。該等疊層可藉由各種沉積技術所構成，而這些技術是部份地由所予沉積之材料的類型所決定。例如，薄膜沉積可牽涉到化學汽相沉積(CVD)、物理汽相沉積(PVD)、電鍍鍍置及無電鍍置製程。各疊層通常係經樣式化以構成主

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動元件、被動元件或是該等元件間之電氣連接的多個局部。

可利用光刻作業以對該等疊層進行樣式化，此作業牽涉到在欲予樣式化之疊層上沉積即如光阻物的光敏材料。利用光線將一樣式自一光罩傳佈至該光阻物。在該光阻物樣式中承受到光線的局部會被利用一溶劑加以移除，從而曝出待予樣式化的底層局部。其餘的光阻物會被移除而留下一經樣式化疊層。或另者，有些類型的材料是將該材料直接地沉積在由一利用像是無電及電鍍鍍置處理之先前沉積/蝕刻製程所構成的區域或空處內之方式所樣式化。

在一現有樣式上沉積一材料薄膜可能誇大底層樣式並且產生一非均勻平坦表面。而為產生較微小且較密集包封的主動及被動元件，均勻平坦表面確為必要。可利用平面化作業以自該晶圓的表面移除材料，並且產生均勻平坦表面。平面化作業牽涉到藉一拋光板以對該晶圓的表面進行拋光處理。可在拋光過程中對該晶圓的表面增置一摩擦性材料及腐蝕性化學物。該摩擦物的合併機械作用以及該化學物的腐蝕性作用可移除任何不規則拓樸，從而獲致一均勻平坦表面。

後端製造是指將所獲晶圓切割或單切成個別晶粒，然後封裝該晶粒以結構性支撐與環境隔離。而為單切該晶粒，可沿該晶圓中稱為鋸切行道或準線之非功能性範圍將該晶圓劃割並予打斷。可利用一雷射切割裝置或鋸刀以單切該晶圓。在單切作業之後，將個別晶粒架置於一封裝基板上，此者含有腳針或接觸板以供互連於其他系統元件。

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然後將經構成於該半導體晶粒上的接觸板連接至該封裝內的接觸板。可利用焊燒凸塊、柱狀凸塊、導體膏劑或接線連附以進行電氣連接。將一密封物或其他模鑄材料沉積在該封裝上，藉以提供物理支撐及電氣隔離。然後再將所獲封裝插入一電氣系統中，並令該半導體裝置的功能性能夠由其他系統元件獲用。

圖 1 說明電子裝置 10，此裝置具有一晶片載板或印刷電路板(PCB) 12，而該板之表面上架置了複數個半導體封裝。該電子裝置 10 可根據應用項目而定具備單一類型的半導體封裝或是多個類型的半導體封裝。而為示範之目的圖 1 顯示不同類型的半導體封裝。

該電子裝置 10 可為一單立式系統，此者利用該等半導體封裝以執行一電氣功能。或另者，該電子裝置 10 可為一較大型系統的子元件。例如，該電子裝置 10 可為一可供插入一電腦之內的圖形卡、網路介面卡或其他信號處理卡。該半導體封裝可含有微處理器、記憶體、應用特定積體電路(ASIC)、邏輯電路、類比電路、RF 電路、離散裝置或是其他半導體晶粒或電氣元件。

在圖 1 中，該 PCB 12 可供作為對於經架置在該 PCB 上之半導體封裝的結構性支撐及電氣互連之一般基板。導體信號跡線 14 係利用汽化處理、電鍍鍍置、無電鍍置、網版印刷、PVD 或是其他的適當金屬沉積製程而經構成於該 PCB 12 的表面之上或疊層之內。該等信號跡線 14 提供該等半導體封裝、所架置元件與其他外部系統元件各者之間的電氣

傳通。該等跡線 14 亦提供對於該等半導體封裝各者的電力及接地連接。

在一些具體實施例裡，一半導體裝置具有兩個封裝層級。第一級封裝處理係一用以將該半導體晶粒機械地及電氣地接附至一載體的技術。第二級封裝處理則牽涉到將該載體機械地及電氣地接附至該 PCB。在其他具體實施例裡，一半導體裝置可僅具有該第一級封裝處理，而其中是將該晶粒直接地以機械方式及電氣方式架置於該 PCB。

為示範之目的，該 PCB 12 上顯示出包含線路貼接封裝 16 及覆晶片 18 在內之多種類型的第一級封裝處理。此外，圖式中顯示在該 PCB 12 上架置有許多類型的第二級封裝處理，包含球柵陣列(BGA) 20、凸塊晶片載體(BCC) 22、雙線內封裝(DIP) 24、地柵陣列(LGA) 26、多晶片模組(MCM) 28、四方扁平無引腳封裝(QFN) 30 及四方扁平封裝 32。根據系統要求而定，可將按任何第一及第二級封裝方式之組合所組態設定的半導體封裝以及其他電子元件的任意組合連接至該 PCB 12。在一些具體實施例裡，該電子裝置 10 含有一經單一接附的半導體封裝，而其他具體實施例可要求多個互連封裝。藉由在一單一基板上組合一或更多的半導體封裝，製造商即可將預製元件併入在電子裝置及系統內。由於該等半導體封裝含有複雜的功能性，因此可利用較價廉的元件及較簡短的製造程序來製造電子裝置。所獲裝置較不易失效且製造成本較低，從而降低消費者的成本。

圖 2a 說明經架置於該 PCB 12 上之 DIP 24 的進一步細

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節。該 DIP 24 包含一半導體晶粒 34，而該晶粒具有接觸板 36。該半導體晶粒 34 含有一主動範圍，其中含有類比或數位電路，此等電路係經實作如經構成於該半導體晶粒 34 內的主動裝置、被動裝置、導體層及介電層，並根據該晶粒的電氣設計所電氣互連。例如該電路可含有一或更多的電晶體、二極體、電感器、電容器、電阻器以及其他經構成於該晶粒 34 之主動範圍內的電路構件。該等接觸板 36 是由導體材料所製成，像是鋁(Al)、銅(Cu)、錫(Sn)、鎳(Ni)、金(Au)或銀(Ag)，並且電氣連接至經該構成於該晶粒 34 內的電路構件。該等接觸板 36 可為由 PVD、CVD、電鍍鍍置或無電鍍置製程所構成。在組裝該 DIP 24 的過程中，可利用一金-矽共熔層，或像是熱性樹脂的黏附材料，以將該半導體晶粒 34 架置於一載體 38。該封裝本體含有一像是聚合物或陶瓷的絕緣封裝材料。導體導線 40 係經連接至該載體 38，並且接線連附 42 係經構成於該等導線 40 與該晶粒 34 的接觸板 36 之間而作為一第一級封裝。密封物 44 係經沉積在該封裝上，俾藉由防止蒸氣及顆粒進入該封裝之內且污染該等晶粒 34、接觸板 36 或接線連附 42 以提供環境性保護。該 DIP 24 係藉由將該等導線 40 插入到穿透該 PCB 12 所構成的孔洞之內而連接至該 PCB 12。焊燒材料 46 在該等導線 40 附近流動，並且進入該等孔洞以將該 DIP 24 實體地且電氣地連接至該 PCB 12。該焊燒材料 46 可為任何金屬或導電性材料，即如 Sn、鉛(Pb)、Au、Ag、Cu、鋅(Zn)、鉍(Bi)及其等之合金，並連同選擇性的焊劑材料。例如，該焊

劑材料可為共熔 Sn/Pb、高鉛或無鉛物。

圖 2b 說明經架置於該 PCB 12 上之 BCC 22 的進一步細節。該半導體晶粒 47 係藉一接線連附式第一級封裝處理而連接至一載體。該 BCC 22 係藉一 BCC 式第二級封裝處理而架置於該 PCB 12。該具有接觸板 48 的半導體晶粒 47 則是利用一底層填入或環氧樹脂黏著材料 50 而架置於一載體上。該半導體晶粒 47 含有一主動範圍，其中含有類比或數位電路，此等電路係經實作如經構成於該半導體晶粒 47 內之主動裝置、被動裝置、導體層及介電層，並且根據該晶粒的電氣設計所電氣互連。例如該電路可含有一或更多的電晶體、二極體、電感器、電容器、電阻器以及其他經構成於該晶粒 47 之主動範圍內的電路構件。該等接觸板 48 是由導體材料所製成，像是 Al、Cu、Sn、Ni、Au 或 Ag，並且電氣連接至經該構成於該晶粒 47 內的電路構件。該等接觸板 48 可為由 PVD、CVD、電鍍鍍置或無電鍍置製程所構成。該等接線連附 54 以及連附板 56 和 58 將該半導體晶粒 47 的接觸板 48 電氣連接至該 BCC 22 的接觸板 52，而構成該第一級封裝處理。模鑄化合物或密封物 60 係經沉積於該等半導體晶粒 47、接線連附 54、接觸板 48 及接觸板 52 上以對於該裝置提供實體支撐及電氣隔離。接觸板 64 係利用汽化處理、電鍍鍍置、無電鍍置、網版印刷、PVD 或是其他的適當金屬沉積製程而構成於該 PCB 12 的一表面上，並且通常是被鍍置以防止氧化。該等接觸板 64 電氣連接至一或更多導體信號跡線 14。焊燒材料係經沉積於該 BCC 22

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的接觸板 52 與該 PCB 12 的接觸板 64 之間。該焊燒材料係經重流以構成凸塊 66，而此等凸塊可構成該 BCC 22 與該 PCB 12 之間的機械及電氣連接。

在圖 2c 裡，該半導體晶粒 18 係藉一覆晶式第一級封裝處理而經架置向下面朝於該載體 76。該 BGA 20 係藉一 BGA 式第二級封裝處理而接附於該 PCB 12。主動範圍 70 含有類比或數位電路，此等電路係經實作如經構成於該半導體晶粒 18 內之主動裝置、被動裝置、導體層及介電層，並且根據該晶粒的電氣設計所電氣互連。例如，該電路可含有一或更多的電晶體、二極體、電感器、電容器、電阻器以及其他經構成於該半導體晶粒 18 之主動範圍 70 內的電路構件。該半導體晶粒 18 係透過大量的個別導體焊燒凸塊或球體 78 所電氣及機械接附於該載體 76。該等焊燒凸塊 78 係經構成於係經設置在該主動範圍 70 上的凸塊板或互連處所 80 上。該等凸塊板 80 是由導體材料所製成，像是 Al、Cu、Sn、Ni、Au 或 Ag，並且電氣連接至經該構成於該主動範圍 70 內的電路構件。該等凸塊板 80 是由 PVD、CVD、電鍍鍍置或無電鍍置製程所構成。該等焊燒凸塊 78 係藉一焊燒重流製程而電氣且機械連接於該載體 76 上的接觸板或互連處所 82。

該 BGA 20 係藉大量的個別導體焊燒凸塊或球體 86 所電氣且機械接附於該 PCB 12。該等焊燒凸塊係經構成於凸塊板或互連處所 84 上。該等凸塊板 84 透過行經該載體 76 的導體線路 90 而電氣連接至互連處所 82。接觸板 88 係利

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用汽化處理、電鍍鍍置、無電鍍置、網版印刷、PVD 或是其他的適當金屬沉積製程而經構成於該 PCB 12 的表面上，並且通常係經鍍置以防止氧化。該等接觸板 88 電氣連接至一或更多導體信號跡線 14。焊燒凸塊 86 係藉一焊燒重流製程而電氣且機械連接至該 PCB 12 上的接觸板或連附板 88。模鑄化合物或密封物 92 係經沉積於該等半導體晶粒 18 及載體 76 上以對於該裝置提供實體支撐及電氣隔離。該覆晶半導體裝置可提供一自該半導體晶粒 18 之主動裝置至該 PCB 12 之導體跡線的短型電氣傳導路徑，藉以縮短信號傳播距離，減少電容性並獲致整體較佳的電路效能。在其他具體實施例裡，可利用覆晶式第一級封裝處理以將該半導體晶粒 18 直接地機械且電氣接附於該 PCB 12，而無須該載體 76。

現參照圖 3，該半導體晶粒或封裝 94 含有一半導體基板 96，此基板是由矽(Si)、砷化鎵(GaAS)、玻璃或是其他體型半導體材料所製成，藉此提供結構性支撐。一主動範圍 98 係經構成於該半導體基板 96 的上方表面上。該主動範圍 98 可根據該晶粒的電氣設計而含有主動裝置及整合式被動裝置(IPD)、導體層及介電層。該等主動裝置包含電晶體、二極體等等。該 IPD 可包含薄膜電感器、電阻器及電容器。該主動範圍 98 佔據該半導體晶粒 94 中約 5-10%的整體厚度或高度 H1。該半導體晶粒 94 可利用覆晶、連附接線或互連腳針以電氣連接至其他裝置。

含有複數個 IPD 的半導體裝置可運用於高頻率應用項

目，像是微波雷達、電信、無線收發器、電子開關及其他執行射頻(RF)電氣功能的裝置。該等 IPF 提供電路功能的電氣特徵，像是平衡-不平衡轉換器(Balun：balanced and unbalanced)、共振器、高通濾波器、低通濾波器、帶通濾波器(BPF)、對稱 Hi-Q 共振變壓器、匹配網路及諧調電容器。例如該等 IPD 可運用作為前端無線 RF 元件而可經設置於天線與收發器之間。該無線應用項目可為利用多個頻帶操作的行動電話，像是寬頻碼分多重存取(WCDMA)頻帶(PCS、IMT，低)以及全球系統行動通訊(GSM)頻帶(低及高)。

平衡-不平衡轉換器經常是用以透過電磁耦接來改變阻抗並將共同模式雜訊最小化。在一些具體實施例裡，可在一相同基板上構成多個平衡-不平衡轉換器以提供多頻帶操作。例如，可在用於行動電話或其他 GSM 通訊的四方頻帶中使用兩個以上的平衡-不平衡轉換器，而各個平衡-不平衡轉換器專屬於該四方頻帶裝置的一操作頻帶。一典型 RF 系統在一或更多半導體封裝裡需要多個 IPD 及其他高頻率電路，藉以執行必要的電氣功能。

圖 4 顯示一使用 RF 積體電路(RFIC) 102 的無線通訊系統 100。該 RFIC 102 執行對於在五個不同頻帶處理通道中(頻帶 A、頻帶 B、頻帶 C、頻帶 D 及頻帶 E)之 RF 信號的 BPF 信號處理。頻帶 A 具有一不平衡式連接埠或終端 104；頻帶 B 具有一不平衡式連接埠或終端 106；頻帶 C 具有一不平衡式連接埠或終端 108；頻帶 D 具有一不平衡式連接埠或終端 110；頻帶 E 具有一不平衡式連接埠或終端 112。接

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地終端 116 係一對於頻帶 A-E 中之不平衡式連接埠 104-112 的回返路徑。頻帶 A 具有一平衡式連接埠或終端 118 和 120；頻帶 B 具有一平衡式連接埠或終端 122 和 124；頻帶 C 具有一平衡式連接埠或終端 126 和 128；頻帶 D 具有一平衡式連接埠或終端 130 和 132；頻帶 E 具有一平衡式連接埠或終端 134 和 136。平衡式連接埠 118-136 係分別地耦接至該收發器 140 以進行進一步的傳送器及接收器信號處理。該等無線 RF 元件利用多個頻帶以增加功能性及服務。例如，頻帶 A-C 處理 WCDMA 而頻帶 D-E 處理 GSM。該 RFIC 102 利用在各頻帶 A-E 內的平衡-不平衡轉換器，藉以轉換阻抗並將共同模式雜訊最小化。

圖 5 顯示具頻帶 A-E 處理通道之 RFIC 102 的進一步佈置細節。在一具體實施例裡，該 RFIC 102 佔據一 3.2 毫米(mm)乘 2.2 mm 的面積。圖 6a 顯示一對應於頻帶 A 而含有不平衡式連接埠 104、接地終端 116 的等同電路略圖，並且電容器 142 及電感器 144 係經耦接於該不平衡式連接埠 104 與該接地終端 116 之間。一電感器 146、電容器 150 及電阻器 152 係經耦接於該等不平衡式連接埠 118 及 120 之間。該電阻器 152 提供一平坦帶通回應。一直流(DC)電力匯流排 154 係經耦接於該電感器 146 的中心點。該 DC 電力匯流排 154 係共用於全部的所連接裝置。該 DC 電力係經施加於終端 156。由於近密間隔及交錯布置之故，可於該等電感器 144 與 146 之間感應出一互相電感或磁性耦接。從而，該等電感器 144-146 可在頻帶 A 裡於一 BPF 排置中運作如一平

衡-不平衡轉換器的一部份。

頻帶B係按類似於圖6a方式所組態設定，其中含有不平衡式連接埠106、接地終端116，並且電容器160及電感器162係經耦接於該不平衡式連接埠106與該接地終端116之間。一電感器164、電容器166及電阻器168係經耦接於該等平衡式連接埠122及124之間。該電阻器168提供一平坦帶通回應。DC電力匯流排154係經耦接於該電感器164的中心點。由於近密間隔及交錯布置之故，可於該等電感器162與164之間感應出一互相電感或磁性耦接。從而，該等電感器162-164可在頻帶B裡於一BPF排置中運作如一平衡-不平衡轉換器的一部份。

頻帶C係按類似於圖6a方式所組態設定，其中含有不平衡式連接埠108、接地終端116，並且電容器170及電感器172係經耦接於該不平衡式連接埠108與該接地終端116之間。一電感器174、電容器176及電阻器178係經耦接於該等平衡式連接埠126及128之間。該電阻器178提供一平坦帶通回應。DC電力匯流排154係經耦接於該電感器174的中心點。由於近密間隔及交錯布置之故，可於該等電感器172與174之間感應出一互相電感或磁性耦接。從而，該等電感器172-174可在頻帶C裡於一BPF排置中運作如一平衡-不平衡轉換器的一部份。

頻帶D係按類似於圖6b方式所組態設定，其中含有不平衡式連接埠110、接地終端116，並且電容器182係經耦接於該不平衡式連接埠110與該接地終端116之間。電感

器 186 係經耦接於該不平衡式連接埠 110 與一節點 185 之間。電容器 184 係經耦接於該節點 185 與該接地終端 116 之間。一電感器 188 及電容器 190 的平行組合係經耦接於該節點 185 與節點 191 之間。電容器 192 及電感器 194 係經耦接於該節點 191 與該接地終端 116 之間。該等電容器 182、184、190 及 192 以及電感器 186 及 188 運作如一低通濾波器。一電感器 196 係經耦接於該等平衡式連接埠 130 及 132 之間。一電容器 198 及 200 的串列組合係經耦接於該等平衡式連接埠 130 及 132 之間。一電阻器 202 係經耦接於該等平衡式連接埠 130 及 132 之間。該電阻器 202 提供一平坦帶通回應。DC 電力匯流排 154 係經耦接於該電感器 196 的中心點和該等電容器 198 與 200 之間的接合點。由於近密間隔及交錯布置之故，可於該等電感器 194 與 196 之間感應出一互相電感或磁性耦接。從而，該等電感器 194-196 可在頻帶 D 裡於一 BPF 排置中運作如一平衡-不平衡轉換器的一部份。

頻帶 E 係按類似於圖 6c 方式所組態設定，其中含有不平衡式連接埠 112、接地終端 116，並且電感器 210 係經耦接於該不平衡式連接埠 112 與一節點 212 之間。一電容器 214 係經耦接於該節點 212 與該接地終端 116 之間。一電容器 216 及電感器 218 的平行組合係經耦接於該節點 212 與節點 220 之間。一電容器 222 及電感器 224 係經耦接於該節點 220 與該接地終端 116 之間。該等電容器 214、216 及 222 以及電感器 210 及 218 運作如一低通濾波器。一電感器

226係經耦接於該等平衡式連接埠134及136之間。一電容器228及230的串列組合係經耦接於該等平衡式連接埠134及136之間。一電阻器232係經耦接於該等平衡式連接埠134及136之間。該電阻器232提供一平坦帶通回應。DC電力匯流排154係經耦接於該電感器226的中心點和該等電容器228與230之間的接合點。由於近密間隔及交錯布置之故，可於該等電感器224與226之間感應出一互相電感或磁性耦接。從而，該等電感器224-226可在頻帶E裡於一BPF排置中運作如一平衡-不平衡轉換器的一部份。

圖7顯示一種在該RFIC 102中所使用之平衡-不平衡轉換器的替代性具體實施例。該平衡-不平衡轉換器238係利用LC(電感器及電容器)共振器所實作，其可整合於圖3的基板96上。在本例中，該平衡-不平衡轉換器238係經耦接於該RFIC 102內的不平衡式連接埠與平衡式連接埠之間。一電感器240含有經耦接於不平衡式連接埠242及244的第一及第二末端終端。在一具體實施例裡，該連接埠242係一單一末端不平衡式連接埠，而該連接埠244係一接地終端。或另者，該連接埠244係一單一末端不平衡式連接埠，而該連接埠242係一接地終端。電容器246係經耦接於該等不平衡式連接埠242及244之間。一電感器240及電容器246組成一第一LC共振器。一電感器248含有經耦接於平衡式連接埠250及252的第一及第二末端終端。一電容器254係經耦接於該等平衡式連接埠250及252之間。該電感器248及該電容器254組成一第二LC共振器。該電

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感器 240 係經設置在距該電感器 248 的距離 d1 處。一電感器 256 含有末端終端 258 及 260。一電容器 262 係經串列耦接於該電感器 256 的末端終端 258 及 260 之間。該等電感器 256 及電容器 262 組成一第三 LC 共振器。電感器 256 係經設置在該等電感器 240 及 248 的週邊附近，並按平面區隔 d2、d3、d4 及 d5 而未重疊。該電感器 256 可相對該等電感器 240 及 248 而具有較大、較小或對稱值。

圖 7 所示電路佈置係經實作於該 RFIC 102 中，並且提供平衡-不平衡轉換器及濾波器功能，亦即按一小型形式因數的平衡式濾波器。該電路利用互相電感或磁性感應耦接而含有三個 LC 共振器。該等電感器 240、248 及 256 可具有一長方形、多邊形或圓形的形式或形狀，並經纏繞以產生磁性耦接。該等電容器 246 及 254 可對該平衡-不平衡轉換器提供靜電釋放(ESD)保護。該等電感器 240、248 及 256 係利用 8μm 像是 Al、Cu、Sn、Ni、Au 或 Ag 的導體材料所實作。該等電容器 246、254 及 262 是利用薄膜介電物所實作。該薄膜材料可提高電容密度。藉由利用跨於脆弱電容器上的電感分流保護，即可在該薄膜材料內獲致 ESD 強固性。在一 ESD 事件裡的大部份能量皆為集中於低頻率，而對此在奈米亨利範圍內的電感器為有效短路。在該磁性耦接電路中，各個電容器係由一低值分流電感器所保護，藉以增加對於 ESD 的強固性。

該等電感器 240 及 248 之間的互相電感或磁性耦接強度是由兩個線圈之間的距離 d1 所決定。同樣地，該等電感

器 240 及 256 之間，以及該等電感器 248 及 256 之間，的磁性耦接強度是由兩個線圈之間的距離 d2、d3、d4 及 d5 所決定。在一具體實施例裡，該等距離 d1-d5 是被設定為 10μm。可調整該等經電容負載之電感環間的分隔以選定該等 BPF 參數，藉此諧調該磁性耦接。該等電容器 246、254 及 262 係經諧調以針對所要求之應用項目進行阻抗匹配。該等不平衡式連接埠 242 及 244 以及平衡式連接埠 250 及 252 並不共享一共用 DC 參考。各個輸入及輸出可為單一末端或是差分方式運作。在要求平衡至不平衡轉換的應用項目中並不需要分別的平衡-不平衡轉換器。

該 RFIC 102 中所使用者之平衡-不平衡轉換器的另一具體實施例可如圖 8 所示。該平衡-不平衡轉換器 268 係利用多個 LC 共振器所實作，且此等共振器可經整合於圖 3 的基板 96 上。在本例中，該平衡-不平衡轉換器 268 係經耦接於該 RFIC 102 的不平衡式連接埠與平衡式連接埠之間。一電感器 270 含有經耦接於該等不平衡式連接埠 272 及 274 的第一及第二末端終端。在一具體實施例裡，該連接埠 272 係一單一末端之不平衡式連接埠，而該連接埠 274 為一接地終端。或另者，該連接埠 274 係一單一末端不平衡式連接埠，而該連接埠 272 係一接地終端。一電容器 276 係經耦接於該等不平衡式連接埠 272 及 274 之間。該電感器 270 及電容器 276 組成一第一 LC 共振器。一電感器 278 含有經耦接於平衡式連接埠 280 及 282 的第一及第二末端終端。一電容器 284 係經耦接於該等平衡式連接埠 280 及 282 之

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間。該電感器 278 及該電容器 284 組成一第二 LC 共振器。該電感器 270 係經設置在距該電感器 278 的距離 d6 處。一電感器 290 含有末端終端 292 及 294。一電容器 296 係經串列耦接於該電感器 290 的末端終端 292 及 294 之間。該等電感器 290 及電容器 296 組成一第三 LC 共振器。該電感器 290 重疊於該等電感器 270 及 278 而為垂直電氣隔離，並且具有平面區隔 d7、d8、d9 及 d10。該電感器 290 可相對該等電感器 270 及 278 而具有較大、較小或對稱值。

圖 8 所示電路佈置係經實作如一 RFIC，並且提供平衡-不平衡轉換器及濾波器功能，亦即按一小型形式因數的平衡式濾波器。該電路利用互相電感或磁性感應耦接而含有三個 LC 共振器。該等電感器 270、278 及 290 可具有一長方形、多邊形或圓形的形式或形狀，並經纏繞以產生磁性耦接。該等電容器 276 及 284 可對該平衡-不平衡轉換器提供 ESD 保護。該等電感器 270、278 及 290 係利用 8μm 像是 Al、Cu、Sn、Ni、Au 或 Ag 的導體材料所實作。該等電容器 276、284 及 296 是利用薄膜介電物所實作。該薄膜材料可提高電容密度。藉由利用跨於脆弱電容器上的電感分流保護，即可在該薄膜材料內獲致 ESD 強固性。在一 ESD 事件裡的大部份能量皆為集中於低頻率，而對此在奈米亨利範圍內的電感器為有效短路。在該磁性耦接電路中，各個電容器係由一低值分流電感器所保護，藉以增加對於 ESD 的強固性。

該等電感器 270 及 278 之間的互相電感或磁性耦接強

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度是由兩個線圈之間的距離 d6 所決定。同樣地，該等電感器 270 及 290 之間，以及該等電感器 278 及 290 之間，的磁性耦接強度是由兩個線圈之間的距離 d7、d8、d9 及 d10 所決定。在一具體實施例裡，該等距離 d6-d10 是被設定為 10μm。可調整該等經電容負載之電感環間的分隔以選定該等 BPF 參數，藉此諧調該磁性耦接。該等電容器 276、284 及 296 係經諧調以針對所要求之應用項目進行阻抗匹配。

該等不平衡式連接埠 272 及 274 以及平衡式連接埠 280 及 282 並不共享一共用 DC 參考。各個輸入及輸出可為單一末端或是差分方式運作。在要求平衡至不平衡轉換的應用項目中並不需要分別的平衡-不平衡轉換器。

圖 9 係一對於不同 d1 值，該平衡-不平衡轉換器 238 之插入損失相對於頻率的圖式。圖 10 係一對於不同 d2 值，該平衡-不平衡轉換器 238 之插入損失相對於頻率的圖式。圖 11 係一對於不同 d3 值，該平衡-不平衡轉換器 238 之插入損失相對於頻率的圖式。

雖既已詳細說明本發明之一或更多具體實施例，然熟諳本項技藝之人士將能瞭解確能對該等具體實施例進行修改及調適，而不致悖離如後載申請專利範圍之中所陳述的本發明範圍。

【圖式簡單說明】

圖 1 說明一 PCB，此者具有屬不同類型而經架置於其表面的封裝；

圖 2a-2c 說明經架置於該 PCB 之半導體封裝的進一步

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細節；

圖 3 說明一含有一整合式被動裝置的半導體封裝；

圖 4 說明一經耦接於一收發器的多通道 RF 信號處理電路；

圖 5 說明該多通道 RF 信號處理電路的佈置方式；

圖 6a-6c 為個別 RF 信號處理通道的略圖；

圖 7 說明複數個運用於一 RF 信號處理通道中之 LC 共振器；

圖 8 說明運用於一 RF 信號處理通道中之 LC 共振器的另一具體實施例；

圖 9 係對於該 LC 共振器之電感器間的不同距離 d1，插入損失相對於頻率的圖式；

圖 10 係對於該 LC 共振器之電感器間的不同距離 d2，插入損失相對於頻率的圖式；以及

圖 11 係對於該 LC 共振器之電感器間的不同距離 d3，插入損失相對於頻率的圖式。

【主要元件符號說明】

10	電子裝置
12	晶片載板/印刷電路板(PCB)
14	導體信號跡線
16	線路貼接封裝
18	覆晶片
20	球柵陣列(BGA)
22	凸塊晶片載體(BCC)

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24	雙線內封裝(DIP)
26	地柵陣列(LGA)
28	多晶片模組(MCM)
30	四方扁平無引腳封裝(QFN)
32	四方扁平封裝
34	半導體晶粒
36	接觸板
38	載體
40	導線
42	接線連附
44	密封物
46	焊燒材料
47	半導體晶粒
48	接觸板
50	底層填入/環氧樹脂黏著材料
52、64	接觸板
54	接線連附
56、58	連附板
60	模鑄化合物/密封物
66	凸塊
70	主動範圍
76	載體
78	導體焊燒凸塊/球體
80	凸塊板/互連處所

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82	接觸板/互連處所
84	凸塊板/互連處所
86	導體焊燒凸塊/球體
88	接觸板
90	導體線路
92	模鑄化合物/密封物
94	半導體晶粒/封裝
96	半導體基板
98	主動範圍
100	無線通訊系統
102	射頻(RF) IC
104-112	不平衡式連接埠
116	接地終端
118-136	平衡式連接埠
140	收發器
142	電容器
144、146	電感器
150	電容器
152	電阻器
154	直流(DC)電力匯流排
156	終端
160	電容器
162、164	電感器
166	電容器

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168	電阻器
170	電容器
172、174	電感器
176	電容器
178	電阻器
182、184	電容器
185	節點
186、188	電感器
190	電容器
191	節點
192	電容器
194、196	電感器
198、200	電容器
202	電阻器
210	電感器
212	節點
214、216	電容器
218	電感器
220	節點
222	電容器
224、226	電感器
228、230	電容器
232	電阻器
238	平衡-不平衡轉換器(Balun)

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240	電感器
242、244	不平衡式連接埠
246	電容器
248	電感器
250、252	平衡式連接埠
254	電容器
256	電感器
258、260	末端終端
262	電容器
268	平衡-不平衡轉換器(Balun)
270	電感器
272、274	不平衡式連接埠
276	電容器
278	電感器
280、282	平衡式連接埠
284	電容器
290	電感器
292、294	末端終端
296	電容器

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五、中文發明摘要：

一種帶通濾波器，其中具有複數個頻帶通道，各通道含有一第一電感器，此電感器的一第一終端係經耦接於一第一平衡式連接埠而一第二終端則經耦接於一第二平衡式連接埠。一第一電容器係經耦接於該第一電感器的第一及第二終端之間。一第二電感器具有一第一終端，此終端係經耦接於一第一不平衡式連接埠，以及一第二終端，此終端係經耦接於一第二不平衡式連接埠。該第二電感器係經設置在該第一電感器的一第一距離之內，藉以感應磁性耦接。一第二電容器係經耦接於該第二電感器的第一及第二終端之間。一第三電感器係經設置在該第一電感器的一第二距離之內以及該第二電感器的一第三距離之內，藉以感應磁性耦接。一第三電容器係經耦接於該第三電感器的第一及第二終端之間。

六、英文發明摘要：

A band-pass filter has a plurality of frequency band channels each including a first inductor having a first terminal coupled to a first balanced port and a second terminal coupled to a second balanced port. A first capacitor is coupled between the first and second terminals of the first inductor. A second inductor has a first terminal coupled to a first unbalanced port and a second terminal coupled to a second unbalanced port. The second inductor is

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disposed within a first distance of the first inductor to induce magnetic coupling. A second capacitor is coupled between the first and second terminals of the second inductor. A third inductor is disposed within a second distance of the first inductor and within a third distance of the second inductor to induce magnetic coupling. A third capacitor is coupled between first and second terminals of the third inductor.

十、申請專利範圍：

1.一種帶通濾波器，其中含有複數個頻帶通道，各通道含有一第一及第二平衡式連接埠以及第一及第二不平衡式連接埠，各頻帶通道含有：

一第一電感器，此者的一第一終端係經耦接於該第一平衡式連接埠，而一第二終端則經耦接於該第二平衡式連接埠；

一第一電容器，此者係經耦接於該第一電感器的第一及第二終端之間；

一第二電感器，此者具有一第一終端，此終端係經耦接於該第一不平衡式連接埠，以及一第二終端，此終端係經耦接於第二不平衡式連接埠，而該第二電感器係經設置在該第一電感器的一第一距離之內，藉以於該等第一與第二電感器之間感應磁性耦接；

一第二電容器，此者係經耦接於該第二電感器的第一及第二終端之間；

一第三電感器，此者係經設置在該第一電感器的一第二距離之內以及該第二電感器的一第三距離之內，藉以於該等第一、第二與第三電感器之間感應磁性耦接；以及

一第三電容器，此者係經耦接於該第三電感器的第一及第二終端之間。

2.如申請專利範圍第 1 項所述之帶通濾波器，其中該等第一、第二及第三電感器為薄膜導體材料，並且該等第一、第二及第三電容器為薄膜介電物。

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3.如申請專利範圍第 1 項所述之帶通濾波器，其中該等第一、第二及第三電感器具有長方形、多邊形或圓形形狀。

4.如申請專利範圍第 1 項所述之帶通濾波器，其中該等第一及第二電感器重疊於該第三電感器。

5.如申請專利範圍第 1 項所述之帶通濾波器，其中該第一電感器係經設置在鄰近於該第二電感器並與其非重疊，同時該第三電感器係經設置在該等第一及第二電感器週邊附近並與其等非重疊。

6.如申請專利範圍第 1 項所述之帶通濾波器，進一步包含一基板，其中該等第一、第二及第三電感器以及該等第一、第二及第三電容器係經整合於該基板上。

7.如申請專利範圍第 1 項所述之帶通濾波器，進一步包含一經耦接於該第二電感器的直流電力匯流排。

8.一種帶通濾波器，其中含有複數個 LC 共振器，各共振器具有一第一及第二平衡式連接埠以及第一及第二不平衡式連接埠，其中包含：

一第一電感器，此者具有一第一終端，此終端係經耦接於該第一平衡式連接埠，以及一第二終端，此終端係經耦接於該第二平衡式連接埠；

一第一電容器，此者係經耦接於該第一電感器的第一及第二終端之間；

一第二電感器，此者具有一第一終端，此終端係經耦接於該第一不平衡式連接埠，以及一第二終端，此終端係經耦接於該第二不平衡式連接埠；

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一第二電容器，此者係經耦接於該第二電感器的第一及第二終端之間；

一第三電感器，此者係經設置在鄰近於該等第一及第二電感器處，藉以於該等第一、第二與第三電感器之間感應磁性耦接；以及

一第三電容器，此者係經耦接於該第三電感器的第一及第二終端之間。

9.如申請專利範圍第 8 項所述之帶通濾波器，其中該第二電感器係經設置在該第一電感器的一第一距離內，藉以於該等第一與第二電感器之間感應磁性耦接。

10.如申請專利範圍第 8 項所述之帶通濾波器，其中該第三電感器係經設置在該第一電感器的一第二距離內並且在該第二電感器的一第三距離內，藉以於該等第一、第二與第三電感器之間感應磁性耦接。

11.如申請專利範圍第 8 項所述之帶通濾波器，其中該等第一、第二及第三電感器為薄膜導體材料，並且該等第一、第二及第三電容器為薄膜介電物。

12.如申請專利範圍第 8 項所述之帶通濾波器，其中該等第一及第二電感器重疊於該第三電感器。

13.如申請專利範圍第 8 項所述之帶通濾波器，其中該第一電感器係經設置在鄰近於該第二電感器並與其非重疊，同時該第三電感器係經設置在該等第一及第二電感器週邊附近並與其等非重疊。

14.如申請專利範圍第 8 項所述之帶通濾波器，進一步

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包含一基板，其中該等第一、第二及第三電感器以及該等第一、第二及第三電容器係經整合於該基板上。

15.一種 LC 共振器電路，其中包含：

一第一電感器，此者具有第一及第二終端；

一第一電容器，此者係經耦接於該第一電感器的第一及第二終端之間；

一第二電感器，此者具有第一及第二終端；

一第二電容器，此者係經耦接於該第二電感器的第一及第二終端之間；

一第三電感器，此者係經設置鄰近於該等第一及第二電感器，藉以於該等第一、第二及第三電感器之間感應磁性耦接；以及

一第三電容器，此者係經耦接於該第三電感器的第一及第二終端之間。

16.如申請專利範圍第 15 項所述之 LC 共振器電路，其中該第二電感器係經設置在該第一電感器的一第一距離內，藉以於該等第一與第二電感器之間感應磁性耦接。

17.如申請專利範圍第 15 項所述之 LC 共振器電路，其中該第三電感器係經設置在該第一電感器的一第二距離內並且在該第二電感器的一第三距離內，藉以於該等第一、第二與第三電感器之間感應磁性耦接。

18.如申請專利範圍第 15 項所述之 LC 共振器電路，其中該等第一及第二電感器重疊於該第三電感器。

19.如申請專利範圍第 15 項所述之 LC 共振器電路，其

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中該第一電感器係經設置在鄰近於該第二電感器並與其非重疊，同時該第三電感器係經設置在該等第一及第二電感器週邊附近並與其等非重疊。

20.如申請專利範圍第 15 項所述之 LC 共振器電路，進一步包含一基板，其中該等第一、第二及第三電感器以及該等第一、第二及第三電容器係經整合於該基板上。

21.一種積體電路封裝，其中承載有複數個 LC 共振器，並且具有第一、第二、第三及第四互連終端，其中包含：

一第一電感器，此者具有一第一終端，此終端係經耦接於該第一互連終端，以及一第二終端，此終端係經耦接於該第二互連終端；

一第一電容器，此者係經耦接於該第一電感器的第一及第二終端之間；

一第二電感器，此者具有一第一終端，此終端係經耦接於該第一互連終端，以及一第二終端，此終端係經耦接於該第二互連終端；

一第二電容器，此者係經耦接於該第二電感器的第一及第二終端之間；

一第三電感器，此者係經設置在鄰近於該等第一及第二電感器處，藉以於該等第一、第二與第三電感器之間感應磁性耦接；以及

一第三電容器，此者係經耦接於該第三電感器的第一及第二終端之間。

22.如申請專利範圍第 21 項所述之積體電路封裝，其中

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該第二電感器係經設置在該第一電感器的一第一距離內，藉以於該等第一與第二電感器之間感應磁性耦接。

23.如申請專利範圍第21項所述之積體電路封裝，其中該第三電感器係經設置在該第一電感器的一第二距離內並且在該第二電感器的一第三距離內，藉以於該等第一、第二與第三電感器之間感應磁性耦接。

24.如申請專利範圍第21項所述之積體電路封裝，其中該等第一及第二電感器重疊於該第三電感器。

25.如申請專利範圍第21項所述之積體電路封裝，其中該第一電感器係經設置在鄰近於該第二電感器並與其非重疊，同時該第三電感器係經設置在該等第一及第二電感器週邊附近並與其等非重疊。

十一、圖式：

如次頁

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該第二電感器係經設置在該第一電感器的一第一距離內，藉以於該等第一與第二電感器之間感應磁性耦接。

23.如申請專利範圍第21項所述之積體電路封裝，其中該第三電感器係經設置在該第一電感器的一第二距離內並且在該第二電感器的一第三距離內，藉以於該等第一、第二與第三電感器之間感應磁性耦接。

24.如申請專利範圍第21項所述之積體電路封裝，其中該等第一及第二電感器重疊於該第三電感器。

25.如申請專利範圍第21項所述之積體電路封裝，其中該第一電感器係經設置在鄰近於該第二電感器並與其非重疊，同時該第三電感器係經設置在該等第一及第二電感器週邊附近並與其等非重疊。

十一、圖式：

如次頁

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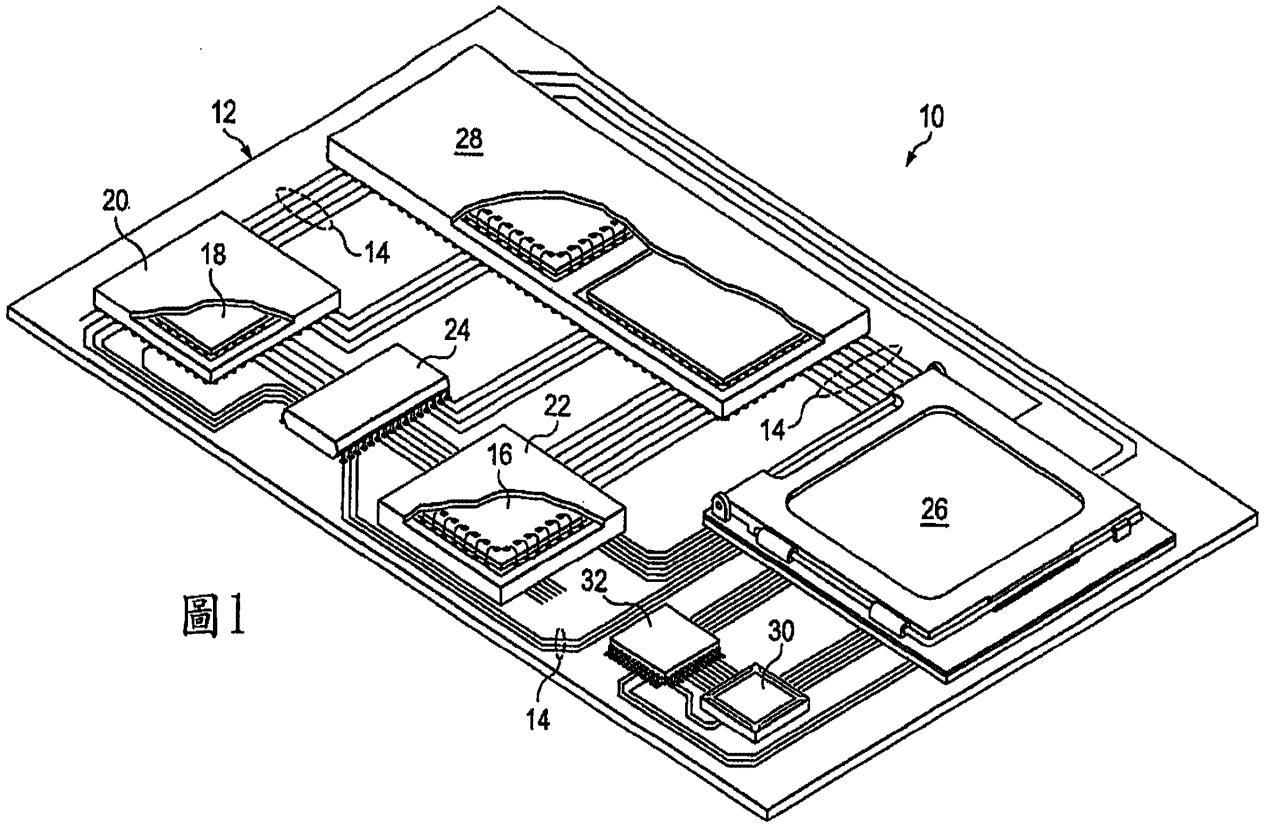


圖1

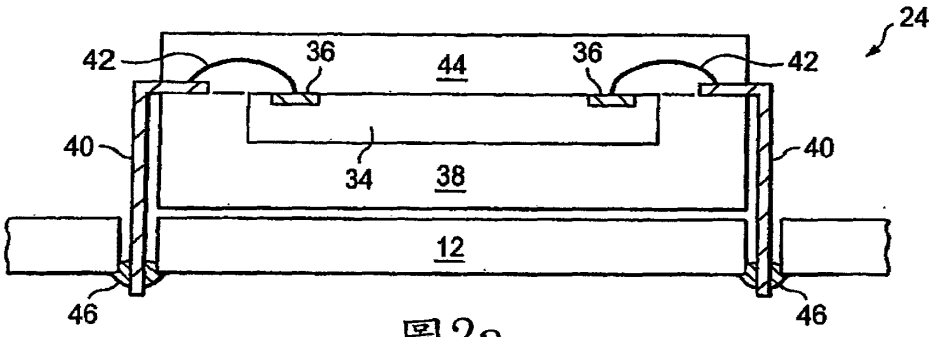

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圖2a

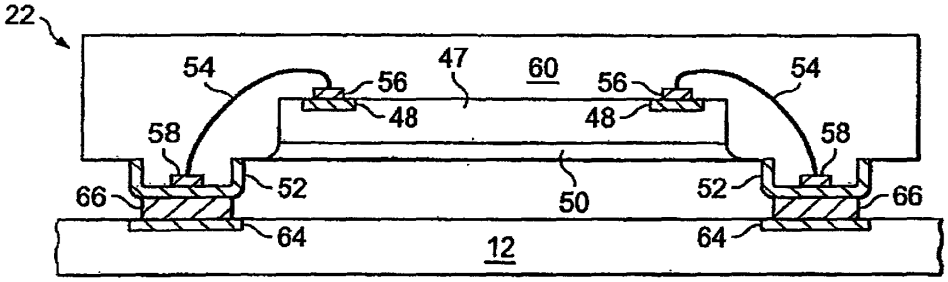

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12

圖2b

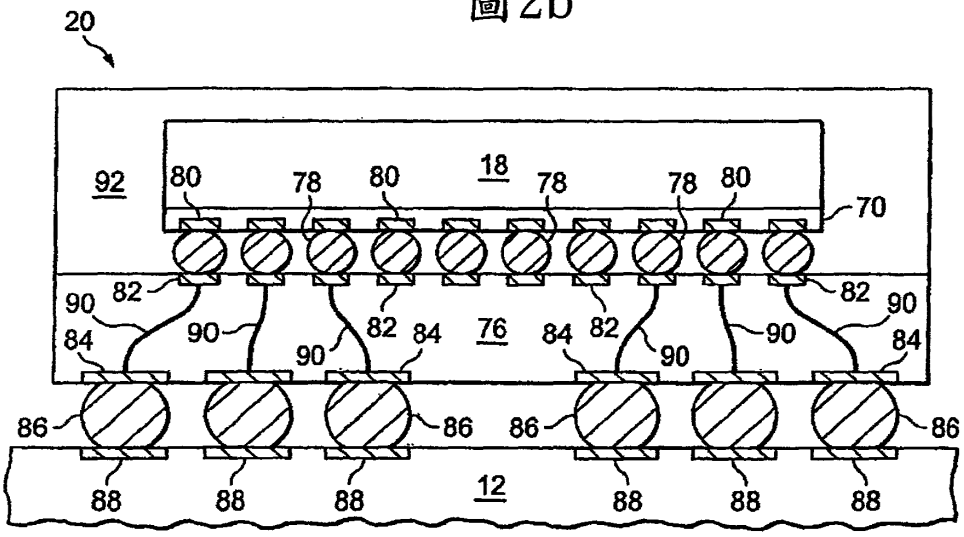

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88

圖2c

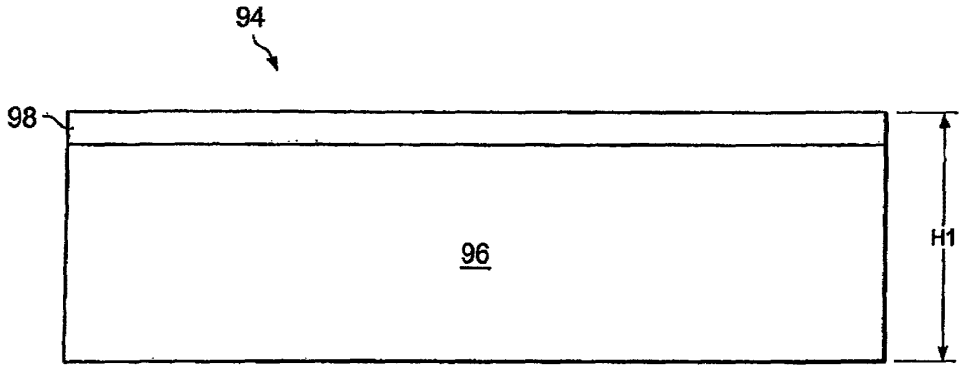

94
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96
H1

圖3

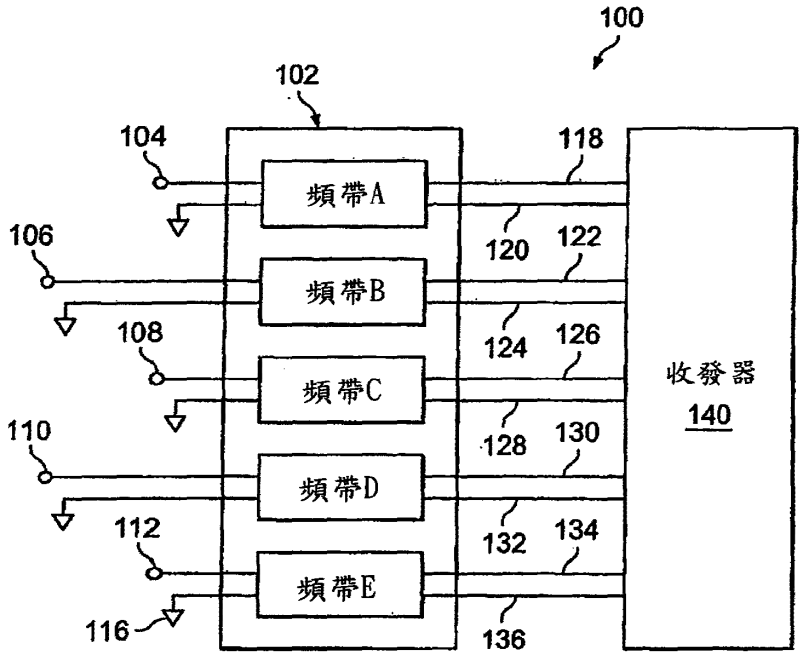

100
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136
頻帶A
頻帶B
頻帶C
頻帶D
頻帶E
收發器
140

圖4

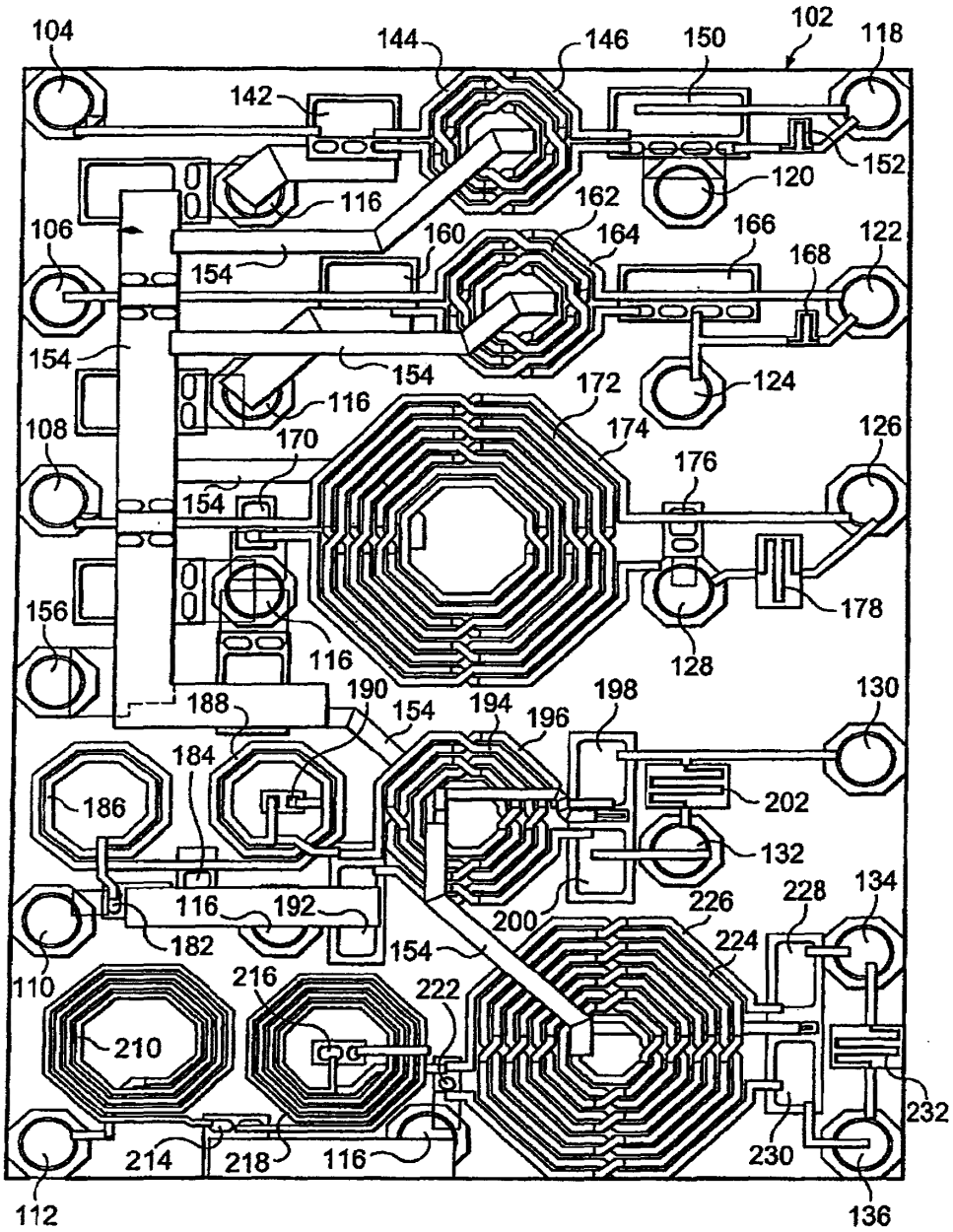

104
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186
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112
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圖5

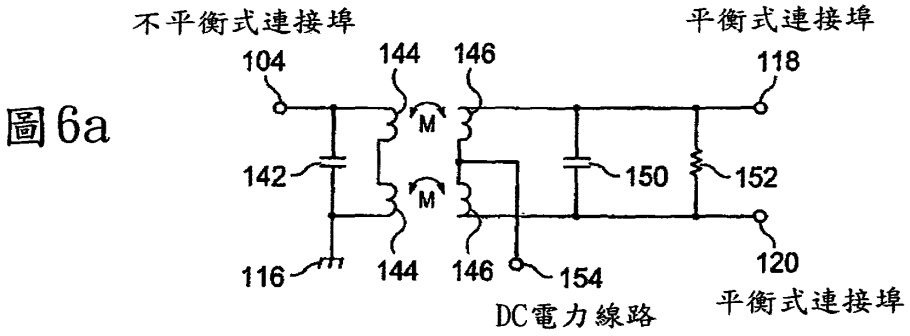

不平衡式連接埠
平衡式連接埠
104
144
146
118
M
142
150
152
M
116
144
146
154
120
DC電力線路
平衡式連接埠

圖6a

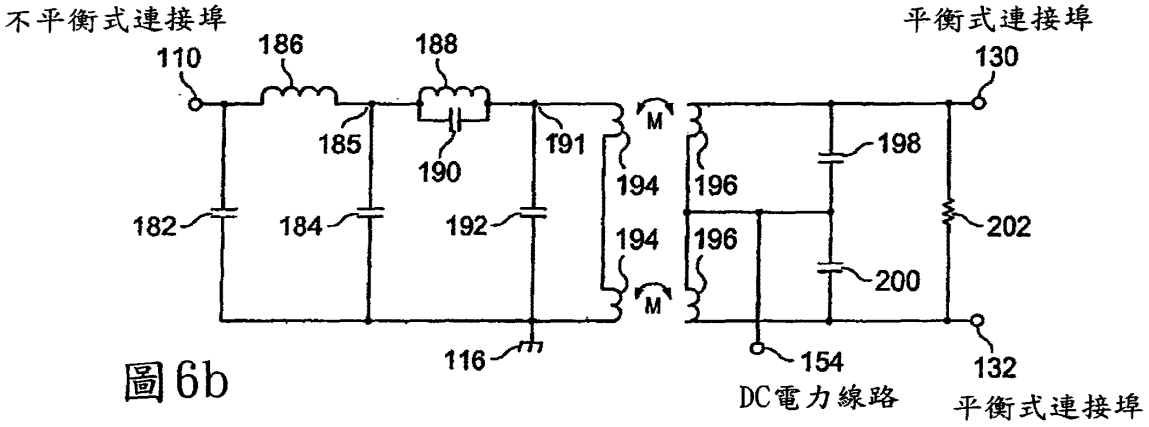

不平衡式連接埠
平衡式連接埠
110
186
188
130
185
190
191
M
194
196
198
182
184
192
194
196
202
200
M
116
154
132
DC電力線路
平衡式連接埠

圖6b

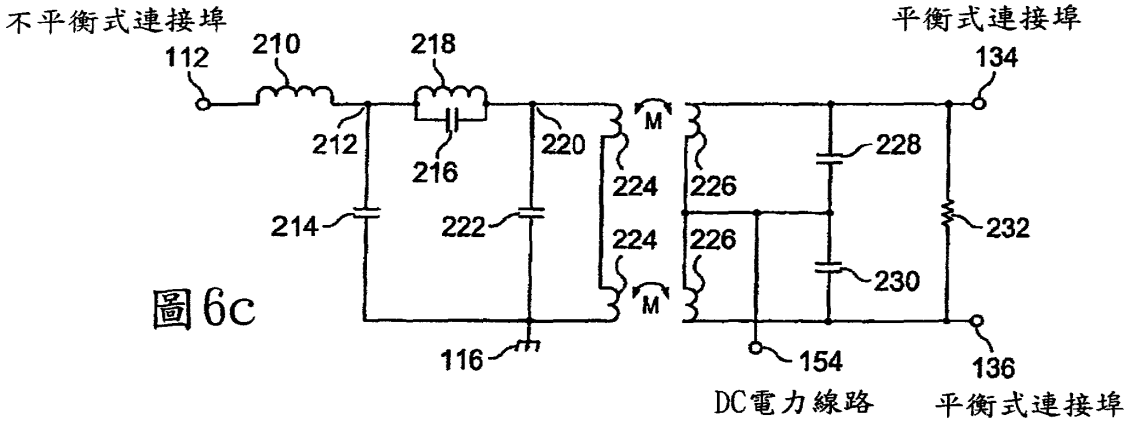

不平衡式連接埠
平衡式連接埠
112
210
218
134
212
216
220
M
224
226
228
214
222
224
226
232
230
M
116
154
136
DC電力線路
平衡式連接埠

圖6c

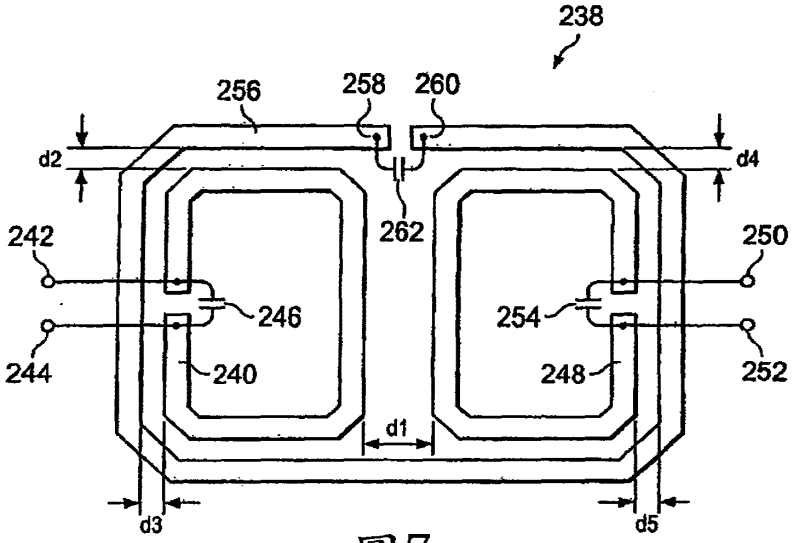

238
256
258
260
d2
d4
242
262
250
246
254
244
240
248
252
d1
d3
d5

圖7

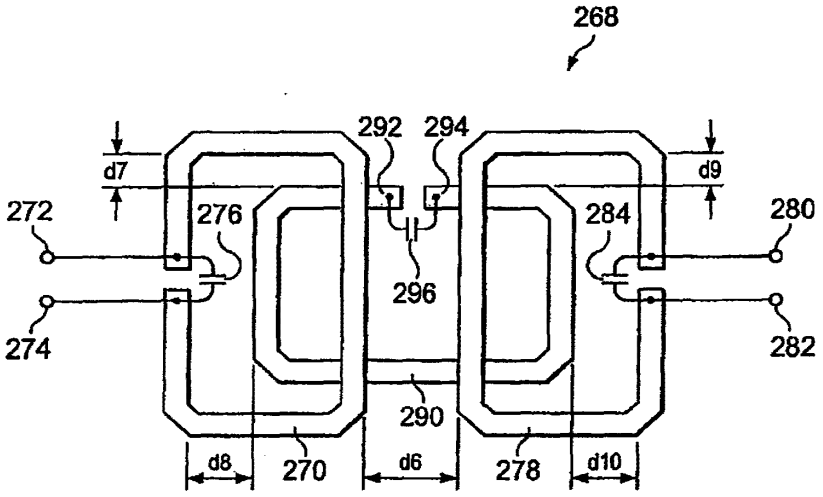

268
292
294
d7
d9
272
276
284
280
296
274
282
290
d8
270
d6
278
d10

圖8

圖9

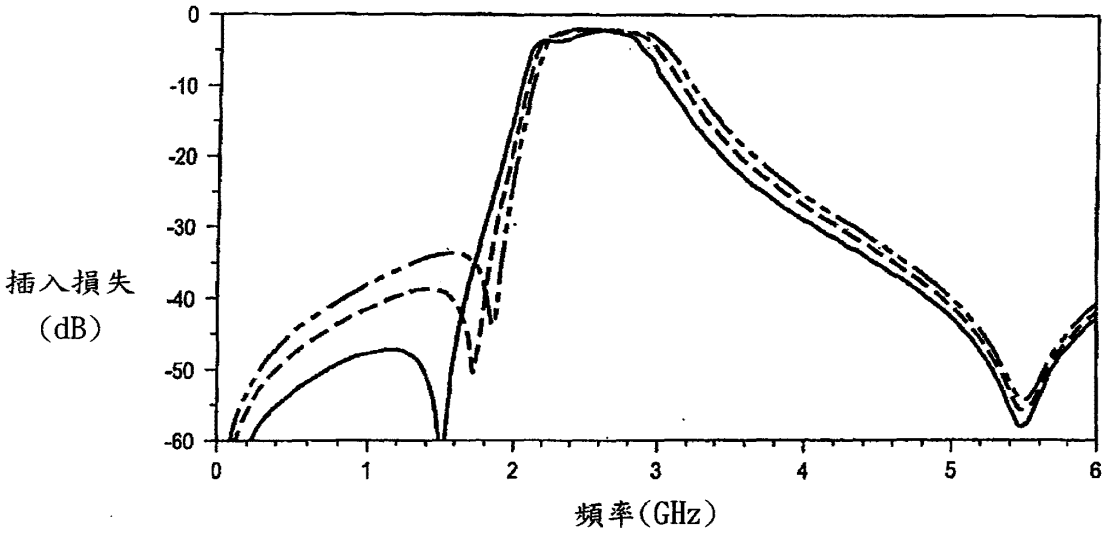

插入損失
(dB)
0
-10
-20
-30
-40
-50
-60
0
1
2
3
4
5
6
頻率(GHz)

圖10

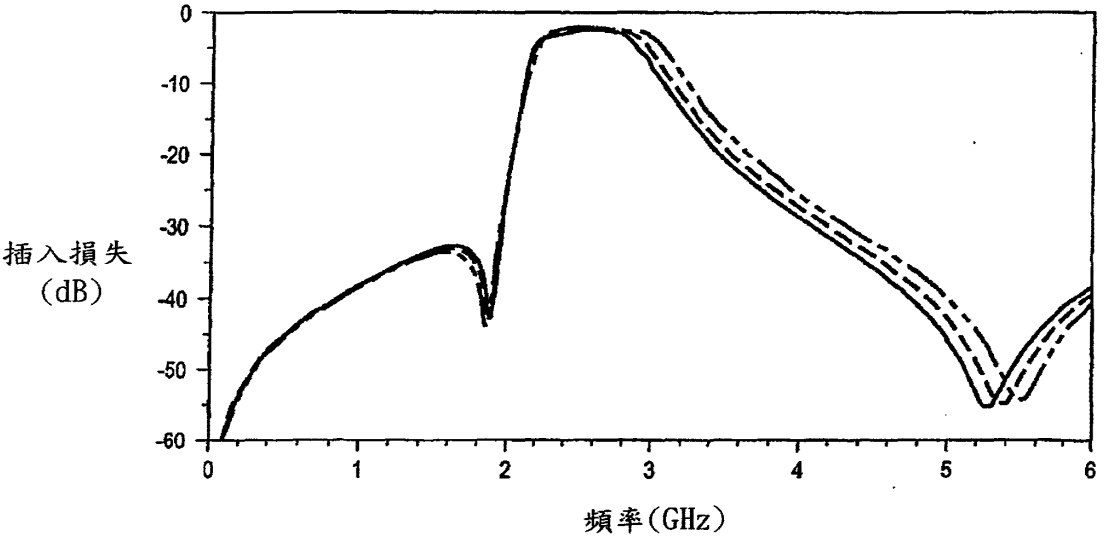
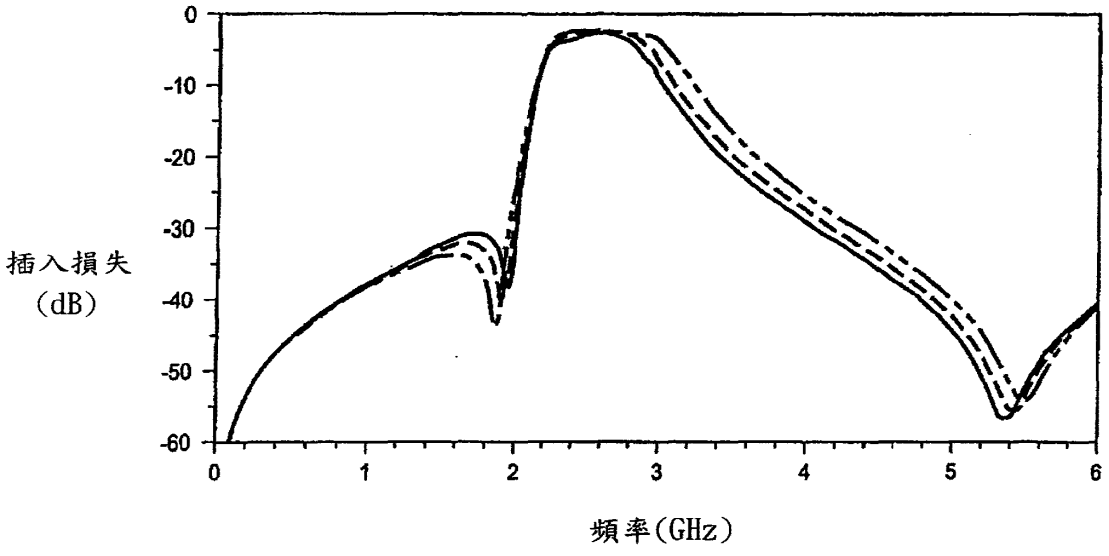

插入損失
(dB)
0
-10
-20
-30
-40
-50
-60
0
1
2
3
4
5
6
頻率(GHz)

圖11



七、指定代表圖：

(一)本案指定代表圖為：第（ 1 ）圖。

(二)本代表圖之元件符號簡單說明:

10	電子裝置
12	PCB
14	跡線
16	線路貼接封裝
18	覆晶片
20	球柵陣列
22	凸塊晶片載體
24	雙線內封裝
26	地柵陣列
28	晶片模組
30	方扁平無引腳封裝
32	方扁平封裝

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1002, p. 304 of 466

200943707

發明專利說明書

98年4月 修正補充

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※ 申請案號： 97148818

※ 申請日期： ※IPC 分類： H03H 7/01 (2006.01)
H03H 7/42 (2006.01)

一、發明名稱：（中文/英文）

具有以 LC 共振器執行平衡式帶通濾波器之半導體裝置

SEMICONDUCTOR DEVICE HAVING BALANCED BAND-PASS FILTER IMPLEMENTED WITH LC RESONATORS

二、申請人：（共 1 人）

姓名或名稱：（中文/英文）

史達晶片有限公司 / STATS ChipPAC, Ltd.

代表人：（中文/英文）

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新加坡 / SINGAPORE

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姓 名：（中文/英文）

1. 劉凱 / LIU, Kai
2. 羅勃特 C. 富萊 / FRYE, Robert C.
3. 林耀劍 / LIN, Yaojian

國 籍：（中文/英文）

1. 中國大陸 / China
2. 美國 / USA
3. 中國大陸 / China

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1002, p. 305 of 466

Electronic Acknowledgement Receipt	
EFS ID:	26101053
Application Number:	14338904
International Application Number:	
Confirmation Number:	1455
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Customer Number:	60601
Filer:	Joe McKinney Muncy/Anita Paka
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	5750/0265PUS1
Receipt Date:	17-JUN-2016
Filing Date:	23-JUL-2014
Time Stamp:	15:21:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-06-17-IDS.pdf	534221 e1d69442655542b150b41f4b7f6f392b93ae23cb	yes	4

	Multipart Description/PDF files in .zip description			
	Document Description	Start	End	
	Transmittal Letter	1	3	
	Information Disclosure Statement (IDS) Form (SB08)	4	4	
Warnings:				
Information:				
2		2016-06-17-Amendment-asfiled.pdf	713066 cd6fd4b96e72de14d480380a934185dead2bd923	yes	7

	Multipart Description/PDF files in .zip description			
	Document Description	Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1	
	Claims	2	4	
	Applicant Arguments/Remarks Made in an Amendment	5	7	
Warnings:				
Information:				
3	Other Reference-Patent/App/Search documents	TWOA.pdf	4225240 de6c53f4e1a91da017758136c0f32f8ec08bb884	no	4
Warnings:				
Information:				
4	Foreign Reference	TW201206059.pdf	1917087 abc15f31d4695987dc4045fdfc9c3550b470b7a9	no	40
Warnings:				
Information:				
5	Foreign Reference	TW201003883.pdf	5140272 dff9bb4839e570454de15dedabefcbaa6a158e62	no	111
Warnings:				
Information:				
6	Foreign Reference	TW201232579.pdf	1380180 d093b5cf5f218fcd8239e04e5314cf03891871cb	no	30
Warnings:				
Information:				

7	Foreign Reference	TW200943707.pdf	2377263 bc56adcea2fa2a5d9e6319ded25cdfba6b7e50e6	no	49

Warnings:	
Information:	
Total Files Size (in bytes):	16287329

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: YEN, Hsiao-Tsung Application No.: 14/338,904 Filed: 23 Jul 2014 Title: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT Attorney Docket No.: 5750/0265PUS1	Examiner: PATEL, Rakesh Bhaskarbhai Art Unit: 2842 Confirmation Number: 1455

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This Information Disclosure Statement is submitted:

☐ under 37 CFR 1.97(b), or
(within three months of filing national application or date of entry of international application; before mailing date of first office action on the merits; or before the mailing of a first Office action after the filing of a request for continued examination)

☒ under 37 CFR 1.97(c) together with either a:
- ☒ statement under 37 CFR 1.97(e), **or**
- ☐ a $180.00 (large entity) or $90 (small entity) fee under 37 CFR 1.17(p),

(after the CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
- ☐ statement under 37 CFR 1.97(e), **and**
- ☐ a $180.00 (large entity) or $90 (small entity) set forth in 37 CFR 1.17(p).

(filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Statement under 37 CFR 1.97(e) (if applicable):

☒ Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement (37 CFR 1.97(e)(1)).

☐ No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the information disclosure statement (37 CFR 1.97(e)(2)).

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the PTO/SB/08 attached hereto.

II. COPIES (check at least one box)

a. ☒ Submitted herewith is a legible copy of (i) each foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.

b. ☐ Submitted herewith is a legible copy of the International Search Report and each foreign patent or publication cited therein.

c. ☐ Some or all of the documents listed on the PTO/SB/08 are not enclosed because they are either U.S. Patents or Published Applications.

d. ☐ As provided in 37 CFR 1.98(d), some or all of the documents listed on the PTO/SB/08 are not enclosed because they were cited in the parent application(s). Accordingly, copies are not submitted herewith.

III. CONCISE EXPLANATION OF THE RELEVANCE
(check at least one box)

a. ☐ DOCUMENTS IN THE ENGLISH LANGUAGE
The attached patents, publications, or other information in the English language do not require a statement of relevancy.

b. ☒ DOCUMENTS NOT IN THE ENGLISH LANGUAGE
A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

An English language abstract is attached to all foreign language documents.

c. ☐ ENGLISH LANGUAGE SEARCH REPORT
An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609.04(a)(III), *"Where the information listed is not in the English language, but was cited in a search report or other action by a foreign patent office in a counterpart foreign application, the requirement for a concise explanation of relevance can be satisfied by submitting an English-language version of the search report or action which indicates the degree of relevance found by the foreign office. This may be an explanation of which portion of the reference is particularly relevant, to which claims it applies, or merely an "X", "Y", or "A" indication on a search report."*

d. ☒ OTHER
The following additional information is provided for the Examiner's consideration.
Office action dated 17 Mar 2016 issued in corresponding TW patent application no. 103113947 (4 pgs).

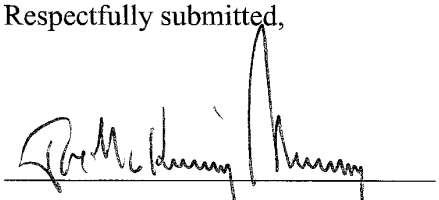
If the Examiner has any questions concerning this Information Disclosure Statement, he/she is requested to contact the undersigned. If it is determined that this Information Disclosure Statement has been filed under the wrong rule, the U.S. Patent and Trademark Office is requested to consider this Information Disclosure Statement under the proper rule and charge the appropriate fee to Deposit Account No. **50-3828**.

It is requested that the information disclosed herein be made of record in this application. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account **50-3828** and please credit any excess fees to such deposit account.

Date: June 17, 2016

Respectfully submitted,

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road, Suite 310
Fairfax, VA 22033
Tel. 703.621.7140
mailroom@mg-ip.com



Joe McKinney Muncy
Attorney/Agent for Applicant(s)
Reg. No. 32334

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	14/338,904
Filing Date	Jul 23, 2014
First Named Inventor	YEN, Hsiao-Tsung
Art Unit	2842
Examiner Name	PATEL, Rakesh Bhaskarbhai
Attorney Docket Number	5750/0265PUS1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
		TW 201206059 A1	02/01/2012	STATS ChipPAC, Ltd.		X
		TW 201003883 A1	01/16/2010	Int'l Business Machines Corp.		X
		TW 201232579 A1	08/01/2012	Nat'l Taiwan Univ. of Sci. and Tech.		X
		TW 200943707	10/16/2009	STATS ChipPAC, Ltd.		X

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional).[2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.[3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).[4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.[6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/338,904	Filing Date 07/23/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	280
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	600
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1600

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	06/17/2016	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/KATINA TOBIN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

60601 7590 03/18/2016

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER	
PATEL, RAKESH BHASKARBHAI	

ART UNIT	PAPER NUMBER
2842	

MAIL DATE	DELIVERY MODE
03/18/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/338,904	Applicant(s) YEN ET AL.	
	Examiner RAKESH PATEL	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/30/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-4 and 6-10* is/are rejected.

8)☒ Claim(s) *5* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. In the amendment dated 12/30/2015, the following has occurred: Claims 1-2, 4-6, and 9-10 have been amended.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-10 are pending.

Claim Objections

6. **Claims 5 and 7 are objected to because of the following informalities:**

On line 3 of claim 5, --in a vertical direction—should be inserted after "respectively" to avoid potential 112 issues and to make it clear how the "connecting segments" are overlapped with "the two extension-conductor segments".

On line 2 of claim 7, "-coil-conductor" should be changed to --coil-conductor-- for grammatical purposes.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Daley et al. US 2009/0322447 (of record).

As per claims 1-4 and 6-10, Daley et al. discloses in Figs. 1-2, 2a-2b, and 3 **a semiconductor device with an LC resonant circuit** (Fig. 1, BEOL wiring structure 10; As stated in Paragraph 2, structure 10 is a semiconductor device. As stated in Paragraph 33 lines 6-8, terminals 56, 58 (i.e. Fig. 1) are coupled with ports 25, 35 (i.e. Fig. 2) to form an LC resonator.)**, comprising:**

as per claims 1, 9, and 10, **a first insulation layer** (Fig. 2a, dielectric layer 18)**; an inductor component** (Fig. 1, on-chip inductor 20) **comprising a coil-conductor segment** (Figs. 1-2a, signal lines 50 and 52) **located on a surface of the first insulation layer** (Fig. 2a; As shown, signal lines 50 and 52 are located on a top surface of dielectric layer 18.)**, and two extension-conductor segments located on the surface of the first insulator layer** (Annotated Fig. 1 below, the conductor segments annotated as A)**, coupled to two ends of the coil-conductor segment respectively** (Annotated Fig. 1 below, the ends annotated as B of signal line 50)**, arranged at an interval, and extending outwards relative to the coil-conductor segment** (Annotated Fig. 1 below; The conductor segments annotated as A are arranged at a distance apart (i.e., an interval) from one another and extend outward from the respective ends annotated as B.)**, wherein a first region is defined between the two extension-conductor segments and the coil-conductor segments** (Fig. 1, the enclosed circular area within inductor 20)**; and a capacitor component** (Fig. 1, on-chip capacitor 16)**, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer** (Fig. 2a; Capacitor 16 is embedded within wiring structure 10 directly below the "first region" on the opposite surface (i.e. bottom surface) of dielectric 18.)**, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment** (Annotated Fig. 1 below; As shown, each of four corners of capacitor 16 all extend outwards in respective directions annotated as W-Z from signal lines 50 and 52.)**;**

as per claims 2, 3, and 8, **a second insulation layer** (Fig. 2a, dielectric layer 12)**, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer** (Fig. 2a; Capacitor 16 is sandwiched between dielectric layers 18 and 12.)**; and a transistor component** (Paragraph 23

and Fig. 2a, field effect transistor 22a) **arranged corresponding to the first region in an embedded manner on the other surface, opposite to the capacitor component, of the second insulating layer** (Fig. 2a; FET 22a is disposed on an opposite surface (i.e. bottom surface) of dielectric layer 12 which is opposite to a top surface of dielectric 12 that faces capacitor 16.)**;**

as per claims 4 and 6, **a tap segment** ("Tap" is defined as an electrical connection made to some point between the end terminals of a component. Vias 48 in Fig. 2 are "tap segments" disposed between input/outputs 25 and 35.)**, electrically connected to the coil-conductor segment; wherein the capacitor component comprises a plurality of connecting segments** (Fig. 2, conductive bars 26 and 28)**, extending corresponding to the two extension-conductor segments in a same direction** (As shown in the annotated Fig. 1 below, conductive bars 26 and 28 (not labeled) which are disposed on the left and right sides of capacitor 16 extend along the line annotated as C, which is the same line direction as which the extension-conductor segments annotated as A extend along.)**; and a plurality of electrode segments** (Fig. 2, electrodes 30 and 32) **located below the first region** (Fig. 1; Electrodes 30 and 32 in Fig. 2 are portions of capacitor 16 which is disposed underneath the enclosed circular area region within inductor 20.)**, wherein one end of each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments** (Paragraph 24 and Fig. 2; Electrodes 30 are directly connected with conductive bars 26 and electrodes 32 are directly connected with conductive tab 28. Each of the electrodes has an end that extends laterally or "toward" the side with the other conductive bar that the respective electrode is not connected to.)**; and**

as per claim 7, **wherein the coil-conductor segment has a pair of staggered parts** (Annotated Fig. 1 below; "Stagger" is defined as a cross-over section of the "coil-conductor segment" based on Fig. 9 and page 14 lines 18-20 of the instant specification. A portion of an outermost loop of the signal lines "crosses over" and connects with a portion of an inner loop of the signal lines within the sections annotated as D and E when viewing the structure in a vertical direction. Thus, signal lines 50 and 52 have a pair of crossover sections or

"staggered parts" annotated as D and E.)**, a second region is defined by outer sides of the pair of staggered parts** (Annotated Fig. 1 below; Left and right sides of each of the sections annotated as D and E necessarily form "a second portion" of the coil-conductor segment.)**.**

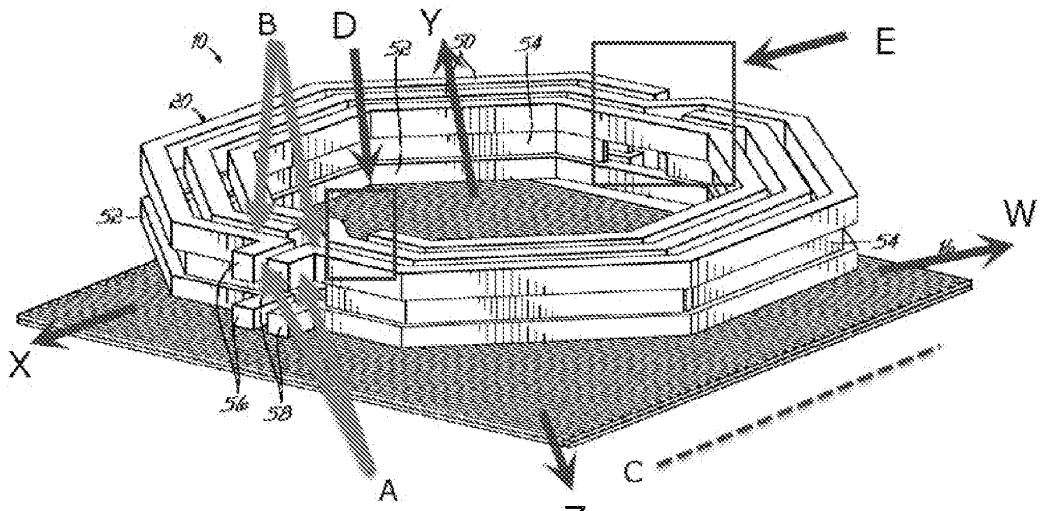


FIG. 1

Allowable Subject Matter

7. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. The Examiner agrees with the Applicant's arguments pertaining to the rejection of claim 7 under 35 USC 112 and thus the rejection has been withdrawn despite no amendment made to claim 7. Because the Examiner is now interpreting the limitation "a pair of staggered parts" in claim 7 differently from the previous interpretation made in the Office action dated 9/30/2015, this Office action has not been made final. However, Applicant's arguments pertaining to the rejections made to claims 1-4 and 6-10 are not persuasive.

The Applicant states that Daley does not teach "the capacitor component is correspondingly configured outwards relative to the coil-conductor segment". That is, the capacitor component is substantially un-

overlapped with the coil-conductor segment. The Examiner respectfully disagrees with the Applicant. As shown in the annotated Fig. 1 above, the four corners of capacitor 16 extend outwards from a perimeter of signal lines 50 and 52 in the directions annotated as W-Z. Thus, "the capacitor component" 16 is configured "outwards" relative to the “coil-conductor segment” 50 and 52. Further, whether or not the capacitor component is un-overlapped with the coil-conductor segment is true, this limitation is not commensurate with the claimed language in claim 1 and thus the related Applicant’s arguments are not germane. Claims 1-4 and 6-10 have been repeated and sustained above with a new interpretation of "pair of staggered parts" as described above.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAKESH PATEL whose telephone number is (571)272-0961. The examiner can normally be reached on Monday-Friday 7:30 am-5:00 pm ET, ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Robert J. Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. P./
Examiner, Art Unit 2842

/ROBERT PASCAL/
Supervisory Patent Examiner, Art Unit 2842

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/18/2015	03/07/2016							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	O							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

CPC- SEARCHED		
Symbol	Date	Examiner
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	9/18/2015	RP
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	3/7/2016	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
333	175,177,185	9/18/2015	RP
336	200	9/18/2015	RP
333	175,177,185	3/7/2016	RP
336	200	3/7/2016	RP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Text Search	9/18/2015	RP
EAST Updated Text Search	3/7/2016	RP
Consulted Examiner, Gerald Stevens	3/7/2016	RP
Inventor Search	3/7/2016	RP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/R.P./ Examiner.Art Unit 2842	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	1	L9 and (semiconductor and LC).clm.	US-PGPUB; USPAT	OR	ON	2016/03/07 14:13
L9	271	(Hsiao with Yen) or (sheng with jean) or (hsun with yeh)	US-PGPUB; USPAT	OR	ON	2016/03/07 14:13
L8	1110	(L1 or L2 or L3 or L4 or L5 or L6 or L7) and semiconductor and (LC or resona$4)	US-PGPUB; USPAT	OR	ON	2016/03/07 14:12
L7	3683	(336/200).ccls.	US-PGPUB; USPAT	OR	ON	2016/03/07 14:11
L6	2486	(333/175,177,185).ccls.	US-PGPUB; USPAT	OR	ON	2016/03/07 14:11
L5	1807	(H01F17/0013).cpc.	US-PGPUB; USPAT	OR	ON	2016/03/07 14:11
L4	440	(H01F2027/2809).cpc.	US-PGPUB; USPAT	OR	ON	2016/03/07 14:11
L3	1549	(H01F27/2804).cpc.	US-PGPUB; USPAT	OR	ON	2016/03/07 14:11
L2	1108	(H03H7/0115).cpc.	US-PGPUB; USPAT	OR	ON	2016/03/07 14:11
L1	1	("7,418,251").PN.	US-PGPUB; USPAT	OR	OFF	2016/03/07 12:11

3/7/2016 2:13:59 PM
C:\Users\rpatel9\Documents\EAST\Workspaces\14338904.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: YEN, Hsiao-Tsung Application No.: 14/338,904 Filed: 23 Jul 2014 Title: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT Attorney Docket No.: 5750/0265PUS1	Examiner: PATEL, Rakesh Bhaskarbhai Art Unit: 2842 Confirmation Number: 1455

MS AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Dear Sir:

In response to the Office Action of 30 Sep 2015, the following are provided:

Amendments to the Claims; and

Remarks.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer,

wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment.

2. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

an electronic component, arranged corresponding to the first region in an embedded manner on ~~the other~~ a surface, opposite to the capacitor component, of the second insulation layer.

3. (Original) The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

4. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 1, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

5. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 4, wherein the plurality of connecting segments are overlapped with the two extension-conductor segments, respectively.

6. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a tap segment, electrically connected to the coil-conductor segment;

wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein one of the plurality of connecting segments is located below the tap segment and overlapped with the tap segment; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

7. (Original) The semiconductor device with an LC resonant circuit according to claim 1, wherein the -coil-conductor segment has a pair of staggered parts, a second region is defined by outer sides of the pair of staggered parts, and the semiconductor device further comprises:

an electronic component, arranged corresponding to the second region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

8. (Original) The semiconductor device with an LC resonant circuit according to claim 7, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

9. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

10. (Currently Amended) The semiconductor device with an LC resonant circuit according to claim 9, wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment.

REMARKS

Claims 1-10 remain present in this application.

Claims 1, 2, 4-6, 9 and 10 have been amended. Favorable consideration of the application, as amended, is respectfully requested.

Entry of Amendments

It is respectfully submitted that the foregoing amendments do not contain new matter. As such, the Examiner is respectfully requested to enter the same.

Objections to the Claims

The claims stand objected to for certain informalities. In view of the foregoing amendments, it is respectfully submitted that these informalities have been addressed. Reconsideration and withdrawal of any objection to the claims are respectfully requested.

Rejections under 35 USC 112

Claims 1-10 stand rejected under 35 USC 112(b). This rejection is respectfully traversed.

Applicants have amended claims 2 and 4 to address the informalities identified by the Examiner.

Regarding claim 7, Applicants submit that it is not necessary to amend the claims. That is, the specification discloses:

> "**the coil-conductor segment 131 includes** a plurality of semi-loop lines L1, L2, L3, and L4 and **at least one pair of staggered parts.** The illustration is provided below by using an example of two turns. The semi-loop lines L1, L2, L3, and L4 may be distinguished to be two first semi-loop lines L1 and L3 and two second semi-loop lines L2 and L4, and **each pair of staggered parts have two staggered guide lines L5 and L6**." (See application at page 14, lines 14-20).

Therefore, the meaning of the phrase "the coil-conductor segment has a pair of staggered parts" recited in claim 7 is clear from the specification, above, and Figure 9.

Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Rejections under 35 USC 102

Claims 1-4 and 6-10 stand rejected under 35 USC 102(a)(1) as being anticipated by Daley, et al. (U.S. Patent Application Publication No. 2009/0322447; hereinafter "Daley"). This rejection is respectfully traversed.

Daley discloses:

> "The on-chip capacitor 16 and the on-chip inductor 20 are arranged laterally within the respective metallization levels and in approximate vertical alignment such that the on-chip capacitor 16 is disposed between the on-chip inductor 20 and the substrate 24. Specifically, **the outermost edges of the on-chip capacitor 16**, such as representative edges 90, 92 respectively visible in FIGS. 2A and 2B, are approximately aligned, **when viewed in a vertical direction, with the outermost edges of the on-chip inductor 20**, such as representative edges 94, 96 respectively visible in FIGS. 2A and 2B. In the representative embodiment, **the on-chip capacitor 16 effectively operates as a Faraday shield** to enhance the inductor quality by increasing the quality factor, Q, of the on-chip inductor 20 and to **provide isolation between the active devices 22 a, 22 b on substrate 24 and the on-chip inductor 20**."

In Daley, the capacitor 16 covers the whole of the inductor 20. Furthermore, in order to operate as a Faraday shield and provide the isolation, **the capacitor 16 of Daley must be overlapped with the coil-conductor segment of the inductor 20 of Daley.**

The specification of the present application discloses:

> "in the semiconductor device with an LC resonant circuit according to the present invention, an LC resonant circuit may be integrated on a semiconductor substrate by means of a 3D die stacking technology, and a resonant capacitor is arranged corresponding to an input/output part of an inductor component, so as to ***reduce generation of phase noise, arrangement of interconnecting wires, and an overall size***. In some embodiments, in the semiconductor device with an LC resonant circuit according to the present invention, other electronic components are arranged corresponding to the input/out part or a staggered part of the inductor component, so as to further ***reduce generation of phase noise, arrangement of interconnecting wires, parasitic RLC (Resistance-Inductance- Capacitance) and an overall size***."

Claim 1 recites "***a first region is defined by the two extension-conductor segments and the coil-conductor segment***" "a capacitor component, ***arranged corresponding to the first region***" and "the capacitor component is correspondingly configured ***outwards relative to the coil-conductor segment***."

That is, in exemplary embodiments of the present invention, the capacitor component is substantially un-overlapped with the coil-conductor segment.

Therefore, Daley fails to teach or suggest, "***a first region is defined by the two extension-conductor segments and the coil-conductor segment***" "*a capacitor component,* ***arranged corresponding to the first region***" and "*the capacitor component is correspondingly configured* ***outwards relative to the coil-conductor segment***," as recited in claim 1.

Therefore, Daley fails to teach or suggest each and every feature of the claimed invention. Accordingly, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Allowable Subject Matter

Applicants gratefully acknowledge that the Examiner considers claim 5 to contain allowable subject matter. In view of the foregoing amendments and/or remarks, it is respectfully submitted that all claims should be fully in condition for allowance.

Conclusion

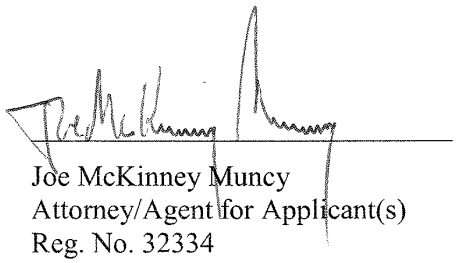
Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require action, it is respectfully requested that the Examiner telephone Joe McKinney Muncy, Applicants' Attorney, at 703.621.7140 so that such issues may be resolved as expeditiously as possible.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; in particular, extension of time fees.

Date: December 30, 2015

Respectfully submitted,



Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road, Suite 310
Fairfax, VA 22033
Tel. 703.621.7140
mailroom@mg-ip.com

Joe McKinney Muncy
Attorney/Agent for Applicant(s)
Reg. No. 32334

Electronic Acknowledgement Receipt

EFS ID:	24493848
Application Number:	14338904
International Application Number:	
Confirmation Number:	1455
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Customer Number:	60601
Filer:	Joe McKinney Muncy/Jonathan Goosens
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	5750/0265PUS1
Receipt Date:	30-DEC-2015
Filing Date:	23-JUL-2014
Time Stamp:	15:26:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2015-12-30-Amendment.pdf	366251 647d64f5ad3d4fe7c4f73327b4f9f39bcf7197f8	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	7
Warnings:			
Information:			
	Total Files Size (in bytes):	366251	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Claims 1-10 remain present in this application.

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Conclusion

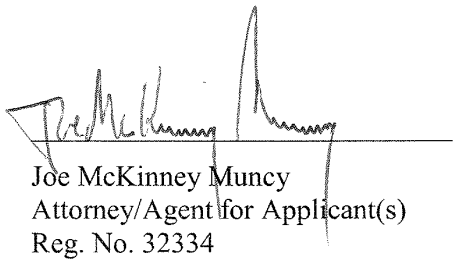
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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; in particular, extension of time fees.

Date: December 30, 2015

Respectfully submitted,



Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road, Suite 310
Fairfax, VA 22033
Tel. 703.621.7140
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Reg. No. 32334

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/338,904	Filing Date 07/23/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/30/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CAROLYN THOMAS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1

CONFIRMATION NO. 1455

60601
Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

PUBLICATION NOTICE



Title:SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

Publication No.US-2015-0303888-A1
Publication Date:10/22/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/338,904	07/23/2014	Hsiao-Tsung YEN	5750/0265PUS1	1455

60601 7590 09/30/2015

Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

EXAMINER	
PATEL, RAKESH BHASKARBHAI	

ART UNIT	PAPER NUMBER
2842	

MAIL DATE	DELIVERY MODE
09/30/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/338,904	Applicant(s) YEN ET AL.	
	Examiner RAKESH PATEL	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *7/23/2014* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☒ All b)☐ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *7/23/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. Claims 1-10 are pending.

Priority

4. Receipt is acknowledged of certified copies of papers required by 37 CFR 1.55.

Claim Objections

5. Claims 1 and 4-6 are objected to because of the following informalities:

On line 9 of claim 1 and line 3 of claim 4, the Examiner suggests inserting --two-- before each occurrence of "extension-conductor" to be consistent with the same limitation recited previously on line 6 of claim 1.

The Examiner suggests making the following changes to be consistent with the same limitation recited previously on line 5 of claim 4 and line 8 of claim 6 respectively: On lines 6 and 7 respectively of claim 4, insert --plurality of-- before each occurrence of “electrode". On lines 9-10 of claim 6, change "electrode segment extends" to --plurality of electrode segments extend--.

On line 2 of claim 5 and line 6 of claim 6, the Examiner suggests inserting --plurality of-- before each occurrence of “connecting segments” to be consistent with the same limitation recited previously on line 3 of claim 4 and line 5 of claim 6 respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of 35 U.S.C. 112(b):

(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

7. The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-10 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 2 recites the limitation "the other surface" in line 6. There is insufficient antecedent basis for this limitation in the claim.

On the last line of claim 4, the Applicant recites "the coupled connecting segment". However, it is unclear to the Examiner as to which "coupled connecting segment" the Applicant is referring to be (i.e. The coupled connecting segment of which one of the plurality of connecting segments"?). The Examiner construes that the Applicant is referring to the respective coupled connecting segment of each of the plurality of electrode segments.

On line 2 of claim 7, the Applicant recites "the coil-conductor segment has a pair of staggered parts". However, Fig. 3 of the drawings and the description on page 8 lines 11-13 of the instant specification shows that it is actually the capacitor component 150 that comprises staggered parts 155 and 156. There is no disclosure or description associated with the coil-conductor segment having a pair of staggered parts. Because of the inconsistency between the claimed limitation and the specification, claim 7 is construed to be vague and indefinite. For examination purposes, the Examiner construes that the capacitor component has a pair of staggered parts.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

10. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Daley et al. US 2009/0322447.

As per claims 1-4 and 6-10, Daley et al. discloses in Figs. 1-2, 2a-2b, and 3 **a semiconductor device with an LC resonant circuit** (Fig. 1, BEOL wiring structure 10; As stated in Paragraph 2, structure 10 is a semiconductor device. As stated in Paragraph 33 lines 6-8, terminals 56, 58 (i.e. Fig. 1) are coupled with ports 25, 35 (i.e. Fig. 2) to form an LC resonator.)**, comprising:**

as per claims 1, 9, and 10, **a first insulation layer** (Fig. 2a, dielectric layer 18)**; an inductor component** (Fig. 1, on-chip inductor 20) **comprising a coil-conductor segment** (Figs. 1-2a, signal lines 50 and 52) **located on a surface of the first insulation layer** (Fig. 2a; As shown, signal lines 50 and 52 are located on a top surface of dielectric layer 18.)**, and two extension-conductor segments located on the surface of the first insulator layer** (Annotated Fig. 1 below, the conductor segments annotated as A)**, coupled to two ends of the coil-conductor segment respectively** (Annotated Fig. 1 below, the ends annotated as B of signal line 50)**, arranged at an interval, and extending outwards relative to the coil-conductor segment** (Annotated Fig. 1 below; The conductor segments annotated as A are arranged at a distance apart (i.e., an interval) from one another and extend outward from the respective ends annotated as B.)**, wherein a first region is defined between the two extension-conductor segments and the coil-conductor segments** (Fig. 1, the enclosed circular area within inductor 20)**; and a capacitor component** (Fig. 1, on-chip capacitor 16)**, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer** (Fig. 2a; Capacitor 16 is embedded within wiring structure 10 directly below the "first region" on the opposite surface (i.e. bottom surface) of dielectric 18.)**;**

as per claims 2, 3, and 8, **a second insulation layer** (Fig. 2a, dielectric layer 12)**, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer** (Fig. 2a; Capacitor 16 is sandwiched between dielectric layers 18 and 12.)**; and a transistor component** (Paragraph 23 and Fig. 2a, field effect transistor 22a) **arranged corresponding to the first region in an embedded manner on the**

other surface, opposite to the capacitor component, of the second insulating layer (Fig. 2a; FET 22a is disposed on an opposite surface (i.e. bottom surface) of dielectric layer 12 which is opposite to a top surface of dielectric 12 that faces capacitor 16.)**;**

as per claims 4 and 6, **a tap segment** ("Tap" is defined as an electrical connection made to some point between the end terminals of a component. Vias 48 in Fig. 2 are "tap segments" disposed between input/outputs 25 and 35.)**, electrically connected to the coil-conductor segment; wherein the capacitor component comprises a plurality of connecting segments** (Fig. 2, conductive bars 26 and 28)**, extending corresponding to the two extension-conductor segments in a same direction** (As shown in the annotated Fig. 1 below, conductive bars 26 and 28 (not labeled) which are disposed on the left and right sides of capacitor 16 extend along the line annotated as C, which is the same line direction as which the extension-conductor segments annotated as A extend along.)**; and a plurality of electrode segments** (Fig. 2, electrodes 30 and 32) **located below the first region** (Fig. 1; Electrodes 30 and 32 in Fig. 2 are portions of capacitor 16 which is disposed underneath the enclosed circular area region within inductor 20.)**, wherein one end of each of the plurality of electrode segments extends laterally relative to the coupled connecting segment** (Paragraph 24 and Fig. 2; Electrodes 30 are directly connected with conductive bars 26 and electrodes 32 are directly connected with conductive tab 28. Each of the electrodes has an end that extends laterally or "toward" the side with the other conductive bar that the respective electrode is not connected to.)**; and**

as per claim 7, **wherein the coil-conductor segment (i.e. capacitor component) has a pair of staggered parts** (Fig. 2; Electrode 30 and conductive bar 26 together forms a "first portion" of capacitor 16. Electrode 32 and conductive bar 28 together forms a "second portion" of capacitor 16. It is readily apparent that electrodes 30 and 32 are staggered with respective to one another, and thus each of the "first and second portions" are necessarily disposed in a "staggered" manner with one another.), **a second region is defined by outer sides of the pair of staggered parts** (Fig. 2; Conductive bars 26 and 28 form "outer sides" of capacitor 16, and thus define a region comprising the "staggered" electrodes 30 and 32 that are disposed therein.)**.**

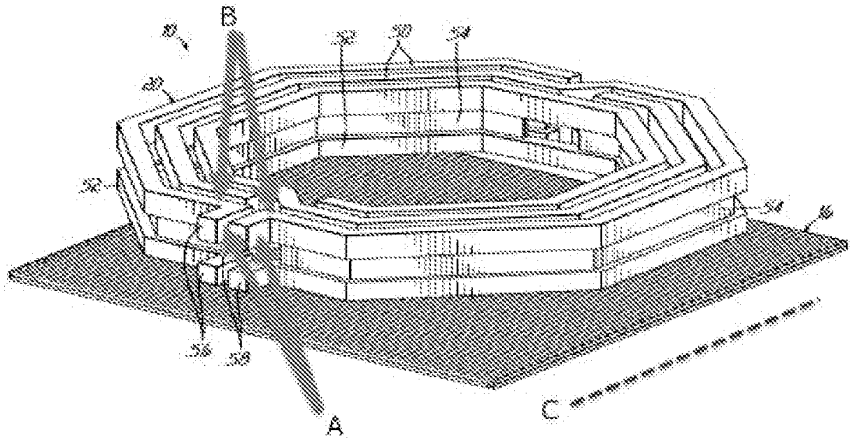


FIG. 1

Allowable Subject Matter

11. Claim 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

As per claim 5, Daley et al. does not disclose the connecting segments being overlapped with the extension-conductor segments, respectively. The connecting segments are disposed to respective sides of the extension-conductor segments.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAKESH PATEL whose telephone number is (571)272-0961. The examiner can normally be reached on Monday-Friday 7:30 am-5:00 pm ET, ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BENNY LEE/
PRIMARY EXAMINER
ART UNIT 2842

/R. P./
Examiner, Art Unit 2842

Notice of References Cited	Application/Control No. 14/338,904	Applicant(s)/Patent Under Reexamination YEN ET AL.	
	Examiner RAKESH PATEL	Art Unit 2842	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0322447 A1	12-2009	Daley; Douglas M.	H01L23/5223	333/185
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

CPC- SEARCHED		
Symbol	Date	Examiner
H03H7/0115, H01F27/2804, H01F2027/2809, H01F17/0013	9/18/2015	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
333	175,177,185	9/18/2015	RP
336	200	9/18/2015	RP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Text Search	9/18/2015	RP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/R.P./ Examiner.Art Unit 2842	

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	NEW 14338904
Filing Date	Jul 23, 2014
First Named Inventor	YEN, Hsiao-Tsung
Art Unit	2842
Examiner Name	Rakesh Patel
Attorney Docket Number	5750/0265PUS1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/RP/		US-8,362,591 B2	01-29-2013	Yen et al.	
/RP/		US-8,552,812 B2	10-08-2013	Yen et al.	
/RP/		US-2011/0128084 A1	06-02-2011	Jin et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/RAKESH PATEL/	Date Considered	09/18/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional).[2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.[3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).[4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.[6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14338904	YEN ET AL.
	Examiner	Art Unit
	RAKESH PATEL	2842

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/18/2015								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	551	(H03H7/0115).cpc.	US-PGPUB; USOCR	OR	ON	2015/09/18 10:58
L2	763	(333/175,185).ccls.	US-PGPUB; USOCR	OR	ON	2015/09/18 10:58
S1	3	("20110128084" | "8552812" | "8362591").PN.	US-PGPUB; USPAT	OR	ON	2015/09/17 11:15
S2	6	("20070155112" | "5015972" | "5477204" | "6949442" | "8072290").PN. OR ("8552812").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 12:44
S3	45	("3539959" | "4313152" | "4616205").PN. OR ("5015972").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 12:45
S4	23	("4816784" | "5015972" | "5061910" | "5477204" | "6097273" | "6320491" | "6380821" | "6396362").PN. OR ("6603383").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 12:52
S5	13	(336/200).ccls. and (333/175).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 13:00
S6	99	(336/200).ccls. and (333/185).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:02
S7	11	(336/200).ccls. and (333/177).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:03
S8	3770	(336/200).ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:29
S9	1398	(H01F27/2804).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:29
S10	343	(H01F2027/2809).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:29
S11	1682	(H01F17/0013).cpc.	US-PGPUB; USPAT;	OR	ON	2015/09/17 14:29

			USOCR			
S12	822	(S9 or S10 or S11) and (resona$4)	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:30
S13	33	S12 and finger	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:30
S14	86	(S9 or S10 or S11) and (LC adj resona$4)	US-PGPUB; USPAT; USOCR	OR	ON	2015/09/17 14:41
S15	1	(12/146555).APP.	US-PGPUB; USOCR	OR	ON	2015/09/17 14:47

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BIB DATA SHEET

CONFIRMATION NO. 1455

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/338,904	07/23/2014	333	2842	5750/0265PUS1

APPLICANTS
REALTEK SEMICONDUCTOR CORP., Hsinchu, TAIWAN;

INVENTORS
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Yuh-Sheng JEAN, Hsinchu, TAIWAN;
Ta-Hsun YEH, Hsinchu, TAIWAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************
TAIWAN 103113947 04/16/2014

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
08/01/2014

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged // Examiner's Signature	☐ Met after Allowance /R.P./ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	17	10	1

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Muncy, Geissler, Olds & Lowe, P.C.
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UNITED STATES

TITLE
SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/338,904

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	10 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/338,904	07/23/2014	2843	1600	5750/0265PUS1	10	1

CONFIRMATION NO. 1455

60601
Muncy, Geissler, Olds & Lowe, P.C.
4000 Legato Road
Suite 310
FAIRFAX, VA 22033

FILING RECEIPT

OC000000069955842

Date Mailed: 08/01/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Applicant(s)

REALTEK SEMICONDUCTOR CORP., Hsinchu, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 60601

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
TAIWAN 103113947 04/16/2014

If Required, Foreign Filing License Granted: 08/01/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/338,904**

Projected Publication Date: 10/22/2015

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

Preliminary Class

333

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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茲證明所附文件，係本局存檔中原申請案的副本，正確無訛，
其申請資料如下 ：

This is to certify that annexed is a true copy from the records of this office of the application as originally filed which is identified hereunder：

申　　請　　日 ： 西元 2014 年 04 月 16 日
Application Date　　Apr. 16, 2014

申 請 案 號 ： 103113947
Application No.

申　　請　　人 ： 瑞昱半導體股份有限公司
Applicant(s)

發　　明　　人 ： 顏孝璁、簡育生、葉達勳
Inventor(s)

局　　長
Director General
王美花

西元 2014 年 05 月 20 日
May. 20, 2014

專利案號：103113947

申請日：
IPC分類：

【發明摘要】

【中文發明名稱】具有電感電容諧振電路之半導體裝置

【英文發明名稱】Semiconductor device with inductor-capacitor resonant circuit

【中文】

一種具有電感電容諧振電路之半導體裝置包括一第一絕緣層、一電感組件以及一電容組件。電感組件包括一線圈線段以及二延伸線段。線圈線段與延伸線段位於第一絕緣層的同一表面上，且延伸線段分別耦接在線圈線段的兩端。延伸線段彼此間隔，並且相對線圈線段向外側延伸。延伸線段與線圈線段定義出一第一區域，而電容組件對應第一區域內藏式設置於第一絕緣層相對電感組件的另一表面。

【英文】

A semiconductor device with inductor-capacitor resonant circuit includes a first isolation layer, an inductance component and a capacitance component. The inductance component includes a winding conductor segment and two extended conductor segments. The winding conductor segment and the extended conductor segments are disposed on the same surface of the first isolation layer. The extended conductor segments are coupled to two ends of the winding conductor segment, respectively. The extended conductor segments are separated from each other, and extend outwardly relative to the winding conductor segment. A first area is defined by

申請案號：103113947

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the winding conductor segment and the extended conductor segments, and the capacitance component is embedded and disposed on another surface of the first isolation layer opposite to the inductance component and corresponding to the first area.

【指定代表圖】　第 7 圖

【代表圖之符號簡單說明】

110	絕緣層
112	絕緣層
120	區域
122	區域
130	電感組件
140	抽頭線段
150	電容組件
170	電晶體組件
191	導孔

【特徵化學式】　無

【發明說明書】

【中文發明名稱】具有電感電容諧振電路之半導體裝置

【英文發明名稱】Semiconductor device with inductor-capacitor resonant circuit

【技術領域】

【0001】 本發明是關於一種半導體裝置，特別是關於一種具有電感電容諧振電路之半導體裝置。

【先前技術】

【0002】 隨著電子產多功能整合的發展趨勢，越來越多的電路元件需要整合設計於半導體晶片中。

【0003】 典型的半導體積體電路包含一矽基底。一層以上的絕緣層設置於基底上，且一層以上的金屬層設置於絕緣層中。這些金屬層可藉由現行的半導體製程技術而形成晶片內建部件。因此，為了縮小電子產品的體積，許多電子元件改以內藏（embedded）式設置，以取代表面黏著（surface mounted technique；SMT）式的設置方式。

【0004】 在電路設計中，常見使用電感電容諧振電路（LC resonant circuit）來提供訊號的傳輸或過濾，例如在濾波器、網路阻抗匹配電路、壓控震盪器（VCO）、傳送與收發模組等電路中。然而，在高頻時，訊號會穿越絕緣層流失到矽基底而造成訊號的能量損耗。因此，如何設計內藏式電感電容諧振電路以進一步縮小整體尺寸且不影響訊號傳輸或過濾的效果，其為相關電路設計者持續努力研究之項目之一。

【發明內容】

【0005】 在一實施例中，一種具有電感電容諧振電路之半導體裝置包括一第一絕緣層、一電感組件以及一電容組件。電感組件包括一線圈線段以及二延伸線段。線圈線段與延伸線段位於第一絕緣層的同一表面上，且延伸線段分別耦接在線圈線段的兩端。延伸線段彼此間隔，並且相對線圈線段向外側延伸。其中，延伸線段與線圈線段定義出一第一區域，而電容組件對應第一區域內藏式設置於第一絕緣層相對電感組件的另一表面。

【0006】 綜上，根據本發明之具有電感電容諧振電路之半導體裝置，其可利用立體堆疊晶粒（3D stacking dies）技術整合電感電容諧振電路在半導體基板上，並對應電感組件的輸入/輸出部設置諧振電容器，以減少相位雜訊的產生、減少內連走線（interconnect）的設置並縮小整體面積。在一些實施例中，根據本發明之具有電感電容諧振電路之半導體裝置更對應電感組件的輸入/輸出部及/或交錯部設置其他電子組件，以更進一步減少相位雜訊的產生、減少內連走線（interconnect）的設置並縮小整體面積。

【圖式簡單說明】

【0007】

[第1圖]是根據本發明第一實施例之具有電感電容諧振電路之半導體裝置的立體圖。

[第2圖]是第1圖之半導體裝置的俯視圖。

[第3圖]是第1圖之半導體裝置的爆炸圖。

[第4圖]是根據本發明第二實施例之具有電感電容諧振電路之半導體裝置的立體圖。

[第5圖]是第4圖之半導體裝置的俯視圖。

[第6圖]是第4圖之半導體裝置的爆炸圖。

[第7圖]是根據本發明第三實施例之具有電感電容諧振電路之半導體裝置的立體圖。

[第8圖]是第7圖之半導體裝置的俯視圖。

[第9圖]是第7圖之半導體裝置的爆炸圖。

[第10圖]是根據本發明第四實施例之具有電感電容諧振電路之半導體裝置的立體圖。

[第11圖]是第10圖之半導體裝置的俯視圖。

[第12圖]是第10圖之半導體裝置的爆炸圖。

[第13圖]是根據本發明第五實施例之具有電感電容諧振電路之半導體裝置的俯視圖。

[第14圖]是根據本發明第六實施例之具有電感電容諧振電路之半導體裝置的立體圖。

[第15圖]是第14圖之半導體裝置的俯視圖。

[第16圖]是根據本發明第七實施例之具有電感電容諧振電路之半導體裝置的立體圖。

[第17圖]是第16圖之半導體裝置的俯視圖。

【實施方式】

【0008】 為了清楚表現各元件，於圖式中有時會以透明化或省略的

方式呈現絕緣層，然此非本發明之限制。並且，以下述及之「第一」、「第二」、「第三」及「第四」等術語，其係用以區別所指之元件，而非用以排序或限定所指元件之差異性，且亦非用以限制本發明之範圍。

【0009】 第1至3圖為根據本發明第一實施例之具有電感電容諧振電路之半導體裝置的示意圖，而第4至6圖為根據本發明第二實施例之具有電感電容諧振電路之半導體裝置的示意圖。

【0010】 參照第1至6圖，具有電感電容諧振電路之半導體裝置包括一絕緣層110（以下稱之為第一絕緣層110）、一電感組件130以及一電容組件150。

【0011】 於此，電感組件130以及電容組件150是分別由位在第一絕緣層110相對二表面上之二金屬層圖案化而成。換言之，電感組件130是形成在第一絕緣層110的上表面上（或上方），而電容組件150是形成在第一絕緣層110的下表面上（或下方）。而電感組件130以及電容組件150可以一層以上的金屬層來形成。

【0012】 電感組件130包括一線圈線段131以及二延伸線段133、135。其中，線圈線段131作為電感器的感應部，即用以產生電磁感應。延伸線段133、135作為輸入/輸出部，即用以接收或輸出信號。線圈線段131以及延伸線段133位在第一絕緣層110的上表面上。延伸線段135能位在第一絕緣層110的上表面上或第一絕緣層110中。

【0013】 二延伸線段133、135彼此間隔，並且分別耦接（直接銜接）在線圈線段131的兩端。換言之，二延伸線段133、135直接銜接線圈線段131的兩端，並從線圈線段131的兩端相對線圈線段131向外側延伸。

換言之，延伸線段133、135朝向遠離線圈線段131的方向延伸。

【0014】 於此，二延伸線段133、135位在線圈線段131的同一側，並且二延伸線段133、135與線圈線段131定義出一區域120（以下稱之為第一區域120）。

【0015】 電容組件150則對應第一區域120內藏式設置於第一絕緣層110相對電感組件130的另一表面（即，第一絕緣層110的下表面）上。換言之，電容組件150是位在第一區域120的下方，並且與電感組件130之間間隔第一絕緣層110。

【0016】 在一些實施例中，電感組件130可為平面螺旋式（spiral）或堆疊螺旋式（helical）（即，以多層金屬連接成螺旋狀）。於此，線圈線段131以及二延伸線段133、135是由多個金屬層圖案化而成。

【0017】 在另一些實施例中，參照第4至6圖，電感組件130具有幾何對稱性，即為對稱式電感。於此，線圈線段131以及二延伸線段133、135均個別為單一路徑的走線。其中，二延伸線段133、135大致上相互平行。延伸線段133銜接線圈線段131的第一端，並且大致上垂直於其與線圈線段131的銜接處。延伸線段135銜接線圈線段131的第二端，並且大致上垂直於其與線圈線段131的銜接處。第一區域120則是位在線圈線段131以及二延伸線段133、135之間。於此，線圈線段131以及二延伸線段133、135是由一金屬層圖案化而成。

【0018】 於此，電容組件150可全部對應設置在延伸線段133、135的外側邊之間。再者，電容組件150亦可對應位在延伸線段133、135中之一的外側邊與另一的內側邊之間。此外，電容組件150亦可全部對應

設置在延伸線段133、135的內側邊之間。

【0019】 其中，電容組件150可為單端式（如第1至3圖所示）或差動式（如第4至6圖所示）。雖然在此些實施例中電容組件150中之所有電容是使用同一層金屬，但本發明不限於此，其亦可使用多層不同金屬層來形成並聯的電容以增加電容值，或是進一步並聯或使用下方的半導體電晶體電容。

【0020】 在一些實施例中，參照第1至3圖，電容組件150包括二連結線段151、152（以下稱之為第一連結線段151以及第二連結線段152）以及多個電極線段155、156（以下稱之為第一電極線段155以及第二電極線段156）。

【0021】 其中，電極線段155、156是作為電容器的電極板，並於電極線段155、156之間產生電容感應。而連結線段151、152則是用以接收或輸出信號。連結線段151、152以及電極線段155、156都是形成在第一絕緣層110的下表面上。於此，連結線段151、152以及電極線段155、156是由第二金屬層圖案化而成。

【0022】 第一連結線段151以及第二連結線段152對應延伸線段133、135同向延伸。第一電極線段155以及第二電極線段156位於第一區域120的下方。

【0023】 在一些實施例中，第一連結線段151對應延伸線段133而設置在第一絕緣層110的下表面上（或下方），而第二連結線段152則對應延伸線段135而設置在第一絕緣層110的下表面上（或下方）(或下方)。其中，第一連結線段151可位在延伸線段133的下方，並且與延伸線段

133重疊。第二連結線段152可位在延伸線段135的下方，並且與延伸線段135重疊。在一些實施例中，第一連結線段151及/或第二連結線段152可不與對應之延伸線段133/135重疊，而是位在第一區域120下方且對應位在二延伸線段133、135之間。

【0024】 於此，第一電極線段155的一端耦接第一連結線段151的側邊，而另一端則相對所耦接的第一連結線段151側向延伸。其中，第一電極線段155由第一連結線段151的側邊朝向第二連結線段152延伸。在一些實施例中，第一電極線段155大致上垂直第一連結線段151。

【0025】 第二電極線段156的一端耦接第二連結線段152的側邊，而另一端則相對所耦接的第二連結線段152側向延伸。其中，第二電極線段156由第二連結線段152的側邊朝向第一連結線段151延伸。在一些實施例中，第二電極線段156大致上垂直第二連結線段152。

【0026】 在此實施例中，第一電極線段155與第二電極線段156交錯設置。

【0027】 在一些實施例中，參照第4至6圖，電容組件150包括三連結線段151、152、153（以下稱之為第一連結線段151、第二連結線段152以及第三連結線段153）以及多個電極線段155、156、157、158（以下稱之為第一電極線段155、第二電極線段156、第三電極線段157以及第四電極線段158）。

【0028】 其中，電極線段155、156、157、158是作為電容器的電極板，並於電極線段155、157之間以及於電極線段156、158之間產生電容感應。連結線段151、152用以接收或輸出信號，而連結線段153則

例如用以接地。連結線段151、152、153以及電極線段155、156、157、158都是形成在第一絕緣層110的下表面上。於此，連結線段151、152、153以及電極線段155、156、157、158是由第二金屬層圖案化而成。

【0029】 第一連結線段151、第二連結線段152以及第三連結線段153同向延伸。第三連結線段153位在第一連結線段151以及第二連結線段152之間，並且位於第一區域120的下方。第一電極線段155、第二電極線段156、第三電極線段157以及第四電極線段158位於第一區域120的下方。其中，第一連結線段151與第二連結線段152的設置方式大致上相同於前述，故不再贅述。

【0030】 於此，第一電極線段155與第三電極線段157配對，而第二電極線段156與第四電極線段158配對。

【0031】 第一電極線段155的一端耦接第一連結線段151的側邊，而另一端則相對所耦接的第一連結線段151側向延伸。其中，第一電極線段155由第一連結線段151的側邊朝向第二連結線段152以及第三連結線段153延伸，並且位在第一連結線段151與第三連結線段153之間。在一些實施例中，第一電極線段155大致上垂直第一連結線段151。

【0032】 第二電極線段156的一端耦接第二連結線段152的側邊，而另一端則相對所耦接的第二連結線段152側向延伸。其中，第二電極線段156由第二連結線段152的側邊朝向第一連結線段151以及第三連結線段153延伸，並且位在第二連結線段152與第三連結線段153之間。在一些實施例中，第二電極線段156大致上垂直第二連結線段152。

【0033】 第三電極線段157的一端耦接第三連結線段153鄰近第一

連結線段151的側邊，而另一端則相對所耦接的第三連結線段153側向延伸。其中，第三電極線段157由第三連結線段153的側邊朝向第一連結線段151延伸，並且位在第一連結線段151與第三連結線段153之間。在一些實施例中，第三電極線段157大致上垂直第三連結線段153。在此實施例中，第一電極線段155與第三電極線段157交錯設置。

【0034】 第四電極線段158的一端耦接第三連結線段153鄰近第二連結線段152的側邊，而另一端則相對所耦接的第三連結線段153側向延伸。其中，第四電極線段158由第三連結線段153的側邊朝向第二連結線段152延伸，並且位在第二連結線段152與第三連結線段153之間。在一些實施例中，第四電極線段158大致上垂直第三連結線段153。在此實施例中，第四電極線段158與第二電極線段156交錯設置。

【0035】 在一些實施例中，電容組件150的電極線段155、156、157、158可對應從延伸線段133、135與線圈線段131的銜接處開始相對線圈線段131向外配置，如第1至6圖所示。在一些實施例中，電容組件150的電極線段155、156、157、158亦可對應從線圈線段131的第2圈（由外側起算）的外側開始相對線圈線段131向外配置，如第7至9圖所示。在一些實施例中，電極線段155、156、157、158可完全位在第一區域120下方且對應位在二延伸線段133、135之間。

【0036】 在一些實施例中，參照第7至12圖，半導體裝置更包括一電子組件以及另一絕緣層112（以下稱之為第二絕緣層112）。於此，其中，此電子組件可為另一電容組件150'（如第10至12圖所示）、電晶體組件170（如第7至9圖所示）、二極體組件或電阻組件等內藏式電子元

件。

【0037】 電子組件夾設在第一絕緣層110與第二絕緣層112之間。電子組件對應第一區域120內藏式設置於第二絕緣層112相對電容組件150的另一表面上。換言之，電容組件150位在第二絕緣層112的上表面，而電子組件則位在第二絕緣層112的下表面。

【0038】 電子組件位在第一區域120下方的與電容組件150不同之電路層上。於此，電子組件是由在第二絕緣層112的下表面上的一第三金屬層圖案化而成。

【0039】 於此，電子組件可全部對應設置在延伸線段133、135的外側邊之間。再者，電子組件亦可對應位在延伸線段133、135中之一的外側邊與另一的內側邊之間。此外，電子組件亦可全部對應設置在延伸線段133、135的內側邊之間。

【0040】 在一些實施例中，當電子組件為電晶體組件170時，參照第7至9圖，電晶體組件170包括二連結線段171、172、二半導體線段173、174以及多個電極線段175、176、177、178。其中，電晶體組件170可以為操作在不同區間的電晶體或一電晶體電容。

【0041】 連結線段171、172以及電極線段175、176、177、178是位在第二絕緣層112的下表面上。在一些實施例中，連結線段171、172以及電極線段175、176、177、178是由位在第二絕緣層112的下表面上的第三金屬層圖案化而成。半導體線段173、174則是由第三金屬層下方之半導體材料層圖案化而成。

【0042】 連結線段171、172分別對應延伸線段133、135同向延伸。

半導體線段172、173以及電極線段175、176、177、178位於第一區域120的下方。在一些實施例中，連結線段171與對應之延伸線段133重疊，而連結線段172與對應之延伸線段135重疊。再者，連結線段171及/或連結線段172亦可不與對應之延伸線段133/135重疊，而是位在第一區域120下方且對應位在二延伸線段133、135之間。

【0043】 電極線段175的一端耦接在連結線段171鄰近連結線段172的一側，而另一端朝向連結線段172延伸。電極線段177與電極線段175同向延伸，並以一間隔設置在電極線段175的側邊。其中，當電極線段175及/或電極線段177為多個時，電極線段175、177交錯配置。

【0044】 電極線段176的一端耦接在連結線段172鄰近連結線段171的一側，而另一端朝向連結線段171延伸。電極線段178與電極線段176同向延伸，並以一間隔設置在電極線段176的側邊。其中，當電極線段176及/或電極線段178為多個時，電極線段176、178交錯配置。

【0045】 半導體線段173位在電極線段175、177的下方，並沿著電極線段175、177的配置方向延伸。在一些實施例中，半導體線段173的延伸方向大致上垂直於電極線段175、177的延伸方向。

【0046】 半導體線段174位在電極線段176、178的下方，並沿著電極線段176、178的配置方向延伸。在一些實施例中，半導體線段174的延伸方向大致上垂直於電極線段176、178的延伸方向。

【0047】 再者，電晶體組件170可更包括一個或多個跨接線段179，並且跨接線段179位在第二絕緣層112的下表面上。在一些實施例中，跨接線段179亦可由第三金屬層圖案化而成。跨接線段179的二端分別耦接

電極線段175、178、或者分別耦接電極線段176、177。

【0048】 在一些實施例中，參照第10至12圖，當電子組件為電容組件150'時，除了電容組件150'在第二絕緣層112的下表面上外，電容組件150'的配置關係可大致上相同於電容組件150。

【0049】 於此，各種內藏式電子元件的結構為本領域所熟知，故不再贅述。

【0050】 在一些實施例中，電感組件130可為一匝，如第4至6圖所示。電感組件130可為多匝，例如：二匝（如第1至3及7至9圖所示）、三匝（如第10至13圖所示）或更多等。

【0051】 在一些實施例中，第一區域120可限制在二延伸線段133、135之間，如第6圖所示。在一些實施例中，第一區域120可限制在二延伸線段133、135及線圈線段131之間，如第9圖所示。

【0052】 舉例來說，參照第4至6圖，當電感組件130為一匝時，第一區域120為夾設在二延伸線段133、135之間的空間。參照第7至9圖，當電感組件130為多匝時，第一區域120為夾設在二延伸線段133、135與線圈線段131的第2圈（由外側起算）之間的空間，即由二延伸線段133、135與線圈線段131的第2圈所圍繞的空間。

【0053】 在一些實施例中，參照第7至9圖，當電感組件130為多匝時，線圈線段131包括多個半圈導線L1、L2、L3、L4以及至少一對交錯部。以下以二匝為例進行說明。

【0054】 半圈導線L1、L2、L3、L4可區分為二個第一半圈導線L1、L3以及二個第二半圈導線L2、L4。每一對交錯部具有二交錯導線L5、

L6。

【0055】 第一半圈導線L1、L3與延伸線段133位在同一側，而第二半圈導線L2、L4與延伸線段135位在同一側。

【0056】 第一半圈導線L1的一端耦接延伸線段133，而第一半圈導線L1的另一端耦接交錯導線L5的一端。交錯導線L5的另一端耦接第二半圈導線L4的一端，而第二半圈導線L4的另一端耦接第一半圈導線L3的一端。第一半圈導線L3的另一端耦接交錯導線L6的一端，而交錯導線L6的另一端耦接第二半圈導線L2的一端。第二半圈導線L2的另一端耦接延伸線段135。

【0057】 其中，交錯導線L5、L6相互交錯並且其外側定義出另一區域122（以下稱之為第二區域122）。

【0058】 於此，參照第14至17圖，亦可對應第二區域122內藏式設置一電子組件在第一絕緣層110相對電感組件130的另一表面（即，第一絕緣層110的下表面）上。其中，對應第二區域122的電子組件可為另一電容組件150''（如第14及15圖所示）、電晶體組件170''（如第16及17圖所示）、二極體組件或電阻組件等內藏式電子元件。於此，內藏式電子元件的結構為本領域所熟知，故不再贅述。

【0059】 在一些實施例中，第二區域122為一空區域，即位在最外側之交錯部的外側的未佈線區域。

【0060】 在一些實施例中，參照第7至17圖，半導體裝置可更包括一抽頭線段140。抽頭線段140電性連接線圈線段131，以致於抽頭線段140與電感組件130形成抽頭式電感器。其中，抽頭線段140例如可用以

電性連接固定電位，藉以提供直流路徑、及/或電源、及/或接地。

【0061】 在一些實施例，參照第7至9、16及17圖，抽頭線段140形成在第一絕緣層110的上表面上。其中，抽頭線段140與電感組件130能以同一金屬層圖案化而成。

【0062】 抽頭線段140在延伸線段133、135之間，並且與延伸線段133、135同向向外延伸。於此，抽頭線段140將第一區域120區隔成一第一空區域120a以及一第二空區域120b。第一空區域120a是由延伸線段133、線圈線段131以及抽頭線段140所圍繞的未佈線區域。第二空區域120b是由延伸線段135、線圈線段131以及抽頭線段140所圍繞的未佈線區域。

【0063】 其中，當在延伸線段133、135之間不存在抽頭線段140時，第一區域120為一空區域，即未佈線區域，如第1至6及10至15圖所示。

【0064】 在一些實施例，參照第7、10及14圖，第一絕緣層110可分為上層110a以及下層110b。抽頭線段140夾設在上層110a以及下層110b之間。換言之，電感組件130形成在上層110a的上表面上，而抽頭線段140則位在上層110a的下表面（即，下層110b的上表面）上。於此，抽頭線段140與電感組件130為不同電路層。其中，抽頭線段140可由在上層110a的下表面（即，下層110b的上表面）上的一第四金屬層圖案化而成。

【0065】 在一些實施例中，位在不同電路層的電子元件，例如：電感組件130、抽頭線段140、電容組件150、150’、150’’、電晶體組件170、170’或其他內藏式電子元件等，任二者之間的電性能經由其它電

路的連接能電性導通。換言之，位在不同電路層的電子元件之間可不直接以導孔（via）連接。

【0066】 在一些實施例中，參照1至17圖，位在不同電路層的電子元件，例如：電感組件130、抽頭線段140、電容組件150、150'、150''、電晶體組件170、170'或其他內藏式電子元件等，任二者之間亦可藉由導孔190/191/192/194/196/198電性導通，以致於二電子元件之間形成並聯或串聯之電性連接關係。

【0067】 參照第7至12圖，一導孔190設置在抽頭線段140與線圈線段131之間，並電性連接抽頭線段140與線圈線段131。換言之，導孔190由上層110a的上表面貫穿至上層110a的下表面，並導通上層110a的上表面與上層110a的下表面。其中，導孔190的一端耦接線圈線段131，而導孔190的另一端耦接抽頭線段140。

【0068】 參照第4至9及11至14圖，一導孔191設置在抽頭線段140與電容組件150（或150'）之連結線段153之間，並電性連接抽頭線段140與連結線段153。換言之，導孔191由第一絕緣層110的上表面貫穿至第一絕緣層110的下表面，並導通第一絕緣層110的上表面與第一絕緣層110的下表面。或者，導孔191是由下層110b的上表面貫穿至下層110b的下表面，並導通下層110b的上表面與下層110b的下表面。其中，導孔191的一端耦接線圈線段131，而導孔191的另一端耦接抽頭線段140。

【0069】 在一些實施例中，線圈線段131、抽頭線段140與連結線段153能以單一導孔（導孔190與導孔191位在相同垂直位置，即為同軸）電性連接。換言之，此導孔二端分別耦接線圈線段131與連結線段153，

而抽頭線段140耦接在此導孔的中段。

【0070】 參照第1至3圖，一導孔194設置在電感組件130之延伸線段135與電容組件150之連結線段152之間，並電性連接電感組件130與電容組件150。換言之，導孔194由第一絕緣層110的上表面貫穿至第一絕緣層110的下表面，並導通第一絕緣層110的上表面與第一絕緣層110的下表面。其中，導孔194的一端耦接延伸線段135，而導孔194的另一端耦接連結線段152。

【0071】 參照第4至6圖，一導孔192設置在電感組件130之延伸線段133與電容組件150之連結線段151之間，並電性連接電感組件130與電容組件150。換言之，導孔192由第一絕緣層110的上表面貫穿至第一絕緣層110的下表面，並導通第一絕緣層110的上表面與第一絕緣層110的下表面。其中，導孔192的一端耦接延伸線段133，而導孔192的另一端耦接連結線段153。

【0072】 換言之，在差動架構下，電感組件130的二端能分別藉由導孔192與導孔194導通連結至電容組件150的二端。

【0073】 參照第10及12圖，一導孔196/198設置在電容組件150之連結線段151/152與其下方之電子組件（例如：電容組件150'之連結線段151/152）之間，並電性連接電容組件150與其下方之電子組件。換言之，導孔196由第二絕緣層112的上表面貫穿至第二絕緣層112的下表面，並導通第二絕緣層112的上表面與第二絕緣層112的下表面。其中，導孔196的一端耦接連結線段151/152，而導孔196的另一端耦接其下方之電子組件（例如：電容組件150'之連結線段151/152）。

【0074】 在一些實施例中，延伸線段133與下方所有之電子組件的連結線段能以單一導孔（導孔192與導孔196位在相同垂直位置，即為同軸）電性連接。舉例而言，一導孔的二端分別耦接電感組件130的延伸線段133與電容組件150'之連結線段151（或電晶體組件170之連結線段171），而電容組件150之連結線段151耦接在此導孔的中段。

【0075】 同樣地，延伸線段135與下方所有之電子組件的連結線段亦能以單一導孔（導孔194與導孔198位在相同垂直位置，即為同軸）電性連接。舉例而言，一導孔的二端分別耦接電感組件130的延伸線段135與電容組件150'之連結線段153（或電晶體組件170之連結線段173），而電容組件150之連結線段153耦接在此導孔的中段。

【0076】 在一些實施例中，電容組件150、150'、150''可為各種型態之電容，例如：金屬-氧化物-金屬（metal-oxide-metal；MOM）電容、金屬-絕緣層-金屬（metal-insulator-metal；MIM）電容、或金屬-氧化物-半導體（metal-oxide-semiconductor；MOS）電容等。於此，各種型態之電容的結構組成為本領域所熟知。以MOS電容為例，參照第12圖，除上述實施例之構件外，電容組件150'更包括至少一半導體線段154、159。各半導體線段154（或159）在介電層的間隔下位在交錯之第一電極線段155（或156）與第二電極線段157（或158）下方，並且半導體線段154、159的延伸方向大致上垂直於第一電極線段155、156與第二電極線段157、158的延伸方向。

【0077】 於此，前述之電容組件150、150'、150''及電晶體組件170的電極線段175、176、177、178在圖式中雖然均是以單層金屬層表現，

但此非本發明之限制，在配合實際電路需求下，前述之電容組件150、150’、150’’及電晶體組件170的電極線段175、176、177、178能為單層金屬層或為多層金屬層（metal stack）。

【0078】 再者，前述之各絕緣層可包括經過一道或多道半導體程序所形成之一層或多層絕緣材料。

【0079】 綜上，根據本發明之具有電感電容諧振電路之半導體裝置可利用立體堆疊晶粒（3D stacking dies）技術整合電感電容諧振電路在半導體基板上，並對應電感組件的輸入/輸出部設置諧振電容器，以減少相位雜訊的產生、減少內連走線（interconnect）的設置並縮小整體面積。在一些實施例中，根據本發明之具有電感電容諧振電路之半導體裝置更對應電感組件的輸入/輸出部及/或交錯部設置其他電子組件，以更進一步減少相位雜訊的產生、減少內連走線（interconnect）的設置並縮小整體面積。

【0080】 雖然本發明以前述之實施例揭露如上，然其並非用以限定本發明，任何熟習相像技術者，在不脫離本發明之精神和範圍內，當可作些許之更動與潤飾，因此本發明之專利保護範圍須視本說明書所附之申請專利範圍所界定者為準。

【符號說明】

【0081】

110	絕緣層
110a	上層
110b	下層
112	絕緣層
120	區域
122	區域
130	電感組件
131	線圈線段
133	延伸線段
135	延伸線段
140	抽頭線段
150	電容組件
150’	電容組件
150’’	電容組件
151	連結線段
152	連結線段
153	連結線段
154	半導體線段
155	電極線段
156	電極線段

157	電極線段
158	電極線段
159	半導體線段
170	電晶體組件
170”	電晶體組件
171	連結線段
172	連結線段
173	半導體線段
174	半導體線段
175	電極線段
176	電極線段
177	電極線段
178	電極線段
190	導孔
191	導孔
192	導孔
194	導孔
196	導孔
198	導孔
L1	半圈導線
L2	半圈導線
L3	半圈導線

L4	半圈導線
L5	交錯導線
L6	交錯導線
120a	第一空區域
120b	第二空區域
179	跨接線段

【發明申請專利範圍】

【第1項】 一種具有電感電容諧振電路之半導體裝置，包括：

一第一絕緣層；

一電感組件，包括：

一線圈線段，位於該第一絕緣層的一表面上；以及

二延伸線段，位於該第一絕緣層的該表面上，分別耦接在該線圈線段的兩端，彼此間隔且相對該線圈線段向外側延伸，其中該些延伸線段與該線圈線段定義出一第一區域；以及

一電容組件，對應該第一區域內藏式設置於該第一絕緣層相對該電感組件的另一表面。

【第2項】 如請求項1所述之具有電感電容諧振電路之半導體裝置，更包括：

一第二絕緣層，與該第一絕緣層之間夾設該電容組件；以及

一電子組件，對應該第一區域內藏式設置於該第二絕緣層相對該電容組件的另一表面上。

【第3項】 如請求項2所述之具有電感電容諧振電路之半導體裝置，其中該電子組件為另一電容組件、一電晶體組件、二極體組件以及一電阻組件中之一。

【第4項】 如請求項1所述之具有電感電容諧振電路之半導體裝置，其中該電容組件更包括：

複數個連結線段，對應該些延伸線段同向延伸；以及

複數個電極線段，位於該第一區域的下方，各該電極線段的一端耦接於該些連結線段中之一，並相對所耦接的該連結線段側向延伸。

【第5項】 如請求項4所述之具有電感電容諧振電路之半導體裝置，其中該些連結線段分別與該些延伸線段重疊。

【第6項】 如請求項1所述之具有電感電容諧振電路之半導體裝置，更包括：

一抽頭線段，電性連接該線圈線段；

其中，該電容組件更包括：

複數個連結線段，對應該些延伸線段同向延伸，其中該些連結線段中之一位在該抽頭線段的下方且與該抽頭線段重疊；以及

複數個電極線段，位於該第一區域的下方，各該電極線段的一端耦接於該些連結線段中之一，並相對所耦接的該連結線段側向延伸。

【第7項】 如請求項1所述之具有電感電容諧振電路之半導體裝置，其中該線圈線段具有一對交錯部，該對交錯部的外側定義一第二區域，且該半導體裝置更包括：

一電子組件，對應該第二區域內藏式設置於該第一絕緣層相對該電感組件的另一表面上。

【第8項】 如請求項7所述之具有電感電容諧振電路之半導體裝置，其中該電子組件為另一電容組件、一電晶體組件、二極體組件以及一電阻組件中之一。

【第9項】 如請求項1所述之具有電感電容諧振電路之半導體裝置，其中該第一區域是限制在該些延伸線段之間。

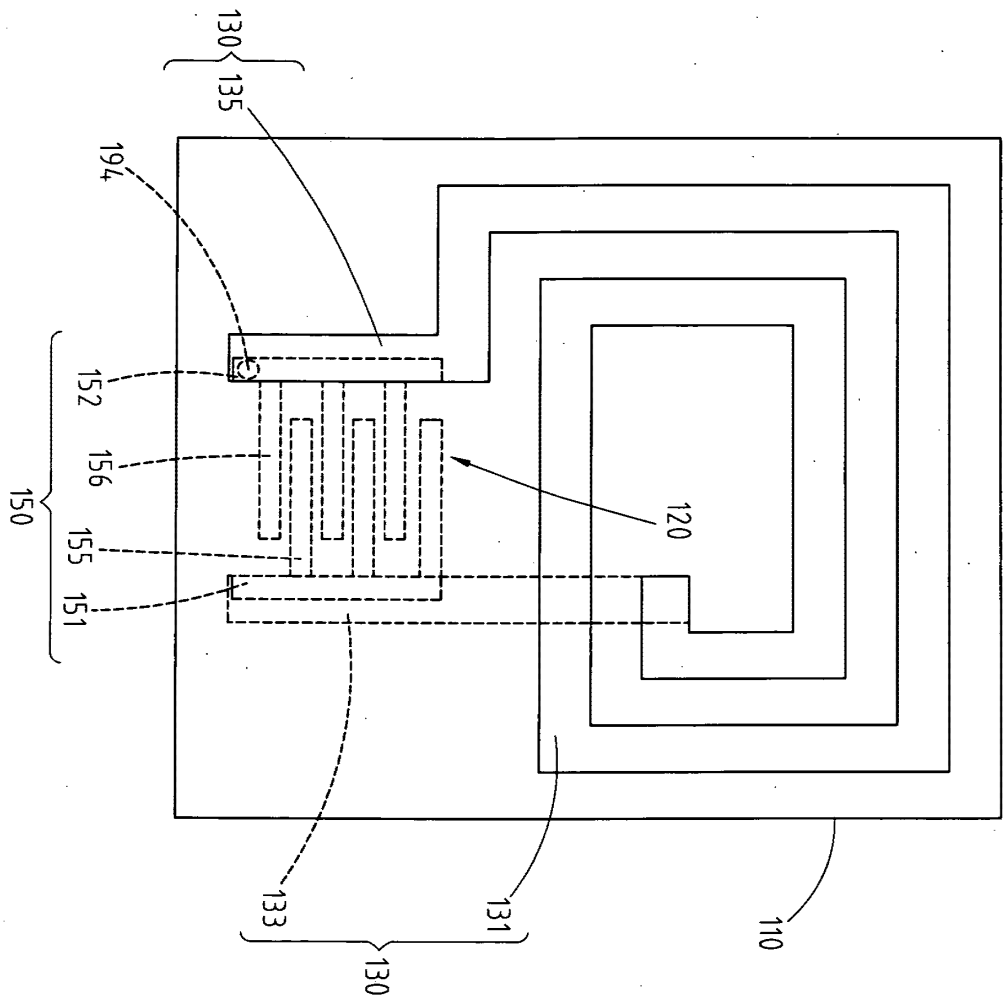
【第10項】 如請求項9所述之具有電感電容諧振電路之半導體裝置，其中該第一區域是限制在該些延伸線段與該線圈線段之間。

第1圖

【發明圖式】

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第2圖

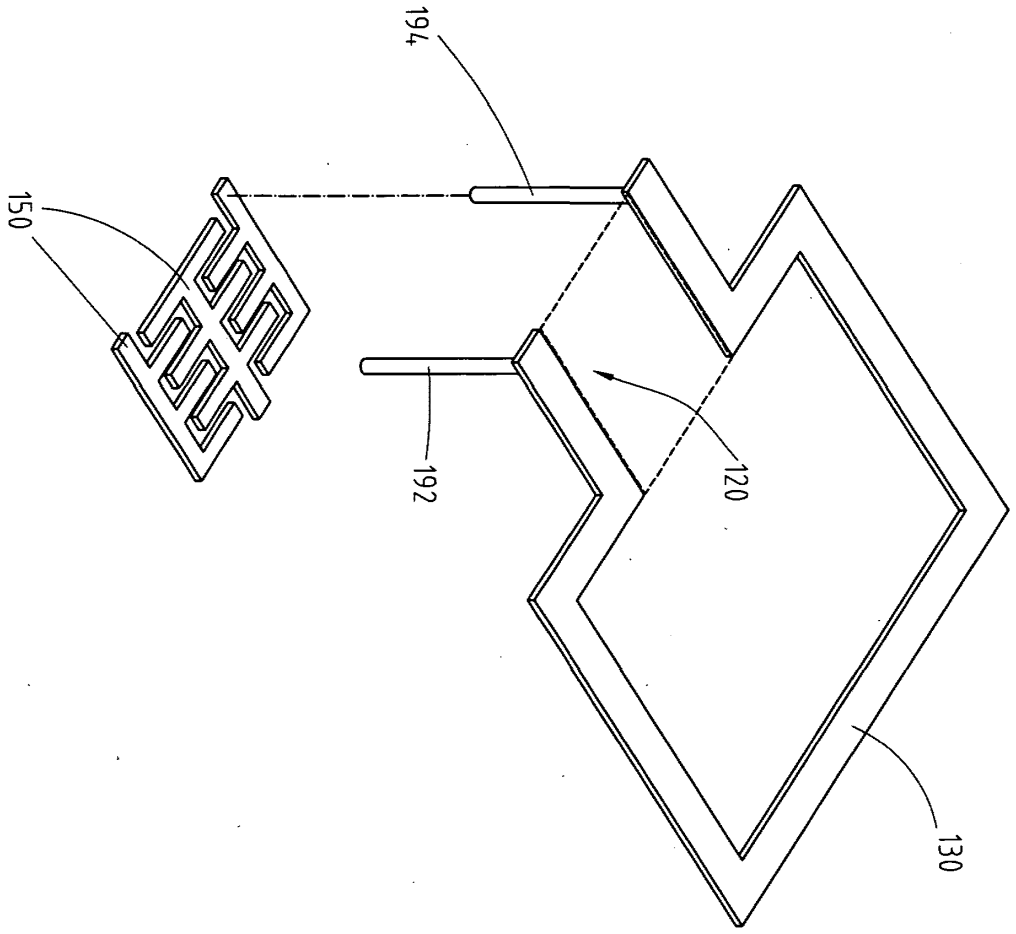
第3圖

第4圖

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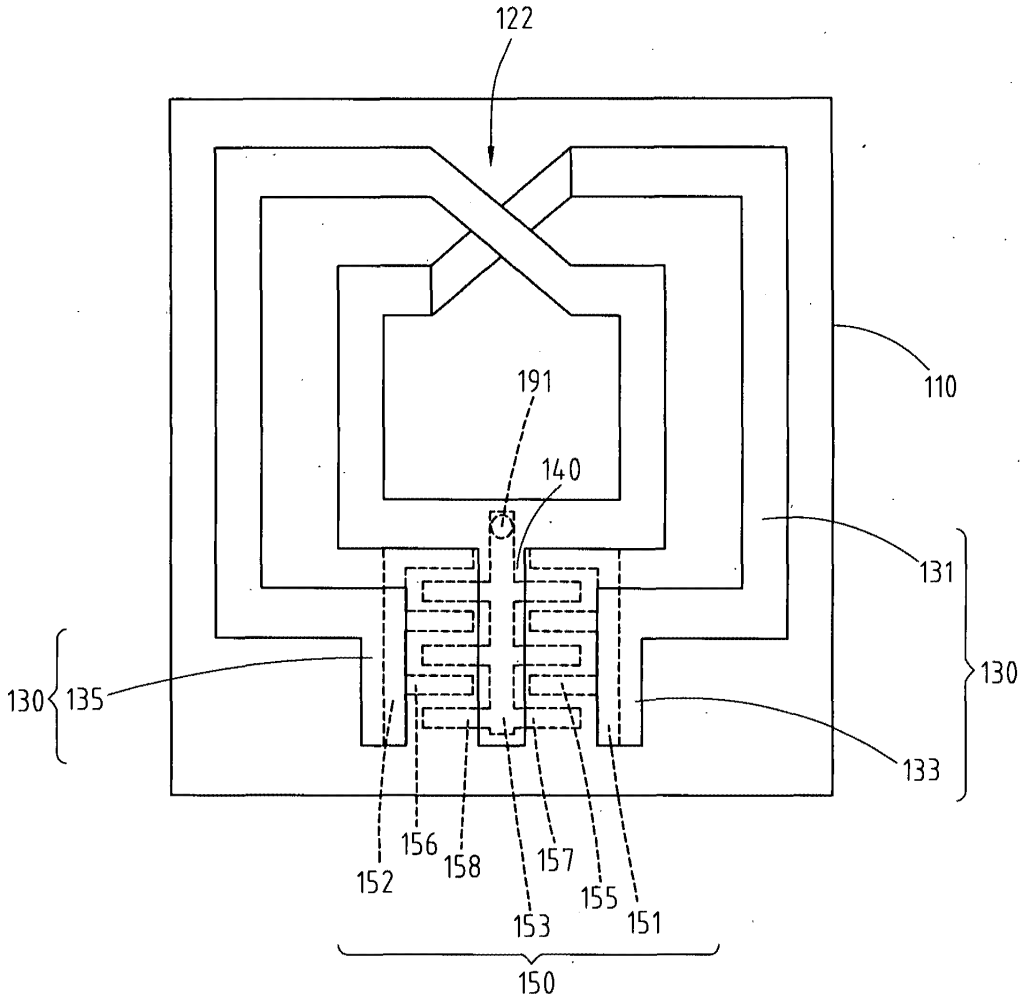
第5圖

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第6圖

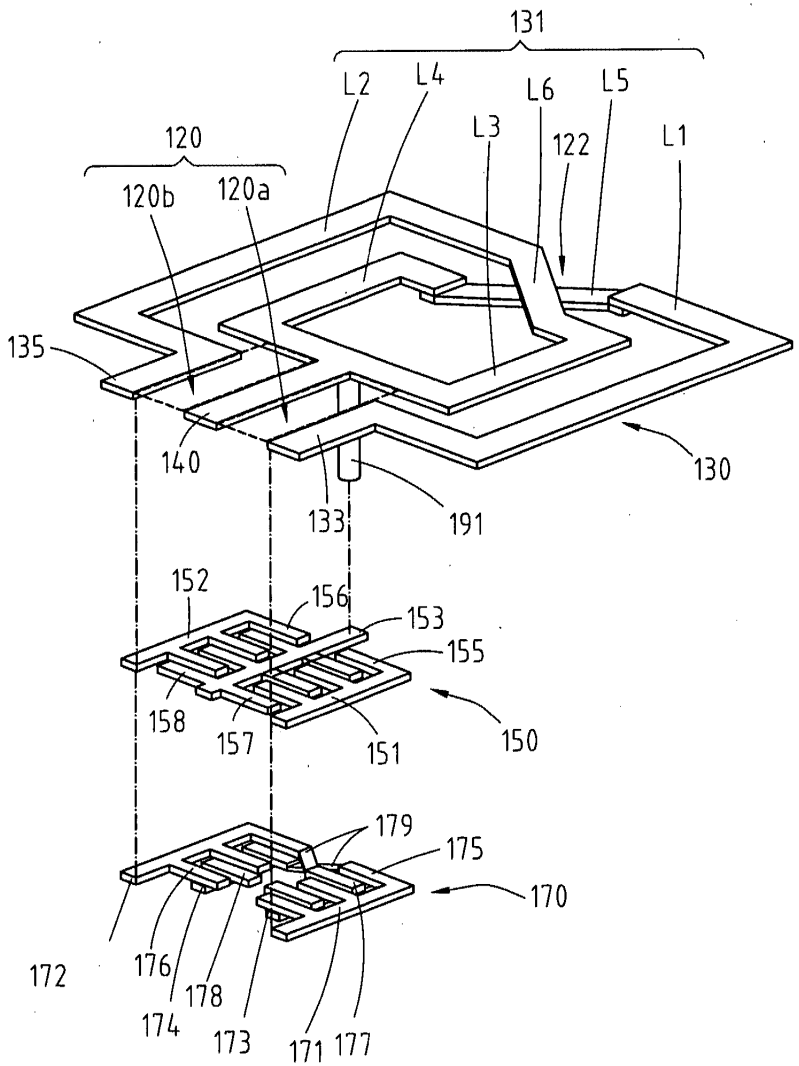
第7圖



第8圖

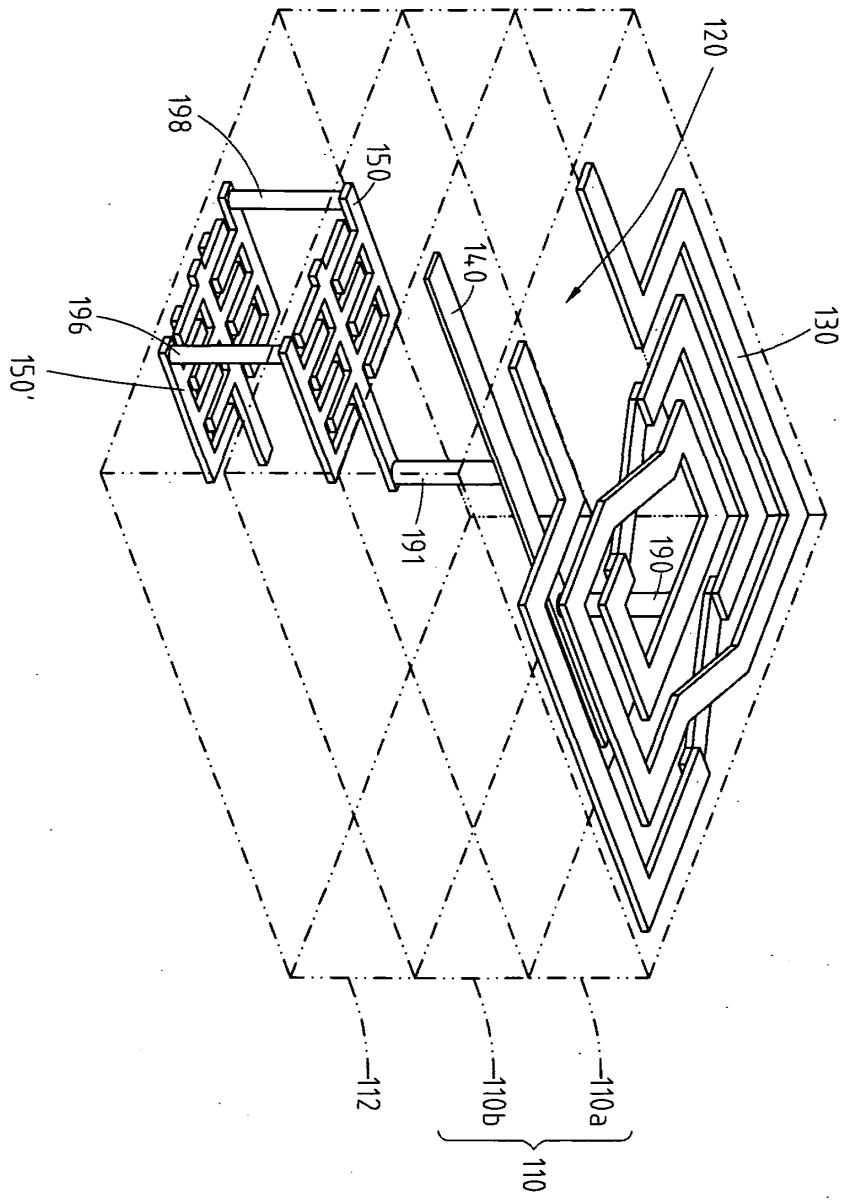
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申請案號：103113947



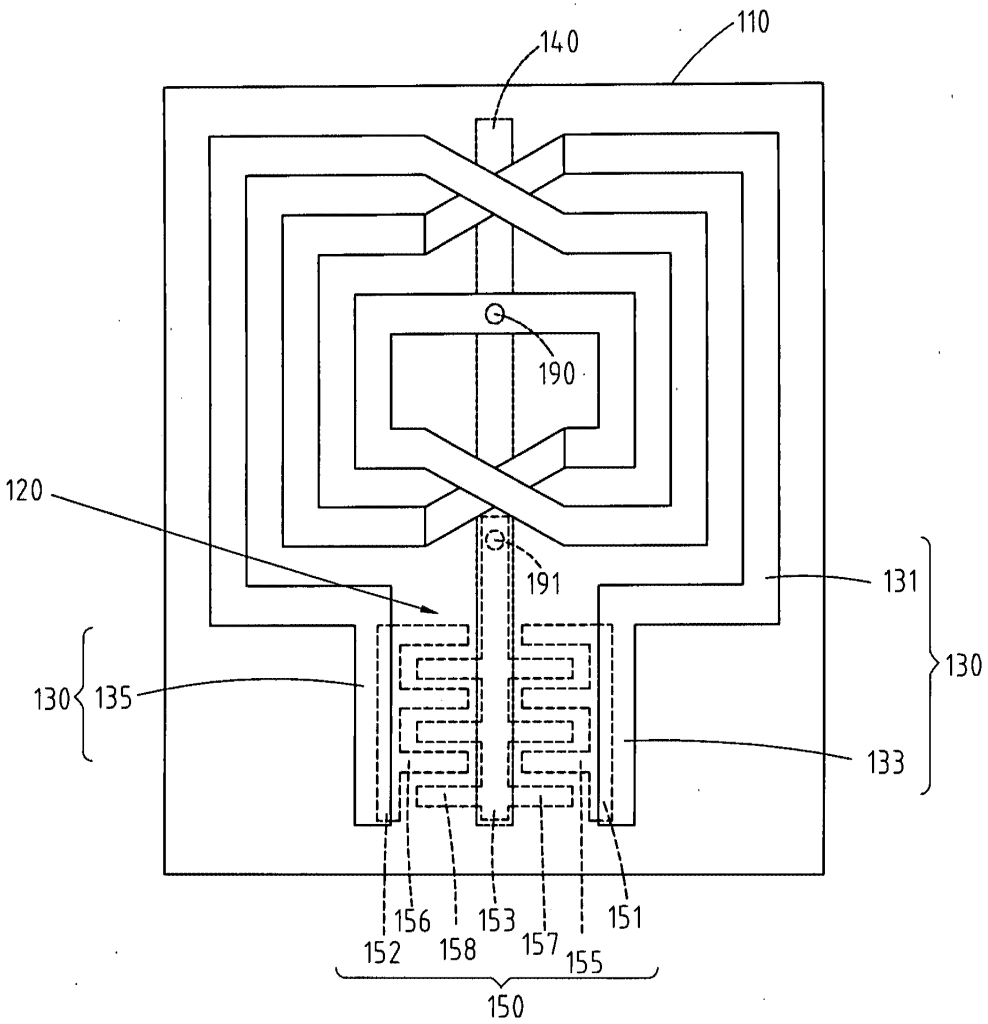
第9圖

申請案號：103113947



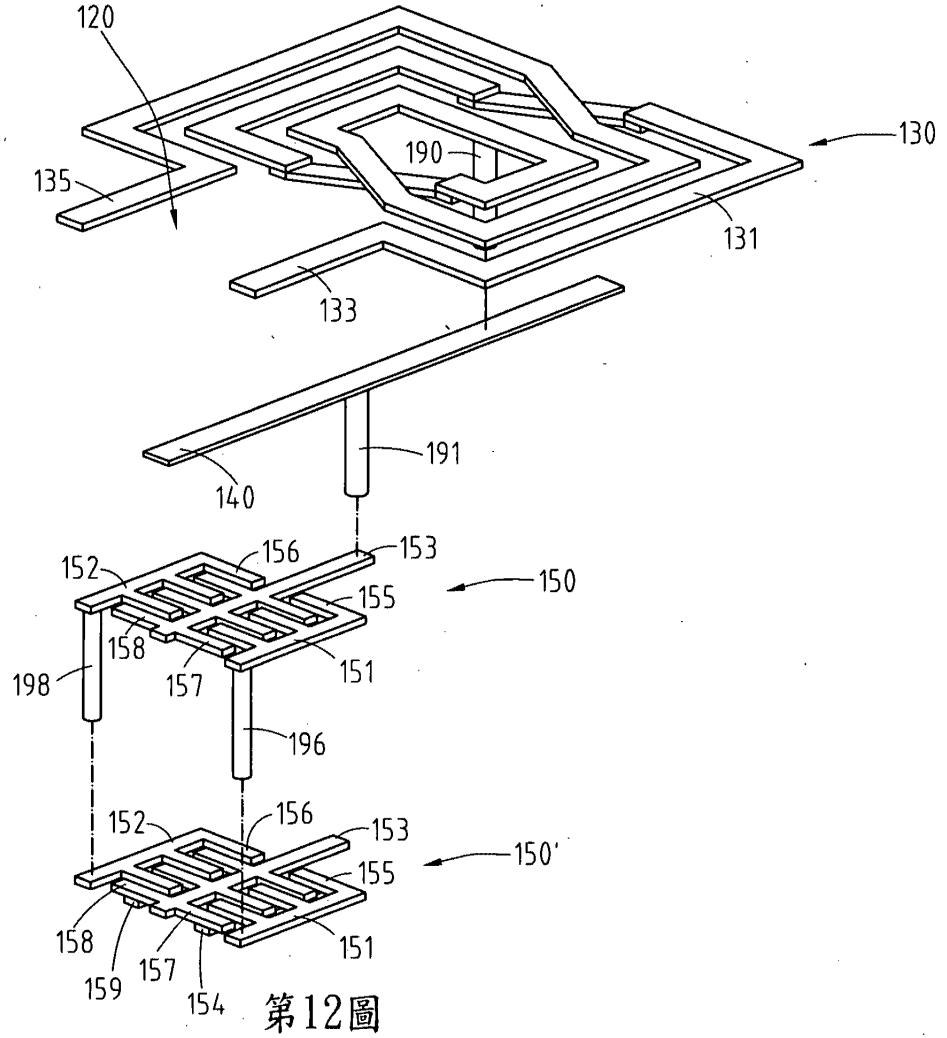
第10圖

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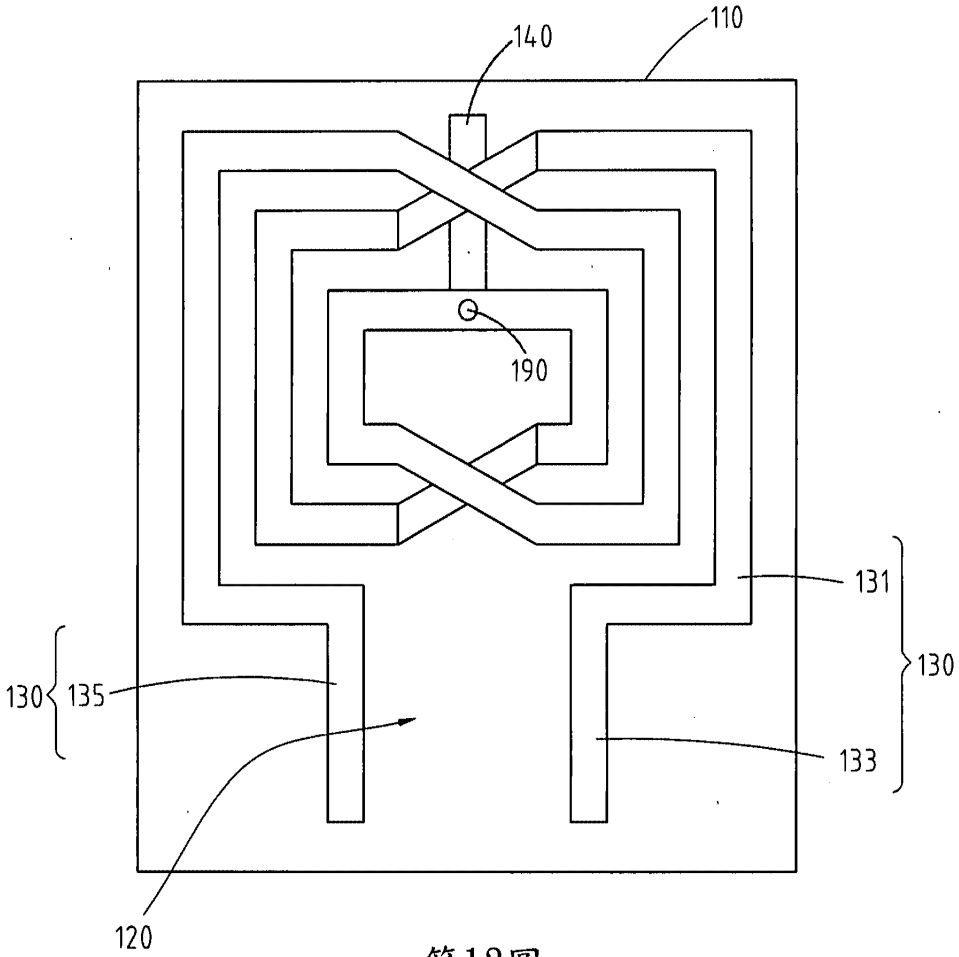
第11圖

申請案號：103113947



第12圖

申請案號：103113947

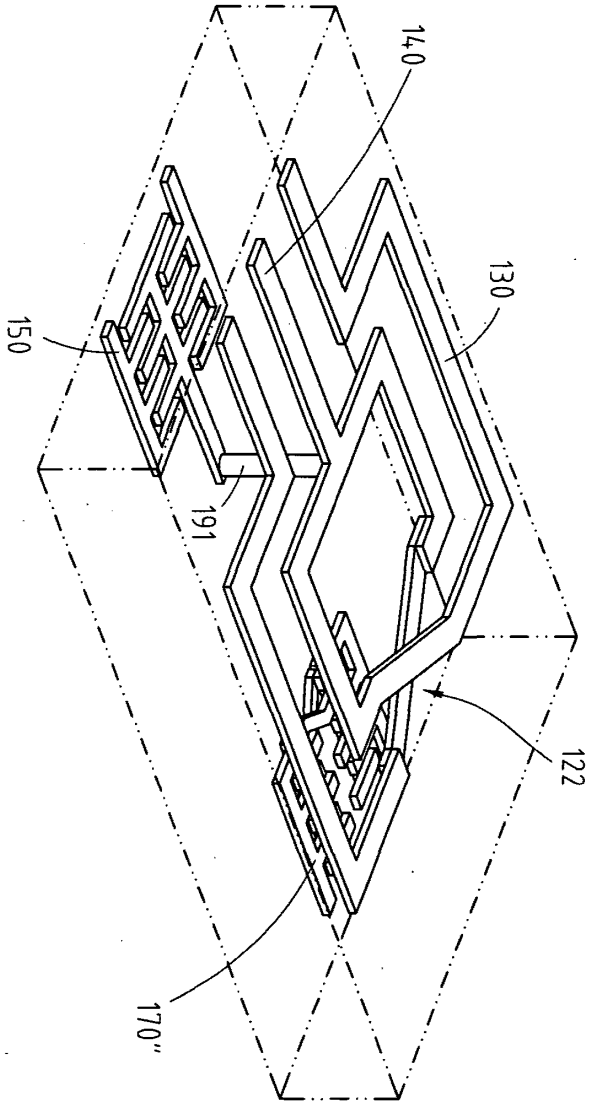


第13圖

申請案號：103113947
1032023134-0

第14圖

第15圖



第16圖

第17圖

OPAP
JUL 2 8 2014
PATENT & TRADEMARK OFFICE

IFW

PTO/SB/21 (10-08)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	14/338,904
Filing Date	Jul 23, 2014
First Named Inventor	YEN, Hsiao-Tsung
Art Unit	
Examiner Name	
Attorney Docket Number	5750/0265PUS1

ENCLOSURES *(Check all that apply)*

- [ ] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment / Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [X] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] Landscape Table on CD
- [ ] After Allowance communication to (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please identify below):

Remarks

A certified copy of Taiwan 103113947 filed on 16 Apr 2014 is attached hereto. A claim for priority to this application is made under 35 U.S.C. § 119.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Muncy, Geissler, Olds & Lowe, P.C.		
Signature			
Printed name	Joe McKinney Muncy		
Date	July 25, 2014	Reg. No.	32334

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature			
Typed or printed name	Joe McKinney Muncy	Date	July 25, 2014

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 14338904 Document Date: 07/23/2014

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

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Form Revision Date: August 26, 2013

PTO/AIA/15 (03-13)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	5750/0265PUS1
First Named Inventor	YEN, Hsiao-Tsung
Title	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT...
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✓] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [✓] **Specification** [*Total Pages* 25] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [✓] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 17]
6. **Inventor's Oath or Declaration** [*Total Pages* 3] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. [✓] Newly executed (original or copy)
   b. [ ] A copy from a prior application (37 CFR 1.63(d))
7. [✓] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. [ ] Computer Readable Form (CRF)
   b. [ ] Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s)) Name of Assignee Realtek Semiconductor Corp.
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [✓] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [✓] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [ ] **Other:**

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[✓] The address associated with Customer Number: 60601 **OR** [ ] Correspondence address below

Name	Muncy, Geissler, Olds & Lowe, PLLC				
Address	4000 Legato Rd., Suite 310				
City	Fairfax	State	VA	Zip Code	22033
Country	US	Telephone	703-621-7140	Email	mailroom@mg-ip.com

Signature	FLOYD E. CANFIELD REG. NO. 69,151		Date	July 23, 2014
Name (Print/Type)	Joe McKinney Muncy		Registration No. (Attorney/Agent)	32,334

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/17 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
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FEE TRANSMITTAL

Complete if known	
Application Number	NEW
Filing Date	July 23, 2014
First Named Inventor	YEN, Hsiao-Tsung
Examiner Name	
Art Unit	
Practitioner Docket No.	5750/0265PUS1

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($) 1600

METHOD OF PAYMENT (check all that apply)

☐ Check ☑ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-3828 Deposit Account Name: MG-IP

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	U ($)	S ($)	M ($)	U ($)	S ($)	M ($)	U ($)	S ($)	M ($)	Fees Paid ($)
Utility	280	140*	70	600	300	150	720	360	180	1600
Design	180	90	45	120	60	30	460	230	115	
Plant	180	90	45	380	190	95	580	290	145	
Reissue	280	140	70	600	300	150	2,160	1,080	540	
Provisional	260	130	65	0	0	0	0	0	0	

* The $140 small entity status filing fee for a utility application is further reduced to $70 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	Undiscounted Fee ($)	Small Entity Fee ($)	Micro Entity Fee ($)
Each claim over 20 (including Reissues)	80	40	20
Each independent claim over 3 (including Reissues)	420	210	105
Multiple dependent claims	780	390	195

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
10	-20 or HP =	0	x _____	=	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
1	-3 or HP =	0	x _____	=	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round **up** to a whole number) x	_____ =	_____

4. OTHER FEE(S) **Fees Paid ($)**

Non-English specification, $130 fee (no small or micro entity discount) _____

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY

Signature	FLOYD (Attorney/Agent) REG. NO. 69,151	Registration No. (Attorney/Agent) 32,334	Telephone 703-621-7140
Name (Print/Type)	Joe McKinney Muncy		Date July 23, 2014

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

CROSS-REFERENCES TO RELATED APPLICATIONS

This non-provisional application claims priority under 35 U.S.C. § 119(a) on Patent Application No. 103113947 filed in Taiwan, R.O.C. on 2014/04/16, the entire contents of which are hereby incorporated by reference.

BACKGROUND

Technical Field

The present invention relates to a semiconductor device, and in particular to a semiconductor device with an inductor-capacitor (LC) resonant circuit.

Related Art

With the development trend of integration of multiple functions of an electronic product, more and more circuit elements need to be designed integrally in a semiconductor chip.

A typical semiconductor integrated circuit includes a silicon substrate. More than one insulation layer is arranged on the substrate, more than one metal layer of is arranged in the insulation layer, and the metal layers may be formed with a built-in part of a chip by means of a semiconductor fabrication process. Therefore, in order to reduce the volume of an electronic product, various electronic elements are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).

In design of circuits such as a filter, a network impedance matching circuit, a voltage-controlled oscillator (VCO), a transmitting and receiving module circuit, an LC resonant circuit is usually used for signal transmission or filtration. At a high frequency, a signal may pass through the insulation layer and leak to the silicon substrate, resulting in

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transmission loss. Therefore, how to design an embedded LC resonant circuit to achieve a further compact size with no or lesser influencing effects of signal transmission or filtration is one of the projects that are researched by relevant circuit designers with continuous effort.

SUMMARY

In an embodiment, a semiconductor device with an LC resonant circuit includes a first insulation layer, an inductor component, and a capacitor component. The inductor component includes a coil-conductor segment and two extension-conductor segments. The coil-conductor segment and the extension-conductor segments are located on a same surface of the first insulation layer, and the extension-conductor segments are coupled to two ends of the coil-conductor segment, respectively. The extension-conductor segments are arranged at an interval, and extend outwards relative to the coil-conductor segment. A first region is defined by the extension-conductor segments and the coil-conductor segment, and the capacitor component is arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

In conclusion, according to the semiconductor device with an LC resonant circuit, the LC resonant circuit may be integrated on a semiconductor substrate by means of a three-dimensional (3D) die stacking technology, and a resonant capacitor is arranged corresponding to an input/output part of the inductor component, so as to reduce generation of phase noise, arrangement of interconnecting wires, and an overall size. In some embodiments, in the semiconductor device with an LC resonant circuit according to the present invention, other electronic components are further arranged corresponding to the input/output part or a staggered part of the inductor component, so as to further reduce generation of phase noise, arrangement of interconnecting wires, and the overall size.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given herein below for illustration only, and thus are not limitative of the present invention,

and wherein:

FIG. 1 is a perspective view of a semiconductor device with an LC resonant circuit according to a first embodiment of the present invention;

FIG. 2 is a top view of the semiconductor device shown in FIG. 1;

FIG. 3 is an exploded view of the semiconductor device shown in FIG. 1;

FIG. 4 is a perspective view of a semiconductor device with an LC resonant circuit according to a second embodiment of the present invention;

FIG. 5 is a top view of the semiconductor device shown in FIG. 4;

FIG. 6 is an exploded view of the semiconductor device shown in FIG. 4;

FIG. 7 is a perspective view of a semiconductor device with an LC resonant circuit according to a third embodiment of the present invention;

FIG. 8 is a top view of the semiconductor device shown in FIG. 7;

FIG. 9 is an exploded view of the semiconductor device shown in FIG. 7;

FIG. 10 is a perspective view of a semiconductor device with an LC resonant circuit according to a fourth embodiment of the present invention;

FIG. 11 is a top view of the semiconductor device shown in FIG. 10;

FIG. 12 is an exploded view of the semiconductor device shown in FIG. 10;

FIG. 13 is a perspective view of a semiconductor device with an LC resonant circuit according to a fifth embodiment of the present invention;

FIG. 14 is a perspective view of a semiconductor device with an LC resonant circuit according to a sixth embodiment of the present invention;

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FIG. 15 is a top view of the semiconductor device shown in FIG. 14;

FIG. 16 is a perspective view of a semiconductor device with an LC resonant circuit according to a seventh embodiment of the present invention; and

FIG. 17 is a top view of the semiconductor device shown in FIG. 16.

DETAILED DESCRIPTION

In order to clearly show all elements, sometimes an insulation layer may be shown in the drawings in a transparent or omitted manner, and therefore is not limitative of the disclosure. Moreover, the terms such as "first", "second", "third", and "fourth" described hereinafter are used for distinguishing indicated elements rather than sequencing or limiting the difference of the indicated elements or limiting the scope of the present invention.

FIG. 1 to FIG. 3 are schematic views of a semiconductor device with an LC resonant circuit according to a first embodiment of the present invention, and FIG. 4 to FIG. 6 are schematic views of a semiconductor device with an LC resonant circuit according to a second embodiment of the present invention.

Referring to FIG. 1 to FIG. 6, the semiconductor device with an LC resonant circuit includes an insulation layer 110 (hereinafter referred to as a first insulation layer 110), an inductor component 130, and a capacitor component 150.

The inductor component 130 and the capacitor component 150 are formed by patterning two metal layers located on two opposite surfaces of the first insulation layer 110. In other words, the inductor component 130 is formed on (or above) an upper surface of the first insulation layer 110, and the capacitor component 150 is formed on (or below) a lower surface of the first insulation layer 110. The inductor component 130 and the capacitor component 150 may be formed by more than one metal layer.

The inductor component 130 includes a coil-conductor segment 131 and two extension-conductor segments 133 and 135. The coil-conductor segment 131 serves as an

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induction part of an inductor for the electromagnetic induction. The extension-conductor segments 133 and 135 serve as an input/output part for receiving or transmitting a signal. The coil-conductor segment 131 and the extension-conductor segments 133 and 135 are located on the upper surface of the first insulation layer 110. The extension-conductor segments 135 may be located on the upper surface of the first insulation layer 110 or in the first insulation layer 110.

The two extension-conductor segments 133 and 135 are arranged at an interval and coupled to two ends of the coil-conductor segment 131, respectively. In other words, the two extension-conductor segments 133 and 135 are directly connected to the two ends of the coil-conductor segment 131 and extend outwards relative to the coil-conductor segment 131 from the two ends of the coil-conductor segment 131. In other words, the extension-conductor segments 133 and 135 extend in a direction away from the coil-conductor segment 131.

Here, the two extension-conductor segments 133 and 135 are located at a same side of the coil-conductor segment 131, and a region 120 (hereinafter referred to as a first region 120) is defined by the two extension-conductor segments 133 and 135 and the coil-conductor segment 131.

The capacitor component 150 is arranged, corresponding to the first region 120, on the other surface (that is, a lower surface of the first insulation layer 110), opposite to the inductor component 130, of the first insulation layer 110 in an embedded manner. In other words, the capacitor component 150 is located below the first region 120 and spaced by the first insulation layer 110 from the inductor component 130.

In some embodiments, the inductor component 130 may be of a flat spiral or stacking helical shape (that is, multiple metal layers are connected to form a helical shape). The coil-conductor segment 131 and the two extension-conductor segments 133 and 135 are formed by patterning multiple metal layers.

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In other embodiments, referring to FIG. 4 to FIG. 6, the inductor component 130 is a symmetric inductor having geometric symmetry. Here, the coil-conductor segment 131 and the two extension-conductor segments 133 and 135 are single wiring paths separately. The two extension-conductor segments 133 and 135 are approximately parallel to each other. The extension-conductor segment 133 is joined to a first end of the coil-conductor segment 131 and is approximately perpendicular to a joining position between the extension-conductor segment 133 and the coil-conductor segment 131. The extension-conductor segment 135 is joined to a second end of the coil-conductor segment 131 and is approximately perpendicular to a joining part of the extension-conductor segment 135 and the coil-conductor segment 131. The first region 120 is located between the coil-conductor segment 131 and the two extension-conductor segments 133 and 135. Here, the coil-conductor segment 131 and the two extension-conductor segments 133 and 135 are formed by pattering a metal layer.

Here, the capacitor component 150 may be entirely and correspondingly arranged between the outer sides of the extension-conductor segments 133 and 135. Moreover, the capacitor component 150 may also be correspondingly located between the outer side of one of the extension-conductor segments 133 and 135 and an inner side of the other of the extension-conductor segments 133 and 135. In addition, the capacitor component 150 may be entirely and correspondingly arranged between the inner sides of the extension-conductor segments 133 and 135.

The capacitor component 150 may be in a single-ended (as shown in FIG. 1 to FIG. 3) or differential (as shown in FIG. 4 to FIG. 6) form. All capacitors in the capacitor component 150 in these embodiments share a same metal layer; however, the present invention is not limited thereto. Capacitors connected in parallel may be formed by using various different metal layers to increase a capacitance value, or a semiconductor transistor capacitor arranged below the capacitor component 150 may be further connected in parallel or used.

In some embodiments, referring to FIG. 1 to FIG. 3, the capacitor component 150 includes two connecting segments 151 and 152 (hereinafter referred to as a first connecting

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segment 151 and a second connecting segment 152) and a plurality of electrode segments 155 and 156 (hereinafter referred to as a first electrode segment 155 and a second electrode segment 156).

The electrode segments 155 and 156 serve as electrode plates of the capacitor, capacitive induction is generated between the electrode segments 155 and 156. The connecting segments 151 and 152 are used for receiving or transmitting a signal. The connecting segments 151 and 152 and the electrode segments 155 and 156 are all formed on the lower surface of the first insulation layer 110. Here, the connecting segments 151 and 152 and the electrode segments 155 and 156 are formed by patterning a second metal layer.

The first connecting segment 151 and the second connecting segment 152 extend corresponding to the extension-conductor segments 133 and 135 in the same direction. The first electrode segment 155 and the second electrode segment 156 are located below the first region 120.

In some embodiments, the first connecting segment 151 is arranged, corresponding to the extension-conductor segment 133, on (or below) the lower surface of the first insulation layer 110, and the second connecting segment 152 is arranged corresponding to, the extension-conductor segment 135, on (or below) the lower surface of the first insulation layer 110. The first connecting segment 151 may be located below the extension-conductor segment 133 and is overlapped with the extension-conductor segment 133. The second connecting segment 152 may be located below the extension-conductor segment 135 and is overlapped with the extension-conductor segment 135. In some embodiments, the first connecting segment 151 and/or the second connecting segment 152 are located below the first region 120 and correspondingly located between the two extension-conductor segments 133 and 135 rather than being overlapped with the corresponding extension-conductor segment 133/135.

Here, one end of the first electrode segment 155 is coupled to a side edge of the first connecting segment 151, and the other end of the first electrode segment 155 extends laterally

relative to the coupled first connecting segment 151. The first electrode segment 151 extends towards the second connecting segment 152 from the side edge of the first connecting segment 151. In some embodiments, the first electrode segment 155 is approximately perpendicular to the first connecting segment 151.

One end of the second electrode segment 156 is coupled to a side edge of the second connecting segment 152, and the other end of the second electrode segment 156 extends laterally relative to the coupled second connecting segment 152. The second electrode segment 156 extends towards the first connecting segment 151 from the side edge of the second connecting segment 152. In some embodiments, the second electrode segment 156 is approximately perpendicular to the second connecting segment 152.

In some embodiments, the first electrode segment 155 and the second electrode segment 156 are arranged in a staggered manner.

In some embodiments, referring to FIG. 4 to FIG. 6, the capacitor component 150 includes three connecting segments 151, 152, and 153 (hereinafter referred to as the first connecting segment 151, the second connecting segment 152, and a third connecting segment 153) and a plurality of electrode segments 155, 156, 157, and 158 (hereinafter referred to as the first electrode segment 155, the second electrode segment 156, a third electrode segment 157, and a fourth electrode segment 158).

The electrode segments 155, 156, 157, and 158 serve as electrode plates of the capacitor, and capacitive induction is generated between the electrode segments 155 and 157 and between the electrode segments 156 and 158. The connecting segments 151 and 152 are used for receiving or transmitting a signal, and the connecting segment 153 is used for, for example, being grounded. The connecting segments 151, 152, and 153 and the electrode segments 155, 156, 157, and 158 are all formed on the lower surface of the first insulation layer 110. Here, the connecting segments 151, 152, and 153 and the electrode segments 155, 156, 157, and 158 are all formed by patterning the second metal layer.

The first connecting segment 151, the second connecting segment 153, and the third connecting segment 153 extend in a same direction. The third connecting segment 153 is located between the first connecting segment 151 and the second connecting segment 153 and located below the first region 120. The first electrode segment 155, the second electrode segment 156, the third electrode segment 157, and the fourth electrode segment 158 are located below the first region 120. The arrangement manner of the first connecting segment 151 and the second connecting segment 152 is approximately the same as the manner discussed above, and therefore is no longer elaborated.

Here, the first electrode segment 155 and the third electrode segment 157 are paired, and the second electrode segment 156 and the fourth electrode segment 158 are paired.

One end of the first electrode segment 155 is coupled to the side edge of the first connecting segment 151, and the other end of the first electrode segment 155 extends laterally relative to the coupled first connecting segment 151. The first electrode segment 151 extends towards the second connecting segment 152 and the third connecting segment 153 from the side edge of the first connecting segment 151 and is located between the first connecting segment 151 and the third connecting segment 153. In some embodiments, the first electrode segment 155 is approximately perpendicular to the first connecting segment 151.

One end of the second electrode segment 156 is coupled to the side edge of the second connecting segment 152, and the other end of the second electrode segment 156 extends laterally relative to the coupled second connecting segment 152. The second electrode segment 156 extends towards the first connecting segment 151 and the third connecting segment 153 from the side edge of the second connecting segment 152 and is located between the second connecting segment 152 and the third connecting segment 153. In some embodiments, the second electrode segment 156 is approximately perpendicular to the second connecting segment 152.

One end of the third electrode segment 157 is coupled to a side edge, near the first

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connecting segment 151, of the third connecting segment 153, and the other end of the third electrode segment 157 extends laterally relative to the coupled third connecting segment 153. The third electrode segment 157 extends towards the first connecting segment 151 from the side edge of the third connecting segment 153 and is located between the first connecting segment 151 and the third connecting segment 153. In some embodiments, the third electrode segment 157 is approximately perpendicular to the third connecting segment 153. In this embodiment, the first electrode segment 155 and the third electrode segment 157 are arranged in a staggered manner.

One end of the fourth electrode segment 158 is coupled to a side edge, near the second connecting segment 152, of the third connecting segment 153, and the other end of the fourth electrode segment 158 extends laterally relative to the coupled third connecting segment 153. The fourth electrode segment 158 extends towards the second connecting segment 152 from the side edge of the third connecting segment 153 and is located between the second connecting segment 152 and the third connecting segment 153. In some embodiments, the fourth electrode segment 158 is approximately perpendicular to the third connecting segment 153. In this embodiment, the fourth electrode segment 158 and the second electrode segment 156 are arranged in a staggered manner.

In some embodiments, the electrode segments 155, 156, 157, and 158 of the capacitor component 150 may be correspondingly configured outwards relative to the coil-conductor segment 131 from the joining part between the extension-conductor segments 133 and 135 and the coil-conductor segment 131, for example, shown in FIG. 1 to FIG. 6. In some embodiments, the electrode segments 155, 156, 157, and 158 of the capacitor component 150 may also be correspondingly configured outwards relative to the coil-conductor segment 131 from the outer side of a second loop (starting from the outer side) of the coil-conductor segment 131, for example, as shown in FIG. 7 to FIG. 9. In some embodiments, the electrode segments 155, 156, 157, and 158 may also be completely located below the first region 120 and correspondingly located between the two extension-conductor segments 133 and 135.

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In some embodiments, referring to FIG. 7 to FIG. 12, the semiconductor device further includes an electronic component and another insulation layer 112 (hereinafter referred to as a second insulation layer 112). The electronic component may be an embedded electronic element such as another capacitor component 150' (as shown in FIG. 10 to FIG. 12), a transistor component 170 (as shown in FIG. 7 to FIG. 9), a diode component or a resistor component.

The electronic component is sandwiched between the first insulation layer 110 and the second insulation layer 112. The electronic component is arranged, corresponding to the first region 120, on the other surface, opposite to the capacitor component, of the second insulation layer 112. In other words, the capacitor component 150 is located on the upper surface of the second insulation layer 112, while the electronic component is located on the lower surface of the second insulation layer 112.

The electronic component is located on a circuit layer which is below the first region 120 and different from the circuit layer on which the capacitor component 150 is located. Here, the electronic component is formed by patterning a third metal layer on the lower surface of the second insulation layer 112.

Here, the electronic component may be entirely and correspondingly arranged between the outer sides of the extension-conductor segments 133 and 135. Moreover, the electronic component may also be correspondingly located between the outer side of one of the extension-conductor segments 133 and 135 and the inner outer side of the other of the extension-conductor segments 133 and 135. In addition, the electronic component may be further entirely and correspondingly arranged between the inner sides of the extension-conductor segments 133 and 135.

In some embodiments, when the electronic component is the transistor component 170 (referring to FIG. 7 to FIG. 9), the transistor component 170 includes two connecting segments 171 and 172, two semiconductor segments 173 and 174, and a plurality of electrode segments 175, 176, 177, and 178. The transistor component 170 may be a transistor or

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transistor capacitor operating at different ranges.

The connecting segments 171 and 172 and the electrode segments 175, 176, 177, and 178 are located on the lower surface of the second insulation layer 112. In some embodiments, the connecting segments 171 and 172 and the electrode segments 175, 176, 177, and 178 are formed by patterning the third metal layer located on the lower surface of the second insulation layer 112. The semiconductor segments 173 and 174 are formed by patterning a semiconductor material layer below the third metal layer.

The connecting segments 171 and 172 extend corresponding to the extension-conductor segments 133 and 135 in a same direction, respectively, and the semiconductor segments 172 and 173 and the electrode segments 175, 176, 177, and 178 are located below the first region 120. In some embodiments, the connecting segment 171 is overlapped with the corresponding extension-conductor segment 133, and the connecting segment 172 is overlapped with the corresponding extension-conductor segment 135. Furthermore, the connecting segment 171 and/or the connecting segment 172 may also be located below the first region 120 and correspondingly located between the two extension-conductor segments 133 and 135 rather than being overlapped with the corresponding extension-conductor segments 133 and 135.

One end of the electrode segment 175 is coupled to the side, near the connecting segment 172, of the connecting segment 171, and the other end of the electrode segment 175 extends towards the connecting segment 172. The electrode segment 177 and the electrode segment 175 extend in a same direction, and the electrode segment 177 is arranged at the side edge of the electrode segment 175 at an interval. When a plurality of electrode segments 175 and/or a plurality of electrode segments 177 are adopted, the electrode segments 175 and 177 are arranged in a staggered manner.

One end of the electrode segment 176 is coupled to the side, near the connecting segment 177, of the connecting segment 172, and the other end of the electrode segment 176 extends towards the connecting segment 171. The electrode segment 178 and the electrode segment

176 extend in a same direction, and the electrode segment 178 is arranged at the side edge of the electrode segment 176 at an interval. When a plurality of electrode segments 176 and/or a plurality of electrode segments 178 are adopted, the electrode segments 176 and 178 are arranged in a staggered manner.

The semiconductor segment 173 is located below the electrode segments 175 and 177 and extends in the configuration direction of the electrode segments 175 and 177. In some embodiments, the extension direction of the semiconductor segment 173 is approximately perpendicular to the extension direction of the electrode segments 175 and 177.

The semiconductor segment 174 is located below the electrode segments 176 and 178 and extends in the configuration direction of the electrode segments 176 and 178. In some embodiments, the extension direction of the semiconductor segment 174 is approximately perpendicular to the extension direction of the electrode segments 176 and 178.

Furthermore, the transistor component 170 may further include one or more bridged segments 179, and the one or more bridged segments 179 are located on the lower surface of the second insulation layer 112. In some embodiments, the one or more bridge segments 179 may also be formed by patterning the third metal layer. The two ends of the one or more bridge segments 179 are coupled to the electrode segments 175 and 178 respectively or coupled to the electrode segments 176 and 177 respectively.

In some embodiments, referring to FIG. 10 to FIG. 12, when the electronic component is the capacitor component 150', except being arranged on the lower surface of the second insulation layer 112, the configuration relationship of the capacitor component 150' may be approximately the same as that of the capacitor component 150.

Here, the structures of various embedded electronic elements are well known to in the field, and therefore are no longer elaborated.

In some embodiments, the inductor component 130 may adopt one turn, as shown in FIG. 4 to FIG. 6, or the inductor component 130 may also adopt two turns (as shown in FIG. 1 to

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FIG. 3 and FIG. 7 to FIG. 9), or three turns (as shown in FIG. 10 to FIG. 13), or more turns.

In some embodiments, the first region 120 may be limited between the two extension-conductor segments 133 and 135, such as shown in FIG. 6. In some embodiments, the first region 120 may be limited between the two extension-conductor segments 133 and 135 and the coil-conductor segment 131, as shown in FIG. 9.

For example, referring to FIG. 4 to FIG. 6, when the inductor component 130 adopts one turn, the first region 120 is sandwiched in a space between the two extension-conductor segments 133 and 135. Referring to FIG. 7 to FIG. 9, when the inductor component 130 adopts multiple turns, the first region 120 is sandwiched in a space between the two extension-conductor segments 133 and 135 and the second loop (starting from the outer side) of the coil-conductor segment 131, that is, the space is surrounded by the two extension-conductor segments 133 and 135 and the second loop of the coil-conductor segment 131.

In some embodiments, referring to FIG. 7 to FIG. 9, when the inductor component 130 adopts multiple turns, the coil-conductor segment 131 includes a plurality of semi-loop lines L1, L2, L3, and L4 and at least one pair of staggered parts. The illustration is provided below by using an example of two turns.

The semi-loop lines L1, L2, L3, and L4 may be distinguished to be two first semi-loop lines L1 and L3 and two second semi-loop lines L2 and L4, and each pair of staggered parts have two staggered guide lines L5 and L6.

The first semi-loop lines L1 and L3 and the extension-conductor segment 133 are located at a same side, and the second semi-loop lines L2 and L4 and the extension-conductor segment 135 are located at a same side.

One end of the first semi-loop line L1 is coupled to the extension-conductor segment 133, and the other end of the first semi-loop line L1 is coupled to one end of the staggered guide line L5. The other end of the staggered guide line L5 is coupled to one end of the second

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semi-loop line L4, and the other end of the second semi-loop line L4 is coupled to one end of the first semi-loop line L3. The other end of the first semi-loop line L3 is coupled to one end of the staggered guide line L6, and the other end of the staggered guide line L6 is coupled to one end of the second semi-loop line L2. The other end of the semi-loop line L2 is coupled to the extension-conductor segment 135.

The staggered guide lines L5 and L6 are staggered to each other, and another region 122 (hereinafter referred to as a second region 122) is defined by the other sides of the staggered guide lines L5 and L6.

Here, referring to FIG. 14 to FIG. 17, an electronic component corresponding to the second region 122 may be further arranged on the other surface, opposite to the inductor component 130, of the first insulation layer 110 (i.e. the lower surface of the insulation layer 110) in an embedded manner. The electronic component corresponding to the second region 122 may be an embedded electronic element such as another capacitor component 150" (as shown in FIG. 14 and FIG. 15), the transistor component 170" (as shown in FIG. 16 and FIG. 17), a diode component or a resistor component. Here, the structure of the embedded electronic element is well known in the field, and therefore is no longer elaborated.

In some embodiments, the second region 122 is a hollow region, that is, a region without wiring located at an outer side of the staggered parts at the outermost side.

In some embodiments, referring to FIG. 7 to FIG. 17, the semiconductor device may further include a tap segment 140. The tap segment 140 is electrically connected to the coil-conductor segment 131, so that the tap segment 140 and the inductor component 130 form a tapped inductor. The tap segment 140 may be used for an electrical connection to a fixed potential, thereby providing a direct-current path, and/or a power supply, and/or grounding. The tap segment 140 is providing both a DC voltage path for inductor and a AC ground node for capacitors under or close to the inductor.

In some embodiments, referring to FIG. 7 to FIG. 9, FIG. 16, and FIG. 17, the tap

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segment 140 is formed on the upper surface of the first insulation layer 110, and the tap segment 140 and the inductor component 130 may be formed by patterning a same metal layer.

The tap segment 140 is arranged between the extension-conductor segments 133 and 135 and extends outwards in the same direction as the extension-conductor segments 133 and 135. Here, the tap segment 140 divides the first region 120 into a first hollow region 120a and a second hollow region 120b. The first hollow region 120a is a region without wiring surrounded by the extension-conductor segment 133, the coil-conductor segment 131, and the tap segment 140. The second hollow region 120b is a region without wiring surrounded by the extension-conductor segment 135, the coil-conductor segment 131, and the tap segment 140.

When the tap segment 140 does not exist between the extension-conductor segments 133 and 135, the first region 120 is a hollow region, that is, is a region without wiring, as shown in FIG. 1 to FIG. 6 and FIG. 10 to FIG. 15.

In some embodiments, referring to FIG. 7, FIG. 10, and FIG. 14, the first insulation layer 100 may be divided into an upper layer 110a and a lower layer 110b. The tap segment 140 is sandwiched between the upper layer 110a and the lower layer 110b. In other words, the inductor component 130 is formed on an upper surface of the upper layer 110a, while the tap segment 140 is located on a lower surface (that is, an upper surface of the lower layer 110b) of the upper layer 110a. Here, the tap segment 140 and the inductor component 130 are located on different circuit layers. The tap segment 140 may be formed by patterning a fourth metal layer on the lower surface (that is, the upper surface of the lower layer 110b) of the upper layer 110a.

In some embodiments, any two of the electronic elements such as the inductor component 130, the tap segment 140, the capacitor components 150, 150', and 150", the transistor component 170 and 170', or other embedded electronic elements located on different circuit layers may be electrically conducted via a connection of other circuits. In other words, the

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electronic elements located on different circuit layers may be not directly connected through a via.

In some embodiments, referring to FIG. 1 to FIG. 17, any two of the electronic elements such as the inductor component 130, the tap segment 140, the capacitor components 150, 150', and 150", the transistor component 170 and 170', or other embedded electronic elements located on different circuit layers may also be electrically conducted through vias 190, 191, 192, 194, 196, and 198, so that two electronic elements are electrically connected in parallel or in series.

Referring FIG. 7 to FIG. 12, the via 190 is arranged between the tap segment 140 and the coil-conductor segment 131 and is used for electrically connecting the tap segment 140 and the coil-conductor segment 131. In other words, the via 190 penetrates from the upper surface of the upper layer 110a to the lower surface of the upper layer 110a, and enables conduction between the upper surface of the upper layer 110a and the lower surface of the upper layer 110a. One end of the via 190 is coupled to the coil-conductor segment 131, while the other end of the via 190 is coupled to the tap segment 140.

Referring to FIG. 4 to FIG. 9 and FIG. 11 to FIG. 14, the via 191 is arranged between the tap segment 140 and the connecting segment 153 of the capacitor component 150 (or 150'), and is used for electrically connecting the tap segment 140 and the connecting segment 153. In other words, the via 191 penetrates from the upper surface of the first insulation layer 110 to the lower surface of the first insulation layer 110, and enables the conduction between the upper surface of the first insulation layer 110 and the lower surface of the first insulation layer 110. Alternatively, the via 191 penetrates from the upper surface of the lower layer 110b to the lower surface of the lower layer 110b, and enables the conduction between the upper surface of the lower layer 110b and the lower surface of the lower layer 110b. One end of the via 191 is coupled to the coil-conductor segment 131, while the other end of the via 191 is coupled to the tap segment 140.

In some embodiments, the coil-conductor segment 131, the tap segment 140, and the

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connecting segment 153 may be electrically connected through a single via (the via 190 and the via 191 are located at a same vertical position, that is, are coaxial). In other words, the two ends of the via are coupled to the coil-conductor segment 131 and the connecting segment 153 respectively, and the tap segment 140 is coupled to the middle of the via.

Referring to FIG. 1 to FIG. 3, the via 194 is arranged between the extension-conductor segment 135 of the inductor component 130 and the connecting segment 152 of the capacitor component 150 and is used for electrically connecting the inductor component 130 and the capacitor component 150. In other words, the via 194 penetrates from the upper surface of the first insulation layer 110 to the lower surface of the first insulation layer 110, and enables the conduction between the upper surface of the first insulation layer 110 and the lower surface of the first insulation layer 110. One end of the via 194 is coupled to the extension-conductor segment 135, while the other end of the via 194 is coupled to the connecting segment 152.

Referring to FIG. 4 to FIG. 6, the via 192 is arranged between the extension-conductor segment 133 of the inductor component 130 and the connecting segment 151 of the capacitor component 150 and is used for electrically connecting the inductor component 130 and the capacitor component 150. In other words, the via 192 penetrates from the upper surface of the first insulation layer 110 to the lower surface of the first insulation layer 110, and enables the conduction between the upper surface of the first insulation layer 110 and the lower surface of the first insulation layer 110. One end of the via 192 is coupled to the extension-conductor segment 133, while the other end of the via 192 is coupled to the connecting segment 153.

In other words, the two ends of the inductor component 130 are conducted and connected with the two ends of the capacitor component 150 through the via 192 and the via 194 in a differential architecture, respectively.

Referring to FIG. 10 and FIG. 12, the via 196/198 is arranged between the connecting segment 151/152 of the capacitor component 150 and the electronic component (for example,

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the connecting segment 151/152 of the capacitor component 150') arranged below the capacitor component 150 and is used for electrically connecting the capacitor component 150 and the electronic component arranged below the capacitor component 150. In other words, the via 196 penetrates from the upper surface of the second insulation layer 112 to the lower surface of the second insulation layer 112, and enables the conduction between the upper surface of the second insulation layer 112 and the lower surface of the second insulation layer 112. One end of the via 196 is coupled to the connecting segment 151/152, while the other end of the via 196 is coupled to the electronic component (for example, the connecting segment 151/152 of the capacitor component 150') arranged below the capacitor component 150.

In some embodiments, the extension-conductor segment 133 and the connecting segments of all electronic components below the extension-conductor segment 133 may be electrically connected through a single via (the via 192 and the via 196 are located at a same vertical position, that is, are coaxial). For example, the two ends of the via are coupled to the extension-conductor segment 133 of the inductor component 130 and the connecting segment 151 of the capacitor component 150' (or the connecting segment of the transistor component 170) respectively, and the connecting segment 151 of the capacitor component 150 is coupled to the middle of the via.

Similarly, the extension-conductor segment 135 and the connecting segments of all electronic components below the extension-conductor segment 135 may be electrically connected through a single via (the via 194 and the via 198 are located at a same vertical position, that is, are coaxial). For example, the two ends of the via are coupled to the extension-conductor segment 135 of the inductor component 130 and the connecting segment 153 of the capacitor component 150' (or the connecting segment 173 of the transistor component 170) respectively, and the connecting segment 153 of the capacitor component 150 is coupled to the middle of the via.

In some embodiments, the capacitor components 150, 150', and 150" may be capacitors in

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various forms, such as a metal-oxide-metal (MOM) capacitor, a metal-insulator-metal (MIM) capacitor, or a metal-oxide-semiconductor (MOS) capacitor. Here, the structures of the capacitors in various forms are well known in the field. By using the MOS capacitor as an example and referring to FIG. 12, the capacitor component 150' further includes at least one semiconductor segment 154/159 in addition to the members shown in the foregoing embodiments. The semiconductor segment 154 (or 159) is located below the first electrode segment 155 (or 156) and the second electrode segment 157 (or 158) which are staggered at an interval of a dielectric layer, and the extension direction of the semiconductor segment 154/159 is approximately perpendicular to the extension direction of the first electrode segment 155/156 and the second electrode segment 157/158.

Here, the foregoing capacitor components 150, 150', and 150" and the electrode segments 175, 176, 177, and 178 of the transistor component 170 are all represented by a single metal layer in the drawings; however, the present invention is not limited thereto. In consideration of actual circuit demands, the foregoing capacitor components 150, 150', and 150" and the electrode segments 175, 176, 177, and 178 of the transistor component 170 may be formed by a single metal layer or a multi-layer metal stack.

Furthermore, the above-mentioned insulation layers may include one layer or multiple layers of insulating materials formed by one or more semiconductor processes.

In conclusion, in the semiconductor device with an LC resonant circuit according to the present invention, an LC resonant circuit may be integrated on a semiconductor substrate by means of a 3D die stacking technology, and a resonant capacitor is arranged corresponding to an input/output part of an inductor component, so as to reduce generation of phase noise, arrangement of interconnecting wires, and an overall size. In some embodiments, in the semiconductor device with an LC resonant circuit according to the present invention, other electronic components are arranged corresponding to the input/out part or a staggered part of the inductor component, so as to further reduce generation of phase noise, arrangement of interconnecting wires, parasitic RLC (Resistance- Inductance- Capacitance) and an overall

size.

While the disclosure has been described by the way of example and in terms of the preferred embodiments, it is to be understood that the invention need not be limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

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CLAIMS

What is claimed is:

1. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

2. The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

an electronic component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the capacitor component, of the second insulation layer.

3. The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

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4. The semiconductor device with an LC resonant circuit according to claim 1, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the extension-conductor segments in a same direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the electrode segments is coupled to one of the connecting segments, and each of the electrode segments extends laterally relative to the coupled connecting segment.

5. The semiconductor device with an LC resonant circuit according to claim 4, wherein the connecting segments are overlapped with the extension-conductor segments, respectively.

6. The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

a tap segment, electrically connected to the coil-conductor segment;

wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the extension-conductor segments in a same direction, wherein one of the connecting segments is located below the tap segment and overlapped with the tap segment; and

a plurality of electrode segments, located below the first region, wherein one end of each electrode segment is coupled to one of the connecting segments, and each of the electrode segment extends laterally relative to the coupled connecting segment.

7. The semiconductor device with an LC resonant circuit according to claim 1, wherein the coil-conductor segment has a pair of staggered parts, a second region is defined by outer sides of the pair of staggered parts, and the semiconductor device further comprises:

an electronic component, arranged corresponding to the second region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

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8. The semiconductor device with an LC resonant circuit according to claim 7, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

9. The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the extension-conductor segments.

10. The semiconductor device with an LC resonant circuit according to claim 9, wherein the first region is defined between the extension-conductor segments and the coil-conductor segment.

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ABSTRACT

A semiconductor device with an inductor-capacitor (LC) resonant circuit includes a first insulation layer, an inductor component, and a capacitor component. The inductor component includes a coil-conductor segment and two extension-conductor segments. The coil-conductor segment and the extension-conductor segments are located on a same surface of the first insulation layer, and the extension-conductor segments are coupled to two ends of the coil-conductor segment, respectively. The extension-conductor segments are arranged at an interval, and extend outwards relative to the coil-conductor segment. A first region is defined by the extension-conductor segments and the coil-conductor segment, and the capacitor component is arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

COMBINED DECLARATION AND ASSIGNMENT

Title of Invention: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT

As a below named inventor, I hereby declare that:

This declaration is directed to:
☒ The attached application; or
☐ United States application number or PCT international application number _____, filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WHEREAS, REALTEK SEMICONDUCTOR CORP. of No.2, Innovation Rd. II, Hsinchu Science Park, HsinChu, Taiwan, R.O.C., its heirs, successors, legal representatives and assigns (hereinafter designated as the Assignee) is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent(s) that may be granted therefor in the United States of America and ☐ in any foreign countries.

NOW, THEREFORE, in consideration of the sum of Ten Dollars ($10.00) to the undersigned in hand paid, the receipt of which is hereby acknowledged, and other good and valuable consideration, the undersigned has (have) sold, assigned and transferred, and by these presents does sell, assign and transfer unto said Assignee the full and exclusive right to the said invention in the United States of America, its territories, dependencies and possessions and the entire right, title and interest in and to any and all Letters Patent(s) which may be granted therefor in the United States of America, its territories, dependencies and possessions, and if the box above is designated, in any and all foreign countries; and to any and all divisions, reissues,

continuations, conversions and extensions thereof for the full term or terms for which the same may be granted.

The undersigned agree(s) to execute all papers necessary in connection with this application and any continuing, divisional, conversion or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agree(s) to execute all papers necessary in connection with any interference which may be declared concerning this application or continuation, division, conversion or reissue thereof or Letter Patent(s) or reissue patent issued thereon and to cooperate with the Assignee in every way possible in obtaining and producing evidence and proceeding with such interference.

The undersigned agree(s) to execute all papers and documents and to perform any act which may be necessary in connection with claims or provisions of the International Convention for the Protection of Industrial Property or similar agreements.

The undersigned agree(s) to perform all affirmative acts which may be necessary to obtain a grant of a valid United States of America patent(s) or a grant of a valid United States of America and any foreign patent(s) to the Assignee and to vest all rights therein hereby conveyed to said Assignee as fully and entirely as the same would have been held by the undersigned if this Assignment and sale had not been made.

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The undersigned hereby covenant(s) that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment.

In witness whereof, executed by the undersigned on the date(s) opposite the undersigned name(s).

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Signature: Yen, Hsiao-Tsung Date: July 7, 2014

LEGAL NAME OF ADDITIONAL JOINT INVENTOR, IF ANY:

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SIGNATURE of Assignee of Record
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Signature	Jinn-Shing Chen	Date
Name	Chen, Jinn-Shing	Telephone
Title	Executive Vice President	

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

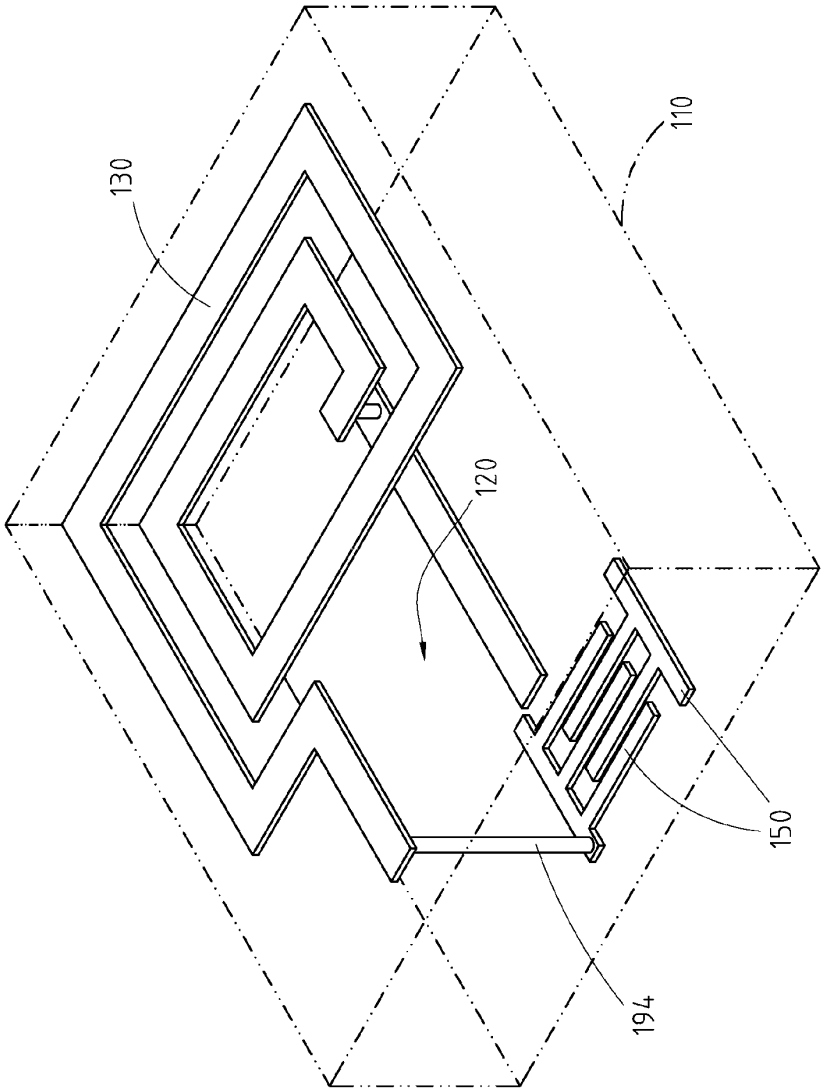


FIG. 1

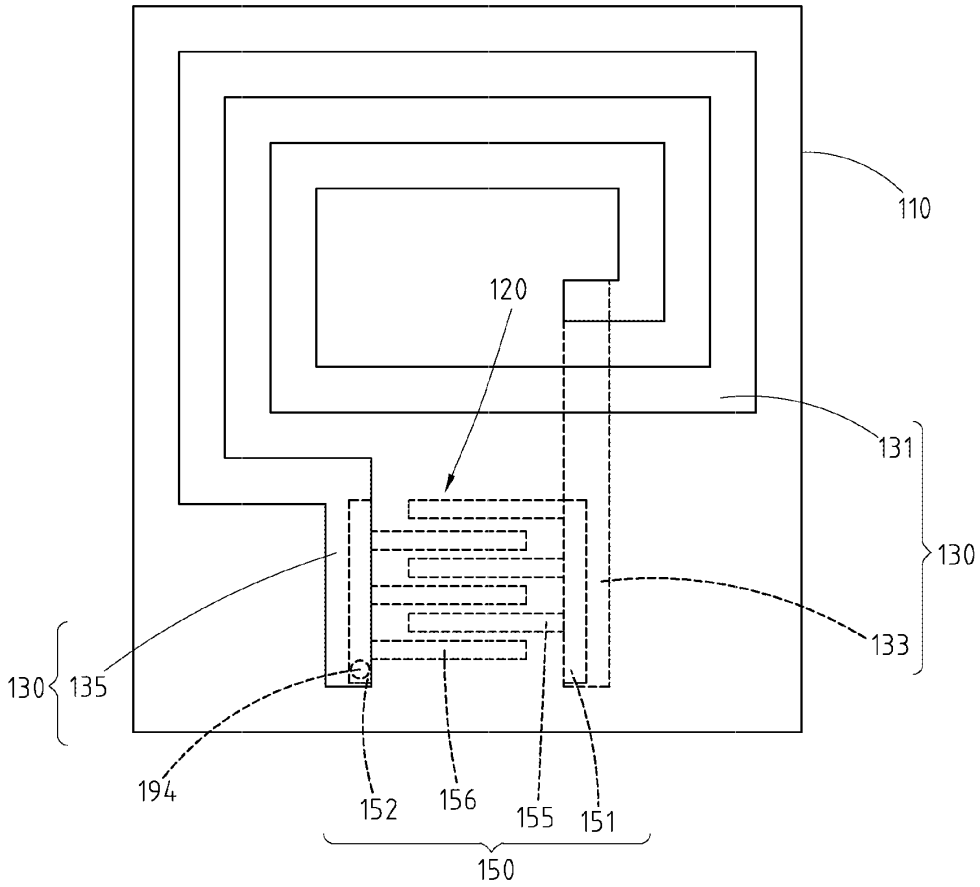


FIG. 2

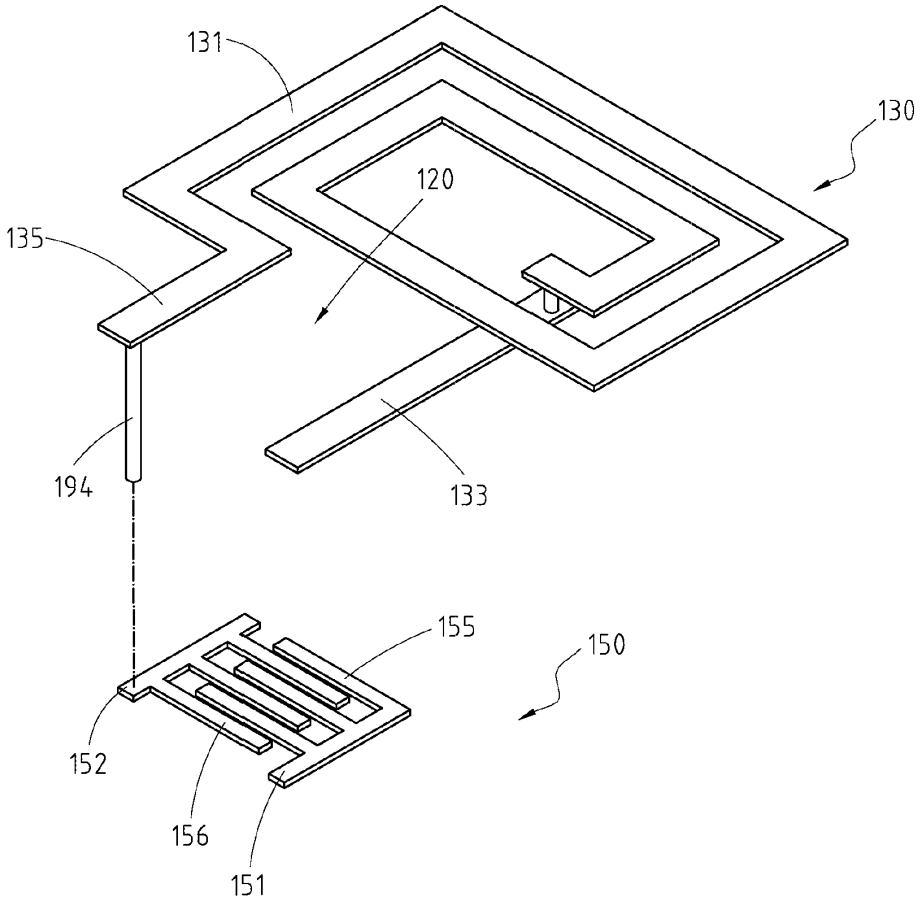


FIG. 3

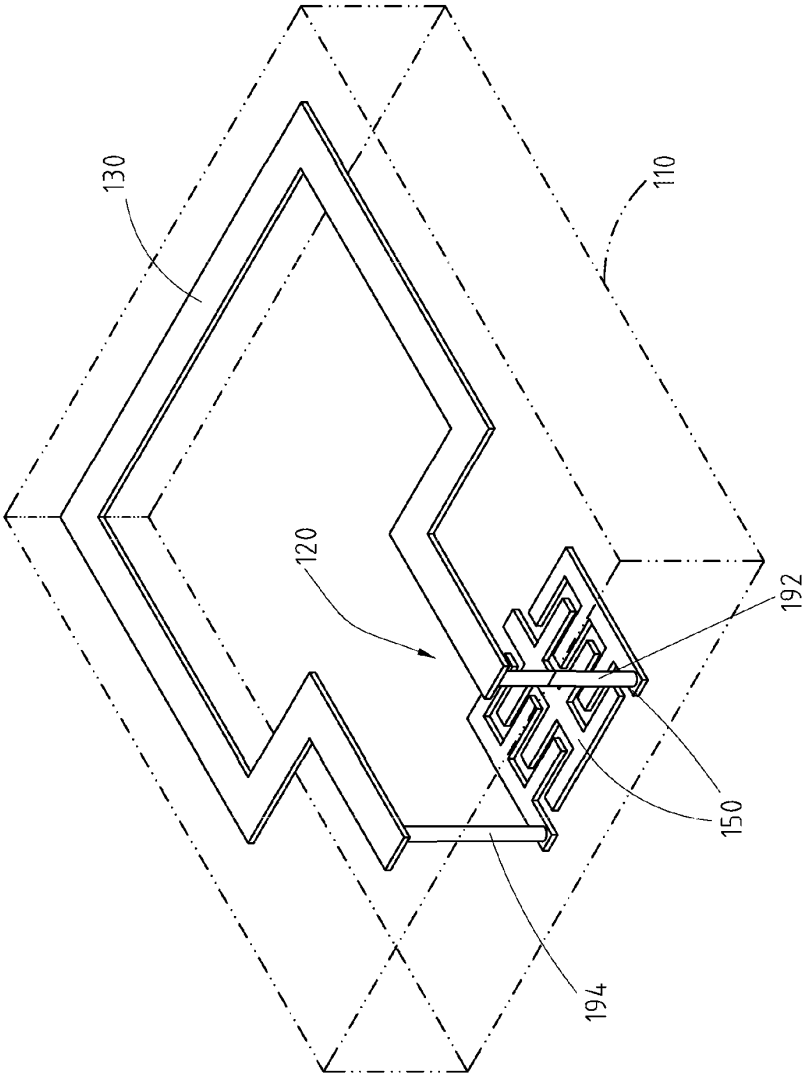


FIG. 4

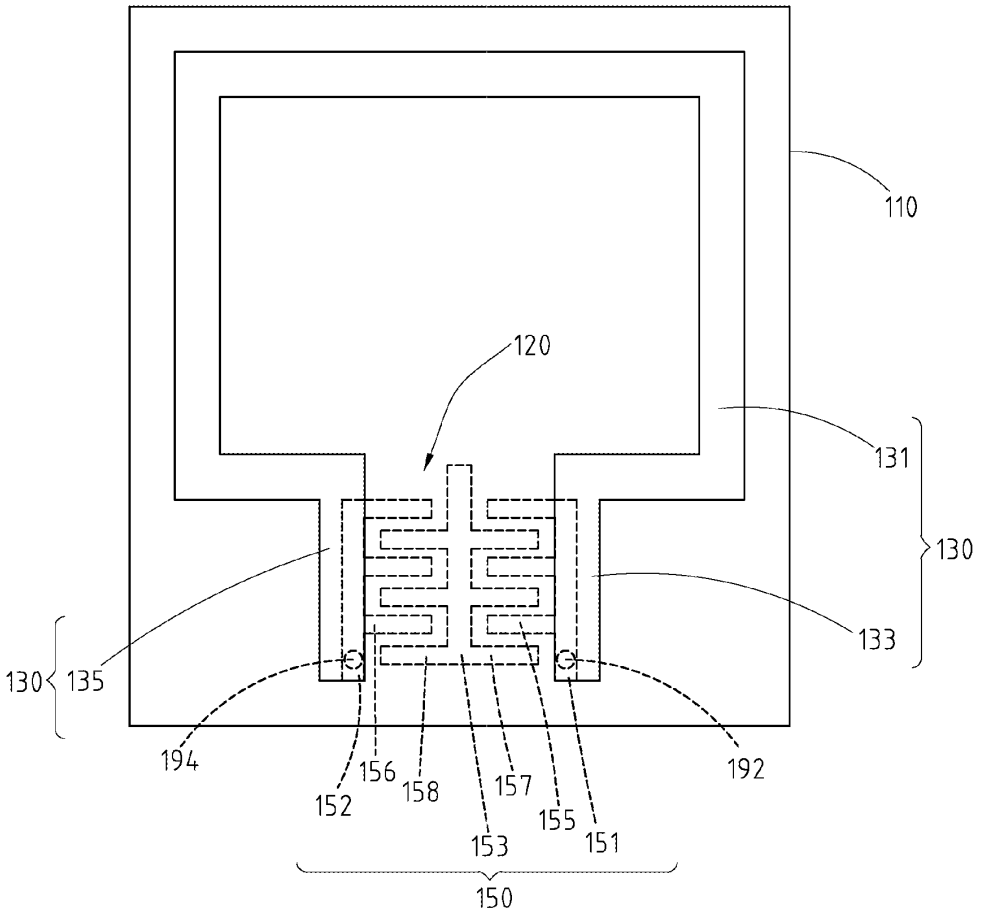

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FIG. 5

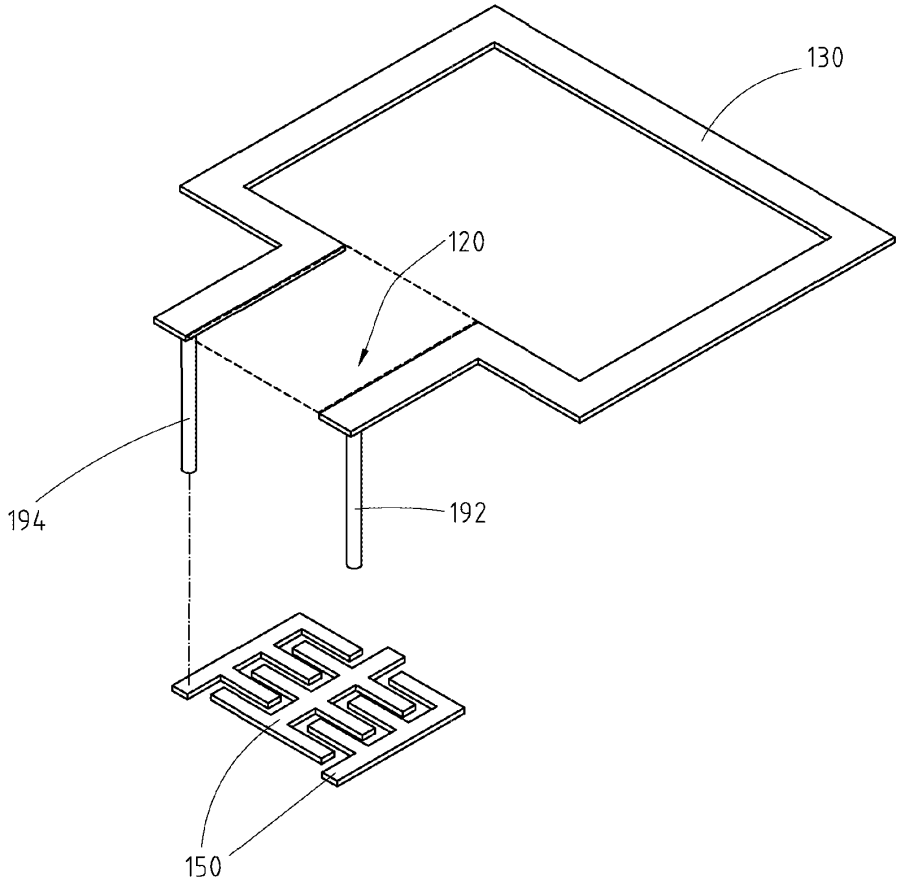


FIG. 6

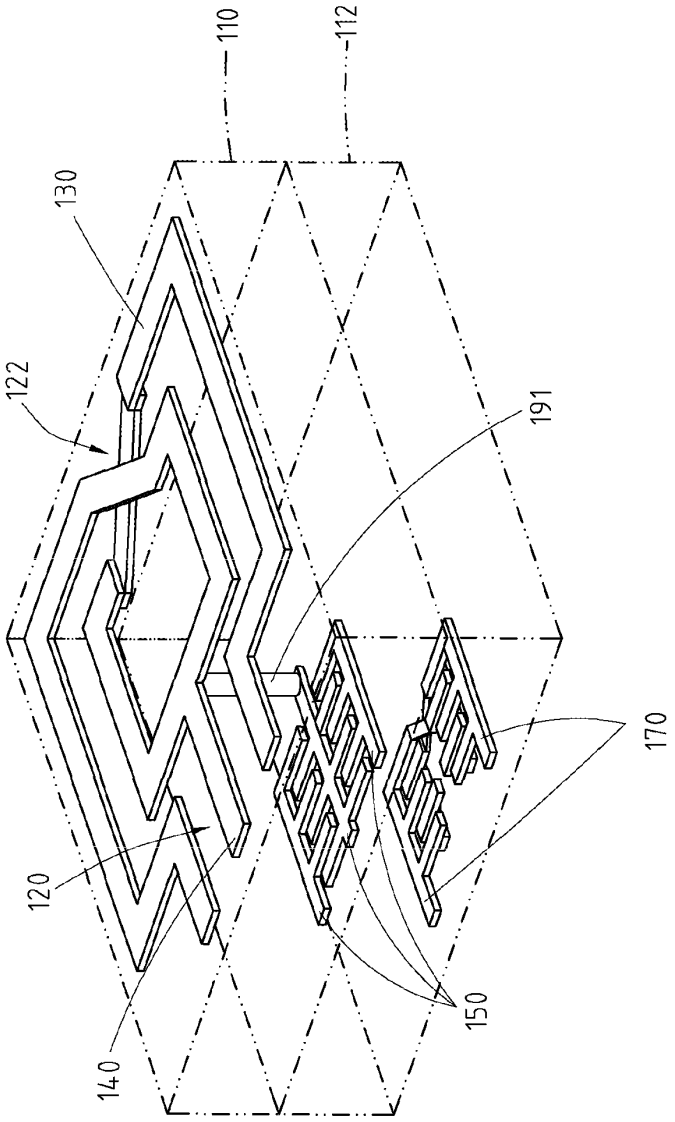


FIG. 7

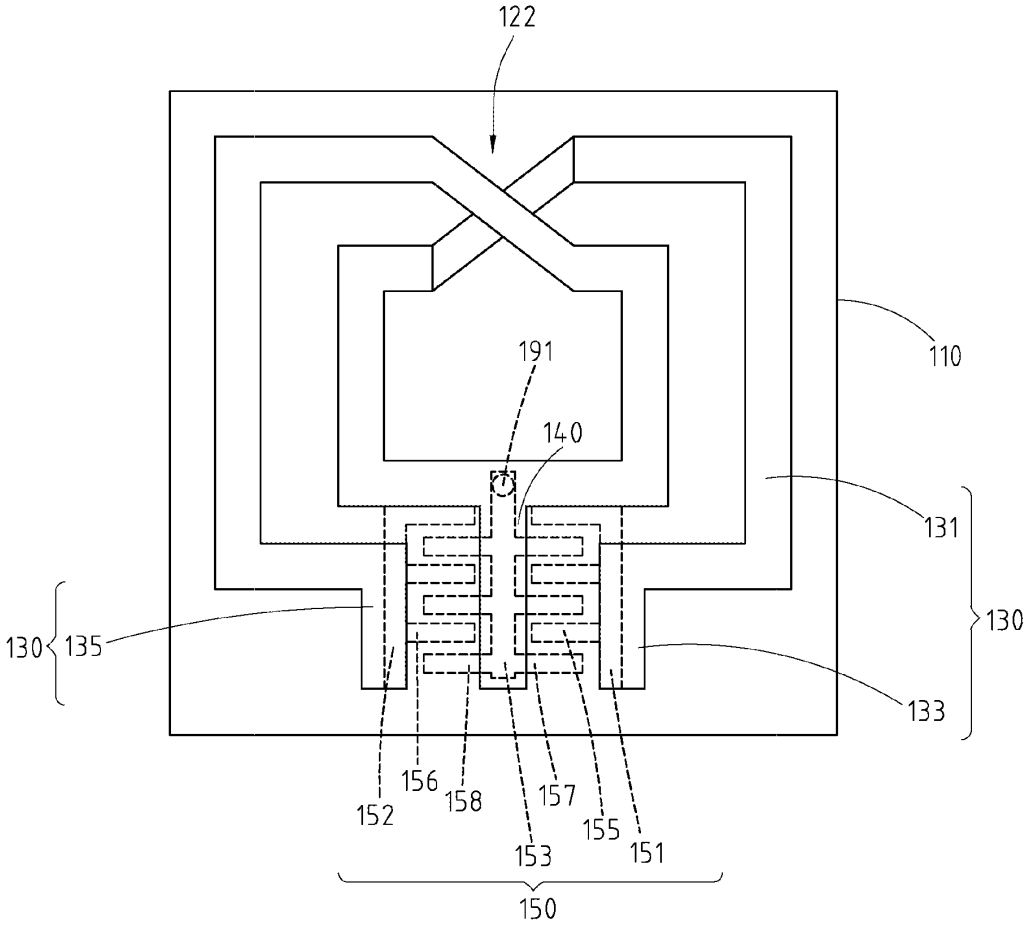

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FIG. 8

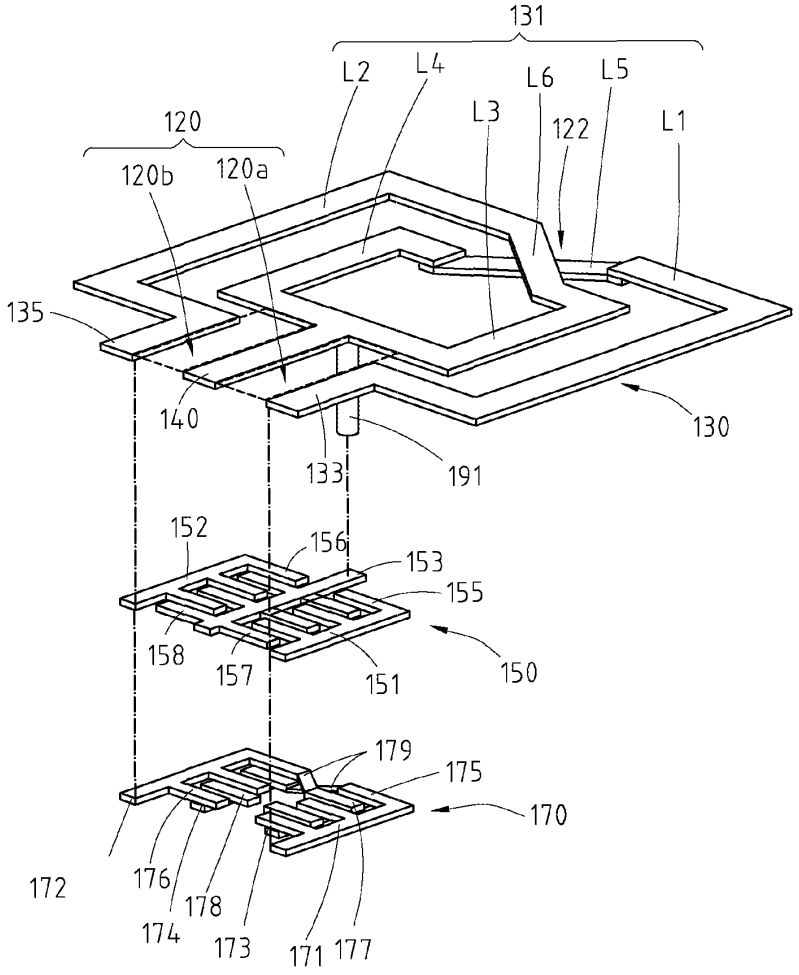

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FIG. 9

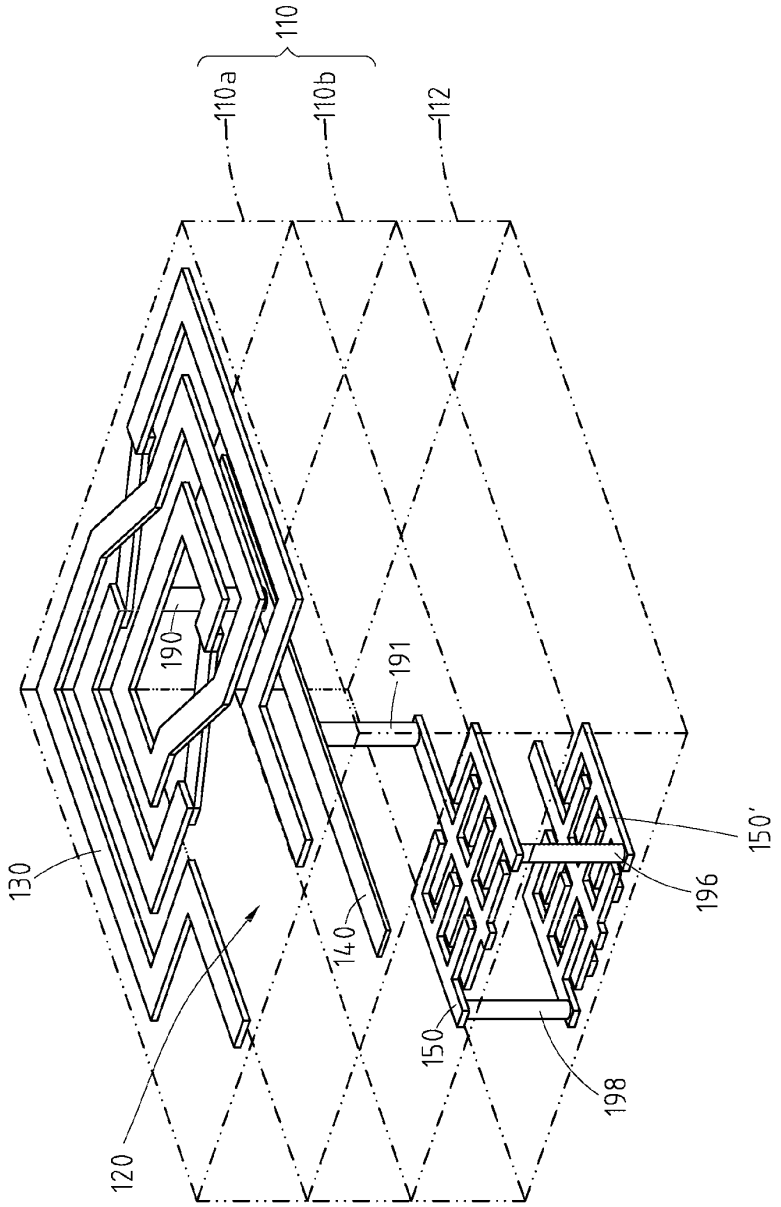


FIG. 10

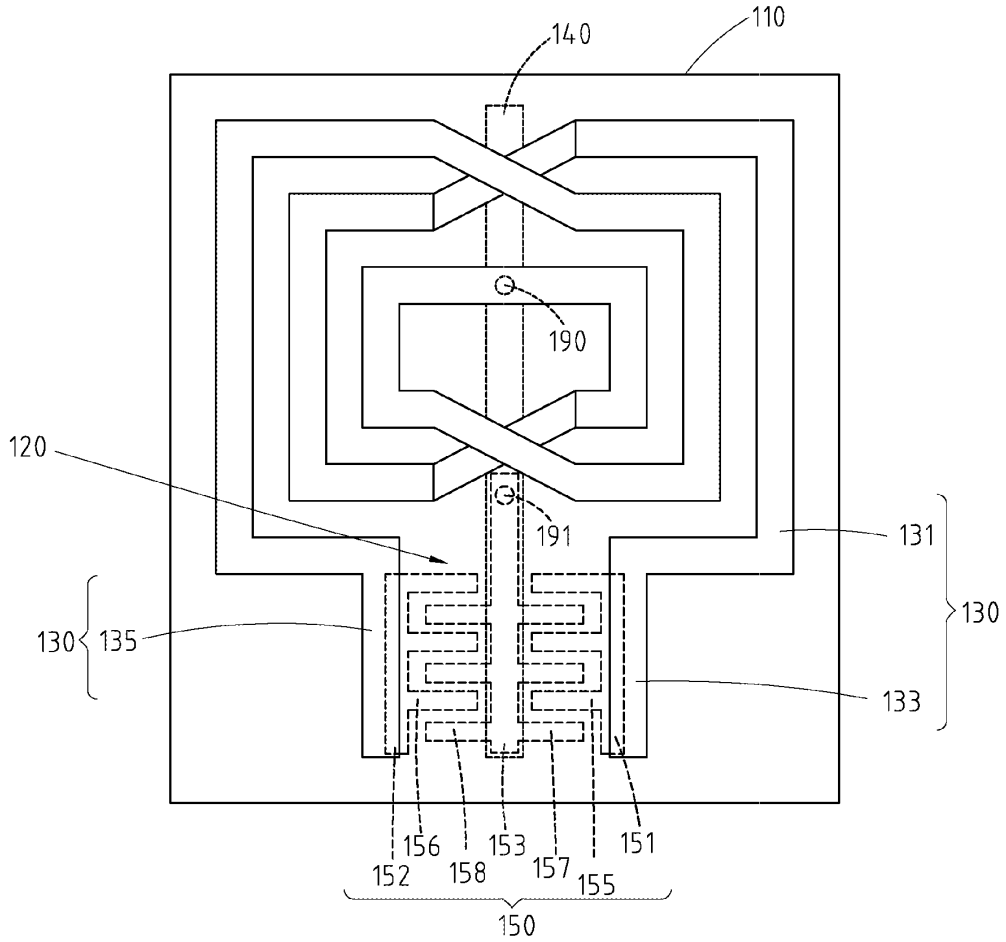

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FIG. 11

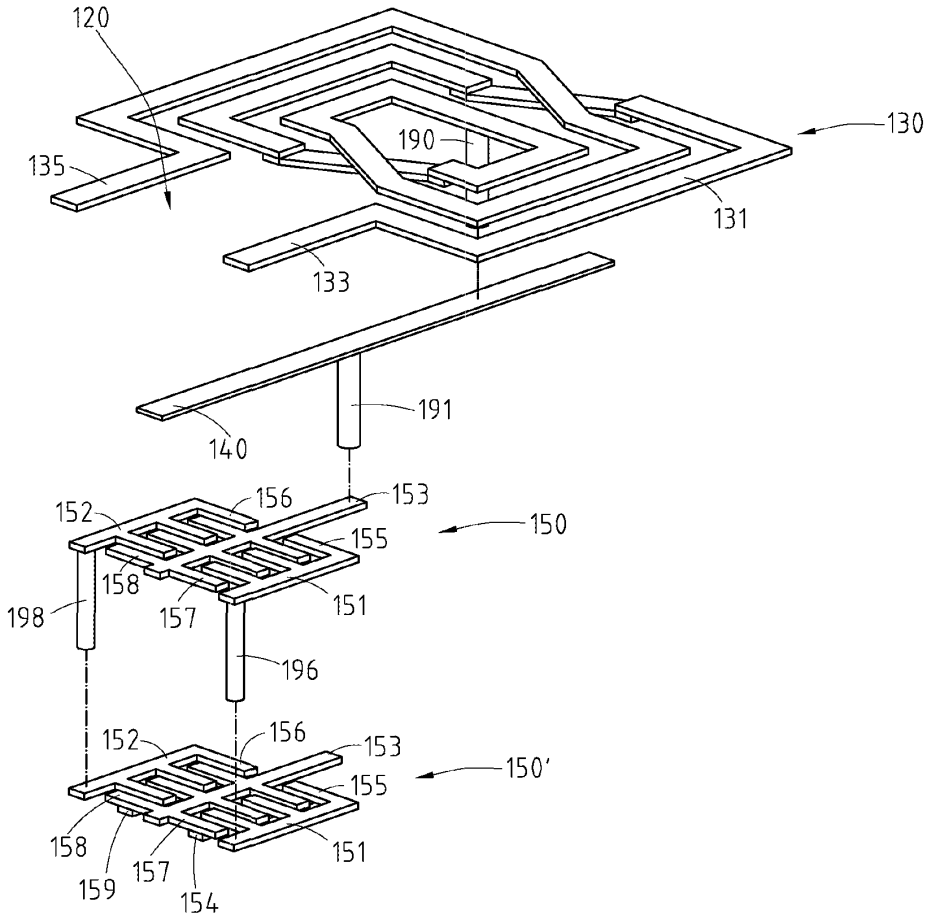

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FIG. 12

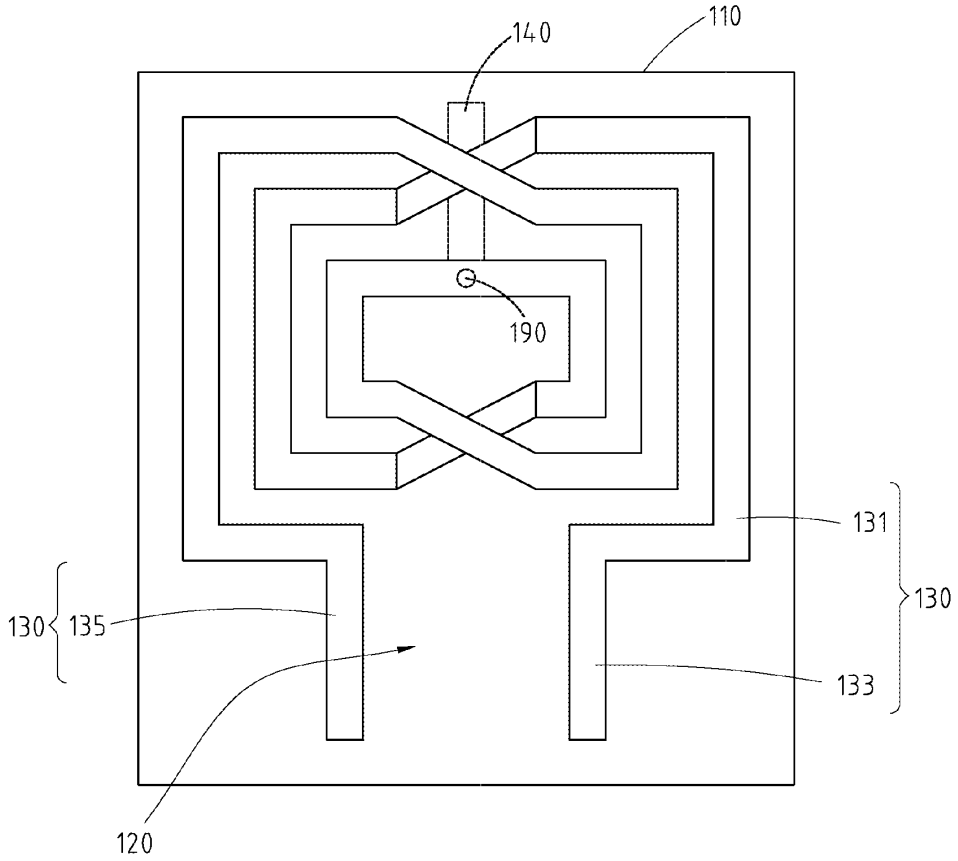


FIG. 13

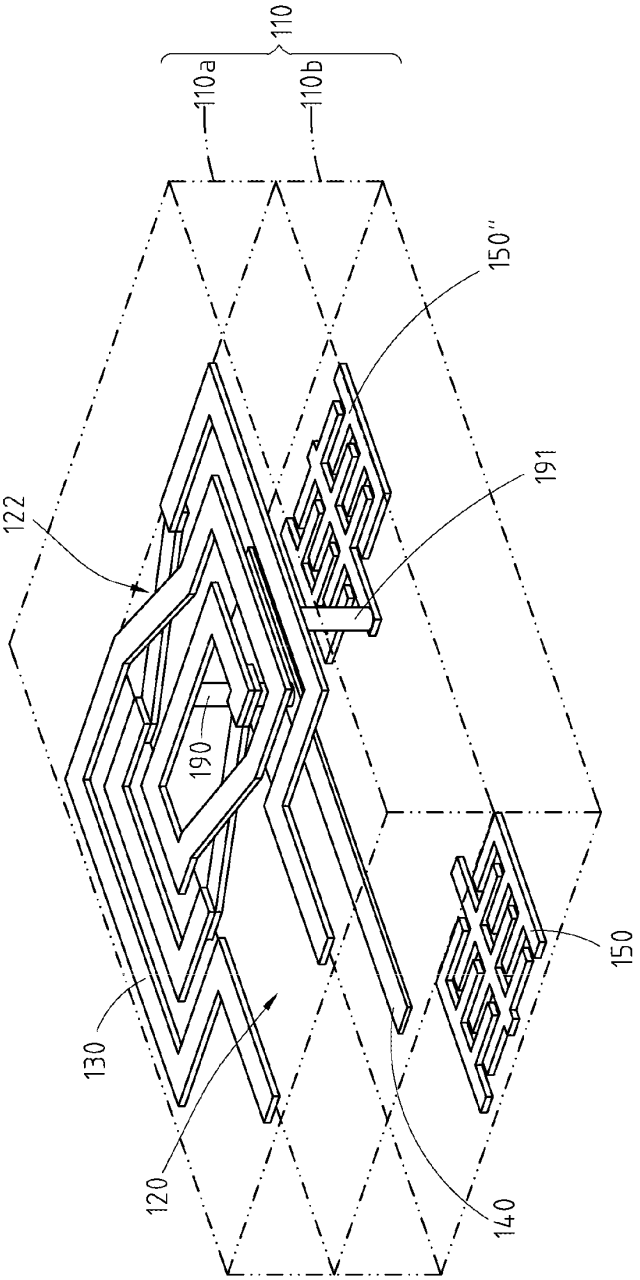


FIG. 14

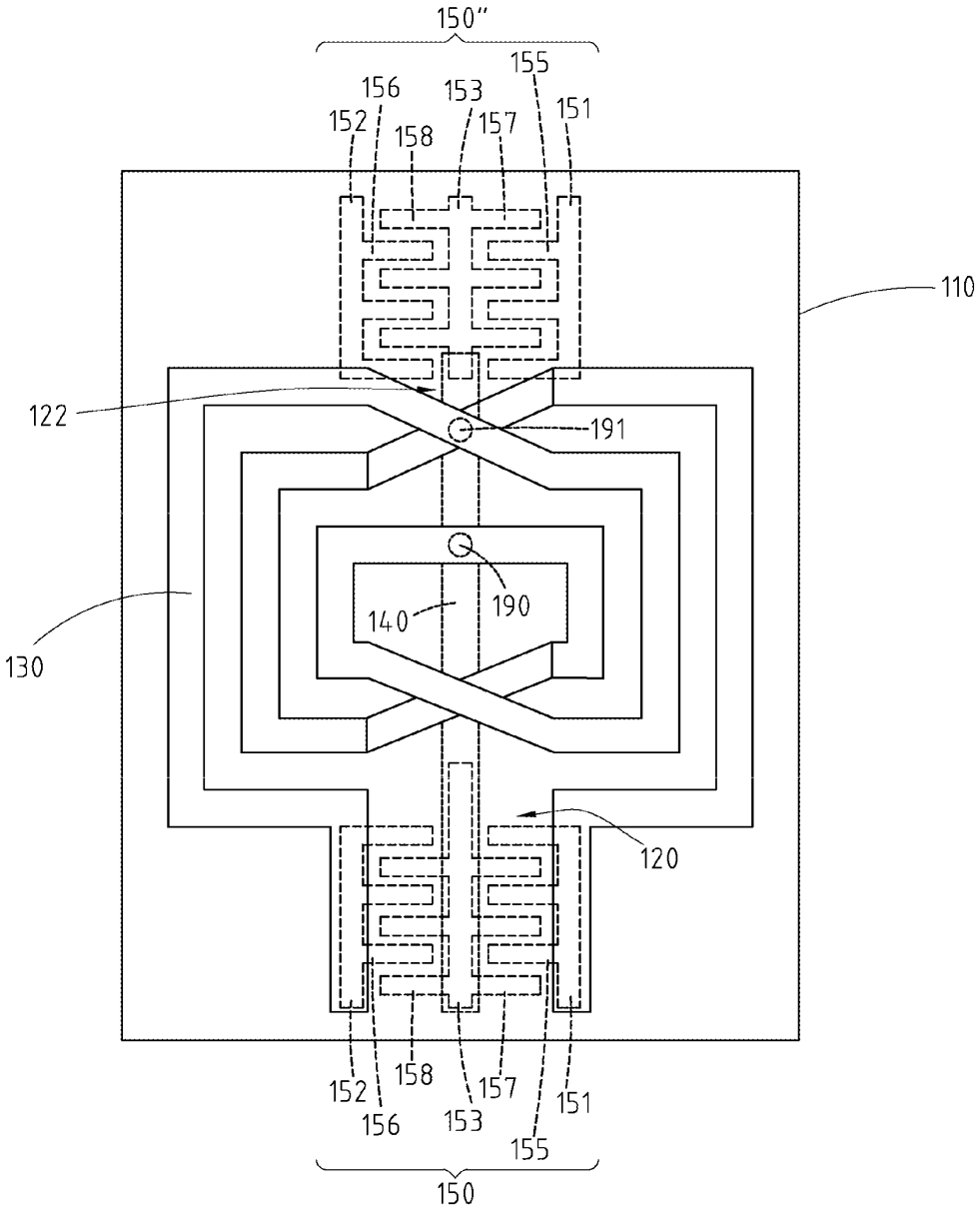

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FIG. 15

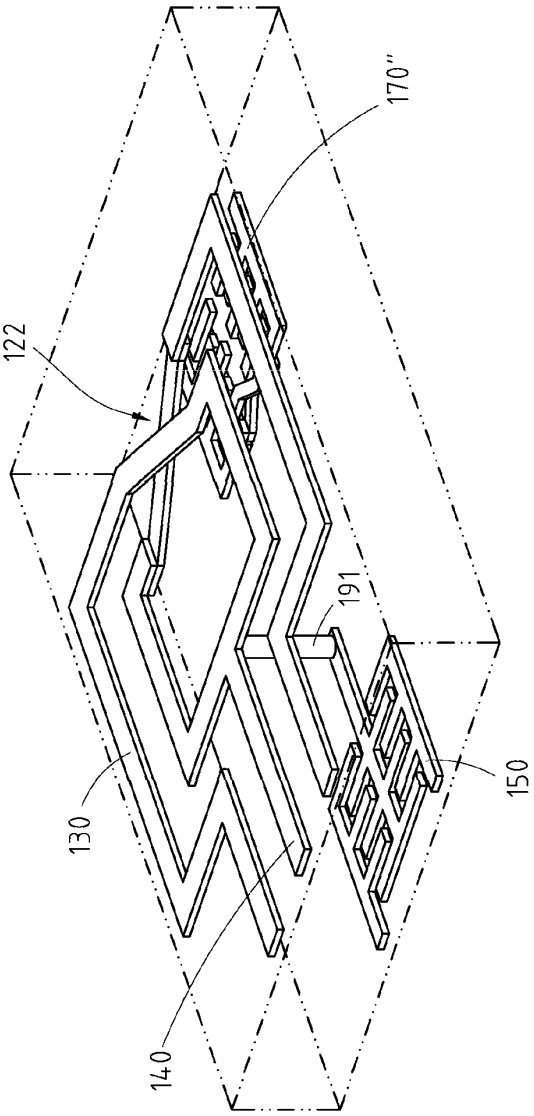


FIG. 16

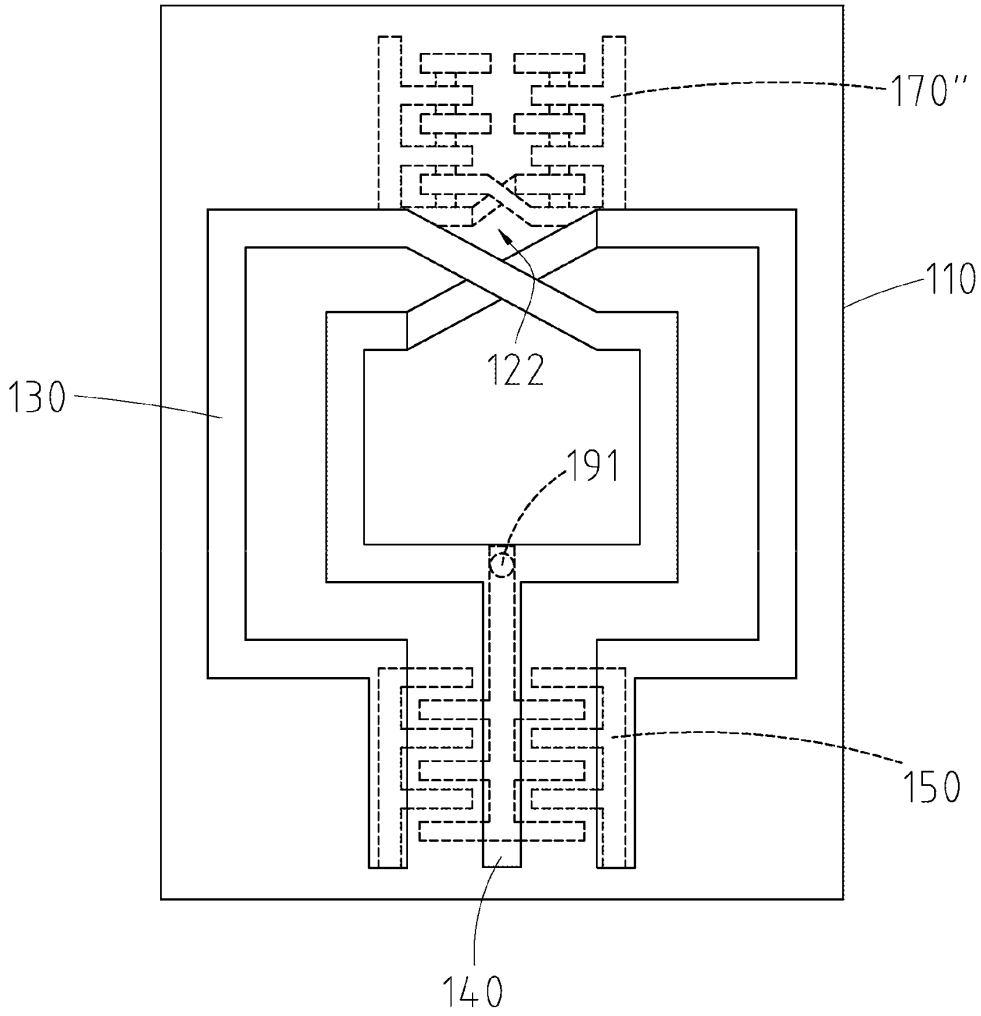


FIG. 17

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5750/0265PUS1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hsiao-Tsung		YEN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Hsinchu	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	No.2, Innovation Rd. II, Hsinchu Science Park,		
Address 2			
City	Hsinchu	State/Province	
Postal Code		Country i	TW

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yuh-Sheng		JEAN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Hsinchu	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	No.2, Innovation Rd. II, Hsinchu Science Park,		
Address 2			
City	Hsinchu	State/Province	
Postal Code		Country i	TW

Inventor 3 Remove

Legal Name

PTO/AIA/14 (03-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5750/0265PUS1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ta-Hsun		YEH	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Hsinchu	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	No.2, Innovation Rd. II, Hsinchu Science Park,		
Address 2			
City	Hsinchu	**State/Province**	
Postal Code		**Country** i	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	60601		
Email Address	mailroom@mg-ip.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT		
Attorney Docket Number	5750/0265PUS1	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	17	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5750/0265PUS1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	(•) Customer Number	( ) US Patent Practitioner	( ) Limited Recognition (37 CFR 11.9)
Customer Number	60601		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)
103113947	TW	2014-04-16	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5750/0265PUS1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5750/0265PUS1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	REALTEK SEMICONDUCTOR CORP.		
Mailing Address Information:			
Address 1	No.2, Innovation Rd. II, Hsinchu Science Park,		
Address 2			
City	Hsinchu	**State/Province**	
Country [i]	TW	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5750/0265PUS1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	

Mailing Address Information:			
Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Joe McKinney Muncy/			Date (YYYY-MM-DD)	2014-07-23
First Name	Joe Mckinney	Last Name	Muncy	Registration Number	32334

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): YEN, Hsiao-Tsung	Examiner:
Application No.: NEW	Art Unit:
Filed: 23 Jul 2014	Confirmation Number:
Title: SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT	
Attorney Docket No.: 5750/0265PUS1	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This Information Disclosure Statement is submitted:

☒ under 37 CFR 1.97(b), or
(within three months of filing national application or date of entry of international application; before mailing date of first office action on the merits; or before the mailing of a first Office action after the filing of a request for continued examination)

☐ under 37 CFR 1.97(c) together with either a:
- ☐ statement under 37 CFR 1.97(e), **or**
- ☐ a $180.00 (large entity) or $90 (small entity) fee under 37 CFR 1.17(p),

(after the CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
- ☐ statement under 37 CFR 1.97(e), **and**
- ☐ a $180.00 (large entity) or $90 (small entity) set forth in 37 CFR 1.17(p).

(filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Statement under 37 CFR 1.97(e) (if applicable):

☐ Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement (37 CFR 1.97(e)(1)).

☐ No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the information disclosure statement (37 CFR 1.97(e)(2)).

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the PTO/SB/08 attached hereto.

II. COPIES (check at least one box)

a. ☐ Submitted herewith is a legible copy of (i) each foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.

b. ☐ Submitted herewith is a legible copy of the International Search Report and each foreign patent or publication cited therein.

c. ☒ Some or all of the documents listed on the PTO/SB/08 are not enclosed because they are either U.S. Patents or Published Applications.

d. ☐ As provided in 37 CFR 1.98(d), some or all of the documents listed on the PTO/SB/08 are not enclosed because they were cited in the parent application(s). Accordingly, copies are not submitted herewith.

III. CONCISE EXPLANATION OF THE RELEVANCE
(check at least one box)

a. ☒ DOCUMENTS IN THE ENGLISH LANGUAGE
The attached patents, publications, or other information in the English language do not require a statement of relevancy.

b. ☐ DOCUMENTS NOT IN THE ENGLISH LANGUAGE
A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

c. ☐ ENGLISH LANGUAGE SEARCH REPORT
An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III)(A)(3).

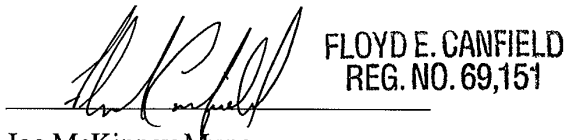
d. ☐ OTHER

The following additional information is provided for the Examiner's consideration.

It is requested that the information disclosed herein be made of record in this application. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account **50-3828** and please credit any excess fees to such deposit account.

Date: July 23, 2014

Respectfully submitted,



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PTO/SB/08a (07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	NEW
Filing Date	Jul 23, 2014
First Named Inventor	YEN, Hsiao-Tsung
Art Unit	
Examiner Name	
Attorney Docket Number	5750/0265PUS1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-8,362,591 B2	01-29-2013	Yen et al.	
		US-8,552,812 B2	10-08-2013	Yen et al.	
		US-2011/0128084 A1	06-02-2011	Jin et al.	
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional).[2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.[3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).[4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.[6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Filer:	Joe McKinney Muncy/Brandi Darden
Attorney Docket Number:	5750/0265PUS1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	19662047
Application Number:	14338904
International Application Number:	
Confirmation Number:	1455
Title of Invention:	SEMICONDUCTOR DEVICE WITH INDUCTOR-CAPACITOR RESONANT CIRCUIT
First Named Inventor/Applicant Name:	Hsiao-Tsung YEN
Customer Number:	60601
Filer:	Joe McKinney Muncy/Brandi Darden
Filer Authorized By:	Joe McKinney Muncy
Attorney Docket Number:	5750/0265PUS1
Receipt Date:	23-JUL-2014
Filing Date:	
Time Stamp:	15:49:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1600
RAM confirmation Number	2305
Deposit Account	503828
Authorized User	MUNCY, JOE MCKINNEY
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2014-07-23-ApplicationAsFiled.pdf	1428340 6d876c086bdeff3fdfad7acc2be0bd5f5fab2a43	yes	31

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal of New Application	1	2
Specification	3	23
Claims	24	26
Abstract	27	27
Oath or Declaration filed	28	30
Power of Attorney	31	31

Warnings:

Information:

2	Drawings-other than black and white line drawings	2014-07-23-Drawings.pdf	837134 b196cdac82ca0c935daa5b5a58e533fd1dd37a78	no	17

Warnings:

Information:

3	Application Data Sheet	2014-07-23-ApplicationDataSheet.pdf	1503279 51ee032587b245c85e36e7c40fb465b5f1b9aef4	no	7

Warnings:

Information:

4		2014-07-23-ids.pdf	201453 14c01c0af66148ec9f13e89989b42185523fde9a	yes	4

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	3
Information Disclosure Statement (IDS) Form (SB08)	4	4

Warnings:

Information:

5	Fee Worksheet (SB06)	fee-info.pdf	33162 7d921bbfc595998c42ba67b495d5b8ca3ad75996	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	4003368	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.