

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE
THE PATENT TRIAL AND APPEAL BOARD**

In re U.S. Patent No. 9,590,582

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Inventors: Hsiao-Tsung, Yen Yuh-Sheng, and Jean Ta-Hsun Yeh

Assignee: Realtek Semiconductor Corp.

Title: Semiconductor Device with Inductor-Capacitor Resonant Circuit

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I, Paul R. Prucnal, make this declaration in connection with the petition for *inter partes* review submitted by Petitioner for U.S. Patent No. 9,590,582. All statements made herein of my own knowledge are true, and all statements made herein based on information and belief are believed to be true. Although I am being compensated for my time in preparing this declaration, the opinions expressed herein are my own, and I have no stake in the outcome of this proceeding or any related litigation or administrative proceedings.

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I. INTRODUCTION

1. I am making this declaration at the request of Advanced Micro Devices, Inc. (“AMD”) in the matter of the Inter Partes Review of U.S. Patent No. 9,590,582 (“the ’582 Patent”) to Yen et al, assigned to Realtek Semiconductor Corp. (“Patent Owner”). I understand that AMD has been sued by Patent Owner in Certain Integrated Circuits, Components thereof, and Products Containing the Same; ITC Inv. No. 337-TA-1350 (DN 3659) where it is has accused AMD of infringing the ’582 Patent as well as U.S. Patent Nos. 7,936,245 (“the ’245 Patent”) and 8,006,218 (“the ’218 Patent”) (collectively, the “Asserted Patents”).

2. In preparing my declaration, I have reviewed the following documents.

Exhibit No.	Description
1001	U.S. Patent No. 9,950,582
1002	File History of U.S. Patent No. 9,590,582
1003	Declaration of Dr. Paul Prucnal
1004	Curriculum Vitae of Dr. Paul Prucnal
1005	J. Gonzalez et al., <i>A 56-GHz LC-Tank VCO With 17% Tuning Range in 65-nm Bulk CMOS for Wireless HDMI</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 58, Issue 5 (May 2010) (“Gonzalez”), available at https://ieeexplore.ieee.org/document/5438827
1006	Matthew Muh, Master of Science thesis entitled <i>Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO</i> , Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley (2005) (“Muh”), available at

Exhibit No.	Description
	https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=7337593a3bdb909b1f7d53da1c3202a61401fac7
1007	A. Niknejad et al., <i>mm-Wave Silicon Technology 60 GHz and Beyond</i> (Springer Science + Business Media 2008) (“Niknejad”) (excerpts)
1008	S. Biswal, <i>Basic Electronics Volume I</i> (Atlantic Publishers 2001) (excerpts)
1009	A. Niknejad & R. Meyer, <i>Design, Simulation and Applications of Inductors and Transformers for Si RF ICs</i> (Springer Science+Business Media 2000) (“Niknejad (2000)”) (excerpts)
1010	A. Niknejad, <i>Electromagnetics for High-Speed Analog and Digital Communication Circuits</i> (Cambridge Univ. Press 2007) (“Niknejad (2007)”) (excerpts)
1011	Joachim N. Burghartz, <i>Spiral Inductors on Silicon – Status and Trends (Invited Article)</i> , International Journal of RF and Microwave Computer-Aided Engineering, V. 8, No. 6, 422-432 (Nov. 1998) (“Burghartz”), available at https://onlinelibrary.wiley.com/doi/abs/10.1002/%28SICI%291099-047X%28199811%298%3A6%3C422%3A%3AAID-MMCE3%3E3.0.CO%3B2-K
1012	O.H. Murphy et al., <i>Design of Multiple-Metal Stacked Inductors Incorporating an Extended Physical Model</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 53, No. 6, 2063-2072 (June 2005) (“Murphy”), available at https://ieeexplore.ieee.org/document/1440724
1013	U.S. Patent No. 6,885,275 filed on Jan. 28, 2000, titled “Multi-track Integrated Spiral Inductor” to James Chang (“Chang”)
1014	U.S. Patent Application Pub. No. US 2008/0074229 published on Mar. 27, 2008 by Shahriar Moinian et al. (“Moinian”)
1015	Bryant Derand Williamson, Masters Thesis entitled <i>A 2.4 GHz LC-VCO Using On-Chip Inductors and Accumulation- Mode Varactors in a CMOS 0.18 μm Process</i> , University of Tennessee – Knoxville, Aug. 2005 (“Williamson”), available at https://trace.tennessee.edu/utk_gradthes/2537/
1016	Axel Dominique Berny, PhD Dissertation entitled <i>Analysis and Design of Wideband LC VCOs</i> , Electrical Engineering and Computer

Exhibit No.	Description
	Sciences, University Of California, Berkeley, Spring 2006 (“Berny”), available at https://www2.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-50.pdf
1017	A. Kral et al., <i>RF-CMOS Oscillators with Switched Tuning</i> , IEEE Custom Integrated Circuits Conference, May 14, 1998 (“Kral”), available at https://ieeexplore.ieee.org/document/695039
1018	Fei Yuan, <i>CMOS Active Inductors and Transformers Principle, Implementation, and Applications</i> , (Springer Science+Business Media, LLC 2008) ISBN 978-0-387-76477-1 (“Yuan”), available at https://link.springer.com/book/10.1007/978-0-387-76479-5
1019	Thomas H. Lee et al., <i>RF Passive IC Components</i> in book entitled <i>Circuits and Filters Handbook</i> , 2d Ed. (CRC Press LLC 2003) (“Lee”), available at http://www.kelm.ftn.uns.ac.rs/literatura/ekui/Circuits_and_Filters_Handbook_CH10.pdf
1020	Agilent Technologies, <i>Overview on interdigital capacitor design</i> , 2008 (“Agilent Technologies”), available at https://www.keysight.com/us/en/assets/7018-08093/technical-overviews-archived/5989-8912.pdf
1021	Sang Wook Park, PhD Dissertation entitled <i>Oscillator Architectures And Enhanced Frequency Synthesizer</i> , Texas A&M University (Dec. 2009) (“Park”), available at https://core.ac.uk/download/pdf/13643134.pdf
1022	Changhua Cao et al., <i>Millimeter-Wave Voltage-Controlled Oscillators in 0.13-um CMOS Technology</i> , IEEE Journal of Solid-State Circuits, Vol. 41, Issue 6 (June 2006) (“Cao”), available at https://ieeexplore.ieee.org/document/1637594
1023	Yue Wu et al., <i>A Temperature Stabilized CMOS VCO for Zero-IF Cellular CDMA Receivers</i> , Digest of Technical Papers, 2005 Symposium on VLSI Circuits, June 16-18, 2005 (“Wu”), available at https://ieeexplore.ieee.org/document/1469413
1024	Dorra Mellouli et al., <i>Design and Implementation of A 6-GHz Array of Four Differential VCOs Coupled Through a Resistive Network</i> , Analog Integrated Circuits and Signal Processing, Vol. 76, pp. 179-193 (2013) (“Mellouli”), available at https://link.springer.com/article/10.1007/s10470-013-0099-6#citeas

Exhibit No.	Description
1025	Xiao Shimao et al., <i>A novel 2.95–3.65 GHz CMOS LC-VCO using tuning curve compensation</i> , Journal of Semiconductors, Vol. 30, No. 10, 105001 (Oct. 2009) (“Xiao”), available at https://iopscience.iop.org/article/10.1088/1674-4926/30/10/105001/pdf
1026	Mohammad Nariman et al., <i>A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS</i> , 2010 IEEE Radio Frequency Integrated Circuits Symposium, May 23-25, 2010, pp. 157-160 (“Nariman”), available at https://ieeexplore.ieee.org/document/5477323
1027	Neric H. W. Fong, PhD Dissertation entitled <i>Low-Voltage Radio-Frequency CMOS Integrated Circuits in Silicon-On-Insulator</i> , Department of Electronics, Carleton University, Ottawa, Canada (May 23, 2002) (“Fong”), available at https://curve.carleton.ca/system/files/etd/63d93fb2-a8cc-4f63-865e-fba751da4fa1/etd_pdf/02a5d5d8788c5ea3b03555a6557ea59c/fong-lowvoltagefrequencycmosintegratedcircuits.pdf
1028	Babak Soltanian et al., <i>An Ultra Compact Differentially Tuned 6 GHz CMOS LC VCO with Dynamic Common-Mode Feedback</i> , IEEE 2006 Custom Integrated Circuits Conference, Sept. 10-13, 2006 (“Soltanian”), available at https://ieeexplore.ieee.org/document/4115046
1029	V. Macaitis et al., <i>Design of 4.48–5.89 GHz LC-VCO in 65 nm RF CMOS Technology</i> , Elektronika Ir Elektrotechnika, Vol. 20, NO. 2, pp. 44-47 (Feb. 5, 2014) (“Macaitis”), available at https://eejournal.ktu.lt/index.php/elt/article/view/6383
1030	Judith Maget, <i>Varactors and Inductors for Integrated RF Circuits in Standard MOS Technologies</i> , Institute of Electronics at the University of Bundeswehr (2002) (“Maget”), available at http://athene-forschung.unibw.de/doc/85282/85282.pdf
1031	Paolo Lucchi, PhD Dissertation entitled <i>Frequency generation for mm-Wave and satellite applications</i> , University of Bordeaux (Feb. 2012) (“Lucchi”), available at https://www.theses.fr/2012BOR14479.pdf
1032	U.S. Patent Publication No. 2009/0322447 (“Daley”)
1033	U.S. Patent No. 9,270,247 (“Jing”)
1034	Realtek Infringement Chart for U.S. Patent No. 9,950,582

Exhibit No.	Description
1035	Printout from www.m-w.com (Merriam-Webster Online Dictionary) (“substantial”)

3. In forming my opinions expressed below, I have considered the documents listed immediately above and my knowledge and experience based on my work and education in this area as described below.

4. The ‘582 Patent issued from U.S. Patent Application Serial No. 14/338,904, filed July 23, 2014. The earliest application it claims priority to is a Taiwanese patent application filed on April 16, 2014. It is my opinion that, as of April 16, 2014, a person of ordinary skill in the art (“POSITA”) pertinent to the subject matter of the ‘582 Patent would have had at least a bachelor’s degree in electrical engineering or an equivalent field, and at least 3-4 years of professional experience in the field of integrated circuit design. Further, it is my opinion that someone with additional education but less professional experience, and vice versa, may qualify as a POSITA. For instance, a POSITA would also include someone with a master’s degree in electrical engineering and 1-2 years of professional experience in the field of integrated circuit design or someone with a Ph.D. in electrical engineering. My analysis and opinions below are given from the perspective of a POSITA in this technological field in the relevant time frame, unless stated otherwise.

II. QUALIFICATIONS AND COMPENSATION

5. I am currently a professor of Electrical and Computer Engineering at Princeton University in the School of Engineering and Applied Science.

6. I received my undergraduate education at Bowdoin College, where I graduated summa cum laude in 1974 with an A.B. in Mathematics and Physics. I then graduated from Columbia University in 1976 with an M.S. in Electrical Engineering. I went on to receive an M.Phil. from Columbia in 1978 in Electrical Engineering and a Ph.D. from Columbia in 1979 in Electrical Engineering.

7. Upon receiving my Ph.D. in 1979, I joined Columbia University as an Assistant Professor of Electrical Engineering and in 1984 I was promoted to Associate Professor.

8. In 1988, I joined the faculty of Princeton University as an Associate Professor of Electrical Engineering. My responsibilities there included teaching and research. During that time, I was also the founding director of the New Jersey Advanced Technology Center for Photonics and Optoelectronic Materials. My responsibilities there included leading a \$10 million research program involving approximately thirty faculty members.

9. In 1990, I was promoted to the position of full Professor of Electrical Engineering at Princeton University. My teaching responsibilities have included courses in electronic circuits, signal processing, photonics, and communications.

My broad research interests at Princeton have included wireless communications, fiber-optic communications networks, computer interconnects, and network security. I also direct the Lightwave Communications Research Laboratory at Princeton University, through which much of my present research is conducted.

10. While at Princeton University, I received several awards and recognitions, including: (a) becoming a Fellow of the Institute for Electrical and Electronics Engineers (IEEE); (b) becoming a Fellow of the Optical Society of America (OSA); (c) receiving the Rudolf Kingslake Medal and Prize from the Society of Photo-Optical Instrumentation Engineers (SPIE) for the most noteworthy original paper in Optical Engineering; (d) receiving the Gold Medal Award from the Faculty of Mathematics, Physics, and Informatics at the Comenius University for leadership in the field of Optics; (e) receiving the Princeton University Graduate Mentoring Award; (f) receiving numerous Engineering Council Teaching Awards; (g) receiving the Walter Curtis Johnson Prize for Excellence in Teaching; (h) receiving the Princeton School of Engineering and Applied Science Distinguished Teacher Award; (i) receiving the 2015 President's Award for Distinguished Teaching at Princeton; (j) being elected to the National Academy of Inventors (2018). My election to the National Academy of Inventors cited my work on advanced wireless interference-cancellation technology.

11. I am the author of two books, “Optical Code Division Multiple Access: Fundamentals and Applications” (2005), and “Neuromorphic Photonics” (2018), and co-author or contributor to approximately 33 additional book chapters, as well as over 300 peer-reviewed publications in peer-reviewed journals, and 365 conference proceedings.

12. In addition to the activities, education, and professional experience listed above, I have been involved in numerous research projects that contribute to my expertise relating to this report. My responsibilities in these projects have included, among other things, interference cancellation techniques for radio-frequency communications, simultaneous transmit-and-receive techniques for cellular radios, anti-jamming systems for radio communications and spread spectrum communications. Specifics on a few of these research projects are provided below.

13. In 1982, I worked for Optical Information Systems, Inc. on a project that involved transceiver design for fiber optic communications. My responsibilities included the design of transmitters and receivers for high-speed communication.

14. From 1983-1984, I worked for GTE Labs on a project that involved performance analysis of fiber optic communication systems. My responsibilities

included the investigation of high-performance modulation formats for communications.

15. From 1985-1986, I worked for AT&T Bell Laboratories on a project that involved research on multiple access techniques. My responsibilities included investigating time-division multiplexing for fiber optic networks.

16. In 1987-1988, I worked for IBM on a project that involved research on multiple access techniques for local area networks.

17. From 1987-1989, I worked for Dove Electronics on a project that involved research on communication switching technology and architectures. My responsibilities included the design and analysis of packet switching architectures.

18. From 1992-1995, I worked for Siemens Corporate Research on a project that involved research on switching technology. My responsibilities included the investigation of technologies for high-speed multiplexing and switching networks.

19. From 1996 - present I have worked for the Institute for Defense Analyses on projects related to national security involving communications and computing.

20. From 1998-2000, I worked on a project for Ultrafast Optical Systems performing testing and measurement on optoelectronic transceivers.

21. From 1999-2000, I worked for SAIC on a project that involved research on communication network architectures. My responsibilities included the investigation of novel switching and multiplexing techniques for high-speed communication networks.

22. From 1999-2002, I worked for Multi Link Technologies, Inc. on a project that involved communication transceiver design.

23. From 2000-2002, I worked for Ultra-Fast Optical Systems on a project that involved research and development on regenerators for communication systems.

24. From 2000 - present, I have been a member of the advisory board on network technology for Alphion, Inc.

25. From 2003-2006, I worked for Kailight Inc. on a project that involved research and development on switching technology. My responsibilities included the design and testing of digital repeater for communication networks.

26. From 2006-2008, I led a DARPA funded project developing an add drop multiplexer for self-healing ring networks.

27. From 2004-2011, I worked for NEC Laboratories on a project that involved research on physical layer security in communication networks. My responsibilities included the design and analysis of techniques for steganography and data encryption.

28. I am also a named inventor on at least 27 issued U.S. patents, and at least 5 additional U.S. patent applications.

29. I have extensive experience in the electrical engineering field throughout my career. In particular, during the past 10 years I have taught several undergraduate and graduate courses at Princeton on communications, such as “Photonics and Lightwave Communications,” which covers optical and radio-frequency analog and digital communications systems; “Electronic Circuit Design,” which covers circuits, including their design and implementation; and “An Introduction to Engineering,” which covers general electrical engineering principles. I am also involved with independent research projects involving senior thesis work in a variety of electrical engineering disciplines.

30. My research has been supported by research contracts and grants from the National Science Foundation (NSF), the U.S. Army Communication Electronics Command, the Defense Advanced Research Projects Agency (DARPA), the U.S. Navy, the National Security Agency, and L3 Telemetry East.

31. I have extensive experience consulting for the communications industry, including AT&T Bell Laboratories, NEC Labs, the Institute for Defense Analyses, and Alphion, Inc.

32. I have been a technical advisor to several startup companies in the telecommunications industry. Based on my patents, Kalight Photonics developed

communication repeaters, before being acquired by a publicly traded company. Another company, in conjunction with L3 Telemetry East, developed an anti-jamming system for the Army that helps defend against IEDs. This work is also based on my patents.

33. Unless otherwise noted, the statements made herein are based on my personal knowledge, experience, and education. If called to testify about this Declaration, I could and would do so competently and truthfully. I reserve the right to amend and/or supplement my opinions to the extent that new information becomes available.

34. I believe I am qualified to serve as a technical expert in this proceeding based upon my educational and work experience. A copy of my current curriculum vitae is provided as Exhibit 1004. A list of cases in which I have testified as an expert in deposition or trial in the past four years is also included with Exhibit 1004.

35. I am being compensated at the rate of \$750 per hour for the time I spend on this matter. I do not have any financial or other interest in this proceeding itself, or in any other proceeding involving the '582 Patent or any related patents. My compensation is not dependent on the substance of my statements in this Declaration. I am over the age of 18 and am competent to write this Declaration.

III. RELEVANT LEGAL STANDARDS

A. Obviousness

36. I understand that obviousness is analyzed from the perspective of a POSITA at the time of the alleged invention. I also understand that a POSITA is presumed to have been aware of all pertinent prior art at the time of the alleged invention.

37. I understand that an obviousness analysis involves comparing a claim to the prior art to determine whether the claimed invention as a whole would have been obvious to a POSITA in view of the prior art and in light of the general knowledge of the art at the time the invention was made. I also understand that the invention may be deemed obvious when a POSITA would have reached the claimed invention through routine experimentation.

38. I understand that obviousness can be established by combining or modifying the disclosures of the prior art to achieve the claimed invention. It is also my understanding that where there is a reason to modify or combine the prior art to achieve the claimed invention, there must also be a reasonable expectation of success in so doing to render the claimed invention obvious. I understand that the reason to combine prior art references can come from a variety of sources, not just the prior art itself or the specific problem the patentee was trying to solve. I also understand that the references themselves need not provide a specific hint or

suggestion of the alteration needed to arrive at the claimed invention; the analysis may include recourse to logic, judgment, and common sense available to a POSITA.

39. I understand that when there is some recognized reason to solve a problem, and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp. If such an approach leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In such a circumstance, when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious.

40. I understand that when considering the obviousness of an invention, one should also consider whether there are any objective indicia that support the non-obviousness of the invention. I further understand that objective indicia of non-obviousness, also known as “secondary considerations,” include failure of others, copying, unexpected results, information that “teaches away” from the claimed subject matter, perception in the industry, commercial success, and long felt but unmet need. I also understand that for objective indicia of non-obviousness to be applicable, the indicia must have some sort of nexus to the subject matter in the claim that was not known in the art. I understand that this nexus includes a

factual connection between the patentable subject matter of the claim and the objective indicia alleged. I also understand that an independently made invention that is made within a comparatively short period is evidence that the claimed invention was the product of ordinary skill.

41. Finally, I understand that patent examiners at the U.S. Patent and Trademark Office (“PTO”) rely upon certain exemplary rationales in reviewing patent applications to understand whether the subject matter of the claims is obvious. I understand that the following is the list of exemplary rationales relied upon by patent examiners at the PTO: (i) combining prior art elements according to known methods to yield predictable results; (ii) simple substitution of one known element for another to obtain predictable results; (iii) use of a known technique to improve similar devices (methods, or products) in the same way; (iv) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (v) “obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (vi) known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art.

B. Construing the Meaning of Claim Terms

42. I understand that an IPR is a proceeding before the PTO for evaluating the validity of issued patent claims. I understand that, in an IPR, a claim term is interpreted in a manner consistent with the standard used in patent litigation, as set forth in a case known as *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). That standard generally construes the claims according to their “ordinary and customary” meaning in view of the claim language, specification, file history, and where applicable, relevant other evidence.

43. I understand that a patent’s “specification” includes all the figures, written descriptions, and claims within the patent. I understand that the PTO will look to the specification and prosecution history to see if there is a definition for a given claim term, and, if not, will apply the ordinary and customary meaning from the perspective of a POSITA at the time in which the alleged invention was made.

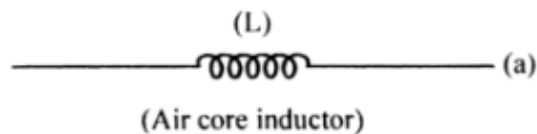
44. As discussed above and detailed in my curriculum vitae, I have extensive experience in the electrical engineering field throughout my career, including related to semiconductors, inductors, and transformers. I believe that I would qualify as understanding the knowledge and skill of a POSITA as of April 16, 2014, and I have a sufficient level of knowledge, experience, and expertise to provide an expert opinion in the field of the ‘582 Patent.

IV. BACKGROUND OF THE TECHNOLOGY

A. Inductor

1. Inductor Basics

45. An inductor is a common electrical component that stores energy in the form of a magnetic field. Biswal (EX-1008) at 13. Inductors are sometimes referred to as “coils” and the symbol for an inductor in an electrical circuit is the letter “L” or a drawn wound coil, as shown below. *Id.* at 14.



Id.

46. A straight wire, when bent into a coil to form an inductor, possesses inductance which is known as the self-inductance of the coil. *Id.* This inductance plays the role of friction in mechanics, and it is sometimes called a “choking coil” because it chokes alternating current (AC). *Id.* at 29. AC current is a current which, when flowing through a conductor, changes continuously in magnitude and varies periodically in direction, as shown below. *Id.* at 26. In the graph below, “I” represents the magnitude of the AC current, and “t” represents time.

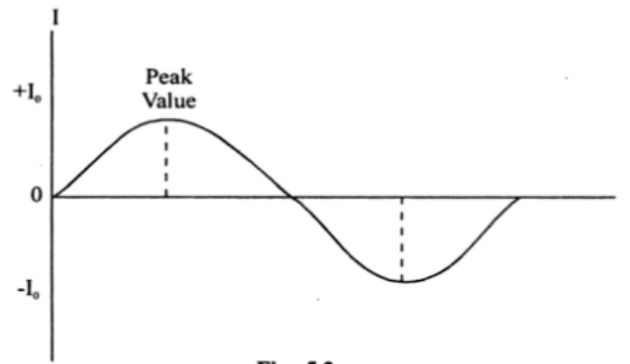


Fig. 5.2

Id.

47. A fundamental principle of inductors is that while it resists the flow of AC current, a pure inductance offers no resistance to the flow of direct current (DC) current through it. *Id.* at 14. Direct current is a current which, when flowing through a conductor, can change in magnitude but not in direction. *Id.* at 26. The role of inductance in an AC circuit is similar to the role of a resistor in a DC circuit, which opposes the flow of current in a conductor. *Id.* at 29.

48. Off-chip inductors are usually realized as a coil with a helical shape, as depicted below. Niknejad (2000) (EX-1009) at 32-33. As current flows through the coil, a magnetic field is produced illustrated by the imaginary field lines that flow through the inner core of the winding and wrap around the outside. *Id.* at 33. Each additional turn of the inductor adds to the magnetic field in phase with the previous turn. *Id.* The inductance is largely a function of the area of the loop and the number of turns in the winding. *Id.*

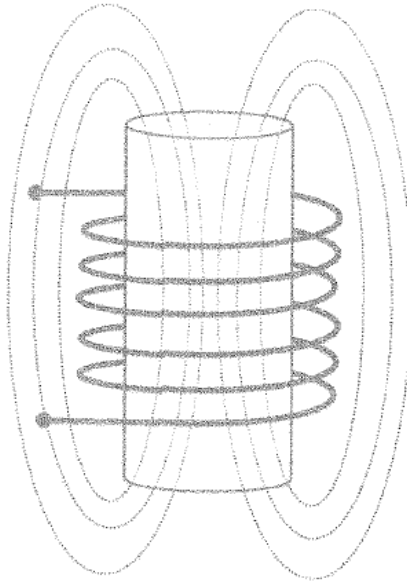


Figure 2.6. The typical coil inductor.

Id.

2. How Inductance is Measured

49. An inductor coil, which is the segment of an inductor that produces an induction effect as a result of current flowing through it, has a co-efficient of self-induction called the inductance “ L ”. Biswal (EX-1008) at 15. Self-inductance L of an inductor is generally defined as the “magnetic flux linked with it when a unit current flows through it,” which is mathematically shown in the equation below.

Id.

$$L = \frac{\phi}{i}$$

Id.

50. In this equation, Φ represents the magnetic flux linked with the coil when the current is unity and “ i ” stands for current. *Id.* Two units used to represent inductance include the Henry and the Electromagnetic Unit (EMU). *Id.* These units, and their relationship to one another, are shown below.

$$1 \text{ Henry} = \frac{1 \text{ volt}}{1 \text{ amp./sec.}}$$

$$1 \text{ Emu of inductance} = \frac{1 \text{ emu of potential difference}}{1 \text{ emu of current / sec.}}$$

Relation between Henry and emu of inductance

$$1 \text{ Henry} = 10^9 \text{ emu of inductance.}$$

Id.

51. Further, another important property of an inductive coil is its Inductive Reactance (X_L). *Id.* at 16. As I previously stated, an inductor does not oppose the flow of DC current because it has negligible DC resistance. *Id.* But when AC current passes through an inductor, induced electromotive force (emf) is created, which opposes the AC current. *Id.* This opposition to AC current, which can be thought of loosely as an AC resistance of an inductor, is measured by inductive reactance (X_L). *Id.* Its equation is below.

$$X_L = \omega L = 2 \pi f L$$

Id.

52. In this equation, “ L ” is the self-inductance of the coil measured in Henry and “ f ” is the frequency of applied AC measured in Hertz. *Id.*

3. The Q-Factor of an Inductor

53. At its core, the “Q-factor” or “Quality Factor” of a coil is the ratio of energy storage to energy loss in a practical inductor over a cycle of excitation, as shown below. Niknejad (2007) (EX-1010) at 142.

$$Q \equiv \frac{\text{energy stored}}{\text{energy loss}}$$

54. From this fundamental equation, we can derive that the Q factor is also equal to the ratio of the reactance (X_L) of a coil at resonance to the resistance (R) of the coil. *Id.* This equation is shown below.

$$Q = \frac{\omega L}{R}$$

Id.

55. L is the inductance, R is the DC resistance, and the product ωL is the inductive reactance. The Q of an inductor at a given frequency is a measure of its efficiency. *Id.* at 142-143. The higher the Q factor of the inductor, the lower the energy loss of the device and the closer it approaches the behavior of an ideal inductor. *Id.*; Niknejad (2000) (EX-1009) at 25. High Q inductors are used with capacitors to make resonant circuits in radio transmitters and receivers, which are discussed in more detail below.

56. To improve an inductor and its Q factor, we must minimize the various loss mechanisms associated with the inductor. Niknejad (2007) (EX-1010) at 143. These loss mechanisms include conductive losses, internally induced losses such as skin effect, externally induced losses such eddy current generated by nearby conductors, magnetization losses, displacement current losses, and radiative losses. *Id.* at 143-145.

57. Sometimes, to improve the Q factor of an inductor, a patterned ground shield is placed under and around the inductor (and above a substrate). A patterned ground shield can include various shaped patterns, such as those shown below, that provide electric shielding between the inductor and the substrate. The patterning prohibits a circular flow of eddy currents generated by the inductor. Maget (EX-1030) at 21; Lee (EX-1019) at 10-12; Niknejad (EX-1007) at 26.

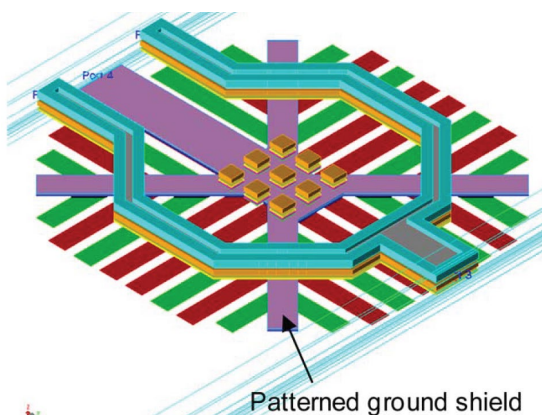
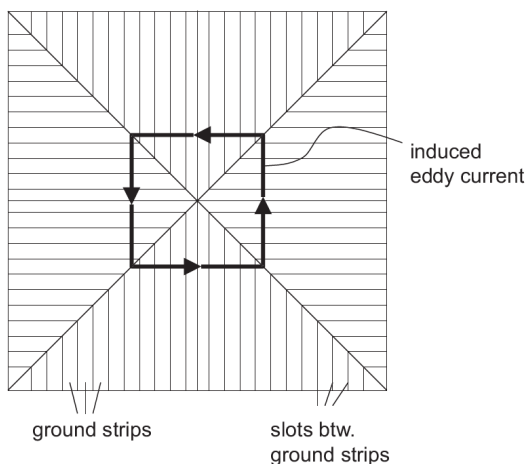


Figure 2.15: Principle of patterned ground shields.  Maget at Fig. 2.15 (left); Gonzalez (EX-1005) at Fig. 8 top half (right).

4. Inductors in Integrated Circuits

58. Inductors have many applications including frequency filters, chokes, sensors, relays, switching power supplies, induction motors, transformers, among many other things. As is generally known, “[p]assive devices such as inductors and transformers, play an integral part in the performance of circuit building blocks....”

Niknejad (2000) (EX-1009) at 16.

59. Until the early 2000s, passive devices such as inductors played a relatively minor role in silicon integrated circuits in comparison with active devices. Niknejad (2000) (EX-1009) at 15. The main reason for this was the size difference. *Id.* Active devices were continually shrinking and occupying less and less chip area whereas passive devices remained large. *Id.* While it was possible to fabricate a small value of capacitance on-chip, inductors were more difficult to integrate due to the large physical area required to obtain sufficient inductance at a given frequency. *Id.* This was compounded by the losses in the substrate which made it very difficult to fabricate high quality devices. *Id.*

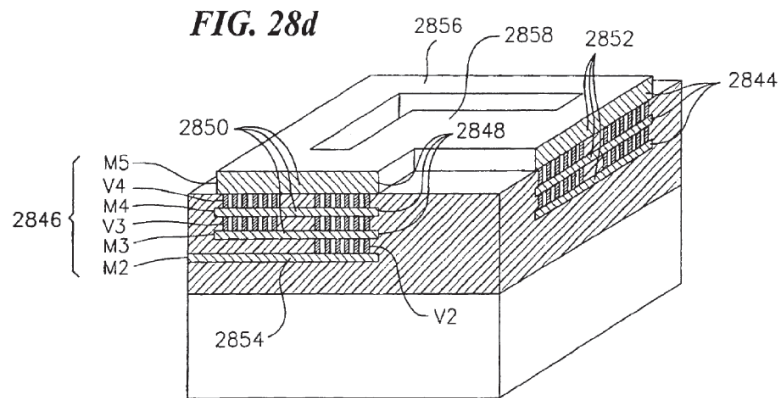
60. When passive devices like inductors were needed, they usually were connected externally on the circuit board rather than on-chip. *Id.* This led to the push for and development of integrating passive devices on semiconductor devices. *Id.* at 7.

61. When formed in integrated circuits, it was well known prior to the priority date of the '582 patent that the coils of an inductor could be formed on a single metal layer (planar) or multiple metal layers. Burghartz (EX-1011) at 2-12, *e.g.*, 6 (“In addition to the planar coil structure ... multilevel interconnects offer the possibility to fabricate inductor structures with several stacked spiral coils.”); Murphy (EX-1012) at 5-13.

5. Use of Vias to Connect Metal Layers

62. At its core, a via is an electrical connection between metal layers. *See* Chang (EX-1013) at 39:12-14, Fig. 28d. Vias can be formed by punching holes through two or more adjacent layers, which are then filled with a metallic paste making the interconnection from layer to layer. *See, e.g.*, Moinian (EX-1014), ¶ 0023.

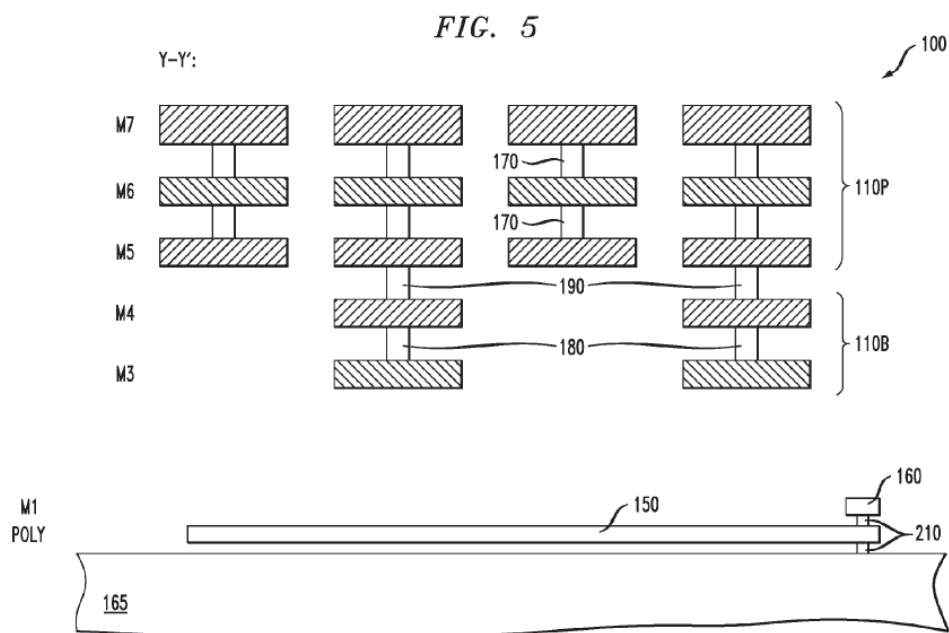
63. As Chang explains, vias can be used in a multi-layer inductor to couple a bottom track to one or more tracks disposed in layers above it. Chang (EX-1013) at 39:12-14. In this case, vias can be used to couple tracks together at the beginning of an inductor winding, at the end of the inductor winding, and along the length of the track. *Id.* at 39:9-15. The vias can be used “in as many places as possible along the length of each track to couple the layers.” *Id.* at 39:29-32. This is illustrated below.



Chang (EX-1013) at Fig. 28d.

64. As shown above, multiple vias (labeled V2, V3, and V4) are used to connect the different metal layers M2, M3, M4, and M5.

65. Another example is illustrated in U.S. Patent Application Pub. No. US 2008/0074229 published on Mar. 27, 2008 by Shahriar Moinian et al. (“Moinian”) (EX-1014). Moinian explains that metal segments can be “electrically connected together by a multiplicity of contact vias 170 so that they are connected in parallel with each other (i.e., they are shunted)” Moinian (EX-1014), ¶ 0023. It also explains that vias can be used for the cross-over bridges as well. *Id.* Using vias to connect segments on various metal layers was very well-known and is illustrated in Moinian below.



Id. at Fig. 5.

B. Capacitor

1. Capacitor Basics

66. A capacitor is a device that stores electrical energy in an electric field by virtue of accumulating electric charges on two close surfaces insulated from each other. Biswal (EX-1008) at 3. The function of the capacitor is to store a large amount of charge for a given voltage difference or to store a given charge at low voltage difference. *Id.*

67. The capacitance of a capacitor is defined as the ratio of charge transferred from one plate to the other plate of the capacitor, to the voltage difference produced between the plates. Mathematically, we can write:

$$C = Q/V,$$

where C is the capacitance of the capacitor, Q is the amount of charge transferred from one plate to the other, and V is the voltage or potential difference between the two plates. *Id.*

68. A simple capacitor can be formed by taking two separate metallic plates with non-conducting substance (dielectric) placed in the space between them, as illustrated in the figure below:

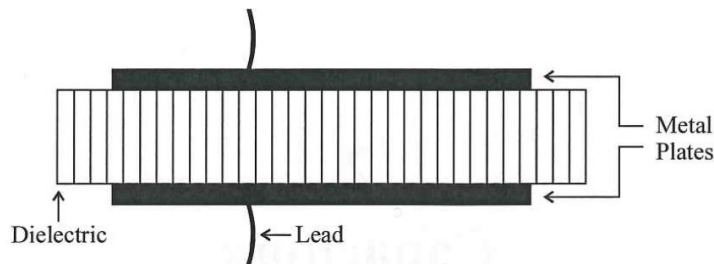


Fig. 2.1

Biswal (EX-1008) at 4.

69. Due to the two-plate nature, a capacitor is typically represented by the following symbols:

Symbols of capacitor

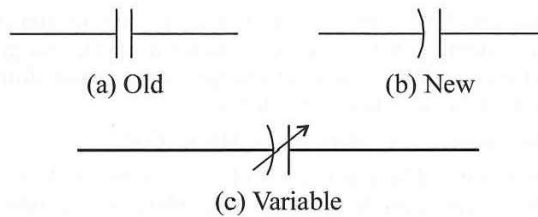


Fig. 2.2

Id. at 4.

70. Solid and liquid materials such as mica, paraffined paper or oil are used as the material medium between the plates. These materials have good insulating properties as well as they also respond to the presence of the electric field between the plates of the capacitor. As a result, the capacitance increases largely. These non-conducting substances introduced in between the two plates of a capacitor are called dielectrics. The presence of a dielectric between the two plates of a capacitor increases the capacitance of the capacitor. *Id.*

71. Based on the capacitance formula above, the capacitance of a parallel plate capacitor can be further determined as follows:

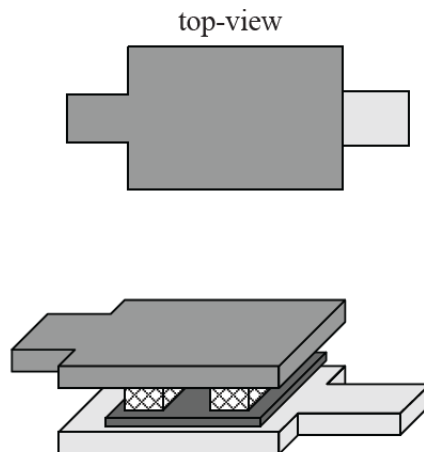
$$C = \epsilon_r \epsilon_o A / S$$

where ϵ_r is the relative permittivity or dielectric constant of the dielectric employed between the two plates, ϵ_o is the permittivity of empty space, A is the surface area of each plate, and S is the distance separating the two plates. *Id.* at 5.

72. It is clear from the above equation that the capacitance of a parallel plate capacitor is directly proportional to the area of each plate, A; inversely proportional to the distance between the two plates, S; directly proportional to the dielectric constant, ϵ_r . This shows that as the area of each plate increases, the capacitance will increase. Increasing a distance between the two plates decreases the capacitance. As the dielectric constant rises, the capacitance also increases. *Id.*

2. Capacitor Types

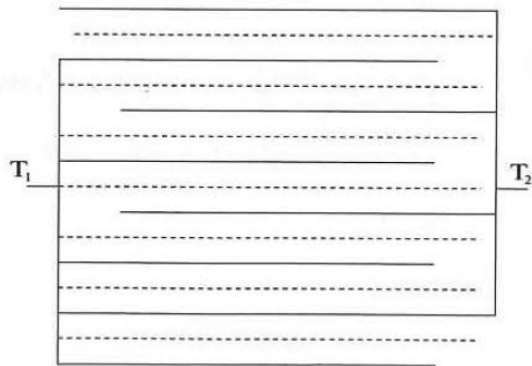
73. It has been known for decades that capacitors come in various forms. One simple type is simple parallel plate capacitors, sometimes also called metal-insulator-metal (MIM) capacitors, as I explained above. Biswal (EX-1008) at 4; Niknejad (EX-1007) at 26. Due to their relatively simple and compact geometry, MIM capacitors were commonly used on integrated circuit chips. Berny (EX-1016) at 90. The capacitance is determined from the parallel plates' area and separation and the type of dielectric. A 3D illustration of an integrated MIM capacitor is below.



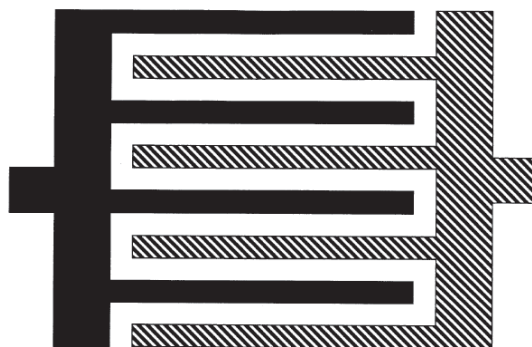
Berny (EX-1016) at 91, Fig. 3.10(a).

74. Another type is finger capacitors, sometimes also called metal-oxide-metal (MOM) capacitors. Biswal (EX-1008) at 4; Niknejad (EX-1007) at 27. Finger capacitors are composed of a large number of parallel fingers connected to either port of the device. Niknejad (EX-1007) at 27. “Finger” (comb) capacitors can be easily fabricated in any modern CMOS process due to the abundance and

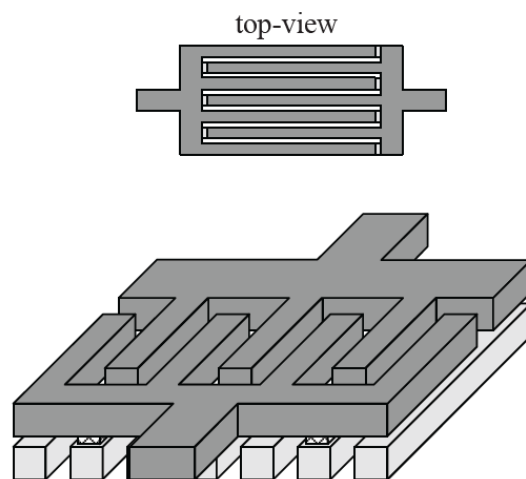
high packing density of the metal layers. Niknejad (EX-1007) at 27. A finger capacitor is equivalent to a large number of parallel plate capacitors, so it is sometimes also called a multi-plate capacitor. Due to the closely packed and interdigitated electrode plates, this capacitor can realize large capacitance with minimal area. Biswal (EX-1008) at 4. Exemplary illustration of finger capacitors are shown below.



Biswal (EX-1008) at 5, Fig. 2.4 (left); Niknejad (EX-1007) at 27, Fig. 3.11 (right).



Lee (EX-1019) at 9, Fig. 11.10 (left);



Berny at 91, Fig. 3.10(b) (right).

75. Yet another type is metal-oxide-semiconductor (MOS) capacitors, which were commonly used as variable capacitors (varactors). Niknejad (2000) (EX-1009) at 44-45; Williamson (EX-1015) at 39; Niknejad (2007) (EX-1010) at 58. MOS varactors are voltage-controlled capacitors established by the MOS structure and used in LC voltage controlled oscillators. Williamson (EX-1015) at 39; Niknejad (2007) (EX-1010) at 58. For example, a MOS transistor with the drain, source, and body tied together would accomplish a MOS capacitor with a variable capacitance between the gate and source. Williamson (EX-1015) at 39; Niknejad (2007) (EX-1010) at 58. An exemplary structure of a MOS capacitor is illustrated below.

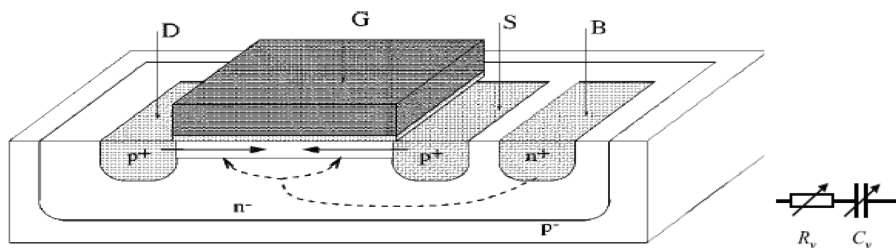
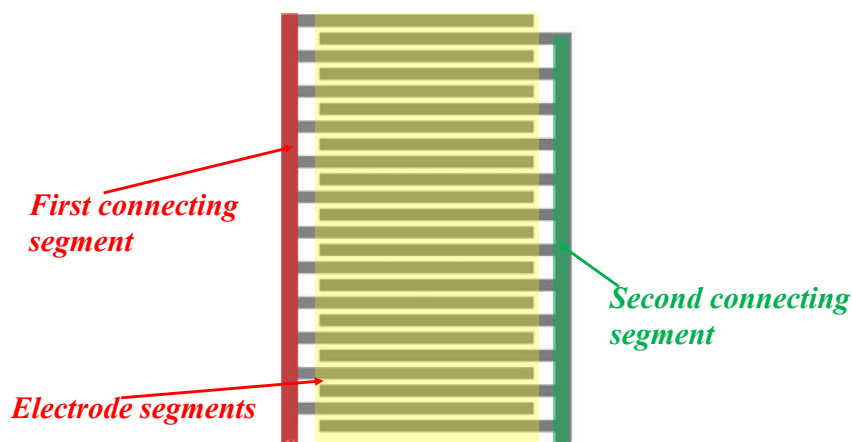


Figure 3.9 MOS Varactor Equivalent Circuit [3]

Id. at 44.

76. Notably, the '582 Patent discloses “capacitors in various forms, such as a metal-oxide-metal (MOM) capacitor, a metal-insulator-metal (MIM) capacitor, or a metal-oxide-semiconductor (MOS) capacitor,” and acknowledges that “the structures of the capacitors in various forms are well known in the field.” '582 Patent (EX-1001) at 12:11-16. For instance, the '582 Patent's Fig. 12 shows a capacitor component 150' which is a “MOS capacitor.” *Id.* at 12:16-17.

77. A capacitor typically has connecting segments and electrode segments, as illustrated below. The electrode segments serve as electrode plates of the capacitor. The connecting segments are used for connecting the capacitor to other circuit components (e.g., receiving or transmitting a signal from other circuit components). Further, various types of capacitors have comb or finger-shaped electrode segments that are each connected to an end of a connecting segment. Such electrode segments commonly extend in a direction perpendicular to a direction of a connecting segment. *See, e.g.,* Niknejad (EX-1007) at Fig. 3.11; Gonzalez (EX-1005) at Fig. 8.



Niknejad (EX-1007) at 27, Fig. 3.11 (annotations added in color).

3. Variable Capacitor

78. Variable capacitor, varactor for short, is a class of a capacitor whose capacitance can be adjusted or varied. Capacitance can be adjusted using different mechanisms.

79. One mechanism is spatial changes. For instance, one capacitor is formed of two sets of plates, one stator or stationary plates and the other rotor or rotatable plates. In this capacitor, when the shafts are rotated the rotor plates mesh into the spaces between stator plates, without touching. Consequently, the area of the plates vary and hence the capacitance changes. Biswal (EX-1008) at 6.

80. Another mechanism is voltage changes. For instance, in a MOS varactor, a voltage difference between a gate electrode and a source electrode can change the channel characteristics and thereby lead to a change in capacitance. Niknejad (2007) (EX-1010) at 59. In oscillator circuits, capacitors are typically variable or tunable, e.g., such that the oscillator can resonate at a desired frequency. MOS varactors are particularly helpful in semiconductor devices, and have been routinely used in VCO designs for decades. *See, e.g.*, Kral (EX-1017) at 1 (1998 article discussing MOS capacitor tuning in a VCO).

C. LC Resonant Circuit

81. It has been known for over a century that an inductor and a capacitor can form a resonant circuit. “LC resonators, also referred as LC tanks,¹ are made up of an inductor and a capacitor connected in series or in parallel. One or more

¹ The name “tank” came from an older name “tank circuit,” because the operation of an LC circuit is analogous to a tank in a fluid system, in which the dimensions of the tank define the natural frequency observed when fluid is pulsed through the tank.

resistive components modeling the resonator losses are generally included.” Berny (EX-1016) at 79. Thus, “in the simplest case, LC tanks are represented as series or parallel RLC networks,” as illustrated below. *Id.*

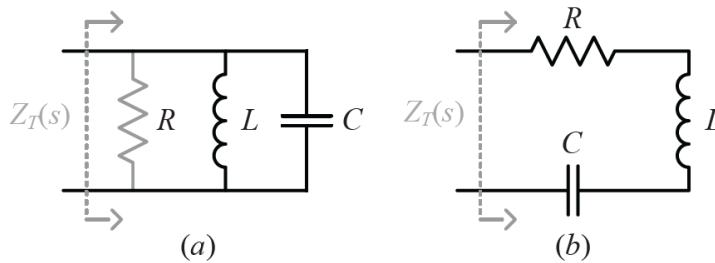


Figure 3.2: (a) Parallel LC tank. (b) Series LC tank.

Id.

82. An LC resonant circuit operates under simple principles. If an inductor is connected across a charged capacitor, the voltage across the capacitor will drive a current through the inductor. Electric charges flow back and forth between the plates of the capacitor, through the inductor. The energy oscillates back and forth between the capacitor and the inductor until internal resistance makes oscillations die out. The tuned circuit’s action, known as a harmonic oscillator, is like a pendulum swinging back and forth, or water sloshing back and forth in a tank. In many applications the tuned circuit is part of a larger circuit which applies AC to it, driving continuous oscillations. If the frequency of the applied current is the LC circuit’s natural resonant frequency, resonance will occur, when a small driving current can excite large amplitude oscillating voltages and

currents. In typical circuits, the oscillations are very fast, from thousands to billions or more of times per second. *See generally id.* at 79-82.

83. The natural frequency, called a resonant frequency (ω_o), is determined by the capacitance value (C) and inductance value (L). A mathematical equation for calculating the resonant frequency is illustrated below:

$$\omega_o = 1/\sqrt{LC}$$

Id. at 80.

84. The LC resonator's quality factor, Q, embodies various losses inherent to its elements and thus indicates its ability to retain energy. *Id.* The Q of an LC resonator can be calculated using the equation below, where ω represents frequency. Obviously, more stored energy and less dissipated power would lead to a higher Q. Quality factor is an important quantity because it often determines the phase noise performance of LC-based VCOs. *Id.*

$$Q \equiv \omega \cdot \frac{\text{Energy stored}}{\text{Average power dissipated}}$$

Id.

D. LC-Based Voltage-Controlled Oscillator (VCO)

85. LC resonant circuits as a basic and fundamental circuit unit have been part of various circuitry such as voltage-controlled oscillators (VCOs). *See, e.g.,* Niknejad (2000) (EX-1009) at 50-67; Fong (EX-1027) at 69-75; Yuan (EX-1018) at 47. Indeed, the '582 Patent acknowledges that, "[i]n design of circuits such as a

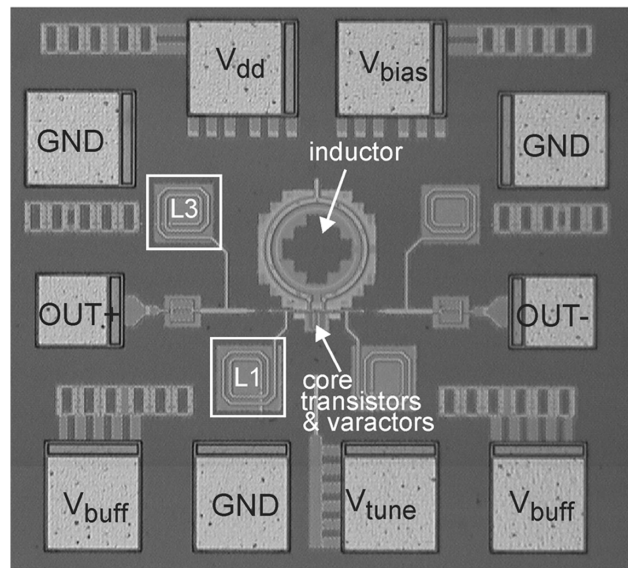
filter, a network impedance matching circuit, a voltage-controlled oscillator (VCO), a transmitting and receiving module circuit,” using a LC resonant circuit in a semiconductor device was known in the art. ’582 Patent (EX-1001) at 1:35-36.

86. An oscillator is an electronic circuit that produces a periodic signal. The frequency of an oscillator is determined by the property of an oscillator circuit, and often, is required to be varied by an external control. If the oscillation frequency is controlled by a voltage input, it is called a voltage-controlled oscillator (VCO). Niknejad (2007) (EX-1010) at 18; Park (EX-1021) at 22. Consequently, a VCO can be used for frequency modulation (FM) or phase modulation (PM) by applying a modulating signal to the control input. Niknejad (2007) (EX-1010) at 18. LC-based VCOs with spiral inductors offer the advantage of a low level of phase noise, which measures the spectral purity of a signal a VCO generates. Yuan (EX-1018) at 10; Fong (EX-1027) at 75.

87. LC-based VCOs are widely used in wireless communication systems. Yuan (EX-1018) at 10; Park (EX-1021) at 26; Niknejad (2007) (EX-1010) at 16, 139. For instance, a VCO is a key component in a wireless transceivers, as the VCO can generate a local oscillator (LO) frequency, which drives receive and transmit mixers by either converting a received signal from radio frequency (RF) to intermediate frequency (IF) or similarly converting an IF signal to RF for transmission. Niknejad (2000) (EX-1009) at 50-51.

88. When implementing an LC resonant circuit as part of a VCO, it was well known that, in terms of spatial relationship between inductor and capacitor components, a capacitor would commonly be offset from an inductor coil. In other words, the capacitor would be placed outwards relative to the inductor coil and not substantially overlapped with the inductor coil. Such layouts were extremely common in VCO designs well before the time of the '582 filing. Below I list a dozen exemplary figures from prior art references that illustrate such spatial relationships between inductor and capacitor/varactor components inside VCOs. Numerous other examples can be provided if needed.

1. See, e.g., Changhua Cao et al., *Millimeter-Wave Voltage-Controlled Oscillators in 0.13-um CMOS Technology*, IEEE Journal of Solid-State Circuits, Vol. 41, Issue 6 (June 2006) (“Cao”) (EX-1022) at 5, Fig. 7(a):



2. Yue Wu et al., *A Temperature Stabilized CMOS VCO for Zero-IF Cellular CDMA Receivers*, Digest of Technical Papers, 2005 Symposium on VLSI Circuits, June 16-18, 2005 (“Wu”) (EX-1023) at 4, Fig. 10:

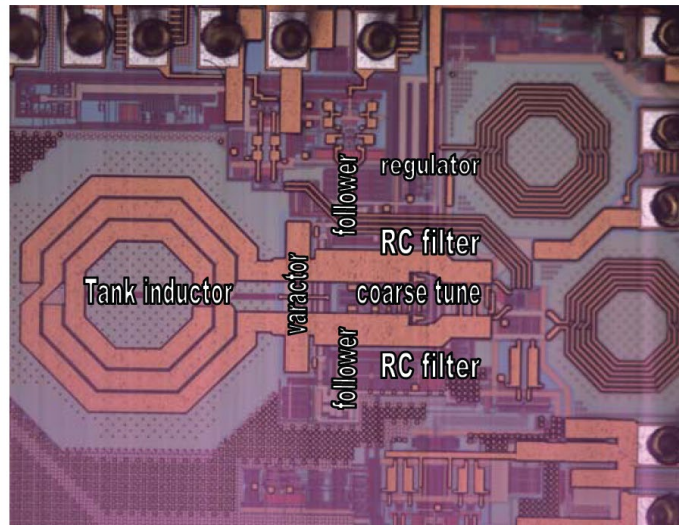


Fig. 10 Microphotograph of temperature stabilized CMOS VCO

3. Dorra Mellouli et al., *Design and Implementation of A 6-GHz Array of Four Differential VCOs Coupled Through a Resistive Network*, Analog Integrated Circuits and Signal Processing, Vol. 76, pp. 179-193 (2013) (“Mellouli”) (EX-1024) at 12, Fig. 10:

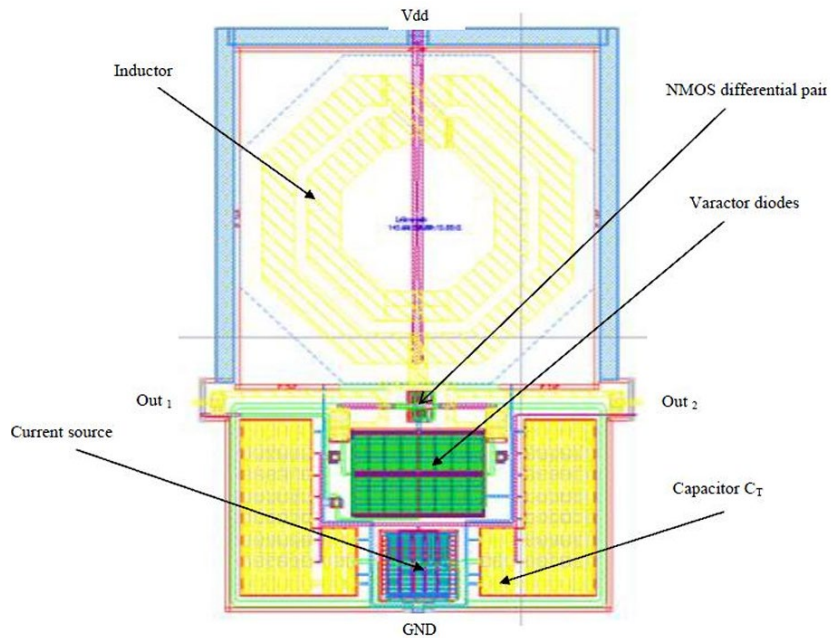


Figure 10. LC-VCO Layout

4. Xiao Shimao et al., *A novel 2.95–3.65 GHz CMOS LC-VCO using tuning curve compensation*, Journal of Semiconductors, Vol. 30, No. 10, 105001 (Oct. 2009) (“Xiao”) (EX-1025) at 4, Fig. 5:

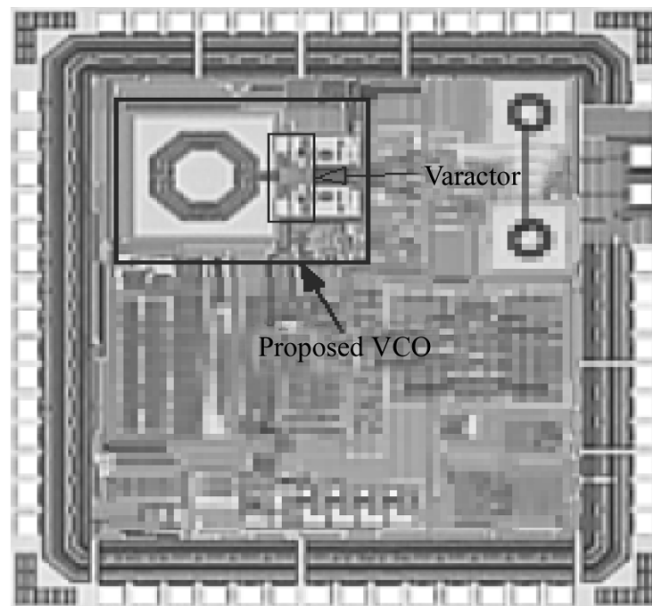


Fig. 5. Die microphoto.

5. Mohammad Nariman et al., *A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS*, 2010 IEEE Radio Frequency Integrated Circuits Symposium, May 23-25, 2010, pp. 157-160 (“Nariman”) (EX-1026) at 5, Fig. 8:

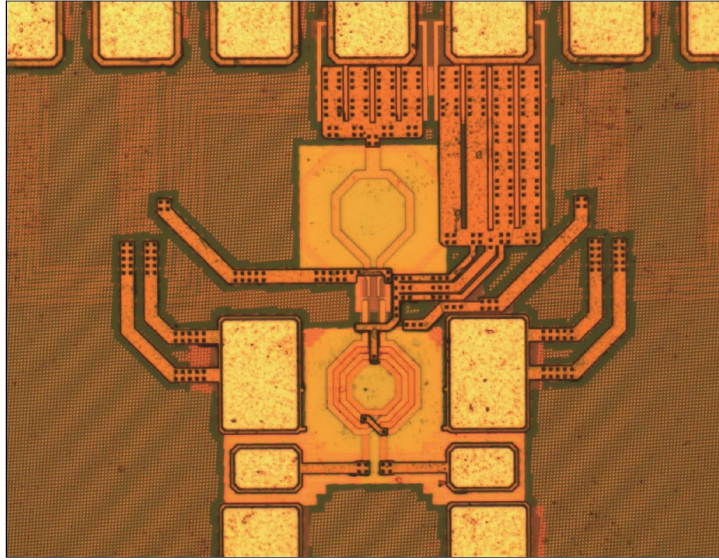


Fig. 8. Micrograph of the 300 μm * 500 μm VCO.

6. Neric H. W. Fong, PhD Dissertation entitled *Low-Voltage Radio-Frequency CMOS Integrated Circuits in Silicon-On-Insulator*, Department of Electronics, Carleton University, Ottawa, Canada (May 23, 2002) (“Fong”) (EX-1027) at 107, Fig. 4.26:

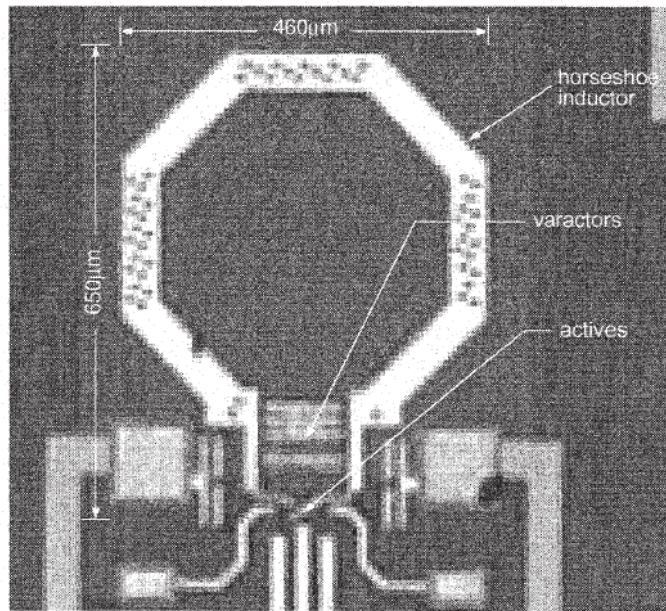


Figure 4.26 Micrograph of band-switching/differentially-tuned VCO

7. Babak Soltanian et al., *An Ultra Compact Differentially Tuned 6 GHz CMOS LC VCO with Dynamic Common-Mode Feedback*, IEEE 2006 Custom Integrated Circuits Conference, Sept. 10-13, 2006 (“Soltanian”) (EX-1028) at 5, Fig. 6:

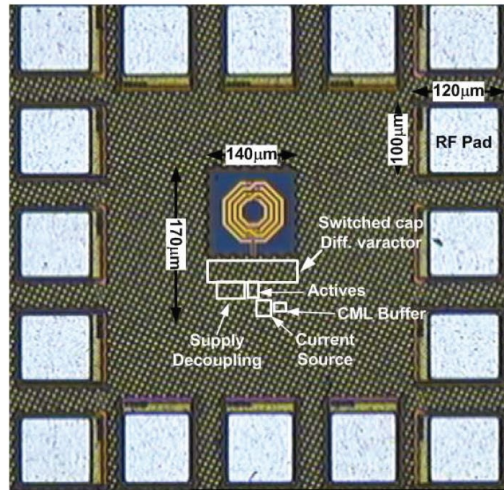


Fig. 6. Die photograph of the VCO test site fabricated in 90nm bulk CMOS; the active and tuning components are covered by metal fills and not visible, but the occupied area is highlighted.

8. V. Macaitis et al., Design of 4.48–5.89 GHz LC-VCO in 65 nm RF CMOS Technology, *Elektronika Ir Elektrotechnika*, Vol. 20, NO. 2, pp. 44-47 (Feb. 5, 2014) (“Macaitis”) (EX-1029) at 3, Fig. 4:

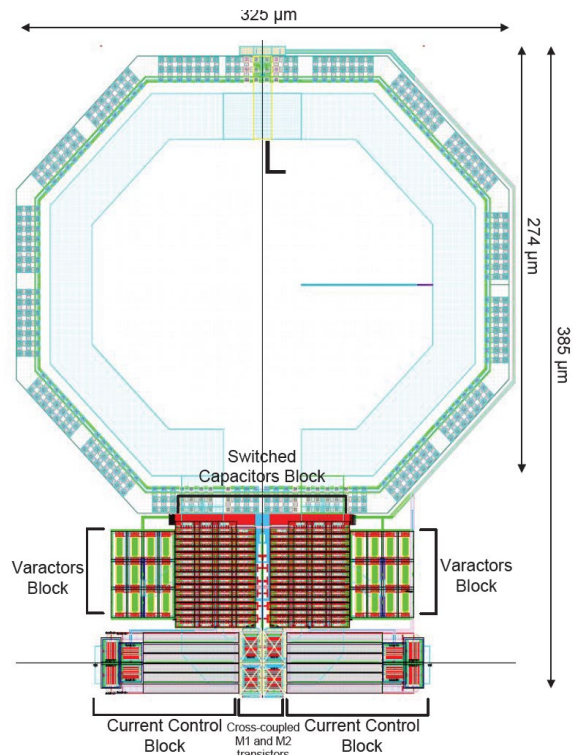


Fig. 4. Layout of the proposed LC-VCO.

9. Judith Maget, *Varactors and Inductors for Integrated RF Circuits in Standard MOS Technologies*, Institute of Electronics at the University of Bundeswehr (2002) (“Maget”) (EX-1030) at 65, Fig. 5.12:

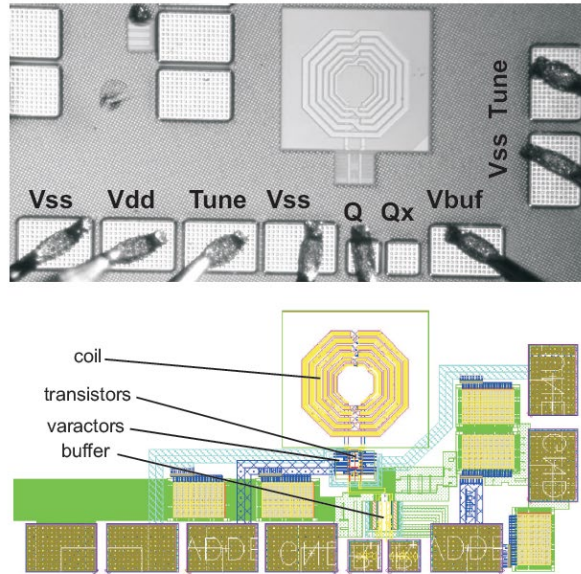
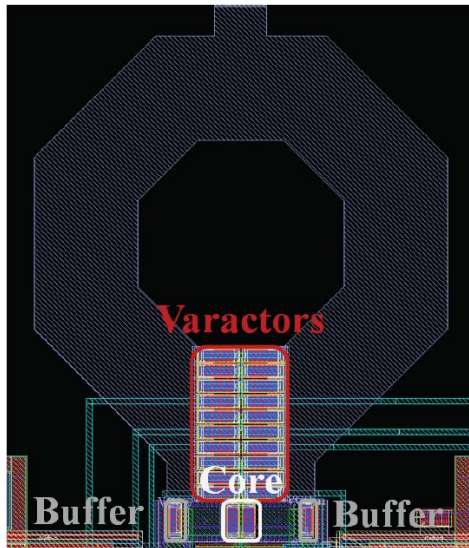
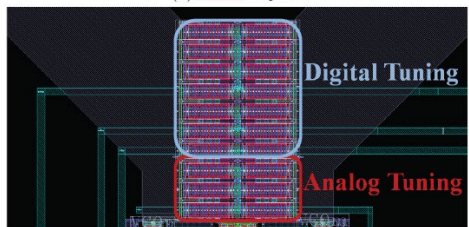


Figure 5.12: Die photograph and layout of one VCO. Metal fill structures are suppressed in the area of the inductor and the VCO-core.

10. Paolo Lucchi, PhD Dissertation entitled Frequency generation for mm-Wave and satellite applications, University of Bordeaux (Feb. 2012) (“Lucchi”) (EX-1031) at 71, Fig. 3.30:



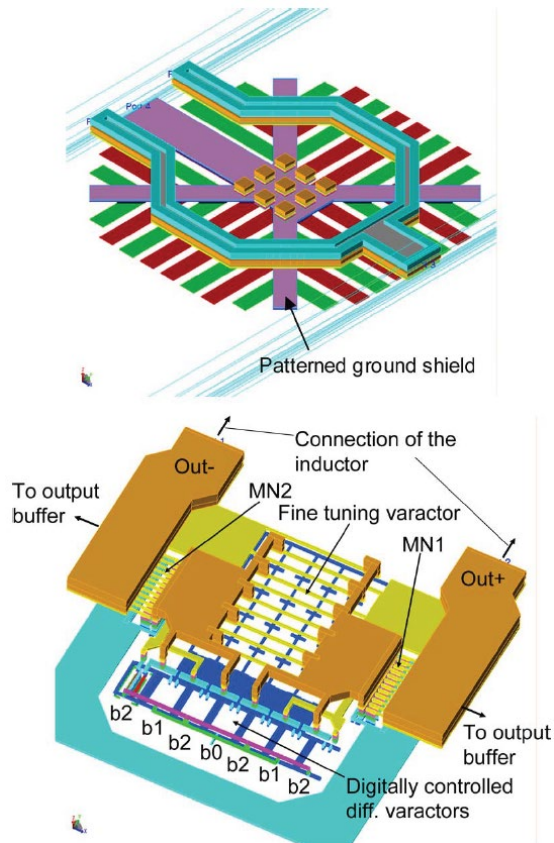
(a) VCO Layout.



(b) Varactors layout.

Figure 3.30: VCO layout.

11. J. Gonzalez et al., *A 56-GHz LC-Tank VCO With 17% Tuning Range in 65-nm Bulk CMOS for Wireless HDMI*, IEEE Transactions on Microwave Theory and Techniques, Vol. 58, Issue 5 (May 2010) (“Gonzalez”) (EX-1005) at 8, Fig. 8:



12. Matthew Muh, Master of Science thesis entitled *Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO*, Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley (2005) (“Muh”) (EX-1006) at 58, Fig. B-3:

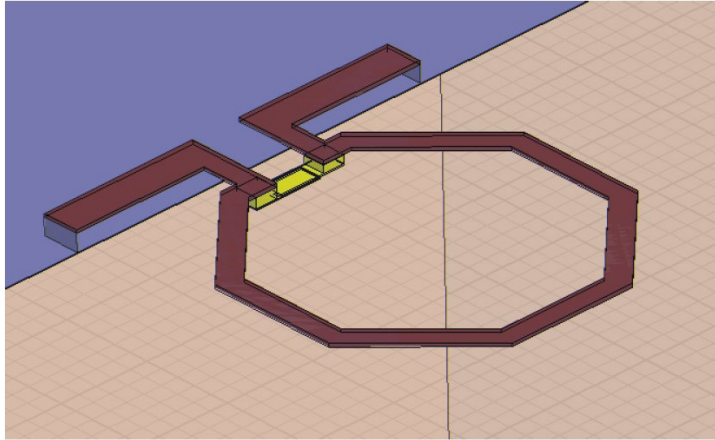


Figure B-3. HFSS model of parallel resonant tank on test chip.

89. As a POSITA would have recognized, VCO designs where a capacitor component is offset from an inductor coil, such as those illustrated above, have various benefits. For example, such designs facilitate the placement of interconnections between capacitor and inductor components by maximizing the use of vias and minimizing the use of lateral interconnections which saves fabrication cost and time. *See, e.g.,* Macaitis (EX-1029) at 2 (stating that the layout of its LC-VCO, i.e., example No. 8 in the preceding paragraph, “can not only reduce the effects of parasitic parameters but also improve the match between devices. In order to avoid as much as possible parasites, layout elements are oriented in minimum distances to each other and connected with the shortest as possible nets.”); Muh (EX-1006) at Fig. B-3 (showing vias directly connecting a capacitor to an inductor without need for lateral interconnections); Gonzalez (EX-1005) at Fig. 8 (same). In addition, as plainly visible from the figures illustrated above, by placing a capacitor under (and being overlapped with) an input/output

part of an inductor, the lateral footprint of the LC tank can be minimized.

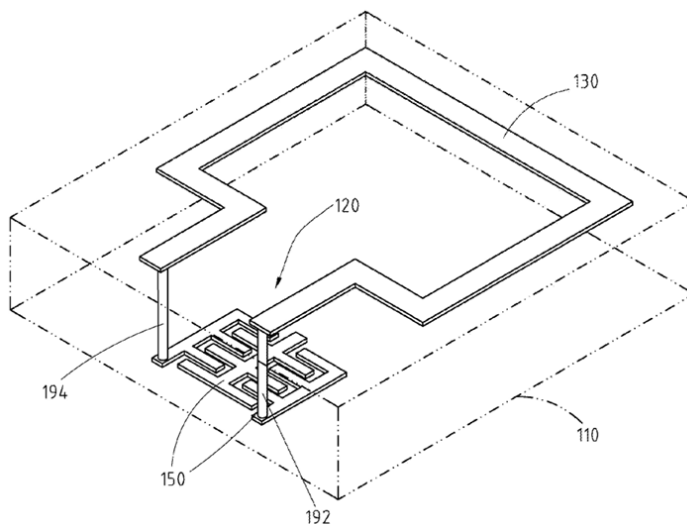
Therefore, a given amount of lateral area/space on a semiconductor device can fit in more LC tanks or other circuits.

V. THE '582 PATENT

A. Introduction

90. The '582 Patent is directed to a semiconductor device with an inductor-capacitor (LC) resonant circuit. '582 Patent (EX-1001) at 1:16-17. In the background section, the '582 Patent acknowledges that, “[i]n design of circuits such as a filter, a network impedance matching circuit, a voltage-controlled oscillator (VCO), a transmitting and receiving module circuit,” using a LC resonant circuit in a semiconductor device was known in the art. *Id.* at 1:35-36.

91. Fig. 4 of the '582 Patent depicts a representative embodiment of the LC resonant circuit.



Id. at Fig. 4.

92. According to the '582 Patent, “the semiconductor device with an LC resonant circuit includes an insulation layer 110 (hereinafter referred to as a first insulation layer 110), an inductor component 130, and a capacitor component 150.” '582 Patent (EX-1001) at 3:9-12. As illustrated in Fig. 5, the inductor component 130 includes a coil-conductor segment 131 and two extension-conductor segments 133 and 135. The coil-conductor segment 131 serves as an induction part of an inductor for the electromagnetic induction. The extension-conductor segments 133 and 135 serve as an input/output part for receiving or transmitting a signal. *Id.* at 3:22-27.

93. The two extension-conductor segments 133 and 135 are arranged at an interval and coupled to two ends of the coil-conductor segment 131, respectively. *Id.* at 3:33-35. Fig. 4 shows the two extension-conductor segments 133 and 135 are located at a same side of the coil-conductor segment 131. A first region 120 is defined by the two extension-conductor segments 133 and 135 and the coil-conductor segment 131. *Id.* at 3:45-47.

94. The capacitor component 150 is arranged, corresponding to the first region 120, on a lower surface of the first insulation layer 110, opposite to the inductor component 130. *Id.* at 3:48-52. In other words, the capacitor component 150 is located below the first region 120 and spaced by the first insulation layer 110 from the inductor component 130. *Id.* at 3:53-55.

95. Notably, the capacitor component 150 is arranged on the first insulation layer 110's surface "in an embedded manner." *Id.* 3:50-52. As the '582 Patent acknowledges in its background section, it was well known that, "in order to reduce the volume of an electronic product, various electronic elements [such as capacitor components] are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT)." 'Id. at 1:29-32; *see also id.* at 8:40-42 ("Here, the structures of various embedded electronic elements are well known to in the field, and therefore are no longer elaborated.").

96. As shown in Fig. 5 below, the capacitor component 150 includes two connecting segments 151 and 152 and a plurality of electrode segments 155 and 156. The electrode segments 155 and 156 serve as electrode plates of the capacitor, capacitive induction is generated between the electrode segments 155 and 156. The connecting segments 151 and 152 are used for connecting the capacitor component 150 to other circuit components (e.g., receiving or transmitting a signal from the inductor component 130). *Id.* at 4:41-45.

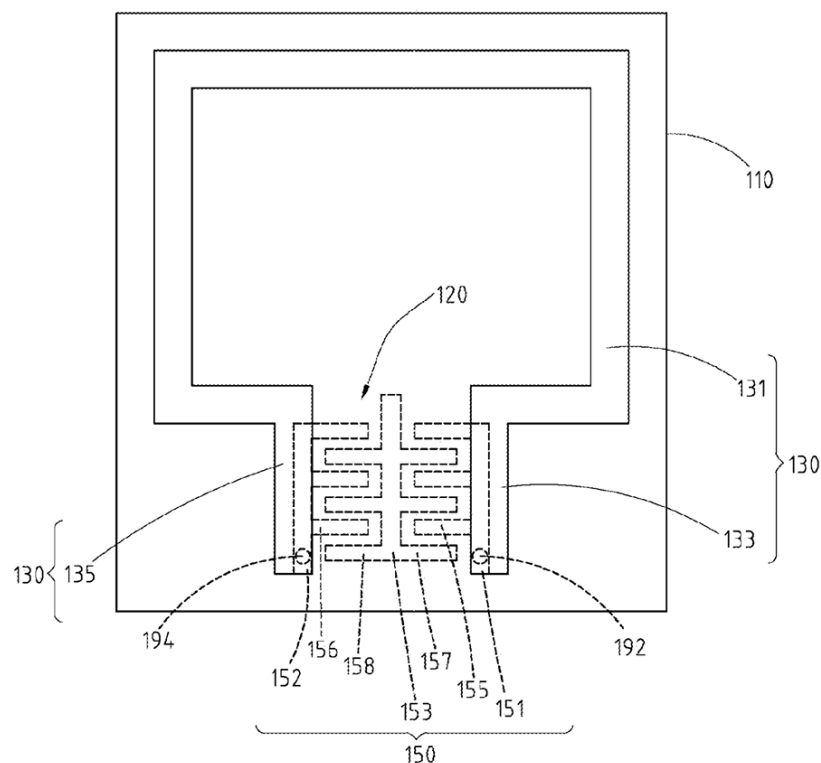


FIG. 5

Id. at Fig. 5.

97. Notably, the '582 Patent discloses “capacitors in various forms, such as a metal-oxide-metal (MOM) capacitor, a metal-insulator-metal (MIM) capacitor, or a metal-oxide-semiconductor (MOS) capacitor,” and acknowledges that “the structures of the capacitors in various forms are well known in the field.” *Id.* at 12:11-16. For instance, the '582 Patent's Fig. 12 shows a capacitor component 150' which is a “MOS capacitor.” *Id.* at 12:16-17.

B. Prosecution History

98. The '582 Patent issued from U.S. Patent Application Serial No. 14/338,904 (the “'904 Application”), filed July 23, 2014. During prosecution of the

'904 Application, there were several rounds of substantive office actions and responses, and the original claims were amended extensively before allowance.

99. Specifically, the as filed '904 Application had 10 claims. The only independent claim 1 recited:

1. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer.

'904 Application filed July 23, 2014, p. 25 (EX-1002 at 426).

100. On September 30, 2015, the examiner issued a first (non-final) office action rejecting all claims 1-10 as indefinite under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA) and rejecting claims 1-4 and 6-10 as being anticipated by Daley et al. US 2009/0322447 ("Daley") under 35 U.S.C. 102(a)(1). *See* Office Action dated Sept. 30, 2015, pp. 3-5 (EX-1002 at 342-344). In response, Applicants amended claims and argued against Daley. Claim 1 was amended as follows:

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer,

wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment.

Dec. 30, 2015 Response to Office Action, p. 2 (EX-1002 at 326).

101. On March 18, 2016, the examiner issued a second (non-final) office action rejecting claims 1-4 and 6-10 again as being anticipated by Daley. *See* Office Action dated Mar. 18, 2016, pp. 2-5 (EX-1002 at 315-319). In response, Applicants amended claims again and argued against Daley. Claim 1 was amended as follows:

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.

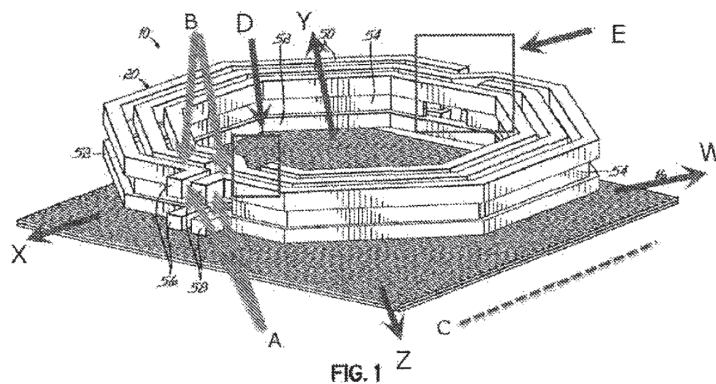
June 17, 2016 Response to Office Action, p. 2 (EX-1002 at 70).

102. Notably, in their June 17, 2016 response, Applicants argued the following against Daley:

Figure 1 of Daley clearly recites that the capacitor 16 covers with the **WHOLE** of the inductor 20.

In other words, in Daley, the four comers of capacitor 16 are **NOT arranged corresponding to the region defined by TWO conductor segments** (annotated as A shown in following FIG. 1) **and the coil-conductor segment** (the signal line 50 shown in following FIG. 1).

...



Id. at p. 5-6 (EX-1002 at 73-74) (emphasis in original).

103. On July 28, 2016, the examiner issued a third (final) office action rejecting claims 1-4 and 6-10 yet again as being anticipated by Daley. *See* Office Action dated Jul. 28, 2016, pp. 2-5 (EX-1002 at 58-61). In response, Applicants amended claims again, added new claim 11, and argued against Daley. Claim 1 was amended as follows:

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:
 - a first insulation layer;
 - an inductor component, comprising:
 - a coil-conductor segment, located on a surface of the first insulation layer; and
 - two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and
 - a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially vertically aligned ~~overlapped~~ with the coil-conductor segment.

Sept. 16, 2016 Response to Office Action, p. 2 (EX-1002 at 47).

104. Shortly after the Applicants' response, an examiner-initiated interview was conducted on September 26, 2016, with the following summary:

Claim(s) discussed: 1.

Identification of prior art discussed: Daley et al. (of record) and Jing et al. US 2015/0145615.

Substance of Interview

(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

The Examiner notified the Applicant that the amendment made to claim 1 (see Amended claims dated 9/16/2016) does not overcome the reference of record Daley et al. Further, a new search was conducted within the allotted time and the Examiner cites a new prior art that also reads on claim 1. Jing et al. discloses in Fig. 5 a semiconductor device with an LC circuit comprising the limitations recited within claim 1. The Examiner notified the Applicant that the amendment dated 9/16/2016 will not be entered. The Applicant acknowledged and stated that an RCE will most probably be submitted.

Sept. 26, 2016 Examiner-Initiated Interview, p. 2 (EX-1002 at 41).

105. Since Applicants' claim amendments in their Sept. 16, 2016 Response were not entered, Applicants amended claims again in a subsequent response on October 28, 2016. Claim 1 was amended as follows:

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,

wherein the capacitor component comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

Oct. 28, 2016 Response to Office Action, p. 2 (EX-1002 at 27).

106. Eventually, on November 22, 2016, the examiner allowed the '904 Application because the examiner believed the closest prior art of record (US Patent No. 9,270,247 ("Jing")) discloses all limitations of claim 1 except "wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments." Specifically, the examiner issued the following reasons for allowance:

The following is an examiner's statement of reasons for allowance: As per claims 1 and 11, the closest prior art Jing et al. US Patent 9,270,247 (of record) discloses in Fig. 7 a semiconductor device with an LC resonant circuit comprising all of the limitations recited therein **EXCEPT** “wherein the plurality of connecting segments of the capacitor component are respectively overlapped with **the two extension-conductor segments**”. Jing et al. discloses an inductor component 705 including legs or “extension-conductor segments” 715 and 720. The inductor 705 is connected to TWO separate finger capacitors or “capacitor components” 725 and 730. Each of the capacitor components overlaps with only a single one of the “extension-conductor segments” in a vertical direction and not both (i.e. “the two extension-conductor segments”) as recited within the claims. Further, each of the finger capacitors or “capacitor components” 725 and 730 is its own separate capacitor structure separated by switches 735 as shown in Fig. 7, and thus elements 725 and 730 together cannot be interpreted as “a capacitor component”.

Nov. 22, 2016 Notice of Allowability, pp. 2-3 (EX-1002 at 12-13) (emphasis in original).

107. For reference, Fig. 7 of the cited reference Jing is reproduced below.

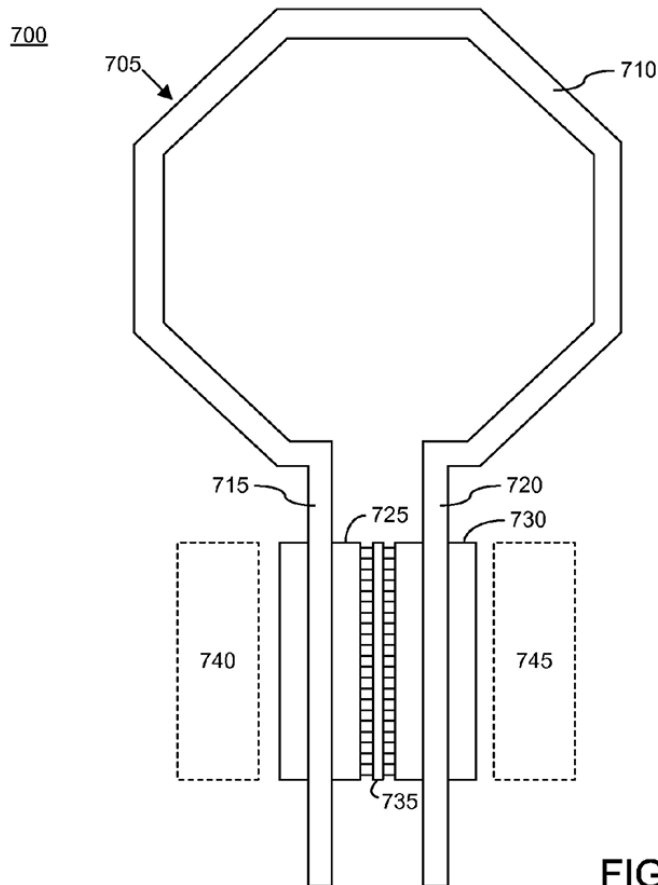


FIG. 7

Jing (EX-1033) at Fig. 7.

108. Notably, none of the prior art relied on for invalidity grounds herein was considered by the Examiner during prosecution.

C. Overview of the Challenged Claims

109. Claim 1 of the '582 Patent is directed to a semiconductor device with an inductor-capacitor (LC) resonant circuit, where an inductor component and a capacitor component have certain shapes and certain spatial relationship to each other. Claim 1 is reproduced below.

1. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;
an inductor component, comprising:
a coil-conductor segment, located on a surface of the first insulation layer; and
two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and
a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,
wherein the capacitor component comprises:
a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and
a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

110. Dependent claim 2, depending from claim 1, further recites a second insulation layer and another electronic component laid out similar to how the first insulation layer and capacitor component are respectively laid out in claim 1.

Claim 3, depending from claim 2, defines the electronic component to be one of another capacitor component, a transistor component, a diode component, and a resistor component.

111. Dependent claim 4, depending from claim 1, further recites “the first region is defined *between* the two extension-conductor segments.” This language differs from claim 1, which recites “a first region is defined *by* the two extension-conductor segments and the coil-conductor segment.” Claim 5, depending from claim 4, further recites “the first region is defined between the two extension-conductor segments and the coil-conductor segment.”

112. Independent claim 9 is the same as claim 1 except that it is broader as it does not have the following limitation of claim 1: “wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.”

VI. GROUND 1: CLAIMS 1-5 AND 9 OF THE '582 PATENT ARE OBVIOUS UNDER 35 U.S.C. § 103 OVER GONZALEZ

113. Gonzalez discloses an LC resonant circuit as part of a VCO. The shape and geometry of the inductor and capacitor components disclosed in Gonzalez are materially the same as the LC resonant circuit claimed in the '582 Patent.

A. Gonzalez Introduction

114. Gonzalez is an article entitled “A 56-GHz LC-Tank VCO With 17% Tuning Range in 65-nm Bulk CMOS for Wireless HDMI” authored by José Luis Gonzalez et al. and published on the IEEE Transactions on Microwave Theory and

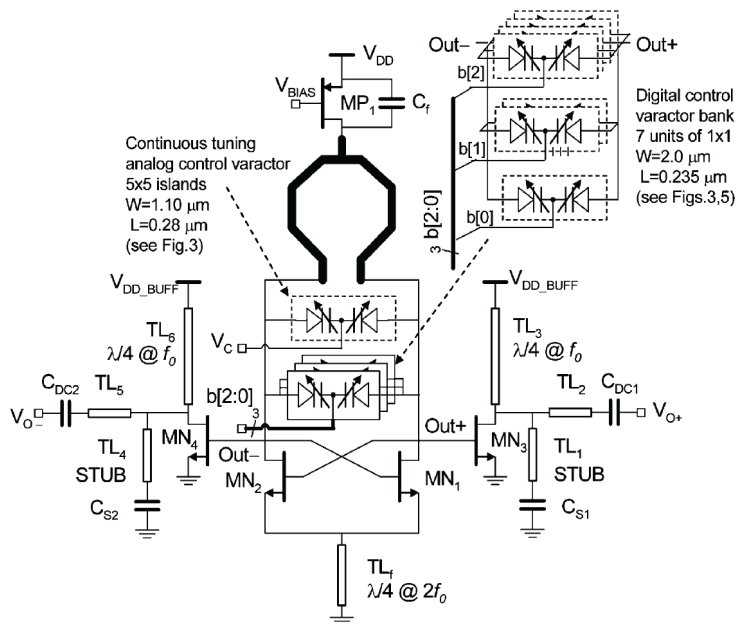
Techniques (Volume: 58, Issue: 5) in May 2010

(<https://ieeexplore.ieee.org/document/5438827>), nearly four years before the earliest application in the 582 patent priority chain. EX1005 at 1.

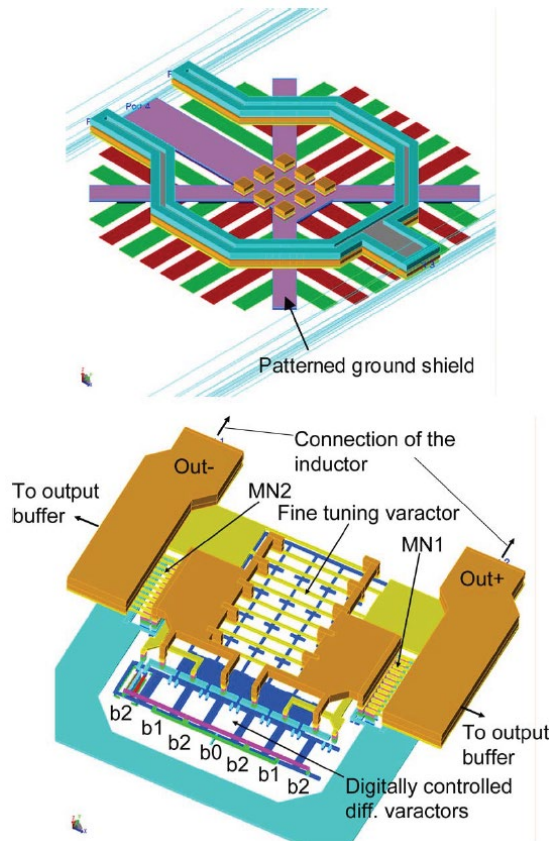
115. Gonzalez discloses a “voltage-controlled oscillator (VCO)” whose “oscillation frequency is tuned both by an analog input and by a 3-bit digital control bus using the same type of differential varactors.” Gonzalez (EX-1005) at Abstract. “The VCO is implemented in a 65-nm bulk CMOS process,” which was commonly used at that time. *Id.* Gonzalez’s VCO design is advantageous in that it “achieves a record figure of merit, considering tuning range of 186.8 dBc/Hz and is able to address the full wireless high-definition multimedia interface band.” *Id.*

116. Gonzalez’s VCO includes, among other components, an inductor-capacitor (LC) resonant circuit, called an LC tank. *See* Gonzalez (EX-1005) at 4 (“The oscillator core is composed of an NMOS cross-coupled pair (MN1, MN2) and an LC tank.”). Particularly relevant to the ’582 Patent, the LC tank includes an inductor, a fine tuning variable capacitor (varactor), and a coarse tuning varactor. *Id.* at 5-6 (“The tank inductance is a single-turn inductor with a central tap. . . . A differential N+poly/Nwell varactor operating in accumulation mode is used for continuous tuning. . . . An additional bank of digitally controlled differential varactors provides coarse tuning”). The LC tank is a resonant circuit that has a “self-resonant frequency.” *Id.* at 5.

117. In Gonzalez's LC tank, the inductor and the fine tuning varactor are positioned relative to each other in the same manner as the LC arrangement described and claimed in the '582 Patent. For instance, a schematic of Gonzalez's VCO is depicted in Fig. 2, and a physical design of the VCO is depicted in Fig. 8, both reproduced below. As shown in Fig. 2 and Fig. 8, Gonzalez's inductor is a horseshoe-shaped "single-turn inductor with a central tap," and its fine tuning varactor includes comb or finger-shaped electrodes interdigitally connected to the left and right sides of the varactor (see yellow metal layer in the bottom half of Fig. 8). The fine tuning varactor is offset from the coil of the horseshoe-shaped inductor and is instead aligned with extension segments of the horseshoe-shaped inductor.



Gonzalez (EX-1005) at Fig. 2 ("VCO and output buffers schematic").



Gonzalez (EX-1005) at Fig. 8 (“Inductor layout (top) and interconnection of varactors and structure of transistors (bottom).”).

B. Gonzalez Invalidates Claim 1

1.1 A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

118. To the extent this preamble of claim 1 is a limitation, Gonzalez discloses it, as Gonzalez discloses a semiconductor device with an LC resonant circuit. For instance, Gonzalez discloses an oscillator core circuit that includes “an LC tank.” Gonzalez (EX-1005) at 4. The LC tank includes an inductor and multiple variable capacitors (varactors). *Id.* at 5-6 (“The tank inductance is a

single-turn inductor with a central tap. . . . A differential N+poly/Nwell varactor operating in accumulation mode is used for continuous tuning. . . . An additional bank of digitally controlled differential varactors provides coarse tuning”). The LC tank is a resonant circuit that has a “self-resonant frequency.” *Id.* at 5.

119. Further, Gonzalez’s “VCO circuit is implemented in a 65-nm bulk CMOS process” on a chip as part of a semiconductor device. *Id.* at 9. A top-view image of the semiconductor device, called a “die micrograph,” is shown in Fig. 12 of Gonzalez, reproduced below. *Id.*

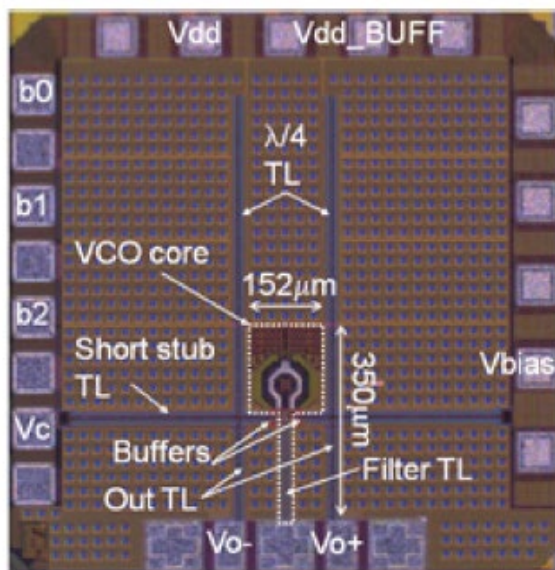


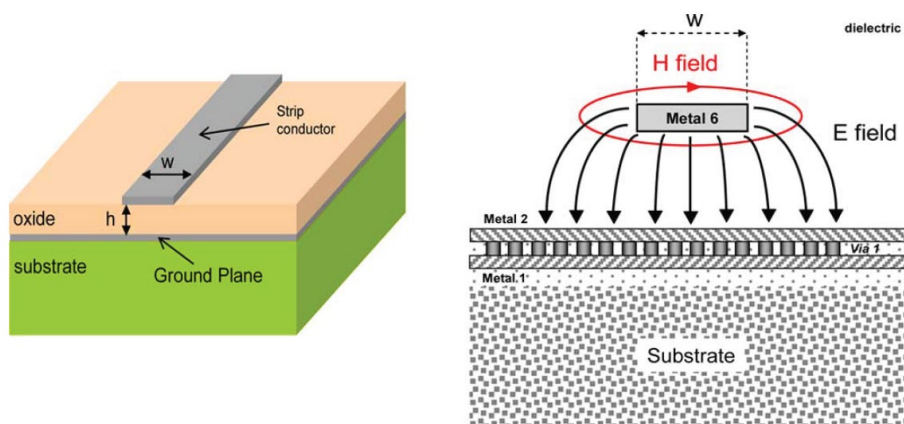
Fig. 12. VCO die micrograph.

Gonzalez (EX-1005) at Fig. 12 (VCO die micrograph)

1.2a first insulation layer

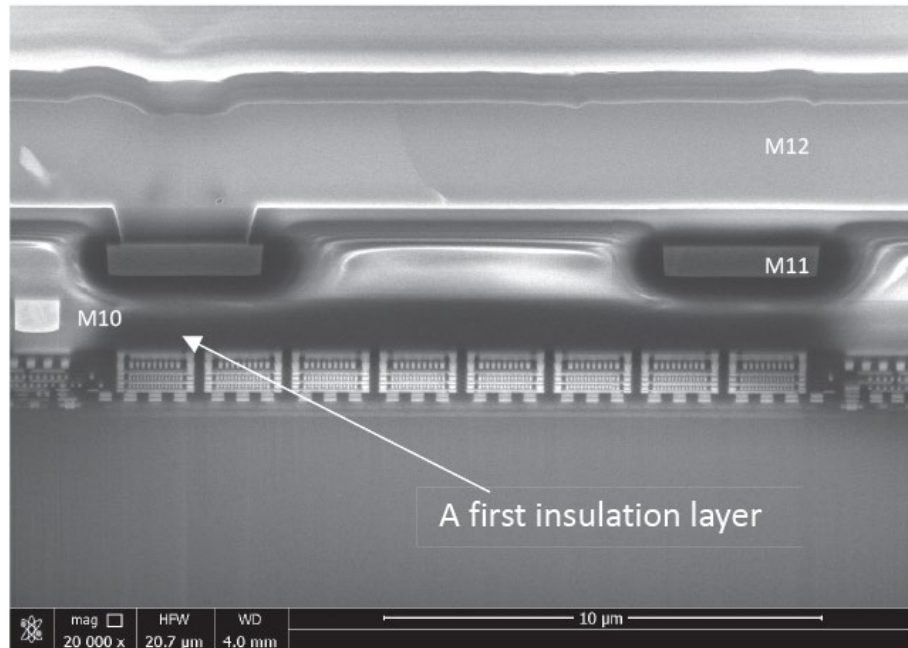
120. Gonzalez discloses this limitation. For example, Gonzalez’s Fig. 9 (reproduced below) discloses “a dielectric” layer, shown as an “oxide,” between a

top metal layer (M6) and a ground plane composed of two bottom metal layers (M1, M2). *Id.* at 8 (“Fig. 9 illustrates the realization of a microstrip line using the top metal level (M6) as a conducting strip and the two bottom metal levels (M1, M2) as ground plane”); *Id.* at 7 (“This microstrip line is made up of a conducting strip on a dielectric in parallel to a ground plane.”). A POSITA would have understood that a dielectric (e.g., an oxide) is an insulation material that can form one or more insulation layers. Therefore, part of Gonzalez’s dielectric material forms a first insulation layer.



Gonzalez (EX-1005) at Fig. 9.

121. This interpretation is consistent with how Realtek interprets the first insulation layer, as shown below.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 7 (Realtek annotations retained).

122. Gonzalez’s Fig. 9 illustrates an oxide between a strip conductor implemented on a top metal layer (M6) and a ground plane implemented on two bottom layers (M1 and M2) for the purpose of “showing electric and magnetic fields” generated by the strip conductor. Gonzalez (EX-1005) at 8. A POSITA would have understood that, between metal layers M6 and M2, additional metal layers can be (and indeed are) implemented inside the oxide, and that more than one insulation layers would be formed inside the oxide. *See, e.g., Id.* at 6 (“The inductor of the tank is a single-turn differential inductor made with the two upper copper metal layers plus the aluminum metallization layer.”); Fig. 8 (showing multiple metal layers for implementing a VCO core circuit). Such interweaved uses of insulation layers and metal layers in semiconductor devices were well

known in the art before the time of the '582 filing. Indeed, the '582 Patent acknowledges this in its background section. *See* '582 Patent (EX-1001) at 1:24-28 (“A typical semiconductor integrated circuit includes a silicon substrate. ***More than one insulation layer is arranged on the substrate, more than one metal layer ... is arranged in the insulation layer***, and the metal layers may be formed with a built-in part of a chip by means of a semiconductor fabrication process.”) (emphasis added).

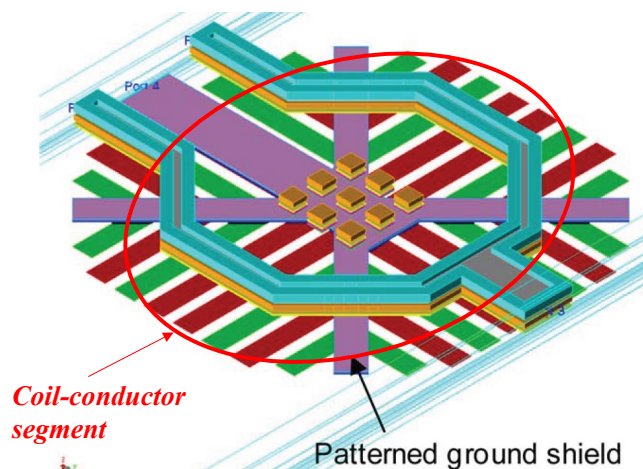
1.3 an inductor component, comprising

123. Gonzalez discloses this limitation. For example, Gonzalez's LC tank includes “a single-turn differential inductor,” which is an inductor component. *Id.* at 6. Gonzalez's inductor is shown in the VCO circuit schematic (Fig. 2, copied below) as a horseshoe-shaped structure. *Id.* at 5.

Gonzalez (EX-1005) at Fig. 8 top half (left); simplified view of Fig. 8 top half after removing patterned ground shield (right).

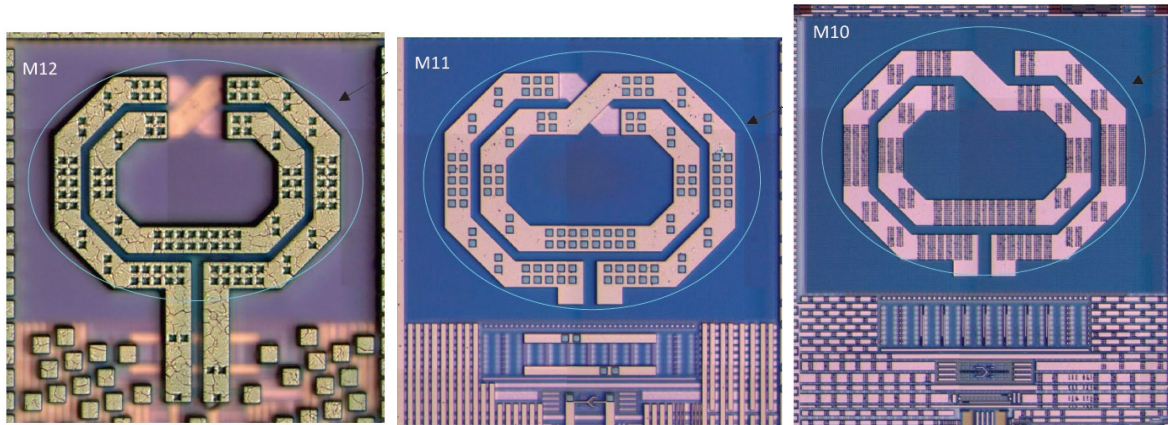
**1.4 a coil-conductor segment, located on a surface of the first insulation layer;
and**

125. Gonzalez discloses this limitation. For example, Gonzalez's inductor includes a coil-conductor segment, as illustrated in Fig. 8 below. The coil-conductor segment serves as an induction part of Gonzalez's inductor for electromagnetic induction. Gonzalez discloses its inductor has an inductance of "95 pH at DC" and 90 pH at a frequency of 60 GHZ. *Id.* at 6.



Gonzalez (EX-1005) at Fig. 8 top half (annotations added in red).

126. This interpretation is consistent with how Realtek interprets the coil-conductor segment of the inductor, as shown below, where the coil-conductor segment is marked by light blue ovals.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 9-10 (Realtek annotations retained).

127. The coil-conductor segment of Gonzalez’s inductor is located on a surface of the first insulation layer. For example, Gonzalez’s inductor is “implemented with a microstrip transmission line (TL).” Gonzalez (EX-1005) at 5. As illustrated in Fig. 9, the microstrip line is located on a surface of an oxide (dielectric) layer. *See also* Gonzalez (EX-1005) at Fig. 12 (a VCO die micrograph showing transmission lines (TL) implemented in a top metal layer on top of an insulation layer).

128. This interpretation is consistent with how Realtek interprets this limitation. *See* Realtek Exhibit 32 to ITC Complaint (EX-1034) at 9 (alleging that, in the accused products, “the coil-conductor segment is located on a surface of the first insulation layer (which is located approximately below the M10 layer)”).

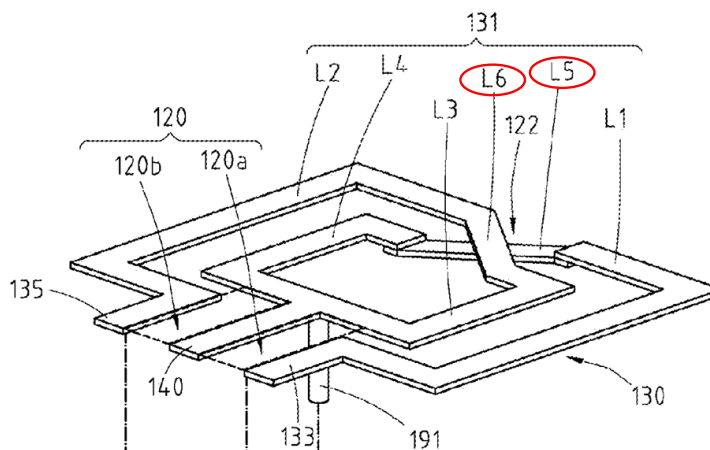
129. This paragraph explains the use of transmission lines in Gonzalez to provide helpful context, but it is not necessary for invalidating this limitation. Fig.

9 shows a “strip conductor” located on an oxide, which is an insulation material. The strip conductor—also called a “transmission line (TL),” “microstrip transmission line,” “microstrip line,” or “microstrip conductor” in Gonzalez—is realized “using the top metal level (M6) as a conducting strip” Gonzalez (EX-1005) at 8; *see also id.* (“The TL used in this study is illustrated in Fig. 9. This microstrip line is made up of a conducting strip on a dielectric in parallel to a ground plane.”). The transmission lines provide connections among different electronic components (e.g., inductor, filter, output) on the top metal level and facilitate transmission of signals. *See* Gonzalez (EX-1005) at Fig. 12 (marking various “TL” such as “Filter TL,” “Out TL,” Short stub TL”); *Id.* at 5 (“The VCO core circuit is completed with ... an inductor implemented with a microstrip transmission line (TL)”).

130. To the extent Gonzalez’s Fig. 8 does not expressly disclose a first insulation layer with a surface on which a coil-conductor segment of Gonzalez’s inductor is located, this would have been understandable to a POSITA, as the purpose of Fig. 8 is to show “[t]he layout of the interconnection between the varactors, the inductor, and the active sections of the VCO core and the buffers.” Gonzalez (EX-1005) at 7. Indeed, showing insulation layers in Fig. 8 would render electronic components on underlying layers invisible and therefore defeat the purpose of Fig. 8.

131. Despite not being expressly shown in Gonzalez's Fig. 8, it would have been obvious to a POSITA to use a first insulation layer with a surface on which a coil-conductor segment of Gonzalez's inductor is located. For example, Gonzalez discloses that its inductor is "made with the two upper copper metal layers plus the aluminum metallization layer" and that a microstrip line of its inductor uses "the top metal level (M6) as a conducting strip." Gonzalez (EX-1005) at 6, 8. In view of this disclosure in Gonzalez, a POSITA would have understood that the inductor's coil-conductor segment, like a microstrip line, would use the top metal level M6, and would also be located on a surface of the first insulation layer. In other words, Gonzalez's multi-layer coil-conductor segment is located on a surface of the first insulation layer because it includes one or more metal levels (e.g., M6, or M6+M5) located on a surface of the first insulation layer. This interpretation is consistent with how Realtek interprets the coil-conductor segment of the accused inductor, which includes multiple metal layers. *See* Realtek Exhibit 32 to ITC Complaint (EX-1034) at 9 (accusing "an inductor component, composed with at least three metal layers (M10-M12)"). And this interpretation is consistent with the '582 Patent itself. For example, the '582 Patent's claim 1 recites "a coil-conductor segment, located on a surface of the first insulation layer," and its claim 7 (depending from claim 1) recites "the coil-conductor segment has a pair of *staggered parts*." '582 Patent (EX-1001) at 13:2-3, 14:8-10 (emphasis added).

According to the '582 specification, the “staggered parts” (e.g., L5 and L6 as illustrated in Fig. 9 below) are multi-layer structures. *Id.* at 8:65-9:7 (“[R]eferring to FIG. 7 to FIG. 9, . . . the coil-conductor segment 131 includes a plurality of semi-loop lines L1, L2, L3, and L4 and at least one pair of staggered parts. . . . and each pair of staggered parts have ***two staggered guide lines L5 and L6.***”) (emphasis added). A POSITA would have understood that an insulation material would exist between the staggered guide lines L5 and L6 to prevent electric shorting between them. Therefore, L5 and L6 are located on different layers. But the '582 Patent claims its coil-conductor segment including the multi-layer structures is “located on a surface of the first insulation layer.” *Id.* at 13:2-3, 14:8-10. In the same way, Gonzalez’s coil-conductor segment including multi-layer structures would be located on a surface of the first insulation layer.

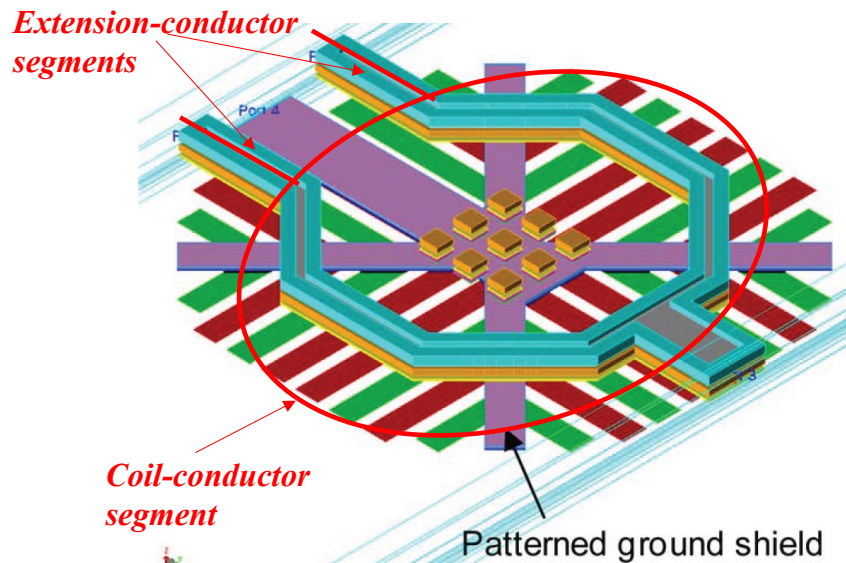


'582 Patent at Fig. 9 partial view (EX-1001) (annotations added in red).

132. Further, using an insulation layer in the claimed manner was well known in the art. Indeed, the '582 Patent acknowledges just that in its background section. *See* '582 Patent (EX-1001) at 1:24-28 (“A typical semiconductor integrated circuit includes a silicon substrate. ***More than one insulation layer is arranged on the substrate, more than one metal layer ... is arranged in the insulation layer***, and the metal layers may be formed with a built-in part of a chip by means of a semiconductor fabrication process.”) (emphasis added).

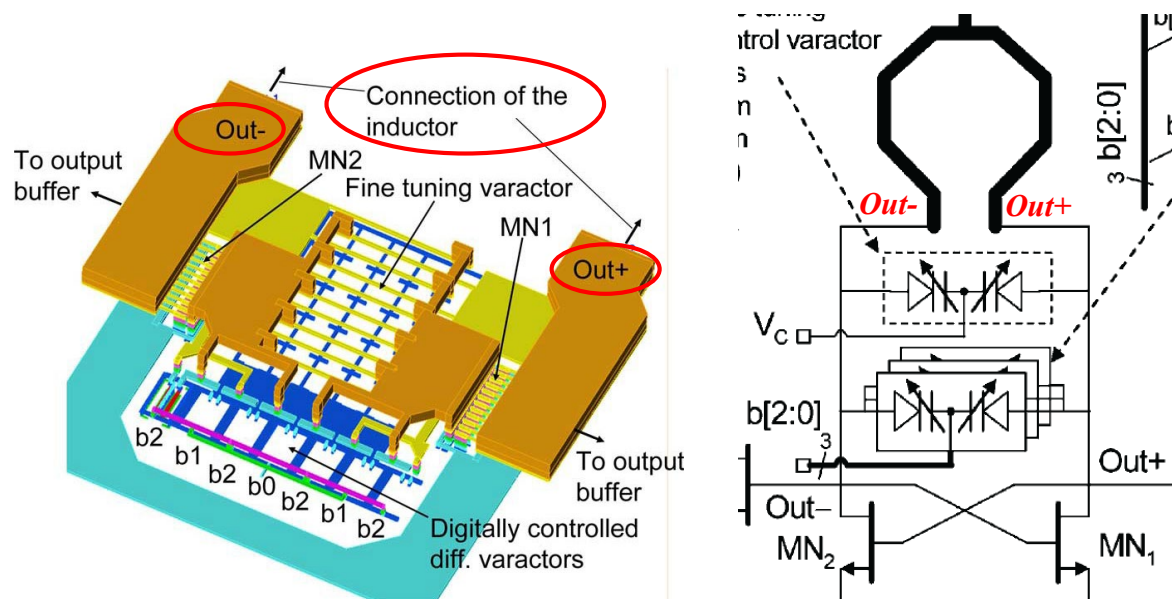
1.5 two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

133. Gonzalez discloses this limitation. For example, Gonzalez's inductor includes two extension-conductor segments, as illustrated in Fig. 8, reproduced below.



Gonzalez (EX-1005) at Fig. 8 top half (annotations added in red).

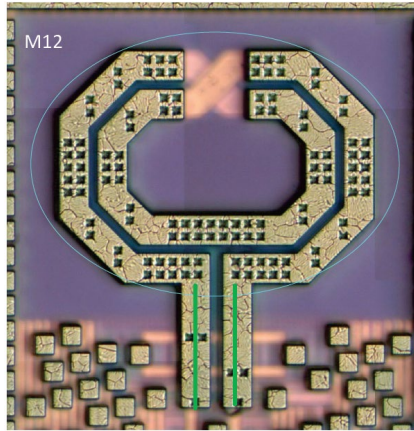
134. In Gonzalez, the extension-conductor segments serve as an input/output part of its inductor. For instance, each extension-conductor segment of Gonzalez’s inductor includes a “connection of the inductor,” as shown in the bottom half of Fig. 8, reproduced below. And the two extension-conductor segments are connected to “two differential terminals (Out+ and Out-)” respectively, as shown in Fig. 2 and the bottom half of Fig. 8. Gonzalez (EX-1005) at 3.



Gonzalez (EX-1005) at Fig. 8 bottom half (left); Fig. 2 partial view (right) (annotations added in red).

135. Like the coil-conductor segment of Gonzalez’s inductor, the two extension-conductor segments are located on the same surface of the first insulation layer. Further, as shown in Fig. 8, the two extension-conductor segments are coupled to two ends of the coil-conductor segment respectively, are arranged at an interval, and extend outwards relative to the coil-conductor segment.

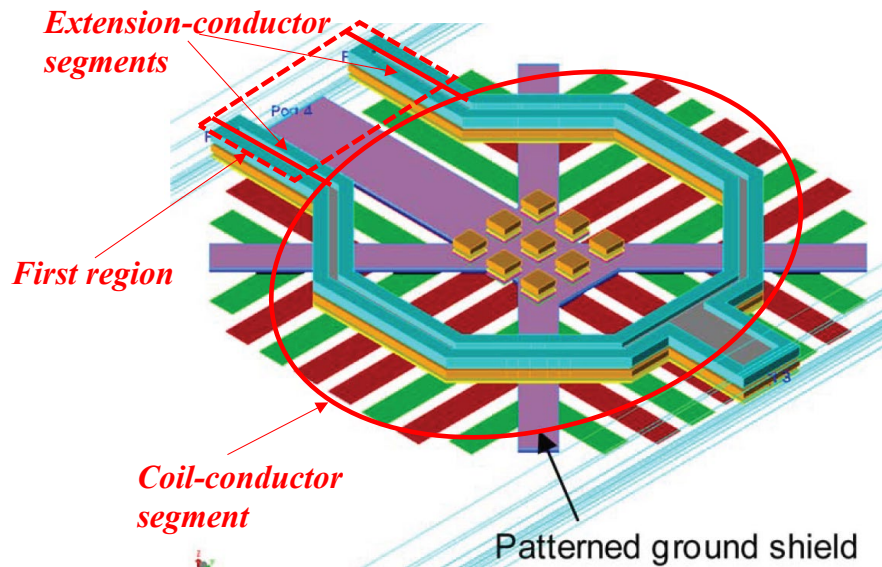
136. This interpretation is consistent with how Realtek interprets the two extension-conductor segments of the inductor, as shown below, where the extension-conductor segments are marked by green lines.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 11 (Realtek annotations retained).

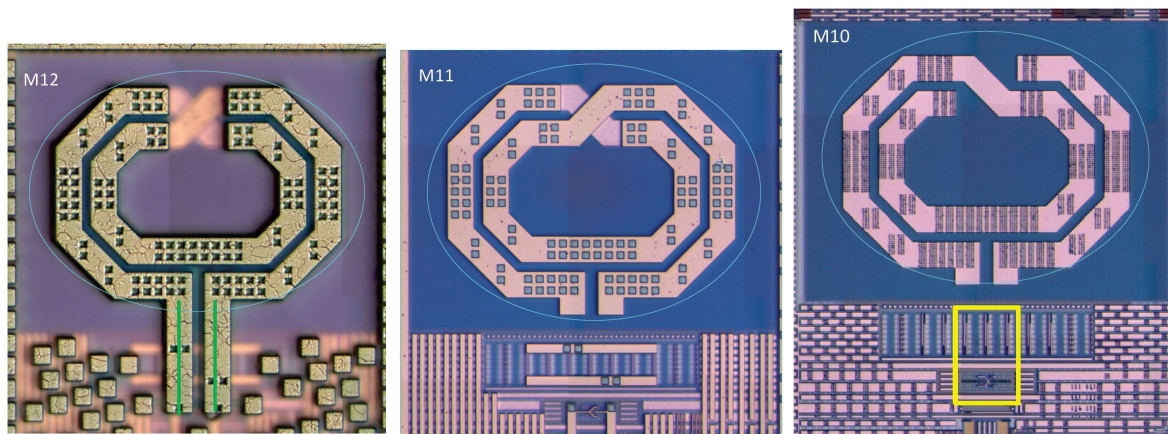
137. Further, based on how Realtek interprets the claim phrase “a first region defined by the two extension-conductor segments and the coil-conductor segment,”² Gonzalez discloses such a first region, as illustrated in Fig. 8 below.

² I believe this claim phrase is indefinite because its scope would not be reasonably clear to a POSITA. Specifically, the '582 Patent has two claims depending from claim 1 that respectively recite “wherein the first region is defined between the two extension-conductor segments” (claim 4) and “wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment” (claim 5). Therefore, under the doctrine of claim differentiation, the first region should be larger than a region defined between the two extension-conductor segments. Further, during prosecution of the '582 Patent, the applicant stated that the first region cannot cover the whole inductor. Therefore, based on the applicant’s statements during prosecution, the first region should be smaller than a region defined by the whole inductor. See Office Action Response dated June 17, 2016 at 5-6 (EX1002 at 73-74) (“Figure 1 of Daley clearly recites that the capacitor 16 covers with the WHOLE of the inductor 20. In other words, in Daley, the four corners of capacitor 16 are NOT arranged corresponding to the region defined by TWO conductor segments (annotated as A shown in following FIG. 1) and the coil-conductor segment (the signal line 50 shown in following FIG. 1).”) In such a context, a POSITA would not reasonably ascertain what is, or is not, covered by the first region. The only first region disclosed in the '582 specification (e.g., first region 120 shown in Fig. 6) appears



Gonzalez (EX-1005) at Fig. 8 top half (annotations added in red).

138. This interpretation is consistent with how Realtek interprets the claimed “first region,” as shown below, where the first region is marked by a yellow box.



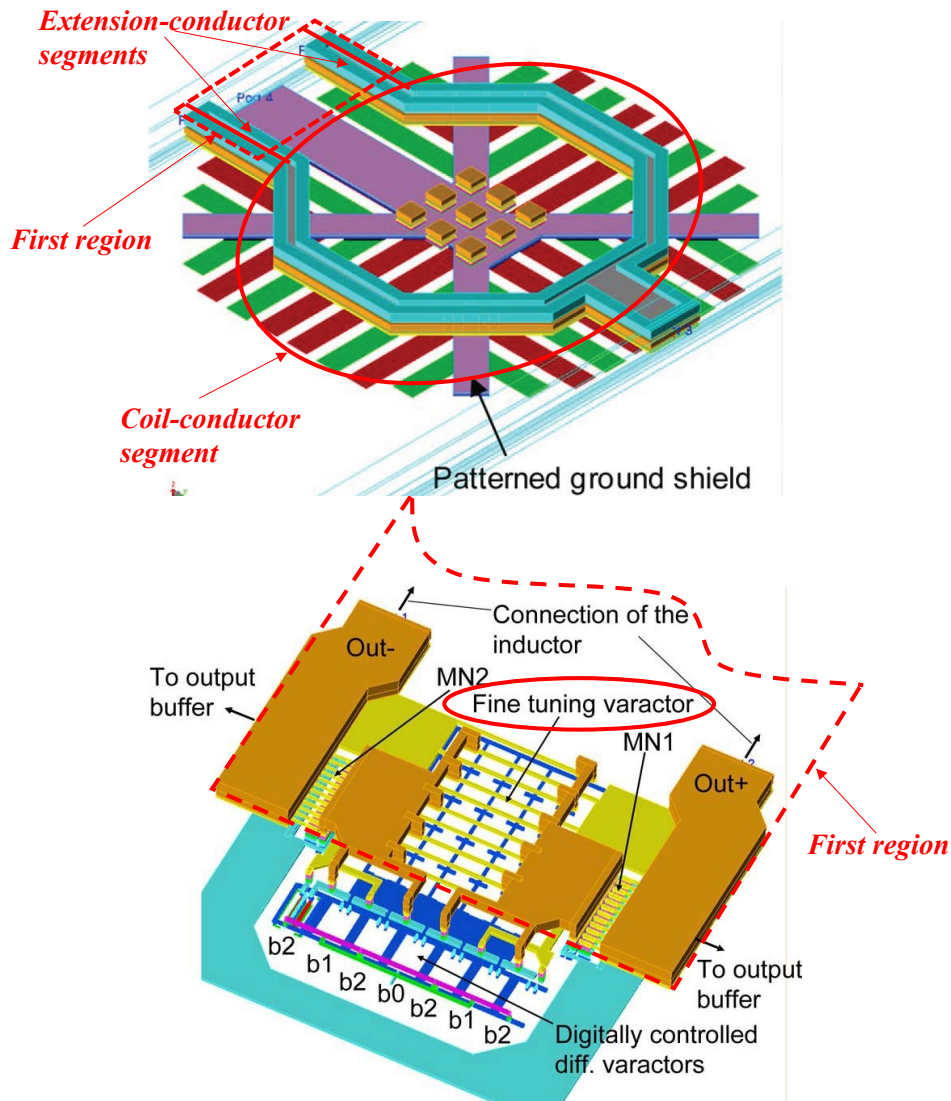
Realtek Exhibit 32 to ITC Complaint (EX-1034) at 12-13 (Realtek annotations retained).

to correspond to the one captured by claim 5, so it does not shed additional light on the scope of “first region” in claim 1. Nonetheless, I am able to apply Gonzalez and other prior art against this claim term for purposes of my obviousness analysis.

1.6a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer,

139. Gonzalez renders this limitation obvious, as Gonzalez discloses everything except for the “embedded manner” part of the limitation. For example, as illustrated in Fig. 8 below, Gonzalez discloses a “fine tuning varactor” (i.e., variable capacitor), which is or includes a capacitor component.

140. Further, each “connection of the inductor” (shown in the bottom half of Fig. 8 on a brown metal layer) is part of an extension-connection segment of the inductor (shown in the top half of Fig. 8 also on a brown metal layer). Based on how Realtek has interpreted the term “first region,” in the bottom half of Fig. 8 (copied below), the first region would extend back to the top half of Fig. 8 which shows the first region as defined by the two extension-conductor segments and the coil-conductor segment. Therefore, Gonzalez’s fine tuning varactor is arranged corresponding to the first region as interpreted by Realtek.



Gonzalez (EX-1005) at Fig. 8 (annotations added in red).

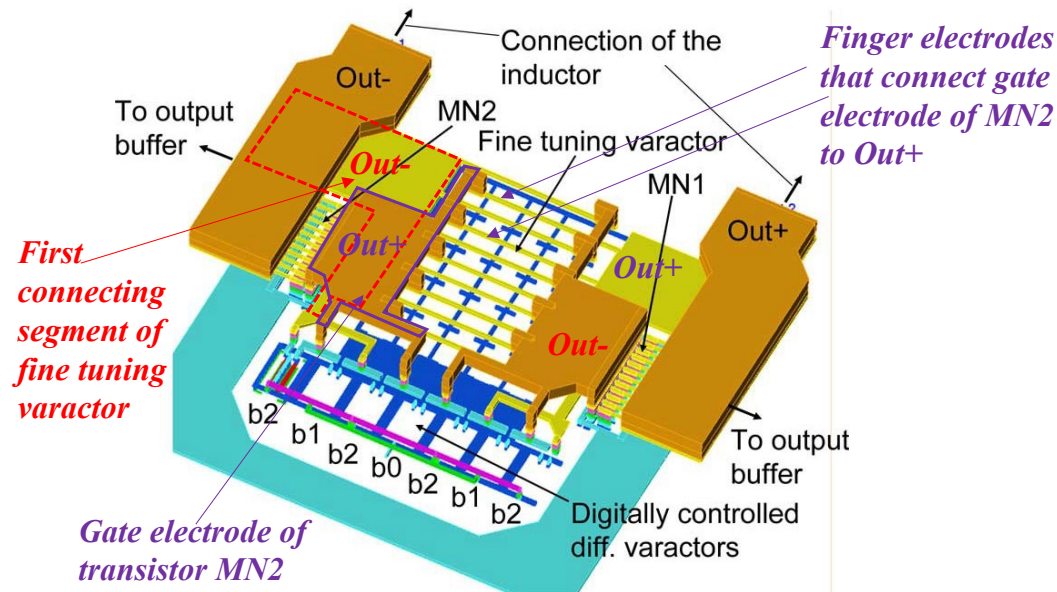
141. In Gonzalez, the fine tuning varactor is “[a] differential N+poly/Nwell varactor operating in accumulation mode [and] is used for continuous tuning” of the VCO. See Gonzalez (EX-1005) at 5; *Id.* at Fig. 2 (illustrating the varactor as a “[c]ontinuous tuning analog control varactor.” The differential varactor “is made with two N+poly/Nwell varactors.” *Id.* at 6. An exemplary structure of the fine tuning differential varactor is illustrated in Gonzalez’s Fig. 5. According to

Gonzalez, “the differential varactor used in our VCO leads to an increased quality factor by reducing the differential current path length through the Nwell and provides a smaller minimum capacitance due to the reduction of the routing interconnections.” *Id.* at 5.

142. To the extent Gonzalez’s Fig. 8 does not expressly disclose a first insulation layer with a surface on which the capacitor component is arranged in an embedded manner opposite to the inductor component, this would have been understandable to a POSITA, as explained above. The purpose of Fig. 8 is to show “[t]he layout of the interconnection between the varactors, the inductor, and the active sections of the VCO core and the buffers.” Gonzalez (EX-1005) at 7. Indeed, showing insulation layers in Fig. 8 would render electronic components on underlying layers invisible and therefore defeat the purpose of Fig. 8.

143. Nevertheless, it would have been obvious to a POSITA to use a first insulation layer between Fig. 8’s brown metal layer (with two extension-conductor segments of the inductor) and yellow metal layer (with the fine tuning varactor). Specifically, the brown metal layer vertically overlaps with the yellow metal layer, as illustrated in the bottom half of Fig. 8, so it would have been obvious to place an insulation layer between them to create electric insulation or separation and ensure proper working of electronic components on these two layers.

144. In this paragraph I give one exemplary reason why it would have been obvious to a POSITA to place an insulation layer between the yellow and brown metal layers, although there are many reasons. As illustrated in Fig. 8, a first connecting segment of the fine tuning capacitor (annotated below in a red box) is connected to one terminal (Out-), while a gate electrode of a transistor MN2 (annotated in a dark purple box) is connected to another terminal (Out+) (from right to left of Fig. 8, through a second connecting segment of the fine tuning varactor and through finger electrodes of the fine tuning capacitor). *See also* Gonzalez (EX-1005) at Fig. 2 (confirming same electric connections); *Id.* at 5 (stating “the dc output voltage of the VCO,” i.e., the voltage difference between terminals Out+ and Out-, “sets the common mode voltage for the differential varactors and the gate-to-source voltage (V_{GS}) for the NMOS transistors.”). Here, the first connecting segment (red box) and the gate electrode of the transistor MN2 (dark purple box) partially overlap. Therefore, an insulation layer here between the metal layers would be necessary to avoid electric shorting between the two terminals (Out+ and Out-).



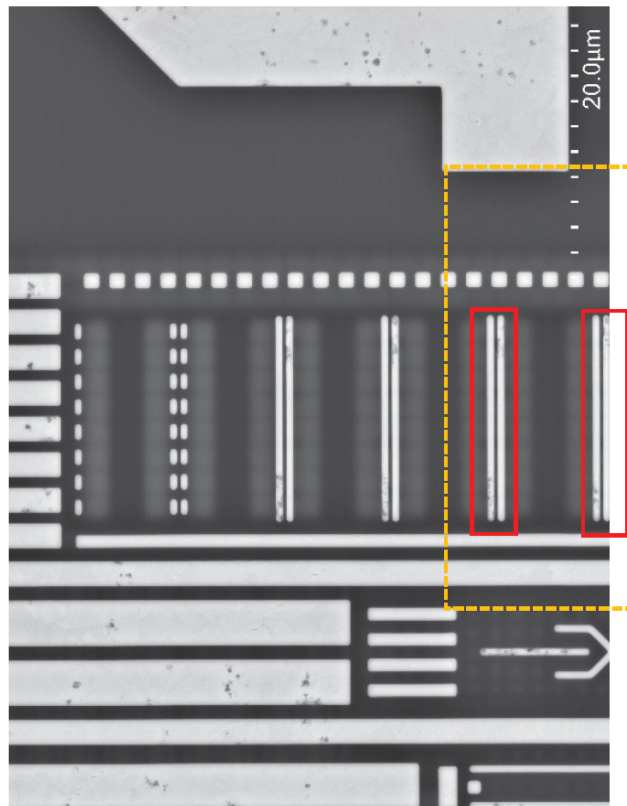
Gonzalez (EX-1005) at Fig. 8 bottom half (annotations added in red and dark purple).

145. Notably, it would have been obvious to a POSITA that cross-layer electric connections, where needed, are easily formed using vias or other vertical interconnect structures. For instance, vias can be used to connect the first connecting segment of the fine tuning varactor to the left extension-conductor segment of the inductor, so that both are connected to the terminal Out-. Indeed, Gonzalez's Fig. 9 illustrates the concept of placing vias between two metal layers (although the vias in Fig. 9 are between Metal 1 and Metal 2 of the ground plane). Gonzalez (EX-1005) at 8.

146. Further, it would have been obvious to a POSITA that Gonzalez's fine tuning varactor would naturally be arranged in an embedded manner on the other surface of the first insulation layer that is opposite to its inductor component.

Embedding electronic elements such as a capacitor component on the surface of an insulation layer was not new. As the '582 Patent acknowledges in its background section, it was well known that, “in order to reduce the volume of an electronic product, various electronic elements [such as capacitor components] are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).” '582 Patent (EX-1001) at 1:29-32; *see also id.* at 8:40-42 (“Here, the structures of various embedded electronic elements are well known to in the field, and therefore are no longer elaborated.”). Gonzalez teaches just that: “Implementation in silicon allows single-chip integration of the millimeter-wave front end, thus enabling a dramatic reduction in size and cost.” Gonzalez (EX-1005) at 4. A POSITA would therefore have understood that Gonzalez does not use surface mount technology, but would instead implement its components in an embedded manner as the '582 Patent admits was known and advantageous. Indeed, Realtek interprets this limitation as allegedly being met by a capacitor that is in a lower metal layer ***adjacent to*** an insulation layer. Realtek Exhibit 32 to ITC Complaint (EX-1034) at 14 (stating that a “capacitor component” is located “in an embedded manner on the other surface (i.e., in the M9 layer ***adjacent to*** the first insulation layer), opposite to the inductor component, of the first insulation layer”). In addition, Realtek maps to a capacitor component located on a same metal layer as the accused inductor component, as illustrated below. *Id.* at 16 (showing a top-

view image of a metal layer on which capacitor connecting segments reside (in red boxes) and on which inductor coil and extension-connection segments reside (at the top of the image)); *id.* at 018 (showing capacitor connecting segments in red boxes being located two layers below a top layer M12 of an inductor (i.e., on the same layer M10 as the bottom layer of the accused inductor)).

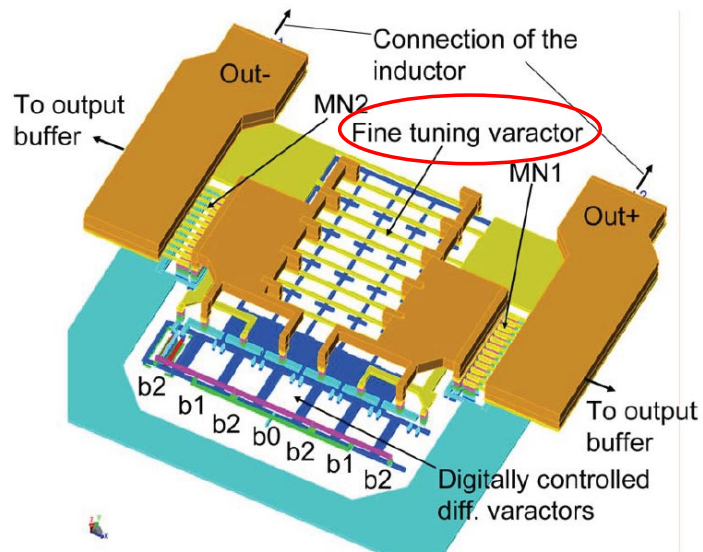
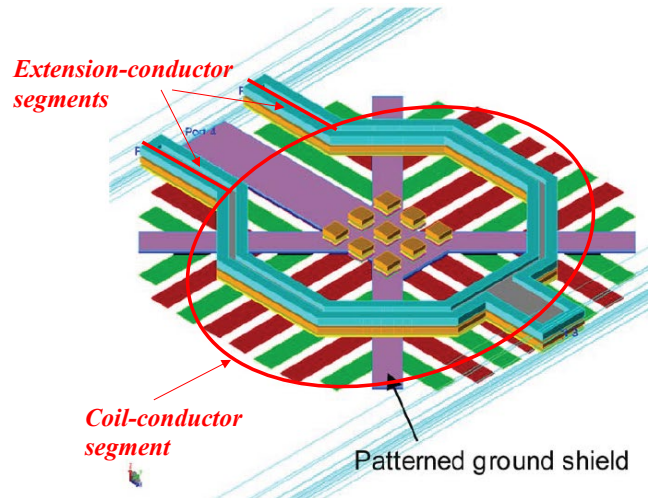


Realtek Exhibit 32 to ITC Complaint (EX-1034) at 16 (Realtek annotations retained).

1.7 wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,

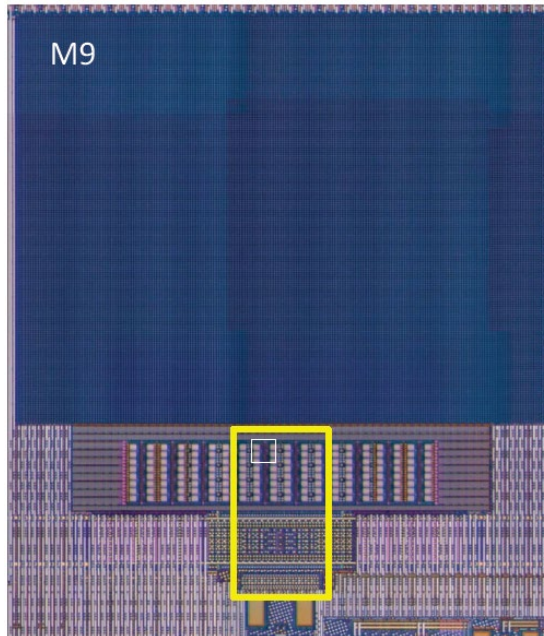
147. Gonzalez discloses this limitation, as Gonzalez's fine tuning varactor (i.e., "the capacitor component") is correspondingly configured outwards relative to the coil-conductor segment of its inductor, and its fine tuning varactor is not substantially overlapped with the coil-conductor segment of its inductor. For example, Gonzalez's Fig. 2 illustrates an inductor and a continuous tuning analog control varactor (i.e., fine tuning varactor), where the varactor is correspondingly configured outwards relative to the coil-conductor segment of the inductor and is not substantially overlapped with the coil-conductor segment of the inductor.

148. Similarly, Fig. 8 also shows a fine tuning varactor located under and between the "connection[s] of the inductor," which are part of the extension segments of the inductor. Here, the fine tuning varactor is correspondingly configured outwards relative to the coil-conductor segment of the inductor, and is not substantially overlapped with the coil-conductor segment of the inductor.



Gonzalez (EX-1005) at Fig. 8 (annotations added in red).

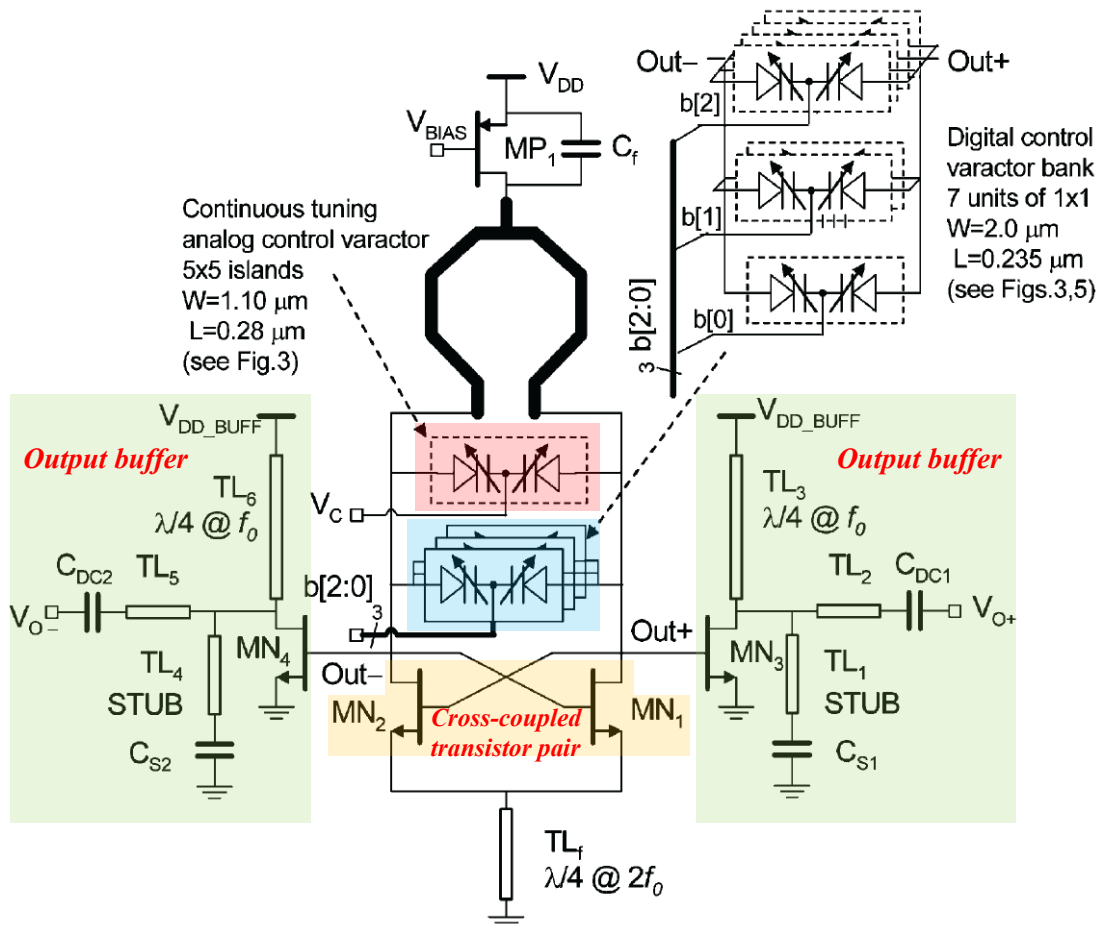
149. This interpretation is consistent with how Realtek interprets this limitation, as shown below.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 14 (Realtek annotations retained); *Id.* (“A capacitor component (e.g. within the white box), arranged corresponding to the first region (yellow block) in an embedded manner on the other surface (i.e., in the M9 layer adjacent to the first insulation layer), opposite to the inductor component, of the first insulation layer. As show in the image above, the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.”)

150. Notably, Gonzalez’s “oscillator core is composed of an NMOS cross-coupled pair (MN1, MN2) and an LC tank” which in turn includes an inductor, an analog control varactor, and a digital control varactor bank. Gonzalez (EX-1005) at 4-5. The oscillator or VCO core is also coupled to two output buffers. Gonzalez (EX-1005) at Fig. 2, Fig. 12. Specifically, Fig. 2 (copied below with annotations) illustrates spatial relationships and electrical connections among VCO core components—including an inductor, an analog control varactor (annotated in red shade), a digital control varactor bank (annotated in blue shade), an NMOS cross-

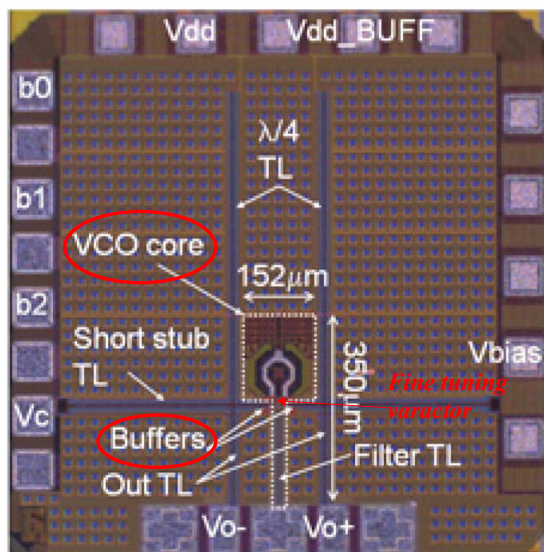
coupled transistor pair (annotated in yellow)—as well as two output buffers (annotated in green).



Gonzalez (EX-1005) at Fig. 2 (annotations added in colors).

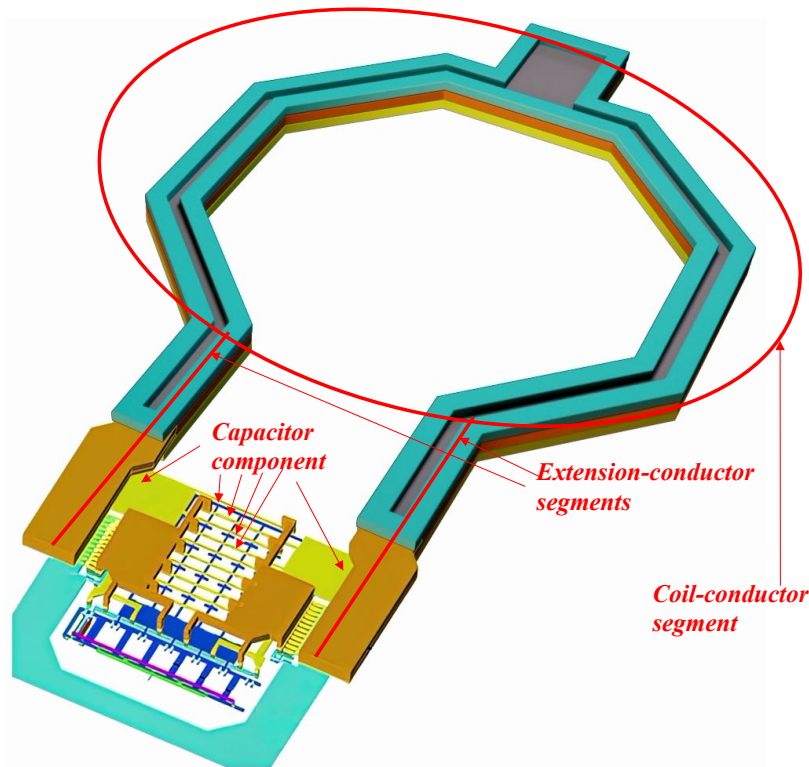
151. Gonzalez's Fig. 12, a top-view micrograph of the VCO die, also illustrates the same spatial arrangement in the VCO core as in Fig. 2. Although the analog control varactor (i.e., fine tuning varactor) is not labeled in Fig. 12, a POSTITA would have understood, in view of other discloses in Gonzalez (e.g., Fig. 2 and Fig. 8), the analog control varactor (as part of the VCO core) would be

placed under the extension segments of the inductor and generally between the two output buffers, as illustrated below.



Gonzalez (EX-1005) at Fig. 12 (annotations added in red).

152. Consistent with Fig. 2 and Fig. 12, Gonzalez’s Fig. 8 shows how its fine tuning varactor is arranged relative to the “connection of the inductor” and to two “output buffers.” Although Fig. 8 does not expressly show all components of the VCO core in a combined view, based on Gonzalez’s disclosures, a POSITA would have been able to readily generate such a combined view. For ease of viewing, an exemplary combination of the upper and bottom halves of Fig. 8 is depicted below. As is clear from the combined view of Fig. 8, Gonzalez’s capacitor component (the fine tuning varactor) is correspondingly configured outwards relative to the coil-conductor segment, and is not substantially overlapped with the coil-conductor segment.



Gonzalez (EX-1005) at Fig. 8 (regenerated by removing the patterned ground shield from the top half of Fig. 8, rotating the inductor into alignment with the bottom half of Fig. 8, and removing texts for ease of viewing).

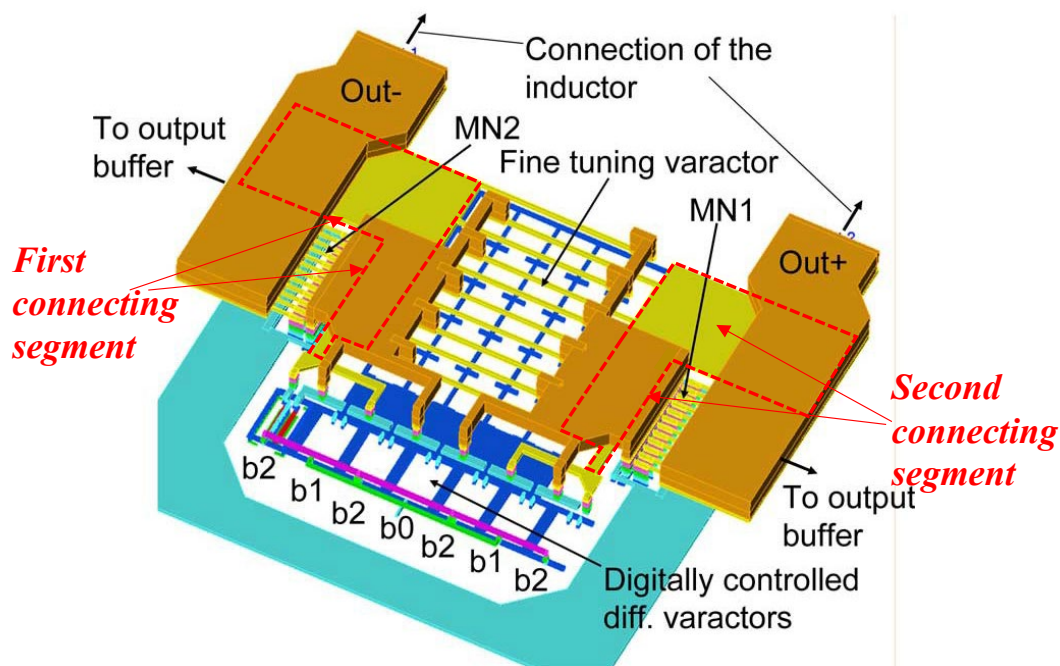
153. The VCO core design as disclosed by Gonzalez has various benefits. For example, as shown in Fig. 8, “[t]he layout of the interconnection between the varactors, the inductor, and the active sections of the VCO core and the buffers is *optimized to reduce parasitic capacitance and inductance.*” Gonzalez (EX-1005) at 7 (emphasis added).

154. As I discussed in the background of technology section, the spatial relationship between the inductor and fine tuning varactor as disclosed by Gonzalez—where the fine tuning varactor is configured outwards relative to the coil-conductor segment of the inductor and is not substantially overlapped with the

coil-conductor segment of the inductor—was well known before the time of the ‘582 filing. A POSITA would have understood similar layouts were extremely common in VCO circuits. *See supra* ¶ 88.

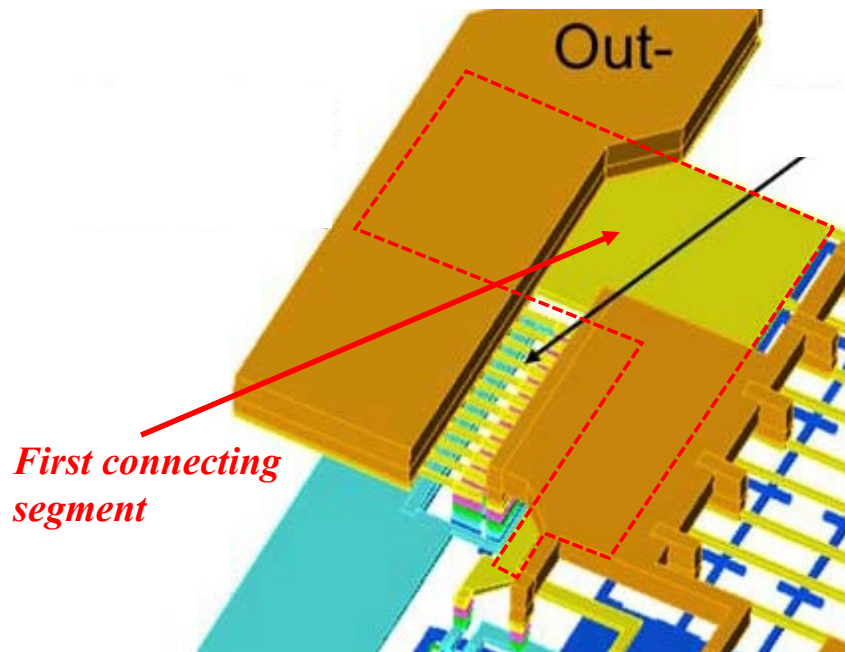
1.8 wherein the capacitor component comprises: a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

155. Gonzalez discloses this limitation. For example, as illustrated in the bottom half of Fig. 8, Gonzalez’s fine tuning varactor includes at least two (first and second) connecting segments on a metal layer shown in yellow color.



Gonzalez (EX-1005) at Fig. 8 bottom half (annotations added in red).

156. For clarity, another zoomed-in partial view of Fig. 8 is reproduced below illustrating the first connecting segment of the fine tuning varactor.



Gonzalez (EX-1005) at Fig. 8 bottom half partial view (annotations added in red).

Although Gonzalez's Fig. 8 does not show the full structure of the first connecting segment, as it is partially hidden from view, a POSITA would have recognized the above to be a reasonable interpretation of its shape and position. For instance, according to Gonzalez, the first connecting segment is connected to a connection of the inductor (Out-) and is connected to five of ten thin fingers in the fine tuning varactor, which is made of 5x5 basic cells. Gonzalez (EX-1005) at Fig. 2 ("Continuous tuning analog control varactor 5x5 islands"), Fig. 5 lower half ("fine

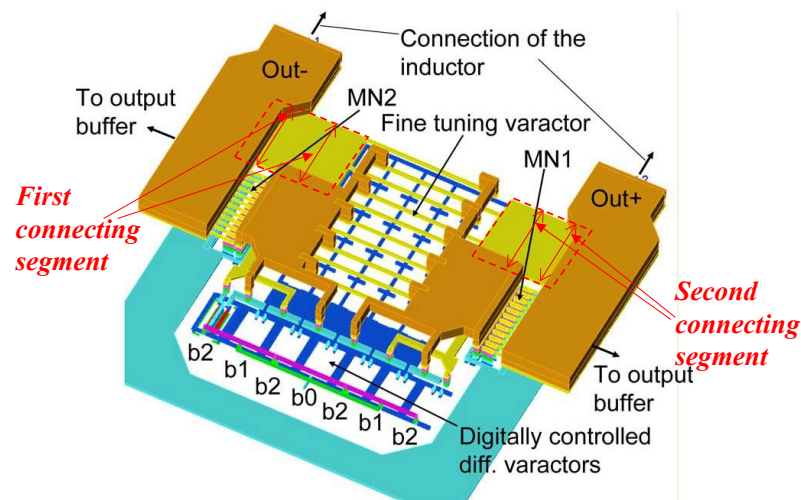
tuning varactor: 5x5 islands”), 6 (“Larger values are obtained using an array of $n \times m$ basic cells”).

157. The connecting segments of Gonzalez’s fine tuning varactor extend corresponding to the two extension-conductor segments (e.g., “connection of the inductor”) in a same direction. Further, the connecting segments of Gonzalez’s fine tuning varactor are respectively overlapped (at least partially) with the two extension-conductor segments in a vertical direction.

158. In Gonzalez, the first and second connecting segments are used for receiving or transmitting a signal. For example, through these connecting segments, “N+poly gates are each connected to one of the two differential terminals (Out+, Out-).” Gonzalez (EX-1005) at 6. And the differential terminals (Out+, Out-) provide output voltage signals of the VCO core. *Id.*

159. In the annotated Fig. 8 above, the first and second connecting segments of Gonzalez’s fine tuning varactor are marked by red dash lines, even though parts of the connecting segments are hidden from view. The dash lines provide one reasonable interpretation of the connecting segments based on Gonzalez’s disclosures. A POSITA would appreciate that the connecting segments can be flexibly interpreted and their shape and/or size are not limited to the dash lines shown above. For instance, the fine tuning varactor can include connecting segments that each have a rectangular or square shape (as illustrated in Fig. 8

below as each connected to two of the ten thin fingers in the fine tuning varactor), or part thereof, that still (1) extends corresponding to an extension-conductor segment in a same direction and (2) overlaps at least partially with an extension-conductor segment in a vertical direction. That is, such connecting segments would still meet the claimed connecting segments in the claimed “capacitor component.”



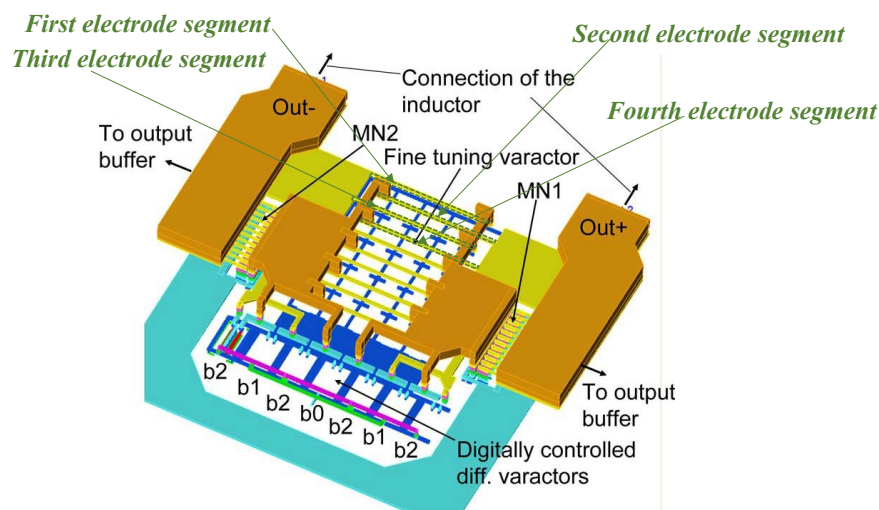
Gonzalez (EX-1005) at Fig. 8 bottom half (annotations added in red).

160. The claimed structure of the capacitor component was not new. Indeed, the '582 Patent acknowledges that the internal structures of its claimed capacitor component were “well known in the field.” '582 Patent (EX-1001) at 12:11-16.

1.9 a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode

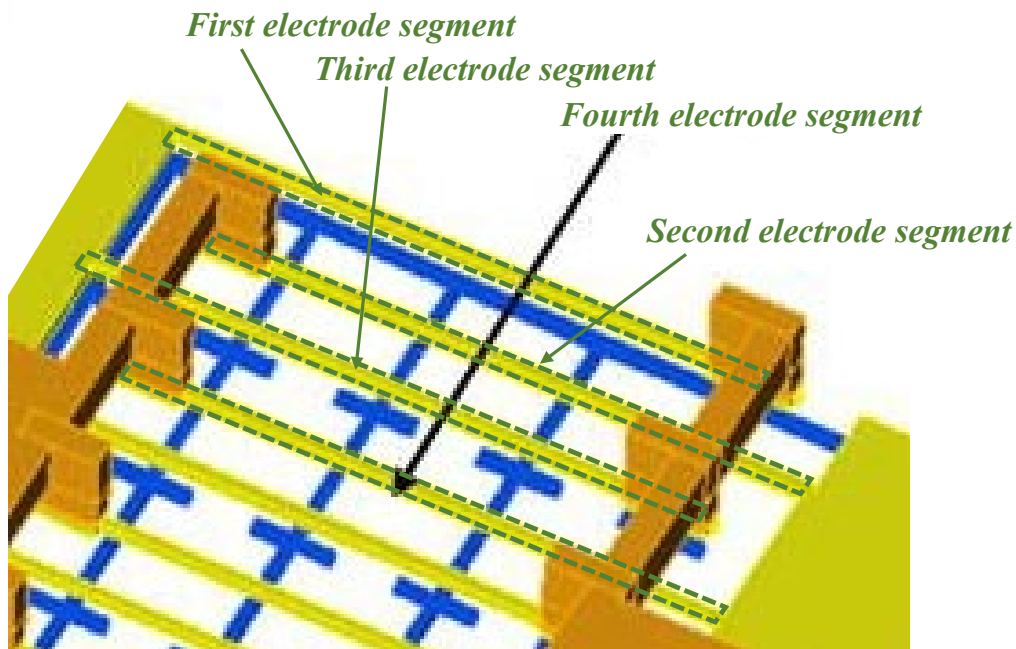
segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

161. Gonzalez discloses this limitation. For example, Gonzalez's fine tuning varactor includes a plurality of finger-shaped, interdigitated electrode segments on a metal layer shown in yellow color. Four (first, second, third, and fourth) such finger-shaped electrode segments are annotated in Fig. 8 below since they are fully visible. Notably, since the fine tuning varactor includes "5x5 islands" of differential varactor units, it can include all ten finger-shaped electrode segments shown in Fig. 8, although some electrode segments are partially hidden from view. Gonzalez (EX-1005) at Fig. 2, Fig. 3.



Gonzalez (EX-1005) at Fig. 8 bottom half (annotations added in dark green).

162. For clarity, another zoomed-in partial view of Fig. 8 is reproduced below illustrating the first, second, third, and fourth electrode segments of the fine tuning varactor:

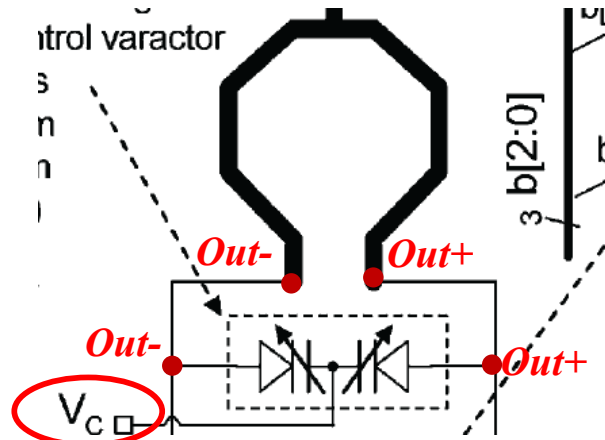


Gonzalez (EX-1005) at Fig. 8 bottom half partial view (annotations added in dark green).

163. In Gonzalez, the finger-shaped, interdigitated electrode segments serve as electrode plates in the fine tuning varactor. As a first example, as shown in Fig. 8, one set of finger-shaped electrode segments (e.g., first and third) is connected to terminal Out-, while the other set of finger-shaped electrode segments (e.g., second and fourth) is connected to terminal Out+. *See also* Gonzalez at Fig. 2 (reproduced below, showing two ends of the fine tuning varactor are connected to Out- and Out+, respectively). The first and second sets of electrode segments are separated by a gap. Therefore, a voltage difference (i.e., Out+ and Out-) between the first and second sets of electrode segments (e.g., between the first and second, or second and third, or third and fourth electrode segments) would cause a build-up

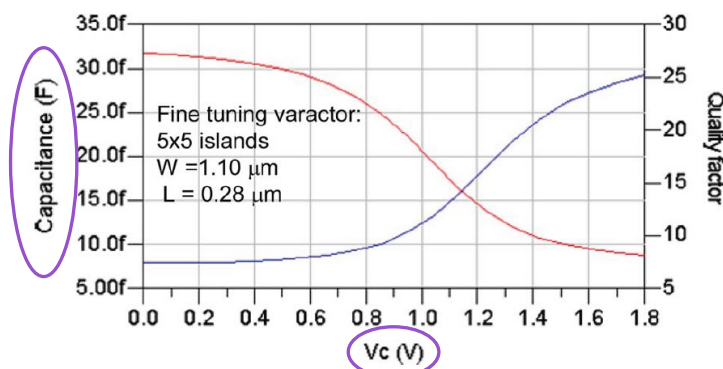
of charge (Q) on the electrodes according to the capacitance between them.

($Q=CV$). *Id.*



Gonzalez (EX-1005) at Fig. 2 partial view (annotations added in red).

164. As a second example, the finger-shaped electrode segments also serve as gate electrode plates that facilitate tuning of the varactor. Gonzalez discloses the capacitance of its fine tuning varactor is tunable via an analog input, e.g., “a common voltage (V_c).” See Gonzalez (EX-1005) at Fig. 2, 5. As illustrated by the red curve in Gonzalez’s Fig. 5 (reproduced below), the capacitance of the fine tuning varactor is tunable by changing common voltage V_c .



Gonzales, Fig. 5 bottom half (annotations added in purple).

165. Specifically, Gonzalez’s fine tuning varactor has a “differential varactor structure” that “is made with two N+poly/Nwell varactors.” Gonzalez (EX-1005) at 6. These are MOS varactors, which are variable capacitors that utilize MOS transistor structures. The ’582 Patent itself discloses MOS capacitors (e.g., capacitor component 150’ in its Fig. 12) and acknowledges that the structures of MOS capacitors were “well known in the field.” ’582 Patent (EX-1001) at 12:11-16. As shown in the ’582 Patent’s Fig. 12 (a partial view reproduced below), the capacitor component 150’—which is a “MOS capacitor”—includes finger-shaped electrode segments 155, 156, 157, 158, just like Gonzalez’s finger-shaped electrode segments. ’582 Patent (EX-1001) at 12:16-23.

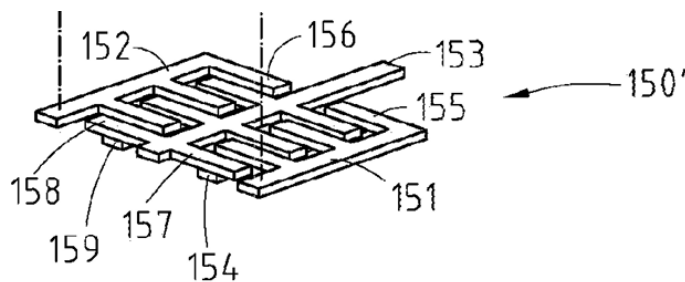
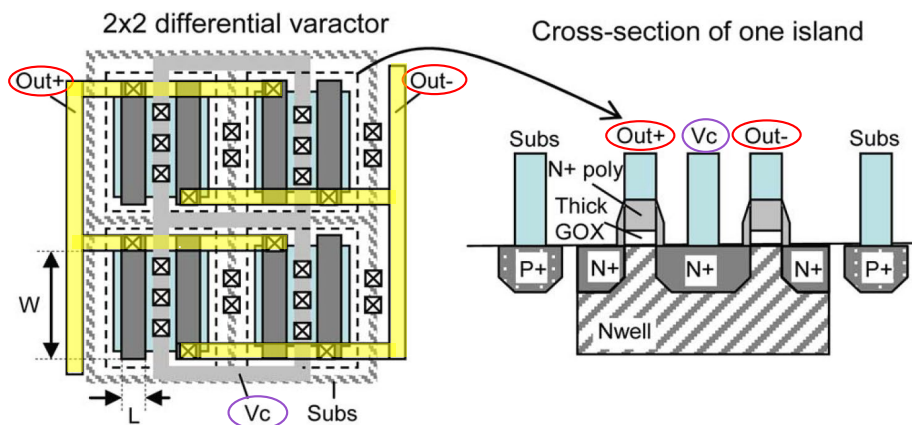


FIG. 12

Id. at Fig. 12 partial view.

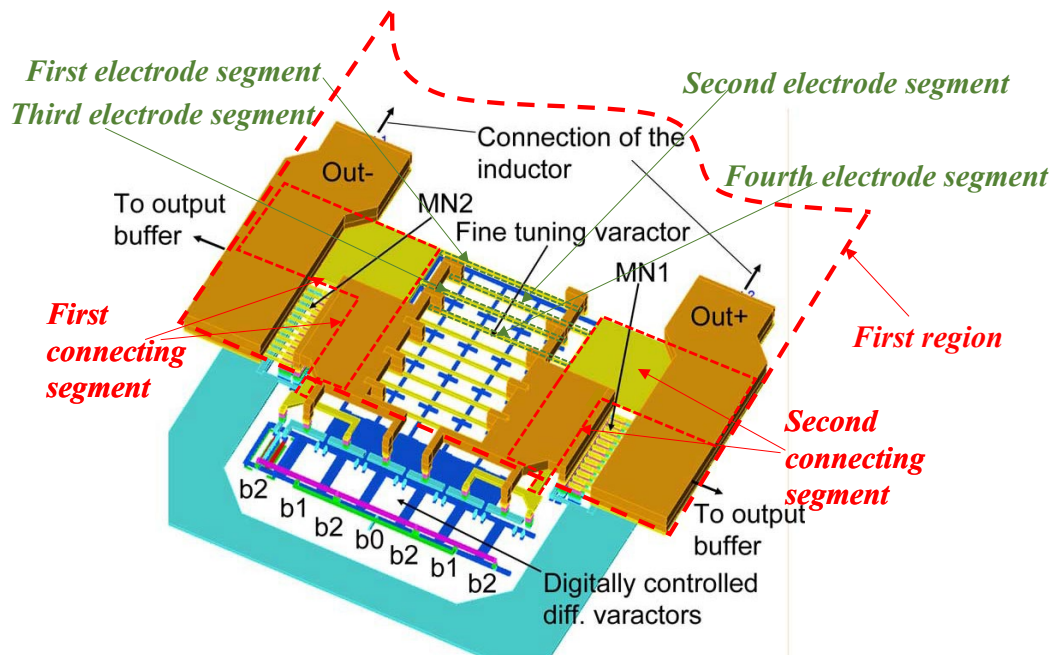
166. As a POSITA would have understood, Gonzalez’s plurality of finger-shaped electrode segments serve as gate electrodes (or parts thereof) of the tunable varactor. For instance, as illustrated by Fig. 5 (top half reproduced below), the capacitance of each MOS varactor is controlled by a voltage difference between its

source (where the common voltage V_c is applied) and its gate (where a voltage Out_- or Out_+ is applied by the finger-shaped electrode segments on the N+poly) across a gate oxide (GOX). As a result, the differential varactor pair's overall capacitance is controlled by differences between the common voltage V_c and the two voltages (Out_- or Out_+) applied by the finger-shaped electrode segments, respectively. This is why Gonzalez's fine tuning varactor has a capacitance that varies with the common voltage V_c .



Gonzalez (EX-1005) at Fig. 5 top half (annotations added to show finger-shaped electrode segments and connecting segments in yellow shade, terminal voltages Out_+ and Out_- circled by red boxes, and common voltage V_c circled by purple boxes).

167. As explained above (*supra* para. 140) and illustrated below, based on how Realtek interprets the term “first region,” Gonzalez’s electrode segments are located below the first region.

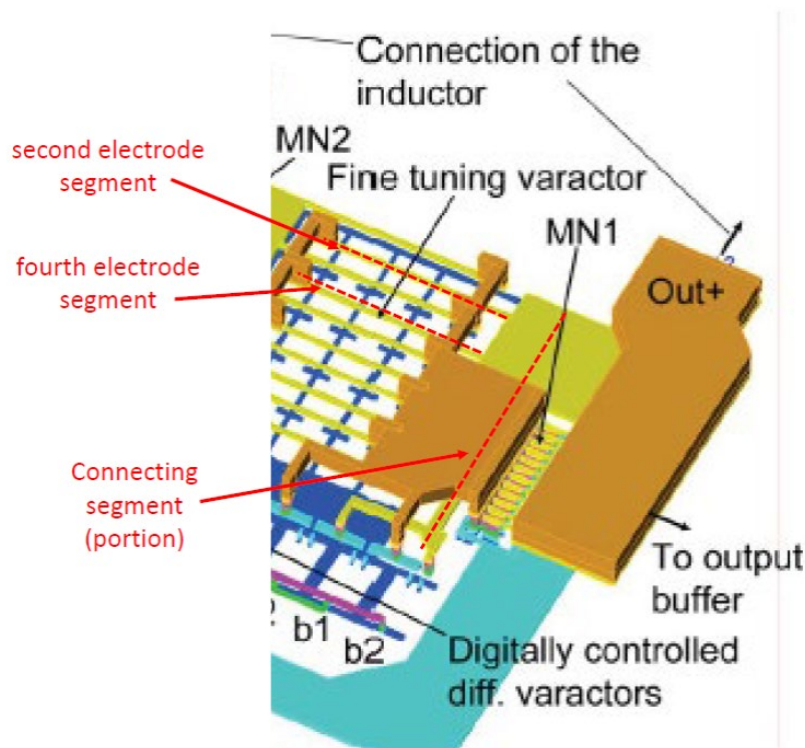


Gonzalez (EX-1005) at Fig. 8 bottom half (annotations added in red and dark green).

168. In Gonzalez's fine tuning varactor, one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments. For instance, as illustrated in Fig. 8 above, the first and third electrode segments are each coupled to the first connecting segment, while the second and fourth electrode segments are each coupled to the second connecting segment.

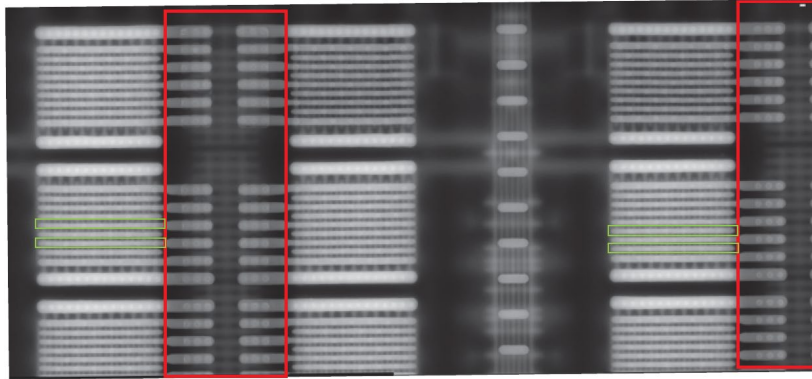
169. Further, in Gonzalez's fine tuning varactor, each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments. For instance, as illustrated in Fig. 8 above, the first and third electrode segments each extend laterally relative to the first connecting segment, while the second and fourth electrode segments each extend laterally relative to the second connecting segment. This is further

illustrated in Fig. 8 below, where the electrode segments (e.g., second and fourth, indicated by red dashed lines) extend laterally relative to the respective coupled connecting segment (indicated by another red dashed line) of the plurality of connecting segments. *See also Gonzalez (EX-1005) at Fig. 5 top-left portion (showing each finger electrode segment extends laterally relative to its coupled connecting segment).*



Gonzalez (EX-1005) at Fig. 8 bottom half partial view (annotations added in red).

170. Gonzalez's disclosures are consistent with how Realtek interprets this limitation, as shown below, where Realtek marks the plurality of electrode segments in green boxes and the plurality of connecting segments in red boxes.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 18 (Realtek annotations retained).

171. Gonzalez’s disclosures are also consistent with the ’582 Patent itself. For example, The ’582 Patent discloses MOS capacitors (e.g., capacitor component 150’ in its Fig. 12) and acknowledges that the structure of MOS capacitors were “well known in the field.” ’582 Patent (EX-1001) at 12:11-16.

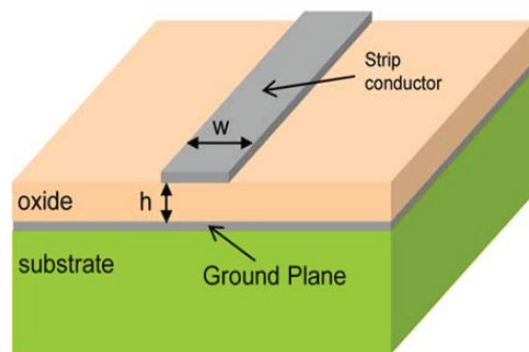
172. To sum up, as I explained above, Gonzalez renders claim 1 obvious. Specifically, Gonzalez explicitly discloses the limitations of claim 1. To the extent certain features are not expressly shown in Gonzalez’s figures, as I explained above, such features would be obvious to a POSITA in view of Gonzalez.

C. Gonzalez Invalidates Claims 2-5 and 9

Claim 2

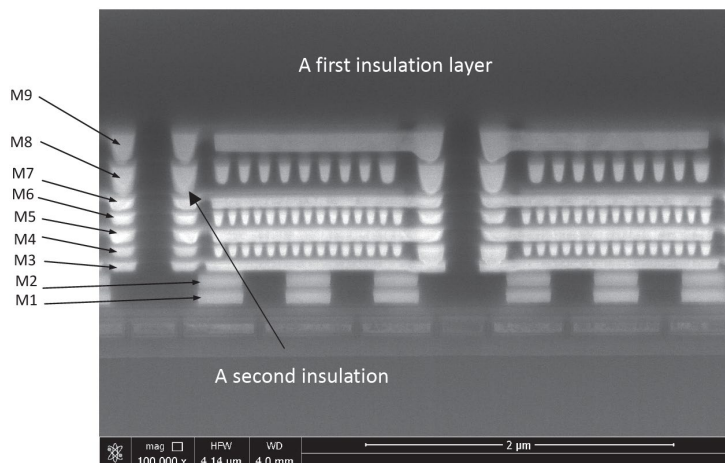
2.1 The semiconductor device with an LC resonant circuit according to claim 1, further comprising: a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

173. Gonzalez discloses this limitation or renders it obvious. For example, Gonzalez discloses “a dielectric” material, shown as an “oxide” in Fig. 9 (copied below). Gonzalez (EX-1005) at 7-8. This dielectric is located between a “top metal level (M6)” and “two bottom metal layers (M1+M2).” *Id.* at 8. A dielectric (e.g., an oxide) is an insulation material that can form one or more insulation layers. Therefore, a POSITA would have understood that part of Gonzalez’s dielectric material forms a second insulation layer.



Id. at Fig. 9.

174. This interpretation is consistent with how Realtek interprets the second insulation layer, as shown below.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 19 (Realtek annotations retained).

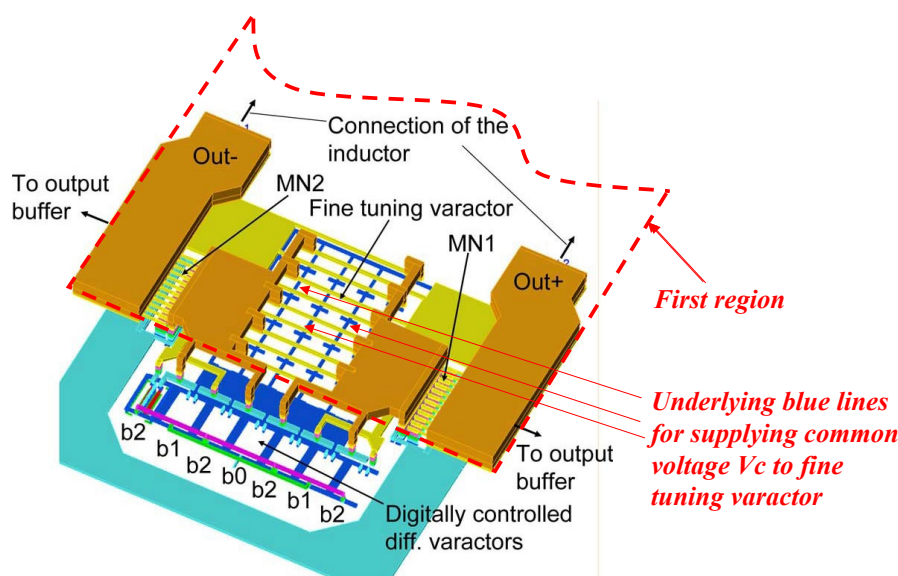
175. To the extent the second insulation layer is not expressly shown in Fig. 8 (which makes sense as the purpose of Fig. 8 is to show “[t]he layout of the interconnection between the varactors, the inductor, and the active sections of the VCO core and the buffers”), it would have been obvious to a POSITA to use a second insulation layer such that the capacitor component is sandwiched between the first insulation layer and the second insulation layer.

176. For example, as shown in Gonzalez’s Fig. 8, in addition to a metal layer (in yellow) which includes connecting segments and electrode segments of the fine tuning capacitor, Gonzalez also discloses an underlying metal layer (in blue) with capacitor components. A common voltage V_c can be applied onto the blue metal layer to tune a capacitance of the fine tuning varactor. *See* Gonzalez (EX-1005) at Fig. 5, Fig. 8; *see also Id.* at 6-7 (“The V_c signal of the varactor is directly connected to a digital signal that switches the varactor ON or OFF by applying 0 or 1.8V to the gate of the N poly/Nwell differential varactor.”). Since different voltages are applied to the overlapping blue and yellow metal layers, it would have been obvious to a POSITA to use a second insulation layer between the yellow and blue metal layers to avoid electric shorting (e.g., between V_c and Out₋, or between V_c and Out₊).

177. This paragraph describes additional reasons why it would have been obvious to have the second insulation layer between the yellow and blue metal layers. As illustrated in the bottom half of Fig. 8, part of the blue metal layer also hosts “[a]n additional bank of digitally controlled differential varactors [that] provides coarse tuning for PVT calibration using three bits (b_2, b_1 , and b_0).” Gonzalez (EX-1005) at 5. Gonzalez also discloses that its “discrete tuning in the VCO is implemented using a binary-scaled set of varactors composed of one, two, and four units controlled by b_0 , b_1 , and b_3 bits, respectively. The digitally controlled differential varactor unit cell has an ON/OFF capacitance and quality factor of 1.98 fF/0.54 fF and 4.5/16.5, respectively, at 60 GHz.” *Id.* at 7. Since Gonzalez discloses using both (1) a yellow metal layer as part of a fine tuning varactor and (2) part of an underlying blue metal layer being a coarse tuning varactor bank, it would have been obvious to a POSITA to use a second insulation layer between the yellow and blue metal layers to avoid electric shorting between them. as yet another benefit, the second insulation layer would help avoid electrical shorting between the fine tuning varactor and the coarse tuning varactor.

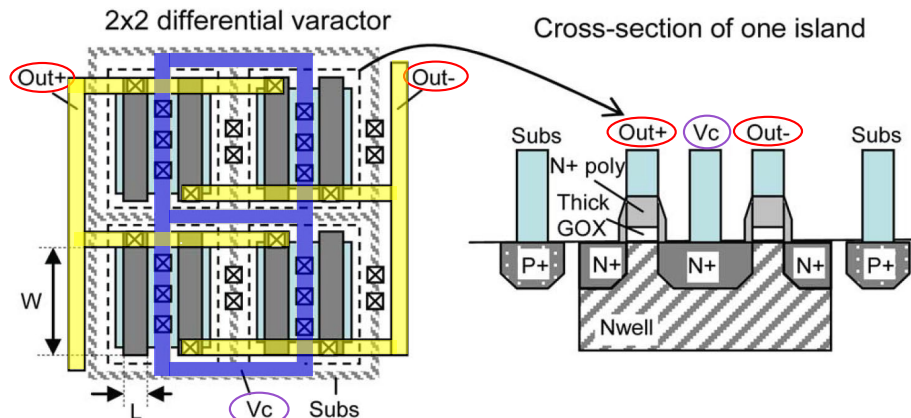
2.2 an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

178. Gonzalez renders this limitation obvious, as Gonzalez discloses everything except for the “embedded manner” part of the limitation. For example, as shown in Fig. 8, a blue metal layer (lying under the yellow metal layer) contains an electronic component on which a common voltage V_c can be applied to tune a capacitance of the fine tuning varactor. *See* Gonzalez (EX-1005) at 6-7. Also, Gonzalez discloses a bank of “digitally controlled differential varactors,” which also includes electronic components implemented on the blue metal layer.



Gonzalez (EX-1005) at Fig. 8 bottom half (annotations added in red).

179. Fig. 5, which shows a differential varactor made of four (2x2) varactor units, also illustrates the common voltage V_c being applied onto an underlying metal layer (annotated in dark blue below to imitate coloring in Fig. 8). Fig. 5 additionally shows non-metal structures, which are omitted from Fig. 8.



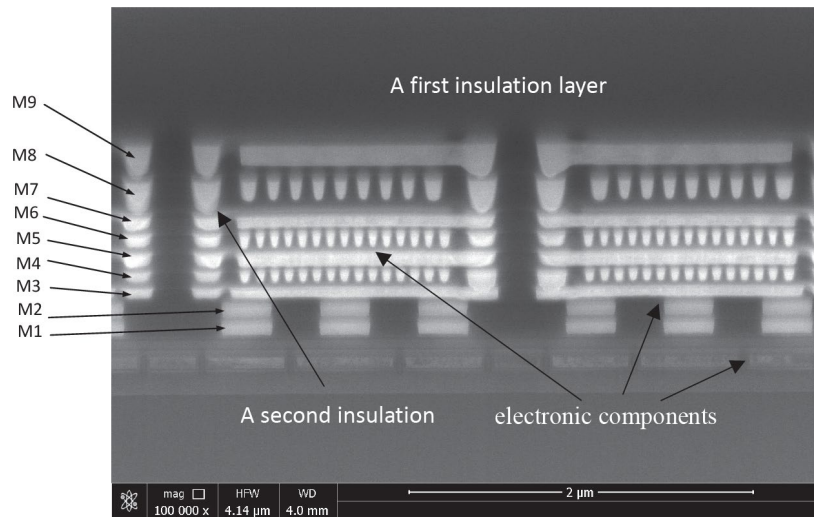
Gonzalez (EX-1005) at Fig. 5 top half (annotations added in yellow, red, dark blue, and purple).

180. Based on how Realtek interprets the term “first region,” Gonzalez discloses at least one electronic component on the blue metal layer arranged corresponding to the first region on a surface, opposite to the capacitor component, of the second insulation layer. For instance, Gonzalez discloses electronic components on the blue metal layer that are located directly under a yellow metal layer of the fine tuning varactor, as shown in the bottom half of Fig. 8.

181. Further, it would have been obvious to a POSITA that Gonzalez’s electronic component on the blue metal layer would be arranged in an embedded manner on the other surface of the second insulation layer that is opposite to its fine tuning varactor. As I explained with reference to claim 1, embedding electronic components on the surface of an insulation layer was not new. As the ’582 Patent acknowledges in its background section, it was well known that, “in order to reduce the volume of an electronic product, various electronic elements

are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).” ’582 Patent (EX-1001) at 1:29-32.

182. This is also how Realtek interprets the claim language, as depicted below.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 19 (Realtek annotations retained).

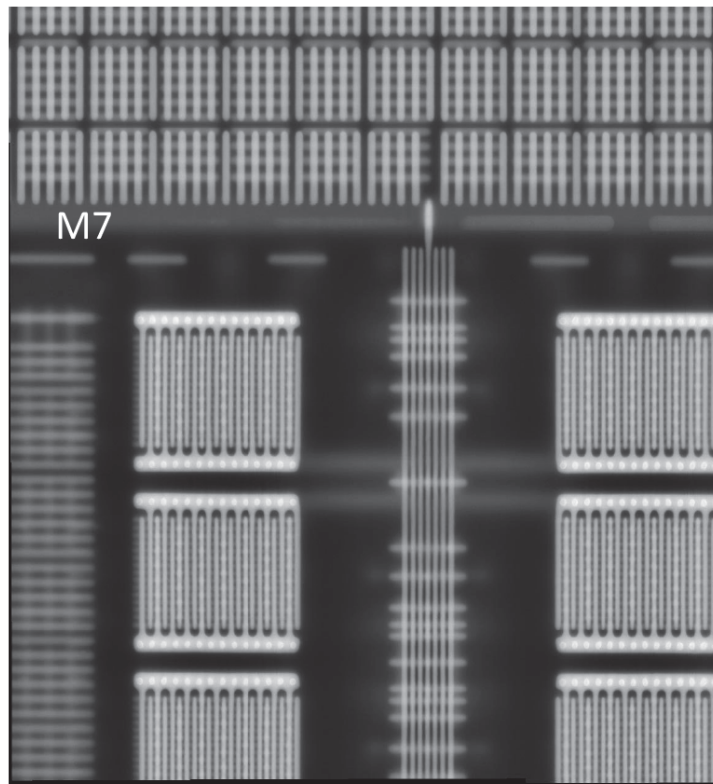
Claim 3

The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

183. Gonzalez discloses this claim. For example, as shown in Fig. 8, a common voltage V_c can be applied on the blue metal layer to tune a capacitance of the fine tuning varactor. *See* Gonzalez (EX-1005) at 6-7. Also, Gonzalez discloses a bank of “digitally controlled differential varactors,” which also includes electronic components implemented on the blue metal layer. Therefore, the electronic

components implemented on the blue metal layer includes at least another capacitor component.

184. This is also how Realtek interprets the claim language, as depicted in the text and accompanying image below.



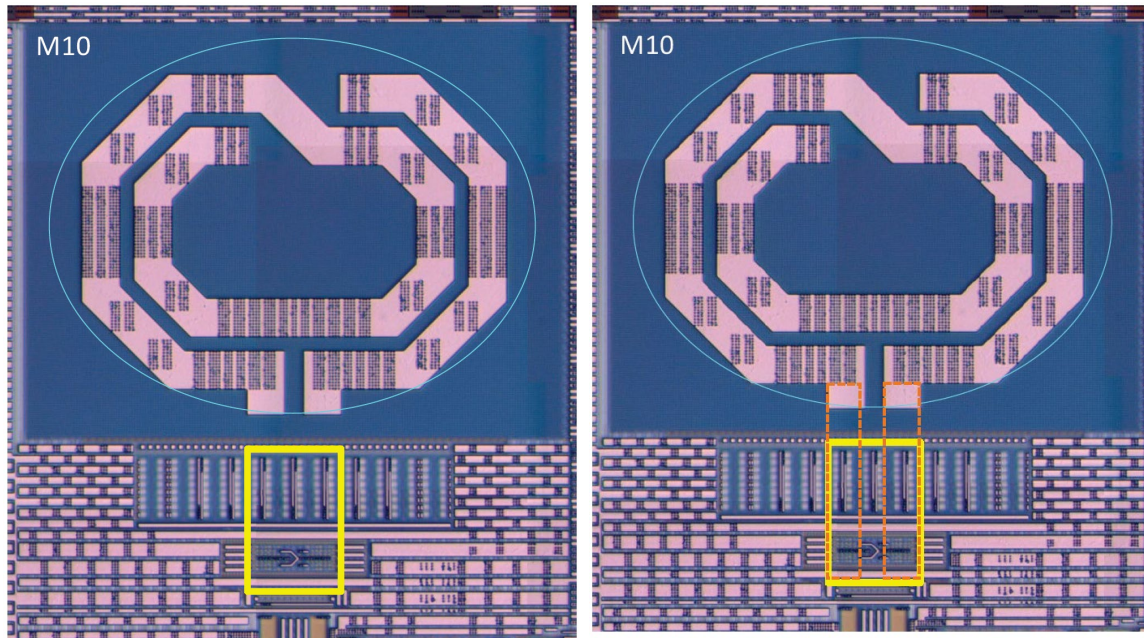
(Depicting a capacitor)

Realtek Exhibit 32 to ITC Complaint (EX-1034) at 20 (Realtek annotations retained).

Claim 4

The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

185. Notably, Realtek interprets the first region of claim 4 as having the same scope as the first region of claim 1, as shown below.



Realtek Exhibit 32 (EX-1034) at 12 (left); *Id.* at 21 (right) (Realtek annotations retained).

186. Gonzalez discloses this claim. For example, since Realtek interprets the first region of claim 4 as having the same scope as the first region of claim 1, Gonzalez discloses claim 4 to the same extent it discloses claim 1.

Claim 5

The semiconductor device with an LC resonant circuit according to claim 4, wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment.

187. The only difference between claim 5 and claim 4 is that claim 5 recites an additional limitation: “the first region is defined between the coil-conductor segment.”

188. Gonzalez discloses this claim. That is, to the extent the first region is defined between the two extension-conductor segments and the coil-conductor segment, the inductor and capacitor components disclosed by Gonzalez still meet such a definition of “the first region.” For example, Gonzalez’s fine tuning capacitor, which is or includes a capacitor component, would still be arranged corresponding to the first region, and a plurality of electrode segments in the fine tuning capacitor would still be located below the first region. *See supra* ¶¶ 139-146, 167.

Claim 9

A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality

of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

189. Based on my review, independent claim 9 is the same as claim 1 except that it is broader as it does not have the following limitation of claim 1: “wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.”

190. Therefore, for at least the reasons provided above for claim 1, Gonzalez renders claim 9 obvious.

VII. GROUND 2: CLAIMS 1-5 AND 9 OF THE '582 PATENT ARE OBVIOUS UNDER 35 U.S.C. § 103 OVER MUH IN VIEW OF NIKNEJAD

191. Muh discloses an LC resonant circuit as part of a VCO. The shape and geometry of the inductor and capacitor components disclosed in Muh are materially the same as the LC resonant circuit claimed in the '582 Patent.

A. Muh Introduction

192. Muh is a 2005 Master of Science thesis entitled “Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO,” authored by Matthew Muh, and submitted to the Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley. Notably, as indicated on the face of Muh, Matthew Muh’s Research Advisor was Professor Ali M. Niknejad, author of mm-Wave Silicon Technology 60 GHz and Beyond

(“Niknejad”). EX1006 at 1. The Muh thesis predates the earliest application in the ’582 priority chain by approximately a decade.

193. Muh discloses a VCO that contains an LC resonant circuit as shown below:

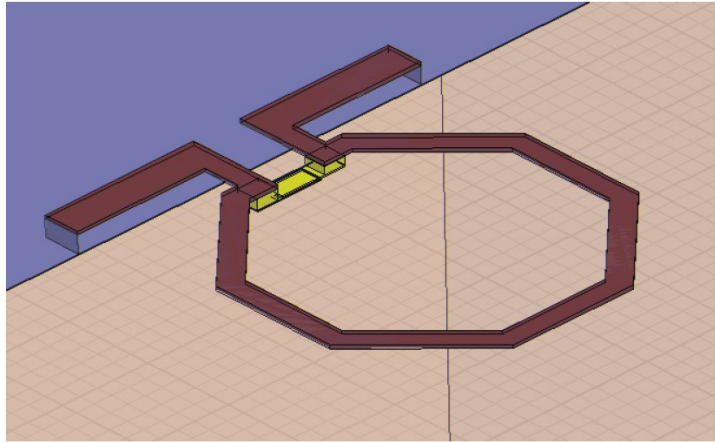


Figure B-3. HFSS model of parallel resonant tank on test chip.

Muh (EX-1006) at 58, Fig. B-3.

194. Muh further elaborates that the LC resonant circuit includes an “inductor in parallel with a capacitor” and that in an actual test chip, an “interdigitated finger capacitor is included” as shown below.

The second structure simulated in HFSS is a resonant tank consisting of the same inductor in parallel with a capacitor. In the test chip, the capacitor is implemented as an interdigitated finger capacitor, with each finger comprising the bottom five metal layers strapped together.

Muh (EX-1006) at 57.

B. Niknejad Introduction

195. Matthew Muh’s research advisor, on the Muh thesis I just discussed, was Berkeley Professor Ali Niknejad. Dr. Niknejad has authored several books in the field of semiconductor circuit design, including the book, “mm-Wave Silicon Technology 60 GHz and Beyond” (Niknejad”), in or around 2008. EX-1007 at 4. Niknejad predates the earliest application in the ’582 priority chain by more than five years.

196. Niknejad articulates that “[r]esearch in silicon mm-wave circuits and technology started at universities and research institutions and now continues in the commercial realm. Many of the researchers in the field have contributed to this book to chronicle these efforts.” Niknejad (EX-1007) at 6. Niknejad explains:

This book is written for practicing RF and analog circuit designers who wish to join this exciting and growing field. The chapters are self-contained and include a short tutorial on important concepts before delving into details. The audience for this book is assumed to be experienced in the field of analog/RF integrated circuits. The focus of each chapter is the key innovations and techniques that enable operation at mm-wave frequencies, which is close to the activity limits of silicon technology.

Id.

197. Sections 3.1.2 and 3.1.3 of Niknejad address inductors and capacitors, respectively, as both are used extensively in resonant circuits. *Id.* at 25-27. And Section 3.1.3.1 elaborates on finger capacitors. “Finger (comb) capacitors, sometimes referred to as MOM (metal-oxide-metal) capacitors, can be easily fabricated in any modern CMOS process due to the abundance and high packing

density of the metal layers.” *Id.* at 27 (internal quotation marks omitted). In terms of internal structure, as Niknejad explains, “[f]inger capacitors are composed of a large number of parallel fingers connected to either port of the device as shown in Fig. 3.11,” reproduced below. *Id.*

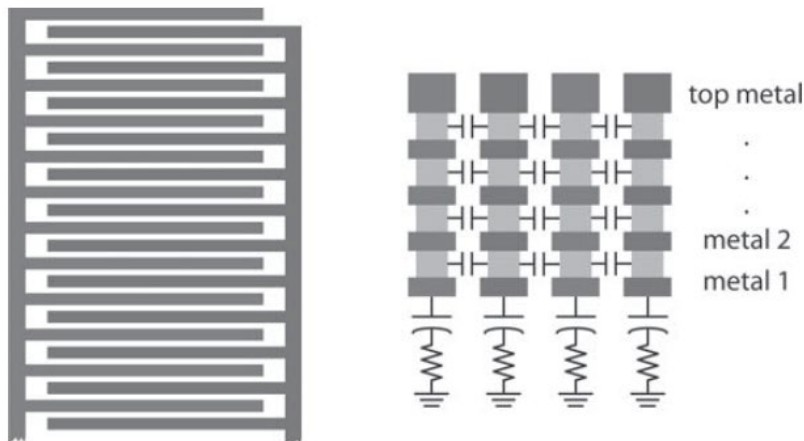


Fig. 3.11 Layout geometry of a “finger” or “comb” capacitor structure.

Id.

198. Fabrication of multi-layer finger capacitors was known well before the time of the ’582 filing. For instance, as Niknejad explains, in one approach, “[e]ach finger consists of all available metal layers stacked on top of each other in order to decrease its resistance whi[le] increasing both its quality factor and the self-resonance frequency.” *Id.* As shown in Fig. 3.11 above, “[t]he metal layers are connected together through the maximum number of vias possible in order to take advantage of the additional via-to-via capacitance.” *Id.*

199. As I discussed above, Muh discloses in the test chip of its LC resonant circuit, “the capacitor is implemented as an interdigitated finger capacitor,” although its simulation model in Fig. B-3 shows a simple parallel-plate capacitor instead. Muh (EX-1006) at 57. To the extent Muh’s Fig. B-3 does not expressly show an interdigitated finger capacitor, it would have been obvious to a POSITA before the time of the 582 patent filing that an interdigitated finger capacitor (e.g., the one disclosed by Niknejad) would easily replace the parallel-plate capacitor shown in Muh’s Fig. B-3, as taught by Muh itself, such that the interdigitated finger capacitor would have its connecting segments overlapped with the extension-conductor segments of the inductor in a vertical direction and would have its electrode segments extend laterally relative to respective coupled connecting segments. I provide my analysis of why a POSITA would have been motivated to make this simple substitution in paragraphs 249-252 below.

C. Muh in Combination with Niknejad Invalidates Claim 1

1.1 A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

200. To the extent this preamble of claim 1 is a limitation, Muh discloses it, as Muh discloses a semiconductor device with an LC resonant circuit. Muh’s introduction discusses complementary metal-oxide semiconductor (CMOS) semiconductor technology, which a POSITA would have understood was used in

most integrated circuits (ICs) at the time. Muh (EX-1006) at 6. Muh specifically discusses semiconductor technology in the introduction:

Technology scaling has enabled CMOS devices to operate at these high frequencies, and numerous millimeter-wave CMOS circuits have been reported in the literature. Compared to the traditional III-V *semiconductor* technologies used for monolithic microwave integrated circuits, CMOS implementations promise higher levels of integration and reduced cost, and thus may begin to make inroads into the compound *semiconductor*-dominated market in the foreseeable future.

Id. at 7 (emphasis added).

201. As I mentioned previously, Muh discloses a VCO that contains an LC resonant circuit. For example, Muh’s Fig. B-3 (reproduced below) shows a simulation model of a “resonant tank on [a] test chip,” which is or includes a semiconductor device. The simulation model uses a high-frequency three-dimensional field solver (HFSS), which is a 3D simulation software tool used for simulating integrated circuits. Muh (EX-1006) at 56.

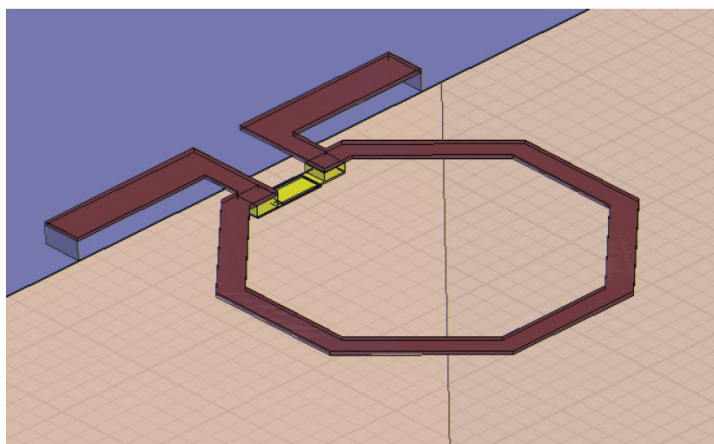
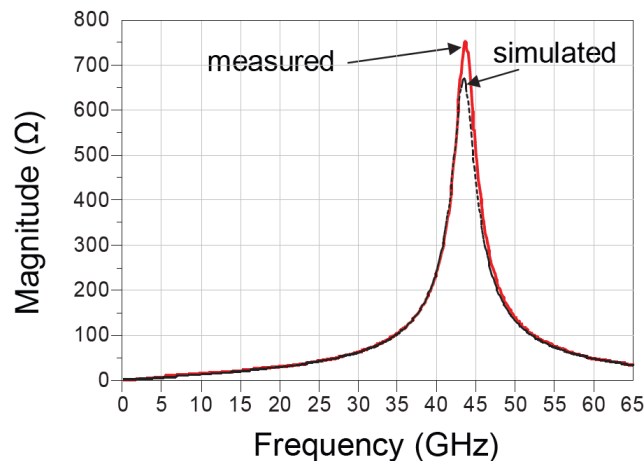


Figure B-3. HFSS model of parallel resonant tank on test chip.

Muh (EX-1006) at Fig. B-3.

202. Muh specifically notes that “[t]he second structure simulated in HFSS is a *resonant tank* consisting of the same *inductor in parallel with a capacitor*.”

Muh (EX-1006) at 57 (emphasis added). Further, Muh’s Fig. B-4, reproduced below, shows that its LC circuit resonates at a resonating frequency. Therefore, taking Muh’s disclosures together, a POSITA would have understood the above to disclose the inductor-capacitor (LC) resonant circuit recited in claim 1’s preamble.



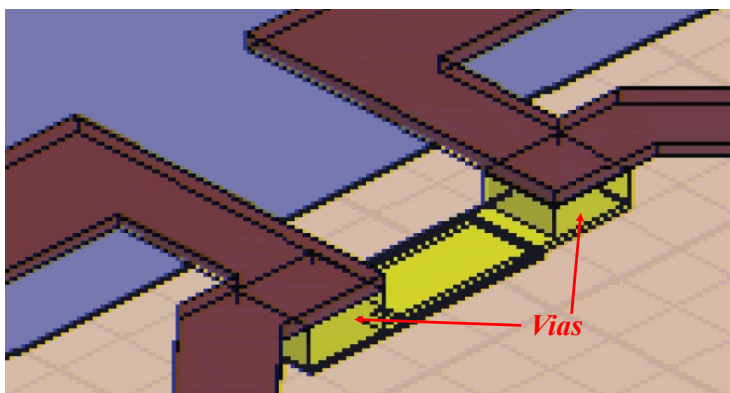
Muh (EX-1006) at Fig. B-4 left half.

1.2a first insulation layer

203. Muh discloses a first insulation layer. Muh discloses that, in the HFSS simulation, a “multi-layer dielectric stack was modeled with two layers: a passivation layer and an oxide layer.” Muh (EX-1006) at 41; *see also Id.* at 56 (“To simplify the simulation, the entire multi-level dielectric stack was lumped into two layers, representing the passivation layer and the rest of the dielectric stack.”). As I

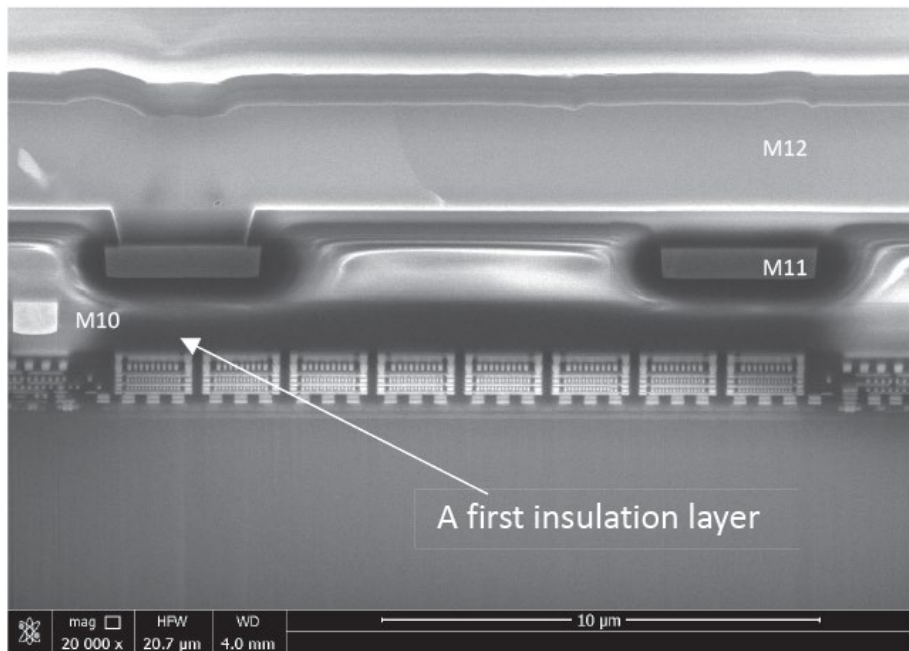
explained above with respect to Invalidity Ground 1, a POSITA would have understood that a dielectric (e.g., an oxide) is an insulation material that can form one or more insulation layers. Therefore, part of Muh's dielectric stack (e.g., the oxide layer or a portion thereof) forms a first insulation layer.

204. Further, Muh's Fig. B-3 (a partial view reproduced below) shows vias connecting an inductor to a capacitor in the LC resonant circuit. A POSITA would have understood that the vias, which are metal structures that connect stacked metal layers, would be implemented in and surrounded by an insulation layer. Therefore, to the extent Muh's Fig. B-3 does not expressly show a first insulation layer, a POSITA would have understood that there would be a first insulation layer between a top metal layer (where the inductor is) and lower metal layers (where the capacitor is). The first insulation layer would surround the vias shown in Fig. B-3.



Muh (EX-1006) at Fig. B-3 partial view (annotated added in red).

205. This interpretation is consistent with how Realtek interprets the first insulation layer, as shown below.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 7 (Realtek annotations retained).

206. Furthermore, as I explained previously, the use of insulation layers and metal layers in semiconductor devices were well known in the art before the time of the '582 filing. Indeed, the '582 Patent acknowledges this in its background section. *See* '582 Patent (EX-1001) at 1:24-28 (“A typical semiconductor integrated circuit includes a silicon substrate. ***More than one insulation layer is arranged on the substrate, more than one metal layer [cis] is arranged in the insulation layer,*** and the metal layers may be formed with a built-in part of a chip by means of a semiconductor fabrication process.”) (emphasis added).

1.3an inductor component, comprising

207. Muh discloses an inductor component. For instance, Figure B-1 of Muh shows a typical “loop inductor on test chip,” which I have reproduced below. Muh explains that the loop inductor utilizes “the top metal layer” of the semiconductor fabrication process. Muh (EX-1006) at 56.

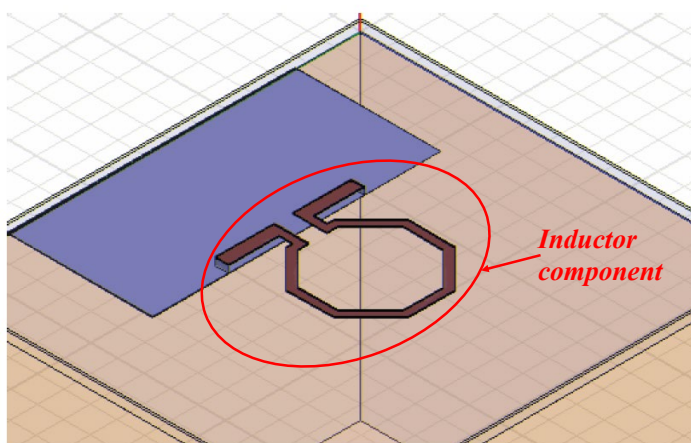


Figure B-1. HFSS model of loop inductor on test chip.

Muh (EX-1006) at Fig. B-1 (annotations added in red).

208. Similarly, Muh’s Fig. B-3 shows a “structure simulated in HFSS [which] is a resonant tank consisting of the *same inductor* in parallel with a capacitor.” Muh (EX-1006) at 57 (emphasis added). As would be evident to a POSITA, the inductor has the same general shape and placement as the inductor previously discussed, thus references to the shape and positioning of the inductor of Fig. B-1 would also apply to the inductor of Fig. B-3 below. Figure 3 simply additionally includes a parallel capacitor.

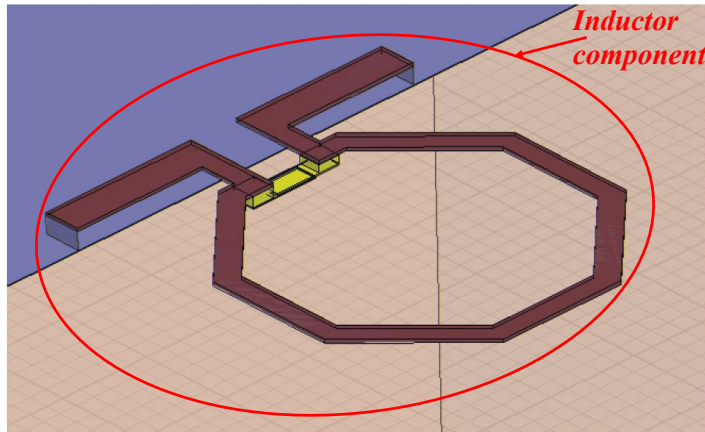
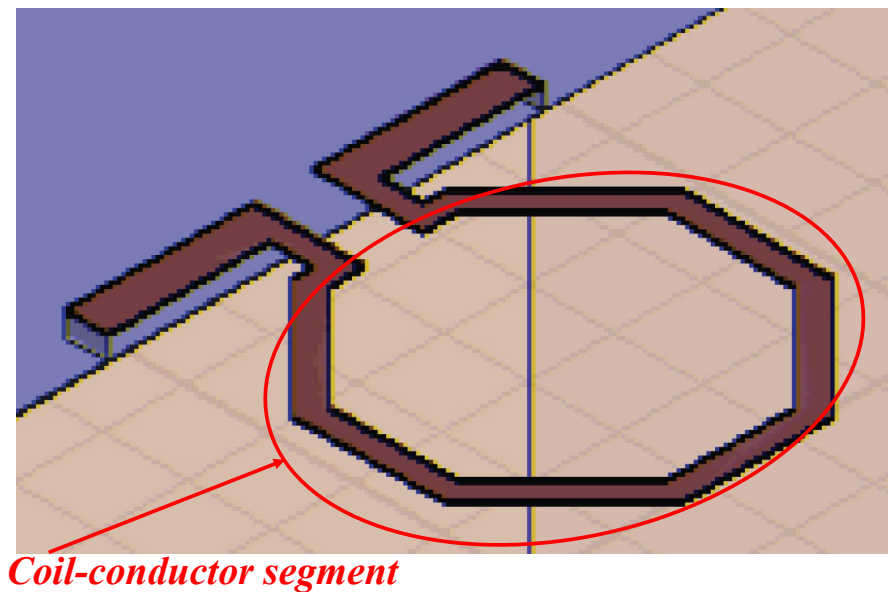


Figure B-3. HFSS model of parallel resonant tank on test chip.

Muh (EX-1006) at Fig. B-1 (annotations added in red).

**1.4a coil-conductor segment, located on a surface of the first insulation layer;
and**

209. Muh discloses this limitation. For example, Muh's inductor includes a conducting coil-conductor segment, as illustrated in Fig. B-1 and Fig. B-3.



Muh (EX-1006) at 56, Fig. B-1 (annotations added in red).

210. The coil-conductor segment serves as an induction part of Muh's inductor for electromagnetic induction. For example, as illustrated in Muh's Fig. B-2 (reproduced below), the inductor has an inductance value that varies with frequency. The below measured and simulated results for the test chip inductor of Fig. B-1 would also apply to the inductor of Fig. B-3 because, as I just explained, the same inductor design was used.

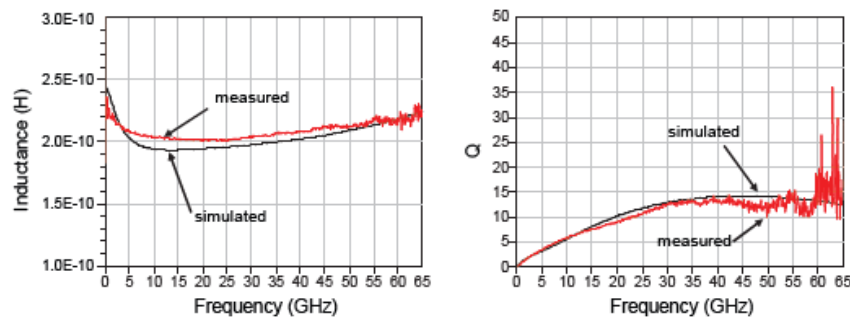
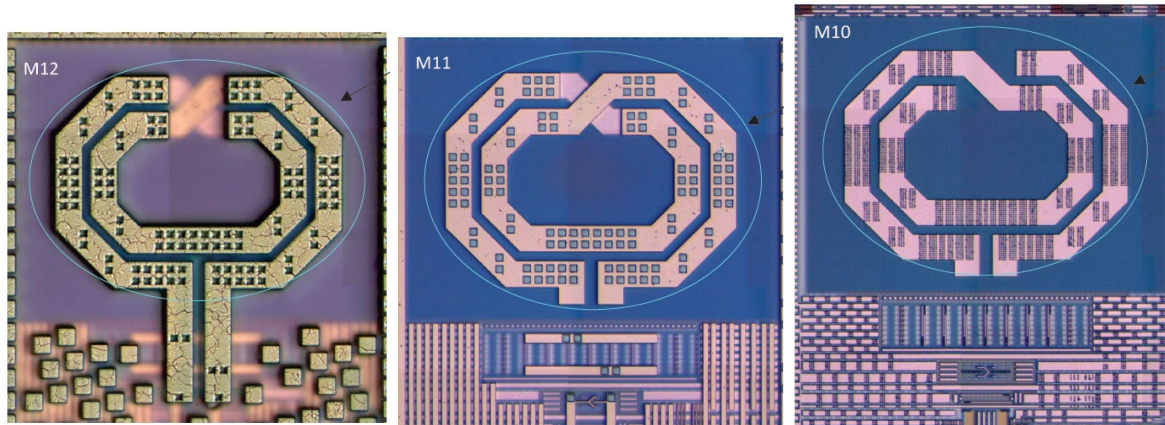


Figure B-2. Comparison of measured and simulated results for test-chip inductor.

Muh (EX-1006) at Fig. B-2.

211. This interpretation is consistent with how Realtek interprets the coil-conductor segment of the inductor, as shown below, where the coil-conductor segment is marked by light blue ovals.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 9-10 (Realtek annotations retained).

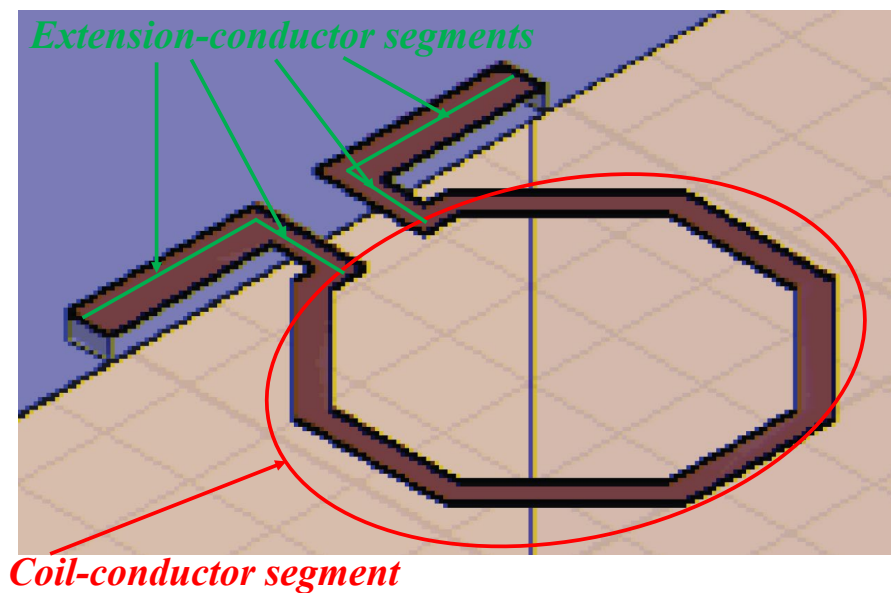
212. The coil-conductor segment of Muh’s inductor is located on a surface of the first insulation layer. For example, Muh explains that “the first structure is a loop inductor *utilizing the top metal layer* of the process.” Muh (EX-1006) at 56 (emphasis added). Further, as I explained above with respect to the claim limitation “a first insulation layer,” Muh’s Fig. B-3 shows vias connecting an inductor to a capacitor in the LC resonant circuit. To the extent Muh’s Fig. B-3 does not expressly show the first insulation layer, a POSITA would have understood that there would be a first insulation layer located between the top metal layer (where the inductor is) and the lower metal layers and surrounding the vias. Accordingly, in view of Muh, a POSITA would have understood that the inductor’s coil-conductor segment would be located on a surface of the first insulation layer.

213. This interpretation is consistent with how Realtek interprets this limitation. See Realtek Exhibit 32 to ITC Complaint (EX-1034) at 9 (alleging that,

in the accused products, “the coil-conductor segment is located on a surface of the first insulation layer (which is located approximately below the M10 layer)”).

1.5 two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

214. Muh discloses this limitation. For example, Muh’s inductor includes two extension-conductor segments, as I have highlighted below in green in Fig. B-1.

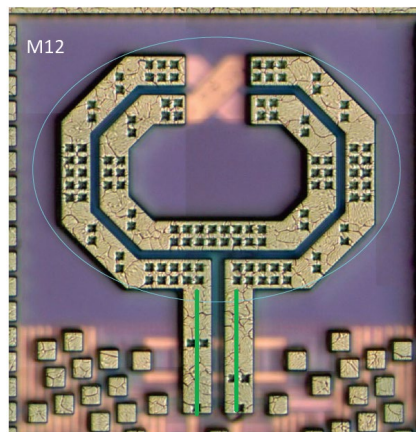


Muh (EX-1006) at Fig. B-1 (annotations added in red and green); *see also id.* at Fig. B-3 (same).

215. In Muh, the extension-conductor segments serve as an input/output part of its inductor. For instance, the two extension-conductor segments are described as “lumped ports” used to connect the inductor to other parts of Muh’s VCO. Muh (EX-1006) at 56; *see Id.* at 41-44.

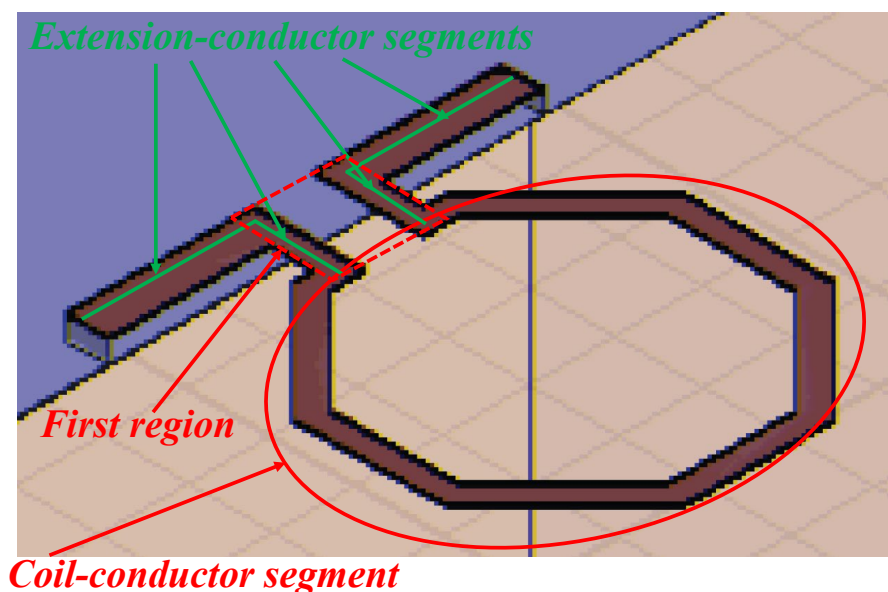
216. Like the coil-conductor segment of Muh’s inductor, the two extension-conductor segments are located on the same surface of the first insulation layer. Muh explains that its loop inductor—including its coil conductor segment and extension-conductor segments—utilizes “the top metal layer.” Muh (EX-1006) at 56. Further, as shown in Fig. B-3, the two extension-conductor segments are coupled to two ends of the coil-conductor segment respectively, are arranged at an interval, and extend outwards relative to the coil-conductor segment.

217. Muh’s disclosures are consistent with how Realtek interprets the two extension-conductor segments of the inductor, as shown below, where the extension-conductor segments are marked by green lines.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 11 (Realtek annotations retained).

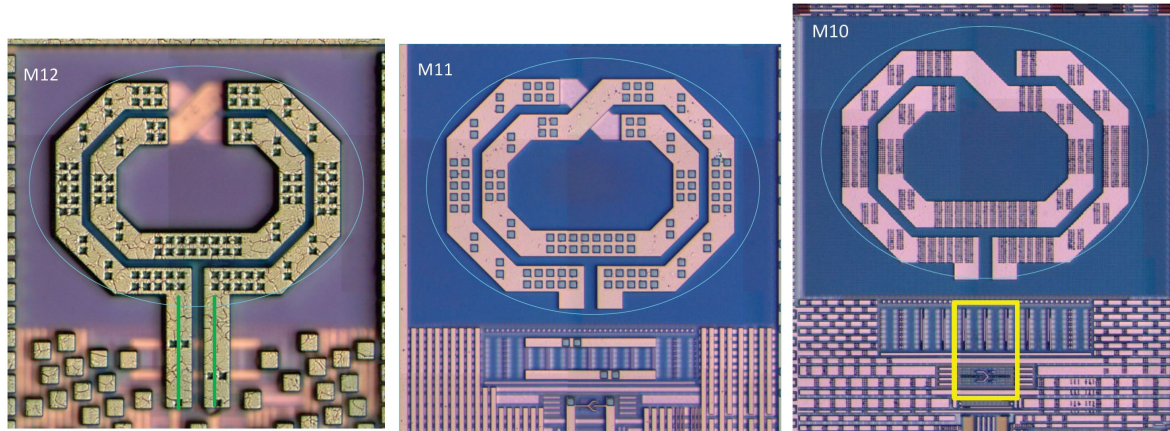
218. Further, based on how Realtek interprets the claim phrase “a first region defined by the two extension-conductor segments and the coil-conductor segment,”³ Muh discloses such a first region, as illustrated in Figs. B-1 and B-3.



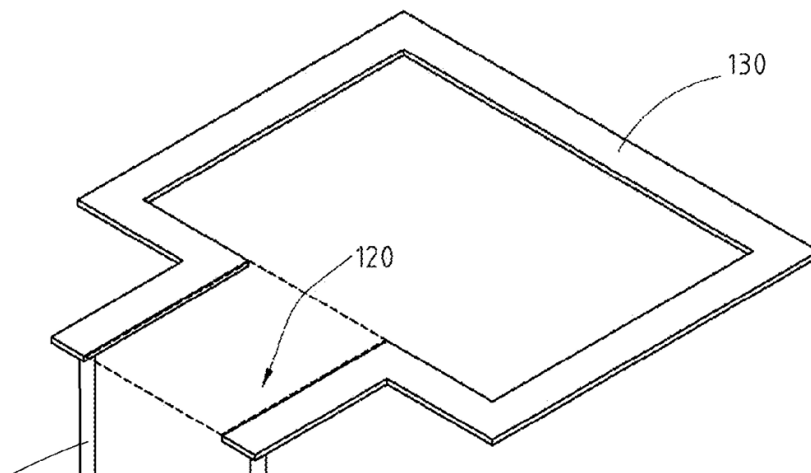
Muh (EX-1006) at Fig. B-1 (annotations added in red and green).

219. This interpretation is consistent with how Realtek interprets the claimed “first region,” as shown below, where the first region is marked by a yellow box.

³ As I discussed prior, I believe this claim phrase is indefinite because its scope would not be reasonably clear to a POSITA. Nonetheless, I am able to apply Muh and Niknejad against this claim term for purposes of my obviousness analysis.

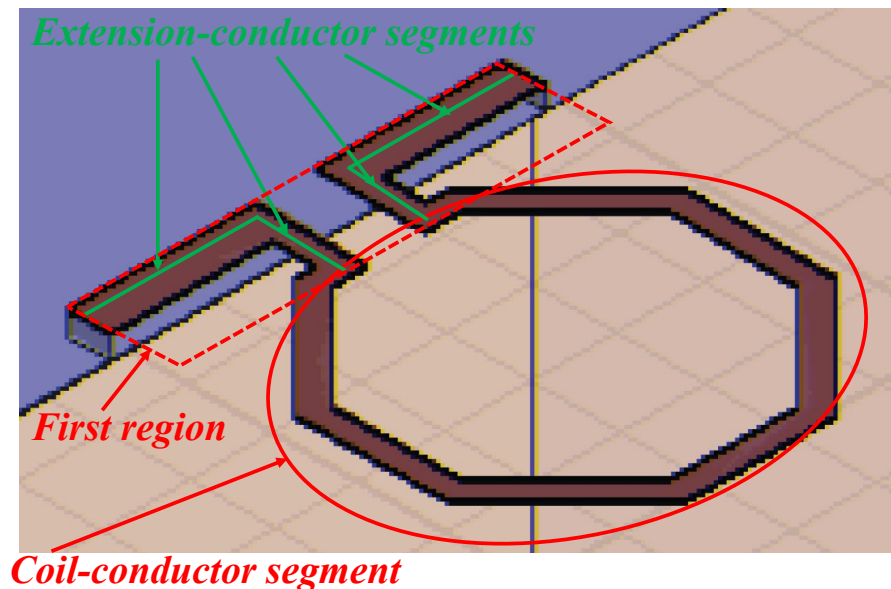


Realtek Exhibit 32 to ITC Complaint (EX-1034) at 12-13 (Realtek annotations retained). And this is consistent with the “first region 120” as described and illustrated in the ’582 Patent. For example, in Fig. 6 of the ’582 Patent, reproduced below, “a region 120 (hereinafter referred to as a first region 120) is defined by the two extension-conductor segments 133 and 135 and the coil-conductor segment 131.” ’582 Patent (EX-1001) at 3:45-47.



’582 Patent (EX-1001) at Fig. 6 partial view.

220. A POSITA would also have appreciated that, in Muh, the two extension-conductor segments of the loop inductor extend away from the coil-conductor segment to each form an “L” shape, as illustrated by green lines below. In this case, the “first region” would cover a wider area, as illustrated by a dashed red box below.

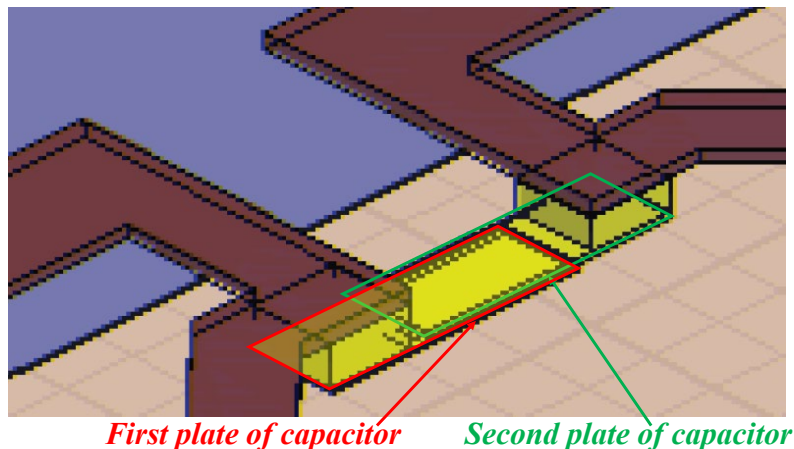


Muh (EX-1006) at Fig. B-1 (annotations added in red and green).

1.6a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer,

221. Muh renders this limitation obvious, as Muh discloses everything except for the “embedded manner” part of the limitation. For example, Muh’s simulated structure uses a “a resonant tank consisting of the same inductor in parallel with a capacitor.” The capacitor shown in Fig. B-3 is “a simple horizontal

parallel-plate capacitor,” which is or includes a capacitor component. The two (first and second) plates of the parallel-plate capacitor are illustrated below. Based on how Realtek has interpreted the term “first region,” Muh’s parallel-plate capacitor is arranged corresponding to the first region, as shown in Fig. B-3.



Muh (EX-1006) at Fig. B-3 partial view (annotations added in red and green).

222. To the extent Muh’s Fig. B-3 does not expressly disclose a first insulation layer with a surface on which the capacitor component is arranged in an embedded manner opposite to the inductor component, as explained above, it would have been obvious to a POSITA to use a first insulation layer between the top metal layer (where the inductor is) and the lower metal layers (where the capacitor is). Indeed, Realtek interprets this limitation as allegedly being met by a capacitor that is in a lower metal layer adjacent to the insulation layer. Realtek Exhibit 32 to ITC Complaint (EX-1034) at 13 (stating that a “capacitor component” is located “in an embedded manner on the other surface (i.e., in the

M9 layer adjacent to the first insulation layer), opposite to the inductor component, of the first insulation layer”). Accordingly, a POSITA would have understood that Muh’s parallel-plate capacitor is arranged on the other surface, opposite to the inductor component, of the first insulation layer.

223. It would have been obvious to a POSITA that Muh’s parallel-plate capacitor would naturally be arranged in an embedded manner on the other surface of the first insulation layer that is opposite to its inductor component. Embedding electronic elements such as a capacitor component on the surface of an insulation layer was not new. As the ’582 Patent acknowledges in its background section, it was well known that, “in order to reduce the volume of an electronic product, various electronic elements [such as capacitor components] are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).” ’582 Patent (EX-1001) at 1:29-32; *see also id.* at 8:40-42 (“Here, the structures of various embedded electronic elements are well known to in the field, and therefore are no longer elaborated.”). Muh likewise discloses the well-known technique of embedding metal structures in an insulation layer. *See, e.g.,* Muh (EX-1006) at 42 (“In the setup on the left in Fig. 3-11, the ground ring is embedded in the oxide and does not touch the substrate.”). A POSITA would therefore have understood that Muh implements its components in an embedded manner as the ’582 patent admits was known and advantageous.

224. Additionally, Muh in combination with Niknejad renders this limitation obvious. Specifically, Muh explains that, “[i]n the test chip, the capacitor is implemented as an *interdigitated finger capacitor*, with each finger *comprising the bottom five metal layers strapped together*.” Muh (EX-1006) at 57 (emphasis added). As I explained in the introduction above, Niknejad discloses exactly such finger capacitors, as follows:

“Finger” (comb) capacitors, sometimes referred to as “MOM” (metal-oxide-metal) capacitors, can be easily fabricated in any modern CMOS process due to the abundance and high packing density of the metal layers. Finger capacitors are composed of a large number of parallel fingers connected to either port of the device as shown in Fig. 3.11. Each finger consists of all available metal layers stacked on top of each other in order to decrease its resistance whi[le] increasing both its quality factor and the self-resonance frequency. The metal layers are connected together through the maximum number of vias possible in order to take advantage of the additional via-to-via capacitance.

Niknejad (EX-1007) at 27.

225. Therefore, to the extent Muh’s Fig. B-3 does not expressly show an interdigitated finger capacitor, it would have been obvious to a POSITA before the time of filing of the ’582 patent that a finger capacitor (e.g., the one disclosed by Niknejad) would easily replace the parallel-plate capacitor, as taught by Muh (e.g., by using Muh’s “bottom five metal layers” of its finger capacitor as Niknejad’s “available metal layers” of its finger capacitor). Muh (EX-1006) at 57; Niknejad

(EX-1007) at 27. Upon such replacement, the finger capacitor would be or would include a capacitor component. Further, it would have been obvious to a POSITA to place the finger capacitor in the same location as Muh's parallel-plate capacitor such that the finger capacitor is arranged corresponding to the first region on the other surface, opposite to the inductor component, of the first insulation layer. In addition, it would have been obvious to a POSITA that Niknejad's finger capacitor would naturally be arranged in an embedded manner on the other surface of the first insulation layer that is opposite to its inductor component. Indeed, the right half of Niknejad's Fig. 3.11 illustrates five metal layers that make up its finger capacitor, where the top metal layer of the finger capacitor is embedded in and surrounded by insulation material. As further explained below in the "Motivations to Combine Muh and Niknejad" section, a POSITA would have been motivated before the time of the '582 filing to implement Niknejad's finger capacitor into Muh's LC resonant circuit for a multitude of reasons. *See infra* ¶¶ 249-252.

226. Notably, both Muh and Niknejad disclose using the same type of multi-layer finger capacitors. *See* Muh (EX-1006) at 57 ("In the test chip, the capacitor is implemented as an interdigitated finger capacitor, with each finger comprising the bottom five metal layers strapped together."); Niknejad (EX-1007) at 27 (disclosing that, in its finger capacitor, "[e]ach finger consists of all available metal layers stacked on top of each other" and the "metal layers are connected

together through the maximum number of vias possible.”). Niknejad’s Fig. 3.11 illustrates five metal layers that make up its finger capacitor. A POSITA would have understood that the top metal layer of the finger capacitor is an example of “a capacitor component” that meets this claim limitation.

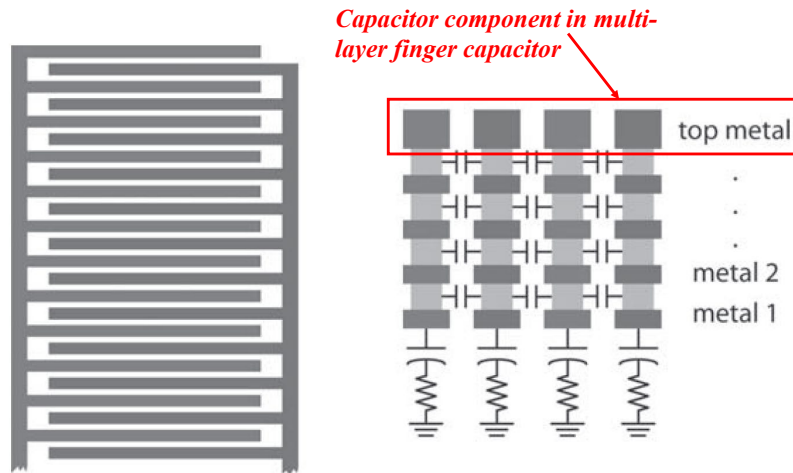


Fig. 3.11 Layout geometry of a “finger” or “comb” capacitor structure.

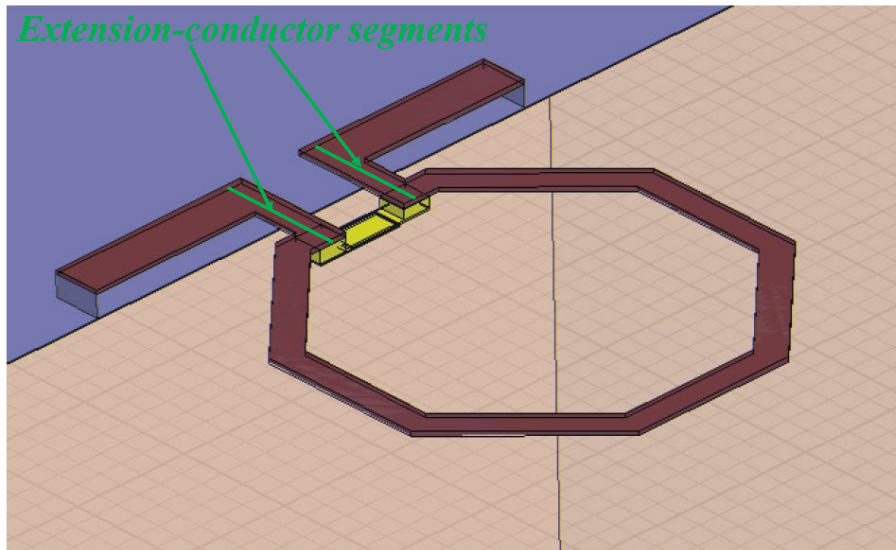
Id.

227. To sum up, as explained above, Muh—as well as Muh in combination with Niknejad—renders this limitation obvious.

1.7 wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,

228. Muh discloses this limitation. For example, Muh’s Fig. B-3 shows a capacitor component configured outwards relative to the coil-conductor segment of Muh’s inductor. Additionally, the capacitor component is not substantially

overlapped with the coil-conductor segment of Muh's inductor. The spatial arrangement is plainly visible from Muh's Fig. B-3.



Muh (EX-1006) at Fig. B-3 (annotations added in red and green).

229. This interpretation is consistent with the '582 Patent. For example, the '582 Patent describes with reference to its Fig. 9 that "the connecting segment 171 is overlapped with the corresponding extension-conductor segment 133." '582 Patent (EX-1001) at 7:50-51. To illustrate such an overlapping, Fig. 9 is reproduced below where the connecting segment 171 (in red shade below) on a bottom layer is vertically projected upward onto the extension-conductor segment 133 (in green shade below) on a top layer. Notably, the '582 Patent does *not* describe that the connecting segment 171 is overlapped with the coil-conductor segment 131 (in yellow shade below).

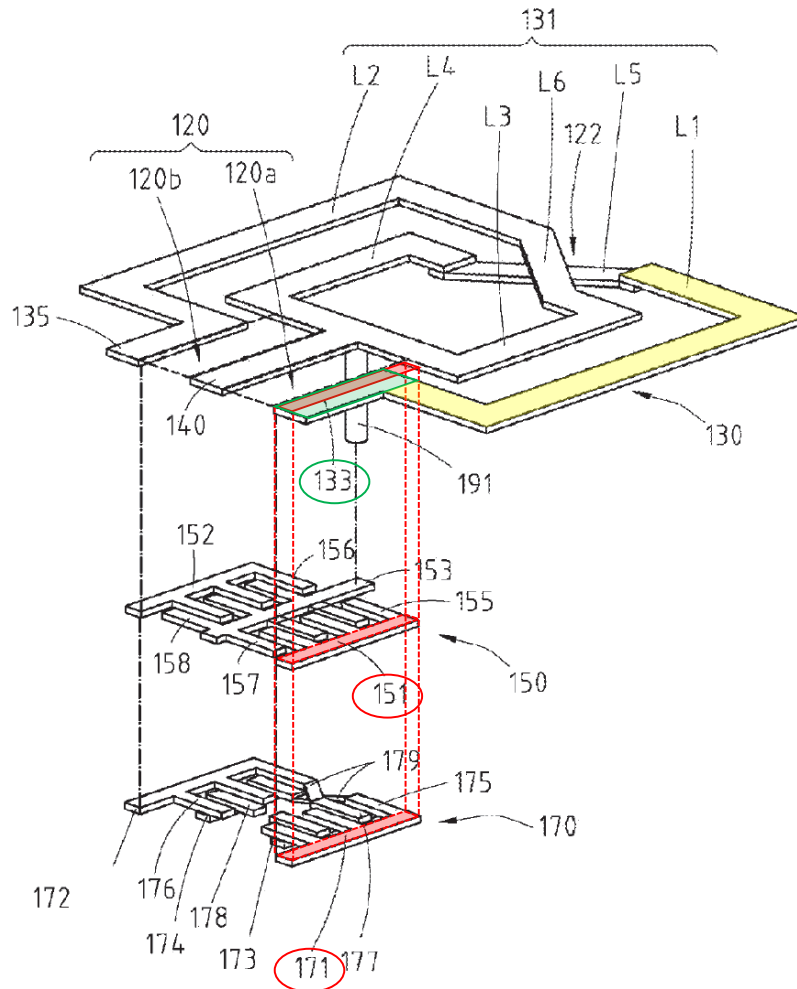


FIG. 9

Id. at Fig. 9.

230. Consistent with Fig. 9, the '582 Patent further describes that its coil-conductor segment 131 stops at its first and second ends:

The extension-conductor segment 133 is joined to **a first end** of the coil-conductor segment 131 and is approximately perpendicular to a joining position between the extension-conductor segment 133 and the coil-conductor segment 131. The extension-conductor segment 135 is joined to **a second end** of the coil-conductor segment 131 and is approximately perpendicular to a joining part of the extension-conductor segment 135 and the coil-conductor segment 131.

'Id. at 4:1-9 (emphasis added).

231. Therefore, a POSITA would have understood, in the '582 Patent, the coil-conductor segment 131 (in yellow shade below) stops at “a first end” and does **not** include the area where “the connecting segment 171 is overlapped with the corresponding extension-conductor segment 133.” *Id.* at 4:1-9, 7:50-51; *see also id.* at 4:62-64 (“The first connecting segment 151 may be located below the extension-conductor segment 133 and is overlapped with the extension-conductor segment 133.”). For the same reason, the coil-conductor segment 131 also stops at “a second end,” and does **not** include the area where “the connecting segment 172 is overlapped with the corresponding extension-conductor segment 135.” *Id.* at 7:52-53; *see also id.* at 4:64-67. This is clearly illustrated below using Fig. 8 of the '582 Patent, which shows a top view of the circuit in Fig. 9, but with connecting segments 171 and 172 hidden under connecting segments 151 and 152, respectively.

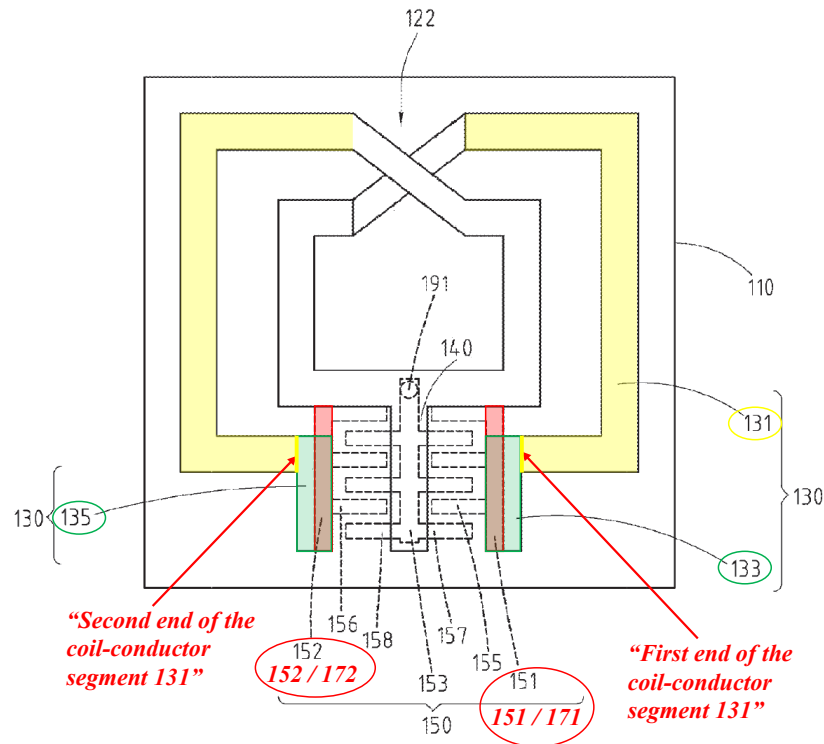
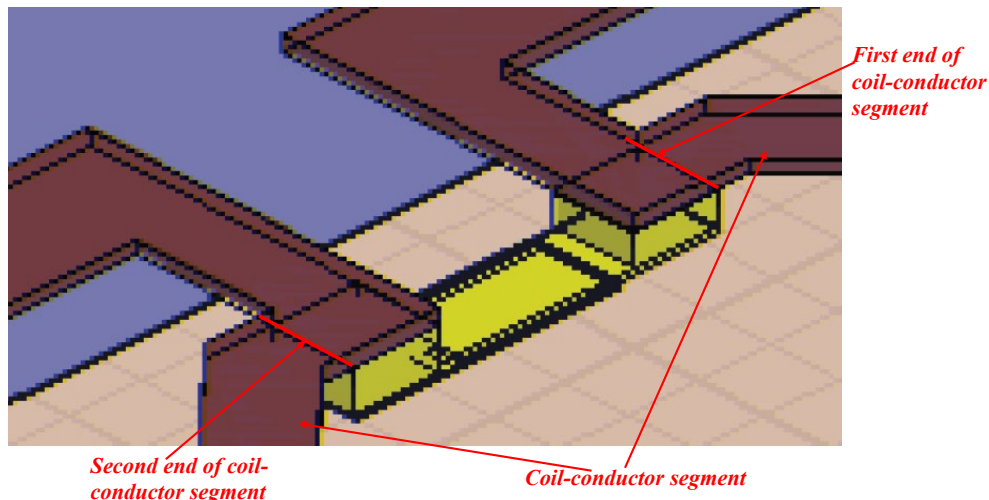


FIG. 8

Id. at Fig. 8 (annotations added in color).

232. Consistent with how the '582 Patent describes its coil-conductor segment, Muh's coil-conductor segment stops at its first and second ends (which are illustrated in Fig. B-3 below by red lines), and does **not** include areas where Muh's connecting segments are overlapped with the underlying capacitor component. Therefore, Muh's capacitor component is not overlapped at all, let alone substantially overlapped, with the coil-conductor segment of Muh's inductor.



Muh (EX-1006) at Fig. B-3 (annotations added in red).

233. In fact, even assuming *arguendo* that Muh’s capacitor component is partially overlapped with the coil-conductor segment of Muh’s inductor, which it is not, a POSITA would have recognized in view of Muh’s Fig. B-3 that Muh’s capacitor component is still “not substantially overlapped” with its coil-conductor segment. The ’582 specification provides no objective measurements or boundaries to assist a POSITA in determining whether the capacitor component is “not substantially overlapped” with the coil-conductor segment. This limitation was added during prosecution of the ’582 Patent, and so the only time the word “substantially” appears in the 582 patent is in claim 1. *See* Office Action Response dated June 17, 2016, pp. 2, 6 (EX-1002 at 70, 74).

234. A POSITA would consider the word “substantially” in this context to be a term of degree, meaning, e.g., “most of” or “largely.” For example, the relevant definition from Merriam-Webster’s Dictionary (www.merriam-

webster.com) is “being largely but not wholly that which is specified.” EX-1035 at 1. If the capacitor component was “substantially overlapped” with the coil-conductor segment, a POSITA would have expected that to mean that the capacitor component mostly or largely overlapped, that is, is most of the capacitor component overlapped with the coil-conductor segment. As the claim requires “not substantially overlapped,” a POSITA would have interpreted that to mean that most of the capacitor component does not overlap with the coil-conductor segment. This leaves open that at least a small portion of the capacitor component may overlap. Indeed, as shown in Figs. 8 and 9 of the ’582 Patent, capacitor components 150 and 170 are considered “not substantially overlapped” with the coil-conductor segment 131 even though portions of capacitor components 150 and 170 are located *fully inside* the coil-conductor segment 131 (in Fig. 8 reproduced below, see red shaded area that extends above segment 131). The extent of overlapping in Fig. 8 of the ’582 Patent is more substantial than in Muh. Therefore, even assuming *arguendo* a small portion of Muh’s capacitor component is overlapped with the coil-conductor segment of Muh’s inductor, it is still “not substantially overlapped” with the coil-conductor segment.

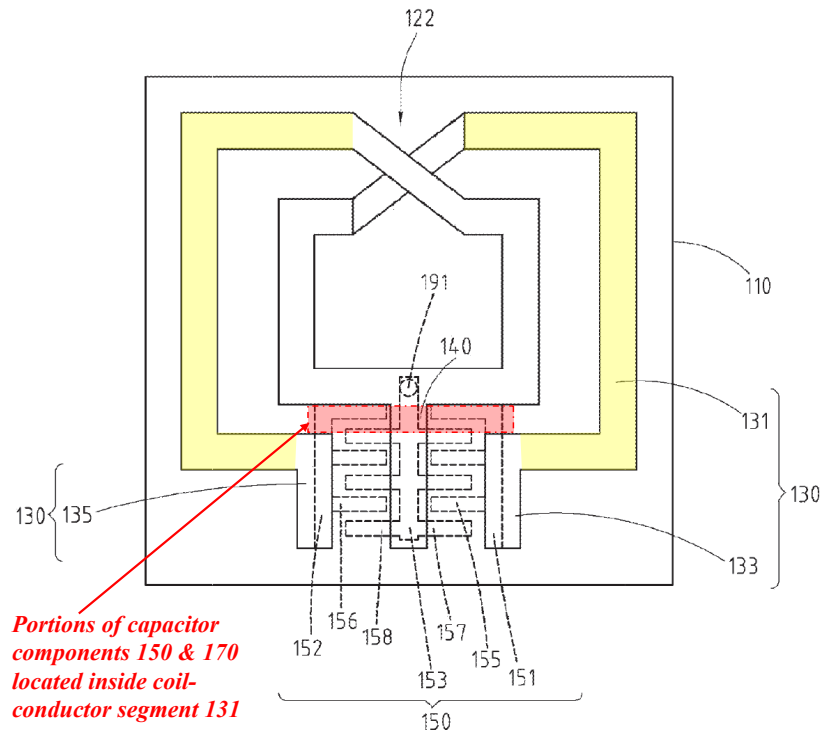
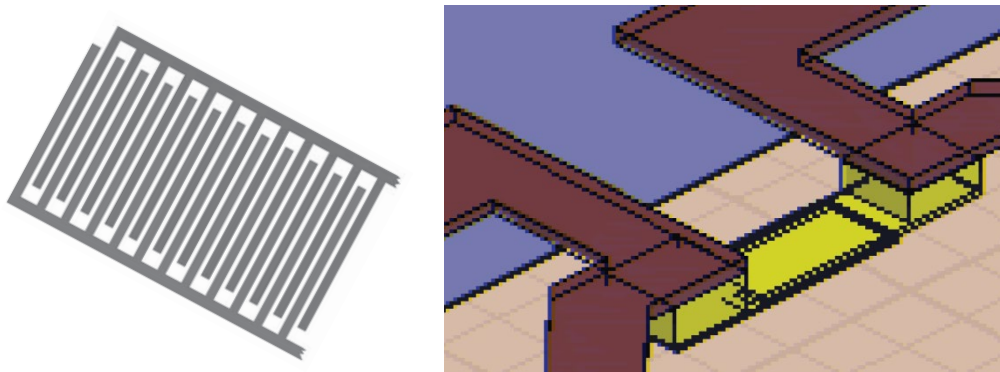


FIG. 8

'582 Patent (EX-1001) at Fig. 8 (annotations added in color).

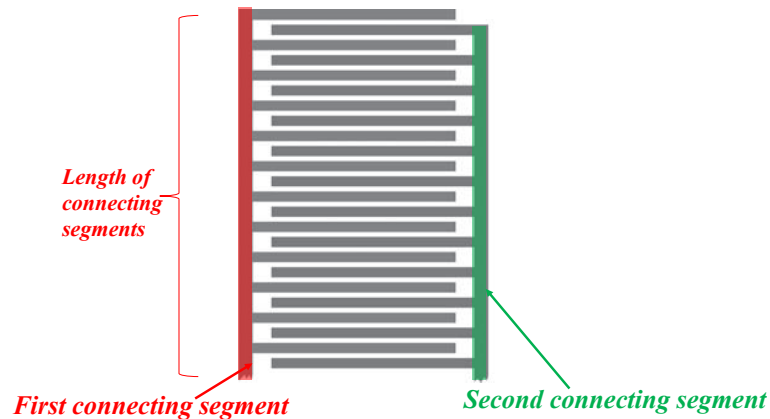
235. Additionally, Muh in combination with Niknejad renders this limitation obvious. Specifically, as I explained above, it would have been obvious to a POSITA to replace the parallel-plate capacitor of Muh's Fig. B-3 with a finger capacitor disclosed by Niknejad, as such replacement is expressly taught by Muh. Upon replacement, the finger capacitor would be correspondingly configured outwards relative to the coil-conductor segment of Muh's inductor, and the finger capacitor would not be substantially overlapped with the coil-conductor segment of Muh's inductor, as illustrated below:



Niknejad (EX-1007) at Fig. 3.11 left half rotated view (left); Muh (EX-1006) at Fig. B-3 partial view (right).

236. Notably, the finger capacitor disclosed by Niknejad can include a large number of fingers (e.g., 24 fingers shown in Niknejad’s Fig. 3.11). Niknejad further discloses that, “to realize a given capacitance, either a large number of short fingers in parallel or a small number of long fingers can be used.” Niknejad (EX-1007) at 28. When a large number of fingers—which are separated by gaps—are used in the finger capacitor, a POSITA would have recognized that the two (first and second) connecting segments of a finger capacitor would need to be relatively long in order to fit all the fingers, as illustrated in Fig. 3.11 below. As a result, when replacing Muh’s parallel-plate capacitor with a finger capacitor with a large number of short fingers, it is expected that the finger capacitor would extend further away from the core-segment of the inductor than Muh’s parallel-plate capacitor. Therefore, the finger capacitor would be correspondingly configured even more outwards relative to the coil-conductor segment, and the finger

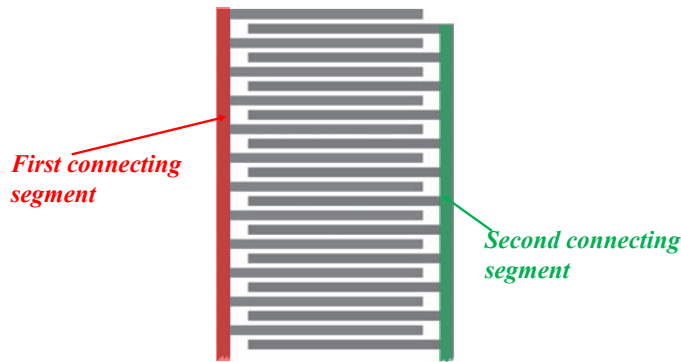
capacitor would still not be substantially overlapped with the coil-conductor segment.



Niknejad (EX-1007) at Fig. 3.11 left half (annotations added in red and green).

1.8 wherein the capacitor component comprises: a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

237. Muh in combination with Niknejad renders this limitation obvious. Specifically, as I explained above, it would have been obvious to a POSITA to replace the parallel-plate capacitor of Muh's Fig. B-3 with a finger capacitor disclosed by Niknejad, as such replacement is expressly taught by Muh. Niknejad's finger capacitor includes two (first and second) connecting segments, as illustrated below.

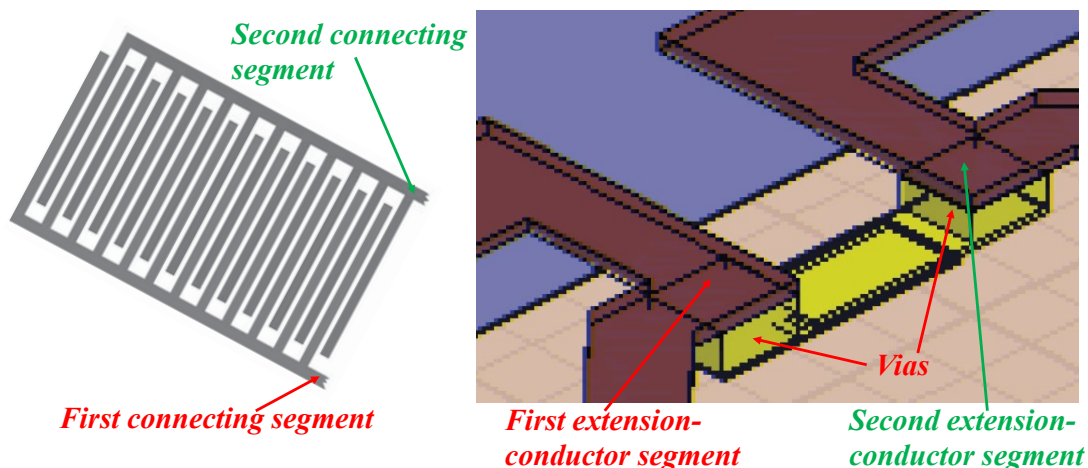


Niknejad (EX-1007) at Fig. 3.11 left half (annotations added in red and green).

238. In Niknejad, the first and second connecting segments of the finger capacitor are used for connecting the finger capacitor to other circuit components (e.g., for receiving or transmitting a signal from an inductor). For example, “[a]t each port, a wide slab consisting of a small 45° taper is used to connect the fingers.” Niknejad (EX-1007) at 28. A POSITA would have recognized each connecting segment is a “port” used for connecting a capacitor to an inductor in an LC tank. *Id.* (“Finger capacitors are composed of a large number of parallel fingers **connected to either port of the device** as shown in Fig. 3.11.”) (emphasis added); *see also* Muh (EX-1006) at 57(“The second structure simulated in HFSS is a **resonant tank** consisting of the same **inductor in parallel with** a capacitor.”) (emphasis added).

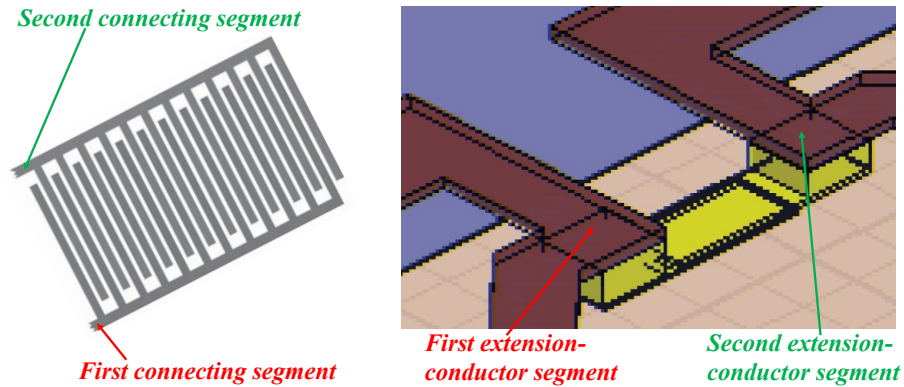
239. Further, it would have been obvious to a POSITA that, when placing a finger capacitor into Muh’s LC tank, the finger capacitor would be easily placed such that its two connecting segments extend corresponding to the two extension-conductor segments of Muh’s inductor in a same direction, and its connecting

segments are respectively overlapped with the two extension-conductor segments in a vertical direction. This would have been an obvious design choice that has a reasonable expectation of success. For example, such placement of the finger capacitor allows its connecting segments to be directly connected to the overlaying inductor through use of vias. Muh already discloses vias between the inductor and the parallel-plate capacitor, so it would have been obvious that the same or similar vias would be used to connect the finger capacitor to the inductor without the need for extra horizontal metal traces. As illustrated below, a first connecting segment of Niknejad's finger capacitor directly connects to a first extension-conductor segment of Muh's inductor through one or more vias. In the same way, a second connecting segment of Niknejad's finger capacitor directly connects to a second extension-conductor segment of Muh's inductor through one or more vias.



Niknejad (EX-1007) at Fig. 3.11 left half rotated view (left); Muh (EX-1006) at Fig. B-3 partial view (right) (annotations added in red and green).

240. This arrangement is the simplest and most reliable design choice. For example, as shown in Niknejad's Fig. 3.11, the finger capacitor is able to connect to other electronic components (such as an inductor) from one side of the finger capacitor (e.g., the right side, where the red/green arrows are, as illustrated in Fig. 3.11 above). Now suppose the finger capacitor were oriented differently with respect to Muh's inductor (e.g., being rotated by 90 degrees so that its connecting segments extend perpendicular to, rather than in the same direction as, the extension-conductor segments of Muh's inductor), as illustrated below. In that case, extra horizontal metal traces would be needed in the lower metal layers to connect the finger capacitor to the overlaying inductor. For instance, horizontal metal trace is needed to connect the second connecting segment of the finger capacitor (located on the left-hand side) to the second extension-conductor segment of the inductor (located on the right-hand side). Such extra metal traces not only increase fabrication costs but also involves additional fabrication processes which create more chances for issues and failures.



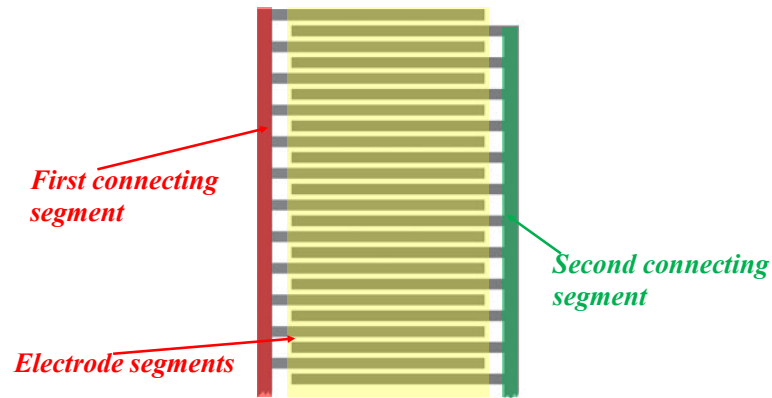
Niknejad (EX-1007) at Fig. 3.11 left half rotated view (left); Muh (EX-1006) at Fig. B-3 partial view (right) (annotations added in red and green).

241. Notably, according to Niknejad, finger capacitors are “sometimes referred to as ‘MOM’ (metal-oxide-metal) capacitors.” The connecting segment structures of MOM capacitors were not new. Indeed, the ’582 Patent itself discloses MOM capacitors and acknowledges their internal structures were “well known in the field.” ’582 Patent (EX-1001) at 12:11-16.

1.9 a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

242. Niknejad discloses everything in this limitation except for the “located below the first region” part which is obvious over the combination of Muh and Niknejad. For example, Niknejad discloses that “[f]inger capacitors are composed

of a large number of parallel fingers connected to either port of the device as shown in Fig. 3.11,” which is reproduced below. Niknejad (EX-1007) at 27.



Niknejad (EX-1007) at Fig. 3.11 left half (annotations added in color).

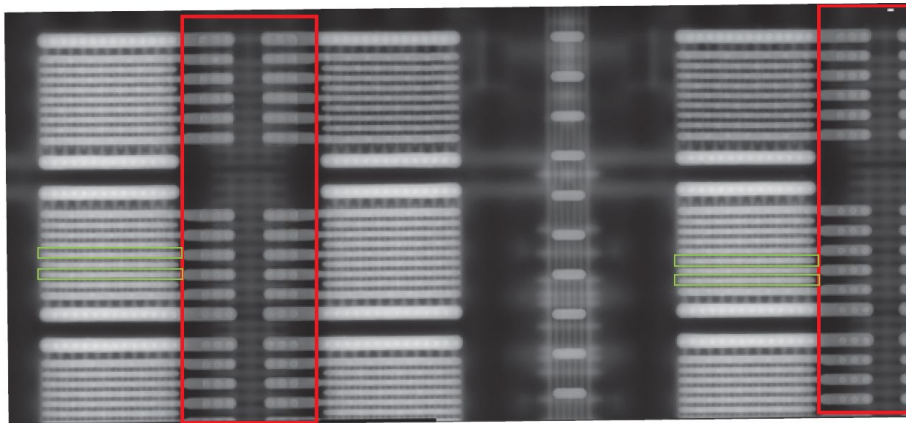
243. In Niknejad’s finger capacitor, each parallel finger includes an electrode segment. For example, as I explained above in Invalidity Ground 1, one set of fingers is connected to a first connecting segment on the left, while the other set of fingers is connected to a second connecting segment on the right. The first and second sets of electrode segments are separated by a gap. The capacitance increases as the width of the gaps are decreased. *See, e.g.*, Agilent Technologies (EX-1020) at 2-4; Niknejad (EX-1007) at 28 (“In order to realize a given capacitance, either a large number of short fingers in parallel or a small number of long fingers can be used.”).

244. As plainly visible from Niknejad’s Fig. 3.11(illustrated above), in the finger capacitor, one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments. Further, each of the plurality of

electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

245. Niknejad does not expressly disclose its finger capacitor is located below the first region as claimed. However, when Niknejad's finger capacitor is implemented into Muh's LC tank, as I explained earlier, the electrode segments of the finger capacitor would be located below the claimed first region based on how Realtek interprets "the first region."

246. The disclosures of Muh and Niknejad are consistent with how Realtek interprets this limitation, as shown below, where Realtek marks the plurality of electrode segments in green boxes and the plurality of connecting segments in red boxes.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 18 (Realtek annotations retained).

247. The disclosures of Muh and Niknejad are also consistent with the '582 Patent itself. The electrode segment structures of finger capacitors (i.e., MOM

capacitors) were not new. Indeed, the '582 Patent discloses MOM capacitors and acknowledges their internal structures were “well known in the field.” '582 Patent (EX-1001) at 12:11-16.

248. In summary, as I explained above, Muh in combination with Niknejad, renders claim 1 obvious.

1. Motivations to Combine Muh and Niknejad

249. Before the time of the '582 filing, a POSITA would have been motivated to implement Niknejad's finger capacitor into Muh's LC resonant circuit for a multitude of reasons. As Muh points out, “[i]n the test chip, the capacitor is implemented as an *interdigitated finger capacitor*, with each finger *comprising the bottom five metal layers strapped together*.” Muh (EX-1006) at 57 (emphasis added). Similarly, as I previously discussed, Niknejad discloses that each finger of such a design consists of all *available metal layers stacked* on top of each other, consistent with the disclosure in Muh. The Niknejad capacitor is therefore the same type of capacitor design as taught by Muh.

250. A POSITA would also have understood that fabricating such finger capacitors in a circuit like Muh's was straightforward to achieve. For instance, a POSITA would know that finger capacitors “*can be easily fabricated in any modern CMOS process* due to the abundance and high packing density of the metal layers.” Niknejad (EX-1007) at 27. A POSITA would have therefore had a

reasonable expectation of success in substituting the Niknejad finger capacitor component in Muh's circuit.

251. As I noted earlier in the introduction of this Ground, Professor Ali M. Niknejad (author of Niknejad) was Matthew Muh's (author of the Muh reference) Research Advisor who directly supervised Matthew Muh in the design of Muh's LC resonant circuit. Muh (EX-1006) at 1. A POSITA viewing Muh would naturally be motivated to review other publications by Professor Ali M. Niknejad covering similar, related subject matter. Indeed, Niknejad articulates that "[r]esearch in silicon mm-wave circuits and technology started at universities and research institutions and now continues in the commercial realm. Many of the researchers in the field have contributed to this book to chronicle these efforts." Niknejad (EX-1007) at 6. As Niknejad explains:

This book is written for practicing RF and analog circuit designers who wish to join this exciting and growing field. The chapters are self-contained and include a short tutorial on important concepts before delving into details. The audience for this book is assumed to be experienced in the field of analog/RF integrated circuits. The focus of each chapter is the key innovations and techniques that enable operation at mm-wave frequencies, which is close to the activity limits of silicon technology.

Id.

252. A POSITA would have readily understood there were clear benefits of using such a finger capacitor structure. In addition to the benefits I discussed above, Niknejad discloses that finger capacitors (i.e., MOM capacitors) "are less

expensive than Metal-Insulator-Metal (MIM) capacitors, which employ a sandwich structure with a thin high-K dielectric.” Niknejad (EX-1007) at 28. A POSITA would have understood the parallel-plate capacitor used in Muh’s simulation model is a type of MIM capacitor, as it employs a sandwich structure with a thin high-K dielectric. Muh (EX-1006) at 57 (“To obtain a similar value of capacitance as the finger capacitor, a high-k dielectric was sandwiched between the two plates.”); *see also* Niknejad (EX-1007) at 26, Fig. 3.10 (showing an LC tank “formed by a ring inductor and MIM capacitors,” which is similar to Muh’s Fig. B-3). Therefore, as taught by Niknejad, replacing Muh’s MIM capacitor with Niknejad’s MOM capacitor would yield potential cost saving. A POSITA would have therefore been motivated to substitute Niknejad’s capacitor in Muh’s circuit, and would have expected success in doing so.

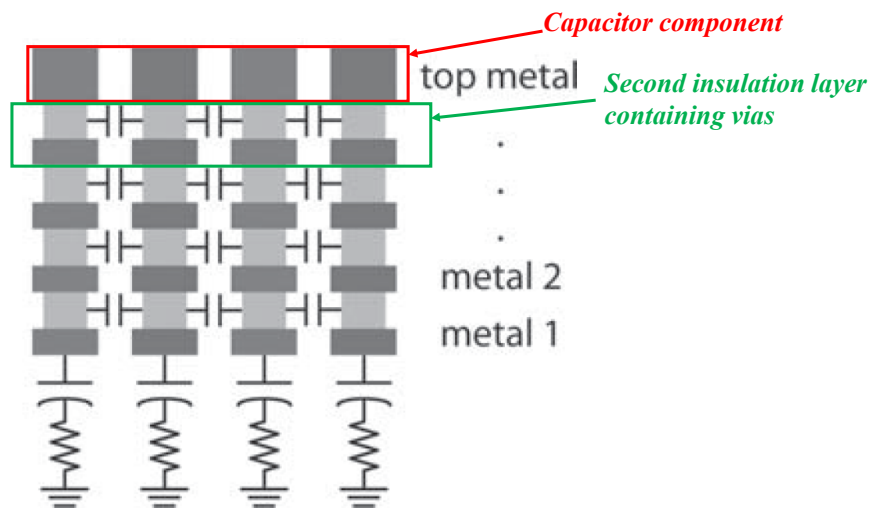
D. Muh Invalidates Claims 2-5 and 9

Claim 2

2.1 The semiconductor device with an LC resonant circuit according to claim 1, further comprising: a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

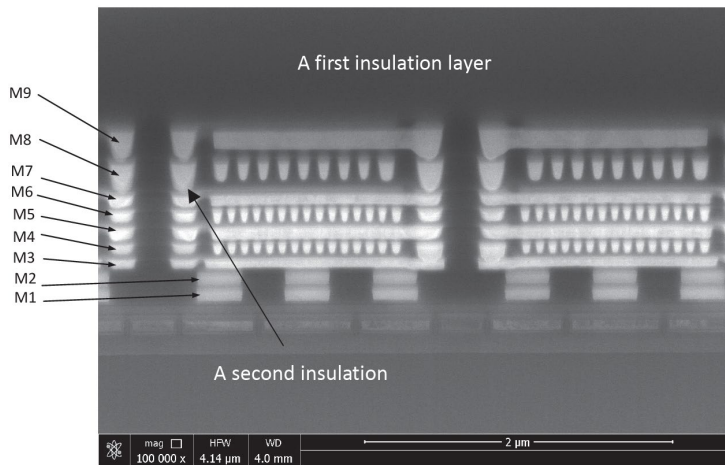
253. Niknejad discloses this claim limitation. For example, in Niknejad’s multi-layer finger capacitor, “[e]ach finger consists of all available metal layers

stacked on top of each other in order to decrease its resistance whi[le] increasing both its quality factor and the self-resonance frequency. The metal layers are connected together through *the maximum number of vias* possible in order to take advantage of the additional via-to-via capacitance.” Niknejad (EX-1007) at 27 (emphasis added). A POSITA would have understood that the vias would be implemented in and surrounded by an insulation layer. Specifically, the finger capacitor shown in Niknejad’s Fig. 3.11 would include a second insulation layer (e.g., between the top metal layer and a lower metal layer), as illustrated below. The second insulation layer would contain and surround the vias between metal layers of the finger capacitor. The capacitor component located on the top metal layer would be sandwiched between the first insulation layer (not shown below) and the second insulation layer.



Niknejad (EX-1007) at Fig. 3.11 right half (annotations added in color).

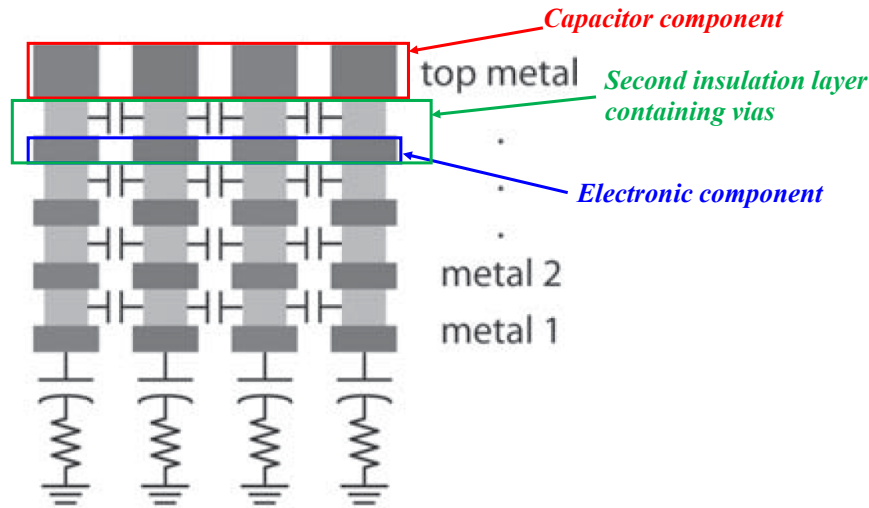
254. This interpretation is consistent with how Realtek interprets the second insulation layer, as shown below.



Realtek Exhibit 32 to ITC Complaint (EX-1034) at 19 (Realtek annotations retained).

2.3 an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

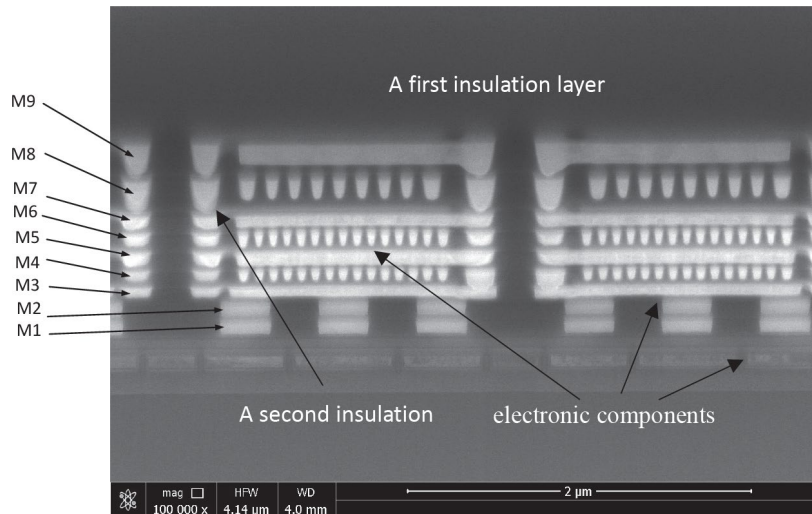
255. Niknejad renders this claim limitation obvious. For example, Niknejad's multi-layer finger capacitor includes an electronic component (e.g., one of the fingers of the capacitor) on the second-topmost metal layer, as illustrated in Fig. 3.11 (reproduced below). Niknejad (EX-1007) at 27. The electronic component on the second-topmost metal layer is arranged on a surface, opposite to the capacitor component (i.e., in top metal layer), of the second insulation layer.



Niknejad (EX-1007) at Fig. 3.11 right half (annotations added in color).

256. Niknejad does not expressly disclose an electronic component of its finger capacitor being arranged corresponding to the first region. However, when Niknejad's finger capacitor is implemented into Muh's LC tank, as I explained earlier, the electronic component of its finger capacitor would be located below the claimed first region based on how Realtek interprets "the first region." Similarly, as I explained earlier with respect to claim 1, it would have been obvious to a POSITA to arrange the electronic component in an embedded manner on a surface of the second insulation layer.

257. This is also how Realtek interprets the claim language, as depicted below.



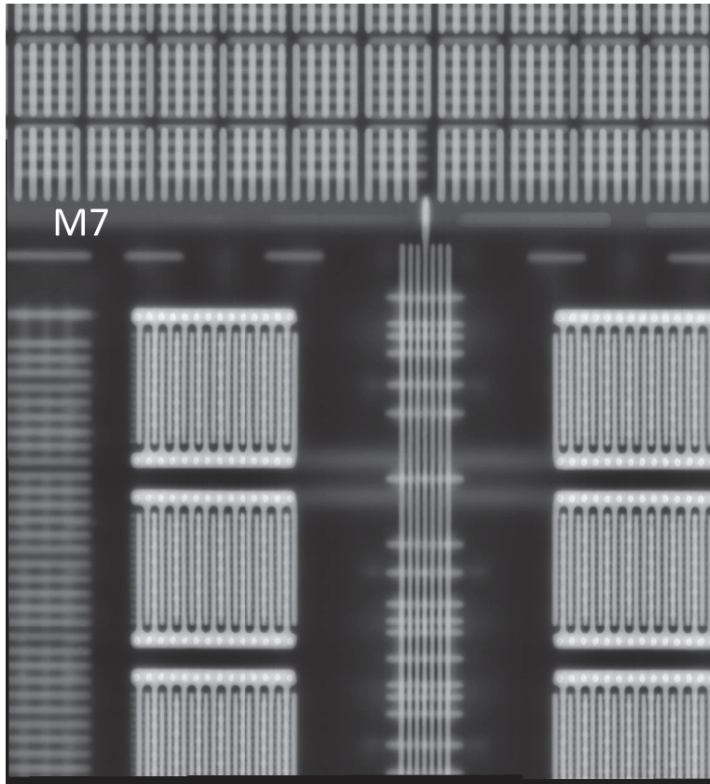
Realtek Exhibit 32 to ITC Complaint (EX-1034) at 19 (Realtek annotations retained).

Claim 3

The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

258. Niknejad discloses this claim. For example, Niknejad's multi-layer finger capacitor includes an electronic component (e.g., on the second-topmost metal layer), as illustrated in Fig. 3.11 above for limitation 2.1. Niknejad (EX-1007) at 27. The electronic component on the second-topmost metal layer is at least a capacitor component, since it is part of the multi-layer finger capacitor.

259. This is also how Realtek interprets the claim language, as depicted in the text and accompanying image below.



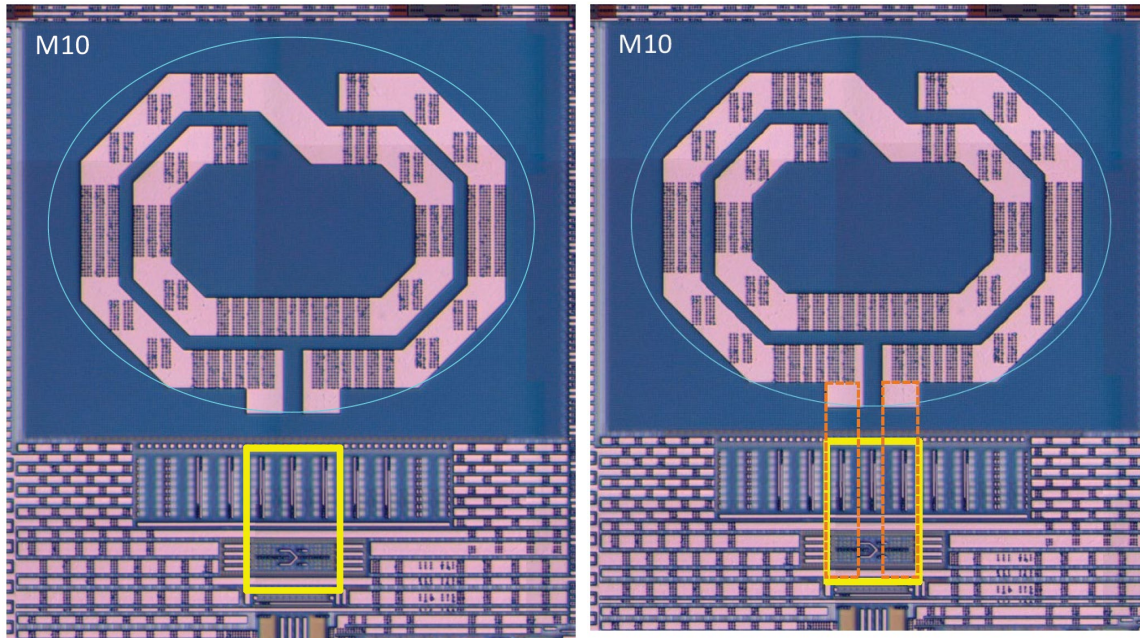
(Depicting a capacitor)

Realtek Exhibit 32 to ITC Complaint (EX-1034) at 20 (Realtek annotations retained).

Claim 4

The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

260. Notably, Realtek interprets the first region of claim 4 as having the same scope as the first region of claim 1, as shown below.



Realtek Exhibit 32 (EX-1034) at 12 (left); *Id.* at 21 (right) (Realtek annotations retained).

261. Muh discloses this claim. For example, since Realtek interprets the first region of claim 4 as having the same scope as the first region of claim 1, Muh discloses claim 4 to the same extent it discloses claim 1.

Claim 5

The semiconductor device with an LC resonant circuit according to claim 4, wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment.

262. The only difference between claim 5 and claim 4 is that claim 5 recites an additional limitation: “the first region is defined between the coil-conductor segment.”

263. Muh alone, or in combination with Niknejad, discloses this claim. That is, to the extent the first region is defined between the two extension-

conductor segments and the coil-conductor segment, the inductor and capacitor components disclosed by Muh and Niknejad still meet such a definition of “the first region.” For example, Niknejad’s finger capacitor, which is or includes a capacitor component, when adopted into Muh’s LC resonant circuit would still be arranged corresponding to the first region, and a plurality of electrode segments in this finger capacitor would still be located below the first region. *See supra* ¶¶ 221-227, 245.

Claim 9

A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component further comprises:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

264. Based on my review, independent claim 9 is the same as claim 1 except that it is broader as it does not have the following limitation of claim 1: “wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.”

265. Therefore, for at least the reasons provided above for claim 1, Muh in combination with Niknejad renders claim 9 obvious.

VIII. JURAT

266. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 8th day of April, 2023 in Princeton, New Jersey.

A handwritten signature in black ink, reading "Paul Prucnal". The signature is written in a cursive style with a large initial "P" and a long, sweeping underline.

Dr. Paul R. Prucnal