Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO

by Matthew Muh

Research Project

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Approval for the Report and Comprehensive Examination:

Committee:

Professor Ali M. Niknejad
Research Advisor

(Date)

* * * * * * *

Professor Tsu-Jae King
Second Reader

(Date)

Table of Contents

1 Introduction....6
2 Application of FinFET technology to high-frequency circuit design....8
2.1 Introduction to FinFET technology and applications....8
2.2 High-frequency transistor performance and design....10
2.3 Small-signal transistor modeling....12
2.4 Design of static frequency divider and other test structures....15
2.4.1 Process information and FinFET orientation....15
2.4.2 Individual transistors....16
2.4.3 Static frequency divider....18
2.4.3.1 Topology....18
2.4.3.2 Estimated performance....20
2.4.3.3 Layout....21
3 Millimeter-wave push-push CMOS VCO design....24
3.1 Push-push oscillator fundamentals....24
3.2 Motivations for using push-push oscillators....25
3.3 Architectural considerations....25
3.4 Dependence of resonator Q on frequency of operation....29
3.5 Negative resistance generation and balanced VCO construction....34
3.6 Design of proposed push-push CMOS VCO....35
3.7 Center-tapped inductor design and modeling....41
3.8 Transmission-line inductor design....46
3.9 Simulation results....47
3.9.1 Effect of L_{shunt} on VCO performance....47
3.9.2 Effect of L_{shunt} (with improved output power)....48
3.10 VCO and L-C tank layout....50
4 Conclusion....53
Appendix A —Description of FinFET test structures....55
Appendix B —Comparison of HFSS results to measured data....56
References....59

List of Figures

Figure 2-1. Simplified schematic diagram of FinFET. 8
Figure 2-2. Layout of multi-finger bulk-CMOS transistor (left) and FinFET (right) 11
Figure 2-3. Gain plots for n-channel FinFET (W/L = 1 μm/0.06 μm). 12
Figure 2-4. Small-signal transistor model. 14
Figure 2-5. Simulated results vs. extracted small-signal model (dots: simulation, solid line: extracted model). 15
Figure 2-6. Layout of NMOS FinFETs with different orientations and gate finger lengths 17
Figure 2-7. Open, short, and thru de-embedding structures. 18
Figure 2-8. Static frequency divider block diagram. 19
Figure 2-9. Simplified circuit schematic of CML static frequency divider with output buffer. 20
Figure 2-10. Simulated clock and output waveforms of frequency divider. 21
Figure 2-11. Layout of an unrotated two-metal layer version of the frequency divider. 22
Figure 2-12. Layout of a rotated single-metal version of the frequency divider. 23
Figure 3-1. Push-push oscillator utilizing a differential oscillator. 24
Figure 3-2. Various 60-GHz LO generation methods in a direct-conversion radio architecture. 26
Figure 3-3. Various 60-GHz LO generation methods in a dual-conversion radio architecture. 29
Figure 3-4. L-C tank impedance for various resonant frequencies (lower frequency range). 32
Figure 3-5. L-C tank impedance for various resonant frequencies (higher frequency range). 33
Figure 3-6. Negative-resistance generator and associated balanced VCO topology. 35
Figure 3-7. Basic schematic of proposed push-push VCO. 36
Figure 3-8. Differential (odd-mode) input impedance (L_{shunt} = 130 pH). 37
Figure 3-9. R_p vs. L_{shunt} at 30 GHz (using an ideal inductor). 38
Figure 3-10. Capacitance of varactors (two connected in series) vs. V_{tune}, with V_{bias} = 0.75 V. 39
Figure 3-11. HFSS models of L_{tank}. Without substrate contact (left). With contact (right). 41
Figure 3-12. HFSS simulation results for center-tapped inductor L_{tank}. 44
Figure 3-13. Schematic of multi-π model of center-tapped inductor L_{tank}. 45
Figure 3-14. HFSS vs. model comparison of center-tapped inductor L_{tank}. 45
Figure 3-15. HFSS model of coplanar transmission line inductor. 46
Figure 3-16. Simulated performance of VCO without L_{shunt} 47
Figure 3-17. Simulated performance of VCO with L_{shunt}. 48
Figure 3-18. Simulated VCO performance with L_{shunt} (with improved output power). 49
Figure 3-19. Simulated VCO phase noise relative to 2nd harmonic. 49
Figure 3-20. Simulated VCO performance without L_{shunt} (with improved output power). 50
Figure 3-21. Proposed layout of push-push VCO. 52
Figure 3-22. Layout of L-C tank structures. 52
Figure B-1. HFSS model of loop inductor on test chip. 56
Figure B-2. Comparison of measured and simulated results for test-chip inductor. 57
Figure B-3. HFSS model of parallel resonant tank on test chip. 58
Figure B-4. Comparison of measured and simulated impedance of resonant tank. 58

List of Tables

Table 2-1. Extracted small-signal model parameters.....14
Table 3-1. Rough estimates of CMOS power consumption for various LO generation schemes.28
Table 3-2. Q-factor of various L-C tanks (lower frequency range).....34
Table 3-3. Q-factor of various L-C tanks (higher frequency range).....34

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 5 of 61

1 Introduction

The downscaling of CMOS technology over the past several decades has resulted in continual improvements in integrated-circuit performance and cost per function. However, the scaling of conventional CMOS devices significantly beyond the 90-nm technology node will be challenging, due to limitations such as subthreshold leakage and gate-dielectric leakage. To overcome some of the problems associated with planar CMOS device scaling, advanced MOSFET structures such as the ultrathin-body SOI single-gate transistor and the double-gate transistor have been explored. These structures enable more aggressive device scaling because of their ability to control short-channel effects more effectively. Compared to a single-gate ultrathin-body device, the double-gate device is more electrostatically robust because two gates are used to control the channel, thus allowing for additional gate length scaling.[1] Although double-gate transistors have been studied for quite some time, their adoption has been hindered by the complexity of their fabrication process. Recently, however, a more practical double-gate structure, the FinFET, was developed, with a process flow similar to that of conventional SOI CMOS processes.[2] A number of functional FinFET digital circuits have been reported, and physical design conversion of planar CMOS circuits to FinFET technology has been demonstrated.[3]

The improvement in circuit performance from continued device scaling applies to RF circuits as well as digital circuits. The improved RF performance of CMOS devices has enabled CMOS to become a viable option for commercial RF applications such as wireless LAN, GSM cellular transceivers, and GPS receivers. Recently, 7 GHz of unlicensed bandwidth around 60 GHz was made available, opening the door for applications such as Gb/s point-to-point links, short-range

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 6 of 61

high data-rate wireless personal area networks, and vehicular radar.[4] Technology scaling has enabled CMOS devices to operate at these high frequencies, and numerous millimeter-wave CMOS circuits have been reported in the literature. Compared to the traditional III-V semiconductor technologies used for monolithic microwave integrated circuits, CMOS implementations promise higher levels of integration and reduced cost,[4] and thus may begin to make inroads into the compound semiconductor-dominated market in the foreseeable future. Future CMOS implementations of millimeter-wave integrated circuits may potentially utilize advanced, highly scalable structures such as the FinFET to take advantage of their increased speed.

To facilitate an initial evaluation of the RF capability of FinFET technology, a 2:1 static frequency divider has been designed using FinFETs, as documented in the second section of this report. In addition to the frequency divider, individual FinFETs have been designed to enable DC and high-frequency S-parameter transistor measurements and to evaluate the effect of layout variations on FinFET performance. The third section of this report documents the design of a CMOS push-push VCO for millimeter-wave applications. Using a balanced architecture, the push-push VCO is designed to operate at a fundamental frequency of 30 GHz while generating a single-ended second-harmonic output at 60 GHz. The VCO is estimated to deliver –3 dBm of output power at 60 GHz into a 50-Ω load while consuming about 20 mA of DC current from a 1.2-V supply.

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ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 7 of 61

2 Application of FinFET technology to high-frequency circuit design

2.1 Introduction to FinFET technology and applications

The FinFET is a double-gate transistor in which the gate straddles a thin, vertical fin-shaped body, creating two channels along the sidewalls of the fin (Fig. 2-1). Using two gates and a thin body helps to control short-channel effects, thereby enabling gate-length scaling deep into the nanometer regime without the use of channel dopants. Although it may be possible to scale the traditional bulk MOSFET into the 10-nm gate length regime, this will probably require heavy channel doping to mitigate short channel effects. This not only presents a challenge in terms of device fabrication, but will probably also result in the degradation of device performance.[1]

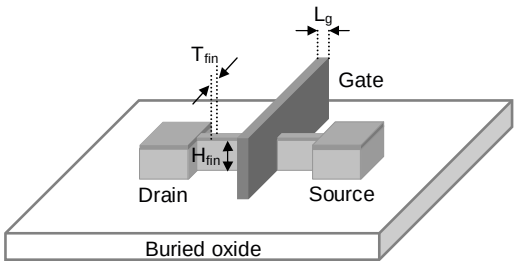


Figure 2-1. Simplified schematic diagram of FinFET.

The ability of double-gate devices to more effectively control short-channel effects and thereby limit the leakage current makes them particularly attractive for low-power digital applications. With a lightly doped channel, double-gate devices have a steep subthreshold slope, which translates to a lower threshold voltage for a given off-state leakage current specification, thus increasing the on-state drive current. In terms of fabricated FinFETs, promising results have

been reported in the literature. For example, symmetric double-gate (SDG) FinFETs with raised source/drain were fabricated with the highest drive current reported for double-gate NMOS and PMOS devices; this current was also competitive with (then) state-of-the-art bulk silicon and SOI technologies.[5] A comparison of reported conventional FETs and FinFETs showed that high-performance FinFETs already met or exceeded the best conventional FET performance for a given gate length, in terms of CV/I delay, despite the youth of this technology.[6]

A number of functional digital FinFET circuits have been reported in the literature, including a four-stage inverter chain,[7] a six-transistor SRAM cell,[8] and a 41-stage ring oscillator.[9] To date, there has not yet been much published work on FinFETs for analog/RF applications. However, the first detailed experimental investigation of the analog performance of FinFETs was recently published, in which the authors reported very high values of the Early voltage and hence, of intrinsic gain.[10] While this is promising for analog applications, the authors also observed that drive currents and transconductance were lagging behind the best planar devices. They believe that performance can be improved by improving the mobility in the side channels and/or increasing the fin density.

The primary aim of this present research is to investigate the suitability of FinFETs for RF applications. To this end, a number of test structures have been designed in order to enable an initial evaluation of the high-frequency performance of FinFETs. Specifically, a static frequency divider has been designed to benchmark the potential speed of FinFET technology in a circuit application. In addition, individual test transistors have been designed for S-parameter measurements, which will facilitate high-frequency transistor characterization and modeling in the future.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 9 of 61

2.2 High-frequency transistor performance and design

An important figure of merit for the high-frequency capability of a technology is the maximum frequency of oscillation (f_{MAX}). The f_{MAX} of a transistor can be determined by finding the frequency at which Mason's unilateral power gain (U) or the maximum available power gain (MAG) is equal to unity. Although f_{MAX} is related to the unity current gain frequency (f_T) of the device, it is also highly dependent on the resistive losses of the device, including the gate resistance, series source/drain resistances, non-quasi-static channel resistance, and the resistive substrate network.[4] Thus, while f_T can be increased simply by scaling down the device, f_{MAX} may not exhibit a corresponding improvement unless the influence of parasitics is appropriately minimized.

To reduce the gate resistance of a conventional CMOS transistor, the width of each finger in a multi-finger transistor should be made very narrow. Although the gate finger width affects the gate resistance and hence f_{MAX}, it has been observed that f_{MAX} is independent of the actual number of fingers of the transistor.[11] The layouts of a representative bulk-CMOS transistor and a FinFET are compared in Fig. 2-2. It can be seen that the FinFET can utilize a similar multi-finger layout to reduce the width of each gate finger and thereby reduce the overall gate resistance. The gate resistance can also be reduced by using a material with a lower resistivity than polysilicon. This approach lends itself nicely to FinFETs, since gate work function engineering using alternative gate materials can be used to achieve threshold voltage adjustments when the body is undoped. For example, a molybdenum gate technology has recently been developed for FinFET technology.[12]

One of the technological challenges facing FinFETs is the high parasitic source/drain series resistance arising in part from the thin fin extension between the gate edge and the source/drain

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 10 of 61

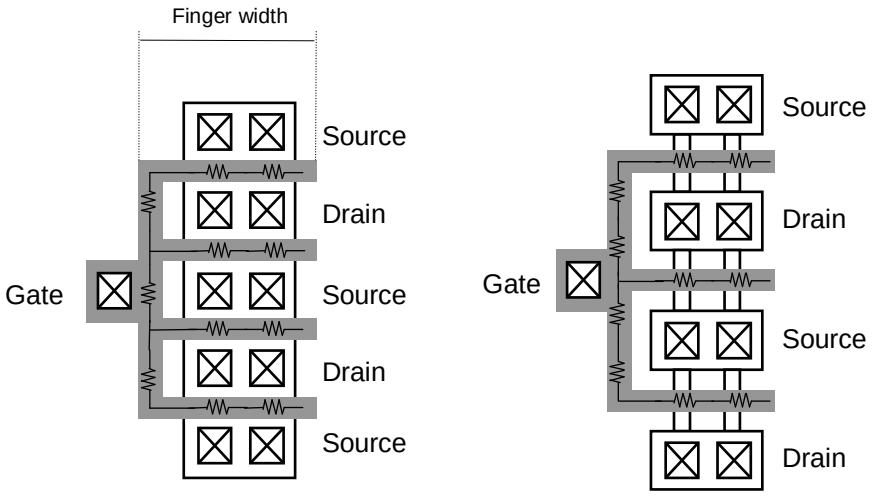


Figure 2-2. Layout of multi-finger bulk-CMOS transistor (left) and FinFET (right).

pads. This reduces not only the drive current but also f_{MAX} of the device. Different methods—angled extension implants and selective silicon epitaxy—have been investigated to minimize this parasitic resistance in FinFETs.[13]

Various definitions of gain for an n-channel FinFET are plotted in Fig. 2-3. The plots are based on a simple BSIM3SOI transistor model adapted from a preliminary BSIM3SOI SPICE model developed at SPAWAR.[14] No AC data was available at the time this version of the model was developed, so the capacitance parameters are estimated, but not calibrated. H_{21} is the current gain and MSG is the maximum stable gain. The effective width of the device is 1 μm, the gate length is 60 nm, and the bias conditions are I_d/W = 165 μA/μm and V_{ds} = 1.2 V. As the plot shows, the value of f_{MAX} is roughly 100 GHz, which is much lower than one would expect for a typical sub-100-nm device with comparable biasing. For example, the f_{MAX} of a properly laid-out and biased NMOS transistor in a standard 130-nm CMOS technology can easily exceed 100 GHz,[4] while the f_{MAX} of an NMOS device in a 90-nm SOI CMOS technology can exceed 200

GHz.[15] The low f_{MAX} of the FinFET is perhaps due in part to high parasitic source/drain resistance and suboptimal RF layout. In addition, it should be noted that the model does not incorporate gate resistance or the effect of various other parasitics, so the actual value of f_{MAX} may be even lower. A more accurate high-frequency model, based on measured C-V or S-parameter data and perhaps utilizing a double-gate SOI transistor model, would yield more accurate results.

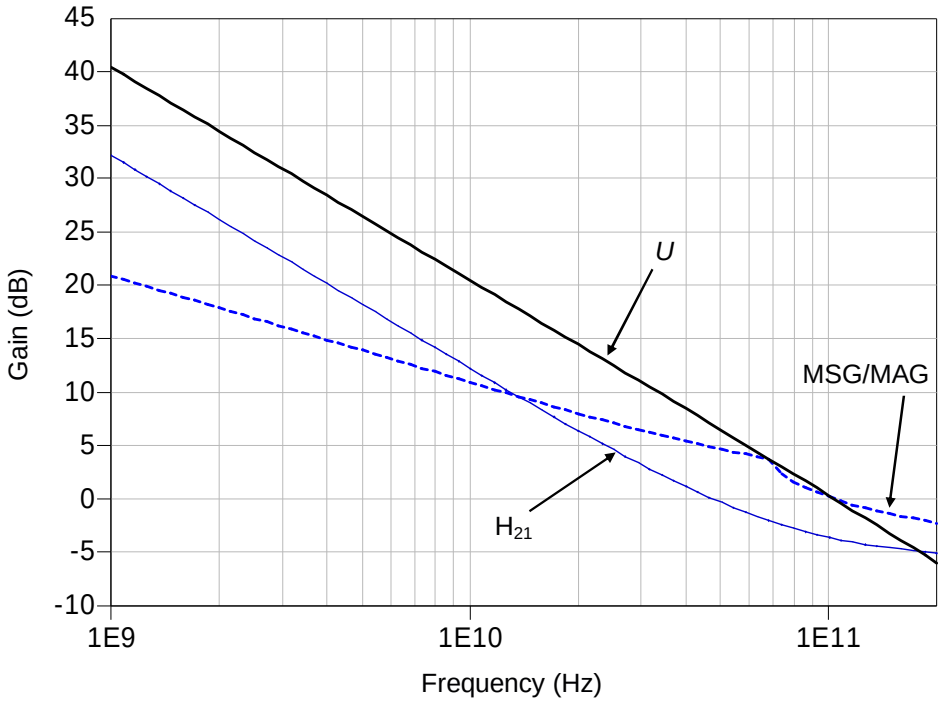


Figure 2-3. Gain plots for n-channel FinFET (W/L = 1 µm/0.06 µm).

2.3 Small-signal transistor modeling

A simple small-signal transistor model of a FinFET based on results from device-level simulations has been developed. A lumped-element small-signal model is useful because of its simplicity and relatively high accuracy, although numerous RF circuits, such as mixers and VCOs, require an accurate large-signal model. A small-signal model is further limited by its

dependence on bias conditions and the specific region of a transistor's operation. Although the model presented here was not used in designing the frequency divider described later, it nonetheless sketches how a basic small-signal model could be developed from measured data.

A simple lumped-element, small-signal equivalent MOSFET model is shown in Fig. 2-4. It includes both the intrinsic transistor and parasitic series resistors. Based on this model, a simple technique is used to extract the model parameters. This technique was developed to extract a high frequency model based only on S-parameter measurements and is described in a paper by Lovelace *et al.*[16] The model shown here is the same as that presented in the aforementioned reference, except that it does not include the additional time-constant factor associated with g_m. Instead of using measured data, a sample FinFET (adapted from a model provided by Hei Kam) was simulated using a 3-D device simulator, resulting in a set of two-port matrix parameters. The FinFET has an effective width of 0.1 μm and a gate length of 65 nm, and was biased at V_{GS} = 1.5 V and V_{DS} = 1 V. The extraction technique is summarized as follows, omitting the mathematical details:

- Initially bias the device at $V_{GS} = V_{DS} = 0$ V and use the resulting zero-bias Z-parameters to extract the parasitic resistances r_g, r_d, and r_s.
- Select the desired bias condition and calculate the resulting Z-parameter network (**Z**).
- Compute the Z-parameter network of the intrinsic model (**Z'**) by subtracting the appropriate parasitic resistances from **Z**.
- Convert **Z'** to the equivalent Y-parameter network (**Y'**).
- From **Y'**, calculate the parameters of the intrinsic small-signal model—C_{gd}, C_{gs}, C_{ds}, r_{ds}, and g_m.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 13 of 61

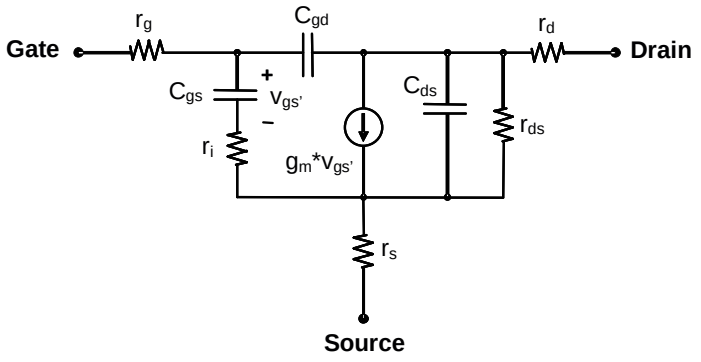


Figure 2-4. Small-signal transistor model.

Parameter	Value	Parameter	Value
r_g	80 Ω	C_{gs}	104 aF
r_d	210 Ω	C_{gd}	22 aF
r_s	160 Ω	C_{ds}	2 aF
r_i	1 kΩ	g_m	160 μS
r_{ds}	140 kΩ		

Table 2-1. Extracted small-signal model parameters.

Using this extraction routine, the small-signal model parameters of the FinFET were obtained (see Table 2-1), and the resulting model was compared to the simulated results, as shown in Fig. 2-5. Except for Y21 at very high frequencies, the plots show very good agreement, which is expected since the FinFET is modeled by a simple, well-behaved structure in the device simulator and various layout parasitics are not included. In practice, the small-signal model must take into account all the relevant layout parasitics, which require additional elements to model. A more sophisticated small-signal model and extraction scheme can be utilized for a better fit, such as the SOI MOSFET model and extraction method presented in the paper by Raskin *et al.*,[17] which take into account the effect of parasitic inductances.

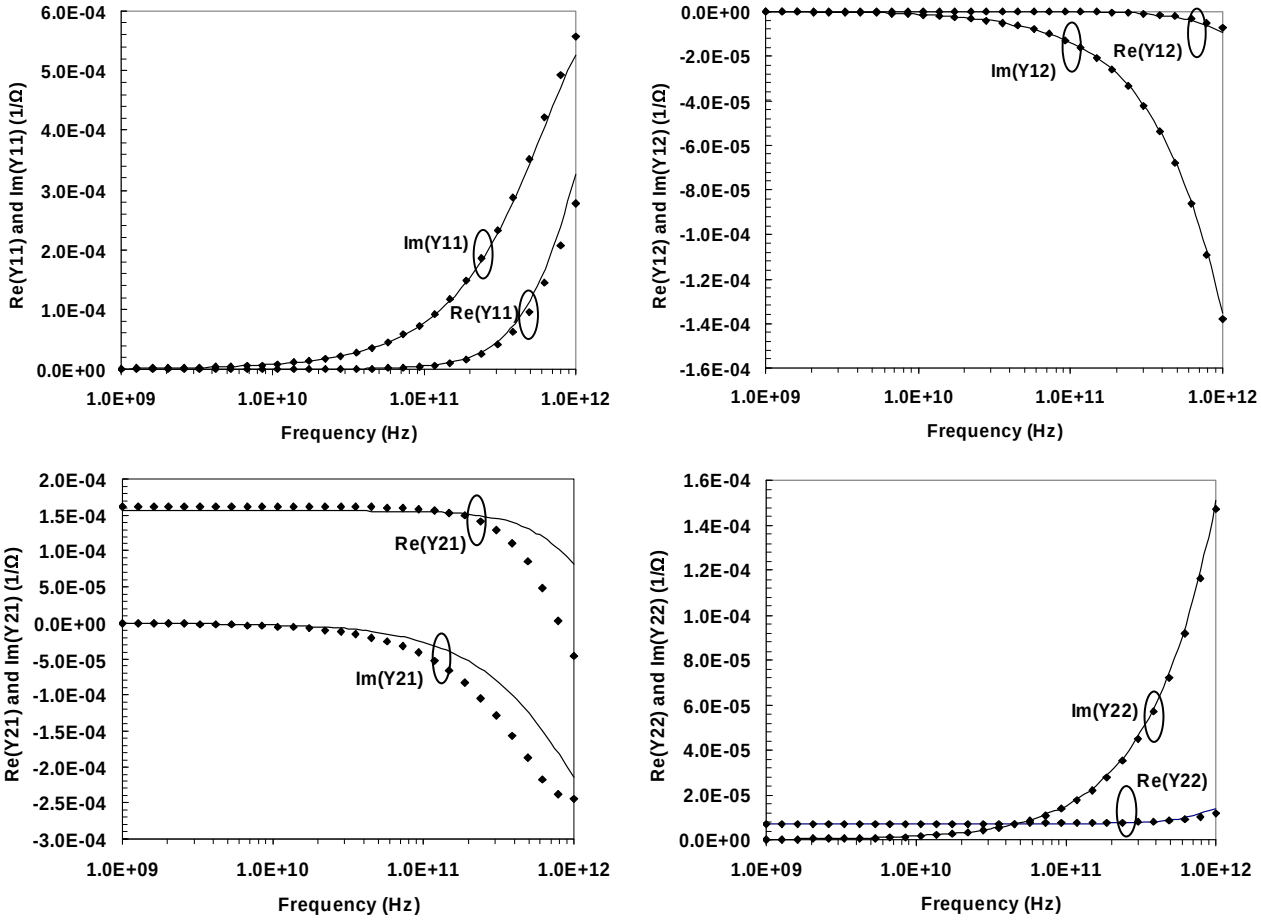


Figure 2-5. Simulated results vs. extracted small-signal model (dots: simulation, solid line: extracted model).

2.4 Design of static frequency divider and other test structures

2.4.1 Process information and FinFET orientation

The test structures are to be fabricated on SOI wafers with a targeted fin height, H_{fin}, of 50 nm. The effective width of a single-fin device is 100 nm (twice the fin height due to the two channels). The gate oxide is expected to be about 20 Å thick. The minimum gate length is 35 nm, and the fin thickness is targeted to be about 20 nm. This process incorporates a molybdenum gate

technology to adjust the gate work function. Up to two metal layers are allowed, although some layouts were routed with only one metal layer to ease fabrication requirements.

In a standard <100> wafer, the FinFET channel is oriented in the <110> plane. Although this orientation is good for PMOS devices due to high hole mobility in the <110> plane, NMOS devices should be oriented at a 45° angle to take advantage of higher electron mobility in the <100> plane. Because the FinFET is a vertical device structure, different surface orientations can be achieved by simply rotating the layout in the plane of the wafer, without the use of non-standard wafer substrates.[18] Since the frequency dividers designed in this work utilize only NMOS devices, a number of layouts are rotated by 45° to evaluate NMOS FinFET performance enhancement due to improved electron mobility.

2.4.2 Individual transistors

A set of individual transistors with corresponding de-embedding structures has been designed. This set comprises NMOS FinFETs with different gate finger lengths, layout configurations, channel lengths, and orientations. The layouts of two of these transistors are shown in Fig. 2-6. Both devices have 600 fins, which is equivalent to a total width of 600 × 100 nm = 60 μm, and a targeted gate length of 50 nm. The transistor on the top is oriented horizontally with each doubly-contacted gate finger running across three fins. The transistor on the bottom is oriented vertically with each gate finger running across six fins. The use of ground-signal-ground pads and coplanar waveguides leading to the transistor facilitates high-frequency S-parameter characterization. A set of open, short, and thru de-embedding structures is shown in Fig. 2-7.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 16 of 61

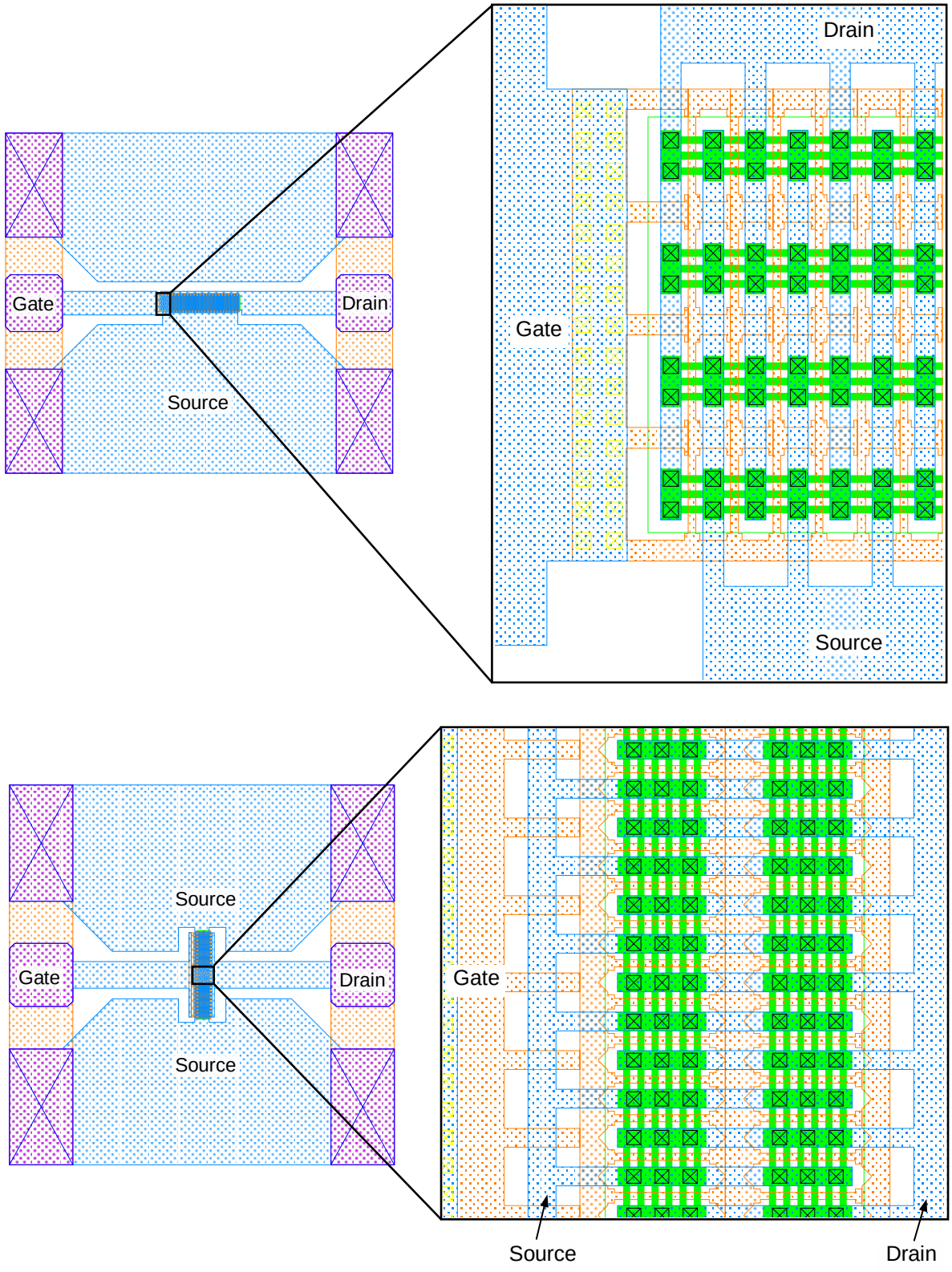


Figure 2-6. Layout of NMOS FinFETs with different orientations and gate finger lengths.

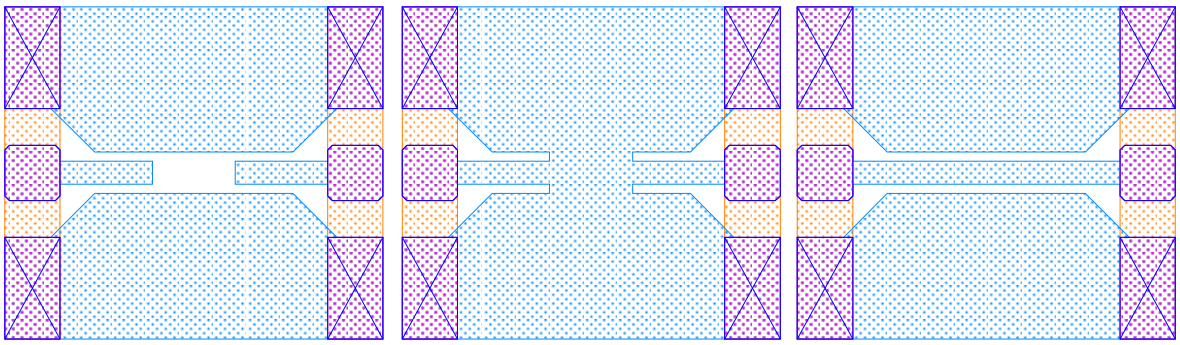


Figure 2-7. Open, short, and thru de-embedding structures.

2.4.3 Static frequency divider

2.4.3.1 Topology

A static frequency divider has been designed in order to evaluate the high-frequency capability of FinFET-based circuits. A frequency divider is an integral component of frequency synthesizers used in communication systems and also serves as a benchmark for high-speed technologies. As shown in Fig. 2-8, a static frequency divider can be implemented with two D-latches in a master-slave configuration. The inverted slave outputs are connected to the master inputs to perform a divide-by-two function on the clock signal. This circuit is a suitable test vehicle because it is fairly robust in the presence of process variations and is able to operate at a maximum frequency that is related to the intrinsic speed of the technology.

As shown in Fig. 2-9, each latch is implemented with a conventional current-mode logic (CML) architecture. Compared to conventional static CMOS logic, CML reduces the internal voltage swing, making it particularly suitable for high-speed operation.[19] To maximize the speed of the circuit, only NMOS devices are used. Due to the lack of well-controlled resistors

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 18 of 61

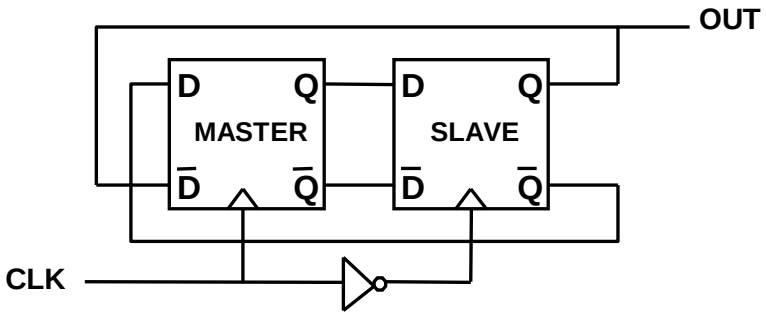


Figure 2-8. Static frequency divider block diagram.

in the process, diode-connected NMOS devices are used as active loads, although PMOS devices could also have been used. Instead of generating complementary clock signals for the two latches, a single clock signal is used in a quasi-differential fashion by swinging it above and below a fixed bias voltage (BIAS1). This clocking scheme is possible because the circuit operates in a fully differential manner. An external bias tee can be used to bring in the DC bias on the clock line. A simple common-source output buffer is used to isolate the frequency divider core and to present a low output impedance to the 50-Ω load.

The transistors are designed with the following widths: 14.4 μm (M1, M4–M5, M10, M13–M14, M23), 19.2 μm (M2–M3, M6–M7, M11–M12, M15–M16, M19–M22), and 9.6 μm (M8–M9, M17–M18). Numerous versions of the frequency divider were designed, with a targeted gate length of either 50 nm or 35 nm (0.3 μm or 0.285 μm drawn length). A simple current mirror is used to bias both the divider and the output buffer, and can be controlled externally by the BIAS2 pad. The nominal DC bias voltage on the clock input and BIAS1 is 700 mV.

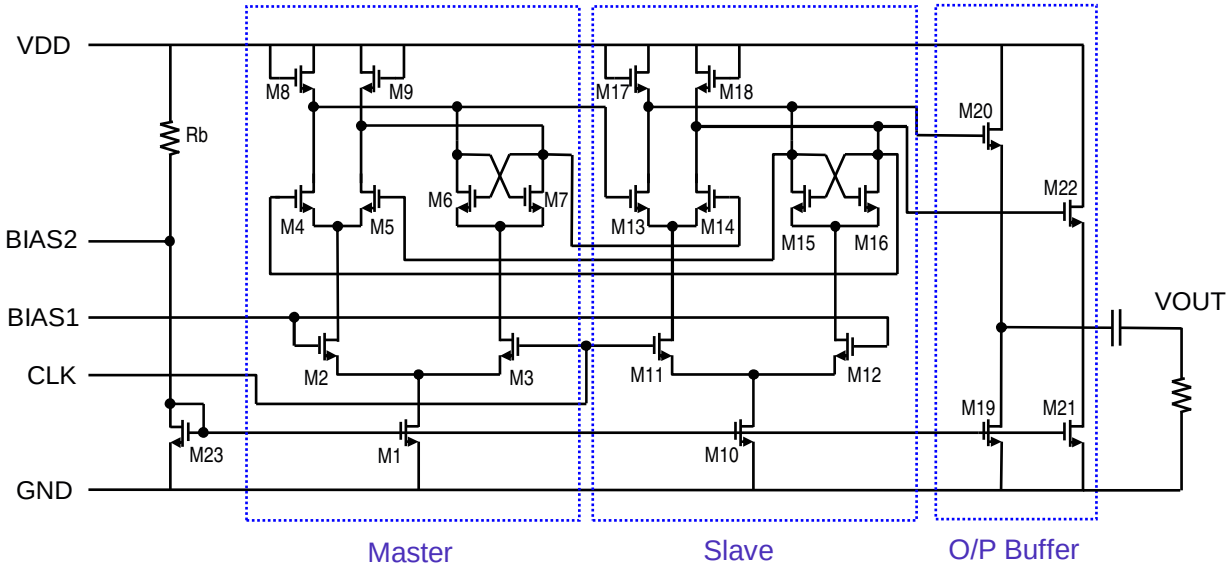


Figure 2-9. Simplified circuit schematic of CML static frequency divider with output buffer.

2.4.3.2 Estimated performance

Due to the lack of a better large-signal model, a simple behavioral (AHDL) FinFET transistor model[20] with lumped parasitic capacitances was used to run circuit-level simulations of the frequency divider. Since this behavioral description is based upon only a small set of parameters fitted to simulated transistor data, it is not expected to yield highly precise results. Nevertheless, it provides a starting point for the design of the FinFET frequency divider. Ultimately, a more accurate model will require measured data from fabricated FinFETs.

Simulations indicate that the frequency divider should be able to operate slightly above 35 GHz. A two-metal layer version of the frequency divider is expected to have better performance due to the reduced capacitance between the metal routing and the active devices. A

plot of the clock and output signals is shown in Fig. 2-10 for an input frequency of 37 GHz. Note that the plotted clock signal is the signal on the clock line, not the actual input signal, which comes from a 50-Ω sinusoidal voltage source with an amplitude of 340 mV. The power consumption of the core divider, including the current source, is estimated to be roughly 10 mW, while the power consumption of the output buffer is about 9 mW. The nominal supply voltage is 1.2 V.

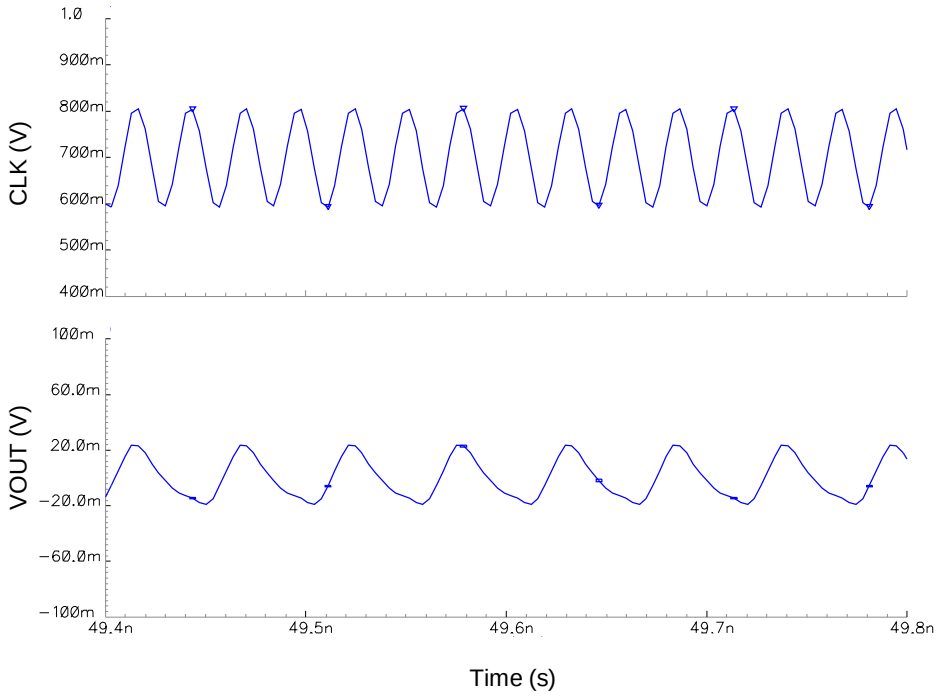


Figure 2-10. Simulated clock and output waveforms of frequency divider.

2.4.3.3 Layout

A high level of symmetry is maintained in the layout to preserve the differential operation of the circuit. Bypass capacitors are implemented using the FinFET gate oxide. Nine different versions of the frequency divider have been laid out, two of which are shown in Figs. 2-11 and 2-12. One of these utilizes two metal layers for routing, while the other uses only one layer. Of the

nine different versions, one has a target gate length of 50 nm, while the other versions have a target gate length of 35 nm. Four are unrotated, while the rest are rotated by 45 degrees. Other variations include added symmetry through the addition of a dummy output buffer, and different sizing and placement of the bypass capacitors. A description of the various frequency dividers and of the individual FinFET structures can found in Appendix A. The input and output probe pads are designed in a ground-signal-ground configuration to allow coplanar probing.

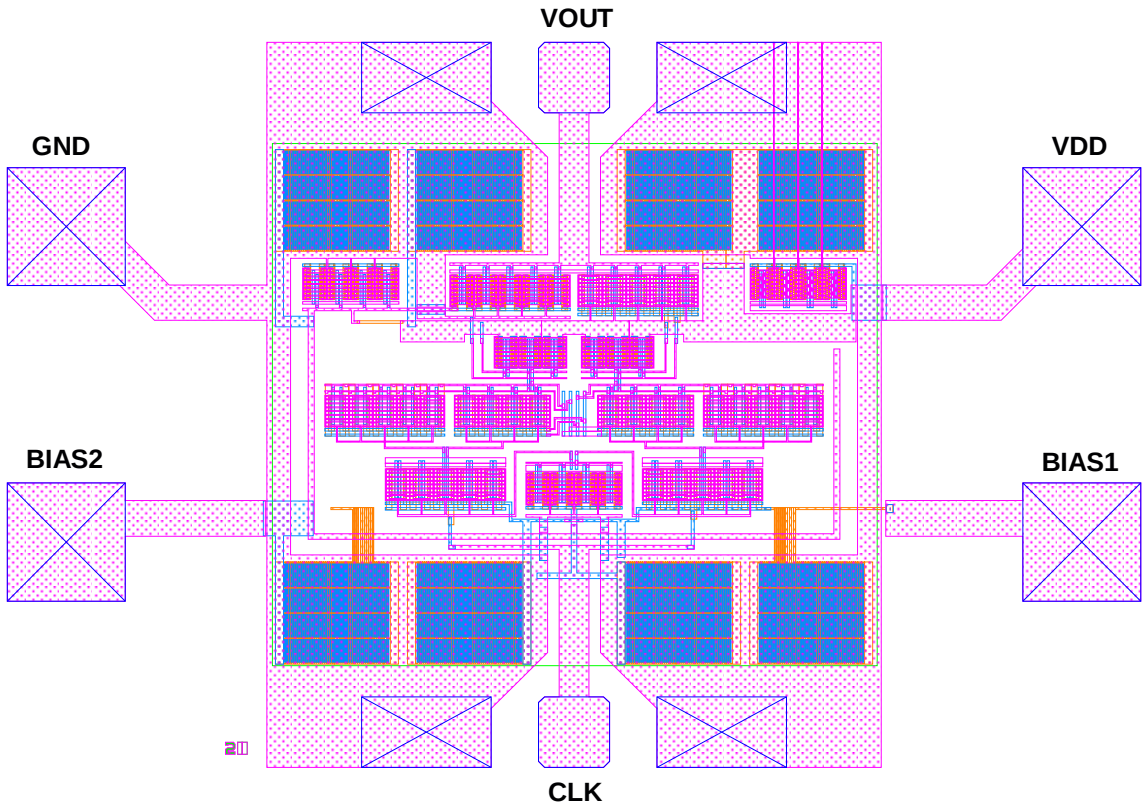


Figure 2-11. Layout of an unrotated two-metal layer version of the frequency divider.

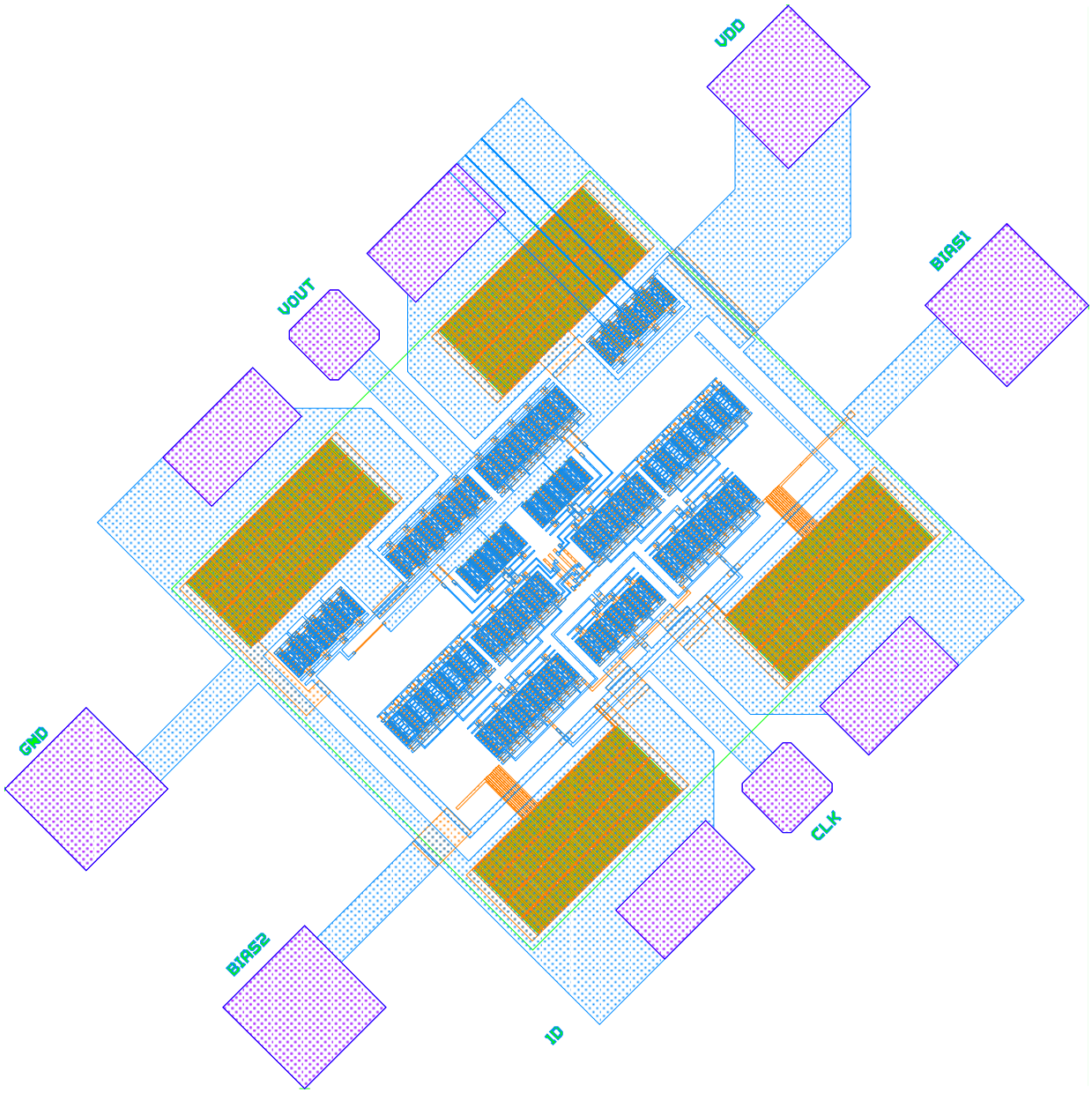


Figure 2-12. Layout of a rotated single-metal version of the frequency divider.

3 Millimeter-wave push-push CMOS VCO design

3.1 Push-push oscillator fundamentals

In general, a push-push oscillator operates by delivering power to a load primarily at the second harmonic. The output signal is generated by combining two symmetric subcircuits in such a way that the fundamental currents cancel while the second-harmonic components add constructively at the load. Thus, the operation of a push-push oscillator requires the generation of current waveforms with strong second-harmonic components and the proper phasing of the fundamental and second-harmonic current components.[21]

It can be shown mathematically that if two periodic signals are out of phase by 180º at the fundamental frequency and are added together in an appropriate output network, all the odd harmonics cancel themselves out while the even harmonics add constructively.[22] If we view each subcircuit as a separate oscillator operating at half the desired frequency, the 180º phase condition requires each oscillator to oscillate in the odd mode while quenching oscillations in the even mode. One method to enforce the 180º phase difference is shown in Fig. 3-1, in which a differential oscillator inherently generates two out-of-phase signals, which are then combined in an appropriate summing network to form the second-harmonic output.

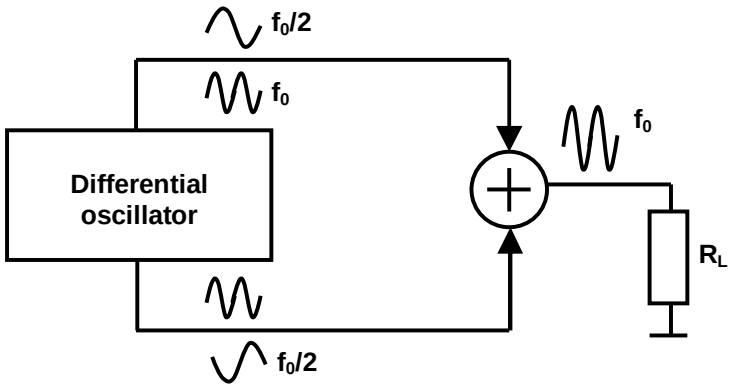


Figure 3-1. Push-push oscillator utilizing a differential oscillator.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 24 of 61

3.2 Motivations for using push-push oscillators

By utilizing the second-harmonic output, push-push oscillators effectively extend the usable frequency range of the active devices and thus enable millimeter-wave design even with circuits having a relatively low value of f_{MAX}. Several technical and practical reasons have been cited for the use of push-push VCOs: higher available device gain at $f_0/2$, higher resonator Q at $f_0/2$ due to higher varactor Q at lower frequencies, and a more compact design compared to a VCO-doubler architecture.[23] The validity of the second reason will be considered in a later section. Design of a fundamental frequency oscillator at f_0 is also very compact, of course, but may be more sensitive to process variations if it operates at frequencies near f_{MAX}, where the active devices can only provide marginal gain. In addition, since a push-push VCO effectively generates two output signals, one at f_0 and one at $f_0/2$, the fundamental output can be used as a reference signal if the VCO is operated in a phase-locked loop, potentially eliminating the need for a frequency divider.[24] Also, due to the separation of internal and external frequencies, it is simpler to suppress load pulling at the output.[22]

3.3 Architectural considerations

In assessing the usefulness of a push-push oscillator compared to a fundamental frequency oscillator, it is also helpful to consider various options in designing the local oscillator (LO) for a radio transceiver. Two possible receiver architectures for a 60-GHz radio are the single-conversion (directly to baseband or to a low-IF) and dual-conversion architectures.[25]

For a direct-conversion architecture, several options for 60-GHz LO generation are shown in Fig. 3-2 below. The most straightforward approach is to use a fundamental-frequency 60-GHz VCO. Although a 60-GHz VCO and its corresponding output buffer can be implemented in a

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 25 of 61

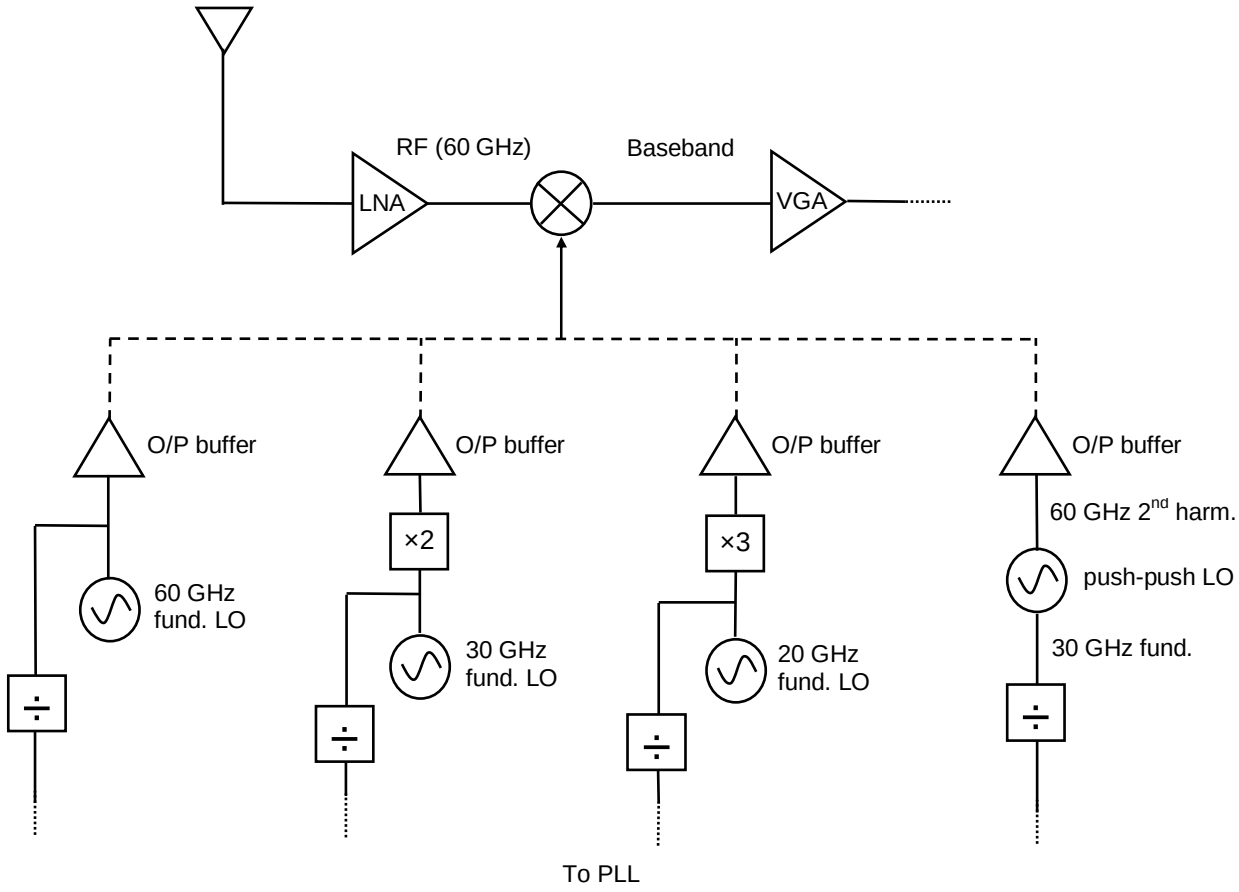


Figure 3-2. Various 60-GHz LO generation methods in a direct-conversion radio architecture.

typical modern CMOS technology, designing a non-injection-locked frequency divider at this high frequency with acceptable power consumption may not be trivial. Common-mode logic (CML) and Miller dividers in CMOS technologies can be realized up to fairly high frequencies, but in general have a relatively high power consumption. For example, a divide-by-four 40-GHz dynamic Miller divider a 0.18-μm CMOS technology has been reported, having a power consumption of 31 mW from a 2.5-V supply.[26] A static CML frequency divider operating up to 25 GHz in 0.12-μm CMOS has also been demonstrated, but it consumes 40.6 mA from a 1.5-V supply (including the output buffer).[19] Injection-locked frequency dividers can operate at very

high frequencies with low power consumption, but typically suffer from limited input locking range. For example, a 40-GHz injection-locked divider has been designed in 0.12-μm CMOS, consuming only 3 mW from a 1.5-V supply, but has a limited locking range of 1.5 GHz.[27] The same article also reported a 50-GHz divider consuming the same amount of power, but with a locking range of only 80 MHz. More recently, however, a 55-GHz injection-locked frequency divider in a 0.2-μm CMOS process was reported, consuming 10.1 mW from a 1.0-V supply while providing a 3.2-GHz locking range.[28] This divider appears to satisfy the requirements of relatively low power, high speed, and sufficient locking range.

Another approach is to utilize a lower frequency oscillator at 20 GHz or 30 GHz followed by a frequency doubler or tripler. This eases the requirements on the frequency divider and reduces the amount of frequency division necessary, potentially leading to power and area savings with respect to the divider block. Recently, 40-GHz and 60-GHz frequency doublers have been demonstrated in 90-nm CMOS.[29] The topology is a single-ended active doubler based on microstrip transmission-line matching structures. The 60-GHz doubler consumes approximately 4 mW with a conversion loss of 15 dB at an input frequency of 30 GHz and an input power of 3 dBm. With this relatively low doubler power consumption, the VCO-doubler approach may yield similar performance as the fundamental-frequency approach with comparable power. However, since this particular doubler architecture introduces a conversion loss, this loss may need to be compensated by increased power in the output buffer.

The push-push VCO approach utilizes the 30-GHz differential output signal that is inherently generated by the push-push VCO. This potentially reduces the power consumption of the frequency divider block by obviating the first divide-by-two stage (from 60 GHz to 30 GHz). Assuming that, to first order, the push-push VCO requires the same amount of power as a

60-GHz fundamental-frequency oscillator (or perhaps slightly more power), the requirement of one less frequency division operation at 60 GHz may lead to an overall power savings. However, since the second harmonic output of the push-push VCO is single ended, some extra area may be required to perform a single-ended to differential conversion and some extra power may be required to compensate for any loss in the conversion process. Compared to the VCO-frequency doubler approach, the push-push approach may result in an overall power savings due to the elimination of the frequency doubler block. An exact comparison of these various approaches is highly topology dependent, but the qualitative analysis presented above suggests that a push-push VCO approach has the potential to consume the same or perhaps even less power than the other approaches. Table 3-1 provides some rough estimates of the power consumption of various CMOS blocks for several of the LO-generation schemes, though actual values are topology and technology dependent. These estimates are loosely based on simulations or various data reported in the literature.

	LO power consumption	**Frequency multiplier power consumption**	**Frequency divider power consumption (for division down to 30 GHz)**
60-GHz fundamental VCO	10–15 mW (for –10 dBm single-ended output power, including output buffers)	---	10–15 mW (injection-locked)
30-GHz fundamental VCO + frequency doubler	15–20 mW (for –5 dBm single-ended output power, including output buffers)	5 mW per doubler (with 15 dB conversion loss)	---
30-GHz push-push VCO (with 60-GHz 2nd harmonic)	20–25 mW (for –5 dBm output power)	---	---

Table 3-1. Rough estimates of CMOS power consumption for various LO generation schemes.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 28 of 61

A schematic of various LO generation options for a dual-conversion architecture is shown in Fig. 3-3. By using a lower LO frequency, this architecture relaxes the design of both the VCO and the phase-locked loop. As before, the push-push approach may potentially yield a power savings since it simultaneously generates both a differential 15-GHz signal and a single-ended 30-GHz signal.

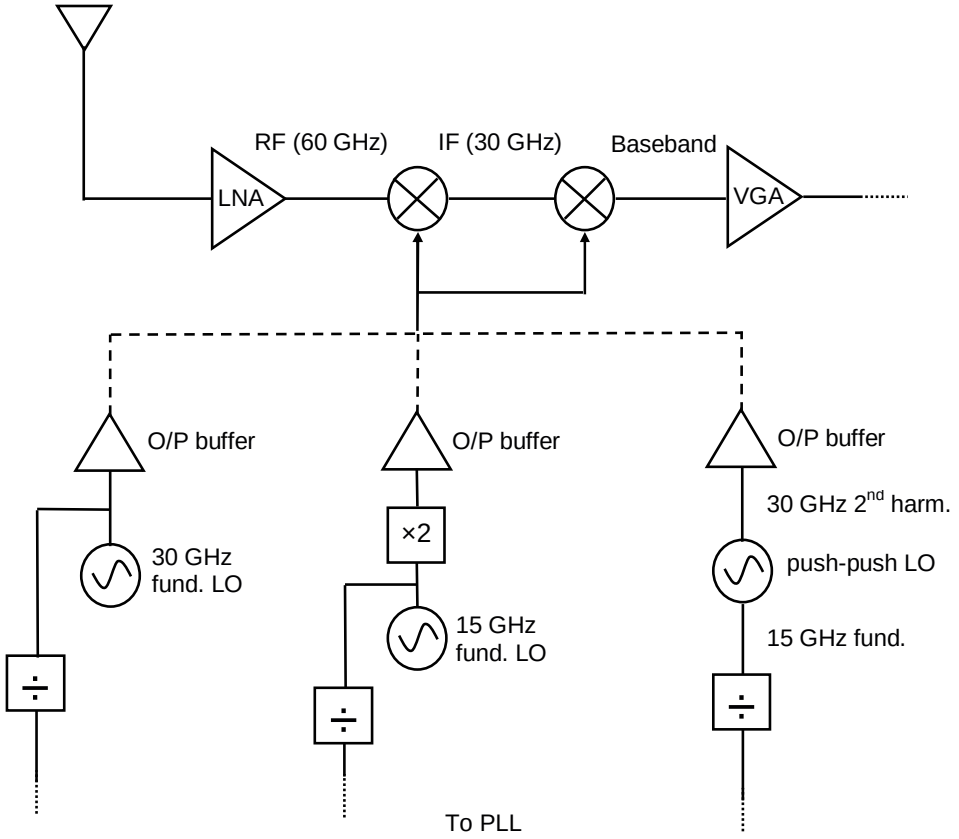


Figure 3-3. Various 60-GHz LO generation methods in a dual-conversion radio architecture.

3.4 Dependence of resonator Q on frequency of operation

A reason cited in the literature for the use of a push-push VCO versus a fundamental-frequency oscillator is high resonator Q at $f_0/2$ versus low resonator Q at f_0, which in turn affects

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 29 of 61

the phase noise performance of the VCO. While one can expect to obtain a lower varactor Q at high frequencies, this is not necessarily true for inductive components, where the Q-factor increases with frequency and then decreases beyond a peak-Q frequency due to substrate loss mechanisms. Therefore, depending on the desired resonant frequency, the resonator Q is not necessarily lower at higher frequencies.

At frequencies approaching the self-resonant frequency of the inductor, it is possible that the overall resonator Q at f_0 will be lower than that of a comparable resonator at $f_0/2$, due to the drop in inductor Q at these high frequencies. In general, however, and especially at lower frequencies, this behavior is not necessarily observed for practical L-C tanks.

A simple circuit simulation of a parallel L-C tank demonstrates the dependence of tank Q on the resonant frequency of the tank. The effective values of L and C were adjusted to shift the resonant frequency of the tank. To ensure a meaningful basis for comparison, a similar L/C ratio was maintained for all cases. The inductor and accumulation-mode varactor models used in the simulation were those provided in the design library of a commercial 0.13-μm mixed-signal CMOS process. For lower frequencies, the inductive element was a spiral inductor; for higher frequencies, the inductive element was implemented using a coplanar transmission line. Simulation results are shown in Figs. 3-4 and 3-5.

The definition of Q chosen here is based on the frequency stability factor (S_F), defined as

$$S_F = -\omega_0 \frac{d\theta}{d\omega}\bigg|_{\omega=\omega_0}$$

where ω_0 is the resonant frequency in radians/sec, and θ is the phase in radians. This can be rewritten as

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 30 of 61

$$S_F = -f_0 \frac{\pi}{180^\circ} \frac{d\varphi}{df}\bigg|_{f=f_0}$$

where f_0 is the resonant frequency in Hertz, and φ is the phase in degrees. The Q-factor is then defined as

$$Q = \frac{S_F}{2}.$$

This definition is useful for circuit applications and particularly for oscillators, since it is directly related to frequency stability.

From Table 3-1, it can be seen that Q *increases* monotonically as the resonant frequency increases, showing that for this particular frequency range it may not be advantageous to choose a push-push topology on the basis of Q enhancement alone. However, for the higher frequency range shown in Fig. 3-5, the results in Table 3-2 suggest that Q begins to level off above a certain frequency. It should be noted that these results are only qualitative, as the models employed are not calibrated to hardware data at very high frequencies and thus are expected to be less accurate at these frequencies. A more precise analysis would, of course, require a detailed three-dimensional electromagnetic simulation of the inductor and capacitor. Nevertheless, it is evident that tank Q does not necessarily degrade with frequency, and a judicious high-frequency design should take this into consideration.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 31 of 61

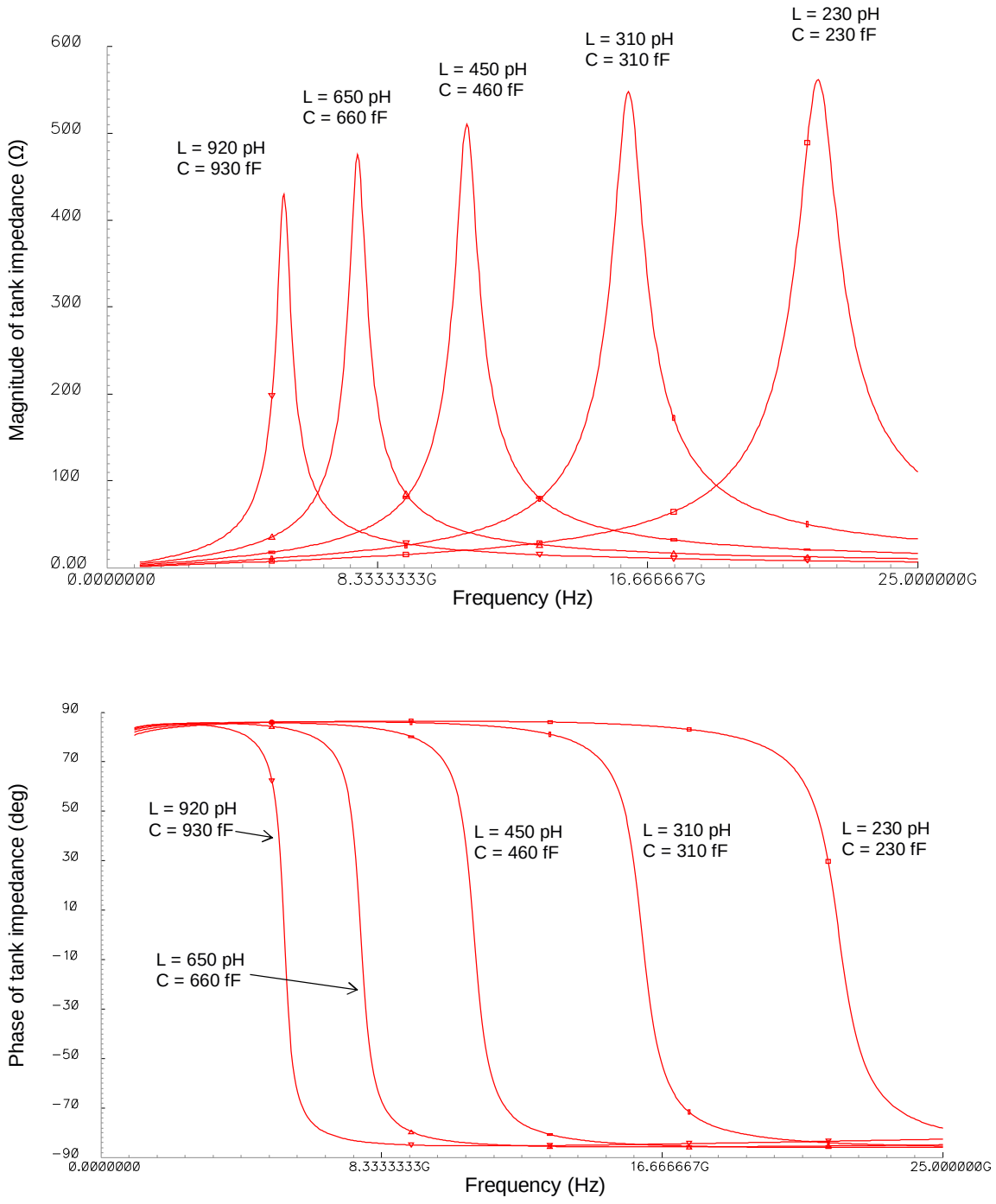


Figure 3-4. L-C tank impedance for various resonant frequencies (lower frequency range).

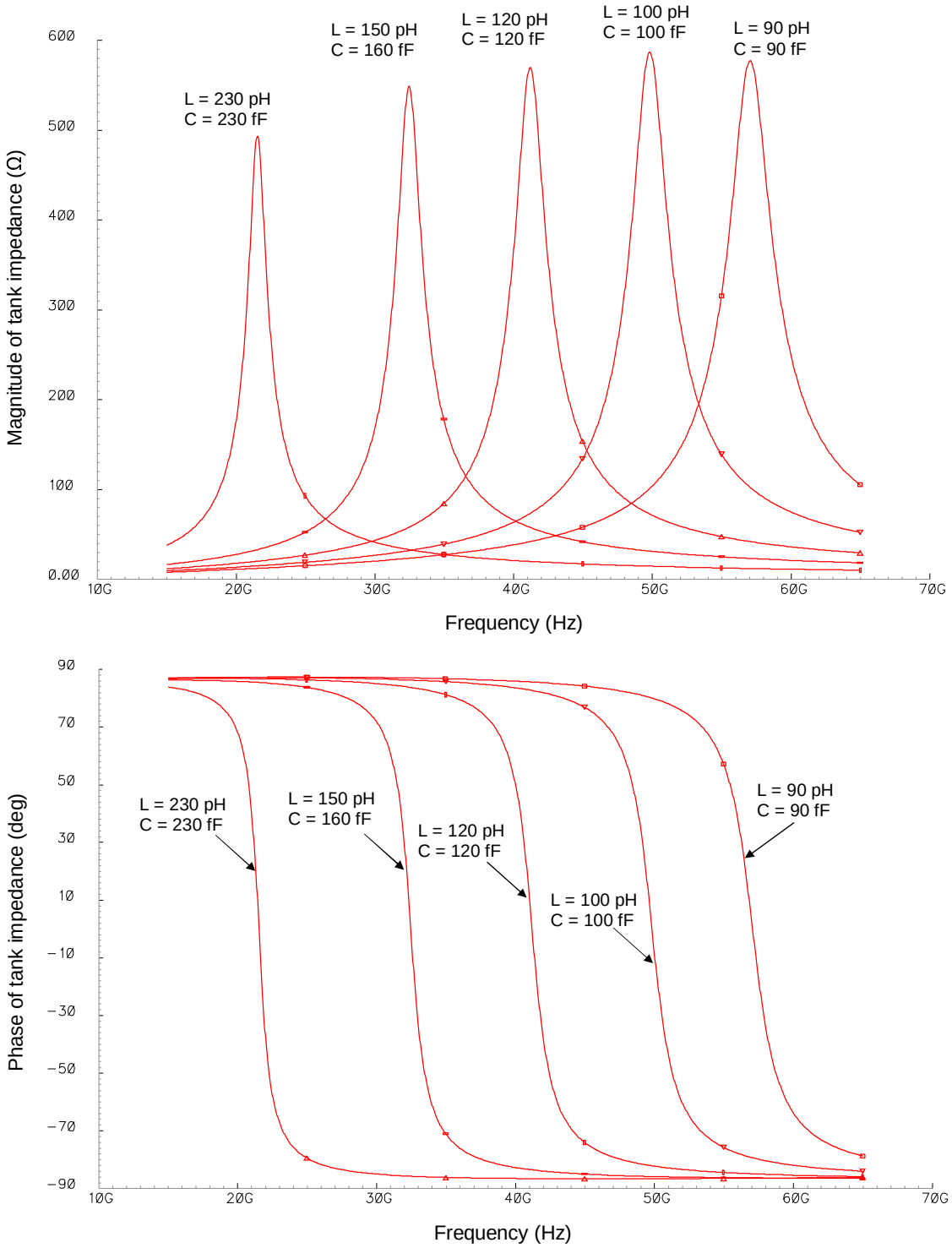


Figure 3-5. L-C tank impedance for various resonant frequencies (higher frequency range).

L	C	f_0	Q
920 pH	930 fF	5.4 GHz	14.0
650 pH	660 fF	7.7 GHz	15.4
450 pH	460 fF	11 GHz	16.8
310 pH	310 fF	16 GHz	18.1
230 pH	230 fF	22 GHz	18.9

Table 3-2. Q-factor of various L-C tanks (lower frequency range).

L	C	f_0	Q
230 pH	230 fF	22 GHz	17.6
150 pH	160 fF	33 GHz	19.6
120 pH	120 fF	41 GHz	20.3
100 pH	100 fF	50 GHz	20.7
90 pH	90 fF	57 GHz	20.6

Table 3-3. Q-factor of various L-C tanks (higher frequency range).

3.5 Negative resistance generation and balanced VCO construction

There are a variety of ways to generate the negative resistance required to produce and sustain an oscillation. One method is based on the source follower configuration, as shown in Fig. 3-6. The impedance seen looking into the gate of the transistor contains a frequency-dependent negative real part, which depends on the device transconductance as well as the sizes of capacitors C_1 and C_2. Two of these source followers can be combined appropriately with a resonant tank to construct a balanced VCO topology, as shown to the right in Fig. 3-6. The differential signals generated by this VCO can then be combined in a straightforward manner to produce a second-harmonic push-push output.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 34 of 61

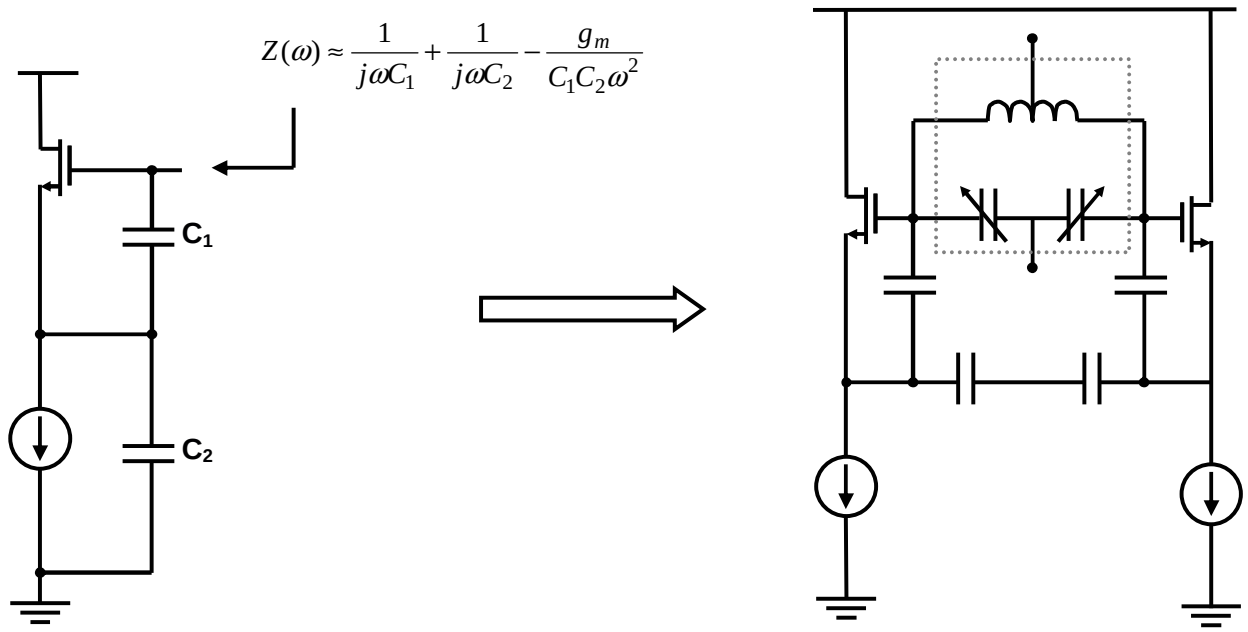


Figure 3-6. Negative-resistance generator and associated balanced VCO topology.

3.6 Design of proposed push-push CMOS VCO

The basic schematic of the CMOS push-push VCO studied in this work is shown in Fig. 3-7. The VCO essentially consists of two source-follower circuits with the resonant circuit connected to the gates. A cascode stage is used to decouple the VCO core from the output.[30,31] Instead of using active current sources to provide a bias current, a pair of small inductors (L_{bias}) is used. Although they require more layout area than active current sources, they do not consume any DC voltage headroom, allow the voltage at the source of M_1 and M_2 to swing below ground, and also generate less noise. The targeted fundamental frequency of oscillation is 30 GHz, and the second-harmonic currents are summed through a pair of capacitors (C_0). A novel component of this VCO design is the addition of the shunt inductor L_{shunt}. Simulations indicate that the

presence of L_{shunt} can boost the second-harmonic output power and increase start-up reliability while reducing overall DC power consumption.

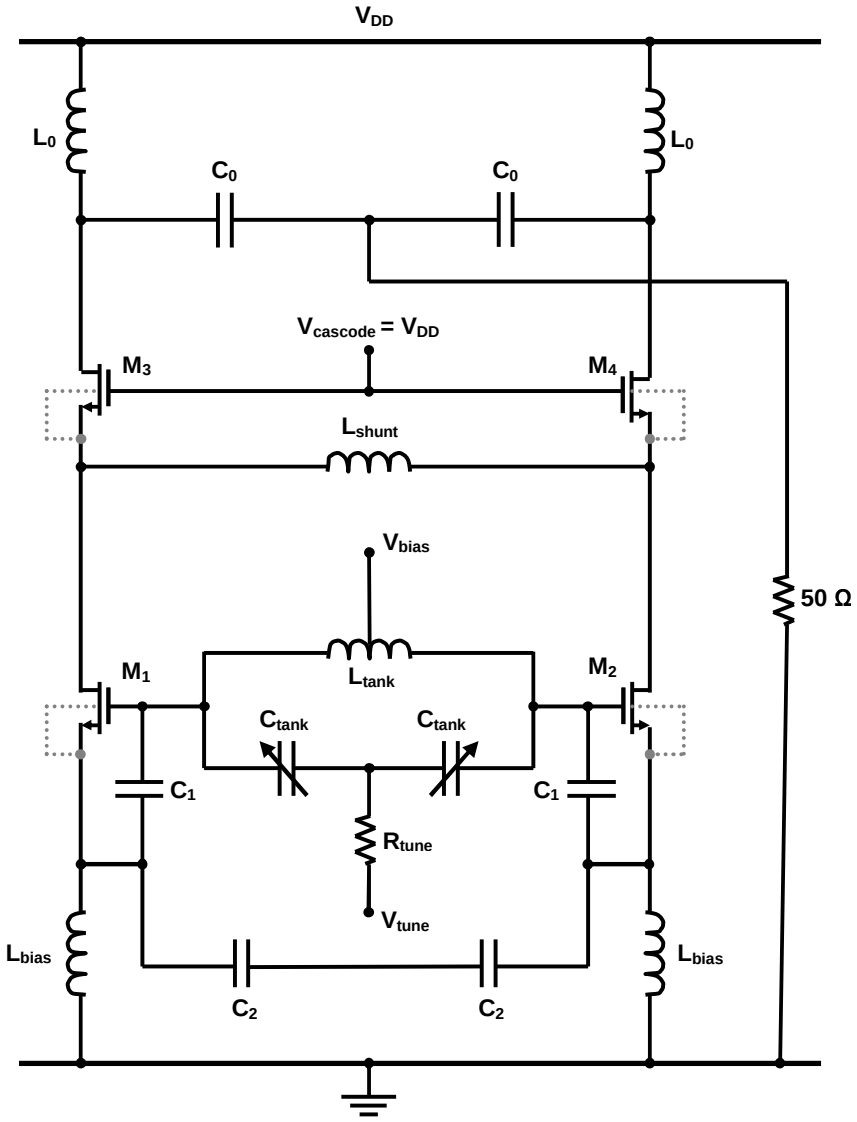


Figure 3-7. Basic schematic of proposed push-push VCO.

A representative plot of the differential (or odd-mode) input impedance seen looking into the gates of M_1 and M_2 with the L-C tank removed is shown in Fig. 3-8, with and without L_{shunt}. For the sake of analysis, the input impedance has been split into two components: a parallel

resistance, R_p, and a parallel capacitance, C_p. To ensure proper start-up of the oscillator, R_p should be sufficiently negative relative to the parallel resistance of the L-C tank (R_{tank}) at the fundamental frequency of oscillation, i.e., $|R_p| < nR_{tank}$, where n is a safety factor, preferably greater than 2 or 3. At the same time, C_p, which is determined by C_1, C_2, and various parasitic capacitances, should not be too large, which would degrade the tuning range of the VCO. Plots of R_p and C_p can thus serve as guidelines in choosing the values of various design parameters of the VCO, such as C_1, C_2, L_{bias}, and the width of the active devices.

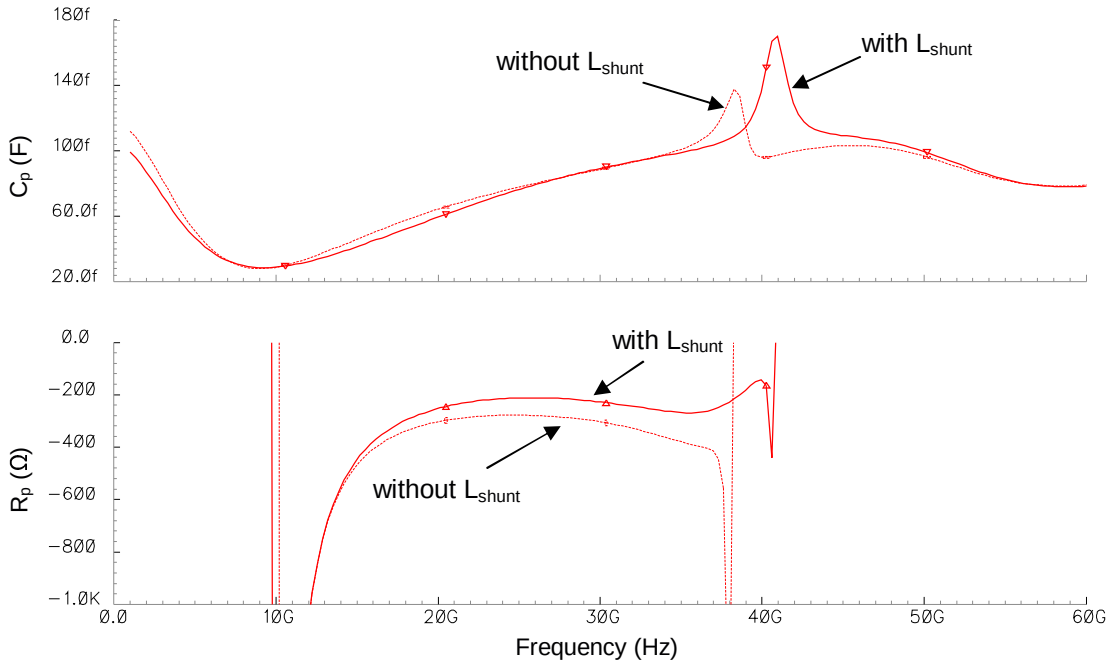


Figure 3-8. Differential (odd-mode) input impedance (L_{shunt} = 130 pH).

By comparing the curves in Fig. 3-8, it can be seen that one of the effects of L_{shunt} on the small-signal behavior, for this particular simulation, is to boost the negative resistance near the frequency of interest (30 GHz), which helps to increase start-up reliability. Simulations show

that the behavior of R_p depends not only on L_{shunt}, but also on the values of L_0 and C_0. In general, the effect of inserting L_{shunt} is to boost R_p near the frequencies of interest. A plot of R_p at 30 GHz as a function of L_{shunt} (using an ideal inductor) is shown in Fig. 3-9, which indicates that there exists a value of L_{shunt} that maximizes the small-signal input resistance. This value of L_{shunt}, however, does not necessarily correspond to the value that maximizes the overall VCO output power at the second harmonic. Using a more realistic model of the inductor, it has been observed that the value of L_{shunt} also affects the roll-off of R_p above 30 GHz, which may create a start-up reliability problem. In the final design, the effective L_{shunt} is approximately 120 pH.

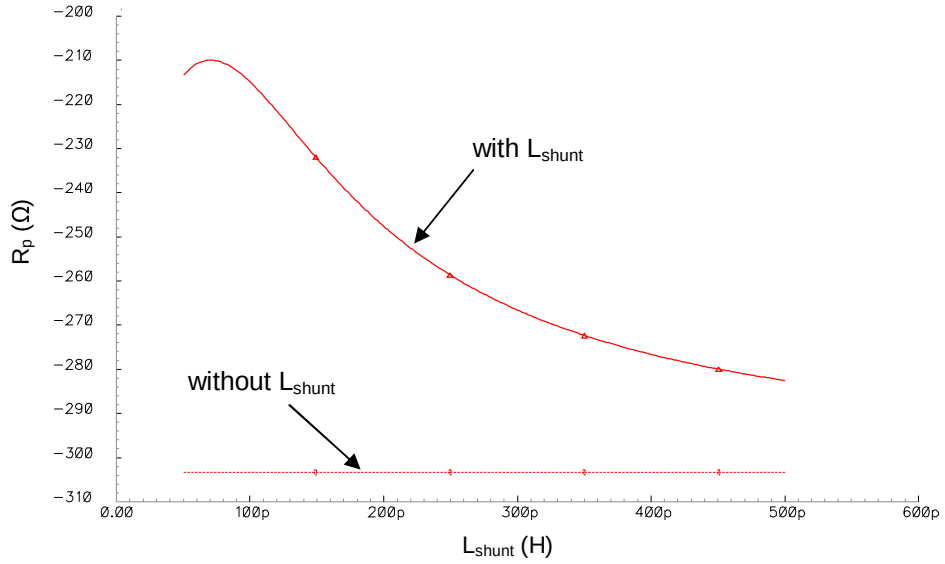


Figure 3-9. R_p vs. L_{shunt} at 30 GHz (using an ideal inductor).

In general, the sizing of C_1 and C_2 represents a tradeoff between R_p and C_p—increasing C_1 or C_2 tends to increase the value of R_p, but also increases C_p. In the actual design, C_1 and C_2 were implemented with metal-insulator-metal (MIM) capacitors.

The varactors were implemented with accumulation-mode (n-FET in n-well) MOS devices. Simulation shows that to maximize the C_{max}/C_{min} ratio for V_{bias} = 0.75 V, the varactors should be oriented with the tuning line (V_{tune}) connected to the drain/source rather than the gate (Fig. 3-10). However, if we add a fixed capacitance, representing the parasitic capacitance of the transistors and tank inductor, in parallel with the varactors, this reduces the C_{max}/C_{min} ratio and also reduces the difference in the C_{max}/C_{min} ratio due to varactor orientation. Estimating the parasitic capacitance to be 100 fF, C_{max}/C_{min} for the drain/source-connected case then drops to 1.39, while C_{max}/C_{min} for the gate-connected case is only slightly smaller, at 1.34. To minimize the effects of polysilicon gate resistance and n-well series resistance and thereby maximize Q, each gate finger of the varactor was designed at the minimum recommended length and width. The varactors were sized large enough to provide an adequate tuning range for the VCO, but not so large as to significantly degrade the parallel L-C tank resistance at resonance.

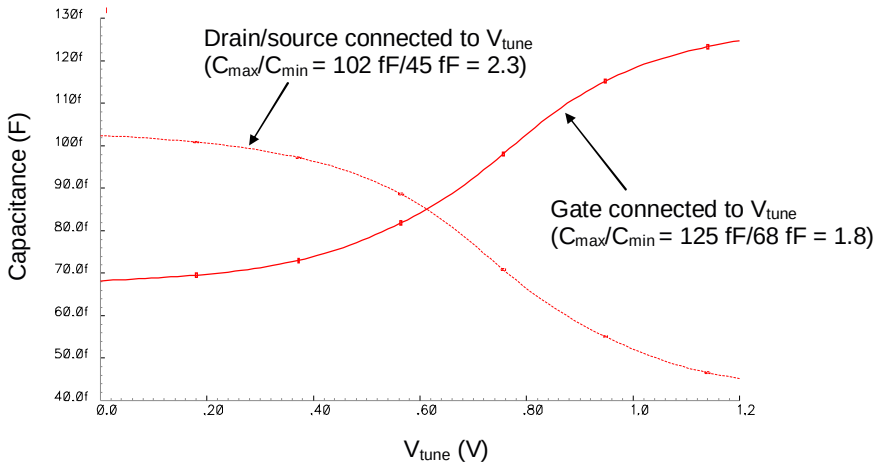


Figure 3-10. Capacitance of varactors (two connected in series) vs. V_{tune}, with V_{bias} = 0.75 V.

Triple-well NFET devices were used to improve the negative resistance generated by the balanced source-follower pair. To reduce the adverse effect of gate resistance on high-frequency performance, all transistors were designed with multiple short fingers (1 μm). The BSIM3-based NFET transistor model provided by the design library was used for simulations. A more advanced high-frequency model, such as BSIM4, would probably yield more accurate results at the frequencies involved in this design.

A small resistor, R_{tune}, was added to help quench any unwanted even-mode oscillations by reducing the even-mode Q of the tank. These resistors were kept relatively small to minimize the degradation of the VCO phase noise due to the thermal noise of the resistors.

The L_{bias} inductors were implemented with top-metal one-and-a-half turn spiral inductors, each with an inductance of approximately 600 pH. The self-resonance frequency of L_{bias} is estimated to be above 60 GHz, which guarantees that L_{bias} still appears inductive at the fundamental frequency of the oscillator.

The L_0 inductors at the top of the VCO were implemented with coplanar transmission lines having a signal width of 15 μm and a signal-to-ground spacing of 10 μm. One benefit of using transmission lines is that they have a well-defined ground return path that confines the fields and thereby reduces magnetic and electric coupling to nearby structures. The signal width can be adjusted to reduce the conductor loss, while the signal-to-ground spacing controls the characteristic impedance Z_0 and also the tradeoff between inductive and capacitive quality factors.[4] In order to prevent gate oxide breakdown, the maximum gate-drain voltage of all the MOSFETs was kept roughly at or below 1.5 V over the entire frequency range of operation. Unfortunately, this constraint results in sub-optimal output power because of the limit imposed on the voltage swing across the gate and drain of the cascode transistors.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 40 of 61

3.7 Center-tapped inductor design and modeling

To maximize its Q-factor and minimize its area, L_{tank} was implemented as a center-tapped symmetric inductor rather than two single-ended inductors. The inductor was simulated with a high-frequency three-dimensional field solver (HFSS), as shown in Fig. 3-11. The multi-layer dielectric stack was modeled with two layers: a passivation layer and an oxide layer. A perfectly conducting ground ring was drawn around the inductor to provide a common reference potential for the three ports. For a two-port simulation, it is possible to simulate the inductor without a ground ring or a ground plane by using a single lumped port to excite the inductor differentially. A simulation performed on a small inductor indicates that using a single port results in a relatively small change in inductance and a more significant change in Q at high frequencies. A radiation boundary was drawn around the structure to allow waves to radiate infinitely far into space. A perfect-E boundary was also assigned to one of the edges of the oxide layer/ground

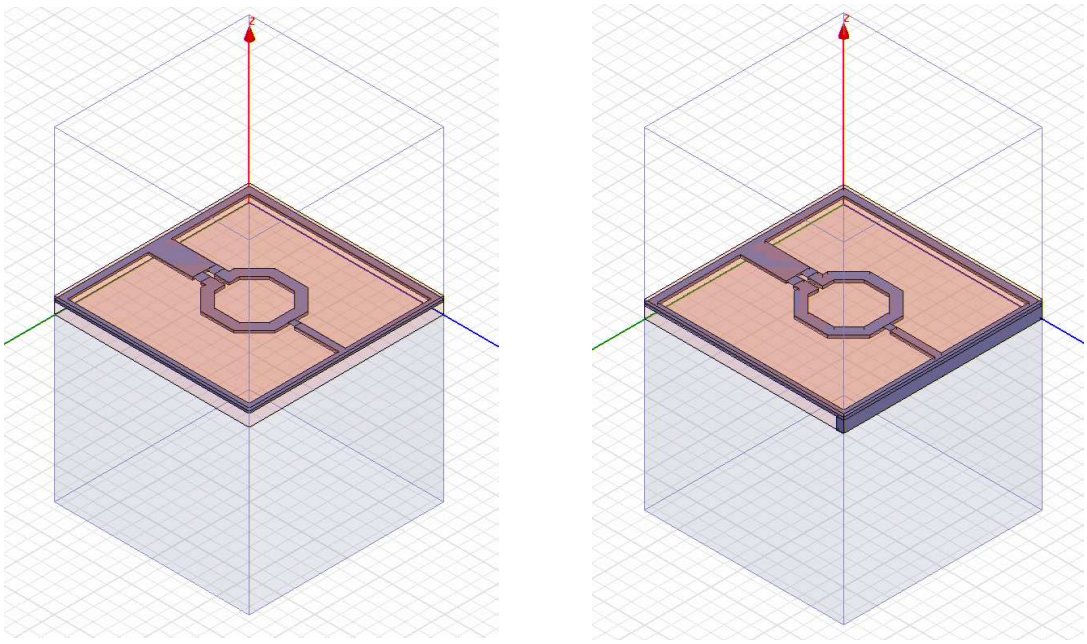


Figure 3-11. HFSS models of L_{tank}. Without substrate contact (left). With contact (right).

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 41 of 61

ring. In the setup on the left in Fig. 3-11, the ground ring is embedded in the oxide and does not touch the substrate. In the setup on the right in Fig. 3-11, the ground ring is extended to touch the substrate at one end of the structure (to emulate the effect of a substrate contact). Simulations indicate that these two structures yield similar results. Due to the availability of some measured data from a recent test chip, additional simulations were performed in order to compare HFSS results to measured data. These simulations are described in Appendix B.

Since the ring inductors L_{tank} and L_{shunt} are driven by differential signals, they should be described by an appropriately-defined differential Q factor. There are several ways to calculate this value of differential Q. The most direct method is to treat the inductor as a one-port device and drive it differentially with a single port. In this case, the conventional differential inductor Q (analogous to the conventional definition of inductor Q, which involves the difference between the average stored magnetic and electrical energies[32]) is simply

$$Q_{DIFF} = \frac{\mathrm{Im}\{Z_{in}\}}{\mathrm{Re}\{Z_{in}\}} = -\frac{\mathrm{Im}\{Y_{in}\}}{\mathrm{Re}\{Y_{in}\}}$$

When the inductor is simulated or measured as a two-port device, it is possible to convert the two-port S-parameters into an equivalent differential one-port S-parameter.[33] Specifically, we can define

$$S_{DIFF} = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2},$$

from which we can determine

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 42 of 61

$$Z_{DIFF} = 2Z_0 \frac{1+S_{DIFF}}{1-S_{DIFF}}$$

where Z_0 is the characteristic impedance of the system, and

$$Q_{DIFF} = \frac{\mathrm{Im}\{Z_{DIFF}\}}{\mathrm{Re}\{Z_{DIFF}\}}.$$

Alternatively, we can define Z_{DIFF} directly from the measured Z-parameters:

$$Z_{DIFF} = Z_{11} + Z_{22} - Z_{12} - Z_{21}.$$

In terms of Y-parameters, we can define

$$Y_{DIFF} = \frac{Y_{11}Y_{22} - Y_{12}^2}{Y_{11} + 2Y_{12} + Y_{22}}$$

and consequently

$$Q_{DIFF} = -\frac{\mathrm{Im}\{Y_{DIFF}\}}{\mathrm{Re}\{Y_{DIFF}\}}.$$

The results of the three-port simulation, in terms of L_{diff} (the inductance between ports 1 and 2), Q_{diff}, and L_{center} (the inductance between port 1 and the center tap) are shown in Fig. 3-12. It is observed that L_{center} is considerably larger than L_{diff}, most likely due to added inductance from the presence of the ground loop. Although this does not accurately reflect the inductance that

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 43 of 61

would be seen in an actual circuit, simulations show that the presence of extra inductance at the center tap has negligible effect on the behavior of the VCO. Although a rough calibration was performed using a modeled inductor from the design library, it was difficult to obtain a reliable estimate of Q in HFSS, especially at higher frequencies. It is expected that the Q value predicted from this simulation is optimistic.

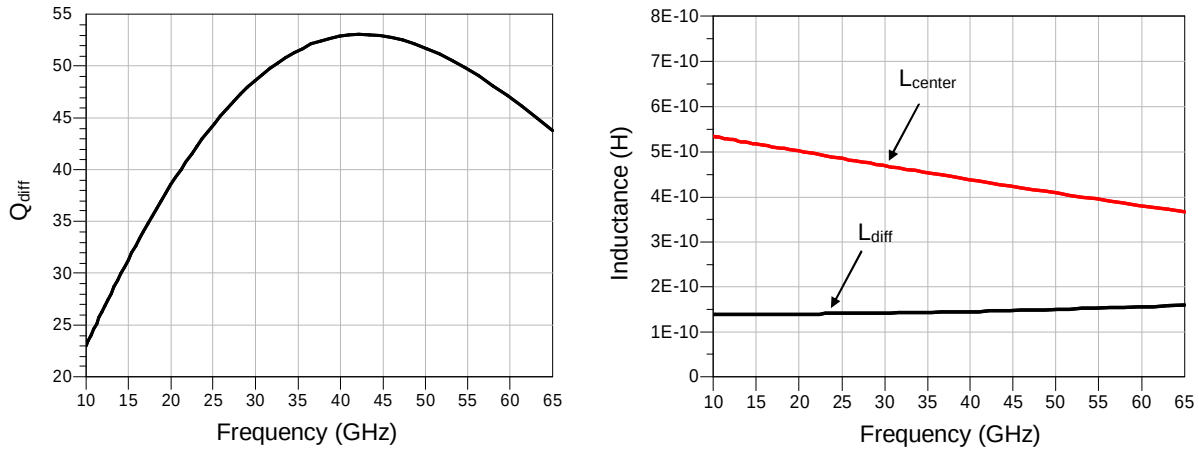


Figure 3-12. HFSS simulation results for center-tapped inductor L_{tank}.

For the center-tapped inductor, a multi-section π-network model (Fig. 3-13) was fitted to the data from HFSS with the aid of an optimizer (Agilent ADS). The results of the fitting are shown in Fig. 3-14. Each double-π section resembles in part the topology presented in the paper by Cao *et al.*[34] Theoretically, due to the distributed nature of the structure at high frequencies, a model consisting of many short microstrip transmission line sections approximated by lumped elements would more fully capture high-frequency effects (cf. Long and Copeland[35]). This, however, would come at the cost of increased model complexity and simulation time. L_{shunt} was also simulated in HFSS, and the resultant two-port S-parameters were directly imported into the circuit simulator.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 44 of 61

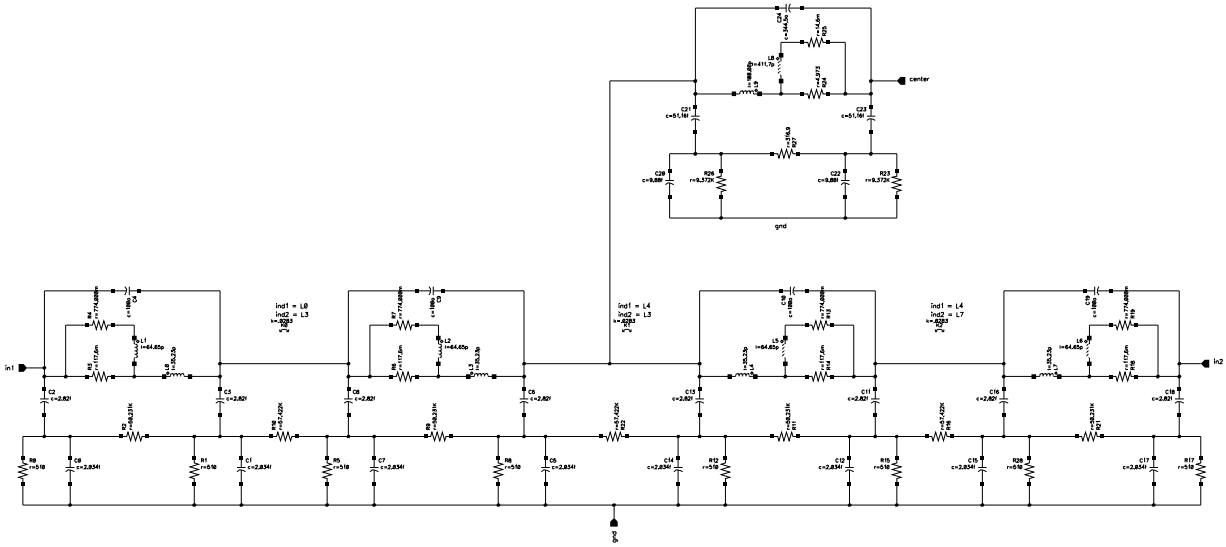


Figure 3-13. Schematic of multi-π model of center-tapped inductor L_{tank}.

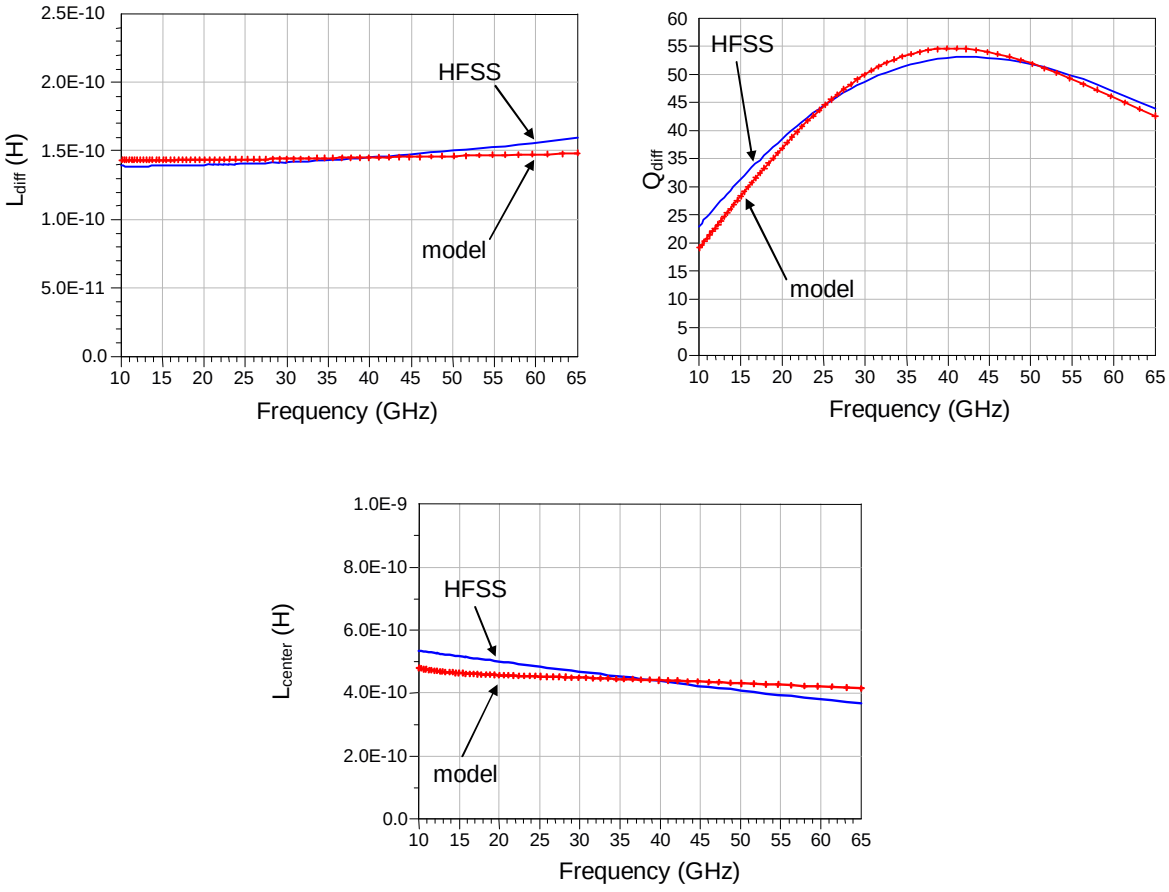


Figure 3-14. HFSS vs. model comparison of center-tapped inductor L_{tank}.

3.8 Transmission-line inductor design

To verify the inductance of the coplanar transmission line inductor L_0, the transmission line was simulated in HFSS. The bend in the structure is required in the VCO layout to keep the ends of a pair of these transmission lines close together, thereby reducing unwanted inductance between them. Underpasses between the ground traces are placed near the discontinuity to maintain a well-defined ground potential and to suppress any parasitic odd coplanar waveguide mode. A scalable model of a straight transmission line, provided by the design library and having a similar value of inductance at 60 GHz as the HFSS model, was used for circuit simulations. This library model is expected to have a more accurate value of Q than that predicted by simulation.

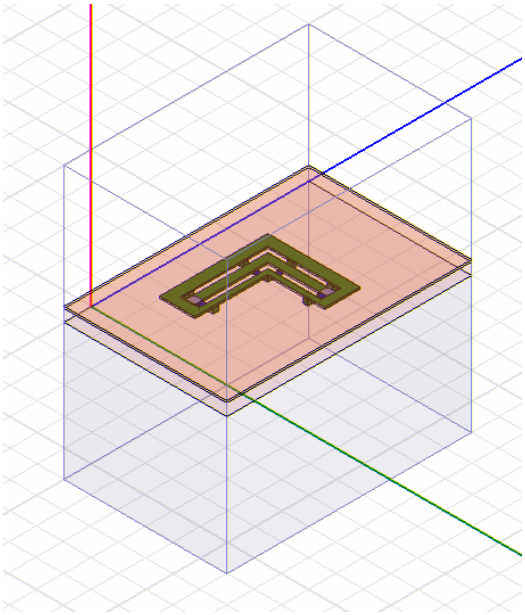


Figure 3-15. HFSS model of coplanar transmission line inductor.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 46 of 61

3.9 Simulation results

3.9.1 Effect of L_{shunt} on VCO performance

In order to investigate the effect of L_{shunt} on VCO performance, the VCO must be designed in such a way that it oscillates both with and without the presence of L_{shunt}. To allow a meaningful comparison, fixed values of L_0 and C_0 were selected for the two cases—with and without L_{shunt}—while maintaining the maximum cascode gate-drain voltage requirement mentioned previously. Two sets of comparisons are made, one in this section and the other, with increased VCO output power, in the next section.

Simulation results for the first VCO, without L_{shunt}, are shown in Fig. 3-16 for V_{bias} = 0.75 V. At V_{tune} = 0.46 V, a second-harmonic frequency of 60 GHz is achieved. At this frequency, the output power is about –21 dBm and the DC current consumption of the voltage supply V_{DD} is 29 mA. The output power peaks at around –20 dBm when V_{tune} = 0.69 V. The tuning range is 8.9 GHz (57.7 GHz to 66.6 GHz for V_{tune} = 0 V to 1.2 V).

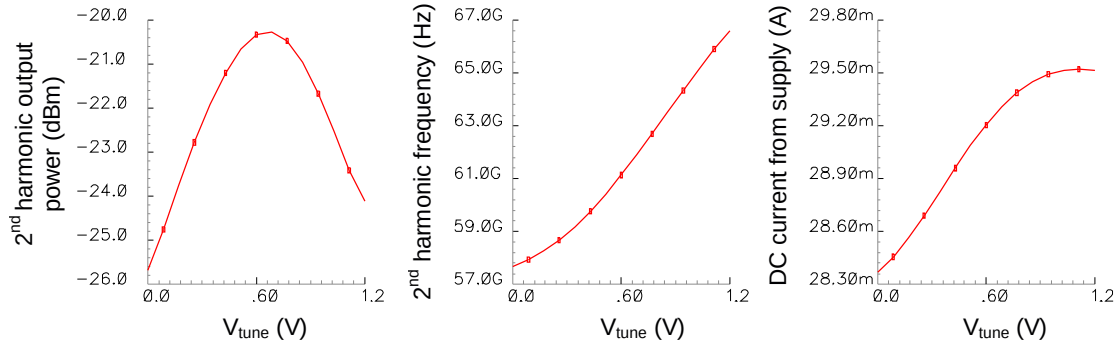


Figure 3-16. Simulated performance of VCO without L_{shunt}.

Simulation results for the same VCO with the addition of $L_{shunt} \approx$ 120 pH are shown in Fig. 3-17 for V_{bias} = 0.75 V. At V_{tune} = 0.48 V, a second-harmonic frequency of 60 GHz is achieved.

At this frequency, the output power is about –19 dBm, and the DC current consumption of the voltage source V_{DD} is 28 mA. The output power peaks at around –18 dBm when V_{tune} = 0.7 V. The tuning range is 8.2 GHz (57.6 GHz—65.8 GHz). A comparison of these results indicates that one effect of L_{shunt} on VCO performance is to slightly boost the second-harmonic output power at 60 GHz, in this case by about 2 dB. For this example, L_{shunt} also appears to increase the output power over the rest of the tuning range.

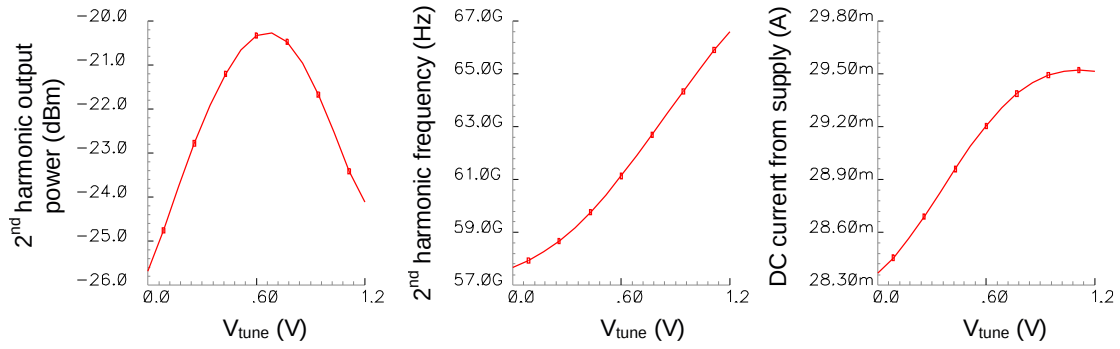


Figure 3-17. Simulated performance of VCO with L_{shunt}.

3.9.2 Effect of L_{shunt} (with improved output power)

The output power can be increased by adjusting the values of L_0 and C_0 while making sure that all gate-drain voltages are safely below the gate oxide breakdown voltage. A different value of C_{tank} is also used this time, which shifts the center frequency. The resulting performance is shown in Fig. 3-18. At V_{tune} = 0.52 V, a second-harmonic frequency of 60 GHz is achieved. At this frequency, the output power is –3.1 dBm and the DC current through V_{DD} is about 20 mA. A maximum output power of –2.8 dBm is achieved when V_{tune} = 0.18 V. The tuning range is 7.7 GHz (58.3 GHz to 66.0 GHz). The phase noise at 1 MHz offset from the 60-GHz second

harmonic is approximately –86 dBc/Hz (Fig. 3-19). It should be noted that these simulation results include the effect of various post-layout parasitics, which were estimated using ASITIC, an inductor modeling tool. The layout of the VCO is discussed in §3.10.

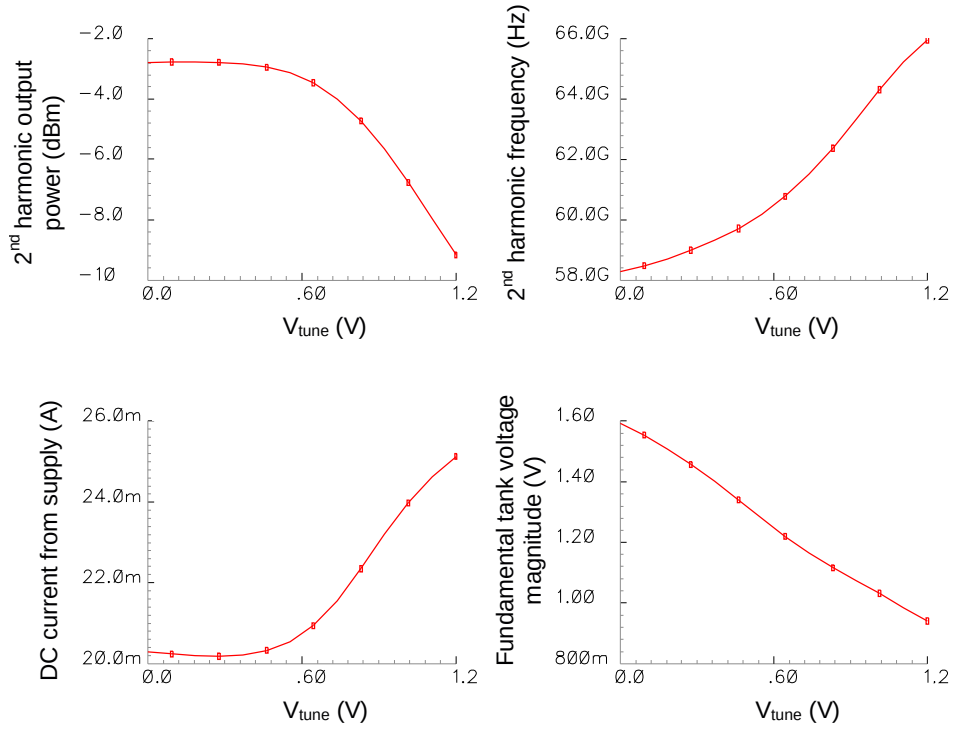


Figure 3-18. Simulated VCO performance with L_{shunt} (with improved output power).

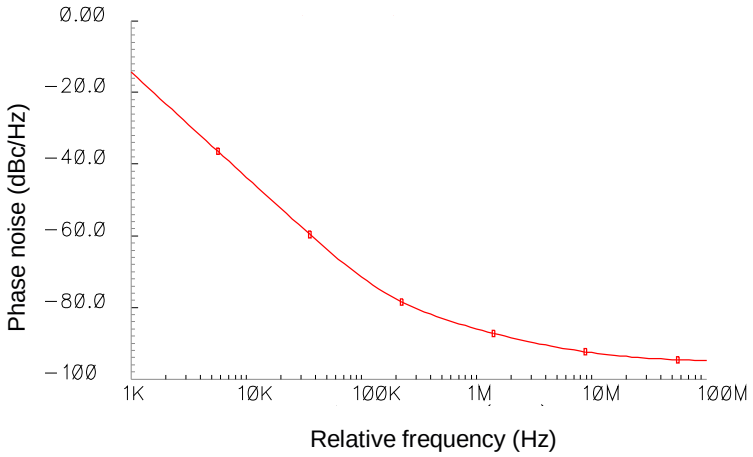


Figure 3-19. Simulated VCO phase noise relative to 2nd harmonic.

The same VCO was simulated without the presence of L_{shunt}, and the results are shown in Fig. 3-20. As before, the output power is lower when L_{shunt} is removed. However, this time the output power at 60 GHz—achieved when V_{tune} = 0.26 V—is substantially lower, by about 9 dB, indicating that the effect of L_{shunt} can be significantly affected by the values of other components of the VCO. The DC current from the voltage supply is also higher than before, by about 8 mA.

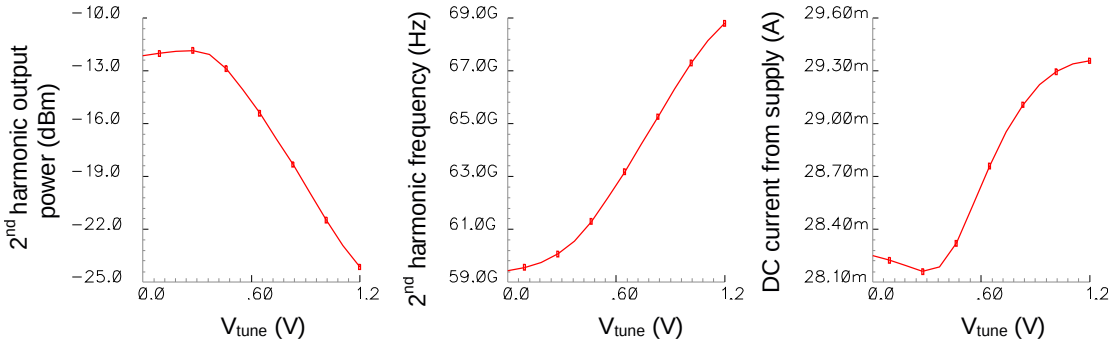


Figure 3-20. Simulated VCO performance without L_{shunt} (with improved output power).

3.10 VCO and L-C tank layout

The VCO was laid out in a 0.13-µm RF bulk-CMOS process utilizing eight metal layers and designed for a nominal supply voltage of 1.2 V. The proposed layout is shown in Fig. 3-21. To suppress the occurrence of unwanted even-mode oscillations at the fundamental frequency, a relatively high degree of symmetry in the layout has been maintained. Bypass capacitors of various sizes, implemented with MIM structures or MOS varactors, are placed at DC nodes throughout the layout in order to improve the AC grounding of these nodes. As noted before, the coplanar transmission lines implementing L_0 are bent inward in order to reach the V_{DD} pad without introducing excessive parasitic inductance between them. The ground traces of the

transmission lines provide shielding between L_{shunt} and the signal traces of L_0, and their presence is expected to slightly decrease the value of L_{shunt}. A simulation in ASITIC indicated that the coupling factor between L_{shunt} and L_{tank} is very small, indicating that the spacing between these inductors, approximately 90 μm, should be sufficient to avoid unwanted magnetic interaction.

The push-push output of the VCO is routed to the probe pad by means of a coplanar transmission line with a ground shield in order to reduce coupling to the lossy substrate. The characteristic impedance of this line is estimated to be near 50 Ω, which provides a reasonably good match with the resistive load at the output. The output probe pad is placed in a ground-signal-ground configuration in order to allow on-wafer probing with coplanar microwave probes. Including the pads, the overall layout area is roughly 860 μm x 650 μm. For this present design, the differential signals at the fundamental frequency are not tapped, e.g., at the gates of M_1 and M_2, although a future design could conceivably do so.

Two separate L-C tank test structures are also included to enable a direct measurement of the resonant frequency of the tank (Fig. 3-22). One test structure includes only the MOS varactors, while the other also includes the MIM capacitors connected to the tank in order to estimate their effect on the resonant frequency.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 51 of 61

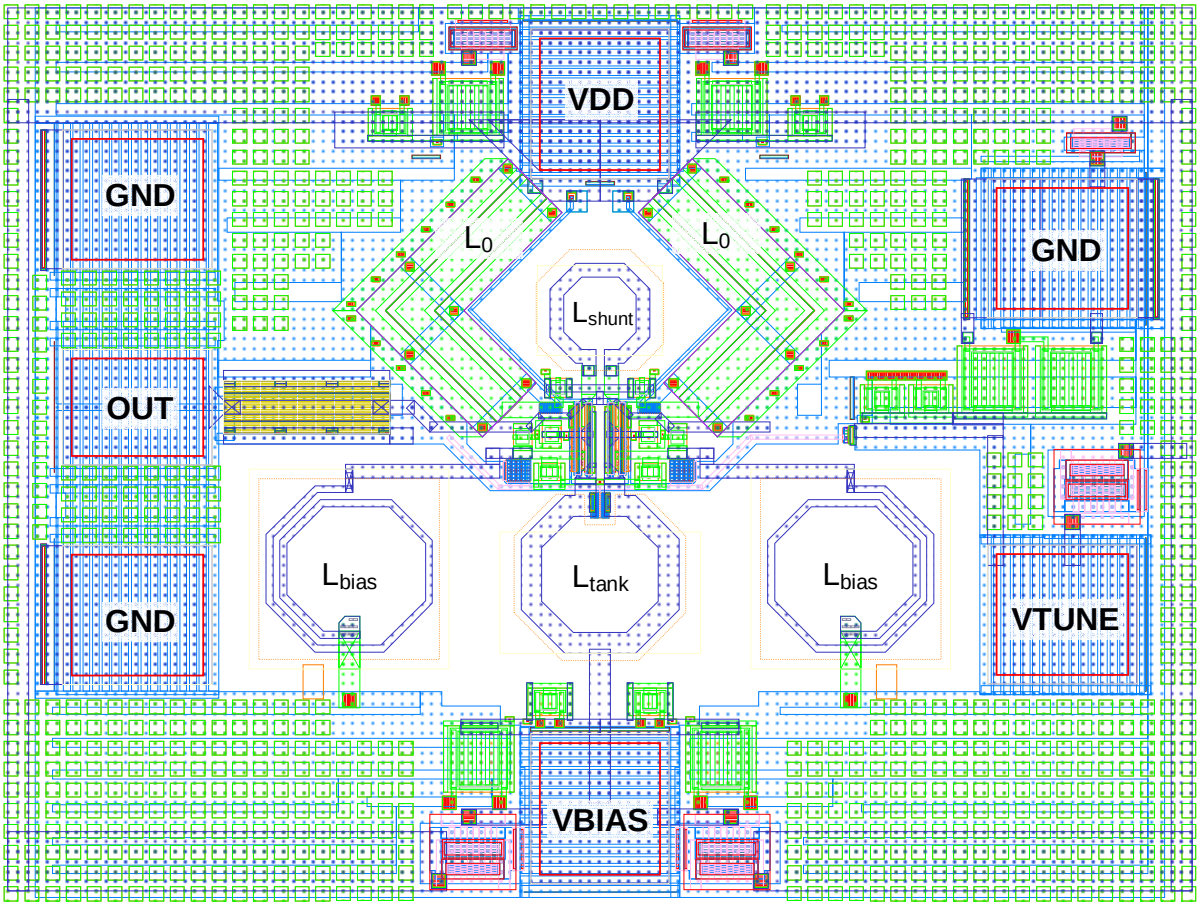


Figure 3-21. Proposed layout of push-push VCO.

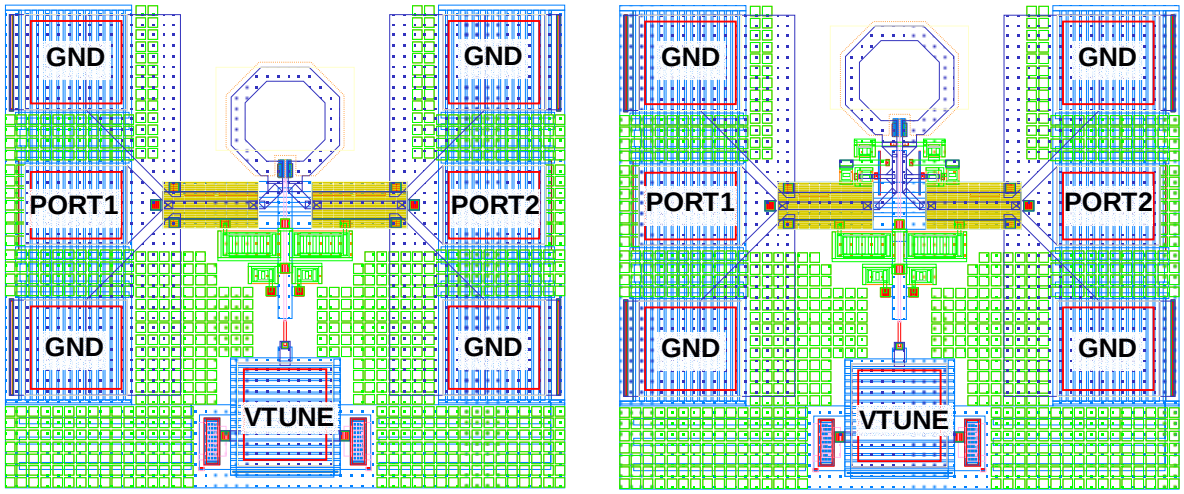


Figure 3-22. Layout of L-C tank structures.

4 Conclusion

The FinFET is a promising candidate to succeed the conventional planar MOSFET as device dimensions scale deeply into the nanometer regime. This work attempts to lay some preliminary groundwork for an evaluation of the RF potential of FinFET technology. Individual test transistors have been laid out for high-frequency measurements, and a static frequency divider has also been designed. S-parameter measurements of these individual transistors will provide a good indication of the intrinsic speed of the technology through the f_{MAX} figure-of-merit. They should also help us to better understand the various sources of device and layout parasitics and their effect on f_{MAX} and other aspects of device performance. High-frequency S-parameter measurements are also useful in the development of a high-frequency transistor model, whether a large-signal BSIM-family model or a lumped-element, bias-dependent small-signal model. In turn, an accurate device model will permit more accurate circuit design of various RF blocks. A static frequency divider is a good circuit to test the speed of the technology, but successful operation may be difficult to achieve at the present time due to fabrication challenges.

Although advanced technologies such as the FinFET hold promise for future high-speed circuit applications, such as millimeter-wave integrated-circuit transceiver design, numerous functional circuits in conventional CMOS have already been demonstrated at microwave frequencies. The design of a push-push CMOS VCO has been described in this report. Although this present design utilizes only the single-ended second-harmonic output, it can be modified to also tap the differential output at the fundamental frequency. In this way, the push-push topology can perhaps obviate the need for one stage of frequency division when used in a phase-locked

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 53 of 61

loop. Various issues involved in the design of the VCO, especially those related to the design and modeling of the passive elements, have been discussed in this report.

ADVANCED MICRO DEVICES, INC. IPR2023-00788 Ex. 1006, p. 54 of 61

Appendix A—Description of FinFET test structures

Unrotated frequency dividers:

1A: L_{drawn} = 0.30 μm, one metal layer, small bypass caps
1B: L_{drawn} = 0.285 μm, one metal layer, small bypass caps
2A: L_{drawn} = 0.285 μm, two metal layers, small bypass caps
3A: L_{drawn} = 0.285 μm, one metal layer, large bypass caps, added symmetry

Rotated frequency dividers:

1C: L_{drawn} = 0.285 μm, one metal layer, small bypass caps
1D: L_{drawn} = 0.285 μm, one metal layer, large bypass caps
2B: L_{drawn} = 0.285 μm, two metal layers, large bypass caps
2C: L_{drawn} = 0.285 μm, two metal layers, small bypass caps
3B: L_{drawn} = 0.285 μm, one metal layer, large bypass caps, added symmetry

Unrotated NMOS FinFETs, one metal layer:

MM1: L_{drawn} = 0.30 μm, W = 60 μm (600 fins), 3 fins/gate finger, compact
MM2: L_{drawn} = 0.30 μm, W = 60 μm (600 fins), 3 fins/gate finger
MM3: L_{drawn} = 0.30 μm, W = 60 μm (600 fins), 3 fins/gate finger, compact, perpendicular
MM4: L_{drawn} = 0.30 μm, W = 60 μm (600 fins), 6 fins/gate finger, perpendicular
MM7: L_{drawn} = 0.285 μm, W = 60 μm (600 fins), 3 fins/gate finger, compact
MM8: L_{drawn} = 0.285 μm, W = 60 μm (600 fins), 3 fins/gate finger

Rotated versions:

MM1T, MM2T, **MM3T, MM4T, MM7T, MM8T**

Unrotated NMOS FinFETs, two metal layers:

MM5: L_{drawn} = 0.30 μm, W = 60 μm (600 fins), 3 fins/gate finger
MM6: L_{drawn} = 0.30 μm, W = 60 μm (600 fins), 3 fins/gate finger, compact
MM11: L_{drawn} = 0.285 μm, W = 60 μm (600 fins), 3 fins/gate finger

Rotated versions:

MM5T, MM6T, MM11T

De-embedding structures, one metal layer:

OPEN-M1, SHORT-M1, THRU-M1

Rotated versions:

OPEN-M1T, SHORT-M1T, THRU-M1T

De-embedding structures for devices MM3 and MM4:

OPEN-M1-TALL, SHORT-M1-TALL, THRU-M1-TALL

Rotated versions:

OPEN-M1-TALLT, SHORT-M1-TALLT, THRU-M1-TALLT

De-embedding structures, two metal layers:

OPEN-M2, SHORT-M2, THRU-M2

Appendix B—Comparison of HFSS results to measured data

To evaluate the accuracy of HFSS in simulating integrated passives, a comparison was made between HFSS results and measured, de-embedded data from a recent 90-nm CMOS test chip (generously made available by Mounir Bohsali). Shown in Fig. B-1, the first structure is a loop inductor utilizing the top metal layer of the process. To simplify the simulation, the entire multi-level dielectric stack was lumped into two layers, representing the passivation layer and the rest of the dielectric stack. A simple ground plane was placed underneath the two lumped ports to account for the presence of a ground plane in the actual test structure, although the layout of the actual ground plane is more complex. A bulk conductivity of 100 S/m was assigned to the substrate, since the actual value was not provided in the process documentation, to the author's knowledge. A comparison of the measured and simulated inductance and Q-factor of the inductor, when excited differentially, is shown in Fig B-2. Overall, there is good agreement in both the inductance and Q-factor.

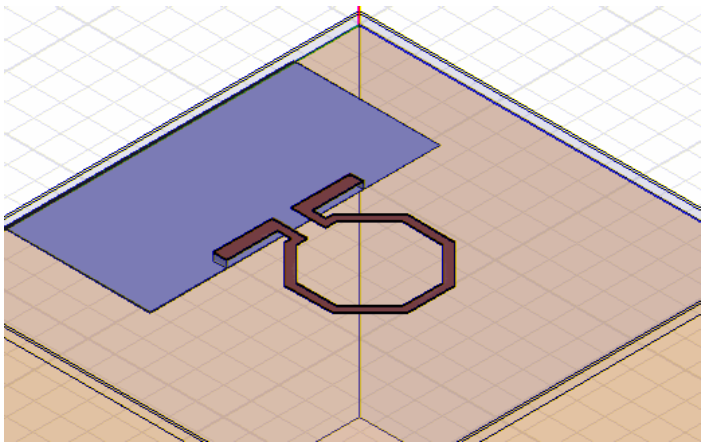


Figure B-1. HFSS model of loop inductor on test chip.

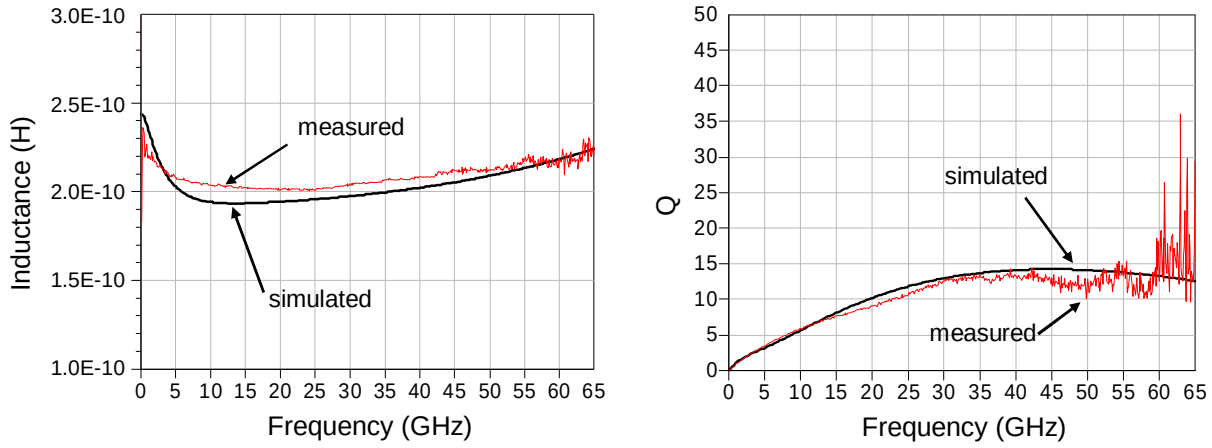


Figure B-2. Comparison of measured and simulated results for test-chip inductor.

The second structure simulated in HFSS is a resonant tank consisting of the same inductor in parallel with a capacitor. In the test chip, the capacitor is implemented as an interdigitated finger capacitor, with each finger comprising the bottom five metal layers strapped together. However, to simplify the structure in HFSS, a simple horizontal parallel-plate capacitor was used instead. To obtain a similar value of capacitance as the finger capacitor, a high-k dielectric was sandwiched between the two plates. The value of k was adjusted to resonate the tank at a similar frequency as the actual tank. Plots of the tank impedance magnitude and phase are shown in Fig. B-3. As expected, the simulated and measured tank impedances agree fairly well, showing that even with a simple capacitor model a reasonably accurate simulation can be performed. The challenge lies in making sure that the simulated capacitor has a similar capacitance as the fabricated capacitor. Also, in cases where the inductor Q is high enough such that the capacitor Q has a significant effect on the overall tank Q, then the Q of the simulated capacitor may also be of concern.

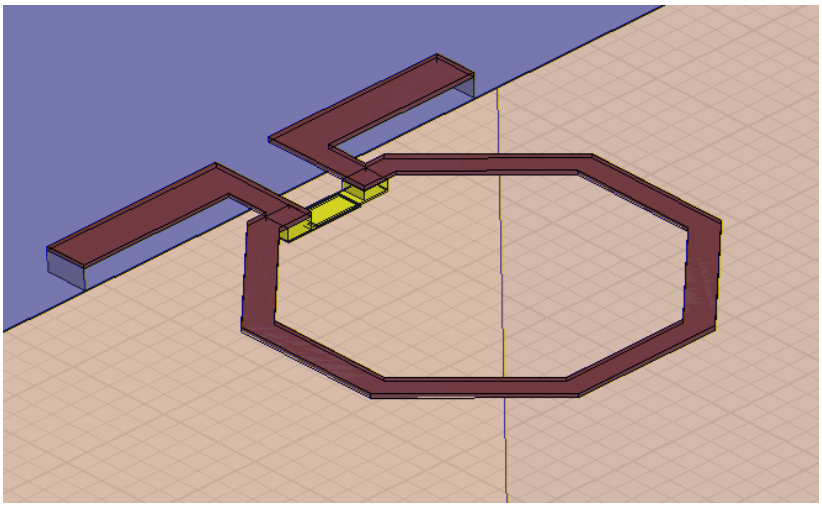


Figure B-3. HFSS model of parallel resonant tank on test chip.

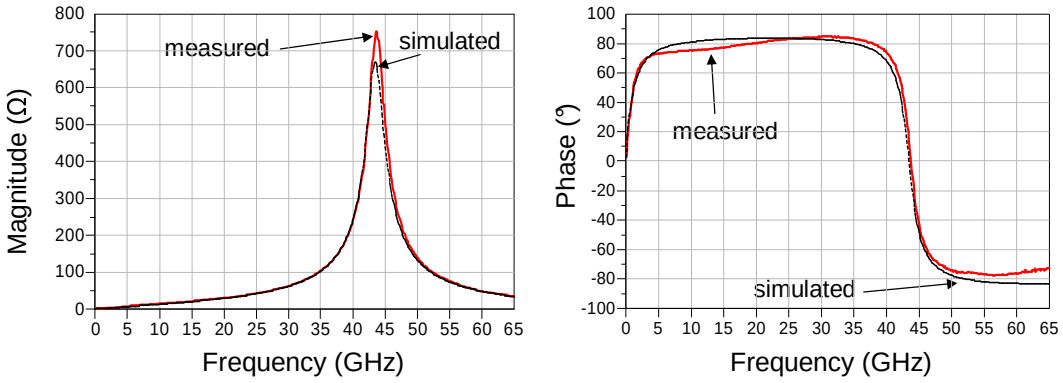


Figure B-4. Comparison of measured and simulated impedance of resonant tank.

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