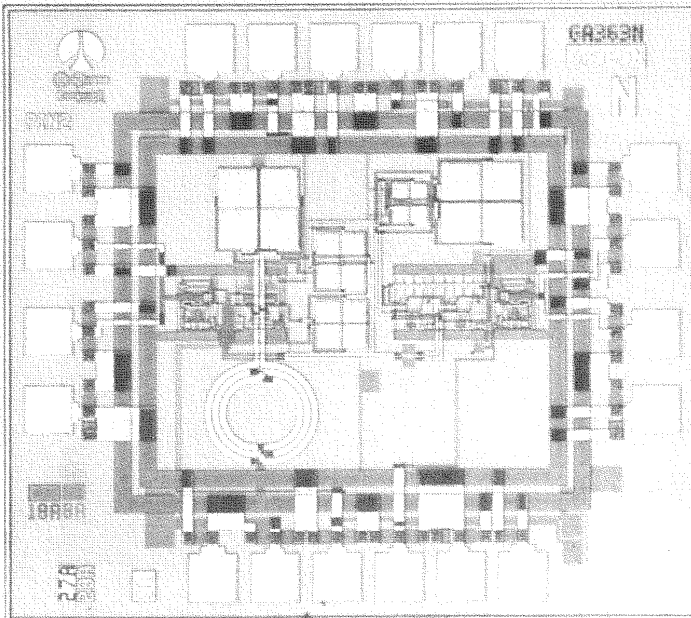


Design, Simulation and Applications of

Inductors and Transformers for Si RF ICs

Ali M. Niknejad
Robert G. Meyer



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I

**ANALYSIS AND SIMULATION OF PASSIVE
DEVICES**

Chapter 1

INTRODUCTION

1. INTRODUCTION

The wireless communication revolution has spawned a revival of interest in the design and optimization of radio transceivers. Passive elements such as inductors, capacitors, and transformers play a critical part in today's transceivers. In this book we will focus on the analysis and applications of such devices. In particular, we will demonstrate techniques for calculating the loss when such devices are fabricated in the vicinity of conductive substrates such as Silicon.

2. PASSIVE DEVICES IN EARLY INTEGRATED CIRCUITS

Until recently, passive devices, especially in integrated form, played a relatively minor role in Si integrated circuits in comparison with active devices such as transistors. The most important reason for this can be attributed to the size difference. Active devices were continually shrinking and occupying less and less chip area whereas passive devices remained large. At low frequencies, circuit designers employed simulated passive devices as much as possible to make their products more compact and reliable.

While it was possible to fabricate small values of capacitance on-chip, inductors were virtually impossible due to the large physical area required to obtain sufficient inductance at a given frequency. This was compounded by the losses in the substrate which made it virtually impossible to fabricate high quality devices. Small Si die were desirable to keep costs low and to improve reliability since larger die resulted in lower yields [Gray and Meyer, 1993].

When passive devices were needed, usually they were connected externally on-board rather than on-chip. This is possible as long as few external components are needed and the package parasitics are negligible in comparison with

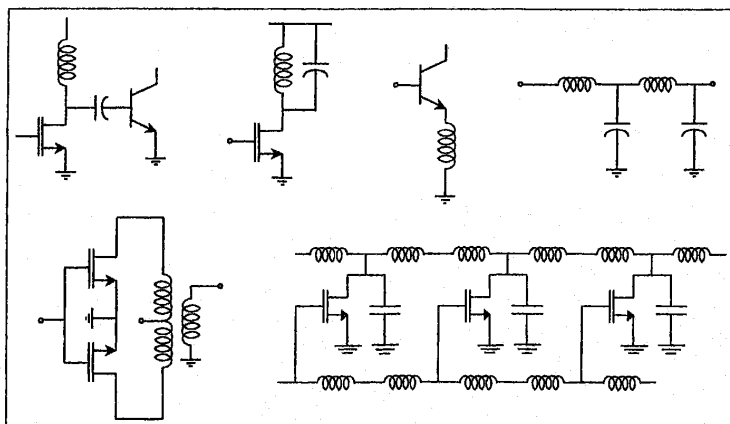


Figure 1.1. Applications of passive devices in Si IC building blocks. (a) Impedance matching. (b) Tuned load. (c) Emitter degeneration. (d) Filtering. (e) Balun. (f) Distributed amplifier.

the external electrical characteristics of the device. Take, for instance, a VCO at 100 MHz versus a VCO at 10 GHz. At 100 MHz a typical tank inductance value will be on the order of 100 nH whereas at 10 GHz the tank inductance is around 1 nH. To access a 1 nH inductor externally is impossible in standard low cost packaging since the package pin and bond wire inductance can exceed 1 nH. Also, as more and more functionality is integrated on-chip, more and more passive devices are needed requiring larger packages which increase the cost. These issues have led to a surge of recent interest in integrated passive devices.

3. APPLICATIONS OF PASSIVE DEVICES

Passive devices, such as inductors and transformers, play an integral part in the performance of circuit building blocks, especially at high frequency. Inductors can be avoided at lower frequencies by using simulated inductances employing active devices. Simulated inductors are more difficult to realize at higher frequencies as active device gain drops. In addition, simulated inductors have finite dynamic range, require voltage headroom to operate, and inject additional noise into the circuits. These limitations place a severe restriction on their application, especially in highly sensitive analog building blocks.

In Fig. 1.1 we see several common applications of inductors, capacitors, and transformers in wireless building block circuits. In (a) we see a narrow-band impedance matching example. Here the input impedance of the second transi-

tor is matched to an optimal impedance value desired by the driving transistor. For instance, in a power amplifier the input impedance of a large output stage device is low due to the capacitance and to obtain sufficient power gain this low impedance is transformed into a larger value. Impedance matching allows circuit designers to obtain minimal noise, maximum gain, minimal reflections, and optimal efficiency when designing circuit building blocks such as low-noise amplifiers (LNAs), frequency-translation circuits (mixers), and amplifiers.

In (b) we see an LC tuned load. A tuned load can take the place of a resistive load to obtain gain at high frequency. The advantages are clear as an LC passive is less noisy than a resistor, consumes less voltage headroom, and obtains a larger impedance at high frequency. A resistive load is always limited by the RC time constant which limits the frequency response. Tuned loads are also a critical component of oscillators. The LC tank tunes the center frequency of the oscillator and the intrinsic Q allows the tank to oscillate with minimal power injection (and hence noise) from the driving transistor.

In (c) an inductor is used as a series-feedback element. Series feedback can be used to increase the input impedance, stabilize the gain, and lower the non-linearity of the amplifier. By using an inductor in place of a resistor, less voltage headroom is consumed, and less additional noise is injected into the circuit. The inductance can also be used to obtain a real input impedance at a particular frequency, thus providing an impedance match at the input of the amplifier.

In (d) inductors and capacitors are used to realize a low-pass filter. Filters of this type are superior to active filter realizations such as gm-C or MOSFET-C filters as they operate at higher frequencies, have higher dynamic range due to the intrinsic linearity of the passive devices, and inject less noise while requiring no DC power to operate.

In (e) we see a center-tapped transformer serving as a balun, a device which converts a differential signal into a single-ended signal to drive external components. Differential operation is advantageous in the on-chip environment due to the intrinsic noise rejection and isolation. Off-chip components, such as SAW filters, though, are single-ended and a balun is needed to convert external single-ended signals to on-chip differential signals.

Finally, in (f) we see inductors and capacitors forming an artificial transmission line in a distributed (traveling-wave) amplifier. Since the LC network acts like a transmission line, it has a broadband response. A wave propagating on the gate-line is amplified and transferred onto the drain line. If the wave speed on the drain line matches the gate line, the signals on the drain line add in phase and the drain line delivers power into a matched load.

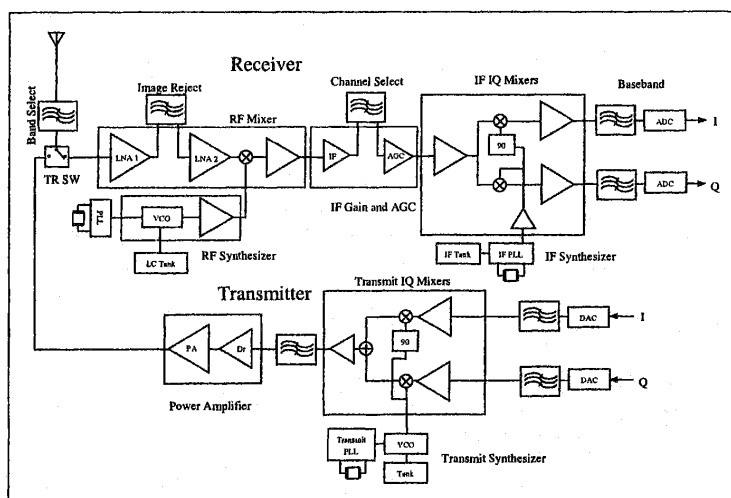


Figure 1.2. Traditional superheterodyne transceiver architecture.

4. WIRELESS COMMUNICATION

The wireless transceiver serves as an excellent example of a system which employs passive devices. In recent times, several factors have contributed to the possibility of portable wireless communications. Continuing technology improvements have enabled low-cost Si circuits to operate in the 1–10 GHz frequency range. In this frequency range efficient portable antennas can be realized since the free-space wavelength is on the order of centimeters. Higher frequencies also allow higher bandwidths to be realized for increased throughput or an increase in the number of users sharing the spectrum. Furthermore, by limiting the transmit power, transceivers which are physically remote can reuse the same spectrum with minimal interference leading to the cellular concept of communication. Finally, at these higher frequencies the critical passive elements, such as inductors and capacitors, are small enough to be realized on-chip.

To see the importance of passive devices, consider the simplified block diagram of a traditional superheterodyne transceiver shown in Fig. 1.2. Note that this transceiver is realized as several different chips or modules and many components of this transceiver are off-chip discrete components. This transceiver is thus bulky and expensive. The goal of many research projects has been to realize this transceiver in a more integrated form [Rudell et al., 1997, Rofougaran

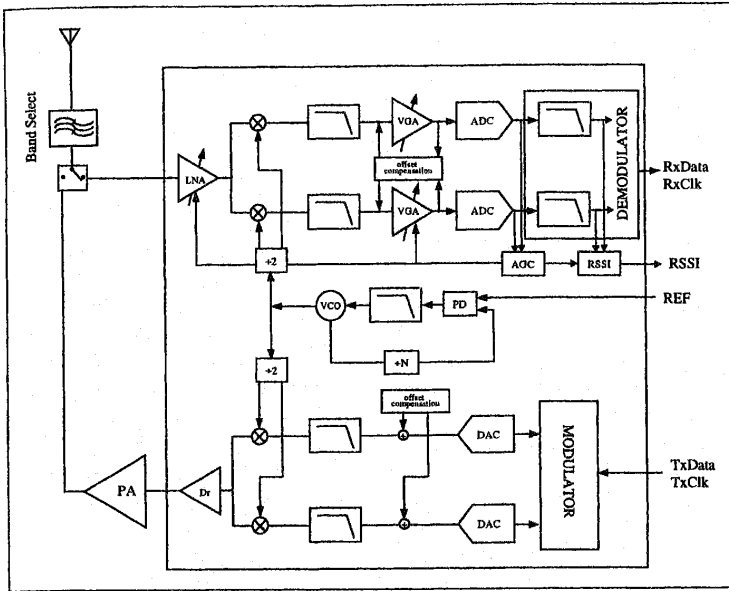


Figure 1.3. Zero-IF direct conversion receiver architecture transceiver.

et al., 1998a, Rofougaran et al., 1998b, Steyaert et al., 1998]. To realize this goal, many off-chip components must be integrated and the inductor is one such key element.

Now contrast Fig. 1.2 with Fig. 1.3 [Eynde et al., 2000], a modern integrated transceiver with minimal off-chip components. Here system architecture innovations such as a zero-IF direct conversion receiver topology eliminates or reduces the need for external filtering. The LNA and VCO tank and the external PLL have also been integrated onto a single chip. The IF is sampled at baseband and digital processing of the signal is performed on the same die. The integrated inductor plays an important role in impedance matching, gain, tuning, and filtering. For instance, in the low noise amplifier (LNA) inductors are used for a real input impedance match and as a narrow-band high impedance load. Here, a resistor is precluded because of the extra noise and voltage headroom required. In the voltage controlled oscillator (VCO) inductors and capacitors form the tuned load of the tank while varactors are used to tune the center frequency to provide a fixed IF frequency. High quality (Q) factor passives limit the phase noise of the VCO which can degrade the receiver sensitivity through

reciprocal mixing. The high Q passives also minimize power leaking into adjacent channels which desensitizes other receiver units in nearby channels. On the transmit side, passives are used in the driver and power amplifier (PA) for impedance matching and gain. Impedance matching allows the power hungry PAs to operate at maximum efficiency and thus extends battery life.

One of the key difficulties in realizing an integrated transceiver lies in the difficult specifications that a transceiver must meet. The harsh wireless environment puts stringent requirements on the dynamic range requirements of the receiver. Since signal strength can vary by many orders of magnitude as mobile users move close to and far from the base station antenna, the transceiver must be able to operate with both extremely small signals close to the intrinsic noise floor of the transceiver and with extremely large signals which excite the desensitizing non-linearities of active devices. Furthermore, these constraints must be met while consuming very low power levels to extend battery life.

Thus, the fully integrated transceiver introduces several new problems. Low power and low noise operation requires the realization of high Q passive devices. Integration introduces parasitic coupling between the various circuit blocks. Within the analog portion parasitic coupling from the powerful transmit circuitry to the sensitive receive path is particularly worrisome. The coupling from the noisy digital blocks to the sensitive analog blocks is also a big concern. Note that this coupling occurs primarily through the package and through the substrate.

5. SI INTEGRATED CIRCUIT TECHNOLOGY

Si technology is a prime candidate for realizing future integrated circuits. While GaAs offers superior gain, higher frequencies of operation, and an insulating substrate, the difference in cost alone favors Si. In addition, emerging advances in Si technology (such as SiGe) are closing the gap between Si and GaAs in performance for the mass commercial market target in the 1–10 GHz frequency range.

When we also consider the potential to integrate digital functionality in CMOS or BiCMOS technology, Si is again the clear winner. Furthermore, due to the mass digital microprocessor and DSP markets, CMOS technology continues to improve. Thus, there are great benefits to integrating passive devices in CMOS technology. Consider the unity gain frequency of an NMOS transistor [Gray and Meyer, 1993]

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs}} = 1.5 \frac{\mu_n}{2\pi L^2} (V_{GS} - V_t) \quad (1.1)$$

and the similar expression for a bipolar transistor

$$f_T = 2 \frac{\mu_n}{2\pi W_B^2} V_T \quad (1.2)$$

Since the vertical base width of a bipolar transistor W_B is determined by a diffusion process whereas the lateral channel length L of an MOS transistor is determined by lithographic processes, bipolar transistors have enjoyed a superiority in speed. New advances in lithographic technology, though, have narrowed the channel length tremendously as MOS technology is the core of the worldwide digital market. Even taking into account that narrow channel device f_T have $1/L$ dependence as opposed to the $1/L^2$ dependence, CMOS technology is today a viable and cost-effective alternative to both bipolar and GaAs and will probably continue to be so for the next decade or longer.

From the perspective of cost, CMOS is the clear winner. But from the perspective of integrated passive devices, GaAs is clearly superior to standard Si. The reason for this stems from the insulating nature of the GaAs substrate which allows very high Q factor passives to be realized on-chip. The dominant limitation in performance is the metal conductivity whereas in Si the dominant loss mechanism at high frequency is the conductive substrate. Electromagnetic energy couples to the substrate and the lossy nature of the Si substrate limits the Q severely.

This is especially the case when the substrate is heavily conductive, as with epi CMOS substrates. Here, magnetically induced eddy currents in the substrate can be a dominant loss mechanism. For moderately conductive substrates, though, electrically induced substrate currents are the dominant loss mechanisms at frequencies below the self-resonant frequency of the device.

6. CONTRIBUTIONS OF THIS RESEARCH

This research has focused on the analysis, design, and applications of passive devices. In Part I emphasis is placed on analyzing inductors and transformers. The solution techniques developed can be easily applied to integrated capacitors and resistors. A general approach is developed from Maxwell's equations to determine the partial inductance and capacitance matrix of an arbitrary arrangement of conductors situated on top of a stratified conductive substrate. The lossy nature of the underlying substrate and losses in the conductors leads to complex capacitance and inductance matrices. These techniques have culminated in a design and analysis software tool called *ASITIC*, "Analysis and Simulation of Inductors and Transformers for ICs." These general techniques can also be applied to extracting the substrate coupling occurring between metal structures residing in the substrate or in the oxide layers on top of the Silicon. This technique is a direct extension of [Gharpurey and Meyer, 1996].

In Part II of the book, we focus on some key applications of passive devices, such as voltage-controlled oscillators and power amplifiers. We show that key performance parameters such as phase noise and power amplifier efficiency depend on the quality of the passive devices. Thus, it is critical to be able to predict the performance of such structures.

Chapter 2

PROBLEM DESCRIPTION

1. DEFINITION OF PASSIVE DEVICES

Consider an arbitrary black box shown in Fig. 2.1 with an arbitrary number of externally accessible terminals. Sample “black” boxes are also shown in the figure. We would like to categorize each black box as passive or active.

Intuitively, the distinction between passive and active devices is clear. While passive devices can only consume or store energy, active devices can also supply energy. Thus, with active devices one can obtain power gain though this is impossible for a passive device. In other words, if we inject power into any terminal of a passive device and observe the power flowing into an arbitrary impedance at another terminal of the device, the real power is necessarily less than or equal to the power injected. If we lift this restriction, the device is active.

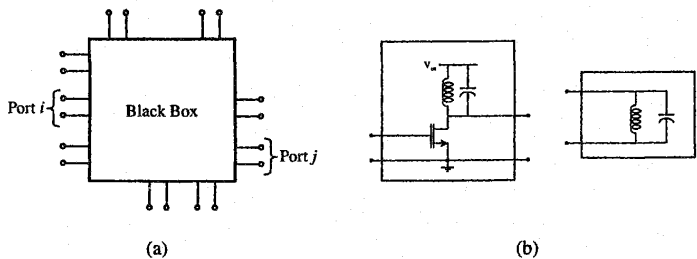


Figure 2.1. (a) An arbitrary black box with externally accessible ports. (b) The contents of two example “black boxes”.

Typical examples of passive devices include linear time-invariant resistors of finite resistance $R > 0$ which dissipate energy, ideal time-invariant linear capacitors and inductors, which only store energy. While the above elements are linear elements, passive elements such as diodes can be non-linear¹. Even though passive devices can have voltage or current gain, they cannot have power gain.

The archetypical example of an active element is of course the transistor and its predecessor, the vacuum tube. Unlike passive devices, such a device can be used to obtain power gain. These devices can be linear or non-linear, but most real world examples are non-linear. The distinction between active and passive is more difficult to make when time-varying elements are employed. For instance, a simple parametric amplifier constructed from a sinusoidally time-varying capacitor in shunt with an RLC tank forms an active device.

A precise definition of passive elements is given in [Desoer and Kuh, 1969]. Given a one-port with port voltage $v(t)$ and port current $i(t)$, the one-port is said to be passive if

$$\int_{t_0}^t v(t')i(t')dt' + \mathcal{E}(t_0) \geq 0 \quad (2.1)$$

where $\mathcal{E}(t_0)$ is the energy stored by the one-port at time t_0 . With application of this definition, one can clearly delineate an element as passive or active.

At high frequencies it is usually more convenient to discuss the scattering matrix S [Carlin and Giordano, 1964]. The power dissipated by an arbitrary port of an n -port is given by

$$P_k = P_{ik} - P_{rk} \quad (2.2)$$

where the subscript i denotes incident power and r denotes reflected power. In terms of the incident and reflected waves we have

$$P_k = a_k \bar{a}_k - b_k \bar{b}_k \quad (2.3)$$

summing over all ports we obtain the total power

$$P = \sum_{k=1}^n P_k = \bar{a}^T a - \bar{b}^T b \quad (2.4)$$

but by the definition of the S matrix $b = Sa$ so that

$$P = \bar{a}^T a - \bar{a}^T \bar{S}^T S a = \bar{a}^T (I - \bar{S}^T S) a = \bar{a}^T Q a \quad (2.5)$$

where Q is the dissipation matrix. Note that

$$\bar{Q}^T = I^T - (\bar{S}^T S)^T = I - \bar{S}^T S = Q \quad (2.6)$$

and so Q is a Hermitian matrix. By definition of passivity, we have

$$P = \bar{a}^T Q a \geq 0 \quad (2.7)$$

Clearly, then, if the matrix Q is positive definite or positive semi-definite, the matrix S corresponds to a passive network. One can also show that this condition implies [Carlin and Giordano, 1964]

$$0 \leq |s_{ij}| \leq 1 \quad (2.8)$$

This can be deduced intuitively in the following manner. Observe that each diagonal entry of the S matrix is the reflection coefficient when all other ports are matched and each off-diagonal component is the transmission coefficient under matched conditions. For a passive network, the conservation of energy implies that the power reflected from any port must be less than the power injected, thus $|\rho|^2 \leq 1$ and the power transmitted similarly must satisfy the same condition, $|\tau|^2 \leq 1$. This implies all matrix elements have magnitude less than or equal to unity and thus reside in the unit circle in the complex plane². An active device consists of a black box with sources, and thus the matrix elements may have magnitude greater than unity. It follows that the real part of the input port impedances may be negative, something that may never occur for a passive network.

1.1 STABILITY AND PASSIVITY

Passivity is closely related to stability [Desoer and Kuh, 1969]. Again, this is clear intuitively as any passive device must be stable by the conservation of energy. In other words, one can never construct an unstable device with purely passive devices. Conditional stability, as with an oscillating LC tank, is possible as long as the initial conditions supply some energy to the tank. It can be shown that a passive circuit is indeed stable and this further implies that any natural frequency of a passive network must lie in the closed left-hand plane, and any $j\omega$ -axis natural frequency must be simple [Desoer and Kuh, 1969].

1.2 RECIPROCITY

Consider the n -port parameters of the black box. If the volume of the black box of Fig. 2.1 is isotropic and encloses no sources, then by the Lorenz reciprocity theorem of electromagnetics it can be shown [Pozar, 1997] that the impedance matrix Z is symmetric. Such a network is called a reciprocal network. A reciprocal network is also described by a symmetric S matrix since in such a case one can show that

$$S = \left(\frac{Z}{Z_0} + I\right)^{-1} \left(\frac{Z}{Z_0} - I\right) = \left(\frac{Z}{Z_0} - I\right) \left(\frac{Z}{Z_0} + I\right)^{-1} \quad (2.9)$$

where Z_0 is the system impedance, usually 50Ω , and I is the identity matrix. If Z is symmetric, then the symmetry of S follows.

It should be noted that reciprocity has nothing to do with passivity. While many passive networks are indeed reciprocal, the connection is not obvious. Any linear time-invariant RLCM network is reciprocal. In fact, some of the elements may be active and reciprocity is still satisfied. A gyrator, a passive device, is non-reciprocal. The reciprocity theorem in circuits follows from excluding any network with gyrators, dependent and independent sources.

1.3 THE QUALITY OF PASSIVE DEVICES

In general, the complex power delivered to a one-port black box network at some frequency ω is given by [Pozar, 1997]

$$P = \frac{1}{2} \oint_S \mathbf{E} \times \mathbf{H}^* \cdot d\mathbf{s} = P_l + 2j\omega(W_m - W_e) \quad (2.10)$$

where P_l represents the average power dissipated by the network and W_m and W_e represent the time average of the stored magnetic and electric energy, respectively. One can define the input impedance as follows [Pozar, 1997]

$$Z_{in} = R + jX = \frac{V}{I} = \frac{VI^*}{|I|^2} = \frac{P}{\frac{1}{2}|I|^2} = \frac{P_l + 2j\omega(W_m - W_e)}{\frac{1}{2}|I|^2} \quad (2.11)$$

If $W_m > W_e$ the device acts inductively whereas if the opposite is true the device acts capacitively.

An important parameter to consider when discussing passive devices is the quality factor. The quality factor has the following general definition

$$Q = 2\pi \frac{E_{\text{store}}}{E_{\text{diss}}} \quad (2.12)$$

where E_{store} is the energy stored per cycle whereas E_{diss} is the energy dissipated per cycle. Implicit in the above definition is that the device is excited sinusoidally. From (2.11) with T equal to the cycle time

$$Q = 2\pi \frac{(W_m + W_e)}{P_l \times T} = \frac{\omega(W_m + W_e)}{P_l} \quad (2.13)$$

The higher the Q factor, the lower the loss of a passive device. This definition is most pertinent when discussing inductors or capacitors as such devices are meant to store energy while dissipating little to no energy in the process. Thus ideal inductors and capacitors have infinite Q whereas practical devices have finite Q . Applying the above definition to an ideal inductor L where $W_e \equiv 0$ in series with a resistor R , one obtains $Q = \omega L/R$ and similarly to an ideal capacitor C where $W_m \equiv 0$ in series with a resistor, $Q = (\omega CR)^{-1}$.

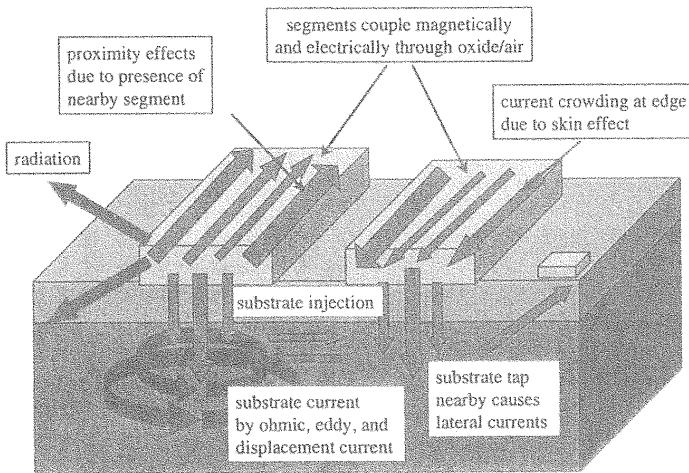


Figure 2.2. Various loss mechanisms present in an IC process.

Physically, the lossy nature of passive devices is rooted in physical phenomena which convert electrical energy into other, unrecoverable forms of energy. Processes which increase entropy are not reversible. For instance, a resistor converts electrical energy into heat. A light bulb converts electrical energy into light and heat. An antenna also converts electrical energy into radiating electromagnetic energy. One can therefore distinguish between passive devices which increase entropy while conserving energy, like a resistor or an incoherent light source, and other devices which conserve energy but do not increase entropy, such as an ideal laser. An ideal laser converts electrical energy into a coherent emission of monochromatic photons. In reality, any physical laser will emit photons with a Lorentzian distribution of energies and thus the entropy of the system increases.

2. LOSS MECHANISMS

The Q factor of integrated passive devices is largely a function of the material properties used to construct the ICs. Specifically, the semiconductor substrate and metal layers used to build the device play the most important roles. The various loss mechanisms are summarized in Fig. 2.2 and discussed further below.

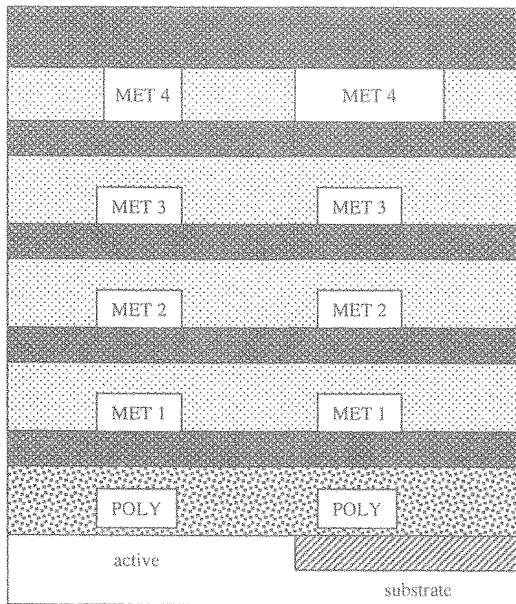


Figure 2.3. Cross-section of metal and polysilicon layers in a typical IC process.

2.1 METAL LOSSES

Passive devices such as inductors and capacitors are constructed from layers of metal, typically aluminum, and polysilicon layers. Hence, the conductivity of such layers plays an integral part in determining the Q factor of such devices, especially at lower frequencies. For instance, a capacitor is constructed by placing two metal conductors in close proximity. Reactive energy is stored in the electric field formed by the charges on such conductors. Since the metal layers are not infinitely conductive, energy is lost to heat in the volume of the conductors. This loss can be represented by a resistor placed in series with the capacitor. Similarly, an inductor is wound using metal conductors of finite conductivity. Most of the reactive energy is stored in the magnetic field of the device, but energy is also lost to heat in the volume of the conductors.

Fig. 2.3 shows a cross-section of the metal layers of a typical modern IC process. Most processes come with three or more interconnection metal layers. This may include one or two layers of polysilicon as well. Some modern CMOS

processes include up to eight metal layers, with the top layer separated from the substrate by $\sim 10\ \mu\text{m}$ of oxide.

Most IC metal layers are constructed from aluminum which has a room temperature conductivity of $\sigma = 3.65 \times 10^7\ \text{S/m}$. Typical metal layers have a thickness ranging from $.5\ \mu\text{m}$ to $4\ \mu\text{m}$, resulting in sheet resistance values from $55\ \text{m}\Omega/\square$ to $7\ \text{m}\Omega/\square$. Even though silver, copper, and gold are more conductive, at $\sigma_{\text{Ag}} = 6.21 \times 10^7\ \text{S/m}$, $\sigma_{\text{Cu}} = 5.88 \times 10^7\ \text{S/m}$, and $\sigma_{\text{Au}} = 4.55 \times 10^7\ \text{S/m}$, aluminum is the more compatible metal in the IC process. Even though Aluminum is prone to spiking and junction penetration [Jaeger, 1993], it is usually mixed with other metals such platinum, palladium, titanium, and tungsten to overcome these limitations. Electromigration in Al is another problem, setting an upper bound on the maximum safe current density. Although electromigration with AC currents is less problematic, it remains one of the important limitations preventing integration of “high-power” passives on Si, such as the matching networks at the output of a power amplifier. The necessary metal width would require excessively large areas resulting in low self-resonant frequencies.

Many IC processes geared for wireless communication applications are now providing a thick top-metal layer option for constructing inductors. Such a metal layer is also useful for high-speed digital building blocks and clock lines and thus this option is widely available in digital processes as well. This top metal layer may also reside on top of an extra thick insulator for minimum capacitance [Kamogawa et al., 1999]. On the other hand, the wealth of interconnection opens up the possibility of designing structures with many different metal layers. This has the added benefit of requiring no extra processing steps as such “3D” interconnection is available with most modern CMOS processes.

At increasingly higher frequencies, even in the absence of the substrate, the current distribution in the metal layers changes due to eddy currents in the metallization, also known as skin and proximity effects, current constriction, and current crowding. At any given frequency, alternating currents take the path of least impedance. Currents tend to accumulate at the outer layer or skin of conductors since magnetic fields of the device penetrate the conductors and produce opposing electric fields within the volume of conductors. When the effective cross-sectional area of the conductors decreases at increasing frequencies, the current density increases, converting more energy into heat. For an isolated conductor, the magnetic fields originate from the conductor itself (the self-inductance). This increase in AC resistance is known as skin effect and typically follows a $\sqrt{f}$ functional dependence. This rate of increase can be traced to the effective depth of penetration δ of the current since the effective area is

a function of the skin depth³

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} \quad (2.14)$$

In a multi-conductor system, the magnetic field in the vicinity of a particular conductor can be written as the sum of two terms, the self-magnetic field and the neighbor-magnetic field⁴. Thus, the increase in resistance of any particular conductor can be attributed not only to skin effect but also to proximity effects, the effect of nearby conductors. If nearby conductors enhance the magnetic field near a given conductor, the AC resistance will increase even further and this is the case for a spiral inductor. On the other hand, if the nearby fields oppose the field of a given conductor, as is the case in a transformer, the AC resistance will decrease as a result.

2.2 SUBSTRATE INDUCED LOSSES

Integrated passive devices must reside near a conductive Si substrate. The substrate is a major source of loss and frequency limitation and this is a direct consequence of the conductive nature of Si as opposed to the insulating nature of GaAs. The Si substrate resistivity varies from 10 k Ω -cm for lightly doped Si (10^{13} atoms/cm³) to .001 Ω -cm for heavily doped Si (10^{20} atoms/cm³). In fact, to combat these substrate induced losses, some researchers propose removing the substrate from under the device by selective etching [Chang et al., 1993] [Lopez-Villegas et al., 2000].

The conducting nature of the Si substrate leads to various forms of loss, namely conversion of electromagnetic energy into heat in the volume of the substrate. To gain physical insight into the problem, we can delineate between three separate loss mechanisms. First, electric energy is coupled to the substrate through displacement current. This displacement current flows through the substrate to nearby grounds, either at the surface of the substrate or at the back-plane of the substrate. Second, induced currents flow in the substrate due to the time-varying magnetic fields penetrating the substrate. These magnetic fields produce time-varying solenoidal electric fields which induce substrate currents. These currents are shown in Fig. 2.4 for the case of a spiral inductor. Note that electrically induced currents flow vertically or laterally, but perpendicular to the spiral segments. Eddy currents, though, flow parallel to the device segments⁵.

Finally, all other loss mechanisms can be lumped into radiation. Electromagnetically induced losses occur at much higher frequencies where the physical dimensions of the device approach the wavelength at the frequency of propagation in the medium of interest. This frequency is actually difficult to quantify due to the various propagation mechanisms of the substrate. For instance, if we consider propagation into air, the free-space wavelength is the appropriate

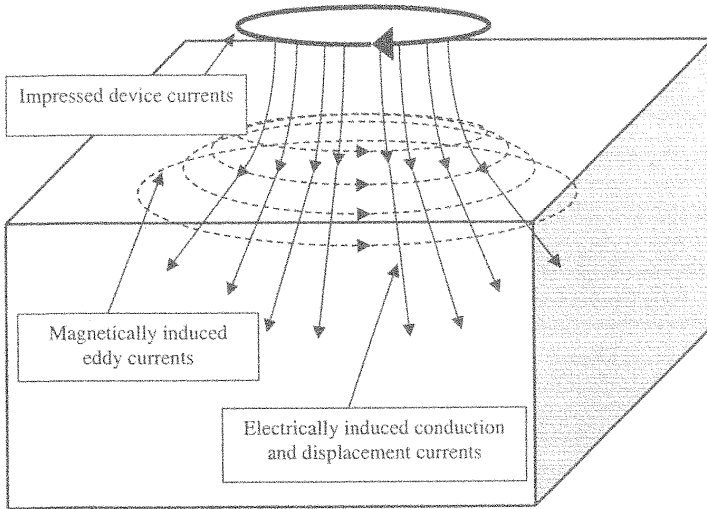


Figure 2.4. Schematic representation of substrate currents. Eddy currents are represented by the dashed lines and electrically induced currents by the solid lines.

factor. Even at 10 GHz, the wavelength in air is 3 cm, much larger than any RF inductor or capacitor. Even at 100 GHz, the wavelength is now 3 mm, still much larger than any device at this frequency. Thus, we can safely ignore the electromagnetic propagation into the air.

Efficient electromagnetic propagation into the substrate, though, occurs at lower frequencies due to the lower propagation speed, roughly at a factor of $\sqrt{\epsilon_{\text{Si}}}$ lower due to the diamagnetic nature of Si. Since $\epsilon \approx 11.9$ in Si, this is slightly slower from propagation in air. Furthermore, due to the lossy nature of the substrate, waves traveling vertically into the surface of the substrate are heavily attenuated. Waves traveling along the surface of the substrate, though, can propagate partially in the lossless oxide and partially in the substrate. For a lightly doped substrate, the wave propagation behaves like a “quasi-TEM” mode. As the substrate is made heavily conductive, the wave is constrained to the oxide and the substrate acts like a lossy ground plane. This is the so-called “skin effect” mode of propagation [Hasegawa et al., 1971]. There is a third kind of possible excitation, the “slow-wave” mode of propagation, where the effective speed of propagation is orders of magnitude slower than propagation in free space [Hasegawa et al., 1971].

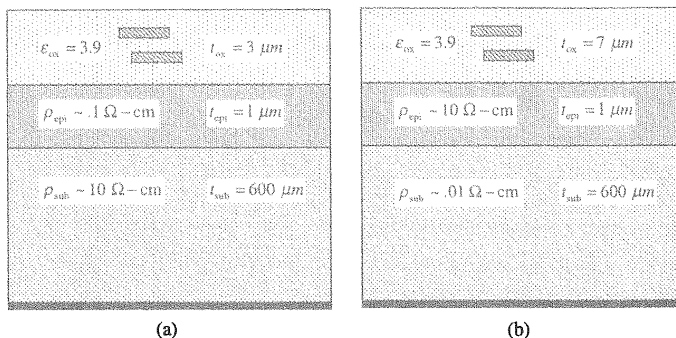


Figure 2.5. Cross-section of typical (a) bipolar and (b) CMOS substrate layers.

2.2.1 SI IC PROCESS SUBSTRATE PROFILE

In Fig. 2.5 typical bipolar and CMOS process substrate profiles are shown. Each substrate consists of one or more layers of Si or a compatible material⁶. Layers of varying conductivity are added to the bulk substrate by various processes, such as diffusion, chemical vapor deposition and growth, epitaxy, and ion implantation. Various layers of oxide (SiO_2 for instance) and polyimide are also grown to provide insulation from the substrate and between metal layers.

In general, the more conductive the substrate layers, the more detrimental the resulting losses. It is therefore no surprise that intrinsic Si substrates⁷ result in the lowest losses [Park et al., 1997b]. Due to the close proximity of the Si substrate to the inductors and transformers residing in the metal layers, the case of an infinitely conductive substrate is also problematic. For a heavily conductive substrate, the magnetic and electric fields do not penetrate the substrate appreciably and even though no substrate induced losses occur, the surface currents flowing in the substrate, acting like “ground-plane” currents, produce opposing magnetic fields which tend to drive the inductance value of coils to low non-usable values.

Therefore, given the choice, designers of ICs and process engineers should ensure that as few as possible conductive substrate layers appear under or near an inductor. This is unfortunately not always possible due to planarization constraints. Furthermore, the thickest possible oxide should be realized under the device to minimize the substrate capacitance. This not only minimizes the losses, but also maximizes the self-resonant frequency of the device. In the limit, self-resonance will occur due to interwinding capacitance as opposed to substrate capacitance. Since interwinding capacitance can be controlled by

increasing the metal spacing, this gives the IC designer more control over the passive device behavior.

Most bipolar and BiCMOS substrates come with a standard 10–20 $\Omega\text{-cm}$ substrate. With this value of resistivity, electrically induced losses dominate the substrate losses in the 1–10 GHz frequency range [Ruehli, 1972]. This is also the case for bulk CMOS substrates with the same range of resistivity. In such a case, one must ensure that no conductive *n*- or *p*-wells appear below the device. This may require a special mask to block the dopants in the well creation process, especially for a twin-well CMOS process. To minimize the chance of latch-up, many modern CMOS processes begin with a heavily conductive thick substrate about 700 μm thick and grow a thin epitaxial layer of resistive Si on the surface to house the wells. This is unfortunate for RF/microwave circuits as the bulk substrate can be as conductive as 10^4 S/m and this can be a major source of substrate induced losses due to eddy currents.

The back-plane of the substrate may or may not be grounded. Even if it is physically grounded for DC signals, AC signals are constrained to flow within several skin depths δ and this factor is a strong function of the conductivity. For heavily conductive substrates, currents are constrained to flow at the surface of the substrate at high frequencies whereas for moderately conductive substrates currents flow deep into the substrate and into the back-plane ground.

A physical ground may be realized if the die (chip) resides in a package with a conductive ground plane, or if the die is bonded directly onto a board, and a conductive epoxy cement glue is used. Although the epoxy is not conductive, metals can be mixed in to produce a conductive solution. In the modeling of the substrate this can be an important factor in enforcing the boundary conditions surrounding the chip.

Unless the substrate thickness is reduced substantially, the conductive back-plane ground is sufficiently distant not to appreciably influence the electromagnetic behavior of the inductor. On the other hand, some packages use “down-bonds,” bond wires from the Si die to the package grounded “paddle”. To minimize the bond wire length, the substrate thickness is reduced in post-processing steps. This has further benefits for a packaged power amplifier since a thinner substrate also has better thermal conductivity. For such a thin, moderately conductive grounded substrate, one must take into account ground “image” currents which can reduce the inductance value and serve as a further loss mechanism [Krafcsik and Dawson, 1986]. If the substrate is sufficiently conductive such that the skin depth δ is much less than the substrate thickness, then image currents will be confined to flow at the substrate surface.

3. DEVICE LAYOUT

In this section we will discuss various ways to lay out inductors using the planar metallization layers of a typical IC process. Off-chip inductors are usu-

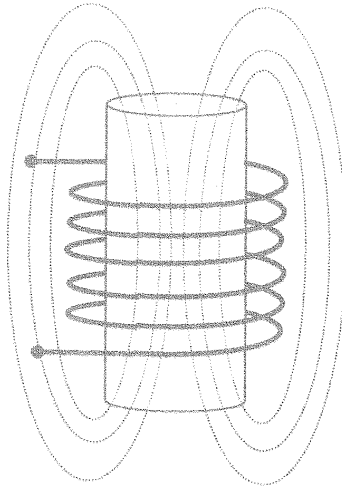


Figure 2.6. The typical coil inductor.

ally realized as a solenoidal coil or toroid, as shown in Fig. 2.6. Each additional turn adds to the magnetic field in phase with the previous turn. The magnetic energy is stored mostly in the inner core of each winding. The inductance is largely a function of the area of the loop and the number of turns in the winding typically resulting in an N^2 dependence.

3.1 PLANAR INDUCTOR STRUCTURES

Since on-chip inductors are constrained to be planar, the typical solution is to form a spiral, as shown in Fig. 2.7. Since some IC processes constrain all angles to be 90° , a square version of the spiral, shown in Fig. 2.8, is a popular alternative. A polygon spiral, as shown in Fig. 2.9, is a compromise between a purely circular spiral and a square spiral.

In designing integrated circuits it is sometimes convenient to tap an inductor at some arbitrary point. While this is certainly possible, as more than one metal layer is present, it is sometimes necessary to tap a spiral in the center, especially for differential circuits. In a spiral it is difficult to find such a symmetric center point since the electric fields on the outer turns tend to fringe and thus the “inductive” center does not correspond to the “capacitive” center. Also, the “inductive” center does not correspond to the “resistive” center due to the non-uniform mutual magnetic coupling. To solve this problem, some researchers

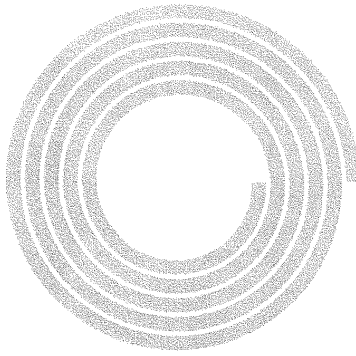


Figure 2.7. A circular spiral inductor.

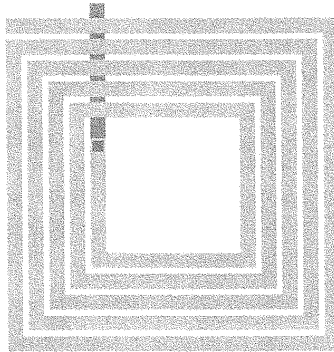


Figure 2.8. A square spiral inductor.

have proposed symmetric structures, such as that shown in Fig. 2.10. Note that each turn involves a metal-level interchange, a process that requires vias. A different center-tapped structure proposed by [Kuhn et al., 1995] requires only one metal interchange. This structure is very similar to a inter-digited planar transformer structure shown in Fig. 2.13. These structures have a natural geometric center which coincides with the electrical center point. This is needed in differential circuits as such points can be grounded or connected to supply

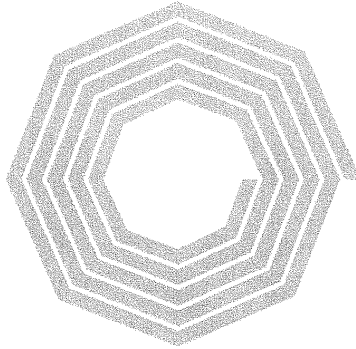


Figure 2.9. A polygon spiral inductor.

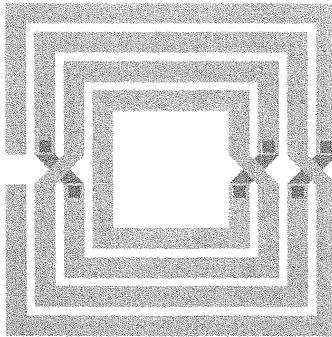


Figure 2.10. A symmetric spiral inductor.

without disturbing the differential signal. Circular or polygon versions are also possible, as shown in Fig. 2.11.

3.2 NON-PLANAR INDUCTOR STRUCTURES

Up to now we have only considered planar structures even though modern IC processes offer many metal layers. Two simple approaches in utilizing the metal layers are to connect multiple spiral inductors in series or in shunt. While N spirals in series increase the series resistance by a factor of approximately N

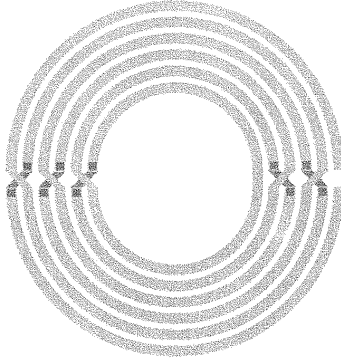


Figure 2.11. A symmetric polygonal spiral inductor.

(neglecting via resistance), the inductance value increases faster due to the mutual magnetic coupling. At low frequencies where the current flowing through each series connected spiral I_j is equal, the effective inductance of N series connected coupled inductors is

$$L_{se} = \sum_{i=1}^N L_i + 2 \sum_{i=1}^N \sum_{j \neq i}^N M_{ij} \quad (2.15)$$

where M_{ij} is the mutual magnetic coupling between each series connected spiral i and j . Thus, the series connection approaches an N^2 increase in inductance and the Q factor can potentially increase by a factor of N for the case of perfectly coupled spirals ($k = 1$).

Alternatively, in the shunt connection, the series resistance drops by a factor of N (assuming equal resistivity in each metal layer and uniform current distribution among the coils) whereas the inductance of mutually coupled inductors drops to⁸

$$L_{sh} = \frac{1}{\sum_{i=1, j=1}^N K_{ij}} \quad (2.16)$$

where the matrix K is the inverse of the partial inductance matrix M . This result certainly agrees with the case of a diagonal matrix M corresponding to zero coupling since in such a case we have the familiar result for parallel inductors

$$L_{sh, k=0} = \frac{1}{\sum_{i=1}^N \frac{1}{M_{ii}}} \quad (2.17)$$

For the case of two coupled inductors we have a simpler relation

$$L_{sh} = \frac{1}{2} \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M} \quad (2.18)$$

For the case of perfectly coupled equal value inductors, with $k = +1$, the above result yields $L_{sh} = L$. For the general case, the matrix M is singular but by symmetry the current flowing through all inductors is equal so the voltage across the j th inductor gives

$$V_j = \sum_{k=1}^N sM_{jk}I_k = \frac{I}{N} \sum_{k=1}^N sM_{jk} = \frac{I}{N} sL \sum_{k=1}^N 1 = sLI \quad (2.19)$$

and so we have

$$L_{sh} = L_1 = L_2 = \dots = L_N \quad (2.20)$$

In this limit, the Q factor also improves by a factor of N due to the drop in series resistance. In practice, both the series and shunt connection offer a Q improvement close to the theoretical limit due to the tight coupling achievable in the on-chip environment. These benefits, though, only occur at low frequencies where the above assumptions hold.

At high frequencies, both approaches are liable to reduce the Q factor over the case of a single layer coil due to the capacitive and substrate effects. The series connection suffers from high interwinding capacitance which lowers the self-resonance frequency lowering the maximum frequency of operation of the device. The shunt connection moves the devices closer to the substrate where capacitive current injection into the substrate may dominate the loss of the device.

Another approach is to attempt to realize a lateral coil on-chip by using the top and bottom metal layers and vias as the side. This approach has been successfully demonstrated in [Young et al., 1997] using special post-processing steps to realize sufficient cross-sectional area in the coil. This approach has the added advantage of positioning the magnetic fields laterally to the substrate where eddy currents are reduced. In a vertical coil or spiral, the magnetic field is strongest at the center of the coil. Due to the finite conductivity of the substrate, these changing magnetic fields leak into the substrate and produce eddy currents. Eddy currents can be a significant source of loss and this technique might be an effective method to combat this loss mechanism. Standard monolithic integration, though, has failed to produce a coil with sufficient cross-sectional area to produce significant Q . Some innovative strategies around this are to employ a combination of metal and bond wires to realize the coil [Lee et al., 1998b]. The work of [Lee et al., 1998b] claims tight tolerance on the inductance value which is a primary concern of using bond wires alone [Craninckx and Steyaert, 1995].

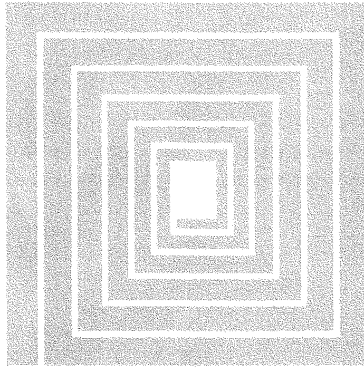


Figure 2.12. A tapered spiral inductor.

3.3 TAPERED SPIRALS

A tapered spiral is shown in Fig. 2.12. The metal pitch and spacing are varied to minimize the current constriction at high frequency [Niknejad, 1997, Lopez-Villegas et al., 2000]. Current constriction, or skin effect, is non-uniform as a function of the location in the spiral due to the non-uniformity of the magnetic field. At low frequencies the current is nearly uniform whereas at high frequency non-uniform current flows due to proximity effects.

The magnetic field is strongest in the center of the spiral [Craninckx and Steyaert, 1997] and thus the time-varying magnetic field produces eddy currents of greatest strength in the volume of conductors near the center of the device. Since at high frequency current constriction limits the current to the outer edges of the conductors, conductor width does not have as strong an influence on minimizing metal losses as at low frequency. For this reason [Craninckx and Steyaert, 1997] advocate removing the inner turns to produce a “hollow” spiral. Another approach is to decrease the width of the inner turns and to effectively move these turns closer to the outer edge. This approach contrasts with the approach suggested by [Lopez-Villegas et al., 2000] where the sum of the metal pitch and spacing, $W + S$, is kept constant.

Tapering is most effective when substrate losses are negligible, as in the case of an insulating substrate. This stems from the fact that current constriction dominates the metallization losses at high frequencies when the substrate losses are also significant. On the other hand, tapering can be an effective means of increasing the self-resonant frequency of a device by decreasing the cross-sectional area of the device.

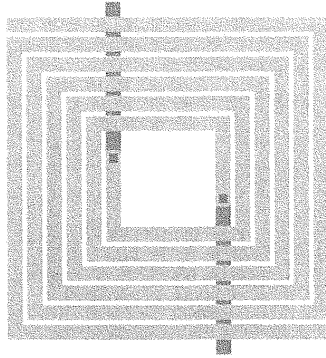


Figure 2.13. A planar square spiral transformer.

3.4 TRANSFORMERS

On-chip transformers are realized very similarly to inductors. To maximize the coupling factor k , two inductors can be interwound as shown in Fig. 2.13. Polygon spirals can be similarly interwound to form transformers. These transformers have equal turns ratio at the primary and secondary. Since the turns ratio n is given by

$$n = k \sqrt{\frac{L_2}{L_1}} \quad (2.21)$$

one way to realize $n \neq 1$ is to alter the number of turns and metal pitch in the secondary. In addition, to lower the losses in the secondary, turns may be connected in shunt [Long and Copeland, 1997]. Typical practical coupling values in the range of $.6 < k < .8$ can be achieved with planar spirals. Metal-metal transformers utilizing two or more metal layers can save area, but cause asymmetry and increased capacitive coupling between the primary and secondary. The asymmetry can be reduced by utilizing a structure such as the one in Fig. 2.14.

If center-tapped transformers are desired, such as in a balun, a structure such as Fig. 2.15 serves well. This structure is formed by interwinding two center-tapped coils of Fig. 2.10.

3.5 SHIELDED STRUCTURES

In an attempt to shield a device from substrate losses, researchers have proposed building a shield with lower metal layers or polysilicon layers to block

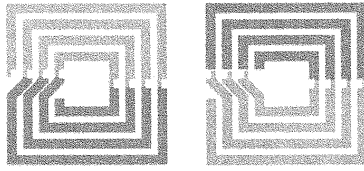


Figure 2.14. An expanded view of a non-planar symmetric spiral transformer. The primary is shown on the left and the secondary on the right. These inductors actually reside on top of one another.

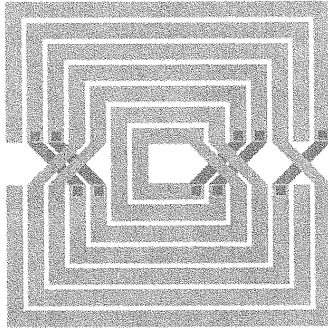


Figure 2.15. A planar symmetric balun transformer.

electromagnetic energy from coupling to the substrate [Yue and Wong, 1997]. While electrostatic shielding works well for capacitors and RF pads, especially at “low-frequencies”, the shield must be patterned in the case of inductors so as to avoid or reduce the effects of eddy currents. Due to the close proximity of the device and the shield, using solid metallization would allow “image” eddy currents to flow which would produce an opposing magnetic field. This would reduce the device magnetic energy storage and hence the Q factor. A patterned shield, similar to Fig. 2.16, only allows shield currents to flow perpendicular to the conductive paths of a spiral inductor, thereby preventing the majority of eddy currents which flow parallel to the device⁹.

The effects of a shield, or any other “grounding” structure, can be analyzed with the techniques presented in this research. At first glance a patterned shield seems like a very effective means of improving the device Q . This, however,

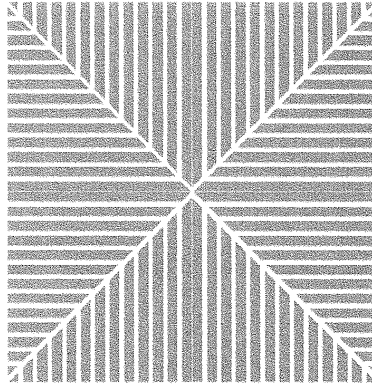


Figure 2.16. A patterned ground shield.

must be carefully examined for each process and product. There are many obvious problems with a shield, such as drastically reduced self-resonant frequency. There are also more subtle problems with a shield.

To see this, consider the inductor layout as a lossy inductor and a parasitic lossy capacitor, C_s in series with a loss resistor R_s . This frequency-independent representation is certainly valid as the network two-port parameters can be transformed into this equivalent circuit uniquely at a given frequency. In practice, the addition of a few elements, such as a lossless interwinding capacitor, broadbands the model, especially below self-resonance [Niknejad, 1997]. Then the action of the shield is to effectively increase the Q_C factor of the capacitor portion of the equivalent circuit. Consider a series to parallel transformation of this lossy capacitor into C_p in shunt with R_p

$$R_p = (1 + Q_C^2)R_s \quad (2.22)$$

$$C_p = \frac{Q_C^2}{1 + Q_C^2}C_s \quad (2.23)$$

Suppose that without a shield the Q_C factor of this capacitor is very low, $Q_C \ll 1$, such that

$$R_{low} \approx R_s \quad (2.24)$$

$$C_{low} \approx Q_C^2 C_s \quad (2.25)$$

If R_{low} is then already larger than the parallel equivalent inductor loss resistor, then this capacitor plays a minor role in determining the overall Q and shielding will actually deteriorate the performance of the device. Note that since

$C_{low} \ll C_s$, the effective shunt capacitance is small and does not lower the self-resonant frequency of the device. Clearly, in this case shielding does not help. Now consider the other extreme where the resistor R_{ow} actually loads the tank significantly. Then clearly increasing the capacitor Q_C factor helps since for $Q_C \gg 1$

$$R_{high} \approx Q_C^2 R_s \quad (2.26)$$

$$C_{high} \approx C_s \quad (2.27)$$

This occurs, on the other hand, at the expense of lowered self-resonance since now the parasitic capacitor loads the tank. So we see the shield may potentially improve the overall tank Q but at the cost of reducing the usable frequency range of the device. Another approach, discussed in [Burghartz et al., 1997], surrounds the device with an open halo of substrate contacts. This has the added benefit of increasing the capacitor Q_C without loading the tank capacitance significantly. Measurements by other researchers have also corroborated these findings [Yoshitomi et al., 9998].

Another potential problem with the shield arises due to finite non-zero ground inductance. Since most packaged ICs suffer both package and bond wire inductance, the actual zero potential resides off-chip and there is considerable “ground bounce” on-chip. A typical IC has several inductors and transformers and if they are shielded, they are all effectively tied to a common non-zero impedance point. Thus a parasitic coupling path exists from device to device.

For instance, in an amplifier, this intra-block leakage can either lower the gain (as negative feedback) or cause instability (as positive feedback). Inter-block coupling, on the other hand, can produce spectral leakage and spurs, jamming and reduced SNR (gain compression), or mode-locking.

Any IC, of course, suffers from parasitic substrate coupling but shielding increases the substrate capacitance value and removes the resistive isolation between the devices.

3.6 VARACTORS (REVERSE-BIASED DIODES)

Varactors, or variable capacitors, are usually constructed as back-biased diodes. Diodes are realized as junctions between p -type and n -type doped regions of Si. Briefly, the presence of an n -type region abutting a p -type region creates a large concentration gradient which leads to diffusion. This diffusion forms the so-called “space-charge” or “depletion” region, a charged volume of space surrounding the junction. The charge of this region is due to the charge of immobile dopant sites. Donor or acceptor atoms are easily ionized at room temperature resulting in free mobile carriers. The diffusion process is balanced by the conduction current resulting from the built-in electric field since the charge buildup from the ionized immobile dopants produces an electric field

opposing the diffusion. Thus a natural barrier is formed against charge crossing the junction boundary.

If the diode is forward biased beyond a threshold, carriers obtain sufficient energy to cross the barrier. On the other hand, if the diode is reverse-biased, no DC conduction current flows. In reality, a small current will flow even under reverse-biased conditions. One contribution to these "leakage currents" is due to minority carriers which are created on average within a diffusion length of the junction. These carriers are actually propelled by the built-in electric field and cross the junction. Note that this current is relatively bias-independent¹⁰.

While little to no DC current flows, AC displacement currents can flow since the reverse-biased diode acts very much like a capacitor. The thin space-charge region serves as the "insulator" and the n -type and p -type Si regions act as capacitor plates. Electric energy is stored in the built-in field of the space-charge region. Under an abrupt junction assumption, the depletion region thickness is given by [Neudeck, 1989]

$$d_j = \left[\frac{2K_S \epsilon_0 (V_{bi} - V_A) (N_A + N_D)}{q N_A N_D} \right]^{1/2} \quad (2.28)$$

N_D and N_A are the donor and acceptor volume densities and V_{bi} is the built-in potential given by

$$V_{bi} = \frac{kT}{q} \ln \left[\frac{N_D N_A}{n_i^2} \right] \quad (2.29)$$

where complete ionization of the donors and acceptor is assumed. Note that under reverse-biased conditions, the spacing d_j is a function of the applied voltage $V_A < 0$. This effect can be exploited to produce a variable capacitor. The physical origin of the dependence of d_j on V_{rev} is simply due to the fact that increasing the voltage difference increases the electric field which requires more charge which in turn comes from extending the space charge region. If $N_D \gg N_A$ then the fractional increase in d_j from the donor side is small compared to the acceptor sites. The opposite, of course, also applies. Thus, in such a case the series resistance of the diode in reverse bias will be dominated by the acceptor side, or the p -type Si, due to its higher resistivity. Note that if both the donor and acceptor densities are increased in an attempt to lower the series losses, the capacitance gets large. While this is desirable, the breakdown voltage of the reverse-biased junction decreases. For avalanche breakdown we have [Neudeck, 1989]

$$V_{BR} = \left(\frac{\epsilon_C T^2 \epsilon_r}{2q} \right) \left[\frac{N_A + N_D}{N_A N_D} \right] \quad (2.30)$$

The same applies for Zener breakdown since decreasing d_j increases the probability that a carrier will tunnel through the potential barrier. Since the operating

voltage of ICs is reducing, a proportional decrease in the breakdown voltage is tolerable allowing lower series resistance and thus higher Q values to be realized.

The equivalent capacitance of a junction with cross-sectional area A is thus given by

$$C_j = \frac{\epsilon_r \epsilon_0 A}{d_j} = \frac{\epsilon_r \epsilon_0}{\left[\frac{2K_S \epsilon_0 (V_{bi} - V_A)}{q} \frac{(N_A + N_D)}{N_A N_D} \right]^{1/2}} \quad (2.31)$$

this can be rewritten as

$$C_j = \frac{C_{j0}}{\left[1 - \frac{V_A}{V_{bi}} \right]^m} \quad (2.32)$$

where C_{j0} is the junction capacitance for the zero applied bias case, $V_A = 0$. The factor m is equal to $1/2$ for an abrupt junction but takes on the value of $1/3$ for a linearly graded junction. For real junctions, one finds that $1/3 < m < 1/2$.

A pertinent factor when designing VCOs and filters with variable cutoff is the derivative of (2.32) with respect to the applied voltage V_A

$$K_{CV} = \frac{C_{j0} m}{V_{bi} (1 - \frac{V_A}{V_{bi}})^{m+1}} \quad (2.33)$$

Increasing this factor is important for maximizing the change in capacitance for a change in the reverse-biased voltage. This maximizes the tuning range of an LC tank, for instance, since

$$\frac{d\omega}{dV} = \frac{-K_{CV}}{2C_j} \omega_0 \quad (2.34)$$

where $\omega_0 = \sqrt{1/LC_j}$.

3.7 MOS CAPACITORS

Another technique to realize a variable capacitor is through an MOS capacitor. The MOS capacitor has four distinct regions of operation: accumulation, depletion, weak inversion, and strong inversion. In accumulation mode, the capacitance is equal to the oxide capacitance

$$C_{acc} = C_{ox} = \frac{\epsilon_r \epsilon_0 A}{t_{ox}} \quad (2.35)$$

where t_{ox} is the gate oxide thickness and A is the capacitor plate area. This assumes that majority carrier distribution equilibrates much faster than the period of the applied signal. We also assume that all the charge resides at the surface of the substrate (delta-function approximation for charge density) and we neglect the fringing fields. In reality, the charge distribution will not peak

at the surface but slightly away from the surface due to quantum mechanical considerations.

In depletion mode, majority carriers at the surface of Si are repelled by the applied electric field and the region is thus depleted of mobile carriers. A depletion region forms in a similar manner to the reverse-biased junction diode considered previously. The capacitance from the gate to the substrate, therefore, has two components, an oxide capacitance in series with a depletion capacitance [Pierret, 1990]

$$C_{dep} = \frac{C_{acc}C_{dep}}{C_{acc} + C_{dep}} = \frac{C_{ox}}{1 + \frac{\epsilon_{r, SiO_2}d_j}{\epsilon_{r, Si}t_{ox}}} \quad (2.36)$$

As the channel region begins to invert, minority carrier charge accumulates at the surface and the capacitance once again approaches the C_{ox} value. This assumes that the rate of minority carrier generation is sufficiently fast to follow the time-varying AC signal. On the other hand, if a MOSFET-C structure is used instead, a large source of minority carrier charge is available from the surrounding source and drain regions. Between inversion and depletion, or in weak inversion, the situation is more complicated as an incremental increase in the applied voltage can result in new field lines terminating on both immobile charges (by an increase in the depletion junction depth) and terminating on newly generated minority carriers.

In the weak inversion region, the capacitance changes rapidly from C_{dep} to C_{ox} due to the exponential build-up of charge at the surface. This results in a very large K_{CV} factor. The quality factor of such a capacitor is limited mainly by the gate series resistance and can be shown to be approximately equal to $R_G/3^{11}$.

3.8 RESISTORS AND CAPACITORS

Resistors can be implemented in several ways but all essentially involve moving current through a length of material with relatively high resistivity. In a standard bipolar process, diffusion resistors are common. The resistance value can be varied by the application of a bias such as in base-pinch and epitaxial pinch resistors [Gray and Meyer, 1993]. In a standard MOS process we also find diffusion resistors, polysilicon resistors, well-resistors, and the MOS device itself as variable resistors. In a modern bipolar, BiCMOS, or MOS process, most of the above options are available.

Capacitors are realized as either MOS capacitors, as poly-poly "metal" capacitors, metal-insulator-metal (MIM) capacitors, and as poly-diffusion capacitors. For RF applications MIM capacitors are preferred since they result in the lowest losses. Even though standard metal interconnection can be used to construct MIM capacitors, this has two negative consequences. First, it will result in a large uncertainty in the capacitance value due to wide oxide thickness variation

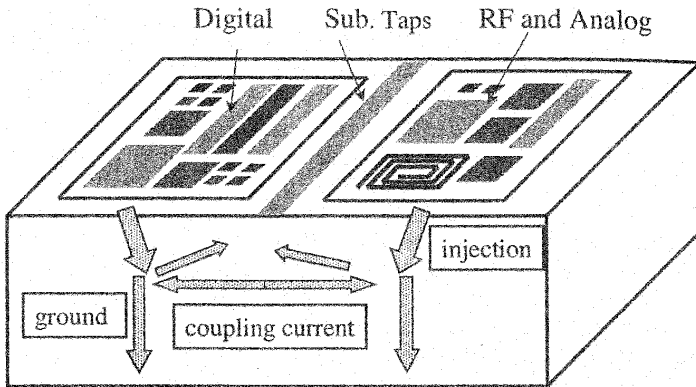


Figure 2.17. Substrate coupling in a mixed-signal system on a chip.

across the wafer. Second, the capacitance value per unit area will be very small due to the thick oxide separating the metal layers. A special MIM capacitor constructed with a well-controlled thin oxide is therefore preferred.

Resistors and capacitors have always been a part of the standard IC process. Thus, great effort has already gone into the analysis and modeling of such structures at lower frequencies. At higher frequencies, though, these structures have many non-ideal effects which must be taken into consideration, such as substrate coupling, self-resonance, and inductance. In this work we will focus on a general interconnection of metal structures above a lossy Si substrate and this generality will allow us to apply our analysis technique to inductors as easily as to capacitors, transformers, and resistors.

4. SUBSTRATE COUPLING

An issue that permeates this research is substrate coupling. Figure 2.17 illustrates the various substrate coupling mechanisms present in an IC environment. Current is injected into the substrate through various mechanisms. Physically large passive devices such as inductors, capacitors, transformers, interconnect and bonding pads inject displacement current in the substrate. This current flows vertically and horizontally to points of low potential in the substrate, such as substrate taps and the back-plane ground. This current couples to other large passive structures in a similar manner.

Active devices also inject current into the substrate, directly and capacitively. Since most active devices are isolated from the substrate by either reverse-biased

pn junctions or oxide, capacitive substrate current injection and reception occur at high frequencies. Direct current can also be injected into the substrate due to hot electron effects. In a short-channel MOS transistor, for instance, electron-hole pair creation takes place in the high-field pinch-off region near the drain due to collisions. The electric field lines lead one set of the carriers into the substrate. Under high field conditions, a multiplication process (avalanche) can also lead to additional hole-pair creation and result in substantial currents.

Coupling between sensitive analog nodes can lead to instability or gain reduction. Furthermore, in a mixed signal IC the coupling between analog and digital portions of the chip can be very problematic. Digital gates switch in a pseudo-random manner and each gate transition results in some energy transfer to the substrate. This energy can couple to sensitive analog nodes and result in reduced signal-to-noise (SNR) ratios.

Though careful layout techniques and differential operation minimize them, these effects can never be totally eliminated or ignored in the design of mixed-signal ICs. Substrate coupling is treated extensively in [Gharpurey and Meyer, 1996]. In this book we draw from an extension of this work, presented in [Niknejad et al., 1998], to analyze passive device substrate coupling.

Notes

- 1 This depends on the I-V curve of a diode. A tunnel diode can certainly be biased as to supply energy, becoming an active device.
- 2 This is a necessary condition for a passive device. However, this condition alone is not sufficient since power gain may occur for a non-matched load or source impedance.
- 3 This is not a rigorous argument since the skin-depth concept of surface impedance applies strictly to a semi-infinite conductor.
- 4 This is due to the linearity of Maxwell's Equations.
- 5 In general the eddy currents are solenoidal whereas the displacement and conductive currents are curl free
- 6 By this we mean the crystal structures of the adjacent layers are compatible.
- 7 By intrinsic we mean no intentional dopants are introduced into the substrate and the only conduction occurs through thermionic emission into the conduction band.
- 8 This result will be established in Chapter 5.
- 9 Current distributions with zero curl lead to zero magnetic fields.
- 10 Consider the current associated with a stream of suicidal lemmings. Given that the cliff is sufficiently high, the suicide rate of lemmings is independent of the height of the cliff.
- 11 See Appendix A.

II

APPLICATIONS OF PASSIVE DEVICES

Chapter 9

VOLTAGE CONTROLLED OSCILLATORS

1. INTRODUCTION

Consider the simplified block diagram of a superheterodyne transceiver, shown in Fig. 9.1. The voltage controlled oscillator (VCO) is a key components of this transceiver as the VCO generates the 'local oscillator' or LO frequency. The LO in turn drives the receive and transmit mixers, converting the received signal from RF to IF or baseband and similarly converting the baseband and IF

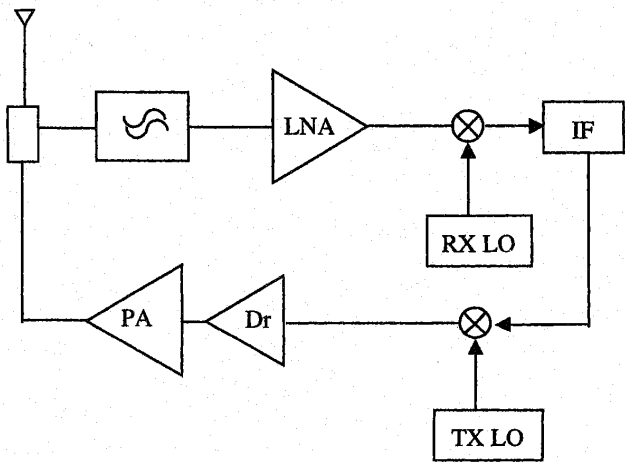


Figure 9.1. Simplified block diagram of a superheterodyne transceiver front-end.

signals to RF for transmission. This conversion process, or mixing, is achieved through multiplication of the sinusoidal output of the VCO with the modulated signal. The LO signal is given by

$$v_{LO}(t) = A \cos(\omega_0 t + \phi_n(t)) \quad (9.1)$$

where A is the constant amplitude of the oscillator, $\omega_0 = f(V_{\text{control}})$ is the frequency of oscillation which can vary by application of the control voltage, and $\phi_n(t)$ represents the random phase noise of the oscillator.

Now consider the information-containing stochastic bandpass signal, $x(t)$, with spectral components centered around ω_1 . Such a process can be uniquely decomposed into two parts as follows [Proakis, 1995]

$$x(t) = B(t) \cos(\omega_1 t + \phi(t)) \quad (9.2)$$

$B(t)$ represents the amplitude modulation and $\phi(t)$ the phase modulation of the signal. Multiplication of the modulated signal with the LO

$$\begin{aligned} v_o(t) &= [A \cos(\omega_0 t + \phi_n(t))] \times [B(t) \cos(\omega_1 t + \phi(t))] \quad (9.3) \\ &= \frac{AB(t)}{2} [\cos((\omega_0 - \omega_1)t + \phi_n(t) - \phi(t)) + \\ &\quad \cos((\omega_0 + \omega_1)t + \phi_n(t) + \phi(t))] \end{aligned}$$

Note that the conversion process has moved the spectral energy from around ω_0 to $\omega_0 \pm \omega_1$. In the case that $x(t)$ represents the received RF signal, then the conversion process moves the input spectrum to a more convenient frequency, usually a lower frequency. In the case that $x(t)$ represents the baseband signal, the conversion process moves the input spectrum to a frequency more convenient for transmission, usually a higher frequency.

Since antenna efficiency is directly related to antenna size relative to the wavelength [Jackson, 1999] at the frequency of interest, higher frequencies allow smaller and more portable antennas to be realized without sacrificing efficiency. In the case of a wired link, mixing with the LO is still useful if the transmission media is shared by several transceivers. In such a case frequency division multiplexing (FDM) or frequency hopping multiple access (FHMA) can be used to share the channel. As evident from (9.1), the phase information can be modulated onto the LO signal directly by means of the voltage control line.

In the superheterodyne receiver, the conversion process occurs in two stages, and the first conversion moves the received signal to the intermediate frequency, or IF. The IF frequency is chosen to simplify the filtering and detection of the input signal. Typically, the input signal bandwidth is much smaller than the carrier signal and thus filtering at RF requires very high Q components. Hence, there is great incentive to perform filtering and channel selection at IF rather

than at RF directly. To alleviate the need for a variable frequency bandpass filter, the LO signal is adjusted so that the IF frequency $\omega_0 - \omega_1$ is a constant center frequency allowing a fixed frequency filter to perform channel selection at IF.

The detrimental effects of the down-conversion or mixing operation are evident when we consider phase noise of the LO

$$V_{IF}(t) = \cos((\omega_0 - \omega_1)t + \phi_n(t) - \phi(t)) \quad (9.4)$$

Note that for proper detection of phase modulation we require that $|\phi_n(t)| \ll |\phi(t)|$. Even when this condition is met, though, the occurrence of a third interfering signal at the input of the receiver can introduce “reciprocal mixing” which can greatly degrade the in-band SNR [Razavi, 1998].

On the transmit side, a low-frequency information signal is modulated onto a higher frequency carrier appropriate for radiative (or optical) transmission. In such a case, the phase noise of the LO leaks outside of the channel bandwidth and through amplification and radiation in the transmit chain appears at the input of transceivers receiving in neighboring bands. This can potentially block or degrade the SNR performance of other users of the spectrum.

2. MOTIVATION

VCOs, as key building blocks in wireless transceivers, require careful design and optimization. The principal performance specifications are power consumption and phase noise performance. Monolithic VCO implementations suffer from poor phase noise performance partly due to low quality factor Q passive components in the frequency band of interest 1–2 GHz. The inductors at these frequencies usually dominate the tank Q . At higher frequencies, 3–10 GHz, it is possible to obtain higher Q inductors over a moderately resistive substrate.

Thus there is a motivation to implement VCOs at higher frequencies where higher Q inductors are easier to fabricate. On the other hand, the varactor Q decreases with frequency and most processes have varactors optimized for 1–2 GHz. Hence, there exists an optimum frequency where the total tank Q is maximum.

While VCOs at higher frequencies can be used directly in many upcoming wireless standards such as wireless LANs at ~ 5 GHz, these VCOs can also be applied to traditional standards in the 1–2 GHz range by the use of frequency dividers. Dividing the VCO output improves the phase noise with little added power consumption. Using a different LO frequency also mitigates coupling problems inherent in monolithic transceiver designs, such as the power amplifier locking the VCO.

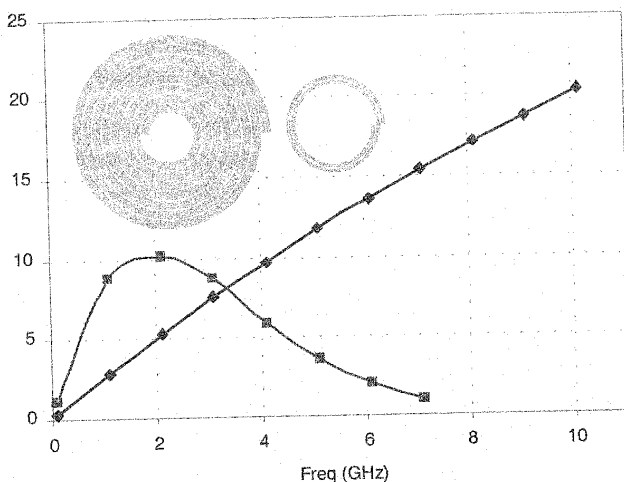


Figure 9.2. The simulated quality factor of a small footprint 1 nH inductor versus an optimal 10 nH inductor. The smaller inductor dimensions are $R = 75\mu\text{m}$ $W = 5\mu\text{m}$ $N = 2$ while the larger inductor has dimensions $R = 150\mu\text{m}$ $W = 12.3\mu\text{m}$ $N = 7.5$. Both structures are realized with a metal spacing $S = 2.1\mu\text{m}$.

3. PASSIVE DEVICE DESIGN AND OPTIMIZATION

3.1 INDUCTOR LOSS MECHANISMS

The analysis and characterization of inductors and other passive devices is a key prerequisite for successful VCO design. Since the VCO phase noise performance is highly dependent on the Q of the tank, as shown approximately from the well-known Leeson formula [Leeson, 1966], it is desirable to obtain high Q inductors.

As we have seen, inductor Q is limited by physical phenomena that convert electromagnetic energy into heat or radiation. If the substrate is sufficiently conductive, magnetically induced currents, or bulk eddy currents, flow in the substrate and act as a possibly dominant form of loss. In the case of highly conductive substrates, such as those of an epi CMOS process, eddy current losses indeed severely limit the Q . In the case of a moderately conductive substrate, such as a bipolar or BiCMOS substrate with resistivity $\sim 10\ \Omega\text{-cm}$, the bulk substrate loss mechanisms are dominated by electrically induced substrate currents while magnetically induced substrate currents are negligible even up to 10 GHz.

Therefore for such moderately conductive substrates there is a great benefit in designing higher frequency VCOs. Substrate losses are curtailed by scaling the inductor size. This also saves valuable chip area since capacitors scale in size at higher frequencies. Skin effect and proximity effect losses prevail but careful analysis can minimize these effects. As a comparison, consider the Q of a 1 nH inductor at 10 GHz versus a 10 nH inductor at 2 GHz. As shown in Fig. 9.2, the simulated maximum quality factor of the 1 nH inductor far exceeds the 10 nH inductor with a considerable savings in chip area.

3.2 DIFFERENTIAL QUALITY FACTOR

It has been recognized that the quality factor of an inductor at high frequency is higher seen differentially rather than single-endedly [Kuhn et al., 1995] [Danesh et al., 1998]. This can be deduced in the following way: if we consider an inductor as a series interconnection of a set of coupled transmission lines [Shepherd, 1986], then we can model the inductor by an equivalent transmission line of appropriate length and impedance by diagonalizing the transmission line matrix. Intuitively, one can see that a shorted inductor self-resonates fundamentally at the quarter-wavelength frequency whereas a differential transmission line self-resonates at the half-wavelength frequency. Hence, we expect an approximate factor of two improvement in the self-resonant frequency of a differential inductor. This means that at a given frequency, less current is injected capacitively into the substrate and therefore fewer substrate losses occur.

It follows that VCO topologies that inherently employ the inductor differentially are advantageous. Differential circuits naturally fit this definition. Using symmetric center-tapped inductors as opposed to two uncoupled inductors leads to a savings in chip area due to the mutual magnetic coupling. Furthermore, the savings in area leads to higher Q values since at high frequencies substrate losses dominate the Q . Lastly, there is no need to model the parasitic coupling that occurs between the two inductors [Meyer et al., 1997].

In this design we employ the center-tapped layout shown in Fig. 9.3 as opposed to the design presented in [Kuhn et al., 1995]. This layout has also been used by [Danesh et al., 1998] [Long and Copeland, 1997]. Fig. 9.4 shows that the maximum Q enhancement is almost a factor of two differentially over single-ended drive. A broadband 3-port equivalent circuit model, shown in Fig. 9.5, can be derived using *ASITIC*.

3.3 VARACTOR LOSSES

A high quality varactor is needed to achieve low phase noise over the full tuning range of the VCO. The varactor is usually designed as a reverse biased PN junction diode. The varactor Q is limited by the intrinsic series resistance

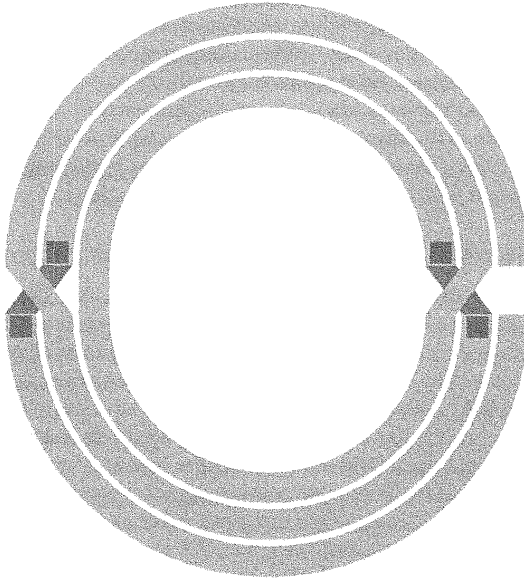


Figure 9.3. Layout of a center-tapped spiral inductor with radius $R = 125 \mu\text{m}$ and the metal width $W = 14.5 \mu\text{m}$.

of the device. Given a layout geometry, *ASITIC* can be used to calculate this distributed resistance.

Typically the varactor Q is sufficiently high in the 1–2 GHz region and thus the varactor loading on the tank is negligible. At increasingly higher frequencies, though, it becomes more difficult to realize a high Q varactor since the $Q = (\omega R_x C_v)^{-1}$ decreases as a function of frequency. To circumvent this, some researchers advocate electrostatically tuned varactors [Young and Boser, 1197] [Dec and Suyama, 1997]. In our process, optimized varactors for 1 GHz were available. These varactors utilize *npn* transistors with higher levels of doping to minimize intrinsic base and emitter resistance. To minimize the noise injection from the control line, a differential structure was used, as shown in Fig. 9.6. The emitters are tied to the tank to allow a monolithic realization since for a single supply design the control voltage range must not exceed the supply voltage. To avoid forward biasing the junctions, the control line voltage V_C should not exceed $V_C \leq V_{CC} - v_o$ where v_o is the steady state oscillation amplitude.

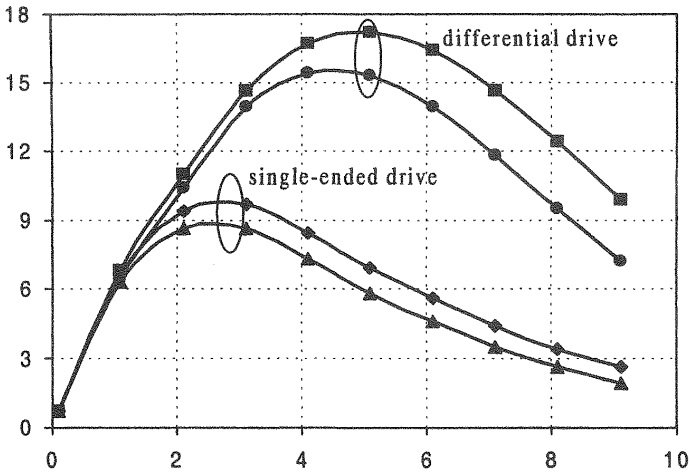


Figure 9.4. Simulated quality factor driven single-endedly (bottom curve) versus differentially (top curve). Note that the comparison is made with both a circular (higher Q value) and square device.

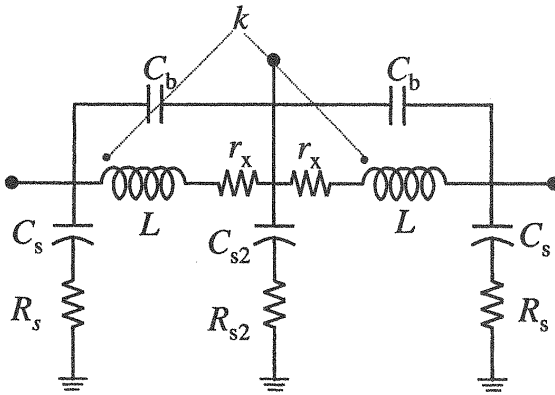


Figure 9.5. Compact circuit model for center-tapped spiral inductor.

To first-order, since the common base connection is a virtual ground for differential signals, noise injected at the control line is rejected. The time-varying nature of the reverse bias voltage, though, leads to noise appearing at

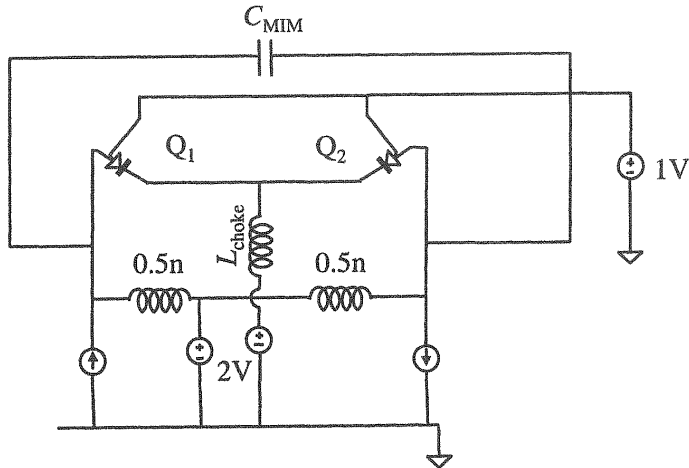


Figure 9.6. Schematic of differential varactors.

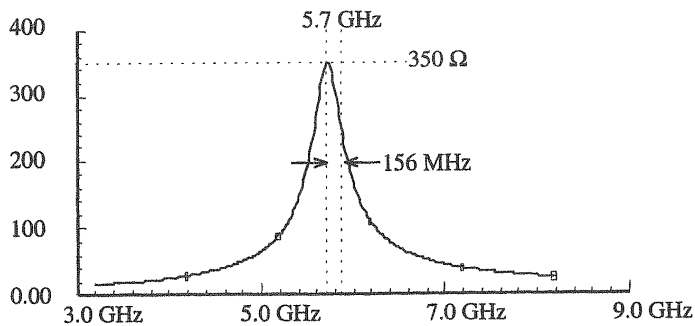


Figure 9.7. Simulated varactor resonance curve.

the output. To avoid this, care must be exercised to properly bypass the control point to ground. Also, the collector node of the varactor is connected to V_{CC} and not to the base to isolate the collector losses from the tank.

The resonance curve of the differential varactor is shown in Fig. 9.7. Note that the varactor Q is on the same order of magnitude as the inductor Q . Hence, to avoid loading the tank it is necessary to add linear capacitance to the tank to increase the effective Q .

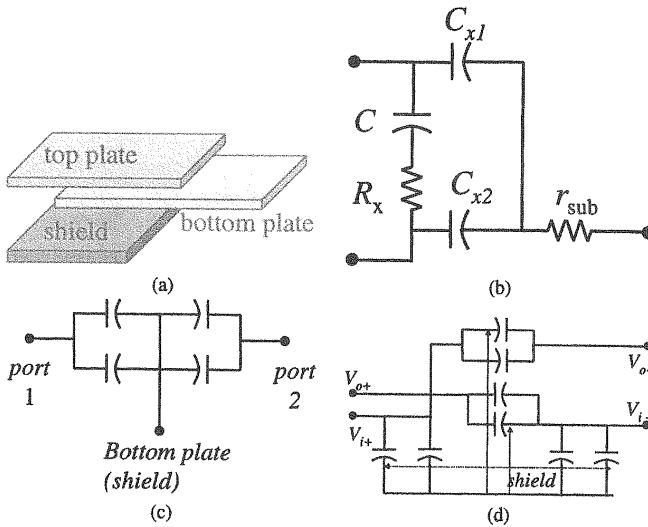


Figure 9.8. Shielded MIM capacitor equivalent circuit. In (a) the top, bottom, and shielding plates are shown. Part (b) shows the equivalent circuit extracted from *ASITTC*. In (c) the load capacitor is shown realized as a symmetric-quad. In (d) the passive capacitive feedback network is shown, also realized as a pair of shielded symmetric quads.

3.4 METAL-INSULATOR-METAL (MIM) CAPACITORS

To realize a high quality factor for the entire tank, high Q capacitors are needed to boost the effective quality factor of the varactor. One may employ a linear high Q capacitor in series or in shunt with the varactor. Both connections limit the tuning range of the VCO. The series connection has the added advantage of allowing a greater range of tuning voltage to be applied to the tank without forward biasing the varactor diode.

While MOS capacitors were an option in this process, we opted for MIM capacitors to avoid any further loading of the tank. MIM capacitors have low density and thus require larger chip area. The process variation of the oxide thickness also further limits the applicability of MIM capacitors in Si. Since MIM capacitors only make up a fraction of the total tank capacitance, the variation in oxide thickness is tolerable.

To avoid substrate injection and the consequent substrate losses, the MIM capacitors are shielded with the bottom metal layer. An equivalent circuit, calculated using *ASITTC*, is shown in Fig. 9.8. To avoid the losses of the

bottom plate parasitics of the shielded capacitors, a differential structure is employed with the bottom plate at the virtual ground.

4. VCO CIRCUIT DESIGN

4.1 VCO TOPOLOGY

For this work the differential topology is a natural choice given the discussion in Section 3.2. Differential operation has many other positive attributes amenable to monolithic integration. It provides better immunity from the package and substrate parasitics, reducing substrate coupling. This is especially important when the VCO is integrated with many other blocks. Differential dividers are also easier to realize at high frequencies as emitter coupled logic can be employed. While the area of active devices is doubled, the area of passive devices reduces due to the mutual coupling and higher differential Q .

For a generic differential pair with positive feedback, the equivalent negative resistance is given by

$$R_{eq} = \frac{-2n}{g_m} \quad (9.5)$$

where the factor n is the fraction of voltage fed back to the base of the differential pair. As shown in Fig. 9.9 the feedback network can be realized using an on-chip transformer [Zannoth et al., 1998], emitter followers [Jansen et al., 1997], a direct connection [Razavi, 1998], or a capacitive transformer [Razavi, 1998]. We opted for a capacitive transformer in order to maximize the oscillation amplitude while minimizing the loading on the tank, the power dissipation, and the noise.

4.2 PHASE NOISE ANALYSIS

Full characterization of the phase noise requires numerical solutions to stochastic differential equations [Kaertner, 1990, Demir et al., 1998]. Approximate linear time-varying techniques have been presented by [Hajimiri and Lee, 1998, Samori et al., 1998] and agree well with measurements. These techniques are more appropriate for simulation rather than the design of a VCO¹. To gain an understanding of the operation of the VCO and phase noise, we follow the technique presented in [Kouznets and Meyer,]. This is a simple engineering approach that gives good insight into the problem.

4.2.1 LINEAR ANALYSIS NOISE TRANSFER COEFFICIENTS

Consider Fig. 9.11, the simplified small signal equivalent circuit of Fig. 9.10. For simplicity, C_μ and r_π have been neglected in the equivalent circuit. Current sources $i_{1a,b}$ model the shot noise generated by the differential pair collector junction. Current sources $i_{2a,b}$ model the base current shot noise. Note that while we ignore the intrinsic base resistance r_b , it is critical to include the noise

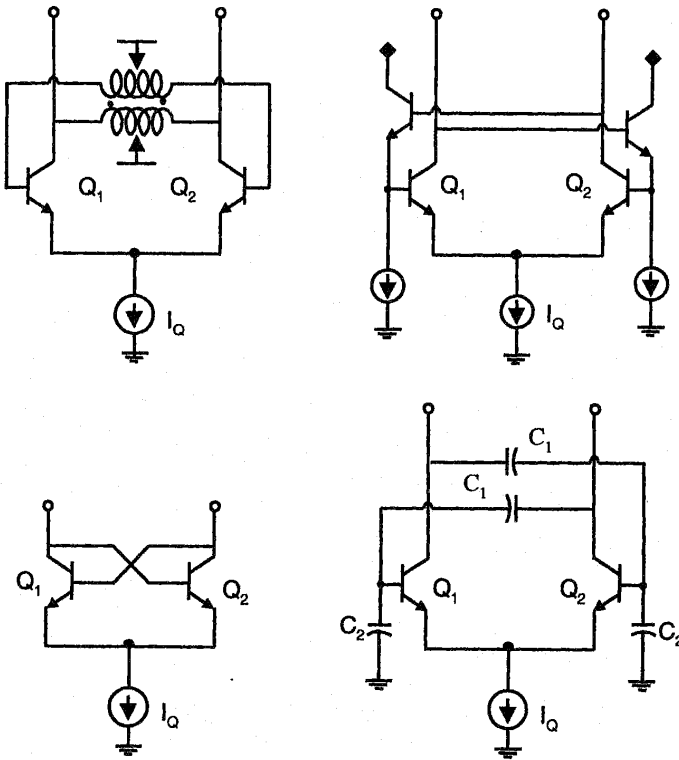


Figure 9.9. Different feedback mechanisms for negative resistance generation.

generated by r_b , and this is represented by the voltage sources $v_{b,a,b}$. The current sources $i_{4a,b}$ represent the current noise generated by the biasing resistors $R_{B1,2}$. Current source i_5 represents the total noise generated by the passive tank, including the thermal noise of the metals that make up the inductance as well as the substrate losses.

From a linear time-invariant point of view, our noise description of the circuit is complete. Due to symmetry, the common emitter node is a virtual ground and thus the noise due to the tail current is shunted to ground. Furthermore, due to the differential output, any noise injected at the emitters is a common mode signal that is attenuated by the common mode rejection, set by the level of matching in the circuit. This argument, though, neglects the time variance of

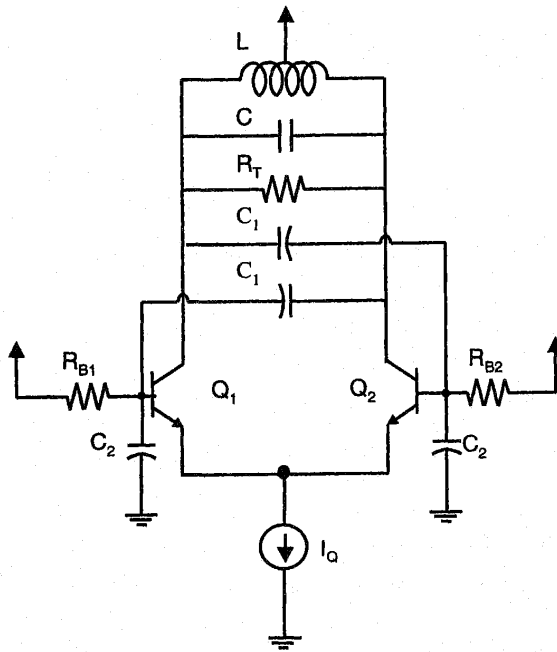


Figure 9.10. Schematic of differential VCO.

the circuit which results in a time-varying transfer function from the tail current source to the output.²

Writing the KVL equations at the input base nodes we have

$$v_{i1,2} s C_{2,4} - i_{4a,b} - i_{2a,b} + (v_{i1,2} - v_{3a,b}) s C_{\pi 1,2} + (v_{i1,2} - v_{o2,1}) s C_1 = 0 \quad (9.6)$$

similarly at the output collector nodes

$$\begin{aligned} 0 = & g_{m1,2} (v_{i1,2} - v_{3a,b}) - i_{1a,b} + (v_{o1,2} - v_{o2,1}) s C_T + \\ & (v_{o1,2} - v_{o2,1}) \frac{1}{sL} + (v_{o1,2} - v_{o2,1}) \frac{1}{R_T} \mp i_5 + \\ & (v_{o1,2} - v_{i2,1}) s C_{3,1} \end{aligned} \quad (9.7)$$

Solving the above system of equations for the differential output voltage we have

$$v_{od} = (a_{i1} i_{1a,b} + a_{i2} i_{2a,b} + a_{v3} v_{3a,b} + a_{i4} i_{4a,b} + a_{i5} i_5) \quad (9.8)$$

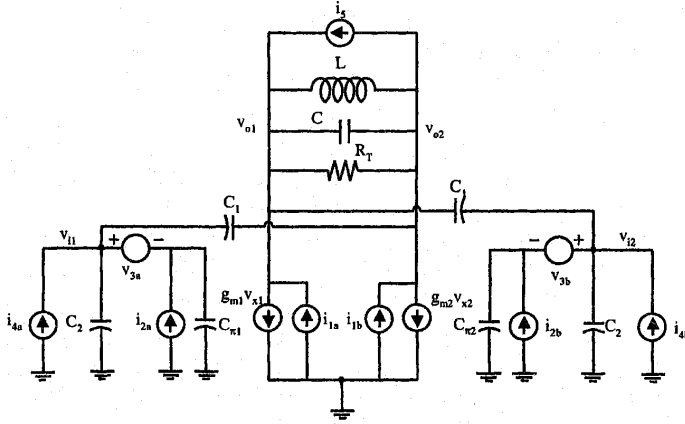


Figure 9.11. Simplified equivalent circuit of differential VCO.

where

$$a_{i1} = \frac{\frac{1}{2}sL}{D(s)} \quad (9.9)$$

$$a_{i2} = \frac{-\frac{1}{2}(g_m + sC_1)\frac{L}{C_\sigma}}{D(s)} \approx \frac{-\frac{1}{2}g_m\frac{L}{C_\sigma}}{D(s)} \quad (9.10)$$

$$a_{v3} = \frac{\frac{1}{2}\frac{C_\pi}{C_\sigma}sL(g_m + sC_1)}{D(s)} \approx \frac{\frac{1}{2}\frac{C_\pi}{C_\sigma}sLg_m}{D(s)} \quad (9.11)$$

$$a_{i4} = a_{i2} \quad (9.12)$$

$$a_{i5} = 2a_{i1} \quad (9.13)$$

where $D(s)$ is the determinant of the system (9.6) (9.6)

$$D(s) = 1 + \left(\frac{C_1g_m}{2C_\sigma} - \frac{1}{R_T}\right)sL + LC_{eff}s^2 \quad (9.14)$$

and C_σ represents the total capacitance at the base of each transistor

$$C_\sigma = C_1 + C_2 + C_\pi \quad (9.15)$$

The capacitance C_{eff} is given by

$$C_{eff} = C_T + \frac{C_1(C_2 + C_\pi)}{2C_\sigma} \quad (9.16)$$

In steady state oscillation, the second expression of (9.14) vanishes and the frequency of oscillation is set by

$$\omega_0 = \frac{1}{\sqrt{LC_{eff}}} \quad (9.17)$$

The vanishing of the second term corresponds to the balancing of the circuit losses with the negative resistance of the differential pair. Equivalently, the balancing occurs when the loop gain of the system is equal to unity. Thus the above equation can be rewritten as

$$D(s) = 1 + (A_\ell - 1) \frac{sL}{R_T} + \frac{s^2}{\omega_0^2} \quad (9.18)$$

The expression A_ℓ is identified as the loop gain of the system

$$A_\ell = \frac{g_m R_T}{2n} \quad (9.19)$$

where n is the feedback factor of the capacitive transformer coupling signals from the collector to the base

$$\frac{1}{n} = \frac{C_1}{C_\sigma} \quad (9.20)$$

In steady state $A_\ell \rightarrow 1$ and thus at frequencies close to the oscillation frequency ω_0 , (9.18) can be simplified to

$$D(\omega_0 + \delta\omega) \approx \frac{-2\delta\omega}{\omega_0} \quad (9.21)$$

This results in the characteristic 6 dB/octave decrease in noise power when one moves away from the carrier, far from the flicker noise corner of the device.

4.2.2 NOISE POWER AT OUTPUT

The total power spectral density of the noise at the output of the differential pair can now be written [Gray and Meyer, 1993]

$$\overline{v_{od}^2} = \frac{1}{2} (a_{i5}^2 \overline{i_5^2} + 2a_{i4}^2 \overline{i_4^2} + 2a_{v3}^2 \overline{v_3^2} + 2a_{i2}^2 \overline{i_2^2} + 2a_{i1}^2 \overline{i_1^2}) \quad (9.22)$$

The factors of two inside the parentheses account for the differential nature of the circuit. The factor of $\frac{1}{2}$ outside of the parentheses is due to the transfer of noise at frequency $(-\omega_0 - \delta\omega)$ to the output [Kouznets and Meyer,].

The noise power spectral densities of the sources are given by [Gray and Meyer, 1993]

$$\overline{i_1^2} = 2qI_C \quad (9.23)$$

$$\overline{v_2^2} = 2qI_B + K_1 \frac{I_B^a}{f} \quad (9.24)$$

$$\overline{v_3^2} = 4k_B T r_b \quad (9.25)$$

$$\overline{i_4^2} = \frac{4k_B T}{R_B} \quad (9.26)$$

$$\overline{i_5^2} = \frac{4k_B T}{R_T} \quad (9.27)$$

For a typical bipolar technology, the flicker noise corner frequency is on the order of 1–10 kHz and thus the direct contribution of the flicker noise term in (9.24) can be neglected at RF frequencies. On the other hand, time variance in the circuit can translate the noise around DC to RF.

To see how the Q of the tank influences the noise gain, consider the current and voltage gains from the base of the transistors to the output. Assume for simplicity that the inductor Q dominates and for g_m substitute the steady state value that solves $A_\ell = 1$. This leads to

$$|a_{i2}|^2 \approx \frac{1}{4C_1^2 Q^2 \delta \omega^2} \quad (9.28)$$

and

$$|a_{v3}|^2 \approx \frac{C_{pi}^2}{C_1} \frac{\omega_0^2}{4Q^2 \delta \omega^2} \quad (9.29)$$

This quadratic dependence on Q is well-documented [Razavi, 1998]. The other noise transfer coefficients do not depend directly on Q

$$|a_{i1}|^2 = \frac{(\omega_0 L)^2 \omega_0^2}{\delta \omega^2} \quad (9.30)$$

$$|a_{i5}|^2 = 4|a_{i1}|^2 \quad (9.31)$$

To minimize the above coefficients, one must minimize the tank inductance. Naturally this requires a compensating increase in the tank capacitance. A similar conclusion is reached by [Samori et al., 1998] and can be verified using SpectreRF simulations. In a practical design, the lower limit is set by the tolerance of L and the realizability of C .

4.3 COMPARISON WITH SPECTRERF SIMULATION

Figure 9.12 shows the simulated and calculated phase noise of a simple VCO with parameters summarized in Table 9.1. The simulated phase noise is computed using SpectreRF. The calculated phase noise is from the equations of the previous section. A good match is observed between theory and calculation. On the other hand, close to the carrier, the mixing effects of the fundamental

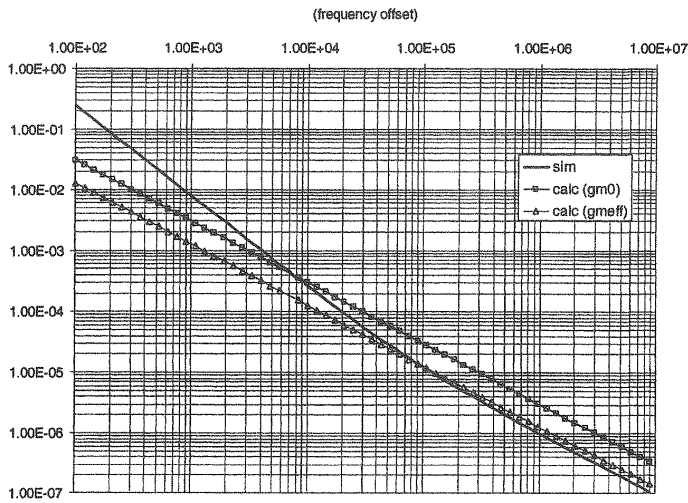


Figure 9.12. Simulated and calculated phase noise spectrum.

Table 9.1. VCO circuit and process parameters.

<i>Bias Current</i> = 5 mA		
$L = 3 \text{ nH}$		
$C1 = C2 = 200 \text{ fF}$	$C_T = 856 \text{ fF}$	
$R_T = 600 \text{ }\Omega$	$R_B = 30 \text{ k}\Omega$	
$r_b = 32.4 \text{ }\Omega$	$f_T = 25 \text{ GHz}$	
$\beta_0 = 168$	$C_{je0} = 48 \text{ fF}$	

component are significant, as can be seen from the close-in phase noise below 100 kHz. Here the rise in noise is faster than ω^{-2} due to the flicker noise up-conversion.

A more thorough comparison can be performed if we sweep the oscillator design parameters A_ℓ , Q , and n . Linear analysis predicts the phase noise well when the loop gain is not too large. This conclusion has also been reached by [Kouznets and Meyer,] for the single-ended Colpitts oscillator.

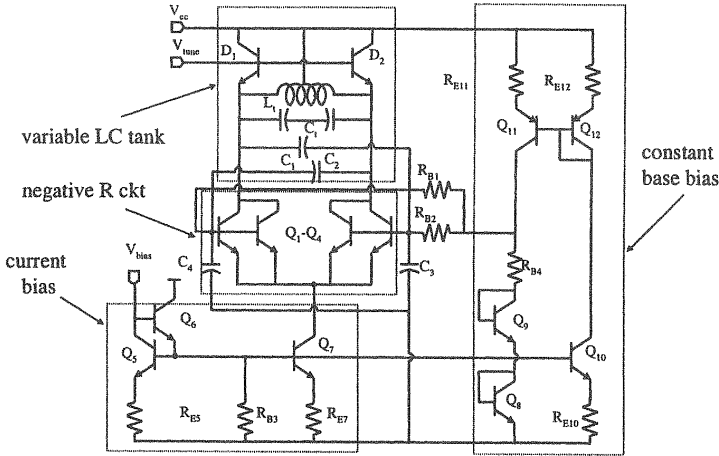


Figure 9.13. VCO core circuit schematic.

5. VCO IMPLEMENTATION

Fig. 9.13 shows a schematic of the VCO core in our practical implementation. Q1-Q4 form a differential quad and are sized each at $5 \times 0.4 \times 0.7 \mu\text{m}$. Shielded (MIM) capacitors C1-C4 of value 100 fF (60 fF)³ are used in the feedback network to allow maximum swing. The capacitors are also in quad formation for matching purposes. Frequency tuning is performed via varactors D1-D2. These are reverse-biased base-emitter junctions with extra doping to minimize series resistance. Nevertheless, the quality factor of the varactors is too low at high frequencies, and thus some 300 fF (0 fF) of MIM capacitance is added to the tank. Inductor L_t is a 3 nH (1.8 nH) inductor realized as a center-tapped device as shown in Fig. 9.3. It has a simulated peak Q of 15 at 3 GHz.

To find the optimum bias current provisions are made to vary the bias current externally. If the base current biasing resistors were tied directly to the supply as in Fig. 9.10, the base DC voltage would vary as a function of β as well as a function of collector current and temperature T . This variation could potentially saturate the tail current source, and to avoid this Q5-Q9 are used to provide a relatively constant bias voltage. This voltage is derived from two V_{BE} drops which are relatively constant as a function of I_C , β , and T . The actual base voltage drop is formed by

$$V_{B1,2} = 2V_{BE} + I_Q R_{B4} - I_B R_{B1,2} \quad (9.32)$$

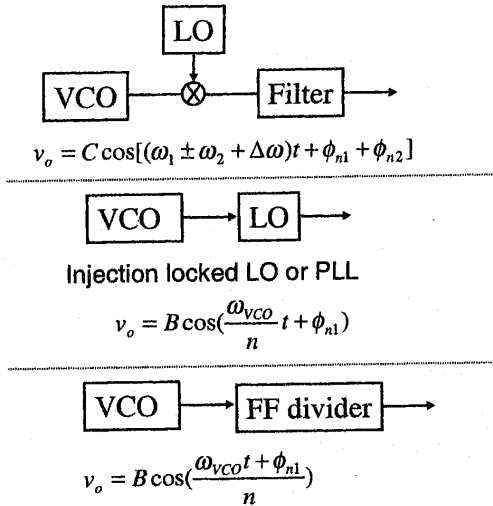


Figure 9.14. Different techniques to convert the VCO frequency: down-conversion, mode-locking, and latch-based frequency division.

Since I_B is a function of I_Q , a first order cancellation is provided by the second and third term in the above equations. Power is coupled capacitively from the VCO core to the frequency divider and output buffer circuits.

5.1 FREQUENCY DIVIDERS

Fig. 9.14 shows different possible techniques to divide the VCO oscillation frequency to a convenience frequency. First we see a traditional mixer-based approach with an LO signal driving a mixer and an on-chip filter selecting the appropriate desired harmonic. This approach is costly in terms of power as it requires several additional components. Also, the LO signal needs to be much cleaner than the VCO in terms of phase noise in order not to degrade the phase noise performance. But since the fixed LO is limited to the same on-chip LC tanks, it is likely that the LO phase noise will be at least as bad as the VCO. Hence, the output of the system suffers from more phase noise.

Another option shown next in Fig. 9.14, is to injection lock the LO to the VCO signal [Rategh and Lee, 1999]. Here, due to injection locking, the phase noise performance of the output follows the phase noise of the VCO for close-in phase noise. For proper locking, the power coupled from the VCO to the LO must exceed the intrinsic noise of the LO.

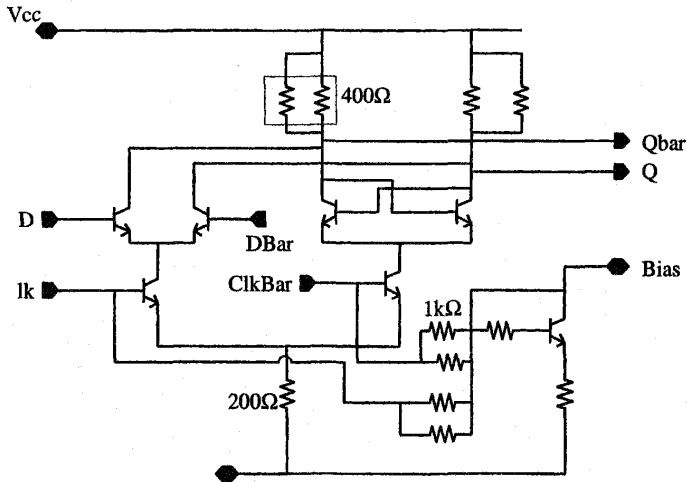


Figure 9.15. Schematic of differential latch.

The third option, and the most common, is to use latch-based frequency dividers. The advantage of using dividers is that the phase noise actually improves as we divide the frequency.

5.1.1 LATCH-BASED DIVIDERS

The differential latch of Fig. 9.15 is used at the heart of the frequency divider. The traditional master-slave topology is used to divide by two. The current consumption is $250\ \mu\text{A}$ per latch and the circuit is operational up to 8 GHz. To improve headroom, the dividers are designed with emitters driving a resistor current source. A mirror biases the latch current level.

SpectreRF periodic steady state noise analysis is used to calculate the noise contribution of the frequency divider. Simulation shows that the noise contribution of the frequency divider is only significant far from the carrier.

5.2 OUTPUT BUFFERS

Figure 9.16 shows the schematic of the output buffers which are capable of delivering -12 dBm into $50\ \Omega$. One buffer is driven by the VCO directly while another buffer is driven at the divided frequency. On-board matching must be used to improve the power gain of these devices. The buffers consume 5 mA. The design is a traditional two stage differential amplifier with input emitter follower buffers to avoid loading the output of the latches.

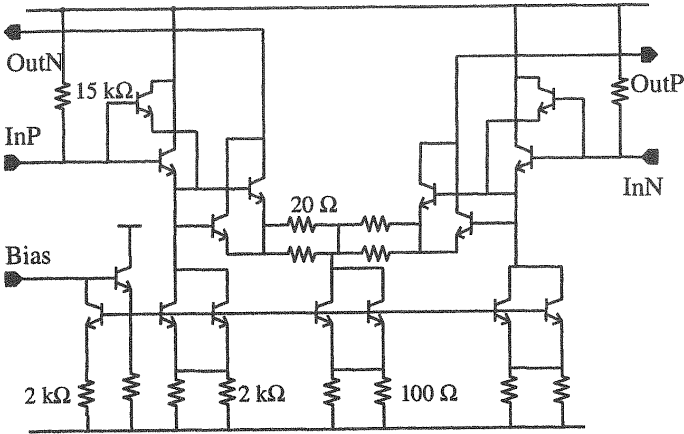


Figure 9.16. Schematic of output buffers.

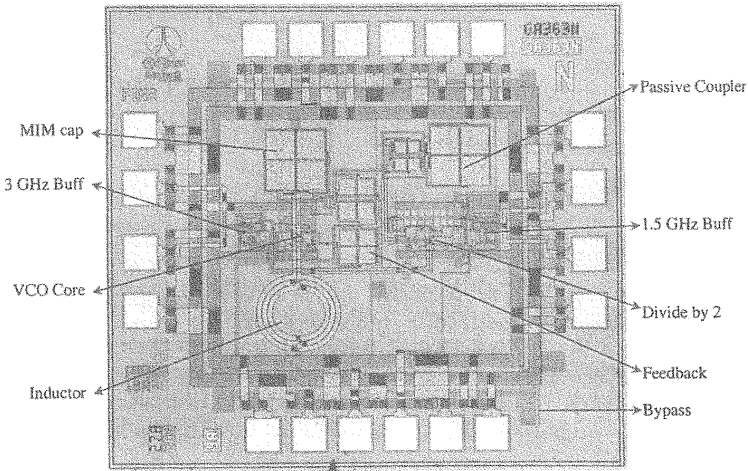


Figure 9.17. Chip-level die photo of 2.9 GHz design utilizing a circular spiral.

6. MEASUREMENTS

A chip-level layout of the final 2.9 GHz design is shown in Fig. 9.17. The 4.4 GHz layout is similar with the exception that no MIM capacitors are used

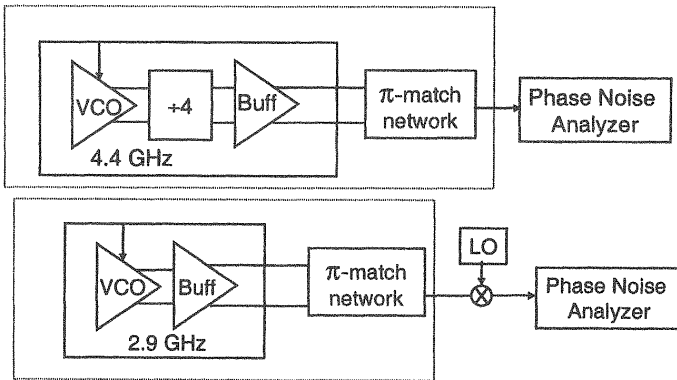


Figure 9.18. Measurement setup.

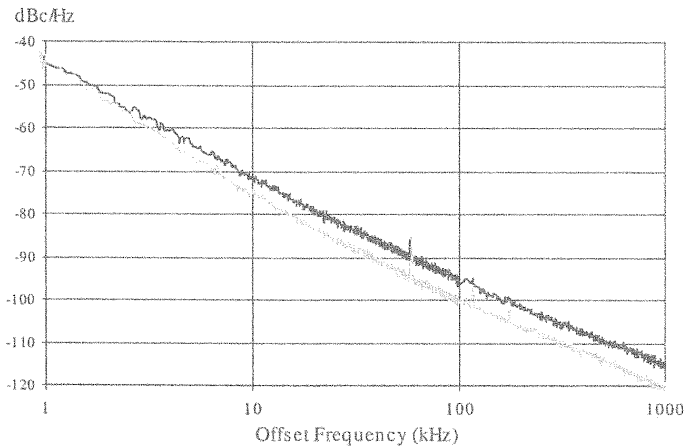


Figure 9.19. Measured phase noise of VCO.

in the tank. On-board transformers and matching networks are used to convert the signal into a single-ended $50\ \Omega$ environment for testing purposes.

Fig. 9.18 shows the test equipment setup. The chip operates on a 2.6-2.8 V supply voltage. The measured, simulated, and calculated phase noise of the 2.9 GHz and 4.4 GHz parts are shown in Fig. 9.19 and summarized in Table 9.2. Note that the 2.9 GHz oscillators were measured by down-converting the

Table 9.2. Summary of measured performance.

Center Freq.	2.9 GHz VCO	4.4 GHz VCO
Core current	3.5 mA	4.0 mA
Tuning Range	250 MHz (10%)	260 MHz (6%)
SSB Phase Noise (100 kHz offset)	-95.2 dBc/Hz	-100.2 dBc/Hz
Technology	25 GHz bipolar	
Substrate	10 Ω -cm	

carrier to near 1 GHz. This was necessary since the RDL model NTS-1000B phase noise analyzer requires a carrier below 1 GHz. Since the phase noise of the LO driving the down-converter is assumed to be better than the VCO under test, the measured phase noise is approximately the same as the phase noise of the VCO. The 4.4 GHz oscillator, though, was measured using the built-in dividers that divided the carrier by a factor of four.

The phase noise of the 2.9 GHz part is superior since the effective tank Q is higher. The oscillator was designed for 5.5 GHz but the tank resonates at 4.4 GHz due to incorrect models for the varactor. The models for the varactor were measured at 1 GHz and extrapolated. Not only is the inductor Q lower than optimal, the varactor loads the tank in the 4.4 GHz design due to the absence of linear capacitors. Measurements also confirm the 6 dB theoretical improvement in phase noise performance due to frequency division by each factor of two.

7. CONCLUSION

In this chapter we have shown that Si inductors above 3 GHz are feasible and in fact desirable. Their application, though, necessitates accurate and efficient analysis of the various loss mechanisms present in the Si IC. We have also shown that differential operation is superior to single-ended designs for fully-integrated VCOs. The phase noise of the oscillator has been calculated and verified with SpectreRF simulations. Measurements on a practical design are close to expectations.

Notes

- 1 It should be noted that the work of Hajimiri [Hajimiri and Lee, 1998] gives good insight into the time-varying nature of the noise and its relation to the collector current waveform.
- 2 This subject is treated in [Hajimiri and Lee, 1998] and is further neglected in the following analysis. The ramifications of this simplification will be noted when we compare our results with SpectreRF simulations.
- 3 Component values are given for the 2.9 GHz design and for the 4.5 GHz design in parentheses.