

JSM
99-185
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International journal of
and microwave computer-a
engineering.
v. 8
no. 6
Nov 1998

JOURNAL OF

International Microwave Computer-Aided Engineering

VOLUME 8/ NUMBER 6

NOVEMBER 1998

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This journal is co-sponsored by the Center for Advanced Manufacturing and Packaging of Microwave, Optical, and Digital
Electronics (CAMPmode) at the University of Colorado, Boulder.



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John Wiley & Sons, Inc.

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Volume 8, Number 6 was mailed the week of October 12, 1998.

ISSN: 1096-4290

Spiral Inductors on Silicon — Status and Trends (Invited Article)

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Received 11 March 1998; accepted 24 June 1998

ABSTRACT: The status of the integration, the modeling, and the layout of spiral inductors on silicon substrates for rf circuits are reviewed. A summary of the current research activity in this field is presented. The possible inductor implementations are categorized either as conservative, following the silicon main stream, or as innovative approaches. It is concluded that the spiral inductor on silicon is a feasible device and finds extensive use in the design of future silicon-based rf circuits. © 1998 John Wiley & Sons, Inc. *Int J RF and Microwave CAE* 8: 422–432, 1998.

Keywords: inductor; spiral inductor; silicon; multilayer interconnects; RF; microwave; passive components

I. INTRODUCTION

The rapidly emerging commercial and consumer markets in wireless communications are raising a demand for integrated solutions in silicon technology [1]. One of the major technical challenges associated with the integration of a wireless RF transceiver on a single silicon chip is the development of integratable inductors. Inductors have not been part of main-stream silicon technology in the past, and useful quality-factors (Q) have not been demonstrated until a few years ago [2]. The optimization of this device is an important task, because the inductor- Q has a profound impact on the performance of the basic RF circuit building blocks [3]. Experience in the integration of inductors has been gained over the past two decades as part of the development of monolithic microwave integrated circuits (MMICs) on GaAs [4]. The optimization of this type of inductor, however, is not as difficult as on silicon, because GaAs is semi-insulating, so that substrate losses are negligible. Also, thick electroplated gold (Au) interconnects are typically used in MMICs, leading to very small ohmic losses in the spiral coil and thus high Q -factors [4]. In contrast, conven-

tional silicon substrates have a resistivity of $10\ \Omega\ \text{cm}$ or lower, so that substrate losses are well noticeable. The interconnects used in silicon technology are designed for very large scale integration (VLSI) applications, i.e., wire widths and spaces measure close to $1\ \mu\text{m}$, limiting the maximum metal thickness to about $1\text{--}2\ \mu\text{m}$, and the metallization is aluminum (Al) with a comparably high resistivity [5].

Modern silicon fabrication processes, however, feature routinely multilevel interconnects with up to six metal layers. In Section II.A, we will discuss how multilevel interconnects can be utilized to reduce both the ohmic losses in the spiral coil and the substrate losses without any alteration of the fabrication process. This kind of inductor design is consequently implied to as a conservative approach. On the other hand, modification of the silicon fabrication process has recently been explored, and novel types of substrates, such as silicon-on-insulator (SOI), silicon-on-sapphire (SOS), high-resistivity silicon (HRS), or glass have been studied as ways to reduce or eliminate substrate losses [6]. Micromachining techniques have been investigated either for the same reason or to enable novel integrated RF structures. Also re-

cently, a strong effort has been made to replace Al VLSI interconnects by copper (Cu), reducing the metal resistivity to about 50% [7]. These novel substrate types and interconnect schemes may be adopted by silicon technology in the near future, either driven by other applications, or they may be part of dedicated silicon processes geared toward RF applications. At the moment, however, those novel processes are implied to as innovative approaches as for mentioned reasons. They will be discussed in Section II.B. Section III is devoted to inductor modeling, which is an important task because the requirements on parameter control in RF circuits are more stringent than those in digital designs. In Section IV, we will address special issues the rf circuit designer may raise. Those include the crosstalk between inductors and the effect of a substrate contact on the inductor characteristics. A summary of the findings and an outlook on future possible developments will be given in Section V.

II. DESIGN OF SPIRAL INDUCTORS ON SILICON

Fundamentally, three basic inductor structures are feasible in silicon technology, i.e., the planar spiral coil structure [2], the multilevel spiral (MLS) coil inductor [8], and the solenoidal device (Fig. 1a–c) [9]. The structures are built by using the metal layers $M-i$ and the via connections $V-i$ between them, with $i = 1$ through n for the metal layers and $i = 1$ through $(n-1)$ for the vias. (The electrical connection to the different silicon regions is provided by an additional via contact that is not considered part of the interconnect scheme and that is not used for the fabrication of the spiral inductor structure.) While a solenoid has the advantage that the main electromagnetic flux is parallel to the silicon surface and thus substrate losses are potentially minimal, it has the disadvantage that it will suffer from the considerable contact resistance between the repeated vias and metal layers in VLSI interconnect structures (Fig. 1a). MLS inductors provide a high inductance per area, but the self-resonance frequency is low, limiting the application of this device to low frequencies (Fig. 1b) [8]. Most inductors on silicon to date are therefore planar spiral inductors, even though the electromagnetic flux is directed into the silicon substrate (Fig. 1c). Another reason for preferring this structure is probably the extensive experience with the design of integrated inductors on GaAs [4]. The basic spiral

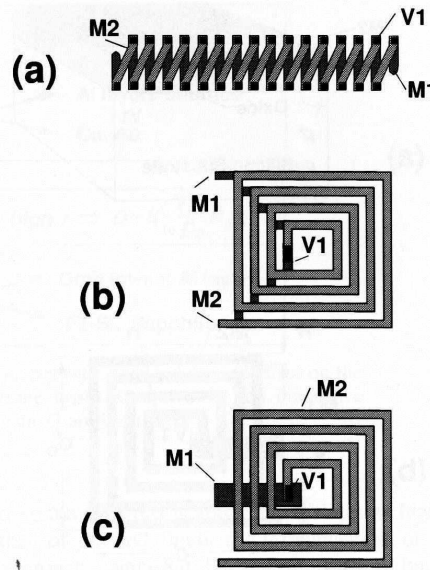


Figure 1. Schematic plan views of (a) a solenoidal inductor, (b) a multilevel-spiral (MLS) inductor, and (c) a planar spiral coil.

inductor structure requires a minimum of two levels of metal and one via connection between them (Fig. 2). The spiral coil is defined by the outer dimensions (d_o), the number of turns (n), the width of the conductor (W), and the space between the turns (S), as shown in Figure 2b. An underpass contact at a lower metal level and a via connection are used to bring the inner end of the coil to the outside (“M1” in Figure 2a and b). The spiral coil can be modeled with good accuracy by using the simple lumped-element representation in Figure 3a [10]. The model consists of the ideal inductance L_s , the series resistance R_s to describe the ohmic losses in the coil, and the capacitance C_p which represents the interwire capacitance components and the capacitance between coil and underpass layers. The resistance R_s can be frequency dependent as a result of the skin effect in the coil conductor. This model holds well for inductors on GaAs, where substrate losses are negligible, but not for silicon. The losses in the silicon substrate are twofold. First, there are the capacitive losses, described in the extended model of Figure 3b by the oxide capacitances C_{ox} and the bulk resistances R_B (in spite of the asymmetry of the spiral coil, identical elements C_{ox} and R_B are considered in Figure 2 for simplicity reasons). Second, eddy currents in the substrate can

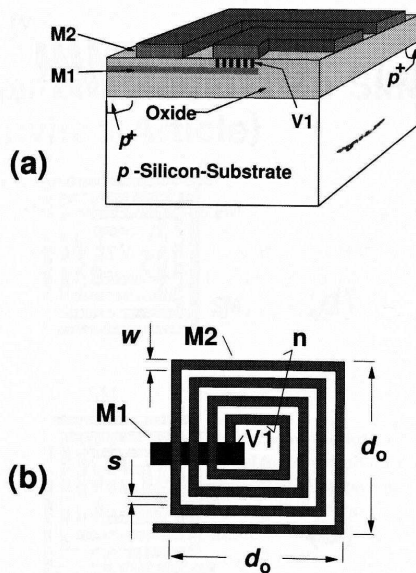


Figure 2. Cross-sectional view (a) and plan view (b) of a basic spiral inductor structure on a silicon substrate.

be significant if the silicon resistivity underneath the spiral coil is low. The physical nature of eddy currents is not considered in the model of Figure 3b, but its effect can be represented by a reduction of the inductance L_S and an increase of the resistance R_S . Likewise, the skin effect in the substrate has to be represented by a frequency-dependent R_B , if applicable. Both, the eddy currents and the skin effect in the substrate are not significant if the substrate resistivity is of the order of $10 \Omega \text{ cm}$, which is usually a preferred and practical value.

Another effect of the conductive silicon substrate is that the definition of the substrate potential is crucial because it can affect the electrical characteristics of the inductor, particularly if the silicon resistivity is high (e.g., $10 \Omega \text{ cm}$) [11]. Differently from conventional MMIC structures, no RF ground potential is provided at the backside of the wafer due to the lack of a via contact through the wafer. The substrate potential is defined by a substrate contact at the wafer surface that is placed close to or at some distance from the spiral coil, depending on the circuit layout. In the lumped-element model, the substrate contact is therefore represented by a resistor R_{Sub} contacting the substrate terminal to the node between C_{Ox} and R_B near the outside terminal (Fig. 3b).

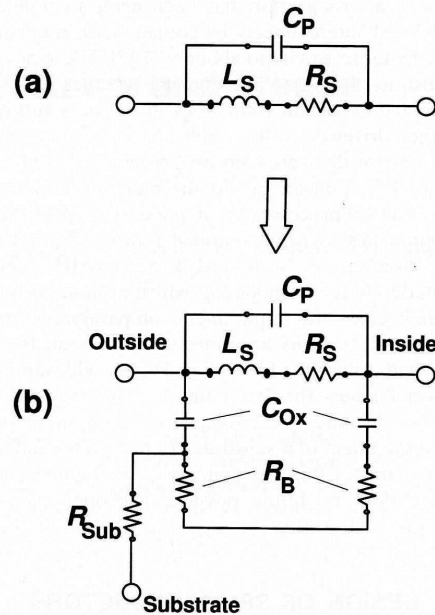


Figure 3. Lumped-element models of (a) a spiral inductor on an ideal substrate and (b) a spiral inductor on a lossy silicon substrate, including a substrate contact.

A closer look at the inductor model in Figure 3b provides an insight in the electrical behavior of the device. It is first important to consider, that the spiral inductor has generally large lateral dimensions and a narrow vertical cross-section, because planar silicon fabrication technology is used for the inductor fabrication. Therefore, the capacitances C_{Ox} are significantly larger than C_P . Of the two possible resonance loops shown in Figure 3b, resonance via C_{Ox} will therefore occur at a much lower frequency than via C_P , restricting the application to low frequencies. In case the C_{Ox} cannot be reduced by increasing the spacing of the spiral coil from the silicon, the only way to prevent self-resonance via C_{Ox} is to provide a sufficiently large R_B . This, however, does not fully eliminate the RF losses through the substrate path (i.e., via C_{Ox}), in particular at the higher frequencies. However, as a result, the RF signal will pass primarily through L_S at low frequencies and increasingly through C_{Ox} at high frequencies.

The degree to which the inductor deviates from an ideal device is described by the quality factor which is $Q = \text{im}(Z)/\text{re}(Z)$ if Z is the impedance of the inductor. (For the one-port case, Z is

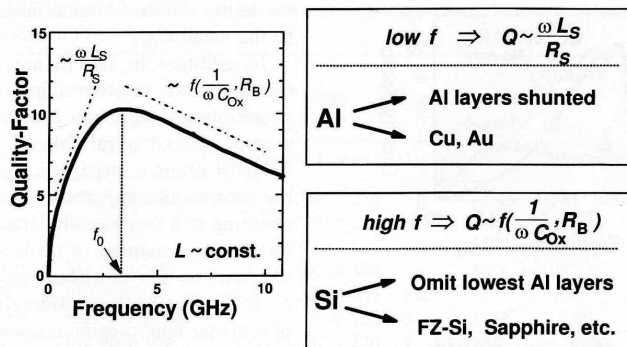


Figure 4. Quality-factor (Q) as a function of frequency with indicated dependencies on the ohmic losses in the spiral coil and on the substrate losses. Conservative and innovative means of optimizing a spiral inductor for a maximum Q are illustrated.

identical to the measured impedance). The higher Q is, the closer is the device to an ideal inductor. Figure 4 shows Q as a function of frequency, indicating that a distinct maximum (Q_{max}) develops at a certain frequency (f_0). From the model in Figure 3b it is obvious, that at low frequencies the increase of Q with frequency depends mainly on R_s , i.e., on the ohmic losses in the spiral coil. The decay of Q at high frequencies depends on C_{ox} and R_B (provided that C_p is small). The challenge in inductor design is therefore to tailor the layout of the spiral coil and the isolation from the silicon substrate in a way that the highest possible Q_{max} is obtained at the desired operating frequency f_0 .

A. Inductors Based on the Conservative Approach

The optimization of an inductor can be approached either in a conservative or an innovative way, as illustrated in Figure 4 [12]. The conservative approach considers the utilization of multi-level interconnects without any process alteration to achieve an optimum inductor design. The thickness of the conventional Al layers is limited to about $2 \mu\text{m}$, because Al interconnects are developed for high levels of integration, requiring a small metal pitch (metal pitch = min. metal width + min. metal space) of the order of $1\text{--}2 \mu\text{m}$. The ohmic losses in the spiral coil can therefore only be reduced if several layers of metal are shunted together, using dense arrays of via connections to achieve an effectively thicker metal layer (Fig. 5) [13, 14]. The resistivity of the

tungsten (W) vias is about three times as high as that of Al and limits the effectiveness of this approach somewhat [10]. Also, with a limited number of metal layers available, shunting several of them together to form the spiral coil, has the consequence that C_{ox} becomes larger than in the case when only the top metal layer is used for the

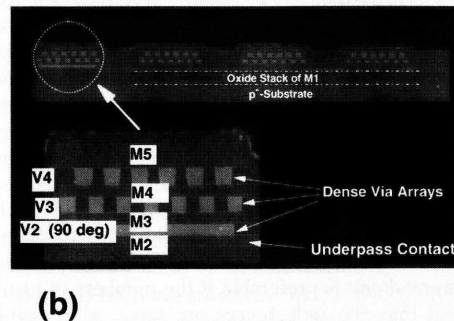
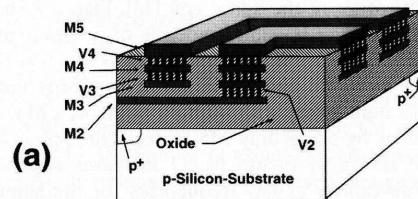


Figure 5. Schematic (a) and scanning electron micrograph (SEM) (b) of a five-level inductor structure.

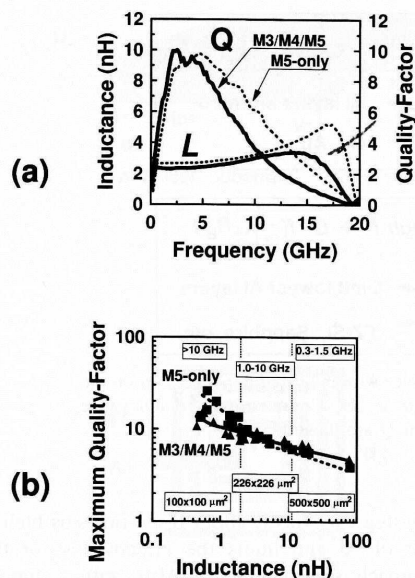


Figure 6. Inductance and quality-factor vs. frequency (a) and maximum quality factors vs. inductances (b) of five-level inductor structures using either the top metal layer (M5-only) or a shunted metal layer configuration (M3/M4/M5).

fabrication of the spiral coil [14]. Figure 6 shows the resulting possible tradeoffs of a conservative inductor design if three metal layers are available. The electrical characteristics of two 2-nH inductors, built either with shunted layers M3, M4, and M5 or by using only M5 to form the spiral coil, are shown in Figure 6a. Q increases somewhat more rapidly at low frequencies for the shunted structure compared to the single-layer inductor due to the lower coil resistance, but the Q falls off faster at high frequencies due to the larger oxide capacitance. $Q_{\max}$ is not very different for the two cases, but f_0 is lower for the inductor with shunted metal layers, indicating the window for tailoring the design of this device. There is, however, a difference in $Q_{\max}$ for smaller or larger inductance values (Fig. 6b). Coils with many turns and thus large inductance values suffer comparably more from the limited metal resistance, while inductors with few turns and small inductance values suffer mostly from the substrate losses. It is therefore obvious that the shunted coil is preferable if the numbers of turns and thus the inductances are large, while using only the top metal layer to form the spiral coil is

the better choice for small inductance values, due to the small C_{ox} .

In addition to the planar coil structure discussed so far, multilevel interconnects offer the possibility to fabricate inductor structures with several stacked spiral coils [8, 15]. Such an MLS inductor offers a larger average area enclosed by the wire turns compared to the planar spiral coil, resulting in a comparably larger inductance value for the same number of turns and the same outer dimensions. The disadvantage of this type of inductor is that C_p is considerably larger than that of a planar coil, causing a severe reduction of the self-resonant frequency (f_{SR}). The low f_{SR} not only limits the application of MLS inductors to low frequencies, but also causes that the inductance changes considerably with frequency near f_0 , which is often not desirable in circuit design. It becomes clear, that the MLS inductor will mainly find an application where a large inductance value at minimum area consumption in combination with a small DC resistance is needed without the requirement of an utmost control of the electrical characteristics, such as for RF chokes [8].

In the upper half of Table I, we have listed the key parameters of some inductor implementations based on the conservative approach. It is obvious that the reported $Q_{\max}$ values differ significantly. That depends in part on the different fabrication processes and lateral designs, but it is also very important to be reminded that for the same fabrication process a small inductance value typically combines with a higher $Q_{\max}$ than a large inductance, and *vice versa* (Fig. 6b) [14]. This observation does not necessarily present a limitation to inductor design. Fortunately, in some applications, large inductance values are needed at low frequencies, where a moderate Q can be sufficient. Lower inductance values are needed at high frequencies, where the spiral inductor inherently provides the required larger Q and f_{SR} . One can therefore say, that the spiral inductor on silicon is roughly scaleable with frequency. This trend is illustrated in Figure 6b, where the maximum Q s and the ranges of f_0 are drawn as a function of the inductance values of a wide variety of inductor dimensions and coil layouts. For other applications, such as in voltage-controlled oscillators, the highest possible Q s are required at high as well as at low frequencies [3]. For those cases, one can say that the application of an integrated inductor on silicon becomes more favorable at high frequencies.

TABLE I. Comparison of Published Inductor Results with Separation into Conservative and Innovative Device Structures and Fabrication Processes

Author(s)	Description	Area (μm^2)	Turns n	Induct. L (nH)	Quality Factor Q_{max}	Operating Freq. f_0 (GHz)	Resonance Freq. f_{SR} (GHz)
Conservative Inductor Designs							
Burghartz et al. [25], 1995	M3/M2/M1 on p^- -Si	226×226	3	1.45	24	2.3	> 20
Burghartz, Jenkins, and Soyuer [8], 1996	MLS on p^- -Si	226×226	8	6.8	7.8	1.3	5.6
Groves et al. [26], 1996	M3 on p^- -Si	$\sim 400 \times 400$	6	10.2	7.5	1	8
Kim and O [27], 1997	M3/M2/M1 on n -well	145×145	9.25	6	2.6	1.5	5.8
Merrill et al. [15], 1995	MLS on p^- -Si	$\sim 150 \times 150$	3	15.5	2.64	0.42	—
Nguyen and Meyer [2], 1990	M2 on p^- -Si	230×230	9	9.7	3	0.9	2.5
Soyuer et al. [13], 1995	M3/M2/M1 on p^- -Si	226×226	4	2.1	9.3	2.4	~ 20
Yue and Wong [28], 1997	M2 on perforated gnd	$\sim 280 \times 280$	6	8	7	1.8	3.5
Innovative Inductor Designs							
Ashby et al. [19], 1994	6 μm Au on HRS	300×300	2	2.88	12	3.2	> 10
Burghartz et al. [18], 1996	2.5 μm Cu on Sapphire	226×226	3	1.45	40	5.8	> 20
Burghartz et al. [3], 1998	4 μm Cu on Quartz	226×226	3	1.5	60	6	> 20
Chang, Abidi, and Gaitan [22], 1993	M2 on suspended Sub.	440×440	20	100			2.9
Dekker et al. [16], 1997	3.5 μm Al on Glass	$\varnothing 600 \mu\text{m}$	2	2.6	39	4.3	10.5
Johnson et al. [29], 1996	M2 on SOS	$\sim 150 \times 150$	5	4	11.9	~ 3.0	13.9
Park et al. [17], 1997	4 μm Al on HRS	290×290	8	11.98	15.3	3.25	~ 9.0
Sun et al. [23], 1996	M2 on suspended Sub.	$\sim 200 \times 200$	4	1.1	28	18	84

B. Innovative Inductor Structures

However, as seen, the conventional approach faces limitations set by the resistivity of the Al wires, the conductivity of the conventional silicon substrate, and the relatively small thicknesses of the dielectric and the metal films. Those limitations can be overcome by deviating from main stream silicon process technology. For instance, thicker Al wires can be realized at the expense of the metal pitch [16, 17]. A more dramatic reduction of the ohmic losses in the spiral coil is possible if the Al lines are replaced by Cu wires. The Cu-Damascene technology, which has recently been proposed for application in VLSI interconnects, offers about a twofold reduction in resistivity, thicker metal layers for a given metal pitch, and taller via connections (Fig. 7) [7]. Cu-interconnects can therefore be used to reduce R_s in comparison to an Al coil having the same dimensions; in the present experiment the Cu line thickness was 4 μm (inset of Fig. 8). Further, the vias between the metal layers are not necessarily limited in width, such as for tungsten (W) vias used in Al interconnects [5], which allows one to minimize R_s , as shown in the inset of Figure 8 as

well. The tall Cu-via connections, shown in Figure 7, can be utilized to space the spiral coil further away from the silicon as if it would be possible in an Al-interconnect scheme; the result is a comparably lower C_{ox} . A dramatic improvement of Q could therefore be demonstrated with Cu interconnects [3, 18]. Similar Q -values can be expected from Au interconnect structures, even though this technology does not currently enjoy the benefit of being driven by VLSI applications [19, 20].

For the reduction of the substrate losses, it seems first plausible to apply silicon substrates with a much higher resistivity, which is possible by using float-zone (FZ) instead of Czochralski material [6, 12, 18]. Such HRS substrates, however, are not likely suitable for the integration of dense circuitry. A good tradeoff between the requirements of circuit integration and inductor optimization is given with a combination of a silicon-on-insulator structure, which electrically isolates the active device silicon region from the bulk silicon, and a HRS substrate. This type of substrate has been advertised as MICROX [21]. SOI alone does not provide any significant benefit for inductor integration, because the buried oxide is

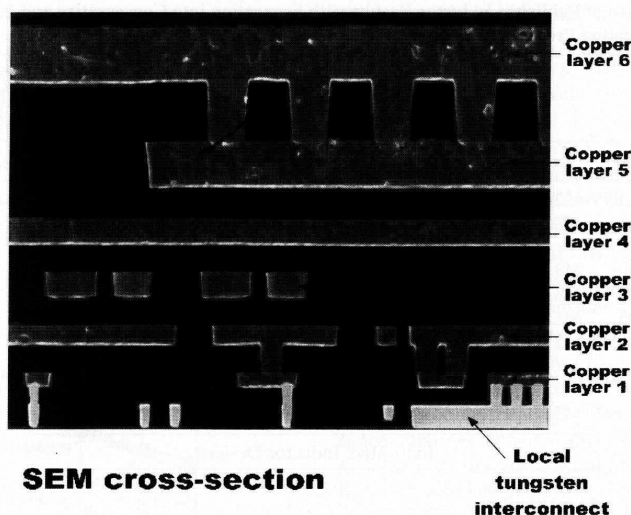


Figure 7. Cross-sectional SEM of a six-layer Cu-Damascene interconnect structure.

typically very thin and the skin depth at GHz-frequencies and for a conventional silicon resistivity is comparable to the substrate thickness [12]. Therefore, the substrate losses can only be eliminated by using either an insulating substrate ma-

terial or by removing the silicon under the spiral coil. Examples of the first option are silicon-on-sapphire substrates or bonding onto glass or quartz carrier wafers [3, 16, 18]. For the second option, micromachining techniques can be used to form a suspended inductor over a cavity of several hundreds of micrometer depth on a conventional silicon wafer [22, 23]. Such a micromachined inductor is an attractive solution toward a higher Q and operation at high frequency. Good compatibility with the active device fabrication is achieved in particular if postprocessing methods are used. Some concerns exist, however, with respect to the stability of such structures during plastic packaging. Farther on the horizon are other micromachining techniques which allow to fully exploit the vertical dimension and enable one to expand vertically from the strictly planar wafer surface in order to realize three-dimensional (3D), solenoidal inductors with eliminated or largely reduced substrate losses [24]. A summary of some published results on innovative inductor structures is given in the bottom part of Table I.

Figure 9 shows a comparison of conservative inductor implementations with the use of different numbers of metal levels to an innovative inductor design, which uses Cu-Damascene interconnects and a low-loss substrate. Inductor designs with three different areas are compared, 100×100 , 226×226 , and $500 \times 500 \mu\text{m}^2$. Within this range of area sizes, inductances in

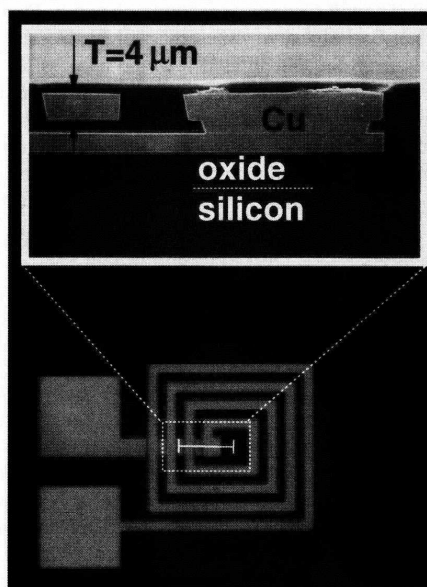


Figure 8. Plan view of a four-turn Cu spiral inductor, and cross-sectional view of the center part of the spiral coil (inset).

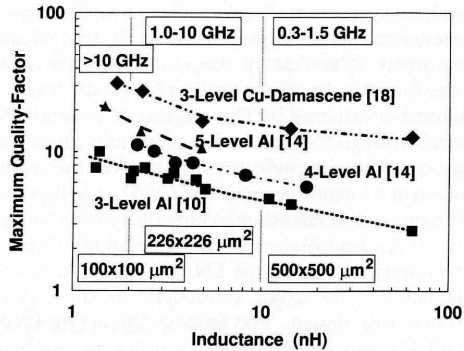


Figure 9. $Q_{\max}$ vs. inductance values for different inductor geometries and fabrication processes.

between 0.5 and 100 nH can be achieved. A 1.5-nH inductor, as an example, has a Q in the range of about 10–40, depending on the fabrication process.

III. INDUCTOR MODELING

Experience in the modeling of the planar spiral inductor has been gathered extensively over the past decades. Various analytical formula have been derived for the calculation of the inductance value for a given lateral layout of the spiral coil [4, 30]. Those models, however, are all based on the assumption of a lossless substrate material. However, as simple as it first seems to extend these models to the case of a lossy substrate, this task turned out to be extremely difficult and consequently has motivated active research in this area. The possible model approaches can be separated in (i) analytical–physical [31–33], (ii) analytical–semi-empirical [34], (iii) three-dimensional (3D) numerical [11], and (iv) inductor library models [10–12, 14, 18, 19]. The advantage of the first three types of models is that they attempt to calculate the electrical characteristics of an inductor structure *a priori*, while the library approach is limited to a fixed number of characterized inductor designs. The highest level of accuracy of the predictive inductor models is expected from the 3D approach. The narrow vertical dimensions of the spiral coil, however, have to be modeled in conjunction with the thick silicon substrate, making the modeling cumbersome and leading to long conversion times. A reasonable solution may come from partial-element equivalent circuit (PEEC) solvers which allow one to

simplify the description of the inductor structure wherever permissible to arrive at reasonable conversion times without sacrificing the level of accuracy too much [11, 35]. The analytical–physical models trade off accuracy for simplicity and are likely suitable only to achieve a rough estimate of the expected electrical characteristics [31–33]. The analytical–semi-empirical modeling approach derives an analytical inductor model from a large characterized inductor library to extrapolate to other inductor structures or implementations, using other fabrication processes [34]. An inductor library model is derived from one-port or two-port S -parameter measurements on fabricated devices. The impedance of the inductor relates to the measured impedance as $Z = Z_{11}$ for the one-port case and $Z = Z_{11} - 50 \Omega$ for the two-port case. Both the inductance $L = \text{im}(Z)/(2\pi f)$ and the quality factor $Q = \text{im}(Z)/\text{re}(Z)$ can be determined from Z . The inductance at low frequency is used in the model in Figure 3 as $L \approx L_s$. R_s in the model is derived from dc measurements, which is a good approximation as long as the skin effect in the metal lines is small. C_p and C_{ox} are calculated from the coil geometry. R_b is more or less a fitting parameter due to the 3D RF current flow in the silicon substrate.

It is the authors opinion, that the stringent requirements in the accuracy of inductor models for RF circuit design make a well characterized inductor library indispensable. Analytical or numerical predictive models may be instrumental in limiting the number of variations in the development of an inductor library, but they will not likely make such a library obsolete.

Figure 10 shows the comparison of the measured and the modeled inductance and Q values vs. frequency for a sample inductor. The schematic of the lumped-element model with the parameter values used is shown in the inset of Figure 10. It is obvious that the agreement of model and measured data is excellent at frequencies below f_{SR} .

IV. CIRCUIT LAYOUT ISSUES

The design of a spiral inductor for use in an integrated RF circuit is not only crucial because the Q of the inductor is low in comparison to other passive RF components. The structure also occupies a large silicon area, crosstalk between inductors potentially limits the flexibility in circuit layout, and the local definition of the substrate bias by a substrate contact can affect the inductor

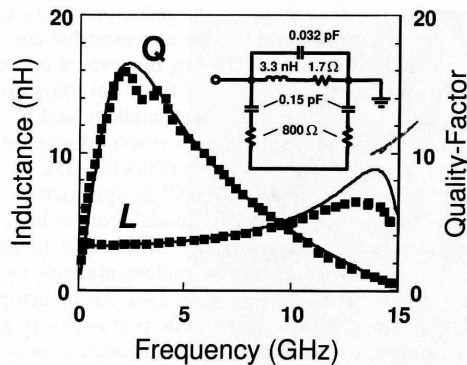


Figure 10. Comparison of measured and modeled inductor characteristics of a copper (Cu) inductor, with the lumped-element model parameters in the inset.

characteristics [3, 11]. The area of an inductor can to some extent be minimized by optimization of the conductor width and the space between the turns of the spiral coil without deviating from the desired inductance value, without sacrificing the Q , and without shifting f_0 significantly [3]. This can be understood as follows: the resistance of the coil wire increases with frequency as a result of the skin effect, which causes that the rf current mainly flows near the edges of the conductor. An increase of the wire width to lower the resistance and enhance the inductor's Q may therefore not be effective. On the contrary, a wider conductor increases the oxide capacitance (C_{ox} in Fig. 3b) and thus the substrate losses, leading eventually to a lower Q_{max} at a reduced f_0 . The minimization of the wire width can therefore have two benefits, i.e., it can allow for a small inductor area and for the highest possible Q_{max} at a maximum f_0 . For a minimum inductor area, the space between the turns (S in Fig. 2b) must be minimized as well. The reduction of S , however, leads to an increase of C_p which must be kept below a certain value in order to maintain a sufficiently high f_{SR} . We had mentioned in Section II.A that the stacking of spiral coils to form an MLS inductor provides an inductance-area that is larger than that of a planar spiral coil at the expense, however, of a severe reduction of f_{SR} [8]. Also in the MLS structure, it is the large C_p that causes f_{SR} to be small.

Crosstalk between inductors can be inductive and capacitive. The inductive coupling between spiral inductors depends significantly on the lateral spacing, but even for adjacent inductors the insertion loss is very low, as long as no capacitive

coupling is present [36]. Capacitive coupling, however, exists on silicon substrates. If the silicon resistivity is sufficiently high, the insertion loss was found to be of the order of -40 dB for the closest proximity [3]. This degree of crosstalk is small enough not to be of concern in most cases, except if on-chip inductors are used in the input stage of a low-noise amplifier (LNA) as well as for the output impedance matching of a power amplifier (PA). An isolation of the order of 80 dB may be required between the LNA and the PA, which is one of the major challenges in single-chip transceiver design. The isolation between LNA and PA can be improved by using an external impedance matching network for the PA or by providing improved AC device isolation [28, 37, 38].

A third circuit layout issue results from the fact that the silicon substrate resistivity is high to provide a large Q_{max} at a high f_0 and a high f_{SR} . The substrate bias is therefore not uniform, as it would be for very conductive silicon or for a metal ground plane. The electrical characteristics of a spiral inductor on silicon can therefore be affected by the proximity of a substrate contact, as Figure 3b illustrates. The position of a substrate contact with respect to the spiral coil of the inductor is modeled there as a lumped resistance R_{Sub} . It has been shown recently that a substrate contact can have a beneficial or a detrimental effect on the inductor- Q , depending if the device is configured as a one-port or a two-port structure. The increase in Q_{max} in case of the one-port configuration, however, is traded against a reduced f_{SR} [11].

V. SUMMARY AND OUTLOOK

Different types of inductor structures on silicon substrates, the modeling issues, and circuit layout aspects have been discussed in this paper. It has been shown that for the inductor integration either a conservative or an innovative approach can be taken, depending if the compatibility with mainstream silicon processing or the highest possible Q is the primary goal. Practical inductance values range from 0.5 to 100 nH, and Q_{max} can be made as high as 25 for conservative and 40 for innovative implementations. Various modeling efforts are underway, ranging from a fully analytical, physical model to a fitted lumped-element library model. Given the complexity of the three-dimensional spiral inductor on the lossy silicon

substrate, the conventional approach in analog circuit design of developing a characterized device library may also be indispensable for spiral inductors. The conductivity of the silicon substrate makes it necessary to consider potential crosstalk and substrate contact effects in circuit layout. Overall, the spiral inductor on a silicon substrate is a feasible device today. It can be expected that integrated inductors will be extensively used in silicon RF circuit design.

ACKNOWLEDGMENTS

The author would like to acknowledge his colleagues at IBM, and in particular Keith Jenkins, Mehmet Soyuer, Dan Edelstein, and Albert Ruehli, for the many stimulating discussions on rf and silicon technology issues over the past years.

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