

Fei Yuan



CMOS Active Inductors and Transformers

Principle, Implementation, and Applications

 Springer

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Fei Yuan
Department of Electrical and Computer Engineering
Ryerson University
Toronto, Ontario, Canada

ISBN 978-0-387-76477-1

e-ISBN 978-0-387-76479-5

Library of Congress Control Number: 2008925091

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PART I

PRINCIPLE AND IMPLEMENTATION OF CMOS ACTIVE INDUCTORS & TRANSFORMERS

Chapter 1

INTRODUCTION

CMOS spiral inductors and transformers have found a broad range of applications in high-speed analog signal processing including impedance matching and gain-boosting in wireless transceivers, bandwidth improvement in broadband data communications over wire and optical channels, oscillators and modulators, RF bandpass filters, RF phase shifters, RF power dividers, and coupling of high-frequency signals, to name a few. Traditionally, passive inductors and transformers are off-chip discrete components. The need for off-chip communications with these passive components severely limits the bandwidth, reduces the reliability, and increases the cost of systems. Since early 1990s, a significant effort has been made to fabricate inductors and transformers on a silicon substrate such that an entire wireless transceiver can be integrated on a single substrate monolithically. In the mean time, the need for a large silicon area to fabricate spiral inductors and transformers has also sparked a great interest in and an intensive research on the synthesis of inductors and transformers using active devices, aiming at minimizing the silicon consumption subsequently the fabrication cost and improving the performance.

This chapter looks into the characteristics of spiral and active inductors and transformers, both their advantages and limitations, and the impact of these characteristics on the applications of these devices. Section 1.1 demonstrates the critical need for an inductive characteristic in high-speed applications. The characteristics of spiral inductors and transformers are examined in Section 1.2. In Section 1.3, we investigate the pros and cons of active inductors and transformers. The chapter is summarized in Section 1.4.

1.1 Inductive Characteristics in High-Speed Applications

Inductive characteristics are critically needed in high-speed applications to improve the performance of the systems, such as improving bandwidth and

boosting gain, and to perform specific tasks, such as impedance matching and frequency selection. These applications include LC tank oscillators, bandwidth enhancement in broadband communications, impedance matching in narrow-band communications, phase shifting for RF antennas and radars, RF power dividers, frequency selection, in particular, RF bandpass filters, RF power amplifiers, and gain boosting of RF low-noise amplifiers.

1.1.1 LC Oscillators

One of the key applications of inductors and transformers in wireless communications is the construction of LC oscillators. As compared with ring oscillators, LC oscillators with spiral inductors or transformers offer the key advantage of a low level of phase noise. They are widely used in wireless communication systems where a stringent constraint on the phase noise of oscillators exists. Frequency tuning of LC oscillators with spiral inductors or transformers is typically done by varying the capacitance of the LC tanks as the inductance tuning of spiral inductors or transformers in a monolithic integration is rather difficult. These variable capacitors are usually realized using MOS varactors and offer a relatively small capacitance tuning range, subsequently a small frequency tuning range of the oscillators. Because the need for the frequency tuning range in narrow-band wireless applications is much relaxed as compared with that for clock and data recovery in broadband data communications over wire lines or optical channels, the capacitance-based frequency tuning usually provides an adequate frequency tuning range. Table 1.1 compiles some of the recently published work on LC oscillators with either spiral inductors or spiral transformers.

1.1.2 Bandwidth Improvement

Bandwidth is of a critical concern in broadband communications, such as optical front-ends and data communications over wire links. The bandwidth of a circuit is set by the time constant of the critical node, i.e. the node that has the largest time constant, of the circuit. Three approaches, namely *inductive peaking*, *current-mode signaling*, and *distributed amplification*, are widely used to improve the bandwidth of circuits.

- *Inductive peaking* - The idea is to place an inductor at the node where a large nodal capacitance exists such that the first-order RC network associated with the node is replaced with a second-order RLC network. Because a RLC network has three different modes of operation, namely over damped, critically damped, and under damped. The bandwidth in these three cases differs with under-damped RLC systems exhibit the largest bandwidth. Both shunt peaking [11, 12] and series peaking [13], have been used, as shown

Table 1.1. Performance comparison of CMOS spiral inductor / transformer LC VCOs.

Reference	Tech.	f_o [GHz]	Tuning range	Phase [dBc/Hz]	Power [mW]
Straayer <i>et al.</i> [1] (2002)	0.35 μ m	1.7	6.3%	-138@0.6MHz	35*
Baek <i>et al.</i> [2] (2003)	0.18 μ m	8.08-7.83	3%	-108@1MHz	24*
Wang <i>et al.</i> [3] (2003)	0.18 μ m	5.75-5.95	3.4%	-105@5MHz	18*
Gierkink <i>et al.</i> [4] (2003)	0.25 μ m	4.57-5.21	13%	-124@1MHz	21.9*
Choi <i>et al.</i> [5] (2004)	0.25 μ m	1.5	–	-100@1MHz	28.8*
Dehghani & Atarodi [6] (2004)	0.25 μ m	5.8	4.4%	-134.6@3MHz	5.8
Kim <i>et al.</i> [7] (2004)	0.25 μ m	2.27	–	-137@1MHz	30*
Chang & Kim [8] (2005)	0.18 μ m	5.5-6.7	20%	-115@1MHz	5.76
Oh & Lee [9] (2005)	0.18 μ m	11	2.73%	-109.4@1MHz	6.84
Soltanian & Kinget [10] (2006)	0.25 μ m	1.755-2.123	19%	-120@0.6MHz	2.25

1. Legends : TVCO - Transformer VCO; QVCO - Quadrature VCO.
2. VCO proposed by Choi *et al.* is a source-injection quadrature VCO.
3. VCO proposed by Chang and Kim is a cascode-coupling quadrature VCO.
4. VCO proposed by Gierkink *et al.* is a super-harmonic coupled VCO.
5. VCO proposed by Oh and Lee is a back-gate transformer feedback VCO.
6. VCO proposed by Soltanian and Kinget is a tail-current shaped VCO.
7. * Total power consumption including buffers. Otherwise, the power consumption of oscillator core only.

in Fig.1.1. It was demonstrated in [11, 12] that inductive shunt peaking can improve the bandwidth of a common-source amplifier by as much as 70%.

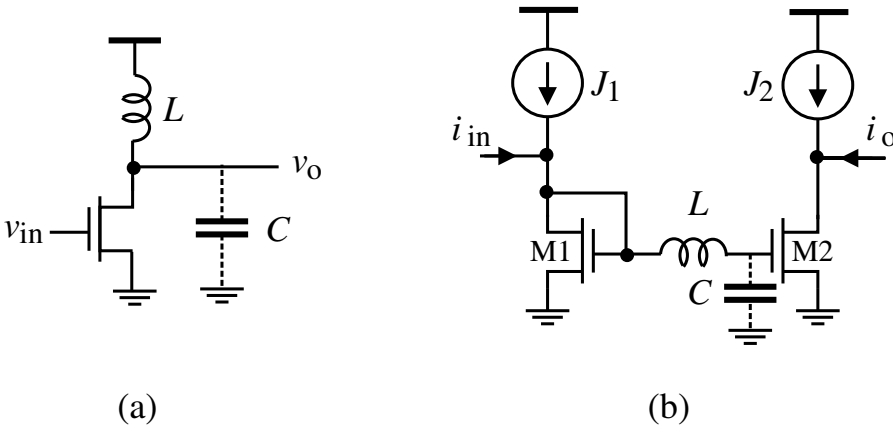


Figure 1.1. Inductive peaking. (a) Shunt peaking - The peaking inductor L is in parallel with the dominant capacitor C . (b) Series peaking - The peaking inductor L is in series with the dominant capacitor C .

- *Current-mode signaling* - A circuit is classified as current-mode if the information carriers of the circuit are the branch currents of the circuit. A key distinction between current-mode and voltage-mode circuits is that the nodal impedance of current-mode circuits is low whereas that of voltage-mode circuits is high. This distinct characteristic forms the foundation on which current-mode circuits are designed. Since the information processed by a current-mode circuit is represented by the branch currents rather than nodal voltages of the circuit, the swing of the nodal voltages of the circuit can be made small without sacrificing the fidelity of the signal. Current-mode circuits offer an improved bandwidth due to the following reasons : (i) Low nodal impedances - the low nodal impedances of current-mode circuits lower the nodal time constants of the circuits. (ii) Low voltage swing - the small swing of the nodal voltages of current-mode circuits reduces the amount of the time required to charge and discharge the nodes of the circuits [14]. It should be emphasized that the speed improvement using current-mode signaling is often moderate as lowering the nodal impedance of a nodal is often echoed with an increase in the capacitance of the node at the same time. Because each node is essentially a first-order RC network whose time constant is given by $\tau_n = R_n C_n$, where R_n and C_n denote the resistance and capacitance of the node, respectively, the net reduction in the nodal time constant is rather moderate.

- *Distributed amplification* - As pointed out earlier that the bandwidth or speed of a circuit is set by the time constant of the critical node of the circuit. An effective way to minimize the effect of the large shunt capacitance of the critical node is to break the large shunt capacitor into several smaller shunt capacitors and separate them with inductors such that the large shunt capacitor is replaced with a distributed LC network or a transmission line [15, 16]. Shown in Fig.1.2 is a common-source amplifier where an shunt-peaking inductor is employed at the drain of the transistor to offset the effect of the large output capacitance C arising from the large width of the transistor. Inductive shunt-peaking, though effective, can not deliver the needed bandwidth in this case. Notice that a transistor is typically laid out in a multi-finger fashion. This is equivalent to connecting N smaller transistors whose width is only $1/N$ of that of the original transistor in parallel, as shown in the figure, where N is the number of the fingers of the transistor. Inductors can then be employed to separate these small transistors and form two transmission lines, one at the drain and the other at the source. Resistors R_{1-4} are for the purpose of impedance matching.

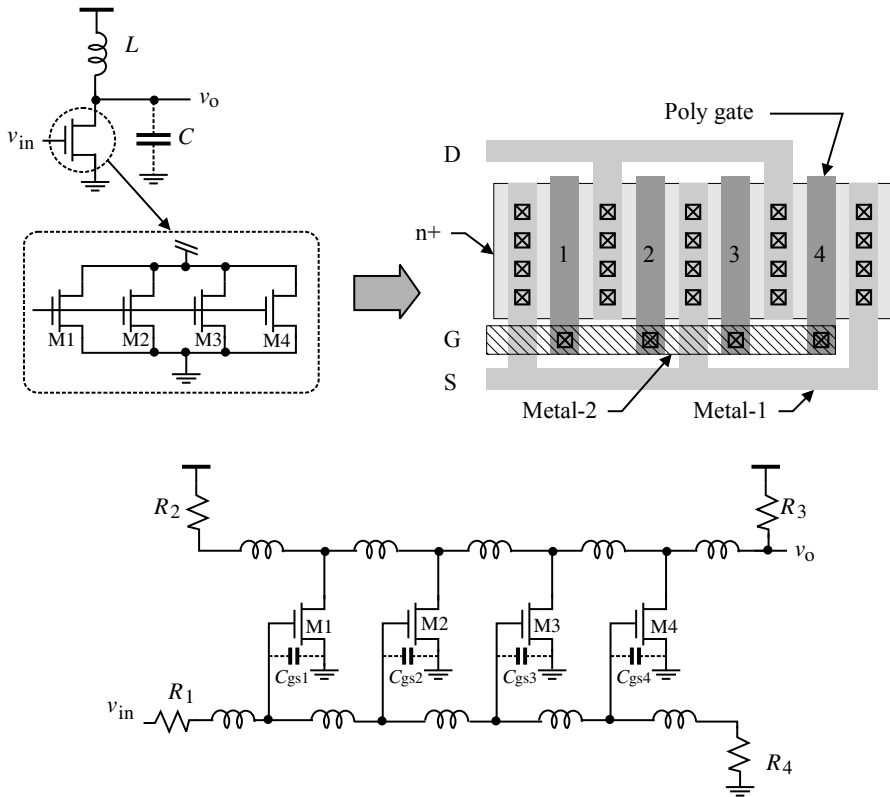


Figure 1.2. Distributed amplifiers.

1.1.3 Impedance Matching

Impedance matching is required between channels and high-speed circuits to minimize signal reflection at their interfaces. Resistors are usually used to provide a matching impedance in broadband communication systems as impedance matching is required over a broad frequency spectrum, as shown in Fig.1.3 where a shunt resistor termination at the far end of the channels is employed. Active termination where transistors are used as termination devices has also been used recently to take the advantage of the tunability of the termination resistance [14]. Frequency-dependent elements, such as capacitors and inductors, can not be used for impedance matching in broadband communication systems simply due to their frequency-dependent characteristics.

Most wireless communication systems operate in a narrow-band mode. A matching impedance in this case is only required over a very narrow frequency

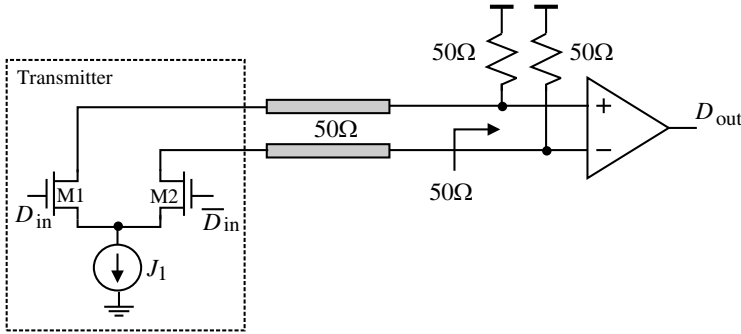


Figure 1.3. Impedance matching in high-speed current-mode serial links.

range. Although resistors can be used for these applications, the high level of the thermal noise of resistors disqualifies themselves from being used in wireless communications where a stringent constraint on the noise performance of the systems exists. Instead, noiseless elements such as capacitors and spiral inductors are widely used in narrow-band impedance matching because these frequency-dependent noiseless elements can provide the desired impedance in a narrow frequency band and at the same time keep the noise at the minimum [17, 18]. Shown in Fig.1.4 is a widely used termination scheme for narrow-band low-noise amplifiers. Neglecting C_{gd} and other parasitic capacitances, it is elementary to show that the input impedance of the LNA is given by

$$z_{in} = \left[j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs1}} \right] + \frac{g_{m1}L_2}{C_{gs1}}, \quad (1.1)$$

where C_{gs1} and g_{m1} are the gate-source capacitance and transconductance of M_1 , respectively. It is seen from (1.1) that the first term on the right hand side of (1.1) is reactive while the second term is resistive. The reactive term can be made zero by imposing

$$\omega(L_1 + L_2) - \frac{1}{\omega C_{gs1}} = 0. \quad (1.2)$$

The input impedance of the LNA in this case becomes purely resistive and is given by

$$z_{in} = \frac{g_{m1}L_2}{C_{gs1}}. \quad (1.3)$$

The need for two inductors L_1 and L_2 with L_1 at the gate and L_2 at the source is justified as the followings : Once the dimension of M_1 is chosen, g_{m1} and

C_{gs1} are determined. The desired input impedance of the LNA in this case can be obtained by adjusting L_2 . Once L_2 is chosen, the value of L_1 can be tuned to ensure the total cancellation of the reactive part of the input impedance.

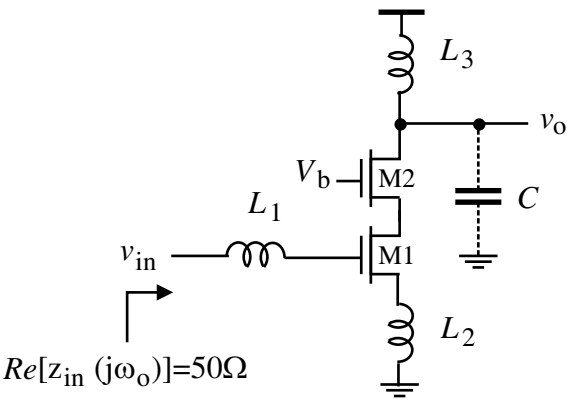


Figure 1.4. Impedance matching in narrow-band low-noise amplifiers.

1.1.4 Phase Shifting

A phase shifter is a uni-directional serial network inserted in a signal path so that the phase of the signal at the output of the signal path can be adjusted in a controlled manner [19, 20]. A well-designed phase shifter should possess the characteristics of a low insertion loss, a high return loss, and a large phase shift range. The common configuration of RF phase shifters is shown in Fig.1.5. The floating inductors are typically implemented using high-impedance metal lines. The tuning of the amount of the phase shift is carried out by varying the capacitance of the shunt varactors.

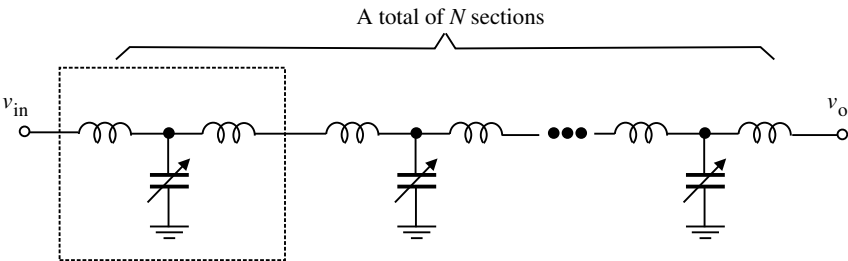


Figure 1.5. RF phase shifters with floating inductors and shunt varactors.

1.1.5 Frequency Selection

Bandpass filters with a high passband center frequency are used extensively in narrow-band wireless communications for RF band selection. These filters are traditionally implemented using lumped LC and surface acoustic wave (SAW) filters with SAW filters the most widely used. SAW filters, however, are not compatible with CMOS technologies. The recent effort on integrating RF bandpass filters on a silicon substrate is accelerated with the emergence of CMOS spiral inductors and transformers. A single-chip realization of RF transceivers with on-chip RF bandpass filters offers a number of critical advantages including a reduced assembly cost, increased system reliability, and improved performance. To compensate for the high insertion loss of spiral inductors at high frequencies, active negative resistors have been used to boost the quality factor of the spiral inductors. Table 1.2 tabulates some recently reported RF bandpass filters with spiral inductors and active Q-enhancement.

Table 1.2. Bandpass filter with Q-enhanced spiral inductors.

Reference	Year	Tech.	f_o	Tuning range
Kuhn <i>et al.</i> [21]	1997	2 μ m	0.2 GHz	4.5%
Duncan <i>et al.</i> [22]	1997	0.8 μ m	0.75 GHz	2.3%
Soorapanth-Wong [23]	2002	0.25 μ m	2.14 GHz	1.4%
Dulger <i>et al.</i> [24]	2003	0.35 μ m	2.1 GHz	13%
Kuhn <i>et al.</i> [25]	2003	-	0.9 GHz	2.2%
Bantas-Koutsoyannopoulos [26]	2004	0.35 μ m	1 GHz	11%
Kulyk-Haslett [27]	2006	0.18 μ m	2.368 GHz	1.3%

1.1.6 Gain Boosting

Traditional gain-boosting techniques such as cascodes and regulated cascodes lose their potency at high frequencies due to the increased gate-source and gate-drain couplings via the gate-source and gate-drain capacitors of MOSFETs. A technique that is widely used in boosting the voltage gain of narrow-band low-noise amplifiers (LNAs) is to use a LC tank as the load of the LNAs, utilizing the infinite impedance of ideal LC tanks at their self-resonant frequency. When a LC tank is used as the load of a common-source amplifier whose voltage gain is approximated by $A_v \approx -g_m z_L$, where g_m is the transconductance of the MOSFET and z_L is the load impedance, as shown in Fig.1.6, the large impedance of the LC tank at its self-resonant frequency $\omega_b = \frac{1}{\sqrt{L_p C}}$

will significantly boost the gain of the amplifier at ω_0 . The resonant frequency of the tank is set to be the same as the frequency of the input of the LNA. Note that voltage gain of the amplifier at frequencies other than ω_0 is low.

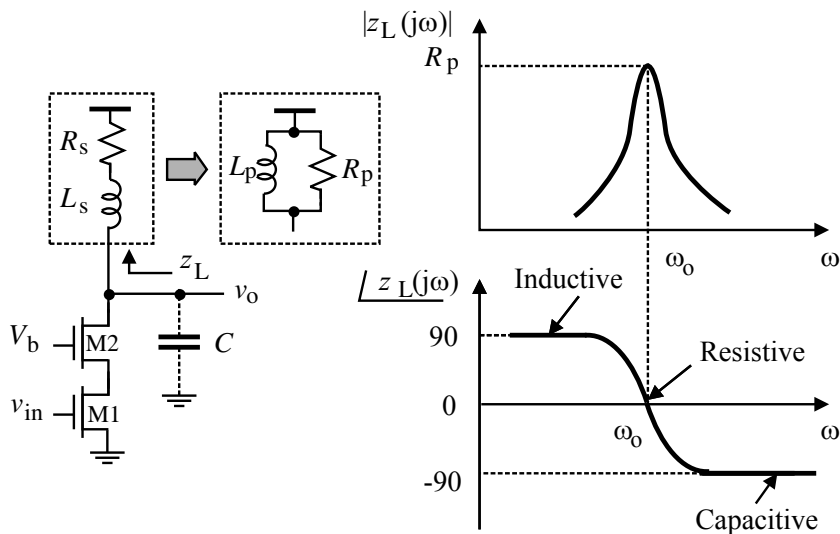


Figure 1.6. Gain boosting of low noise amplifiers using LC tank load.

1.1.7 Power Dividers

RF power dividers are traditionally realized using transmission lines. Lumped passive implementation of power dividers has also been used to reduce the size of the power dividers, however, at the cost of a high insertion loss and a limited bandwidth. Fig.1.7 shows the equivalent circuit of lumped Wilkinson power divider. The use of CMOS active inductors to replace passive spiral inductors of RF power dividers was proposed by Lu and Wu in [28] to take the advantages of the high quality factor, low silicon consumption, and high self-resonant frequency of CMOS active inductors.

1.2 Spiral Inductors and Transformers

Monolithic on-chip inductors and transformers are also known as spiral inductors and transformers due to the way in which these inductors and transformers are laid out. Both planar and stacked spiral inductors and transformers have been developed and the detailed characterization and modeling of these inductors and transformers are available. Modern CAD tools for IC design are equipped with spiral inductors as standard elements in their component libraries.

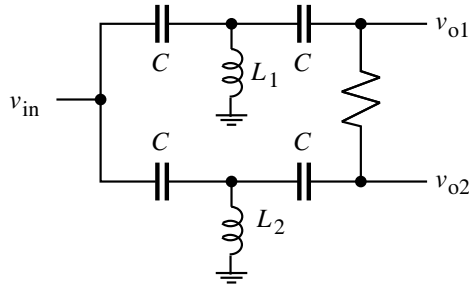


Figure 1.7. Equivalent circuit of lumped Wilkinson power divider.

1.2.1 Planar Spiral Inductors

Fig.1.8 is a sketch of square-shaped planar spiral inductors. The lumped equivalent circuit of spiral inductors is given in Fig.1.9, where L is the inductance of the spiral inductor, R_s represents the series resistance of the spiral caused by the skin-effect induced resistance in the spiral and the resistance induced by the eddy current in the substrate [29], C_s accounts for the capacitance due to the overlap of the spiral and the center-tap underpasses, C_{ox} denotes the capacitance between the spiral and the substrate, C_b and R_b quantify the capacitance and resistance of the substrate, respectively. Although modern CMOS technologies are equipped with multiple metal layers, typically only the top metal layer is used to construct planar spiral inductors and transformers such that the unwanted parasitic capacitance between the spiral and the substrate is minimized. As pointed out in [29], the substrate loss accounts for 10-30% reduction of the quality factor of the spiral inductors in low GHz ranges, mainly due to the penetration of the electric field generated by the spiral into the substrate. A main drawback of planar spiral inductors is their low inductance.

1.2.2 Stacked Spiral Inductors

The inductance of spiral inductors can be increased significantly using stacked configurations, as shown in Fig.1.10, however, at the price of an increased spiral-substrate capacitance because the lower metal layers are also used in the construction of the inductors [30]. The total inductance of a stacked inductor with two spiral layers is given by

$$L_{total} = L_1 + L_2 + 2M, \quad (1.4)$$

where L_1 and L_2 are the self-inductances of spirals 1 and 2, respectively, and M is the mutual inductance between the two spirals. Note the direction of the routing of the spirals in differential metal layers must be carefully

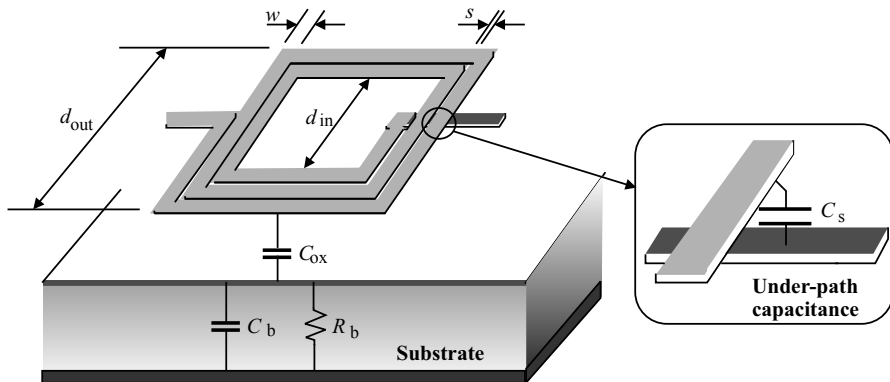


Figure 1.8. Square-shaped planar spiral inductors. w is the width of the spiral and s is the spacing between the turns of the spiral.

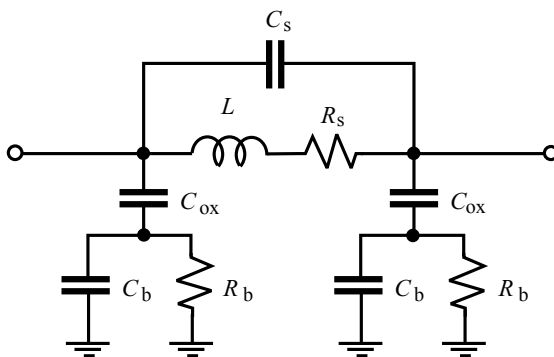


Figure 1.9. Lumped circuit model of planar spiral inductors.

chosen such that the total inductance increases. Figs.1.11 and 1.12 show the dependence of the measured inductance and self-resonant frequency of stacked inductors on the number of spiral layers [30]. It is seen that the inductance of stacked spiral inductors increases approximately linearly with the increase in the number of the spiral layers of the inductors. The self-resonant frequency of stacked inductors decreases with the increase in the number of spiral layers in a nonlinear fashion.

1.2.3 Spiral Transformers

To increase the inductance without significantly increasing silicon consumption, stacked spiral transformers and bilifar spiral transformers emerged. Transformers are essentially two spiral inductors coupled via a magnetic link.

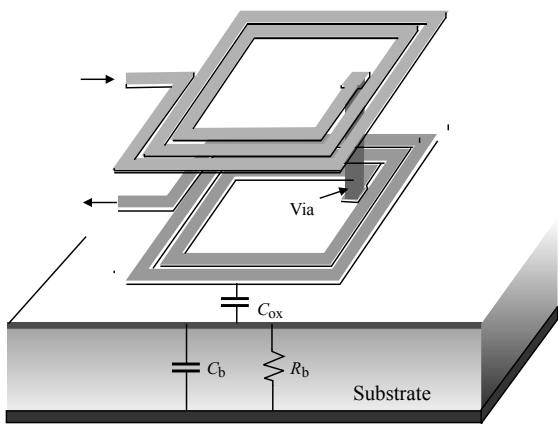


Figure 1.10. Square-shaped stacked spiral inductors.

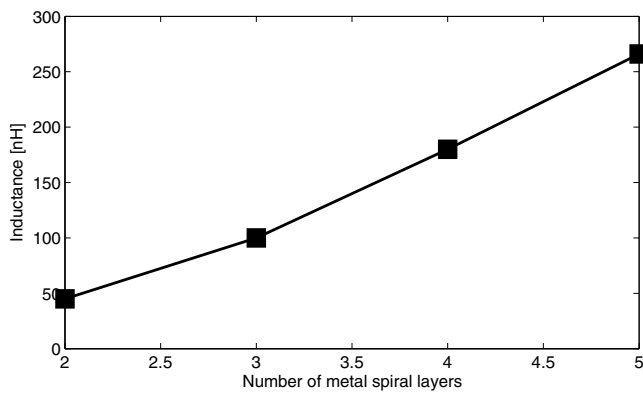


Figure 1.11. Dependence of the inductance of stacked spiral inductors on the number of spiral layers.

Fig.1.13 shows the lumped circuit model of bifilar spiral transformers [31], where C_{12} is the mutual capacitance between the primary and secondary windings, and k_{12} , k_{21} are the coupling coefficients. All other parameters are the same as those in Fig.1.9.

1.2.4 Characteristics of Spiral Inductors and Transformers

Spiral inductors and transformers offer the key advantages of superior linearity and a low level of noise. The performance and applications of spiral inductors and transformers are affected by a number of drawbacks that are intrinsic to the physical geometry of these passive devices and CMOS tech-

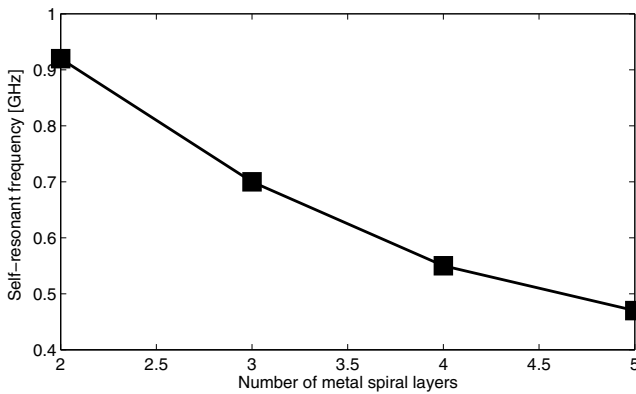


Figure 1.12. Dependence of the self-resonant frequency of stacked spiral inductors on the number of spiral layers.

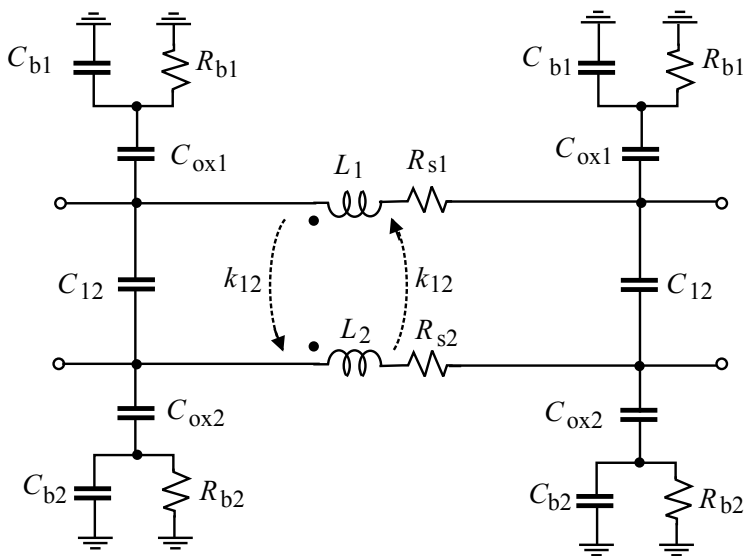


Figure 1.13. Lumped circuit model of spiral transformer.

nologies in which spiral inductors and transformers are implemented. These drawbacks include :

- *Low quality factor* - The quality factor of spiral inductors and transformers is limited by the ohmic loss of the spiral at high frequencies. Two sources that contribute to the ohmic loss of the spiral inductors and transformers exist : the skin-effect induced resistance of the spiral and the resistance

induced by the eddy currents in the substrate. The former is proportional to the square-root of the frequency of the signal flowing in the spiral whereas the latter is proportional to the square of the frequency of the signal flowing in the spiral. Because the resistance of the substrate in the lateral direction is much larger as compared with that in the vertical direction [32], the eddy currents in the lateral direction in the substrate are small. The substrate eddy-current induced resistance of the spiral is often negligible as compared with the resistance caused by the skin-effect [23]. The quality factor of spiral inductors in standard CMOS is typically below 20, as is evident in Table 1.3 where the parameters of some recently reported CMOS spiral inductors are tabulated.

- *Low self-resonant frequency* - The self-resonance of a spiral inductor is the resonance of the LC tank formed by the series inductance of the spiral inductor and the shunt capacitance between the spiral of the inductor and the substrate, as well as its underpass capacitance. The low self-resonant frequency of spiral inductors is mainly due to the large spiral-substrate capacitance, arising from the large metal area occupied by the spiral. The typical self-resonant frequency of spiral inductors is in the low GHz range, as is evident in Table 1.3.
- *Low and fixed inductance* - As pointed out earlier that the inductance of a planar spiral inductor is low and fixed once the number of the turns of the spiral is set. The only way to increase the inductance of the spiral inductor is to either increase the number of the turns of the spiral or use a stacked configuration where spirals on multiple metal layers are connected using vias. The former is at the expense of a large silicon area while the latter increases the spiral-substrate capacitance.
- *Large silicon area* - Due to the low inductance of spiral inductors, especially planar spiral inductors, and the fact that the inductance of these inductors is directly proportional to the number of the turns of the spiral of the inductors, the silicon area required for routing the spiral of the inductors is large. As an example, it was shown in [11] that a square-shaped spiral inductor of an inductance 8 nH will require 6 turns with $d_{out} = 400\mu m$. The actual silicon consumption of the inductor is larger than $400 \times 400 \mu m^2$ when design rules on the minimum spacings are followed. Moreover, the design rules of most IC foundries prohibit the placement of either active or passive devices in the region between the spiral of the inductors and the substrate, making spiral inductors the most silicon-consuming components.

Table 1.3. Key parameters of some CMOS spiral inductors.

Structure	Inductance [nH]	d_{out} [μm]	Turns	$Q(\omega_o)$	f_o [GHz]	Year	Ref.
Square	3.5	330	4	11	3.9	1996	[21]
Square	<6	–	7	<6	1	1996	[33]
Square	15.2	310	8	<4	1.5	1998	[34]
Square	8	400	6	–	–	1999	[11]
Octagon	6	320	4	11	1.4	2003	[35]
Octagon	4.3	200	3	5	4	2003	[36]

1.3 Active Inductors and Transformers

CMOS active inductors are active networks that consist mainly of MOS transistors. Resistors are sometimes used as feedback elements to improve the performance of active inductors. Under certain dc biasing conditions and signal-swing constraints, these networks exhibit an inductive characteristic in a specific frequency range. As compared with their spiral counterparts, CMOS active inductors offer the following attractive advantages :

- *Low silicon consumption* - Because only MOS transistors are usually required in the realization of CMOS active inductors and the inductance of these active inductors is inversely proportional to the transconductances of the transistors, the silicon consumption of CMOS active inductors is negligible as compared with that of their spiral counterparts.
- *Large and tunable self-resonant frequency* - CMOS active inductors with a large self-resonant frequency are highly desirable. For example, the pass-band center frequency of an active inductor RF bandpass filter is typically set to the self-resonant frequency of the active inductor of the filter. The larger the self-resonant frequency of the active inductor, the higher the passband center frequency of the filter. In applications where CMOS active inductors are used for low-pass filters, these filters are operated at frequencies below their self-resonant frequency of active inductors. A large self-resonant frequency of active inductors ensures that the active inductors will have an inductive characteristic over a large frequency range. As to be seen in Chapter 2 that the self-resonant frequency of a CMOS active inductor is the maximum frequency of the transconductors constituting the active inductor. When the basic configurations of transconductors, such as common-source

and common-gate transconductors, are used, this frequency approaches f_T of the devices.

- *Large and tunable inductance* - As to be seen in Chapter 2, the inductance of CMOS active inductors is inversely proportional to the transconductances of the transistors synthesizing the inductors. The smaller the width of the transistors, the larger the inductance. Also the inductance can be tuned conveniently by varying the dc biasing condition of the transistors synthesizing the inductor with a large inductance tuning range. The coarse tuning of the inductance of active inductors is typically attained in this way. The fine tuning of the inductance of active inductors can also be achieved by varying the load capacitance of the transconductors of the active inductors using MOS varactors.
- *Large and tunable quality factor* - The quality factor of CMOS active inductors is set by the ohmic loss of the inductors, arising mainly from the finite output resistance of the transconductors of the inductors. The quality factor of CMOS active inductors can be increased by increasing this output resistance. A number of methods are available to boost the output resistance, such as cascodes, regulated cascodes, and negative resistor compensation. In each of these approaches, the degree of compensation can be varied. For example, in the cascode approach, the output resistance of a cascode-configured transconductor can be adjusted by varying the biasing voltage of the cascoding transistor. In the regulated cascode approach, the output resistance of the regulated-cascode configured transconductor can be changed by varying the voltage gain of its auxiliary voltage amplifier. In the negative resistor compensation approach, the resistance of the compensating negative resistor can be adjusted by varying the biasing current of the negative resistor. A detailed presentation of these approaches will be given in Chapter 2.
- *Compatibility with digital CMOS technologies* - Spiral inductors are not available in low-cost digital-oriented CMOS processes. They are available only in more expensive mixed-mode CMOS technologies. CMOS active inductors, however, can be realized using standard digital CMOS processes.

CMOS active inductors and transformers have found increasing applications in areas where an inductive characteristic is required. These applications include LC and ring oscillators, RF bandpass filters, RF phase shifters, limiting amplifiers for optical communications, low-noise amplifiers for wireless communications, RF power dividers, ultra wideband low-noise amplifiers, and transceivers for high-speed data links over wire lines. Table 1.4 summarizes some of the recently published work where CMOS active inductors and transformers were employed.

Table 1.4. Applications of CMOS active inductors and transformers.

Reference	Year	Tech.	Applications	Remarks
Thanachayanont & Payne [37]	2000	0.8 μ m	IF Bandpass	100 MHz
Thanachayanont [38]	2000	0.8 μ m	LC VCO	0.45-1.2 GHz
Lin & Payne [39]	2000	0.35 μ m	LC VCO	1.1-2.1 GHz
Säckinger & Fischer [40, 41]	2000	0.25 μ m	Limiting amp.	3 GHz
Wu <i>et al.</i> [42]	2001	0.35 μ m	LC VCO	0.1-0.9 GHz
Grözing <i>et al.</i> [43, 44]	2001	0.30 μ m	LC VCO	0.4-4 GHz
Wu <i>et al.</i> [45, 46, 36]	2001	0.35 μ m	RF bandpass	0.4-1.1 GHz
Thanachayanont [47]	2002	0.35 μ m	RF bandpass	2.4-2.6 GHz
Xiao & Schaumann [48]	2002	0.18 μ m	RF lowpass	4.57 GHz
Xiao <i>et al.</i> [49]	2004	0.18 μ m	RF bandpass	3.5-5.7 GHz
Lu <i>et al.</i> [28]	2005	0.18 μ m	RF power divider	4.5 GHz
Liang <i>et al.</i> [50]	2005	0.18 μ m	RF bandpass	3.45-3.6 GHz
Gao <i>et al.</i> [51-53]	2005	0.25 μ m	RF bandpass	2.05-2.45 GHz
Chen <i>et al.</i> [54, 55]	2005	0.35 μ m	Limiting amp.	2.3 GHz
Lu & Liao [20]	2005	0.18 μ m	RF Phase shifter	360 degrees
Mahmoudi & Salama [56]	2005	0.18 μ m	QVCO	8 GHz
Jiang & Yuan [57]	2005	0.18 μ m	Gb/s Tx.	10 Gbps
Yuan [58, 59]	2006	0.18 μ m	Ring VCO	1.7-2.7 GHz
Lu <i>et al.</i> [60]	2006	0.18 μ m	LC VCO	0.5-3.0 GHz
Xiao & Schaumann [61]	2007	0.18 μ m	RF bandpass	3.34-5.72 GHz
Weng & Kuo [62]	2007	0.18 μ m	RF bandpass	2-2.9 GHz
Tang <i>et al.</i> [63]	2007	0.18 μ m	RF modulators	1.6 GHz
Tang <i>et al.</i> [64]	2007	0.18 μ m	VCOs	1.6 GHz

1. For bandpass filters, the frequency range is the passband center frequency range.

2. For VCOs, the frequency range is the oscillation frequency range.

3. For limiting amplifiers, the frequency is the bandwidth of the amplifiers.

The applications of active inductors, however, are affected by several difficulties arising from the intrinsic characteristics of MOS devices. These difficulties include a limited dynamic range, a high level of noise, and a high sensitivity to process spread, supply voltage fluctuation, and ground bouncing. It should be noted that these limitations are not unique to CMOS active inductors but rather common to all synthesized devices. Also, the effect of many of these difficulties can be reduced through innovative designs. For example, the limited dynamic range of active inductors can be expanded using class AB configurations where the voltage swing of active inductors can be made nearly rail-to-rail [65]. The effect of the high sensitivity to process spread can be minimized by making use of the tunability of both the inductance and quality factor of active inductors. The effect of supply voltage fluctuation and ground bouncing can be greatly reduced by using replica-biasing techniques and proper circuit configurations

[66]. The effect of the high level of the noise of active inductors on the phase noise of LC oscillators with active inductors can be minimized by boosting the quality factor of the active inductors [67].

New design techniques are yet critically needed to further improve the performance of active inductors and transformers. The emerging applications of CMOS active inductors continue to be unfolded along with the inception of new design techniques and circuit topologies of these active devices.

1.4 Chapter Summary

The critical need for inductive characteristics in high-speed applications, specifically, LC oscillators, bandwidth improvement of broadband amplifiers, narrow-band impedance matching, RF phase shifters, RF power dividers, RF frequency selection, and gain boosting of LNAs, has been investigated. An in-depth evaluation of the pros and cons of spiral inductors and transformers has been given. We have shown that spiral inductors and transformers suffer from a low quality factor, a low self-resonant frequency, a low and fixed inductance, and the need for a large silicon area.

We have shown that CMOS active inductors that are synthesized using MOS transistors offer a number of attractive characteristics as compared with their spiral counterparts. These characteristics include a low silicon consumption, a large and tunable self-resonant frequency, a large and tunable inductance, a large and tunable quality factor, and fully realizable in digital CMOS technologies. The applications of active inductors, however, are affected by several stiff difficulties arising from the intrinsic characteristics of MOS devices including a limited dynamic range, a high level of noise, and a high sensitivity to process spread, supply voltage fluctuation, and ground bouncing.

Chapter 6

OSCILLATORS WITH ACTIVE INDUCTORS & TRANSFORMERS

This chapter deals with the design of ring and LC tank oscillators using active inductors and transformers investigated in Chapters 2 and 3. The fundamentals of oscillators including voltage or current-controlled oscillators are available in numerous texts, such as [17, 68] and will therefore not be repeated here. Instead, our focus will be given to the circuit implementation of voltage / current-controlled oscillators employing active inductors and transformers for performance enhancement and cost reduction.

The chapter is organized as the followings : Section 6.1 briefly examines the operation of ring oscillators and LC oscillators. The phase noise of oscillators is investigated in detail. Ring oscillators with active inductors are investigated in Section 6.2. Ring oscillators studied in this section include source-coupled ring oscillators, cross-coupled ring oscillators, and Park-Kim ring oscillators. Section 6.3 deals with the design of LC oscillators with active inductors. The use of active transformers in LC oscillators is dealt with in Section 6.4. The design of quadrature LC oscillators using active inductors and transformers is studied in Sections 6.5 and 6.6, respectively. The chapter is concluded in Section 6.8.

6.1 Introduction

The oscillators that are used in data communications over wire channels are mainly ring oscillators due to the need for a large number of clock phases and a large frequency tuning range in these applications. The oscillators that are used in data communications over wireless channels are typically LC oscillators with spiral inductors or transformers, owing to the stringent phase noise requirements and the nature of the narrow-band operation of these systems. The former are usually constructed using a set of voltage-controlled delay cells that are

interconnected in a ring format whereas the latter are constructed using cross-coupled amplifiers with LC tank loads.

Oscillators are feedback systems with a positive feedback. The oscillation is initiated by either the noise or disturbances that are either generated internally or coupled externally. Because the amplitude of these noise or disturbances is very small, oscillators can be treated as linear systems at the start of the oscillation where the voltage swing of the oscillators is small. The closed-loop transfer function of the oscillators in this case is given by

$$H_c(j\omega) = \frac{H(j\omega)F(j\omega)}{1 + H(j\omega)F(j\omega)}, \quad (6.1)$$

where $H(j\omega)$, $F(j\omega)$, and $H_c(j\omega)$ are the transfer functions of the forward path, the feedback path, and the closed-loop, respectively. $H_o(j\omega) = H(j\omega)F(j\omega)$ is called the loop gain. Under the condition $H(j\omega)F(j\omega) = -1$, known as Barkhausen criteria, or equivalently

$$\begin{cases} |H(j\omega)F(j\omega)| = 1, \\ \angle H(j\omega)F(j\omega) = -180 \text{ degrees}, \end{cases} \quad (6.2)$$

the system has an infinite gain (oscillation). Although the noise or disturbances generated internally or coupled externally will be amplified with an infinitely large voltage gain theoretically, the finite voltage gain of practical VCOs and the amplitude-limiting mechanism existing in the oscillators ensure that only a finite voltage will appear at the output of the oscillators.

6.1.1 LC Oscillators

An oscillator must have a sufficiently large voltage gain in order to satisfy Barkhausen criteria and start an oscillation in a short period of time. For the LC oscillator shown in Fig.6.1, the voltage gain of a delay stage is given by $A_v \approx -g_m Z$, where Z is the impedance of the LC tank. A large voltage gain exists at the self-resonant frequency of the LC tank. This is because for an ideal LC tank, the impedance of the tank at the resonant frequency ω_o is infinite, i.e. $Z(j\omega_o) = \infty$, where $\omega_o = \frac{1}{\sqrt{LC}}$ is the resonant frequency of the LC tank, L and C are the inductance and capacitance of the tank, respectively. For a lossy LC tank, $Z(j\omega_o) = R_p$, where R_p is the shunt resistance of the tank. When neglecting the capacitances of the transistor, the voltage gain of the common-source amplification stage with a lossy LC tank load at the resonant frequency of the LC tank is given by $A_v \approx -g_m R_p$. Although a phase delay of -180 degrees exists ideally, the phase shift is smaller than -180 degrees for

practical circuits due to the capacitances of the transistors. Two back-to-back connected common-source amplifiers with LC-tank loads will thus be required to provide a sufficiently large phase shift in order to satisfy Barkhausen criteria.

If the tank is lossy, in order to start an oscillation and sustain the oscillation, a negative resistor connected in parallel with the LC tanks is required to cancel out the resistance of the tanks so that the tanks are lossless. The added negative resistor has two distinct functions : (i) The amplification stages of the LC oscillator have sufficiently large voltage gains to start an oscillation. (ii) The loss of the oscillator is sufficiently small so that an oscillation of a constant amplitude can be sustained.

A widely used differential negative resistor is the cross-coupled transistor pair consisting of $M_{1,2}$ and the tail biasing current source J , as shown in Fig.6.1. A tail biasing current source in this case is needed to provide dc biasing currents for $M_{1,2}$ and to tune the resistance. The resistance of the negative resistor can be tuned by varying the dc biasing current. The resistance of the negative resistor must be at least equal to the resistance of the LC tanks so that the ohmic loss of the tanks can be eliminated completely. For practical circuits, a rule-of-thumb is to set the resistance of the negative resistor three times the resistance of the LC tanks so that the effect of process variation, supply voltage fluctuation, and temperature drift of practical LC oscillators can be accounted for adequately [60, 39].

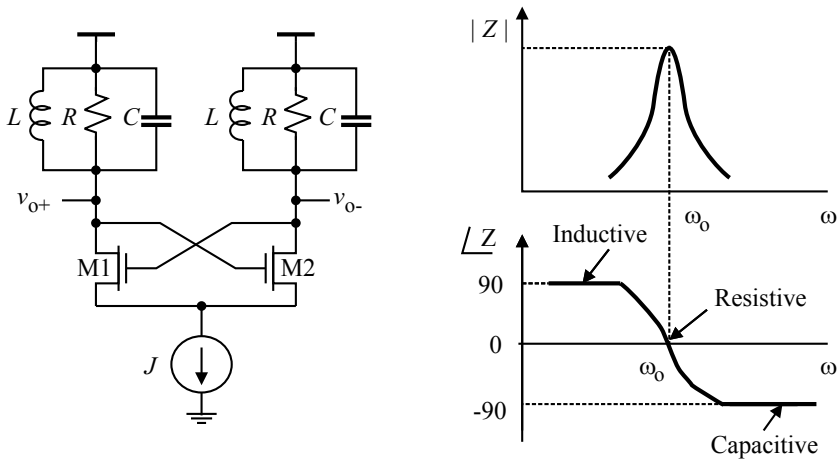


Figure 6.1. Resonance of RLC networks and LC oscillators.

6.1.2 Ring Oscillators

For ring oscillators, such as a static inverter oscillator, a large voltage gain exists when the input of each static inverter stage of the oscillator falls into the

transition region of the voltage transfer characteristic curve of the inverter, i.e. $V_{IL} \leq v_{in} \leq V_{IH}$, as shown in Fig.6.2. The voltage gain in this region is given by

$$A_v \approx - (g_{m,n} + g_{m,p})(r_{o,n} || r_{o,p}), \quad (6.3)$$

where $g_{m,n}$ and $g_{m,p}$ are the transconductances of nMOS and pMOS transistors, respectively, and $r_{o,n}$ and $r_{o,p}$ are the output resistances of nMOS and pMOS transistors, respectively. When the input voltage falls outside the transition region, two cases exist :

- Case 1 - When v_{in} is high, the nMOS transistor is in the saturation and the pMOS transistor is OFF. The voltage gain of the inverter stage drops to $A_v \approx - g_{m,n} r_{o,n}$. To ensure that the nMOS transistor is in the saturation, $v_{DS,n} \geq v_{GS,n} - V_T$ is required. This is equivalent to $v_{in} \leq v_o + V_T$. Clearly, if v_{in} is high enough, the nMOS transistor will be pushed into the triode region. In this case, not only the output resistance of the delay stage will drop from $r_{o,n}$ to $r_{ds,n}$, where $r_{o,n}$ to $r_{ds,n}$ are the channel resistance of the nMOS when the device is in the saturation region and the triode region, respectively, the transconductance of the nMOS transistor will also drop significantly, diminishing the voltage gain.
- Case 2 - When v_{in} is low, the pMOS transistor is in the saturation and the nMOS transistor is OFF. The voltage gain drops to $A_v \approx - g_{m,p} r_{o,p}$. To ensure that the pMOS transistor is in the saturation, $v_{SD,p} \geq v_{SG,p} - V_T$ is required. This is equivalent to $v_{in} \geq v_o + V_T$. If v_{in} is low enough, the pMOS transistor will be pushed into the triode region. Both the output resistance of the delay stage and the transconductance of the pMOS transistor will drop significantly and the voltage gain of the stage will vanish.

Because oscillators are positive feedback systems, an automatic amplitude attenuation and expansion mechanism must be present such that a sustained oscillation with a constant amplitude can be obtained. For the static inverter ring oscillator shown in Fig.6.2, the voltage gain of each inverter stage of the oscillator is very large if the input voltage (noise or disturbances) is small and falls into the transition region of the inverter. The voltage gain of the inverter stages drops drastically when the input voltage of the stages increases and falls outside the transition region. It is this gain drop that limits the amplitude of the output voltages of the inverter stages, giving rise to the peak-to-peak oscillation of the oscillator.

For the LC oscillator shown in Fig.6.1, the voltage gain of the common-source amplifier stages with the LC tank load is limited by the loss of the tank load and the finite transconductance of the transistor. The latter is determined

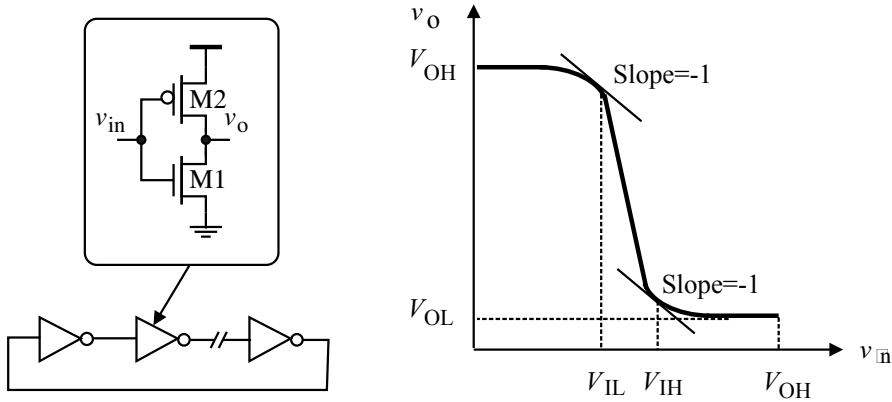


Figure 6.2. Ring oscillators with static inverter delay stages.

by the width of the transistor and its dc biasing current, which is upper-bounded by the tail current of the oscillator. Also, the voltage gain drops drastically when the frequency drifts away from the resonant frequency of the LC tank. Barkhausen criteria are only satisfied at the resonant frequency of the LC tank. This ensures that the oscillation frequency of the LC oscillator will only be the resonant frequency of the LC tank.

The oscillation frequency of a ring oscillator is determined by the number of the delay stages of the oscillator and the average propagation delay of the delay stages of the oscillator.

6.1.3 Phase Noise of Oscillators

The phase noise of oscillators have been studied extensively and various mathematical models of the phase noise of oscillators have been proposed. Perhaps the most widely cited early work on the phase noise of oscillators is the empirical expression by Leeson [139]. It predicts the power of the single-side-band (SSB) phase noise of a LC tank oscillator

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_s}\left[1 + \left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right]\left(1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right)\right\}, \quad (6.4)$$

where $\Delta\omega$ is the frequency offset from the oscillation frequency ω_o , Q is the quality factor of the oscillator, F is the excess noise factor, k is Boltzmann constant, T is absolute temperature in degrees Kelvin, P_s is the average power loss of the oscillator, and $\Delta\omega_{1/f^3}$ is the corner frequency between $1/f^2$ and $1/f^3$ regions. As shown in Fig.6.3, $1/f$ -noise is up-converted to the vicinity of the oscillation frequency. This region is identified as the $1/f^3$ -region and

affects the phase noise of the oscillators the most. The $1/f^2$ -region of the phase noise spectrum is due to the white noise sources of the oscillators whereas the flat region is due to the white noise sources of the output buffers.

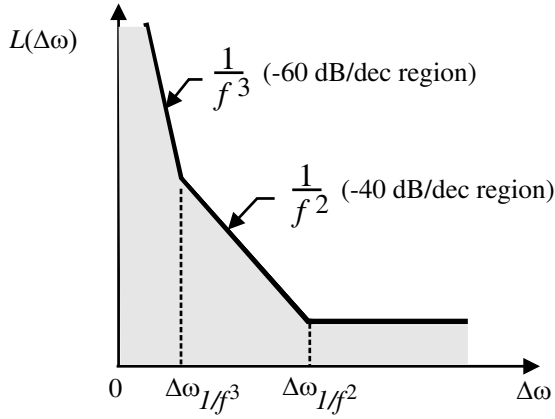


Figure 6.3. Phase noise spectrum of oscillators.

Weigandt *et al.* showed that an error voltage of an oscillator's output at the nominal time of threshold crossings shifts the actual threshold crossing time by an amount that is proportional to the voltage error and inversely proportional to the slew rate of the output of the oscillator, as shown in Fig.6.4 [140, 141].

$$\overline{\Delta\tau^2} = \frac{\overline{v_n^2}}{(dv/dt)^2}, \quad (6.5)$$

where $\overline{\Delta\tau^2}$ is the timing jitter, $\overline{v_n^2}$ is the power of the noise injected at the threshold-crossing, and dv/dt is the slew rate of the output voltage of the oscillator at the threshold-crossing point.

Razavi showed in [69] that the closed-loop transfer function of oscillators at the frequency that is offset from the oscillation frequency ω_o by $\Delta\omega$ with $\Delta\omega \ll \omega$ is given by

$$\begin{aligned} |H_c(\omega_o + \Delta\omega)|^2 &\approx \frac{1}{(\Delta\omega)^2 \left| \frac{dH_o(j\omega)}{d\omega} \right|_{\omega=\omega_o}^2}, \\ &= \frac{1}{(\Delta\omega)^2 \sqrt{\left[\frac{dA(j\omega)}{d\omega} \right]_{\omega_o}^2 + \left[\frac{d\phi(j\omega)}{d\omega} \right]_{\omega_o}^2}}, \end{aligned} \quad (6.6)$$

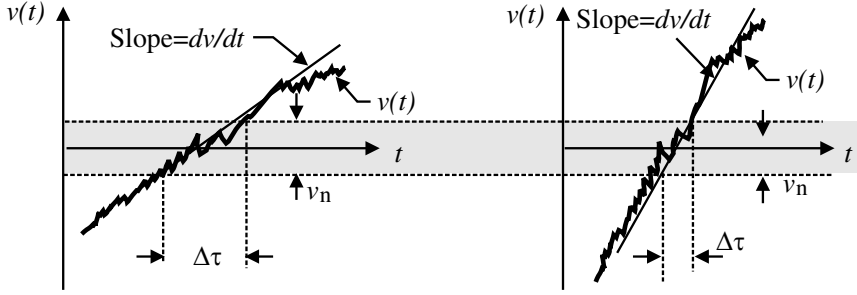


Figure 6.4. Weigandt model of phase noise of oscillators.

where $A(\omega)$ and $\phi(\omega)$ are the magnitude and phase of $H_o(j\omega)$, respectively. By defining the quality factor of the oscillators

$$Q(\omega_o) = \frac{\omega_o}{2} \sqrt{\left[\frac{dA(\omega)}{d\omega} \right]_{\omega_o}^2 + \left[\frac{d\phi(\omega)}{d\omega} \right]_{\omega_o}^2}, \quad (6.7)$$

we arrive at

$$|H_c(\omega_o + \Delta\omega)|^2 \approx \frac{1}{4Q^2(\omega_o)} \left(\frac{\omega_o}{\Delta\omega} \right)^2. \quad (6.8)$$

Eq.(6.8) reveals that to minimize the phase noise of oscillators, the quality factor of the oscillators should be maximized.

For saturated ring oscillators, Q is much smaller as compared with that of LC oscillators. This is because at the threshold-crossing of the output voltage of saturated ring oscillators, such as inverter ring oscillators, both the nMOS and pMOS transistors of the inverter stage are in the saturation, exhibiting a large resistance $r_o = r_{o,n} || r_{o,p}$. Further, there does not exist a Q-enhancement mechanism similar to that in LC oscillators to eliminate the effect of this large resistance. As a result, ring oscillators exhibit a high level of phase noise.

For LC oscillators, because

$$\left. \frac{dA}{d\omega} \right|_{\omega_o} = 0, \quad (6.9)$$

Eq.(6.7) is simplified to

$$Q(\omega_o) = \frac{\omega_o}{2} \left| \frac{d\phi}{d\omega} \right|_{\omega_o}. \quad (6.10)$$

Eq.(6.10) reveals that the quality factor of LC oscillators can be maximized by maximizing the sensitivity of the phase $\phi(\omega)$ with respect to frequency at ω_b .

Because the voltage swing of saturated ring VCOs is usually rail-to-rail and the systems are highly nonlinear, the linearization approach can not characterize the phase noise of saturated ring oscillators accurately. Also, it fails to take into account of the periodically time-varying characteristics of oscillators. As a result, the effect of frequency conversion, especially the up-version of 1/f noise arising from the periodically time-varying characteristics of oscillators, can not be counted for.

Hajimiri and Lee introduced an impulse sensitivity function $\Gamma(\omega_b\tau)$ to quantify the impulse response of oscillators [142]

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_o\tau)}{q_{max}} u(t - \tau), \quad (6.11)$$

where q_{max} is the maximum charge displacement at the node where the impulse response $h_\phi(t, \tau)$ is measured, $u(t - \tau)$ is the unit step function specifying the time instant at which the noise is injected, τ and t are the noise launch time and response observation time, respectively. Impulse sensitivity function reaches its minima at the peak of the output voltage of the oscillator and its maxima at the threshold-crossing of the output voltage of the oscillator. The periodical operation of oscillators ensures that the impulse sensitivity function is periodic in the observation time t with its period equal to the period of the oscillators. Representing the impulse sensitivity function in its Fourier series expansion

$$\Gamma(\omega_o\tau) = \frac{c_0}{2} + \sum_{m=1}^{\infty} c_m \cos(m\omega_o\tau), \quad (6.12)$$

we arrive at the phase noise induced by a noise current $i_n(t)$

$$\begin{aligned} \phi(t) &= \int_{-\infty}^{\infty} h_\phi(t, \tau) i_n(\tau) d\tau \\ &= \frac{1}{q_{max}} \int_{-\infty}^t \Gamma(\omega_o\tau) i_n(\tau) d\tau \\ &= \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^t i_n(\tau) d\tau + \sum_{m=1}^{\infty} c_m \int_{-\infty}^t \cos(m\omega_o\tau) i_n(\tau) d\tau \right]. \end{aligned} \quad (6.13)$$

Eq.(6.13) provides a theoretical foundation for analysis of the up-conversion of low-frequency noise.

For a white noise source with its PSD given by

$$S(\omega) = \frac{\overline{i_n^2}}{\Delta f}, \quad (6.14)$$

the SSB computed from (6.13) is given by

$$L(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \frac{\overline{i_n^2}/\Delta f}{2(\Delta\omega)^2}. \quad (6.15)$$

For a $1/f$ noise source with its PSD given by

$$S(\omega) = \overline{i_{n,1/f}^2} = \overline{i_n^2} \frac{\omega_{1/f}}{\Delta\omega}, \quad (6.16)$$

where $\omega_{1/f}$ is the corner frequency of the $1/f$ noise, the SSB is given by

$$L(\Delta\omega) = \frac{c_0^2}{q_{max}^2} \frac{\overline{i_n^2}/\Delta f}{4(\Delta\omega)^3} \omega_{1/f}. \quad (6.17)$$

6.2 Ring Oscillators With Active Inductors

Voltage-controlled ring oscillators offer many attractive advantages over their LC counterparts including full compatibility with standard CMOS processes, a large frequency tuning range, a large number of complementary phases, a low level of power consumption, and a low silicon consumption. The stringent timing jitter constraint of high-speed data communications require that these ring oscillators be configured in a fully differential way such that the common-mode noise generated internally by the oscillators or coupled externally to the oscillators is suppressed effectively.

Eq.(6.5) reveals that an increase in the slew-rate at the threshold-crossing of the output voltage of VCOs will lower the timing jitter, as depicted graphically in Fig.6.4. The output voltage of ring VCOs should therefore be designed to have fast rising and falling edges such that the transition window during which circuit noise contributes the most to the timing jitter of the oscillators is minimized.

It is well understood that the slope of the rising and falling edges of the output voltage of a conventional ring VCO is set by the RC time constant of the output node of the VCO. Although this RC time constant can be reduced by varying the width of the transistors of the delay cell of the VCO, the improvement is rather moderate. This is because an increase in the width of the transistors of the delay cell of the VCO, though lowering R , increases C at the same time as well. As a result, the net reduction in the time constant of the output node of the delay stage of the VCO is rather marginal.

This section looks into the use of active inductors in design of ring oscillators to improve the slope of the output voltage of the oscillators at threshold crossings.

6.2.1 Source-Coupled Ring VCOs

The schematic of the delay cell of source-coupled differential ring VCOs is shown in Fig.6.5. Common-mode disturbances either generated internally or coupled externally, such as supply voltage fluctuations, are suppressed effectively by the differential configuration of the delay cell. The effect of ground bouncing is also minimized as the delay cell is isolated from the ground rail by the biasing tail current source. The impedance of the active loads is voltage-dependent and varies with the swing of the output voltage v_o . When v_o is low, the load transistors are in the saturation and behave as current sources, exhibiting a large impedance. When v_o is high, the load transistors enter the triode region and behave as resistors, exhibiting a low impedance. The time delay of the delay cell can be varied in three different ways :

- Bias the active load transistors $M_{3,4}$ in the triode region by keeping V_{c2} low and control their resistance by varying the gate voltage V_{c2} . Because $M_{3,4}$ behaves as voltage-controlled resistors only when they are in the triode, the swing of the output voltage of the delay cell must be kept small. This can be achieved by keeping the number of the delay stages small such that $v_{SD3,4} < V_{sat}$. A key advantage of this approach is that the total current drawn by the delay cell from the power supply is constant and is set by the tail current source. As a result, the switching noise generated by the delay cell is minimized.
- Bias the active load transistors $M_{3,4}$ in the saturation and control their channel currents by varying the gate voltage V_{c2} . Similar to the case in which $M_{3,4}$ are in the triode, the total current drawn by the delay cell is constant and is set by the tail current source. The switching noise generated by the delay cell is minimized. It should be noted that the preceding two approaches are often used without a clear boundary as the mode of the operation of $M_{3,4}$ is dependent of both the biasing voltage V_{c2} and the output voltage. Also, the preceding two methods vary the propagation delay of the delay cell by only changing the charge time of the output nodes. The discharge time is fixed.
- Vary the gate voltage V_{c1} of the tail transistor M_5 . Because $g_{m1,2}$ vary with V_{c1} in this case, the delay of the delay stage experiences a large variation, echoed with a large frequency tuning range. A downside of this approach is that when the VCO is used in a phase-locked loop with a bang-bang phase detector, the control voltage fluctuates in the vicinity of its nominal value.

The total current of the delay cell injected into the ground rail and drawn from the supply voltage is no longer constant. As a result, the switching noise generated by the delay cell increases. Note that the propagation delay of the delay cell is varied by changing the discharge time in this case.

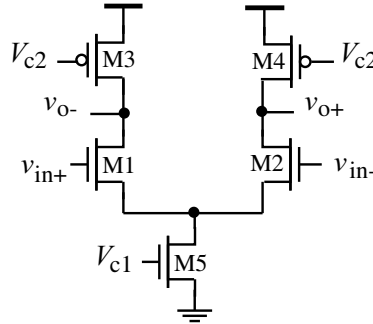


Figure 6.5. Schematic of source-coupled ring VCO delay cell with active loads.

The delay of the preceding source-coupled delay cell is set by the RC time constant of the output nodes. To further reduce the delay, active inductors can be used to replace the active loads of the delay cell, as shown in Fig.6.6 where Hara active inductors are used as the loads of the delay cell [41, 40]. The time constant of the output nodes of the delay cell is now determined by the RLC networks at the output nodes. In addition to the time constant reduction obtained from the inductive peaking, the added Hara active inductors further improve the performance of the delay cell in the following aspects :

- Although Hara active inductors employ two transistors with the pMOS transistor biased in the triode and behaving as a voltage-controlled resistor, only the nMOS transistor of the active inductors is connected to the output nodes of the delay cell. As a result, the output capacitance of the delay cell is approximately the same as that of the delay cell with the active loads.
- The low impedance looking into Hara active inductors given by $\frac{1}{g_{m5,6}}$ lowers the time constant of the output nodes of the delay cell from $\tau_o \approx C_o (r_{o1,2} || r_{o3,4})$ without the active inductors to $\tau_o \approx \frac{C_o}{g_{m5,6}}$ with the active inductors, where C_o is the capacitance encountered at the output node. A nMOS-latch formed by $M_{7,8}$ and shown in Fig.6.6 can also be employed to further improve the performance of the delay cell [81].

The frequency tuning of source-coupled ring VCOs with Hara active inductor loads can be carried out in two ways :

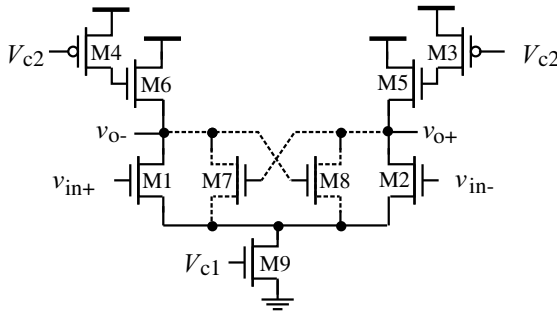


Figure 6.6. Schematic of source-coupled ring VCO delay with Hara active inductor loads.

- Approach 1 - Vary the gate voltage of $M_{3,4}$. Because $M_{3,4}$ are in the triode and behave as voltage-controlled resistors, a change of V_{c2} will change the resistance of the resistor of Hara active inductors. It was shown in Chapter 2 that the inductance of Hara active inductors can be tuned by varying its resistor R with a small inductance tuning range. The small inductance tuning range of Hara active inductors results in a small frequency tuning range of the VCOs obtained from varying R , as demonstrated in [143].
- Approach 2 - Vary the gate voltage of the tail biasing transistor M_9 . A large frequency tuning range can be obtained in this way. As pointed out earlier that a downside of this approach is that the total current by the delay cell injected to the ground rail and drawn from the power supply is no longer constant. This is echoed with an increase in the switching noise generated by the delay cell.

The delay cell with Hara active inductor loads suffers from a voltage swing loss of at least V_T because when v_o exceeds $V_{DD} - V_T$, the nMOS transistor of Hara active inductors switches off, disabling the active inductors. This drawback can be eliminated by adding a pull-up pMOS latch, as shown in Fig.6.7. The added pMOS latch will continue to charge the output nodes even when Hara active inductors switch off.

6.2.2 Cross-Coupled Ring VCOs

A main drawback of the preceding source-coupled delay cells is the need for a biasing tail current source. As pointed out in [142] that the flicker noise of the tail current source of the delay stage of a ring oscillator will be up-converted to the vicinity of the oscillation frequency of the ring oscillator, deteriorating the phase noise of the oscillator. Also, the output voltage swing of the oscillator is limited by the voltage drop across the tail current source.

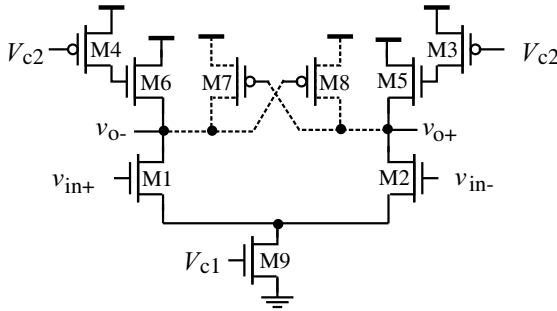


Figure 6.7. Schematic of source-coupled ring VCO delay with Hara active inductor loads and a pull-up pMOS latch.

The cross-coupled delay cell shown in Fig.6.8 removes the need for a tail biasing current source [144, 145]. It operates in a full rail-to-rail swing mode. A nMOS-latch is often employed to speed up the transition of the output voltages, reducing the transient duration in which device and supply voltage noise contributes the most to the timing jitter of the oscillators. The latch also ensures that the output voltage is less sensitive to both supply voltage variation and ground bouncing once the latch is established.

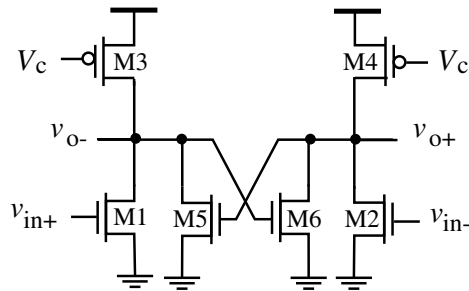


Figure 6.8. Cross-coupled ring VCO delay cell with active loads and a pull-down nMOS latch.

$M_{3,4}$ can be either in the triode or in the saturation, depending upon V_c . Also, their region of operation is dependent of the output voltage swing of the delay cell. Frequency tuning is achieved by varying V_c that controls $r_{ds3,4}$ when $M_{3,4}$ are in the triode or $i_{DS3,4}$ when $M_{3,4}$ are in the saturation. A drawback of cross-coupled ring VCOs is waveform asymmetry. As shown in Fig.6.9, the rise time of the cross-coupled VCOs varies with the control voltage while the fall time remains unchanged. As a result, the duty cycle of the waveform varies with the control voltage. Another drawback is the timing-varying current injected into the ground rail, increasing the level of switching noise.

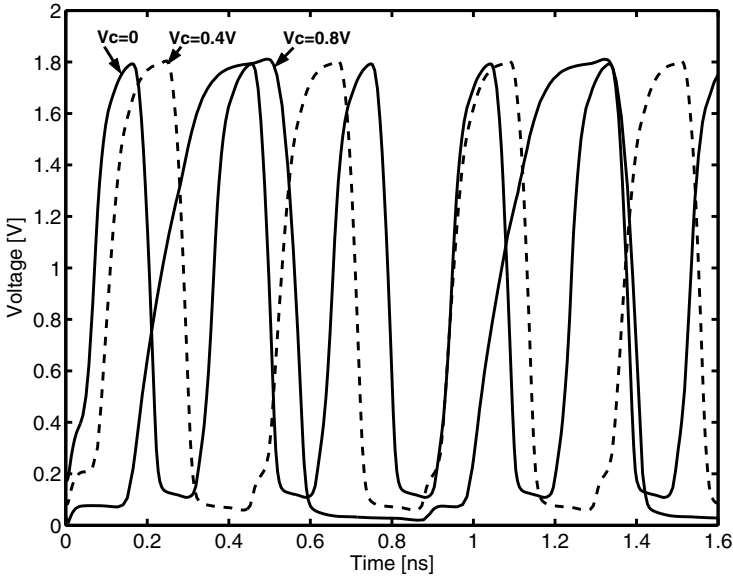


Figure 6.9. Simulated output voltage of a 4-stage cross-coupled ring VCO with active loads and a nMOS pull-down latch.

To reduce the time delay of the cross-coupled delay cells, the active loads can be replaced with Hara active inductor loads, as shown in Fig.6.10 [81]. The added active inductors form RLC networks at the output nodes of the delay cell. Inductor shunt peaking lowers the time for charging and discharging the output nodes. The tuning of the oscillation frequency is achieved by varying the value of the resistor of Hara active inductors via adjusting V_c . This delay cell, however, suffers from two main drawbacks : (i) The frequency tuning range is small as the resistance of the resistor of Hara active inductors has a marginal effect on the inductance of the active inductors. (ii) The voltage headroom loss of at least V_T at the output nodes of the delay cell because v_o is upper-bounded by $V_{DD} - V_T$.

The preceding voltage headroom loss can be eliminated by connecting a pull-up pMOS latch in parallel with the active inductor load, as shown in Fig.6.11 [59]. The pull-up pMOS latch takes over the charging process of the output node when the output voltage exceeds $V_{DD} - V_T$ at which the nMOS transistor of Hara active inductors enters its cut-off mode. Because no change is made to the frequency tuning mechanism, the drawback of the small frequency tuning range remains.

Fig.6.12 and Fig.6.13 compare the waveform of the output voltage of two 4-stage cross-coupled ring VCOs, one with resistor loads and the other with

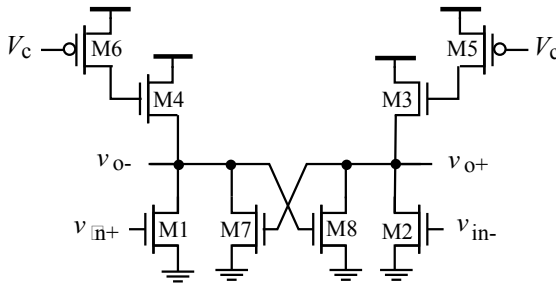
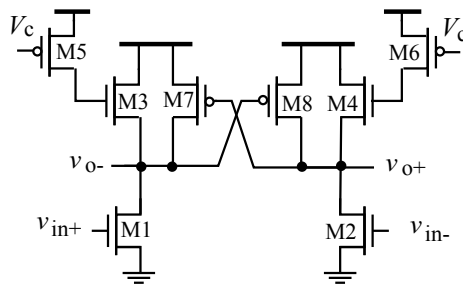


Figure 6.10. Schematic of cross-coupled ring VCO delay cell with Hara active inductor loads and a pull-down nMOS latch.



(c)

Figure 6.11. Schematic of cross-coupled ring VCO delay cell with Hara active inductor loads and a pull-up pMOS latch.

Hara active inductor loads. The corresponding transistors of two ring VCOs were chosen to have the same dimension so that a fair comparison was obtained. Both VCOs were implemented in TSMC-0.18 μ m 1.8V CMOS technology and analyzed using SpectreRF with BSIM3V3 device models. It is seen that the oscillation frequency of the VCO with Hara active inductor loads is approximately twice that of the VCO with the resistor loads. The loss of the swing of the output voltage of the VCO with Hara active inductor loads is also evident. Fig.6.14 plots the output voltage of a 4-stage cross-coupled ring VCO with Hara active inductor loads and the pull-up pMOS-latch. It is observed that the swing of the output voltage of the VCO is rail-to-rail. Also, the added pMOS-latch improves the slew rate of the output voltage, reflected by the increased time duration of the Logic-0 and Logic-1 stages of the output voltage.

6.2.3 Park-Kim Ring VCOs

The delay cell proposed by Park and Kim in [146] and shown in Fig.6.15 controls the propagation delay of the delay cell by varying the intensity of

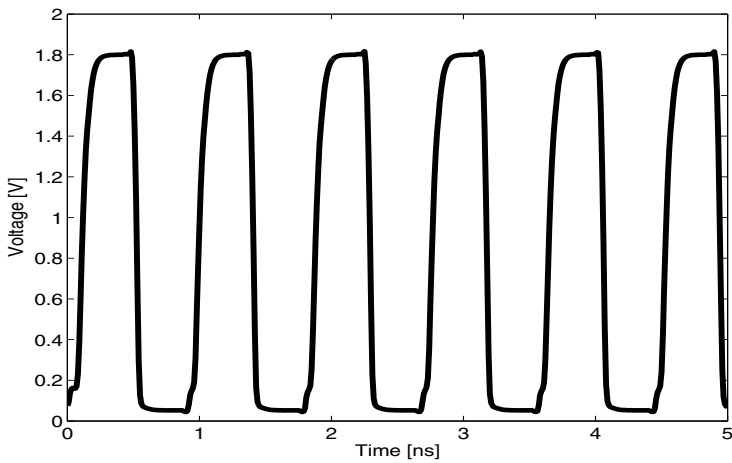


Figure 6.12. Simulated output voltage of a 4-stage cross-coupled ring VCO with resistor loads.

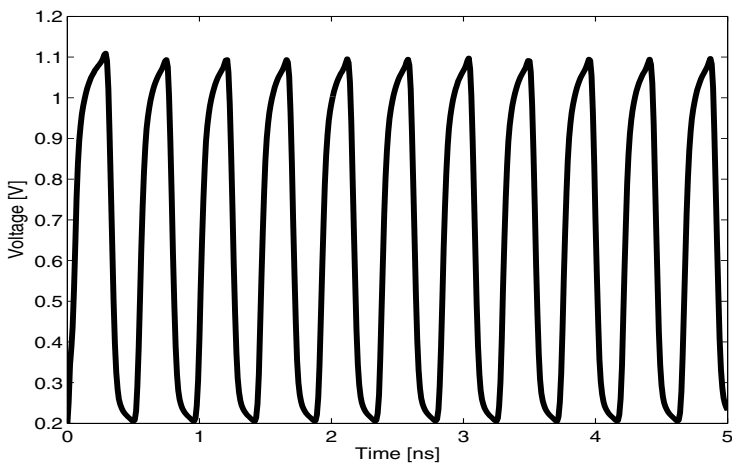


Figure 6.13. Simulated output voltage of a 4-stage cross-coupled ring VCO with Hara active inductor loads.

the latch. An advantage of doing so is that both the rise and fall times are controlled by V_c . As a result, an improved waveform symmetry over a large range of the control voltage is obtained, as evident in Fig.6.16. This is an important advantage of Park-Kim ring VCOs over the cross-coupled ring VCOs investigated earlier.

In [58], a pair of Hara active inductors were connected in parallel with the pull-up pMOS transistors of Park-Kim ring VCO delay cell to provide an

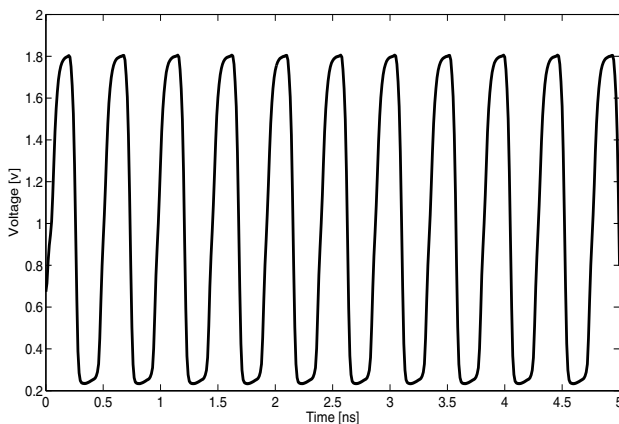


Figure 6.14. Simulated output voltage of a 4-stage cross-coupled ring VCO with Hara active inductor loads and a pull-up pMOS latch.

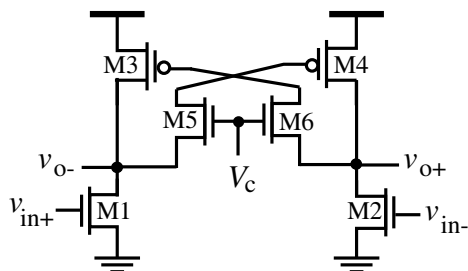


Figure 6.15. Schematic of single-loop Park-Kim ring VCO delay cell.

additional charge path to compensate for the slow turn-on of the pull-up pMOS transistors and to provide active inductors at the output nodes of the delay cell, as shown in Fig.6.17. The frequency tuning mechanism of the delay cell is the same as that of Park-Kim ring VCO delay cell so that the waveform symmetry property of Park-Kim ring VCO delay cell is preserved.

Figs.6.18 and 6.19 plot the simulated output voltage of two 8-stage Park-Kim ring VCOs, one with Hara active inductor loads and the other without. The VCOs were implemented in TSMC-0.18 μm 1.8V CMOS technology and analyzed using SpectreRF with BSIM3V3 device models. The size of corresponding transistors in the delay cells was made identical in order to obtain a fair comparison. The improvement in the oscillation frequency from employing Hara active inductors is evident. The oscillation frequency of the VCO with

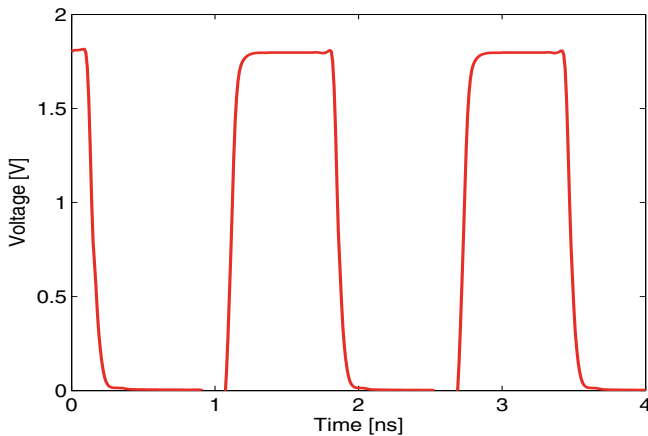


Figure 6.18. Simulated output voltage of a 8-stage single-loop Park-Kim ring VCO.

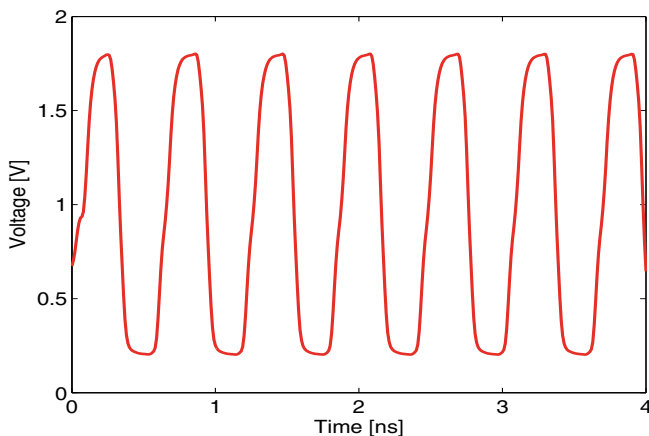
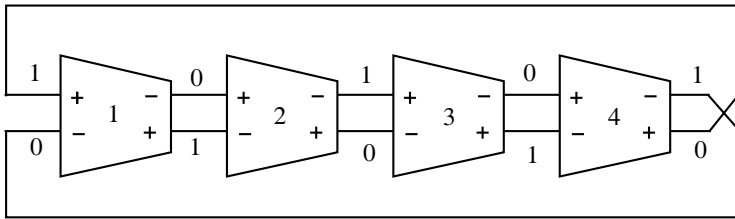


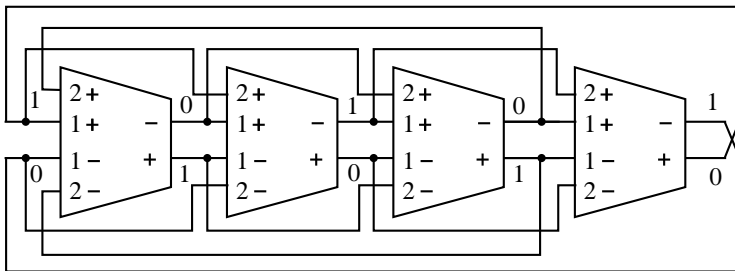
Figure 6.19. Simulated output voltage of a 8-stage single-loop Park-Kim ring VCO with Hara active inductor loads.

the delay stage so that the slow turn-on of the pMOS transistors of the delay cell can be compensated for effectively.

The delay of the dual-loop Park-Kim VCO delay cell can be further increased by replacing the pull-up transistors $M_{7,8}$ in Fig.6.21 with a pair of Hara active inductors, as shown in Fig.6.22. The dual-loop Park-Kim delay cell with Hara active inductor loads bears a strong resemblance to the dual-loop Park-Kim delay cell in the following aspects :



(a) Single-loop ring VCOs



(b) Dual-loop ring VCOs

Figure 6.20. Configuration of single-loop and dual-loop ring VCOs.

- Frequency tuning mechanism - Both delay cells adjust the time delay by varying the intensity of the latch. This not only enables the secondary inputs of the delay cells to be used to compensate for the slow turn-on of the pull-up pMOS load and ensures that the frequency tuning range of Park-Kim ring VCOs with Hara active inductor loads is comparable to that of corresponding Park-Kim ring VCOs, it also preserves the waveform symmetry property of Park-Kim ring VCOs.
- Output time constant - The output capacitance of the dual-loop Park-Kim delay cell with Hara active inductor loads is approximately the same as that of the dual-loop Park-Kim delay cell as the number of the transistors at the output node is the same.

The output resistance of the dual-loop Park-Kim delay cell with Hara active inductor loads given by $\frac{1}{g_{m7,8}}$, however, is smaller. As a result, a smaller time constant at the output nodes of the delay cell is obtained.

Fig.6.23 and Fig.6.24 compare the waveforms of the output voltage of two 8-stage dual-loop Park-Kim VCOs with and without Hara active inductor loads. The delay cells of both VCOs have the same transistor size and biasing condi-

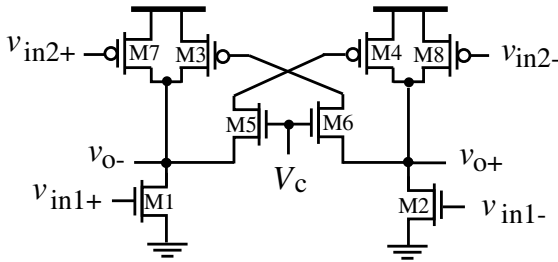


Figure 6.21. Schematic of dual-loop Park-Kim ring VCO delay cell.

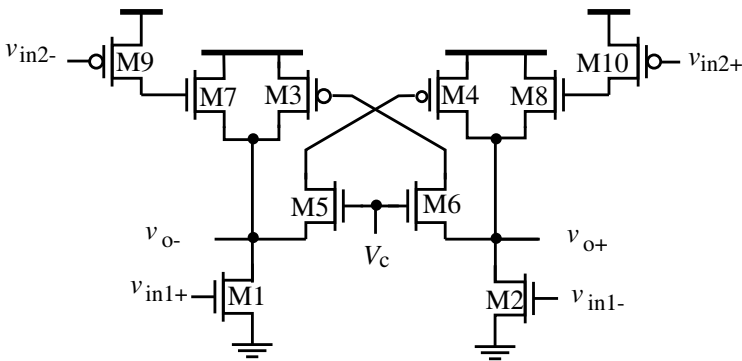


Figure 6.22. Schematic of dual-loop Park-Kim ring VCO delay cell with Hara active inductor loads.

tions. They were implemented in TSMC-0.18 μ m 1.8V CMOS technology and analyzed using SpectreRF with BSIM3V3 device models. The improvement in the oscillation frequency obtained from using Hara active inductor loads is evident.

6.3 LC Oscillators With Active Inductors

As compared with ring oscillators, LC oscillators with spiral inductors offer a key advantage of a low level of phase noise. They are widely used in wireless communications where a stringent constraint on phase noise exists. Two widely used configurations of LC oscillators with spiral inductors are shown in Figs.6.25 and 6.26 [148, 6]. Both are differentially configured in order to suppress common-mode disturbances effectively. The LC oscillator in Fig.6.26 employs two negative resistors implemented using a cross-coupled nMOS pair ($M_{1,2}$) and a cross-coupled pMOS pair ($M_{3,4}$) to compensate for the loss of the tanks. The oscillation amplitude of this oscillator is approximately twice that of the oscillator of Fig.6.25. In addition, it offers a lower phase noise

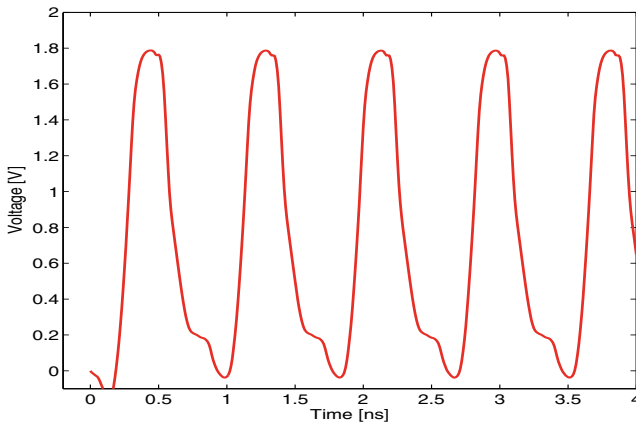


Figure 6.23. Simulated output voltage of a 8-stage dual-loop Park-Kim VCO.

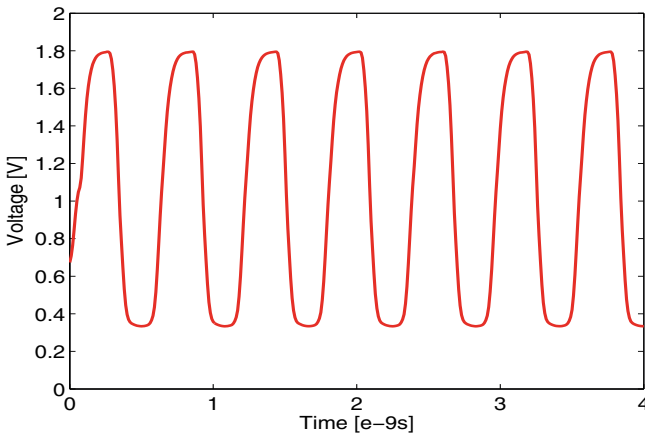


Figure 6.24. Simulated output voltage of a 8-stage dual-loop Park-Kim VCO with Hara active inductor loads.

as compared with the oscillator of Fig.6.25 [142]. Note that the total current drawn by the oscillator in Fig.6.25 is constant, minimizing the switching noise.

Frequency tuning of monolithic spiral LC oscillators is typically carried out by varying the capacitance of their LC tanks as the inductance tuning of spiral inductors in a monolithic integration is rather difficult. These variable capacitors are normally realized using MOS varactors. As a result, monolithic spiral LC oscillators have a small frequency tuning range, typically around

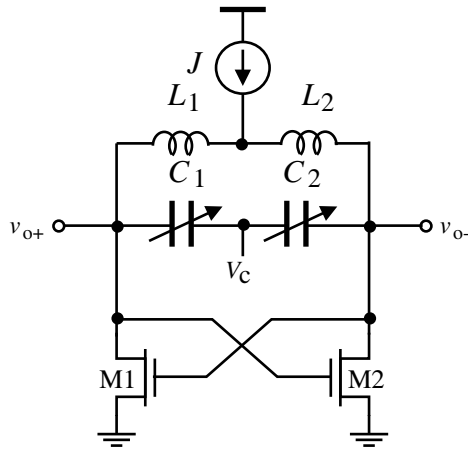


Figure 6.25. LC oscillators with a nMOS negative resistor.

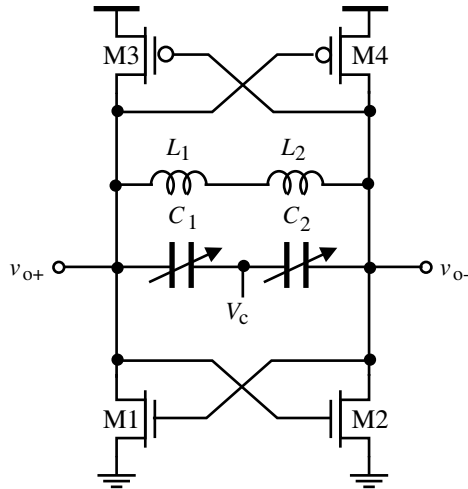


Figure 6.26. LC oscillators with complementary nMOS and pMOS negative resistors.

10%. The requirements for the frequency tuning range in narrow-band wireless applications are much relaxed as compared with those for clock and data recovery in broadband data communications over wire lines and optical channels, varactor-based tuning provides an adequate frequency tuning range. Spiral LC oscillators suffer from a number of drawbacks, in particular,

- Large silicon area - A notable disadvantage of LC oscillators with spiral inductors or transformers is the large silicon area required for the fabrication of the spiral inductors and transformers. Not only the inductance of

spiral inductors is low, the silicon area occupied by spiral inductors is also proportional to the inductance of the spiral inductors. Often, the silicon area of a RF front-end is primarily consumed by a few spiral inductors.

- Low self-resonant frequency - The self-resonant frequency of a spiral inductor is set by the inductance of the spiral and the parasitic capacitance between the spiral and the substrate. The large metal area of the spiral gives rise to a large spiral-substrate capacitance, which limits the self-resonant frequency of spiral inductors to a few GHz typically.
- Low quality factor - The ohmic losses of spirals at high frequencies, mainly due to the skin-effect induced resistance of the spirals and the substrate eddy-current induced resistance, limits the quality factor of spiral inductors to below 20 typically. Although the ohmic losses can be compensated for by employing negative resistors, the compensation result is generally poor over a large frequency range. This is because negative resistors are active networks while the parasitic resistance of spirals is a strong function of frequency.

Although active inductors offer several attractive advantages over their spiral counterparts including a large and tunable inductance, a low silicon consumption, and fully realizable in digital-oriented CMOS technologies. The applications of active inductor LC oscillators are confronted with two difficulties : a high level of phase noise and a limited dynamic range. An in-depth research in these areas and novel circuit topologies are critically needed in order to lower the phase noise and improve the dynamic range of these oscillators prior to a large scale deployment of active inductor oscillators in applications where passive inductors are dominating currently.

6.3.1 LC VCOs with Wu Current-Reuse Active Inductors

Fig.6.27 is the simplified schematic of a voltage-controlled LC oscillator employing Wu current-reuse active inductors investigated in Chapter 2. Transistors $M_{1,2,3a/b}$ form two Wu current reuse active inductors whose inductance is tuned by varying the dc biasing current J_1 . Transistors $M_{4a/b}$ and J_2 form a negative resistor whose resistance is given by $-\frac{2}{g_{m4}}$ approximately and is tunable by varying J_2 . This negative resistor is used to cancel out the parasitic resistances of the active inductors.

As demonstrated in [42], the silicon area of the VCO implemented in a $0.35\mu\text{m}$ 3V CMOS technology was only $100\mu\text{m} \times 120\mu\text{m}$. Frequency tuning range of the VCO was from 100 MHz to 900 MHz with phase noise of approximately -95 dBc/Hz at 500 kHz frequency offset. The high level of the phase noise is mainly due to the use of the active inductors and the tail current

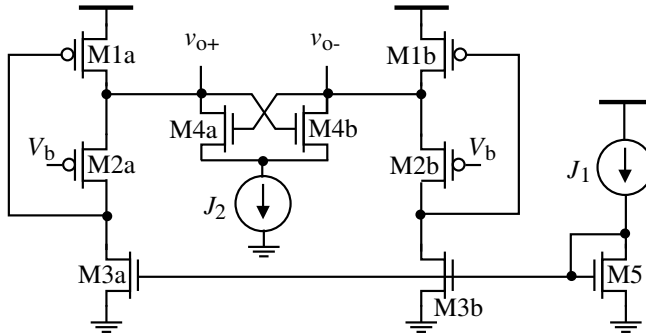


Figure 6.27. Simplified schematic of LC VCO with Wu current-reuse active inductors.

source of the negative resistor. Note that the phase noise can be improved by removing the tail current source of the negative resistor with the downside that the resistance of the negative resistor will not be variable.

6.3.2 LC VCOs with Lin-Payne Active Inductors

Lin-Payne active inductors investigated in Chapter 2 were used in design of LC oscillators. Fig.6.28 shows the simplified schematic of a LC oscillator with Lin-Payne active inductors. The pMOS transistor branches are used as inductance tuning branches subsequently frequency tuning branches while the nMOS transistor branches are connected to a negative resistor to cancel out the parasitic resistances of the active inductor. The resistance of the negative resistor is tuned by varying J_2 for a total compensation. This in turn adjusts the quality factor of the LC oscillator. The inductance of the active inductors is tuned by varying J_1 . The quality factor and oscillation frequency of the oscillator can thus be tuned independently.

It was demonstrated in [39] that in a $0.35\mu\text{m}$ implementation of a LC oscillator with Lin-Payne active inductors, the phase noise of the oscillator when $Q = 7$ was -83 dBc/Hz at 600 kHz frequency offset from a 1.5 GHz oscillation frequency. The power consumption of the oscillator was 2.5 mW . When $Q = 24$, the phase noise was reduced to -88 dBc/Hz at 600 kHz frequency offset from a 2.5 GHz oscillation frequency. The power consumption in this case was 4.5 mW . The frequency tuning range of the oscillator was 48% . The total active area of the oscillator excluding the biasing current sources was only $24\mu\text{m}^2$.

6.3.3 LC VCOs with Grözing Active Inductors

Grözing active inductors investigated in Chapter 2 are differentially configured such that they are less sensitive to common-mode disturbances. They

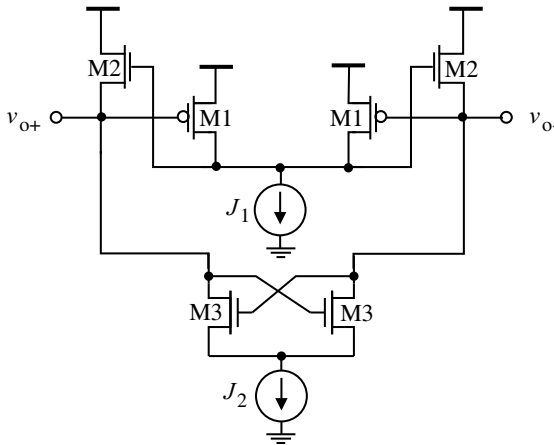


Figure 6.28. Simplified schematic of LC VCO with Lin-Payne active inductors.

were used in design of LC oscillators in [43, 44]. Fig.6.29 shows the simplified schematic of a LC oscillator with Grözing active inductors. The loads of the two differentially configured transconductors are controlled by V_{b1} . V_{b2} controls the tail biasing currents of the transconductors, which in turn tunes the transconductances of the transconductors, subsequently the inductance of the active inductor and the oscillation frequency of the oscillator. Two negative resistors implemented using the popular cross-coupled nMOS pair are employed at the output nodes of the transconductors to cancel out the parasitic output resistances of the transconductors subsequently the parasitic resistances of the active inductors. Note that the input impedances of the transconductors are infinity. So G_{o11} , G_{o12} , G_{o21} and G_{o22} , which contribute to the parasitic resistances of the active inductor, are solely due to the output resistances of the transconductors. The resistances of the two negative resistors are tuned individually by varying $J_{2,3}$ such that the output impedances of the two transconductors can be compensated for individually.

It was demonstrated in a $0.30\ \mu\text{m}$ 2.5 V implementation of a LC oscillator with Grözing active inductors, the self-resonant frequency of the active inductor was 5.6 GHz [43, 44]. The total power consumption of the oscillator was 15 mW. The quality factor was greater than 100 over the frequency range from 400 MHz to 4 GHz. The layout area of the oscillator was $200\ \mu\text{m} \times 200\ \mu\text{m}$.

6.3.4 LC VCOs with Karsilayan-Schaunann Active Inductors

Karsilayan-Schaunann active inductors investigated in Chapter 2 offer a large quality factor and the independent tunability of the inductance and quality

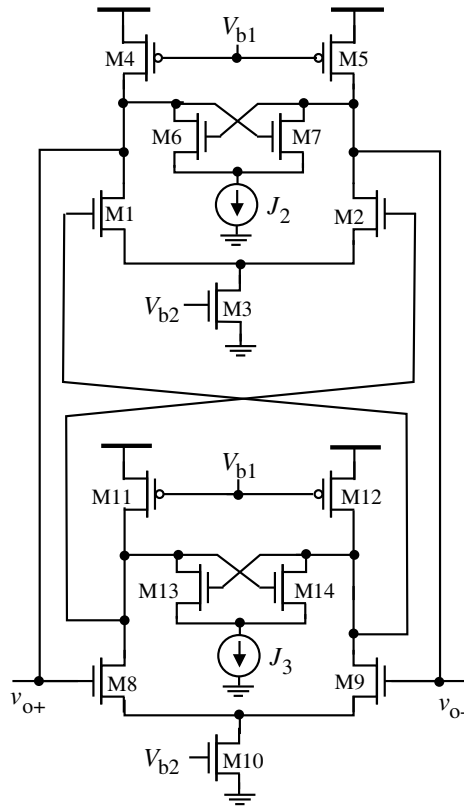


Figure 6.29. Simplified schematic of LC VCO with Grözing active inductors.

factor. LC oscillators that are based on Karsilayan-Schaunann active inductors were developed by Xiao and Schaunann in [75]. The simplified schematic of a LC oscillator employing Karsilayan-Schaunann active inductors is shown in Fig.6.30. Current sources J_1 – J_6 that provide dc biasing currents can be generated from a single master current source using current mirrors. J_7 is used to tune the resistance of the compensating negative resistor. As pointed out in Chapter 2 that the inductance of Karsilayan-Schaunann active inductors is tuned by varying C_I while its quality factor is adjusted by varying C_Q . These auxiliary capacitors can be implemented using MOS varactors.

It was demonstrated in a $0.20\ \mu\text{m}$ implementation of a LC oscillator with Karsilayan-Schaunann active inductors, the oscillation frequency of the oscillator was 4.95 GHz. The total power consumption was approximately 1.16 mW. The phase noise of the oscillator was -81 dBc/Hz at 500 kHz frequency offset. The total silicon consumption of the oscillator core was $24 \times 22\ \mu\text{m}^2$.

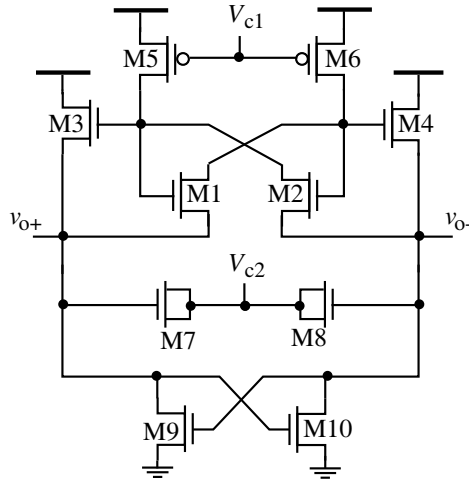


Figure 6.31. Simplified schematic of LC VCO with Lu floating active inductors.

6.4 LC VCOs With Active Transformers

Transformer LC oscillators are the newest members of the VCO family. As compared with spiral inductor LC VCOs, transformer LC VCOs use both the self and mutual inductances of a spiral transformer to form resonating LC tanks, as shown in Fig.6.32 [1]. Transformer LC oscillators offer the critical advantages of a reduced silicon area as compared with LC oscillators with two individual spiral inductors, an increased effective inductance $L_{eff} = L_{11} + kM_{12}$ where k is the coupling coefficient, L_{11} is the self-inductance of the primary winding and M_{12} is the mutual inductance from the secondary winding to the primary winding, and an improved quality factor.

The current of the primary winding I_1 of a lossless transformer generates a voltage drop at the secondary winding of the transformer $V_{21} = (R_{21} + j\omega M_{21})I_1$. Because the transformer does not transfer DC currents from the primary winding to the secondary winding, $R_{21} = 0$. As a result, $V_{21} = j\omega M_{21}I_1$. This observation suggests that the mutual quality factor of the transformer computed from $Q_{21} = \frac{\omega L_{21}}{R_{21}}$ is infinite ideally.

Fig.6.33 plots the real and imaginary parts of the input impedance of the primary winding of Wu active inductors investigated in Chapter 2. Because the real part of the impedance is larger than the imaginary part in the frequency range of our interest (> 1 GHz), a low self-quality factor of the primary winding exists.

Fig.6.34 shows the real and imaginary parts of the mutual inductance from the primary winding to the secondary winding of Tang active transformers

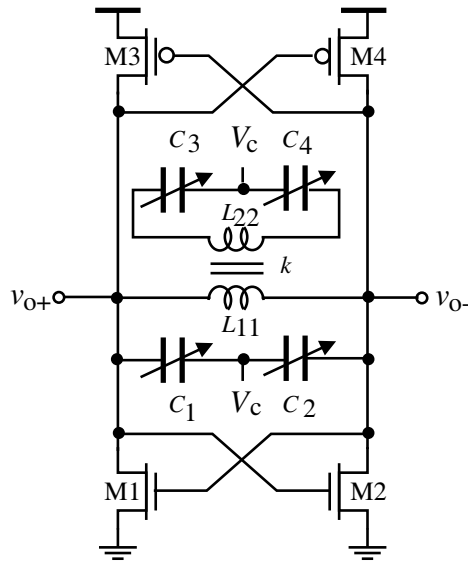


Figure 6.32. LC oscillators with spiral transformers.

investigated in Chapter 3. It is seen that the real part of the mutual inductance vanishes at 1.6 GHz approximately, resulting in a large mutual quality factor at 1.6 GHz.

The large mutual inductance of the active transformer at 1.6 GHz suggests that a lower phase noise can be obtained if LC oscillators are constructed using CMOS active transformers and operate at 1.6 GHz. Fig.6.35 shows the simplified schematic of a LC VCO using Tang active transformers investigated in Chapter 3. The LC VCO is designed to oscillate at 1.6 GHz. Fig.6.36 plots the phase noise of the active transformer oscillator at nominal process condition and at process corners, namely FF (Fast-nMOS/Fast pMOS), FS (Fast nMOS/slow pMOS), SS (slow nMOS/slow pMOS). The phase noise of the VCO is better than that of active inductor LC VCOs investigated earlier in this chapter.

The preceding LC oscillator with Tang active transformers can also be implemented using the class AB active transformers proposed by Tang *et al.* in [64] and investigated in Chapter 3. The schematic of the LC oscillator remains unchanged except that the transformer is replaced with a Tang class AB active transformer. To compare the performance of the preceding LC oscillator with Tang active transformers and Tang class AB active transformers, both oscillators are designed to oscillate at 1.6 GHz and have the same transistor sizes in order to have a fair comparison. The phase noise of the two oscillators is plotted in Fig.6.37. It is seen that the oscillator with Tang class AB transformers

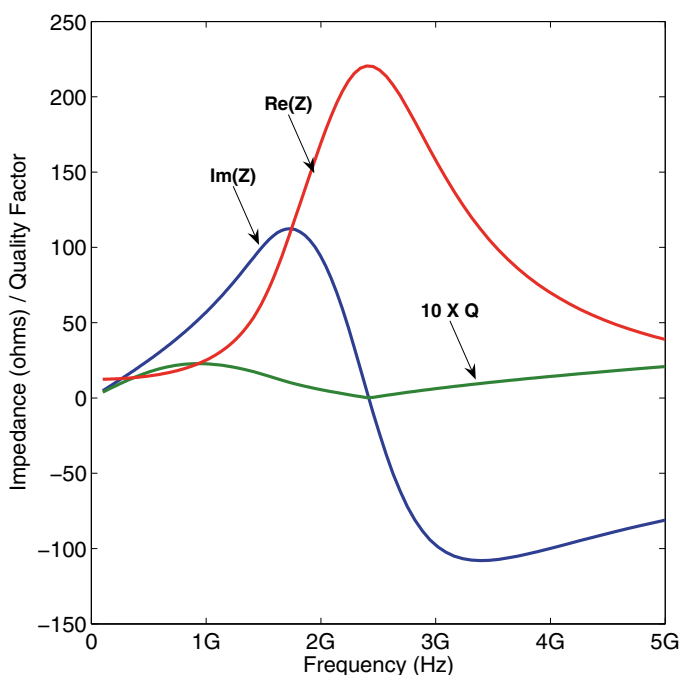


Figure 6.33. Simulated real and imaginary parts of the input impedance of Wu current reuse active inductor. Q is multiplied by 10 for a better view (© IEEE 2007).

exhibits a lower level of phase noise. As pointed out in Chapter 3, class AB active transformers exhibit a large average mutual quality factor as compared with their class A counterparts. It is this large mutual quality factor that yields a better phase noise.

Fig.6.38 plots the phase noise of the class AB transformer LC oscillator at four process corners provided by TSMC, namely FF (Fast-nMOS/Fast-pMOS), FS (Fast-nMOS/Slow-pMOS), SF (Slow-nMOS/Fast-pMOS), and SS (Slow-nMOS/Slow-pMOS). It is observed that the phase noise of the oscillator is sensitive to process variation. It should be noted that the biasing condition of the transformer was adjusted for each process corner and supply voltage variation to ensure that the oscillation frequency of the oscillator remains at 1.6 GHz.

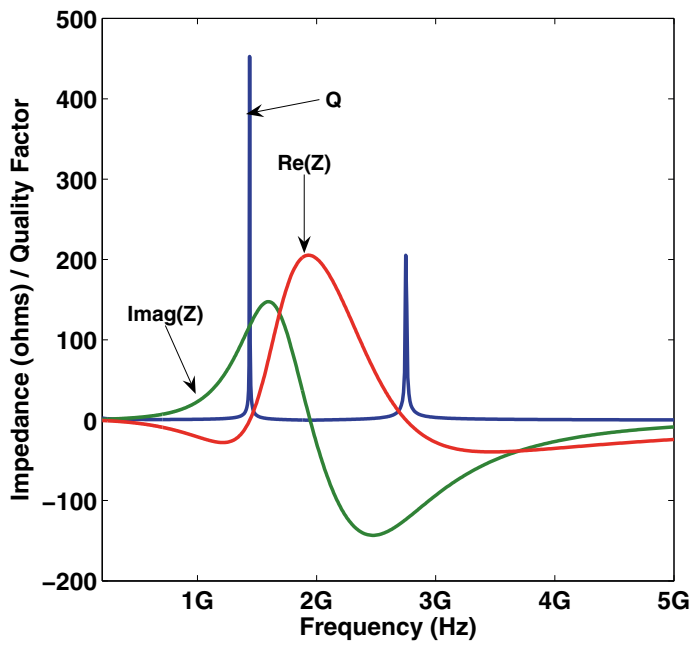


Figure 6.34. Simulated real and imaginary parts of the mutual impedance from the primary winding to the secondary winding of Tang active transformer (© IEEE 2007).

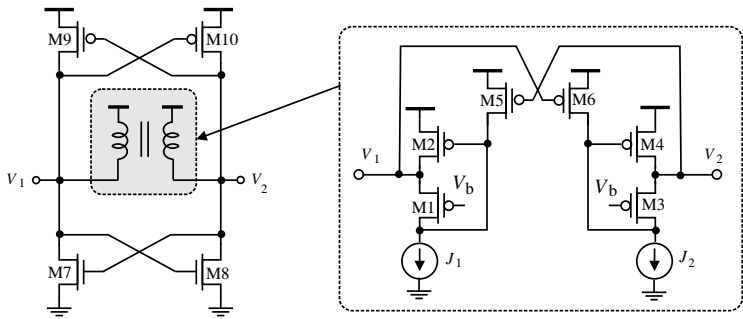


Figure 6.35. LC oscillator with Tang active transformers.

6.5 Quadrature LC VCOs With Active Inductors

Quadrature oscillators are usually implemented using LC-tank VCOs with spiral inductors or transformers. Fig.6.39 shows the simplified schematic of the quadrature LC oscillator proposed in [5]. The simplified schematic of trans-

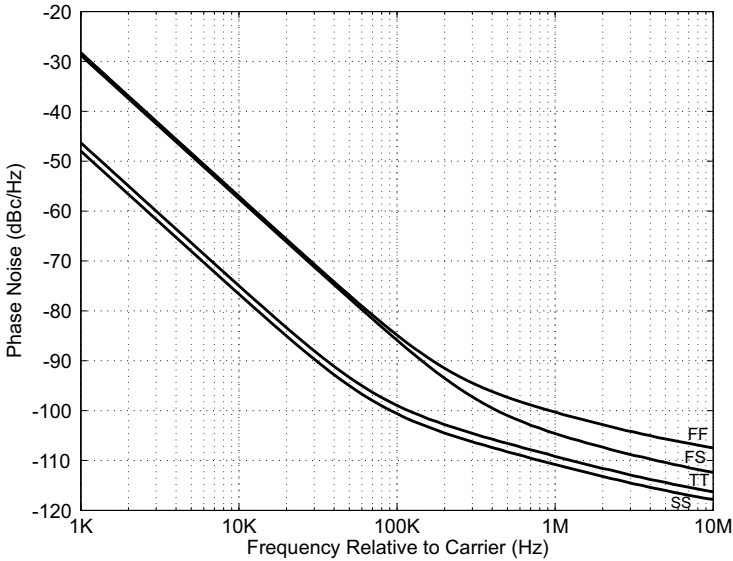


Figure 6.36. Simulated phase noise of LC oscillator with Tang active transformer (© IEEE 2007).

former quadrature oscillator proposed in [2] are shown in Fig.6.40. Variable capacitors C_{1-4} are MOS varactors for frequency tuning.

These oscillators typically require a large silicon area due to the need for four spiral inductors or two spiral transformers. In this section, we show that quadrature oscillators can be implemented using CMOS active inductors to significantly reduce silicon consumption.

Mahmoudi-Salama floating active inductors investigated in Chapter 2 are based on differential-pair transconductors. As compared with Lu floating active inductors, although Mahmoudi-Salama active inductors require more transistors subsequently a larger silicon area, their modular configuration greatly eases the difficulties encountered in both transistor sizing and proper dc biasing. Fig.6.41 shows the simplified schematic of a quadrature LC oscillator with Mahmoudi-Salama active inductors. Transistors $M_{5-7,16-19}$ form negative resistors whose resistances are tuned by varying V_{c2} , as detailed in Chapter 2. MOS varactors are implemented by M_{8-11} . They contribute to the capacitances of the tanks of the oscillator. The oscillation frequency can be tuned by varying V_{c1} for coarse tuning and $V_{c3,c4}$ for fine tuning. Note that $V_{c3,c4}$ also adjust the quadrature phases of the oscillator so that a better quadrature phase relation can be obtained.

Implemented in a 0.18 μm 1.8 V CMOS technology, the quadrature phase and magnitude matching of the oscillator exceeded 1.5 degree and 1 dB, re-

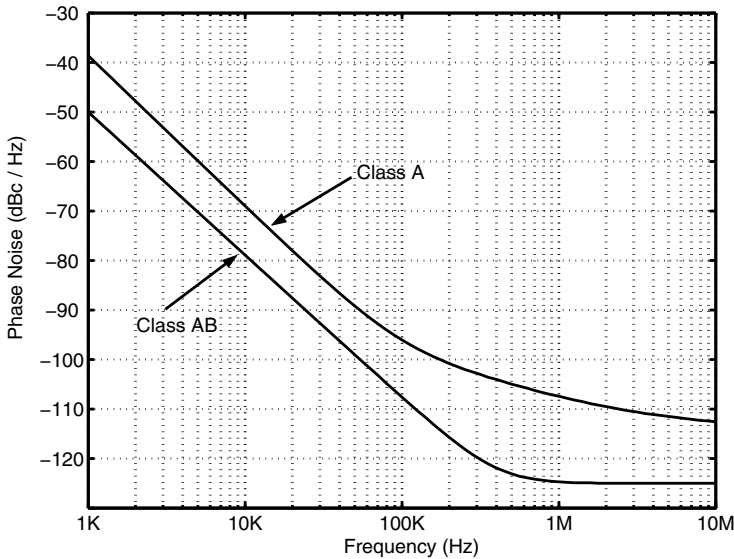


Figure 6.37. Simulated phase noise of class A and class AB CMOS active transformer VCOs (© IEEE 2007).

spectively over the bandwidth of 100 MHz at 8 GHz. The power consumption of the oscillator was 12 mW. The silicon consumption of the oscillator was $0.15 \times 0.09 \text{ mm}^2$.

6.6 Quadrature LC VCOs with Active Transformers

As compared with quadrature LC oscillators with spiral inductors, quadrature LC oscillators with spiral transformers offer several advantages including a smaller silicon area, a large inductance, and an improved quality factor. In this section, we show that CMOS active transformers investigated in Chapter 3 can be used to construct quadrature LC oscillators to significantly reduce the silicon consumption while providing a good phase noise performance.

The simplified schematic of the quadrature oscillator employing two Tang active transformers is shown in Fig. 6.42. The oscillator consists of two LC oscillators with Tang active transformers. Each LC oscillator employs two negative resistors, one implemented using a nMOS pair and the other implemented in a pMOS pair, to improve the quality factor of the transformers, subsequently the phase noise of the oscillator. The coupling between the two tank oscillators is via four nMOS-based transconductors in a parallel manner. The oscillation frequency can be tuned by varying the inductances of the transformers, which is adjustable by varying the dc biasing currents of the transformers.

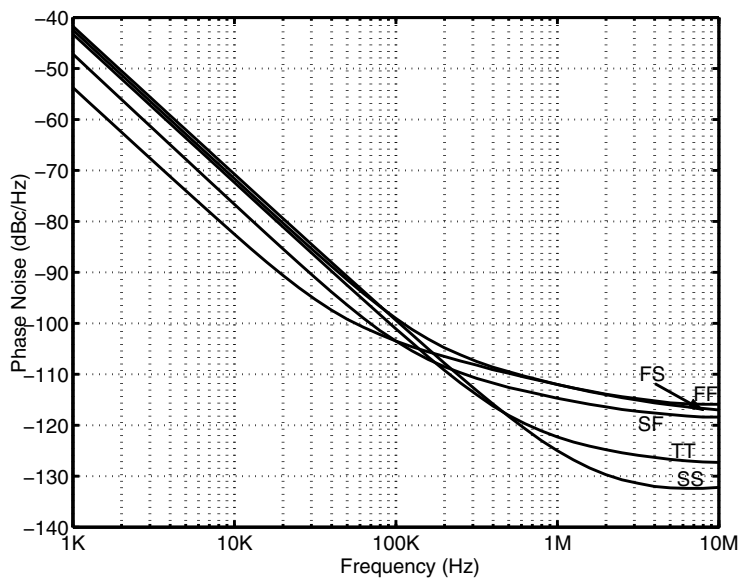


Figure 6.38. Simulated phase noise of class AB transformer oscillator at process corners (© IEEE 2007).

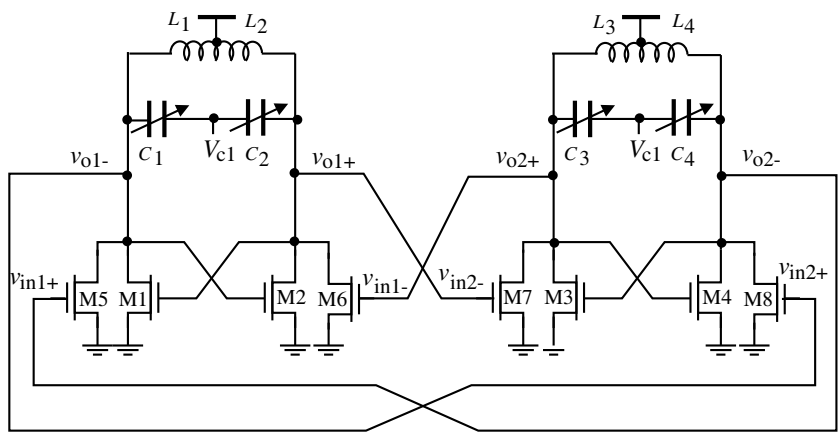


Figure 6.39. Quadrature oscillators with spiral inductors. Two LC oscillators are coupled using parallel transistors M_{5-8} .

Implemented in TSMC-0.18 μ m 1.8V CMOS technology with an oscillation frequency of 1.6 GHz, the phase noise of the oscillator is plotted in Fig.6.43 in the typical process condition and at process corners. The phase noise in the

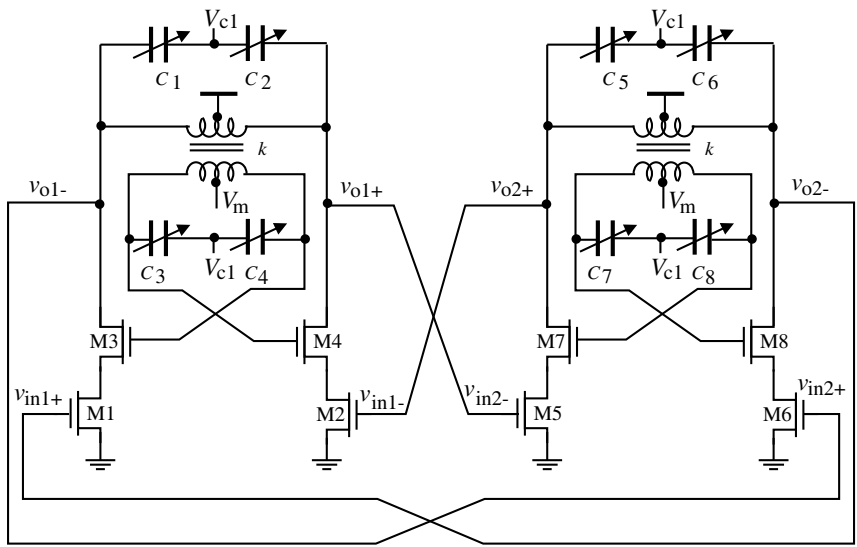


Figure 6.40. Quadrature oscillators with spiral transformers. V_m provides dc biasing voltages for $M_{3,4,7,8}$. Two spiral transformer LC oscillators are coupled using series transistors $M_{1,2,5,6}$.

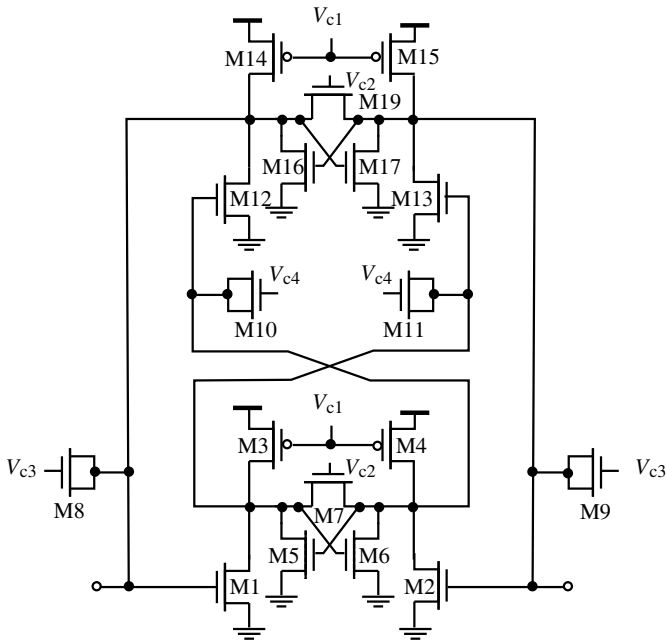


Figure 6.41. LC VCO with Mahmoudi-Salama floating active inductors.

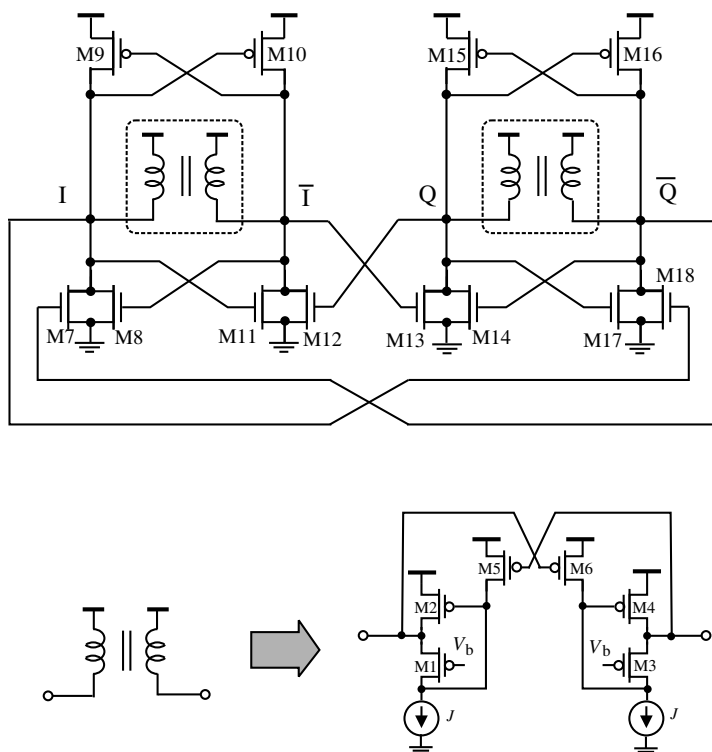


Figure 6.42. Quadrature LC oscillator using Tang active transformers. Two active transformer LC oscillators are coupled using parallel transistors $M_{7,12,13,18}$.

typical process condition is approximately -110 dBc/Hz at 1 MHz frequency offset.

6.7 Performance Comparison of Active LC VCOs

The performance of the active LC oscillators, which include LC oscillators with active inductors and LC oscillators with active transformers is compared in Table 6.1. It is observed that the active LC oscillator with Lu active inductors outperforms other active LC oscillators due to the compact differential configuration of Lu active inductors. The Tang active LC oscillator with active transformers offers a low level of phase noise. The phase noise of the active LC oscillator with Tang class AB active transformers is the lowest (-125 dBc/Hz @ 1 MHz) and is comparable to that of passive LC oscillators. Also the phase noise of the quadrature active LC oscillator proposed by Tang *et al.* offers a low level of phase noise.

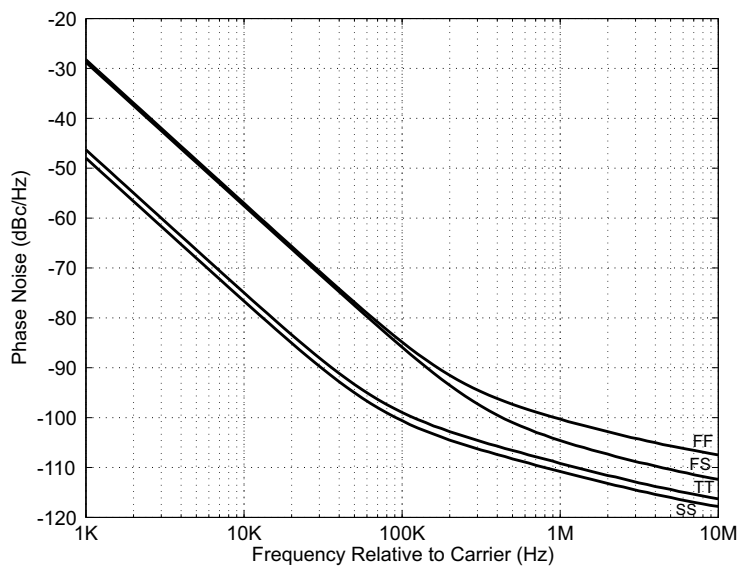


Figure 6.43. Simulated phase noise of quadrature oscillator with Tang active transformers (© IEEE 2007).

Table 6.1. Performance comparison of active inductor / active transformer LC oscillators.

Ref.	Year	Technology	VCO	f_o [GHz]	Phase noise [dBc/Hz]
Lin-Payne [39]	2000	0.35 μ m	VCO	2.5	-88 @0.6 MHz
Wu <i>et al.</i> [42]	2001	0.35 μ m	VCO	0.1-0.9	-95 @0.5 MHz
Xiao-Schaumann [75]	2002	0.20 μ m	VCO	4.95	-81 @0.5 MHz
Lu <i>et al.</i> [60]	2006	0.18 μ m	VCO	0.5-3.0	-101~-118 @1 MHz
Tang <i>et al.</i> [63]	2007	0.18 μ m	TVCO (Class A)	1.6	-108 @1 MHz
Tang <i>et al.</i> [64]	2007	0.18 μ m	TVCO (Class AB)	1.6	-125 @1 MHz
Tang <i>et al.</i> [149]	2007	0.18 μ m	QVCO	1.6	-115 @1 MHz

6.8 Chapter summary

The principles of the operation of ring oscillators and LC oscillators have been presented. We have shown that for LC oscillators, Barkhausen amplitude criterion is satisfied by employing LC tanks as the load of the amplification stages while Barkhausen phase criterion is met by employing two amplification stages. The large impedance of LC tank loads at the resonant frequency of the

tanks also ensures that the oscillation frequency of LC oscillators is the resonant frequency of the LC tanks. For ring oscillators, Barkhausen criteria are satisfied by a proper choice of the number of delay stages and the large voltage gain of each delay stage in its transition region. The phase noise of oscillators has also been investigated in detail. We have shown that in order to minimize the phase noise of oscillators, boosting the quality factor of the oscillators is critical.

Three families of ring oscillators with active inductors, namely source-coupled ring oscillators, cross-coupled ring oscillators, and Park-Kim ring oscillators, have been investigated in detail. Source-coupled ring oscillators offer the advantage of a constant current drawn from the supply voltage. As a result, the switching noise generated by the oscillators is minimized. The voltage swing of source-coupled ring oscillators, however, is small due to the voltage drop of the biasing tail current source. Cross-coupled ring oscillators offer a rail-to-rail output voltage swing, however, at the cost of a high level of switching noise. This is because the total current drawn by each delay stage of the oscillators is no longer constant. Both source-coupled and cross-coupled ring oscillators suffer from the drawback of waveform asymmetry because only the charge time of the output nodes of the delay stages of these VCOs is controlled. The key advantage of Park-Kim ring oscillators is the improved waveform symmetry as the delay of the delay stages of these oscillators is controlled by adjusting the intensity of the latch that affects both the charge and discharge times of the stages.

The design of active LC oscillators, which include active inductor LC oscillators, active inductor quadrature LC oscillators, active transformer LC oscillators, and active transformer quadrature LC oscillators, has been investigated in detail. The performance of these active LC oscillators has been compared. We have shown that the phase noise of active LC oscillators is high, approximately 10-20 dB higher as compared with that of passive LC oscillators. The active LC oscillator with Lu active inductors outperforms other active LC oscillators due to the compact differential configuration of Lu active inductors. The Tang active transformer LC oscillator offers a low level of phase noise. The phase noise of the active LC oscillator with Tang class AB active transformers is the lowest (-125 dBc/Hz @ 1 MHz). Also the quadrature active transformer LC oscillator proposed by Tang *et al.* offers a low level of phase noise.