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RF Passive IC Components

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11.1 Introduction

Passive energy storage elements are widely used in radio-frequency (RF) circuits. Although their impedance behavior often can be mimicked by compact active circuitry, it remains true that passive elements offer the largest dynamic range and the lowest power consumption. Hence, the highest performance will always be obtained with passive inductors and capacitors. Unfortunately, standard integrated circuit technology has not evolved with a focus on providing good passive elements. This chapter describes the limited palette of options available, as well as means to make the most use out of what is available.

11.2 Fractal Capacitors

Of capacitors, the most commonly used are parallel-plate and MOS structures. Because of the thin gate oxides now in use, capacitors made out of MOSFETs have the highest capacitance density of any standard IC option, with a typical value of approximately $7 \text{ fF}/\mu\text{m}^2$ for a gate oxide thickness of 5 nm. A drawback, however, is that the capacitance is voltage dependent. The applied potential must be well in excess of a threshold voltage in order to remain substantially constant. The relatively low breakdown voltage (on the order of 0.5 V/nm of oxide) also imposes an unwelcome constraint on allowable signal amplitudes. An additional drawback is the effective series resistance of such structures, due to the MOS channel resistance. This resistance is particularly objectionable at radio frequencies, since the impedance of the combination may be dominated by this resistive portion.

Capacitors that are free of bias restrictions (and that have much lower series resistance) may be formed out of two (or more) layers of standard interconnect metal. Such parallel-plate capacitors are quite linear and possess high breakdown voltage, but generally offer two orders of magnitude lower capacitance density than the MOSFET structure. This inferior density is the consequence of a conscious and continuing effort by technologists to keep low the capacitance between interconnect layers. Indeed, the

vertical spacing between such layers generally does not scale from generation to generation. As a result, the disparity between MOSFET capacitance density and that of the parallel-plate structure continues to grow as technology scales.

A secondary consequence of the low density is an objectionably high capacitance between the bottom plate of the capacitor and the substrate. This bottom-plate capacitance is often a large fraction of the main capacitance. Needless to say, this level of parasitic capacitance is highly undesirable.

In many circuits, capacitors can occupy considerable area, and an area-efficient capacitor is therefore highly desirable. Recently, a high-density capacitor structure using lateral fringing and fractal geometries has been introduced.¹ It requires no additional processing steps, and so it can be built in standard digital processes. The linearity of this structure is similar to that of the conventional parallel-plate capacitor. Furthermore, the bottom-plate parasitic capacitance of the structure is small, which makes it appealing for many circuit applications. In addition, unlike conventional metal-to-metal capacitors, the density of a fractal capacitor increases with scaling.

Lateral Flux Capacitors

Figure 11.1(a) shows a lateral flux capacitor. In this capacitor, the two terminals of the device are built using a single layer of metal, unlike a vertical flux capacitor, where two different metal layers must be used. As process technologies continue to scale, lateral fringing becomes more important. The lateral spacing of the metal layers, s , shrinks with scaling, yet the thickness of the metal layers, t , and the vertical spacing of the metal layers, t_{ox} , stay relatively constant. This means that structures utilizing lateral flux enjoy a significant improvement with process scaling, unlike conventional structures that depend on vertical flux. Figure 11.1(b) shows a scaled lateral flux capacitor. It is obvious that the capacitance of the structure of Fig. 11.1(b) is larger than that of Fig. 11.1(a).

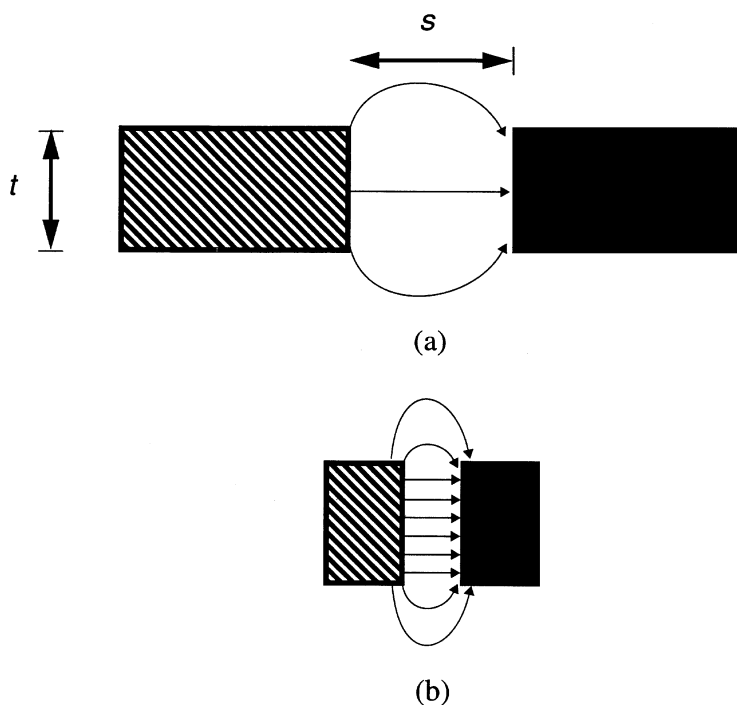


FIGURE 11.1 Effect of scaling on lateral flux capacitors: (a) before scaling and (b) after scaling.

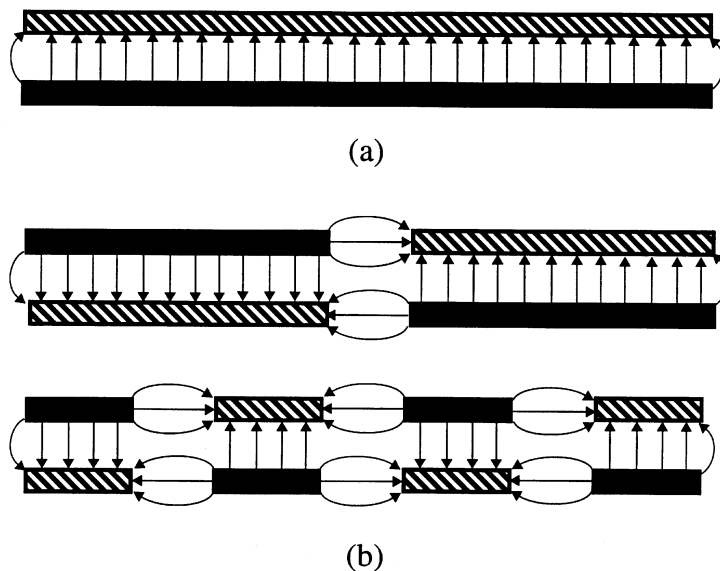


FIGURE 11.2 Vertical flux vs. lateral flux: (a) a standard parallel-plate structure, and (b) cross-connected metal layers.

Lateral flux can be used to increase the total capacitance obtained in a given area. Figure 11.2(a) is a standard parallel-plate capacitor. In Fig. 11.2(b), the plates are broken into cross-connected sections.² As can be seen, a higher capacitance density can be achieved by using lateral flux as well as vertical flux. To emphasize that the metal layers are cross connected, the two terminals of the capacitors in Fig. 11.2(b) are identified with two different shadings. The idea can be extended to multiple metal layers as well.

Figure 11.3 shows the ratio of metal thickness to minimum lateral spacing, t/s , vs. channel length for various technologies.^{3–5} The trend suggests that lateral flux will have a crucial role in the design of capacitors in future technologies.

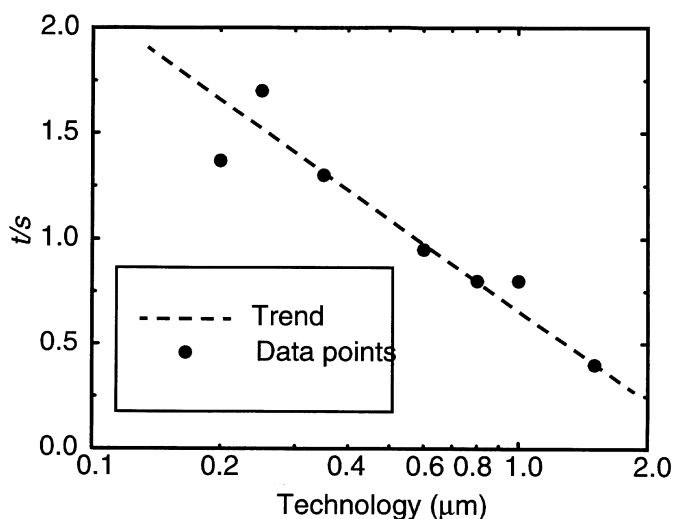


FIGURE 11.3 Ratio of metal thickness to horizontal metal spacing vs. technology (channel length).

The increase in capacitance due to fringing is proportional to the periphery of the structure; therefore, structures with large periphery per unit area are desirable. Methods for increasing this periphery are the subject of the following sections.

Fractals

A fractal is a mathematical abstract.⁶ Some fractals are visualizations of mathematical formulas, while others are the result of the repeated application of an algorithm, or a *rule*, to a *seed*. Many natural phenomena can be described by fractals. Examples include the shapes of mountain ranges, clouds, coastlines, etc.

Some ideal fractals have finite area but infinite perimeter. The concept can be better understood with the help of an example. *Koch islands* are a family of fractals first introduced as a crude model for the shape of a coastline. The construction of a Koch curve begins with an *initiator*, as shown in the example of Fig. 11.4(a). A square is a simple initiator with $M = 4$ sides. The construction continues by replacing each segment of the initiator with a curve called a *generator*, an example of which is shown in Fig. 11.4(b) that has $N = 8$ segments. The size of each segment of the generator is $r = 1/4$ of the initiator. By recursively replacing each segment of the resulting curve with the generator, a fractal border is formed. The first step of this process is depicted in Fig. 11.4(c). The total area occupied remains constant throughout the succession of stages because of the particular shape of the generator. A more complicated Koch island can be seen in Fig. 11.5. The associated initiator of this fractal has four sides and its generator has 32 segments. It can be noted that the curve is self similar, that is, each section of it looks like the entire fractal. As we zoom in on Fig. 11.5, more detail becomes visible, and this is the essence of a fractal.

Fractal dimension, D , is a mathematical concept that is a measure of the complexity of a fractal. The dimension of a flat curve is a number between 1 and 2, which is given by

$$D = \frac{\log(N)}{\log\left(\frac{1}{r}\right)} \quad (11.1)$$

where N is the number of segments of the generator and r is the ratio of the generator segment size to the initiator segment size. The dimension of a fractal curve is not restricted to integer values, hence the term “fractal.” In particular, it exceeds 1, which is the intuitive dimension of curves. A curve that has a high degree of complexity, or D , fills out a two-dimensional flat surface more efficiently. The fractal in Fig. 11.4(c) has a dimension of 1.5, whereas for the border line of Fig. 11.5, $D = 1.667$.

For the general case where the initiator has M sides, the periphery of the initiator is proportional to the square root of the area:

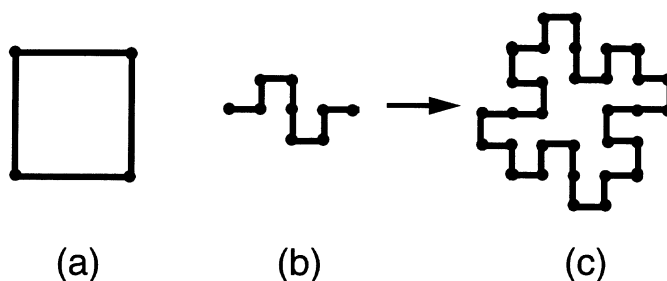


FIGURE 11.4 Construction of a Koch curve: (a) an initiator, (b) a generator, and (c) first step of the process.

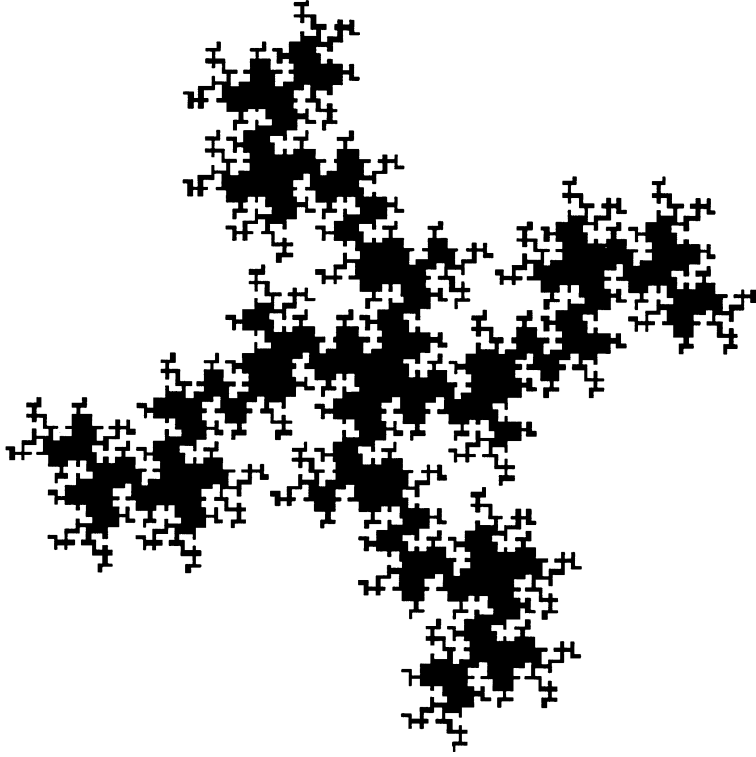


FIGURE 11.5 A Koch island with $M = 4$, $N = 32$, and $r = 1/8$.

$$P_0 = k \cdot \sqrt{A} \quad (11.2)$$

where k is a proportionality constant that depends on the geometry of the initiator. For example, for a square initiator, $k = 4$; and for an equilateral triangle, $k = 2 \cdot \sqrt[4]{27}$. After n successive applications of the generation rule, the total periphery is

$$P = k\sqrt{A} \cdot (Nr)^n \quad (11.3)$$

and the minimum feature size (the resolution) is

$$l = \frac{k\sqrt{A}}{M} \cdot r^n \quad (11.4)$$

Eliminating n from Eqs. (11.3) and (11.4) and combining the result with Eq. (11.1), we have

$$P = \frac{k^D}{M^{D-1}} \cdot \frac{(\sqrt{A})^D}{l^{D-1}} \quad (11.5)$$

Equation (11.5) demonstrates the dependence of the periphery on parameters such as the area and the resolution of the fractal border. It can be seen from Eq. (11.5) that as l tend toward zero, the periphery goes to infinity; therefore, it is possible to generate fractal structures with very large perimeters in any given area. However, the total periphery of a fractal curve is limited by the attainable resolution in practical realizations.

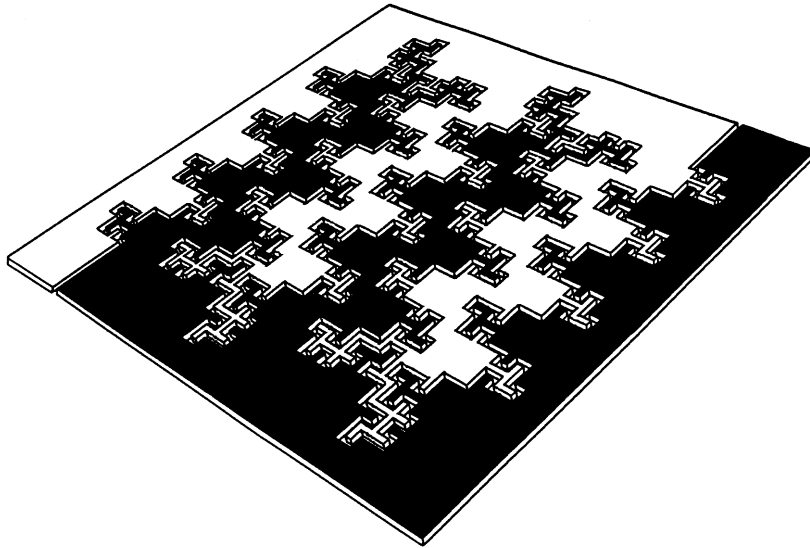


FIGURE 11.6 3-D representation of a fractal capacitor using a single metal layer.

Fractal Capacitor Structures

The final shape of a fractal can be tailored to almost any form. The flexibility arises from the fact that a wide variety of geometries can be used as the initiator and generator. It is also possible to use different generators during each step. This is an advantage for integrated circuits where flexibility in the shape of the layout is desired.

Figure 11.6 is a three-dimensional representation of a fractal capacitor. This capacitor uses only one metal layer with a fractal border. For a better visualization of the overall picture, the terminals of this square-shaped capacitor have been identified using two different shadings. As was discussed before, multiple cross-connected metal layers may be used to improve capacitance density further.

One advantage of using lateral flux capacitors in general, and fractal capacitors in particular, is the reduction of the bottom-plate capacitance. This reduction is due to two reasons. First, the higher density of the fractal capacitor (compared to a standard parallel-plate structure) results in a smaller area. Second, some of the field lines originating from one of the bottom plates terminate on the adjacent plate, instead of the substrate, which further reduces the bottom-plate capacitance as shown in Fig. 11.7. Because of this property, some portion of the parasitic bottom-plate capacitor is converted into the more useful plate-to-plate capacitance.

The capacitance per unit area of a fractal structure depends on the dimension of the fractal. To improve the density of the layout, fractals with large dimensions should be used. The concept of fractal dimension is demonstrated in Fig. 11.8. The structure in Fig. 11.8(a) has a lower dimension compared to the one in Fig. 11.8(b), so the density (capacitance per unit area) of the latter is higher.

To demonstrate the dependence of capacitance density on dimension and lateral spacing of the metal layers, a first-order electromagnetic simulation was performed on two families of fractal structures. In Fig. 11.9, the boost factor is plotted vs. horizontal spacing of the metal layers. The *boost factor* is defined as the ratio of the total capacitance of the fractal structure to the capacitance of a standard parallel-plate structure with the same area. The solid line corresponds to a family of fractals with a moderate fractal dimension of 1.63, while the dashed line represents another family of fractals with $D = 1.80$, which is a relatively large value for the dimension. In this first-order simulation, it is assumed that the vertical spacing and the thickness of the metal layers are kept

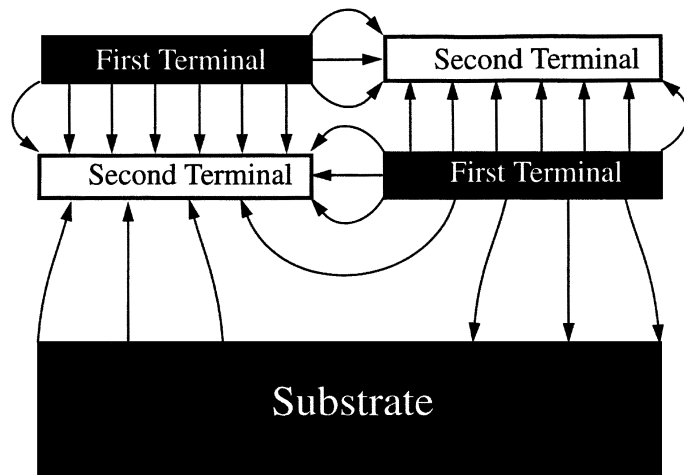
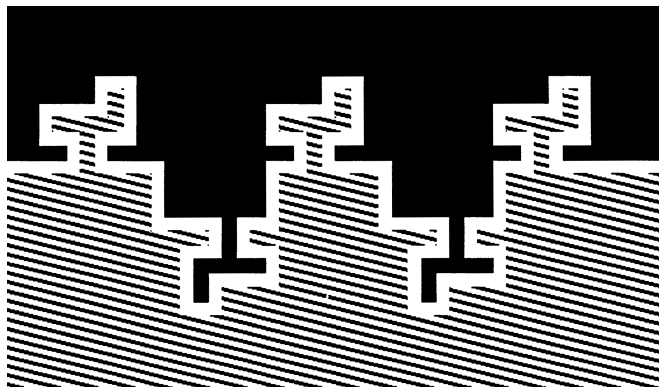
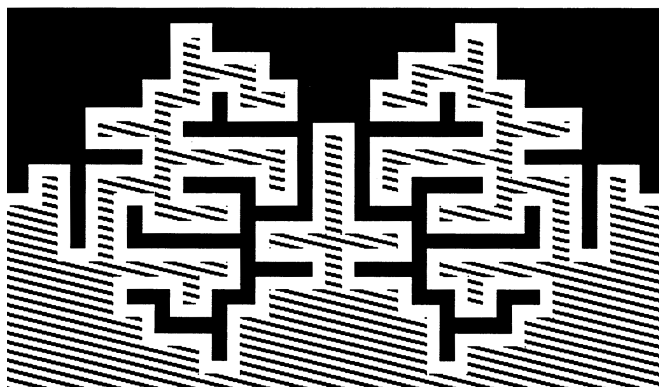


FIGURE 11.7 Reduction of the bottom-plate parasitic capacitance.



(a)



(b)

FIGURE 11.8 Fractal dimension of (a) is smaller than (b).

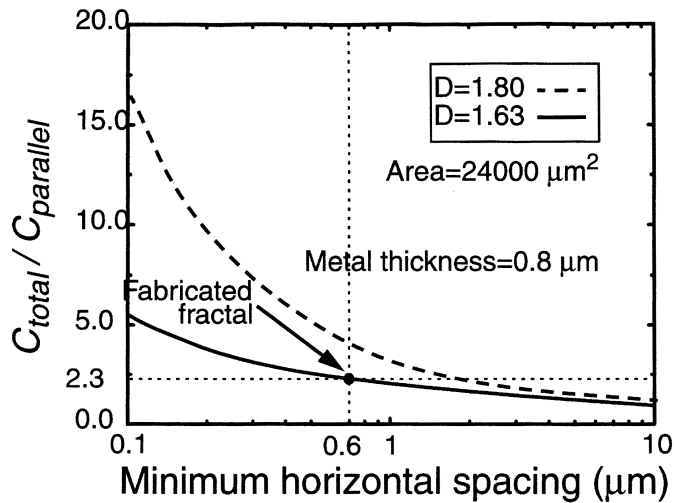


FIGURE 11.9 Boost factor vs. lateral spacing.

constant at a 0.8- μm level. As can be seen in Fig. 11.9, the amount of boost is a strong function of the fractal dimension as well as scaling.

In addition to the capacitance density, the quality factor, Q , is important in RF applications. Here, the degradation in quality factor is minimal because the fractal structure automatically limits the length of the thin metal sections to a few microns, keeping the series resistance reasonably small. For applications that require low series resistance, lower dimension fractals may be used. Fractals thus add one more degree of freedom to the design of capacitors, allowing the capacitance density to be traded for a lower series resistance.

In current IC technologies, there is usually tighter control over the lateral spacing of metal layers compared with the vertical thickness of the oxide layers, from wafer to wafer and across the same wafer. Lateral flux capacitors shift the burden of matching away from oxide thickness to lithography. Therefore, by using lateral flux, matching characteristics can improve. Furthermore, the pseudo-random nature of the structure can also compensate, to some extent, the effects of non-uniformity of the etching process. To achieve accurate ratio matching, multiple copies of a unit cell should be used, as is standard practice in high-precision analog circuit design.

Another simple way of increasing capacitance density is to use an interdigitated capacitor depicted in Fig. 11.10.^{2,7} One disadvantage of such a structure compared to fractals is its inherent parasitic inductance. Most of the fractal geometries randomize the direction of the current flow and thus reduce the effective series inductance; whereas for interdigitated capacitors, the current flow is in the same direction for all the parallel stubs. In addition, fractals usually have lots of rough edges that accumulate electrostatic energy more efficiently compared to interdigitated capacitors, causing a boost in capacitance (generally of the order of 15%). Furthermore, interdigitated structures are more vulnerable to non-uniformity of the etching process. However, the relative simplicity of the interdigitated capacitor does make it useful in some applications.

The woven structure shown in Fig. 11.11 may also be used to achieve high capacitance density. The vertical lines are in metal-2 and horizontal lines are in metal-1. The two terminals of the capacitor are identified using different shades. Compared to an interdigitated capacitor, a woven structure has much less inherent series inductance. The current flowing in different directions results in a higher self-resonant frequency. In addition, the series resistance contributed by vias is smaller than that of an interdigitated capacitor, because cross-connecting the metal layers can be done with greater ease. However, the capacitance density of a woven structure is smaller compared to an interdigitated capacitor with the same metal pitch, because the capacitance contributed by the vertical fields is smaller.

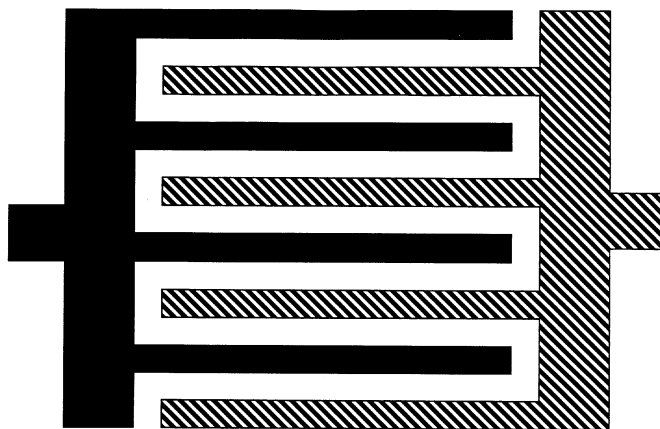


FIGURE 11.10 An interdigitated capacitor.

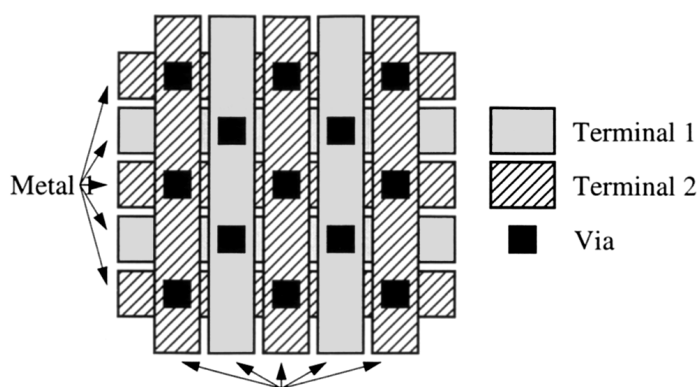


FIGURE 11.11 A woven structure.

11.3 Spiral Inductors

More than is so with capacitors, on-chip inductor options are particularly limited and unsatisfactory. Nevertheless, it is possible to build practical spiral inductors with values up to perhaps 20 nH and with Q values of approximately 10. For silicon-based RF ICs, Q degrades at high frequencies due to energy dissipation in the semiconducting substrate.⁸ Additionally, noise coupling via the substrate at GHz frequencies has been reported.⁹ As inductors occupy substantial chip area, they can potentially be the source and receptor of detrimental noise coupling. Furthermore, the physical phenomena underlying the substrate effects are complicated to characterize. Therefore, decoupling the inductor from the substrate can enhance the overall performance by increasing Q , improving isolation, and simplifying modeling.

Some approaches have been proposed to address the substrate issues; however, they are accompanied by drawbacks. Some¹⁰ have suggested the use of high-resistivity (150 to 200 Ω -cm) silicon substrates to mimic the low-loss, semi-insulating GaAs substrate, but this is rarely a practical option. Another approach selectively removes the substrate by etching a pit under the inductor.¹¹ However, the etch adds extra processing cost and is not readily available. Moreover, it raises reliability concerns such as packaging yield and long-term mechanical stability. For low-cost integration of inductors, the solution to substrate problems should avoid increasing process complexity.

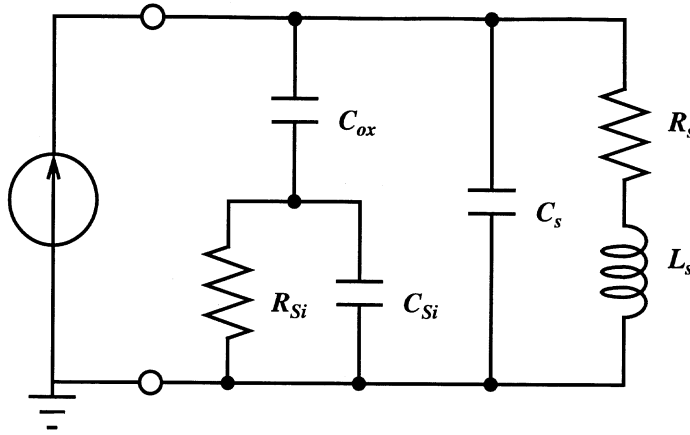


FIGURE 11.12 Lumped physical model of a spiral inductor on silicon.

In this section, we present the *patterned ground shield* (PGS),²³ which is compatible with standard silicon technologies, and which reduces the unwanted substrate effects. The great improvement provided by the PGS reduces the disparity in quality between spiral inductors made in silicon and GaAs IC technologies.

Understanding Substrate Effects

To understand why the PGS should be effective, consider first the physical model of an ordinary inductor on silicon, with one port and the substrate grounded, as shown in Fig. 11.12.⁸ An on-chip inductor is physically a three-port element including the substrate. The one-port connection shown in Fig. 11.12 avoids unnecessary complexity in the following discussion and at the same time preserves the inductor characteristics. In the model, the series branch consists of L_s , R_s , and C_s . L_s represents the spiral inductance, which can be computed using the Greenhouse method¹² or well approximated by simple analytical formulas to be presented later. R_s is the metal series resistance whose behavior at RF is governed by the eddy current effect. This resistance accounts for the energy loss due to the skin effect in the spiral interconnect structure as well as the induced eddy current in any conductive media close to the inductor. The series feedforward capacitance, C_s , accounts for the capacitance due to the overlaps between the spiral and the center-tap underpass.¹³ The effect of the inter-turn fringing capacitance is usually small because the adjacent turns are almost at equal potentials, and therefore it is neglected in this model. The overlap capacitance is more significant because of the relatively large potential difference between the spiral and the center-tap underpass. The parasitics in the shunt branch are modeled by C_{ox} , C_{Si} , and R_{Si} . C_{ox} represents the oxide capacitance between the spiral and the substrate. The silicon substrate capacitance and resistance are modeled by C_{Si} and R_{Si} , respectively.^{14,15} The element R_{Si} accounts for the energy dissipation in the silicon substrate.

Expressions for the model element values are as follows:

$$R_s = \frac{\rho l}{\delta w \left(1 - e^{-\frac{l}{\delta}} \right)} \quad (11.6)$$

$$C_s = nw^2 \cdot \frac{\epsilon_{ox}}{t_{oxM1-M2}} \quad (11.7)$$

$$C_{ox} = \frac{\epsilon_{ox}}{2t_{ox}} \cdot l \cdot w \quad (11.8)$$

$$C_{Si} = \frac{1}{2} \cdot l \cdot w \cdot C_{sub} \quad (11.9)$$

$$R_{Si} = \frac{2}{l \cdot w \cdot G_{sub}} \quad (11.10)$$

where ρ is the DC resistivity of the spiral; l is the overall length of the spiral windings; w is the line width; δ is the skin depth; n is the number of crossovers between the spiral and center-tap (and thus $n = N - 1$, where N is the number of turns); $t_{oxM1-M2}$ is the oxide thickness between the spiral and substrate; C_{sub} is the substrate capacitance per unit area; and G_{sub} is the substrate conductance per unit area. In general, one treats C_{sub} and G_{sub} as fitting parameters.

Exploration with the model reveals that the substrate loss stems primarily from the penetration of the electric field into the lossy silicon substrate. As the potential drop in the semiconductor (i.e., across R_{Si} in Fig. 11.12) increases with frequency, the energy dissipation in the substrate becomes more severe. It can be seen that increasing R_p to infinity reduces the substrate loss. It can be demonstrated that R_p approaches infinity as R_{Si} goes either to zero or infinity. This observation implies that Q can be improved by making the silicon substrate *either* a perfect insulator or a perfect conductor. Using high-resistivity silicon (or etching it away) is equivalent to making the substrate an open circuit. In the absence of the freedom to do so, the next best option is to convert the substrate into a better conductor. The approach is to insert a ground plane to block the inductor electric field from entering the silicon. In effect, this ground plane becomes a pseudo-substrate with the desired characteristics.

The ground shield cannot be a solid conductor, however, because image currents would be induced in it. These image currents tend to cancel the magnetic field of the inductor proper, decreasing the inductance. To solve this problem, the ground shield is patterned with slots orthogonal to the spiral as illustrated in Fig. 11.13. The slots act as an open circuit to cut off the path of the induced loop current. The slots should be sufficiently narrow such that the vertical electric field cannot leak through the patterned ground shield into the underlying silicon substrate. With the slots etched away, the ground strips serve as the termination for the electric field. The ground strips are merged together around the four outer edges of the spiral. The separation between the merged area and the edges is not critical. However, it is crucial that the merged area not form a closed ring around the spiral since it can potentially support unwanted loop current. The shield should be strapped with the top layer metal to provide a low-impedance path to ground. The general rule is to prevent negative mutual coupling while minimizing the impedance to ground.

The shield resistance is another critical design parameter. The purpose of the patterned ground shield is to provide a good short to ground for the electric field. Because the finite shield resistance contributes to energy loss of the inductor, it must be kept small. Specifically, by keeping the shield resistance small compared to the reactance of the oxide capacitance, the voltage drop that can develop across the shield resistance is very small. As a result, the energy loss due to the shield resistance is insignificant compared to other losses. A typical on-chip spiral inductor has parasitic oxide capacitance between 0.25 and 1 pF, depending on the size and the oxide thickness. The corresponding reactance due to the oxide capacitance at 1 to 2 GHz is of the order of 100 Ω , and hence a shield resistance of a few ohms is sufficiently small not to cause any noticeable loss.

With the PGS, one can expect typical improvements in Q ranging from 10 to 33%, in the frequency range of 1 to 2 GHz. Note that the inclusion of the ground shields increases C_p , which causes a fast roll-off in Q above the peak- Q frequency and a reduction in the self-resonant frequency. This modest improvement in inductor Q is certainly welcome, but is hardly spectacular by itself. However, a more dramatic improvement is evident when evaluating inductor-capacitor resonant circuits. Such LC tank circuits can absorb the parasitic capacitance of the ground shield. The energy stored in such parasitic elements is now part of the circuit, therefore, the overall circuit Q is greatly increased. Improvements of factors of approximately two are not unusual, so that tank circuits realized with PGS inductors possess roughly the same Q as those built in GaAs technologies.

As stated earlier, substrate noise coupling can be an issue of great concern owing to the relatively large size of typical inductors. Shielding by the PGS improves isolation by 25 dB or more at GHz

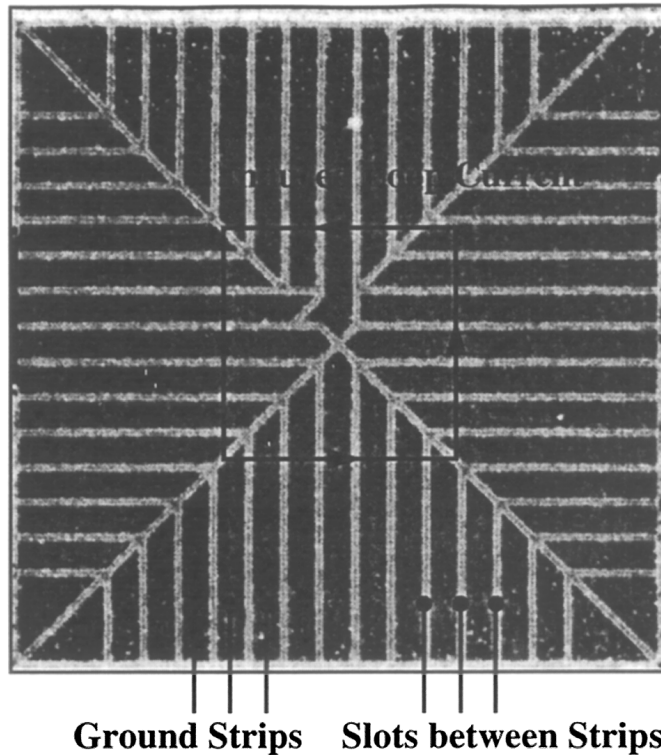


FIGURE 11.13 A close-up photo of the patterned ground shield.

frequencies. It should be noted that, as with any other isolation structure (such as a guard ring), the efficacy of the PGS is highly dependent on the integrity of the ground connection. One must often make a tradeoff between the desired isolation level and the chip area that is required to provide a low-impedance ground connection.

Simple, Accurate Expressions for Planar Spiral Inductances

In the previous section, a physically based model for planar spiral inductors was offered, and reference was made to the Greenhouse method as a means for computing the inductance value. This method uses as computational atoms the self- and mutual inductances of parallel current strips. It is relatively straightforward to apply, and yields accurate results. Nevertheless, simpler analytic formulas are generally preferred for design since important insights are usually more readily obtained.

As a specific example, square spirals are popular mainly because of their ease of layout. Other polygonal spirals have also been used to improve performance by more closely approximating a circular spiral. However, a quantitative evaluation of possible improvements is cumbersome without analytical formulas for inductance.

Among alternative shapes, hexagonal and octagonal inductors are used widely. [Figures 11.14 through 11.16](#) and show the layout for square, hexagonal, and octagonal inductors, respectively. For a given shape, an inductor is completely specified by the number of turns n , the turn width w , the turn spacing s , and any one of the following: the outer diameter d_{out} , the inner diameter d_{in} , the average diameter $d_{\text{avg}} = 0.5(d_{\text{out}} + d_{\text{in}})$, or the fill ratio, defined as $\rho = (d_{\text{out}} - d_{\text{in}})/(d_{\text{out}} + d_{\text{in}})$. The thickness of the inductor has only a very small effect on inductance and will therefore be ignored here.

We now present three approximate expressions for the inductance of square, hexagonal, and octagonal planar inductors. The first approximation is based on a modification of an expression developed by

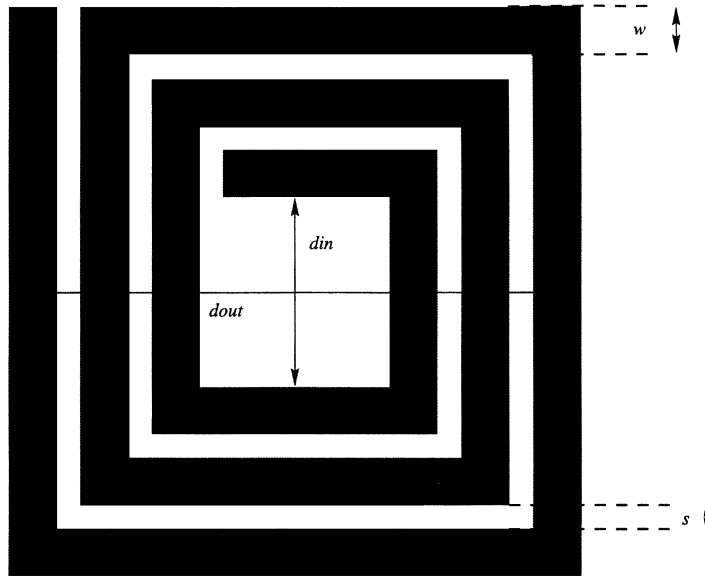


FIGURE 11.14 Square inductor.

Wheeler¹⁶; the second is derived from electromagnetic principles by approximating the sides of the spirals as current sheets; and the third is a monomial expression derived from fitting to a large database of inductors (whose exact inductance values are obtained from a 3-D electromagnetic field solver). All three expressions are accurate, with typical errors of 2 to 3%, and very simple, and are therefore excellent candidates for use in design and optimization.

Modified Wheeler Formula

Wheeler¹⁶ presented several formulas for planar spiral inductors, which were intended for discrete inductors. A simple modification of the original Wheeler formula allows us to obtain an expression that is valid for planar spiral integrated inductors:

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \quad (11.11)$$

where ρ is the fill ratio defined previously. The coefficients K_1 and K_2 are layout dependent and are shown in [Table 11.1](#)

The fill factor ρ represents how hollow the inductor is: for small ρ , we have a hollow inductor ($d_{out} \cong d_{in}$), and for a large ρ we have a filled inductor ($d_{out} \gg d_{in}$). Two inductors with the same average diameter but different fill ratios will, of course, have different inductance values; the filled one has a smaller inductance because its inner turns are closer to the center of the spiral, and so contribute less positive mutual inductance and more negative mutual inductance. Some degree of hollowness is generally desired because the innermost turns contribute little overall inductance, but significant resistance.

Expression Based on Current Sheet Approximation

Another simple and accurate expression for the inductance of a planar spiral can be obtained by approximating the sides of the spirals by symmetrical current sheets of equivalent current densities.¹⁷ For example, in the case of the square, we obtain four identical current sheets: the current sheets on opposite sides are parallel to one another, whereas the adjacent ones are orthogonal. Using symmetry and the fact

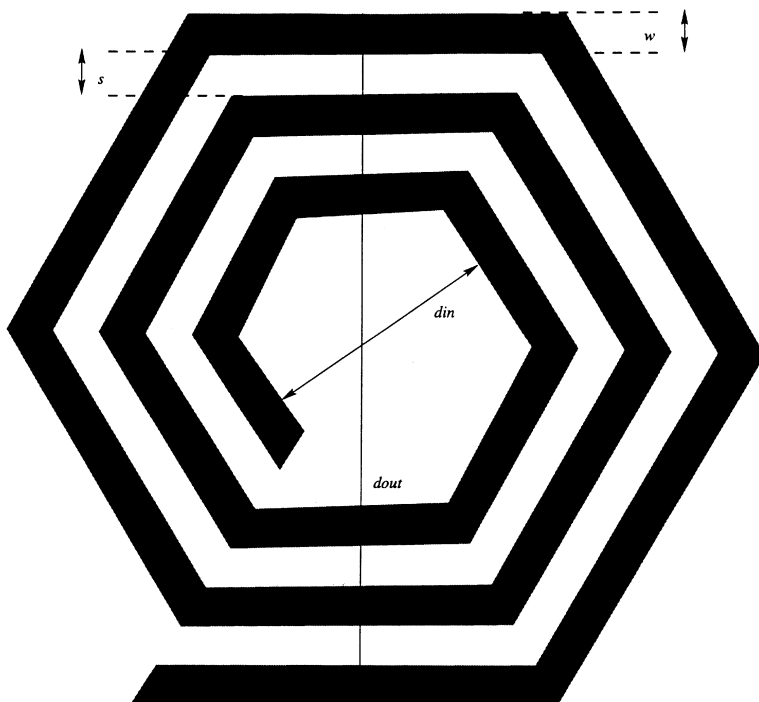


FIGURE 11.15 Hexagonal inductor.

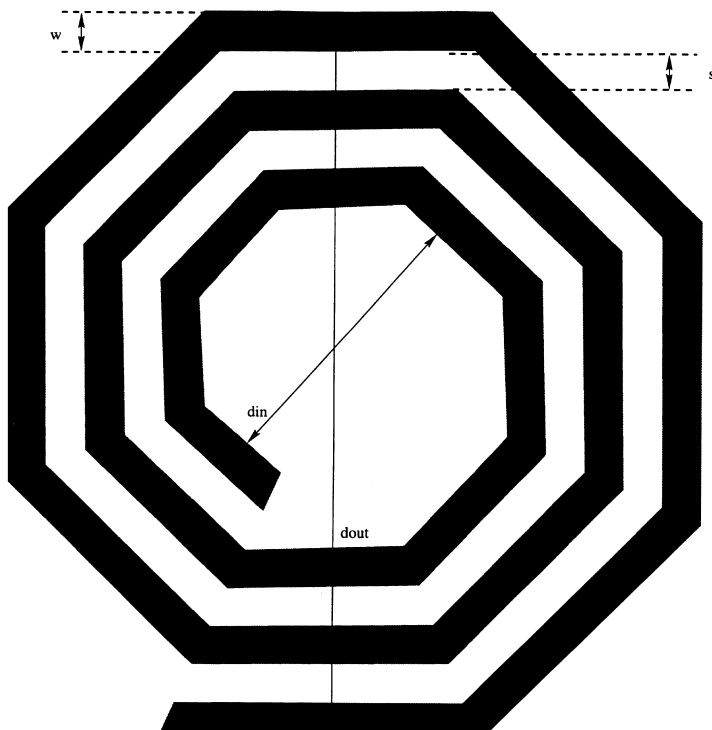


FIGURE 11.16 Octagonal inductor.

TABLE 11.1 Coefficients for Modified Wheeler Formula

Layout	K ₁	K ₂
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

that sheets with orthogonal current sheets have zero mutual inductance, the computation of the inductance is now reduced to evaluating the self-inductance of one sheet and the mutual inductance between opposite current sheets. These self- and mutual inductances are evaluated using the concepts of geometric mean distance (GMD) and arithmetic mean distance (AMD).^{17,18} The resulting expression is:

$$L_{gmd} = \frac{\mu n^2 d_{avg}}{\pi} (c_1 (\log c_2 / \rho) + c_3 \rho) \quad (11.12)$$

where the coefficients c_i are layout dependent and are listed in Table 11.2

TABLE 11.2 Coefficients for Current-Sheet Inductance Formula

Layout	c ₁	c ₂	c ₃
Square	2.00	2.00	0.54
Hexagonal	1.83	1.71	0.45
Octagonal	1.87	1.68	0.60

A detailed derivation of these formulas can be found in Ref. 19. Because this formula is based on a current sheet approximation, its accuracy worsens as the ratio s/w becomes large. In practice, this is not a problem because practical integrated spiral inductors are built with $s < w$. The reason is that a smaller spacing improves the inter-winding magnetic coupling and reduces the area consumed by the spiral. A large spacing is only desired to reduce the inter-winding capacitance. This is rarely a concern as this capacitance is always dwarfed by the under-pass capacitance.⁸

Data-Fitted Monomial Expression

Our final expression is based on a data-fitting technique, in which a population of thousands of inductors are simulated with an electromagnetic field solver. The inductors span the entire range of values of relevance to RF circuits. A monomial expression is then fitted to the data, which ultimately yields:

$$L_{mon} = \beta d_{avg}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \quad (11.13)$$

where the coefficients β and α_i are layout dependent, and given in Table 11.3.

TABLE 11.3 Coefficients for Monomial Inductance Formula

Layout	b	α_1	α_2	α_3	α_4	α_5
Square	1.66×10^{-3}	-1.33	-0.13	2.50	1.83	-0.022
Hexagonal	1.33×10^{-3}	-1.46	-0.16	2.67	1.80	-0.030
Octagonal	1.34×10^{-3}	-1.35	-0.15	2.56	1.77	-0.032

Of course, it is also possible to use other data-fitting techniques; for example, one which minimizes the maximum error of the fit, or one in which the coefficients must satisfy given inequalities or bounds. The monomial expression is useful because, similar to the other expressions, it is very accurate and very simple. Its real value, however, is that it can be used for the optimal design of inductors and

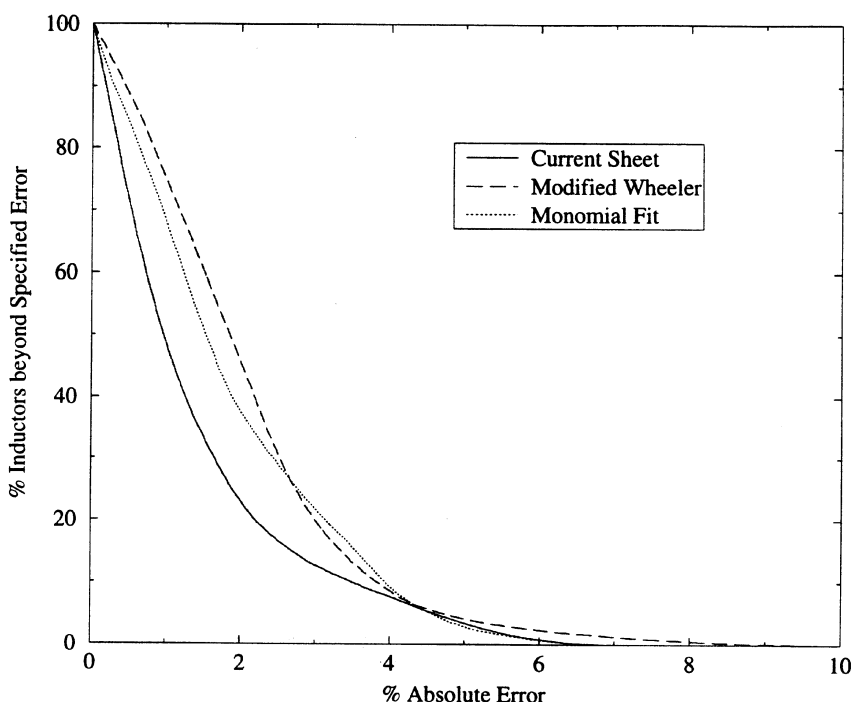


FIGURE 11.17 Error distribution for three formulas, compared with field solver simulations.

circuits containing inductors, using geometric programming, which is a type of optimization method that requires monomial models.^{20,21}

Figure 11.17 shows the absolute error distributions of these expressions. The plots show that typical errors are in the 1 to 2% range, and most of the errors are below 3%. These expressions for inductance, while quite simple, are thus sufficiently accurate that field solvers are rarely necessary.

These expressions can be included in a physical, scalable lumped-circuit model for spiral inductors where, in addition to providing design insight, they allow efficient optimization schemes to be employed.

11.4 On-Chip Transformers

Transformers are important elements in RF circuits for impedance conversion, impedance matching, and bandwidth enhancement. Here, we present an analytical model for monolithic transformers that is suitable for circuit simulation and design optimization. We also provide simple expressions for calculating the mutual coupling coefficient (k).

We first discuss different on-chip transformers and their advantages and disadvantages. We then present an analytical model along with expressions for the elements in it and the mutual coupling coefficient.

Monolithic Transformer Realizations

Figures 11.18 through 11.23 illustrate common configurations of monolithic transformers. The different realizations offer varying tradeoffs among the self-inductance and series resistance of each port, the mutual coupling coefficient, the port-to-port and port-to-substrate capacitances, resonant frequencies, symmetry, and area. The models and coupling expressions allow these trade-offs to be systematically explored, thereby permitting transformers to be customized for a variety of circuit design requirements.

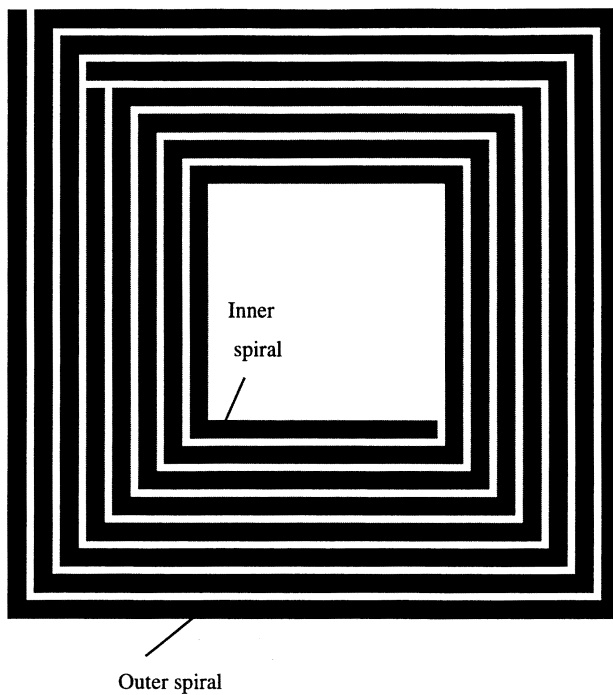


FIGURE 11.18 Tapped transformer.

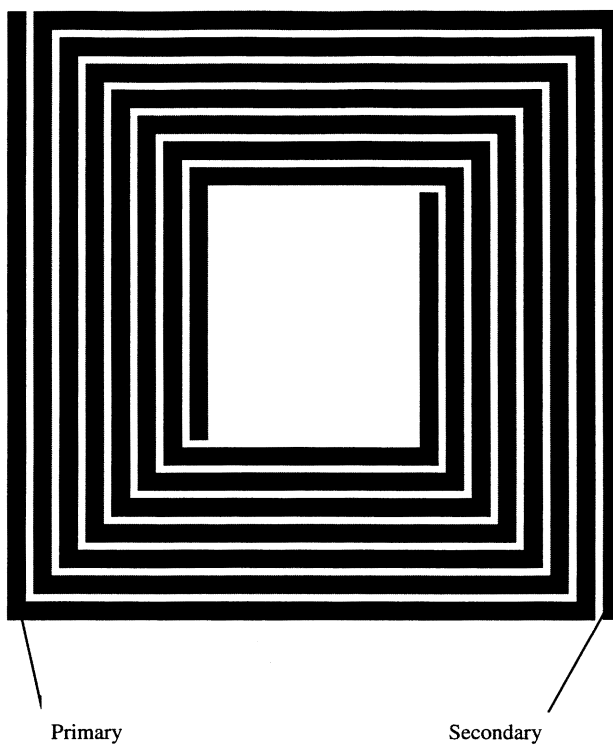


FIGURE 11.19 Interleaved transformer.

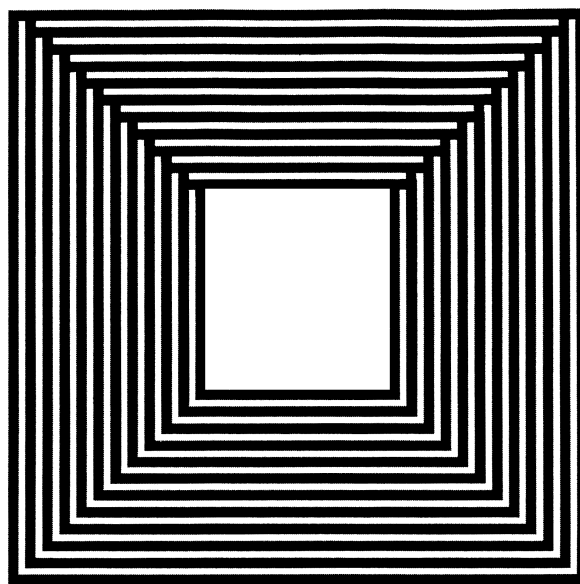


FIGURE 11.20 Stacked transformer with top spiral overlapping the bottom one.

The characteristics desired of a transformer are application dependent. Transformers can be configured as three or four-terminal devices. They may be used for narrowband or broadband applications. For example, in single-sided to differential conversion, the transformer might be used as a four-terminal narrowband device. In this case, a high mutual coupling coefficient and high self-inductance are desired, along with low series resistance. On the other hand, for bandwidth extension applications, the transformer is used as a broadband three-terminal device. In this case, a small mutual coupling coefficient and high series resistance are acceptable, while all capacitances need to be minimized.²²

The tapped transformer (Fig. 11.18) is best suited for three-port applications. It permits a variety of tapping ratios to be realized. This transformer relies only on lateral magnetic coupling. All windings can be implemented with the top metal layer, thereby minimizing port-to-substrate capacitances. Because the two inductors occupy separate regions, the self-inductance is maximized while the port-to-port capacitance is minimized. Unfortunately, this spatial separation also leads to low mutual coupling ($k = 0.3\text{--}0.5$).

The interleaved transformer (Fig. 11.19) is best suited for four-port applications that demand symmetry. Once again, capacitances can be minimized by implementing the spirals with top level metal so that high resonant frequencies may be realized. The interleaving of the two inductances permit moderate coupling ($k = 0.7$) to be achieved at the cost of reduced self-inductance. This coupling may be increased at the cost of higher series resistance by reducing the turn width (w) and spacing (s).

The stacked transformer (Fig. 11.20) uses multiple metal layers and exploits both vertical and lateral magnetic coupling to provide the best area efficiency, the highest self-inductance, and highest coupling ($k = 0.9$). This configuration is suitable for both three- and four-terminal configurations. The main drawback is the high port-to-port capacitance, or equivalently a low self-resonant frequency. In some cases, such as narrowband impedance transformers, this capacitance may be incorporated as part of the resonant circuit. Also, in multi-level processes, the capacitance can be reduced by increasing the oxide thickness between spirals. For example, in a five-metal process, 50 to 70% reductions in port-to-port capacitance can be achieved by implementing the spirals on layers five and three instead of five and four. The increased vertical separation will reduce k by less than 5%. One can also trade off reduced coupling for reduced capacitance by displacing the centers of the stacked inductors (Figs. 11.21 and 11.22)

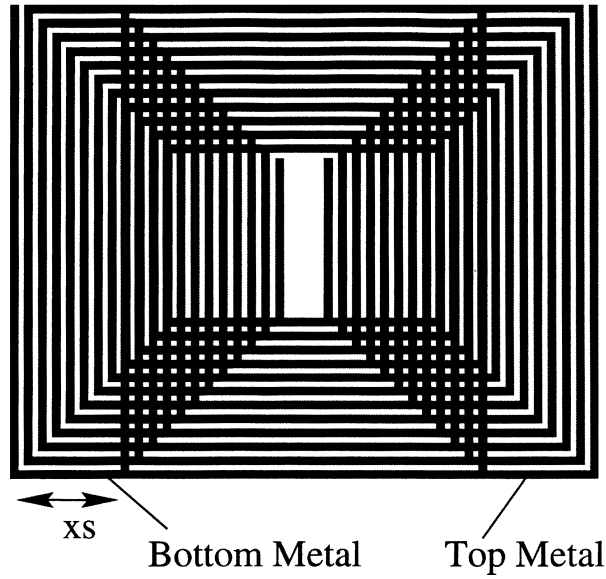


FIGURE 11.21 Stacked transformer with top and bottom spirals laterally shifted.

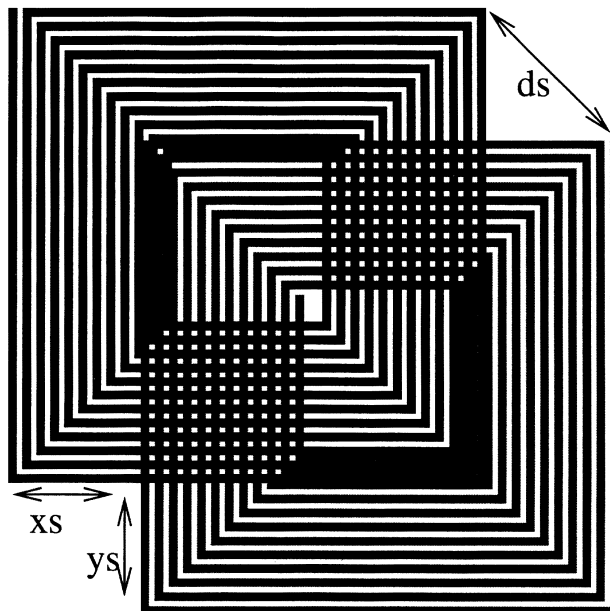


FIGURE 11.22 Stacked transformer with top and bottom spirals diagonally shifted.

Analytical Transformer Models

Figures 11.23 and 11.24 present the circuit models for tapped and stacked transformers, respectively. The corresponding element values for the tapped transformer model are given by the following equations (subscript o refers to the outer spiral, i to the inner spiral, and T to the whole spiral):

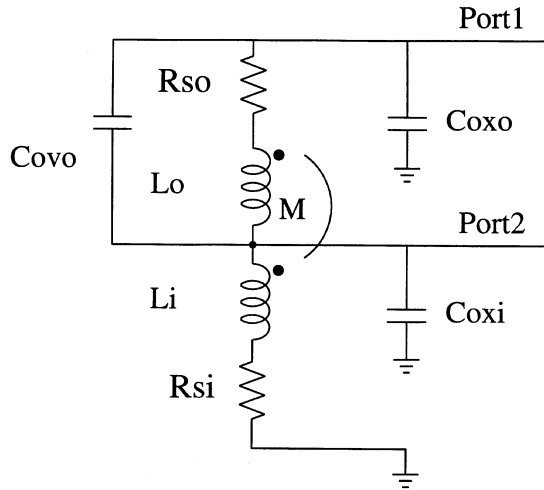


FIGURE 11.23 Tapped transformer model.

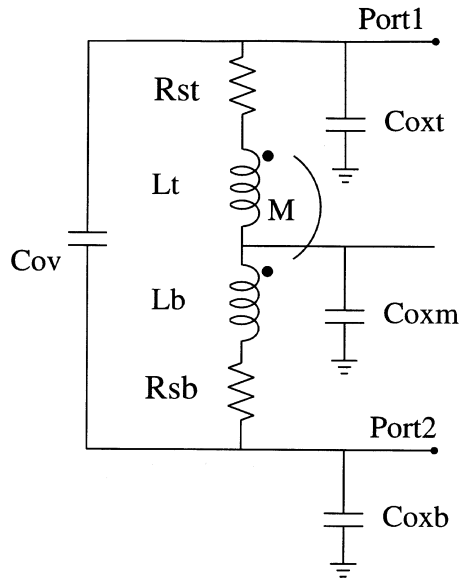


FIGURE 11.24 Stacked transformer model.

$$L_T = \frac{9.375\mu_0 n_T^2 A D_T^2}{11OD_T - 7AD_T} \quad (11.14)$$

$$L_o = \frac{9.375\mu_0 n_o^2 A D_o^2}{11OD_o - 7AD_o} \quad (11.15)$$

$$L_i = \frac{9.375\mu_0 n_i^2 A D_i^2}{11OD_i - 7AD_i} \quad (11.16)$$

$$M = \frac{L_T - L_o - L_i}{2\sqrt{L_o L_i}} \quad (11.17)$$

$$R_{so} = \frac{\rho l_o}{\delta w \left(1 - e^{-\frac{t}{\delta}}\right)} \quad (11.18)$$

$$R_{si} = \frac{\rho l_i}{\delta w \left(1 - e^{-\frac{t}{\delta}}\right)} \quad (11.19)$$

$$C_{ovo} = \frac{\epsilon_{ox}}{t_{ox, t-b}} \cdot (n_o - 1)w^2 \quad (11.20)$$

$$C_{oxo} = \frac{\epsilon_{ox}}{2t_{ox}} \cdot l_o w \quad (11.21)$$

$$C_{oxi} = \frac{\epsilon_{ox}}{2t_{ox}} \cdot (l_o + l_i)w \quad (11.22)$$

where ρ is the DC metal resistivity; δ is the skin depth; $t_{ox, t-b}$ is the oxide thickness from top level metal to bottom metal; n is the number of turns; OD , AD , and ID are the outer, average, and inner diameters, respectively; l is the length of the spiral; w is the turn width; t is the metal thickness; and A is the area.

Expressions for the stacked transformer model are as follows (subscript t refers to the top spiral and b to the bottom spiral):

$$L_t = \frac{9.375\mu_0 n^2 AD^2}{11OD_T - 7AD_T} \quad (11.23)$$

$$L_b = L_t \quad (11.24)$$

$$k = 0.9 - \frac{d_s}{AD} \quad (11.25)$$

$$M = k\sqrt{L_t L_b} \quad (11.26)$$

$$R_{st} = \frac{\rho_t l}{\delta_t w \left(1 - e^{-\frac{t_t}{\delta_t}}\right)} \quad (11.27)$$

$$R_{sb} = \frac{\rho_b l}{\delta_b w \left(1 - e^{-\frac{t_b}{\delta_b}}\right)} \quad (11.28)$$

$$C_{ov} = \frac{\epsilon_{ox}}{2t_{ox, t-b}} \cdot l \cdot w \cdot \frac{A_{ov}}{A} \quad (11.29)$$

$$C_{oxi} = \frac{\epsilon_{ox}}{2t_{oxi}} \cdot l \cdot w \cdot \frac{A - A_{ov}}{A} \quad (11.30)$$

$$C_{oxb} = \frac{\epsilon_{ox}}{2t_{ox}} \cdot l \cdot w \quad (11.31)$$

$$C_{oxm} = C_{oxt} + C_{oxb} \quad (11.32)$$

where t_{oxt} is the oxide thickness from top metal to the substrate; t_{oxb} is the oxide thickness from bottom metal to substrate; k is the coupling coefficient; A_{ov} is the overlap area of the two spirals; and d_s is the center-to-center spiral distance.

The expressions for the series resistances (R_{so} , R_{sb} , R_{st} , and R_{sb}), the port-substrate capacitances (C_{axo} , C_{oxi} , C_{oxp} , C_{oxb} , and C_{oxm}) and the crossover capacitances (C_{ovo} , C_{ovi} , and C_{ov}) are taken from Reference 8. Note that the model accounts for the increase in series resistance with frequency due to skin effect. Patterned ground shields (PGS) are placed beneath the transformers to isolate them from resistive and capacitive coupling to the substrate.²³ As a result, the substrate parasitics can be neglected.

The inductance expressions in the foregoing are based on the modified Wheeler formula discussed earlier.²⁴ This formula does not take into account the variation in inductance due to conductor thickness and frequency. However, in practical inductor and transformer realizations, the thickness is small compared to the lateral dimensions of the coil and has only a small impact on the inductance. For typical conductor thickness variations (0.5 to 2.0 μm), the change in inductance is within a few percent for practical inductor geometries. The inductance also changes with frequency due to changes in current distribution within the conductor. However, over the useful frequency range of a spiral, this variation is negligible.²³ When compared with field solver simulations, the inductance expression exhibits a maximum error of 8% over a broad design space (outer diameter OD varying from 100 to 480 μm , L varying from 0.5 to 100 nH, w varying from 2 μm to 0.3 OD , s varying from 2 μm to w , and inner diameter ID varying from 0.2 to 0.8 OD).

For the tapped transformer, the mutual inductance is determined by first calculating the inductance of the whole spiral (L_T), the inductance of the outer spiral (L_o), the inductance of the inner spiral (L_i), and then using the expression $M = (L_T - L_o - L_i)/2$. For the stacked transformer, the spirals have identical lateral geometries and therefore identical inductances. In this case, the mutual inductance is determined by first calculating the inductance of one spiral (L_T), the coupling coefficient (k) and then using the expression $M = kL_T$. In this last case, the coupling coefficient is given by $k = 0.9 - d_s/(AD)$ for $d_s < 0.7AD$, where d_s is the center-to-center spiral distance and AD is the average diameter of the spirals. As d_s increases beyond 0.7 AD , the mutual coupling coefficient becomes harder to model. Eventually, k crosses zero and reaches a minimum value of approximately -0.1 at $d_s = AD$. As d_s increases further, k asymptotically approaches zero. At $d_s = 2AD$, $k = -0.02$, indicating that the magnetic coupling between closely spaced spirals is negligible.

The self-inductances, series resistances, and mutual inductances are independent of whether a transformer is used as a three- or four-terminal device. The only elements that require recomputation are the port-to-port and port-to-substrate capacitances. This situation is analogous to that of a spiral inductor being used as a single- or dual-terminal device.

As with the inductance formulas, the transformer models obviate the need for full field solutions in all but very rare instances, allowing rapid design and optimization.

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