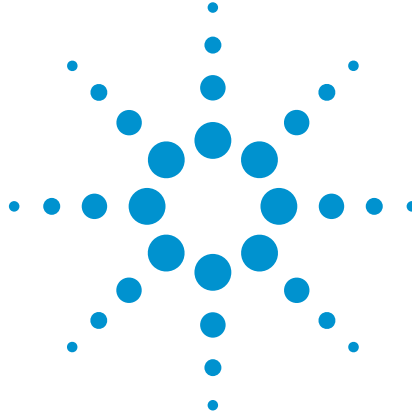




Agilent EEsof EDA

Overview on Interdigital Capacitor Design

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Interdigital Capacitor Design

Introduction: The objective of this report is to present design techniques for interdigital capacitors using the GENESYS environment. Linear and electromagnetic simulations models are considered and the results compared with hardware measurements. The results demonstrate the accuracy of these models and the power of the design software.

The interdigital (or interdigitated) capacitor is an element for producing a capacitor-like, high pass characteristic using microstrip lines. The shape of conductors is defined by the parameters shown in Figure 1. Notice that the long conductors or “fingers” provide coupling between the input and output ports across the gaps. Typically, the gaps (G) between fingers and at the end of the fingers (G_E) are the same. The length (L) and width (W) of the fingers are also specified. Since the conductors are mounted on a substrate, its characteristics will also affect performance. Of particular importance are the height of the substrate (h) and its dielectric constant (ϵ_r). In addition, the thickness of the conductor (t) and its resistivity (ρ) will also impact the electrical characteristics.

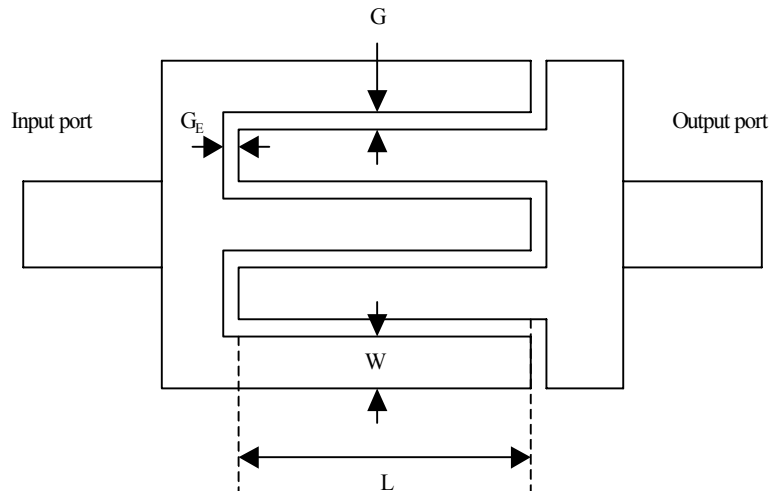


Figure 1. Interdigital Capacitor Geometry

The design objectives are generally to provide the desired capacitance at the design frequency in a reasonable area. The dielectric constant is often given, since the printed circuit board may have other uses. The capacitance increases as the gaps are decreased. Manufacturing tolerances may dictate the smallest repeatable gap. Reducing the width of the fingers reduces the required area, but increases the characteristic impedance of the line, and in general lowers the effective capacitance. As shown later in the design issues section, increasing the length of the fingers increases the capacitance, but increases the required board area.

Linear models provide a fast, accurate method of performing design trades and system optimization. The following sections describe the nature of the new linear model and its associated layout. The performance of the model will be compared with and electromagnetic simulation using this layout. Comparisons with measurements of hardware are also being presented.

New Linear Model: The GENESYS environment provides both a linear model and a corresponding layout for EM simulation. Unlike earlier linear models which employed a lumped capacitor representation, the new model (MIDCAP2) uses a distributed model. This model uses linear models of coupled lines and end gaps. The schematic symbol of MIDCAP2 is that of a capacitor with appropriate parameters (Figure 2).

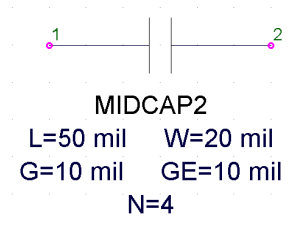


Figure 2. Schematic Symbol for MIDCAP2.

In this model the number of fingers is limited to the range of 2 to 20. The schematic for the model tested is shown in Figure 3. The microstrip lines (TL2, TL3) model the leads in the hardware model fabricated for test purposes.

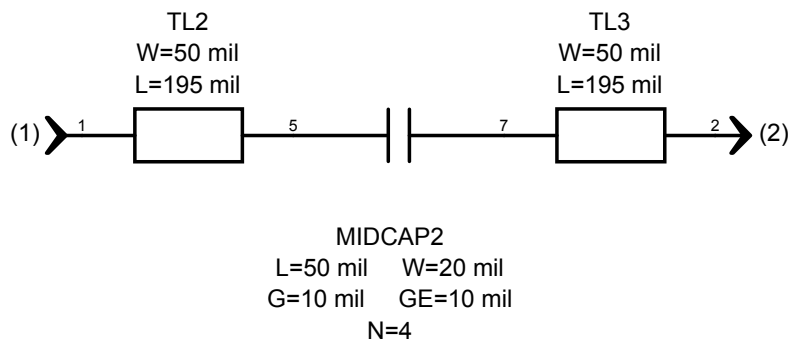


Figure 3. Schematic for Test Model.

GENESYS will automatically generate a corresponding layout by simply choosing “Add Layout” by right clicking on “Designs\Models” on the Workspace Tree. Be sure that the appropriate schematic is selected. For this example, the layout is shown in Figure 4. Leads were added to this model for hardware testing purposes. Ports are positioned at the ends of these leads in preparation for an EMPOWER simulation.

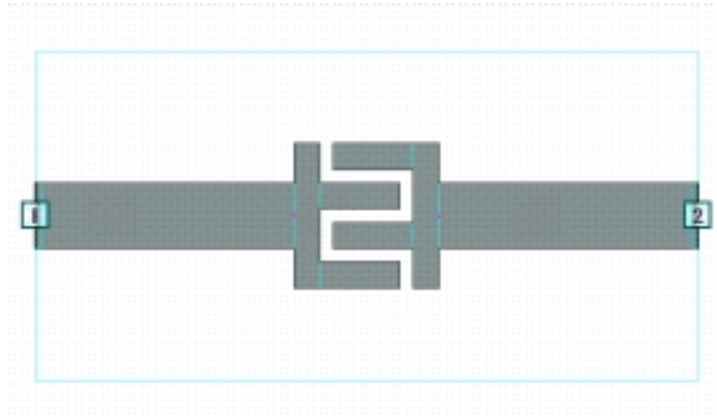


Figure 4. Layout for MIDCAP2 Example.

Example: The capacitor design with four fingers shown in Figure 4 has the following parameters:

W = Width of each conductor (finger) = 20 mils
 G = Space between conductors (fingers) = 10 mils
 GE = Space at end of conductor (finger) = 10 mils
 L = Length of fingers = 50 mils
 N = Number of fingers = 4

Substrate Definition

ϵ_r = Dielectric constant = 3.05	t = Metal thickness = 1.4 mils
$\tan\delta$ = Loss tangent = 0.0045	Sr = Surface roughness = 0.094
ρ = Resistivity = 1.	h = Height = 20 mils

This design was fabricated and tested. The data was collected using a network analyzer connected to a PC with a GPIB interface. The data was imported into GENESYS using TEST LINK. A photograph of the hardware is presented as Figure 5.



Figure 5. Four Finger MIDCAP Element Under Test.

The s-parameters for the linear model, EM simulation and test data are compared in Figure 6. The design frequency was 5.0 GHz. At this frequency, the differences in effective capacitance (C_{eff}) are:

EMPOWER: $C_{\text{eff}} = 0.082$ pf
MIDCAP2: $C_{\text{eff}} = 0.089$ pf
Hardware: $C_{\text{eff}} = 0.068 - 0.077$ pf

The spread of values for the hardware represents the scatter in the data in the 4 to 6 GHz region. Some of the differences between the models and the hardware test can be attributed to the milling process. It was estimated that 1-2 mils of substrate might have been removed in the gaps. This can easily account for the reduced capacitance of the hardware. A first order test of this hypothesis was to reduce the thickness of the substrate by 2 mils. Using the linear model, the capacitance was reduced to 0.073 pf. This is about the middle of the range of hardware values. Also shown in Figure 6 is another advanced simulator response (AdSim) with similar characteristics, but lower overall accuracy.

GENESYS provides an easy way to compute an effective capacitance. In a blank schematic window, add a capacitor by pressing the “C” key. Then add an input port (“I”) and output (“O”). Set the capacitor value to “?1” in the capacitor dialog box to make it tunable. Add the measurement s21 to the graph of the measured s21. Adjust the magnitude of s21 by using the button on the tuning window or with the value highlighted press the “Page/UP” and “Page/Down” keys. By clicking on the curve at 5 GHz, markers are displayed with the numerical values. The resulting plot (Figure 7) shows the adjusted lumped capacitance ($C_{\text{eff}} = 0.073$ pf) that matches the measurement at 5 GHz.

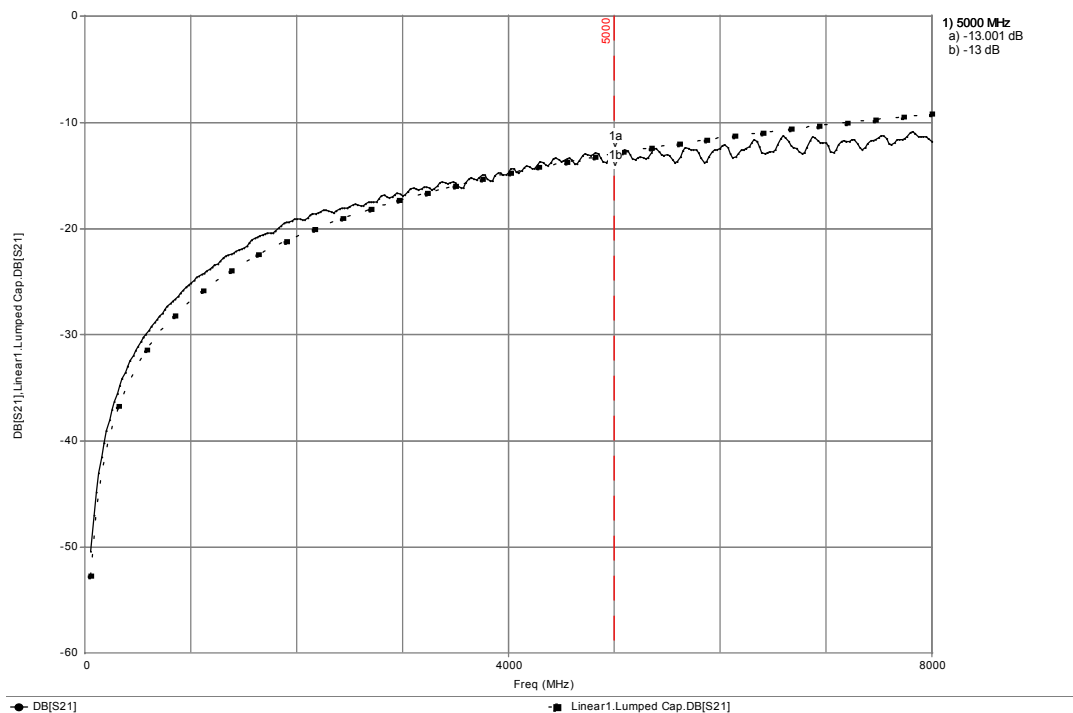
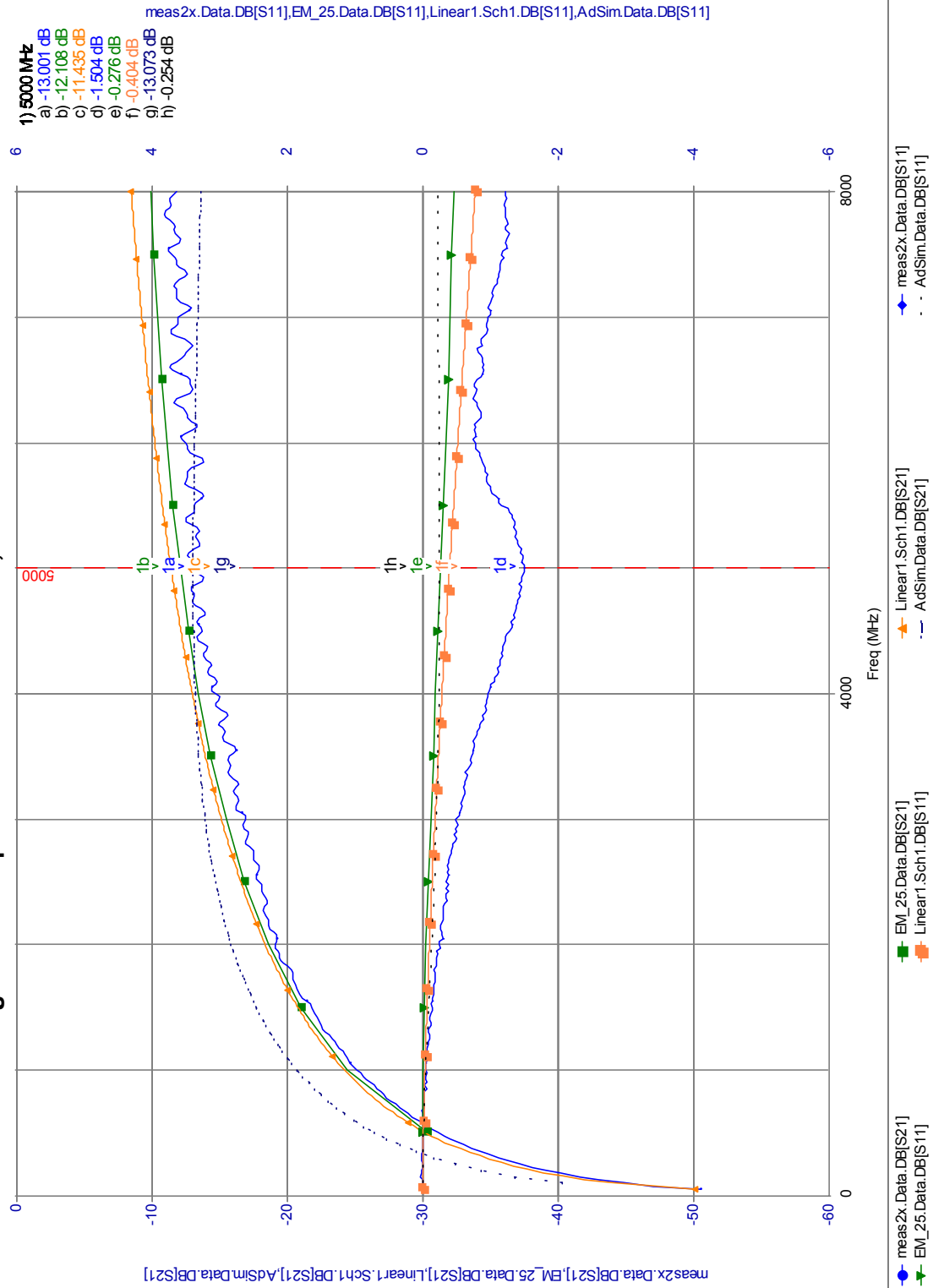


Figure 7 Computing Effective Capacitance Using GENESYS

Figure 6. Comparison of Linear model, EM and Measurements



Design Issues: As noticed from the test values, the amount of capacitance is very small. To obtain larger values, there are a number of design options. In general, these cause increases in the required board area. Increases in the number of fingers and length of fingers increase the width and length of the capacitor, respectively. The impacts of these design variations can readily be evaluated using linear models.

Consider the affect of increasing the finger length (L). GENESYS will readily generate a parameter sweep over the desired range. To set up a sweep, give the length parameter a variable name such as “L”. Under Equations, enter: $L=750$. Then select “Add Parameter Sweep” by right clicking on “Simulations/Data” on the “Workspace Tree”. Fill in the resulting dialog box with start value (40), stop value (160) and number of points (7). Add a graph of s21 using the sweep simulation data. The resulting plot (Figure 8) is shown below. Note the law of diminishing returns for larger lengths. As the length of the fingers increases, the frequency response deviates more from that of a lumped capacitor.

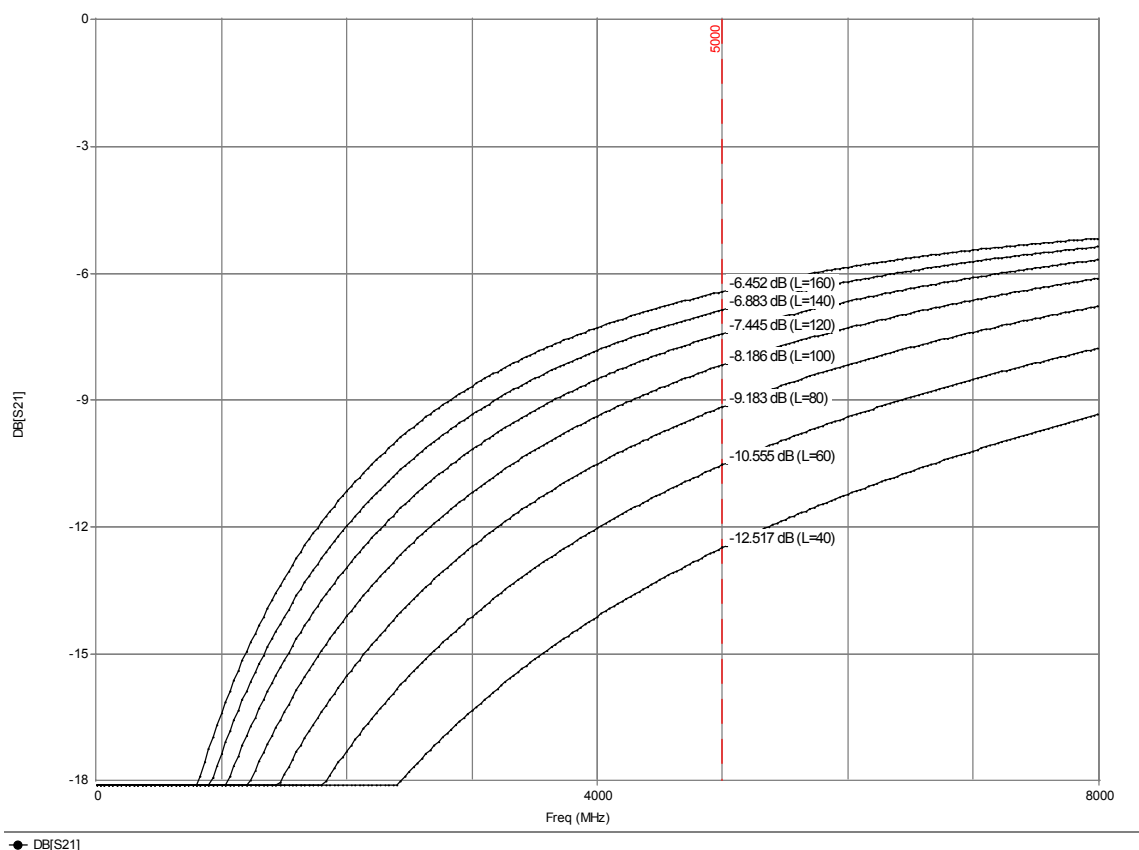


Figure 8. Parameter Sweep for Finger Lengths Between 40 – 160 mils.

GENESYS makes it easy to sweep a second parameter, such as width, on top of the original sweep. In the above example, consider that the chosen length is between 40 and 80 mils. To consider the sensitivity to finger widths in the range of 10 to 30 mils, a second sweep is added. The same procedure described above is used, with width (W) the swept variable and start value (10), stop value (30), and number of points (3). However, in this case the “Simulation to Sweep” is set to “Sweep 1”. This yields a family of curves (Figure 9) covering the ranges: $[10 < w < 30]$, $[40 < L < 80]$.

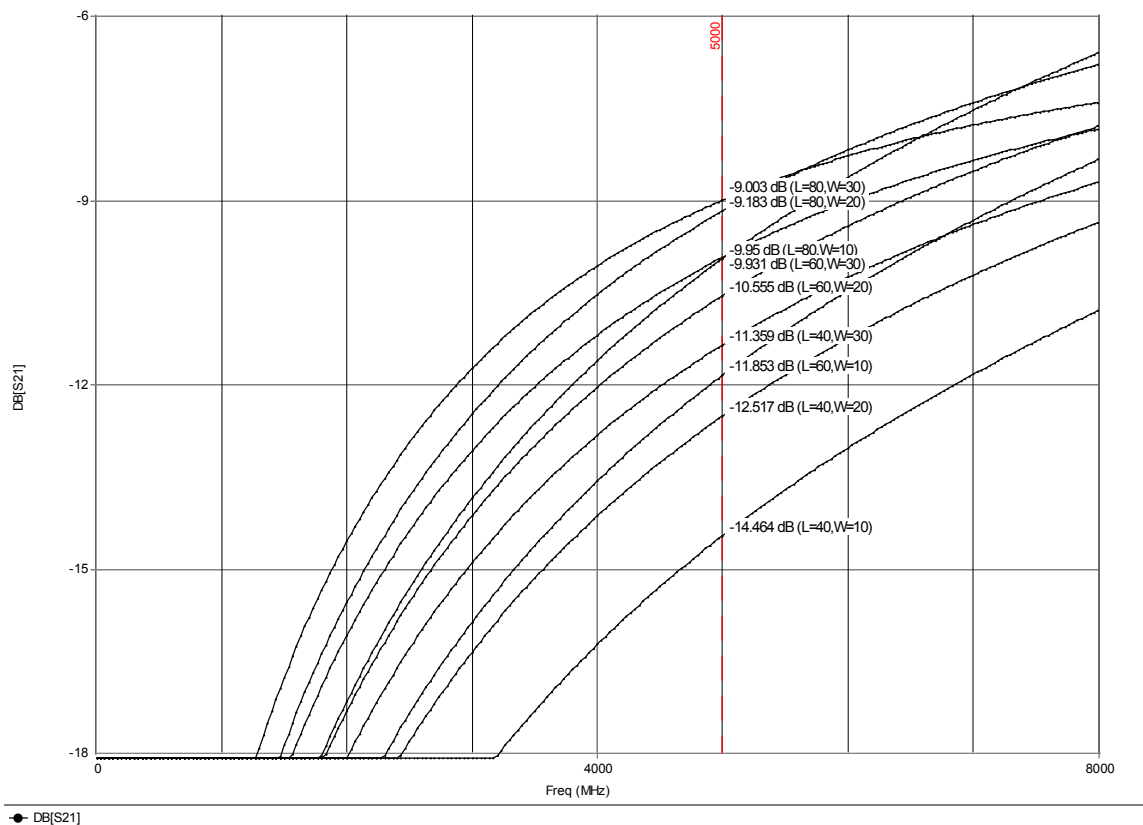


Figure 9. Sweep of Length and Width of Fingers

Plotting the effective capacitance at 5 GHz as a function of length (Figure 10) combines the data from the two sweeps. This graph can be useful in making design decisions. The optimization features of GENESYS can be used to establish a set of parameters to obtain the required response. In GENESYS 8.0, variables involved in the optimization can be constrained to specified ranges.

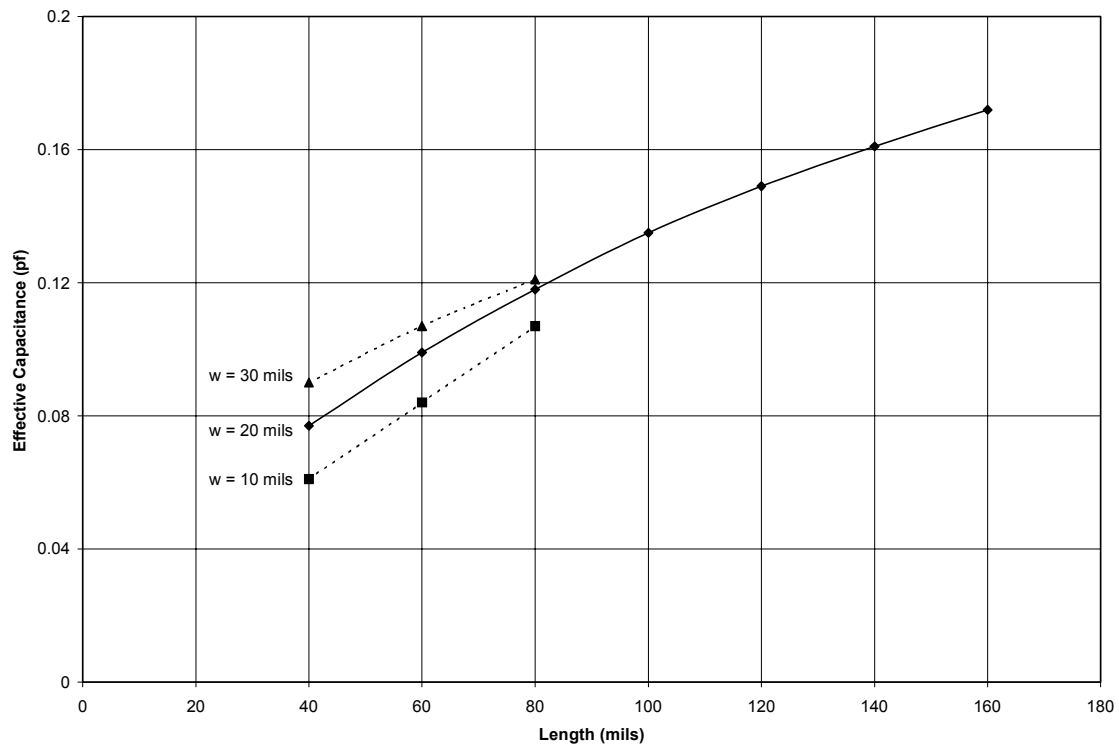


Figure 10. Effective Capacitance at 5 GHz as a Function of Length.

Conclusions: The new linear interdigital capacitor model demonstrates improved accuracy over earlier lumped element models. The s-parameters show reasonable agreement with electromagnetic simulations and hardware tests. The linear model is useful in design studies due to its speed and ease of changing parameters. This allows parameter sweeps and performance optimization in the GENESYS environment. To include cover effects and special geometries, the EM simulation is appropriate. It was also shown that the TEST LINK instrument interface can be used in confirming performance and validating models using hardware tests. A special thanks to Lance Lascari of Microwave Data Systems for providing the test data.

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