

A Temperature Stabilized CMOS VCO for Zero-IF Cellular CDMA Receivers

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Abstract

A fully integrated CMOS VCO which has low temperature and power supply sensitivity has been implemented in a 0.25 μm 4-metal 1-poly process. The causes of oscillation frequency drift over temperature have been investigated. By adjusting the reverse biasing voltage of junction diodes and the back-side voltage of linearized MOS varactors, less than 10 $\text{ppm}/^\circ\text{C}$ frequency drift has been achieved at 1.7GHz. Phase noise at 900kHz offset is less than -134dBc/Hz and varies less than 1dBc over $-30^\circ\text{C} \sim +90^\circ\text{C}$.

Key Words: VCO, frequency stability, linearized MOS varactor

Introduction

Frequency stability is an important issue in VCO design, this is especially true for full duplex system like CDMA receiver which receives signal continuously and can not be interrupted to re-calibrate the VCO discrete frequency control [1]. The minimum VCO continuous tuning range is set by the maximum frequency drift of the VCO, which has a trade-off for phase noise. Inside a cellular phone, the VCO frequency drift is most likely to be caused by the temperature or power supply variations. A VCO topology with low supply sensitivity has been presented before [2]. In this paper we present a fully integrated CMOS VCO with very low sensitivity to both temperature and supply variations, meeting the stringent phase noise requirement for Zero-IF CDMA receivers.

Causes of Oscillation Frequency Temperature Drift

In an LC tank oscillator, the oscillation frequency is determined by the inductance and the effective capacitance. Small variation of capacitance or inductance will change the frequency as $f \approx f_0 \left(1 - \frac{\delta_C}{2} - \frac{\delta_L}{2} \right)$ with $\delta_C = \Delta C / C_0$, $\delta_L = \Delta L / L_0$ and f_0 the center frequency. With a center frequency to be around 1.7GHz, a small percentage variation over temperature could result in large frequency drift. For a fully integrated VCO, the inductance of the on-chip inductor is mainly determined by the physical dimensions. Even though the inductor loss will increase at high temperature, inductance temperature variation is neglectable[3]. On the other hand, the effective capacitance in an integrated VCO can vary a lot over temperature, several contributors are identified in a typical cross-coupled CMOS VCO with discrete tuning. As shown in the shaded area of Fig 1, the drain-bulk junction diodes of transistors M1~M4 are in shunt connection with tank inductor. When a coarse tuning capacitor is turned off, the drain and source bulk diodes of the switch transistors (Md) are also in shunt with the inductor

through the MIM capacitors. Those reverse biased diodes present strong temperature dependency as

$$C_j(T) = \frac{C_j}{\sqrt[2]{V_D + \phi(T)}}, \text{ where } V_D \text{ the reverse biasing voltage,}$$

γ around 0.3~0.5 and $\phi(T)$ the junction potential which drops $2\text{mV}/^\circ\text{C}$. The temperature coefficient (TC) of the diode is $TC_D = \frac{\gamma}{1 + V_D / \phi} \cdot TC_\phi$ which is about $250 \sim 350 \text{ ppm}/^\circ\text{C}$

depending on the reverse biasing voltage. Temperature variation may also cause minor change of the relative permittivity of the dielectric, thus the MIM capacitor may show some temperature dependency. For the process we used, MIM capacitor has a TC_{MIM} of $20 \text{ ppm}/^\circ\text{C}$. The combined temperature coefficient for the tank capacitors will be

$$TC_{total} = \frac{C_D}{C_D + C_{mim}} \cdot TC_D + \frac{C_{mim}}{C_D + C_{mim}} \cdot TC_{mim}, \text{ which varies for}$$

different coarse tuning codes. Besides the variation caused by the components' temperature dependency, the non-linear behavior of the varactor may also generate temperature variation. As shown in Fig.2, the large signal swing across the varactor will generate an effective capacitance which is a function of the oscillation amplitude A_0 [4]. If A_0 is not well controlled over temperature, the effective capacitance will vary over temperature according to the following equation:

$$\frac{\partial C_{eff}}{\partial T} = - \frac{C_{max} - C_{min}}{A_0} \cdot \Delta V \cdot TC_{A_0}, \text{ with } \Delta V \text{ the DC bias voltage}$$

across the varactor and TC_{A_0} the amplitude temperature coefficient. Thus the C_{eff} variation has different polarity for positive and negative ΔV and making the compensation difficult.

Compensating Frequency Drift

With all the above effects combined, a 1.7GHz CMOS VCO can easily drift tens of MHz from -30°C to 90°C , which may cause the PLL out of lock if the continuous tuning range of the VCO is not wide enough. Circuit techniques should be employed to minimize that frequency drift without modifying the tuning voltage. To compensate the junction capacitance variation of the switching transistors Md, a voltage source with $+2\text{mV}/^\circ\text{C}$ increase can be used to reverse bias those diodes compensating the junction voltage drop. Fig.3 shows that the capacitance variation is one order lower by using this technique. To further compensate the junction diodes of M1~M4 of Fig.1 and MIM capacitor variations, the back-side bias voltage of the NMOS varactor can be varied over temperature to generate an offset capacitance canceling the drift. This is shown conceptually in Fig.4 that by increasing the back-side bias voltage V_{CM} over temperature,

the varactor capacitance is decreased by ΔC without changing the tuning voltage V_f . Note the varactor is coupled through MIM capacitor to the VCO tank so that the voltage swing across the varactor is small enough to neglect the non-linear averaging effect. For a varactor that has steep variation, the offset capacitance for temperature compensation ΔC_1 varies with different tuning voltage as shown in Fig.5. This is undesirable because the compensation would then highly dependent on the tuning voltage. As such, one more pair of varactors is added in parallel and the back-side is biased at shifted voltage V_{CM2} . The offset capacitance ΔC_2 is now averaged over the ranged from $V_{CM1} \sim V_{CM2}$, a relative constant compensation can thus be achieved over wider tuning voltage range.

Circuit Implementation

The above compensation approaches have been explored in a fully integrated CMOS VCO for CDMA receiver as shown in Fig.6. The oscillator topology is stacked diff-pairs with regulator explained in [2]. The regulating amplifier is a telescopic OTA for its high GBW and low noise. Note the regulator reference voltage is generated from a replica NFET M6 and its noise is attenuated by a first-order RC filter(R1 & C2). Similarly, to reduce the noise at the varactor back-side biasing node, RC filter is employed which has low pole around several kHz. To avoid this low pole frequency interfering with the PLL loop filter, low-noise voltage followers are employed to present low impedance at the common nodes of the varactor pairs. The bias voltages are set at 0.9V and 1.9V at room temperature with their TC adjustable. This adjustment is done by changing the temperature coefficient of resistor R2 in the PTAT circuit, where R2 is made of an array of composite resistors. Inside each composite resistor, it is a series connection of two resistors which have positive and negative TC . Changing the percentage of the two resistors can generate different TC . The inverter supply voltage for coarse tuning transistor is set

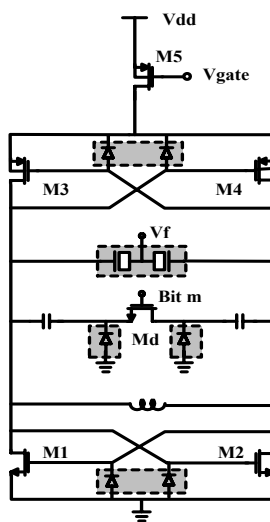


Fig. 1 Contributors of VCO frequency temperature drift

to 2V and has a $TC = 1000 \text{ ppm}/^\circ\text{C}$ which can compensate the junction voltage drop.

Measurements

The VCO is implemented in a $0.25 \mu\text{m}$ 4-metal 1-poly CMOS process and packaged in a 32-pin QFN. As shown in Fig.7, without any temperature compensation, the frequency drops more than 16MHz(@ 1.7GHz) when temperature varies from -30°C to $+90^\circ\text{C}$. By turning on the positive TC biasing voltages, the frequency drift is lower than 2MHz over 0.6~1.8V fine tune range which corresponding to an equivalent TC of less than $10 \text{ ppm}/^\circ\text{C}$. Phase noise measurement in Fig.8 shows the phase noise decreases at a rate of $1/f^2$ below 4.5kHz and continues at a rate of $1/f^4$ till 200kHz where back to $1/f^2$ again. This is caused by the dominating noise up-conversion of the first-order filter shaped noise. Phase noise variation over temperature is less than 1dB due to the PTAT nature of the VCO biasing current. The VCO can be tuned to cover 1.55GHz~1.95GHz through 6 discrete tuning branches with less than 100kHz/V power supply sensitivity. The die microphotograph is shown in Fig.10, the power consumption is 6.5mA from 2.5V including biasing circuit.

Reference

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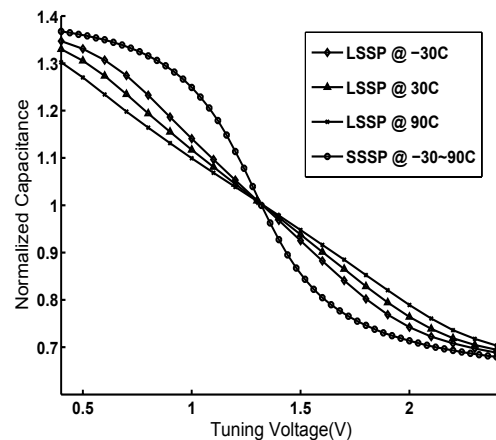


Fig.2 MOS varactors over temperature, note the Large-Signal-S-Parameter(LSSP) effective capacitance varies with temperature while Small-Signal-S-Parameter(SSSP) shows invisible temperature dependency

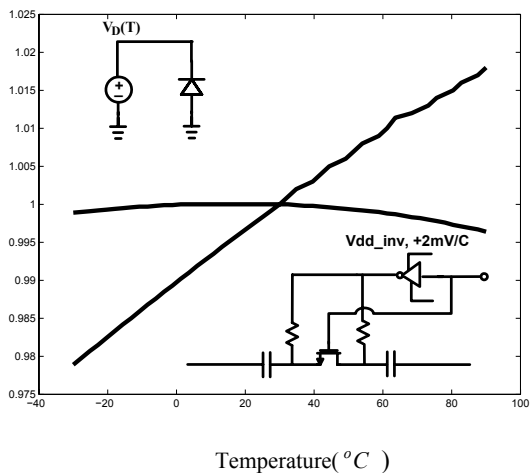


Fig.3 Normalized junction capacitance $C(T)/C_0$ over temperature (w/o compensation and with compensation)

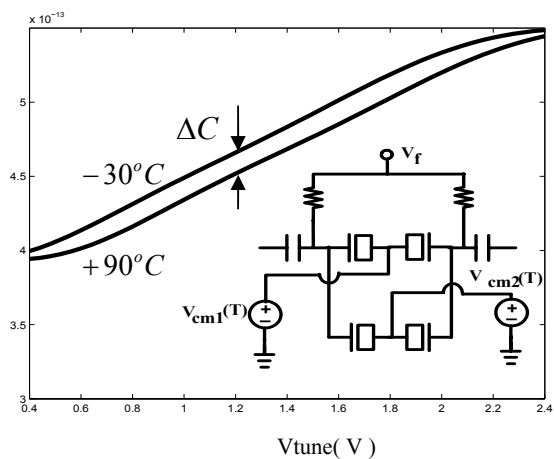


Fig.4 Linearized MOS varactor temperature compensation using back-side bias

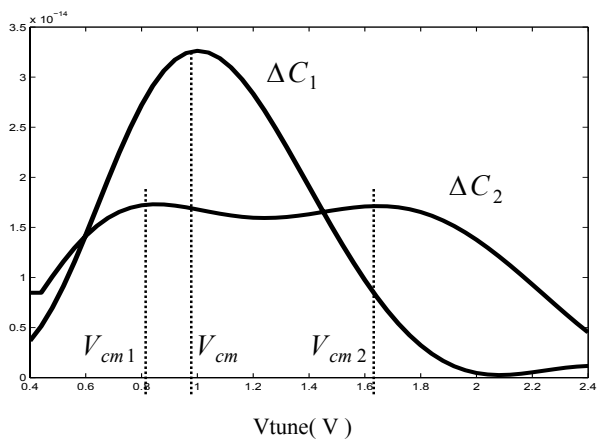
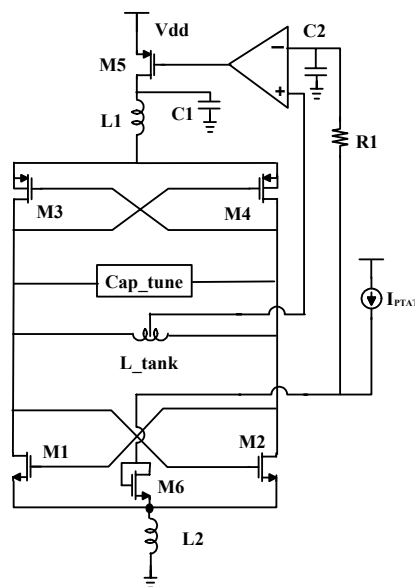
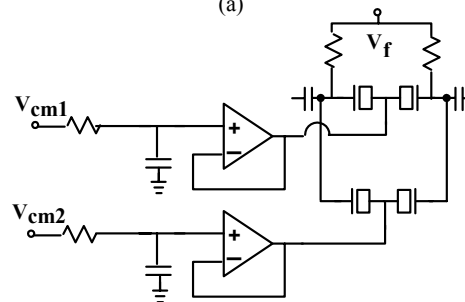


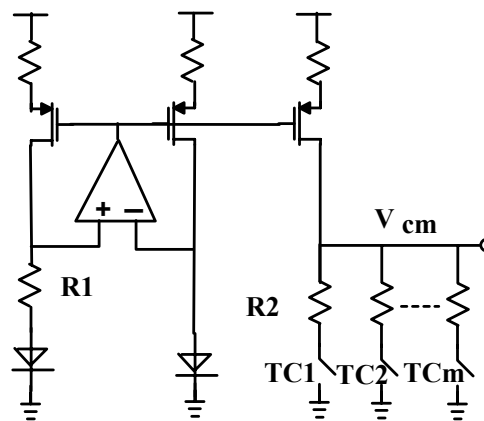
Fig.5 Compensating capacitance w/o linearization (ΔC_1) and with linearization (ΔC_2)



(a)



(b)



(c)

Fig. 6 Circuit implementation (a) VCO core with regulated power supply (b) MOS varactor back-side bias compensation (c) Bias circuit for different temperature coefficients

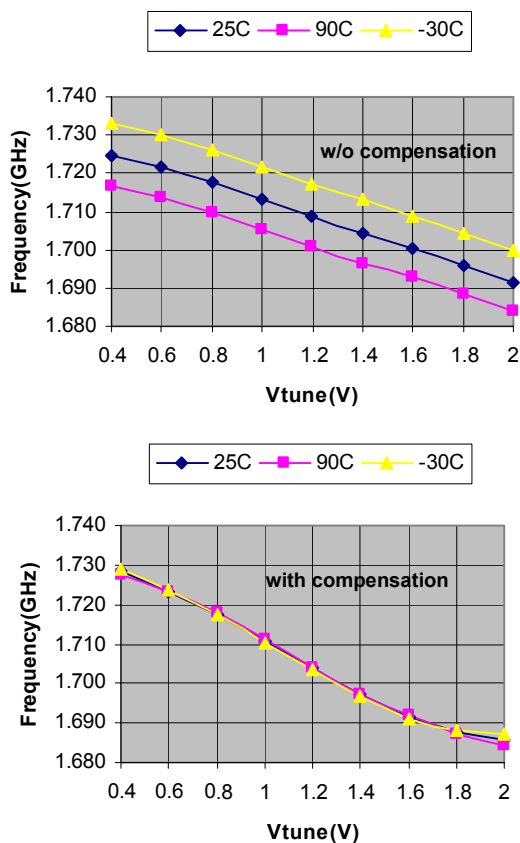


Fig. 7 Temperature drift measurement of VCO oscillation frequency before and after temperature compensation

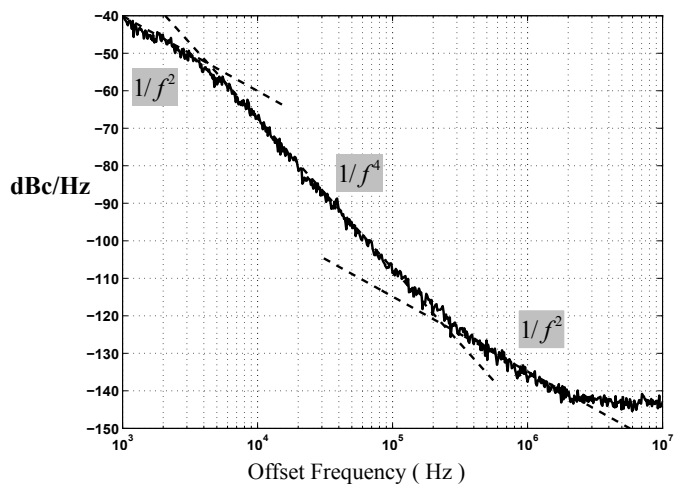


Fig. 8 VCO Phase noise at 1.7GHz. Note the slope of the PN curve caused by the RC filter

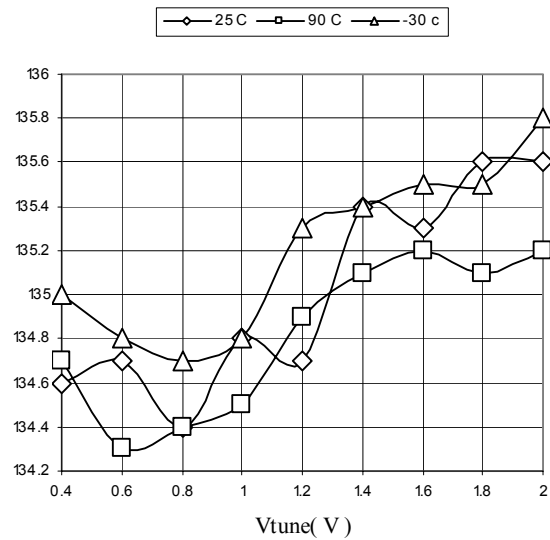


Fig. 9 Phase noise variation at 900kHz offset over fine tune voltage at different temperature

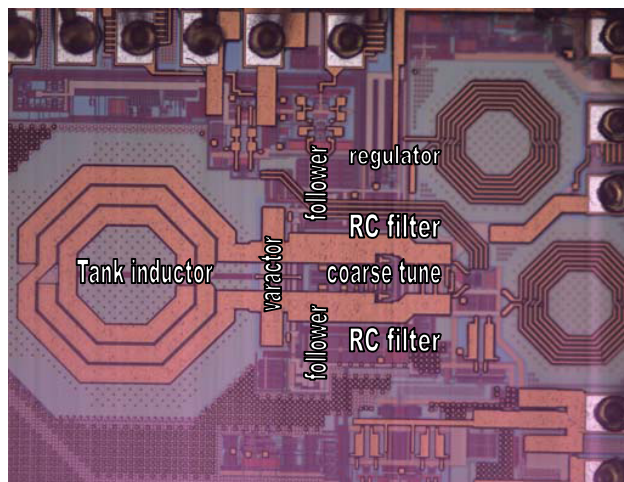


Fig. 10 Microphotograph of temperature stabilized CMOS VCO