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An Ultra Compact Differentially Tuned 6 GHz CMOS LC VCO with Dynamic Common-Mode Feedback

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I. ABSTRACT

A fully integrated 0.024mm^2 differentially tuned 6GHz LC VCO for 6+Gbps high speed serial (HSS) links in a 90nm bulk CMOS is presented. It is smaller than any LC-VCO reported to date at this frequency. Its size is comparable with ring oscillators but it has significantly better phase noise. A circuit technique is introduced to dynamically set the common-mode (CM) voltage of the differential varactor control signals equal to the VCO's CM. Using a differential control a very wide tuning range from 4.5GHz to 7.1GHz (45%) is achieved. The VCO has a measured phase noise of -117.7dBc/Hz at a 3MHz offset from a 5.63GHz carrier while dissipating 14mW from a 1.6V supply.

II. INTRODUCTION

Continuous CMOS technology scaling enables increased complexity and operating speeds in integrated circuits. As a result, the on-chip data processing capability of integrated systems is growing very quickly and high data-rate inter-chip I/Os become a necessity on advanced communications and data processing ICs. Electrical HSS links have become the preferred solution for short distance interconnects because of their lower cost and easier manufacturability compared to optical links. There is a growing need to make fast (6+Gbps and beyond) but very compact HSS links. Due to the larger number of I/Os required per chip, small size is the primary design target. The I/Os are further targeted at non-portable applications so that power consumption is a somewhat lesser concern. PLLs using widely tuneable VCOs are key components of the HSS I/Os [1]. Ring oscillators are very small but their high phase noise results in excessive timing jitter. LC-VCOs have superior phase noise but their on-chip spiral inductors occupy a large area. We show that a substantial reduction in the size of inductors for LC-VCO in advanced CMOS processes is possible for HSS link applications. Smaller inductors are compatible with wide tuning range requirements but result in a power consumption increase to guarantee oscillator startup and phase noise. However, the resulting ultra compact LC-VCO, while occupying an area comparable to a ring oscillator, still offers substantial lower phase noise and lower power consumption compared to ring oscillators.

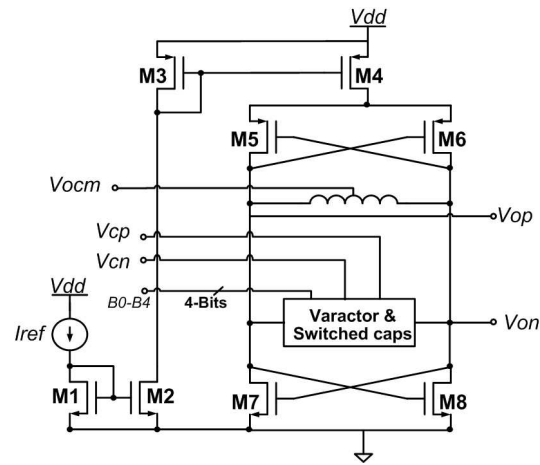


Fig. 1. (a) Schematic of the differentially tuned 6 GHz LC-VCO where the inductor's center tap is used to dynamically set the common-mode of the differential tuning signals.

Fig. 1 shows the schematic of the presented ultra compact VCO where a top-biased complementary CMOS topology is used to improve PSRR. M5-M8 are the negative resistance active devices. Two current mirrors (M1-M4) generate the bias current from a small I_{ref} . The tank (Fig. 2) consists of a differential inductor, digitally controlled switched capacitors, and a differentially controlled varactor. The coarse and fine oscillation frequency tuning is set by a four bit digital (B0-B3) control and by an analog differential tuning control (V_{cp} and V_{cn}). Moreover, a circuit technique employing a differential inductor's center tap is introduced that is compatible with the differential tuning common-mode feedback.

III. COMPACT AND WIDE TUNING RANGE VCO DESIGN

Designing an ultra compact LC VCO with wide tuning range is complex and requires a multi-dimensional optimization. Using a 90nm CMOS technology offers fast MOS devices with low parasitics but the gain and noise of the devices are compromised due to shorter channel lengths [2]. Specifically VCO design directly suffers from higher white and flicker noise in the devices. Also, using lower gain devices dictates higher power dissipation to sustain minimum loop gain.

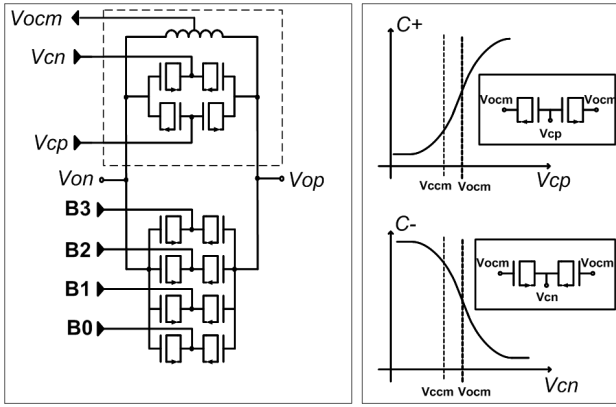


Fig. 2. The differentially tuned LC tank with common-mode feedback. V_{cp} and V_{cn} are differential tuning control signals where $V_{ccm} = (V_{cp} + V_{cn})/2$ is their common-mode. The LC VCO outputs are V_{op} and V_{on} where the common-mode is $V_{ocm} = (V_{op} + V_{on})/2$.

In first order, the inductance, L , of a planar inductor, is proportional to $A_{ind}^{3/2}$ and its quality factor, Q_L , is proportional to $\sqrt{A_{ind}}$ where A_{ind} is the inductor's area so that L and Q_L decrease significantly when reducing the inductor's area [3]. In a compact and wide tuning range design, the acceptable range of the inductance shrinks considerably because a large enough inductance is required to maintain the minimum tank impedance, whereas increasing the inductance limits the tuning range and can translate to a large size spiral inductor. On the other hand, inductor's self resonance frequency and its parasitics are other important characteristics that must be considered in the whole VCO design process. Design and analysis of integrated inductors is complex and involves EM simulations, but we find the approximate equations presented in [4] very useful in the early design stages. We started with a very small size differential octagonal spiral inductor, i.e. $90\mu m \times 90\mu m$ for our VCO, and optimized the dimensions to get the highest possible L and Q_L . A relatively large N , the number of turns, is chosen ($N=4$) to improve L as it is directly proportional to N . Metal layers 6 and 7 in a 7-level copper metal stack are shunted to decrease the series resistance and increase Q_L . The metals width and the lateral spacing between them are optimized to improve L and Q_L and achieve an acceptable parasitic capacitance and a high enough self-resonance frequency simultaneously. The designed inductor occupies $90 \times 90 \mu m^2$ and has simulated inductance of $0.9nH$ and a Q_L of 11.5 at 6 GHz.

To achieve a wide tuning range while keeping the VCO tuning gain low, a large number of digitally controlled switched capacitors are used to divide the tuning range into multiple low gain frequency bands. In the used technology, Accumulation Mode NMOS varactors (AMOS) are the only choice available for implementing the switched tank capacitors. Their quality factor, Q_{ncap} , is relatively low. The AMOS varactors of the tank at the lower band show a minimum simulated $Q_{ncap} = 9.7$. The low Q_L resulting from using a small size inductor, the

low Q_{ncap} and the small tank inductance to tank capacitance ratio result in a small equivalent tank impedance at resonance. However, to compensate the low tank impedance to achieve sufficient loop and start-up gain, the size of the active devices cannot be simply increased because all parasitic capacitances from the active devices, inductors, and loads contribute in the tank capacitance and limit the minimum tank capacitance and consequently the maximum oscillation frequency. As the transistors' transconductance and parasitic capacitances increase simultaneously with increasing the device size, this places another challenge on the VCO design. Therefore, the active devices (M5-M8) have to be biased for a high f_T which incurs a power penalty but allows a large g_m in combination with low device parasitics to avoid frequency reductions.

The optimization process was iterative and involved multi-dimensional trade offs which were complemented by extensive simulations especially for different process corners and different operating conditions.

IV. COMMON-MODE FEEDBACK FOR DIFFERENTIAL TUNING

PLLs for communication systems typically use differential building blocks to reduce the effect of supply or substrate interference, however, a differential LC VCO with single-ended frequency tuning is often employed and an active differential-to-single-ended converter is placed after a differential charge pump to convert its output to a single-ended tune voltage [1]. Using a differentially controlled VCO eliminates the need for the noisy active differential-to-single-ended converter and also minimizes the impact of common-mode noise [5]. Differential tuning further offers better tuning linearity compared to a single-ended tuned VCO with a differential-to-single ended converter because the gain of any active converter reduces at the extreme ends of the tuning voltage which can cause locking problems in a PLL.

In a differentially tuned LC VCO, it is crucial to accurately set the common-mode (V_{ccm}) of the differential tune signals (V_{cp} and V_{cn}). If V_{ccm} is not accurately set equal to the common-mode of the VCO's output (V_{ocm}), the differential tuning characteristic of the varactor becomes asymmetrical and its dynamic range also degrades (Fig. 2). Most of LC VCOs used in modern equipment use a digitally controlled coarse tuning scheme to cover a large tuning range with multiple overlapping tune curves to reduce the VCO's gain to a level compatible to the PLL requirements; this also reduces the AM-to-FM noise conversion in the VCO. When placed in a PLL, a multiband VCO mostly operates in the middle of each tuning curve, which is less prone to the locking problems. However, these operating range shift towards the extreme ends of the tuning curves if $V_{ccm} \neq V_{ocm}$ (Fig. 3). In this case, the differential tuning characteristic becomes asymmetrical which has two major drawbacks. First, the differential tuning characteristic is not efficiently used and we lose some of the dynamic range. This creates either locking problems in a PLL because the VCO quickly enters the flatter part of the tuning characteristic by increasing $V_{tune} = V_{cp} - V_{cn}$, or a fatal

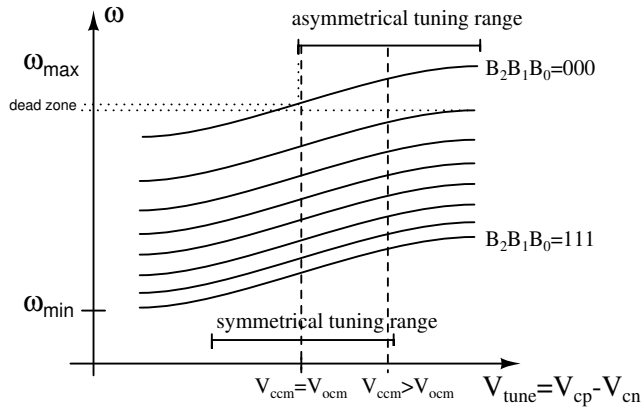


Fig. 3. Conceptual diagram of symmetrical and asymmetrical tuning characteristic in a differentially tuned LC VCO depending on the difference between V_{ccm} and V_{ocr} .

frequency dead zone at the worst case, which can be due to process variations or changes in the operating condition. Second, the asymmetrical tuning characteristic can increase the AM-to-FM noise conversion in the VCO. It is known that amplitude noise converts to FM noise if the oscillation frequency varies with the oscillation amplitude. In the widely used LC VCO topologies, the tuning varactors sit across the differential outputs and experience the excursions of the output voltage, which modulates their capacitance and creates an amplitude dependent oscillation frequency characteristic [6]. In this case, an effective capacitance determines the oscillation frequency. If the differential output voltage sweeps across a symmetrical varactors characteristic, the dependence of the frequency on the amplitude and consequently AM-to-FM noise conversion becomes negligible. Whereas, for an asymmetrical tuning characteristic the slope of the effective capacitance versus oscillation amplitude increases and enhances AM-to-FM noise conversion in the VCO [6].

Usually a replica biasing circuit is used to set the common-mode voltage of the differential tuning control signals generated by a charge pump, but this technique has two drawbacks. First, it dissipates excess power which is not desired in low power applications. Second, this technique replicates the VCO's common-mode voltage when the VCO is at *rest* and does not oscillate. It is known that in some of the widely used LC VCO topologies, e.g., complementary CMOS, the common-mode voltage at the VCO's outputs shifts to a different value when the circuit oscillates [7]. Therefore, in most of the LC VCO topologies, there is an inherent systematic error between the common-mode voltage of the differential control signals (V_{ccm}) and the VCO's common-mode voltage V_{ocr} , if a replica biasing scheme is used to set the common-mode of the charge pump's differential outputs. Moreover, the replica biasing relies on excellent matching between the active devices in the LC VCO and their counterparts in the replica biasing circuit, so any mismatch is another source of error in this method although less profound comparing to the already discussed error.

Using a differential inductor instead of two single-ended inductors is very common in differential LC VCOs because of their compact layout and also a better differential characteristic. In the proposed topology, we use the center tap node of the differential inductor, which is a virtual AC ground and its DC value is equal to the common-mode of the VCO's outputs, to *dynamically* detect the common-mode voltage at the VCO's differential outputs (V_{ocr}) and use it as a common-mode feedback signal to accurately set $V_{ccm} = V_{ocr}$ in the charge pump. Comparing to the replica biasing solution, the accuracy of the proposed technique is excellent and there is no error in detecting V_{ocr} . Furthermore, this technique does not use any extra active device and does not dissipate any power. Fig. 4 shows the block diagram of a differential PLL with the proposed common-mode feedback.

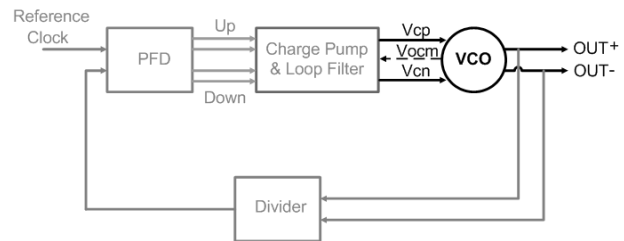


Fig. 4. Block diagram to show how the presented VCO is used in a PLL

V. EXPERIMENTAL RESULTS

The circuit is fabricated in 90nm bulk CMOS process. Fig. 5 shows the measured tuning curves. The entire range from 4.5GHz to 7.1GHz is covered by 12 overlapping bands selected by the 4-bits control bus. The VCO has 1.1GHz wider tuning range compared to a state-of-art VCO for the same application in [1]. At a 3MHz offset from 5.63GHz carrier the phase noise is -117.7dBc/Hz while the core VCO dissipates 14 mW from a 1.6V supply. We can trade tuning range or phase noise with power dissipation if necessary, e.g., the measured phase noise at 3MHz offset is -115.2dBc/Hz from a 6.4GHz carrier when the VCO dissipates 7.5mW from a 1.2V supply. In this low power mode, the VCO has a 20% tuning range from 5.72GHz to 7.02GHz.

Fig. 6 shows the die photograph of the 90nm bulk CMOS VCO which occupies $170 \times 140 \mu m^2$. An RF pad on the same die occupies $120 \times 100 \mu m^2$ which is a good reference point to illustrate the compactness of the presented VCO. The comparison of the VCO performance with other VCOs in the 4-6 GHz range in table I illustrates that the presented VCO has a very large tuning range and is extremely compact; it is about 10, 5, 20, and 100 times smaller than the reported LC-VCOs in [5], [8], [9], and [10], respectively. In comparison with the ring oscillator in [11], the presented VCO has a comparable size but more than 20 dB better phase noise, 5.7 times less power dissipation, and 10% more tuning range. Also its power dissipation is comparable with the VCOs for wireless applications in [9], [12] while maintaining larger

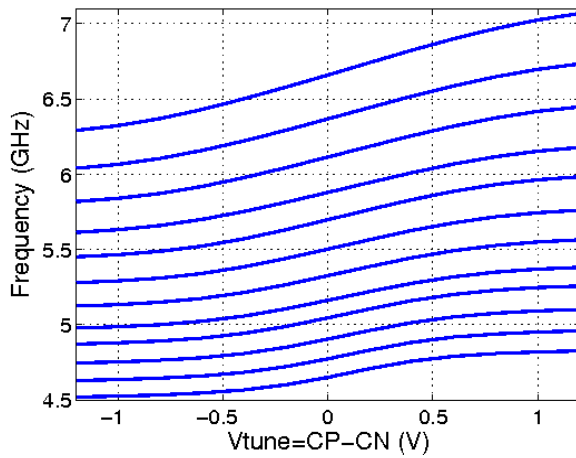


Fig. 5. Measured VCO tuning curves

TABLE I
COMPARISON OF STATE OF THE ART VCOs IN 4-6GHz RANGE

Ref.	f_0 (GHz)	Pdd (mW)	TR (%)	PN@1MHz (dBc/Hz)	Size (mm^2)	Tech. μm
[5]	4.4	2.7	40	-117.8	0.3	0.13-SOI
[8]	5.0	3.0	8.3	-120.4	0.107 ^a	0.18-CMOS
[9]	4.4	21.6	13	-119	0.5	0.5-BiCMOS
[10]	5.0	100	39	-115	4.0	0.5-SiGe
[12]	5	13.75	18	-115	NA	0.25-CMOS
[11] ^b	5	80	35	-85	0.03 ^a	0.18-CMOS
This	5.63	14	45	-108.5	0.024	0.09-CMOS

^aarea estimate from die photograph

^bRing VCO

tuning range and trading 6-10dB of the phase noise. The lower phase noise is attributed to the substantially smaller inductor, AM-to-FM noise conversion in AMOS varactors, large and low Q capacitance, and inferior devices from noise and gain perspectives.

VI. CONCLUSIONS

An ultra compact fully integrated 6 GHz LC VCO for high speed serial link (HSS) applications in 90nm bulk CMOS is presented which occupies $0.024mm^2$. Its size is comparable with ring oscillators but it has substantially better phase noise and lower power dissipation. Also it is at least 5x smaller than any LC-VCO reported to date at this frequency. Using a differential control a very wide tuning range from 4.5GHz to 7.1GHz (45%) is achieved. A circuit technique employing a differential inductor's center tap is presented to accurately set the common-mode of the differential tune signals equal to the common-mode of the VCO's output. Comparing to the commonly used replica biasing, the presented method dynamically detects the common-mode of the VCO's output and is very accurate and does not dissipate extra power.

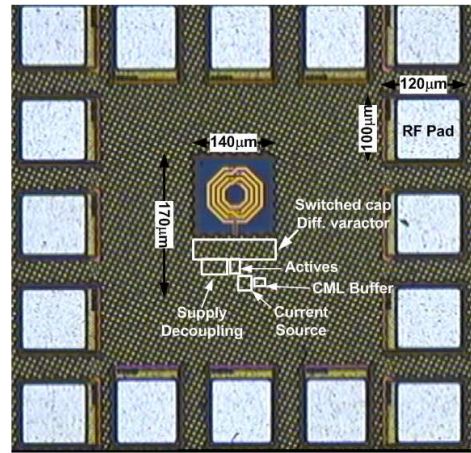


Fig. 6. Die photograph of the VCO test site fabricated in 90nm bulk CMOS; the active and tuning components are covered by metal fills and not visible, but the occupied area is highlighted.

ACKNOWLEDGEMENT

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