UNIVERSITÄT DER BUNDESWEHR MÜNCHEN
Fakultät für Elektrotechnik und Informationstechnik

VARACTORS AND INDUCTORS FOR INTEGRATED RF CIRCUITS IN STANDARD MOS TECHNOLOGIES

Dipl.-Phys. (Univ.) Judith Maget

Vorsitzender des Promotionsausschusses:	Prof. Dr.-Ing. habil. H. Lindenmeier
1. Berichterstatter:	Prof. Dr.-Ing. K. Hoffmann
2. Berichterstatter:	Prof. Dr.-Ing. U. Barabas

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*intgrated, variable capacitor

*integrated circuit with a varactor

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List of symbols

Symbol	Meaning	Unit
AC	alternating current	
A-mode	accumulation mode	
BiCMOS	bipolar and CMOS	
CMOS	complementary MOS	
DC	direct current	
GSG	ground signal ground	
I-mode	inversion mode	
Im	imaginary part	
LDD	lightly doped drain	
MOS	metal oxide semiconductor	
NMOS	n-type MOS	
PMOS	p-type MOS	
Re	real part	
STI	shallow trench isolation	
VCO	voltage-controlled oscillator	
A_g	gate area	m^2
$A_{1,2,3}$	area parameters for calculation of well resistance	m^2
C	capacitance	F
C'	effective capacitance due to parasitic inductances	F
$c_{1,2,3}$	current constriction parameters	1
C_{av}	averaged capacitance	F
$C_{av,max}$	maximum averaged varactor capacitance	F
$C_{av,min}$	minimum averaged varactor capacitance	F
$C_{av,ratio}$	averaged capacitance tuning range	1

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Symbol	Meaning	Unit
C_f	fringing capacitance in varactors	F
C_f	input to output capacitance of inductor	F
$C_{f,fix}$	fixed fringing capacitance	F
$C_{f,var}$	variable fringing capacitance	F
C_d	depletion capacitance	F
C_{jd}, C_{pn}	junction capacitance	F
C_{max}	maximum varactor capacitance	F
C_{min}	minimum varactor capacitance	F
C_o	overlap capacitance	F
C_{ox}	gate oxide capacitance of varactor	F
C_{ox}	parasitic oxide capacitance of inductor	F
C_p	parasitic capacitance	F
C_{pC}	parasitic capacitances of the VCO circuit	F
C_{ratio}	capacitance tuning range	1
C_v	variable capacitance	F
$C_{var,max}$	maximum variable varactor capacitance	F
$C_{var,min}$	minimum variable varactor capacitance	F
$\delta_{a,d}$	smoothing parameter for effective voltage calculation in accumulation, depletion	V
Δf	frequency offset	Hz
ϵ_0	permittivity of vacuum	F/m
ϵ_{ox}	dielectric constant of silicon dioxide	1
ϵ_{si}	dielectric constant of silicon	1
f	frequency	Hz
F	excess noise factor	Hz
f_0	center frequency of the VCO	GHz
f_{i1}	frequency limit for thermal generation of charge	Hz
	carriers	Hz
f_{i2}	frequency at which NQS effects become important in the I-mode devices	Hz
f_{ratio}	frequency tuning range	1
f_{res}	resonance frequency	Hz
Δf_{3dB}	3dB-bandwidth	Hz
FOM	figure of merit	dBc/Hz
$\mathcal{L}$	phase noise	dBc/Hz
k	Boltzmann's constant	J/K

Symbol	Meaning	Unit
K_{Vdd}	sensitivity of VCO frequency to variations in V_{dd}	Hz/V
K_{VCO}	sensitivity of VCO frequency to variations in V_{tune}	Hz/V
L	inductance	H
$l_{av,1,1a}$	length parameters for calculation of well resistance	m
$l_{1b,2,3}$		m
l_f	finger length	m
l_g	gate length	m
L_p	parasitic inductance	H
μ_0	permeability of vacuum	Vs/(Am)
$\mu_{1,2,3}$	mobility parameters for calculation of well resistance	m^2/Vs
N_F	number of fingers	1
Φ_s	surface potential	V
P_{loss}	power consumption	W
P_{sig}	signal power	W
q	elementary charge	C
Q	quality factor	1
Q_{acc}	charge in accumulation layer	C
Q_{av}	averaged quality factor	1
$Q_{av,min}$	minimum averaged quality factor	1
Q_{BW}	quality factor according to bandwidth definition	1
Q_{dep}	charge in depletion layer	C
Q_g	charge at gate node	C
Q_{LC}	quality factor of LC-tank	C
Q_{min}	minimum quality factor	1
Q_{PS}	quality factor according to phase stability definition	1
R_s	series resistance	Ω
R_{inv}	resistance of the inversion layer	Ω
R_{acc}	resistance of the accumulation layer	Ω
R_{gate},R_g	gate resistance	Ω
R_p	parasitic resistance	Ω
$R_{p1,2}$	resistances in the p^- bulk	Ω
$R_\square$	resistance per square	Ω/□
R_{sub}	substrate resistance	Ω
R_v	variable resistance	Ω
$R_{w,1,2,3}$	well resistances	Ω
T	temperature	K

Symbol	Meaning	Unit
τ	life time of charge carriers	s
t_{ox}	gate oxide thickness	m
V_{dd}	supply voltage	V
V_{eff}	effective voltage across gate oxide and depletion region	V
$V_{eff,a,d}$	effective voltages for accumulation, depletion	V
V_{FB}	flatband voltage	V
V_{gate}	gate voltage	V
V'_{gate}	gate voltage at node of variable capacitance	V
V_{th}	threshold voltage	V
V_{tune}	tuning voltage	V
V'_{tune}	well voltage at node of variable capacitance	V
V_{well}	well voltage	V
w_f	finger width	m
w_d	width of depletion region	m
w_g	gate width	m

Chapter 1

Introduction

The popularity of mobile telephones attracted exceptional attention to wireless architectures and circuit techniques in the last few years. Simultaneously the scaling of complementary metal-oxide-semiconductor (CMOS) technologies in the last decade resulted in strong improvements of the radio-frequency (RF) performance of MOS devices. This made it possible to serve the ever-increasing demand for lower cost and higher integration in the important mobile communications market.

The design of single-chip transceivers has already been demonstrated in low-cost CMOS technologies [1]-[11] and now RF CMOS integrated circuits (ICs) have advanced far enough to be at the threshold of commercial deployment. One of the key elements of the important transceivers for wireless communications are voltage-controlled oscillators (VCOs). They are part of the frequency synthesizer to generate the local oscillator (LO) signal for both, upconversion from and downconversion to the baseband signal. For monolithic integration in CMOS inductance-capacitance (LC) tank oscillators are preferred over ring oscillators due to better relative phase noise performance [30] and the necessity of low power consumption (battery operated systems). The interest in fully integrated LC-tank CMOS VCO's for RF systems is demonstrated by the large number of publications in the last few years [12] - [21].

Despite the continuous improvement VCOs still remain the bottle neck and

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thus the main challenge of RF transceivers. This is due to the most important and demanding parameters of a VCO: phase noise, power consumption and frequency tuning range. In LC-tank VCO's phase noise and power consumption depend primarily on the quality factor of the tank and the nonlinearities of the varactors. Also the frequency tuning range is determined by the capacitance tuning range of the varactor and parasitics in the VCO. Thus a main task is to optimize the performance of inductors and varactors.

Bond wires and integrated spiral inductors are available as inductive elements. Bond wires offer high quality factors (>50) but have large spreads ($> \pm 20\%$). Often non standard wire length or die-to-die bonding is required and it is questionable if this approach can be regarded as standard. Integrated spiral inductors, instead, feature less spread, but suffer from much lower quality factors in standard digital CMOS processes (low-resistivity substrates, thin metals). A great effort has been undertaken to increase the quality factor by reducing the losses in spiral inductors [21],[22]-[29]. However many solutions are non-standard CMOS and still, in most cases the inductor limits e.g. the phase noise performance of fully integrated VCOs.
The switched capacitor concept offers wide tuning ranges at possibly high tank quality factors [47] but increases circuit complexity.
Single device varactors are readily realized as junction diodes, but in CMOS technologies only source/drain to well junctions are available. Quality factors are quite high but the tuning ranges nearly unacceptable low. The approach of differential operation increases the quality factor but leaves the tuning range still below 2 [44]. Down-scaling of the supply voltage aggravates this tuning problem [46].
More promising is the approach of tuning with the voltage-controlled gate capacitance of the MOS structure [19]. Quality factors are generally high and tuning ranges well above 2 possible [44]. Strong capacitance variation within a few hundreds of millivolts makes the MOS devices feasible for low-power supply voltages.
However, low-power, low-phase noise VCO design calls for even higher tuning ranges. VCO parasitics deteriorate the effective tuning capabilities of varactors. Process variations in the capacitor itself (up to 15% [45]) and in the inductors (5% to above 20%) need to be compensated. Therefore highly tunable varactors are required to guarantee specified center frequencies and frequency tuning ranges.
For optimization of VCO performance and operation at higher frequencies,

varactors need to be scaled down [21]. However, VCO parasitics do not scale down to the same extent as the varactor size. Additionally the reduction of process variations is long-winded and difficult last but not least due to the rapid development of technologies with smaller minimum feature sizes. Clearly this intensifies the demand for varactors with wide tuning range further.

The aim of this work is the analysis and improvement of passive devices (varactors and inductors) for fully integrated RF circuits, e.g. VCOs, in standard digital CMOS or BiCMOS technologies.
It will be investigated how the capacitance tuning range of varactors can be improved. Identifying the effects which limit the tuning range leads to the development of several proposed varactor structures which reduce these effects. As the resistance of the device determines the quality factor, special attention is paid to the resistive behaviour.
The proposed devices include

- accumulation mode varactors with and without STIs (shallow trench isolation) and variations in CMOS as well as BiCMOS technologies,
- MOS varactors with alternating n and p doping of the gate and
- inversion mode varactors in CMOS technologies.

For integrated inductors a way to improve the quality factor is proposed. A substrate structure reduces the coupling between inductor and substrate.
The performance of the developed varactors is analyzed in VCOs. Frequency tuning range, the contribution of varactors and inductors to phase noise and the influence of variations of supply and tuning voltage will be studied. Possibilities to improve VCO performance will be shown.
As for circuit design accurate simulations are essential a model of the proposed varactor is developed.

The work is organized as follows. Chapter 2 provides the basics of MOS varactors, their capacitance characteristics, tuning behaviour and the problems of present varactor devices. The description of the electrical properties of integrated inductors, the problems of integration and known methods of resolution follow. Finally key parameters of VCOs, their description and optimization are covered.
Chapter 3 describes the design and discusses measurement results of various

proposed varactors with improved tuning range in standard CMOS as well as BiCMOS technologies. Also the frequency dependent capacitance behaviour is discussed.
Chapter 4 presents the preferred design of symmetrical integrated inductors and the performance of state-of-the-art devices. Further a substrate structure to improve the quality factor of integrated inductors is introduced.
Chapter 5 presents measurement results of VCOs using proposed MOS varactors as tuning elements. First the performance of VCOs with a proposed A-mode varactor is compared to the otherwise identical VCO with a conventional NMOS varactor. Then the influence of the MOS varactor gate doping on VCO performance is investigated. Finally the switched varactor concept is described and its potential and specialties are discussed. Several proposed varactor parameters are introduced that provide insight into VCO phase noise and sensitivity to variations of supply voltage and allow an estimation of these effects.
Chapter 6 describes the development of a physical model for the proposed varactors and its application to simulate a fully integrated VCO.
The last chapter summarizes this work.

Chapter 2

Basics of MOS varactors, integrated inductors and LC-voltage-controlled oscillators

This chapter covers the basic concepts, realisation and problems of varactors, integrated inductors and voltage-controlled oscillators.
The first section treats MOS varactors. It covers the inversion and accumulation mode devices, their voltage-dependent characteristics and tuning of the varactor's capacitance. The last part of the section introduces performance parameters, which are necessary to compare different devices, and estimate their potential for VCOs.
Fully integrated inductors are the subject of the second section. Common inductor designs are shown and electrical properties explained. The reason for frequency dependent inductance and resistance values is revealed. Finally the quality factor, which is used throughout this work, is defined and possibilities of its improvement are identified.
The section about voltage-controlled oscillators presents first the basic principle of a VCO. Then follows the description of power consumption and its

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optimization. Additionally insight into phase noise mechanisms and optimization possibilities is provided.

2.1 MOS varactors

MOS varactors are variable, voltage-controlled capacitors based on the MOS structure. Their main application are LC-voltage-controlled oscillators (VCOs). Together with an inductor L the varactor C determines the VCO frequency f_0 (without damping)

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{2.1}$$

2.1.1 Principle of inversion mode varactors

Fig. 2.1 shows a cross section of a NMOS varactor and the small-signal model generally assumed for varactors: a variable capacitance in series with a variable resistance.

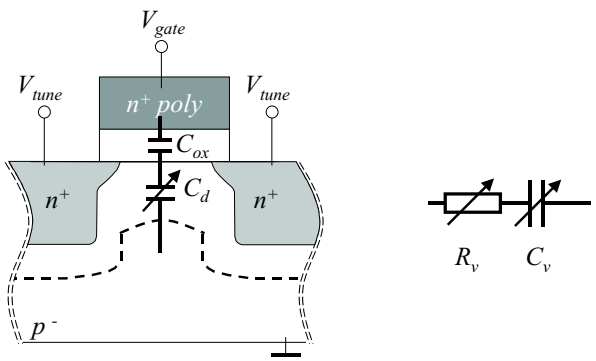

Figure 2.1: Cross section of a conventional NMOS varactor (in depletion; left) and the generally assumed model (right). The dashed line indicates the border of the depletion region.

For the NMOS device source and drain are n^+-doped. The substrate (or well) region between and around source and drain is of opposite doping, i.e. p^--type. Process determined the polysilicon gate is of the same doping as source and drain, i.e. n^+-type. A PMOS device is obtained when all regions have opposite doping as in the NMOS.
The MOS varactor is not a four-terminal device as the transistor but a three-terminal device. The source and drain regions are shorted to apply the voltage V_{tune} that tunes the variable capacitance. The p^- body is grounded and the voltage V_{gate} is applied to the gate node.
The variable capacitance C_v appears between the gate node and all other nodes at AC ground. Essentially it is the series connection of the gate oxide capacitance C_{ox} and the variable depletion region capacitance C_d

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d}. \tag{2.2}$$

Fig. 2.2 depicts the small-signal capacitance of a NMOS varactor at zero tuning voltage. The corresponding charges and the relevant lumped elements in the device are included also.
Negative gate voltages result in a hole surplus at the surface of the semiconductor; the device is in accumulation. Charge variations at the gate are balanced by changes in the accumulation layer charge. A large capacitance determined by the gate oxide is effective.
At increasing gate voltage the flat-band situation is reached. The semiconductor beneath the gate is neutral and fixed oxide and interface charges balance the gate charge. The flat-band voltage V_{FB} is usually negative as especially the oxide charges are comprised of positively charged alkali-ions unintentionally introduced during processing. Further for the value of V_{FB} the different work functions of the gate and the well have to be considered. If gate and well are of the same type of doping flat-band occurs close to 0V. Different doping shifts V_{FB} by ca. 1V.
Just above the flat-band voltage holes are repelled from the surface and the negatively charged ions of the fixed dopand atoms (acceptors) form a depletion region. Now changes in the gate charge are balanced by more or less negative dopands, i.e. by a deeper or shallower depletion region. The capacitance in this situation is a series connection of the gate oxide capacitance C_{ox} and the variable depletion region capacitance C_d.

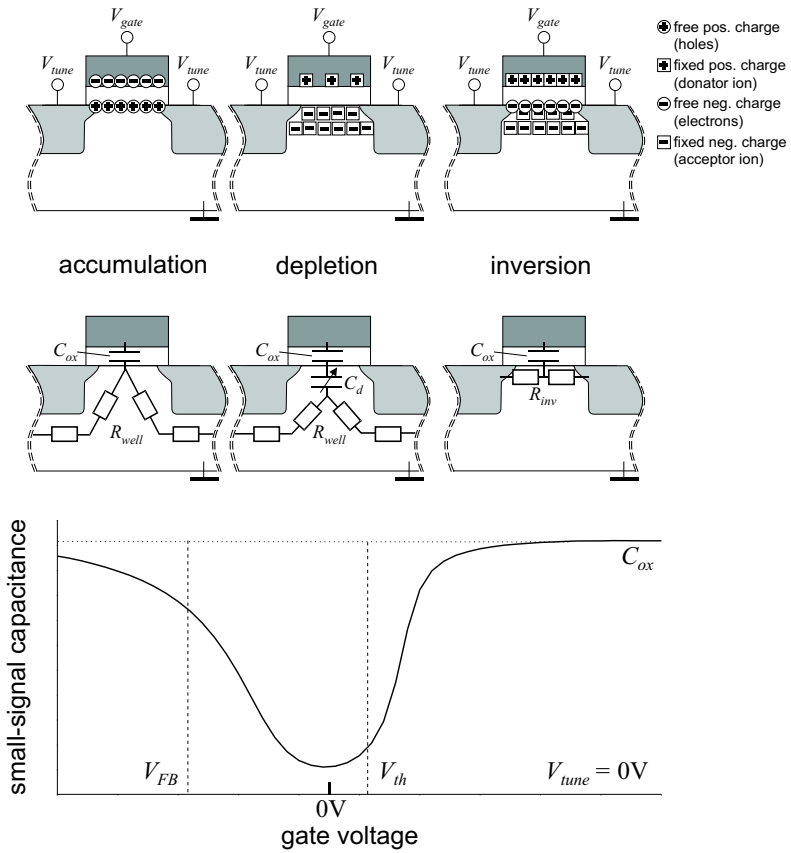

Figure 2.2: Typical measured small-signal capacitance characteristic of a NMOS varactor (bottom), the corresponding charges (top) and the relevant lumped elements (middle) at zero tuning voltage. Oxide, interface charges and charges at pn junctions are not shown.

Gate voltages above a certain threshold V_{th} result in a surplus of electrons at the semiconductor surface; the device is in inversion. In this situation the depth of the depletion region remains constant and changes in the gate charge are balanced by changes in the electron inversion layer. Again the

effective capacitance is determined by the gate oxide capacitance. The necessary electrons can be provided by thermal generation in the depletion region. However, at the voltages leading to inversion the electric field between the gate and the source/drain lowers the barrier between the source/drain and the semiconductor's surface considerably. Therefore the main source of electrons are the n^+-doped source and drain regions.

Part of the resistance is always the gate resistance determined by the polysilicon line. The gate area and thus the gate width have to be large to achieve the necessary capacitance values (≈500fF...2pF) for VCOs in wireless communication systems. With a regular straight transistor design the corresponding gate resistance

$$R_{gate} \propto N_{\square} R_{\square} \tag{2.3}$$

is large. $N_{\square}$ and $R_{\square}$ are the number of squares and the square resistance of the gate, respectively. To avoid this large, undesired resistance RF transistors as well as varactors are layed out in so called multifinger structures (Fig. 2.3).

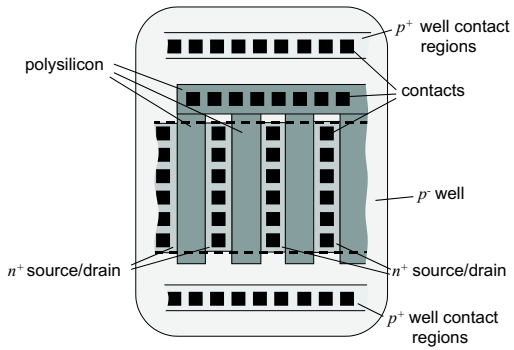

Figure 2.3: Typical multifinger structure of RF varactors. Dashed line indicates area of thin oxide.

Many short fingers (often less than 10μm) connected in parallel resemble a device with large total gate width

$$w_g = l_f N_F \tag{2.4}$$

with N_F the number of parallel fingers and l_f the length of each finger. Thereby the gate resistance is considerably reduced to

$$R_{gate} \propto \frac{F_\square R_\square}{N_F} \tag{2.5}$$

with $F_\square$ the number of squares per finger. A typical value for R_{gate} is around 300mΩ for a 600μm wide device (at 0.25μm gate length). Further reduction of the gate resistance by a factor of $\frac{1}{4}$ is achieved when contacting the gate fingers at both ends.
The typical behaviour of the total resistance of a NMOS varactor is shown in Fig. 2.4.

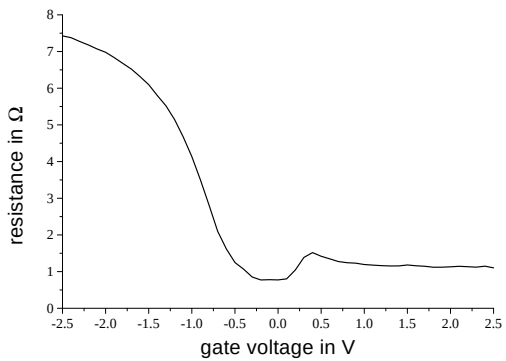

Figure 2.4: Typical measured small-signal resistance characteristic of a NMOS varactor.

In accumulation the gate resistance is in series to the resistance from the accumulation layer to substrate (well) contacts outside the device, see Fig. 2.3. This resistance is strongly layout dependent.
In depletion the resistance is usually lower than in accumulation, as the resistive path, now from the border of the depletion region to the substrate (well) contacts, is shorter. Above V_{th} the resistance is determined by the inversion layer. Thus a peak in the resistance is observed at the onset of inversion, as the semiconductor surface is only weakly inverted with few electrons. At higher gate voltages and strong inversion the resistance drops to a relatively low value. The resistance in inversion is proportional to the

gate length of the varactor.
The transition from depletion to inversion is determined by the voltage difference between gate and source/drain and the threshold voltage. Therefore the transition voltage will be increased with increasing tuning voltage (Fig. 2.5). The threshold voltage depends on the voltage between source/drain and substrate (bulk effect) and contributes additionally to the shift of the transition.

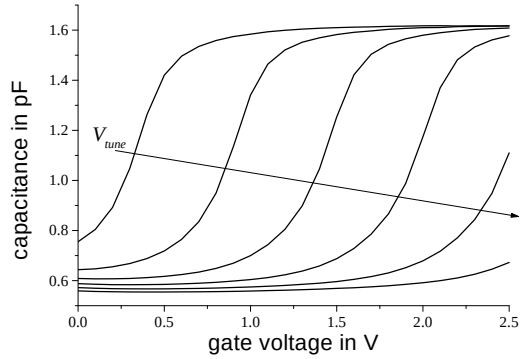

Figure 2.5: Typical measured small-signal capacitance characteristic of a conventional NMOS varactor at various tuning voltages (0V...2.5V; 0.5V steps).

Accumulation occurs only for gate voltages more negative than the bulk (substrate) voltage. However, independently of the tuning voltage the well is always at 0V and the transition to accumulation remains at fixed voltage (<0V). The device remains in depletion, the maximum depth of the depletion region is increased and the total capacitance slightly decreased (deep depletion).
Devices in practical circuits are operated in the positive voltage range. As NMOS and also PMOS varactors are then between depletion and inversion they are called inversion mode (I-mode) varactors. Their maximum capacitance appears in inversion, the maximum resistance at the onset of inversion.

2.1.2 Accumulation mode varactors

Devices that are in depletion or accumulation in the positive voltage range are called accumulation mode (A-mode) varactors. Fig. 2.6 shows a cross section of an A-mode varactor in n^- well and the small-signal capacitance characteristic. The device is derived from a PMOS varactor[1], in which the p^+ source/drain regions are replaced by n^+-well contacts. Thus the potential of the complete well is tuned.
Due to the close similarities with a NMOS structure, the A-mode in n^- well is often called "NFET in Nwell".

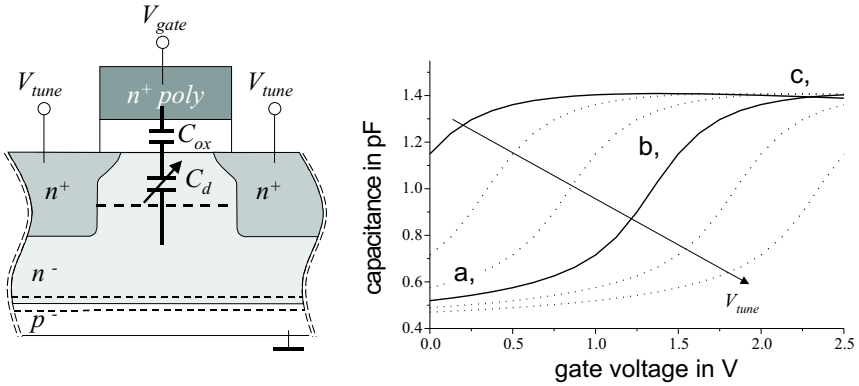

Figure 2.6: Cross section of an A-mode varactor in n^- well (in depletion; left) and the measured small-signal capacitance characteristic (right) at various tuning voltages (0V...2.5V; 0.5V steps). Dashed lines indicate the borders of depletion regions.

The flat-band voltage is close to 0V, as gate and well are of the same doping type.
First the behaviour at zero tuning voltage is considered. At zero gate voltage the device is already at the onset of accumulation. A small increase of V_{gate} drives the varactor entirely into "strong accumulation". The capacitance shows a high value determined by the gate oxide. The resistance is given by

[1] classification by the carrier type in the inversion layer; here holes

the accumulation layer and the parallel well resistance, in addition to the gate resistance.
An increase in tuning voltage shifts the transition voltage (depletion to accumulation) to higher gate voltages. Contrary to the I-mode varactors this corresponds to simply shifting the capacitance characteristic. At some tuning voltage both, depletion and accumulation occur within the usable voltage range. At medium tuning voltages and low gate voltages the varactor is in depletion (a,). The capacitance is low due to the series connection of oxide and depletion capacitance.
With increasing gate voltage the flat-band case for the respective tuning voltage is reached (b,). Again, increasing the gate voltage beyond $V_{FB}(V_{tune})$ leads to accumulation (c,), with high capacitance.
Even at high tuning and low gate voltages no capacitance increase due to inversion is observed. Without p^+ source/drain inversion can occur through thermally generated holes only. Such an inversion layer is present, however, it is electrically isolated and there is no reservoir of holes. At frequencies well above the generation rate of holes small-signal changes in the gate charge can not be balanced by changes in the inversion layer, but must be balanced by changes in the depth of the depletion layer. Therefore the capacitance remains low. Variation of the "DC" gate voltage, however, is very slow, and the corresponding change of gate charge is still balanced by holes. Thus the depth of the depletion region remains constant and the capacitance has a low value.
The resistance behaviour is discussed in detail in section 3.2.3.
For very low frequencies, at which holes can be generated fast enough the high capacitance due to inversion can be observed [33]. But as the doping dependent generation rates are on the order of milliseconds [36] and the corresponding frequencies in the hertz range, it is not expected that this phenomenon plays a role at the frequencies of interest, which are in the GHz range.

2.1.3 Performance parameters of varactors

The following performance parameters, capacitance tuning range and quality factor, provide a tool to compare different varactors. Their definition stem from VCO requirements, which will be treated in detail in section 2.3.

Conventional absolute data

Conventionally the absolute capacitance tuning range is defined as

$$C_{ratio} = \frac{C_{max}}{C_{min}}. \tag{2.6}$$

It is determined by the maximum capacitance C_{max} in inversion or accumulation and the minimum capacitance C_{min} in depletion. Typical values of NMOS varactors in 0.25μm technologies are between 2.5 and 3.0 (including wiring within the varactor). Results for PMOS and A-mode devices are similar.

The second generally important figure to measure the performance of varactors is the quality factor. The conventional definition of quality factor can be written as

$$Q = \frac{\text{(Capacitively) Stored energy per cycle}}{\text{(Resistively) Dissipated energy per cycle}}. \tag{2.7}$$

For varactors this expression simplifies to

$$Q = \frac{1}{2\pi f RC}. \tag{2.8}$$

f is the frequency and R and C are the instantaneous values of the series resistance and the total capacitance, respectively.
The minimum quality factor is of special interest, since it marks the low-end performance. For I-mode varactors it appears at the onset of inversion where the capacitance is already high and the resistance-peak occurs. Typical 0.25μm NMOS varactors reach Q_{min}-values around 40...45. Similar PMOS devices offer somewhat reduced minimum quality factors due to lower mobility of holes compared to electrons and therefore higher resistances. Usually the minimum quality factors of the A-mode devices are higher than for the NMOS varactors, due to lower resistance.

Averaged varactor data

Typical VCOs incorporate MOS varactors with DC-voltages at the tuning input and the VCO output signal at the gate. Due to phase noise considerations (in detail in section 2.3.3) the signal swing at the output should be

as large as possible, ideally V_{dd}.
MOS-Varactors feature high tuning ranges but a steep capacitance variation not only with tuning voltage but also with gate voltage (Fig 2.5). Thus the large signal swing in the VCO means not only a strong variation of gate voltages, but also the instantaneous capacitance values vary widely, especially at low/medium tuning voltages, where the transition between depletion and inversion/accumulation can be observed. This behaviour occurs within each period of the oscillation (in the GHz-range) and therefore it is more meaningful to consider averaged capacitances than absolute capacitances. This averaged capacitance mimics large-signal behaviour.
At a signal swing of ideally V_{dd} the averaged values for each tuning voltage are obtained by

$$C_{av}(V_{tune}) = \frac{1}{V_{dd}} \int_{0V}^{V_{dd}} C(V_{gate}, V_{tune}) \mathrm{d}V_{gate}. \tag{2.9}$$

The integral simultaneously denotes the total charge, which is necessary to charge or discharge the varactor in each cycle.
Consequently an averaged capacitance tuning range is defined as

$$C_{av,ratio} = \frac{C_{av,max}}{C_{av,min}}. \tag{2.10}$$

Clearly $C_{av,max} < C_{max}$ and $C_{av,min} > C_{min}$ lead to lower averaged than absolute capacitance tuning ranges. C_{max} and C_{min} denote the absolute values extracted from the small-signal capacitance characteristic.
Parasitic capacitances C_{pC} in the rest of the VCO lower the effective capacitance tuning range further to

$$C_{eff,ratio} = \frac{C_{av,max} + C_{pC}}{C_{av,min} + C_{pC}}. \tag{2.11}$$

Similarly to the capacitance tuning range of varactors it is more meaningful to consider the averaged quality factor

$$Q_{av}(V_{tune}) = \frac{1}{V_{dd}} \int_{0V}^{V_{dd}} Q(V_{gate}, V_{tune}) \mathrm{d}V_{gate} \tag{2.12}$$

where $Q(V_{gate})$ is the quality factor obtained from small-signal measurements.

2.1.4 Present varactor designs and problems in CMOS

Currently, varactors in standard CMOS technologies are realized as junction-diodes [20, 44] or as MOS-varactors.
In contrast to optimized bipolar or BiCMOS RF-processes, no process option for specific varactor junction-diodes is available in standard CMOS technologies. Therefore source/drain-well junctions of NMOS or PMOS structures (e.g. p^+ in n^- well) have to be used as diodes, leading to either moderate quality factors or tuning ranges significantly lower than MOS varactors. The approach of differential operation or concentric diode layouts to increase quality factors leaves the capacitance tuning ranges of diodes still below the values that MOS varactors reach [44]. The ongoing decrease of power supply voltages in CMOS circuits further aggravates the tuning problem of junction-diode varactors. [19, 46]. Additionally it has to be ensured that diodes are not forward-biased. Therefore this work considers only MOS varactors.
Most MOS varactors published either individually or in the context of VCOs are I-mode NMOS [12, 21] or PMOS [19, 21, 44] or A-mode varactors in n^- well [1, 8, 13, 19, 46, 59]. One A-mode varactor has been presented with extraction regions for thermally generated charge carriers [45]. Thereby deep depletion instead of inversion is reached. But all solutions suffer from relatively high parasitic capacitances C_p that limit their capacitance tuning range as then Eq. 2.6 reads

$$C_{ratio} = \frac{C_{max} + C_p}{C_{min} + C_p}. \tag{2.13}$$

A combination of MOS and diode varactors has been presented in [65]. The main disadvantages of this approach are low quality factors and two tuning voltages, which complicate circuit design.
Although capacitance tuning ranges of MOS varactors are well above the values of diodes the development of varactors with even wider tuning ranges is pushed. The reason are frequency tuning specifications that exist for VCOs in e.g. wireless communications. As process variations can lead to 15% variations in capacitance [45] a large capacitance tuning range is necessary to nevertheless guarantee a specified frequency tuning range of the VCO. The parasitic capacitances in the VCO intensify the problem as they deteriorate the effective capacitance tuning range further (Eq. 2.11). If bondwires are used as inductors the inductance can differ substantially from

the intended value, due to difficult manufacturability and reproducability. Integrated inductors are very easy and exact to manufacture but the prediction of inductance value holds some uncertainties. The varactor has to compensate these variations in inductance also.
For increasing frequencies the varactor needs to be scaled down. However, the parasitic capacitances in the VCO do not scale to same extent as the varactor. Thus the trend to higher frequencies aggravates the described problems.

2.2 Integrated inductors

Inductors are widely used in RF circuits, e.g. as inductive load or matching element in low noise amplifiers (LNAs) or as part of the frequency determining LC-tank in voltage-controlled oscillators. This work focuses on integrated symmetrical inductors for use in VCOs in standard digital CMOS technologies.
Easy and exact manufacturability with very little inductance variations are the most important among the advantages that integrated inductors offer over bond-wires (despite the relatively large die area). Digital CMOS technology holds some disadvantages for inductors like thin metals, thin isolator between metals and substrate and highly doped substrates. Nevertheless a strong urge exists to use this technology due to cost considerations and the possibility to integrate both, digital and analog functions on the same chip.

2.2.1 Common inductor designs

The most common integrated inductors are hollow spiral inductors (connected metal traces arranged in a spiral configuration). Mostly the spiral inductors have several windings, and hollow in this context means that none of the windings extends into or near to the center of the device. (Further on inductor stands for integrated, spiral, hollow inductor.) Fig. 2.7 depicts some important inductor designs, a quadratical, an octagonal and a symmetrical, octagonal inductor.

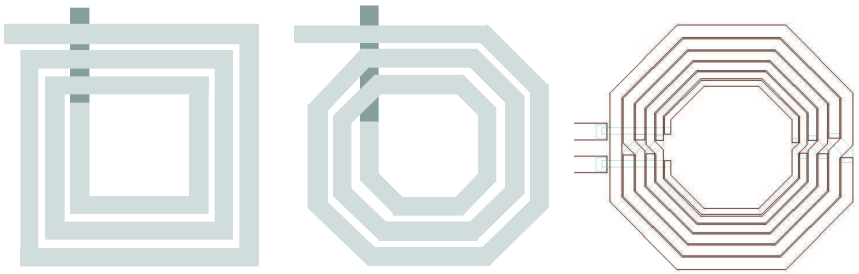

Figure 2.7: Quadratical, octagonal and symmetrical, octagonal inductor designs.

Symmetrical inductors offer the advantage of appearing identical from either port, which is especially important for differential applications.
The homogeneity of the magnetic field can be increased through increasing the circularity. However in many cases the extent to which the number of corners can be increased is limited by mask data preparation often only allowing 45deg and 90deg angles between metal lines (i.e. quadratical and octagonal inductors).
As all modern (deep-sub-micron) technologies offer several metal layers there exist two options to use this feature. Each uses the identical pattern for all chosen metal layers. The first method connects these layers in series to mimic a solenoid-like behaviour and to thereby increase the homogeneity of the magnetic field, i.e. the inductance, compared to a one layer structure. However, the series resistance of this inductor increases as the total length of the metal line increases. Further, as adjacent metal layers are not at the same potential capacitances between them become active. The second method connects the metal layers with identical pattern in parallel. The aim is to reduce the series resistance, as the effective metal thickness of the resulting inductor is roughly the sum of all used metal layers. Additionally the available low-ohmic connections between adjacent metal layers keep the capacitance between them low.

2.2.2 Electrical properties of inductors

The differential output signals of the VCO appear at the inductor nodes. The swing of this signal is large and the inductor is subject to large-signal

AC currents. To describe the resulting electrical properties (and problems) of an inductor a simple π-model is sufficient (although it might not be enough to simulate the inductor accurately). Fig. 2.8 shows the cross section of a simple integrated inductor and the lumped elements forming the π-model (grey bar indicates the simplified one metal layer inductor). The inductor is described by the inductance L and the series resistance of the metal windings R_l. There is a parasitic capacitance C_f from input to output (including the capacitances between adjacent windings) and a capacitance C_{ox} from the inductor to the grounded substrate. R_{sub} describes an effective substrate resistance.

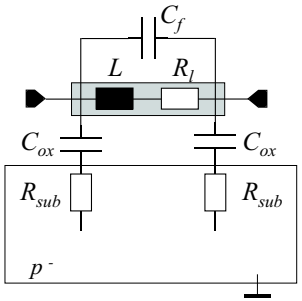

Figure 2.8: Cross section of a simple one-layer inductor (grey bar) and its lumped-elements model (in low-ohmic substrate).

Inductance

The inductance L of a rectangular inductor can be calculated by the Greenhouse method [32]. But there exist handier simplifications, e.g. the inductance of a hollow, square inductor is approximated by [52, 53]

$$L \approx \frac{45\mu_0 n^2 a^2}{22r - 14a} \tag{2.14}$$

with μ_0 the permeability of vacuum (the relative permeability μ_r is assumed to be 1), n the number of windings, r the outer radius and a the mean

radius of the inductor (Fig. 2.9). This formula generally yields accurate results with less than 5% error.

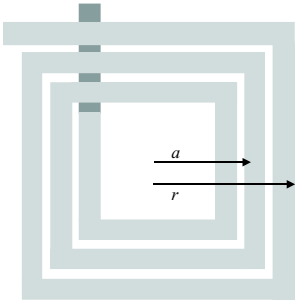

Figure 2.9: Top view of a square inductor and dimensions necessary for inductance calculation.

The above formula is often simplified to

$$L \approx \mu_0 n^2 r, \tag{2.15}$$

for quick, crude calculations.
Other shapes can be accomodated when using the argument that all loops with same area have about the same inductance ($L \approx \mu\sqrt{\pi}A$, A the area)[52]. The inductance equations for a square inductor simply have to be multiplied by the area ratio of the new shape compared to the square, e.g. for a circular inductor by $\sqrt{\pi/4}$. The crude approximation of Eq. 2.15 in all cases reads as $L \propto n^2 r$.

Losses in the metal windings

The series resistance of the metal windings at low frequencies can be calculated as the product of the resistance per square and the total number of metal squares. However, at high frequencies magnetic field effects result in non-uniform current flow in the conductor and increased series resistance of the windings. The most prominent of these effects is the skin effect resulting from the inner self inductance of the conductor [55]. It causes a current

crowding at the surface of the conductor. The thickness of the sheet in which current flows depends on permeability and resistivity of the conductor and frequency. The skin depth decreases when increasing either of the mentioned parameters. In digital CMOS metal layers are quite thin and current crowding in the vertical direction does not play a role. However, the winding width often exceeds the skin depth and the skin effect leads to a noticeable increase in series resistance. For example for a 10μm wide aluminum line at 10GHz a 20% increase of resistance compared to the DC resistance has been observed [54]. This situation can be aggravated by the proximity effect: the magnetic field originating from a nearby conductor can enhance the skin effect.
The magnetic field generated by the inductor passes not only through the center of the inductor but is also strong in a certain area around the center. If windings extend near to or into the center of the inductor the magnetic field will lead to circular eddy currents in the inner windings. These eddy currents will disturb the original current flow in the inductor and generate a magnetic field in the opposite direction of the inductor's field. Therefore, at high frequencies, the total resistance increases and the inductance decreases (as the total magnetic field decreases). So, the innermost windings do not contribute significantly to the inductance (as they enclose only a small area) but have a detrimental effect on resistance. The conclusion is to omit the innermost windings, i.e. use a hollow inductor, and thereby achieve better performance [20, 38].

Losses in the substrate

The large-signal AC currents in the inductor result in undesired capacitively and inductively induced substrate currents. They are described by the resistances R_{sub}.
The capacitively induced substrate currents stem from the capacitive coupling between the inductor and the substrate through C_{ox}. As first order approximation $C_{ox} \propto A_{metal}/d_{ox}$, with A_{metal} the total metal area of the inductor and d_{ox} the thickness of the oxide between the metal layer and the substrate.
The constantly changing magnetic field around the inductor results in inductively induced eddy currents in the substrate (according to Lenz's Law). Flowing circular in the opposite direction as the current in the inductor they generate a magnetic field opposing the inductor's magnetic

field. The total magnetic field and the inductance is reduced.
Both type of currents increase the losses of the inductor and deteriorate its performance.
To alleviate this problem inductors are advantageously realized in the topmost metal layers. This reduces the coupling capacitance C_{ox} (as the oxide thickness is increased) and simultaneously the magnetic field of the inductor (and therefore the induced eddy currents) in the substrate. Further it is generally assumed that the problem becomes less serious with less high doped substrates, i.e. highly resistive substrates, as current flow should be suppressed.
In reality a careful study of the interaction of the capacitances and resistances is necessary to decide whether an increasing substrate resistance is beneficial.

2.2.3 Model for extraction of inductor parameters

For extracting parameters the complex inductor is generally viewed as simple series connection of an effective inductance and an effective series resistance (Fig. 2.10), both with frequency dependent values $L_{eff}(f)$ and $R_{eff}(f)$.

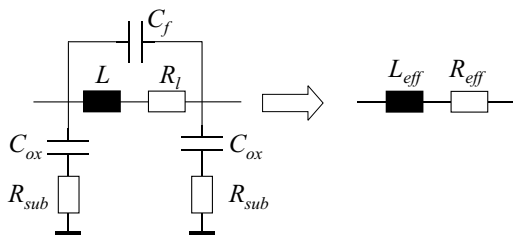

Figure 2.10: Further simplification of simple π-model of inductor for parameter extraction.

Due to this simplification the typical inductance and resistance plots (Fig. 2.11) of an inductor show the strong frequency dependence introduced mainly through the parasitic capacitances.

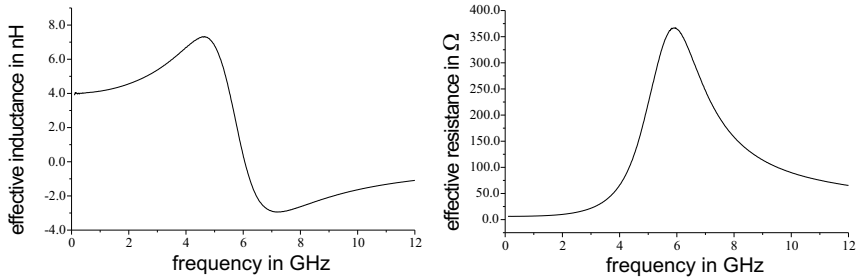

Figure 2.11: Typical measured effective inductance and resistance plots of an inductor.

At a certain frequency, the self-resonance frequency, the effective inductance even becomes zero, as L is in resonance with the parasitic capacitances.

2.2.4 Quality factor of inductors

The performance of the inductor is limited by the losses through undesired currents in the substrate and in the series resistance of the inductor windings. Although there exist several definitions of quality factor they can be reduced to the common, central statement: the quality factor increases when the losses decrease.

Definition of quality factor

The general definition of quality factor is

$$Q = \frac{\text{(Inductively) Stored energy per cycle}}{\text{(Resistively) Dissipated energy per cycle}}. \tag{2.16}$$

The most common and most widely used definition of quality factor Q [31]

$$Q = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{2.17}$$

reads in terms of effective inductance and resistance as

$$Q = \frac{2\pi f L_{eff}(f)}{R_{eff}(f)}. \tag{2.18}$$

with f the frequency. Fig. 2.12 shows a typical quality factor plot. Due to its definition this quality factor is zero at the self resonance frequency of the inductor, which is a physically unreasonable result [31].

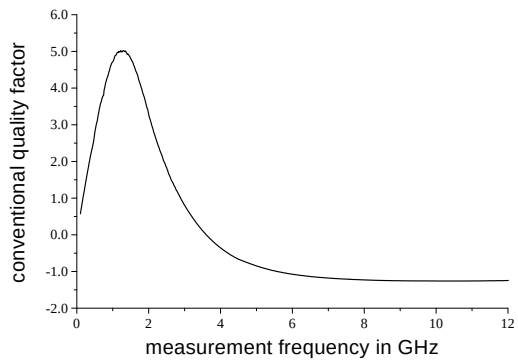

Figure 2.12: Typical measured plot of conventional quality factor according to Eq. 2.17.

Therefore [31] suggests different quality factors based on the consideration that parameters of interest to designers are loss, bandwidths of resonant circuits and frequency stability factors of oscillators (in more detail in section 2.2.4). The definition of choice in this work is the bandwidth definition. However, a bandwidth is only defined at a resonance frequency, of which the inductor shows only one. But this proves not to be a problem, because using an inductor in a circuit always requires adding intentional or unintentional (parasitic) capacitances. This alters the resonance frequency and the bandwidth. To obtain both parameters an ideal capacitance (no series resistance), whose value is swept, is numerically added in parallel to the measured Y_{11} data of the inductor (Fig. 2.13).

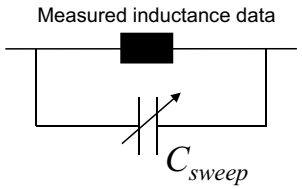

Figure 2.13: Test circuit to extract quality factors according to bandwidth definition.

The 3dB-bandwidth Δf_{3dB} at the resonance frequency f_{res} of the resulting network is then converted to an effective quality factor Q_{BW} via

$$Q_{BW} = \frac{f_{res}}{\Delta f_{3dB}}. \tag{2.19}$$

This figure serves as quality factor as it describes the frequency selectivity of the virtual LC-tank.
In plots Q_{BW} is typically shown as function of the resonance frequency of the "virtual" tank (Fig. 2.14; Details of the extraction procedure can be found in appendix C).

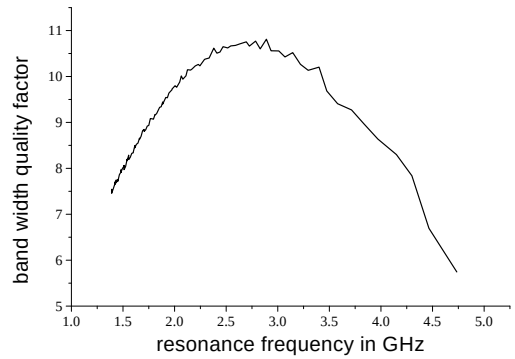

Figure 2.14: Typical plot of quality factor according to bandwidth definition based on measured inductor data.

The quality factor according to bandwidth definition offers two considerable advantages over the conventional definition. First, it remains useful up to

the self resonance frequency of the inductor. Second, it allows the designer to identify an oscillator's frequency range at which the quality factor is highest and simultaneously gives the necessary parallel capacitance.

Methods to improve Q of inductors

For low phase noise and power consumption of a VCO it is essential that the passive elements of the tank have large quality factors (details in the following section 2.3, page 27).
However, at the frequencies for mobile communications the quality factors of integrated inductors are usually much lower than the quality factors of conventional diode or MOS varactors. Therefore VCO designers strive for inductor designs providing higher quality factors.
In digital CMOS technologies the thickness of the metal layers is lower than in bipolar and BiCMOS technologies, leading to higher series resistances. Further the distance between the inductor and the substrate are low and substrates are highly doped. This results in strong coupling to the substrate.
As mentioned before the lower cost of CMOS nevertheless drives designers and industry to use this technology. Therefore a strong urge exists to improve the performance of inductors. Naturally this is done by reducing losses through a reduction of parasitic components.
One prominent measure to reduce the series resistance is the parallel connection of metal layers. Further a variety of substrate structures and ground shields has been published. Many aim mainly at reducing eddy currents, whereas capacitive coupling between inductor and substrate remains constant or is even increased. [22, 24, 25] use so called patterned ground shields (Fig. 2.15) to terminate electrical field lines. A low ohmic resistance to ground in series to the oxide capacitance reduces capacitively induced losses. Simultaneously the patterning prohibits the circular flow of eddy currents. A drawback of this method is the increase of oxide capacitance leading to lower self resonance frequencies, as the shields are formed in either polysilicon or the first metal layer.

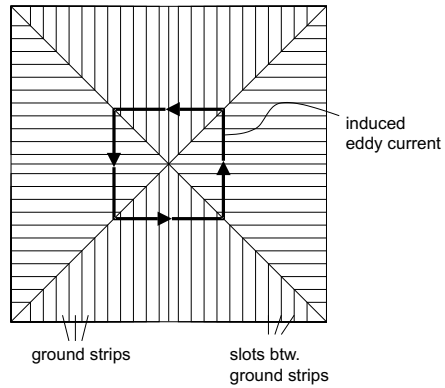

Figure 2.15: Principle of patterned ground shields.

[23] achieves a reduction of eddy current flow by using the channel stop implant under field oxide as highly doped but very thin and therefore highly resistive layer.
A reduction of parasitic capacitances is achieved in [25, 26, 27, 28], but always in non-standard CMOS technology. E.g. [27] introduces an array of closely spaced stripes of deep trenches (known from DRAM cells) underneath the inductor, or [28] uses suspended inductors, where the substrate beneath the inductor has been etched away. The only solution compatible with standard CMOS technology is obtained by a biased n^- well described in [29]. But this solution has a homogeneous region below the inductor. Only a vertical depletion region below the n^- well can be used to decrease the parasitic capacitance, and there is no patterning that could reduce eddy currents.

2.3 LC-tank voltage-controlled oscillators

In this section the basic principle and important parameters in LC-tank voltage-controlled oscillators are described. The easy to integrate and widely tunable CMOS ring oscillators with low area-consumption exhibit inferior phase noise at the same power consumption [30]. Therefore they are not an

alternative for wireless, battery powered communications systems; LC-VCOs feature lower power consumption and phase noise but only moderate tuning ranges and the required inductor design is complicated (on-chip, bond-wire, external,...).
The large number of publications [12] - [21] demonstrates the importance of VCOs for wireless systems.
Oscillators in communication systems provide the periodic signals for timing of digital circuits or frequency translation. This work is focused on the oscillators for frequency translation, often referred to as local oscillators (LO), used in receivers or transmitters. Assuming both, the signal and the LO, to be sinusoidal with frequencies f_{signal} and f_{LO} the signal can be down or up-converted through mixing to intermediate frequencies (IF)

$$f_{IF} = f_{signal} \pm f_{LO}. \tag{2.20}$$

2.3.1 Basic principle

A general LC-VCO can be symbolized as in Fig. 2.16.

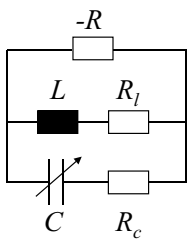

Figure 2.16: General LC-VCO.

The oscillator consists of an inductor L and a varactor C, building a parallel resonance tank, and an active element $-R$, compensating the losses of the inductor (R_l) and the losses of the capacitor (R_c). The value of the capacitance C is varied by a DC tuning input voltage and the circuit results into a voltage-controlled oscillator with center frequency:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{2.21}$$

The frequency tuning range of the VCO is then determined by

$$f_{ratio} = \frac{f_{max}}{f_{min}} = \sqrt{\frac{C_{C,max}}{C_{C,min}}} \tag{2.22}$$

where $C_{C,max}$ and $C_{C,min}$ are the maximum and minimum achievable capacitances in the complete circuit.

2.3.2 Power consumption

Description of power consumption

Due to energy conservation, the maximum energy stored in the inductor must equal the maximum energy stored in the varactor when the losses are compensated. Thus

$$CV_{peak}^2 = LI_{peak}^2 \tag{2.23}$$

with V_{peak} the peak voltage across the varactor and I_{peak} the maximum current through the inductor [21]. The power consumption results as

$$P_{loss} = \frac{1}{2}RI_{peak}^2 = \frac{1}{2}C\frac{R}{L}V_{peak}^2. \tag{2.24}$$

Rewriting with Eq. 2.21 and $\omega = 2\pi f$ yields

$$P_{loss} = \frac{1}{2}\omega^2 RC^2 V_{peak}^2 = \frac{1}{2}\frac{1}{\omega^2}\frac{R}{L^2}V_{peak}^2. \tag{2.25}$$

These losses in the tank have to be compensated through the power consumption of the VCO.

Optimization of power consumption

As at a given frequency P_{loss} is inversely proportional to L^2 the most effective way to decrease power consumption is to increase L/R [21]. This

can simply be accomplished by increasing the winding count n of the inductor, as $R \propto n$, but $L \propto n^2$ (see section 2.2.2). Larger inductance requires lower capacitance values C for constant frequency (Eq. 2.21). As a certain frequency tuning range is usually required, a decrease of tank capacitance is only possible when the effective capacitance tuning range (Eq. 2.11) remains high, i.e. with highly tunable varactors.
For a given VCO with fixed inductance value the power consumption reduces when tuning to higher frequencies f_0 (for constant V_{peak}).

2.3.3 Phase noise

Definition of phase noise

The ideal sinusoidal oscillator is described as

$$V_{out}(t) = Acos[2\pi f_0 t + \phi] \tag{2.26}$$

with A the amplitude, f_0 the frequency and ϕ a fixed phase. In the frequency domain the spectrum of this oscillator consists of Dirac-impulses at $\pm f_0$. The real oscillator is more generally given by

$$V_{out}(t) = A(t)y[2\pi f_0 t + \phi(t)]. \tag{2.27}$$

y is a 2π-periodic function. The fluctuations introduced by $A(t)$ and $\phi(t)$ - now functions in time - result in sidebands close to f_0, with symmetrical distribution around f_0 (Fig. 2.17) [30]. The frequency fluctuations correspond to jitter in the time-domain, which is a random perturbation of zero-crossings of a periodic signal (Fig. 2.18).

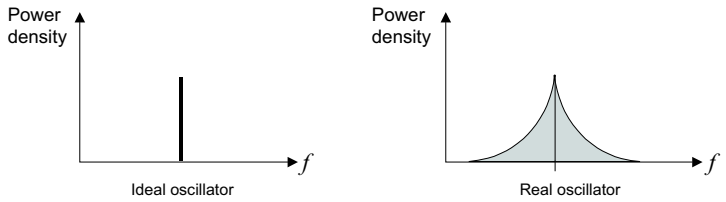

Figure 2.17: Frequency spectrum of ideal and real oscillators.

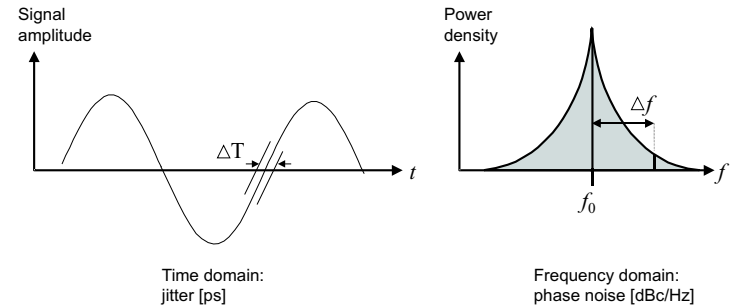

Figure 2.18: Jitter in the time domain relates to phase noise in the frequency domain.

Frequency fluctuations are usually characterized by the single sideband noise spectral density normalized to the carrier signal power (Fig. 2.17). It is defined as

$$\mathcal{L}_{total}(f_0, \Delta f) = 10 \log \left[\frac{\mathcal{P}_{sideband}\left(f_0 + \Delta f, 1\text{Hz}\right)}{\mathcal{P}_{carrier}} \right] \tag{2.28}$$

and has units of decibels below the carrier per hertz (dBc/Hz). $\mathcal{P}_{carrier}$ is the carrier signal power at the carrier frequency f_0 and $\mathcal{P}_{sideband}(f_0 + \Delta f, 1\text{Hz})$ denotes the single sideband power at the offset Δf from the carrier f_0 at a measurement bandwidth of 1Hz.
The total phase noise $\mathcal{L}_{total}$ includes both the amplitude $A(t)$ and phase $\phi(t)$ fluctuations. In practical oscillators the amplitude is limited and $\mathcal{L}_{total}(f_0, \Delta f)$ is dominated by the phase part, the phase noise [30, 38].

Importance of phase noise

The front-end of a typical receiver is shown in Fig. 2.19, where a mixer and a LO downconvert the incoming radio frequency (RF) signal to a lower, intermediate frequency (IF). With a LO frequency lower than the RF frequency (low-side LO) the resulting intermediate (IF) frequency is determined by: $f_{IF} = f_{RF} - f_{LO}$. As the IF-frequency is fixed the LO is varied according to the RF signal. To achieve synchronization between the RF and LO signals, the VCO is engaged in a phase-locked-loop (PLL, Fig. 2.19). A typical PLL consists of a VCO, a low-pass loop filter, a phase detector and a frequency divider. It forces the output frequency to be equal to (a multiple of) the input reference frequency. [30, 38, 39]

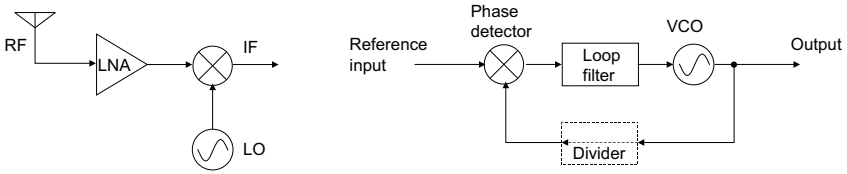

Figure 2.19: Simplified receiver block diagram (left) and phase-locked loop (right).

PLL design is eased significantly with a VCO offering a linear dependence between tuning voltage and frequency [49].
To understand the importance of phase noise Fig. 2.20 depicts the situation in a receiver. The LO signal used for downconversion has a noisy spectrum. Besides the wanted signal with small power an unwanted signal with large power is present in an adjacent channel (at a close-by frequency).
After mixing with the LO the downconverted spectrum consists of two overlapping spectra. The wanted signal suffers from significant noise due to the tail of the interferer: the signal-to-noise ratio is degraded [30, 38, 39].
In order to be able to detect the signals from all channels while (stronger) interferers may be present stringent phase noise specifications have to be met in wireless communication systems.

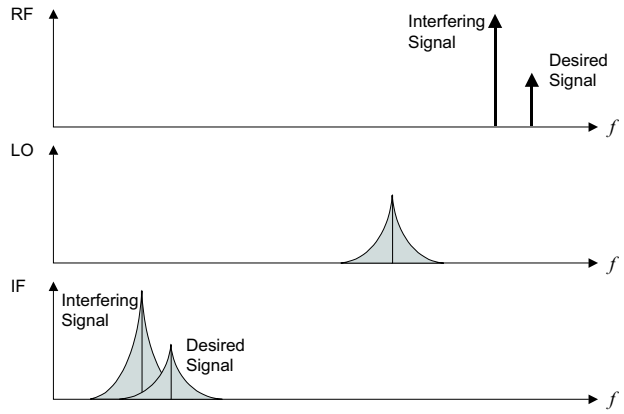

Figure 2.20: Effect of oscillator phase noise in a receiver.

Description of phase noise

A typical single side band phase noise spectrum is given in Fig. 2.21 [30, 38]. At low offset frequencies up to a corner frequency $\Delta f_{1/\Delta f^3}$ a $1/\Delta f^3$ behaviour is observed. For medium offset frequencies the phase noise shows a $1/\Delta f^2$-dependence up to where the constant amplifier noise floor begins to dominate.
The semi-empirical Leeson-Cutler [37, 40, 41] model describes the following behaviour of the phase noise $\mathcal{L}$ at the carrier frequency f_0 and the offset frequency Δf [37, 40, 41]:

$$\mathcal{L}\left(f_0, \Delta f\right) = 10 \log \frac{2FkT}{P_{sig}} \underbrace{\underbrace{\left[1 + \left(\frac{f_0}{2Q_{LC}\Delta f}\right)^2\right]}_{\frac{1}{\Delta f^2}} \left(1 + \frac{\Delta f_{1/f^3}}{|\Delta f|}\right)}_{\frac{1}{\Delta f^3}}. \tag{2.29}$$

where F is the empirical device excess noise factor, k is the Boltzmann's constant, T is the absolute temperature, P_{sig} is the signal power, f_0 is the

oscillation frequency and Q_{LC} is the quality factor of the loaded tank. This description of phase noise has been theoretically proved in [16].

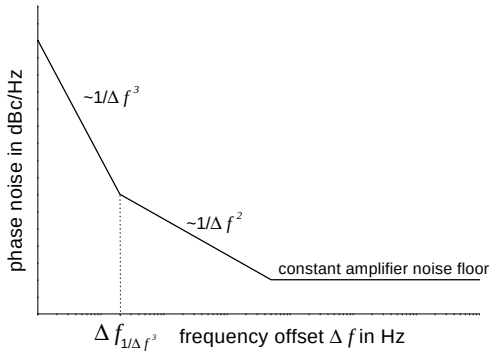

Figure 2.21: Typical phase noise spectrum of a LC-oscillator.

The $1/\Delta f^2$ portion of the spectrum follows from applying the LC-tank's transfer function and considering the Barkhausen criterion for steady state oscillation. It is dominated from the thermal noise sources in the oscillator, the parasitic resistances in the tank and the active devices. Their influence is described by the factor $2FkT/P_{sig}$, where kT stems from the effective resistance in the tank and F is a multiplicative factor accounting for excess noise due to the active devices in terms of resistor noise. The frequency and quality factor dependence is introduced by the transfer function of the tank. Intuitively it is clear that increasing thermal noise ($2FkT$) or decreasing signal power (P_{sig}) deteriorates the signal-to-noise ratio thereby increasing phase noise.
Viewing the LC-tank as simple RLC band-pass filter explains the influence of Δf and Q_{LC}. The amplitude response of the oscillator with respect to a driving frequency is shown in Fig. 2.22(top) [30].
With increasing Q_{LC} the pass band is narrower and oscillations at offset frequencies are more effectively damped: the corresponding phase noise decreases. The white noise of the devices in the VCO can be viewed as sources driving the oscillator. Noise around the oscillation frequency f_0 is amplified. The roll-off of the amplitude response is inversely proportional to $Q_{LC}\Delta f$.

As for phase noise the power behaviour has to be considered the frequency roll-off of the phase noise follows a $(Q_{LC}\Delta f)^{-2}$ behaviour.

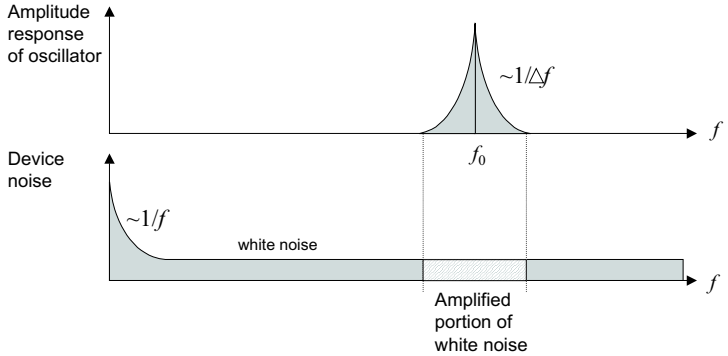

Figure 2.22: Amplification of white noise into the $1/\Delta f^2$ phase noise spectrum of a LC-oscillator.

Unluckily the mechanisms leading to the $1/\Delta f^3$ portion of the spectrum are less easy to understand and quite different than for thermally induced noise. However the general understanding is that low-frequent $1/f$ noise of the active devices undergoes upconversion to the oscillation frequency and via the transfer function of the LC-tank results in the $1/\Delta f^3$-behaviour of the phase noise [16, 42, 48]. Non-linearities in the devices lead to asymmetrical waveforms and harmonics to the carrier frequency and it is assumed, and experimentally supported, that this asymmetry plays the main role in upconversion of low-frequent noise [16]. Symmetrical in this context means symmetrical rise and fall behaviour in each half-period (between two zero-crossings).
An intuitive view how upconversion occurs and relates to the symmetry properties of the waveform can be found in the time-domain (Fig. 2.23). The output signal voltage is assumed to be sinusoidal (bottom) and reflects the loading and unloading of the capacitance. Compared to the signal the low frequent noise can be approximated to be DC (top).
Rising will be accelerated by a factor determined by the value of the capacitance, the slope of the transition and the noise current. Similarly the falling transition will be slowed down [30, 50].

For symmetrical waveforms rising is accelerated and falling slowed down to the same extent resulting in equal but opposite phase shift. The net shift is zero and the resulting zero-crossing will coincide with the zero-crossing of the original waveform. Although a noise source is present it does not lead to jitter or phase noise.
For asymmetrical waveforms the situation is different. Exemplarily Fig. 2.23 considers a waveform with fast rising and slow falling. Due to fast rising of the original (asymmetric) voltage the noise current can accelerate the loading of the capacitance only marginally, the introduced phase shift is small. However at the long falling transition the influence of the noise current is significant leading to a large phase shift. More generally, in asymmetrical waveforms the phase shift introduced during rising and falling is not equal and therefore the zero-crossings are shifted leading to observable jitter and phase noise.

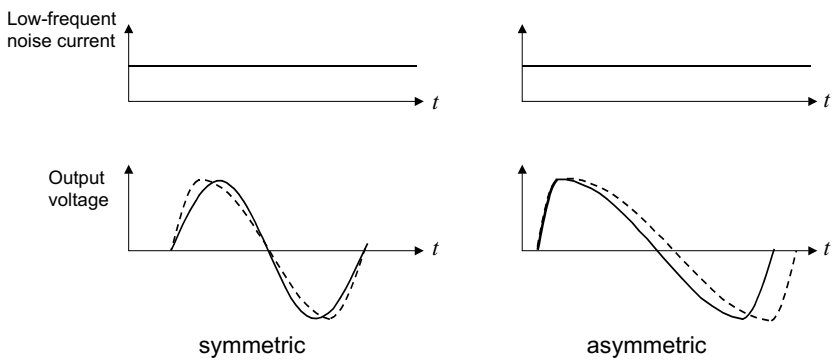

Figure 2.23: Influence of asymmetry in the signal waveform on upconversion of flicker noise. Solid line: waveform without noise, dashed line: waveform with noise.

The non-linearities leading to asymmetrical waveforms can be introduced by the large capacitance variations of the varactors especially at low tuning voltages (large C_{av}).
Interestingly the corner frequency of the $1/f$ noise of the transistors is not identical to the $1/\Delta f^3$ corner in the phase noise [16], but

$$\Delta f_{1/\Delta f^3} = c f_{1/f}. \tag{2.30}$$

The factor c is always smaller than 1 and can be significantly decreased if the waveform of the oscillation is made more symmetric. Thus the inferior $1/f$ device noise in CMOS transistors compared to their bipolar counterparts does not necessarily imply poor close-in phase noise performance, but can be compensated by proper design [30].

Optimization of phase noise

Reduction of phase noise can be achieved in several ways, besides the above described increase of symmetry in the waveform. First, increasing the signal power by maximizing the signal swing of the output signal is advantageous (see page 34). The second strategy is to increase the quality factor Q_{LC} of the tank to reduce the influence of white thermal noise (see page 35). Basis for the latter optimization is either the quality factor according to bandwidth or phase stability considerations (Fig. 2.24). Both quality factors lead to comparable results [31].The quality factor according to bandwidth definition relates the center frequency of the oscillators amplitude response to its 3dB-bandwidth. With higher Q_{BW}, i.e. smaller bandwidth, oscillations at offset frequencies are more effectively damped.

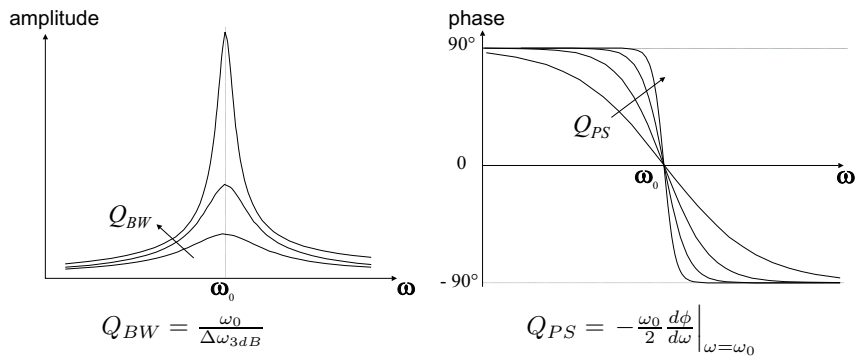

Figure 2.24: Definition of quality factor according to bandwidth and phase stability criterions.

The quality factor according to phase stability definition relates to the nor-

malized slope of the phase transfer function. Introduced phase lags or leads have to be compensated by a change in instantaneous frequency. For a given phase shift the required frequency change is smaller with higher Q_{PS}: the oscillation frequency is more stable and phase noise lower.
The phase stability definition [31]

$$Q_{PS} = -\frac{\omega_0}{2}\frac{d\phi}{d\omega}\bigg|_{\omega=\omega_0} = -\frac{\omega_0}{2}\frac{d}{d\omega}\left[\arctan\left(\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})}\right)\right]\bigg|_{\omega=\omega_0} \tag{2.31}$$

yields [21] after lengthy calculations

$$Q_{PS} = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{L}{R}\frac{1}{\omega_0}. \tag{2.32}$$

According to this equation increasing the ratio L/R increases the quality factor of the tank. This is the same result as found for the optimization of power consumption (page 30).
This implies that highly tunable varactors can be used to increase the VCO frequency tuning range or to decrease power consumption and phase noise by enabling the use of a higher tank inductance.

Impact on PLL noise

PLL noise is mainly determined by noise introduced by the reference signal and the VCO. In the context of this work only VCO noise is of interest. A thorough analysis of the transfer characteristic and loop response to noise signals shows that the PLL functions as high-pass for the noise from the VCO [38]. Above a cut-off frequency f_c, noise passes unattenuated. f_c is determined by the overall forward gain of the loop and the order of the divider [38]. Due to the existence of many adjacent channels specifications for the maximum PLL noise output have to be met. Fig. 2.25 compares the spectra of the VCO noise and the resulting PLL noise output.

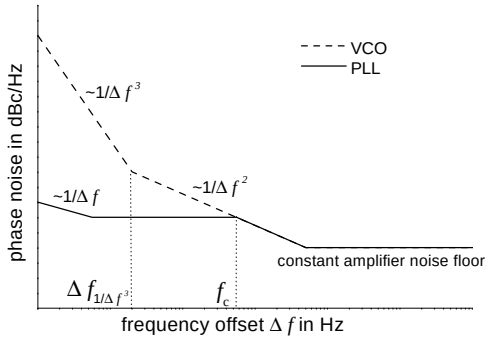

Figure 2.25: Noise spectra of the VCO and the resulting PLL output.

Below f_c the output characteristics are dominated by the PLL transfer function. Output noise is significantly reduced compared to the "input" from the VCO. Above f_c essentially the VCO noise will be observed.

Figure of merit

To compare VCOs in different technologies and with different designs, the normalized phase noise has been defined [56] as a figure of merit (FOM) for VCOs

$$\mathrm{FOM} = \mathcal{L}(f_0, \Delta f) + 10\log\left(\left(\frac{\Delta f}{f_0}\right)^2 \frac{P_{VCO}}{[\mathrm{mW}]}\right). \tag{2.33}$$

$\mathcal{L}(f_0, \Delta f)$ is the single-side-band noise at the offset frequency Δf from the carrier frequency f_0. P_{VCO} denotes the total power consumption of the VCO in mW. The performance of a VCO is regarded to be better with higher absolute value of the figure of merit.

Chapter 3

MOS Varactors

This chapter presents the design and measurement results of proposed A-mode and I-mode varactors.
First an overview over test structures, technologies, measurement environment and methodology is given.
Then A-mode varactors using STIs within the device and versions with n^+ and p^+ regions are covered in standard CMOS as well as BiCMOS technologies.
The proposed A-mode varactor is compared to conventional A-mode varactors and the gate length dependent performance of devices with STI and conventional varactors is investigated. Further the influence of the polysilicon gate doping on the performance of a MOS varactor is discussed. The properties of an A-mode varactor with lateral contact offset are also described. I-mode varactors with deep/source drain in standard CMOS technologies are introduced. The influence of the frequency on the proposed varactors is explained.

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3.1 Design of A-mode and I-mode MOS varactors

As described in section 2.1 all accumulation mode varactors are realized as PMOS capacitors in n^- well (see Fig. 2.6).
The I-mode devices of section 3.1.5 and 3.2.9 are based on conventional NMOS varactors.

3.1.1 A-mode varactors with STI in CMOS technology

Design with STI

To avoid overlap of gate and n^+ regions as in conventional A-mode varactors STIs are inserted between the active area beneath the gate and the well contacts. Traditionally STIs are not used within a device, but between active devices or wells to provide isolation or prevent latch-up.
Both types of varactors and the relevant capacitances are shown in Fig. 3.1.

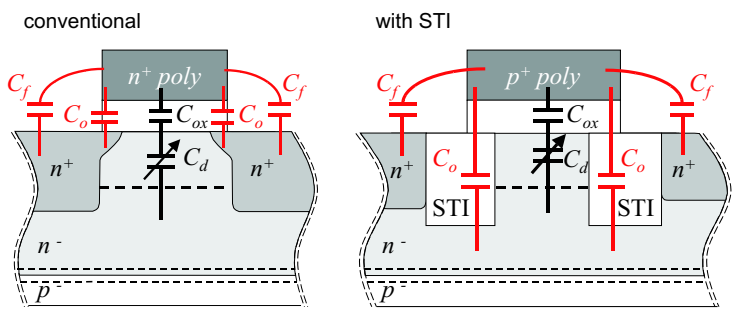

Figure 3.1: Cross sections of a conventional A-mode varactor and one with STIs. The relevant capacitances in depletion are shown.

The series connection of the oxide capacitance C_{ox} and the depletion region capacitance C_d forms the variable capacitance. Parasitic capacitances are

comprised mainly of overlap and fringing capacitances. The overlap capacitances C_{ov} of conventional MOS varactors are determined by the gate oxide thickness, in the proposed varactor by the STI thickness. The considerably (approx. 50 times) thicker STIs lead to reduced overlap capacitances.
Further with STI the well contacts are at a greater distance to the poly gate as in the conventional accumulation mode varactor. Since this distance determines the fringing capacitances C_f the conventional devices with smaller distance show higher fringing capacitances.
As the STIs reduce both types of parasitic capacitances considerably the capacitance tuning range C_{max}/C_{min} strongly increases, because

$$\frac{C_{max}}{C_{min}} = \frac{C_{var,max} + C_{parasitics}}{C_{var,min} + C_{parasitics}}. \tag{3.1}$$

The values $C_{var,max}$, $C_{var,min}$ denote the maximum, minimum values, that are possible by the series connection of C_{ox} and C_d.
Further particular importance is attached to the minimum quality factor (page 14) and therefore to the resistances of the devices. Fig. 3.2 shows the situation at minimum quality factors and the relevant resistances of a conventional and an A-mode varactor with STI.

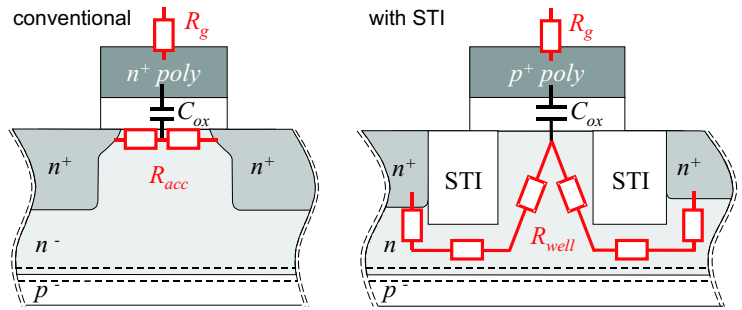

Figure 3.2: Cross sections of a conventional A-mode varactor and a proposed device with STI and the relevant resistances in accumulation.

The minimum quality factor of both types occurs in accumulation when the maximum capacitance is achieved. With STI the resistance is given by the path from the accumulation layer through the n^- well to the well

contacts. Therefore not only the capacitance but also the resistance is at its maximum in accumulation. The disadvantage of the long path is to some extent aggravated by the relative low doping of the n^- well. Thus somewhat reduced quality factors compared to the conventional device are expected.

p^+ connections

Holes that are thermally generated in the depletion region eventually form an inversion layer. As this inversion layer is electrically isolated and there is no reservoir for holes, the charge in the inversion layer can not follow the high frequent signal at the gate. The capacitance will not increase to the large value determined by the gate oxide capacitance (as in accumulation). However, the inversion layer will keep the depletion region from extending further, leading to a slightly increased minimum capacitance compared to the situation without inversion. Fig. 3.3 describes a possibility to prevent inversion.

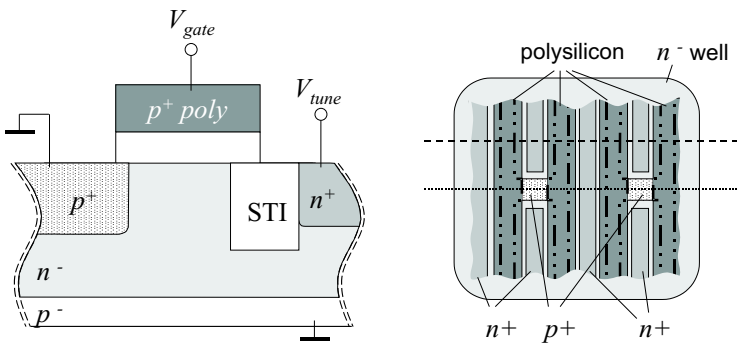

Figure 3.3: Cross section of the A-mode varactor with STI where a p^+ connection is realized (left). Layout example (right). Dot-dashed line: border between thick and thin oxide, dotted line: area where cross section with p^+ regions is present, dashed line: area of the main cross section with STIs and n^+ regions at both sides of the gate (as in Fig. 3.1(right)).

At few points along the gate (once at each finger) the STI and n^+ region at one side of the active area are replaced by small, grounded p^+ regions. These

p^+ regions will extract the positively charged holes and the device reaches deep depletion instead of inversion and features a lower overall minimum capacitance [45]. The layout example shows how the small p^+ regions can advantageously be included in the layout.
The size of the p^+ regions is chosen to be minimum, to increase the parasitic overlap and fringing capacitances only negligibly. Minimum size is sufficient, as the generation time of holes is very long compared to the period of the signal at the gate [36].

n^+ connections

Similarly to the p^+ connections described above, n^+ connections can be included in the layout. At few points along the gate the STI at one side of the gate is omitted and a laterally enlarged n^+ region touches the active area beneath the gate (Fig 3.4).

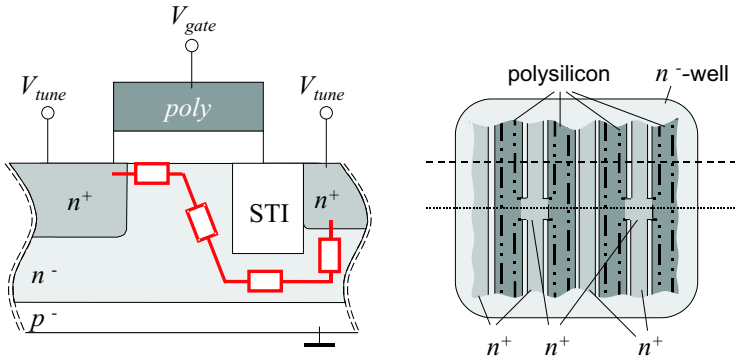

Figure 3.4: Cross section of the A-mode varactor with STI where a n^+ connection is realized (left). Layout example (right). Dot-dashed line: border between thick and thin oxide, dotted line: area where cross section with n^+ regions is present, dashed line: area of the main cross section with STIs and n^+ regions at both sides of the gate (as in Fig. 3.1(right)).

The purpose of the n^+ connections is to provide a low ohmic path in accumulation to increase the achievable minimum quality factor. To keep the

increase in parasitic capacitances negligible the width of the n^+ regions is chosen to be minimum. However, for quality factor reasons several n^+ connections per finger are more advantageous than only one.

3.1.2 A-mode varactor with STI in BiCMOS technology

The basic CMOS version of the varactors with STI showed increased series resistances compared to conventional A-mode or I-mode varactors. This drawback can be alleviated when using BiCMOS technologies. The fairly shallow n^+ implants forming the well contacts of the CMOS device are replaced by deep n^+ sinkers which are connected by a n^+ buried layer. These typical elements of any BiCMOS technology are generally used to form the collector node of *npn* bipolar transistors.
Without influencing the capacitances the resistances can strongly be reduced, as the n^+ sinkers feature a lateral outdiffusion underneath the STIs and their doping concentration is higher than that of the n^- well.
A BiCMOS version of the varactor with STI and its relevant resistances are compared to the CMOS version in Fig. 3.5.

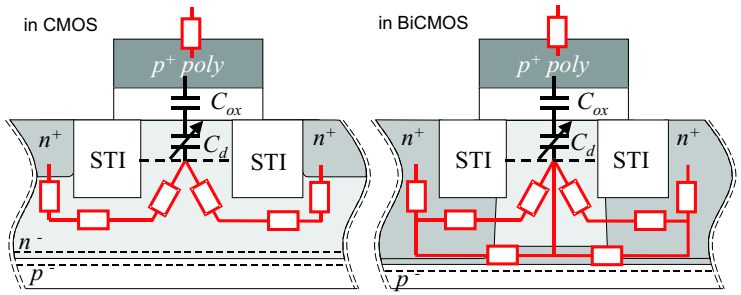

Figure 3.5: Cross sections and relevant resistances of the CMOS (left) and BiCMOS (right) version of the A-mode varactor with STI.

Part of the well resistance which is effective in the CMOS version can be neglected in the BiCMOS version, as it is within the highly doped n^+

sinkers. The also highly doped n^+ buried layer represents an additional parallel and low ohmic path, which can further reduce the resistance.
Attention has to be paid to the width of the STIs: it may not be less than the lateral outdiffusion of the n^+ sinkers, as then dopands would diffuse underneath the gate. Certainly n^+ and p^+ regions, as described for the CMOS varactors with STI, can improve the device in BiCMOS technology further.

3.1.3 A-mode varactor with lateral contact offset

One alternative method to reduce overlap capacitances is based on the varactor with STIs. It omits the STIs and leaves the n^+ regions at a certain distance to the polysilicon gate. The influence on the capacitance tuning range is expected to be small. The overlap capacitances are eliminated, but the fixed fringing capacitance $C_{f,fix}$ increases by a variable part $C_{f,var}$, which is small in depletion. At the same time the resistive path through the n^- well is considerably shortened and the quality factor improved. Fig. 3.6 depicts the cross sections and the relevant resistances and capacitances of the designs with STI and the described lateral contact offset in depletion. The reduction in series resistance is obvious.

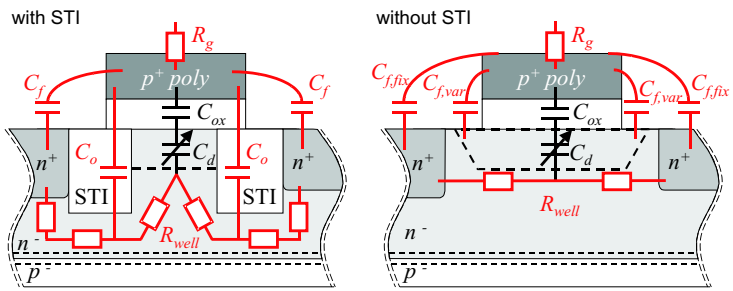

Figure 3.6: Cross sections and relevant resistances and capacitances of the A-mode varactor with STI (left) and with lateral contact offset (right). Dashed lines indicate borders of depletion regions.

Evidently p^+ and n^+ connections (as described before) can be used to improve the behaviour of the device with lateral contact offset.

3.1.4 A-mode varactor without LDD

Besides lateral contact offset another method to reduce overlap capacitances is based on the conventional transistor structure. It omits the LDD regions (lightly doped drain) [61], that are situated adjacent to source and drain and shorten the effective channel length. LDDs were introduced in short (sub-μm) transistors to lower the maximum lateral electric field between source and drain, which helps to reduce hot electron effects [35]. To achieve this behaviour LDDs are of the same type of doping as the source/drain, but the dopand concentration is considerably lower.
In varactors there is no lateral field between source and drain, so it is safe to omit the LDDs, which are electrically a part of the source/drain. The benefits are reduced overlap between gate and source/drain and lower overlap capacitance. A disadvantage is increased series resistance due to the larger gate length.

3.1.5 I-mode varactors with deep source/drain

Contrary to the conventional NMOS varactor the I-mode varactors with deep source/drain use not only the regular, shallow and highly doped source/drain implants, but also an additional n^- well to form a deeper source/drain region. The tuning voltage alters the onset of inversion but also controls the width of depletion regions around the n^- wells. Touching depletion regions reduce the minimum capacitance. Optional STI regions reduce parasitic capacitances. The different I-mode varactors in CMOS technology - conventional NMOS, varactor with deep source/drain and optional STI - are shown in Fig. 3.7.

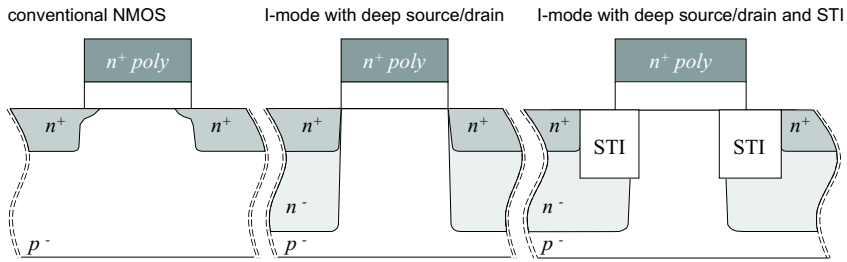

Figure 3.7: Cross sections of conventional I-mode varactor and I-mode varactors with deep source/drain.

When the tuning voltage, applied to the n^+ regions and the n^- wells is increased, the depletion regions around the n^- wells expand and spread out laterally under the gate (Fig. 3.8 exemplarily without STIs).

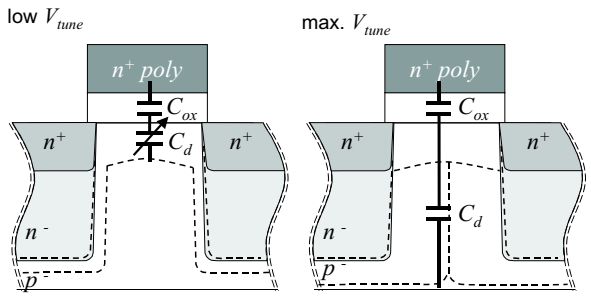

Figure 3.8: Depletion regions in the I-mode varactor with deep source/drain at low tuning voltages (left) and maximum V_{tune} (right). Dashed lines indicate borders of depletion regions.

At some tuning voltage the depletion regions around adjacent n^- wells touch and totally deplete the area beneath the gate at least to the depth of the n^- wells (Fig. 3.8(right)). This results in a very low minimum capacitance and therefore high capacitance tuning range. Without STIs the minimum quality factor will remain unaltered compared to the conventional NMOS

varactor, as it is determined by the same parameters.
Attention has to be paid to the doping of the p^- region and the distance between the n^- wells. They must have values that lead to sufficient wide depletion regions, but avoid too wide outdiffusion of the n^- wells.
When using STIs it is necessary to introduce n^+ connections as described for the A-mode varactors. They are essential to provide the electrons for inversion at high frequencies and to thereby reach the maximum capacitance.

3.2 Experimental results

3.2.1 Test structures and technologies

The MOS varactors, inductors and VCOs described in this work have been designed in standard digital CMOS and BiCMOS technologies of *INFINEON Technologies* with minimum feature sizes of 0.25μm (*c9n*, *b9c*) and 0.12μm (*c11n*). The 0.25μm technologies offer four metal layers of aluminum, whereas the 0.12μm CMOS technology features six copper layers. All technologies provide STIs (Shallow Trench Isolations) to isolate adjacent active devices and prevent latch-up.
The supply voltage (V_{dd}) in the 0.25μm technologies is 2.5V and is reduced to 1.5V for the 0.12μm CMOS technology.
All varactors employ multifinger layout, which is common for RF transistors to reduce gate resistances. Although the gate width may be large, a single finger is often less than 10μm long, but many fingers are connected in parallel (see page 10). Furthermore, the gate fingers are contacted at both ends to reduce the resistance by $\frac{1}{4}$ compared to connections at one end only.
Fig. 3.9 shows a die photograph of a proposed varactor with STI and an enlargement of part of its layout. All varactors are realized in metal 1...4 only. Metal routing is based on several considerations. All regions (polysilicon gate, p^+, and n^+ diffusions) need to be contacted. The contacts connect all regions to metal 1. Therefore no routing can be realized in metal 1 in order to avoid shorts. Polysilicon contacts are only allowed above thick oxide, i.e. along the connections between the individual fingers. Thus wiring of the polysilicon places no difficulties as the connections between the fingers do not cross with n^+ or p^+ diffusions. For the gate connections

all metals (1-4) are connected in parallel to reduce series resistance. Metal 2 features the highest sheet resistance and smallest distance to poly. It is therefore not used for the tune input, but with minimum width only for the p^+ connections. The n^+ diffusions are wired in metal 3 and 4 to achieve low resistance but simultaneously also low capacitance to the gate fingers (which need to be crossed).
Outside of the varactor the gate and drain wiring is realized in metal 3 and 4 only to avoid large capacitances to ground (substrate).

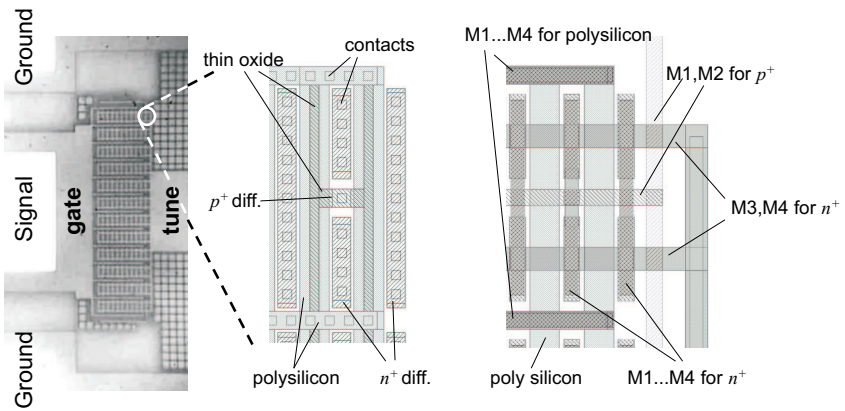

Figure 3.9: Die photograph of a proposed A-mode device with STI and p^+ regions and enlargement of part of its layout, showing different mask layers.

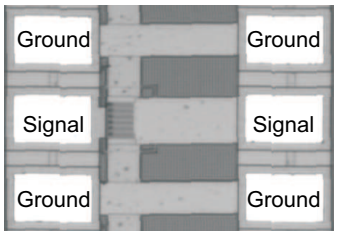

Figure 3.10: GSG environment of test structures.

All devices (varactors and inductors) are tested in a GSG (ground-signal-ground) test structure with a pitch of 100μm (Fig. 3.10). The two signal pads allow applying a voltage to the gate and to tune the shorted source/drain or well contacts. The p^- bulk (substrate) is connected to ground.
Where not mentioned explicitly devices have been fabricated in the 0.25μm technologies.

3.2.2 Measurement methodology

All devices have been tested on-wafer. The thermo chuck of a *Cascade Microtech* Microchamber supported the wafer and *Cascade Microtech* copper-beryllium air co-planar probes (100μm pitch) were used to contact the test structures. Tungsten probes have not been used, as the measurement time for each varactor was relatively long (up to 40min.) and the contact resistance of tungsten probes increases significantly over time [60]. Operating points of the devices were adjusted with a *HP4156* DC parameter analyzer and S-parameter measurements were performed with a *HP8510* network analyzer at each operating point.
Due to higher accuracy hardware calibration (Short-Open-Load-Thru) was preferred over software calibration (isolation omitted). A *Cascade Microtech* standard impedance (ceramic) substrate with laser trimmed 50Ω resistance provided the standards for calibration. The open was not realized by lifting the probes off the substrate, but by gently pushing them onto the ceramic substrate. This mimics the placement of the probes during later measurements better.
The *Agilent Technologies* Software *IC-CAP* was employed to gather and analyze the data.

Extraction of parameters

For extraction of parameters the varactor is considered as series connection of a resistance R and a capacitance C (Fig. 3.11(right)). This is a generally accepted simplification compared to the more realistic situation of additionally a parallel, parasitic capacitance C_p and a constant gate resistance R_g in series (Fig. 3.11(left)).

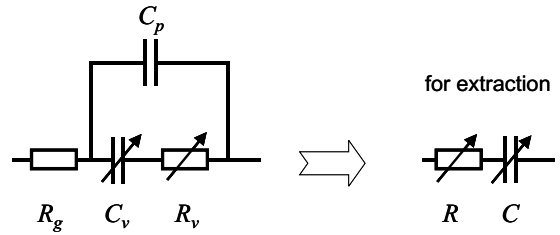

Figure 3.11: A simple realistic model (left) of a MOS varactor and the most simplified case for extraction (right).

After de-embedding (Appendix B.2) and based on the simple model effective values for the capacitance and series resistance are extracted from the measured S-parameters by

$$\begin{aligned} C &= -(2\pi f \mathrm{Im}(\tfrac{1}{Y_{11}}))^{-1} \\ R &= \mathrm{Re}(\tfrac{1}{Y_{11}}) \end{aligned} \tag{3.2}$$

with f the frequency. Furtheron "measured resistance of the varactor" or "measured capacitance of the varactor" relates to theses effective values.
The resulting quality factor is obtained from Eq. 2.8 by

$$Q = \frac{1}{2\pi f RC} = -\frac{\mathrm{Im}(\frac{1}{Y_{11}})}{\mathrm{Re}(\frac{1}{Y_{11}})} \tag{3.3}$$

The relationship between S and Y parameters is given in Appendix A.

Influence of simplified model on extracted parameters

The model simplification for parameter extraction leads to the following probable results for the extracted (effective) series resistance and capacitance:

- frequency dependent values for R and C

- depending on the real values of the capacitances the effective resistance can be significantly different compared to its real value

  For example: if the parasitic capacitances C_p are high compared to the variable capacitance C_v the parallel path to the resistance R is low-ohmic and the effective resistance appears lower. This resistance-lowering effect is more pronounced in depletion, when the variable capacitance is low.
  These effects are frequency dependent.

The effective values for resistance and capacitance extracted with the model of one capacitance and one resistance in series will be used in this work.

3.2.3 Comparison of A-mode varactor with STI and conventional A-mode varactor

This section compares the A-mode varactor with STI with conventional A-mode varactors either with or without LDDs. Cross sections of all three devices are given in Fig. 3.12. Design data can be found in Table 3.1. The results of the performance comparison are shown in Fig. 3.13.

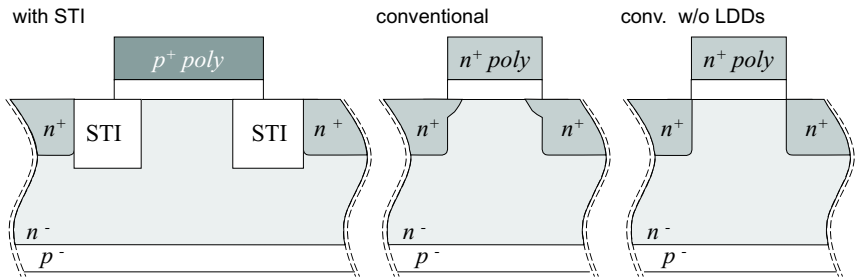

Figure 3.12: Cross sections of the proposed device with STI and conventional A-mode varactors either with or without LDD.

Table 3.1: Design data of the proposed device with STI and the conventional A-mode varactors either with or without LDDs.

	gate length	finger length	fingers	STI width	distance gate - n^+
with STI	0.32μm	8μm	120	0.49μm	0.16μm
conv.	0.35μm	3μm	96	n.a.	0μm
conv. no LDD	0.32μm	3μm	256	n.a.	0μm

The absolute as well as the averaged capacitance tuning ranges with STI are significantly higher than the values for the conventional A-mode varactor. The absolute value increases by nearly 50% (2.5 to 3.7), the averaged value by 26% (1.9 to 2.4). Although the device without LDDs offers some improvements, it is still outperformed by 10% (averaged) and 32% (absolute) higher tuning ranges. The better performance is the result of reduced parasitic capacitances with STIs.
The advantage of omitting LDDs is a 12% higher averaged and a 16% higher absolute capacitance tuning range compared to the device with LDDs. The reason is the voltage dependent behaviour of the n^- LDD regions. At zero tuning voltage and maximum gate voltage both, the LDD regions and the well beneath the gate show an electron surplus. Thus there is no difference in the maximum capacitance whether LDDs are present or not. At low gate voltage and maximum tuning voltage again both, the LDD regions and the well beneath the gate are depleted. However, due to the higher doping in the LDDs compared to the well the depletion region in the area of the LDDs is smaller and therefore the total capacitance larger than in the case without LDD regions. The same maximum, but larger minimum capacitance result and the conventional A-mode varactor with LDDs shows a lower capacitance tuning range.
The observation that the varactor with STI "looses" more capacitance tuning range by averaging than both of the conventional A-mode varactors is a result of the type of gate doping. With STI the polysilicon gate is p^+-doped whereas the gate of the conventional varactors is n^+ type. This shifts the transition voltage of the varactors with STI by the difference of the flatband voltages (ca. 1V) and explains the different averaging behaviour.

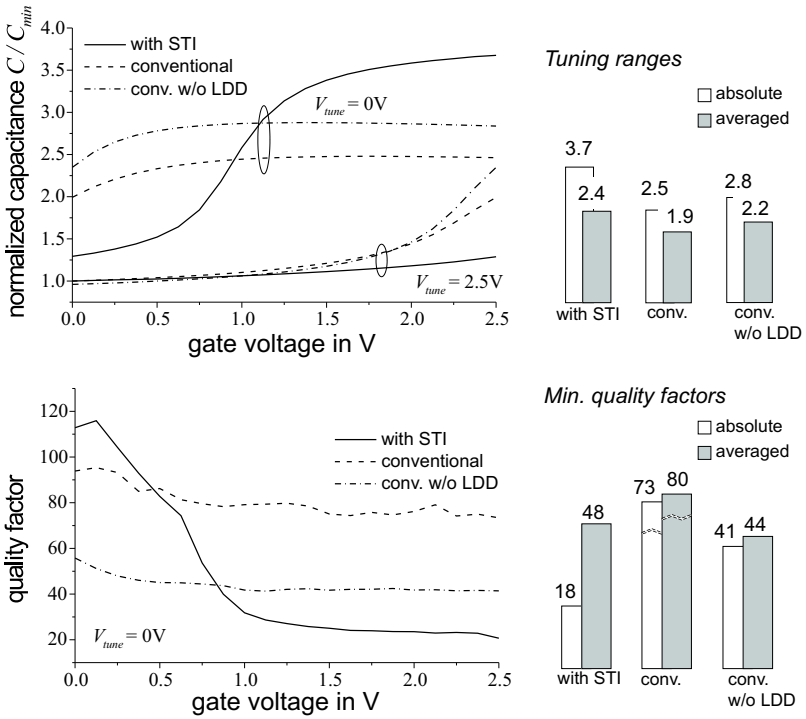

Figure 3.13: Comparison of the device with STI and the conventional A-mode varactors either with or without LDD ($f = 2$GHz). Left: Measured small-signal capacitance (normalized) and quality factor. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

For all three devices the minimum quality factors occur in accumulation, where both capacitance and resistance are at their maximum. Fig. 3.14 shows normalized (100μm gate width) resistances of the varactor with STI and a conventional A-mode varactor.
With STI the resistance is larger due to the relatively long path through the lowly doped n^- well. Further the resistive path is restricted by the STIs and additionally longest in accumulation. Therefore the resistance maximum occurs in accumulation. As the length of the path through the n^-

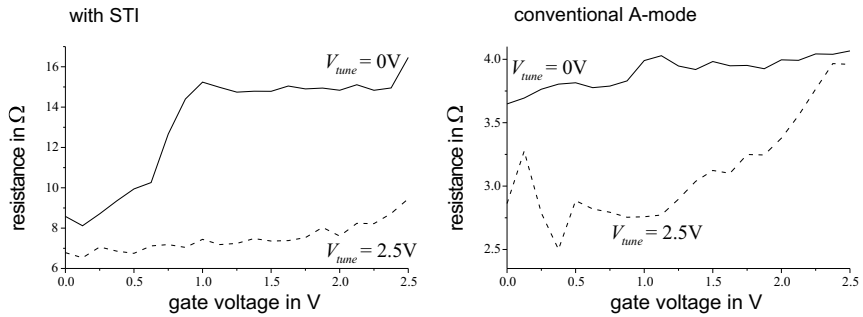

Figure 3.14: Measured and normalized (to 100μm gate width) small-signal resistances of the device with STI and a conventional A-mode varactor.($f = 2$GHz).

well is altered by the depth of the depletion region, the resistance decreases monotonically with decreasing gate or increasing tuning voltage.
Although it is expected that the accumulation layer is low ohmic, the conventional A-mode varactors feature the largest resistance in accumulation also. There are several reasons for this behaviour. The channel doping is buried and with increasing depth the doping increases monotonically up to the maximum depth of the depletion region, i.e. the specific resistance of the semiconductor material is higher at the surface. Though the number of electrons is strongly increased in accumulation the mobility is severely impaired by surface effects and strong vertical fields due to the high gate voltage.
As a result of the different resistances the minimum quality factor with STI is significantly lower. It reaches absolute 18 instead of 73 and averaged 48 instead of 80 for the conventional A-mode varactor.
When omitting the n^- LDDs, which are higher doped than the n^- well, the average doping along the accumulation region decreases and therefore the resistance increases with an adverse effect on the quality factor. Compared to the varactor with LDDs, the absolute minimum quality factor is reduced to 41 and the minimum averaged value drops to 44, which is less than the value for the device with STI.
The quality factors of all varactors, inlcuding the one with STI, are well above the maximum 3dB-quality factor of typical integrated inductors in this 0.25μm technology, which is below 10. Thus no matter what type of

varactor will be used in a fully integrated VCO, the inductor and not the varactor will determine the minimum quality factor of the complete *LC*-tank. Hence it is expected that the proposed devices with advantageously higher capacitance tuning range can be used without deteriorating the VCO phase noise, that results from thermal noise.

3.2.4 Gate length dependent performance of A-mode varactors with STI and conventional MOS varactors

In this section first the influence of the gate length on the performance of the proposed varactors with STI is described. Then the findings are compared to the behaviour of conventional varactors.

3.2.4.1 A-mode varactors with STI

To test the influence of the gate length A-mode varactors with STI (Fig. 3.1) with 0.32μm and 0.64μm gate length are compared (Table 3.2). For the long device the gate is only half as wide to keep the gate area equal. As there is only one shared p^+ region per gate finger, the varactor with short gate length has twice the number of p^+ connections (p^+ in detail in section 3.2.6).

Table 3.2: Devices to test the influence of the gate length on A-mode varactors with STI.

	gate length	finger length	fingers	STI width	distance gate - n^+	p^+ conn.
short	0.32μm	16μm	60	0.49μm	0.16μm	1 x 0.64μm
long	0.64μm	16μm	30	0.49μm	0.16μm	1 x 0.64μm

Fig. 3.15 displays the measurement results of both varactors.
The varactor with short gate length shows higher capacitance in accumulation as well as in depletion, with a more pronounced difference in depletion.

This can be explained by a lower constant parasitic but larger variable capacitance in the longer device. The varactor with 0.64μm gate length is only half as wide and has therefore only half the parasitic capacitances. Further edge effects with inhomogeneous electric field lines [55] always reduce the effective gate area and variable capacitance. Due to only half the gate width the long varactor suffers less from this reduction effect and features the higher variable capacitance.
Even with STI the parasitic capacitances are large enough to hold a potential for improvement. Doubling gate length and thereby reducing parasitic capacitances increases the absolute capacitance tuning range by 30% from 4.1 to 5.3. Even $C_{av,ratio}$ is almost 21% higher (3.1 compared to 2.6).
The resistance of the longer device is noticeable higher, especially in accumulation. Its gate resistance is only slightly higher ($\approx$ 60mΩ) because of the lower number of fingers (Eq. 2.5).
But the following equation describes the total well resistance

$$R_{well} = \frac{R'_w}{l_f N_F} \tag{3.4}$$

with R'_w the well resistance per μm width, l_f the finger length, and N_F the number of fingers. Two effects have to be considered when increasing the gate length. First the lower number of gate fingers and second the different R'_w.
Assuming equal resistance per μm width, halved N_F would lead to a twice as high maximum resistance. As this is not observed R'_w must counteract. Differences in resistance per μm result from the resistance between the STIs only, as all other parts of the path are identical in both devices. The resistance between the STIs experiences a larger cross section with longer gate, which leads to a resistance reduction. This reduction due to larger cross section outweighs the influence of the increased path and the resistance per μm width is lower for the longer varactor. Consequently the total well resistance is less than twice as high as the short varactor's resistance.
The measurements proof that with STIs increasing gate length strongly increases capacitance tuning range but imposes only slight reductions on the quality factor.

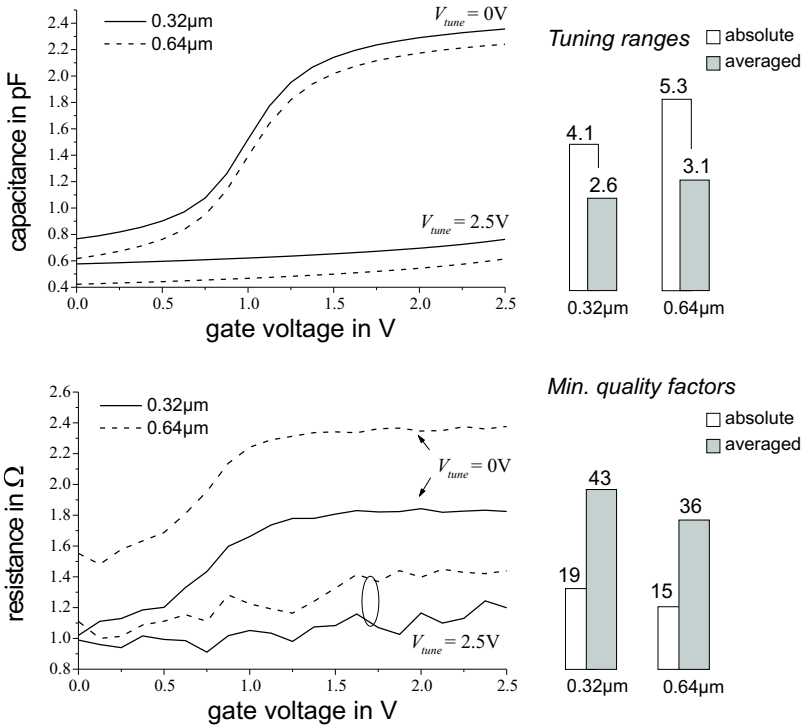

Figure 3.15: Comparison of the device with STI and either 0.32μm or 0.64μm gate length (f = 2GHz). Left: Measured small-signal capacitance and resistance. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

3.2.4.2 Comparison of A-mode varactors with STI and conventional MOS varactors

In MOS varactors the capacitance tuning ranges increase with increasing gate length. This is due to relatively decreasing parasitic capacitances. Therefore the objection might be raised that one simply has to increase the gate length of a conventional varactor to reach the capacitance tuning range of varactors with STI at perhaps higher quality factors. Therefore the gate length dependent performance of the proposed devices with STI and

conventional varactors is investigated with the help of four devices. Two devices with STI and gate lengths 0.32μm and 0.64μm and two conventional NMOS varactors with gate lengths 0.35μm and 1.05μm are compared (Table 3.3).

Table 3.3: Devices to compare the influence of the gate length on conventional varactors and devices with STI.

	gate length	finger length	fingers	STI width	distance gate - n^+	p^+ conn.
with STI, short	0.32μm	8μm	120	0.49μm	0.16μm	1 x 0.64μm
with STI, long	0.64μm	8μm	60	0.49μm	0.16μm	1 x 0.64μm
conv. short	0.35μm	3μm	96	n.a.	0.0μm	n.a.
conv. long	1.05μm	3μm	24	n.a.	0.0μm	n.a.

The relative reduction of parasitic capacitances with increasing gate length l_g holds for both types of varactors. Therefore increasing capacitance tuning ranges are expected and observed for each type. Beyond this the total capacitance is approx. $\propto l_g$ (at constant gate width).
For the quality factor differentiating between the two varactor types is necessary. In conventional varactors the maximum resistance is approx. $\propto l_g$ (at the onset of inversion/in accumulation). Therefore the minimum quality factor will decrease with l_g^{-2}. In the varactors with STI the length parameter which is important for the resistance is not the gate length but the total length of the path around the STIs. E.g. doubling the gate length does not lead to a twice as long resistance path. Additionally with increasing l_g the resistance which is restricted between the STIs experiences a larger cross section. If the resistance reduction due to this larger cross section outweighs the influence of increased path length the total resistance can drop although the gate length is increased (at constant gate width).
The relevant measurement results for capacitance tuning range and minimum quality factors are summarized in Fig. 3.16.
The increase of capacitance tuning range with gate length is very clear for both types of varactors. However, even with 1.05μm gate length the NMOS can not reach the high values that the STI-design offers with the much shorter gate length of 0.64μm.
Additionally the NMOS's quality factor suffers strongly from the gate length

increase. With three times longer gate Q_{min} drops approx. by a factor of $3^2 = 9$ from 43 to 5. The averaged value decreases from 73 to 20. With STI the quality factors remain not only nearly unchanged at doubling the gate length but the 0.64μm device features higher quality factors than the long NMOS varactor.
This proofs that at longer gate lengths the varactors with STI allow simultaneously higher capacitance tuning ranges and higher quality factors than conventional varactors.

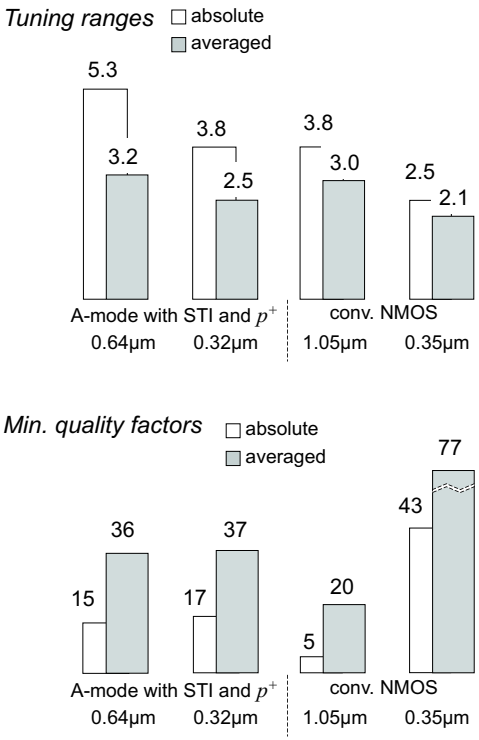

Figure 3.16: Measured capacitance tuning ranges and minimum quality factors of proposed devices with STI and conventional NMOS varactors at different gate lengths.

3.2.5 Influence of the polysilicon gate doping on varactor performance

The use of STIs makes it possible to choose gate doping independent of the doping of the source/drain (in I-mode varactors) or the well contacts (in A-mode varactors).
In this section the influence of the polysilicon gate doping on the characteristic of the A-mode varactor with STI is investigated. Three CMOS devices with identical design (Table 3.4) are compared in 0.12μm technology.

Table 3.4: Devices with STI to test the influence of the gate doping.

gate length	finger length	fingers	STI width	distance gate - n^+	p^+ conn.
0.32μm	6.6μm	50	0.33μm	0.16μm	1 x 0.28μm

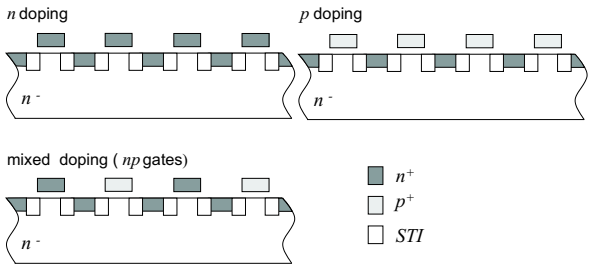

Figure 3.17: Cross sections of the three varactors with different gate doping.

In two devices all fingers are either homogeneously n- or homogeneously p-doped. In the third device gate fingers are alternating n- and p-doped. Fig. 3.17 shows schematic cross sections of all three devices. Fig. 3.18 summarizes measurement results.
Differences between the three devices are readily explained by the shift in flat-band voltage introduced by the different gate doping. For n-type polysilicon the flat-band voltage is low (close to 0V), but is shifted by ca. 1V when using p doping for the gate. The varactor with mixed gate doping

(50% n, 50% p) resembles the behaviour of two parallel varactors with half the gate width but different gate doping. Its capacitance is an average between the two varactors with entirely n- and p-doped gates: there are two, less high and less steep "stages" of transition, one at the transition voltage of the half with n gates, one at the transition of the half with p gates.

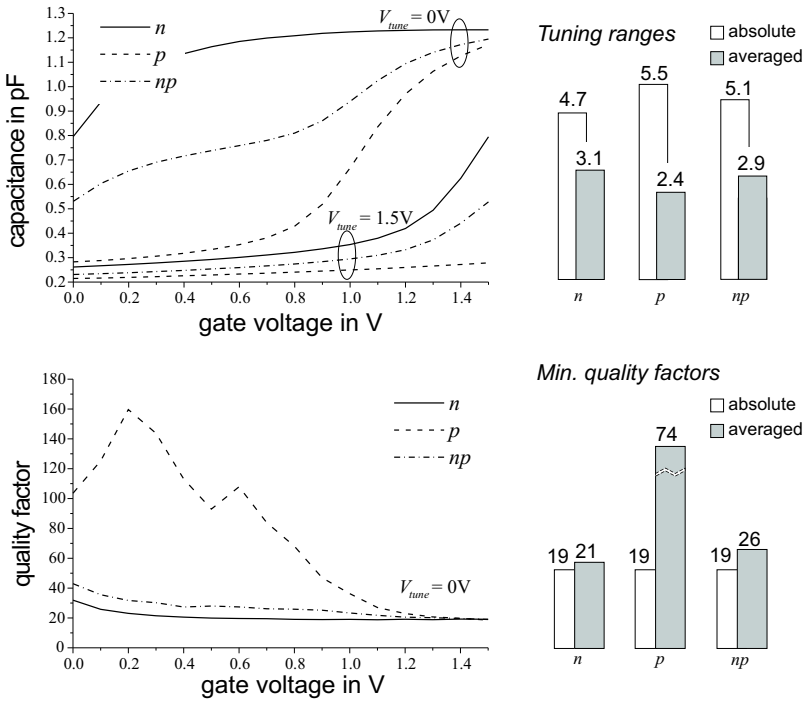

Figure 3.18: Comparison of the A-mode varactors with STI and different gate doping (f = 2GHz). Left: Measured small-signal capacitance and quality factors. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

At zero tuning voltage all varactors reach accumulation and their maximum capacitance is determined by the gate oxide and the parasitic capacitances. At the maximum tuning voltage of 1.5V all varactors remain in depletion for

a wide range of gate voltages. Only close to V_{gate} = 1.5V the capacitance of the varactors with n and mixed doping increases at the onset of accumulation.

The varactor with p gates reaches the highest capacitance tuning range (5.5), as it remains in deep depletion throughout the whole gate voltage range (at V_{tune}=1.5V) and therefore has a very low minimum capacitance. However, the averaged value $C_{av,ratio}$ = 2.4 is considerably lower than the absolute value, as the averaging process strongly reduces the maximum averaged capacitance. The varactor with n gates suffers less from averaging, and the absolute tuning range of 4.7 is only reduced to 3.1 after averaging. Naturally the varactor with mixed gate doping reaches values 2.9 (averaged) and 5.2 (absolute) between the two other devices.

The absolute minimum quality factor of all varactors is equally 19, as Q_{min} occurs for all devices in accumulation with comparable capacitances. The path through the n^- well determines the resistance in accumulation, where the type of poly is not important.

The shift in flat-band voltage for p gates and the flatter capacitance characteristic for mixed doping explains differences in minimum averaged quality factors. At V_{tune}=1.5V The varactor with p gates is in depletion for a wide range of gate voltages with a small capacitance and simultaneously a low resistance (shorter path through well) resulting in quality factors that are much higher than Q_{min}. Consequently there is a large difference between the absolute and averaged values. Contrary the n-doped varactor is for almost all gate voltages in accumulation with simultaneously high capacitance and resistance. The averaged quality factor differs little from the absolute value. Again the varactor with mixed gate doping reaches values between the other two devices: absolute 19 and averaged 26.

The aim of mixed doping is a smoother capacitance characteristic, which can be advantageous for VCO phase noise (confirmed in section 5.3). A parameter to measure this smoothness is the maximum slope of the capacitance with respect to the gate voltage dC/dV_{gate}. Exemplarily for tuning voltages 0V, 1.5V Fig. 3.19 depicts the slopes for all three varactors. Table 3.5 lists values for four tuning voltages. Due to the less steep two-transition behaviour mixed doping is an effective method to halve the maximum slope compared to homogeneously doped devices.

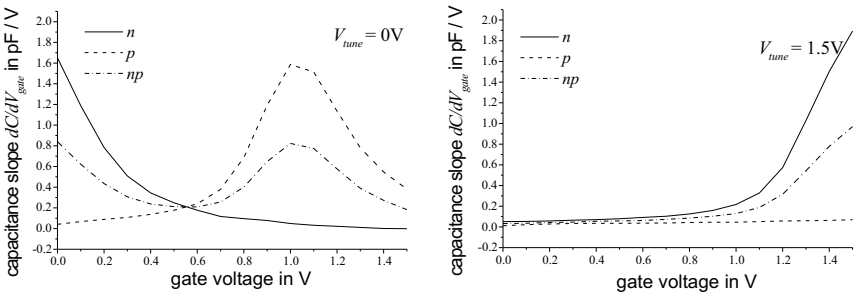

Figure 3.19: Capacitance slopes of the three varactors with different gate doping. Left: $V_{tune} = 0V$, right: $V_{tune} = 1.5V$. Values extracted from measurements.

Table 3.5: Maximum capacitance slope of the three varactors with STI and different gate doping (f =2GHz). Extracted from measurements.

	max. dC/dV_{gate} in pF/V		
V_{tune}	n	p	np
0.0V	1.65	1.83	0.84
0.5V	1.83	1.73	0.92
1.0V	1.83	0.14	0.92
1.5V	1.83	0.08	0.92

3.2.6 Variations of the A-mode varactor with STI

This section describes the influence of p^+, n^+ connections and the STI width on the performance of the A-mode varactors with STI.

Influence of p^+ connections on varactor performance

Otherwise identical A-mode varactors with STI, one with and one without p^+ connections are compared. Design data can be found in Table 3.6, cross sections on page 42. The width of the p^+ regions is minimum and always two polysilicon fingers share one p^+ connection (Fig. 3.3). Fig. 3.20 presents the measurement results.

Table 3.6: Devices to test the influence of p^+ connections.

	gate length	finger length	fingers	STI width	distance gate - n^+	p^+ conn.
with p^+	0.32μm	8μm	120	0.49μm	0.16μm	1 x 0.64μm
no p^+	0.32μm	8μm	120	0.49μm	0.16μm	no

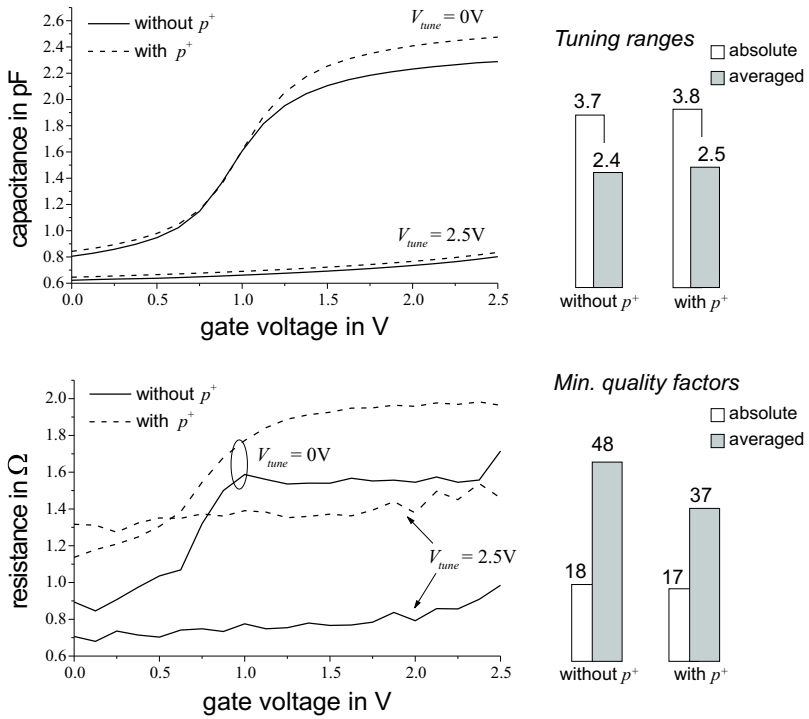

Figure 3.20: Comparison of the devices with STI and either with or without p^+ connections (f = 2GHz). Left: Measured small-signal capacitance and resistance. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

Despite the expectation that the p^+ regions allow deep depletion, the capacitance of the varactor with p^+ is higher not only in accumulation but also

in depletion. This is a result of increased gate area. Where p^+ regions are inserted only thin gate oxide instead of STIs is beneath the gate. In the results of the varactor without p^+ the influence of inversion (constant depth of depletion region) is not clearly visible, as the sweep of the gate voltage was too fast. Thus the varactor with p^+ regions features only slightly higher capacitance tuning ranges of absolute 3.8 instead of 3.7, and averaged 2.5 instead of 2.4.
However, from VCO measurements it can be concluded that the difference between the effective capacitance tuning ranges is larger than these measurements show (section 5.2). I.e. p^+ connections are more effective as it might seem from device measurements only.
The voltage dependent behaviour of the resistance of the device without p^+ regions has been explained in section 3.2.3 already. With p^+ regions the resistance is in accumulation as well as in depletion significantly higher. Where p^+ connections substitute the STI and the n^+ regions the resistance path within the n^- well (to reach n^+ regions) is lengthened. This increased path length results in higher resistances.
With p^+ the resistance at $V_{tune} = 2.5$V is higher than the resistance at $V_{tune} = V_{gate} = 0$V. A larger depletion region around the p^+ regions restricts the cross section between the STIs and also lengthens the path further.
The gate resistance of both devices is equal due to identical gate length, finger length and total gate width.
The different capacitive and resistive behaviour of the two devices results directly in different quality factors. Without p^+ connections the absolute minimum quality factor is slightly higher. After averaging the advantage of omitting the p^+ regions is more obvious: $Q_{av,min}$ increases by almost 30% (from 37 to 48).

Influence of n^+ connections on varactor performance

The purpose of inserting n^+ connections is to decrease the resistance in accumulation and thereby increase the minimum quality factors. Two otherwise identical devices with STI either with or without n^+ connections have been measured (Table 3.7). Two n^+ connections per finger are arranged symmetrically to the p^+ regions in the middle. Fig. 3.21 summarizes the measurement results.

Table 3.7: Devices to test the influence of n^+ connections.

	gate length	finger length	fingers	STI width	distance gate - n^+	p^+ conn.	n^+ conn.
with n^+	0.32μm	8μm	120	0.32μm	0.16μm	1x0.64μm	2x0.32μm
no n^+	0.32μm	8μm	120	0.32μm	0.16μm	1x0.64μm	no

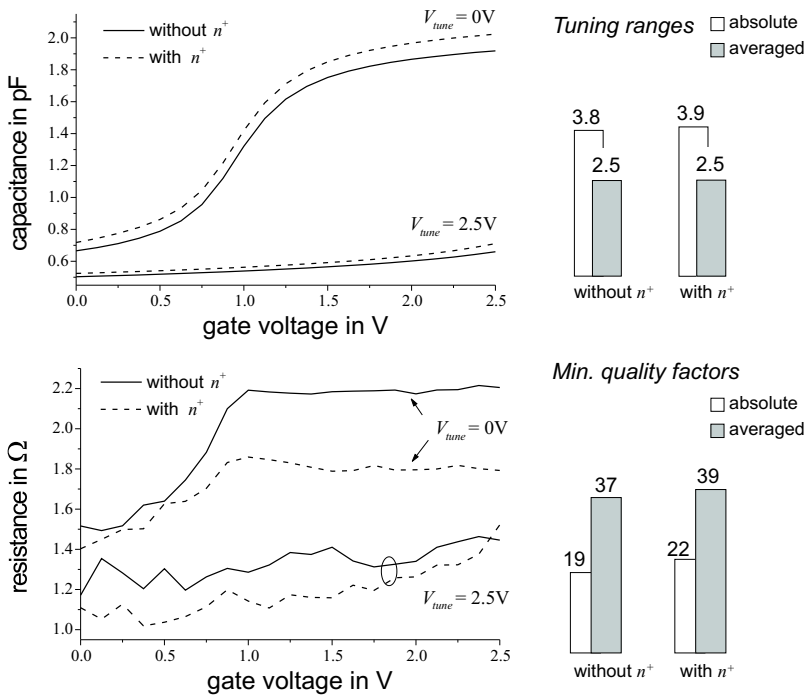

Figure 3.21: Comparison of devices with STI and either with or without n^+ connections (f = 2GHz). Left: Measured small-signal capacitance and resistance. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

Without n^+ connections the capacitance is smaller, and the difference between the two devices is larger in accumulation. An increased gate area

with n^+ connections explains this behaviour (similar to the case with p^+ regions). The n^+ connections leave the capacitance tuning range nearly unaltered at 3.8 (without) and 3.9 (with). The averaged capacitance tuning range remains unchanged at 2.5. I.e. the n^+ connections increase parasitic capacitances only negligible.
n^+ connections lower the total resistance significantly. As intended the largest difference of nearly 20% occurs in accumulation at the maximum resistance. The advantage is lower in depletion, as the total resistance is lower and hence the n^+ connections are less influential.
The gate resistance of both devices is equal.
The minimum quality factors, as shown in Fig. 3.21 (right), prove the effectiveness of the n^+ connections: the minimum quality factor increases from 19 to 22 and the averaged value from 37 to 39.
Measurements of further devices showed that improvement in quality factor is stronger for wider STIs. The reason is the increased total well resistance and thus the low ohmic parallel path through the n^+ connections has more influence.
It is expected that with more than one, perhaps smaller, n^+ connections per finger the quality factor improves further, as the average path within the accumulation region is shortened.

Influence of the STI width on varactor performance

The influence of the STI width is tested with one device having 0.32μm and an other device having 0.49μm wide STIs (Table 3.8). The distance between the polysilicon gate and the n^+ regions is kept constant. Therefore wider STI means also wider polysilicon overlap over STI.
Fig. 3.22 summarizes the measurement results.

Table 3.8: Devices to test the influence of the STI width. No n^+ connections have been used.

	gate length	finger length	fingers	STI width	distance gate - n^+	p^+ conn.
wide STI	0.32μm	8μm	120	0.49μm	0.16μm	1 x 0.64μm
narrow STI	0.32μm	8μm	120	0.32μm	0.16μm	1 x 0.64μm

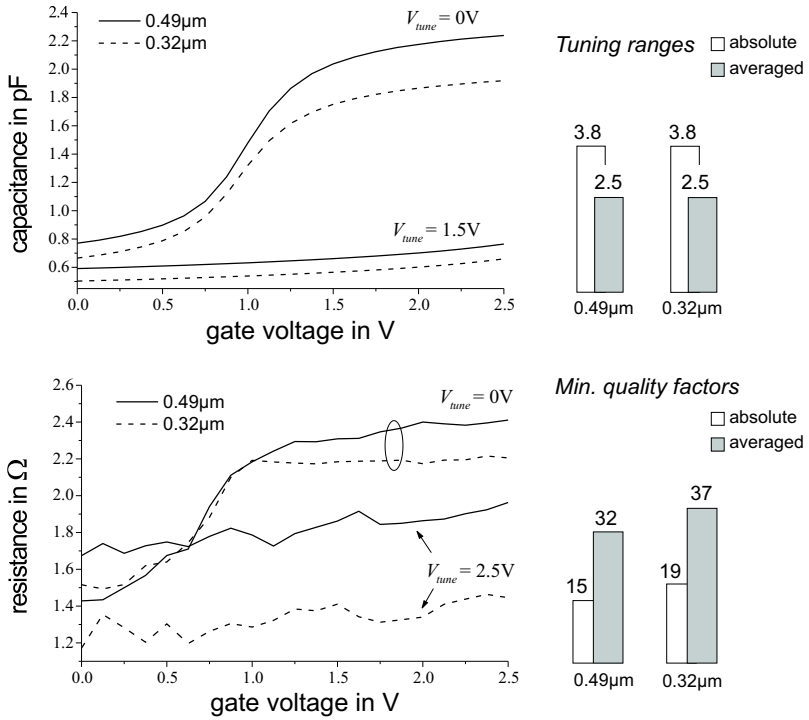

Figure 3.22: Comparison of devices with 0.49μm or 0.32μm wide STIs (f = 2GHz). Left: Measured small-signal capacitance and resistance. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

Higher capacitance with wider STI is the result of two effects. Larger overlap of the gate over the STIs increases parasitic overlap capacitances (from ≈50fF to ≈100fF) and leads to a larger gate area (same number of p^+ regions). Usually a gate area increase leads to an increase of capacitance tuning range, due to longer effective gate length. On the other hand higher parasitic capacitances decrease the tuning range. Nevertheless the results for both devices are identical, 3.8 (absolute) and 2.5 (averaged). Thus the difference in gate area is compensated by a change in overlap capacitances. This confirms the finding of section 3.2.4.2, that even in the proposed

type of varactors the overlap capacitances still hold some potential of improvement.
The total resistance of the device with narrower STIs is lower. Clearly the resistance path through the n^- well is shortened and the resistance beneath the STI reduced. Due to the lower "lateral" resistance the depletion regions around the p^+ regions have less influence at increasing tuning voltage. This explains the larger difference of resistances in depletion.
Gate resistances are negligibly different ($\approx$ 10mΩ).
The cross-over point in the resistance graph of the device with wider STI has been explained in this section on page 68.
As the capacitance as well as the resistance of the device with wider STI is higher, the minimum quality factors must be lower. In fact the wider STI leads to a Q_{min} of 15 instead of 19, and an averaged minimum quality factor of 32 instead of 37.

3.2.7 A-mode varactors with STI in BiCMOS technology

A BiCMOS version of the device with STI is compared to a CMOS version and a conventional A-mode varactor without n^- LDDs (Table 3.9).
As described in section 3.1.2 deep collector implants connected by the n^+ buried layer replace the shallow source/drain regions of the CMOS process (cross sections in section 3.1.2). Fig. 3.23 summarizes measurement results.

Table 3.9: A-mode varactors with STI in BiCMOS and CMOS technology and a conventional A-mode varactor for comparison. No n^+ connections have been used.

	gate length	finger length	fingers	STI width	distance gate - n^+	p^+ conn.	well contact
CMOS with STI	0.32μm	8μm	120	0.49μm	0.16μm	1x0.64μm	shallow source/drain
BiCMOS with STI	0.32μm	8μm	120	0.49μm	0.16μm	1x0.64μm	deep sinker+ buried layer
BiCMOS with STI	1.0μm	8μm	30	0.49μm	0.16μm	1x0.64μm	deep sinker+ buried layer
A-mode no LDDs	0.35μm	3μm	256	n.a.	0μm	n.a.	shallow source/drain

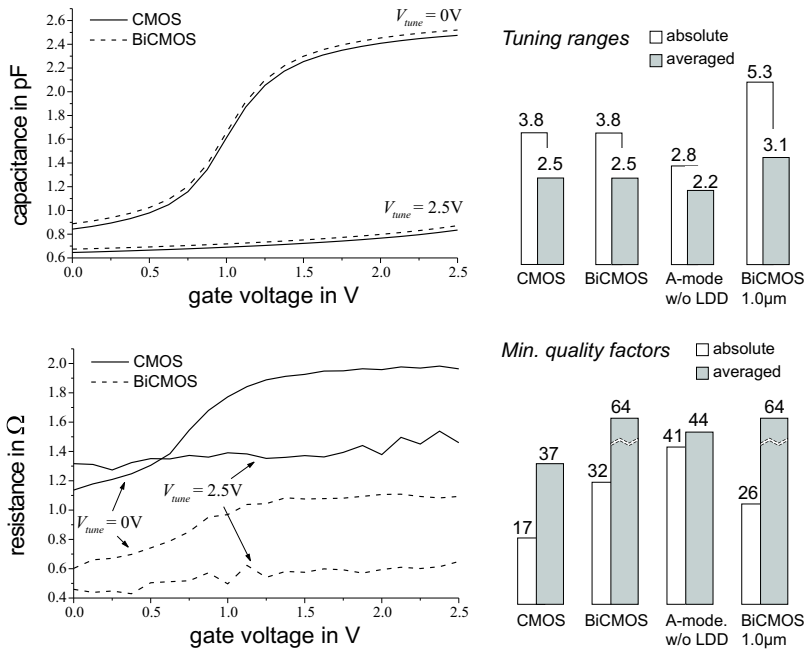

Figure 3.23: Comparison of the A-mode varactors with STI in BiCMOS and CMOS technologies (f = 2GHz). Left: Measured small-signal capacitance and resistance of the BiCMOS and CMOS versions with 0.32μm gate length. Right: Measured absolute and averaged tuning ranges and minimum quality factors of all devices; CMOS version (0.32μm), BiCMOS version (0.32μm and 1.0μm) and conventional A-mode varactor without LDDs (0.35μm).

The capacitance of the BiCMOS version is always a small amount higher than for the CMOS version. The difference is approx. the same in accumulation and in depletion, which can be explained by different wiring capacitances, as the distance between metal layers is different in the CMOS and BiCMOS technologies. Nevertheless, the absolute and averaged capacitance tuning ranges are identical with 3.8 and 2.5, respectively, which are considerably higher than the values for the conventional A-mode varactor without LDDs.
The BiCMOS version with larger gate length (less parasitic capacitances)

reaches an absolute capacitance tuning range of 5.3 and a $C_{av,ratio}$ of 3.1. The gate resistance is equal for CMOS and BiCMOS version (equal gate length).
The total resistance with n^+ sinkers is smaller in accumulation as well as in depletion, with a slightly larger reduction ($\approx 1\Omega$) in accumulation. This proofs how effectively the low ohmic buried layer and especially the highly doped n^+ sinkers and their lateral outdiffusion underneath the STIs reduce the resistance.
The minimum quality factors will be strongly increased in BiCMOS technology. In fact both, the absolute as well as the averaged minimum quality factors are doubled to values of 32 and 64, respectively.
Even the 1μm BiCMOS version reaches a higher averaged quality factor value than the shorter CMOS version.
Both BiCMOS devices offer considerably higher averaged quality factors than the conventional A-mode varactor without LDDs.
BiCMOS devices offer an effective way in standard technologies to achieve similar quality factors but significantly higher capacitance tuning ranges than conventional MOS varactors

3.2.8 A-mode varactor with lateral contact offset in CMOS technology

A proposed A-mode varactor with STIs is compared to one with lateral contact offset in 0.12μm technology (see page 47). Gate length and distance between gate and n^+ contacts are the same in both devices (Table 3.10).
Fig. 3.24 summarizes measurement results for both varactors.

Table 3.10: Compared devices with STI and with lateral contact offset. No p^+ or n^+ connections have been used

	gate length	finger length	fingers	STI width	distance gate - n^+
with STI	0.64μm	6.6μm	25	0.36μm	0.20μm
contact offset	0.64μm	6.6μm	25	n.a.	0.20μm

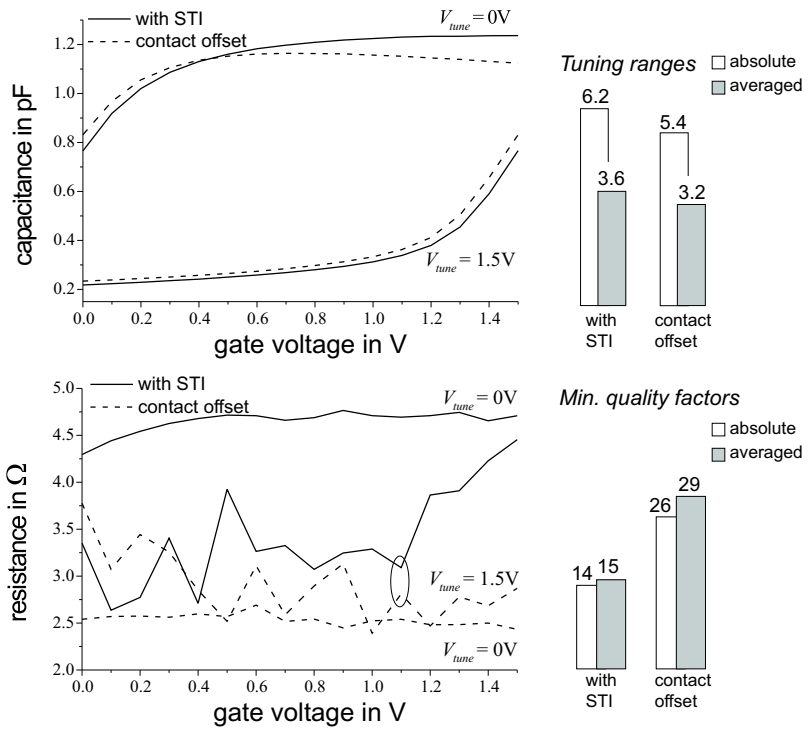

Figure 3.24: Comparison of devices with STI and lateral contact offset (f = 2GHz). Left: Measured small-signal capacitance and resistance. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

With contact offset the minimum capacitance is somewhat increased due to slightly higher fringing capacitances (see Fig. 3.6). However, the capacitance in accumulation is not constant (at $V_{tune} = 0V$), but decreases with increasing gate voltage and the maximum value is lower than with STIs. This is a result of process necessities leading to the so called "poly gate depletion effect". Between the gate and the n^+ contacts, all implantations leading to highly doped regions need to be blocked. Due to mask requirements the blocking layer overlaps the gate to some extent. Therefore the polysilicon gate is not homogeneously n^+-doped but practically undoped at the edges.

The charge in the accumulation layer has to be balanced by a depletion layer in the polysilicon. The width of this depletion layer is negligible in the highly doped gate but can be significant in the undoped gate regions, i.e. the poly gate depletion effect occurs. The depletion layer at the edges of the gate increases with gate voltage and decreases the total capacitance as it is in series with the gate oxide capacitance. Thus with higher minimum but lower maximum capacitance a lower capacitance tuning range is observed.
The gate resistance with contact offset is little higher than with STIs, as the polysilicon line is less wide. Partial low doping of the gate poses no problem for the resistance, since low-ohmic silicide is used additionally to polysilicon. However, the higher gate resistance is more than outweighed by the reduction of the well resistance. The maximum resistance with contact offset is almost halved compared to the device with STI, which is a result of the significantly shorter path through the n^- well. As the doping can be assumed to be homogeneous the resistance with contact offset is similar in accumulation and depletion.
The fluctuations in resistance at V_{tune} =1.5V result from the very low capacitance close to the resolution of the measurement equipment.
With lateral contact offset the absolute as well as the averaged quality factors are nearly twice as high than with STIs at the cost of 15% reduced tuning range.

3.2.9 I-mode varactors with deep source/drain in CMOS technology

I-mode varactors with deep source/drain have been tested in the 0.12μm CMOS technology. They are compared to conventional NMOS varactors and the influence of STIs is investigated.

Table 3.11: Design data of I-mode varactors with deep source/drain and optional STIs and the conventional NMOS for comparison. S/D stands for source/drain.

	gate length	finger length	fingers	STI width	distance gate - n^+	well distance	n^+ conn.
NMOS	0.24μm	3μm	128	n.a.	0μm	n.a.	n.a.
deep S/D	0.32μm	6.6μm	100	n.a.	0μm	0.7μm	n.a.
deep S/D with STI	0.32μm	6.6μm	100	0.33μm	0.16μm	0.7μm	2x0.24μm

The design data of the I-mode varactors with deep/source drain (with and without STI) and of the conventional NMOS for comparison are summarized in Table 3.11. To assure large depletion regions around the n^- wells the doping between them is chosen to be very low (i.e. p^- substrate instead of p^- well).

Influence of simplified model on extracted parameters

Similarly to the A-mode varactors the simplified model of only an effective capacitance and an effective series resistance is used to extract values for C and R_c. However, due to the pn junctions between p^- well/substrate and n^+ regions/n^- wells the real situation in depletion is different than for the A-mode varactors.
For I-mode varactors with deep source/drain the cross-section and equivalent model for depletion and inversion are depicted in Fig. 3.25.

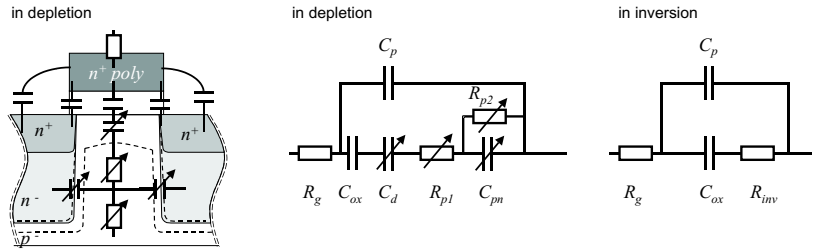

Figure 3.25: Cross-section and lumped-elements of a I-mode varactor with deep source/drain in depletion. Dashed lines indicate borders of depletion regions. Equivalent circuits in depletion and inversion (right).

The main difference to the A-mode varactors appears in depletion. On the one hand the series resistance is higher, as the path through the p^- region is long and additionally restricted by the depletion regions at the pn junctions. On the other hand the pn junction capacitances are parallel to part of the resistance. This situation results in a more important role of the parasitic capacitance and a stronger resistance-lowering effect than in A-mode devices.

Comparison of I-mode varactor with deep source/drain and conventional NMOS varactor

The proposed I-mode device with deep source/drain is compared to the conventional NMOS varactor. Fig. 3.26 shows the measurement results.

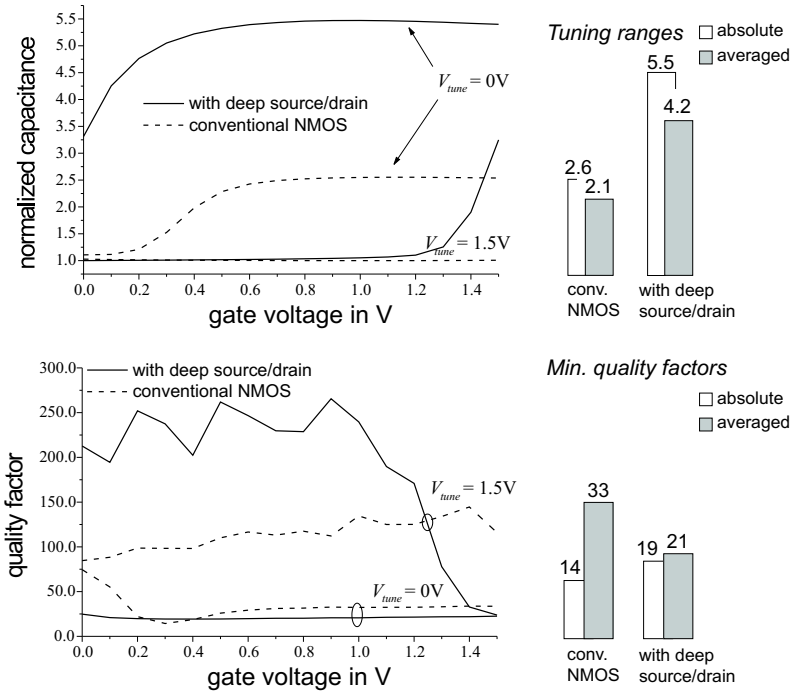

Figure 3.26: Comparison of the I-mode varactor with deep source/drain and a conventional NMOS ($f = 2$GHz). Left: Measured small-signal capacitance (normalized) and quality factor. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

With deep source drain the capacitance tuning range of 5.5 is more than twice as high than $C_{ratio} = 2.6$ of the conventional NMOS varactor. Similarly the averaged capacitance tuning range is doubled from 2.1 to 4.2. These

strong increases stem from the very low minimum capacitance with deep source/drain.
The device with deep source/drain reaches inversion at much lower voltages than the conventional varactor. As the gates are in both cases n^+-doped, the shift in threshold voltage results from the considerably different doping of the p^- regions.
The absolute capacitance of the I-mode varactor with deep source/drain at several tuning voltages is shown in Fig. 3.27. In depletion the capacitance drops to the same value for all tuning voltages and the curves are extremely flat.

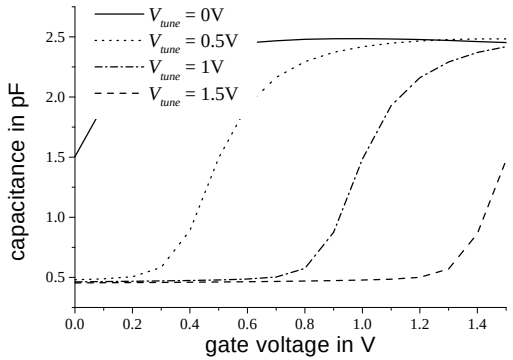

Figure 3.27: Absolute small-signal capacitance of the I-mode varactor with deep source/drain at various tuning voltages (0V...1.5V; 0.5V steps @ $f = 2$GHz).

The effect that the capacitance drops significantly at a certain tuning voltage when the depletion regions around the n^- wells touch is not visible. Thus it is concluded that the capacitance decrease is limited by parasitic capacitances. Further due to the low doping already the gate-controlled depletion region seems to be large enough to increase the capacitance tuning range by the observed large value.

Fig. 3.28 compares the resistances of the conventional NMOS varactor and the I-mode device with deep source/drain (normalized to 100μm gate width). At zero tuning voltage the resistance of the NMOS peaks at the transition to inversion. In strong inversion the resistance drops to a much lower value. No peak occurs at $V_{tune} = 1.5$V as the device remains in

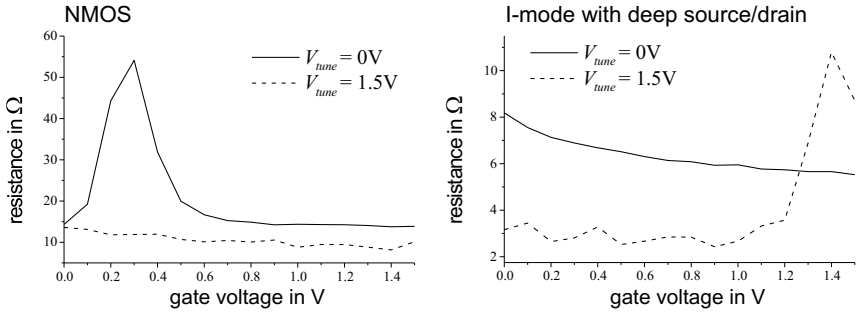

Figure 3.28: Absolute resistances of a conventional NMOS (left) and a I-mode varactor with deep source/drain (right). Values are normalized to 100μm gate width.

depletion at all gate voltages. The path from the border of the depletion region around the n^+ source/drain regions to the p^+ substrate contacts (guard ring) determine the resistance. A careful designed guard ring and the resistance-lowering effect of the parasitic capacitances facilitate the observed lower resistance in depletion.
With deep source/drain a peak in resistance is not observed at zero tuning voltage but at V_{tune} = 1.5V, which is a result of the shifted threshold voltage.
The lower resistance in depletion can not be explained by carefully designed guard rings only, as there is still a long path around the deep n^- wells. Further this path is restricted by the depletion regions of pn junctions and leads through a very low doped p^- substrate. However, in depletion the variable capacitance is very low and the parasitic capacitances determine the total capacitance. Therefore the effective resistance is almost entirely given by the path across the parasitic capacitances, leading to the observed low effective resistance value in depletion.
With deep source/drain the series resistance is lower in inversion also. This implies that the lateral outdiffusion of the n^- well during processing is larger than expected and the effective gate length is reduced even below the length of the conventional NMOS. Thus the absolute minimum quality factor with deep source/drain is almost 39% higher than the value of the conventional NMOS varactor; Q_{min} increases from 14 to 19. But the minimum averaged quality factor of the NMOS varactor has a value of 33,

which is more than 50% higher than $Q_{av,min}$ = 21 with deep source/drain. This unusual result of a higher absolute but lower averaged minimum quality factor is a result of the voltage dependencies of the capacitance and resistance at V_{tune} = 1.5V. With deep source/drain both are very flat, which leads to only a small increase of quality factor through averaging. Contrary, the conventional NMOS varactor's absolute minimum quality factor is determined by a distinct peak in the resistance.

I-mode varactor with deep source/drain and STIs

The influence of STIs on the I-mode varactor with deep source/drain is shown in Fig. 3.29 where devices with and without STI are compared.
The maximum capacitances reach the same value, proving that the two n^+ connections per finger in the STI-design are effective in providing the electrons for inversion. The lower minimum capacitance with STIs is expected, as they reduce parasitic capacitances considerably. Also with STIs the capacitance characteristic shows a very flat behaviour in depletion. This observation leads to the same conclusion as for the varactor without STIs: the minimum capacitance is already determined by the gate controlled depletion region and it is limited (i.e. given) by the parasitic capacitances. A decrease in parasitic capacitances directly converts to a decrease in minimum achievable capacitance. This explains the 60% higher absolute and 57% higher averaged capacitance tuning ranges with STIs: C_{ratio} is increased from 5.5 to 8.8, and a $C_{av,ratio}$ of 6.6 instead of 4.2 is achieved.
The transition from depletion to inversion is strikingly flatter with STIs. This is caused by the long path for the electrons in the inversion layer to the source regions (n^+ connections). It is determined by the distance between the n^+ connections and corresponds to a gate length of more than 3.2μm. For such a large gate length the frequency has some influence at 2GHz already (in detail next subsection 3.2.10). The charge in the inversion layer can not follow the high frequent signal at the gate, leading to a reduction in capacitance and the observed flatter transition region.
The resistance graph (Fig. 3.29(bottom left)) reveals the poor resistive behaviour of the I-mode device with deep source/drain and STI. Independently of biasing, but especially at the onset of inversion and in strong inversion the resistances are severely higher than without STIs. These large resistances

are determined by the long path in inversion.
The high resistances lead to low minimum quality factors with STI (≈ 1). Increasing the number of n^+ connections per finger can increase the quality factor. However, it will always remain lower than the values without STI.

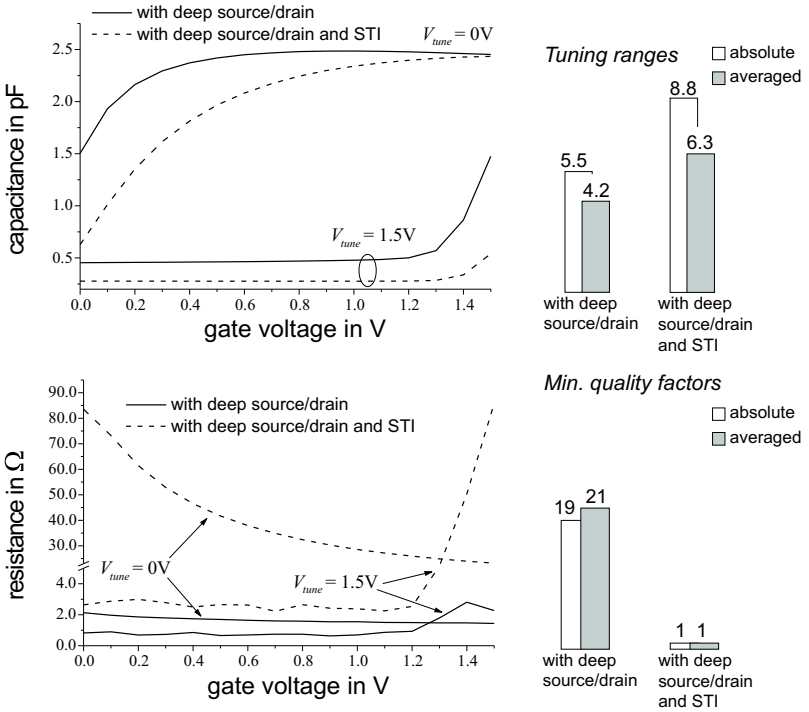

Figure 3.29: Comparison of the I-mode varactors with deep source/drain and either with or without STIs (f = 2GHz). Left: Measured small-signal capacitance and resistance. Right: Measured absolute and averaged tuning ranges and minimum quality factors.

3.2.10 Influence of the frequency on measured results

The measured capacitances and to a lesser extent the resistances show a frequency dependence. As an example serves the A-mode varactor with STI (Fig. 3.30).
The capacitance increases noticeable with frequency, as a result of the simple model for extraction.
A parasitic inductance determined by the wiring (≈100pH) is in series with the varactor. At low frequencies it acts as a short. However, at increasing frequencies it interacts with the rest of the device and the total network mimics a higher effective capacitance C'

$$C' = -\frac{1}{\omega \mathrm{Im}(\frac{1}{Y_{11}})} = \frac{C}{1-\omega^2 L_p C}. \tag{3.5}$$

With further de-embedding structures it is possible to obtain the varactor without a parasitic inductance. However, the results with inductance seem more appropriate, as in applications the varactor can not be used without wiring.

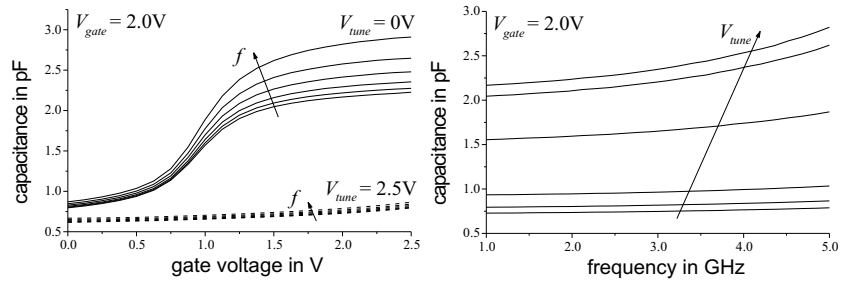

Figure 3.30: Influence of the frequency on measured small-signal capacitance of the A-mode varactor with STI. Left: Measured capacitance as function of gate voltage at $V_{tune} = 0V, 2.5V$ for different frequencies (0.2GHz...5.2GHz; 1GHz steps). Right: Measured capacitance as function of frequency at $V_{gate} = 2V$ and $V_{tune} = 0V, 2.5V$.

Besides this influence of the parasitic inductance the frequency dependent behaviour of the charge in the inversion layer has to be considered. Above a

certain frequency the carriers in the inversion layer can not react fast enough to AC-changes of the gate charge.
Although the inversion layer exists it becomes "invisible" in the small-signal analysis. In the A-mode devices the reason for this is the slow generation of holes. In the I-mode varactors the carriers supplied by the source/drain regions are delayed due to the RC-time of the inversion layer. The frequency around which this behaviour becomes observable is approximated by

$$\begin{aligned} f_{i,1} &= \tau^{-1} && \text{A-mode – without source/drain} \\ f_{i,2} &= (RC)_{max,DC}{}^{-1} && \text{I-mode – with source/drain} \end{aligned} \tag{3.6}$$

$(RC)_{max,DC}$ is the maximum (extrapolated) value at DC and τ is the doping dependent lifetime of holes. As the resistance R and the capacitance C increase with gate length the frequency $f_{i,2}$ decreases.
For A-mode varactors the frequencies of interest (in the GHz range) are always several orders above $f_{i,1}$ [36], therefore a large inversion capacitance (gate oxide capacitance) is not observed. Contrary, for I-mode varactors with gate lengths below ca. 0.35μm the frequencies $f_{i,2}$ are usually one order of magnitude or more above the frequencies of interest. Therefore a delay in inversion layer charge is usually not observed. However for large gate lengths, e.g. the I-mode varactors with deep source/drain and STIs, the delay becomes observable and the capacitance does not increase with frequency, but decreases (Fig. 3.31).

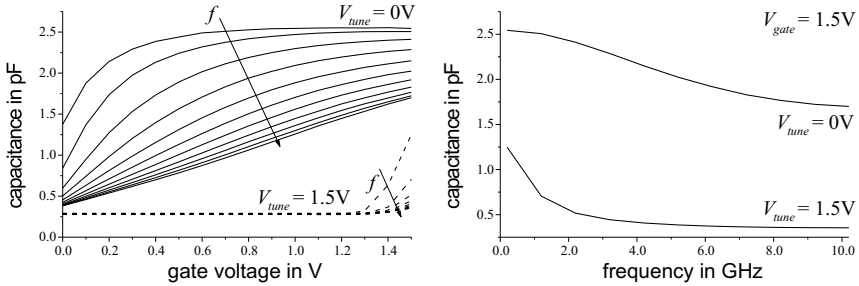

Figure 3.31: Influence of the frequency on measured small-signal capacitance of the I-mode varactor with deep source/drain and STI. Left: Measured capacitance as function of gate voltage at $V_{tune} = 0V, 1.5V$ (0.2GHz...10.2GHz; 1GHz steps). Right: Measured capacitance as function of frequency at $V_{gate} = 0V$ and $V_{tune} = 0V, 1.5V$.

The I-mode varactors with deep source/drain and STI feature a short drawn gate length (0.35μm), but a large effective gate length (>3.2μm) determined by the distance between the n^+ connections and their length. The frequency $f_{i,2}$ extracted from measurements is around 1GHz. (The corresponding values without STIs are more than 100 times higher.) Measurement results of the small-signal capacitance show a strong dependence on frequency (Fig. 3.31). Increasing frequency near to and above $f_{i,2}$ decreases capacitance significantly. Charge changes at the gate cannot be balanced by the inversion layer anymore, but find the mirror charges in a depletion region with varying depth. The effect is strongest at the transition to inversion, where the resistance (and thus the product RC) of I-mode varactors peaks. The decrease in capacitance due to the long RC-time outweighs an increase due to the parasitic inductance.
For all other varactors a behaviour with increasing capacitance has been observed (as shown in Fig. 3.30).

3.3 Conclusion

This chapter describes the design and measurement results for the various proposed accumulation mode as well as inversion mode varactors. The aim was to provide devices with higher capacitance tuning range compared to conventional MOS varactors and sufficient high quality factors for application in LC-VCOs.
Except two devices in standard BiCMOS technology all devices have been realized in standard digital CMOS technologies.
The proposed accumulation mode varactors in n^- well include STIs within the device between the active area beneath the gate and the well contacts. The resulting reduction of parasitic overlap and fringing capacitances increases capacitance tuning ranges up to 50% (at equal gate length). At minimum gate length averaged minimum quality factors are lower than those of conventional MOS varactors. But the resistance of the proposed devices increases much less with gate length. Therefore at longer gate lengths the varactors with STI simultaneously feature higher capacitance tuning ranges and higher quality factors than conventional MOS varactors.
In standard digital CMOS technology the proposed devices promise higher frequency tuning ranges than conventional MOS varactors at sufficient high

quality factors (confirmed in section 5.2).
Several methods have been presented to further improve the performance of devices with STI. p^+ regions increase tuning range and n^+ connections or decreased STI width improve the quality factor.
In BiCMOS versions of the proposed device highly doped n^+ sinkers replace the shallow n^+ source/drain regions of the CMOS process. This increases quality factors significantly (by 100%) without impairing the high capacitance tuning range. These BiCMOS devices outperfom conventional MOS devices at all gate lengths.
Varactors with entirely n- or p- or alternating n- and p-doped gate fingers have been compared. Due to the influence of different flatband voltages the device with np gates features capacitance tuning ranges and quality factors in between the values of the devices with homogeneous gate doping. Mixed doping is an effective method to achieve significantly less steep capacitance characteristics, which is advantageous as it can reduce flicker noise upconversion in VCOs (confirmed in section 5.3).
The solution without STI but lateral offset of well contacts provides higher quality factors (90% increase compared to CMOS version with STI). But due to the manufacturing process the gate will be partly low-doped, which leads to the poly gate depletion effect and hence reduces capacitance tuning.

For the proposed I-mode varactors deep n^- wells are used additionally to the highly doped, but shallow source/drain implants of conventional NMOS devices. Lateral depletion regions around the wells can reduce the minimum capacitance. The I-mode varactors with deep source/drain double the capacitance tuning range compared to conventional NMOS devices without impairing the minimum quality factor.

For the I-mode varactors with deep source/drain it is somewhat critical to get the desired distance of the wells, which is due to the lateral outdiffusion of dopands. The varactors with STI do not pose problems since all combinations of technology elements are well characterized and etching of the STI is very exact and more controllable than diffusion processes. This is demonstrated by the fact that all manufactured and measured A-mode devices with STIs (more than 30) functioned well.

Chapter 4

Integrated inductors

This work and the following sections focus on symmetrical inductors for differential VCOs. Section 4.1 of this chapter treats the inductor design which is common to all of the inductors herein. The second section describes briefly the measurement methodology. The third section covers the inductors used in the VCOs of the following chapter 5. A substrate structure for inductors in standard CMOS technologies is proposed in the fourth section.

4.1 Inductor design

The inductors in this work are all intended for use in differential LC-VCOs. They are realized either in the 0.25μm technology with four aluminum layers or in the 0.12μm technology with six copper layers (more details of technology in section 3.2.1).
Instead of two inductors (area-consuming) one coupled inductor with special layout is employed (Fig. 4.1) [49, 21, 12].

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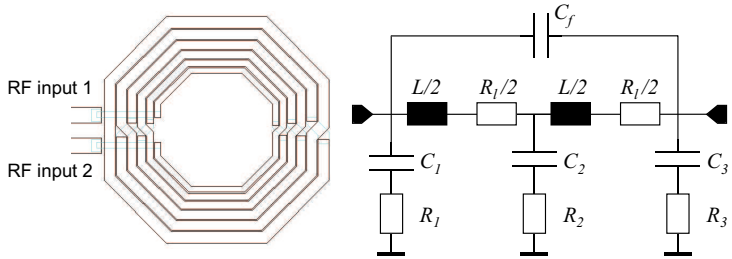

Figure 4.1: Symmetrical, octagonal inductor and equivalent double-π model.

The symmetrical inductor with octagonal windings features the two RF inputs at the inner windings, the outer winding is at common mode. Therefore the winding width can be increased from inner to outer winding without capacitive penalty. At the same time the series resistance is decreased, as the outer (widest) winding is the longest.
To further reduce series resistance several metal layers are shunted, resulting in an thicker effective metal layer. With copper metallisation connection between the layers can be made with interleaved copper vias, so-called "viabars", to provide low-ohmic connection between the windings and hence lower the series resistance [49].
The inductor can be represented by the double-π model of Fig. 4.1. L denotes the inductance and R_l the series resistance. The parasitic capacitances between the metal layers of the inductor and the substrate are denoted by C_1, C_2 and C_3 where C_1 and C_3 are equal due to symmetry reasons. The same applies to the effective substrate resistances $R_1 = R_3$ and R_2. C_f describes the parasitic capacitance resulting from the coupling between the windings and the two inputs.

4.2 Parameter extraction

S-parameter measurements have been carried out on-wafer with a HP 8510 network analyzer (details of measurement environment and methodology in

section 3.2.2). After de-embedding (appendix B.3) the effective inductance and resistance are extracted via

$$\begin{aligned} L_{eff}(f) &= \frac{\mathrm{Im}(Y_{11}^{-1})}{2\pi f} \\ R_{eff}(f) &= \mathrm{Re}(Y_{11}^{-1}) \end{aligned} \tag{4.1}$$

with f the frequency. Further on inductance L and resistance R_l denote the effective, frequency dependent values. Quality factors according to the bandwidth definition result from the LC-tanks formed when connecting an ideal capacitance in parallel to the measured data of the inductor. The importance of this quality factor has been discussed in section 2.2.4 and the extraction procedure is given in appendix C.

4.3 Inductors for test VCOs

4.3.1 3.7nH inductor

Inductor design

The differential, symmetrical inductor is comprised of six octagonal windings. To reduce series resistances the winding width is staggered (larger width at outer winding) and metals 2, 3, 4 (aluminum) of the four metal layer process are connected in parallel (0.25μm technology). Design data and layout are given in Table 4.1 and Fig. 4.2.

Table 4.1: Design data of the 3.7nH inductor used in the VCOs of section 5.2.

windings	winding width min/max	radius inner/outer	spacing min/max	metal
6	2.9μm/5.8μm	30μm/58μm	0.6μm	2,3,4 aluminum

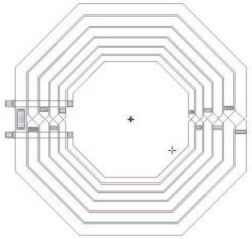

Figure 4.2: Layout of the 3.7nH inductor used in the VCOs of section 5.2.

The inductor in the VCO is derived from a larger inductor by scaling with a factor 72/84. Scaling rules stem from considering the geometry dependence for the separate elements of the model. E.g. the series resistance remains constant, as the number of squares of each segment remains constant, since the length and the width are reduced by the same factor.

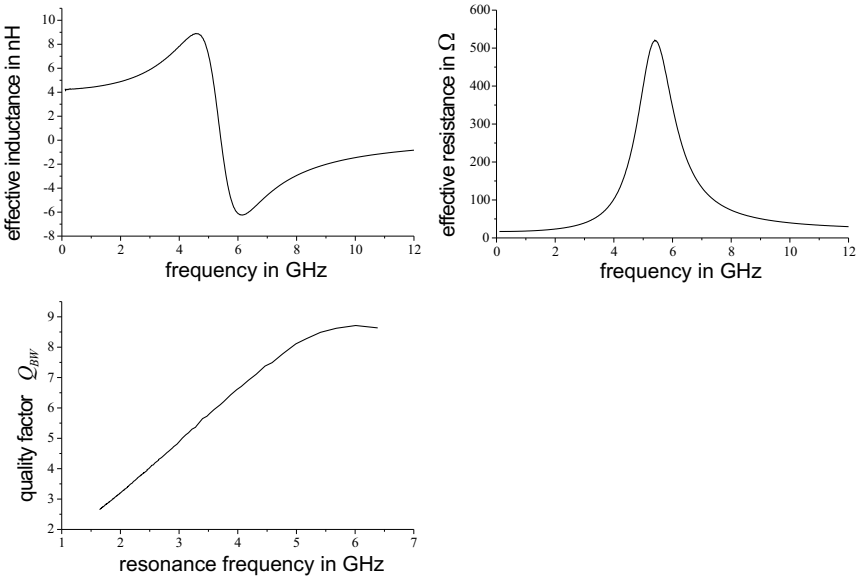

Figure 4.3: Measurement results of the original 4.2nH inductor (3.7nH by scaling).

Measurement results

Fig. 4.3 summarizes measurement results for the original inductor. The low-frequency inductance is 4.2nH (scaled 3.7nH), the resistance 16.7Ω. The quality factor reaches a maximum value above 9 (scaled 7.5).

4.3.2 4.4nH inductor

Inductor design

The differential, symmetrical inductor has six octagonal windings. To reduce series resistances the winding width is staggered (larger width at outer winding) and metals 4, 5, 6 (copper) of the 0.12μm digital CMOS process are connected in parallel with copper viabars. Layout and design data are given in Fig. 4.4 and Table 4.2.

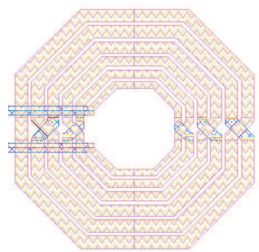

Figure 4.4: Layout of the inductor used in the VCOs of section 5.3.

Table 4.2: Design data of the inductor used in the VCOs of section 5.3.

windings	winding width min/max	radius inner/outer	spacing min/max	via bars width/spacing	metal
6	5μm/10μm	32μm/95μm	2.8μm/3.2μm	0.4μm/0.8μm	4,5,6 copper

Measurement results

Fig. 4.5 summarizes measurement results for the inductor.

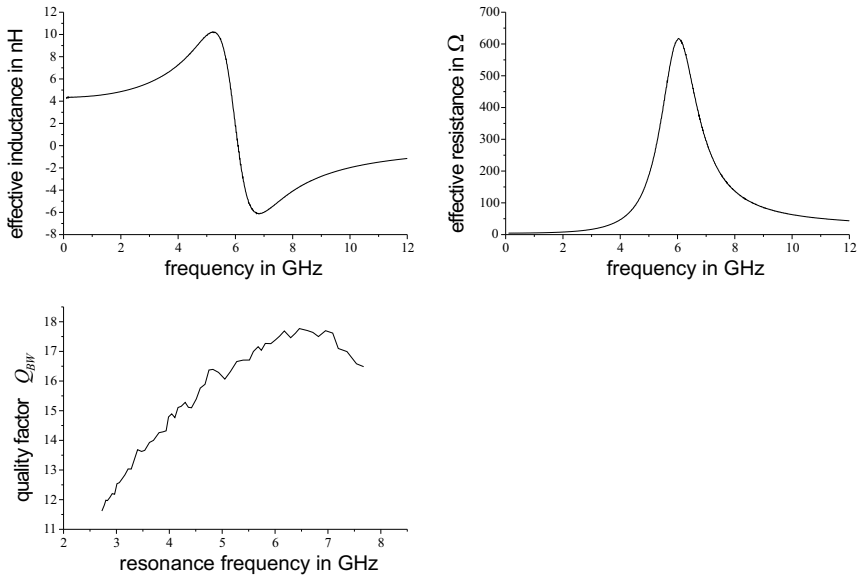

Figure 4.5: Measurement results for the inductor used in the VCOs of section 5.3.

The inductor features an inductance of 4.4nH and a DC series resistance of 4.7Ω. The maximum quality factor is ca. 18.

4.4 Substrate structure for integrated inductors

This section presents a substrate structure for integrated inductors. A variety of substrate structures and ground shields has been published already

(briefly described in section 2.2.4). Many aim mainly at reducing eddy currents [22, 23, 24, 25], whereas capacitive coupling between inductor and substrate remains constant or is even increased. A reduction of parasitic capacitances is achieved in [25, 26, 27, 28], but always using non-standard CMOS technology. The only solution compatible with standard CMOS technology is obtained by a biased n^- well described in [29]. But this solution has a homogeneous region below the inductor. Thus only a vertical depletion region below the n^- well can be used to decrease the parasitic capacitance, and there is no patterning that could reduce eddy currents.
The herein proposed structure is fully compatible with standard digital CMOS process flow and low resistivity substrates. It is comprised of alternating n^--well and p^--substrate regions. By applying a voltage to the structure the semiconductor region below the inductor is depleted from mobile charge carriers up to a certain depth. Substrate losses due to parasitic capacitances and eddy currents are thereby reduced.
Four test structures with the identical inductor, three with and one without substrate structure, are compared in a standard 0.12μm digital CMOS process.

4.4.1 Principle of substrate structure

The cross-section of the substrate structure and (for simplicity) a one-metal-layer inductor is shown in Fig. 4.6, a top view in Fig. 4.7.

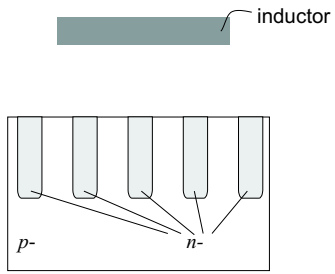

Figure 4.6: Substrate structure: thin, parallel n^- wells in p^- substrate and a simple one-layer inductor (grey bar).

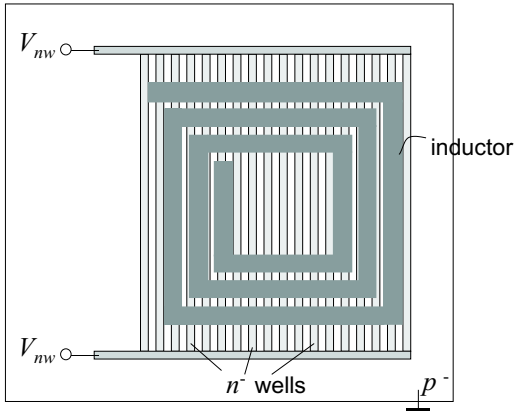

Figure 4.7: Substrate structure: thin, parallel n^- wells in p^- substrate and a simple one-layer inductor.

In the simplest case the substrate structure is implemented as parallel stripes of equidistant n^--well and p^--substrate regions. At both ends the n^- wells are connected by highly doped n^+ regions and a voltage can be applied.
Increasing the voltage applied to the n^- wells increases the depletion region laterally between them, and vertically beneath them. At some n^--well voltage the depletion regions of two adjacent n^- wells touch and deplete the p^- substrate totally to at least the depth of the n^- wells (Fig. 4.8). The n^- wells themselves will be partially depleted, too.
The depleted semiconductor layer leads to a reduced effective small-signal capacitance between inductor and substrate. Assuming that the non-depleted width of the n^- wells is negligible, this capacitance can be approximated by

$$C_{eff} = (C_{ox}^{-1} + C_{jd}^{-1})^{-1} \tag{4.2}$$

with C_{jd} the depletion region capacitance.
As parasitic capacitances reduce the quality factor and the self-resonance frequency of the inductor, the performance of an inductor can be enhanced by applying a voltage to the substrate structure.

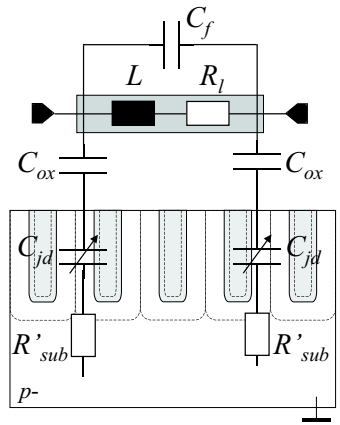

Figure 4.8: Simple inductor (grey bar) and substrate structure with totally depleted p^--substrate regions between the n^- wells. Dashed lines indicate the borders of the depletion regions.

The n^- wells should be as thin as possible, as they usually can be depleted only partially due to their higher doping compared to the p^- substrate.
Patterning the substrate structure as described in [22, 25] can further reduce the influence of eddy currents.

4.4.2 Inductor design

The differential, symmetrical inductors used for evaluation of the substrate structure have five windings with staggered winding width to reduce series resistances. Metal fill structures, which are common to modern sub-micron processes, are suppressed for the benefit of a higher quality factor [17]. Table 4.3 summarizes design data and Fig. 4.9 shows a die photograph and layout of one of the inductors. Clearly visible is the suppression of metal fill structures in the area of the inductor. Inductor size is 200μm x 200μm.

Table 4.3: Design data of the inductor used for evaluation of the substrate structure.

windings	winding width min/max	radius inner/outer	spacing min/max	via bars width/spacing	metal
5	4.8μm/10.0μm	45μm/90μm	1.8μm/2.9μm	0.2μm/0.8μm	2,3,4 copper

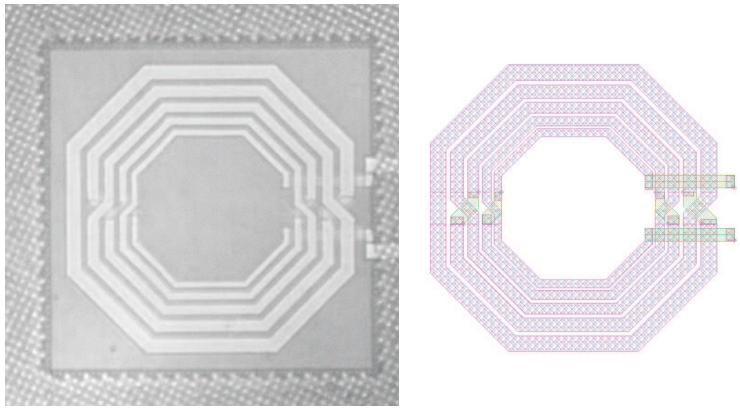

Figure 4.9: Die photograph and layout of the inductor used for evaluation of the substrate structure.

The reference inductor is fabricated without substrate structure. The substrate structures for the other three inductors feature equidistant n^- well stripes with minimum allowed width. Spacing of the n^- wells is 0.7μm, 1.0μm or 1.3μm.

4.4.3 Measurement results

Fig. 4.10 summarizes measurement results for the reference inductor. The measured inductance is 4.0nH at a DC series resistance of 6.2Ω. These values are not influenced by the substrate and are identical for the other three inductors. The 3dB quality factor of the reference inductor reaches a maximum value of 8.6.

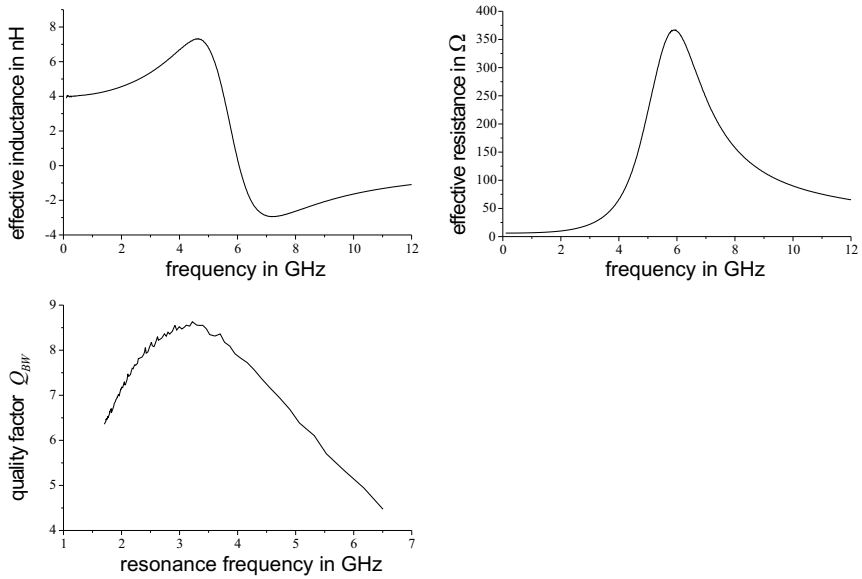

Figure 4.10: Measurement results of the reference inductor.

The measured quality factors of inductors with substrate structures are visualized in Figs. 4.11 - 4.13. Table 4.4 lists the maximum quality factors and the corresponding resonance frequencies.
Fig. 4.11 depicts the quality factors of the inductor with 0.7μm distance of the n^- wells at 4 different n^--well voltages V_{nw} in comparison to the reference inductor.
Due to the built-in voltage (ca. 1V) of the n^-well/p^--substrate junction, depletion regions are already present at zero n^--well voltage. They reduce C_{eff} (see Eq. 4.2) and also eddy currents. Thus, already at zero V_{nw} the substrate structure increases the maximum quality factor as well as the corresponding resonance frequency by 34% compared to the reference inductor. Increasing V_{nw} from 0V to 1.5V increases the maximum quality factor by further 5%. The corresponding resonance frequency is 16% higher.
At n^--well voltages of 3V and 4.5V no influence is observed any more: the p^--substrate regions are totally depleted at 1.5V already.

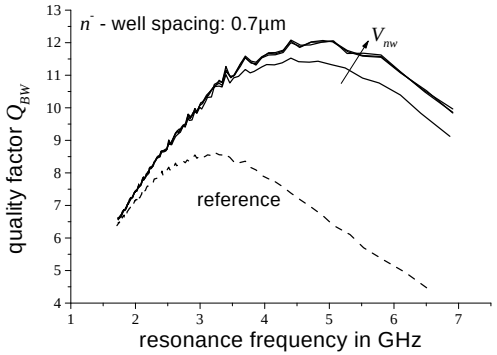

Figure 4.11: Measured bandwidth quality factors of the inductor with substrate structure with n^--well distance 0.7μm and at n^--well voltages (0V...4.5V; 1.5V steps).

The quality factor results for the inductor with n^--well distance of 1.0μm in comparison to the reference inductor are shown in Fig. 4.12. At zero n^--well voltage a 27% higher quality factor and a 25% shift in resonance frequency is obtained. With a V_{nw} increase from 0V to 1.5V the maximum quality factor of the inductor increases by further 12% and the resonance frequency shifts by 25%.

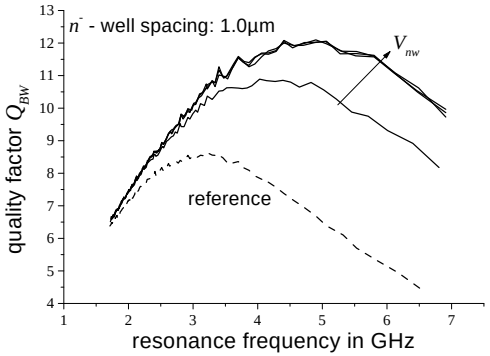

Figure 4.12: Measured bandwidth quality factors of the inductor with substrate structure with n^--well distance 1.0μm and at n^--well voltages (0V...4.5V; 1.5V steps).

Similarly to the substrate structure with 0.7μm distance of the n^- wells, the p^--substrate regions seem to be totally depleted at 1.5V already and a further increase of applied voltage has no effect.
Fig. 4.13 depicts the quality factor of the inductor with 1.3μm n^--well distance in comparison to the reference inductor. At zero V_{nw} a 16% higher maximum quality factor and a 22% higher resonance frequency as for the reference inductor are observed. The maximum quality factors are increased by further 14% through applying a voltage. The resonance frequency at maximum quality factor shifts to higher frequencies by another 28%.
Contrary to the two inductors with less n^--well spacing different maxima are observed at all voltages V_{nw}, indicating that only above 4.5V a total depletion of the p^--substrate regions between the n^- wells can be obtained.

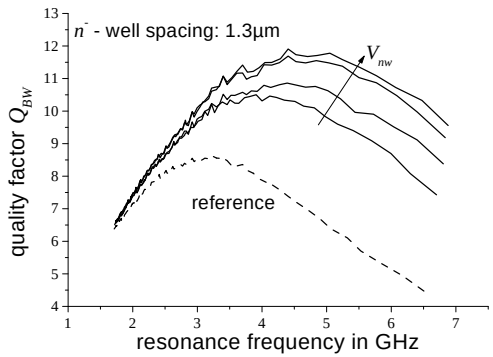

Figure 4.13: Measured bandwidth quality factors of the inductor with substrate structure with n^--well distance 1.3μm and at n^--well voltages (0V...4.5V; 1.5V steps).

Apparently the maximum quality factors at zero V_{nw} are lower with larger n^--well distance (compare Figs. 4.11, 4.12, 4.13). With closely spaced n^- wells the depletion regions due to the built-in voltage of n^--well/p^--substrate junction lead to a larger amount of depleted area and smaller capacitance. At larger n^--well spacing this situation with already - to some extent - decreased capacitance is only reached at some non-zero V_{nw}.
Additionally more freely flowing eddy currents in wider p^--substrate regions might be of importance.

Table 4.4: Measured maximum quality factors and corresponding resonance frequencies at different n^--well voltages.

	$Q_{BW,max}$ @ $f_{resonance}$		
V_{nw}	0.7μm	1.0μm	1.3μm
0V	11.5 @ 4.3GHz	10.9 @ 4.0GHz	10.5 @ 3.9GHz
1.5V	12.0 @ 5.0GHz	12.1 @ 5.0GHz	10.9 @ 4.4GHz
3.0V	12.0 @ 5.0GHz	12.1 @ 5.0GHz	11.6 @ 4.9GHz
4.5V	12.0 @ 5.0GHz	12.1 @ 5.0GHz	11.9 @ 5.0GHz

reference: 8.6 @ 3.2GHz

All inductors reach the same values at total depletion between the p^- substrate. This is despite the fact that the total number of n^- wells underneath the inductor is different in each case. Outdiffusion of n^- wells into p^- substrate (here) is considerably larger than into p^- wells. Therefore the average doping of the n^- wells in the substrate structure is much lower and depletion regions within much wider than in conventionally used n^- wells. The non-depleted regions within the n^- wells do not play a significant role and thus the different number of n^- wells does not show in the maximum results. As mentioned before, patterning the n^- wells according to [22, 25] can strongly reduce eddy currents leading to a further increase of the quality factor.

4.5 Conclusion

The inductors of choice in this work are symmetrical and octagonal. Using several windings with increasing winding width reduces the metal series resistance without capacitive penalty (outer winding at common mode).
With a proposed substrate structure for integrated inductors the coupling between the inductor and the substrate is reduced. The structure consists of alternating n^--well and p^--substrate regions and is compatible with standard digital CMOS process flow. Applying a voltage to the structure controls variable lateral and vertical depletion regions and alters the number of free carriers underneath the inductor. Thus the parasitic capacitances and eddy currents can be reduced
A 4.0nH inductor with 6.2Ω DC resistance is used to investigate the influence of the substrate structure. With 5 windings in metal 2,3,4 (copper) of

the 0.12μm CMOS technology it features a maximum quality factor of 8.6 without substrate structure.
Applying a voltage to the substrate structure increases the maximum quality factor by 41% and the resonance frequency at peak quality factor by up to 56%. Especially at high frequencies the proposed structure offers large advantages.
The improvements achieved through the substrate structure are more pronounced when the distance between the lowest metal layer of the inductor and the substrate is low. Thus the proposed substrate structure offers high practical value. In technologies with few metal layers the advantage has been demonstrated. In technologies with more metal layers a maximum number of layers can be connected in parallel (for low series resistance) with only little (if at all) capacitive penalty.
The same measurement results have been obtained for 0.7μm and 1.0μm distance of the wells and a n^--well voltage of 1.5V. Thus the problem of controlling the lateral outdiffusion of the n^- wells is not severe, since the n^--well distance is not critical.

Chapter 5

CMOS VCO designs based on proposed MOS varactors

This chapter presents the design, results and discussion of several VCOs. The first section introduces the most common active, differential VCO topologies and the topology used for the VCOs in this work. The second section investigates the suitability of the A-mode varactors with STI for fully integrated VCOs by comparing three VCOs with a conventional varactor and varactors with STI. The influence of the MOS varactor gate doping on the performance of a VCO is presented in the third section. The fourth section explains the switched varactor concept to reduce sensitivity to variations in supply and tuning voltage and the concept's impacts on the VCO performance. The final section summarizes the main findings.

5.1 VCO topology

Fig. 5.1 gives an overview of the most widely used active, differential *LC*-VCO topologies. Either NMOS-only, PMOS-only or complementary solu-

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tions are possible. In the complementary circuit power consumption is lower as current is reused. Exemplarily for the NMOS-only topology it has further been shown that phase noise at a given power consumption is inferior compared to the complementary case [30].
Current sources imprint a defined current and - depending on the size of the current - limit the amplitude of the signal. Using the current source at V_{dd} (V_{ss}) reduces the sensitivity of oscillation frequency to variations in V_{dd} (V_{ss}), as the potential at the respective point is pinned. Voltage variations in V_{dd} are expected to be more relevant, thus using the current source at V_{dd} instead of V_{ss} is advantageous in terms of overall sensitivity.

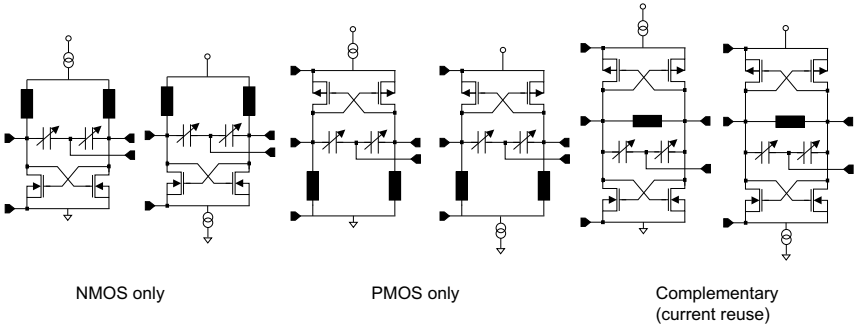


Figure 5.1: Active differential VCO topologies.

Fig. 5.2 shows the topology [21] of the fully, symmetric VCO used in this work. For low power consumption and phase noise a complementary solution was chosen, where a differential pair overcomes the losses in the tank. Furthermore, the current source was omitted to maximize the signal swing and eliminate an important phase noise source [49, 42].
The sizes of the MOS-transistors are chosen for maximum symmetry of the waveforms in order to minimize the upconversion of flicker noise.
The tuning voltage applied to the source/drain-regions (I-mode varactor) or well contacts (A-mode varactor) of the varactor controls the capacitance. The oscillating voltage of the output signal of the VCO appears at the gate of the varactor. To linearize the VCO frequency tuning, the varactors are directly coupled to the inductor and their steep characteristic is averaged out over the large voltage swing [49].

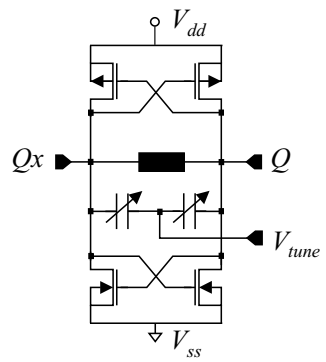


Figure 5.2: Topology of VCO circuits.

Varactor design in each case is corresponding to the description in chapter 3. The symmetrical, differential inductors have been designed as described in chapter 4.
The VCOs in the following three sections utilize the described complementary, differential topology without current source. They are realized in 0.25μm and 0.12μm standard digital CMOS technologies with transistor f_t of 40GHz (NMOS), [49] and 100GHz (NMOS) [66], respectively (more details in section 3.2.1).
Varactors and inductors have been characterized separately by S-parameter measurements as described in the previous two chapters.
For measuring the VCO, buffers have been implemented on the same chip to drive the output pads (Fig 5.3). To connect the VCO to the measurement equipment it had to be custom-bonded on a printed circuit board (PCB; Fig. 5.3). Further, capacitors of different values are connected between DC lines and ground to damp noise incoming from the measurement equipment. Frequency tuning behaviour and pushing (±50mV) was measured with an HP 53152 frequency counter. Phase noise results were obtained with an *Europtest*PN9000 (delay-line method).

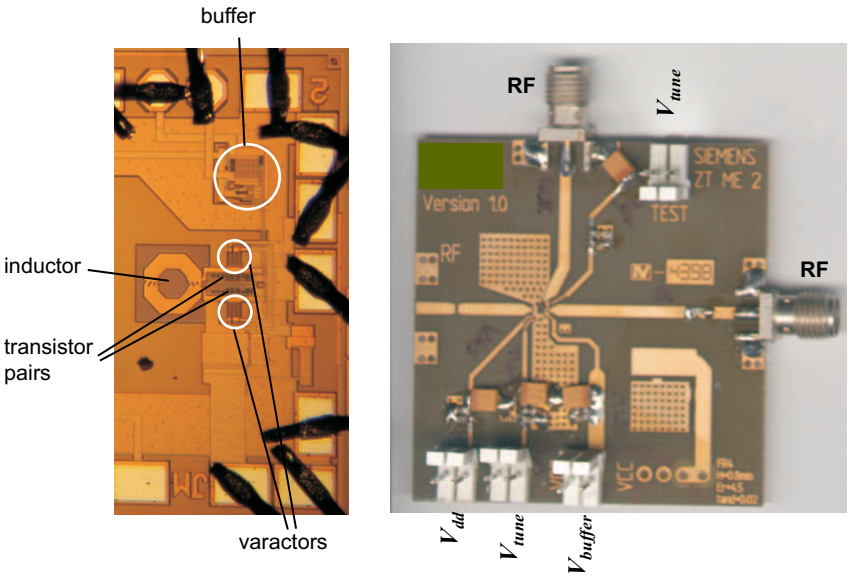


Figure 5.3: VCO chip with buffer (left) and PCB ready for measurement (right).

5.2 VCO with the proposed device with STI

In this section three fully integrated VCOs are compared in 0.25μm standard digital CMOS technology. The reference VCO utilizes a conventional NMOS I-mode varactor as tuning element. The two other VCOs (otherwise identical) employ devices with STI either with or without p^+ connections to tune the frequency.
All VCOs consume equally 7.5mW at a 2.5V power supply and achieve a measured phase noise of -117dBc/Hz and a figure of merit of -180.3dBc/Hz at a 1MHz offset from a 4.0GHz carrier, fulfilling UMTS Tx (transmit) frequency tuning and phase noise specifications.
UMTS stands for "Universal Mobile Telecommunicatios System" also 3G, third generation. Tx frequencies are 1900MHz-2025MHz and phase noise specification of -147dBc/Hz at 20Mhz offset is set by the antenna filter and

the maximum allowed power in the neighbouring GSM1800 band.
Fig. 5.4 shows a die photo and the layout of two VCOs on one chip (1mm x 1mm). Inductor size is 115μm x 115μm.

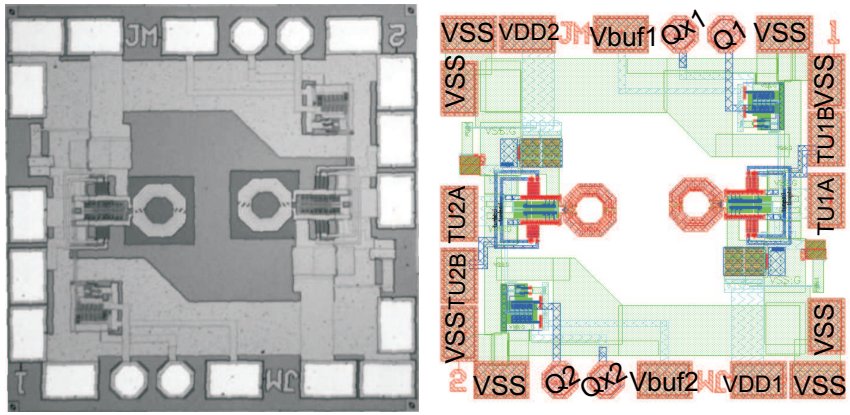


Figure 5.4: Die photograph of two VCOs on one chip (left) and layout (right).

5.2.1 Passive elements of the LC-tank

The design data of the NMOS varactor and the two devices with STI used for tuning the VCOs is given in Table 5.1. Additionally a large device with STI has been included to show its tuning potential. The poly gate of all devices with STI is p^+-doped whereas the NMOS varactor has n^+-doped gates, resulting in different transition voltages. A detailed discussion of the varactors can be found on pages 54ff, 58 and 66.
The gate areas are similar (ca. 100μm^2) and aimed at reaching UMTS Tx frequencies.
The differential, symmetrical inductor in the VCOs has been described in section 4.3.1, page 89. It features an inductance of 3.7nH and a DC-resistance of 16.7Ω. The quality factor reaches a maximum value above 7.5.

Table 5.1: Design data of the varactors.

	gate length	finger length	fingers	STI width	distance gate - n^+
with STI	0.32μm	8μm	2x42	0.49μm	0.16μm
with STI and p^+	0.32μm	8μm	2x42	0.49μm	0.16μm
conv. NMOS	0.35μm	3μm	2x96	n.a.	0μm
with STI and p^+, large	0.64μm	16μm	30	0.49μm	0.16μm

5.2.2 VCO performance

VCO frequency tuning

For frequency tuning of the VCO considering the capacitance behaviour of the varactors is essential (Fig. 5.5).

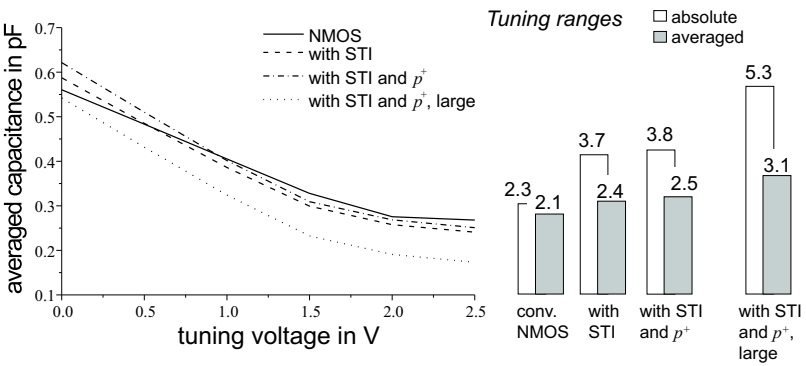


Figure 5.5: Measured averaged capacitances and capacitance tuning ranges of the varactors ($f = 2$GHz).

The NMOS varactor reaches a $C_{ratio} = C_{max}/C_{min}$ of 2.3 and is clearly outperformed by the devices with STI, which offer 3.7 up to 5.3. The same applies to the more meaningful averaged capacitance tuning ranges. With STI the devices reach $C_{av,ratio}$ values up to 2.5 and promise larger VCO

frequency tuning ranges than the NMOS varactor with 2.1. The reduction from absolute to averaged capacitance tuning ranges is stronger for the accumulation mode devices than for the NMOS varactor, as the transition from depletion to accumulation is smoother than the transition to inversion.
The averaged capacitances show that for reaching the same oscillation frequency the tuning voltages differ up to 0.6V. This results mainly from the different transition voltages and the slightly larger (ca. 7%) gate area of the devices with STI.

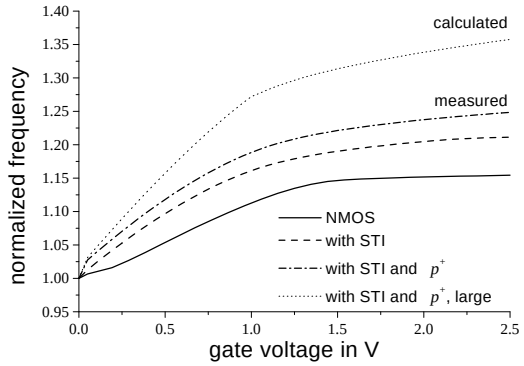


Figure 5.6: Measured and normalized frequencies of the UMTS VCOs.

Fig. 5.6, displaying normalized frequencies f/f_{min} versus tuning voltage, demonstrates the advantage of the devices with STI. The NMOS varactor allows a frequency tuning ratio f_{ratio} of 1.15 ($\pm$7%), compared to the STI-design with 1.21 ($\pm$11%) and 1.25 ($\pm$13%) with p^+ regions. Calculated values for the varactor with STI and larger finger dimensions reveal a f_{ratio} of 1.36 ($\pm$18%).
The measured frequency tuning ratios are significantly lower than what was expected from averaged capacitance tuning ranges, which is a result of the parasitic capacitances $C_{pC} \approx 600$fF of the rest of the circuitry (see Eq. 2.11). This demonstrates the importance of reducing parasitic capacitances wherever possible.
Table 5.2 summarizes absolute VCO frequencies for the three different varactor designs.

Table 5.2: Measured absolute oscillation frequencies. Frequency is divided by two to meet UMTS specifications.

Design	f_{min} in GHz	f_{max} in GHz	f_{max}/f_{min}
conv. NMOS	3.51	4.04	1.15
with STI	3.37	4.07	1.21
with STI and p^+	3.28	4.11	1.25

VCO phase noise

Phase noise measurements have been carried out over the whole range of frequencies. But to obtain a meaningful comparison of the performance equal carrier frequencies have been chosen, 3.5GHz and 4.0GHz.
Phase noise due to thermal noise is determined by the quality factors of the devices in the VCO. Fig. 5.7 depicts the averaged quality factor as function of the averaged capacitance. Via

$$f = \frac{1}{2\pi\sqrt{L(C_{av} + C_{pC})}} \tag{5.1}$$

with C_{pC} the constant parasitic circuit capacitances and L the constant inductance the x-axis corresponds to a frequency axis. Averaged capacitances corresponding to the oscillation frequencies 3.5GHz and 4.0GHz are indicated.
The NMOS varactor reaches the largest values. The long resistive path through the n^- well results in lower values for the device with STI. The further reduction due to p^+ regions has been explained before (see page 68).
An important message in Fig. 5.7 is given through the line indicating the maximum 3dB quality factor of a typical integrated inductor in the technology (ca. 10). The quality factors of all varactors are well above the quality factor of the inductor. Therefore it is expected, that independent of the type of varactor (and inductor), the inductor will determine the worst case quality factor of the LC-tank.
Fig. 5.8 depicts phase noise measurements at both frequencies, 3.5GHz and 4.0GHz. The results at 4.0GHz verify that the quality factors of the devices with STI are large enough not to influence the phase noise negatively. All three measured VCOs exhibit essentially the same phase noise with less than -117dBc/Hz at a 1MHz offset.

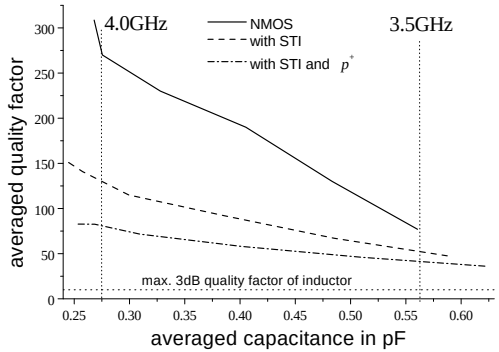


Figure 5.7: Measured averaged quality factors of the varactors. Averaged capacitances corresponding to f =3.5GHz, 4.0GHz are marked.

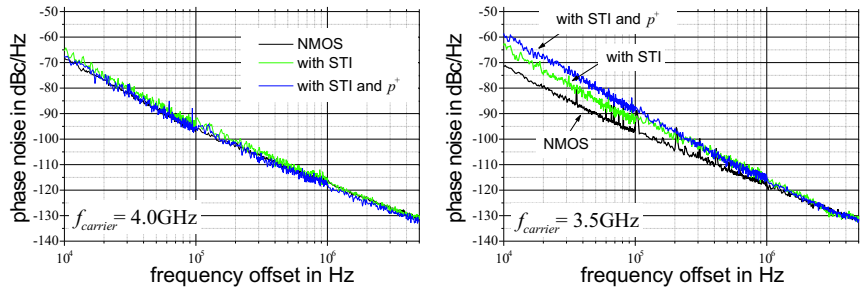


Figure 5.8: Phase noise measurements at carrier frequencies 4.0GHz and 3.5GHz.

However, at a carrier frequency of 3.5GHz there is a slightly different picture. The close-in phase noise is higher for the VCOs using varactors with STI. Yet, this cannot be negatively attributed to the STI-design, as this behaviour is inherent to tuning with MOS varactors. It has been explained that tuning of the capacitance is achieved by shifting the transition voltage to higher gate voltages. Therefore a varactor with higher capacitance tuning range can only be obtained when already the capacitance variation with gate voltage (from depletion to accumulation/inversion) is larger. In some tuning voltage range the transition will be observed within the usable gate voltage range.

Thus the capacitance variation in each period of the oscillation will be larger resulting in a less symmetric waveform and stronger upconversion of flicker noise.
A measure for the capacitance variation with gate voltage is the tuning voltage dependent relative capacitance variation

$$\frac{\Delta C}{C_{av} + C_{pC}}, \tag{5.2}$$

with ΔC the averaged deviation from C_{av}

$$\Delta C = \frac{1}{V_{dd}} \int_{0V}^{V_{dd}} |C(V_{gate}) - C_{av}| \mathrm{d}V_{gate}. \tag{5.3}$$

Fig. 5.9 shows this parameter for the three varactors in the VCOs as a function of the averaged capacitance (oscillation frequency).

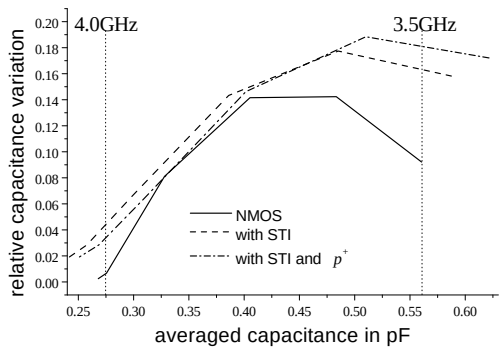


Figure 5.9: Relative capacitance variation of the varactors extracted from measurements.

At the averaged capacitance for $f = 3.5$GHz the varactor with STI and p^+ regions shows the highest relative capacitance variation, the conventional NMOS varactor the lowest. This explains the phase noise results with highest close-in phase noise for varactors with p^+ regions and lowest for the NMOS varactor.
The identical results above 1MHz offset demonstrate that also at 3.5GHz

the different quality factors of the varactors do not have an influence.
The relative capacitance variations of the three varactors differ at 4.0GHz also. However, at 4.0GHz the absolute value is much smaller than at 3.5GHZ. Thus the variations are less effective and do not show as different phase noise of the oscillators.
Despite the behaviour at 3.5GHz, phase noise specifications for UMTS applications are fulfilled. Additionally the offset frequencies, at which increased phase noise is observed, are well within the bandwidth of the PLL [49], and thus do not negatively influence the phase noise of the total system (see page 38).

VCO pushing

Variations in supply voltage result in variations of the oscillation frequency, as varying V_{dd} leads to varying values of the varactor's averaged capacitance (Eqs. 2.21, 2.9). Pushing, this sensitivity of oscillation frequency to variations of supply voltage is defined as

$$K_{Vdd} = \frac{\mathrm{d}f}{\mathrm{d}V_{dd}} \tag{5.4}$$

with units MHz/V (Fig. 5.10).
Maximum sensitivities occur at medium tuning voltages whereas close to V_{dd} the influence of the supply voltage is lowest. The proposed devices show larger variations with supply voltage with maximum values of 360MHz/V and 380MHz/V (with p^+) compared to the NMOS varactor with 270MHz/V (Fig. 5.10). Further the maxima are shifted towards lower tuning voltages. With

$$f = \frac{1}{2\pi\sqrt{LC_{av}}} \tag{5.5}$$

and C_{av} as defined in Eq. 2.9 it can be shown that the variation of frequency with supply voltage $\frac{\mathrm{d}f}{\mathrm{d}V_{dd}}$ (pushing) is determined by the varactor parameter

$$-\frac{dC_{av}}{dV_{dd}} \propto -(C(V_{dd}) - C_{av}). \tag{5.6}$$

$C(V_{dd})$ is the tuning voltage dependent capacitance at $V_{gate} = V_{dd}$, C_{av} the corresponding averaged capacitance.

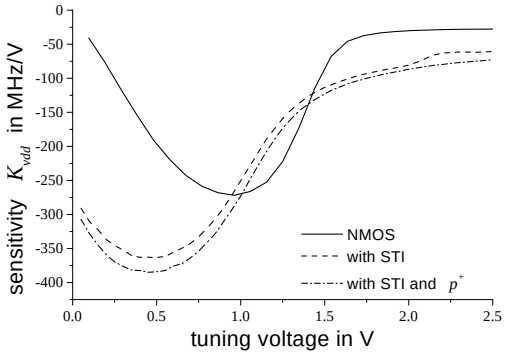


Figure 5.10: Measured VCO pushing.

Fig. 5.11 compares this parameter for all three varactors.
A good qualitative agreement between the varactor parameter and the VCO pushing behaviour is obtained. With the proposed parameter a method to predict the pushing behaviour of different VCOs is at hand.
The ca. 0.5V different location of the maxima within each graph results from the ca. 0.5V different transition voltages of the NMOS varactor and the devices with STI (depletion to inversion/accumulation).

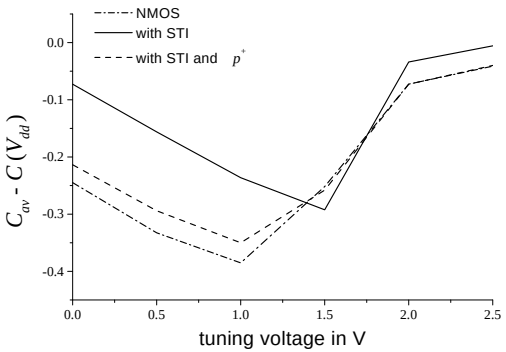


Figure 5.11: The parameter $-(C(V_{dd}) - C_{av})$ of all three devices (extracted from measurements).

5.3 Influence of the MOS varactor gate doping on VCO performance

This section presents the influence of the polysilicon type of the MOS varactor on the tuning range and phase noise of a fully integrated LC-VCO. Two identical VCOs differing only in the varactor (n- or np-doped gates) are compared in standard 0.12μm CMOS technology.
The varactor with completely p^+-doped gates has not been used for implementation in a VCO, because its averaged capacitance tuning range is much lower than with n or np gates (see Fig. 5.13).
Fig. 5.12 shows a die photo of one VCO. Die and inductor size are 450μm x 1mm and 190μm x 190μm, respectively.
Current consumption of both VCOs is 1mA from a 1.5V supply voltage. They show a measured phase noise of -115dBc/Hz and a figure of merit (FOM) of -185.3dBc/Hz at a 1MHz offset from a 4GHz carrier.

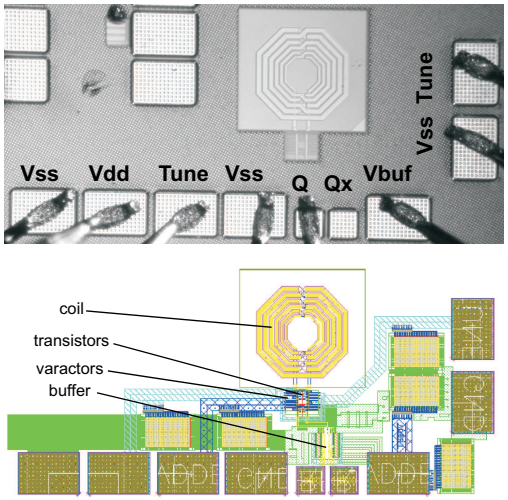


Figure 5.12: Die photograph and layout of one VCO. Metal fill structures are suppressed in the area of the inductor and the VCO-core.

5.3.1 Passive elements of the LC-tank

Varactors

The devices tuning the VCOs are A-mode varactors with STI with either homogeneously n-doped or alternating n- and p-doped gate fingers (mixed doping, np gates). The varactors have been discussed in detail in section 3.2.5, page 63.
Section 4.3.2(page 91) treats the differential, symmetrical inductor featuring an inductance of 4.4nH and a DC series resistance of 4.7Ω. In the frequency range of interest (3GHz-4GHz) the quality factor according to bandwidth definition is between 11.6 and 14.8 with higher quality factors at higher frequencies.

5.3.2 VCO measurements

VCO frequency tuning

For the frequency tuning of the VCO the varactors' capacitance behaviour has to be taken into account (Fig. 5.13; p doping included for comparison).

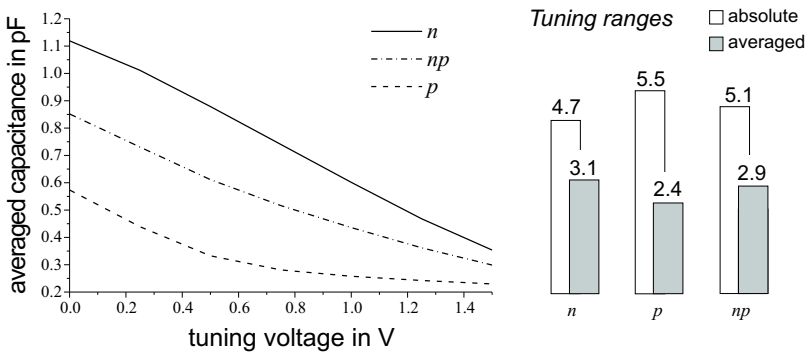


Figure 5.13: Measured averaged capacitance and capacitance tuning ranges (f = 2GHz).

The varactor with mixed doping reaches a lower averaged capacitance tuning range and also the absolute values of the averaged capacitance are lower than with n doping.
The measured normalized frequencies of the two VCOs (Fig. 5.14) reveal a lower frequency tuning range but more linear behaviour with mixed gate doping.
With a n-doped varactor the VCO offers a tuning of 1.31GHz (±20%), with mixed doping 1.06GHz (±15%) is reached. The lower f_{max}/f_{min} value is a direct consequence of the lower averaged capacitance tuning range of the varactor with np gates.
Further the lower absolute values of averaged capacitance with mixed doping shift the oscillation frequencies of the VCO to higher values.
A large difference between absolute and averaged values is possible. Further, a device with higher absolute capacitance tuning range may even lead to a lower averaged value and thus to a lower frequency tuning range. This demonstrates that the averaged capacitance tuning range really is the more important figure than the absolute value.
The more linear behaviour results from the flatter and therefore smoother gate voltage dependent capacitance behaviour with np gates. It significantly eases the phase locking process and therefore PLL-design. Usually complicated designs are necessary to solve the non-linearity problem. Herein a way is demonstrated to provide a simple solution at the device level.

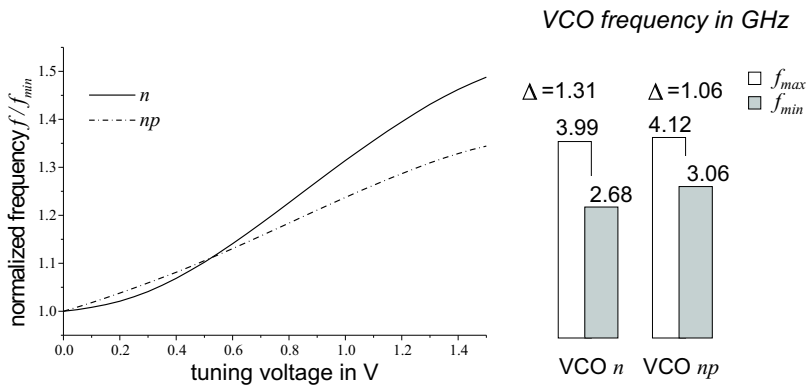


Figure 5.14: Measured normalized and absolute VCO oscillation frequencies.

VCO phase noise

Phase noise will be compared for both VCOs at the same frequencies

$$f \propto \frac{1}{\sqrt{C_{av}(V_{tune}) + C_{pC}}} \tag{5.7}$$

with C_{pC} the parasitic capacitances in the rest of the VCO. For the same carrier frequency the varactors need to have the same averaged capacitance and therefore the tuning voltage for the n-doped varactor is higher (Fig. 5.13).
Phase noise due to thermal noise is characterized by the quality factors of the devices in the VCO. Fig. 5.15 depicts the averaged quality factor as function of the averaged capacitance and the maximum 3dB quality factor of the inductor. At large averaged capacitance (low frequencies) the n-doped varactor features higher quality factors than the device with np gates. However below 0.55pF (above ca. 3.5GHz) the situation is reversed.
In the frequency range of interest the quality factor of the inductor is always lower than the values the varactors achieve, and it is expected that mainly the inductor determines the phase noise of the VCO due to thermal noise (especially at low capacitances/high oscillation frequencies).

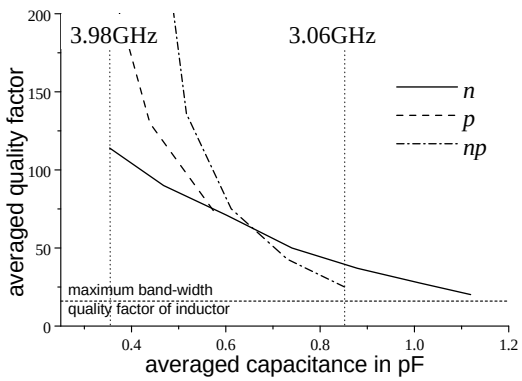


Figure 5.15: Measured averaged quality factors of the varactors. Averaged capacitances corresponding to f =3.06GHz and 3.98GHz are marked.

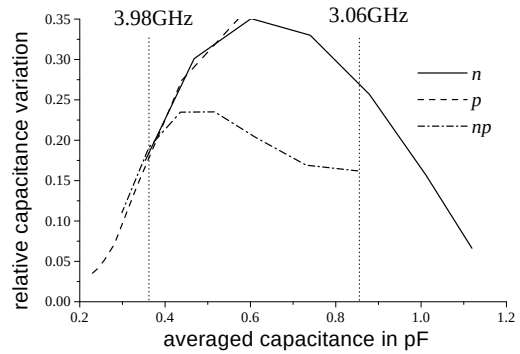
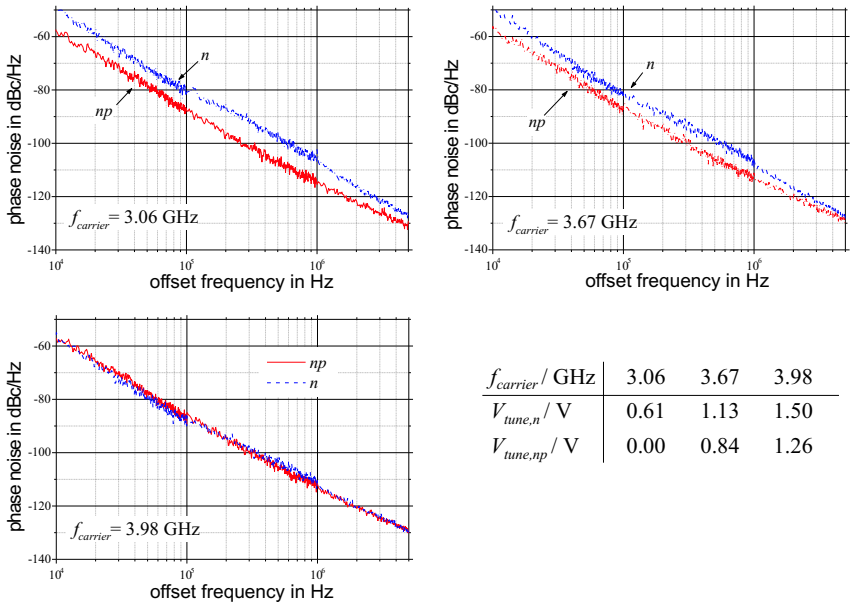


Figure 5.16: Relative capacitance variation of the varactors extracted from measurements. Averaged capacitances corresponding to f =3.06GHz and 3.98GHz are marked.

The newly introduced parameter of relative capacitance variation $\frac{\Delta C}{C_{av}+C_{pC}}$ provides insight to the extent of upconversion of flicker noise (see page 112). $C_{pc} \approx 250fF$ results from comparing the frequency tuning range with averaged capacitances. C_{pc} is lower than for the UMTS VCO in the previous section mainly due to the inductor, which is realized in copper layers 4,5,6 instead of aluminum layers 2,3,4.
At all averaged capacitances (i.e. VCO frequencies) the mixed doping varactor features lower or approx. equal relative capacitance variation.
Additionally another parameter that is believed to influence the close-in phase noise the maximum slope dC/dV_{gate} is halved with np gates due to the smoother two-transition behaviour.
The two considered parameters are related as $\Delta C(V_{tune})$ is an integral of the slope over the whole range of gate voltages.
At a given VCO frequency (given C_{av}) both, the capacitance variation ΔC as well as the maximum slope dC/dV_{gate} are lower for mixed doping (see page 66). Thus it is not possible to distinguish the importance of a single parameter. But it can be expected that upconversion of flicker noise is always less pronounced in the VCO with the mixed gate doping varactor.



$f_{carrier}$ / GHz	3.06	3.67	3.98
$V_{tune,n}$ / V	0.61	1.13	1.50
$V_{tune,np}$ / V	0.00	0.84	1.26

Figure 5.17: Phase noise measurements at 3.06GHz, 3.67GHz and 3.98GHz.

Fig. 5.17 shows the measured phase noise for frequencies between 3GHz and 4GHz. At 3.06GHz the VCO with mixed doping varactor features significantly lower phase noise throughout the entire offset frequency range. This is despite the lower minimum averaged quality factor with *np* doping at the relevant tuning voltages. The lower phase noise is explained by the fact that making the waveform more symmetric by lower relative capacitance variation of the varactor has a large advantageous effect on the phase noise [16]. Only well above 5MHz offset the results converge for both VCOs, indicating a very wide $1/\Delta f^3$ region with the n varactor.
The phase noise of the VCO with *np* varactor is lower at 3.67GHz also, but the difference between the two VCOs is less pronounced.
For the close-in phase noise at high frequencies the type of polysilicon does not play a role. Both VCOs reach the same phase noise, as the relative capacitance variations are similar for both varactors.

VCO pushing

Fig. 5.18 shows measured pushing results for both VCOs. Mixed doping reduces the maximum sensitivity to variations in supply voltage ($K_{vdd,max}$) by 20% from 800MHz/V with n gates to 600MHz/V.

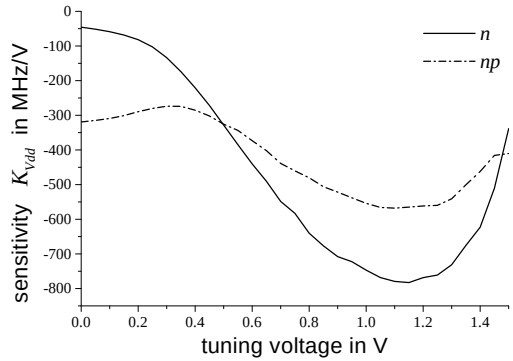


Figure 5.18: Measured pushing of the VCO.

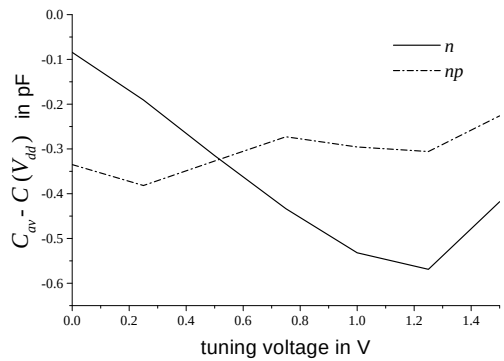


Figure 5.19: The varactor parameter $-(C(V_{dd}) - C_{av})$ extracted from measurements.

In the previous section (page 113) a varactor parameter $C_{av} - C(V_{dd})$ has been introduced to describe and explain pushing of the VCO. Fig. 5.19 compares this parameter for the two varactors with n- and np-doped gates. Again a good agreement between varactor (Fig. 5.19) and VCO data (Fig. 5.18) is obtained.

5.4 Switching varactors

5.4.1 Switched capacitor concept

The oscillation frequency is not only sensitive to variations in supply voltage, but naturally to variations in tuning voltage, denoted as K_{VCO} in units MHz/V which is derived from the frequency characteristic by

$$K_{VCO} = \frac{\mathrm{d}f(V_{tune})}{\mathrm{d}V_{tune}}. \tag{5.8}$$

Desired frequency tuning and undesired frequency fluctuations due to tuning voltage variations have the same origin. Thus low sensitivity to tuning voltage seems to be contradictory to a desired large frequency tuning range. One way to overcome this problem are switched capacitors [47, 7, 10]. This means that instead of only one varactor for continuous tuning a capacitor/varactor array for discrete tuning is used additionally to a continuously tuned varactor (Fig. 5.20).

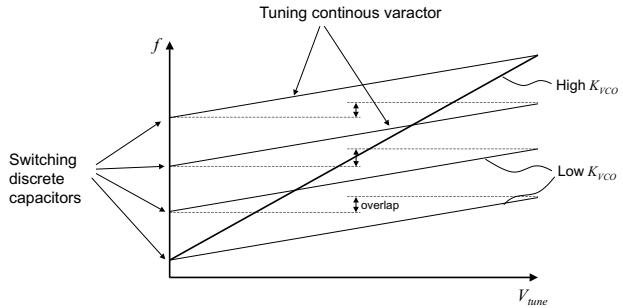


Figure 5.20: Switched capacitor concept versus tuning with one varactor only.

In a conventional VCO with only one varactor a large capacitance tuning range is necessary to cover a large frequency tuning range. With the switched concept selectively switching discrete capacitors and then continuously varying the tuning voltage of a varactor with possibly low capacitance tuning range can also result in large frequency tuning ranges. The tuning characteristics with two consecutive discrete capacitors need to overlap (or at least touch) in order to cover the whole frequency range. The sensitivity to variations in tuning voltage is reduced, since the slope in Fig. 5.20 corresponds to K_{VCO}.
Theoretically switched capacitors allow achieving any frequency tuning range. Therefore the concept is often used for LC-oscillators with bond wire inductors, to compensate for the considerable inductance variations.
Metal-insulator-metal (MiM) capacitors can provide the discrete tuning. However these MiMcaps are not necessarily available in standard, low-cost technologies. Therefore MOS-capacitors are also used for discrete tuning, by switching the tuning voltage between a low and a high value [49]. In all cases care has to be taken in the design of the RF switches to not influence the phase noise negatively. Additionally the gate of the "discrete" MOS varactors are coupled to the tank, and their gate voltage dependent capacitance has an influence on the performance of the VCO also.

5.4.2 VCO measurements

In this section the influence of switching varactors is investigated with the help of the VCO with the n-doped varactor from the previous section. The total varactor is divided 40%/60%. The tuning voltage of each part can be varied independently.

VCO frequency tuning

The frequency tuning range with partly fixed varactor is given by

$$\frac{f_{max}}{f_{min}} = \sqrt{\frac{C_{var,max} + C_{av,fix} + C_{pC}}{C_{var,min} + C_{av,fix} + C_{pC}}}. \tag{5.9}$$

$C_{var,max}$ and $C_{var,min}$ denote the maximum and minimum capacitance values of the continuously tuned part, $C_{av,fix}$ describes the constant averaged capacitance of the fixed part and C_{pC} the parasitic capacitances in the circuit. Reducing the size of the continuous varactor reduces the frequency tuning range, because simultaneously the constant capacitances increase and the variable decrease.
For tuning measurements one part of the varactor is exemplarily either biased at 0V or V_{dd}, the tuning voltage of the other part varies between the minimum and maximum voltage (Fig. 5.21). The frequency tuning characteristic for tuning the total varactor is obtained also.

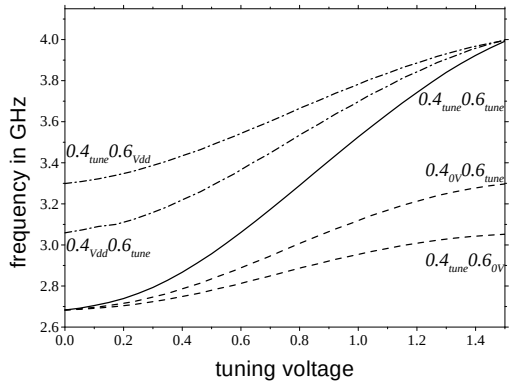


Figure 5.21: Measured tuning results with partly switched varactor. The index "*tune*" indicates which part of the varactor is continuously tuned.

As predicted and explained by Eq. 5.9 the frequency tuning range is lowest when the smaller part of the varactor (40%) is continuously tuned, highest when the entire varactor is tuned. When selecting the tuning procedure attention has to be paid that it must be possible to tune to all frequencies. Fixing the tuning voltage of either part at V_{dd} instead of 0V results in the minimum averaged capacitance of this "discrete part" and shifts frequencies at zero tuning voltage to higher values. The shift is larger with the larger varactor part as discrete capacitance, because the absolute capacitance shift is higher.
Switching varactors reduces the slope of the frequency curves corresponding

to lower sensitivity to tuning voltage variations, although the same frequency tuning range can be covered.

VCO phase noise

From Fig. 5.21 it becomes clear that for each frequency (except f_{max} and f_{min}) there are numerous ways to bias the two parts of the varactor.
The frequency $f = 3.06$GHz of the VCO with n-doped varactor results (for example) from the three bias conditions listed in Table 5.3.

Table 5.3: Bias conditions for $f = 3.06$GHz (some examples).

V_{bias} of 0.4 part	0.6V	1.0V	1.6V
V_{bias} of 0.6 part	0.6V	0.3V	0V

Although the oscillation frequency is the same the phase noise results for the different tuning possibilities can vary considerably (Fig. 5.22).

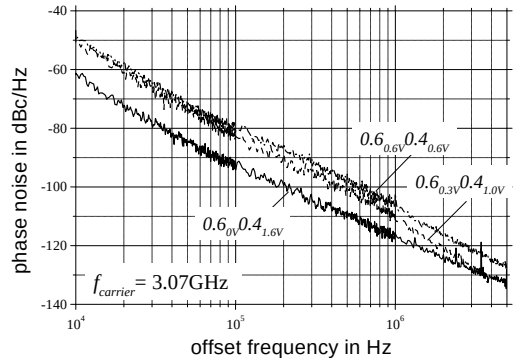


Figure 5.22: Measured phase noise results with subdivided varactor.

Tuning the entire varactor leads to the highest close-in phase noise and $1/\Delta f^3$ corner. Biasing the small varactor part at highest voltage results

in overall lowest phase noise. As in each case the frequency determining averaged capacitance has to be equal (and also C_{pC}) the extent to which flicker noise is upconverted is described by the total (from both varactor parts) capacitance variation over signal period ΔC_{total}. This figure can be calculated from the measurement results of the entire varactor by e.g.

$$\Delta C_{total}(0.4_{1.0V}0.6_{0.3V}) = 0.4\Delta C(V_{tune} = 1.0\text{V}) + 0.6\Delta C(V_{tune} = 0.3\text{V}) \tag{5.10}$$

with ΔC according to Eq. 5.3 and shown in Fig. 5.23.

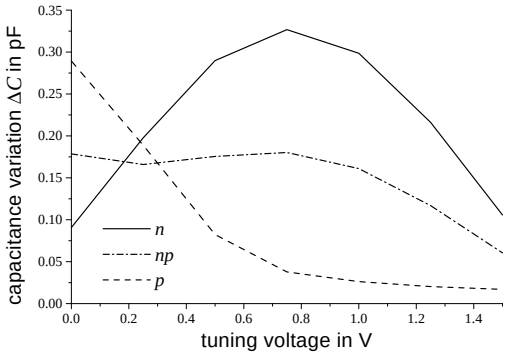


Figure 5.23: ΔC of the varactors with different gate doping extracted from measurements ($f = 2$GHz).

ΔC of the entire varactor is low at low tuning voltages, since the device is in accumulation at almost all gate voltages and shows a flat capacitance characteristic. At medium tuning voltages the entire transition from depletion to accumulation occurs during the signal swing resulting in high ΔC. At high tuning voltages the varactor stays in depletion for a wide range of gate voltages and again the capacitance characteristic is flat and thus ΔC is small.
Table 5.4 summarizes ΔC_{total} for the various biasing conditions and relates them to the phase noise results, underlining again how low ΔC_{total} corresponds to low close-in phase noise.

Table 5.4: Bias conditions and corresponding total ΔC extracted from measurements ($f = 3.06$GHz).

V_{bias} of 0.4 part	0.6V	1.0V	1.6V
V_{bias} of 0.6 part	0.6V	0.3V	0V
total ΔC	0.30pF	0.25pF	0.10pF
$1/f^3$ corner	highest	—	lowest

With the help of the ΔC versus tuning voltage behaviour of the varactor the optimum bias condition (i.e. minimum ΔC_{total}) for the varactor's parts in the VCO can be found to condition lowest possible phase noise at a given frequency.
These optimum conditions differ for varying types of varactors, as the ΔC characteristics are not similar even qualitatively. As an example may serve the varactors with different gate doping (Fig. 5.23) from section 3.2.5, where the different ΔC vs. tuning voltage behaviour is obvious.

VCO pushing

For pushing measurements one part of the varactor is either biased at 0V or V_{dd}, the tuning voltage of the other part varies in between. Results for tuning the entire varactor are obtained also, and have been discussed in detail in section 5.3.2. Fig. 5.24 depicts the measurement results.
Using part of the varactor as discrete capacitor can reduce pushing considerably from a maximum value of 780MHz/V to as low as 250MHz/V. The reductions are stronger when fixing the larger part, 60%, of the varactor. In this case simultaneously the constant capacitances are large and capacitance variations leading to frequency variations are low, as

$$C_{total} = C_{av,var} + C_{av,fix} + C_{pC}. \tag{5.11}$$

Although the tuning voltage of the discrete part is fixed the device nevertheless contributes to K_{Vdd}. From the pushing characteristic of the entire varactor it is clear that the influence of the fixed capacitor is more pronounced when connecting its tuning voltage to V_{dd}, explaining that biasing the discrete capacitor at 0V instead of V_{dd} advantageously reduces pushing. Covering the same frequency tuning range as the entire varactor switching

40% and tuning only 60% reduces the maximum pushing by more than 38% from 780MHz/V to 480MHz/V.

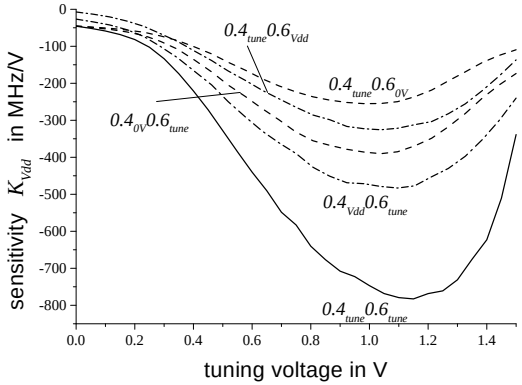


Figure 5.24: Measured pushing results with subdivided varactor.

Due to the measurement procedure the pushing characteristics do not coincide at the maximum tuning voltage. The supply voltage variations externally introduced to measure the sensitivity K_{Vdd} appear at the discrete varactor as varying tuning voltage. The continuously tuned varactor however received a constant tuning voltage. Small increases (decreases) of the tuning voltage have the opposite effect on frequency as small increases (decreases) of the VCO supply voltage.

5.5 Conclusion

This chapter demonstrates the suitability of the A-mode varactors with STI for fully integrated VCOs and shows ways to improve VCO performance.
The complementary VCO topology without current source is identified as optimum with respect to power consumption and phase noise and is used for all VCOs herein.
Varactor parameters have been introduced that predict the frequency tuning behaviour, the influence of the varactor on the $1/\Delta f^2$-and $1/\Delta f^3$-portion of

the phase noise and explain the pushing behaviour of the VCO.
Compared to a conventional NMOS varactor, the A-mode devices with STI increase the frequency tuning range of a VCO in standard digital 0.25μm CMOS technology from $\pm$7% to $\pm$13%. In the 0.12μm technology even a tuning range of $\pm$20% has been achieved. Figure of merits (FOM) are -180.3dBc/Hz in 0.25μm and -185.3dBc/Hz in 0.12μm technology, each at a 1MHz offset from a 4.0GHz carrier.
Higher capacitance tuning ranges have the undesired consequence of stronger distortion of the the signal waveform which upconverts flicker noise. Further higher sensitivity to variations in supply and tuning voltage result. However, these effects can be significantly reduced, if either varactors with mixed *np* gate doping are used or the whole varactor is divided in two or more parts where only one part is continuously tuned and the other part(s) are switched in discrete steps. Mixed gate doping has the further advantage of yielding very linear VCO frequency tuning which significantly eases PLL design.

Chapter 6

Modelling and simulation

Accurate device models are the basis for any circuit design. Therefore this chapter describes the development of a model for the A-mode varactor with STI and its application to simulating a fully integrated LC-VCO.

6.1 Modelling of the A-mode varactor with STI

The varactor modelled in this section is the A-mode varactor with STI as described in 3.1.1 and 3.2.3. Little modifications are needed to accommodate the other structures based on this device.

6.1.1 Varactor structure and lumped elements

To model the device it is very helpful to first visualize the lumped elements in the device (Fig. 6.1).

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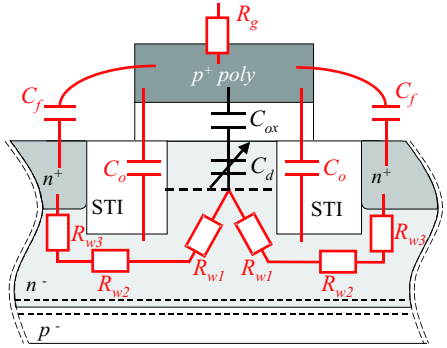


Figure 6.1: Lumped elements in the A-mode varactor with STI.

Simple formulas for the total resistance R and the capacitance C can be found, when assuming a small overlap capacitance C_o

$$\begin{aligned} R &= R_g + \tfrac{1}{2}(R_{w1} + R_{w2} + R_{w3}) \\ C &= (C_{ox}^{-1} + C_d^{-1})^{-1} + 2(C_f + C_o). \end{aligned} \tag{6.1}$$

6.1.2 Physical modelling

Fig. 6.2 shows the model of the device derived from the lumped elements (Fig. 6.1).

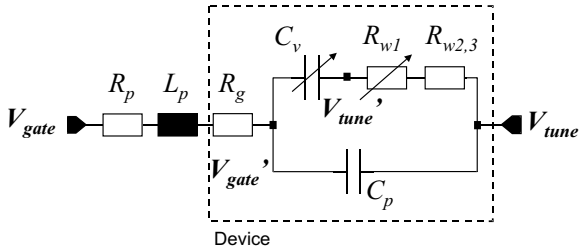


Figure 6.2: Physical model of the A-mode varactor with STI.

The dashed box indicates the five elements describing the device itself: the gate resistance R_g, the variable capacitance C_v (series connection of C_{ox} and C_d), the variable well resistance R_{w1} and the constant well resistances R_{w2} and R_{w3}. The parasitic capacitance C_p includes overlap and fringing capacitances and is parallel to C_v and the well resistances.
The wiring within the varactor introduces the parasitic resistance R_p and the inductance L_p. Although there is no general formula for R_p and L_p, values can be extracted from the sizing of the wiring and the type of metal used.
In determining overlap and fringing capacitances many distributed effects are encountered, so no simple formula for C_p is available.

Variable capacitance

The variable capacitance is modelled as the derivative of the gate charge with respect to the gate voltage. The total gate charge Q_g mirrors the charge in the accumulation layer Q_{acc} or the depletion region Q_{dep}. For the mathematical expression the sum of both charges can be used

$$Q_g = -(Q_{acc} + Q_{dep}). \tag{6.2}$$

The charges are determined by the effective voltage V_{eff}

$$V_{eff} = V'_{gate} - V_{FB} - V'_{tune}. \tag{6.3}$$

V'_{gate} and V'_{tune} are the voltages at the nodes of the variable capacitance C_v (see Fig. 6.2) and V_{FB} is the flat-band voltage of the device.
Inversion through thermally generated holes had been considered, but its influence seems to be small enough to be neglected, since the varactor is operated in the GHz-range. (It can be included by using a fixed width of depletion region w_d when inversion occurs.)
The accumulation charge can be described as

$$Q_{acc} = -C_{ox} V_{eff,a} \tag{6.4}$$

with the gate oxide capacitance

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox} A_g}{t_{ox}} \tag{6.5}$$

where A_g is the gate area given by the gate length l_g times the total gate width. ϵ_0 is the permeability of vacuum, ϵ_{ox} the dielectric constant of silicon oxide, and t_{ox} is the thickness of the gate oxide. The voltage $V_{eff,a}$

$$V_{eff,a} = \frac{1}{2}(\sqrt{V_{eff}^2 + \delta_a} + V_{eff}) \tag{6.6}$$

is introduced to ensure that Q_{acc} goes to zero, when V_{eff} becomes negative, which means that the device is in depletion. δ_a functions as a smoothing parameter to obtain a smooth transition between accumulation and depletion. Assuming a homogeneous doping concentration n_1 in the area between the STIs, the following equation holds for the depletion region charge

$$Q_{dep} = qn_1 w_d A_g \tag{6.7}$$

with q the elementary charge and w_d the voltage dependent depth of the depletion region

$$w_d = \sqrt{\frac{2\epsilon_0\epsilon_{si}}{qn_1}}\sqrt{\Phi_s} = \sqrt{\frac{2\epsilon_0\epsilon_{si}}{qn_1}}\sqrt{V_{eff,d} - \frac{Q_{dep}}{C_{ox}}}. \tag{6.8}$$

Φ_s is the surface potential, ϵ_{si} is the relative dielectric constant of silicon and $V_{eff,d}$ ensures that w_d and Q_{dep} approach zero when V_{eff} becomes positive and the device is driven into accumulation. The parameter δ_d is used to smooth the transition.

$$V_{eff,d} = \frac{1}{2}(\sqrt{V_{eff}^2 + \delta_d} - V_{eff}) \tag{6.9}$$

Equation (6.8) is the solution of the poisson equation with the depletion approximation [33]. Substituting Eq. 6.8 into Eq. 6.7 and solving for Q_{dep} yields the formula needed for Q_g.

Gate resistance

To reduce the poly gate resistance R_g the varactor utilizes multi-finger layout; therefore the well known formula

$$R_g = \frac{l_f}{w_f} R_\square \frac{1}{N_F 12} \tag{6.10}$$

is applied. l_f and w_f are finger length and width, $R_\square$ the poly gate resistance per square and N_F the number of parallel fingers. As the gate fingers are contacted on both ends the factor 12 appears.

Well resistance

The well resistance R_w is the series connection of the voltage dependent R_{w1} and the constant resistances R_{w2} and R_{w3}

$$R_w = \frac{1}{2}(R_{w1} + R_{w2} + R_{w3}) \tag{6.11}$$

The constant values for R_{w2} and R_{w3} are calculated assuming a uniformly doped semiconductor rod.

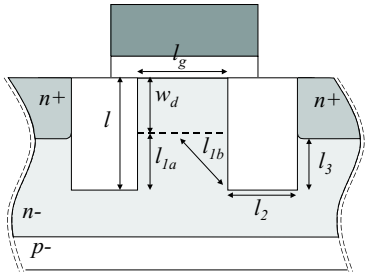
$$R_{w2,3} = \frac{l_{2,3}}{qn_{2,3}\mu_{2,3}(c_{2,3}A_{2,3})} \tag{6.12}$$

In this equation l_2 is equal to the width of the STIs and l_3 denotes the distance between the lower edge of the STI and the n^+ region (see Fig. 6.3). n_2 and n_3, respectively, are the doping concentrations near the lower edges of the STI and the n^+ regions. The (doping concentration dependent) mobilities in the respective areas are given by μ_2 and μ_3. The area A_2 is the total device width times the depth of the n^- well underneath the STI. The area A_3 is the total device width times the width of the n^+ regions. Since the current flow is not homogeneous, but rather restricted to a small part of the areas A_2 and A_3, the parameters c_2 and c_3 (with values < 1) are used. For the variable resistance R_{w1} the same considerations hold

$$R_{w1} = \frac{l_{av}}{qn_1\mu_1(\frac{1}{2}c_1A_1)}. \tag{6.13}$$

A_1 is the total device width times the gate length. The mobility in the area underneath the gate is μ_1 and the effective-area parameter due to current constriction is c_1. l_{av} is an average value of the different distances between the border of the depletion region and the lower edge of the STI (see Fig. 6.3). Contrary to l_2 and l_3 the length l_{av} is not constant, since the width of the depletion region varies with voltage. With l, the depth of the STIs, one gets:

$$l_{av} = \frac{1}{2}(l - w_d) + \frac{1}{2}\sqrt{(l - w_d)^2 + (\frac{1}{2}l_g)^2}. \tag{6.14}$$



$$l_{1a} = l - w_d$$
$$l_{1b} = \sqrt{(l - w_d)^2 + (\tfrac{1}{2} l_g)^2}$$

Figure 6.3: Length parameters of the device for the modelling of the well resistances.

For BiCMOS A-mode varactors only the constant resistance R_{w2} has to be adjusted and R_{w3} is approx. zero. The descriptions of the capacitances and the variable resistance are similar.

6.1.3 Simulation results

The model equations are implemented in VHDL-AMS (Appendix D) and simulations are carried out with *TITAN* (Infineon in-house simulator based on Spice), but the model can readily be implemented in other circuit simulators. Measurement and simulations results are compared exemplarily for the CMOS version of the A-mode varactor with STI (without p^+ or n^+ connections and 0.32μm gate length). Measurement results are extracted from S-parameters (Eq. 3.2) and AC-simulations yield the simulated values for comparison.

Simulations of A-mode varactor with STI

Fig. 6.4 depicts capacitance and resistance values at a frequency of 3.64GHz and several tuning voltages V_{tune}. The simulation results show strong agreement with measurements, which remains at other frequencies.

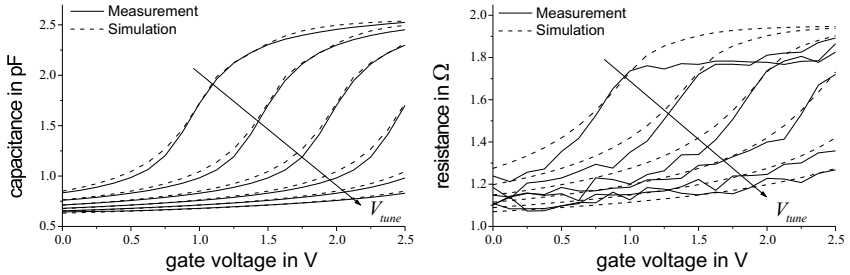


Figure 6.4: Measured and simulated small-signal capacitance and resistance of the A-mode varactor with STI and 0.32μm gate length at $f = 3.64$GHz and various tuning voltages (0V...2.5V; 0.5V steps).

Due to the parasitic inductance of the wiring the capacitance derived by Eq. 3.2 shows a dependence on frequency (Fig. 6.5). The simulated results match the measured results closely. For other tuning voltages the match is as good. The results for $V_{tune} = 0$V have been chosen for presentation, because the capacitance variation with gate voltage is largest.

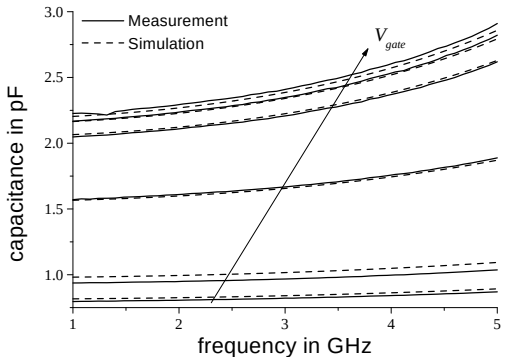


Figure 6.5: Measured and simulated small-signal capacitance of the A-mode varactor with STI and 0.32μm gate length at $V_{tune} = 0V$ and various gate voltages (0V...2.5V; 0.5V steps).

Scalability

As the variable and parasitic capacitances, as well as the series resistance depend on the device geometry (e.g. gate length, finger length, gate width, ...), it is important that the model also predicts the values for devices with other geometries correctly. The scalability is tested by applying the model to a varactor with the same gate area as before but double gate length (i.e. half gate width).
Fig. 6.6 demonstrate the good agreement between measured and simulated results for the varactors capacitance and resistance.

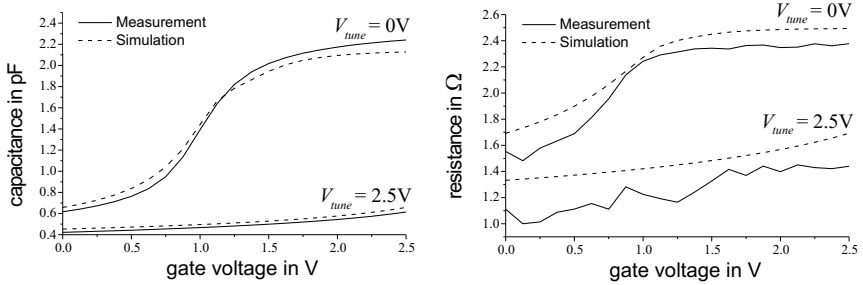


Figure 6.6: Measured and simulated small-signal capacitance and resistance of the A-mode varactor with STI and 0.64μm gate length at $f = 3.64$GHz and tuning voltages 0V and 2.5V.

6.2 VCO simulations

This section presents the simulation of the UMTS VCO using the A-mode varactor with STI as tuning element (see section 5.2). The simulated circuit includes not only the VCO but also the integrated buffer and external passive components, which are necessary for measurement and inherent to the measurement results. Simulations are carried out with the circuit simulator *TITAN* [57].

The frequency tuning of the oscillator results from a swept harmonic balance simulation. Fig. 6.7 shows the results for the VCO using the A-mode varactor with STI and the varactor model developed in section 6.1.
The simulated frequencies are in good agreement with measured frequencies. This proves that the dependence on V_{gate} and V_{tune} of the varactor's capacitance are thoroughly modelled over the whole range of oscillation frequencies.

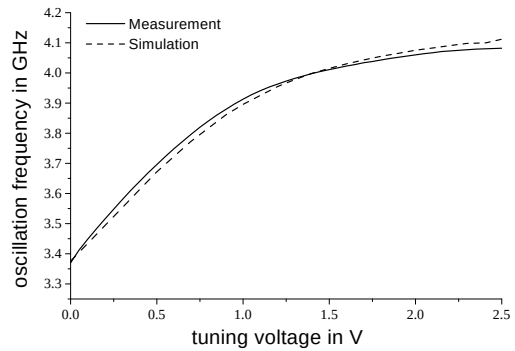


Figure 6.7: Comparison of measured and simulated oscillation frequencies of the VCO with the A-mode varactor with STI.

Harmonic balance noise analysis (periodic noise analysis of circuits in periodic steady state) provides the simulation results for the phase noise of the VCO. Fig. 6.8 demonstrates a good agreement between measured and simulated phase noise results at 3.4GHz, which is similar good at other frequencies (tested up to 4.0GHz).

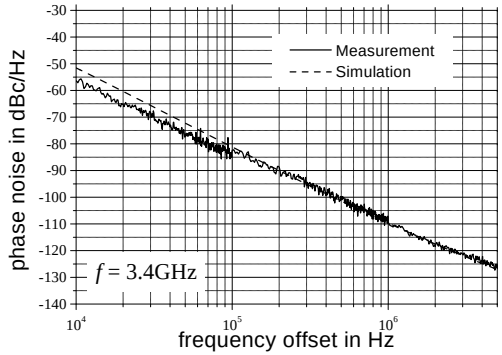


Figure 6.8: Measured and simulated phase noise of the VCO using the A-mode varactor with STI at a carrier frequency of 3.4GHz.

6.3 Conclusion

A physical VHDL-AMS model for the standard A-mode varactor has been developed and implemented in a circuit simulator. The simulated results agree well with measured values of the voltage and frequency dependent small-signal capacitance and resistance for different device geometries.
VCO simulations with the varactor model yield good agreement between measurement and simulation for key parameters of the VCO, frequency tuning and phase noise. This demonstrates the usefulness of the model for RF circuit design.

Chapter 7

Summary

This work presents varactors (variable capacitors) with improved capacitance tuning range and analyzes their performance in voltage-controlled oscillators (VCOs). Further a substrate structure for integrated inductors is proposed, which leads to significantly higher quality factors. An overview of the basic structures is given Fig. 7.1
Except two varactors in standard BiCMOS technology all devices and circuits have been realized in standard digital CMOS technologies.

The proposed accumulation mode varactors incorporate shallow trench isolation (STI) within the device. Thereby reduced parasitic capacitances result in the largest reported capacitance tuning ranges (for the used gate length). Although the resistance at minimum gate length is higher in the proposed varactor and thus the quality factor lower than in conventional devices, the achieved values are high enough to meet UMTS specifications when used in VCOs.
Increasing gate length improves tuning range for both, proposed and conventional, types of varactors since the ratio of variable to parasitic capacitance improves. But simultaneously the resistance in conventional varactors increases proportional to gate length and the quality factor is significantly reduced. Contrary, in the proposed varactor the change of resistance is much smaller. Thus at longer gate lengths the proposed varactors outperform conventional MOS varactors in terms of capacitance tuning range as

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well as quality factor.
A physical and scalable VHDL-AMS model for the proposed varactor has been developed. Capacitance and resistance of the varactor as well as frequency tuning and phase noise of a VCO are accurately reproduced.

A proposed substrate structure improves the quality factor of integrated inductors by reducing the coupling between inductor and substrate. The structure consists of alternating n^--well and p^--substrate regions with voltage-controlled, variable lateral and vertical depletion regions. It increases the maximum quality factor by 41%. Simultaneously the resonance frequency at peak quality factor shifts towards higher frequencies by up to 56%. Especially at high frequencies the advantages of the proposed structure are more pronounced.

VCOs have been tested in standard digital 0.25μm and 0.12μm technologies with supply voltages of 2.5V and 1.5V, respectively.
Three VCOs in 0.25μm technology compare the proposed accumulation mode varactor with a conventional NMOS varactor. The proposed varactors increase frequency tuning range from ±7% with conventional device to ±13%. All VCOs fulfill UMTS Tx phase noise and frequency tuning specifications consuming only 7.5mW (current: 3mA). Measured phase noise is -117dBc/Hz at a 1MHz offset from a 4.0GHz carrier.
Two VCOs in 0.12μm technology describe the different performance of varactors with n-doped and mixed np-doped gates. The n varactor increases the VCO tuning range to ±20% compared to ±15% with mixed doping. The np gates however offer smoother capacitance variation with gate voltage and therefore less upconversion of flicker noise and lower close-in phase noise. Further advantages are a highly linear frequency behaviour of the VCO and a reduction of the maximum sensitivity to variations in supply voltage. Consuming 1mA from a 1.5V supply both VCOs show a phase noise of -115dBc/Hz at a 1MHz offset from a 4GHz carrier. At no extra cost mixed-doping offers a simple way to improve VCO phase noise already at the device level.

To further improve the performance of the proposed varactor several design variations are analyzed. Tuning ranges up to C_{max}/C_{min}=6 have been obtained and resistances at short gate lengths can be reduced leading to quality factors comparable to conventional MOS varactors.

In the VCO analysis new varactor parameters are proposed that can easily be extracted from device measurements. Phase noise is to a large extent

determined by the quality factor of the inductor. But also contributing is the varactor's capacitance variation over the large VCO signal swing, since it causes upconversion of flicker noise. The sensitivity of frequency to supply voltage variations can be explained by variations in the varactor's averaged capacitance.
Beside varactors with mixed gate doping the switched varactor concept with digitally operated varactor parts and continuously tuned parts is identified as a possibility to improve VCO performance.

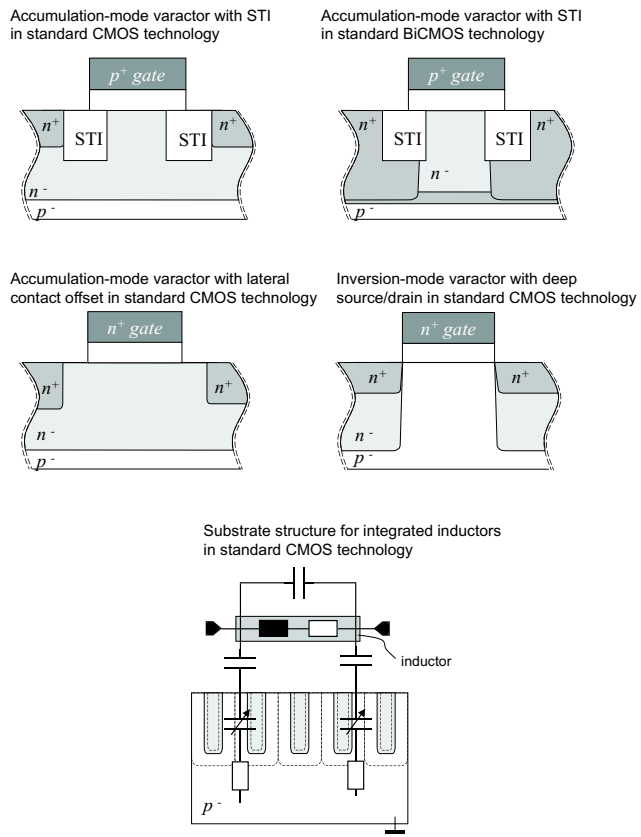

Figure 7.1: Overview of the basic structures proposed and analyzed in this work.

Appendix A

Scattering parameters

A.1 General definition

At low frequencies two-port systems are described in impedance or admittance representation. The impedance and admittance parameters relate port voltages to port currents (Fig. A.1).

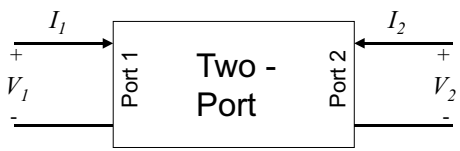

Figure A.1: Low-frequency description of two-port.

The description of the above system in impedance parameters is:

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2. \end{aligned} \tag{A.1}$$

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To experimentally determine the various parameters it is best to successively open-circuit the ports. Then several terms become zero.
Similarly the determination of admittance parameters is easiest with short-circuit conditions.
At high frequencies it is difficult to provide adequate shorts and opens. Thus different two-port parameters are necessary, the scattering parameters, S-parameters [34, 18]. The port variables for S-parameter representation are defined in terms of incident (E_{1i}, E_{2i}) and reflected = scattered (E_{1r}, E_{2r}) voltage waves

$$\begin{aligned} a_1 &= \frac{E_{1i}}{\sqrt{Z_0}} & a_2 &= \frac{E_{2i}}{\sqrt{Z_0}} \\ b_1 &= \frac{E_{1r}}{\sqrt{Z_0}} & b_2 &= \frac{E_{2r}}{\sqrt{Z_0}}. \end{aligned} \tag{A.2}$$

Thus a_1, b_1, a_2, b_2 are normalized voltage waves. The normalization is chosen to make the square of the magnitude of a variable equal to the power of the corresponding wave.

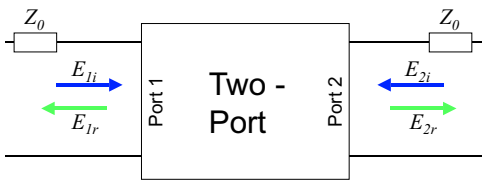

Figure A.2: High-frequency description of twoport. Z_0 is the characteristic impedance of the lines.

The complex S-parameters describe the relationship between the normalized voltage waves by

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}b_1 + S_{22}a_2. \end{aligned} \tag{A.3}$$

Determination of the parameters is based on the fact that terminating a line in its characteristic impedance (here Z_0) gives rise to no reflections. E.g.

driving port 1 with port 2 terminated in Z_0 yields $a_2 = 0$ and

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1} = \frac{E_{1r}}{E_{1i}} \\ S_{21} &= \frac{b_2}{a_1} = \frac{E_{2r}}{E_{1i}}. \end{aligned} \tag{A.4}$$

Similarly S_{21} and S_{22} can be obtained, when driving port 2 and terminating port 1.
S_{11} is the input, S_{22} the output reflection coefficient. S_{21} is some kind of gain and S_{12} is the reverse transmission.
The transmission coefficients S_{12} and S_{21} are usually depicted in polar diagrams. For the reflection parameters S_{11} and S_{22} a new type of diagram, the Smith-plot has been introduced [34].

A.2 Transformation to Y- and Z-parameters

Measured S-parameters can be transformed to Y-(admittance)-parameters and Z-(impedance)-parameters. Especially for de-embedding measurement results this is important.

$$\begin{aligned} Y_{11} &= \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} & Y_{12} &= \frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \\ Y_{21} &= \frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} & Y_{22} &= \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \end{aligned} \tag{A.5}$$

$$\begin{aligned} Z_{11} &= \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} & Z_{12} &= \frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \\ Z_{21} &= \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} & Z_{22} &= \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \end{aligned} \tag{A.6}$$

Appendix B

De-embedding

To create an environment, which is suitable for on-wafer testing wiring and pads have to be added to the DUT (device under test). To obtain results for the DUT only the influence of these additional elements has to be subtracted, i.e. de-embedded. Fig. B.1 shows a typical equivalent circuit for the DUT and parasitic elements for on-wafer measurements [51].

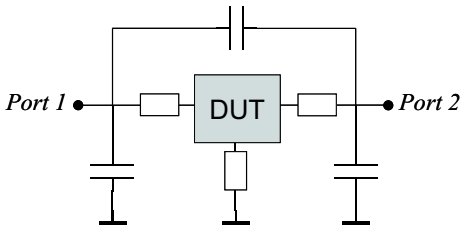

Figure B.1: Typical equivalent circuit for DUT and parasitic elements on-wafer.

Parasitic resistances (wiring) are assumed as in series to the DUT. Parasitic capacitances (mainly pads) are parallel to the DUT and the parasitic resistances.

B.1 General procedure

Most common is the 2-step de-embedding with Open and Short[51]. Open and Short are dummy devices for measuring the parasitic elements only. Fig. B.2 shows exemplarily a DUT, Open and Short and the corresponding equivalent circuits.

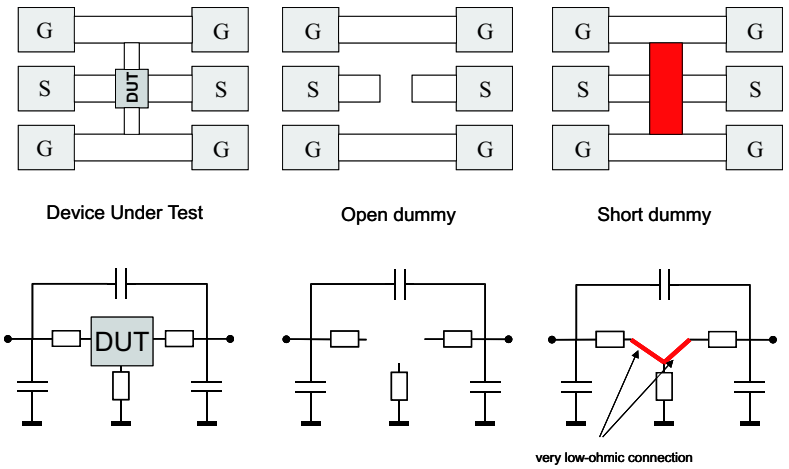

Figure B.2: DUT, Open and Short dummies (top) and the corresponding equivalent circuits.

Besides the DUT itself, which is left out, the Open dummy has identical pads and wiring. Based on the Open a Short dummy is obtained through establishing low-ohmic connections between each signal path and the ground lines. The Open dummy provides the influence of the pads only, the Short dummy the influence of the serial resistances and additionally the pads.
The procedure for Open-Short de-embedding is summarized in Table B.1.
Parallel elements, i.e. the Open, can simply be subtracted from DUT and Short in Y-matrix description (Step 1 and 2).
The resulting parameters of the DUT include the influence of the serial resistances only. These are now given by the Open de-embedded Short. Serial elements, i.e. the Short, are best subtracted in Z-matrix description

(Step 3 and 4). The conversion to S-parameters yields the parameters of DUT only.
More elaborate 3- or 4-step de-embedding methods can be found in [62, 63, 64].

Table B.1: Open-Short de-embedding.

Step 1	Convert measured S- to Y-parameters: $S_{meas,DUT} \longrightarrow Y_{meas,DUT}$ $S_{meas,Short} \longrightarrow Y_{meas,Short}$ $S_{meas,Open} \longrightarrow Y_{meas,Open}$
Step 2	De-embed DUT and short from parallel pad parasitics: $Y_{meas,DUT} - Y_{meas,Open} = Y_{DUT-Open}$ $Y_{meas,Short} - Y_{meas,Open} = Y_{Short-Open}$
Step 3	Convert Y- to Z-parameters: $Y_{DUT-Open} \longrightarrow Z_{DUT-Open}$ $Y_{Short-Open} \longrightarrow Z_{Short-Open}$
Step 4	De-embed DUT (without Open) from serial resistive parasitics (Short without Open): $Z_{DUT-Open} - Z_{Short-Open} = Z_{DUT}$
Step 5	Convert DUT's Z- to S-parameters: $Z_{DUT} \longrightarrow S_{DUT}$

B.2 Varactor de-embedding

As the gate input is directly connected to the signal pad de-embedding with Open only is accepted to be sufficient. The low ohmic (less than 40mΩ) wiring between the tune input of the varactor and the second signal pad is neglected. Thus the only steps that have to be performed to obtain the S-parameters of the DUT only are B.1.

Table B.2: Open de-embedding for varactors.

Step 1	Convert measured S- to Y-parameters: $S_{meas,DUT} \longrightarrow Y_{meas,DUT}$ $S_{meas,Open} \longrightarrow Y_{meas,Open}$
Step 2	De-embed DUT and short from parallel pad parasitics: $Y_{meas,DUT} - Y_{meas,Open} = Y_{DUT}$
Step 3	Convert DUT's Y- to S-parameters: $Y_{DUT} \longrightarrow S_{DUT}$

A serial inductance, and thus the (small) inductance of the wiring between the tune input of the varactor and the signal pad, can increase the effective capacitance and resistance (see section 3.2.10). Measurements showed that for a varactor with ca. 1.5pF gate-oxide capacitance the results with only-Open and Open+Thru de-embedding differ only negligibly up to ca. 5GHz. Above 5GHz both, Open and Thru (see next section) should be used. The inductance of the wiring was typically ca. 100pH.
The frequency below which only-Open de-embedding is sufficient increases with decreasing oxide capacitance of the varactor and inductance of the wiring (see Eq. 3.5).
In the frequency range of interest and for the varactors studied in this work only-Open de-embedding proved to be sufficient.

B.3 Inductor de-embedding

In the case of inductors Short de-embedding seems not to be applicable as the wiring from the signal pads to the RF inputs of the inductors is long (Fig. B.3). Thus the very low resistance necessary for a Short can not be realized.

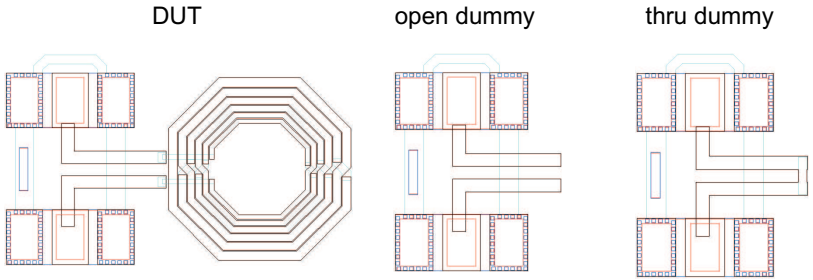

Figure B.3: Inductor with GSG pads and corresponding dummies.

Instead of Short a Thru de-embedding is applied. Based on a Open dummy a Thru is obtained with a very low-ohmic connection between the two signal pads. Fig. B.4 shows the equivalent circuit of a Thru.

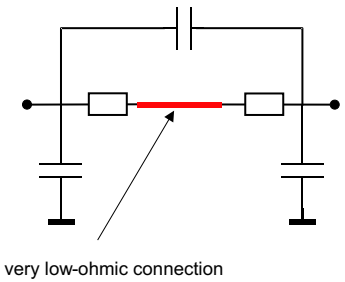

Figure B.4: Equivalent circuit of a Thru.

Similar to de-embedding with Short and Open, first the measured DUT and Thru parameters have to be de-embedded from the Open (Step 1 and 2). Contrary to de-embedding with Short the subtraction of the parasitic serial elements represented by the Thru can not be done by simple subtraction of Z-matrices. The reason is that the Thru-parameters include the total path between the two signal pads. But only a part, due to symmetry of the wiring, half of the path, has to be subtracted from e.g. $Z_{11,DUT-Open}$. Thus the procedure given in Step 4 is applied.

Table B.3: Open-Thru de-embedding for inductors.

Step 1	Convert measured S- to Y-parameters: $S_{meas,DUT} \longrightarrow Y_{meas,DUT}$ $S_{meas,Thru} \longrightarrow Y_{meas,Thru}$ $S_{meas,Open} \longrightarrow Y_{meas,Open}$
Step 2	De-embed DUT and short from parallel pad parasitics: $Y_{meas,DUT} - Y_{meas,Open} = Y_{DUT-Open}$ $Y_{meas,Thru} - Y_{meas,Open} = Y_{Short-Open}$
Step 3	Convert Y- to Z-parameters: $Y_{DUT-Open} \longrightarrow Z_{DUT-Open}$ $Y_{Thru-Open} \longrightarrow Z_{Short-Open}$
Step 4	De-embed DUT (without Open) from serial resistive parasitics (Short without Open): $Z_{11,DUT} = Z_{11,DUT-Open} - \frac{1}{2}(Y_{11,Thru-Open})^{-1}$ $Z_{12,DUT} = Z_{12,DUT-Open}$ $Z_{21,DUT} = Z_{21,DUT-Open}$ $Z_{22,DUT} = Z_{22,DUT-Open} - \frac{1}{2}(Y_{22,Thru-Open})^{-1}$
Step 5	Convert DUT's Z- to S-parameters: $Z_{DUT} \longrightarrow S_{DUT}$

Appendix C

Calculation of band-width quality factor

The figures which visualize the following explanations have been obtained using the measurement results of symmetrical, octagonal inductor with a low-frequency inductance of 6.1nH and resistance of 6.6Ω.

In section 2.2.4 it has been shown that the quality factor of choice in this work is the quality factor according to bandwidth definition. Here a more detailed description and mathematical method how to obtain Q_{BW} is given.

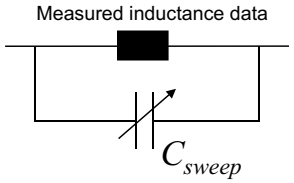

Figure C.1: Test circuit to calculate the bandwidth quality factor.

Every S-Parameter measurement of inductors will give the parameters as function of measurement frequency. It is important to notice that measure-

ment frequency and resonance frequency of the inductor or a virtual parallel connection of the inductor and a capacitor are not identical. Already the inductor alone serves as resonating LC-tank through its parasitic capacitances. The resonance frequency of the inductor alone is also called the self-resonance frequency of the inductor.
The differential amplitude responses of the inductor alone or of a virtual LC-tank with a capacitance C_{sweep} are obtained by the formulas [49]:

$$\mathrm{mag}(Z_{11} + Z_{22} - Z_{12} - Z_{21}) \qquad \text{inductor alone}$$

$$\mathrm{mag}\left(\frac{(Z_{11} + Z_{22} - Z_{12} - Z_{21})(j2\pi f C_{sweep})^{-1}}{(Z_{11} + Z_{22} - Z_{12} - Z_{21}) + (j2\pi f C_{sweep})^{-1}}\right) \qquad \text{with capacitance} \tag{C.1}$$

A typical plot of various of these functions is shown in Fig. C.2. The corresponding quality factor according to bandwidth definition results via

$$Q_{BW} = \frac{f_{res}}{\Delta f_{3dB}}. \tag{C.2}$$

How to obtain the corresponding resonance frequency and 3dB-bandwidth is exemplarily shown for the inductor without C_{sweep}.

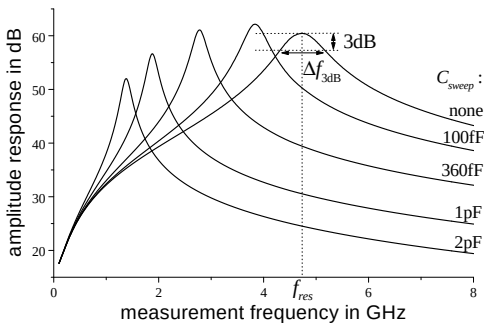

Figure C.2: Amplitude response of the inductor only and virtual parallel connections of the inductor and an ideal capacitance.

The resulting resonance frequencies and 3dB-bandwidths for swept capacitances are shown in Fig. C.3

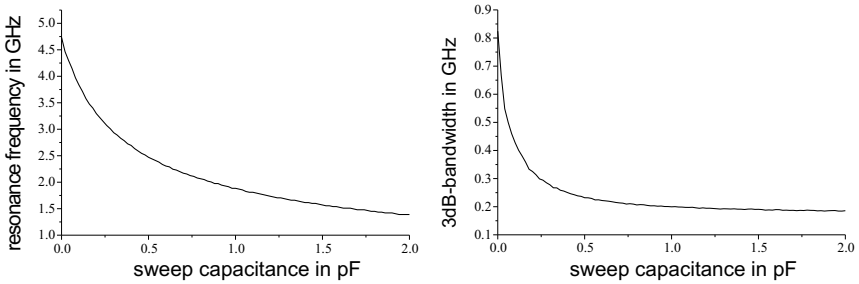

Figure C.3: Resonance frequencies and 3dB-bandwidths as result of swept parallel capacitance.

As expected the resonance frequency decreases with increasing sweep capacitance. Simultaneously the response function gets narrower. The resulting differential quality factor is depicted in Fig. C.4 vs. sweep capacitance (left) and as usual vs. resonance frequency (right).

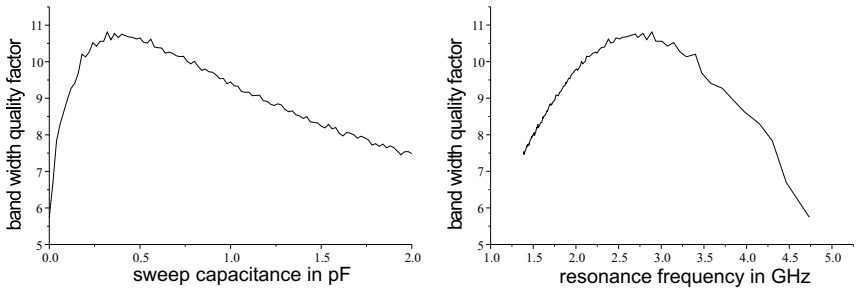

Figure C.4: Bandwidth quality factor as function of the sweep capacitance and as function of the resulting resonance frequency.

As comparison serves the following figure Fig. C.5 depicting the conventional quality factor $\frac{2\pi f L}{R}$ as function of the measurement frequency.

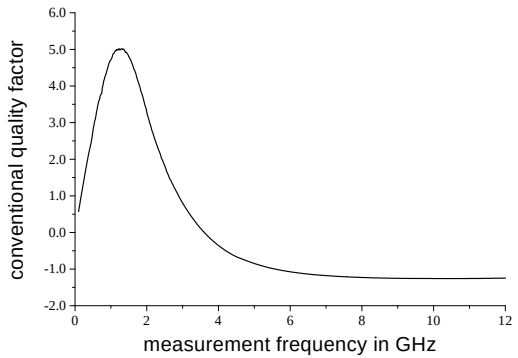

Figure C.5: Conventional quality factor.

It is clear that the potential of the inductor is predicted incorrectly and designs based on this quality factor may hardly turn out to perform as intended.

Appendix D

VHDL-AMS model of the proposed A-mode varactor

D.1 VHDL-AMS model

The following code describes the inner part of the varactor: the oxide capacitance, the variable capacitance and the variable resistance of the n^- well (C_v, $R_{w,1,2,3}$ in Fig. 6.2). These three elements are combined in a "black-box" with two nodes, called *varac_STI*, used in circuit simulation.

```
-- ********************************************************************
-- Function: model of varactor with STI spacer in multifinger layout
--
-- edited by J. Maget CPR HF
-- ********************************************************************


-----------------------------------------------------------------------
-- ENTITY definition
-----------------------------------------------------------------------
use work.electrical_pack.all; -- All names of package "electrical_pack" from
                              -- previous example

ENTITY varactor is
   generic (                -- data for MOS Varactor with STIs:
N1   :  real := 5e23 ;   -- doping under gate [1/m3]
```



```
N2   :  real := 3e23;      -- doping under STI [1/m3]
N3   :  real := 4e23;    -- doping under n+ [1/m3]
u1   :  real := 0.03 ;   -- mobility under gate [m2/Vs]
u2   :  real := 0.05 ;   -- mobility under STI [m2/Vs]
u3   :  real := 0.05 ;   -- mobility under n+ [m2/Vs]
l    :  real := 0.3e-6 ;   -- depth of STI [m]
l2   :  real := 0.5e-6 ;   -- width of STI [m]
l3   :  real := 0.1e-6 ;   -- depth of n+ to STI [m]
lg   :  real := 0.3e-6 ;   -- gate length [m]
wdiff:  real := 0.7e-6 ;   -- width of n+ diffusion [m]
tw   :  real := 2e-6 ;   -- well depth [m]
c1   :  real := 0.512 ;     -- eff. area par. under gate [1]
c2   :  real := 0.636 ;    -- eff. area par. under STI [1]
c3   :  real := 0.512 ;    -- eff. area par. under n+ [1]
lf   :  real := 0.8e-5 ;   -- finger length [m]
wf   :  real := 1.0e-6 ;  -- finger width [m]
NF   :  real := 120 ;    -- number of fingers [1]
q    :  real := 1.6e-19;    -- electron charge [C]
epsox:  real := 3.65;       -- rel. dielectric constant of gate oxide [1]
dox  :  real := 7e-9;    -- gate oxide thickness [m]
eps  :  real := 8.45e-12;  -- dielectric constant of vacuum [F/m]
epsi :  real := 11.9;      -- rel. dielectric const. of silicon [1]
dd   :  real := 0.05;      -- voltage param. for depletion cap. [V2]
da   :  real := 0.14;      -- voltage param. for accumulation cap [V2]
dr   :  real := 0.05;      -- voltage param. for resistance [V2]
Rsq  :  real := 6.0;     -- gate resistance per square [ohm/sq]
VFB  :  real := 1.2;       -- flatband voltage [V]
Rbypass:  real := 1e9);  -- Bypass resistance [Ohm]

port (terminal p, m: ELECTRICAL);
END varactor;


-----------------------------------------------------------------------
-- ARCHITECTURE definition
-----------------------------------------------------------------------
library ieee;                  -- Lib 'IEEE'
use ieee.math_real.exp;        -- Function exp()  of package "math_real"
use ieee.math_real.sqrt;       -- Function sqrt() of package "math_real"

ARCHITECTURE varac_STI of varactor is

--constants
constant A1 : real:=NF*lg*lf*c1;
constant A2 : real:=(tw-l)*NF*lf*c2;
constant A3 : real:=wdiff*NF*lf*c3;
constant A : real:=lg*lf*NF;
constant c : real:=(A**2)*eps*epsi*N1*q;
constant n : real:=epsi*A*N1*q*dox/epsox;
constant Cox: real:=eps*epsox*A/dox;
constant R2 : real:=l2/(q*N2*u2*A2);
constant R3 : real:=l3/(q*N3*u3*A3);
--constant Rgate:real:=(lf*gr)/(wf*NF*12);

-- branch quantities
quantity V_varac across
```

```
        I_varac through   p to m;

-- free quantities
quantity Q_Cv:    real;
quantity I_Cv:    real;
quantity V_Cv:    real;
-- quantity I_R:   real;
quantity wd:      real;
quantity lav:      real;
quantity R1:      real;
quantity Rv:      real;
quantity I_R:      real;

BEGIN

wd==-((epsi*dox)/epsox)+
    sqrt((epsi*eps*(sqrt((-V_Cv)**2+dr)-V_Cv)/(q*N1))+(dox*epsi/epsox)**2);
lav==0.5*((l-wd)+sqrt((l-wd)**2+(0.5*lg)**2));
R1==lav/(q*N1*u1*A1);
Rv==R1+0.5*(R2+R3);


V_varac  == V_Cv + VFB + Rv*I_Cv;
Q_Cv == 0.5*Cox*(sqrt(V_Cv**2+da)+V_Cv)+n-sqrt(c*(sqrt(V_Cv**2+dd)-V_Cv)+n**2);
I_Cv == Q_Cv'DOT;

I_R == V_varac/Rbypass;

I_varac  == I_Cv+I_R;

END varac_STI;
```

The node-list below shows how the inner varactor has to be accompanied by constant elements for full-value simulations. These constant elements are

- rp : parasitic resistance
- ls : serial inductance
- rg : gate resistance
- cp : parasitic capacitance.

```
* cxxxx
igate 0 g dc 0 ac 1
vg gdc 0 dc 0
lgatebias gdc g 10m
rp g 1 0.9
ls 1 2 110e-12
rg 2 3 25.8m
cp 3 w 380f
zvc 3 w z_varac_sti modlib='TEMP'
vw w 0 dc 0 ac 0
```


D.2 Parameter extraction

The runset below describes how the capacitance and resistance of the varactor can be extracted from an ac-analysis using the real and imaginary parts of the voltage at the gate (here for a frequency of 3.64GHz).

```
* cxxxx

.ac lin 3 3.63G 3.65G
.print type=(R I) ac v(*)

.measure ac real_vg value 're(v(g))' targ xvar=3.64e9
.measure ac cap value '-1.0/(2*3.14*3.64e9*im(v(g)))' targ xvar=3.64e9
.alter tune n=6
vw dc 0.0 2.5
.alter gate n=21
vg dc 0 2.5
.enda gate
.enda tune
```

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