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Ecole Doctorale des Sciences Physiques et de l'Ingenieur

et

Université de Modène et Reggio Émilie

Ecole Doctorale de l'Information et de la Technolgie de la Comunication cycle 24

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présentée par

Paolo LUCCHI

Pour obtenir le grade de

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Génération de fréquences pour applications millimétrique et satellite

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to Me...

"stay hungry, stay foolish"
Steve Jobs

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List of Symbols

Δf	Frequency range	(Hz)
ϵ_0	Permittivity of free space	($\mathrm{F\,m^{-1}}$)
ϵ_{ox}	Permittivity of silicon oxide	($\mathrm{F\,m^{-1}}$)
γ	White noise coefficient	
λ_0	Permeability of free space	($\mathrm{N/A^2}$)
$\mathcal{L}$	Phase Noise	(dBc/Hz)
ω_0	Central angular velocity	($\mathrm{rad\,s^{-1}}$)
B_W	PLL bandwidth	(Hz)
c	Light speed	($\mathrm{m\,s^{-1}}$)
C_V	Variable capacitance	(F)
C_{fix}	Fix capacitance	(F)
C_{ox}	Oxide capacitance	(F)
C_{Si}	Capacitance of the depletion layer under the gate	(F)
C_{Sub}	Substrate capacitance	(F)
f	Frequency	(Hz)
f_0	Oscillator central frequency	(Hz)
f_{max}	Maximum operation frequency	(Hz)
f_{min}	Minimum operation frequency	(Hz)
f_{OUT}	PLL Output frequency	(Hz)

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f_{REF}	PLL Reference frequency	(Hz)
g_m	Transconductance of MOS transistor	(S)
I_{DC}	Large-signal drain current of MOS transistor	(A)
I_{INJ}	Large-signal injected drain current of MOS transistor	(A)
k	Boltzmann's constant	($\mathrm{J\,K^{-1}}$)
L	Length of MOS transistor	(m)
M	Integer-N PLL division ratio	
$N/N+1$	Dual-modulus prescaler division ratio	
P_{DIS}	Power Dissipation	(W)
Q_C	Capacitances quality factor	
Q_L	Inductor quality factor	
Q_T	Total tank quality factor	
R_p	Parallel loss resistance	(Ω)
r_{ch}	Equivalent resistance of the channel underneath the oxide	(Ω)
r_g	Access resistance of the polysilicon gate	(Ω)
R_{pc}	Parallel capacitance resistance	(Ω)
R_{peq}	Equivalent parallel resistance of the circuits	(Ω)
R_{pl}	Parallel inductor resistance	(Ω)
$r_{s/d}$	Source/drain contact resistance	(Ω)
R_{sc}	Series capacitance resistance	(Ω)
R_{sl}	Series inductor resistance	(Ω)
T	Absolute temperature	(K)
T_S	PLL settling time	(s)
V_0	Output voltage at f_0 frequency	(V)
V_{DD}	Supply voltage	(V)
V_{GS}	Peak gate-to-source voltage	(V)
V_{out}	Output voltage	(V)

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V_{TH}	Threshold voltage of MOS transistor	(V)
V_{TUNE}	Tuning voltage	(V)
W	Width of MOS transistor	(m)
W_F	Width of a single finger in MOS transistor	(m)
Z_0	Characteristic impedance	(Ω)
Z_{out}	Output impedance	(Ω)

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Abstract

[EN] *The research activities presented in this thesis are related to the design of analog CMOS Radio Frequency Integrated Circuits. In particular the effort was focused on frequency synthesizers (Phase-Locked Loop) for transceiver. This work especially deals with critical blocks such as Voltage Controlled Oscillator (VCO) and Frequency Dividers.*
The first part of the thesis reports the design guidelines of a negative resistance LC-tank VCO and the design of a 15 GHz *Quadrature Voltage Controlled Oscillator. This represents the contributions to the realizations of a Phase-Locked Loop (PLL) realization in CMOS* 130 nm *technology for satellite applications in collaborations with the Polytech'Nice Sophia laboratory in France.*
The second part of this work reports the design contribution of a 60 GHz *Phase-Locked Loop in* 65 nm *CMOS technology for Wireless Personal Area Network (WPAN) applications in collaboration with the LAAS laboratory (Toulouse, France). In particular the design efforts were devote to the blocks working at millimeter Wave (mmW) frequency such as VCO and Frequency Divider (FD). Concerning the Frequency Dividers the Injection-Locked topology was selected for the sake of its high frequency and low power characteristics. In particular the prescaler is an Injection-Locked LC-tank Frequency Divider (ILLCFD) followed by an Injection-Locked Ring Oscillator Frequency Divider (ILROFD). For the VCO the negative resistance design approach has been employed. All cited circuits have been implemented and succesfully tested.*

[IT] *Il lavoro di ricerca presentato in questa tesi è incentrato sulla progettazione di circuiti integrati a radio frequenza in tecnologia CMOS. In particolare l'impegno e' stato focalizzato sui circuiti per la sintesi di frequenza (circuiti ad aggancio di fase) per ricetrasmettitori. L'attenzione è incentrata sulla progettazione dei blocchi più critici come oscillatori controllati in tensione (VCO) e divisori di frequenza.*
La prima parte della tesi presenta le linee guida per la progettazione di LC VCO a resistenza negativa e la progettazione di un oscillatore in quadratura controllato in tensione (QVCO) a 15 GHz. *Quest'ultimo rappresenta il contributo alla realizzazione di un sintetizzatore di frequenza a* 15 GHz *in tecnologia CMOS* 130 nm *per applicazioni satellitari*

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in collaborazione con il Politecnico di Nizza (Sophia Antipolis, Francia).
La seconda parte della tesi riporta il contributo alla realizzazione di un sintetizzatore di frequenza a 60 GHz *in tecnologia CMOS* 65 nm *in collaborazione con i laboratori LAAS (Tolosa, Francia) per reti senza fili ad alta velocità e corta distanza WPAN. In particolare la progettazione dei blocchi a onde millimetriche come l'oscillatore e i primi due blocchi della catena di divisione. Per quanto riguarda i divisori di frequenza sono state utilizzate due topologie Injection-Locked per la efficacia ad alte frequenze e il loro basso consumo. Il prescaler é stato realizzato con una topologia oscillatore a risonatore LC sincronizzato e il secondo blocco con oscillatore ad anello sincronizzato. Il VCO è stato realizzato a resistenza negativa. Tutti i circuiti sopracitati sono stato testasti con successo.*

[FR] *Cette thèse se concentre sur la conception de circuits intégrés radio fréquence en technologie CMOS. En particulier, l'effort est axé sur les circuits pour la synthèse de fréquence (boucles à verrouillage de phase) pour les émetteurs/récepteurs. L'attention se concentre sur la conception des blocs critiques comme les oscillateurs controlé en tension (VCO) et les diviseurs de fréquence.*
La première partie de la thèse présente des directives pour la conception de VCO à résonateur LC à résistance négative et la conception d'un oscillateur en quadrature controlé en tension (QVCO) à 15 GHz*. Ce dernier représente la contribution à la réalisation d'un synthétiseur de fréquence à* 15 GHz *en technologie CMOS* 130 nm *pour des applications satellites réalisé en collaboration avec Polytech'Nice (Sophia Antipolis, France).*
La deuxième partie de la thèse montre la contribution à la réalisation d'un synthétiseur de fréquence 60 GHz *en technologie CMOS* 65 nm*, en collaboration avec le laboratoire LAAS (Toulouse, France) pour les réseaux haut débit sans fil et à courte distance WPAN. Une attention particuliére a été portée sur la conception des blocs fonctionnant des lesbandes millimétriques tel que l'oscillateur et les deux premiers blocs de la chaine de division. En ce qui concerne les diviseurs de fréquence, deux topologies à injection ont été utilisées pour leur efficacité et leur basse consommation. Le prédiviseur a été concu avec une topologie oscillateur à résonateur LC synchronisé suivi d'un oscillateur en anneau synchronisé. Le VCO a une topologie à résistance négative. Tous les circuits ci-dessus ont été réalisés et testée avec succès.*

1 Introduction

The cut-off frequency increase achieved by the scaling of CMOS processes (e.g. f_T beyond 200 GHz for a 32 nm bulk process), combined with the relative low cost of these processes with respect to other ones, has led the CMOS to dominate the Integrated Circuits (ICs) market: as a result, monolithic CMOS transceivers have been realized targeting several different standards [1].

A building block diagram representing an example of a monolithic frequency division duplexing transceiver is depicted in Figure 1.1. The duplexer filter separates the transmitted frequency (f_{TX} in blue) and the received frequency (f_{RX} in red), allowing to use only one antenna for both the transmission and the reception. Even though frequency division duplexing transceivers suffer from multiple drawbacks (e.g. transmitter signal leakage into the receiver path, duplexer attenuation-quality factor trade-off, spectral leakage to adjacent channels in transmitter output) they are employed in many Radio Frequency (RF) systems (e.g. in cellular communications) because they isolate the receivers from the signal produced by transmitters [1].

The received signal, capted by the antenna, is passed to the receiver path through the duplexer filter: since its low amplitude, it first of all undergoes a low noise amplification, performed by the Low Noise Amplifier (LNA), then it is band-pass filtered and finally it undergoes a frequency down-conversion to baseband, performed by a mixer.

On the other side, the transmitted signal is first of all up-converted to the carrier frequency by a mixer, then is band-pass filtered and eventually it undergoes a power amplification, performed by the Power Amplifier (PA), to rise its power level before transmission. Finally, the duplexer filter pass the power amplified signal to the antenna for the transmission.

The tones used for the frequency up- and down-conversions, performed by the mixers, are produced by the frequency synthesizer. This is a system which receives a stable and low-noise input signal, called reference signal, and generates an output signal which is precisely locked in phase and frequency to a reference one. The main design challenge is to realize a low-voltage, low-power, low-cost monolithic synthesizer able to meet the constraints specified by the standard in terms of phase-noise, spurious tones, settling time, tuning range and resolution. A common implementation of a frequency synthesizer is

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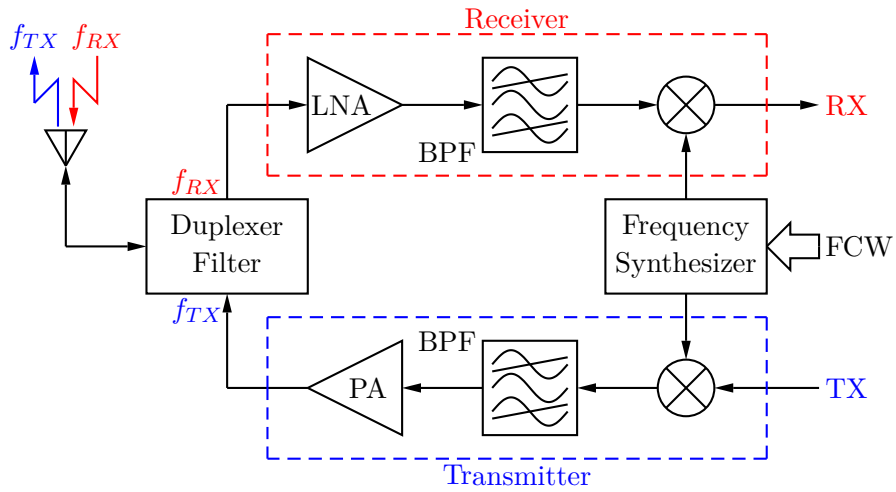

Figure 1.1: Frequency division duplexing transceiver block diagram.

based on a Phase-Locked Loop (PLL) (Figure 1.2), which can be both implemented in analog or digital form [2]. The relation between the reference and output signal frequencies is determined by the Frequency Control World (FCW) as depicted in Figure 1.2.

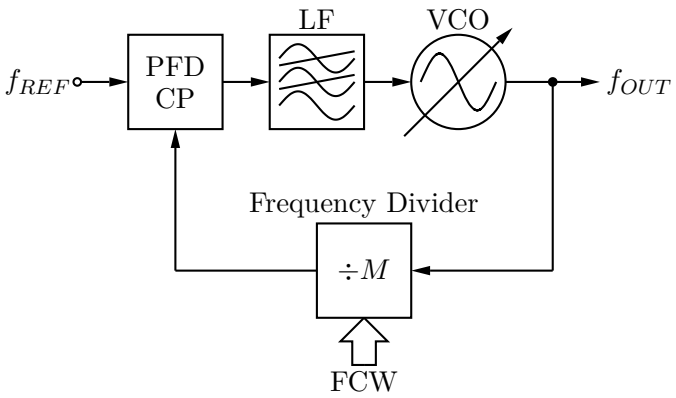

Figure 1.2: General block diagrams of a CPPLL.

The present Ph.D. thesis addresses the design of the Phase-Locked Loop building blocks working at high frequency, and epecially the Voltage Controlled Oscillator (VCO) and the Frequency Divider (FD). The interface matching between these two blocks is a critical point of every PLL. The central VCO frequency carrier must be around the minimum input power sensitivity of the first division chain block in order to transmit all VCO available power to the FD. The FD locking range must be larger than the VCO frequency tuning range in order to compensate eventually frequency shifts. This Ph.D. thesis addresses these topics in different bands and in different CMOS technologies.

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Chapter 2 concerns the design contribution to the realization of a 15 GHz PLL in 130 nm CMOS bulk process for Digital Video Broadcasting - Satellite (DVB-S) applications. The project has been developed in collaboration with the Polytech of NICE-SOPHIA ANTIPOLIS. My work was focused on the design of a 15 GHz Quadrature Voltage Controlled Oscillator (QVCO).

Chapter 3 mainly reports the contribution to the NANOCOMM ANR project whose aim is the realization of a low-cost, highly-integrated CMOS transmitter prototypes sending data up to 1 Gbps in a range up to 1 m to target 60 GHz Wireless Personal Area Network (WPAN) applications. The used technology was the CMOS bulk 65 nm by STMicroelectronics. The project was carried out in collaboration with LAAS-CNRS Laboratory of Toulouse. My work was focused on the design of the PLL blocks which work at millimeter wave frequency: in particular the design of the Voltage Controlled Oscillator (VCO) and the first two blocks of the division chain: divide-by-2 Injection-Locked LC-tank Frequency Divider (ILLCFD) and a divide-by-2 Injection-Locked Ring Oscillator Frequency Divider (ILROFD).

The first part of each chapter is devoted to some theory and applications related to the addressed topic.

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2

Ku band Oscillator

This chapter reports on the Ku band standard for Digital Video Broadcasting. The fundamental guideline for CMOS Oscillators and the Voltage Controlled Oscillators design are presented. A 15 GHz *QVCO has been designed in a* 130 nm *CMOS technology. The phase noise and voltage tuning range performances of the QVCO are compared with the literature.*

2.1 DVB-S2 standard

The DVB-S2 standard is the second-generation specification for satellite broadcasting - developed by the Digital Video Broadcasting (DVB) Project in 2003. It benefits from more recent developments in channel coding, Low Density Parity check Codes (LDPC), combined with a variety of modulation formats (QPSK, 8PSK, 16APSK and 32APSK). When used for interactive applications, such as Internet navigation, it may implement Adaptive Coding & Modulation (ACM), thus optimizing the transmission parameters for each individual user, dependant on path conditions. Backwards-compatible modes are available, allowing existing DVB-S set-top-boxes to continue working during any transitional period.

The DVB-S2 system has been designed for several satellite broadband applications:

- broadcast services for standard definition TV and HDTV;
- interactive services, including Internet access, for consumer applications;
- professional applications, such as Digital TV contribution and News Gathering, TV distribution to terrestrial VHF/UHF transmitters;
- data content distribution and Internet trunking.

It is based on a "tool-kit" approach which allows us to cover all the application areas while still keeping the single-chip decoder at reasonable complexity levels, thus enabling the use of mass market products also for professional applications.

The DVB-S2 standard has been specified around three key concepts:

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1. best transmission performance,
2. total flexibility,
3. reasonable receiver complexity.

To achieve the best performance complexity trade-off, quantifiable in about 30 % capacity gain over DVB-S, DVB-S2 benefits from more recent developments in channel coding and modulation. For interactive point-to-point applications such as IP unicasting, the adoption of the Adaptive Coding & Modulation (ACM) functionality allows to optimize the transmission parameters for each individual user on a frame-by-frame basis, dependant on path conditions, under closed-loop control via a return channel (terrestrial or by satellite): the result is an even greater gain of DVB-S2 over DVB-S.

DVB-S2 is so flexible that it can cope with any existing satellite transponder characteristics, with a large variety of spectrum efficiencies and associated Carrier-to-Noise ratio (C/N) requirements. Furthermore, it is not limited to MPEG-2 video and audio coding, but it is designed to handle a variety of advanced audiovideo formats which the DVB Project is currently defining. DVB-S2 accommodates any input stream format, including single or multiple MPEG Transport Streams, continuous bit-streams, IP as well as ATM packets.

2.1.1 Forward Error Correction (FEC) and modulation

Figure 2.1 shows the DVB-S2 detailed system block diagram [3]. The FEC is the key subsystem to achieve excellent performances by satellite, in the presence of high levels of noise and interference. The selection process, based on computer simulations, compares seven proposals - parallel or serially concatenated convolutional codes, product codes, low density parity check codes (LDPC) - all using "turbo" (i.e. recursive) decoding techniques. The winning system, based on Low Density Parity check Codes (LDPC), offeres the minimum distance from the Shannon limit on the linear AWGN channel, under the constraint of maximum decoder complexity of 14 mm^2 of silicon (0.13 µm technology). The selected LDPC codes use very large block lengths (64800 bits for applications not too critical for delays, and 16200 bits). Code rates of 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10 are available, depending on the selected modulation and the system requirements. Coding rates 1/4, 1/3 and 2/5 have been introduced to operate, in combination with QPSK, under exceptionally poor link conditions, where the signal level is below the noise level. Concatenated Bose-Chaudhuri-Hocquenghem (BCH) outer codes are introduced to avoid error floors at low Bit Error Rate (BER).

Four modulation modes can be selected for the transmitted payload (see Figure 2.2). QPSK and 8PSK are typically proposed for broadcast applications, since they are virtually constant envelope modulations and can be used in non-linear satellite transponders driven near saturation. The 16APSK and 32APSK modes, mainly targeted at professional applications, can also be used for broadcasting, but these require a higher level of available C/N and the adoption of advanced pre-distortion methods in the up-link station to minimize the effect of transponder non-linearity. Whilst these modes are not

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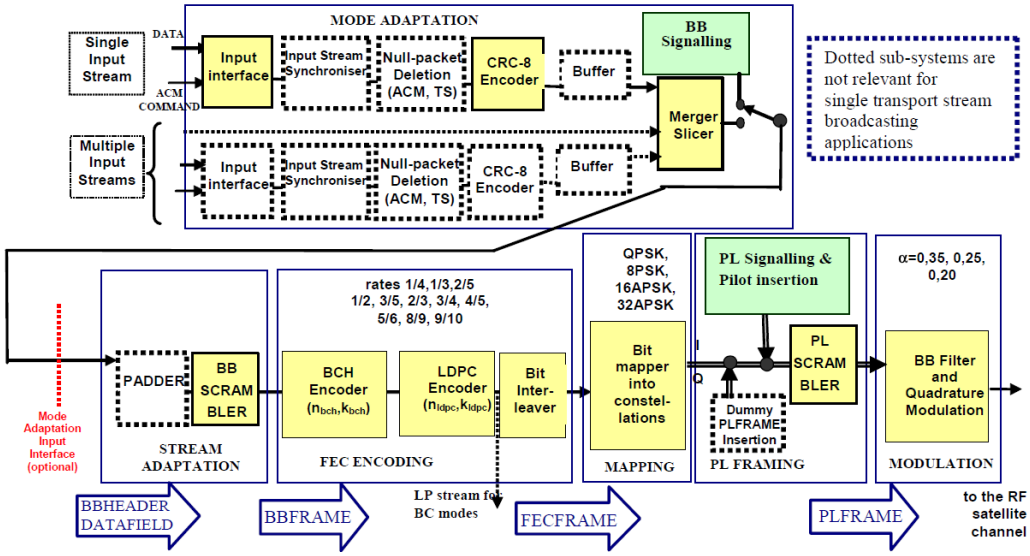

Figure 2.1: Functional block diagram of the DVB-S2 System characteristic.

as power-efficient as the other modes, the spectrum efficiency is much greater. The 16APSK and 32APSK constellations have been optimized to operate over a non-linear transponder by placing the points on circles. Nevertheless their performances on a linear channel are comparable with those of 16QAM and 32QAM respectively. By selecting the modulation constellation and code rates, spectrum efficiencies from 0.5 to 4.5 bits per symbol are available and can be chosen depending on the capabilities and restrictions of the satellite transponder used. DVB-S2 has three "roll-off factor" choices to determine spectrum shape: 0.35 as in DVB-S, 0.25 and 0.20 for tighter bandwidth restrictions.

Framing structure

Two levels of framing structures have been designed:

- the first at the physical level (PL), carrying few highly-protected signaling bits;
- the second at base-band level, carrying a variety of signaling bits, to allow maximum flexibility on the input signal adaptation.

The first level of framing structure has been designed to provide robust synchronization and signaling at the physical layer. Thus a receiver may synchronize (carrier and phase recovery, frame synchronization) and detect the modulation and coding parameters before demodulation and FEC decoding. With reference to Figure 2.3, the DVB-S2 physical layer signal is composed of a regular sequence of "lorries" (frames): within a lorry, the modulation and coding scheme is homogeneous, but may change (Adaptive Coding & Modulation) in adjacent lorries. Every frame is composed of a payload of 64800 bits (or

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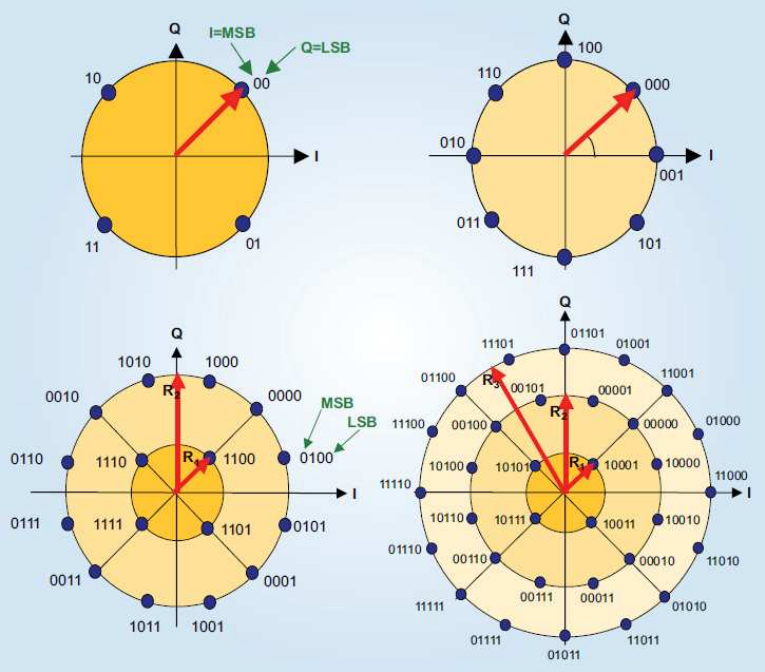

Figure 2.2: The four possible DVB-S2 constellations before physical layer scrambling.

16200 bits), corresponding to a code block of the concatenated LDPC/BCH FEC, and a Header (90 binary modulation symbols), containing synchronization and signaling informations. Since the PL Header is the first entity to be decoded by the receiver, it could not be protected by the powerful LDPC/BCH FEC scheme. On the other hand, it has

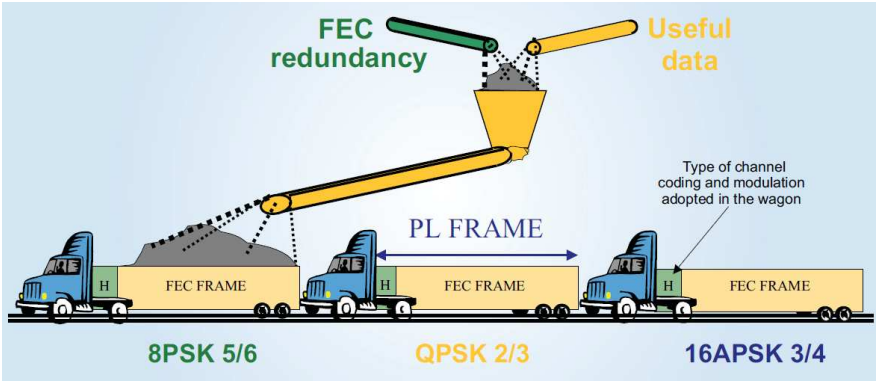

Figure 2.3: Pictorial representation of the physical-layer framing structure.

to be perfectly decodable under the worst-case link conditions. Therefore, the system designers selected a very low-rate 7/64 block code to protect it, suitable for soft-decision correlation decoding, and minimized the number of signaling bits to reduce decoding

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complexity and global efficiency loss.

The second level of framing structure, the "baseband frame", allows a more complete signaling functionality to configure the receiver according to the application scenarii: single or multiple input streams, generic or transport stream, Constant Coding & Modulation (CCM) or Adaptive Coding & Modulation (ACM), and many other configuration details. Thanks to the LDPC/BCH protection and the wide length of the FEC frame, the Base-Band (BB) Header may contain many signaling bits (80) without losing transmission efficiency or ruggedness against noise.

Backwards-compatible modes

The large number of DVB-S receivers already installed makes it very difficult for many established broadcasters to think of an abrupt change of technology in favour of DVB-S2 - especially where there is a receiver subsidy and for free-to-air public services. In such scenarii, backwards-compatibility may be required in the migration period, allowing legacy DVB-S receivers to continue operating, while providing additional capacity and services to new, advanced receivers. At the end of the migration process, when the complete receiver population has migrated to DVB-S2, the transmitted signal could be modified to the non-backward compatible mode, thus exploiting the full potential of DVB-S2.

Optional Backwards-Compatible (BC) modes have therefore been defined in DVB-S2, intended to send two Transport Streams on a single satellite channel. The first (High Priority, HP) stream is compatible with DVB-S receivers as well as with DVB-S2 receivers, while the second (Low Priority, LP) stream is compatible with DVB-S2 receivers only. Backwards compatibility can be implemented by hierarchical modulation, where the two HP and LP Transport Streams are synchronously combined at modulation symbol level on a non-uniform 8PSK constellation. The LP DVB-S2-compliant signal is BCH and LDPC encoded, with LDPC code rates 1/4, 1/3, 1/2 or 3/5. Then the hierarchical mapper generates the non-uniform 8PSK constellation: the two HP DVB-S bits define a QPSK constellation point, while the single bit from the DVB-S2 LDPC encoder sets an additional rotation before transmission. Since the resulting signal has a quasi-constant envelope, it can be transmitted on a single transponder driven near saturation.

System performance

Depending on the selected code rate and modulation constellation, the system can operate at carrier-to-noise ratios from $-2.4\,\mathrm{dB}$ (using QPSK 1/4) to $16\,\mathrm{dB}$ (using 32APSK 9/10), assuming an AWGN channel and ideal demodulator (see Figure 2.4). These results have been obtained by computer simulations for a Packet Error Rate of 10-7 (one erroneous Transport Stream Packet per transmission hour in a $5\,\mathrm{Mbit/s}$ video service). The distance from the Shannon limit ranges from $0.7\,\mathrm{dB}$ to $1.2\,\mathrm{dB}$. On AWGN, the result is typically a 20 - 35 percent capacity increase over DVB-S and DVB-DSNG under the same transmission conditions and 2 - $2.5\,\mathrm{dB}$ more robust reception for the same spectrum efficiency. The DVB-S2 system may be used in "single-carrier-per-transponder"

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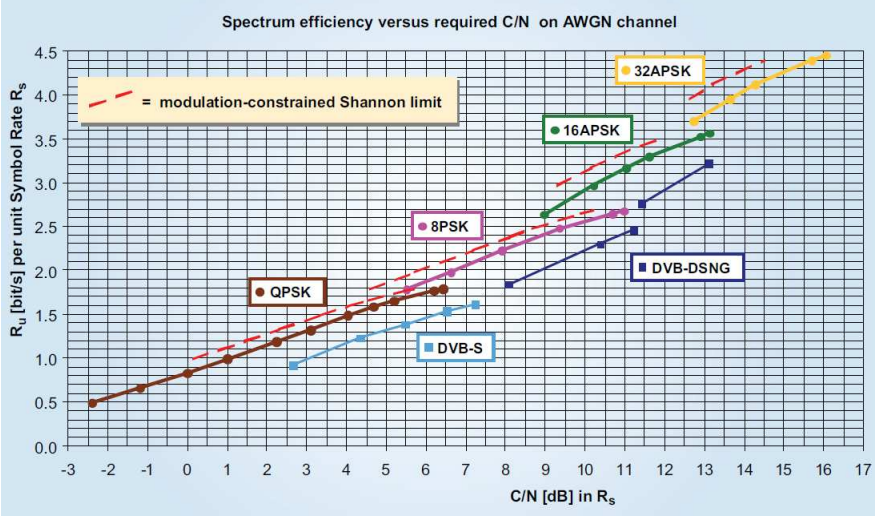

Figure 2.4: Required C/N versus spectrum efficiency on the AWGN channel.

or in "multi-carriers-per-transponder" (FDM) configurations. Figure 2.4 also indicates examples of the useful bitrate capacity R_U achievable by the system in the different modulation/coding configurations, assuming unit symbol rate R_S. The symbol rate R_S corresponds to the $-3\,\mathrm{dB}$ bandwidth of the modulated signal, while $R_S(1+\alpha)$ corresponds to the theoretical total signal bandwidth after the modulator, with representing the roll-off factor of the modulation. The use of the narrower roll-off $\alpha = 0.25$ and $\alpha = 0.20$ may allow a transmission capacity increase, but may also produce larger non-linear degradations by satellite for single-carrier operation.

When DVB-S2 is transmitted by satellite, quasi-constant envelope modulations such as QPSK and 8PSK are power efficient in the single-carrier-per-transponder configuration, since they can operate on transponders driven near saturation. 16APSK and 32APSK, which are inherently more sensitive to non-linear distortions and would require quasi-linear transponders (i.e., with larger Output Back- Off, OBO) may be improved in terms of power efficiency by using non-linear compensation techniques in the up-link station. In FDM configurations, where multiple carriers occupy the same transponder, this latter must be kept in the quasi-linear operating region (i.e., with large OBO) to avoid excessive inter-modulation interference between signals. In this case, the AWGN performance figures may be adopted for link budget computations.

Examples of possible uses of the system

Some examples may better clarify the functionalities and flexibility of DVB-S2. Starting from TV broadcasting using constant coding and modulation, and variable coding and modulation, some examples are given in the following to cover professional TV applications such as DSNG and DTT distribution to transmitters. For broadcasting services,

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only down-link parameters have been evaluated, for satellite EIRPs of 51 and 53.7 dBW at the service area contour. Conversely, for professional applications, link budget evaluations have been carried out for a typical Ku-band 36 MHz satellite with European-wide up-link and down-link coverage. Ideal target carrier-to-noise ratios are derived from Figure 2.4. The following link characteristics have been adopted:

- Up-link: ITU climatic zone L; frequency: 14.29 GHz; Atmospheric loss and rain attenuation for 99.9 % of average year (a.y.): 0.2 + 5.6 dB.
- Satellite: G/T(dB K^{-1}): 4.3; transmitted EIRP at saturation: 46.5 dBW.
- Down-link: ITU climatic zone K; frequency: 10.99 GHz; antenna efficiency: 60 %; coupling loss: 0.5 dB, pointing loss: 0.5 dB; LNB noise figure: 1.1 dB; Atmospheric loss and rain attenuation for 99.9 % a.y.: 0.1 + 2.4 dB.

2.1.2 Adaptive Coding and Modulation for one-to-one services

When DVB-S2 is used for interactive point-to-point applications like IP unicasting, its gain over DVB-S is even greater, if Adaptive Coding & Modulation (ACM) schemes are used. In fact ACM allows us to recover the so called "clear sky margin" (4 dB to 8 dB of power), typically wasted in conventional "constant coding and modulation" satellite links, thus doubling or even tripling the average satellite throughput and reducing dramatically the service cost. The ACM gain versus CCM increases for critical propagation conditions: therefore ACM is fundamental for the higher frequency bands (e.g. Ka band) and for tropical climatic zones. Figure 2.5 shows the scheme of an ACM satellite link, composed

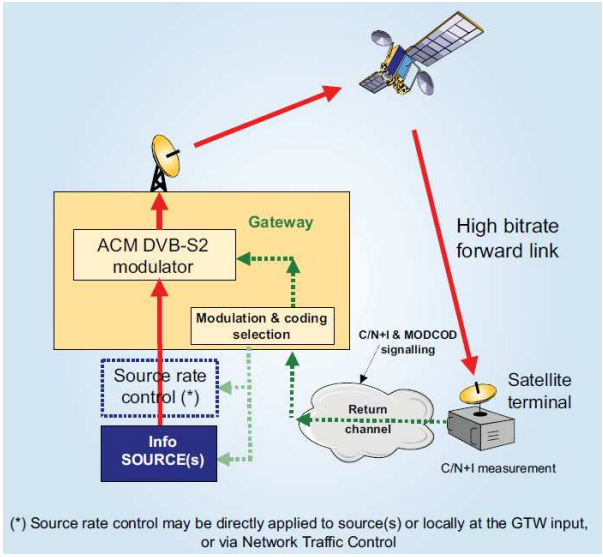

Figure 2.5: Block diagram of a DVB-S2 ACM link.

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of an ACM Gateway (GW), the DVB-S2 ACM modulator, the up-link station, the Satellite and the Satellite receiving Terminal (ST) connected to the ACM GW via a return channel. The DVB-S2 ACM modulator operates at constant symbol rate, since the available transponder bandwidth is assumed to be constant. ACM is implemented by the DVB-S2 modulator by transmitting a TDM sequence of frames, where coding and modulation format may change frame-by-frame. Therefore service continuity is achieved, during rain fades, by reducing user bits while increasing at the same time the FEC redundancy and/or modulation ruggedness.

Physical layer adaptation is achieved as follows:

- Each ST measures the channel status (available C/N+I) and reports it via the return channel to the Gateway (GW);
- The ST reports are taken into account by the GW while selecting the assigned protection level for data packets addressed to the ST;
- In order to avoid information overflow during fades, a user bitrate control mechanism should in principle be implemented, adapting the offered traffic to the available channel capacity. This can be implemented in various ways, according to the specific service requirements and network architecture. The GW imposes error protection, applied to a given portion of user data via suitable interfacing mechanisms. With respect to one-to-one services (e.g., DSNG), IP unicast links using DVB-S2 ACM must adapt the error protection on a user-per-user basis: the number of users may be very large (e.g. up to hundreds of thousands). Furthermore, direct source rate control may be impossible, since information sources (IP information providers) are far from the satellite GW.

A crucial issue in ACM systems is the physical layer adaptation loop delay, as it is strictly linked to the system capability of tracking channel variations. If loop adaptation is fast, service continuity may be guaranteed even during fast rain fades while, at the same time, keeping low C/N transmission margins to maximize the overall system throughput. Since maximum C/N+I variation rates at Ka band have been estimated to be of about 0.5 dB per second during heavy rain fades, and since the C/N distance between two adjacent DVB-S2 protection levels is around 1 dB, control loop delays smaller than 1 second should allow minimization of transmission packet losses.

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2.2 CMOS oscillator

Figure 2.6 shows a parallel ideal lossless LC tank. If the capacitor (or the inductor) is initially charged, when the switch closes the voltage across the resonator is sinusoidal with a constant amplitude (determined by the initial condition and by the L and C values).

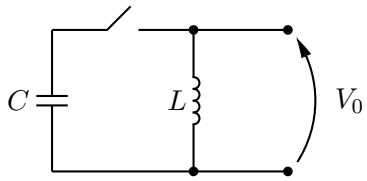


Figure 2.6: Ideal inductor capacitor resonator.

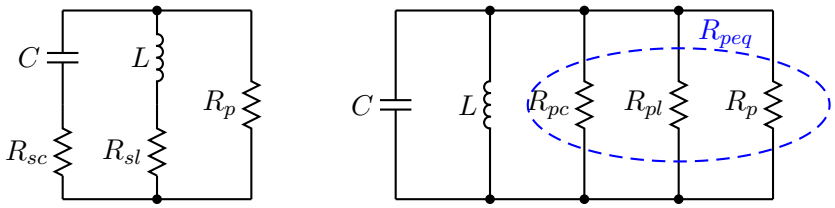
The frequency of the sinusoidal waveform is simply related to the tank parameters by the following equation:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

Under the hypothesis of lossless components, the inductor and capacitor continue to exchange the stored energy each other in the form of magnetic and electric field and the sinusoidal output voltage persists indefinitely. Obviously, the hypothesis of lossless component is not found in practice. Figure 2.7 shows a real case of LC resonant tank, including series losses for all components (R_{sl}, R_{sc}) and a parallel loss (R_p). The loss associated with the reactive components identifies the quality factors:

$$Q_L = \frac{\omega L}{R_{sl}} \tag{2.2}$$

$$Q_C = \frac{1}{\omega C R_{sc}} \tag{2.3}$$



(a) *series losses.* (b) *parallel losses.*

Figure 2.7: Tank series and parallel losses.

For sufficiently large Q_L and Q_C the tank can be represented (near the resonant frequency) by the circuit of Figure 2.7b with:

$$R_{pl} = Q_L \omega L \tag{2.4}$$

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$$R_{pc} = \frac{Q_C}{\omega C} \tag{2.5}$$

It is now useful to define the characteristic impedance Z_0 and the quality factor of the complete tank circuit Q_T as follows:

$$Z_0 = \sqrt{\frac{L}{C}} = \left(\frac{1}{\omega_0 C}\right) = \omega_0 L \tag{2.6}$$

$$R_{peq} = R_p // R_{pc} // R_{pl} \tag{2.7}$$

$$Q_T = \frac{R_{peq}}{Z_0} = \frac{R_{peq}}{\omega_0} = \omega_0 C R_{peq} \tag{2.8}$$

$$\left(\frac{1}{Q_T}\right) = \frac{Z_0}{R_p} + \left(\frac{1}{Q_L}\right) + \left(\frac{1}{Q_C}\right) \tag{2.9}$$

The total tank quality Q_T is dominated by the lowest quality factor component. Due to the presence of the tank losses (represented by R_{peq}) the oscillation vanishes, because part of the energy exchanged in each cycle from the inductor to the capacitor and viceversa is dissipated by R_{peq}. To get a real oscillator, a negative conductance must be added in parallel to the resonator to compensate the tank losses. Negative conductance (or resistance) can be obtained with active circuits providing energy to the LC resonator, at least equal to the energy dissipated by the tank losses in each cycle. The minimum needed negative conductance g_{m_c} must be at least equal to the total loss conductance ($\frac{1}{R_{peq}}$):

$$|g_{m_c}| \geq \frac{1}{R_{peq}} = \frac{1}{Q_T Z_0} \tag{2.10}$$

To guarantee oscillations start-up under Process-Voltage-Temperature (PVT) variations the negative conductance is designed with a factor 1.5 to 3 times larger than the required minimum. There are several circuits able to provide negative conductance (or resistance), leading to a wide variety of oscillator topologies [1][4]. Among them, the widely used circuit topology of a CMOS LC tank oscillator is depicted in Figure 2.8. It is commonly preferred for several reasons:

1. it requires a minimal number of active (and noisy) components, resulting low noise;
2. it requires a minimal number of passive components, and thus low silicon area;
3. it is very easy to insert variable capacitors to tune the output frequency;
4. it is a differential topology providing two anti-phase (180° shifted) output signals.

Differential circuit topologies are preferred, at radio frequency, due to the higher immunity to substrate and supply noise and, because differential circuits intrinsically remove even order distortions.

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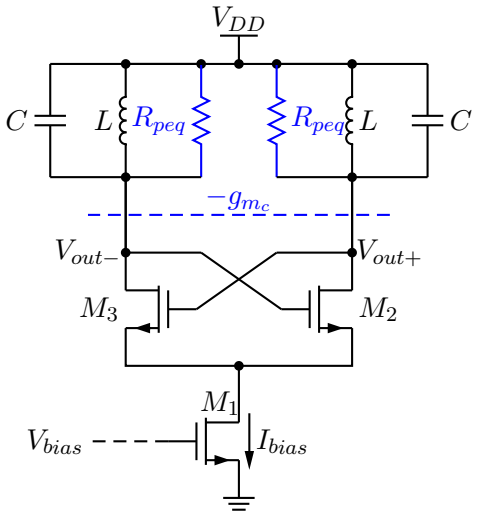

Figure 2.8: Circuit schematic of negative resistance LC CMOS Oscillator.

The differential resonator of the Figure 2.8 is composed by two LC tanks where the parallel losses are represented by R_{peq}. When the tail transistor is biased in saturation region the circuit gives the differential negative conductance to compensate the tank losses. The small signal differential conductance is given by: $g_{m_c} = -\frac{g_m}{2}$ where gm is the transconductance of the transistor $M_{2,3}$. To guarantee the oscillation start-up the following equation must be satisfied:

$$|g_{m_c}| = \frac{g_m}{2} \geq \frac{1}{2R_{peq}} \tag{2.11}$$

where $2R_{peq}$ is the total differential resistance seen across the two LC tanks. The transconductance of each cross coupled transistor must be higher than the corresponding LC tank loss [5].

2.2.1 Oscillation amplitude

In order to obtain a sinusoidal output voltage, the tank current must be a squarewave ranging from -$\frac{I_{bias}}{2}$ and $\frac{I_{bias}}{2}$; the tank filters higher order harmonics of this current and only its Fourier component at f_0 $\left(I_{f_0} = \frac{2I_{bias}}{\pi}\right)$ is covered into a differential voltage by the equivalent impedance at resonance $2R_{peq} = 2Q_T Z_0$. The zero-peak differential output voltage is then:

$$V_{out_{diff}} = \frac{4}{\pi} I_{bias} Z_0 Q_T = \frac{4}{\pi} I_{bias} \omega_0 L Q_T \tag{2.12}$$

We can observe the linear dependance between the oscillation amplitude and I_{bias}, Q_T, and Z_0. To save power and to achieve high spectral purity the total tank quality factor value should be maximized.

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Generally speaking the single ended output voltage (V_{out+} and V_{out-}) increases with the increasing bias current; his value must be smaller than V_{DD}. To increase the bias current, the transistor M_1 must be pushed in triode region, and the oscillator goes from a current limited operation to a voltage limited operation [6].
The output voltage saturates to a value close to two times the voltage supply V_{DD}. The bias current at which the oscillator saturates is $I_{bias_{sat}}$

$$V_{sat} = 2\alpha V_{DD} = \frac{4}{\pi} I_{bias_{sat}} Q_T Z_0 \tag{2.13}$$

Therefore:

$$I_{bias_{sat}} = \frac{\pi}{2} \frac{\alpha V_{DD}}{Q_T Z_0} = \frac{\alpha V_{DD}}{\omega_0 L Q_T} \tag{2.14}$$

with $\alpha < 1$ [5].

2.2.2 Phase noise minimization

To arrive at the guidelines for the optimum design, we use the Leeson's formula for the white phase noise $\mathcal{L}_w(\Delta\omega)$ at an offset frequency ($\Delta\omega$) from an ω_0 carrier

$$\mathcal{L}_w(\Delta\omega) = kTR_{peq} \frac{F}{V_0^2} \left(\frac{\omega_0}{Q_T \Delta\omega} \right) \tag{2.15}$$

where k is the Boltzmann's constant, T is the absolute temperature, R_{peq} is the equivalent tank parallel resistance, V_0 is the peak oscillation amplitude, Q_T is the tank quality factor. F, the noise factor, is given by [7]

$$F = 2 + \frac{8\gamma R_{peq} I_{bias}}{\pi V_0} + \gamma \frac{8}{9} g_{m_{bias}} R_{peq} \tag{2.16}$$

where γ is the device white noise coefficient and g_{mbias} is the current source transconductance. The typical Figure Of Merit (FOM) of an oscillator compares the phase noise $\mathcal{L}$, measured at a given offset frequency ($\Delta\omega$) from the carrier frequency f_0 normalized to the oscillation frequency, the frequency offset and the power consumption:

$$\text{FOM} = \mathcal{L}(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left(\frac{P_{DIS}}{1\,\text{mW}}\right) \tag{2.17}$$

where $\Delta\omega = 2\pi\Delta f$ and P_{DIS} is the dissipated power. The FOM allows therefore for an homogeneous comparison between oscillators designed for different operation frequencies and dissipated powers. As previously seen, at low bias current, while the amplitude of oscillation is smaller than the power supply, the differential pair acts as a simple current switch driving the resonators and V_{out} is expressed by Eq: 2.12. For higher currents the output voltage saturates close to two times the supply voltage. Neglecting the noise of the biasing transistor we can obtain:

$$\mathcal{L}(\Delta\omega) = \begin{cases} (2+2\gamma) \frac{\pi^2 kT}{16\omega_0 L Q_T I_{bias}^2} \left(\frac{\omega_0^2}{Q_T \Delta\omega} \right)^2 & \textit{current limited} \\ \left(2 + \frac{4\gamma\omega_0 L Q_T I_{bias}}{\pi\alpha V_{DD}} \right) \frac{kT\omega_0 L Q_T}{4(\alpha V_{DD})^2} \left(\frac{\omega_0^2}{Q_T \Delta\omega} \right)^2 & \textit{voltage limited} \end{cases} \tag{2.18}$$

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Eq: 2.18 shows that the phase noise decreases with I_{bias} in the current limited region and increases in the voltage limited region. Therefore, minimum phase noise is achieved at the transition of the two regions [8], when $V_{out} = V_{sat} = 2\alpha V_{DD}$ (Eq: 2.13); the optimum bias current is given by Eq: 2.14. Substituting Eq: 2.14 in Eq: 2.18 provides:

$$\mathcal{L}_{min}(\Delta\omega) = (2 + 2\gamma)\,\frac{kT\omega_0 L Q_T}{4\,(\alpha V_{DD})^2}\left(\frac{\omega_0^2}{Q_T \Delta\omega}\right)^2 \tag{2.19}$$

For a given technology, V_{DD} and γ are fixed. The tank quality factor Q_T can be maximize by an optimum choise of inductor and varactor. To reduce the minimum achievable phase noise of an oscillator, the inductor should be reduced, and the current consumption equally increased (in according with Eq: 2.14) to fall in to the optimum region of operation [5].

2.2.3 CMOS Voltage Controlled Oscillator

Figure 2.9 shows the schematic of a CMOS Voltage Controlled Oscillator. The variable capacitors (C_V), realized with a MOS transistors, are connected in parallel with the inductor. The gate terminals of the varactor are connected to the tank and the drain/source terminals are connected together in a common node. This node acts as a virtual ground for a differential signal. The tuning voltage is applied at the drain/source terminal.

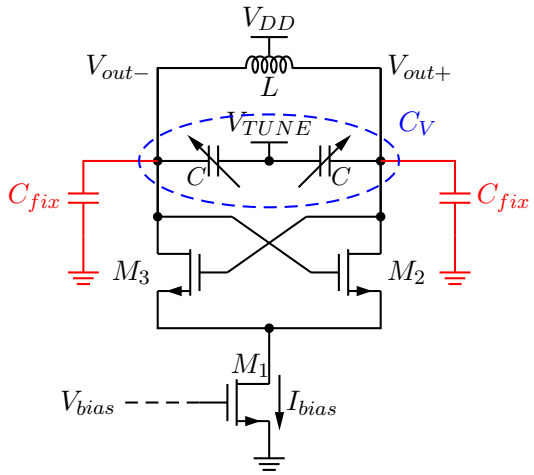

Figure 2.9: Schematic diagram of a CMOS Voltage Controlled Oscillator

Fixed capacitors (C_{fix}) represent the parasitic capacitance of interconnects, inductors, and transistors. The tuning range of a VCO is define as:

$$\mathrm{TR} = \frac{\Delta f}{f_0} = 2\frac{f_{max} - f_{min}}{f_{max} + f_{min}} \tag{2.20}$$

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Combining Eq: 2.1 and Eq: 2.20 leads to the relationship between the tank capacitance change and the oscillator tuning range:

$$\frac{\Delta f}{f_0} \approx \frac{1}{2}\frac{\Delta C}{C} \tag{2.21}$$

where $\Delta C = C_{var_{max}} - C_{var_{min}}$ is capacitance variation and C is the average tank capacitance composed by the varactor capacitance (C_V) itself and the parasitic fixed capacitance (C_{fix}). The second term of Eq: 2.21 can be rewritten as follows:

$$\frac{1}{2}\frac{\Delta C}{C} = \frac{1}{2}\frac{\Delta C}{C_V}\frac{1}{1+\frac{C_{fix}}{C_V}} \tag{2.22}$$

To increase the tuning range, the effect of the parasitic fixed capacitance C_{fix} must be negligible. This goal can be achieved by reducing as much as possible the parasitic capacitance and/or by using larger value of varactor capacitance. Therefore the inductance value must be reduced in according with Eq: 2.1 to keep constant the central oscillation frequency. As a consequence, the tank characteristic impedance Z_0 decreases and the bias current needed to keep constant the output voltage swing increases according to Eq: 2.12.
Usually in a CMOS circuit, the varactors are building using MOSFET transistors. Since the varactor gates are directly connected to a DC voltage equal to voltage supply (V_{DD}), the tuning voltage can range from 0 V to V_{DD}. In addition, it is worth noticing that the VCO of Figure 2.9 features a high sensitivity of the output frequency to changes in the supply voltage, leading to a poor power supply noise rejection. In fact, since the varactor gates are DC connected to the supply, supply voltage noise change provides the same effect on the output frequency as a tuning voltage change.
To minimize this issue, several alternative topologies of CMOS Voltage Controlled Oscillator isolating the voltage across the LC tank from the supply voltage have been presented. Some examples are depicted in Figure 2.10.

For any VCO, the dependance of the output signal on the tuning voltage is described by the following expression:

$$V_{out} = V_0 \cos\left[2\pi\left(f_0 + K_{\mathrm{VCO}}\int_{-\infty}^{t} V_{TUNE}\,dt\right)\right] \tag{2.23}$$

where K_{VCO} is the VCO gain. In case of linear relationship between the tuning voltage and the output frequency, K_{VCO} is expressed by:

$$K_{\mathrm{VCO}} = \frac{f_{max} - f_{min}}{V_{TUNE_{max}} - V_{TUNE_{min}}} \tag{2.24}$$

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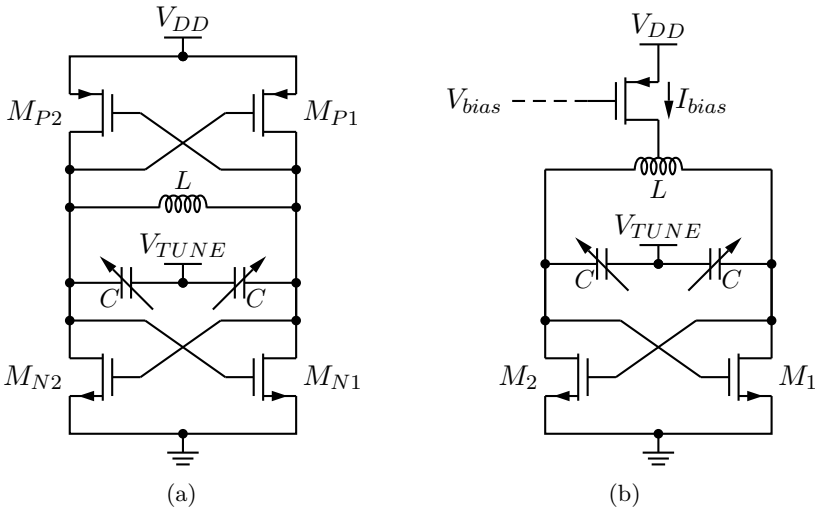

Figure 2.10: VCO which isolates the voltage across the LC tank from the V_{DD}.

A larger VCO gain is rarely preferred. This is because a noise voltage present at the tuning port of the oscillator results in a frequency modulation of the carrier and thus in phase noise. It is intuitive that a larger tuning gain gives a larger sensitivity to noise sources. If we assume a resistor R at the tuning port, for example the output resistance of the tuning source, it is possible to show that a voltage noise results in a phase noise magnitude given by [9]:

$$\mathcal{L}(\Delta\omega) = 2kTR\left(\frac{2\pi K_{\mathrm{VCO}}}{\Delta\omega}\right)^2 \tag{2.25}$$

In addition to the case of a simple oscillator, the International Technology Roadmap for Semiconductor (ITRS) FOM of a VCO takes into account also the tuning range [9, 5]:

$$\mathrm{FOM}_T = \mathcal{L}(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\frac{\mathrm{TR}}{10}\right) + 10\log\left(\frac{P_{DIS}}{1\,\mathrm{mW}}\right) \tag{2.26}$$

2.3 Quadrature Voltage Controlled Oscillator

This section provides insight on the main limitations of conventional techniques for quadrature signals generation [5]:

1. RC-CR networks lead to high power consumption when high phase accuracy or large tuning bandwidth are required.

2. Digital frequency dividers do not ensure high phase accuracy and are not suited to drive large capacitive loads. In both cases typical power consumptions are well above the tens of mW.

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3. Ring Oscillator (RO) fulfills this requirement, but the notorious low spectral purity (or better, the low phase noise FOM) of ring oscillators disqualifies this choice for most applications in modern radio transceivers.

A more attractive approach to direct quadrature synthesis relies on the possibility of coupling two symmetric LC-tank VCOs to each other, thereby exploiting the good phase noise performance of LC-oscillators.

In the present section a LC Quadrature Voltage Controlled Oscillator (QVCO) in 130 nm CMOS technology is investigated having in mind the idea of replacing the traditional superheterodyne architecture of the DVB-S receiver with a direct conversion architecture where the Low Noise Block (LNB) receives the composite signal from the satellite and provides at the output in one single step the I and Q bit stream at the base band. The QVCO is usually the preferred solution to generate in-quadrature signals with respect to poly-phase filters, ring oscillators, or frequency dividers.
In particular, the central frequency was fixed at 15 GHz, to evaluate the technology capabilities not only for the ground receiver (e.g. in the Digital Video Broadcasting - Satellite (DVB-S) the down-link frequency band is 10.7- 12.75GHz) but also for the on satellite receiver (e.g. in the DVB-S the up-link frequency band is 12.9-18.4GHz).

2.3.1 Circuit design

Figure 2.11 depicts the schematic of the fully differential designed QVCO. The circuit was biased without current mirror for sake of phase noise minimization. In addition the lack of a current mirror allows to reduce the power consumption and to avoid the introduction of an automatic amplitude control circuit. To fix the output voltage swing

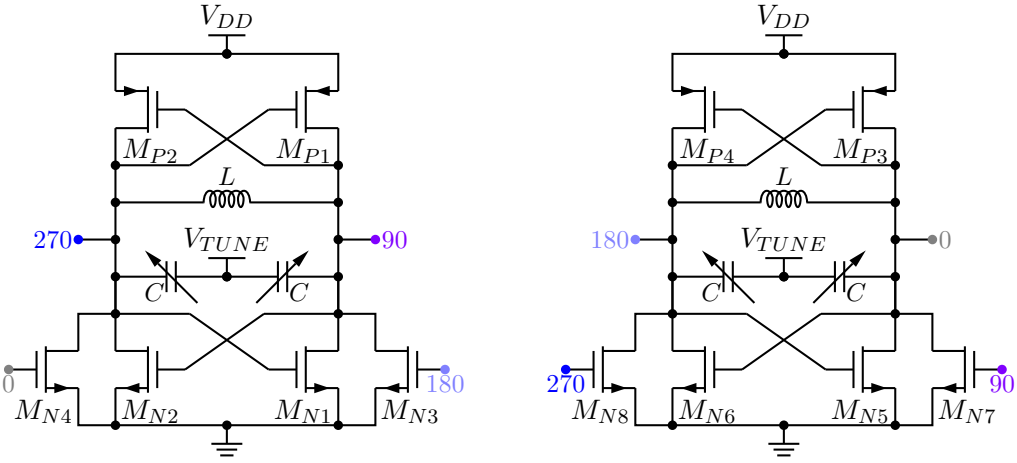

Figure 2.11: QVCO schematic.

between current limited and voltage limited region the circuit requires a loop gain higher

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than 3:

$$|g_{m_c}| = \frac{g_{m_p} + g_{m_n}}{2} = \frac{1}{R_{peq}} \geq 3 \tag{2.27}$$

$$\left(\frac{W}{L}\right)_p = \left(\frac{56\,\mu\text{m}}{130\,\text{nm}}\right)_p \tag{2.28}$$

$$\left(\frac{W}{L}\right)_n = \left(\frac{10\,\mu\text{m}}{130\,\text{nm}}\right)_n \tag{2.29}$$

Eq: 2.28 and 2.29 fix the transistors size, and as a consequence the bias current to 4.5 mA for each VCO. The cross-coupled transistors have been designed with a minimum length to get a maximum transconductance. The inductor resonates directly with the parasitic capacitances of the transistors. The transistors have been laid out multifinger and with a double gate access, in order to reduce as much as possible the parasitic access resistance. The accumulation varactors are connected with the drain of the transistors and DC voltage close to 600 mV. Therefore the DC voltage of varactors is not directly sensible to the voltage supply variations. Figure 2.12 shows the equivalent small signal model which can be used to evaluate the quality factor of an accumulation MOS varactor and to arrive at the optimum varactor design. C_{sub} and r_{sub} are the parasitic capacitance

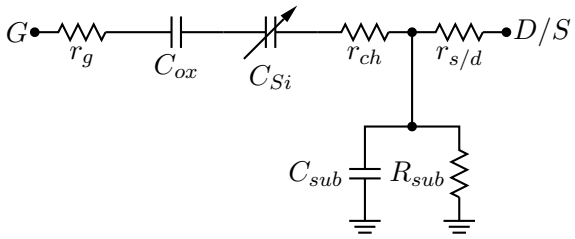

Figure 2.12: Small signal equivalent lumped model of an Accumulation MOS varactor

and resistance of the reverse biased P-N junction of the N-well and P-type substrate. If source and drain are tied to ground, the substrate parasitics are shorted and can be neglected. r_g, r_{ch} and $r_{s/d}$ are respectively the access resistances of the polysilicon gate, the equivalent resistance of the channel underneath the oxide and the source/drain contact resistance. Eq: 2.3 approximates the quality factor of the varactor as:

$$Q_C = \frac{1}{\omega C_V (r_g + r_{ch} + r_{s/d})} \tag{2.30}$$

where $C_V = C_0 W L$

$$C_0 = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{Si}}} \tag{2.31}$$

in which C_{ox} and C_{Si} are, respectively, the oxide capacitance and the capacitance of the depletion layer under the gate, per unit area. By applying a positive voltage between the gate and the N-well the surface is accumulated and the device capacitance equals the oxide capacitance. If the applied voltage is reversed, the surface layer is depleted and

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the series capacitance decreases. The maximum capacitance, per unit area, of the device corresponds to a heavily accumulated surface and equals $C_{ox} = \frac{\epsilon}{t_{ox}}$. On the other side, a minimum value (C_{dmin}) is reached when the voltage difference between the electrodes equals the threshold voltage. Beyond this point, an inversion layer is formed under the gate. N-type source/drain diffusions can not provide the holes required to invert the surface layer transistor which are then thermally generated. At low frequency this effect brings the value of the capacitance close to the oxide one. At high frequency, where the varactor is assumed to operate, this effect is not seen and the capacitance remains at its minimum value.

The quality factor is thus almost roughly independent of the varactor width. To optimize the quality factor, the series resistances must be minimized with multifinger layouts. On the other hand, increasing the number of fingers rises the fixed parasitic capacitance of interconnects, reducing the tuning capability of the varactor. The gate and channel resistances behave in a different way changing the gate length L_g. The quality factor can be expressed with Eq: 2.3 and Eq: 2.30. The varactor capacitance increases linearly with the MOS width, while all the parasitic resistances reduce linearly. Figure 2.13 shows the simulated capacitance at 15 GHz frequency versus the gate-source

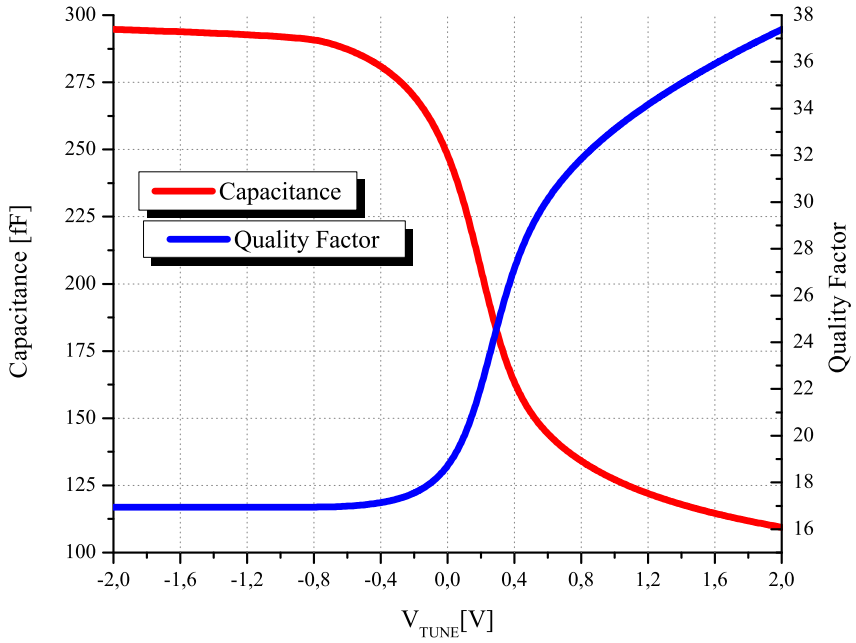

Figure 2.13: QVCO varactor C-V characteristic

voltage for the chosen 300 fF MOS varactor designed with a minimum possible length of 0.35 µm and multifinger (20) [10]. Changing the gate voltage from −2 V to 2 V, with the source and drain contacts connected to ground, the capacitance ranges from 109.4 fF to 294.7 fF. Figure 2.14 shows the quality factor and the $\frac{C_{max}}{C_{min}}$ characteristics versus

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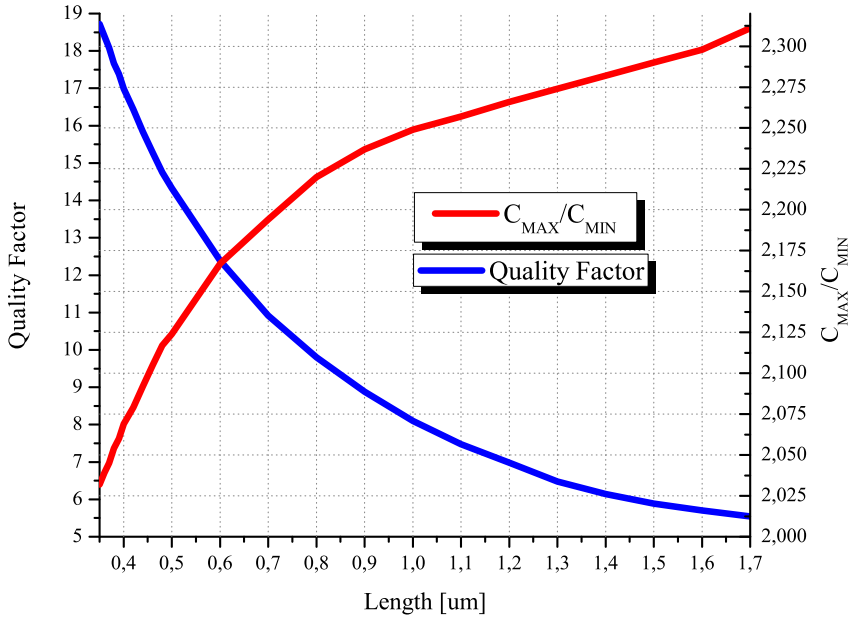

Figure 2.14: QVCO varactor $\frac{C_{max}}{C_{min}}$ characteristic

the varactors length. For high quality factor the minimum length is needed; as a consequence the tuning range decreases. We can observe in Eq: 2.2 and Eq: 2.3 that for frequencies higher than 10 GHz, Q_L increases with the frequency while Q_C decreases. For this reason, a carefully varactor design is very important to get a good tank quality factor.

The total fixed capacitance accounting for inductor, two cross-coupled pair and buffer plus minimum varactor capacitance is 61.5 fF. In order to set the center frequency around 15 GHz, a 290 pH octagonal one turn coil inductance has been selected. A compact model as that described in [6] (Figure: 2.15a) was extracted from electromagnetic simulations carried out both with the 2D $\frac{1}{2}$ electromagnetic simulator Momentum by Agilent Technologies and with the 3D electromagnetic simulator by CST. The inductor exhibits an inductance of about 290 pH and a maximum quality factor in the range of 27 (Figure: 2.15b). It is worth pointing out that these values of inductance and quality factor are very close to those claimed in [11] for a 65 nm CMOS LC VCO working in the Ku-band. The parallel between the inductor quality factor and the minimum varactor quality factor (Eq: 2.9) gives a value close to 11 for the total tank quality factor.

For sake of good locking capability and flicker noise minimization, the coupling N-channel transistors width was fixed equal to:

$$\left(\frac{W}{L}\right)_{3,4,7,8} = \left(\frac{16\,\mu m}{0.3\,\mu m}\right)_{3,4,7,8} \tag{2.32}$$

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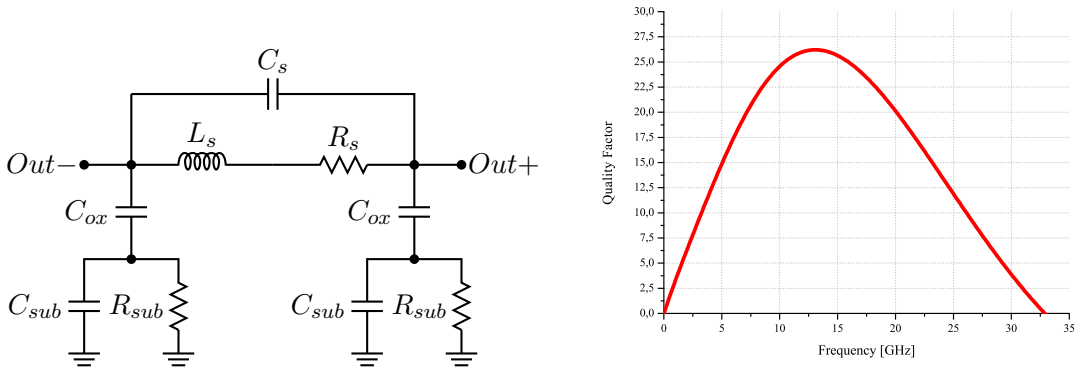

(a) *lumped model* (b) *quality factor*

Figure 2.15: VCO Inductor quality factor and lumped model.

2.3.2 Measurements results

Figure: 2.16 shows the microphotograph of the fabricated prototype. In the middle of the chip are visible the two inductors of the VCO core. In the microphotograph are also visible the two buffers to drive the load of the instruments. Under an experimental point of view, the use of buffers is mandatory, in order to perform reliable measurements. Without buffers, the losses of the external load connected to the circuit during the characterization can degraded the VCO performances or, on the other hand, high-Q lines connected to the pads via the coplanar probes and coaxial cables can improve the VCO performances. The GSGSG pads for the differential in-phase (I+, I-) and in

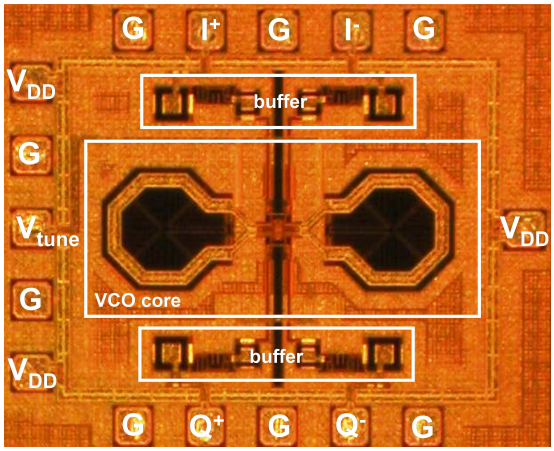

Figure 2.16: QVCO microphotograph.

quadrature (Q+, Q-) RF output signals are visible on the top and on the bottom of the chip, respectively. At the left side the GSG pad for the tuning voltage (V_{TUNE}) is

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visible. Eventually, three pads for the supply (V_{DD}) are distributed along the pad-ring. The chip size is $900 \cdot 1100\,\mu m^2$, pads enclosed. The differential output signals were made available to the single-ended input of the Agilent E4408B spectrum analyzer using a wideband Anaren 30070 hybrid. Figure: 2.17 reports the dependence of the output

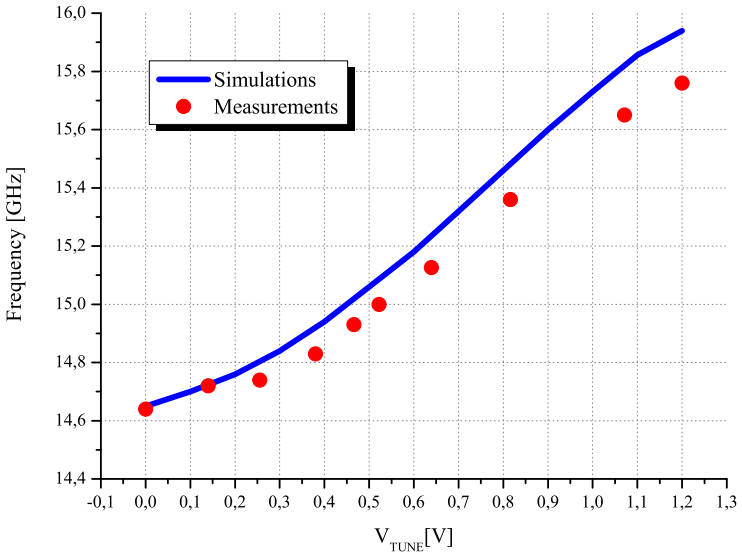

Figure 2.17: Comparison between measured and simulated tuning range.

frequency on the tuning voltage. A difference less than 1.3 % between simulations and measurements was obtained on the whole tuning range. The carrier frequency (f_0) goes from 14.6 GHz to 15.8 GHz for V_{TUNE} ranging between 0 V and 11.2 V corresponding to a tuning range of 7.4 %. The QVCO delivers about −20 dBm on a 50 Ω load and it sinks 9.4 mA from a 1.2 V supply. Phase noise measurements were carried out using an Agilent E5500 phase noise meter. Figure 2.18 shows the measured phase noise for f_0=14.6 GHz. The QVCO exhibits a phase noise of −106 dBc/Hz at the offset frequency (Δf) of 1 MHz, and −129.5 dBc/Hz at the offset frequency (Δf) of 10 MHz. This value is very close to the −107 dBc/Hz at the offset frequency (Δf) 1 MHz recently claimed for the VCO used in the PLL of a monolithic Ku-band receiver [12]. For other values of applied V_{TUNE} the phase noise did not change in agreement with simulations.

The performance of the fabricated QVCO has been compared with other 130 nm CMOS VCO reported in the literature through FOM in Eq: 2.17 and the FOM_T in the Eq: 2.26.

The FOM are −178.56 dBc/Hz at the offset frequency of 1 MHz and −182.28 dBc/Hz at the offset frequency of 10 MHz.

The FOM_T are −175.91 dBc/Hz at the offset frequency of 1 MHz and −179.63 dBc/Hz at the offset frequency of 10 MHz. The FOM_T is worse then FOM because of the tuning range. Table 2.1 and Figure 2.19 compare the designed QVCO with the state of the art

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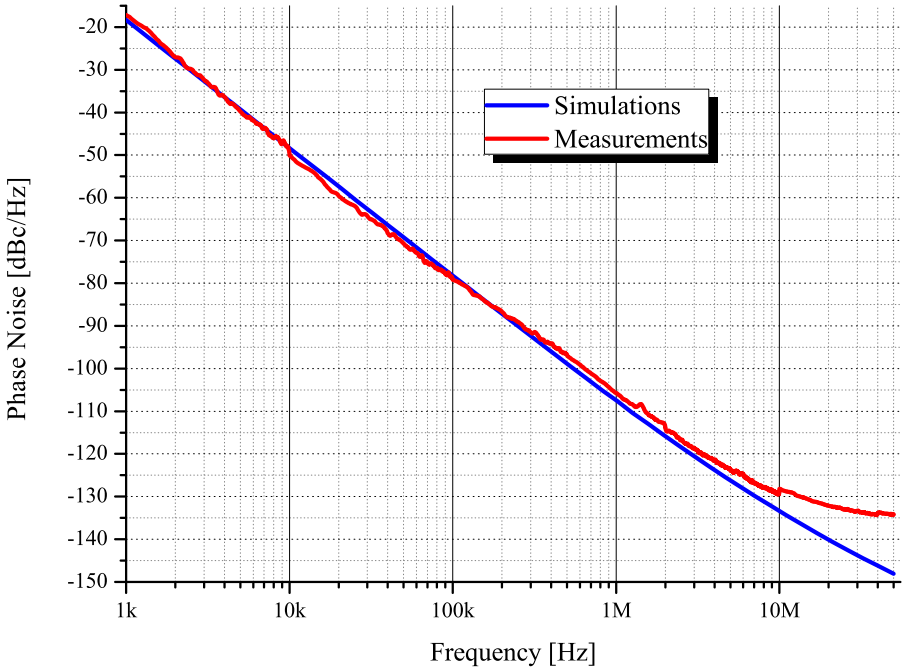

Figure 2.18: Comparison between measured and simulated phase noise.

of VCO designed in 0.13 µm CMOS technology.

Table 2.1: VCO CMOS 0.13 µm state of art.

Ref	Tech. [µm]	Freq. [GHz]	TR [%]	Voltage [V]	P_{DISS} [mW]	$\mathcal{L}$ @ 1 MHz [dBc/Hz]	FOM [dBc/Hz]	FOM_T [dBc/Hz]
[13]	0.13	4.91	15	0.8	3.2	−112	−180.8	−184.3
[14]	0.13	5	20	1.2	5.28	−117	−183.8	−189.8
[15]	0.13	5.1	5.26	1.2	3.7	−118	−186.7	−181.1
[16]	0.13	11.2	n.a.	0.8	4.8	−106	−180.2	n.a.
[17]	0.13	20	10.2	n.a.	32	−102	−173.4	−174.6
[18]	0.13	20	12	n.a.	20	−101	−174.0	−175.6
[19]	0.13	26	3.1	1.35	24	−96	−170.5	−160.3
THIS	0.13	14.6	7.4	1.2	11	−106	−178.6	−175.9

In conclusion, a 130 nm CMOS QVCO exhibiting a central frequency of 15 GHz has been demonstrated. The phase-noise-related FOM is well aligned with other 130 nm CMOS VCOs reported in the literature. In particular, the comparison with other CMOS VCOs claimed in the literature for Ku-band satellite receiver, with the DVB-S standard,

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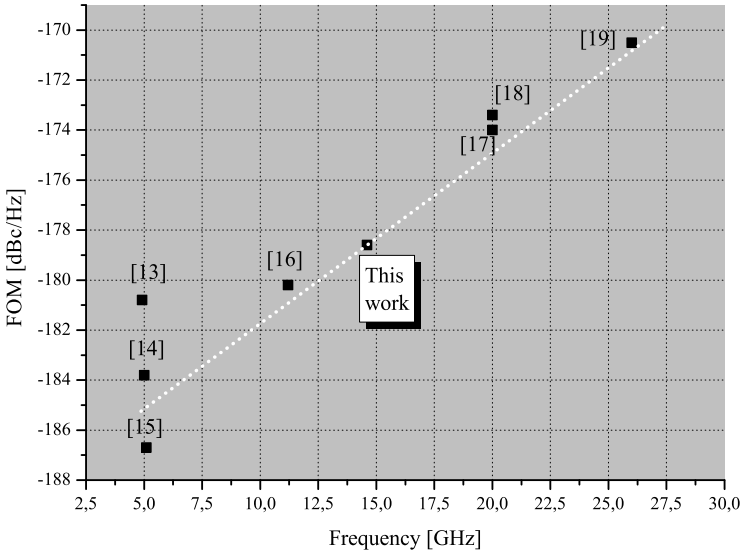

Figure 2.19: VCO CMOS 0.13 µm state of the art.

and with commercial products implemented in SiGe BiCMOS technologies suggests that the 130 nm CMOS technology can be evaluated with interest for the design of a DVB-S satellite receiver front-end. Since the VCO has to be employed in a PLL, the measured

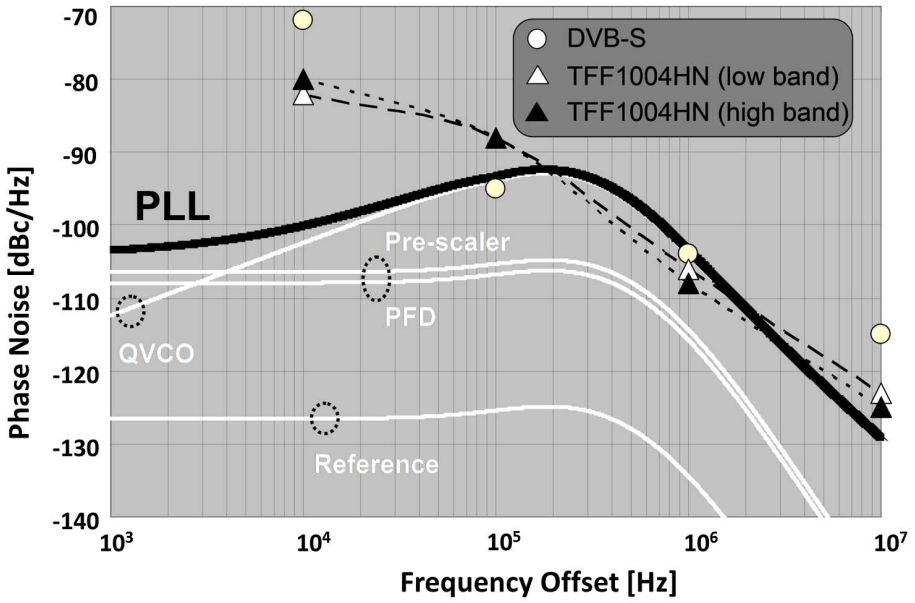

Figure 2.20: Simulated PLL phase noise (black curve).

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phase noise depicted in Figure 2.18 has been therefore inserted in a PLL simulation carried out with Matlab. The noise contributions of the pre-scaler, of the phase and frequency detector, and of the reference have been set to typical values. The loop filter was designed so that to obtain a PLL bandwidth of 400 kHz and a phase margin of 60°. Figure 2.20 shows the simulated phase noise (black curve). The white lines are the contributions of the single building blocks. The PLL phase noise is very close to the DVB-S phase noise specifications (open circles) at the offset frequencies of 100 kHz and 1 MHz [20]. The simulated phase noise is higher than standard limit in the offset frequency range 100 kHz - 1 MHz. The simulated phase noise is also comparable with the phase noise exhibited by the TFF1004HN commercial product [21] and it is better for offset frequencies lower than 100 kHz. As further discussion about Figure 2.20, it is worth pointing out that the phase noise and, in particular, the tuning range specifications have to be addressed by introducing a switched capacitor bank in the VCO topology during the design of the final PLL [22].

The quadrature outputs measurements have not carried out because we don't have the instrumentations for this kind of measurements at 15 GHz.

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3 millimeter Wave PLL

This chapter introduces the main mmW applications at 60 GHz*,* 77 GHz *and* 94 GHz*. In particular, this chapter reports on the design of the VCO and the division chain of a Phase-Locked Loop for WPAN applications. The blocks are designed in Si CMOS* 65 nm *technology.*

3.1 Phase-Locked Loop

Phase-Locked Loops (PLL), as mentioned earlier, have a variety of applications. However, in this work we will focus on their use as a frequency synthesizer. In a Charge-Pump PLL (CPPLL) based frequency synthesizer [23], a frequency divider is inserted in the feedback path, as depicted in Figure 3.1. The Phase-Frequency Detector (PFD) receives at one input the low-frequency low-noise input signal (running at f_{REF}) and at the other one the signal coming from the feedback. It compares their phase and frequency and it generates a digital waveform at output. This digital waveform, which is a train of voltage pulses, is then transformed into a train of current pulses by the Charge-Pump (CP), which output is averaged by the low-pass Loop Filter (LF) to produce the tuning voltage that controls the VCO oscillation frequency, namely f_{OUT}. As clearly seen in Figure 3.1, the signal at frequency f_{OUT} is not simply used as the output of the system, but is also divided down by M (an integer number known as the frequency divider division module) and fed back to the other input of the PFD. After a given settling time (related to the loop bandwidth), as a result of the negative feedback action performed by the loop, the phase and frequency of the output signal will be precisely related (locked) to the phase and frequency of the reference signal, which is both a stable and a low-noise source. In Figure 3.1, starting from a reference signal at frequency f_{REF}, an output frequency M times higher is obtained, i.e. $f_{OUT} = M \cdot f_{REF}$. By varying the frequency divider division module M in integer steps acting on the FCW, it is possible to vary the output frequency f_{OUT} with a frequency resolution equal to f_{REF}. This architecture is thus known as Integer-N frequency synthesizer.

In order to handle several tightly spaced channel, e.g. for the Global System for

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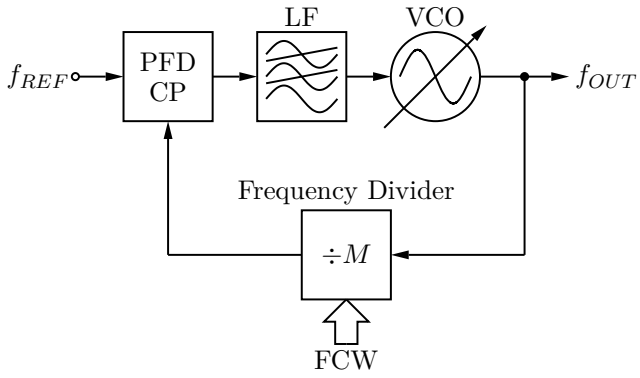

Figure 3.1: General block diagram of a CPPLL.

Mobile communication (GSM) a channel spacing of 200 kHz is used while the received frequency is at 1.8 GHz, it is of course desirable to increase the frequency resolution, which in turn requires lowering the reference frequency. Stability considerations require the loop bandwidth B_W to be lower than the reference frequency (as a rule-of-thumb, $B_W \approx f_{REF}/10$ [23]), thus lowering f_{REF} means lowering B_W. Indeed, lowering the bandwidth of the loop has some drawbacks, for instance:

- the correcting action performed by the negative feedback as a result of, let's say, a variation in the division module M, will be slowed down (the settling time T_S of the loop is inversely proportional to its bandwidth, i.e. $T_S \alpha B_W^{-1}$);

- the VCO phase-noise undergoes high-pass filtering while passing through the loop. So its suppression will be poorer if the bandwidth is decreased (this is a big issue in CMOS technology because of the high MOS flicker noise level).

To solve these problems, the constraint that the divider division module must be an integer number has to be broken, in particular modifying (dithering) dynamically its value such that on the average a fractional division module is produced; for this reason, such an architecture is known as Fractional-N frequency synthesizer: in this way the frequency resolution is no more dependent on the reference frequency.

In the end, the objective is to produce a division module that is a fractional number by switching between N and $N+1$; using an accumulator and a dual-modulus frequency divider (also called prescaler), as depicted in Figure 3.2, allows to achieve this result: assuming that the loop is locked and the division module is set to N, at each divider output pulse the accumulator value is increased by $n\,[k]$; once its internal state reaches or surpasses the full-scale, the carry output (called $c_O\,[k]$ in Figure 3.2) is asserted, thus the division module is set to $N+1$ for the entire cycle. The result is that, on the average, the divider module turns out to be a fractional number [2].

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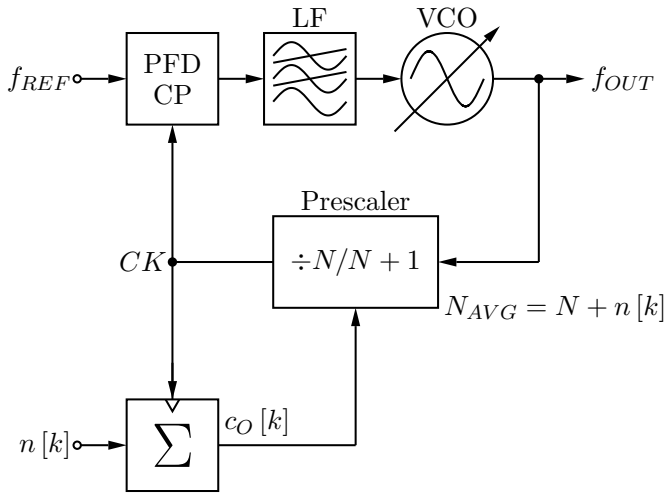

Figure 3.2: General block diagrams of a fractional CPPLL.

3.1.1 PLL linear model

Phase-Locked Loop are feedback systems which are inherently non-linear. However, their essential operation can be approximated very well by linear analysis. In such an analysis, the Laplace transform is a valuable tool. The concept of transfer functions, which describe the s- domain relation between input and output of a linear circuit, is used to analyze the open-loop and closed-loop characteristics of the PLL.

In [24], the phase of a locked PLL is described with the mathematical model depicted in Figure 3.3 where K_ϕ represents the PFD, $Z\,(s)$ the LF loop filter, K_{VCO}/s is the VCO and $1/N$ the frequency divider transfer functions.

Assuming that Figure 3.3 represents a general CPPLL, as it is done in [24], cutting the feedback and taking the ratio θ_I/θ_E gives the open loop gain G_{LOOP}:

$$G_{LOOP}\,(s) = \frac{\theta_I}{\theta_E} = \frac{K_\phi Z\,(s)}{N}\frac{2\pi K_{VCO}}{s} \tag{3.1}$$

where $K_\phi = K_{PFD} \cdot I_{CP}/\,(2\pi)$ is the gain of the PFD-CP combination and $Z\,(s)$ the LF transfer function. A 2π factor has been added to the K_{VCO} gain to take into account the frequency-to-phase conversion. The LF transfer function, $Z\,(s)$, depends of the filter chosen. A simple choice is a 2^{nd}-order passive LF, depicted in Figure 3.4a; in Figure 3.4b is depicted a 3^{rd}-order passive LF, which is an alternative to the 2^{nd}-order LF to be used when a stronger spurs suppression is required. Since the VCO itself introduces a pole in the origin in the transfer function and the 2^{nd}-order LF adds other two poles, the resulting overall PLL is a 3^{rd}-order system; on the other hand, if a 3^{rd}-order LF is used, the resulting overall PLL is a 4^{th}-order system.

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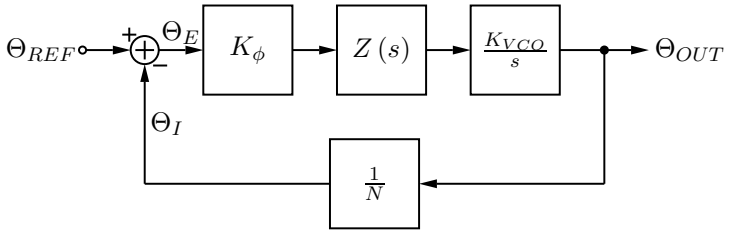

Figure 3.3: Generalized PLL linear model.

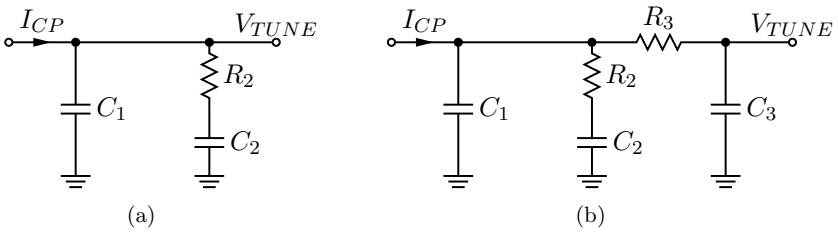

Figure 3.4: Analog LFs of: (a) 2^{nd} and (b) 3^{rd}-order.

The 2^{nd}-order passive LF transfer function is equal to:

$$\begin{aligned} Z(s) &= \left(R_2 + \frac{1}{sC_2}\right) // \frac{1}{sC_1} \\ &= \frac{1 + sR_2C_2}{s^2(C_1C_2R_2) + s(C_1 + C_2)} \\ &= \frac{1}{s} \cdot \frac{1}{C_1 + C_2} \cdot \frac{1 + sR_2C_2}{1 + sR_2\frac{C_1C_2}{C_1+C_2}} \qquad (3.2) \\ &= \frac{1}{s} \cdot \frac{1}{C_1 + C_2} \cdot \frac{1 + sT_Z}{1 + sT_P} \qquad (3.3) \\ &= \frac{1}{sC_1} \cdot \frac{T_P}{T_Z} \cdot \frac{1 + sT_Z}{1 + sT_P} \qquad (3.4) \end{aligned}$$

In Equation (3.3) and Equation (3.4) the zero and pole time constants, $T_Z = R_2C_2$ and $T_P = R_2C_1C_2/(C_1 + C_2)$ respectively, have been defined. As expected, the 2^{nd}-order LF transfer function contains two poles. Substituting Equation (3.4) in Equation (3.1) for $Z(s)$, the 3^{rd}-order open loop gain G_{LOOP} useful in the design process is obtained:

$$G_{LOOP}(s) = \frac{2\pi K_\phi K_{VCO}}{sN} \cdot \frac{1}{sC_1} \cdot \frac{T_P}{T_Z} \cdot \frac{1 + sT_Z}{1 + sT_P} \qquad (3.5)$$

which, if plotted versus the frequency, assumes the general form sketched in Figure 3.5.

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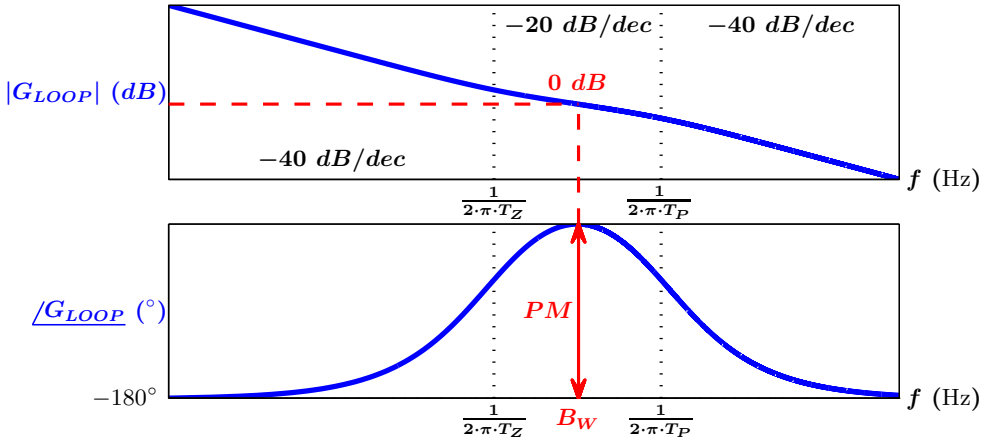

Figure 3.5: 3^{rd}-order system open loop gain Bode plot.

In Figure 3.5 both the phase margin PM and the bandwidth B_W are highlighted. The LF component can be designed to achieve the target PM and B_W as follows: from the inspection of Figure 3.5, the phase margin PM is defined as the difference between $-180°$ and the open loop transfer function phase at the frequency corresponding to a 0 dB gain. In order to insure stability, the phase margin must be chosen between 30° and 70°: choosing higher phase margin gives higher stability but with a slower transient response.

Since $s = j\omega$, Equation (3.5) is equivalent to:

$$G_{LOOP}(j\omega) = -\frac{2\pi K_\phi K_{VCO} T_P}{\omega^2 N C_1 T_Z} \cdot \frac{1 + j\omega T_Z}{1 + j\omega T_P} \tag{3.6}$$

The magnitude of the open loop gain is then equal to:

$$|G_{LOOP}(\omega)| = \frac{2\pi K_\phi K_{VCO} T_P}{\omega^2 N C_1 T_Z} \cdot \frac{\sqrt{1 + (\omega T_Z)^2}}{\sqrt{1 + (\omega T_P)^2}} \tag{3.7}$$

On the other hand, the phase of the open loop gain is then equal to:

$$\angle G_{LOOP}(\omega) = 180 + \arctan(\omega T_Z) - \arctan(\omega T_P) \tag{3.8}$$

which has the trend expected from Figure 3.5.

In order to compute the frequency value for which the phase reaches the maximum in term of T_Z and T_P, the derivative of Equation (3.8) must be computed. First of all, recall the notable derivative from mathematical analysis:

$$\frac{\mathrm{d}}{\mathrm{d}x} \arctan(f(x)) = \frac{f'(x)}{1 + f^2(x)} \tag{3.9}$$

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Then, the derivative of Equation (3.8) is taken and set equal to zero:

$$\frac{\mathrm{d}}{\mathrm{d}\omega}\angle G_{LOOP}\left(2\pi B_W\right) = 0$$
$$\frac{T_Z}{1+\left(2\pi B_W T_Z\right)^2} - \frac{T_P}{1+\left(2\pi B_W T_P\right)^2} = 0 \tag{3.10}$$

which, solved for the bandwidth, gives $B_W = 1/\left(2\pi\sqrt{T_Z T_P}\right)$. Substituting $\omega = 2\pi B_W$ in Equation (3.8) and the resulting equation in the phase margin definition, i.e. $PM \triangleq -180 + \angle G_{LOOP}\left(B_W\right)$:

$$PM = \arctan\left(2\pi B_W T_Z\right) - \arctan\left(2\pi B_W T_P\right) \tag{3.11}$$

and then applying the tangent operator at both the members:

$$\tan\left(PM\right) = \tan\left[\arctan\left(2\pi B_W T_Z\right) - \arctan\left(2\pi B_W T_P\right)\right] \tag{3.12}$$

Applying the trigonometric identity:

$$\tan\left(\alpha-\beta\right) = \frac{\tan\alpha - \tan\beta}{1+\tan\alpha\cdot\tan\beta} \tag{3.13}$$

into left side of Equation (3.12):

$$\begin{aligned}\tan\left(PM\right) &= \frac{\tan\left[\arctan\left(2\pi B_W T_Z\right)\right] - \tan\left[\arctan\left(2\pi B_W T_P\right)\right]}{1+\tan\left[\arctan\left(2\pi B_W T_Z\right)\right]\cdot\tan\left[\arctan\left(2\pi B_W T_P\right)\right]} \\ &= \frac{2\pi B_W T_Z - 2\pi B_W T_P}{1+\left(2\pi B_W\right)^2 T_Z T_P}\end{aligned} \tag{3.14}$$

From Equation (3.10) $B_W = 1/\left(2\pi\sqrt{T_Z T_P}\right)$, then Equation (3.14) simplifies in:

$$2\cdot\tan\left(PM\right) = 2\pi B_W T_Z - 2\pi B_W T_P \tag{3.15}$$

and substituting $T_Z = 1/\left[\left(2\pi B_W\right)^2 T_P\right]$ into Equation (3.15) gives the second order equation:

$$\left(2\pi B_W\right)^2 T_P^2 + 2\cdot\tan\left(PM\right)\cdot\left(2\pi B_W\right) T_P - 1 = 0 \tag{3.16}$$

Solving Equation (3.16) for T_P and discarding the negative solution (since it is a time constant its value is bounded to values greater than 0):

$$T_P = \frac{\sqrt{1+\tan^2\left(PM\right)} - \tan\left(PM\right)}{2\pi B_W} = \frac{\sec\left(PM\right) - \tan\left(PM\right)}{2\pi B_W} \tag{3.17}$$

where the identity $\sqrt{1+\tan^2\alpha} = 1/\cos\alpha = \sec\alpha$ has been exploited.

Since T_P has been calculated and B_W is known, T_Z is found as:

$$T_Z = \frac{1}{\left(2\pi B_W\right)^2 T_P} \tag{3.18}$$

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To summarize, for given phase margin and bandwidth values, the pole and zero time constants are found using Equations (3.17) and (3.18), respectively.

The following step, which allows to synthesize a LF which satisfies to the PM and B_W constraints when inserted in the loop, i.e. it introduces a zero and a pole at respectively $1/(2\pi T_Z)$ and $1/(2\pi T_P)$, is to compute C_1, C_2 and R_2. From Figure 3.5, for a frequency equal to B_W, the magnitude of the open loop gain is unitary; therefore substituting $\omega = 2\pi B_W$ in Equation (3.7) and equating the result to one allows to compute the value of C_1:

$$|G_{LOOP}(2\pi B_W)| = 1$$

$$C_1 = \frac{2\pi K_\phi K_{VCO}}{(2\pi B_W)^2 N} \cdot \frac{T_P}{T_Z} \cdot \frac{\sqrt{1+(2\pi B_W T_Z)^2}}{\sqrt{1+(2\pi B_W T_P)^2}} \tag{3.19}$$

Furthermore, recall that $T_Z = R_2 C_2$ and $T_P = R_2 C_1 C_2/(C_1 + C_2)$. Solving the ratio T_Z/T_P for C_2

$$C_2 = C_1 \left(\frac{T_Z}{T_P} - 1\right) \tag{3.20}$$

while solving T_Z for R_2:

$$R_2 = \frac{T_Z}{C_2} \tag{3.21}$$

This method allows to design a LF for given values of open loop bandwidth B_W, phase margin PM, VCO gain K_{VCO}, CP current I_{CP}, PFD gain and divider division module N, so in the end to synthesize the required CPPLL.

If a 3^{rd}-order LF is used, the attenuation introduced is [24]:

$$\alpha_{\text{dB}} = 20\log\left[(2\pi f_{REF} R_3 C_3)^2 + 1\right] \tag{3.22}$$

that can be solved for the time constant $T_{P3} = R_3 C_3$:

$$T_{P3} = \frac{\sqrt{10^{\frac{\alpha_{\text{dB}}}{20}} - 1}}{2\pi f_{REF}} \tag{3.23}$$

The additional pole must be lower than the reference frequency, in order to significantly attenuate the spurs, but must be at least 5 times higher than the loop bandwidth, or the loop will almost assuredly become unstable.

In order to compensate for the added low-pass section, the filter component values are recalculated using the new open loop unity gain frequency, B_C [24]:

$$B_C = \frac{\tan(PM)\cdot(T_P + T_{P3})}{2\pi\left[(T_P + T_{P3})^2 + T_P T_{P3}\right]} \cdot \left[\sqrt{1 + \frac{(T_P + T_{P3})^2 + T_P T_{P3}}{\tan(PM)\cdot(T_P + T_{P3})}} - 1\right] \tag{3.24}$$

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Then, also T_Z is modified as follows:

$$T_Z = \frac{1}{(2\pi B_C)^2 (T_P + T_{P3})} \tag{3.25}$$

and C_1 as:

$$C_1 = \frac{T_P}{T_Z} \cdot \frac{K_\phi K_{VCO}}{(2\pi B_C)^2 N} \cdot \sqrt{\frac{\left[1 + (2\pi B_C T_Z)^2\right]}{\left[1 + (2\pi B_C T_P)^2\right]\left[1 + (2\pi B_C T_{P3})^2\right]}} \tag{3.26}$$

On the other hand, C_2 and R_2 are still derived from Equations (3.20) and (3.21), respectively.

The only component values that still remain to be determined are therefore C_3 and R_3: being bounded by Equations (3.22) and (3.23), their values are somewhat arbitrary. As a rule of thumb C_3 can be chosen equal to $C_1/10$ otherwise T_{P3} will interact with the primary poles of the filter. Likewise, R_3 must be chosen at least twice the value of R_2.

Although not exact, the linear assumptions used in this design technique provide good results for loop filter bandwidths of up to one-fifth of the reference rate [24, 2].

3.2 Frequency Divider

Frequency Divider (FD) can be categorized into digital or analog. The digital class of dividers is sub-divided into static and dynamic FDs whereas the analog consist of regenerative or Miller divider and Injection-Locked (IL) Frequency Divider.

3.2.1 Static Frequency Divider

Static FD (SFD) are one of the most widely used class of dividers [25, 26]. They are usually based on an edge-triggered flip-flop in a negative feedback loop. The flip-flop is composed of two master and slave D-latches which are driven by anti-phase clock pulses. Figure 3.6 shows a standard Static FD. The dividing operation is achieved by connecting the inverted slave outputs to master D-latch inputs. Seen as a two stage ring oscillator, static frequency dividers can provide highly matched quadrature outputs which are required in the two step down-conversion in a transceiver.

In principle, any type of latch can be utilized in a SFD. However, traditional CMOS rail-to-rail implementations lead to long rise and fall times, resulting in low operation frequencies. In addition, the single-ended structure also suffers from supply noise coupling, potentially introducing jitter in the output. MOS current mode logic (MCML or just CML) sometimes also referred to as source coupled logic SCL, is a better alternative for D-latch implementation [27]. This logic family is characterized by, firstly, small voltage swings thus reducing the rise and fall times and enhancing the operation frequency. Secondly, the differential and current steering nature of MCML reduces the switching and supply noise resulting in a spur-free synthesizer output spectrum and lastly, it consumes

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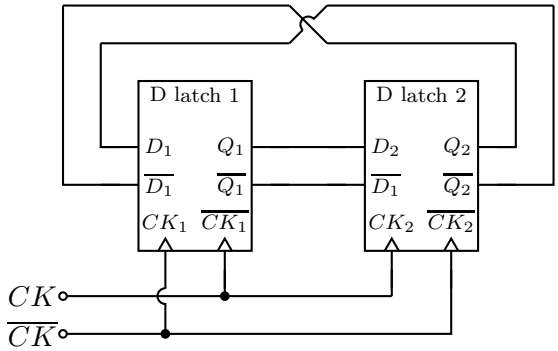

Figure 3.6: SCL based divide-by-two frequency divider.

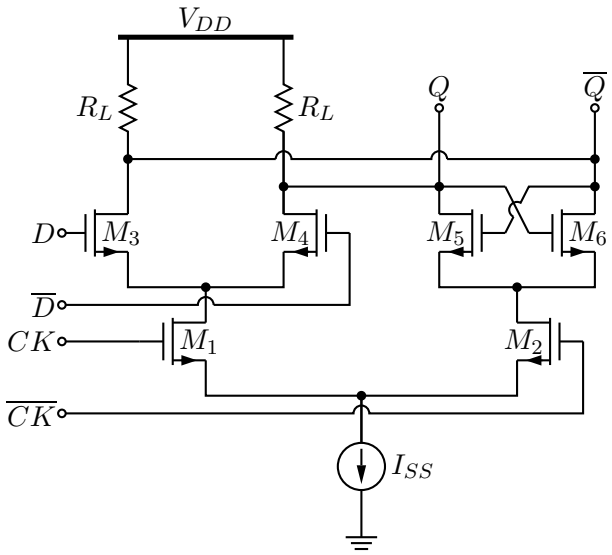

Figure 3.7: SCL D latch.

a constant current, hence the name static frequency divider. A D-latch based on MCML logic is shown in Figure 3.7. The maximum operation frequency of the SFD depends on the propagation delay from input D to output Q in a D-latch and can be estimated by:

$$f_{max} \leq \frac{1}{\tau_{dp}} \tag{3.27}$$

where τ_{dp} is the propagation delay. In a differential circuit (such as CML logic) τ_{dp} for rising and falling edge is identical and in first order, proportional to the charging time constant τ_L, i.e.,

$$\tau_{dp} \propto \tau_L = R_L C_L \tag{3.28}$$

where R_L is the load resistance and C_L is the total capacitance at the output node

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consisting of parasitic contribution from the latch transistors $M_4 - M_6$, output buffer transistors (not shown in Figure 3.7) and layout interconnects. It is evident that, to maximize speed, τ_L or R_L and C_L should be minimized. However, there is a trade-off between the two passive values. If R_L decreases, the gain $g_m R_L$ of the transistors $M_3 - M_4$ also decreases. In order to compensate this decrease, larger transistors are required to boost the g_m thus increasing the total capacitance. On the other hand if C_L is reduced by using smaller transistors, R_L needs to be increased to maintain a sufficient output voltage swing. Techniques such as inductive peaking [25, 28], distributed loading and LC-tank loading [29] have been employed to increase the bandwidth of SFDs.

A large number of static frequency dividers have been reported in the frequency range up to 40 GHz [25, 28, 30, 31, 32, 33, 34] and a few implementations above 60 GHz [2].

3.2.2 True Single Phase Clock

The True Single Phase Clock (TSPC) logic was firstly proposed in [35], to overcome the problems of the clocked CMOS logic which requires a non-overlapping pseudo two-phase clock to work properly; in the end this means that four clock signals have to be distributed and between these two pairs no overlap should occur. Of course, clock skews in the system will cause serious problems, which are exacerbated with the increasing of the operating speed. On the other hand, TSPC logic requires only one clock signal, thus avoiding the skew problem present in the clocked CMOS logic.

In Figure 3.8a is proposed a TSPC positive-edge triggered register, while in Figure 3.8c is proposed a TSPC divide-by-two frequency divider. The TSPC positive-edge triggered register of Figure 3.8a works as follows: when CK is low M_{P1} is ON thus the series of M_{N1}, M_{P1} and M_{P2} behaves as an inverter, sampling the data D and inverting it at node G_3. Furthermore, since CK is low M_{N2} is OFF. As a consequence, even if G_3 is high, the pull-down network is OFF: the only path for the current is through M_{P3}, thus when CK is low M_{P3} pre-charges node D_3 to V_{DD}. As a consequence, both M_{N5} and M_{P4} are OFF because the gate of M_{N5} is held low by the CK while the gate of M_{P4} is held high by D_3 and therefore the output $\overline{Q}$ is holding the previous state being floating (high-impedance level).

To sum up, when CK is low:

- the inverter M_{N1}, M_{P1} and M_{P2} is ON and thus it samples and inverts the input D at node G_3;
- the inverter M_{N2}, M_{N3} and M_{P3} is OFF and thus M_{P3} is pre-charging node D_3 at V_{DD};
- the inverter M_{N4}, M_{N5} and M_{P4} is OFF and thus the output $\overline{Q}$ is floating, i.e. the output of the previous state is held stable.

On the clock rising edge, the inverter M_{N2}, M_{N3} and M_{P3} evaluates the data at node G_3 because M_{P3} is now OFF while M_{N2} is ON, so the value of D_3 depends on

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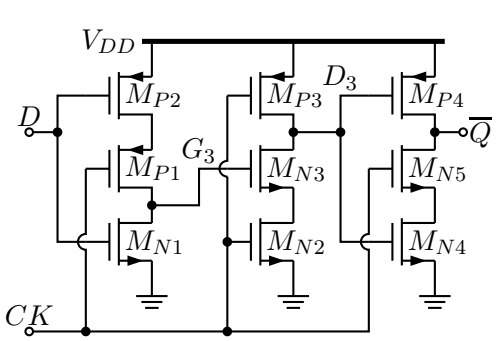
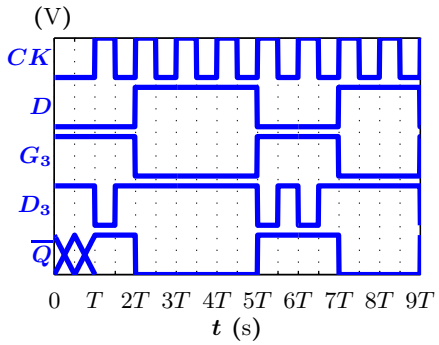
the logic level at node G_3: if G_3 is high then D_3 is discharged to ground, otherwise D_3 stays at V_{DD}. The inverter M_{N4}, M_{N5} and M_{P4} is now ON because M_{N5} is turned ON by the high CK: the level of D_3 is then inverted and transferred to the output $\overline{Q}$ (the input data D has undergone three inversions and thus it is copied in its complementary form at output $\overline{Q}$).

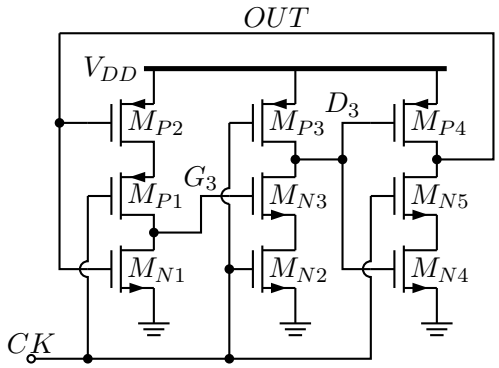
During the positive clock phase there is one criticality: if data D is high, since the M_{N1}, M_{P1} and M_{P2} inverter pull-up network is OFF, node G_3 is discharged to ground by M_{N1}. As a consequence, the input must be kept stable until the value at node G_3 has propagated correctly to node D_3: this is the hold time of the register. The overall propagation delay, on the other hand, is roughly equal to three times the delay of one inverter.



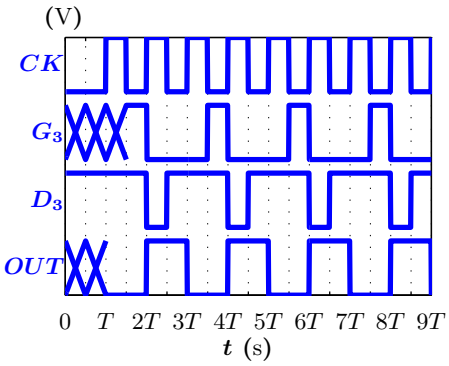
(a) Register.



(b) Transient response of Figure 3.8a.



(c) Divide-by-two frequency divider.



(d) Transient response of Figure 3.8c.

Figure 3.8: TSPC based: (a) register and (c) divide-by-two frequency divider.

Passing from the TSPC register described to a divide-by-two-frequency divider is quite simple: it is enough to connect nodes $\overline{Q}$ and D with a feedback, as in Figure 3.8c. In Figure 3.8d it is depicted the divider transient response: assume that CK is low; as a result, M_{P3} keeps D_3 at V_{DD}. As soon as the clock goes high, M_{N4} and M_{N5} turn ON lowering OUT. At the next clock negative pulse, at $t = 1.5T$, since OUT and CK are both low, M_{P1} and M_{P2} turn ON so G_3 goes high. At $t = 2T$, when CK is high, M_{N2}

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and M_{N3} turn ON lowering D_3, then OUT will go high (after an inverter propagation delay); after another inverter propagation delay also M_{N1} will turn ON lowering G_3. The next clock negative pulse charges D_3 to V_{DD} by means of M_{P3}. At $3T$, when both CK and D_3 are high, M_{N4} and M_{N5} turn ON lowering OUT. Then at $t = 3.5T$, when both CK and OUT are low, M_{P1} and M_{P2} turn ON again so G_3 goes high. At the next clock pulse the result is that D_3 goes low, so OUT goes high and the cycle will start again from the beginning.

The transistors' sizing is of course critical to achieve a correct functionality. There are no general guidelines, but the following example helps in focusing a problem related to the TSPC register and explain how to correct it if, from simulation results, it turns out that the TSPC register is affected by this kind of problem. Consider the following case: CK low, D low (which means G_3 high) and also Q low [36] (Q is obtained by inverting $\overline{Q}$ with an inverter). As explained, node D_3 is pre-charged to V_{DD}, thus M_{N4} turns ON. When CK goes high, both D_3 and $\overline{Q}$ begin to discharge: D_3 discharges through M_{N2} (that is ON since CK is high) and M_{N3} (that is ON since G_3 is high by hypothesis) while $\overline{Q}$ discharge through M_{N4} (that is ON since D_3 is pre-charged to V_{DD}) and M_{N5} (that is ON since CK is high). Once D_3 is low enough, $\overline{Q}$ is pulled high by M_{P4}. This results in a glitch in the output which may cause fatal errors. To avoid this problem, care must be taken in increasing the relative strength of the $M_{N2} - M_{N3}$ pull-down network with respect to that of the $M_{N4} - M_{N5}$ pull-down network, so that D_3 discharges faster then $\overline{Q}$.

Also in [35] the sizing of the transistors is discussed: neither there design guidelines are given since this is a complex problem because the speed of a CMOS circuits depends in a complex way on the sizes as they influence both the current capability and the capacitance. The general rule is to just keep the transistors length as small as possible (it is limited by the process), whereas the widths are optimized for speed; often, the speed versus width function does not show an optimum but is monotonic: in such cases the cost must be taken into account.

For simple structures, as an inverter chain, general rules exist for sizing: for example, each inverter has devices that are three times larger than the previous inverter devices. But for more complex structure it is not possible to obtain analytical results, so the best thing to do is to vary the device sizes in a simulator or to use a computer tool developed for automatic speed optimization through device sizing [2].

3.2.3 Regenerative frequency dividers

The working principle of regenerative frequency dividers can be explain with the aid of Figure 3.9 [37]: one input of the mixer is fed with the input frequency f_{in}, while the other input with the output frequency f_{out}. As a consequence, at the output of the mixer two tones at $f_{in} \pm f_{out}$ appear, with lower amplitudes with respect to the input f_{in} because of the mixer action (this is why an amplifier with gain A is inserted in the chain).

The action of the Low-Pass Filter (LPF) is to remove the tone at $f_{in} + f_{out}$ so just

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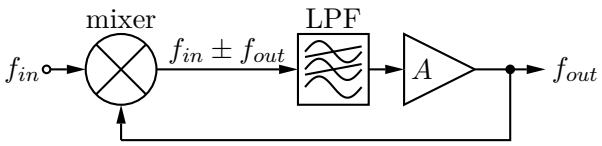

Figure 3.9: Regenerative divide-by-two frequency divider block diagram.

the $f_{in} - f_{out}$ frequency survives at the output of the loop; at the output node therefore holds the relation:

$$f_{in} - f_{out} = f_{out} \Rightarrow f_{out} = \frac{f_{in}}{2} \tag{3.29}$$

As clear from Figure 3.9, this kind of dividers require many building blocks, so they are not suited for low-power applications.

3.2.4 Injection Locking Frequency Dividers

Figure 3.10 depicts the model for an Injection-Locked Oscillator (ILO) proposed in [38]. If one supposes to ground the input signal v_{in}, the model describes a free-running oscillator: for example, in a cross-coupled LC oscillator, the nonlinear block $f(e)$, which models all the nonlinearities of the system, is the cross-couple pair while the Band-Pass-Filter (BPF), which is a frequency selective block, is the LC tank. The output of the nonlinear block is spectrally rich but the BPF extracts from it just the desired tone and feeds it back to the input, closing the loop.

When v_{in} is grounded, the system oscillates if the loop satisfies the Barkhausen oscillation criteria:

$$\begin{cases} |G_{LOOP}| & = 1 \\ \underline{/G_{LOOP}} & = 0 \end{cases} \tag{3.30}$$

where G_{LOOP} is the loop gain. If a non-zero input is applied and the system has to keep oscillating, the Barkhausen oscillation criteria must be indeed met.

If the goal is to realize an ILO that operates as a divide-by-two frequency divider, the BPF must be tuned to f_{out}. In addition, since a division-by-two must be achieved so that $f_{in} = 2f_{out}$, the nonlinearity must be of the second order.

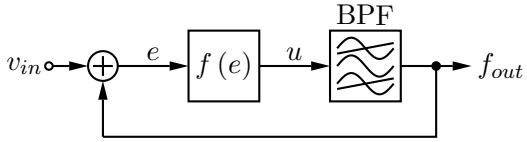

Figure 3.10: Injection Locking Frequency Divider block diagram.

The advantage of this family of dividers is their low-power consumption because of the reactive components used in the BPF which conserves the energy instead of wasting it. On the other hand, the reactive components are also a disadvantage in the integrated

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realization because they use a large die area and also because they limit the bandwidth [2].

3.3 Millimeter Wave IC Applications

The expression millimeter Wave (mmW) designates a RF band having a wavelength of ten to one millimeter. According to the International Telecommunications Union (ITU) radio regulations resumed in Table 3.1, it corresponds to the region of Extremely High Frequency (EHF: 30 GHz to 300 GHz).

Table 3.1: International Telecommunications Union (ITU) Radio Band.

Nr	Symbol	Desigantion	Frequency Range	Wavelangth Range
1	ELF	Extremely Low Frequency	3 Hz to 30 Hz	100 000 km to 10 000 km
2	SLF	Super Low Frequency	30 Hz to 300 Hz	10 000 km to 1000 km
3	ULF	Ultralow Frequency	300 Hz to 3000 Hz	1000 km to 100 km
4	VLF	Very Low Frequency	3 kHz to 30 kHz	100 km to 10 km
5	LF	Low Frequency	30 kHz to 300 kHz	10 km to 1 km
6	MF	Medium Frequency	300 kHz to 3000 kHz	1 km to 0.1 km
7	HF	High Frequency	3 MHz to 30 MHz	100 m to 10 m
8	VHF	Very High Frequency	30 MHz to 300 MHz	10 m to 1 m
9	UHF	Ultrahigh Frequency	300 MHz to 3000 MHz	1 m to 0.1 m
10	SHF	Super High Frequency	3 GHz to 30 GHz	1 m to 0.1 m
11	EHF	Extremely High Frequency	30 GHz to 300 GHz	0.1 mm to 1 mm

In the context of microelectronics it is more useful to consider the wavelength in a silicon oxide layer that is roughly half the wavelength in open space, according to the well-known relation:

$$\lambda_{ox} = \frac{1}{f\sqrt{\epsilon_{ox}\epsilon_0\mu_0}} = \frac{1}{f\sqrt{\epsilon_{ox}}\sqrt{\epsilon_0\mu_0}} = \frac{c}{f\sqrt{\epsilon_{ox}}} = \frac{\lambda_0}{\sqrt{\epsilon_{ox}}} \approx \frac{\lambda_0}{1.9} \tag{3.31}$$

where the relative permittivity of silicon oxide ϵ_{ox} is assumed to be equal to 3.6 and frequency-independent.
A more appropriate placement of the millimeter wave band is therefore in the 15-158 GHz range. In particular, we will consider as millimeter wave the electromagnetic spectrum between 60 GHz to 110 GHz.
As a matter of fact, electronics at lower frequencies (at least up to 20-30 GHz) can rely over the traditional radiofrequency design methods and techniques. On the contrary design of silicon-based integrated circuits operating in the 60-110 GHz range, requires the development of a dedicated methodology capable to address the numerous difficulties

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emerging along with the frequency increase.
Very recently the same design methodology has been gradually extended to higher frequency known as sub-millimeter wave or terahertz radiation, opening the way to the so-called terahertz-electronics that however will not be considered in this thesis.
During the last few years, the interest towards mmWs has rapidly grown, leading to the development of a large number of potential applications. As well, the recent improvements in silicon-based technologies like CMOS and BiCMOS processes have made possible the realization of low-cost implementations of microelectronic systems operating in the millimeter wave band.
Without any presention of being exhaustive, the next three sections give an overview of the most common applications in millimeter wave band such as Wireless Personal Area Network (WPAN), high data rate wireless communications at 60 GHz, short and long range radar at 77-79 GHz, and imaging systems at 94 GHz [39].

3.3.1 Millimeter wave applications at 60 GHz

The 60GHz band [40, 41] has attracted the interest of researchers in the past several years, as it offers ample and license-free bandwidth. This advantage becomes more evident when considering that the availability of about 7 GHz of unlicensed bandwidth is guaranteed in many countries worldwide, as shown in Figure 3.11. For example, the range from 57 GHz to 64 GHz is currently available in the US, while 59 GHz to 66 GHz are available in Japan. Furthermore 60 GHz band is less restrict in terms of power limits when compared to other concurrent wideband systems, like Ultra-Wideband (UWB), for instance. These characteristics make 60 GHz technology particularly suited for gigabit wireless applications that currently are technically constrained at lower frequency.

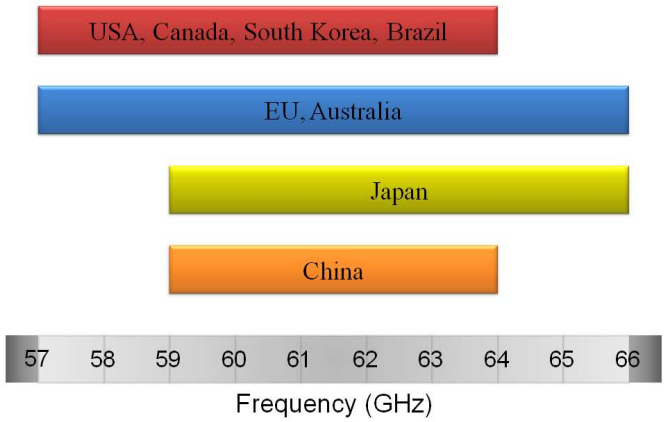

Figure 3.11: Worldwide frequency allocation for 60 GHz band and operation.

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As depicted in Figure 3.12, the atmospheric absorption presents a peak at 60 GHz due to oxygen absorption that puts a severe limit on the distance that 60 GHz transmissions can handle - at least in the case of low-power applications - limiting it to close-range communications. In home-space, however, oxygen absorption is not a big problem, so 60 GHz is beginning to look like a useful way to provide dramatic speed-ups over traditional Wireless Local Area Networks (WLANs) and is particularly indicated for Wireless Personal Area Network (WPAN)s. A WPAN is designed to provide short-range (<10 m), very-high-speed (>2 Gb/s) multi-media data services to computer terminals and consumer appliances located in rooms, office space, "hot spots" and kiosks.

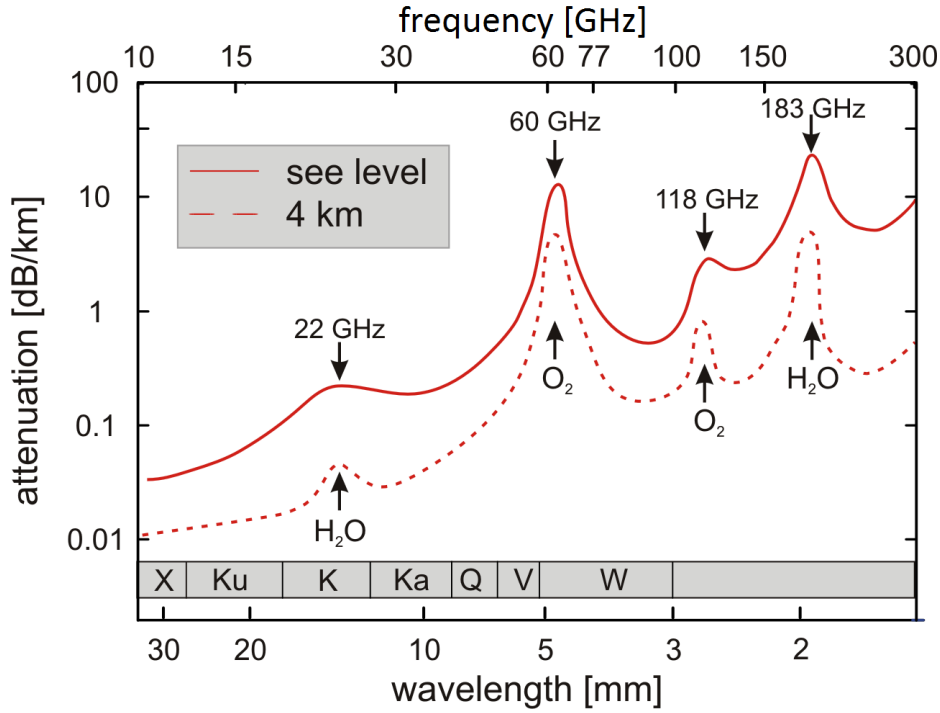

Figure 3.12: Atmospheric absorption of millimeter wave.

Wireless PANs will provide higher data rates, and shorter range, than comparable WLANs but long enough to cover the size of most offices, medium-size conference rooms, and rooms in personal home. Various electronic devices could be interconnected, including laptops, cameras, and monitors. Potential applications include wireless display, wireless docking station, and wireless streaming of data from one device to the other. A 60 GHz link could be used to replace various cables used today in the office or home, including gigabit Ethernet (1 Gbps), USB 2.0 (480 Mbps), or IEEE 1394 (800 Mbps). Currently, the data rates of these connections have precluded wireless links, since they require so much bandwidth. While other wireless standards are evolving to address this

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market (802.11n and UWB), 60 GHz is still a viable candidate.

Figure 3.13: Example of Wireless Personal Area Network applications.

Besides oxygen absorption in open-space, different materials affect the propagation of 60 GHz signals in different ways and, whereas plasterboard or drywall absorption is not much greater than in the case of 2.4 GHz signals, other materials, on the contrary, cause a big fall-off in signal strength. Also human skin, for instance, absorbs 60 GHz radiation pretty efficiently and crossing a link between a computer and a media player synchronized over a 60 GHz system would break it.
To reduce the effect of absorption loss, many solutions such as directional antennas or beamforming techniques are currently investigated. If sufficient directionality is guaranteed in transmission, then atmospheric and material properties could also prove more of a benefit than a limitation, since they can prevent the signal from leaking into adjacent environment, reducing the risk of interference and enhancing security [39].

Standards and Regulations for 60 GHz WPAN applications

Several attempts of standardization have been recently proposed or are still in course of definition. For example, the IEEE 802.15 Task Group 3c is working since 2005 on the Wireless Personal Area Network (WPAN), leading to the definition of the IEEE 802.15.3c standard in September 2009 [42, 43]. Besides, Wireless HD [44], the Wireless Gigabit Alliance (WiGig)[45], the IEEE 802.11ad working group [46] and the ECMA-387 [47] have been also making standardization efforts on the 60 GHz frequency band. A detailed description of these documents is beyond the interest of this thesis; however

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the most important features of the IEEE and the ECMA standards are briefly described hereafter.
IEEE Std 802.15.3c is an amendment to IEEE Std 802.15.3 that defines a Physical Layer (PHY) operating in the millimeter Wave band and the necessary modifications to the Medium Access Control (MAC) changes to support this PHY.
The PHY defines three operational modes as follows:

- Single Carrier (SC) mode optimized for low power and low complexity.
- High-Speed Interface (HSI) mode optimized for low-latency bidirectional data transfer.
- Audio/Visual (AV) mode optimized for the delivery of uncompressed, high-definition video and audio.

For devices that implement the mmW PHY, at least one of the three PHY modes is required. In addition, to promote coexistence and interoperability, a Common Mode Signaling (CMS) is defined based on a low data rate SC PHY mode.
The single carrier mode in mmW PHY (SC PHY) provides three classes of modulation and coding schemes targeting different wireless connectivity applications. As summarized in Table 3.2, Class 1 is specified to address the low-power low-cost mobile market while maintaining a relatively high data rate of up to 1.5 Gb/s; Class 2 is specified to achieve data rates up to 3 Gb/s; Class 3 is specified to support high performance applications with data rates in excess of 3 Gb/s.

Table 3.2: Modulation and Coding Schemes Classes in the SC PHY.

Class	Categorization
1	Data rate < 1.5 Gb/s
2	1.5 Gb/s $<$ Data rates < 3 Gb/s
3	Data rates > 3 Gb/s

The SC PHY supports a wide range of modulations, $\frac{\pi}{2}$ BPSK, $\frac{\pi}{2}$ QPSK, $\frac{\pi}{2}$ 8-PSK, $\frac{\pi}{2}$ 16-QAM, pre-coded MSK, pre-coded GMSK, on-off keying (OOK), and Dual Alternate Mark Inversion (DAMI). It operates on four RF channels, as defined in Table 3.3. A compliant implementation shall support at least 1 channel from the channels allocated for operation by its corresponding regulatory body.

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Table 3.3: RF Channels for mmW PHY.

Channel ID	Start Freq. [GHz]	Center Freq. [GHz]	Stop Freq. [GHz]
1	57.24	58.32	59.40
2	59.40	60.48	61.52
3	61.56	62.64	63.72
4	63.72	64.80	65.88

The high speed interface mode of mmW PHY (HSI PHY) is designed for devices with low-latency, bidirectional high-speed data and uses Orthogonal Frequency Division Multiplexing (OFDM). HSI PHY supports a variety of modulation and coding schemes (MCSs) using different frequency-domain spreading factors, modulations, and LDPC block codes.
The Audio/Visual (AV) PHY is implemented with two PHY modes, the High-Rate PHY (HRP) and Low-Rate PHY (LRP), both of which use Orthogonal Frequency Division Multiplexing (OFDM). The data rates supported by the HRP and the LRP are defined in Table 3.4 and Table 3.5, respectively.

Table 3.4: AV HRP data rates.

HRP mode index	Modulation	Data rate [Gb/s]
0	QPSK	0.952
1	QPSK	1.904
2	16-QAM	3.807
3	QPSK	1.904
4	16-QAM	3.807
5	QPSK	0.952
6	QPSK	1.904

Table 3.5: AV LRP data rates.

LRP mode index	Modulation	Data rate [Gb/s]
0	BPSK	0.952
1		1.904
2		3.807
3		1.904

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Different PHYs are a result of demands of different market segments. For example, one usage model is for kiosk applications. This usage model requires 1.5 Gb/s at a 1 m range. The SC-PHY can provide such a data rate at that short range with less complexity thus lower cost than an OFDM PHY. Another usage model is required by the streaming of uncompressed video. Due to the nature of uncompressed video signals, a special PHY, the AV PHY, was selected to provide high throughput. A third usage model involves an ad-hoc system to connect computers and devices around a conference table. In this usage model, all of the devices in the WPAN will have bidirectional, Non-LIne-Of-Sight (NLOS) high speed, low-latency communication, which is provided for by the HSI PHY.
Besides the suggestions for MAC and physical level, IEEE standard specifies also an optional beam forming protocol that can support a multitude of antenna configurations such as single antenna element, sectored antennas, switched antennas, and one-dimensional (1-D) and two-dimensional (2-D) beam forming antenna arrays.
The ECMA 387 standard defines three device types as follows:

- A type A device offers video streaming and WPAN applications in 10 m range line of sight/not line of sight multipath environments. It uses high gain trainable antennas. This device type is considered as the 'high end' - high performance device.

- A second type, type B device offers video and data applications over shorter range (1-3 m) point to point line of sight links with non-trainable antennas. It is considered as the 'economy' device and trades off range and not line of sight performance in favor of low cost implementation and low power consumption.

- The third type, type C device is positioned to support data only applications over point to point line of sight links at less than 1 m range with non-trainable antennas and no QoS guaranties. This type is considered as 'bottom end' device providing simpler implementation, lowest cost and lowest power consumption

The A, B, and C devices can interoperate with their own types independently and can coexist and interoperate with the other types leading to the implementation of heterogeneous network solution that provides interoperability between all device types. As depicted in Figure 3.14, each one of the three device types corresponds to a different organization of the PHY layer. The three PHYs converge into a single MAC level based on the ECMA-368 standard, with the necessary changes to support directional communication in 60GHz band.

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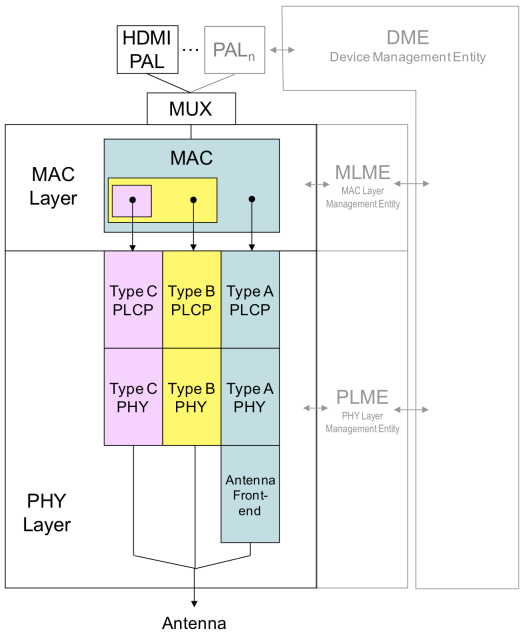

Figure 3.14: Protocol Structure of ECMA standard.

The Type A PHY includes two general transmission schemes, namely Single Carrier Block Transmission (SCBT), also known as Single Carrier with Cyclic Prefix, and OFDM; the Type B PHY has been designed using a simplified single carrier transmission scheme with a common beaconing mode based on differentially encoded BPSK modulation (DBPSK), thus allowing for both simple coherent and non-coherent demodulation and minimizing the implementation overhead to support interoperability with type A devices; the Type C PHY uses the simplest single carrier transmission scheme based on the Amplitude-Shift-Keying (ASK) modulation scheme.
The standard specifies four frequency channels each with a symbol rate of 1.728 Giga-Symbols/second and with a separation of 2.160 GHz, as suggested in Figure 3.15. All device types follow the same frequency plan.

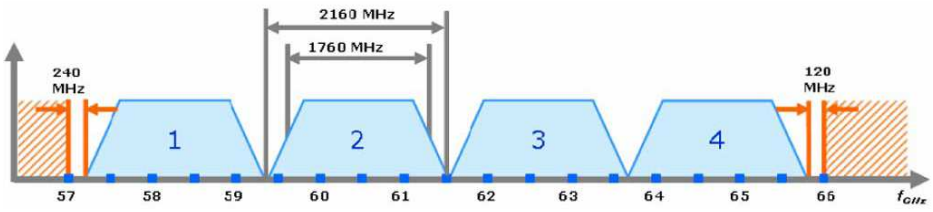

Figure 3.15: Frequency plan of ECMA standard.

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European regulation of WLANs and WPAN system operating in the 60 GHz band is provided by the European Telecommunications Standards Institute (ETSI). The technical characteristics of these applications are described in [48] and the specific technical requirements are defined in [49]. The most important features can be summarized as follows:

- frequency band is defined from 57 GHz to 66 GHz;
- the maximum spectral power density shall be limited to 13 dBm/MHz for indoor usage and to −2 dBm/MHz for indoor/outdoor;
- the maximum output power level, Effective Isotropic Radiated Power (EIRP), shall be limited to 40 dBm for indoor usage and to 25 dBm for indoor/outdoor;
- the limit level of unwanted emissions in the spurious domain for transmitter are reported in Table 3.6 (measured with 0 dBi antenna gain);
- the limit level of unwanted emissions in the spurious domain for receiver are reported in Table 3.7 (measured with 0 dBi antenna gain);
- the use of an integral antenna (that is an antenna designed as a fixed part of the equipment, without the use of an external connector and that, therefore, cannot be disconnected from the equipment by a user with the intent to connect another antenna) is required, to provide interference protection;
- a medium access protocol shall be implemented by the equipment and shall be active under all circumstances, in order to facilitate spectrum sharing with other devices in the wireless network [39].

Table 3.6: Transmitter spurious emissions.

Frequency band	Measurement bandwidth	Field Strenght at 3 m [dBμV/m]
30 MHz to 1 GHz	100 kHz	59
1 GHz to 132 GHz	100 MHz	65

Table 3.7: Receiver spurious emissions.

Frequency band	Measurement bandwidth	Field Strenght at 3 m [dBμV/m]
30 MHz to 1 GHz	100 kHz	38
1 GHz to 132 GHz	100 MHz	48

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3.3.2 Millimeter wave automotive radar sensors

The first experimental applications of radar in the automotive industry date back to the 1950s and yet in 1970s automotive radars were the object of systematic investigations [50, 51].
Years after years, safety has been one of the main concerns in the development of car industry, leading to several structural improvements capable to reduce the consequences of accidents on the driver and the passengers. In such a context, the introduction of radars represents a disruptive event, focusing on accident avoidance and prevention that, undeniably, are preferred to any system of crash protection.
Nowadays, the so-called autonomous or a Adaptive Cruise Control (ACC) is probably the most common application of automotive radar and is used to assist the driver and to augment its comfort. Practically speaking, a radar sensor is mounted behind the front

Figure 3.16: DISTRONIC radar sensor mounted on Mercedes Benz S-class vehicles.

bumper of a vehicle at a height of less than 1 m, where it is able to interrogate the road ahead and the adjacent traffic lanes forward of the vehicle location (Figure 3.16). Using this radar, the control system within the vehicle adjusts the cruise speed in response to a slower vehicle in a merging lane, or when following a vehicle in the same lane, in order to maintain the driver's selected minimum separation distance behind the other vehicle (Figure 3.17). An ACC system can constantly provide the driver with information about traffic situation in the environment, making driving less strenuous, especially in flowing traffic and in critical context like on motorways or dual carriageways.
ACC today uses Long-Range Radar (LRR) operating between 76 GHz and 77 GHz with a maximum bandwidth of 1 GHz. It uses distance scanning, which requires an operating range of approximately 150 m and is used at vehicle velocities not below 30 km/h. One or multiple narrow lobes control or scan the driving path in front of the car to determine the distance to the vehicle driving ahead for maintaining a constant minimum safety distance.
In 1999 Mercedes-Benz has been the first car manufacturer who introduced radar-based ACC system in its S-class vehicles [52]. Since then, radar based ACC systems are available in many high and mid-class models such as BMW 7 series, Jaguar (XKR, XK6), Cadillac (STS, XLR), Audi A8, VW Phaeton, Mercedes E, CL, CLK, SL class, BMW

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5 and 6 series, Audi A6, Nissan (Cima, Primera), Toyota (Harrier, Celsior), Lexus (LS, GS), Honda (Accord, Inspire, Odyssey) and their functionality have been gradually extended, including also pre-crash sensing and collision mitigation.
Besides radar-based equipments, also competing and complementing technologies in vehicular surround sensing and surveillance like Lidar, ultrasonics, and video-cameras have been tested since the first 1990s to implement parking aid, collision warning, and ACC as well. However, radar seems still to be the key technology for driver assistance and safety applications, due to its inherent advantages like weather independence and direct acquisition of range and velocity especially when compared to alternative sensors like video, laser, and ultrasonics. More recently, in 2003 - whereas European car manufacturers

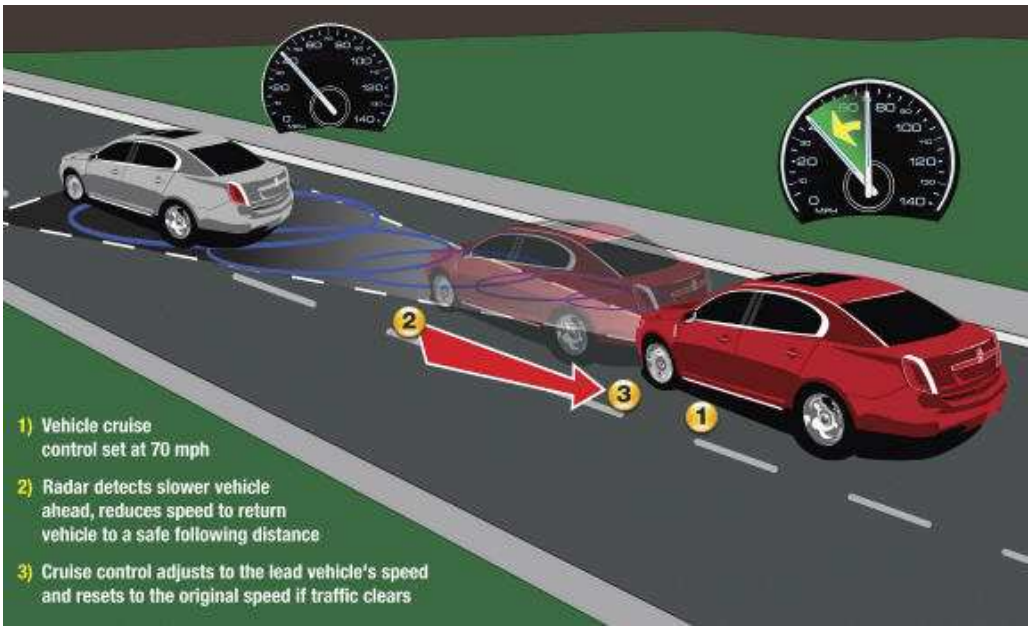

Figure 3.17: Schematic example of Adaptive Cruise Control (ACC) operation.

offer radar systems only for ACC systems so far, their Japanese competitors Honda and Toyota introduced an active brake assist for collision mitigation (in addition to ACC) based on 77 GHz Long-Range Radar (LRR) technology. In contrast to the only smooth deceleration capability of an ACC system (because ACC is only marketed as a comfort feature), the active brake assist provides much higher braking forces for deceleration, when a threatening situation is identified and the driver starts breaking but maybe not as strong as it would be necessary to avoid a crash. This shows the trend from "comfort only" functions to active safety systems with radar sensing technologies that serve both the comfort and the safety domain.
As a matter of fact, car companies and suppliers are currently working on the development of the next generations of LRR at 77 GHz that will show improvements with respect

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to maximum and minimum range, wider field of view, improved range and angular resolution and accuracy, self alignment, and blockage detection capability. In addition to forward-looking LRR, Ultra-Wideband (UWB) Short Range Radar (SRR) sensors with coverage up to 30 m are under development for a variety of further applications that will result in significant improvements of road safety.
Short range radar and Ultra-Wideband sensors can enable a variety of applications such as:

- Support of ACC with Stop and Go functionality
- Collision warning
- Collision mitigation
- Blind spot monitoring
- Parking aid
- Lane change assistant
- Rear crash collision warning

LRR and SRR devices can be used to combine their functionalities creating a protection wall all around the vehicle that is referred to in the literature as a "safety belt" for cars (Figure 3.18).

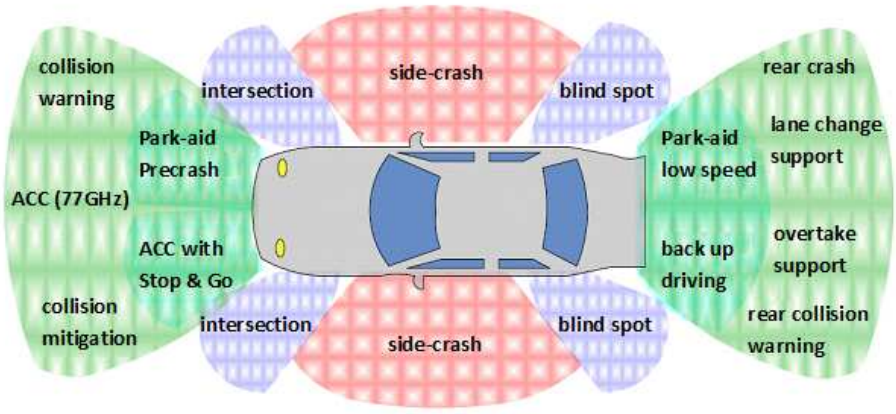

Figure 3.18: Possible applications for automotive radars.

Beside LRR and SRR systems, a complementary branch of potential applications of millimeter wave technology to the automotive industry is given by the next-generation road vehicle communication. Many companies are currently working on the implementation of millimeter wave sensors capable to support inter-vehicle (IVC) (Figure 3.19) and/or vehicle to roadside and roadside to vehicle (RVC) (Figure 3.20) communication.

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Next-generation cars will be able to exchange data - concerning, for example, their relative position or information and warning about weather and traffic status - with the surrounding vehicles and with beacons placed on the roadside at regular intervals along all inter-urban trunk routes and at strategic location (e.g. junctions) on more minor roads and in urban areas.
A huge number of applications of inter-vehicle and roadside to vehicle communication can be realized and are investigated by various project and groups; some examples are:

- Traffic information
- Collision avoidance
- Work zone safety warning
- Vehicle and cargo tracking
- Electronic license plate
- Repair-service record
- Parking, fuel, or fast food payment
- Disaster and emergency warning and control

More in general, IVC and RVC systems can be considered as part of a wider context, concerning the so-called Intelligent Transportation Systems (ITS) which represent the application of information and communications technology to transport infrastructure and vehicles, in an effort to manage factors that typically are at odds with each other, such as vehicles, loads, and routes to improve safety and reduce vehicle wear, transportation times, and fuel consumption.

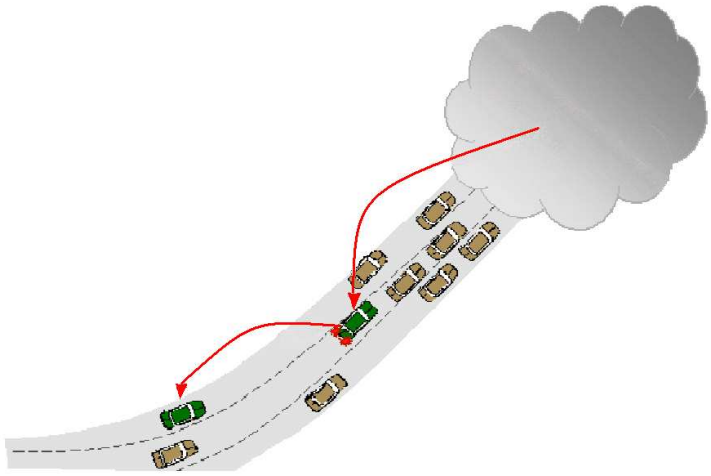

Figure 3.19: An example of IVC.

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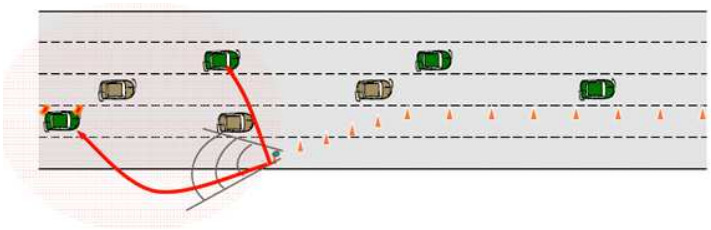

Figure 3.20: An example of RVC.

An exhaustive description of all the potential applications of millimeter wave to the automotive industry is beyond the aim of this thesis. Nevertheless, in conclusion of this brief overview, it is important to remark that the applications currently available, as the examples discussed here above, are substantially based on compound-semiconductors technologies. The considerably elevated cost of these technologies has therefore prevented the large diffusion of automotive radar equipments so far, relegating them to the high and mid-class market segments. Moreover, in the particular case of inter-vehicle communication, implementation cost is a concern, as it prevents an adequate diffusion of inter-communicating devices. Nowadays, thanks to the recent improvements in silicon-based technologies it is possible to realize low-cost and high-volume production of systems and circuits for automotive radar operating at millimeter wave frequencies [39].

3.3.3 Millimeter wave imaging in the 94 GHz band

The upper portion of the millimeter wave spectrum has been traditionally exploited for applications in the field of astronomy. Recently, further improvements of the related technology have turned the interest of industry on the development of terrestrial applications based on millimeter wave imaging [53, 54].
As a matter of fact, the property of millimeter wave imaging systems to see through materials that are opaque to more conventional imaging wavebands (visible, IR and UV) makes them remarkably useful for many scientific and industrial applications.
In particular, millimeter waves can readily penetrate common clothing materials and are reflected from the human body and any concealed items. For this reason they can be efficiently used in the field of security and defense, for the detection of concealed weapons or explosives. Furthermore, since millimeter wave imaging uses low-power and not-ionizing radiations, it results to be safer when compared to concurrent technologies based on X-rays and is better suited for the implementation of body scanner used for example for airport security screening. In such a context, it is possible to reveal not only weapons and explosives, but also any object hidden on the body, like drugs and contraband stuff. The personal scanner uses harmless coherent radar waves from a millimeter wave antenna array to illuminate the person under surveillance. Then the reflected signal from the body or from any object on the body is collected by the array and processed to form high-resolution three-dimensional images like that of Figure 3.21.

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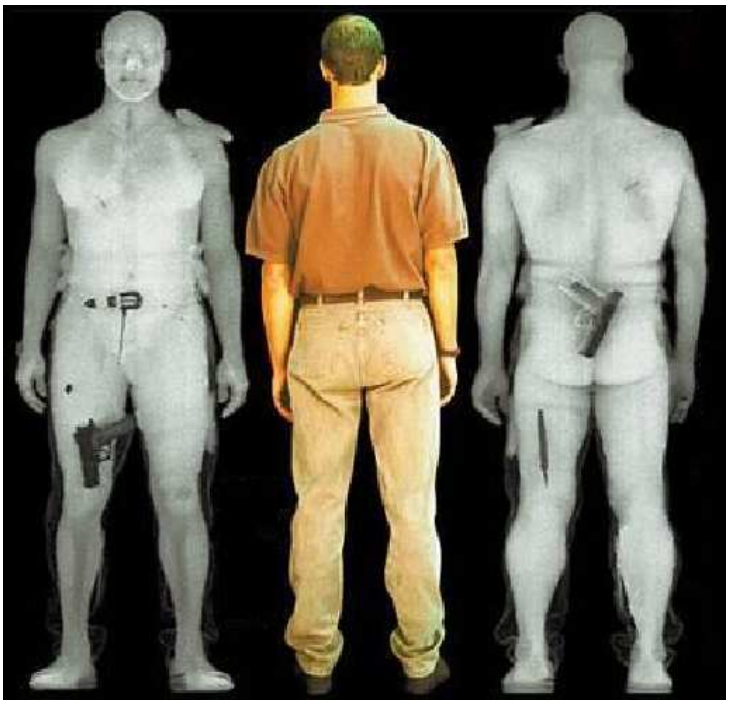

Figure 3.21: An example of body scanner operation based on millimeter waves.

Following a similar approach it is possible to realize many other applications of millimeter Wave as ground penetrating radar Ground Penetrating Radar (GPR) imaging, and wall probing systems like inner-wall imaging, through-wall imaging, through-concrete imaging.
Ground Penetrating Radar (GPR) (Figure 3.22) is a geophysical method that uses radar pulses to image the subsurface and detects the reflected signals from subsurface structures. GPR can be used in a variety of media, including rock, soil, ice, fresh water, pavements and structures. It can detect hidden objects, changes in material, and voids and cracks, without drilling, probing, or digging. The applications of GPR imaging cover a large number of fields as engineering, where it is used for non-destructive testing of structures and pavements, for example to map defects such as voids, moisture and cracking or to determine pavement type and thickness in the context of highway and airport runway inspection without traffic interruption; archeology, where it is used to map archeological structures and sites; military, for landmine detection; geophysical, for ground investigation in order to trace foundations and other obstructions, and to locate geological hazards that may pose a risk to construction activity or human habitation; or environmental protection, where GPR can be used to define landfills, contaminant plumes, and remediation sites.
Also wall probing systems can be useful for non-destructive structural test, to map buried utility cables, pipes and ducts or to measure the depth to buried utilities, so making

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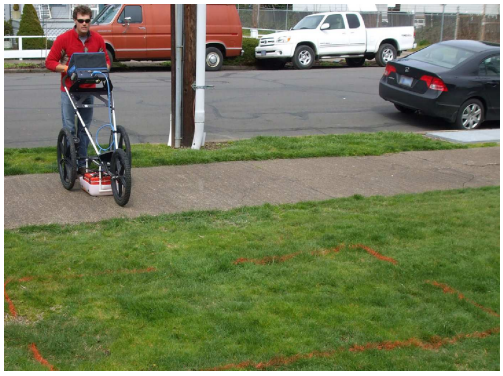
maintenance interventions simpler, reducing costs and the risk of accidental damage to power and gas lines.



(a) *Surface mapping of an underground storage tank.*

(b) *Roadway inspection.*

Figure 3.22: GPR apllications.

Many of the applications discussed so far are currently realized using concurrent technologies (like UWB in the range from 30 MHz to 12.4 GHz in the case of GPR). Nevertheless, all of them can be potentially supported by millimeter wave systems operating in the frequency range around 94 GHz.
The importance of 94 GHz band is given by the fact that the atmospheric absorption reaches a minimum level precisely at 94 GHz, as depicted in Figure 3.12. Besides imaging, millimeter wave technology can be applied also to the implementation of a Cloud Profiling Radar (CPR) employed in satellite missions to investigate cloud structure and its variability. By using the 94 GHz frequency range it is possible to penetrate ice clouds with negligible attenuation and obtain a profile of cloud characteristics.
Moreover, the capability of 94 GHz signals to propagate through fog, clouds, rain, and even sandstorms with irrelevant attenuation can be exploited to design millimeter wave sensor capable to improve the aviation safety and facilitate airport ground control in extremely poor visibility [39].

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3.4 mmW PLL state of the art

Advances in nanoscale CMOS technology have made it feasible to implement mmW Band circuits in CMOS for applications such as 60 GHz WPAN, 77 GHz anti-collision systems, 94 GHz imaging systems.

Due to the evolution of wireless communication, the transceivers operating at multi-gigahertz are required for the high-speed and broadband communications. In order to satisfy these increasing demands, the unlicensed millimeter band between 59 and 66 GHz is released for those applications. In the high-speed communication system, it is necessary for the clock generator to generate a very high frequency clock, such as 60 GHz.

In the recent years, several very high frequency clock generators have been realized in advanced CMOS technologies. However it is still a big challenge to implement the CMOS Phase-Locked Loop at millimeter Wave frequency while maintaining the sufficient performance to match the application requirements.

Table 3.8: State of the art of CMOS mmW PLLs close to 60 GHz.

Ref	Tech. [nm]	Frequency Range [GHz]	Divider Ratio	Voltage [V]	Power [mW]	P_{OUT} [dBm]	$\mathcal{L}$ [dBc/Hz]	Area [mm^2]
[55]	130	49.5 to 50.5	1024	1.5	57	-10	−72 @1 MHz	1.16x0.75
[56]	90	61.1 to 63.1	1024	1.2	78	-7	−80 @1 MHz	0.6x0.6
[57]	90	58 to 60.4	256/258	1.2	60	-	−85.1 @1 MHz	0.95x1
[58]	90	74.64 to 75.32	64	1.45	88	-16	−88 @1 MHz	0.8x1
[59]*	130	62 to 66.1	128	1.5	89	-	−74.5 @1 MHz	1.33x0.9
[60]	130	50.8 to 53	256	1.5	87	-	−107 @10 MHz	0.93x1
[61]*	90	59.6 to 64	256	1.2	26.3	-	−112 @10 MHz	0.93x1
[62]	65	95 to 96.5	256	1.2	47	-	−75 to −75.86 @1 MHz	1x0.7
[63]	65	70 to 78	1024-1984	1.0	65	-	−83 @1 MHz	0.16 (core)
[64]	45	57 to 66	512-8184	1.1	76	-	−75 @1 MHz	0.82
[65]	90	49.68 to 56.16	1840-2080	1.0	60	-	−80.1 @1 MHz	1.1
[66]	90	60.2 to 62.4	768	1.5	106.6	-	−93 @10 MHz	1.1

*VCO Push-Push

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To design such ultra-high-speed PLL implies a robust VCO together with properly arranged dividers, whose operation locking ranges need to be overlapped with each other. At such high frequencies, connecting blocks with perfect frequency alignment in a loop is much more challenging than making blocks individually. It is because any unexpected parasitic may cause significant frequency shift in the VCO or dividers, prohibiting the loop from lock.

Table 3.9: Frequency divider topology of CMOS PLL close to 60 GHz.

Ref	Tech. [nm]	Locking Range [GHz]	Divider Ratio	Divider Topology
[55]	130	49.5 to 50.5	1024	÷2 ILLCFD
				÷512 CML
[56]	90	61.1 to 63.1	1024	÷4 ILROFD
				÷16 CML
				÷16 CML
[57]	90	58 to 60.4	256/258	÷2 CML
				÷4/5 CML
				÷32 CML
[58]	90	74.64 to 75.32	64	÷2 ILLCFD
				÷4/5 MILLER
				÷32 CML
				÷32 CML
[59]*	130	62 to 66.1	128	÷2 ILLCFD
				÷8 CML
[60]	130	50.8 to 53	256	÷2 CML
				÷4/5 CML
				÷32 CML
[61]*	90	59.6 to 64	256	÷2 CML
				CML
				TSPC
				DFF
[62]	65	95 to 96.86	256	÷2 ILLCFD
				÷2 ILFD
				÷2 ILFD
				÷4 CML
				÷4 TSPC
[63]	65	70 to 78	1024-1984	÷2 ILLCFD
				CML
[64]	45	57 to 66	512-8184	÷4 ILLCFD
				÷2 CML
				÷64*to*1023 SCL
[65]	90	49.68 to 56.16	1840-2080	÷2ILLCFD
				÷8 CML
				÷5 DFF
				÷(23, 24, 25, 26) DFF
[66]	90	60.2 to 62.4	1840-2080	÷3ILLCFD
				÷3 ILROFD
				÷128 DFF

*VCO Push-Push

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Table 3.8 shows the state of the art of millimeter Wave Phase-Locked Loops in CMOS technology. The most utilized technology for the mmW PLL is the 90 nm [56, 57, 58, 61, 65, 66] following by the 130 nm in [55, 59, 60]. The literature also reported two PLL in 65 nm in [62, 63] and one synthetizer in 45 nm in [64]. A fractional PLL has been presented in [57, 63, 64, 65]. The voltage supply range is from 1.0 V to 1.5 V and the power consumption ranges from 26.6 mW to 106.6 mW.

The Table 3.9 shows in detail the composition of the division chain of the previously shows mmW PLLs. Focusing the attention on the first block of the division chain we can observe that in [55, 56, 58, 59, 62, 63, 64, 65, 66] the prescaler has been realized with an Injection-Locked (IL) Frequency Divider (FD) topology for the sake of its high frequency and low power characteristics. In particular [55, 58, 59, 62, 63, 64, 65, 66] utilize a divide-by-2 ILLCFD, composed by a LC oscillator working around half of the input frequency. This kind of FD uses one inductor, therefore occupies large area. For silicon save, a divide-by-4 inductorless IL Ring Oscillator Frequency Divider (ROFD) is proposed in [56]; the circuit is composed by a Ring Oscillator working around 15 GHz in free running condition, and locked at one-fourth of injected RF frequency. In [57, 60, 61] the prescaler is realized with a CML topology. A latch-type divider is reported in [57, 60], but it also uses several inductors, and consumes large area. In [61] an inductorless CML topology is presented, but the prescaler input signal is half than the PLL output frequency.

CML Frequency Divider is wider used in the following divider stage where the input frequency is lower [55, 56, 57, 59, 60, 61, 63, 64, 65]. Also in the second stage of the division chain [62, 66] utilize an IL topology, respectivelly ILROFD in [66] and ILLCFD in [62]. Finally a dual modulus divide-by-4/5 Miller divider is proposed in [60].

For the rest of the division chain, that works at low frequency, a D-Flip-Flop (DFF) FD and CML FD are widely used.

A negative resistance LC-tank (LC) Voltage Controlled Oscillator (VCO) is employed in [55, 56, 57, 58, 59, 62, 63, 64, 65, 66] for it high spectral purity and because its requires a minimal number of passive components, and thus low silicon area. A differential Colpitts oscillator topology has been adopted in [60, 61]. All cited VCOs work at the PLL output frequency except in [59, 61] where mmW output frequency is generated by VCO Push-Push topology.

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3.5 Frequency planning

In the present thesis, effort have been done on the design of a part of a millimeter Wave Phase-Locked Loop in CMOS 65 nm technology for Wireless Personal Area Networks. The following section shows the design of the circuits and how they works at high frequency:

1. 60 GHz Voltage Controlled Oscillator in the section 3.6
2. first stage of the division chain at 60 GHz (prescaler) in the section 3.7
3. second stage of the division chain at 30 GHz in the section 3.8

Table 3.10 reports the specifications of each block and the chosen topology. In particular the VCO should work from 57 GHz to 63 GHz to satisfied to the WPAN standard. The prescaler input frequency goes from 55 GHz to 65 GHz, with a minimum frequency margin between the output VCO frequency and prescaler (Injection-Locked LC-tank Frequency Divider) operation frequency in order to compensate eventual frequency shift. Same consideration hold for the prescaler and the second stage of the division chain (Injection-Locked Ring Oscillator Frequency Divider). In the present thesis a voltage supply of 1.2 V has been selected.

Table 3.10: Frequency planning.

block	Topology	Operation Frequency
VCO	LC VCO LC-tank Voltage Controlled Oscillator	57 GHz to 63 GHz
1 stage	ILLCFD Injection-Locked LC-tank Frequency Divider	55 GHz to 65 GHz
2 stage	ILROFD Injection-Locked Ring Oscillator Frequency Divider	25 GHz to 35 GHz

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3.6 60 GHz Voltage Controlled Oscillator

This section will present the VCO design that will be utilized in the 60 GHz proposed synthesizer. Among the LC-VCO topologies, the negative g_m topology is chosen for this design due to its simple structure and easily available differential outputs [55, 56, 57, 58, 59, 62, 63, 64, 65, 66]. The losses of the resonator in this topology are compensated by placing transistors in positive feedback (cross-coupled) which generates the required negative resistance to initiate oscillation.

3.6.1 Inversion mode MOS varactor

Figure 3.23 shows the cross section of an inversion mode N-MOS (I-MOS) variable capacitor. A Metal-Oxide-Semiconductor structure is opened on the P substrate, with two *N+*

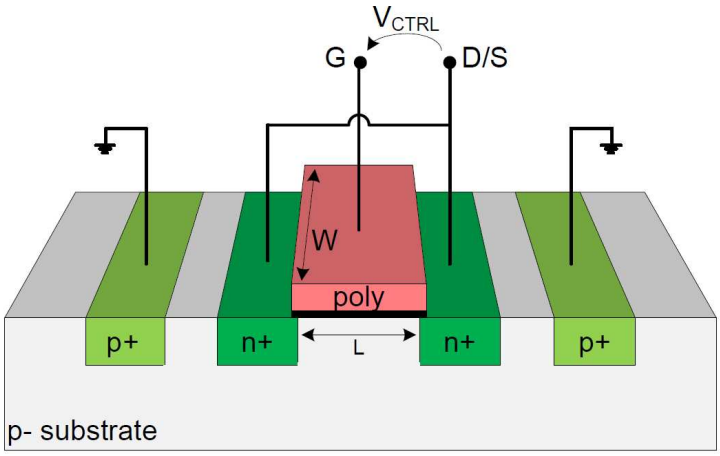

Figure 3.23: Cross section of I-MOS varactor.

diffusion providing the minority carriers when the surface layer is inverted. The contacts (D/S) to the *N+* diffusion are connected together and the capacitor is controlled by the voltage applied between the Gate and Drain/Source (V_{CTRL}) terminals.

An I-MOS VCO, employing N-MOS cross coupled pairs, allows a full exploitation of the C-V varactors characteristic keeping both the control terminals within the voltage range allowed by the technology.

The operation of the I-MOS varactor is as follows. Let us assume the gate voltage is the maximum available voltage, i.e. the supply voltage V_{DD}, and the bulk is connected to ground. When V_{CTRL} is equal to V_{DD} the channel is strongly inverted and the capacitance is mainly the oxide capacitance $C_{ox} \cdot W \cdot L$. The capacitance seen from the gate is hence given by the series of the gate oxide and the depletion oxide capacitances, the latter being smaller than the former. Note that, because the gate-bulk voltage is always positive, this configuration does not allow the device to operate in accumulation mode, resulting in a strictly monotonic C-V characteristic.

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However, this simple model does not take into account the overlap capacitance that, in modern CMOS technologies, is not a negligible fraction of the oxide capacitance. For minimum length device, the overlap capacitance is greater that the depletion one and represents the minimum varactor capacitance.

The main limit of the tank quality factor (Q_T) at mmW frequencies is the varactor quality factor Q_C. For this reason, maximizing Q_C is very important. The Gate resistance is proportional to the channel length L, the quality factor increases as $\frac{1}{L}$, therefore the quality factor is maximum with the minimum length device. Usually the device is made up of several wide finger in parallel, in order to reduce the gate resistance. On the other hand, the fixed parasitic capacitance takes more relevance by reducing the finger width, thus reducing the achievable tuning range. $W_F = 1\,\mu m$ has been chosen as a trade-off between varactor quality factor and tuning range [67].

Figure 3.24 shows the Q_C and $\frac{C_{max}}{C_{min}}$ ratio of a varactor of $W_{TOT} = 15\,\mu m$ simulated for several gate lengths at 60 GHz. The minimum Q_C largely decreases with increasing the gate length, while the tuning ratio increases. It is worth noticing that, in order to achieve a high Q_C at 60 GHz, a minimum length is mandatory. Figure 3.25 shows the simulated C-V and Q-V characteristics, for a varactor structure with 15 finger of 1 µm width and minimum length.

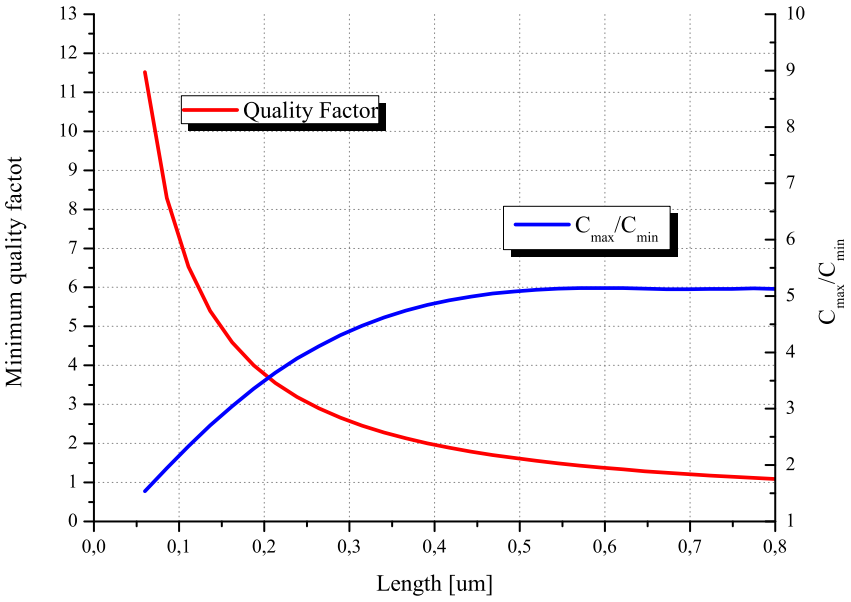

Figure 3.24: Varactor minimum quality factor and $\frac{C_{max}}{C_{mic}}$ versus transistor length

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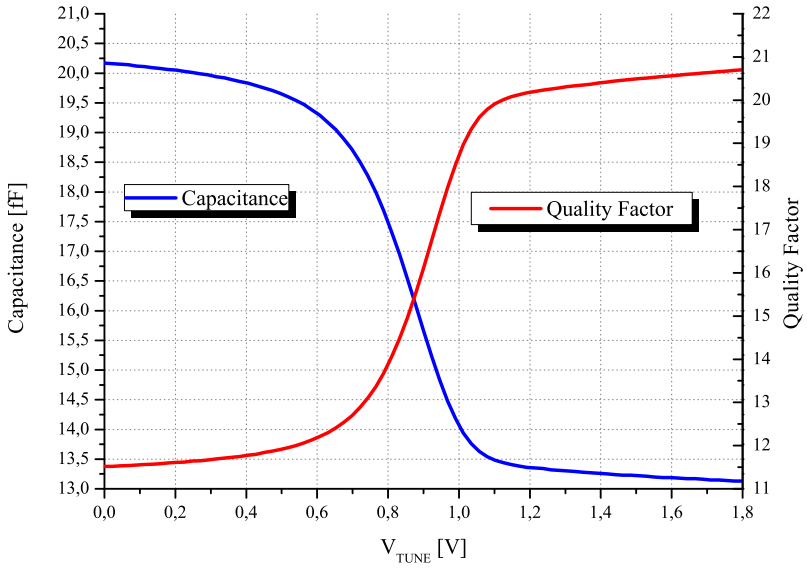

Figure 3.25: Varactor quality factor and capacitance versus V_{TUNE}.

3.6.2 Circuit design

Figure 3.26 shows the N-MOS cross-coupled pair VCO topology [68]. In order to maximize the frequency tuning range, tank capacitance should be maximized. As a consequence a small inductance would penalize the oscillation amplitude for a given bias current. To achieve a differential voltage amplitude of 700 mV the bias current must be set to 9 mA. Consequently, the following aspect ratio of the transistors $M_{2,3}$ has been chosen.

$$\left(\frac{W}{L}\right)_{2,3} = \left(\frac{12\,\mu m}{65\,nm}\right)_{2,3} \tag{3.32}$$

The transistors have been laid out with minimum length, with a $W_F = 1\,\mu m$ and double gate access, in order to find the best trade-off between the gate resistance and the fixed capacitance.

The varactor is composed with a parallel of ten I-MOS with a $W_{TOT} = 15\,\mu m$ and $W_F = 1\,\mu m$. The varactor was laid out in two sections: analog and digital. The analog section, controlled by a control voltage from 0 V to 1.8 V, is composed by a parallel of three I-MOS for reducing the parasitic series gate resistance in order to improve the varactor quality factor Q_C. The digital section, controlled by three bits line, is composed by seven I-MOS connected in parallel. The combination of analog and digital tuning varactors splits the frequency range of the VCO in several sub-bands. Each sub-band is activated by a circuit show in Figure 3.26; when the voltage on BIT terminals is equal to V_{DD} the circuit connect the drain/source terminals of the selected varactors to ground. Viceversa when the voltage on BIT terminals is equal to ground the the circuit connects

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the drain/source terminals of the selected varactors to V_{DD}. This approach allows a lower VCO gain in each sub-band, with benefits to supply noise rejection and minimization of AM to PM conversion, as a consequence. The required frequency tuning range is close

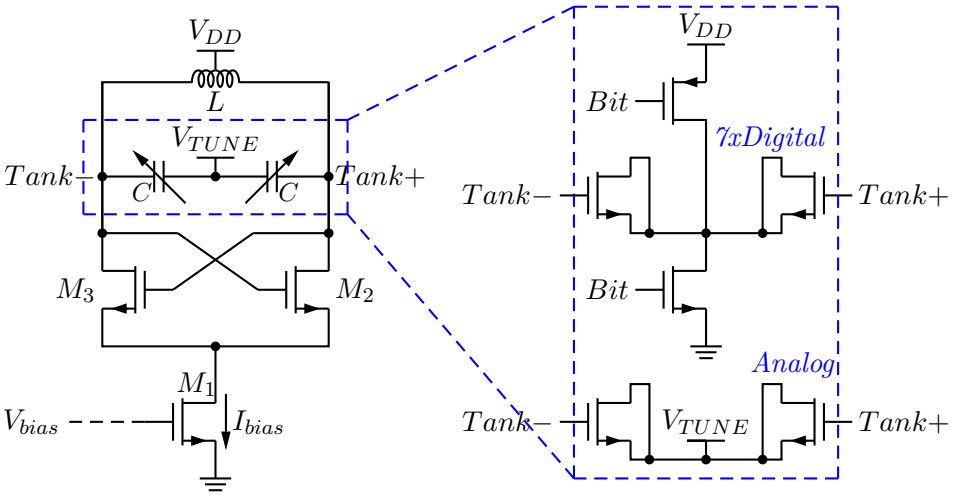

Figure 3.26: VCO schematic.

to 10 % with a central frequency of 60 GHz; the frequency range spans therefore from 57 GHz to 63 GHz. The fixed tank capacitance due to inductor, cross-coupled pairs and buffer parasitic plus maximum varactor capacitance is 150 fF; this value loads to 51 pH inductance for a 57 GHz oscillation frequency.

Figure 3.27 shows the designed inductor geometry. The inductor has been designed only in metal 7 and without shield. As in the other parts of the chip uses a ground plane, this one has been laid out in metal 1 and metal 2 only at 11 µm of distance from the inductor in order to reduce the coupling between the inductor and the ground plane. Figure 3.28 shows the inductance and its quality factor simulated with the HFSS

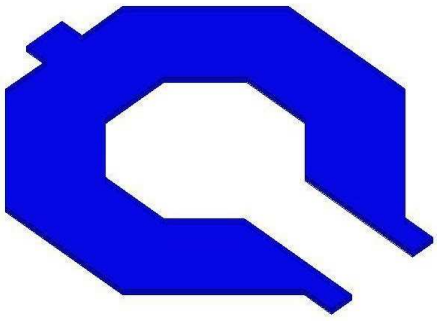

Figure 3.27: Inductor geometry.

electromagnetic simulator. Near 60 GHz the inductance value is close to 50 pH and the quality factor is close to 17.

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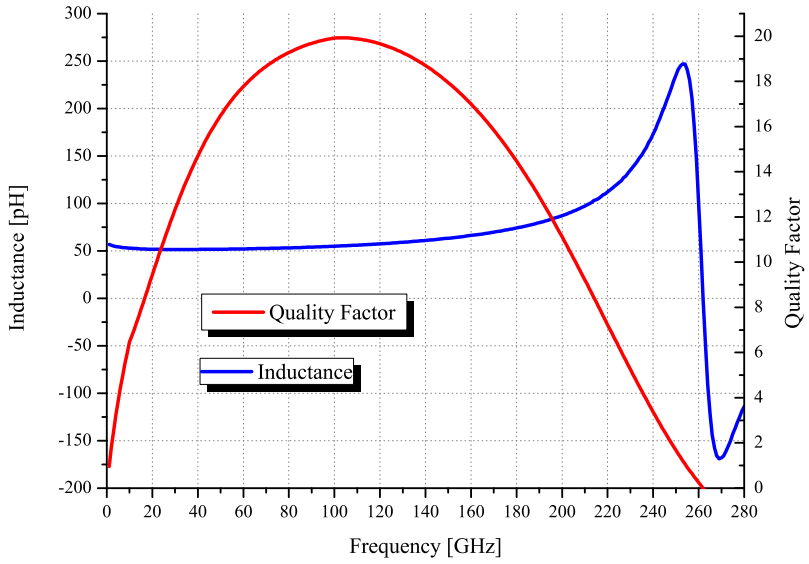

Figure 3.28: Inductance and quality factor versus frequency.

A differential lumped equivalent 2π model (seen in Figure 3.29) has been extracted, in order to integrate the inductor into spectre simulations.

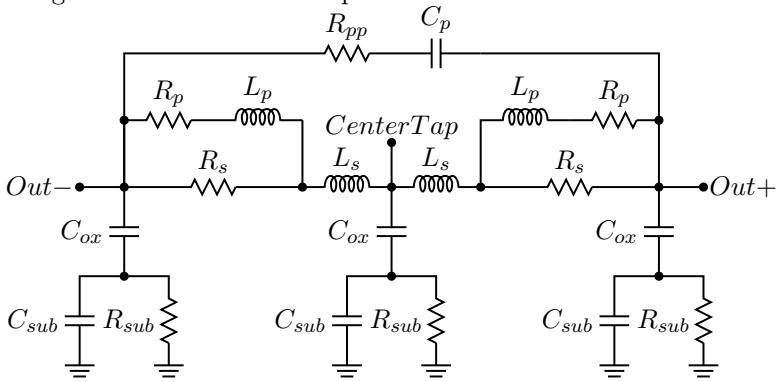

Figure 3.29: 2π differential lumped model.

The total tank quality factor which is equal to the inductor quality factor in parallel with the minimum varactor quality factor (Eq: 2.9) gives a value close to 7 for the total tank quality factor.

The circuit of the VCO has been laid out very compact and carefully in order to minimize the connection lengths between the devices. In this way the HFSS electromagnetic simulations of parasitic inductances were not necessary. The parasitic capacitances were extracted with STAR-RCXT.

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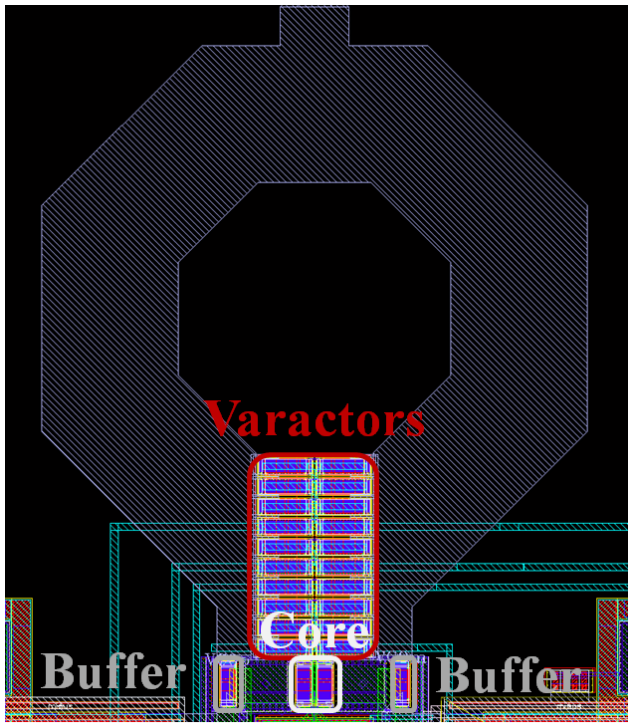
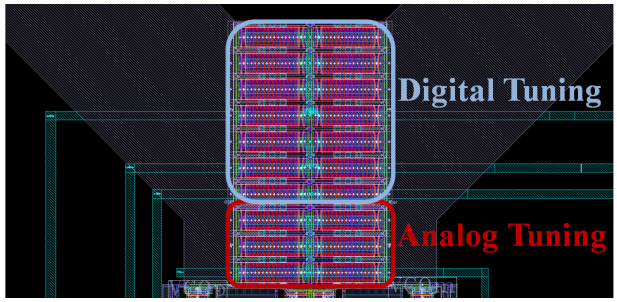
3.6.3 Layout

Figure 3.30a shows the layout of the designed VCO. The varactors are placed inside the inductor accesses and very close to the cross coupled pair. Also the buffers are laid out near the inductor accesses in order to minimize the metal interconnections. Figure 3.30b shows in detail the varactors structure described in the previous section 3.6.2. We can observe the analog tuning composed by three I-MOS and the digital tuning composed by seven I-MOS.



(a) *VCO Layout.*



(b) *Varactors layout.*

Figure 3.30: VCO layout.

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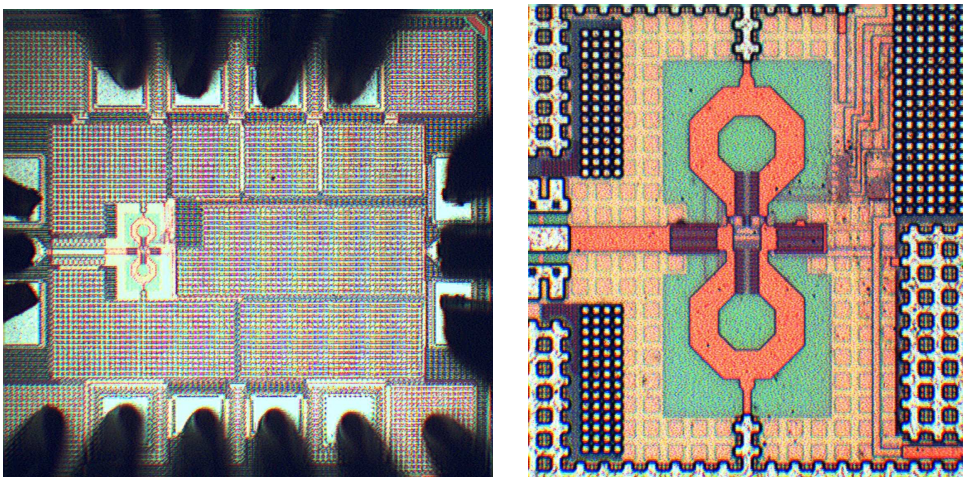
3.6.4 Measurements results

Figure 3.31a shows the photomicrograph of the prototype implemented in the 65 nm CMOS technology from STMicroelectronics. The circuit was integrated with differential buffers loaded with the same tank VCO. One output has been connected to a single-ended GSG pad for the measurements and the other was connected to a 50 Ω resistance for sake of load symmetry. The chip size is $910 \cdot 850\,\mu m^2$ including pads and the core of the circuit Figure 3.31b is $150 \cdot 80\,\mu m^2$.



(a) *microphotograph.* (b) *core.*

Figure 3.31: VCO microphotograph.

Figure 3.32 shows the measured and simulated circuit tuning range. The measured carrier frequency (f_0) goes from 71.87 GHz to 81.44 GHz for V_{TUNE} ranging between 0 V and 1.8 V corresponding to a tuning range of 12.4 %.

The STAR-RCXT extracted simulation carrier frequency (f_0) goes from 56.85 GHz to 63.72 GHz corresponding to a tuning range of 11.4 %. As stated above, the VCO was designed using the STAR-RCXT tool for the extraction of the parasitic capacitances. Figure 3.32 shows that the STAR-RCXT extraction simulated carrier frequency is as required by the spec's.

The comparison with the measurements demonstrates that the STAR-RCXT simulations provide an overestimation of the parasitic capacitances; the real parasitic capacitances in the fabricated prototype are lower then forecasted by STAR-RCXT, resulting, therefore, in a higher center frequency and a wider tuning range. In order to depth investigate this issue, a further parasitic capacitances extraction has been carried out using the PEX tool of Calibre. Figure 3.32 shows that for PEX extracted simulations the carrier frequency (f_0) goes from 63.30 GHz to 71.5 GHz corresponding to a tuning range of 12.3 %. The Calibre forecast is closer to the experimental results, giving further evidence of the fact that STAR-RCXT suffers from an overestimation of the parasitic

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capacitances.

Nevertheless, even Calibre is not able to reproduce the measured center frequency and tuning range. The sketched general frame suggests that electromagnetic simulations are needed for a more accurate estimation of the parasitic capacitances.

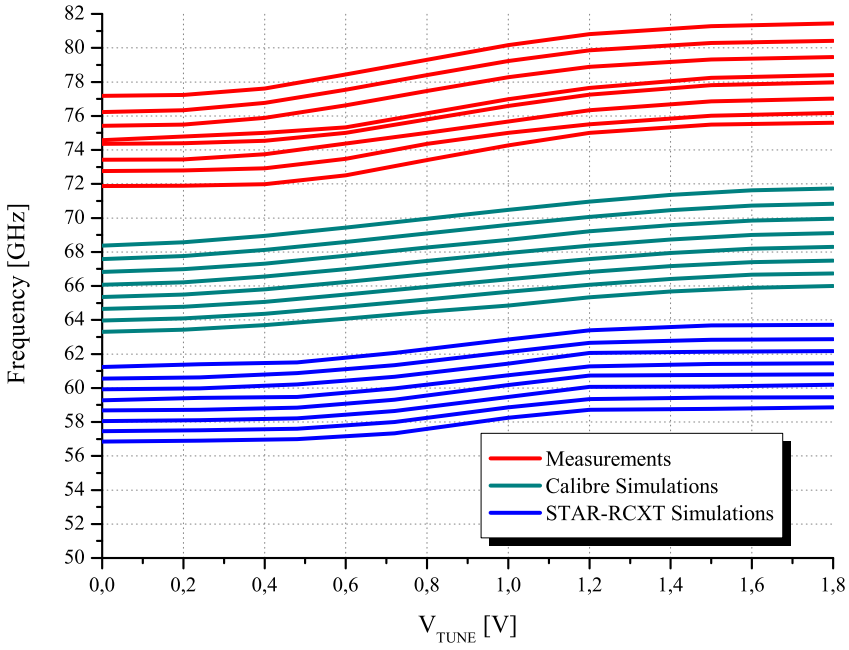

Figure 3.32: VCO voltage tuning range.

The circuit core power consumption is 15.6 mW for a voltage supply of 1.2 V. The measured sinked current of 13 mA is higher than the simulated one of 9 mA. This increase is due to the fact that the fabricated oscillator works at a higher frequency than the simulated one. Figure 3.33 shows the measured phase noise for f_0=71.8 GHz. The VCO exhibits a phase noise of −116 dBc/Hz at the offset frequency (Δf) of 10 MHz. The FOM is −181.2 dBc/Hz and FOM$_T$ is −183.1 dBc/Hz at the same offset frequency.

Figure 3.34 shows the measured output spectrum with a 500 MHz span.

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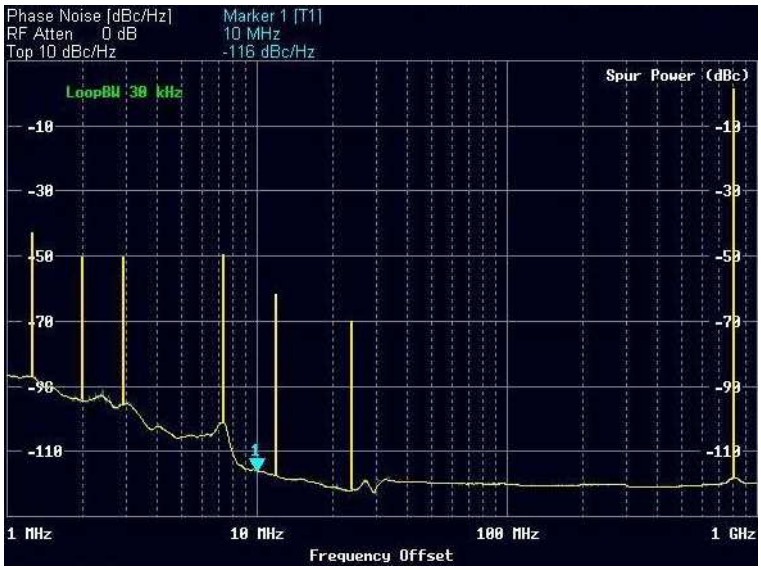

Figure 3.33: VCO phase noise.

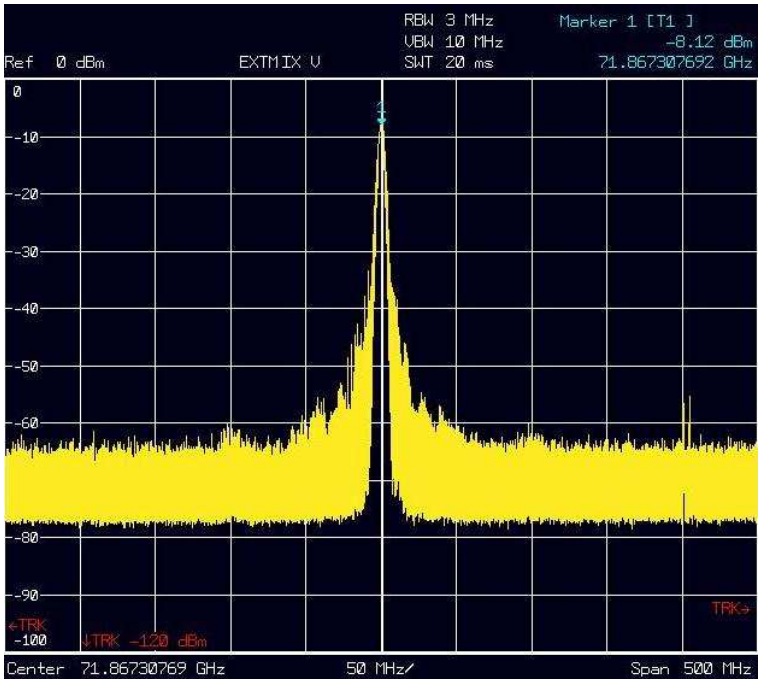

Figure 3.34: VCO output spectrum.

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Table 3.11 compares the designed VCO with the state of the art of VCO designed at mmW frequency. In conclusion a 65 nm CMOS VCO exhibiting a central frequency

Table 3.11: State of the art of CMOS mmW Voltage Controlled Oscillators.

Ref.	Pub.	Tech. [nm]	f_0 [GHz]	TR [%]	Voltage [V]	P_{DIS} [mW]	$\mathcal{L}$ [dBc/Hz]	FOM [dBc/Hz]	FOM_T [dBc/Hz]
[69]	ISSCC2006	130	59	5.8	1.5	9.8	-89 @1 MHz	−174.5	−169.8
[70]	JSSC2006	90	60	0.2	1.0	1.9	-100 @1 MHz	−192.8	−158.8
[68]	RFIC2008	65	54	11.4	1.2	7.2	-118 @10 MHz	−184.1	−185.2
[71]	RFIC2008	130	62.1	9.9	1	3.9	-91 @1 MHz	−180.5	−180.7
			59.1	10.3	1	3.9	-95 @1 MHz	−185.0	−184.9
[72]	MWCL2008	130	69.8	4.5	0.6	4.3	-98.8 @1 MHz	−189.3	−182.5
			69.8	4.5	0.6	4.3	-115.5 @1 MHz	−186.0	−179.2
[73]	EuMIC 2009	65	60.29	9.3	1.2	36	-95.3 @1 MHz	−174.9	−174.3
[74]	TMTT2011	90	64	9.9	0.6	3.2	-95 @1 MHz	−186.1	−184.9
[75]	TMTT2011	65	56	16.9	1.2	15	-99 @1 MHz	−182.2	−186.8
[76]	SiRF2011	90	58.4	4.3	1.2	55	-106.2 @1 MHz	−184.1	−176.7
THIS	WORK	65	77	12.4	1.2	15.6	-116 @10 MHz	−181.3	−183.1

of 77 GHz has been designed. The phase-noise-related FOM is well aligned with other CMOS bulk VCOs reported in the literature, in particular for mmW applications.

Unfortunately the VCO was designed to work around 60 GHz for WPAN standard. The circuit exhibits a good performance for the automotive radar standard. The redesign of inductor is needed to restore the central frequency at 60 GHz.

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3.7 Divided by 2 LC prescaler

For very high frequency applications the Injection Locking Frequency Divider (ILFD) is a widely used solution [55, 56, 58, 59, 62, 63, 64, 65, 66]. To accommodate the severe tradeoffs between the input frequency and the operation range, different types of dividers can be employed. Generally speaking, the ILFD achieves the highest operation frequency due to the simplest structure, but with the narrowest locking range.

3.7.1 Circuit Design

The first stage is realized as a simple LC-tank structure, where the biasing is established by a current mirror and the cross-coupled pair gives a negative resistance to compensate the tank losses (Figure 3.35). In this case, the input signal is directly applied to the gate of the NMOS current mirror transistor.

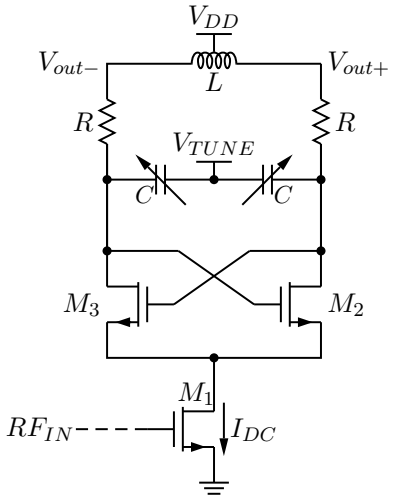

Figure 3.35: Injection-Locked Frequency Divider schematic.

The LC-tank works at half frequency of the signal input. For this FD topology, the locking range is set to (Eq:3.33)[77]:

$$\mathrm{LR} \approx \frac{2f_0}{3Q_T}\frac{I_{INJ}}{I_{DC}} \tag{3.33}$$

where f_0 is the center frequency, Q_T is the total tank quality factor, I_{DC} is the DC current, and I_{INJ} is the injection current. We can observe that the locking range is directly proportional to the injection current. For this reason, an optimum matching between VCO and ILLCFD is needed to maximize the current injection. Furthermore the amplitude of the output voltage oscillation is directly proportional to the tank quality factor. In the locking bandwidth, the oscillation amplitude is given by (Eq:3.34)[77]:

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$$V_{out} = Z_{out}\frac{4}{\pi}I_{DC}\left[1 + \frac{I_{INJ}}{3I_{DC}}\cos(2\phi)\right] \tag{3.34}$$

where $Z_{out} = 2\pi f_0 Q_T L$ and ϕ is the phase shift between the input and the output signals. The tank quality factor has been reduced from 12 to 2 (Figure 3.36) with two identical series resistors [78], connected between the tank and the cross-coupled pair, in order to improve the locking range.

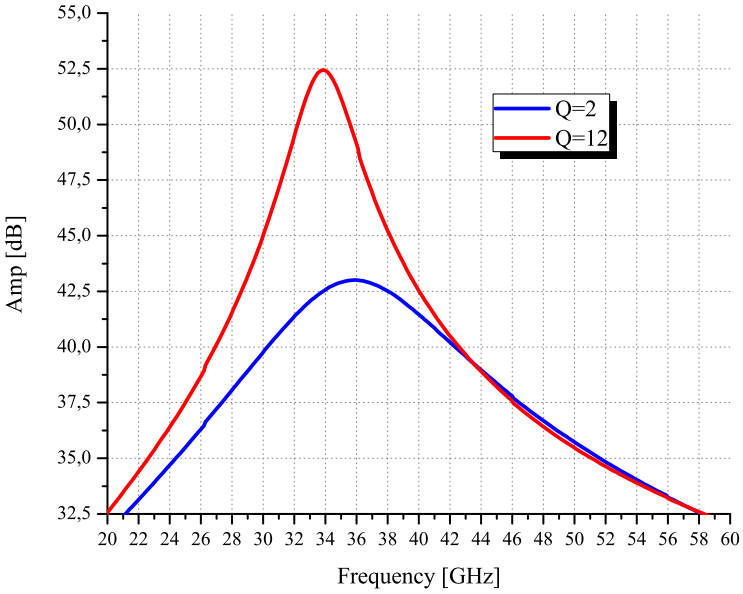

Figure 3.36: Tank quality factor for V_{TUNE} 0 V.

A trade-off exists therefore between the locking range and the output voltage signal amplitude. A careful layout has been done, in order to reduce as much as possible the capacitive parasitics. As a consequence the inductance value is large enough to generate the needed amplitude voltage to drive the second stage of the division chain without buffering. The required output voltage set the DC current to 3 mA. The aspect ratio of the transistors M_2 and M_3 is chosen to provide a small signal loop gain higher or equal to one and half (Eq:3.35), to fullfill the self oscillation start-up condition:

$$|g_{m_c}| = \frac{g_{m_{2,3}}}{2} = \frac{1}{R_{peq}} \geq 1.5 \tag{3.35}$$

where g_{m_c} is the small signal differential transconductance of the circuit, $g_{m_{2,3}}$ is the transconducance of the transistor $M_{2,3}$ and R_{peq} is the total differential resistance across the LC tank. To minimize the capacitance associated to the transistors and to achieve the highest transconductance, the minimum gate length is required. The transistor ratio is therefore set to:

$$\left(\frac{W}{L}\right)_{2,3} = \left(\frac{30\,\mu m}{65\,nm}\right)_{2,3} \tag{3.36}$$

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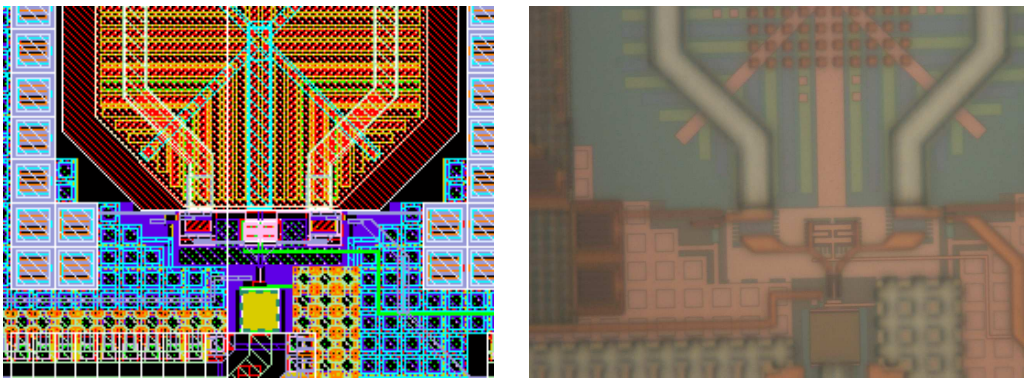
The tail transistor M_1 has been designed, even in this case, with the minimum length for the maximum transconductance. The width has been chosen, in order to find an optimum value of input impedance and a higher injection efficiency. The biasing voltage is $V_{GS} = 0.3\,\mathrm{V} \approx V_{TH}$.

$$\left(\frac{W}{L}\right)_1 = \left(\frac{50\,\mu\mathrm{m}}{65\,\mathrm{nm}}\right)_1 \tag{3.37}$$

The RF MOS transistor must be designed with short fingers to be functional at millimeter wave frequencies. Indeed, the gate serial resistance is responsible for the degradation of f_{max}. Our transistor exhibits a finger width (W_F) ranging from 1 µm to 2 µm to keep high performances at 60 GHz and to have a trade-off between the transistors performances and a compact layout, in order to reduce as much as possible the connections between the current mirror and the differential cross-coupled pair. In addition, the increase of the gate resistance of the cross-coupled differential pair helps to decrease the total tank quality factor (Eq: 3.33).

During the design, Process-Voltage-Temperature (PVT) variations have also been taken into account as follows: a ±10% variation of the supply voltage $V_{DD} = 1.2\,\mathrm{V}$ and an operating temperature range between −40 °C and 125 °C. To compensate for the frequency shift, a varactor was added in parallel to tune the FD free running frequency. The layout of the tank connections have been made in top metal with a minimum width in accordance with the maximum current allowed in the Design Rules Manual (DRM). For this reason, the tank connections are very tiny and consequently very inductive and



(a) *Layout.* (b) *Microphotograph.*

Figure 3.37: Injection-Locked LC-tank Frequency Divider tank.

resistive. The parasitic capacitances have been extracted with Star-RCXT. This tool is not able to extract the parasitic inductances and the extracted resistances are not accurate. Therefore, 3D electromagnetic simulations have been carried out with the Ansoft HFSS electromagnetic simulator, in order to precisely control the tank resonance frequency and quality factor. Each connection brings 5 pH and 2 Ω of parasitic inductance and resistance at the circuit output node. This value of resistance includes the

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transistor accesses, the metal lines, and the resistance accesses. To achieve a total tank quality factor of two the value of the resistance must be equal to 10 Ω. Therefore the chosen value is set to 8 Ω. Even if the tank circuit does not work at mmW frequency, the contribution of the parasitic inductances is not negligible. Figure 3.38 shows the impact of the tank parasitic inductances in the FD free running frequency. For sake of mea-

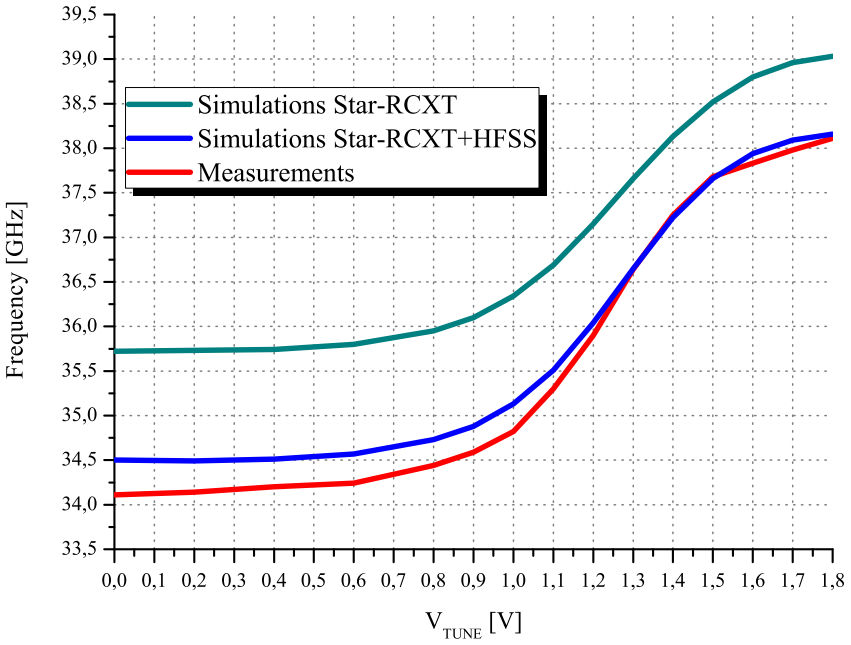

Figure 3.38: Injection-Locked LC-tank Frequency Divider free running frequency.

surements, the test chip has been designed to operate around 70 GHz; as a consequence, the free running frequency of the FD is close to 36 GHz. The total fixed capacitance for inductor, cross-coupled pair and buffer plus the minimum varactor capacitance is 90 fF. In order to set the center frequency around 36 GHz, a 230 pH octagonal one turn coil differential inductance has been selected. The inductance value keeps into account the parasitic inductances extracted through electromagnetic simulations.

3.7.2 Measurement Results

Figure 3.39 shows the photomicrograph of the prototype implemented in the 65 nm CMOS technology from STMicroelectronics. The circuit was integrated with two common drain buffers. One output has been connected to single-ended GSG pad for the measurements and the other is connected to a 50 Ω resistance for sake of load symmetry. The chip size is $650 \cdot 700\,\mu m^2$ including pads. The ILLCFD consumes 3.6 mW from a 1.2 V supply, excluding buffers. Figure 3.38 shows the simulated and the measured free running frequency of the circuit with a control voltage ranging between 0 V

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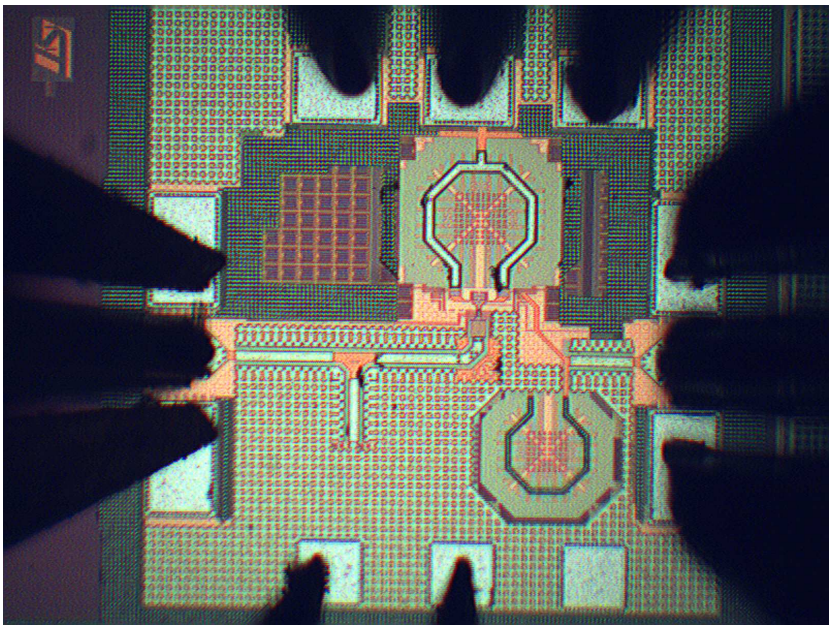

Figure 3.39: Injection-Locked LC-tank Frequency Divider Photomicrograph.

and 1.8 V. The Star-RCXT postlayout simulated free running frequency goes from 35.72 GHz to 39.03 GHz, the Star-RCXT+HFSS postlayout simulated free running frequency goes from 34.50 GHz to 38.16 GHz, and the measured free running frequency goes from 34.11 GHz to 38.11 GHz. The maximum frequency difference between Star-RCXT simulations and measurements is equal to 1.61 GHz for a control voltage of 0 V with a relative error of 4.51 %. The introduction of the electromagnetic simulation carried out by HFSS reduces the maximum frequency variation from 1.61 GHz to 0.39 GHz and the maximum relative error from 4.51 % to 1.14 % and provides a very good agreement between simulations and measurements.

Table 3.12: LC Frequency Divider free running frequency.

	f_{min} [GHz]	f_{max} [GHz]	Δf_{max} [GHz]	ϵ [%]
Star-RCXT	35.72	39.03	1.61	4.51
Star-RCXT+HFSS	34.50	38.16	0.39	1.14
Measurements	34.11	38.11	-	-

Table 3.13 summarized the measured and simulated locking range (Eq:3.38, Eq:3.39)

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for a control voltage of 0 V, 1 V, 1.2 V, 1.5 V and 1.8 V.

$$\mathrm{LR}_{[\mathrm{GHz}]} = f_{max} - f_{min} \tag{3.38}$$

$$\mathrm{LR}_{[\%]} = 2 \cdot \frac{f_{max} - f_{min}}{f_{max} + f_{min}} \cdot 100 \tag{3.39}$$

With 0 dBm input power and V_{DD}=1.2 V, the proposed ILLCFD Locking Range, in the best case, is 10.5 GHz (65.3 GHz to 75.8 GHz) or 14.88 % of the center frequency. The total measured Locking Range of the circuit is 15.7 GHz (63.5 GHz to 79.2 GHz) or 22.00 % of the center frequency. Even in this case, we can observe a very good agreement between simulations and measurements.

Table 3.13: LC Frequency Divider Locking Range

(a) *Simulations.*

V_{TUNE} [V]	f_{min} [GHz]	f_{max} [GHz]	LR [GHz]	LR [%]
0	63.2	73.0	9.8	14.39
1.0	64.0	74.5	10.5	15.16
1.2	65.3	76	10.7	15.15
1.5	67.5	77.7	10.2	14.05
1.8	68.9	78.5	9.6	13.03
TOT	63.2	78.5	15.3	21.59

(b) *Measurements.*

V_{TUNE} [V]	f_{min} [GHz]	f_{max} [GHz]	LR [GHz]	LR [%]
0	63.5	72.3	8.8	12.96
1.0	64.5	74.0	9.5	13.72
1.2	65.3	75.8	10.5	14.88
1.5	68.5	78.4	9.9	13.48
1.8	69.2	79.2	10.0	13.48
TOT	63.5	79.2	15.7	22.00

Figure 3.40 shows the input sensitivity of the Frequency Divider for several values of control voltage.

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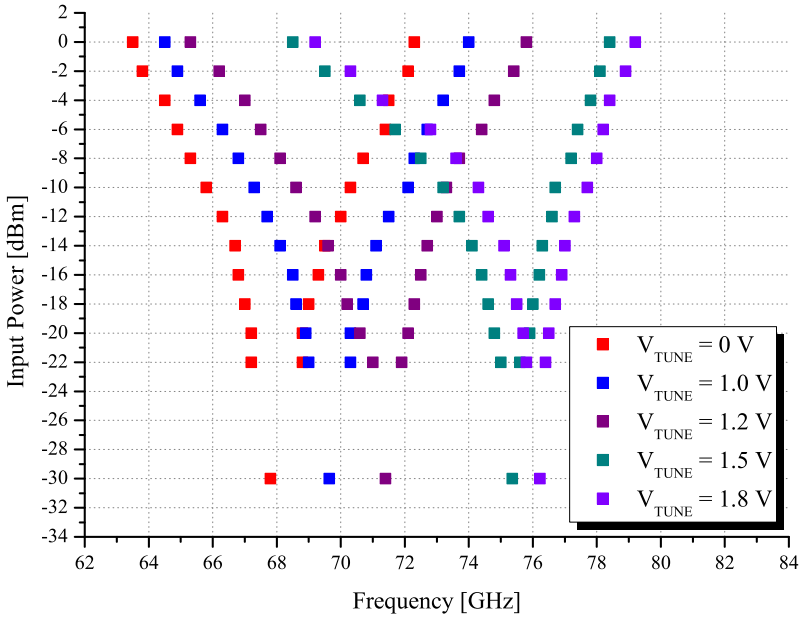
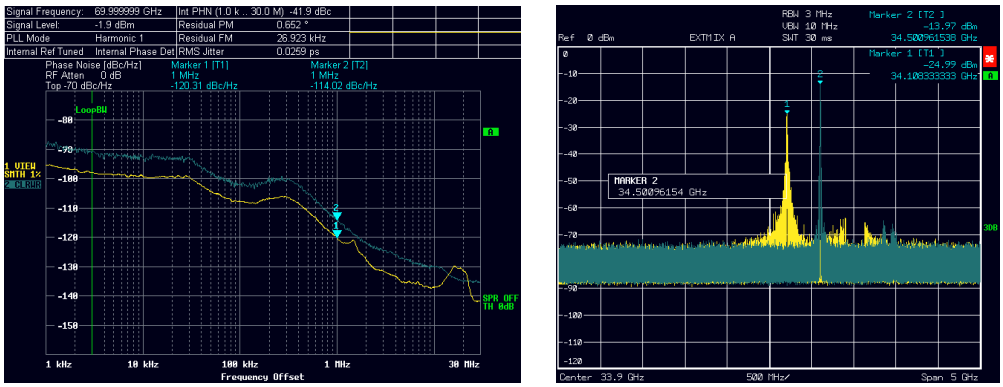


Figure 3.40: Injection-Locked LC-tank Frequency Divider sensibility.



(a) *Phase Noise.* (b) *Output spectrum.*

Figure 3.41: LC Frequency Divider measurements.

Figure 3.41a shows the Frequency Divider phase noise measurement compared with the phase noise of input signal source. The phase noise of the Frequency Divider is 6 dB lower than the phase noise of the source, suggesting that the circuit does not contribute significantly to the total phase noise. The Figure 3.41b shows the output spectrum in free running mode close 34 GHz and the output signal at 34.5 GHz with an input signal

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of 0 dBm at 69 GHz.

A comparison with the state of art Injection-Locked LC-tank Frequency Divider has been reported in the following Table 3.14 using the following Figure Of Merit:

$$FOM = \frac{\mathrm{LR}_{[\mathrm{GHz}]}}{P_{DIS}} \tag{3.40}$$

Table 3.14: State of the art of CMOS mmW Injection Locking Frequency Dividers.

Ref.	Tech. [nm]	LRf [GHz]	LR [%]	Input Power [dBm]	Voltage [V]	Power [mW]	FOM [GHz/mW]
[79]	90	85.2 to 96.2	12.13	0	1.2	3.5	3.14
[79]	90	99 to 105	5.88	0	1.2	3.3	1.82
[80]	65	81.5 to 85.9	5.1	0	1.55	12	0.36
[81]	65	93.5 to 109.1	15.3	0	1.1	5.5	2.84
[82]	65	48.5 to 62.9	25.9	0	1.2	1.65	8.72
[83]	65	82 to 94	13.6	0	0.56	3.92	3.06
[84]	65	104 to 112.8	8.14	< -5	1.2	7.2	1.22
[85]	65	128.24 to 137	6.6	0	1.1	5.5	1.59
[86]	65	132.7 to 142.5	6.6	< -4	1.1	5.28	1.85
[87]	130	66.4 to 76	13.6	4	1	4	2.4
[88]	90	51 to 74	36.8	0	0.5	3	7.6
[89]	65	158 to 195	20.96	0	1	2.5	14.8
[90]	130	59.6 to 67	11.69	0	0.8	1.6	4.63
[91]	90	52.7 to 64.8	20.60	0	1.2	8.6	1.41
THIS WORK	65	63.5 to 79.2	22.00	0	1.2	3.6	4.36

The circuit is well aligned with other CMOS bulk Injection-Locked LC-tank Frequency Divider reported in the literature. In particular for the PLL the inductor resizing is needed to restore the central frequency to 60 GHz.

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3.8 Divided-by-2 Injection-Locked Ring Oscillator Frequency Divider

For the second stage of the division chain we select a divide-by-2 inductor-less Injection-Locked Ring Oscillator Frequency Divider (ILROFD). Figure 3.42 shows the circuit block diagram of the circuit. The ILROFD is composed of four-stage series connected with resistive load, which is another candidate to avoid inductors or active load; because in our process, the parasitic capacitance of the PMOS is larger than the resistances parasitic capacitances. For a ring oscillator, large parasitic capacitances cause high current consumption to oscillate at the same oscillation frequency. So we select resistive load in this design.

To guarantee the same impedance at the output of each amplifier stage another amplifier stage was connected as output buffer.

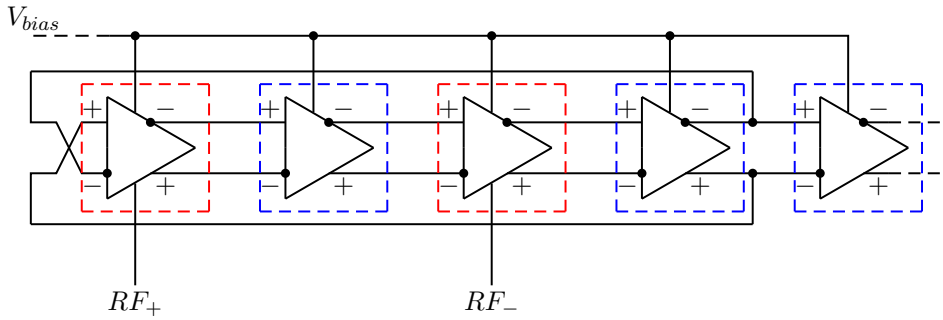
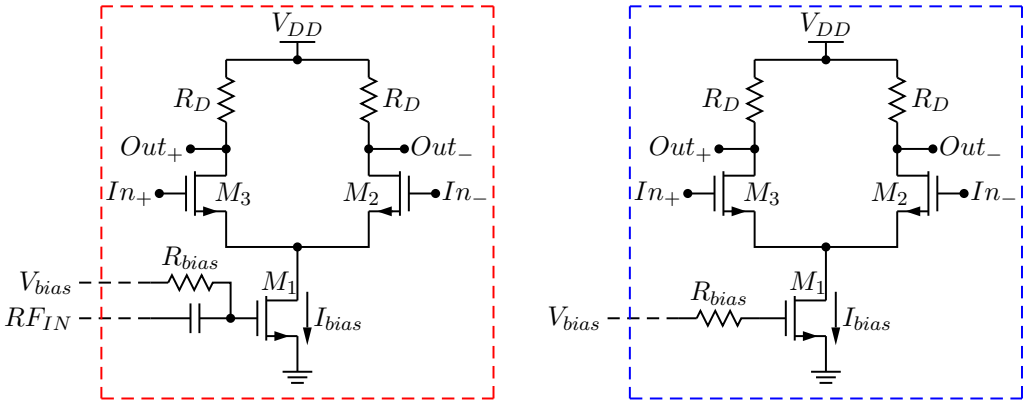


Figure 3.42: IL Ring Oscillator Frequency Divider block diagram.



(a) *Differential pair with injection signal.* (b) *Differential pair and output buffer.*

Figure 3.43: Differential amplifier schematics.

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3.8.1 Circuit design

The closed loop transfer function of Ring Oscillator show in the Figure 3.42 is:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \tag{3.41}$$

The transfer function of each stage is given by: $-\frac{A_0}{1+\left(\frac{s}{\omega_0}\right)}$, we have for the loop gain:

$$H(s) = \frac{{A_0}^4}{\left(1 + \frac{s}{\omega_0}\right)^4} \tag{3.42}$$

The circuit oscillates only if the frequency-dependent phase shift equal to 180° therefore each stage contributes 45°. The frequency at which this occurs is given by

$$\arctan\left(\frac{\omega_{osc}}{\omega_0}\right) = 45^\circ \tag{3.43}$$

and hence:

$$\omega_{osc} = \omega_0 \tag{3.44}$$

The minimum voltage gain per stage must be such that the magnitude of the loop gain at ω_{osc} is equal to unity:

$$\frac{A_0}{\sqrt{1 + \left(\frac{\omega_{osc}}{\omega_0}\right)^2}} = 1 \tag{3.45}$$

$$A_0 = \sqrt{2} \tag{3.46}$$

The voltage gain for the schematic show in Figure 3.43b at the first order is given by:

$$A_0 \approx g_{m2,3} R_D \tag{3.47}$$

$$g_{m2,3} \approx \sqrt{2\mu_n C_{ox} \frac{W_{2,3}}{L_{2,3}} I_{bias}} \tag{3.48}$$

Combining Eq 3.47 and Eq 3.48 we obtain:

$$A_0 \approx \sqrt{2\mu_n C_{ox} \frac{W_{2,3}}{L_{2,3}} I_{bias}}\, R_D \tag{3.49}$$

For a given technology μ_n, C_{ox} are fixed. Eq 3.46 shows that needed gain for the oscillation start-up (Eq 3.48), at the first order, only depends of R_D, $W_{2,3}$, $L_{2,3}$ and I_{bias} .

$$R_D = 600\,\Omega \tag{3.50}$$

$$\left(\frac{W}{L}\right)_{2,3} = \left(\frac{10\,\mu\text{m}}{65\,\text{nm}}\right)_{2,3} \tag{3.51}$$

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$$I_{bias} \approx 670\,\mu A \tag{3.52}$$

Eq 3.50, Eq 3.51 and Eq 3.52 show the chosen resistor load, transistors size and bias current in order to fix the frequency of the designed RO (Figure 3.42) around 15 GHz and to have a best trade-off between output node capacitance and current consumption. To keep high performance with minimum current consumption, and to reduce the transistor capacitance minimum length is required for the differential couple transistors. The bias voltage is directly connected to gate of the transistor M_1.

$$\left(\frac{W}{L}\right)_1 = \left(\frac{4\,\mu m}{65\,nm}\right)_1 \tag{3.53}$$

The differential output signal given by the ILLCFD is directly injected on the gate of transistor M_1 of the odd stage amplifier (Figure 3.43a). Even in this case for high injection efficiency a minimum transistors length is mandatory.

The double injection increases the divider Locking Range [92] and provides the same charge at the prescaler output.

3.8.2 Post layout simulations

Figure 3.44 shows the post layout simulations of total current consumption and oscillation frequency versus the bias voltage. The oscillation starts for a voltage bias of 0.4 V with a current consumption of 2.7 mA with a voltage supply of 1.2 V at 12.4 GHz.

The frequency of this voltage controlled ring oscillator goes form 12.4 GHz to 17.1 GHz for a voltage bias ranging from 0.4 V to 1.1 V and a current consumption from 2.7 mA to 8.4 mA.

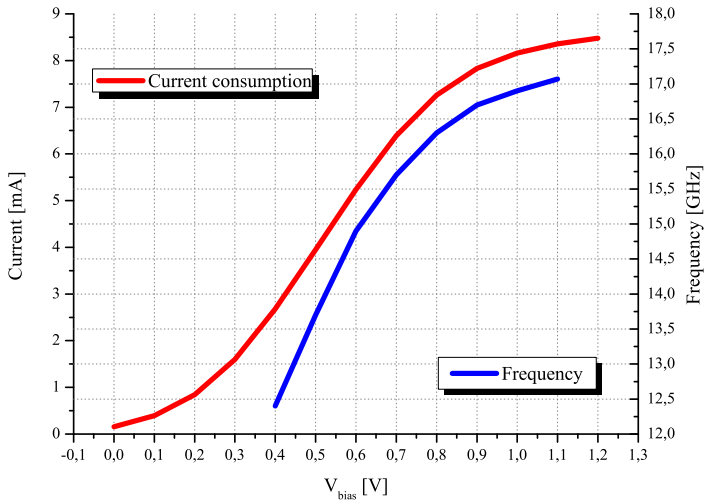

Figure 3.44: Frequency and current consumption versus bias voltage.

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Table 3.15: Ring Oscillator Frequency Divider Locking Range

V_{bias} [V]	f_0 [GHz]	f_{min} [GHz]	f_{max} [GHz]	LR [GHz]	LR [%]	I_{TOT} [mA]
0.4	12.4	17.7	33.0	15.3	60.4	2.68
0.5	13.7	18.3	38.0	19.7	69.8	3.95
0.6	14.9	21.3	39.1	17.7	58.7	5.24
0.7	15.7	24.5	38.6	14.1	44.7	6.39
0.8	16.3	27.6	37.9	10.3	31.5	7.26
0.9	16.9	30.4	37.2	6.8	20.1	7.83
1.0	16.9	32.4	36.6	4.2	11.9	8.36
1.1	12.4	32.2	34.2	2.0	5.1	8.48

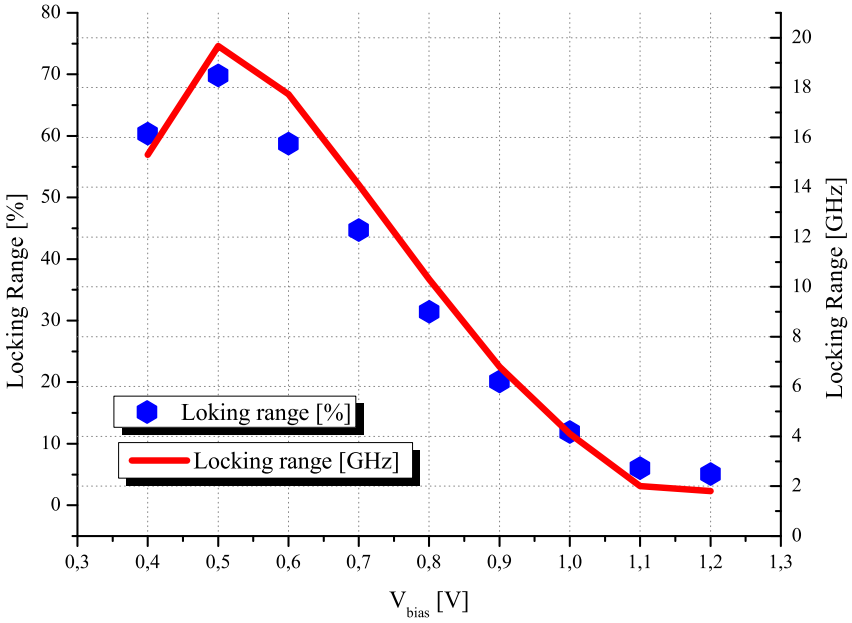

Figure 3.45: Locking range versus bias voltage.

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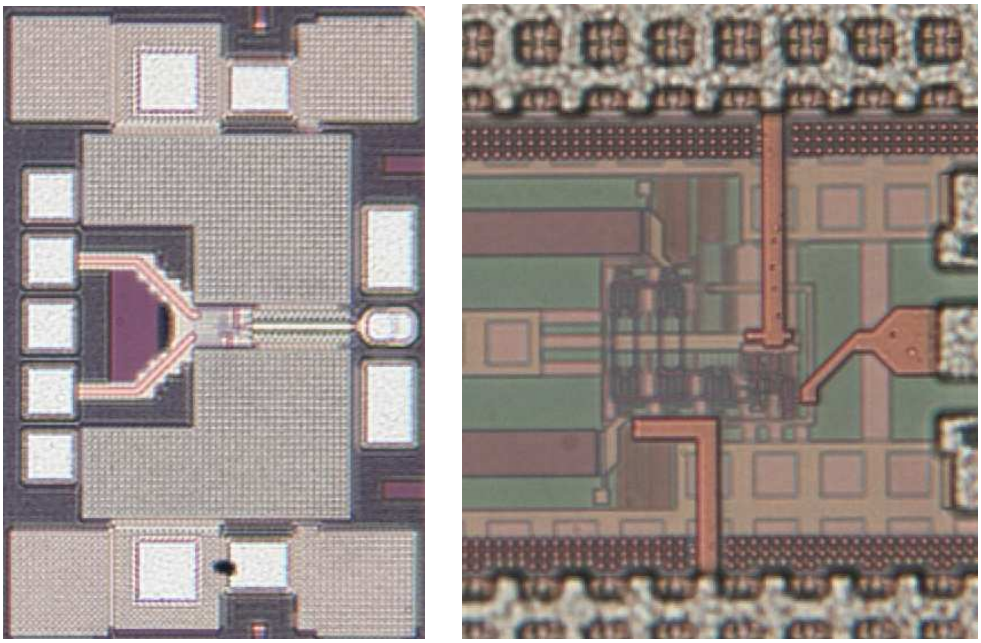
Figure 3.45 shows the locking range versus the bias voltage with a differential input signal of 300 mV . The optimum bias value is 0.5 V with a total power consumption of 4.8 mW. Table 3.15 shows the summary of the locking range for each value of bias voltage. Figure 3.46 shows the photomicrograph of the prototype implemented in the 65 nm CMOS technology from STMicroelectronics. The chip size is $620 \cdot 950\,\mu m^2$ including pads. The effective core chip area is $25 \cdot 35\,\mu m^2$.



(a) *Chip microphotograph.* (b) *Core Microphotograph.*

Figure 3.46: Injection-Locked Ring Oscillator Frequency Divider microphotograph.

The post layout simulations are in good agreement with the pecifications reported in the section 3.8.

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4 Conclusions

This last part summarizes the results presented in the Ph.D. thesis. The main topics have been handled. In particular the frequency generation at 15 GHz and 60 GHz for DVB-S and WPAN applications, respectively. For the second topic two kinds of injection locked frequency dividers have been designed.

In Chapter 2, the Voltage Controlled Oscillator (VCO) is discussed and a 15 GHz 130 nm CMOS Quadrature Voltage Controlled Oscillator (QVCO) is presented, which is used in a Ku band frequency synthesizer. At f_0=14.6 GHz the QVCO exhibits a phase noise of −106 dBc/Hz at the offset frequency (Δf) of 1 MHz. The FOM of −178.56 dBc/Hz is well aligned with other 130 nm CMOS VCOs reported in the literature.

In Chapter 3, frequency synthesizers are discussed and the millimeter wave VCO and Injection Locking Frequency Divider blocks are presented.

Concerning the VCO, the measured carrier frequency (f_0) goes from 71.87 GHz to 81.44 GHz for V_{TUNE} ranging between 0 V and 1.8 V corresponding to a tuning range of 12.4 %. The measurements of Voltage Controlled Oscillator (VCO) reveal a frequency shift versus the simulations. At f_0=71.8 GHz the VCO exhibits a phase noise of −116 dBc/Hz at the offset frequency (Δf) of 10 MHz. The FOM is −181.2 dBc/Hz and the FOM_T is −183.1 dBc/Hz. The phase-noise-related FOM is well aligned with other CMOS bulk VCOs reported in the literature, in particular for mmW applications.

Concerning the Injection Locking Frequency Divider two kinds of divider have been designed: an Injection-Locked LC-tank Frequency Divider (ILLCFD) and a Injection-Locked Ring Oscillator Frequency Divider (ILROFD).

- Concerning the ILLCFD, it consumes 3.6 mW from a 1.2 V supply, excluding buffers. With 0 dBm input power and V_{DD}=1.2 V, the proposed ILLCFD Locking Range is 15.7 GHz (63.5 GHz to 79.2 GHz) or 22 % of the center frequency. The measurements of Injection-Locked LC-tank Frequency Divider (ILLCFD) present very good agreement with the simulations and are well aligned with the state of the art claimed in the literature.

- The proposed ILROFD is just back from the foundry and will be tested as soon as

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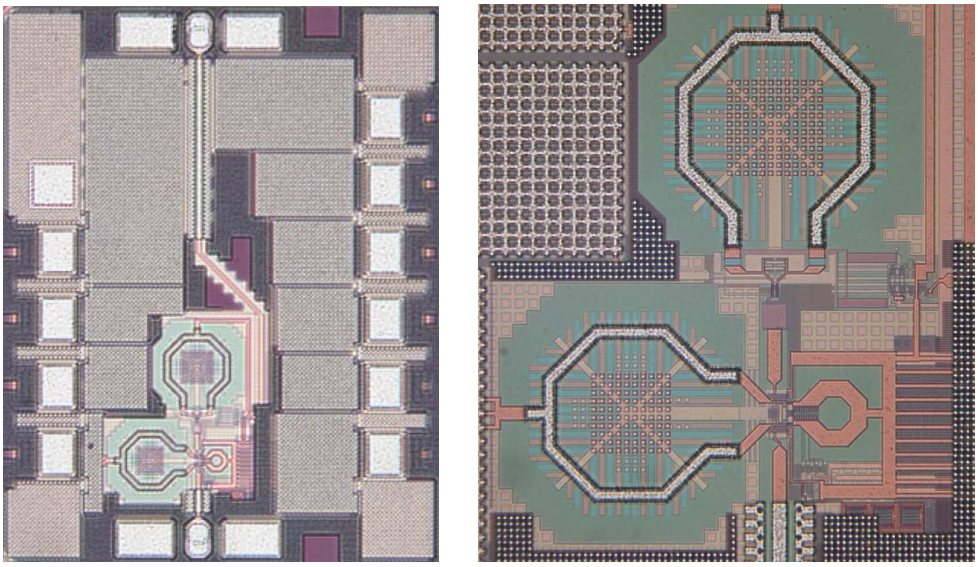
possible. The post layout simulations show good performances with a total power consumption of 4.8 mW.



(a) *Chip microphotograph.* (b) *Core Microphotograph.*

Figure 4.1: Microphotograph of th cascoded VCO, ILLCFD and ILROFD.

Finally, the last contribution of the present Ph.D. thesis has been the integration on the same die of the designed VCO, ILLCFD, and ILROFD. A microphotograph of the fabricated prototype is depicted in Figure 4.1. The chip will be test as soon as possible.

All designed circuits shows a good performance in millimeter wave band. The critical blocks of the PLL for WPAN applications have been designed. Next step is the design of the rest of division chain, Phase-Frequency Detector (PFD), Charge-Pump (CP), ad Loop Filter (LF).

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Acronyms

ACC	Adaptive Cruise Control
ACM	Adaptive Coding & Modulation
AM	Amplitude Modulation
APSK	Amplitude and Phase-Shift-Keying
ASK	Amplitude-Shift-Keying
ATM	Asynchronous Transfer Mode
AV	Audio/Visual
AWGN	Additive White Gaussian Noise
BB	Base-Band
BC	Backwards-Compatible
BCH	Bose-Chaudhuri-Hocquenghem
BER	Bit Error Rate
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BPF	Band-Pass-Filter
BPSK	Binary PSK
CCM	Constant Coding & Modulation
CML	Current Mode Logic
CMOS	Complementary MOS
CMS	Common Mode Signaling

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CP	Charge-Pump
CPPLL	Charge-Pump PLL
CPR	Cloud Profiling Radar
C/N	Carrier-to-Noise ratio
DAMI	Dual Alternate Mark Inversion
DBPSK	Differential BPSK
DC	Direct Current
DFF	D-Flip-Flop
DK	Design Kit
DRM	Design Rules Manual
DSNG	Digital Satellite News Gathering
DVB	Digital Video Broadcasting
DVB-S	Digital Video Broadcasting - Satellite
DVB-S2	Digital Video Broadcasting - Satellite - Second Generation
ECMA	European Computer Manufacturers Association
EHF	Extremely High Frequency
EIRP	Effective Isotropic Radiated Power
ELF	Extremely Low Frequency
ETSI	European Telecommunications Standards Institute
FCW	Frequency Control World
FD	Frequency Divider
FDM	Frequency Division Multiplex
FEC	Forward Error Correction
FOM	Figure Of Merit
GMSK	Gaussian MSK
GPR	Ground Penetrating Radar
GSG	Ground-Signal-Ground

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GSGSG	Ground-Signal-Ground-Signal-Ground
GSM	Global System for Mobile communication
HDMI	High Definition Multimedia Interface
HRP	High-Rate PHY
HEMT	High Electron Mobility Transistor
HSI	High-Speed Interface
HF	High Frequency
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IL	Injection-Locked
ILO	Injection-Locked Oscillator
I-MOS	inversion mode N-MOS
ITRS	International Technology Roadmap for Semiconductor
ITU	International Telecommunications Union
ITS	Intelligent Transportation Systems
ILFD	Injection Locking Frequency Divider
IR	infrared
IVC	inter-vehicle
LC	LC-tank
ILLCFD	Injection-Locked LC-tank Frequency Divider
ILROFD	Injection-Locked Ring Oscillator Frequency Divider
LDPC	Low Density Parity check Codes
LF	Loop Filter
LPF	Low-Pass Filter
LNA	Low Noise Amplifier
LNB	Low Noise Block
LR	Locking Range

LRP	Low-Rate PHY
LRR	Long-Range Radar
MAC	Medium Access Control
MCML	MOS Current Mode Logic
MF	Medium Frequency
MOS	Metal-Oxide-Semiconductor
MPEG	Moving Picture Experts Group
MOSFET	MOS Field-Effect Transistor
MSK	Minimum-Shift Keying
mmW	millimeter Wave
NLOS	Non-LIne-Of-Sight
OBO	Output Back-Off
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase-Frequency Detector
PHY	Physical Layer
PLL	Phase-Locked Loop
PM	Phase Modulation
PSK	Phase-Shift Keying
PVT	Process-Voltage-Temperature
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature PSK
QVCO	Quadrature Voltage Controlled Oscillator
RF	Radio Frequency
RO	Ring Oscillator
ROFD	Ring Oscillator Frequency Divider

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RVC	roadside to vehicle
SC	Single Carrier
SCBT	Single Carrier Block Transmission
SCL	Source Coupled Logic
SFD	Static FD
SHF	Super High Frequency
SLF	Super Low Frequency
SRR	Short Range Radar
TR	Tuning Range
TSPC	True Single Phase Clock
ULF	Ultralow Frequency
UV	ultraviolet
UHF	Ultrahigh Frequency
USB	Universal Serial Bus
UWB	Ultra-Wideband
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency
VLF	Very Low Frequency
WPAN	Wireless Personal Area Network
WLANs	Wireless Local Area Networks

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