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A. Amerasekera, Texas Instruments

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T. Blalock, University of Virginia

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2005 VLSI Circuits Short Course Program

"Multi-GHz Clocking Technologies for Microprocessors"

Wednesday, June 15, 2005 (Suzaku)

Organizers/Chairs: Makoto Nagata, Kobe University
Vivek De, Intel Corp.

8:30 Opening

8:40 Basics of High Performance Clock Delivery

Keng Wong, *Intel Corp.*

9:50 Break

10:10 High Frequency Clock Distribution and Resonant Clocking

Phillip Restle, *IBM*

11:10 PLL's, VCO's, DLL's & Delay Elements

Greg Taylor, *Intel Corp.*

12:20 Lunch

14:00 Clock Timing Adjustment With Genetic Algorithms

Tetsuya Higuchi, *AIST, Japan*

14:50 Techniques for Synchronizing Multiple Clock Domains

Masayuki Mizuno, *NEC*

15:40 Break

16:00 Clock Methodology for Low Power Design

Michio Komoda, *Renesas Technology Corp.*

16:50 Closing

A Temperature Stabilized CMOS VCO for Zero-IF Cellular CDMA Receivers

Yue Wu and Vladimir Aparin

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Abstract

A fully integrated CMOS VCO which has low temperature and power supply sensitivity has been implemented in a 0.25 μm 4-metal 1-poly process. The causes of oscillation frequency drift over temperature have been investigated. By adjusting the reverse biasing voltage of junction diodes and the back-side voltage of linearized MOS varactors, less than 10 ppm/ $^{\circ}\text{C}$ frequency drift has been achieved at 1.7GHz. Phase noise at 900kHz offset is less than -134dBc/Hz and varies less than 1dBc over $-30^{\circ}\text{C} \sim 90^{\circ}\text{C}$.

Key Words: VCO, frequency stability, linearized MOS varactor

Introduction

Frequency stability is an important issue in VCO design, this is especially true for full duplex system like CDMA receiver which receives signal continuously and can not be interrupted to re-calibrate the VCO discrete frequency control [1]. The minimum VCO continuous tuning range is set by the maximum frequency drift of the VCO, which has a trade-off for phase noise. Inside a cellular phone, the VCO frequency drift is most likely to be caused by the temperature or power supply variations. A VCO topology with low supply sensitivity has been presented before [2]. In this paper we present a fully integrated CMOS VCO with very low sensitivity to both temperature and supply variations, meeting the stringent phase noise requirement for Zero-IF CDMA receivers.

Causes of Oscillation Frequency Temperature Drift

In an LC tank oscillator, the oscillation frequency is determined by the inductance and the effective capacitance. Small variation of capacitance or inductance will change the frequency as $f \approx f_0 \left(1 - \frac{\delta_C}{2} - \frac{\delta_L}{2} \right)$ with $\delta_C = \frac{\Delta C}{C_0}$,

$\delta_L = \frac{\Delta L}{L_0}$ and f_0 the center frequency. With a center frequency to be around 1.7GHz, a small percentage variation over temperature could result in large frequency drift. For a fully integrated VCO, the inductance of the on-chip inductor is mainly determined by the physical dimensions. Even though the inductor loss will increase at high temperature, inductance temperature variation is neglectable[3]. On the other hand, the effective capacitance in an integrated VCO can vary a lot over temperature, several contributors are identified in a typical cross-coupled CMOS VCO with discrete tuning. As shown in the shaded area of Fig 1, the drain-bulk junction diodes of transistors M1~M4 are in shunt connection with tank inductor. When a coarse tuning capacitor is turned off, the drain and source bulk diodes of the switch transistors(M_d) are also in shunt with the inductor

through the MIM capacitors. Those reverse biased diodes present strong temperature dependency as

$$C_j(T) = \frac{C_j}{\sqrt[2]{V_D + \phi(T)}}, \text{ where } V_D \text{ the reverse biasing voltage,}$$

γ around 0.3~0.5 and $\phi(T)$ the junction potential which drops 2mV/ $^{\circ}\text{C}$. The temperature coefficient (TC) of the diode is $TC_D = \frac{\gamma}{1 + V_D / \phi} \cdot TC_{\phi}$ which is about 250~350 ppm/ $^{\circ}\text{C}$

depending on the reverse biasing voltage. Temperature variation may also cause minor change of the relative permittivity of the dielectric, thus the MIM capacitor may show some temperature dependency. For the process we used, MIM capacitor has a TC_{MIM} of 20 ppm/ $^{\circ}\text{C}$. The combined temperature coefficient for the tank capacitors will be

$$TC_{total} = \frac{C_D}{C_D + C_{min}} \cdot TC_D + \frac{C_{min}}{C_D + C_{min}} \cdot TC_{min}, \text{ which varies for}$$

different coarse tuning codes. Besides the variation caused by the components' temperature dependency, the non-linear behavior of the varactor may also generate temperature variation. As shown in Fig.2, the large signal swing across the varactor will generate an effective capacitance which is a function of the oscillation amplitude A_0 [4]. If A_0 is not well controlled over temperature, the effective capacitance will vary over temperature according to the following equation:

$$\frac{\partial C_{eff}}{\partial T} = - \frac{C_{max} - C_{min}}{A_0} \cdot \Delta V \cdot TC_{A0}, \text{ with } \Delta V \text{ the DC bias voltage}$$

across the varactor and TC_{A0} the amplitude temperature coefficient. Thus the C_{eff} variation has different polarity for positive and negative ΔV and making the compensation difficult.

Compensating Frequency Drift

With all the above effects combined, a 1.7GHz CMOS VCO can easily drift tens of MHz from -30°C to 90°C , which may cause the PLL out of lock if the continuous tuning range of the VCO is not wide enough. Circuit techniques should be employed to minimize that frequency drift without modifying the tuning voltage. To compensate the junction capacitance variation of the switching transistors M_d , a voltage source with +2mV/ $^{\circ}\text{C}$ increase can be used to reverse bias those diodes compensating the junction voltage drop. Fig.3 shows that the capacitance variation is one order lower by using this technique. To further compensate the junction diodes of M1~M4 of Fig.1 and MIM capacitor variations, the back-side bias voltage of the NMOS varactor can be varied over temperature to generate an offset capacitance canceling the drift. This is shown conceptually in Fig.4 that by increasing the back-side bias voltage V_{CM} over temperature,

the varactor capacitance is decreased by ΔC without changing the tuning voltage V_f . Note the varactor is coupled through MIM capacitor to the VCO tank so that the voltage swing across the varactor is small enough to neglect the non-linear averaging effect. For a varactor that has steep variation, the offset capacitance for temperature compensation ΔC_1 varies with different tuning voltage as shown in Fig.5. This is undesirable because the compensation would then highly dependent on the tuning voltage. As such, one more pair of varactors is added in parallel and the back-side is biased at shifted voltage V_{CM2} . The offset capacitance ΔC_2 is now averaged over the ranged from $V_{CM1} \sim V_{CM2}$, a relative constant compensation can thus be achieved over wider tuning voltage range.

Circuit Implementation

The above compensation approaches have been explored in a fully integrated CMOS VCO for CDMA receiver as shown in Fig.6. The oscillator topology is stacked diff-pairs with regulator explained in [2]. The regulating amplifier is a telescopic OTA for its high GBW and low noise. Note the regulator reference voltage is generated from a replica NFET M6 and its noise is attenuated by a first-order RC filter(R1 & C2). Similarly, to reduce the noise at the varactor back-side biasing node, RC filter is employed which has low pole around several kHz. To avoid this low pole frequency interfering with the PLL loop filter, low-noise voltage followers are employed to present low impedance at the common nodes of the varactor pairs. The bias voltages are set at 0.9V and 1.9V at room temperature with their TC adjustable. This adjustment is done by changing the temperature coefficient of resistor R2 in the PTAT circuit, where R2 is made of an array of composite resistors. Inside each composite resistor, it is a series connection of two resistors which have positive and negative TC . Changing the percentage of the two resistors can generate different TC . The inverter supply voltage for coarse tuning transistor is set

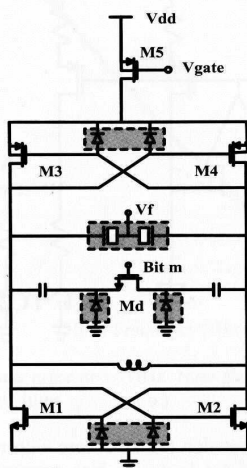


Fig. 1 Contributors of VCO frequency temperature drift

to 2V and has a $TC = 1000 \text{ ppm}/^\circ\text{C}$ which can compensate the junction voltage drop.

Measurements

The VCO is implemented in a $0.25 \mu\text{m}$ 4-metal 1-poly CMOS process and packaged in a 32-pin QFN. As shown in Fig.7, without any temperature compensation, the frequency drops more than 16MHz(@ 1.7GHz) when temperature varies from -30°C to $+90^\circ\text{C}$. By turning on the positive TC biasing voltages, the frequency drift is lower than 2MHz over 0.6~1.8V fine tune range which corresponding to an equivalent TC of less than $10 \text{ ppm}/^\circ\text{C}$. Phase noise measurement in Fig.8 shows the phase noise decreases at a rate of $1/f^2$ below 4.5kHz and continues at a rate of $1/f^4$ till 200kHz where back to $1/f^2$ again. This is caused by the dominating noise up-conversion of the first-order filter shaped noise. Phase noise variation over temperature is less than 1dB due to the PTAT nature of the VCO biasing current. The VCO can be tuned to cover 1.55GHz~1.95GHz through 6 discrete tuning branches with less than 100kHz/V power supply sensitivity. The die microphotograph is shown in Fig.10, the power consumption is 6.5mA from 2.5V including biasing circuit.

Reference

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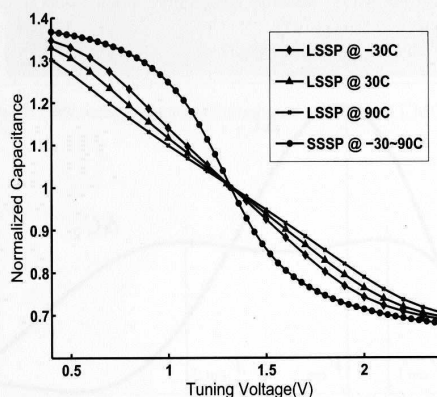


Fig.2 MOS varactors over temperature, note the Large-Signal-S-Parameter(LSSP) effective capacitance varies with temperature while Small-Signal-S-Parameter(SSSP) shows invisible temperature dependency

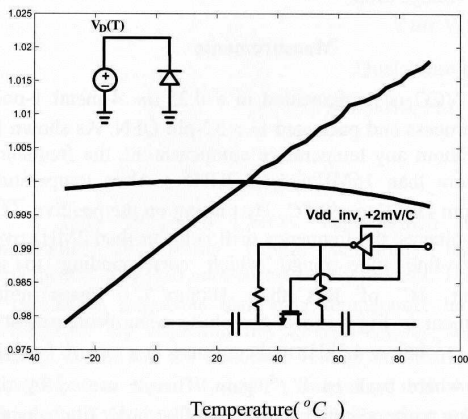


Fig.3 Normalized junction capacitance $C(T)/C_0$ over temperature (w/o compensation and with compensation)

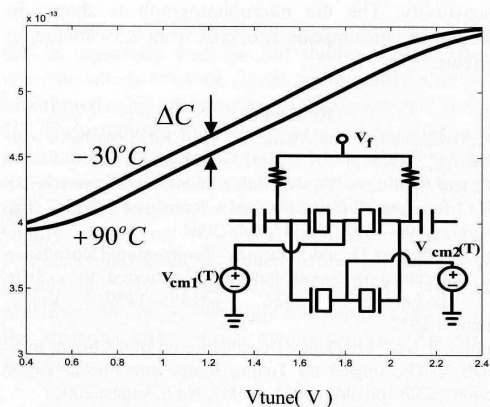


Fig.4 Linearized MOS varactor temperature compensation using back-side bias

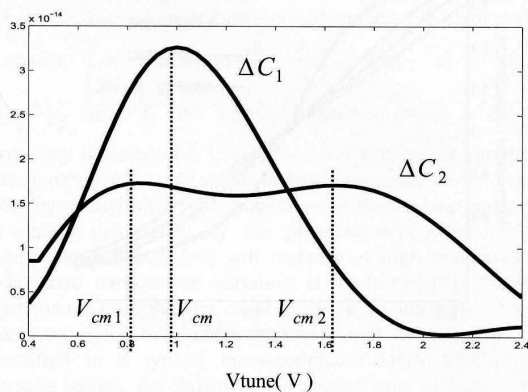


Fig.5 Compensating capacitance w/o linearization (ΔC_1) and with linearization (ΔC_2)

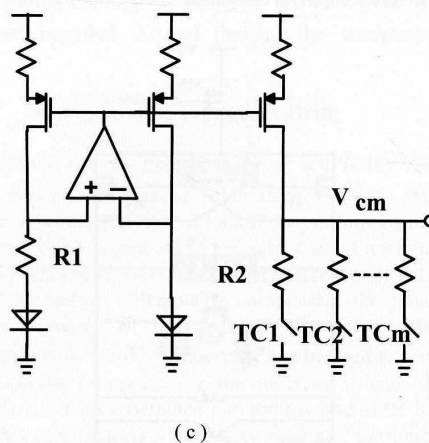
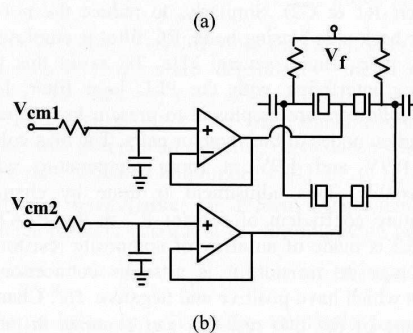
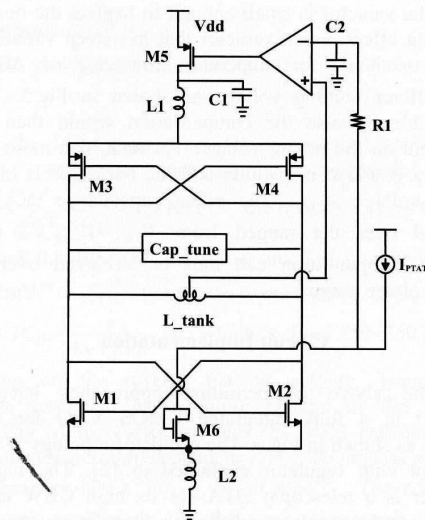


Fig. 6 Circuit implementation (a) VCO core with regulated power supply (b) MOS varactor back-side bias compensation (c) Bias circuit for different temperature coefficients

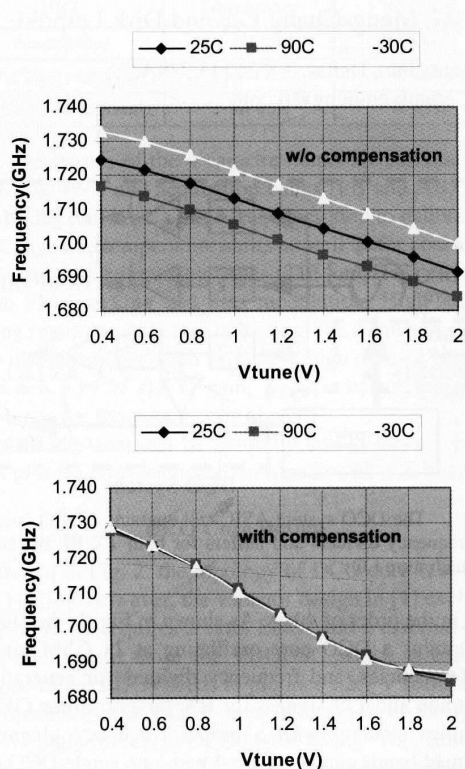


Fig. 7 Temperature drift measurement of VCO oscillation frequency before and after temperature compensation

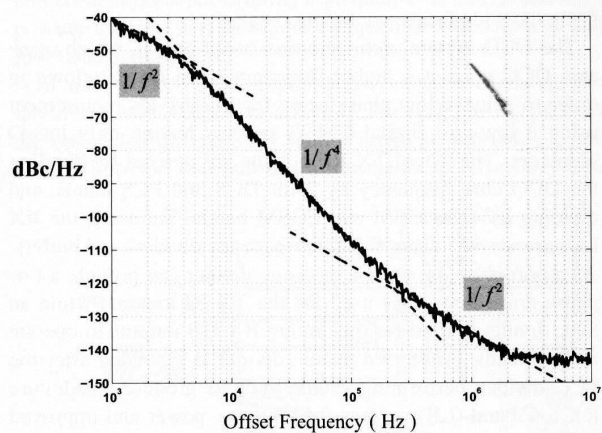


Fig. 8 VCO Phase noise at 1.7GHz. Note the slope of the PN curve caused by the RC filter

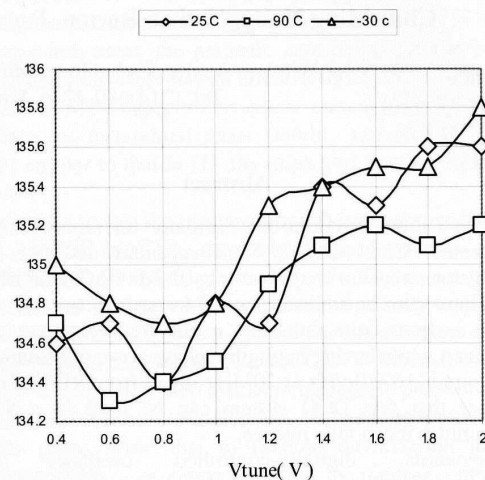


Fig. 9 Phase noise variation at 900kHz offset over fine tune voltage at different temperature

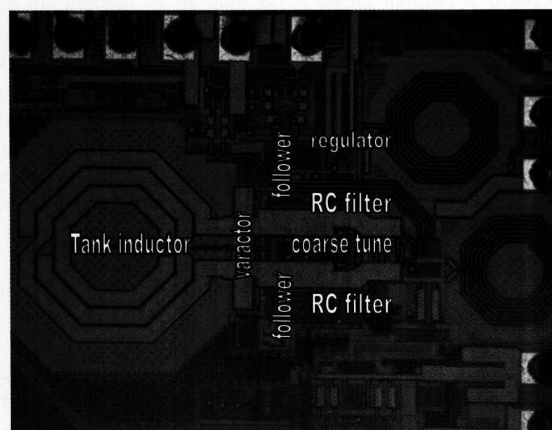


Fig. 10 Microphotograph of temperature stabilized CMOS VCO

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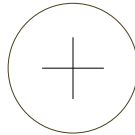
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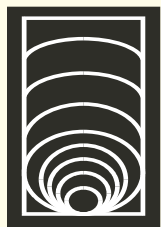
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200GHz CMOS Prescalers with Extended Dividing Range via Time-Interleaved Dual Injection Locking
(*Qun Jane Gu, Heng-Yu Jian, Zhiwei Xu, Yi-Cheng Wu, Mau-Chung Frank Chang, Yves Baeyens, Young-Kai Chen*)

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RMO1D: W-band and Above

Chair: Jenshan Lin, University of Florida — Co-Chair: Georg Boeck, Berlin Institute of Technology

Venue 212AB, Time 08:00–09:40, Monday May 24th 2010

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Transmitter Chipset for 24/77GHz Automotive Radar Sensors

(Vittorio Giammello, Egidio Ragonese, Giuseppe Palmisano)

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A 94GHz Passive Imaging Receiver Using a Balanced LNA with Embedded Dicke Switch

(Leland Gilreath, Vipul Jain, Hsin-Cheng Yao, Le Zheng, Payam Heydari)

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94GHz Silicon Co-Integrated LNA and Antenna in a mm-Wave Dedicated BiCMOS Technology

(R. Pilard, D. Gloria, F. Giancesello, F. Le Pennec, C. Person)

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A 3G-Bit/s W-Band SiGe ASK Receiver with a High-Efficiency On-Chip Electromagnetically-Coupled Antenna

(Jason W. May, Ramadan A. Alhalabi, Gabriel M. Rebeiz)

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A 325GHz Frequency Multiplier Chain in a SiGe HBT Technology

(Erik Öjefors, Bernd Heinemann, Ullrich R. Pfeiffer)

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RMO2A: RFID Circuits

Chair: Glenn Chang, MaxLinear — Co-Chair: Natalino Camilleri, Alien Technology

Venue 208AB, Time 10:10 – 11:50, Monday May 24th 2010

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Semi-Active High-Efficient CMOS Rectifier for Wireless Power Transmission
(*Stephen T. Kim, Taejoong Song, Jaehyouk Choi, Franklin Bien, Kyutae Lim, Joy Laskar*)

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A Single-Chip CMOS UHF RFID Reader Transceiver
(*Runxi Zhang, Chunqi Shi, Yihao Chen, Wei He, Ping Xu, Shuai Xu, Zongsheng Lai*)

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Near Zero Turn-On Voltage High-Efficiency UHF RFID Rectifier in Silicon-on-Sapphire CMOS
(*Paul T. Theilmann, Calogero D. Presti, Dylan Kelly, Peter M. Asbeck*)

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A Low Power Low Cost Fully Integrated UHF RFID Reader with 17.6dBm Output P1dB in 0.18 μ m CMOS Process
(*Jingchao Wang, Chun Zhang, Zhihua Wang*)

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Far-Field RF Powering System for RFID and Implantable Devices with Monolithically Integrated On-Chip Antenna
(*Soheil Radiom, Majid Baghaei-Nejad, Guy Vandenbosch, Li-Rong Zheng, Georges Gielen*)

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RMO2B: Wideband LNAs

Chair: Jean-Baptiste Begueret, IMS Lab, University of Bordeaux — Co-Chair: Danilo Manstretta, University of Pavia

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10:10 |  | A 2–1100MHz Wideband Low Noise Amplifier with 1.43dB Minimum Noise Figure
<i>(Mohamed El-Nozahi, Ahmed A. Helmy, Edgar Sánchez-Sinencio, Kamran Entesari)</i> |
| PAGE 123
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10:30 |  | A 0.045mm² 0.1–6GHz Reconfigurable Multi-Band, Multi-Gain LNA for SDR
<i>(Arnd Geis, Yves Rolain, Gerd Vandersteen, Jan Craninckx)</i> |
| PAGE 127
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10:50 |  | A Linearity-Enhanced Wideband Low-Noise Amplifier
<i>(Kihwa Choi, Tamal Mukherjee, Jeyanandh Paramesh)</i> |
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11:10 |  | Power Efficient Distributed Low-Noise Amplifier in 90nm CMOS
<i>(Brecht Machiels, Patrick Reynaert, Michiel Steyaert)</i> |
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11:30 |  | A Wide-Band RF Front-End with Linear Active Notch Filter for Mobile TV Applications
<i>(Seung Hwan Jung, Kang Hyuk Lee, Young Jae Lee, Hyun Kyu Yu, Yun Seong Eo)</i> |

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RMO2C : Millimeter-Wave VCOs

Chair: Jing-Hong Chen, Analog Devices — Co-Chair: Tian-Wei Huang, National Taiwan University

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A mm-Wave Arbitrary 2^N Band Oscillator Based on Even-Odd Mode Technique

(Alvin Hsing-Ting Yu, Sai-Wang Tam, David Murphy, Tatsuo Itoh, Mau-Chung Frank Chang)

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A 24GHz and 60GHz Dual-Band Standing-Wave VCO in 0.13 μ m CMOS Process

(Liang Wu, Alan W.L. Ng, Lincoln L.K. Leung, Howard C. Luong)

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Multi-Band Multi-Standard Local Oscillator Generation for Direct Up/Down Conversion Transceiver Architectures Supporting WiFi and WiMax Bands in Standard 45nm CMOS Process

(Ram Sadhwani, Assaf Ben Bassat, Adil A. Kidwai, Shahar Rivel)

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A 0.13 μ m CMOS Local Oscillator for 60GHz Applications Based on Push-Push Characteristic of Capacitive Degeneration

(Tino Copani, Hyungseok Kim, Bertan Bakkaloglu, Sayfe Kiaei)

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A Switched-Capacitor mm-Wave VCO in 65nm Digital CMOS

(Mohammad Nariman, Reza Rofougaran, Franco De Flaviis)

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RMO2D: Reconfigurable PA Concepts

Chair: Joseph Staudinger, Freescale — Co-Chair: Jyoti P. Mondal, Northrop Grumman

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Multi-Mode WCDMA Power Amplifier Module with Improved Low-Power Efficiency Using Stage-Bypass

(Gary Hau, Mahendra Singh)

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A 3.4GHz to 4.3GHz Frequency-Reconfigurable Class E Power Amplifier with an Integrated CMOS-MEMS LC Balun

(Leon Wang, Tamal Mukherjee)

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A Q-Band 6W MMIC Power Amplifier with 3-Way Power Combination Circuit

(Hiroshi Otsuka, Kazuhisa Yamauchi, Koji Yamanaka, Shin Chaki, Kazuhiko Nakahara, Kunihiro Endo, Akira Inoue, Yoshihito Hirano)

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A Multi-Band Reconfigurable Power Amplifier for UMTS Handset Applications

(Unha Kim, Kyutae Kim, Junghyun Kim, Youngwoo Kwon)

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High-Efficiency Reconfigurable RF Transmitter for Wireless Sensor Network Applications

(Francesco Carrara, Giuseppe Palmisano)

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RMO3A : CMOS Wideband Transceiver ICs

Chair: Domine Leenaerts, NXP Semiconductor — Co-Chair: Haolu Xie, Fujitsu Microelectronics

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A Triband 65nm CMOS Tuner for ATSC Mobile DTV SoC

(Sanghoon Kang, Huijung Kim, Jeong-Hyun Choi, Jae-Hong Chang, Jong-Dae Bae, Woooseung Choo, Byeong-ha Park)

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A Multi-Standard Multi-Band Tuner for Mobile TV SoC with GSM Interoperability

(Huijung Kim, Sanghoon Kang, Jae-Hong Chang, Jeong-Hyun Choi, Hangun Chung, Jungwook Heo, Jong-Dae Bae, Woooseung Choo, Byeong-ha Park)

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A 2.2mW Regenerative FM-UWB Receiver in 65nm CMOS

(Nitz Saputra, John R. Long, John J. Pekarik)

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A 75pJ/Bit All-Digital Quadrature Coherent IR-UWB Transceiver in 0.18 μ m CMOS

(Enrique Barajas, Didac Gómez, Diego Mateo, José Luis González)

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A 90nm-CMOS, 500Mbps, Fully-Integrated IR-UWB Transceiver Using Pulse Injection-Locking for Receiver Phase Synchronization

(Changhui Hu, Patrick Y. Chiang, Kangmin Hu, Huaping Liu, Rahul Khanna, Jay Nejedlo)

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RMO3B: Advanced Characterization of mm-Wave Components

Chair: Kevin McCarthy, University College Cork — Co-Chair: Herbert Zirath, Chalmers University of Technology

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The “Load-Thru” (LT) De-Embedding Technique for the Measurements of mm-Wave Balanced 4-Port Devices

(Zhiming Deng, Ali M. Niknejad)

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RF-Pad, Transmission Lines and Balun Optimization for 60GHz 65nm CMOS Power Amplifier

(Sofiane Aloui, Eric Kerherve, Robert Plana, Didier Belot)

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200GHz f_T SiGe HBT Load Pull Characterization at mm-Wave Frequencies

(Luciano Boglione, Richard T. Webster)

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A Miniature 26/77GHz Dual-Band Branch-Line Coupler Using Standard 0.18 μ m CMOS Technology

(Yu-Sheng Lin, Cheng-Ying Hsu, Huey-Ru Chuang, Chu-Yu Chen)

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Compact Transformer Power Combiners for Millimeter-Wave Wireless Applications

(Yi Zhao, John R. Long, Marco Spirito)

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RMO3C : Advanced Device Technologies & Design Techniques

Chair: Aditya Gupta, Northrup Grumman — Co-Chair: Eli Reese, TriQuint Semiconductor

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Integration of Multi-Standard Front End Modules SOCs on High Resistivity SOI RF CMOS Technology

(F. Giancesello, S. Boret, B. Martineau, C. Durand, R. Pilard, D. Gloria, B. Rauber, C. Raynaud)

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Vast-Fast Low-Triggering LTdSCR ESD Protection Structure for RF ICs in CMOS

(Jian Liu, Lin Lin, Xin Wang, Hui Zhao, He Tang, Qiang Fang, Albert Wang, Hongyi Chen, Haolu Xie, Siqiang Fan, Bin Zhao, Gary Zhang)

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A Cost-Competitive High Performance Junction-FET (JFET) in CMOS Process for RF & Analog Applications

(Yun Shi, Robert M. Rassel, Richard A. Phelps, Panglijen Candra, Douglas B. Hershberger, Xiaowei Tian, Susan L. Sweeney, Jay Rascoe, BethAnn Rainey, Jim Dunn, David Haramé)

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Tunability of Bulk Acoustic Wave Filters Using CMOS Transistors: Concept, Design and Implementation

(M. El Hassan, Eric Kerherve, Yann Deval, J.B. David, Didier Belot)

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A Layout Efficient, Vertically Stacked, Resonator-Coupled Bandpass Filter in LTCC for 60GHz SOP Transceivers

(Rony E. Amaya)

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Co-Design Considerations for Frequency Drift Compensation in BAW-Based Time Reference Application

(S. Razafimandimby, D. Petit, P. Bar, S. Joblot, J.-F. Carpentier, J. Morelle, C. Arnaud, G. Parat, Patrice Garcia, C. Garnier)

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RMO3D: Switch & Switch-mode Technologies

Chair: Nick Cheng, Skyworks Solutions — Co-Chair: Youngwoo Kwon, Seoul National University

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High Efficiency and Wideband Envelope Tracking Power Amplifier with Sweet Spot Tracking

(Dongsu Kim, Jinsung Choi, Daehyun Kang, Bumman Kim)

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A 150MHz, 84% Efficiency, Two Phase Interleaved DC-DC Converter in AlGaAs/GaAs P-HEMT Technology for Integrated Power Amplifier Modules

(Han Peng, V. Pala, T.P. Chow, Mona Hella)

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A 0dBm 10Mbps 2.4GHz Ultra-Low Power ASK/OOK Transmitter with Digital Pulse-Shaping

(Xiongchuan Huang, Pieter Harpe, Xiaoyan Wang, Guido Dolmans, Harmke de Groot)

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A Linear-in-dB SiGe HBT Wideband High Dynamic Range RF Envelope Detector

(Hsuan-yu Marcus Pan, Lawrence E. Larson)

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Cellular Antenna Switches for Multimode Applications Based on a Silicon-on-Insulator Technology

(Ali Tombak, Christian Iversen, Jean-Blaise Pierres, Dan Kerr, Mike Carroll, Phil Mason, Eddie Spears, Todd Gillenwater)

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RMO4A: Ultra Low Power Receivers and Transmitters

Chair: Julian Tham, Arda Technologies — Co-Chair: Bill Redman-White, NXP

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A 120 μ W Fully-Integrated BPSK Receiver in 90nm CMOS

(Han Yan, Jose Gabriel Macias-Montero, Atef Akhnoukh, Leo C.N. de Vreede, John R. Long, John J. Pekarik, Joachim N. Burghartz)

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A Fully Integrated 2.4GHz CMOS Diversity Receiver with a Novel Antenna Selection

(Yong-IL Kwon, Sang-Ku Park, T.J. Park, Hai-Young Lee)

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A 90 μ W MICS/ISM Band Transmitter with 22% Global Efficiency

(Jagdish Pandey, Brian Otis)

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A 2mW CMOS MICS-Band BFSK Transceiver with Reconfigurable Antenna Interface

(Seungkee Min, S. Shashidharan, Mark Stevens, Tino Copani, Sayfe Kiaei, Bertan Bakkaloglu, Sudipto Chakraborty)

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A 1.8 to 2.4GHz 20mW Digital-Intensive RF Sampling Receiver with a Noise-Canceling Bandpass Low-Noise Amplifier in 90nm CMOS

(Joonhee Lee, Jaewook Kim, SeongHwan Cho)

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RMO4B: Optimized Design Techniques for RF Front-end Building Blocks

Chair: Osama Shana'a, Mediatek Corp. — Co-Chair: Ali Afsahi, Broadcom

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A Differential 4-Path Highly Linear Widely Tunable On-Chip Band-Pass Filter

(Amir Ghaffari, Eric A.M. Klumperink, Bram Nauta)

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A CMOS Wide-Bandwidth High-Power Linear-in-dB Variable Attenuator Using Body Voltage Distribution Method

(Yan-Yu Huang, Wangmyong Woo, Chang-Ho Lee, Joy Laskar)

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A 17GHz Transformer-Neutralized Current Re-Use LNA and Its Application to a Low-Power RF Front-End

(Sandipan Kundu, Jeyanandh Paramesh)

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A Self-Healing 2.4GHz LNA with On-Chip S_{11}/S_{21} Measurement/Calibration for *in-situ* PVT Compensation

(Karthik Jayaraman, Qadeer Khan, Baoyong Chi, William Beattie, Zhihua Wang, Patrick Y. Chiang)

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A Low Power LNA Using Miniature 3D Inductor Without Area Penalty of Passive Components

(Akira Tanabe, Ken'ichiro Hijioaka, Hirokazu Nagase, Yoshihiro Hayashi)

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RMO4C: Temperature Compensated Oscillators

Chair: Timothy Hancock, MIT Lincoln Laboratory — Co-Chair: Donald Y.C. Lie, Texas Tech. University

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A 65nm CMOS DCXO System for Generating 38.4MHz and a Real Time Clock from a Single Crystal in 0.09mm²

(Danielle Griffith, Fikret Dülger, Gennady Feygin, Ahmed Nader Mohieldin, Prasanth Vallur)

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A 50ppm 600MHz Frequency Reference Utilizing the Series Resonance of an FBAR

(Julie Hu, Lori Callaghan, Richard Ruby, Brian Otis)

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An Electronically Temperature-Compensated 427MHz Low Phase-Noise AlN-on-Si Micromechanical Reference Oscillator

(Hossein Miri Lavasani, Wanling Pan, Farrokh Ayazi)

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A Wide Tuning 1.3GHz LC VCO with Fast Settling Noise Filtering Voltage Regulator in 0.18μm CMOS Process

(Hiroshi Akima, Aleksander Dec, Ken Suyama)

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A Wide-Range VCO with Optimum Temperature Adaptive Tuning

(Behzad Saeidi, Joshua Cho, Georgi Taskov, Aaron Paff)

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RMO4D: Silicon Millimeter-Wave Amplifiers

Chair: Kevin Kobayashi, RF Micro Devices — Co-Chair: Paul Blount, Custom MMIC Design

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A 60GHz Transformer Coupled Amplifier in 65nm Digital CMOS

(Michael Boers)

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A Stage-Scaled Distributed Power Amplifier Achieving 110GHz Bandwidth and 17.5dBm Peak Output Power

(Jiashu Chen, Ali M. Niknejad)

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DC Hot Carrier Stress Effect on CMOS 65nm 60GHz Power Amplifiers

(T. Quémerais, L. Moquillon, V. Huard, J.-M. Fournier, P. Benech, N. Corrao)

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A Layout-Based Optimal Neutralization Technique for mm-Wave Differential Amplifiers

(Zhiming Deng, Ali M. Niknejad)

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A 100GHz Transformer-Coupled Fully Differential Amplifier in 90nm CMOS

(Noël Deferm, Patrick Reynaert)

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RTU1B: CMOS Millimeter-Wave 60/24GHz Radio

Chair: Frank Henkel, IMST GmbH, Kamp-Lintfort — Co-Chair: Mark Ruberto, Intel Corp.

Venue 207AB, Time 08:00 – 09:40, Tuesday May 25th 2010

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| PAGE 365
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08:00 |  | A 68–82GHz Integrated Wideband Linear Receiver Using 0.18μm SiGe BiCMOS
<i>(Austin Ying-Kuang Chen, Yves Baeyens, Young-Kai Chen, Jenshan Lin)</i> |
| PAGE 369
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08:20 |  | A 24GHz Low-Power Fully Integrated Receiver with Image-Rejection Using Rich-Transformer Direct-Stacked/Coupled Technique
<i>(Nobuhiro Shiramizu, Takahiro Nakamura, Toru Masuda, Katsuyoshi Washio)</i> |
| PAGE 373
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08:40 |  | A 60GHz CMOS Receiver Front-End with Integrated 180° Out-of-Phase Wilkinson Power Divider
<i>(Chi-Chen Chen, Yo-Sheng Lin, Jen-How Lee, Jin-Fa Chang)</i> |
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09:00 |  | Coherent Parametric RF Downconversion in CMOS
<i>(Zhixing Zhao, Jean-François Bousquet, Sebastian Magierowski)</i> |
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09:20 |  | 60GHz Broadband Image Rejection Receiver Using Varactor Tuning
<i>(Jihoon Kim, Wooyeol Choi, Youngrak Park, Youngwoo Kwon)</i> |

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RTU1C: CMOS PAs

Chair: Eddie Spears, RFMD — Co-Chair: Freek van Straten, NXP Semiconductors

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A Discrete Resizing and Concurrent Power Combining Structure for Linear CMOS Power Amplifier

(Jihwan Kim, Hyungwook Kim, Youngchang Yoon, Kyu Hwan An, Woonyun Kim, Chang-Ho Lee, Kevin T. Kornegay, Joy Laskar)

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A Single-Chip 2.4GHz Double Cascode Power Amplifier with Switched Programmable Feedback Biasing Under Multiple Supply Voltages in 65nm CMOS for WLAN Application

(Mingyuan Li, Ali Afsahi, Arya Behzad)

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A 31dBm, High Ruggedness Power Amplifier in 65nm Standard CMOS with High-Efficiency Stacked-Cascode Stages

(Stephan Leuschner, Sandro Pinarello, Uwe Hodel, Jan-Erik Mueller, Heinrich Klar)

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Analysis and Design of a Wideband High Efficiency CMOS Outphasing Amplifier

(M.C.A. van Schie, M.P. van der Heijden, M. Acar, A.J.M. de Graauw, Leo C.N. de Vreede)

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A Highly Efficient 5.8GHz CMOS Transmitter IC with Robustness Over PVT Variations

(Eun-Hee Kim, Jeong-Ki Choi, Seok-Oh Yun, Jinho Ko, Kwyro Lee)

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RTU1D: Emerging Architectures in Digital Frequency Synthesis

Chair: Stefano Pellerano, Intel Corporation — Co-Chair: Sanjay Raman, Virginia Tech

Venue 212AB, Time 08:00–09:40, Tuesday May 25th 2010

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A 700 μ A, 405MHz Fractional-N All Digital Frequency-Locked Loop for MICS Band Applications

(S. Shashidharan, W. Khalil, Sudipto Chakraborty, Sayfe Kiaei, Tino Copani, Bertan Bakkaloglu)

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A 2MHz Bandwidth Δ - Σ Fractional-N Synthesizer Based on a Fractional Frequency Divider with Digital Spur Suppression

(Pin-En Su, Sudhakar Pamarti)

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A 6fJ/step, 5.5ps Time-to-Digital Converter for a Digital PLL in 40nm Digital LP CMOS

(J. Borremans, K. Vengattarmane, Jan Craninckx)

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A 6GHz Direct Digital Synthesizer MMIC with Nonlinear DAC and Wave Correction ROM

(Danyu Wu, Gaopeng Chen, Jianwu Chen, Xinyu Liu, Lixin Zhao, Zhi Jin)

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A 10GHz 8-Bit Direct Digital Synthesizer Implemented in GaAs HBT Technology

(Gaopeng Chen, Danyu Wu, Zhi Jin, Jin Wu, Xinyu Liu)

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RTU2A: WLAN Transceivers and Components

Chair: Albert Jerng, Ralink Technology — Co-Chair: Srenik Mehta, Atheros Communications

Venue 207AB, Time 13:20 – 15:00, Tuesday May 25th 2010

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Dual-Band CMOS Transceiver with Highly Integrated Front-End for 450Mb/s 802.11n Systems

(Shai Gross, Tzvi Maimon, Fabian Cossoy, Mark Ruberto, Georgi Normatov, Alexander Rivkind, Nikolay Telzhensky, Rotem Banin, Ori Ashckenazi, Assaf Ben Bassat, Sharon Zaguri, Gabriel Hara, Mario Zajac, Nir Shaha, Shay Shahaf, Hani Yousef, Eyal Mor, Yishai Eilat, Anna Nazimov, Zeev Beer, Amir Fridman, Ofir Degani)

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A CMOS Transceiver with Internal PA and Digital Pre-Distortion for WLAN 802.11a/b/g/n Applications

(Chia-Jun Chang, Po-Chih Wang, Chih-Yu Tsai, Chin-Lung Li, Chiao-Ling Chang, Han-Jung Shih, Meng-Hsun Tsai, Wen-Shan Wang, Ka-Un Chan, Ying-Hsi Lin)

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Highly Linear SOI Single-Pole, 4-Throw Switch with an Integrated Dual-Band LNA and Bypass Attenuators

(Chun-Wen Paul Huang, Lui Lam, Mark Doherty, William Vaillancourt)

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A 6.1GS/s 52.8mW 43dB DR 80MHz Bandwidth 2.4GHz RF Bandpass $\Delta\Sigma$ ADC in 40nm CMOS

(Julien Ryckaert, Arnd Geis, Lynn Bos, Geert Van der Plas, Jan Craninckx)

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Single-Chip WiFi b/g/n 1×2 SoC with Fully Integrated Front-End & PMU in 90nm Digital CMOS Technology

(J.C. Jensen, Ram Sadhwani, Adil A. Kidwai, B. Jann, A. Oster, M. Sharkansky, I. Ben-bassat, Ofir Degani, S. Porat, Amir Fridman, H. Shang, C. Chu, A. Ly, M. Smith)

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RTU2C: Millimeter-Wave Arrays

Chair: Brian Floyd, North Carolina State University — Co-Chair: C. Patrick Yue, UC Santa Barbara

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A 44GHz 8-Element Phased-Array SiGe HBT Transmitter RFIC with an Injection-Locked Quadrature Frequency Multiplier
(*Sunghwan Kim, Prasad S. Gudem, Lawrence E. Larson*)

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A Thirty Two Element Phased-Array Transceiver at 60GHz with RF-IF Conversion Block in 90nm Flip Chip CMOS Process
(*Emanuel Cohen, Claudio Jakobson, Shmuel Ravid, Dan Ritter*)

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A 16-Element Phased-Array Receiver IC for 60GHz Communications in SiGe BiCMOS
(*Scott K. Reynolds, Arun S. Natarajan, Ming-Da Tsai, Sean Nicolson, Jing-Hong Conan Zhan, Duixian Liu, Dong G. Kam, Oscar Huang, Alberto Valdes-Garcia, Brian A. Floyd*)

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A 24GHz Phased-Array Receiver in 0.13 μ m CMOS Using an 8GHz LO
(*Satwik Patnaik, Ramesh Harjani*)

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Wafer-Scale W-Band Power Amplifiers Using On-Chip Antennas
(*Yusuf A. Atesal, Berke Cetinoneri, Ramadan A. Alhalabi, Gabriel M. Rebeiz*)

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RTU2D: RF Modeling for Switch and PA Applications

Chair: Francis Rotella, Peregrine Semiconductor — Co-Chair: Yuhua Cheng, Peking University

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Application of BSIMSOI MOSFET Model to SOS Technology

(James Roach, Lee-Wen Chen, Peter Clarke, Francis M. Rotella)

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Modeling of SOI FET for RF Switch Applications

(Tzung-Yin Lee, Sunyoung Lee)

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A High Power CMOS Differential T/R Switch Using Multi-Section Impedance Transformation Technique

(Hyun-Woong Kim, Minsik Ahn, Ockgoo Lee, Chang-Ho Lee, Joy Laskar)

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(Mauro Marchetti, Rob Heeres, Michele Squillante, Marco Pelk, Marco Spirito, Leo C.N. de Vreede)

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Venue 208AB, 209AB, Time 14:00 – 16:00, Tuesday May 25th 2010

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A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS

Mohammad Nariman^{1,2}, Reza Rofougaran², and Franco De Flaviis^{1,2}

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Abstract — A 34-40 GHz VCO fabricated in 65 nm digital CMOS technology is demonstrated in this paper. The VCO uses a combination of switched capacitors and varactors for tuning and has a maximum K_{VCO} of 240 MHz/V. It exhibits a phase noise of better than -98 dBc/Hz @ 1-MHz offset across the band while consuming 12 mA from a 1.2-V supply, an FOM_T of -182.1 dBc/Hz. A cascode buffer following the VCO consumes 11 mA to deliver 0 dBm LO signal to a 50Ω load.

Index Terms — CMOS LC-VCO, figure of merit, FOM_T , mm-wave, phase noise, switched capacitor, tuning range.

I. INTRODUCTION

In recent years, the large amount of unlicensed spectrum at the millimeter-wave frequency range has attracted attention for wireless uncompressed video streaming and high performance personal area network applications. Realization of mm-wave radios in digital CMOS makes it possible for the high performance applications to benefit from high integration capacity offered by this technology. Further integration can be achieved by using monolithic mm-wave antennas as they require small footprints.

The high level of integration creates the possibility of realizing “DC-Boards” on which interconnections are limited to pure DC routings and their high speed data buses are replaced by chip to chip wireless links, resulting in significant cost and power savings. This work is part of a project with an aim of evaluating the feasibility of small, low power, and high performance mm-wave transceivers in pure digital CMOS technology. As one of the most challenging parts of a mm-wave radio, the VCO often has to meet stringent specifications. This paper demonstrates the design and implementation of a VCO in 65 nm digital CMOS process with f_{max} of 200 GHz and f_T of 140 GHz.

As indicated in (1), phase noise of the VCO degrades 6 dB/octave as the oscillation frequency increases [1]-[2]. At frequencies > 20 GHz non-quasi-static effects for the capacitors and the skin and the proximity effects for the inductors severely degrade their quality factors and pose significant challenges to the design of the VCO [3].

$$L\{\Delta f\} = 10 \log \left[\frac{FkT}{2P_s} \cdot \left(\frac{f_0}{2Q_T \Delta f} \right)^2 \cdot \left(1 + \frac{f_c}{\Delta f} \right) \right] \quad (1)$$

Where $L\{\Delta f\}$ is the single sideband power spectral density of the phase noise in dBc/Hz at the offset frequency of Δf from the oscillation frequency of f_0 . f_c is the flicker noise corner. Q_T is the loaded quality factor of the tank. P_s is the VCO signal power in Watt. F is the effective noise factor of the oscillator. T is the temperature in °K and k is the Boltzmann’s constant.

Section II covers the architecture design and describes the topology. In section III detailed description of each component of the design is provided, with emphasis on the innovative parts. Section IV discusses the experimental results and summarizes the performance characteristics in comparison with the results of other recently published CMOS VCOs. Probing unlocked mm-wave VCOs is extremely challenging and section V is dedicated to discuss that. Section VI concludes this paper by presenting a quick summary of what has been achieved.

II. ARCHITECTURE AND TOPOLOGY

Several architectures have been evaluated including Colpitts in terms of their achievable FOM. As shown in Fig. 1 a cross-coupled VCO architecture with doughnut-shaped grounded-gate NMOS pair has been chosen due to its superior power and area efficiency. A combination of switched capacitors and accumulation-mode varactors comprise the variable capacitance of the tank. A shared-diffusion cascode buffer with a balanced transformer load delivers the LO signal to the probe pads.

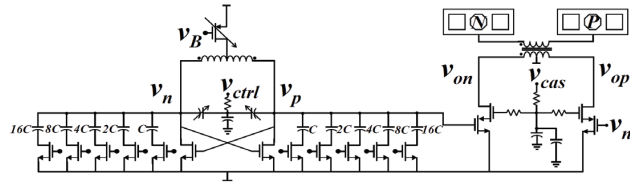


Fig. 1. Simplified schematic of the VCO and its buffer.

Using only varactors to achieve a large tuning range for the VCO results in a high K_{VCO} which as (2) indicates increases the AM to PM conversion gain which in turn causes high phase noise and spurious signal levels. In this work using the switched-capacitors has helped in reducing the K_{VCO} and increasing the tuning range significantly.

$$\Phi_{PM}(f_0 + f_{AM}) = \left[\frac{K_{VCO}}{2f_{AM}} \right] \cdot V_{AM}(f_{AM}) \quad (2)$$

Where Φ_{PM} is the level of the PM signal at the output of the VCO oscillating at the frequency of f_0 in response to an AM disturbance voltage with amplitude of V_{AM} and frequency of f_{AM} .

The reliability concerns of deep sub-micron processes make the VCO operate in the current-limited mode. Using a PMOS current source is optimum for biasing the VCO in this mode. This is also to provide the VCO buffer with a proper DC bias needed for an efficient LO power delivery.

III. CIRCUIT DESIGN AND IMPLEMENTATION

Detailed descriptions of the VCO components and explanations of the design are presented in this section.

A. VCO Core

Doughnut transistors comprised of square-shaped polysilicon gates are used for the VCO cross-coupled pair. This reduces the contribution of the drain junction capacitors to less than 5% of the overall tank capacitance. Size selection for the core devices has been done based on four different factors: gain, Noise Figure (NF), current switching capability, and efficient power delivery by providing a proper bias to the VCO buffer. The optimum current density for the lowest NF depends on the lateral electric field in the channel [4]. For the process of this VCO, a current density of $0.35 \text{ mA}/\mu\text{m}$ results in a suitable performance from all of the mentioned aspects.

Fig. 2 shows the unit cell of the VCO core with an optimal layout. The layout of the transistors should be optimized in order to achieve an optimal performance in terms of f_{max} , maximum stable gain, and the noise figure. Wider routings cause larger parasitic capacitances and couplings, while narrower interconnections create larger series resistances and inductances.

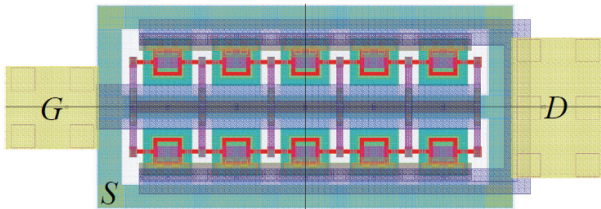


Fig. 2. Layout of the unit cell of the VCO core containing ten doughnut-shaped transistors with optimized routings.

B. Resonant Tank

The resonant tank is composed of a 135 pH differential octagonal-shaped inductor, accumulation-mode varactors and 5-bit binary-weighted switched finger-capacitors. The inductor uses a wall of well-grounded metals to provide a good current return-path and help confinement of the field, at the price of more parasitic capacitance and a little lower overall inductance. To reduce the losses due to the eddy currents, any substrate doping under the inductor and any metal loops in the guard rings and the routings have been avoided. The differential inductor has a quality factor of 24 at 34 GHz and a self resonance frequency of 200 GHz .

The switched capacitor uses doughnut-shaped NMOS switches to achieve a high ON to OFF capacitance ratio. As Fig. 3 demonstrates the capacitor array benefits from an innovative design in which a large finger capacitor splits to five binary-weighted capacitors to be used for the digital frequency tuning. The LSB units are positioned in between the MSB units in order to achieve a better accuracy. Conventional unit-cell based arrays suffer from

significant relative accuracy when used for small capacitor sizes. The proposed compact layout results in a better accuracy, a lower parasitic capacitance, and shorter connections to the switches. Effective parallel resistance of the tank is dominated by the capacitive branches, resulting in an overall tank quality factor of 10 at 40 GHz .

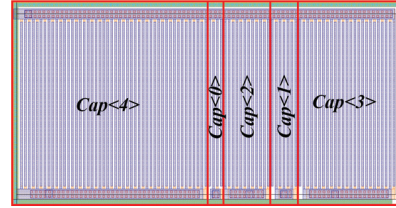


Fig. 3. Layout of the proposed capacitor array consisting of five binary-weighted capacitors in the optimum order.

C. Current Source

The current source is programmable to work in either the linear mode or the saturation mode in order to be able to optimize the overall phase noise. When the current source is in the saturation mode its noise contribution increases, but the contribution of the supply and the cross-coupled pair decrease. In this design, should the current source be set to supply the same amount of current in both modes the linear mode shows a slightly better phase noise.

D. VCO Buffer

A differential cascode buffer has been designed to deliver a 0 dBm LO power to a 50Ω load while isolating the VCO from the load. The VCO buffer also reduces the load pull for the VCO significantly. The operating points are set for an efficient LO power delivery. As shown in Fig. 4 the diffusion regions of the input and the cascode devices have been shared to minimize the parasitic capacitances of the junctions and the routings which create significant loss and current leakage at this common node.

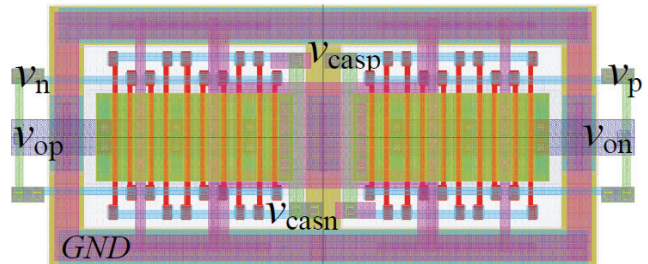


Fig. 4. The unit cell of the differential VCO buffer with five differential pairs of the cascode devices.

A transformer has been used to convert the buffer output impedance of 125Ω , which is optimum for an efficient power delivery, to a 50Ω level at the input of the following stages which can be a mixer and a divider. This feature together with the possibility of having shorter signal feeds to the following stages make the transformer superior to a differential inductor as the VCO buffer load.

E. Common-Mode Nodes

A ground grid covers all the layers of the layout, with the exceptions of the parts which introduce excessive eddy currents or couplings to the sensitive nodes. All Common-Mode (CM) nodes of the circuit have their unnecessary bandwidths suppressed by maintaining low impedance levels to the ground in all frequencies. This requires different sizes of decoupling capacitors to be used at all of the CM nodes and to be repeated in short intervals. This also improves CM noise rejection and CM stability.

There are two CM nodes which do not need extra capacitors: The center tab of the inductor and the voltage control node. At the center tab of the inductor higher impedance levels can suppress the noise of the cross-coupled pair. And the voltage control node has to connect to the loop filter when the VCO is employed by a PLL.

IV. EXPERIMENTAL RESULTS

The measurement results of the switched-capacitor VCO prove that it can satisfy stringent specifications for phase noise, tuning range, and LO power. It covers from 34.29 to 39.88 GHz., a tuning range of 15.1% and has a maximum K_{VCO} of 240 MHz/V. It exhibits a worst case phase noise of -98.1 dBc/Hz at 1-MHz offset from the highest oscillation frequency, as shown in Fig. 5.

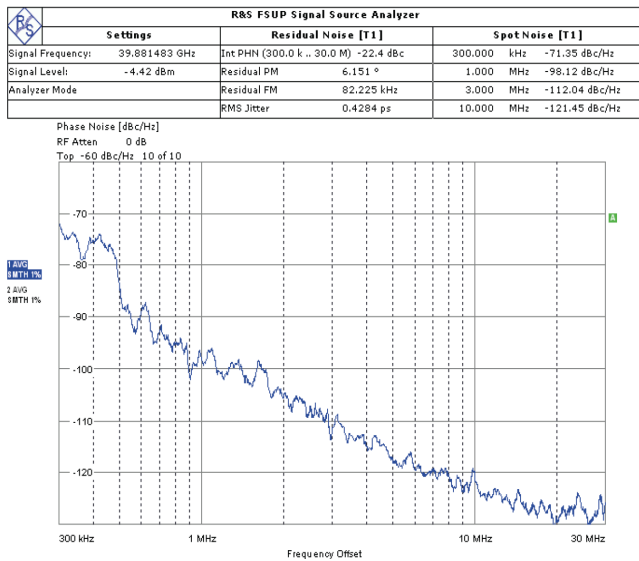


Fig. 5. Phase noise measurement result at 1-MHz offset from 39.88 GHz with 4.5 dB loss in the test equipments.

The VCO consumes 12 mA from a 1.2-V supply and the differential VCO buffer uses 11 mA to deliver a Single-Ended (SE) LO power of 0 dBm to the 50Ω probe. FOM and FOM_T , as defined in (3) and (4), are better than -178.5 dBc/Hz and -182.1 dBc/Hz respectively at 1-MHz offset across the band. Since the VCO operates in the current-

limited mode, using a 0.9-V supply to lower the power consumption improves the FOM_T to -183.4 dBc/Hz. In this case the Single-Ended LO power reduces by 2.5 dB.

$$FOM(\Delta f) = L\{\Delta f\} - 20 \log \left(\frac{f_0}{\Delta f} \right) + 10 \log \left(\frac{P_{DC}}{1mW} \right) \quad (3)$$

$$FOM_T(\Delta f) = FOM(\Delta f) - 20 \log \left(\frac{TR}{10} \right) \quad (4)$$

Where the quantities share the descriptions with (1). P_{DC} is the VCO power dissipation in mW, and TR is the tuning range in percentage.

Across the band, the varactor comprises a small portion of the overall capacitance of the tank. Thus, its undesired effects on the delivered power and the phase noise are minimal. However the digital tuning with 15.1% change in the frequency causes 3 dB change in the phase noise. Fig. 6 summarizes the results of the simulations and the measurements of the VCO versus the digital tuning code when the control voltage is set to the mid-rail.

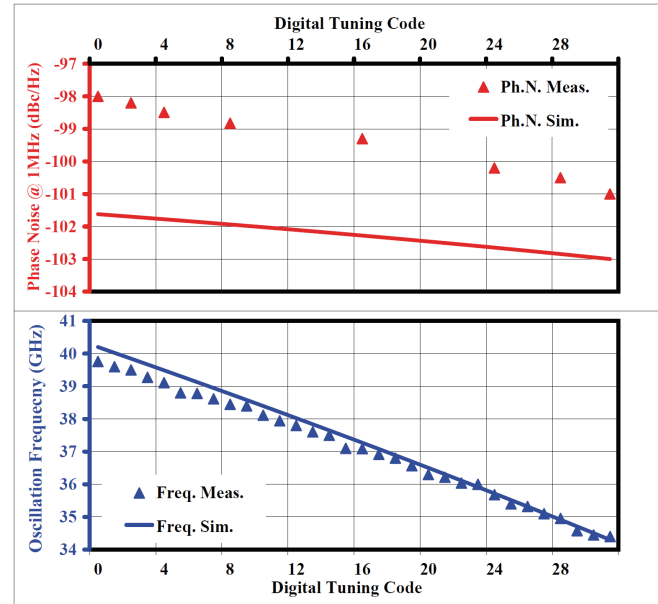


Fig. 6. Summary of the measured and simulated characteristics of the VCO vs. the digital tuning code.

The results of the VCO show significant improvements compared to an earlier version of the design which used only varactors. The varactor-only version measured a tuning range of 5.8% and a K_{VCO} of 2.1 GHz/V.

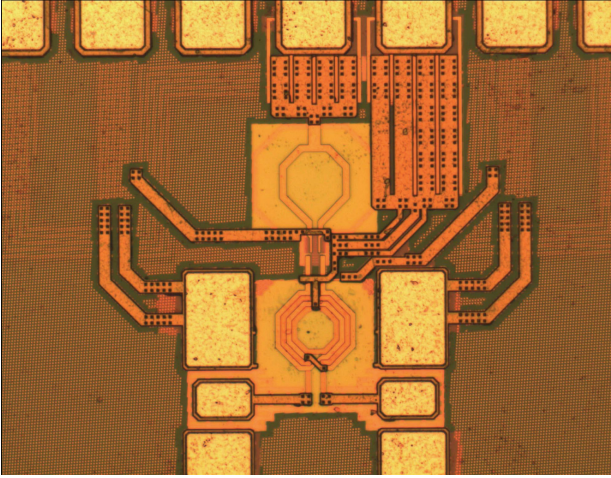
Table I presents a summary of the characteristics of this switched-capacitor VCO in comparison with other recently published mm-wave CMOS VCOs [5]-[9]. The table reports the worst case results of each work.

TABLE I

SUMMARY OF THE SPECIFICATIONS OF THIS DESIGN IN COMPARISON WITH RECENTLY PUBLISHED MM-WAVE CMOS VCOS

Reference	Year	Publ.	Process Technology	Freq. (GHz)	Ph.N.@1MHz (dBc/Hz)	Tuning Range%	PDC (mW)	FOM _T (dB)	Pout (dBm)
[3]	2006	RFIC	CMOS 0.18 μ m	21.6	-101.7	6.25	45	-171.9	-4.2
[5]	2009	VLSI	CMOS 0.13 μ m	47.9	-102.5	1.59	5.6	-172.7	-19
[6]	2009	JSSC	CMOS 90 nm	58.4	-91.0	9.32	8.1	-176.7	-14
[7]	2008	ISSCC	CMOS 90 nm	49.9	-87.0	12	10.4	-172.4	-
[8]	2009	CICC	CMOS 65 nm	60	-97.1	16.7	30	-182.3	-
[9]	2009	IMS	CMOS 90 nm	61	-90.1	9.27	10.6	-174.9	-5
This Work	2010	RFIC	CMOS 65 nm	39.9	-98.1	15.1	14.4	-182.1	0

Fig. 8 shows the micrograph of the 0.15 mm² VCO, including the differential inductor and the transformer along with their guard rings. The DC pads on the top are to supply ground, supply, and the control signals.

Fig. 8. Micrograph of the 300 μ m * 500 μ m VCO.

V. MEASUREMENT CHALLENGES

Probing unlocked high performance mm-wave VCOS for the purpose of phase noise measurements is extremely sensitive to their natural frequency drifts. The range of the frequency drift can exceed the offset frequency range of interest which makes it hard to have reliable low-offset phase noise measurements. Elements like the illuminator's light and mechanical stress or strain are destructive to these measurements. Vibration isolation table, wide probe tips, and wafer probing, as opposed to single die probing, significantly improve the reliability of the measurements.

Phase noise analysis mode of Rohde Schwartz FSUP50 has been used to measure this design. There are some settings which are vitally important. In the measurement setup, manual setting with a RBW of 0.1% increases the chance of success. Tracking and verifying the level and the frequency as well as the AFC should be turned off as they are not designed for unlocked VCOS. A combination of mechanical stability of the setup, quiet environment, and proper instrument settings can make low-offset phase noise measurements of the mm-wave VCOS reliable.

VI. CONCLUSION

The design and implementation of a switched-capacitor VCO in 65nm digital CMOS to cover 34 to 40 GHz has been presented. The measurement results demonstrate a tuning range of 15.1%, a phase noise of better than -98.1 dBc/Hz at 1-MHz offset across the band, a maximum K_{VCO} of 240 MHz/V, and a minimum SE LO power of 0 dBm. The 0.15 mm² VCO can support a mm-wave transceiver with stringent phase noise, tuning range, and LO power delivery specifications.

ACKNOWLEDGEMENT

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II. ARCHITECTURE AND TOPOLOGY

Several architectures have been evaluated including Colpitts in terms of their achievable FOM. As shown in Fig. 1 a cross-coupled VCO architecture with doughnut-shaped grounded-gate NMOS pair has been chosen due to its superior power and area efficiency. A combination of switched capacitors and accumulation-mode varactors comprise the variable capacitance of the tank. A shared-diffusion cascode buffer with a balanced transformer load delivers the LO signal to the probe pads.

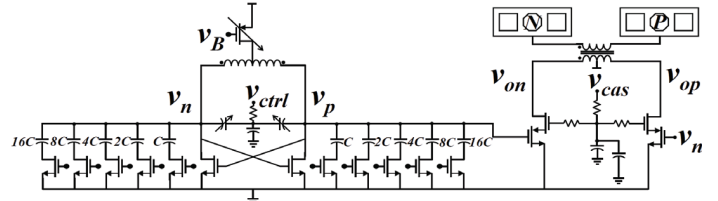


Fig. 1. Simplified schematic of the VCO and its buffer.

Using only varactors to achieve a large tuning range for the VCO results in a high K_{VCO} which as (2) indicates increases the AM to PM conversion gain which in turn causes high phase noise and spurious signal levels. In this work using the switched-capacitors has helped in reducing the K_{VCO} and increasing the tuning range significantly.

$$\Phi_{PM}(f_0 + f_{AM}) = \left[\frac{K_{VCO}}{2f_{AM}} \right] \cdot V_{AM}(f_{AM}) \quad (2)$$

Where Φ_{PM} is the level of the PM signal at the output of the VCO oscillating at the frequency of f_0 , in response to an AM disturbance voltage with amplitude of V_{AM} and frequency of f_{AM} .

The reliability concerns of deep sub-micron processes make the VCO operate in the current-limited mode. Using a PMOS current source is optimum for biasing the VCO in this mode. This is also to provide the VCO buffer with a proper DC bias needed for an efficient LO power delivery.

III. CIRCUIT DESIGN AND IMPLEMENTATION

Detailed descriptions of the VCO components and explanations of the design are presented in this section.

A. VCO Core

Doughnut transistors comprised of square-shaped polysilicon gates are used for the VCO cross-coupled pair. This reduces the contribution of the drain junction capacitors to less than 5% of the overall tank capacitance. Size selection for the core devices has been done based on four different factors: gain, Noise Figure (NF), current switching capability, and efficient power delivery by providing a proper bias to the VCO buffer. The optimum current density for the lowest NF depends on the lateral electric field in the channel [4]. For the process of this VCO, a current density of $0.35 \text{ mA}/\mu\text{m}$ results in a suitable performance from all of the mentioned aspects.

Fig. 2 shows the unit cell of the VCO core with an optimal layout. The layout of the transistors should be optimized in order to achieve an optimal performance in terms of f_{max} , maximum stable gain, and the noise figure. Wider routings cause larger parasitic capacitances and couplings, while narrower interconnections create larger series resistances and inductances.

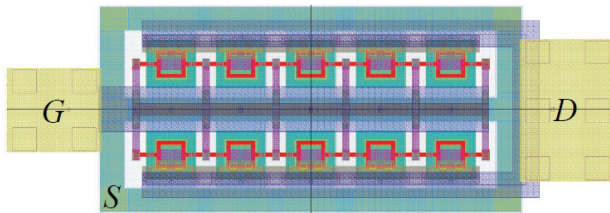


Fig. 2. Layout of the unit cell of the VCO core containing ten doughnut-shaped transistors with optimized routings.

B. Resonant Tank

The resonant tank is composed of a 135 pH differential octagonal-shaped inductor, accumulation-mode varactors and 5-bit binary-weighted switched finger-capacitors. The inductor uses a wall of well-grounded metals to provide a good current return-path and help confinement of the field, at the price of more parasitic capacitance and a little lower overall inductance. To reduce the losses due to the eddy currents, any substrate doping under the inductor and any metal loops in the guard rings and the routings have been avoided. The differential inductor has a quality factor of 24 at 34 GHz and a self resonance frequency of 200 GHz .

The switched capacitor uses doughnut-shaped NMOS switches to achieve a high ON to OFF capacitance ratio. As Fig. 3 demonstrates the capacitor array benefits from an innovative design in which a large finger capacitor splits to five binary-weighted capacitors to be used for the digital frequency tuning. The LSB units are positioned in between the MSB units in order to achieve a better accuracy. Conventional unit-cell based arrays suffer from

significant relative accuracy when used for small capacitor sizes. The proposed compact layout results in a better accuracy, a lower parasitic capacitance, and shorter connections to the switches. Effective parallel resistance of the tank is dominated by the capacitive branches, resulting in an overall tank quality factor of 10 at 40 GHz .

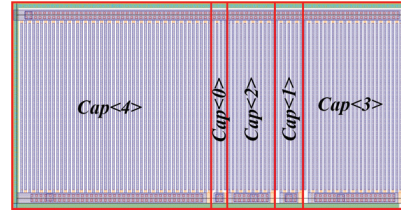


Fig. 3. Layout of the proposed capacitor array consisting of five binary-weighted capacitors in the optimum order.

C. Current Source

The current source is programmable to work in either the linear mode or the saturation mode in order to be able to optimize the overall phase noise. When the current source is in the saturation mode its noise contribution increases, but the contribution of the supply and the cross-coupled pair decrease. In this design, should the current source be set to supply the same amount of current in both modes the linear mode shows a slightly better phase noise.

D. VCO Buffer

A differential cascode buffer has been designed to deliver a 0 dBm LO power to a 50Ω load while isolating the VCO from the load. The VCO buffer also reduces the load pull for the VCO significantly. The operating points are set for an efficient LO power delivery. As shown in Fig. 4 the diffusion regions of the input and the cascode devices have been shared to minimize the parasitic capacitances of the junctions and the routings which create significant loss and current leakage at this common node.

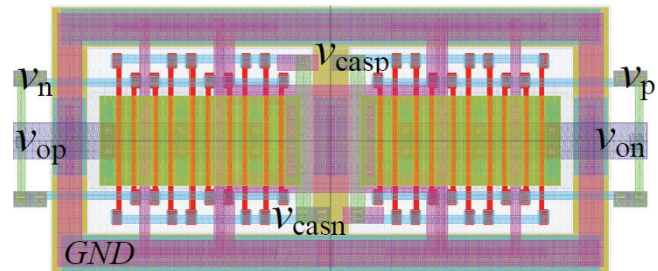


Fig. 4. The unit cell of the differential VCO buffer with five differential pairs of the cascode devices.

A transformer has been used to convert the buffer output impedance of 125Ω , which is optimum for an efficient power delivery, to a 50Ω level at the input of the following stages which can be a mixer and a divider. This feature together with the possibility of having shorter signal feeds to the following stages make the transformer superior to a differential inductor as the VCO buffer load.

E. Common-Mode Nodes

A ground grid covers all the layers of the layout, with the exceptions of the parts which introduce excessive eddy currents or couplings to the sensitive nodes. All Common-Mode (CM) nodes of the circuit have their unnecessary bandwidths suppressed by maintaining low impedance levels to the ground in all frequencies. This requires different sizes of decoupling capacitors to be used at all of the CM nodes and to be repeated in short intervals. This also improves CM noise rejection and CM stability.

There are two CM nodes which do not need extra capacitors: The center tab of the inductor and the voltage control node. At the center tab of the inductor higher impedance levels can suppress the noise of the cross-coupled pair. And the voltage control node has to connect to the loop filter when the VCO is employed by a PLL.

IV. EXPERIMENTAL RESULTS

The measurement results of the switched-capacitor VCO prove that it can satisfy stringent specifications for phase noise, tuning range, and LO power. It covers from 34.29 to 39.88 GHz., a tuning range of 15.1% and has a maximum K_{VCO} of 240 MHz/V. It exhibits a worst case phase noise of -98.1 dBc/Hz at 1-MHz offset from the highest oscillation frequency, as shown in Fig. 5.

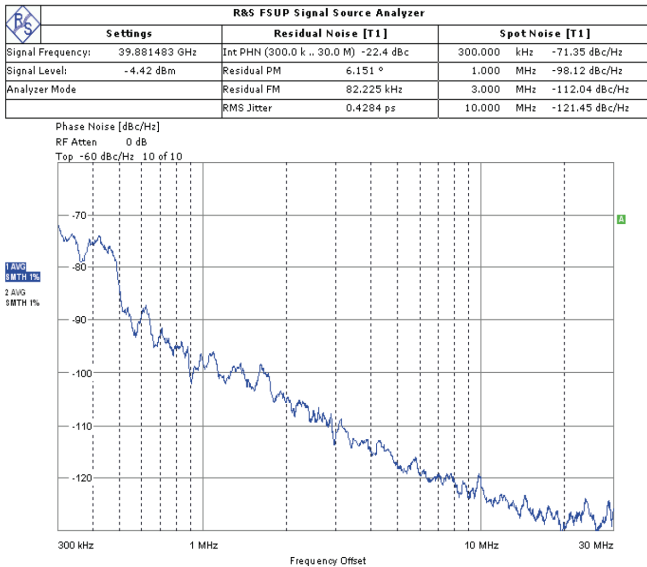


Fig. 5. Phase noise measurement result at 1-MHz offset from 39.88 GHz with 4.5 dB loss in the test equipments.

The VCO consumes 12 mA from a 1.2-V supply and the differential VCO buffer uses 11 mA to deliver a Single-Ended (SE) LO power of 0 dBm to the 50Ω probe. FOM and FOM_T , as defined in (3) and (4), are better than -178.5 dBc/Hz and -182.1 dBc/Hz respectively at 1-MHz offset across the band. Since the VCO operates in the current-

limited mode, using a 0.9-V supply to lower the power consumption improves the FOM_T to -183.4 dBc/Hz. In this case the Single-Ended LO power reduces by 2.5 dB.

$$FOM(\Delta f) = L\{\Delta f\} - 20 \log \left(\frac{f_0}{\Delta f} \right) + 10 \log \left(\frac{P_{DC}}{1mW} \right) \quad (3)$$

$$FOM_T(\Delta f) = FOM(\Delta f) - 20 \log \left(\frac{TR}{10} \right) \quad (4)$$

Where the quantities share the descriptions with (1). P_{DC} is the VCO power dissipation in mW, and TR is the tuning range in percentage.

Across the band, the varactor comprises a small portion of the overall capacitance of the tank. Thus, its undesired effects on the delivered power and the phase noise are minimal. However the digital tuning with 15.1% change in the frequency causes 3 dB change in the phase noise. Fig. 6 summarizes the results of the simulations and the measurements of the VCO versus the digital tuning code when the control voltage is set to the mid-rail.

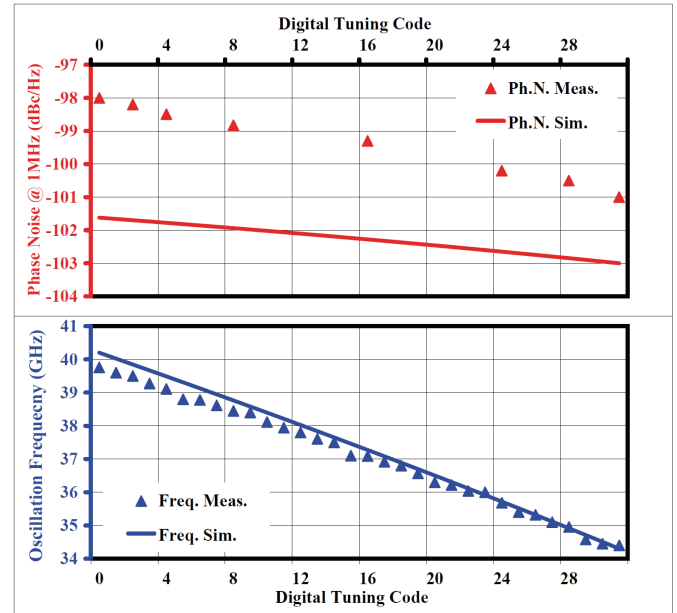


Fig. 6. Summary of the measured and simulated characteristics of the VCO vs. the digital tuning code.

The results of the VCO show significant improvements compared to an earlier version of the design which used only varactors. The varactor-only version measured a tuning range of 5.8% and a K_{VCO} of 2.1 GHz/V.

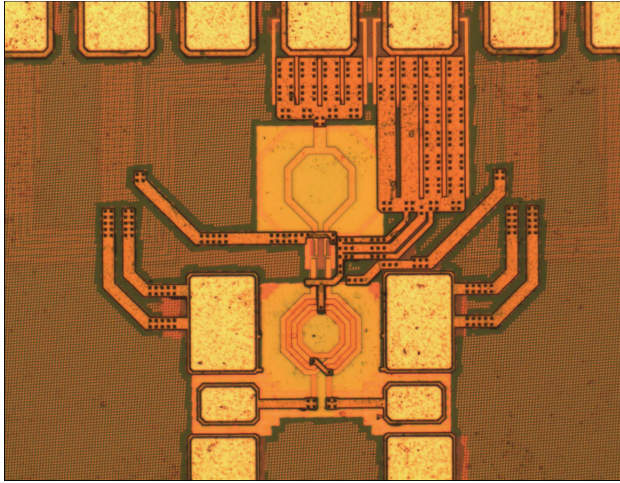
Table I presents a summary of the characteristics of this switched-capacitor VCO in comparison with other recently published mm-wave CMOS VCOs [5]-[9]. The table reports the worst case results of each work.

TABLE I

SUMMARY OF THE SPECIFICATIONS OF THIS DESIGN IN COMPARISON WITH RECENTLY PUBLISHED MM-WAVE CMOS VCOS

Reference	Year	Publ.	Process Technology	Freq. (GHz)	Ph.N.@1MHz (dBc/Hz)	Tuning Range%	PDC (mW)	FOM _T (dB)	Pout (dBm)
[3]	2006	RFIC	CMOS 0.18 μm	21.6	-101.7	6.25	45	-171.9	-4.2
[5]	2009	VLSI	CMOS 0.13 μm	47.9	-102.5	1.59	5.6	-172.7	-19
[6]	2009	JSSC	CMOS 90 nm	58.4	-91.0	9.32	8.1	-176.7	-14
[7]	2008	ISSCC	CMOS 90 nm	49.9	-87.0	12	10.4	-172.4	-
[8]	2009	CICC	CMOS 65 nm	60	-97.1	16.7	30	-182.3	-
[9]	2009	IMS	CMOS 90 nm	61	-90.1	9.27	10.6	-174.9	-5
This Work	2010	RFIC	CMOS 65 nm	39.9	-98.1	15.1	14.4	-182.1	0

Fig. 8 shows the micrograph of the 0.15 mm² VCO, including the differential inductor and the transformer along with their guard rings. The DC pads on the top are to supply ground, supply, and the control signals.

Fig. 8. Micrograph of the 300 μm * 500 μm VCO.

V. MEASUREMENT CHALLENGES

Probing unlocked high performance mm-wave VCOS for the purpose of phase noise measurements is extremely sensitive to their natural frequency drifts. The range of the frequency drift can exceed the offset frequency range of interest which makes it hard to have reliable low-offset phase noise measurements. Elements like the illuminator's light and mechanical stress or strain are destructive to these measurements. Vibration isolation table, wide probe tips, and wafer probing, as opposed to single die probing, significantly improve the reliability of the measurements.

Phase noise analysis mode of Rohde Schwartz FSUP50 has been used to measure this design. There are some settings which are vitally important. In the measurement setup, manual setting with a RBW of 0.1% increases the chance of success. Tracking and verifying the level and the frequency as well as the AFC should be turned off as they are not designed for unlocked VCOS. A combination of mechanical stability of the setup, quiet environment, and proper instrument settings can make low-offset phase noise measurements of the mm-wave VCOS reliable.

VI. CONCLUSION

The design and implementation of a switched-capacitor VCO in 65nm digital CMOS to cover 34 to 40 GHz has been presented. The measurement results demonstrate a tuning range of 15.1%, a phase noise of better than -98.1 dBc/Hz at 1-MHz offset across the band, a maximum K_{VCO} of 240 MHz/V, and a minimum SE LO power of 0 dBm. The 0.15 mm² VCO can support a mm-wave transceiver with stringent phase noise, tuning range, and LO power delivery specifications.

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Exhibit 1005

Low-Voltage Radio-Frequency CMOS Integrated Circuits in Silicon-On-Insulator

by

Neric H. W. Fong

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment
of the requirements for the degree of Doctor of Philosophy in Engineering

Ottawa-Carleton Institute for Electrical Engineering

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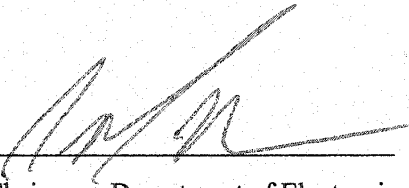
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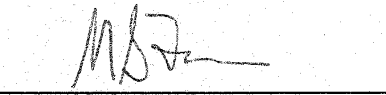
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Carleton University

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Abstract

This thesis examines the advantages of silicon-on-insulator (SOI) CMOS for low-voltage radio-frequency (RF) application. It explores the unique properties of SOI transistors, exploiting these properties to construct RF circuits with better performance (such as higher speed lower noise) compared to bulk CMOS. The cross-coupled complementary voltage-controlled oscillator (VCO) was chosen as the baseline circuit for the comparison.

First, a wideband VCO using AMOS varactors with more than 50% tuning range was implemented, demonstrating the low-voltage frequency tuning capability in CMOS. Next, a 40 GHz VCO using both PMOS and NMOS was constructed to illustrate the high speed performance of SOI CMOS transistors. High-speed design issues, especially regarding frequency tuning capability, have been studied and analyzed. While AMOS varactors make low-voltage tuning in CMOS possible, the high varactor sensitivity introduces excessive phase noise into the system. This thesis explores and analyzes this noise problem. Two design methodologies, namely band-switching and differential tuning, were employed to reduce such noise. Furthermore, a general phase noise improvement technique, which can be applied to both SOI and bulk CMOS VCOs, was also developed and demonstrated. This technique utilizes the complementary topology to reduce upconversion flicker noise, while using the non-minimum gate length NMOS devices to maximize signal swing and reduce transistor noise. All the VCOs described above are implemented in a 0.13 μm SOI CMOS technology, and the theories developed were verified experimentally by these RF circuits.

Finally, several high-speed low-voltage circuits are either simulated or implemented to demonstrate the improved circuit performance available with SOI: (a) a bias-T source follower for accurate high-speed VCO measurement; (b) a 5.4 GHz low-noise amplifier with image reject using high- Q passives, giving zero dc power dissipation for the image reject circuit; (c) a 1 V, 40 μW , 50 MHz, 6-bit, $\Delta\Sigma$ analog-to-digital converter (ADC) to demonstrate low-voltage switched-C performance; and (d) a 1 V, 5 GHz, 3-bit pipeline ADC used as a multi-bit quantizer for future $\Delta\Sigma$ bandpass ADC implementation.

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First, I would like to thank my supervisors Sir Calvin Plett and Sir Garry Tarr for their constant support and endless patience throughout my Ph. D. program. Calvin's knowledge in circuit design and Garry's expertise in fabrication and device physics have broadened my knowledge in integrated circuits. Their financial support in terms of travel reimbursement is also greatly appreciated (San Francisco, New York, Orlando, Seattle, and Hawaii). Thanks Sirs!

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