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List of Symbols and Terms

ADC	Analog-to-Digital Convertor
AMOS	Accumulation Metal-Oxide-Semiconductor
BiCMOS	Bipolar and Complementary Metal-Oxide Semiconductor
C	capacitor or capacitance [F]
C_{box}	buried oxide capacitance per area [F/m^2]
C_{d}	depletion capacitance [F/m^2]
C_{in}	input capacitance [F]
C_{JSD}	source/drain junction capacitor per area [F/m^2]
C_{ox}	gate oxide capacitance per area [F/m^2]
C_{Si}	depletion capacitance in channel [F/m^2]
C_{v}	varactor capacitance [F]
CAD	Computer-Aided Design
CLK	clock signal
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Convertor
DSP	Digital Signal Processing
Δf	delta frequency from the carrier [Hz]
$\Delta\Sigma$	delta-sigma
DIBL	Drain Induced Barrier Lowering
DSP	Digital Signal Processing
DUT	Device Under Test
EM	Electro-Magnetic
E_{n}	electric field in direction n [V/m]
ϵ_0	permittivity of air
ϵ_{e}	effective permittivity
ϵ_{ox}	relative permittivity of silicon dioxide [F/m]
ϵ_{r}	relative permittivity
ϵ_{Si}	relative permittivity of silicon [F/m]
F	noise factor
ϕ	phase deviation
ϕ_{B}	built-in voltage of p-n junction [V]
f_{c}	flicker noise corner frequency [Hz]
f_{m}	frequency offset [Hz]
F_{min}	minimum noise factor
f_{o}	carrier or centre frequency [Hz]
f_{s}	sampling frequency [Hz]
f_{T}	cut-off frequency [Hz]
FDSOI	Fully-Depleted Silicon-On-Insulator
g_{DS}	output conductance [Ω]

g_m	transconductance [A/V]
G_{max}	maximum achievable power gain [dB]
Γ_{min}	minimum reflection coefficient [V/V]
Γ_{opt}	optimum noise reflection coefficient [V/V]
G	gain [dB]
G_p	available power gain [dB]
HBT	Heterojunction Bipolar Transistor
HD	Harmonic Distortion [dB]
HICUM	Hi-Current Model
I_{DD}	drain current
I_f	flicker noise current
I_s	saturation current [A or A/m ²]
IIP3	input third-order intercept point [dBm]
IP3	third-order intercept point [dBm]
IR	Image Reject
ISF	Impulse Sensitivity Function
k	Boltzmann's constant [eV/K]
k_p	process constant of MOSFET [A/V ²]
k_V	varactor gain [F/V]
k_{VCO}	VCO gain [Hz/V]
L	inductor or inductance [H]
l	length of MOS device [m]
λ	channel modulation [V ⁻¹]
$\mathcal{L}(f)$	phase noise [dBc/Hz]
LNA	low-noise amplifier
LO	local oscillator
m	number of fingers in MOSFET
MIM	metal-insulator-metal
MOSFET	Metal-Oxide Semiconductor Field Effective Transistor
M_n	MOS transistor n
N_A	p-type doping concentration [cm ⁻³]
N_D	n-type doping concentration [cm ⁻³]
n_i	carrier concentration of intrinsic silicon [cm ⁻³]
NF	Noise Figure [dB]
NF_{min}	minimum noise figure [dB]
PDSOI	Partially Depleted Silicon-On-Insulator
OSR	OverSampling Ratio
Q	quality factor
q	electron charge [C]
q_d	phase deviation [rad]
ρ	resistivity [Ω -cm]
PLL	Phase-Locked Loop

P_S	signal power [W]
R_{ch}	channel resistance [Ω]
r_o	output impedance of MOSFET [Ω]
RF	Radio Frequency
rms	root mean square
R_s	series resistance [Ω]
S	subthreshold swing
S_{ij}	2-port s-parameter of port i,j
SGPM	Spice Gummel-Poon Model
SiGe	Silicon Germanium
SiO_2	silicon dioxide
SNDR	Signal-to-Noise/Distortion Ratio [dB]
SNR	Signal-to-Noise Ratio [dB]
SOI	Silicon-On-Insulator
T	temperature [K]
t_{box}	buried gate oxide thickness [m]
t_{depl}	depletion width [m]
t_{ox}	gate oxide thickness [m]
v_C	varactor control voltage [V]
VCO	Voltage-Controlled Oscillator
V_D	voltage drop across a diode
V_{DD}	supply voltage [V]
v_n	noise voltage
v_{on}	transistor on-voltage, given by $V_{GS} - V_{th}$ [V]
V_R	reversed-bias voltage for a p-n junction [V]
v_p	phase velocity [ms^{-1}]
V_T	thermal voltage, about 26mV at room temperature [V]
V_{th}	threshold voltage [V]
v_{tune}	varactor tuning voltage [V]
VLSI	Very Large Scale Integration
w	width of MOS device [μm]
ω	frequency in radian [rad/s]
Y	admittance [Ω^{-1}]
Y_S	source or input admittance [Ω^{-1}]
Y_{opt}	optimum noise admittance [Ω^{-1}]
Z	impedance [Ω]
Z_0	characteristic impedance [Ω]

Chapter 1 Introduction

In this thesis, the advantages of silicon-on-insulator (SOI) transistors for radio frequency (RF) circuits are explored. Several bottlenecks that were imposed by traditional bulk CMOS technology are resolved, making CMOS a feasible technology for single chip integration of RF systems.

1.1 Why RF CMOS?

Recently, the telecommunication industry has been seeking a means of integrating the RF frontend and the digital-oriented backend of wireless communication systems onto a single chip for economic reasons. For a silicon process, heterojunction bipolar transistors (HBT) are used for the high-speed RF frontend, while CMOS is used for the DSP at the backend. The HBT has better device performance in terms of gain, speed and noise. However, it is more expensive to fabricate¹, and cannot replace the CMOS DSP at the backend due to a relatively high power dissipation in the static state (i.e., power is drained even though the device is not switching). Therefore, the focus of the integration solution has shifted towards the replacement of HBT by CMOS, especially with the emergence of deep submicron lithography, which makes the speed of CMOS approach that of HBTs. However, when operating at RF frequencies (above 1 GHz), larger power consumption is usually required for CMOS to achieve comparable performance to the HBT technology [Voi95].

1. Cost in terms of number of fabrication steps and yield.

Since power consumption is usually the prime concern in mobile communication, *single chip integration* is the major reason for using CMOS for RF blocks. Otherwise, the industry should remain with the traditional HBT devices for RF circuits to take advantage of their better device performance.

1.2 Motivation

One approach for single-chip integration is to implement all radio functions in CMOS¹. This approach takes advantage of the high state of development of CMOS technology, driven by the enormous market for high-performance digital CMOS circuits. With the development of deep submicron lithography, the speed of CMOS transistors is now comparable to modern HBT processes, making the implementation of RF functions feasible in CMOS technology. However, the shrinking of feature size forces the supply voltage to scale down to ensure reliability. Therefore, RF CMOS design is usually considered as a high-speed low-voltage design.

The outlook for RF CMOS has improved recently with the maturation of a special branch of CMOS technology called silicon-on-insulator (SOI). SOI CMOS is similar to traditional bulk CMOS transistors except the body silicon is isolated by a layer of silicon dioxide, reducing the junction capacitance, hence making the transistor about 30% faster than in bulk [Sha99]. In this thesis, besides demonstrating the technology advantage in terms of speed improvement of SOI, special properties of this type of transistor are utilized to improve circuit performance, resolving some of the high-speed low-voltage design bottlenecks in bulk RF CMOS as described below.

- **Poor frequency tuning of a VCO at low-voltage**

One of the major bottlenecks in RF CMOS design is the limited frequency tuning range of the VCO. While the gain (or sensitivity, defined as the ratio of capacitance change to applied voltage) of a traditional pn diode varactor remains constant, the tuning voltage decreases due to the voltage supply reduction imposed by technology limitations. Therefore, a low-voltage VCO requires a different type of varactor with high C_{max}/C_{min} ratio to maintain the desired tuning range.

1. Another one is using BiCMOS technology.

Although this type of varactor can be realized in bulk technology, its performance is much better in SOI, as will be described in the thesis.

- **Excessive phase noise due to high gain varactor of low-voltage VCO**

A low-voltage VCO requires a high gain varactor for frequency tuning. However, a high gain varactor introduces excess phase noise into the system, degrading the performance of the VCO significantly. This problem is obvious but is often overlooked in VCO design. Therefore, in this thesis, the relationship between varactor gain and phase noise is analyzed, and then an SOI-based solution that reduces the effect of this problem will be provided.

- **Poor phase noise due to gate length and voltage supply reduction in VCO**

A transistor with a smaller gate length has worse flicker noise than a long channel device. Therefore, using minimum gate length results in worse flicker noise, which is upconverted near the VCO carrier [Haj99]. Such upconversion can be minimized by exploiting symmetry in the output waveform, but this may result in an undesirable dc level shift, such that the output swing is not at its maximum. With a low supply voltage, the VCO output swing has to be maximized to improve the signal-to-noise ratio (SNR) of the system to achieve reasonable phase noise performance. Waveform symmetry and output maximization are effectively two contradictory conditions, but in this thesis, a new circuit technique is developed such that both conditions can be met simultaneously. This technique can be used for both bulk and SOI CMOS technology.

- **Poor frequency tuning of very high speed VCO**

Although very high speed VCOs up to 50 GHz have been demonstrated in bulk CMOS [Hun00b][Wan01], the tuning ranges are so poor (less than 2%) that the designs are unsuitable for commercial realization. The poor tuning range is the result of the high parasitic capacitance of bulk transistors and the lack of high- Q , high C_{max}/C_{min} ratio varactors. In this thesis, the shortcomings of bulk CMOS are resolved by using SOI transistors, and a 40 GHz VCO with adequate tuning range (9 to 15%) was implemented in SOI to demonstrate the advantage of this technology at very high speed.

- **Inaccurate measurement of low-voltage VCO due to losses in the output buffer**

In order to drive a $50\ \Omega$ load for measurement, source followers are usually added to the VCO as the output buffers. At low voltage, large-size transistors are required to provide enough current to drive the load because v_{on} is small. However, large drivers have high parasitic capacitance, which reduces the speed of the VCO. At high frequency, for example at 40 GHz, this imposes a significant problem for oscillation frequency and output power measurement. In this thesis, a unique property of SOI is exploited to allow more accurate measurements of the VCO.

- **Design flexibility of low-noise amplifier (LNA) in deep submicron SOI**

Before the introduction of submicron technology, the performance of CMOS LNAs was limited by the speed of the transistor. Deep-submicron SOI technology offers an extremely high speed transistor that not only provides enough gain at high frequency but also relaxes design constraints, which makes a high-speed high-performance LNA feasible. In this thesis, a 5.4 GHz simultaneous noise and power matched LNA with image rejection was designed to demonstrate this design flexibility.

- **Reduced dynamic range of analog circuits at low voltage**

The reduced voltage supply decreases the output signal swing, and this makes it challenging to achieve wide dynamic range at high speeds. In this thesis, a 50 MHz switched-C $\Delta\Sigma$ analog-to-digital converter (ADC) was designed and operated down to 0.9 V supply to examine the limitations of dynamic range and circuit noise at low voltage. At this supply voltage, the circuit only draws 40 μW for 6-bit performance, demonstrating the low power capability of SOI.

- **Reduced speed of transistors at low voltage**

A high frequency circuit requires the transistors to operate in the saturation region to provide enough speed for the circuit. However, low voltage operation sometimes forces the device to run either in the triode or the subthreshold region, degrading the speed of the transistor. In this thesis, a 1 V, 5 GHz, 3-bit pipelined ADC was designed as an example. The design was such that some of the transistors were required to operate in the triode mode, and a low-voltage circuit technique was introduced to address this problem.

1.3 Contributions

This thesis examines the advantages of SOI CMOS technology for low-voltage RF application. The circuits implemented are mainly for theory verification and technology demonstration. Although the circuits are not targeted at particular specifications, they are designed at the frequency around 5 GHz for possible wireless local area network (WLAN) applications. Contributions of this work include:

Passive components:

- design, analysis and measurement of high- Q AMOS varactors;
- design and implementation of horseshoe inductor in silicon with single-ended Q greater than 20 at frequencies between 3 and 5 GHz [Zam01];
- design and implementation of multi-level multi-turn RF choke with 17 nH inductance that only occupies an area of 140 μm by 140 μm .

Voltage-controlled oscillators:

- analysis of the relationship between phase noise and varactor gain at low voltage;
- broadband frequency tuning (more than 50% tuning range) using AMOS varactors with band-switching topology in SOI [Fon02a];
- application of differentially tuned varactor to reduce common-mode noise and hence phase noise in SOI [Fon02b];
- introduction of a novel design technique called “simultaneous g_m and impedance matching” for phase noise improvement in deep submicron CMOS technology [Fon02d];
- design and implementation of a 40 GHz complementary VCO that demonstrates frequency tuning capability and speed of PMOS in SOI [Fon02c];
- application of bias-T source follower in SOI for accurate high-speed circuit measurement;

Low-noise amplifiers:

- theory and analysis of simultaneous noise and power matching in deep submicron CMOS;
- design and implementation of a 1 V, 5.4 GHz LNA with a novel zero-dc power image rejection circuit in SOI;

Analog-to-digital converters:

- testing of a low-voltage 50 MHz $\Delta\Sigma$ ADC in SOI to examine the low power capability of SOI for analog circuits [Swa99];
- design of a 1 V, 5 GHz, 3-bit pipeline ADC with a novel digital correction technique to compensate for low-speed transistors operating in the triode region.

1.4 Thesis Outline

Chapter 1 is the introduction of the thesis.

Chapter 2 gives a brief background of SOI devices and the process technology used in this thesis.

Chapter 3 outlines the design of the passives such as inductors and varactors that are used in the RF circuits. Design and measurement of very high Q inductors and varactors are described, and an RF AMOS varactor is analyzed.

Chapter 4 contains the designs of the VCOs. Three novel design techniques, (a) band-switching, (b) differentially-tuned varactor, and (c) simultaneous g_m and impedance matching, are introduced to improve phase noise and the frequency tuning range. Furthermore, the design of a very high frequency (40 GHz) VCO is discussed, together with the design of a high speed buffer. Measurement of each VCO is given for theory verification.

Chapter 5 contains the designs of the LNAs, including a novel all-passive image rejection filter utilizing the high quality passives described in Chapter 3. Some of the high frequency and matching issues for both power and noise for submicron CMOS technology are also discussed.

Chapter 6 contains the designs of mixed-signal analog circuits. The designs include the world's first SOI low-pass second-order ADC (measured), and a 3-bit, 5 gigabit/second quantizer (simulation). All of the circuits are designed at 1 V to demonstrate the low-voltage capability of SOI in mixed-signal design.

Chapter 7 is the thesis conclusion and the proposal of future work.

Chapter 2 SOI Devices

SOI CMOS technology has been in commercial use for over a decade. Although SOI offers significant performance advantages over bulk CMOS, until very recently SOI remained a niche technology, relegated to limited applications such as radiation-hard circuitry. The reluctance for the microelectronics industry to adopt SOI CMOS was based in large measure on an unwillingness to risk investment in new technology when comparable performance advantages could be achieved simply by scaling bulk CMOS to smaller gate lengths. SOI CMOS also suffered from high substrate costs and floating body effects which complicated device and circuit modeling. Conversion from bulk to SOI CMOS requires major changes in device models, CAD tools (e.g. layout synthesis), cell libraries and even system architecture, all of which are extremely costly. Recently the exponentially rising cost and difficulty of scaling bulk CMOS technology beyond the 0.25 μm generation has led to the acceptance of SOI as a commercially viable alternative.

The RF frontend has traditionally been constructed using III-V devices, particularly gallium arsenide based technology. Recently, SiGe-based HBT devices have begun to take part of the market share for its comparable circuit performance, reduction in cost and better production yield. Silicon-based CMOS cannot compete in performance with either of the devices mentioned above. Despite the reduction of gate length in CMOS which allows the device to achieve similar cut-off frequency f_T (i.e., speed), short-channel effects significantly hinder the analog performance of the

MOSFET. However, RF CMOS does attract a lot of attention in both academia and industry these days. Driven by the market demand such as Bluetooth, a single-chip system has become the holy grail for telecommunications products. Since CMOS is the most economical and practical choice for the digital backend (e.g., DSP and memory), the technology options left for such integration are CMOS and BiCMOS. Since BiCMOS is inherently a more expensive process, CMOS has the advantage for economic reasons. Therefore, the philosophy behind RF CMOS is single-chip integration, with the result that designers utilize an inferior technology to achieve the required specifications for economic advantage.

2.1 SOI vs. Bulk

Before performing a comparison between bulk and SOI devices, first consider the physical structure of an SOI MOSFET as shown in Figure 2.1. Compared with a bulk MOSFET, there is a layer of buried oxide that separates the silicon bulk into two regions called the body and the substrate. There are three methods used commercially to form such a buried oxide [Kuo98]. The simplest and most widely used way is to implant oxygen ions into the silicon and thermally anneal the wafer to repair the damage to the body silicon crystal structure. The body silicon is usually very thin, ranging from 100 nm for partially-depleted SOI (PDSOI), to around 20 nm for fully-depleted SOI (FDSOI). The latter films are formed by silicon thinning through sacrificial oxidation [Kuo98] (see Section 2.2 for further detail). The buried oxide is about 300 nm for an older process and 100 nm for a more modern process. The electrical properties for both body silicon and buried oxide are discussed in a later section.

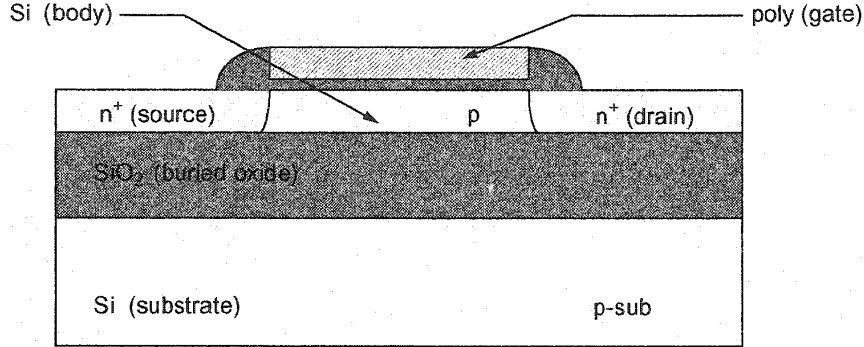


Figure 2.1 Device Structure of a n-type SOI MOSFET

Other than the creation of the buried oxide, the rest of the processing steps are practically the same¹ as in the bulk CMOS. Therefore, (a) formation of the buried oxide film and (b) body silicon thinning (for FDSOI) are the two extra fabrication steps incurred in SOI compared to bulk CMOS.

Perhaps the most obvious advantage of introducing the buried oxide is the reduction of the area junction capacitance C_{JSD} under the source/drain regions. In bulk CMOS, the capacitance is formed mainly by the depletion region of the reverse biased pn junction under the source-drain diffusion. Assuming a simple parallel plate structure with no fringing field, the capacitance per unit area is therefore

$$C_{JSD} = \frac{\epsilon_{si}\epsilon_0}{t_{depl}} \quad (2.1)$$

where ϵ_{si} is the relative permittivity of the silicon, ϵ_0 is the permittivity of air, and t_{depl} is the depletion width (for n-type MOSFETs) given by

$$t_{depl} = \left[\frac{2\epsilon_{si}\epsilon_0(\phi_B + V_R)}{q} \cdot \frac{N_D}{N_A(N_A + N_D)} \right]^{1/2} \quad (2.2)$$

1. In fact, the isolation is easier to fabricate in SOI because of the buried oxide.

where V_R is the reverse bias voltage, q is the charge of an electron, N_A and N_D the dopings of the p-type and the n-type materials respectively. ϕ_B is the built-in voltage of a pn junction given by

$$\phi_B = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right) \quad (2.3)$$

where V_T is the thermal voltage (which is about 26 mV at room temperature), and n_i is the carrier concentration of intrinsic silicon. Assuming a p-well doping $N_A = 10^{17} \text{ cm}^{-3}$ for a modern submicron process¹, and $N_D = 10^{21} \text{ cm}^{-3}$, t_{depl} is around 0.1 μm at zero bias, and C_{JSD} is about 9.1 $\mu\text{F}/\text{m}^2$.

In SOI, the area capacitance results from buried oxide instead of the depletion region. The buried oxide thickness t_{box} for a modern process is about 0.1 μm (which is approximately equal to t_{depl} if not thicker), but the relative permittivity of oxide ϵ_{ox} is 3.9, which is about three times smaller than silicon's ϵ_{si} of 11.8. Therefore, the C_{JSD} of SOI is at least three times smaller than that of the bulk process. For this reason, the SOI transistor is about 20-30% faster than traditional bulk devices [Sha99].

From the dc point of view, the buried oxide provides isolation from neighbouring devices. Therefore, adverse effects such as latch-up and body effect are absent in SOI. Furthermore, the designer is allowed to bias the source/drain node to a voltage below the substrate voltage (usually ground) without worrying about forward biasing the source/drain-substrate pn junction, which provides an extra level of design flexibility. This flexibility is applied in the design of an AMOS varactor (Chapter 3) and buffer (Chapter 4).

1. The doping for the substrate is relatively high for modern submicron process to suppress the short channel effect.

2.2 Partially and Fully Depleted SOI

Like MOSFETs in bulk CMOS, under normal bias conditions SOI MOSFETs have a depletion region in the channel under the gate electrode. Depending on how deep this region extends, SOI devices can be categorized into two types as shown in Figure 2.2: (a) partially depleted SOI (PDSOI) if the depletion region only occupies a portion of the body silicon, and (b) fully depleted SOI (FDSOI) [Mac90] if the depletion region extends all the way down to the buried oxide, occupying the entire body silicon.

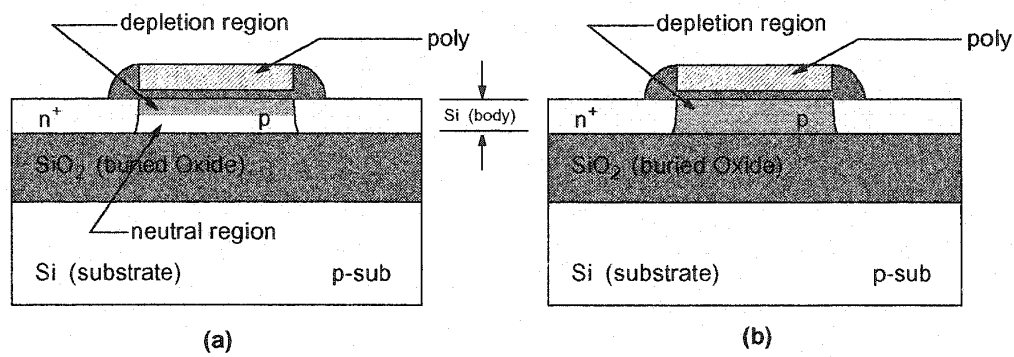


Figure 2.2 (a) Partially depleted SOI and (b) fully depleted SOI

Thickness and doping of the body silicon determines whether the device is partially or fully depleted. Compared to a fully depleted device, a partially depleted device has thicker body silicon and heavier substrate doping to allow formation of a neutral region between the depletion region and the buried oxide.

2.3 SOI Properties

The following sections discuss some of the most common characteristics of subquarter micron MOS devices for low-voltage circuit design, and how SOI can improve or worsen these properties. These effects are (a) the floating body effect, (b) the subthreshold swing, (c) short channel effects, and (d) the threshold voltage variation.

2.3.1 Floating Body Effect

The buried oxide in SOI is like a Pandora's box, in that the oxide offers the device better speed and isolation, but at the same time it also introduces many undesirable effects. One of the major drawbacks is the floating body effect¹ [Lu97]. As its name suggests, the silicon body is floating, that is, without a defined node connection as in the bulk device due to the buried oxide isolation. At dc, when the MOSFET is on, majority carriers generated by impact ionization accumulate inside the floating body near the drain end where the electric field is the highest. The generated charges gradually build up and the body potential increases until the voltage reaches the barrier potential of the pn junction of the source-body, forward biasing the diode. This results in a sudden increase in drain current² (the kink effect). Note that this mechanism is time dependent (finite time to accumulate enough charge to forward bias the junction), and therefore the floating body effect is dynamic and history dependent³. Both kink and history effects due to the floating body introduce severe problems for circuit design and simulation.

For analog circuits, the Kink effect is seen as a sudden increase in drain current (I_{DD}) with respect to the drain-source voltage (V_{DS}), which can be translated directly to an upward spike in the output conductance (g_{DS}), decreasing the dc self-gain (defined as g_m/g_{DS}) of the transistor abruptly. Since the body potential (V_B) is changing, the threshold voltage V_{th} is modulated as well due to the body effect:

$$V_{th} = 2\phi_B + \frac{\sqrt{2\epsilon_{si}\epsilon_0 q N_A (2\phi_B + V_{SB})}}{C_{ox}} \quad (2.4)$$

where V_{SB} is the source-bulk voltage, and C_{ox} is the capacitance of the gate oxide.

The time dependence of such phenomena makes modelling and circuit design extremely difficult. For example, for precise circuit simulation, only transient analysis can be used in circuit

-
1. Floating body effect is a phenomenon for PDSOI; in FDSOI, the channel is fully-depleted, so the Kink effect is less severe [Tse98].
 2. Neric's analogy: the reservoir can only hold that much water before it floods.
 3. The history effect is due to charge accumulation in the body

simulation because dc and ac simulation are no longer accurate due to the history effect. As for digital circuits used in VLSI, the situation is no better because threshold voltage variation with time raises many concerns for switching circuits due to transient leakage current [Lim83]. Although SOI is considered a better technology than bulk for both SRAM and DRAM [Kuo98], memory cells may suffer degradation attributed to the Kink effect in the form of lowered output impedance. For bulk devices, all of the charges generated are discharged through the substrate node to the ground¹. Therefore, floating body effect only occurs in SOI devices.

Nevertheless, in submicron devices, the floating body effect is greatly reduced due to the scaling down of supply voltage². Modern CMOS technology has the gate length scaled down below a quarter micron, and the reduction of short channel effects is the prime issue for the transistor to function properly [Bul00]. Therefore, the gate oxide is made very thin (e.g., far below 10 nm) for the gate electrode to maintain control of the current flow in the channel, but thinner oxide has lower breakdown voltage. Therefore, the supply voltage is scaled down for three main reasons: (a) to prevent gate oxide breakdown, (b) to minimize the horizontal electric field from the drain to source and hence the short channel effect, and (c) to lower power dissipation. Therefore, for modern submicron devices, many adverse SOI effects are alleviated due to the scaling down of the supply voltage, and as result it is now a competitive alternative to bulk CMOS [Kri98].

-
1. Body contacts can be added to PDSOI to remove the channel charge. This effectively makes the PDSOI device a bulk device except that the source/drain junction is reduced by the buried oxide, and the transistor is individually isolated.
 2. Recall that the kink effect is due to the high electric field at the drain-end that creates excess charges and builds up a voltage potential across the body. Therefore, reducing voltage supply alleviates the Kink effect.

2.3.2 Subthreshold Swing

Perhaps one of the most important parameters for low-voltage operation is the subthreshold swing, which is a measure of how well the gate can shut the transistor off. A typical subthreshold characteristic (I_{DD} vs. V_{GS}) of a MOS device has the y-axis on a log scale to emphasize the region of operation below the threshold voltage (subthreshold region) as shown in Figure 2.3.

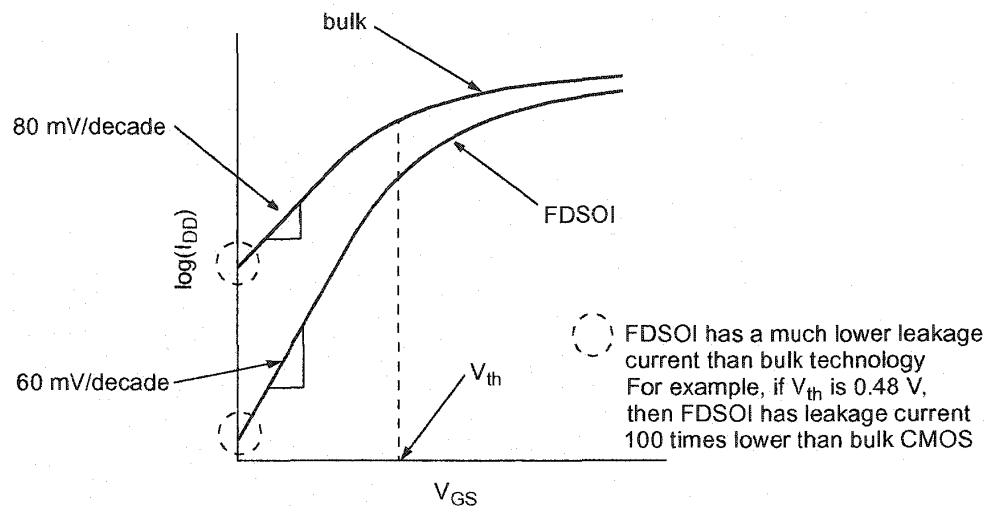


Figure 2.3 Subthreshold characteristic

In the subthreshold region, the channel is in the depletion region. The MOSFET has a behaviour similar to that of a pn diode (or bipolar transistor) in that the drain current I_{DD} is exponentially dependent on the gate voltage V_{GS} given approximately by

$$I_{DD} = I_S e^{nV_{GS}/V_T} \quad (2.5)$$

where I_S is a saturation current and V_T is the thermal voltage. The subthreshold swing S is used to describe the ability of the gate to turn the channel off in this bias regime, defined as

$$S = \frac{\Delta V_{GS}}{\Delta \log_{10}(I_{DD})} \quad (2.6)$$

with units of mV/decade. A small subthreshold swing is desirable to minimize channel leakage at V_{GS} of 0 V, and the minimum achievable subthreshold swing is the same as the slope of a pn junction, which is given by

$$\log_{10} I_{DD} = \log_{10} I_S + \frac{V_D q}{kT} \log_{10} e$$

$$S_{min} = \frac{\Delta V_D}{\Delta \log_{10}(I_{DD})} = \frac{kT}{q \log_{10} e} \quad (2.7)$$

where V_D is the voltage across the diode. At room temperature, the minimum achievable S is approximately 60 mV/decade. Typically, for PDSOI and bulk CMOS, the subthreshold swing is typically around 80 mV/decade, while FDSOI has S close to 60 mV/decade. Before this is explained, the importance of a good subthreshold swing is first discussed.

The subthreshold swing and the threshold voltage determine the leakage current when the transistor is off (Figure 2.3). Consider a typical MOS device which has a subthreshold slope of 80 mV/decade. This means that a reduction of 80 mV at the gate reduces the drain current by 10 times. If this device has a V_{th} of 0.8 V with I_{DD} of 0.1 mA at this voltage, then at $V_{GS} = 0$, the current is reduced by 10 decades, so

$$I_{DD} = 0.1 \times 10^{-3} / 10^{10} = 10 \times 10^{-15}$$

and therefore the leakage current is 10 fA. If the threshold voltage is lowered to 0.64 V, then at $V_{GS} = 0$ V the drain current is only reduced by 8 decades, and leakage current will therefore be increased by 100 times. In other words, a higher threshold voltage will have a lower leakage current for a given subthreshold swing.

However, for low voltage circuit design, it is favorable to have reduced V_{th} because this gives extra dynamic range for the circuit when cascoding transistors, given by the formula:

$$V_{min} = V_{th} + n v_{on} \quad (2.8)$$

where V_{min} is the minimum supply voltage, n is the number of cascoded transistors, and v_{on} is the on-voltage defined as $V_{GS} - V_{th}$. However, as mentioned in the previous paragraph, a reduction in V_{th} increases the leakage current for a given subthreshold slope, resulting in an increase in standby power consumption. Therefore, a device with an improved subthreshold slope can have a lower V_{th} without the penalty of an increase in the leakage current, which allows the low-voltage circuits to have a wider dynamic range for analog circuits, while maintaining power consumption at a low level for digital parts.

In order to have an ideal subthreshold slope of 60 mV/decade, all of the gate voltage should be used to control the energy barrier of the silicon channel, i.e., the gate voltage has to be equal to the diode voltage V_D as in equation (2.7). However, the gate oxide between the gate electrode and the channel forms a voltage divider as shown in Figure 2.4, so V_{GS} becomes

$$V_{GS} = \frac{1/C_{Si}}{1/C_{Si} + 1/C_{ox}} \cdot V_D \quad (2.9)$$

The voltage drop across C_{ox} reduces the ability of the gate to control the channel, and hence increases the subthreshold swing.

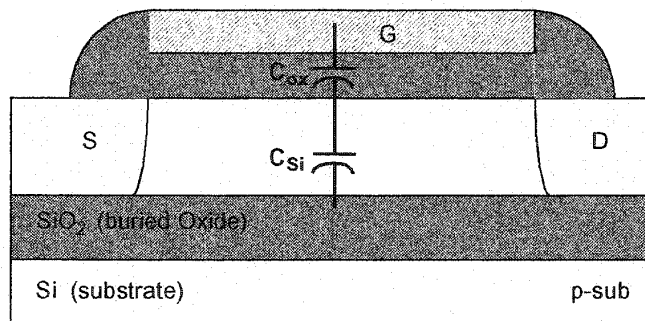


Figure 2.4 Capacitor model to demonstrate subthreshold swing

Even though the presence of the gate oxide is unavoidable in MOSFET devices, FDSOI has a subthreshold characteristic which is close to ideal. The reason is that FDSOI has a fully depleted

channel, and hence there is no charge stored in the silicon channel. Therefore, C_{si} is much smaller than C_{ox} so that all the voltage applied at the gate is directly applied to the channel as V_D . On the other hand, PDSOI is similar to bulk in that charges in the neutral region result in a finite value to C_{si} , and hence the subthreshold characteristic is worse than it is for FDSOI.

2.4 Short Channel Effects

In this section, a capacitor model similar to the previous section will be used to explain short channel effects. Although the model is not quantitatively precise, it provides an intuitive understanding from the circuit point of view.

Short channel effects are adverse effects that occur when the gate electrode does not completely control the channel charge. There are three major effects:

1. channel length modulation in saturation regime;
2. drain induced barrier lowering (DIBL), which leads to punch-through in extreme cases;
3. threshold voltage reduction.

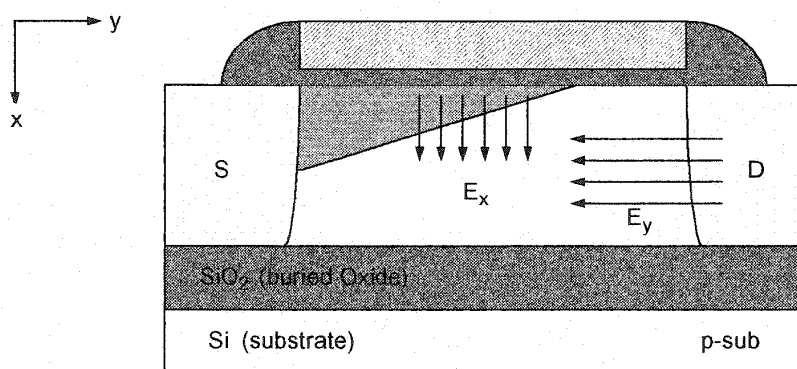


Figure 2.5 MOSFET short channel effects

To understand short channel effects, consider the model as shown in Figure 2.5. Ideally, in saturation, the conduction of the device should be completely controlled by the gate through electric field E_x . However, if there is a potential difference between the source and the drain, a

horizontal electric field E_y will be generated along the channel. E_y is undesirable because it modulates the channel length, making the device dependent on V_{DS} and hence increases the output conductance. Such dependency can be described by the parameter λ in the saturation mode of operation:

$$I_{DD} = k_p \frac{w}{l} v_{on}^2 (1 + \lambda V_{DS}) \quad (2.10)$$

where k_p is the process constant, w and l are the width and length of the device respectively, and v_{on} is the on-voltage defined as $V_{GS} - V_{th}$. An ideal MOSFET has a λ of zero for an infinite output impedance.

As E_y becomes larger, the gate loses more control to the source/drain electric field leading to an increase in leakage current, that is threshold voltage reduction and increase in subthreshold swing (DIBL). If the channel is extremely short, E_y can be large enough to carry electrons punching through the channel from the drain to source, causing a current conduction even though the device is off (punch-through).

Besides the undesirable electric field E_y , the depletion regions of the pn junctions between the active regions (source and drain) and the channel have similar effects to a short channel device. Consider the example as shown in Figure 2.6. A greater percentage of the channel region is depleted as the channel shortens, so the threshold voltage is also reduced according the Yau's trapezoidal model¹ [Sze81].

1. The threshold voltage is proportional to the charge in the depleted region controlled by the gate.

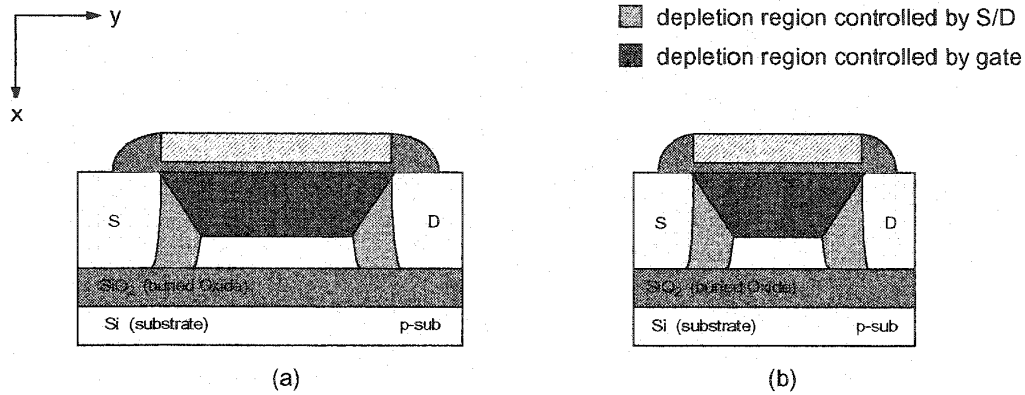


Figure 2.6 Gate-controlled depletion charges reduced from (a) to (b)

Usually, PDSOI has less severe short channel effect than FDSOI because PDSOI has a stronger E_x dominance over E_y . To observe this, assume the channel is partially depleted and behaves as a dielectric material. Then the channel can be modelled as two capacitors: one for the gate to represent the vertical field E_x , and one for the source/drain to represent the horizontal field E_y as shown in Figure 2.7.

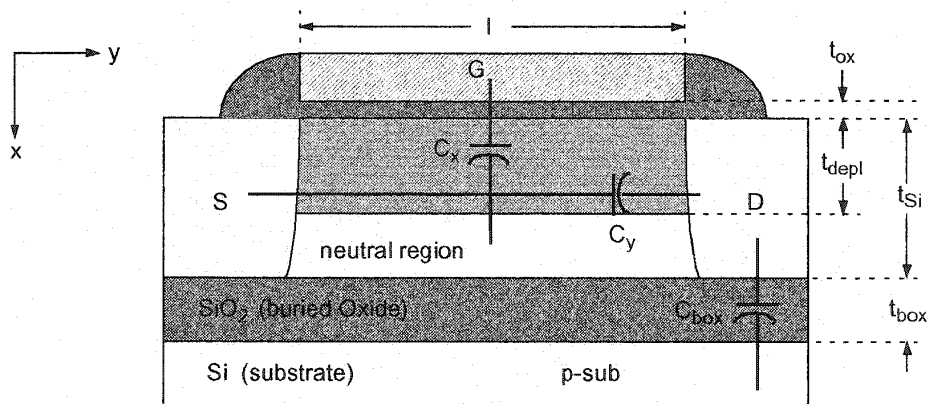


Figure 2.7 Capacitor model to demonstrate short channel effect

Assume the drain and the gate have the same potential when the transistor is on (saturation region of operation), then the capacitance ratio C_x to C_y can be used as a figure of merit for the short channel effect:

$$\frac{E_x}{E_y} \approx \frac{C_x}{C_y} \quad (2.11)$$

Therefore, for a given C_y , maximizing C_x minimizes the short channel effect.

For PDSOI (and bulk), C_x is given by

$$C_x = \frac{\epsilon_{Si}\epsilon_0}{3t_{ox} + t_{depl}} \quad (2.12)$$

assuming $\epsilon_{Si} \approx 3\epsilon_{ox}$ and the electric field E_x is terminated by the charge in the neutral region. Therefore, in any MOSFET (whether PDSOI, FDSOI or bulk), the gate oxide thickness t_{ox} is made as thin as possible to control the short channel effect, while the channel is doped as high as possible to reduce t_{depl} .

For FDSOI, since the channel is fully depleted, the electric field E_x is terminated in the charges below the buried oxide (substrate) instead of the neutral region (below the depletion region). Hence C_x is given by:

$$C_x = \frac{\epsilon_{Si}\epsilon_0}{3t_{ox} + t_{Si} + 3t_{box}} \quad (2.13)$$

Since $t_{Si} > t_{depl}$ and $3t_{box} > t_{Si}$ ¹, C_x in FDSOI is much smaller than in PDSOI, and hence short channel effects are worse in FDSOI. Now consider C_y , which is given primarily by

$$C_y = \frac{\epsilon_{Si}}{l} \quad (2.14)$$

1. t_{box} is usually 10 times thicker than t_{Si} in modern SOI process.

so the shorter the effective channel length l , the worse the short channel effects because C_y increases. Actually, for a very short gate length, most of the electric field penetrates the channel through the buried oxide because of its lower permittivity and larger cross sectional area compared to the body silicon. This suggests that in order to reduce C_y , especially for FDSOI, $C_{box} \gg C_y$ is desirable because this forces most of the horizontal electric field E_y to become vertical through the buried oxide C_{box} because

$$\frac{E_x}{E_y} = \frac{C_{box}}{C_y} \quad (2.15)$$

Therefore the body silicon film has to be made very thin for a smaller cross sectional area to reduce C_y , and the buried oxide film has to be thin as well for large C_{box} . In general, FDSOI with an effective gate length below 0.1 μm can only be made with very thin body silicon film (in the order of 10 - 20 nm).

2.4.1 Threshold Voltage

In PDSOI, the threshold voltage is insensitive to the body silicon thickness because the depletion region is not dependent on the film thickness. For FDSOI, the device mechanism is more complicated. The fully-depleted device requires a highly doped channel for the correct threshold voltage, and a very thin body film to control the short channel effects. The threshold voltage is sensitive to the amount of charges that exist in the channel, and its sensitivity increases as the body doping increases. However, this channel charge is governed by the body silicon dimensions because the body is made extra thin and is highly doped. Therefore, the threshold voltage can be linearly dependent on film thickness [She95] for a given doping. This is a concern from a manufacturing standpoint because process tolerance control becomes increasingly difficult to ensure uniformity of such thin body silicon across the wafer.

2.5 A 0.13 μm SOI CMOS Technology

In this thesis, most of the circuits were designed in an IBM 0.13 μm SOI CMOS technology. For NMOS, the f_t and f_{max} are 148 GHz and 162 GHz respectively, and for PMOS, the f_t and f_{max} are 68 GHz and 102 GHz respectively. The f_t and f_{max} plot is shown in Figure 2.8.

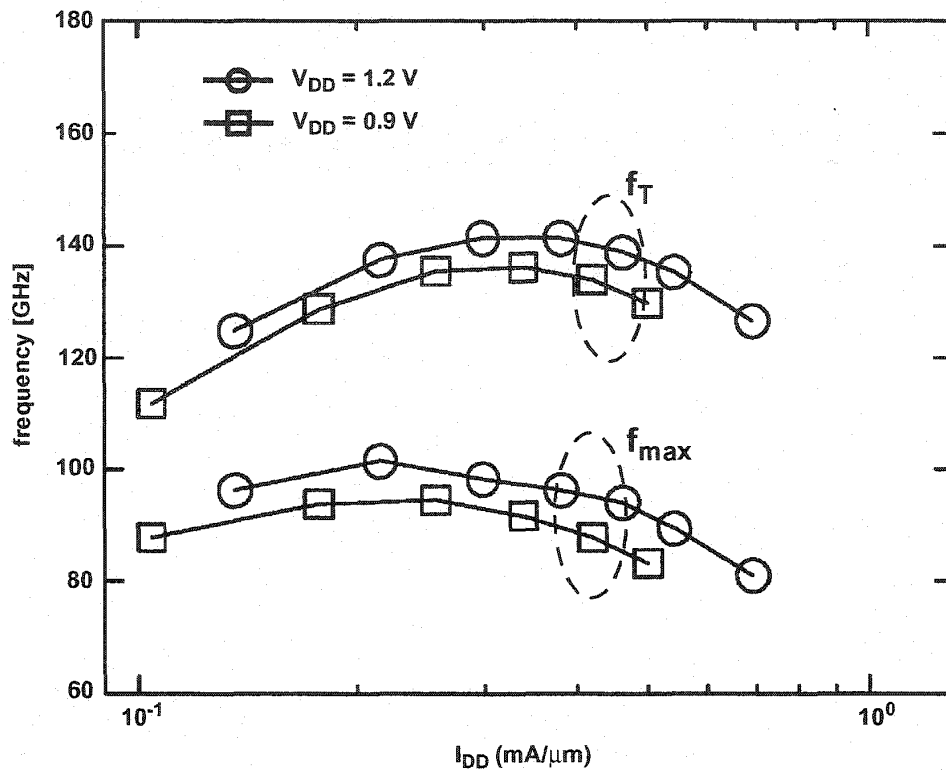


Figure 2.8 f_t and f_{max} of the transistors in 0.13 μm SOI CMOS technology¹

1. Data from [Zam01]. The peak f_{max} was later measured to be 162 GHz with better equipment setting.

2.6 Summary

SOI MOSFETs have greater speed than bulk devices mainly because of reduced junction capacitance below the source and drain. Bulk devices have no Kink effect, while PDSOI has a worse Kink than FDSOI [Tse98]. However, the Kink effect is minimized at lower voltage because the electric field at the drain side is smaller, which reduces the impact ionization. The subthreshold swing of FDSOI is close to ideal, while the bulk and PDSOI has a similar subthreshold slope. The short channel effects of bulk are similar to that of PDSOI, while FDSOI is worse because the vertical electric field is terminated below the buried oxide instead of below the depletion region. This can be amended by making the body silicon very thin. As for fabrication tolerance, body silicon thinning makes FDSOI devices vulnerable to process tolerance because many electrical parameters (such as the threshold voltage) become sensitive to the body thickness due to high doping and extra thin film. In a nutshell, FDSOI is inherently a better device compared to PDSOI and bulk. However, the fabrication process is more difficult to control, so that yield is a significant issue when it comes to high volume production. The properties of the MOSFET devices are summarized in Table 2.1.

Table 2.1: Comparison between Bulk, PDSOI and FDSOI Devices

	BULK $\xrightarrow{\text{add buried oxide}}$ PDSOI $\xrightarrow{\text{body silicon thinning}}$ FDSOI		
speed	slowest	fast	fast
Kink Effect (Low Voltage)	none	worst	reduced
Subthreshold Swing	poor	poor	close to ideal
Short Channel Effect	good	good	worst
Process Tolerance	good	good	worst

Chapter 3 Passives in SOI

In RF design, both actives and passives are crucial for circuit performance. In the previous chapter, active devices were discussed, and in this chapter, the focus is on the passive components. Passive components can be categorized into three types: resistive, inductive and capacitive. However, in RF integrated circuits, a passive component is often made up of all the elements mentioned above.

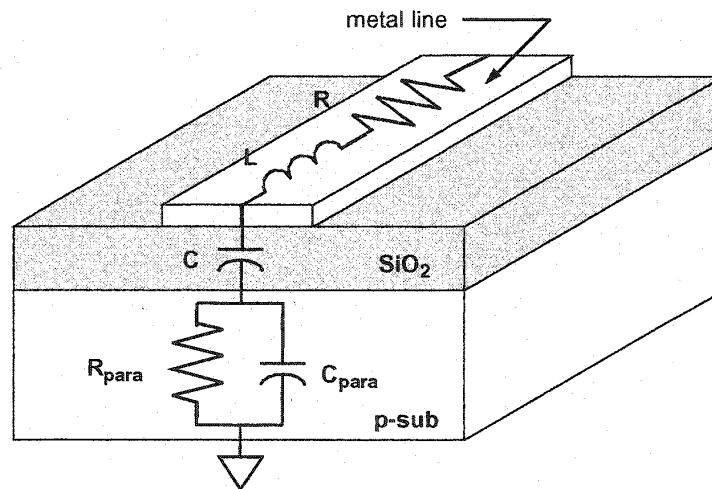


Figure 3.1 A metal line and its equivalent compact model at RF

As an example, consider a simple metal line as shown in Figure 3.1. In the equivalent model, there are resistive, inductive and capacitive components. Therefore, in designing passives at RF,

the goal is to maximize the desired component while minimizing the parasitic components at a particular frequency.

3.1 Inductor Design

3.1.1 An Inductor, or a Capacitor?

Probably one of the best examples to demonstrate the concept mentioned above is the monolithic inductor. A simple rectangular spiral inductor is shown in Figure 3.2. The inductance is generated by a magnetic field created by the flow of ac current, and aided by the magnetic coupling with the adjacent line which has the current flowing in the same direction. The parasitic components are the series resistance due to finite conductivity of the metal, substrate capacitance and resistive loss to the substrate. However, if the cross-section of the inductor (Figure 3.2) is examined, this inductor can also be visualized as a capacitor with the metal line as the top plate, the substrate as the bottom plate, and SiO_2 as the dielectric. Note that the substrate resistance is ignored in the figure.

To study the frequency characteristic of the spiral as shown in Figure 3.2, the spiral is modelled as a RLC distributed network¹ as shown in Figure 3.3. The model can be used to explain the inductor behaviour. At low frequencies, the impedance is frequency independent because the inductors behave like short circuits and the capacitors behave like open circuits. Therefore, the spiral behaves like a resistor. As the frequency goes up, the inductive reactance increases, but the capacitive reactance is still small enough to be ignored. The positive imaginary part dominates over the real resistive part and hence, the impedance of the spiral becomes inductive. However, at extremely high frequencies, the capacitance to substrate shorts all inductance to ground, making the spiral capacitive. Therefore, research has been done on suspended inductors [His96] and inductors with polyimide isolation [Rog01a] in an attempt to minimize this capacitance for high frequency operation.

1. Substrate loss is ignored for now for argument simplification.

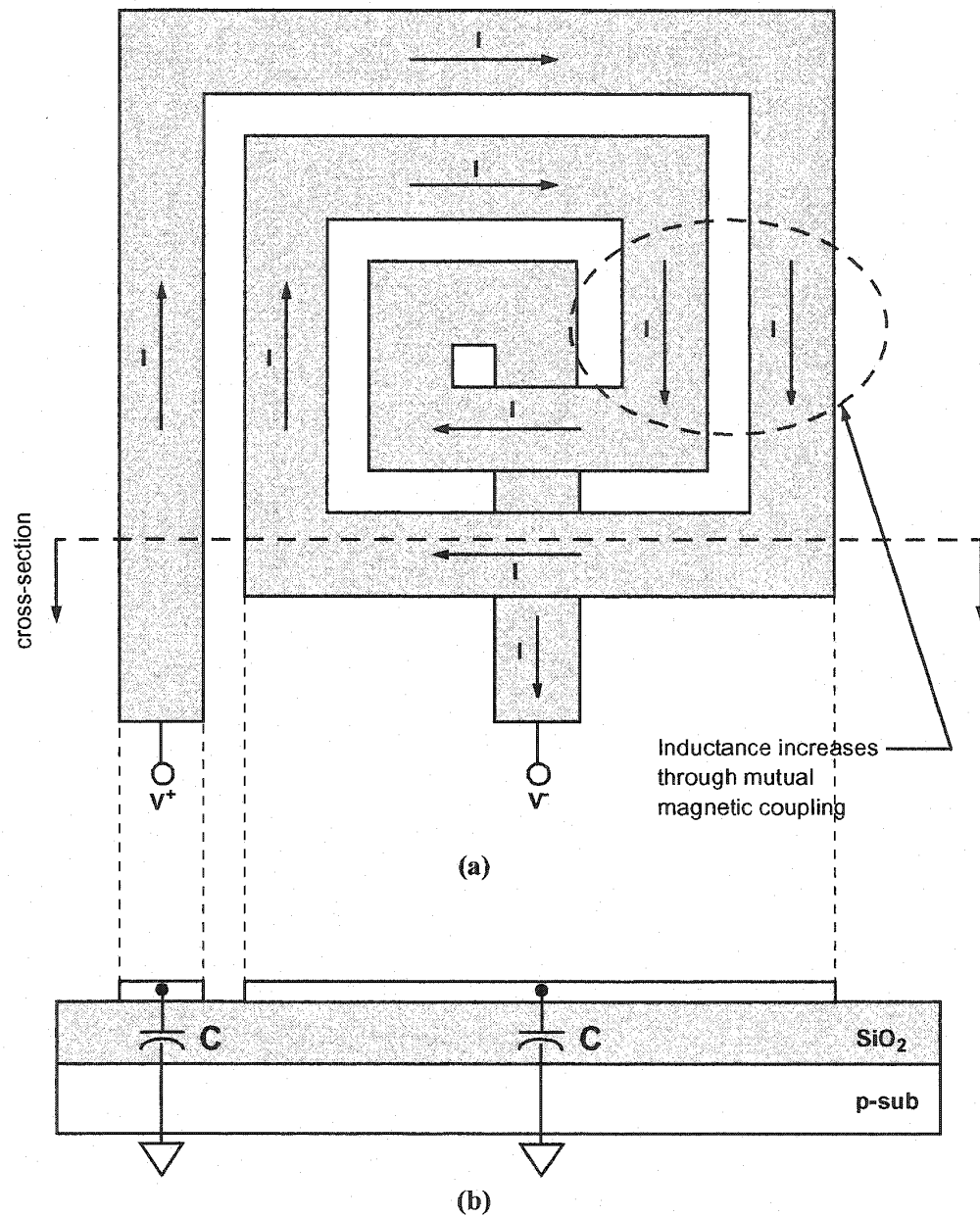


Figure 3.2 Spiral inductor (a) top view and (b) cross section

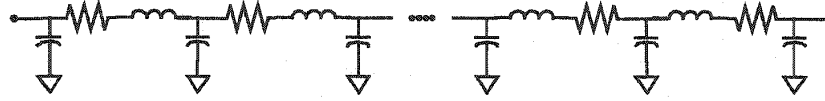


Figure 3.3 RLC distributed network of the spiral inductor

3.1.2 Quality Factor

Since the parasitics can change the characteristic of the passive devices significantly, a figure of merit called “quality factor” Q is used to measure the ratio of the desired impedance to the parasitics. This is formally defined as

$$Q = \frac{\text{Energy stored per cycle}}{\text{Energy loss per cycle}} \quad (3.1)$$

From the circuit point of view, it can also be treated as a ratio of the imaginary reactive component to the real resistive component. For example, the Q of an inductor L is

$$Q = \frac{\omega L}{R_s} \quad (3.2)$$

where L is the reactive inductance while R_s is the series resistance associated with the inductor. The higher the Q , the less the parasitic effect and hence the better the quality of the inductor. However, L and R_s are not constant because of (a) parasitic components C_{para} and R_{para} , and (b) frequency effects such as magnetic coupling and skin effect. Therefore, to maximize the Q of the inductor, the conductivity of the metal, substrate losses and frequency effect have to be considered.

3.1.3 Relationship between Inductance, Series Resistance and Substrate Loss

A good inductor has the inductance maximized and the series resistance and substrate loss minimized. However, all these three parameters are correlated with each other for a given structure. Consider the simplest form of an inductor: a metal line as given in Figure 3.4.

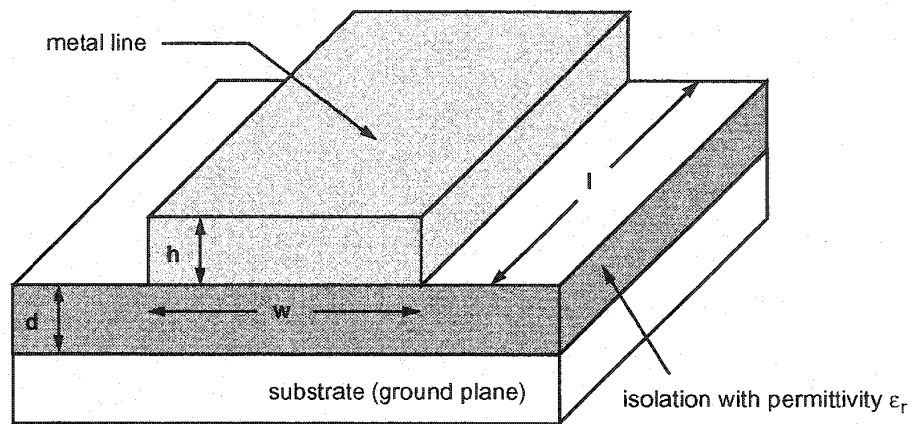


Figure 3.4 A metal line on a piece of substrate

The inductance L can be approximated by using microstrip formulas given by [Poz98]:

$$L = \frac{Z_0}{v_p} \cdot l \quad (3.3)$$

where Z_0 is the characteristic impedance and v_p is the phase velocity, given by:

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_e} [w/d + 1.39 + 0.67 \ln(w/d + 1.44)]} \quad (3.4)$$

$$v_p = \frac{c}{\sqrt{\epsilon_e}} \quad (3.5)$$

ϵ_e is the effective permittivity given by

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \frac{1}{\sqrt{1 + 12d/w}}$$

where ϵ_r is the relative permittivity of the isolation¹. The dc series resistance is given by:

$$R_s = \rho \frac{l}{wh} \quad (3.6)$$

where ρ is the resistivity of the metal. Finally, the substrate loss (in Ω) is given by

$$S_{LOSS} = (Z_{C_{para}} \parallel Z_{R_{para}}) \cdot wl \quad (3.7)$$

where $\hat{C}_{para}$ and $\hat{R}_{para}$ are parasitics per unit area.

Based on equations (3.3)-(3.7), the relationships between the physical design parameters and the electrical properties of the inductor are summarized in Figure 3.5.

	l (increase)	w (increase)	h (increase)
Inductance	↑	↓*	↓*
Series Resistance	↑	↓	↓
Substrate Loss	↑	↑	—

* decrease slightly compared to increase in inductance

Figure 3.5 Relationship between electrical properties and physical structure

Figure 3.5 shows the electrical trends and trade-offs for an inductor between each pair of design parameters. For example, if a large inductance is required at RF, the line has to be long (large l) while making the width narrow (small w) to minimize substrate loss, and maybe with the option of stacking two or more metal levels together (increase h) to lower the series resistance. However, the parameters are not linearly related to each other because they are heavily dependent

1. For simplicity, the loss factor is not included since the equations are used to relate inductance to l , w and h only.

on the frequency of operation and the physical parameters of the technology backend. Therefore, electromagnetic (EM) simulation is often employed to optimize the inductor design.

3.1.4 Metal Stacking in RFIC

A common design technique to reduce R_s is to increase h by stacking two or more metal levels, as shown in the cross section of Figure 3.6.

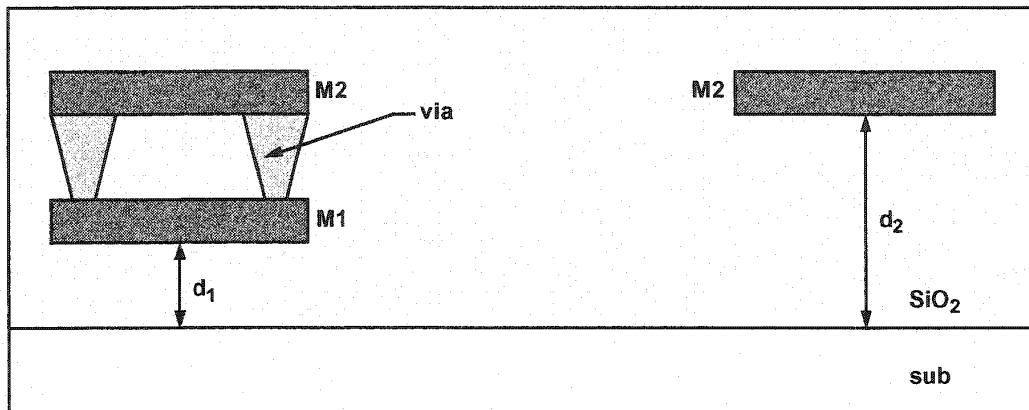


Figure 3.6 Metal stacking in monolithic technology

Vias are usually used to stack two metals, and ideally it is desirable to use as many vias as possible to reduce the via resistance. However, process limitations such as the antenna rule¹ limit the number of via placements for a given area. Therefore, placement of vias can be tricky for submicron technology. Via placement suggestions are given in Figure 3.7. Each via has finite resistance. However, multiple via placement makes such resistance negligible compared to R_s of the metal. Nevertheless, it is incorrect to assume that the via height as part of the total metal thickness. The detail is given in Section 3.1.7.

1. Electrical charges build up during the processing of vias. If too many vias are placed for a given area, the charges can be large enough to destroy the thin gate oxide [IBM00]. Protection diode can sometimes be used to resolve the problem. However, for circuits such as cross-coupled VCO, the parasitic components of the diode degrades the circuit performance.

Metal stacking also reduces device isolation. As shown in Figure 3.6, for a metal-stacked device, the distance to the substrate is reduced from d_2 to d_1 . Therefore, the parasitic capacitance¹ is increased.

Since metal stacking reduces device isolation from the substrate, there is a trade-off between series resistance and substrate loss. Moreover, due to the skin depth of the metal, extra stacking may not improve the series resistance but the device isolation will still be reduced. Therefore, it is

1. Recall that capacitance per unit area $C_{para} = \epsilon_{ox}/d$ where d is the distance to the substrate.

reasonable to stack metals if the inductor is designed for 1 GHz, but not if the inductor is to be operated at 40 GHz.

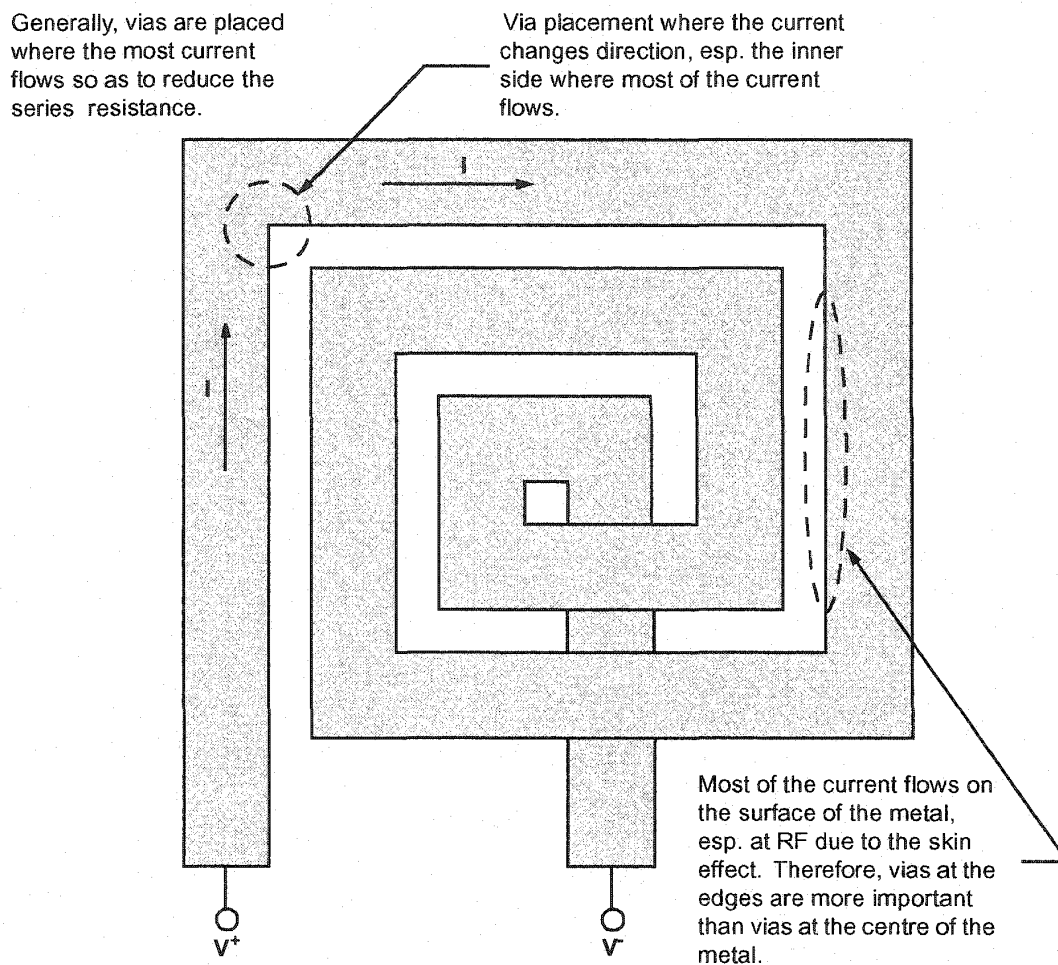


Figure 3.7 Via placement in a metal stacked spiral inductor

3.1.5 Differential Excitation of Inductor

Having a high Q inductor is very important to many circuits, especially a VCO, because inductor loss is the most significant contributor to phase noise [Lon97][Yue97]. One of the common techniques to boost the Q is to operate the inductor differentially [Dan98], which results in substrate loss being reduced by one half compared to the single-ended excitation as explained in Figure 3.8.

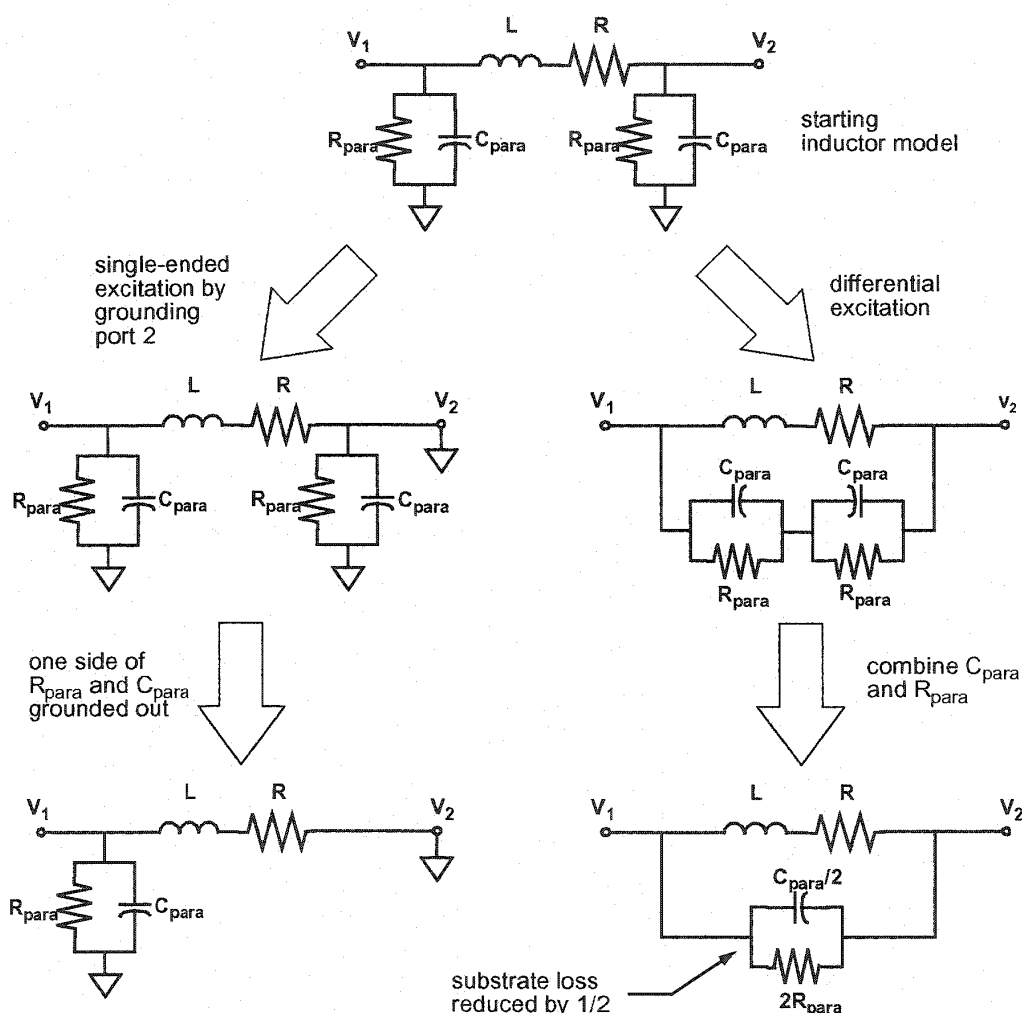


Figure 3.8 Models of single-ended and differentially excited inductor

3.1.6 Copper Metal in Fabrication

Another way to boost the Q of the inductor is to improve the conductivity of the metal to reduce series resistance. Traditionally, aluminum is the most commonly used material for metallization due to the ease of fabrication. Recently, copper metallization technology has become mature enough to be employed in VLSI. The copper technology offers better conductivity¹, and it has much lower electromigration so that enables the metal to handle higher current density. Therefore, narrower lines can be used, which not only help to save chip area, but also reduce parasitic capacitance and hence improve circuit performance (reduced delay, for example).

There are two copper metallization approaches: one for digital VLSI circuits [IBM00], and one for analog RF designs [Rog01a]. In digital VLSI circuits, thousands to millions of transistors are to be connected by metal, so the interconnects are featured with short and fine metals (e.g., 0.5 μm line width) to reduce parasitic capacitances, hence reducing the propagation delay and power consumption. However, in analog RF circuits, much wider line widths are required (e.g., 25 μm line width) for power supply lines and inductors.

The fabrication method for the fine and the wide lines are different, especially during the etching steps, when the metal shape is defined. Fine metal is usually shaped by dry ion etch, while wide metal is often processed by a wet etch. The fabrication process is shown in Figure 3.9.

Note that the fine line copper process cannot be used to make wide metals, and vice versa. For the fine line process, if the metal is too wide, the concave surface profile due to the ion etching process removes copper all the way to the bottom, leaving an opening at the centre, and hence the conductivity of the metal is reduced. On the other hand, using the wide metal process to fabricate fine lines is also impossible. A less controllable copper growing procedure expands the dimension of the copper, making the process tolerance unacceptable for industrial standards. Furthermore, the wet etch cannot be used for metals for fine resolution because it removes the target metal lines, and for fine lines it may even remove the metals completely.

1. The conductivity of copper and aluminum are 1.6 $\mu\Omega\text{-cm}$ and 2.7 $\mu\Omega\text{-cm}$ respectively.

In this thesis, since the IBM SOI process [IBM00] is used, the metal lines are fabricated with the fine line copper process, which is not ideal for fabricating inductors.

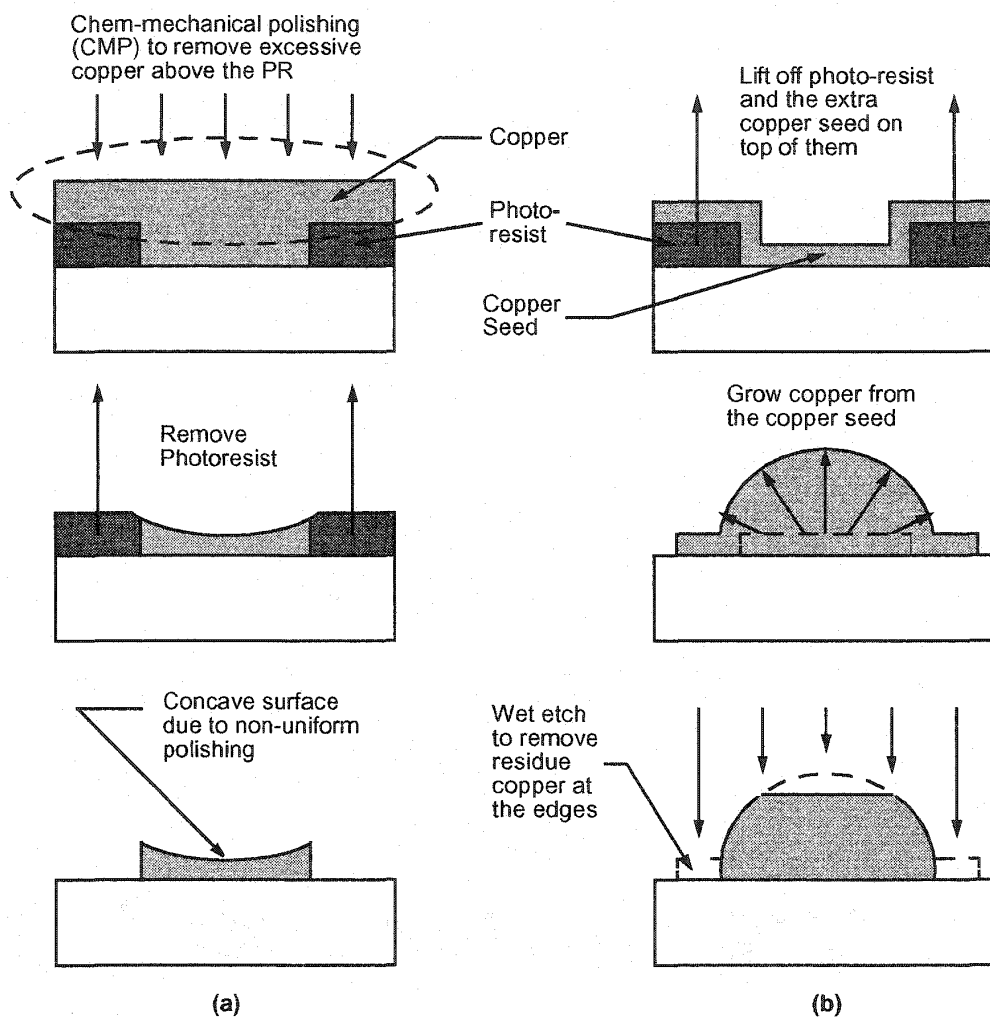


Figure 3.9 (a) Fine line copper process for digital VLSI and (b) thick copper metal process for analog RF design

3.1.7 Horseshoe Inductor

A few inductors have been designed for operation at different frequencies. The backend of the SOI technology features multi-levels of copper metals and vias, and 10 μm of low- k dielectric for isolation [IBM00]. Among these inductors, one of the designs is the horseshoe inductor as shown in Figure 3.10, which is used for the VCO LC resonant tank around 4.8 GHz.

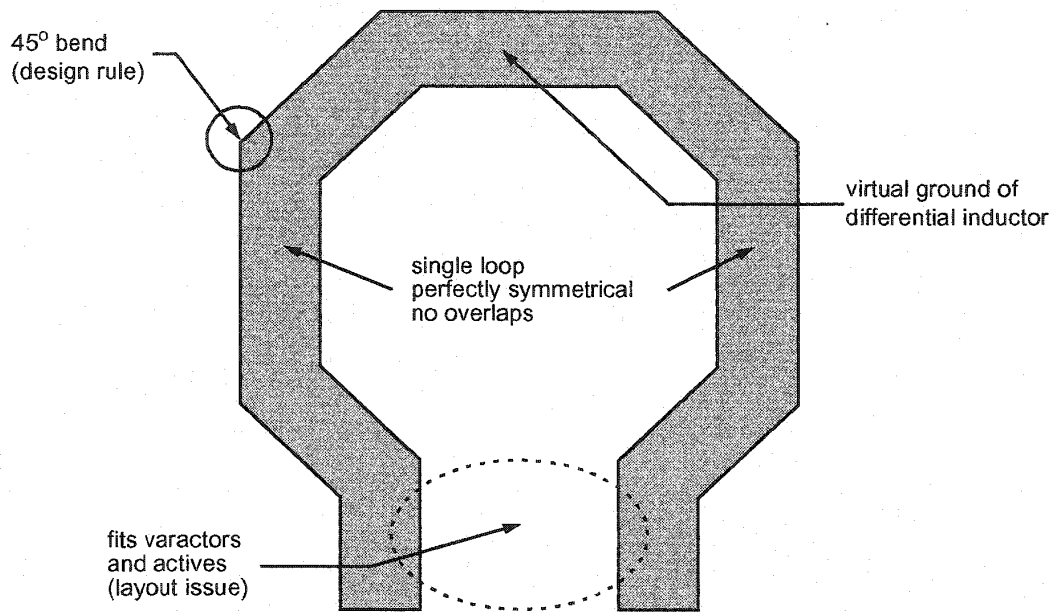


Figure 3.10 Horseshoe inductor

The horseshoe inductor is designed to operate differentially. Even though a single loop inductor does not provide large inductance, it only requires one level of metal without overlaps, and hence it is perfectly symmetrical. Furthermore, as the operating frequency increases, both inductance and capacitance required for the LC resonator decreases, therefore a multi-turn design is sometimes not necessary.

During the design phase, the technology design kit for inductors was not available, and therefore EM simulation with IE3D [IE3D] was used for inductor design. The inductor was

constructed by stacking the top two layers of 1.2- μm -thick copper metal using bar-shaped vias. Metal stacking was used because (a) resistive loss is greater than substrate loss due to good inductor isolation, and (b) the skin-depth is more than 1.2 μm in the 4.8 GHz range. The diameter of the inductor is 460 μm . Assuming the metal thickness is 4 μm (thickness of two metal layers plus via height), the simulation gives an inductance of 0.65 nH, with single-ended peak Q of 40 at 4 GHz.

The simulated small-signal s-parameter model is optimized to a lumped circuit model as shown in Figure 3.11. The model consists of seven sections of a simple transmission line model, and the inductance L for each line represents both inductance for the line and coupling from the single loop.

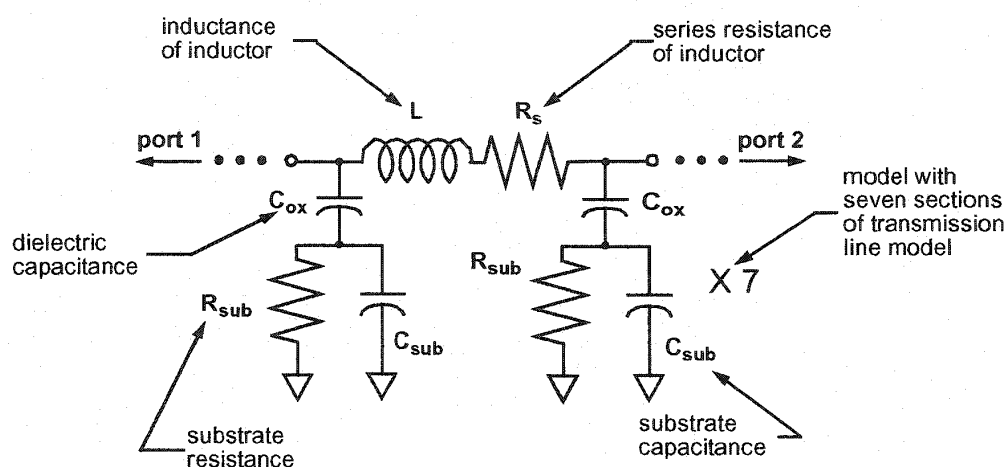


Figure 3.11 Inductor compact model for circuit simulation

The one-port s-parameter measurement is shown in Figure 3.12. The measured inductance is about 0.85 nH with peak Q around 24 at 3 GHz. The large discrepancy between theory and measurement is primarily due to the fact that, since it is impossible to fill the via bar between the two metal layers, the true metal thickness is not the same as was assumed in theory. Therefore, the effective metal thickness is only 2.4 μm instead of 4 μm . The inductance is therefore

increased as described in Figure 3.5. As for Q , the change in thickness causes R_s to increase by about 67%, and from (3.2), Q is decreased from 40 to 24 as measured. The measured peak Q frequency is very close to the simulated results because the distance between the lower metal and the substrate remains the same, and hence C_{para} is predicted correctly. The slight shift in frequency is due to the change in inductance. Note that the measurement near the peak Q is not smooth. This is due to measurement limitations because the small parasitic resistance causes numerical error in Q computation.

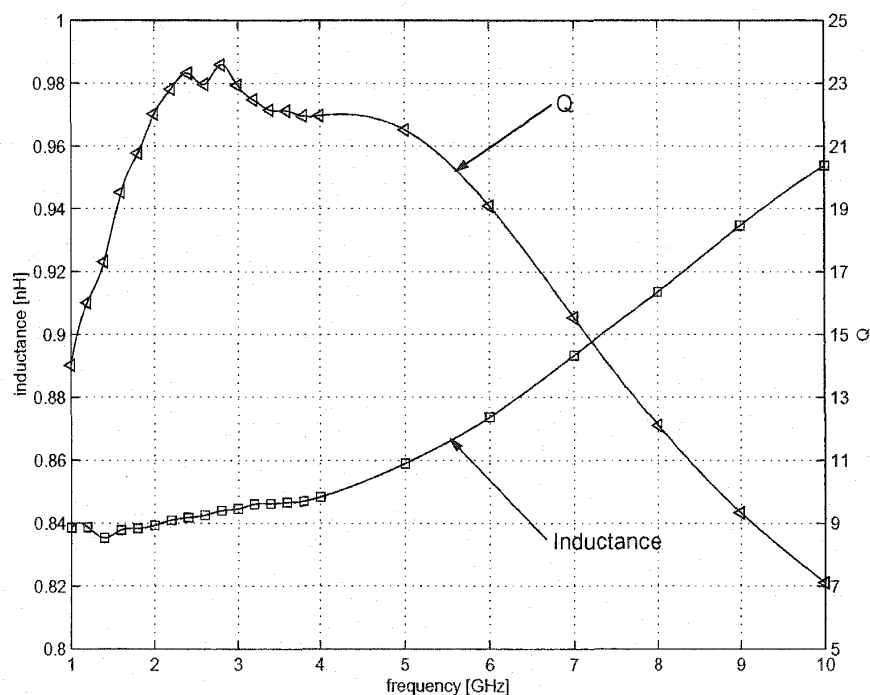


Figure 3.12 Single-ended measurement of horseshoe inductor

Despite the discrepancy in the simulation results, the horseshoe inductor offers high Q and reasonable inductance for VCO applications. Note that the structure of the inductor is perfectly symmetrical, and therefore the Q will be much higher when operated in a differential VCO. The inductor performance summary is given in Table 3.1.

Table 3.1: Horseshoe inductor performance summary

inductance	0.84 - 0.86 nH between 2 to 5 GHz
Q	> 20 between 2 to 5 GHz
peak Q	23 at 3 GHz
resonant frequency	> 10 GHz
diameter	460 μm

3.1.8 Multi-Level Multi-Turn IF Inductor

A choke was designed for analog filters at the IF stage. This choke is an octagonal spiral which is interwound between 4 levels of metal and has 3 turns per level as shown in the micrograph Figure 3.13. It has a structure which ensures that all the current is going in the same direction, and the metal-to-metal spacing is minimized to result in maximum coupling. Since the frequency is not high, the series resistance is more dominant than the substrate loss, and therefore metal stacking is used to reduce the lossy parasitic. Since EM simulation is impractical, the inductance is estimated by an analytical formula with substrate loss ignored [Lee98]:

$$L = 4\pi\mu_0 n^2 r \quad (3.8)$$

where μ_0 is the permeability of space, n is the number of turns, which is 12 (4 levels with 3 turns), the outer radius r is 70 μm , and the inductance is estimated to be 12 nH.

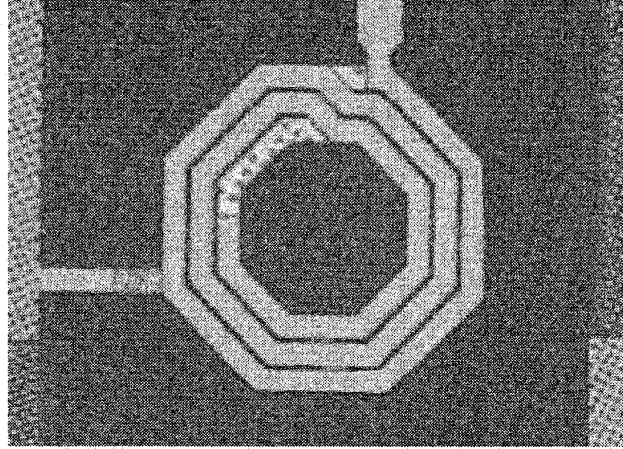


Figure 3.13 Micrograph of multi-level multi-turn IF inductor

Next, the resonant frequency is to be estimated. Using the parallel plate capacitance formula

$$C = \frac{\epsilon_{Si}\epsilon_0}{d} \quad (3.9)$$

where d is the distance between the lowest metal level and the substrate, the effective parasitic capacitance per unit area¹ $\hat{C}_{para}$ is approximately $16 \mu\text{F}/\text{m}^2$. The total metal area is approximately $9 \times 10^{-9} \text{ m}^2$, and therefore the total parasitic capacitance is 0.15 pF . The resonant frequency f_{res} is calculated by using

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (3.10)$$

which is approximately 3.7 GHz . The measured inductance and Q using a one-port s-parameter measurement is shown in Figure 3.14. The inductance is approximately 16 nH between 100 MHz to 1.6 GHz , where the Q peaks at 7 . The resonant frequency is approximately at 4 GHz . Note that the analytical formula gives a good approximation as long as the inductor is operated at low

1. Estimated from the minimum distance between the metal and the substrate.

frequency. The high inductance and small chip area (140 μm by 140 μm) makes this inductor attractive for RF or IF choke applications.

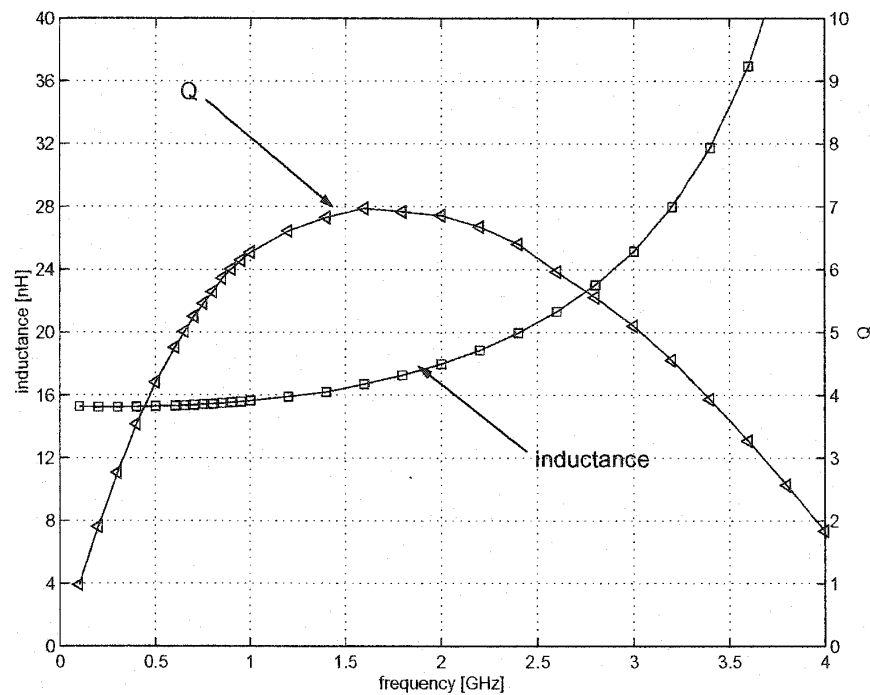


Figure 3.14 Measurement of multi-level multi-turned IF inductor

3.2 CMOS Accumulation Mode Varactor

The AMOS capacitor has recently been a popular choice for VCO varactors [Ain00][Fon02e]. A good C_{max}/C_{min} ratio of about 3.5 has been reported in a 0.25 μm bulk CMOS technology with a tuning voltage of ± 1 V [Sam01]. This ratio can be improved further by using better lithography and SOI technology to reduce the parasitic capacitances, and a C_{max}/C_{min} ratio of 5 for the same tuning voltage has been demonstrated in this technology [Zam01]. These AMOS varactors have been employed in several VCO circuits (see Chapter 4), and measured results showed that they can work at 40 GHz and beyond [Fon02c]. Despite the good performance, a study of these types of AMOS at the device level has never been conducted. Furthermore, AMOS varactors are

critical for the VCO design as described in Chapter 4. Therefore, in this section, the structure and basic operation of AMOS capacitor is first reviewed. Then, measured C-V and Q-V data are presented, and the varactor performance is evaluated. Finally, AMOS varactor designs in SOI and bulk are compared.

3.2.1 AMOS Structure and Operation Principle

The cross-section of an n-type AMOS varactor in SOI is shown in Figure 3.15a. The structure is very similar to a MOSFET, except that both the channel and source/drain regions are doped with the same dopants, which is n-type in this case. The channel is isolated from the substrate by the buried oxide, forming the parasitic capacitance C_{box} . The gate of the device is defined as the cathode v^+ , while the source and drain are tied together, forming the anode v^- of the device. The symbol for the AMOS varactor is shown in Figure 3.15b, with the convention that the varactor arrow is pointing towards the cathode.

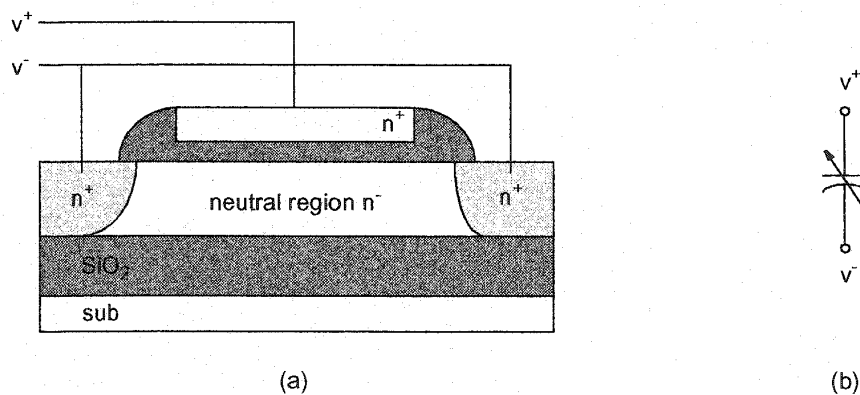


Figure 3.15 (a) Structure and (b) symbol of AMOS varactor

An AMOS capacitor has three modes of operation: accumulation, depletion and inversion as shown in Figure 3.16, and the capacitance of the device depends on the mode of operation.

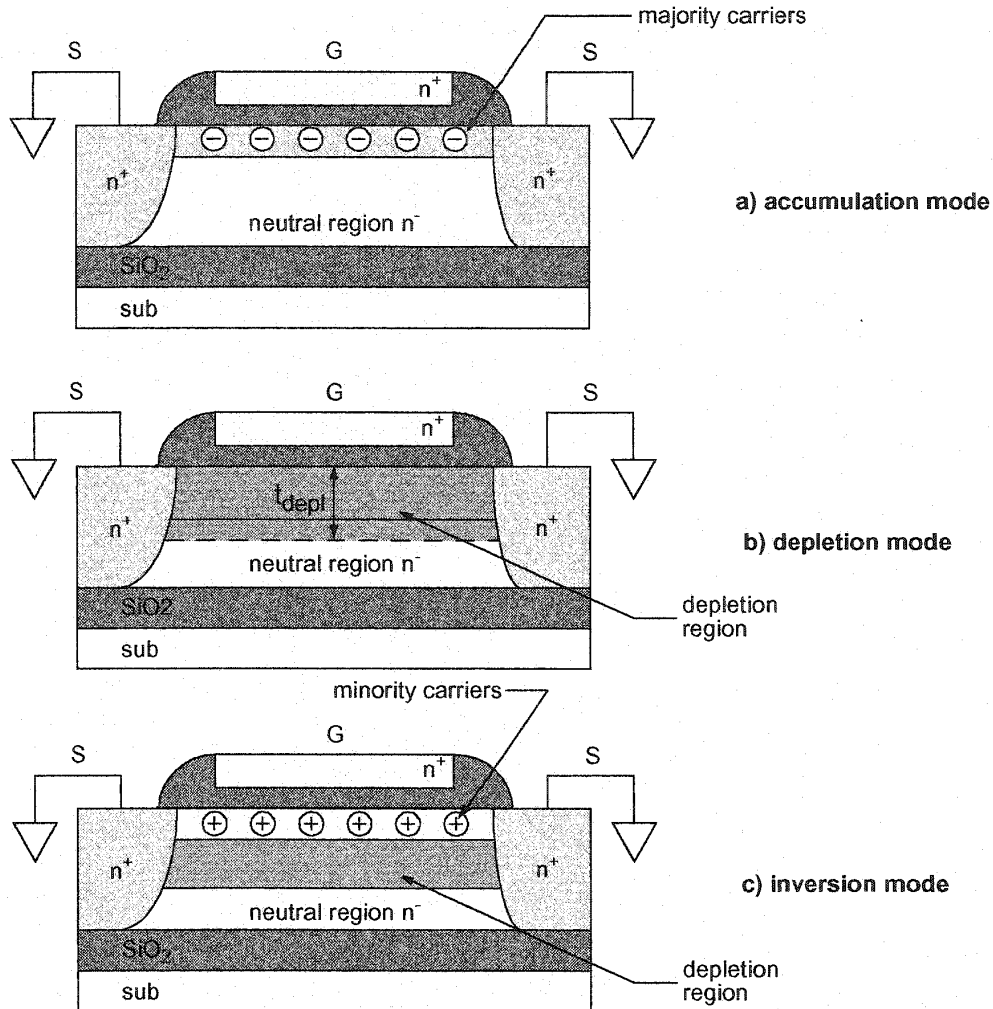


Figure 3.16 Operation principle of n-type AMOS varactor

When the gate electrode is very positive, the AMOS is operated in the accumulation mode. The majority carrier forms a conduction plane at the surface of the channel, and the capacitance of the varactor C_v is the gate oxide capacitance, which represents the maximum capacitance (C_{max}):

$$C_v = C_{ox} \quad (3.11)$$

As the gate electrode becomes negative, holes are attracted to the surface and neutralize the electrons, and a depletion region is formed. Therefore, the varactor capacitance is the gate oxide capacitance in series with the depletion capacitance C_d :

$$C_v = \frac{C_{ox}C_d}{C_{ox} + C_d} \quad (3.12)$$

where C_d is given by

$$C_d = \frac{\epsilon_{Si}}{t_{depl}} \quad (3.13)$$

where t_{depl} is the depletion depth as defined in Figure 3.16. The depletion depth is gate voltage dependent, because the depth of the depletion depends on the amount of holes attracted to the surface for neutralization. For a given doping and voltage, t_{depl} can be calculated by:

$$t_{depl} = \left(\frac{2\epsilon_{Si}\phi_s}{qN_d} \right)^{1/2} \quad (3.14)$$

where ϕ_s is the surface potential and N_d is the doping concentration of the depletion region.

This depletion region grows with increased voltage across the AMOS capacitor, and this capacitance-voltage dependency continues until inversion is reached. A sheet of holes (minority carriers) accumulate at the surface of the channel, shielding the depletion region from growing any further. Unlike the MOS device, although this inversion layer of holes is conductive, it is insulated from the n-type S/D terminals by the pn junction voltage barrier. This represents the minimal capacitance (C_{min}) of the varactor, and any further decrease in voltage does not change the capacitance.

3.2.2 Figure of Merit

Two figures of merit (FOM) are often used to measure varactor performance: C_{max}/C_{min} ratio and quality factor Q . C_{max}/C_{min} is the ratio of maximum to minimum capacitance that the AMOS device can provide, which is a measure of tunability. The higher the capacitance ratio, the wider the tuning range. C_{max} is usually determined by the gate oxide capacitance C_{ox} , while C_{min} is usually limited by the overlap capacitance C_{ov} and buried oxide capacitance C_{box} as defined in Figure 3.17.

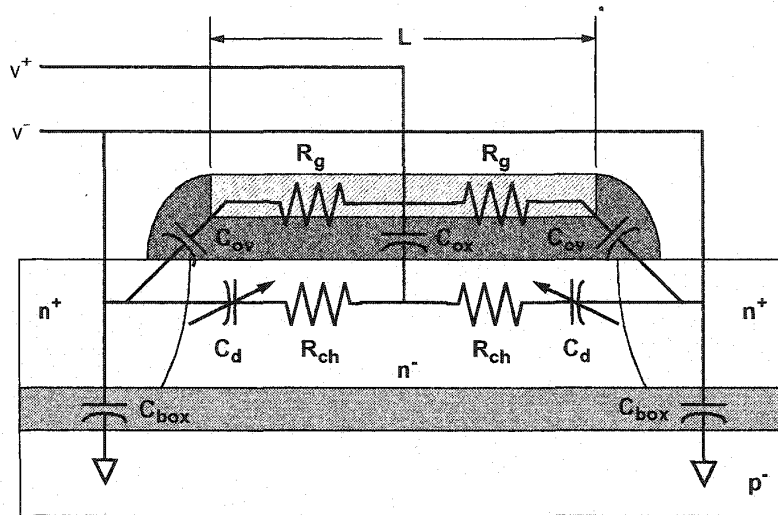


Figure 3.17 Lump model of AMOS varactor

Q is the ratio of the reactance to resistance of the passive device, which is given by

$$Q = \frac{1}{\omega C_v R_v} \quad (3.15)$$

where C_v is the total series capacitance given by C_{ox} , depletion capacitance C_d and the parasitic capacitance, while R_v is the series parasitic resistance including the channel resistance R_{ch} and gate resistance R_g . The gate oxide C_{ox} usually has very high quality (and hence high Q) to prevent

oxide breakdown. Most of the lossy parasitic component (grouped as R_{ch}) comes from the channel, where the depletion layer forms. The channel resistance is proportional to the gate length, therefore a lower channel series resistance is expected for a smaller gate length l . At the same time, making the gate length smaller may decrease tunability because of the overlap capacitance from the side walls which is bias independent. Therefore, minimum gate length provides the best Q but the worst tuning range.

To improve Q further, the gate resistance can be improved by (a) connecting both ends of the gate-poly with metal (double-side tapped gate), which reduces the resistance by a factor of 4, and (b) using multi-fingers that reduces the resistance by a factor of m , where m is the number of fingers. If these techniques are employed, R_g is usually insignificant compared to R_{ch} . Meanwhile, channel resistance R_{ch} can only be improved by reducing L . Making the AMOS varactor with wider channel width or multi-fingers does not improve R_{ch} . This is because if the channel resistance is reduced by m times, the area is increased by m times, and the effective Q remains the same as shown below:

$$Q = \frac{1}{\omega \cdot mC \cdot \frac{R_{ch}}{m}} = \frac{1}{\omega CR_{ch}} \quad (3.16)$$

Therefore, R_{ch} is usually the dominant factor for lossy parasitic components. This is verified by device simulation [MEDICI], which demonstrated that if a 0.2 μm instead of a 0.1 μm lithography is used, Q is reduced by half due to the 2 times increase in channel resistance (Figure 3.18). Therefore, the gate lithography is crucial for making a good AMOS varactor.

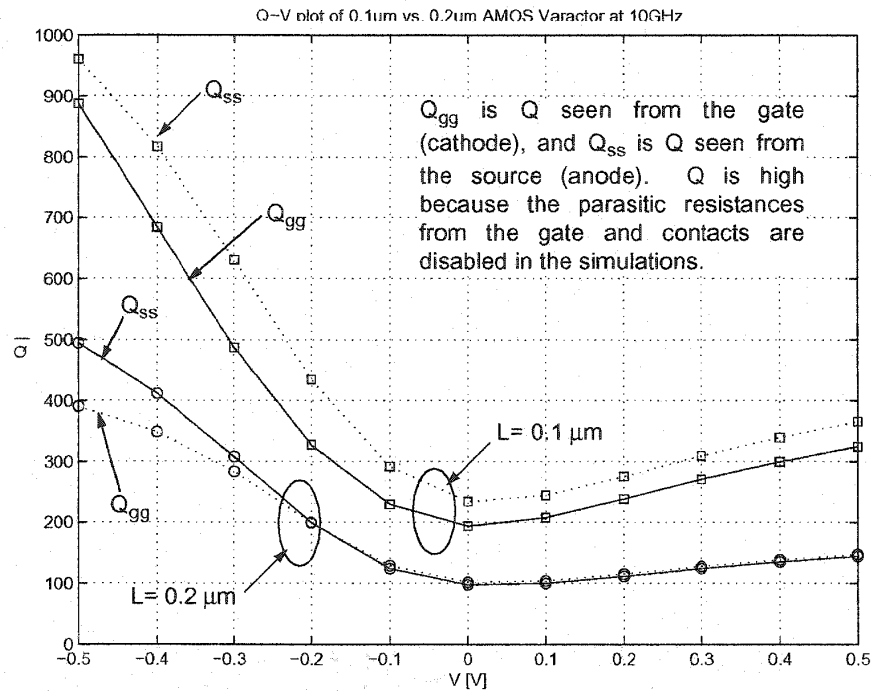


Figure 3.18 Q-V curves for channel length of 0.1 μ m and 0.2 μ m

3.2.3 Measurement

The varactor in this technology was measured with a one-port s-parameter measurement at 1 GHz [Zam01]. The capacitance and Q are shown in Figure 3.19. As described in Section 3.2.1, there are three modes of operation: accumulation mode in region A where the capacitance is the maximum (almost 100% of C_{ox}), depletion mode in region B where the varactor gain k_v (defined as change of capacitance per unit voltage) is high, and inversion mode where the capacitance flattens at minimum capacitance at 16% of C_{ox} . The varactor has a C_{max}/C_{min} about 6.

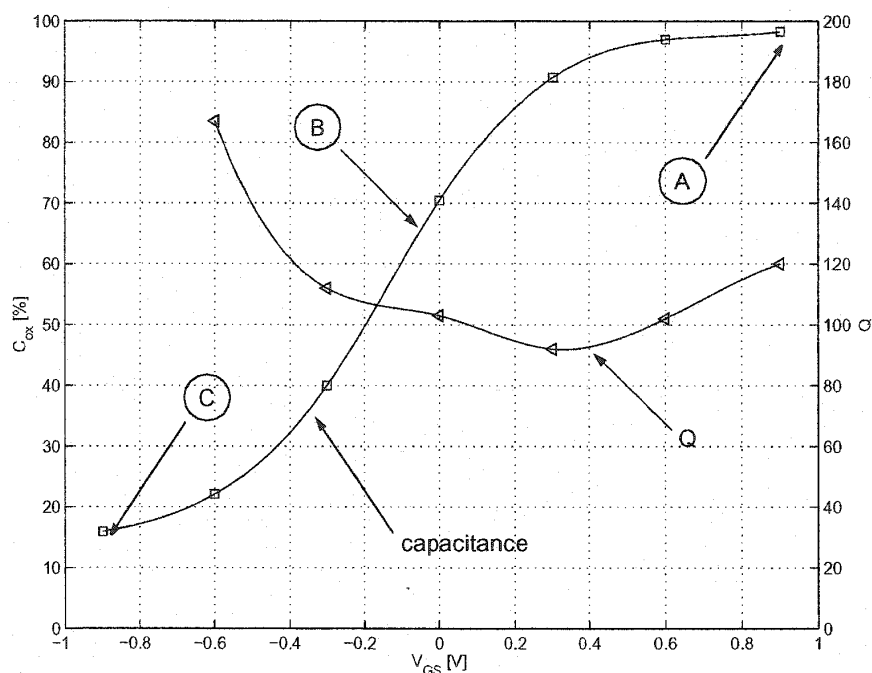


Figure 3.19 Measured C-V and Q-V curve of a AMOS varactor at 1 GHz

As for Q , it first drops from 120 to a minimum around 95 when the operation of AMOS shifts from accumulation (region *A*) to depletion (region *B*), then it rises again as the AMOS shifts toward inversion mode (region *C*). The Q characteristic of an AMOS varactor can be explained using a similar charge redistribution argument as in Section 3.2.1.

In the accumulation mode (point *A* in Figure 3.19), the majority carriers are attracted to the surface of the channel, forming a conductive layer that lowers the channel resistance, with the result that Q is high. By decreasing the voltage at the cathode v^+ , the AMOS enters the depletion-mode, moving from point *A* to region *B*. Majority carriers are repelled from the surface of the channel, and the carriers are recombined to form the depletion region. Since there are fewer conductive carriers in the channel, the channel resistance increases and therefore Q decreases according to (3.15). The Q decreases as v^+ decreases, until the voltage becomes so negative that

minority carriers start to accumulate at the surface of the channel. There are two reasons for this: (a) while R_v is lower in the accumulation mode, C_v in the inversion mode is about 4.5 times lower¹ than in the accumulation mode given by C_{max}/C_{min} , therefore Q in the inversion mode is better than in the accumulation mode according to (3.15), and (b) high Q parasitic capacitance such as overlap capacitance dominates in inversion mode, so that the overall Q of the AMOS device increases [Fon02e].

Finally, a performance summary is given in Table 3.2.

Table 3.2: AMOS varactor performance summary

technology	0.13 μ m SOI CMOS
tuning voltage	$\pm(0.9)$ V
capacitance	16% - 97% of C_{ox}
C_{max}/C_{min} ratio	6
Q	95 - 170 at 1 GHz

3.2.4 SOI vs. Bulk

In this section, the performance of AMOS is compared between SOI and bulk technology using device simulation [MEDICI]. The simulated C-V curves, shown in Figure 3.20, demonstrate that C_{ss} in bulk is much larger than in SOI. This is because the parasitic capacitance formed from the depletion region between the n-well and the p-substrate is larger than that formed from the buried oxide between the S/D region and the p-substrate. For cathode excitation (C_{gg}), the C-V characteristics for both SOI and bulk are the same because the anode is analog grounded.

1. Note that the Q is only measured down to a control voltage of -0.6 V due to apparatus limitation.

As will be described in Chapter 4, the C_{gg} and C_{ss} ¹ symmetry is crucial for differentially-tuned varactor topology for good common-mode noise rejection [Fon02b], for which the ideal case is

$$C_{gg} = C_{ss} \quad (3.17)$$

Therefore, SOI offers much better symmetry for common-mode rejection, which is critical for low-voltage VCO design. Finally, from simulation, Q is roughly the same for both technologies.

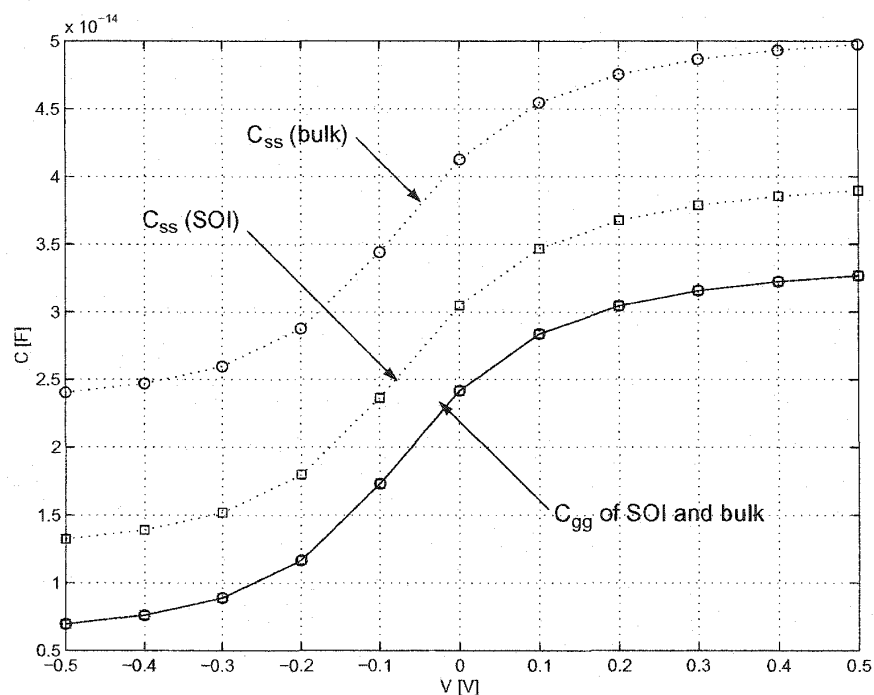


Figure 3.20 Simulated C-V curves of SOI vs. bulk AMOS at 10 GHz

1. C_{gg} is capacitance seen from the gate (cathode), and C_{ss} is capacitance seen from the source (anode).

3.3 Test Pads

Since both inductors and varactors are high- Q , high-frequency elements, test pad design becomes trickier because parasitics in the pad may lower the Q of the device under test (DUT) significantly. One of the most commonly used probes for the passives in this work is the ground-signal-ground (G-S-G) probe. The pad design and its philosophy is shown in Figure 3.21.

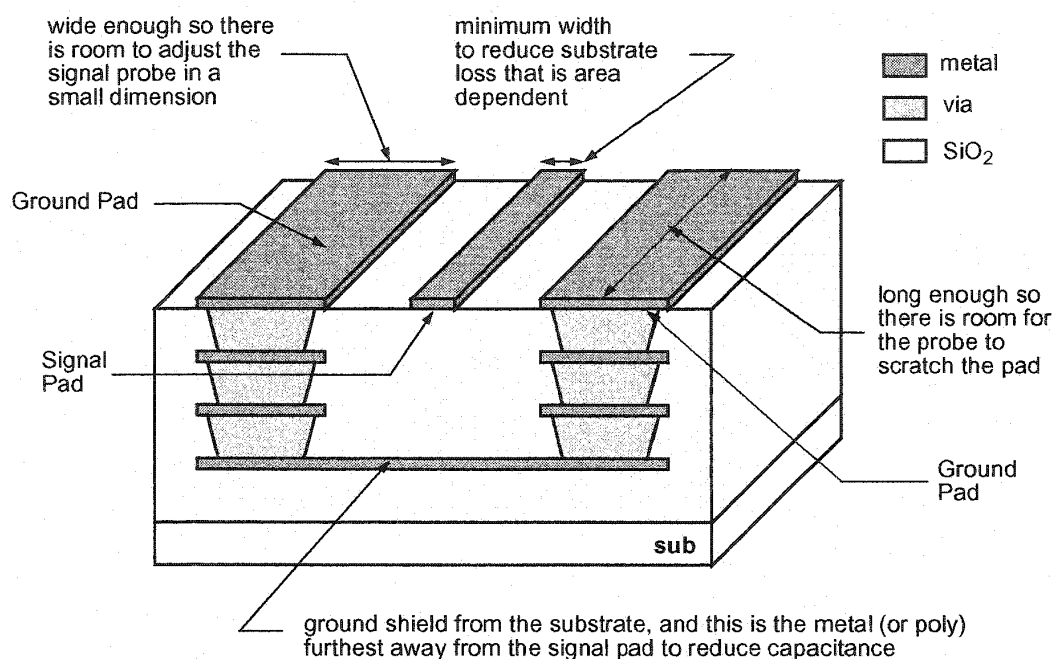


Figure 3.21 Test Pad Design

Since substrate loss is area dependent, the signal pad is made as small as possible. The ground shield is very important for RF measurement. First it connects all the ground pads together to provide a single reference level, as very often the probe does not have the grounds shorted together at the probe tip. However, the most important feature of the ground shield is that it isolates the signal pad from the substrate. With the parasitic capacitance defined by the top and bottom level metal (or poly), de-embedding is much easier and more accurate. A standard open-and-short de-embedding scheme is used to subtract the pad parasitics.

3.4 Summary

In this chapter, two important passive components, namely the inductor and varactor, for radio applications were discussed. First, the structures and theories of monolithic inductors were explained. The design of the single-loop inductor was given, and a 0.85 nH horseshoe inductor with single-ended Q over 20 between 2 to 5 GHz was measured. Then, the design of a multi-turn, multi-level area-efficient IF inductor was presented, with the measured inductance of 16 nH between 100 MHz to 1.6 GHz. Next, the AMOS varactor was mentioned. The physical operation principal was explained, and the figure of merits, C_{max}/C_{min} ratio and Q , were defined to evaluate the performance of the component. The varactor has a measured C_{max}/C_{min} ratio of 6 over a tuning voltage of ± 0.9 V, with Q over 95 at 1 GHz. Finally, the design of the test pads used for measurement was discussed.

Chapter 4 Voltage-Controlled Oscillator

A voltage-controlled oscillator (VCO) is a one-port circuit that generates a relatively large periodic signal at a particular frequency. This frequency has to be tunable for several reasons, including the need for frequency selection and phase locking when the oscillator is used as a local oscillator for a receiver, and compensation for process variations. The relatively poor phase noise and tuning range of CMOS VCOs are major bottlenecks for RF CMOS receivers in meeting most commercial specifications. The downscaling of CMOS further complicates VCO realization, because the low breakdown voltage of modern submicron transistors limits the operating voltage to less than 1.5 V. This not only imposes further limitations to the already-low tuning range, but also degrades phase noise because the varactor must have a higher gain if the same tuning range is to be maintained. Although this tuning range problem and the associated phase noise degradation is obvious and critical for CMOS VCO realization, it has seldom been addressed in the CMOS literature¹.

In this chapter, the problems of poor phase noise and limited tuning range mentioned above are addressed, and a feasible commercially realizable solution is provided. For phase noise improvement in CMOS VCOs, the general VCO operation theory and design procedure based on the time-invariant Leeson's formula [Lee66] are first reviewed. Then, the cyclostationary noise

1. In other technologies, yes [Bur97]. It is likely that the CMOS world is well aware of the problem, but a solution has not yet been found and therefore the problem is conveniently ignored or forgotten [Wan01][Tie02].

properties in the time-domain are examined using impulse sensitivity function (ISF) [Haj99], and the relationship between the phase noise improvement and waveform symmetry is interpreted. Based on this interpretation, a novel concept of simultaneous g_m and impedance matching that gives better waveform symmetry is introduced, and the proof-of-concept in terms of phase noise improvement is provided by simulations and experimental results.

Next, the problem of poor tuning range of CMOS VCOs at low voltage is explored. The application of high-gain accumulation MOS (AMOS) varactors in SOI as described in Chapter 3 is mentioned. However, such a high gain degrades phase noise, and the relationship between varactor gain and phase noise is discussed. Two solutions, namely band-switching [Fon02a] and differential tuning [Fon02b], are introduced to reduce the degradation¹. The advantage of SOI over its bulk counterpart is significant, and will be discussed in detail. The verification of the developed concepts by simulation and experimental results is given.

Despite the low breakdown voltage, the submicron feature size, together with low-voltage operation, improves the speed of the transistor dramatically. Moreover, the reduced parasitics in SOI allows the varactor to have a reasonable tuning range at very high speed. In order to study the performances of the passives (inductor and varactor) and the actives (PMOS and NMOS transistors in SOI) at very high speed, a 40 GHz complementary LC VCO was designed and implemented. The measurement results are given, and the VCO limitations at very high speed are discussed.

1. Although these two topologies have been used recently [Lov01][Tie01], they have never been used in a low-voltage context for phase noise improvement, and have never been implemented in SOI.

4.1 Topology and Operation Theory

There are many circuit topologies for VCOs, but in this thesis, all the VCOs implemented are based on the complementary LC VCO due to its simplicity and inherently differential nature [Lee98]. The circuit topology is shown in Figure 4.1.

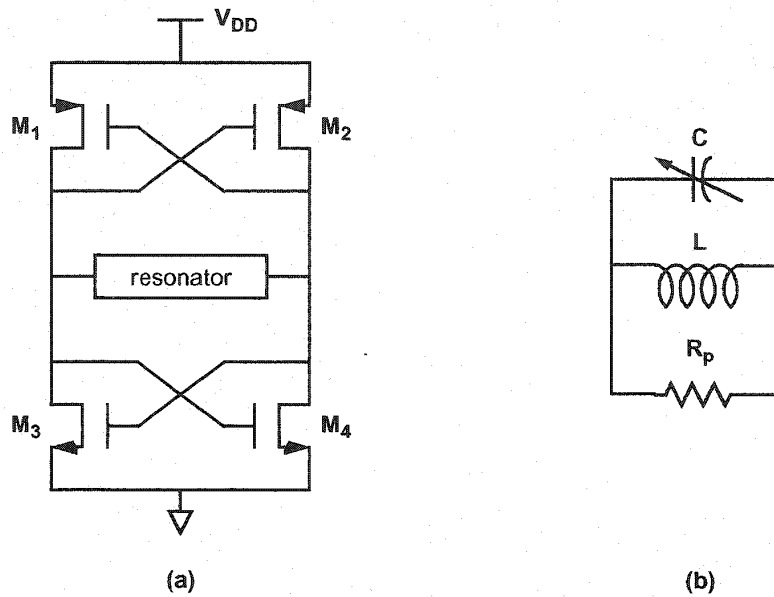


Figure 4.1 (a) Complementary VCO and (b) the associated LC resonator

The complementary VCO consists of a resonator for frequency generation, and both PMOS and NMOS latches to compensate for losses of the resonator. The resonator can be modelled as an inductor L in parallel with a capacitor C^1 , and the resonator losses are lumped as a parasitic resistor R_p^2 as shown in Figure 4.1b. The frequency of oscillation f_o is then given by

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (4.1)$$

-
1. The varactor is modelled as a capacitor to simplify the explanation.
 2. Note that since R_p is connected in parallel, the higher the R_p , the lower the loss.

Since energy is lost due to R_p , extra energy must be provided to maintain the signal amplitude. The latches serve this purpose. Consider the small-signal diagram of a latch as shown in Figure 4.2, assuming the transistors M_1 and M_2 are identical.

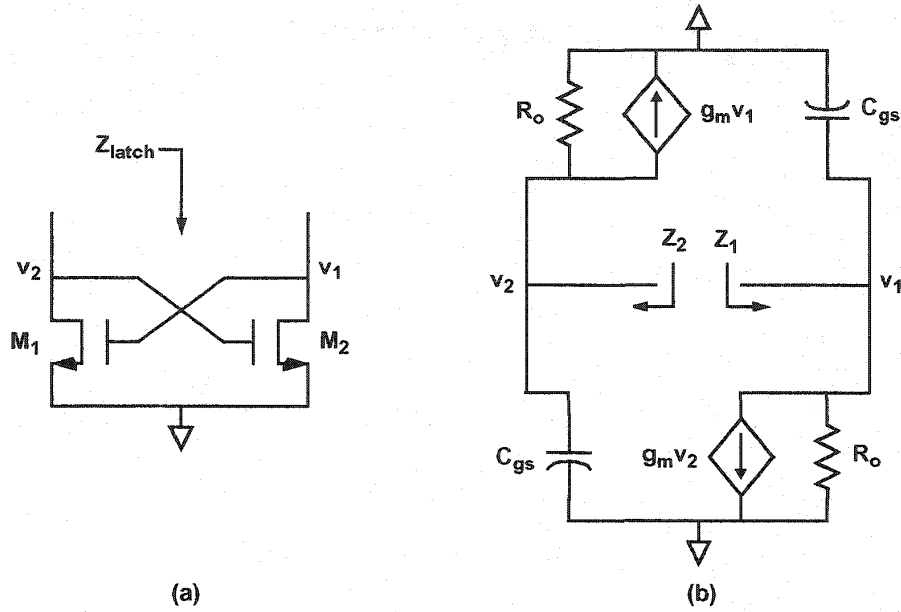


Figure 4.2 (a) Latch schematic and (b) its simplified small-signal model

The equivalent impedance of the latch Z_{latch} is the series equivalent of Z_1 and Z_2 , which are given by

$$Z_1 = v_1 / (g_m v_2) \quad (4.2)$$

$$Z_2 = v_2 / (g_m v_1) \quad (4.3)$$

Since $v_1 = -v_2$, the latch behaves like a negative resistance such that

$$Z_{latch} = -2 / g_m \quad (4.4)$$

which is g_m dependent. For a complementary topology as shown in Figure 4.1a, the equivalent impedance Z_c is given by

$$Z_c = -2/(g_{mp} + g_{mn}) \quad (4.5)$$

where g_{mp} and g_{mn} are the transconductances of PMOS and NMOS respectively. Therefore, for the circuit to oscillate, the following condition must be met¹:

$$|Z_c| \leq R_p \quad (4.6)$$

where R_p is the lumped parasitic resistor as shown in Figure 4.1, and the resonator becomes purely reactive and resonates without amplitude attenuation. In the actual circuit implementation, $|Z_c|$ is often made at least two or three times smaller than R_p to guarantee oscillator start-up. The amplitude is limited by the non-linearity of the transistors such that if the voltage is too high or too low, the node voltage of the resonator turns off the PMOS or NMOS respectively. Such non-linear operation makes the output sinusoidal-like (this is not a perfect sine wave).

The calculation above assumes the inductor is the only parasitic element, and does not include energy loss from the varactor and the active devices. At frequencies below 10 GHz, the accumulation MOS varactor as described in Chapter 3 has very high Q compared to the inductor, therefore its effect on Z_c is insignificant. However, for the transistors, especially with a submicron gate length, the output impedance is significantly lower than that of a long channel counterpart. The output resistance is usually of the order of few hundred ohms, and therefore it must be included for more accurate Z_c estimation. Using the equivalent circuit diagram as shown in Figure 4.3, the overall R_{pVCO} is

$$R_{pVCO} = \left(\frac{1}{R_p} + \frac{1}{2R_{op}} + \frac{1}{2R_{on}} \right)^{-1} \quad (4.7)$$

1. Note that all components are in the parallel configuration.

where R_p is the parasitics from the passives, and R_{op} and R_{on} are the output resistances of the PMOS and NMOS transistors respectively.

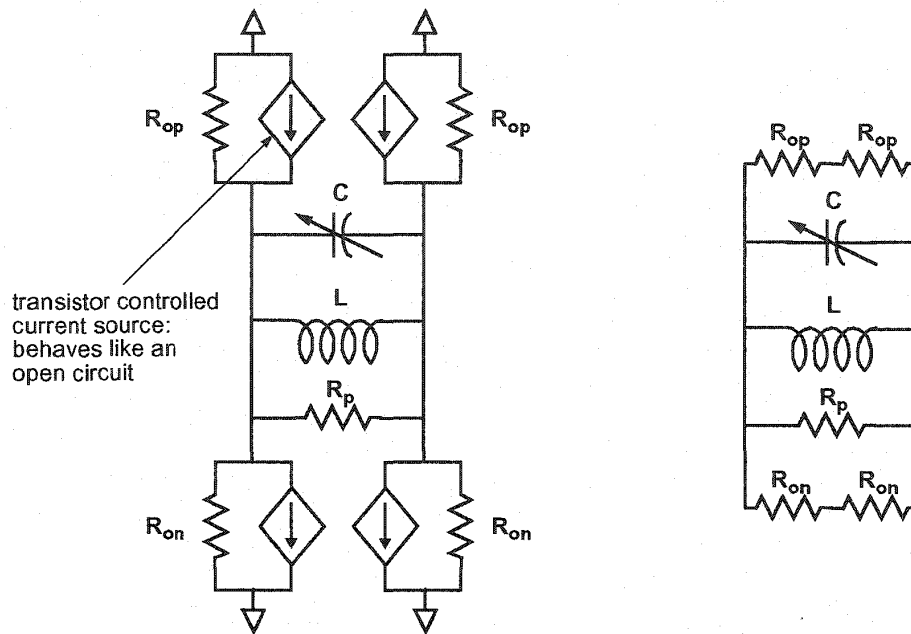


Figure 4.3 Primary parasitic resistances in complementary VCO

4.2 Phase Noise, Leeson's Formula and Oscillator Design

The primary figure of merit¹ of the VCO is the phase noise, which is measured in dBc/Hz. It is a measure of the spectral purity of the signal the VCO generates. Ideally, a delta-function-like spectrum with limited amplitude is desirable, but realistically, different noise sources in the circuit make the spectrum skirt-like as shown in Figure 4.4.

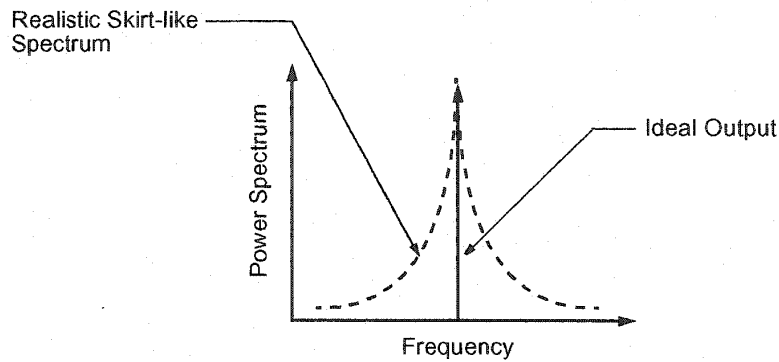


Figure 4.4 VCO output spectrum

Phase noise $\mathcal{L}$ can be described by the well-known Leeson's formula [Lee66]

$$\mathcal{L}(\Delta f) = 10 \log \left(\frac{f_o}{2Q\Delta f} \right)^2 \left[\frac{FkT}{2P_o} \left(1 + \frac{f_c}{\Delta f} \right) \right] \quad (4.8)$$

where f_o is the frequency of oscillation, Q is the quality factor, Δf is the frequency offset from the carrier, F is the noise factor of the amplifier gain element, k is Boltzmann's constant, T is the temperature, P_o is the RF power produced by the VCO, and f_c is the flicker noise corner frequency.

Leeson's formula is based on a time-invariant model, in which the noise sources are assumed stationary and independent of time. However, a better description of phase noise is cyclostationary (time varying). Good examples can be found in [Haj99]. Despite the deficiencies

1. Other figures of merit include power consumption, tuning range and output power etc..

of the model, Leeson's formula provides many important insights for designing a good VCO. The following are the general design procedures used in this thesis, with Q , P_o and F used as design parameters. The minimization of f_c is less obvious, and is described in detail in Section 4.3.

The Q of the resonator is the dominant factor which contributes to the phase noise as described in Leeson's formula. As the Q of the inductor-on-chip is usually poorer than that of the varactor, the major focus is on the Q optimization of the inductor¹, as described back in Chapter 3. Next, (4.8) suggests that phase noise decreases with increasing output signal P_o . To maximize P_o in the complementary VCO, the voltage swing has to be maximized. This can be achieved by setting the dc operating voltage at the resonator to $V_{DD}/2$ by making the g_m of the PMOS the same as that of the NMOS:

$$g_m = g_{mp} = g_{mn} \quad (4.9)$$

Then, the current I_{DD} required to achieve a maximum swing of V_{DD} is calculated using

$$I_{DD} = \frac{V_{DD}}{R_{pVCO}} = \frac{V_{DD}}{Q\omega_o L} \quad (4.10)$$

with the approximation that the inductor is the dominant contributor to Q of the circuit. This current I_{DD} represents the minimum current required to achieve maximum output swing. Further increases in I_{DD} will not improve P_o but increase the drain noise, degrading the noise factor F . Therefore, I_{DD} is the optimum current for the best phase noise achievable, provided that it can generate enough energy for the VCO to start up and oscillate. This can be verified by the value of g_m for a given I_{DD} . First, the transistor dimensions, namely width w and length l , are estimated by the square law model:

$$I_{DD} = k_p \frac{w}{l} (V_{gs} - V_{th})^2 \quad (4.11)$$

1. However, this is not true at very high frequency such as 40 GHz, and details are given in Section 4.8.

where k_p is given approximately by $\mu_n C_{ox}/2$, V_{gs} is $V_{DD}/2$, and V_{th} is the threshold voltage of the device. Then, g_m is given by

$$g_m = 2k_p \frac{w}{l} (V_{gs} - V_{th}) \quad (4.12)$$

Hence, the g_m in (4.12) must be checked against (4.5) and (4.6) to ensure the transistors provide enough energy for oscillation. Once the oscillation condition is confirmed, the phase noise minimization problem is reduced to inductor optimization¹ because noise factor F is a function of I_{DD} , and I_{DD} is directly related to Q from (4.10).

Once the inductance L is determined, the required capacitance C can be easily calculated by using (4.1). However, care must be taken to ensure that the varactor is large enough to provide enough tuning range, and this is discussed in Section 4.5.

4.3 Waveform Symmetry

As pointed out by many [Wei94][Dem00], the phase noise in a VCO is time-varying, and a better assumption for the phase noise behaviour is cyclostationary: that is, the phase noise behaviour repeats itself for every cycle of oscillation. If a time-varying model is used, flicker noise upconversion can be minimized by exploiting waveform symmetry for example [Bra00], by using the impulse sensitivity function (ISF) [Haj99]. The ISF is a periodic function that describes the sensitivity of an oscillator to phase perturbation due to the amplitude noise for the circuit. Ideally, making ISF zero results in no conversion of amplitude noise to phase noise. Of course, anything ideal is impossible, but one can minimize certain noise conversions from certain frequencies by manipulating the ISF. One classic example given in [Haj99] is flicker noise upconversion. If the waveform is half-symmetrical (i.e., no even harmonics), the flicker noise upconversion is minimal. Mathematically, the waveform $f(t)$ is given by

$$f(t) = -f(t \pm T/2) \quad (4.13)$$

1. Design for inductance, frequency of operation and peak Q .

where T is the period of the waveform. This has been confirmed by [Pos98], and is summarized as follows:

1. for minimal flicker noise upconversion, the waveform is half-wave symmetrical as given by (4.13);
2. DC offset does not affect waveform symmetry;

ISF provides insights to the waveform properties in the time domain, overcoming the deficiency of the time-invariant model. This is especially important for CMOS VCOs because upconverted flicker noise from the MOS transistor is comparable to the noise caused by the loss in the resonator¹. Despite the good waveform treatment by ISF, it is mathematical and indirect, and design using ISF involves certain parameter optimizations. In the following section, a simple physical model of waveform symmetry is introduced, providing an alternative for understanding the relationship between waveform symmetry and phase noise. Then, a new design methodology based on the insights gained by this model is developed.

4.3.1 A Physical Waveform Symmetry Model

The shortcoming of the time-invariant model is that amplitude noise is assumed to be time-independent. The ISF model, assuming that the noise is cyclostationary, resolves the problem by including the amplitude noise as a function of time and expressing it as a periodic function. ISF analysis suggests that phase noise is the most sensitive at the zero crossing, where the amplitude noise causes the most phase jitter. Therefore, for simplicity, the model assumes that phase noise is purely determined at this location. Furthermore, the switching is fast at the zero crossings for negative g_m VCOs, and therefore the waveform near the zero crossings is considered to be linear as shown in Figure 4.5. With these two assumptions, the phase deviation ϕ due to amplitude noise described by voltage v_n is given by

$$\phi = \frac{2\pi}{T} \cdot \frac{v_n}{S} \quad (4.14)$$

1. The flicker noise of the transistor is much lower in bipolar technology, and the loss of the resonator usually dominates. Therefore, flicker noise upconversion is not as important.

where T is the period, and S is the slew rate (slope) of the waveform near the zero crossing.

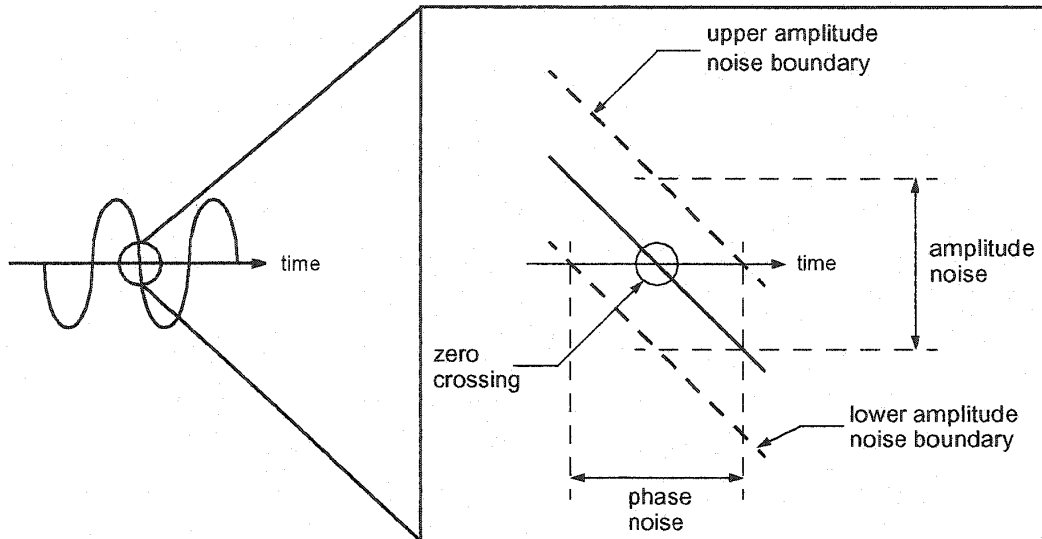


Figure 4.5 Relationship between amplitude noise and phase noise in the time-domain

For a given period, there are two zero crossings: one when the signal slews up with the slope defined as S_u , and the other when the signal slews down with the slope defined as S_d . For a given frequency of oscillation f_o , the slews add up to a constant such that

$$\frac{1}{S_u} + \frac{1}{S_d} = k \quad (4.15)$$

where k is a constant defined by f_o . The slopes S_u and S_d have opposite sign. Next, two assumptions are made: (a) v_n is independent of time, and (b) the magnitude of v_n is the same for both slew-up and slew-down. Then, the phase noise for a given period T is

$$\phi^2 = \left(\frac{2\pi}{T}\right)^2 \left[\left(\frac{v_n}{S_u}\right)^2 + \left(\frac{v_n}{S_d}\right)^2 \right] \quad (4.16)$$

Substituting S_d from (4.15) into (4.16) and setting $d\phi/dS_u$ to zero results in S_u for minimum ϕ :

$$k = \frac{2}{S_u} \quad (4.17)$$

Putting (4.17) back into (4.15) gives

$$|S_u| = |S_d| \quad (4.18)$$

that is, the slew rates of the up-and-down cycle are the same. This corresponds to the half-wave symmetry using ISF with only the two zero-crossings of the oscillation waveform are considered. Both theories suggest that noise upconversion from even harmonics is minimized if the waveform is symmetrical, and hence the overall phase noise is reduced. In fact, this model can be considered as a simplified version of ISF method with v_n generalized. However, rather than using extensive simulations to optimize the waveform symmetry using ISF, the simple model suggests that phase noise is minimal as long as (4.18) is met: if the noise is uncorrelated and equal in magnitude, making the up and down slew rate the same will minimize phase noise, regardless of the individual noise contribution. This simplified VCO design dramatically.

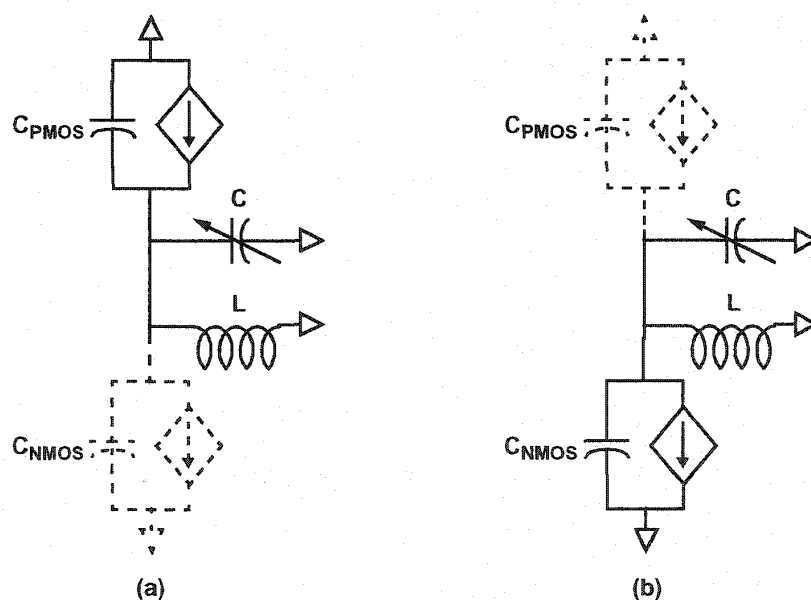


Figure 4.6 Simplified single-sided model of complementary VCO at (a) signal swinging up and (b) signal swinging down

For circuit realization, the slew rate is usually not the same for S_u and S_d due to the asymmetry of the active devices. Consider the simplified single-sided equivalent circuit as shown in Figure 4.6. The resonator sees a different impedance when the signal swings up and down. To a first order (i.e., only C_{gs} is concerned), the frequency shifts for every half a cycle, and the resultant resonant frequency is given by

$$f_o = \frac{1}{\pi} [\sqrt{L(C + C_{PMOS})} + \sqrt{L(C + C_{NMOS})}]^{-1} \quad (4.19)$$

For the waveform to be symmetrical as given in (4.13), transistor impedance seen by the resonator must be the same, resulting in:

$$C_{PMOS} = C_{NMOS} \quad (4.20)$$

4.4 Simultaneous g_m and Impedance Matching of PMOS and NMOS

4.4.1 Theory

As described in the previous sections, the phase noise of the VCO can be minimized by doing the following:

1. “ g_m matching”: the g_m of both PMOS and NMOS transistors should be the same such that

$$\frac{w_{PMOS}/l_{PMOS}}{w_{NMOS}/l_{NMOS}} = \frac{k_{pNMOS}}{k_{pPMOS}} \quad (4.21)$$

where k_p is the process parameter of the transistor. This condition allows maximum output voltage swing;

2. “impedance matching”: the input impedances seen by the resonator, determined by C_{gs} of the transistors, are the same as given in (4.20) to achieve half-wave symmetry, which leads to

$$w_{PMOS} \cdot l_{PMOS} = w_{NMOS} \cdot l_{NMOS} \quad (4.22)$$

If minimum gate lengths are used such that $l_{PMOS} = l_{NMOS}$, condition (4.21) and (4.22) cannot be satisfied simultaneously because $k_{pPMOS} \neq k_{pNMOS}$ ¹. In most of the literature [Mue00][Tie01], “impedance matching” is preferred over “ g_m matching”, because upconverted flicker noise is the major noise contributor in CMOS VCOs, and output signal power P_o gained from “ g_m matching” is not as significant.

It is, however, possible to satisfy both conditions simultaneously. This can be achieved by *not* using the minimum gate length for NMOS. This frees up the design parameter l_{NMOS} , making (4.21) and (4.22) solvable simultaneously. Analytically, using (4.12) and the square law model, the required w and l for both PMOS and NMOS for simultaneous g_m and impedance matching are:

$$l_{PMOS} = l_{min} \quad (4.23)$$

$$w_{PMOS} = \frac{g_m}{2k_{pPMOS}(V_{DD}/2 - V_{th})} \cdot l_{min} \quad (4.24)$$

$$l_{NMOS} = \sqrt{\frac{k_{pNMOS}}{k_{pPMOS}}} \cdot l_{min} \quad (4.25)$$

$$w_{NMOS} = \frac{g_m}{2\sqrt{k_{pPMOS} \cdot k_{pNMOS}} \cdot (V_{DD}/2 - V_{th})} \cdot l_{min} \quad (4.26)$$

where l_{min} is the minimum gate length.

Using non-minimum gate length degrades the speed of the transistor. However, in complementary topology, the PMOS transistors limit the performance, thus using non-minimum gate length for NMOS does not necessarily hinder the overall circuit performance. Finally, aside from serving the purpose for simultaneous matching of g_m and impedance, the use of non-minimum gate length has the following advantages. First, the flicker noise of the transistor is

1. k_{pNMOS} is usually 3 times larger than k_{pPMOS} .

reduced with increasing transistor length. For the BSIM3 [BSIM] model, the flicker noise current density is given by:

$$\overline{i_f^2} = \frac{k_f \cdot I_{DD}^\alpha}{f \cdot C_{ox} \cdot l^2} \quad (4.27)$$

where k_f is the flicker noise coefficient, α is flicker noise exponent, f is the frequency and C_{ox} is the gate oxide capacitance per unit area. Second, from the square law model, the output impedance R_o of the transistor improves with increasing gate length by reducing the channel length modulation λ because

$$R_o \equiv \frac{1}{\lambda I_{DD}} \quad (4.28)$$

and λ is given by

$$\lambda = \frac{k_{ds}}{2 \cdot l \cdot \sqrt{V_{DS} - v_{on} + \phi_b}} \quad (4.29)$$

where k_{ds} and ϕ_b are process parameters¹, V_{DS} is the voltage between the source and drain of the transistor, which is $V_{DD}/2$ in complementary VCOs, and v_{on} is the on-voltage given by $V_{gs} - V_{th}$. An increase in R_o reduces the loss of R_{pVCO} given by (4.7), which results in a phase noise improvement because of the higher Q of the circuit. At the same time, lower loss requires less negative g_m , and hence less I_{DD} because

$$g_m = \frac{2I_{DD}}{v_{on}} \quad (4.30)$$

1. $k_{ds} = \sqrt{\frac{2\epsilon_{st}\epsilon_0}{qN_A}}$ and $\phi_b = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$, where ϵ is the permittivity, q is the charge of an electron, k is

Boltzmann's constant, T is the temperature in Kelvin, N_A and N_D are the doping of the p- and n-type material respectively, and n_i is the carrier concentration of intrinsic silicon.

and hence the noise factor F is lower (due reduced drain shot noise).

4.4.2 Design and Simulation

The key for simultaneous g_m and impedance matching relies on the use of non-minimum gate length for NMOS transistors. The rest of the design procedure is the same as given in Section 4.2. Once the required g_m was determined, the w and l for PMOS transistors were found by (4.23), (4.24) and circuit simulation.

The input impedance of the PMOS latch Z_{PMOS} was then determined by small-signal simulation across the frequency band of interest as shown in Figure 4.7, with the nodes at v_1 and v_2 set to $V_{DD}/2$. Next, the NMOS latch was designed. To achieve simultaneous g_m and impedance matching, I_{DD} and Z_{NMOS} of the NMOS latch were made the same as I_{DD} and Z_{PMOS} of the PMOS latch. Equations (4.25) and (4.26) were used for an initial guess, and the design was then refined using circuit simulation, as shown in Figure 4.8. For a first-order approximation, only the imaginary parts of Z_{PMOS} and Z_{NMOS} are matched because waveform symmetry is dominated by capacitive matching as given by (4.20).

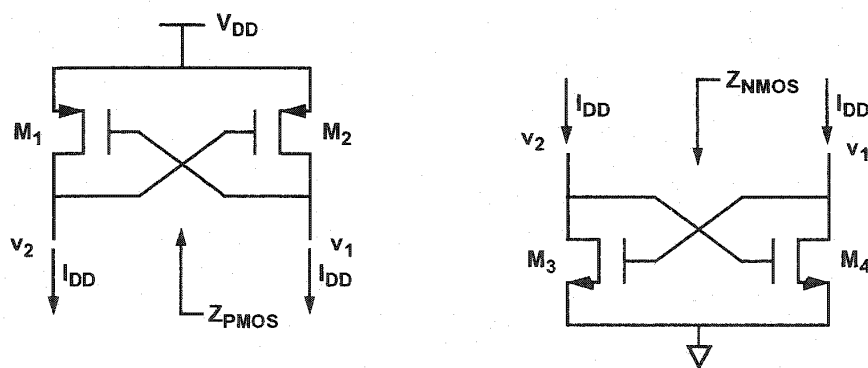


Figure 4.7 Simultaneous g_m and impedance matching

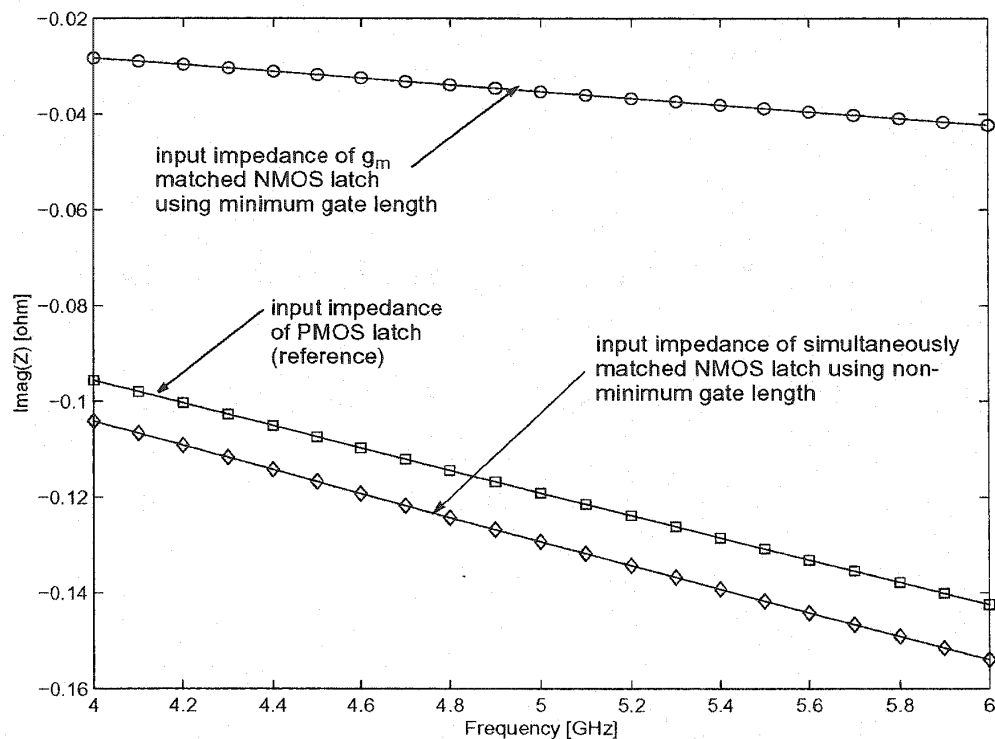


Figure 4.8 Impedance matching with s-parameter simulation in the band of interest

The latches were put together with the resonator to construct the VCO as shown in Figure 4.9. A band-switching topology was used for varactors, using AMOS capacitors with nominal capacitances 0.4 pF (C_1), 0.4 pF (C_2) and 1.2 pF (C_3). More detail is given in Section 4.6. The inductor is a horseshoe-shaped single loop as described in Chapter 3. The measured inductance is 0.85 nH with Q greater than 20 across the band of interest, which is between 3.0 GHz to 5.6 GHz. The bias-T is used as an inductive choke for measurement purposes. Further details are given in Section 4.9.

4.4.3 Experimental Result

The VCO was measured using wafer probing together with a 26.5 GHz HP8563 spectrum analyzer with a phase noise module. The frequency vs. tuning voltage is shown in Figure 4.10. C_3 was the tuning varactor, and C_1 and C_2 are switching capacitors for band-switching. The VCO can be tuned from 3.0GHz to 5.0GHz for a tuning voltage of ± 0.7 V, and a tuning range of 50% with frequency centred at 4.0GHz. The frequency tuning is discussed in further detail in Section 4.6.3.

The phase noise was measured using the phase noise module of the HP8563 spectrum analyser. At 1 MHz offset, the best phase noise of -125.2 dBc/Hz was measured at 3.0 GHz and 1.4 V V_{DD} , as shown in Figure 4.11.

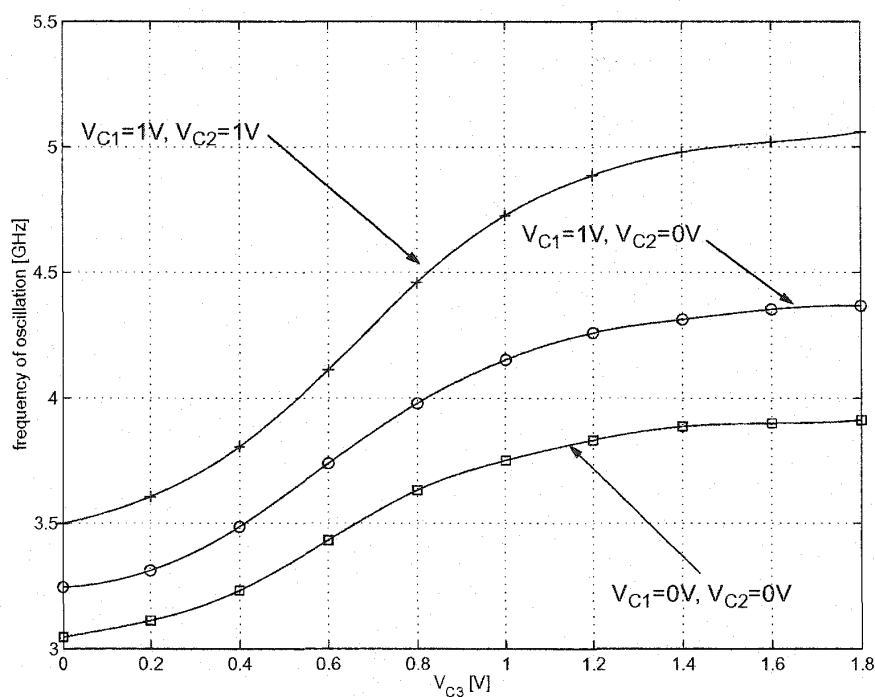


Figure 4.10 Frequency vs. tuning voltage V_{C3} of simultaneously matched VCO

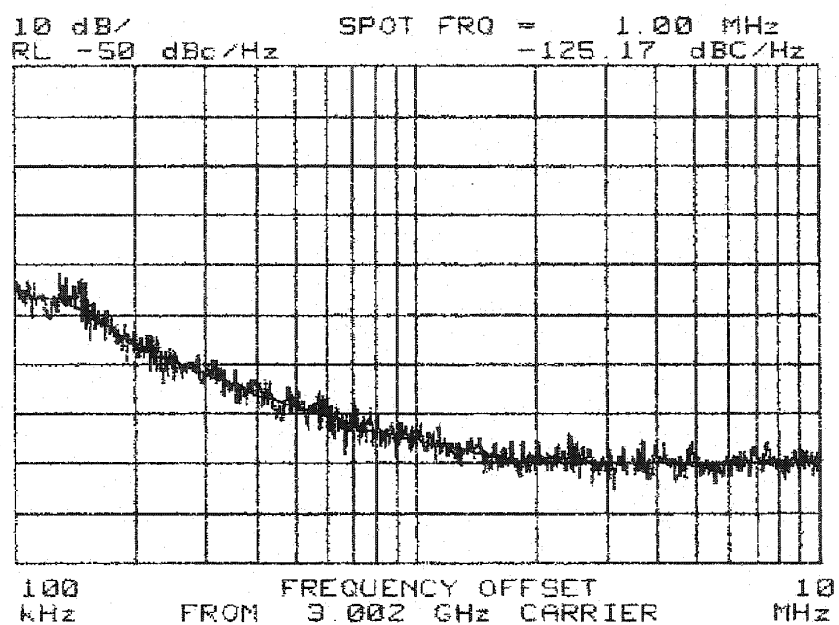


Figure 4.11 Phase noise vs. frequency offset from carrier of simultaneously matched VCO

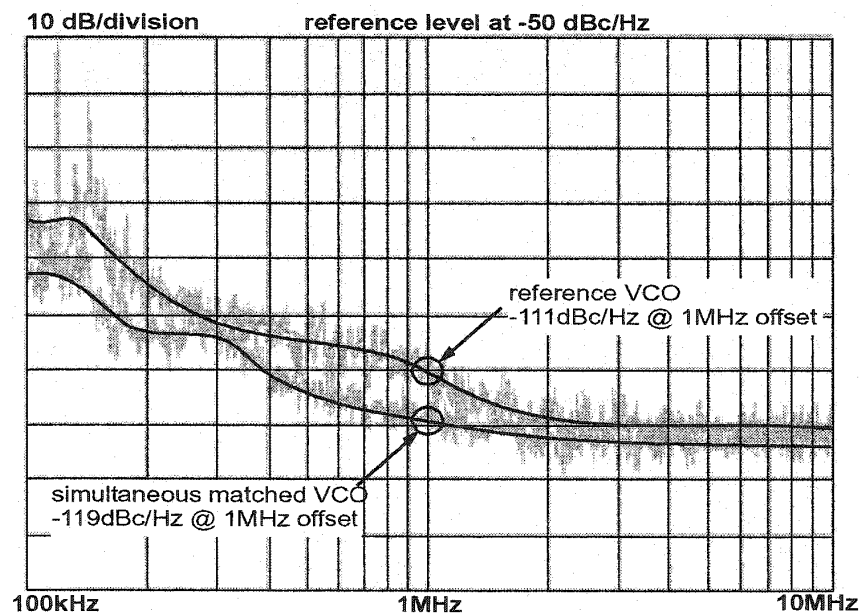


Figure 4.12 Phase noise comparison at centre frequency of 3.7 GHz and 1 V V_{DD}

The simultaneous matched design was then compared with minimum-gate length designs for improvement verification. A reference VCO was fabricated with minimum-gate length and a g_m matched NMOS latch, while all other components (resonator and PMOS latch) remained the same. The frequency was set to 3.1 GHz, where the large varactor C_3 was operating in the *high-gain region* as is described in Section 4.6 [Fon02a]. The VCOs were measured at 1 V V_{DD} , and their phase noise is shown in Figure 4.12. At 1 MHz offset, the phase noise was improved by a total of 8 dB using the described technique. The output power of both VCOs is -9 dBm over the tunable frequency range, indicating no voltage swing reduction using this technique.

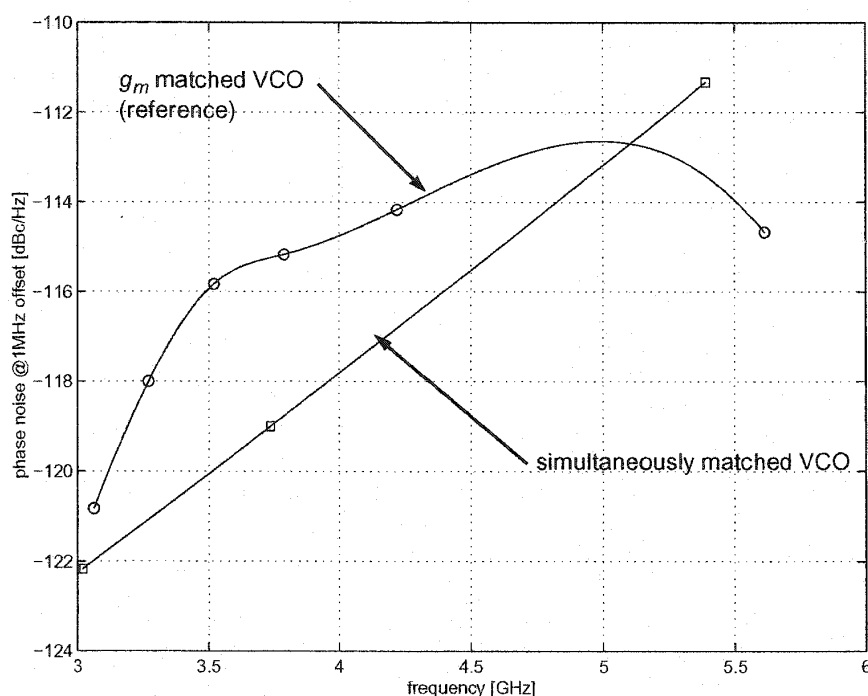


Figure 4.13 Phase noise (at 1MHz offset) vs. frequency for 1 V V_{DD}

The phase noise was then measured across of the band of interest. The result at 1 V V_{DD} and frequency offset of 1 MHz is shown in Figure 4.13. Using the described technique, the phase noise improves at the lower frequency but degrades as the frequency approaches the upper band. This is because non-minimum gate length decreases the speed of the transistor (f_T) and increases

C_{gs} significantly. The circuit draws more current, increasing drain noise and hence the phase noise of the VCO. The phase noise is measured in the low varactor gain region (Section 4.5.2).

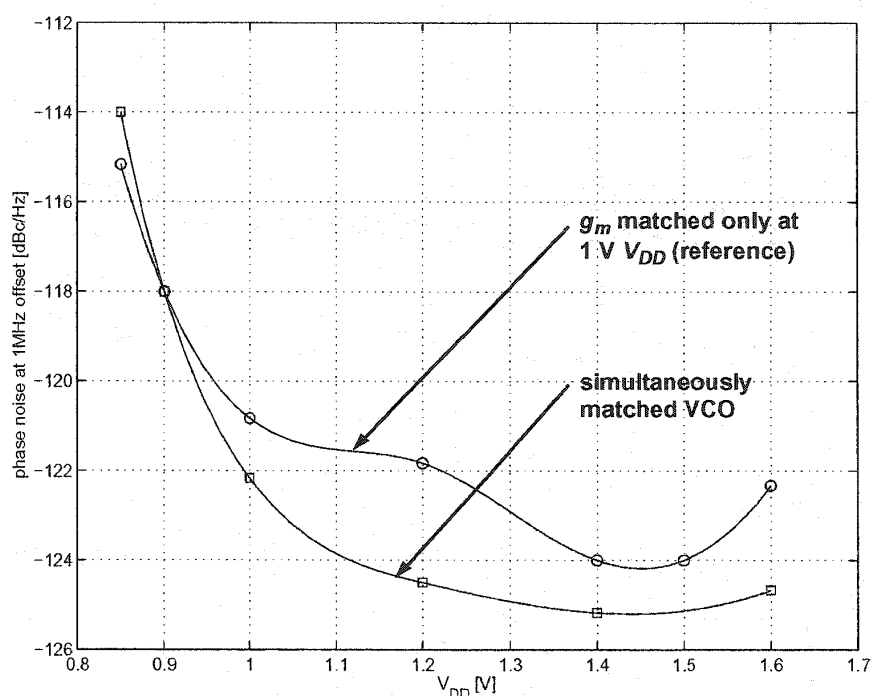


Figure 4.14 Phase noise vs. V_{DD} at 3.1 GHz (1 MHz offset frequency)

Next, both VCOs were swept at different values of V_{DD} to study the improvement versus the supply. The result of phase noise vs. V_{DD} at a centre frequency of 3.1 GHz at a 1MHz offset is shown in Figure 4.14. This frequency was chosen because it gives the best phase noise for both VCOs. As shown, the simultaneous matched VCO has a better phase noise as compared to the reference VCO across all the supply V_{DD} , demonstrating the advantage of the technique. The phase noise was also measured across of the band of interest. The result at 1 V V_{DD} and a frequency offset of 1 MHz is shown in Figure 4.13.

The summary of the measured VCO performance is listed in Table 4.1.

Table 4.1: Performance summary of simultaneous matched VCO

frequency tuning (tuning voltage)	3.0 - 5.5 GHz (± 1 V)
nominal V_{DD}	1.0 V
nominal phase noise at 1 MHz offset	-122.0 dBc/Hz (3.0 GHz, 1.0 V V_{DD})
best phase noise at 1 MHz offset	-125.2 dBc/Hz (3.0 GHz, 1.4 V V_{DD})
worst phase noise at 1 MHz offset	-110.0 dBc/Hz (5.4 GHz, 1.0 V V_{DD})
output power	-9 dBm
power consumption	2.5 mW

4.5 Low-Voltage Frequency Tuning

Frequency tuning is the most basic function of VCOs. In LC-type VCOs, frequency tuning is achieved by a voltage-controlled capacitor, commonly known as a varactor. Mathematically, the frequency f_o is given by (4.1)

$$f_o(v_{tune}) = \frac{1}{2\pi\sqrt{LC(v_{tune})}} \quad (4.31)$$

where f_o is a function of control voltage v_{tune} , and hence the circuit is called a voltage-controlled oscillator. As a rule of thumb, a minimum frequency tuning of 10% is required to cover the spread in process tolerance. However, many CMOS publications [Wan01][Tie02] tend to ignore the importance of tuning capability, making the VCO impractical for commercial realization.

Yet, there is always a purpose behind such negligence. Limited frequency tuning range has always been a notorious problem for VCOs in CMOS technology. Varactors using reverse biased diode junction capacitance from a p^+/n -well results in limited tuning range around a few percent and poor Q around 20 at 1 GHz [Hun00a]. On the other hand, other than not meeting the tuning

specification, a VCO with limited frequency tuning range does make the reported phase noise more “impressive” due to lack of tunability. This is explained in Section 4.5.2.

The lowering of the voltage supply due to technology scaling further complicates the tuning problem. As the technology advances, the gate length reduces from 0.35 to 0.13 μm , and the maximum supply V_{DD} drops from 3.3 V to 1.5 V. The range of the varactor control voltage v_{tune} decreases accordingly, resulting in a reduction in frequency tuning range if the varactor gain remains the same. Therefore, for low-voltage CMOS VCOs to achieve respectable performance, a high- Q high-gain varactor is required. The accumulation MOS varactor comes to the rescue.

4.5.1 Frequency Tuning using Accumulation MOS Varactor

The SOI accumulation MOS (AMOS) varactor as described in Chapter 3 has a high C_{max}/C_{min} ratio of 6 for a tuning voltage v_{tune} less than ± 1 V. Even for a 1 V supply with v_{tune} of ± 0.5 V, a C_{max}/C_{min} of 3.8 with Q around 100 is achievable as shown in Figure 4.15. It is important to note that it is unfavorable to have v_{tune} exceed V_{DD} . Many CMOS VCOs reported in the literature [Sve00] have a range for v_{tune} greater than the standard power supply, which is impractical in most of the applications.

The high C_{max}/C_{min} ratio of the AMOS varactor implies high VCO gain that degrades phase noise, as is described in the next section. The requirement for low-voltage operation is a further complication. To maintain the desired tuning range, the varactor gain has to be made even larger in order to compensate for the V_{DD} reduction, making the varactor a major noise contributor compared to the inductor. In the following section, the relationship between varactor gain and phase noise is examined, and important insights are developed which lead to possible solutions.

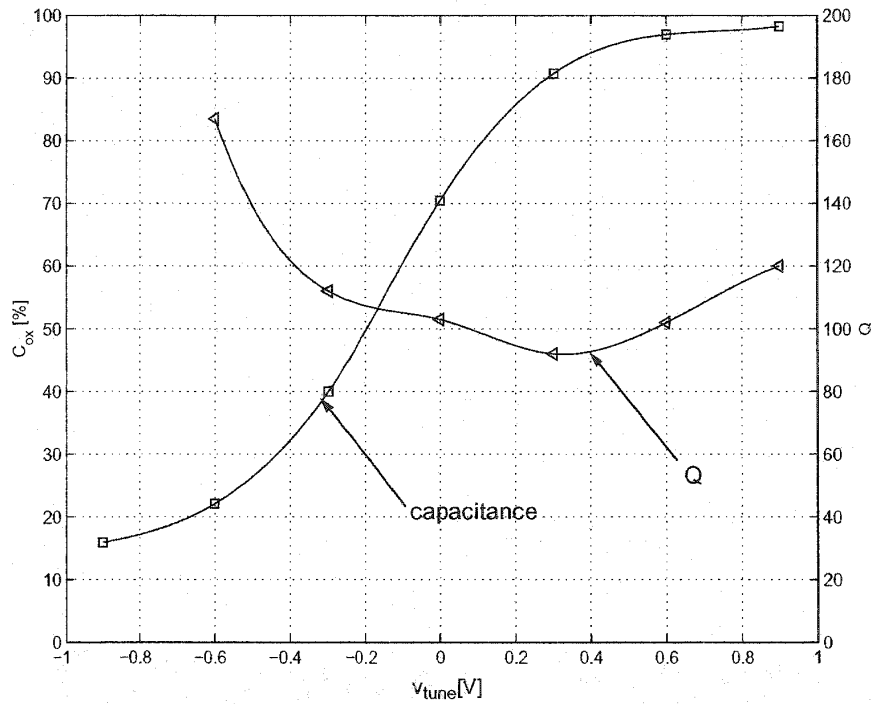


Figure 4.15 Measured C-V and Q-V characteristics of SOI AMOS varactor at 1 GHz

4.5.2 Varactor Gain and Phase Noise

The varactor gain is strongly related to phase noise. To understand their relationship physically, consider a varactor with noise v_n ¹ on the control nodes. Since tuning is usually performed at low frequencies, v_n is therefore considered to be low-frequency noise. The units for noise are $V/\sqrt{\text{Hz}}$. The noise v_n will cause a capacitance perturbation ΔC as shown in Figure 4.16, and hence modulates the frequency of oscillation by

$$f_o = \frac{1}{2\pi\sqrt{L(C + \Delta C)}} \quad (4.32)$$

1. v_n can be noise from the transistor, such as flicker noise and shot noise for example.

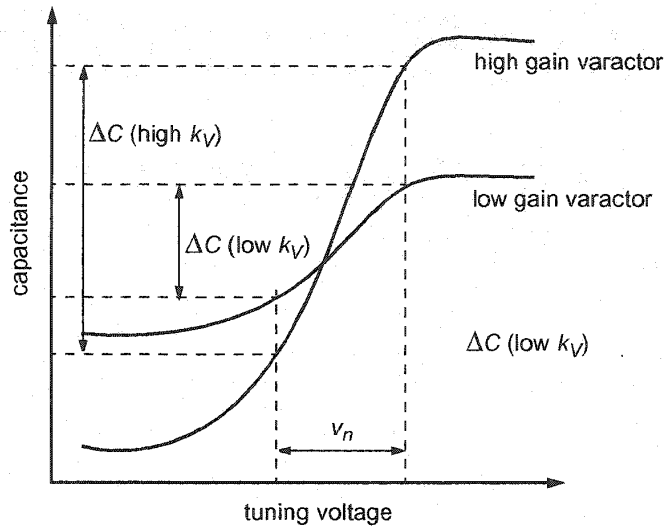


Figure 4.16 Relationship between varactor gain and tuning voltage noise

C is a function of tuning voltage v_{tune} given by

$$C = C_0 + k_V v_{tune} \quad (4.33)$$

where C_0 is the zero-bias capacitance, defined as nominal capacitance, and k_V is the varactor gain.

The magnitude of the perturbation is directly proportional to the varactor gain

$$\Delta C = k_V \cdot v_n \quad (4.34)$$

Therefore, lowering the varactor gain generally reduces the phase noise. The ideal case for best phase noise achievable is using a fixed capacitor instead of varactor, for which k_V is zero. However, this is not feasible because tuning is required to cover the process spread. Equation (4.34) describes one of the most important low-frequency noise upconversion mechanisms for low-voltage VCOs, and it is discussed in further detail in Section 4.7.

The phase noise contribution due to the varactor can be added to Leeson's formula easily [Rog01b]. First, Leeson's formula deals with noise perturbation in the phase/frequency domain, and therefore the parameter VCO gain k_{VCO} (the sensitivity of frequency to tuning voltage) is

more meaningful than varactor gain k_V . These two parameters can be related by differentiating (4.1) with respect to the tuning voltage of the varactor, which gives

$$\frac{df}{dv} = -\frac{1}{4\pi}(LC)^{-3/2}\frac{dC}{dv} \quad (4.35)$$

where df/dv is k_{VCO} , and dC/dv ¹ is k_V . Then, the frequency deviation Δf can be determined by:

$$\Delta f_n = k_{VCO} \cdot v_n \quad (4.36)$$

and the phase deviation θ_d is therefore:

$$\theta_d = \frac{\Delta f_n}{\Delta f} \quad (4.37)$$

with Δf the frequency of offset from the carrier. Then the single-sideband phase noise introduced is:

$$\mathcal{L}(\Delta f) = 20\log(\theta_d/2) \quad (4.38)$$

Adding the extra term in (4.38) results in the modified Leeson's formula [Rog01b]:

$$\mathcal{L}(\Delta f, k_{VCO}) = 10\log\left\{\left(\frac{f_o}{2Q\Delta f}\right)^2\left[\frac{FkT}{2P_s}\left(1 + \frac{f_c}{\Delta f}\right)\right] + \left(\frac{k_{VCO}v_n}{2\Delta f}\right)^2\right\} \quad (4.39)$$

As described in the previous section, a low-voltage VCO requires high k_{VCO} to maintain the tuning range. Therefore, the phase noise degrades accordingly as described in (4.39). In the following sections, two topologies are introduced to reduce such degradation by decreasing k_V (or k_{VCO}) while maintaining the desired tuning range. Although the topologies are not novel, in the literature, they have been used only as a technique to boost tuning range, but have never been used in the phase noise reduction context. This is because k_V was never a problem before the AMOS

1. Just a reminder that C is a varactor and therefore it is a function of voltage.

varactor was introduced in low-voltage circuits. Therefore, the novel applications are considered as part of the contributions of this thesis.

4.6 Band-Switching VCO

The band-switching varactor topology has been around for a while [Lov01], and it has been used extensively to increase the limited tunability of traditional CMOS diode varactors [Che02]. The general topology is shown in Figure 4.17.

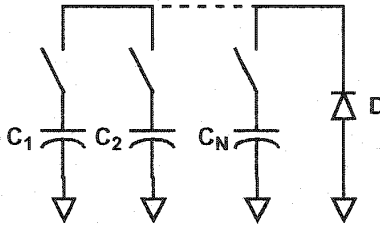


Figure 4.17 Switched-C topology for band-switching

The varactor consists of an array of binary-weighted switched capacitors ($C_1, C_2 \dots C_N$) for band-switching, and a diode varactor D for continuous capacitance tuning. This topology improves both the tuning range and Q of the overall varactor. The tuning range is increased from $C_D(v_{tune})$ to

$$C = \sum_N C_i + C_D(v_{tune}) \quad (4.40)$$

and Q can be improved by making the low- Q diode D smaller, and using high- Q fixed capacitors extensively for tuning.

Nonetheless, the low C_{max}/C_{min} of a diode varactor implies a large switched-C array is necessary to cover the required tuning range. This not only implies large chip area for the fixed capacitors, but also circuit complexity to control the switched-Cs. Furthermore, at high

frequencies such as 40 GHz, the switches impose excessive parasitics that make this topology unfeasible for frequency tuning.

The band-switching topology introduced in this thesis is different [Fon02a]. The novelty lies in the use of AMOS varactors to replace the switches and the fixed-capacitors. As mentioned in the previous section, the primary purpose of band-switching in AMOS is *not* to increase the tuning range but to improve the phase noise. In the following section, the theory, design and experimental results of VCO using band-switching AMOS varactor are given.

4.6.1 Band-Switching AMOS Varactor

While using a pair of AMOS varactors (Figure 4.18a) in the resonator may provide enough frequency tuning for the VCO, the large tuning range implies excessive VCO gain that degrades the phase noise. This can be shown by a modified Leeson's model as given in (4.39). The band-switching topology (Figure 4.18b) can be used to improve the noise performance by reducing the VCO gain while maintaining the desired tunability. Similar to traditional switched-C varactors, the AMOS band-switching topology consists of two sets of varactors: a bank of switching on/off-only varactors ($C_1, C_2, \dots, C_N$), and one continuous varactor C_t for fine tuning. The capacitance of the resonator C is given by

$$C = \sum_N C_i + C_t \quad (4.41)$$

Ideally, the switching varactors have zero k_p , and C_t is the only varactor that v_n can modulate to generate ΔC_t as in (4.34). The noise improvement k_n compared to a single varactor as shown in Figure 4.18a is

$$k_n = C_t / C \quad (4.42)$$

Therefore, C_t should be minimized, and the minimum is limited by the tuning range and the continuity between frequency bands. Although the derivation is simple and obvious, it is seldom mentioned in CMOS VCO publications because a low-voltage high-gain varactor was never an issue in CMOS technology. Therefore it is considered as a contribution of this thesis.

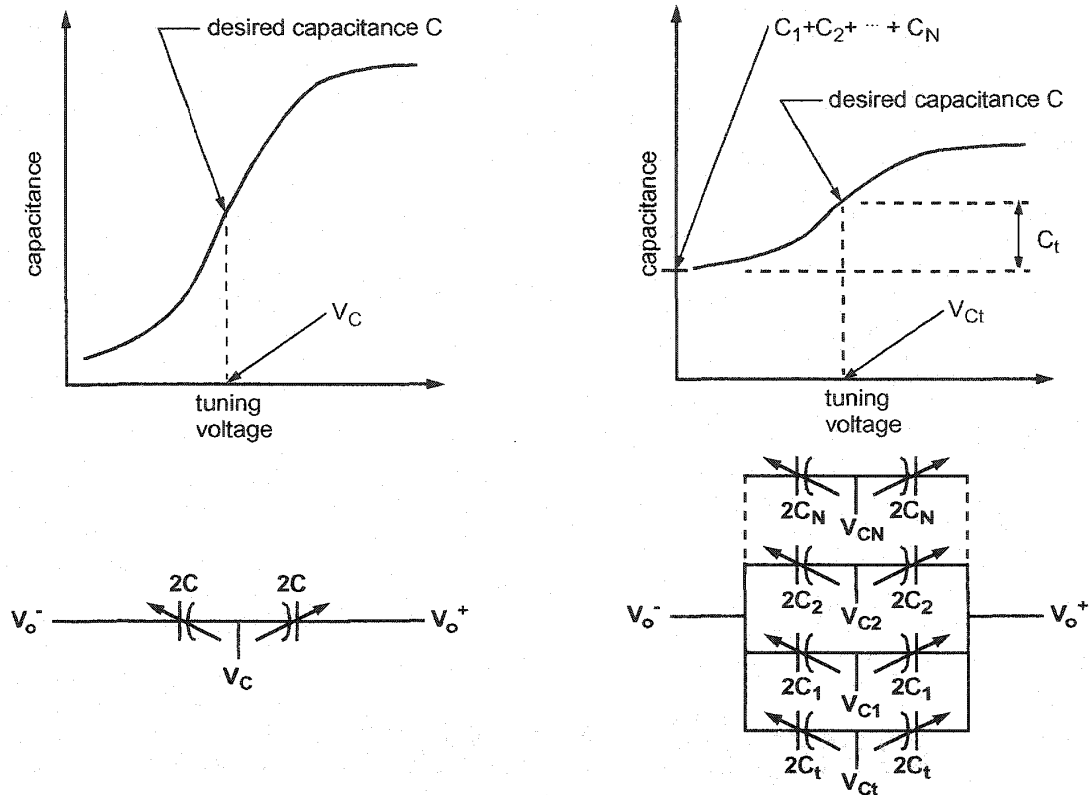


Figure 4.18 (a) Single varactor vs. (b) band-switching tuning scheme

Conventionally, the switching varactor consists of an active switch and a fixed capacitor as described in the previous section. The switching varactor in this topology, however, is different from [Che02], in that it does not require a switch. Consider the AMOS C-V curve as shown in Figure 4.19. Point A (fully on) and point C (fully off) have k_V close to zero, and band switching is achieved by operating the varactor at one of these two points. The drawback is that the C-V characteristic is not symmetrical around a tuning voltage of 0 V, and that the varactor requires ± 0.7 V to switch the AMOS varactor either fully on or fully off. This non-symmetry is due to the parasitic capacitance of the SOI buried oxide C_{box} , which can be reduced by using a high-

resistivity substrate. However, for this given process, a V_{DD} of 1.4 V is required to take advantage of the band-switching topology.

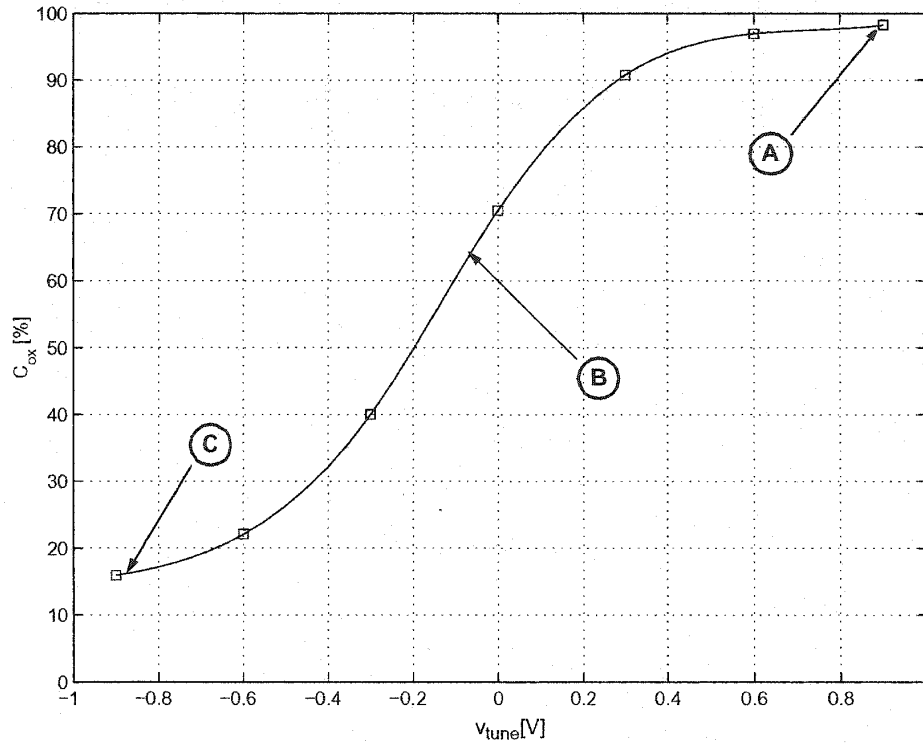


Figure 4.19 AMOS varactor region of operation

Finally, note that a pn diode gives inferior performance in the band-switching topology. Besides the poor Q of the device, the k_V of the diode does not flatten out at the upper tuning end. This is because the C-V characteristic of the pn junction is monotonically increasing, as given by

$$C = \frac{C_{j0}}{(1 - v/\phi_b)^m} \quad (4.43)$$

where C_{j0} is the zero-bias capacitance, ϕ_b the built-in voltage, and m is the exponent which depends on the doping gradient. Therefore, this unique C-V characteristic makes the AMOS

varactor applicable as a switching capacitor, without the penalty of greater chip area and high-frequency isolation.

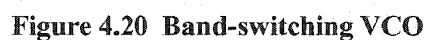
4.6.2 VCO Implementation

The C-V curve as shown in Figure 4.15 (or Figure 4.19) was used extensively to design the AMOS varactor. Before going any further, several parameters are to be clarified:

1. v_{tune} is the voltage across the varactor as described in Chapter 3;
2. The capacitance is measured in percentage of C_{ox} ;
3. nominal capacitance C_{norm} is defined as the capacitance when $v_{tune} = 0$ ¹;

Therefore, the nominal capacitance of the AMOS varactor in this technology is 70% of C_{ox} . C_{max} is approximately the same as C_{ox} , while C_{min} is about 16% of C_{ox} , resulting in a C_{max}/C_{min} of 6. Note that in an AMOS varactor, the off-capacitance is C_{min} instead of zero as in switched-C. Therefore, the binary weighting scheme used in the switched-C topology is usually not the optimal configuration to cover all the possible frequencies within the range. In this design, the VCO consists of an array of three varactors for band-switching: two small varactors C_1 and C_2 with nominal capacitance of 0.4 pF, and one large varactor C_3 with nominal capacitance of 1.2 pF. All varactors can be used as either switching or tuning varactors due to the unique property of AMOS varactors. The monolithic inductor is a horseshoe shaped single loop with a diameter of 460 μm as shown in the micrograph Figure 4.26. The measured inductance is 0.85 nH and Q is above 20 at frequencies between 3.8 and 5.7 GHz as shown in Figure 3.12. The overall VCO schematic is shown in Figure 4.20.

1. Mid-capacitance can be used as an alternative definition for nominal capacitance such that $C_{norm} = (C_{max} - C_{min})/2$ with $v_{tune} = -0.1$ V.



The implemented VCO as shown in Figure 4.20 was measured using wafer probing together with a 26.5 GHz HP8563 spectrum analyzer with a phase noise module. The frequency of oscillation vs. varactor tuning voltage is shown in Figure 4.21, where C_1 and C_2 are the switching varactors, and C_3 is the tuning varactor. For a varactor tuning voltage up to 1.4 V, at V_{DD} of 1 V, the carrier frequency can be tuned between 3.065 GHz and 5.612 GHz, achieving 58.7% tuning range with the centre frequency at 4.353 GHz. Note that 1 V may provide enough tuning capability for many applications. However, to ensure minimal gain for the switching varactors, at least 1.4 V is required to guarantee complete switching between points A and C (Figure 4.19). The frequency-voltage characteristics were also measured for V_{DD} between 0.8 V to 1.6 V. The frequency variation was within 2% of the 1 V V_{DD} measurement, and therefore they are not shown here.

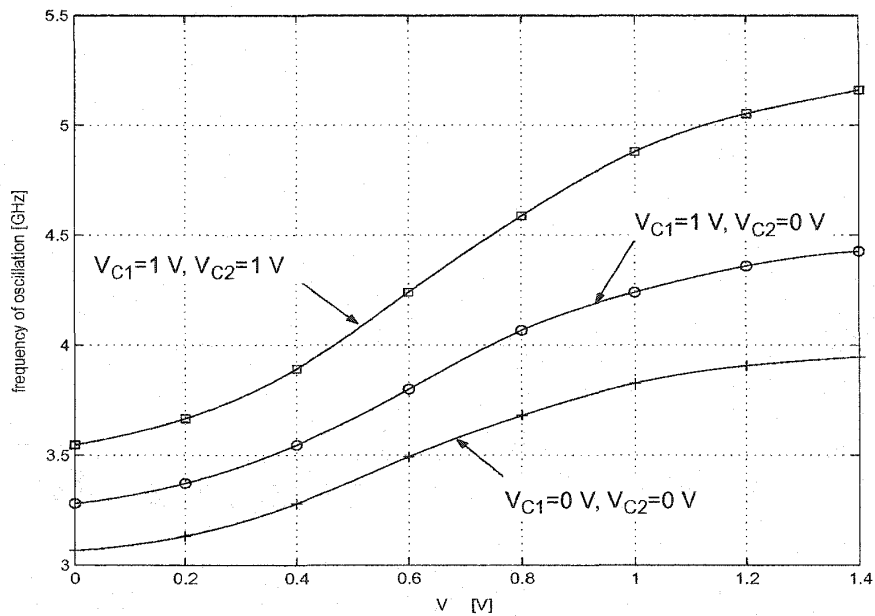


Figure 4.21 Frequency vs. tuning voltage of band-switching VCO

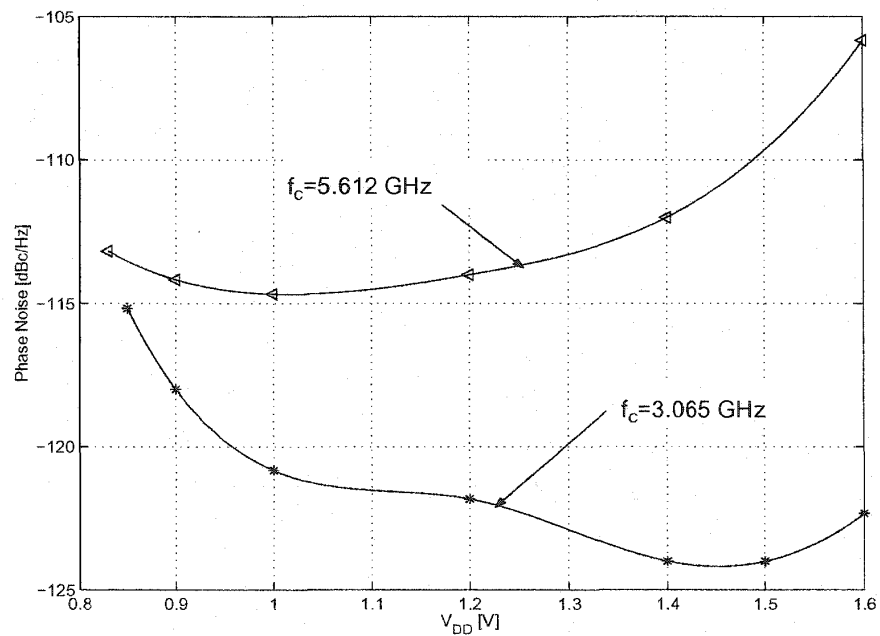


Figure 4.22 Phase noise vs. V_{DD} of band-switching VCO

The phase noise was measured versus V_{DD} using the phase noise module of the HP8563 spectrum analyzer. All varactor tuning voltages were set to either 0 V to give a lower frequency of 3.065 GHz, or to 1.4 V to give the upper frequency of 5.612 GHz. The measured results are shown in Figure 4.22.

The phase noise first improves as V_{DD} increases up to an optimum, then degrades for further increases of the supply. At 3.065 GHz, the best phase noise of -124 dBc/Hz at 1 MHz offset is achieved at the expense of power dissipation by operating the VCO at 1.4 V V_{DD} (power dissipation increases to 8.4 mW compared to 3 mW at 1 V V_{DD} , for which the phase noise is -120.8 dBc/Hz at 1 MHz offset). The phase noise plot is shown in Figure 4.23.

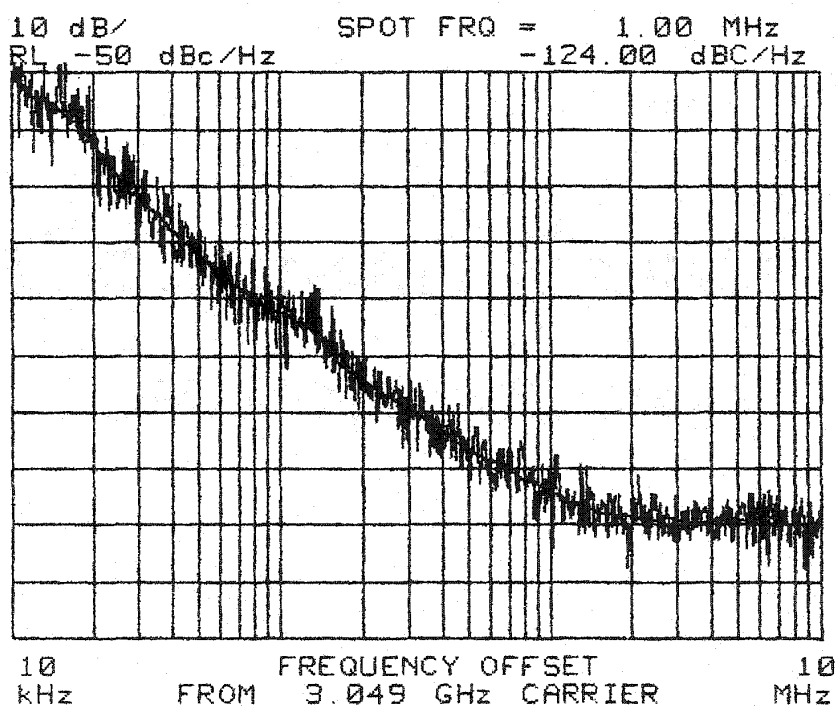


Figure 4.23 Phase noise vs. frequency offset from carrier of band-switching VCO

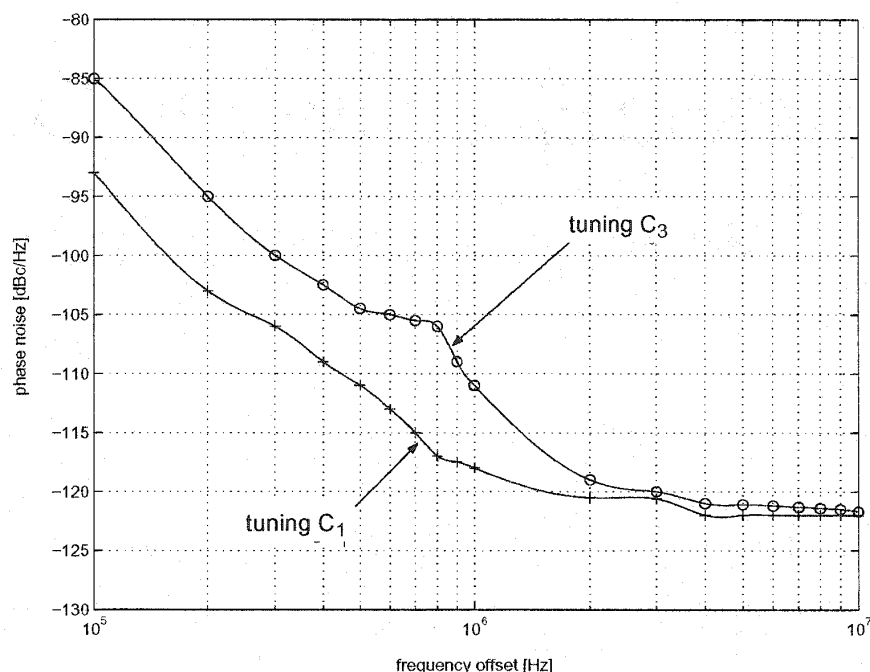


Figure 4.24 Phase noise comparison between tuning C_1 and C_3 of band-switching VCO

The phase noise improvement through reduction of k_V is shown by comparing the continuous tuning using the large varactor C_3 versus the small varactor C_1 . First, C_3 was tuned to 0.5 V so that it operated in region B (Figure 4.19). C_1 and C_2 were fixed to their minimum. The VCO frequency was 3.3 GHz and the phase noise is -111.17 dBc/Hz at a 1 MHz offset.

Next, C_1 was tuned to set the frequency to 3.3 GHz with C_2 and C_3 fixed to the minimum. The phase noise was measured to be -118 dBc/Hz, an improvement close 7 dB as shown in Figure 4.24. The phase noise improves as the varactor gain k_V decreases. Therefore, the worst phase noise is recorded when all the varactors are operating in region B. For 1 V V_{DD} , the worst phase noise was measured when V_{C1} , V_{C2} and V_{C3} were set to 1 V (region B). The frequency of oscillation is 4.88 GHz, and the phase noise is -109 dBc/Hz at a 1 MHz offset.

A widely used figure of merit (FOM) for VCO performance is defined as

$$FOM = \mathcal{L}\{\Delta f\} - 20\log(f_o/\Delta f) + 10\log(P_{dc}) \quad (4.44)$$

where $\mathcal{L}\{\Delta f\}$ is the measured phase noise at the frequency offset Δf from the carrier at f_o , and P_{dc} is the measured DC power dissipation in mW. The result is plotted in Figure 4.25. The best FOM is achieved at 5.612 GHz at a low V_{DD} of 0.83 V, drawing 1.2 mA of current with power dissipation just below 1 mW. The FOM is -188.3 dBc/Hz, with a phase noise of -113.2 dBc/Hz at 1 MHz offset.

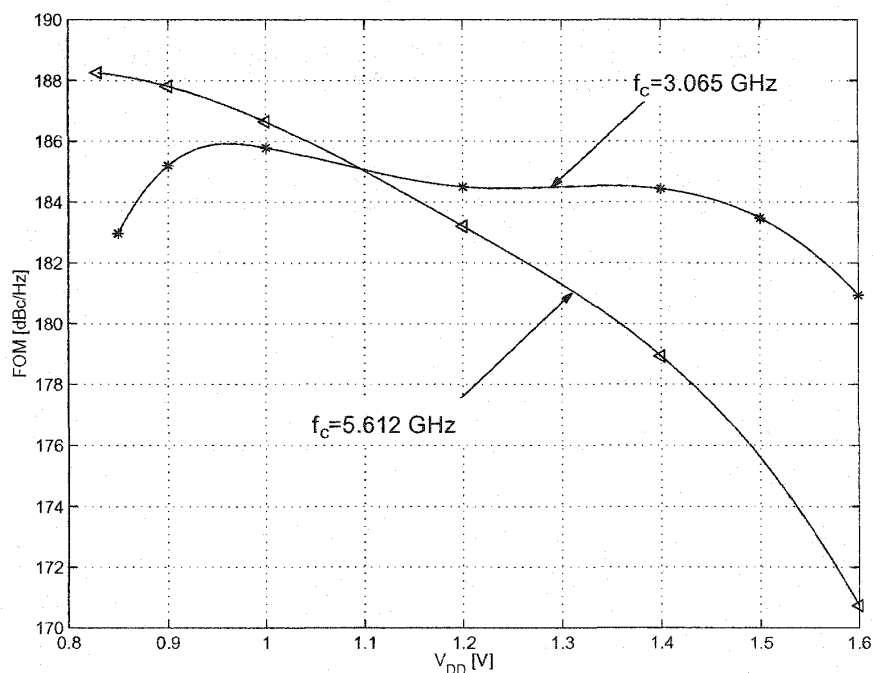


Figure 4.25 FOM vs. V_{DD} of band-switching VCO

Finally, 1 V V_{DD} has the phase noise and FOM near the optimal for both frequencies (3.065 GHz and 5.612 GHz), and is used for comparison with some recently published VCOs listed in Table 4.2.

Table 4.2: Comparison with recently published VCOs

Ref.	f_c [GHz]	$\mathcal{L}\{1\text{MHz}\}$ [dBc/Hz]	V_{DD} [V]	Tuning Range	P_{dc} [mW]	Technology
[Sam01]	4.20	-114	2.5	18%	13.8	CMOS
	5.05	$f_c = 5\text{ GHz}$		(2.5 V)		
[Sve00]	1.80	-125	2.0	26.5%	2.0	CMOS
	2.45	$f_c = 1.9\text{ GHz}$		(4.0 V)		
[Kuc01]	1.75	-134	2.7	35.7%	12.2	SiGe
	2.51	$f_c = 2.05\text{ GHz}$		(2.7 V)		BiCMOS
[Vaa01]	3.3	-120	2.5	46.5%	36.5	BiCMOS
	5.3	$f_c = 4.4\text{ GHz}$		(2.7 V)		
This work	3.065	-120.8	1.0	58.7%	3.0	SOI
[Fon02a]	5.612	-114.6		(1.4 V)	2.0	CMOS

4.6.4 SOI vs. Bulk in Band-switching VCO

Besides the higher speed performance of the SOI transistor as compared to its bulk counterpart, SOI offers several advantages over bulk in band-switching topology. First, the reduced parasitic allows SOI AMOS to have better C_{max}/C_{min} , resulting in better tuning range. Second, the nominal v_{tune} , the voltage that gives a capacitance in the middle of C_{max} and C_{min} , is closer to zero as compared to bulk. Having the nominal v_{tune} reduces the required tuning voltage to cover the full range. For example, in this particular technology, nominal v_{tune} is -0.1 V , and 1.4 V is mandatory to switch the varactor. If v_{tune} is at zero, 1.2 V may be enough to switch the AMOS varactor completely. As for bulk technology, [Sve00] gives a worse nominal v_{tune} between -3 to 1 V , and C_{max}/C_{min} is lower. Therefore, a tuning voltage much higher than V_{DD} is

required to achieve the wideband tuning, and making bulk technology unfavorable for band-switching topology

4.6.5 Summary

This section has dealt with the design and testing of a 3.0-5.6 GHz band-switching VCO. The VCO features a high- Q horseshoe inductor (Chapter 3) and an array of band-switching varactors, occupying a total area of $650\text{ }\mu\text{m}$ by $460\text{ }\mu\text{m}$ excluding the pads as shown in the micrograph Figure 4.26. The use of an AMOS band-switching varactor bank for phase noise improvement was discussed. Furthermore, the superiority of SOI in terms of low parasitics compared to bulk is demonstrated by the wide tuning range and the sub-1V, sub-mW operation.

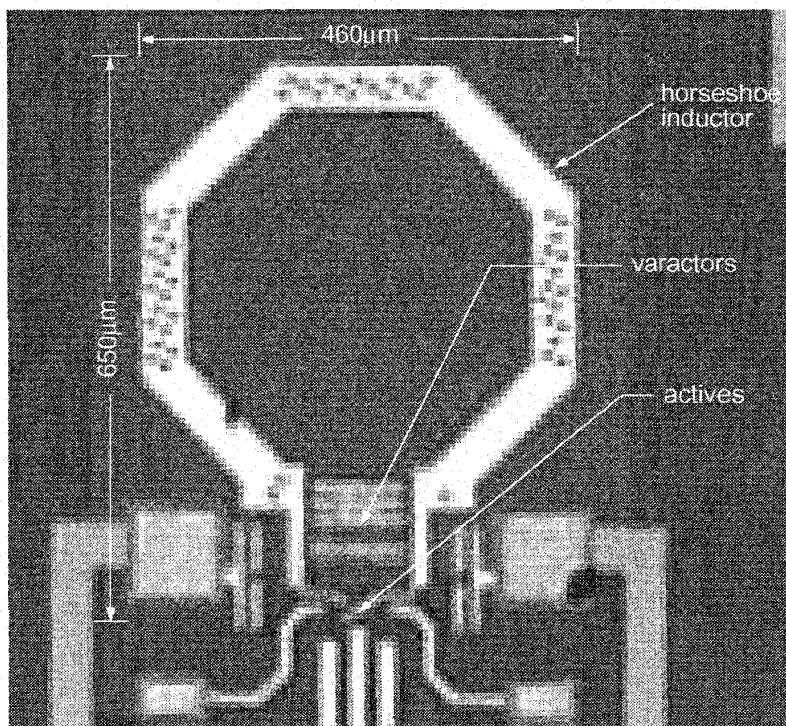


Figure 4.26 Micrograph of band-switching/differentially-tuned VCO

4.7 Differentially-Tuned VCO

Band-switching is a direct but cumbersome way to resolve the problem of excessive phase noise introduced by high k_V . Extra control circuitry is required to control the switching varactor, and the high C_{max}/C_{min} property of the AMOS varactor is hindered. In this section, a simple theory is introduced to explain how varactors up-convert low-frequency common-mode noise, such as flicker noise, near the carrier. Then, a technique known as differential tuning [Fon02b] is used to fully utilize the wide tuning capability of an AMOS varactor while the up-converted noise due to high k_V is suppressed. Finally, the theory is verified by measurement.

4.7.1 Low-Frequency Noise Upconversion

One mechanism for upconversion of low-frequency noise, such as flicker noise, is the non-linearity of the circuit [Haj99]. However, the low-frequency noise can also modulate the varactor directly and this is seen as jitter near the carrier. Consider a complementary LC-VCO as shown in Figure 4.27.

The resonator consists of the inductor L and the capacitor C , which consists of C_1^+ , C_1^- , C_2^+ and C_2^- . Consider v_n^+ and v_n^- as the total noise from the transistors at each side as shown in Figure 4.27. At low frequencies, the inductor L behaves like a short-circuit, so

$$v_n^+ = v_n^- \quad (4.45)$$

Therefore, all the noise power at low frequencies can be considered as common-mode noise, defined as v_{ncm} . One mechanism for low-frequency noise upconversion is that v_{ncm} is injected into the varactor through the nodes v_o^+ and v_o^- . This noise is subsequently upconverted to the carrier frequency by the resonator as described in (4.32)

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (4.46)$$

$$C = C_0 + k_V(v_{tune} + v_{ncm}) \quad (4.47)$$
[illegible]

Figure 4.27 Schematic of differentially-tuned VCO

4.7.2 Single-ended vs. Differentially Tuning

In this section, common-mode noise rejection in the differentially-tuned varactor is analyzed. The effect of common-mode noise in single-ended tuned varactors is first analyzed starting from the varactor topology given in Figure 4.28a.

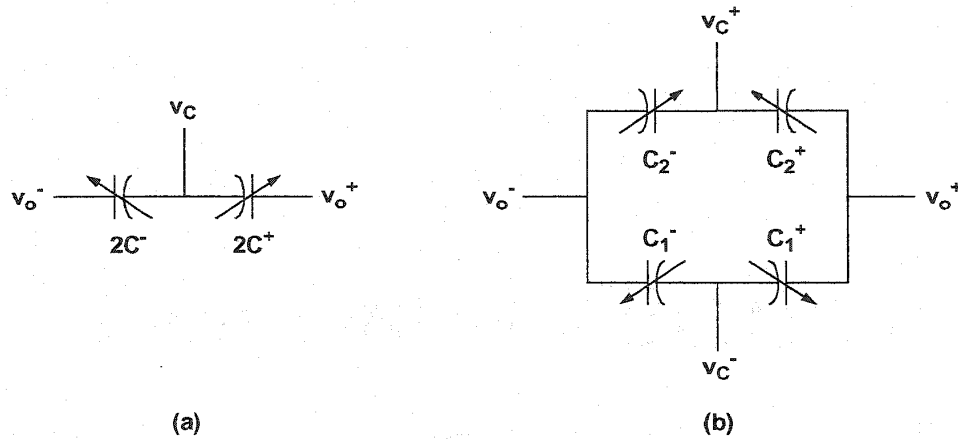


Figure 4.28 (a) Single-ended and (b) differentially-tuned varactor

To demonstrate common-mode noise rejection, the equivalent capacitance C between v_C and v_o^+ is calculated. From (4.47), it is given by

$$C = 2C^+ = 2C_0 + 2k_F(v_C + v_{ncm}) \quad (4.48)$$

Hence, the common-mode noise modulates the varactor, which will result in jitter and phase noise. If the varactor is differentially-tuned as shown in Figure 4.28b, then the capacitances are given by v_C^+ , v_C^- and v_o^+ such that

$$C_1^+ = C_0 + k_F(v_C^+ + v_{ncm}) \quad (4.49)$$

$$C_2^+ = C_0 - k_F(v_C^- + v_{ncm}) \quad (4.50)$$

Since $C = C_1^+ + C_1^-$, if the varactor is perfectly symmetrical such that $k_{V1} = -k_{V2}$, the expression for C is

$$C = 2C_0 + 2k_V v_C \quad (4.51)$$

where $v_C = v_C^+ - v_C^-$. If $|k_{V1}|$ and $|k_{V2}|$ are not the same, the gain of the common-mode noise is reduced to $|k_{V1} - k_{V2}|$. Therefore, it has been shown that differential tuning can be used to reject common-mode noise, such as flicker noise and shot noise.

4.7.3 VCO Implementation

The VCO implementation is basically the same as the band-switching VCO as described in Section 4.6, except that differentially-tuned varactors were used instead of band-switching varactors. As shown in Figure 4.28, the VCO is an LC cross-coupled differential circuit with both PMOS and NMOS latches which generate negative resistance to cancel losses in the LC resonator. The monolithic inductor is the 0.85 nH horseshoe-shaped single loop with Q above 20 at frequencies between 3.8 and 5.7 GHz described in Figure 3.12. The AMOS varactors are differentially tuned for common-mode noise rejection. Bias-T source followers, as are described in Section 4.9, are used as the output buffers.

4.7.4 Experimental Result

The VCO was measured using wafer probing together with a 26.5 GHz HP8563 spectrum analyzer with a phase noise module. The frequency vs. varactor tuning voltage at 1V V_{DD} is shown in Figure 4.29. The differential tuning voltage v_{dtune} is related to v_C^+ and v_C^- by

$$v_C^{+/-} = (V_{DD}/2) \pm v_{dtune} \quad (4.52)$$

For example, if $v_{dtune} = 0$ V, then $v_C^+ = 0.5$ V and $v_C^- = 0.5$ V. If $v_{dtune} = -0.5$ V, then $v_C^+ = 0$ V and $v_C^- = 1$ V. For a tuning voltage between 0 and 1 V, the carrier frequency can be tuned from 3.812 GHz to 5.716 GHz, achieving a 40% tuning range. This wide tuning range is

made possible by the high C_{max}/C_{min} ratio of the AMOS varactor. Note that while band-switching requires ± 0.7 V, this only requires ± 0.5 V, making it a true 1 V oscillator.

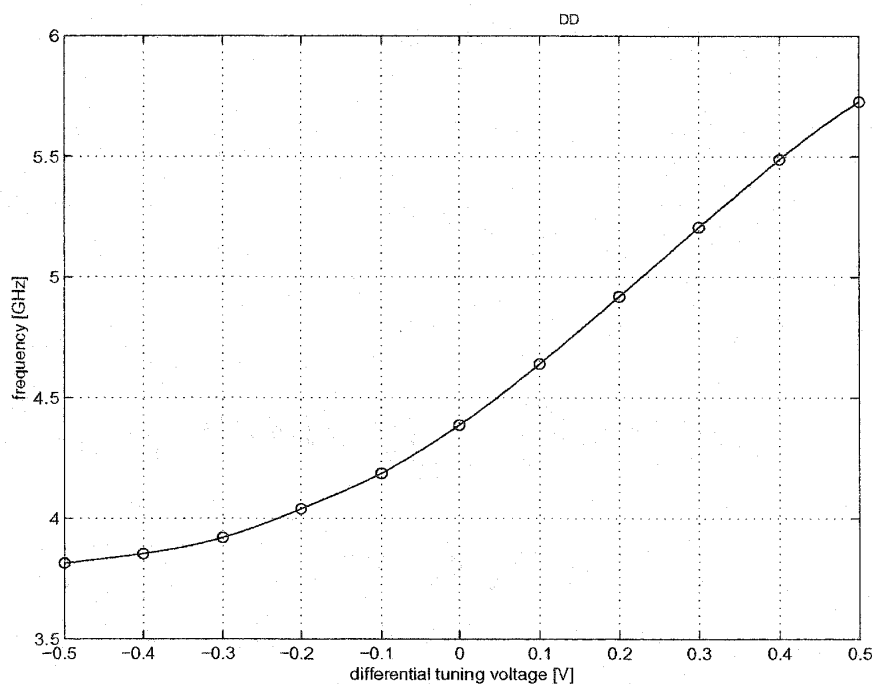


Figure 4.29 Frequency vs. tuning voltage at 1 V V_{DD} of differentially-tuned VCO

Next, the common-mode rejection of the varactor was measured. At 1 V V_{DD} , a common-mode voltage was applied such that $v_C^+ = v_C^-$, and the result is summarized in Table 4.3.

Table 4.3: Common-mode performance measurement

$v_C^+ = v_C^-$	f_c	phase noise @ 1 MHz
0.0 V	4.492 GHz	-117.00 dBc/Hz
0.5 V	4.401 GHz	-117.83 dBc/Hz
0.6 V	4.404 GHz	-118.33 dBc/Hz
1.0 V	4.475 GHz	-118.50 dBc/Hz

The frequency variation is within 2%, while the phase noise variation is within ± 1 dB. Therefore, it is concluded that the varactors are highly symmetrical, which should result in good common-mode noise rejection.

A figure of merit is introduced to provide a numerical standard for the performance of common-mode rejection. In analog circuit design, common-mode rejection ratio (CMRR) [Joh97] is defined as

$$CMRR = A_d/A_c \quad (4.53)$$

where A_d is the differential gain, and A_c is the common mode gain. A_d is similar to k_V , which can be extracted from the frequency-voltage curve shown in Figure 4.29. Meanwhile, A_c is estimated from the frequency deviation from the common-mode measurement, defined as

$$k_{Vc} = \frac{\text{maximum change in } f_c}{\text{change in } v_C} \quad (4.54)$$

In this design, $\max(\Delta f_c)$ is $4.492 - 4.401 = 0.091$ GHz, and Δv_C is $1 - 0.5 = 0.5$ V, therefore the common-mode varactor gain is 0.182 GHz/V. Hence, the common-mode rejection ratio is

$$CMRR = 20 \cdot \log(k_V/k_{Vc}) \quad (4.55)$$

which gives 20 dB. Thus, the upconversion noise is expected to be suppressed by 20 dB.

With CMRR defined, the phase noise was measured at several different frequencies across the wide tuning range. At 1 V V_{DD} , the best phase noise is -121.67 dBc/Hz at 1 MHz offset, measured at the lower frequency bound (3.812 GHz at $v_{dtune} = -0.5$ V) where the VCO gain is minimal and the inductor Q is near its peak. At the middle of the range (4.4 GHz at $v_{dtune} = 0$), k_V is high and the phase noise is -117.83 dBc/Hz at 1 MHz offset. At the upper end of the tuning range (5.716 GHz at $v_{dtune} = 0.5$ V), the phase noise is -111.67 dBc/Hz at 1 MHz offset. The phase noise was also measured for V_{DD} between 0.75 V and 1.4 V, and the results are summarized in Figure 4.30.

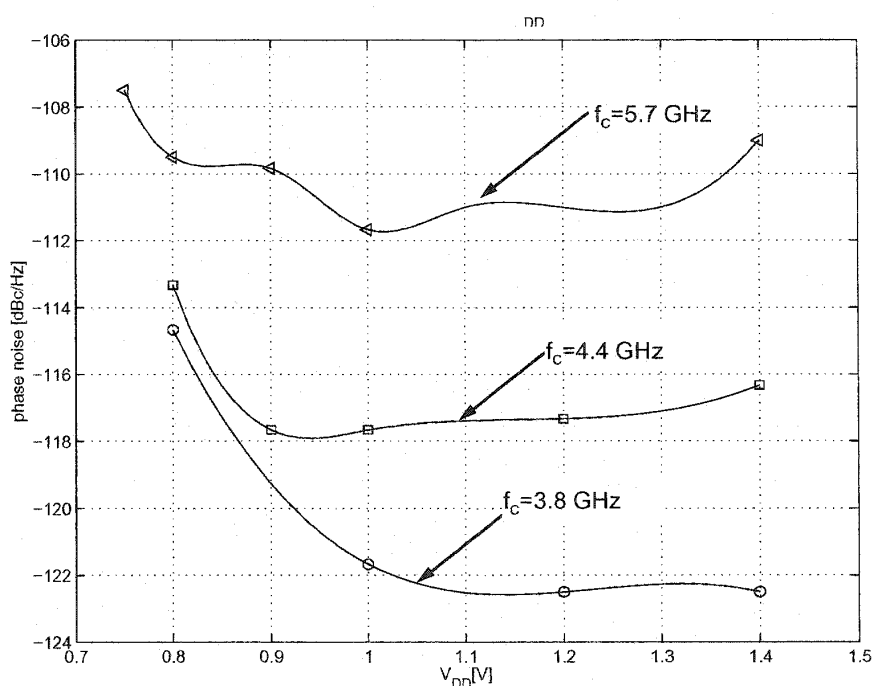


Figure 4.30 Phase noise vs. V_{DD} differentially-tuned VCO

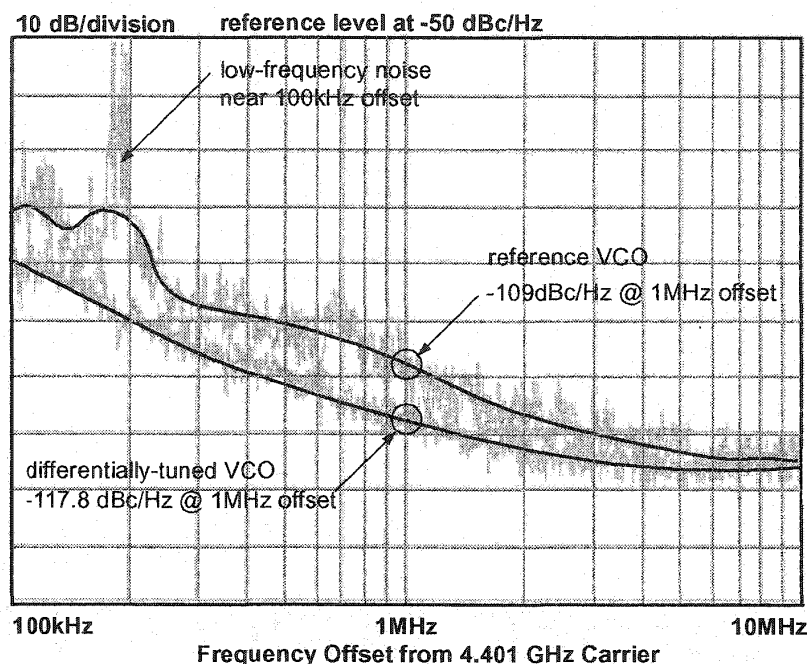


Figure 4.31 Phase noise comparison at 4.4 GHz

To evaluate the phase noise improvement over a conventional single-ended tuning scheme, a reference VCO with varactor topology as shown in Figure 4.28a was fabricated and measured. At 4.4 GHz, with both VCOs operating in the high k_V region (middle of the tuning range), the phase noise was measured and compared as shown in Figure 4.31. At 1 MHz offset, the differential-tuning topology improves the phase noise by about 9 dB. Due to common-mode rejection, the upconverted low-frequency noise near the 100 kHz offset is filtered out, offering a cleaner frequency spectrum. The differentially-tuned VCO can be operated at $0.75 V_{DD}$, drawing only 0.8 mW at 5.5 GHz. Meanwhile, the reference VCO can only operate down to 0.83 V, drawing about 1 mW at that frequency.

The DC power dissipation is plotted in Figure 4.32, and FOM is plotted in Figure 4.33. The lowest power dissipation is achieved at 0.75 V V_{DD} , where only 0.8 mW of power is drawn at 5.5 GHz. To the author's knowledge, this VCO has the lowest power dissipation compared to any published CMOS VCOs at this frequency. Meanwhile, the best FOM is -189 dBc/Hz at 1 V V_{DD} .

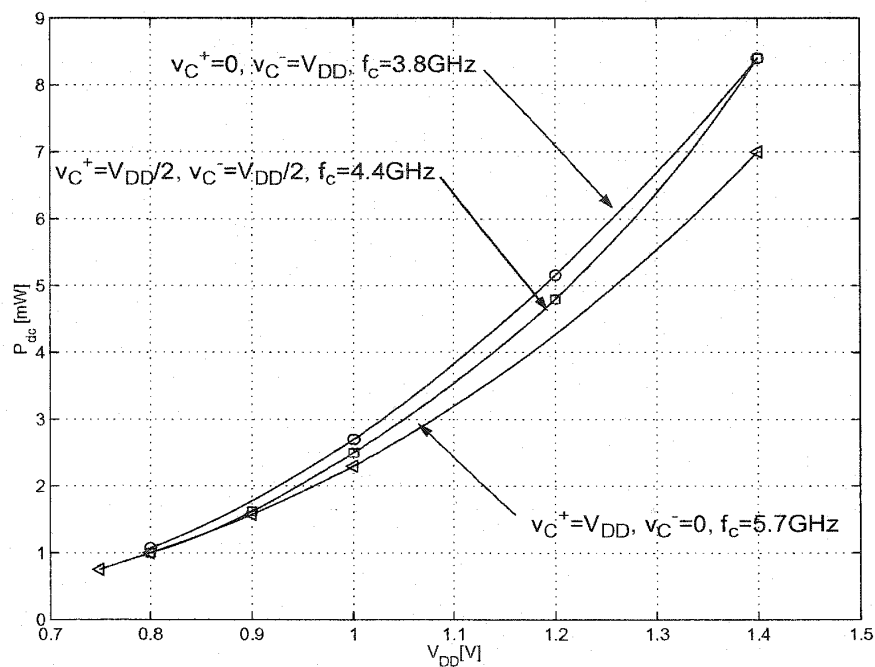


Figure 4.32 DC power dissipation of differentially-tuned VCO

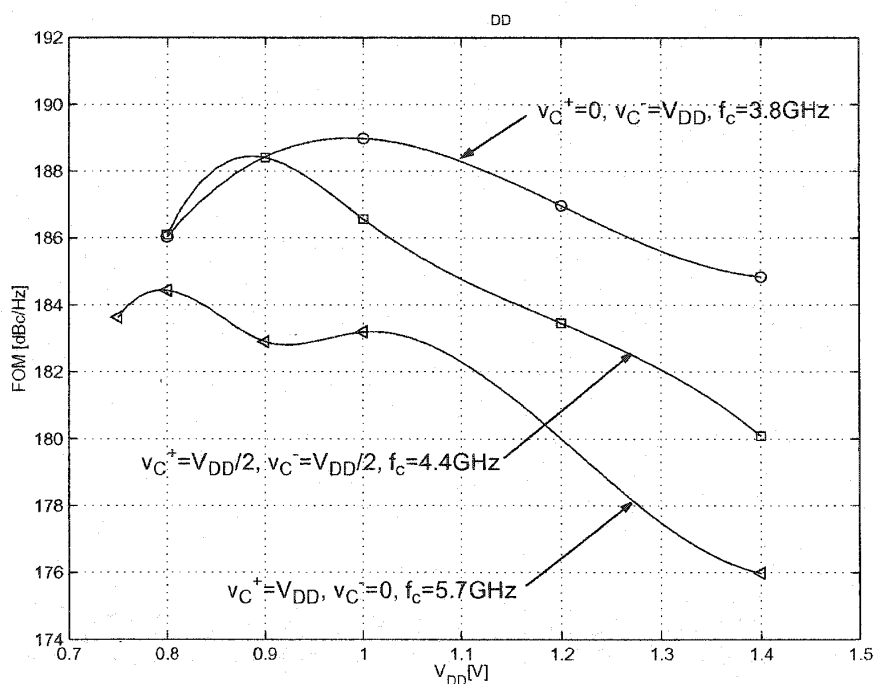


Figure 4.33 FOM measurement of differentially-tuned VCO

4.7.5 Summary

In this section, a 1 V 3.8-5.7 GHz differentially-tuned complementary LC-VCO with 40% tuning range was designed and measured. The VCO has demonstrated that differentially-tuned varactors can provide wide tuning range and reject common-mode noise. At 1 MHz offset, the nominal phase noise (4.4 GHz at $v_{dtune} = 0$) is -117.83 dBc/Hz, and the FOM is 187 dBc/Hz. The power consumption is between 2.3-2.7 mW, and the buffered output power is -9 dBm. If the VCO is operated at 0.75 V V_{DD} , the circuit only draws 0.8 mW of power, the lowest power dissipation compared to any published CMOS VCO. The VCO occupies a total area of 650 μm by 460 μm excluding the pads, as shown in the micrograph Figure 4.26.

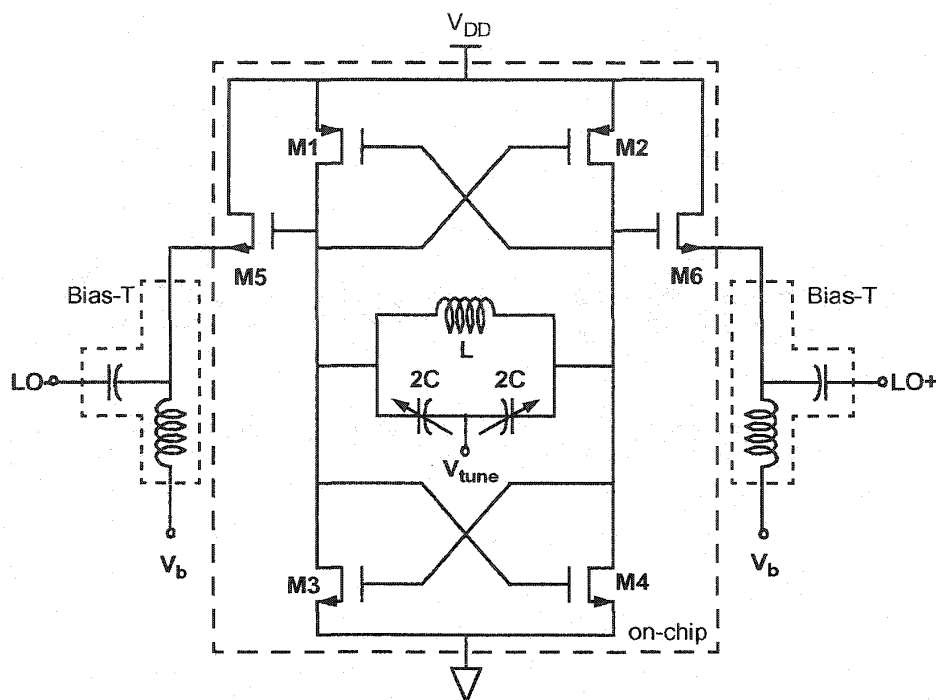
4.8 Low-Voltage High-Speed Design

Modern submicron CMOS technology offers devices with comparable speed performance to SiGe HBT technologies, and very high speed components such as a 50 GHz VCO have been demonstrated in bulk technology [Wan01][Tie02]. However, the inductors employed in these designs are gigantic compared to the varactors, and the parasitics associated with the devices are large. Therefore, despite a reasonable phase noise, the frequency tuning is limited to less than 2%, making the VCO unsuitable for manufacturing. Nevertheless, these circuits demonstrate the speed capability of submicron transistors.

In this section, the design and implementation of a 40 GHz VCO [Fon02c] is described to demonstrate the high-speed low-voltage low-power application of SOI transistors. While the high-speed of submicron SOI is able to deliver enough gain at high frequency, the reduced parasitics for the actives and high C_{max}/C_{min} ratio of AMOS varactors promises a wider range of frequency tunability. Through careful design considerations as described in the following section, the measured results show a frequency tuning range of 9 to 15% from a 1.5 to 2 V V_{DD} with good phase noise performances. This is the first CMOS VCO that achieves adequate tuning range at this frequency. Furthermore, a complementary topology was used in the design, demonstrating the feasibility of PMOS operation at this frequency. With the PMOS latch available, the low-voltage phase noise optimization technique as described in [Haj99] can be used to increase the performance of the VCO.

4.8.1 VCO Design

The schematic of the LC cross-coupled differential VCO is shown in Figure 4.34. As described in Chapter 2, this SOI technology offers an NMOS device with f_T and f_{MAX} of 148 GHz and 162 GHz respectively, and a PMOS device with f_T and f_{MAX} of 68 GHz and 102 GHz respectively. Therefore, both PMOS and NMOS latches were used to generate the negative resistance. The resonator consists of (a) a single-loop inductor that is estimated to be 60 pH using EM simulation [IE3D], and (b) AMOS varactors which have a nominal capacitance of 0.4 pF. The



outputs are buffered using bias-T source-followers (M5, M6) for measurement purposes (see Section 4.9).

Figure 4.34 Schematic of a 40 GHz complementary VCO

At frequencies as high as 40 GHz, only small L and C are required in the resonator. As C becomes smaller, the parasitics from the transistors and the inductor dominate the total capacitance and thus limit the frequency tuning. Mathematically, varactor tuning is governed by

$$\text{Tuning} = \frac{C_{V, \max} + C_{\text{fix}}}{C_{V, \min} + C_{\text{fix}}} \quad (4.56)$$

where C_V is the varactor capacitance, and C_{fix} is the fixed capacitance from the parasitics. Therefore, a large varactor with a high $C_{\max}/C_{\min}$ ratio is required to overcome the fixed capacitance.

AMOS varactors as described in Section 4.5.1 were used because they have a good C_{max}/C_{min} ratio of 5 at 1 GHz as shown in Figure 4.15. For the varactor in this technology, a tuning voltage v_{tune} of ± 1 V is required to cover the full tuning range. The varactor has the Q peak at the most negative v_{tune} (inversion mode of operation), and decreases by about 45% as v_{tune} approaches the middle of the tuning range (depletion mode of operation). Q then rises by about 30% as v_{tune} approaches +1 V (accumulation mode of operation). As the frequency is increased to 40 GHz, Q scales down proportionally with increasing frequency but C_{max}/C_{min} remains the same. This is verified by numerical simulation using MEDICI as described in Section 3.2. Therefore, a relatively large AMOS varactor (0.4 pF) was used to provide wide enough tuning to overcome the fixed capacitances from the transistors and the inductor, and hence the VCO can be tuned to cover anticipated process variations.

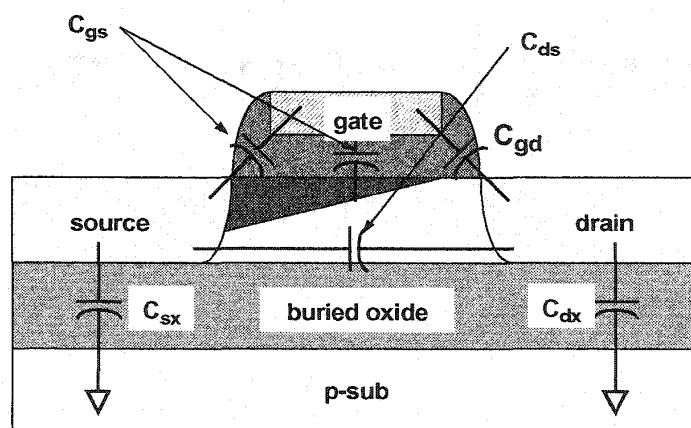


Figure 4.35 Capacitances of SOI transistors

There are three significant fixed capacitances associated with the transistor: the gate capacitance C_{gs} , the overlap capacitance C_{dg} , and the parasitic drain capacitance $C_{ds} + C_{dx}$ as shown in Figure 4.35. C_{sx} is eliminated because the source of the transistor is grounded owing to the circuit topology, and C_{gx} (capacitance from gate to p-sub) is negligible. The SOI transistors

(M1 to M4) were simulated in the saturation region, and the contribution of each parasitic is summed and listed in Table 4.4.

Table 4.4: Total fixed capacitance of SOI transistors

	Capacitance [fF]	Percentage [%]
C_{gs}	15.4	53
C_{dg}	9.1	31
$C_{dx}+C_{ds}$	4.5	16

For a given process lithography, SOI and bulk have approximately the same C_{gs} and C_{dg} . However, in SOI, both C_{dx} and C_{ds} are reduced, resulting in about 30% smaller parasitics compared to its bulk counterpart. Such a reduction is significant because of the small varactor capacitance at high frequency.

As for the inductor L , the parasitic capacitance is proportional to the area of the passive. Therefore, the smaller the inductor, the lower the parasitic. Hence, the inductor is relatively small compared to the varactor. Furthermore, the effect of skin-depth at 40 GHz is significant. Therefore, only the top-level metal was used instead of metal stacking to form the inductor to reduce substrate loss and improve Q . Since large varactors and a small inductor were used in the design, the active area is only 100 μm by 100 μm (see micrograph in Figure 4.40).

4.8.2 Measurement

The VCO was measured using wafer probing with a 40 GHz Rhode & Schwarz spectrum analyzer. The total loss from the wiring cables and the bias-T was measured to be 6 dB at 40 GHz.

The frequency of oscillation and output power versus varactor tuning voltage is shown in Figure 4.36. The tuning voltage of the varactor v_C and the VCO v_{tune} is related by

$$v_{tune} = V_{DD}/2 + v_C \quad (4.57)$$

The tuning range is 9% (from 37.1 to 40.6 GHz) with a V_{DD} of 1.5 V and 15.2% (from 34.6 to 40.3 GHz) with a V_{DD} of 2 V. Because ± 1 V is required for the full tuning of the varactor, v_{tune} may exceed V_{DD} . The output power decreases as the frequency of oscillation approaches the lower frequency limit, and the VCO shuts down for v_{tune} less than 0.9 V. This is because (a) the inductor has higher Q at higher frequencies, and (b) the Q of the AMOS varactor drops significantly as v_{tune} decreases from V_{DD} to $V_{DD}/2$ (or V_C decreases from -1 to 0) as shown in the AMOS Q-V curves (Figure 4.15).

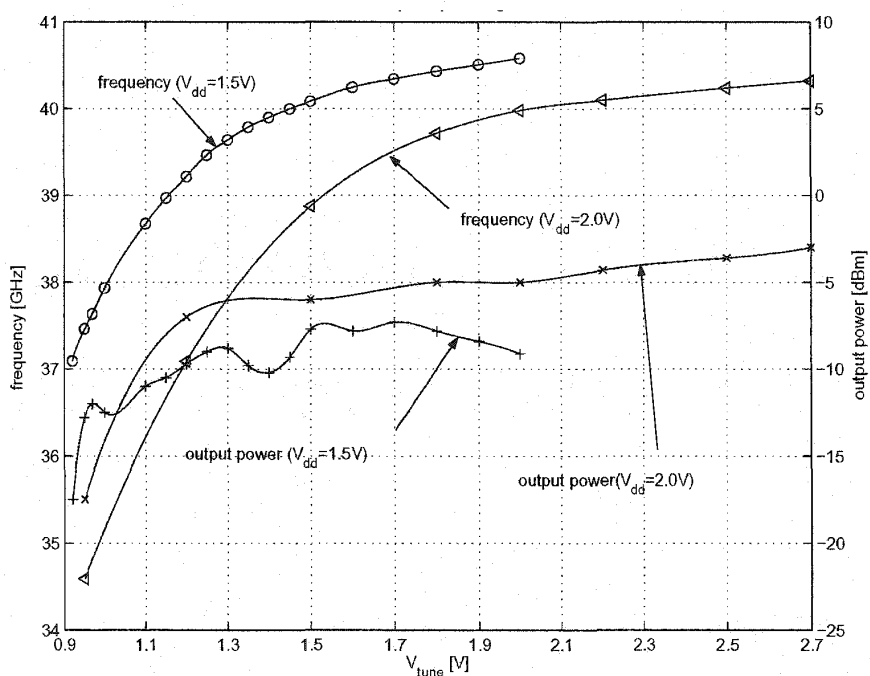


Figure 4.36 Frequency and output power vs. tuning voltage

The VCO can only oscillate when the varactor is operating in the high- Q inversion region. Therefore, the tuning range of the VCO is limited by the Q of the passives. One way to compensate for the problem is to increase V_{DD} . For example, given that v_{tune} has to be greater than 0.9 V for the VCO to operate, increasing V_{DD} from 1.5 V to 2 V increases v_C by 0.25 V.

Hence, the varactor can be tuned to provide larger capacitance, allowing the VCO to have a wider tuning range toward lower frequencies.

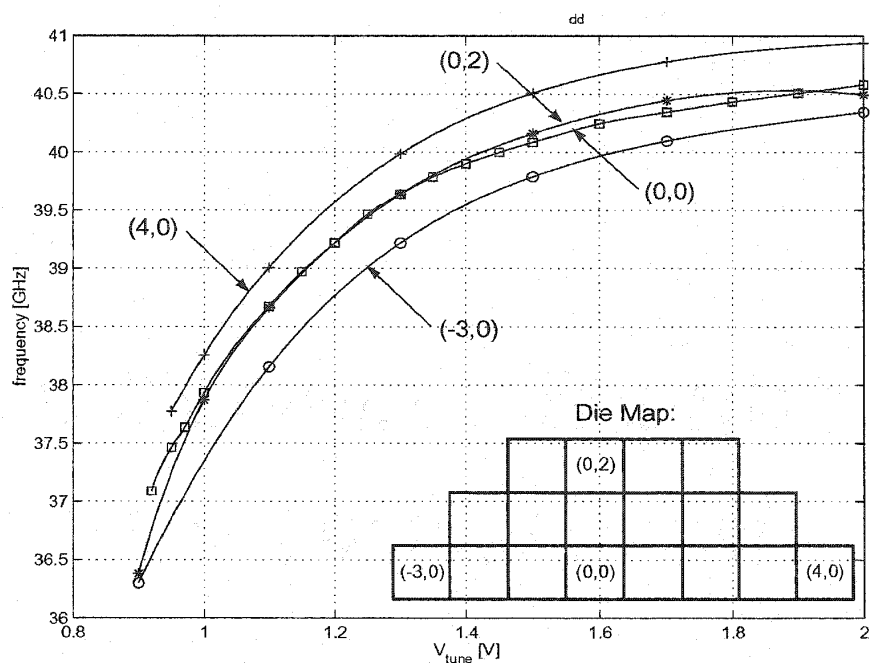


Figure 4.37 Frequency-voltage variation across the wafer at 1.5 V V_{DD}

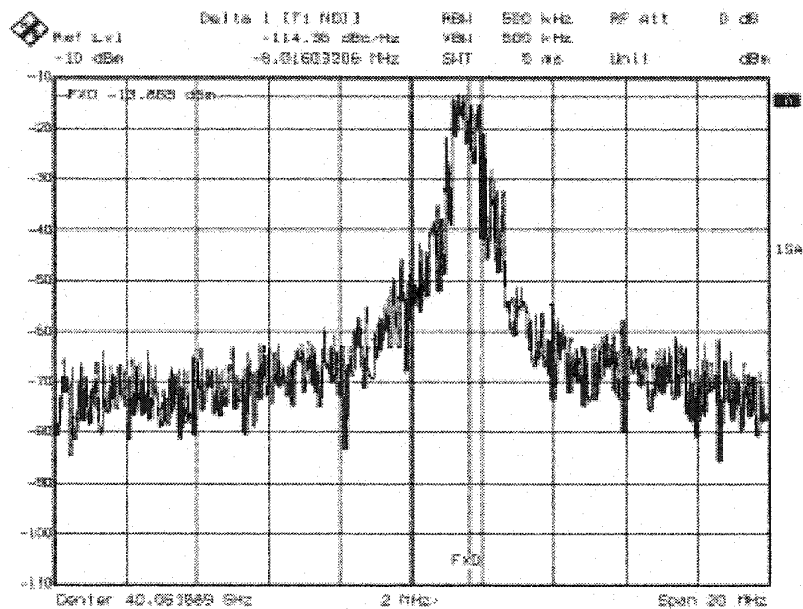


Figure 4.38 Output spectrum of the 40 GHz carrier at 1.5 V V_{DD}

Figure 4.37 gives the frequency versus tuning voltage curves of four VCOs across an 8-inch wafer to provide some information about process variation. The frequency variation is less than 2% across the wafer. With a frequency tuning range of 9% or more, the feasibility of the VCO in this SOI technology for commercial production is partially demonstrated.

Figure 4.38 is the output spectrum of the VCO at 40.062 GHz, 1.5 V V_{DD} . The output power is -7.9 dBm after accounting for the 6 dB cable losses. The phase noise at 40 GHz for several offsets from the carrier was measured as shown in Table 4.5. Due to apparatus limitations, the phase noise at 1 MHz offset is pessimistic due to noise jitter around the carrier, while at 8 MHz offset the phase noise is limited by the noise floor of the equipment.

Table 4.5: Phase noise at 40 GHz carrier ($V_{DD} = 1.5$ V)

Frequency Offset f_{off}	Phase Noise $\mathcal{L}\{f_{off}\}$
1 MHz	-90.03 dBc/Hz
4 MHz	-109.73 dBc/Hz
8 MHz	-114.36 dBc/Hz

Figure 4.39 compares the performance of the VCO reported here with other recently published VCOs. The FOM is calculated using the measurement at 1.5 V V_{DD} with the phase noise at 4 MHz offset from the 40 GHz carrier. The VCO core draws 7.5 mA from the supply, and the power dissipation is 11.25 mW.

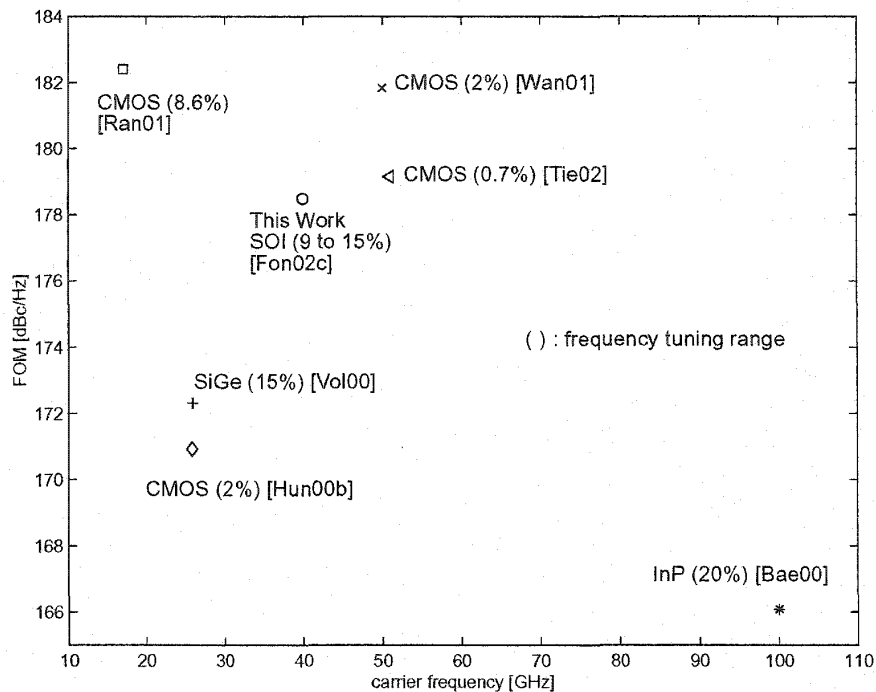


Figure 4.39 Performance comparison with recently published VCOs

For VCOs implemented in bulk silicon technologies, the parasitics are usually high and the tuning range is limited to about or less than 2% [Hun00b][Wan01][Tie02] at high frequency. Hence, for manufacturability, it is very important to have a technology that offers a low parasitic capacitance as in SOI.

For VCOs implemented in HBT technologies using SiGe [Vol00] and InP [Bae00], despite the better phase noise and tuning range, the V_{DD} and power dissipation are high (5V, 50mW for [Vol00] and 6V, 78mW for [Bae00]). Therefore, they cannot be operated at low voltage such as 1.5 V at this frequency due to device limitations, making them unfavourable for single-chip integration with modern submicron CMOS technology.

Hence, SOI is considered to be a better technology option for implementing components for low-voltage high-frequency applications, especially if single-chip integration is desired.

4.8.3 Summary

In this section, we have designed and measured a complementary LC cross-coupled VCO working up to 40 GHz in a 0.13 μm SOI CMOS technology. This is the first working LC type VCO that used both PMOS and NMOS cross-coupled inverters reported at this frequency. The power dissipation is only 11.25 mW in the core, and the measured phase noise is -109 dBc at 4 MHz offset from the 40 GHz carrier. The tuning range, which is 9 to 15% depending on V_{DD} , can compensate for process variations, thus demonstrating the feasibility of low-cost commercial applications at millimeter wavelengths.

The VCO occupies an area of only 100 μm by 100 μm as shown in Figure 4.40 (excluding pads). This is the smallest active area compared to other LC type VCOs, and therefore it is a good candidate for multi-PLLs integrated on a single chip.

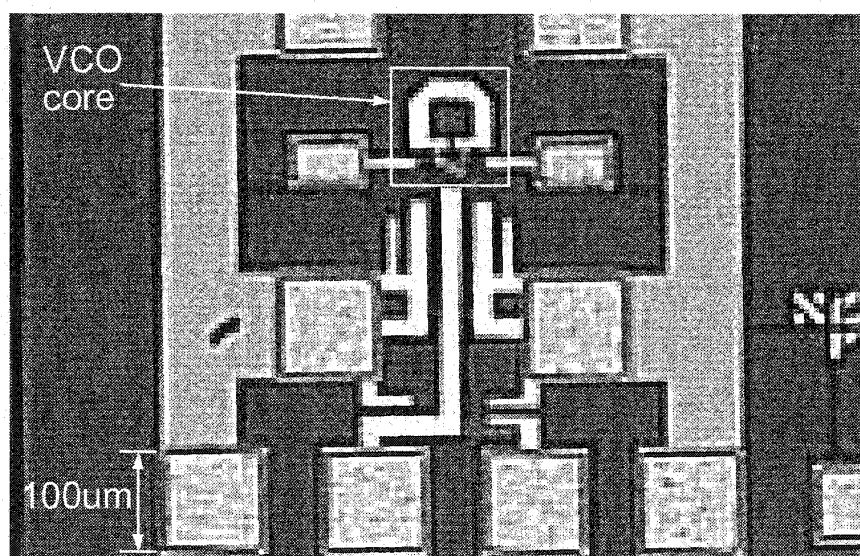


Figure 4.40 Micrograph of 40 GHz VCO

4.9 Bias-T Source Follower

In this section, a bias-T source follower as a buffer for measurement is described. This type of buffer can only be implemented in SOI technology, and it provides significant advantage over bulk CMOS in terms of accuracy for measuring low-voltage and high-speed circuits.

Consider a 1 V complementary VCO as shown in Figure 4.41a. The dc voltage at the output v_o is at $V_{DD}/2$, which is 0.5 V. Figure 4.41b is the schematic of a conventional source follower. Transistor $M6$ is a current source, and the dc level of v_{buf} is equal to v_{on} for $M6$ to operate in the saturation region. Then, when v_{on} is 0.2 V, the v_{gs} of $M5$ is 0.3 V. Even for low- V_{th} technology, 0.3 V can barely turn on the device, and hence the current sourcing capability is poor. A large transistor is therefore required to generate enough current at low v_{gs} , and the parasitics associated with the transistor slow down the VCO.

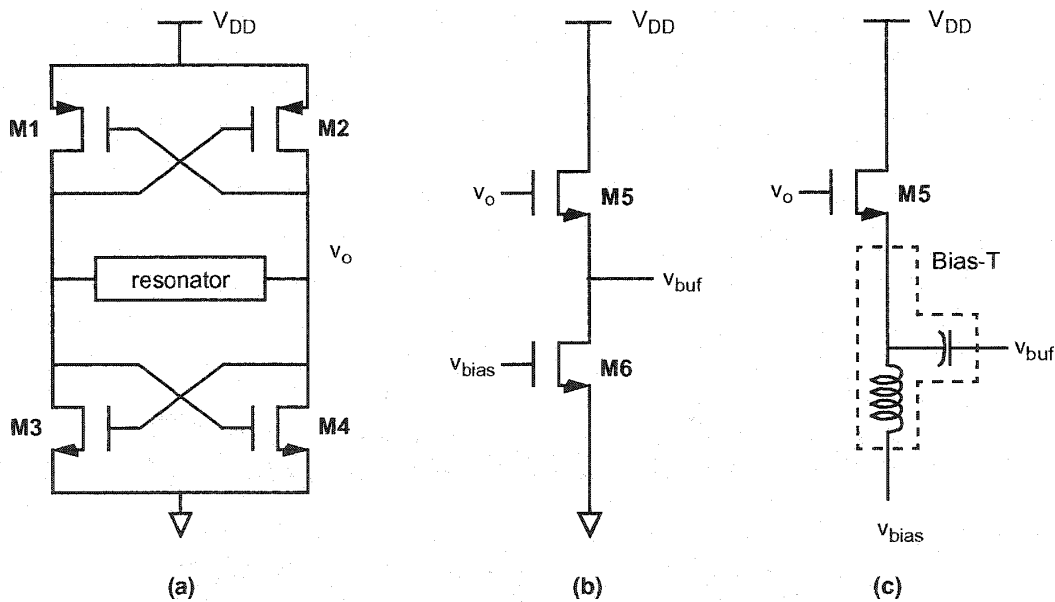


Figure 4.41 Schematics of (a) complementary VCO, (b) NMOS source follower and (c) bias-T source follower

For example, from simulation, for a $0.13\text{ }\mu\text{m}$ gate length and 0.3 V v_{gs} , the current per unit width is $35\text{ }\mu\text{A}/\mu\text{m}$. Assume the buffer is to deliver 1 dBm to a $50\text{ }\Omega$ output, then the required current is approximately 4.5 mA . Therefore, the transistor width is $128\text{ }\mu\text{m}$. For simplicity, only the parasitic at the drain side (C_{ds} and C_{dx}) of $M5$ is considered, which is typically 10% of C_{ox} . Therefore, the total parasitic associated with the 1-dBm buffer is 0.23 pF . Now, consider that the buffer is used for a 40 GHz VCO as in Section 4.8. The varactor is only 0.4 pF , and adding the buffer decreases the speed of the VCO by at least 50%.

Consider the bias-T buffer as shown in Figure 4.41c. The inductor of the bias-T provides high impedance for the ac signal at high-frequency, and a dc short for transistor biasing. If v_b is connected to ground, v_{gs} of $M5$ is 0.5 V , the current density is increased to $175\text{ }\mu\text{A}/\mu\text{m}$, and the parasitic is now 5 times lower. The current density can be further improved by using SOI technology. Unlike bulk CMOS, each individual MOSFET is dc isolated from each other by the buried oxide, v_b can be extended to *negative* voltages. In a nutshell, the advantage of SOI bias-T source followers are that for low voltage operation, (a) a smaller buffer can be used to reduce the load of the circuit, and (b) the voltage attenuation due to the follower can be minimized by providing enough current drive, so that the voltage gain is close to 1. The VCO measurement with different v_b is shown in Figure 4.42 for comparison.

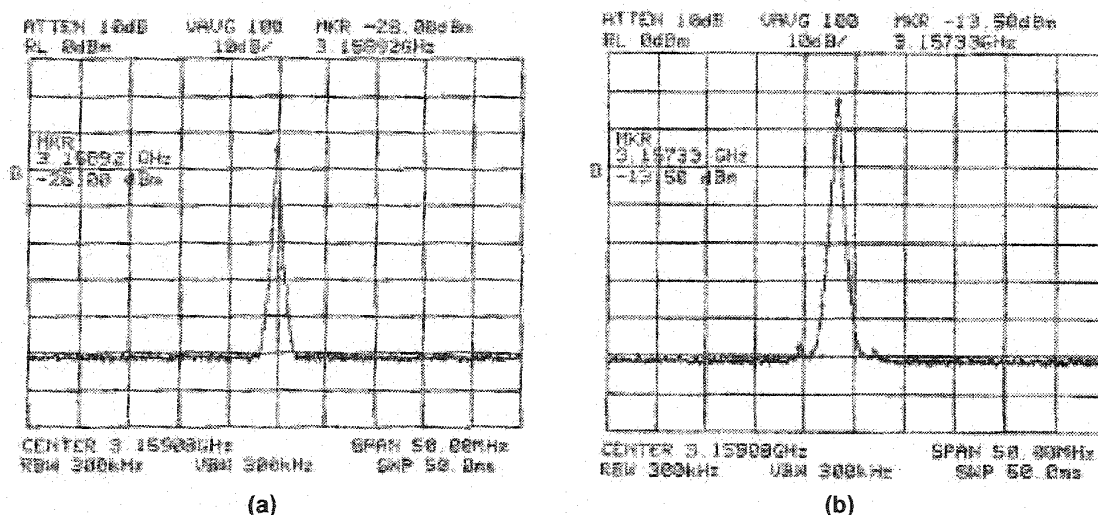


Figure 4.42 VCO output spectrum with bias-T output buffer of v_b at (a) 0 and (b) -0.7 V

4.10 Summary

In this chapter, the basic theory of complementary VCOs was reviewed. A phase noise improvement technique “simultaneous g_m and impedance matching” [Fon02d] was introduced together with experimental results for theory verification. Next, low voltage frequency tuning issues were discussed, and the application of high gain varactors in SOI was described. A frequency tuning range up to 58% was demonstrated using a band-switching topology [Fon02a], and the relationship between varactor gain and phase noise was studied. To reduce the phase noise due to the high gain varactor, differential tuning was employed to reject common-mode noise [Fon02b]. Theory of common-mode noise rejection was developed, and was verified by measurement. Next, the design of a 40 GHz VCO with up to 15% frequency tuning was described. Both PMOS and NMOS latches were used to demonstrate the high speed capability of SOI [Fon02c]. The frequency tuning problem as observed in [Wan01][Tie02] was discussed in detail, and the low parasitics of SOI was utilized to expand the tuning range. Finally, the bias-T source follower was mentioned for accurate high-speed VCO measurement.

Chapter 5 Low Noise Amplifier

5.1 LNA in 5 Minutes

The low noise amplifier (LNA) represents the first stage of the receiver chain, and it has two main purposes: (a) amplifies the signal without introducing excessive noise and (b) serves as an interface with the external $50\ \Omega$ world for maximum power transfer. It therefore allows the receiver to detect weak signals, and provides gain to suppress the noise generated by the later stages. This noise suppression is described by

$$F_{TOT} = F_{ext} + F_{LNA} + \frac{F_{MIX} - 1}{G_{LNA}} + \dots + \frac{F_n - 1}{G_{LNA} G_{MIX} \dots G_{n-1}} \quad (5.1)$$

where F is the noise factor, G is the gain, F_{TOT} represents the noise factor of the total system, F_{ext} is the noise factor of the external off-chip components, the subscript LNA is the low noise amplifier, the subscript MIX is the mixer, and n the stage number, where $n = 1$ for the LNA, and $n = 2$ for the mixer in this example. From (5.1), it is obvious that the purpose of the LNA is to minimize F_{LNA} while maximizing G_{LNA} , which translates directly to low noise figure and high gain. A brief system overview is shown in Figure 5.1.

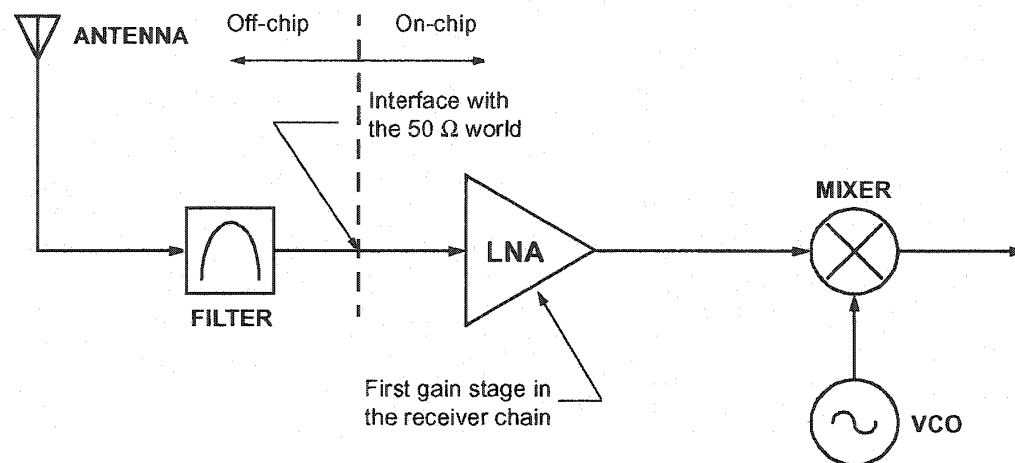


Figure 5.1 LNA in a receiver chain

From the circuit point of view, the figures of merits as shown in Figure 5.2 are used to measure the performance. Gain can be represented in two forms: S_{21} for small-signal voltage gain, and G_p for power gain with source and load impedances taken into account. G_{max} is the maximum achievable power gain, which represents the gain when the circuit is perfectly power matched.

Dynamic range of the circuit is usually limited at the low end by noise and at the top end by non-linearity. Noise is usually measured in terms of noise figure (NF), which is the ratio (in dB) of total output noise to noise from the source. It can also be defined as SNR_{input}/SNR_{output} . NF_{min} is the minimum achievable noise figure under the condition that the source impedance is equal to the optimum impedance. This is often expressed in terms of reflection coefficient, such that NF_{min} is achieved when source reflection Γ_s is equal to the optimum reflection Γ_{opt} . The linearity issue arises from the fact that the transfer function of the transistor is ultimately non-linear. If the signal is too large, distortion occurs and the performance of the circuit degrades. Usually, two figures of merit are used to describe the linearity of the circuit, which are the 1-dB compression point for gain compression, and the third-order intercept point ($IP3$) for intermodulation.

Matching can be categorized into power matching and noise matching. Power matching results in optimum power transfer between two impedances, while noise matching results in minimal noise added to the system. The general characteristic curves for the figures of merit are given in Section 5.4.

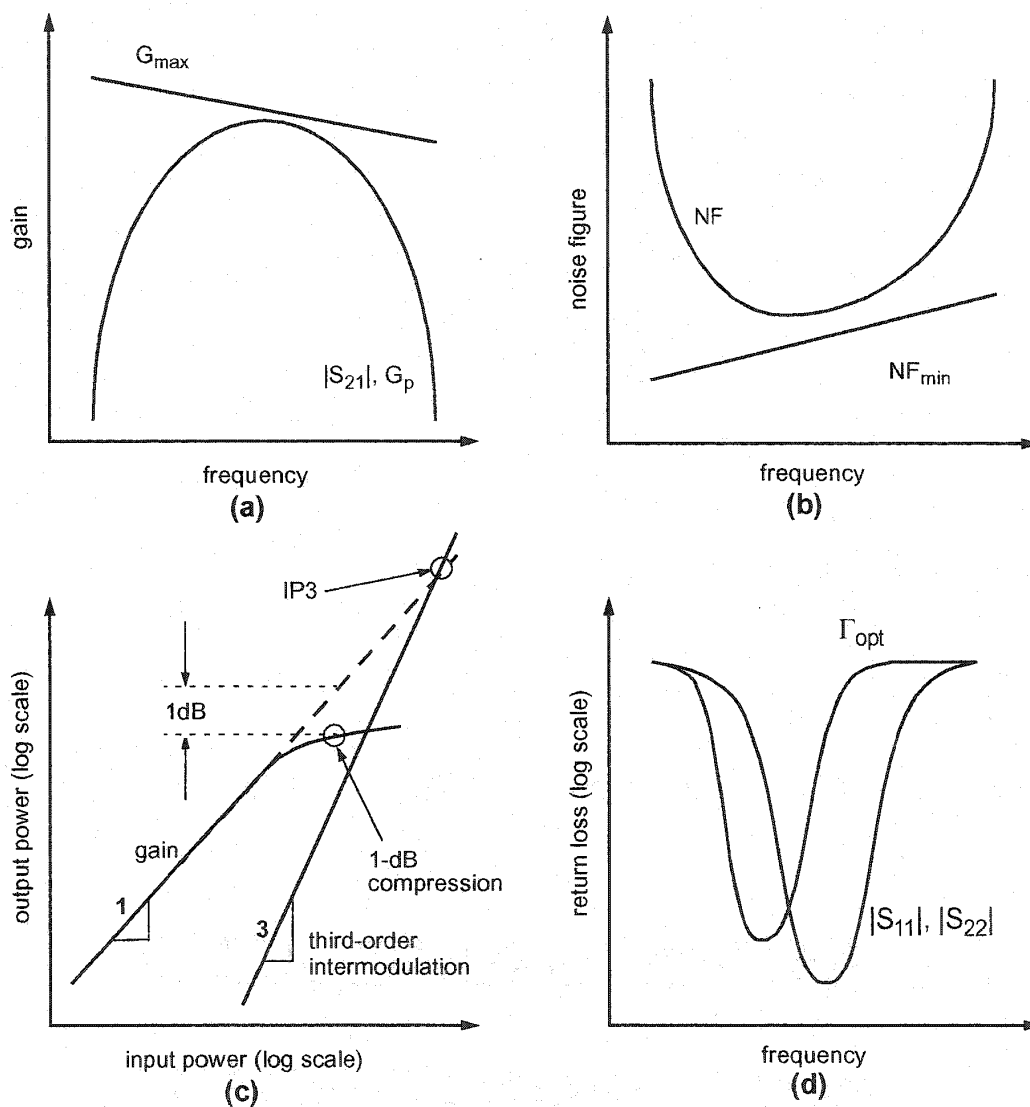


Figure 5.2 Figures of merit of LNA: (a) gain, (b) noise figure, (c) linearity and (d) noise and power matching

5.2 LNA topology

There are two choices considered for the LNA topology: a cascode configuration, or a cascade configuration (Figure 5.3). The cascoded LNA is considered as the traditional and the most popular choice of topology because the cascode transistor reduces Miller capacitance and hence provides better gain performance and output to input isolation (S_{12}). Furthermore, the current is reused and hence there is no extra cost in power consumption. The drawback is that an extra v_{on} ($V_{GS} - V_{th}$) is required to bias the cascode transistor in the saturation region, and hence linearity is degraded. This may be undesirable for low voltage-design, and the alternative solution is the cascade topology. However, in a cascade design, more power is usually required because current reuse is no longer applicable, and larger chip area is required if passive loads are used¹. Since this thesis is targeted for both low-voltage and low-power, the cascode topology is chosen for implementation.

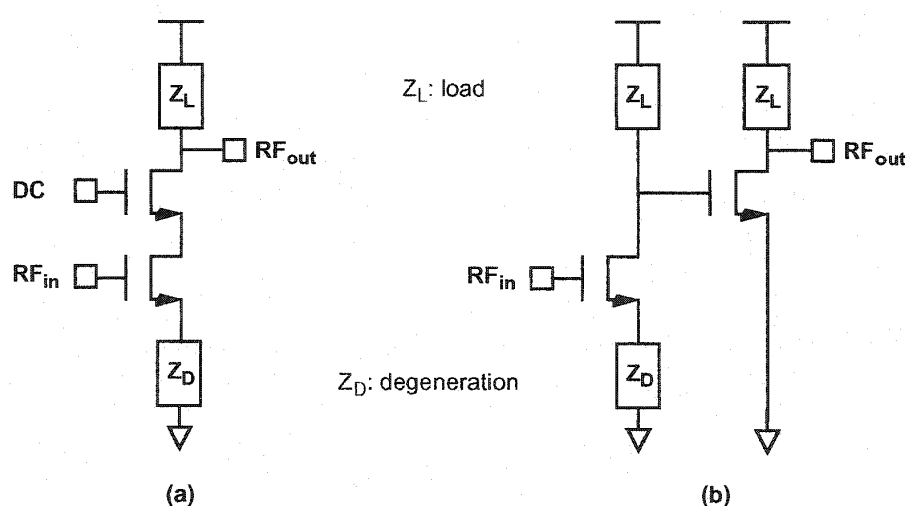


Figure 5.3 (a) Cascode configuration and (b) cascade configuration

1. The chip area is nearly doubled if integrated inductors are used for the loads Z_L . The degeneration Z_D is at least two times smaller than Z_L because of gain and noise performances.

5.3 Simultaneous Power and Noise Matching in LNA

Traditionally, simultaneous power and noise matching is not possible in both bipolar and MOSFET silicon technologies. In the bipolar transistors, the lack of scalable compact models hinders the development of such a technique, while for MOSFETs, the transistors are simply too slow, so that most of the design efforts go towards maximizing gain and power matching at RF while drawing enough power to minimize the noise [Kar96]. Recently, scalable bipolar models such as SGPM and HICUM [Sch96] using emitter scaling, have become available, for example, a scalable high-frequency noise model was proposed in [Voi97]. This model can be directly employed in both bipolar and MOSFET transistors. What this means is that simultaneous power and noise matching can be achieved in a MOSFET if it has sufficient speed. Note that this simultaneous matching does not necessarily lead to the lowest achievable global noise figure¹, but often it is the best compromise between gain and noise. Details are given in Section 5.4.

5.3.1 Speed and Size in MOSFET

One of the common figures of merit to measure the speed of a transistor is the cutoff frequency f_T , the frequency where the small-signal current gain is 1 (or 0 dB). To demonstrate how shrinking the gate length l improves the performance of the transistor, consider the following simplified equation for f_T :

$$f_T = \frac{g_m}{C_{in}} \quad (5.2)$$

where g_m is the small signal transconductance which can be expressed as:

$$g_m = 2 \frac{w}{l} k_p C_{ox} v_{on} \quad (5.3)$$

while in saturation C_{in} is approximately:

1. NF_{min} is defined for a given dc bias. Therefore, the dc required to achieve simultaneous matching does not necessarily give the best NF_{min} .

$$C_{in} = \frac{2}{3}wlC_{ox} \quad (5.4)$$

Combining (5.3) and (5.4) gives the relationship between f_T and gate length:

$$f_T \propto l^2 \quad (5.5)$$

Therefore, a reduction of gate length by 2 times results in a 4 times improvement in speed intrinsically. In reality, this is obviously not the case as the extrinsic capacitances does not scale directly with gate length, and also the square law expression for g_m is not very accurate. However, this simple calculation shows the importance of gate length reduction to speed improvement of transistors.

5.3.2 Design Relaxation in Deep Submicron MOSFET

Consider designing a 1.9 GHz LNA in a commercially available 0.5 μm CMOS technology, with the effective gate length¹ of 0.35 μm and f_T of 35 GHz. For simplicity, assume the small signal current gain² is 10, and a tuned cascode topology with inductive degeneration as shown in Figure 5.3a is used. Then the maximum current gain, assuming 20 dB/decade at roll-off, is about 18. However, adding inductive degeneration (especially with a lossy on-chip inductor) for power matching and linearity, degrades gain significantly. The poor Q on-chip inductor at the tuned-load also reduces gain. Therefore, designing an LNA in this technology for minimum power dissipation simply involves squeezing as much gain as possible at the desired frequency:

1. use minimum gate length for l ;
2. bias the transistor at the current density that gives minimum NF_{min} (see Figure 5.4 in the next section for reference);
3. set transistor width w so it allows enough current for the peak f_T to meet the gain specification;
4. extra current may be necessary to achieve the required linearity.

1. The drawn gate length is 0.5 μm , while the effective gate length (actual) is 0.35 μm .

2. In this example, current gain instead of power gain is used because the figure of merit is f_T not f_{max} .

It is obvious from the above design procedures that the major design variables, namely the width w and the length l , are set to reach the gain at the desired frequency. However, this is no longer the case for subquarter-micron devices because the f_T is much higher, and it is not necessary to bias the transistor at its peak f_T . This relaxation allows simultaneous noise and power matching.

5.4 Minimum Noise Figure and Noise Matching

The noise factor F of the transistor is given by [Gon97]

$$F = F_{min} + \frac{R_n}{G_s} (Y_s - Y_{opt})^2 \quad (5.6)$$

where F_{min} is the minimum noise figure, R_n is the equivalent noise resistance, G_s is the source conductance, Y_s is the source admittance and Y_{opt} is the optimum noise admittance. Using (5.6), the definition for perfectly matched noise is achieved if F is equal to F_{min} , which will occur when Y_s is equal to Y_{opt} . However, the condition $Y_s = Y_{opt}$ does not mean F_{min} is the minimum achievable F_{min} globally. Consider the NF vs. current plot with different transistor sizes as shown in Figure 5.4.

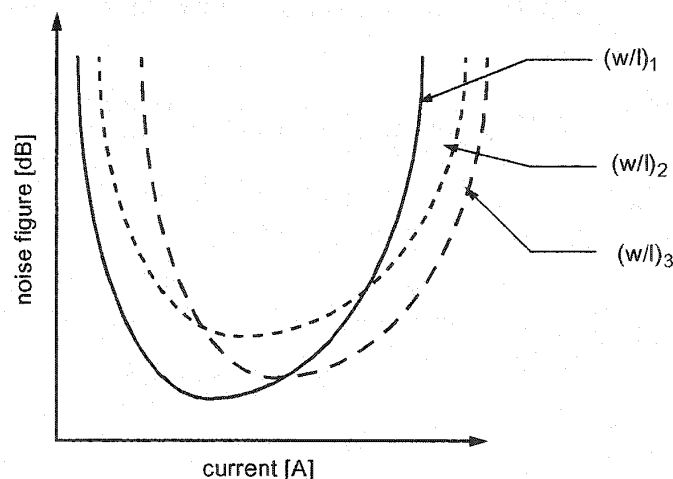


Figure 5.4 NF vs. current of different sizes of MOSFET

There is an optimum transistor size to achieve the lowest possible F_{min} . However, under this condition, simultaneous matching (i.e., $Y_s - Y_{opt}$ and S_{11} minimization) is not likely to be possible because there are not enough design variables (size and current). One other option is to add feedback from the output back to the input (Y_{12}) [Lon00a], but this complicates power matching, and cascode design can no longer provide isolation between the input and the output. Therefore, to achieve simultaneous matching, global minimum F_{min} is discarded for more design variables. In other words, instead of choosing $(w/l)_1$ which gives the minimum F_{min} as in Figure 5.4, $(w/l)_2$ or $(w/l)_3$ may be necessary for matching purposes.

Therefore, it is not guaranteed that simultaneous noise and power matching results in the best design in terms of NF because F_{min} is no longer minimal. However, in RF, the change in F_{min} is usually small (within 0.5 dB for submicron design) while “ $Y_s - Y_{opt}$ ” is often the dominant factor. Therefore, this matching technique is beneficial for CMOS LNA circuits.

5.4.1 An Example 2 GHz CMOS LNA Design

The technology used in this design is a commercially available 0.24 μm CMOS technology, and the desired carrier frequency is 2 GHz. First, the optimum current density is determined by sweeping F_{min} vs. V_{GS} using minimum gate length, and then the dc bias and degeneration inductance are set such that

$$S_{11} = \Gamma_{opt}^* \quad (5.7)$$

Once this condition is met, an input inductor can easily be added to match both S_{11} and Γ_{opt} to 50 Ω . The simulated results are shown in Table 5.1 and Figure 5.5.

As good as it may seem, a new solution is usually accompanied by a new problem. Due to the small geometry of the device, on-chip matching becomes extremely difficult, and this is discussed in the next section.

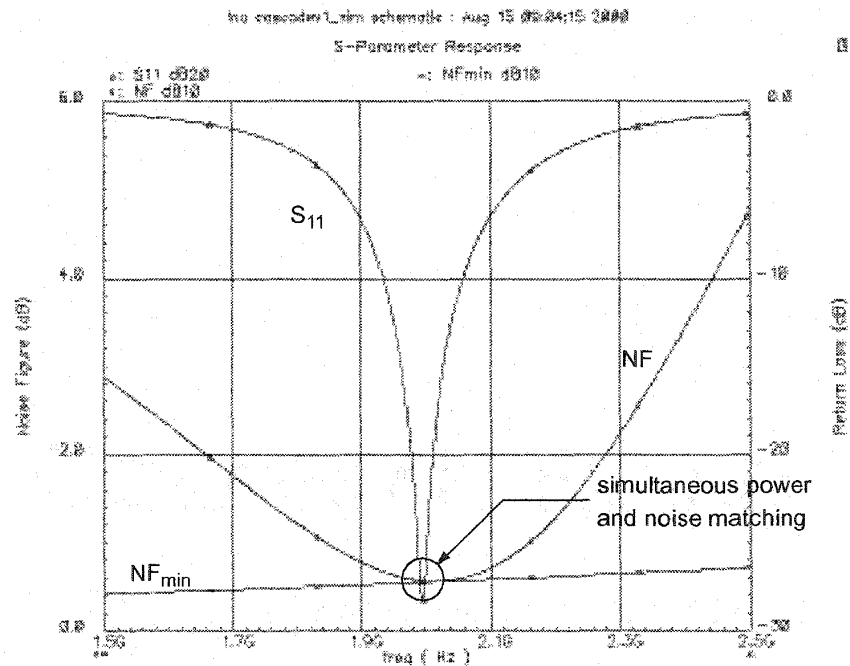


Figure 5.5 Simulation of a 2 GHz bulk 0.24 μm CMOS LNA with gate inductor off-chip

Table 5.1: Simulated result of a 2 GHz CMOS LNA with 20 nH off-chip inductor

Voltage Supply	1.5 V	2.5 V
Gain	15 dB	15 dB
NF ^a	0.68 dB	0.56 dB
Input 1dB Compression	-21.7 dBm	-21.7 dBm
IIP3	-9.2 dBm	-7.8 dBm
Power Dissipation	4.4 mW	9.5 mW

a. Free lunch: something too good to be true is usually false.

5.5 Power Matching in Deep Submicron Devices

The improvement in speed of subquarter micron devices allows design relaxation, and hence simultaneous power and noise matching becomes achievable. One of the reasons for the speed improvement in deep submicron technology is due to gate area reduction, such that C_{in} is decreased and hence the speed improves as described in (5.2). At the same time, however, if single chip integration is desired¹, small C_{in} imposes major matching problems, especially at the low GHz range. For example, consider the RF input stage of the LNA as shown in Figure 5.6.

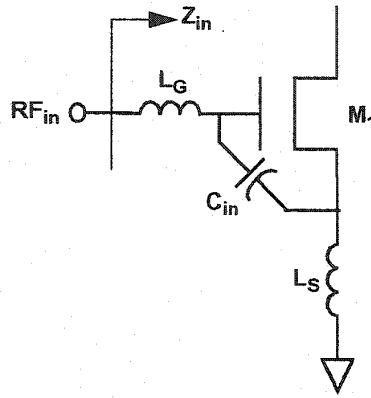


Figure 5.6 LNA input transistor

The input impedance Z_{in} is given by:

$$Z_{in} = R_0 + j\omega(L_G + L_S) + \frac{1}{j\omega C_{in}} \quad (5.8)$$

where R_0 is the real part of Z_{in} (R_0 is 50Ω for perfectly matched input). The imaginary terms can be resonated out by setting

$$\omega(L_G + L_S) = \frac{1}{j\omega C_{in}} \quad (5.9)$$

1. Single-chip integration is the main driving force for RF CMOS, or otherwise one should stick with GaAs FETs or HBTs for multi-chip solution.

For this particular technology, the transistor requires $0.24\ \mu\text{m}$ by $150\ \mu\text{m}$ to draw $4\ \text{mA}$ of current for circuit operation. However, the C_{in} in this dimension is less than $400\ \text{fF}$. For simplicity, assume the C_{in} is $400\ \text{fF}$, and to match the input stage to $2\ \text{GHz}$, the required total inductance ($L_G + L_S$) is $15.8\ \text{nH}$! A large L_S degrades the gain of the amplifier significantly, while making L_G huge (on-chip) impacts the noise figure directly. It is interesting to note that the component values are more reasonable at higher frequencies. For example, at $6\ \text{GHz}$, the required inductance ($L_G + L_S$) is only $1.76\ \text{nH}$. Note that adding an extra capacitor to C_{in} is feasible, but this decreases the gain of the transistor dramatically¹. The detail is given in Section 5.5.1.

The poor Q of on-chip inductors is a stumbling block for deep submicron CMOS LNA, at least for frequencies in the low GHz range. For example, for a good commercial process, the highest achievable Q on-chip of a $10\ \text{nH}$ inductor is about 10 in a silicon bulk process². Using the simple formula

$$R = \frac{\omega L}{Q} \quad (5.10)$$

the parasitic series resistance (just dc: ac will be even higher) is about $12\ \Omega$. The noise figure, simply from the resistance of the inductor, will be

$$NF = 10\log\left(\frac{N_{src} + N_{ind}}{N_{src}}\right) = 10\log\left(\frac{50 + 12}{50}\right) = 1.9\text{dB}$$

The most direct solution is to reduce the parasitic resistance, or in other words, to boost the Q of the inductor. The two obvious methods are (a) to boost the Q by poly-shielding [Yue97] or (b) to reduce the inductance. Let's consider (a) first³.

-
1. Doubling C_{in} would result in $6\ \text{dB}$ loss in gain voltage, according to equation (5.2).
 2. For inductance of $3\ \text{nH}$ the Q is about 20 in this process.
 3. The odd thing is that whatever is considered first usually does not work.

5.5.1 Polysilicon Shielding in Gate Inductor

Two vital features for a good inductor process are highly conductive metal and good device isolation. Adding a poly shield effectively brings the ground plane closer to the inductor and hence reduces isolation. This not only reduces the self-resonant frequency of the inductor, but, as will be shown next, the added capacitance severely degrades the speed of the associated transistor performance, especially if the device has a deep submicron feature size. Consider the inductor and its equivalent circuit model as shown in Figure 5.7.

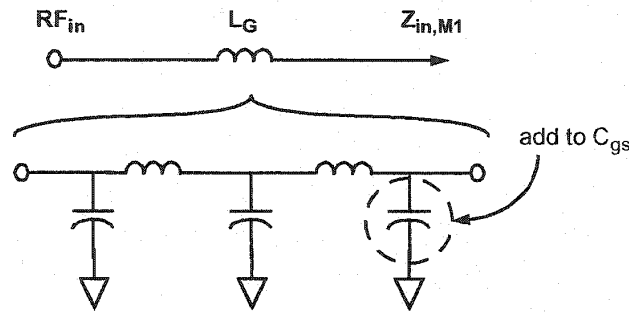


Figure 5.7 A simple inductor model

For this particular technology, the dimension for a 7 nH inductor at 2 GHz is about 400 μm by 400 μm with a hollowness¹ of 0.5. The oxide thickness from the inductor to the ground substrate is 8.2 μm , and the effective additional capacitance to C_{in} is 1/3 of the total capacitance, then

$$C_{add} = \frac{1}{3} \cdot \frac{\epsilon_r \epsilon_0}{t_{ox}} \cdot A_{ind} = \frac{1}{3} \cdot \frac{3.9 \times 8.854 \times 10^{-12}}{8.2 \times 10^{-6}} \cdot (400 \times 10^{-6} \cdot 400 \times 10^{-6}) = 0.1 \text{ pF}$$

Recall that C_{in} is less than 0.4 pF, so adding a ground shield to the gate inductor results in an additional 0.1 pF of parasitic capacitance, which reduces the speed of the transistor at least by 25%, or 2.5 dB loss in voltage gain.

1. Hollowness is the metal-to-void ratio (a measure of metal density) for a given area, that is defined by the periphery of the outermost spiral [IBM00].

5.5.2 Input Inductance Reduction

If the inductance can be reduced, the improvement can be significant because (a) shorter wire means less parasitic resistance, and (b) smaller area means less loss and hence higher Q . If the inductance is reduced from 10 nH to 4 nH, then Q can be improved from 10 to 20, and hence the parasitic resistance will be reduced from 12 Ω to 2.4 Ω using equation (5.10). From equation (5.9), inductance reduction can be achieved by increasing C_{in} , or by changing the system specification (e.g., by increasing the LNA frequency). Since the second option is not usually available, let's focus on the first option.

Increasing C_{in} can be achieved by simply using a bigger transistor at the expense of power. There are three parameters controlling the dimensions of the transistor: the length l , the width w , and the number of fingers m . Increasing l reduces device speed, while increasing w increases gate resistance. Increasing m seems to be a better choice. Assuming a linear relationship as in (5.9) and L_S is small¹, doubling C_{in} by doubling m reduces L_G (Figure 5.6) by about a half, but increases current by 2 times at the same time. Unfortunately, power is usually the prime consideration in mobile circuit design, and therefore this approach seems to be unfavorable unless there is a way to reduce the current. One way is to take advantage of the fact that it is not required to bias the device at its peak f_T .

Lowering V_{GS} drastically reduces I_D but not f_T , so it is possible to increase C_{in} without an excessive increase in I_{DD} and with a minimum disturbance to f_T (which translate directly to gain and noise performance). This is because I_{DD} is proportional to v_{on}^2 while g_m is only proportional to v_{on} . From simulation, a 20 nH input inductance is reduced to 7 nH with a 30% increase in I_{DD} at 2 GHz. This indicates that a CMOS LNA with all inductors on-chip is feasible with the availability of a deep submicron process. Note that input dynamic range and linearity can be degraded significantly due to small v_{on} . The simulation results are shown in Figure 5.8.

1. When speed (and hence gain) is an issue, L_S is usually much smaller than L_G because of gain degeneration. If there is enough gain, it is better to increase l rather than increase m .

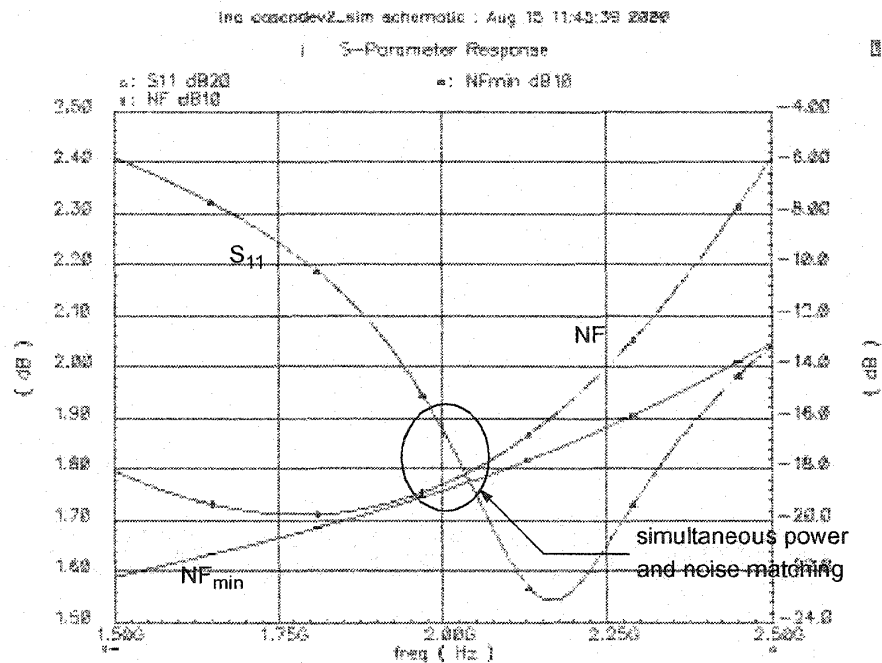


Figure 5.8 Simulation of a 2 GHz bulk 0.24 μm CMOS LNA with L_G on-chip

Table 5.2: Simulated result of a 2 GHz CMOS LNA with 7 nH on-chip inductor

Voltage Supply	1.5 V	2.5 V
Gain	12.1 dB	12.1 dB
NF	1.81 dB	1.76 dB
1dB Compression	-8.0 dB	-6.6 dB
IIP3	N/A ^a	-2.0 dBm
Power Dissipation	7.1 mW	12.0 mW

a. The MOSFET is operated at the verge of inversion and the simulator hits some discontinuous region of the model.

5.6 CMOS LNA in SOI

Using the simultaneous matching design methodology outlined previously, a 1 V, 5.8 GHz LNA is designed for possible wireless LAN application. The topology is similar to the LNA in Section 5.3, except that (a) a PMOS load is used instead of an LC resonator¹, and (b) the bias-T source follower (see Section 4.9) is used to replaced the output matching network. The schematic is shown in Figure 5.9.

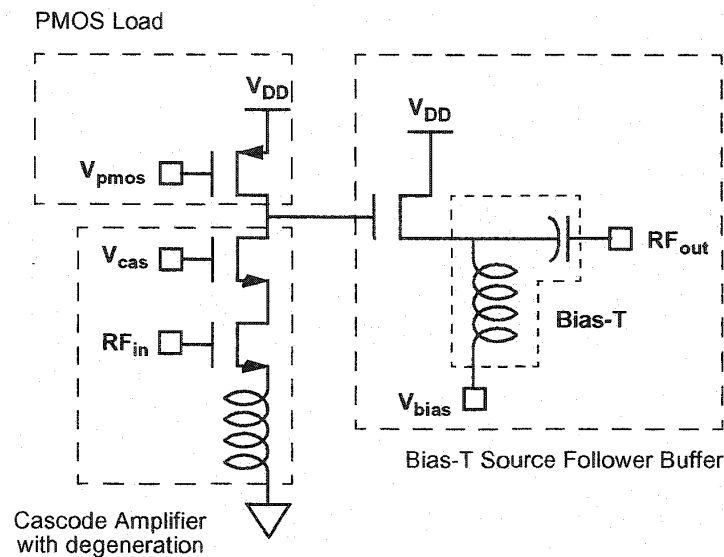


Figure 5.9 Cascode LNA with PMOS load in SOI

The PMOS load can be operated in two modes: (a) saturation mode and (b) triode mode. In the saturation mode, the PMOS device serves as a current source, and the gain is high. To avoid the transistor leaving the saturation region, the current of the PMOS load must be made the same as the NMOS transistors by adjusting both V_{DD} and V_{PMOS} , and complex biasing circuits are required. Furthermore, the dc gain is very high that extra circuitry may be needed to stabilize the amplifier². In the triode mode, the PMOS behaves like a voltage-controlled resistor, and the noise

1. If an LC resonator is used, the $2x V_{DD}$ swing may destroy the cascode transistor and the output buffer.
2. The input matching, however, may provide enough filtering to stabilize the circuit.

performance is better [Joh97] but the gain is lower compared to the saturation operation. The supply V_{DD} remains undisturbed, and only V_{PMOS} is required to be adjusted to control the gain. Thus, V_{PMOS} can serve as a tuning node for automatic gain control (AGC) in a later application of this amplifier in a receiver.

The main reason for choosing this topology instead of a tuned load is because of the lack of accurate analog models for both transistors and inductors during the design stage¹. Therefore, using both a PMOS load and output buffer allows the output to be matched over a wide band of frequencies, which means less difficulty in matching the output. A PMOS load is inherently a wideband element if the reactive parasitic components are small, while the buffer matching is achieved by adjusting V_{bias} of the source follower so that $1/g_m$ of the transistor is equal to $50\ \Omega$. Note that this type of buffer may only work in SOI but not bulk CMOS because negative bias may be used at the source. The simulation results of this LNA are shown in Figure 5.10².

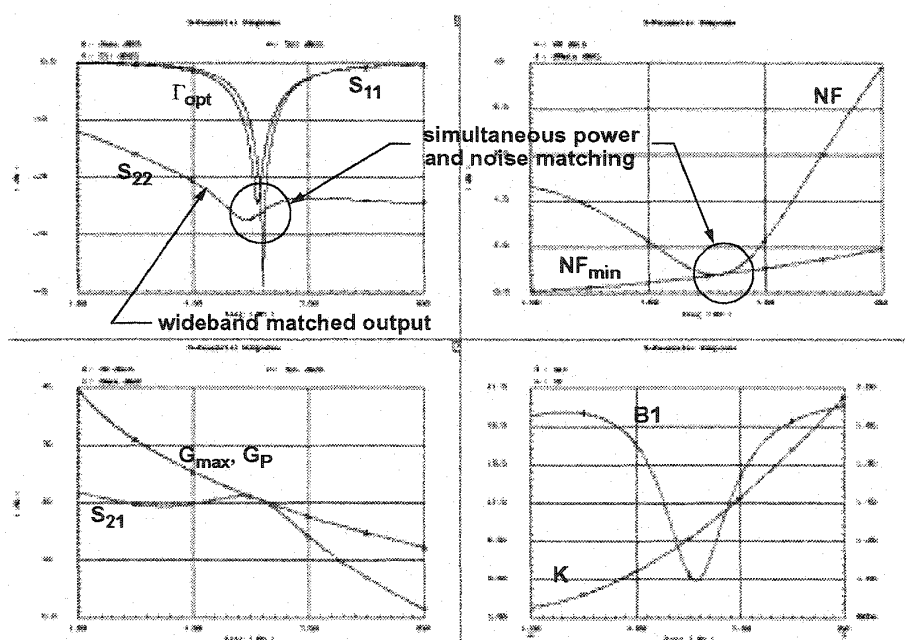


Figure 5.10 Simulation of a 5.8 GHz LNA in SOI

1. The circuit was designed before the technology was qualified.
2. The simulations shown are for proof of concepts. Only graphical data is available for this documentation.

5.7 LNA with Image Reject Filter

The image reject (IR) filter is used to suppress the unwanted image frequency located two IF's away from the desired carrier frequency. For example, in this design the RF is 5.4 GHz and the IF is at 500MHz. Therefore, the image reject filter should have a notch at either 4.4 GHz (for LO = 4.9 GHz) or 6.4 GHz (for LO = 5.9 GHz) depending which sideband is to be mixed at the mixer.

Traditionally, off-chip components such as SAW filters are used for image rejection, but these devices usually cannot be integrated monolithically, which defeats the purpose of single-chip integration. An integrated IR filter using an on-chip inductor was proposed [Mac98][Sam00], using an active negative g_m circuit to boost the Q of the inductor to achieve useful rejection.

For this work, the negative g_m circuit is not used, but the filter relies only on the high Q inductor to provide the image rejection. By pushing the passive technology to the limit, the filter consumes no dc power, and may be suitable for low power application if the rejection is respectable.

A few options can be used to modify the LNA circuit to achieve the required transfer function (i.e., a notch at a particular frequency). Since the LNA is a linear circuit, modifying the output impedance Z_o directly changes the transfer function because

$$H(f) = g_m Z_o \quad (5.11)$$

Consider the circuit as shown in Figure 5.11a [Mac98], and the equivalent model as shown in Figure 5.11b. By simple circuit analysis, the output impedance Z_o is:

$$Z_o \approx r_{oc} [1 + g_m (C_{in} \parallel r_{od} \parallel Z_{IR})] \quad (5.12)$$

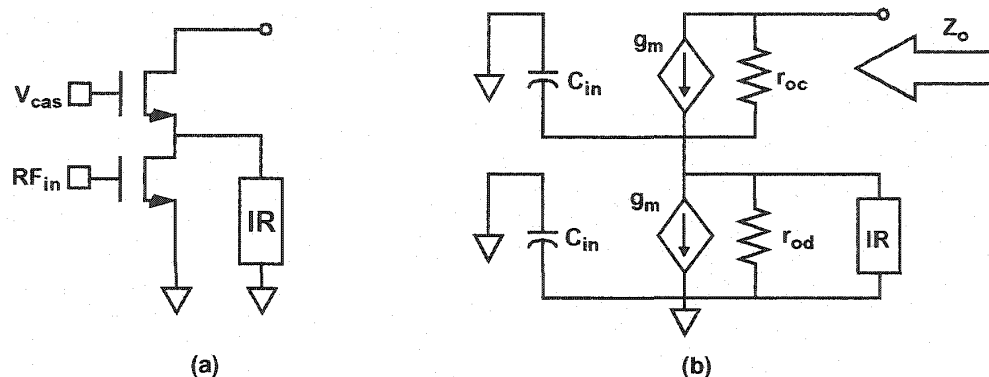


Figure 5.11 (a) Cascode amplifier with IR filter and (b) equivalent output impedance

To obtain a notch at a particular frequency, from equation (5.12) a zero is required at the resonant frequency, therefore a series LC resonator is required. To obtain a deeper notch, the order of the resonator is increased by adding a capacitor in parallel with the inductor of the resonator. The schematic of the image reject filter is shown in Figure 5.12b. All capacitors are implemented as varactors for frequency and Q tuning of the filter. Since the inductor has a very good Q , and the image reject specification is very relaxed (about 9dB image attenuation), no actives are used for Q boosting. Therefore, this image reject filter does not draw any DC current. The transfer function of the image reject filter is:

$$Z_{IR}(s) = \frac{L_{IR}(C_{IR1} + C_{IR2})s^2 + 1}{C_{IR1}C_{IR2}L_{IR}s^3 + C_{IR1}s} \quad (5.13)$$

An all-passive image reject filter on-chip is added to the LNA for image rejection. The schematic is shown in Figure 5.12, and the simulation result in Figure 5.13.

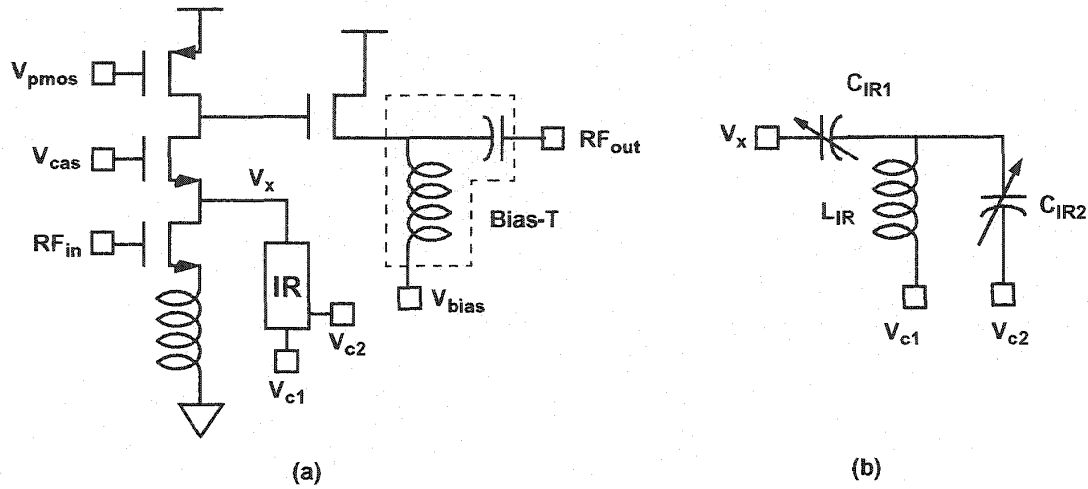


Figure 5.12 (a) LNA with image reject filter and (b) image reject filter

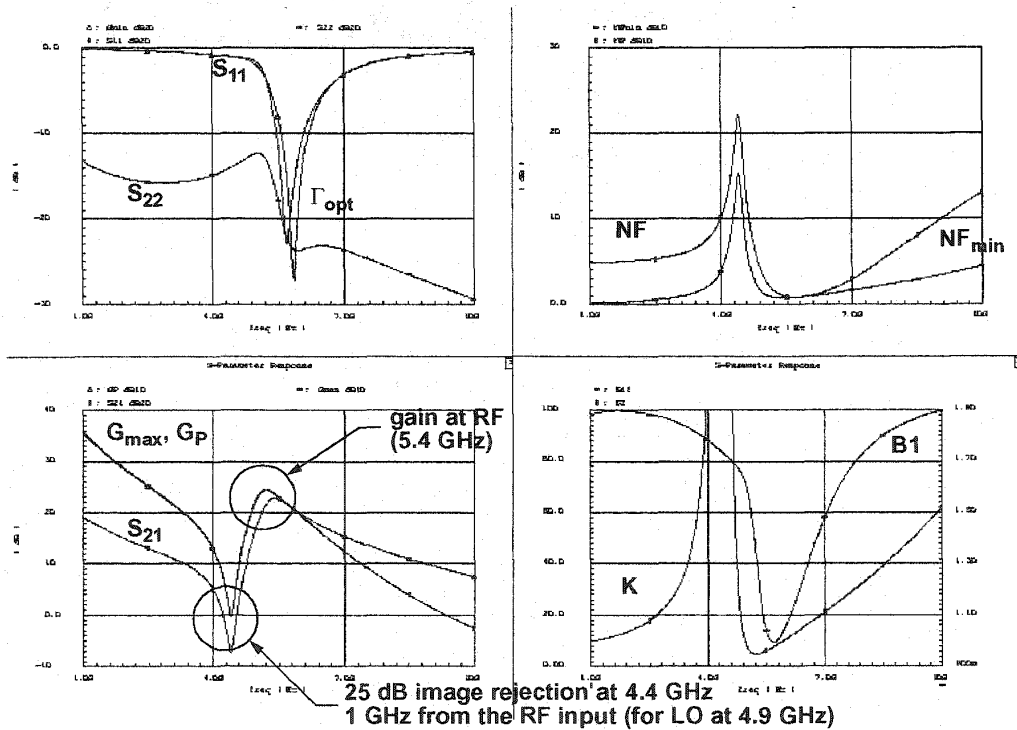


Figure 5.13 Simulation of a 5.4 GHz LNA with image rejection

5.8 Layout, Test and Measurement

The layout of the LNAs are shown in Figure 5.14. Since all the circuits are single-ended, the chip is designed for on-wafer measurement. Tune-stubs will be used for external matching.

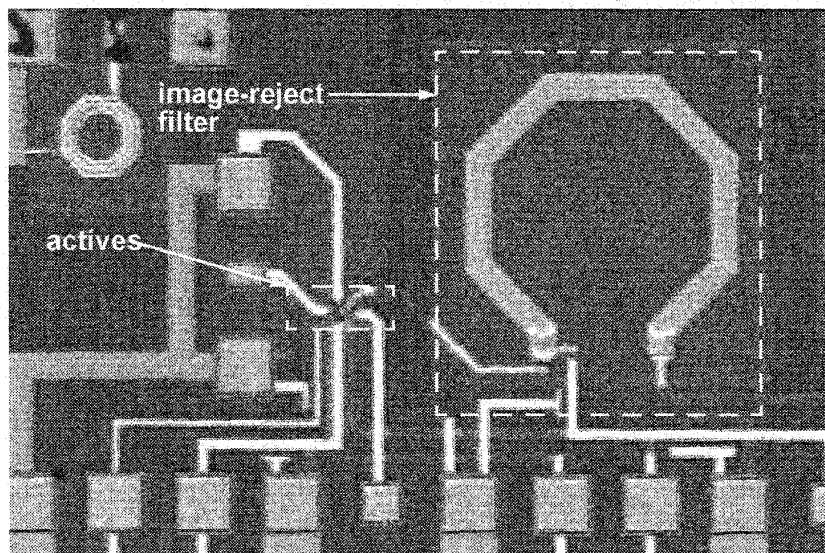


Figure 5.14 Layout of the SOI LNA

5.9 Summary

In this chapter, the feasibility of simultaneous noise and power matching in submicron CMOS is examined, and this technique is applied in designing two 2 GHz CMOS LNAs in bulk CMOS as examples. The technique is also applied to the SOI design. The LNA has gain controllable by using a PMOS load, and a new SOI-only output buffer topology is used to measure the output signal. An all-passive zero-dc-power image-rejection circuit was added to one of the LNA designs, utilizing the high Q inductors designed in Chapter 3.

Chapter 6 Analog-to-Digital Converter

In this chapter, data conversion circuits are chosen to demonstrate high-speed and low-voltage capabilities of SOI for mixed-signal applications. The first circuit is an oversampling $\Delta\Sigma$ ADC to demonstrate low-voltage low-power switched-C circuit performance in SOI technology. First, the classic theory of oversampling $\Delta\Sigma$ conversion technique is reviewed, and the circuit design using a double-sampling technique is given. Next, the experimental results are presented, along with a discussion on low-voltage low-power switched-C circuits.

Next, a pipelined ADC design is examined with simulation to demonstrate high-speed analog capabilities. The pipelined ADC design serves as a stepping stone for future high-speed bandpass $\Delta\Sigma$ ADC circuit implementations, which are touched upon at the introduction of the circuit. Then, the design challenges of low-voltage high-speed circuits are examined, and the solution using complementary topology with digital correction is suggested. The proposed methodology is verified by simulation.

6.1 Oversampling Delta-Sigma Modulation Theory

Oversampling $\Delta\Sigma$ modulation is one of the most popular methodologies to achieve high resolution data conversion with low cost technologies. This method was originally developed for analog-to-digital signal conversion, but it is widely used in other areas including RF applications such as radio bandpass filters [Sin95], frequency synthesis [Ril93] and frequency discrimination

[Bea94]. Conventional ADC requires high precision analog components, while an ADC with $\Delta\Sigma$ modulation uses simple and crude analog circuits with less precision, but has to operate at a frequency much higher than the Nyquist rate. For example, a conventional 8-bit ADC can be replaced by a $\Delta\Sigma$ loop using only a 1-bit quantizer and a relatively low-order filter. However, the data has to be oversampled, which means the system has to run at a greater speed and hence higher power consumption. Hence, submicron SOI technology is considered to be a good candidate with which to implement this type of converter for its low power and high speed capabilities.

6.1.1 Oversampling and Noise Shaping

The philosophy behind $\Delta\Sigma$ modulation is a combination of (a) oversampling and (b) noise shaping. Oversampling is well-understood from the classic digital modulation theory, in that each doubling of frequency decreases the in-band noise by 3 dB, thus increasing the resolution by 0.5 bit [Nor97]. Therefore, to achieve an 8-bit resolution from a 1-bit ADC, the sampling rate has to be at least 2^7 or 128 times greater than the Nyquist rate ($\text{OSR} > 128$). Meanwhile, noise shaping refers to shifting the quantization noise away from the band of interest (Figure 6.1), and this can be achieved by using a feedback loop.

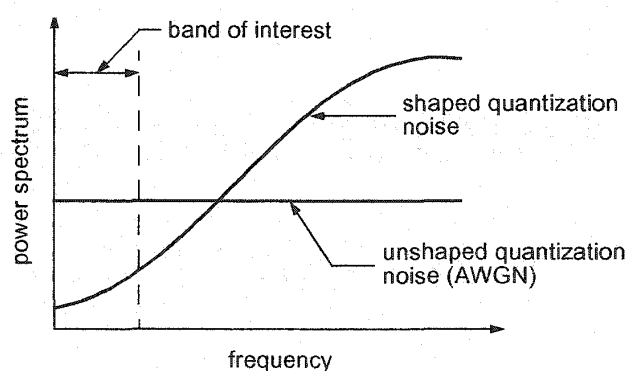


Figure 6.1 Noise shaping

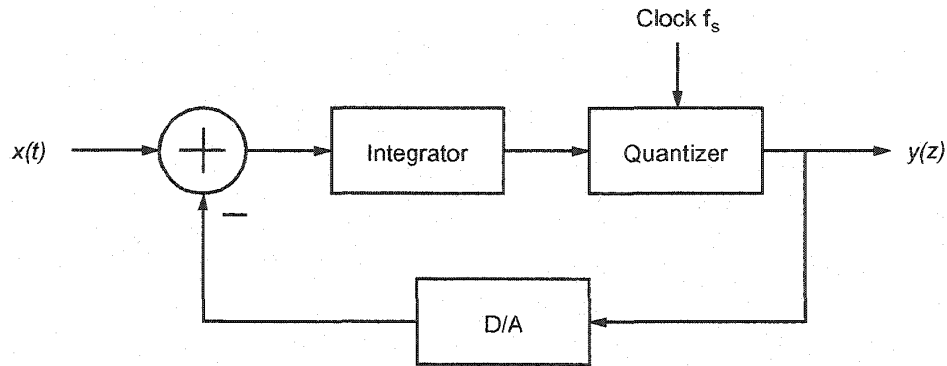


Figure 6.2 $\Delta\Sigma$ feedback loop for noise shaping

Consider the feedback system as shown in Figure 6.2. $x(t)$ is the continuous input signal to the system, while $y(z)$ is the sampled digital data at sampling frequency f_s after the quantizer. If the integrator has infinite gain, then *on average*, $y(z)$ is the digital representation of $x(t)$ such that

$$\overline{x(t)} = \overline{y(z)} \quad (6.1)$$

because the negative feedback loop forces the input of the integrator to be zero. To analyse noise shaping, the loop is linearized as shown in Figure 6.3.

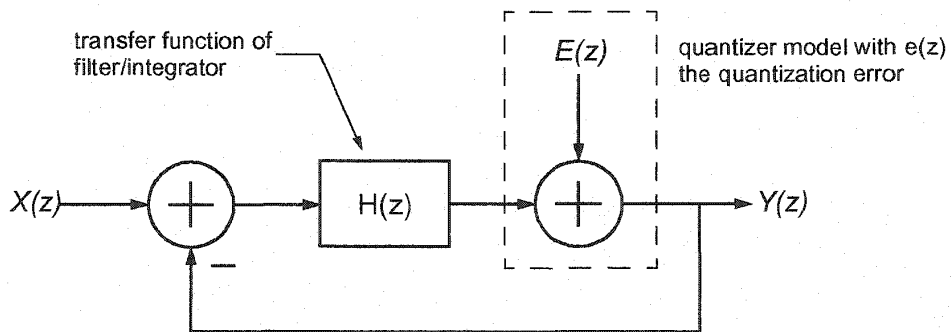


Figure 6.3 Linearized transfer function of the $\Delta\Sigma$ loop

From simple control theory, the transfer function of the loop is

$$Y = \frac{HX + E}{1 + H} \quad (6.2)$$

Since it is only the noise but not the signal that is to be shaped, the analysis can be simplified by splitting (6.2) into two parts: the noise transfer function (NTF), and the signal transfer function (STF) as follows:

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \quad (6.3)$$

$$STF = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \quad (6.4)$$

The filter H often has high gain around the signal frequency, and the gain rolls off as the frequency approaches the out-of-band region. Therefore, in terms of magnitude, the in-band NTF is $1/H$ while the in-band STF is 1. This suggests that the filter H only alters the noise spectrum but not the signal, and hence noise can be shaped by applying proper filters. The noise shaping technique improves the in-band noise by $6 \times N$ dB per octave, where N is the order of the filter. Therefore, for every doubling of the sampling rate, $\Delta\Sigma$ modulation improves the resolution by $6 \times N + 3$ dB. If a 1-bit quantizer is used in the $\Delta\Sigma$ loop with a second-order filter H , the resolution is improved by 15dB or 2.5 bits per octave. Therefore, instead of $OSR > 128$, an OSR of 8 is sufficient to achieve an 8-bit Nyquist ADC performance.

6.1.2 Low-Pass $\Delta\Sigma$ Modulator Transfer Function

This type of modulator converts a baseband analog waveform into a digital signal, which has the same functionality as the classical Nyquist ADC. The reason it is called “low-pass” is because a low-pass filter (namely an integrator) is used for $H(z)$. Consider a first-order integrator used in the $\Delta\Sigma$ loop. The transfer functions are

$$H(z) = \frac{1}{z - 1} \quad (6.5)$$

$$NTF = \frac{z-1}{z} \quad (6.6)$$

$$STF = \frac{1}{z} \quad (6.7)$$

From (6.6), the noise is shaped from a flat AWGN to a 20dB per decade high-pass function (similar to Figure 6.1) with a zero at dc. NTF is high-pass because H is a low-pass function, and the magnitude of NTF is approximately $1/H$. As for the STF, it remains constant except for a sample delay.

Even though the first-order loop described above has the simplest implementation, the resolution gained from noise shaping is marginal, and the first-order system has some unique but adverse problems such as severe idle tones from limit cycles. Therefore, a second-order $\Delta\Sigma$ loop is constructed by cascading two integrators from (6.5) together to form the filter:

$$H(z) = \left(\frac{1}{z-1} \right)^2 \quad (6.8)$$

This gives a high-pass NTF for which noise shaping is improved from 20 dB to 40 dB per decade. A second-order low-pass $\Delta\Sigma$ modulator is inherently stable [Nor97], and therefore stability analysis is not included.

6.2 Low Power Delta-Sigma ADC

A low-power second-order double-sampled $\Delta\Sigma$ ADC with 50MHz sampling rate in a 0.25 μ m FDSOI CMOS technology [MIT] was first designed and implemented by Swaminathan, and later tested and analyzed by the author [Swa99]. FDSOI has a better subthreshold swing and reduced short-channel effect than traditional bulk CMOS as described in Chapter 2, and therefore the threshold voltage and hence the supply voltage can be lowered for low power applications.

6.2.1 Design and Simulation

In this section, a circuit is discussed which was originally designed, simulated and implemented by Swaminathan [Swa99]. The contributions of the author are described in the next section. The double-sampling technique [Yan96] was used in the circuit to enhance speed performance. This technique involves using the opamp in a switched-C integrator on both phases of the clock, effectively doubling the sampling rate. Consider a classical integrate-and-dump integrator as shown in Figure 6.4. The opamp is accumulating the charges during phase 1, but remains idle for the duration of phase 2 and hence is wasting power. The double-sampling technique allows the opamp to work during both phases by adding another set of switches (Figure 6.5) so that $S1$ is integrating while $S2$ is dumping in phase 1, and $S1$ is dumping and $S2$ is charging during phase 2.

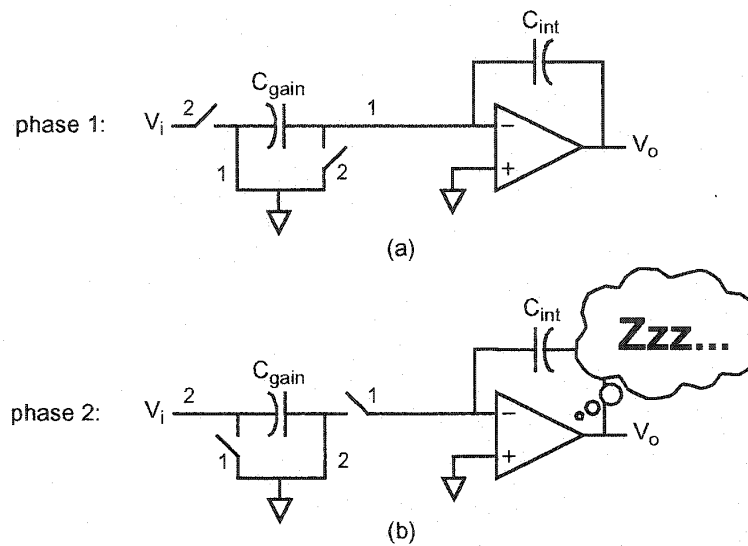


Figure 6.4 Integrate-and-dump integrator: (a) integration phase and (b) dump phase

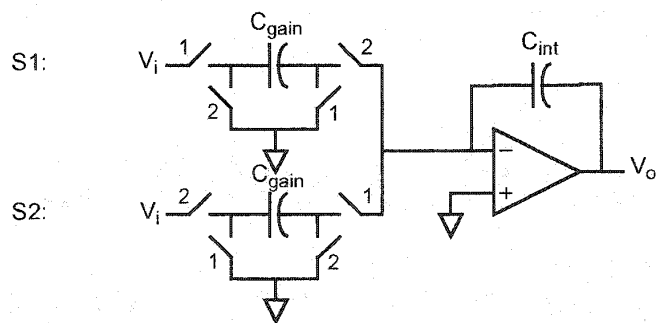


Figure 6.5 Double-sampling configuration

As the OSR doubles, the resolution is increased by $6 \times N + 3$ dB or 15 dB improvement. The disadvantage of using a double-sampled circuit is the mismatch between paths. This causes any signals at $f_s/2$, namely the high-power out-of-band quantization noise, to be mixed down near dc. Since the output is fed back to the input, high-power quantization noise is mixed into baseband, degrading the SNR. Therefore, a bilinear integrator was employed in the first stage to average out the error caused by capacitor mismatch, because the first stage dominates the noise-shaping performance of a $\Delta\Sigma$ modulator [Yan96]. The circuit diagram is shown in Figure 6.6.

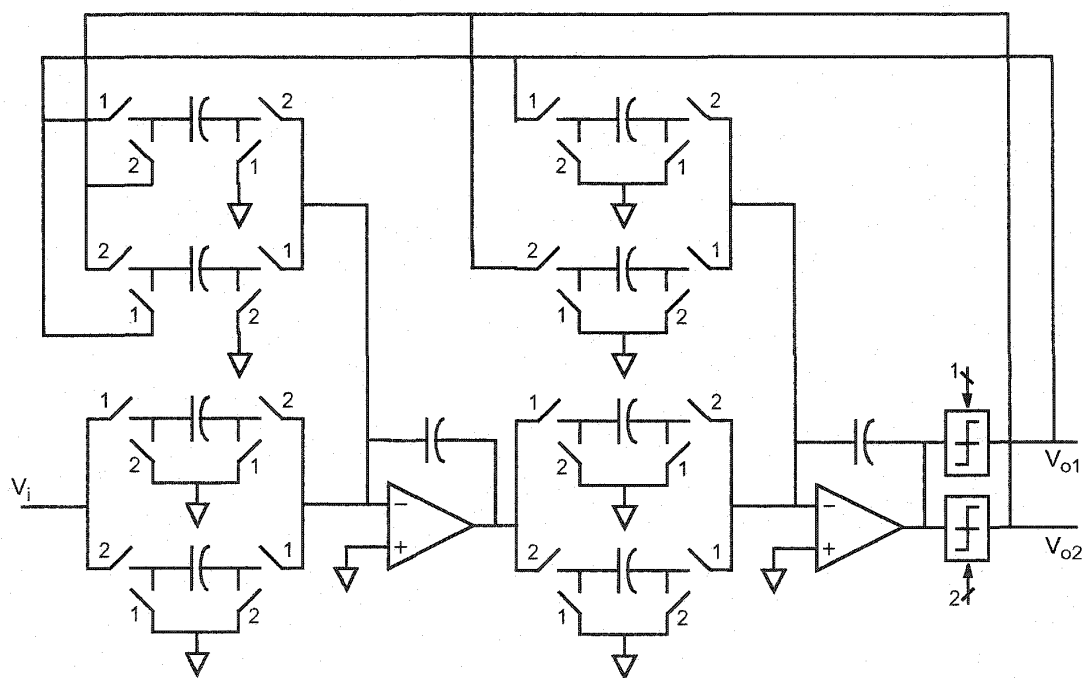


Figure 6.6 Second-order $\Delta\Sigma$ modulator with the bilinear first stage

The circuit was a single-ended design using single-ended cascode inverter amplifiers as shown in Figure 6.7. These amplifiers had a fairly good simulated gain of 43 dB and 164 MHz UGBW.

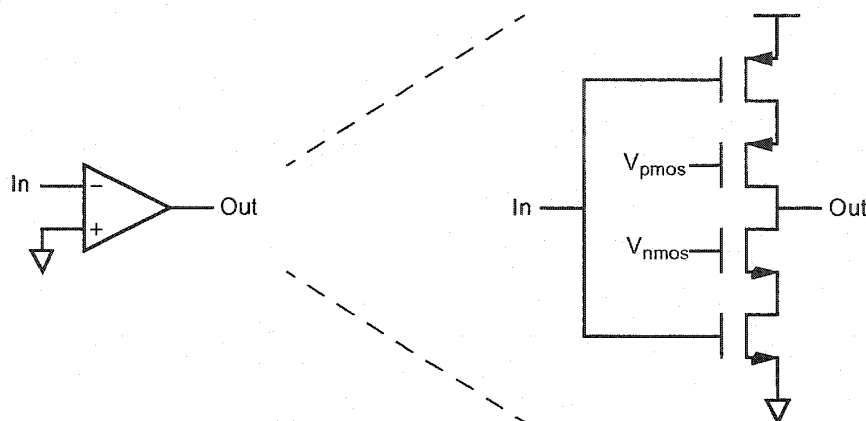


Figure 6.7 Single-ended cascode inverter amplifier

The obvious problem with this design is that the analog ground voltage is ill-defined. Any mismatch between analog ground and the midpoint voltage threshold results in a dc offset at the output of each amplifier. This leads to a reduction in dynamic range. The comparator was a simple preamp/sense amplifier [Joh97]], which has very low power dissipation.

Since this process [MIT] does not have analog poly-poly or MIM capacitors, low- Q capacitors were formed using the n-well as the bottom plate, gate oxide as the insulator and n-type polysilicon as the top plate. The minimum capacitor used was 0.4 pF, which has a kT/C noise of 100 mV_{rms} over the entire sampling bandwidth.

The modulator was simulated with the BSIM3v3 SPICE model. The spectrum can be seen in Figure 6.8 for a 10 MHz and 50 MHz clock frequency (effective sampling rate is 20 MHz and 100 MHz respectively). The SNR numbers are shown for an OSR of 50. The power dissipation for both sets of data was 200 mW.

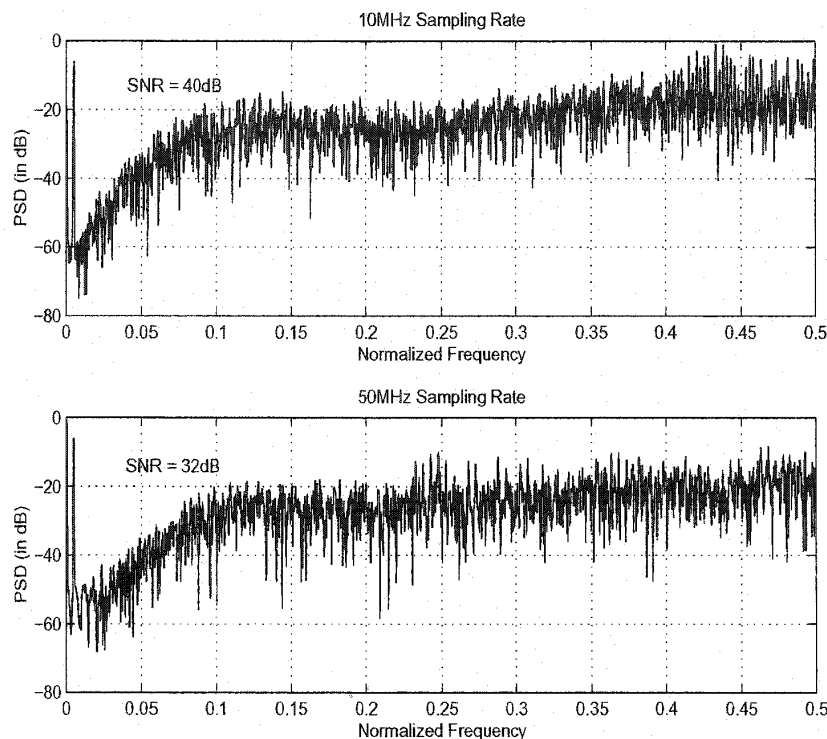


Figure 6.8 Simulation result for second order $\Delta\Sigma$ modulator

6.2.2 Experimental Results

In this section, contributions by the author are discussed. This includes testing and debugging the circuit, evaluating the performance, and presenting the overall work at a conference [Swa99].

The circuit was tested with an HP4145 semiconductor parameter analyzer to provide dc biases and to perform low current measurements for power calculations. There are two modes of operation for this modulator: the normal mode and the low-power mode.

In the normal mode, the op-amps are biased at the nominal supply voltage (1 V) so that the op-amps can operate at a higher frequency. Figure 6.9 is the power spectrum of the output. The input signal is a -13 dBm sinusoidal tone at 100 kHz, and the effective sampling rate is 50 MHz, which

is limited by the available test equipment. The SNR is 36 dB (6 bits) over a 1 MHz bandwidth, and 48 dB (8 bits) over a 200kHz bandwidth, corresponding to CDMA and GSM bandwidths respectively. The power dissipation is 300 mW. As shown in Figure 6.9, the second-order low-pass noise shaping is clearly indicated by the 40 dB/decade slope from 600 kHz to 3 MHz.

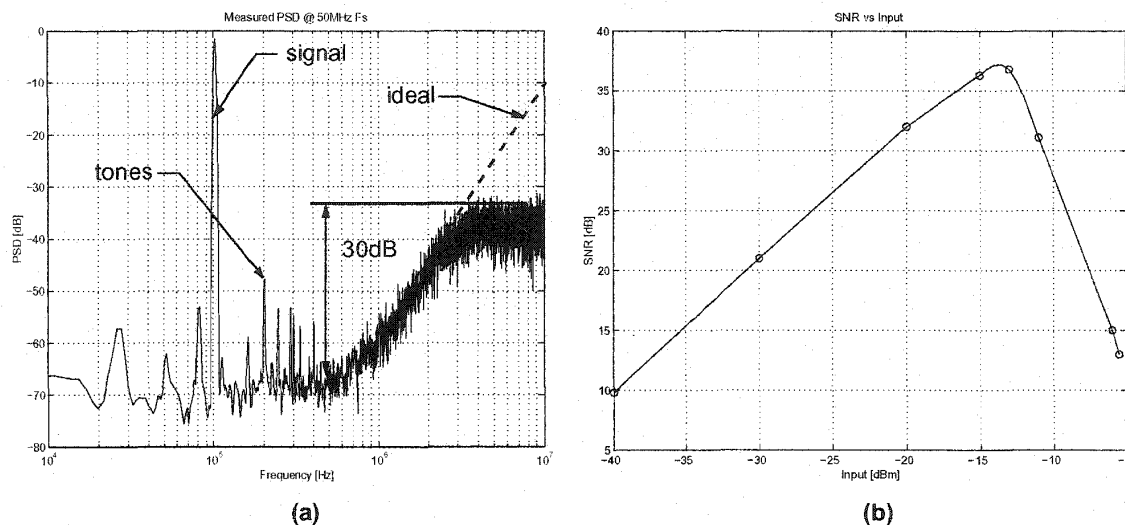


Figure 6.9 Normal mode (a) power spectrum and (b) SNR vs. input power at BW = 1 MHz

The low frequency noise floor has only been attenuated by about 30 dB, which is 10 dB worse than the simulation results. This phenomenon is either due to the high circuit noise or low opamp gain. The circuit noise can be examined by adjusting the amplitude of the feedback signal. In simulation, adding extra power to the feedback signal lowers the quantization noise until the threshold where the improvement stops and the noise floor increases again due to the circuit noise. This relationship is shown in Figure 6.12. However, when the amplitude was increased in this circuit during the measurement, the noise floor could not be further decreased, which suggested the performance of the circuit was limited by the low opamp gain. The opamp gain is reduced because the opamps cannot be biased at the optimum analog ground due to the cascade configuration and incompatibility between required input and output voltages. Instead, the best gain was achieved in the non-linear region, and this led to a poor harmonic distortion (HD): an

HD2 of -48 dB and an HD3 of -54 dB. Measurement shows that a slight shift of analog ground (50 mV) can result in the distortion increasing by 30dB.

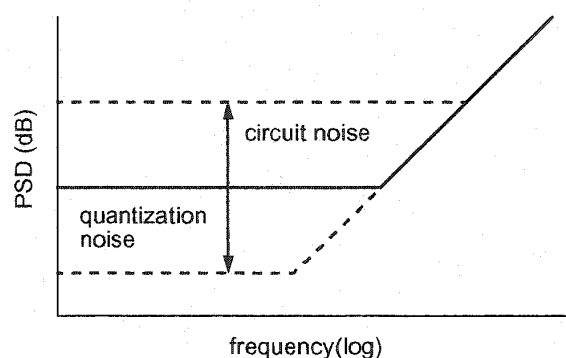


Figure 6.10 Circuit and quantization noise for increasing feedback voltage

Over a 1 MHz bandwidth, the HD contribution to total noise is insignificant, and therefore the SNR is close to the SNDR (noise+distortion). However, for a bandwidth of 200 kHz, the SNDR is about 3 dB lower. The plot of SNR versus input for a bandwidth of 1MHz is shown in Figure 6.9. Path mismatch due to non-linear capacitors was suppressed to 30 dB due to the bilinear configuration, and the measurements are shown in Figure 6.11. The noise at low frequency is flat because of the low opamp gain, not because of circuit noise.

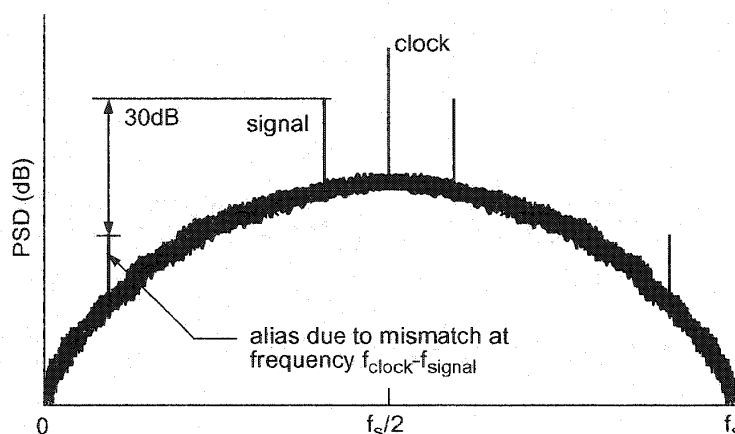


Figure 6.11 Path mismatch measurement

In the low power mode, the supply voltage V_{DD} was dropped to 0.9 V with $V_{DD} = V_{th,n} + V_{th,p} + 50\text{mV}$ where $V_{th,p}$ and $V_{th,n}$ are the threshold voltages for the PMOS and NMOS respectively. Figure 6.12 is the output power spectrum. The effective sampling frequency is 5 MHz, and a -14.5 dBm sinusoidal tone at 10 kHz is applied. The SNR is 51 dB (8 bits) for a bandwidth of 20 kHz, and the SNDR is 47 dB. The HD is more severe because the opamp is more non-linear as V_{DD} is lowered. The power dissipation is 40 μW . The SNR versus input power is shown in Figure 6.12.

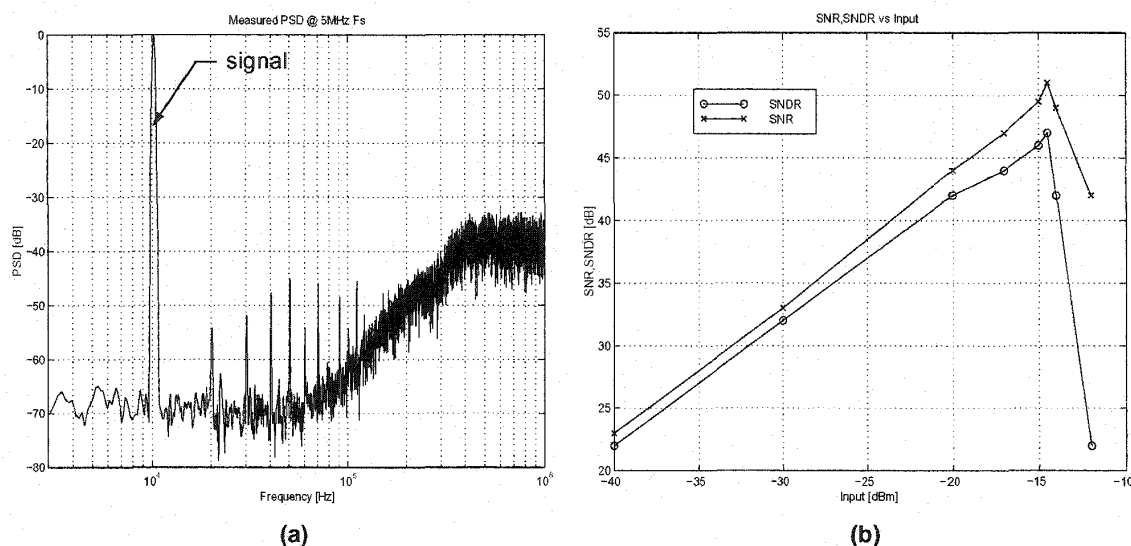


Figure 6.12 Low-power mode (a) power spectrum and (b) SNR/SNDR vs. input power at BW = 20 kHz

The chip was fabricated in a 0.25 μm triple-metal single-poly FDSOI CMOS process, and the chip area is 0.7mm by 0.6mm. The micrograph is shown in Figure 6.13.

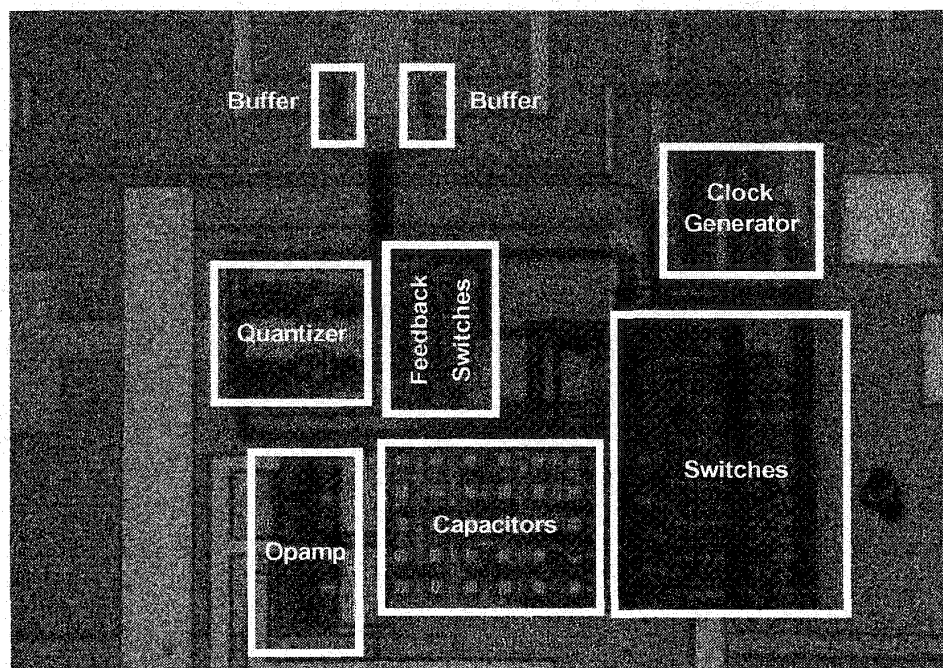


Figure 6.13 Micrograph of the 50 MHz second-order $\Delta\Sigma$ modulator

6.3 Low-Voltage High-Speed Multi-bit Quantizer

In this section, the design of a 1 V 3-bit pipelined ADC is described to demonstrate the low-voltage and high-speed capability of SOI for mixed-signal applications. The circuit consists of a novel digital logic circuitry called “complement-and-combine” to alleviate some adverse device limitations at low voltage. The design was verified by simulation. This ADC is designed for future radio bandpass $\Delta\Sigma$ ADC implementations as the multi-bit quantizer.

6.3.1 Radio Bandpass $\Delta\Sigma$ ADC

SOI transistors for both PMOS and NMOS have demonstrated their high-speed performance at low-voltage from both device and circuit measurements. Therefore, a 1-V GHz radio bandpass $\Delta\Sigma$ ADC as shown in Figure 6.14 is being considered for implementation.

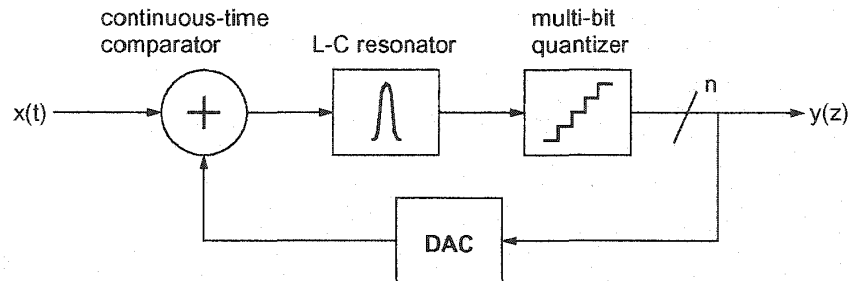


Figure 6.14 Proposed radio bandpass $\Delta\Sigma$ ADC

The system consists of four building blocks: a continuous-time comparator, a second-order resonator, a multi-bit quantizer and a digital-to-analog converter. The continuous-time comparator is to be realized by a g_m -C transconductance amplifier, for which the gain is controlled by the feedback current from the DAC. The bandpass filter is an L-C resonator using on-chip passive components as described in Chapter 3, and positive feedback circuits for Q -enhancement. The multi-bit quantizer is a pipelined ADC, and the DAC is an array of switching transconductance amplifiers. Details of the quantizer and DAC are discussed below.

6.3.2 Multi-bit Quantizer Specification

To achieve better resolution for a $\Delta\Sigma$ ADC, a multi-bit quantizer can be used instead of a single-bit quantizer [Nor97]. The quantization noise is lower by 6 dB for every additional bit, and the AWGN model is more accurate because the multi-bit quantizer is based on linear operation. Furthermore, the $\Delta\Sigma$ loop is easier to stabilize so that quantizer overload can be avoided. However, any non-linear error of the quantizer directly contributes to the modulator non-linearities, increasing harmonic distortions and reducing the dynamic range.

Before designing the circuit, performance specifications targeted for the future bandpass $\Delta\Sigma$ ADC were considered as follows:

1. sampling frequency: in order to realize the resonator using an on-chip inductor, the resonator must be operated in the low to middle GHz range. Next, $f_s/4^1$ is where the notch will be

placed, then for a resonant frequency of 1 GHz, the sampling frequency is 4 GHz. Therefore, the quantizer must be able to operate at this speed. A pipelined ADC using dynamic comparators [Cho95] was chosen due to its circuit simplicity for high-speed operation.

2. quantizer level: the next question is the number of bits for the quantizer. Since high speed up to 4 GHz is required, operational amplifier feedback circuits and hence many analog techniques are not applicable. Since dynamic comparators are used to compare the signal level against the reference voltage level, the quantizer level is limited by the 1 V voltage headroom (V_{DD}) and circuit noise. In this design, 8 quantization levels (3 bits) from 0.2 V to 0.8 V with a quantization step of 0.1 V were chosen. A 4-bit quantizer requires a quantization step of at least 62.5 mV, making the realization extremely difficult at high speeds because the threshold voltage is about 0.2 V.
3. signal encoding: digital representation $y(z)$ is important because this determines the design of the quantizer output and the DAC input. The two most commonly used codes are the binary code and the thermometer code as shown in Table 6.1. Clearly, the thermometer code is not as efficient as the binary code since, to represent 2^n digital signals, it requires $2^n - 1$ digits as opposed to n digits as required in binary code. However, thermometer coding has lower differential non-linearity error, guaranteed monotonicity and reduced glitching noise [Joh97], which are important in high speed DAC design. One of the most crucial reasons for using this coding is that the output of a pipelined ADC is inherently thermometer coded, so extra circuitry for binary code conversion is not required in the critical feedback path, making the high speed operation more probable. For the above reasons, the thermometer code was chosen for implementation.

In summary, a 3-bit thermometer coded ADC with f_s greater than 4 GHz using pipelined architecture is to be designed at 1 V V_{DD} .

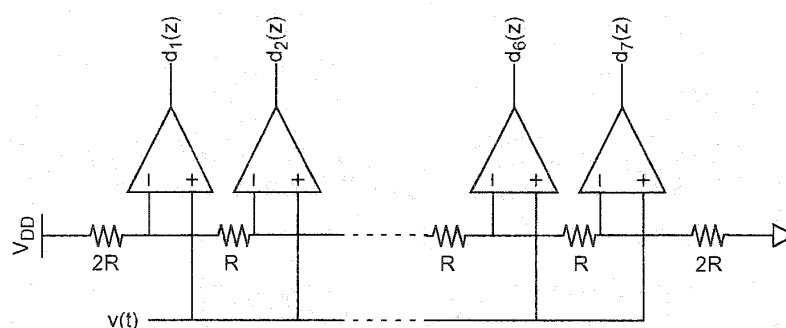
1. $f_s/4$ is a popular choice for easy transfer function realization. However, $3f_s/4$ can also be realizable if the sampling frequency is too high.

Table 6.1: 3-bit representation using binary and thermometer code

decimal	binary			thermometer code						
	b_1	b_2	b_3	d_1	d_2	d_3	d_4	d_5	d_6	d_7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

6.3.3 Quantizer Circuit Design with Dynamic Comparator

The 3-bit pipelined ADC has 7 comparators in parallel to perform signal level comparison. The general structure is shown in Figure 6.15. A resistor chain is used to provide the reference voltages, and the continuous input $v(t)$ is fed into all comparators simultaneously. The outputs $d_n(z)$ are thermometer coded because d_{i-1} must be on if d_i is on, where $i \in [1 \dots 7]$.

**Figure 6.15 3-bit pipelined ADC architecture**

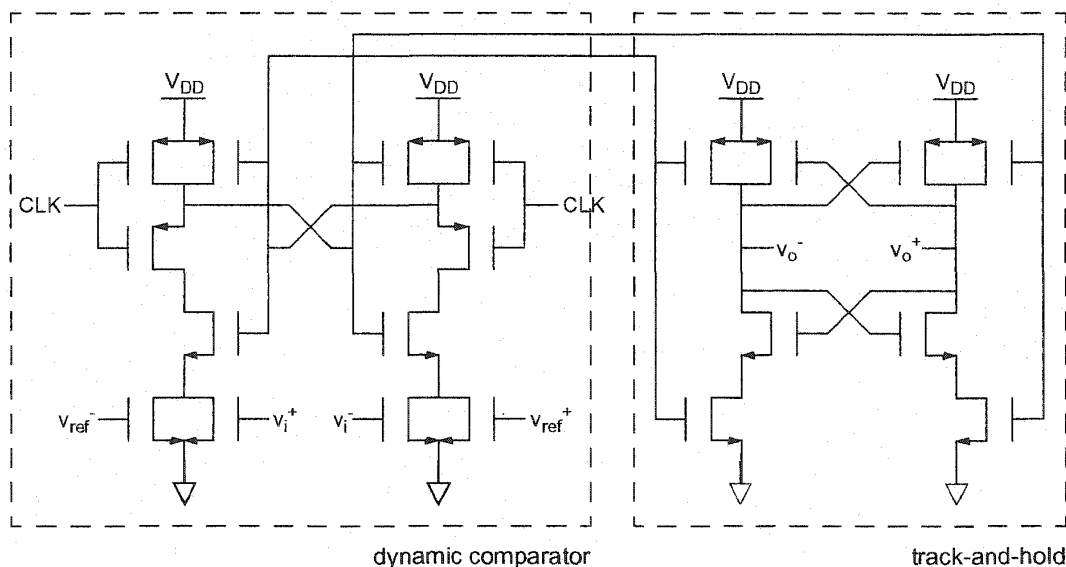


Figure 6.16 Schematic of dynamic comparator and track-and-hold circuit

To achieve high speed performance, each comparator as shown in Figure 6.15 is composed of a dynamic comparator [Cho95] followed by a track-and-hold circuit as shown in Figure 6.16. The inputs, v_i^+ and v_i^- , of this dynamic comparator are driven by NMOS transistors and they are paired with the reference voltages v_{ref}^- and v_{ref}^+ respectively. The sums of their currents are compared, and the latch on top of the input transistors pulls up or down accordingly. The latch is reset every clock cycle by the CLK signal at the frequency of f_s . Therefore, a comparator is followed by a track-and-hold circuit to hold the signal until a change is detected. The simulation results of this circuit are shown in Figure 6.17. In this simulation, it was assumed that the input signal has been sampled and held, so the input was fixed at a dc level which was set at the middle of the quantization step. The CLK signal is a square wave with f_s of 5 GHz, and the input is a square wave with amplitude between 0.15 to 0.85 V, with an f_{in} of 1.22GHz.

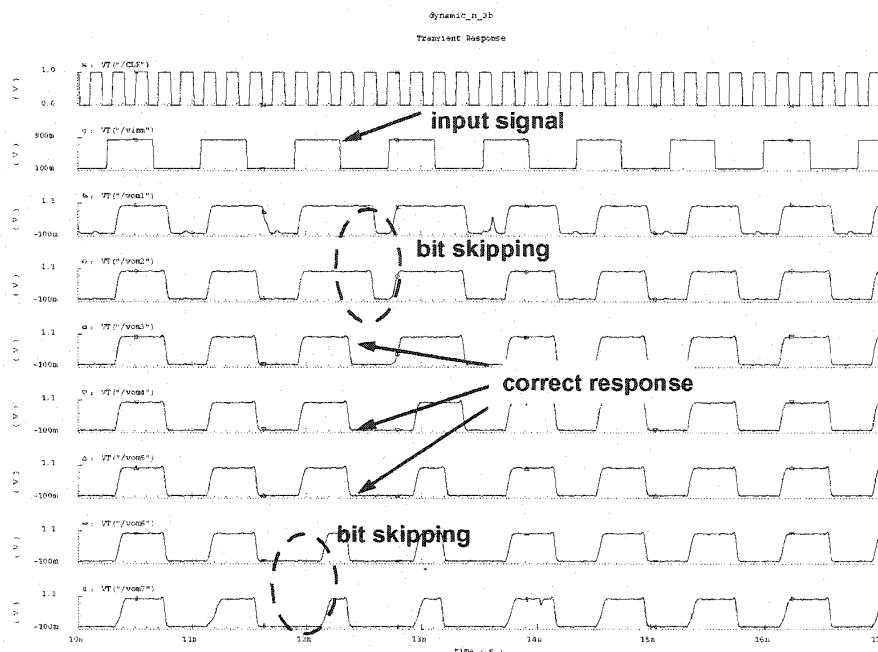


Figure 6.17 Simulation of dynamic comparator with track-and-hold circuit

At 5 GHz f_s , “bit skipping” was observed such that the correct bit representation was delayed by a clock cycle. This is because the NMOS drivers of each half-circuit of the comparator were operating in different regions: one in saturation ($v_{gs} = 0.8$), and the other one near the sub-threshold region ($v_{gs} = 0.2$ V), where the transistor has lower current driving capability and the speed is slower. Thus, the missing of a cycle was due to the slow response of the half-circuit. However, this problem can be amended by using a novel “complement-and-combine circuit”, which is described in the next section.

6.3.4 Complement-and-Combine Circuit

The slow response of the half circuit is due to the low v_{gs} (0.2 V) of the NMOS drivers. This problem can be alleviated by using the complement of the dynamic comparator with PMOS as the drivers. Nonetheless, the same problem persists at high v_{gs} (0.8 V) that makes the PMOS drivers operate in the sub-threshold region. One possible solution is to use PMOS drivers when v_{gs} is low (0.2 V), and use NMOS drivers when v_{gs} is high (0.8 V). The circuit block diagram is shown in Figure 6.18.

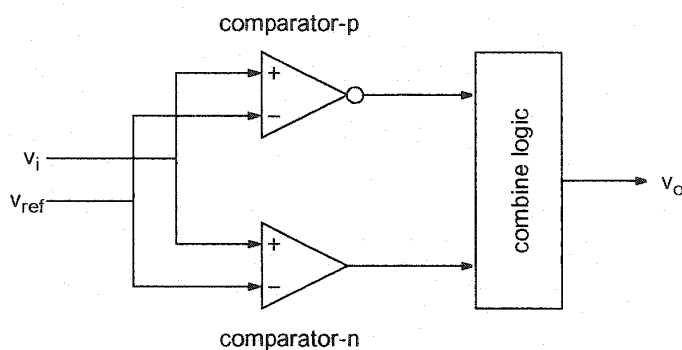


Figure 6.18 Complement-and-combine topology

The complement-and-combine topology consists of a comparator with NMOS drivers (Figure 6.16) called “comparator-n”, the complementary circuit¹ of the comparator-n which is made with PMOS drivers, called “comparator-p”, and a logic circuit that combines the outputs of the two comparators and selects the proper signal to output.

The combine logic was designed based on the assumption that the slow comparator is able to respond correctly within n clock cycles, where n is given by

$$n = f_s/f_{in} - 2 \quad (6.9)$$

1. complementing a circuit is achieved by interchanging PMOS and NMOS transistors, and interchanging V_{DD} and ground.

where f_{in} is the input frequency, and -2 comes from the fact that the digital logic requires one cycle to respond and one cycle for margin. Consider an example for bit skipping as shown in Figure 6.19. v_{in} is the sampled-and-held input signal at $f_s/4$ that swings between 0.15 and 0.85 V. This causes both p- and n- comparators with slow transistors (v_{ref} at 0.2 and 0.8 V) to switch output responses, which are $v_{o,p}$ and $v_{o,n}$ respectively. $v_{o,p}$ has the correct pull-up response but is slow in pulling down, while $v_{o,n}$ has the correct pull-down response but is slow in pulling up. Therefore, the selection criteria for the logic function is defined as “use $v_{o,p}$ for pull-up, and $v_{o,n}$ for pull-down”.

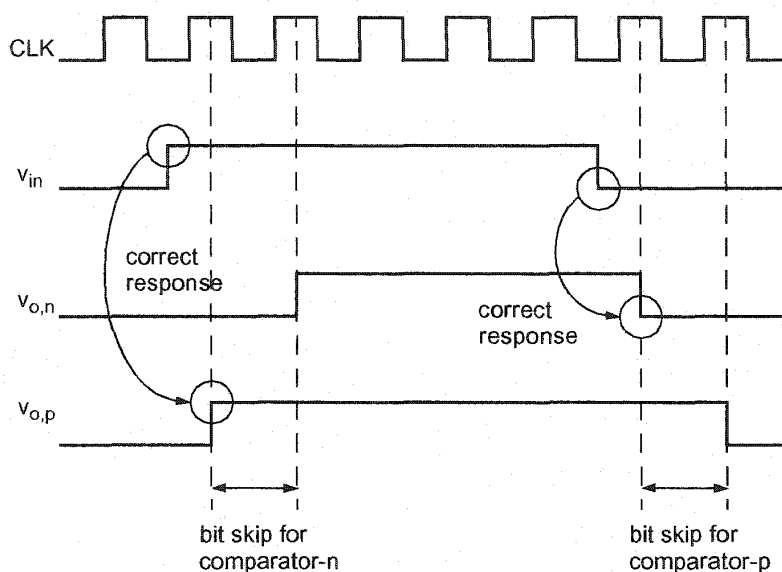


Figure 6.19 Bit skipping for comparator-n and comparator-p

This logic can be realized using a Mealy machine in 2 states. After some state diagrams and Karnaugh map analysis, the logic functions for the next state Q^+ is

$$Q^+ = UD + QD + QU \quad (6.10)$$

where U and D are the digital representations of $v_{o,p}$ and $v_{o,n}$ respectively, and Q is the present state variable. The output logic function O is:

$$O = UD + \bar{Q}U + \bar{Q}D \quad (6.11)$$

From (6.10) and (6.11), only one flip-flop and a few logic gates are required to construct the combined logic circuit. A dynamic flip-flop is used for its high speed performance, and static logic gates are used for the rest of the circuits.

The circuits were put together and simulated. The results are shown in Figure 6.20. Up to $5 \text{ GHz } f_s$ and $1.25 \text{ GHz } f_{in}$, the circuits function properly with no bit skipping observed. Hence, the functionality of complement-and-combine circuits was verified. Finally, the simulated power dissipation of the whole circuit is only 4 mW at $1 \text{ V } V_{DD}$.

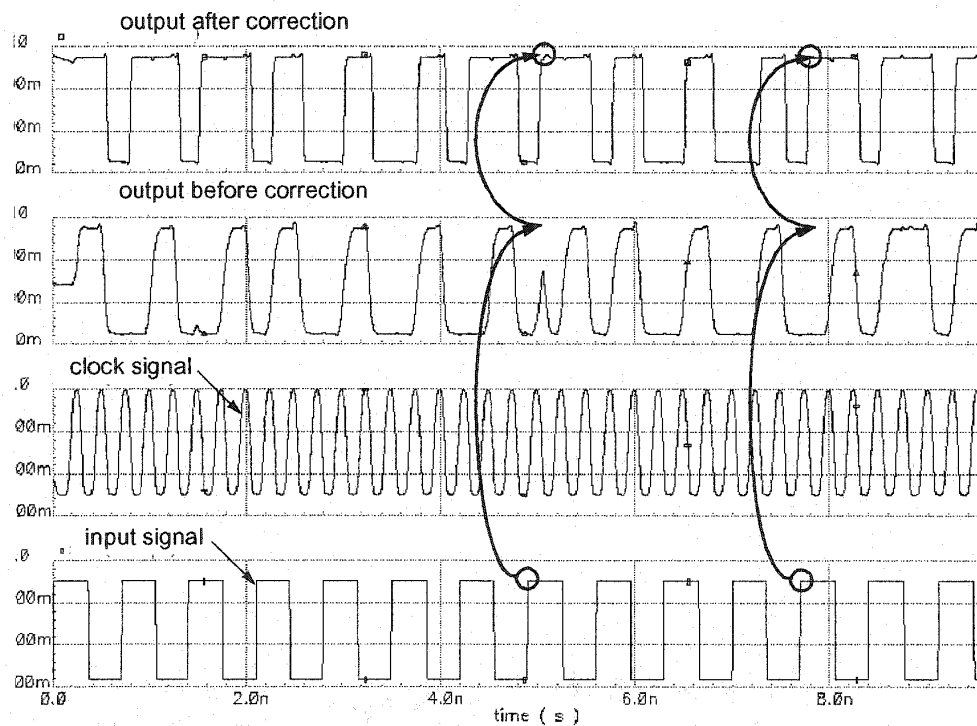


Figure 6.20 Simulation of ADC with complement-and-combine circuit

6.3.5 Current-Mode DAC

In this section, the design and simulation of a 3-bit current-mode DAC is discussed. This circuit serves two purposes: (a) provides a means of measuring the 3-bit pipelined ADC, and (b) serves as the DAC in the feedback path as shown in Figure 6.14 for future bandpass $\Delta\Sigma$ ADC implementation. A single-supply positive-output DAC as described in [Joh97] was used, and the schematic of the DAC is shown in Figure 6.21.

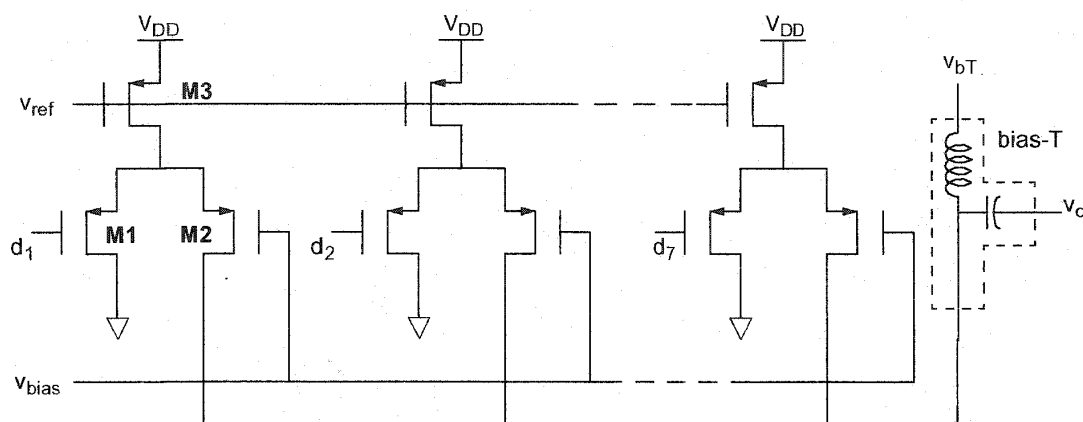


Figure 6.21 3-bit single-supply positive-output DAC with bias-T load

The inputs d_1 to d_7 are the 3-bit digital thermometer coded signals, v_{ref} is the reference voltage that determines the current for each branch, v_{bias} and v_{bT} are the dc biases for cascode transistor $M2$ and the bias-T, and v_o is the analog output voltage. The circuit works as follows. $M3$ behaves like a current source that provides constant current determined by v_{ref} , and d_n is the digital input that switches the transistor $M1$ on or off. When d_n is low, $M1$ is on and the current from $M3$ steers through $M1$ to ground, nulling the output current through $M2$. When d_n is high, $M1$ is off, $M2$ and $M3$ forms a cascode current source so that the current is delivered to the output. The output current of each branch are summed and delivered to the output load, which is an external bias-T in this case. The inductive choke of the bias-T provides a high ac impedance for measurement (see Section 4.9).

For measurement purpose, the ADC (Section 6.3.4) and the DAC are connected as shown in Figure 6.22. The accurate measurement of the ADC depends on the accuracy of the DAC. The rule of thumb is that if the DAC has 2 bits more accuracy¹ than the ADC, then it can be considered as an ideal element, 5 bits for the DAC in this case and the ADC is 3 bits. The accuracy of the DAC is mainly dependent on the mismatch of the current source $M3$ (Figure 6.21). For this technology, adjacent transistor mismatch is less than 1%, which corresponds to 6.6 bits of accuracy. Therefore, the DAC is considered as an ideal block in measurement.

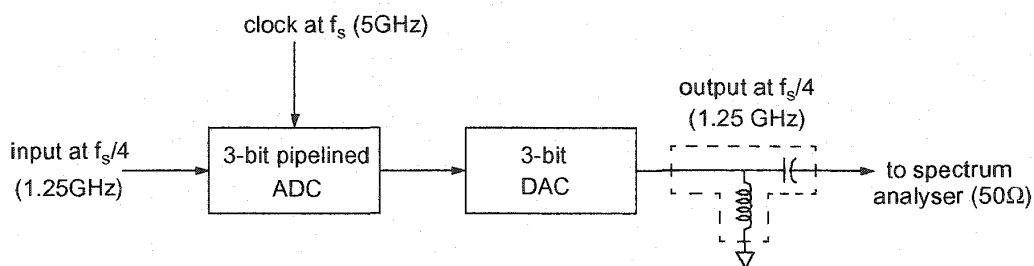


Figure 6.22 Proposed 3-bit pipelined ADC

For future radio bandpass $\Delta\Sigma$ ADC implementation, the current signal from the DAC can be fed back to control the gain transconductance amplifier through a current mirror as shown in Figure 6.23.

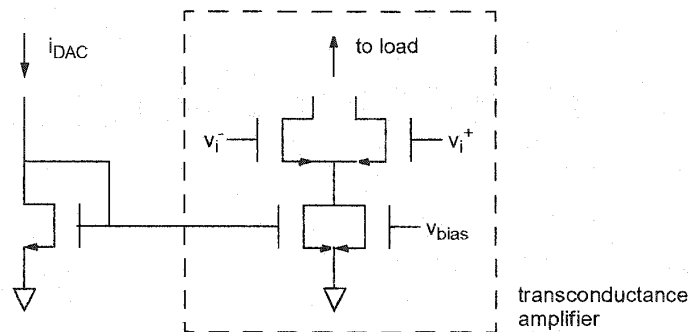


Figure 6.23 An example feedback circuit from DAC

1. : Note that resolution and accuracy are two different measurements

6.4 Summary

In this chapter, the basic theory of $\Delta\Sigma$ modulation is reviewed. Next, a 50 MHz second-order $\Delta\Sigma$ ADC was designed, implemented and measured. The performance of the ADC is listed in Table 6.2.

Table 6.2: $\Delta\Sigma$ ADC performance summary

mode	bandwidth	SNR/SNDR	power dissipation
nominal	1 MHz	36 dB/ 36 dB (6 bit)	300 mW
nominal	200 kHz	48 dB/ 48 dB (8 bit)	300 mW
low power	20 kHz	51 dB/ 47 dB (8 bit)	40 μ W

Next, the design of a high-speed low-voltage 3-bit pipelined ADC was presented, and this circuit serves as a multi-bit quantizer for future bandpass $\Delta\Sigma$ ADC implementations. At 4 GHz, the simulation shows “bit-skipping” so that the correct response was delayed by one clock cycle due to device speed limitation at low-voltage. Therefore, a novel circuitry called “complement-and-combine” was introduced to resolve the speed reduction, and operation up to 5 GHz with no bit-skipping was shown by simulation. The ADC incorporates a current-mode DAC for measurement. The simulated total current of the circuit is 4 mW.

Chapter 7 Conclusions and Future Work

7.1 Conclusions

The advancement in fabrication technology to deep submicron makes it feasible to implement RF function blocks in CMOS. This makes it possible to realize single-chip integration in CMOS-only technology instead of a more expensive BiCMOS technology. As a result of technology advancement in CMOS, SOI has also gained popularity because it is inherently better than bulk CMOS in high-speed low-power performance at low supply voltage.

This thesis presents the design, analysis, simulation and experimental verification of several benchmark RF circuits in SOI CMOS to demonstrate the strength and advantages of this technology. Taking advantage of the unique properties of SOI, several intuitive theoretical concepts and innovative design techniques were applied to resolve the bottlenecks in bulk technology and hence improve circuit performance. All the circuits in this thesis are the first reported implementation in SOI, and measured results show that these circuits clearly out-perform all other reported CMOS high-speed low-voltage low-power RF circuits.

In this thesis, the basic properties of the SOI transistors were first studied in Chapter 2. Capacitor models were introduced to gain an intuitive understanding of the device phenomena from the circuit point of view. The low-voltage high-speed performance of the 0.13 μm

technology used here for circuit design (e.g., 148 GHz f_T for NMOS transistor at 1 V operation) shows promise of these devices for RF applications.

In Chapter 3, high quality passive devices were examined and developed because they are crucial for high performance RF circuits. For inductors, a 0.85 nH horseshoe inductor with single-ended Q over 20 between 2 to 5 GHz was implemented. The high Q performance is mainly due to highly conductive copper metal, thick isolation between the inductor metal and the substrate, and small inductor area that minimizes substrate loss. This is the first report of a single-loop inductor in CMOS circuits, demonstrating the application and feasibility of the inductor in the 5 GHz range. As an aside, a 17 nH inductor was also designed for future application as an IF/RF choke. It has a Q above 5 between 0.6 to 3 GHz, and occupies an area of only 140 μm by 140 μm .

As for varactors, the operation principal of an AMOS varactor was analyzed. The figures of merit, namely $C_{\max}/C_{\min}$ ratio and Q , were defined. As well, the characteristic curves of the AMOS varactor were explained. Through the physical understanding of the device, the crucial factors that lead to high performance AMOS varactor were identified: (a) the reduced parasitic capacitance in SOI technology results in better $C_{\max}/C_{\min}$ than bulk, and (b) improved lithography leads to high Q . This hypothesis was verified with numerical device simulation. Finally, an AMOS varactor with $C_{\max}/C_{\min}$ of 6 and tuning voltage of ± 0.9 V with Q between 95 to 170 was designed and measured at 1 GHz.

With high quality inductors and varactors, several VCOs were designed and measured as described in Chapter 4. Simplified phase noise theory was reviewed, and new techniques for VCO design were developed, making use of both high performance active and passive devices. First, a low-voltage circuit technique called “simultaneous g_m and impedance matching” was developed to improve phase noise of the VCO, taking full advantage of the availability of deep submicron gate length transistors (0.13 μm in this case) [Fon02d]. Compared to conventional design methods, the application of this technique results in phase noise improvement of up to 8 dB without any VCO performance penalty.

Limited tuning range is one of the major bottlenecks in CMOS VCOs. However, the high C_{max}/C_{min} ratio measured in the SOI AMOS varactor suggested a possible solution to this problem. Therefore, low-voltage frequency tuning of the VCO was studied, and the relationship between phase noise and varactor gain (and hence frequency tuning range) was determined. In the analysis as well as in measurements, it was found that high varactor gain introduces excess noise into the VCO, degrading the phase noise significantly. To compensate this adverse effect, two novel approaches, band-switching [Fon02a] and differentially-tuned topologies [Fon02b], were used to reduce the undesirable effects of high varactor gain, while maintaining the frequency tuning range.

Band-switching topology uses a bank of digitally-controlled switching capacitors to select the frequency band of operation, and a small tuning varactor to control the VCO to oscillate at the desired frequency. Through frequency band selection, the frequency tuning range is maintained, while the excess phase noise is reduced by tuning a smaller varactor. The implemented band-switching VCO achieves a wide tuning range up to 58.7% with ± 0.7 V tuning voltage using three varactors, demonstrating the wide tuning capability of the SOI AMOS varactor. Furthermore, it was observed that a three times smaller varactor gain results in phase noise improvement up to 7 dB, illustrating the concept of excess phase noise reduction through band-switching topology.

Next, the differentially-tuned varactor was examined, and a simple but novel theory for low-frequency common-mode noise rejection was developed. This new theory clearly points out the advantage of differential tuning as compared to conventional single-ended tuning, and the theory was verified by experimental measurement. Moreover, the advantage of using SOI as compared to bulk technology was explained. By using differential tuning, the VCO was able to operate at 1 V, 4.4 GHz centre frequency with a 40% tuning range. If the voltage supply is reduced to 0.75 V, the power dissipation is only 0.8 mW at 5.7 GHz. This is the first sub-1V sub-mW CMOS VCO reported at this frequency.

In order to evaluate the performance limit of the SOI transistor and the AMOS varactor, a 40 GHz VCO was implemented. A complementary VCO topology, using both PMOS and NMOS latches, was employed to study the feasibility of PMOS transistors in SOI at this speed. This is

crucial because additional phase noise improvement techniques can be applied if PMOS transistors are available. A number of design considerations regarding frequency tuning were identified, and they were employed to construct the first CMOS VCO with a record frequency tuning range up to 15% [Fon02c]. The area of the circuit is only 100 μm by 100 μm . Finally, in order to measure high-speed low-voltage circuits (e.g., the 40 GHz VCO) accurately, a bias-T source follower was introduced. The advantage was explained and verified by measurement in Section 4.9.

To illustrate that SOI technology is the best technology option for low voltage RF system integration in a single chip, several high frequency circuits were designed or implemented. In Chapter 5, LNAs were designed with the “simultaneous power and matching” technique, utilizing the advantage of high-speed transistors in deep submicron technology. Then, in Chapter 6, high-speed low-voltage mixed-signal and analog issues were studied. As switched-C is one of the most important circuit techniques used in mixed signal, a 50 MHz $\Delta\Sigma$ ADC [Swa99] was measured to evaluate the low-voltage low-power analog and switched-C performance in SOI. Measured results demonstrated circuit operation down to 0.9 V, drawing only 40 μW with 6-bit performance. Next, the low-voltage high-speed capability in mixed-signal circuits was studied. A 1 V 5 GHz 3-bit pipelined ADC was designed and simulated, and it was found that circuit performance was limited due to transistor speed degradation at low voltage. To resolve the problem, a new circuit technique “complement-and-combine” was introduced to improved the circuit performance, and the concept was verified by simulation.

In summary, the key for building high performance RF integrated circuits is high speed transistors and good quality passives. The 0.13 μm SOI CMOS technology provides transistors which have both f_T and f_{max} above 100 GHz for NMOS devices, and above 60 GHz for PMOS devices. Inductors with Q greater than 20 and varactors with Q above 95 were designed in this technology. Several high-speed low-voltage circuits (VCO, LNA and ADC) were designed, simulated and measured. Besides the speed advantage, the superiority of SOI over bulk technology was demonstrated from the measured performance of the varactor and the VCOs. Furthermore, measured data also shows the high speed, low voltage and low power capability of

SOI, and therefore it is concluded that SOI should be considered as a prime technology for single-chip RF system integration.

7.2 Future Work

- **Measurement**

Several circuits were submitted for fabrication and still need to be measured when the chips return. The circuits include the 5.4 GHz LNA with all-passive zero-dc-power image rejection (Section 5.7), the 1 V 5 GHz 3-bit pipeline ADC (Section 6.3), and several transformer [Lon00b] designs that are not described in this thesis. Similar to the inductors, the transformers are to be characterized for the technology component library.

- **5 GHz bandpass $\Delta\Sigma$ ADC**

As described in Section 6.3.1, the high-speed pipelined ADC is designed as a multi-bit quantizer for a high-speed bandpass $\Delta\Sigma$ ADC. Resonant circuits will be used as the continuous-time loop filter, taking advantage of the high Q inductors and widely tunable varactors. If this circuit is successfully implemented, the architecture of the receiver front-end will be simplified enormously. The measured LNA, VCO and ADC are to be integrated together to construct a 5 GHz RF front-end receiver.

- **40 GHz phase-locked loop**

In this thesis, a 40 GHz VCO with a tuning range up to 15% was designed and measured. Since complementary topology was used for the VCO, this suggested PMOS latches can operate at a speed above 40 GHz. This suggests the possibility of implementing gigabit communication circuits such as clock and data recovery circuit using the SOI technology.

7.3 Technology Trend

- **Which technology will win the battle, bulk or SOI?**

RF CMOS is driven by the enormous demand from the CMOS digital market. Within the digital market, a large portion of the pie goes to personal computers chip sets, which are dominated by the commercial giants such as Intel, AMD and IBM. Conventionally, the advantages of bulk over SOI is technology cost and maturity. However, as the lithography continues to improve to 0.08 μm and below, the substrate capacitance of the bulk device imposes the major limitation to transistor speed and power dissipation, while SOI still enjoys the advantage of reduced capacitance due to the body oxide, taking full advantage of lithography down-scaling. For these reasons, Intel and AMD have announced that they will switch from bulk technology to SOI for their next generation computer processors¹, while IBM has already employed SOI in production for their Power PC series. The technology switching to SOI will significantly lower the wafer cost, and the technology has been (or has to be) qualified due the strong demand for commercial production.

Therefore, it is predicted that SOI will become the dominant technology over bulk CMOS, at least in the high-speed low-voltage low-power category.

- **Integrated optical circuit in SOI**

Despite recent economic trends, fibre optics remains the only viable choice for tera-bit telecommunication systems. Using the body oxide as the bottom boundary as shown in Figure 7.1, optical rib waveguides have been implemented successfully on SOI substrates. If a suitable detector for the 1.3 to 1.5 μm light used in optical telecommunication can be integrated with SOI², optical and electronic circuit integration in a single chip may become a possibility. For example, an optical receiver could have de-multiplexed certain wavelength down to 100 GHz for

1. Intel announced it plans to use Tera Hertz SOI CMOS transistors for the next generation microprocessor between the year 2005 to 2010 (www.intel.com/research/silicon/micron.htm).

2. One possible solution is to use SiGe based PIN diode for light detection.

electronic processing. Since the NMOS transistors have both f_t and f_{max} greater than 100 GHz¹, the signal, in theory, can be de-multiplexed by 4, and processed digitally at 25 GHz.

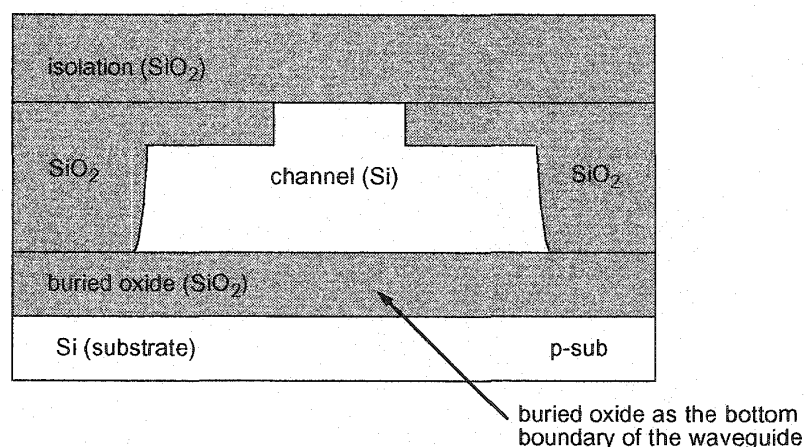


Figure 7.1 Integrated rib waveguide in SOI

- **To infinity, and beyond**

Besides high-speed low-voltage capability for communication and digital applications such as RF systems and microprocessors, the extra buried oxide of SOI enables additional applications not possible in bulk devices. An exciting application of SOI is single electron transistor (SET) based microelectronics for high-density low-power information processing and memory applications. One of the keys for SET circuit is that the body silicon layer has to be extremely thin to minimize charge leakage. The successful fabrication of ultra thin silicon film down to 1 nm demonstrates that one monolayer of silicon is achievable in SOI technology [Ern99], which makes SET technology a promising field in the future.

Another interesting field for SOI is three-dimensional integration circuit (3D-IC), in which multiple layers of active silicon are vertically stacked and interconnected using the SOI

1. The IBM 0.12 μm SOI NMOS transistor has a measured $f_T > 200$ GHz.

fabrication technology [Sar99]. The most significant advantages of 3D-IC are that chip area is reduced to increase circuit density, and distance between circuits is shortened to improve interconnect delay. Fabrication difficulty is the major stumbling block, at least for the moment, preventing deep submicron technology from being integrated in 3D-IC. However, with technology advancement, it is possible to have deep submicron transistors at the bottom layer, and low thermal-budget transistors at the upper levels as shown in Figure 7.2. For example, memory circuits can be placed on the top levels and fast digital processor on the base layer.

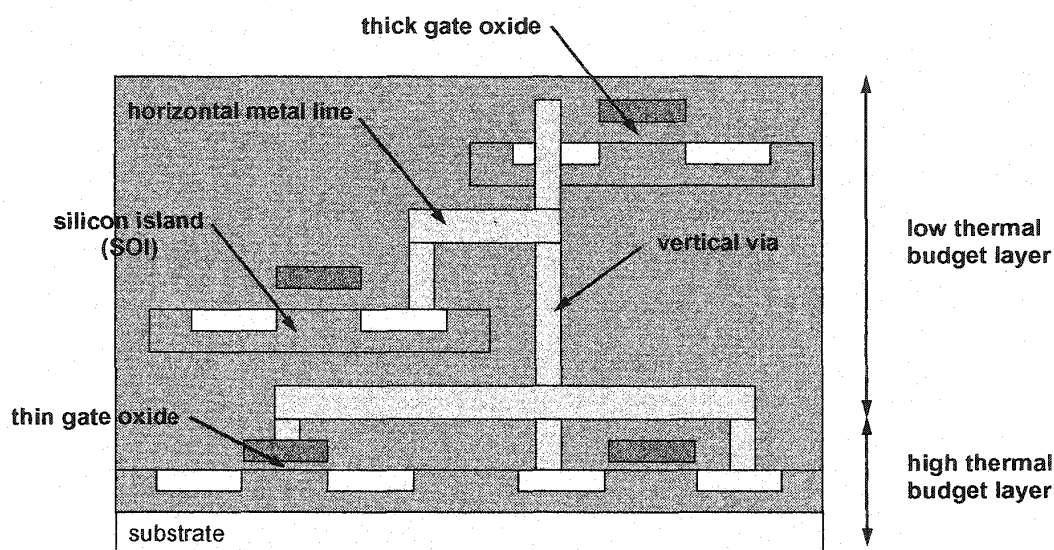


Figure 7.2 3D-IC transistor and metal layers

There are many other applications of the buried oxide. For example, it reduces substrate parasitic capacitance for lateral bipolar transistors¹, serves as the isolation layer for high-resistivity substrate fabrication or silicon micro-machining² in the substrate, and SiGe implementation in the channel. All these wide possibilities have made SOI an exciting technology to keep an eye on.

1. A 0.7 μm Lateral Diffused MOSFET has a measured f_T and f_{max} above 10 GHz for high-speed and ultra-low-power analog applications.
2. This can be used for application such as fabrication of hollow inductors.

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Exhibit 1006

Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO

by Matthew Muh

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

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Professor Ali M. Niknejad
Research Advisor

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* * * * *

Professor Tsu-Jae King
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1 Introduction

The downscaling of CMOS technology over the past several decades has resulted in continual improvements in integrated-circuit performance and cost per function. However, the scaling of conventional CMOS devices significantly beyond the 90-nm technology node will be challenging, due to limitations such as subthreshold leakage and gate-dielectric leakage. To overcome some of the problems associated with planar CMOS device scaling, advanced MOSFET structures such as the ultrathin-body SOI single-gate transistor and the double-gate transistor have been explored. These structures enable more aggressive device scaling because of their ability to control short-channel effects more effectively. Compared to a single-gate ultrathin-body device, the double-gate device is more electrostatically robust because two gates are used to control the channel, thus allowing for additional gate length scaling.¹ Although double-gate transistors have been studied for quite some time, their adoption has been hindered by the complexity of their fabrication process. Recently, however, a more practical double-gate structure, the FinFET, was developed, with a process flow similar to that of conventional SOI CMOS processes.² A number of functional FinFET digital circuits have been reported, and physical design conversion of planar CMOS circuits to FinFET technology has been demonstrated.³

The improvement in circuit performance from continued device scaling applies to RF circuits as well as digital circuits. The improved RF performance of CMOS devices has enabled CMOS to become a viable option for commercial RF applications such as wireless LAN, GSM cellular transceivers, and GPS receivers. Recently, 7 GHz of unlicensed bandwidth around 60 GHz was made available, opening the door for applications such as Gb/s point-to-point links, short-range

high data-rate wireless personal area networks, and vehicular radar.⁴ Technology scaling has enabled CMOS devices to operate at these high frequencies, and numerous millimeter-wave CMOS circuits have been reported in the literature. Compared to the traditional III-V semiconductor technologies used for monolithic microwave integrated circuits, CMOS implementations promise higher levels of integration and reduced cost,⁴ and thus may begin to make inroads into the compound semiconductor-dominated market in the foreseeable future. Future CMOS implementations of millimeter-wave integrated circuits may potentially utilize advanced, highly scalable structures such as the FinFET to take advantage of their increased speed.

To facilitate an initial evaluation of the RF capability of FinFET technology, a 2:1 static frequency divider has been designed using FinFETs, as documented in the second section of this report. In addition to the frequency divider, individual FinFETs have been designed to enable DC and high-frequency S-parameter transistor measurements and to evaluate the effect of layout variations on FinFET performance. The third section of this report documents the design of a CMOS push-push VCO for millimeter-wave applications. Using a balanced architecture, the push-push VCO is designed to operate at a fundamental frequency of 30 GHz while generating a single-ended second-harmonic output at 60 GHz. The VCO is estimated to deliver -3 dBm of output power at 60 GHz into a $50\text{-}\Omega$ load while consuming about 20 mA of DC current from a 1.2-V supply.

This work was sponsored by SPAWAR (FinFET circuit design) and by DARPA (millimeter-wave Si-based circuits).

2 Application of FinFET technology to high-frequency circuit design

2.1 Introduction to FinFET technology and applications

The FinFET is a double-gate transistor in which the gate straddles a thin, vertical fin-shaped body, creating two channels along the sidewalls of the fin (Fig. 2-1). Using two gates and a thin body helps to control short-channel effects, thereby enabling gate-length scaling deep into the nanometer regime without the use of channel dopants. Although it may be possible to scale the traditional bulk MOSFET into the 10-nm gate length regime, this will probably require heavy channel doping to mitigate short channel effects. This not only presents a challenge in terms of device fabrication, but will probably also result in the degradation of device performance.¹

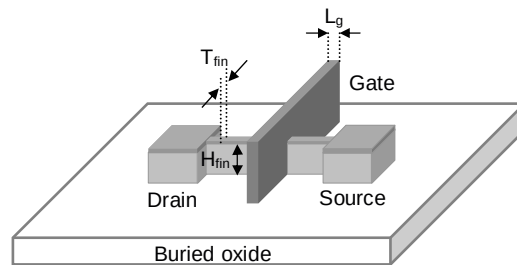


Figure 2-1. Simplified schematic diagram of FinFET.

The ability of double-gate devices to more effectively control short-channel effects and thereby limit the leakage current makes them particularly attractive for low-power digital applications. With a lightly doped channel, double-gate devices have a steep subthreshold slope, which translates to a lower threshold voltage for a given off-state leakage current specification, thus increasing the on-state drive current. In terms of fabricated FinFETs, promising results have

been reported in the literature. For example, symmetric double-gate (SDG) FinFETs with raised source/drain were fabricated with the highest drive current reported for double-gate NMOS and PMOS devices; this current was also competitive with (then) state-of-the-art bulk silicon and SOI technologies.⁵ A comparison of reported conventional FETs and FinFETs showed that high-performance FinFETs already met or exceeded the best conventional FET performance for a given gate length, in terms of CV/I delay, despite the youth of this technology.⁶

A number of functional digital FinFET circuits have been reported in the literature, including a four-stage inverter chain,⁷ a six-transistor SRAM cell,⁸ and a 41-stage ring oscillator.⁹ To date, there has not yet been much published work on FinFETs for analog/RF applications. However, the first detailed experimental investigation of the analog performance of FinFETs was recently published, in which the authors reported very high values of the Early voltage and hence, of intrinsic gain.¹⁰ While this is promising for analog applications, the authors also observed that drive currents and transconductance were lagging behind the best planar devices. They believe that performance can be improved by improving the mobility in the side channels and/or increasing the fin density.

The primary aim of this present research is to investigate the suitability of FinFETs for RF applications. To this end, a number of test structures have been designed in order to enable an initial evaluation of the high-frequency performance of FinFETs. Specifically, a static frequency divider has been designed to benchmark the potential speed of FinFET technology in a circuit application. In addition, individual test transistors have been designed for S-parameter measurements, which will facilitate high-frequency transistor characterization and modeling in the future.

2.2 High-frequency transistor performance and design

An important figure of merit for the high-frequency capability of a technology is the maximum frequency of oscillation (f_{MAX}). The f_{MAX} of a transistor can be determined by finding the frequency at which Mason's unilateral power gain (U) or the maximum available power gain (MAG) is equal to unity. Although f_{MAX} is related to the unity current gain frequency (f_T) of the device, it is also highly dependent on the resistive losses of the device, including the gate resistance, series source/drain resistances, non-quasi-static channel resistance, and the resistive substrate network.⁴ Thus, while f_T can be increased simply by scaling down the device, f_{MAX} may not exhibit a corresponding improvement unless the influence of parasitics is appropriately minimized.

To reduce the gate resistance of a conventional CMOS transistor, the width of each finger in a multi-finger transistor should be made very narrow. Although the gate finger width affects the gate resistance and hence f_{MAX} , it has been observed that f_{MAX} is independent of the actual number of fingers of the transistor.¹¹ The layouts of a representative bulk-CMOS transistor and a FinFET are compared in Fig. 2-2. It can be seen that the FinFET can utilize a similar multi-finger layout to reduce the width of each gate finger and thereby reduce the overall gate resistance. The gate resistance can also be reduced by using a material with a lower resistivity than polysilicon. This approach lends itself nicely to FinFETs, since gate work function engineering using alternative gate materials can be used to achieve threshold voltage adjustments when the body is undoped. For example, a molybdenum gate technology has recently been developed for FinFET technology.¹²

One of the technological challenges facing FinFETs is the high parasitic source/drain series resistance arising in part from the thin fin extension between the gate edge and the source/drain

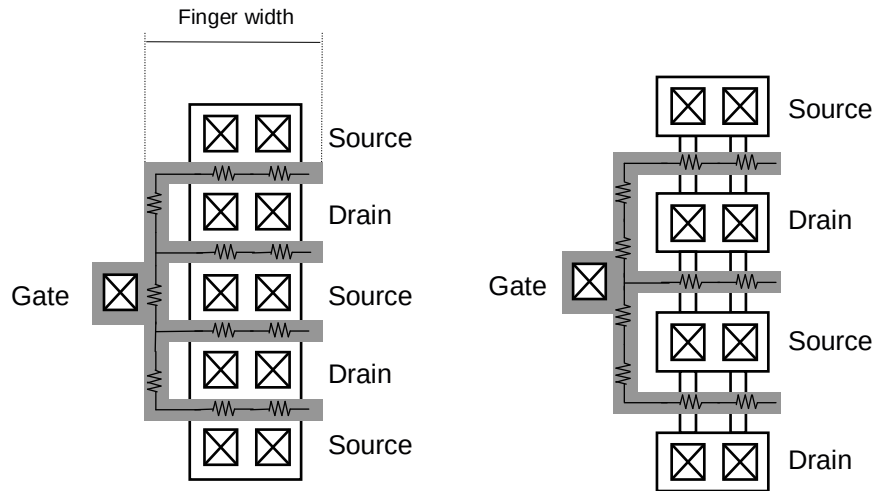


Figure 2-2. Layout of multi-finger bulk-CMOS transistor (left) and FinFET (right).

pads. This reduces not only the drive current but also f_{MAX} of the device. Different methods—angled extension implants and selective silicon epitaxy—have been investigated to minimize this parasitic resistance in FinFETs.¹³

Various definitions of gain for an n-channel FinFET are plotted in Fig. 2-3. The plots are based on a simple BSIM3SOI transistor model adapted from a preliminary BSIM3SOI SPICE model developed at SPAWAR.¹⁴ No AC data was available at the time this version of the model was developed, so the capacitance parameters are estimated, but not calibrated. H_{21} is the current gain and MSG is the maximum stable gain. The effective width of the device is 1 μm , the gate length is 60 nm, and the bias conditions are $I_d/W = 165 \mu\text{A}/\mu\text{m}$ and $V_{ds} = 1.2 \text{ V}$. As the plot shows, the value of f_{MAX} is roughly 100 GHz, which is much lower than one would expect for a typical sub-100-nm device with comparable biasing. For example, the f_{MAX} of a properly laid-out and biased NMOS transistor in a standard 130-nm CMOS technology can easily exceed 100 GHz,⁴ while the f_{MAX} of an NMOS device in a 90-nm SOI CMOS technology can exceed 200

GHz.¹⁵ The low f_{MAX} of the FinFET is perhaps due in part to high parasitic source/drain resistance and suboptimal RF layout. In addition, it should be noted that the model does not incorporate gate resistance or the effect of various other parasitics, so the actual value of f_{MAX} may be even lower. A more accurate high-frequency model, based on measured C-V or S-parameter data and perhaps utilizing a double-gate SOI transistor model, would yield more accurate results.

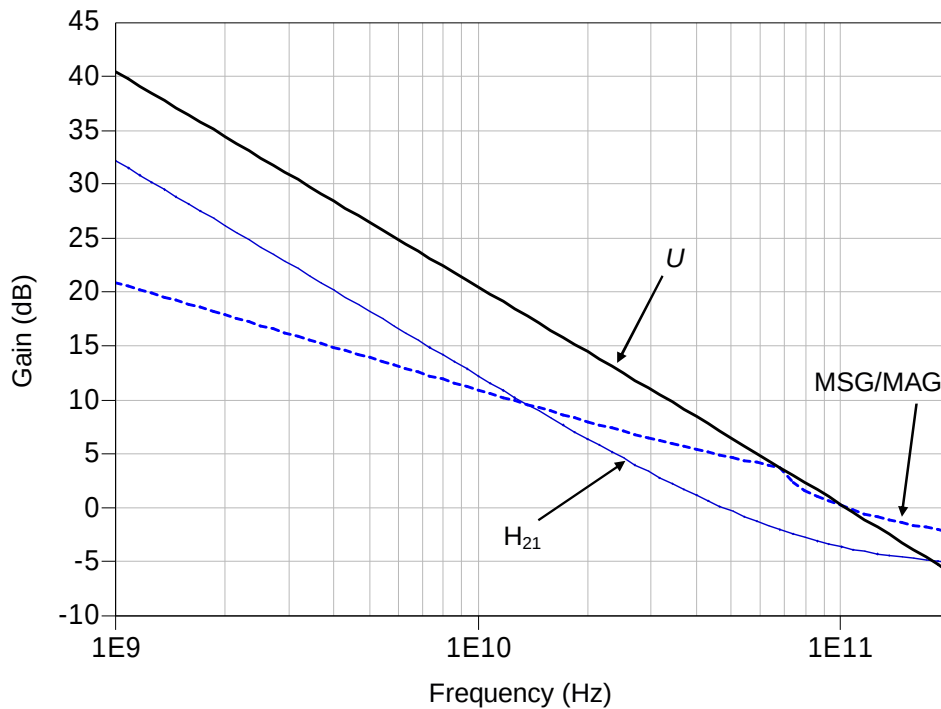


Figure 2-3. Gain plots for n-channel FinFET (W/L = 1 μm /0.06 μm).

2.3 Small-signal transistor modeling

A simple small-signal transistor model of a FinFET based on results from device-level simulations has been developed. A lumped-element small-signal model is useful because of its simplicity and relatively high accuracy, although numerous RF circuits, such as mixers and VCOs, require an accurate large-signal model. A small-signal model is further limited by its

dependence on bias conditions and the specific region of a transistor's operation. Although the model presented here was not used in designing the frequency divider described later, it nonetheless sketches how a basic small-signal model could be developed from measured data.

A simple lumped-element, small-signal equivalent MOSFET model is shown in Fig. 2-4. It includes both the intrinsic transistor and parasitic series resistors. Based on this model, a simple technique is used to extract the model parameters. This technique was developed to extract a high frequency model based only on S-parameter measurements and is described in a paper by Lovelace *et al.*¹⁶ The model shown here is the same as that presented in the aforementioned reference, except that it does not include the additional time-constant factor associated with g_m . Instead of using measured data, a sample FinFET (adapted from a model provided by Hei Kam) was simulated using a 3-D device simulator, resulting in a set of two-port matrix parameters. The FinFET has an effective width of 0.1 μm and a gate length of 65 nm, and was biased at $V_{GS} = 1.5\text{ V}$ and $V_{DS} = 1\text{ V}$. The extraction technique is summarized as follows, omitting the mathematical details:

- Initially bias the device at $V_{GS} = V_{DS} = 0\text{ V}$ and use the resulting zero-bias Z-parameters to extract the parasitic resistances r_g , r_d , and r_s .
- Select the desired bias condition and calculate the resulting Z-parameter network ($\mathbf{Z}$).
- Compute the Z-parameter network of the intrinsic model ($\mathbf{Z}'$) by subtracting the appropriate parasitic resistances from $\mathbf{Z}$.
- Convert $\mathbf{Z}'$ to the equivalent Y-parameter network ($\mathbf{Y}'$).
- From $\mathbf{Y}'$, calculate the parameters of the intrinsic small-signal model— C_{gd} , C_{gs} , C_{ds} , r_{ds} , and g_m .

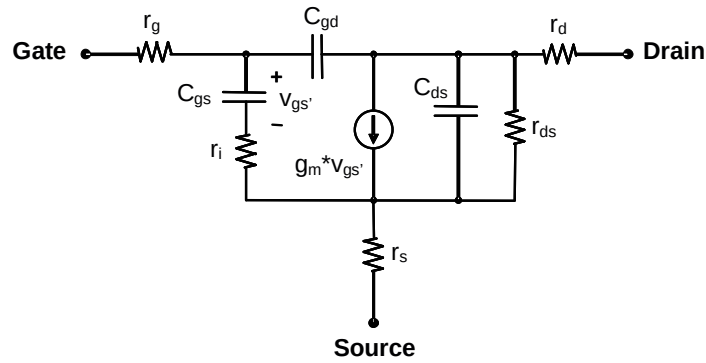


Figure 2-4. Small-signal transistor model.

Parameter	Value	Parameter	Value
r_g	80 Ω	C_{gs}	104 aF
r_d	210 Ω	C_{gd}	22 aF
r_s	160 Ω	C_{ds}	2 aF
r_i	1 k Ω	g_m	160 μS
r_{ds}	140 k Ω		

Table 2-1. Extracted small-signal model parameters.

Using this extraction routine, the small-signal model parameters of the FinFET were obtained (see Table 2-1), and the resulting model was compared to the simulated results, as shown in Fig. 2-5. Except for Y21 at very high frequencies, the plots show very good agreement, which is expected since the FinFET is modeled by a simple, well-behaved structure in the device simulator and various layout parasitics are not included. In practice, the small-signal model must take into account all the relevant layout parasitics, which require additional elements to model. A more sophisticated small-signal model and extraction scheme can be utilized for a better fit, such as the SOI MOSFET model and extraction method presented in the paper by Raskin *et al.*,¹⁷ which take into account the effect of parasitic inductances.

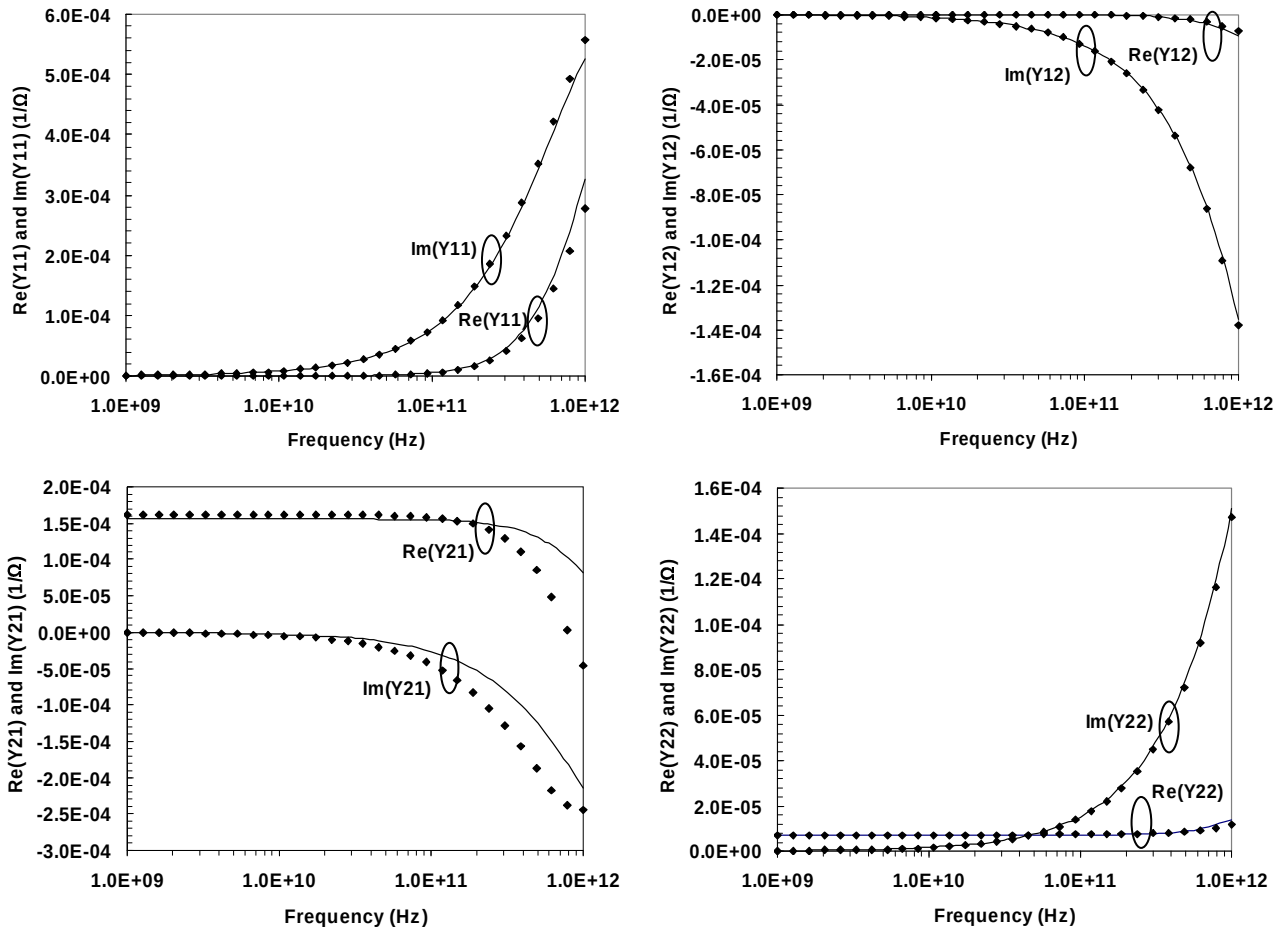


Figure 2-5. Simulated results vs. extracted small-signal model (dots: simulation, solid line: extracted model).

2.4 Design of static frequency divider and other test structures

2.4.1 Process information and FinFET orientation

The test structures are to be fabricated on SOI wafers with a targeted fin height, H_{fin} , of 50 nm. The effective width of a single-fin device is 100 nm (twice the fin height due to the two channels). The gate oxide is expected to be about 20 Å thick. The minimum gate length is 35 nm, and the fin thickness is targeted to be about 20 nm. This process incorporates a molybdenum gate

technology to adjust the gate work function. Up to two metal layers are allowed, although some layouts were routed with only one metal layer to ease fabrication requirements.

In a standard $\langle 100 \rangle$ wafer, the FinFET channel is oriented in the $\langle 110 \rangle$ plane. Although this orientation is good for PMOS devices due to high hole mobility in the $\langle 110 \rangle$ plane, NMOS devices should be oriented at a 45° angle to take advantage of higher electron mobility in the $\langle 100 \rangle$ plane. Because the FinFET is a vertical device structure, different surface orientations can be achieved by simply rotating the layout in the plane of the wafer, without the use of non-standard wafer substrates.¹⁸ Since the frequency dividers designed in this work utilize only NMOS devices, a number of layouts are rotated by 45° to evaluate NMOS FinFET performance enhancement due to improved electron mobility.

2.4.2 Individual transistors

A set of individual transistors with corresponding de-embedding structures has been designed. This set comprises NMOS FinFETs with different gate finger lengths, layout configurations, channel lengths, and orientations. The layouts of two of these transistors are shown in Fig. 2-6. Both devices have 600 fins, which is equivalent to a total width of $600 \times 100 \text{ nm} = 60 \text{ }\mu\text{m}$, and a targeted gate length of 50 nm. The transistor on the top is oriented horizontally with each doubly-contacted gate finger running across three fins. The transistor on the bottom is oriented vertically with each gate finger running across six fins. The use of ground-signal-ground pads and coplanar waveguides leading to the transistor facilitates high-frequency S-parameter characterization. A set of open, short, and thru de-embedding structures is shown in Fig. 2-7.

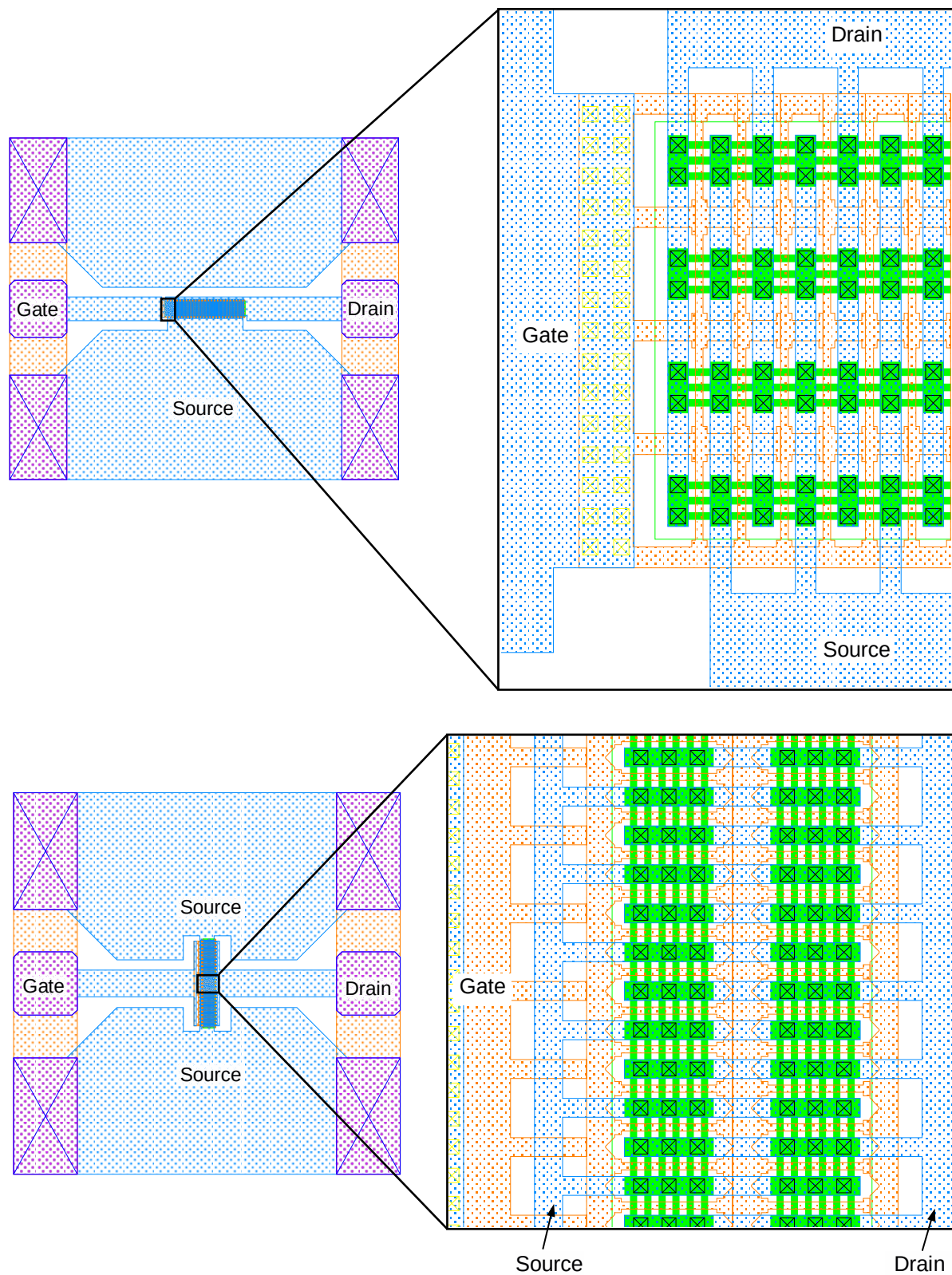


Figure 2-6. Layout of NMOS FinFETs with different orientations and gate finger lengths.

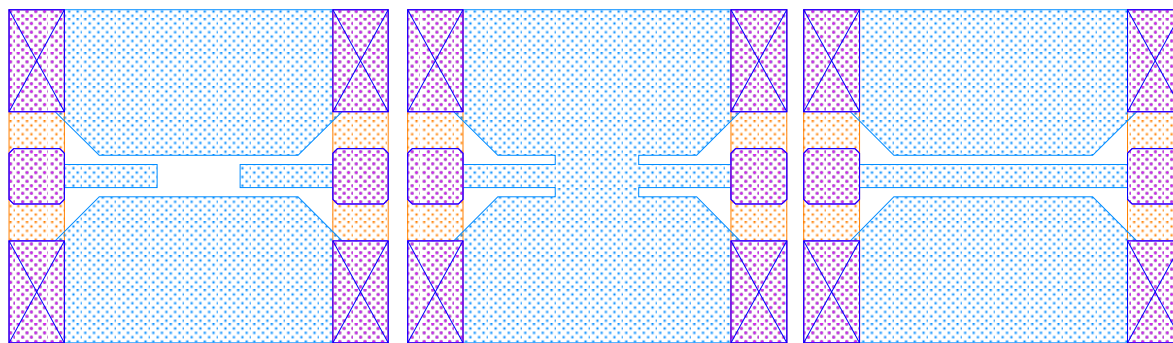


Figure 2-7. Open, short, and thru de-embedding structures.

2.4.3 Static frequency divider

2.4.3.1 Topology

A static frequency divider has been designed in order to evaluate the high-frequency capability of FinFET-based circuits. A frequency divider is an integral component of frequency synthesizers used in communication systems and also serves as a benchmark for high-speed technologies. As shown in Fig. 2-8, a static frequency divider can be implemented with two D-latches in a master-slave configuration. The inverted slave outputs are connected to the master inputs to perform a divide-by-two function on the clock signal. This circuit is a suitable test vehicle because it is fairly robust in the presence of process variations and is able to operate at a maximum frequency that is related to the intrinsic speed of the technology.

As shown in Fig. 2-9, each latch is implemented with a conventional current-mode logic (CML) architecture. Compared to conventional static CMOS logic, CML reduces the internal voltage swing, making it particularly suitable for high-speed operation.¹⁹ To maximize the speed of the circuit, only NMOS devices are used. Due to the lack of well-controlled resistors

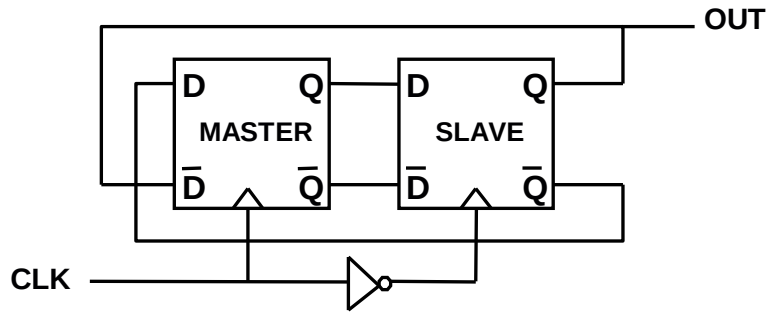


Figure 2-8. Static frequency divider block diagram.

in the process, diode-connected NMOS devices are used as active loads, although PMOS devices could also have been used. Instead of generating complementary clock signals for the two latches, a single clock signal is used in a quasi-differential fashion by swinging it above and below a fixed bias voltage (BIAS1). This clocking scheme is possible because the circuit operates in a fully differential manner. An external bias tee can be used to bring in the DC bias on the clock line. A simple common-source output buffer is used to isolate the frequency divider core and to present a low output impedance to the 50- Ω load.

The transistors are designed with the following widths: 14.4 μm (M1, M4–M5, M10, M13–M14, M23), 19.2 μm (M2–M3, M6–M7, M11–M12, M15–M16, M19–M22), and 9.6 μm (M8–M9, M17–M18). Numerous versions of the frequency divider were designed, with a targeted gate length of either 50 nm or 35 nm (0.3 μm or 0.285 μm drawn length). A simple current mirror is used to bias both the divider and the output buffer, and can be controlled externally by the BIAS2 pad. The nominal DC bias voltage on the clock input and BIAS1 is 700 mV.

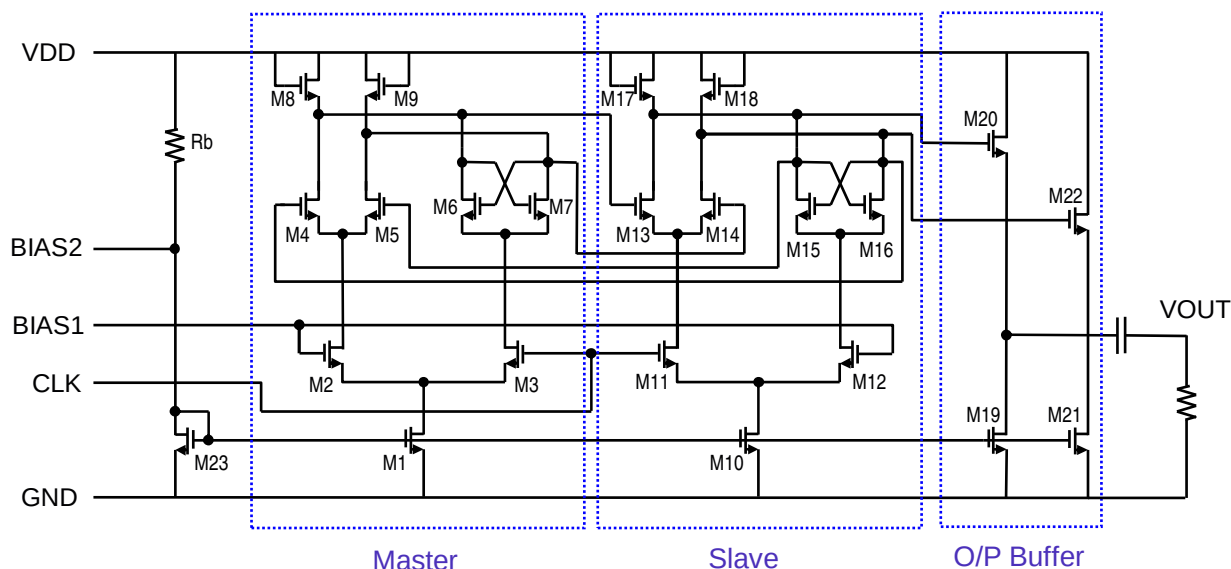


Figure 2-9. Simplified circuit schematic of CML static frequency divider with output buffer.

2.4.3.2 Estimated performance

Due to the lack of a better large-signal model, a simple behavioral (AHDL) FinFET transistor model²⁰ with lumped parasitic capacitances was used to run circuit-level simulations of the frequency divider. Since this behavioral description is based upon only a small set of parameters fitted to simulated transistor data, it is not expected to yield highly precise results. Nevertheless, it provides a starting point for the design of the FinFET frequency divider. Ultimately, a more accurate model will require measured data from fabricated FinFETs.

Simulations indicate that the frequency divider should be able to operate slightly above 35 GHz. A two-metal layer version of the frequency divider is expected to have better performance due to the reduced capacitance between the metal routing and the active devices. A

plot of the clock and output signals is shown in Fig. 2-10 for an input frequency of 37 GHz. Note that the plotted clock signal is the signal on the clock line, not the actual input signal, which comes from a 50- Ω sinusoidal voltage source with an amplitude of 340 mV. The power consumption of the core divider, including the current source, is estimated to be roughly 10 mW, while the power consumption of the output buffer is about 9 mW. The nominal supply voltage is 1.2 V.

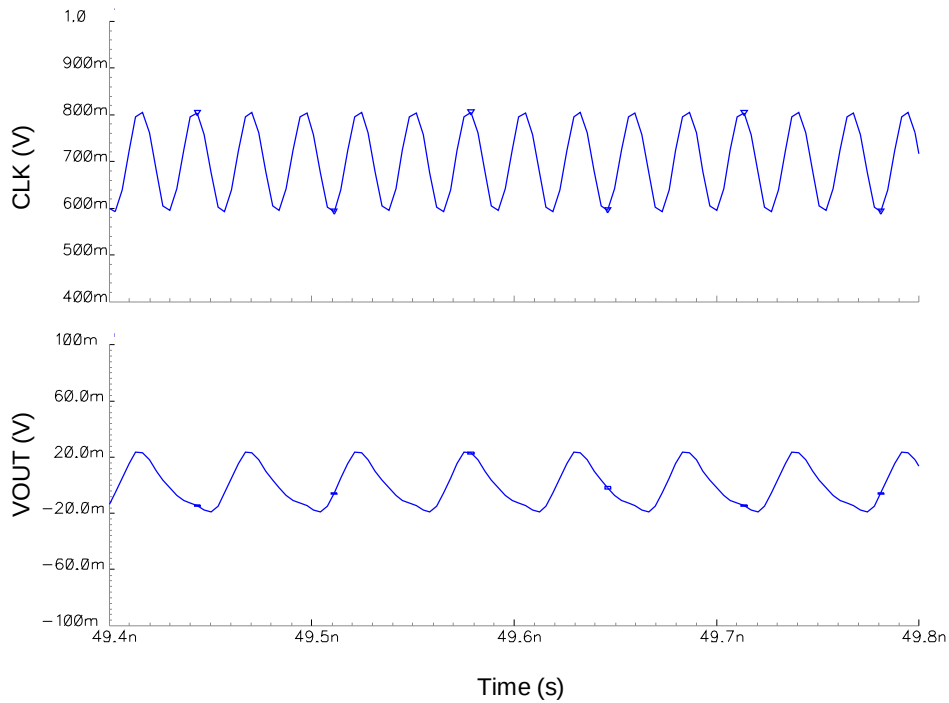


Figure 2-10. Simulated clock and output waveforms of frequency divider.

2.4.3.3 Layout

A high level of symmetry is maintained in the layout to preserve the differential operation of the circuit. Bypass capacitors are implemented using the FinFET gate oxide. Nine different versions of the frequency divider have been laid out, two of which are shown in Figs. 2-11 and 2-12. One of these utilizes two metal layers for routing, while the other uses only one layer. Of the

nine different versions, one has a target gate length of 50 nm, while the other versions have a target gate length of 35 nm. Four are unrotated, while the rest are rotated by 45 degrees. Other variations include added symmetry through the addition of a dummy output buffer, and different sizing and placement of the bypass capacitors. A description of the various frequency dividers and of the individual FinFET structures can found in Appendix A. The input and output probe pads are designed in a ground-signal-ground configuration to allow coplanar probing.

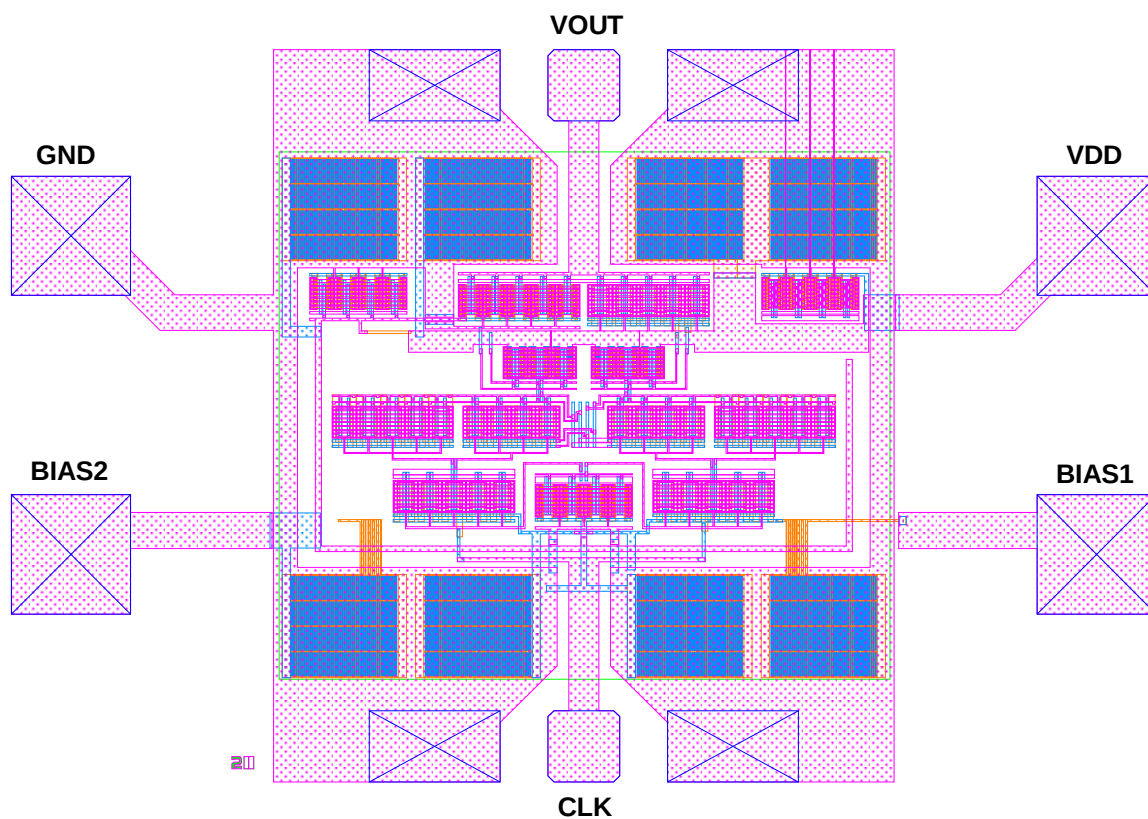


Figure 2-11. Layout of an unrotated two-metal layer version of the frequency divider.