

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Advanced Micro Devices, Inc.,
Petitioner,

v.

Realtek Semiconductor Corporation,
Patent Owner

IPR2023-00788

PETITION FOR INTER PARTES REVIEW

OF

U.S. PATENT NO. 9,590,582 B2

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PETITIONER'S EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 9,950,582
1002	File History of U.S. Patent No. 9,590,582
1003	Declaration of Dr. Paul Prucnal
1004	Curriculum Vitae of Dr. Paul Prucnal
1005	J. Gonzalez et al., <i>A 56-GHz LC-Tank VCO With 17% Tuning Range in 65-nm Bulk CMOS for Wireless HDMI</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 58, Issue 5 (May 2010), available at https://ieeexplore.ieee.org/document/5438827
1006	Matthew Muh, Master of Science thesis entitled <i>Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO</i> , Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley (2005), available at https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=7337593a3bdb909b1f7d53da1c3202a61401fac7
1007	A. Niknejad et al., <i>mm-Wave Silicon Technology 60 GHz and Beyond</i> (Springer Science + Business Media 2008) (excerpts)

Exhibit No.	Description
1008	S. Biswal, <i>Basic Electronics Volume I</i> (Atlantic Publishers 2001) (excerpts)
1009	A. Niknejad & R. Meyer, <i>Design, Simulation and Applications of Inductors and Transformers for Si RF ICs</i> (Springer Science+Business Media 2000) (excerpts)
1010	A. Niknejad, <i>Electromagnetics for High-Speed Analog and Digital Communication Circuits</i> (Cambridge Univ. Press 2007) (excerpts)
1011	Joachim N. Burghartz, <i>Spiral Inductors on Silicon – Status and Trends (Invited Article)</i> , International Journal of RF and Microwave Computer-Aided Engineering, V. 8, No. 6, 422-432 (Nov. 1998), available at https://onlinelibrary.wiley.com/doi/abs/10.1002/%28SICI%291099-047X%28199811%298%3A6%3C422%3A%3AAID-MMCE3%3E3.0.CO%3B2-K
1012	O.H. Murphy et al., <i>Design of Multiple-Metal Stacked Inductors Incorporating an Extended Physical Model</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 53, No. 6, 2063-2072 (June 2005), available at https://ieeexplore.ieee.org/document/1440724

Exhibit No.	Description
1013	U.S. Patent No. 6,885,275 filed on Jan. 28, 2000, titled “Multi-track Integrated Spiral Inductor” to James Chang (“Chang”)
1014	U.S. Patent Application Pub. No. US 2008/0074229 published on Mar. 27, 2008 by Shahriar Moinian et al. (“Moinian”)
1015	Bryant Derand Williamson, Masters Thesis entitled <i>A 2.4 GHz LC-VCO Using On-Chip Inductors and Accumulation- Mode Varactors in a CMOS 0.18 μm Process</i>, University of Tennessee – Knoxville, Aug. 2005, available at https://trace.tennessee.edu/utk_gradthes/2537/ Axel Dominique Berny, PhD Dissertation entitled <i>Analysis and Design of Wideband LC VCOs</i>, Electrical Engineering and Computer Sciences, University Of California, Berkeley, Spring 2006, available at https://www2.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-50.pdf
1016	Axel Dominique Berny, PhD Dissertation entitled <i>Analysis and Design of Wideband LC VCOs</i>, Electrical Engineering and Computer Sciences, University Of California, Berkeley, Spring 2006, available at https://www2.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-50.pdf

Exhibit No.	Description
1017	A. Kral et al., <i>RF-CMOS Oscillators with Switched Tuning</i> , IEEE Custom Integrated Circuits Conference, May 14, 1998 available at https://ieeexplore.ieee.org/document/695039
1018	Fei Yuan, <i>CMOS Active Inductors and Transformers Principle, Implementation, and Applications</i> , (Springer Science+Business Media, LLC 2008) ISBN 978-0-387-76477-1, available at https://link.springer.com/book/10.1007/978-0-387-76479-5
1019	Thomas H. Lee et al., <i>RF Passive IC Components</i> in book entitled <i>Circuits and Filters Handbook</i> , 2d Ed. (CRC Press LLC 2003), available at http://www.kelm.ftn.uns.ac.rs/literatura/ekui/Circuits_and_Filters_Handbook_CH10.pdf
1020	Agilent Technologies, <i>Overview on interdigital capacitor design</i> , 2001, available at https://www.keysight.com/us/en/assets/7018-08093/technical-overviews-archived/5989-8912.pdf
1021	Sang Wook Park, PhD Dissertation entitled <i>Oscillator Architectures And Enhanced Frequency Synthesizer</i> , Texas A&M University (Dec. 2009) (“Park”), available at https://core.ac.uk/download/pdf/13643134.pdf

Exhibit No.	Description
1022	Changhua Cao et al., <i>Millimeter-Wave Voltage-Controlled Oscillators in 0.13-um CMOS Technology</i> , IEEE Journal of Solid-State Circuits, Vol. 41, Issue 6 (June 2006) (“Cao”), available at https://ieeexplore.ieee.org/document/1637594
1023	Yue Wu et al., <i>A Temperature Stabilized CMOS VCO for Zero-IF Cellular CDMA Receivers</i> , Digest of Technical Papers, 2005 Symposium on VLSI Circuits, June 16-18, 2005 (“Wu”), available at https://ieeexplore.ieee.org/document/1469413
1024	Dorra Mellouli et al., <i>Design and Implementation of A 6-GHz Array of Four Differential VCOs Coupled Through a Resistive Network</i> , Analog Integrated Circuits and Signal Processing, Vol. 76, pp. 179-193 (2013) (“Mellouli”), available at https://link.springer.com/article/10.1007/s10470-013-0099-6#citeas
1025	Xiao Shimao et al., <i>A novel 2.95–3.65 GHz CMOS LC-VCO using tuning curve compensation</i> , Journal of Semiconductors, Vol. 30, No. 10, 105001 (Oct. 2009) (“Xiao”), available at https://iopscience.iop.org/article/10.1088/1674-4926/30/10/105001/pdf

Exhibit No.	Description
1026	Mohammad Nariman et al., <i>A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS</i>, 2010 IEEE Radio Frequency Integrated Circuits Symposium, May 23-25, 2010, pp. 157-160 (“Nariman”), available at https://ieeexplore.ieee.org/document/5477323
1027	Neric H. W. Fong, PhD Dissertation entitled <i>Low-Voltage Radio-Frequency CMOS Integrated Circuits in Silicon-On-Insulator</i>, Department of Electronics, Carleton University, Ottawa, Canada (May 23, 2002) (“Fong”), available at https://curve.carleton.ca/system/files/etd/63d93fb2-a8cc-4f63-865e-fba751da4fa1/etd_pdf/02a5d5d8788c5ea3b03555a6557ea59c/fong-lowvoltagefrequencycmosintegratedcircuits.pdf
1028	Babak Soltanian et al., <i>An Ultra Compact Differentially Tuned 6 GHz CMOS LC VCO with Dynamic Common-Mode Feedback</i>, IEEE 2006 Custom Integrated Circuits Conference, Sept. 10-13, 2006 (“Soltanian”), available at https://ieeexplore.ieee.org/document/4115046

Exhibit No.	Description
1029	V. Macaitis et al., <i>Design of a 4.48-5.89 GHz LC-VCO in nm RF CMOS Technology</i> , Elektronika IR Elektrotechnika, Vol. 20, No. 2, 44-47 (Feb. 5, 2014) (“Macaitis”), available at https://eejournal.ktu.lt/index.php/elt/article/view/6383
1030	Judith Maget, <i>Varactors and Inductors for Integrated RF Circuits in Standard MOS Technologies</i> , Institute of Electronics at the University of Bundeswehr (2002) (“Maget”), available at http://athene-forschung.unibw.de/doc/85282/85282.pdf .
1031	Paolo Lucchi, PhD Dissertation entitled <i>Frequency generation for mm-Wave and satellite applications</i> , University of Bordeaux (Feb. 2012) (“Lucchi”), available at https://www.theses.fr/2012BOR14479.pdf
1032	U.S. Patent Publication No. 2009/0322447 (“Daley”)
1033	U.S. Patent No. 9,270,247 (“Jing”)
1034	Realtek Infringement Chart for U.S. Patent No. 9,950,582
1035	Printout from www.m-w.com (Merriam-Webster Online Dictionary) (“substantial”)
1036	Declaration of Sylvia D. Hall-Ellis, Ph.D.

Exhibit No.	Description
1037	Curriculum Vitae of Sylvia D. Hall-Ellis, Ph.D
1038	Website Printout Regarding Gonzalez (EX-1005) accessed at: https://ieeexplore.ieee.org/abstract/document/5135585/figures#figures
1039	Website Printout Regarding IEEE Transactions on Microwave Theory and Techniques, accessed at: https://ieeexplore.ieee.org/abstract/document/5135585/figures#figures

I. MANDATORY NOTICES

A. Real Party-in-Interest

The real party-in interest is Advanced Micro Devices, Inc. (“AMD” or “Petitioner”).

B. Related Matters

U.S. Patent Nos. 9,590,582 (“the 582 patent”), 7,936,245, and 8,006,218 (collectively, “the asserted patents”) have been asserted by Realtek Semiconductor Corporation (“Realtek” or “PO”) in the case *Realtek Semiconductor Corp. v. Advanced Micro Devices, Inc.*, Case No. 4:22-cv-04769-JSW (N.D. Cal.), filed on August 19, 2022 (“the N.D. Cal. Case”). On December 12, 2022, Realtek filed a complaint with the International Trade Commission identifying the asserted patents as allegedly being infringed by AMD. The ITC instituted an investigation on January 19, 2023, captioned *Certain Integrated Circuits, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1350 (“the ITC Investigation”). The ITC Investigation is proceeding. AMD filed a motion to stay the N.D. Cal. Case pursuant to 28 U.S.C. § 1659, which mandates a stay of district court proceedings when there is a parallel ITC investigation pending. That motion is pending, although Realtek has informed the district court it does not oppose the motion.

C. Lead and Back-up Counsel and Service Information

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Petitioner consents to email service at: AMD-IPR@winston.com.

II. GROUNDS FOR STANDING

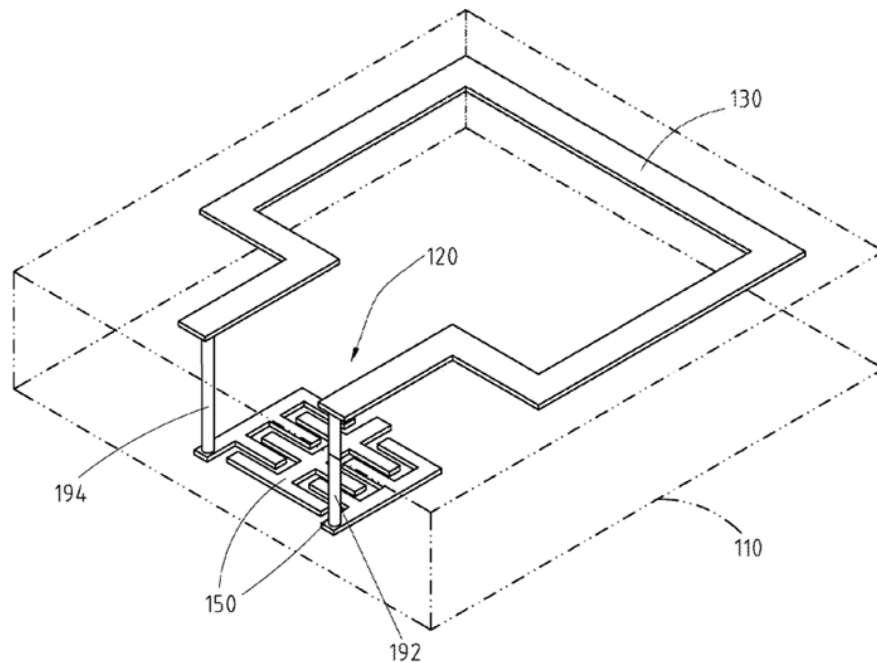
Petitioner certifies that the 582 patent is available for IPR and that Petitioner is not barred or estopped from requesting review challenging the claims on the identified grounds.

III. INTRODUCTION

The 582 patent, which claims priority to an application filed April 16, 2014, is directed to an “inductor-capacitor resonant circuit.” EX-1001, Title. These circuits (called “LC resonant circuits” or “LC tanks”) have been known for decades. The LC circuit oscillates at a particular frequency (the resonant frequency), and energy may be stored up in the capacitor. LC resonant circuits were therefore used to generate signals at a particular frequency, such as in radio

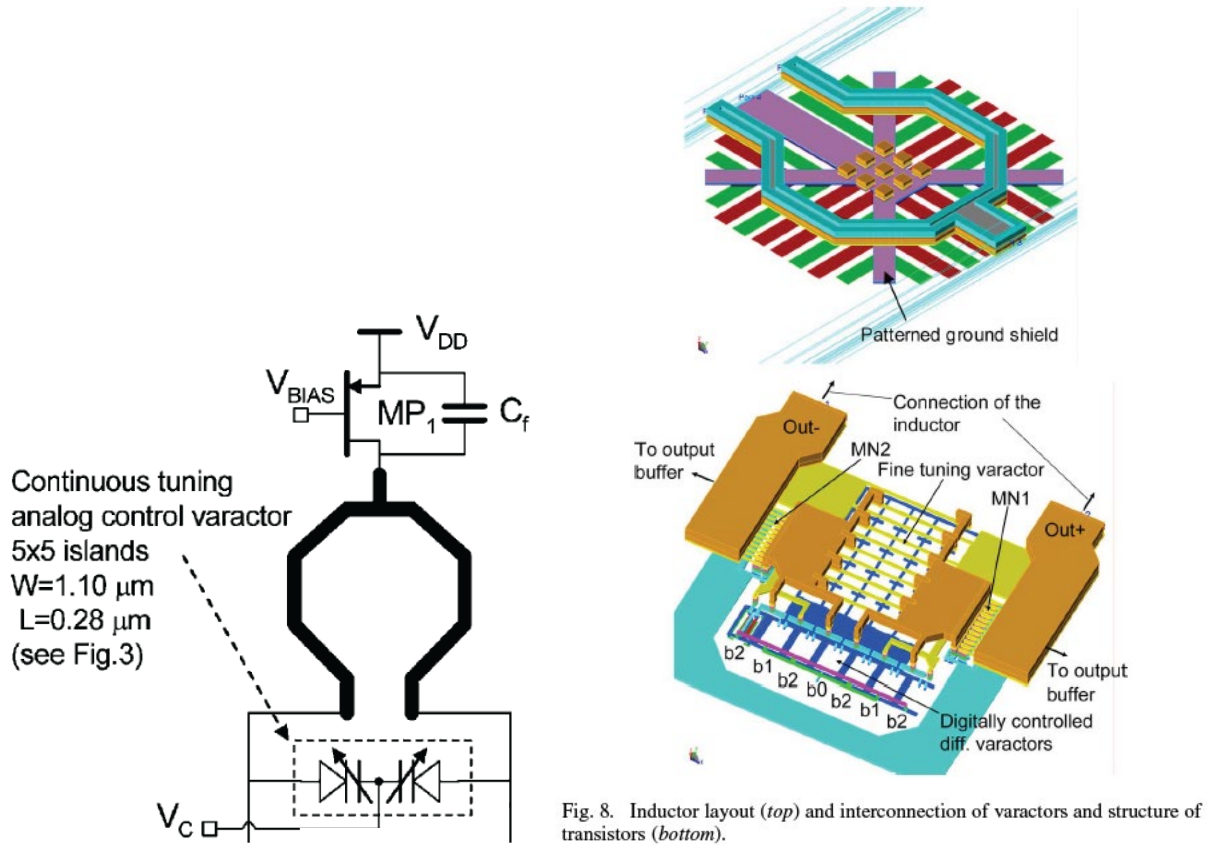
frequency (RF) chips. The 582 patent admits this. EX-1001 [1:33-36]. *See* EX-1003, ¶¶ 81-89.

The 582 patent thus proposes a specific LC circuit design in a multi-layer integrated circuit where the capacitor is offset from the inductor and on a lower surface. *Id.*, [3:48-55) (“The capacitor component 150 is arranged ... on the other surface (that is a lower surface of the first insulation layer 110), opposite to the inductor component 130...”). *See* Fig. 4:



582 Patent, Fig. 4 (EX-1001)

By 2014 such arrangements were already well-known. For example, Gonzalez (EX-1005), publicly available in 2009, describes an LC-Tank VCO (voltage-controlled oscillator) with the same inductor-capacitor arrangement as in the 582 patent:



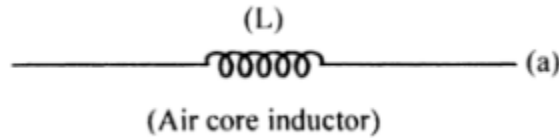
Gonzalez, Figs. 1 (partial) and 8 (EX-1005)

Other references also disclose this well-known concept. AMD respectfully requests that the Board institute trial and cancel the challenged claims as unpatentable.

IV. BACKGROUND OF THE TECHNOLOGY

A. Inductor Basics

Inductors (“L”) are common electrical components that store energy in the form of a magnetic field. Biswal, EX-1008:¹



Biswal, Inductor (EX-1008.014)

A straight wire bent into a coil possesses inductance which is known as the self-inductance of the coil. *Id.* This inductance is used to resist the flow of A.C. current in a circuit. *Id.*, .013. On the other hand, pure inductance offers no resistance to D.C. current flow. *Id.*, .014. An inductor’s ability to resist A.C. current flow is measured as “inductive reactance” (X_L). Biswal, EX-1008.016.

Inductors are usually coil-shaped:

¹ Pin cites are to the page number applied to exhibits in accordance with 37 C.F.R. § 42.63(d)(2)(ii). This number aligns with the PDF page number.

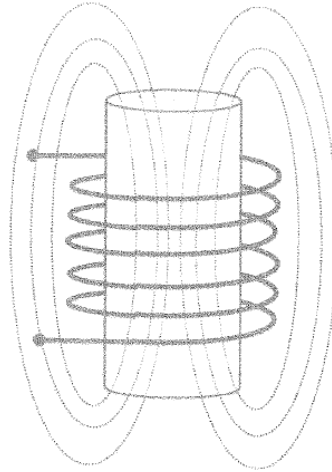


Figure 2.6. The typical coil inductor.

Niknejad (2000), Fig. 2-6 (EX-1009.033)

As current flows through the coil, a magnetic field is produced as illustrated by the imaginary flux lines above. Each additional turn of the inductor adds to the magnetic field. *Id.* The inductance is a function of the area of the loop and the number of turns. *Id.* The inductance L is generally defined as the magnetic flux (Φ) linked with it when a unit current (i) flows through it:

$$L = \frac{\Phi}{i}$$

Biswal, EX-1008.015; *see* EX-1003, ¶¶ 45-52.

B. Q-Factor

An inductor's “quality factor” (“Q-factor”) represents the ratio of energy storage to energy loss over an excitation cycle:

$$Q \equiv \frac{\text{energy stored}}{\text{energy loss}}$$

Niknejad (2007), EX-1010.142. An inductor's Q-factor at a given frequency is a measure of its efficiency; the higher the Q, the lower its energy loss and the closer it approaches an ideal inductor. *Id.*, .142-.143; Niknejad (2000), EX-1009.025; EX-1003, ¶¶ 53-57.

C. Capacitors

Capacitors store electrical energy by accumulating electric charges on two close surfaces insulated from each other. Biswal, EX-1007.003. The function of the capacitor is to store a large amount of charge for a given voltage difference or to store a given charge at low voltage difference. *Id.*

Capacitance is the ratio of charge transferred from one plate to the other plate, to the voltage difference produced between the plates: $C = Q/V$, where C is the capacitance, Q is the amount of charge transferred from one plate to the other, and V is the voltage or potential difference between the two plates. *Id.*; EX-1003, ¶¶ 66-72. A capacitor is schematically represented below:

Symbols of capacitor

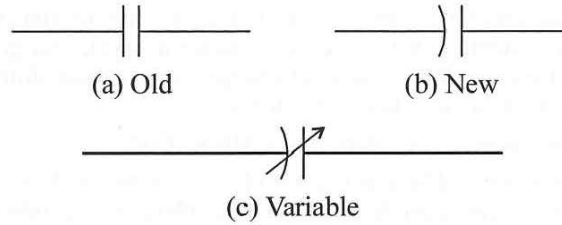
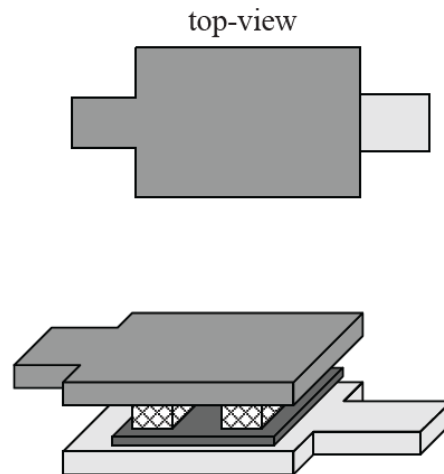


Fig. 2.2

Biswal, Fig. 2.2 Capacitor Symbols (EX-1008.004)

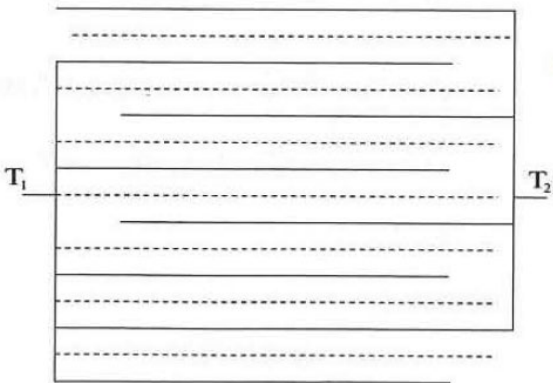
1. Capacitor Types

Capacitors come in various forms. One is parallel plate capacitors, also called metal-insulator-metal (MIM) capacitors. Biswal, EX-1008.004; Niknejad, EX-1007.026-.028. Due to their simple and compact geometry, MIM capacitors were commonly used on IC chips. Berny, EX-106.090; Niknejad, EX-1007.026; EX-1003, ¶ 73. An illustration of an integrated MIM capacitor is below:

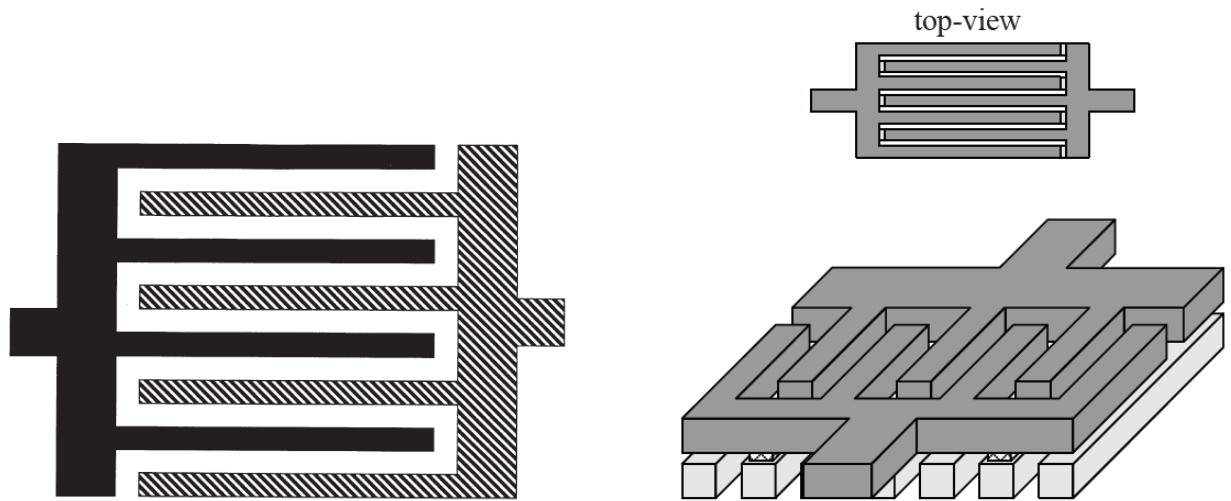


Berny, Fig. 3.10 (partial) MIM Capacitor (EX-1016.091)

Another type is finger capacitors, also called metal-oxide-metal (MOM) capacitors. Niknejad, EX-1007.027. Finger capacitors are composed of parallel fingers connected to either port of the device. *Id.* “Finger” capacitors can be easily fabricated in any modern CMOS process due to the abundance and high packing density of the metal layers. *Id.* A finger capacitor is equivalent to many parallel plate capacitors, so it is sometimes called a multi-plate capacitor. Biswal, EX-1008.005 (commercial capacitor). This capacitor can realize large capacitance with minimal area. *Id.*; EX-1003, ¶ 74. Examples are shown below:



Biswal, Fig. 2.4 (EX-1008.005) (left); Niknejad, Fig. 3.11 (EX-1007.027) (right)



Lee, Fig. 11.10 (EX-1019.009) (left); Berny, Fig. 3.10 (EX-1016.091) (right)

Another type is metal-oxide-semiconductor (MOS) capacitors, commonly called variable capacitors or “varactors.” Niknejad (2000), EX-1009.042-.045.

Varactors are voltage-controlled capacitors used in LC voltage-controlled oscillators. Williamson, EX-1015.039; Niknejad (2007), EX-1010.016-.018. An exemplary MOS varactor is below:

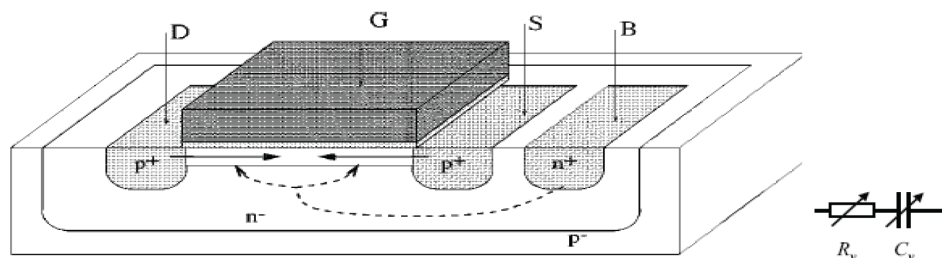


Figure 3.9 MOS Varactor Equivalent Circuit [3]

Williamson, Fig. 3.9 (EX-1015.044)

Varactors are so named because their capacitance can be varied. Williamson, EX-1015.039. Varactors have been used in VCO designs for decades. *See* Kral, EX-1017 (discussing MOS capacitor tuning in a VCO).

Not surprisingly, the 582 patent acknowledges that “capacitors in various forms, such as a metal-oxide-metal (MOM) capacitor, a metal-insulator-metal (MIM) capacitor, or a metal-oxide-semiconductor (MOS) capacitor” are “well known in the field.” EX-1001, [12:11-16]; *see* EX-1003, ¶¶ 75-80.

D. LC Resonant Circuits

It has been known for over a century that an inductor and a capacitor can form a resonant circuit. EX-1003, ¶ 81. “LC resonators, also referred as LC tanks, are made up of an inductor and a capacitor connected in series or in parallel. One or more resistive components modeling the resonator losses are generally included.” Berny, EX-1016.079. Thus, “in the simplest case, LC tanks are represented as series or parallel RLC networks,” as illustrated below. *Id.*

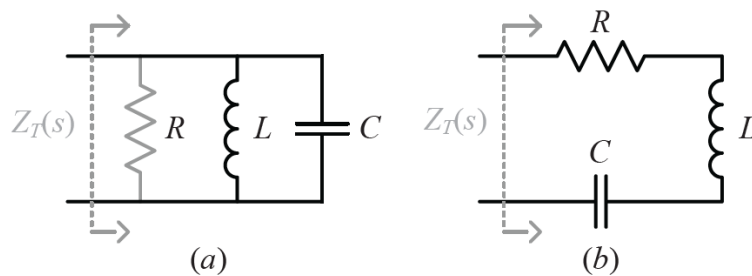


Figure 3.2: (a) Parallel LC tank. (b) Series LC tank.

Berny, Fig. 3.2 (EX-1016.079)

An LC resonant circuit operates as follows. *See* EX-1003, ¶ 82 (*citing* Berny, EX-1016.079-.082). Connecting an inductor across a charged capacitor results in the voltage across the capacitor driving a current through the inductor. Electric charges flow back and forth between the plates of the capacitor, through the inductor. The energy oscillates back and forth between the capacitor and the inductor. The tuned circuit's action, known as a harmonic oscillator, is like a pendulum swinging back and forth. In most applications the tuned circuit is part of a larger circuit which applies alternating current (AC) to it, driving continuous oscillations. If the frequency of the applied current is the LC circuit's natural resonant frequency, resonance will occur, where a small driving current can excite large amplitude oscillating voltages and currents. EX-1003, ¶ 82.

The resonant frequency (ω_o) is determined by the capacitance (C) and inductance (L). The equation for calculating the resonant frequency is:

$$\omega_o = 1/\sqrt{LC}$$

Berny, EX-1016.080. The LC resonator's quality factor, Q, indicates its ability to retain energy. *Id.* The Q of an LC resonator can be calculated using the equation below, where ω represents frequency. More stored energy and less dissipated power leads to a higher Q. *See id.:*

$Q \equiv \omega \cdot \frac{\text{Energy stored}}{\text{Average power dissipated}}$
--

Berny, EX-1016.080. An LC resonant circuit is used in circuits such as voltage-controlled oscillators (VCO) and phase lock loops (PLL), among others. *See* Niknejad, EX-1007.032-.034; Berny, EX-1016.023-.027; Williamson, EX-1015.012-.014. LC oscillators are widely used in wireless communication systems. Yuan, EX-1018.018; Niknejad (2007), EX-1010.018; *see* EX-1003, ¶¶ 83-87. The 582 patent acknowledges that, “[i]n design of circuits such as a filter, a network impedance matching circuit, a voltage-controlled oscillator (VCO), a transmitting and receiving module circuit,” using an LC resonant circuit in semiconductor devices was known in the art. EX-1001, [1:35-36].

A common design approach to LC circuits was to place the capacitor at a position aligned with the extension segments of the inductor and being offset from the core-conductor segment of the inductor. EX-1003, ¶ 88. Such a spatial relationship, as well as the benefits thereof, was well-known before the 582 patent. *Id.*, ¶¶ 88-89. The below image from an academic thesis pre-dating the 582 patent priority date by more than a decade shows this:

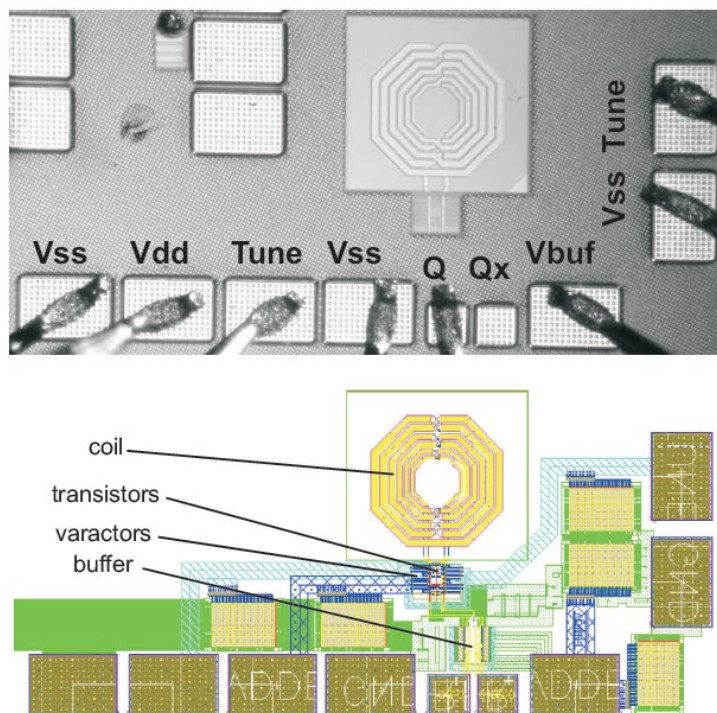


Figure 5.12: Die photograph and layout of one VCO. Metal fill structures are suppressed in the area of the inductor and the VCO-core.

Maget, Fig. 5.12 (EX-1030.065)

AMD's expert identifies numerous other examples. *See* EX-1003, ¶ 88-89.

V. THE 582 PATENT AND FILE HISTORY

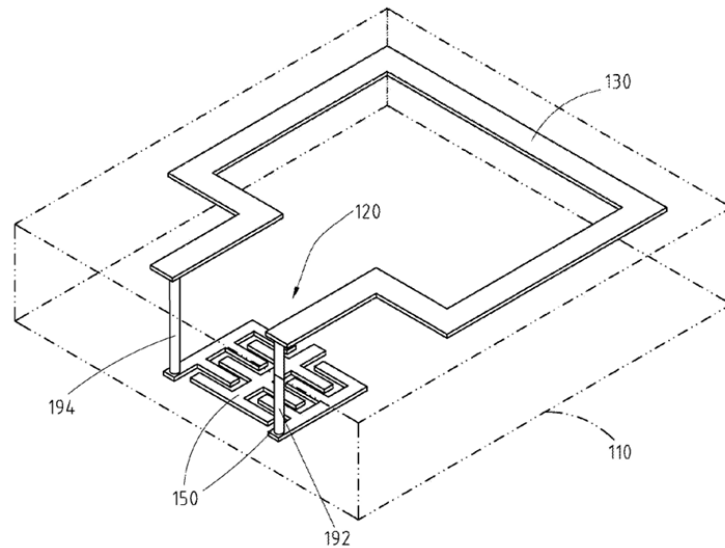
A. The 582 Patent

The 582 Patent is directed to an LC resonant circuit. EX-1001, [1:16-17].

The patent acknowledges that “[i]n design of circuits such as a filter, a network impedance matching circuit, a voltage-controlled oscillator (VCO), a transmitting and receiving module circuit,” using a LC resonant circuit in a semiconductor device was known in the art. [1:35-36]. It also acknowledges that arranging various electronic components onto a semiconductor device using insulation layers was

well-known. [1:24-32], [8:40-42] (“Here, the structures of various embedded electronic elements are well known to in the field, and therefore are no longer elaborated.”).

Fig. 4 depicts a representative embodiment:



582 Patent, Fig. 4 (EX-1001)

The “semiconductor device with an LC resonant circuit includes an insulation layer 110, ... an inductor component 130, and a capacitor component 150.” [3:9-12]. In Fig. 5, the inductor component 130 includes a coil-conductor segment 131 and two extension-conductor segments 133,135:

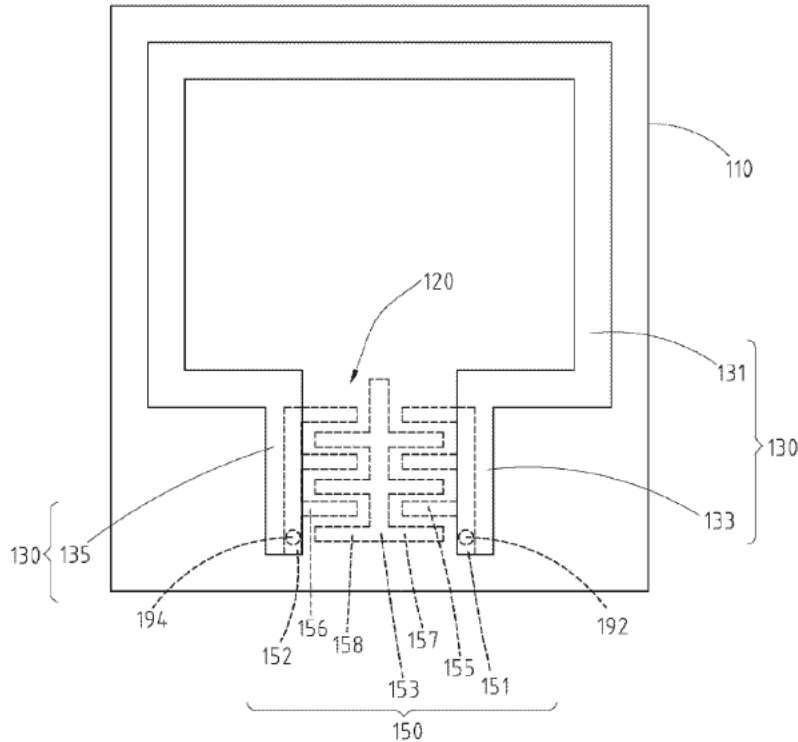


FIG. 5

582 Patent, Fig. 5 (EX-1001)

The coil-conductor segment 131 serves as an induction part of the inductor. The extension-conductor segments 133, 135 serve as input/output parts for receiving or transmitting signals. [3:22-27]. The two extension-conductor segments 133, 135 are connected to the two ends of the coil-conductor segment 131 and extend outwards in a direction away from the two ends of the coil-conductor segment 131. [3:33-42]. Region 120 is defined by the two extension-conductor segments 133, 135 and the coil-conductor segment 131. [3:43-47].

The capacitor component 150 is arranged on a lower surface of the insulation layer 110, opposite to the inductor component 130. That is, the capacitor

component 150 is located below the first region 120 and spaced by the insulation layer 110 from the inductor component 130. [3:48-54]. The capacitor component 150 includes two connecting segments 151, 152 and a plurality of electrode segments 155, 156. The electrode segments serve as electrode plates of the capacitor. The connecting segments 151, 152 are used for receiving or transmitting signals. [4:34-45]; EX-1003, ¶¶ 90-97.

B. The Prosecution History

The 582 patent issued from an application filed July 23, 2014. There were several rounds of substantive office actions and responses, and the claims were extensively amended. *See generally* EX-1002; EX-1003, ¶¶ 98-107.

Originally-filed claim 1 required, *inter alia*, an inductor component with a coil-conductor segment and two extension conductor segments formed in an insulation layer, and a capacitor component on the other surface of the insulation layer. EX-1002.426. The claims were rejected, and the applicants amended claim 1 to require that the capacitor component was “configured outwards relative to the coil-conductor segment.” *Id.*, .326. The Examiner again rejected the claims, leading to another amendment, this one specifying that the capacitor component “is not substantially overlapped with the coil-conductor segment.” *Id.*, .070. The Examiner remained unconvinced, and finally rejected the claims.

The applicants filed a request for continued examination (*id.*, .023) and again amended the claims. The capacitor component was amended to recite:

a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

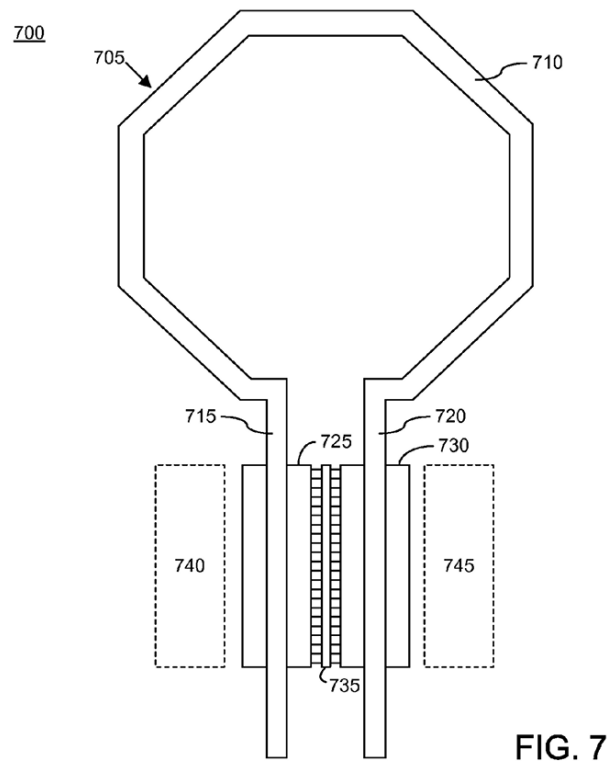
a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

EX-1002.027. The Examiner allowed these claims, but gave detailed reasons for doing so. *Id.*, .011-.013. Specifically, the Examiner found that the closest prior art (U.S. Patent No. 9,270,247 to Jing, EX-1033) disclosed all limitations except “wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments.” Concerning Jing, the Examiner stated:

The inductor 705 is connected to TWO separate finger capacitors or “capacitor components” 725 and 730. Each of the capacitor components overlaps with only a single one of the “extension-

conductor segments” in a vertical direction and not both (i.e. “the two extension-conductor segments”) as recited within the claims. Further, each of the finger capacitors or “capacitor components” 725 and 730 is its own separate capacitor structure separated by switches 735 as shown in Fig. 7, and thus elements 725 and 730 together cannot be interpreted as “a capacitor component”.

EX-1002.012-.013. Jing fig. 7 is shown below:



Jing, Fig. 7 (EX-1033)

The Examiner thus held that the two finger capacitors 725, 730 did not read on the claims because, first, the claims require that the plurality of connecting segments of the capacitor component are “respectively overlapped” with the two extension-

conductor segments of the inductor. As shown in Jing, one finger capacitor 725 is overlapped by one extension-conductor segment, and the other finger capacitor 730 is overlapped by the second extension-conductor segment. But the claims require that the “connecting segments of the capacitor component” be overlapped by both extension conductor segments (not merely one). Second, the Examiner found that the two finger capacitors in Jing (725, 730) are each their “own separate capacitor structure” and cannot together be “interpreted as ‘a capacitor component.’” EX-1002.012-.013.

C. The Challenged Claims

The challenged claims are 1-5 and 9.

VI. LEVEL OF ORDINARY SKILL IN THE ART

By April 16, 2014, a person of ordinary skill in the art (“POSITA”) would have had a B.S.E.E. and at least 3-4 years of professional experience in the field of integrated circuit design; or a M.S.E.E. and 1-2 years of professional experience in the field of IC design; or a Ph.D. in electrical engineering. EX-1003, ¶ 4.

VII. STATUTORY GROUNDS FOR THE CHALLENGES

Ground 1	Obviousness under § 103 of Claims 1-5, 9 based on Gonzalez, <i>A 56-GHz LC-Tank VCO With 17% Tuning Range in 65-nm Bulk CMOS for Wireless HDMI</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 58, Issue 5 (May 2010) (EX-1005)
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Ground 2	Obviousness under § 103 of Claims 1-5, 9 Based on Matthew Muh, Master of Science thesis entitled <i>Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO</i> , Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley, 2005 (EX-1006) in view of A. Niknejad, <i>mm-Wave Silicon Technology 60 GHz and Beyond</i> (Springer Science+Business Media 2008) (EX-1007)
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Gonzalez appeared in the May 2010 issue of IEEE Transactions on Microwave Theory and Techniques, which is “published monthly by the Institute of Electrical and Electronics Engineers, Inc.” EX-1005.001-002. That issue was a “special issue on 2009 Radio Frequency Integrated Circuits (RFIC) Symposium.” *Id.* As the IEEE website shows, that conference occurred on June 7-9, 2009, and Gonzalez was added to the IEEE website Xplore on June 26, 2009. *See* EX-1038. At a minimum, Gonzalez was available shortly after the May 2010 issue of IEEE Transactions on Microwave Theory and Techniques was published. *See* EX-1039 (showing the May 2010 issue and Gonzalez were published in 2010). Dr. Sylvia Hall-Ellis, a library and information resources expert, asserts that Gonzalez was

publicly accessible by June 26, 2009, or shortly thereafter. EX-1036, ¶¶ 39-45.²

Gonzalez is therefore prior art under 35 U.S.C. § 102(a)(1) (post-AIA).

Telegonaktiebolaget LM Ericsson v. TCL Corp., 941 F.3d 1341, 1347 (Fed. Cir. 2019) (journal paper “published for at least thirty years” and in libraries “accessible to the public” qualified as printed publication); *Voter Verified, Inc. v. Premier Election Sols., Inc.*, 698 F.3d 1374, 1380-81 (Fed. Cir. 2012).

Dr. Hall-Ellis demonstrates that the Muh thesis was cataloged on July 8, 2005 at the University of California-Berkeley Libraries, indexed, and searchable by key word (title, author, institution). EX-1036, ¶¶ 72-77. Thus, Muh was publicly accessible as of July 8, 2005, and is § 102(a)(1) prior art. *GoPro, Inc. v. Contour IP Holding LLC*, 908 F.3d 690, 693 (Fed. Cir. 2018) (“We have interpreted § 102 broadly, finding that even relatively obscure documents qualify as prior art so long as the relevant public has a means of accessing them.... For example, we have determined that a single cataloged thesis in a university library was sufficiently accessible to those interested in the art exercising reasonable diligence.”).

² Dr. Hall-Ellis also confirms that the IEEE Journal in which Gonzalez appeared in print form has been published since at least 1963 and is available in 387 libraries. EX-1036, ¶¶ 42-45.

Niknejad is a book published by Springer Science+Business Media in 2008. EX-1007. Dr. Hall-Ellis has confirmed that Niknejad was publicly accessible on or shortly after February 1, 2008. EX-1036, ¶¶ 78-85. Niknejad is therefore § 102(a)(1) prior art.

VIII. CLAIM CONSTRUCTION

Petitioner applies herein the understanding of the claims set forth in Realtek's infringement chart in the ITC Investigation. EX-1034. Petitioner reserves the right to challenge Realtek's proposed constructions in litigation and to assert that certain terms are invalid under 35 U.S.C. § 112.

IX. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

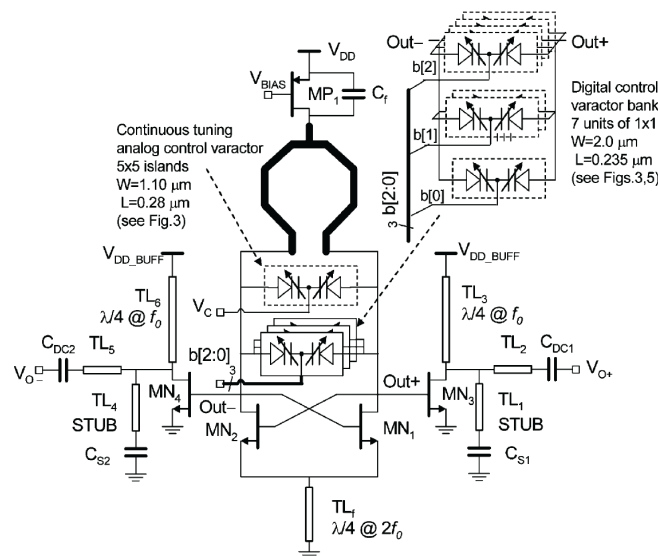
A. GROUND 1: Claims 1-5, 9 are Obvious Under 35 U.S.C. § 103 Based on Gonzalez

1. Gonzalez Introduction

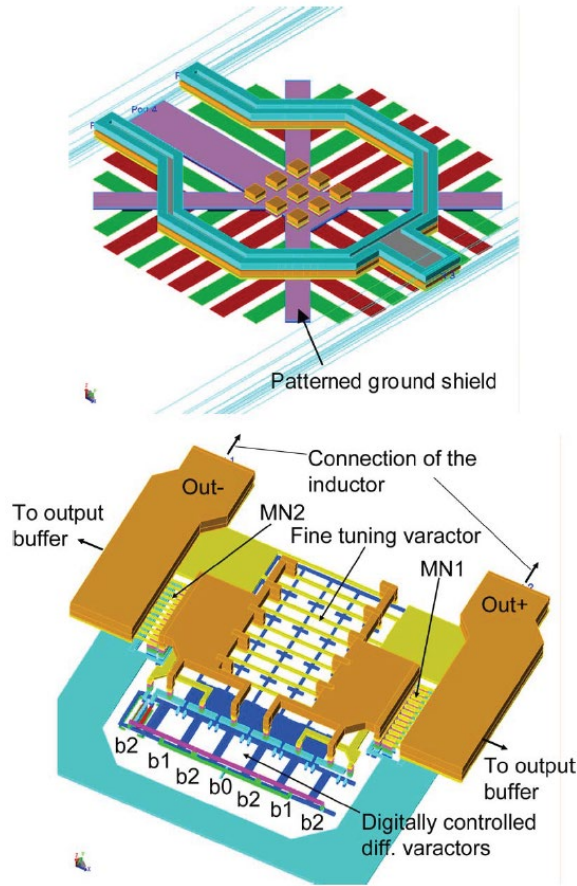
Gonzalez discloses a “voltage-controlled oscillator (VCO)” implemented using a CMOS process whose “oscillation frequency is tuned both by an analog input and by a 3-bit digital control bus using the same type of differential varactors.” EX-1005.004, Abstract.

Gonzalez's VCO includes an inductor-capacitor resonant circuit (LC tank). *Id.*, .004 (“The oscillator core is composed of ... an LC tank.”). The LC tank includes an inductor, a fine-tuning variable capacitor (varactor), and a coarse-tuning varactor. *Id.*, .005-.006.

The inductor and fine-tuning varactor are positioned in the same manner as the LC arrangement described and claimed in the 582 patent. *See* EX-1003, ¶¶ 113-117. A schematic of Gonzalez’s VCO is depicted in Fig. 2, and a physical design is depicted in Fig. 8, both reproduced below. As shown in those figures, Gonzalez’s inductor is a “single-turn inductor with a central tap,” EX-1005.005-.006, and its fine-tuning varactor includes finger-shaped electrodes inter-digitally connected to the left and right sides of the varactor (*see* yellow metal layer in the bottom half of Fig. 8). The fine-tuning varactor is offset from the coil of the inductor and is aligned with the inductor’s extension segments:



Gonzalez, Fig. 2 (EX-1005)



Gonzalez, Fig. 8 (EX-1005)

EX-1003, ¶ 117. Gonzalez discloses, or at a minimum, renders obvious, each limitation of the challenged claims.

2. Gonzalez Invalidates Claim 1

i. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising: [preamble]

Gonzalez discloses a semiconductor device with an LC resonant circuit.

Gonzalez discloses an oscillator circuit having “an LC tank.” EX-1005.004. The LC tank includes an inductor and multiple variable capacitors (varactors). *Id.*, .004-

.005 (“The tank inductance is a single-turn inductor with a central tap.... A differential N+poly/Nwell varactor operating in accumulation mode is used for continuous tuning.... An additional bank of digitally controlled differential varactors provides coarse tuning”). The LC tank is a resonant circuit with a “self-resonant frequency.” *Id.*, .005; EX-1003, ¶ 118.

Further, Gonzalez’s “VCO circuit is implemented in a 65-nm bulk CMOS process” as part of a semiconductor device. EX-1005.009. An image of the semiconductor device is below:

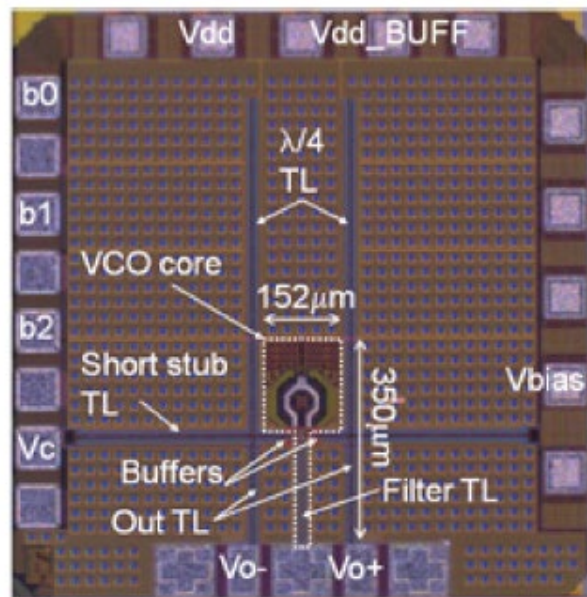


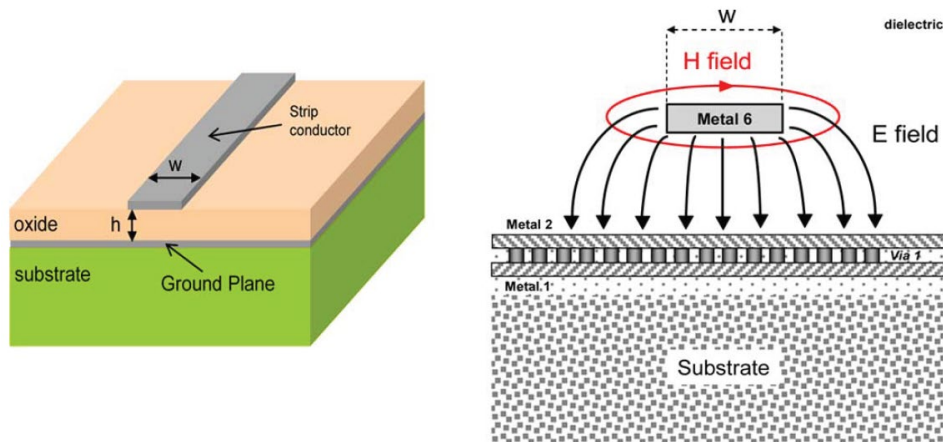
Fig. 12. VCO die micrograph.

Gonzalez, Fig. 12 (EX-1005)

See EX-1003, ¶ 119.

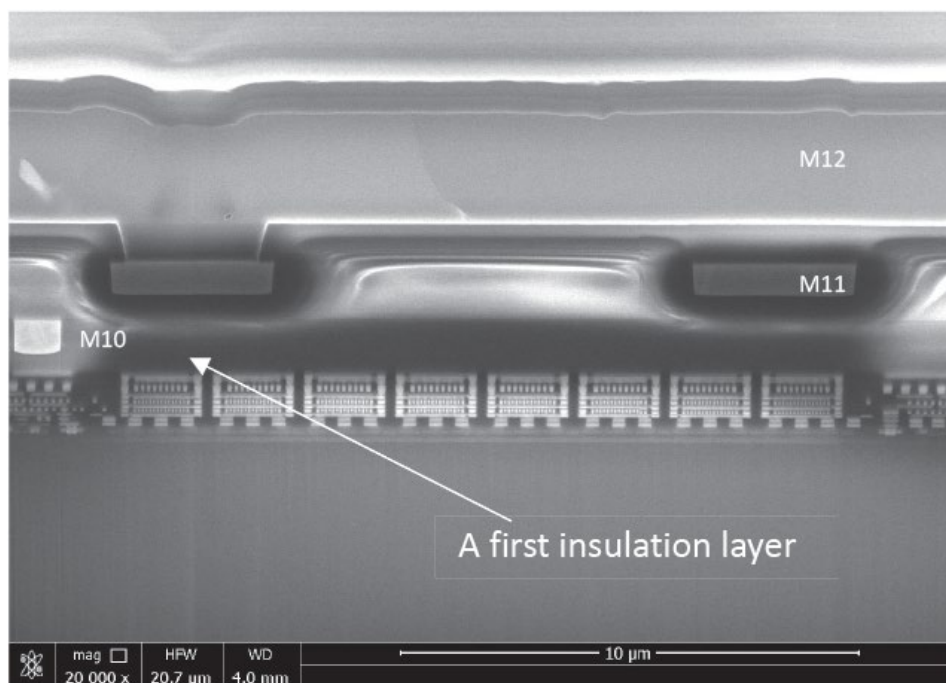
ii. “a first insulation layer”

Gonzalez discloses this limitation. Fig. 9 (below) discloses “a dielectric” layer (“oxide”) between a top metal layer (M6) and a ground plane composed of two bottom metal layers (M1, M2). EX-1005.007-008 (“This microstrip line is made up of a conducting strip on a dielectric in parallel to a ground plane.”). A POSITA would understand that a dielectric (*e.g.*, oxide) is an insulation material that can form insulation layers. EX-1003, ¶ 120. Therefore, part of Gonzalez’s dielectric material forms a first insulation layer:



Gonzalez, Fig. 9 (EX-1005)

See EX-1003, ¶ 120. This interpretation is consistent with Realtek’s interpretation:



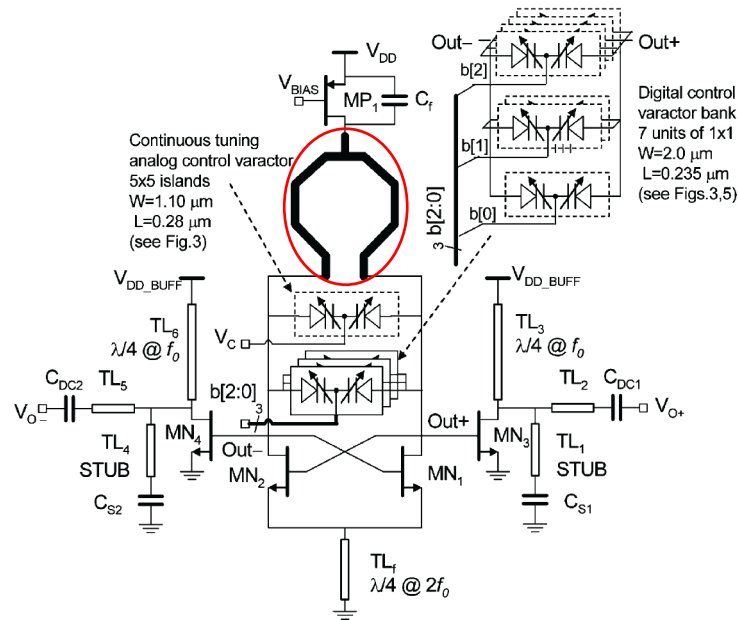
Realtek Infringement Chart (EX-1034.008)

Gonzalez’s Fig. 9 illustrates an oxide between a strip conductor implemented on a top metal layer (M6) and a ground plane implemented on two bottom layers (M1 and M2) for the purpose of “showing electric and magnetic fields” generated by the strip conductor. EX-1005.008. A POSITA would understand that, between metal layers M6, M2, additional metal layers can be (and indeed are) implemented inside the oxide, and that more than one insulation layer would be formed inside the oxide. *Id.*, .006 (“The inductor of the tank is a single-turn differential inductor made with the two upper copper metal layers plus the aluminum metallization layer.”); Fig. 8 (showing multiple metal layers for implementing a VCO core circuit); EX-1003, ¶ 122. Such interweaved uses of insulation layers and metal layers in semiconductor devices were well-known

before the 582 patent priority date. *Id.* Indeed, the 582 patent acknowledges this. EX-1001, [1:24-28] (“A typical semiconductor integrated circuit includes a silicon substrate. *More than one insulation layer is arranged on the substrate, [and] more than one metal layer ... is arranged in the insulation layer...*”).³ EX-1003, ¶ 122.

iii. “an inductor component, comprising”

Gonzalez’s LC tank includes “a single-turn differential inductor.” EX-1005.006. This is shown in Fig. 2 as a horseshoe-shaped structure. EX-1005.004:

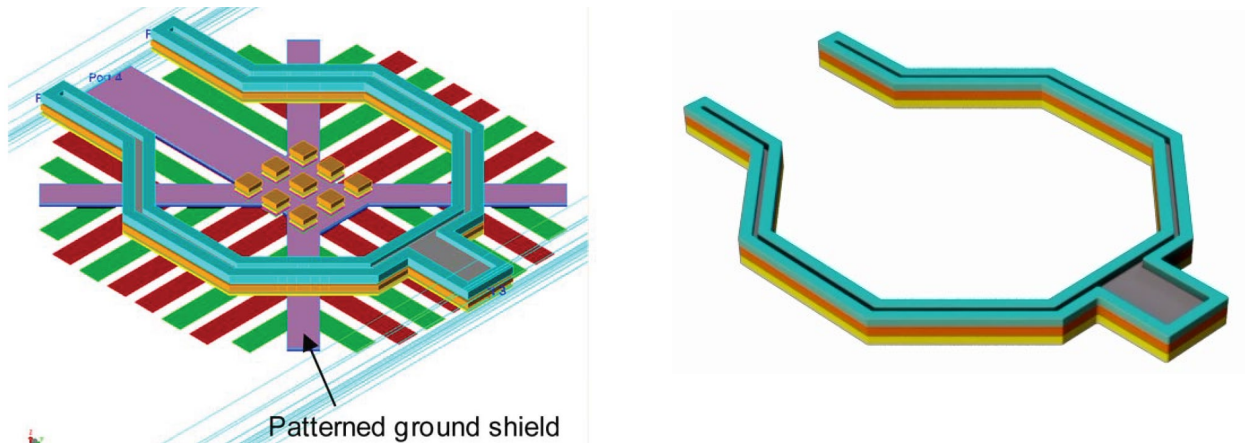


Gonzalez, Fig. 2 (EX-1005) (annotated)

EX-1003, ¶ 123. Gonzalez’s inductor, along with a patterned ground shield formed under the inductor, is also shown in the top half of Fig. 8 (below, left). A

³ All emphasis added herein.

simplified view of Fig. 8's inductor without the ground shield is also shown
(below, right):

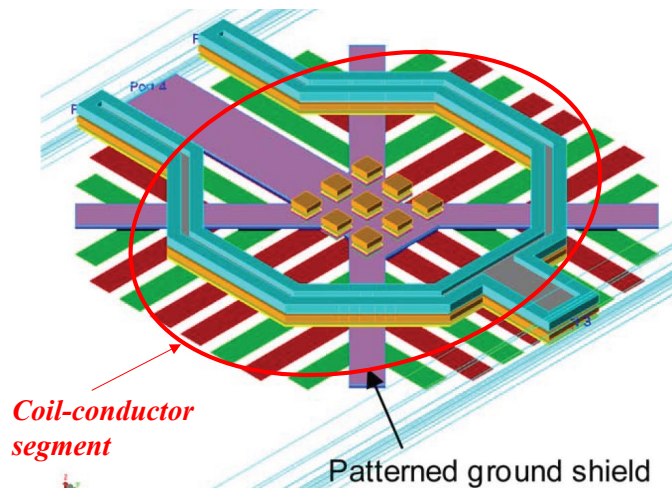


Gonzalez, Fig. 8 (partial and simplified) (EX-1005)

EX-1003, ¶ 124.

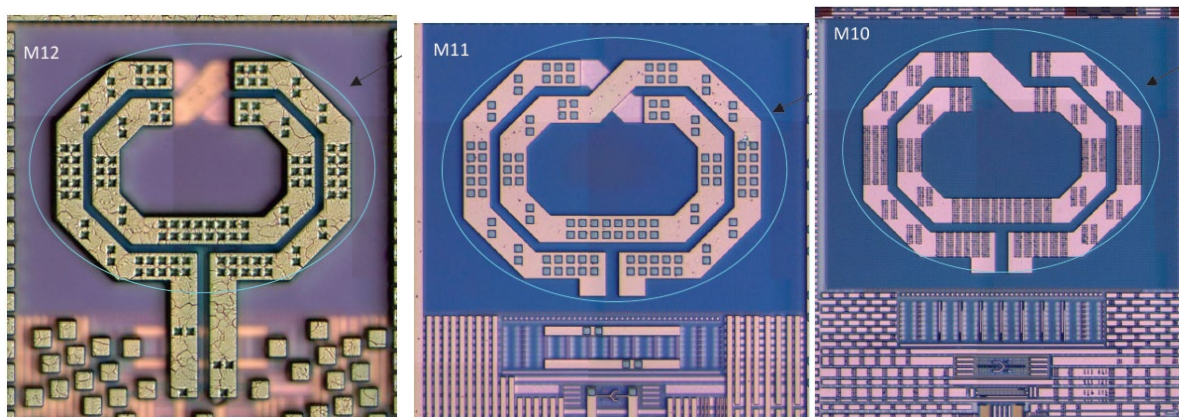
- iv. **“a coil-conductor segment, located on a surface of the first insulation layer; and”**

Gonzalez's inductor includes a coil-conductor segment that serves as an induction part of Gonzalez's inductor. EX-1005.005:



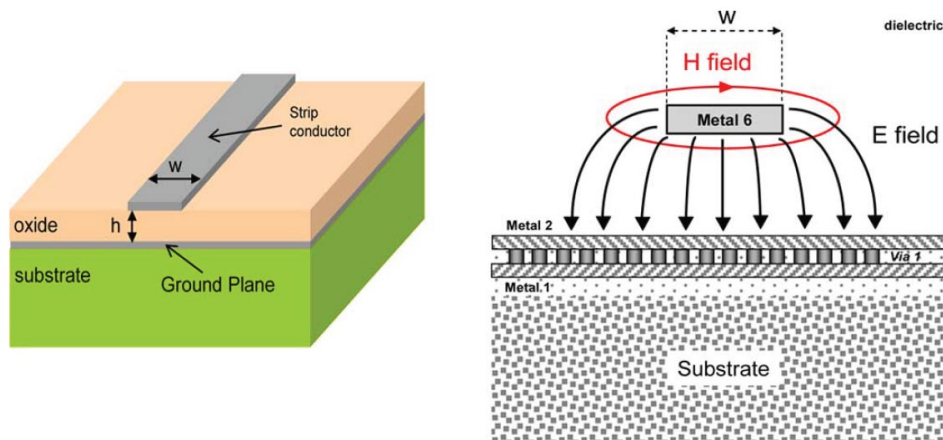
Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶¶ 125-126. This interpretation is consistent with Realtek’s interpretation of the coil-conductor segment (inside light blue ovals):



Realtek Infringement Chart (EX-1034.011-.012)

The coil-conductor segment of Gonzalez’s inductor is located on a surface of the first insulation layer. Gonzalez’s inductor is “implemented with a microstrip transmission line (TL).” EX-1005.005. As illustrated in Fig. 9, the microstrip line is located on a surface of an oxide (dielectric) layer:



Gonzalez, Fig. 9 (EX-1005)

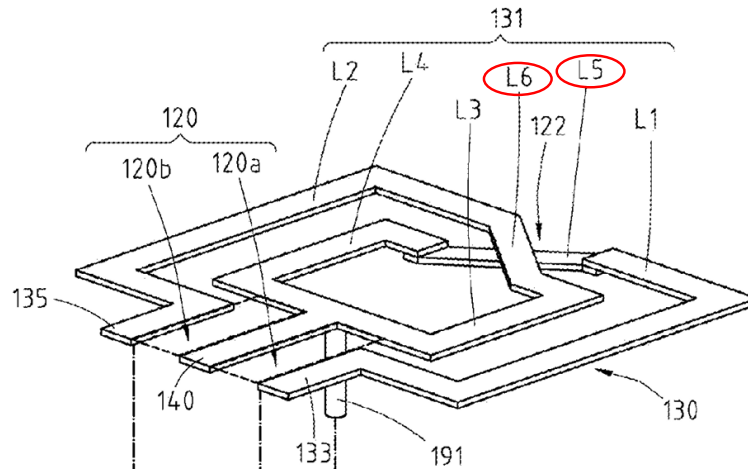
EX-1003, ¶¶ 127-128; *see* Gonzalez Fig. 12 (showing transmission lines (TL) implemented in a top metal layer on top of an insulation layer). This interpretation is consistent with how Realtek interprets this limitation. *See* EX-1034.010 (alleging that “the coil-conductor segment is located on a surface of the first insulation layer (which is located approximately below the M10 layer)”); EX-1003, ¶¶ 128-129.

To the extent Gonzalez’s Fig. 8 does not expressly disclose a first insulation layer with a surface on which a coil-conductor segment of Gonzalez’s inductor is located, this would have been obvious to a POSITA, as the purpose of Fig. 8 is to show “[t]he layout of the interconnection between the varactors, the inductor, and the active sections of the VCO core and the buffers.” EX-1005.007. Including insulation layers in Fig. 8 would render electronic components on underlying layers invisible and therefore defeat the figure’s purpose. EX-1003, ¶ 130. It would

have been obvious to a POSITA to use a first insulation layer with a surface on which a coil-conductor segment of Gonzalez's inductor is located. *Id.*, ¶ 131. Gonzalez discloses that the inductor is "made with the two upper copper metal layers plus the aluminum metallization layer" and that a microstrip line of the inductor uses "the top metal level (M6) as a conducting strip." EX-1005.006, .008. In view of this disclosure, a POSITA would have understood that the inductor's coil-conductor segment, like the microstrip line, would use the top metal level M6 and would also be located on a surface of the first insulation layer. EX-1003, ¶ 131. That is, Gonzalez's multi-layer coil-conductor segment is located on a surface of the first insulation layer because it uses one or more metal levels (*e.g.*, M6, or M6+M5) located on a surface of the first insulation layer. *Id.*

This interpretation is consistent with how Realtek interprets the coil-conductor segment of the accused inductor, which includes multiple metal layers. *See* EX-1034.009 (accusing "an inductor component, composed with at least three metal layers (M10-M12)"). Further, this interpretation is consistent with the 582 patent claims. Claim 1 recites "a coil-conductor segment, located on a surface of the first insulation layer," while claim 7 (depending from claim 1) recites "the coil-conductor segment has a *pair of staggered parts*." EX-1001, claims 1, 7. The "staggered parts" (*e.g.*, L5 and L6 illustrated in Fig. 9 below) are multi-layer structures. EX-1001, [8:65-9:7] (stating that the "coil-conductor segment 131"

includes “at least one pair of staggered parts. . . . and each pair of staggered parts have two staggered guide lines L5 and L6.”):



582 Patent, Fig. 9 (partial) (EX-1001) (annotated)

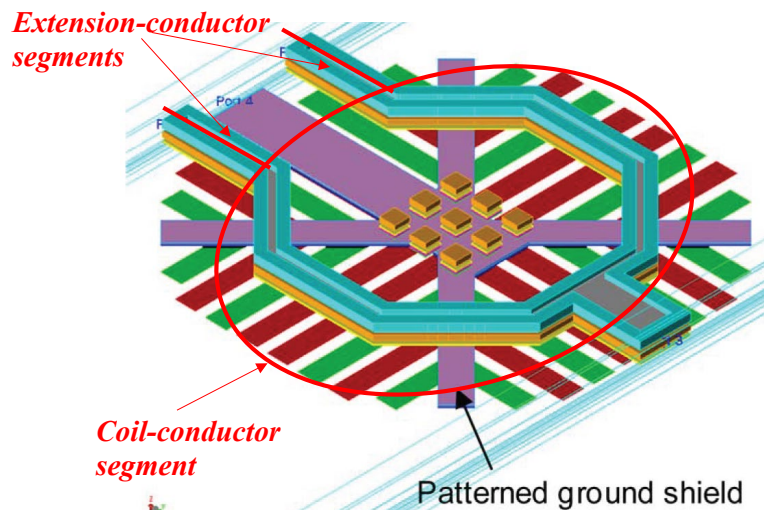
A POSITA would have understood from Fig. 9 that staggered guide lines L5, L6 are on different metal layers and an insulation layer exists between them to prevent electrical shorting. EX-1003, ¶ 131. Nonetheless, the 582 patent claims its coil-conductor segment (including multi-layer structures like in Fig. 9) is “located on a surface of the first insulation layer.” In the same way, a POSITA would have understood that Gonzalez’s coil-conductor segment including multi-layer structures is located on a surface of the first insulation layer. EX-1003, ¶ 131.

Further, using an insulation layer as claimed was well-known in the art. The 582 patent acknowledges this. EX-1001, [1:24-28] (“A typical semiconductor integrated circuit includes a silicon substrate. *More than one insulation layer is arranged on the substrate, more than one metal layer ... is arranged in the*

insulation layer, and the metal layers may be formed with a built-in part of a chip by means of a semiconductor fabrication process.”); EX-1003, ¶ 132.

- v. “two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and”

Gonzalez’s inductor includes two extension-conductor segments, *see* Fig. 8:

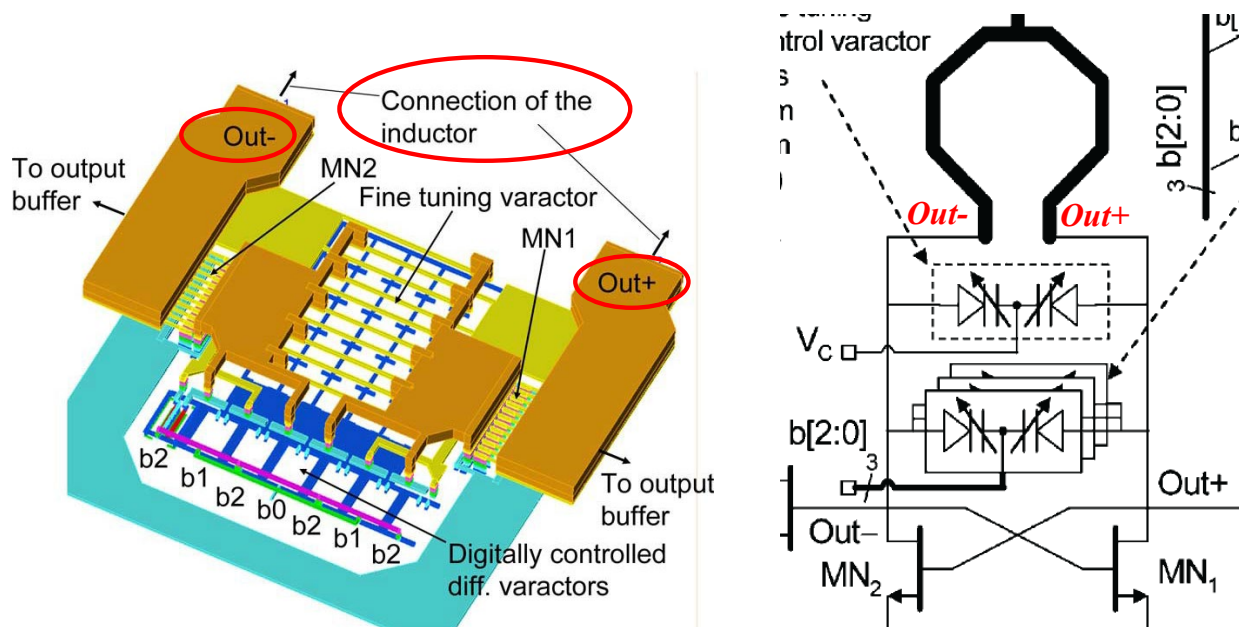


Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶ 133. The extension-conductor segments serve as input/output for the inductor. Each extension-conductor segment includes a “connection of the inductor,” as shown in the bottom half of Fig. 8. The two extension-conductor

segments are connected to “two differential terminals (Out+ and Out-)”

respectively, as shown in Fig. 2 and the bottom half of Fig. 8. EX-1005.006:

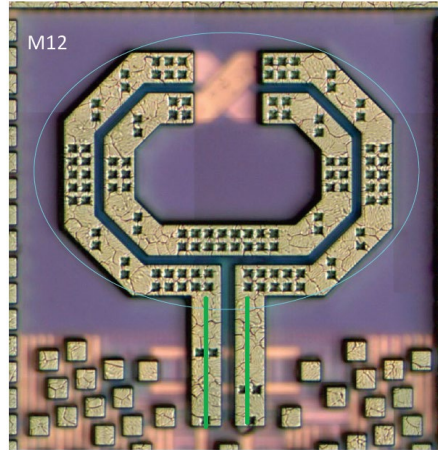


Gonzalez, Fig. 8 (partial), Fig. 2 (partial) (EX-1005) (annotated)

EX-1003, ¶ 134.

Like the coil-conductor segment, the two extension-conductor segments are located on the same surface of the first insulation layer. *Id.*, ¶ 135. Further, as shown in Fig. 8, the two extension-conductor segments are coupled to two ends of the coil-conductor segment respectively, are arranged at an interval, and extend outwards relative to the coil-conductor segment. *Id.*

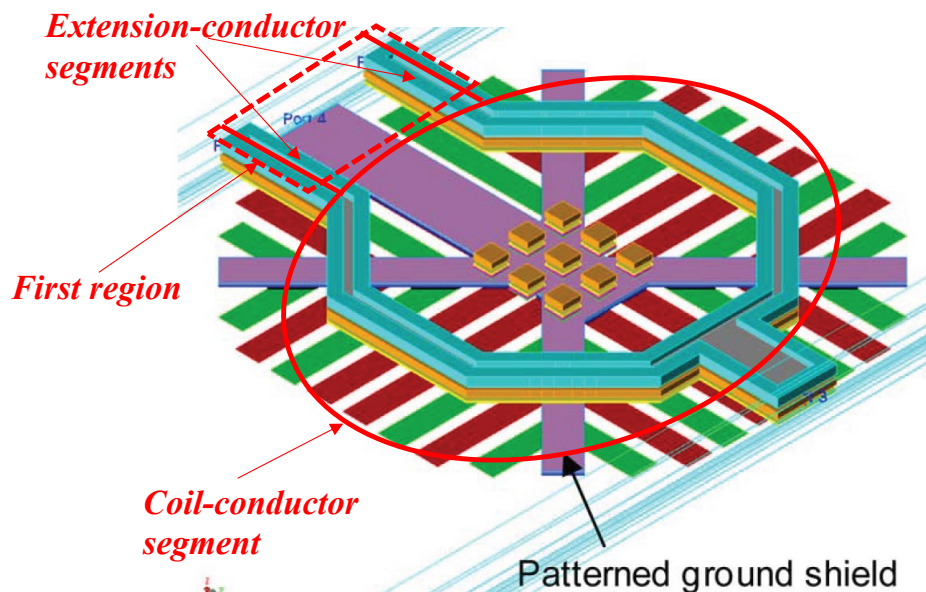
This interpretation is consistent with Realtek’s interpretation of the limitation, where the extension-conductor segments are marked by green lines.



Realtek Infringement Chart (EX-1034.012)

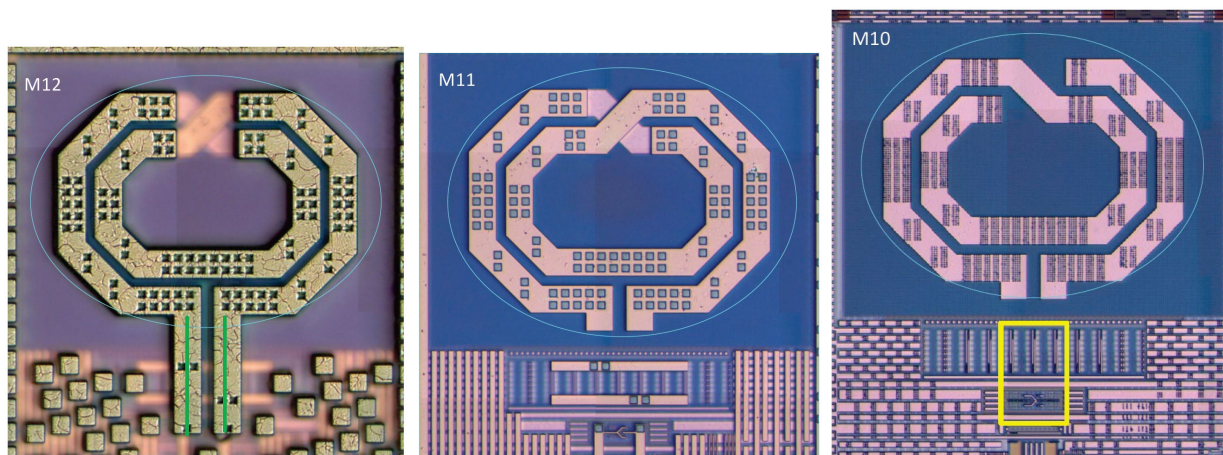
EX-1003, ¶ 136.

Further, based on how Realtek interprets the “first region defined by the two extension-conductor segments and the coil-conductor segment,” Gonzalez discloses such a first region, as illustrated in Fig. 8:



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶ 137. Realtek’s interpretation of the claimed “first region,” is shown below, where the first region is marked by a yellow box.



Realtek Infringement Chart (EX-1034.013)

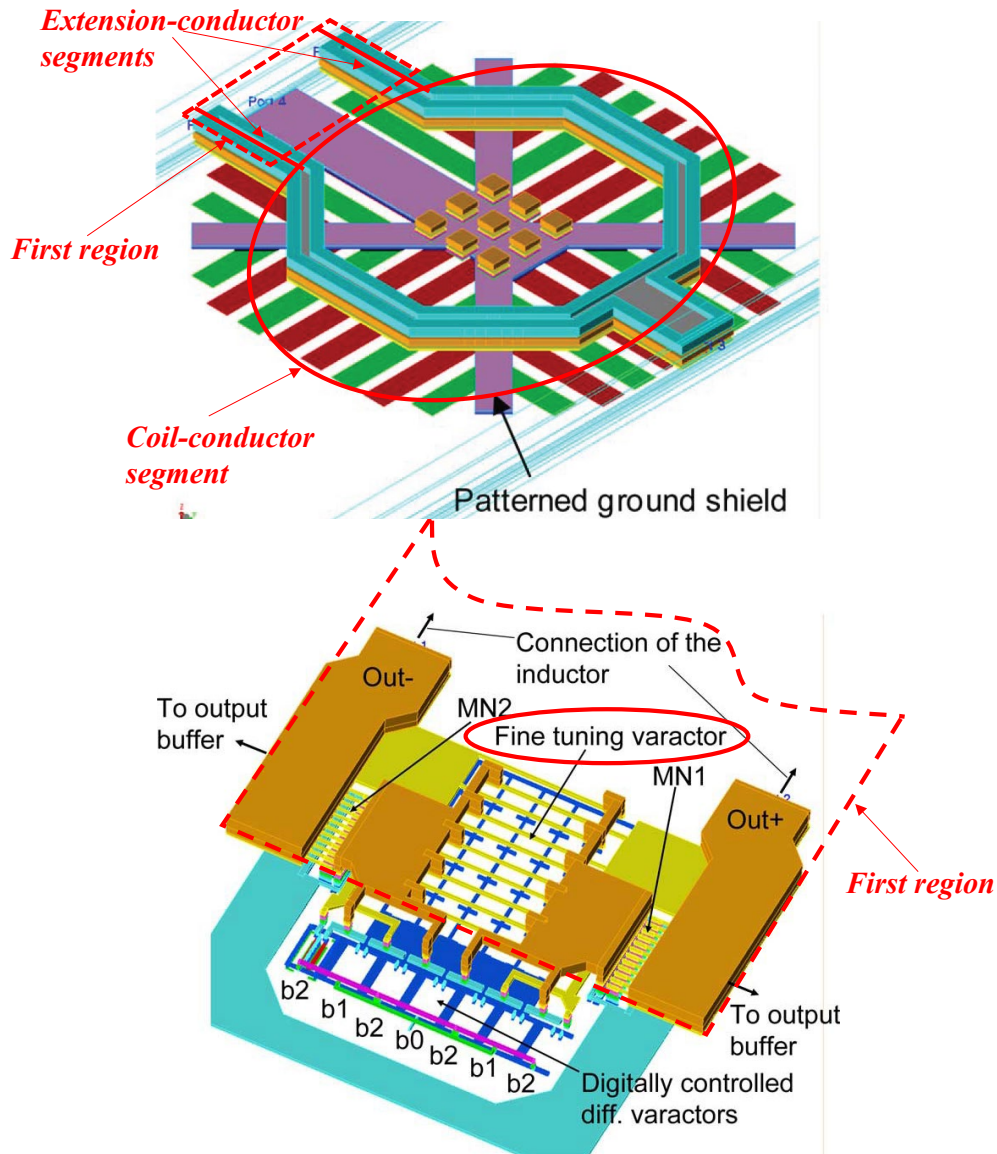
EX-1003, ¶ 138.

- vi. **“a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer,”**

Gonzalez renders this limitation obvious to a POSITA. EX-1003, ¶ 139-146.

Gonzalez discloses a “fine tuning varactor,” *see* Section IV.C.1 *supra*, which is or includes a capacitor component. EX-1003, ¶ 139; *see* EX-1005, Fig. 8. Each “connection of the inductor” (shown in the bottom half of Fig. 8 on a brown metal layer) is part of an extension-connection segment of the inductor (shown in the top half of Fig. 8 also on a brown metal layer). Based on how Realtek has interpreted the term “first region,” in the bottom half of Fig. 8, the first region would extend

back to the top half of Fig. 8 which shows the first region as defined by the two extension-conductor segments and the coil-conductor segment. Therefore, Gonzalez's fine-tuning varactor is arranged corresponding to the first region as interpreted by Realtek. EX-1003, ¶ 140:



Gonzalez, Fig. 8 (EX-1005) (annotated)

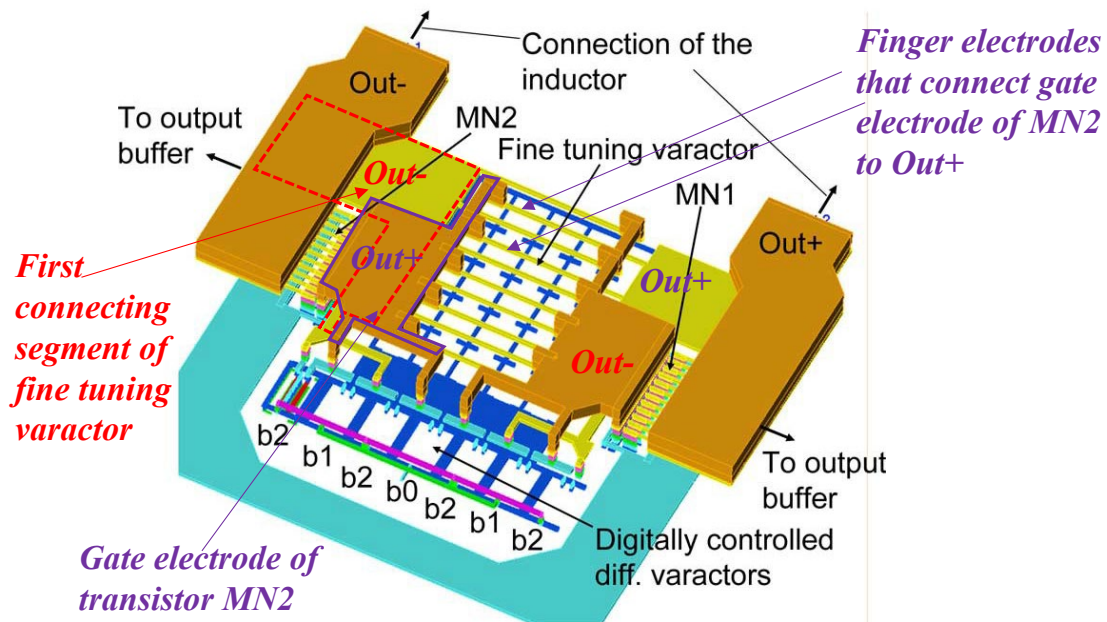
The fine-tuning varactor is “[a] differential N+poly/Nwell varactor operating in accumulation mode [and] is used for continuous tuning” of the VCO. *See* EX-1005.005; Fig. 2; EX-1003, ¶ 141.

To the extent Gonzalez’s Fig. 8 does not expressly disclose a first insulation layer with a surface on which the capacitor component is arranged in an embedded manner opposite to the inductor component, this would have been understandable and obvious to a POSITA. EX-1003, ¶ 142. The purpose of Fig. 8 is to show “[t]he layout of the interconnection between the varactors, the inductor, and the active sections of the VCO core and the buffers.” EX-1005.007. Showing insulation layers in Fig. 8 would render electronic components on underlying layers invisible and therefore defeat the purpose of the figure. EX-1003, ¶ 142.

Nevertheless, it would have been obvious to a POSITA to use a first insulation layer between Fig. 8’s brown metal layer (with two extension-conductor segments of the inductor) and yellow metal layer (with the fine-tuning varactor). Specifically, the brown metal layer vertically overlaps with the yellow metal layer, as illustrated in the bottom half of Fig. 8, so it would have been obvious to place an insulation layer between them to create electric insulation and ensure proper working of electronic components on these two layers. EX-1003, ¶¶ 143-146.

As illustrated in Fig. 8, a first connecting segment of the fine tuning capacitor (annotated below in a red box) is connected to one terminal (Out-), while

a gate electrode of a transistor MN2 (annotated in a dark purple box) is connected to another terminal (Out+) (from right to left of Fig. 8, through a second connecting segment of the fine-tuning varactor and through finger electrodes of the fine tuning capacitor). EX-1003, ¶ 144; *see* EX-1005, Fig. 2 (confirming same electric connections); *id.*, .005 (stating “the dc output voltage of the VCO,” i.e., the voltage difference between terminals Out+ and Out-, “sets the common mode voltage for the differential varactors and the gate-to-source voltage (VGS) for the NMOS transistors.”). Here, the first connecting segment (red box) and the gate electrode of the transistor MN2 (dark purple box) partially overlap. Therefore, an insulation layer between the metal layers is necessary to avoid electric shorting between the terminals (Out+ and Out-). EX-1003, ¶ 144:



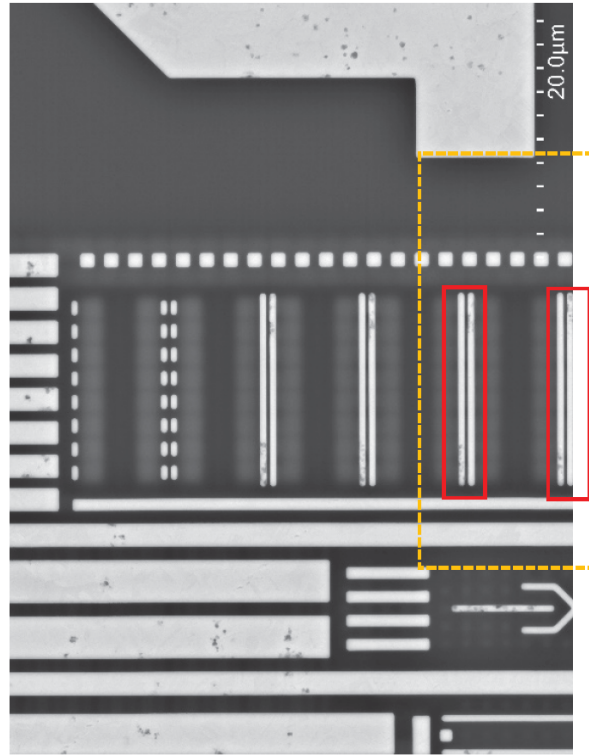
Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶ 144. It would have been obvious to a POSITA that cross-layer electric connections, where needed, can be readily formed using vias or other interconnect structures. *Id.*, ¶ 145. Vias may be used to connect the first connecting segment of the fine-tuning varactor to the left extension-conductor segment of the inductor, so that both are connected to the terminal “Out-.” EX-1003, ¶ 145. Indeed, Gonzalez’s Fig. 9 illustrates vias (the vertical boxes located between Metal 1 and Metal 2) between two metal layers. *Id.*; EX-1005.008.

Further, it would have been obvious to a POSITA that Gonzalez’s fine-tuning varactor would naturally be arranged in an embedded manner on the other surface of the first insulation layer that is opposite the inductor. EX-1003, ¶ 146. Embedding electronic elements such as a capacitor component on the surface of an insulation layer was not new. As the 582 patent itself acknowledges, it was well known that “in order to reduce the volume of an electronic product, various electronic elements [such as capacitor components] are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).” EX-1001, [1:29-32]. Gonzalez teaches just that: “[i]mplementation in silicon allows single-chip integration of the millimeter-wave front end, thus enabling a dramatic reduction in size and cost.” EX-1005.004. A POSITA would therefore understand that Gonzalez does not use surface mount technology but

would instead implement its components in an embedded manner as the 582 patent admits was known and advantageous. EX-1003, ¶ 146.

Indeed, Realtek interprets this limitation as allegedly being met by a capacitor that is in a lower metal layer adjacent to an insulation layer. EX-1034.014 (stating that a “capacitor component” is located “in an embedded manner on the other surface (i.e., in the M9 layer adjacent to the first insulation layer), opposite to the inductor component, of the first insulation layer”). In addition, Realtek maps a capacitor component located on the same metal layers as the accused inductor component, as illustrated below. EX-1034.016 (showing capacitor connecting segments in red boxes which are located on the same metal layer as the coil and extension-connection segments of an inductor (the white shape touching the top of the gold box below):



Realtek Infringement Chart (EX-1034.016)

See EX-1003, ¶ 146; EX-1034.018

- vii. **“wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment”**

Gonzalez discloses this limitation. EX-1003, ¶ 147. Fig. 2 illustrates the fine-tuning varactor configured outwards relative to the coil-conductor segment of the inductor and not substantially overlapped therewith. Specifically, Fig. 2 illustrates spatial relationships and electrical connections among the inductor, the fine-tuning varactor (annotated in red shade), a digital control varactor bank

(annotated in blue shade), an NMOS cross-coupled transistor pair (annotated in yellow)—as well as two output buffers (annotated in green):

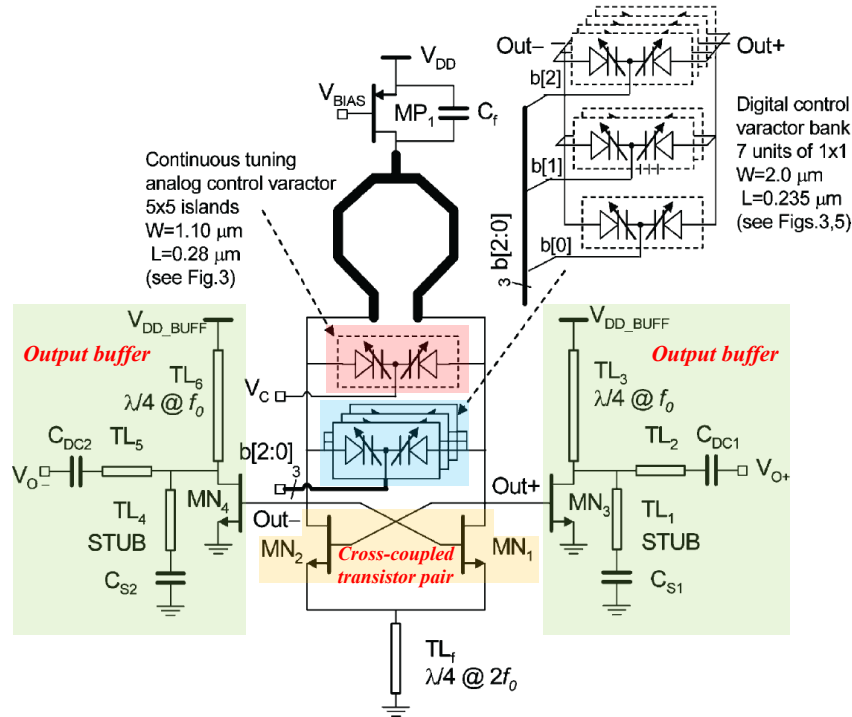
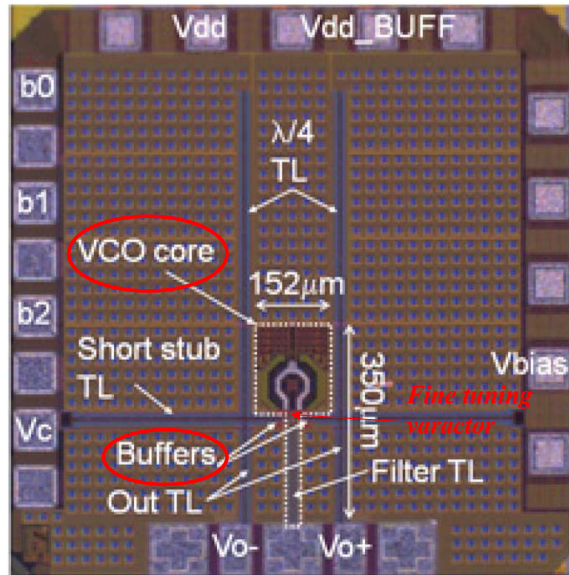


Fig. 2. VCO and output buffers schematic.

Gonzalez, Fig. 2 (EX-1005) (annotated)

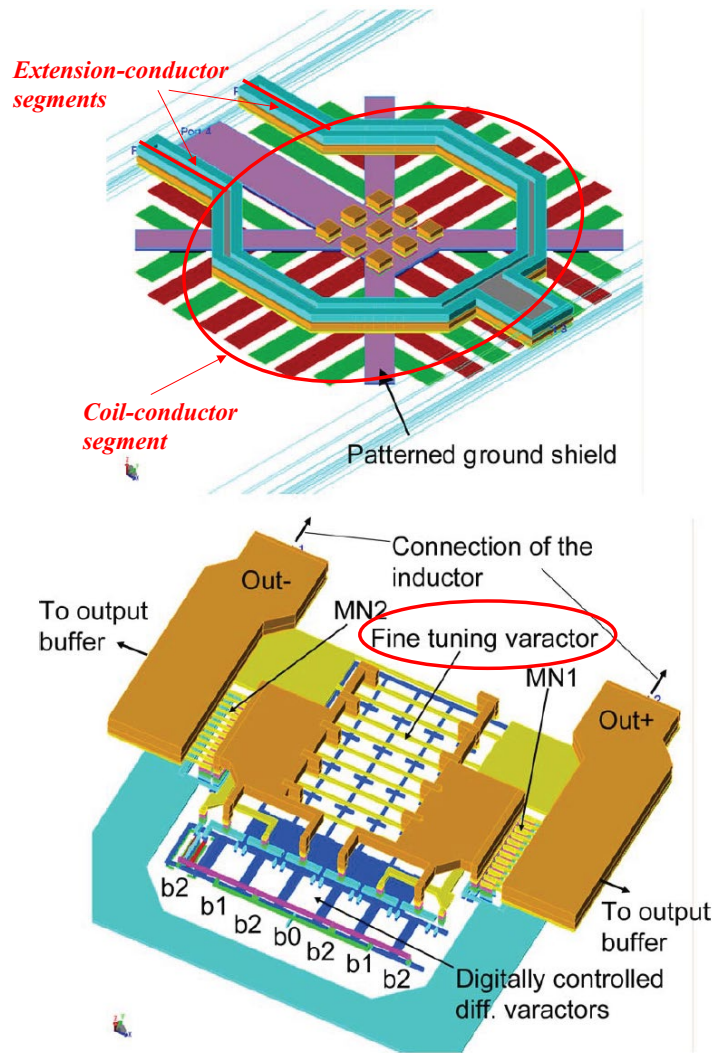
EX-1003, ¶¶ 148-150.

Gonzalez Fig. 12 also illustrates the same spatial arrangement in the VCO core as in Fig. 2. Although the fine-tuning varactor is not labeled in Fig. 12, a POSTITA would understand, in view of other discloses in Gonzalez (*e.g.*, Fig. 2 and Fig. 8), that the fine-tuning varactor (as part of the VCO core) would be placed under the extension segments of the inductor and generally between the two output buffers, as illustrated below. EX-1003, ¶¶ 151-152.



Gonzalez, Fig. 12 (EX-1005) (annotated)

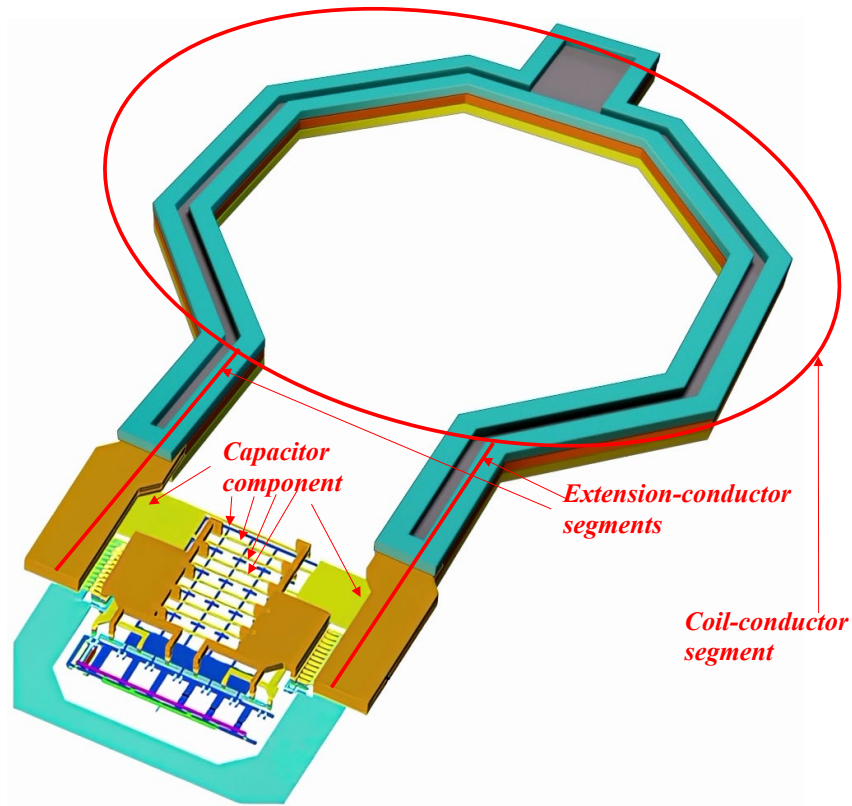
Similarly, Fig. 8 shows the fine-tuning varactor located under and between the “connection[s] of the inductor,” which are part of the extension segments of the inductor. Here, the fine-tuning varactor is correspondingly configured outwards relative to the coil-conductor segment of the inductor, and not substantially overlapped with the coil-conductor segment:



Gonzalez, Fig. 8 (EX-1005) (annotated)

EX-1003, ¶ 148. Consistent with Figs. 2 and 12, Gonzalez’s Fig. 8 shows how the fine-tuning varactor is arranged relative to the “connection of the inductor” and to two “output buffers.” Although Fig. 8 does not show the VCO core in a combined view, based on Gonzalez’s disclosures, a POSITA would be able to readily generate such a combined view. EX-1003, ¶ 152. A combination of the upper and bottom halves of Fig. 8 as understood by a POSITA is depicted below. As is clear

from the combined view of Fig. 8, Gonzalez's capacitor component (the fine-tuning varactor) is correspondingly configured outwards relative to the coil-conductor segment and is not substantially overlapped with it:



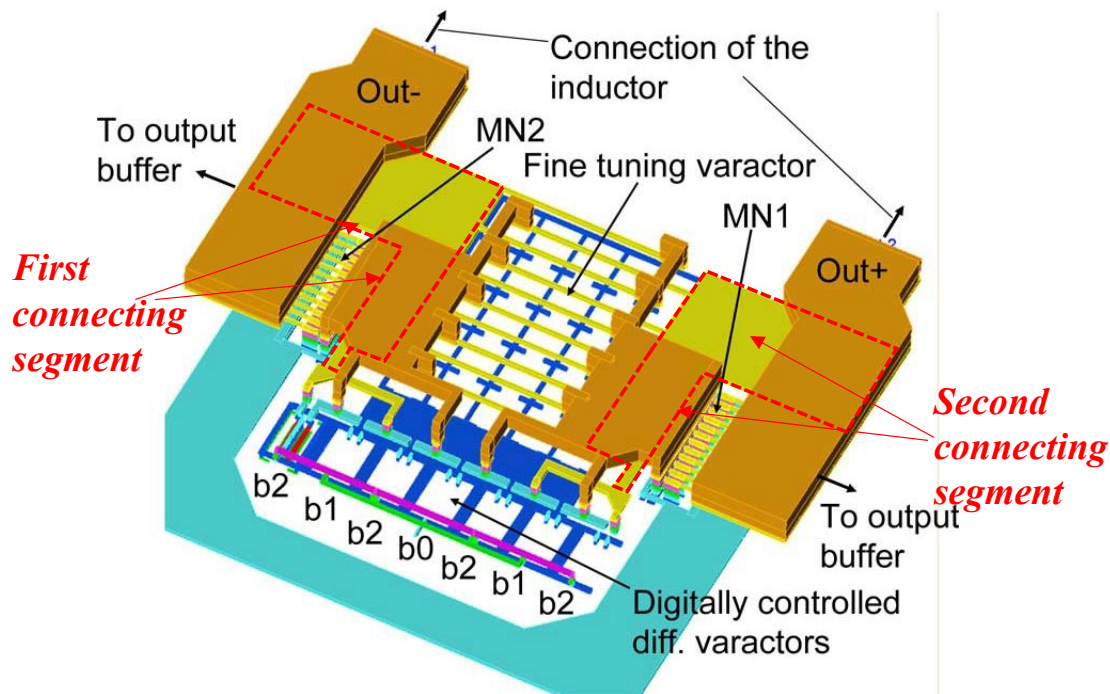
Gonzalez, Fig. 8 (modified) (EX-1005) (annotated)

EX-1003, ¶¶ 152-154.⁴ For all these reasons, a POSITA would understand that Gonzalez discloses, or at a minimum, renders obvious this limitation.

⁴ The modified Fig. 8 has removed the ground shield from the top half of the drawing and rotated the inductor into alignment with the bottom half of the

viii. “wherein the capacitor component comprises: a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and”

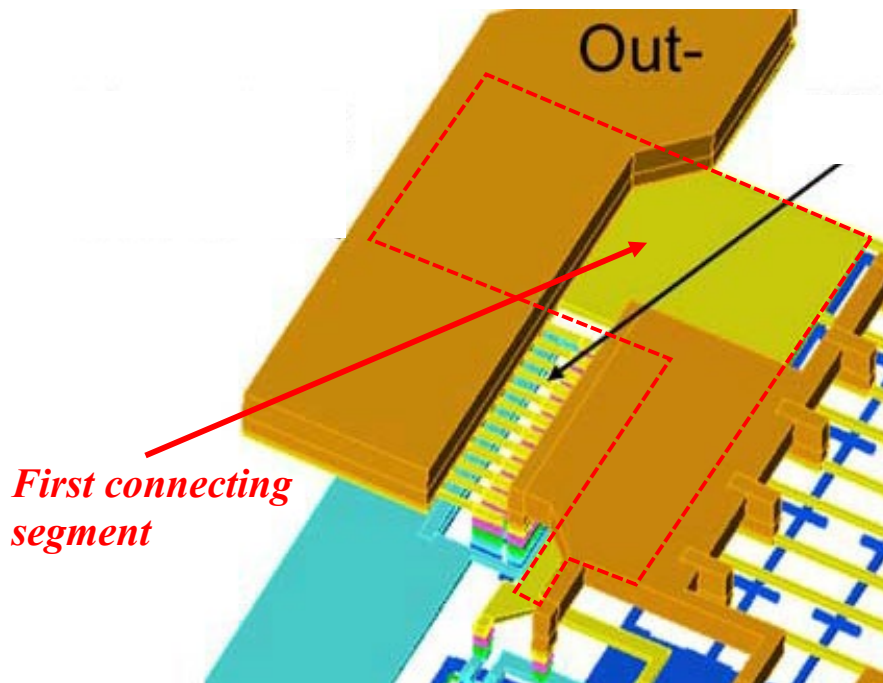
Gonzalez discloses this in Fig. 8, which shows that the fine-tuning varactor includes two (first and second) connecting segments shown in a yellow-gold color:



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

This is confirmed by zooming in on the first connecting segment:

drawing. Some text has also been removed to make the drawing easier to see. EX-1003, ¶ 152.



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶¶ 155-156. Although in Fig. 8 the full structure of the first connecting segment is partially hidden, a POSITA would recognize the above to be a reasonable interpretation of its shape. EX-1003, ¶ 156. Indeed, according to Gonzalez, the first connecting segment is connected to the inductor connector (Out-) (on the left) and is also connected to five of the ten thin fingers (on the right, in yellow) in the fine-tuning varactor made of 5x5 basic cells. EX-1005, Fig. 2 (“Continuous tuning analog control varactor 5x5 islands”), Fig. 5 (same); EX-1005.006; EX-1003, ¶¶ 156-158. Further, a POSITA would have recognized that the first connecting segment may be flexibly interpreted and its shape and/or size may take a different form such as a rectangle connected to two of the ten thin

fingers. Such a connecting segment would still constitute one of the claimed connecting segments in a “capacitor component.” EX-1003, ¶ 159.

The connecting segments of Gonzalez’s fine-tuning varactor extend corresponding to the two extension-conductor segments (*e.g.*, “connection of the inductor”) in a same direction. EX-1003, ¶ 157.⁵ Further, the connecting segments of Gonzalez’s fine-tuning varactor are respectively overlapped (at least partially) with the two extension-conductor segments in a vertical direction. *Id.*⁶

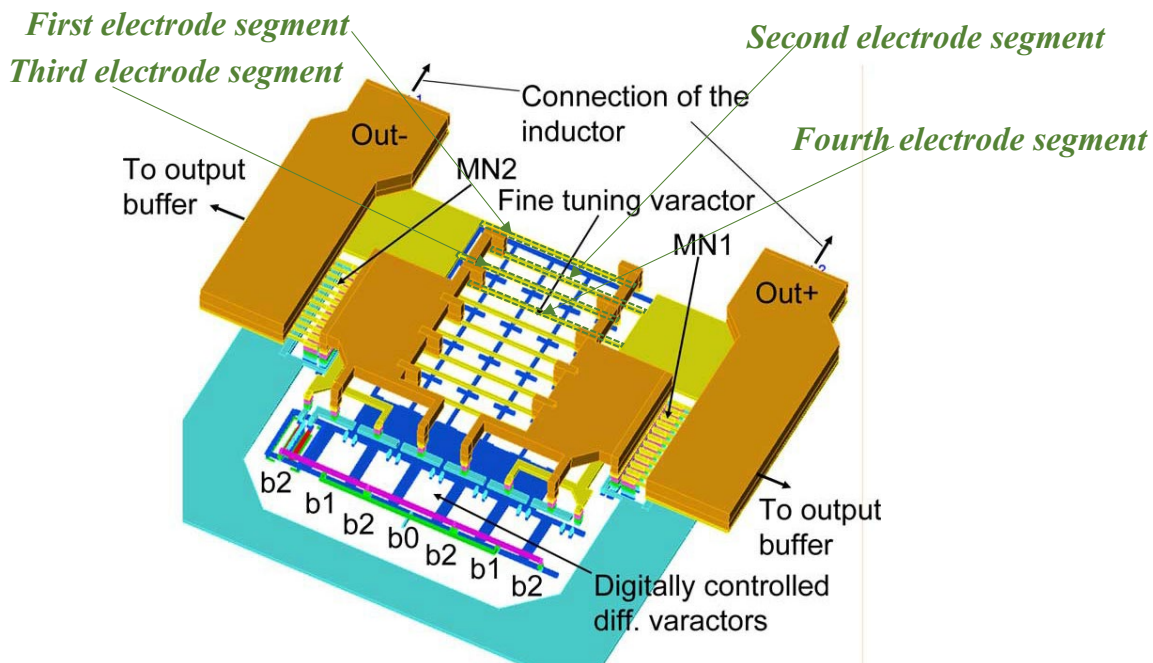
Finally on this limitation, the claimed structure of the capacitor component was not new. *Id.*, ¶ 160. The 582 patent acknowledges that the internal structures of its claimed capacitor component were “well known in the field.” EX-1001, [12:11-16].

⁵ In the annotated Fig. 8, the first and second connecting segments of Gonzalez’s fine-tuning varactor are marked by red dash lines. Parts of the connecting segments are hidden from view. EX-1003, ¶ 159.

⁶ In Gonzalez, the first and second connecting segments are used for receiving or transmitting signals. Through these connecting segments, “N+poly gates are each connected to one of the two differential terminals (Out+, Out-).” EX-1005.006. The differential terminals (Out+, Out-) provide output voltage signals of the VCO core. *Id.*; EX-1003, ¶ 158.

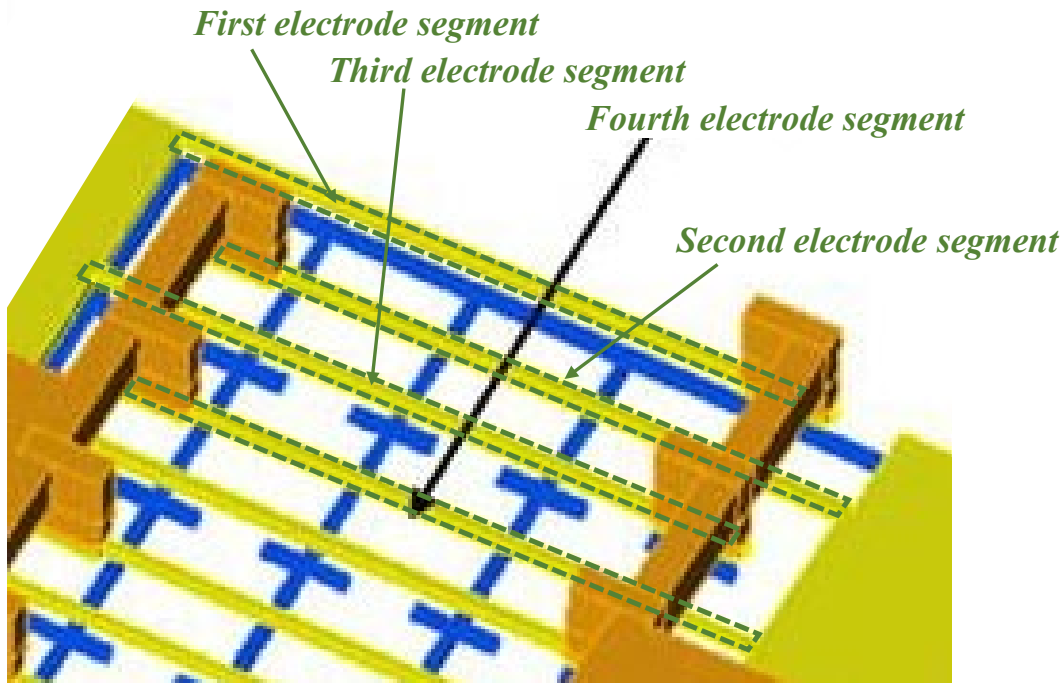
- ix. “a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.”

Gonzalez discloses this limitation. Gonzalez’s fine-tuning varactor includes a plurality of finger-shaped, interdigitated electrode segments on a metal layer shown in yellow color. Out of 10 such segments, four (first, second, third, and fourth) are fully visible and annotated in Fig. 8:



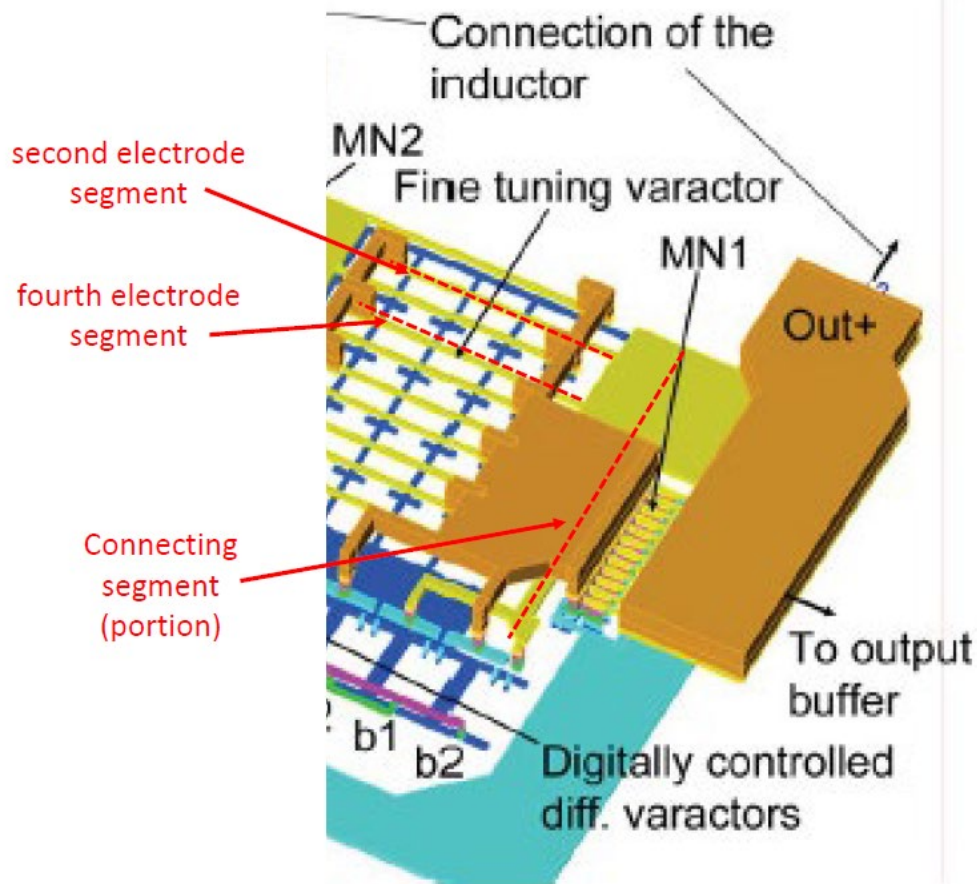
Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶ 161. Another zoomed-in view is reproduced below, illustrating the first, second, third, and fourth electrode segments of the fine-tuning varactor:



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

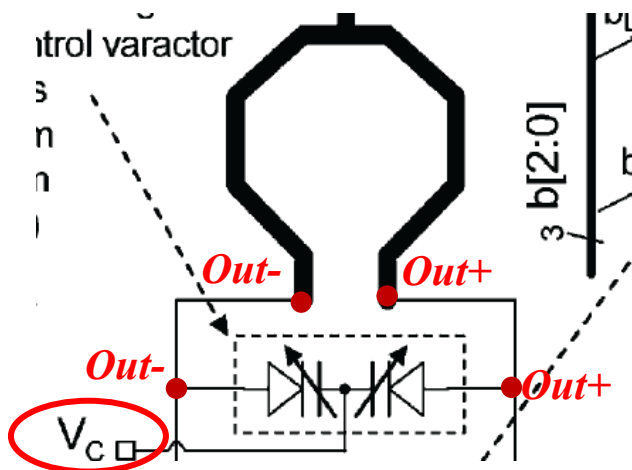
EX-1003, ¶ 162. One end of each of the electrode segments is coupled to one of the connecting segments. As shown above, the first and third electrode segments are each coupled to the first connecting segment, while the second and fourth electrode segments are each coupled to the second connecting segment. EX-1003, ¶¶ 163, 167. Further, as demonstrated in the below figure, the electrode segments (e.g., second and fourth, indicated by red dashed lines) extend laterally relative to the respective coupled connecting segment (indicated by another red dashed line) of the plurality of connecting segments:



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶ 169. In Gonzalez, the finger-shaped electrode segments serve as electrode plates in the fine-tuning varactor. As shown in Fig. 8, one set of finger-shaped electrode segments (e.g., first and third) is connected to terminal Out-, while the other set of finger-shaped electrode segments (e.g., second and fourth) is connected to terminal Out+. EX-1003, ¶ 169. *See also* Fig. 2 (reproduced below, showing two ends of the fine-tuning varactor are connected to Out- and Out+, respectively). The first and second sets of electrode segments are separated by a gap. Therefore, a voltage difference (i.e., Out+ and Out-) between the first and

second sets of electrode segments (e.g., between the first and second, or second and third, or third and fourth electrode segments) would cause a build-up of charge (Q) on the electrodes according to the capacitance between them. ($Q=CV$). *Id.*



Gonzalez, Fig. 2 (partial) (EX-1005) (annotated)

EX-1003, ¶¶ 163-164.

Gonzalez’s fine-tuning varactor has a “differential varactor structure” that “is made with two N+poly/Nwell varactors.” EX-1005.006. These are MOS varactors, which are variable capacitors that utilize MOS transistor structures. EX-1003, ¶ 165. The 582 patent acknowledges that the structures of MOS capacitors were “well known in the field.” EX-1001, [12:11-16]; EX-1003, ¶ 171. As shown in the 582 patent’s Fig. 12 (partially reproduced below), the capacitor component 150’—which is a “MOS capacitor”—includes finger-shaped electrode segments 155, 156, 157, 158, just like Gonzalez’s finger-shaped electrode segments. *Id.*, [12:16-23].

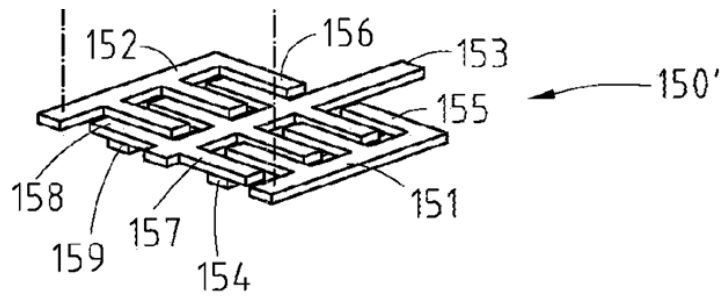
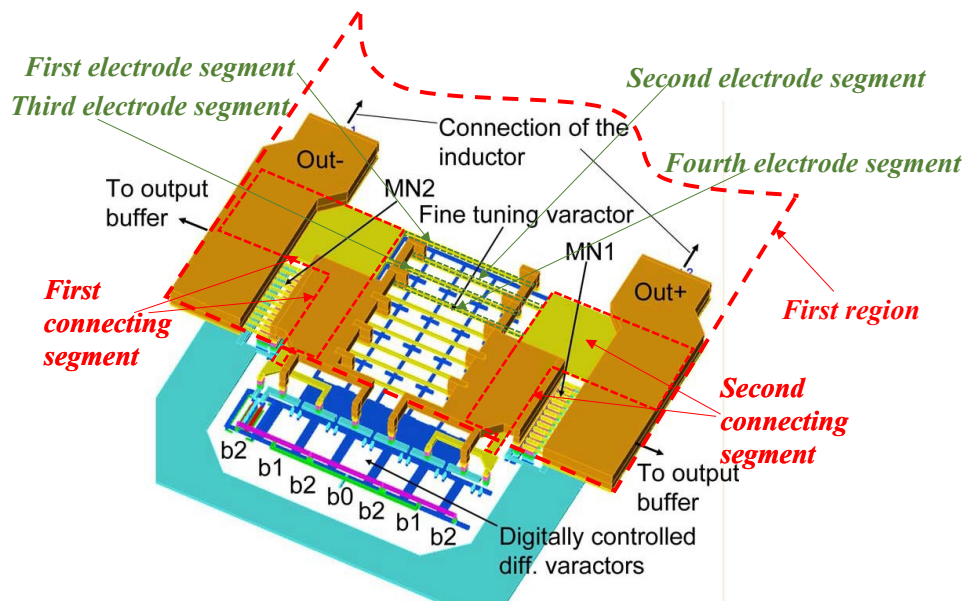


FIG. 12

582 Patent, Fig. 12 (partial) (EX-1001)

EX-1003, ¶¶ 165-166.

Finally, based on how Realtek interprets the term “first region,” Gonzalez’s electrode segments are located below the first region:



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶ 167.

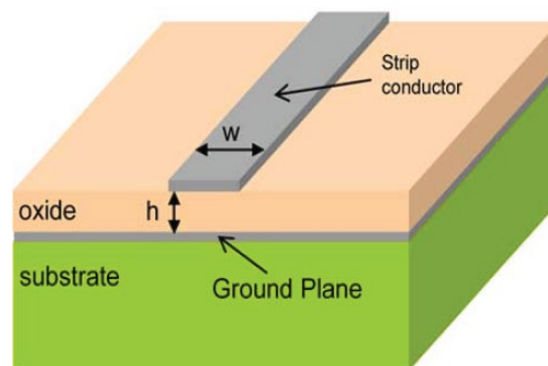
For these reasons, a POSITA would understand that Gonzalez renders obvious claim 1.

3. Gonzalez Invalidates Claims 2-5 and 9

a. Claim 2

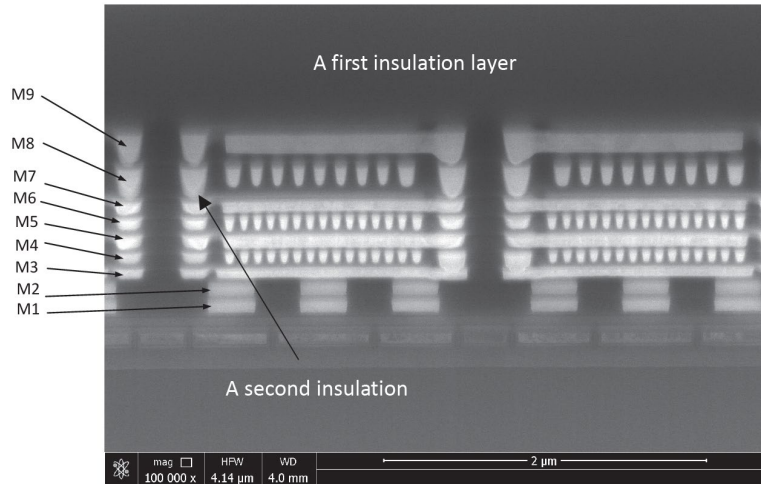
Claim 2 requires a “second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.” EX-1001, claim 2.

Gonzalez discloses this claim or, at a minimum, renders it obvious. Regarding the “second insulation layer,” Gonzalez discloses “a dielectric” material, shown as an “oxide” in Fig. 9. EX-1005.007-.008. This dielectric is located between a “top metal level (M6)” and “two bottom metal levels (M1+M2).” *Id.*, .008. A dielectric (e.g., oxide) is an insulation material that forms one or more insulation layers. EX-1003, ¶ 173. Thus, a POSITA would understand that part of Gonzalez’s dielectric material forms a second insulation layer:



Gonzalez, Fig. 9 (EX-1005) (annotated)

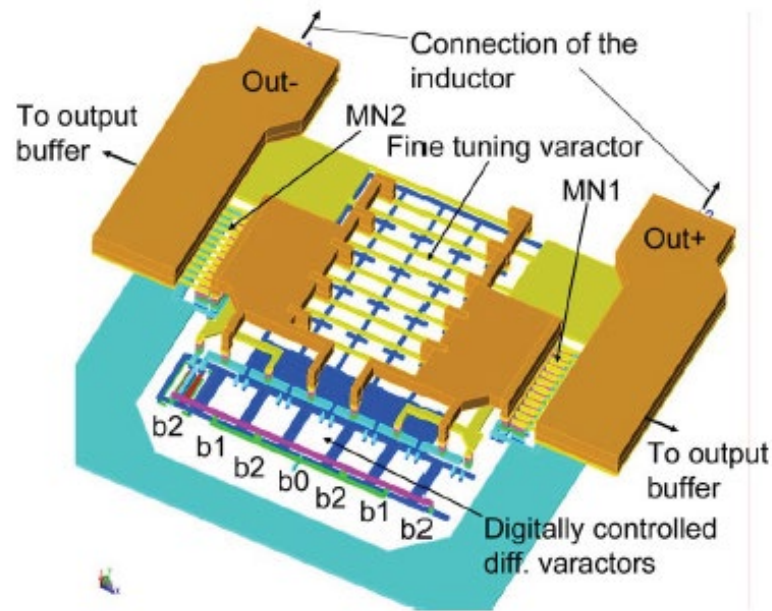
EX-1003, ¶ 173. This interpretation is consistent with how Realtek interprets the second insulation layer, as shown below:



Realtek Infringement Chart (EX-1034.020)

EX-1003, ¶ 174.

To the extent the second insulation layer is not expressly shown in Gonzalez Fig. 8, it would have been obvious to a POSITA to use a second insulation layer such that the capacitor component is sandwiched between the first insulation layer and the second insulation layer. *Id.*, ¶ 175. For example, as shown in Gonzalez's Fig. 8, in addition to a metal layer (in yellow) which includes connecting segments and electrode segments of the fine-tuning capacitor, Gonzalez also discloses an underlying metal layer (in blue) with capacitor components:



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

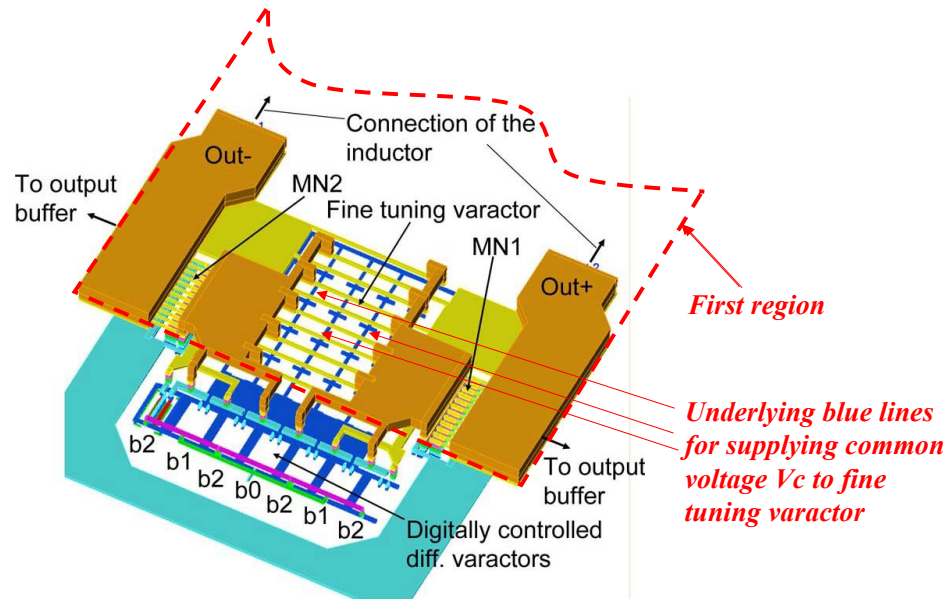
EX-1003, ¶ 176. A common voltage V_c can be applied onto the blue metal layer to tune a capacitance of the fine tuning-varactor. *See* EX-1005, Fig. 5, Fig. 8; *see id.*, .006-.007 (“The V_c signal of the varactor is directly connected to a digital signal that switches the varactor ON or OFF by applying 0 or 1.8V to the gate of the N poly/Nwell differential varactor.”). Since different voltages are applied to the overlapping blue and yellow metal layers, it would have been obvious to a POSITA to use a second insulation layer between the yellow and blue metal layers to avoid electric shorting (*e.g.*, between V_c and Out-, or between V_c and Out+). EX-1003, ¶ 176.

Further, as illustrated in the bottom half of Fig. 8, part of the blue metal layer also hosts “[a]n additional bank of digitally controlled differential varactors

[that] provides coarse tuning for PVT calibration using three bits (b_2 , b_1 , and b_0).” EX-1005.005. Gonzalez also discloses that its “discrete tuning in the VCO is implemented using a binary-scaled set of varactors composed of one, two, and four units controlled by b_2 , b_1 , and b_0 bits, respectively. The digitally controlled differential varactor unit cell has an ON/OFF capacitance and quality factor of 1.98 fF/0.54 fF and 4.5/16.5, respectively, at 60 GHz.” *Id.*, .007. Since Gonzalez discloses using both (1) the yellow metal layer as part of a fine-tuning varactor and (2) part of an underlying blue metal layer being a coarse tuning varactor bank, it would have been obvious to a POSITA to use a second insulation layer between the yellow and blue metal layers to avoid electric shorting between them. EX-1003, ¶ 177. As yet another benefit, the second insulation layer would help avoid electrical shorting between the fine-tuning varactor and the coarse tuning varactor. *Id.*

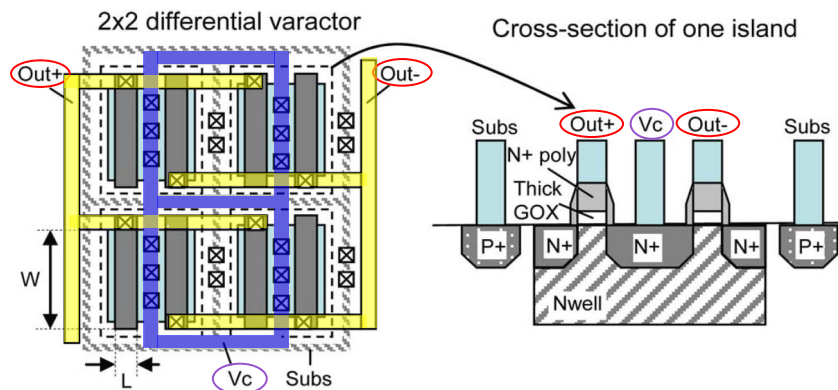
The second portion of claim 2 requires an “electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.” Gonzalez renders this limitation obvious. As shown in Fig. 8, the blue metal layer contains an electronic component on which a common voltage V_c can be applied to tune a capacitance of the fine-tuning varactor. *See* EX-1005.006-.007. Also, Gonzalez discloses a bank

of “digitally controlled differential varactors,” which also includes electronic components implemented on the blue metal layer.



Gonzalez, Fig. 8 (partial) (EX-1005) (annotated)

EX-1003, ¶ 178. Fig. 5, which shows a differential varactor made of four (2x2) varactor units, also illustrates the common voltage Vc being applied onto an underlying metal layer (annotated in dark blue below to imitate coloring in Fig. 8):



Gonzalez, Fig. 5 (partial) (EX-1005) (annotated)

EX-1003, ¶ 179.

Based on how Realtek interprets the term “first region,” Gonzalez discloses at least one electronic component on the blue metal layer arranged corresponding to the first region on a surface, opposite to the capacitor component, of the second insulation layer. EX-1003, ¶ 180. Gonzalez discloses electronic components on the blue metal layer that are located directly under a yellow metal layer of the fine-tuning varactor, as shown in the bottom half of Fig. 8. *Id.*

Further, it would have been obvious to a POSITA that Gonzalez’s electronic component on the blue metal layer would be arranged in an embedded manner on the other surface of the second insulation layer that is opposite to its fine-tuning varactor. As explained with reference to claim 1, *see* Section IX.A.2.vi *supra*, embedding electronic components on the surface of an insulation layer was not new and would have been obvious to a POSITA. As the 582 patent itself acknowledges, it was well-known that, “in order to reduce the volume of an electronic product, various electronic elements are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).” EX-1001 [1:29-32]; EX-1003, ¶¶ 181-182.

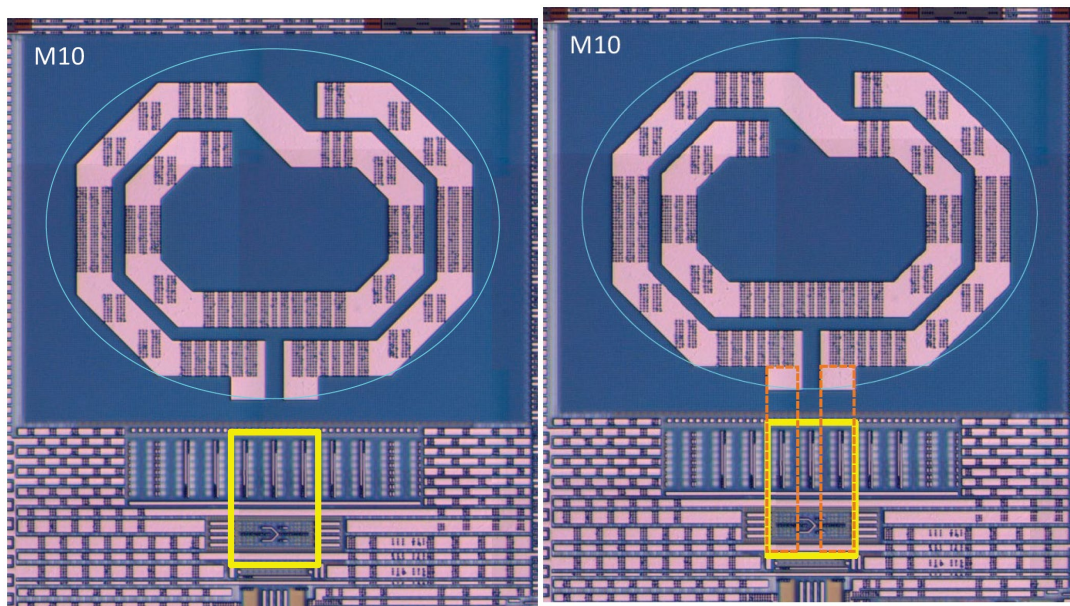
b. Claim 3

Claim 3 depends from claim 2 and specifies that the electronic component is “one of another capacitor component, a transistor component, a diode component, and a resistor component.”

Gonzalez discloses this claim. As shown in Fig. 8, a common voltage V_c can be applied on the blue metal layer to tune a capacitance of the fine-tuning varactor. See EX-1005.006-.007. Also, Gonzalez discloses a bank of “digitally controlled differential varactors,” which also includes electronic components implemented on the blue metal layer. Therefore, the electronic components implemented on the blue metal layer include at least another capacitor component (differential varactor). EX-1003, ¶¶ 183-184.

c. Claim 4

Claim 4 depends from claim 1 and requires that the “first region is defined between the two extension-conductor segments.” Realtek interprets this limitation as being the same as the first region in claim 1:



Realtek Infringement Chart, Claims 1 (left) and 4 (right) (EX-1034.013, .022)

Accordingly, Gonzalez discloses claim 4 to the same extent it discloses claim 1.

EX-1003, ¶¶ 185-186.

d. Claim 5

Claim 5 depends from claim 4 and requires that the “first region is defined between the two extension-conductor segments and the coil-conductor segment.” Gonzalez discloses this as well. To the extent that the first region is defined “between” the two extension-conductor segments and the coil-conductor segment, Gonzalez’s fine-tuning capacitor, which includes a capacitor component, would still be arranged corresponding to the first region, and a plurality of electrode segments in the fine-tuning capacitor would still be located below the first region. *See* Sections IX.A.2.v-vi, *ix supra*. EX-1003, ¶¶ 187-188.

e. Claim 9

Independent Claim 9 is identical to claim 1 except lacking the limitation “wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.” Therefore, for the same reasons as claim 1, Gonzalez renders claim 9 obvious. EX-1003, ¶¶ 189-190.

B. GROUND 2: Claims 1-5, 9 are Obvious Under 35 U.S.C. § 103 Based on Muh in View of Niknejad

1. Muh Introduction

Muh is a 2005 thesis submitted to the Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley. Muh's Research Advisor was Professor Niknejad. *See* EX-1006, EX-1007.

Muh discloses a VCO with an LC resonant circuit, shown below:

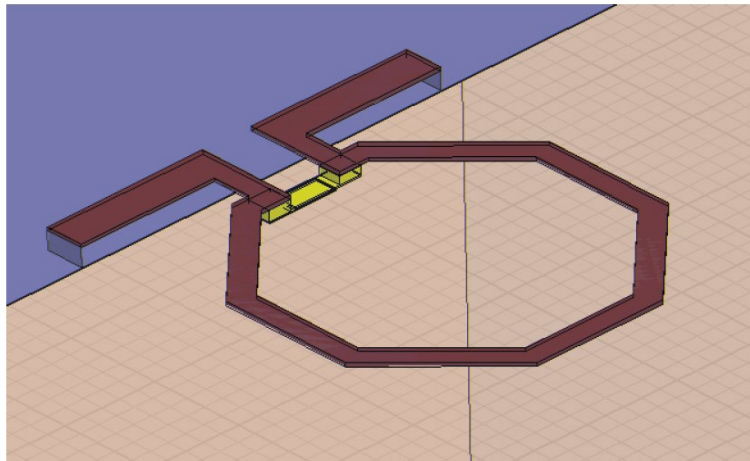


Figure B-3. HFSS model of parallel resonant tank on test chip.

Muh, Fig. B-3 (EX-1006.058)

Muh states that the LC resonant circuit includes an “inductor in parallel with a capacitor” and that in an actual test chip, the “capacitor is implemented as an interdigitated finger capacitor, with each finger comprising the bottom five metal layers strapped together.” EX-1006.057; EX-1003, ¶¶ 192-194.

2. Niknejad Introduction

Berkeley professor Niknejad has authored several books regarding semiconductor circuit design, including *mm-Wave Silicon Technology 60 GHz and Beyond* (“Niknejad”). EX-1007.

Niknejad explains that the book was “written for practicing RF and analog circuit designers.... The audience ... is assumed to be experienced in the field of analog/RF integrated circuits. The focus of each chapter is the key innovations and techniques that enable operation at mm-wave frequencies....” EX-1007.006.

Niknejad addresses inductors and capacitors, which are used extensively in resonant circuits. *Id.*, .025-.027. Niknejad states that “[f]inger (comb) capacitors, sometimes referred to as MOM (metal-oxide-metal) capacitors, can be easily fabricated in any modern CMOS process due to the abundance and high packing density of the metal layers.” *Id.*, .027. Niknejad explains that “[f]inger capacitors are composed of a large number of parallel fingers connected to either port of the device as shown in Fig. 3.11,” *id.*:

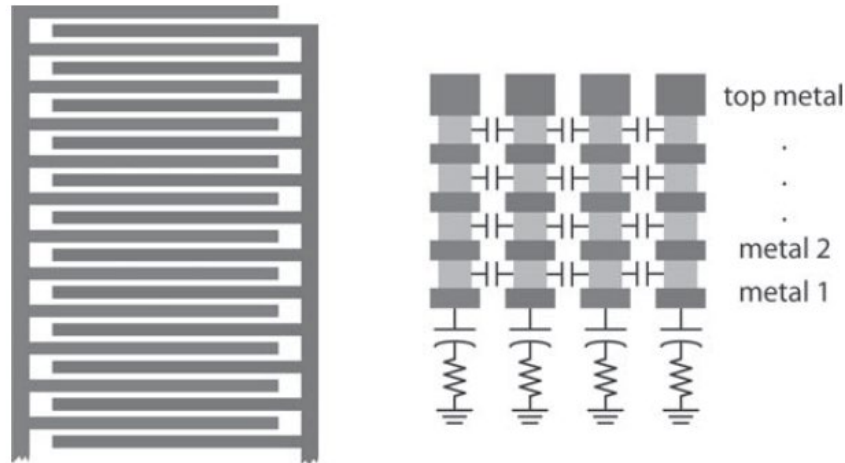


Fig. 3.11 Layout geometry of a “finger” or “comb” capacitor structure.

Niknejad, Fig. 3.11 (EX-1007.027)

Thus, fabrication of multi-layer finger capacitors was well-known before the 582 patent priority date. In one approach, “[e]ach finger consists of all available metal layers stacked on top of each other in order to decrease its resistance whi[le] increasing both its quality factor and the self-resonance frequency.” EX-1007.027. In Fig. 3.11, “[t]he metal layers are connected together through the maximum number of vias possible in order to take advantage of the additional via-to-via capacitance.” *Id.*

Muh discloses that, in the LC circuit in the test chip, “the capacitor is implemented as an interdigitated finger capacitor,” although the simulation model in Fig. B-3 shows a simple parallel-plate capacitor instead. EX-1006.057. To the extent Muh’s Fig. B-3 does not expressly show an interdigitated finger capacitor, as explained below it would have been obvious to a POSITA to use one by April

2014. A POSITA would have understood that an interdigitated finger capacitor (as disclosed by Niknejad) would easily replace the parallel-plate capacitor in Muh's Fig. B-3, as Muh teaches. EX-1003, ¶¶ 195-199.

3. Muh and Niknejad Invalidate Claim 1

i. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising: [preamble]

Muh contemplates using CMOS semiconductor technology, which a POSITA would have understood was (and is) used in most integrated circuits. EX-1006.006; EX-1003, ¶ 200. Muh further discloses a VCO containing an LC resonant circuit. Fig. B-3 shows a model of a “resonant tank on [a] test chip,” which is a semiconductor device. The model uses a high-frequency three-dimensional field solver (HFSS), which is a 3D software tool used for simulating ICs. EX-1006.057-.058.

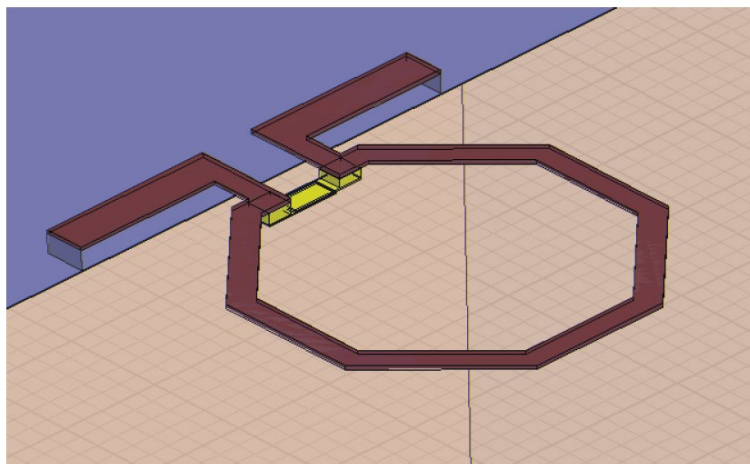
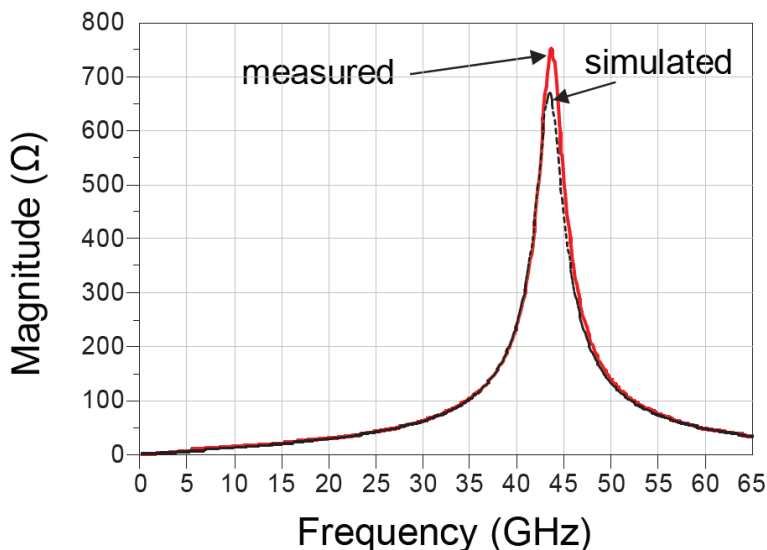


Figure B-3. HFSS model of parallel resonant tank on test chip.

Muh, Fig. B-3 (EX-1006.058)

EX-1003, ¶ 201. Muh notes that “[t]he second structure simulated in HFSS is a *resonant tank* consisting of the same *inductor in parallel with a capacitor*.” EX-1006.057. Further, Fig. B-4 shows the LC circuit’s resonating frequency:



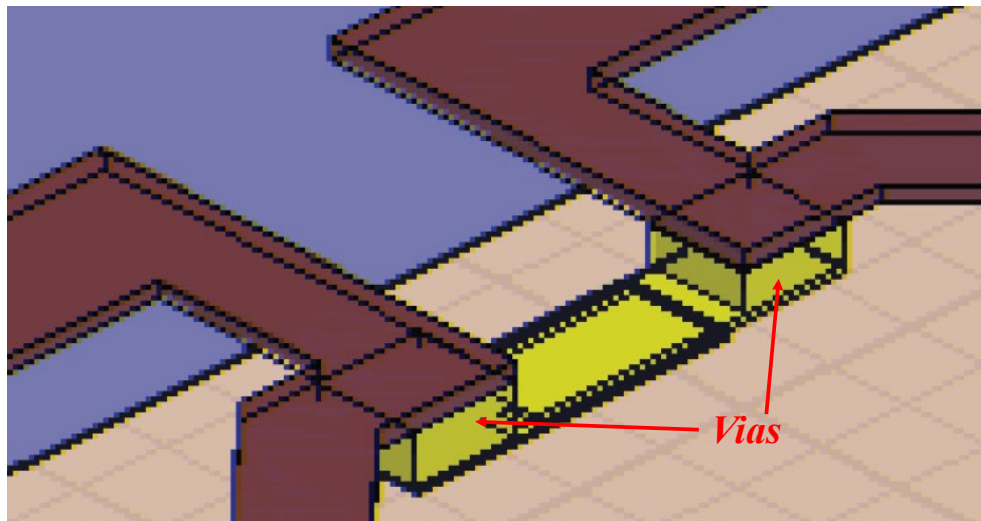
Muh, Fig. B-4 (partial) (EX-1006.058)

A POSITA would have understood Muh to disclose the inductor-capacitor (LC) resonant circuit of claim 1’s preamble. EX-1003, ¶ 202.

ii. “a first insulation layer”

Muh discloses that a “multi-layer dielectric stack was modeled with two layers: a passivation layer and an oxide layer.” EX-1006.041; *id.*, .056. As explained in Ground 1, Section IX.A.2.ii *supra*, a POSITA would have understood that a dielectric (*e.g.*, oxide) is an insulation material for forming one or more insulation layers. Therefore, part of Muh’s dielectric stack (*e.g.*, the oxide layer or a portion thereof) forms a first insulation layer. EX-1003, ¶ 203.

Fig. B-3 shows vias connecting an inductor to a capacitor in the LC resonant circuit. A POSITA would have understood that the vias, which are metal structures connecting stacked metal layers, would be implemented in and surrounded by an insulation layer. EX-1003, ¶¶ 62-65, 204. Therefore, to the extent Fig. B-3 does not expressly show a first insulation layer, a POSITA would have understood that there would be an insulation layer between a top metal layer (where the inductor is) and lower metal layers (where the capacitor is). The insulation layer would surround the vias shown in Fig. B-3. EX-1003, ¶¶ 204-205:



Muh, Fig. B-3 (partial) (EX-1006.058) (annotated)

The use of insulation layers and metal layers was well-known before the 582 patent priority date, as acknowledged therein. EX-1001, [1:24-28] (“A typical semiconductor integrated circuit includes a silicon substrate. *More than one insulation layer is arranged on the substrate, more than one metal layer [] is arranged in the insulation layer*, and the metal layers may be formed with a built-

in part of a chip by means of a semiconductor fabrication process.”). EX-1003, ¶ 206.

iii. “an inductor component, comprising”

Muh discloses in Figure B-1 a “loop inductor on test chip.” EX-1006.056.

Muh explains that the loop inductor utilizes “the top metal layer” of the semiconductor fabrication process. *Id.*:

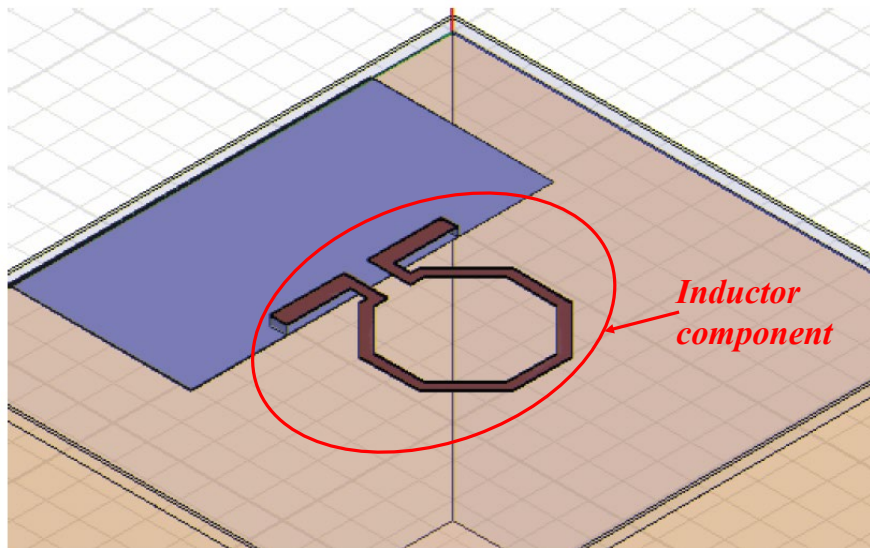


Figure B-1. HFSS model of loop inductor on test chip.

Muh, Fig. B-1 (partial) (EX-1006.056) (annotated)

Fig. B-3 also shows a “structure simulated in HFSS [which] is a resonant tank consisting of the same inductor in parallel with a capacitor.” EX-1006.057. A POSITA would have understood the inductors in Figs. B-1, B-3 are materially the same, with Fig. B-3 adding the parallel capacitor. EX-1003, ¶¶ 207-208:

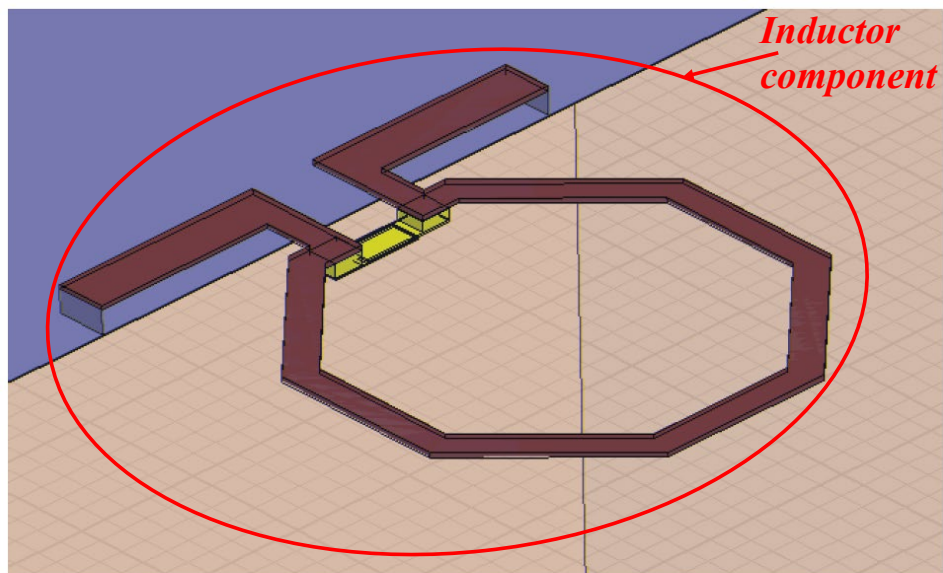
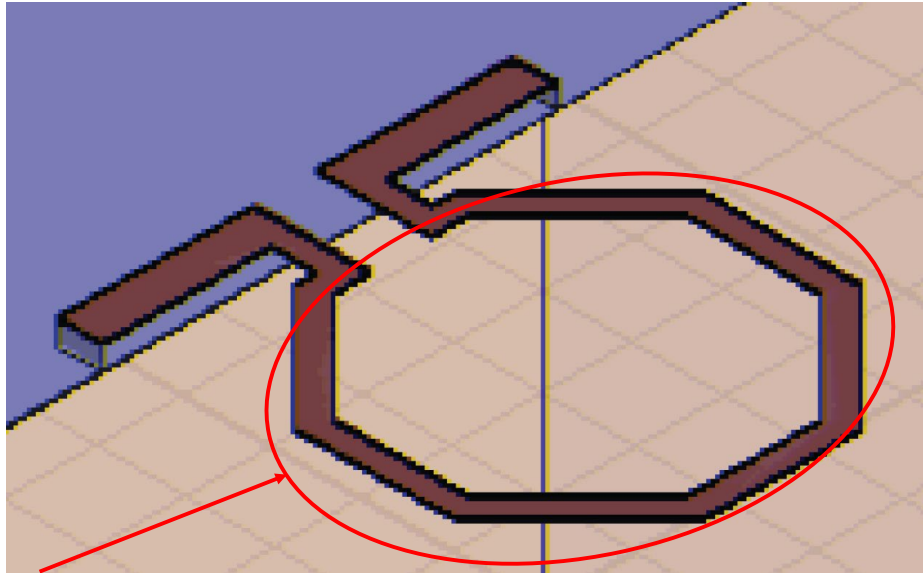


Figure B-3. HFSS model of parallel resonant tank on test chip.

Muh, Fig. B-3 (partial) (EX-1006.058) (annotated)

- iv. “a coil-conductor segment, located on a surface of the first insulation layer; and”

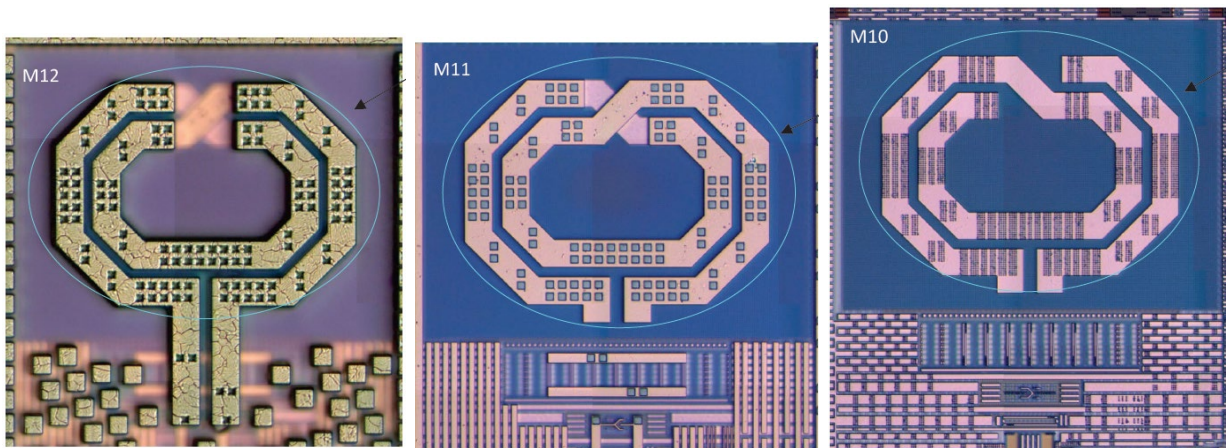
Muh discloses this, *see* Fig. B-1:



Coil-conductor segment

Muh, Fig. B-1 (partial) (EX-1006.056) (annotated)

EX-1003, ¶¶ 209-210. This is consistent with Realtek’s interpretation of this limitation, with the coil component circled in blue:



Realtek Infringement Chart (EX-1034.011-.012)

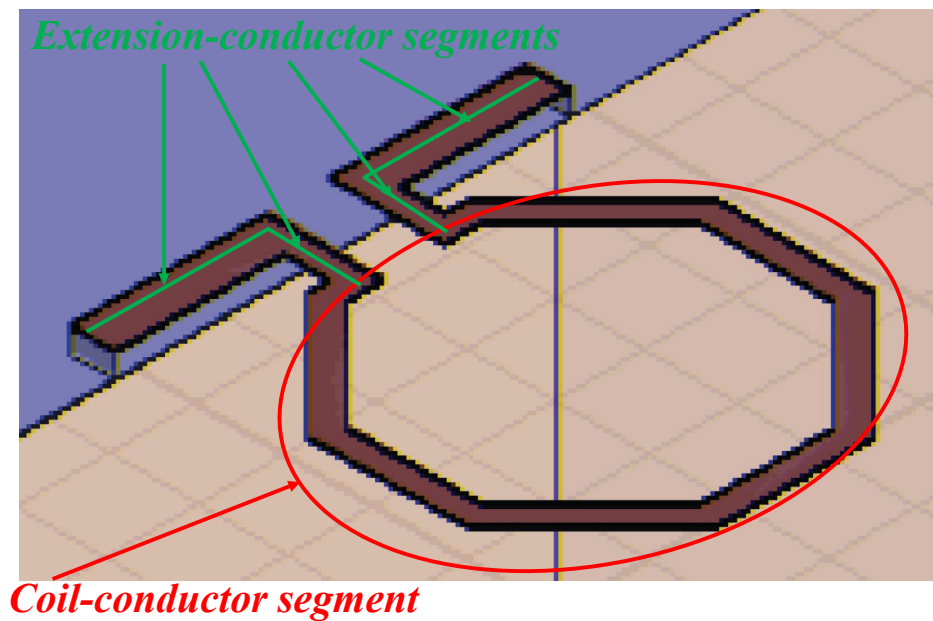
EX-1003, ¶ 211.

The coil-conductor segment of Muh’s inductor is located on a surface of the first insulation layer. *Id.*, ¶ 212. Muh explains that “the first structure is a loop

inductor *utilizing the top metal layer* of the process.” EX-1006.056. Further, as explained above with respect to the claimed “first insulation layer,” Muh’s Fig. B-3 shows vias connecting an inductor to a capacitor in the LC resonant circuit. EX-1003, ¶ 212. To the extent Fig. B-3 does not expressly show the first insulation layer, a POSITA would have understood that there would be an insulation layer located between the top metal layer (where the inductor is) and the lower metal layers and surrounding the vias. EX-1003, ¶ 212. Accordingly, a POSITA would have understood that the inductor’s coil-conductor segment would be located on a surface of the first insulation layer. *Id.* This is consistent with Realtek’s interpretation of this limitation. *See* EX-1034.010 (alleging that, in the accused products, “the coil-conductor segment is located on a surface of the first insulation layer (which is located approximately below the M10 layer)”); *see* EX-1001, [1:24-28] (“A typical semiconductor integrated circuit includes a silicon substrate. *More than one insulation layer is arranged on the substrate, more than one metal layer ... is arranged in the insulation layer*, and the metal layers may be formed with a built-in part of a chip by means of a semiconductor fabrication process.”); EX-1003, ¶ 213.

- v. “two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and”

Muh discloses this limitation, *see* Fig. B-1:

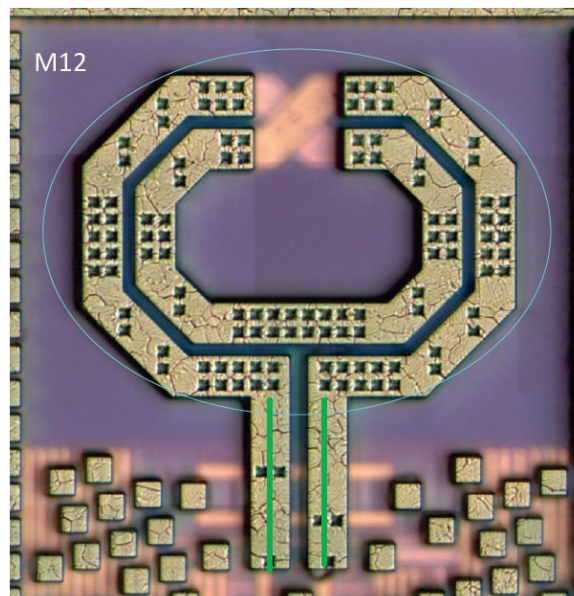


Muh, Fig. B-1 (partial) (EX-1006.056) (annotated)

EX-1003, ¶ 214. In Muh, the extension-conductor segments serve as input/output parts of the inductor. *Id.*, ¶ 215. They are described as “lumped ports” used to connect the inductor to other parts of Muh’s VCO. EX-1006.056; *id.*, .041-.044; EX-1003, ¶ 215.

The two extension-conductor segments are also located on the same surface of the first insulation layer. *Id.*, ¶ 216. Muh explains that its inductor—including its coil conductor segment and extension-conductor segments—utilizes “the top metal layer.” EX-1006.056. Further, as shown above, the two extension-conductor segments are coupled to two ends of the coil-conductor segment respectively, are arranged at an interval, and extend outwards relative to the coil-conductor segment as claimed. EX-1003, ¶ 216.

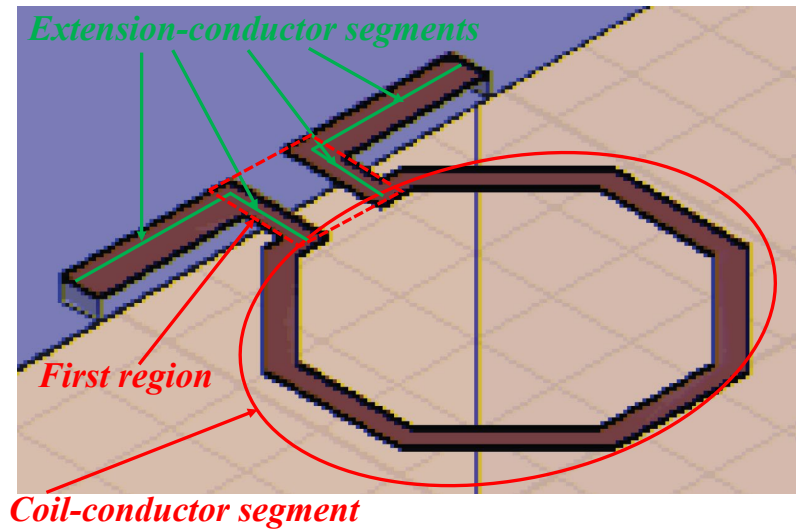
This is consistent with Realtek’s interpretation of this limitation as shown below, where the extension-conductor segments are marked by green lines:



Realtek Infringement Chart (EX-1034.012)

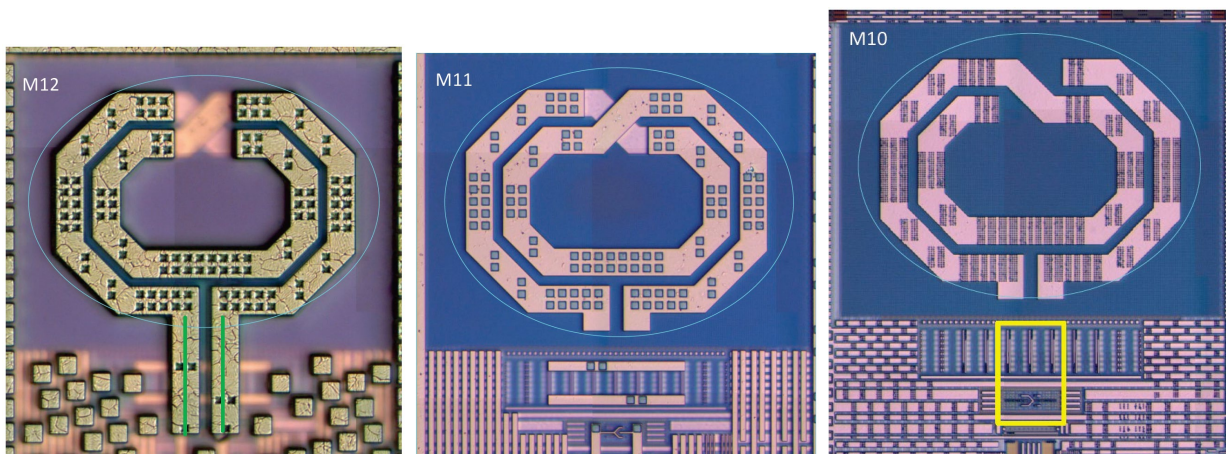
EX-1003, ¶ 217.

Further, based on how Realtek interprets the limitation “a first region defined by the two extension-conductor segments and the coil-conductor segment,” Muh discloses a first region (red dotted box), *see* Fig. B-1:



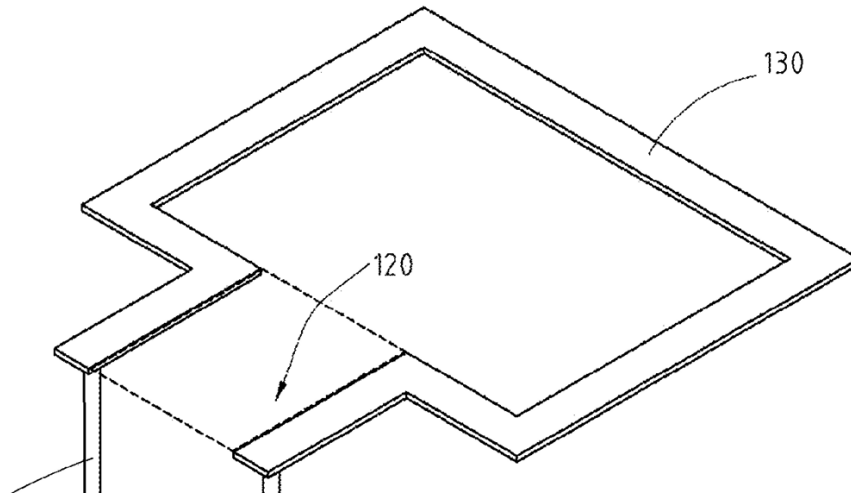
Muh, Fig. B-1 (partial) (EX-1006.056) (annotated)

This is consistent with Realtek’s interpretation of the claimed first region (yellow box):



Realtek Infringement Chart (EX-1034.012-.013)

EX-1003, ¶¶ 218-219. This is also consistent with the “first region” shown in the 582 patent. Fig. 6 (below) shows a “first region 120” “defined by the two extension-conductor segments” 133, 135 and the “coil-conductor segment” 131 (EX-1001, [3:45-47]):



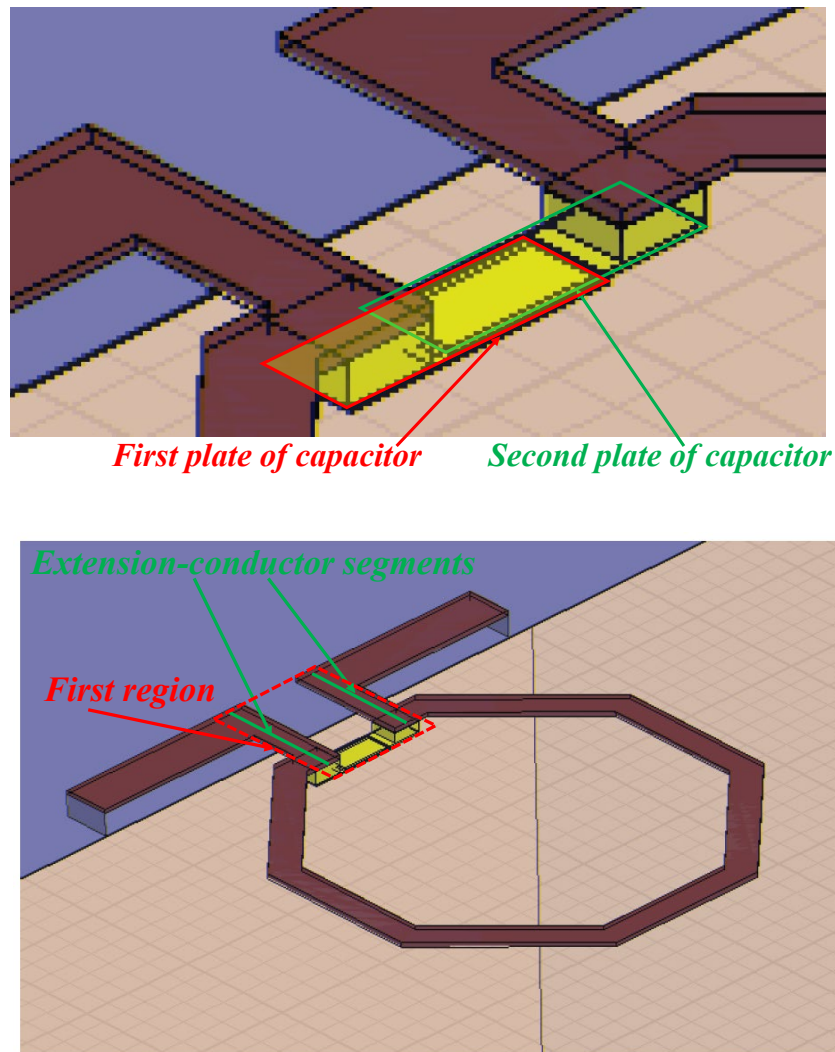
582 Patent, Fig. 6 (partial) (EX-1001)

EX-1003, ¶ 219. A POSITA would have also appreciated that, in Muh, the two extension-conductor segments extend away from the coil-conductor segment to each form an “L” shape, so the “first region” may also cover a wider area. *Id.*, ¶ 220.

- vi. **“a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer,”**

This limitation would have been obvious to a POSITA in view of Muh and Niknejad. EX-1003, ¶¶ 221-226. Muh discloses “a resonant tank” having an

“inductor in parallel with a capacitor.” EX-1006.057. The capacitor in Fig. B-3 is “a simple horizontal parallel-plate capacitor,” *id.*, which is or includes a capacitor component. EX-1003, ¶ 221. The two plates of the parallel-plate capacitor are illustrated below. Based on how Realtek has interpreted the term “first region,” Muh’s capacitor is arranged corresponding to the first region, as shown in Fig. B-3:



Muh, Fig. B-3 (partial) (EX-1006.058) (annotated)

EX-1003, ¶ 221.

To the extent Muh does not expressly disclose a first insulation layer with a surface on which the capacitor component is arranged in an embedded manner opposite to the inductor component, it would have been obvious to a POSITA to use a first insulation layer between the top metal layer (where the inductor is) and the lower metal layers (where the capacitor is). EX-1003, ¶ 222. This is consistent with Realtek’s interpretation. EX-1034.014 (stating that a “capacitor component” is located “in an embedded manner on the other surface (i.e., in the M9 layer adjacent to the first insulation layer), opposite to the inductor component, of the first insulation layer”). Accordingly, a POSITA would have understood that Muh’s parallel-plate capacitor is arranged on the other surface, opposite to the inductor component, of the first insulation layer. EX-1003, ¶ 222.

Embedding electronic elements such as a capacitor component on the surface of an insulation layer was not new. The 582 patent acknowledges that it was well-known that “in order to reduce the volume of an electronic product, various electronic elements [such as capacitor components] are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).” EX-1001, [1:29-32]. Muh likewise discloses the well-known technique of embedding metal structures in an insulation layer. EX-1006.042 (“In the setup on the left in Fig. 3-11, the ground ring is *embedded in the oxide* and does not touch the substrate.”). A POSITA would therefore understand that Muh’s

components are formed in an embedded manner as the 582 patent admits was known and advantageous. EX-1003, ¶ 223.

Additionally, Muh in combination with Niknejad renders this limitation obvious. Specifically, Muh explains that “[i]n the test chip, the capacitor is implemented as an *interdigitated finger capacitor*, with each finger comprising the bottom five metal layers strapped together.” EX-1006.057. Niknejad discloses such finger capacitors:

“Finger” (comb) capacitors, sometimes referred to as “MOM” (metal-oxide-metal) capacitors, can be easily fabricated in any modern CMOS process due to the abundance and high packing density of the metal layers. Finger capacitors are composed of a large number of parallel fingers connected to either port of the device as shown in Fig. 3.11. Each finger consists of all available metal layers stacked on top of each other in order to decrease its resistance whi[le] increasing both its quality factor and the self-resonance frequency. The metal layers are connected together through the maximum number of vias possible in order to take advantage of the additional via-to-via capacitance.

EX-1007.027; EX-1003, ¶ 224.

Therefore, it would have been obvious to a POSITA that a finger capacitor (*e.g.*, as disclosed by Niknejad) would easily replace Muh’s parallel-plate capacitor

(e.g., by using Muh’s “bottom five metal layers” of its finger capacitor (EX-1006.057) as Niknejad’s “available metal layers” (EX-1007.027) for its finger capacitor). *Id.*, ¶ 225. Upon such replacement, the finger capacitor would include a capacitor component. *Id.*

Further, it would have been obvious to a POSITA to place the Niknejad finger capacitor in the same location as Muh’s parallel-plate capacitor such that the finger capacitor is arranged corresponding to the first region on the other surface, opposite to the inductor component, of the first insulation layer. EX-1003, ¶ 225. A POSITA would understand that the top metal layer of the finger capacitor is an example of “a capacitor component” that meets this claim limitation:

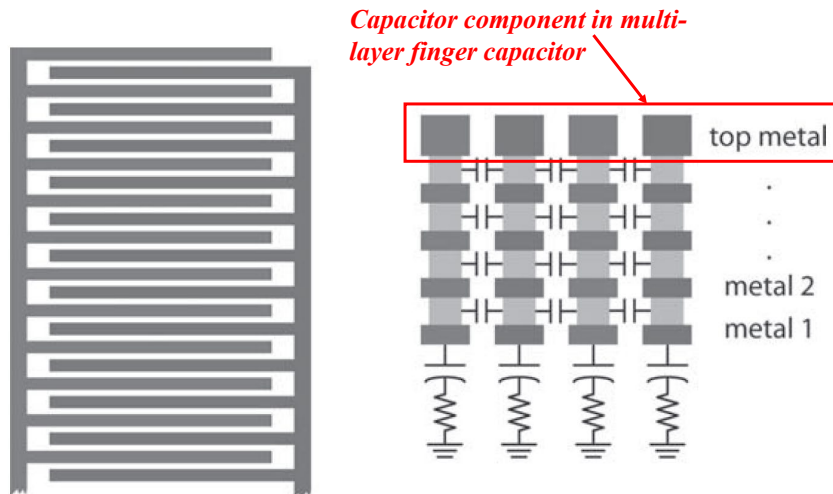


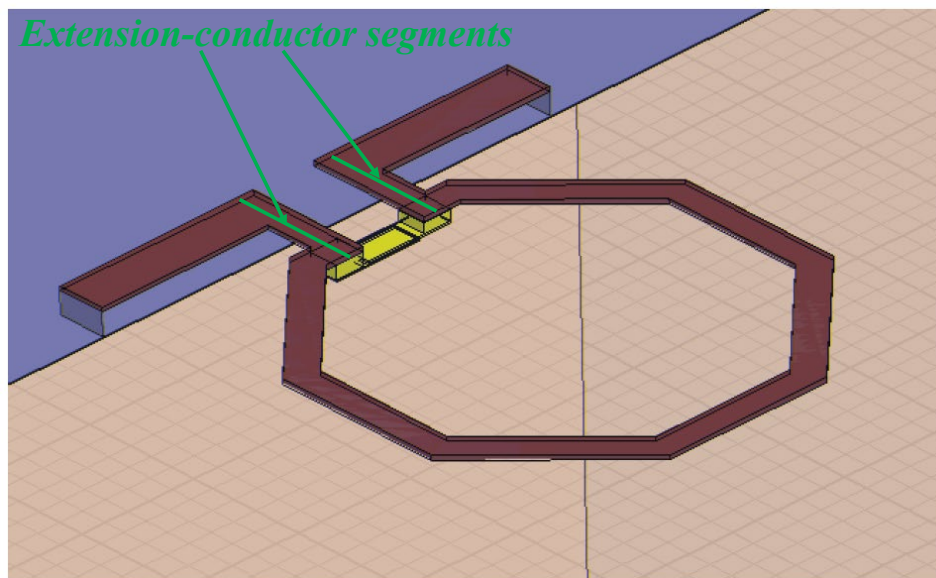
Fig. 3.11 Layout geometry of a “finger” or “comb” capacitor structure.

Niknejad, Fig. 3.11 (EX-1007.027) (annotated)

EX-1003, ¶ 226; *see* Section IX.B.4 *infra* (discussing motivation to combine Muh and Niknejad).

- vii. “wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment”

Muh discloses this limitation. Fig. B-3 shows a capacitor component configured outwards relative to the coil-conductor segment of Muh’s inductor. The capacitor component is not substantially overlapped with the coil-conductor segment:



Muh, Fig. B-3 (partial) (EX-1006.058) (annotated)

EX-1003, ¶ 228.

This interpretation is consistent with the 582 patent, which describes with reference to Fig. 9 that “the connecting segment 171 is overlapped with the corresponding extension-conductor segment 133.” EX-1001, [7:50-51]. Fig. 9 is

reproduced below where the capacitor connecting segment 171 (in red shade) on a bottom layer is vertically projected upward onto the inductor extension-conductor segment 133 (in green shade) on a top layer:

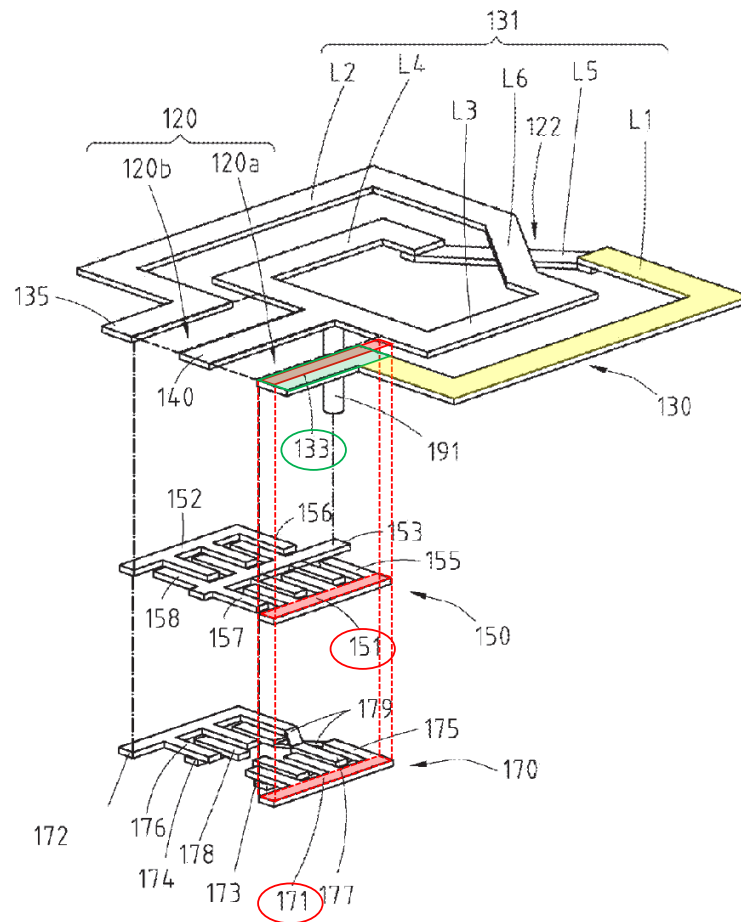


FIG. 9

582 Patent, Fig. 9 (EX-1001) (annotated)

EX-1003, ¶ 229. Notably, the 582 patent does not state that the capacitor connecting segment 171 is overlapped with the inductor coil-conductor segment 131 (in yellow shade). *Id.* To the contrary, the patent describes that the coil-conductor segment 131 stops at its first and second ends: “[t]he extension-

conductor segment 133 is joined to a first end of the coil-conductor segment 131 and is approximately perpendicular to a joining position between the extension-conductor segment 133 and the coil-conductor segment 131.” EX-1001, [4:1-9]; EX-1003, ¶ 230.

Therefore, a POSITA would understand that the coil-conductor segment 131 (in yellow shade) stops at “a first end” and does not include the area where “the connecting segment 171 is overlapped with the corresponding extension-conductor segment 133.” EX-1001, [4:1-9]; [7:50-51]; [4:62-64] (“The first connecting segment 151 may be located below the extension-conductor segment 133 and is overlapped with the extension-conductor segment 133.”). For the same reason, the coil-conductor segment 131 also stops at “a second end,” and does not include the area where “the connecting segment 172 is overlapped with the corresponding extension-conductor segment 135.” [7:52-53]; [4:64-67]; EX-1003, ¶ 231. This is illustrated in Fig. 8 of the 582 patent, showing a top view of the Fig. 9 circuit, but with connecting segments 171, 172 hidden under connecting segments 151, 152, respectively:

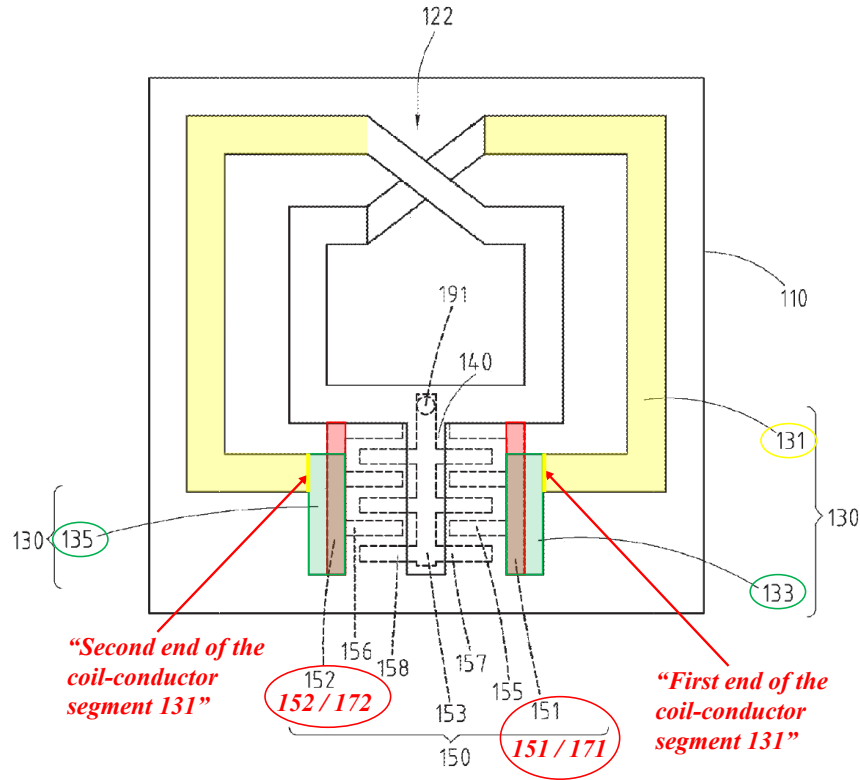
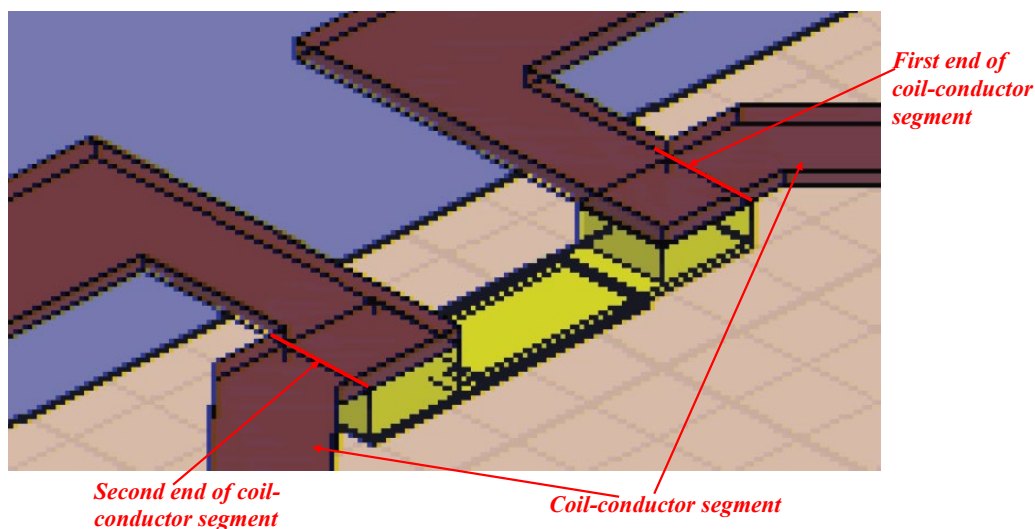


FIG. 8

582 Patent, Fig. 9 (EX-1001) (annotated)

EX-1003, ¶ 231.

Consistent with how the 582 patent describes its coil-conductor segment, Muh's coil-conductor segment stops at its first and second ends (which are illustrated in Fig. B-3 below by red lines) and does not include areas where Muh's connecting segments are overlapped with the underlying capacitor component. EX-1003, ¶ 232. Therefore, Muh's capacitor component is not overlapped at all, let alone substantially overlapped, with the coil-conductor segment of Muh's inductor:



Muh, Fig. B-3 (partial) (EX-1006.058) (annotated)

EX-1003, ¶ 232.

Even assuming *arguendo* that Muh’s capacitor component is partially overlapped with the coil-conductor segment of Muh’s inductor, a POSITA would recognize based on Fig. B-3 that the capacitor component is “not substantially overlapped” with its coil-conductor segment. EX-1003, ¶ 233. The 582 patent specification provides no objective measurements or boundaries to assist a POSITA in determining whether the capacitor component is “not substantially overlapped” with the coil-conductor segment. This limitation was added during prosecution of the 582 patent, and the only time the word “substantially” appears in the patent is in claim 1. *See* EX-1002.070, .074.

A POSITA would consider the word “substantially” in this context to be a term of degree, meaning, e.g., “most of” or “largely.” EX-1003, ¶ 234; *see* EX-

1035 (defining “substantially” as “being largely but not wholly that which is specified”). If the capacitor component was “substantially overlapped” with the coil-conductor segment, a POSITA would have understood that to mean that the capacitor component mostly or largely overlapped, that is, is most of the capacitor component overlapped with the coil-conductor segment. *Id.* As the claim requires “*not* substantially overlapped,” a POSITA would have understood that to mean that most of the capacitor component does not overlap with the coil-conductor segment. *Id.* This leaves open that at least a small portion of the capacitor component may overlap. Indeed, as shown in Figs. 8 and 9 of the 582 patent, capacitor components 150 and 170 are considered “not substantially overlapped” with the coil-conductor segment 131 even though portions of capacitor components 150 and 170 are located fully inside the coil-conductor segment 131 (in Fig. 8 below, *see* red shaded area that extends above segment 131). EX-1003, ¶ 234. Therefore, even assuming *arguendo* a small portion of Muh’s capacitor component is overlapped with the coil-conductor segment of the inductor, it is still “not substantially overlapped” with the coil-conductor segment. *Id.*:

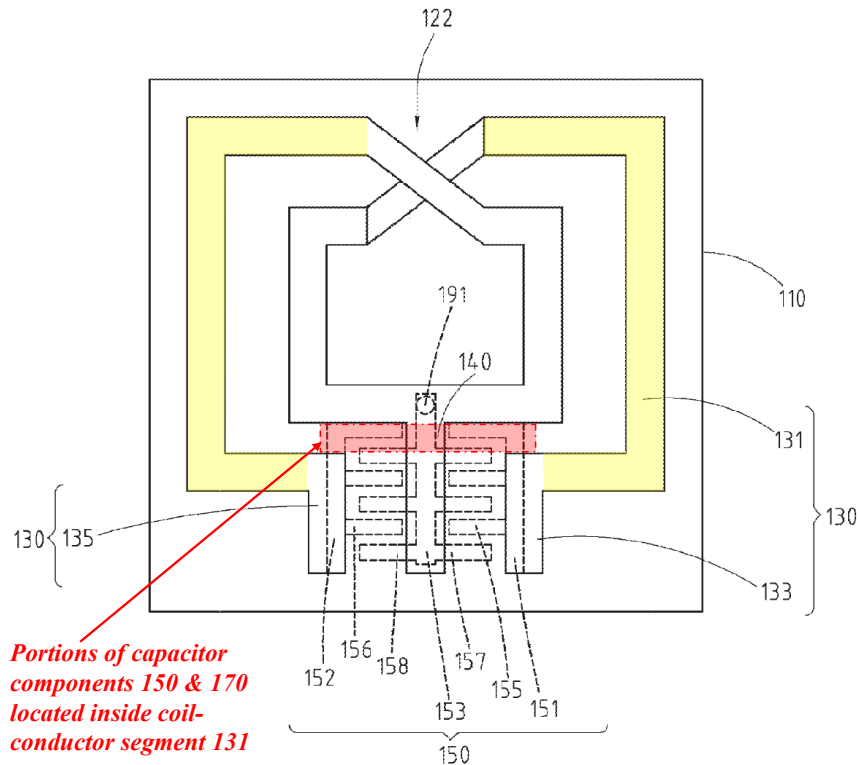
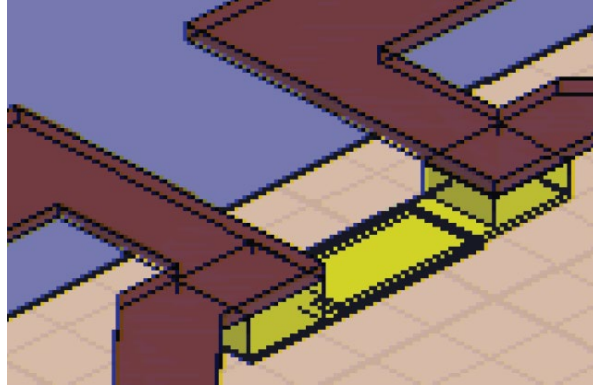
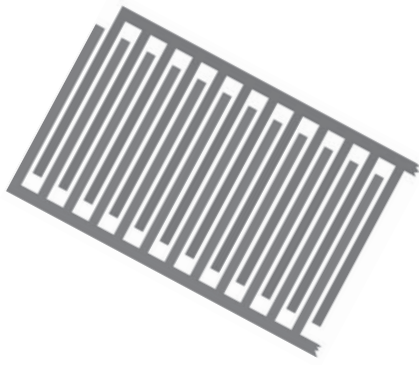


FIG. 8

582 Patent, Fig. 8 (EX-1001) (annotated)

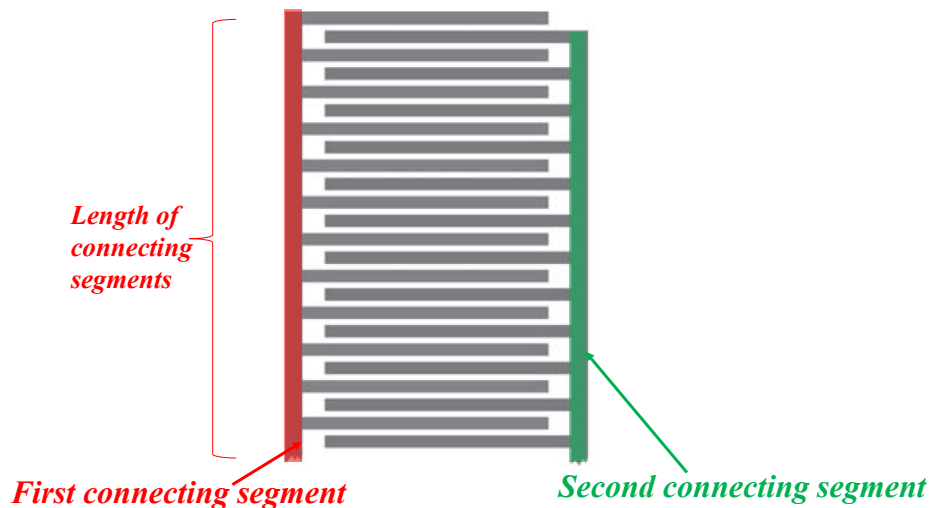
EX-1003, ¶ 234.

Additionally, Muh in combination with Niknejad renders this limitation obvious. *Id.*, ¶ 235. It would have been obvious to a POSITA to replace the parallel-plate capacitor of Muh's Fig. B-3 with a finger capacitor disclosed by Niknejad. The finger capacitor would be correspondingly configured outwards relative to the coil-conductor segment of Muh's inductor, and the finger capacitor would not be substantially overlapped with the coil-conductor segment of Muh's inductor, as illustrated below (EX-1003, ¶ 235):



Niknejad, Fig. 3.11 (partial, rotated) (left) (EX-1007.027);
Muh, Fig. B-3 (partial) (right) (EX-1006.058)

Niknejad's finger capacitor includes many fingers (*e.g.*, 24 fingers shown in Fig. 3.11). EX-1007.028. When numerous fingers—separated by gaps—are used as shown in Fig. 3.11 below, a POSITA would have recognized that the two (first and second) connecting segments would need to be relatively long to fit the fingers:

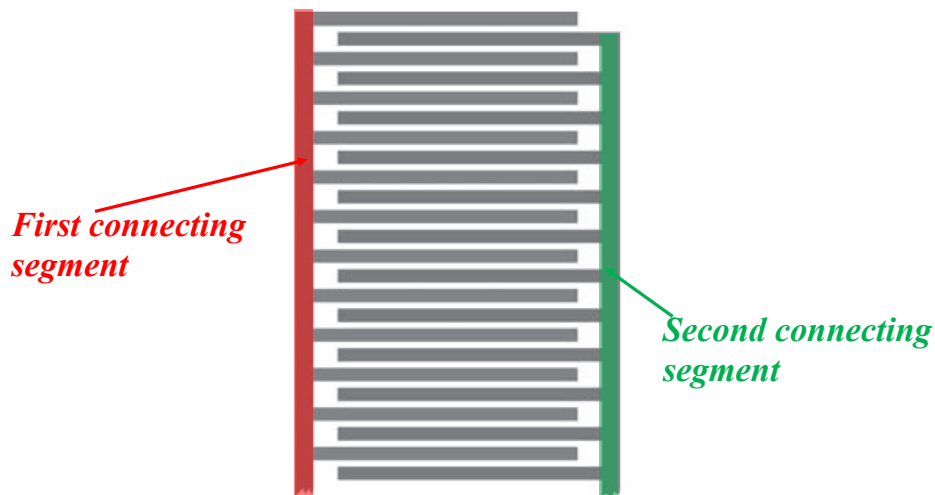


Niknejad, Fig. 3.11 (partial, rotated) (EX-1007.027) (annotated)

EX-1003, ¶ 236. When replacing Muh’s parallel-plate capacitor with Niknejad’s multi-finger capacitor, a POSITA would have understood that the finger capacitor would naturally extend further away from the core-segment of the inductor than Muh’s parallel-plate capacitor. *Id.* Therefore, the finger capacitor would be correspondingly configured even further outwards relative to the coil-conductor segment, and the Niknejad capacitor would not be substantially overlapped with the coil-conductor segment. *Id.*

viii. “wherein the capacitor component comprises: a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and”

It would have been obvious to a POSITA to replace Muh’s Fig. B-3 parallel-plate capacitor with Niknejad’s finger capacitor, as explained in Section IX.B.4 *infra*. EX-1003, ¶ 237. Niknejad’s finger capacitor (below) includes two (first and second) connecting segments:



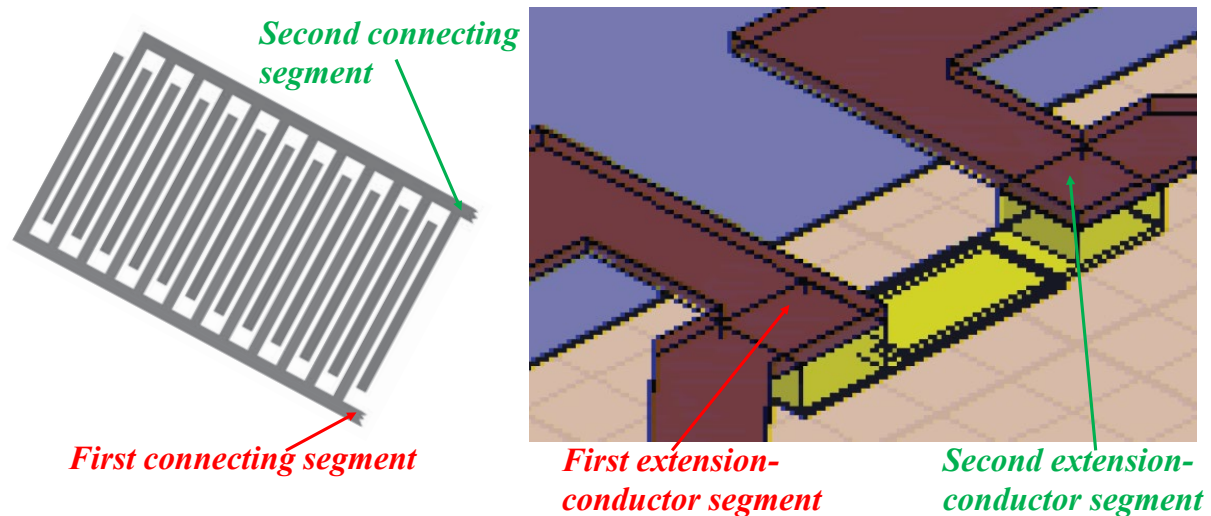
Niknejad, Fig. 3.11 (partial, rotated) (EX-1007.027) (annotated)

A POSITA would have recognized each connecting segment is a “port” used for receiving or transmitting signals such as from an inductor. EX-1007.027 (“Finger capacitors are composed of a large number of parallel fingers *connected to either port of the device* as shown in Fig. 3.11.”); EX-1003, ¶ 238.

Further, it would have been obvious to a POSITA that, when using a finger capacitor with Muh’s LC tank, the finger capacitor would be placed such that its two connecting segments extend corresponding to the two extension-conductor segments of Muh’s inductor in a same direction, and its connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction. EX-1003, ¶ 239. This would have been an obvious design choice that has a reasonable expectation of success. *Id.* Orientating the finger capacitor this way allows its connecting segments to be directly connected to the overlaying inductor using vias. *Id.* Muh already discloses vias between the inductor and the parallel-

plate capacitor, so it would have been obvious that the same or similar vias would be used to connect the finger capacitor to the inductor. *Id.*

As illustrated below, a POSITA would understand that a first connecting segment of Niknejad's finger capacitor would connect to a first extension-conductor segment of Muh's inductor through one or more vias. Likewise, a second connecting segment of Niknejad's finger capacitor would connect to a second extension-conductor segment of Muh's inductor through one or more vias:

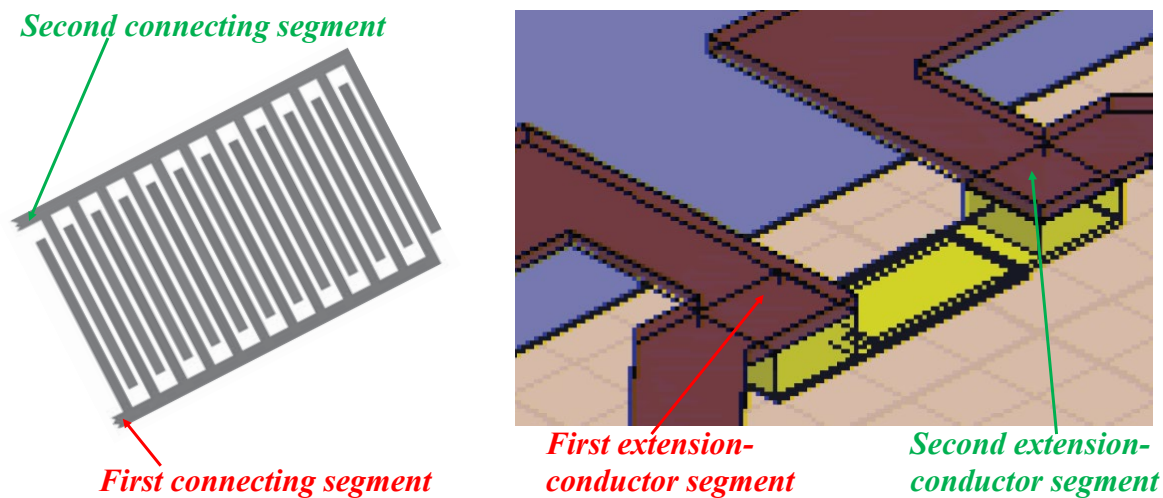


Niknejad, Fig. 3.11 (partial, rotated) (left) (EX-1007.027);
Muh, Fig. B-3 (partial) (right) (EX-1006.058) (annotated)

EX-1003, ¶ 239. This arrangement is the simplest and most reliable design choice.

Id., ¶ 240. As shown in Niknejad's Fig. 3.11, the finger capacitor can connect to other electronic components (*e.g.*, an inductor) from only one side of the finger capacitor (as shown by the red/green arrows in Fig. 3.11 above). EX-1003, ¶ 240.

Were the finger capacitor oriented differently (*e.g.*, being rotated by 90 degrees so that its connecting segments extend perpendicular to, rather than in the same direction as, the extension-conductor segments of Muh's inductor as shown below), extra horizontal metal traces would be needed in the lower metal layers to connect the finger capacitor to the overlaying inductor. EX-1003, ¶ 240.



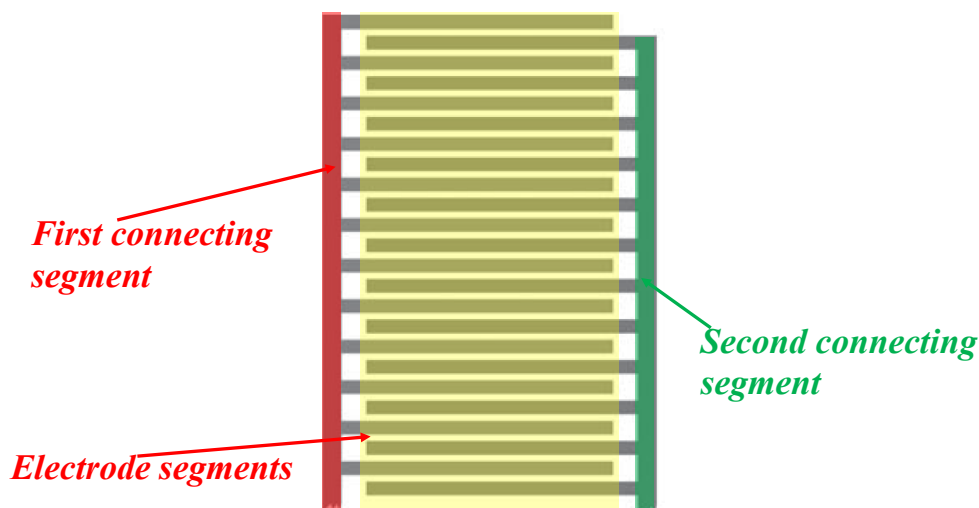
Niknejad, Fig. 3.11 (partial, rotated) (left) (EX-1007.027);
Muh, Fig. B-3 (partial) (right) (EX-1006.058) (annotated)

In this orientation, a horizontal metal trace is needed to connect the second connecting segment of the finger capacitor (located on the left-hand side) to the second extension-conductor segment of the inductor (located on the right-hand side). EX-1003, ¶ 240. Such extra metal traces not only increase fabrication costs but also involve additional fabrication processes which create more chances for issues and failures. *Id.* For these reasons, a POSITA would have understood to orient the finger capacitor such that the two connecting segments extend

corresponding to the two extension-conductor segments of Muh's inductor in a same direction, and its connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction. EX-1003, ¶¶ 239-241.

- ix. **“a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.”**

The combination of Muh and Niknejad renders obvious this limitation. EX-1003, ¶¶ 242-247. Niknejad discloses that finger capacitors have many “parallel fingers connected to either port of the device as shown in Fig. 3.11,” reproduced below. EX-1007.027:

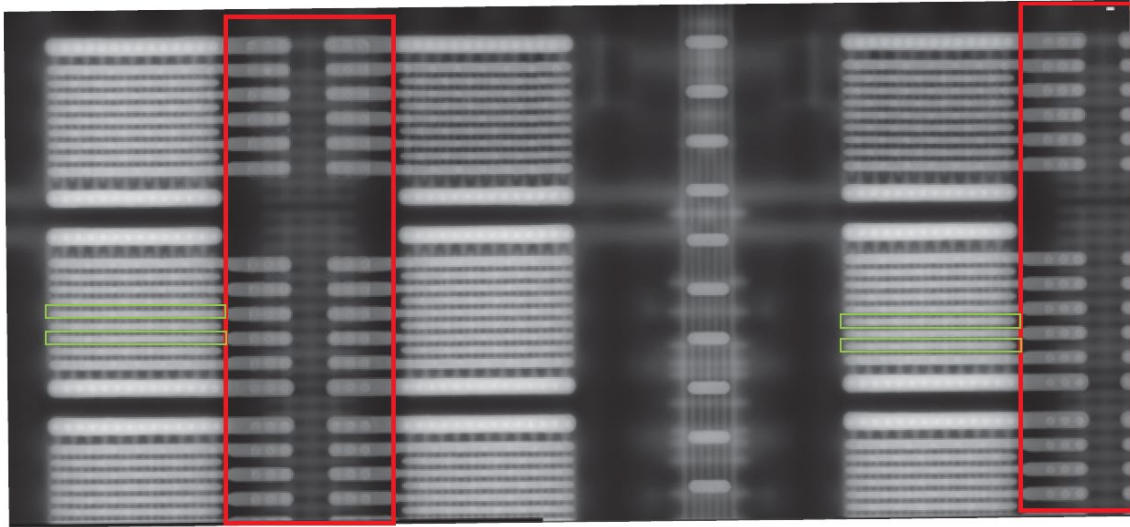


Niknejad, Fig. 3.11 (partial, rotated) (left) (EX-1007)

EX-1003, ¶ 242.

In Niknejad’s finger capacitor, each parallel finger includes an electrode segment. As shown above, one set of fingers is connected (“coupled”) to the first connecting segment on the left, while the other set of fingers is connected (“coupled”) to the second connecting segment on the right. The electrode segments are separated by a gap. The capacitance increases as the width of the gaps are decreased. EX-1003, ¶ 243; EX-1007.028. Each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments. EX-1003, ¶ 244.

When Niknejad’s finger capacitor is implemented into Muh’s LC tank, the electrode segments of the finger capacitor would be located below the claimed first region based on how Realtek interprets “the first region.” EX-1003, ¶¶ 245-246, *see* Section IX.B.3.vi *supra*. Indeed, the disclosures of Muh and Niknejad are consistent with how Realtek interprets this limitation, as shown below, where Realtek marks the plurality of electrode segments in green boxes and the plurality of connecting segments in red boxes.



Realtek Infringement Chart (EX-1034.019)

Finally, the disclosures of Muh and Niknejad are consistent with the 582 patent. The electrode segment structures of finger capacitors (*i.e.*, MOM capacitors) were not new. The 582 patent itself discloses MOM capacitors and acknowledges their structures were “well known in the field.” EX-1001, [12:11-16]; EX-1003, ¶ 247.

For these reasons, Muh in combination with Niknejad renders claim 1 obvious.

4. Motivation to Combine Muh and Niknejad

Before the 582 patent priority date, a POSITA would have been motivated to implement Niknejad’s finger capacitor into Muh’s LC resonant circuit for numerous reasons. EX-1003, ¶ 249. Foremost, it is explicitly proposed in Muh: “[i]n the test chip, the capacitor is *implemented as an interdigitated finger capacitor*, with each finger comprising the bottom five metal layers strapped

together.” EX-1006.057. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (holding that “the simple substitution of one known element for another” is likely obvious). Similarly, Niknejad discloses that each finger of such a design consists of all available metal layers stacked on top of each other, consistent with the disclosure in Muh. EX-1007.027; EX-1003, ¶ 249. The Niknejad capacitor is therefore the same type of capacitor taught by Muh. *Id.*

A POSITA would also have understood that fabricating such finger capacitors in Muh’s circuit was easily achieved. Niknejad teaches that finger capacitors “can be *easily fabricated* in any modern CMOS process due to the abundance and high packing density of the metal layers.” EX-1007.027. A POSITA would have therefore had a reasonable expectation of success in substituting Niknejad’s finger capacitor in Muh’s circuit. EX-1003, ¶ 250.

Next, Professor Niknejad was Matthew Muh’s Research Advisor who directly supervised him in the design of the LC resonant circuit. EX-1006.001. A POSITA reviewing Muh would naturally be motivated to review publications by Professor Niknejad covering related subject matter. EX-1003, ¶ 251. Indeed, Niknejad articulates that “[r]esearch in silicon mm-wave circuits and technology started at universities and research institutions and now continues in the commercial realm.” EX-1007.006. Further, the audience for Niknejad’s book was “assumed to be experienced in the field of analog/RF integrated circuits.” *Id.*

Finally, a POSITA would have readily understood the benefits of using a finger capacitor. Finger capacitors (*i.e.*, MOM capacitors) “are less expensive than Metal-Insulator-Metal (MIM) capacitors, which employ a sandwich structure with a thin high-K dielectric.” EX-1007.028. A POSITA would have understood the parallel-plate capacitor used in Muh’s simulation model is a type of MIM capacitor, as it employs a sandwich structure with a thin high-K dielectric. EX-1006.057 (“To obtain a similar value of capacitance as the finger capacitor, a high-k dielectric was sandwiched between the two plates.”); *see* Niknejad, EX-1007.026, Fig. 3.10 (showing an LC tank “formed by a ring inductor and MIM capacitors,” which is akin to Muh’s Fig. B-3). EX-1003, ¶ 252. Therefore, as taught by Niknejad, replacing Muh’s MIM capacitor with Niknejad’s MOM capacitor would also yield cost savings. *Id.*

A POSITA would have therefore been motivated to substitute Niknejad’s capacitor in Muh’s circuit, and would have expected success in doing so. *Id.*

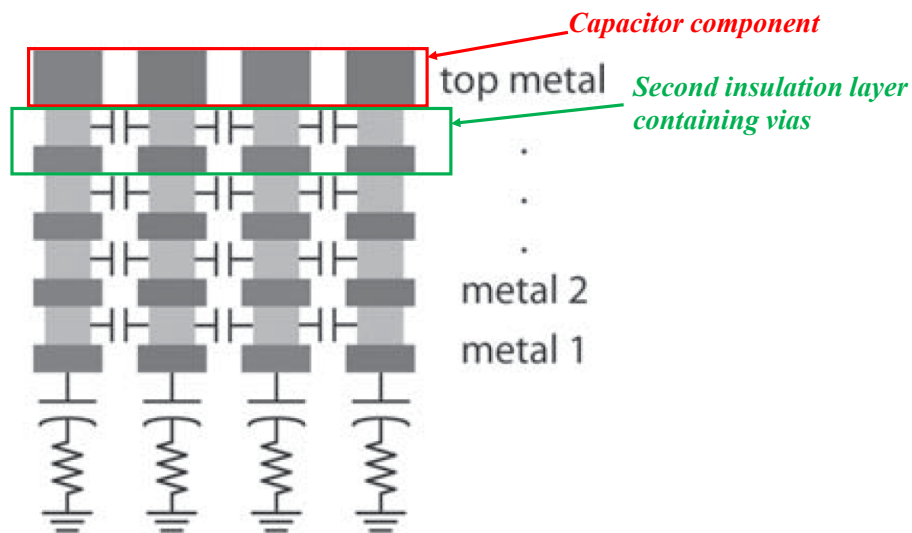
5. Muh/Niknejad Invalidate Claims 2-5 and 9

a. Claim 2

Claim 2 requires a “second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and an electronic component, arranged corresponding to the first

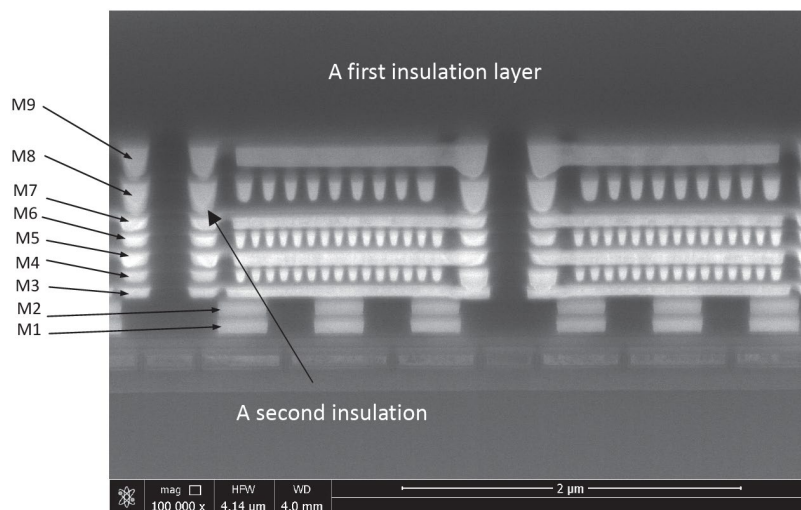
region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.” EX-1001, claim 2.

Muh/Niknejad discloses, or at a minimum, renders this claim obvious. In Niknejad’s multi-layer finger capacitor, “[e]ach finger consists of all available metal layers stacked on top of each other in order to decrease its resistance whi[le] increasing both its quality factor and the self-resonance frequency. The metal layers are connected together through the maximum number of vias possible in order to take advantage of the additional via-to-via capacitance.” EX-1007.027. A POSITA would have understood that the vias would be implemented in and surrounded by an insulation layer. EX-1003, ¶ 253. Specifically, the finger capacitor in Niknejad’s Fig. 3.11 would include a second insulation layer (*e.g.*, between the top metal layer and a lower metal layer), as illustrated below. The second insulation layer would contain and surround the vias between metal layers of the finger capacitor. The capacitor component located on the top metal layer would be sandwiched between the first insulation layer (not shown below) and the second insulation layer:



Niknejad, Fig. 3.11 (partial) (EX-1007.027) (annotated)

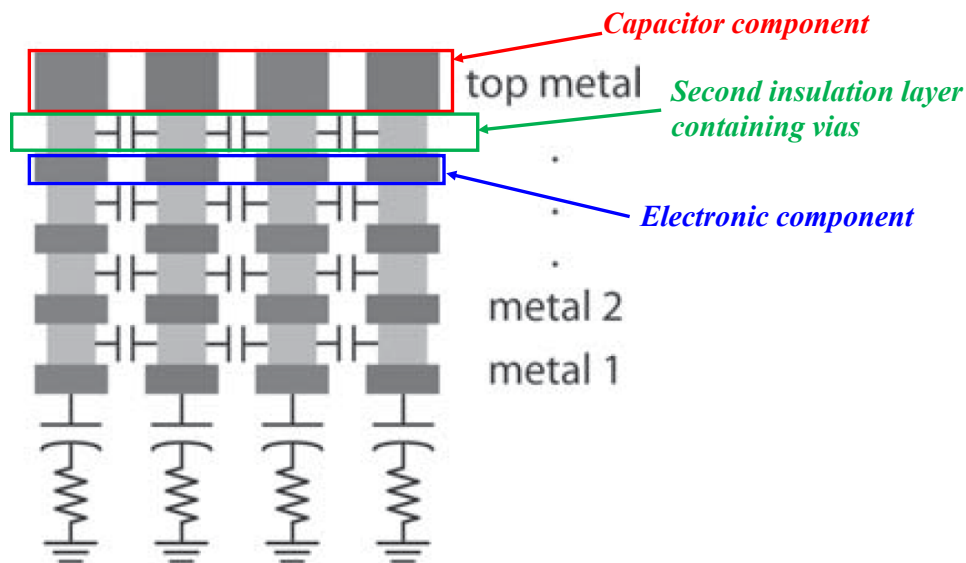
EX-1003, ¶ 253. This is consistent with Realtek’s interpretation of the second insulation layer (*id.*, ¶ 254):



Realtek Infringement Chart (EX-1034.020)

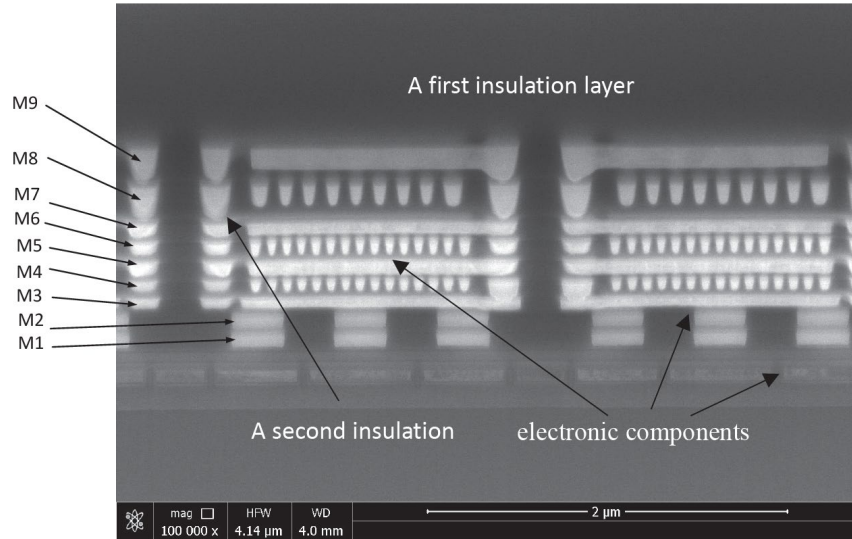
Next, Niknejad’s multi-layer finger capacitor includes an electronic component (*e.g.*, one of the fingers of the capacitor) on the second-topmost metal layer, as illustrated in Fig. 3.11 (below). EX-1007.027. The electronic component

on the second-topmost metal layer is arranged on a surface, opposite to the capacitor component (*i.e.*, in the top metal layer), of the second insulation layer:



Niknejad, Fig. 3.11 (partial) (EX-1007.027) (annotated)

EX-1003, ¶ 255. When Niknejad’s finger capacitor is implemented into Muh’s LC tank, the electronic component of the finger capacitor would be located below the claimed first region based on how Realtek interprets “the first region.” Likewise, as explained in section IX.B.3.vi *supra*, it would have been obvious to a POSITA to arrange the electronic component in an embedded manner on a surface of the second insulation layer. EX-1003, ¶ 256. As the 582 patent acknowledges, it was well-known that, “in order to reduce the volume of an electronic product, various electronic elements are arranged in an embedded manner in place of an arrangement manner adopting a surface mount technology (SMT).” EX-1001, [1:29-32]. Indeed, this is how Realtek interprets the claim, as depicted below:



Realtek Infringement Chart (EX-1034.020)

EX-1003, ¶ 257.

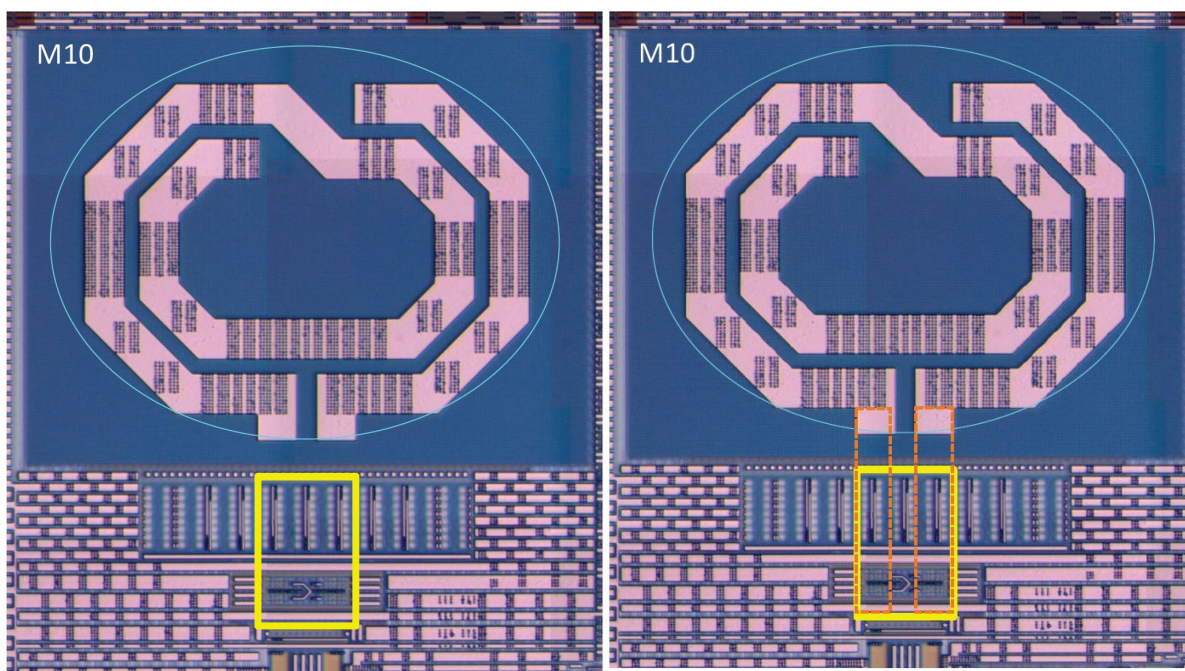
f. Claim 3

Claim 3 depends from claim 2 and specifies that the electronic component is “one of another capacitor component, a transistor component, a diode component, and a resistor component.”

Niknejad discloses this claim. Niknejad’s multi-layer finger capacitor includes an electronic component (*e.g.*, on the second-topmost metal layer), as illustrated in Fig. 3.11 above for claim 2. EX-1007.027. The electronic component on the second-topmost metal layer is at least a capacitor component, since it is part of the multi-layer finger capacitor. EX-1003, ¶¶ 258-259. This is also consistent with how Realtek interprets claim 3. *Id.*; *see* EX-1034.020-.021.

g. Claim 4

Claim 4 depends from claim 1 and requires that the “first region is defined between the two extension-conductor segments.” Realtek interprets this limitation as being the same as the first region in claim 1:



Realtek Infringement Chart, Claims 1 (left) and 4 (right) (EX-1034.013, .022)

Accordingly, Muh/Niknejad discloses claim 4 to the same extent it discloses claim 1. EX-1003, ¶¶ 260-261.

h. Claim 5

Claim 5 depends from claim 4 and requires that the “first region is defined between the two extension-conductor segments and the coil-conductor segment.” Muh/Niknejad discloses this as well. To the extent that the first region is defined “between” the two extension-conductor segments and the coil-conductor segment,

the Muh/Niknejad capacitor, which is or includes a capacitor component, would still be arranged corresponding to the first region, and a plurality of electrode segments in the finger capacitor would still be located below the first region. *See* Sections IX.B.3.v-vi, *ix supra*. EX-1003, ¶¶ 262-263.

i. Claim 9

Independent claim 9 is identical to claim 1 except lacking the limitation “wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.” Therefore, for the reasons provided for claim 1, the Muh/Niknejad combination renders claim 9 obvious. EX-1003, ¶¶ 264-265.

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

Discretionary denial under 35 U.S.C. § 314(a) is not warranted. A final written decision here will issue long before any trial in the N.D. Cal. Case because that case will be stayed while the ITC Investigation proceeds, as mandated by 28 U.S.C. § 1659. Further, the Director has instructed that the Board “will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.” Director Memorandum, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, at 7 (June 21, 2022). There is thus no basis to discretionarily deny institution under § 314(a).

XI. CONCLUSION

Petitioner respectfully requests that the Board institute trial and cancel all challenged claims as obvious.

Date: April 10, 2023

Respectfully submitted,

/s/ Brian E. Ferguson

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that this petition complies with the word-count limitations of 37 C.F.R. § 42.24(a)(1)(i). This petition contains 13,610 words as calculated by the Word Count feature of Microsoft Word, the word processing program used to create it, and an additional 316 words used to annotate figures, totaling 13,926 words.

The undersigned further certifies that this petition complies with the typeface requirements of 37 C.F.R. § 42.6(a)(2)(ii) and typestyle requirements of 37 C.F.R. § 42.6(a)(2)(iii). This petition has been prepared in a proportionally spaced typeface using Microsoft Word in Times New Roman 14-point font.

Dated: April 10, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105 and § 42.6(e), the undersigned certifies that on April 10th, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were sent via International Priority FedEx to:

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