

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES INC.,
Petitioner,

v.

REALTEK SEMICONDUCTOR CORPORATION,
Patent Owner.

CASE: IPR2023-00788
U.S. PATENT NO. 9,590,582

Declaration of Dr. Joshua Phinney (Ex.2003)

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I, Joshua Phinney, declare as follows:

1. I am over eighteen years of age, and I am competent to testify regarding the matters set forth in this declaration if called upon to do so.

2. I have been retained in this matter on behalf of the Patent Owner Realtek Semiconductor Corporation (“Realtek”).

3. I submit this declaration at the request of K&L Gates, counsel for Patent Owner Realtek in this proceeding.

4. I have been asked to provide an opinion in response to Petitioner AMD and its expert Dr. Prucnal’s papers in this proceeding, specification regarding whether the Petition and Dr. Prucnal have establish whether any claim of U.S. Patent No. 9,590,582 (“the ’582 patent”) is unpatentable under the United States Patent and Trademark Office’s *inter partes* review standard of a preponderance of the evidence.

5. In the preparation of this declaration, I have studied the ’582 Patent (Ex.1001), its file history (Ex.1002), the Declaration of Dr. Paul R. Prucnal (Ex.1003), three prior art references Gonzalez (Ex.1005), Muh (Ex.1006), and Niknejad (Ex.1007). I also have considered the other documents or references cited in this declaration.

6. In forming the opinions expressed below, I have considered the documents listed above, the relevant legal standards as provided to me by counsel, and my own knowledge and experience.

7. I expect to continue my review, evaluation, and analysis of the information generated during discovery between the parties. I understand Dr. Prucnal has already provided his opinions in Ex.1003, however if he is permitted to offer additional opinions, I reserve my right to respond to those should I be asked.

I. Qualifications and Background Information

8. A summary of my experience, qualifications, and current employment are included in my CV, which is attached as Appendix A. The following is a brief summary of my relevant qualifications and professional experience.

9. I am a Principal Engineer in the Electrical Engineering and Computer Science practice at Exponent, an engineering and scientific consulting firm headquartered at 149 Commonwealth Drive, Menlo Park, California 94025. I received a Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology (“MIT”) in 2005. I also earned S.M. and B.S. degrees in Electrical Engineering from MIT and the University of Illinois, Chicago (“UIC”), respectively.

10. My master’s thesis at MIT focused on the miniaturization of power converters, by reducing the energy storage and improving the performance of inductors. As part of this work, I designed, tested, and constructed ferrite, iron powder, and air-core inductors, while minimizing magnetic losses. During this time, I invented with my advisor, Dr. David Perreault, an electrical component with a capacitive impedance and an inductance-cancellation feature provided by

magnetically coupled windings. This work was later extended to a second patent, with magnetically coupled windings used to improve EMI filters and common-mode chokes.

11. My doctoral work at MIT centered on miniaturization of power converters and magnetics. As part of my doctoral work, I constructed and modeled planar magnetic systems, including magnetically coupled, printed magnetic coils that were part of LC (inductor-capacitor) resonators. By incorporating such compact LC resonators into power converters, the resulting converter enjoyed multiple benefits, including waveform-shaping and reduction of switch stresses. Through the modeling associated with this dissertation, I become proficient in methods for analyzing the inductances of packages and interconnects, especially planar or filamentous systems of conductors.

12. For my publications related to both my Master's and Ph.D. thesis, I received the William M. Portnoy Prize Paper Award (2003) and the IEEE Power Electronics Society Transactions Prize Paper Award (2004).

13. After earning my Ph.D., I joined Exponent and have led technical investigations to portable electronic devices, microcomputers, as well as industrial and consumer devices with embedded controllers. My job functions include analyzing hardware and software of these devices to understand their modes of

failure, and testifying regarding these devices in legal matters involving patents and trade secrets.

14. As part of my employment at Exponent, I have performed design, design reviews, and failure analysis for wireless charging and communication systems. The focus of this work has been (1) coupling between transmitter and receiver coils from the standpoint of efficiency and magnetic-field exposure to users, in particular for the Power Matters Alliance; (2) coupling of interrogators and transponder coils in printed magnetic cards; and (3) integrated-circuit and coil failures due to wear, dimensional changes, and triboelectric charging. In addition to testifying regarding resonant and inductive wireless-power transfer, I have consulted for industry regarding coil design, RFID and near-field communication (NFC) integrated circuits, modulation methods, and on-metal RFID tags.

15. I have testified regarding the software-defined features, internal circuitry, and physical embodiments of electronic equipment. Regarding electronics, I have testified regarding power electronics in communication systems, wind turbines, grid-scale photovoltaic plants, and consumer electronics. In addition, I have testified regarding control and compensation in industrial controllers, voltage regulators, and switched-mode power converters. My experience with wireless RF circuitry includes failure analysis of amplifiers, power supplies, matching networks, and multiplexers in satellites, semiconductor processing equipment, and medical

devices. In addition, I have performed board- and die-scale root-cause failure analysis for low-power mobile designs centered around SoCs (system-on-a-chip) and PMICs (power-management integrated circuits).

16. Regarding the mechanical elements of electronic equipment, I have testified regarding buttons and touch interfaces, connectors, linear and rotary actuators, position-measuring devices, and the design and construction of modular housings for computerized equipment and peripherals. In particular, I have testified regarding detachable components as they are constructed in relation to the housing and underlying electronic assemblies, including printed circuit boards, flex printed circuits, and other connector assemblies within the housing of electronic equipment.

17. In addition to the forgoing, I perform electromagnetic assessment of utility and communication infrastructure. These issues include permitting, interference, and environmental impact of radar, AC and HVDC transmission lines, substations, photovoltaic installations, generators, broadcast antennas, and electrified mass transit systems.

18. I am being compensated for my work associated with this case at a rate of \$725 per hour plus reimbursement of reasonable expenses. My compensation is not contingent on my opinions or the outcome of the case, and I have no other interest in this case or the parties thereto.

II. Legal Standards

19. Although I am not a lawyer, I have been advised on the relevant legal principles by Realtek's counsel and have used them as a basis for my opinions. These are consistent with my understanding of the legal principles based on my prior experience with patent litigation matters.

20. I have also been informed and understand that terms in the patent claims must be read as they would have been understood by a "person of ordinary skill in the art" ("POSITA") at the time of the claimed invention.

21. I understand that at POSITA is a person to which the claimed subject matter pertains with the capability of understanding the scientific and engineering principles applicable to the pertinent art. I understand that the following factors may be considered in determining the level of ordinary skill: the type of problems encountered in the art; prior art solutions to those problems; the speed with which innovations are made; the sophistication of the technology; and the educational level of active workers in the field. I also understand that not every factor may be present and that one or more factors may predominate.

22. I understand that the claims within a patent set forth what the inventors have presented as their inventions. I understand that claims can be independent or in dependent form, meaning that they depend from the identified independent claims and add requirements to those claims.

23. I understand that there are other parts of a patent, including the abstract, the figures of a patent, the background of the invention, the summary of the invention, and the detailed description of the invention. I understand that these portions often are collectively referred to as the “specification” of a patent. I understand that technically, the claims are part of the specification, but that referring to the “specification” typically means referring to the written description of the inventions rather than the claims. I understand that the specification informs the understanding of the claims by, for example, describing the claimed invention and providing preferred examples of the claimed invention.

24. I have also been informed and understand that terms of a claim should be understood in the context of the claim as a whole. I also understand that the specification of the patent is relevant to the meaning of a claim term. I further understand that the claims must be read in light of the specification.

25. I understand that the correspondence back and forth between the representative of the applicant, and the U.S. Patent and Trademark Office, leading up to the issuance of a patent is called the “file history” or “prosecution history.” It has been explained to me that, in the process of obtaining a claim of a patent, the inventors and the examiner may make statements explaining their understanding of the scope of their claimed invention. It has also been explained to me that for a statement by the inventors to narrow the scope of a claimed invention, the statement

must clearly and unambiguously limit the scope of an invention. I understand this is called “prosecution disclaimer” or “prosecution disavowal.”

26. I understand that the claim language, specification, and file history are referred to as “intrinsic evidence” or “the intrinsic record.”

27. I understand that, unlike at the district court, patents subject to *inter partes* review, such as this proceeding, are not presumed to be valid, such that a lower burden of proof is used to judge the patentability of challenged claims. Unlike the district court’s “clear and convincing” burden, here a “preponderance of the evidence” burden exists.

28. I understand that a patent claim is invalid as “anticipated” by a single “prior art” reference if the reference discloses every single element of the claim with sufficient precision and detail to establish that the subject matter of the claim existed in the prior art. In particular, I understand that it is not sufficient to establish that all of the elements are collectively disclosed within the four corners of a particular document. Instead, the operative question is whether a person of ordinary skill would have understood the elements as being arranged as in the claim itself. I also understand that a prior art reference cannot “anticipate” a patent claim unless that reference enables one of ordinary skill in the art to make and use what is disclosed without undue experimentation. Thus, if the reference does not enable one of

ordinary skill to make or use each and every claim limitation, then the claim cannot be “anticipated” by the reference.¹

29. I understand that a prior art reference can disclose a given claim element actually or inherently.

30. In the case of actual disclosure, I understand that a person of ordinary skill would need to have understood that the disclosure corresponds to the claim element in question. I also understand that such disclosure may be implicit rather than explicit. For example, prior art need not use the same words as the claimed invention. However, I understand that ambiguous references do not anticipate.

31. In the case of alleged “inherent” anticipation, I understand that the claim element in question must necessarily be present when practicing the described technology even though the prior art reference itself contains no express description of the element in question. In particular, I understand that “possibilities or probabilities” are not sufficient to establish inherency. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, the

¹ I understand that Petitioner and Dr. Prucnal are not advancing any anticipation-based theories of unpatentability.

essence of inherency is that one of ordinary skill in the art would recognize that a reference unavoidably teaches the property in question.

32. I understand that a patent claim may describe an invention that was new (i.e., not anticipated by any prior art reference), but nevertheless be invalid for “obviousness” if the differences between the patented subject matter and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention was made.²

33. I understand that an invention is not rendered obvious simply on the basis of two or more different disclosures that collectively disclose all of the claimed elements. In other words, an invention is not obvious just because all of the elements that comprise the invention may have been known in the prior art. Instead, a person of ordinary skill in the art must have had a reasonable expectation of success in pursuing the possibility that turns out to succeed and is claimed. In particular, I understand that knowledge of a goal does not itself render achievement of that goal obvious.

² I understand that the Petition and Dr. Prucnal are advancing two “obviousness” theories.

34. I also understand that determining whether or not a claimed invention would have been obvious requires assessing facts related to (1) the scope and content of the prior art, (2) the differences between the prior art and the claimed invention, (3) the level of ordinary skill in the art, and (4) any objective evidence (“secondary considerations”) of non-obviousness. I understand that this is known as consideration of the “Graham Factors.”

35. I further understand that an invention is not obvious just by demonstrating that each of its elements was, independently, known in the prior art. To prove that an invention is obvious, I understand that it can be important to point to a reason or reasons, such as a teaching, suggestion, or motivation, that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed invention does. I understand that this is because inventions in most (if not all) instances rely upon building blocks already known, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known, therefore it can be important to point to such a reason or reasons. I understand that in identifying such a reason, the analysis need not require precise teachings in the prior art directed to the specific subject matter of the challenged claim.

36. I understand that it will often be necessary for a court to look to interrelated teachings of multiple patents and the background knowledge possessed

by a person having ordinary skill in the art in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. I understand that the combination of familiar elements according to known methods may be obvious when it does no more than yield predictable results.

37. I also understand that a claim is not invalid as obvious if it is more than the predictable use of prior art elements according to their established functions.

38. Further, I understand that while predictability is a touchstone of obviousness, the concept of a “predictable result” under the law refers not only to the expectation that prior art elements are capable of being physically combined, but also that the combination would have worked for its intended purpose.

39. I also understand that if the prior art teaches away from combining known elements in the manner claimed by the invention at issue, discovering a successful way to combine them is less likely to be obvious. In particular, I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set

out in the reference, or would be led in a direction divergent from the path that was taken by the applicant, or would understand based on the reference that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. Likewise, I understand that similar subject matter may not be sufficient motivation for a person of skill in the art to combine references if the references have conflicting elements.

40. Further, I understand that even if a reference does not necessarily “teach away,” its statements regarding preferences are relevant to a finding regarding whether a person of ordinary skill would have had reason to combine that reference with another reference

41. I also understand that one must be cautious and resist the temptation to rely on hindsight reasoning when attempting to combine references to suggest that a claim may be obvious. It is important to analyze validity based on the perspective of one at the time of the invention, which I understand is at least as early as the effective filing date. I understand that objective indicia (or “secondary considerations”) of non-obviousness or obviousness may be particularly probative and helpful in avoiding hindsight.

42. I also understand that the burden of persuasion concerning unpatentability (in other words, the ultimate burden to prove the relevant facts to the specified degree of certainty—here, preponderance of the evidence) remains at all

times on the party challenging patentability—here, the Petitioner, AMD. If the fact trier of the issue is left uncertain as to validity issues, Petitioner has thus failed to meet its burden.

III. Level of Ordinary Skill in the Art

43. In my opinion, a person of ordinary skill in the art (“POSITA”) with respect to the ’582 Patent would have had at least a bachelor’s degree in electrical engineering or an equivalent field. My analysis and opinions below are given from the perspective of a POSITA in this technological field in the relevant time frame, unless stated otherwise.

44. I satisfied the definition of a POSITA long before the filing date of the application leading to the ’582 Patent. I now consider myself an expert in the relevant field of technology for the ’582 Patent.

45. In forming my opinions for this declaration, I have used the perspective of one of ordinary skill in the art as defined above. My opinions, however, would not be affected if a POSITA is defined as someone who has slightly more or slightly less experience than described above.

46. For example, I understand that Dr. Prucnal opines that a POSITA would be an individual with at least bachelor’s degree in electrical engineering or an equivalent field, and at least 3-4 years of professional experience in the field of integrated circuit design. I understand that Dr. Prucnal has further opined that a

person with additional education but less professional experience, and vice versa, may qualify as a POSITA. For instance, he believes a POSITA would also include someone with a master's degree in electrical engineering and 1-2 years of professional experience in the field of integrated circuit design or someone with a Ph.D. in electrical engineering.

47. I disagree that 3-4 years of professional experience in the field of integrated circuit design or additional education but less professional experience is necessary for a POSITA with respect to the '582 Patent. However, my opinions would not be affected if a POSITA is defined as someone who also has some basic, professional experience working with LC circuits. Further, I was a POSITA under Dr. Prucnal's definition at least as early as 2002, when I had attained a B.S. and S.M. in Electrical Engineering and was one year into my Ph.D. program at MIT.

IV. 582 Patent

48. I have reviewed the specification and prosecution of the '582 Patent. The '582 Patent describes and claims an improved design for an LC circuit, with a specific orientation of the capacitor of the LC circuit in relation to the inductor.

49. Dr. Prucnal's opinions focus primarily on Claim 1 of the '582 Patent, although he also addresses dependent Claims 2-5 and independent Claim 9. Independent Claim 9 is substantially the same as independent Claim 1. Ex.1001, Cl. 9.

50. Independent claim 1 (which the Petition treats as essentially identical as independent claim 9) recites:

A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

- a first insulation layer;

- an inductor component, comprising:

 - a coil-conductor segment, located on a surface of the first insulation layer; and

 - two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

- a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment, wherein the capacitor component comprises:

 - a plurality of connecting segments, extending corresponding to the two

extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments. Ex.1001, Claim 1.

Additional claims are also at issue, including claims 2-4, the text of which can be found in Exhibit 1001. I am not offering an opinion on claim 5 of the '582 Patent.

A. Patent Overview

51. The specification of the '582 Patent describes a configuration for circuitry components that comprise an inductor-capacitor (LC) resonant circuit. Ex.1001, 1:16-18. Independent claim 1 similarly claims a specific arrangement of these components, including a specific location and orientation of the capacitor component relative to the inductor component. Ex.1001, claim 1.

52. As part of its specification, the '582 Patent outlines certain prior art circuits where “a signal may pass through the insulation layer and leak to the silicon substrate, resulting in transmission loss.” Ex.1001, 1:33-39. It goes on to explain a solution to this problem, noting that its claimed configuration is able to “reduce[]

generation of phase noise, arrangement of interconnecting wires, and an overall size.” Ex.1001, 1:47-2:3. This configuration also reduces “parasitic RLC (Resistance-Inductance-Capacitance).” Ex.1001, 12:47-54. These prior art configurations often utilized “surface-mount” components that increased the size and volume of a given LC circuit implementation. Ex.1001, 1:29-32. Surface-mount components are utilized mainly for implementations of circuits on printed circuit boards, and these implementations are almost always significantly larger than an on-chip implementation of similar functionality.

53. Instead of using surface-mount components, the ’582 Patent describes the use of various metal fabrication techniques, such as layer-by-layer lithography processes, to create an LC circuit. Ex.1001, 3:48-55. In doing so, a first metal layer would be deposited, certain portions etched away, insulative material applied, certain portions etched away, and a second metal layer deposited. This process would be repeated according to a recipe of fabrication steps until the desired chip, as specified by a GDS or OASIS file compliant with certain “Design Rules,” was complete.

54. The ’582 Patent claims an orientation of a capacitor component so that it is located below, and has connecting segments overlapped by, the extension-conductor segments in a vertical direction. By setting up such a configuration, the capacitor component is therefore “arranged corresponding to the first region in an

embedded manner.” Ex.1001, cls. 1, 9. This takes advantage of “prime real estate” of the LC circuit.

55. The '582 Patent has important benefits that arise out of the design described and claimed by the patent. It explains, “[a]t a high frequency, a signal may pass through the insulation layer and leak to the silicon substrate, resulting in transmission loss.” Ex.1001, 1:36-39. This transmission loss can have negative impacts on inductor quality factor (Q) and self-resonance frequency.

56. The '582 patent claims a design where extension conductor segments overlap connecting segments (Ex.1001, Cl. 1) and require a specific location of the capacitor in relation to the inductor coil that moves the capacitor out from under the coil-conductor segment. As a result of these requirements, the design achieves the aims of “reduc[ing] generation of phase noise,” facilitating “arrangement of interconnecting wires,” reducing “overall size,” and limiting parasitic RLC. Ex.1001, 1:63-2:3, 12:51-54.

57. The '582 Patent claims priority to a Taiwanese application filed on April 16, 2014, and was filed in the United States as Application No. 14/338,904 on July 23, 2014. The '582 Patent issued on March 7, 2017 and contains two independent claims.

B. Prosecution History Overview

58. The Application received its first rejection in view of U.S. Patent Publication No. 2009/0322447 to Daley et al. (“Daley”). Ex.1002, 342. In the rejection, the examiner noted that while the independent claim was rejected, “Claim 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.” Ex.1002, 345. That claim, then-pending Claim 5, included limitations directed towards the relative location of the connecting segments of the capacitor component to the extension conductor segments of the inductor component. Ex.1002, 327. The applicant elected to argue patentability without any amendment. See Ex.1002, 330-331.

59. The claims were again rejected over Daley. Ex.1002, 319. The examiner again stated that “Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.” Ex.1002, 319. The applicant again argued that the specific orientation of the capacitor and inductor on respective sides of the insulation layer distinguished the then-amended claims from the cited prior art. See Ex.1002, 73-74.

60. The then-pending claims were rejected a third time over Daley. Ex.1002, 58-62. The examiner again indicated that then-pending Claim 5 would be allowable if rewritten in independent form. Ex.1002, 61. The applicant incorporated the subject matter suggested by the examiner into the independent claims. Ex.1002, 27.

61. The Examiner identified U.S. Patent No. 9,270,247 to Jing (“Jing”) during an interview and substantively discussed Jing, for the first time, in the “Examiner’s Statement of Reasons for Allowance.” Ex.1002, 12. Notably, Jing was not ever used in a rejection and the examiner incorrectly characterized Jing’s disclosure. Ex.1002, 12.

62. Contrary to the Examiner’s statements, Jing’s “connecting segments” do not “extend[] corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction” and the examiner improperly alleged that “elements 725 and 730 together cannot be interpreted as ‘a capacitor component.’” Ex. 1002, 12-13.

63. The applicant did not respond to these inaccurate statements.

64. I have also reviewed the ITC’s order regarding Jing, where the ALJ concluded that the examiner’s analysis of Jing and understanding of the claims in relation to Jing was incorrect. Ex.2001, 32-36.

V. Claim Construction

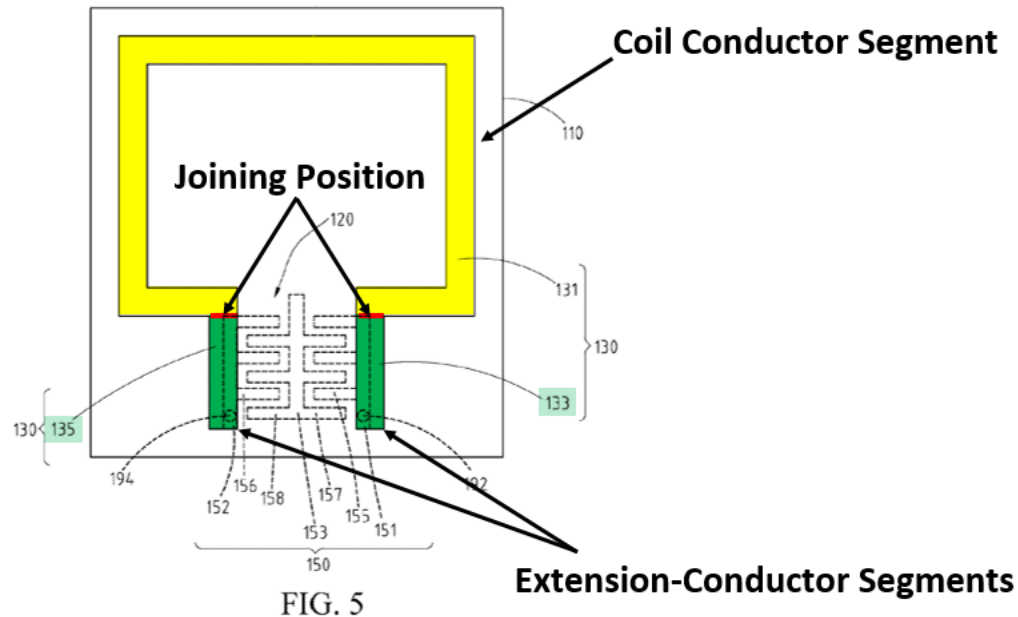
65. I have been asked to analyze two terms: “two extension-conductor segments” and “coil conductor segment.” I have done so below and offer the following opinions of how a POSITA would understand these terms in view of the intrinsic record.

66. I note that Dr. Prucnal has not offered any opinions about the “plain and ordinary” or “ordinary and customary” meaning of any claim elements and has further not identified any specific constructions that should be adopted for any terms. To the extent he is permitted to supplement his opinions, I reserve my right to respond to any new opinions he may offer.

C. Extension Conductor Segment

67. It is my opinion that a POSITA would understand the term “extension conductor segments” to be “the two portions of the inductor that extend approximately perpendicular from where each joins the coil conductor segment.” Beginning with the claim language itself, Claim 1 requires that the extension-conductor segments “extend[] outwards relative to the coil-conductor segment.” The division point between the coil-conductor segment and the extension-conductor segments is set forth in greater detail in the specification, which describes a joining position that exists between the extension-conductor segment 133 and the coil-conductor segment 131. Ex.1001, 4:1-5.

68. I have prepared an annotated version of Figure 5 below that shows how the extension conductor segments (green) extend approximately perpendicularly away from the joining position (red) that forms the border with the coil-conductor segment (yellow).



69. The above annotated figure shows how the “extension-conductor segment 133 is joined to a first end of the coil-conductor segment 131 and is approximately perpendicular to a joining position between the extension-conductor segment 133 and the coil-conductor segment 131.” Ex.1001, 4:1-5. This perpendicular relationship is essential to understanding where the coil portion of the inductor begins and ends in relation to the extension-conductor segments.

70. I depict this joining portion as a red line that has some width, however in reality this red line is used for illustrative purposes only. The joining portion is

simply where the two segments of the inductor component meet and is not a separate segment.

71. While Dr. Prucnal only mentions this joining position in passing (*see* Ex.1003, ¶230), he appears to disregard this **perpendicular** disclosure in favor of a focus on Figure 8. Ex.1003, ¶¶230-232. I address this in greater detail later in my declaration, however in my opinion that Figure 8 is an unclaimed embodiment because it depicts a capacitor that is substantially overlapped by the coil conductor segment.

72. In the ITC, Dr. Prucnal argued that both the above understanding, as well as that reflected in the annotated version of Figure 5 below are correct. However, this cannot be so as the understanding reflected below is inconsistent with the embodiments that are claimed in the '582 Patent. This type of joining position has two primary problems.

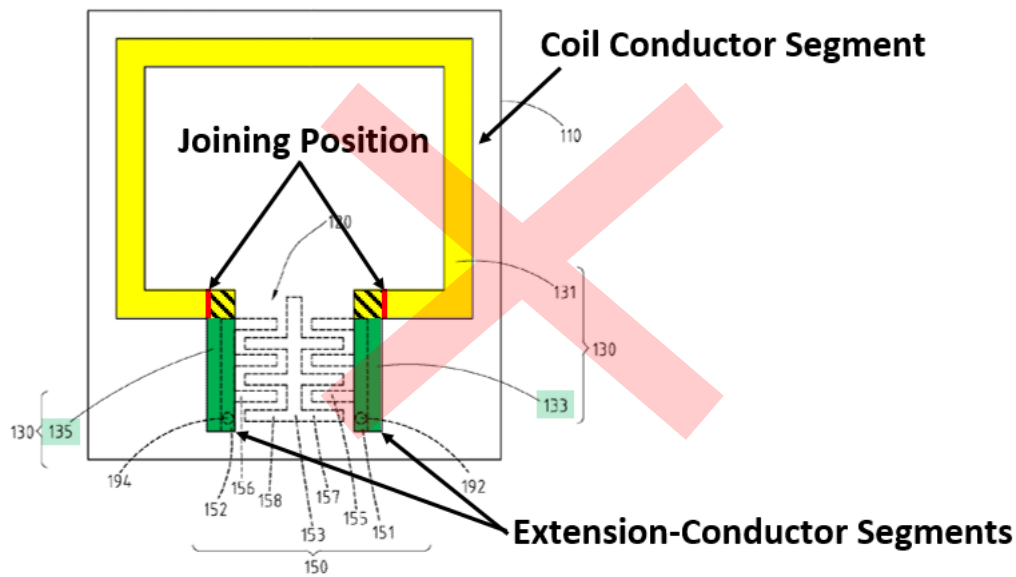
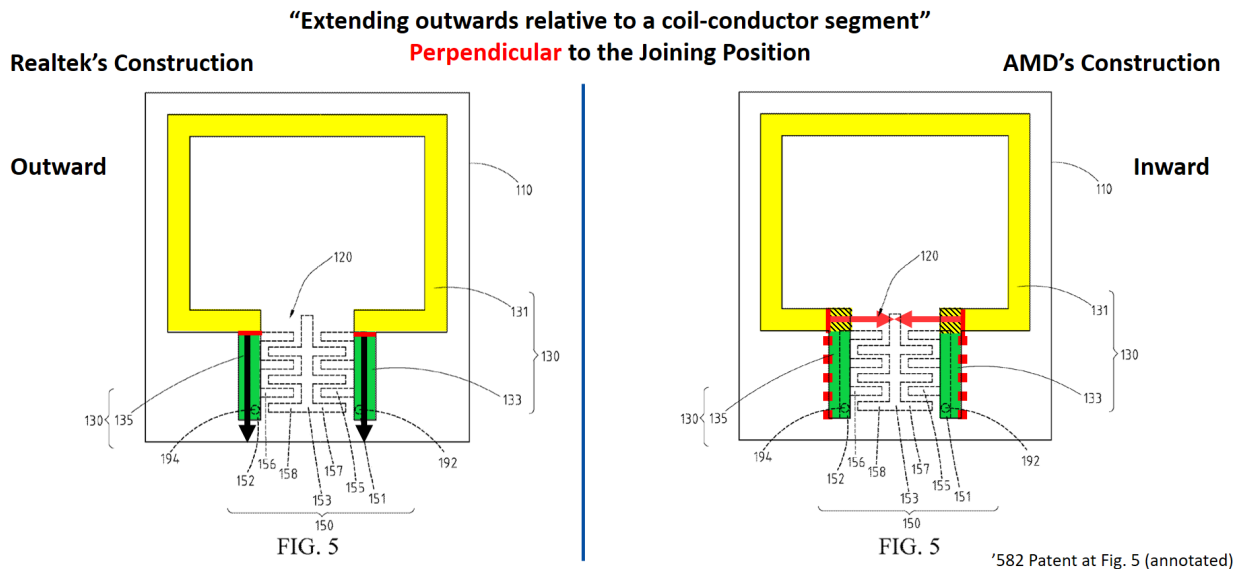


FIG. 5

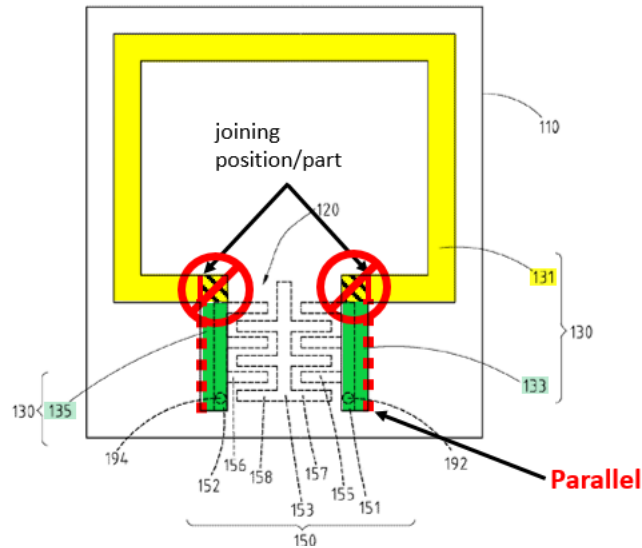
73. First, the specification is clear that the extension-conductor segments are “perpendicular to a joining position between the extension-conductor segment 133 and the coil-conductor segment 131.” Ex.1001, 4:1-13. The above theory does not show such a perpendicular relationship between the joining position and the extension conductor segment, and therefore runs afoul of the requirement that the claimed extension conductor segments “extend[] outward relative the coil-conductor segments.”

74. Second, the above theory improperly identifies a portion of the coil-conductor segment as being part of the extension conductor segment, and as a result, under this formulation, the extension-conductor segments do not “extend outward relative to the coil-conductor segment.” Ex.1001, 3:36-42.

75. I've further created an annotated figure that shows how my proposed construction (Left) ensures the extension conductor segment extends outward, and how AMD's proposal (Right) does not. The right side, by improperly including the edge or corner of the coil-conductor segment in the extension-conductor segment, has the extension-conductor segments parallel to the joining portion:



76. I've further created an annotated image that shows how the "square" corner cannot be part of the extension conductor segment, akin to the right side of the above image:



77. My proposed understanding also ensures that the claimed first region is “defined by the two extension-conductor segments and the coil-conductor segment.” Ex.1001, cl. 1. In the below annotated figure, the entire first region (shaded in red) is located *outside* the coil such that there is no portion of the capacitor component overlapped by the coil conductor segments.

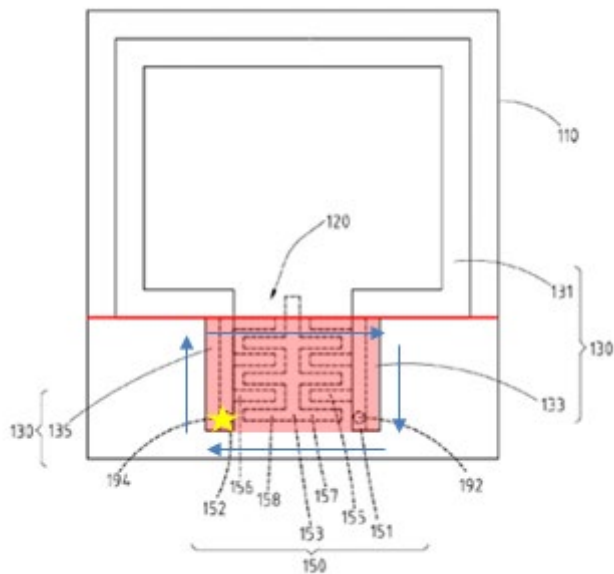


FIG. 5

78. In the above annotated figure, I've shaded the first region in red. This first region is "defined by" the two extension conductor segments (up to the joining positions, at the red line). To outline this first region, I first began at the star, an arbitrary point on one of the extension conductor segments, since the first region is defined *by* the left extension conductor segment, the first region is outlined in a vertical direction, until reaching the coil conductor segment (at the red horizontal line) and the joining portion. Then, turning right, across the space between the two extension conductor segments, the first region outline continues until reaching the other extension conductor segment, and the first region extends downward again.

79. I have further identified what the first region would look like in the event the joining positions were described differently, as it just so happens "defined by the coil conductor segment" and the location of the joining positions above lead to the same first region.

80. Below, I have outlined how the first region looks if the joining positions were described in the specification to be diagonal (instead of perpendicular to the extension conductor segment, as is the case in the '582 Patent). Specifically, the same first region (shaded in red) would exist, because the first right-hand turn would still occur at the same location because tracing along the outer edge of the extension conductor segment, one arrives the coil conductor segment at the same location.

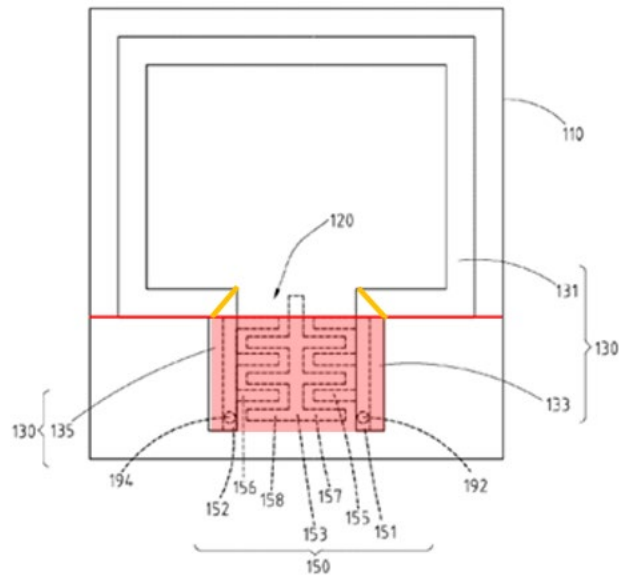


FIG. 5

81. Petitioner's prior construction however, has the first region defined only by the extension-conductor segments, and fails to indicate how a larger first region would be defined by the extension conductor segments *and* the coil conductor segment:

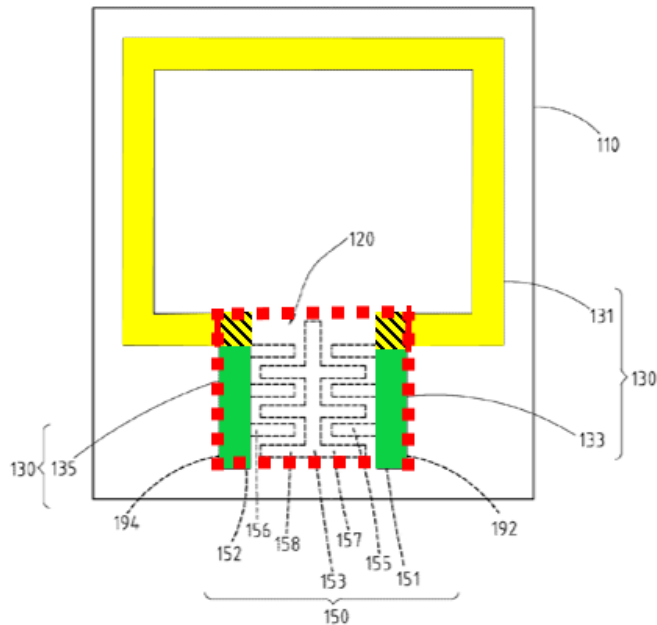


FIG. 5

82. I have also provided an annotated version of Figure 5 to depict the claimed first region in dependent claim 4, where instead of defined *by* the extension conductor segments and *by* the coil conductor segment, the first region is more narrowly defined *between* the extension conductor segments and *by* the coil conductor segment.

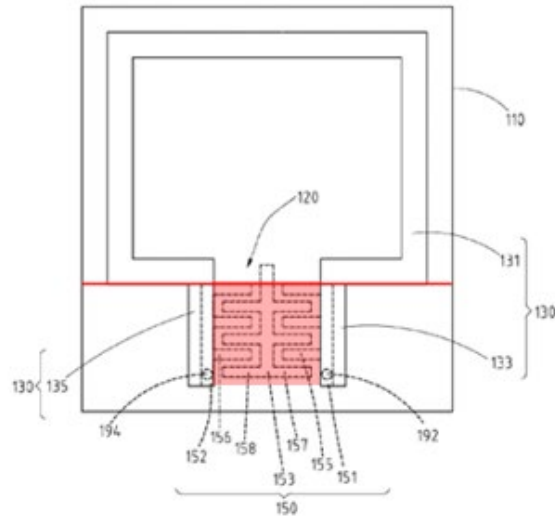


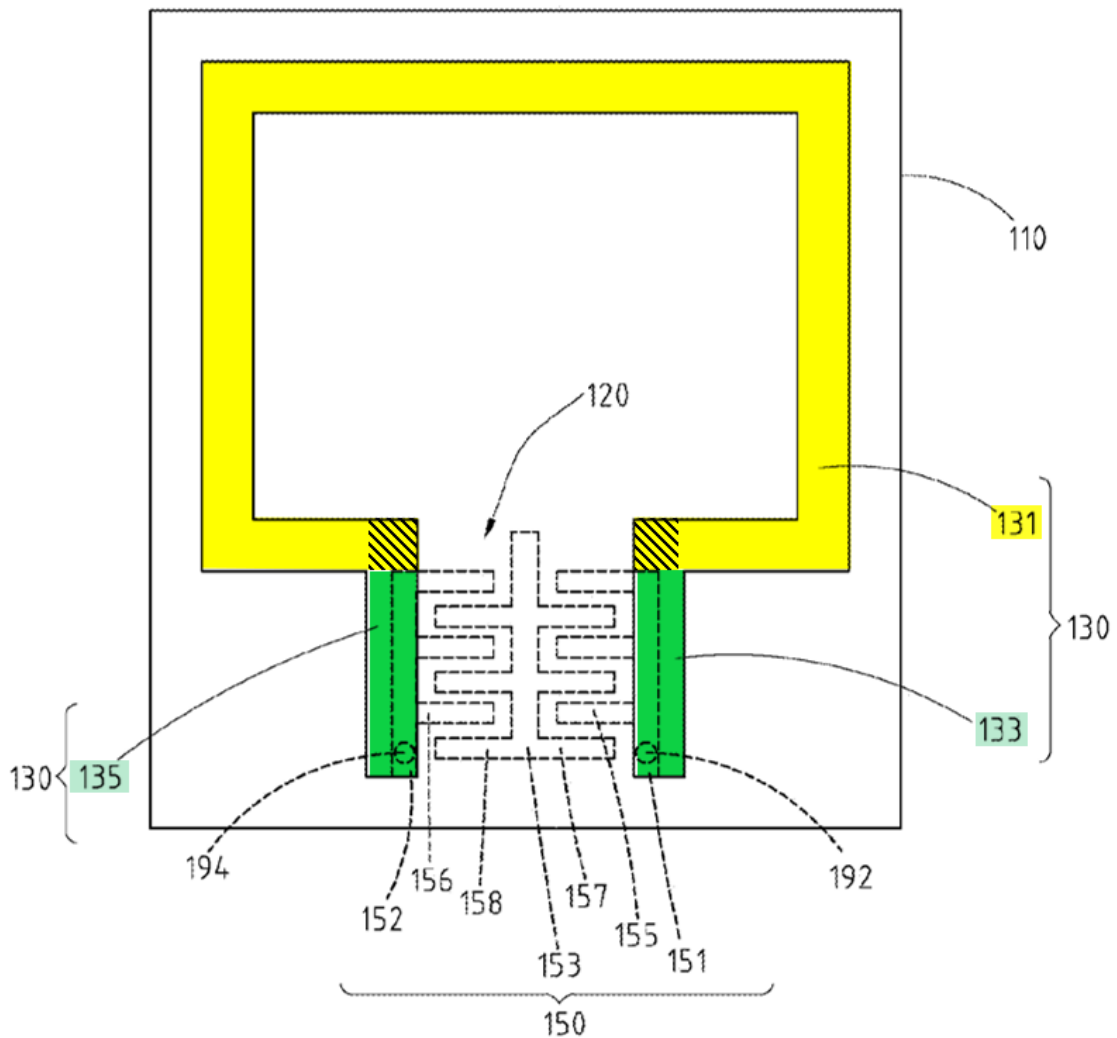
FIG. 5

83. Based on the intrinsic record, it is my opinion that a POSITA would understand the claimed “extension conductor segments” to be “the two portions of the inductor that extend approximately perpendicular from where each joins the coil conductor segment.”

D. Coil Conductor Segment

84. The '582 Patent is clear that the extension-conductor segments extend *away* from coil-conductor segments approximately perpendicularly. Ex.1001, 4:1-5, 3:66-4:1, 3:22-27, claim 1. This necessitates an understanding of where one begins and one ends.

85. A POSITA would understand that the inductor coil includes the edges of the inductor coil, which are in cross-hatch in the image below, and which are separated from the extension-conductor segments at the joining position/part:



Ex.1001, Fig. 5.

86. These portions of Figure 5 in cross-hatch above cannot be part of the extension conductor segments, as set forth above.

87. The constructions of these two terms go hand-in-hand and in view of the arguments and construction I explained above, the “coil-conductor segment” would be understood to be “inductor coil.”

VI. Prior Art

88. I have reviewed the prior art Dr. Prucnal relies upon for his two grounds of unpatentability, Gonzalez, Muh, and Niknejad. Notably, none of these three references shows a capacitor in the claimed orientation relative to the inductor. I provide more technical details regarding these references as I discuss them in my opinions below, but provide brief bibliographical overviews here.

A. Gonzalez

89. Gonzalez is a research paper that analyzes certain microwave theories and techniques. Ex.1005. Gonzalez does not contain any circuit designs beyond a schematic and limited perspective views of a 3D model. Ex.1005, Figs. 2, 8. Gonzalez's paper describes different aspects of an LC circuit, but never describes how the various aspects would fit together. Moreover, Gonzalez makes clear that the wires that AMD identifies as capacitors are deliberately designed to minimize capacitance and therefore cannot serve as the electrode segments of the claimed capacitor component.

B. Muh

90. Muh, a facially undated thesis (Ex.1006, 1), is purportedly obtainable from the University of California library system. Ex.1006, 1. The thesis is primarily directed towards a push-push VCO, and Dr. Prucnal's opinions are almost exclusively based on the image of Figure B-3. Ex.1006, 56-58. Figure B-3 depicts a HFSS (high-frequency three-dimensional field solver) model of an LC circuit but

also fails to provide detail regarding the format, shape, or orientation of the capacitor.

C. Niknejad

91. The final prior art reference, Niknejad, is a textbook comprising almost 300 pages. Ex.1007, 12. Like with Muh, the Petition relies on only a small subset of the pages of Niknejad: 26-28. Niknejad fails to provide any detail as to how its disclosed finger capacitor would be actually designed, positioned, or shaped and, more importantly, teaches that a POSITA would be motivated to orient a finger capacitor in an LC circuit contrary to the claims of the '582 Patent.

VII. Ground 1

92. Dr. Prucnal and I appear to agree that none of the references he relies on, by themselves, disclose the LC circuit as claimed. Where we disagree is whether a POSITA would interpret Gonzalez in a manner that teaches the claimed configuration and, as I describe in more detail below, his opinions are inconsistent with the actual disclosure of Gonzalez.

93. As an initial matter, Gonzalez is an academic article, not a PCB schematic or detailed layout diagram. As such, it lacks the detail that is found in the '582 Patent's claims and does not describe how the VCO of Gonzalez would be oriented. In fact, Gonzalez confirms that it was focusing on using "PCells" for its research. Ex.1005, 5. The name 'PCell' means 'Parametrized Cell' and is a standard

data structure in computer-aided chip design. (Ex.2007)³ A PCell is capable of generating a circuit component, such as a capacitor or inductor, based on parameters entered by the designer. For instance, if designing a capacitor via a PCell, a designer could enter the amount of capacitance desired, as well as the desired width of the capacitor, and the PCell will automatically generate a layout for a capacitor having the desired parameters. However, a PCell does not normally account for the specific orientation of different components, such that a PCell for a vertically oriented inductor will normally be identical to a PCell for a horizontally oriented inductor. This greatly saves designer time.

94. Ultimately, for its research purposes a “middle ground” inductor PCell was selected because the author deemed it “as a good tradeoff between” having too low of a Q factor (albeit opening the door to a wider selection of varactors that would be available) and having too few varactor options (limited to varactors with largest capacitance ranges) but the highest Q factor. Ex.1005, 5. In this selected PCell, the inductor of the LC tank includes “two upper copper metal layers, plus [an] aluminum metallization layer.” These layers are visible in the top image of Figure 8. Ex.1005, Fig. 8.

³ Cadence PCell Designer Datasheet

95. Gonzalez describes two types of varactors (i.e., voltage controlled or voltage tunable capacitors): 1) fine tuning varactors and 2) binary switched varactors. Ex.1005, 5. But, Gonzalez explains that these “are made from the same structure,” such that they are effectively the same for the purposes of their structure. Ex.1005, 5. These varactors “are implemented using a thick gate-oxide available in the process that provides a capacitance ratio” of approximately 3 “for voltages between 0 and 1.8V.” Ex.1005, 6. This capacitance ratio means that the largest capacitance realizable via one of these varactors is approximately three times larger than the smallest realizable capacitance.

96. Gonzalez explains these varactors are made “with N+poly/Nwell varactors” where the “N+poly gates are each connected to one of the two differential terminals (Out+ and Out-)” of the circuit and are “placed in the same Nwell that is biased using a common voltage (V_c).” Ex.1005, 6.

97. While these varactors provide a designed capacitance and are certainly considered a capacitor, they are not the capacitor component that is described and claimed in the '582 Patent. Gonzalez explains that its varactor structure ensures that the differential current path length (the length that current must travel from each differential terminal (Out+ and Out-)) is minimized. Ex.1005, 6. As part of Gonzalez’s efforts to minimize the Out+ and Out- current lengths, it notes that when greater capacitive values are needed, an array of these varactors, with a waffle

structure, is used (as shown in Gonzalez Fig. 5). Ex.1005, 6. When this waffle structure of additional varactors is utilized, Gonzalez depicts additional “wires” in place to ensure the voltage of the two differential terminals (Out+ and Out-) is provided to the various places the appropriate voltage is needed (as shown in, for example, figures 2 and 8) while maintaining the minimized differential current path. Ex.1005, Figs. 2, 8.

98. Dr. Prucnal identifies only these varactors as the claimed capacitor component; he identifies no other capacitor component. These varactors do indeed provide the capacitance of the LC circuit described in Gonzalez. However, the varactors themselves have no electrode segments. Instead, the capacitance of these varactors comes from electric fields created substantially vertically between transistor gates and the doped substrate beneath, not from electric fields extending laterally between interdigitated metals.

99. Dr. Prucnal and I both agree that the varactors of Gonzalez are not finger capacitors and lack any connecting segment or electrode segments as are required by the claims. His reliance on them further shows how his opinions are not rooted in the actual disclosure of Gonzalez. Instead, a POSITA would understand that the “wires” that Dr. Prucnal alleges are “electrode segments” are simply wires that perform Gonzalez’s stated goal of minimizing the differential current path length. Moreover, because Gonzalez seeks to maintain fine control over the

capacitance of the LC circuit, there is, by intentional design of their layout, minimal capacitance between these wires.

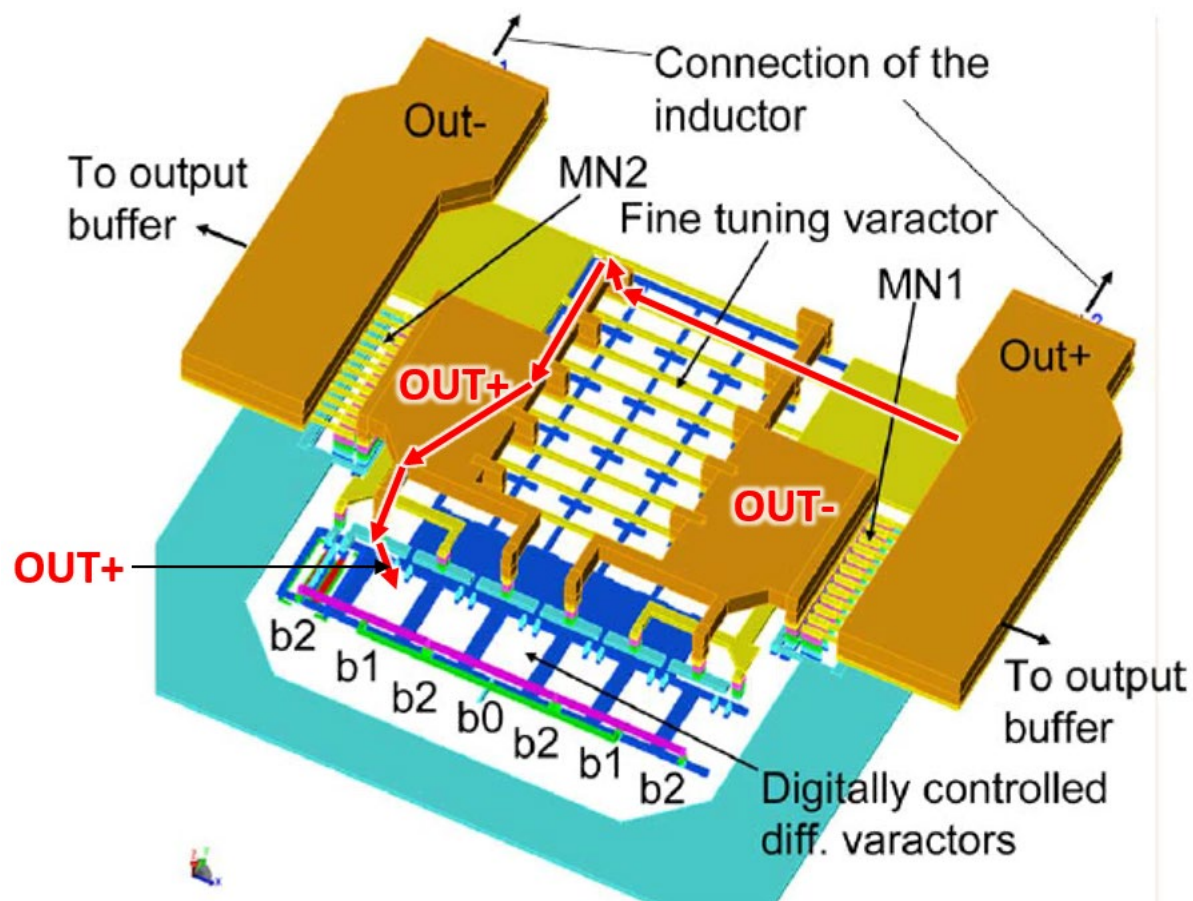
A. Gonzalez does not disclose an “electrode segment”

100. Dr. Prucnal alleges that the yellow wires of Figure 8 are the electrode segments of Claim 1. However, these are plainly wires that exist simply to convey a voltage and current from one portion of the circuit to another.

101. The '582 Patent explains what it's “electrode segments” are: “The electrode segments 155 and 156 serve as electrode plates of the capacitor, capacitive induction is generated between the electrode segments.” Ex.1001, 4:41-43. While Dr. Prucnal and I agree that there is capacitance between any two electrically conductive materials (including my fingertips), that does not mean that any two pieces of conductive material are electrode plates or electrode segments. Ex.1005, Ex.2005, 40:23-44:18. The claimed electrode segments are not merely wires or metallic components that incidentally have a capacitance. Instead, a POSITA would understand that the claimed electrode segments are specifically the electrode plates of the claimed capacitor of the claimed LC circuit, the component that provides the capacitance for the LC circuit.

102. Dr. Prucnal cannot identify any instance of these electrode segments in the varactors of Gonzalez, as they do not exist. Instead, he relies on the yellow wires of Figure 8. A POSITA would not understand these yellow wires of Gonzalez to be

a capacitor (or part of a capacitor). They are not electrodes and do not provide any designed capacitance, such that they cannot be the claimed electrode segments. Ex.1005, Fig. 8. In fact, they are specifically designed as a sparse, comb structure in order to introduce as little differential capacitance as possible, since such static capacitance would decrease tuning range and maximum frequency of the VCO. These yellow wires are not part of any varactor or capacitor component. They simply carry charge from, for example, the Out+ terminal to the digitally controlled varactors:



103. Dr. Prucnal also fails to address the fact that the yellow wires are located many layers above any actual varactor. When counting the number of metal layers between the yellow wires and the silicon-based varactors, one counts at least five metal layers:

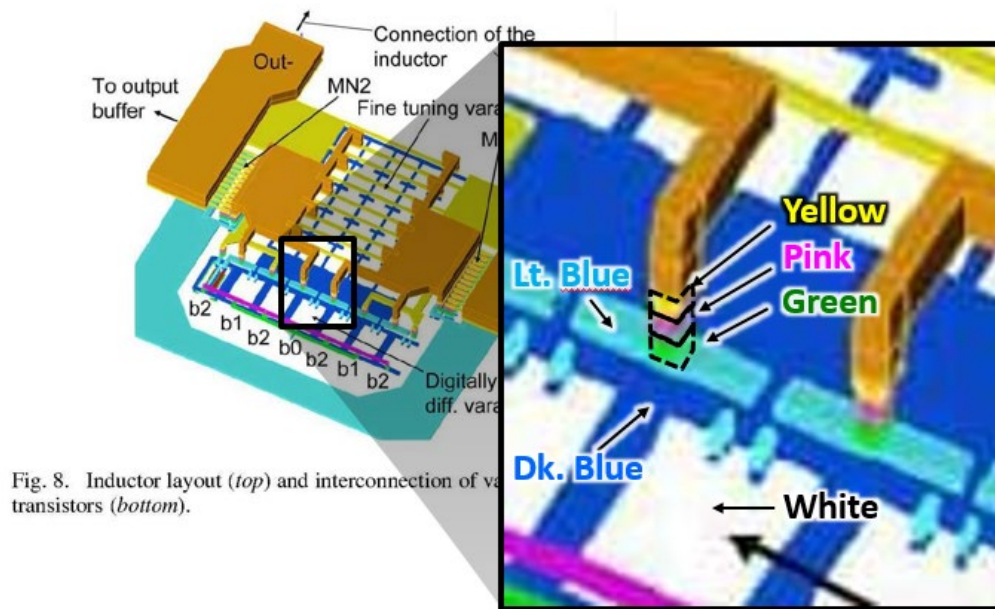


Fig. 8. Inductor layout (top) and interconnection of varactors (bottom).

104. The yellow wires simply carry the respective electrical charge from one alleged extension-conductor segment to the other side, to provide the varactors (which are located outside of any first region), with both charges necessary to operate the varactor. *Id.* For example, looking at Figure 8, varactor b2 needs to have one lead having an Out+ voltage and one lead having an Out- voltage, and that is accomplished through these yellow wires. *Id.*

105. Having reviewed Gonzalez and Dr. Prucnal's declaration, there is simply no evidence that these yellow wires provide any charge to any fine-tuning

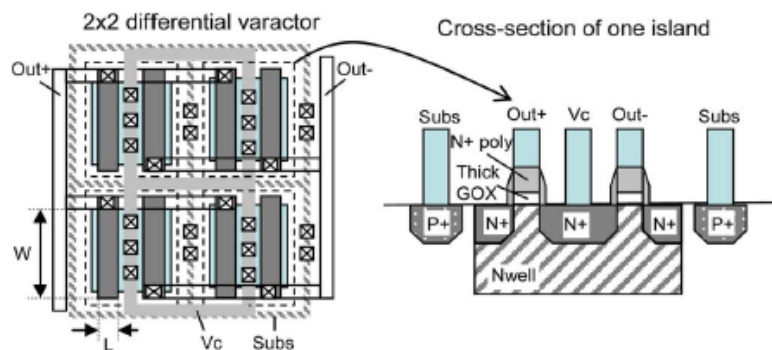
varactor. *Id.* Dr. Prucnal does not identify any connection between these yellow wires and the white “fine tuning varactors” that sit in a 5x5 grid. Looking at Figure 8, the only image that shows both the varactors and what Dr. Prucnal identifies as the extension-conductor segments/connecting segments, there does not appear to be any such connection either.

106. Instead, Dr. Prucnal identifies Figure 2, which is the circuit schematic, but a schematic that fails to show anything more than the existence of an electrical connection, not the specific path the connection takes. Most troubling of this reliance is the fact that a schematic will be identical regardless of the relative location of the two components. For example, two circuits, one with a capacitor located directly below the coil of an inductor and another with a capacitor located elsewhere, would have the exact same schematic, assuming all electrical connections remained identical.

107. Dr. Prucnal also relies, in part, on Figure 5 to support his conclusion. But Figure 5 depicts varactors without any regard for the source of the Out+/Out-/V_c lines. A POSITA would understand that the layout in Figure 5 is configured to intentionally route the Out+/Out-/V_c lines in a manner that minimizes any extra capacitance. Ex.1005, 6. Gonzalez explains that it seeks to minimize the differential current path. *Id.* As a result, a POSITA would not have interpreted the wires of Gonzalez to be “electrode segments” which are defined in the ’582 Patent as to

“serve as electrode plates of the capacitor, capacitive induction is generated between the electrode segments” Ex.1001, 4:41-43, because Gonzalez itself teaches that it positions those wires in a manner that minimizes any incidental capacitance between the wires carrying Out+/Out-/V_c to the various gates. Any actual measurable capacitance between these wires would negatively impact the ability of the fine-tuning varactors to perform their fine-tuning capabilities, by adding extra, uncontrollable capacitance.

108. Moreover, a closer look at Figure 5, with Dr. Prucnal’s “annotations” and coloring removed, shows that while the yellow wires of Figure 8 are at least 5 metal layers above the silicon, in Figure 5 the “Out+ and Out- “fingers” are at most two metal layers above the silicon.



109. In this regard, Gonzalez is simply showing exemplary, stand-alone depictions of various aspects of its modeled design, not a specific circuit drawing of the actual implementation of its VCO.

B. The Images Of Gonzalez Do Not Suggest The Claimed Configuration To A POSITA

110. While Dr. Prucnal goes to great lengths to combine two images from Figure 8 (Ex 1003, Prucnal Declaration, p. 95) Gonzalez does not disclose or teach toward the specified combination.

111. The claims of the '582 Patent require a specific relative placement of the capacitor component with the coil of the inductor component, namely that “the capacitor component is not substantially overlapped with the coil-conductor segment.” Ex.1001, Cl. 1. Dr. Prucnal identifies three images in Gonzalez, none of which show this configuration.

112. A POSITA would understand that Figure 2 is simply a circuit schematic. To begin, the self-ascribed title of this figure within Gonzalez is “schematic,” which a POSITA would understand does not show the relative position of any component, instead it shows the electrical connections between different circuit components. Ex.1005, Fig.2. Dr. Prucnal incorrectly asserts in his declaration that Figure 2 “illustrates spatial relationships.” The schematic of Figure 2 does not depict any spatial relationship. Two circuits, one with a capacitor was located directly below the coil of an inductor, and a second where the capacitor was located elsewhere. Both would have the same exact schematic assuming, all electrical connections remained identical.

113. Other types of circuit depictions, such as the circuit layout of Figure 3-21 of Muh, may show the relative position of components. Ex.1006, 52 (Fig. 3-21). However, Gonzalez, in using a schematic as opposed to including a depiction of a full circuit layout, simply lacks this level of specificity.

114. Dr. Prucnal also relies on Figure 12 of Gonzalez. However, he added annotations without any basis to do so. The un-annotated version of Figure 12 does not show any varactors or capacitors:

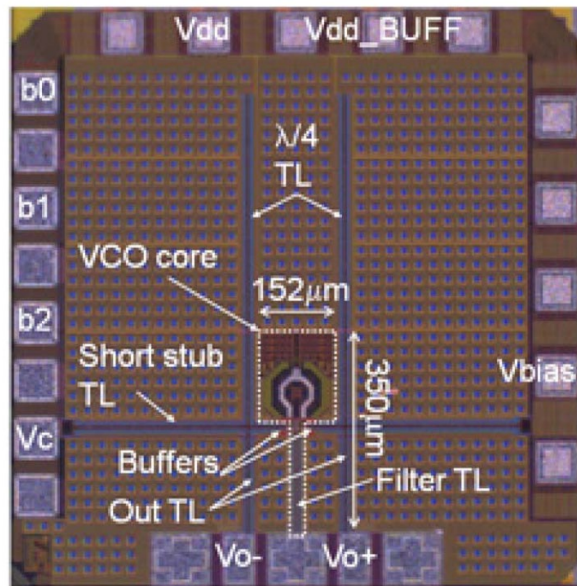
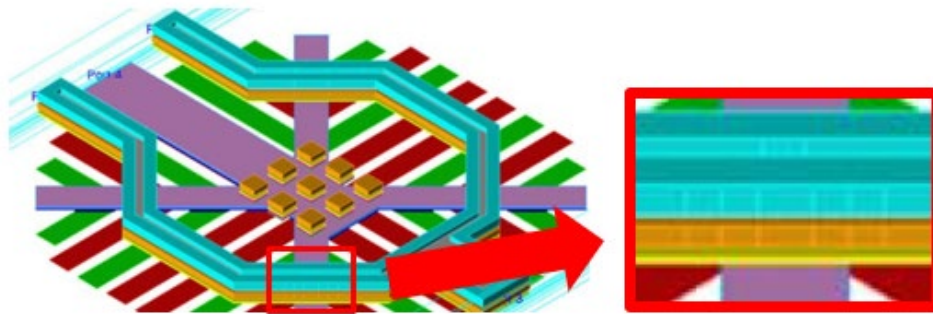


Fig. 12. VCO die micrograph.

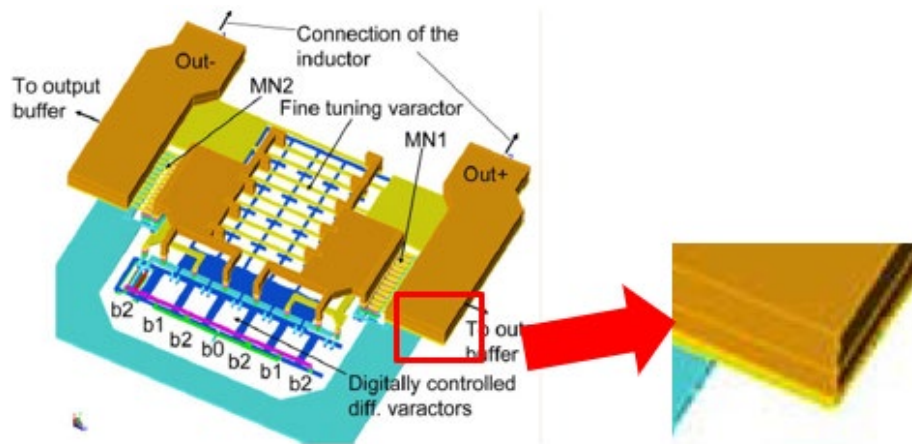
115. The description of Figure 12 is silent with regard to any positioning of the two components (inductor and varactor).

116. Dr. Prucnal also relies on Figure 8 of Gonzalez. However, Figure 8 as it is depicted in Gonzalez, plainly does not depict a combined view that includes both a coil and a capacitor.

117. The coil structure of the inductor of Gonzalez is three layers thick: blue, gold, and yellow. This represents “two upper copper metal layers plus the aluminum metallization layer.” Ex.1005, 6.



118. The bottom portion of Figure 8 depicts, at the “Out+” and “Out-” terminals, a three layer structure instead having a double thick gold layer atop a yellow layer:



119. Gonzalez is clear that it was constructed using design rules that permit the use of six metal layers, M1 through M6. Ex.1005, 8, Fig. 9.

120. These metal layers are built upon a silicon substrate and therefore sit above a silicon layer. These two different images from Figure 8 cannot be combined

as Dr. Prucnal suggests as doing so would create more than 6 metal layers: one blue in the top image, one gold in the top image, one yellow in the top image, two gold in the bottom image, one yellow in the bottom image, one pink in the bottom image, one green in the bottom image, one light blue in the bottom image, and one blue in the bottom image. Even if the blue in the top image is intended to be the same metal layer as the top gold in the bottom image, there are still more metal layers than the design rules permit (two gold, yellow, pink, green, light blue, dark blue). It is clear for review of these images and the paper that the various images that are part of Gonzalez are simply there for illustrative purposes and do not reflect combinable teachings.

121. The descriptions of Figure 8 in Gonzalez themselves indicate that the top portion shows the inductor layout and the bottom portion shows the interconnection of the varactors and the structure of the transistors. Ex.1005, 8. Neither picture is intended to demonstrate the relative positioning of the varactors of the bottom portion of the image and the inductor of the top image. A POSITA would not view these to be combinable as Dr. Prucnal has assumed and relied upon (without basis rooted in Gonzalez itself). These two distinct aspects of Figure 8 have different thicknesses, different numbers of layers, and, apart from using the specification or claims of the '582 Patent as a roadmap to make the combination,

there is no basis to conclude the connection would happen in the manner Dr. Prucnal proposes.

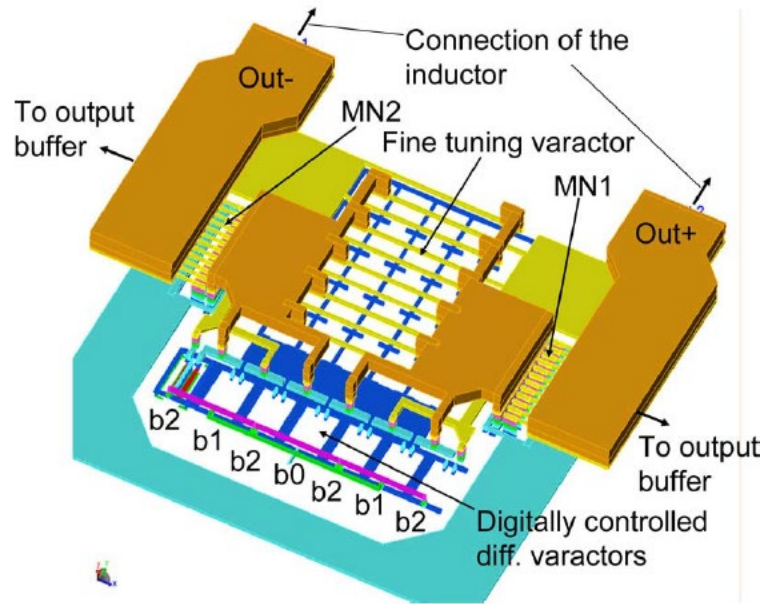
122. A POSITA would not interpret Gonzalez to show or suggest that the claimed capacitor component “is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.” Therefore it is my opinion that Dr. Prucnal has not and cannot show Gonzalez teaches this limitation.

C. Gonzalez does not disclose a “connecting segment”

123. Gonzalez simply lacks any disclosure of what Dr. Prucnal alleges would be the claimed “connecting segments.”

124. The claimed connecting segments must “extend[] corresponding to the two extension-conductor segments in a same direction” and be “respectively overlapped with the two extension-conductor segments in a vertical direction.” Ex.1001, Cl. 1.

125. Gonzalez’s yellow layer of Figure 8 sits below the alleged “extension-conductor segments” (the brown or gold colored portions) and are completely covered in Figure 8:



126. However, there is no disclosure in Gonzalez about the shape or form of this yellow layer in the space below the brown or gold layer. The shape is completely hidden and there is no evidence of what it looks like. It is simply not important for what Gonzalez’s PCells are accomplishing.

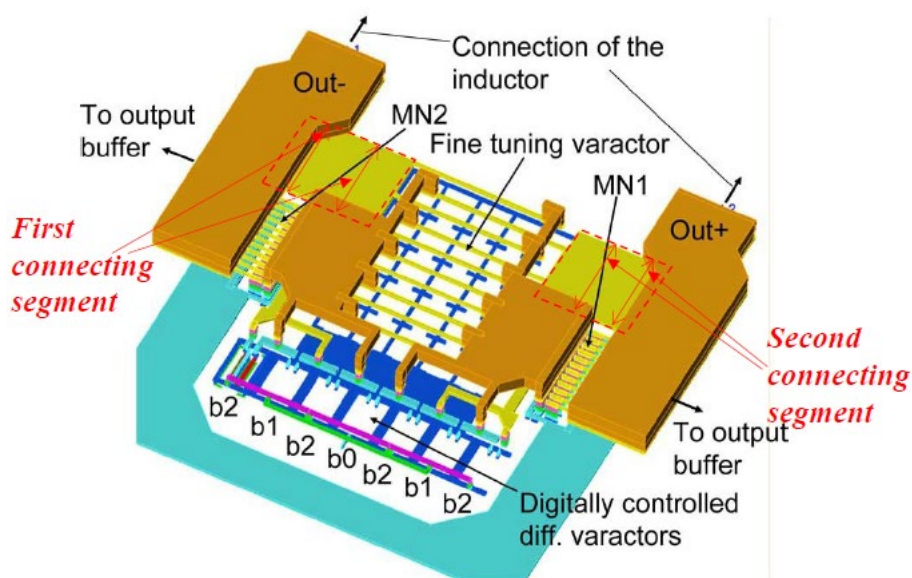
127. There are an infinite number of options of how this yellow layer could be shaped below the two Out+/Out- “paddles.” For example,

- The yellow layer could take the form of a cross-hatch structure beneath the two Out+/Out- “paddles”;
- The yellow layer could be a series of conductors not substantially overlapped by the two Out+/Out- “paddles”;
- The yellow layer could be a series of conductors that extend in a different direction from the direction of the extension-conductor segments; and/or
- The yellow layer could be a series of fingers that extend perpendicular to the direction of the extension-conductor segments.

There may be additional options beyond the above four that come to mind.

128. Because of this lack of disclosure in Gonzalez, there is no credible reason to conclude that they necessarily “extend[] corresponding to the two extension-conductor segments in a same direction,” or that they “are respectively overlapped with the two extension-conductor segments in a vertical direction,” as required by the claims.

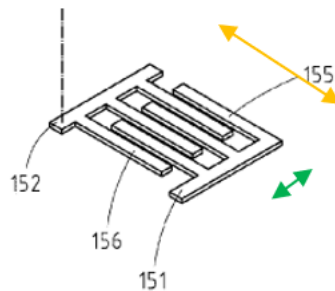
129. Notably, Dr. Prucnal identified one option that would decidedly not meet the claims:



130. In this option (of the countless options for the “yellow portion”), the portions outlined in yellow do not “extend[] corresponding to the two extension conductor segments in the same direction” and are not “respectively overlapped with the two extension-conductor segments in a vertical direction.”

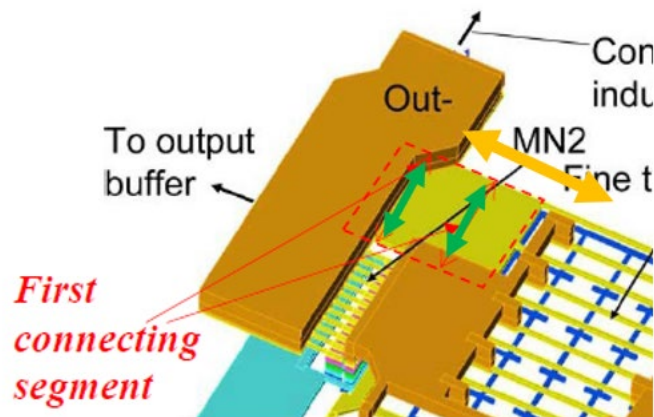
131. As the term is used in the '582 Patent, “extend” means the primary direction that the structure of the component exists in. The '582 Patent explains that “the other end of the first electrode segment 155 extends laterally relative to the coupled first connecting segment 151.” Ex.1001, 5:8-10, Fig. 3.

132. I have provided an annotated example of Figure 3 below depicting how the electrode segment “extends”:



133. In the above image, electrode segment 155 has material that exists in both a direction extending away from 151 and, material that exists in the same direction as the direction 151 extends. Said otherwise, 155 has a length and a width. The length is traditionally the longer of the two dimensions and the width is traditionally the shorter of the two. In Figure 3, the length of 155 extends away from 151 (in a top left to bottom right direction in the above), as indicated by the orange arrow. The width of 155 exists parallel to the direction of 151 (in a top right to bottom left direction in the above), as indicated by the green arrow.

134. Following this understanding, the red “connecting segment” of Dr. Prucnal’s declaration extends in the direction of the orange arrow (as annotated below): the “length” of the red annotated box, and not the green annotated width.



135. The above identified red “connecting segment” over-estimates what the yellow shape could be, but even that image fails to disclose any connecting segment “extending” in the green direction. Further, removing the “guess work” from the above annotation results in a portion of yellow metal that “extends” even more in the orange direction.

136. The yellow structures are simply masked by the alleged “extension-conductor segments,” such that it is impossible to identify the structure that exists below the brown/gold layers. It would be improper to guess as to what that shape may be, and that is simply what Dr. Prucnal has done, guessed. This fails to suggest

the claimed requirement that the connecting segment “extend[] corresponding to the two extension-conductor segments in a same direction.”⁴

D. Gonzalez does not disclose a second component

137. Dependent Claim 2 requires “an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.”

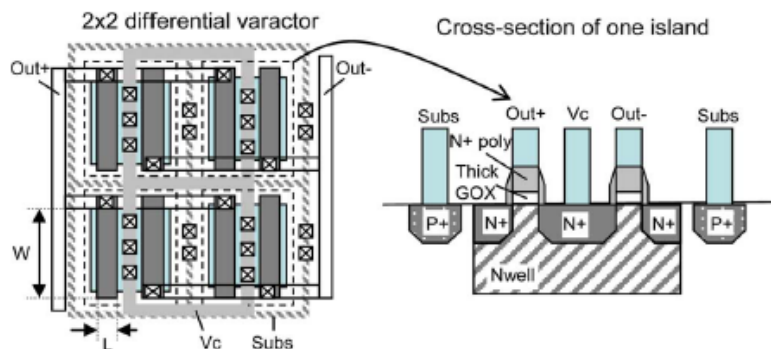
138. Dependent Claim 3 specifies what form that component should take, namely that “the [second] electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.”

139. Gonzalez simply lacks any second insulation layer or electronic component located below the second insulation layer as is required.

140. Dependent claim 2 requires, in short, a second insulation layer below the capacitor component (in a direction opposite the inductor component), and an electronic component located below that second insulation layer.

⁴ My lack of opinion on any other elements of Claim 1 is not an admission that those claim elements are taught by Gonzalez. Further, Dr. Prucnal treats Claims 1 and 9 as identical, so I do not independently analyze Claim 9. However, my opinions apply to the identical claim elements in Claim 9 as appear above for Claim 1.

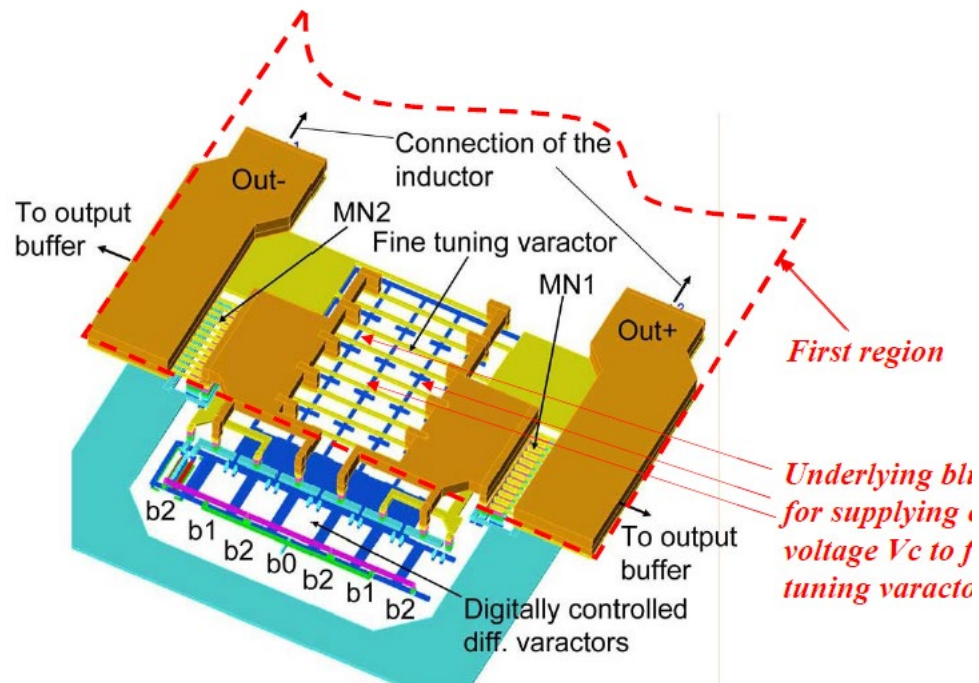
141. Figure 5 of Gonzalez establishes no such arrangement is depicted in Gonzalez. The fine-tuning varactor of Gonzalez appears atop a silicon layer:



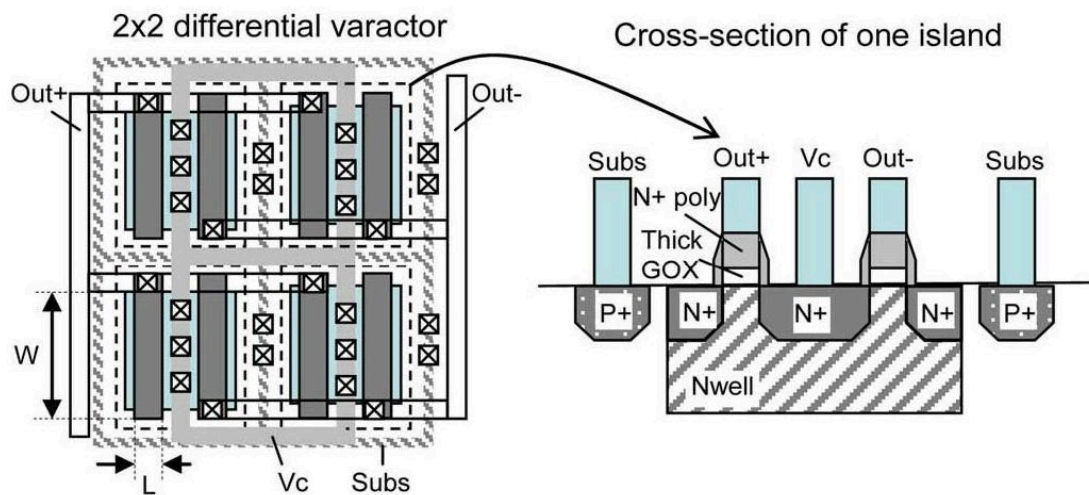
142. Dr. Prucnal's "capacitor component" includes these varactors located in the silicon layer. Gonzalez lacks any disclosure of what exists below these varactors.

143. The two different varactors are explained in Gonzalez to be made from the same structure. Ex.1005, 5. There is no teaching in Gonzalez that any of the digitally controlled differential varactors are located below any silicon layer in which the fine-tuning varactors are located. Moreover, there is no teaching or suggestion in Gonzalez of any insulation layer below any silicon layer in which the fine-tuning varactors are located.

144. Further, this "electronic component" must be "arranged corresponding to the first region." Ex.1001, Cl.2. The differential varactors are not "arranged corresponding to the first region." Instead, even as Dr. Prucnal admits, they are located *outside* the first region:



145. Figure 5 confirms that the V_c lead and the digitally controlled differential varactors are not embedded on an opposite surface of a second insulation layer:



Ex.1005, Fig. 5. Instead, it is clear that they are above, or at least at the same level as the varactors, not below the varactors.

146. Gonzalez lacks any teaching of what is located below the varactors (which themselves include the Nwell). There is no description of a second insulation layer and no description of any additional electrical components below the varactors.

147. As such, I disagree that Gonzalez teaches or suggests the subject matter of Claims 2 and 3.⁵

VIII. Ground 2

148. Dr. Prucnal also relies on the combination of Muh (Ex.1006) and Niknejad (Ex.1007) in his second theory of unpatentability. Again, Dr. Prucnal appears to agree that Muh by itself does not disclose the claimed structure, however what he fails to acknowledge is no prior art reference that he relies on has the claimed configuration of capacitor in an LC circuit.

149. I understand that there is a dispute as to whether Muh itself is prior art. While I am not offering an opinion on that issue and have not reviewed Dr. Hall-Ellis's report, I do simply state that I have never personally used and am unfamiliar with how to search for documents using MARC records. Further, having placed

⁵ I have not offered any independent opinions about claims 4 or 5 for Gonzalez. Regardless, my lack of opinion is not a concession that Gonzalez teaches these dependent claims.

myself in the shoes of a POSITA, it is my opinion that a POSITA in this matter would also be unfamiliar with MARC records and how to use them.

150. I disagree with Dr. Prucnal that a POSITA would have been motivated to combine any teachings of Niknejad with the teachings of Muh, and further disagree that any combination (if proper) would suggest what is claimed by the '582 Patent.

151. First, while each Muh and Niknejad independently disclose finger capacitors, they do not depict or describe the orientation of those finger capacitors. Similarly, while each Muh and Niknejad depict in images LC circuits, they never do so with a finger capacitor, only with plate-style MIM capacitors. Contrary to Dr. Prucnal's suggestions, the combination of Muh and Niknejad actually suggests to a POSITA reasons to orient the capacitor contrary to that orientation of the claims, and instead more akin to the structure of the prior art (such as the Jing reference considered by the Examiner during prosecution).

152. Second, the disclosure of Muh and Niknejad do not support the conclusions alleged by Dr. Prucnal. In this regard, the focus of Muh is on maximizing the Quality-Factor or Q-factor of its LC circuit. Ex.1006, 31, 41. To accomplish this, the capacitor is placed as close to the coil portion of the inductor as possible.

153. Indeed, the only instance of the claimed configuration is found in the '582 Patent itself. No other reference shows a finger capacitor in the claimed manner, having an extension conductor segment overlapping a connecting segment that extends in the same direction as the extension conductor segment, and having electrode segments extending laterally relative to a connecting segment.

A. No Basis To Orient any finger capacitor as claimed

154. Niknejad explains that when there is a need to “decrease finger resistance and inductance,” as is the case in an LC circuit, a POSITA would be motivated to use “a large number of short fingers in parallel.” Ex. 1007 at 73. During the co-pending ITC proceedings, Dr. Prucnal explained that it would be favorable to decrease finger resistance in an LC circuit. Ex. 2004 at 1134:2-3 (“If one could decrease finger resistance, that would be favorable.”)

155. Notably, this is exactly how the prior art reference, Jung (Ex.1033) depicts its own capacitors. As shown below, in Jung, the leg 125 of the inductor overlays a capacitor structure that includes bus lines 105 and finger elements 115.

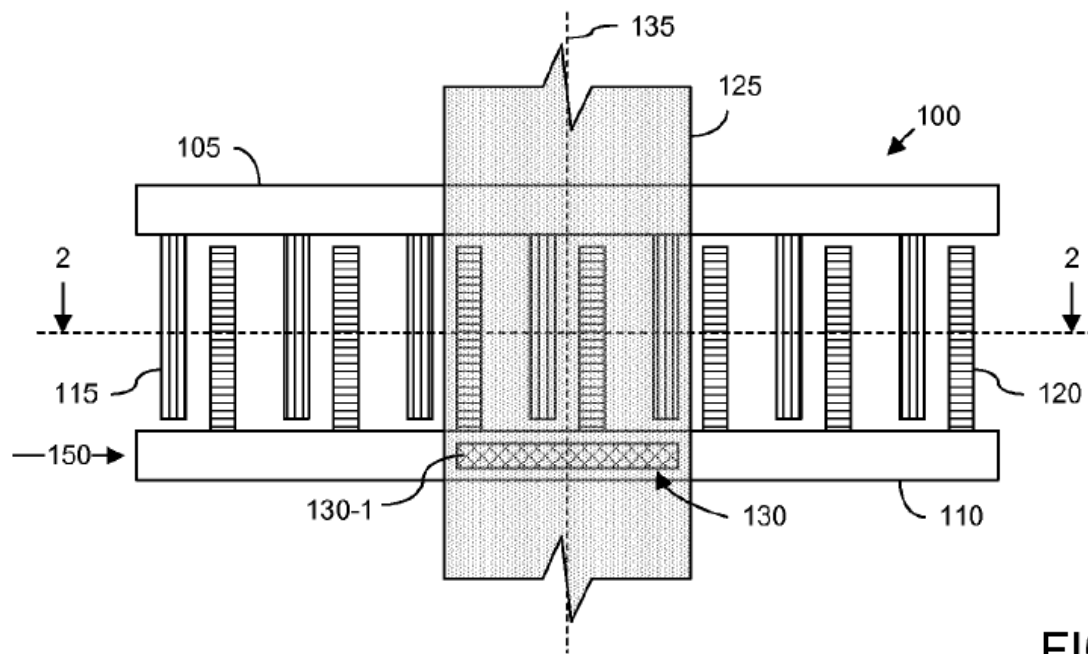


FIG. 1

Ex.1033, Fig. 1.

156. Niknejad teaches that a finger capacitor should have “a large number of short fingers in parallel” to have “smaller finger resistance.” Ex.1007, 28.

157. Dr. Prucnal and I both agree that it is better to decrease finger resistance in an LC circuit. As a result, we both agree that a POSITA reading Niknejad would be similarly driven to have a finger capacitor with a larger number of short fingers.

158. Specifically, Niknejad confirms that there are two ways to design a finger capacitor: (1) with a larger number of short fingers or (2) a smaller number of long fingers. Ex.1007, 28. It explains that “[t]he former structure results in smaller finger resistance and inductance but larger lead parasitics due to the transition from

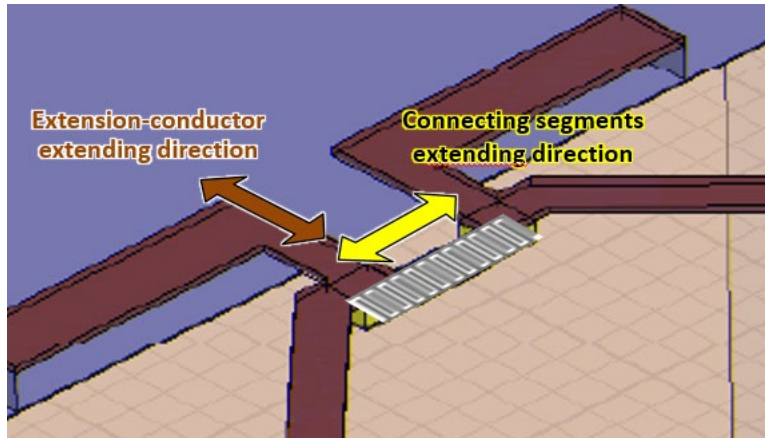
the signal lines to the capacitor plates. The latter structure exhibits the opposite tradeoff.” Ex.1007, 28.

159. LC circuits that employ finger capacitors attain certain benefits from decreasing finger resistance. Dr. Prucnal agrees that “[i]f one could decrease the finger resistance, that would be favorable.” Ex.2004 at 1135:2-5. Other advantages include those set forth above in paragraphs 154-158.

160. These advantages stem, in part, because decreasing the series resistance of the fingers increases the Q factor, again, an express goal of Muh. *See* Ex.2004 at 1134:15-24.

161. Additionally, a POSITA would know that while any curvature of a metal provides some degree of inductance, the designed inductance of the inductor will come from the loops of the coil. Ex.1007, 25 (3.1.2). Further, a POSITA would recognize, like Dr. Prucnal admitted, one would try to minimize any “ancillary inductance from the fingers.” Ex.2004 at 1135:8-12. It is best to minimize the additional inductance within the capacitor component to have control over the amount of total inductance in the LC Circuit. In an LC circuit, a larger number of shorter fingers can be used to obtain all of the necessary capacitance and, as discussed above, allows for the minimizing of any ancillary inductance. In view of the above, a POSITA reading Niknejad would be motivated to design a capacitor in an LC circuit having larger number of short fingers. Ex.1007, 28. To the extent any

POSITA would be motivated to change the capacitor of Muh (which I disagree they would) from a plate capacitor to a finger capacitor, the resulting configuration would be like this:



162. A POSITA would not orient the finger capacitor to have fewer and longer fingers, which is what would be required for the finger capacitor to be oriented as Dr. Prucnal suggests. Doing so would result in the capacitor adding unwanted parasitic inductance. Furthermore, the extension-conductor segments will contribute parasitic inductance with relatively high loss compared to the octagonal part of the inductor geometry and a POSITA would not be motivated to offset the capacitor structure.

163. Niknejad teaches the same LC circuit structure as that of Muh:

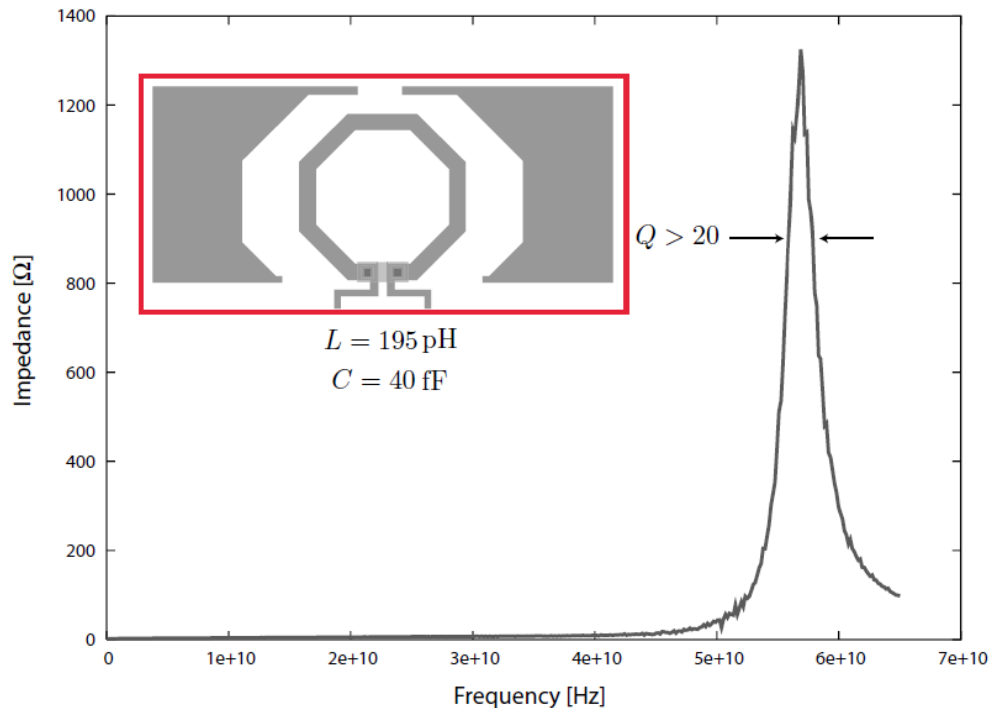


Fig. 3.10 Measured resonance of a mm-wave tank formed by a ring inductor and MIM capacitors.

Ex.1007, 26 at Fig. 3.10. This location and use of a MIM capacitor is exactly the same as that of Muh. Ex,1006, 58.

164. Muh (and Niknejad) deliberately position the capacitor of the LC circuit in the area under the coil-conductor segment. They do so because that orientation improves the Q factor of the LC Circuit. In contrast, the '582 Patent accepts the lower Q factor in exchange for significant benefits in reducing parasitics and phase noise, and the stated benefit of achieving a beneficial size and arrangement of interconnecting wires. Ex.1001, 1:63-2:3, 12:51-54.

165. Muh and Niknejad show *only* LC circuits with capacitors that are overlapped by, and connected to, the coil-conductor segment, which is a design

choice made explicitly to improve the Q factor. Ex.1006, 58; Ex.1007, 26. The two references only teach the use of a larger number of shorter fingers. Together those teachings show that a POSITA would not be motivated to modify Muh and Niknejad to have a capacitor component that extends beyond the area they identified for such capacitors and would not select finger lengths that are longer, which is what would be required in Petitioner's proposed configuration.

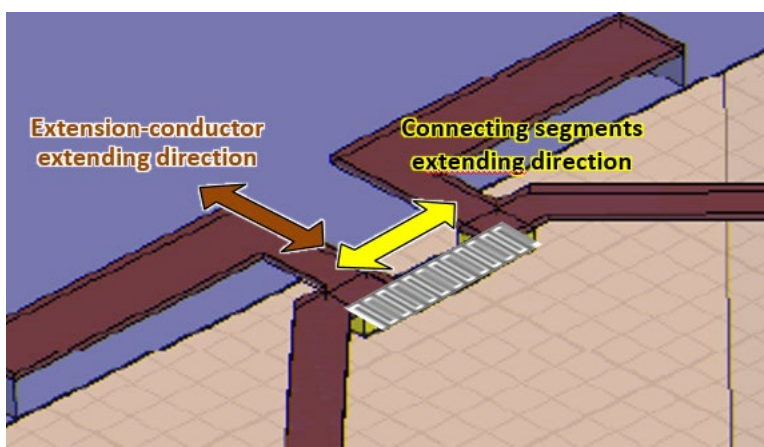
166. The prior art, including Jing and Muh, taught different orientations in order to achieve other goals, such as higher Q. *See Supra*. The insight, and a key inventive concept of the '582 patent, is that orienting the capacitor component in a specific manner, in "the prime real estate" of the first region of the inductor, would achieve significant benefits.

167. Neither Muh, nor Niknejad, describe any instance of a connecting segment of a capacitor component located below any extension conductor segment of an inductor component and extending in the same direction as the extension conductor segment.

168. Muh is entirely silent with regard to vias. I have reviewed Muh and find no instance of vias described. However, if a POSITA were to employ vias in the connection between any capacitor of Muh and the inductor of Muh, they would be used to connect one end of the coil-conductor segment to one of the connecting segments, and the other end of the coil-conductor segment to the other connecting

segment. The Jing reference on which the examiner relied shows how this was done using either a “trench’ via” or “standard sized” vias. Ex.1033 at 5:19-28, Fig.1.

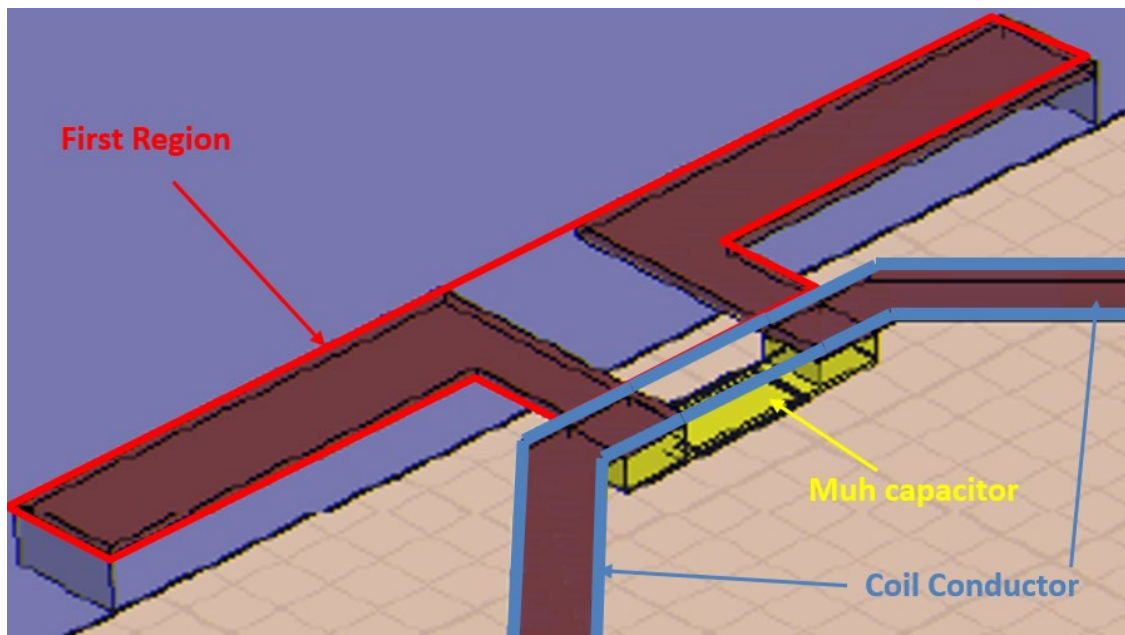
169. To the extent any capacitor would replace the plate capacitor of Muh, it would be oriented rotated 90 degrees to what is required by the claims of the ’582 Patent:



In this position, the capacitors match the prior art reference Jing (Ex.1033). Ex.1033, Figs. 1, 3, 4. The orientation of Jing’s “extension conductor segment” 125 and “connecting segment” 105/110 is unaddressed by Dr. Prucnal. Dr. Prucnal disregards that the orientation of Jing, the only actual orientation that exists in the prior art references of record. Doing so, without any basis in the prior art, is only further evidence of the hindsight bias that infects Ground 2). The orientation of Jing is far more likely and, contrary to the Petition’s unsupported conclusions, the simplest and most reliable design choice, as it was already proven to exist. The only reference that I have reviewed in this proceeding that includes a finger capacitor oriented in the claimed manner in this proceeding is the ’582 Patent itself.

B. The Capacitor of Muh and Niknejad Is Substantially Overlapped with the Coil-Conductor Segment

170. Under the proper construction of “extension conductor segments” the capacitor of Muh and Niknejad is substantially overlapped with the coil-conductor segment. As shown in the below annotated image of Muh, the coil-conductor completely overlaps the capacitor:



Ex.1006, 58. In fact, the capacitor of Muh does not correspond at all to the first region, being located completely outside the first region. Because of this overlap, Muh also fails to teach or suggest any electrodes “located below the first region” as that term is used in the ’582 Patent.

171. There is no basis in Muh or Niknejad to suggest to a POSITA that it should move the capacitor from the depicted locations into the first region defined by the coil-conductor segment and the extension-conductor segments. In fact, as

discussed above, Muh expressly states that as part of his research, the author was trying to maximize the Q factor of its VCO circuit. Ex.1006, 41. Niknejad similarly explains that it was a known goal to try to maximize the Q factor. Ex.1007, 29 (“The quality factor of capacitors drops inversely with frequency due to any series resistance, and this is a severe limitation for on-chip structures.”). A POSITA would have understood that keeping the capacitor as close to the coil as possible would accomplish this maximization goal. Ex.2006, 37 (“...compact layout”). For instance, this will keep the routing between the inductor and the capacitor as short as possible, thus minimizing series resistance that can significantly reduce Q, especially at the high frequencies (60 GHz) considered in Muh.

172. Muh’s capacitor is connected to the two ends of the coil, which is fundamental to minimizing the series resistance and thus maximizing the Q value of the LC circuit. To the contrary, the claims of the ’582 Patent require that the capacitor be located further away from the nearest most point of the coil, thereby slightly reducing the Q-value to provide the other benefits attained by the claimed configuration. A POSITA would not have modified Muh to move the capacitor component into the first region because such a modification would be opposite Muh’s stated goal of maximization of Q value. Ex.1006, 31, 41.

173. Niknejad also shows the capacitor of its LC circuit in this same Q-maximization position. Ex. 1007 at 26, Fig.3.10.

174. Nothing in either of Muh nor Niknejad (or any other evidence from before the '582 Patent) suggests that adding a finger capacitor of Niknejad to the LC Circuit of Muh would yield an LC circuit in which the capacitor component is not substantially overlapped by the coil-conductor segment as is required by the '582 Patent. Similarly, nothing in either of Muh nor Niknejad (or any other evidence from before the '582 Patent) suggests an LC circuit in which the electrodes segments are “located below the first region.”

175. There is simply no basis to modify Muh, and the teachings of Muh and Niknejad are at odds with the modification Dr. Prucnal advances.

C. Dr. Prucnal’s Obviousness Opinion is Fraught with Hindsight Bias

176. Dr. Prucnal’s opinions suffer from hindsight bias. None of the references he identifies actually show the claimed configuration. The only reference that shows the claimed configuration is the '582 Patent itself.

177. Muh discloses two LC tank test structures (Fig. 3-22) for the designed push-push VCO. One test structure includes only the MOS varactors (which are active devices), and the other test structure includes MOS varactors and MIM capacitors (connected to the tank in order to estimate MIM capacitors’ effect on the resonant frequency). Nothing in Muh suggests the use of a finger capacitor (also referred to as “MOM (metal-oxide-metal) capacitor” by Niknejad) in the LC tank test structure for the designed push-push VCO. In addition, the MOS varactors in

these two LC tanks substantially overlap with the coil-segment of the inductor, which teaches away from the claimed invention of '582 Patent and undercuts the conclusion that a POSITA would be modified to change Muh to the claimed structure.

178. Muh also discloses that MOS varactors used in the LC tank for the push-push VCO are active device (e.g., the capacitance is variable based on the controlled gate voltage). However, the MOM (metal-oxide-metal) finger capacitor of Niknejad is a passive device where its capacitance is not variable based on input voltage as the MOS varactor. Muh further identifies that the challenge using the HFSS simulation, which AMD improperly relies upon, lies in making sure that the simulated capacitor has a similar capacitance as the fabricated capacitor. Ex.1006 at 55. If a structurally more complicated interdigitated finger capacitor is used in the HFSS, it would defeat the purpose of simplifying the structure in the HFSS mode, and make the evaluation of the accuracy of HFSS more difficult than its original purpose.

179. Niknejad only describes using MIM capacitors (such as the plate capacitors of Muh) in tank (LC) circuits. See Ex.1007, 26. In no instance does Niknejad describe using the finger capacitors in place of a MIM capacitor, and Niknejad certainly does not describe how to orient such a capacitor if one were used.

180. Any efforts to replace a horizontal plate capacitor used in the HFSS model with a more complicated multilayer stacked finger capacitor disclosed in Niknejad, which further requires the metal layers to connect together through the (preferably) maximum number of vias, would require extensive modification and could be contrary to design rules governing the structure. Ex.1007, 27 (Niknejad's teachings on vias). Design rules are mandated by the foundry as a means to ensure that submitted chip designs can actually be fabricated, and chief among these are rules governing the minimum width individual pieces of metals can have, and minimum spacing that can exist between these pieces of metal. Rules such as these place upper limits on the amount of capacitance realizable in a fixed area, thus calling into question whether a capacitor technology that arranges metal in one geometry (such as a MIM capacitor) can be replaced with a technology that arranges metal in an entirely different geometry (such as a finger capacitor). In particular, MIM capacitors are implemented using a specialized layer, unused for other routing, that is very closely spaced vertically to the next routing layer beneath, allowing for high levels of capacitance density; special design rules exist to accommodate this structure, while finger capacitors are less commonly able to take advantage of specially reduced metal spacing rules in order to increase capacitance density.

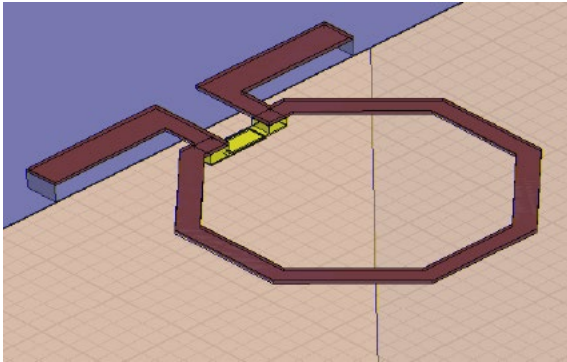
181. Further, AMD's reliance on only a single layer of Niknejad's finger capacitor is misplaced and contrary to the teachings of Niknejad. Ex.1007, 72

(“[e]ach finger consists of all available metal layers stacked on top of each other to decrease its resistance which increasing both its quality factor and the self-resonance frequency”). A POSITA would not have made the combination AMD alleges.

182. There is no explanation as to why a POSITA would have made any changes to Muh or Niknejad other than suggesting “it was straightforward.” Ex.1003, ¶250.

183. Dr. Prucnal implies at ¶252 that a POSITA would be inclined to substitute a finger capacitor for the alleged capacitor used in Muh in pursuit of cost savings, stating that “Niknejad discloses that finger capacitors (i.e., MOM capacitors ‘are less expensive than Metal-Insulator-Metal (MIM) capacitors’” (Prucnal at ¶252 quoting Niknejad EX-1007). He fails to mention, however, that in the very next sentence Niknejad suggests that the economics may in fact fall in favor of the MIM capacitor implementation, stating “[i]f the density of MIM capacitors are sufficiently larger than “finger” structures, then the area savings may outweigh the additional fabrication costs (Niknejad EX-1007 at 28).

184. Finally, I note that both Muh and Niknejad have the same LC tank structure:



Ex.1006, 58 (left); Ex.1007, 26 (right, and rotated). In both, a plate capacitor is located in the same connection point to the inductor coil. Contrary to Dr. Prucnal's opinion, there would not have been any expectation of success to support the alleged combination. A chapter of the textbook of origin for Niknejad confirms that "high performance oscillators and dividers operating in the mm-wave range continue to pose difficult challenges even in today's technology" and it goes on to explain that "careless modification of the structure can lead to unpredictable results." Ex.2006, 1, 9. Moreover, there is no basis rooted in any reference or any prior art perspective of a POSITA to support the combination advanced by Petitioner and Dr. Prucnal. Accordingly, there is no showing that a POSITA would have modified Muh to arrive at the claimed capacitor configuration.

D. Claim 4

185. Claim 4 has a first region that is more narrow than the first region of independent Claim 1. Specifically, Claim 1 recites a first region "defined *by* the two

extension-conductor segments and the coil-conductor segment” whereas Claim 4 recites a first region “defined *between* the two extension-conductor segments.”

IX. Reservation of Rights

186. I reserve the right to amend or supplement this declaration as this case proceeds and any additional information comes to light.

187. I understand that traditionally no live expert testimony is used at the PTAB, and I presently have no plans to testify, however should I be asked, I reserve my right to use exhibits to summarize or exemplify my opinions (including exhibits I have not yet created) if called to testify.

188. If it would be helpful to the Tribunal, I am willing and able to provide additional background.

189. I further reserve the right to respond to any opinions presented by any of Respondents’ experts regarding the meaning of any claim term or limitation within the Asserted Claims. I also reserve the right to provide further opinions in this case, such as opinions regarding non-infringement and/or invalidity of the Asserted Patents, if requested to do so.

190. I declare under penalty of perjury that this declaration contains a true and correct statement of my opinions, based on the information available to me.

Dated: February 8, 2024



Dr. Joshua Phinney

Appendix A

Curriculum Vita

Joshua W. Phinney, Ph.D., P.E.
Principal Engineer

Professional Profile

Dr. Joshua W. Phinney is a Principal Engineer in Exponent's Electrical Engineering and Computer Science practice. Dr. Phinney's background is in electrical and electronic engineering, particularly related to power electronics, electromagnetics, and electromechanics. His specialties include power supplies, radio-frequency electronics, control systems, printed circuits, integrated-circuit packaging, magnetics design, and power transmission and distribution. He has related experience in embedded software, acoustics, and numerical methods for optimization and simulation.

At Exponent, Dr. Phinney has assisted clients with identifying the root cause of failures in mobile electronic devices, industrial and automotive controllers, capacitors, transformers, amplifiers, and power supplies. He has testified in patent and trade secret litigation regarding computer hardware and software, audio circuitry, mobile telephones, tablets, power supplies, control systems, hard disk drives, and electronic instruments. In addition, Dr. Phinney has assisted clients with electromagnetic assessment issues pertaining to utility and communication infrastructure. These issues include permitting, interference, and environmental impact of radar, AC and HVDC transmission lines, substations, photovoltaic installations, generators, broadcast antennas, and electrified mass transit systems. In addition, Dr. Phinney has written software for data classification and machine learning in radar-return and other image-analysis applications.

Dr. Phinney received his Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology. His doctoral work centered on miniaturization of power converters and electromechanical power conversion. He has related experience in radio-frequency electronics (particularly phase-locked loops and RF amplifiers), network synthesis, system identification, and control. Dr. Phinney is the co-inventor on patents for improving the performance of capacitors, EMI filters, and common-mode chokes.

Academic Credentials and Professional Honors

Ph.D., Electrical Engineering, Massachusetts Institute of Technology, 2005
S.M., Electrical Engineering, Massachusetts Institute of Technology, 2001
B.S., Electrical Engineering, University of Illinois at Chicago (*summa cum laude*), 1999
B.A., Ancient and Classical Languages, Philosophy, Wheaton College, 1995

2004 IEEE Power Electronics Society Transactions Prize Paper Award (for the paper "Filters with Active Tuning for Power Applications"); 2003 William M. Pormoy Prize Paper Award (Awarded by the Power Electronics Devices and Components Committee of the IEEE Industry Applications Society)

1993-1994 Lawrence Livermore National Laboratory, Nuclear Chemistry Division. Associated Western Universities internship: Neural-network classification of gamma-ray detector events.

Work History

2005-*present* Exponent, Inc.

Licenses and Certifications

Registered Professional Electrical Engineer, New York, #084129

Languages

German

Patents

U.S. Patent No. 7,242,269: Filter Having Parasitic Inductance Cancellation, July 2007 (with D.J. Perreault and T.C. Neugebauer).

U.S. Patent No. 6,937,115: Filter Having Parasitic Inductance Cancellation, February 2002 (with D.J. Perreault and T.C. Neugebauer).

Publications

Phinney JP, Perreault DJ, Lang JH. Synthesis of lumped transmission-line analogs. IEEE Transactions on Power Electronics 2007; 22(4):1531–1542.

Phinney JP, Perreault DJ, Lang JH. Radio-frequency inverters with transmission-line input networks. IEEE Transactions on Power Electronics 2007; 22(4):1154–1161.

Phinney JP, Perreault DJ, Lang JH. Multi-resonant microfabricated inductors and transformers. IEEE Power Electronics Specialists Conference 2004; 4527–4536.

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Neugebauer TC, Phinney JP, Perreault DJ. Filters and components with inductance cancellation. IEEE Transactions on Industry Applications 2002; 939–947.

Phinney JP, Perreault DJ. Filters with active tuning for power applications. IEEE Power Electronics Specialists Conference 2001; 363–370.

Batzer MA, Arcot SS, Phinney JP, et al. Genetic variation of recent Alu insertions in human populations. Journal of Molecular Evolution 1996; 42(1):22–29.

Academic Appointments

Joshua W. Phinney, Ph.D., P.E.

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Adjunct Professor, Hofstra University, 2008-2018

Peer Reviewer

- IEEE Transactions on Power Electronics, 2013-2015
- Health Physics Journal, 2007
- IEEE Power Electronics Letters, 2006
- Power Electronics Specialists Conference, Recife, Brazil, 2005
- Power Electronics Specialists Conference, Jeju, Korea, 2006

Professional Affiliations

- Institute of Electrical and Electronic Engineers (member)
- Tau Beta Pi

Joshua W. Phinney, Ph.D., P.E.
Principal Engineer

Testimony

Convolve, Inc. and MIT v. Compaq Computer Corp. and Seagate Technology, LLC.
Case No. 00 CIV. 5141 in the United States District Court, Southern District of
New York. Deposition 2008

IBM v. ASUSTek Computer, Inc., ASUS Computer International, Pegatron Corporation,
and Unihan Corporation. Certain Computer Products, Computer Components and
Products Containing Same, Case No. 337-TA-628 before the International Trade
Commission. Deposition and trial 2008

Xentaur Corporation v. Bedros Bedrossian. Index No, 23403/06 in the Supreme Court of
the State of New York, County of Suffolk. Trial testimony 2010

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and Components Thereof, Case No. 337-TA-796 before the International Trade
Commission. Deposition and trial 2011, 2012

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before the U.S. Patent Trial and Appeal Board. Depositions 2014.

Smart Skins LLC v. Microsoft Corporation. Case No. 2:15-CV-00544-MJP in the United
States District Court, Western District of Washington at Seattle. Deposition 2016.

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testimony 2016.

IPS Group, Inc. v. Duncan Solutions, Inc. and Duncan Parking Technologies, Inc., Case
No. 3:15CV1526-CAB (MDD) in the United States District Court, Southern District of
California. Deposition 2017.

Maxell, Ltd. v. Huawei Device USA, Inc., Huawei Device Co., Ltd., and Maxell, Ltd. v. ZTE Corporation, and ZTE USA, Inc., Lead Case No. 5:16-cv-00178-RWS in the United States District Court, Eastern District of Texas, Depositions and trial 2018.

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Siemens Industry, Inc. v. Westinghouse Air Brake Technologies Corp. and Wabtec Railway Electronics, Inc., Case No. 1:16-CV-284-LPS in the United States District Court, District of Delaware. Deposition 2018, trial 2019.

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Spark Connected v. Semtech Corp., Case No. 4:18-CV-00748 in the United States District Court, Eastern District of Texas, Sherman Division. Hearing 2019.

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BlueRadios, Inc v. Kopin Corporation, Inc., Case No. 16-CV-02054-JLK in the United States District Court, District of Colorado. Deposition 2019.

The Hillman Group, Inc v. KeyMe, LLC., Case No. 12:19-CV-00209 in the United States District Court Eastern District of Texas, Marshall Division. Depositions 2020, 2021. Trial 2021.

Tractel Ltd. v. WTC Tower 1, LLC., AAA Case No: 01-18-0000-9638. Hearing 2020.

KeyMe, LLC. v. The Hillman Group, Inc., Case No. 19-1539-LPS in the United States District Court for the District of Delaware, Deposition 2021.

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Bel Power Solutions, Inc. v. Monolithic Power Systems, Inc., Case No. 6:21-cv-655-ADA in the United States District Court for the Western District of Texas, Waco Division Deposition 2023.

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