

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES,	) Case No. IPR2023-00788
INC.,	)
	) U.S. Patent No. 9,590,582
Petitioner	)
	)
vs.	)
	)
REALTEK SEMICONDUCTOR	)
CORPORATION,	) REMOTE DEPOSITION OF
	)
Patent Owner	) DR. PAUL R. PRUCNAL

TRANSCRIPT of the stenographic notes of the
proceedings in the above-entitled matter, as taken by
and before NANCY CARIDES, RMR, CRR, Certified Court
Reporter and Notary Public of the State of New Jersey,
held via Zoom Videoconference at various locations,
with the witness located in Sanibel, Florida, on
Thursday, January 25, 2024, commencing at 3:23 p.m.

Page 2 1 A P P E A R A N C E S: (All via Zoom) 2 FOR THE PETITIONER: 3 WINSTON & STRAWN, LLP BY: JOSEPH C. MASULLO, ESQ. 4 BRIAN E. FERGUSON, ESQ. 1901 L Street, N.W. 5 Washington, D.C. 20036 202-282-5897 6 jmasullo@winston.com beferguson@winston.com 7 8 WINSTON & STRAWN, LLP BY: CHARLES LIU, ESQ. 9 2121 North Pearl Street Suite 900 10 Dallas, Texas 75201 214-453-6423 11 ccli@winston.com 12 FOR THE PATENT OWNER: 13 K&L GATES, LLP 14 BY: R. GREGORY PARKER, ESQ. 501 Commerce Street 15 Suite 1500 Nashville, Tennessee 37203 16 615-780-6751 greg.parker@klgates.com 17 18 K&L GATES, LLP BY: ERIK J. HALVERSON, ESQ. 19 4 Embarcadero Center Suite 1200 20 San Francisco, California 94111 415-882-8238 21 erik.halverson@klgates.com 22 --- 23 24 25	Page 4 1 (All attorneys have agreed to the 2 witness being sworn in remotely.) 3 (Documents have been premarked for 4 identification.) 5 --- 6 DR. PAUL R. PRUCNAL, after having been 7 first duly sworn, was examined and testified 8 as follows: 9 --- 10 DR. PAUL R. PRUCNAL, after having been 11 first duly sworn, was examined and testified 12 as follows: 13 --- 14 BY MR. HALVERSON: 15 Q. Good afternoon, Dr. Prucnal. We won't 16 go back through all of the introductory stuff you did 17 this morning, but the same ground rules apply for this 18 half. To the extent you don't understand a question, 19 please ask, so that we can make sure we're on the same 20 page. Otherwise, the transcript will reflect an 21 answer, and we'll assume you understood the question 22 as it was posed. Does that make sense? 23 A. Yes. 24 Q. And if you need a break at any time, by 25 all means, go ahead and ask. The only caveat to that
Page 3 1 1 I N D E X 2 2 WITNESS PAGE 3 3 DR. PAUL R. PRUCNAL 4 4 BY MR. HALVERSON: 4, 102 5 5 BY MR. LIU: 98 6 6 --- 7 7 8 8 E X H I B I T S 9 9 NUMBER DESCRIPTION PAGE 10 10 Exhibit 582-1001 U.S. Patent No. 9,590,582 6 11 11 Exhibit 582-1003 Prucnal '582 Patent 6 12 12 Declaration 13 13 Exhibit 582-1005 Gonzalez article 23 14 14 Exhibit 582-1006 Muh Thesis 64 15 15 Exhibit 582-1007 Niknejad mmWave book excerpt 74 16 16 Exhibit 582-1032 Daley Patent Application 86 17 17 Exhibit 582-1033 Jing U.S Patent Publication 86 18 18 19 19 --- 20 20 21 21 22 22 23 23 24 24 25 25	Page 5 1 is to the extent there is a question pending, I would 2 love it if you would give an answer to that question 3 before we take that break. Is that okay? 4 A. Yes. 5 Q. And then in addition to Charles and 6 J.C., is there anybody else there in the room with 7 you? 8 A. Brian Ferguson. 9 Q. And do you have any papers or anything 10 else in front of you right now? 11 A. Nothing in front of me. I have some 12 reports that are unmarked on a table in the room 13 elsewhere. 14 Q. Would you prefer to use the physical 15 copies rather than the Exhibit Share? 16 A. Well, I think so far it's worked okay. 17 And sometimes when we need to have multiple things 18 open at one time, it helps to have the physical 19 document, but let's go ahead and try without them. 20 Q. Sounds good. And if at any point you 21 would rather use the physical copy, let me know, and 22 we can figure out how to make sure that we are all 23 talking about the same thing. But we definitely want 24 to make sure you have the information that you need to 25 answer the questions. All right?

Page 6 1 A. Thank you. Yes. 2 Q. So, in front of you in the Exhibit 3 Share folder, I've added Exhibit 582-1001 and Exhibit 4 582-1003, the second of which is your declaration in 5 IPR2023-00788, as it relates to U.S. Patent No. 6 9,590,582. Is that right? 7 (Exhibit 582-1001 and Exhibit 582-1003 8 were introduced.) 9 THE WITNESS: Well, I don't see. I 10 have the Marked Exhibits open, and I do see my 11 '582 declaration, but I don't see the other 12 document, 582-1001, that you mentioned. 13 BY MR. HALVERSON: 14 Q. If you refresh that page, sometimes 15 Exhibit Share takes a second to actually register the 16 upload. 17 A. Okay. Now it's there. 18 Q. And U.S. Patent No. 9,590,582, which is 19 marked as Exhibit 582-1001, is it fair to call that 20 the '582 patent? 21 A. Yes. 22 Q. If I say that, you'll know what I'm 23 talking about? 24 A. Of course. 25 Q. And then the other exhibit there is	Page 8 1 A. No. I'm just making sure my phone is 2 off. No, there's nothing that I would change. 3 Q. All right. So, in paragraph 2, you 4 list a number of exhibits that you referred to in 5 preparing your declaration, right? 6 A. Yes. 7 Q. So Exhibit 1003 there is the 8 declaration of Dr. Paul Prucnal. Do you see that? 9 A. Yes. 10 Q. What were you reviewing when you were 11 preparing this declaration that in your mind was 12 Exhibit 1003? 13 A. Oh, I think I was just reviewing the 14 declaration that I was working on. I don't think 15 there was another declaration. 16 Q. That is intending to mean this document 17 that we're looking at right now? 18 A. I think so. I'm not one hundred 19 percent certain, but I do think so. 20 Q. Then as far as your opinions in the 21 declaration, as far as I could tell, you are not 22 offering any opinions about the prior art status of 23 any of these documents that you rely on in here. Is 24 that correct? 25 A. That is correct.
Page 7 1 your declaration in the IPR that's related to the '582 2 patent; is that right? 3 A. Yes. 4 Q. And if you scroll all the way to the 5 back of that declaration, we see your signature there. 6 A. I haven't opened it. I was actually 7 just looking at the labels. So, I've opened my 8 declaration. That's my signature at the end. 9 Q. So, I want to talk to you a little bit 10 about what went into this declaration. So, if you go 11 back to the beginning of the declaration, a couple 12 pages in, I want to talk about page 4, which is the 13 second paragraph of your '582 declaration. Let me 14 know when you're there. 15 A. I'm there. 16 Q. So, in paragraph 2, you list a number 17 of documents that you reviewed in preparation for your 18 deposition; is that right? 19 A. Yes. 20 Q. And actually, before I dive into that, 21 have you reviewed your declaration in preparation for 22 today? 23 A. Yes, I have. 24 Q. Is there anything that you would 25 change?	Page 9 1 Q. And so, did you identify any of these 2 documents to counsel in preparation of this 3 declaration? 4 A. Any of the prior art documents? 5 Q. Any of the exhibits in paragraph 2. 6 A. I don't recall that, exactly, either. 7 I know that I did some research. I know that I was 8 reading a lot. I know that I was offering things. 9 I'm not sure, at this point, what ended up in this 10 list. But if I relied on it, it should have ended up 11 in this list. 12 Q. So, my question was less about whether 13 or not it's in the list and more about whether or not 14 you found it, or you got it from counsel. 15 A. Oh, I was trying to answer that 16 question. Certainly, the primary prior art references 17 I got from counsel. 18 Q. And just so we're all on the same page, 19 none of the information that's in this declaration is 20 confidential; is that right? This is all publicly 21 available information, to your understanding? 22 A. Well, I'm not sure. I mean, that would 23 be my inclination to say so. I know that sometimes 24 when there are chips involved, I'm not the one who 25 makes that call. I mean, so for example, scrolling

Page 10 1 down, and I don't think this is confidential, but 2 scrolling down, on page 70 at the top, there's a 3 cross-section of a chip from a Realtek exhibit, and I 4 assume that that's not confidential. That was in a 5 complaint. But I can't really make that call. 6 Q. So, you're referring to page 70 of your 7 '582 declaration; is that right? The black-and-white 8 image in paragraph 121? 9 A. Yes. I'm just saying that to the 10 extent I have something like that in my report, I 11 don't think it's confidential, it shouldn't be 12 confidential, but I wouldn't know for sure. 13 Q. And so, if you go a couple more pages 14 to page 74, we see some additional pictures that are 15 also from a document from the ITC. Do you see that? 16 A. Yes. 17 Q. Do you have any idea whether those are 18 confidential? 19 MR. LIU: Objection, foundation. 20 THE WITNESS: Again, that's something 21 that I wouldn't know. I'd have to get that 22 information from the attorneys that I work 23 with. 24 BY MR. HALVERSON: 25 Q. But you'd agree that the '582 patent,	Page 12 1 providing design examples and questions on exams 2 involving those things. The class also had a 3 laboratory that involved LC circuits. So, I was part 4 of designing the laboratory and the experiments there. 5 And also, I may be redundant from what I said in the 6 earlier deposition, but I will, for completeness. I 7 have a research laboratory that's experimental, and 8 it's very deeply experimental, we're building things 9 all the time, primarily involving photonics, but also 10 involving electronics, and many times there's circuits 11 involved, LC circuits. 12 Q. So, in those circuits in your labs, are 13 you fabricating new LC circuits or are you 14 implementing existing LC circuits? 15 A. Typically, that would be -- well, I 16 guess I'd have to make sure I understand your 17 question, but I'll try to answer. The subject of our 18 research is not coming up with a new form of VCO. The 19 subject of our research would be using LC circuits as 20 part of a filter, for example, or as part of some sort 21 of a controlled circuit. So, we would be, typically, 22 taking them from an existing library, typically, in 23 order to make the LC circuit. As I mentioned earlier, 24 in some cases I know of recently, we've needed to use 25 LC circuits for impedance matching, so maybe you would
Page 11 1 in general, is about an LC circuit, right? 2 A. Yes. 3 Q. So we're all on the same page about our 4 nomenclature there, the L represents an inductor, 5 right? 6 A. Right. 7 Q. The C represents a capacitor, right? 8 A. Yes. 9 Q. Which sometimes can be referred to as 10 an LC tank; is that correct? 11 A. That's correct. 12 Q. And is that also something that can be 13 referred to as a VCO? 14 A. The LC tank would, presumably, be part 15 of the VCO. 16 Q. And is that to say that there are more 17 components in a VCO than in an LC tank? 18 A. I would say so, yes. 19 Q. Did you ever design an LC circuit, Dr. 20 Prucnal? 21 A. Well, you know, my experience goes back 22 so far that it's hard for me to recall all the things 23 I've done. Again, I would say that I taught circuits 24 for many years, and certainly, LC tanks were part of 25 that instruction, part of the teaching involved	Page 13 1 consider that designing a new LC circuit. I probably 2 wouldn't consider putting an LC circuit onto a chip 3 that we're making designing new LC circuits. 4 Q. So, in that answer you mentioned a 5 library, specifically taking them, the LC circuit, 6 from an existing library. When you are talking about 7 what your understanding of your design work on LC 8 circuits is, are you referring to physical circuits in 9 the context of that library, or are you referring to 10 electronic designs and electronic models more on the 11 lines of, like, a P-cell? 12 A. More along the lines of a P-cell. 13 Q. And just so we're all on the same page, 14 what is a P-cell? 15 A. Well, that's just an existing sort of 16 package or unit that you can just lift out and plug in 17 and use. 18 Q. And would that P-cell be the full LC 19 circuit in that it includes both an inductor and a 20 capacitor? 21 A. That, I can't recall, exactly. And 22 usually, it's my graduate students that actually have 23 the hands-on in this kind of stuff. So, I know the 24 outcome, I know the goals, but they're the hands-on 25 putting the things together. So, I don't know if it

Page 14 1 was an LC and a P-cell, or just a capacitor. I don't 2 know for sure. I know there are -- 3 Q. And the outcome -- I apologize. 4 A. I paused to think, but I just wanted to 5 sort of repeat that I know there are examples where 6 we've put Ls and Cs that are individually designed 7 onto a circuit. So, I'm speaking of a photonic 8 integrated circuit, where some electronics are 9 required on the circuit in order to control it. And 10 for example, doing impedance matching, as I mentioned 11 before, that's not a P-cell. That's a designed 12 inductor. 13 Q. And where does your lab get those 14 libraries from? 15 A. That, I don't know either. They're 16 licensed by the university. The software that's used 17 to design is licensed by the university. Some of the 18 software used I know is open-source, but I don't know, 19 in particular, where this came from. 20 Q. And I know this morning you spent a 21 fair amount of time talking about Q, the Q-factors, so 22 forgive me if we reread just a little bit, but what 23 is a Q-factor in the context of an inductor? 24 A. It's a quality factor. 25 Q. What does that mean?	Page 16 1 Q. So, if you go to paragraph 55 that's on 2 page 24 of your '582 declaration, the third sentence 3 says, "The higher the Q-factor of the inductor, the 4 lower the energy loss of the device and the closer it 5 approaches the behavior of an ideal inductor." Do you 6 see that? 7 A. Yes. 8 Q. And so, is there an ascertainable Q 9 value of an ideal inductor, or does that turn into an 10 infinite number at that point? 11 A. Again, that's not something I 12 considered. My, sort of, reaction to that would be as 13 you decrease the energy loss, the Q gets higher and 14 higher, the frequency response gets narrower and 15 narrower, if you were to put that into a filter. So, 16 approaching the ideal means that the R in the 17 denominator goes to zero, effectively making omega L 18 over R infinity. 19 Q. So, the next paragraph in your 20 declaration you talk about, in general terms, 21 mechanisms to improve an inductor and its Q-factor. 22 Is it the case that a higher Q-factor is always an 23 improvement on the inductor? 24 A. I don't know that I would say always. 25 I don't know if I ever say always. But I think,
Page 15 1 A. So, the Q-factor is referring to, in 2 the context of an inductor, and I think I say this in 3 my report, it's a ratio of the energy stored to the 4 energy dissipated, or some words like that, probably 5 in the introduction of my report. So, it's really 6 meant to be a ratio of how much energy can be kept in 7 the inductor, which is a good thing, versus how much 8 energy is lost, which is a bad thing. And when I 9 think, for example, of an LC circuit, of a resonant 10 circuit, a Q is going to be a measure of its frequency 11 performance. I mean, the inductor has an impedance. 12 That's a function of omega or the frequency, as well. 13 But when I think of Q, usually I'm thinking of, like, 14 a tank circuit, and I want to know what the resonant 15 frequency is of that tank circuit, and how narrow a 16 spectrum of filtering it will do. And so, the Q ends 17 up telling me how narrow that frequency characteristic 18 is. 19 Q. So, what would be the Q-factor of an 20 ideal inductor? 21 A. Well, I hadn't thought about the 22 Q-factor of an ideal -- an ideal inductor wouldn't be, 23 I think, ideally dissipating any power. So, I think 24 of an ideal inductor as simply being represented by 25 its inductance.	Page 17 1 generally, a high Q is desirable in an inductor. All 2 of the loss mechanisms that are described there, the 3 conductive loss, the internally-induced loss, the skin 4 effect, which increases at higher frequencies, the 5 induced losses, those are undesirable effects. 6 Q. Is there a Q-factor of an LC circuit 7 separate and apart from the Q-factor of the L of that 8 LC circuit? 9 A. I believe so, yes. 10 Q. So, is there a Q-factor, then, of the 11 capacitor, or is that larger Q-factor of the LC 12 circuit just the way that the overall quality of the 13 LC circuit is analyzed? 14 A. I'd have to look back at that. I 15 somehow thought that the Q of an LC circuit goes as 16 the product of the L and C. I think I might have it 17 in my introduction somewhere. 18 Q. I'm going to shift gears a little bit. 19 Are you familiar with the term varactor? 20 A. Yes. 21 Q. What's a varactor? 22 A. It's a variable capacitor. 23 Q. And how does one vary the capacitance 24 of a varactor? 25 A. Well, that depends on the physical

Page 18 1 structure of the capacitor. So, historically, a 2 varactor -- so, a capacitor, a simple capacitor, is 3 two parallel plates, and one can vary the capacitance 4 by varying the overlap of the two plates, for example, 5 or the separation of the two plates. A typical 6 varactor might have, if you see my finger -- I don't 7 see myself on the screen, but if I were to take my two 8 hands, and my fingers were the plates of the 9 capacitor, and you could sort of role them into each 10 other or apart from each other, and you can vary the 11 overlap of the plates by doing that, that would be one 12 type of variable capacitor or varactor. 13 Q. Would that be kind of like how the 14 radio dial on an older vehicle may work? 15 A. Yes. When you turn the dial, you're 16 turning the LC. The C, in particular. 17 Q. Now, you also refer to a different kind 18 of capacitor in your declaration, a MOS capacitor, in 19 the context of a varactor. How do you tune the 20 capacitance of a MOS capacitor? 21 A. Well, so, the MOS capacitor, it's a 22 semiconductor device, and it's based upon having a 23 source, a gate, and a drain. And depending on the 24 particular design, the voltage, for example, I think 25 in Gonzalez the voltage is varied on the source of the	Page 20 1 A. Okay. I'm missing a little bit of what 2 you're saying. Before we were talking about the 3 physical plates interacting and moving them to change 4 the capacities. 5 Q. Yes. 6 A. And then I mentioned the MOS varactor 7 in Gonzalez, which has connections to the source, 8 drain and gate. So, which electrode are you referring 9 to that we spoke about before? 10 Q. So, in the tunability, when we were 11 talking about the radio example, where you've got two 12 metal electrodes that you are varying the amount of 13 interaction between those two electrodes in order to 14 change the capacitance, you would agree that the two 15 different pieces that are movable are electrodes; is 16 that right? 17 A. Well, it's a matter of terminology. I 18 would typically refer to them as plates, because we're 19 talking about the fundamental parallel plate capacitor 20 with the overlap of the plates being varied between 21 the two, except that this is repeated over and over 22 again in that old radio style movable capacitor. So, 23 I would just call them plates, usually. 24 Q. Okay. In the context of capacitors, in 25 general, have you ever used the term electrode to
Page 19 1 MOS varactor. And in doing so, one can alter the 2 build-up of charge in the relevant region where the 3 capacitance is occurring. So, applying the voltage to 4 that will achieve the tuning of the capacitance. 5 Q. So, let's go to paragraph 75 of your 6 declaration, on page 34. 7 A. Yes. 8 Q. Here, you're introducing the concept of 9 a MOS, Metal Oxide Semiconductor, capacitor, right? 10 A. Yes. 11 Q. So, looking at the figure down at the 12 bottom of paragraph 75, is there an electrode in that 13 figure? 14 MR. LIU: Objection, form. 15 THE WITNESS: So, are you speaking of 16 electrode in the context of the capacitor 17 above that, the finger capacitor? 18 BY MR. HALVERSON: 19 Q. Yes. So, so far we've been talking 20 about varactors in the context of having two metal 21 plates that you can vary the capacitance of the 22 varactor by moving them, and in this MOS varactor 23 there is no moveability. So, I'm wondering if there 24 is an electrode in the same way that we were thinking 25 about the electrode before.	Page 21 1 describe anything? 2 A. Well, the interdigitated finger 3 capacitors, as a class, I think I would refer to the 4 fingers as electrodes. 5 Q. How about in any other kind of 6 capacitor? 7 MR. LIU: Objection, form. 8 THE WITNESS: We have, I mean, I'm 9 thinking about Gonzalez, which I know we're 10 going to discuss, Gonzalez has sort of a 11 combination of interdigitated finger 12 structure, which are electrodes, together with 13 the MOS varactor, the back-to-back MOS 14 varactor. So, that whole structure has 15 electrodes as part of the capacitor component. 16 BY MR. HALVERSON: 17 Q. And so, we'll get to Gonzalez in a 18 second, but right now I'm just wondering about 19 situations beyond interdigitated capacitors where you 20 would refer to a portion of a capacitor as being an 21 electrode. So, you identified the finger components 22 of the finger capacitor. Is there any other situation 23 or any other type of capacitor that you would consider 24 it as an electrode? 25 A. I don't think I've considered that, and

Page 22 1 I don't think of anything off the top of my head. 2 Q. So, looking at the MOS capacitor in 3 paragraph 75, you wouldn't consider any of those 4 components to be electrodes? 5 MR. LIU: Objection, form. 6 THE WITNESS: As I said, we have the 7 source, the gate, and the drain, which would 8 have connections to them, metal connections to 9 them. At this moment, I don't know whether I 10 would refer to those as electrodes or not, but 11 there are terminations that are metal 12 terminations coming down to these three 13 regions. 14 BY MR. HALVERSON: 15 Q. So, in this MOS capacitor in paragraph 16 75, between which two points or which two components 17 is there a capacitance? 18 A. Well, you can have a capacitance 19 between the source and the gate, as I mentioned 20 earlier. 21 Q. And so, in this figure, in paragraph 22 75, the source would be the P well that's labeled with 23 an S; is that right? 24 A. I'm going to enlarge that. Yes, the P 25 well that's labeled source, that's right. It's P+,	Page 24 1 is going to be governed by their design rules of what 2 they will fabricate. 3 Q. And so, you have to adhere to that 4 foundry's design rules for the product that you are 5 designing, or you have to at least stay within those 6 design rules when you're making a product; is that 7 right? 8 A. Yes. That's a general statement, but 9 yes, in general. 10 Q. So, in Gonzalez, how many metal layers 11 do the design rules allow for? 12 A. I don't think I know the answer to that 13 without looking. 14 Q. It's not a memory test, so by all 15 means, take a peak. I'm happy to direct you to page 16 8. 17 A. That will speed things up. 18 Q. Left-hand column of page 8, about 19 halfway through that first paragraph. 20 A. Yes, I recognize that. 21 Q. So, now that we're there, how many 22 metal layers do the design rules of Gonzalez allow 23 for? 24 MR. LIU: Objection, form. 25 THE WITNESS: Well, Gonzalez says that
Page 23 1 yes. 2 Q. And it's just labeled S; is that right? 3 A. Labeled S, yes. 4 Q. And then the gate is the metallic 5 structure that sits atop that area and is labeled G; 6 is that right? 7 A. That's right. 8 Q. So, you've mentioned Gonzalez a couple 9 times. You're welcome to pull it up, if you'd like. 10 It's been added to the Exhibit Share folder as Exhibit 11 582-1005. 12 (Exhibit 582-1005 was introduced.) 13 BY MR. HALVERSON: 14 Q. In general, are you familiar with the 15 concept of a design rule, or design rules, when 16 designing circuits? 17 A. Yes. 18 Q. What are they? 19 A. Well, when designing an IC, design 20 rules are rules about the configuration and the 21 layout. Design rules could dictate the width and 22 thickness of metal lines, for example. Design rules 23 could limit the minimum spacing between metal lines. 24 These design rules are usually provided by the 25 foundry, so what you make when you lay out a circuit	Page 25 1 he is using the metallization M1 through M6 2 layers. 3 BY MR. HALVERSON: 4 Q. And then he goes on to say that the top 5 metal layer is M6; is that right? The sentence that 6 begins Figure 9. 7 A. Yes, that's correct. 8 Q. And he also refers to -- and I 9 apologize, I just said "he" twice. And so, if you 10 continue in that sentence, he also describes the 11 bottom two metal layers as M1 and M2; is that right? 12 A. Yes. 13 Q. So, the lowest-most metal layer of his 14 design rules is M1, and the top-most metal layer of 15 his design rules is M6; is that right? 16 A. Well, that's his design. Whether those 17 are design rules or not, I'm not sure. I didn't think 18 of it that way. But those are the metal layers he's 19 dealing with, that he's using. 20 Q. And not just the metal layers he's 21 using, but those are the design rules that he's 22 constraining his analysis to; is that right? 23 A. My understanding is just that he is 24 doing a design, using six metal layers, the top one 25 M6, and the bottom two M1 and M2. So, those are the

Page 26 1 parameters of his design. 2 Q. So, if you go on to the next column of 3 the same page, about halfway through that full 4 paragraph there's a sentence that begins, "However." 5 Do you see that? 6 A. Yes. 7 Q. So, here, the author is saying that he 8 has to account for the design rules so that he can 9 keep a wide range of characteristic impedance, and 10 therefore, he has to make a certain decision about 11 what option exists for where to place his microstrip 12 conductor layer; is that right? 13 A. Let me have a look at that, please. 14 Yes, the context of this is that he wants to reduce 15 the resistance of the strip line, and because of that, 16 he uses metal layer M6, which typically is a thick 17 layer, and that would reduce the resistance. 18 Q. Can you go back a couple of pages to 19 page 6 of Gonzalez? I want to ask a couple questions 20 about Figure 5, please. 21 A. Okay. 22 Q. Figure 5 is a little small, so it may 23 be helpful to zoom in, but by all means, feel free to 24 review any portion of Gonzalez or your declaration, if 25 you think that would be helpful to answer these	Page 28 1 A. Thank you. So, I think that section 2 starts at page 6, right-hand column. You may have 3 found that already. And that indicates -- 4 Q. I actually want to go back to page 5, 5 in the left-hand column, and just before the first 6 paragraph break, the second to the last sentence that 7 begins, "The binary switched." 8 A. Yes. 9 Q. So, Gonzalez uses the same structure 10 for both types of varactors; is that right? 11 A. Yes, that's right. 12 Q. So, going back to Figure 5, this 13 varactor is a MOS varactor; is that right? 14 A. Yes. 15 Q. And so, everything below the horizontal 16 line in the right-hand side of Figure 5, so the P+ 17 well, the N well the N+ well, all of those sit in 18 silicon, right? 19 A. Yes. 20 Q. Those are all below the bottom metal 21 layer? 22 A. That's correct. 23 Q. So, on the right-hand side of Figure 5, 24 still, we see something called an N+ poly? Do you see 25 that between the left two columns? Really small. You
Page 27 1 questions. My understanding is your opinion is Figure 2 5 indicates the form of the varactors that Gonzalez is 3 using. Is that right? 4 A. That's right. 5 Q. And Gonzalez Figure 8, which is a 6 couple of pages later, describes two different kinds 7 of varactors, digitally-controlled differential 8 varactors and fine-tuning varactors. Is that right? 9 A. I'm just getting to page 8. Where did 10 you point to? 11 Q. Figure 8. It's actually on page 8, as 12 well. 13 A. Yes. So, Figure 8 has both the 14 fine-tuning varactors and digitally-controlled 15 differential varactors. 16 Q. And Gonzalez used the same varactor, 17 that back in Figure 5, for both types of varactors 18 depicted in Figure 8; is that right? 19 A. I've looked most closely at the 20 fine-tuning varactor, where this is used. I'd have to 21 look and see how he designed the coarse-tuning 22 varactor. I think it's the same design, but I don't 23 recall, exactly. 24 Q. Let me see if I can find that section 25 for you.	Page 29 1 may have to zoom in. 2 A. I'm zooming in. Yes, I see the N+ 3 poly, which is the gray square below the blue 4 rectangle. 5 Q. So, below the N+ poly, there's a Thick 6 GOX. Do you see that? 7 A. Yes. 8 Q. Is a thick GOX a metal layer? 9 A. No, that's a gate-oxide. So, it's an 10 oxide layer. It's an oxide. 11 Q. And the N+ poly, is that a metal layer? 12 A. That is a layer with metallic 13 characteristics, but not strictly metal. 14 Q. What do you mean by that? 15 A. I believe that's a heavily-doped region 16 that provides a good connection between the metal 17 above, which is, I guess in this picture, the light 18 blue region, at L+ and the gate-oxide. So, it's sort 19 of an intermediate layer. An intermediate region, I 20 guess I should say. 21 Q. And is that N+ poly, that light-gray 22 square between the Thick GOX and the Out+ of the same 23 material as the N+ well in the N well? 24 A. No, the N+ well is a doped region in 25 the semiconductor, in the silicon.

Page 30 1 Q. So, what is the difference between the 2 heavily-doped N+ poly and the N+ well? 3 A. They are there for different purposes. 4 So, the N+ doped regions are the source and drain of 5 the MOS, and the N+ poly is used just as an interface 6 from the metal to the gate-oxide below. I don't 7 recall exactly what material is used for the N+ poly, 8 but it's different than the semiconductor below. 9 Q. So, in this 2x2 differential varactor 10 at Figure 5, where is the capacitance created between? 11 A. The capacitance is created between VC 12 and Out+. So, it's created as you pass through the 13 source region into the gate region, there would be 14 capacitance between the two. The gate and source in 15 the semiconductor. 16 Q. So, which metal layer is VC created out 17 of? 18 A. So, VC is actually a via that comes 19 down from a layer that's above. I don't remember the 20 number of the layer. But VC, in the right-hand 21 diagram, VC, as you can see, extends upward from the 22 source. And that translates into the left-hand of the 23 two diagrams, which is looking at the top, down. 24 That, I believe, translates into the little x in the 25 box. Let's see if I've got this right. It's probably	Page 32 1 A. Yes. 2 Q. So, you said that the via brings the 3 Out+ voltage from that letter F, called an electrode, 4 down to the source VC voltage; is that right? 5 A. Yes. 6 Q. So, there is a different letter x 7 that's associated with the VC voltage in Figure 5, 8 right? In each of the 2x2 varactors in the left-hand 9 image here, we see the Out+ via in the top left 10 corner, we see an Out- via in the bottom right corner, 11 and we see three x's off of the shaded VC Figure 8 12 that sits between the Out+ via and the Out- via. You 13 see those three x's? 14 A. So, either I misspoke or I agreed with 15 something that maybe wasn't what I intended to say. 16 It's not the VC that extends up to the Out+. I 17 misspoke there. Entirely misspoke. Because clearly, 18 it's the Out+ that extends to the Out+. And so, 19 everything I said is correct, except that I identified 20 the wrong blue pillar, the wrong blue via. And just 21 to correct what I said, if I may, the Out+ that's over 22 the gate, that blue via is what extends upward to the 23 letter F that's carrying the Out+ voltage. And there 24 are four of those connections. And as you correctly 25 pointed out, the other three x's are not on that
Page 31 1 easier to see in the diagram in my report, but I can 2 just pick one of them. You see on the left-hand side, 3 2x2 differential varactor, and it's labeled Out+ on 4 the left? 5 Q. Yes. 6 A. That Out+ is a conductor at a higher 7 layer, it's actually an electrode, and it's not shaded 8 in there, right? So, if you trace -- if your eye 9 follows that Out+ to the extent of it, you can see it 10 sort of looks like an F, like the letter F upright. 11 And the top of that F extends from the word Out+ over 12 to the right, and there's two places where there are 13 little x's in a box. I believe, and this is hard to 14 visualize just looking at this, but those are the vias 15 that bring the Out+ voltage from that letter F, the 16 electrodes, down to the source VC voltage. So, you 17 asked me what layer it's in, and just to summarize, 18 it's a via, and the via goes up from the N+ region and 19 then interconnects to the top of that F, or indeed, 20 any of those vias from the F. I think there are four 21 of them there. 22 Q. So, you said that the vias off of the 23 Out+, those four x's, there's one in the top left 24 corner of each differential varactor in the 2x2 25 differential varactor, right?	Page 33 1 letter F layer of electrodes. They're actually on 2 something that looks like a shaded-gray number 8, if 3 you can see that. And that carries the VC, as it's 4 labeled at the bottom of that particular figure. 5 Right? And then there are four groups of three x's 6 that would carry the voltage VC down to the source, to 7 the N+ source on the right side. 8 Q. And so, looking at the left side of 9 Figure 5, let's just isolate the top left differential 10 varactor, so we're all talking about the same portion 11 of this figure. Is that fair? 12 A. It's a little hard for me to make the 13 correspondence between the orientation of the varactor 14 on the right figure and on the left figure. I can 15 identify where the vias go down from the top, by 16 looking at the top, and I know Out+ goes down to the 17 gate, and I know that the nearest x, which is VC, 18 would go down to the source. It's a little hard for 19 me to visualize where the -- I see. The Out- is on 20 the other side. Okay? So, it looks like, if I may 21 continue, which I'm just trying to tell you what I 22 think I see, if we're looking at an individual 23 varactor, there's an Out+ in the top left of the 24 figure, and then there's an Out- that's sort of 25 diagonally below and to the right, which is carried by

Page 34 1 the inverted letter F. And in between those two are 2 three vias for VC, but those can't all be seen in the 3 figure on the right. 4 Q. So, is it fair to say that the figure 5 on the right is like a flattened cross-section, not an 6 actual cross-section, because in the figure on the 7 left, the Out+ via and the Out- via and the VC via are 8 not in the same plane? 9 A. Well, I don't have the entire physical 10 structure of the MOS here, but I interpreted this as 11 being sort of a diagonal cross-section. So, I'm 12 looking up at a screen rather than you. I apologize. 13 Q. That's okay. 14 A. But I took the cross-section, to make 15 sense, the cross-section would be a diagonal line, in 16 the same region we're talking about, from the Out+ on 17 the upper left, extending diagonally through, sort of, 18 the middle of the three VC connections, the VC vias, 19 and ending, maybe not necessarily ending, but 20 extending to the lower right Out- connection. 21 Q. And so, if we assume that type of a 22 slice for our cross-section on the right, where do we 23 find the subs, the two outer-most vias that go into 24 the P-wells in the figure on the left? 25 A. Okay. So, the subs in the top-down	Page 36 1 represented here, which is the 8, overlaps, looking 2 from top, down, overlaps Out+ and Out-, and therefore, 3 should be on a different metal layer. 4 Q. And you would agree that the right 5 side, the cross-section of one island portion of 6 Figure 5 of Gonzalez, does not show a finger electrode 7 in the context that we were using that term earlier 8 with the radio example, right? 9 MR. LIU: Objection, form. 10 THE WITNESS: Well, I would not choose 11 to use it in the context of the radio 12 electrode. I would say I would use it in the 13 context of an interdigitated finger, in a 14 finger capacitor, and in that case, the letter 15 F on the top, in fact, you know, where those 16 two letter Fs come together, inverted and not 17 inverted, would represent the fingers, and 18 they're connected downward through vias to the 19 Out+ and Out-. So, that's how -- 20 BY MR. HALVERSON: 21 Q. No, I'm talking about the right side, 22 the cross-section, which is the vias, but it doesn't 23 show the F's. 24 A. That's right. That's because, as I 25 just said, the vias come up to a higher layer, where
Page 35 1 view are the cross-hatched, sort of, rectangular 2 grade, I would say. It has vertical lines in it. It 3 has horizontal lines. And some of them are connected 4 with vias downward. I'm not sure that this is showing 5 all of them, but I took that as being the via that 6 goes down to the P+. 7 Q. And so, Out+ and Out- and VC in the 8 figure on the left cannot all be on the same metal 9 layer; is that right? There would be a short? 10 A. Well, we don't want shorts, okay, and 11 so the way this is laid out, the electrodes that 12 interconnect to L+, for example, are represented by, 13 if you wish, the letter F. And that can be on the 14 layer, I think it was the yellow layer in the other 15 figure, whichever figure that was, Figure 8. And the 16 Out-, where those come together, are interdigitated. 17 So, I'd have to look back at the other figure, I think 18 it's Figure 8, but I believe that the Out+ and Out- 19 electrodes, at that point, can be on the same metal 20 layer, which I believe was yellow. On the other hand, 21 did you say the VC? 22 Q. Yes, the third one that couldn't be on 23 the same layer, or you couldn't have all three, was 24 VC, in this outline, right? 25 A. Exactly. Exactly. So, the VC, as it's	Page 37 1 they are connected to the electrodes of the finger 2 capacitor. 3 Q. And so, in your interpretation of the 4 electrodes of the finger capacitors of the two F's, 5 what role do the vias and the remaining components in 6 the right side of Figure 5 play in the capacitance? 7 A. Okay. In the figure on the right-hand 8 side, the electrodes are not playing a role in the 9 capacitance. They're not shown there. It's the 10 source gate interface that is causing the capacitance 11 of the MOS, of this part of the MOS varactor. 12 Q. And so, in your experience with circuit 13 design, would you have a metal layer below a silicon 14 layer? 15 A. I don't have experience with that. I 16 don't know. I know that at some place there may be a 17 ground plane, but I don't know where that would be. 18 Q. And so, instead of doing this in the 19 abstract, let's do this in the context of Gonzalez, 20 which defines its ground plane as levels M1 and M2. 21 Do you remember we were talking about that on page 8? 22 A. Yes. 23 Q. So, if levels M1 and M2 are the ground 24 plane, and you look at, for example, Figure 9, do you 25 see any metal layers below any silicon layers?

Page 38 1 A. Well, Figure 8 shows only the -- 2 Q. Sorry, I'm asking about Figure 9, which 3 shows the ground plane and the substrate and the top 4 metal layer 6. 5 A. I think that the silicon falls below M1 6 here. So, looking at Figure 9, the ground plane would 7 be two metal layers at the bottom, and then the three 8 metal layers that comprise the loop would be 6, 5, and 9 4. 10 Q. And so, when you say the three metal 11 layers that comprise the loop, you're referring to the 12 blue layer, the gold or brown layer, and then the 13 yellow layer that are part of the inductor in the top 14 part of Figure 8? 15 A. Actually, this is a little difficult to 16 see, but I believe -- it's hard to see the details, 17 because the figure is so small, but it appears as if 18 -- so, the patent says a layer of aluminum and two 19 layers of copper to form the loop, and it appears as 20 if what looks like the brown layer here is actually 21 two layers of brown. And we can sort of see that if 22 we look at where the brown layer continues into Figure 23 8. There's a very fine line that's hard to see. It's 24 best seen by looking at the end of the brown 25 connection at the bottom.	Page 40 1 layer, because copper doesn't always do well sitting 2 on top of the oxide, on top of the insulation layer. 3 So, it could be for adhesion of the copper to the 4 insulation layer, or it could be just as a barrier to 5 prevent, sort of, diffusion of the copper. I think 6 that may be something that's typically done in 7 fabricating copper layers. 8 Q. But as you look at the top of Figure 8, 9 it's your understanding that these three metal layers 10 are represented by two brown layers and one blue 11 layer, not one blue layer, one brown layer, and one 12 yellow layer? 13 A. Looking at this very closely, because 14 these are tiny, I've come to this conclusion. 15 Q. I'm sorry, when you say this 16 conclusion, what do you mean? 17 A. What I mean to say is looking at it in 18 the past, and not looking at it this carefully, it's 19 easy to assume that the three metal layers are the 20 three colors, blue, brown, and yellow, but I mean, my 21 conclusion is after looking at it more closely, that 22 the three metal layers are blue and two brown. 23 Q. Got it. You would agree that there is 24 a capacitance between any two pieces of conducting 25 material, right?
Page 39 1 Q. So, I'll get to the bottom part of 2 Figure 8 in just a second, but if you zoom in on the 3 top part of Figure 8, the inductor coil, just above 4 where it says Patterned Ground Shield, you would agree 5 that you see three different colors there, right? You 6 see a blue layer on top, a gold or a brown layer in 7 the middle, and then a yellow layer beneath that gold 8 or brown layer? 9 A. I agree, I see three different colors. 10 But what I'm saying is I think the brown -- it's very 11 tiny, but I think the brown may actually be two brown 12 layers, one on top of the other, representing two 13 copper layers. 14 Q. And so, that was going to be my 15 question. Is it your opinion, then, that those two 16 brown layers are two copper layers? 17 A. Yes, I think so. And I think there's 18 clearly a yellow layer below that, as well. 19 Q. So, given that Gonzalez explains its 20 conductor coil is made up of three metal layers, an 21 aluminum layer and two copper layers, what is the 22 yellow layer in the top portion of Figure 8 that 23 depicts the coil? 24 A. That's not explained in Gonzalez, to my 25 knowledge. This could be some kind of a barrier	Page 41 1 A. Yes, as long as they're in reasonable 2 proximity of some kind, there's going to be some 3 capacitance. 4 Q. So, two pieces of a paperclip would 5 have a capacitance between them? 6 A. Well, when you apply a voltage to two 7 pieces of metal, you end up with a capacitance between 8 them. 9 Q. And not just metal. There's a 10 capacitance between, for example, my two fingers? 11 A. I suppose there could be. I don't know 12 very much about that, but I think that's possible. 13 Q. Have you ever used a capacitive 14 touchscreen? 15 A. Yes. And I think that's how it works. 16 I'm just not too familiar with how it works, but -- 17 Q. So, that's what I was going to ask, is 18 there a capacitance there between your finger and then 19 the metallic layer somewhere within the stack of the 20 touchscreen? 21 A. That's correct. 22 Q. But you would not consider your finger 23 and that touchscreen to be a capacitor; is that right? 24 MR. LIU: Objection, form. 25 THE WITNESS: Well, it's not a

Page 42 1 capacitor that I would build into an 2 integrated circuit, but it has capacitance. 3 And if I wanted to model that system, if I 4 wanted to model that circuit, I might model 5 the aspect of the circuit that had the 6 touchscreen and the finger as being 7 represented by a capacitor. 8 BY MR. HALVERSON: 9 Q. I agree with that, but would you 10 consider a user's finger and a capacitor touchscreen 11 to be, collectively, a capacitor, as a professor? 12 MR. LIU: Objection, form. 13 THE WITNESS: So, not conventionally, I 14 wouldn't think of my finger as a capacitor, 15 but if I think of a capacitor as an element 16 that has capacitance, and in the context of 17 designing a touchscreen that uses that 18 capacitance that we talked about between the 19 screen and the finger, in that sense they're 20 behaving as a capacitor would. 21 BY MR. HALVERSON: 22 Q. So, I think there's two separate 23 concepts here. There's this idea of two components 24 that have a capacitance between them, and then there 25 is this idea of a capacitor. My question is do any	Page 44 1 stop, you could turn, you get yourself from point A to 2 point B, but you, on your bicycle, is not a car. 3 Nobody would ever consider that to be a car. Nobody 4 is denying that you on your bicycle could act like a 5 car, or behave like a car, or have some 6 characteristics akin to a car, but I don't think 7 anybody would consider an individual on a bicycle to 8 be a car. And so, I'm just curious as to whether or 9 not you would consider any two components that have a 10 capacitance to necessarily be a capacitor. 11 A. Well, I mean, the way you've put it, of 12 course a bicycle is not a car, and of course, an 13 electronic capacitor is not the interface between a 14 finger and a screen. So, they both have capacitance. 15 One I would call a capacitor. What else would you 16 need to make a capacitor? Probably, that the 17 capacitor would exist in some kind of a circuit, I 18 would say. 19 Q. Can you go to Figure 2 for me of 20 Gonzalez? It's on page 5, top left corner. 21 A. Okay. 22 Q. So, Figure 2 is a schematic diagram of 23 a VCO and output buffers; is that right? 24 A. Yes. 25 Q. So, we see the inductor as the
Page 43 1 two components that have a capacitance between them 2 necessarily create a capacitor, or is there something 3 else that goes into distinguishing a capacitor on the 4 one hand and my two fingers on the other hand? 5 A. Well, typically, a capacitor has a 6 dielectric between the two plates. So, there should 7 be an insulator between the two plates that keeps them 8 separated and allows the charge to build up on the two 9 plates. So, if I wanted to go further into what a 10 capacitor typically includes, there's some kind of a 11 gap, and then maybe the dielectric, or some kind of 12 insulator. 13 Q. Is that it? 14 A. Well, I mean, I think you're asking me, 15 broadly, would I say that anything that has the 16 capacitance to be a capacitor, and I typically think 17 of capacitors as electronic components. That's pretty 18 simple. But I also understand that other things that 19 may have capacitance could behave the way a capacitor 20 does, could be modeled as a capacitor. But would you 21 call it a capacitor? That's stretching it a bit. 22 Q. I agree. I was just curious. Because 23 for example, I can envision a situation where you 24 could be riding a bicycle, and you, on your bicycle, 25 could behave like a car, you could go fast, you could	Page 45 1 almost-octagon with an open bottom. 2 A. Yes. 3 Q. You chuckled there. Is there a better 4 way that you would describe that? 5 A. I feel like I've been talking about 6 octagons all day. 7 Q. I feel like I've listened to a lot of 8 octagon discussions. So, the almost-octagon there 9 that is the inductor, and then below that we see an 10 arrow, a dotted-line arrow, that identifies, 11 "Continuous tuning analog control varactor 5x5 12 islands." Do you see that? 13 A. Yes. 14 Q. And then below that we see another 15 arrow, and if we follow that bottom arrow up to the 16 top and the right, we see, "Digital control varactor 17 bank 7 units 1x1." Do you see that? 18 A. Yes. 19 Q. And so, the continuous tuning 20 varactors, the figure says see Figure 3, right? 21 A. Yes. 22 Q. And the digital control varactor bank, 23 the figure says see Figure 3 and 5, right? 24 A. Right. 25 Q. So, how far is the continuous tuning

Page 46 1 varactor of Figure 2 from the leads of the inductor of 2 Figure 2? Can you tell? 3 A. Well, I can't tell, because this is 4 sort of a hybrid schematic that sort of shows, maybe, 5 a physical octagonal representation of the inductor 6 loop. That octagon might not be the way you typically 7 represent an inductor as a coil, as a circuit element. 8 And below that are circuit elements representing the 9 varactors. So, once it becomes a circuit diagram, you 10 know, the distances, it's more making the electrical 11 connections clear, and I can't tell from the circuit 12 diagram how far things are apart. 13 Q. Instead, you would need something like 14 an image, or a PCB schematic, or some other form of 15 figure to be able to see how they're actually 16 oriented? 17 A. That might help. The right image might 18 help, and the PCB could help, if you showed where the 19 components are. 20 Q. And so, a schematic such as Figure 2 21 would look the same whether or not two components were 22 a millimeter apart or three millimeters apart? 23 A. Well, yes, but I would add that this 24 schematic, as I said, is sort of a hybrid, where it 25 seems to be showing, to some extent, where things are	Page 48 1 A. I'm there. 2 Q. Before we dive into this, I'm sorry, I 3 haven't been keeping track of time. Do you need a 4 break, or are you fine to keep going? 5 A. I'm fine to keep going. 6 MR. HALVERSON: Charles, are you okay 7 to keep going? 8 MR. LIU: Can I ask for a 5-minute 9 break, maybe? 10 MR. HALVERSON: That's fine. We're 11 over an hour now, so I'm happy to take a 12 break. Does five minutes work? 13 MR. LIU: It's 4:42 right now. How 14 about we just round it to 4:50, and we come at 15 4:50? 16 MR. HALVERSON: Eight minutes. Sounds 17 good. 18 (A 7-minute recess was taken.) 19 BY MR. HALVERSON: 20 Q. So, we're at Figure 12 of Gonzalez, and 21 Figure 12 is a die micrograph, right? 22 A. Yes. 23 Q. What's a die micrograph? 24 A. Well, the die is a chip, and a 25 micrograph is an image of the chip, some kind of
Page 47 1 located, you know, so that somehow the varactor is 2 located below the octagonal loop. And the digital 3 control varactor is below that, and then the 4 oscillator below that, and the two buffers up on the 5 side. I think there's some correspondence in the 6 general layout of where these things are positioned 7 and located, but you can't tell distances. And you 8 can't even tell exact locations. 9 Q. Can you point out where in Figure 2 you 10 see finger electrodes, if anywhere? 11 MR. LIU: Objection, form. 12 THE WITNESS: Figure 2 doesn't indicate 13 where the finger electrodes are. It points to 14 a continuous tuning analog varactor. And to 15 understand what that is, one has to look at 16 another figure to see what's in that varactor. 17 By the way, that's where the fingers are. 18 BY MR. HALVERSON: 19 Q. But you can't see them in Figure 2? 20 You've got to go look at the other figures? 21 A. Yes, I have to go look at more of the 22 detail of what's in that dashed box. 23 Q. Can you go down a few pages to page 9, 24 and look at figure 12, please. Let me know when 25 you're there.	Page 49 1 photograph of the chip. 2 Q. But it's a photograph taken of an 3 actual physical thing, not a model for representation 4 of what the physical thing should look like? 5 A. That's my understanding, but this is a 6 photograph, top, down, of the surface of a chip. 7 Q. So, looking at Figure 12, and just 8 Figure 12, can you tell me where the fingers of the 9 capacitors are? 10 A. I'm blowing it up. So, we see the 11 octagonal loop sort of just below dead center. It has 12 a box around it, and it's labeled as VCO core. And 13 then we see the buffers labeled on the side. 14 Q. And can you tell what those buffers, 15 the form of those buffers take? 16 A. I can't tell from looking at this. 17 Q. Can you see a capacitor in those 18 buffers? 19 A. No, I can't. 20 Q. Can you see a resistor or -- I'm sorry. 21 Go ahead. 22 A. No, I was just going to say that I 23 don't see the details of the components here. And 24 just pointing out where the VCO core is, that the 25 finger capacitor and the varactor would be within the

Page 50 1 VCO core, within that box, but at a lower layer. 2 Q. Why are they at a lower layer? 3 A. Well, the design is such that some of 4 the components are located below the extension 5 segments of that inductor, and so you know, when we 6 look at the design that Gonzalez shows, we can see 7 that they're located under that. 8 Q. All right. Let's go back a couple of 9 pages to page 8, and talk about Figure 8, and you've 10 been very excited to talk about Figure 8, so let's do 11 it. 12 A. Okay. I've got it. 13 Q. So, starting with the bottom part of 14 Figure 8 -- I guess to orient ourselves before we do 15 that, Figure 8 has two halves to it. Is that a fair 16 statement? The top half and the bottom half? 17 A. Yes. 18 Q. So, the top half depicts an inductor 19 layout; is that right? 20 A. That's right. 21 Q. And the bottom half depicts the 22 interconnection of varactors and the structure of 23 transistors; is that right? 24 A. Yes. 25 Q. Where do you see a transistor in the	Page 52 1 right? 2 A. Yes. 3 Q. Is it your understanding that those 4 colored layers represent different metal layers? 5 A. Yes. 6 Q. So, earlier you had pointed to the thin 7 line between the two gold or brown layers. So, does 8 that mean that there are two metal layers that 9 comprise that, or one metal layer that comprises that 10 Out- or Out+ paddle? 11 A. I believe there are two metal layers 12 there, and that's on the basis of relating it to the 13 top half of Figure 8, which is described as having two 14 copper layers, as we discussed before. 15 Q. And so, are those two metal layers 16 directly on top of each other without any interstitial 17 insulating material? 18 A. No, they should be separated by an 19 insulator. 20 Q. That's interesting. How are they 21 connected, then? 22 A. This doesn't show how they're 23 connected, but presumably, by some kind of vias. 24 Q. And then how do you know that they are 25 not one on top of each other?
Page 51 1 bottom half of Figure 8? 2 A. I don't see the transistor itself, but 3 I see the interconnections to the transistors. So, 4 for example, MN1 and MN2, I believe, are two 5 transistors. In Figure 2, MN1 and MN2 are two 6 transistors, as I said. And those transistors -- 7 Q. And so -- 8 A. I'm sorry. 9 Q. You like to give pensive thought to 10 your answers, and I like to jump on in, so I 11 apologize. You go ahead. What were you going to say? 12 A. I was just going to say you asked me 13 where the transistors are shown, and the transistors 14 are going to be below what you see here, because 15 they're in the semiconductor. 16 Q. So, you can't actually see the 17 structure of any transistors in the bottom half of 18 Figure 8; is that fair? 19 MR. LIU: Objection, form. 20 THE WITNESS: Well, not exactly. I 21 mean, it's showing the interconnections to the 22 transistors. It's pointing to them. 23 BY MR. HALVERSON: 24 Q. So, the bottom half of Figure 8 25 includes a number of different-colored layers; is that	Page 53 1 A. Because of the conventional way that 2 ICs are fabricated with metal layers separated by 3 insulators. 4 Q. Could you ever fabricate two metal 5 layers, one on top of the other, without any 6 interstitial insulating material? 7 A. Well, I suppose it would be possible, 8 but you might run into problems doing that. So, for 9 example, thermal expansion coefficient of the metal 10 would be slightly different, and that would lead to 11 stress. I think there are a number of reasons why, in 12 practice, one does not want to put metal on top of 13 metal, but I think -- 14 Q. Other than thermal expansion 15 coefficient, why else would you not want to put metal 16 on metal? 17 A. There might be issues with adhesion. 18 I'm not sure of all the reasons, but adhesion could be 19 one. Thermal could be the other. 20 Q. And if you were depositing two metal 21 layers that had the same composition, they would have 22 the same thermal expansion coefficient, right? 23 A. Presumably, they'd be the same. 24 Q. That would be the goal? 25 A. Well, I don't know that that would be a

Page 54 1 goal, but if you had copper on copper, for example, it 2 should expand and contract at the same rate. But 3 nevertheless, I know that it's frowned on, putting 4 metal on metal. 5 Q. So, we've got two brown-ish, 6 gold-ish -- what color would you use for that, the 7 Out+ paddle? 8 A. I think I'm very bad with colors, 9 because I've been told that the layer under that is 10 yellow, and it looks greenish to me, but everyone 11 agrees that it's yellow. So, I'm going to say that it 12 looks like the extension segments are brown. 13 Q. So, we've got two brown layers. And 14 then are you zoomed in on this bottom part of Figure 15 8? 16 A. No, but I will. 17 Q. Please do, because I'm going to ask 18 about pink and red and green, and they're pretty 19 small. 20 A. Okay. I'm zoomed in. 21 Q. So, we've got, below the two brown 22 layers, we've got a yellow layer; is that right, the 23 one that you called greenish? 24 A. Yes. 25 Q. And so, below that, we have a pink	Page 56 1 spot, I think, to see this continued descent, is going 2 to be at the digitally-controlled differential 3 varactor, but below that teal, light blue color, we 4 see a dark blue layer; is that right? 5 A. Yes. 6 Q. And then below that, we see a white 7 square, right? 8 A. With white under it. 9 Q. And that's my ultimate question, is it 10 your understanding that that white there is a layer, a 11 boundary, or just an absence of color, based on there 12 not being something there? 13 A. To me, and again, this isn't described 14 in the paper, so I'm inferring by looking at this that 15 it's just an absence of color. If you're referring to 16 the white that is at the boundaries of the light blue 17 or teal, and extending under the dark blue, I think 18 that's unspecified. It's not another metal layer. 19 Q. And then looking in the middle, you see 20 the arrow that says, "Fine Tuning Varactor?" Do you 21 see that? 22 A. Yes. 23 Q. And there's a black arrow pointing 24 generally towards the middle of the image, right? 25 A. Well, it's sort of touching that
Page 55 1 layer; is that right? And for orientation, I think 2 the easiest spot to see this is either in those MN 3 areas, at the very bottom of that MN comb, or at the 4 bottom part of the brown cables in the middle, those 5 legs that go down. 6 A. I see pink. I do see pink under there, 7 yes. 8 Q. And below that, do you see, kind of, a 9 neon green? And the neon green is pretty small, just 10 a little square across the bottom there. It's a 11 little bit more pronounced in the MN1 and MN2 areas. 12 A. I can barely see it. I can't say that 13 I'm certain in the MN1 and MN2 areas. I do see the 14 pink, but it looks to me like there's light blue under 15 the pink. I don't know for sure with the green. 16 Q. I definitely see the light blue, and we 17 see that light blue has, kind of, a collar around the 18 full bottom half of Figure 8; is that right, kind of a 19 teal-light blue? 20 A. Yes. 21 Q. And is it your understanding that that 22 is also a metal layer? 23 A. It's not described in the paper, in 24 Gonzalez, but that's my understanding. 25 Q. And so, below that, in the easiest	Page 57 1 electrode. 2 Q. That was my question. Is it your 3 opinion that that fine tuning varactor arrow is 4 pointing to the yellow electrode, or pointing to 5 something below the yellow electrode? 6 MR. LIU: Objection, form. 7 THE WITNESS: I think it could be 8 either. I mean, it could be taken as 9 generally pointing to the middle of that 10 region, but also pointing to the yellow 11 electrode. 12 BY MR. HALVERSON: 13 Q. Do you see any pink or teal or light 14 blue in the area where the fine tuning varactor arrow 15 is pointing? 16 A. No. It seems to start at the yellow 17 layer with the fingers, and then there is nothing in 18 that middle region until we get to the blue layer 19 underneath. There's nothing else intervening in that 20 region. 21 Q. So, can you tell me, looking at the 22 bottom part of Figure 8, how the Out- paddle -- do you 23 see that, in the top left part of the bottom part of 24 Figure 8? 25 A. Yes.

Page 58 1 Q. -- how the Out- paddle is connected to 2 the yellow layer beneath the Out- paddle? 3 A. Well, these are two different metal 4 layers, which would have an insulator between them, 5 and the insulator would have vias through them 6 connecting the brown extension segment and what you 7 called the paddle underneath it. The Out- voltage 8 from the extension segment, therefore, is being 9 carried by the paddle, as you would say. But that 10 paddle, that yellowish layer, also extends, appears to 11 extend, down the length of that paddle to the end, 12 because we can see in cross-section that below the 13 lower brown layer is a yellow layer. And in doing so, 14 it's connecting to MN2, as well, those sort of little 15 finger connections that come out from under the paddle 16 to the right. So, that's how I think the yellow layer 17 connects to the brown paddle. 18 Q. Can you tell me how many vias there are 19 between the Out- paddle and the yellow layer? 20 A. I don't know. 21 Q. Can you tell me whether the yellow 22 metal layer is a continuous metal layer? 23 A. Whatever is going on under that brown 24 extension segment isn't shown, so I don't know what 25 the shape of it is. What I can say is that it extends	Page 60 1 Q. What do the blue lines do? 2 A. These blue lines are carrying Vc to the 3 sources of the MOS varactors. 4 Q. How do you know that? 5 A. Well, I'd have to look at a different 6 figure, the one that shows the cross-section. 7 Q. Is that Figure 2 or Figure 5, or 8 something else? 9 A. No, Figure 5. 10 Q. Let's go back to Figure 5. Now, we're 11 looking at, I assume, the left-hand portion of Figure 12 5? 13 A. Yes. So, we already know that, I think 14 we already know, that Out+ and Out- come from those 15 F-shaped fingers, we already discussed that, on the 16 left-hand side. And then we have the thing that looks 17 like an 8, that's grayish, which has Vc going to it, 18 and that's providing the Vc to a source. So, this, in 19 my opinion, corresponds to the blue lines, the dark 20 blue lines, that we just discussed. I would call it 21 -- 22 Q. So, looking at this figure, Figure 5, 23 you would agree that Vc, the gray Figure 8, is above 24 Out+, right? It obscures the Out+ portions of the F? 25 A. Well, I think it's not entirely drawn
Page 59 1 underneath, and I know that because I know that we 2 need the Out- voltage being carried by that. And I 3 also believe that makes a left-hand -- a right angle 4 to the left, and goes down and interconnects to MN2, 5 to provide the Out- voltage to MN2, as well. The 6 detailed shape of that isn't shown, and I don't know. 7 Q. Now, the '582 patent refers to 8 something as a first region. Are you familiar with 9 that concept? 10 A. Yes. 11 Q. I believe in your declaration you've 12 got a red dotted line in an annotated version of the 13 bottom part of Figure 8 that outlines the first 14 region, and I'm happy to find that for you, but I want 15 to ask my question first and see if we need it or not. 16 Do you agree that the digitally-controlled 17 differential varactors, the seven across the bottom, 18 are not underneath the first region that you've 19 identified? 20 A. As far as I can tell, they are not. 21 Q. The blue lines that are in the center 22 portion of the bottom part of Figure 8, they've got 23 stubs that stick off. Do you see those stubs? Do you 24 know what I'm talking about? 25 A. Yes.	Page 61 1 consistently. If you look at the inverted F on the 2 right-hand side, the, sort of, fingers of the F that 3 extend from the Out- vertical bar to the left, they 4 cross the Vc gray bar by going over it. 5 Q. And you can tell that because the black 6 outer-boundary of the Out+ F, or inverted F prongs are 7 over the top of the gray Figure 8 VCC, right? 8 A. I'm inferring a lot into this by saying 9 that, but here, just from this drawing, it looks like 10 the minus fingers are above the Vc gray bar. Now, on 11 the other side, it's shown in a different way, I 12 believe, with the F that is right-side up. It looks 13 like the fingers of the F go under the gray Vc area. 14 So, to some extent, that may just be drawn poorly, but 15 when I combine that with Figure 8, I see that the blue 16 Vc connections are under the fingers. 17 Q. And there's no label in Figure 8 or 18 indication in Figure 8 of Vc; is that right? 19 A. No, Vc is not labeled in Figure 8. But 20 I do know from the circuit diagram what Vc needs to be 21 connected to, and it needs the fine tuning varactor to 22 tune it. 23 Q. Can you go to paragraph 144 of your 24 declaration for me, please? It's on page 86 of the 25 pdf.

Page 62 1 A. I'm clicking to the left to get there, 2 and it's taking a few minutes. 3 Q. Those files are also downloadable. I 4 don't know if you have Adobe on your desktop, but it's 5 a little bit easier to search and navigate if you get 6 a local a copy, but up to you. 7 A. Thank you. I want to play it safe 8 right now, if you don't mind. 9 Q. That's just fine. Take your time. 10 A. What paragraph did you say? I'm not 11 there. 12 Q. 144. 13 A. Okay. 14 Q. On paragraph 144, the second sentence 15 begins, "As illustrated." Do you see that? 16 A. I'm sorry, I pulled up the wrong 17 document. 18 Q. Were you clicking through your 245 19 declaration? 20 A. I was. How did you know? 21 Q. It's the only other really long 22 document. 23 A. I'm going back to the Marked Exhibits 24 now. It's going to be the safest way. I'm opening my 25 '582 declaration, and I'll scroll down to paragraph,	Page 64 1 MIM capacitor and a MOM capacitor, in your mind? 2 A. So, the MOM capacitor, the 3 metal-oxide-metal capacitor, I believe that 4 corresponds to the parallel plate capacitor. And the 5 MIM, or metal-insulator-metal capacitor, I understand 6 as a vertical parallel plate capacitor, a VPP 7 capacitor, which, for example, would be a capacitor 8 with the fingers stacked and connected by vias, 9 effectively forming parallel plates in a vertical 10 direction. 11 Q. All right. Can you go back to the 12 Exhibit Share folder, the Marked Exhibits? I've added 13 Muh. 14 A. I've got Muh. 15 MR. HALVERSON: For the record, Muh is 16 582-1006. 17 (Exhibit 582-1006 was introduced.) 18 BY MR. HALVERSON: 19 Q. Have you read Muh? 20 A. I've gone through the whole thing. 21 Q. Cover-to-cover? 22 A. Yes, very detailed in various places, 23 yes. 24 Q. And my read of your declaration is most 25 of what you focused on in Muh is in the appendix of
Page 63 1 did you say, 144? 2 Q. Paragraph 144, yes, page 86. 3 A. Okay. 4 Q. The second sentence, "As illustrated in 5 Figure 8," do you see that? 6 A. Yes. 7 Q. So, this sentence refers to a 8 fine-tuning capacitor and a fine-tuning varactor, and 9 I just want to make sure those are the same thing, in 10 your mind, right? 11 A. Is that figure in the neighborhood of 12 this? 13 Q. It's on the next page. 14 A. I wanted to see what the red box was 15 it's referring to. (Pause.) The answer is yes. 16 Q. All right. While I wait for something 17 to load, hang on one second. Bear with me for just a 18 second. So, we talked a little bit earlier about MOS 19 capacitors. We also talked about the concept of a 20 MIM, M-I-M, capacitor? 21 A. Yes. 22 Q. Are you also familiar with the concept 23 of a MOM, M-O-M, capacitor? 24 A. Yes. 25 Q. So, what is the difference between a	Page 65 1 Muh, not the body of Muh. Is that a fair 2 characterization? 3 A. That is correct. 4 Q. So, is it your understanding that the 5 appendix of Muh is describing testing that the student 6 performed on a chip that he was given? 7 A. Yes. 8 Q. And that is not the chip or the 9 analysis that was done in the rest of his thesis; is 10 that right? 11 A. He's using a different capacitor in the 12 rest of his thesis, doing an analysis of a VCO. 13 Q. And in fact, all he was doing with 14 what's in Appendix B was checking whether or not the 15 HFSS analysis that he was doing in the rest of his 16 thesis was, itself, accurate; is that right? 17 A. That was one of the goals of the 18 appendix. The other was to test the VCO with the 19 interdigitated capacitor. 20 Q. When you say the VCO, what are you 21 referring to? 22 A. Well, he compared to the inductor 23 capacitor circuit that he modeled in Appendix B and 24 that he compared to experiment in Appendix B. So, I 25 should probably look at Appendix B, so that I'm not --

Page 66 1 Q. Appendix B starts on page 56. Let me 2 know when you're there. 3 A. I am there. 4 Q. So, take a look at whatever is on the 5 first page of Appendix B, or anywhere else in Appendix 6 B, but my question is actually going to be about the 7 rest of the thesis. Is it your understanding that the 8 bulk of Matthew Muh's thesis was directed towards a 9 millimeter-wave CMOS push-push VCO? 10 A. Yes. 11 Q. And so, in Appendix B, what Mr. Muh was 12 doing was evaluating the accuracy of the HFSS model 13 that he was using in the rest of his thesis; is that 14 right? 15 A. To answer that, I'm going to look back 16 to where he refers to Appendix B, which I think was 17 toward the end of his thesis. (Pause.) So, part of 18 his thesis towards the end, and specifically, section 19 3.10, on page 50, he's talking about laying out the 20 VCO in CMOS, utilizing eight layers, et cetera, and he 21 proposes a layout for that a couple of pages later, I 22 think. And then he says, later on, that he included 23 in this layout -- this would be the next page, 51, in 24 the last paragraph, that he included two separate LC 25 tank structures. And the reason for doing that is	Page 68 1 Muh says due to the availability of some measured data 2 from a recent test chip, additional simulations were 3 performed in order to compare HFSS results to measured 4 data. These simulations are described in Appendix B. 5 Is that right? 6 A. Yes. 7 Q. So, Muh's Appendix B is just verifying 8 the accuracy of the HFSS results that he was receiving 9 by using a test chip with known HFSS results 10 associated with that test chip; is that right? 11 A. So, he had measured data from the test 12 chip. He also performed additional simulations of the 13 test chip, and compared those both to the HFSS 14 simulations, that's correct. 15 Q. And if you go down to page 57 of Muh, 16 you look at him describing what he was doing, the 17 third sentence begins, "However." Actually, that's 18 not the sentence I want to start with. The fourth 19 sentence begins, "To obtain." Do you see that? 20 A. Yes. 21 Q. It says, "To obtain a similar value of 22 capacitance as the finger capacitor, a high-K 23 dielectric was sandwiched between the two plates. The 24 value of K was adjusted to resonate the tank at a 25 similar frequency as the actual tank." And he goes on
Page 67 1 that he could make a direct measurement of the 2 resonant frequency, which he might not be able to do 3 exactly if it were embedded in the remainder of the 4 circuit. And so, that's referring to the layouts on 5 the next page. 6 So, and it says further there that one 7 of the test structures that he laid out included only 8 MOS varactors, and the other one included MIM 9 capacitors connected to the tank. That is, finger 10 capacitors. 11 Q. Connected to the tank, right? 12 A. Yes, connected to the inductor. 13 Q. Well, Muh says connected to the tank, 14 right? 15 A. That's right. 16 Q. Not to the inductor. 17 A. He says connected to the tank, that's 18 right. 19 Q. So, you were looking for something that 20 was referring to Appendix B. Did you find that? 21 A. Not yet. 22 Q. I can probably short-circuit, play on 23 words, some of this, if you look at page 42. 24 A. Yes. 25 Q. At the very end of the top paragraph,	Page 69 1 to describe some plotting, some analysis that he did; 2 is that right? 3 A. Yes. 4 Q. So, what Muh did is he took known 5 measurements of this test chip, and in his HFSS model 6 tweaked the HFSS model's value of K to align the data 7 of his HFSS model for his testing that he was doing in 8 the body of his thesis; is that right? 9 A. He was comparing measured results from 10 the test chip which used the finger capacitor. And in 11 his model, in his simulation, for simplicity, rather 12 than trying to model and simulate a finger capacitor, 13 which was actually on the test chip, for which he had 14 data, he was trying to mimic the finger capacitor by 15 using a simple parallel plate capacitor with the same 16 capacitance. And that's why he was tweaking the K 17 value, the dielectric, so he could match the finger 18 capacitor and then use that to do a simpler 19 simulation. So, he actually had a test chip. He 20 measured data with a finger capacitor on it. 21 Q. And we don't know what that test chip 22 looked like, right? If you go back to page 56, all we 23 know is there was a 90-nanometer CMOS test chip that 24 was made available by somebody named Mounir Bohsali; 25 is that right?

Page 70 1 A. Yes, that's right. 2 Q. Did Mr. Muh use a 90-nanometer CMOS 3 tank, CMOS-equipped tank, in the rest of his thesis? 4 A. I don't think so. I think it was a 5 different -- according, at least, if I go back to 6 3.10, he used a 0.13 micron bulk CMOS process for his 7 design. 8 Q. Can you go to page 39 for me, please? 9 So, here, in the body of Mr. Muh's thesis, he's 10 explaining that he was actually modeling for MOS 11 varactors; is that right? 12 A. Yes. That's what I recall. I can look 13 at this. 14 Q. I'm happy for you to. Let me know when 15 you've read through that. 16 A. I see it in the first sentence, and 17 it's confirmed that he's using MOS devices and the 18 varactors. 19 Q. And so, when we look at the structures 20 on page 52 you were talking about before, the tank 21 structure of the LC tanks and the push-push VCO are 22 created using varactors in Muh's thesis, right? 23 A. That is right. 24 Q. What is your understanding of the 25 frequency range that Muh's VCO was intended to operate	Page 72 1 know when you're there. 2 A. Okay. I just got there. 3 Q. The last sentence here refers to a 4 library model. Do you see that? 5 A. Yes. 6 Q. Is that the same kind of library model 7 that you were referring to earlier with your own lab 8 work? 9 A. No. I think this is a model for doing 10 RF simulations. 11 Q. You don't think this is an existing 12 library of P-cells that Mr. Muh had access to when he 13 was creating his thesis? 14 A. Well, let me look back and see what 15 he's doing at this point. He talks about difficult to 16 get a reliable estimate of Q using HFSS, especially at 17 high frequencies. 18 Q. Do high frequencies impact Q value for 19 an LC circuit? 20 A. Yes, the Q is a function of frequency. 21 Q. Do higher frequencies have a bigger 22 impact on Q? 23 A. A bigger impact than, you mean, in the 24 model? 25 Q. Than the use of a lower frequency. In
Page 71 1 at? 2 A. It was a pretty high frequency. I'd 3 have to look back and see. 4 Q. 60 gigahertz ring a bell? 5 A. 60 gigahertz definitely rings a bell. 6 Q. Do you think there was a higher range, 7 as well? 8 A. He talks about some frequencies going 9 up to 100 gigahertz, but I don't know if that's the 10 entire VCO. 11 Q. What are some concerns with operating 12 frequencies that are that high in LC circuits? 13 A. Well, I think any circuit at such a 14 high frequency is going to tend to radiate. So, you 15 know, a lot of the elements in the circuit can act as 16 an antenna. I think, also, the losses can get to be 17 quite high at high frequencies. 18 Q. Was that tied to the transmission lines 19 within the circuit? 20 A. To some extent. So, transmission lines 21 at high frequencies would tend to propagate the 22 EM-wave on the surface of the conductor. You'd have 23 the skin effect and high loss. The higher the 24 frequency, the higher the loss. 25 Q. Can you go to page 46 of Muh? Let me	Page 73 1 the model, yes. 2 A. Yes, apparently, the model becomes less 3 accurate at high frequencies. So, difficult to trust 4 the results. 5 Q. Do LC circuits typically have more loss 6 at high frequencies? 7 A. I think, generally, we can say that 8 that would be the case. 9 Q. Can you go to page 50? I think you 10 were looking at 50 earlier when you found the .13 11 micromere RF bulk CMOS process that was being used to 12 design the VCO of Mr. Muh's thesis? 13 A. Yes. 14 Q. So, this process utilized eight metal 15 layers; is that right? 16 A. Yes. 17 Q. Is that what page 50 says, top 18 sentence, in 3.10? 19 A. That's what that says, yes. 20 Q. It says it was also a design for a 21 nominal supply voltage of 1.2 volts. Do you see that? 22 A. Yes. 23 Q. Does that suggest to you that there was 24 a defined design process that Mr. Muh was using when 25 designing his VCO of his thesis?

Page 74 1 MR. LIU: Objection, form. 2 THE WITNESS: By defined design 3 process, do you mean a standard design 4 process, or for a particular time? 5 BY MR. HALVERSON: 6 Q. Yes. Sorry. We were talking earlier 7 about design rules. I meant to say design rules, a 8 defined set of design rules that Mr. Muh was 9 following. 10 A. I think so. 11 Q. I added another exhibit. I bet you can 12 guess what it is. Bear with me just a second. 13 (Exhibit 582-1007 was introduced.) 14 MR. LIU: Erik, can we take a quick 15 restroom break? 16 MR. HALVERSON: Sure. Ten minutes? 17 MR. LIU: Six minutes will be fine. 18 We'll be back 5:50. Thank you. 19 (A 6-minute recess was taken.) 20 BY MR. HALVERSON: 21 Q. Dr. Prucnal, if you could refresh 22 Exhibit Share. I've added another exhibit, 582-1007, 23 submitted in with your declaration, referred to as 24 Niknejad. Do you see that? 25 A. Yes, I do.	Page 76 1 Q. Have you read the entirety of the 2 textbook? 3 A. No. 4 Q. Have you looked at any other portions 5 of the textbook? 6 A. At various times, I have, but not in 7 connection with this case. 8 Q. And so, was that at various times for 9 your work as a professor, or for different cases, or 10 for something else? 11 A. Work as a professor. 12 Q. If you go to page 11, do you see 13 Chapter 5? 14 A. Page 11 in the contents, yes, I see 15 Chapter 5. 16 Q. Chapter 5 says, Voltage-Controlled 17 Oscillators and Frequency Dividers, right? 18 A. Yes. 19 Q. Did you ask to look at Chapter 5 or 20 include Chapter 5 as part of your analysis? 21 A. I didn't. 22 Q. Why? 23 A. I was just looking for a description of 24 finger capacitors. Muh was Niknejad's student, and he 25 referred to a chip that had been made that had an LC
Page 75 1 Q. Do you recognize that? 2 A. I do. 3 Q. Now, Niknejad is, as a reference as a 4 whole, is a textbook; is that right? 5 A. Yes. 6 Q. And so, you've included a subset of 7 that textbook, right? 8 A. Yes. 9 Q. So, if we look at the last page of what 10 you have looked at, in the bottom right-hand corner we 11 see Exhibit 1007, page 63 of 63, right? 12 A. Yes. 13 Q. And the top left corner we see 108; is 14 that right? 15 A. Yes. 16 Q. If we go back to page 9 of the pdf -- 17 A. Okay. I'm on page 9. 18 Q. Page 9 begins the Table of Contents; is 19 that right? 20 A. Yes. 21 Q. So, we see on page 9 two chapters, 22 Chapter 1 and 2, and on page 10 we see 3 and 4, on 11 23 we see 5 and 6, and then on 12 we see Chapter 7 and 24 the index indicated, right? 25 A. That's right.	Page 77 1 circuit on it with a finger capacitor. It's pretty 2 well-known what a finger capacitor looks like, but 3 this textbook had some discussion and an illustration 4 of the finger capacitor. That's really all. 5 Q. And Muh's thesis was titled, "Design of 6 a FinFET static frequency divider and a 7 millimeter-wave CMOS push-push VCO," right? 8 A. I don't have it in front of me, but 9 I'll take your word for it. I think so. 10 Q. I'm happy to represent that I read 11 that. VCO is voltage-controlled oscillator, right? 12 A. Yes. 13 Q. And frequency divider, the second half 14 of Chapter 5, right? 15 A. Yes. 16 Q. If you look down at 5.4.2, we see 17 push-push oscillators, right? 18 A. Yes. 19 Q. If you look at 5.4.1, we see 20 millimeter-wave oscillators, right? 21 A. Yes. 22 Q. None of that you thought would be 23 relevant to your opinions on Muh's thesis titled 24 Design of a FinFET status frequency divider in a 25 millimeter-wave CMOS push-push VCO?

Page 78 1 MR. LIU: Objection to form. 2 THE WITNESS: Well, as we discussed, my 3 focus was not on the heart of the thesis. My 4 focus was on the Appendix B, and the fact that 5 he referred to a test chip that had an 6 inductor and finger capacitor. So, that was 7 really the focus of my attention, not the rest 8 of the thesis. 9 BY MR. HALVERSON: 10 Q. So, back in your declaration -- we're 11 going to bounce back and forth a little bit. I'm not 12 sure if you have a way of opening two windows, one 13 with your declaration and one with Niknejad? 14 Otherwise, we can just go slow. 15 A. I have a hard copy of it behind me on 16 the table, and it hasn't been marked. If I could use 17 that? 18 Q. If you want to use the hard copy of 19 your declaration, that's probably fine. 20 A. I think it would speed things up rather 21 than flipping back and forth. 22 Q. Yeah, why don't you grab that, if you 23 don't mind. 24 MR. HALVERSON: Or Charles, is that 25 okay if he uses that?	Page 80 1 A. Yes. 2 Q. You added the green line on the right? 3 A. Yes. 4 Q. And then you added a yellow box in the 5 middle? 6 A. Yes. 7 Q. What's the yellow box intending to 8 describe or convey? 9 A. The yellow box conveys the region where 10 the electrode segments are located. 11 Q. And you confined the yellow box, 12 because it doesn't go all the way to the green or the 13 red. What was the intent with that? 14 A. Well, it could have gone to the green 15 or red. I think it was just arbitrary. The way it's 16 drawn here, the boundaries extend to the end of the, 17 say, the short end of the electrodes, and not all the 18 way to the base of the electrode. 19 Q. So, it reflects where more capacitance 20 is generated as opposed to off the tip of the finger, 21 where there would still be capacitance, but less so 22 than across the broad side of the finger? 23 A. I think that would be the case. That 24 wasn't the intention of putting the yellow box here, 25 but that would be the case.
Page 79 1 MR. LIU: That's fine. 2 THE WITNESS: Do you want to grab that, 3 Charles? The big notebook. Thank you. So, I 4 have the hard copy of the declaration here. 5 BY MR. HALVERSON: 6 Q. Just so that we're all on the same 7 page, the last page has your signature on it, and the 8 front page says something about the '582 patent? 9 A. Last page has my signature. Front page 10 is about the '582 patent. 11 Q. And there's 166 pages in it? 12 A. 166 pages in it, yes. 13 Q. Okay. I will assume we're on the same 14 page, and that that is an entire version of your 15 declaration in this matter. So, if you could flip to 16 paragraph 77, it is on page 35. 17 A. Got it. 18 Q. And it refers to Figure 3.11 of 19 Niknejad, which can be found in Niknejad at page 27. 20 A. I see that reference. Would you like 21 me to go to page 27? 22 Q. I would, please. 23 A. Okay. I'm on page 27 of Niknejad. 24 Q. So, you added the coloring, right? You 25 added the red line on the left?	Page 81 1 Q. So, here, in your declaration at 2 paragraph 77, you've oriented Niknejad's Figure 3.11 3 in the same manner that it's oriented in Niknejad, 4 itself, right, vertical, with a clean corner on the 5 top of both, which you've labeled as connecting 6 segments, and a jagged corner on the bottom of each of 7 which you've labeled as connecting segments? 8 A. Yes. 9 Q. And that jagged line in Niknejad, 10 itself, in Figure 3.11, indicates to the reader that 11 their capacitor could be bigger, right, could have 12 more to it? 13 A. Well, it could indicate that. It could 14 also indicate that these are the connecting segments 15 of the capacitor, and those would be extended to 16 connect to whatever it's going to connect to. So, it 17 could just be an extension -- 18 Q. So -- 19 A. Sorry. 20 Q. Go ahead. 21 A. I was being pensive. 22 Q. And I was being jumpy. 23 A. Just to summarize, the jagged edge 24 could either indicate the extension of the connecting 25 segments or of the capacitor itself to have more

Page 82 1 electrodes, as well. 2 Q. So, if you were to connect an 3 interdigitated capacitor, such as this one of 4 Niknejad, to a voltage source, such that the voltage 5 came in at that jagged line as opposed to down from a 6 via, how would that impact how the capacitance at the 7 various fingers would occur? 8 MR. LIU: Objection to form. 9 THE WITNESS: Well, in the capacitor, 10 presumably, there would be some resistive 11 loss, perhaps some voltage drop, from one end 12 of the line to the other. So, it may be that 13 there's less, slightly less voltage applied to 14 the capacitors that are at the -- the fingers 15 that are at the furthest extreme of the finger 16 capacitors, the higher voltage closer in. 17 BY MR. HALVERSON: 18 Q. And so, to minimize that loss, you 19 would want to minimize the average distance from 20 voltage source to capacitor; is that right? 21 A. Let's see, minimize the average 22 distance. I would say something like that. I'm not 23 sure it's quite that straightforward, but something 24 like that. You would want to minimize the distance, 25 as a whole, of these electrode segments to the voltage	Page 84 1 the '582 patent that describe a joining portion? 2 A. I am familiar with them. 3 Q. If we call that line the joining 4 portion, that joining portion goes in the same 5 direction as the green segment 133 that you've circled 6 in Figure 9, right? 7 MR. LIU: Objection, form. 8 THE WITNESS: So, that joining 9 direction -- 10 BY MR. HALVERSON: 11 Q. Joining portion? 12 A. Joining portion, yes, lies in the same 13 direction as the, I guess, the green area called 133, 14 I suppose. The answer is yes. 15 Q. You reviewed the '582 patent as part of 16 this exercise, right? 17 A. Yes. 18 Q. And as part of the other cases that are 19 involved in the '582 patent that you've talked about? 20 A. Right. 21 Q. Is it fair to say you've read it more 22 than once? 23 A. That's right. 24 Q. And you've reviewed other patents for 25 other cases, right?
Page 83 1 source. I don't know if you mentioned vias or not, 2 but that would be one reason to place these connecting 3 segments directly under the electrode segments of the 4 inductor, so that you're minimizing the average 5 distance, or at least the average loss, and coming 6 directly down from the electrode segments to these 7 connecting segments. I think that would minimize the 8 loss in the connection. 9 Q. Do you have your declaration in front 10 of you? 11 A. Yes. 12 Q. Let's shift gears a little bit. If you 13 could go to page 141, an image that's associated with 14 paragraph 229. 15 A. Okay. 16 Q. So, here you've colored some aspects of 17 Figure 9 red and green and yellow, right? 18 A. Yes. 19 Q. I want to focus on the green and 20 yellow, and you've got an intersection or meeting 21 place for the green and the yellow combined. Do you 22 see that? There's a line there where those two colors 23 touch. 24 A. Yes. 25 Q. You're familiar with the passages in	Page 85 1 A. Yes. 2 Q. Is your understanding of a patent 3 specification that it needs to describe only one way 4 of doing something? 5 A. I think that's correct. 6 Q. Have you ever heard of the concept of 7 embodiments? 8 A. Yes. It's a way of doing something. 9 Q. So, have you ever seen a patent that 10 describes multiple embodiments? 11 A. Yes. 12 Q. And so, have you seen a claim of a 13 patent that claims one embodiment, as described in a 14 patent specification? 15 A. That's getting a bit into legal 16 territory, and I'm not sure. 17 Q. That's fine. You've, as far as I can 18 tell, not provided any explicit claim constructions in 19 your declaration. Is that fair? 20 MR. LIU: Objection, form. 21 THE WITNESS: I'm just checking. 22 Apparently, I have not provided any of my own 23 claim constructions in the declaration. 24 BY MR. HALVERSON: 25 Q. And so, is it your understanding that

Page 86 1 you've analyzed the claims under their ordinary and 2 customary meaning? 3 A. Yes, I have. 4 Q. And so, I didn't see this before, but 5 there's a reflection of a large display screen in the 6 window behind you. When you keep looking up, are you 7 looking up at an external monitor or a projector 8 display screen? 9 A. I'm looking directly at your face. 10 Q. Oh, that's unfortunate. 11 A. So, I have in front of me my laptop, 12 and my laptop is connected to a large display so that 13 I can see the documents better. And I've got you and 14 the other images just next to that. And I guess it's 15 reflecting -- oh, it's getting dark out, so it's 16 reflecting in the window behind me. 17 Q. So, there's no projector up on the wall 18 or anything. What I see in the window is your display 19 screen? 20 A. Yes, it's exactly what I have on my 21 display. 22 MR. LIU: We can lower the blinds. 23 MR. HALVERSON: No, it's okay. 24 (Exhibit 582-1032 and Exhibit 582-1033 25 were introduced.)	Page 88 1 could be one large capacitor, because it doesn't show 2 any more detail. In Figure 2, which shows more 3 detail, it seems to have cut that capacitor into 4 pieces. So, I'd have to look to the text to see how 5 Figure 2 is described. 6 Q. If you go to page 12 and look at 7 paragraph 13, or if you look at paragraph 26, I'm not 8 sure Daley describes a lot specifically about Figure 9 2. My understanding is that most of the description 10 is like what is done in paragraph 22, where there is 11 reference to Figures 1, 2, 2A and 2B, and is generally 12 describing the concept of what Daley considered to be 13 his invention. So, by all means, free feel to skim 14 through the rest of Daley, if you think that would be 15 helpful. 16 A. Okay. I think this would take me quite 17 a bit of time to sift through, because apparently, 18 it's not just paragraph 22 that's describing this. I 19 do see places where Daley is referring to a singular 20 capacitor, but I would have to flip through back and 21 forth to the figures to identify that. 22 Q. Okay. Let's go back to Niknejad, then, 23 582-1007, page 27, which is section 3.1.3.1. 24 A. Okay. 25 Q. So, is it your understanding that the
Page 87 1 BY MR. HALVERSON: 2 Q. If you can refresh Exhibit Share, I 3 want to ask about Exhibit 582-1032, which is the Daley 4 publication. And you're welcome to look at 1033, 5 which is Jing. I uploaded that on accident. I'm not 6 going to ask you about that right now. 1032. 7 A. Okay. I've got it. 8 Q. So, Daley describes a large capacitor 9 16 in its figures; is that right? 10 A. Yes. 11 Q. There's a bunch of interdigitated 12 fingers associated with that capacitor; is that right? 13 MR. LIU: Objection, form. 14 THE WITNESS: I'm trying to enlarge it 15 so I can see. 16 BY MR. HALVERSON: 17 Q. Figure 2 may be the easiest. Figure 1, 18 maybe you can see them. 19 A. Now I do. I see it in both. 20 Q. And I believe there's a passage in 21 Daley, itself, it's not all that important, but you're 22 welcome to zoom into the text, as well. But my 23 question is how many capacitors are there in Daley? 24 A. Well, this, as you said, has 25 interdigitated fingers, and from Figure 1, it almost	Page 89 1 right-hand image is a cross-section of, for example, 2 the top four interdigitated fingers of the left-hand 3 image? 4 A. Yes, this cross-section describes or 5 shows the cross-section of four of the fingers. The 6 left side is the top view. The right side is the 7 cross-section. The cross-section shows that each of 8 the fingers extends downward and is connected by vias 9 to corresponding fingers on successively lower layers. 10 Q. So, the intent would be that the 11 left-hand image is five layers deep, if you were to 12 combine the two? 13 A. It could be. You were right that the 14 image on the right-hand side shows five metal layers. 15 It doesn't count all of them. It's a little curious, 16 because it says metal 1, metal 2, dot, dot, dot, then 17 top metal. So, the dot, dot, dot, might indicate, as 18 he says above, that all available metal layers are 19 stacked together. So, this would be representative of 20 however many available layers were there to be stacked 21 together. 22 Q. So, on the right-hand side of this 23 Figure 3.11, there are little capacitor symbols 24 between the vias, but not between the metal layers. 25 Do you know why?

Page 90 1 A. Yeah, I think he's illustrating a point 2 that he makes at the top, which is that -- rather, 3 that he makes in the paragraph above it, that it's 4 desirable to use as many vias as possible, because in 5 doing so, the capacitance between the vias will serve 6 to increase the overall capacitance between the 7 plates. The plates being the vertical structures. 8 Q. So, Niknejad's Figure 3.11 is not 9 saying that there's no capacitance between the two 10 fingers on a given metal layer; just that you get 11 additional capacitance between the metal vias that sit 12 between each metal layer? 13 A. That's what I believe he's saying, yes. 14 Q. Let's go back a page for a second, 15 please, to 26. 16 A. Okay. 17 Q. The bottom paragraph here, the third 18 sentence says, "In this way, the Q-factor is 19 insensitive to small lead inductance and resistance." 20 What does that mean, "insensitive to?" 21 A. In order to tell you, I need to read a 22 little bit around that sentence. (Pause.) So, what 23 he's saying is that they've designed a ring inductor, 24 and they want to measure its Q-factor, and they do 25 that by making a resonant circuit, a parallel LC	Page 92 1 got the terminology backwards. The MIM are two 2 parallel plates with a high K dielectric in the 3 middle, and the MOM are layers of metal with oxide 4 between them. 5 Q. Do you agree that MIM capacitors have 6 better linearity than MOM capacitors do? 7 MR. LIU: Objection, form. 8 THE WITNESS: I guess I'd have to 9 understand linearity to what? Like, what are 10 we plotting to determine linearity? 11 BY MR. HALVERSON: 12 Q. Behavior over a range of current or 13 voltage. Have you ever heard of the term linearity to 14 describe a circuit? 15 A. Linearity describes the circuit, the 16 input/output response of a circuit. Generally, I 17 think -- 18 Q. To what? 19 A. Sorry? 20 Q. What do you mean by that, it describes 21 the input/output response of a circuit. The response 22 to what? 23 A. To an input signal to the circuit. So, 24 generally, when I think of linear components, I'm 25 thinking of things like resistive components, where
Page 91 1 circuit, and the C in the LC are MIM capacitors, such 2 as we've been discussing. And by doing that, by 3 putting it in parallel, at resonance, the circuit is 4 open, it's a large impedance, and so at resonance, any 5 small lead inductance or any other resistances, small 6 resistances, would be negligible compared to the large 7 impedance of the circuit. I think that's what it's 8 saying. 9 Q. And you said MIM capacitor, such as 10 we've been discussing. What do you mean by that? 11 A. Vertical parallel plate capacitors. 12 But I just threw that in. 13 Q. But if you go to the next page, 14 Niknejad's vertical parallel plate capacitors are MOM 15 capacitors, right? 16 A. Maybe I got that backwards. Maybe it's 17 possible that the VPP capacitors are MOMs. 18 Q. When you say VPP capacitors, what are 19 you referring to now? 20 A. So, the vertical parallel plate 21 capacitors are shown on the next page in Figure 3.11, 22 and those are actually the metal-oxide-metal 23 capacitor. I've gotten the nomenclature wrong. The 24 MIM capacitors are the parallel plate capacitors. So, 25 when I talked earlier about MOM and MIM, I believe I	Page 93 1 you have current versus voltage. And a linear 2 resistor is a straight line. A nonlinear resistor is 3 a diode. So, I wouldn't typically think about the 4 linearity of the capacitor or inductor. I usually 5 think about its response as a function of frequency. 6 So, I would think about the impedance of the capacitor 7 or inductor. 8 MR. HALVERSON: Why don't we take five 9 minutes. I might be done. 10 THE WITNESS: Thank you. 11 MR. HALVERSON: 6:35. 12 MR. LIU: Sounds good. 13 (A 5-minute recess was taken.) 14 BY MR. HALVERSON: 15 Q. Do you still have Muh available, 582 16 Exhibit 1006? 17 A. I have Niknejad open, so I'll go back 18 and open Muh. 19 Q. Could you go to page 39 for me, please? 20 A. Okay. 21 Q. The second to last sentence of page 39 22 says, "To minimize the effects of polysilicon gate 23 resistance and N well series resistance and thereby 24 maximize Q, each gate finger of the varactor was 25 designed at the minimum recommended length and width."

Page 94 1 Do you see that? 2 A. Yes. 3 Q. So, you would agree that Muh, here, is 4 explaining that one of his goals is to maximize Q; is 5 that right? 6 MR. LIU: Objection, form. 7 THE WITNESS: Well, generally, I'm not 8 sure what else he's talking about in this 9 paragraph, although he seems to start off by 10 talking about varactors in accumulation mode, 11 MOS devices, and then he's talking about the 12 design of that capacitor, and then he says he 13 wants to maximize the Q. 14 BY MR. HALVERSON: 15 Q. And you would agree that here, one of 16 the goals that Muh is explaining is his desire to 17 maximize Q? 18 A. Yes. Yes. And he's doing that, in 19 part, by trying to minimize the gate resistance, 20 polysilicon gate resistance, and also the N well 21 series resistance. 22 Q. So, one way he does that is minimizes 23 the length and width of the lead that leads to that 24 gate; is that right? 25 A. I don't recall what the layout was of	Page 96 1 Q. Just making sure. Can you go to page 2 115 for me? 3 A. Okay. 4 Q. 115, associated with paragraphs 185 and 5 186 of the '582 declaration, which is your opinions 6 about claim 4; is that right? 7 A. That's right. 8 Q. And so, here, it's your opinion that 9 the claim scope of claim 4 is the same as the claim 10 scope of claim 1; is that right? 11 MR. LIU: Objection, form. 12 THE WITNESS: Well, what I'm saying 13 here is that I'm adopting Realtek's position, 14 where Realtek said that the first region of 15 claim 4 has the same scope as the first region 16 of claim 1. 17 BY MR. HALVERSON: 18 Q. So, you doesn't have any opinion, one 19 way or another, about whether or not claim 4 has the 20 same scope as claim 1, right? 21 A. Unless I express it elsewhere, I've 22 just adopted Realtek's interpretation. 23 Q. And where did you get Realtek's 24 interpretation from? 25 A. As I recall, this had to do with -- and
Page 95 1 this MOS varactor and what the gate fingers looked 2 like, but he is saying that he wants to minimize the 3 recommended length and width of the gate fingers. 4 Q. Do you recall Muh ever describing what 5 the gate fingers of his thesis looked like? For what 6 it's worth, I don't. I'm just wondering if I missed 7 it somewhere. 8 A. No, I didn't see that in going through 9 it. 10 Q. Do you still have your declaration? Go 11 to page 52 for me. Paragraph 94 of your '582 12 declaration is describing a, "capacitor component 150 13 is arranged, corresponding to the first region 120, on 14 a lower surface," and then it goes on. And then you 15 paraphrase it, perhaps, I'm not really sure, but you 16 use the introductory phrase, "In other words." Do you 17 see that? 18 A. Yes. 19 Q. So, when you use the introductory 20 phrase, "In other words," are you trying to provide an 21 example of what you've just described in the preceding 22 sentence? 23 A. I think I'm just trying to paraphrase 24 or state differently what is stated in the first 25 sentence.	Page 97 1 I may be wrong. I think it had to do with 2 infringement contentions, where Realtek was contending 3 that the accused products infringed on the '582, and 4 used this position, that the first region of claim 4 5 was the same as the first region of claim 1. 6 Q. So, do you agree that the first region 7 of claim 4 is the first region of claim 1? 8 A. I'm not sure that I've fully analyzed 9 that. I mean, I can look now and see what my opinion 10 is off the top of my head, but if I just adopted 11 Realtek's interpretation, then that's the extent of my 12 opinion. 13 Q. Are you aware of anywhere else in your 14 '582 IPR declaration that we've been looking at today 15 where you had offered any opinions about Gonzalez as 16 it relates to claim 4? 17 A. Well, not off the top of my head, at 18 this moment. So, I could look through. It's the only 19 thing I can do at this point, to see if I talk about 20 claim 4 in this or anywhere else. Would you like me 21 to look through and confirm, or not? 22 Q. You're welcome to. I don't think it's 23 in there. I didn't see anything else. I just want to 24 make sure that you didn't intend to have anything else 25 anywhere else. Because as I read those two

Page 98 1 paragraphs, I don't see any other analysis. I just 2 want to make sure I'm not missing it. 3 A. I don't think you are. I think that's 4 the extent of it. 5 MR. HALVERSON: Okay. So, with that, 6 Dr. Prucnal, I don't have any other questions 7 on the '582, subject to anything from our dear 8 friend Charles. That's all I've got. Thank 9 you very much. 10 THE WITNESS: Thank you. 11 MR. LIU: Could you give us a few 12 minutes, and I'll decide whether I have any 13 questions? 14 MR. HALVERSON: Sure. You want five? 15 Is that enough? 16 MR. LIU: Let's do ten. 17 MR. HALVERSON: Sounds good. We'll be 18 back at 55. 19 MR. LIU: Five is fine. 20 MR. HALVERSON: Okay. We'll be back at 21 50. 22 (A 5-minute recess was taken.) 23 MR. LIU: I just have a few simple 24 questions. 25 BY MR. LIU:	Page 100 1 BY MR. LIU: 2 Q. And the same is true of the Out- side, 3 right, the fingers are also connected to the N+ poly 4 on the Out- and then down to the gate-oxide. Is that 5 fair? 6 A. Yes, that's right. 7 Q. So, what role does the finger electrode 8 play in this MOS varactor? 9 A. Well, there are two roles that the 10 F-shaped fingers play. One is this can serve as an 11 interdigitated capacitor, where the fingers on one 12 side are interleaved with the fingers on the other. 13 And the other role it can play is that it serves as an 14 interconnection to the MOS varactor that is beneath, 15 bringing the Out+ voltage and the Out- voltage to the 16 appropriate gate-oxides. So, as such, the electrodes 17 both provide a capacitance between them, and serve as 18 part of the capacitor component that includes both the 19 MOS varactor and its interconnections. 20 Q. Can we go to Figure 8? Do you recall 21 discussing this figure? It's on page 8 of Gonzalez. 22 A. I've got it. 23 Q. Those metal fingers that we just 24 discussed, those are connected to the inductor that's 25 on the top half of Figure 8, correct?
Page 99 1 Q. Dr. Prucnal, can you go to Exhibit 2 1005, the Gonzalez reference, Figure 5 on page 6? Do 3 you recall discussing this figure? 4 A. Yes. 5 Q. As part of that discussion, I believe 6 you said at some point that, in Figure 5, on the 7 right-hand side, the electrodes are not playing a role 8 in the capacitance; it's the source gate interface 9 that is causing the capacitance of the MOS varactor. 10 Do you recall that testimony? 11 A. I recall the general testimony. 12 Q. So, I just wanted to get some 13 clarification on what you meant. So, here, I believe 14 you discussed the F-shaped metal fingers on the left 15 side of Figure 5. Do you recall that? 16 A. Yes. 17 Q. Is each finger connected to the N+ poly 18 on top of the gate-oxide on the right-hand side of 19 Figure 5? 20 A. Yes. 21 MR. HALVERSON: Objection, form. 22 THE WITNESS: Here we have the fingers 23 with the F-shape layout, and they are 24 connected through vias down to Out+ to the N+ 25 poly.	Page 101 1 MR. HALVERSON: Objection, form. 2 THE WITNESS: So, the F-shaped fingers 3 that we just discussed are connected to the 4 connecting segments, which are the yellow 5 segments extending under the extension 6 segments, which are brown, and those are 7 ultimately connected to the upper portion of 8 Figure 8 to the loop. Was that your question? 9 BY MR. LIU: 10 Q. Yes. 11 A. Okay. 12 Q. So, the fingers are part of the LC 13 resonant circuit? 14 A. Yes, they are. 15 MR. HALVERSON: Objection, leading. 16 BY MR. LIU: 17 Q. Are all the fingers part of the LC 18 resonant circuit? 19 A. The fingers are part of the LC resonant 20 circuit, and as I said, for two reasons. One, because 21 they serve as a finger capacitor, and the other 22 because they serve as interconnections providing the 23 appropriate voltage levels to the gates of the N-minus 24 varactor, the varactor and the interconnections. The 25 interconnections are part of the capacitor component,

Page 102 1 including the varactor and the fingers. 2 MR. LIU: No more questions. 3 BY MR. HALVERSON: 4 Q. Very briefly, Dr. Prucnal, if you go 5 back to Figure 5 for me, to make sure I understand 6 this, so there is an F-shaped conductive piece on the 7 left that's labeled Out+, right? 8 A. Yes. 9 Q. There is an inverted F-shaped 10 conductive piece on the right that's labeled Out- 11 right? 12 A. Yes. 13 Q. Each of those F's have a, in this 14 figure, vertical, top to bottom of the page, lead, as 15 well as two horizontal leads; is that right? 16 A. So, each of those F's, I would call the 17 vertical lead a connecting segment, that connects the 18 fingers that extent horizontally. 19 Q. So, as you sit here today, it's your 20 opinion that the horizontal top finger of the Out+ F 21 and the horizontal top finger of the Out- inverted F, 22 together, form a capacitor? 23 A. Yes. The collection of these fingers 24 on the left and the right will form a finger 25 capacitor. The fingers are somewhat spaced apart, but	Page 104 1 A. I would expect the capacitor, the 2 varactor, the MOS varactor, to have a greater 3 capacitance. 4 Q. How far apart are the two components of 5 the F and inverted F in that last question? 6 A. I think that the position of the F, the 7 normally-oriented F, would correspond to where that 8 via comes down, that that position would correspond to 9 the position of the Out+ on the right-hand side of 10 Figure 5 on the cross-section. There's an Out+ via 11 that comes down to the poly and the gate-oxide, and 12 that would, sort of, mark the location of the upper 13 portion of the non-inverted F, if you will. 14 Q. Yep. 15 A. Then the Out-, the inverted F, would 16 have a corresponding via that connects down to the 17 Out- connection, same Figure 5, on the right-hand 18 side, to the N+ poly and gate-oxide. So, I don't know 19 that this is an exact -- you know, the cross-section 20 is sort of a schematic representation of the MOS 21 varactor. I don't take it to be literally exactly how 22 it's laid out. But at least in terms of the way these 23 figures are drawn, I think the separation between the 24 fingers on the Out+ side and the Out- side would 25 correspond to the separation between these two vias,
Page 103 1 nevertheless, have some capacitance between them. 2 Q. So, earlier today we were talking about 3 a capacitance that was formed between the Out+ via and 4 the Vc via in the right-hand side of Figure 2, right? 5 A. One moment. I don't recall that. Let 6 me look at Figure 2. 7 Q. Sorry, Figure 5. Same figure. I said 8 the wrong thing. Let me ask it again. Can you go 9 back to Figure 5? 10 A. I'm there. 11 Q. And so, earlier today we were talking 12 about how in the right-hand portion of Figure 5 there 13 was a capacitance between the Out+ via and the Vc via. 14 Do you remember that? 15 A. The Out+ via and the Vc via, yes, I was 16 talking about the capacitance in the MOS varactor 17 between the source and the gate through the 18 semiconductor. I think that's what I was talking 19 about. 20 Q. And so, comparing the capacitance in 21 the MOS varactor between the source and the gate, and 22 the capacitance between a horizontal top finger of the 23 Out+ F and the horizontal top finger of the Out- 24 inverted F, which of those two has a greater 25 capacitance?	Page 105 1 Out+ and Out-. 2 Q. And so, you're disregarding the 3 teaching of the left side of Figure 5 that shows three 4 Vc vias between the Out+ via and the Out- via when you 5 come to that conclusion; is that right? 6 MR. LIU: Objection, form. 7 THE WITNESS: Well, I said that this is 8 a schematic representation of the MOS 9 varactor, and it doesn't necessarily represent 10 dimensions. I believe I said that. So, if we 11 look at the top half, as you've just pointed 12 out, then the distance between them would be 13 the distance as seen between the fingers of 14 the non-inverted F and the inverted F. And 15 there, the spacing would be different, if you 16 look at the middle two fingers versus the 17 outside fingers. I don't know what's adjacent 18 to that. 19 BY MR. HALVERSON: 20 Q. What's the typical spacing between 21 fingers in an interdigitated finger capacitor? 22 A. I don't have a feeling for that, and I 23 don't think there's a typical spacing. That's going 24 to depend upon many things, as you probably know. 25 It's going to depend upon the capacitance that's

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1 desired, the type of insulator between them, the
2 thickness and width of the fingers, as well as the
3 length of the fingers. So, all those various
4 parameters would come into design considerations that
5 would also relate to the separation.
6 Q. So, in a 56-gigahertz LC tank VCO made
7 in a 65-nanometer process, what kind of separation
8 would two fingers of a finger capacitor have?
9 A. I don't know, off the top of my head.
10 Q. How would you figure that out?
11 A. Well, that's why simulations are done,
12 you know, something is laid out, as you see here, and
13 it has a number of parameters that can be adjusted to
14 see how the whole circuit works as a whole. There's
15 many things that come to bear here, and it's not just
16 going to be the separation of the fingers, but the
17 relationship of the fingers to each other, and other
18 conductors to each other. So, there's a lot of things
19 that will go on, as well as the functionality of
20 bringing these fingers to deliver the voltages as
21 interconnects, to deliver the voltages to the MOS
22 varactors.
23 MR. HALVERSON: I have no further
24 questions, again, subject to anything from
25 Charles.

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1 MR. LIU: None here.
2 MR. HALVERSON: Thank you, Dr. Prucnal.
3 I appreciate your willingness to squeeze this
4 in. I know it's been a long day.
5 THE WITNESS: Thank you. As always,
6 it's a pleasure talking with you.
7 COURT REPORTER: Mr. Liu, do you need a
8 copy of the transcript?
9 MR. LIU: Yes.
10 MR. HALVERSON: I need it faster than
11 normal, a final by end of day Monday, with a
12 rough sometime today.
13 MR. LIU: Same, yes, rough today and
14 final Monday.
15 (Deposition concluded at 7:06 p.m.)
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1 REPORTER'S CERTIFICATE
2
3 I, Nancy Carides, RMR, CRR, a Notary Public and
4 Certified Court Reporter of the State of New Jersey,
5 License No. 30XI00236500, do hereby certify that prior
6 to the commencement of the examination, DR. PAUL R.
7 PRUCNAL was duly sworn by me to testify the truth, the
8 whole truth and nothing but the truth.
9 I DO FURTHER CERTIFY that the foregoing is a
10 true and accurate transcript of the testimony as taken
11 stenographically by and before me at the time, place
12 and on the date hereinbefore set forth.
13 I DO FURTHER CERTIFY that I am neither a
14 relative nor employee nor attorney nor counsel of any
15 of the parties to this action, and that I am neither a
16 relative nor employee of such attorney or counsel, and
17 that I am not financially interested in the action.
18 
19
20
21 Notary Public of the State of New Jersey
22 My commission expires March 17, 2024
23
24 Certification Date: January 28, 2024
25

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Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

DISCLAIMER: THE FOREGOING FEDERAL PROCEDURE RULES ARE PROVIDED FOR INFORMATIONAL PURPOSES ONLY.

THE ABOVE RULES ARE CURRENT AS OF APRIL 1, 2019. PLEASE REFER TO THE APPLICABLE FEDERAL RULES OF CIVIL PROCEDURE FOR UP-TO-DATE INFORMATION.

VERITEXT LEGAL SOLUTIONS

COMPANY CERTIFICATE AND DISCLOSURE STATEMENT

Veritext Legal Solutions represents that the foregoing transcript is a true, correct and complete transcript of the colloquies, questions and answers as submitted by the court reporter. Veritext Legal Solutions further represents that the attached exhibits, if any, are true, correct and complete documents as submitted by the court reporter and/or attorneys in relation to this deposition and that the documents were processed in accordance with our litigation support and production standards.

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