Chapter 5
Voltage-Controlled Oscillators and Frequency Dividers

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5.1 Considerations of VCOs

Voltage-controlled oscillators (VCOs) and frequency dividers play critical roles in all synchronous circuits. They comprise the core components in phase-locked systems, sometimes necessitating co-design and having great influence on the overall performance. Even though we have witnessed a proliferation of VCO and divider topologies in the past two decades of Si RF, high performance oscillators and dividers operating in the mm-wave range continue to pose difficult challenges even in today's technology. We begin our discussion with basic oscillation properties as well as a VCO figure of merit.

Oscillation behavior can be explained in different ways. A well-known model is shown in Fig. 5.1(a), where an amplifier $A(s)$ is placed in a feedback loop. The overall transfer function is given by

$$H(s) = \frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + A(s)}. \tag{5.1}$$

To make it oscillate at certain frequency ω_{osc}, we must satisfy the Barkhausen criteria

$$|A(j\omega_{osc})| = 1 \tag{5.2}$$

$$\angle A(j\omega_{osc}) = 180^\circ, \tag{5.3}$$

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which govern all kinds of oscillators. These conditions are actually self-proven: a "stable oscillation" exactly implies "unity loop gain" and "total phase shift of 0°" (or a multiple of 360°). Physically, oscillation initiates from white noise, an initial condition (charge on a capacitor), or a "kick", an input waveform with sufficient spectral content to excite the right half plane poles of the system. We set a loop gain greater than unity in actual designs so as to start up the oscillation. While the energy at other frequencies decays eventually, the component at ω_{osc} survives and grows up until the effective loop gain drops to unity. Since all the coefficients of $H(s)$ are real, the poles of $H(s)$ should be either real or complex conjugate pairs. In steady-state oscillation, all of the poles of H(s) are pushed to the left-hand side except that one dominant pair locates at the $j\omega$-axis [Fig. 5.1(b)]. The output in frequency domain can be represented as

$$V_{out}(s) = \frac{a_0 s + b_0}{s^2 + \omega_{osc}^2} + \sum_i \frac{c_i s + di}{(s+\alpha_i)^2 + \beta_i^2} + \sum_j \frac{e_j}{s + \gamma_j}, \tag{5.4}$$

where the coefficients $\{\alpha_i\}$ and $\{\gamma_j\}$ are positive. Since the second and the third terms of Eq. (5.4) produce transient responses only, the time-domain output in steady state is indeed a sinusoid.

By the same token, we can depict the loop gain $A(s)$ in Gaussian plane, arriving at a Nyquist plot as shown in Fig. 5.1(c). The curve passes through $(-1, 0)$ whenever a stable oscillation occurs.

In most cases, an oscillator could become useful only if its frequency is tunable. The tuning range must be large enough to cover the overall bandwidth of interest with sufficient margin for process, temperature and supply (PVT) variations. Also, in a PLL, the VCO gain (K_{VCO}) must be kept as constant as possible, otherwise the loop phase margin suffers. Compared to wireless LAN systems at 2.4 or 5.2 GHz, the 60-GHz indoor RF band, for example, has 7-GHz unlicensed band available. The VCO must accommodate as wide as 15% of the center frequency, across which no serious deviation is allowed.

The output purity of VCOs is quantified as phase noise, i.e., the cyclic uncertainty induced by the noise of the active and passive devices. The phase noise is defined as "the relative noise power per unit bandwidth at certain offset with respect to the carrier power". That is,

$$L(\Delta\omega) = 10\log_{10}\left(\frac{P_{\text{noise}}}{P_{\text{signal}}}\right)(\text{dBc/Hz}). \tag{5.5}$$

Phase noise has been studied extensively and a great volume of references can be found in the literature. Here we state without proof that for an inductor-based oscillator with quality factor Q, the phase noise can be represented as [1]

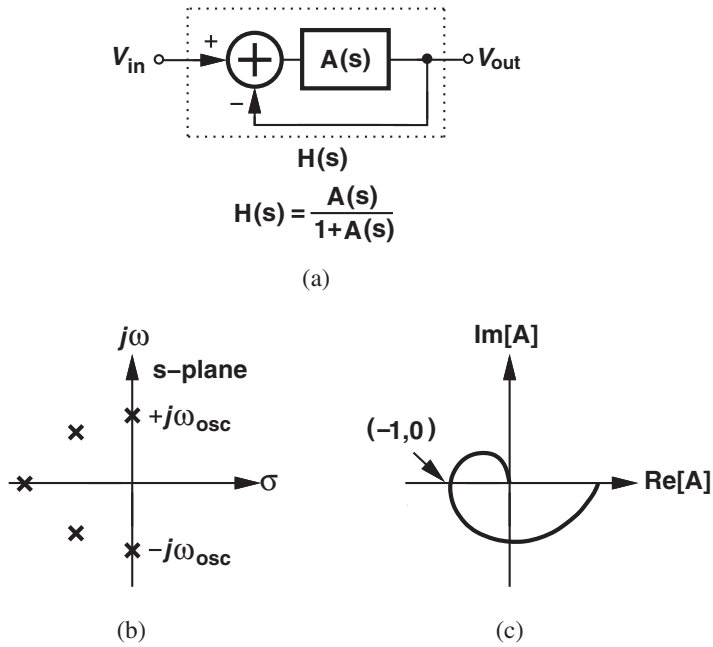


Fig. 5.1 (a) Feedback system, (b) poles of a certain oscillator in steady state, (c) its Nyquist plot.

$$L(\Delta\omega) \propto \frac{1}{Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{5.6}$$

at moderate frequency offset. At very small offset, phase noise drops faster due to some complex effects, presenting a steeper falling in this region. Figure 5.2 reveals a general phase noise spectrum.

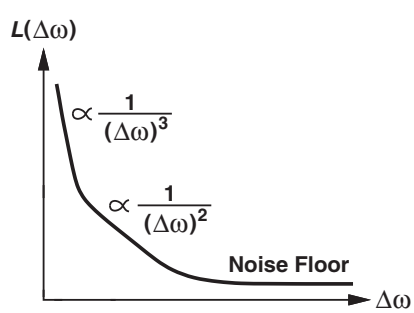


Fig. 5.2 Typical phase noise plot.

A popular figure of merit (FOM) for oscillators summarizes the important performance parameters, i.e., phase noise and power consumption P, to make a fair comparison:

$$\mathrm{FOM} = L(\Delta\omega) + 10\log_{10}\left(\frac{\Delta\omega}{\omega_0}\right)^2 + 10\log_{10}\left(\frac{P}{1\mathrm{mW}}\right). \tag{5.7}$$

The second term is to neutralize the effect of offset in $L(\Delta\omega)$ while taking the center frequency into account. The power consumption is calculated as dBm such that the unit of FOM remains the same as that of $L(\Delta\omega)$. For example, for a 40-GHz VCO with phase noise of -90 dBc/Hz while consuming 1 mW, the FOM is equal to -182 dBc/Hz.

5.2 Cross-Coupled Oscillators

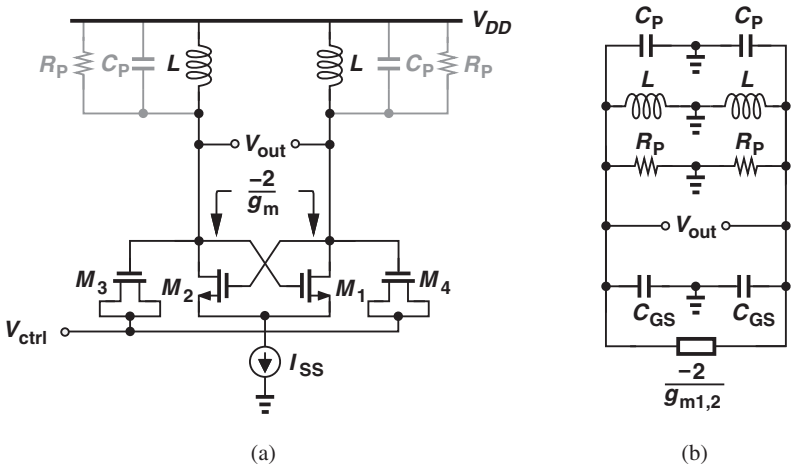
LC-tank VCOs are probably the most pervasive ones in high-speed systems, providing numerous merits that satisfy the requirements of different applications. The simple yet symmetric configuration facilitates high-speed and differential designs with large swing, reasonable tuning range, and low power consumption. The plain structure also allows low-supply operation, even below 1 V. Depending on the inductor Q, the cross-coupled oscillators can achieve sufficiently low phase noise for most applications. We begin our discussion with the fundamental properties.

A typical realization of cross-coupled VCOs can be found in Fig. 5.3(a), where the pair M_1-M_2 provides negative resistance $-2/g_{m1,2}$ (differentially) to compensate for the inductor loss R_P. At resonance, these two resistances cancel each other and the oscillation frequency is given by

$$\omega_{osc} = \frac{1}{\sqrt{LC_P}}, \tag{5.8}$$

where L and C_P denote the loading inductor and parasitic capacitance at output nodes, respectively, and M_3-M_4 the MOS varactors. Barkhausen criteria imply that we must have $g_{m1,2} \geq (1/R_P)$ to make the circuit oscillate, while practical design would choose a higher value (≈ 3) to ensure oscillation over PVT variations.

It is instructive to derive an alternative expression for ω_{osc} with simplified conditions to examine what factors actually limit the operation frequency. Modeling the VCO as Fig. 5.3(b), we obtain R_P and ω_{osc} in stable oscillation as



(a) (b)

Fig. 5.3 (a) Typical LC oscillator with cross-coupled pair providing negative resistance, (b) its equivalent model with varactors neglected.

$$R_P = Q \cdot \omega_{osc} L = \frac{1}{g_{m1,2}} \tag{5.9}$$

$$\omega_{osc} = \frac{1}{\sqrt{2L(\frac{C_P}{2} + \frac{C_{GS}}{2})}}, \tag{5.10}$$

where Q represents the quality factor of the tank, and C_{GS} the average gate-source capacitance contributed by $M_{1,2}$. Here, we take off the varactors for simplicity. If C_P is negligible as compared with C_{GS} (which is basically true at high frequencies), we arrive at

$$\omega_{osc} \approx \frac{1}{\sqrt{LC_{GS}}} \tag{5.11}$$

$$= \frac{1}{\sqrt{\frac{1}{g_m Q \omega_{osc}} C_{GS}}} \tag{5.12}$$

$$= \sqrt{Q \omega_T \omega_{osc}}, \tag{5.13}$$

where ω_T denotes the transit frequency of $M_{1,2}$. It follows that

$$\omega_{osc} = Q \cdot \omega_T. \tag{5.14}$$

In other words, a cross-coupled oscillator can operate at very high frequencies, given that the inductors provide a sufficiently high Q. In reality, however, several issues discourage ultra high-speed oscillation: (1) the on-chip inductors usually have a self-resonance frequency (f_{SR}) of only a few hundred GHz; (2) the varactors present significant loss at high frequencies, and it could eventually dominate the Q of the tank; (3) even (2) is not a concern, the on-chip inductors can never reach a very high Q due to the physical limitations; (4) C_P may not be negligible in comparison with other parasitics. Nonetheless, cross-coupled VCOs are still expected to operate at frequencies close to device f_T. For example, 50- and 96- and 140-GHz realizations[1] have been reported in 0.25-μm, 0.13-μm, and 90-nm CMOS technologies [2][3][4]. The final example illustrates oscillation above f_T.

It is important to know that, if the varactor's capacitance is much greater than other parasitics, the tuning range of an LC VCO approaches a constant and has nothing to do with the inductance. Figure. 5.4 illustrates such an effect. On the other hand,

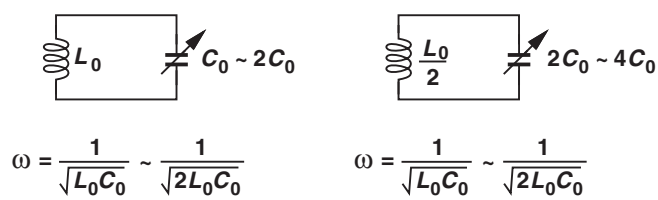


Fig. 5.4 Two LC networks with equal resonance frequency and tuning range. (The varactors are assumed to have 100% variation.)

lowering the inductance leads to smaller swing and puts the oscillator in danger of failing unless the current is increased (assuming that $R_P = Q\omega_0 L$ decreases). Consequently, it is always desirable to use inductors as large as possible.

Several techniques have been developed to improve the performance of LC oscillators. Figure 5.5(a) shows a popular topology moving the tail current to the top to setup the output common-mode around $V_{DD}/2$. The noise of the top current source may disturb the voltage at node P and hence modulate the frequency, resulting in higher phase noise. Figure 5.5(b) incorporates PMOS devices, but the oscillation frequency (or tuning range) degrades due to the extra parasitic capacitance. Note that the tail current plays important role here, because it defines the bias current (and hence the output amplitude if the inductor Q is known) while giving a high impedance to ground so as to maintain a more constant quality factor for oscillation. The tail current in Fig. 5.5(a) and (b) can be removed to accommodate low-supply operation but at a cost of higher supply sensitivity. An approach preserving these merits while eliminating its noise contribution is illustrated in Fig. 5.5(c). A large bypass capacitor C_p absorbs the noise of the current source M_1. With the L_s-C_s network resonating at twice the output frequency, the common-source node P still experiences a high

[1] Here we consider only the fundamental frequency.

impedance to ground. Differential voltage control is also achievable by adding two sets of varactors with opposite direction, as illustrated in Fig. 5.5(c). The differential operation improves the common-mode rejection by 10-20 dB.

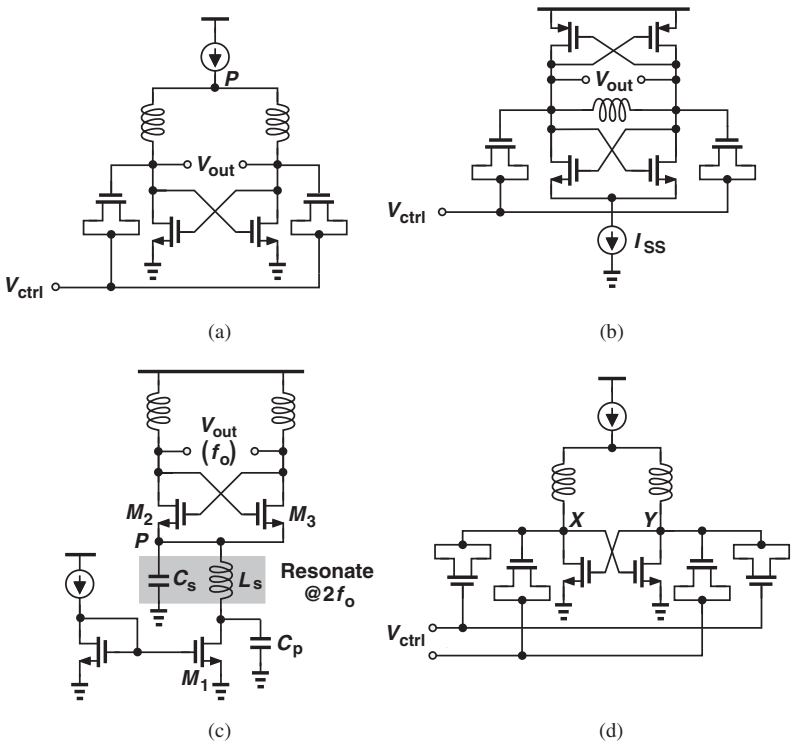


Fig. 5.5 LC VCO modification with (a) top biasing, (b) dual pairs, (c) differential control.

Inductors can also be improved by changing the physical shapes. One useful modification for differential circuit is to wrap the spiral symmetrically [Fig. 5.6(a)]. Due to the differential operation, the effective substrate loss is reduced by a factor of 2, leading to a higher Q. The only side effect is that the spacing between turns needs to be wider so as to minimize the interwinding capacitance. Vertical stacking is another useful technique to shrink the occupied area for a given inductance [Fig. 5.6(b)]. Depending on the mutual coupling factor, the inductance of a two-layer structure is around $3.5 \sim 4$ times larger than that of a single layer one with the same area. Note that the two layers should be kept as far as possible in order to maximize the self-resonance frequency. A method combining these two techniques is depicted in Fig. 5.6(c). Recognized as a differentially-stacked inductor, it preserves the benefits from both structures. More details can be found in [5][6][7].

A few techniques are commonly-used to extend the tuning range. A straightforward method is to employ a capacitor array (preferably binary-weighted for better

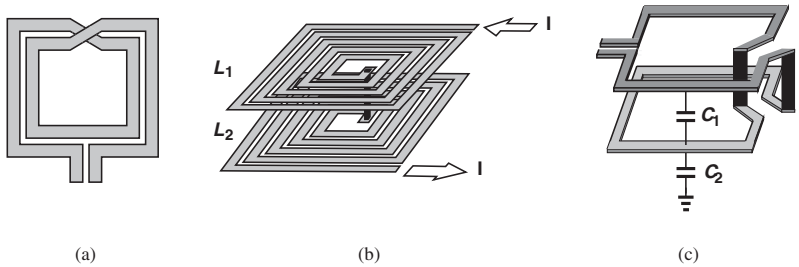


Fig. 5.6 (a) Differential inductor, (b) stacked inductor, (c) differentially-stacked inductor.

efficiency) to tune the VCO coarsely [Fig. 5.7(a)][8]. Such a band selection mechanism sometimes benefits the PLL design because the VCO gain becomes smaller. Similar approach can be applied to inductors. Figure 5.7(b) shows an example where segmented inductors with switches accomplish the digital tuning [9]. Another interesting realization of variable inductors is depicted in Fig. 5.7(c), where the auxiliary inductor L_2 is tuned gradually by means of $M_{3,4}$ and V_{ctrl}. Nevertheless, all of the

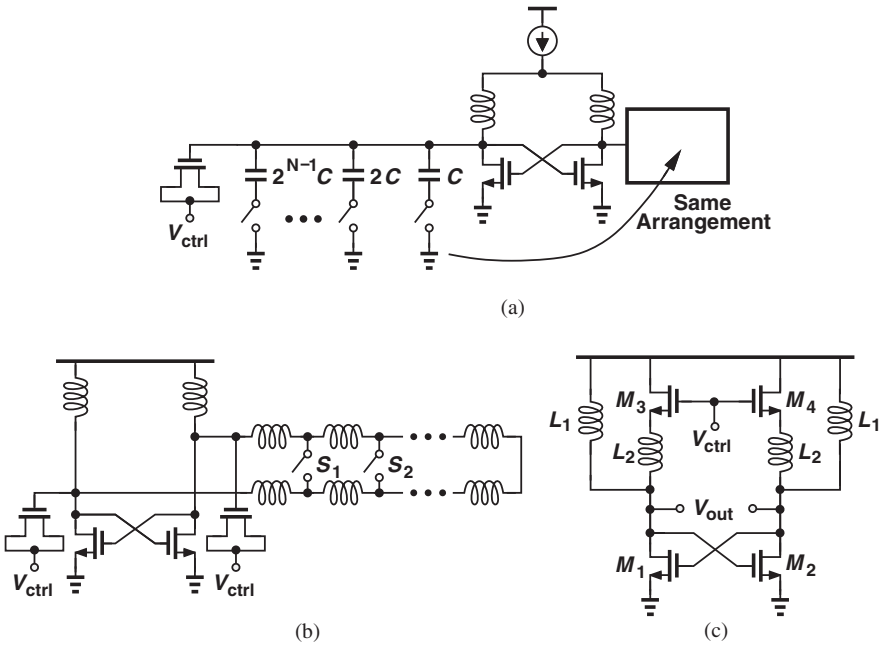


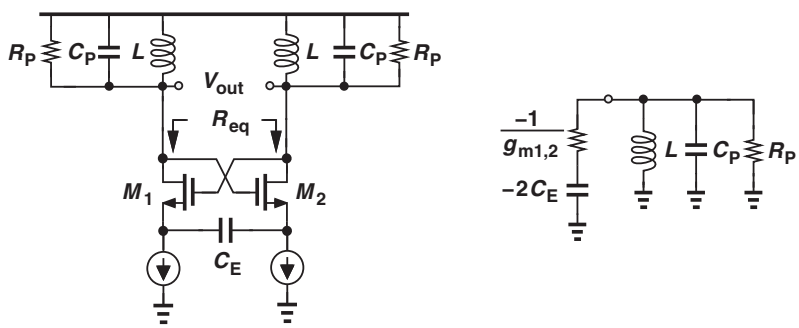
Fig. 5.7 Methods to enlarge the tuning range using (a) Capacitor array, (b) switching inductors, (c) auxiliary inductors.

circuits in Fig. 5.7 suffer from degradation on the tank Q (and hence the phase noise) because of the finite resistance of the MOS switches.

It is noteworthy that the basic cross-coupled oscillators are very efficient, and careless modification of the structure can lead to unpredictable results. One example using capacitive degeneration is illustrated in Fig. 5.8(a). Like a relaxation oscillator, the impedance seen looking into the cross-coupled pair is given by

$$R_{eq} = -\frac{2}{g_{m1,2}} - \frac{1}{sC_E}, \tag{5.15}$$

and the equivalent small-signal model is shown in Fig. 5.8(b). Intuitively, such a



(a) (b)

Fig. 5.8 Cross-coupled VCO with capacitive degeneration.

degeneration provides a negative capacitor to cancel out part of the positive capacitor C_P, raising the oscillation frequency. In reality, however, this frequency boosting is accomplished at a cost of weakening the negative resistance, making the circuit harder to oscillate. To see why, let us first consider a general transformation between series and parallel networks. As shown in Fig. 5.9(a), a series circuit containing R_1 and C_1 can be converted to a parallel one by equating the impedance. Defining Q_d as $1/(R_1C_1\omega)$, we arrive at

$$\frac{R_2}{R_1} = 1 + Q_d^2 \tag{5.16}$$

$$\frac{C_2}{C_1} = \frac{Q_d^2}{1+Q_d^2} \tag{5.17}$$

where R_2 and C_2 are of the equivalent parallel combination. Figure 5.9(b) plots R_2 and C_2 as a function of Q_d. Obviously, depending on Q_d, the transformed network behaves differently. For $Q_d \gg 1$, $C_2 \approx C_1$ and $R_2 \approx Q_d^2 R_1$; whereas for lower Q_d, both R_2 and C_2 degrade.

Applying this result into Fig. 5.8(b), we arrive at the small-signal model in Fig. 5.10. The resonance frequency now becomes

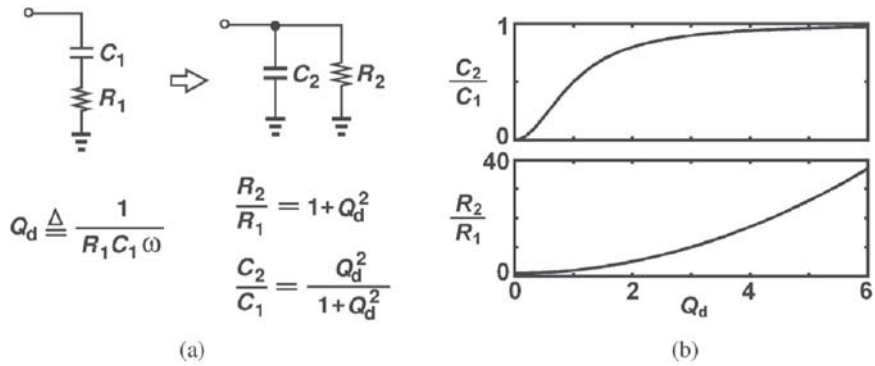


Fig. 5.9 Conversion between series and parallel RC networks.

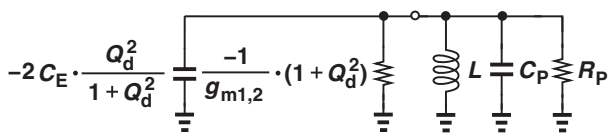


Fig. 5.10 Modification of Fig.5.8(b).

$$\omega_{osc} = \frac{1}{\sqrt{L(C_P - 2C_E \cdot \frac{Q_d^2}{1+Q_d^2})}}. \tag{5.18}$$

Although degraded, it is indeed a boost in the frequency. However, a more difficult condition is imposed on the start-up oscillation:

$$g_{m1,2} \geq \frac{1+Q_d^2}{R_P}. \tag{5.19}$$

For a Q_d of 3, this circuit needs a transconductance 10 times larger in order to ignite (and maintain) the oscillation. As a result, wider devices may be required to implement $M_{1,2}$, leading to less improvement or even deterioration in oscillation frequency. The circuit may consume more power as well.

5.3 Colpitts Oscillator

Another important VCO topology that has been widely used in high-speed systems is Colpitts oscillator. First proposed in 1920's [10], this type of oscillator could be operated with only one transistor. In modern times, the abundance of transistors and the desire for differential circuits favors a symmetric Colpitts oscillators.

A Colpitts VCO can be easily understood by examining a resonating circuit shown in Fig. 5.11(a), where an inductor is sitting across the drain and gate of a MOS with two capacitors C_1 and C_2 connected to these nodes. In order to oscillate, the signal in the feedback path through the C-L-C network must satisfy Barkhausen criteria. Breaking the loop and exciting it with an input V_1 [Fig. 5.11(b)], we obtain the loop

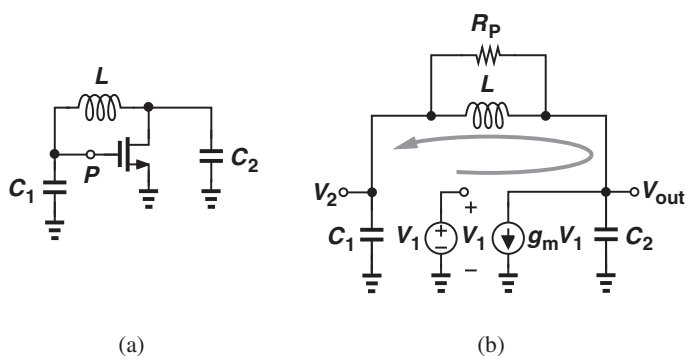


Fig. 5.11 (a) Colpitts oscillator, (b) its linear model with feedback broken at node P.

gain as

$$\frac{V_2}{V_1}(s) = -g_m \cdot \frac{R_P + sL}{s^3 LC_1C_2R_P + s^2L(C_1+C_2) + sR_P(C_1+C_2)}. \tag{5.20}$$

To make the oscillation happen at a frequency ω_{osc}, we have $|V_2/V_1| \geq 1$ and $\angle(V_2/V_1) = 0°$. In other words, at $\omega = \omega_{osc}$, the ratio of the real and imaginary parts of the numerator must be equal to that of the denominator:

$$\frac{R_P}{\omega_{osc}L} = \frac{-\omega_{osc}^2 L(C_1+C_2)}{\omega_{osc}R_P(C_1+C_2) - \omega_{osc}^3 LR_pC_1C_2}. \tag{5.21}$$

It follows that

$$\omega_{osc} = \frac{1}{\sqrt{\frac{LC_1C_2}{C_1+C_2}}} \cdot \sqrt{1+\frac{1}{Q^2}} \approx \sqrt{\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)}. \tag{5.22}$$

Here, Q denotes the quality factor of the inductor and $R_P = \omega_0 LQ$. The loop gain requirement yields

$$\left|\frac{V_2}{V_1}\right|(j\omega_{osc}) = \frac{g_m R_P}{\omega_{osc}^2 L(C_1+C_2)} \geq 1. \tag{5.23}$$

As a result, we have the following condition for oscillation:

$$g_m R_P \geq \frac{(C_1+C_2)^2}{C_1C_2} \geq 4. \tag{5.24}$$

An alternative explanation of a Colpitts oscillator is to investigate the impedance seen looking into the gate-drain port of such a circuit [Fig. 5.12(a)]. It can be shown that R_{eq} is given by

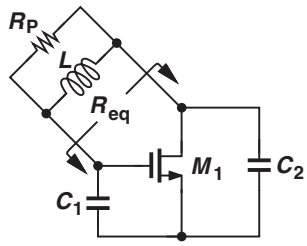
$$R_{eq} = \frac{g_m}{C_1C_2s^2} + \frac{1}{C_2s} + \frac{1}{C_1s}, \tag{5.25}$$

which is equivalent to a negative resistance $-g_m/(C_1C_2\omega^2)$ in series with a capacitor $C_1C_2/(C_1+C_2)$. If the quality factor of this RC network is high, we can approximate it as a parallel combination as shown in Fig. 5.12(b). Obviously the circuit may oscillate if the negative resistance is strong enough to cancel out the inductor loss R_P. As expected, the oscillation frequency is equal to

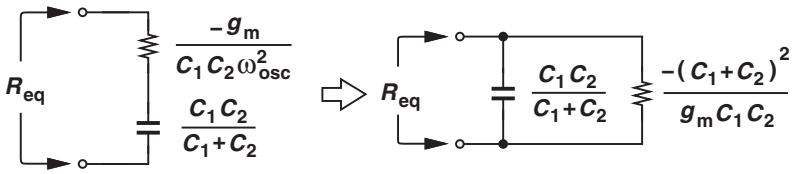
$$\omega_{osc} = \sqrt{\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)}, \tag{5.26}$$

same result as Eq. (5.22). Equation. (5.24) can be obtained with a similar approach.

Depending on the bias, the prototype in Fig. 5.12(a) provides three topologies of Colpitts oscillators, as shown in Fig. 5.13 [11]. Among them, Fig. 5.13(a) reveals the greatest potential for high-speed operation, since C_1 can be realized by the intrinsic capacitance C_{GS} of M_1. The capacitor C_2 is replaced by a varactor M_2 to accomplish the frequency tuning. At resonance, all the components oscillate at the same frequency ω_{osc}, including the drain current of M_1. That allows us to place a loading R_D at drain and take the voltage output from this node. Inductive peaking could be an option here if the output needs to drive large capacitance. Figure 5.13(b) provides another



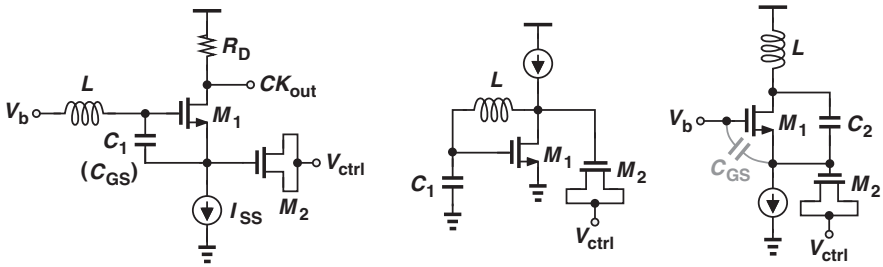
(a)



(b)

Fig. 5.12 Alternative approach to analyze Colpitts oscillators by examining the equivalent impedance.

structure with C_2 connecting to the source and drain of M_1. The parasitic capacitance C_{GS} would limit the oscillation frequency or equivalently the tuning range, making this topology less attractive. The structure in Fig. 5.13(c) requires L to be floating at both ends, presenting more parasitic to the circuit. For this reason, the topology in Fig. 5.13(c) is rarely used.



(a) (b) (c)

Fig. 5.13 Three realizations of Colpitts oscillator, (a) common-drain, (b) common-source, (c) common-gate.

Despite many advantages, the circuit in Fig. 5.13(a) still suffers from two drawbacks: the single-ended operation makes the oscillator vulnerable to supply noise,

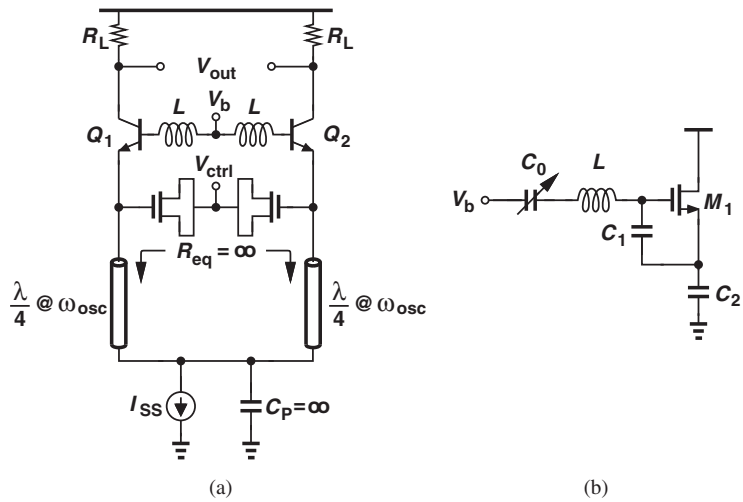


Fig. 5.14 (a) Differential Colpitts oscillator, (b) Clapp oscillator.

and the capacitance contributed by the tail current source degrades the oscillation frequency. To remedy these issues, we usually implement the Colpitts oscillator as a differential configuration with $\lambda/4$-lines between $Q_{1,2}$ and I_{SS}. Figure 5.14(a) illustrates such a realization. The combined bias points of the symmetric circuit facilitate differential operation, and $\lambda/4$-transmission lines make the equivalent impedance looking down (R_{eq}) become infinity.[2] Colpitts VCOs operating at 60 GHz and beyond with silicon compound technologies have been reported extensively [12][13][14]. In fact, the current source can be replaced with a "choke" inductor, or a sufficiently large inductor such that the impedance to ground is dominated by the capacitance for proper feedback. A Colpitts oscillator taking this approach is presented in [15], which demonstrates 104 GHz operation in a 90-nm CMOS technology.

The circuit in Fig. 5.13(a) tunes the frequency at the risk of losing stability or failing the oscillation. According to Eq. (5.24), $g_m R_p$ must be greater than $(C_1 + C_2)^2/(C_1 C_2)$, which varies as the control voltage changes. To guarantee safe margin for oscillation, one can introduce another capacitor C_0 (which is variable) in series with L and level C_1 and C_2 fixed as depicted in Fig. 5.14(b). The oscillation frequency therefore becomes

$$\omega_{osc} = \sqrt{\frac{1}{L}\left(\frac{1}{C_0} + \frac{1}{C_1} + \frac{1}{C_2}\right)}. \tag{5.27}$$

Also known as "Clapp oscillator" , this circuit inevitably suffers from less tuning range.

[2] Here we assume a very large bypass capacitor C_P is used. Line length other than $\lambda/4$ could be chosen for finite C_P.

One important application of Colpitts oscillators is the so-called "Pierce oscillator" . As shown in Fig. 5.15, it incorporates a piezoelectric crystal (serving as an inductor) and two capacitors C_1 and C_2 to form a Colpitts oscillator. Here. the crystal

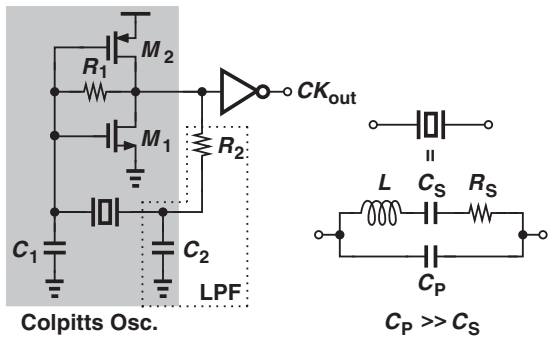


Fig. 5.15 Example of Pierce oscillator.

can be modeled as a series RLC network (i.e., L, C_S and R_S) in parallel with another capacitor C_P and $C_P \gg C_S$. Similar to M_1 in Fig. 5.12(a), the inverter-like amplifier M_1 and M_2 provides negative resistance to compensate for the loss. Note that the circuit is self-biased through R_1 such that both M_1 and M_2 are in saturation. The reader can easily prove that the oscillation frequency is equal to

$$\omega_{osc} \approx \frac{1}{\sqrt{LC_S}}, \tag{5.28}$$

which is an unchangeable value for a given crystal. To increase oscillation stability, R_2 can be added in the loop to dampen the higher order harmonics. Such a crystal-based oscillator achieves marvelous frequency stability in the presence of temperature variation, and is extensively used as a reference clock in various applications.

5.4 Other Topologies

In addition to the cross-coupled and Colpitts oscillators, many other VCO topologies have been proposed to achieve high-speed operation. We look at some representative structures in this section.

5.4.1 mm-Wave Oscillators

Similar to Colpitts VCOs, mm-wave oscillators can also create periodic signals with only one active device. The approach of a mm-wave oscillator is illustrated in Fig.

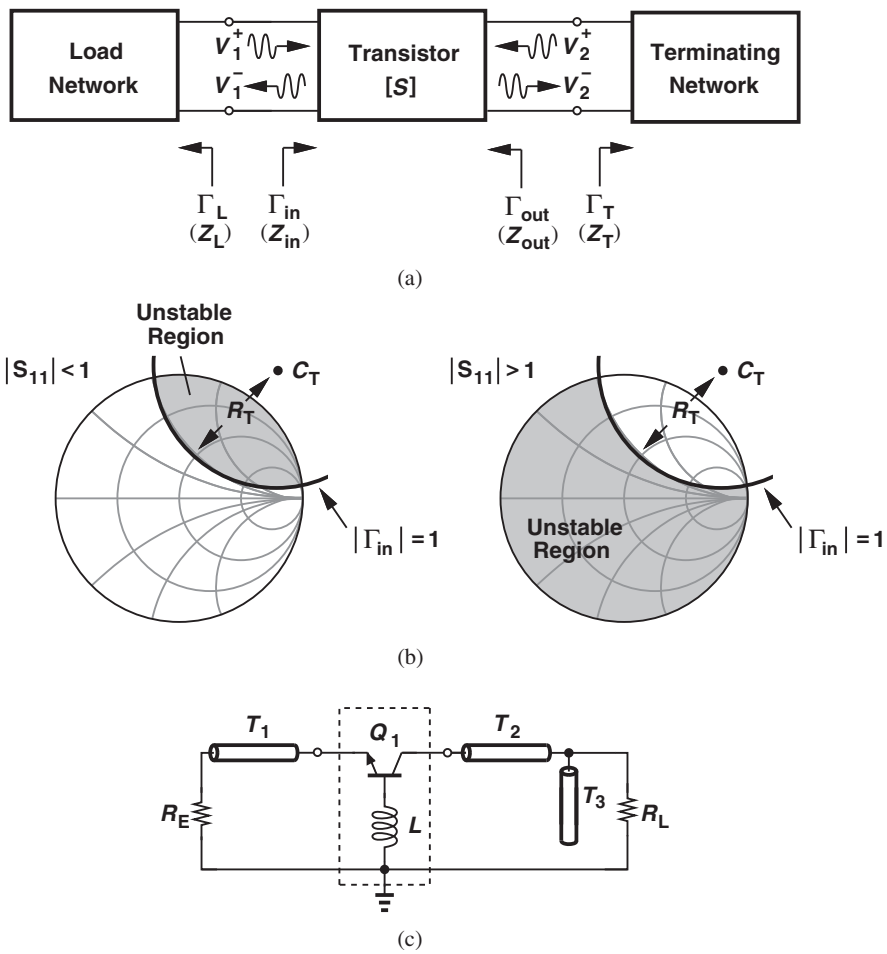


Fig. 5.16 (a)Design of mm-wave oscillators, (b)Smith chart for determining Γ_T, (c)example of mm-wave oscillators.

5.16, where Γ_L, Γ_{in}, Γ_{out}, and Γ_T denote the corresponding reflection coefficients. In order to make the circuit oscillate, we need to build up a device which becomes highly unstable in the vicinity of the desired frequency. It is clear that

$$\Gamma_{\rm in} = \frac{V_1^-}{V_1^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_{\rm T}}{1 - S_{22}\Gamma_{\rm T}}, \tag{5.29}$$

and oscillation would occur only if the input impedance Z_{in} possesses negative real part. Assuming all the connections are implemented as 50-Ω transmission lines, we have $|\Gamma_{\rm in}| > 1$ and the boundary condition $|\Gamma_{\rm in}| = 1$ can be further derived to correlate with $\Gamma_{\rm T}$. It can be shown that [16]

$$|\Gamma_{\rm T} - C_T| = R_T, \tag{5.30}$$

where

$$C_T = \frac{(S_{22} - \triangle S_{11}^*)^*}{|S_{22}|^2 - |\triangle|^2} \tag{5.31}$$

$$R_T = \left| \frac{S_{12} - S_{21}}{|S_{22}|^2 - |\triangle|^2} \right|, \tag{5.32}$$

and $\triangle$ represents the determinant of the scattering matrix:

$$\triangle = S_{11}S_{22} - S_{12}S_{21}. \tag{5.33}$$

The selection of $\Gamma_{\rm T}$ for different $|S_{11}|$ conditions is illustrated in Fig. 5.16(b). For $|S_{11}| < 1$, the unstable region is the inside region of the $|\Gamma_{\rm in}| = 1$ circle that intersects the Smith chart, whereas for $|S_{11}| > 1$ it is the whole Smith chart outside the $|\Gamma_{\rm in}| = 1$ circle. $\Gamma_{\rm T}$ must locate in the unstable region in order to oscillate. In mm-wave oscillator design, common-source or common-gate devices with positive feedback are often incorporated. After the transistor configuration is selected, the $|\Gamma_{\rm in}| = 1$ circle becomes readily available and $\Gamma_{\rm T}$ can be properly chosen to produce a large negative resistance at the input of the transistor. The load impedance Z_L needs to match Z_{in} as well. Typical design would require a $3\times$ margin (i.e., $R_L = -R_{in}/3$) to secure oscillation. The imaginary matching $X_L = -X_{in}$ determines the oscillation frequency. Figure 5.16(c) depicts a design example. Hence, Q_1-L network serves as a two-port and matching techniques are employed. With a good matching, the output could deliver a high power. Due to the simplicity, the mm-wave oscillator can operate at high frequency as well. The reader can refer to [16] for more details.

The major drawback of this circuit is the difficulty of frequency tuning. The length and characteristic impedance of a transmission line are almost inalterable because of physical limitation and matching requirements. Single-ended operation is another minus. The reader can see that a differential mm-wave oscillator resembles the Colpitts VCO [e.g., Fig. 5.14(a)] in many aspects.

5.4.2 Push-Push Oscillators

One important application of $\lambda/4$ transmission line technique is the push-push oscillators. As suggested by its name, this type of oscillator takes the 2nd-order harmonic from the common-mode node, and amplifies it properly as an output. Note that second-order harmonic is generated by the nonlinearity of the circuit, which manifests itself in large-signal operation. Figure 5.17 reveals an example, where V_P needs

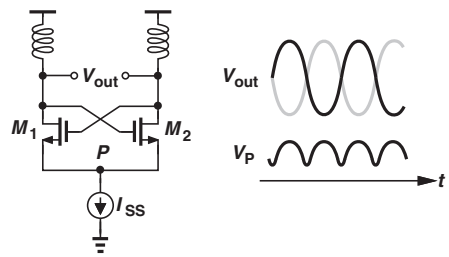


Fig. 5.17 Generation of 2nd-order harmonic.

to swing up and down at twice the fundamental frequency so as to maintain a constant I_{SS}. Similar to a frequency doubler, the desired harmonic can be extracted while the others are suppressed.

Since node P suffers from large parasitic capacitance, we usually resort to other common-mode points to obtain the output. Two examples of circuit-level realization based on cross-coupled and Colpitts structures are illustrated in Fig. 5.18. The $\lambda/4$ lines in both cases reinforce the $2\omega_{osc}$ signal by providing an equivalent open at node P when looking into it, and the output power could be quite large if proper matching

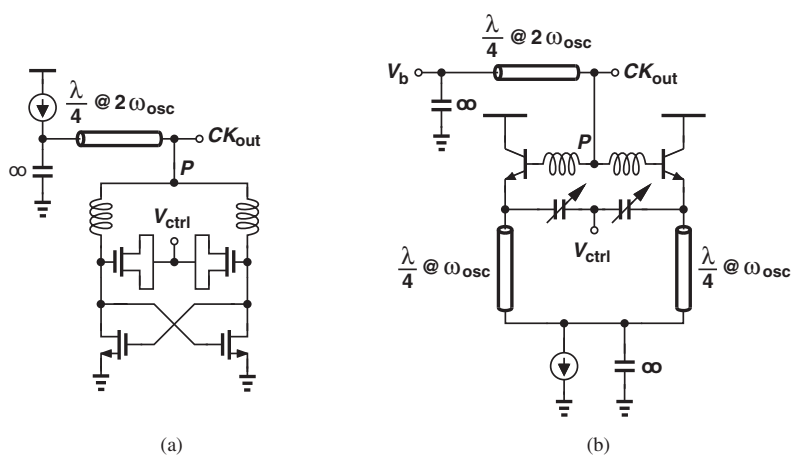


Fig. 5.18 Push-push VCOs based on (a) cross-coupled, (b) Colpitts topologies.

is achieved. Compared with typical frequency doublers, this topology consumes less power and area, resulting in a more efficient approach. More details are described in [17][18].

The push-push oscillator can only provide a single-ended output. In addition, tuning the fundamental frequency could result in a mismatch in the $\lambda/4$ lines, potentially leading to lower output power.

5.4.3 Distributed Oscillators

Another distinctive VCO topology shooting for high-speed operation is the distributed oscillator. As shown in Fig. 5.19, the output of a distributed amplifier is returned back to the input, yielding wave circulation along the loop. Oscillation is therefore obtained at any point along the transmission line. Here, the transmission line loss is

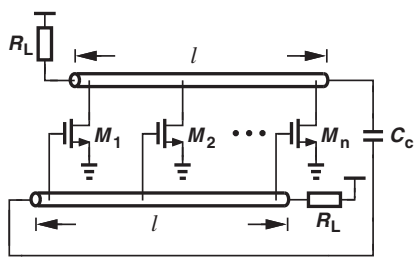


Fig. 5.19 Distributed oscillator.

overcome by the gain generated along the line. To be more specific, we assume the two propagation lines in Fig. 5.19 to be identical, i.e., the characteristic impedances, group velocities, and physical lengths are the same. The oscillation period under such circumstances is nothing more than twice the propagation time along the length l:

$$f_{osc} = \frac{1}{2l\sqrt{L_0 C_0}} \tag{5.34}$$

where L_0, C_0 denote the equivalent inductance and capacitance (with the MOS capacitance included) per unit length. It can be shown that the oscillation frequency is commensurate with the device f_T[8].

While looking attractive, the distributed oscillator suffers from a number of drawbacks: (1) the group velocities along the two lines may deviate from each other due to the difference between the gate and drain capacitance; (2) the circuit would need larger area and higher power dissipation, (3) the frequency tuning could be difficult. The third point becomes clear if we realize that adding any varactors to the lines can

cause significant degradation on the oscillation frequency and the quality factor Q. Varying the bias voltage of the transistors may change the intrinsic parasitics (and therefore the oscillation frequency) to some extent, but the imbalanced swing and the mismatch between the lines could make things worse. The circuit may even stop oscillating in case of serious deviation. Note that placing a "short-cut" on the lines by steering the current of two adjacent transistors is plausible as well [19]: it is hard to guarantee that the wave still propagates appropriately along the lines while both devices are partially on.

A modification of distributed oscillators can be found if we terminate a transmission line by itself. The circuit is based on the concept of the differential stimulus of a closed-loop transmission line at evenly-spaced points, as illustrated conceptually in Fig. 5.20(a). In contrast to regular distributed oscillators, the transmission line requires no termination resistors, lowering phase noise and enlarging voltage swings. The circuit can be approximated by lumped inductors and capacitors, and one example is shown in Fig. 5.20(b). Here, eight inductors form a loop with four differential negative-Gm cells driving diagonally opposite nodes. In steady state, the eight nodes are equally separated by 45°, providing multiphase output if necessary.

The oscillation frequency of the circuit is uniquely given by the travel time of the wave around the loop. We write the oscillation frequency of this topology as

$$f = \frac{1}{8\sqrt{LC}} \tag{5.35}$$

where L and C, respectively, denote the lumped inductance and capacitance of each of the eight sections. The circuit can be further modified as shown in Fig. 5.20(c) to avoid long routing, and the negative-Gm cell can be simply implemented as Fig. 5.20(d). The PMOS transistors help to shape the rising and falling edges while providing lower $1/f$ noise.

One interesting issue in such a VCO is that, due to symmetry, the wave may propagate clockwise rather than counterclockwise. To achieve a more robust design, a means of detecting the wave direction is necessary. Since nodes that are 90° apart in one case exhibit a phase difference of $-90°$ in the other case, a flipflop sensing such nodes generates a constant high or low level, thereby providing a dc quantity indicating the wave direction. Other approach to avoid direction ambiguity can be found in [20].

5.5 Considerations of Dividers

Frequency dividers are also of great concern in communication systems. A good divider must provide correct frequency division over the whole band of interest while contributing negligible noise. At frequency above 10 GHz, designers begin to face a

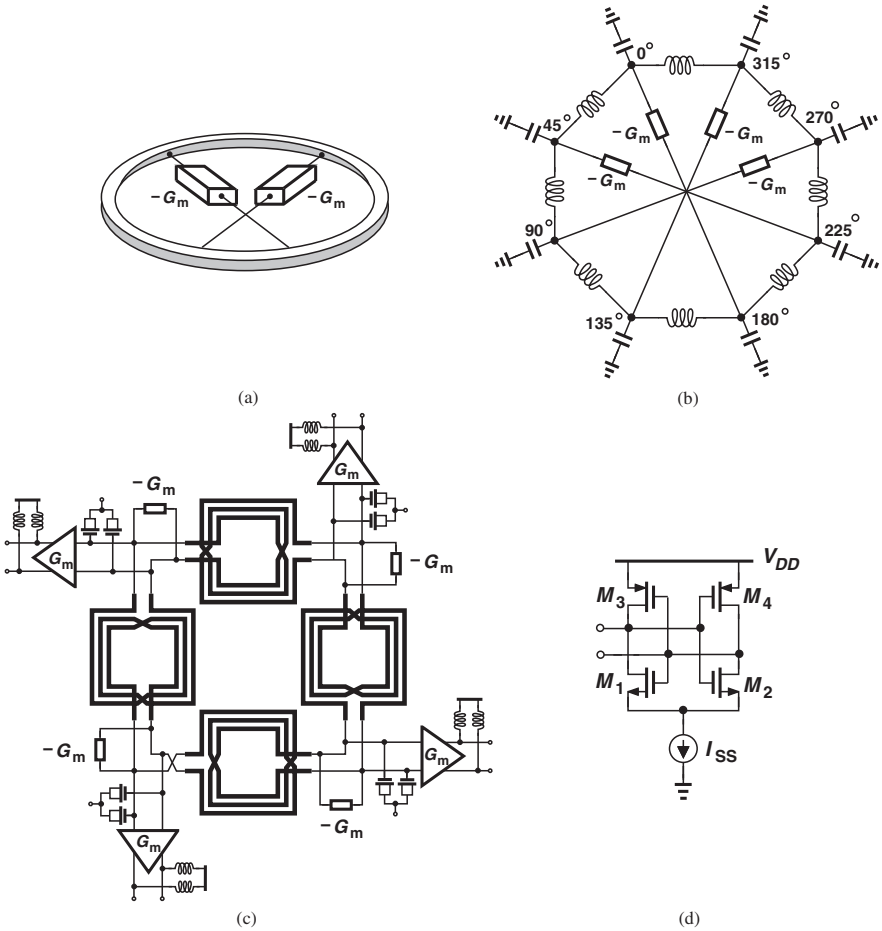


Fig. 5.20 (a) Oscillator based on closed-loop transmission line, (b) half-quadrature realization, (c) modification of (b), (d) implementation of $-Gm$ cell.

tradeoff between the input frequency and operation range. Generally speaking, the injection-locked dividers achieves the highest operation frequency due to the simplest structure while providing the narrowest locking range. Static dividers reveal a relatively wide range of operation but only for low frequencies. Regenerative dividers, also known as Miller dividers, act as a compromise between the two. Figure 5.21 plots the simulated operation ranges for three dividers targeting 80, 40 and 20 GHz with injection-locked, Miller and static topologies. The three curves can be roughly aligned (as the bold dash line), suggesting a direct tradeoff between the input frequency and the operation range since the product of the two is approximately a constant.

The noise induced by the dividers directly affects the overall signal purity. An easy way to examine how much the overall performance degradation is to check the output spectrum: for an ideal divider chain with total modulus of N, the output

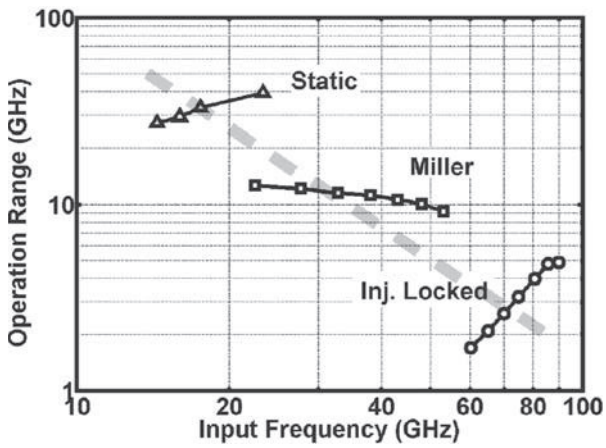


Fig. 5.21 Simulated operation ranges of 3 dividers in 90-nm CMOS.

spectrum should be approximately $20\log_{10} N$ dB lower than that of the input. Power consumption is another important parameters. In a PLL, for example, the power dissipated by the first few dividers begins to dominate the overall power consumption as the operation frequency approaches 10 GHz. We analyze the three topologies in detail in the following sections.

5.6 Static Dividers

Frequency division of a periodic signal could be achieved in different ways. One of the simplest $\div 2$ realizations is to place an edge-triggered flipflop (composed of two latches) in a negative feedback loop, as illustrated in Fig. 5.22(a). Differentially driven by the input clock, the two latches provide quadrature outputs running at half the input frequency[3] [Figure 5.22(b)]. Since the stored information can be held in the latches forever, the static frequency dividers can theoretically operate at arbitrarily low frequencies. Such a simple yet robust configuration manifests itself in low to moderate speed applications.

Although almost any type of latch can be adopted in a static divider, tradeoffs exist among bandwidth, power, robustness and signal integrity. For pure digital implementations such as C^2MOS or TSPC latches, the stacking of devices as well as the

[3] $CK_{out,I}$ and $CK_{out,Q}$ are separated by exactly 90° if the two latches experience the same loading.

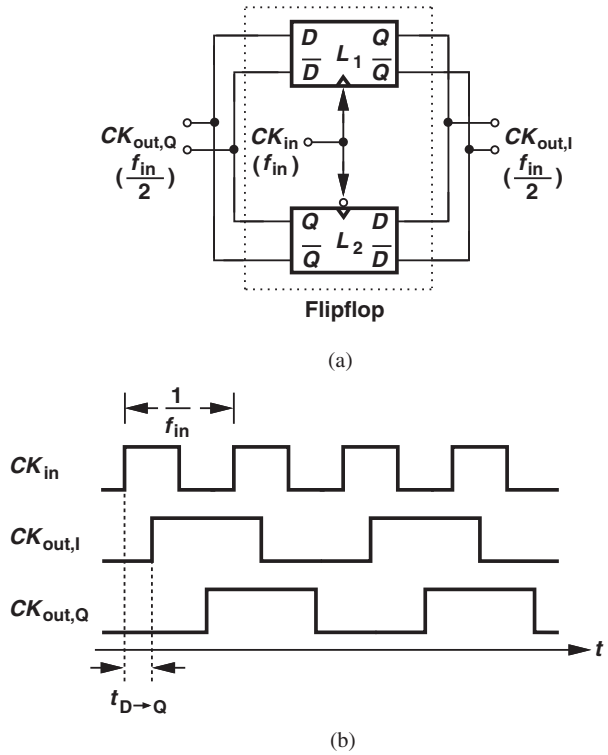


Fig. 5.22 (a) Typical static divider, (b) its waveforms.

rail-to-rail operation lead to long rising and falling times. The single-ended structure also suffers from supply noise coupling, potentially introducing jitter in the output. Meanwhile, the abrupt switching of the circuit would pull significant current from V_{DD} momentarily during transitions, which induces voltage bounce and perturbs the quiet analog region nearby. Even if supplies are separated, unwanted coupling can occur through the substrate or package. A better choice is to use current-mode logic (CML), and Fig. 5.23 depicts two examples for CMOS and bipolar realizations. Controlled by CK_{in} and $\overline{CK_{in}}$, it samples (amplifies) the input while $M_{1,2}$ ($Q_{1,2}$) pair is activated, and holds (regenerates) the data by means of the cross-coupled pair $M_{3,4}$ (Q_3-Q_6). The emitter followers (Q_5 and Q_6) in Fig. 5.23(b) serve as level shifters for Q_3 and Q_4. The constant tail current and differential operation alleviate a number of design issues.

Now let us consider the operation of a static divider with CML latches. At low frequencies, the latches lock the sampled data and wait until the next clock phase comes in. Apparently, the loop gain of the positive feedback (e.g., M_3-M_4 pair and R_D) must exceed unity, and the output looks like square wave under such a condition. As frequency goes up, the idle time decreases, and the divider would work properly as long as the input pair M_5-M_6 switches the current completely. Afterwards, the divider

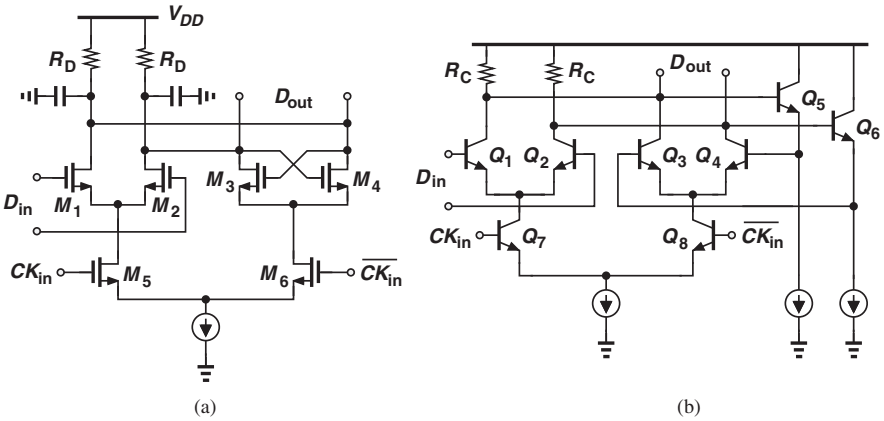


Fig. 5.23 CML latch of (a) CMOS, (b) bipolar technologies.

encounters a self-resonance frequency, where the divider operates as a two-stage ring oscillator. At this moment, the regenerative pairs provide sufficient hysteresis such that each latch contributes 90° of phase shift, and no input power is required. Beyond this frequency, the divider acts as a driven circuit again. It hits a limit as the frequency reaches the bandwidth of the circuit. That is, the D-to-Q delay of the latches ($t_{D\rightarrow Q}$) approaches half input cycle [1/($2f_{in}$)]. As can be clearly explained in Fig. 5.22(b), the timing sequence becomes out of order in such a circumstance, failing the division no matter how large the input power is. Figure 5.24(a) reveals the simulated input sensitivity (i.e., minimum required power) as a function of input frequency of a typical static divider in 90-nm CMOS technology.

It is worth noting that at very low speed, the CML-based static divider may not function properly if the input is sinusoidal. It is because the slow transition of CK_{in} and $\overline{CK_{in}}$ would turn on both latches simultaneously, making the loop transparent for a short period of time. As a result, "racing" phenomenon occurs, and the output toggles rapidly while CK_{in} and $\overline{CK_{in}}$ are transitioning. The simulated waveforms are demonstrated in Fig. 5.24(b). Here we operate the same divider with 20-MHz sinusoidal input, and the unwanted output switching is clearly observed in the inset. Fortunately, the low-speed inputs in most cases have sharp transitions (i.e., square-wave-like) to avoid such an incorrect operation.

It is always possible to extend the bandwidth by introducing inductive peaking or shrinking the size of the cross-coupled pair. However, the price to pay is the degradation of stability at low frequencies and the reduction of overall operation range.

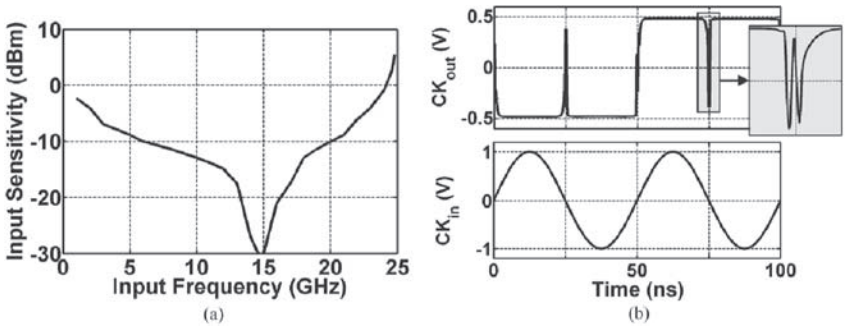


Fig. 5.24 (a) Simulated input sensitivity of a CML static divider in 90-nm CMOS, (b) erroneous switching caused by slow sinusoidal input.

5.7 Regenerative (Miller) Dividers

Originally proposed by Miller in 1939 [21], the regenerative divider is based on mixing the output with the input and applying the result to a low-pass filter (Fig. 5.25). Under proper phase and gain conditions, the component at $\omega_{in}/2$ survives and circulates around the loop, achieving $\div 2$ operation. Such a configuration allows joint design of the mixer and the low-pass filter to arrive at a high speed, since the device capacitance of the former can be absorbed as part of the latter. This topology thus becomes attractive and popular at moderate to high frequencies.

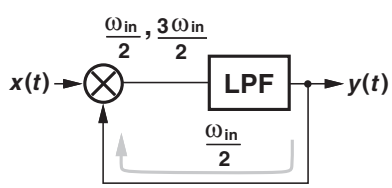


Fig. 5.25 Regenerative divider.

Let us first examine the division behavior and estimate the operation range. For the circuit to divide properly, the loop gain at $\omega_{in}/2$ must exceed unity. Redrawing the divider in Fig. 5.26(a) with simple RC filter and input amplitude A, we have

$$\frac{\beta A}{2}\left|H(j\frac{\omega_{in}}{2})\right| \geq 1, \tag{5.36}$$

where β denotes the conversion gain of the mixer. It can be further derived that

$$A \geq \frac{2}{\beta}\sqrt{1+\left(\frac{\omega_{in}}{2\omega_c}\right)^2} \geq \frac{2}{\beta}. \tag{5.37}$$

Here, the corner frequency $\omega_c = (R_1C_1)^{-1}$. Equation (5.37) implies that a minimum level of at least $2/\beta$ is required for the input. Unlike the static or the injection-locked dividers, the regenerative ones present no self-resonance frequency, resulting in a relatively flat input sensitivity.

Realizing that the LPF is to filter out the component at $3\omega_{in}/2$ and preserve that at $\omega_{in}/2$, we examine two cases to determine the operation range. As illustrated in

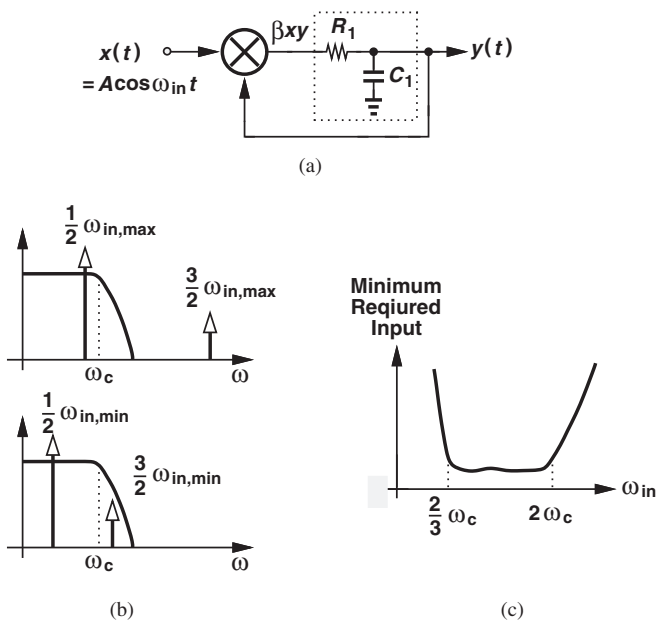


Fig. 5.26 (a) Regenerative divider with an RC filter, (b) operation range determination, (c) typical input sensitivity.

Fig. 5.26(b), the rule of thumb is to keep $\omega_{in}/2$ inside the passband while rejecting $3\omega_{in}/2$ and other harmonics. In other words, we can roughly estimate the operation range as

$$\frac{\omega_{in,max}}{2} \leq \omega_c \quad \text{and} \quad \frac{3\omega_{in,min}}{2} \geq \omega_c, \tag{5.38}$$

and hence

$$\frac{2\omega_c}{3} \leq \omega_{in} \leq 2\omega_c. \tag{5.39}$$

Figure 5.26(c) illustrates the sensitivity of a typical regenerative divider.

While providing an intuitive understanding of the circuit's behavior, the model in Fig. 5.26(a) fails to stipulate the condition for proper division. Neglecting nonlinearities in the mixer, we have

$$R_1C_1\frac{dy}{dt}+y=\beta yA\cos\omega_{in}t. \tag{5.40}$$

An explicit solution can be obtained as

$$y(t)=y(0)\exp\left(-\frac{t}{R_1C_1}+\frac{\beta A}{R_1C_1\omega_{in}}\sin\omega_{in}t\right). \tag{5.41}$$

That is, $y(t)$ decays to zero with a time constant of R_1C_1, i.e., the circuit fails to divide regardless of the ratio of ω_{in} and ω_c. Such a contradiction implies that the model in Fig. 5.26(a) is oversimplified. A more accurate model can be obtained by introducing a delay ΔT following the LPF to represent the broadband phase shift around the loop [Fig. 5.27(a)]. Indeed, as shown in Fig.5.27(b), a typical bipolar

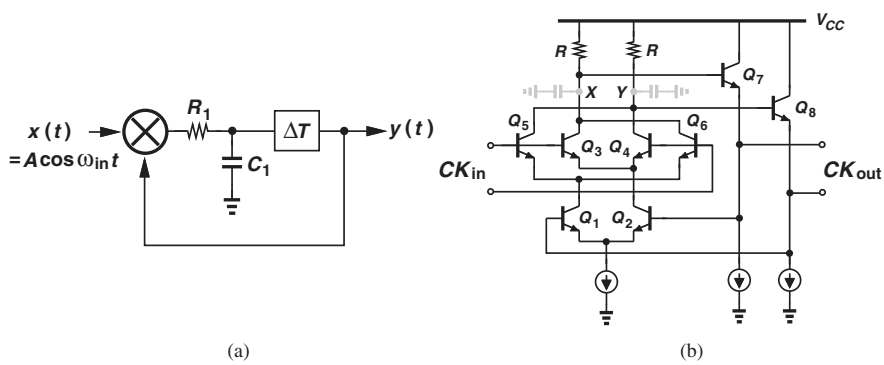


Fig. 5.27 (a) Modified Miller divider model, (b) bipolar realization.

implementation introduces delay at nodes X and Y through the emitter followers and at the collectors of Q_1 and Q_2. This delay is indispensable and almost all the bipolar Miller dividers belong to this topology.

However, the configuration of Fig. 5.27(b) is difficult to realize in CMOS technologies because the relatively low transconductance of CMOS devices arrives at a source follower with poor performance. It may consume substantial voltage headroom while attenuating the signal and discouraging the divider from high-speed operation. An alternative approach of Miller divider suitable for CMOS devices has been proposed by employing an LC tank (or equivalently, a bandpass filter) as the

load in the mixer [22]. Shown in Fig. 5.28(a), a bandpass filter replaces the low-pass one to suppress the higher-order harmonic. Again, the loop gain at ω_{in}/2 must be greater than unity. Following the same derivation for Eq. (5.37), we obtain the minimum input level necessary for correct division as

$$A \geq \frac{2}{\beta}\sqrt{1+\frac{\left(1-\frac{\omega_{in}^2}{4\omega_n^2}\right)^2}{\xi^2\frac{\omega_{in}^2}{\omega_n^2}}}, \tag{5.42}$$

given that $2\xi\omega_n = (RC)^{-1}$ and $\omega_n^2 = (LC)^{-1}$. For $\Delta\omega = |\omega_{in} - 2\omega_n| \ll 2\omega_n$, we have

$$1-\frac{\omega_{in}^2}{4\omega_n^2} \approx \frac{\Delta\omega}{\omega_n}. \tag{5.43}$$

Realizing that $\xi = (2Q)^{-1}$, we reduce the fraction under the square root in Eq. (5.42) to $(Q\Delta\omega/\omega_n)^2$ and arrive at

$$A \geq \frac{2}{\beta}\sqrt{1+\left(\frac{Q\Delta\omega}{\omega_n}\right)^2}. \tag{5.44}$$

Figure 5.28(b) plots a typical input sensitivity as a function of ω_{in}. One CMOS example of such a BPF-based divider is depicted in Fig. 5.28(c).

It is interesting to note that a mixer has two input ports, that leads to two possible configurations of Miller dividers. As illustrated in Fig. 5.29, the output could either return to the RF port (type I) or the LO port (type II) of the mixer. Although conceptually indistinguishable, these two approaches still make difference in circuit implementation. Figure 5.30(a) shows a CMOS Miller divider with the output directly applied to the LO port. The M_3-M_6 quad of the double-balanced mixer can be redrawn as that in Fig. 5.30(b). It in fact resembles an injection-locked divider (which will be discussed in the next section): M_3 and M_4 form a cross-coupled pair, and M_5 and M_6 appear as diode-connected transistors to lower the Q of the tank and increase the locking range. The differential injection in such a manner is believed to help enlarge the range of operation to some extent. It is possible to find a self-resonance frequency of the circuit if $(W/L)_{3,4} > (W/L)_{5,6}$ [22].

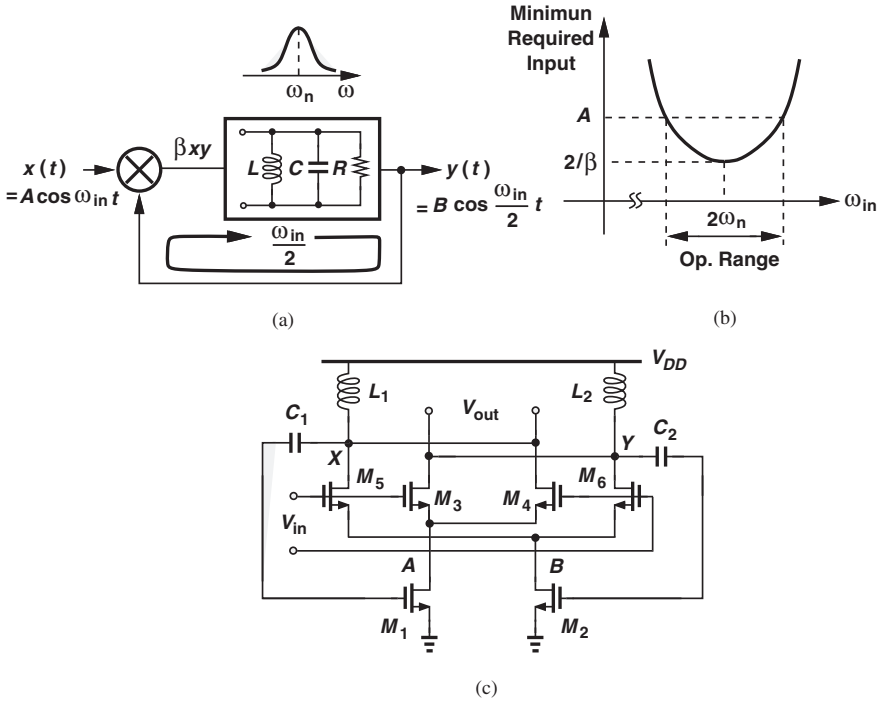


Fig. 5.28 (a) Regenerative divider with bandpass filter; (b) its input sensitivity, (c) typical CMOS realization.

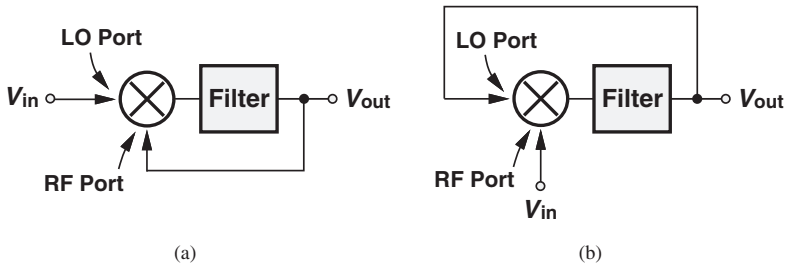


Fig. 5.29 Regenerative divider with the output fed back to (a) RF port, (b) LO port.

5.8 Injection-Locked Dividers

The operation speed of dividers can be further boosted up if we simplify the structure at the circuit level. Since a cross-coupled VCO provides ultimate simplicity in generating differential oscillation, one may think of injecting a periodic signal (approximately twice the VCO free-running frequency) into the common-mode point of it and forcing the VCO to lock. Recognized as an injection-locked divider, this

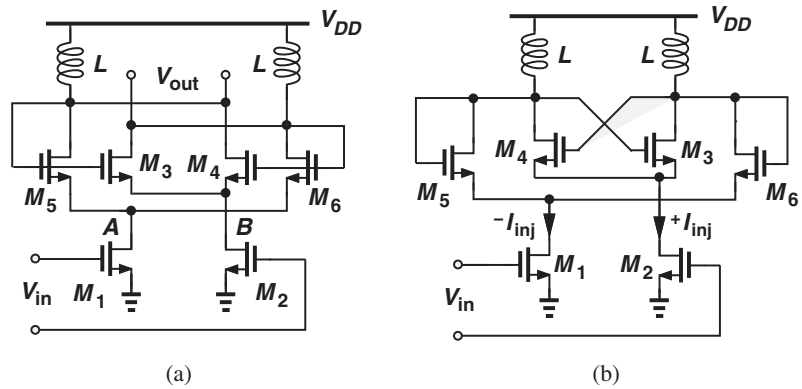


Fig. 5.30 (a) Type II regenerative divider, (b) redrawn to shown injection locking.

approach is indeed an inverse operation of push-push oscillators. Among the existing divider topologies, it basically reaches the highest speed.

The injection locking phenomenon can be explained as adding an external sinusoidal current I_{inj} to a well-behaved oscillator [Figure 5.31(a)]. If the amplitude and frequency of I_{inj} are chosen properly, the circuit oscillates at the injection frequency of ω_{inj} rather than the tank resonance frequency ω_0. The key point here is that, to accommodate the phase shift contributed by the tank at ω_{inj}, I_{osc} (the intrinsic oscillation current) and I_{inj} must sustain a certain phase difference such that the total phase shift maintains 0°. Intuitively, the injection locking would occur only in the vicinity of ω_0 and the locking range is limited. In fact, it can be analytically derived from different approaches [23][24] that the normalized locking range is given by

$$\frac{\Delta\omega}{\omega_0} = \frac{1}{Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I^2{}_{inj}}{I^2{}_{osc}}}}, \tag{5.45}$$

where Q denotes the quality factor of the tank. It degenerates to a simple form as $I_{inj} \ll I_{osc}$:

$$\frac{\Delta\omega}{\omega_0} \approx \frac{1}{Q} \cdot \frac{I_{inj}}{I_{osc}}. \tag{5.46}$$

The injection locking technique can be easily applied to dividers. Figure 5.31(b) shows such a circuit with the injection input I_{inj} of approximately twice the tank resonance frequency. The cross-coupled pair M_1-M_2 can be considered as a mixer down-converting ω_{inj} into $\omega_{inj} - \omega_0$. With abrupt switching,[4] it is equivalent to injecting a current of $I_{inj} \cdot (2/\pi)$ at $\omega_{inj} - \omega_0$ into the LC tank. Since $\omega_{inj} - \omega_0 \approx \omega_0$,

[4] It is expectable if the tail current and the inductors create enough swing at V_{out}.

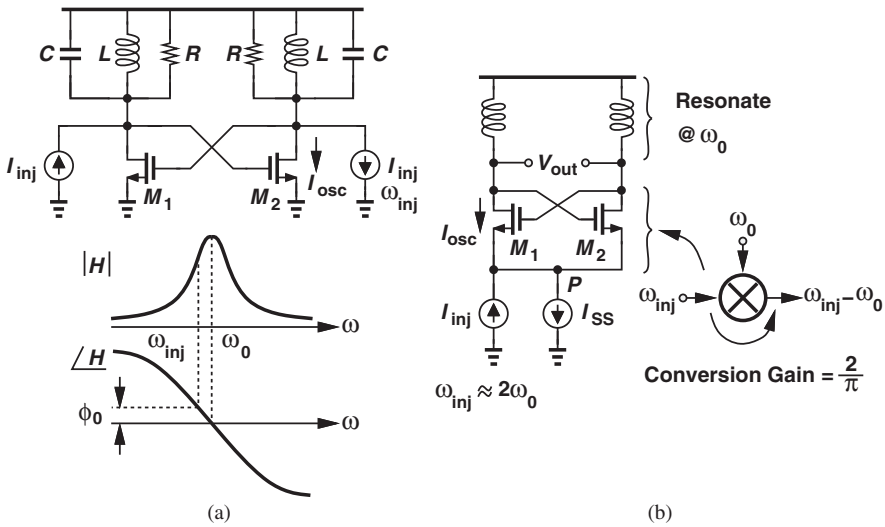


Fig. 5.31 (a) Operation of injection locking, (b) injection-locked divider.

we achieve the $\div 2$ operation with the following locking range

$$\frac{\Delta\omega}{\omega_0} = \frac{1}{Q} \cdot \frac{2}{\pi} \cdot \frac{I_{inj}}{I_{osc}}. \tag{5.47}$$

Note that Eqs. (5.45)-(5.47) define the *relative* locking range, which makes no difference whether it is observed from the input or the output.

A few modifications can be made to improve the performance of the divider in Fig. 5.31(b). One issue of the circuit in Fig. 5.31(b) stems from the parasitic capacitance associated with node P. At high speed, it creates a path to ground, robbing significant portion of I_{inj} and undermining the injection. To modify it, an inductor L can be added to resonate out the capacitance C_P [Fig. 5.32(a)], enlarging lock range without extra power consumption [25]. Other than the parasitic, the circuit in Fig. 5.31(b) is driven single-endedly, wasting 50% of the injection power. Another topology called “direct injection" is shown in Fig. 5.32(b) [26]. Here, the signal injection is accomplished by driving the two switches M_5 and M_6 differentially, which are sitting across the two outputs of the oscillator made of M_1-M_4 and L. Note that M_5 and M_6 are turned on and off almost simultaneously. Here, the input signals still drive the common-mode points, i.e., gates of M_5 and M_6. With proper design and biasing, the quasi-differential operation is expected to achieve a wider locking range.

The injection locking technique can be also utilized to implement dividers with modulus other than 2. Figure 5.33(a) reveals a possible realization of $\div 3$ circuit [27]. Here, transistors M_1-M_3 form a ring oscillator, and the input signal (approximately 3 times of the ring oscillation frequency) is injected into the “common-mode" point

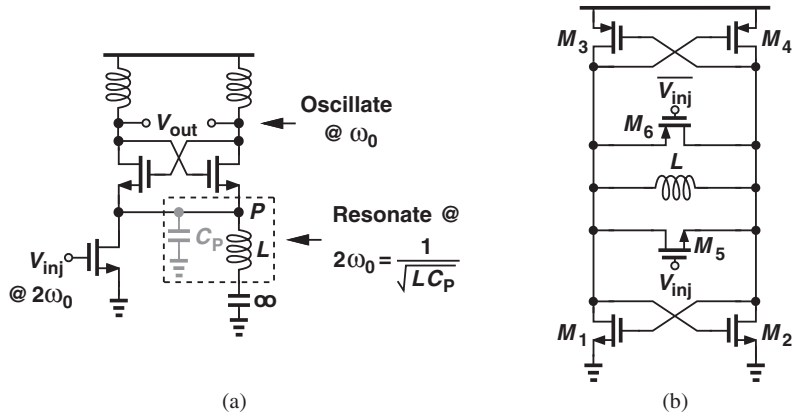


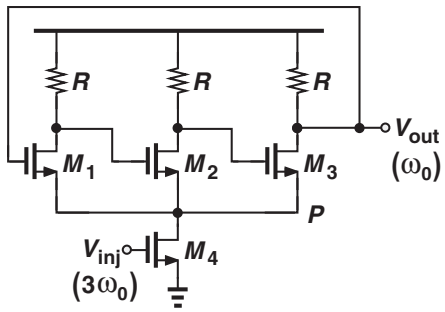
Fig. 5.32 Modified injection-locking dividers with (a) shunt peaking inductor, (b) direct injection.

by means of M_4. Again with proper design, the ring would lock to one-third of the input frequency. Figure 5.33(b) shows another divider example that performs $\div 4$ operation [28]. The circuit is nothing more than a direct injection divider but with M_3 functioning as a 3rd-order harmonic mixer. That is, under proper biasing, the 3rd-order harmonic of M_3 becomes comparable with the fundamental component [Fig. 5.33(b)]. In other words, the circuit mixes the input ($\approx 4\omega_0$) with the 3rd-order harmonic of the output, while the LC tank provides bandpass filtering at ω_0. Such an arrangement reaches twofold power efficiency as regular $\div 2$ circuits because the modulus is doubled.

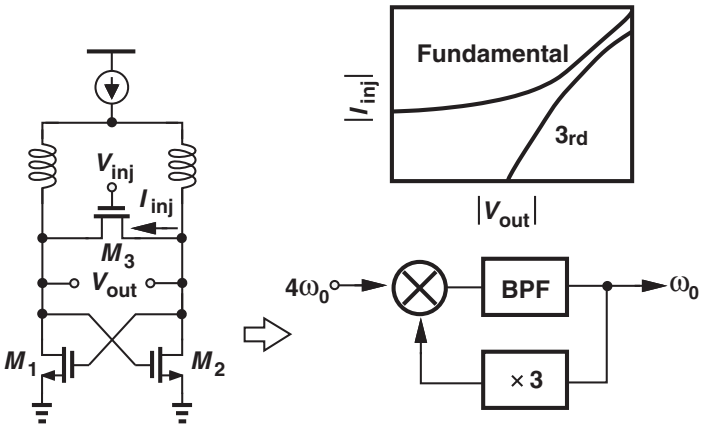
The narrow locking range of injection-locked dividers usually necessitates careful design, skillful layout, as well as meticulous EM simulations. It is especially true at high speed since the deviation of natural frequency caused by PVT variations may destroy the locking. Any tuning technique intended to dynamically adjust the locking range would prove futile because the varactor's overhead may have degraded the natural frequency considerably.

5.9 Case Study

To reinforce the design ideas described above, we analyze three mm-wave PLLs that can be incorporated in future wireless systems. Emphasizing the VCO and dividers, we present the circuit details and measurement results of these works in ascending order of frequency and sophistication.



(a)



(b)

Fig. 5.33 Higher modulus dividers utilizing injection-locking technique, (a)÷3, (b)÷4.

5.9.1 52-GHz LO Signal Generator

We first see the design of a 52-GHz PLL in a wireless transceiver [29]. It contains an on-chip VCO, an injection-locked divider as the first stage, a subsequent divider chain of modulus 512, an off-chip phase and frequency detectors, and a loop filter. The VCO is shown in Fig. 5.34(a), where the cross-coupled topology with ac coupling achieves a 10% tuning range around 52 GHz. In order to generate quadrature clocks, the first $\div 2$ circuit [Fig. 5.34(b)] is implemented as two identical injection-locked dividers coupling to each other. The transmission line and the varactor reveal a quality factor of 24 and 40, respectively. Measurement verifies that the VCO and its buffers consume 25 mW, and the divider presents a locking range of 3.1 GHz while drawing 3.1 mA from a 2.5-V supply. The circuits is implemented in SiGe BiCMOS process with an f_T of 200 GHz. Figure 5.35 depicts the VCO tuning curve, phase noise performance, and divider sensitivity. The phase noise at 1-MHz offset is -95 dBc/Hz.

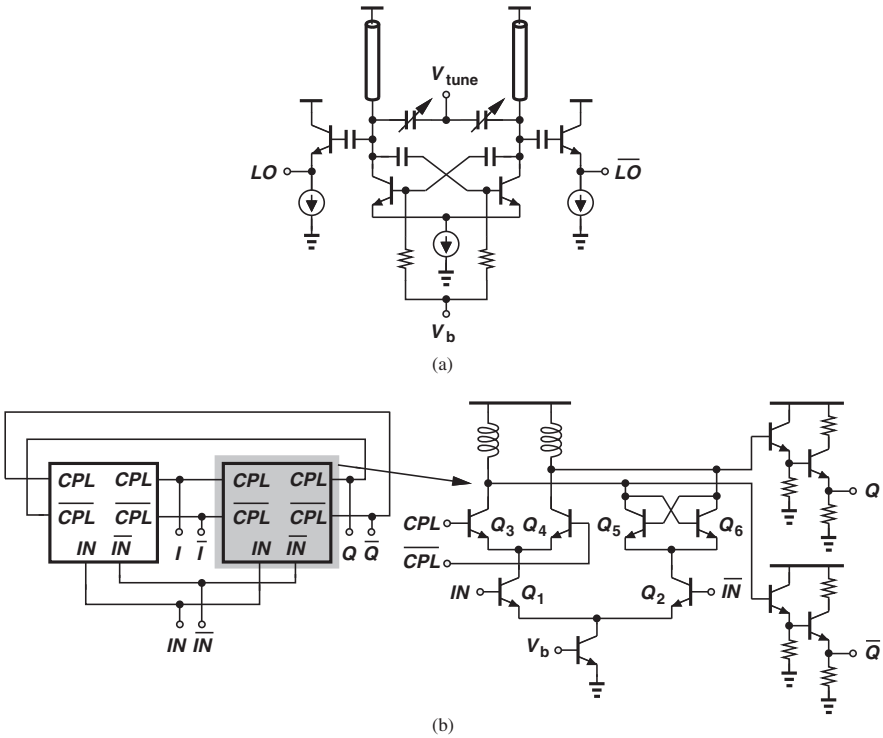


Fig. 5.34 (a)VCO, (b)first divider in [29].

5.9.2 60-GHz PLL in 0.15-μm GaAs

In the second case we look at a V-band PLL as shown in Fig. 5.36[30]. It consists of a single-transistor mm-wave VCO, a $\div 3$ circuit, a fourth-subharmonic mixer working as a phase detector, a low-pass filter, and amplifiers. With pure reference available, this design uses large loop bandwidth to obviate the need for frequency acquisition loop and to suppress the VCO phase noise. Figure 5.37(a) illustrates the VCO design. The common-source FET with series feedback structure is used to generate negative resistance with low phase noise [31][32]. The source series feedback employs a simple transmission line slightly longer than quarter wavelength so as to provide capacitive feedback. The parasitic inductance of the via is also included. The transmission lines and the varactor at the gate determine the oscillation frequency. The HEMT device and the varactor diode are 100 μm and 80 μm, respectively, achieving $2.5\times$ capacitance variation or equivalently 10% tuning range at 60 GHz. The anode and cathode are biased independently, and the capacitance C_{B1} and C_{B3} further suppress the high-frequency spurious and harmonics from the phase detector. A large resistor is used at the drain for low-frequency stability.

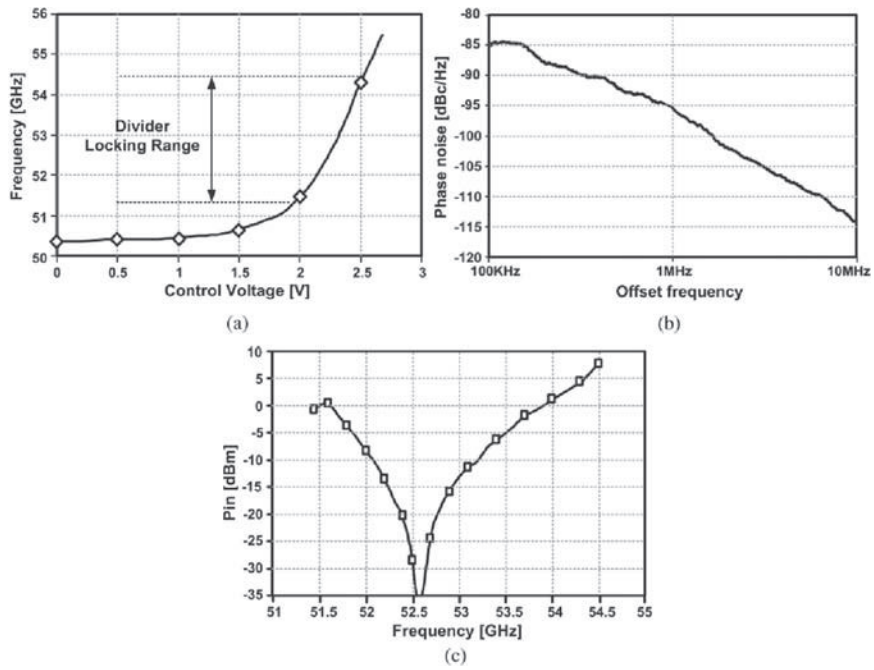


Fig. 5.35 (a)VCO tuning range, (b)VCO phase noise, (c)divider sensitivity of [29] (©IEEE 2006).

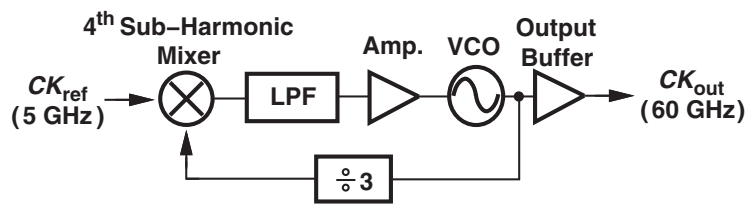


Fig. 5.36 PLL architecture of [30].

The $\div 3$ divider is designed based on a cascode injection locking topology. As shown in Fig. 5.37(b), it consists of cascode FETs and phase-delay lines tending to resonate at 1/3 of the input frequency. The inter-modulation terms are generated through nonlinear multiplication, which along with the feedback loop arrives at $\div 3$ operation. Two gate biases V_{g1} and V_{g2} are adjusted externally to optimize the performance. The output is coupled out of the circuit at a low-impedance point in the feedback loop. The feedback line is realized with impedance matching at both ends to maintain sufficient loop gain at f_0/3. The matching circuit at the gate of M_2 is implemented as the lowest impedance at f_0/3 for the same reason. The quarter wavelength open stub at f_0 is placed at the drain of M_2 to provide short circuit to

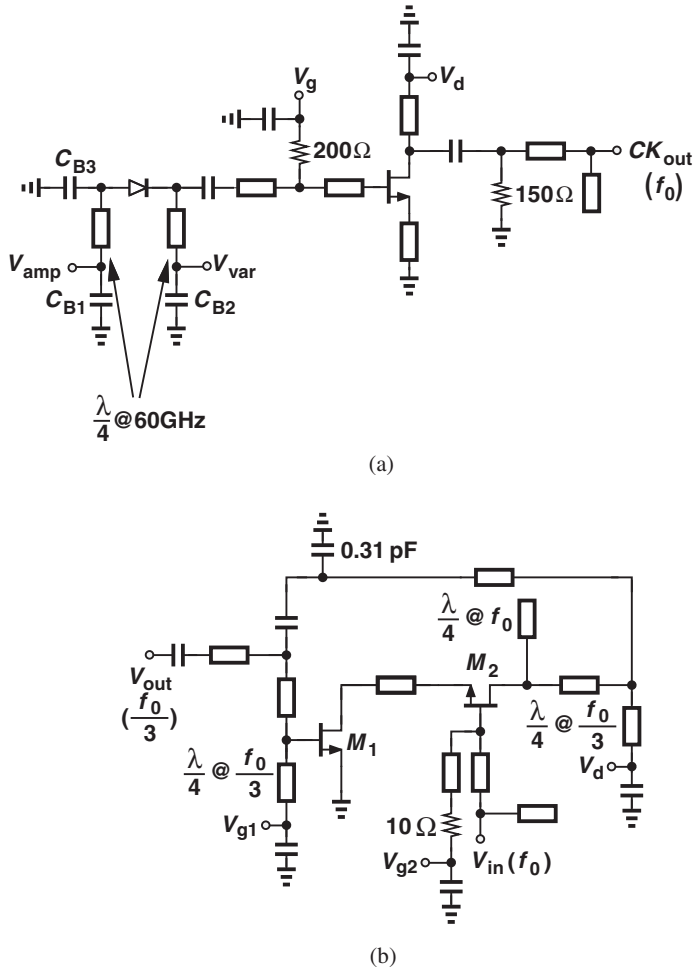


Fig. 5.37 (a)VCO, (b)÷3 circuit in [30].

the input signal. These stubs also act as band selecting filters, reducing the unwanted harmonics and spurs.

The VCO achieves a tuning range of 2.2 GHz and a phase noise of -87.7 dBc/Hz at 1-MHz offset. With $V_g = -0.4$ V and $V_d = 1.5$ V, the dc current of the VCO equals 28 mA. The ÷3 circuit reveals a bandwidth of 2.3 GHz around 60.9 GHz with an input power of 1 dBm. The power consumption is 7 mW. Figure 5.38 shows the VCO tuning curve and divider locking bandwidth.

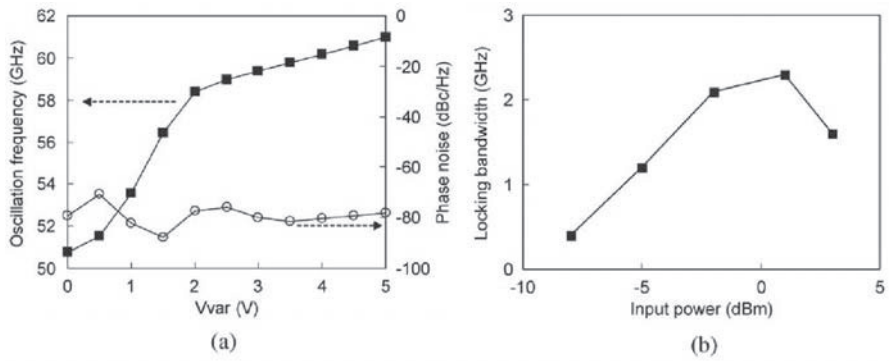


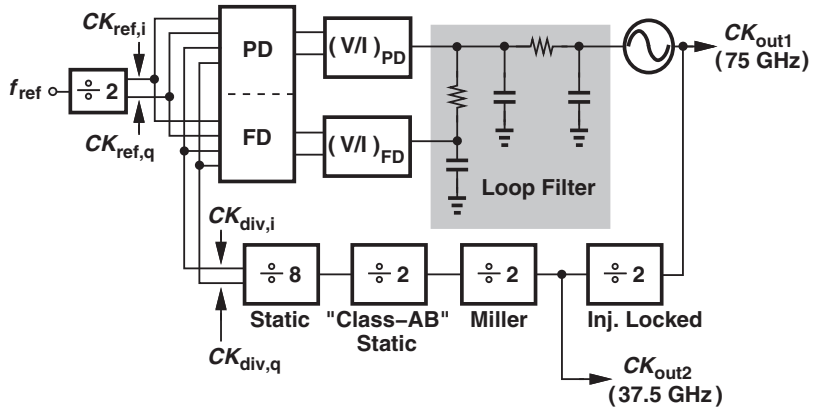
Fig. 5.38 Performance of [30]: (a)VCO tuning range and phase noise, (b)locking range of ÷3 circuit (©IEEE 2006).

5.9.3 A 75-GHz PLL in 90-nm CMOS

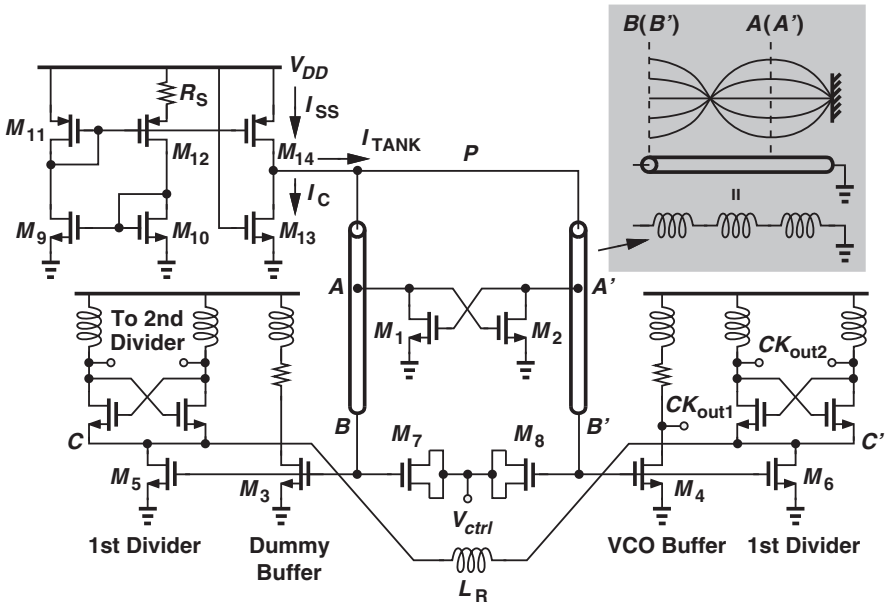
In the last case we study a fully-integrated CMOS design recently published [33]. Figure 5.39(a) shows the PLL architecture. It consists of a differential VCO running at full rate, a divider chain with total modulus of 64, a phase and freuquency detector, and a third-order loop filter. Different divider topologies: injection-locked, Miller, and static, are employed and placed in descendant order of frequency to accommodate the severe tradeoffs between the input frequency and operation range.

Figure 5.39(b) depicts the VCO and the first divider stage. Transmission lines equivalent to 3/4 wavelength of a 75-GHz clock is introduced here to distribute the capacitive loading and boost the oscillation frequency. Having one end short-circuited and the other open-circuited, these lines resonate differentially with the cross-coupled pair M_1-M_2 providing negative resistance. Connecting to the 1/3 points of the lines (nodes A and A'), this pair forces the transmission lines to create peak swings at these nodes. The waves thus propagate and reflect along the lines, forming the second maximum swings with opposite polarities at nodes B and B'. That is, node A (A') and node B (B') are 180° out of phase. As a result, the buffers (M_3-M_4), dividers (M_5-M_6), and varactors (M_7-M_8) can be removed to these ends, making the two zenith positions bear approximately equal capacitance. This arrangement absorbs the loading into the transmission lines and raises the oscillation frequency. To achieve high Q and compact layout, the transmission lines are actually realized as three identical inductors in series. The natural biasing established by M_1-M_2 pair facilitates dc coupling between the VCO and subsequent blocks. Careful layout arrives at perfect symmetry between the loadings at nodes B and B'. Inductor L_R is added to resonate out the parasitic capacitance associated with nodes C and C', allowing stronger signal injection through M_5 and M_6.

The VCO is biased with a supply-independent circuit M_9-M_{12} and R_S. To further reject the supply noise, M_{13} is introduced to absorb extra current variation caused by channel-length modulation. That is, $|\partial I_{SS}/\partial V_{DD}| = |\partial I_C/\partial V_{DD}|$ and the



(a)



(b)

Fig. 5.39 (a) PLL architecture, (b) VCO and first divider of [33].

current flowing into M_1-M_2 pair (I_{TANK}) remains constant. It leads to a fixed voltage at node P, leaving the resonance frequency insensitive to supply perturbation.

The PLL has been fabricated in 90-nm CMOS technology. The total power consumption with a 1.45-V supply is 88 mW, of which 8 mW is dissipated in the VCO, 66 mW in the divider chain, and 14 mW in the PFD and V/I converters. Figure 5.40 depicts the output spectra of the VCO and the first divider under locked condition.

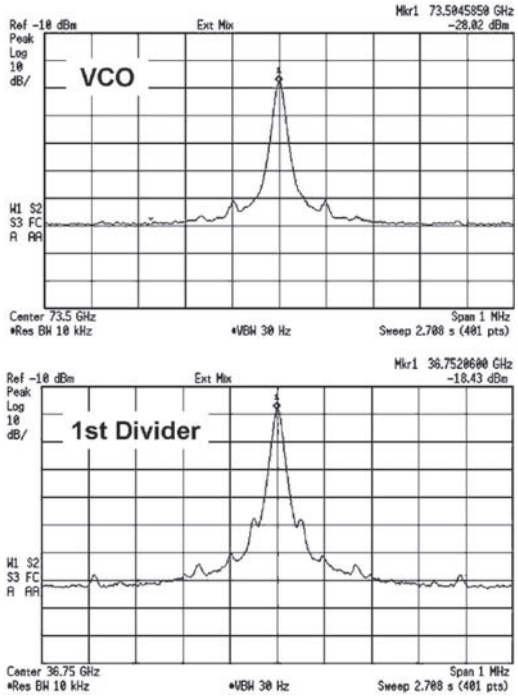


Fig. 5.40 Output spectra of VCO and first divider in [33].

The phase noise at 100-kHz offset measures −88 and −94 dBc/Hz, respectively. The time domain performance are recorded as shown in Fig. 5.40. The 75-GHz output presents peak-to-peak and rms jitter of 609 fs,pp and 87 fs,rms, respectively, whereas the 37.5-GHz output reveals jitter of 2.15 ps,pp and 293 fs,rms.

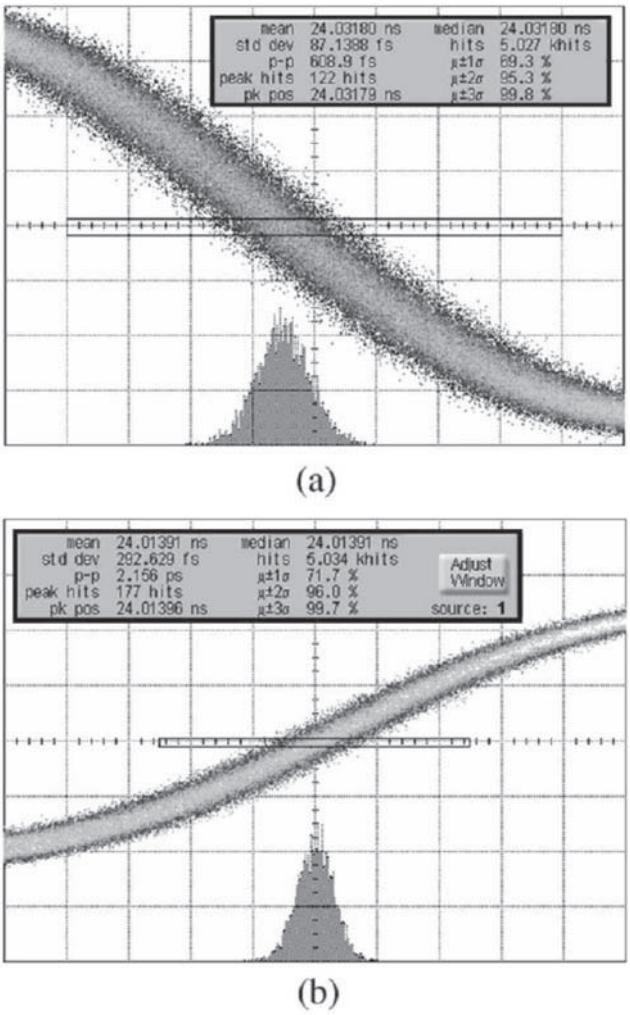


Fig. 5.41 Waveforms in [33] for (a) 75-GHz, (b) 37.5-GHz outputs.

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