

Performance Improvement of FinFET using Nitride Spacer

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Abstract— The Double Gate FinFET has been designed for 90nm as an alternative solution to bulk devices. The FinFET with independent gate (IDG) structure is designed to control V_{th} . When the V_{th} is controlled the leakage current can be decreased by improving its current driving capability. The metal used for the front gate and back gate is TiN. Here the device performance is compared using nitride spacer and device without spacer. The work function is a very important consideration in the selection of metal for the gate structure and also it affects the V_{th} and the performance of a device.

Keywords— DG FinFET, DIBL, SS

I. INTRODUCTION

According to International Technology Roadmap for Semiconductors (ITRS) by the year 2014, 94% of the chip is occupied by the memory devices. A FinFET is an intrinsic body which will greatly suppresses the device-performance variability caused by the fluctuation in the number of dopant ions. Heavy doping reduces mobility due to impurity scattering and a high transverse electric field in the on state worsens sub-threshold swing and increases parasitic junction capacitance. FinFETs are alternatives to bulk FETs due to their stronger electrostatic control over the channel which have improved short channel behaviour.

II. DIFFICULTIES IN MOSFET DESIGN

The threshold (V_{th}) variation caused by random dopant fluctuations is a major concern for nanoscale bulk MOSFETs. In a bulk MOSFET cell, exponential increase in leakage current results in large standby power. The width of the fin is the effective body thickness, and the height of the fin is the effective channel width. In the ON condition, current flows between the source and drain along the gated sidewall surfaces of the Si fin [1] [9]. Due to high leakage current and increased process variation, designing low-power and robust memories is a major challenge in nanoscale technologies.

III. DOUBLE GATE FINFET

Double Gate FinFET at 90 nm is suitable for future nanoscale memory circuits design due to its reduced Short Channel Effects (SCE) and leakage current. A nitride spacer that behaves as an etch stop layer is a popular choice for sidewall

spacer in modern complementary metal oxide semiconductor (CMOS) process flows [19]. As MOSFETs are scaled down to nano scale measure, dopant fluctuations, oxide thickness variations and line edge roughness increases the fluctuations in transistor threshold voltage (V_t) and correspondingly affect the ON and OFF currents. To solve this problem new MOSFET architectures involving the use of multiple gates controlling the transistor have been proposed. The OFF-current also increases with oxide thickness because of increase in the short channel effects [5]. Process and device simulations are performed with varying doping of the fin, anti-punch implant dose and energy, fin width, fin height and thickness of gate oxide [5]. Non-planar MOSFETs have potential advantages in density of packing, carrier transport, and scalability of device. The 3D view of the FinFET device is given below.

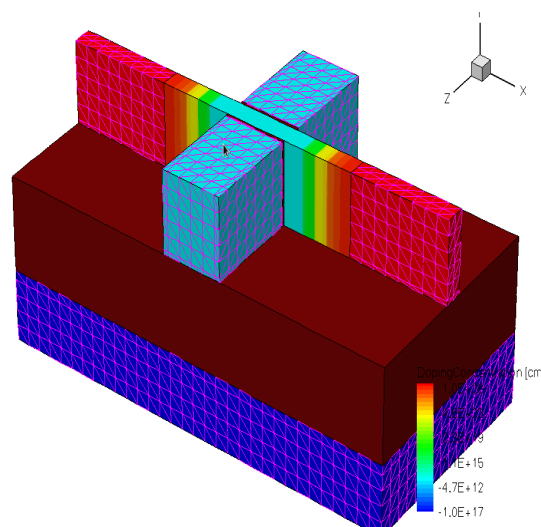


Fig 1. Meshed Structure of DG FinFET

The OFF-current will increase with oxide thickness because of increase in the short channel effects [5]. The effective gate length is reduced which results in an increased short channel effects and threshold voltage therefore decreases with the increased thickness of oxide. When the gate length is shorter, the control of short channel effect in the bulk devices is difficult. So the FinFET devices have increasing performance

improvements over bulk-Si MOSFETs with technology scaling.

A. 90 nm Technology

In 90nm technology, the oxide thickness is 1.5nm and the fin thickness is 30nm. The doping concentration of source and drain is $1e+20$ and the channel is doped with $1e+17$. The addition of the Raised Source and Drain structures reduces the lateral diffusion of the highly doped source and drain (HDD) under the sidewall spacers.

TABLE I
DIFFERENT PARAMETERS AT 90NM TECHNOLOGY

Parameters	Dimensions
Length of the gate (L_g)	90nm
Spacer Width	15nm
Gate oxide thickness (T_{ox})	1.5nm
Thickness of fin (T_{fin})	30nm
Doping Conc. of source and drain	$1e+20$
V_{DD}	1V
Doping Conc. For Channel	$1e+17$

One of the most promising structures is the DG FinFET which consists of a narrow silicon fin, which provides an ideal 60 mV/dec sub threshold swing and robustness against short-channel effects. The thin body reduces sub-surface leakage paths between source and drain.

IV. RESULTS AND DISCUSSIONS

Device simulations have been performed using the drift-diffusion model which solves self-consistently the Poisson and carrier continuity equations in the designated device regions with specified boundary conditions. Threshold voltage V_T is the minimum gate voltage which can form a channel between the source and drain. ON current is defined as the maximum drain current (I_D) produced due to the flow of the electrons from source to drain when the gate voltage (V_{GS}) is applied. As the gate voltage (V_G) increases above the threshold voltage (V_T), the device channel begins to conduct current. The current flow depends on the ON-resistance of the device. The implementation of a metal gate requires metal gate work function (WF) engineering which is an important option in order to set the threshold voltage (V_T). For a metal gate thickness higher than 10 nm the work function reaches a constant value[24].

TABLE II
COMPARISON OF PARAMETERS AT 90NM TECHNOLOGY USING SPACER AND WITHOUT SPACER

90nm	I_{ON} current (μA)	I_{OFF} current (μA)	DIBL (mV/V)	Subthreshold Swing (SS) (mV/Dec)	Transconductance (gm) ($\mu\Omega$)
With Nitride Spacer	$1e-03$	$3.08e-08$	67.15	75.159	$2.1e-04$
Without Spacer	$1e-04$	$3.607e-08$	69.96	69.11	$1.97e-04$

The DIBL should be small and Subthreshold Swing should be larger for 90nm technology using spacer. I_{on}/I_{off} should be above ($e+03$) which may increase the switching speed of the device [13]. Transconductance of a device is the amplification delivered by the device. Hence transconductance-to-current ratio is a better method to access the performance of a device. The equation given below shows the relation between drain current and transconductance which is directly proportional to each other [21].

$$g_m = \Delta I_{on} / \Delta V_{gs}$$

where I_{on} is the drain current and V_{gs} is the gate voltage given to the device. DIBL is defined as the phenomenon to a reduction of threshold voltage at higher drain voltages.

$$DIBL = dV_{th} / dV_d$$

The sub threshold slope is equal to its reciprocal value called sub threshold swing which is given below:-

$$S = \ln(10)kT/q(1 + C_d / C_{ox})$$

where the value for C_d and C_{ox} is given as C_d = Depletion layer capacitance, C_{ox} = Gate-oxide Capacitance.

ACKNOWLEDGMENT

We thank the Almighty on course of completion of this work. This research project would not have been possible without the support of many people. The authors wish to express their thanks to the faculties of Electronics department who works on "Device Modeling".

V. CONCLUSIONS

FinFETs have been designed for 90nm using metal gate and Nitride Spacer. It is also found that the threshold voltage is controlled by applying a voltage at the back gate. The device designed using nitride spacer is better compared to normal FinFET without spacer. The device performance is analysed practically and the results thus obtained is compared with the mathematical models.

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