

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE
THE PATENT TRIAL AND APPEAL BOARD**

In re U.S. Patent No. 9,590,582

IPR2023-00788

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Inventors: Hsiao-Tsung, Yen Yuh-Sheng, and Jean Ta-Hsun Yeh

Assignee: Realtek Semiconductor Corp.

Title: Semiconductor Device with Inductor-Capacitor Resonant Circuit

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U.S.P.T.O.

P.O. Box 1450

Alexandria, VA 22313-1450

I, Paul R. Prucnal, make this supplemental declaration in connection with the petition for *inter partes* review submitted by Petitioner for U.S. Patent No. 9,590,582 to supplement a prior declaration I made for the same proceeding (EX-1003). All statements made herein of my own knowledge are true, and all statements made herein based on information and belief are believed to be true. Although I am being compensated for my time in preparing this declaration, the opinions expressed herein are my own, and I have no stake in the outcome of this proceeding or any related litigation or administrative proceedings.

I. INTRODUCTION

1. In preparing my declaration, I have reviewed documents listed below and those cited herein.

Exhibit No.	Description
1001	U.S. Patent No. 9,950,582
1002	File History of U.S. Patent No. 9,590,582
1003	Declaration of Dr. Paul Prucnal
1004	Curriculum Vitae of Dr. Paul Prucnal
1005	J. Gonzalez et al., <i>A 56-GHz LC-Tank VCO With 17% Tuning Range in 65-nm Bulk CMOS for Wireless HDMI</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 58, Issue 5 (May 2010), available at https://ieeexplore.ieee.org/document/5438827
1006	Matthew Muh, Master of Science thesis entitled <i>Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO</i> , Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley (2005), available at https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=7337593a3bdb909b1f7d53da1c3202a61401fac7
1007	A. Niknejad et al., <i>mm-Wave Silicon Technology 60 GHz and Beyond</i> (Springer Science + Business Media 2008) (excerpts)
1008	S. Biswal, <i>Basic Electronics Volume I</i> (Atlantic Publishers 2001) (excerpts)
1009	A. Niknejad & R. Meyer, <i>Design, Simulation and Applications of Inductors and Transformers for Si RF ICs</i> (Springer Science+Business Media 2000) (excerpts)
1010	A. Niknejad, <i>Electromagnetics for High-Speed Analog and Digital Communication Circuits</i> (Cambridge Univ. Press 2007) (excerpts)
1011	Joachim N. Burghartz, <i>Spiral Inductors on Silicon – Status and Trends (Invited Article)</i> , International Journal of RF and Microwave Computer-Aided Engineering, V. 8, No. 6, 422-432 (Nov. 1998), available at https://onlinelibrary.wiley.com/doi/abs/10.1002/%28SICI%291099-047X%28199811%298%3A6%3C422%3A%3AAID-MMCE3%3E3.0.CO%3B2-K

Exhibit No.	Description
1012	O.H. Murphy et al., <i>Design of Multiple-Metal Stacked Inductors Incorporating an Extended Physical Model</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 53, No. 6, 2063-2072 (June 2005), available at https://ieeexplore.ieee.org/document/1440724
1013	U.S. Patent No. 6,885,275 filed on Jan. 28, 2000, titled “Multi-track Integrated Spiral Inductor” to James Chang (“Chang”)
1014	U.S. Patent Application Pub. No. US 2008/0074229 published on Mar. 27, 2008 by Shahriar Moinian et al. (“Moinian”)
1015	Bryant Derand Williamson, Masters Thesis entitled <i>A 2.4 GHz LC-VCO Using On-Chip Inductors and Accumulation- Mode Varactors in a CMOS 0.18 μm Process</i> , University of Tennessee – Knoxville, Aug. 2005, available at https://trace.tennessee.edu/utk_gradthes/2537/ Axel Dominique Berny, PhD Dissertation entitled <i>Analysis and Design of Wideband LC VCOs</i> , Electrical Engineering and Computer Sciences, University Of California, Berkeley, Spring 2006, available at https://www2.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-50.pdf
1016	Axel Dominique Berny, PhD Dissertation entitled <i>Analysis and Design of Wideband LC VCOs</i> , Electrical Engineering and Computer Sciences, University Of California, Berkeley, Spring 2006, available at https://www2.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-50.pdf
1017	A. Kral et al., <i>RF-CMOS Oscillators with Switched Tuning</i> , IEEE Custom Integrated Circuits Conference, May 14, 1998 available at https://ieeexplore.ieee.org/document/695039
1018	Fei Yuan, <i>CMOS Active Inductors and Transformers Principle, Implementation, and Applications</i> , (Springer Science+Business Media, LLC 2008) ISBN 978-0-387-76477-1, available at https://link.springer.com/book/10.1007/978-0-387-76479-5
1019	Thomas H. Lee et al., <i>RF Passive IC Components</i> in book entitled <i>Circuits and Filters Handbook</i> , 2d Ed. (CRC Press LLC 2003), available at http://www.kelm.ftn.uns.ac.rs/literatura/ekui/Circuits_and_Filters_Handbook_CH10.pdf
1020	Agilent Technologies, <i>Overview on interdigital capacitor design</i> , 2001, available at https://www.keysight.com/us/en/assets/7018-08093/technical-overviews-archived/5989-8912.pdf

Exhibit No.	Description
1021	Sang Wook Park, PhD Dissertation entitled <i>Oscillator Architectures And Enhanced Frequency Synthesizer</i> , Texas A&M University (Dec. 2009) (“Park”), available at https://core.ac.uk/download/pdf/13643134.pdf
1022	Changhua Cao et al., <i>Millimeter-Wave Voltage-Controlled Oscillators in 0.13-um CMOS Technology</i> , IEEE Journal of Solid-State Circuits, Vol. 41, Issue 6 (June 2006) (“Cao”), available at https://ieeexplore.ieee.org/document/1637594
1023	Yue Wu et al., <i>A Temperature Stabilized CMOS VCO for Zero-IF Cellular CDMA Receivers</i> , Digest of Technical Papers, 2005 Symposium on VLSI Circuits, June 16-18, 2005 (“Wu”), available at https://ieeexplore.ieee.org/document/1469413
1024	Dorra Mellouli et al., <i>Design and Implementation of A 6-GHz Array of Four Differential VCOs Coupled Through a Resistive Network</i> , Analog Integrated Circuits and Signal Processing, Vol. 76, pp. 179-193 (2013) (“Mellouli”), available at https://link.springer.com/article/10.1007/s10470-013-0099-6#citeas
1025	Xiao Shimao et al., <i>A novel 2.95–3.65 GHz CMOS LC-VCO using tuning curve compensation</i> , Journal of Semiconductors, Vol. 30, No. 10, 105001 (Oct. 2009) (“Xiao”), available at https://iopscience.iop.org/article/10.1088/1674-4926/30/10/105001/pdf
1026	Mohammad Nariman et al., <i>A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS</i> , 2010 IEEE Radio Frequency Integrated Circuits Symposium, May 23-25, 2010, pp. 157-160 (“Nariman”), available at https://ieeexplore.ieee.org/document/5477323
1027	Neric H. W. Fong, PhD Dissertation entitled <i>Low-Voltage Radio-Frequency CMOS Integrated Circuits in Silicon-On-Insulator</i> , Department of Electronics, Carleton University, Ottawa, Canada (May 23, 2002) (“Fong”), available at https://curve.carleton.ca/system/files/etd/63d93fb2-a8cc-4f63-865e-fba751da4fa1/etd_pdf/02a5d5d8788c5ea3b03555a6557ea59c/fong-lowvoltagefrequencycmosintegratedcircuits.pdf
1028	Babak Soltanian et al., <i>An Ultra Compact Differentially Tuned 6 GHz CMOS LC VCO with Dynamic Common-Mode Feedback</i> , IEEE 2006 Custom Integrated Circuits Conference, Sept. 10-13, 2006

Exhibit No.	Description
	(“Soltanian”), available at https://ieeexplore.ieee.org/document/4115046
1029	V. Macaitis et al., <i>Design of a 4.48-5.89 GHz LC-VCO in nm RF CMOS Technology</i> , Elektronika IR Elektrotechnika, Vol. 20, No. 2, 44-47 (Feb. 5, 2014) (“Macaitis”), available at https://eejournal.ktu.lt/index.php/elt/article/view/6383
1030	Judith Maget, <i>Varactors and Inductors for Integrated RF Circuits in Standard MOS Technologies</i> , Institute of Electronics at the University of Bundeswehr (2002) (“Maget”), available at http://athene-forschung.unibw.de/doc/85282/85282.pdf .
1031	Paolo Lucchi, PhD Dissertation entitled <i>Frequency generation for mm-Wave and satellite applications</i> , University of Bordeaux (Feb. 2012) (“Lucchi”), available at https://www.theses.fr/2012BOR14479.pdf
1032	U.S. Patent Publication No. 2009/0322447 (“Daley”)
1033	U.S. Patent No. 9,270,247 (“Jing”)
1034	Realtek Infringement Chart for U.S. Patent No. 9,950,582
1035	Printout from www.m-w.com (Merriam-Webster Online Dictionary) (“substantial”)
1040	Order Denying Realtek’s Motion for Summary Determination (Public Version), <i>Certain Integrated Circuits, Components Thereof, and Products Containing the Same</i> , Inv. No. 337-TA-1350 (Sept. 7, 2023)
1044	B. Raj et al., <i>Analytical Modeling of Nanoscale Double Gate FinFET Device</i> , Journal on Intelligent Electronic Systems, Vol. 1, No. 1 (Nov. 2007)
1045	F. Nesamani et al., <i>Performance Improvement of FinFET using Nitride Spacer</i> , International Journal of Engineering Trends and Technology, Vol. 4, Issue 3 (2013)
1048	Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond, <i>Certain Integrated Circuits, Components Thereof, and Products Containing the Same</i> , Inv. No. 337-TA-1350 (Jan. 19, 2024) (public version)
1049	Portions of Transcript from October 16-20, 2023, Trial in <i>Certain Integrated Circuits, Components Thereof, and Products Containing the Same</i> , Inv. No. 337-TA-1350 (portions from public hearing)
1051	Transcript of April 19, 2024 Deposition of Dr. Joshua Phinney

2. In forming my opinions expressed below, I have considered the documents listed immediately above and my knowledge and experience based on my work and education in this area as described below. In particular, I have reviewed EX-2003, the Declaration of Joshua Phinney, Ph.D., and the exhibits cited therein, which I respond to herein.

II. QUALIFICATIONS AND COMPENSATION

3. My qualifications and compensation are laid out in my Initial Declaration which I incorporate herein by reference. *See*, EX-1003.

III. GROUND 1: OBVIOUSNESS BASED ON GONZALEZ

1. The 582 patent expressly teaches in its Fig. 12 that a MOS capacitor has electrode segments

4. As I have explained, “the ’582 Patent itself discloses MOS capacitors (e.g., capacitor component 150’ in its Fig. 12)” that have electrode segments. EX-1003, ¶165. Specifically, in Fig. 12 of the 582 patent, “the capacitor component 150’—which is a ‘MOS capacitor’—includes finger-shaped electrode segments 155, 156, 157, 158, just like Gonzalez’s finger-shaped electrode segments.” *Id.*

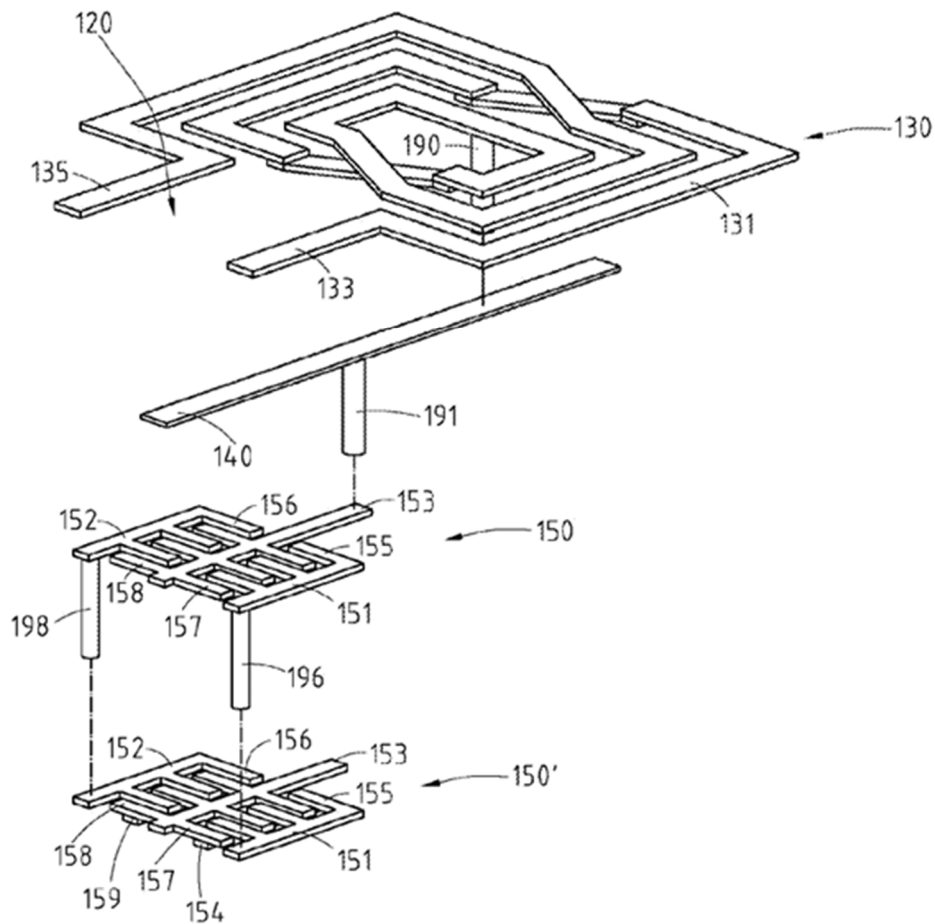


FIG. 12

EX-1001, Fig. 12.

5. Realtek in the POR and Dr. Phinney in his declaration do not address the MOS capacitor 150' in Fig. 12 of the 582 patent, let alone address whether/how it differs from Gonzalez's MOS capacitors. *See generally* POR.

6. Realtek and Dr. Phinney's argument that "silicon-based" MOS capacitors cannot include metal electrode segments above silicon structures contradicts the 582 patent's disclosures. POR, 26, 31. In the MOS capacitor 150', segments 155-158 are interdigitated metals. EX-1001, Fig. 12, 5:45-47 ("the

electrode segments 155, 156, 157, and 158 are all formed by patterning the second metal layer.”); EX-1051 (Phinney Dep.).125:23-25 (“those electrode segments are metal”).

7. Notably, segments 155-158 are described in the 582 patent as “electrode segments,” contradicting Dr. Phinney’s assertion that “the capacitance of [MOS] varactors comes from electric fields created substantially vertically between transistor gates and the doped substrate beneath, *not from electric fields extending laterally between interdigitated metals.*” EX-2003, ¶98. Also, the 582 patent discloses additional structures below the segments 155-158 in the MOS capacitor 150’ as “semiconductor segment 154/159,” not electrode segments. EX-1001, 12:16-20 (“By using the MOS capacitor as an example and referring to FIG. 12, the capacitor component 150’ further includes at least one *semiconductor segment 154/159* in addition to the members shown in the foregoing embodiments [e.g., electrode segments 155, 156, 157, 158].”)

8. Dr. Phinney argues that “a POSITA would understand that the claimed electrode segments are specifically the electrode plates of the claimed capacitor of the claimed LC circuit, the component that provides the capacitance for the LC circuit.” EX-2003, ¶101. Following this definition and his opinion above that “the capacitance of [MOS] varactors comes from electric fields created substantially vertically between transistor gates and the doped substrate beneath, not from

electric fields extending laterally between interdigitated metals”, the segments 155-158 in the MOS capacitor 150’ would not be electrode segments.

9. The 582 patent acknowledges that “the structures of the capacitors in various forms [including MOS capacitor] are well known in the field.” EX-1001, 12:11-16. The 582 patent does not disclose how semiconductor segment 154/159 works in connection with electrode segments 155-158 to induce capacitance in the MOS capacitor 150’. Based on “well-known” structures of MOS capacitors such as those disclosed by Gonzalez, a POSITA would understand that the semiconductor segment 154 (or 159) can work as a gate (e.g., N⁺ poly gate), which receives a voltage (e.g., Out⁺ or Out⁻) delivered through some (but not all) of the electrode segments 155-158 using vias to induce capacitance while avoiding electrical shorting. EX-1003, ¶162-166; EX-1051 (Phinney Dep.).82:8-25.

2. Gonzalez’s yellow fingers meet the claimed “electrode segments.”

10. A POSITA would have understood that Gonzalez’s yellow fingers share many similarities with the 582 patent’s electrode segments 155-158 in the MOS capacitor 150’.

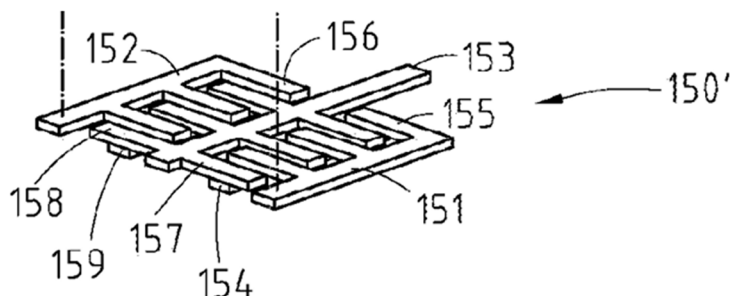
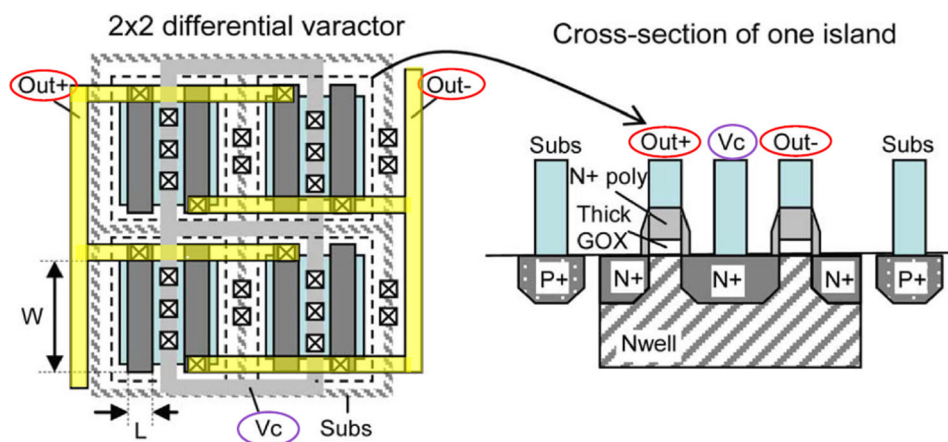


FIG. 12

EX-1001, Fig. 12 (partial).



EX-1003, ¶166.

11. I provide a list of some of these similarities below:

- Like the electrode segments 155-158, Gonzalez's yellow fingers are metal wires. Dr. Phinney confirmed Gonzalez's yellow fingers are metal wires. EX-1051 (Phinney Dep.).35:1-7; EX-2003 ¶100. He also confirmed that in the 582 Fig. 12 the electrode segments 157, 158, via 191, center tap 140, and the extension-conductor segments are all metal wires. EX-1051 (Phinney Dep.).22:22-24:14, 84:13-15. Also, he

testified in the parallel ITC trial that the extension-conductor segments are also “wiring.” EX-1049.216:6-14.

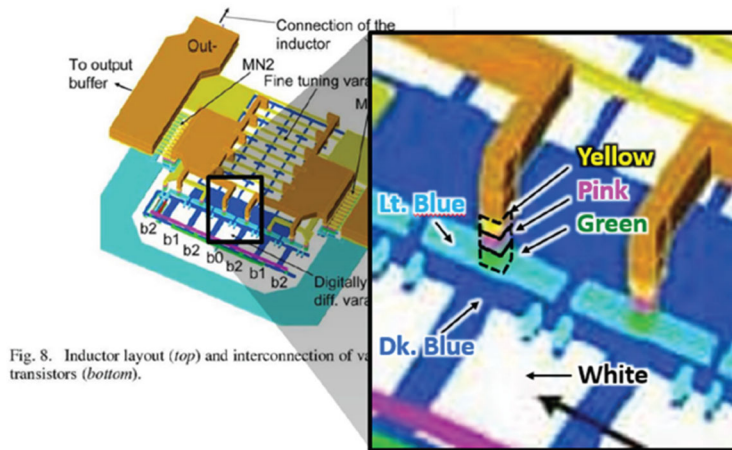
- Like the electrode segments 155-158, Gonzalez’s yellow fingers are part of a MOS capacitor. EX-1003, ¶162-166 (citing, e.g., EX-1005, Fig. 5 and explaining that the yellow fingers are part of the fine tuning MOS varactor); EX-1001, Fig. 12.
- Like the electrode segments 155-158, Gonzalez’s yellow fingers are located above, and extend approximately perpendicular to, underlying semiconductor segments. As I explained, Gonzalez’s Fig. 5 illustrates the F-shaped yellow fingers as located above the N⁺ poly gates, which are semiconductor structures. EX-1003, ¶166 (citing EX-1005, Fig. 5); EX-1051 (Phinney Dep.).82:8-25, 85:5-23, 86:16-87:1, 90:4-9 (Dr. Phinney agreeing that the F-shaped structures are located on a layer above the N⁺ poly gates (darker-grey boxes), and that the horizontal lines of the F-shapes are perpendicular to those N⁺ poly gates). Similarly, the 582 patent discloses that, in Fig. 12, “[t]he semiconductor segment 154 (or 159) is located below the first electrode segment 155 (or 156) and the second electrode segment 157 (or 158) . . . , and the extension direction of the semiconductor segment 154/159 is approximately perpendicular to the extension

direction of the first electrode segment 155/156 and the second electrode segment 157 /158.” EX-1001, 12:20-28.

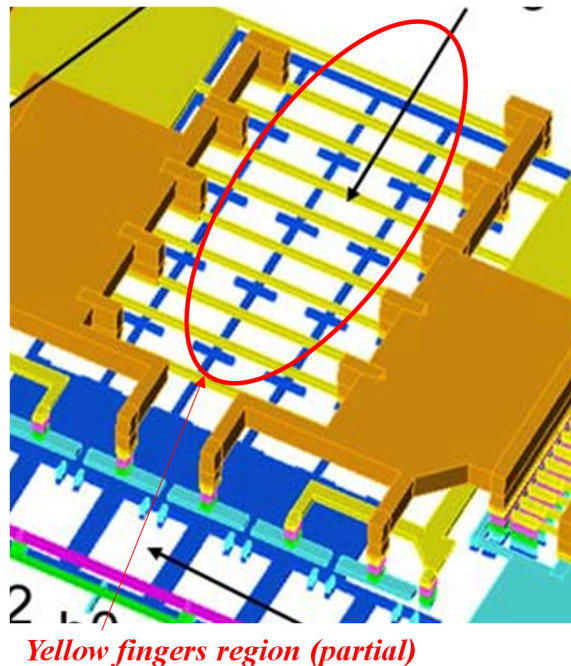
- Like the electrode segments 155-158, Gonzalez’s yellow fingers form a comb structure capacitor. EX-2003, ¶102 (Dr. Phinney stating the yellow fingers are designed as a “comb structure” to introduce a “static capacitance”); EX-1003, ¶162.
- Like the electrode segments 155-158, Gonzalez’s yellow fingers serve as gate electrodes (or parts thereof) that deliver voltage to the underlying semiconductor segments (e.g., N+ poly gate) to induce capacitance while avoiding electrical shorting. EX-1003, ¶166.

a. Gonzalez’s yellow fingers are part of its MOS capacitor

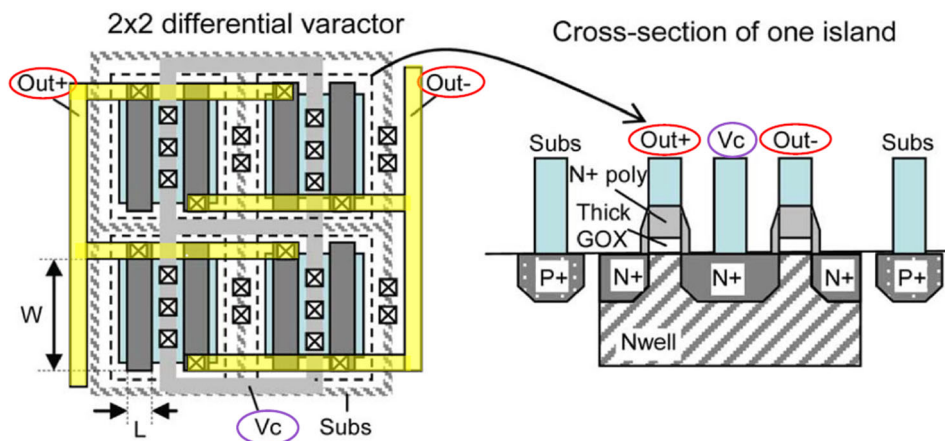
12. As I previously explained, Gonzalez’s fine tuning MOS varactor includes the yellow fingers as electrode segments. Fig. 5 of Gonzalez describes a “varactor structure” and expressly includes the F-shaped finger structures. EX-1003, ¶162-166 (citing EX-1005, Fig. 5). Realtek and Dr. Phinney assert that Gonzalez’s yellow fingers of Fig. 8 cannot correspond to the F-shaped fingers in Fig. 5 allegedly because the yellow fingers in Fig. 8 “sit at least five metal layers” above silicon, while the F-shaped fingers are “at most two metal layers above the silicon.” POR, 30-34. As explained below, that argument is incorrect and irrelevant.



13. First, in Gonzalez's Fig. 8, the additional metal layers (e.g., light blue, green, pink) highlighted by Realtek and Dr. Phinney do not extend into the region under the yellow fingers, as illustrated below. EX-1051 (Phinney Dep.).64:10-65:11 (Dr. Phinney agreeing the additional metal layers do not extend below the yellow fingers).



14. Second, in Gonzalez's Fig. 8, the yellow fingers connect directly downward to the N+ poly gates, just as shown in Fig. 5.¹ This explains why the same fingers are shown in Fig. 5 as F-shaped fingers directly above the N+ poly gates. The fact that the yellow fingers sit above the silicon is consistent with Fig. 12 of the 582 patent, which discloses its electrode segments 155-158 sitting above semiconductor segments. Indeed, viewing Gonzalez's overall disclosures including Figs. 2, 5, and 8, which all show voltage terminals Out+ and Out-, a POSITA would have readily concluded that the yellow fingers correspond to the F-shaped fingers in Fig. 5 to supply the Out+ and Out- voltages to the underlying N+ poly gates.



EX-1003, ¶166.

¹ There is a dark-blue metal layer located below the yellow fingers. The dark-blue metal layer provides a common voltage Vc and so it is not directly connected to the yellow fingers which supply the Out+ and Out- voltages. EX-1003, ¶¶166, 176.

15. In addition, Gonzalez's Fig. 5 shows a "2x2 differential varactor" (per figure caption), which includes 4 "basic cells." EX-1005.6; EX-1051 (Phinney Dep.).81:7-12. And the F-shaped fingers reside within the 2x2 differential varactor to deliver voltages (Out+, Out-) to each basic cell. Since the overall varactor maps to the claimed "capacitor component," the F-shaped fingers (i.e., yellow fingers in Fig. 8) are part of that "capacitor component."

b. Gonzalez's design rules of six metal layers apply to Fig. 9 and not Fig. 8

16. Realtek and Dr. Phinney also argue that connecting the yellow fingers of Fig. 8 to underlying semiconductor structures "would be at odds with the design rules of Gonzalez, limiting it to 6 metal layers." POR, 32. But this argument misreads Gonzalez. In Gonzalez, the design rules apply to Fig. 9, which permits six metal layers. EX-1005, 8 ("However, to make microstrip lines in CMOS technology, the choices of width and height are also constrained by the technology design rules. Fig. 9 illustrates the realization of a microstrip line using the top metal level (M6) as a conducting strip and the two bottom metal levels (M1 M2) as ground plane.").

17. But Fig. 9 and Fig. 8 use completely different EM modeling approaches. Fig. 9 relates to modeling and studying transmission lines (TLs). *Id.*, 7 ("The TL used in this study is illustrated in Fig. 9.") And this modeling of TLs is "*an alternative modeling approach*" compared to the modeling approach used in

Fig. 8, which is concerned with optimizing the layout of the VCO core. *Id.*

Gonzalez confirms that Fig. 8's modeling approach, i.e., "the previous approach" "is suitable for fixed layout structures," but does not work where "the length of the TLs has to be adjusted in the framework of an optimization process run at schematic level." *Id.*; EX-1051 (Phinney Dep.).77:7-14 (Dr. Phinney confirming the "previous approach" refers to the one used in Fig. 8, and that Fig. 8 and Fig. 9 use different modeling approaches). Therefore, the design rules of Fig. 9 do not apply to the VCO core structure shown in Fig. 8. Indeed, Gonzalez's Fig. 12 confirms that the TLs are not about Fig. 8's VCO core, and that they relate to other parts of the circuit outside the VCO core. Dr. Phinney agreed. EX-1051 (Phinney Dep.).78:6-15, 80:18-81:6.

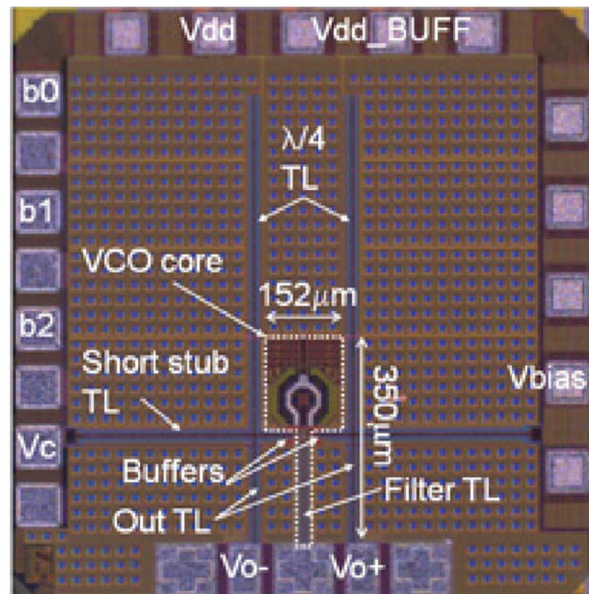


Fig. 12. VCO die micrograph.

EX-1005, Fig. 12.

18. In fact, a POSITA would have appreciated that the design rules of six metal layers cannot apply to Fig. 8. The bottom half of Fig. 8 alone has at least seven metal layers (without adding any layer from elsewhere). POR, 39; EX-1051 (Phinney Dep.).65:22-66:1. If the design rules Realtek and Dr. Phinney identified were relevant to Fig. 8, then Fig. 8 itself would plainly violate them, which would prevent the VCO core structure of Fig. 8 from being simulated and tested. But Gonzalez discloses successful simulation and testing results, EX-1005.7-10, which confirm that Fig. 8's structure satisfied whatever design rules, if any, that applied.

c. Even if not part of any MOS capacitor, Gonzalez's yellow fingers still meet the claimed electrode segments

19. Even assuming Realtek and Dr. Phinney were correct that the yellow fingers are outside of the fine tuning varactor (and they are not), the yellow fingers still meet the claimed electrode segments because, as Dr. Phinney stated, they still provide a "comb structure" that induces a "static capacitance." EX-2003, ¶102. Importantly, Dr. Phinney confirmed in the ITC trial that "after reviewing the '582 patent and the asserted claims, [] a POSITA would conclude that the *claims at issue are purely structural and do not include any functional requirements.*" EX-1049.1273:21-24. Therefore, the yellow fingers are structurally "electrode segments," and the claim limitation is met.

20. Further, the 582 patent discloses multiple stacked capacitor components in an LC circuit. For example, Fig. 12 includes a capacitor component

150 (finger capacitor) and another capacitor component 150' (MOS capacitor).

Claim 1 requires only “a capacitor component.” EX-1051 (Phinney Dep.).11:15-20 (“So if a capacitor component meets the limitations . . . and there happened to be other [capacitor component]s, but I think if you can identify one that meets the limitations in the claim, that would seem to be covered by the claim.”). Similarly, even assuming Gonzalez’s yellow finger capacitor were not part of the fine tuning MOS varactor, it would constitute “a capacitor component” just like capacitor component 150 in Fig. 12 of the patent.

21. But even assuming a functional requirement applied, the yellow fingers still function as electrode segments to induce a “static capacitance.” Realtek and Dr. Phinney argue that Gonzalez aims to minimize this capacitance because “it seeks to minimize the differential current path”. EX-2003, 107; POR, 32-33. This argument is unsupported by Gonzalez,² but even if it were, it is

² Gonzalez does not teach minimizing the “differential current path length” by minimizing the capacitance induced by the yellow fingers. EX-2003, ¶107; POR, 32-33. Rather, as Dr. Phinney agrees, in Gonzalez, the differential current path length is minimized by placement of N+ poly gates in a differential varactor, as shown in Fig. 5. See EX-1005, 6 (“Fig. 5 shows the simplified varactor cross-section and the capacitance and quality factor curves. It is made with two N poly/Nwell varactors. The N poly gates are each connected to one of the two differential terminals (Out+, Out-). They are placed in the same Nwell that is

irrelevant. As is clear from the claim language and as Dr. Phinney confirmed, the claims do not require a threshold amount of capacitance. EX-1051 (Phinney Dep.).40:9-13. It does not matter whether the capacitance is “substantial” or not. POR, 32.

22. Once the layout structure of the yellow fingers are “fixed,” as is the case in Gonzalez’s Fig. 8, the capacitance of the yellow fingers is “static” and so its value is predictable. EX1005-7 (“The previous approach [of Fig. 8] is suitable for *fixed layout structures* requiring EM models.”); EX-1051 (Phinney Dep.).43:9-23, 44:14-24. Therefore a POSITA would know how to account for this capacitance when designing Fig. 8’s LC circuit. Regardless of its capacitance value, this capacitance is one of the design considerations when designing Fig. 8’s LC circuit. EX-1051 (Phinney Dep.).37:10-39:2 (Dr. Phinney acknowledging the capacitance cannot be avoided and needs to be accounted for in designing Gonzalez’s VCO circuit).

23. Realtek and Dr. Phinney’s suggestion that the yellow wires correspond only to the “crossover structure” to convey electric charges (POR, 32) ignores the fact that the same yellow wires serve multiple purposes/functions. As Dr. Phinney agrees, even the 582 patent’s electrode segments also convey electric charges. EX-

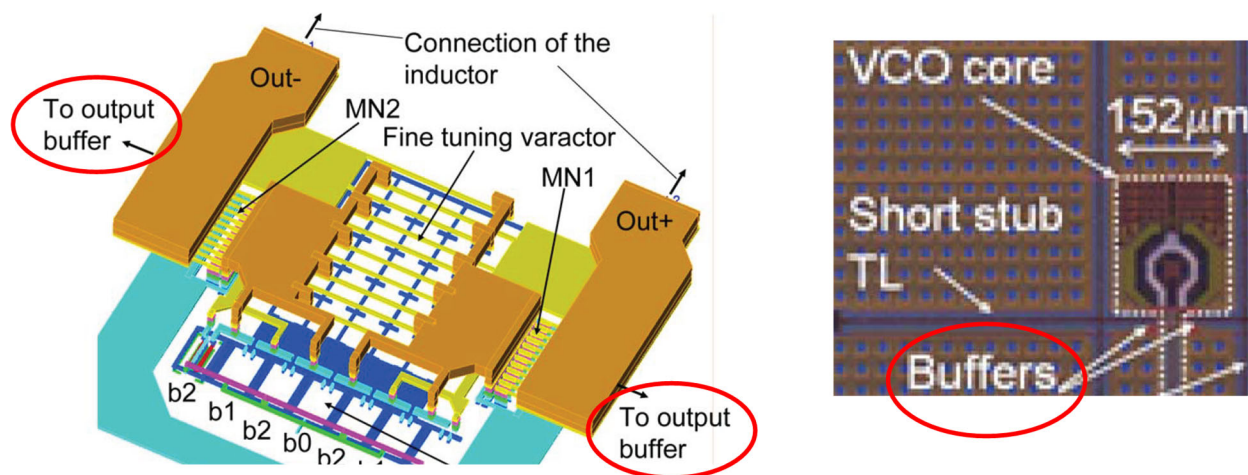
biased using a common voltage (V_c). The differential current path length is *thus* minimized.”). EX-1051.46:9-17, 48:1-6, 91:1-114.

1051 (Phinney Dep.).22:1-21. Indeed, a POSITA would have appreciated that the genius of Gonzalez's design was using the minimal amount of components in a very tight footprint/space to implement its VCO core. For instance, Gonzalez uses the same yellow segments to serve as gate electrodes of the fine tuning varactor, to convey electric charges to the underlying poly gates, to convey electric charges to the discrete tuning varactor bank, and to convey electric charges to the cross-paired transistors, etc. Other than the yellow fingers, Dr. Phinney was unable to identify other structures that connect the inductor to the fine tuning varactor. EX-1051 (Phinney Dep.).56:1-13.

3. Gonzalez's figures and descriptions disclose its capacitor component is not substantially overlapped with its coil-conductor segment

24. In view of the overall disclosure of Gonzalez, it would have been obvious for a POSITA to combine the top and bottom portions of Fig. 8 in a manner that meets the claim. EX-1003, ¶150-152. For example, Gonzalez's Fig. 8 shows its fine tuning varactor is positioned between the two output buffers, and Gonzalez's Fig. 12 shows the two output buffers (whose location are expressly indicated by two white arrows as shown below) are located at the extension-

conductor segments of the inductor, not at the inductor coil.



EX-1005, Fig. 8, Fig. 12 (partial views); EX-1003, ¶152.

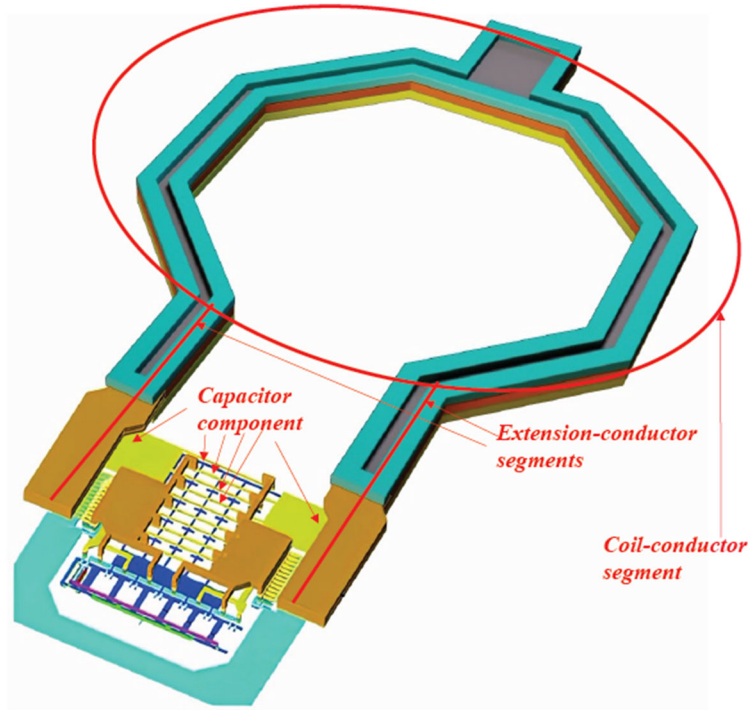
25. PO asserts that Fig. 12 does not show varactors. For one, Fig. 12 does not have sufficient resolution to determine whether it shows varactors. Further, Fig. 12 is a “die micrograph” that captures an image of a physical device that would have all layers and structures present, including a top layer that has metal and insulation portions. And when varactors are located below the top layer (e.g., insulation material directly above the yellow and brown metal wires).

26. The relative positioning of the VCO’s physical structures is further corroborated by Gonzalez’s Fig. 2. Although Gonzalez Fig. 2 does not show exact locations of circuit components and distances between them, it still shows the relative positioning of components (e.g., left, right, center, up, or down). EX-1003, ¶150.

27. Further, in Gonzalez the top half of Fig. 8 shows an “inductor layout,” and the bottom half of Fig. 8 contains “connection of *the* [same] inductor.” A POSITA would recognize the term “connection” here refers to extension-conductor segments of the inductor component. Also, the brown and yellow metal layers appear in both halves of Fig. 8. Realtek and Dr. Phinney rely on the “design rules” to attack against this combination, but as discussed above, the design rules do not even apply to Fig. 8.³

28. Here is a combined view of the top and bottom halves of Fig. 8:

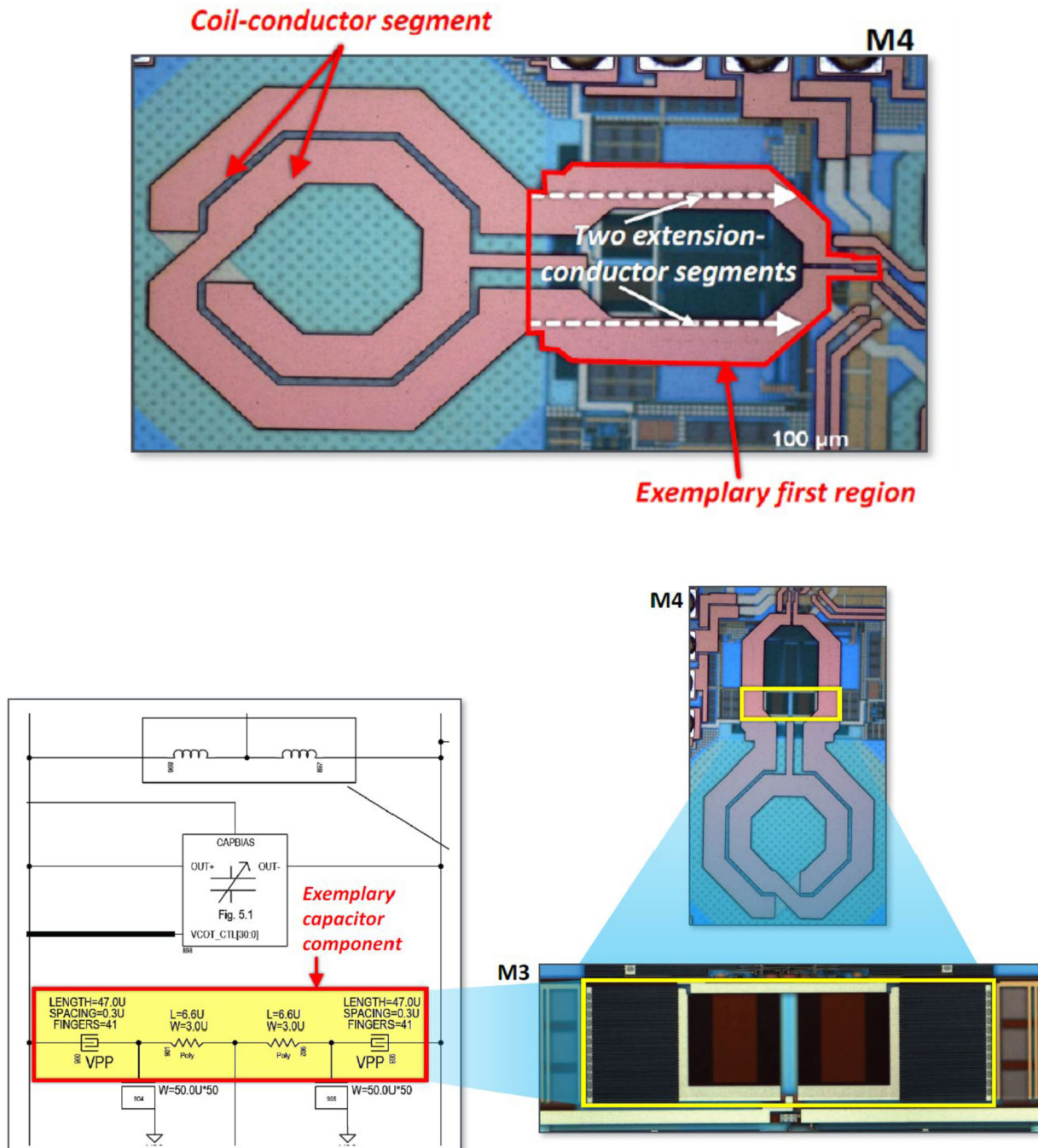
³ Realtek and Dr. Phinney are wrong that “These two portions *could* be combined in a number of different ways that could satisfy the design rules, but many of those ways would have capacitors located below the inductor coil.” POR, 40. As discussed above, the bottom half of Fig. 8 alone would violate the design rules of Fig. 9, so this is another clear indication that Fig. 9’s design rules do not apply to Fig. 8. Realtek and Dr. Phinney did not present a single way where the two portions of Fig. 8 can be combined while keeping a maximum of six metal layers.

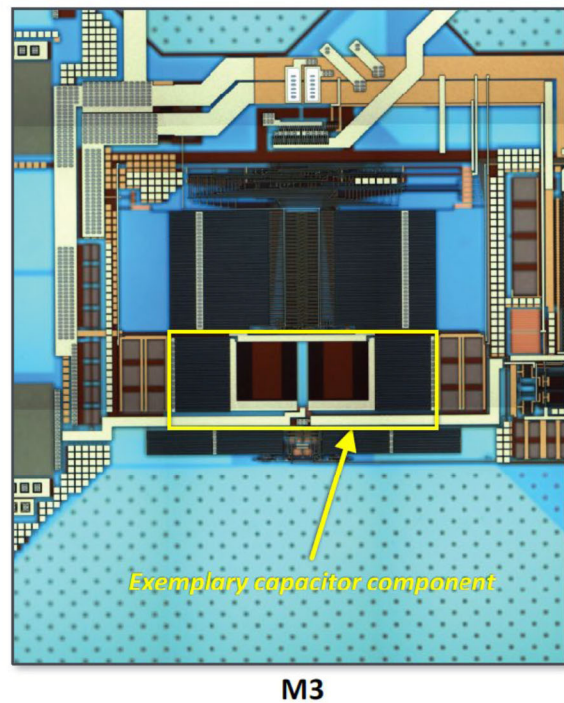
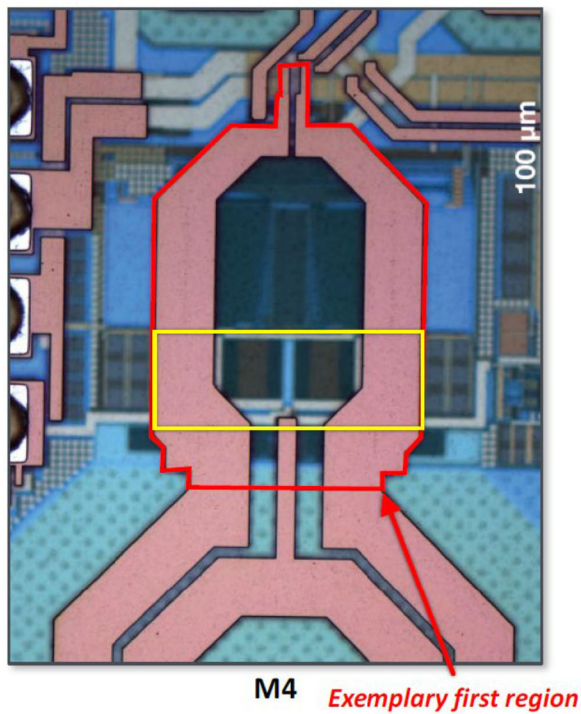
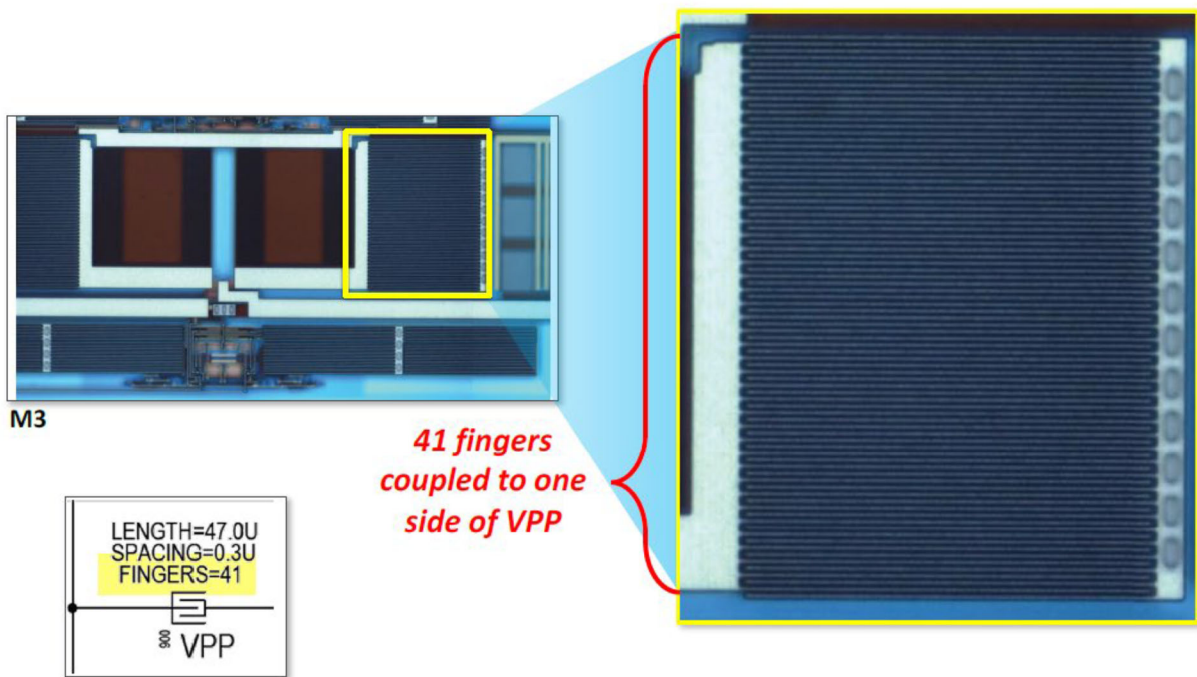


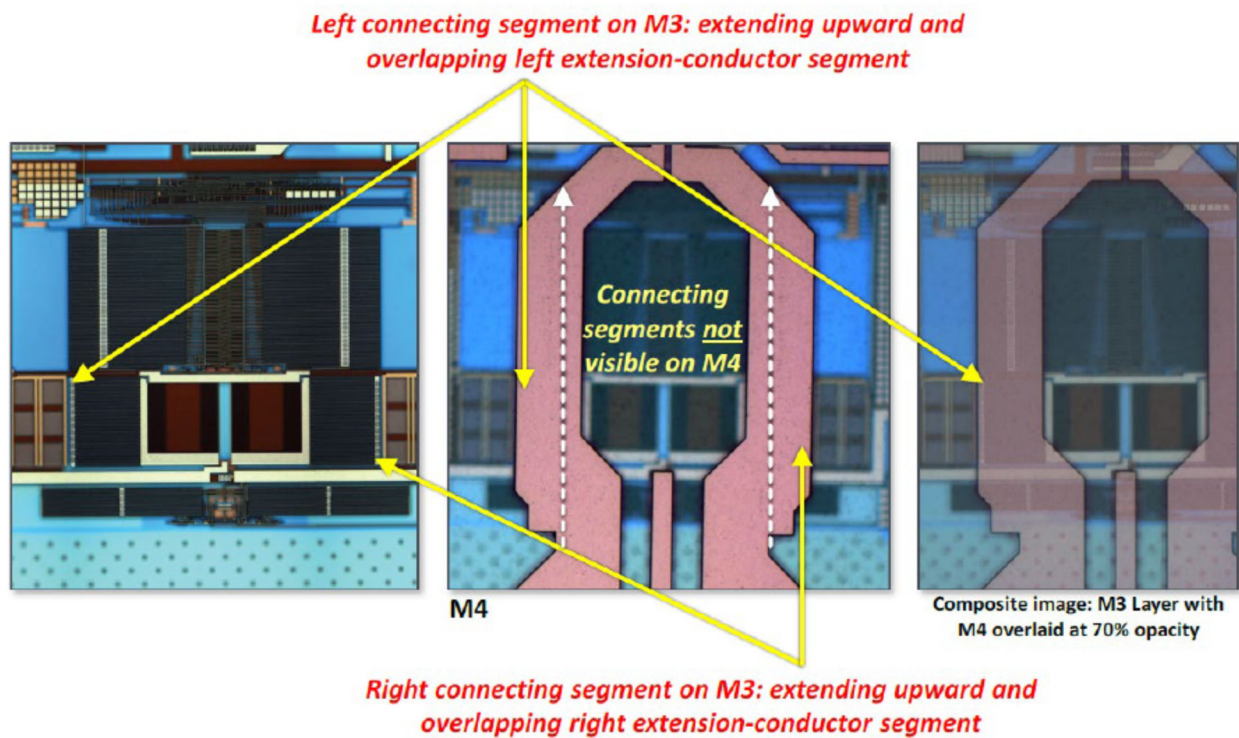
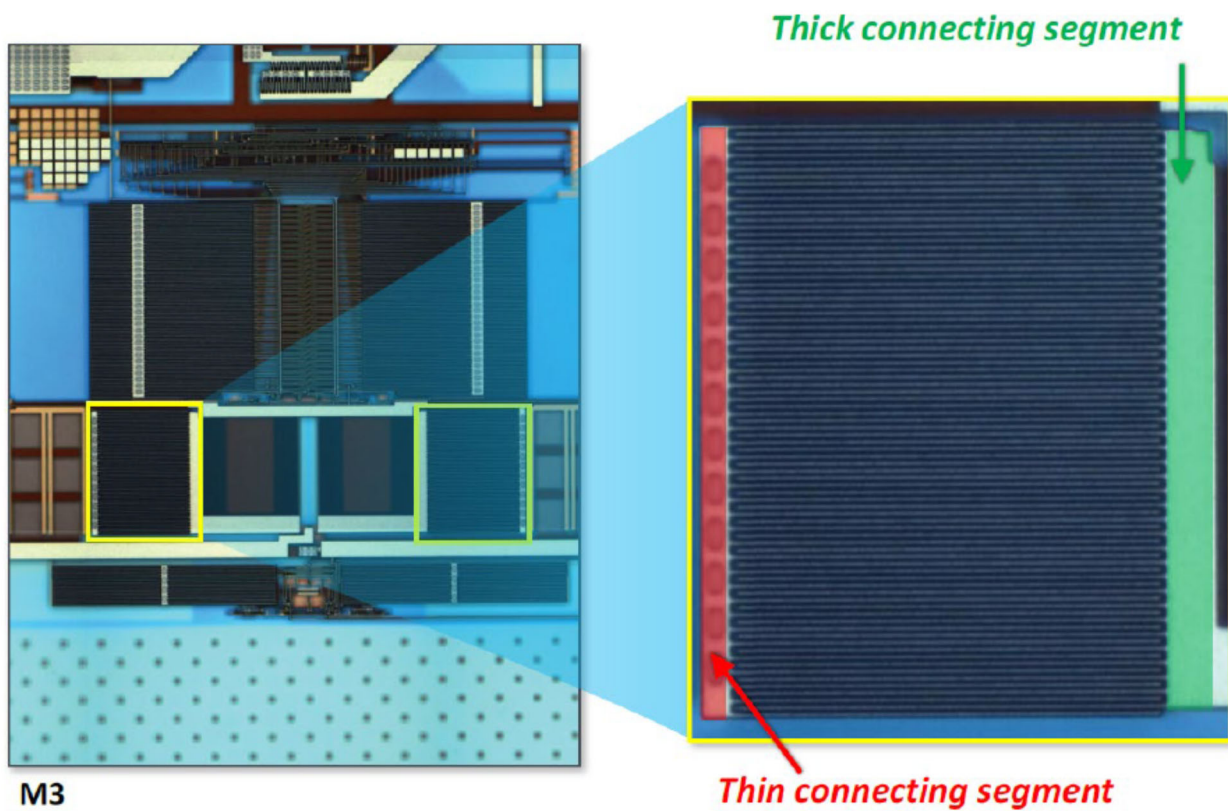
EX-1003, ¶152.

29. A POSITA need not use “the ’582 Patent as a roadmap to piece together the disclosures of Gonzalez,” as Realtek alleges. POR, 40. As illustrated by multiple prior art references, it was well known to design an LC circuit, where a capacitor component is offset from (not substantially overlapped with) the coil-conductor segment of the inductor, and aligned with the extension-conductor segments. E.g., EX-1003, ¶88. Such a spatial relationship had various known benefits. EX-1003, ¶89. Indeed, the ALJ in the parallel ITC proceedings agreed with AMD that a prior art chip Qualcomm RBR1000 invalidates claim 1. Therefore, it would have been obvious for a POSITA to combine the top and bottom portions of Fig. 8 in a manner that met the limitations of claim 1.

30. Specifically, the ALJ found that the prior art Qualcomm RBR1000 (publicly available several years before the 582 filing date) disclosed the same arrangement and anticipated the claims. EX-1048.204-207, .211-219:







EX-1048.213-219; *id.*, .223 (“[A]ll limitations of claim 1 are met in the Qualcomm RBR1000 and claim 1 is invalid as anticipated....”).

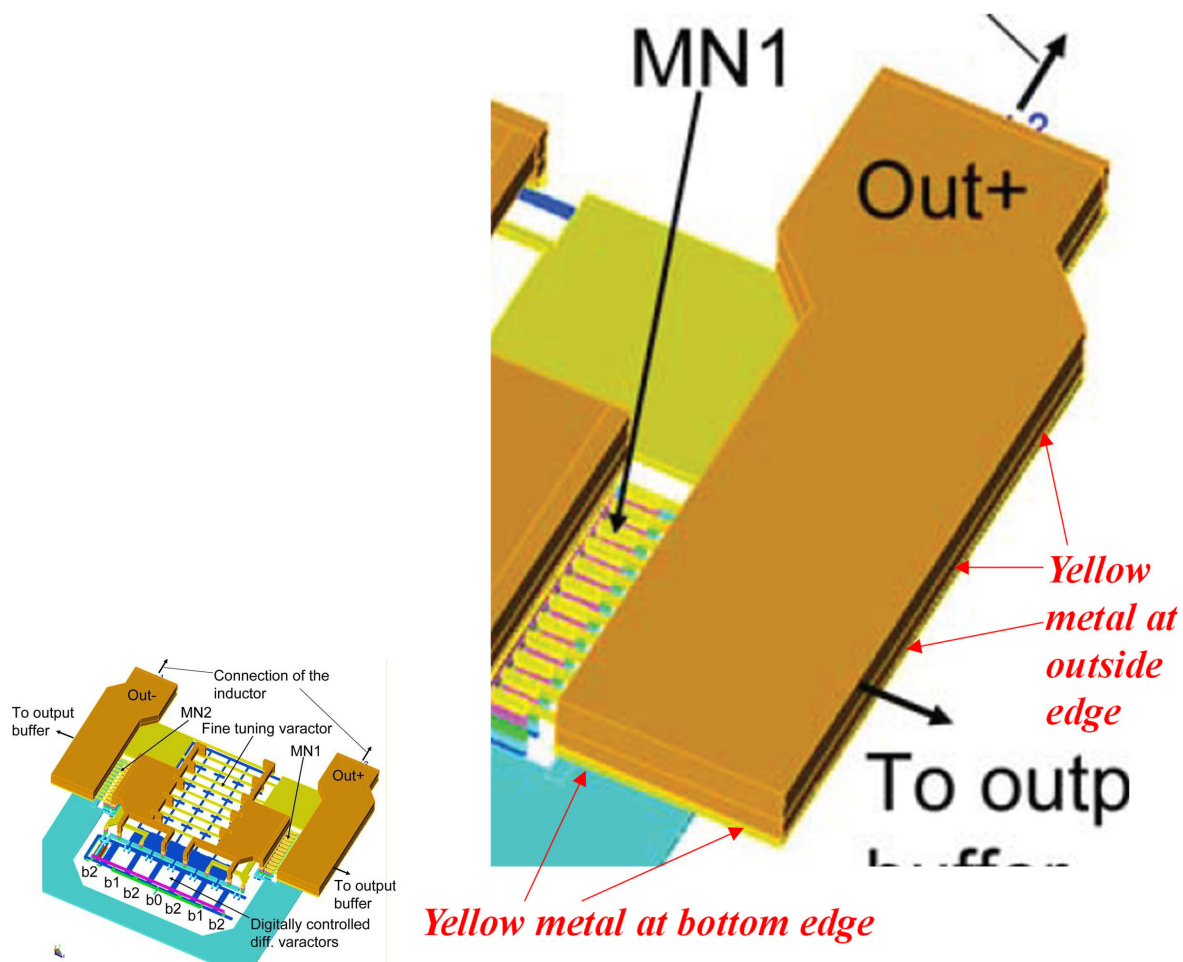
4. Gonzalez’s yellow “connecting segments” meet the claim limitations

31. A POSITA would have been able to discern, based on Gonzalez’s disclosure (including Fig. 8 and Fig. 2) and their knowledge of the art, that Gonzalez’s yellow metal layer would *include* “connecting segments” with certain shapes. EX-1051 (Phinney Dep.).14:18-20 (“Q: What is the ordinary meaning of connecting segment here? A: A segment that connects”). This conclusion is not pure speculation as Realtek argues, but based on the level of skill and knowledge of the art. For example, Dr. Phinney stated that the yellow metal is connected to voltage terminal Out+, but he cannot see direction connection points (e.g., vias) between the yellow and brown metal layers. EX-2003, ¶102; EX-1051 (Phinney Dep.).59:9-21, 61:7-62:17. He nonetheless understood based on his knowledge and understanding in the art that vias would be there.

32. Moreover, consistent with Realtek’s and Dr. Phinney’s infringement analysis in the ITC action, the rectangular shape would extend in the claimed direction. Specifically, Realtek alleged in the ITC proceeding that an L-shaped connecting segment in Petitioner’s products meets the claim. Just like a rectangle, an L-shape extends in multiple directions without a primary direction. Further, Realtek relied on one leg of the L-shape and contended that constituted the claimed

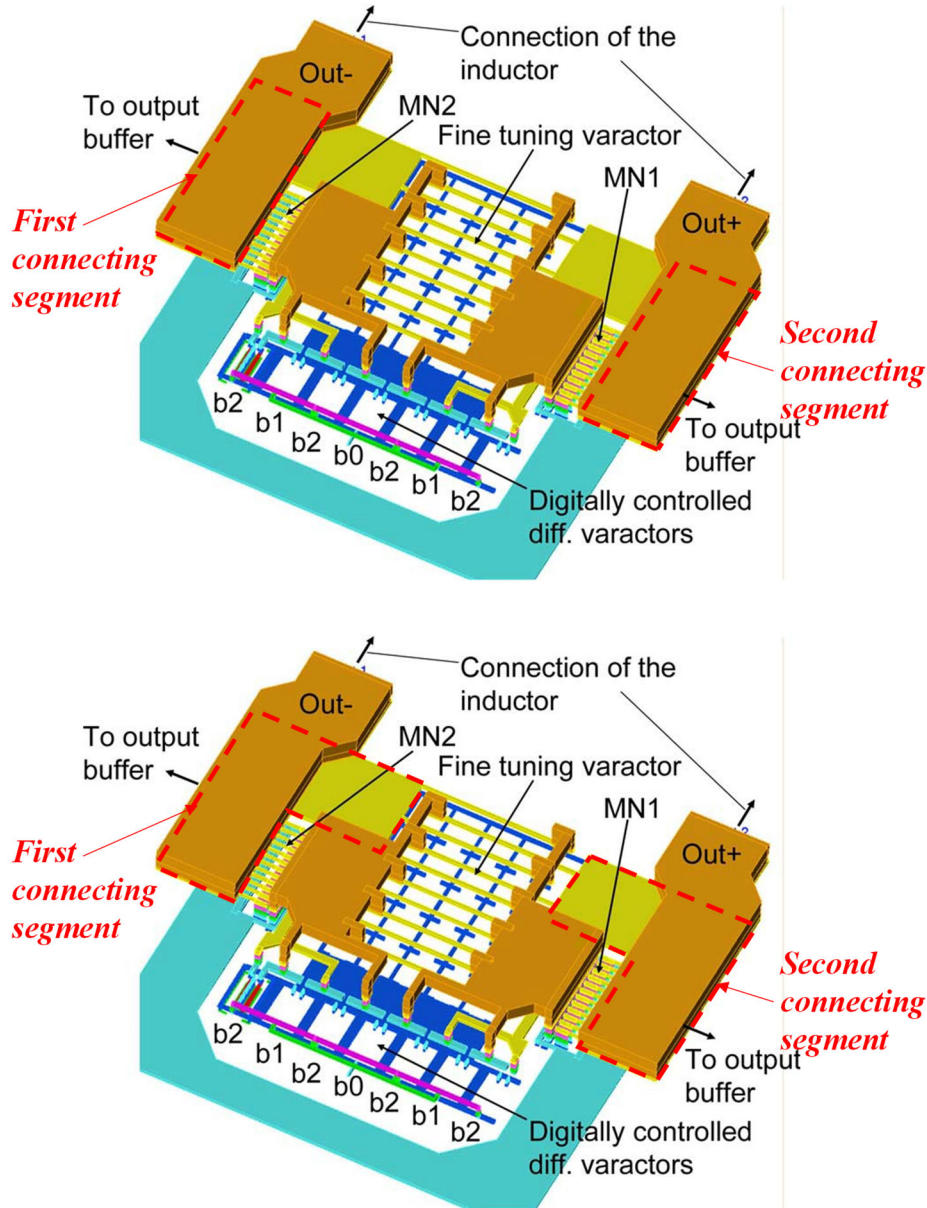
“connecting segment.” Following Realtek’s understanding of the claim language, a POSITA would have understood that any part of the yellow metal in Gonzalez would meet the claimed “connecting segment,” assuming that part extends in the same direction as the extension-conductor segments.

33. Furthermore, when zooming-in on Fig. 8 of Gonzalez, one can see that the yellow metal extends to the bottom edge and outside edge of the brown metal, as illustrated below.



EX-1005, Fig. 8 (with zoom-in view).

layer includes connecting segments shaped as follows:



Id.

35. As I have explained before, a POSITA would have readily recognized either example of the “connecting segments” would meet claim 1’s limitations. EX-1003, ¶¶155-160.

5. Gonzalez discloses an electronic component below its yellow fingers for claims 2 and 3

36. The 582 patent discloses multi-layer capacitors. EX-1001.12:28-36. Dr. Phinney agreed that in a multi-layer capacitor, one layer constitutes a capacitor component. EX-1051 (Phinney Dep.).12:19-24 (“In the case of a multi-layer capacitor, would one layer constitute a capacitor component? THE WITNESS: I think it could be.”).

37. Gonzalez’s fine tuning MOS varactor is a multi-layer capacitor. As shown in Fig. 5, each varactor includes at least a metal layer connected to a voltage terminal Out+ or Out- (F-shaped fingers), a poly gate layer under the metal, a gate oxide (GOX) layer under the poly gate layer, and a bulk silicon layer. EX-1005, Fig. 5. The layer including F-shaped fingers alone constitutes a capacitor component, since it has the structure of a finger capacitor and functions to induce some capacitance. In addition, this layer including F-shaped fingers, along with the poly gate layer, also constitutes a capacitor component.

38. Therefore, the electronic component can be the transistor structure of the bulk silicon layer (e.g., between source and drain). EX-1001.7:34-35 (“The transistor component 170 may be a transistor or *transistor capacitor* operating at

different ranges.”); EX-1051 (Phinney Dep.).29:11-18 (Dr. Phinney appearing to contradict the 582 patent’s teaching by arguing a MOS capacitor is not transistor). The insulation layer is/includes the GOX layer. It meets claim 2.

39. This transistor structure is both a “transistor component” and a “capacitor component.” It meets claim 3. The 582 Patent itself discloses “transistor capacitor” and “MOS capacitor” both of which would encompass the bulk silicon structure shown in Fig. 5 of Gonzalez.

IV. GROUND 2: OBVIOUSNESS BASED ON MUH AND NIKNEJAD

1. Muh

40. Dr. Phinney states that “the focus of Muh is on maximizing the Quality-Factor or Q-factor of its LC circuit,” and therefore has to place a finger capacitor in his proposed orientation in order to decrease “the series resistance of the fingers in its LC circuit” and “improve[] the Q factor of the LC circuit.” EX-2003, ¶¶152, 160, 161, 164. I disagree.

41. The portion of Muh Dr. Phinney cites to support his opinion teaches: “To maximize its Q-factor and minimize its area, L_{tank} was implemented as a center-tapped symmetric inductor rather than two single-ended inductors.” EX-1006.41. That is, Muh teaches that its Q-factor is maximized by implementing an inductor as a center-tapped inductor, not by orienting its finger capacitor in a given orientation. EX-1051 (Phinney Dep.).112:8-12.

42. Further, the LC circuit I rely on in the invalidity ground is shown in Fig. B-3 of Muh, copied below. It shows a single-ended inductor, ***not a center-tapped inductor***. EX-1051 (Phinney Dep.).107:15-20. Therefore, the Q-factor discussion in Muh relied on by Dr. Phinney does not apply to this LC circuit.

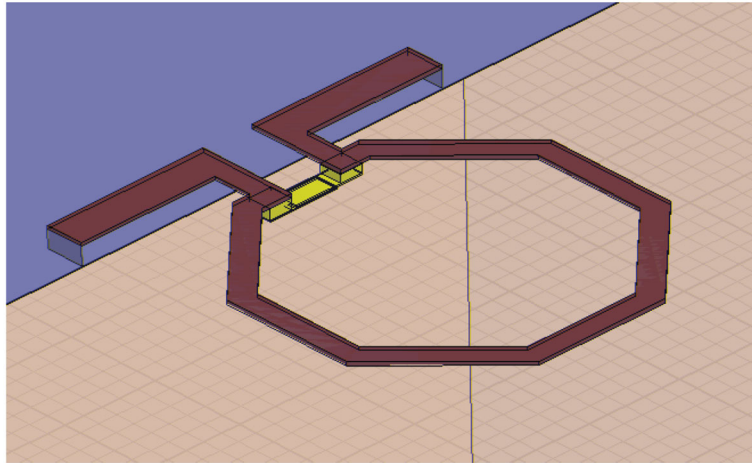


Figure B-3. HFSS model of parallel resonant tank on test chip.

EX-1006.58.

43. Further, the LC resonant tank implemented in Muh’s “test chip” does not have to be part of a VCO. EX-1006.56-58. Indeed, it was a simple simulation of the LC structure. *Id.* Likewise, there is no requirement in the 582 patent claims that the “inductor-capacitor (LC) resonant circuit” identified in claim 1 must be part of a VCO either. EX-1051 (Phinney Dep.).8:21-25 (“Q Does this LC resonant circuit here have to be part of a VCO? [A] It's not part of the claim. It's not a limitation of the claim”). Therefore, not all design considerations for a VCO would apply to either the LC resonant circuit shown in Muh or the one claimed in the 582 patent. And even if the Q factor was taken into account when considering a VCO

design, as Dr. Phinney agrees, a POSITA would have known that maximizing Q is just one of many design considerations for a VCO, such as frequency, tuning range, etc. EX-1051 (Phinney Dep.).93:94:7.

44. Realtek argues that my identification of vias in Muh connecting the inductor to the capacitor is wrong because Muh does not discuss vias. POR, 63. But Muh teaches insulation layers between the inductor and capacitor, and a POSITA would have understood that vias were used to connect them. EX-1003, ¶¶203-206. Moreover, Muh teaches that when using the finger capacitor, “each finger” comprises the “bottom five metal layers strapped together.” EX-1006.057. And Niknejad expressly states that this done through “the maximum number of vias possible.” EX-1007.027. A POSITA would have understood that vias would connect the inductor and capacitor. EX-1003, ¶¶203-206, 212, 224-226, 239-241.

45. Dr. Phinney states that there are certain “design rules” that would prevent Muh from having an LC circuit arranged as claimed. EX-2003, ¶180. I disagree. First, Muh does not discuss any design rules. Second, as Dr. Phinney agrees, Muh’s LC tank (including an interdigitated finger capacitor) already complied with applicable design rules (if any) because a “test chip” was successfully implemented and tested. EX-1051 (Phinney Dep.).122:10-25; EX-1006.056-058. Otherwise, if the finger capacitor did not pass design rules, the LC tank would not have been implemented into the test chip and tested. Therefore, a

POSITA would have understood that replacing the parallel plate capacitor with a finger capacitor in Muh's LC circuit shown in Fig. B-3 would not, and did not, violate any design rules.

2. Niknejad

46. PO argues that the combination of Muh and Niknejad does not read on the claims based on its assertion that "[t]he two references only teach the use of a larger number of shorter fingers." POR, 58-60; EX-2003, ¶165. I disagree.

Niknejad teaches that:

In order to realize a given capacitance, either a large number of short fingers in parallel or a small number of long fingers can be used. The former structure results in smaller finger resistance and inductance but larger lead parasitics due to the transition from the signal lines to the capacitor plates. The latter structure exhibits the opposite tradeoff. This *tradeoff* and the optimum geometry are dependent on the overall capacitor size.

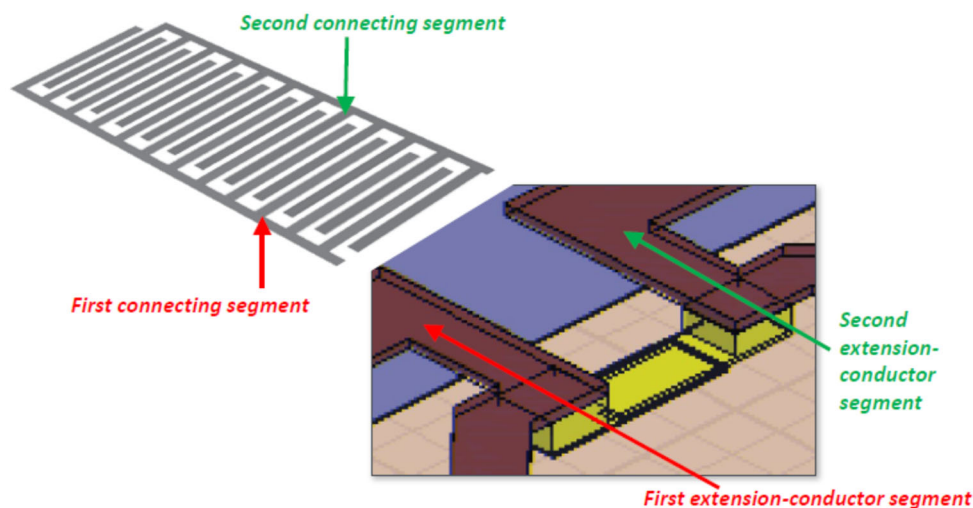
EX-1007.28 (emphasis added).

47. Niknejad discusses both the pros and cons of using "either a large number of short fingers in parallel or a small number of long fingers" but does not instruct a POSITA to only use a large number of shorter fingers. Instead, Niknejad states there is a "tradeoff" to consider. EX-1051 (Phinney Dep.).99:1-5. A POSITA would have known that a small number of long fingers has benefits in an LC circuit. For instance, it would have smaller "lead parasitics," which is one of the alleged goals of the 582 patent. EX-1001, 12:51-54.

48. Realtek selectively cites Niknejad’s chapter 5 to give the impression that VCO design is “unpredictable.” POR, 73-74; Ex.2003, ¶184. But the cited quote concerns “cross-coupled oscillators” and dividers, not a simple LC circuit claimed by the 582 patent. EX-2006.009; EX-1051 (Phinney Dep.).8:17-25, 9:19-22 (Dr. Phinney agreed the claims do not have to be part of a VCO or divider). Moreover, Niknejad was published more than six years before the filing date of the 582 application. EX-1036, ¶¶78-85.

3. The Combination Would Have Been Obvious

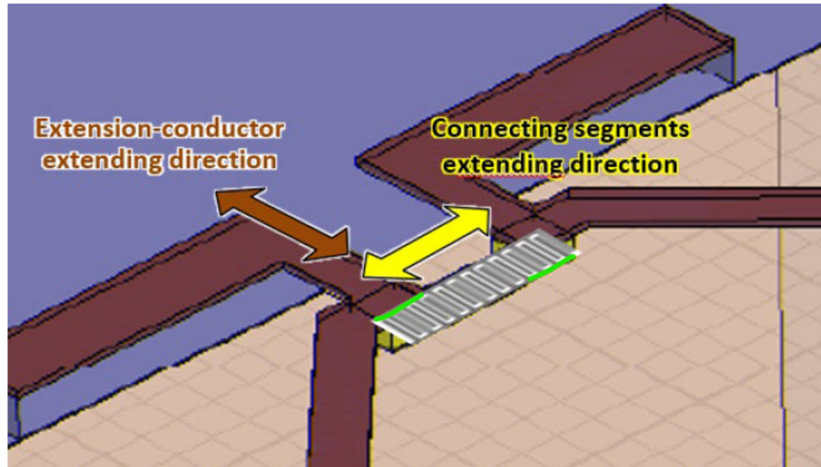
49. The claim requires only that the capacitor is “not *substantially* overlapped” with the coil-conductor segment. When Niknejad’s finger capacitor is substituted in Muh, the capacitor is not substantially overlapped with the coil-conductor segment, as a POSITA would have understood that most of the capacitor would extend outward and away from the coil-conductor segment:



Composite of EX-1006.058, EX-1007.027 (annotated); EX-1003, ¶¶235-236.

50. In my opinion, even when a large number of shorter fingers are used, it remains obvious that the finger capacitor would be arranged in the claimed direction. Indeed, the arrangement as I propose can fit a larger number of fingers because the fingers can simply extend further away from the inductor coil. In contrast, it would be more difficult for the arrangement that Realtek proposes to fit a larger number of fingers because that would result in a larger gap between the two extension-conductor segments, which would affect the performance of the LC circuit (e.g., a lower quality factor, which Dr. Phinney stated was critical in Muh). EX-2003, ¶¶152, 160, 164-165.

51. A POSITA would have recognized that a finger capacitor orientated as proposed by Dr. Phinney would lead to structural asymmetry in the LC circuit. For example, using trench vias of prior art reference Jing, as Dr. Phinney proposes, would lead to one trench via(s) being closer to the inductor coil than the trench other via(s). The difference in proximity to the coil would equal about the width of the capacitor. That is, as illustrated below in green lines, the trench via on the left side would extend further into the extension-conductor segment than the trench via on the right side. This structure would “disrupt bilateral symmetry” per Dr. Phinney and is not ideal because bilateral symmetry is important, as Dr. Phinney agrees. EX-1051 (Phinney Dep.).50:4-11, 118:14-119:1.



Phinney Dep. Ex. 2 (annotated screenshot of Dr. Phinney's figure in EX-2003, ¶161).

V. JURAT

52. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 3rd day of May, 2024 in Princeton, New Jersey.

Dr. Paul R. Prucnal