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IPR2023-00788
U. S. Patent No.
9,590,582

Certification No. 084-003435, 1245

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Jason Snyder, Videographer

* * * * *

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4	EXAMINED BY	
5	Mr. Liu	5
6	* * * * *	
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09:57:49 1 VIDEOGRAPHER: Here begins file number 1,
09:57:50 2 Volume 1 in the deposition of Dr. Joshua Phinney in
09:57:55 3 the matter of Advanced Micro Devices, Inc. versus
09:58:01 4 Realtek Semiconductor Corporation being held in the
09:58:02 5 United States Patent and Trademark Office before the
09:58:06 6 Patent Trial and Appeal Board.

09:58:07 7 Today's date is April 19th of the year 2024.
09:58:10 8 The time is 9:58 a.m. eastern daylight time. This
09:58:14 9 deposition is being taken remotely via the Zoom
09:58:19 10 video conferencing platform and was made at the
09:58:21 11 request for attorneys for the Petitioner.

09:58:23 12 I'm Jason Snyder, the videographer. The
09:58:26 13 court reporter is Sandra Rocca from GregoryEdwards
09:58:28 14 LLC.

09:58:29 15 Counsel, please identify yourselves and
09:58:31 16 state whom you represent, after which the court
09:58:33 17 reporter will please swear in the witness.

09:58:35 18 MR. LIU: For Petitioner AMD, this is
09:58:38 19 Charles Liu of Winston & Strawn.

09:58:41 20 MR. HALVERSON: And for the witness and
09:58:46 21 Patent Owner Realtek, this is Erik Halverson from
09:58:49 22 K&L Gates.

09:58:49 23 JOSHUA PHINNEY, Ph.D.,
09:58:49 24 having been first duly sworn, was examined and
09:58:49 25 testified as follows:

09:58:59 1 CROSS EXAMINATION

09:58:59 2 BY MR. LIU:

09:59:04 3 Q Good morning, Dr. Phinney. Nice to see you

09:59:07 4 again.

09:59:07 5 A Morning. Nice to see you.

09:59:10 6 Q Where are you located this morning,

09:59:14 7 Dr. Phinney?

09:59:14 8 A I'm at the offices of K&L Gates in New York

09:59:18 9 City.

09:59:18 10 Q Sounds good. We're doing this deposition

09:59:26 11 remotely so I want to check real quick. Is there

09:59:29 12 anyone else in the room with you?

09:59:30 13 A Mr. Halverson is here.

09:59:32 14 Q Anyone else connected via chat or texting?

09:59:40 15 A I don't -- I don't have visibility into

09:59:43 16 that. Just I see the video PiPs above the Zoom.

09:59:52 17 Q So you're not talking to anyone else other

09:59:55 18 than Mr. Halverson via like chat or on a computer,

10:00:00 19 right?

10:00:00 20 A Correct.

10:00:02 21 Q Sounds good. So is there any reason that

10:00:06 22 you cannot provide truthful and accurate testimony

10:00:08 23 today?

10:00:09 24 A No.

10:00:11 25 Q I'm sure you're a pro at this already. I

10:00:21 1 don't want to belabor you with the ground rules, but
10:00:23 2 just want to make sure that any time that you don't
10:00:27 3 understand a question from me, could you let me
10:00:31 4 know?

10:00:31 5 A Yes.

10:00:32 6 Q And if you answer my question, I'll assume
10:00:37 7 that you heard it, understood it and answered to the
10:00:40 8 best of your ability. That sounds good?

10:00:46 9 A Yes.

10:00:47 10 Q Dr. Phinney, what did you to prepare for
10:00:52 11 your deposition today?

10:00:54 12 A I met with Mr. Halverson on Wednesday and
10:00:59 13 briefly yesterday.

10:01:04 14 Q How long did you meet with Mr. Halverson?

10:01:17 15 A Maybe a total of five hours.

10:01:22 16 Q Five hours for just today's deposition or
10:01:28 17 including the deposition for yesterday?

10:01:31 18 A Basically for today's deposition, I worked
10:01:35 19 with two attorneys and then they had divided what
10:01:40 20 patent they were focused on, so that five hours
10:01:44 21 would be the time for the '582 patent.

10:01:48 22 Q Did you bring any notes with you today?

10:01:54 23 A No.

10:01:55 24 Q Did you bring documents with you today?

10:01:57 25 A No.

10:01:59 1 Q Sounds good. So you mentioned the '582 so
 10:02:13 2 today we will be covering the '582 patent. This is
 10:02:18 3 U.S. Patent Number 9,590,582. Let me actually
 10:02:24 4 upload that document. I already uploaded it.
 10:02:24 5 (Document marked previously as
 10:02:30 6 Exhibit 1001 was presented.)
 10:02:30 7 BY MR. LIU:
 10:02:30 8 Q Do you see Exhibit 1001, the '582 patent?
 10:02:36 9 A Yes, I have it downloaded.
 10:02:37 10 Q Thank you. So this patent will be the one
 10:02:41 11 we talk about. And unless we otherwise specify, the
 10:02:47 12 patent and its claims will be the subject of today's
 10:02:50 13 deposition. Sound good?
 10:02:52 14 A Yes.
 10:02:52 15 Q Fair to say that you have looked at this
 10:02:58 16 patent many times by now?
 10:02:59 17 A Yes.
 10:03:00 18 Q And you have previously testified about this
 10:03:06 19 patent at a Trade Commission hearing, correct?
 10:03:10 20 MR. HALVERSON: Objection, form.
 10:03:13 21 THE WITNESS: Yes.
 10:03:14 22 BY MR. LIU:
 10:03:17 23 Q And your opinions at the Trade Commission
 10:03:20 24 hearing are still your testimony -- are still your
 10:03:23 25 opinions today?

10:03:28 1 A Yeah, I think that's fair.

10:03:30 2 Q No need to change anything?

10:03:36 3 A Yeah, that's right.

10:03:39 4 Q And you were also deposed in that Trade

10:03:45 5 Commission proceeding about this patent, correct?

10:03:48 6 A Yes.

10:03:49 7 Q And do you stand by your deposition

10:03:52 8 testimony from that proceeding?

10:03:54 9 A Yes.

10:03:56 10 Q Sounds good. So could we go to claim 1 in

10:04:06 11 this patent? It's in column 12.

10:04:13 12 A I'm there.

10:04:14 13 Q So claim 1 recites a semiconductor device

10:04:27 14 with an inductor-capacitor LC resonant circuit. Do

10:04:33 15 you see that?

10:04:34 16 A Yes.

10:04:34 17 Q So claim 1 doesn't recite a VCO, right?

10:04:49 18 A That's right.

10:04:53 19 Q And do you know what VCO stands for?

10:04:57 20 A Yes, voltage controlled oscillator.

10:05:04 21 Q Does this LC resonant circuit here have to

10:05:10 22 be part of a VCO?

10:05:14 23 MR. HALVERSON: Objection, form.

10:05:15 24 THE WITNESS: It's not part of the claim.

10:05:20 25 It's not a limitation of the claim.

10:05:25 1 BY MR. LIU:

10:05:36 2 Q Does it have to be part of a divider?

10:05:41 3 A Make sure I heard your question. I didn't
10:05:45 4 maybe hear that last word.

10:05:46 5 Q Does the claimed LC circuit have to be part
10:05:51 6 of a divider circuit?

10:05:55 7 MR. HALVERSON: Objection, form.

10:05:56 8 THE WITNESS: Maybe you could be more
10:06:00 9 specific.

10:06:01 10 BY MR. LIU:

10:06:01 11 Q Do you know what is a divider circuit?

10:06:04 12 A There are several things called divider
10:06:07 13 circuits. So I'm just -- are you talking about like
10:06:10 14 a frequency divider or something like that?

10:06:13 15 Q Yeah. Are you familiar with a frequency
10:06:15 16 divider circuit?

10:06:17 17 A Yeah, like where a VCO is part of a phase
10:06:21 18 lock loop.

10:06:22 19 Q Right. So for instance, does the LC circuit
10:06:25 20 here have to be part of a frequency divider circuit?

10:06:30 21 A No, it's not an embodiment -- sorry. It's
10:06:32 22 not a limitation of the claim.

10:06:40 23 Q Going down in claim 1, it claims an inductor
10:06:48 24 component. Do you see that?

10:06:49 25 A Yes.

10:06:50 1 Q And further down it claims a capacitor
10:06:56 2 component. Do you see that?

10:06:57 3 A Yes.

10:06:58 4 Q So Dr. Phinney, an LC circuit can have
10:07:16 5 multiple capacitor components, is that right?

10:07:23 6 A Yeah, I think that's right. You could have
10:07:31 7 embodiments with multiple capacitor components.

10:07:35 8 Q And the multiple capacitor components, they
10:07:44 9 together can provide the capacitance for the LC
10:07:49 10 circuit, right?

10:07:56 11 MR. HALVERSON: Objection, form.

10:07:57 12 THE WITNESS: I think that's -- if they're
10:08:03 13 connected in parallel, they could together provide a
10:08:05 14 capacitance or an LC resonant circuit.

10:08:14 15 BY MR. LIU:

10:08:14 16 Q Here in claim 1, if a capacitor component is
10:08:17 17 one of several capacitor components in the LC
10:08:22 18 circuit, would that meet claim 1?

10:08:26 19 MR. HALVERSON: Objection, form, beyond the
10:08:27 20 scope.

10:08:29 21 THE WITNESS: You know, I do recall
10:08:40 22 discussing these kind of issues in the ITC hearing
10:08:45 23 where we were concerning -- comparing particular
10:08:48 24 embodiments to the claims. But you know, I don't
10:08:55 25 think this is in my declaration now in this -- in

10:08:58 1 this IPR.

10:09:01 2 BY MR. LIU:

10:09:01 3 Q But do you have an opinion on that?

10:09:06 4 A Maybe if you could ask it again.

10:09:09 5 Q If a capacitor component is one of several
10:09:13 6 capacitor components in the LC circuit, would that
10:09:17 7 meet claim 1?

10:09:19 8 MR. HALVERSON: Objection, form, beyond the
10:09:20 9 scope. Charles, we'll have a little bit of leeway
10:09:26 10 on this, but this is not going to be an opportunity
10:09:28 11 to rehash the initial determination from the ITC
10:09:31 12 case in the context of Dr. Phinney's deposition.

10:09:36 13 MR. LIU: I'm not trying to do that here.
10:09:38 14 This is totally within the scope of the IPR.

10:09:44 15 THE WITNESS: So if a capacitor component
10:09:47 16 meets the limitations — and I think you're kind of
10:09:53 17 asking if there's just one and there happened to be
10:09:56 18 others, but I think if you can identify one that
10:09:58 19 meets the limitations in the claim, that would seem
10:10:04 20 to be covered by the claim.

10:10:06 21 BY MR. LIU:

10:10:21 22 Q And the '582 patent also allows multi-layer
10:10:26 23 capacitor components, right?

10:10:34 24 MR. HALVERSON: Objection, form.

10:10:35 25 THE WITNESS: I'm not aware of a limitation

10:10:43 1 that like restricts the capacitor component to have
10:10:53 2 only one layer, for instance.

10:10:57 3 BY MR. LIU:

10:11:09 4 Q So if we have a multi-layer capacitor, could
10:11:29 5 one layer of that multi-layer capacitor constitute a
10:11:33 6 capacitor component?

10:11:38 7 MR. HALVERSON: Objection, form. Beyond the
10:11:40 8 scope of Dr. Phinney's IPR declaration.

10:11:44 9 THE WITNESS: I recall in the ITC
10:11:51 10 proceeding, you know, we were talking about this a
10:11:52 11 lot. And we also had a construction, you know, so
10:11:56 12 that a capacitor component was -- I think it was
10:12:01 13 construed to mean a component that had one or more
10:12:04 14 capacitors. I think it was the subject of a
10:12:08 15 construction. And I just don't recall this being a
10:12:15 16 -- this is not part of the declaration I offer now
10:12:18 17 for -- in this IPR proceeding.

10:12:24 18 BY MR. LIU:

10:12:25 19 Q I'm asking based on your understanding of
10:12:27 20 this patent. In the case of a multi-layer
10:12:33 21 capacitor, would one layer constitute a capacitor
10:12:35 22 component?

10:12:39 23 MR. HALVERSON: Same objection.

10:12:40 24 THE WITNESS: I think it could be.

10:13:10 25 ///

10:13:10 1 BY MR. LIU:

10:13:11 2 Q Moving further down in claim 1, it says

10:13:16 3 wherein the capacitor -- strike that. Sorry.

10:13:21 4 Wherein the capacitor component comprises a

10:13:24 5 plurality of connecting segments. Do you see that?

10:13:39 6 It's in column 13, line 29 -- line 19 to 20.

10:13:47 7 A Yes, I see that.

10:13:48 8 Q So here in your opinion, what is an

10:13:58 9 electrode segment?

10:14:01 10 A You did ask electrode segment, so the next

10:14:21 11 element?

10:14:24 12 Q I'm sorry. Yeah. I should have finished

10:14:27 13 the whole limitation. So on line 26, it also

10:14:33 14 mentions the capacitor component comprises a

10:14:40 15 plurality of electrode segments. Do you see that?

10:14:44 16 A Yes.

10:14:44 17 Q My first question is so in your opinion,

10:14:49 18 what is a connecting segment?

10:14:51 19 A Well, it's this segment for connecting and

10:15:07 20 it has the limitations described here. It's

10:15:13 21 connecting electrode segments and it is also

10:15:20 22 overlapped by extension-conductor segments, so it

10:15:24 23 has these other limitations here.

10:15:29 24 Q So is there anything that connects the

10:15:39 25 electrode segment and also overlapped by

10:15:41 1 extension-conductor segment is a connecting segment?

10:15:46 2 MR. HALVERSON: Objection, form.

10:15:47 3 THE WITNESS: I maybe missed a word at the
10:15:52 4 beginning of the question. I'm sorry. If you could
10:15:53 5 just -- if you could repeat that.

10:15:57 6 BY MR. LIU:

10:15:57 7 Q So anything that connects the electrode
10:16:01 8 segment and also overlapped by the
10:16:05 9 extension-conductor segment is a connecting segment?

10:16:11 10 MR. HALVERSON: Objection, form.

10:16:12 11 THE WITNESS: No. What I'm trying to
10:16:14 12 indicate is that the connecting segment is -- you
10:16:19 13 know, I think it just has its plain meaning and its
10:16:23 14 ordinary and customary meaning and it's got these
10:16:26 15 limitations here in the claim. So there's more
10:16:30 16 limitations.

10:16:31 17 BY MR. LIU:

10:16:31 18 Q What is the ordinary meaning of connecting
10:16:34 19 segment here?

10:16:38 20 A A segment that connects; you know, something
10:16:44 21 like that. It's just the words themselves I think
10:16:46 22 are the best guide for the scope of what that is.

10:16:49 23 Q What is your understanding of an electrode
10:17:04 24 segment?

10:17:06 25 A One way to think of this is it of course has

10:17:50 1 to have the limitations that are listed here. But
10:17:52 2 one way to think of this in the context of these
10:17:55 3 interdigitated finger capacitors, also called
10:17:59 4 metal-oxide-metal capacitors, is that it is the
10:18:06 5 structures between which the electric field exists
10:18:09 6 to make a designed capacitance. That's how you
10:18:13 7 design the capacitance of the capacitor component is
10:18:17 8 to create these electrode segments that have an
10:18:22 9 electric field between them and a designed
10:18:26 10 capacitance.

10:18:29 11 Q So you mentioned designed capacitance
10:18:33 12 several times. So are you saying that it has to
10:18:37 13 function as a designed capacitor?

10:18:40 14 A Yeah, more or less. I mean, it's -- that's
10:19:09 15 how the capacitance is made is with the electric
10:19:15 16 field between those electrode segments. So a person
10:19:19 17 of ordinary skill knows that by laying out those
10:19:21 18 electrode segments, that's how they're making the
10:19:26 19 capacitance of the capacitor component.

10:19:31 20 Q I think you gave the example of an
10:19:47 21 interdigitated finger capacitor. Could the
10:19:51 22 electrode segment exist in other types of
10:19:54 23 capacitors?

10:19:57 24 A There could be other examples I suppose that
10:20:25 25 meet the limitations. Really the one that comes to

10:20:30 1 mind is, you know, this plurality of electrode
10:20:35 2 segments. It's depicted in the patent as sort of
10:20:39 3 like a comb, like the teeth of a comb that
10:20:43 4 interdigitate with fingers of another part of the
10:20:52 5 capacitor structure.

10:20:54 6 Q Is that the only example you recall from the
10:20:56 7 patent? So strike that.

10:21:44 8 To save some time, Dr. Phinney, so for
10:21:47 9 example, in a parallel plate capacitor, would there
10:21:51 10 be electrode segments that generate the electric
10:21:54 11 field between them to make a designed capacitance?

10:22:04 12 A You could think of plates as being
10:22:43 13 electrodes and as long as you could identify a
10:22:45 14 plurality of them, they would have to meet all the
10:22:48 15 limitations in the claim, but you could consider the
10:22:52 16 plates to be electrodes of a capacitor.

10:22:55 17 Q I'd like to look at an example of electrode
10:23:08 18 segments. Could you see to Figure 9 in this patent?
10:23:12 19 It's on page 11 of the Exhibit 1001.

10:23:20 20 A Okay, I'm there.

10:23:22 21 Q Here do you see capacitor component 150 in
10:23:43 22 the middle of the figure?

10:23:47 23 A Yes.

10:23:47 24 Q Do you see connecting segments 151 and 152?

10:24:08 25 A Yes.

10:24:09 1 Q Do you see electrode segments 155, 156, 157,
10:24:18 2 158?

10:24:21 3 A Yes.

10:24:28 4 Q Here based on your understanding of the LC
10:24:54 5 circuit shown in Figure 9, how would the electric
10:25:00 6 voltage get delivered to this capacitor component
10:25:03 7 150?

10:25:05 8 A If I could just hear that again. I think I
10:25:11 9 missed a word.

10:25:12 10 Q Sorry. Let me back up a little.

10:25:17 11 So this capacitor, component 150, it works
10:25:22 12 with the inductor on top as part of an LC circuit,
10:25:27 13 right?

10:25:33 14 A I mean, you'd hope.

10:25:50 15 Q So if the LC circuit includes the inductor
10:25:56 16 and the capacitor component, my question is how does
10:26:04 17 the capacitor component 150 get the voltage from the
10:26:12 18 output of the inductor, even though I understand
10:26:18 19 that the connections are not completely shown here,
10:26:21 20 but as an expert in the field, how would you think
10:26:24 21 the voltage gets delivered to the capacitor
10:26:29 22 component 150?

10:26:33 23 A Well, one thing I see is that the capacitor
10:26:37 24 150 really includes three separate and unconnected
10:26:46 25 pieces of metal. And so as it's drawn now, those

10:26:53 1 connecting segment parts that we looked at, 151 and
10:26:56 2 152, aren't connected to anything. So you know, to
10:27:04 3 not have an undefined potential -- you know, I
10:27:09 4 presume there would be some sort of connection. It
10:27:15 5 could be -- you know, it doesn't have to go back to
10:27:20 6 the inductor necessarily. It could be a series
10:27:22 7 connection. But there needs to be a complete
10:27:25 8 circuit for this to -- for that capacitor to be --
10:27:30 9 really function as a capacitor.

10:27:32 10 Q So would it be reasonable to say there could
10:27:40 11 be a connection, for example, between the connecting
10:27:45 12 segment 151 and the extension-conductor segment 133
10:27:50 13 on top of it?

10:27:54 14 A So that's not shown. You don't need to do
10:27:57 15 that because that would put -- that would make sort
10:28:00 16 of a parallel connection. But you can have a series
10:28:05 17 connection. You know, you could have a connection
10:28:10 18 to ground or some other node so that you're
10:28:16 19 providing a path through both components, but not
10:28:18 20 where both -- the inductor component and capacitor
10:28:22 21 component are connected in parallel.

10:28:24 22 Q Sure. So in the series connection, so the
10:28:36 23 voltage or electric charge would flow down from --
10:28:42 24 induct from the inductor down by via 191, is that
10:28:49 25 right?

10:28:49 1 A Yeah, so you'd say current flows or charge
10:28:52 2 flows. And you can sometimes I guess talk about
10:28:57 3 voltage flowing, but we prefer to talk about current
10:29:03 4 or charge being the things that are the flow
10:29:06 5 variable.

10:29:06 6 Q Sounds good. So electric charges would flow
10:29:11 7 from the inductor to the connecting segment 151
10:29:18 8 through via 191, is that fair?

10:29:22 9 A Yeah, you could say it that way. And
10:29:25 10 typically these are AC circuits, so that the charge,
10:29:28 11 you could think of it, kind of never gets there.
10:29:31 12 It's oscillating back and forth and you still talk
10:29:35 13 about that though as being a current that has a
10:29:37 14 direction.

10:29:38 15 Q So current would flow from the inductor
10:29:44 16 through via 191 to the connecting segment 153?

10:29:52 17 A That's one option. You can -- you can think
10:29:59 18 of current going the other way too. But in that
10:30:03 19 series connection idea that I'm talking about, yeah,
10:30:06 20 you can -- there can be driving terminals where
10:30:13 21 there's no further connection between an inductor
10:30:16 22 and capacitor and that still can make a useful
10:30:20 23 resonant circuit.

10:30:22 24 Q So connecting segment 153 would carry the
10:30:36 25 electric charges in that AC operation, for example,

10:30:43 1 right?

10:30:45 2 A That's right. In AC operation, the actual
10:31:01 3 individual charge will actually drift one direction
10:31:04 4 and then go back the other. The charge will sort of
10:31:09 5 oscillate back and forth. And --

10:31:15 6 Q But they would flow -- sorry.

10:31:18 7 A No, no. Sorry. Go ahead.

10:31:20 8 Q But I understand that the electric charges
10:31:23 9 would, you know, go back and forth in an AC
10:31:26 10 operation, but they would flow through connecting
10:31:29 11 segment 153, right?

10:31:31 12 A You can think of it like that. It's like --
10:31:35 13 it's that oscillatory behavior of charges. They'll
10:31:41 14 tend to have a quite slow actually drift velocity.
10:31:46 15 But the way a current signal propagates through
10:31:50 16 there, it's almost like billiard balls that are kind
10:31:54 17 of like sort of aligned next to one other. So if I
10:32:00 18 push on one billiard ball, it will make the last one
10:32:03 19 in the chain move, so there's actually quite fast
10:32:07 20 travel of current or a wave through the charge
10:32:09 21 carriers. The charge carriers themselves actually
10:32:12 22 kind of move and oscillate quite slowly actually in
10:32:18 23 the -- as part of that process.

10:32:19 24 Q Thank you. So if we look at electrode
10:32:27 25 segments 157 and 158 here, they are connected to the

10:32:35 1 connecting segment 153. Do you see that?

10:32:38 2 A Okay, can you just say that again? I'm
10:32:40 3 looking at the figure now.

10:32:42 4 Q Electrode segments 157 and 158, they are
10:32:48 5 both connected to that center connecting segment
10:32:54 6 153. Do you see that?

10:32:55 7 A Yes. And to be clear, I'm looking in 150,
10:32:59 8 not 150 prime.

10:33:02 9 Q Yeah, in Figure 9, right?

10:33:05 10 A Oh, gosh. So sorry. Yeah, excuse me. I
10:33:13 11 was -- for some reason I was on Figure 12. Yeah, I
10:33:16 12 see what you're talking about.

10:33:18 13 Q So the electric charges would also flow
10:33:27 14 through the electrode segments 157 and 158, right?

10:33:41 15 A I'd give the same kind of answer. They --
10:33:44 16 you know, don't think of it like a DC. You know,
10:33:47 17 it's not like the charge carriers go and continue to
10:33:53 18 flow. They would have that same oscillatory
10:33:56 19 behavior that I described. They would cause induced
10:34:01 20 charges across the gap between electrode segments.
10:34:07 21 And that's how you know that process goes further.

10:34:11 22 We say the current actually goes through the
10:34:13 23 capacitor and that happens through that induced
10:34:19 24 charges across the gap, sometimes called a
10:34:21 25 displacement current.

10:34:23 1 Q Sure. So when the current goes through that
10:34:27 2 capacitor, so the electrical charges would flow
10:34:32 3 through these electrode segments 157 and 158, for
10:34:37 4 example, right?

10:34:38 5 A Yeah, you could think of it like that.
10:34:41 6 Another way to imagine this is that there's going to
10:34:50 7 be excess surface charge on the electrodes. So when
10:34:51 8 they have that kind of oscillatory behavior and when
10:34:54 9 sort of an excess of charge gets -- there's excess
10:35:00 10 surface charge on the surface of one of the
10:35:02 11 electrodes and there will be like, let's say,
10:35:04 12 negative charge carriers, which you expect in metal,
10:35:06 13 that will be a negatively charged surface of that
10:35:09 14 electrode. It will induce a positive charge on the
10:35:12 15 other side. It will tend to exclude electrons from
10:35:16 16 surface states on the other electrode.

10:35:19 17 So that sort of -- remember I was talking
10:35:22 18 about billiard balls pushing, that kind of pushing
10:35:27 19 and redistribution of charge over these small scales
10:35:31 20 will continue to happen across the gap between
10:35:36 21 electrodes.

10:35:38 22 Q Thank you. That's helpful. Here if we stay
10:36:04 23 with the electrode segments 157 and 158, for
10:36:07 24 example, do you think those are metal wires?

10:36:23 25 A You could call them that, but the patent

10:36:26 1 calls them electrode segments. And one reason is
10:36:30 2 that the -- you know, they're there to create the
10:36:33 3 design capacitance of this capacitor structure. So
10:36:37 4 a person of ordinary skill understands that they're
10:36:39 5 there to define the electric field region which is
10:36:43 6 how the energy is stored in this capacitor.

10:36:52 7 Q What about that via 191, would you call that
10:36:56 8 a metal wire?

10:37:00 9 MR. HALVERSON: Objection, form.

10:37:01 10 THE WITNESS: In this context, I call it a
10:37:06 11 via. I can understand why you'd call it a metal
10:37:09 12 wire because it's, you know, a piece of metal. But
10:37:13 13 you know, it's called a via in this context.

10:37:23 14 BY MR. LIU:

10:37:24 15 Q How about that center tap 140, is that a
10:37:27 16 metal wire?

10:37:29 17 MR. HALVERSON: Same objection.

10:37:29 18 THE WITNESS: Well, it's got, you know, a
10:37:33 19 special name, the center tap. You know, I can
10:37:36 20 understand why you'd want to call it a metal wire
10:37:39 21 because it's a piece of metal laid out on one of the
10:37:42 22 metal layers. But it's -- you know, it has a
10:37:48 23 special name in this -- in this patent.

10:37:53 24 BY MR. LIU:

10:37:58 25 Q You said a special name. Did you mean that

10:38:01 1 the patentee gave it a special meaning here?

10:38:03 2 A No, not a special meaning, but it's called a
10:38:06 3 tap segment. And you know, I can understand why --
10:38:11 4 when people will say the tap segment is a wire.
10:38:14 5 Okay, you know, it's a piece of metal, but it's --
10:38:19 6 when we call it a tap segment, you know, that bears
10:38:22 7 some meaning. You know, it's a -- it's a tap, a
10:38:27 8 center tap in this case.

10:38:29 9 Q What about the extension-conductor segments
10:38:36 10 133 and 135 here, are those wires?

10:38:41 11 A I'd give the same kind of answer. I could
10:38:45 12 understand how you could say, well, it's a piece of
10:38:47 13 metal, it's a wire, but it does have a special -- a
10:38:51 14 special name, extension-conductor segments.

10:38:56 15 Q I understand that they're not -- they're not
10:39:14 16 -- like they all have their special names because,
10:39:17 17 you know, to describe the figure you need to give
10:39:19 18 names to different parts, right. But so the parts
10:39:26 19 that we talked about, 157, 158, via 191,
10:39:34 20 extension-conductor segment, those are all metal
10:39:36 21 wires, right?

10:39:38 22 MR. HALVERSON: Objection, form.

10:39:39 23 THE WITNESS: If you could repeat it again.
10:39:43 24 I'm looking at Figure 9 and you mentioned the
10:39:46 25 numbers. If you don't mind asking again.

10:39:49 1 BY MR. LIU:

10:39:49 2 Q So we discussed 157, 158, 191, 133, 135.

10:39:59 3 Those are all metal wires, right?

10:40:03 4 MR. HALVERSON: Same objection.

10:40:04 5 THE WITNESS: Well, I think the important
10:40:06 6 thing to realize is a person of ordinary skill
10:40:08 7 understands that these electrode segments, the 157
10:40:11 8 and 158, are part of a capacitor component. They're
10:40:16 9 where the action happens as far as generating
10:40:20 10 capacitive reactance. So this is a place where
10:40:23 11 there's a dead end and this is a place where the
10:40:26 12 flow variable has to precede the voltage. So in
10:40:31 13 other words, you have to get flow into it, excess
10:40:35 14 charge, that will then result in the voltage and the
10:40:39 15 energy being stored in an electric field.

10:40:41 16 And that phase relationship, that's what's
10:40:44 17 key for this being a capacitor and that's what's key
10:40:47 18 for that capacitance to resonate with the
10:40:51 19 inductance. So without that -- you know, so I don't
10:40:56 20 know that I agree with your -- the way you're
10:41:01 21 characterizing this.

10:41:02 22 BY MR. LIU:

10:41:07 23 Q Okay. Again, you're saying that the
10:41:12 24 electrode segments 157, 158 have to be part of a --
10:41:17 25 sorry, strike that. Let me just read what you said.

10:41:31 1 So the electrode segment 157 and 158, they
10:41:34 2 have to function as part of a designed capacitor?

10:41:38 3 MR. HALVERSON: Objection, form.

10:41:40 4 THE WITNESS: A way of thinking about this
10:41:43 5 is that they're a dead end. So the charge that goes
10:41:47 6 in there, the charge has to precede the voltage. So
10:41:53 7 a capacitor, you have to provide -- 90 degrees
10:41:58 8 before the voltage rises, you have to provide the
10:42:01 9 current. The current has to precede the voltage.

10:42:04 10 In an inductor, it's the other way around.
10:42:07 11 And that's because these are like electrode
10:42:11 12 segments, they're sort of a dead end for the charge.
10:42:14 13 The charge, as it goes in, will now develop an
10:42:18 14 electric field so that the voltage on the capacitor
10:42:22 15 will rise. It's like -- it's like a -- it's like a
10:42:32 16 bucket of charge or there's something called a
10:42:34 17 hydraulic accumulator. Like if you put flow into
10:42:38 18 something that has a back pressure, it will generate
10:42:40 19 pressure in response to your adding more charge or
10:42:43 20 current into it. It's like if you put a hydraulic
10:42:47 21 fluid in an accumulator, its pressure will rise
10:42:51 22 because you put more fluid into it.

10:42:56 23 BY MR. LIU:

10:43:07 24 Q Okay, let's move. I want to show you some
10:43:10 25 descriptions about the Figure 9. Could you go to

10:43:14 1 the specification in column 8, line 50?

10:43:21 2 A Okay, I'm there.

10:43:23 3 Q It says here, In some embodiments the first
10:43:29 4 region 120 may be limited between the two
10:43:31 5 extension-conductor segments 133 and 135, and the
10:43:35 6 coil-conductor segment 131 as shown in Figure 9. Do
10:43:40 7 you see those texts?

10:43:46 8 MR. HALVERSON: Sorry, Charles. I
10:43:48 9 apologize. Which lines?

10:43:51 10 MR. LIU: Line 50 through line 53.

10:43:59 11 MR. HALVERSON: Thank you.

10:44:01 12 THE WITNESS: Yeah, I see that.

10:44:02 13 BY MR. LIU:

10:44:10 14 Q So according to this description in
10:44:13 15 Figure 9, the first region is between the two
10:44:16 16 extension-conductor segments 133 and 135 and the
10:44:20 17 coil-conductor segment 131, right?

10:44:24 18 A Yes, that's what it says.

10:44:26 19 Q And that's three things that define the
10:44:31 20 first region, fair, 133, 135 and 131?

10:44:41 21 A Yeah, it seems like that's what it's saying,
10:44:43 22 yeah.

10:44:43 23 Q Now, the sentence before that in the same
10:44:50 24 paragraph it says, In some embodiments, the first
10:44:56 25 region 120 may be limited between the two

10:44:59 1 extension-conductor segments 133 and 135 as shown in
10:45:06 2 Figure 6. Do you see those?

10:45:11 3 A Yes.

10:45:15 4 Q So according to this sentence, in Figure 6,
10:45:20 5 the first region is between the two
10:45:22 6 extension-conductor segments 133 and 135, right?

10:45:30 7 A Yeah, that's what it says there just above
10:45:34 8 that line 50 in column 8.

10:45:36 9 Q And that's two things that define the first
10:45:44 10 region, right, 133 and 135?

10:45:50 11 A Yeah, that makes sense. It provides two
10:45:54 12 things and it says the first region is limited
10:45:57 13 between those two things.

10:45:59 14 Q Okay. Let me upload an exhibit real quick.
10:45:59 15 (Document marked previously as
10:46:33 16 Exhibit 1005 was presented.)

10:46:33 17 BY MR. LIU:

10:46:33 18 Q I'm uploading Exhibit 1005, the Gonzalez
10:46:38 19 reference.

10:46:38 20 (Discussion off the record.)

10:47:05 21 MR. LIU: Mr. Halverson, I recall this is
10:47:08 22 how you did it in Dr. Prucnal's deposition if I
10:47:11 23 recall. I think it just makes it easier
10:47:13 24 logistically.

10:47:14 25 MR. HALVERSON: I think that's right.

10:47:17 1 THE WITNESS: Okay, I have that open.

10:47:18 2 BY MR. LIU:

10:47:21 3 Q Fair to say you are very familiar with this
10:47:23 4 reference at this point?

10:47:24 5 A Yes.

10:47:25 6 Q I think the Gonzalez reference talks about
10:47:38 7 MOS varactors. Do you recall that?

10:47:42 8 A Yes.

10:47:44 9 Q So is a MOS varactor a capacitor?

10:47:49 10 A Like a type of variable capacitor.

10:47:58 11 Q Is it also a transistor?

10:48:07 12 A It's not a transistor. It's a -- it does
10:48:12 13 have -- that MOS part, it does have an MOS
10:48:20 14 capacitance in it. And the ones in Gonzalez have
10:48:24 15 two of those in series. So it's -- it's sometimes
10:48:31 16 thought of as varactor diodes that are opposing one
10:48:37 17 another and each of those varactor diodes has a
10:48:40 18 capacitance across the gate oxide.

10:48:46 19 Q It uses a transistor structure though,
10:48:51 20 right?

10:48:51 21 A That's -- yeah. It's close. When you learn
10:48:56 22 about transistors, the first thing you learn about
10:48:59 23 is an MOS capacitor because you're learning about
10:49:03 24 what inversion is. It creates a channel for charge
10:49:09 25 in a transistor. But a transistor also has a drain

10:49:13 1 and a source. And you're trying to modulate current
10:49:21 2 between the drain and the source. But that's not
10:49:24 3 what's happening in a varactor. It's really taking
10:49:27 4 part of the structure that's in a transistor and
10:49:31 5 doing some capacitance tricks with it.

10:49:35 6 Q Are you saying that a MOS varactor would not
10:49:38 7 have sources and drains and gate?

10:49:42 8 A Yeah, not really. I mean, you know, a
10:49:46 9 transistor, the whole point is you've got the gate
10:49:48 10 and you're using that to modulate effectively like
10:49:52 11 the transconductance in a drain-to-source circuit.
10:49:56 12 You're using it like a valve. And that's a
10:49:59 13 three-terminal device. When you're thinking about
10:50:04 14 varactors, you're thinking about them as
10:50:06 15 two-terminal devices where you're really focusing on
10:50:09 16 the variable capacitance between the gate and the --
10:50:14 17 a region below that.

10:50:18 18 Q Okay. So would a MOS -- sorry.

10:50:25 19 Would a MOS capacitor include electrode
10:50:29 20 segments?

10:50:32 21 A You can think of there being electrodes.
10:50:55 22 For instance, the gate electrode would be -- is a
10:51:01 23 way people talk when they would talk about -- in a
10:51:11 24 varactor. But with the segments part, I think
10:51:15 25 that's where -- I don't think it really has that

10:51:21 1 per se. There's not electrode segments there or
10:51:26 2 Dr. Prucnal hasn't identified any that I agree with.

10:51:32 3 Q Let me make sure I understand. So you're
10:51:34 4 saying a MOS capacitor has electrodes when the gate
10:51:42 5 -- sorry. Strike that.

10:51:43 6 So you're saying that a MOS capacitor has a
10:51:46 7 gate electrode, but it wouldn't have electrode
10:51:50 8 segments?

10:51:53 9 A Yeah, that's more or less right. You know,
10:51:55 10 I can -- I can understand us talking about
10:51:58 11 electrodes in the context of a varactor. But, you
10:52:04 12 know, I understand there's different positions about
10:52:06 13 what are -- constitute electrode segments in
10:52:10 14 Gonzalez that are -- that I don't agree with. I
10:52:16 15 don't agree with those identifications.

10:52:17 16 Q So would a gate electrode be an electrode
10:52:22 17 segment?

10:52:24 18 A Well, that's what I'm saying. It's like
10:52:27 19 that's the -- I'm saying no. I'm saying that I can
10:52:33 20 understand it being an electrode, but any of these
10:52:35 21 theories about why this would be somehow an
10:52:39 22 electrode segment because of other things it's
10:52:41 23 connected to and how those are laid out, I disagree
10:52:45 24 with all those positions. I just -- I don't -- I
10:52:49 25 don't buy it.

10:52:50 1 Q So we're not talking about its connections
10:52:52 2 to others. I'm just asking you is the gate
10:52:55 3 electrode in a MOS capacitor, is that by itself an
10:52:59 4 electrode segment?

10:53:01 5 MR. HALVERSON: Objection, form.

10:53:02 6 THE WITNESS: Yeah, so I'm trying to -- the
10:53:04 7 short answer is no. That's what I'm trying to tell
10:53:08 8 you in these answers.

10:53:09 9 BY MR. LIU:

10:53:16 10 Q So we went through what's your understanding
10:53:17 11 of electrode segments, right. So you said it
10:53:22 12 carries electric charges in the oscillatory fashion,
10:53:28 13 right?

10:53:30 14 MR. HALVERSON: Objection, form;
10:53:31 15 mischaracterizes the witness' testimony.

10:53:34 16 MR. LIU: Counsel, no speaking objections,
10:53:35 17 please. That's prohibited in this proceeding.

10:53:43 18 THE WITNESS: The real distinguishing part
10:53:51 19 of why this is an electrode segment is that it is --
10:53:55 20 as I was talking about with that dead end idea, the
10:53:58 21 idea that the charge that goes in is now
10:54:03 22 establishing an electric field, which in response to
10:54:07 23 the charge, is now creating a voltage. So the
10:54:12 24 voltage lags the charge. We also say the current
10:54:18 25 leads the voltage. And that's why this is a

10:54:21 1 capacitor. So that's really the important thing I
10:54:26 2 see in an electrode segment.

10:54:29 3 BY MR. LIU:

10:54:30 4 Q So are you saying the MOS capacitor does not
10:54:32 5 have this part?

10:54:35 6 A Yeah, it doesn't do that at all.

10:54:37 7 Q Are you saying in the MOS capacitor, the
10:54:47 8 charge does not establish an electric field in
10:54:51 9 response to I guess creating a voltage?

10:54:58 10 A There's not -- there's not two electrode
10:55:02 11 segments between which that happens. So the way --
10:55:07 12 in the MOS capacitor, there's going to be an
10:55:09 13 inversion layer of charge down in that Nwell. And
10:55:16 14 that's -- so the electric field is across the gate
10:55:20 15 oxide. So there's not that interelectrode
10:55:26 16 capacitance. That's just that's not how it works.
10:55:29 17 It's going to work into the bulk of the silicon.

10:55:38 18 Q Could you go to Figure 8 in the Gonzalez
10:55:54 19 reference?

10:55:55 20 A Okay, I'm there.

10:55:57 21 Q Do you see those yellow fingers in the
10:56:02 22 bottom of Figure 8?

10:56:05 23 A I maybe know what you mean. I think I
10:56:13 24 probably know what you mean. There's a lot of
10:56:15 25 fingers though or things that have potentially been

10:56:22 1 identified like that. So...

10:56:23 2 Q I mean the fingers that Dr. Prucnal has
10:56:26 3 characterized as electrode segments. And I
10:56:29 4 understand you disagree with that, but you know the
10:56:31 5 yellow finger structures that I'm talking about,
10:56:34 6 right?

10:56:34 7 A I think so. And maybe if we could just
10:56:37 8 spend just a tiny amount of time just to make sure
10:56:39 9 we're completely on the same page with this. Like
10:56:47 10 where, for instance, it says the fine-tuning
10:56:50 11 varactor, and I'm not -- I'm not -- where that
10:56:56 12 arrowhead is is roughly right on top. I'm not
10:57:02 13 saying it's pointing -- I'm not saying that's a
10:57:04 14 label of it, but what I'm just saying where the
10:57:06 15 arrowhead is on. So it's the longer ones that are
10:57:11 16 -- that's the ones I'm thinking of when you say the
10:57:14 17 yellow fingers.

10:57:15 18 Q That's right. I think there are roughly ten
10:57:19 19 of them, but let me count.

10:57:24 20 A Yeah, I count ten.

10:57:26 21 Q Yeah. Fair to say those ten fingers are at
10:57:34 22 the center of the dispute about Gonzalez in some
10:57:37 23 way?

10:57:40 24 A That's -- they're certainly an important
10:57:44 25 part of the disagreement, yes.

10:57:46 1 Q So are those yellow fingers metal wires?

10:58:04 2 A Yeah, they're -- you know, they're pieces of
10:58:11 3 metal that are laid out. They're connecting things
10:58:13 4 on either side of them so they're not a dead end.
10:58:18 5 And I don't believe they're given special names. So
10:58:26 6 they're -- I think it's fair to say, yeah, they're
10:58:30 7 wires.

10:58:31 8 Q Are they part of any transistors that you
10:58:47 9 know of, for example, MN1 and MN2?

10:58:54 10 MR. HALVERSON: Objection, form.

10:58:55 11 THE WITNESS: So a person of ordinary skill
10:59:00 12 doesn't think of wires that are sort of getting
10:59:05 13 there, you know, going to the thing, doesn't think
10:59:11 14 of that as part of -- part of the -- doesn't think
10:59:15 15 of the wires as part of that device. So even if
10:59:18 16 those connect through some of that orange stuff,
10:59:22 17 that metal and then maybe go down and connect to MN1
10:59:26 18 and MN2, you don't think of the yellow fingers as
10:59:31 19 being part of the transistors.

10:59:41 20 BY MR. LIU:

11:00:07 21 Q Are those yellow fingers in a comb-like
11:00:13 22 structure?

11:00:17 23 A I'm going to say no. And the reason is
11:00:23 24 because they connect through to things. So when we
11:00:27 25 think of a comb, that's like dead ends where the

11:00:31 1 teeth are each sort of like you walk the plank and
11:00:36 2 there's nothing there. The teeth sort of end. And
11:00:40 3 so the difference here is that the ends of those
11:00:47 4 what might otherwise be teeth kind of keep on going
11:00:52 5 and are connecting to other things. And that's the
11:00:57 6 way it's different from a comb.

11:01:00 7 Q Would there capacitance between these yellow
11:01:05 8 fingers?

11:01:07 9 A Well, I'd say two things about that. One is
11:01:11 10 there's -- you know, just when there's metal
11:01:16 11 generally, or anything actually, things that are
11:01:22 12 conductive, there's capacitance and stray
11:01:24 13 capacitance between things. So you know, the
11:01:26 14 example I gave is like even between my fingers, my
11:01:30 15 fingers, there's capacitance.

11:01:32 16 But these are wires and they don't have that
11:01:38 17 property of like being like dead ends where they're
11:01:42 18 accumulating charge and inducing charge as part of a
11:01:45 19 designed capacitance. So that way, there's just --
11:01:55 20 there's not a designed capacitance there and in
11:01:57 21 fact, they're designed to be not that. They're
11:02:00 22 designed to not be -- to have high stray capacitance
11:02:06 23 even.

11:02:08 24 Q But there still would be capacitance between
11:02:11 25 these fingers, right?

11:02:13 1 A In that -- in that sense of like, yes,
11:02:15 2 there's capacitance between everything. In that
11:02:20 3 way, there is stray capacitance. But even the stray
11:02:23 4 capacitance is designed to be -- you know, you want
11:02:30 5 it to be as low as possible. You lay this out to be
11:02:34 6 as sparse as possible because you do have to cross.
11:02:38 7 It's unavoidable in a cross-coupled pair in a VCO,
11:02:42 8 you have to cross wires, but when you do that, you
11:02:45 9 want to do so minimizing stray capacitance.

11:02:49 10 Q Can capacitance be avoided between the
11:02:56 11 fingers?

11:02:57 12 A In a chip, practically speaking, it can't be
11:03:04 13 avoided or reduced to zero. Even like our body to
11:03:08 14 the room around us, we have, you know, a picofarad
11:03:11 15 of capacitance to the structures surrounding us.
11:03:14 16 You know, you can't -- you're never getting rid of
11:03:19 17 this because the electric fields do exist between
11:03:22 18 different components that are at different
11:03:25 19 potentials.

11:03:26 20 Q So when you're designing a circuit like, you
11:03:33 21 know, the VCO circuit in Gonzalez, that capacitance
11:03:36 22 has to be part of the design considerations, fair?

11:03:44 23 A As a parasitic or as a stray, you may
11:03:51 24 account for it. And there's a typical design cycle
11:03:57 25 that happens where you lay something out and then

11:04:00 1 you extract -- it's called extracting the parasitics
11:04:05 2 from your layout. And you can include that back in
11:04:09 3 the design just to see if one of those parasitics is
11:04:12 4 really harming performance and if you need to maybe
11:04:16 5 tweak layout to avoid parasitics. So there tends to
11:04:22 6 be a cycle of layout parasitic extraction, but you
11:04:29 7 can account -- you can account for strays and
11:04:33 8 parasitics in that way.

11:04:34 9 Q So in designing the LC circuit, you would
11:04:52 10 account for the stray capacitance generated by these
11:04:56 11 fingers?

11:05:01 12 MR. HALVERSON: Objection, form.

11:05:02 13 THE WITNESS: I would say that generally a
11:05:06 14 process of integrated circuit layout, you often
11:05:11 15 don't just like lay it out once and then go right to
11:05:17 16 the fab. That would be imprudent. So usually you
11:05:24 17 create a design and you've laid it out and then you
11:05:30 18 do this parasitic extraction. And so it's a normal
11:05:34 19 thing to then look at, well, what are the
11:05:37 20 parasitics? How bad are they? Does this whole
11:05:41 21 thing not work the way I've laid it out? And you
11:05:45 22 can adjust.

11:05:47 23 You know, in a way you're kind of -- you're
11:05:49 24 thinking about all the problems that can arise
11:05:51 25 because it's so expensive to fabricate, you kind of

11:05:54 1 want to spend some time iterating a design to
11:05:57 2 account for parasitics.

11:06:06 3 BY MR. LIU:

11:06:07 4 Q So by parasitics, do you mean the parasitic
11:06:10 5 capacitance generated by these fingers or do you
11:06:14 6 mean some other parasitics?

11:06:15 7 A It would be all of them and it could include
11:06:18 8 parasitic capacitance generated by these fingers,
11:06:21 9 which is already then made to be, you know,
11:06:26 10 minimized. You can tell by how the structure is
11:06:29 11 built. You know, it's designed to -- you know,
11:06:32 12 these aren't close, you might say. They've been
11:06:35 13 pushed far apart, yet you know, as a necessary evil,
11:06:39 14 because they do have to cross. You have to make
11:06:42 15 wires across. If you just made them cross one on
11:06:48 16 top of another, gosh, maybe you'd have more
11:06:51 17 capacitance and you could do better. You could have
11:06:54 18 more stray capacitance in that case. So this is a
11:06:57 19 structure that I think was made to minimize stray
11:06:59 20 capacitance.

11:07:02 21 Q By minimizing, I mean, do you know typical
11:07:11 22 values for these stray capacitances?

11:07:16 23 MR. HALVERSON: Objection, form.

11:07:20 24 THE WITNESS: I could look to see if there's
11:07:25 25 some range, but I mean, capacitance tends to be

11:07:34 1 higher than you might think in a chip because things
11:07:37 2 are close to one another. And that actually -- when
11:07:41 3 you make things smaller, the capacitance actually
11:07:43 4 goes up, like if things get closer. So you know,
11:07:49 5 the kinds of numbers you hear about are -- they're
11:07:52 6 measured often picofarads. They could be measured
11:07:58 7 potentially in a smaller unit.

11:08:03 8 BY MR. LIU:

11:08:07 9 Q Do you think certain minimal capacitance
11:08:11 10 values are needed to satisfy the claims here?

11:08:19 11 A I don't -- I don't see it that way. I don't
11:08:23 12 think it's -- there's not a limitation about the
11:08:29 13 magnitude of the capacitance. But so no.

11:08:34 14 Q And when the fingers generate these stray
11:08:43 15 capacitance, they generate it in the same way a
11:08:50 16 finger capacitor generates capacitance, right?

11:08:57 17 A I wouldn't necessarily agree with that
11:09:00 18 because these are wires. You remember how I was
11:09:04 19 talking about like the dead end concept of like --
11:09:08 20 this isn't -- this isn't a place for charge to go
11:09:14 21 and accumulate as a surface charge to then induce a
11:09:19 22 surface charge in something else that was brought
11:09:21 23 right to it to make what persons of ordinary skill
11:09:24 24 understand to be a capacitor and a capacitor
11:09:27 25 component. You know, this is rather like a wire

11:09:30 1 and -- because there's an outlet on the other side.

11:09:35 2 It's like it's a -- it's not a dead end.

11:09:38 3 Q I understand that. I understand that it's

11:09:40 4 not a dead end. And your point is it generates a

11:09:44 5 straight capacitance, right, not a design

11:09:46 6 capacitance. But what I'm asking you is when it is

11:09:49 7 generating that stray capacitance, it still has

11:09:52 8 surface charges that -- between these two fingers to

11:09:56 9 generate that stray capacitance in the same way that

11:09:59 10 a finger capacitor would generate designed

11:10:03 11 capacitance, right?

11:10:04 12 MR. HALVERSON: Counsel, I'd ask you to let

11:10:07 13 Dr. Phinney finish his answer before you jump in

11:10:10 14 with a question. Dr. Phinney, go ahead.

11:10:11 15 THE WITNESS: I would say that that

11:10:13 16 capacitance that we're talking about between two

11:10:16 17 pieces of metal that I've called like a stray

11:10:20 18 capacitance, that that is -- would generally be an

11:10:24 19 electrostatic capacitance. And so I think I would

11:10:28 20 agree with you that it's an electrostatic

11:10:31 21 phenomenon, like the energy stored is between

11:10:35 22 charges in metal and there's an electric field

11:10:40 23 between them. So that's the kind of principle. We

11:10:45 24 would call it an electrostatic capacitance.

11:10:48 25 ///

11:10:48 1 BY MR. LIU:

11:10:51 2 Q So you're saying that the fingers generate a
11:10:53 3 static capacitance?

11:10:58 4 A No, no, no. I said electrostatic. That's
11:11:01 5 one word. I'm sorry if that -- when I said electro
11:11:07 6 -- an electrostatic capacitance, I mean that there's
11:11:10 7 an electric field -- the stray capacitance
11:11:13 8 phenomenon is through -- there's still charges that
11:11:21 9 are creating -- that are terminating an electric
11:11:24 10 field between two pieces of metal. And I called
11:11:30 11 that an electrostatic capacitance.

11:11:34 12 Q I don't think you answered my question. I
11:11:38 13 think are you saying these fingers generate a static
11:11:42 14 capacitance, yes or no?

11:11:44 15 A Oh, okay. I thought you were -- I thought
11:11:47 16 we weren't communicating about the word
11:11:49 17 electrostatic and static. So your question still is
11:11:52 18 about static?

11:11:53 19 Q Yes.

11:11:54 20 A Okay.

11:11:55 21 Q Do the fingers -- sorry. Go ahead. Sorry.
11:12:02 22 Let me reask my question. I think it's getting
11:12:05 23 muddled up.

11:12:05 24 So my question is simply do these fingers
11:12:09 25 generate a static capacitance or not?

11:12:17 1 A I would say they do generate a stray
11:12:26 2 capacitance that is static in the sense that it is a
11:12:32 3 function of the shape and position of the metal
11:12:44 4 which isn't -- those are parameters that don't
11:12:48 5 change. So I'm answering -- do you see what I'm
11:12:53 6 saying? I'm answering static in that way. It's
11:12:55 7 like it would be sort of fixed by shape and
11:12:59 8 position.

11:13:00 9 Q Because the capacitance value generated by
11:13:04 10 these fingers do not -- does not change?

11:13:11 11 A To a very good approximation, that's -- the
11:13:17 12 real things that create this stray capacitance are
11:13:20 13 the shape and location of the metal, like how thick
11:13:24 14 it is. And so, you know, when that -- when all
11:13:28 15 those parameters aren't changing, the capacitance
11:13:31 16 would be -- the stray capacitance would be a
11:13:34 17 function of those unchanging or not very much
11:13:39 18 changing parameters.

11:13:39 19 Q So the stray capacitance value would not
11:13:46 20 change, right? Fair?

11:13:49 21 MR. HALVERSON: Objection, form.

11:13:50 22 THE WITNESS: Pretty much; to a very good
11:13:52 23 approximation.

11:14:04 24 MR. HALVERSON: Counsel, we're a little over
11:14:06 25 an hour. Good time for a quick break?

11:14:08 1 MR. LIU: Yeah, sounds good.

11:14:13 2 VIDEOGRAPHER: Going off the record. The

11:14:14 3 time is 11:14 a.m.

11:14:17 4 (Short recess.)

11:24:59 5 VIDEOGRAPHER: Going back on the record.

11:26:03 6 The time is 11:26 a.m. This marks the beginning of

11:26:06 7 media Number 2. Please continue.

11:26:08 8 BY MR. LIU:

11:26:10 9 Q Dr. Phinney, welcome back. So --

11:26:13 10 A Thank you.

11:26:13 11 Q We were talking about the yellow fingers in

11:26:18 12 Figure 8 before the break. Recall that?

11:26:23 13 A Oh, yes. Sorry.

11:26:29 14 Q Once the dimensions of the fingers are

11:26:37 15 fixed, the stray capacitance that it generates

11:26:42 16 remains the same, right?

11:26:46 17 A To a very good approximation and that's what

11:26:49 18 I was answering with the static question.

11:26:51 19 Q So during the design of the LC circuit, you

11:27:06 20 pretty much know how much stray capacitance you will

11:27:09 21 get from this part once the dimensions are fixed,

11:27:14 22 right?

11:27:17 23 A I would agree with that. There's -- that's

11:27:22 24 part of parasitic extraction.

11:27:32 25 Q Does Gonzalez teach minimizing that

11:27:43 1 capacitance?

11:27:48 2 MR. HALVERSON: Objection, form.

11:27:49 3 THE WITNESS: I'd say so because of how
11:27:59 4 sparse it is.

11:28:07 5 BY MR. LIU:

11:28:20 6 Q Based on the dimensions shown in Figure 8?

11:28:29 7 MR. HALVERSON: Objection, form.

11:28:32 8 THE WITNESS: So that's about right. The
11:28:37 9 how sparse the structure is and then just when you
11:28:43 10 understand that the differential capacitance is the
11:28:48 11 thing that needs to be tuned, you know, that's --
11:28:58 12 any static differential capacitance is -- doesn't
11:29:06 13 promote either frequency tuning range or maximum
11:29:12 14 frequency. It tends to counteract those figures of
11:29:16 15 merit or the VCO.

11:29:20 16 BY MR. LIU:

11:29:48 17 Q So could you go to page 4 of Gonzalez? I
11:29:54 18 believe somewhere it's -- let me check real quick.
11:30:11 19 So below Figure 1, about seven or eight lines down
11:30:23 20 it says, "The best comprise for FTR, PN, and power
11:30:30 21 consumption can be obtained using LC-tank VCOs by
11:30:35 22 optimally sizing the VCO transistors in order to
11:30:39 23 minimize the parasitic capacitances and by
11:30:43 24 maximizing the varactor capacitance range."

11:30:47 25 Do you see that?

11:30:49 1 A Yes.

11:30:57 2 Q Would you say this description teaches
11:31:02 3 minimizing the capacitance between those fingers we
11:31:06 4 were talking about?

11:31:13 5 A I think it's generally saying minimize
11:31:18 6 parasitic capacitance that can include the static
11:31:23 7 differential capacitance between the fingers which
11:31:40 8 is a parasitic.

11:31:42 9 Q Right. But here it is saying minimizing the
11:31:48 10 parasitic capacitances by optimally sizing the VCO
11:31:52 11 transistors. Do you see that?

11:31:57 12 A Yes, I see that. The first part of that
11:32:14 13 sentence is by optimally sizing the VCO transistors
11:32:18 14 in order to minimize the parasitic capacitances.

11:32:21 15 Q And the fingers are not part of any VCO
11:32:28 16 transistors, right?

11:32:30 17 A Yeah, that's right. I understood I answered
11:32:34 18 that question before when you were asking — I think
11:32:37 19 you asked that before.

11:32:39 20 Q Right. So here what do you think is meant
11:32:43 21 by optimally sizing the VCO transistors to minimize
11:32:48 22 the parasitic capacitances?

11:32:52 23 A Well, there's many knobs that you have in
11:32:56 24 laying out a transistor. You can choose like how
11:32:59 25 large the source and drain diffusions are and how

11:33:03 1 large the gate is. And so you need to -- yeah, you
11:33:08 2 have many parameters to play with and there's going
11:33:10 3 to be parasitics associated with the layout of that
11:33:13 4 transistor, so that includes parasitic capacitances
11:33:17 5 that you want to minimize.

11:33:21 6 Q But that parasitic capacitance would relate
11:33:23 7 to the transistors and not those fingers we're
11:33:28 8 talking about, right?

11:33:28 9 A Yeah, in that sentence that's what it's
11:33:31 10 talking about. It's like you're tuning those knobs
11:33:35 11 related to the layout of the transistor in order to
11:33:37 12 minimize parasitic capacitances is what that
11:33:40 13 sentence is saying.

11:33:42 14 Q Yeah. My point is the parasitic capacitance
11:33:51 15 mentioned here is not the parasitic capacitance
11:33:55 16 between those fingers, right, because here we're
11:33:58 17 talking about the VCO transistors?

11:34:01 18 MR. HALVERSON: Objection, form. That's not
11:34:03 19 a question.

11:34:10 20 THE WITNESS: Could you just maybe just ask
11:34:13 21 that again? I'm sorry.

11:34:14 22 BY MR. LIU:

11:34:15 23 Q So do you still believe the parasitic
11:34:18 24 capacitance here refers to the parasitic capacitance
11:34:21 25 between those fingers we discussed?

11:34:25 1 A In this sentence, it's talking about the
11:34:31 2 minimize the parasitic capacitances -- you know,
11:34:34 3 optimize the transistor in order to change its
11:34:36 4 parasitic capacitances. So that's not -- that's not
11:34:39 5 the -- that relates to parasitic capacitances at the
11:34:47 6 transistor, not between the fingers.

11:34:51 7 Q I believe you talked something before, but I
11:35:23 8 want to make sure that, you know, I understand what
11:35:26 9 you were saying.

11:35:26 10 So let me ask, do you know why those yellow
11:35:29 11 fingers are designed as interdigitated finger
11:35:35 12 structures?

11:35:38 13 A I see it as a layout choice to minimize
11:35:47 14 parasitic differential capacitance.

11:35:59 15 Q I don't understand because if they are
11:36:07 16 designed to be interdigitated fingers, wouldn't that
11:36:12 17 increase the capacitance between them?

11:36:14 18 A Not at all. Imagine you made them just one
11:36:21 19 -- one wire.

11:36:25 20 Q Right.

11:36:26 21 A Now, there let's say you say, well, I'm
11:36:29 22 going to make them far apart to minimize their
11:36:32 23 capacitance. I'm going to separate those two wires.
11:36:34 24 You actually haven't avoided the necessary evil of
11:36:39 25 crossing because even if you separate them at one

11:36:42 1 point, they have to cross at some point because it's
11:36:47 2 a cross-coupled pair. And so you're faced with
11:36:50 3 having to pass these things past one another, yet
11:36:55 4 make their parasitic static differential capacitance
11:37:03 5 as low as you can. And so that's why I say the
11:37:07 6 sparse structure is something that's accomplishing
11:37:15 7 that. It's crossing yet with just about the lowest
11:37:19 8 capacitance you can -- you can muster.

11:37:24 9 Q For example, why wouldn't the designer put
11:37:29 10 them into different layers? Why do we have these
11:37:35 11 fingers on the same layers at all? Do they have to
11:37:39 12 be on the same layer?

11:37:40 13 MR. HALVERSON: Objection, form.

11:37:40 14 THE WITNESS: I don't think they would
11:37:48 15 necessarily have to be on the same layer, but any --
11:37:54 16 there's many concerns that a designer will likely
11:37:59 17 have. And they're going to be worried about things
11:38:01 18 like matching and balancing two sides of a
11:38:06 19 cross-coupled differential pair.

11:38:09 20 I think there's going to be a lot of
11:38:11 21 scrutiny given to, you know, a lot of these
11:38:15 22 different layout considerations. So I think there
11:38:20 23 will be a tendency to want to make a symmetric
11:38:22 24 structure. You know, you don't want to like offset
11:38:28 25 the crossing or do something like that, but you also

11:38:31 1 want the crossing to not have a static differential
11:38:35 2 stray capacitance.

11:38:40 3 BY MR. LIU:

11:38:48 4 Q So you're saying generally it is desirable
11:38:52 5 to make the structure symmetrical in terms of how
11:38:59 6 they match to the, for example, extension-conductor
11:39:03 7 segments of the inductor?

11:39:08 8 MR. HALVERSON: Objection, form.

11:39:12 9 THE WITNESS: That could be. When you look
11:39:27 10 at the Figure 8, for instance, you notice it's not
11:39:39 11 perfect, but close bilateral symmetry.

11:39:55 12 BY MR. LIU:

11:40:06 13 Q So is it fair to say that although these
11:40:09 14 fingers generate a small stray capacitance, they're
11:40:15 15 designed this way because their benefits outweigh
11:40:19 16 the potential downside of that stray capacitance?

11:40:23 17 A I really apologize. It was like the first
11:40:27 18 word in that I didn't quite hear it. I'm sorry. If
11:40:32 19 I could make sure I heard the question.

11:40:34 20 Q So the fingers are designed this way as
11:40:36 21 shown in Figure 8 because their benefits outweigh
11:40:40 22 the downside of the small stray capacitance, right?

11:40:46 23 MR. HALVERSON: Objection, form.

11:40:46 24 THE WITNESS: I don't know that I'd agree
11:40:49 25 with that that the — it's not just like benefits.

11:40:58 1 It's like a necessity.

11:41:00 2 What I'm talking about is if we look at
11:41:02 3 Figure 2, do you see there's a crossing? Like
11:41:12 4 there's a need to get a signal from one side of the
11:41:16 5 circuit to the other side. And so I don't know that
11:41:24 6 I'd call like that a benefit. That's why I call
11:41:29 7 that a necessary evil. In other words, you have to
11:41:33 8 have a crossing and so you want to do that in a way
11:41:37 9 that minimizes the stray differential static
11:41:45 10 capacitance.

11:41:51 11 BY MR. LIU:

11:42:12 12 Q So you mentioned Figure 2. Let's go to
11:42:14 13 Figure 2. Give me a second. I actually would like
11:42:26 14 to use an annotated version of Figure 2, if you
11:42:29 15 don't mind. So let me upload the next exhibit real
11:42:34 16 quick.

11:42:34 17 (Document marked previously as
11:42:41 18 Exhibit 1003 was presented.)

11:42:41 19 BY MR. LIU:

11:42:50 20 Q I just uploaded Exhibit 1003. That's
11:42:54 21 Dr. Prucnal's declaration in this IPR.

11:43:01 22 A It will be about 40 seconds. Okay, I have
11:43:51 23 it open.

11:43:52 24 Q Could you go to PDF page 93? At the end of
11:44:02 25 paragraph 150, there's an annotated version of

11:44:06 1 Figure 2 there.

11:44:08 2 A Okay, I'm there.

11:44:09 3 Q So in the middle there is a blue box. That
11:44:26 4 is the digital control varactor bank also called a
11:44:31 5 discrete tuning varactor bank, right?

11:44:40 6 A Yeah, that's the one in blue.

11:44:45 7 Q And that discrete tuning varactor bank is
11:44:51 8 connected to the inductor terminals Out+ and Out-
11:45:01 9 right?

11:45:02 10 A Yeah, that's -- that's right. It's
11:45:12 11 connected in a so-called differential position.

11:45:14 12 Q On top of the -- sorry, strike that.

11:45:26 13 So above the blue box is an orange-ish box
11:45:32 14 that's the continuous tuning varactor, right?

11:45:41 15 A Yes, that's the schematic depiction of it
11:45:45 16 where it has that continuous control voltage, the
11:45:49 17 Vc, as opposed to digital control voltages.

11:45:54 18 Q And that continuous tuning varactor is also
11:46:04 19 connected to the inductor terminals Out+ and Out-
11:46:10 20 right?

11:46:11 21 A Yeah, I'd agree with that. It's connected
11:46:15 22 again in that so-called differential position.

11:46:18 23 Q Actually, we can see here that like the same
11:46:25 24 wires are used to provide both connections to the
11:46:31 25 continuous tuning varactor and the discrete tuning

11:46:35 1 varactor bank, right?

11:46:39 2 A Here I'd say in this schematic, we see the
11:46:47 3 same connections to those same two signals, Out+ and
11:46:52 4 Out-.

11:46:53 5 Q And we looked at Figure 8 which shows the
11:47:18 6 physical layout of the schematic diagram, right?

11:47:28 7 A Parts of it.

11:47:30 8 Q Right. So do the yellow fingers in Figure 8
11:47:39 9 provide the connection from the inductor to the
11:47:43 10 continuous tuning varactor?

11:47:55 11 MR. HALVERSON: Objection, form.

11:47:56 12 THE WITNESS: That's not something that's
11:47:59 13 depicted in Figure 8.

11:48:06 14 BY MR. LIU:

11:48:08 15 Q Well, as an expert, would you be able to
11:48:11 16 tell that the yellow fingers provide the connection
11:48:15 17 from the inductor to the fine-tuning varactor?

11:48:23 18 MR. HALVERSON: Objection, form.

11:48:25 19 THE WITNESS: So that connection's not shown
11:48:30 20 and the connection -- you were asking about the
11:48:32 21 continuous varactors, I believe?

11:48:35 22 BY MR. LIU:

11:48:35 23 Q Yes.

11:48:37 24 A Those connections aren't shown in Figure 8.

11:48:46 25 Q Yeah, but you're an expert, right? So I'm

11:48:49 1 asking you, does it make sense that the yellow
11:48:53 2 fingers would provide that connection from the
11:48:56 3 inductor terminals to that varactor?

11:49:00 4 MR. HALVERSON: Objection, form; asked and
11:49:01 5 answered.

11:49:04 6 MR. LIU: Counsel, again I'm going to remind
11:49:09 7 you not to have speaking objections.

11:49:13 8 MR. HALVERSON: That's not a speaking
11:49:14 9 objection.

11:49:19 10 MR. LIU: If you keep doing this, then I'll
11:49:22 11 reserve rights to seek sanctions from the Board.

11:49:28 12 MR. HALVERSON: Want to ask your question
11:49:30 13 again?

11:49:37 14 BY MR. LIU:

11:49:38 15 Q Dr. Phinney, does it make sense to you as an
11:49:40 16 expert that the yellow fingers would provide the
11:49:43 17 connection from the inductor terminals to the
11:49:46 18 fine-tuning varactor?

11:49:48 19 MR. HALVERSON: Same objection.

11:49:49 20 THE WITNESS: It's not a connection that's
11:49:54 21 shown.

11:49:56 22 BY MR. LIU:

11:49:58 23 Q How about the discrete tuning varactor bank
11:50:02 24 shown in the blue box, does the yellow fingers
11:50:08 25 provide that connection from the inductor terminals

11:50:11 1 to the discrete tuning varactor bank?

11:50:32 2 A I'd say in part.

11:50:43 3 Q For example, the terminal Out+, it goes
11:50:53 4 through the yellow fingers to one side of the
11:51:01 5 discrete tuning varactor bank, right?

11:51:07 6 A I think I'd agree with that. You know, like
11:51:11 7 if we look at some of these yellow fingers, they go
11:51:17 8 across and then up to that more copper-colored or
11:51:20 9 orange-colored metal piece and then downward to make
11:51:30 10 some of the connections to the digitally controlled
11:51:34 11 differential varactors.

11:51:37 12 Q So if the yellow fingers deliver -- if the
11:51:53 13 -- sorry, strike that.

11:51:54 14 If the yellow fingers provide that
11:51:56 15 connection for the discrete tuning varactor, it
11:52:03 16 would make sense that they also provide the
11:52:06 17 connection for the fine-tuning varactor, right?

11:52:11 18 A Yeah, I disagree with this. And that's --
11:52:17 19 that connection that you're talking about to the
11:52:19 20 fine-tuning varactor is not shown. And I talk about
11:52:25 21 the reasons why I -- further reasons why I don't
11:52:31 22 think that connection makes sense in my declaration.

11:52:34 23 Q Then in your opinion, how is that -- how is
11:52:43 24 that -- I guess in your opinion, where is that
11:52:46 25 connection -- sorry. Strike that.

11:52:49 1 How is the fine-tuning varactor actually
11:52:53 2 connected to the inductor terminals?

11:52:56 3 A Through something that's not shown because
11:53:06 4 it's not shown; so some other wires or connections.

11:53:11 5 Q So you're saying Figure 8 does not provide
11:53:31 6 all the metal connections between the capacitor and
11:53:37 7 the inductor?

11:53:39 8 A Yeah, that's right. It's -- there's
11:53:49 9 connections where the layout is not shown.

11:53:52 10 Q But you're not saying that the fine-tuning
11:54:02 11 varactor would be like floating or isolated, right?

11:54:09 12 A Yeah, I don't think it would be. It's just
11:54:19 13 that the connection to it is not shown.

11:54:37 14 By the way, I just want to clarify, I
11:54:40 15 realized that I've given two answers where at the
11:54:43 16 very beginning, I say the word "yeah." And I'm not
11:54:48 17 -- that was just a way of speaking to like lead into
11:54:51 18 what my answer was. I'll not say that again, just
11:54:56 19 to make it clear.

11:54:57 20 Q Thank you. I get it.

11:54:59 21 A It was a social word.

11:55:10 22 Q Also in Figure 2, do you see the inductor
11:55:13 23 being drawn as a horseshoe-shaped finger?

11:55:20 24 A I see that.

11:55:23 25 Q Is that a typical inductor signal that you

11:55:29 1 would see in a circuit diagram?

11:55:32 2 A And you were talking about Figure 2, I

11:55:35 3 believe, in your question?

11:55:36 4 Q Yes, that's right.

11:55:38 5 A That appears to be quite a specific shape.

11:55:48 6 An inductor you often see represented we say

11:55:56 7 schematically, it can look like a coil. It can

11:56:01 8 almost look like a spring is usually how that's

11:56:03 9 drawn schematically.

11:56:08 10 Q I want to continue discussing Figure 8, but

11:56:36 11 I would like to discuss maybe some of your opinions

11:56:39 12 from your declaration about Figure 8. So I would

11:56:42 13 like to upload your declaration here.

11:56:42 14 (Document marked previously as

11:56:48 15 Exhibit 2003 was presented.)

11:56:48 16 BY MR. LIU:

11:57:02 17 Q Let me know when you have the declaration,

11:57:04 18 which is Exhibit 2003.

11:57:08 19 A Okay, I have it open.

11:57:22 20 Q Actually, could you go to page 77? I think

11:57:27 21 that's your CV at the end of your declaration.

11:57:33 22 A Okay, I'm there.

11:57:36 23 Q Do you recall providing a CV in the ITC

11:57:40 24 proceeding?

11:57:42 25 A Yes.

11:57:45 1 Q Any notable changes you note from that prior
11:57:50 2 CV?

11:57:53 3 A I suppose the testimony list would have
11:57:59 4 grown, testimony list.

11:58:01 5 Q But no other notable changes other than the
11:58:07 6 more cases you might have worked on, right?

11:58:15 7 A I maybe in the last year put some old LIGO
11:58:20 8 publications on -- in publications -- in the
11:58:24 9 publications section.

11:58:27 10 Q Could you go to paragraph 102?

11:59:00 11 A Okay, I'm there.

11:59:01 12 Q Here at the end of 102, you said, "These
11:59:19 13 yellow wires are not part of any varactor or
11:59:24 14 capacitor component. They simply carry charge from,
11:59:27 15 for example, the Out+ terminal to the digitally
11:59:30 16 controlled varactors. "

11:59:31 17 Do you see that?

11:59:32 18 A Yes.

11:59:32 19 Q And then you show an annotated diagram of
11:59:38 20 Figure 8. So here there are several arrows in red
11:59:48 21 that you added to Figure 8. The first arrow you
11:59:52 22 added starts in the yellow metal layer, right?

12:00:01 23 A Yes.

12:00:02 24 Q And that yellow metal is partly covered by
12:00:08 25 the brown metal on top of it, right?

12:00:14 1 A Maybe. The part we see is the part not
12:00:20 2 covered.
12:00:31 3 Q And here the yellow metal is connected to
12:00:51 4 the -- sorry.
12:00:52 5 The first the arrow you added, that part is
12:00:56 6 connected to the Out+ terminal from the inductor,
12:01:00 7 right?
12:01:05 8 A Yeah, I think so.
12:01:10 9 Q How do you know that part is connected to
12:01:20 10 the Out+ terminal?
12:01:26 11 A Because the Out+ connection needs to get to
12:01:33 12 the cross-coupled differential pair and to the
12:01:35 13 digitally controlled varactors connected in a
12:01:38 14 differential position.
12:01:41 15 Q So you assume that the connection from the
12:01:56 16 Out+ terminal in brown, it would actually extend
12:02:01 17 down to the yellow metal layer?
12:02:04 18 A That's what I concluded. There's some
12:02:14 19 ambiguity sometimes because yellow metal underneath
12:02:16 20 the brown in other places doesn't appear to make a
12:02:20 21 connection in this -- in this figure.
12:02:32 22 Q In this figure, I mean do you see points
12:03:01 23 that actually connect the yellow metal layer to the
12:03:07 24 brown metal layer on top?
12:03:09 25 A So one place that I think that occurs is you

12:03:21 1 see where it says MN1? And do you see how

12:03:25 2 there's --

12:03:26 3 Q Right.

12:03:26 4 A Yeah. If we're doing down further, so at

12:03:30 5 the very -- I'm going to call it the bottom of the

12:03:32 6 brown thing that's labeled Out+, that's a place

12:03:39 7 where I think there's connections shown from the

12:03:43 8 brown to the yellow. But it gets a little ambiguous

12:03:50 9 in this figure because if we see where it says Out-

12:03:55 10 in red, just to -- jumping over to the next brown

12:03:59 11 thing, there's yellow below that and I don't think

12:04:04 12 there's a connection there because that would just

12:04:06 13 be -- that would be a differential short. You know,

12:04:12 14 there's -- brown is shown on top of yellow, but I

12:04:17 15 think you have to -- you have to think about the

12:04:21 16 circuit to know whether or not there's a connection.

12:04:25 17 Q I think I understand what you're saying. So

12:04:34 18 you cannot determine the connections in this circuit

12:04:39 19 based on Figure 8 alone; you have to understand

12:04:42 20 these things in the context of the -- you know, the

12:04:44 21 LC circuit that Gonzalez is trying to build, right?

12:04:53 22 A I think that's fair to say because let's say

12:04:57 23 you made an assumption that yellow is -- when

12:04:59 24 there's brown above it, is always connected. You

12:05:03 25 know, I think you'd run into some wrong conclusions.

12:05:15 1 Q So for instance -- this figure is kind of
12:05:36 2 small, so I'm trying to make myself clear.

12:05:39 3 So if you look at the right side of this
12:05:43 4 figure, it says "to output buffer." Do you see
12:05:49 5 those texts?

12:05:49 6 A Yes.

12:05:50 7 Q So if we talk about this brown metal
12:05:55 8 structure that has yellow metal under it, and you
12:06:03 9 think there would be connections between the yellow
12:06:05 10 and the brown because both have to be connected to
12:06:08 11 the Out+ terminal, right?

12:06:12 12 A You had asked this about that longer arrow,
12:06:18 13 the red arrow, and I answered, yeah, I think that
12:06:22 14 yellow is connected to the brown. So I think -- I
12:06:28 15 think that's an instance where, yeah, I think that
12:06:31 16 would be connected to -- so that the Out+ signal
12:06:36 17 could be conveyed to the other side of the circuit.

12:06:48 18 Q Even though we can't really see the
12:06:52 19 connections between them from Figure 8, for
12:06:55 20 instance, we don't really see like vias connecting
12:06:58 21 these two layers, fair?

12:07:03 22 A I think that's fair. We don't see vias. I
12:07:10 23 think there would be a connection at that place that
12:07:13 24 I talked about with that longer red arrow because
12:07:16 25 that's -- that's how this makes sense, this

12:07:23 1 structure makes sense.

12:07:28 2 Q By the way, these metal layers would
12:07:31 3 generally be stacked on top of each other with vias
12:07:36 4 between them, right?

12:07:38 5 A Maybe. So for instance, there's two -- if
12:07:46 6 you look carefully at these brown ones, the brown
12:07:49 7 are actually a stack or a sandwich of like two. And
12:07:56 8 you know, that could mean different things. But
12:08:03 9 vias would be one way to connect metal layers, I'd
12:08:06 10 agree with you there, vertically.

12:08:09 11 Q So my point is that Figure 8 doesn't
12:08:42 12 directly show the connections between the yellow
12:08:46 13 metal and the brown metal on top of it at the
12:08:49 14 location where your first arrow is. So are you
12:08:58 15 speculating that the yellow is connected to the Out+
12:09:02 16 terminal?

12:09:09 17 A That's what I concluded.

12:09:18 18 Q And the first arrow that you added to the
12:09:38 19 figure, it kind of traces one of those fingers in
12:09:44 20 yellow. So you're not disputing that yellow finger
12:09:49 21 is not part of the LC circuit, right?

12:09:58 22 A If you don't mind -- okay, first of all,
12:10:02 23 we're talking about the long red arrow.

12:10:05 24 Q That's right.

12:10:06 25 A And I think we agree about that. Would you

12:10:08 1 mind just asking that in a way -- I just want to
12:10:11 2 make sure. I heard a couple notes and I just want to
12:10:15 3 make sure.

12:10:16 4 Q Apologies.

12:10:17 5 A It's no problem. Just to be clear for me.

12:10:19 6 Q Yeah, let me rephrase that.

12:10:21 7 So is that finger covered by the long red
12:10:27 8 arrow part of the LC circuit in Gonzalez?

12:10:34 9 A I think that's fair to say. It's part of a
12:10:46 10 connection.

12:10:49 11 Q Moving down to the next paragraph, which is
12:11:32 12 paragraph 103.

12:11:38 13 A Okay, I'm there.

12:11:39 14 Q I think here you are showing metal layers in
12:11:49 15 part of Figure 8 that's under the brown layers,
12:11:52 16 right?

12:11:56 17 A Yeah, that's right. Like a colorful totem
12:12:00 18 pole of metal layers to get down to the blue layers.

12:12:16 19 Q The part that you zoomed in, do you know
12:12:22 20 there -- do you know the purpose or the function of
12:12:25 21 these additional layers that you labeled as pink,
12:12:34 22 green, light blue or dark blue?

12:12:39 23 A The way I see it is -- and I called it a
12:12:46 24 colorful totem pole, I see it as a way to depict the
12:12:51 25 connection going down from upper layers to lower

12:12:56 1 layers.

12:13:07 2 Q And do you think these same layers that you
12:13:12 3 zoomed in here, would they extend into the region
12:13:15 4 under the yellow fingers?

12:13:24 5 A Okay, I don't -- I don't understand what
12:13:27 6 you're asking.

12:13:29 7 Q So for instance, you have a pink metal layer
12:13:35 8 here in the zoomed-in part, right?

12:13:38 9 A Yes.

12:13:39 10 Q Would the pink metal layer exist in the
12:13:44 11 region that's directly below the ten yellow fingers?

12:13:52 12 A The way I've interpreted this is there are
12:14:02 13 multiple metal layers, one on top of the other, and
12:14:19 14 the pink layer would be at that same height, you
12:14:31 15 might say, underneath all the structures that we
12:14:39 16 see. But we don't see an actual pink structure,
12:14:44 17 meaning that what's not depicted is a structure
12:14:49 18 actually on the pink layer even though the pink
12:14:53 19 layer like could have been, you know, at different
12:14:59 20 locations.

12:15:03 21 Q So the pink is part of the connection from
12:15:12 22 upper layers to lower layers at the location where
12:15:15 23 you zoomed in. But Figure 8 doesn't show the same
12:15:21 24 connection using that pink layer in the region
12:15:25 25 directly under the ten yellow fingers, right?

12:15:30 1 A Yeah, that's right. You don't see the
12:15:33 2 colorful totem pole in -- you know, around the
12:15:43 3 fine-tuning varactors.

12:15:48 4 Q And we don't see the green layer or the
12:15:53 5 light blue layer either under the ten yellow
12:16:00 6 fingers, is that right?

12:16:03 7 A That's right. I don't see structures there
12:16:07 8 with those colors.

12:16:09 9 Q And Figure 8 shows that only the dark blue
12:16:26 10 metal layer is under those yellow fingers, right?

12:16:38 11 A I agree with that.

12:16:40 12 Q By the way, in the zoomed-in view here, how
12:17:14 13 many metal layers in total do you see?

12:17:17 14 A I'm going to count up from dark blue so I'm
12:17:29 15 not going to count white. I'd answer seven.

12:18:03 16 Q Okay.

12:18:04 17 A Because I'm counting -- I'm sorry.

12:18:07 18 Q I see seven too, so that makes sense to me.

12:18:11 19 A Yeah, and I'm -- because I'm counting two
12:18:13 20 browns. Remember how I said the brown is sort of
12:18:17 21 divided.

12:18:18 22 Q That's fine. I understand. So there are --
12:18:24 23 so you'd agree that there is a dark blue, light
12:18:28 24 blue, green, pink, yellow, brown and brown? That's
12:18:34 25 seven in total, right?

12:18:36 1 A Yeah, that's how I was counting.

12:18:39 2 Q Can you go to paragraph 118? I think there

12:18:50 3 you are discussing more about these layers.

12:18:54 4 A Okay, I'm there.

12:18:55 5 Q So in paragraph 118, you show a zoomed-in

12:19:04 6 view of where it has two brown layers and a yellow

12:19:09 7 layer at the bottom, right?

12:19:13 8 A Yes.

12:19:13 9 Q So the yellow layer at the bottom in the

12:19:21 10 zoomed-in view, that's part of the same metal layer

12:19:25 11 as the yellow fingers, right?

12:19:31 12 A That's how I've interpreted things is that

12:19:34 13 the yellow is all at one height in the same layer.

12:19:38 14 Q So if you look at the zoomed-in view, so the

12:19:55 15 yellow metal layer actually follows the brown layer

12:19:58 16 all the way till the end of that brown layers,

12:20:04 17 right?

12:20:07 18 A I'm not sure I understand your question.

12:20:09 19 Q So the inductor -- sorry, strike that.

12:20:18 20 So you see two big blocks of brown, one is

12:20:25 21 annotated Out+, the other is Out-. You see those

12:20:29 22 two, right?

12:20:30 23 A Yes.

12:20:30 24 Q And on both sides, there's a metal layer

12:20:40 25 under those two brown layers, right?

12:20:48 1 A At the bottom?

12:20:51 2 Q Right.

12:20:51 3 A I see it.

12:20:53 4 Q So my question is based on your zoomed-in
12:20:57 5 view, does the yellow metal layer follow the two
12:21:02 6 brown layers on top all the way till the end of the
12:21:06 7 brown layers?

12:21:14 8 A I don't know that I agree with that. First
12:21:18 9 of all, the brown is sort of opaque and it's -- you
12:21:25 10 can't see much about the yellow underneath. I would
12:21:28 11 agree that when you're at the bottom in that
12:21:32 12 zoomed-in view, the yellow is there.

12:21:38 13 Q Yeah.

12:21:38 14 A I don't know that I agree -- oh, sorry.

12:21:41 15 Q I probably -- it was poor wording on my
12:21:44 16 part.

12:21:45 17 So my question was does the yellow metal
12:21:49 18 follow the brown layer all the way till the bottom
12:21:52 19 of that brown layer?

12:21:56 20 A I don't know that I agree with that. I see
12:22:02 21 -- I see it in the zoomed-in view at the bottom, but
12:22:05 22 I don't know that I agree with this, you know,
12:22:08 23 follow all the way down.

12:22:10 24 Q So you think the brown layer -- sorry.
12:22:14 25 Strike that.

12:22:15 1 So you think the yellow metal layer might
12:22:20 2 have gaps or breaks between the part that's in the
12:22:24 3 middle and then the part at the bottom that's shown
12:22:27 4 in the zoomed view?

12:22:32 5 A I think there's lots of options for how the
12:22:35 6 yellow could be shaped. I think that could include
12:22:38 7 gaps.

12:22:48 8 Q Would you think it's a reasonable
12:22:53 9 interpretation to say that the yellow metal layer
12:22:55 10 would follow the brown layer to the bottom of that
12:22:59 11 brown layer?

12:23:07 12 A I'm not quite sure I understand when you're
12:23:09 13 saying follow. Maybe if I can just make sure I
12:23:15 14 understand what you're asking. I'm not quite sure.

12:23:18 15 Q Yeah. Let me see if I can share my screen.
12:23:38 16 Do you see my screen, Dr. Phinney?

12:23:40 17 A Yes.

12:23:41 18 Q I'm going to make a snapshot of this here.
12:23:56 19 I'm going to draw a line in green. Do you see a
12:24:10 20 green arrow that I drew on this snapshot?

12:24:17 21 MR. HALVERSON: Charles, can you make it
12:24:19 22 bigger at all? It's on a screen in the room, but
12:24:22 23 it's --

12:24:27 24 THE WITNESS: Okay, I see that green arrow
12:24:29 25 now.

12:24:30 1 MR. HALVERSON: Thank you.

12:24:30 2 BY MR. LIU:

12:24:32 3 Q So my question is would you think the yellow
12:24:36 4 metal layer would follow the brown layer on top to
12:24:46 5 the bottom as indicated in the green arrow?

12:24:59 6 A Oh, this is something I address in
12:25:04 7 paragraph 127 of my report or my declaration. And I
12:25:08 8 think there's so many possibilities, so many options
12:25:12 9 for how the yellow layer could be shaped underneath
12:25:16 10 because we don't see it.

12:25:17 11 Q Okay. But what I drew in the green arrow,
12:25:26 12 would that be a reasonable interpretation based on
12:25:31 13 your understanding of Gonzalez?

12:25:41 14 A It's one of those many options that I
12:25:45 15 mentioned. You could say it that way. It's -- it's
12:25:52 16 not shown. So I do agree that the -- where we do
12:26:02 17 see that yellow, I think it needs to have the Out+
12:26:08 18 signal. But the form of those connections and the
12:26:14 19 form of the conductors on that yellow layer are not
12:26:18 20 visible. They're not shown.

12:26:22 21 Q Do you have any reasons to doubt that the
12:26:36 22 yellow -- let me draw another -- I just drew a
12:26:51 23 second green arrow following the direction of one of
12:26:57 24 those fingers.

12:27:00 25 So my question is do you have any reasons to

12:27:03 1 doubt that the shorter red arrow -- sorry. Strike
12:27:09 2 that.

12:27:09 3 Do you have any reasons to doubt that the
12:27:10 4 shorter green arrow would be disconnected from the
12:27:17 5 longer -- from the yellow metal layer indicated by
12:27:23 6 the longer green arrow?

12:27:27 7 MR. HALVERSON: Objection, form.

12:27:28 8 THE WITNESS: I think the yellow there is
12:27:35 9 connected to the Out+. It's just that the shape of
12:27:44 10 what that yellow is behind the brown is just
12:27:47 11 something that's not shown.

12:27:54 12 BY MR. LIU:

12:28:11 13 Q So I'm drawing a double arrow in green at
12:28:15 14 the bottom of the yellow layer. Do you see that?

12:28:18 15 A Yes.

12:28:19 16 Q So you'd agree that part is also connected
12:28:24 17 to the Out+ terminal, right?

12:28:27 18 A That's what I concluded, that it goes back
12:28:32 19 to the ambiguity I mentioned where sometimes you do
12:28:36 20 see that yellow layer underneath the brown layer and
12:28:39 21 it really shouldn't be connected even though it's
12:28:42 22 drawn the same way. But I concluded that I think
12:28:45 23 that that's connected there.

12:28:51 24 Q Okay. Thank you. I'm going to save this as
12:29:02 25 a screenshot and upload it I guess just for the

12:29:06 1 record. Give me a minute.

12:29:12 2 A By the way, my Zoom is down and it says my
12:29:17 3 network connection is --

12:29:21 4 MR. HALVERSON: We're still on in the room.

12:29:26 5 THE WITNESS: I'm going to get back in with
12:29:28 6 my exhibit share if that's all right.

12:29:31 7 MR. LIU: We can take a break. I think we
12:29:33 8 have been going for a while maybe.

12:29:35 9 VIDEOGRAPHER: Going off the record. The
12:29:36 10 time is 12:29 p.m.

12:29:36 11 (Whereupon, the deposition in the
12:29:36 12 above-entitled cause was recessed
12:29:36 13 to 1:06 p.m. this date.)

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12:58:06 1 A F T E R N O O N S E S S I O N

13:00:42 2 VIDEOGRAPHER: Going back on the record.

13:06:30 3 The time is 1:06 p.m. This marks the beginning of

13:06:34 4 media Number 3. Please continue.

13:06:34 5 CROSS EXAMINATION (resumed)

13:06:34 6 BY MR. LIU:

13:06:36 7 Q Welcome back, Dr. Phinney. So did you

13:06:41 8 confer with counsel during any of the breaks today

13:06:44 9 on your testimony?

13:06:46 10 A No.

13:06:48 11 Q Thank you. I would like to just note for

13:06:56 12 the record I uploaded Phinney Exhibit 1, which is a

13:06:59 13 screenshot of my annotations in the figure in

13:07:04 14 paragraph 118 of Dr. Phinney's declaration.

13:07:04 15 (Phinney Exhibit 1 marked for

13:07:08 16 identification.)

13:07:08 17 BY MR. LIU:

13:07:09 18 Q Dr. Phinney, I would like to continue

13:07:10 19 discussing Figure 8. So if you could go back to

13:07:17 20 Exhibit 1005, the Gonzalez reference. Are you

13:07:30 21 there?

13:07:30 22 A Yes.

13:07:31 23 Q The top part of Figure 8 shows an inductor.

13:07:37 24 And my question is when this inductor gets connected

13:07:41 25 to the MOS varactors, does its orientation matter?

13:07:51 1 A I'm not quite sure what you're asking.

13:08:12 2 Q So for example, would you consider rotating
13:08:19 3 it by 90 degrees?

13:08:22 4 MR. HALVERSON: Objection, form.

13:08:25 5 THE WITNESS: It could be positioned in
13:08:29 6 different ways and be connected to other structures.
13:08:38 7 BY MR. LIU:

13:08:48 8 Q Would a POSITA know that the orientation of
13:08:55 9 the inductor would impact the performance of the LC
13:08:58 10 circuit?

13:09:00 11 A All right. There was just one word in that
13:09:03 12 I didn't quite hear.

13:09:05 13 Q Would a POSITA know that the orientation of
13:09:09 14 the inductor would impact the performance of the LC
13:09:12 15 circuit?

13:09:13 16 A I guess it depends on what the orientation
13:09:26 17 is and with respect to what.

13:09:32 18 Q For example, if the extension-conductor
13:09:43 19 segments of the inductor, if they are aligned with
13:09:50 20 the brown metal shown at the bottom of Figure 8,
13:09:56 21 would that configuration be better than an
13:10:02 22 alternative configuration where the
13:10:05 23 extension-conductor of the inductor is rotated
13:10:13 24 90 degrees with respect to the bottom of Figure 8?

13:10:19 25 MR. HALVERSON: Objection, form.

13:10:20 1 THE WITNESS: I think you're asking me if
13:10:36 2 there's still a connection, but it's -- there's
13:10:42 3 somehow a rotation in the inductor with respect to
13:10:56 4 the varactors?

13:10:57 5 BY MR. LIU:

13:10:57 6 Q That's right.

13:10:58 7 A A person of ordinary skill would know that
13:11:11 8 the interconnection, the length and route could have
13:11:19 9 an effect on the circuit.

13:11:21 10 Q So to you as an expert, would it make sense
13:11:30 11 that the extension-conductor segment of the inductor
13:11:38 12 would be lined up with the MOS varactors as is shown
13:11:42 13 in Figure 8?

13:11:46 14 MR. HALVERSON: Objection, form.

13:11:46 15 THE WITNESS: So I'm not sure when you're
13:11:51 16 asking your question that -- because Figure 8
13:11:55 17 doesn't show that lined up part. So I'm not sure if
13:11:59 18 that's what you meant when you asked the question.

13:12:03 19 BY MR. LIU:

13:12:04 20 Q So the brown metal here, do you consider
13:12:12 21 that as part of the extension-conductor segment?

13:12:16 22 MR. HALVERSON: Objection, form.

13:12:18 23 THE WITNESS: Well, it's labeled Out+ and
13:12:22 24 Out-, but the connection isn't shown. So it's
13:12:26 25 something where we know that, you know, you might

13:12:28 1 say the signal, but you don't see how all this is
13:12:33 2 constructed together.

13:12:37 3 BY MR. LIU:

13:12:38 4 Q Assuming those brown metals are the
13:12:41 5 extension-conductor segment, I mean does this
13:12:47 6 configuration make sense to you from designing an LC
13:12:52 7 circuit?

13:12:55 8 A You know, you said assuming they're an
13:13:00 9 extension-conductor segment and that has a lot of
13:13:03 10 limitations in the claim. So and I think you're
13:13:09 11 asking me to assume that all those limitations are
13:13:11 12 met.

13:13:11 13 Q Okay. I'm not asking you to assume that.
13:13:14 14 So let me rephrase my question.

13:13:17 15 Would you consider -- would a POSITA
13:13:20 16 consider rotating the two brown metals by 90 degrees
13:13:26 17 in the bottom of Figure 8?

13:13:32 18 A I think they could consider a lot of things
13:13:34 19 to make the connection. The connection of
13:13:38 20 everything isn't shown in one place so they could --
13:13:44 21 they could consider different alternatives.

13:13:47 22 Q Are there benefits in -- sorry. Strike
13:14:07 23 that. Let's just move on and cover another aspect
13:14:10 24 of Gonzalez.

13:14:15 25 Gonzalez talks about a transmission, line,

13:14:18 1 right? Do you recall?

13:14:22 2 A I think that's fair.

13:14:25 3 Q Do you know what a transmission line is?

13:14:28 4 A Yes.

13:14:30 5 Q What is a transmission line?

13:14:34 6 A You can think of it like a distributed as
13:14:41 7 opposed to a lumped system where it's like there's a
13:14:47 8 length of something we often just call a line or a
13:14:52 9 transmission line. And it can have voltage and
13:14:58 10 current that vary along the length, how they're
13:15:03 11 analyzed and they can be terminated in a special
13:15:05 12 way. So they're a way to convey signals along that
13:15:11 13 line, but where we're thinking a little bit more
13:15:16 14 about how voltage and current vary down the length
13:15:23 15 of the line because the length is often larger
13:15:27 16 compared to the wavelength, let's say.

13:15:31 17 Q Thank you. Can you go to Gonzalez at
13:15:35 18 page 7?

13:15:37 19 A Okay, I'm there.

13:15:44 20 Q In Section IV, there are two subsections.
13:15:50 21 4A is on physical design and integration of EM
13:15:56 22 models. Do you see that?

13:15:57 23 A Yes.

13:15:58 24 Q In that Section 4A, about five lines down it
13:16:10 25 says, the structure in Figure 8 is simulated using

13:16:17 1 an EM simulator, right?

13:16:20 2 A Yes.

13:16:21 3 Q Going down on the same page, now in

13:16:32 4 Section 4B, parameterized EM modelling. Do you see
13:16:38 5 that?

13:16:38 6 A Yes.

13:16:39 7 Q The first sentence says, "The previous
13:16:41 8 approach is suitable for fixed layout structures
13:16:47 9 requiring EM models."

13:16:50 10 See that?

13:16:51 11 A Yes.

13:16:52 12 Q So here the previous modelling approach
13:16:57 13 refers to Section 4A, right?

13:17:02 14 A That's my understanding.

13:17:03 15 Q And it says in that same paragraph, to
13:17:22 16 adjust the length of a TL, an alternative modelling
13:17:28 17 approach has been used, right?

13:17:33 18 A Yes.

13:17:33 19 Q I think that TL -- sorry. In next
13:17:43 20 paragraph it says, "The TL used in this study is
13:17:46 21 illustrated in Figure 9."

13:17:48 22 Do you see that?

13:17:48 23 A Yes.

13:17:49 24 Q So fair to say that Figure 9, which is on
13:18:02 25 page 8, Figure 9 doesn't use the same modelling

13:18:08 1 approach as Figure 8?

13:18:10 2 A I think you could say that. The
13:18:18 3 parameterized EM modelling is where the length of
13:18:22 4 these different microstrip lines can be -- you can
13:18:29 5 adjust it.

13:18:30 6 Q So Figure 9 here shows a microstrip
13:19:02 7 transmission line. So my question is in your
13:19:08 8 opinion, would -- a microstrip transmission line, is
13:19:13 9 that part of the LC circuit?

13:19:21 10 A No.

13:19:22 11 Q Sorry?

13:19:23 12 A No.

13:19:24 13 Q So they are outside of the LC circuit, but
13:19:35 14 still part of the VCO, right?

13:19:39 15 A I'd agree with that.

13:19:40 16 Q I don't believe Figure 8 shows any
13:19:54 17 transmission lines, but correct me if I'm wrong.

13:19:59 18 A I don't see any there.

13:20:00 19 Q So below Figure 9 in the bottom paragraph in
13:20:41 20 that column, I think in the middle of that
13:20:45 21 paragraph it says, However, to make microchips in
13:20:50 22 CMOS technology, the choices of width and height are
13:20:53 23 also constrained by the technology design rules.

13:20:56 24 Do you see that?

13:20:58 25 A I do, with the one exception that the word

13:21:01 1 microchip that you said reads microstrip.

13:21:05 2 Q Sorry. And the next immediately after that
13:21:13 3 sentence it says, Figure 9 illustrates the
13:21:17 4 realization of a microstrip line using the top metal
13:21:21 5 level (M6) as a conducting strip and the two bottom
13:21:26 6 metal layers (M1 plus M2) as ground plane.

13:21:34 7 Do you see that?

13:21:35 8 A Yes.

13:21:35 9 Q So here, the design rules of having six
13:21:43 10 metal layers refer to Figure 9, right?

13:21:47 11 A This is in the context of talking about the
13:22:03 12 microstrip cross-section. And I had interpreted
13:22:09 13 this -- because of that additional phrase in front
13:22:14 14 of the discussion of the six metal layers, it says
13:22:18 15 in the case of the 65 nanometer CMOS technology, so
13:22:26 16 where it was really -- that indicated to me that
13:22:33 17 there were six layers available in that technology
13:22:35 18 node.

13:22:37 19 Q I think we discussed earlier today that you
13:22:51 20 counted that there are seven metal layers in
13:22:53 21 Figure 8, right?

13:22:55 22 A Yes, where I was counting a brown twice.

13:23:01 23 Q Right. So why would there be seven metal
13:23:09 24 layers in Figure 8 if the design rules say only six
13:23:13 25 metal layers is available?

13:23:16 1 A One reason I can think of is that Figure 8
13:23:20 2 is not intended to show structure in as punctilios
13:23:30 3 detail as we might think as related to particular
13:23:34 4 metal layers. And this goes to what I've said about
13:23:39 5 the views of Figure 8 not necessarily being
13:23:42 6 combinable teachings because of their different
13:23:46 7 colors and layers and thicknesses.

13:23:52 8 Q But before any combination, the bottom part
13:23:56 9 of Figure 8 itself has at least seven layers
13:24:00 10 according to your testimony, right?

13:24:04 11 A Yeah, I counted seven, but I double-counted
13:24:08 12 brown. But like, for instance, what if, you know,
13:24:12 13 the lower brown is like a via under the brown or --
13:24:17 14 you know, we don't really know because this isn't a
13:24:22 15 set of masks for a product. You know, this is --
13:24:28 16 this is a three-dimensional view in a research
13:24:34 17 paper.

13:24:36 18 Q Is it reasonable that the design rules
13:24:39 19 actually refer to the illustration of the
13:24:44 20 transmission line in Figure 9, but it doesn't -- the
13:24:48 21 rules don't apply to Figure 8?

13:24:53 22 A I think it's reasonable because it can show
13:24:57 23 that the depictions that we're seeing are, you know,
13:25:03 24 intended to convey certain information to the
13:25:06 25 reader, but not be like a set of masks for a

13:25:10 1 product.

13:25:11 2 Q And Figure 9 is part of an alternative
13:25:36 3 modelling approach compared to Figure 8, right?

13:25:41 4 A That's the way I've understood it when we
13:25:44 5 were looking at the division in Section IV of
13:25:47 6 Section A and B.

13:25:51 7 Q Could you go to Figure 5 in Gonzalez on
13:26:15 8 page 6?

13:26:17 9 A Okay, I'm there.

13:26:19 10 Q Does Figure 5 show a differential varactor?

13:26:31 11 A Yes, fine-tuning differential varactor
13:26:42 12 structure.

13:26:42 13 Q Do you know what is a differential varactor
13:26:56 14 compared to a regular varactor, I guess?

13:27:00 15 A Yeah. This would be connected in the
13:27:02 16 differential position so that the -- it includes
13:27:10 17 like a neutral point, meaning that it could be
13:27:14 18 operated in a balanced manner so that the Out+ and
13:27:29 19 the Out- are like a seesaw, one's going up when the
13:27:36 20 other goes down and the neutral point is balanced --
13:27:43 21 at a balance point between equal and opposite
13:27:52 22 voltages on either end.

13:27:54 23 Q I'm trying to understand how this
13:27:58 24 differential varactor works. So if you can help me
13:28:02 25 out, for example, using the upper right part of

13:28:07 1 Figure 5, it shows a cross-sectional view, right?

13:28:11 2 Do you see that?

13:28:12 3 A Yeah.

13:28:12 4 Q So my understanding is that a differential
13:28:19 5 varactor essentially has two varactors. Is that
13:28:23 6 fair?

13:28:24 7 A Yeah.

13:28:25 8 Q So in this cross-section, you have Out+ and
13:28:35 9 Vc. Does that part form like one of those two
13:28:40 10 varactors?

13:28:43 11 A The varactor itself goes from the N+ poly,
13:28:50 12 which is a gate, and then under the gate oxide. So
13:28:53 13 most of the energy stored in the capacitance is in
13:28:55 14 that thing that says GOX. So that means gate oxide.
13:29:00 15 So that's where the action is. And there's an
13:29:03 16 inversion layer in the bulk down underneath there.
13:29:07 17 And so additional -- additional charge, the other
13:29:12 18 end of that variable capacitor, but that amount of
13:29:17 19 modulated charge on that other part of the varactor
13:29:20 20 can be modulated by changing the N+ bias, that will
13:29:26 21 sort of eat into the -- eat into the modulated
13:29:32 22 charge underneath the gate oxide.

13:29:37 23 Q So the N+ poly forms the gate electrode,
13:29:44 24 right?

13:29:44 25 A Yes.

13:29:44 1 Q The other electrode in the varactor, you
13:29:49 2 said it's in the N+ well?

13:29:54 3 A Can you ask that again? I'm sorry.

13:29:56 4 Q I'm trying to understand. So is the other
13:29:58 5 electrode in that varactor in that N+ well under the
13:30:06 6 Vc?

13:30:14 7 A It could be there. I think a lot of the
13:30:19 8 conduction can occur through the N+ diffusion that's
13:30:22 9 biased by Vc or -- but also Nwell. There can be
13:30:35 10 conduction there back out through the other --
13:30:39 11 through the Out-. So it's like back-to-back diodes
13:30:45 12 that include a capacitance and so that's why they're
13:30:48 13 drawn as like diodes with an extra line at the
13:30:57 14 cathode.

13:30:58 15 Q So on the other side, I guess you've got
13:31:03 16 sort of a symmetrical structure that forms the other
13:31:09 17 one of the differential varactors, is that fair?

13:31:12 18 A Yeah.

13:31:12 19 Q So my understanding is that the Vc provides
13:31:19 20 the control voltage to modulate the capacitance in
13:31:24 21 this varactor?

13:31:26 22 A Yes.

13:31:26 23 Q And the Out+ and Out-, they are connected to
13:31:34 24 inductor terminals?

13:31:38 25 A Ultimately through -- but that's what the

13:31:45 1 Out+ and Out- means is that that's the signal that's
13:31:49 2 put there. That's what it means to be connected at
13:31:52 3 that differential position, but the wires used to do
13:32:01 4 that aren't depicted in Gonzalez.

13:32:10 5 Q Let's talk about that. So here do you see
13:32:15 6 -- on the left side of Figure 5, do you see two sort
13:32:20 7 of F-shaped structures each with two horizontal
13:32:26 8 lines and one vertical line?

13:32:27 9 A Yes. The F-shaped structures, yes.

13:32:32 10 Q And one is annotated with Out+, the other is
13:32:43 11 annotated with Out- right?

13:32:47 12 A Yes.

13:32:47 13 Q The two F-shaped structures, are they metal
13:32:57 14 wires?

13:32:58 15 A I think that's right. The ultimate
13:33:09 16 connection to the Out+ and Out-, they're labeled
13:33:14 17 Out+ and Out- but really the shape of everything to
13:33:18 18 get back to the Out+ and Out- that we see in other
13:33:21 19 views, that's the thing that's not depicted.

13:33:25 20 Q But you agree that electrically they are
13:33:28 21 connected to the Out+ and Out- terminals of the
13:33:32 22 inductor, right?

13:33:35 23 A Electrically, I agree with that. That's --
13:33:40 24 they're labeled that Out+ and Out- to indicate that
13:33:45 25 it's that same signal.

13:33:48 1 Q Do you see the gray-colored area? I believe
13:34:07 2 there are eight of them in that figure.

13:34:12 3 A Yes, I see those. Those are the darker
13:34:15 4 gray, not the lighter gray.

13:34:17 5 Q Yeah, sorry. The darker gray areas they
13:34:25 6 extend vertically, right, eight of them?

13:34:29 7 A Yes.

13:34:30 8 Q Do you know -- so are those the poly gates?

13:34:43 9 A Yes, that's how I interpreted that N poly
13:34:49 10 gates and so you can see that four of them are
13:34:53 11 connected to Out- and four of them are connected to
13:34:57 12 Out+ which make sense because this is depicting a
13:35:00 13 2x2 differential varactor where each one of the four
13:35:07 14 differential varactors will have one Out+ and one
13:35:10 15 Out- connection.

13:35:12 16 Q And poly here means polysilicon, right?

13:35:22 17 A Yes, highly doped though. So when it says
13:35:25 18 N+ poly, it would be like 1025 doping.

13:35:29 19 Q It's highly doped silicon?

13:35:31 20 A Yeah, highly doped polysilicon.

13:35:34 21 Q Sorry. So the highly doped polysilicon is a
13:35:44 22 semiconductor, right?

13:35:45 23 A That's fair to say. It's just not
13:35:50 24 monocrystalline. It's not beautiful bulk
13:35:55 25 crystalline oriented silicon like in the bulk. It's

13:35:59 1 got greens and it's got imperfections, but it's
13:36:03 2 highly conductive.

13:36:04 3 Q But it's not metal, right?

13:36:15 4 A It's not metal. It's basically a silicon
13:36:19 5 lattice that has grain boundaries and grains. And
13:36:25 6 it would like almost like compacted gravel if you
13:36:29 7 looked at it close up. And it has many dopant atom
13:36:35 8 impurities, a very high concentration in there.

13:36:39 9 Q And those darker gray areas, they are
13:36:48 10 located below the F-shaped structures, right?

13:36:56 11 A The F shapes are kind of to connect to
13:37:01 12 those. So when you see those little Xs, the little
13:37:04 13 boxes with the Xs, that's the contact points. Where
13:37:09 14 you don't see an X in a box, that's an overpass
13:37:13 15 without a connection.

13:37:16 16 Q Thank you. But looking at the height, the
13:37:29 17 N+ poly gate in gray, darker gray, they are located
13:37:38 18 under the F-shaped metal wires?

13:37:45 19 A That's how I understand it because those
13:37:48 20 gates do need to be down very close to the bulk and
13:37:52 21 only separated from the bulk by a very thin gate
13:37:56 22 oxide. You normally think of that as below metals.

13:38:02 23 Q And those darker gray poly gates, they are
13:38:07 24 also perpendicular to the horizontal line part of
13:38:12 25 the F-shape?

13:38:13 1 A Yes.

13:38:14 2 Q And under the darker gray shape, do you also

13:38:34 3 see like four light blue boxes?

13:38:40 4 A Yes.

13:38:40 5 Q Do you know what are they?

13:38:44 6 A Like Nwells.

13:38:55 7 Q So you think they map to the like the Nwell

13:39:02 8 on the right-hand side that has this hashed shape,

13:39:10 9 using hash, right?

13:39:11 10 A Yeah, that's what I think those are.

13:39:15 11 Sometimes you think of that as like defining like an

13:39:19 12 active region because between those can be called a

13:39:25 13 field oxide. So it's -- you know, that's defining

13:39:31 14 where the action is as far as interaction with the

13:39:34 15 bulk, those blue areas.

13:39:36 16 Q But the Nwell on the right-hand side and the

13:39:41 17 left-hand side, it doesn't match the -- I guess what

13:39:45 18 I'm trying to say is the color of the Nwell on the

13:39:50 19 right side doesn't match the color of the Nwell on

13:39:56 20 the left, right?

13:39:58 21 A Yeah, that's right. The Nwell that you see

13:40:02 22 there isn't blue.

13:40:07 23 Q I guess this figure is not perfect in the

13:40:17 24 coloring.

13:40:19 25 A I think that makes sense. It's -- the

13:40:24 1 figure on the right of Figure 5 uses blue for that
13:40:28 2 Vc and Out+ and then the Out+ as we saw is more like
13:40:33 3 dark gray looking. And yeah, so it's not -- it's
13:40:38 4 not perfectly consistent.

13:40:39 5 Q By the way, the left side here shows a top
13:40:52 6 view, the right side shows a cross-sectional view,
13:40:55 7 right?

13:40:56 8 A Yes.

13:40:56 9 Q I'm trying to understand. So where would
13:41:01 10 you think the cross-section is cut on the left-hand
13:41:06 11 side to lead to the view that we see here on the
13:41:09 12 right-hand side?

13:41:12 13 A So I think it needs to be -- it's an
13:41:19 14 interesting point because there's staggered
13:41:23 15 connections. From the top view, you can tell that
13:41:30 16 there's staggered connections to Out+ and Out- so
13:41:32 17 you never see Out+ and Out- connections at the same
13:41:37 18 vertical level on the left. So in a way, this
13:41:46 19 cross-section is kind of a fictitious summary of
13:41:50 20 what would happen if there was a vertical alignment
13:41:56 21 on the left of the Out+ and Out- connections and so
13:42:00 22 you could see all the salient connections at least
13:42:04 23 aligned in one plane so you can get a sense of what
13:42:08 24 they look like even though they're actually in and
13:42:10 25 out of that plane.

13:42:12 1 Q On the right side, the Out+ and Out-, their
13:42:19 2 top is on the same vertical level, right?

13:42:24 3 A That's how it's shown, yeah. But I was
13:42:31 4 referring to that on the left that -- when I was
13:42:37 5 talking about vertical, I meant like viewed from the
13:42:41 6 top on the left, you notice that like when those
13:42:45 7 F-shapes, those F-shapes don't have like their top
13:42:48 8 bar aligned. They're sort of offset from one
13:42:53 9 another and the cross-section kind of ignores that
13:42:58 10 detail, but rather gets a cross-section to show the
13:43:03 11 Out+ and Out- connections in one plane.

13:43:06 12 Q Okay. Well, this Figure 5 like it has
13:43:10 13 certain imperfections, for example, the coloring is
13:43:14 14 not like consistent. So would it be -- is it
13:43:16 15 possible that on the left-hand side, the two
13:43:24 16 F-shape, they're slightly inaccurately shown on
13:43:30 17 their vertical level, that they're actually on the
13:43:33 18 same -- on the same level as shown on the right
13:43:36 19 side?

13:43:39 20 A The way you're asking this, I'm not sure
13:43:43 21 we're on the same page with the level. And so I'm
13:43:48 22 not -- I'm not sure I'm understanding your question
13:43:51 23 because when you're asking this, I'm wondering if
13:43:54 24 when I'm saying vertical with respect to the left,
13:43:59 25 I'm wondering if you're thinking about that as being

13:44:01 1 like the height off the bulk in the cross-section
13:44:04 2 view. So I'm not -- I'm not sure I'm understanding
13:44:07 3 your question.

13:44:08 4 Q Let me simplify it. So is it possible that
13:44:16 5 the two F-shaped structures on the left side, that
13:44:22 6 they're vertically on the same level?

13:44:27 7 A Yeah, I think that's possible; by that I
13:44:34 8 mean height. That's how I'm interpreting your
13:44:37 9 question, at the same height.

13:44:39 10 Q Okay. I understand. Thank you. So if you
13:44:51 11 could go to -- still saying on page 6, but let me
13:44:59 12 see where is that. There is a Section IIIB on this
13:45:05 13 page. I think it's talking about the same part.
13:45:14 14 Maybe the -- there's one paragraph on that page
13:45:22 15 starting from "the varactors are implemented." Do
13:45:26 16 you see that?

13:45:27 17 A Yes.

13:45:27 18 Q A few lines down there it says, "The N+ poly
13:45:35 19 gates are each connected to one of the two
13:45:39 20 differential terminals (Out+, Out-). They are
13:45:45 21 placed in the same Nwell that is biased using a
13:45:50 22 common voltage (Vc). The differential current path
13:45:56 23 length is thus minimized."

13:45:58 24 Do you see that?

13:45:59 25 A Yes.

13:45:59 1 Q So here, like in Gonzalez, the differential
13:46:10 2 current path is minimized by placing the N+ poly
13:46:16 3 gate in the same Nwell, right?

13:46:22 4 A Yeah, I think that's right. You're killing
13:46:26 5 two birds with one stone. You have two -- the two
13:46:31 6 varactors in the one well and the connection between
13:46:35 7 them is through the bulk. It's not like you had one
13:46:41 8 of them and then you'd come out and then connect to
13:46:43 9 the second one through more metal. You build them
13:46:48 10 both connected cathode-to-cathode right through the
13:46:57 11 bulk.

13:46:59 12 Q And here it cites an article number 14. Did
13:47:06 13 you ever review that article art, number 14?

13:47:11 14 A I don't think I did.

13:47:14 15 Q That's okay. So here does minimizing the
13:47:28 16 current path have any impact on the VCO,
13:47:35 17 specifically on its quality factor?

13:47:38 18 A Could.

13:47:43 19 Q How?

13:47:47 20 A Let's say the current path were long and all
13:48:00 21 other things being equal, the OMIC loss will be
13:48:08 22 proportional to length which will diminish Q. So
13:48:16 23 higher OMIC loss essentially means higher series
13:48:20 24 resistance.

13:48:21 25 Q So one way of designing an LC circuit in a

13:48:39 1 VCO, so for example, when a capacitor is offset from
13:48:42 2 an inductor coil, can the quality factor still be
13:48:47 3 increased by reducing the differential current path?

13:48:52 4 A I think you asked can the quality factor
13:48:59 5 still be decreased? Is that what you asked?

13:49:01 6 Q I asked can the quality factor still be
13:49:04 7 increased by reducing the differential current path?

13:49:12 8 A I'd say so. You know, when you're talking
13:49:25 9 about making something shorter, all other things
13:49:29 10 being equal, that would tend to decrease the
13:49:33 11 resistance of that conduction path. And decreasing
13:49:40 12 resistance, generally speaking, is going to
13:49:44 13 increase Q.

13:49:51 14 Q Actually like the bottom of Figure 5 on the
13:49:54 15 same page, it actually lists the quality factor
13:50:02 16 versus a controlled Vc, right? Do you see that?

13:50:08 17 A Yes.

13:50:09 18 Q And here it says -- it shows quality factor
13:50:14 19 increases when Vc gets higher, right?

13:50:18 20 A Yes.

13:50:23 21 Q Do you know why?

13:50:32 22 A It could have to do with more -- more
13:50:46 23 conduction of AC current through more highly doped
13:50:54 24 N-type silicon.

13:50:57 25 Q So here the control when teaching Gonzalez

13:51:08 1 is not limited to 1.8 volts, but it actually has a
13:51:11 2 range, right, between 0 to 1.8 volts?

13:51:17 3 A Yes, I think that's right. And you know,
13:51:20 4 when we talk about continuously tuned varactor, it
13:51:24 5 can traverse -- the voltage can traverse this and
13:51:29 6 assume different intermediate values versus the
13:51:33 7 digitally tuned where it's more or less all the way
13:51:37 8 to one side or the other.

13:51:40 9 Q Right. So even though the V_c if it's below
13:51:46 10 1.8 might lead to a lower quality factor, Gonzalez
13:51:52 11 still uses that range of control voltage. So
13:51:55 12 Gonzalez is concerned with more than just the
13:51:59 13 quality factor, right?

13:52:11 14 A One thing I'd point out is I interpret this
13:52:14 15 quality factor to be the quality factor of the
13:52:21 16 capacitance. So that's not a system issue. That's
13:52:35 17 more like a component issue.

13:52:38 18 Q Would that quality factor of the capacitance
13:52:43 19 impact the overall quality factor of the LC circuit?

13:52:47 20 A Yes.

13:52:49 21 Q So I'm trying to ask, so quality factor of
13:53:17 22 the LC circuit is not the only consideration
13:53:19 23 involved in Gonzalez, right?

13:53:23 24 A Yeah, that's right. I think Gonzalez cares
13:53:26 25 about how high a frequency can be achieved.

13:53:31 1 Gonzalez cares about tuning range. And those are
13:53:33 2 things that are actually you see right in the title.
13:53:37 3 I think, you know, you can tell by the -- Gonzalez I
13:53:44 4 think was really kind of proud of this 17 percent
13:53:46 5 tuning range and talked about this as being like,
13:53:52 6 you know, a world record practically; that being a
13:53:56 7 really important measure.

13:54:14 8 Q I think we talked enough about Gonzalez. So
13:54:38 9 let me check if there's anything else.

13:54:42 10 Could you go to your declaration again in
13:54:45 11 paragraph 99.

13:54:51 12 A I'm there.

13:54:52 13 Q I think here in the beginning you say,
13:54:56 14 "Dr. Prucnal and I both agree that the varactors of
13:55:00 15 Gonzalez are not finger capacitors and lack any
13:55:05 16 connecting segment or electrode segment as are
13:55:10 17 required by the claims."

13:55:11 18 Do you see that?

13:55:11 19 A Yes.

13:55:12 20 Q Here, because you didn't cite a paragraph to
13:55:19 21 his declaration, so I'm curious where did
13:55:21 22 Dr. Prucnal say that the varactors are not finger
13:55:26 23 capacitors or that they lack any connecting segment
13:55:31 24 or electrode segments?

13:55:35 25 A Here this is where I'm -- as I've understood

13:55:39 1 Dr. Prucnal's position, he's saying that wires that
13:55:43 2 connect to the varactors, so things like the yellow
13:55:49 3 fingers that we were talking about, I think that's
13:55:55 4 what he's identifying as being electrode segments.
13:55:59 5 But then I don't think that he's gone and said that
13:56:02 6 the varactors down at that bulk with the gate oxide
13:56:05 7 are themselves -- those MOS capacitors aren't things
13:56:09 8 that have a connecting segment or electrode
13:56:15 9 segments.

13:56:16 10 Q Let me upload the next exhibit. I've just
13:57:04 11 uploaded the Niknejad reference which is
13:57:14 12 Exhibit 1007. Let me know when you have it.

13:57:14 13 (Document marked previously as
13:57:14 14 Exhibit 1007 was presented.)

13:57:20 15 THE WITNESS: Okay, I have it open.

13:57:21 16 BY MR. LIU:

13:57:21 17 Q Could you go to PDF page 26? The page that
13:57:30 18 shows Figure 3.10?

13:57:37 19 A Page 26.

13:57:42 20 Q Yeah. So in Figure 3.10, it mentions MIM
13:57:54 21 capacitors, right, the caption?

13:57:55 22 A Yes.

13:57:55 23 Q So MIM capacitors are parallel plate
13:58:05 24 capacitors, right?

13:58:05 25 A I think that's fair.

13:58:07 1 Q I think you said the finger capacitors are
13:58:11 2 sometimes called like MOM capacitors,
13:58:16 3 metal-oxide-metal?

13:58:18 4 A Yes.

13:58:20 5 Q And they're not the same thing, right, the
13:58:23 6 MIM and MOM?

13:58:25 7 A That's right. They are not the same thing.
13:58:29 8 MOM and MIM are different.

13:58:32 9 Q So the capacitors shown in Figure 10, that's
13:58:44 10 a parallel plate capacitor, not a finger capacitor,
13:58:51 11 right?

13:58:51 12 A I think that's a fair way to characterize
13:58:55 13 it. The MIM capacitor is sort of a specialized,
13:59:00 14 thin dielectric capacitor with a vertical electric
13:59:06 15 field.

13:59:06 16 Q Do you recall if AMD relied on this
13:59:19 17 Figure 3.10 on its invalidity ground in the IPR?

13:59:26 18 A I think so. I could check.

13:59:46 19 Q So I think the next page, page 27, has
14:00:09 20 Figure 3.11 and then after that is page 28. I think
14:00:16 21 it's the same section in terms of text. But I want
14:00:22 22 to direct your attention to one of these paragraphs.
14:00:27 23 Let me check.

14:00:30 24 The first paragraph on page 28, starting
14:00:38 25 from line number 3 it says, "In order to realize a

14:00:42 1 given capacitance, either a large number of short
14:00:45 2 fingers in parallel or a small number of long
14:00:48 3 fingers can be used. "

14:00:50 4 Do you see that?

14:00:51 5 A Yes.

14:00:52 6 Q And can you just, you know, finish reading
14:00:59 7 through the rest of that paragraph?

14:01:01 8 A Yes.

14:01:03 9 Q You're very familiar --

14:01:04 10 A Do you want me to do it out loud?

14:01:06 11 Q No, that's okay. You don't have to do --
14:01:09 12 you're very familiar with Niknejad and this
14:01:11 13 paragraph, right?

14:01:12 14 A Yes, this is one that I cited and discussed.

14:01:17 15 Q So here Niknejad says a large number of
14:01:23 16 short fingers results in larger lead parasitics,
14:01:29 17 right?

14:01:32 18 A Can you ask that again? I'm sorry.

14:01:35 19 Q So here, on Niknejad says a large number of
14:01:40 20 short fingers results in large lead parasitics,
14:01:46 21 right?

14:01:49 22 A It does. And that's part of its
14:02:11 23 characterization of the larger number of shorter
14:02:14 24 fingers more completely where it reads, "The former
14:02:17 25 structure results in smaller finger resistance and

14:02:22 1 inductance, but larger lead parasitics."

14:02:26 2 Q Right. And the former structure refers to a
14:02:30 3 large number of short fingers, right?

14:02:33 4 A Yes.

14:02:35 5 Q So a large number of short fingers results
14:02:40 6 in smaller finger resistance but larger lead
14:02:44 7 parasitics, accurate?

14:02:47 8 A Yes. And just the one other thing that was
14:02:51 9 thrown in that sentence is results in smaller finger
14:02:56 10 resistance and inductance.

14:02:59 11 Q Sorry. Let me try this again. So strike
14:03:04 12 that.

14:03:04 13 A large number of short fingers results in
14:03:07 14 smaller finger resistance and inductance but larger
14:03:11 15 lead parasitics?

14:03:14 16 A Yes.

14:03:16 17 Q And Niknejad says a small number of long
14:03:23 18 fingers on the other hand results in bigger finger
14:03:28 19 resistance, but smaller parasitics, right?

14:03:35 20 A Yeah, that's partially true. And you know,
14:03:39 21 if I were to be all complete about it with the
14:03:43 22 parallel that characterizing the opposite trade-off,
14:03:47 23 I'd say that the smaller number of longer fingers
14:03:52 24 would have smaller lead parasitics but result in
14:03:57 25 larger finger resistance and inductance.

14:04:00 1 Q Okay. Thank you. So it's basically a
14:04:21 2 trade-off between a large number of short fingers
14:04:26 3 and a small number of long fingers, right?

14:04:33 4 A For these two alternatives that Niknejad is
14:04:37 5 talking about, that's what he's saying there.

14:04:42 6 Q Okay. Would a POSITA reading Niknejad
14:04:51 7 consider using a small number of longer fingers
14:04:55 8 because it leads to smaller parasitics?

14:05:02 9 MR. HALVERSON: Objection, form.

14:05:02 10 THE WITNESS: I think it could depend on
14:05:19 11 what -- what design situation they're faced with.
14:05:26 12 They could be trying to fill up a square and not
14:05:28 13 really care. They could have a -- it would depend
14:05:36 14 on their situation, I guess.

14:05:38 15 BY MR. LIU:

14:05:55 16 Q So reducing parasitics here is a good thing?
14:06:00 17 It's a benefit, right?

14:06:02 18 A It's often thought to be a great thing to
14:06:10 19 reduce parasitics. One thing that's important to
14:06:13 20 realize is that you can be able to better manage
14:06:20 21 parasitics for some structures compared to others,
14:06:27 22 especially when -- in a MOM capacitor where you
14:06:32 23 really need to increase the density of capacitance
14:06:37 24 that you're realizing within a given area, you may
14:06:42 25 have not as many options there to improve the

14:06:48 1 capacitance density. And you may be able to better
14:06:53 2 manage or reduce parasitics associated with
14:06:58 3 connections to those MOM capacitor fingers.

14:07:04 4 Q Is reducing parasitics something this patent
14:07:23 5 tries to do, the '582 patent?

14:07:30 6 A I think there's a parasitic benefit is one
14:07:42 7 potential advantage to ultimately the purpose of
14:07:50 8 improving Q of an LC resonant circuit.

14:07:55 9 Q Does Niknejad, here in this paragraph, does
14:08:08 10 it favor either option? Is it one a large number of
14:08:15 11 short fingers or a smaller number of longer fingers?

14:08:20 12 MR. HALVERSON: Objection, form.

14:08:21 13 THE WITNESS: Well, Niknejad here is just
14:08:29 14 talking generally and so that's why I said it could
14:08:35 15 depend on -- you know, when a person of ordinary
14:08:40 16 skill is trying to do different things, they could
14:08:42 17 come up with different approaches to this trade-off.

14:08:46 18 But the one thing I was trying to mention
14:08:50 19 with the fingers and managing parasitics, another
14:08:54 20 way of putting that is in a MOM capacitor, you
14:08:57 21 probably want the teeth of your comb to be pretty
14:09:05 22 much as numerous and close together as you can make
14:09:11 23 them. You know, you're often trying to increase the
14:09:15 24 amount of capacitance per unit area. So you want
14:09:18 25 those teeth to be really close. And you may be able

14:09:21 1 to manage parasitics associated with the back of
14:09:24 2 comb, the connection to the teeth. You maybe have
14:09:27 3 more options and more degrees of freedom there to
14:09:31 4 offset some problems, but you can make it wider at
14:09:37 5 the back of the comb. Things like that. So there's
14:09:42 6 tons of trade-offs.

14:09:46 7 BY MR. LIU:

14:09:47 8 Q So just to make sure I understand, so you're
14:09:50 9 saying in a MOM capacitor, which is a finger
14:09:53 10 capacitor, you would want to maximize the density of
14:09:57 11 those fingers in order to get a higher capacitance?

14:10:04 12 A Yeah, a higher -- sorry.

14:10:06 13 Q Like per area or per voltage?

14:10:14 14 A That's about right, a higher capacitance
14:10:18 15 density. You know, imagine had you spent all that
14:10:22 16 area to have just one finger because you're relying
14:10:24 17 on sidewall capacitance. And imagine you built
14:10:29 18 something that, you know, had big, thick comb
14:10:36 19 fingers and then you'd have very few sidewalls. And
14:10:39 20 it's like, well, that wasn't great because now
14:10:41 21 you've spent a lot of area to get very little
14:10:44 22 capacitance. And do you see there's just a lot of
14:10:48 23 trade-offs in a capacitor.

14:10:54 24 Q So with the higher capacitance density in a
14:11:03 25 finger capacitor, you would have higher density

14:11:11 1 capacitance than a parallel plate capacitor, say a
14:11:17 2 MIM capacitor, right?

14:11:18 3 A I don't think that's really the case.
14:11:22 4 What's nice about a MIM, or this MIM capacitor, is
14:11:27 5 it has a specialized dielectric that's made just to
14:11:34 6 have a ton of capacitance per unit area. And with
14:11:39 7 the MOM capacitors, you're really -- you're relying
14:11:43 8 on your process and how close you can put different
14:11:49 9 metal layers. And I mean, bottom line, you'd have
14:11:55 10 to compare. But a MIM capacitor is sort of like an
14:12:02 11 extra capacitor specific feature that you can get in
14:12:09 12 some processes. I think it's quite dense actually
14:12:16 13 in terms of the capacitance per unit area.

14:12:19 14 Q So would someone like a POSITA know
14:12:24 15 generally which would have a higher density of
14:12:29 16 capacitance per unit area between the MOM and the
14:12:34 17 MIM?

14:12:36 18 A That's about right. You know, they're going
14:12:39 19 to have a process design kit and they're going to
14:12:45 20 know -- you know, usually a designer is part of a
14:12:48 21 team and there's going to be a lot of knowledge in
14:12:50 22 all the people working on a chip about like here's
14:12:54 23 what we got for capacitors, here's our options. And
14:12:57 24 people are going to have that somewhat
14:13:03 25 characterized, you know, in the course of their

14:13:04 1 work. They're not going to -- they'll have a sense
14:13:07 2 of how those two stack up.

14:13:12 3 Q So do you know on that -- between the MIM
14:13:17 4 and the MOM generally which one would have higher
14:13:21 5 density of capacitance, like --

14:13:27 6 A I think it can really vary. I don't know if
14:13:32 7 I could give you a general answer, but I have -- my
14:13:37 8 thought is that a MIM capacitor is actually quite
14:13:40 9 dense in terms of capacitance per unit area.

14:13:52 10 Q Have you -- you still recall the Muh
14:14:10 11 reference, right?

14:14:11 12 A Yes, Muh.

14:14:12 13 MR. HALVERSON: If we're going to switch, is
14:14:15 14 it a good time for a quick break?

14:14:17 15 MR. LIU: Yes. Thank you.

14:14:18 16 VIDEOGRAPHER: Going off the record. The
14:14:20 17 time is 2:14 p.m.

14:14:22 18 (Short recess.)

14:25:01 19 VIDEOGRAPHER: Going back on the record.
14:25:17 20 The time is 2:25 p.m. This marks the beginning of
14:25:21 21 media Number 4. Please continue.

14:25:23 22 BY MR. LIU:

14:25:25 23 Q Dr. Phinney, so next I'd like to talk about
14:25:28 24 the Muh reference. But before we turn to the Muh
14:25:32 25 reference, I'd actually like to clarify something

14:25:35 1 you said in your declaration about it. So could you
14:25:37 2 go to your declaration, which is Exhibit 2003,
14:25:42 3 paragraph 164.

14:25:57 4 A Okay, I'm there.

14:26:00 5 Q Here you said "Muh (and Niknejad)
14:26:04 6 deliberately position the capacitor of the LC
14:26:06 7 circuit in the area under the coil-conductor
14:26:11 8 segment."

14:26:11 9 Do you see that?

14:26:12 10 A Yes.

14:26:12 11 Q You say, "They do so because that
14:26:19 12 orientation improves the Q factor of the LC
14:26:26 13 circuit."

14:26:26 14 Do you see that?

14:26:27 15 A Yes.

14:26:28 16 Q In the paragraph immediately above that, you
14:26:56 17 have a Figure 3.10 from Niknejad which shows a MIM
14:27:04 18 capacitor. Do you see that?

14:27:06 19 A Yes.

14:27:07 20 Q I just want to make sure, so are you saying
14:27:12 21 here that Muh and Niknejad teaches against using a
14:27:19 22 finger capacitor?

14:27:27 23 A I think all the LC resonant circuits that
14:27:33 24 they're depicting are with MIM capacitors. So even
14:27:40 25 in the simulation in Muh, that too uses a parallel

14:27:46 1 plate-style MIM capacitor, at least it's sort of a
14:27:53 2 jury-rigged version. So yeah, they're all --
14:27:57 3 they're all using MIM capacitors when Niknejad shows
14:28:01 4 the ring oscillator, it's with the MIM. And
14:28:05 5 elsewhere in Muh, that's what it shows.

14:28:08 6 Q Could you go to paragraph 151? I think that
14:28:18 7 relates to your answer.

14:28:24 8 A Yeah, I'm there.

14:28:25 9 Q Actually, let's just move on. Can you go to
14:28:55 10 152 right below that? It's on the same page.

14:28:57 11 A Okay, I'm there.

14:28:59 12 Q You said here -- you said, "The focus of Muh
14:29:22 13 is to maximize the quality factor or Q factor of its
14:29:25 14 LC circuit." And you cite to Muh on page 31 and 41.
14:29:32 15 Do you see that?

14:29:33 16 A Yes.

14:29:33 17 Q So I just uploaded Exhibit 1006, Muh, during
14:29:42 18 the break. Do you have that?

14:29:44 19 A I have it. I have it open.

14:29:44 20 (Document marked previously as

14:29:44 21 Exhibit 1006 was presented.)

14:29:45 22 BY MR. LIU:

14:29:45 23 Q So I want to go to page 41 that you cite
14:29:48 24 here. In the first sentence it says, "To maximize
14:30:04 25 its Q factor and minimize its area, Ltank was

14:30:12 1 implemented as a center-tapped symmetric inductor
 14:30:15 2 rather than two single-ended signal inductors."

14:30:18 3 Do you see that?

14:30:19 4 A Yes.

14:30:20 5 Q So here it's saying that maximizing the Q
 14:30:26 6 factor was accomplished by using a center-tapped
 14:30:29 7 inductor rather than two single-ended inductors,
 14:30:32 8 right?

14:30:34 9 MR. HALVERSON: Objection, form.

14:30:36 10 THE WITNESS: I think that implementation is
 14:30:58 11 part of what serves the goal of maximizing Q factor.

14:31:03 12 BY MR. LIU:

14:31:30 13 Q And that implementation uses a symmetric
 14:31:34 14 inductor, right?

14:31:36 15 A And I didn't quite hear. I really
 14:31:39 16 apologize. If you could just repeat that.

14:31:41 17 Q And that implementation uses a symmetric --
 14:31:45 18 sorry. Strike that.

14:31:46 19 And that implementation uses a center-tapped
 14:31:51 20 symmetric inductor, right?

14:31:52 21 A In that sentence that's what it's talking
 14:31:55 22 about, that's right.

14:31:56 23 Q On this page 41, does it describe anywhere
 14:32:12 24 that Muh wants to place the capacitor as close to
 14:32:18 25 the coil of the inductor as possible?

14:32:27 1 A What I was interpreting here is that the
14:33:51 2 idea of maximizing the Q factor is stated. And when
14:33:59 3 I looked at the implementations elsewhere in Muh, in
14:34:03 4 the appendix, for instance, there's this notion of
14:34:07 5 putting the capacitor, you know, right at the --
14:34:19 6 right at the ends of the coil. I'm more like
14:34:23 7 reading -- I'm reading some of what we see on this
14:34:26 8 page sort of in light of the other parts of the
14:34:33 9 reference.

14:34:33 10 Q I believe you're referring to maybe page 58
14:34:41 11 or 57? Can we go to page 58 in Muh?

14:34:48 12 A Okay, I'm there.

14:34:50 13 Q It shows Figure B-3. Do you see that?

14:34:55 14 A Yes.

14:34:56 15 Q Does Figure B-3 show a center-tapped
14:35:06 16 inductor?

14:35:09 17 A No, I don't think so.

14:35:18 18 Q So it's a single-ended inductor, right?

14:35:27 19 A Or it's differential, but without a center
14:35:30 20 tap.

14:35:32 21 Q I think you said Muh wants the capacitor in
14:36:14 22 this position shown in Figure B-3 because it wants
14:36:23 23 -- let me just use your language. I think it's in
14:36:26 24 your declaration, paragraph 164. "Muh (and
14:36:45 25 Niknejad) deliberately position the capacitor of the

14:36:48 1 LC circuit in the area under the coil-conductor
14:36:53 2 segment. They do so because that orientation
14:36:57 3 improves the Q-factor of the LC circuit."

14:37:00 4 Do you see that?

14:37:00 5 A Yes.

14:37:01 6 Q So my question is how does this orientation
14:37:04 7 improve the quality factor of the LC circuit?

14:37:08 8 A It's something I explain in a little more
14:37:30 9 detail in paragraph 161.

14:37:49 10 Q Okay. I see it. Thank you. Next still
14:38:04 11 going back to 164, it says, "In contrast, the '582
14:38:10 12 patent accepts the lower Q factor in exchange for
14:38:16 13 significant benefits in reducing parasitics and
14:38:20 14 phase noise."

14:38:30 15 But here, you do confirm the '582 patent
14:38:40 16 aims to reduce parasitics and phase noise, right?

14:38:48 17 A I think that's right. It's got more of a
14:38:57 18 system-level approach to improving Q. And so for
14:39:05 19 instance, by not putting the capacitor right up with
14:39:11 20 overlap of the coil, but offsetting it, it's
14:39:18 21 measuring the parasitics of this LC resonant tank so
14:39:22 22 that, for instance, in a VCO application, the VCO
14:39:25 23 could be operated with improved phase noise.

14:39:28 24 Q Are you saying here that reducing parasitic
14:39:39 25 capacitance would actually decrease the Q factor of

14:39:43 1 the LC circuit?

14:39:46 2 A What -- I guess what I'm really getting at
14:39:50 3 here is that the offsetting of the capacitor and not
14:39:58 4 putting it right at the -- right at the ends of a
14:40:04 5 ring defining the inductor, but offsetting it, is a
14:40:10 6 choice that you only see really in the '582 combined
14:40:15 7 with, you know, the limitations about the capacitor
14:40:18 8 orientation. And overall, the '582 seems to be --
14:40:27 9 it's like managing the parasitics of that LC
14:40:29 10 structure so that even if it's giving up a little
14:40:33 11 bit of Q for the inductor, the Q of the entire
14:40:39 12 system, the glossiness of the entire system and its
14:40:42 13 parasitics can be better managed for a VCO
14:40:47 14 application, for instance.

14:40:49 15 Q So does offsetting the capacitor lower the Q
14:41:17 16 factor of the LC circuit or does it lower the Q
14:41:20 17 factor of the inductor or both?

14:41:28 18 A I think for the inductor, that was really
14:41:38 19 what I had in mind when I wrote this sentence
14:41:40 20 because if you think about those leads as they go
14:41:44 21 out, which, you know, the patent calls
14:41:48 22 extension-conductor segments, they link less flux
14:41:55 23 for a given length. Like you're spending more
14:42:01 24 length of conductor, but you're not linking as much
14:42:06 25 flux as you would if you used that conductor around

14:42:14 1 the periphery of a ring where the magnetic flux is
14:42:18 2 inside that. So you tend to -- that tends to
14:42:22 3 diminish Q a little bit. But overall -- and again
14:42:28 4 this is more the LC picture -- that that entire
14:42:32 5 structure better manages the parasitics of the LC
14:42:38 6 resonant circuit. And I think that's one of the
14:42:42 7 distinguishing features of the '582 patent.

14:42:46 8 Q Here in paragraph 164, you write -- so you
14:42:52 9 are saying the '582 patent accepts a lower quality
14:42:55 10 factor of the LC circuit in exchange for reducing
14:43:00 11 parasitics and phase noise, right?

14:43:04 12 A What I was really trying to convey in my
14:43:14 13 last answer is that in contrast, the '582 patent
14:43:17 14 accepts the lower Q factor of the inductor. You
14:43:21 15 know, it's like you're spending inductor length to
14:43:40 16 not link as much flux as you would had that
14:43:54 17 conductor been really used in the periphery of the
14:44:03 18 -- like a ring inductor.

14:44:10 19 Another way to put this is that if we just
14:44:14 20 consider the LC resonant circuit, it could have
14:44:21 21 higher Q if we don't offset the capacitor. And by
14:44:27 22 offsetting the capacitor, perhaps it diminishes Q a
14:44:31 23 little bit. But by the time you actually connect
14:44:35 24 this LC resonant circuit in a larger system, like a
14:44:48 25 VCO, it could actually benefit you in the long run

14:44:53 1 to do that offsetting, thus the orientation of the
14:44:56 2 capacitor as claimed.

14:44:59 3 Q So here in reducing the parasitics, you
14:45:16 4 would decrease the Q factor of the LC slightly, but
14:45:21 5 it is accepted in the '582 patent, right?

14:45:28 6 A You know, when I wrote that, I was really
14:45:43 7 thinking of decreasing the Q factor of the inductor
14:45:46 8 that is related to the Q factor of the LC circuit.
14:45:51 9 And so the point I'm making is that maybe have a
14:45:57 10 little bit of a non-intuitive offset between the L
14:46:00 11 and the C in the '582 patent, but then when you are
14:46:05 12 connecting that system through things like an
14:46:09 13 extension-conductor segment, you actually have a net
14:46:14 14 win because of reduced parasitics of that overall
14:46:19 15 structure.

14:46:22 16 Q So here would reducing the parasitics
14:46:29 17 decrease the quality factor of the inductor? I
14:46:35 18 think you said yes, but I just want to make sure.

14:46:38 19 A Gosh, it's a complicated answer. Okay. I'd
14:46:53 20 say reducing the parasitics -- to me there what I
14:47:04 21 was trying to get at is that the -- reducing the
14:47:08 22 parasitics in the connection to the capacitor can
14:47:14 23 have a benefit for the inductance to the -- phase
14:47:23 24 inductance with the capacitor.

14:47:25 25 The very fact that -- the very fact that you

14:47:29 1 offset the capacitor will tend to diminish somewhat
14:47:33 2 the Q of the inductive portion of the LC resonant
14:47:41 3 circuit because you're having these
14:47:44 4 extension-conductor segments that are not linking as
14:47:47 5 much flux for their length as they might otherwise
14:47:52 6 do if the capacitor were sort of brought back,
14:47:58 7 overlap the coil or be at the ends of the ring.

14:48:01 8 Q And all other things being equal, a lower
14:48:07 9 quality factor of the inductor would lead to a lower
14:48:10 10 quality factor of the LC circuit, right?

14:48:13 11 A Yeah, that's right, other things being
14:48:16 12 equal.

14:48:17 13 Q So I wonder, could reducing parasitics and
14:48:34 14 increasing the quality factor of the inductor be
14:48:40 15 accomplished at the same time?

14:48:46 16 A I think it would depend sort of what level
14:49:28 17 you looked at the problem. Like if you -- if you
14:49:33 18 looked at it as you really wanted to just build the
14:49:37 19 best LC tank, LC resonant circuit that you could and
14:49:43 20 you didn't really care as much about like a
14:49:49 21 surrounding system, you know, I think that your
14:49:54 22 answer would vary depending on how high a system
14:49:57 23 level approach you were taking.

14:49:59 24 Q Okay. Can you go up in your declaration to
14:50:07 25 paragraph 161 at the end?

14:50:13 1 A Okay, I'm there.

14:50:14 2 Q There's this figure. I think it's part of
14:50:20 3 Figure B-3 where you show the direction of a finger
14:50:26 4 capacitor. Do you see that?

14:50:28 5 A Yes.

14:50:28 6 Q So here if the finger capacitor were to be
14:50:34 7 rotated 90 degrees so that it has the same
14:50:37 8 orientation as disclosed in the patent, would that
14:50:44 9 decrease the Q factor of the LC circuit?

14:50:49 10 A I think you asked would it decrease?

14:51:01 11 Q Yes.

14:51:02 12 A So I guess the short answer I'd give you is
14:51:32 13 that it would depend. And I see other potential
14:51:41 14 problems if the fingers were to be made fewer in
14:51:46 15 number and longer. So it's not -- it ends up not
14:51:51 16 being an apples-to-apples comparison because of how
14:51:57 17 the realizable capacitance could change given a
14:52:02 18 change in orientation using the same area.

14:52:09 19 Q So you don't know one way or the other
14:52:13 20 whether rotating 90 degrees would actually like
14:52:19 21 increase or decrease the quality factor?

14:52:25 22 A There's some interrelated considerations
14:52:31 23 that I think make that answer not -- it would depend
14:52:40 24 on some things we'd need to pin down in your
14:52:44 25 question I think to really -- to really compare

14:52:55 1 orientations.

14:52:56 2 Q So fair to say that in the patent itself, I
14:53:12 3 mean because you're trying to offset the capacitor
14:53:14 4 and reduce parasitics and phase noise, so you're not
14:53:22 5 as concerned about the quality factor of the LC
14:53:26 6 circuit, right? You're willing to sacrifice to some
14:53:31 7 extent?

14:53:32 8 A The way I'd say it is you are concerned of
14:53:39 9 the quality factor of the LC circuit, but in a
14:53:41 10 system — at a system level where it is connected to
14:53:49 11 other things. So the phase noise concept, that's
14:53:52 12 really a VCO concept. That's an application
14:53:55 13 concept. And you know, what I'm kind of getting at
14:53:59 14 is what good would it do you to make a wonderful,
14:54:03 15 high Q LC oscillator if you couldn't connect to it
14:54:07 16 in a way that enabled the system as a whole to
14:54:15 17 function with improved phase noise because I think
14:54:19 18 that what the inventors are — you know, what they
14:54:24 19 invented was something where there's this
14:54:27 20 combination of offset where you're able to manage
14:54:30 21 parasitics in the capacitor. And there could be
14:54:33 22 some aspect where they kind of, you might say, took
14:54:36 23 a hit in terms of Q. But overall in that system, it
14:54:40 24 actually did good. And I think that's what they
14:54:43 25 were excited about and why they thought this was

14:54:48 1 patentable subject matter.

14:54:49 2 Q And parasitics here include parasitic
14:54:54 3 capacitance, right? I think we discussed that
14:54:58 4 earlier today.

14:55:00 5 A It could. But the type that I'm really
14:55:04 6 thinking most about when I'm thinking about
14:55:07 7 capacitor position is the parasitic inductance and
14:55:14 8 resistance. That's really what I'm thinking about
14:55:20 9 most as far as this position of the capacitor and
14:55:25 10 then adding the offset with respect to the inductor.

14:55:31 11 Q Can we go down to -- in your declaration to
14:55:41 12 paragraph 168?

14:55:45 13 A Okay, I'm there.

14:55:46 14 Q You said in the second line, "If a POSITA
14:55:53 15 were to employ vias in the connection between any
14:55:57 16 capacitor of Muh and the inductor of Muh, they would
14:56:03 17 be used to connect one end of the coil-conductor
14:56:08 18 segment to one of the connecting segment, and the
14:56:09 19 other end of the coil-conductor segment to the other
14:56:15 20 connecting segment."

14:56:20 21 Will you finish reading that paragraph?

14:56:23 22 A And I apologize. I think you said 168?

14:56:27 23 Q That's right. Just read 168. You don't
14:56:31 24 have to read it out loud.

14:56:53 25 A Okay.

14:56:55 1 Q You are saying that in Muh, the connection
14:57:10 2 between the capacitor and inductor can be done using
14:57:19 3 trench vias, right?

14:57:22 4 A Jing shows how to make a connection using
14:57:25 5 either sort of standard vias that are more like a
14:57:30 6 post or the more elongated trench-style.

14:57:42 7 Q Okay. I just want to kind of figure --
14:57:45 8 understand how you actually accomplish that. So
14:57:48 9 could you go back to the end of paragraph 161 where
14:57:53 10 you have that figure shown? I'm actually going to
14:57:59 11 share my screen real quick.

14:58:02 12 A Okay, I'm there.

14:58:12 13 Q Do you see the screen?

14:58:13 14 A Yes.

14:58:15 15 Q I'm taking a snippet of this figure. And I
14:58:23 16 want to understand how you would accomplish the
14:58:25 17 connection between the finger capacitor here and the
14:58:31 18 inductor. So if I draw a line here in green -- I'm
14:58:48 19 drawing a line in green in this figure. Would that
14:58:54 20 be a fair way that you could use a trench via to
14:59:03 21 connect the segment to the inductor?

14:59:11 22 MR. HALVERSON: Objection, form.

14:59:22 23 THE WITNESS: So a couple things occur to me
14:59:25 24 is if below that were sort of the back of the comb,
14:59:31 25 like the connecting segment, and then we were to go

14:59:35 1 down from that green line, that could be a way to
14:59:39 2 connect to the back of that comb there.

14:59:42 3 Another would be, you know, maybe the whole
14:59:46 4 comb part is really more not as wide. And yeah, you
14:59:55 5 could have vias that just go down, so something
15:00:01 6 that's more like a square and then coming off from
15:00:03 7 that square is something like the back of the comb
15:00:11 8 that then goes off to the little electrode segments,
15:00:16 9 the greater number of shorter electrode segments.

15:00:26 10 So that would be like the way Jing does it
15:00:29 11 is my point. That's a way that you can manage the
15:00:32 12 parasitics of the capacitor in that case because you
15:00:38 13 have -- there's more freedom to make the back of the
15:00:42 14 comb wider, for instance, and have less parasitic
15:00:49 15 resistance and inductance in the fingers themselves.

15:00:58 16 BY MR. LIU:

15:00:59 17 Q So in the illustration you're showing here,
15:01:04 18 if you are connecting the finger capacitor to the
15:01:07 19 inductor using the trench via or the standard size
15:01:14 20 via taught by Jing, so you would have, you know, on
15:01:20 21 one side of the inductor, a via that is closer to
15:01:27 22 the coil than the other side, right?

15:01:31 23 A I'm not sure I understood that.

15:01:41 24 Q For example, I'm again adding a second green
15:01:47 25 line into this illustration of yours. So I guess

15:01:56 1 when you are connecting the finger capacitor to the
15:02:00 2 inductor, the connecting point on one side would be
15:02:03 3 closer to the coil than the other side?

15:02:10 4 A I see how you've staggered those. So that's
15:02:15 5 one way to do it. And then another way could be --
15:02:19 6 I was trying to indicate this -- where you could go
15:02:22 7 down without being staggered to -- you could think
15:02:34 8 of it like a square of metal from which extend the
15:02:41 9 backs of the comb. So you could go to some
15:02:44 10 intermediate structure and then over. So the vias
15:02:48 11 themselves wouldn't necessarily need to be staggered
15:02:51 12 depending on what they were connecting to down
15:02:54 13 below.

15:02:54 14 Q If we follow the teachings of Jing, would we
15:03:01 15 lead to a symmetrical structure in terms of how the
15:03:05 16 capacitor connects to the inductor?

15:03:10 17 A It could be symmetric and like not staggered
15:03:17 18 in terms of like the vias. But when you get into
15:03:22 19 the capacitor itself, there would be an asymmetry
15:03:31 20 because one side would have to be, you know, further
15:03:37 21 out or further in compared to the other. One back
15:03:44 22 of the comb would sort of be further outward from
15:03:48 23 the -- compared to the center of the coil than the
15:03:51 24 other. So that the bilateral symmetry -- that would
15:04:00 25 disrupt bilateral symmetry as far as the backs of

15:04:05 1 the comb.

15:04:09 2 Q Okay. If we can go down in your declaration
15:04:29 3 to paragraph 169.

15:04:38 4 A Okay, I'm there.

15:04:39 5 Q Near the bottom of that page, that
15:04:53 6 paragraph, you said, "The only reference I have
15:04:57 7 reviewed in this proceeding that includes an
15:05:02 8 oriented in the claimed manner in this proceeding is
15:05:08 9 the '582 patent itself."

15:05:12 10 So my question is so you were part of the
15:05:21 11 ITC proceeding, right?

15:05:23 12 A Yes.

15:05:23 13 Q And there was a prior art article called the
15:05:26 14 Qualcomm RBR 1000 against this patent. Do you
15:05:31 15 recall that?

15:05:32 16 MR. HALVERSON: Objection, form, beyond the
15:05:35 17 scope.

15:05:36 18 THE WITNESS: I do remember an RBR 1000,
15:05:39 19 yes.

15:05:39 20 BY MR. LIU:

15:05:41 21 Q Are you aware that the Administrative Law
15:05:47 22 Judge, the ALJ, in that proceeding felt that the
15:05:51 23 Qualcomm RBR 1000 did invalidate claim 1 of this
15:05:55 24 patent?

15:05:58 25 A I think -- yeah, I think I heard that about

15:06:03 1 the ID. Would you mind -- the RBR 1000 is the one
15:06:15 2 that I had what I call the sister coil?

15:06:18 3 Q That's right. So here by this sentence you
15:06:22 4 just mean that the only reference I have reviewed in
15:06:27 5 this proceeding, like but you are aware of other
15:06:30 6 references in other proceedings that includes the
15:06:35 7 finger capacitor oriented in a claimed manner,
15:06:41 8 right?

15:06:43 9 A Not in my view because I think the RBR 1000,
15:06:48 10 I think -- when we were discussing that, I was
15:06:52 11 focused on an area away from the coil and the sister
15:07:11 12 coil and I was looking at that location.

15:07:24 13 Q Let's move down in your declaration to
15:07:26 14 paragraph 180.

15:07:35 15 A Okay, I'm there.

15:07:36 16 Q In this paragraph, a few lines down you talk
15:07:49 17 about design rules are mandated by the foundry. Do
15:07:54 18 you see that?

15:07:54 19 A Yes.

15:07:55 20 Q I guess so my question is does Muh or
15:08:07 21 Niknejad talk about design rules?

15:08:12 22 A I'd say that Niknejad, as far as I'm aware,
15:08:54 23 would have only talked about design rules in
15:08:57 24 generalities. They do come up. So it's not talking
15:09:02 25 about a specific set of design rules, if that

15:09:07 1 answers your question.

15:09:09 2 Q Does Muh talk about design rules?

15:09:14 3 A I think we'd have to look. Muh, you know,

15:09:19 4 in a way those design rules are in the background

15:09:24 5 sometimes because it's sometimes depicting actual

15:09:32 6 layout, you know. And you could be right that it's

15:09:36 7 not sort of discussing in the text what those design

15:09:41 8 rules are, but we could look. I can't -- I could

15:09:45 9 look.

15:10:00 10 Q Can we go to Muh, which is Exhibit 1006.

15:10:16 11 Let's go to page 57. That's the page before Figure

15:10:26 12 B-3.

15:10:26 13 A Okay, I'm there.

15:10:28 14 Q Second sentence of that paragraph there it

15:10:35 15 says, "In the test chip, the capacitor is

15:10:37 16 implemented as an interdigitated finger capacitor."

15:10:41 17 Do you see that?

15:10:41 18 A Yes.

15:10:42 19 Q So according to this sentence here, so Muh

15:10:50 20 did successfully make a test chip using a finger

15:10:53 21 capacitor, right?

15:10:57 22 A There's one word I didn't hear in your

15:11:01 23 question. And I apologize about that. It was maybe

15:11:04 24 the word "make." If I could just hear the question

15:11:07 25 again.

15:11:07 1 Q So Muh did successfully make a test chip
15:11:11 2 using a finger capacitor, right?

15:11:13 3 A I disagree with that. This appendix is one
15:11:19 4 where Mr. Muh gets a test chip from a collaborator.
15:11:28 5 And this appendix is sort of like a test to see if
15:11:36 6 they can make a model of that test chip to match the
15:11:39 7 un-embedded parameters of this LC resonant circuit
15:11:47 8 on the test chip and compare that with this HFSS
15:11:50 9 model.

15:11:54 10 Q Okay. So whether it's the collaborator or
15:11:57 11 Mr. Muh himself, so there is a test chip on which
15:12:03 12 the capacitor has been implemented as an
15:12:08 13 interdigitated finger capacitor, right?

15:12:12 14 A That's what it's saying, yeah. It was
15:12:15 15 implemented as an interdigitated finger capacitor on
15:12:19 16 that test chip.

15:12:20 17 Q So presumably whatever design rules there
15:12:37 18 were, that test chip would have considered the
15:12:40 19 design rules, right?

15:12:45 20 A As a general proposition, I'd agree with
15:12:49 21 that. It's -- it's almost like you can't violate
15:12:54 22 the design rules and even have it built. It's like
15:12:57 23 there's something called design rule check and
15:13:01 24 errors are flagged and you have to fix them to have
15:13:05 25 your masks sent for production.

15:13:07 1 Q If you don't mind, can we go back to the
15:13:29 2 '582 patent itself? I think that's Exhibit 1001.
15:13:37 3 A Okay, I'm there.
15:13:38 4 Q Let's go to Figure 12 that's on page 14.
15:13:51 5 A Okay, I'm there.
15:13:53 6 Q Do you see a capacitor component 150 in the
15:14:01 7 middle of Figure 12?
15:14:06 8 A Yes, I see that.
15:14:12 9 Q That's a finger capacitor, right?
15:14:22 10 A I'd say so.
15:14:36 11 Q And I think we talked about this before. So
15:14:42 12 this capacitor component 150, it includes connecting
15:14:49 13 segment 151 and 152, right?
15:14:52 14 A Yeah, that's what I recall us identifying
15:14:57 15 earlier.
15:14:59 16 Q And it also includes electrode segments 155,
15:15:03 17 156, 157 and 158, right?
15:15:17 18 A I think that's right.
15:15:19 19 Q Now, do you see capacitor component 150
15:15:24 20 prime at the bottom of Figure 12?
15:15:29 21 A Yes.
15:15:56 22 Q Does 150 prime also include a finger
15:16:00 23 capacitor?
15:16:03 24 A It's a little unusual because it's got this
15:16:43 25 159. It's drafted a little differently. It's got

15:16:48 1 this thing that I think it's called the
15:16:50 2 semiconductor segment 159, 154. And the reason I
15:16:59 3 mention this is that this 150 prime, as well as
15:17:03 4 there's a 150 double prime, are described as being
15:17:09 5 capacitors in various forms. But given the
15:17:18 6 similarity in how it's drawn, I think -- I think
15:17:22 7 what you're saying is right, that it can -- it can
15:17:27 8 be a finger capacitor but I think it's maybe drafted
15:17:32 9 to try to show different possibilities.

15:17:38 10 Q So the top layer of the 150 prime, not
15:17:46 11 including the segments 154 and 159, that part I mean
15:17:52 12 looks awfully close to 150. So that is a finger
15:17:56 13 capacitor, right?

15:17:57 14 MR. HALVERSON: Objection, form.

15:17:58 15 THE WITNESS: It really is drawn the same
15:18:32 16 way, that 150 prime, if we ignore 159 and 154. In
15:18:39 17 fact, even the labels are the same numbers. So I
15:18:48 18 think I agree with that. It's like it could be --
15:18:53 19 it's maybe said to be in the text like it could be
15:18:56 20 different embodiments, but this type of embodiment
15:18:59 21 would be something like a finger capacitor.

15:19:03 22 BY MR. LIU:

15:19:21 23 Q You mentioned the semiconductor segments 154
15:19:26 24 and 159. So do you think the semiconductor segments
15:19:33 25 154 and 159 here would be connected to the electrode

15:19:39 1 segments say 155 and 157 -- sorry. Let me simplify
15:19:49 2 that question.

15:19:51 3 For example, would the semiconductor segment
15:19:54 4 154 be connected to the electrode segment 155 and
15:19:59 5 157 that's sort of on the right side of that
15:20:04 6 capacitor?

15:20:06 7 A I've got to think that when I look at the
15:20:28 8 specification at column 12, around line 16, and it
15:20:34 9 says, "By using the MOS capacitor as an example and
15:20:39 10 referring to Figure 12, the capacitor component 150
15:20:43 11 prime further includes at least one semiconductor
15:20:46 12 segment 154, in addition to the members shown in the
15:20:51 13 foregoing embodiments."

15:20:53 14 And it says, "The semiconductor segment 154
15:20:56 15 is located below the first electrode segment at 155
15:21:01 16 and the second electrode segment 157 which are
15:21:07 17 staggered at an interval of a dielectric layer."
15:21:14 18 I'm going to stop reading that because it goes on.

15:21:17 19 But so when I started reading those
15:21:23 20 sentences, you notice how it said by using the MOS
15:21:27 21 capacitor, as an example. When you see MOS, that's
15:21:31 22 going to mean vertically. It's always a vertical
15:21:35 23 concept, metal-oxide-semiconductor. So 154 is
15:21:42 24 called semiconductor and then those electrode
15:21:47 25 segments are metal. And so, you know, one thing

15:21:51 1 this could be implying is that there's additional
15:21:54 2 capacitance there because this is forming a MOS
15:21:58 3 capacitor and those two aren't connected, you know,
15:22:02 4 that there's rather a capacitance between them with
15:22:07 5 an electric field in an oxide.

15:22:13 6 Q Are you saying segment 154 may not be like
15:22:21 7 connected to the layer on top because it's forming a
15:22:26 8 capacitance between the metal layer and the
15:22:29 9 semiconductor segment?

15:22:33 10 A Yeah, that's more or less right. Like if
15:22:36 11 you think about 154, let's say -- let's say it did
15:22:39 12 connect to things that are above it. Well, that
15:22:42 13 could be a problem because then maybe it's just
15:22:44 14 shorting out. 153 and 151 is an example. And you
15:22:52 15 know, that's no good. Maybe what it's doing instead
15:22:55 16 is it has a MOS capacitor structure where it's not
15:23:02 17 connecting to at least 153 or at least 151 and maybe
15:23:11 18 both.

15:23:13 19 Q I thought you said earlier that in a MOS
15:23:18 20 capacitor, the capacitance is not formed between
15:23:24 21 like the metal and the semiconductor, but it's
15:23:28 22 rather formed between a gate electrode and an Nwell,
15:23:39 23 for instance, in the silicon, right?

15:23:43 24 A Just taking that last part, translating into
15:23:49 25 what we see here, let's say the 153, let's say

15:23:52 1 that's effectively like a gate over an oxide where
15:23:59 2 it is over 154. So 154 would be akin to the well
15:24:04 3 that I mentioned before and something in the bulk
15:24:08 4 silicon. So that's adding additional capacitance
15:24:14 5 through the bulk to the other -- the 151. So it's a
15:24:19 6 way of increasing capacitance by taking advantage of
15:24:25 7 MOS capacitors structures at the bulk silicon
15:24:31 8 surface.

15:25:13 9 MR. LIU: Can we take a short break?

15:25:17 10 VIDEOGRAPHER: Going off the record. The
15:25:20 11 time is 3:25 p.m.

15:25:22 12 (Short recess.)

15:36:28 13 VIDEOGRAPHER: Going back on the record.

15:37:26 14 The time is 3:37 p.m. This marks the beginning of
15:37:29 15 media Number 5. Please continue.

15:37:33 16 MR. LIU: Dr. Phinney, thank you for your
15:37:34 17 time. I think I'm actually done with my questions.
15:37:37 18 I pass the witness.

15:37:38 19 MR. HALVERSON: Apologies. Two minutes. Be
15:37:43 20 right back.

15:37:44 21 VIDEOGRAPHER: Go off the record? Going off
15:37:47 22 the record. The time is 3:37 p.m.

15:37:50 23 (Short recess.)

15:40:45 24 VIDEOGRAPHER: Going back on the record.

15:41:09 25 The time is 3:41 p.m. This marks the beginning of

15:41:13 1 media Number 6. Please continue.
15:41:15 2 MR. HALVERSON: Nothing else from me. Thank
15:41:18 3 you everybody for your time today.
15:41:20 4 MR. LIU: Thank you.
15:41:21 5 VIDEOGRAPHER: This marks the end of media 6
15:41:23 6 of 6. Going off the record. The time is
15:41:25 7 3:41 p.m.
8 (Phinney Exhibit 2 marked for
9 identification.)

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12 (Time Noted: 3:41 p.m.)

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1 C E R T I F I C A T E

2

3 I, Sandra L. Rocca, CSR, RMR, RDR, CRR, a
4 Certified Court Reporter within and for the States
5 of Illinois, Florida, Washington and Georgia, do
6 hereby certify:

7 That JOSHUA PHINNEY, Ph.D., the witness
8 whose deposition is hereinbefore set forth, was duly
9 sworn by me and that such deposition is a true
10 record of the testimony given by such witness.

11 I further certify that I am not related to
12 any of the parties to this action by blood or
13 marriage; and that I am in no way interested in the
14 outcome of this matter.

15 IN WITNESS WHEREOF, I have hereunto set my
16 hand this 20th of April, 2024.

17

18

19



20

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21

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