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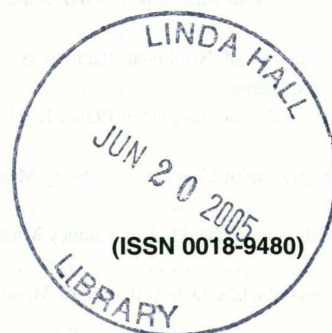


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Design of Multiple-Metal Stacked Inductors Incorporating an Extended Physical Model

Olive H. Murphy, *Student Member, IEEE*, Kevin G. McCarthy, *Member, IEEE*, Christophe J. P. Delabie, Aidan C. Murphy, *Member, IEEE*, and Patrick J. Murphy, *Member, IEEE*

Abstract—Modern analog circuits are heavily dependent on inductor performance, where the poor inductor quality factor (Q) of silicon processes leads to degradation in circuit efficacy, especially at RF and microwave frequencies. Several techniques have been proposed to enhance the Q of integrated on-chip inductors, but the most effective method of Q improvement is to lower the series resistance by increasing the inductor metal thickness. This paper presents the most cost-effective method of achieving a thick metal by using a standard 0.18- μm multilayer BiCMOS process. An expanded physically based model for multiple-metal stacked inductors is presented, which expands on previous research to show the effects and limitations of stacking two, three, and four metal layers in a five-metal-layer process. The excellent accuracy of this geometrical model is illustrated with respect to a range of inductor designs showing that an improvement in Q of more than 50% may be achieved. Due to the increased parasitics in multilayer structures, the Q improvement is very frequency dependent, which is clearly predicted with the expanded model. The predictive capability of the model is further used to provide detailed insight into the effectiveness of a patterned ground shield for different substrate characteristics. This predictive ability will contribute greatly to first time right inductor designs and eliminate the expensive and time-consuming fabrication iterations required to fine tune other inductor models.

Index Terms—Integrated stacked inductor model, patterned ground shield (PGS), Q improvement, Q prediction.

I. INTRODUCTION

THE POOR quality factor (Q) of integrated silicon inductors has led to circuit inefficiencies. This is especially evident in wireless local area network (WLAN) applications at 5.25 GHz where poor Q values can result in increased noise figure, power consumption, and linearity deterioration. Excellent Q values can be achieved using three-dimensional (3-D) fabricated inductors [1] and other processes such as liquid crystal polymer (LCP) [2] and low temperature co-fired ceramic (LTCC) [3], leading to excellent overall circuit performance [4], [5]. However, to achieve complete silicon integration, there is much attention paid to on-chip Q improvement techniques, especially inexpensive noninvasive process-independent approaches, which do not require complex process adaptation. Driving inductors differentially [6] using a patterned ground

shield (PGS) [7], [8] and using thick metal [9] or stacking inductors [10] are all methods of noninvasive process-independent techniques. The possibility of combining all of these methods has been investigated by the authors [11] and it has been shown that simultaneously combining these techniques does not necessarily lead to an improvement in Q . A thicker inductor, which reduces the series resistance, will result in a significant Q improvement as opposed to the more subtle improvements achieved by driving an inductor differentially or by using a PGS. These issues are discussed in detail in Section II.

The post-fabrication cost of adding thick copper to silicon processes is beginning to outweigh the advantages of increased circuit performance resulting from improvement of the Q of integrated inductors. Stacking two, three, and four metal layers, as presented in this paper, increases thickness while reducing resistance, all without the added cost of post-fabrication metal addition. Furthermore, modern fabrication costs are putting pressure on designers to produce ready-to-market designs in fewer iterations. This reduces the opportunity to fine-tune s -parameter-based [3], [12] or empirical [13] models to specific processes and increases the need for predictive physically based models, as discussed here.

Whereas electromagnetic simulators can produce accurate results, depending on the inductor geometry, they still have considerable scope for improvement, notwithstanding the lengthy simulation times and issues with integrated-circuit (IC) simulators. Therefore, there is a need for accurate models for custom inductors, which designers can include in their circuit designs. This study uses the physical model developed in [11] as a basis, but extends the methodology to a more detailed consideration of multiple-metal stacked inductors. It uses a simple π model without the added complexity of multiple transformer loops [12] or T-models [3] to model frequency dependence. The existing physically based model has been further developed to incorporate skin, proximity, and fringing effects. The lateral substrate resistance is also included in the model, as outlined in Section III. This model is subsequently reduced to a simple model for Q calculation and prediction. While previous research [11] was related to differential inductors, this paper concentrates on single-ended topologies, as these devices are the most prevalent in circuit design.

As mentioned earlier, PGSs can cause a subtle improvement in Q by virtue of eliminating the substrate resistance. This improvement is governed by the conductivity of the bulk substrate, which may render the PGS useless [11]. It is necessary to ascertain this prior to fabrication. A method of achieving this will be presented in Section IV where the new stacked metal model is

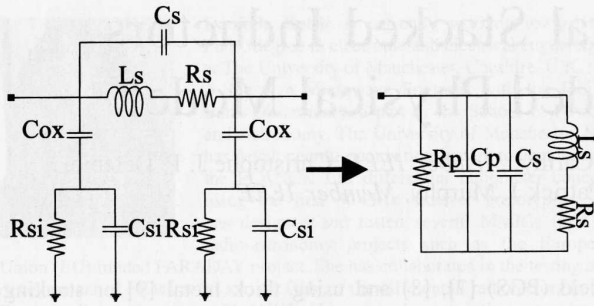
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Fig. 1. Simple π model for an integrated inductor.

used to generate predictive graphs, which show the viability of PGSS. These graphs also show the impact of process and substrate characteristics on Q .

Section V presents the test patterns characterized, while Section VI illustrates the accurate simulations achieved with the new models, which match the measurements very well across all frequency bands.

II. Q IMPROVEMENT TECHNIQUES

Fig. 1 shows the simple π model for an integrated inductor [14] from which the Q may be derived using (1) as follows:

$$Q = \frac{\omega L_S}{R_S} \cdot \frac{R_p}{R_p + \left[\left(\frac{\omega L_S}{R_S} \right)^2 + 1 \right] R_S} \cdot \underbrace{\left[1 - \frac{R_S^2}{L_S} (C_S + C_p) - \omega^2 L_S (C_S + C_p) \right]}_{\text{Self Resonant Factor}} \quad (1)$$

where

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{Si}} + \frac{R_{Si}(C_{ox} + C_{Si})^2}{C_{ox}^2} \quad (2)$$

$$C_p = C_{ox} \cdot \frac{1 + \omega^2 (C_{ox} + C_{Si}) C_{Si} R_{Si}^2}{1 + \omega^2 (C_{ox} + C_{Si})^2 R_{Si}^2} \quad (3)$$

There are many ways of improving the Q of integrated inductors, but few do so inexpensively using standard layout techniques and rules [6]–[10]. Three such approaches are presented as follows.

- As may be seen from (1), a reduction in series resistance R_s leads to an increase in Q . As area constraints mitigate the use of wider tracks, thicker tracks may be used [9] or the multilayer capability of the process may be utilized by joining metal layers using multiple vias to create a thicker metal track [10] and, hence, a stacked metal inductor.
- The *substrate loss factor* approaches unity as R_p approaches infinity. R_p approaches infinity as R_{Si} approaches zero or infinity, as may be seen in (2), which can be achieved by making the Si substrate a short or an open. A PGS can act as a short [7], [8]. Slotted patterning, which is orthogonal to the spiral, reduces the effect of negative mutual coupling (Lenz's Law [15]). The slots act as an open circuit to the loop current, but must be sufficiently

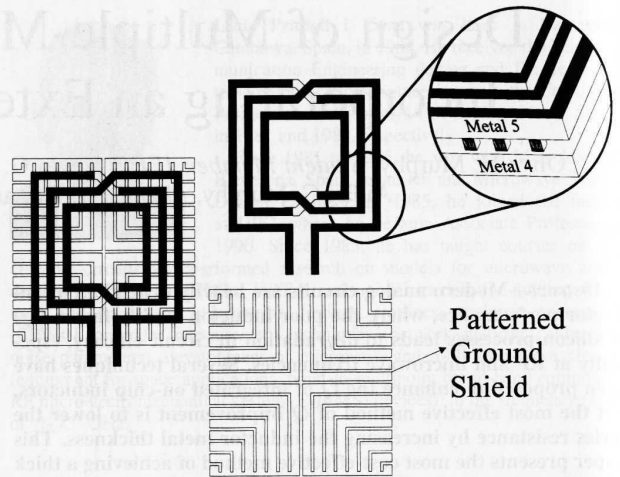


Fig. 2. Symmetric differentially driven stacked inductor with PGS.

narrow to prevent leakage of the vertical electric field. To make the substrate an open, an insulating substrate [16] may be used or it may be removed completely [17], but these are costly adaptations to a standard process.

- When a symmetric inductor is driven differentially, voltages on adjacent conductors are in antiphase, but currents flow in the same direction on each side. This increases the overall magnetic field [6] when compared to two asymmetric inductors. The substrate parasitics, C_p and R_p , as associated with each port, are thus combined to give a higher impedance at a given frequency than for single-ended termination, thus improving Q .

In terms of the three methods of Q improvement just mentioned and from examination of (1), it is easily seen that the most significant Q improvement is brought about by reducing R_s for a given L_s , as indicated in the first approach above. The impact of a thicker metal on inductor Q was demonstrated when a differential inductor using single and double metal layers was placed over a PGS [11], as indicated in Fig. 2. As seen in Fig. 3, a 40% improvement in Q is seen when Metal4 is stacked together with Metal5, as opposed to just Metal5 alone. The impact of driving the substrate loss factor to unity is slight as the value of the substrate loss factor prior to adding the PGS is already close to unity. The Q for the differential inductor, using either Metal5 or Metal5 + Metal4, does not improve when a PGS is placed underneath the inductor, as seen in Fig. 3 because, as mentioned, the substrate loss factor was close to unity to begin with [11].

III. MULTIPLE METAL-LAYER MODEL

When stacking metal layers to obtain a thicker conductor, the complexity of the new structure must be fully understood to achieve optimum Q . Two, three, and four metal layers are stacked to form multiple-metal stacked inductors, as seen in Fig. 4. Fundamentally, a parallel array of inductances and resistances is created, the latter being desired to improve Q , but not at the expense of a lower inductance, as would be created by the former. The resistance and inductance of the vias must also be taken into consideration. The approach taken in the new model is to break the inductor into segments, as seen in Fig. 5.

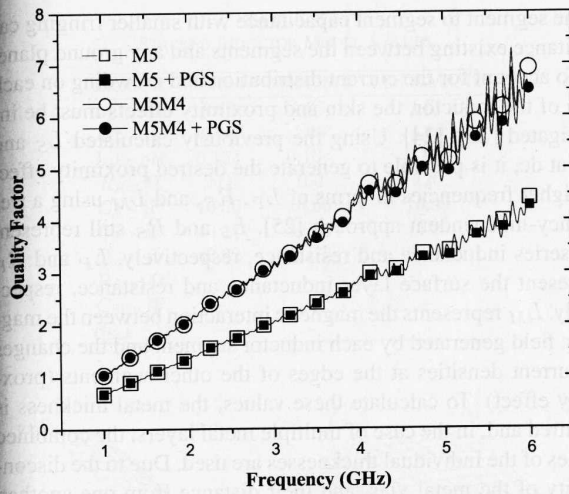


Fig. 3. Improvement in the Q of metal5 and metal5 + metal4 differential inductor.

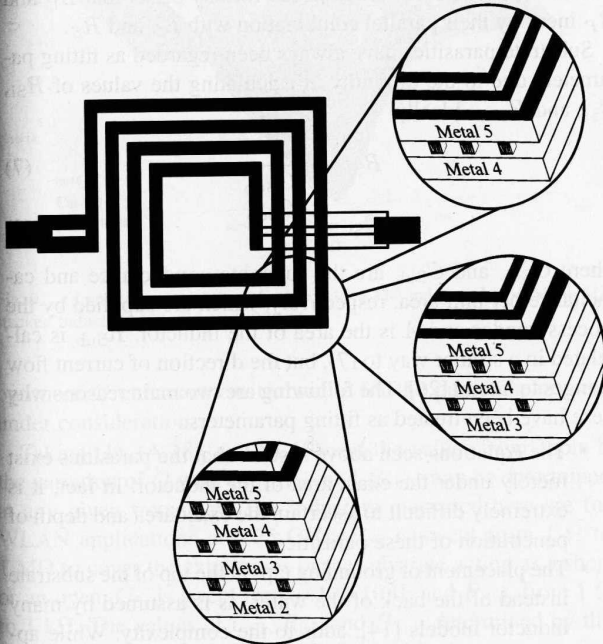


Fig. 4. Multiple-metal stacked inductor.

Each element of the model is based on the physical attributes of the inductor and process stack; therefore, each element is calculated from first principles.

The series inductance L_S is calculated using the data filled monomial expression [18]. Special care must be taken as the exact inner and outer diameters must be used; otherwise significant errors can be introduced. In this case, due to the inductor starting and ending midsegment, a weighted average of the diameters is used, where the weighting is determined by the fraction of a turn and the diameter that the fraction encompasses, as may be seen in Fig. 6, as follows:

$$D_{in} = x_1(d_{in1}) + x_2(d_{in2}) + x_3(d_{in3}) \quad (4)$$

$$D_{out} = x_1(d_{out1}) + x_2(d_{out2}) + x_3(d_{out3}) \quad (5)$$

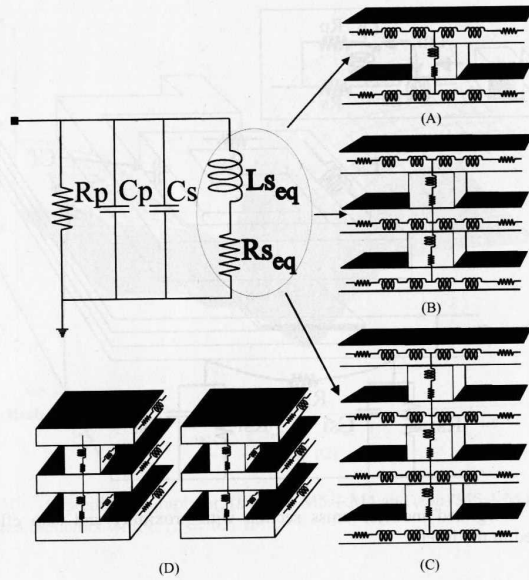


Fig. 5. Expanded π model showing each via segment for: (a) two metal layers, (b) three metal layers, (c) four metal layers, and (d) cross section of stacked metal traces.

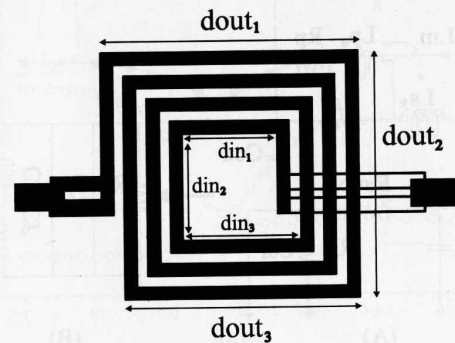


Fig. 6. Different inner and outer diameters.

where

$$x_1 + x_2 + x_3 = 1 \text{ turn} \quad (6)$$

and x_n is the fraction of a turn for which $d_{in_n}(d_{out_n})$ is valid. The inductor shown in Fig. 6 is referred to as a 3.5-turn inductor. A closer analysis shows that while this inductor is perfectly symmetrical about a line drawn through its start and end points, the number of turns is, in fact, 3.62 and not 3.5. This is because the first and last segments must be taken as a ratio of their length to the overall length of that side of the turn. For multiple metal inductors, the mutual inductance between each metal must also be calculated [19]. This is calculated for metals vertically above each other and also for neighboring metals, which are not part of the primary inductor. Its presence is critical in achieving proper frequency dependency at higher frequencies.

In a single metal track where the metal thickness is much less than the skin depth, the series resistance R_S does not have to account for the exponential decay of current so skin effect is not of concern. The resistance correction factor for all the corners in the inductor are also accounted for [20].

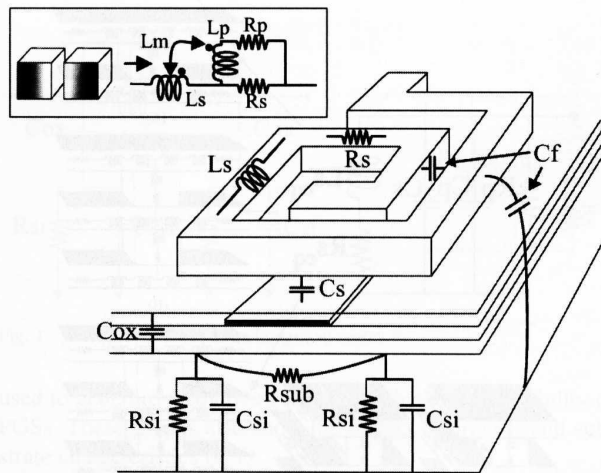


Fig. 7. Integrated inductor cross section with proximity and skin effect illustrated in the inset.

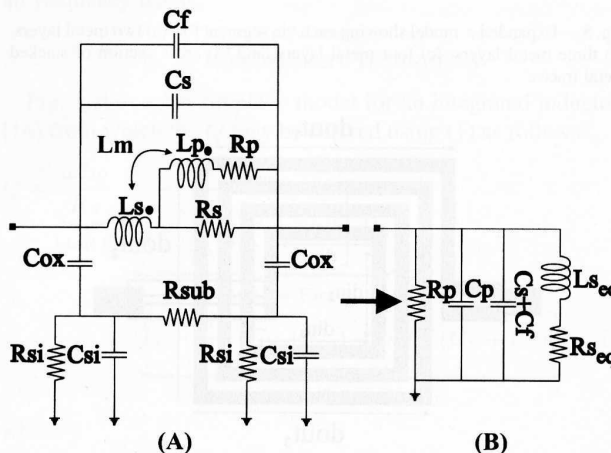


Fig. 8. Expanded physical model for stacked inductors.

These inductance and resistance values for each of the via segments are added using a series of $\Delta - Y$ transformations to give L_S and R_S .

As previously mentioned, there is no skin effect for a single metal layer, but it must be accounted for when stacked metals are used. Therefore, the simple π model needs adjustment to account for the skin effect along with the proximity and fringing effects of the metal. C_F , L_P , L_M , R_P , and R_{Sub} are added to the π model of Fig. 1. The physical representation of these may also be seen in Fig. 7, while the equivalent circuit is shown in Fig. 8.

C_F accounts for the substantial fringe capacitance or electric-field coupling present in integrated inductors. In previous publications [21], this parasitic has been lumped together with C_S , the underpass to inductor track capacitance. However, C_F is harder to quantify than C_S and needs to be analyzed separately. Here, it is calculated using a parallel lines over a ground-plane formulation [22]. Taking account of the previously calculated C_{ox} and the number of parallel coupling components, a good approximation for C_F is deduced. The largest contributor to C_F

is the segment to segment capacitance with smaller fringing capacitance existing between the segments and any ground plane.

To account for the current distribution and crowding on each turn of the inductor, the skin and proximity effects must be investigated [23], [24]. Using the previously calculated L_S and R_S at dc, it is possible to generate the desired proximity effect at higher frequencies in terms of L_P , R_P , and L_M using a frequency-independent approach [25]. L_S and R_S still represent the series inductance and resistance, respectively. L_P and R_P represent the surface layer inductance and resistance, respectively. L_M represents the magnetic interaction between the magnetic field generated by each inductor segment and the changes in current densities at the edges of the other segments (proximity effect). To calculate these values, the metal thickness is required and, in the case of multiple metal layers, the combined values of the individual thicknesses are used. Due to the discontinuity of the metal vias, and their distance from one another, their presence is not included in the proximity effect calculations. To maintain the overall value for the series inductance and resistance, L_S and R_S are adjusted for any offset that L_P and R_P incur by their parallel combination with L_S and R_S .

Substrate parasitics have always been regarded as fitting parameters due to the difficulty in calculating the values of R_{Si} , C_{Si} , and R_{Sub} . Ideally

$$R_{Si} = \frac{2}{AG_{Sub}} \quad (7)$$

$$C_{Si} = \frac{AC_{Sub}}{2} \quad (8)$$

where G_{Sub} and C_{Sub} are the substrate conductance and capacitance per unit area, respectively, which are supplied by the process vendor and A is the area of the inductor. R_{Sub} is calculated in a similar way to (7), but the direction of current flow changes to lateral [26]. The following are two main reasons why these have been treated as fitting parameters.

- The equations seen above assume that the parasitics exist merely under the exact area of the inductor. In fact, it is extremely difficult to ascertain the exact area and depth of penetration of these parasitics.
- The placement of grounding taps at the top of the substrate instead of the back of the wafer, as is assumed by many inductor models [14], adds to the complexity. While approximations may be made, better results are achieved by treating these quantities as fitting parameters within certain constraints.

Table I shows the calculated values for each element of the enhanced physically based stacked inductor model.

IV. ANALYSIS OF Q ENHANCEMENT USING THE EXTENDED PHYSICAL MODEL

Using a sequence of circuit transformations, as presented in the Appendix, the elements of Fig. 8(a) can be reduced to the elements of Fig. 8(b) at any given frequency. As the reduced element model is the same as that of Fig. 1, (1) may be used to calculate Q using the new formulas for R_P (A.18) and C_P (A.19). Consequently, it is possible to predict Q prior to fabrication and to identify the impact of each parameter on Q , especially the fitting parameters. This approach then identifies the

TABLE I
STACKED INDUCTOR MODEL VALUES

Element	M5M4	M5M4M3	M5M4M3M2
L_S - nH	1.69	1.65	1.61
R_S - Ω	6.98	4.99	4.16
L_P - nH	0.154	0.164	0.169
R_P - Ω	244	160	126
C_S - fF	16.50	16.60	16.99
C_P - fF	40.17	42.62	44.25
C_{ox} - fF	43.32	61.78	99.66
R_{Si} - Ω	-	-	-
C_{Si} - fF	-	-	-
R_{Sub} - Ω	-	-	-

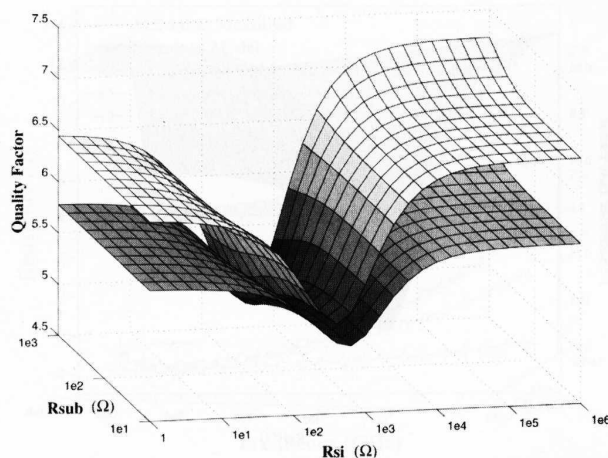


Fig. 10. Q prediction graph for: (bottom) M5 + M4 and (top) M5 + M4 + M3 stacked inductors with $C_{ox} = 0.5$ fF.

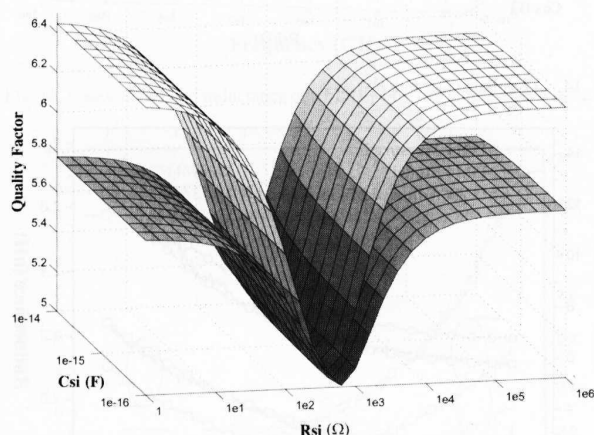


Fig. 9. Q prediction graph for: (bottom) M5 + M4 and (top) M5 + M4 + M3 stacked inductors with $R_{Sub} = 200 \Omega$.

optimum Q enhancement technique for the particular process under consideration.

Taking (1), (A.18), and (A.19) and the values from Table I, the variation of Q with C_{Si} , R_{Si} , and R_{Sub} may be determined at any given frequency. The inductors measured here are for WLAN applications at 5.25 GHz. R_{Si} is swept from 1Ω to $1 \text{ M}\Omega$ to cover the extremities of the substrate acting as a short or an open. C_{Si} is swept from 0.1 to 10 fF and R_{Sub} from 1Ω to $1 \text{ k}\Omega$. The values of C_{Si} , R_{Si} , and R_{Sub} determined by the approximate formulas (7) and (8) fall within these ranges, i.e., $R_{Si} = 27 \text{ k}\Omega$, $C_{Si} = 0.5$ fF, and $R_{Sub} = 200 \Omega$.

The minimum Q occurs when R_{Si} is $\sim 550 \Omega$, as may be seen from the hollows in both Figs. 9 and 10. The maximum Q occurs when R_{Si} approaches either zero or infinity. Any point on the left-hand-side plateau may be considered zero, while any point on the right-hand-side plateau may be considered infinity.

From Section II, it was seen that placing a PGS under an inductor will drive the value of R_{Si} toward 0Ω . From both Figs. 9 and 10, it is seen that a PGS will be effective in improving Q if the value of R_{Si} before placing the PGS lies at a point in the hollow lower than the Q when R_{Si} approaches zero. In this case, the PGS will drive the Q value out of the hollow and left along the graph to reside at a lower value of R_{Si} and subsequently a larger value of Q . If the value of R_{Si} lies on the right-hand-side plateau prior to placing the PGS under the inductor, no improvement in Q will be achieved, and it may even show a decrease.

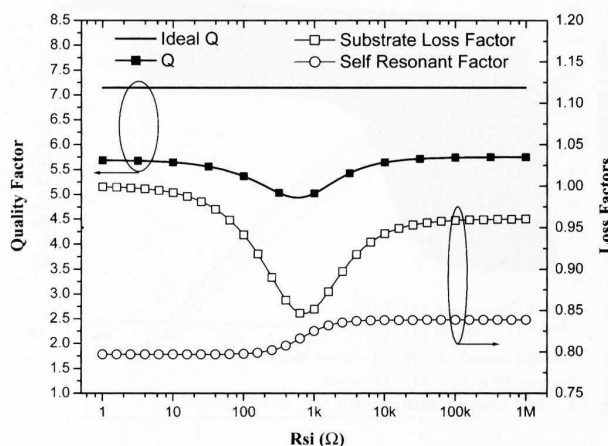
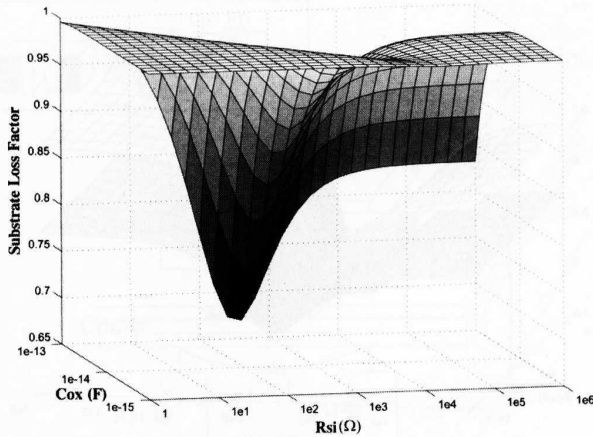
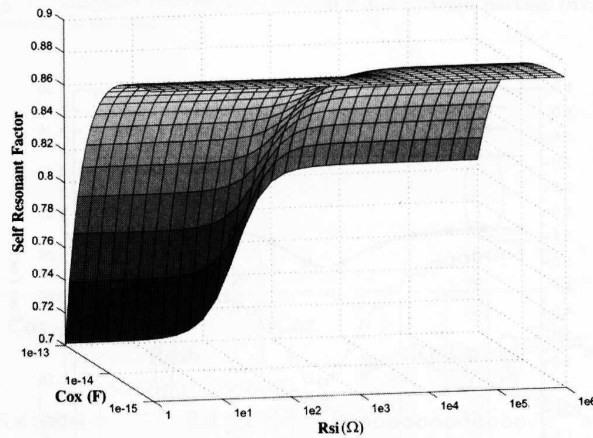


Fig. 11. Q factor in terms of ideal Q , substrate loss factor, and self resonant factor.

This is the expected case using the approximate value of $27 \text{ k}\Omega$ for R_{Si} for this process. The large value of R_{Si} is attributed to the fact that this test wafer is not thinned.

The effectiveness of the PGS is determined by the position of the hollow and the value of R_{Si} prior to placement of the PGS. As Q is calculated using (1), it is necessary to establish what exactly determines the position of the hollow. Fig. 11 shows a graphical representation of (1) versus R_{Si} and also shows individual loss factors, allowing their influence on Q to be seen explicitly. It is seen that the substrate loss factor has the largest impact on the position of the hollow with the self-resonant factor impacting to a lesser degree.

In turn, these loss factors are strongly influenced by C_{ox} , as derived in the Appendix, and may be visualized in Figs. 12 and 13. Consequently, the largest factor in determining the position of the hollow and, thus, the useful range of the PGS, is the value of C_{ox} , which is governed by the area of the inductor and the thickness of the oxide. The impact of C_{Si} is minimal, as seen in Figs. 9 and 10 so a constant value is used for further analysis.

Fig. 12. Substrate loss factor versus C_{ox} and R_{Si} .Fig. 13. Self-resonant factor versus C_{ox} and R_{Si} .

The overall impact of C_{ox} on Q may be seen in Fig. 14, which illustrates how the hollow varies with C_{ox} and R_{Si} .

Following this discussion, it is apparent that the effect of a PGS is more complex than initially thought [27]. A knowledge of initial R_{Si} and C_{ox} is required to predict the subsequent effectiveness of a PGS. If R_{Si} is at infinity relative to the hollow prior to placing a PGS under the inductor, then it will not be effective in improving Q . This method of Q prediction can be applied to any model element or any inductor geometry [11] as each element of (1) is geometrically calculated, as is apparent from Figs. 7 and 8.

V. TEST PATTERNS

All inductors were fabricated using a Freescale Semiconductor BiCMOS 0.18- μm five-metal process [28]. The four top metal layers (Metal5–Metal2) were used for inductor structures and the PGS is placed on the bottom layer (Metal1). Track widths and spacing are 6 μm and the metal thickness is 0.37 μm for Metal5–Metal3 and 0.29 μm for Metal2 and Metal1. Five single-ended 3.62-turn inductors were designed, fabricated, and tested; a double layer Metal5 + Metal4 (M5 + M4) with and without a PGS, a triple layer Metal5 + Metal4 + Metal3 (M5 + M4 + M3) with and without a PGS, and a quadruple layer

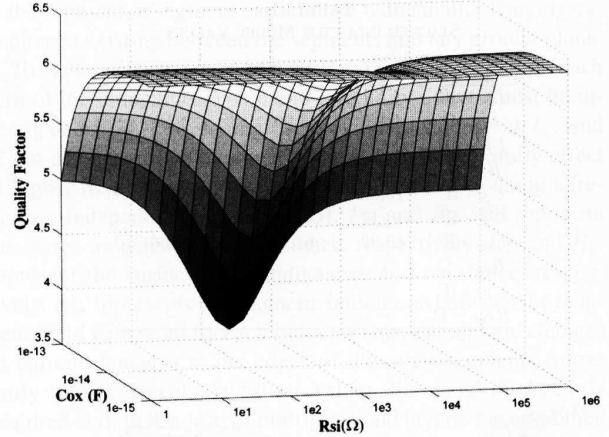
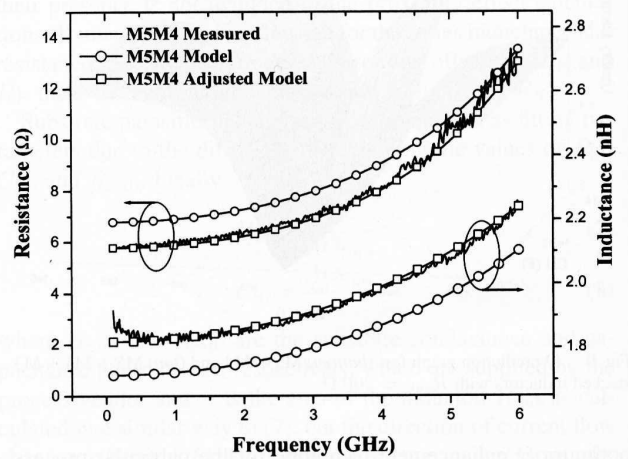
Fig. 14. Q versus C_{ox} and R_{Si} .

Fig. 15. Resistance and inductance of a M5 + M4 single-ended inductor.

Metal5 + Metal4 + Metal3 + Metal2 (M5 + M4 + M3 + M2) without a PGS. The inductors were designed to be probed using Cascade's Infinity ground–signal–ground (GSG) RF probes [29]. Short and open deembedding structures were also fabricated to eliminate the effects of pad parasitics.

VI. RESULTS

From the measured Y -parameters, the inductance, resistance, and Q factor were calculated as follows [30]:

$$L = \frac{\text{Im}\left(\frac{1}{Y_{11}}\right)}{2\pi f} \quad R = \text{Re}\left(\frac{1}{Y_{11}}\right) \quad Q = \frac{\text{Im}\left(\frac{1}{Y_{11}}\right)}{\text{Re}\left(\frac{1}{Y_{11}}\right)} \quad (9)$$

Several inductors were measured and curves representing the average data are presented here along with model comparisons in Figs. 15–22. Using the model in Fig. 8 and the values from Table I, the simulated model matches very well with the inductor measurements. Slight errors exist in calculating the inductance and resistance of each inductor (Figs. 15–17), which may be accounted for by taking linewidth, thickness, and conductivity variations into account. When the model

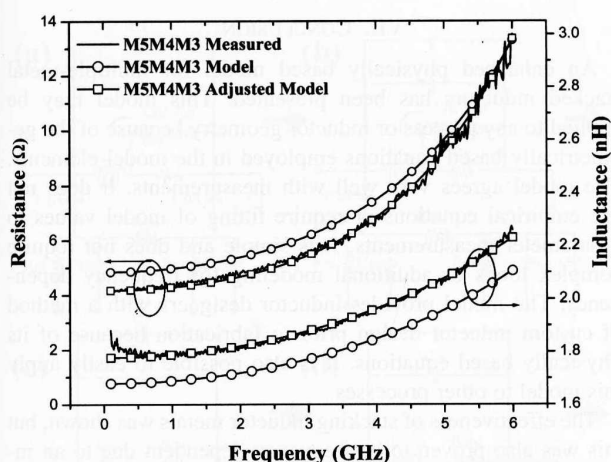


Fig. 16. Resistance and inductance of a M5 + M4 + M3 single-ended inductor.

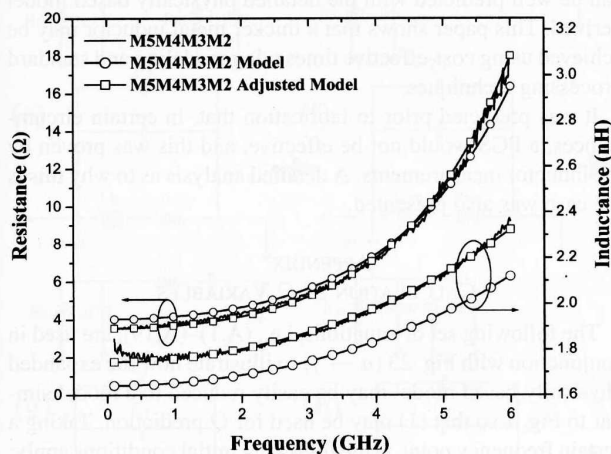


Fig. 17. Resistance and inductance of a M5 + M4 + M3 + M2 single-ended inductor.

values are adjusted for these variations, very good matches with measurements are achieved across the frequency band. It is noted that the calculated fringing capacitance for the M5 + M4 and M5 + M4 + M3 inductors are sufficient to match the frequency dependence of the inductance and resistance measurements. However, extra fringing capacitance is required to match the M5 + M4 + M3 + M2 inductor. This is due to the structure of the thickest inductor with M2 being closest to the substrate. Additionally, due to the complex grounding arrangement for this particular substrate, R_{Sub} was increased. Fig. 18 shows the parasitic dependence of a three metal stacked inductor and shows how the simulation accuracy is improved by successively incorporating more effects. Firstly, the frequency dependence of the simple π model is demonstrated. Subsequently, the proximity and skin effects are added to the model in terms of L_P , L_M , and R_P . As expected, the series resistance of the inductor is affected more than the series inductance, as is seen in Fig. 18. The fringing capacitance (C_F) is then added into the model and, finally, R_{Sub} is added, giving a very good match with measurements. This match illustrates the precise nature of the formulation of this extended physical model.

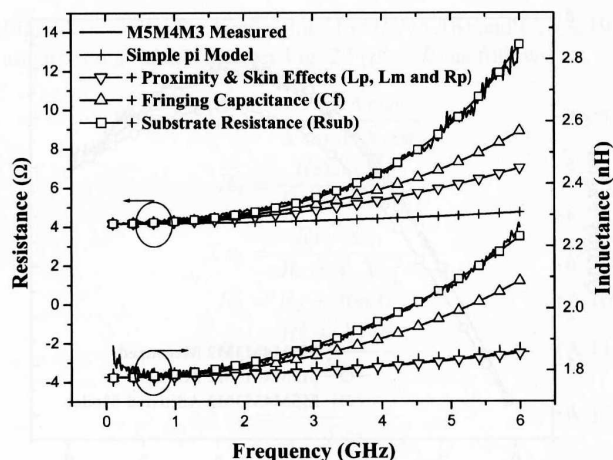
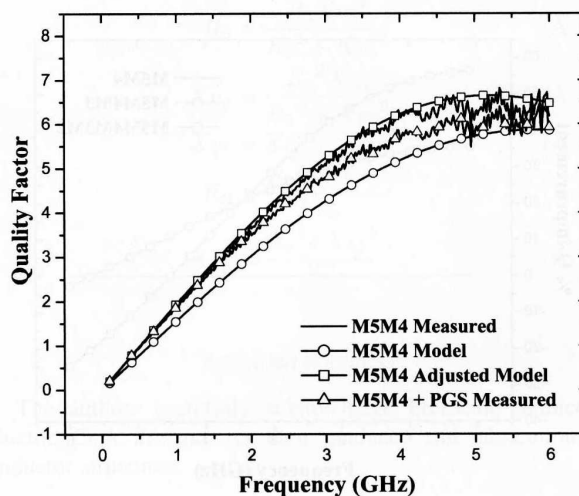
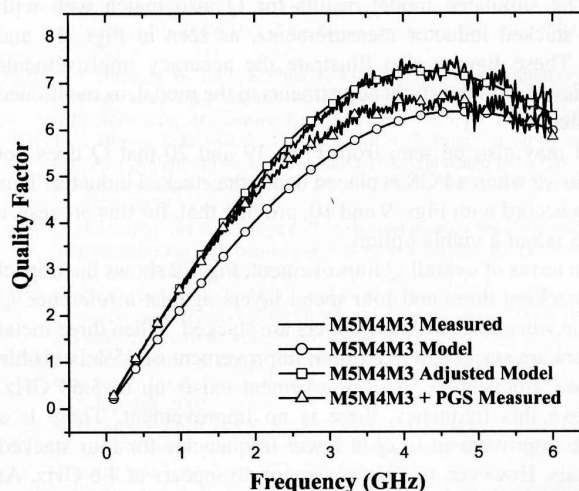


Fig. 18. Impact of extended physical model elements on the resistance and inductance of M5 + M4 + M3 stacked inductor.

Fig. 19. Q of a M5 + M4 single-ended inductor.Fig. 20. Q of a M5 + M4 + M3 single-ended inductor.

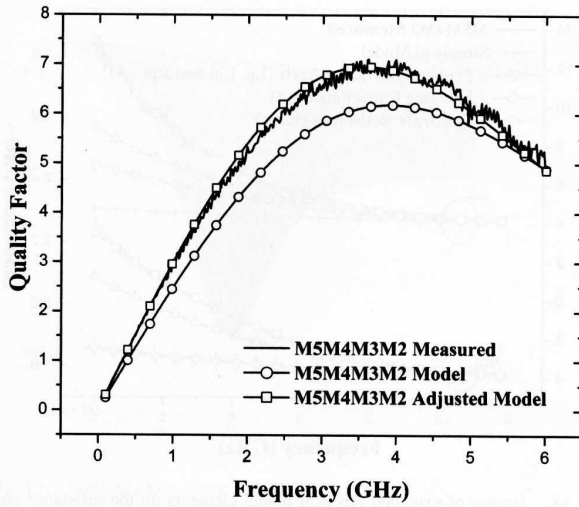


Fig. 21. Q of a M5 + M4 + M3 + M2 single-ended inductor.

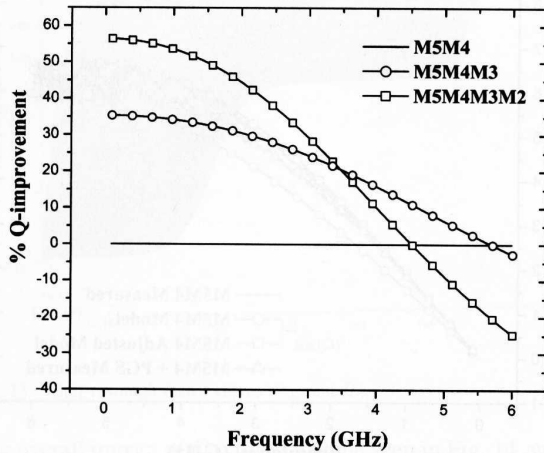


Fig. 22. Q improvement for multiple layers.

The simulated model results for Q also match well with the stacked inductor measurements, as seen in Figs. 19 and 20. These figures also illustrate the accuracy improvements achieved with the slight adjustments to the model, as mentioned earlier.

It may also be seen from Figs. 19 and 20 that Q does not improve when a PGS is placed under the stacked inductor. This is in accord with Figs. 9 and 10, proving that, for this process, a PGS is not a viable option.

In terms of overall Q improvement, Fig. 22 shows the impact of stacking three and four metal layers against a reference Q value when just two metal layers are stacked. When three metal layers are stacked, a maximum improvement of 35% is visible at low frequencies. An improvement exists up to 5.68 GHz. Above this frequency, there is no improvement. There is a 56% improvement in Q at lower frequencies for four stacked metals. However, this improvement disappears at 4.6 GHz. At 5.25 GHz, three metal layers offer a 4% improvement and four metal layers is not an option for Q enhancement.

VII. CONCLUSION

An enhanced physically based model for multiple-metal stacked inductors has been presented. This model may be applied to any process or inductor geometry because of the geometrically based equations employed in the model elements. The model agrees very well with measurements. It does not use empirical equations or require fitting of model values to s -parameter measurements. It is simple and does not require complex loops or additional modeling for frequency dependency. The model provides inductor designers with a method of custom inductor design prior to fabrication because of its physically based equations. It is also possible to easily apply this model to other processes.

The effectiveness of stacking inductor metals was shown, but this was also proven to be frequency dependent due to an increase in inductor parasitics. The simulations and measurements presented show that the behavior of multiple-metal inductors can be well predicted with the detailed physically based model derived. This paper shows that a thicker metal inductor may be achieved using cost-effective timesaving modeling and standard processing techniques.

It was predicted prior to fabrication that, in certain circumstances, a PGS would not be effective, and this was proven by the inductor measurements. A detailed analysis as to why this is the case was also presented.

APPENDIX

CALCULATION OF Q VARIABLES

The following set of equations, i.e., (A.1)–(A.19), are used in conjunction with Fig. 23 ($a \rightarrow j$) to illustrate how the expanded physically based model may be easily reduced to a model similar to Fig. 1 so that (1) may be used for Q prediction. Taking a certain frequency point f , the following initial conditions apply:

$$Xlp = (2\pi f)Lp \quad (\text{A.1})$$

$$Xls = (2\pi f)Ls \quad (\text{A.2})$$

$$Lm = k\sqrt{LpLs} \quad (\text{A.3})$$

$$Xlm = (2\pi f)Lm. \quad (\text{A.4})$$

As the model is essentially single-ended, one port is always grounded. Thus, it is possible to place C_{ox} in parallel with C_{Si} and R_{Si} ($a \rightarrow b$). Reducing all the elements for inductance and resistance to two elements is more complex, as it necessitates the evaluation of voltages and currents in each branch, including the extra induced current resulting from the mutual inductor Lm to give (A.5), (A.6), and Fig. 23 ($b \rightarrow c$). In this same step, C_{ox} is added in parallel with C_{Si} to give C_1 as follows:

$$\begin{aligned} X L s_{eq} &= X l s + \frac{R s^2 X l p - X l m^2 X l p + 2 X l m R s (R s + R p)}{(R s + R p)^2 + X l p^2} \end{aligned} \quad (\text{A.5})$$

$$\begin{aligned} R s_{eq} &= R s + \frac{X l m^2 (R s + R p) - R s^2 R p - R s^3 + 2 X l m X l p R s}{(R s + R p)^2 + X l p^2}. \end{aligned} \quad (\text{A.6})$$

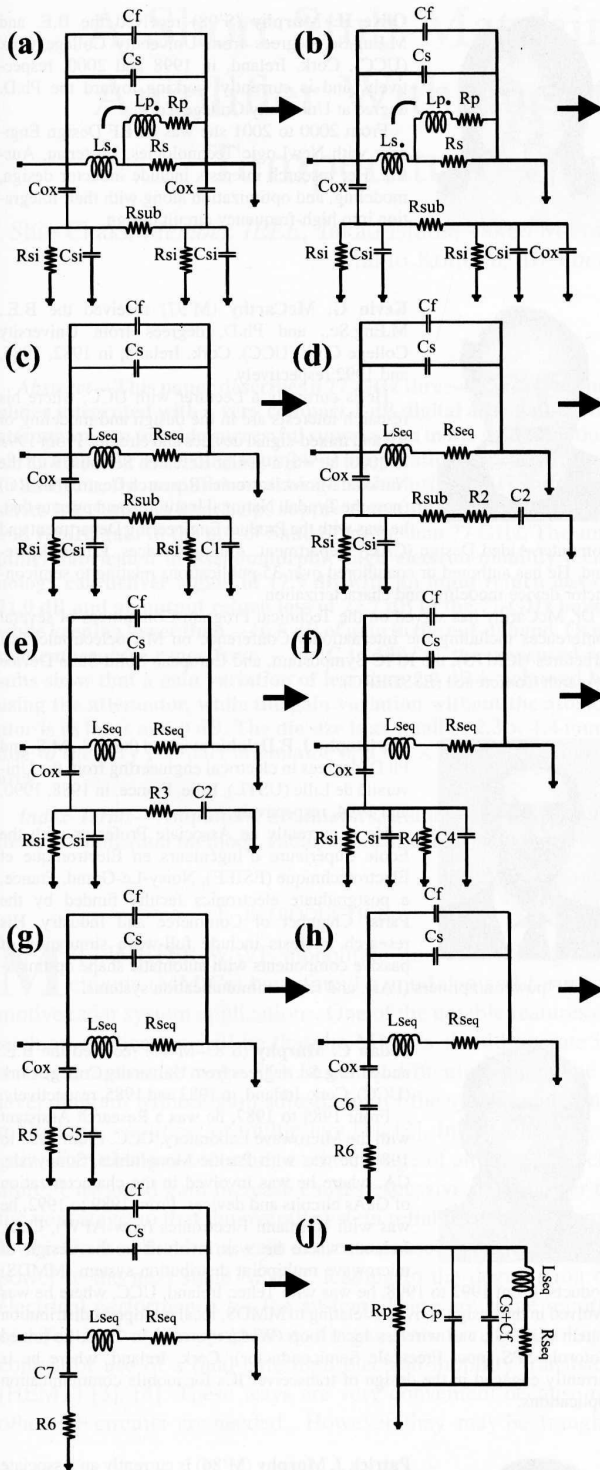


Fig. 23 (c $\rightarrow$ d). The final values for R_p (A.18) and C_p (A.19) are arrived at in this manner Fig. 23 (d $\rightarrow$ k) as follows:

$$X_{c1} = \frac{X_{csi} X_{cox}}{X_{csi} + X_{cox}} \quad (\text{A.7})$$

$$R_2 = \frac{R_{si} X_{c1}^2}{R_{si}^2 + X_{c1}^2} \quad (\text{A.8})$$

$$X_{c2} = \frac{R_{si}^2 X_{c1}}{R_{si}^2 + X_{c1}^2} \quad (\text{A.9})$$

$$R_3 = R_2 + R_{sub} \quad (\text{A.10})$$

$$R_4 = \frac{R_3^2 + X_{c2}^2}{R_3} \quad (\text{A.11})$$

$$X_{c4} = \frac{R_3^2 + X_{c2}^2}{X_{c2}} \quad (\text{A.12})$$

$$R_5 = \frac{R_{si} R_4}{R_{si} + R_4} \quad (\text{A.13})$$

$$X_{c5} = \frac{X_{csi} X_{c4}}{X_{csi} + X_{c4}} \quad (\text{A.14})$$

$$R_6 = \frac{R_5 X_{c5}^2}{R_5^2 + X_{c5}^2} \quad (\text{A.15})$$

$$X_{c6} = \frac{R_5^2 X_{c5}}{R_5^2 + X_{c5}^2} \quad (\text{A.16})$$

$$X_{c7} = X_{c6} + X_{cox} \quad (\text{A.17})$$

$$R_p = \frac{R_6^2 + X_{c7}^2}{R_6} \quad (\text{A.18})$$

$$X_{c_p} = \frac{R_6^2 + X_{c7}^2}{X_{c7}} \quad (\text{A.19})$$

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REFERENCES

- [1] D. H. Weon, J. H. Jeon, J. I. Kim, S. Mohammadi, and L. P. B. Katehi, "High- Q integrated 3-D inductors and transformers for high frequency applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2004, pp. 877–880.
- [2] M. F. Davis, S. W. Yoon, S. Pinel, K. Lim, and J. Laskar, "Liquid crystal polymer-based integrated passive development for RF applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2003, pp. 1155–1158.
- [3] T. S. Horng, J. M. Wu, L. Q. Yang, and S. T. Fang, "A novel modified-T equivalent circuit for modeling LTCC embedded inductors with a large bandwidth," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 12, pp. 2327–2333, Dec. 2003.
- [4] O. H. Murphy and P. J. Murphy, "Low temperature co-fired ceramic and its applications at high frequencies," in *Proc. Irish Signals and Systems Conf.*, Jun. 2002, pp. 333–338.
- [5] Y. S. Lin, C. C. Liu, K. M. Li, and C. H. Chen, "Design of an LTCC tri-band transceiver module for GPRS mobile applications," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 12, pp. 2718–2724, Dec. 2004.
- [6] M. Danesh and J. R. Long, "Differentially driven symmetric microstrip inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 332–341, Jan. 2002.
- [7] S. M. Yim, T. Chen, and K. K. O, "The effects of a ground shield on the characteristics and performance of spiral inductors," *IEEE J. Solid-State Circuits*, vol. 7, no. 2, pp. 237–244, Feb. 2002.
- [8] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

Fig. 23. Transformation of expanded physical model to a simple model for Q calculation.

A parallel-to-series transformation [31] further simplifies the circuit. For example, the parallel arrangement of C_1 and R_{Si} is converted to R_2 (A.8) and C_2 (A.9) using this method, as per

- [9] Y. S. Choi and J. B. Yoon, "Experimental analysis of the effect of metal thickness on the quality factor in integrated spiral inductors for RF IC's," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 76–79, Feb. 2004.
- [10] M. Soyuer, J. N. Burghartz, K. A. Jenkins, S. Ponnappalli, J. F. Ewen, and W. E. Pence, "Multilevel monolithic inductors in silicon technology," *Electron. Lett.*, vol. 31, no. 5, pp. 359–360, Mar. 1995.
- [11] O. H. Murphy, K. G. McCarthy, C. Delabie, A. C. Murphy, T. Chan, and P. J. Murphy, "Differential inductor design incorporating multiple Q-enhancement techniques and expanded physical model," in *Proc. 34th Eur. Microwaves Conf.*, Amsterdam, The Netherlands, Oct. 11–15, 2004, pp. 1373–1376.
- [12] A. C. Watson, D. Melendy, P. Francis, K. Hwang, and A. Weisshaar, "A comprehensive compact-modeling methodology for spiral inductors in silicon-based RFICs," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 3, pp. 849–857, Mar. 2004.
- [13] A. Scuderi, T. Biondi, E. Ragonese, and G. Palmisano, "A scalable model for silicon spiral inductors," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2003, pp. 2117–2120.
- [14] C. P. Yue, C. Ryu, J. Lau, T. Lee, and S. S. Wong, "A physical model for planar spiral inductors on silicon," in *Proc. Int. Electron Devices Meeting*, Dec. 1996, pp. 155–158.
- [15] P. Lorrain and D. Corson, *Electromagnetic Fields and Waves*, 1st ed. San Francisco, CA: Freeman, 1969, ch. 8, pp. 335–335.
- [16] W. B. Kuhn, X. He, and M. Mojaradi, "Modeling spiral inductors in SOS process," *IEEE Trans. Electron Devices*, vol. 51, no. 5, pp. 677–683, May 2004.
- [17] M. C. Hsieh, Y. K. Fang, C. H. Chen, S. M. Chen, and W. K. Yeh, "Design and fabrication of deep submicron CMOS technology compatible suspended high-Q spiral inductors," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 324–331, Mar. 2004.
- [18] S. S. Mohan, M. del Mar Henshenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.
- [19] F. W. Grover, *Inductance Calculations*. New York: Dover, 1964, ch. 5, pp. 31–34.
- [20] A. B. Glaser and G. E. Subak-Sharpe, *Integrated Circuit Engineering*, 2nd ed. Reading, MA: Addison-Wesley, 1979, ch. 4, pp. 118–118.
- [21] J. Sieiro, J. K. Lopez-Villegas, J. Cabanillas, J. A. Osorio, and J. Samitier, "A physical frequency-dependent compact model for RF integrated inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 384–392, Jan. 2002.
- [22] S. C. Wong, G. Y. Lee, and D. J. Ma, "Modeling of interconnect capacitance, delay and crosstalk in VLSI," *IEEE Trans. Semicond. Manuf.*, vol. 13, no. 1, pp. 108–111, Feb. 2000.
- [23] W. B. Kuhn, "Analysis of current crowding effects in multiturn spiral inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 1, pp. 31–38, Jan. 2001.
- [24] C. B. Sia, K. S. Yeo, M. A. Do, and J.-G. Ma, "Metallization proximity studies for copper spiral inductors on silicon," *IEEE Trans. Semicond. Manuf.*, vol. 16, no. 2, pp. 220–227, May 2003.
- [25] Y. Cao, R. A. Groves, N. D. Zamdmer, J.-O. Plouchart, R. A. Wachnik, X. Huang, T.-J. King, and C. Hu, "Frequency-independent equivalent circuit model for on-chip spiral inductors," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 2002, pp. 217–220.
- [26] J. Gil and H. Shin, "A simple wide-band on-chip inductor model for silicon-based RF ICs," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 9, pp. 2023–2028, Sep. 2003.
- [27] C. P. Yue and S. S. Wong, "A study on substrate effects of silicon-based RF passive components," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 1999, pp. 1625–1628.
- [28] J. Kirchgessner, S. Bigelow, F. K. Chai, R. Cross, P. Dahl, A. Duvallet, B. Gardner, M. Griswold, D. Hammock, J. Heddleson, S. Hildreth, A. Irudayam, C. Leshner, S. Meixner, P. Meng, M. Menner, J. McGinley, D. Monk, D. Morgan, H. Rueda, C. Small, S. Stewart, M. Ting, I. To, P. Welch, T. Zirkle, and W. Huang, "A 0.18 μm SiGe: C RF BiCMOS technology for wireless and gigabit optical communication applications," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting*, Sep. 2001, pp. 151–151.
- [29] J. Browne, "On-wafer probes test silicon IC's to 110 GHz," *Microwaves RF*, no. 4, pp. 84–90, Apr. 2003.
- [30] Y. K. Koutsoyannopoulos and Y. Papananos, "Systematic analysis and modeling of integrated inductors and transformers in RF IC design," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 8, pp. 699–713, Aug. 2000.
- [31] R. L. Boylestad, *Introductory Circuit Analysis*, 9th ed. Upper Saddle River, NJ: Prentice-Hall, 2000, ch. 15, pp. 657–658.



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