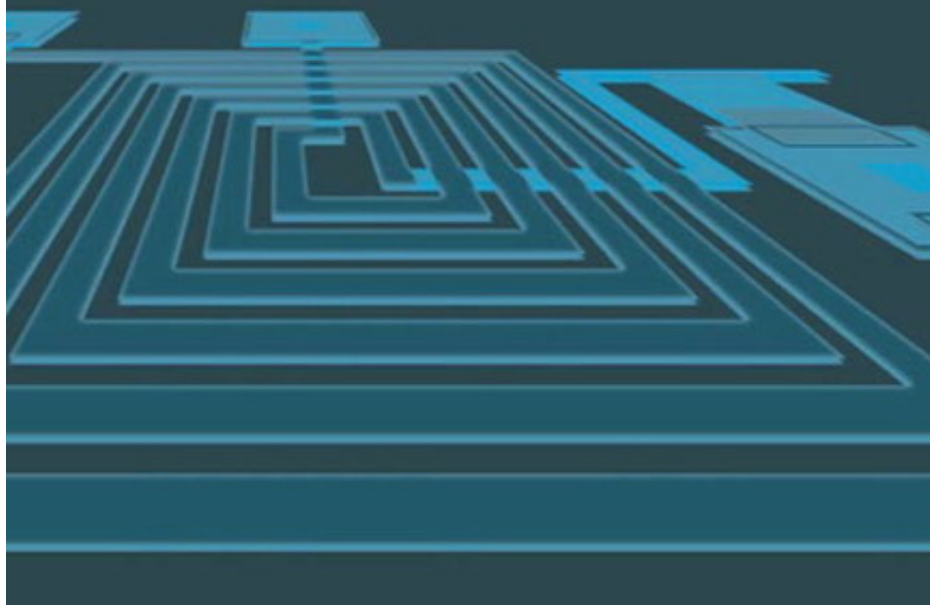


Inder Bahl

Lumped Elements for RF and Microwave Circuits



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2.2.7 Quality Factor

Several different definitions of Q -factors for inductors have been used in the literature [9–18]. The most general definition of Q is based on ratio of energy stored, W_S , to power dissipated, P_D , in the inductor per cycle; that is

$$Q = \frac{\omega W_S}{P_D} \quad (2.8)$$

At low frequencies an inductor's primary reactance is inductive and

$$Q = \frac{\omega \frac{1}{2} L i_0^2}{\frac{1}{2} R i_0^2} = \frac{\omega L}{R} \quad (2.9)$$

where i_0 is the rms value of the current. When the inductor is used as a resonant component close to its *self-resonance frequency* (SRF) f_{res} , a more appropriate definition of the Q -factor is in terms of its 3-dB bandwidth (BW) is given by

$$Q = \frac{f_{\text{res}}}{\text{BW}} \quad (2.10)$$

A third definition of Q -factor, which has been used for distributed resonators, is evaluated from the rate of change of input reactance with frequency [19, 20]:

$$Q = \frac{f_{\text{res}}}{2R} \left[\frac{dX_{\text{in}}}{df} \right] \quad (2.11)$$

where X_{in} is the input reactance of the inductor and dX_{in}/df is determined at f_{res} .

In microwave circuits where the inductors are used far below the self-resonance frequency, the degree at which the inductor deviates from an ideal component is described by the effective quality factor Q_{eff} , expressed as [18]:

$$Q_{\text{eff}} = \frac{\text{Im}[Z_{\text{in}}]}{\text{Re}[Z_{\text{in}}]} = \frac{X}{R} = \frac{\omega L_e}{R} \quad (2.12)$$

where $\text{Re}[Z_{\text{in}}]$ and $\text{Im}[Z_{\text{in}}]$ are the real and imaginary parts of the input impedance of the inductor, respectively. This definition leads to the unusual

condition that Q_{eff} becomes zero at resonance. Since in RF and microwave circuits, for series applications of inductors, the operating frequencies are well below the self-resonance frequency, the preceding definition is traditionally accepted.

2.2.8 Self-Resonant Frequency

The self-resonant frequency (f_{res}) of an inductor is determined when $\text{Im}[Z_{\text{in}}] = 0$; that is, the inductive reactance and the parasitic capacitive reactance become equal and opposite in sign. At this point, $\text{Re}[Z_{\text{in}}]$ is maximum due to parallel resonance and the angle of Z_{in} changes sign. The inductor's first resonant frequency is of the parallel resonance type. Beyond the resonant frequency, the inductor becomes capacitive.

2.2.9 Maximum Current Rating

The maximum dc current an inductor can withstand without being destroyed (fusing or electromigration) or overheating due to its finite resistance is known as the *maximum current rating*. This maximum current limit depends on the conductor material, shape, core material used, surrounding environment, and temperature.

2.2.10 Maximum Power Rating

The maximum RF power that can be applied safely to an inductor without changing its characteristics or destroying it due to heat generated is known as the *maximum power rating*. The maximum power limit depends on the inductor's Q , area/volume, core material used, surrounding environment, and temperature. Printed inductors have higher maximum power ratings than air coil inductors.

2.2.11 Other Parameters

The reader must consider several other inductor parameters per design requirements. These parameters are as follows:

Operating temperature range. This is the specified temperature limit within which the inductor can be operated safely. Above the specified limits, the inductor's maximum current rating is reduced due to thermal effects as well as reliability concerns.

Temperature coefficient of inductance. This is the amount the inductance changes with temperature and is expressed in parts per million per degree Celsius (ppm/°C).

3

Printed Inductors

Planar inductors can be classified into two-dimensional and three-dimensional structures. Two-dimensional inductors are further grouped into four categories based on their shape, that is, meander, rectangular, hexagonal, or octagonal and circular as shown in Figure 3.1. Table 3.1 summarizes the major advantages and disadvantages of each shape. The circular geometry has the best electrical performance, whereas meander line inductors are seldom used. Three-dimensional inductor topologies are shown in Figure 3.2 and their major advantages and disadvantages are summarized in Table 3.2.

In this chapter we discuss planar inductors on semiconductor substrates such as Si and GaAs, on printed circuit boards, and on hybrid integrated circuit substrates. Silicon is a potential candidate for RFICs, and GaAs is widely used for MMICs. Standard silicon substrates have low resistivity and Si-based technologies use thin metallization layers that give rise to high substrate and conductor losses. In comparison, GaAs substrates are semi-insulating (having very high resistivity), and GaAs-based technologies use thick electroplated gold interconnects. GaAs passive components have low capacitive and conductor losses. Several different techniques in both these technologies are employed to reduce losses in order to enhance the quality factor of inductors.

Low-cost wireless applications require integration of more circuit components using *multichip modules* (MCMs). At RF, organic substrate-based MCM technology using a standard FR-4 board is another viable approach to develop low-cost integrated solutions by printing inductors on the same substrate. Several hybrid integrated technologies are being pursued to integrate inductors along with other passive components into a MCM substrate. These include thin film, thick film, and LTCC; and are suitable for high-quality, low-cost, and compact, high-performance inductors, respectively.

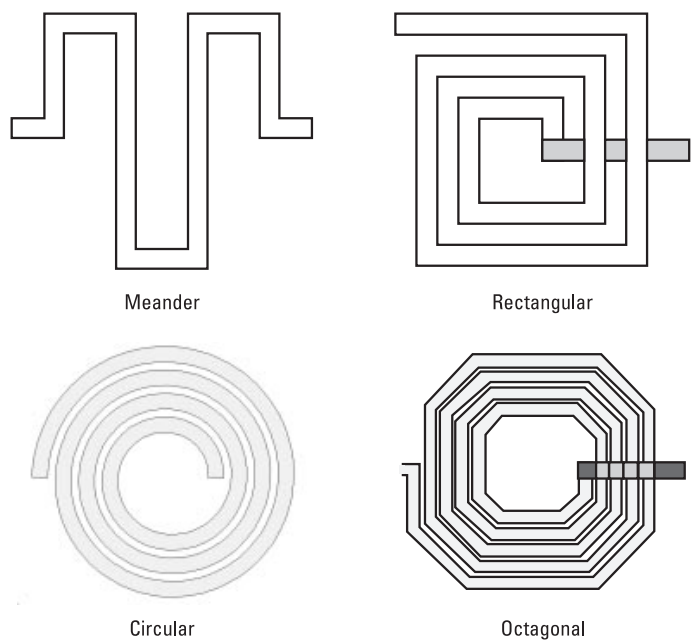


Figure 3.1 Two-dimensional inductor types: (a) meander, (b) rectangular, (c) circular, and (d) octagonal.

Table 3.1
Two-Dimensional Inductor Configurations and Their Features

Configuration	Advantage	Disadvantage
Meander line	Lower eddy current resistance	Lowest inductance and SRF
Rectangular	Easy layout	Lower SRF
Octagonal	Higher SRF	Difficult layout
Circular	Highest SRF	Difficult layout

3.1 Inductors on Si Substrate

RF monolithic ICs are being developed using Si employing CMOS, BiCMOS, and SiGe-HBT technologies in order to take advantage of mature Si processes and low-cost potential. One of the major disadvantages of standard Si technologies is the high substrate losses due to much lower substrate resistivity (less than $10^3 \text{ } \Omega\text{-cm}$) compared to GaAs substrate ($10^7 \text{ } \Omega\text{-cm}$). High-density CMOS

Finite resistivity loss can be minimized by either using very high resistivity substrates or by placing a shield between the oxide layer and the substrate.

3.1.2.3 Magnetic Loss

In heavily doped Si substrates, currents induced by the penetration of the magnetic fields of the inductor into the substrate cause extra resistive loss. Consider Figure 3.4, which shows magnetic field flux lines associated with the coil excitation current. The flux lines uniformly surround the inductor and penetrate into the substrate. As discussed in Section 3.1.1, due to the Faraday-Lenz law, loops of eddy currents I_{sub} flow in the low-resistivity substrate underneath the coil, with higher current density closer to the coil. The direction of I_{sub} is opposite to the direction of I_{coil} , giving rise to extra substrate loss. Because this loss is associated with magnetic fields, it is commonly referred to as *magnetic* or *inductive substrate loss*. Substrates with high resistivity have negligible magnetic loss.

In summary, by using narrow conductors that meet skin effect requirements ($W \cong 3\delta$) in the inner turns, using a hollow coil design, and using compact area coils, one can keep the substrate loss to a minimum. Because the magnetic field in a small coil penetrates less deeply into the substrate, eddy current loss is not severe as for large coils. Therefore, an optimum solution, in terms of inside dimensions and coil area for a given substrate, can be found. These losses are again discussed in detail in Section 3.1.5.

3.1.3 Layout Considerations

For a given inductance value, one would like to have the highest possible values of Q and SRF in the smallest possible area of an inductor using standard process

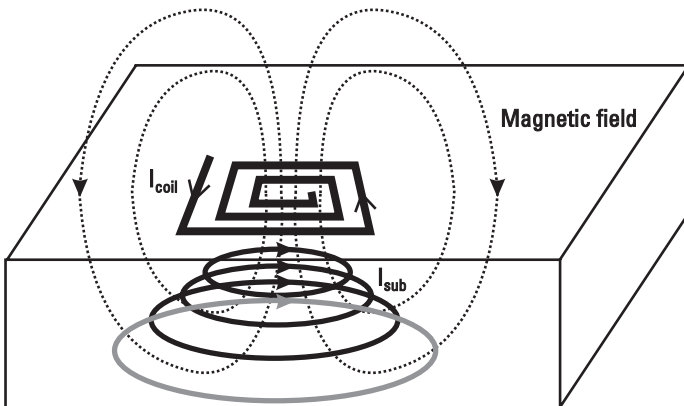


Figure 3.4 Currents and fields in a coil printed on a lossy Si substrate.

between the inductor and ports. As a first-order approximation, shunt values for ports 1 and 2 can be assumed identical.

3.1.5 Q -Enhancement Techniques

One of the important characteristics of an inductor on a Si substrate is its quality factor Q . Techniques used to enhance the Q -factor of inductors on a Si substrate can be grouped into four categories as shown in Figure 3.8. These are based on trace layout, trace metal parameters, the use of a high resistivity substrate, and the use of a substrate shield. These are discussed in this section.

3.1.5.1 Trace Layout

For a given set of inductor conductor and substrate materials, one can optimize the inductor's Q by properly selecting the physical layout of the inductor trace to minimize the resistive, capacitive, and inductive losses. Several techniques discussed in the literature include variable line width [21, 38], differential configuration [22, 57], and vertical inductor.

Variable Line Width

The effect of eddy currents can be minimized by making the line widths of the inner turns of the inductor narrower than the outer turns [21, 38]. Narrower line widths have higher dc resistance; however, this is compensated by using wider line widths in the outer turns. This structure is shown in Figure 3.9(a). In this structure the improvement in Q -value is more pronounced at higher than lower frequencies, because the effect of eddy currents is more severe at high frequencies.

For inductors having variable line width on a conducting Si substrate, no substantial improvement in Q is possible, because of excessive capacitive losses

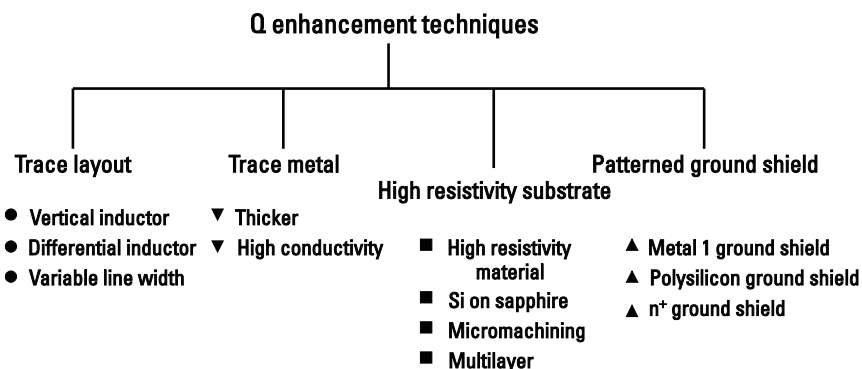


Figure 3.8 Q -Enhancement techniques for inductors on Si substrate.

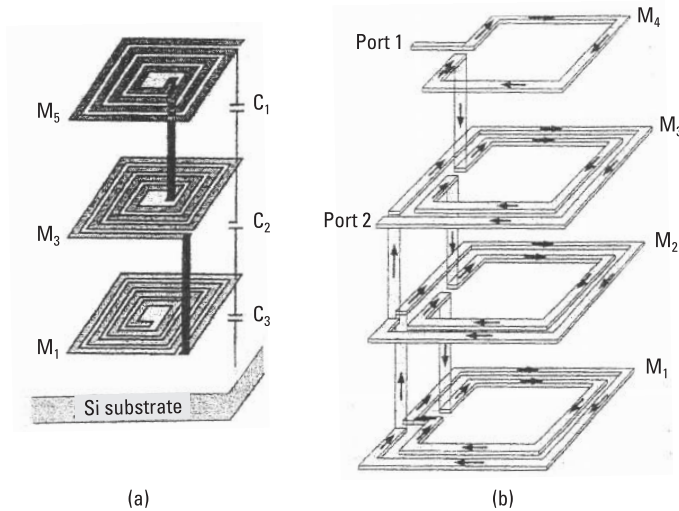


Figure 3.19 (a) Conventional three-level inductor using metals 5, 3, and 1 on a Si substrate. (b) Improved SRF four-level stacked inductor with current flow path. (From: [48]. © 2002 IEEE. Reprinted with permission.)

Table 3.8

Summary of Measured Performance of Stacked Inductors Fabricated in 0.25- μm CMOS Technology*

Inductor	Metal Layers	Number of Turns	L (nH)	Measured f_{res} (GHz)
L_1 (240 μm) ²	5,4	7	45	0.92
L_2 (240 μm) ²	5,3	7	45	1.5
L_3 (240 μm) ²	5,2	7	45	1.8
L_4 (240 μm) ²	5,4,3	7	100	0.7
L_5 (240 μm) ²	5,3,1	7	100	1.0
L_6 (200 μm) ²	5,2,1	5	50	1.5
L_7 (200 μm) ²	5,2,1	5	48	1.5
L_8 (240 μm) ²	5,4,3,2	7	180	0.55
L_9 (240 μm) ²	5,4,3,2,1	7	266	0.47

*Line width = 9 μm ; line spacing = 0.72 μm .

9

Via Holes

In RF and microwave circuits, low-loss and low-inductance grounds are very important to achieve good gain, noise figure, insertion loss, VSWR, output power, *power-added efficiency* (PAE), and bandwidth performance. In MICs/MMICs, one needs the backside ground metallization to be connected with minimum possible inductance path to the top side of the substrate having RF ground pads. In MICs four basic techniques are used to achieve such ground connections. As shown in Figure 9.1, these are via hole, wire bonds, ribbon bonds, and wrap-around grounds. For RF applications of MMICs, via hole and wire bond techniques are commonly used, whereas the via hole is an integral part of monolithic microwave and millimeter-wave integrated circuits. A comparison of these ground connections is given in Table 9.1.

9.1 Types of Via Holes

There are two types of via holes (Figure 9.2): one used for interconnections of metal layers in a multilayer technology and the second type used for a backside via hole ground. These are briefly discussed next.

9.1.1 Via Hole Connection

In multilayer ceramics, via hole connections are an integral part of the process. The holes are punched in each green ceramic sheet and subsequently filled with a metal paste consisting of tungsten or molybdenum, which makes interconnections from layer to layer. Computer-controlled step and repeat equipment is