

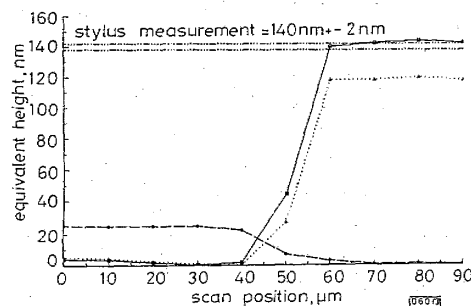


Fig. 3 Experimental results for gold-silicon step

..... combined response
 ---- material response
 — true topography

Results are shown in Fig. 3 for a line scan across a step consisting of a gold layer on a silicon substrate. The dotted line represents the overall phase measured by the interferometer and would correspond to a step height of ~ 116 nm. The broken line shows the correction of 26 nm which must be made to this result due to material properties, and is calculated from the ellipsometric profile. Finally the solid line shows the final result obtained when the material measurement is subtracted from the overall result, leaving a measurement which may be attributed to topography alone. It can be seen that this correction leads to a result which is in excellent agreement to that obtained by a mechanical stylus probe on the same sample.

In conclusion, if optical interferometry is to be used to profile samples with material variations it is important to make an adjustment to the phase measurement in order to compensate for material effects. Our results show that the technique described above is capable of determining the phase changes due to material variations, so that the phase shift due to topography alone can be recovered. Future publications are to describe the system operation in more detail and discuss the algorithm used to calculate the phase shift due to material properties.

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Multilevel monolithic inductors in silicon technology

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Indexing terms: BiCMOS integrated circuits, Inductors, MMIC

Multilevel monolithic inductors implemented in a standard BiCMOS technology are presented. Use of top metal layers shunted with vias provides Q values approaching 10 at 2.4 GHz and above 6 at 900 MHz for a 2 nH inductor. There is no modification to the conventional wiring metallurgy and no need for extra processing steps.

Introduction: Miniaturisation of RF electronic circuits is very desirable to reduce the manufacturing costs. Integration in a silicon VLSI technology can provide many high-speed and baseband functions, thus offering a low-cost solution. The problem of producing high- Q inductors in silicon technologies, however, presents a serious challenge to RF integration at widely used microwave frequencies from 900 MHz to 2.4 GHz. Recent attempts to integrate inductors into conventional silicon technologies have yielded either inductor Q values of less than 5 [1], or required additional processing steps to remove the lossy silicon substrate [2]. Another obvious alternative is to use more conductive metallisation schemes, such as gold, and high-resistivity substrates by modifying the technology accordingly [3]. In this Letter, however, we present a different approach which does not rely on any modifications to a standard silicon technology. The reduction of the inductor loss is achieved by use of multiple upper levels to implement the inductor. Because almost all of the current silicon VLSI technologies have at least three or four levels of metal with relatively thick dielectric isolation, this approach can easily be used without any extra cost.

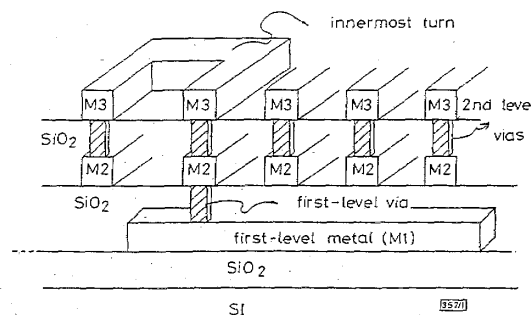


Fig. 1 Cross-section of four-turn M2/M3 inductor with M1 cross-under (not drawn to scale)

Inductor design: It is well known that the resistance of a metal line that forms a spiral inductor is a major contributor to the inductor Q degradation. One way to reduce this effect is to use wide metal lines. This, however, increases the inductor area and the parasitic capacitance associated with the structure. The larger inductor area limits the miniaturisation that can be achieved, and the parasitic capacitance limits its useful frequency range and increases the coupling through the substrate. A better way to solve this problem is to use the top metal levels available within a multilevel wiring technology and connect them through a generous number of inter-level vias to simulate a thicker, hence more conductive, spiral structure. Fig. 1 shows the cross-section of such an inductor with four turns and three levels of metal. The top metal levels M2 and M3 implement the turns and the lowest level M1 is used as a cross-under for the inside terminal connection. Three different versions of the four-turn structure with the same lateral dimensions have been built by using levels M2/M3, M3/M4 and M2/M3/M4 to implement the spiral turns in a four-level metal silicon technology. A custom 3-D electromagnetic simulation tool [4] predicted inductor values of 1.8-1.9 nH with Q values up to 11 at 2.4 GHz. Simulation of the same inductor using only level M2 shows a Q of 5.5 at 2.4 GHz, a 50% degradation.

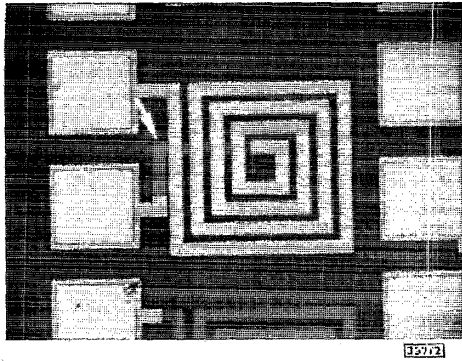


Fig. 2 Chip photograph of M2//M3//M4 inductor test site

Measurement results: Four aluminium wiring levels of a 0.8 μm BiCMOS technology [5] are used to implement the spiral inductors. The levels M2 and M3 have a thickness of 1 μm , and M4 is 2 μm thick. The dielectric thickness under M2 and M3 is about 4.5 and 7 μm , respectively. The substrate resistivity is 10 $\Omega\cdot\text{cm}$. The total inductor area is $230 \times 230 \mu\text{m}^2$ with a metal pitch of 26 μm . Fig. 2 shows one of the fabricated inductor structures. The measurements are performed at wafer level using on-chip calibration techniques and microwave probes. The one-port reflection coefficient S_{11} is measured and plotted on a Smith chart as a function of frequency. Measured self-resonance frequencies are more than 15 GHz for all three structures indicating a very wide useful range for this inductor value. Q is computed from the measured reactance and resistance. Table 1 summarises the experimental results at 900 and 2400 MHz. Overall, there is a good correlation between the simulated and measured results. The inductor M2//M3 has the lowest Q factor due to the minimum equivalent metal thickness.

Table 1: Summary of experimental results at 0.9 and 2.4 GHz

	M2//M3		M3//M4		M2//M3//M4	
F_{meas}	L	Q	L	Q	L	Q
GHz	nH		nH		nH	
0.9	2.2	4.9	2.1	6.4	2.2	6.0
2.4	2.2	7.2	2.0	8.2	2.1	9.3

The inductor M2//M3//M4 has the highest Q (9.3) at 2.4 GHz. At 900 MHz, the M2//M3//M4 structure has a slightly lower Q than M3//M4 (6 against 6.4) indicating the detrimental effects of the substrate losses. These results show that it is possible to integrate inductors with Q values above 5 in a conventional silicon technology without resorting to exotic techniques.

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10GHz-spaced arrayed-waveguide grating multiplexer with phase-error-compensating thin-film heaters

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Indexing terms: Grating demultiplexers

An arrayed-waveguide grating multiplexer with thin-film heaters is fabricated to compensate for phase errors in arrayed waveguides. The phase errors are measured by Fourier transform spectroscopy with a low-coherence interferometer and are used as a monitor when we adjust the phases by controlling thin-film heaters. A channel crosstalk of $\sim 25\text{dB}$ and a loss of 4.2 dB are achieved in a 5×5 10GHz-spaced multiplexer.

Introduction: The arrayed-waveguide grating (AWG) multiplexer is one of the most promising components for optical communication systems. A channel crosstalk of $\sim 30\text{dB}$ has been realised in an AWG multiplexer with a channel spacing of 100GHz [1]. However, a 10GHz-spaced multiplexer has exhibited a higher channel crosstalk [2]. In an earlier Letter we measured the power and phase of the light propagating through each of the arrayed waveguides in the above multiplexers and showed that phase errors are the main cause of the high crosstalk in the 10GHz-spaced multiplexer [3]. Because the phase errors are caused by the random deviation of the optical path lengths of the arrayed waveguides, it increases with path length difference, resulting in higher crosstalk in a multiplexer with a narrower channel spacing.

This Letter describes a way to compensate for phase errors by inducing a phase shift in an arrayed waveguide after fabrication. We demonstrate phase error compensation for a 10GHz-spaced 5×5 AWG multiplexer with thin-film heaters formed on arrayed waveguides.

Principle: The actual optical length of the arrayed waveguide is different from the designed value due to the variations in refractive index, waveguide dimension and waveguide length caused during fabrication. When the designed optical length and the difference between the designed and actual optical lengths of an i th arrayed waveguide are denoted as L_i and δL_i , the phase shift ϕ_i due to light propagation through the i th waveguide is given by

$$\phi_i = (2\pi/\lambda)L_i + (2\pi/\lambda)\delta L_i \quad (1)$$

The second term of this equation is a phase error which causes a degradation in the frequency response. To compensate for the phase error, we add an excess optical length p_i individually at a given wavelength λ_0 so that all the phases satisfy the following equation:

$$\phi_i(\lambda_0) = (2\pi/\lambda_0)L_i + (2\pi/\lambda_0)\delta L_i + (2\pi/\lambda_0)p_i \quad (2)$$

$$= (2\pi/\lambda_0)L_i + 2\pi m_i + C \quad (3)$$

where m_i is an integer and C is a constant. In this case, the phase at wavelengths other than λ_0 is given by

$$\phi_i(\lambda_0 + \delta\lambda) = [2\pi/(\lambda_0 + \delta\lambda)](L_i + \delta L_i + p_i) \quad (4)$$

$$= 2\pi L_i/(\lambda_0 + \delta\lambda) + (2\pi m_i + C) \quad (5)$$

$$- (2\pi m_i + C)[\delta\lambda/(\lambda_0 + \delta\lambda)]$$

Therefore, phase adjustment at a given wavelength λ_0 will result in phase error compensation around λ_0 , when the third term in eqn. 5 is negligible. Excess optical length can be provided by using the thermo-optic effect with a thin-film heater, the photoelastic effect with a-Si film or refractive index change by intense UV light irradiation [4, 5].

Experiments and results: The experimental setup is shown in Fig. 1. The device under test was a 10GHz-spaced 5×5 AWG multiplexer constructed with Ge-doped silica-based single-mode optical waveguides [4]. It consists of five input/output waveguides, two concave slab waveguides, 21 arrayed waveguides with a path length difference of $\Delta L = 3312\mu\text{m}$, and 21 Cr thin-film heaters. The configuration of the above waveguides is the same as that in a