

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,

Petitioner

v.

REALTEK SEMICONDUCTOR CORPORATION,

Defendant

Case No. IPR2023-00789

Patent 7,936,245

DECLARATION OF SYLVIA D. HALL-ELLIS, Ph.D.

I, Sylvia D. Hall-Ellis, declare as follows:

I. INTRODUCTION

1. My name is Sylvia D. Hall-Ellis. I have been retained as an expert by Advanced Micro Devices, Inc., the Petitioner.

2. I have written this declaration at the request of the Petitioner to provide my expert opinion regarding the authenticity and public availability of several publications. My declaration sets forth my opinions in detail and provides the basis for my opinions regarding the authenticity and public availability of these publications. If called to testify in the above-captioned proceeding, I will testify regarding the opinions and bases set forth below.

3. I reserve the right to supplement or amend my opinions, and bases for them, in response to any additional evidence, testimony, discovery, argument, and/or other additional information that may be provided to me after the date of this declaration.

4. I am being compensated for my time spent working on this matter at my normal consulting rate of \$350 per hour, plus reimbursement for any additional reasonable expenses. My compensation is not in any way tied to the content of this declaration, the substance of my opinions, or the outcome of this proceeding. I have no other interests in this proceeding or with any of the parties.

5. All the materials that I considered and relied upon are discussed explicitly in this declaration.

II. QUALIFICATIONS

6. I am currently an Adjunct Professor in the School of Information at San José State University in San José, California. I obtained a Master of Library Science from the University of North Texas in 1972 and a Ph.D. in Library and Information Science from the University of Pittsburgh in 1985. Over the last fifty years, I have held various positions in the field of library and information resources. I was first employed as a librarian in 1966 and have been involved in the field of library sciences since, holding numerous positions.

7. I am a member of the American Library Association (ALA) and its Association for Library Collections & Technical Services (ALCTS) Division, and I served on the Committee on Cataloging: Resource and Description (which wrote the new cataloging rules) and as the chair of the Committee for Education and Training of Catalogers and the Competencies and Education for a Career in Cataloging Interest Group. I also served as the founding Chair of the ALCTS Division's Task Force on Competencies and Education for a Career in Cataloging. Additionally, I have served as the Chair for the ALA Office of Diversity's Committee on Diversity, as a member of the REFORMA National Board of Directors, as a member of the Editorial Board for the ALCTS premier cataloging

journal, *Library Resources and Technical Services*, and as a Co-Chair of the Membership Committee for the Library Research Round Table (LRRT) of the American Library Association. Currently I serve as a member of the LRRT Nominating Committee.

8. I have also given over one hundred presentations in the field, including several on library cataloging systems and Machine-Readable Cataloging (“MARC”) standards. My current research interests include library cataloging systems, metadata, and organization of electronic resources.

9. I have been deposed twenty-seven times: (1) *Symantec Corp. v. Finjan, Inc.*, Petition for *Inter Partes Review* of U.S. Patent No. 7,613,926, May 26, 2016, on behalf of Symantec Corp.; (2) *Symantec Corp. v. Finjan, Inc.*, 14-cv-299-HSG (N.D. Cal.), on behalf of Symantec Corp., September 14, 2017; (3) one deposition for ten matters: *Intellectual Ventures I LLC v. AT&T Mobility LLC*; AT&T Mobility II LLC, New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Wayport, Inc., and Cricket Wireless LLC, C.A. No. 12-193 (LPS); *Intellectual Ventures II LLC v. AT&T Mobility LLC*; AT&T Mobility II LLC, New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Wayport, Inc., and Cricket Wireless LLC, C.A. No. 13-1631 (LPS); *Intellectual Ventures I LLC v. T-Mobile USA, Inc. and T-Mobile US, Inc.*, C.A. No. 13-1632 (LPS); *Intellectual Ventures II LLC v. T-Mobile USA, Inc. and T-Mobile US, Inc.*, C.A.

No. 13-1633 (LPS); *Intellectual Ventures I LLC, v. Nextel Operations, Inc., Sprint Spectrum L.P., Boost Mobile, LLC and Virgin Mobile USA, L.P.*, C.A. No. 13-1634 (LPS); *Intellectual Ventures II LLC v. Nextel Operations, Inc., Sprint Spectrum L.P., Boost Mobile, LLC and Virgin Mobile USA, L.P.*, C.A. No. 13-1635 (LPS); *Intellectual Ventures I LLC, v. United States Cellular Corporation*, C.A. No. 13-1636 (LPS); *Intellectual Ventures I LLC v. United States Cellular Corporation*, C.A. No. 13-1637 (LPS); *Intellectual Ventures II LLC v. AT&T Mobility LLC, AT&T Mobility II LLC, New Cingular Wireless Services, Inc.*, C.A. No. 15-799 (LPS); *Intellectual Ventures I LLC v. T-Mobile USA, Inc. and T-Mobile US, Inc.*, C.A. No. 15-800 (LPS), on behalf of AT&T Mobility LLC; AT&T Mobility II LLC, Boost Mobile, LLC Cricket Wireless LLC, Nextel Operations, Inc., New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Sprint Spectrum L.P., T-Mobile USA, Inc., T-Mobile US, Inc., United States Cellular Corporation Virgin Mobile USA, L.P., and Wayport, Inc., November 15, 2016; (4) *Hitachi Maxell, LTD., v. Top Victory Electronics (Taiwan) Co. Ltd., et al.*, 2:14-cv-1121 JRG-RSP (E.D. Texas), on behalf of Top Victory Electronics (Taiwan) Co. LTD, *et. al.*, January 20, 2016; (5) *Sprint Spectrum, L.P. v. General Access Solutions, Ltd.*, Petition for *Inter Partes* Review of U.S. Patent No. 7,173,916, on behalf of Sprint Spectrum L.P., July 13, 2018; (6) *Nichia Corporation v. Vizio, Inc.*, 8:16-cv-00545; on behalf of Vizio, Inc., October 12, 2018; (7) *Intellectual Ventures I*

LLC, v. T-Mobile USA, Inc., T-Mobile US, Inc., Ericsson Inc., and Telefonaktiebolaget LM Ericsson, 2:17-cv-00557 (JRG), on behalf of T-Mobile USA, Inc., T-Mobile US, Inc., Ericsson Inc., and Telefonaktiebolaget LM Ericsson, October 19, 2018; (8) *Pfizer, Inc. v. Biogen, Inc.*, Petition for *Inter Partes Review* of U.S. Patent No. 8,821,873, on behalf of Pfizer, November 3, 2018; (9) *Finjan, Inc. v. ESET, LLC and ESET SPOL. S.R.O.*, 3:17-cv-00183-CAB-BGS, on behalf of ESET, January 15, 2019; (10) *Finjan, Inc. v. Cisco Systems, Inc.*, 5:17-cv-00072-BLF-SVK, on behalf of Cisco Systems, Inc., September 6, 2019; (11) *Facebook, Inc., Instagram, LLC and Whatsapp Inc. v. Blackberry Limited*, Petition for *Inter Partes Review* of U.S. Patent No. 9,349,120 B2, on behalf of Facebook, Inc., Instagram, LLC and Whatsapp Inc. December 20, 2019; (12) *3Shape A/S and 3Shape Inc. v. Align Technology, Inc.*, Petition for *Inter Partes Review* of U.S. Patent No. 7,156,661, IPR 2020-00222 and IPR 2020-00223, August 10, 2020, on behalf of 3Shape A/S and 3Shape Inc.; (13) *Finjan Inc. v. Rapid7, Inc. and Rapid7 LLC*, Northern District of Delaware; 1:18-cv-01519-MN, September 15, 2020; (14) *VLSI Technology LLC v. Intel Corporation*, Western District of Texas, 6:19-cv-00254, 6:19-cv-00255, 6:19-cv-00256, on behalf of Intel Corporation, September 23, 2020; (15) *Finjan Inc. v. Sonicwall, Inc.*, Northern District of California, 5:17-cv-04467-BLF-HRL, on behalf of Sonicwall, Inc., October 27, 2020; (16) *VLSI Technology, LLC v. Intel*

Corporation, District of Delaware, 1:18-cv-00966-CFC-CJB, February 5, 2021, on behalf of the Intel Corporation; (17) *Unified Patents, LLC v. Good Kaisha IP Bridge 1*, Petition for *Inter Partes Review* of U. S. Patent 7,817,868, February 11, 2021, on behalf of Unified Patents; (18) *Finjan, Inc. v. Qualsys, Inc.*, Northern District of California, 4:18-cv-07229-YGR, March 1, 2021, on behalf of Qualsys, Inc.; (19) *Qualcomm, Inc. v. Monterey Research LLC*, Petition for *Inter Partes Review* of U. S. Patent 6,534,805, May 6, 2021, on behalf of Qualcomm, Inc.; (20) *Hulu, LLC v. Sound View Innovations, LLC*, Petition for *Inter Partes Review* of U. S. Patent 5,806,062, May 14, 2021, on behalf of Hulu, LLC; (21) *VLSI Technology LLC v. Intel Corporation*, Western District of Texas, 6:19-cv-00254, 6:19-cv-00255 and 6:19-cv-00256, August 3, 2021, on behalf of Intel Corporation; (22) *Liquidia Technologies, Inc. v. United Therapeutics Corporation*, Petition for *Inter Partes Review* of U. S. Patent 10,716,793 B2, October 20, 2021, on behalf of Liquidia Technologies, Inc.; (23) *EcoFactor, Inc. v. Google, Inc.*, Western District of Texas, 6:20-cv-00075 (ADA), 6:20-0078-ADA, and 6:20-cv-00080 ADA, October 27, 2021, on behalf of Google, Inc.; (24) *Liquidia Technologies, Inc. v. United Therapeutics Corporation*, Petition for *Inter Partes Review* of U. S. Patent 10,716,793 B2, March 11, 2022, on behalf of Liquidia Technologies, Inc.; (25) *Juniper Networks, Inc. v. Swarm Technology LLC*, Petition for *Inter*

Partes Review of U. S. Patent 9,852,004, May 5, 2022, on behalf of Juniper Networks, Inc.; (26) *ParkerVision, Inc. v. Intel Corporation*, Western District of Texas, 6:20-cv-108 (ADA), October 26, 2022, on behalf of the Intel Corporation; and, (27) *CommScope v. TQ Delta*, Petition for *Inter Partes Review* of U. S. Patents 9,094,348 and 10,833,809, February 16, 2023, on behalf of CommScope.

10. My full curriculum vitae is attached as EX-1032.

III. PRELIMINARIES

A. Scope of Declaration and Legal Standards

11. I am not an attorney and will not offer opinions on the law. I am, however, rendering my expert opinion on the authenticity of the documents referenced herein and on when and how each of these documents was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising ordinary diligence, could have located the documents prior to May 19, 2009.

12. I am informed by counsel that a printed publication qualifies as publicly accessible as of the date it was disseminated or otherwise made available such that a person interested in and ordinarily skilled in the relevant subject matter could locate it through the exercise of ordinary diligence.

13. While I understand that the determination of public accessibility under

the foregoing standard rests on a case-by-case analysis of the facts particular to an individual publication, I also understand that a printed publication is rendered “publicly accessible” if it is cataloged and indexed by a library such that a person interested in the relevant subject matter could locate it (*i.e.*, I understand that cataloging and indexing by a library is sufficient, though there are other ways that a printed publication may qualify as publicly accessible). One manner of sufficient indexing is indexing according to subject matter category. I understand that the cataloging and indexing by a single library of a single instance of a particular printed publication is sufficient, even if the single library is in a foreign country. I understand that, even if access to a library is restricted, a printed publication that has been cataloged and indexed therein is publicly accessible so long as a presumption is raised that the portion of the public concerned with the relevant subject matter would know of the printed publication. I also understand that the cataloging and indexing of information that would guide a person interested in the relevant subject matter to the printed publication, such as the cataloging and indexing of an abstract for the printed publication, is sufficient to render the printed publication publicly accessible.

14. I understand that routine business practices, such as general library cataloging and indexing practices, can be used to establish an approximate date on which a printed publication became publicly accessible.

B. Persons of ordinary skill in the art.

15. I am told by counsel that the subject matter of this proceeding relates to the design and structure of an integrated circuit inductor.

16. I have been informed by counsel that a “person of ordinary skill in the art at the time of the invention” (“POSITA”) is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the inventions. This hypothetical person is also a person of ordinary creativity, capable of understanding the scientific principles applicable to the pertinent field.

17. I am told by counsel that persons of ordinary skill in this subject matter or art would have had (a) a B.S. in electrical engineering and 3-4 years of integrated circuit design experience; or (b) a M.S. in electrical engineering and 1-2 years of integrated circuit design experience; or (c) a Ph.D. in electrical engineering. I have been further informed by counsel that a person of ordinary skill in the art would have been familiar with and able to understand the information known in the art relating to these fields, including the publication discussed in this declaration.

18. It is my opinion that such a person would have been engaged in research, learning, study, and practice in the field, and formal instruction so that bibliographic resources relevant to his or her research would be familiar. Prior to May 19, 2009, such a person would have had access to a vast array of long-

established print resources in electrical engineering circuit design as well as to a rich set of online resources providing indexing information, abstracts, and full text services.

IV. LIBRARY PROFESSIONAL PRACTICES

19. In preparing this declaration, I used authoritative databases, such as the OCLC bibliographic database, the Library of Congress Online Catalog, and the Library of Congress Subject Authorities, to confirm citation details of the various publications discussed. Unless I note otherwise below in reference to a specific serial publication, it is my expert opinion that this standard protocol was followed for the serial publication discussed below.

20. *Indexing.* A researcher may discover material relevant to his or her topic in a variety of ways. One common means of discovery is to search for relevant information in an index of periodicals and other publications. Having found relevant material, the researcher will then normally obtain it online, look for it in libraries, or purchase it from the publisher, a bookstore, a document delivery service, or other provider. Sometimes, the date of a document's public accessibility will involve both indexing and library date information. However, date information for indexing entries is often unavailable. This is especially true for online indices.

21. Indexing services use a wide variety of controlled vocabularies to provide subject access and other means of discovering the content of documents.

The Library of Congress Subject Authorities includes standard forms of terms and cross references that are included in bibliographic records. Subject headings are terms that an individual seeking a document regardless of format can enter in the search bar of the online catalog. Subjects also connect an authenticated term (one included in the Library of Congress subject headings list) with related, broader, and narrower terms. The formats in which these access terms are presented vary from service to service.

22. Online indexing services commonly provide bibliographic information, abstracts, and full-text copies of the indexed publications, along with a list of the documents cited in the indexed publication. These services also often provide lists of publications that cite a given document. A citation of a document is evidence that the document was publicly available and in use by researchers no later than the publication date of the citing document. Prominent indexing services include the *IEEE Xplore* database, the *ACM Digital Library*, and the digital repositories *ResearchGate* and *Semantic Scholar*.

V. LIBRARY CATALOGING PRACTICES

23. I am fully familiar with the library cataloging standard known as the MARC standard, which is an industry-wide standard method of storing and

organizing library catalog information.¹ MARC was first developed in the 1960's by the Library of Congress. A MARC-compatible library is one that has a catalog consisting of individual MARC records for each of its items. Today, MARC is the primary communications protocol for the transfer and storage of bibliographic metadata in libraries.²

24. Since at least the early 1970s and continuing to the present day, MARC has been the primary communications protocol for the transfer and storage of bibliographic metadata in libraries.³ As explained by the Library of Congress:

¹ The full text of the standard is available from the Library of Congress at <http://www.loc.gov/marc/bibliographic/> (last visited March 2, 2023).

² Almost every major library in the world is MARC-compatible. *See, e.g., MARC Frequently Asked Questions (FAQ)*, Library of Congress, <https://www.loc.gov/marc/faq.html> (last visited March 2, 2023) (“MARC is the acronym for Machine-Readable Cataloging. It defines a data format that emerged from a Library of Congress-led initiative that began nearly fifty years ago. It provides the mechanism by which computers exchange, use, and interpret bibliographic information, and its data elements make up the foundation of most library catalogs used today.”). MARC is the ANSI/NISO Z39.2-1994 (reaffirmed 2016) standard for Information Interchange Format.

³ A complete history of the development of MARC can be found in *MARC: Its History and Implications* by Henrietta D. Avram (Washington, DC: Library of Congress, 1975) and available online from the Hathi Trust

You could devise your own method of organizing the bibliographic information, but you would be isolating your library, limiting its options, and creating much more work for yourself. Using the MARC standard prevents duplication of work and allows libraries to better share bibliographic resources. Choosing to use MARC enables libraries to acquire cataloging data that is predictable and reliable. If a library were to develop a “home-grown” system that did not use MARC records, it would not be taking advantage of an industry-wide standard whose primary purpose is to foster communication of information.

Using the MARC standard also enables libraries to make use of commercially available library automation systems to manage library operations. Many systems are available for libraries of all sizes and are designed to work with the MARC format. Systems are maintained and improved by the vendor so that libraries can benefit from the latest advances in computer technology. The MARC standard also allows libraries to replace one system with another with the assurance that their data will still be compatible. *Why Is a MARC Record Necessary?* LIBRARY OF CONGRESS.⁴

25. Thus, almost every major library in the world is MARC-compatible.

*See, e.g., MARC Frequently Asked Questions (FAQ), LIBRARY OF CONGRESS.*⁵

(“MARC is the acronym for MACHine-Readable Cataloging. It defines a data format that emerged from a Library of Congress-led initiative that began fifty years ago. It provides the mechanism by which computers exchange, use, and interpret bibliographic information, and its data elements make up the foundation of most

(<https://babel.hathitrust.org/cgi/pt?id=mdp.39015034388556;view=1up;seq=1>; last visited March 2, 2023).

⁴ <http://www.loc.gov/marc/umb/um01to06.html#part2>

⁵ <https://www.loc.gov/marc/faq.html>

library catalogs used today.”). MARC is the ANSI/NISO Z39.2-1994 standard (reaffirmed in 2016) for Information Interchange Format. The full text of the standard is available from the Library of Congress.⁶

26. A MARC record comprises several fields, each of which contains specific data about the work. Each field is identified by a standardized, unique, three-digit code corresponding to the type of data that follow. For example, a work’s title is recorded in Field 245; the primary author of the work is transcribed in Field 100; an item’s International Standard Book Number (“ISBN”) consisting of ten or thirteen digits is transcribed in Field 020; an item’s International Standard Serial Number (“ISSN”) is transcribed in Field 022; the Library of Congress classification notation is recorded in Field 050; and the publication date is recorded in Field 260 under the subfield “c.” If a work is a periodical, then its publication frequency is recorded in Field 310, and the publication dates (e.g., the first and last publication) are recorded in Field 362, which is also referred to as the enumeration/chronology field.⁷

27. The library that created the record is recorded in Field 040 in subfield “a” with a unique library code. When viewing the MARC record online via Online Computer Library Center’s (“OCLC”) bibliographic database, hovering over this

⁶ <http://www.loc.gov/marc/bibliographic/>

⁷ <http://www.loc.gov/marc/bibliographic/bd3xx.html>

code with the mouse reveals the full name of the library. I used this method of “mousing over” the library codes in the OCLC database to identify the originating library for the MARC records discussed in this declaration. Where this “mouse over” option was not available, I consulted the Directory of OCLC Libraries to identify the institution that created the MARC record.⁸

28. MARC records also include several fields that include subject matter classification information. An overview of MARC record fields is available through the Library of Congress.⁹ For example, 6XX fields are termed “Subject Access Fields.”¹⁰ Among these, for example, is the 650 field; this is the “Subject Added Entry – Topical Term” field.¹¹ The 650 field is a “[s]ubject added entry in which the entry element is a topical term.” These entries “are assigned to a bibliographic record to provide access according to generally accepted thesaurus-building rules (e.g., *Library of Congress Subject Headings* (LCSH), *Medical Subject Headings* (MeSH)).” *Id.* Further, MARC records include call numbers, which themselves include a classification number. For example, the 050 field is the

⁸ <https://www.oclc.org/en/contacts/libraries.html>

⁹ <http://www.loc.gov/marc/bibliographic/>

¹⁰ <http://www.loc.gov/marc/bibliographic/bd6xx.html>

¹¹ <http://www.loc.gov/marc/bibliographic/bd650.html>

“Library of Congress Call Number.”¹² A defined portion of the Library of Congress Call (LCC) Number is the classification number, and “source of the classification number is *Library of Congress Classification* and the *LC Classification-Additions and Changes*.” Thus, included in the 050 field is a subject matter classification. Further, the 082 field is the “Dewey Decimal Call Number.”¹³ A defined portion of the Dewey Decimal Call (DDC) Number is the classification number, and “source of the classification number is the *Dewey Decimal Classification and Relative Index*.” Thus, included in the 082 field is a subject matter classification. Each item in a library has a single classification number. A library selects a classification scheme (e.g., the Library of Congress classification scheme just described or a similar scheme such as the Dewey Decimal classification scheme) and uses it consistently. When the Library of Congress assigns the LCC classification number, it appears as part of the 050 field. When the Library of Congress assigns the DDC classification number, it appears as part of the 082 field. If a local library assigns the classification number, it appears in a 090 field. In either scenario, the MARC record includes a classification number that represents a subject matter classification.

29. The OCLC was created “to establish, maintain and operate a

¹² <http://www.loc.gov/marc/bibliographic/bd050.html>

¹³ <http://www.loc.gov/marc/bibliographic/bd082.html>

computerized library network and to promote the evolution of library use, of libraries themselves, and of librarianship, and to provide processes and products for the benefit of library users and libraries, including such objectives as increasing availability of library resources to individual library patrons and reducing the rate of rise of library per-unit costs, all for the fundamental public purpose of furthering ease of access to and use of the ever-expanding body of worldwide scientific, literary and educational knowledge and information.”¹⁴ Among other services, OCLC and its members are responsible for maintaining the WorldCat database (<http://www.worldcat.org/>), used by independent and institutional libraries throughout the world.

30. OCLC also provides its members online access to MARC records through its OCLC bibliographic database. When an OCLC member institution acquires a work, it creates a MARC record for this work in its computer catalog system in the ordinary course of its business. MARC records created at the Library of Congress are tape-loaded into the OCLC database through a subscription to MARC Distribution Services daily or weekly. Once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library

¹⁴ Third Article, Amended Articles of Incorporation of OCLC Online Computer Library Center, Incorporated (available at <https://www.oclc.org/content/dam/oclc/membership/articles-of-incorporation.pdf>).

of Congress, the MARC record is then made available to any other OCLC members online, and therefore made available to the public. Accordingly, once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress or another library anywhere in the world, any publication corresponding to the MARC record has been cataloged and indexed according to its subject matter such that a person interested in that subject matter could, with reasonable diligence, locate and access the publication through any library with access to the OCLC bibliographic database or through the Library of Congress.

31. When an OCLC member institution creates a new MARC record, OCLC automatically supplies the date of creation for that record. The date of creation for the MARC record appears in the fixed Field (008), characters 00 through 05. The MARC record creation date reflects the date on which, or shortly after which, the item was first acquired or cataloged. Initially, Field 005 of the MARC record is automatically populated with the date the MARC record was created in year, month, day format (YYYYMMDD) (some of the newer library catalog systems also include hour, minute, second (HHMMSS)). Thereafter, the library's computer system may automatically update the date in Field 005 every time the library updates the MARC record (*e.g.*, to reflect that an item has been moved to a different shelving location within the library). Field 005 is visible when

viewing a MARC record via an appropriate computerized interface, but when a MARC record is printed to hardcopy, no “005” label appears. The initial Field 005 date (*i.e.*, the date the MARC record was created) does appear, however, next to the label “Entered.”¹⁵ The date upon which the most recent update to Field 005 occurred also appears, next to the label “Replaced.” Thus, when an item’s MARC record has been printed to hardcopy—as is the case with the exhibits to this declaration—the date reflected next to the label “Entered” is necessarily on or after the date the library first cataloged and indexed the underlying item.

32. Once one library has cataloged and indexed a publication by creating a MARC record for that publication, other libraries that receive the publication do not create additional MARC records—the other libraries instead rely on the original MARC record. They may update or revise the MARC record to ensure accuracy, but they do not replace or duplicate it. This practice does more than save libraries from duplicating labor. It also enhances the accuracy of MARC records. Further, it allows librarians around the world to know that a particular MARC record is authoritative (in contrast, a hypothetical system wherein duplicative records were created would result in confusion as to which record is authoritative).

¹⁵ Field 005 is visible when viewing a MARC record via an appropriate computerized interface. But when a MARC record is printed directly to hardcopy from the OCLC database, the “005” label is not shown. The date in the 005 field instead appears next to the label “Replaced.”

33. Catalogers can create MARC records for all types of print, online, and digital resources. The date of creation of the MARC record by a cataloger at an OCLC member institution reflects when the underlying item is accessible to the public. Upwards of two-thirds to three-quarters of book sales to libraries come from a jobber or wholesaler for online and print resources. These resellers make it their business to provide books to their customers as fast as possible, often providing turnaround times of only a single day after publication. Libraries purchase a significant portion of the balance of their books directly from publishers themselves, which provide delivery on a similarly expedited schedule. In general, libraries make these purchases throughout the year as the books are published and shelve the books as soon thereafter as possible to make the books available to their patrons. Thus, books are generally available at libraries across the country within just a few days of publication.

34. *Journals.* MARC records that cover serial publications include both serially-published monographs and journals. OCLC hosts MARC records for more than 320 million serial publications. Serial publications are those publications that have the same collective title but are intended to be continued indefinitely with enumeration such as a volume or issue number (*e.g.*, magazines, journals, etc.). In the OCLC bibliographic database, the first issue of the serial publication is typically cataloged (*i.e.*, a corresponding MARC record is created), but the date is

left open-ended with the use of a punctuation mark such as a dash. OCLC serial publication MARC records represent the entire run of the serial title. With knowledge of the first issue published, future issues can be predicted based on the information provided in the MARC record, for example in field 362. In my extensive professional experience, is it highly unusual for a library to stop collecting and shelving a serial publication prior to the end of its publication run. If a subscription to a serial publication ends its run or is cancelled before the end of its run, the library will denote that it has stopped receiving new volumes by filling in the end date in the MARC record.

35. The handling of printed journal subscriptions is shown on the cover or the first few pages of individual issues. As was the best practice among libraries, issues arrived at a central facility and were immediately received, verified as part of a subscription, checked in, and stamped or labeled with the institution's name and date. Determining that the issue was part of the library subscription ensured that the entire set of publications for the year had been received so that they could be professionally bound and retained. This process also verified that all of the published issues arrived so that the library staff did not have to request or claim an issue that did not arrive as expected. In large public libraries with branches and multi-campus libraries within academic institutions, the journals were sorted and delivered to the subscribing unit. The new issue was placed in the public area; the

older issue was stored so that it remained available.

36. The foregoing process has been standard library practice longer than I have been working in the profession. I first learned the steps in the process in the late 1970s and later supervised it. Although the checking in process has become automated and now links electronically to holdings records for the MARC record for each serial title, the manual placement of a stamp or label and placing the issue in a public area has not changed for 50 years. Unless I note otherwise below in reference to a specific serial publication, it is my expert opinion that this standard protocol was followed for the serial publication discussed below.

VI. PUBLICATION 1: “*Spiral Inductors on Silicon, Status and Trends*” by Joachim N. Burghartz. Exhibit 1 (“Burghartz 1998”)

37. Attached hereto as Exhibit 1 is a copy of the journal article “Spiral Inductors on Silicon, Status and Trends” by Joachim N. Burghartz (hereafter “Burghartz 1998”). The Burghartz 1998 article was published in Volume 8, Number 6 of the *International Journal of RF and Microwave Computer-Aided Engineering* and was found in the New York Public Library. The Burghartz 1998 article appears beginning on page 422 of this issue dated November 1998. Exhibit 1 is a true and correct copy of the Burghartz 1998 article (pages 422-432). Specifically, the text of the article is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. The Burghartz 1998 article is also

available from the publisher, Wiley¹⁶ and through the digital repository *Semantic Scholar*.¹⁷ Exhibit 1 was found within the custody of a library – a place where an authentic copy of this journal would likely be. Exhibit 1 is a true and correct copy in a condition that creates no suspicion about its authenticity.

38. Attached hereto as Attachment 1A is a true and correct copy of the metadata record for the *International Journal of RF and Microwave Computer-Aided Engineering* in the New York Public Library. The library ownership is indicated by the presence of the library's name at the top of the screen. I personally identified and retrieved the MARC record that is Attachment 1A.

39. Based on finding a print copy of Exhibit 1 in the New York Public Library and metadata record in its online library catalog attached as Attachment 1A, it is my opinion that the Burghartz 1998 article published in the *International Journal of RF and Microwave Computer-Aided Engineering* was publicly available on or shortly after December 7, 1998, as indicated by the publisher's website. Attachment 1A also shows that Exhibit 1 was catalogued with two descriptor terms

¹⁶ <https://onlinelibrary.wiley.com/doi/abs/10.1002/%28SICI%291099-047X%28199811%298%3A6%3C422%3A%3AAID-MMCE3%3E3.0.CO%3B2-K>

¹⁷ <https://www.semanticscholar.org/paper/Spiral-inductors-on-silicon%E2%80%94status-and-trends-Burghartz/86d495b88eb7a1207ad3bfl1ea0fd11f9344e158>

in the “additional suggestions” section reading “Microwave devices \$x Computer-aided design \$v Periodicals” (see Attachment 1B, Library of Congress subject heading sh85084958, Attachment 1C, Library of Congress subject heading sh85029476, and Attachment 1D, Library of Congress subject heading sh85099890) and “Computer-aided engineering \$v Periodicals” (see Attachment 1E, Library of Congress subject heading sh89002586 and Attachment 1D, Library of Congress subject heading sh85099890) in the 650 fields.

40. As noted in the holdings information (362 field), the New York Public Library has received the *International Journal of RF and Microwave Computer-Aided Engineering* since January 1998 and continues to receive the digital version of the publication.¹⁸ The print version ceased in December 2013. In view of the MARC record for Exhibit 1, the Burghartz 1998 article was publicly available on or shortly after December 7, 1998, because the serial title had been received, cataloged, and indexed in the new York Public Library and made part of its online catalog database.

41. Attached hereto as Attachment 1F is a true and correct copy of the MARC record for the *International Journal of RF and Microwave Computer-*

¹⁸ The publication was originally titled the *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering* (January 1991-November 1997) and adopted the current title, *International Journal of RF and Microwave Computer-Aided Engineering* in January 1998.

Aided Engineering obtained from the OCLC bibliographic database. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 1F, that library code is “NSD,” which means that the MARC record for this serial was cataloged as part of the National Serials Data Program at the Library of Congress. As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger in the Library of Congress created OCLC record number 37784096 on October 15, 1997, as shown in the “Entered” field (“19971015”). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 1F occurred on February 1, 2019, as shown in the “Replaced” field (“20190201”). I personally identified and retrieved the MARC record that is Attachment 1F. The “BLvl” entry in Attachment 1F is “s,” which indicates that the *International Journal of RF and Microwave Computer-Aided Engineering* is a serial publication. Field 310 of Attachment 1F reads “Bimonthly.” Accordingly, the MARC record for Exhibit 1 corresponds to the *International Journal of RF and Microwave Computer-Aided Engineering* from the time the serial title adopted the current title and includes the date of the Burghartz 1998 article.

42. Attachment 1F includes an entry in field 050 (“TK7876 \$b .I547”)—as described above, a subject matter classification number consistent with the

Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.381/3”), a subject matter consistent with the Dewey Decimal classification system. Attachment 1F further includes two descriptor terms reading “Microwave devices \$x Computer-aided design \$v Periodicals” (see Attachment 1B, Library of Congress subject heading sh85084958, Attachment 1C, Library of Congress subject heading sh85029476, and Attachment 1D, Library of Congress subject heading sh85099890) and “Computer-aided engineering \$v Periodicals” (see Attachment 1E, Library of Congress subject heading sh89002586 and Attachment 1D, Library of Congress subject heading sh85099890) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 1F was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. As of October 15, 1997, the MARC record attached hereto as Attachment 1F was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that subscribed to the serial, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

43. Attachment 1F indicates that the *International Journal of RF and*

Microwave Computer-Aided Engineering as cataloged in the Library of Congress is currently available from 46 libraries. In view of the above, this issue of the *International Journal of RF and Microwave Computer-Aided Engineering* was publicly available on or shortly after December 7, 1998, because by that date it had been cataloged and indexed in the Library of Congress, made part of the OCLC bibliographic database, and received in the New York Public Library. For these reasons, it is my opinion that Exhibit 1 was published and accessible to the public on or shortly after December 7, 1998.

VII. PUBLICATION 2: *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs* by Ali M. Niknejad and Robert G. Meyer. Exhibit 2 (“Niknejad 2000”)

44. Exhibit 2 attached hereto is a copy of the title page, copyright page, table of contents, and excerpts from the book titled *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs* by Ali M. Niknejad and Robert G. Meyer (hereafter “Niknejad 2000”) and issued by Kluwer Academic Publishers with a 2000 copyright date. The book is part of The Springer International Series in Engineering and Computer Science (SECS, volume 586). The following excerpts are included in Exhibit 2: Chapter 1, “Introduction” (pages 3-9); Chapter 2, “Problem Description” (pages 11-37); Chapter 5, “Inductance Calculations” (pages 59-73); and, Chapter 8, “Experimental Study” (pages 109-122). Exhibit 2 is a true and correct copy from the book titled *Design, Simulation*

and Applications of Inductors and Transformers for Si RF ICs held by The Ohio State University Libraries (Columbus, Ohio). The excerpts from Exhibit 2 are complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit 2 is a true and correct copy in a condition that creates no suspicion about its authenticity.

45. Attachment 2A is a true and correct copy of the MARC record for this monograph from the online catalog in The Ohio State University Libraries. The library ownership is indicated by the presence of the library's code (OSU) in field 049. I personally identified and retrieved the library catalog record which is Attachment 2A.

46. Based on finding a print copy of the book titled *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs* in The Ohio State University Libraries and MARC record in its online library catalog attached as Attachment 2A, it is my opinion that the Niknejad 2000 book was publicly available on November 20, 2000, as indicated in field 971 ("20001120"). The International Standard Book Number (ISBN) on Exhibit 2 (0-7923-7986-1) matches the ISBN on page 2 of Exhibit 1002. Therefore, Exhibit 2 is the same book as the one that the cataloger in The Ohio State University Libraries used to create the metadata record that is Attachment 2A.

47. Attached hereto as Attachment 2B is a true and correct copy of the MARC record for the book titled *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs* from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 2B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 2B that library code is “DLC,” which means that the MARC record for this book was created in the Library of Congress as part of the Cataloging in Publication (CIP) Program.¹⁹ A cataloger prepares basic information about the forthcoming book which is included on the verso of the title page (also called the copyright page). The information is provided to save time needed for the cataloging process at the library after the book is purchased. The CIP data includes the author (field 100), title and subtitle (field 245), ISBN (field 022), suggested subject headings (field 650), classification numbers for the Library of Congress classification number (field 050), and the Dewey Decimal classification number (field 082). These data elements are included in the MARC record that the Library of Congress contributes to the OCLC bibliographic database. The MARC record in the Library of Congress online catalog indicates

¹⁹ <https://www.loc.gov/publish/cip/about/>

that the Niknejad 2000 book was publicly available on April 27, 2001.²⁰ The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent enhancement to Attachment 2B occurred on November 1, 2022, as shown in the “Replaced” field (“20221101”). I personally identified and retrieved the MARC record that is Attachment 2B.

48. Attachment 2B further includes an entry in field 050 (“TK7872.I63 \$b N55 2000”) as described above, this includes a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.381”) as described above, this includes a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 2B further includes four descriptor terms reading “Electric inductors \$x Computer-aided design” (see Attachment 2C, Library of Congress subject heading sh85041716 and Attachment 1C, Library of Congress subject heading sh85029476), “Electronic transformers \$x Computer-aided design” (see Attachment 2D, Library of Congress subject heading sh85042378 and Attachment 1C, Library of Congress subject heading sh85029476), “Silicon-on-insulator technology” (see Attachment 2E, Library of

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<https://catalog.loc.gov/vwebv/staffView?searchId=22596&recPointer=4&recCount=25&bibId=12127424>

Congress subject heading sh89003063), and “Microwave integrated circuits \$x Computer-aided design” (see Attachment 2F, Library of Congress subject heading sh85084963 and Attachment 1C, Library of Congress subject heading sh85029476) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 2B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of August 2, 2000, the MARC record attached hereto as Attachment 2B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that added this book to its collection, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

49. Further supporting my opinion that Exhibit 2 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs* was registered with the U. S. Copyright Office as item TX0005307708 on November 22, 2000, and indicated a publication date of October 13, 2000 (see Attachment 2G, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other

tools to locate this book.

50. Attachment 2B indicates that the book titled *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs* as cataloged at the Library of Congress is currently available from 114 libraries. In view of above, the book titled *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs* was publicly available on or shortly October 13, 2000, because by that date it had been cataloged and indexed in the Library of Congress and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit 1002 was published and accessible to the public on or shortly after October 13, 2000.

VIII. PUBLICATION 3: *Electromagnetics for High-Speed Analog and Digital Communication Circuits* by Ali M. Niknejad. Exhibit 3 (“Niknejad 2007”)

51. Exhibit 3 attached hereto is a copy of the title page, copyright page, table of contents, and excerpts from the book titled *Electromagnetics for High-Speed Analog and Digital Communication Circuits* by Ali M. Niknejad (hereafter “Niknejad 2007”) and issued by Cambridge University Press with a 2007 copyright date. Exhibit 3 is a true and correct copy from the book titled *Electromagnetics for High-Speed Analog and Digital Communication Circuits* held by the Shanghai Library (Shanghai, China). The following excerpts are included in Exhibit 3: Chapter 1, “Introduction” (pages 1-17); Chapter 5, “Inductance” (pages 96-136);

and Chapter 6, “Passive Device Design and Layout” (pages 137-167). The excerpts in Exhibit 3 are complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit 3 is a true and correct copy in a condition that creates no suspicion about its authenticity.

52. Attachment 3A is a true and correct copy of the metadata record for this monograph from the online catalog in the Shanghai Library. The library ownership is indicated by the presence of the library’s code (uwmadisondb) in the third field 035. I personally identified and retrieved the library catalog record which is Attachment 3A.

53. Based on finding a print copy of the book titled *Electromagnetics for High-Speed Analog and Digital Communication Circuits* in the Shanghai Library and metadata record in its online library catalog attached as Attachment 3A, it is my opinion that the Niknejad 2007 book was publicly available. The International Standard Book Number (ISBN) on Exhibit 1003 (0-521-85350-8) matches the ISBN on page 2 of Exhibit 3. Therefore, Exhibit 3 is the same book as the one that the cataloger in the Shanghai Library used to create the metadata record that is Attachment 3A.

54. Attached hereto as Attachment 3B is a true and correct copy of the MARC record for the book titled *Electromagnetics for High-Speed Analog and*

Digital Communication Circuits from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 3B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 3B that library code is “UKM,” which means that the MARC record for this book was created in the British Library. The MARC record in the British Library online catalog indicates that the Niknejad 2007 book was publicly available on May 8, 2006.²¹ The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent enhancement to Attachment 3B occurred on September 18, 2022, as shown in the “Replaced” field (“20220918”). I personally identified and retrieved the MARC record that is Attachment 3B.

55. Attachment 3B further includes an entry in field 050 (“TK7867 \$b .N54 2007”) as described above, this includes a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.3815”) as described above, this includes a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 3B further includes six

²¹

http://primocat.bl.uk/F/?func=direct&local_base=PRIMO&doc_number=013552544&format=001&con_lng=eng

descriptor terms reading “Electronic circuits” (see Attachment 3C, Library of Congress subject heading sh85042279), “Electromagnetic compatibility” (see Attachment 3D, Library of Congress subject heading sh85042167), “Digital integrated circuits” (see Attachment 3E, Library of Congress subject heading sh85037979), “Linear integrated circuits” (see Attachment 3F, Library of Congress subject heading sh85077176), “Electromagnetism” (see Attachment 3G, Library of Congress subject heading sh85042184) and “Very high speed integrated circuits” (see Attachment 3H, Library of Congress subject heading sh85142925) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 3B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of May 8, 2006, the MARC record attached hereto as Attachment 3B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that added this book to its collection, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

56. Attachment 3B indicates that the book titled *Electromagnetics for High-Speed Analog and Digital Communication Circuits* as cataloged at the British Library is currently available from 225 libraries. In view of above, the book titled

Electromagnetics for High-Speed Analog and Digital Communication Circuits was publicly available on or shortly May 8, 2006, because by that date it had been cataloged and indexed in the British Library and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit 1003 was published and accessible to the public on or shortly after May 8, 2006.

IX. PUBLICATION 4: “*On the Design of RF Spiral Inductors on Silicon*” by Joachim N. Burghartz and Behzad Rejaei. Exhibit 4 (“Burghartz 2003”)

57. Attached hereto as Exhibit 4 is a copy of the journal article “On the Design of RF Spiral Inductors on Silicon” by Joachim N. Burghartz and Behzad Rejaei (hereafter “Burghartz 2003”). The Burghartz 2003 article was published in Volume 50, Number 3 of the journal *IEEE Transactions on Electron Devices* and was found in the Linda Hall of Science, Engineering & Technology (Kansas City, Missouri). The Burghartz 2003 article appears beginning on page 718 of this issue dated March 2003. Exhibit 4 is a true and correct copy of the Burghartz 2003 article (pages 718-729). Specifically, the text of the article is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. The Burghartz 2003 article is also available in the *IEEE Xplore Database*²² and through the digital

²² <https://ieeexplore.ieee.org/document/1202600>

repositories *ResearchGate*²³ and *Semantic Scholar*.²⁴ Exhibit 4 was found within the custody of a library – a place where an authentic copy of this journal would likely be. Exhibit 4 is a true and correct copy in a condition that creates no suspicion about its authenticity.

58. Attached hereto as Attachment 4A is a true and correct copy of the MARC record for the journal *IEEE Transactions on Electron Devices* in the Linda Hall Library of Science, Engineering & Technology. The library ownership is indicated by the presence of the library's code (LHL) in field 049. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 4A occurred on October 30, 2019, as shown in field 005 ("20191030"). I personally identified and retrieved the MARC record that is Attachment 4A.

59. Based on finding a print copy of Exhibit 1004 in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 4A, it is my opinion that the Burghartz 2003 article published in the journal *IEEE Transactions on Electron Devices* was

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https://www.researchgate.net/publication/3065153_On_the_design_of_RF_spiral_inductors_on_silicon

²⁴ <https://www.semanticscholar.org/paper/On-the-design-of-RF-spiral-inductors-on-silicon-Burghartz-Rejaei/131554851965ccbbe32fa5d0420accb94a2d87ba>

publicly available on or shortly after June 16, 2003, as shown on the cover. This date stamp has the general appearance of date stamps that libraries have long affixed to periodicals to show when an issue was received, verified, and checked in. Attachment 4A also shows that Exhibit 4 was catalogued with a descriptor term reading “Electronic apparatus and appliances \$v Periodicals” (see Attachment 4B, Library of Congress subject heading sh2008102923) in the 650 field.

60. As noted in the holdings information (362 field), the Linda Hall Library of Science, Engineering & Technology has received the journal *IEEE Transactions on Electron Devices* since January 1963 and continues to receive the publication.²⁵ In view of the MARC record for Exhibit 1004, the Burghartz 2003 article was publicly on or shortly after June 16, 2003, because the serial title had been received, cataloged, and indexed in the Linda Hall Library of Science, Engineering & Technology and made part of its online catalog database.

61. Attached hereto as Attachment 4C is a true and correct copy of the MARC record for the journal *IEEE Transactions on Electron Devices* obtained from the OCLC bibliographic database. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For

²⁵ The publication was originally titled *IRE Transactions on Electron Devices* (January 1955-December 1962) and adopted the current title, *IEEE Transactions on Electron Devices* in January 1963.

Attachment 4C, that library code is “NLM,” which means that the MARC record for this serial was cataloged in the National Library of Medicine (Bethesda, Maryland). As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger in the National Library of Medicine created OCLC record number 935837 on July 3, 1974, as shown in the “Entered” field (“19740703”). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 4C occurred on August 10, 2022, as shown in the “Replaced” field (“20220810”). I personally identified and retrieved the MARC record that is Attachment 4C. The “BLvl” entry in Attachment 4C is “s,” which indicates that the journal *IEEE Transactions on Electron Devices* is a serial publication. Field 310 of Attachment 4C reads “Monthly, \$c <1964-.” Accordingly, the MARC record for Exhibit 4 corresponds to the journal *IEEE Transactions on Electron Devices* from the time the serial title adopted the current title and includes the date of the Burghartz 2003 article.

62. Attachment 4C includes an entry in field 050 (“TK7870 \$b .I2”)—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 060 (“W1 I223E ”), a subject matter consistent with the National Library of Medicine classification system (analogous to the Dewey

Decimal classification system). Attachment 4C further includes a descriptor term reading “Electronic apparatus and appliances \$v Periodicals” (see Attachment 4B, Library of Congress subject heading sh2008102923) in the 650 field. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 4C was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 060 entry, and the field 650 entry. As of July 3, 1974, the MARC record attached hereto as Attachment 4C was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that subscribed to the serial, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

63. Attachment 4C indicates that the journal *IEEE Transactions on Electron Devices* as cataloged in the National Library of Medicine is currently available from 428 libraries. In view of the above, this issue of the journal *IEEE Transactions on Electron Devices* was publicly available on or shortly after June 16, 2003, because by that date it had been cataloged and indexed in the National Library of Medicine, made part of the OCLC bibliographic database, and received in the Linda Hall Library of Science, Engineering & Technology. For these reasons, it is my opinion that Exhibit 4 was published and accessible to the public

on or shortly after June 16, 2003.

X. PUBLICATION 5: “Design of Multiple-Metal Stacked Inductors Incorporating an Extended Physical Model” by Olive H. Murphy, Kevin G. McCarthy, Christophe J. P. Delabie, Aidan C. Murphy, Member, and Patrick J. Murphy. Exhibit 5 (“Murphy”)

64. Attached hereto as Exhibit 5 is a copy of the journal article “Design of Multiple-Metal Stacked Inductors Incorporating an Extended Physical Model” by Olive H. Murphy, Kevin G. McCarthy, Christophe J. P. Delabie, Aidan C. Murphy, Member, and Patrick J. Murphy (hereafter “Murphy”). The Murphy article was published in Volume 53, Number 6 of the journal *IEEE Transactions on Microwave Theory and Techniques* and was found in the Linda Hall of Science, Engineering & Technology (Kansas City, Missouri). The Murphy article appears beginning on page 2063 of this issue dated July 2005. Exhibit 5 is a true and correct copy of the Murphy article (pages 2063-2072). Specifically, the text of the article is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. The Murphy article is also available in the *IEEE Xplore Database*²⁶ and through the digital repository *ResearchGate*.²⁷ Exhibit 5 was found within the custody of a library – a place where an authentic copy of this journal would likely

²⁶ <https://ieeexplore.ieee.org/document/1440724>

²⁷ https://www.researchgate.net/publication/3130955_Design_of_multiple-metal_stacked_inductors_incorporating_an_extended_physical_model

be. Exhibit 5 is a true and correct copy in a condition that creates no suspicion about its authenticity.

65. Attached hereto as Attachment 5A is a true and correct copy of the MARC record for the journal *IEEE Transactions on Microwave Theory and Techniques* in the Linda Hall Library of Science, Engineering & Technology. The library ownership is indicated by the presence of the library's code (LHL) in field 049. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 5A occurred on October 30, 2019, as shown in field 005 ("20191030"). I personally identified and retrieved the MARC record that is Attachment 5A.

66. Based on finding a print copy of Exhibit 5 in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 5A, it is my opinion that the Murphy article published in the journal *IEEE Transactions on Microwave Theory and Techniques* was publicly available on or shortly after June 20, 2005, as shown on the cover. This date stamp has the general appearance of date stamps that libraries have long affixed to periodicals to show when an issue was received, verified, and checked in. Attachment 5A also shows that Exhibit 5 was catalogued with a descriptor term reading "Microwaves \$v Periodicals" (see Attachment 5B, Library of Congress

subject heading sh2010101691) in the 650 field.

67. As noted in the holdings information (362 field), the Linda Hall Library of Science, Engineering & Technology has received the journal *IEEE Transactions on Microwave Theory and Techniques* since January 1963 and continues to receive the publication.²⁸ In view of the MARC record for Exhibit 5, the Murphy article was publicly on or shortly after June 20, 2005, because the serial title had been received, cataloged, and indexed in the Linda Hall Library of Science, Engineering & Technology and made part of its online catalog database.

68. Attached hereto as Attachment 5C is a true and correct copy of the MARC record for the journal *IEEE Transactions on Microwave Theory and Techniques* obtained from the OCLC bibliographic database. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 5C, that library code is “DLC,” which means that the MARC record for this serial was cataloged in the Library of Congress. As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger in the Library of Congress created OCLC record number 1752555 on November 1, 1975, as shown in the “Entered” field (“19751101”). The library continues to update this

²⁸ The publication was originally titled *IRE Transactions on Microwave Theory and Techniques* (March 1955-November 1962) and adopted the current title, *IEEE Transactions on Microwave Theory and Techniques* in January 1963.

MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 5C occurred on April 21, 2021, as shown in the “Replaced” field (“20210421”). I personally identified and retrieved the MARC record that is Attachment 5C. The “BLvl” entry in Attachment 5C is “s,” which indicates that the journal *IEEE Transactions on Microwave Theory and Techniques* is a serial publication. Field 310 of Attachment 5C reads “Monthly, \$c <1966-.” Accordingly, the MARC record for Exhibit 5 corresponds to the journal *IEEE Transactions on Microwave Theory and Techniques* from the time the serial title adopted the current title and includes the date of the Murphy article.

69. Attachment 5C includes an entry in field 050 (“TK7800 \$b .I23”)—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.381/3/05”), a subject matter consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 5C further includes a descriptor term reading “Microwaves \$v Periodicals” (see Attachment 5B, Library of Congress subject heading sh2010101691) in the 650 field. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 5C was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650

entry. As of November 1, 1975, the MARC record attached hereto as Attachment 5C was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that subscribed to the serial, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

70. Attachment 5C indicates that the journal *IEEE Transactions on Microwave Theory and Techniques* as cataloged in the Library of Congress is currently available from 387 libraries. In view of the above, this issue of the journal *IEEE Transactions on Microwave Theory and Techniques* was publicly available on or shortly after June 20, 2005, because by that date it had been cataloged and indexed in the Library of Congress, made part of the OCLC bibliographic database, and received in the Linda Hall Library of Science, Engineering & Technology. For these reasons, it is my opinion that Exhibit 5 was published and accessible to the public on or shortly after June 20, 2005.

XI. PUBLICATION 6: “Modeling and Analysis of Multilevel Spiral Inductors for RFICs” by R. D. Luta, Y. Hahm, A. Weisshaar, V. K. Tripathi, H. Wu, and N. Kanaglekar. Exhibit 6 (“Luta”)

71. Attached hereto as Exhibit 6 is a copy of a conference paper published in the four-volume set titled *1999 IEEE MTT-S International Microwave Symposium Digest* found in the Karl F. Wendt Engineering Library at the

University of Wisconsin – Madison. The conference paper titled “Modeling and Analysis of Multilevel Spiral Inductors for RFICs” by R. D. Luta, Y. Hahm, A. Weisshaar, V. K. Tripathi, H. Wu, and N. Kanaglekar (hereafter “Luta”) appears beginning on page 43 in volume 1. The 1999 IEEE MTT-S International Microwave Symposium was held on June 13-19, 1999, in Anaheim, California. Exhibit 6 is a true and correct copy of the Luta conference paper (volume 1, pages 43-46). I obtained this copy of the conference paper in the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison. Specifically, the text of the Luta conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit 6 was found within the custody of a library – a place where, if authentic, a copy of this conference proceedings volume would likely be. Exhibit 6 is a true and correct copy in a condition that creates no suspicion about authenticity.

72. The Luta conference paper is also available in the *IEEE Xplore* database²⁹ and the digital repository *Semantic Scholar*.³⁰

73. Attached hereto as Attachment 6A is a true and correct copy of the

²⁹ <https://ieeexplore.ieee.org/document/779421>

³⁰ <https://www.semanticscholar.org/paper/Modeling-and-analysis-of-multilevel-spiral-for-Lutz-Hahm/ef5e8a1c80f35695c3b623f93f2e199690283d5c>

MARC record for this conference proceedings volume from the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison online catalog. The library ownership is indicated by the presence of the library’s name at the top of the screen. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on August 7, 2021, as shown in field 005 (“20210807”). I personally identified and retrieved the library catalog record which is Attachment 6A.

74. Based on finding a print copy of Exhibit 6 in the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison and MARC record in its online library catalog attached as Attachment 6A, it is my opinion that the four-volume set titled *1999 IEEE MTT-S International Microwave Symposium Digest* was publicly available at the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison as of March 10, 1999, as shown in field 008 (“990310”).

75. Attached hereto as Attachment 6B is a true and correct copy of the MARC record for the four-volume set titled *1999 IEEE MTT-S International Microwave Symposium Digest* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 6B. As previously noted, the library that created the record is recorded in field 040 with a

unique library code. For Attachment 6B, that library code is “DLC,” which means that the MARC record for this conference proceedings volume was cataloged at the Library of Congress as part of the Cataloging in Publication (CIP) Program.³¹ As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger at the Library of Congress created OCLC record number 40939098 on September 10, 1998, as shown in the “Entered” field (“19980910”). A cataloger prepares basic information about the forthcoming book which may be included on the verso of the title page (also called the copyright page). The information is provided to save time needed for the cataloging process at the library after the book is purchased. The CIP data includes the author (field 100), title and subtitle (field 245), ISBN (field 022), suggested subject headings (field 650), classification numbers for the Library of Congress classification number (field 050), and the Dewey Decimal classification number (field 082). These data elements are included in the MARC record that the Library of Congress contributes to the OCLC bibliographic database. The MARC record in the Library of Congress online catalog indicates that the four-volume set titled *1999 IEEE MTT-S International Microwave*

³¹ <https://www.loc.gov/publish/cip/about/>

Symposium Digest was publicly available on March 7, 2000.³² The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent enhancement to Attachment 6B occurred on May 23, 2022, as shown in the “Replaced” field (“20220523”). I personally identified and retrieved the MARC record that is Attachment 6B.

76. Attachment 6B further includes an entry in field 050 (“TK5103.2 \$b .I34 1999”)—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.382”)—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 6B also shows that Exhibit 6 was catalogued with three descriptor terms reading “Wireless communication systems \$v Congresses” (see Attachment 6C, Library of Congress subject heading sh2008113541), “Microwave communication systems \$v Congresses” (see Attachment 6D, Library of Congress subject heading sh2010101688), and “Microwave circuits \$v Congresses” (Attachment 6E, Library of Congress subject heading sh85084954 and Attachment 6F, Library of Congress subject heading

³²

<https://catalog.loc.gov/vwebv/staffView?searchId=12649&recPointer=0&recCount=25&searchType=0&bibId=150634>

sh85031115) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 6B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of September 10, 1998, the MARC record attached hereto as Attachment 6B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the four-volume conference proceedings set, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

77. Further supporting my opinion that Exhibit 6 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the four-volume set titled *1999 IEEE MTT-S International Microwave Symposium Digest* was registered with the U. S. Copyright Office as item TX0005007560 on July 2, 1999, and indicated a publication date of June 13, 1999 (see Attachment 6G, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

78. Attachment 6B indicates that the four-volume set titled *1999 IEEE MTT-S International Microwave Symposium Digest* as cataloged at the Library of Congress is currently available from 48 libraries. In view of the above, the print

version of the four-volume set titled *1999 IEEE MTT-S International Microwave Symposium Digest* was publicly available on or shortly after March 7, 2000, because by that date it had been received, cataloged, and indexed in the Library of Congress and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit 6 was published and publicly accessible on or shortly after March 7, 2000.

XII. SUMMARY OF OPINIONS

79. In view of the foregoing, it is my opinion that the publication described above were publicly available no later than the corresponding date listed in the table below:

Exhibit	Publication	Publicly Available No Later Than
1	Burghartz, Joachim N. "Spiral Inductors on Silicon, Status and Trends." <i>International Journal of RF and Microwave Computer-Aided Engineering</i> , vol. 8, issue 6 (November 1998): 422-432.	December 7, 1998
2	Niknejad, Ali M., and Robert G. Meyer. <i>Design, Simulation and Applications of Inductors and Transformers for Si RF ICs</i> . The Springer International Series in Engineering and Computer Science (SECS, volume 586). Boston, MA: Kluwer Academic Publishers, ©2000.	October 13, 2000
3	Niknejad, Ali M. <i>Electromagnetics for High-Speed Analog and Digital Communication Circuits</i> . Cambridge; New York: Cambridge University Press, 2007.	May 8, 2006
4	Burghartz, Joachim N., and Behzad Rejaei. "On the Design of RF Spiral Inductors on Silicon." <i>IEEE Transactions on Electron Devices</i> , vol. 50,	June 16, 2003

Exhibit	Publication	Publicly Available No Later Than
	no. 3 (March 2003): 718-729.	
5	Murphy, Olive H., Kevin G. McCarthy, Christophe J. P. Delabie, Aidan C. Murphy, Member, and Patrick J. Murphy. "Design of Multiple-Metal Stacked Inductors Incorporating an Extended Physical Model." <i>IEEE Transactions on Microwave Theory and Techniques</i> , vol. 53, no. 6 (July 2005): 2063-2072.	June 20, 2005
6	Luta, R. D., Y. Hahm, A. Weisshaar, V. K. Tripathi, H. Wu, and N. Kanaglekar. "Modeling and Analysis of Multilevel Spiral Inductors for RFICs." <i>1999 IEEE MTT-S International Microwave Symposium Digest</i> (vol. 1, pp. 43-46). 4 vols. Piscataway, NJ: Institute of Electrical and Electronics Engineers, ©1999.	March 7, 2000

80. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: March 20, 2023



Sylvia D. Hall-Ellis, Ph.D.

Exhibit 1001

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Spiral Inductors on Silicon — Status and Trends (Invited Article)

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ABSTRACT: The status of the integration, the modeling, and the layout of spiral inductors on silicon substrates for rf circuits are reviewed. A summary of the current research activity in this field is presented. The possible inductor implementations are categorized either as conservative, following the silicon main stream, or as innovative approaches. It is concluded that the spiral inductor on silicon is a feasible device and finds extensive use in the design of future silicon-based rf circuits. © 1998 John Wiley & Sons, Inc. *Int J RF and Microwave CAE* 8: 422–432, 1998.

Keywords: inductor; spiral inductor; silicon; multilayer interconnects; RF; microwave; passive components

I. INTRODUCTION

The rapidly emerging commercial and consumer markets in wireless communications are raising a demand for integrated solutions in silicon technology [1]. One of the major technical challenges associated with the integration of a wireless RF transceiver on a single silicon chip is the development of integratable inductors. Inductors have not been part of main-stream silicon technology in the past, and useful quality-factors (Q) have not been demonstrated until a few years ago [2]. The optimization of this device is an important task, because the inductor- Q has a profound impact on the performance of the basic RF circuit building blocks [3]. Experience in the integration of inductors has been gained over the past two decades as part of the development of monolithic microwave integrated circuits (MMICs) on GaAs [4]. The optimization of this type of inductor, however, is not as difficult as on silicon, because GaAs is semi-insulating, so that substrate losses are negligible. Also, thick electroplated gold (Au) interconnects are typically used in MMICs, leading to very small ohmic losses in the spiral coil and thus high Q -factors [4]. In contrast, conven-

tional silicon substrates have a resistivity of $10\ \Omega\ \text{cm}$ or lower, so that substrate losses are well noticeable. The interconnects used in silicon technology are designed for very large scale integration (VLSI) applications, i.e., wire widths and spaces measure close to $1\ \mu\text{m}$, limiting the maximum metal thickness to about $1\text{--}2\ \mu\text{m}$, and the metallization is aluminum (Al) with a comparably high resistivity [5].

Modern silicon fabrication processes, however, feature routinely multilevel interconnects with up to six metal layers. In Section II.A, we will discuss how multilevel interconnects can be utilized to reduce both the ohmic losses in the spiral coil and the substrate losses without any alteration of the fabrication process. This kind of inductor design is consequently implied to as a conservative approach. On the other hand, modification of the silicon fabrication process has recently been explored, and novel types of substrates, such as silicon-on-insulator (SOI), silicon-on-sapphire (SOS), high-resistivity silicon (HRS), or glass have been studied as ways to reduce or eliminate substrate losses [6]. Micromachining techniques have been investigated either for the same reason or to enable novel integrated RF structures. Also re-

cently, a strong effort has been made to replace Al VLSI interconnects by copper (Cu), reducing the metal resistivity to about 50% [7]. These novel substrate types and interconnect schemes may be adopted by silicon technology in the near future, either driven by other applications, or they may be part of dedicated silicon processes geared toward RF applications. At the moment, however, those novel processes are implied to as innovative approaches as for mentioned reasons. They will be discussed in Section II.B. Section III is devoted to inductor modeling, which is an important task because the requirements on parameter control in RF circuits are more stringent than those in digital designs. In Section IV, we will address special issues the rf circuit designer may raise. Those include the crosstalk between inductors and the effect of a substrate contact on the inductor characteristics. A summary of the findings and an outlook on future possible developments will be given in Section V.

II. DESIGN OF SPIRAL INDUCTORS ON SILICON

Fundamentally, three basic inductor structures are feasible in silicon technology, i.e., the planar spiral coil structure [2], the multilevel spiral (MLS) coil inductor [8], and the solenoidal device (Fig. 1a–c) [9]. The structures are built by using the metal layers $M - i$ and the via connections $V - i$ between them, with $i = 1$ through n for the metal layers and $i = 1$ through $(n - 1)$ for the vias. (The electrical connection to the different silicon regions is provided by an additional via contact that is not considered part of the interconnect scheme and that is not used for the fabrication of the spiral inductor structure.) While a solenoid has the advantage that the main electromagnetic flux is parallel to the silicon surface and thus substrate losses are potentially minimal, it has the disadvantage that it will suffer from the considerable contact resistance between the repeated vias and metal layers in VLSI interconnect structures (Fig. 1a). MLS inductors provide a high inductance per area, but the self-resonance frequency is low, limiting the application of this device to low frequencies (Fig. 1b) [8]. Most inductors on silicon to date are therefore planar spiral inductors, even though the electromagnetic flux is directed into the silicon substrate (Fig. 1c). Another reason for preferring this structure is probably the extensive experience with the design of integrated inductors on GaAs [4]. The basic spiral

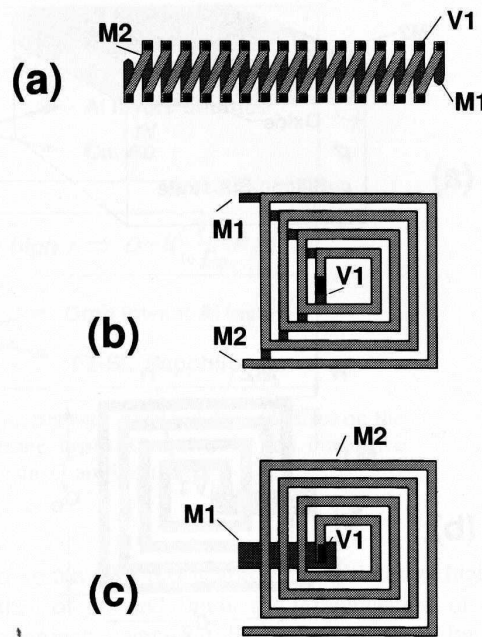


Figure 1. Schematic plan views of (a) a solenoidal inductor, (b) a multilevel-spiral (MLS) inductor, and (c) a planar spiral coil.

inductor structure requires a minimum of two levels of metal and one via connection between them (Fig. 2). The spiral coil is defined by the outer dimensions (d_o), the number of turns (n), the width of the conductor (W), and the space between the turns (S), as shown in Figure 2b. An underpass contact at a lower metal level and a via connection are used to bring the inner end of the coil to the outside (“M1” in Figure 2a and b). The spiral coil can be modeled with good accuracy by using the simple lumped-element representation in Figure 3a [10]. The model consists of the ideal inductance L_s , the series resistance R_s to describe the ohmic losses in the coil, and the capacitance C_p which represents the interwire capacitance components and the capacitance between coil and underpass layers. The resistance R_s can be frequency dependent as a result of the skin effect in the coil conductor. This model holds well for inductors on GaAs, where substrate losses are negligible, but not for silicon. The losses in the silicon substrate are twofold. First, there are the capacitive losses, described in the extended model of Figure 3b by the oxide capacitances C_{ox} and the bulk resistances R_b (in spite of the asymmetry of the spiral coil, identical elements C_{ox} and R_b are considered in Figure 2 for simplicity reasons). Second, eddy currents in the substrate can

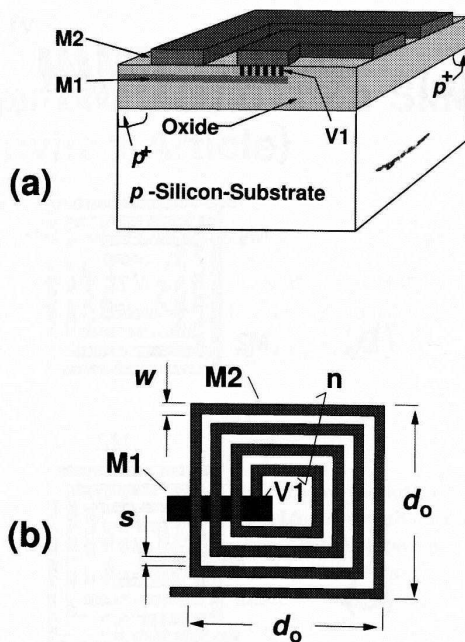


Figure 2. Cross-sectional view (a) and plan view (b) of a basic spiral inductor structure on a silicon substrate.

be significant if the silicon resistivity underneath the spiral coil is low. The physical nature of eddy currents is not considered in the model of Figure 3b, but its effect can be represented by a reduction of the inductance L_S and an increase of the resistance R_S . Likewise, the skin effect in the substrate has to be represented by a frequency-dependent R_B , if applicable. Both, the eddy currents and the skin effect in the substrate are not significant if the substrate resistivity is of the order of $10\ \Omega\ \text{cm}$, which is usually a preferred and practical value.

Another effect of the conductive silicon substrate is that the definition of the substrate potential is crucial because it can affect the electrical characteristics of the inductor, particularly if the silicon resistivity is high (e.g., $10\ \Omega\ \text{cm}$) [11]. Differently from conventional MMIC structures, no RF ground potential is provided at the backside of the wafer due to the lack of a via contact through the wafer. The substrate potential is defined by a substrate contact at the wafer surface that is placed close to or at some distance from the spiral coil, depending on the circuit layout. In the lumped-element model, the substrate contact is therefore represented by a resistor R_{Sub} contacting the substrate terminal to the node between C_{Ox} and R_B near the outside terminal (Fig. 3b).

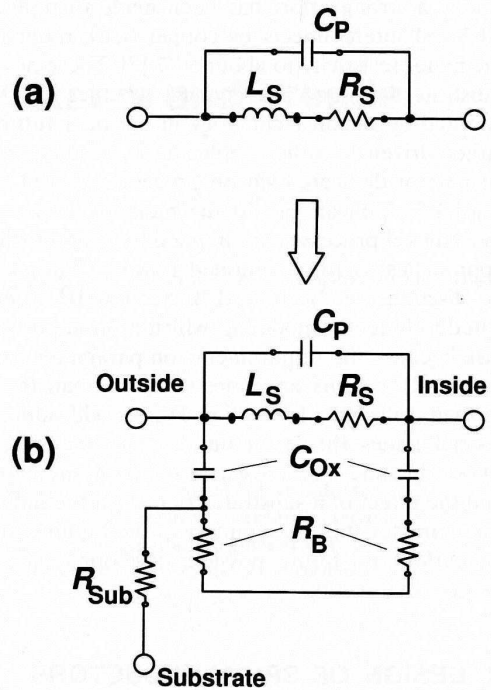


Figure 3. Lumped-element models of (a) a spiral inductor on an ideal substrate and (b) a spiral inductor on a lossy silicon substrate, including a substrate contact.

A closer look at the inductor model in Figure 3b provides an insight in the electrical behavior of the device. It is first important to consider, that the spiral inductor has generally large lateral dimensions and a narrow vertical cross-section, because planar silicon fabrication technology is used for the inductor fabrication. Therefore, the capacitances C_{Ox} are significantly larger than C_P . Of the two possible resonance loops shown in Figure 3b, resonance via C_{Ox} will therefore occur at a much lower frequency than via C_P , restricting the application to low frequencies. In case the C_{Ox} cannot be reduced by increasing the spacing of the spiral coil from the silicon, the only way to prevent self-resonance via C_{Ox} is to provide a sufficiently large R_B . This, however, does not fully eliminate the RF losses through the substrate path (i.e., via C_{Ox}), in particular at the higher frequencies. However, as a result, the RF signal will pass primarily through L_S at low frequencies and increasingly through C_{Ox} at high frequencies.

The degree at which the inductor deviates from an ideal device is described by the quality factor which is $Q = \text{im}(Z)/\text{re}(Z)$ if Z is the impedance of the inductor. (For the one-port case, Z is

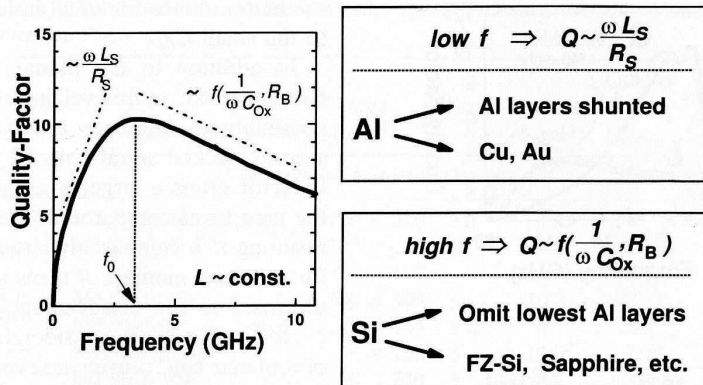


Figure 4. Quality-factor (Q) as a function of frequency with indicated dependencies on the ohmic losses in the spiral coil and on the substrate losses. Conservative and innovative means of optimizing a spiral inductor for a maximum Q are illustrated.

identical to the measured impedance). The higher Q is, the closer is the device to an ideal inductor. Figure 4 shows Q as a function of frequency, indicating that a distinct maximum ($Q_{\max}$) develops at a certain frequency (f_0). From the model in Figure 3b it is obvious, that at low frequencies the increase of Q with frequency depends mainly on R_S , i.e., on the ohmic losses in the spiral coil. The decay of Q at high frequencies depends on C_{Ox} and R_B (provided that C_P is small). The challenge in inductor design is therefore to tailor the layout of the spiral coil and the isolation from the silicon substrate in a way that the highest possible $Q_{\max}$ is obtained at the desired operating frequency f_0 .

A. Inductors Based on the Conservative Approach

The optimization of an inductor can be approached either in a conservative or an innovative way, as illustrated in Figure 4 [12]. The conservative approach considers the utilization of multi-level interconnects without any process alteration to achieve an optimum inductor design. The thickness of the conventional Al layers is limited to about $2\ \mu\text{m}$, because Al interconnects are developed for high levels of integration, requiring a small metal pitch (metal pitch = min. metal width + min. metal space) of the order of $1\text{--}2\ \mu\text{m}$. The ohmic losses in the spiral coil can therefore only be reduced if several layers of metal are shunted together, using dense arrays of via connections to achieve an effectively thicker metal layer (Fig. 5) [13, 14]. The resistivity of the

tungsten (W) vias is about three times as high as that of Al and limits the effectiveness of this approach somewhat [10]. Also, with a limited number of metal layers available, shunting several of them together to form the spiral coil, has the consequence that C_{Ox} becomes larger than in the case when only the top metal layer is used for the

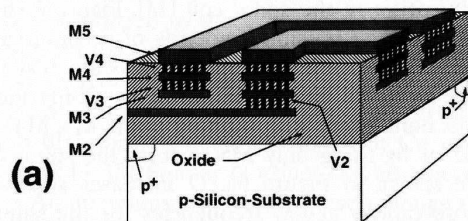
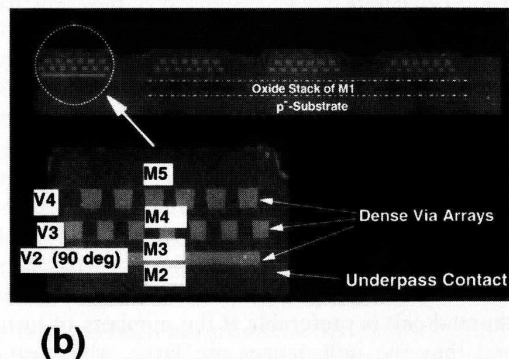


Figure 5. Schematic (a) and scanning electron micrograph (SEM) (b) of a five-level inductor structure.

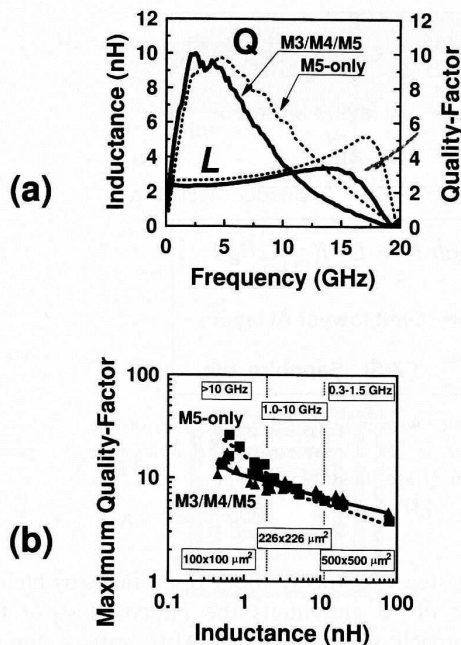


Figure 6. Inductance and quality-factor vs. frequency (a) and maximum quality factors vs. inductances (b) of five-level inductor structures using either the top metal layer (M5-only) or a shunted metal layer configuration (M3/M4/M5).

fabrication of the spiral coil [14]. Figure 6 shows the resulting possible tradeoffs of a conservative inductor design if three metal layers are available. The electrical characteristics of two 2-nH inductors, built either with shunted layers M3, M4, and M5 or by using only M5 to form the spiral coil, are shown in Figure 6a. Q increases somewhat more rapidly at low frequencies for the shunted structure compared to the single-layer inductor due to the lower coil resistance, but the Q falls off faster at high frequencies due to the larger oxide capacitance. $Q_{\max}$ is not very different for the two cases, but f_0 is lower for the inductor with shunted metal layers, indicating the window for tailoring the design of this device. There is, however, a difference in $Q_{\max}$ for smaller or larger inductance values (Fig. 6b). Coils with many turns and thus large inductance values suffer comparably more from the limited metal resistance, while inductors with few turns and small inductance values suffer mostly from the substrate losses. It is therefore obvious that the shunted coil is preferable if the numbers of turns and thus the inductances are large, while using only the top metal layer to form the spiral coil is

the better choice for small inductance values, due to the small C_{ox} .

In addition to the planar coil structure discussed so far, multilevel interconnects offer the possibility to fabricate inductor structures with several stacked spiral coils [8, 15]. Such an MLS inductor offers a larger average area enclosed by the wire turns compared to the planar spiral coil, resulting in a comparably larger inductance value for the same number of turns and the same outer dimensions. The disadvantage of this type of inductor is that C_p is considerably larger than that of a planar coil, causing a severe reduction of the self-resonant frequency (f_{SR}). The low f_{SR} not only limits the application of MLS inductors to low frequencies, but also causes that the inductance changes considerably with frequency near f_0 , which is often not desirable in circuit design. It becomes clear, that the MLS inductor will mainly find an application where a large inductance value at minimum area consumption in combination with a small DC resistance is needed without the requirement of an utmost control of the electrical characteristics, such as for RF chokes [8].

In the upper half of Table I, we have listed the key parameters of some inductor implementations based on the conservative approach. It is obvious that the reported $Q_{\max}$ values differ significantly. That depends in part on the different fabrication processes and lateral designs, but it is also very important to be reminded that for the same fabrication process a small inductance value typically combines with a higher $Q_{\max}$ than a large inductance, and *vice versa* (Fig. 6b) [14]. This observation does not necessarily present a limitation to inductor design. Fortunately, in some applications, large inductance values are needed at low frequencies, where a moderate Q can be sufficient. Lower inductance values are needed at high frequencies, where the spiral inductor inherently provides the required larger Q and f_{SR} . One can therefore say, that the spiral inductor on silicon is roughly scaleable with frequency. This trend is illustrated in Figure 6b, where the maximum Q s and the ranges of f_0 are drawn as a function of the inductance values of a wide variety of inductor dimensions and coil layouts. For other applications, such as in voltage-controlled oscillators, the highest possible Q s are required at high as well as at low frequencies [3]. For those cases, one can say that the application of an integrated inductor on silicon becomes more favorable at high frequencies.

TABLE I. Comparison of Published Inductor Results with Separation into Conservative and Innovative Device Structures and Fabrication Processes

Author(s)	Description	Area (μm^2)	Turns n	Induct. L (nH)	Quality Factor Q_{max}	Operating Freq. f_0 (GHz)	Resonance Freq. f_{SR} (GHz)
Conservative Inductor Designs							
Burghartz et al. [25], 1995	M3/M2/M1 on p^- -Si	226×226	3	1.45	24	2.3	> 20
Burghartz, Jenkins, and Soyuer [8], 1996	MLS on p^- -Si	226×226	8	6.8	7.8	1.3	5.6
Groves et al. [26], 1996	M3 on p^- -Si	$\sim 400 \times 400$	6	10.2	7.5	1	8
Kim and O [27], 1997	M3/M2/M1 on n -well	145×145	9.25	6	2.6	1.5	5.8
Merrill et al. [15], 1995	MLS on p^- -Si	$\sim 150 \times 150$	3	15.5	2.64	0.42	—
Nguyen and Meyer [2], 1990	M2 on p^- -Si	230×230	9	9.7	3	0.9	2.5
Soyuer et al. [13], 1995	M3/M2/M1 on p^- -Si	226×226	4	2.1	9.3	2.4	~ 20
Yue and Wong [28], 1997	M2 on perforated gnd	$\sim 280 \times 280$	6	8	7	1.8	3.5
Innovative Inductor Designs							
Ashby et al. [19], 1994	6 μm Au on HRS	300×300	2	2.88	12	3.2	> 10
Burghartz et al. [18], 1996	2.5 μm Cu on Sapphire	226×226	3	1.45	40	5.8	> 20
Burghartz et al. [3], 1998	4 μm Cu on Quartz	226×226	3	1.5	60	6	> 20
Chang, Abidi, and Gaitan [22], 1993	M2 on suspended Sub.	440×440	20	100			2.9
Dekker et al. [16], 1997	3.5 μm Al on Glass	$\varnothing 600 \mu\text{m}$	2	2.6	39	4.3	10.5
Johnson et al. [29], 1996	M2 on SOS	$\sim 150 \times 150$	5	4	11.9	~ 3.0	13.9
Park et al. [17], 1997	4 μm Al on HRS	290×290	8	11.98	15.3	3.25	~ 9.0
Sun et al. [23], 1996	M2 on suspended Sub.	$\sim 200 \times 200$	4	1.1	28	18	84

B. Innovative Inductor Structures

However, as seen, the conventional approach faces limitations set by the resistivity of the Al wires, the conductivity of the conventional silicon substrate, and the relatively small thicknesses of the dielectric and the metal films. Those limitations can be overcome by deviating from main stream silicon process technology. For instance, thicker Al wires can be realized at the expense of the metal pitch [16, 17]. A more dramatic reduction of the ohmic losses in the spiral coil is possible if the Al lines are replaced by Cu wires. The Cu-Damascene technology, which has recently been proposed for application in VLSI interconnects, offers about a twofold reduction in resistivity, thicker metal layers for a given metal pitch, and taller via connections (Fig. 7) [7]. Cu-interconnects can therefore be used to reduce R_s in comparison to an Al coil having the same dimensions; in the present experiment the Cu line thickness was 4 μm (inset of Fig. 8). Further, the vias between the metal layers are not necessarily limited in width, such as for tungsten (W) vias used in Al interconnects [5], which allows one to minimize R_s , as shown in the inset of Figure 8 as

well. The tall Cu-via connections, shown in Figure 7, can be utilized to space the spiral coil further away from the silicon as if it would be possible in an Al-interconnect scheme; the result is a comparably lower C_{ox} . A dramatic improvement of Q could therefore be demonstrated with Cu interconnects [3, 18]. Similar Q -values can be expected from Au interconnect structures, even though this technology does not currently enjoy the benefit of being driven by VLSI applications [19, 20].

For the reduction of the substrate losses, it seems first plausible to apply silicon substrates with a much higher resistivity, which is possible by using float-zone (FZ) instead of Czochralski material [6, 12, 18]. Such HRS substrates, however, are not likely suitable for the integration of dense circuitry. A good tradeoff between the requirements of circuit integration and inductor optimization is given with a combination of a silicon-on-insulator structure, which electrically isolates the active device silicon region from the bulk silicon, and a HRS substrate. This type of substrate has been advertised as MICROX [21]. SOI alone does not provide any significant benefit for inductor integration, because the buried oxide is

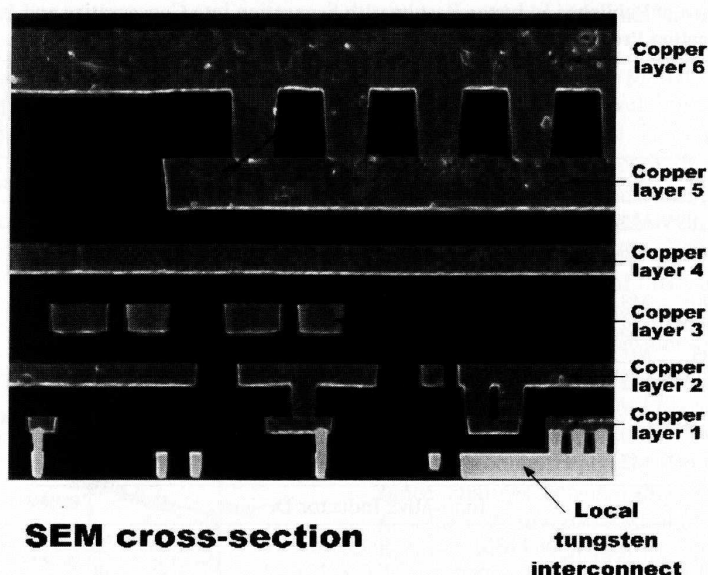


Figure 7. Cross-sectional SEM of a six-layer Cu-Damascene interconnect structure.

typically very thin and the skin depth at GHz-frequencies and for a conventional silicon resistivity is comparable to the substrate thickness [12]. Therefore, the substrate losses can only be eliminated by using either an insulating substrate ma-

terial or by removing the silicon under the spiral coil. Examples of the first option are silicon-on-sapphire substrates or bonding onto glass or quartz carrier wafers [3, 16, 18]. For the second option, micromachining techniques can be used to form a suspended inductor over a cavity of several hundreds of micrometer depth on a conventional silicon wafer [22, 23]. Such a micromachined inductor is an attractive solution toward a higher Q and operation at high frequency. Good compatibility with the active device fabrication is achieved in particular if postprocessing methods are used. Some concerns exist, however, with respect to the stability of such structures during plastic packaging. Farther on the horizon are other micromachining techniques which allow to fully exploit the vertical dimension and enable one to expand vertically from the strictly planar wafer surface in order to realize three-dimensional (3D), solenoidal inductors with eliminated or largely reduced substrate losses [24]. A summary of some published results on innovative inductor structures is given in the bottom part of Table I.

Figure 9 shows a comparison of conservative inductor implementations with the use of different numbers of metal levels to an innovative inductor design, which uses Cu-Damascene interconnects and a low-loss substrate. Inductor designs with three different areas are compared, 100×100 , 226×226 , and $500 \times 500 \mu\text{m}^2$. Within this range of area sizes, inductances in

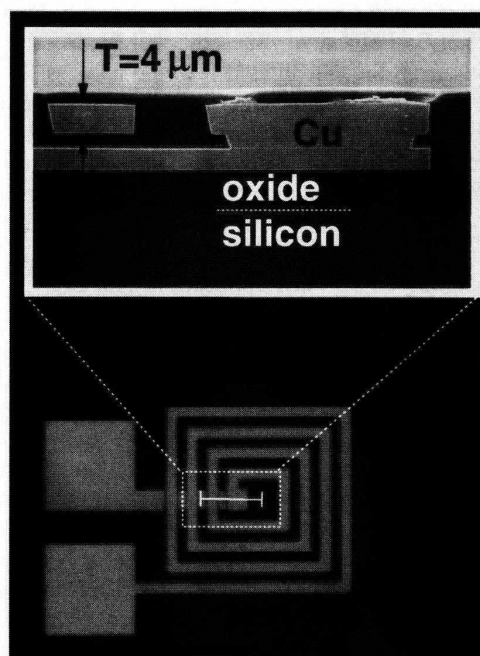


Figure 8. Plan view of a four-turn Cu spiral inductor, and cross-sectional view of the center part of the spiral coil (inset).

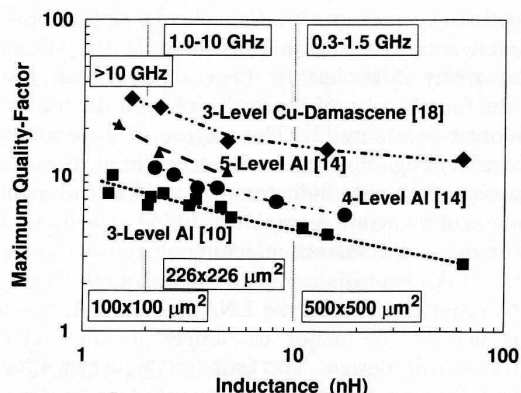


Figure 9. $Q_{\max}$ vs. inductance values for different inductor geometries and fabrication processes.

between 0.5 and 100 nH can be achieved. A 1.5-nH inductor, as an example, has a Q in the range of about 10–40, depending on the fabrication process.

III. INDUCTOR MODELING

Experience in the modeling of the planar spiral inductor has been gathered extensively over the past decades. Various analytical formula have been derived for the calculation of the inductance value for a given lateral layout of the spiral coil [4, 30]. Those models, however, are all based on the assumption of a lossless substrate material. However, as simple as it first seems to extend these models to the case of a lossy substrate, this task turned out to be extremely difficult and consequently has motivated active research in this area. The possible model approaches can be separated in (i) analytical–physical [31–33], (ii) analytical–semi-empirical [34], (iii) three-dimensional (3D) numerical [11], and (iv) inductor library models [10–12, 14, 18, 19]. The advantage of the first three types of models is that they attempt to calculate the electrical characteristics of an inductor structure *a priori*, while the library approach is limited to a fixed number of characterized inductor designs. The highest level of accuracy of the predictive inductor models is expected from the 3D approach. The narrow vertical dimensions of the spiral coil, however, have to be modeled in conjunction with the thick silicon substrate, making the modeling cumbersome and leading to long conversion times. A reasonable solution may come from partial-element equivalent circuit (PEEC) solvers which allow one to

simplify the description of the inductor structure wherever permissible to arrive at reasonable conversion times without sacrificing the level of accuracy too much [11, 35]. The analytical–physical models trade off accuracy for simplicity and are likely suitable only to achieve a rough estimate of the expected electrical characteristics [31–33]. The analytical–semi-empirical modeling approach derives an analytical inductor model from a large characterized inductor library to extrapolate to other inductor structures or implementations, using other fabrication processes [34]. An inductor library model is derived from one-port or two-port S -parameter measurements on fabricated devices. The impedance of the inductor relates to the measured impedance as $Z = Z_{11}$ for the one-port case and $Z = Z_{11} - 50 \Omega$ for the two-port case. Both the inductance $L = \text{im}(Z)/(2\pi f)$ and the quality factor $Q = \text{im}(Z)/\text{re}(Z)$ can be determined from Z . The inductance at low frequency is used in the model in Figure 3 as $L \approx L_S$. R_S in the model is derived from dc measurements, which is a good approximation as long as the skin effect in the metal lines is small. C_P and C_{Ox} are calculated from the coil geometry. R_B is more or less a fitting parameter due to the 3D RF current flow in the silicon substrate.

It is the authors opinion, that the stringent requirements in the accuracy of inductor models for RF circuit design make a well characterized inductor library indispensable. Analytical or numerical predictive models may be instrumental in limiting the number of variations in the development of an inductor library, but they will not likely make such a library obsolete.

Figure 10 shows the comparison of the measured and the modeled inductance and Q values vs. frequency for a sample inductor. The schematic of the lumped-element model with the parameter values used is shown in the inset of Figure 10. It is obvious that the agreement of model and measured data is excellent at frequencies below f_{SR} .

IV. CIRCUIT LAYOUT ISSUES

The design of a spiral inductor for use in an integrated RF circuit is not only crucial because the Q of the inductor is low in comparison to other passive RF components. The structure also occupies a large silicon area, crosstalk between inductors potentially limits the flexibility in circuit layout, and the local definition of the substrate bias by a substrate contact can affect the inductor

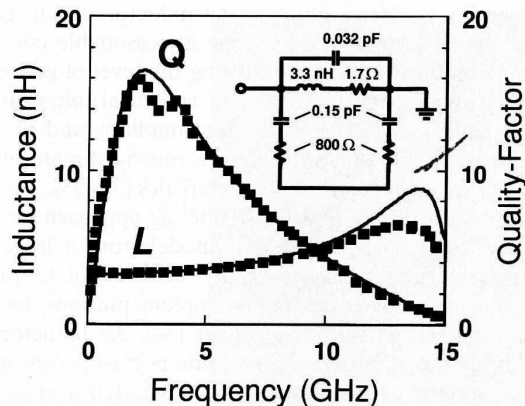


Figure 10. Comparison of measured and modeled inductor characteristics of a copper (Cu) inductor, with the lumped-element model parameters in the inset.

characteristics [3, 11]. The area of an inductor can to some extent be minimized by optimization of the conductor width and the space between the turns of the spiral coil without deviating from the desired inductance value, without sacrificing the Q , and without shifting f_0 significantly [3]. This can be understood as follows: the resistance of the coil wire increases with frequency as a result of the skin effect, which causes that the rf current mainly flows near the edges of the conductor. An increase of the wire width to lower the resistance and enhance the inductor's Q may therefore not be effective. On the contrary, a wider conductor increases the oxide capacitance (C_{ox} in Fig. 3b) and thus the substrate losses, leading eventually to a lower Q_{max} at a reduced f_0 . The minimization of the wire width can therefore have two benefits, i.e., it can allow for a small inductor area and for the highest possible Q_{max} at a maximum f_0 . For a minimum inductor area, the space between the turns (S in Fig. 2b) must be minimized as well. The reduction of S , however, leads to an increase of C_p which must be kept below a certain value in order to maintain a sufficiently high f_{SR} . We had mentioned in Section II.A that the stacking of spiral coils to form an MLS inductor provides an inductance–area that is larger than that of a planar spiral coil at the expense, however, of a severe reduction of f_{SR} [8]. Also in the MLS structure, it is the large C_p that causes f_{SR} to be small.

Crosstalk between inductors can be inductive and capacitive. The inductive coupling between spiral inductors depends significantly on the lateral spacing, but even for adjacent inductors the insertion loss is very low, as long as no capacitive

coupling is present [36]. Capacitive coupling, however, exists on silicon substrates. If the silicon resistivity is sufficiently high, the insertion loss was found to be of the order of -40 dB for the closest proximity [3]. This degree of crosstalk is small enough not to be of concern in most cases, except if on-chip inductors are used in the input stage of a low-noise amplifier (LNA) as well as for the output impedance matching of a power amplifier (PA). An isolation of the order of 80 dB may be required between the LNA and the PA, which is one of the major challenges in single-chip transceiver design. The isolation between LNA and PA can be improved by using an external impedance matching network for the PA or by providing improved AC device isolation [28, 37, 38].

A third circuit layout issue results from the fact that the silicon substrate resistivity be high to provide a large Q_{max} at a high f_0 and a high f_{SR} . The substrate bias is therefore not uniform, as it would be for very conductive silicon or for a metal ground plane. The electrical characteristics of a spiral inductor on silicon can therefore be affected by the proximity of a substrate contact, as Figure 3b illustrates. The position of a substrate contact with respect to the spiral coil of the inductor is modeled there as a lumped resistance R_{Sub} . It has been shown recently that a substrate contact can have a beneficial or a detrimental effect on the inductor- Q , depending if the device is configured as a one-port or a two-port structure. The increase in Q_{max} in case of the one-port configuration, however, is traded against a reduced f_{SR} [11].

V. SUMMARY AND OUTLOOK

Different types of inductor structures on silicon substrates, the modeling issues, and circuit layout aspects have been discussed in this paper. It has been shown that for the inductor integration either a conservative or an innovative approach can be taken, depending if the compatibility with mainstream silicon processing or the highest possible Q is the primary goal. Practical inductance values range from 0.5 to 100 nH, and Q_{max} can be made as high as 25 for conservative and 40 for innovative implementations. Various modeling efforts are underway, ranging from a fully analytical, physical model to a fitted lumped-element library model. Given the complexity of the three-dimensional spiral inductor on the lossy silicon

substrate, the conventional approach in analog circuit design of developing a characterized device library may also be indispensable for spiral inductors. The conductivity of the silicon substrate makes it necessary to consider potential crosstalk and substrate contact effects in circuit layout. Overall, the spiral inductor on a silicon substrate is a feasible device today. It can be expected that integrated inductors will be extensively used in silicon RF circuit design.

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BIOGRAPHY



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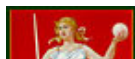
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Exhibit 1002

DESIGN, SIMULATION AND APPLICATIONS OF INDUCTORS AND TRANSFORMERS FOR SI RF ICs

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Chapter 1

INTRODUCTION

1. INTRODUCTION

The wireless communication revolution has spawned a revival of interest in the design and optimization of radio transceivers. Passive elements such as inductors, capacitors, and transformers play a critical part in today's transceivers. In this book we will focus on the analysis and applications of such devices. In particular, we will demonstrate techniques for calculating the loss when such devices are fabricated in the vicinity of conductive substrates such as Silicon.

2. PASSIVE DEVICES IN EARLY INTEGRATED CIRCUITS

Until recently, passive devices, especially in integrated form, played a relatively minor role in Si integrated circuits in comparison with active devices such as transistors. The most important reason for this can be attributed to the size difference. Active devices were continually shrinking and occupying less and less chip area whereas passive devices remained large. At low frequencies, circuit designers employed simulated passive devices as much as possible to make their products more compact and reliable.

While it was possible to fabricate small values of capacitance on-chip, inductors were virtually impossible due to the large physical area required to obtain sufficient inductance at a given frequency. This was compounded by the losses in the substrate which made it virtually impossible to fabricate high quality devices. Small Si die were desirable to keep costs low and to improve reliability since larger die resulted in lower yields [Gray and Meyer, 1993].

When passive devices were needed, usually they were connected externally on-board rather than on-chip. This is possible as long as few external components are needed and the package parasitics are negligible in comparison with

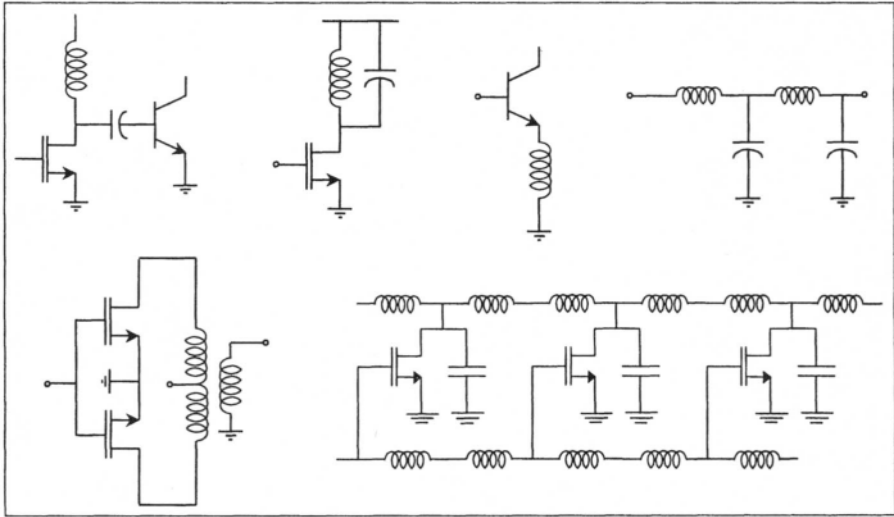


Figure 1.1. Applications of passive devices in Si IC building blocks. (a) Impedance matching. (b) Tuned load. (c) Emitter degeneration. (d) Filtering. (e) Balun. (f) Distributed amplifier.

the external electrical characteristics of the device. Take, for instance, a VCO at 100 MHz versus a VCO at 10 GHz. At 100 MHz a typical tank inductance value will be on the order of 100 nH whereas at 10 GHz the tank inductance is around 1 nH. To access a 1 nH inductor externally is impossible in standard low cost packaging since the package pin and bond wire inductance can exceed 1 nH. Also, as more and more functionality is integrated on-chip, more and more passive devices are needed requiring larger packages which increase the cost. These issues have led to a surge of recent interest in integrated passive devices.

3. APPLICATIONS OF PASSIVE DEVICES

Passive devices, such as inductors and transformers, play an integral part in the performance of circuit building blocks, especially at high frequency. Inductors can be avoided at lower frequencies by using simulated inductances employing active devices. Simulated inductors are more difficult to realize at higher frequencies as active device gain drops. In addition, simulated inductors have finite dynamic range, require voltage headroom to operate, and inject additional noise into the circuits. These limitations place a severe restriction on their application, especially in highly sensitive analog building blocks.

In Fig. 1.1 we see several common applications of inductors, capacitors, and transformers in wireless building block circuits. In (a) we see a narrow-band impedance matching example. Here the input impedance of the second trans-

tor is matched to an optimal impedance value desired by the driving transistor. For instance, in a power amplifier the input impedance of a large output stage device is low due to the capacitance and to obtain sufficient power gain this low impedance is transformed into a larger value. Impedance matching allows circuit designers to obtain minimal noise, maximum gain, minimal reflections, and optimal efficiency when designing circuit building blocks such as low-noise amplifiers (LNAs), frequency-translation circuits (mixers), and amplifiers.

In (b) we see an LC tuned load. A tuned load can take the place of a resistive load to obtain gain at high frequency. The advantages are clear as an LC passive is less noisy than a resistor, consumes less voltage headroom, and obtains a larger impedance at high frequency. A resistive load is always limited by the RC time constant which limits the frequency response. Tuned loads are also a critical component of oscillators. The LC tank tunes the center frequency of the oscillator and the intrinsic Q allows the tank to oscillate with minimal power injection (and hence noise) from the driving transistor.

In (c) an inductor is used as a series-feedback element. Series feedback can be used to increase the input impedance, stabilize the gain, and lower the non-linearity of the amplifier. By using an inductor in place of a resistor, less voltage headroom is consumed, and less additional noise is injected into the circuit. The inductance can also be used to obtain a real input impedance at a particular frequency, thus providing an impedance match at the input of the amplifier.

In (d) inductors and capacitors are used to realize a low-pass filter. Filters of this type are superior to active filter realizations such as gm-C or MOSFET-C filters as they operate at higher frequencies, have higher dynamic range due to the intrinsic linearity of the passive devices, and inject less noise while requiring no DC power to operate.

In (e) we see a center-tapped transformer serving as a balun, a device which converts a differential signal into a single-ended signal to drive external components. Differential operation is advantageous in the on-chip environment due to the intrinsic noise rejection and isolation. Off-chip components, such as SAW filters, though, are single-ended and a balun is needed to convert external single-ended signals to on-chip differential signals.

Finally, in (f) we see inductors and capacitors forming an artificial transmission line in a distributed (traveling-wave) amplifier. Since the LC network acts like a transmission line, it has a broadband response. A wave propagating on the gate-line is amplified and transferred onto the drain line. If the wave speed on the drain line matches the gate line, the signals on the drain line add in phase and the drain line delivers power into a matched load.

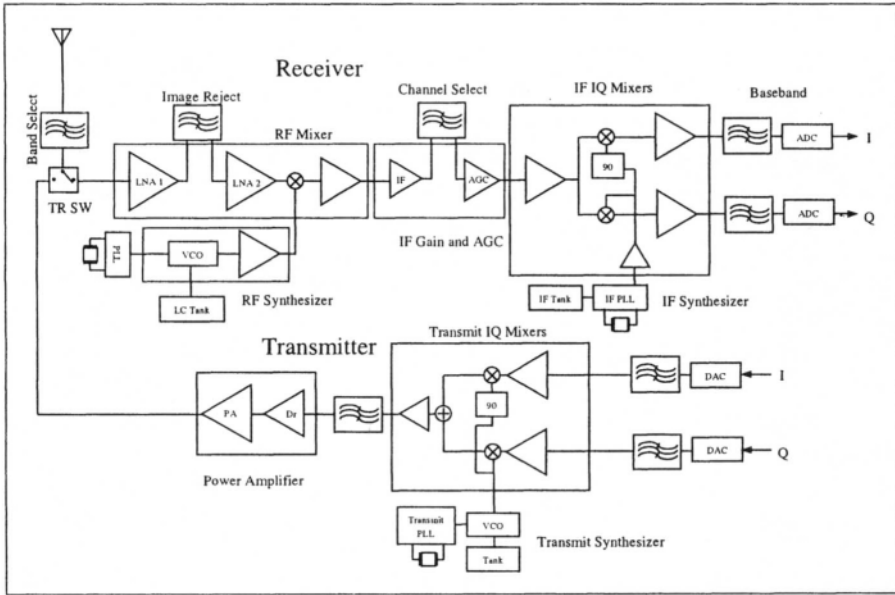


Figure 1.2. Traditional superheterodyne transceiver architecture.

4. WIRELESS COMMUNICATION

The wireless transceiver serves as an excellent example of a system which employs passive devices. In recent times, several factors have contributed to the possibility of portable wireless communications. Continuing technology improvements have enabled low-cost Si circuits to operate in the 1–10 GHz frequency range. In this frequency range efficient portable antennas can be realized since the free-space wavelength is on the order of centimeters. Higher frequencies also allow higher bandwidths to be realized for increased throughput or an increase in the number of users sharing the spectrum. Furthermore, by limiting the transmit power, transceivers which are physically remote can reuse the same spectrum with minimal interference leading to the cellular concept of communication. Finally, at these higher frequencies the critical passive elements, such as inductors and capacitors, are small enough to be realized on-chip.

To see the importance of passive devices, consider the simplified block diagram of a traditional superheterodyne transceiver shown in Fig. 1.2. Note that this transceiver is realized as several different chips or modules and many components of this transceiver are off-chip discrete components. This transceiver is thus bulky and expensive. The goal of many research projects has been to realize this transceiver in a more integrated form [Rudell et al., 1997, Rofougaran

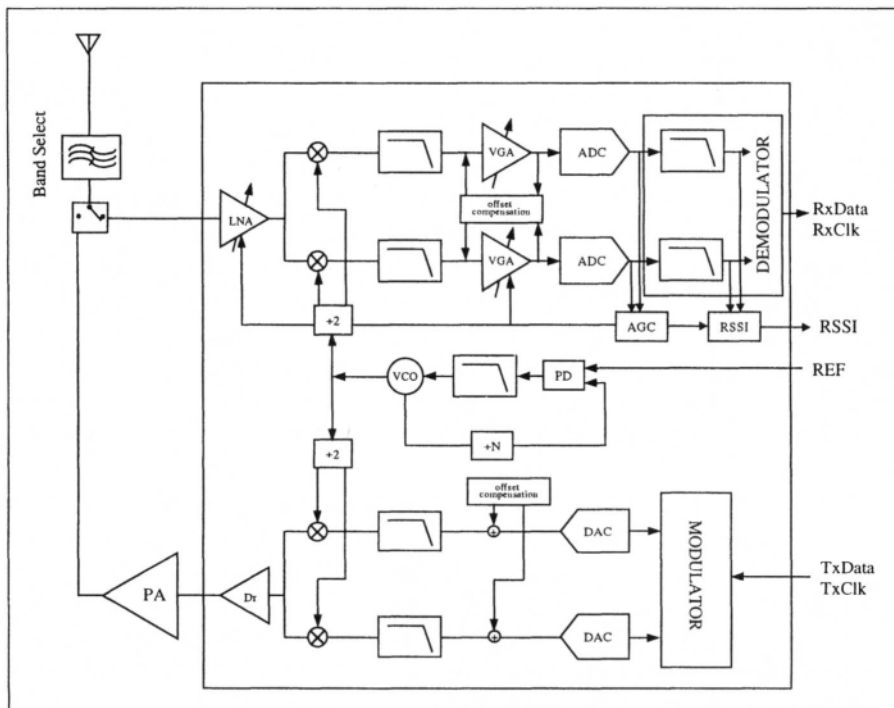


Figure 1.3. Zero-IF direct conversion receiver architecture transceiver.

et al., 1998a, Rofougaran et al., 1998b, Steyaert et al., 1998]. To realize this goal, many off-chip components must be integrated and the inductor is one such key element.

Now contrast Fig. 1.2 with Fig. 1.3 [Eynde et al., 2000], a modern integrated transceiver with minimal off-chip components. Here system architecture innovations such as a zero-IF direct conversion receiver topology eliminates or reduces the need for external filtering. The LNA and VCO tank and the external PLL have also been integrated onto a single chip. The IF is sampled at baseband and digital processing of the signal is performed on the same die. The integrated inductor plays an important role in impedance matching, gain, tuning, and filtering. For instance, in the low noise amplifier (LNA) inductors are used for a real input impedance match and as a narrow-band high impedance load. Here, a resistor is precluded because of the extra noise and voltage headroom required. In the voltage controlled oscillator (VCO) inductors and capacitors form the tuned load of the tank while varactors are used to tune the center frequency to provide a fixed IF frequency. High quality (Q) factor passives limit the phase noise of the VCO which can degrade the receiver sensitivity through

reciprocal mixing. The high Q passives also minimize power leaking into adjacent channels which desensitizes other receiver units in nearby channels. On the transmit side, passives are used in the driver and power amplifier (PA) for impedance matching and gain. Impedance matching allows the power hungry PAs to operate at maximum efficiency and thus extends battery life.

One of the key difficulties in realizing an integrated transceiver lies in the difficult specifications that a transceiver must meet. The harsh wireless environment puts stringent requirements on the dynamic range requirements of the receiver. Since signal strength can vary by many orders of magnitude as mobile users move close to and far from the base station antenna, the transceiver must be able to operate with both extremely small signals close to the intrinsic noise floor of the transceiver and with extremely large signals which excite the desensitizing non-linearities of active devices. Furthermore, these constraints must be met while consuming very low power levels to extend battery life.

Thus, the fully integrated transceiver introduces several new problems. Low power and low noise operation requires the realization of high Q passive devices. Integration introduces parasitic coupling between the various circuit blocks. Within the analog portion parasitic coupling from the powerful transmit circuitry to the sensitive receive path is particularly worrisome. The coupling from the noisy digital blocks to the sensitive analog blocks is also a big concern. Note that this coupling occurs primarily through the package and through the substrate.

5. SI INTEGRATED CIRCUIT TECHNOLOGY

Si technology is a prime candidate for realizing future integrated circuits. While GaAs offers superior gain, higher frequencies of operation, and an insulating substrate, the difference in cost alone favors Si. In addition, emerging advances in Si technology (such as SiGe) are closing the gap between Si and GaAs in performance for the mass commercial market target in the 1–10 GHz frequency range.

When we also consider the potential to integrate digital functionality in CMOS or BiCMOS technology, Si is again the clear winner. Furthermore, due to the mass digital microprocessor and DSP markets, CMOS technology continues to improve. Thus, there are great benefits to integrating passive devices in CMOS technology. Consider the unity gain frequency of an NMOS transistor [Gray and Meyer, 1993]

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs}} = 1.5 \frac{\mu_n}{2\pi L^2} (V_{GS} - V_t) \quad (1.1)$$

and the similar expression for a bipolar transistor

$$f_T = 2 \frac{\mu_n}{2\pi W_B^2} V_T \quad (1.2)$$

Since the vertical base width of a bipolar transistor W_B is determined by a diffusion process whereas the lateral channel length L of an MOS transistor is determined by lithographic processes, bipolar transistors have enjoyed a superiority in speed. New advances in lithographic technology, though, have narrowed the channel length tremendously as MOS technology is the core of the worldwide digital market. Even taking into account that narrow channel device f_T have $1/L$ dependence as opposed to the $1/L^2$ dependence, CMOS technology is today a viable and cost-effective alternative to both bipolar and GaAs and will probably continue to be so for the next decade or longer.

From the perspective of cost, CMOS is the clear winner. But from the perspective of integrated passive devices, GaAs is clearly superior to standard Si. The reason for this stems from the insulating nature of the GaAs substrate which allows very high Q factor passives to be realized on-chip. The dominant limitation in performance is the metal conductivity whereas in Si the dominant loss mechanism at high frequency is the conductive substrate. Electromagnetic energy couples to the substrate and the lossy nature of the Si substrate limits the Q severely.

This is especially the case when the substrate is heavily conductive, as with epi CMOS substrates. Here, magnetically induced eddy currents in the substrate can be a dominant loss mechanism. For moderately conductive substrates, though, electrically induced substrate currents are the dominant loss mechanisms at frequencies below the self-resonant frequency of the device.

6. CONTRIBUTIONS OF THIS RESEARCH

This research has focused on the analysis, design, and applications of passive devices. In Part I emphasis is placed on analyzing inductors and transformers. The solution techniques developed can be easily applied to integrated capacitors and resistors. A general approach is developed from Maxwell's equations to determine the partial inductance and capacitance matrix of an arbitrary arrangement of conductors situated on top of a stratified conductive substrate. The lossy nature of the underlying substrate and losses in the conductors leads to complex capacitance and inductance matrices. These techniques have culminated in a design and analysis software tool called *ASITIC*, "Analysis and Simulation of Inductors and Transformers for ICs." These general techniques can also be applied to extracting the substrate coupling occurring between metal structures residing in the substrate or in the oxide layers on top of the Silicon. This technique is a direct extension of [Gharpurey and Meyer, 1996].

In Part II of the book, we focus on some key applications of passive devices, such as voltage-controlled oscillators and power amplifiers. We show that key performance parameters such as phase noise and power amplifier efficiency depend on the quality of the passive devices. Thus, it is critical to be able to predict the performance of such structures.

Chapter 2

PROBLEM DESCRIPTION

1. DEFINITION OF PASSIVE DEVICES

Consider an arbitrary black box shown in Fig. 2.1 with an arbitrary number of externally accessible terminals. Sample “black” boxes are also shown in the figure. We would like to categorize each black box as passive or active.

Intuitively, the distinction between passive and active devices is clear. While passive devices can only consume or store energy, active devices can also supply energy. Thus, with active devices one can obtain power gain though this is impossible for a passive device. In other words, if we inject power into any terminal of a passive device and observe the power flowing into an arbitrary impedance at another terminal of the device, the real power is necessarily less than or equal to the power injected. If we lift this restriction, the device is active.

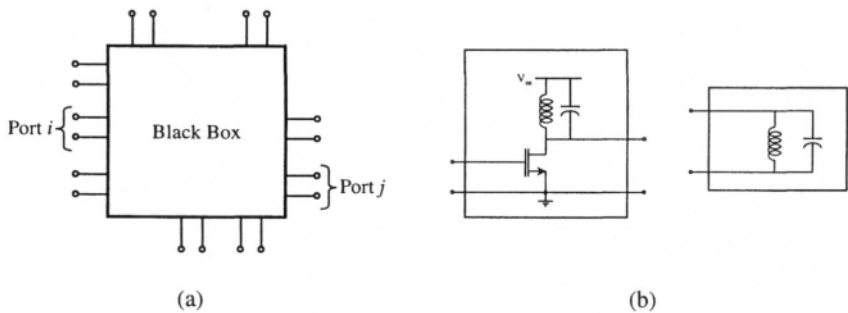


Figure 2.1. (a) An arbitrary black box with externally accessible ports, (b) The contents of two example “black boxes”.

Typical examples of passive devices include linear time-invariant resistors of finite resistance $R > 0$ which dissipate energy, ideal time-invariant linear capacitors and inductors, which only store energy. While the above elements are linear elements, passive elements such as diodes can be non-linear¹. Even though passive devices can have voltage or current gain, they cannot have power gain.

The archetypical example of an active element is of course the transistor and its predecessor, the vacuum tube. Unlike passive devices, such a device can be used to obtain power gain. These devices can be linear or non-linear, but most real world examples are non-linear. The distinction between active and passive is more difficult to make when time-varying elements are employed. For instance, a simple parametric amplifier constructed from a sinusoidally time-varying capacitor in shunt with an RLC tank forms an active device.

A precise definition of passive elements is given in [Desoer and Kuh, 1969]. Given a one-port with port voltage $v(t)$ and port current $i(t)$, the one-port is said to be passive if

$$\int_{t_0}^t v(t')i(t')dt' + \mathcal{E}(t_0) \geq 0 \quad (2.1)$$

where $\mathcal{E}(t_0)$ is the energy stored by the one-port at time t_0 . With application of this definition, one can clearly delineate an element as passive or active.

At high frequencies it is usually more convenient to discuss the scattering matrix S [Carlin and Giordano, 1964]. The power dissipated by an arbitrary port of an n -port is given by

$$P_k = P_{ik} - P_{rk} \quad (2.2)$$

where the subscript i denotes incident power and r denotes reflected power. In terms of the incident and reflected waves we have

$$P_k = a_k \bar{a}_k - b_k \bar{b}_k \quad (2.3)$$

summing over all ports we obtain the total power

$$P = \sum_{k=1}^n P_k = \bar{a}^T a - \bar{b}^T b \quad (2.4)$$

but by the definition of the S matrix $b = Sa$ so that

$$P = \bar{a}^T a - \bar{a}^T \bar{S}^T S a = \bar{a}^T (I - \bar{S}^T S) a = \bar{a}^T Q a \quad (2.5)$$

where Q is the dissipation matrix. Note that

$$\bar{Q}^T = \bar{I}^T - \overline{(\bar{S}^T S)}^T = I - \bar{S}^T S = Q \quad (2.6)$$

and so Q is a Hermitian matrix. By definition of passivity, we have

$$P = \bar{a}^T Q a \geq 0 \quad (2.7)$$

Clearly, then, if the matrix Q is positive definite or positive semi-definite, the matrix S corresponds to a passive network. One can also show that this condition implies [Carlin and Giordano, 1964]

$$0 \leq |s_{ij}| \leq 1 \quad (2.8)$$

This can be deduced intuitively in the following manner. Observe that each diagonal entry of the S matrix is the reflection coefficient when all other ports are matched and each off-diagonal component is the transmission coefficient under matched conditions. For a passive network, the conservation of energy implies that the power reflected from any port must be less than the power injected, thus $|\rho|^2 \leq 1$ and the power transmitted similarly must satisfy the same condition, $|\tau|^2 \leq 1$. This implies all matrix elements have magnitude less than or equal to unity and thus reside in the unit circle in the complex plane². An active device consists of a black box with sources, and thus the matrix elements may have magnitude greater than unity. It follows that the real part of the input port impedances may be negative, something that may never occur for a passive network.

1.1 STABILITY AND PASSIVITY

Passivity is closely related to stability [Desoer and Kuh, 1969]. Again, this is clear intuitively as any passive device must be stable by the conservation of energy. In other words, one can never construct an unstable device with purely passive devices. Conditional stability, as with an oscillating LC tank, is possible as long as the initial conditions supply some energy to the tank. It can be shown that a passive circuit is indeed stable and this further implies that any natural frequency of a passive network must lie in the closed left-hand plane, and any $j\omega$ -axis natural frequency must be simple [Desoer and Kuh, 1969].

1.2 RECIPROCITY

Consider the n -port parameters of the black box. If the volume of the black box of Fig. 2.1 is isotropic and encloses no sources, then by the Lorenz reciprocity theorem of electromagnetics it can be shown [Pozar, 1997] that the impedance matrix Z is symmetric. Such a network is called a reciprocal network. A reciprocal network is also described by a symmetric S matrix since in such a case one can show that

$$S = \left(\frac{Z}{Z_0} + I\right)^{-1} \left(\frac{Z}{Z_0} - I\right) = \left(\frac{Z}{Z_0} - I\right) \left(\frac{Z}{Z_0} + I\right)^{-1} \quad (2.9)$$

where $\mathbf{Z}_0$ is the system impedance, usually $50\ \Omega$, and I is the identity matrix. If Z is symmetric, then the symmetry of S follows.

It should be noted that reciprocity has nothing to do with passivity. While many passive networks are indeed reciprocal, the connection is not obvious. Any linear time-invariant RLCM network is reciprocal. In fact, some of the elements may be active and reciprocity is still satisfied. A gyrator, a passive device, is non-reciprocal. The reciprocity theorem in circuits follows from excluding any network with gyrators, dependent and independent sources.

1.3 THE QUALITY OF PASSIVE DEVICES

In general, the complex power delivered to a one-port black box network at some frequency ω is given by [Pozar, 1997]

$$P = \frac{1}{2} \oint_S \mathbf{E} \times \mathbf{H}^* \cdot d\mathbf{s} = P_l + 2j\omega(W_m - W_e) \quad (2.10)$$

where P_l represents the average power dissipated by the network and W_m and W_e represent the time average of the stored magnetic and electric energy, respectively. One can define the input impedance as follows [Pozar, 1997]

$$Z_{in} = R + jX = \frac{V}{I} = \frac{VI^*}{|I|^2} = \frac{P}{\frac{1}{2}|I|^2} = \frac{P_l + 2j\omega(W_m - W_e)}{\frac{1}{2}|I|^2} \quad (2.11)$$

If $W_m > W_e$ the device acts inductively whereas if the opposite is true the device acts capacitively.

An important parameter to consider when discussing passive devices is the quality factor. The quality factor has the following general definition

$$Q = 2\pi \frac{E_{\text{store}}}{E_{\text{diss}}} \quad (2.12)$$

where E_{store} is the energy stored per cycle whereas E_{diss} is the energy dissipated per cycle. Implicit in the above definition is that the device is excited sinusoidally. From (2.11) with T equal to the cycle time

$$Q = 2\pi \frac{(W_m + W_e)}{P_l \times T} = \frac{\omega(W_m + W_e)}{P_l} \quad (2.13)$$

The higher the Q factor, the lower the loss of a passive device. This definition is most pertinent when discussing inductors or capacitors as such devices are meant to store energy while dissipating little to no energy in the process. Thus ideal inductors and capacitors have infinite Q whereas practical devices have finite Q . Applying the above definition to an ideal inductor L where $W_e \equiv 0$ in series with a resistor R , one obtains $Q = \omega L/R$ and similarly to an ideal capacitor C where $W_m \equiv 0$ in series with a resistor, $Q = (\omega CR)^{-1}$.

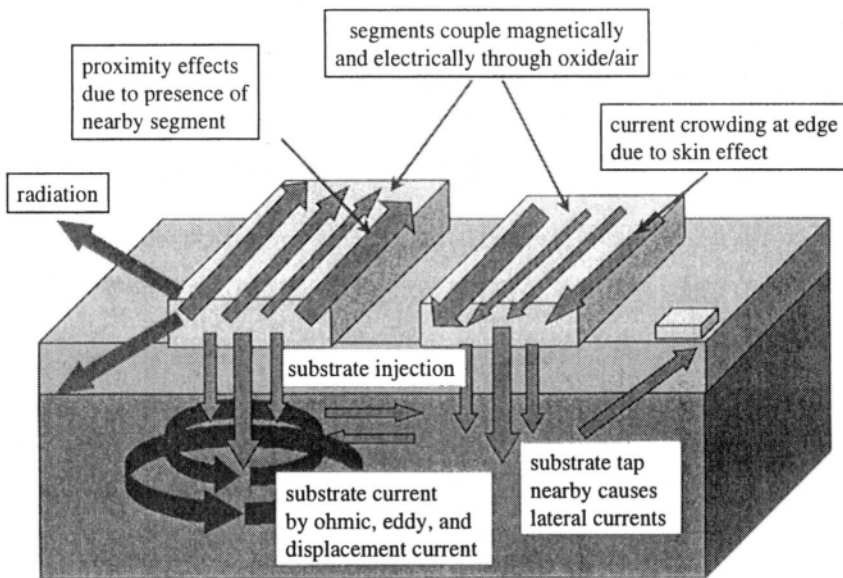


Figure 2.2. Various loss mechanisms present in an IC process.

Physically, the lossy nature of passive devices is rooted in physical phenomena which convert electrical energy into other, unrecoverable forms of energy. Processes which increase entropy are not reversible. For instance, a resistor converts electrical energy into heat. A light bulb converts electrical energy into light and heat. An antenna also converts electrical energy into radiating electromagnetic energy. One can therefore distinguish between passive devices which increase entropy while conserving energy, like a resistor or an incoherent light source, and other devices which conserve energy but do not increase entropy, such as an ideal laser. An ideal laser converts electrical energy into a coherent emission of monochromatic photons. In reality, any physical laser will emit photons with a Lorentzian distribution of energies and thus the entropy of the system increases.

2. LOSS MECHANISMS

The Q factor of integrated passive devices is largely a function of the material properties used to construct the ICs. Specifically, the semiconductor substrate and metal layers used to build the device play the most important roles. The various loss mechanisms are summarized in Fig. 2.2 and discussed further below.

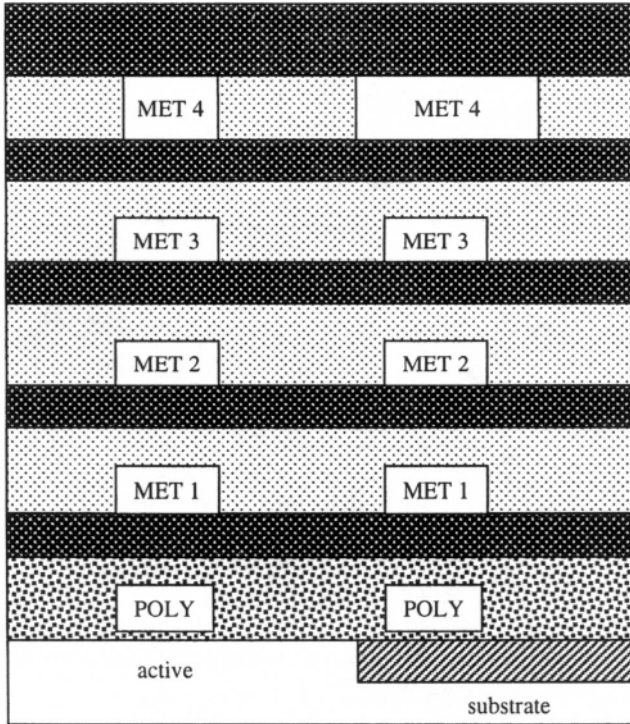


Figure 2.3. Cross-section of metal and polysilicon layers in a typical IC process.

2.1 METAL LOSSES

Passive devices such as inductors and capacitors are constructed from layers of metal, typically aluminum, and polysilicon layers. Hence, the conductivity of such layers plays an integral part in determining the Q factor of such devices, especially at lower frequencies. For instance, a capacitor is constructed by placing two metal conductors in close proximity. Reactive energy is stored in the electric field formed by the charges on such conductors. Since the metal layers are not infinitely conductive, energy is lost to heat in the volume of the conductors. This loss can be represented by a resistor placed in series with the capacitor. Similarly, an inductor is wound using metal conductors of finite conductivity. Most of the reactive energy is stored in the magnetic field of the device, but energy is also lost to heat in the volume of the conductors.

Fig. 2.3 shows a cross-section of the metal layers of a typical modern IC process. Most processes come with three or more interconnection metal layers. This may include one or two layers of polysilicon as well. Some modern CMOS

processes include up to eight metal layers, with the top layer separated from the substrate by $\sim 10\ \mu\text{m}$ of oxide.

Most IC metal layers are constructed from aluminum which has a room temperature conductivity of $\sigma = 3.65 \times 10^7\ \text{S/m}$. Typical metal layers have a thickness ranging from $.5\ \mu\text{m}$ to $4\ \mu\text{m}$, resulting in sheet resistance values from $55\ \text{m}\Omega/\square$ to $7\ \text{m}\Omega/\square$. Even though silver, copper, and gold are more conductive, at $\sigma_{\text{Ag}} = 6.21 \times 10^7\ \text{S/m}$, $\sigma_{\text{Cu}} = 5.88 \times 10^7\ \text{S/m}$, and $\sigma_{\text{Au}} = 4.55 \times 10^7\ \text{S/m}$, aluminum is the more compatible metal in the IC process. Even though Aluminum is prone to spiking and junction penetration [Jaeger, 1993], it is usually mixed with other metals such platinum, palladium, titanium, and tungsten to overcome these limitations. Electromigration in Al is another problem, setting an upper bound on the maximum safe current density. Although electromigration with AC currents is less problematic, it remains one of the important limitations preventing integration of “high-power” passives on Si, such as the matching networks at the output of a power amplifier. The necessary metal width would require excessively large areas resulting in low self-resonant frequencies.

Many IC processes geared for wireless communication applications are now providing a thick top-metal layer option for constructing inductors. Such a metal layer is also useful for high-speed digital building blocks and clock lines and thus this option is widely available in digital processes as well. This top metal layer may also reside on top of an extra thick insulator for minimum capacitance [Kamogawa et al., 1999]. On the other hand, the wealth of interconnection opens up the possibility of designing structures with many different metal layers. This has the added benefit of requiring no extra processing steps as such “3D” interconnection is available with most modern CMOS processes.

At increasingly higher frequencies, even in the absence of the substrate, the current distribution in the metal layers changes due to eddy currents in the metallization, also known as skin and proximity effects, current constriction, and current crowding. At any given frequency, alternating currents take the path of least impedance. Currents tend to accumulate at the outer layer or skin of conductors since magnetic fields of the device penetrate the conductors and produce opposing electric fields within the volume of conductors. When the effective cross-sectional area of the conductors decreases at increasing frequencies, the current density increases, converting more energy into heat. For an isolated conductor, the magnetic fields originate from the conductor itself (the self-inductance). This increase in AC resistance is known as skin effect and typically follows a $\sqrt{f}$ functional dependence. This rate of increase can be traced to the effective depth of penetration δ of the current since the effective area is

a function of the skin depth³

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \quad (2.14)$$

In a multi-conductor system, the magnetic field in the vicinity of a particular conductor can be written as the sum of two terms, the self-magnetic field and the neighbor-magnetic field⁴. Thus, the increase in resistance of any particular conductor can be attributed not only to skin effect but also to proximity effects, the effect of nearby conductors. If nearby conductors enhance the magnetic field near a given conductor, the AC resistance will increase even further and this is the case for a spiral inductor. On the other hand, if the nearby fields oppose the field of a given conductor, as is the case in a transformer, the AC resistance will decrease as a result.

2.2 SUBSTRATE INDUCED LOSSES

Integrated passive devices must reside near a conductive Si substrate. The substrate is a major source of loss and frequency limitation and this is a direct consequence of the conductive nature of Si as opposed to the insulating nature of GaAs. The Si substrate resistivity varies from **10 kΩ-cm** for lightly doped Si (**10¹³ atoms/cm³**) to **.001 Ω-cm** for heavily doped Si (**10²⁰ atoms/cm³**). In fact, to combat these substrate induced losses, some researchers propose removing the substrate from under the device by selective etching [Chang et al., 1993] [Lopez-Villegas et al., 2000].

The conducting nature of the Si substrate leads to various forms of loss, namely conversion of electromagnetic energy into heat in the volume of the substrate. To gain physical insight into the problem, we can delineate between three separate loss mechanisms. First, electric energy is coupled to the substrate through displacement current. This displacement current flows through the substrate to nearby grounds, either at the surface of the substrate or at the back-plane of the substrate. Second, induced currents flow in the substrate due to the time-varying magnetic fields penetrating the substrate. These magnetic fields produce time-varying solenoidal electric fields which induce substrate currents. These currents are shown in Fig. 2.4 for the case of a spiral inductor. Note that electrically induced currents flow vertically or laterally, but perpendicular to the spiral segments. Eddy currents, though, flow parallel to the device segments⁵.

Finally, all other loss mechanisms can be lumped into radiation. Electromagnetically induced losses occur at much higher frequencies where the physical dimensions of the device approach the wavelength at the frequency of propagation in the medium of interest. This frequency is actually difficult to quantify due to the various propagation mechanisms of the substrate. For instance, if we consider propagation into air, the free-space wavelength is the appropriate

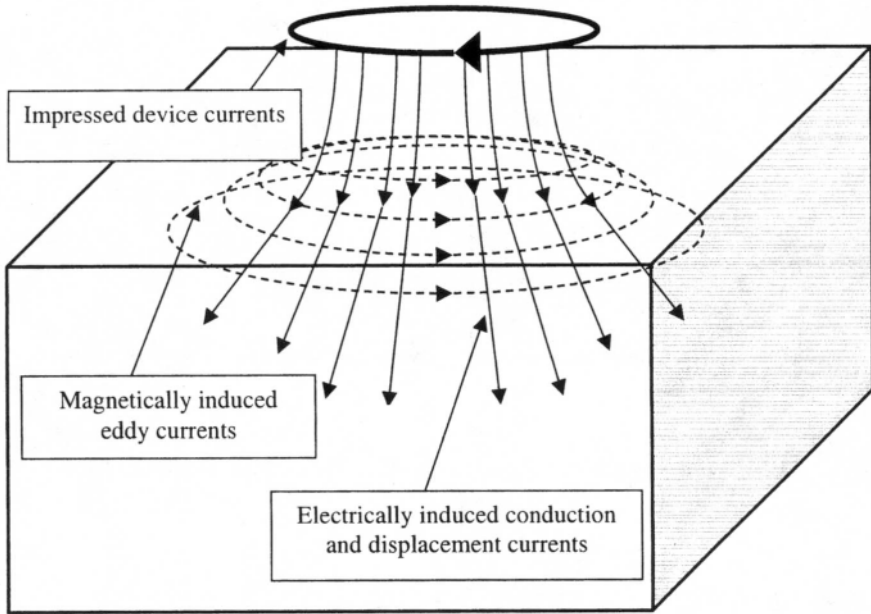


Figure 2.4. Schematic representation of substrate currents. Eddy currents are represented by the dashed lines and electrically induced currents by the solid lines.

factor. Even at 10 GHz, the wavelength in air is 3 cm, much larger than any RF inductor or capacitor. Even at 100 GHz, the wavelength is now 3 mm, still much larger than any device at this frequency. Thus, we can safely ignore the electromagnetic propagation into the air.

Efficient electromagnetic propagation into the substrate, though, occurs at lower frequencies due to the lower propagation speed, roughly at a factor of $\sqrt{\epsilon_{\text{Si}}}$ lower due to the diamagnetic nature of Si. Since $\epsilon \approx 11.9$ in Si, this is slightly slower from propagation in air. Furthermore, due to the lossy nature of the substrate, waves traveling vertically into the surface of the substrate are heavily attenuated. Waves traveling along the surface of the substrate, though, can propagate partially in the lossless oxide and partially in the substrate. For a lightly doped substrate, the wave propagation behaves like a “quasi-TEM” mode. As the substrate is made heavily conductive, the wave is constrained to the oxide and the substrate acts like a lossy ground plane. This is the so-called “skin effect” mode of propagation [Hasegawa et al., 1971]. There is a third kind of possible excitation, the “slow-wave” mode of propagation, where the effective speed of propagation is orders of magnitude slower than propagation in free space [Hasegawa et al., 1971].

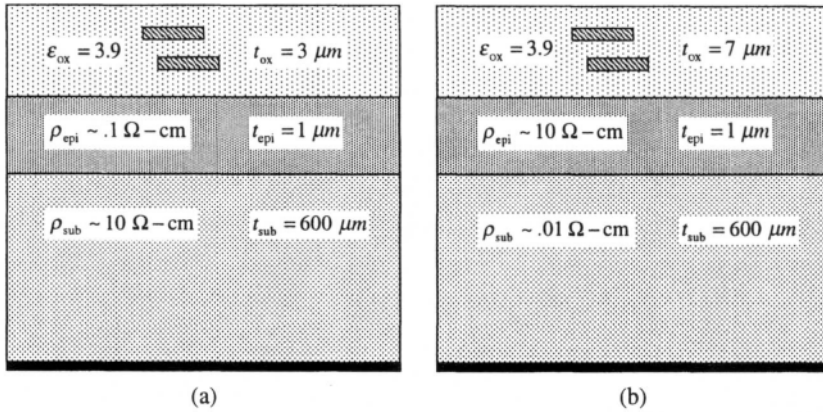


Figure 2.5. Cross-section of typical (a) bipolar and (b) CMOS substrate layers.

2.2.1 SI IC PROCESS SUBSTRATE PROFILE

In Fig. 2.5 typical bipolar and CMOS process substrate profiles are shown. Each substrate consists of one or more layers of Si or a compatible material⁶. Layers of varying conductivity are added to the bulk substrate by various *g* processes, such as diffusion, chemical vapor deposition and growth, epitaxy, and ion implantation. Various layers of oxide (**SiO₂** for instance) and polyimide are also grown to provide insulation from the substrate and between metal layers.

In general, the more conductive the substrate layers, the more detrimental the resulting losses. It is therefore no surprise that intrinsic Si substrates⁷ result in the lowest losses [Park et al., 1997b]. Due to the close proximity of the Si substrate to the inductors and transformers residing in the metal layers, the case of an infinitely conductive substrate is also problematic. For a heavily conductive substrate, the magnetic and electric fields do not penetrate the substrate appreciably and even though no substrate induced losses occur, the surface currents flowing in the substrate, acting like “ground-plane” currents, produce opposing magnetic fields which tend to drive the inductance value of coils to low non-usable values.

Therefore, given the choice, designers of ICs and process engineers should ensure that as few as possible conductive substrate layers appear under or near an inductor. This is unfortunately not always possible due to planarization constraints. Furthermore, the thickest possible oxide should be realized under the device to minimize the substrate capacitance. This not only minimizes the losses, but also maximizes the self-resonant frequency of the device. In the limit, self-resonance will occur due to interwinding capacitance as opposed to substrate capacitance. Since interwinding capacitance can be controlled by

increasing the metal spacing, this gives the IC designer more control over the passive device behavior.

Most bipolar and BiCMOS substrates come with a standard $10\text{--}20\ \Omega\text{-cm}$ substrate. With this value of resistivity, electrically induced losses dominate the substrate losses in the $1\text{--}10\ \text{GHz}$ frequency range [Ruehli, 1972]. This is also the case for bulk CMOS substrates with the same range of resistivity. In such a case, one must ensure that no conductive n - or p -wells appear below the device. This may require a special mask to block the dopants in the well creation process, especially for a twin-well CMOS process. To minimize the chance of latch-up, many modern CMOS processes begin with a heavily conductive thick substrate about $700\ \mu\text{m}$ thick and grow a thin epitaxial layer of resistive Si on the surface to house the wells. This is unfortunate for RF/microwave circuits as the bulk substrate can be as conductive as $10^4\ \text{S/m}$ and this can be a major source of substrate induced losses due to eddy currents.

The back-plane of the substrate may or may not be grounded. Even if it is physically grounded for DC signals, AC signals are constrained to flow within several skin depths δ and this factor is a strong function of the conductivity. For heavily conductive substrates, currents are constrained to flow at the surface of the substrate at high frequencies whereas for moderately conductive substrates currents flows deep into the substrate and into the back-plane ground.

A physical ground may be realized if the die (chip) resides in a package with a conductive ground plane, or if the die is bonded directly onto a board, and a conductive epoxy cement glue is used. Although the epoxy is not conductive, metals can be mixed in to produce a conductive solution. In the modeling of the substrate this can be an important factor in enforcing the boundary conditions surrounding the chip.

Unless the substrate thickness is reduced substantially, the conductive back-plane ground is sufficiently distant not to appreciably influence the electromagnetic behavior of the inductor. On the other hand, some packages use “down-bonds,” bond wires from the Si die to the package grounded “paddle”. To minimize the bond wire length, the substrate thickness is reduced in post-processing steps. This has further benefits for a packaged power amplifier since a thinner substrate also has better thermal conductivity. For such a thin, moderately conductive grounded substrate, one must take into account ground “image” currents which can reduce the inductance value and serve as a further loss mechanism [Krafcsik and Dawson, 1986]. If the substrate is sufficiently conductive such that the skin depth δ is much less than the substrate thickness, then image currents will be confined to flow at the substrate surface.

3. DEVICE LAYOUT

In this section we will discuss various ways to lay out inductors using the planar metallization layers of a typical IC process. Off-chip inductors are usu-

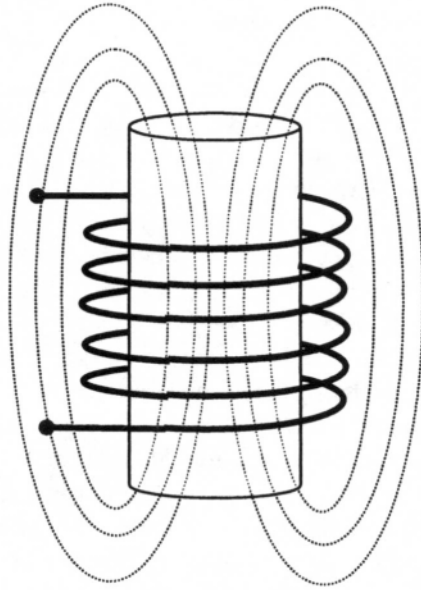


Figure 2.6. The typical coil inductor.

ally realized as a solenoidal coil or toroid, as shown in Fig. 2.6. Each additional turn adds to the magnetic field in phase with the previous turn. The magnetic energy is stored mostly in the inner core of each winding. The inductance is largely a function of the area of the loop and the number of turns in the winding typically resulting in an N^2 dependence.

3.1 PLANAR INDUCTOR STRUCTURES

Since on-chip inductors are constrained to be planar, the typical solution is to form a spiral, as shown in Fig. 2.7. Since some IC processes constrain all angles to be 90° , a square version of the spiral, shown in Fig. 2.8, is a popular alternative. A polygon spiral, as shown in Fig. 2.9, is a compromise between a purely circular spiral and a square spiral.

In designing integrated circuits it is sometimes convenient to tap an inductor at some arbitrary point. While this is certainly possible, as more than one metal layer is present, it is sometimes necessary to tap a spiral in the center, especially for differential circuits. In a spiral it is difficult to find such a symmetric center point since the electric fields on the outer turns tend to fringe and thus the “inductive” center does not correspond to the “capacitive” center. Also, the “inductive” center does not correspond to the “resistive” center due to the non-uniform mutual magnetic coupling. To solve this problem, some researchers

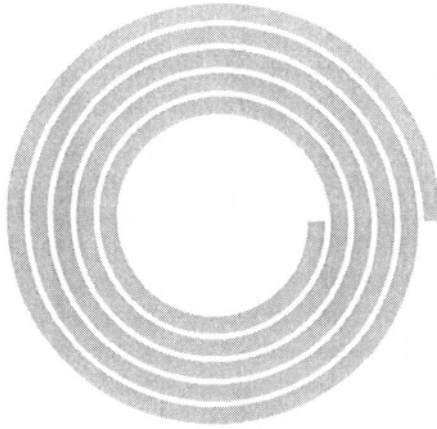


Figure 2.7. A circular spiral inductor.

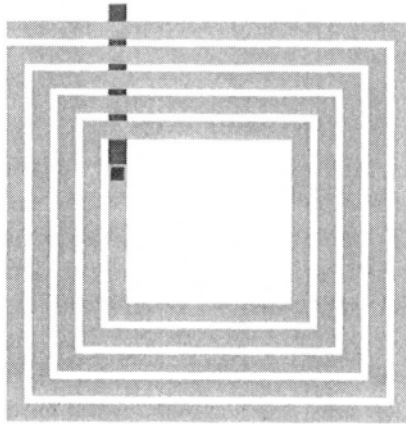


Figure 2.8. A square spiral inductor.

have proposed symmetric structures, such as that shown in Fig. 2.10. Note that each turn involves a metal-level interchange, a process that requires vias. A different center-tapped structure proposed by [Kuhn et al., 1995] requires only one metal interchange. This structure is very similar to a inter-digitated planar transformer structure shown in Fig. 2.13. These structures have a natural geometric center which coincides with the electrical center point. This is needed in differential circuits as such points can be grounded or connected to supply

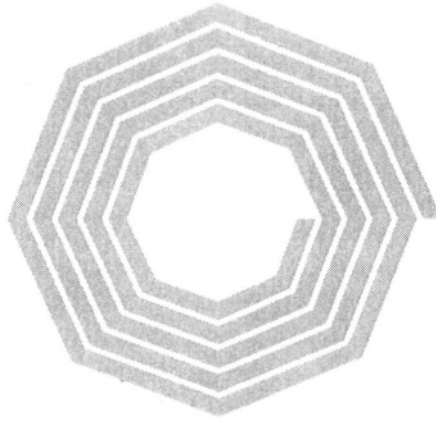


Figure 2.9. A polygon spiral inductor.

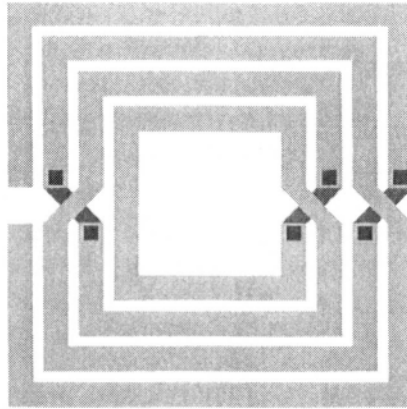


Figure 2.10. A symmetric spiral inductor.

without disturbing the differential signal. Circular or polygon versions are also possible, as shown in Fig. 2.11.

3.2 NON-PLANAR INDUCTOR STRUCTURES

Up to now we have only considered planar structures even though modern IC processes offer many metal layers. Two simple approaches in utilizing the metal layers are to connect multiple spiral inductors in series or in shunt. While N spirals in series increase the series resistance by a factor of approximately N

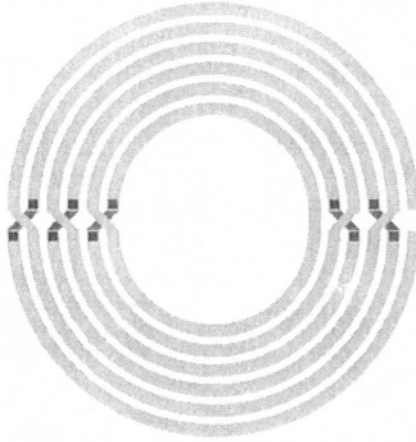


Figure 2.11. A symmetric polygon spiral inductor.

(neglecting via resistance), the inductance value increases faster due to the mutual magnetic coupling. At low frequencies where the current flowing through each series connected spiral I_j is equal, the effective inductance of N series connected coupled inductors is

$$L_{se} = \sum_{i=1}^N L_i + 2 \sum_{i=1}^N \sum_{j \neq i}^N M_{ij} \quad (2.15)$$

where M_{ij} is the mutual magnetic coupling between each series connected spiral i and j . Thus, the series connection approaches an N^2 increase in inductance and the Q factor can potentially increase by a factor of N for the case of perfectly coupled spirals ($k = 1$).

Alternatively, in the shunt connection, the series resistance drops by a factor of N (assuming equal resistivity in each metal layer and uniform current distribution among the coils) whereas the inductance of mutually coupled inductors drops to⁸

$$L_{sh} = \frac{1}{\sum_{i=1, j=1}^N K_{ij}} \quad (2.16)$$

where the matrix K is the inverse of the partial inductance matrix M . This result certainly agrees with the case of a diagonal matrix M corresponding to zero coupling since in such a case we have the familiar result for parallel inductors

$$L_{sh, k=0} = \frac{1}{\sum_{i=1}^N \frac{1}{M_{ii}}} \quad (2.17)$$

For the case of two coupled inductors we have a simpler relation

$$L_{sh} = \frac{1}{2} \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M} \quad (2.18)$$

For the case of perfectly coupled equal value inductors, with $k = +1$, the above result yields $L_{sh} = L$. For the general case, the matrix M is singular but by symmetry the current flowing through all inductors is equal so the voltage across the j th inductor gives

$$V_j = \sum_{k=1}^N sM_{jk} I_k = \frac{I}{N} \sum_{k=1}^N sM_{jk} = \frac{I}{N} sL \sum_{k=1}^N 1 = sLI \quad (2.19)$$

and so we have

$$L_{sh} = L_1 = L_2 = \dots = L_N \quad (2.20)$$

In this limit, the Q factor also improves by a factor of N due to the drop in series resistance. In practice, both the series and shunt connection offer a Q improvement close to the theoretical limit due to the tight coupling achievable in the on-chip environment. These benefits, though, only occur at low frequencies where the above assumptions hold.

At high frequencies, both approaches are liable to reduce the Q factor over the case of a single layer coil due to the capacitive and substrate effects. The series connection suffers from high interwinding capacitance which lowers the self-resonance frequency lowering the maximum frequency of operation of the device. The shunt connection moves the devices closer to the substrate where capacitive current injection into the substrate may dominate the loss of the device.

Another approach is to attempt to realize a lateral coil on-chip by using the top and bottom metal layers and vias as the side. This approach has been successfully demonstrated in [Young et al., 1997] using special post-processing steps to realize sufficient cross-sectional area in the coil. This approach has the added advantage of positioning the magnetic fields laterally to the substrate where eddy currents are reduced. In a vertical coil or spiral, the magnetic field is strongest at the center of the coil. Due to the finite conductivity of the substrate, these changing magnetic fields leak into the substrate and produce eddy currents. Eddy currents can be a significant source of loss and this technique might be an effective method to combat this loss mechanism. Standard monolithic integration, though, has failed to produce a coil with sufficient cross-sectional area to produce significant Q . Some innovative strategies around this are to employ a combination of metal and bond wires to realize the coil [Lee et al., 1998b]. The work of [Lee et al., 1998b] claims tight tolerance on the inductance value which is a primary concern of using bond wires alone [Craninckx and Steyaert, 1995].

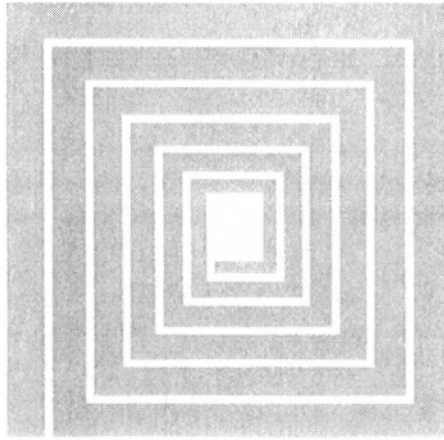


Figure 2.12. A tapered spiral inductor.

3.3 TAPERED SPIRALS

A tapered spiral is shown in Fig. 2.12. The metal pitch and spacing are varied to minimize the current constriction at high frequency [Niknejad, 1997, Lopez-Villegas et al., 2000]. Current constriction, or skin effect, is non-uniform as a function of the location in the spiral due to the non-uniformity of the magnetic field. At low frequencies the current is nearly uniform whereas at high frequency non-uniform current flows due to proximity effects.

The magnetic field is strongest in the center of the spiral [Craninckx and Steyaert, 1997] and thus the time-varying magnetic field produces eddy currents of greatest strength in the volume of conductors near the center of the device. Since at high frequency current constriction limits the current to the outer edges of the conductors, conductor width does not have as strong an influence on minimizing metal losses as at low frequency. For this reason [Craninckx and Steyaert, 1997] advocate removing the inner turns to produce a “hollow” spiral. Another approach is to decrease the width of the inner turns and to effectively move these turns closer to the outer edge. This approach contrasts with the approach suggested by [Lopez-Villegas et al., 2000] where the sum of the metal pitch and spacing, $W + S$, is kept constant.

Tapering is most effective when substrate losses are negligible, as in the case of an insulating substrate. This stems from the fact that current constriction dominates the metallization losses at high frequencies when the substrate losses are also significant. On the other hand, tapering can be an effective means of increasing the self-resonant frequency of a device by decreasing the cross-sectional area of the device.

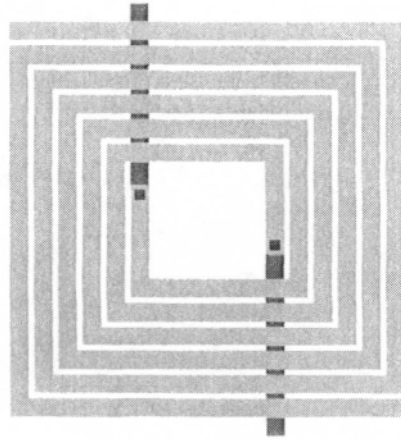


Figure 2.13. A planar square spiral transformer.

3.4 TRANSFORMERS

On-chip transformers are realized very similarly to inductors. To maximize the coupling factor k , two inductors can be interwound as shown in Fig. 2.13. Polygon spirals can be similarly interwound to form transformers. These transformers have equal turns ratio at the primary and secondary. Since the turns ratio n is given by

$$n = k \sqrt{\frac{L_2}{L_1}} \tag{2.21}$$

one way to realize $n \neq 1$ is to alter the number of turns and metal pitch in the secondary. In addition, to lower the losses in the secondary, turns may be connected in shunt [Long and Copeland, 1997]. Typical practical coupling values in the range of $.6 < k < .8$ can be achieved with planar spirals. Metal-metal transformers utilizing two or more metal layers can save area, but cause asymmetry and increased capacitive coupling between the primary and secondary. The asymmetry can be reduced by utilizing a structure such as the one in Fig. 2.14.

If center-tapped transformers are desired, such as in a balun, a structure such as Fig. 2.15 serves well. This structure is formed by interwinding two center-tapped coils of Fig. 2.10.

3.5 SHIELDED STRUCTURES

In an attempt to shield a device from substrate losses, researchers have proposed building a shield with lower metal layers or polysilicon layers to block

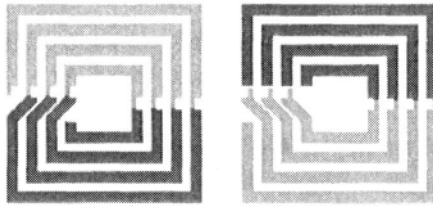


Figure 2.14. An expanded view of a non-planar symmetric spiral transformer. The primary is shown on the left and the secondary on the right. These inductors actually reside on top of one another.

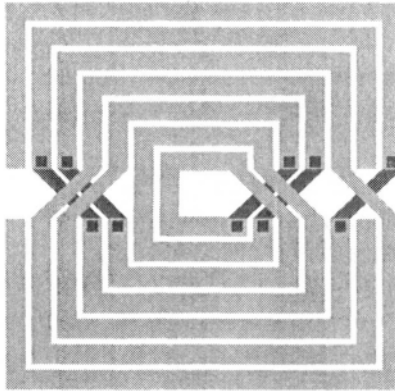


Figure 2.15. A planar symmetric balun transformer.

electromagnetic energy from coupling to the substrate [Yue and Wong, 1997]. While electrostatic shielding works well for capacitors and RF pads, especially at “low-frequencies”, the shield must be patterned in the case of inductors so as to avoid or reduce the effects of eddy currents. Due to the close proximity of the device and the shield, using solid metallization would allow “image” eddy currents to flow which would produce an opposing magnetic field. This would reduce the device magnetic energy storage and hence the Q factor. A patterned shield, similar to Fig. 2.16, only allows shield currents to flow perpendicular to the conductive paths of a spiral inductor, thereby preventing the majority of eddy currents which flow parallel to the device⁹.

The effects of a shield, or any other “grounding” structure, can be analyzed with the techniques presented in this research. At first glance a patterned shield seems like a very effective means of improving the device Q . This, however,

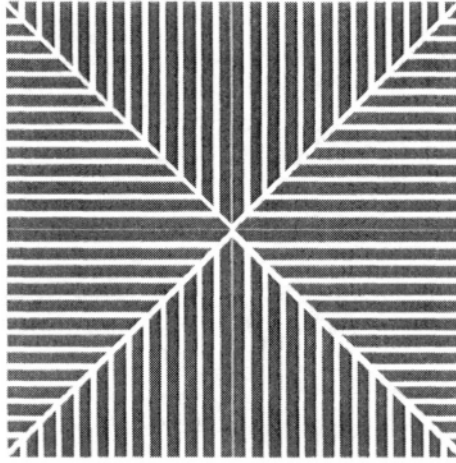


Figure 2.16. A patterned ground shield.

must be carefully examined for each process and product. There are many obvious problems with a shield, such as drastically reduced self-resonant frequency. There are also more subtle problems with a shield.

To see this, consider the inductor layout as a lossy inductor and a parasitic lossy capacitor, C_s in series with a loss resistor R_s . This frequency-independent representation is certainly valid as the network two-port parameters can be transformed into this equivalent circuit uniquely at a given frequency. In practice, the addition of a few elements, such as a lossless interwinding capacitor, broadbands the model, especially below self-resonance [Niknejad, 1997]. Then the action of the shield is to effectively increase the Q_C factor of the capacitor portion of the equivalent circuit. Consider a series to parallel transformation of this lossy capacitor into C_p in shunt with R_p

$$R_p = (1 + Q_C^2)R_s \quad (2.22)$$

$$C_p = \frac{Q_C^2}{1 + Q_C^2}C_s \quad (2.23)$$

Suppose that without a shield the Q_C factor of this capacitor is very low, $Q_C \ll 1$, such that

$$R_{low} \approx R_s \quad (2.24)$$

$$C_{low} \approx Q_C^2 C_s \quad (2.25)$$

If R_{low} is then already larger than the parallel equivalent inductor loss resistor, then this capacitor plays a minor role in determining the overall Q and shielding will actually deteriorate the performance of the device. Note that since

$C_{low} \ll C_s$, the effective shunt capacitance is small and does not lower the self-resonant frequency of the device. Clearly, in this case shielding does not help. Now consider the other extreme where the resistor R_{low} actually loads the tank significantly. Then clearly increasing the capacitor Q_C factor helps since for $Q_C \gg 1$

$$R_{high} \approx Q_C^2 R_s \quad (2.26)$$

$$C_{high} \approx C_s \quad (2.27)$$

This occurs, on the other hand, at the expense of lowered self-resonance since now the parasitic capacitor loads the tank. So we see the shield may potentially improve the overall tank Q but at the cost of reducing the usable frequency range of the device. Another approach, discussed in [Burghartz et al., 1997], surrounds the device with an open halo of substrate contacts. This has the added benefit of increasing the capacitor Q_C without loading the tank capacitance significantly. Measurements by other researchers have also corroborated these findings [Yoshitomi et al., 1998].

Another potential problem with the shield arises due to finite non-zero ground inductance. Since most packaged ICs suffer both package and bond wire inductance, the actual zero potential resides off-chip and there is considerable “ground bounce” on-chip. A typical IC has several inductors and transformers and if they are shielded, they are all effectively tied to a common non-zero impedance point. Thus a parasitic coupling path exists from device to device.

For instance, in an amplifier, this intra-block leakage can either lower the gain (as negative feedback) or cause instability (as positive feedback). Inter-block coupling, on the other hand, can produce spectral leakage and spurs, jamming and reduced SNR (gain compression), or mode-locking.

Any IC, of course, suffers from parasitic substrate coupling but shielding increases the substrate capacitance value and removes the resistive isolation between the devices.

3.6 VARACTORS (REVERSE-BIASED DIODES)

Varactors, or variable capacitors, are usually constructed as back-biased diodes. Diodes are realized as junctions between p -type and n -type doped regions of Si. Briefly, the presence of an n -type region abutting a p -type region creates a large concentration gradient which leads to diffusion. This diffusion forms the so-called “space-charge” or “depletion” region, a charged volume of space surrounding the junction. The charge of this region is due to the charge of immobile dopant sites. Donor or acceptor atoms are easily ionized at room temperature resulting in free mobile carriers. The diffusion process is balanced by the conduction current resulting from the built-in electric field since the charge buildup from the ionized immobile dopants produces an electric field

opposing the diffusion. Thus a natural barrier is formed against charge crossing the junction boundary.

If the diode is forward biased beyond a threshold, carriers obtain sufficient energy to cross the barrier. On the other hand, if the diode is reverse-biased, no DC conduction current flows. In reality, a small current will flow even under reverse-biased conditions. One contribution to these “leakage currents” is due to minority carriers which are created on average within a diffusion length of the junction. These carriers are actually propelled by the built-in electric field and cross the junction. Note that this current is relatively bias-independent¹⁰.

While little to no DC current flows, AC displacement currents can flow since the reverse-biased diode acts very much like a capacitor. The thin space-charge region serves as the “insulator” and the n -type and p -type Si regions act as capacitor plates. Electric energy is stored in the built-in field of the space-charge region. Under an abrupt junction assumption, the depletion region thickness is given by [Neudeck, 1989]

$$d_j = \left[\frac{2K_S \epsilon_0 (V_{bi} - V_A) (N_A + N_D)}{q N_A N_D} \right]^{1/2} \quad (2.28)$$

N_D and N_A are the donor and acceptor volume densities and V_{bi} is the built-in potential given by

$$V_{bi} = \frac{kT}{q} \ln \left[\frac{N_D N_A}{n_i^2} \right] \quad (2.29)$$

where complete ionization of the donors and acceptor is assumed. Note that under reverse-biased conditions, the spacing d_j is a function of the applied voltage $V_A < 0$. This effect can be exploited to produce a variable capacitor. The physical origin of the dependence of d_j on V_{rev} is simply due to the fact that increasing the voltage difference increases the electric field which requires more charge which in turn comes from extending the space charge region. If $N_D \gg N_A$ then the fractional increase in d_j from the donor side is small compared to the acceptor sites. The opposite, of course, also applies. Thus, in such a case the series resistance of the diode in reverse bias will be dominated by the acceptor side, or the p -type Si, due to its higher resistivity. Note that if both the donor and acceptor densities are increased in an attempt to lower the series losses, the capacitance gets large. While this is desirable, the breakdown voltage of the reverse-biased junction decreases. For avalanche breakdown we have [Neudeck, 1989]

$$V_{BR} = \left(\frac{\epsilon_C T^2 \epsilon_r}{2q} \right) \left[\frac{N_A + N_D}{N_A N_D} \right] \quad (2.30)$$

The same applies for Zener breakdown since decreasing d_j increases the probability that a carrier will tunnel through the potential barrier. Since the operating

voltage of ICs is reducing, a proportional decrease in the breakdown voltage is tolerable allowing lower series resistance and thus higher Q values to be realized.

The equivalent capacitance of a junction with cross-sectional area A is thus given by

$$C_j = \frac{\epsilon_r \epsilon_0 A}{d_j} = \frac{\epsilon_r \epsilon_0}{\left[\frac{2K_S \epsilon_0 (V_{bi} - V_A)}{q} \frac{(N_A + N_D)}{N_A N_D} \right]^{1/2}} \quad (2.31)$$

this can be rewritten as

$$C_j = \frac{C_{j0}}{\left[1 - \frac{V_A}{V_{bi}} \right]^m} \quad (2.32)$$

where C_{j0} is the junction capacitance for the zero applied bias case, $V_A = 0$. The factor m is equal to $1/2$ for an abrupt junction but takes on the value of $1/3$ for a linearly graded junction. For real junctions, one finds that $1/3 < m < 1/2$.

A pertinent factor when designing VCOs and filters with variable cutoff is the derivative of (2.32) with respect to the applied voltage V_A

$$K_{CV} = \frac{C_{j0} m}{V_{bi} \left(1 - \frac{V_A}{V_{bi}} \right)^{m+1}} \quad (2.33)$$

Increasing this factor is important for maximizing the change in capacitance for a change in the reverse-biased voltage. This maximizes the tuning range of an LC tank, for instance, since

$$\frac{d\omega}{dV} = \frac{-K_{CV}}{2C_j} \omega_0 \quad (2.34)$$

where $\omega_0 = \sqrt{1/LC_j}$.

3.7 MOS CAPACITORS

Another technique to realize a variable capacitor is through an MOS capacitor. The MOS capacitor has four distinct regions of operation: accumulation, depletion, weak inversion, and strong inversion. In accumulation mode, the capacitance is equal to the oxide capacitance

$$C_{acc} = C_{ox} = \frac{\epsilon_r \epsilon_0 A}{t_{ox}} \quad (2.35)$$

where t_{ox} is the gate oxide thickness and A is the capacitor plate area. This assumes that majority carrier distribution equilibrates much faster than the period of the applied signal. We also assume that all the charge resides at the surface of the substrate (delta-function approximation for charge density) and we neglect the fringing fields. In reality, the charge distribution will not peak

at the surface but slightly away from the surface due to quantum mechanical considerations.

In depletion mode, majority carriers at the surface of Si are repelled by the applied electric field and the region is thus depleted of mobile carriers. A depletion region forms in a similar manner to the reverse-biased junction diode considered previously. The capacitance from the gate to the substrate, therefore, has two components, an oxide capacitance in series with a depletion capacitance [Pierret, 1990]

$$C_{dep} = \frac{C_{acc}C_{dep}}{C_{acc} + C_{dep}} = \frac{C_{ox}}{1 + \frac{\epsilon_{r,SiO_2}d_j}{\epsilon_{r,Si}t_{ox}}} \quad (2.36)$$

As the channel region begins to invert, minority carrier charge accumulates at the surface and the capacitance once again approaches the C_{ox} value. This assumes that the rate of minority carrier generation is sufficiently fast to follow the time-varying AC signal. On the other hand, if a MOSFET-C structure is used instead, a large source of minority carrier charge is available from the surrounding source and drain regions. Between inversion and depletion, or in weak inversion, the situation is more complicated as an incremental increase in the applied voltage can result in new field lines terminating on both immobile charges (by an increase in the depletion junction depth) and terminating on newly generated minority carriers.

In the weak inversion region, the capacitance changes rapidly from C_{dep} to C_{ox} due to the exponential build-up of charge at the surface. This results in a very large K_{CV} factor. The quality factor of such a capacitor is limited mainly by the gate series resistance and can be shown to be approximately equal to $R_G/3^{11}$.

3.8 RESISTORS AND CAPACITORS

Resistors can be implemented in several ways but all essentially involve moving current through a length of material with relatively high resistivity. In a standard bipolar process, diffusion resistors are common. The resistance value can be varied by the application of a bias such as in base-pinch and epitaxial pinch resistors [Gray and Meyer, 1993]. In a standard MOS process we also find diffusion resistors, polysilicon resistors, well-resistors, and the MOS device itself as variable resistors. In a modern bipolar, BiCMOS, or MOS process, most of the above options are available.

Capacitors are realized as either MOS capacitors, as poly-poly "metal" capacitors, metal-insulator-metal (MIM) capacitors, and as poly-diffusion capacitors. For RF applications MIM capacitors are preferred since they result in the lowest losses. Even though standard metal interconnection can be used to construct MIM capacitors, this has two negative consequences. First, it will result in a large uncertainty in the capacitance value due to wide oxide thickness variation

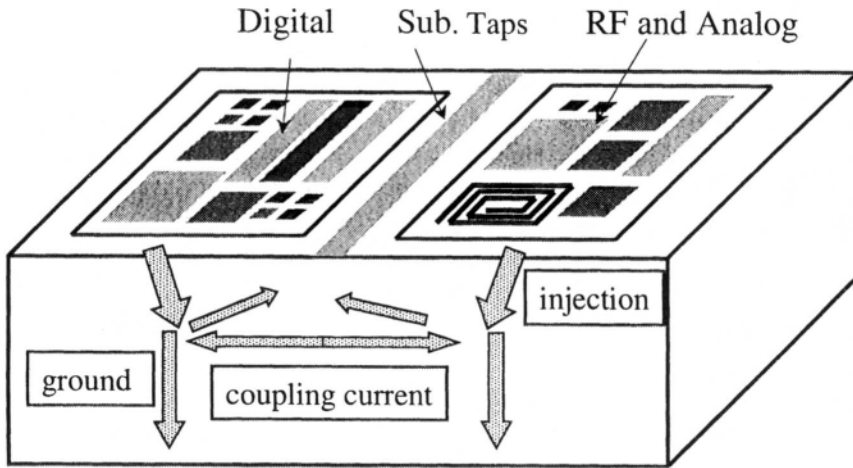


Figure 2.17. Substrate coupling in a mixed-signal system on a chip.

across the wafer. Second, the capacitance value per unit area will be very small due to the thick oxide separating the metal layers. A special MIM capacitor constructed with a well-controlled thin oxide is therefore preferred.

Resistors and capacitors have always been a part of the standard IC process. Thus, great effort has already gone into the analysis and modeling of such structures at lower frequencies. At higher frequencies, though, these structures have many non-ideal effects which must be taken into consideration, such as substrate coupling, self-resonance, and inductance. In this work we will focus on a general interconnection of metal structures above a lossy Si substrate and this generality will allow us to apply our analysis technique to inductors as easily as to capacitors, transformers, and resistors.

4. SUBSTRATE COUPLING

An issue that permeates this research is substrate coupling. Figure 2.17 illustrates the various substrate coupling mechanisms present in an IC environment. Current is injected into the substrate through various mechanisms. Physically large passive devices such as inductors, capacitors, transformers, interconnect and bonding pads inject displacement current in the substrate. This current flows vertically and horizontally to points of low potential in the substrate, such as substrate taps and the back-plane ground. This current couples to other large passive structures in a similar manner.

Active devices also inject current into the substrate, directly and capacitively. Since most active devices are isolated from the substrate by either reverse-biased

pn junctions or oxide, capacitive substrate current injection and reception occur at high frequencies. Direct current can also be injected into the substrate due to hot electron effects. In a short-channel MOS transistor, for instance, electron-hole pair creation takes place in the high-field pinch-off region near the drain due to collisions. The electric field lines lead one set of the carriers into the substrate. Under high field conditions, a multiplication process (avalanche) can also lead to additional hole-pair creation and result in substantial currents.

Coupling between sensitive analog nodes can lead to instability or gain reduction. Furthermore, in a mixed signal IC the coupling between analog and digital portions of the chip can be very problematic. Digital gates switch in a pseudo-random manner and each gate transition results in some energy transfer to the substrate. This energy can couple to sensitive analog nodes and result in reduced signal-to-noise (SNR) ratios.

Though careful layout techniques and differential operation minimize them, these effects can never be totally eliminated or ignored in the design of mixed-signal ICs. Substrate coupling is treated extensively in [Gharpurey and Meyer, 1996]. In this book we draw from an extension of this work, presented in [Niknejad et al., 1998], to analyze passive device substrate coupling.

Notes

- 1 This depends on the I-V curve of a diode. A tunnel diode can certainly be biased as to supply energy, becoming an active device.
- 2 This is a necessary condition for a passive device. However, this condition alone is not sufficient since power gain may occur for a non-matched load or source impedance.
- 3 This is not a rigorous argument since the skin-depth concept of surface impedance applies strictly to a semi-infinite conductor.
- 4 This is due to the linearity of Maxwell's Equations.
- 5 In general the eddy currents are solenoidal whereas the displacement and conductive currents are curl free
- 6 By this we mean the crystal structures of the adjacent layers are compatible.
- 7 By intrinsic we mean no intentional dopants are introduced into the substrate and the only conduction occurs through thermionic emission into the conduction band.
- 8 This result will be established in Chapter 5.
- 9 Current distributions with zero curl lead to zero magnetic fields.
- 10 Consider the current associated with a stream of suicidal lemmings. Given that the cliff is sufficiently high, the suicide rate of lemmings is independent of the height of the cliff.
- 11 See Appendix A.

Chapter 5

INDUCTANCE CALCULATIONS

1. INTRODUCTION

In this chapter we will define inductance, calculate the low frequency inductance of several common configurations of conductors, and extend the results of our calculations to high frequency.

Up until recently, the calculation of inductance has received relatively little attention from the integrated circuit community. Only very specialized fields, such as power engineering, have dealt directly with inductors. The reason for this is simply related to the relatively minor role that inductors have played at lower frequencies, especially in the IC environment. In such cases, parasitic capacitance plays a dominant role in determining circuit behavior whereas the effects of parasitic inductance are minor. The physical origin of this stems from the relatively small size of integrated circuits. The typical inductance associated with long integrated circuit metal traces is on the order of 1 nH, a small enough value of inductance as to produce negligible reactance at typical IC frequencies less than 100 MHz. Today, RF, microwave, and digital ICs are operating at 1 - 10 GHz and these inductive effects are no longer negligible.

Comparatively, magnetic forces tend to have longer range effects than electric forces. This can be attributed to the absence of magnetic monopoles. Whereas electric field lines terminate on charges in nearby conductors and the substrate, magnetic field lines are divergenceless and only wane in the presence of induced eddy currents.

At very high frequencies, frequencies often encountered by the microwave community, the skin depth δ is small and magnetic fields are confined to the external volume of conductors. In such a case, the inductances of a system of coupled multi-conductor transmission lines can be derived from the capacitance matrix. Therefore, more emphasis has been placed on deriving the capacitance

matrix as the source of capacitance is charge derived from a scalar Poisson's equation whereas the source of inductance is from currents satisfying the vector Poisson's equation.

The situation has changed as on-chip frequencies have increased to the point where magnetic effects are appreciable. In his pioneering work, Ruehli [Ruehli, 1972] focused attention on efficient techniques for predicting inductive effects in an integrated circuit environment at moderate frequencies where internal inductance cannot be ignored. These techniques are widely applicable, even to board and package environments.

2. DEFINITION OF INDUCTANCE

Inductance is the electric dual of capacitance. While capacitors store electric energy, inductors store magnetic energy. The self-inductance of a circuit can be thought of as the “mass”, or resistance to change in “motion”, of the circuit. The origin of this “mass” comes from the magnetic field of a circuit, which originates from the currents in the circuit. Any change in the current of a circuit induces a change in the magnetic field. From Faraday's law we know that a changing magnetic field induces an electric field. From Lenz's law we can deduce further that this induced electric field always opposes further change in the current.

2.1 ENERGY DEFINITION

From circuit theory the total magnetic energy stored by an inductor is given by

$$W_m = \frac{1}{2}LI^2 \quad (5.1)$$

If we thus calculate the total magnetic energy in a volume V by a physical inductor

$$W_m = \frac{1}{2} \int_V \mathbf{B} \cdot \mathbf{H} dV \quad (5.2)$$

we can equate the above quantities to obtain the inductance.

We have already alluded to the energy definition of an inductor in Chapter 2 when we examined the complex power flowing into a black box

$$P = \frac{1}{2} \oint_S \mathbf{E} \times \mathbf{H}^* \cdot d\mathbf{s} = P_l + 2j\omega(W_m - W_e) \quad (5.3)$$

implying that the device acts inductively if $W_m > W_e$. This also has some interesting implications for the impedance of a lossless passive device as a function of frequency. It can be shown that [Ramo et al., 1994]

$$\frac{dX}{d\omega} = 4 \frac{W_m + W_e}{II^*} \quad (5.4)$$

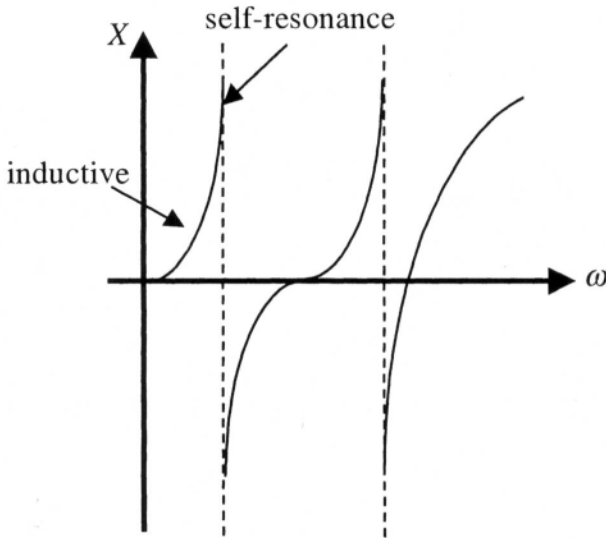


Figure 5.1. The reactance of a lossless passive device as a function of frequency.

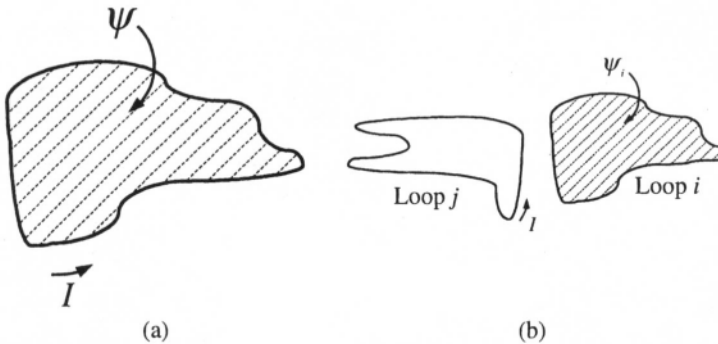


Figure 5.2. (a) An isolated current loop. (b) A magnetically coupled pair of loops. Current only flows in loop j .

which implies that the slope of the impedance versus frequency is never negative. Such a typical profile as a function of frequency is shown in Fig. 5.1.

2.2 MAGNETIC FLUX OF A CIRCUIT

Consider an arbitrary closed-circuit formed by conductors, as shown in Fig. 5.2a. The magnetic flux of this circuit is defined as the magnetic field

crossing the cross-sectional area of the circuit

$$\psi = \oint_S \mathbf{B} \cdot d\mathbf{S} \quad (5.5)$$

The origin of the magnetic field $\mathbf{B}$ is from the circuit itself since there are no other currents in the system. Now, the self-inductance of the circuit is simply defined as

$$L = \frac{\psi}{I} \quad (5.6)$$

where I is the total current flowing in the circuit. If we now consider an arrangement of loops as shown in Fig. 5.2b, then if we let current flow in loop j and measure the impinging flux on loop i , we have the following definition of mutual inductance

$$M_{ij} = \frac{\psi_i}{I_j} \quad (5.7)$$

where

$$\psi_i = \oint_{S_i} \mathbf{B} \cdot d\mathbf{S} \Big|_{I_k=0 \forall k \neq j} \quad (5.8)$$

By Faraday's well-known law, the voltage induced on a loop is related to the flux as follows

$$V = \frac{d\psi}{dt} \quad (5.9)$$

and by the definition of inductance this is simply

$$V = L \frac{dI}{dt} \quad (5.10)$$

2.3 MAGNETIC VECTOR POTENTIAL

From Maxwell's equation, we know that all physically observable magnetic fields are solenoidal, i.e. $\nabla \cdot \mathbf{B} = 0$ and thus we can write $\mathbf{B} = \nabla \times \mathbf{A}$ for some vector potential function $\mathbf{A}$. Note that we are free to choose the divergence of $\mathbf{A}$ as we wish. From the definition of flux, we can invoke Stoke's theorem to obtain

$$\psi = \oint_S (\nabla \times \mathbf{A}) \cdot d\mathbf{S} = \oint_C \mathbf{A} \cdot d\mathbf{l} \quad (5.11)$$

In many practical cases, it is more convenient to work with the magnetic vector potential $\mathbf{A}$ than the magnetic field $\mathbf{B}$. Although the magnetic field has a more physical interpretation, the magnetic vector potential is often simpler to derive.¹ The governing equation for the vector potential is the vector Poisson's equation derived in Chapter 4

$$\nabla^2 \mathbf{A} = \mu \mathbf{J} \quad (5.12)$$

The solution of this equation can be written with the aid of a dyadic Green function $\bar{\mathbf{G}}$

$$\mathbf{A}(\mathbf{r}) = \mu \int_{V'} \bar{\mathbf{G}}(\mathbf{r}, \mathbf{r}') \cdot \mathbf{J}(\mathbf{r}') dV' \quad (5.13)$$

where for instance the component of $\bar{\mathbf{G}}$ for a test source in the direction of $\hat{\mathbf{x}}_i$ is a solution of

$$\nabla^2 \mathbf{G}_i = \mu \delta(\mathbf{r} - \mathbf{r}') \hat{\mathbf{x}}_i \quad (5.14)$$

In an isotropic medium, such as free-space or a spherically symmetric arrangement of conductors, $G_x = G_y = G_z$ and $G_{km} = 0 \forall k \neq m$ and thus the equation can be simplified

$$\mathbf{A}(\mathbf{r}) = \mu \int_{V'} G(\mathbf{r}, \mathbf{r}') \mathbf{J}(\mathbf{r}') dV' \quad (5.15)$$

By definition, then, the mutual inductance between two loops can be derived from the voltage induced in one loop (unprimed coordinates) for a changing current flowing in some “source” loop (primed coordinates). This voltage is given by

$$V_{\text{fld}} = - \oint_C \mathbf{E} \cdot d\mathbf{l} \quad (5.16)$$

From Maxwell’s equation, the electric field is given by

$$\mathbf{E} = -\nabla\phi - \frac{d\mathbf{A}}{dt} \quad (5.17)$$

Since the first term is “conservative” in nature, its line integral along a closed path yields zero. Thus, we have

$$V_{\text{fld}} = \frac{d}{dt} \oint_C \mathbf{A} \cdot d\mathbf{l} = M \frac{dI}{dt} \quad (5.18)$$

Hence

$$M = \frac{1}{I} \oint_C (\mu \int_{V'} G(\mathbf{r}, \mathbf{r}') \mathbf{J}(\mathbf{r}') dV') \cdot d\mathbf{l} \quad (5.19)$$

At low frequencies, the current distribution $\mathbf{J}$ is uniform and the second integration therefore only involves the function G . We can view this volume integral as the line integral of the cross-sectional area of the conductor along the path of the conductor. Therefore

$$\int_{V'} G(\mathbf{r}, \mathbf{r}') J(\mathbf{r}') dV' = I \oint_{C'} \left(\int_{A'} G(\mathbf{r}, \mathbf{r}') dA' \right) d\mathbf{l}' = I \oint_{C'} \bar{G}(\mathbf{r}, \mathbf{r}') d\mathbf{l}' \quad (5.20)$$

where $\bar{G}$ is the value of G averaged over the cross-sectional area of the “source” circuit at any location along the loop. Substituting the above in the equation for inductance we have

$$M = \mu \oint_C \oint_{C'} \bar{G}(\mathbf{r}, \mathbf{r}') d\mathbf{l} \cdot d\mathbf{l}' \quad (5.21)$$

The current factors out in the above equation and thus we see that the inductance at low frequency is simply related to the geometry of conductors in question. For the case of free-space

$$G(\mathbf{r}, \mathbf{r}') = \frac{1}{4\pi|\mathbf{r} - \mathbf{r}'|} \quad (5.22)$$

If the source loop is filamental, then we have Neumann's famous result [Ramo et al., 1994]

$$M = \frac{\mu}{4\pi} \oint \oint \frac{d\mathbf{l} \cdot d\mathbf{l}'}{R} \quad (5.23)$$

which incidentally proves the reciprocity relation $M_{ji} = M_{ij}$.

Evidently, the above result is dependent on the path of integration in the "source" loop. For instance, if we take the inner most turn in a loop of finite width, the value of inductance is different from the outer most loop, due to path length difference and the non-uniformity of the magnetic field. This path dependence is in fact a paramount property of a solenoidal field. Thus, to obtain a path independent mutual inductance, we should average M over all paths. Consider the set of all paths parameterized by $\mathbf{s} \in [0, 1]$ tangent to the current flow $K = \{\mathbf{r}_1(\mathbf{s}) : \mathbf{n}(\mathbf{s}) \cdot \mathbf{J} = 0\}$. The vector $\mathbf{r}_1(\mathbf{s})$ traces one particular path and the vector $\mathbf{n}(\mathbf{s})$ is always normal to the path. Let the average path be described by the following convergent infinite sum

$$\mathbf{r}(\mathbf{s}) = \sum_{j \in K} \mathbf{r}_j(\mathbf{s}) \quad (5.24)$$

and let this path be described by C_1 . Now let us integrate the field quantity $\mathbf{E}'$ along this path to obtain a scalar value with units of voltage

$$V' = - \oint_{C_1} \mathbf{E}' \cdot d\mathbf{l}_1 \quad (5.25)$$

where the field quantity $\mathbf{E}'$ is the average value of the electric field along the cross-section of the path C_1

$$\mathbf{E}'(r) = \int_{A_1} \mathbf{E}(\mathbf{r}) dA_1 \quad (5.26)$$

We can thus interpret (5.25) as the average voltage induced in our "source" loop. Thus, the average mutual inductance becomes

$$M = \mu \oint_{C_1} \oint_{C'} H(\mathbf{r}, \mathbf{r}') d\mathbf{l} \cdot d\mathbf{l}' \quad (5.27)$$

where H is given by

$$H(\mathbf{r}, \mathbf{r}') = \int_{A_{src}} \int_{A_{fld}} G(\mathbf{r}, \mathbf{r}') dA_{src} dA_{fld} \quad (5.28)$$

We can interpret the function $H(\mathbf{r}, \mathbf{r}')$ as the average value of G evaluated for all points in the cross-sectional areas of the source and field loops at a given position $\mathbf{r}$ in the field and $\mathbf{r}'$ in the source loops.

3. PARALLEL AND SERIES INDUCTORS

When N inductors are connected in series, the effective mutual inductance can be computed easily since the voltage across the series connection gives

$$V = \sum_{i=1}^N V_i = \sum_{i=1}^N \sum_{j=1}^N s M_{ij} I_j = I s \sum_{i=1}^N \sum_{j=1}^N M_{ij} \quad (5.29)$$

where we have assumed that the branch current is equal to I for all branches since we are neglecting displacement current at low frequencies. Clearly, then

$$L_{se} = \sum_{i=1}^N L_i + 2 \sum_{i=1}^N \sum_{j \neq i}^N M_{ij} \quad (5.30)$$

The case of parallel connected inductors is more complicated. The result has already been stated in Chapter 2

$$L_{sh} = \frac{1}{\sum_{i=1, j=1}^N K_{ij}} \quad (5.31)$$

where the matrix K is the inverse of the partial inductance matrix M . To see that this is true in general, consider N -shunt connected coupled inductors described by the partial inductance matrix M ,

$$\mathbf{v} = j\omega M \mathbf{i} \quad (5.32)$$

where element v_j of vector $\mathbf{v}$ is the voltage across j th inductor and the element i_j of vector $\mathbf{i}$ is the current through the j th inductor. Since the voltages are connected in shunt, all voltages are equal

$$v_x = v_1 = v_2 = \cdots = v_N \quad (5.33)$$

and thus

$$\mathbf{v} = v_x \mathbf{s} \quad (5.34)$$

where $\mathbf{s} = \begin{pmatrix} 1 \\ \vdots \\ 1 \end{pmatrix}$ and the total current is given by

$$i_x = i_1 + i_2 + \cdots + i_N = \mathbf{s}^T \mathbf{i} \quad (5.35)$$

Since the effective input inductance is given by

$$L_{sh} = \frac{v_x}{j\omega i_x} \quad (5.36)$$

we have from (5.32)

$$(j\omega M)^{-1} \mathbf{v} = (j\omega M)^{-1} \mathbf{s} v_x \quad (5.37)$$

and further

$$\mathbf{s}^T (j\omega M)^{-1} \mathbf{s} v_x = \mathbf{s}^T \mathbf{i} = i_x \quad (5.38)$$

and

$$L_{sh} = \frac{1}{\mathbf{s}^T M^{-1} \mathbf{s}} \quad (5.39)$$

which establishes (5.31). In [Ruehli, 1972] the above result is stated in the following form

$$L_{sh} = \left[2 \sum_{i=1}^{N-1} \sum_{j=i+1}^N \text{cof } M_{ij} + \sum_{i=1}^N \text{cof } M_{ii} \right]^{-1} \det M \quad (5.40)$$

4. FILAMENTAL INDUCTANCE FORMULAE FOR COMMON CONFIGURATIONS

Consider a $\hat{\mathbf{z}}$ directed filament of finite length l carrying a current I in free-space located at the origin of a rectangular coordinate system. The magnetic vector potential at any point in space is given by (5.15)

$$\mathbf{A}(x, y, z) = \hat{\mathbf{z}} \frac{\mu_0 I}{4\pi} \int_{-l/2}^{l/2} \frac{1}{\sqrt{x^2 + y^2 + (z - z')^2}} dz' \quad (5.41)$$

Performing the above integration we have

$$A_z(x, y, z) = \hat{\mathbf{z}} \frac{\mu_0 I}{4\pi} \log \left[\frac{(z + l/2) + \sqrt{x^2 + y^2 + (z + l/2)^2}}{(z - l/2) + \sqrt{x^2 + y^2 + (z - l/2)^2}} \right] \quad (5.42)$$

Now consider the mutual magnetic inductance of two such parallel filaments separated by a distance d . If we integrate the expression for A_z along the path of the second filament we obtain

$$M(l, d) = \int_{-l/2}^{l/2} A_z(d, 0, z') dz' \quad (5.43)$$

The above integral can be simplified into the following form

$$M(l, d) = \frac{\mu_0 l}{4\pi} \left[\log \left(\sqrt{1 + \left(\frac{l}{d}\right)^2} + \frac{l}{d} \right) - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l} \right] \quad (5.44)$$

The above expression is the starting point for calculating the mutual inductance between two arbitrary parallel filaments. The technique is described in Grover [Grover, 1946] and Ruehli [Ruehli, 1972].

5. CALCULATION OF SELF AND MUTUAL INDUCTANCE FOR CONDUCTORS

Following the averaging procedure described in (5.21), we can find the mutual inductance between two parallel conductors of arbitrary cross-section by integrating the filamental formula (5.44) over the area of the cross-section of the conductors

$$M_{12} = \frac{1}{A_1 A_2} \int_{A_1} \int_{A_2} M(L, r) dA_1 dA_2 \quad (5.45)$$

where $r = \sqrt{(x_1 - x_2)^2 + (y_1 - y_2)^2 + (z_1 - z_2)^2}$. For the case of self-inductance, we can set $A_1 = A_2$ and perform the integration. This will result in an integrable singularity in the calculation.

5.1 THE GEOMETRIC MEAN DISTANCE (GMD) APPROXIMATION

If the filaments under consideration are long such that $L \gg d$, then the results for $M(L, d)$ can be simplified if we neglect the term $\left(\frac{d}{L}\right)^2$

$$M(L, d) \approx \frac{\mu_0}{4\pi} L \left(\frac{d}{L} - \log d + \log 2L - 1 \right) \quad (5.46)$$

Integration of the above expression across the cross-section yields a simpler calculation. The only difficult term to integrate is the $\log(d)$. This term, the *Geometric Mean Distance*, or GMD, is the average value of the logarithm of the distance between all points between the conductors. This integral can be calculated for several simple configurations, especially for arbitrary rectangular cross-sections. Some of these results can be found in [Niknejad, 1997].

A simple interpretation of the above result can be obtained if we make the $L \gg d$ approximation from the outset. If we let $L \rightarrow \infty$ we have the following 2D magnetic vector potential

$$\mathbf{A}(x, y) = \hat{z} \frac{\mu_0 I}{4\pi} \log \sqrt{x^2 + y^2} \quad (5.47)$$

And thus the mutual inductance per unit length between two infinite parallel conductors is given by

$$M_{12} = \frac{\mu_0}{4\pi} \int_{A_1} \int_{A_2} \log(r) dA_1 dA_2 \quad (5.48)$$

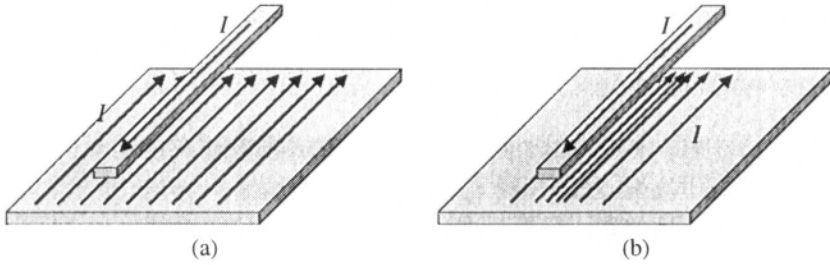


Figure 5.3. (a) Ground current at low frequency. (b) Ground current at high frequency.

where r takes on the value of the distance between every pair of points in the cross-section of each conductor. With the exception of the Arithmetic Mean Distance (AMD) correction factor, this is exactly the same expression found with the GMD approximation.

6. HIGH FREQUENCY INDUCTANCE CALCULATION

6.1 BACKGROUND

All the equations derived thus far for inductance have made the assumption of uniform current distribution within the volume of conductors. While this applies to low frequencies, we know that at high frequencies currents redistribute to minimize the energy of the system. Consider, for instance, a conductor carrying a low frequency current above a ground plane as shown Fig. 5.3a. At low frequencies (strictly DC) the return current flowing in the ground plane flows uniformly and so the resistance per unit length for the entire system can be computed by

$$R_{\text{tot}} = R_{\square} \left(\frac{1}{W} + \frac{1}{W_{\text{gnd}}} \right) \quad (5.49)$$

At higher frequencies, though, currents redistribute to minimize the energy of the system as shown in part (b) of Fig. 5.3. The magnetic energy of the system can be minimized by minimizing the inductance value per unit length. Thus, the ground currents redistribute and concentrate under the signal carrying conductor.² The ground current will flow as close as possible to the signal carrying current in order to minimize the magnetic field (since ground currents flow in the opposite direction). The high frequency resistance is thus closer to

$$R_{\text{tot}} \approx 2 \frac{R_{\square}}{W} \quad (5.50)$$

Another perspective is to note that AC current takes the path of least impedance. Now consider the inductance value of the various paths through the ground plane. As shown in Fig. 5.4 a path far removed from the substrate has a large

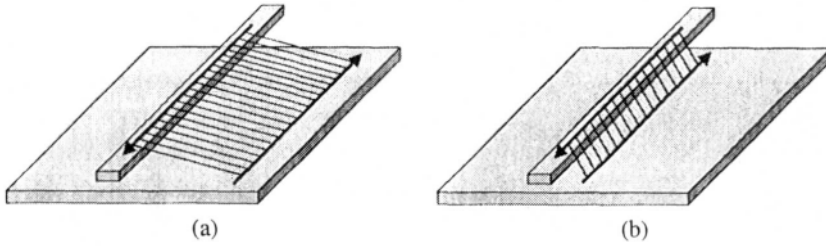


Figure 5.4. The cross-sectional area of a return path loop (a) far removed from the conductor and (b) near the conductor.

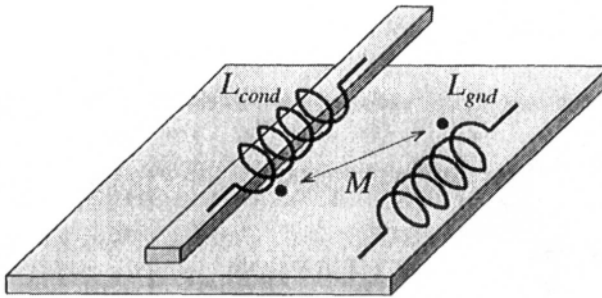


Figure 5.5. The self and mutual inductance of the conductor and return path.

cross-sectional area and thus a large value of inductance. A path directly under the inductor involves the smallest area and thus the smaller value of inductance. Therefore, AC current will flow in paths of low inductance.

A final perspective to this problem can be drawn from our study of “partial” inductance. As shown in Fig. 5.5, the total inductance for a typical path in the ground plane is given by

$$L_{\text{tot}} = L_{\text{cond}} + L_{\text{gnd}} - 2M \quad (5.51)$$

Since M varies from path to path whereas the L for a typical path is constant, nature chooses a path to maximize M so as to minimize the total inductance.

It is interesting to note that the high frequency current distribution is a result of the electric field term of

$$\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B}) \quad (5.52)$$

rather than the magnetic field term. This is a result of the electromagnetic interaction or Faraday’s law. To see this is true consider the static magnetic force on two current carrying wires. It is well known that if the currents are in opposite directions, the wires repel one another. So based on the magnetic

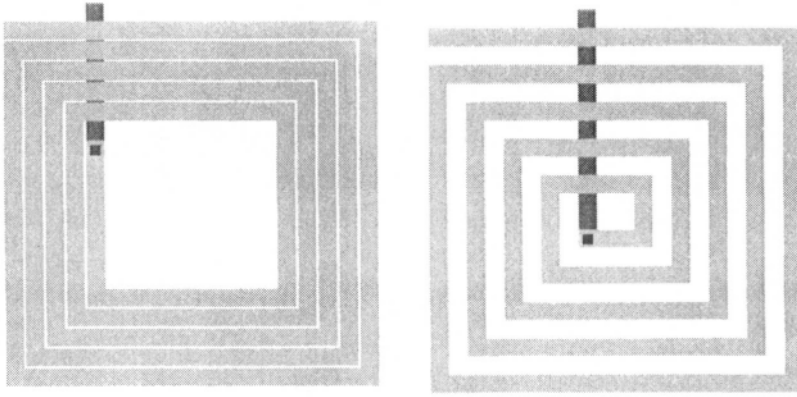


Figure 5.6. Two inductors realized with different metal spacing values of $1\ \mu\text{m}$ and $10\ \mu\text{m}$.

forces alone the current distribution in our example should be the exact opposite of Fig. 5.3b.

6.2 EXAMPLE CALCULATION

We will now illustrate the importance of calculating the partial inductance matrix at high frequency with an example. Consider the two spiral inductor layouts shown in Fig. 5.6. The inductor geometries are identical with outer length $L = 200\ \mu\text{m}$, and five turns of metal pitch $W = 10\ \mu\text{m}$. In (a), though, the metal spacing $S = 1\ \mu\text{m}$ whereas in (b) $S = 10\ \mu\text{m}$.

We analyze both devices by computing the partial inductance matrix $\tilde{\mathbf{Z}}$. Each segment of the spirals is sub-sectioned into twenty separate conductors producing a 400×400 matrix $\tilde{\mathbf{Z}}$. The matrix is reduced in order by computing $\mathbf{Z}^M = (\mathbf{S}\tilde{\mathbf{Z}}^{-1}\mathbf{S}^T)^{-1}$ and then by summing over the elements to obtain

$$R(f) + j\omega L(f) = \sum_{i,j} Z_{i,j}^M(f) \quad (5.53)$$

From an inductance point of view, using the smaller value of spacing results in a higher DC inductance value of 5.2 nH as opposed to 2.6 nH. From Fig. 5.7 we see that as a function of frequency, the inductance values of both devices decrease slightly approaching the external inductance limit³, falling about 4% from the DC value at 5 GHz.

The series resistance of the device, though, increases much more rapidly for the smaller value of spacing, as shown in Fig. 5.7b, where the ratio of AC to DC resistance is plotted. While the device with large spacing shows a 40% increase in series resistance at 5 GHz compared to DC, the device with small spacing suffers nearly twice as much loss at 5 GHz compared to low frequency. This

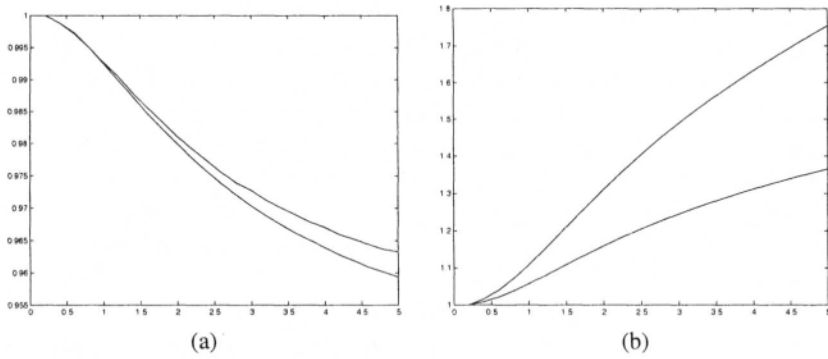


Figure 5.7. The ratio of AC to DC inductance and resistance as a function of frequency plotted for two inductors of Fig. 5.6.

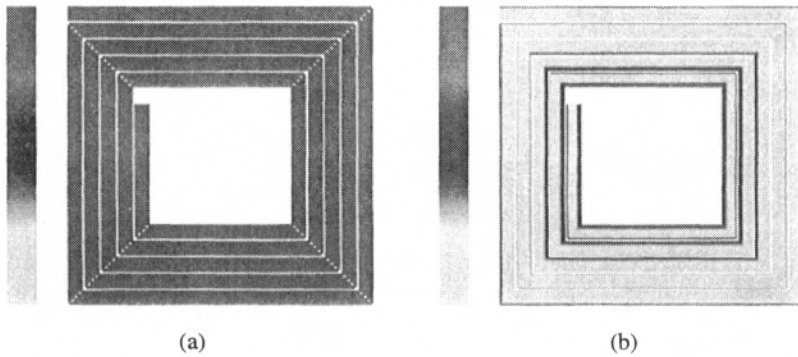


Figure 5.8. The current density at (a) 1 GHz and (b) 5 GHz.

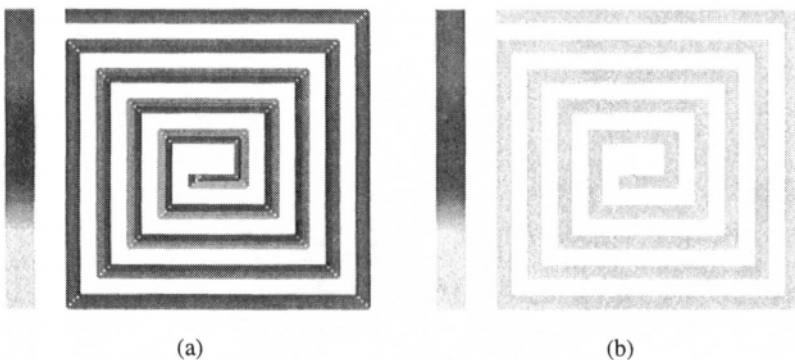


Figure 5.9. The current density at (a) 1 GHz and (b) 5 GHz.

increase is faster than the $\sqrt{f}$ increase predicted by simple skin effect theory. To see why, note that the magnetic field is non-uniform across the cross-section of the inductor and increases rapidly towards the center of the device. Thus the magnetic field penetrating the conductors results in eddy currents with a more profound influence over the loss at the inner core of the spiral. A plot of the current density⁴, shown in Fig. 5.8, shows that the $1\ \mu\text{m}$ design suffers from current constriction at 5 GHz in the innermost turn. On the other contrary, as shown in Fig. 5.9, the $10\ \mu\text{m}$ design has uniform current distribution even at 5 GHz, more uniform than at 1 GHz.

Now consider an optimization routine searching for a value of spacing S to optimize the Q of the device. If the optimizer makes the assumption that resistance increases like $\sqrt{f}$ independent of spacing, then clearly the optimizer will select the smallest possible value of S to maximize the inductance. In other words, an optimizer will find an incorrect optimal solution, an artifact created by the weakness of the modeling process.

Notes

- 1 Magnetic vector potential also has physical meaning in the study of quantum mechanics [Feynman et al., 1963].
- 2 For simplicity we have ignored the current distribution in the signal conductor.
- 3 Please note that this is the physical inductance of the device and not the effective inductance. In other words, the capacitive effects have been completely ignored in computing (5.53).
- 4 See Chapter 7 for an explanation of how these plots were generated. Note that these plots show the current distribution after solving the electric and magnetic problem.

Chapter 8

EXPERIMENTAL STUDY

In this chapter we will compare measured device characteristics to simulated predictions based on the techniques described in the previous chapters. In a previous report [Niknejad, 1997], experimental results confirmed the validity of the our approach. Several structures were fabricated and measured in a BiCMOS process including square and polygon spiral inductors, planar and non-planar transformers, and coupled inductors.

In this chapter, we would like to make the same comparisons but with devices fabricated over a conductive substrate. As previously discussed, a heavily conductive substrate gives rise to new loss mechanisms, in particular magnetically induced eddy current losses. Conductive substrates are typically employed in CMOS processes to minimize latch-up. Latch-up occurs when the parasitic lateral and vertical bipolar transistors of a CMOS inverter turn on in a positive feedback loop [Johns and Martin, 1997]. To minimize voltage drops in the substrate capable of potentially forward biasing these bipolar devices, a heavily conductive highly doped bulk substrate is employed. A more resistive, lightly doped layer is then grown epitaxially over this substrate to house the wells and MOS transistors, hence the name “epi” substrate. A cross-section of such a process is shown in Fig. 2.5. Another variation, similar to the bipolar substrate, is to start with a lightly doped substrate but to grow a heavily conductive surface layer to shunt substrate currents to a low potential.

1. MEASUREMENT RESULTS

As shown in Fig. 8.1, several planar and non-planar spiral inductors have been fabricated in National Semiconductor's **0.25 μm** CMOS-8 process. This process utilizes a bulk substrate of **10 $\Omega\text{-cm}$** , sufficiently resistive that eddy currents play a minor part in the bulk. However, the top layer of Si is fairly conductive at **$15 \times 10^{-4} \Omega\text{-cm}$** . The thickness of this layer is less than **1 μm** but

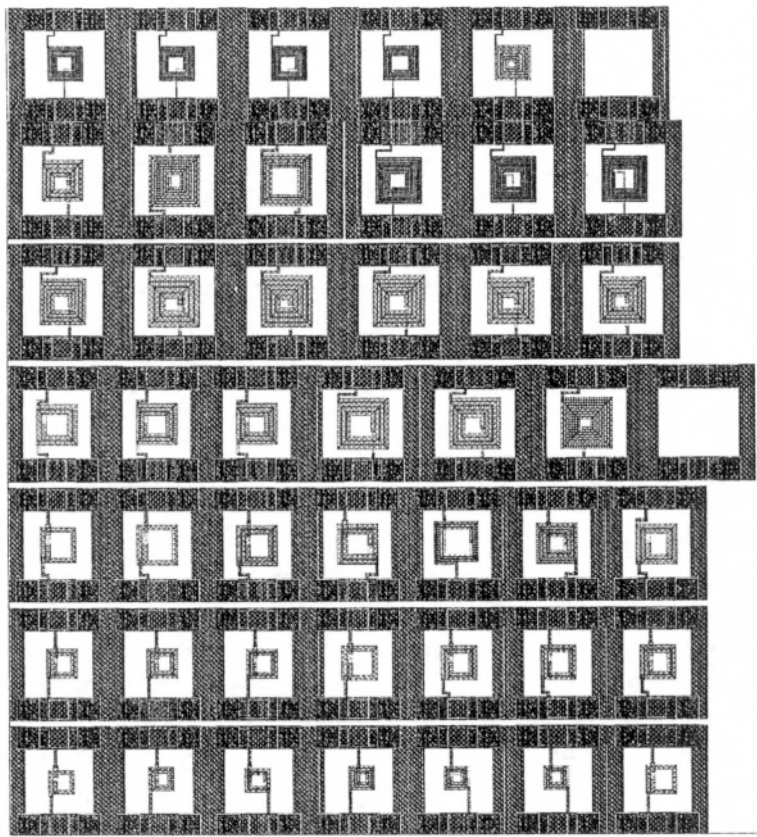


Figure 8.1. Inductor test structures.

this is enough to cause significant eddy current loss. The process parameters are summarized in Table 8.1.

The layout of two representative inductors is summarized in Table 8.2. As shown in Fig. 8.2, spiral inductor L27 is a planar device utilizing the top metal layer. Inductor L19 resides on metal layers M5-M3 connected in series realizing a large inductance value in a relatively small area. The layout of L19 is shown in Fig. 8.3.

2. DEVICE CALIBRATION

Measurements are performed using a ground-signal-ground co-planar waveguide pad configuration. The *s*-parameters are measured using the HP 8719C Network Analyzer. G-S-G co-planar cascade probes are used and the setup is calibrated using the Cascade Microtech 832210 calibration substrate. The

Table 8.1. CMOS Process Parameters Summary

Metal 5	$R_{sh} = 35 \text{ m}\Omega/\text{sq}$	$t = 0.91 \mu\text{m}$	$C_{sub} = 6.12 \text{ aF}/\mu\text{m}^2$ $C_{M4} = 53.1 \text{ aF}/\mu\text{m}^2$ $C_{M3} = 19.1 \text{ aF}/\mu\text{m}^2$
Metal 4	$R_{sh} = 60 \text{ m}\Omega/\text{sq}$	$t = 0.51 \mu\text{m}$	$C_{sub} = 7.69 \text{ aF}/\mu\text{m}^2$ $C_{M3} = 53.1 \text{ aF}/\mu\text{m}^2$
Metal 3	$R_{sh} = 60 \text{ m}\Omega/\text{sq}$	$t = 0.51 \mu\text{m}$	$C_{sub} = 10.4 \text{ aF}/\mu\text{m}^2$
Surface Layer	$\rho = 15 \times 10^{-4} \Omega\text{-cm}$	$t = 0.8 \mu\text{m}$	$p^+ \text{ Si}$
Bulk Substrate	$\rho = 10 \Omega\text{-cm}$	$t = 725 \mu\text{m}$	$p^- \text{ Si}$

Table 8.2. Device Physical Dimensions

Spiral Name	L19	L27
Outer Length (μm)	200	250
Metal Width W (μm)	11	10.5
Metal Spacing S (μm)	3	3
No. of Turns N	2.5	7.75
Metal Layer(s)	M3-M5	M5

open-pad y -parameters are also measured and subtracted from the measured y -parameters to remove the pad capacitance and loss.

It is interesting to note that the G-S-G approach has some clear advantages over the S-G approach presented previously in [Niknejad and Meyer, 1998]. To see this, consider the ground pad configurations of each approach, as shown in Fig. 8.4. As noted in [Niknejad, 1997], the S-G approach is prone to calibration errors resulting from the substrate coupling between the pads, since the presence of the device under test alters the substrate coupling. On the other hand, in the G-S-G approach, the substrate pads are widely separated and the presence of the ground de-couples the input from the output port. Thus, the G-S-G calibration step only subtracts out the input and output capacitance and has a minor influence on the coupling capacitance between the input and output ports, in stark contrast to the S-G approach where a large coupling capacitance is involved.

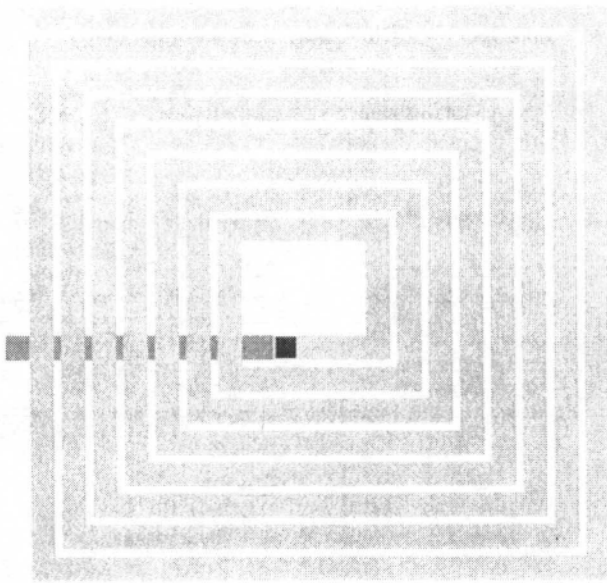


Figure 8.2. Layout of inductor L27.

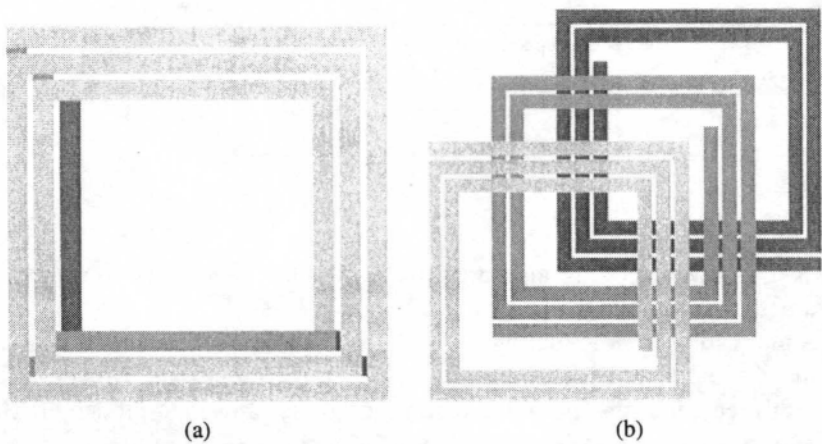


Figure 8.3. Layout of inductor L19. In part (b) the lower metal layers have been staggered to give a clear picture of the device geometry.

For these reasons, the G-S-G calibration procedure was selected. Designing a proper G-S-G calibration test structure in CMOS requires special care. With a device under test connected to the calibration structure, return ground currents flow through the calibration structure. To minimize the losses resulting

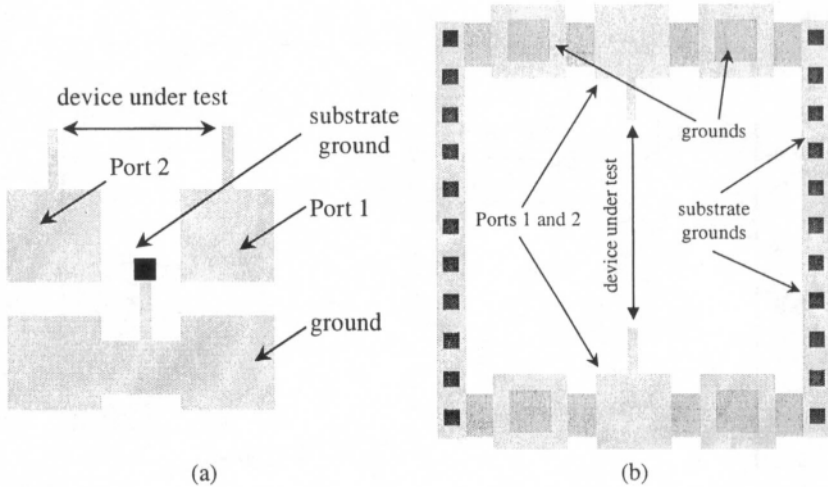


Figure 8.4. Calibration pad structures. (a) S-G structure. (b) G-S-G structure.

from such ground currents, metal layers M1-M5 have been strapped with an ample supply of vias and substrate ground connections to minimize the losses. Furthermore, in the G-S-G approach the signal ports can be isolated from the substrate by using an M1 shield under the pads, minimizing the loss contribution from the pads. In the S-G case, the pads introduce substantial loss which must be calibrated out of the device loss.

3. SINGLE LAYER INDUCTOR

Measured s -parameters for inductor L27 are shown in Fig. 8.5. The simulated and measured results match well. The discrepancy above the self-resonant frequency is in the capacitive region where we are less interested in the device. Notice that the inductor self-resonates at a frequency of 4.25 GHz. Simulations using *ASITIC* predicted a self-resonant frequency of 4.15 GHz. The simulations are performed on a Pentium II 400 MHz machine running the Linux operating system. Each frequency point requires less than ten seconds of computation. In Fig. 8.6 we plot the effective value of inductance. This is derived using a one-to-one transformation of the s -parameters into π -parameters [3]. Again, a good match is observed between the theory and measurements. The inductance decrease is due mostly to the capacitive effects rather than the inductive effects. Inductance value decreases slightly due to skin effect and eddy currents in the substrate but the main reason for the decrease is that energy is coupled from port to port through the winding capacitance at higher frequencies.

Fig. 8.7 shows the effective value of series resistance as a function of frequency. Two simulations are performed, with and without eddy current losses.

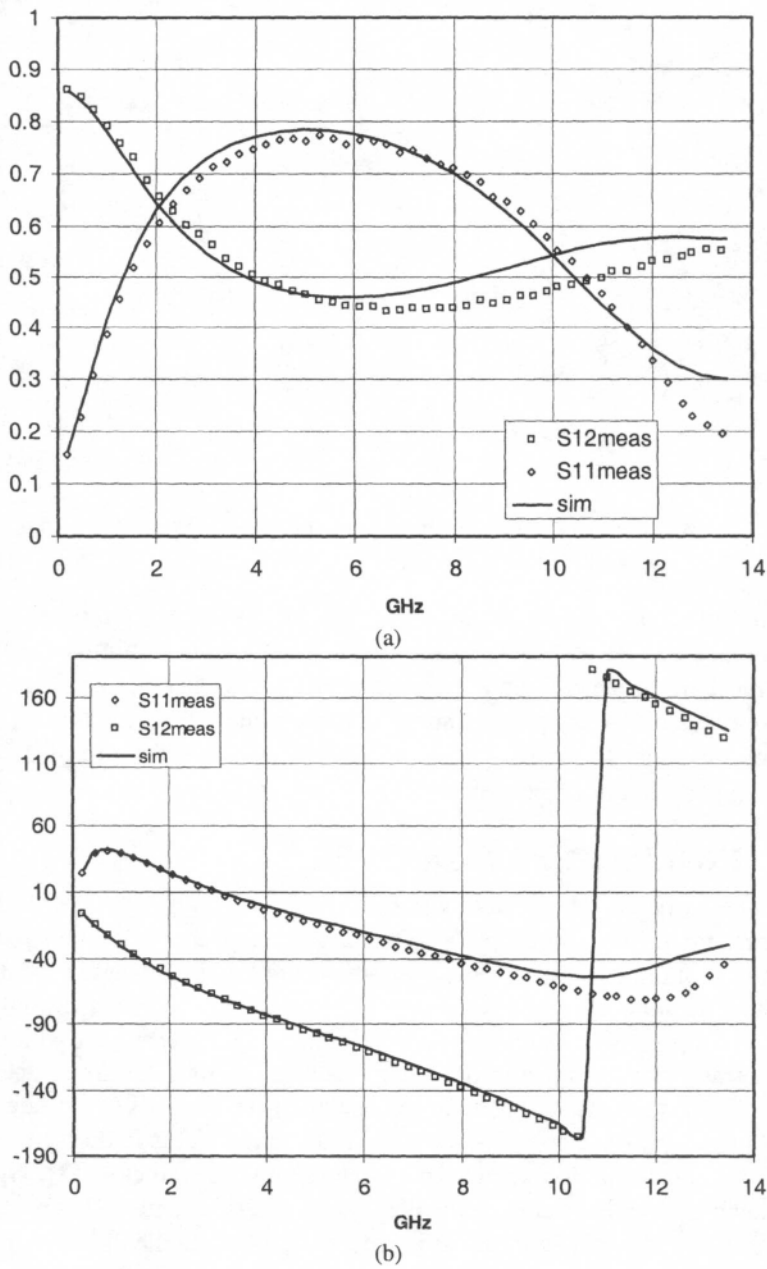


Figure 8.5. Measured and simulated (a) magnitude and (b) phase *s*-parameters of spiral inductor L27.

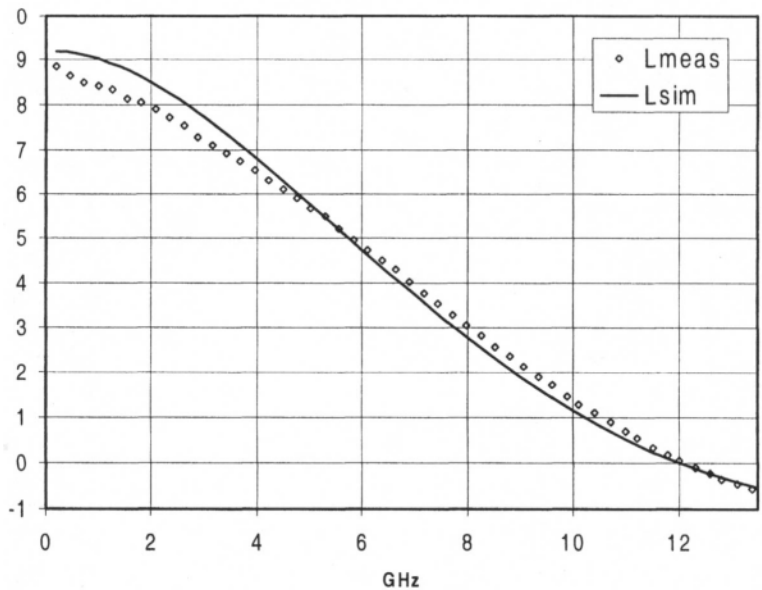


Figure 8.6. Measured and simulated inductance (imaginary component of Y_{21}) of spiral inductor L27.

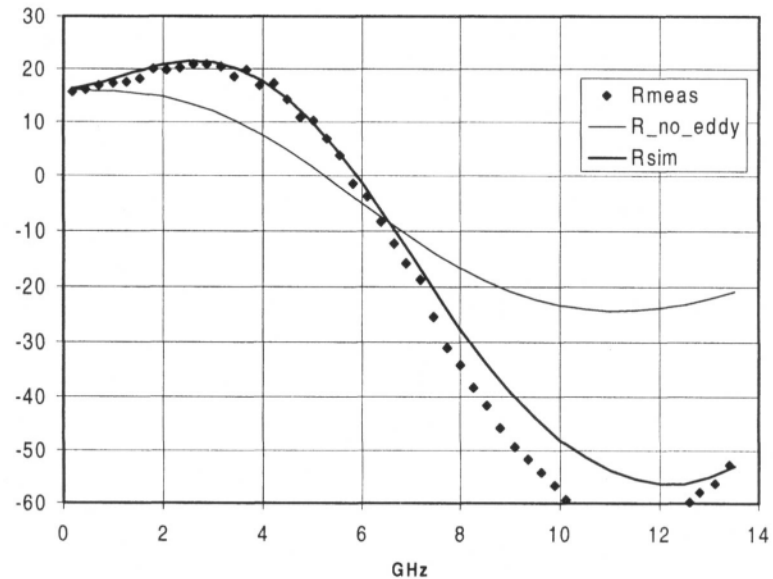


Figure 8.7. Measured and simulated resistance (real component of Y_{21}) of spiral inductor L27.

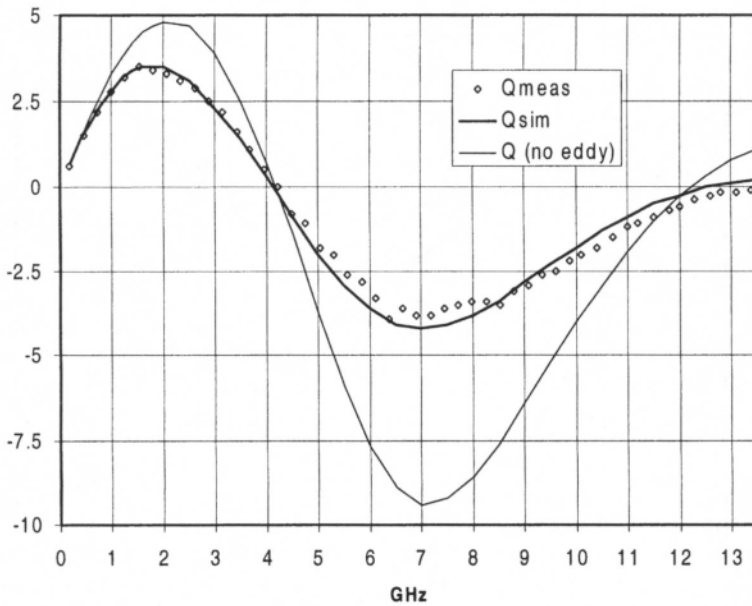


Figure 8.8. Measured and simulated quality factor (imaginary over real component of Y_{21}) of spiral inductor L27.

As evident in the figure, eddy current losses are critical to model. The variation in frequency of the series resistance is due to various competing effects. Skin effect and proximity effects increase the series resistance but beyond 1 GHz this is swamped by the increase from eddy currents. At higher frequencies more energy is transported capacitively, and consequently the resistance decreases and eventually becomes negative. The real part of the total input impedance looking into each port, of course, is positive at all frequencies.

The quality factor Q , the ratio between the imaginary and real part of the input impedance, is plotted in Fig. 8.8. Again, a good match is observed between the theory and measurements. Note that negative quality factor implies that the device is acting as a capacitor rather than an inductor. In reality, this plot is misleading as it implies a Q of zero at self-resonance. A better way to calculate Q is given in [3] but for comparison the given definition is better since it involves a minimal transformation of the measured s -parameters. The substrate resistance and capacitance are also shown in Fig. 8.9 and Fig. 8.10. The overall shape of both curves matches the measurements well. The low frequency substrate resistance measurements are noisy due to measurement error.

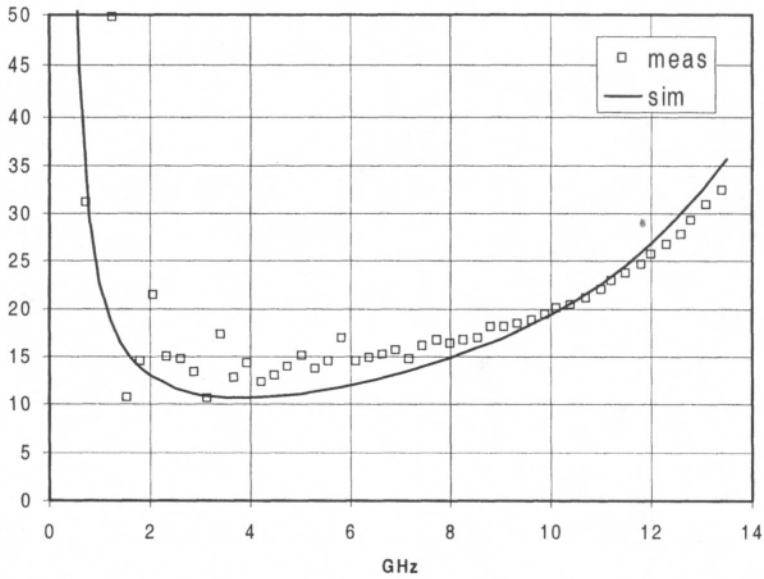


Figure 8.9. Measured and simulated substrate resistance of spiral inductor L27.

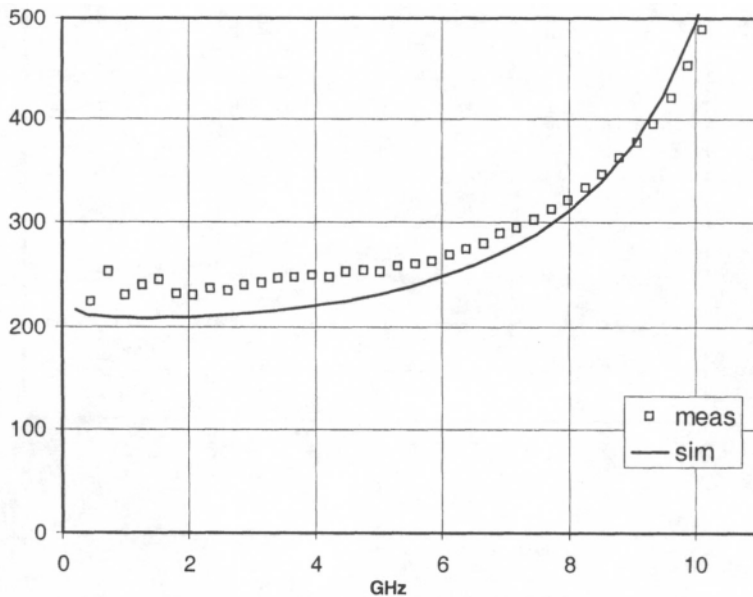


Figure 8.10. Measured and simulated substrate capacitance of spiral inductor L27.

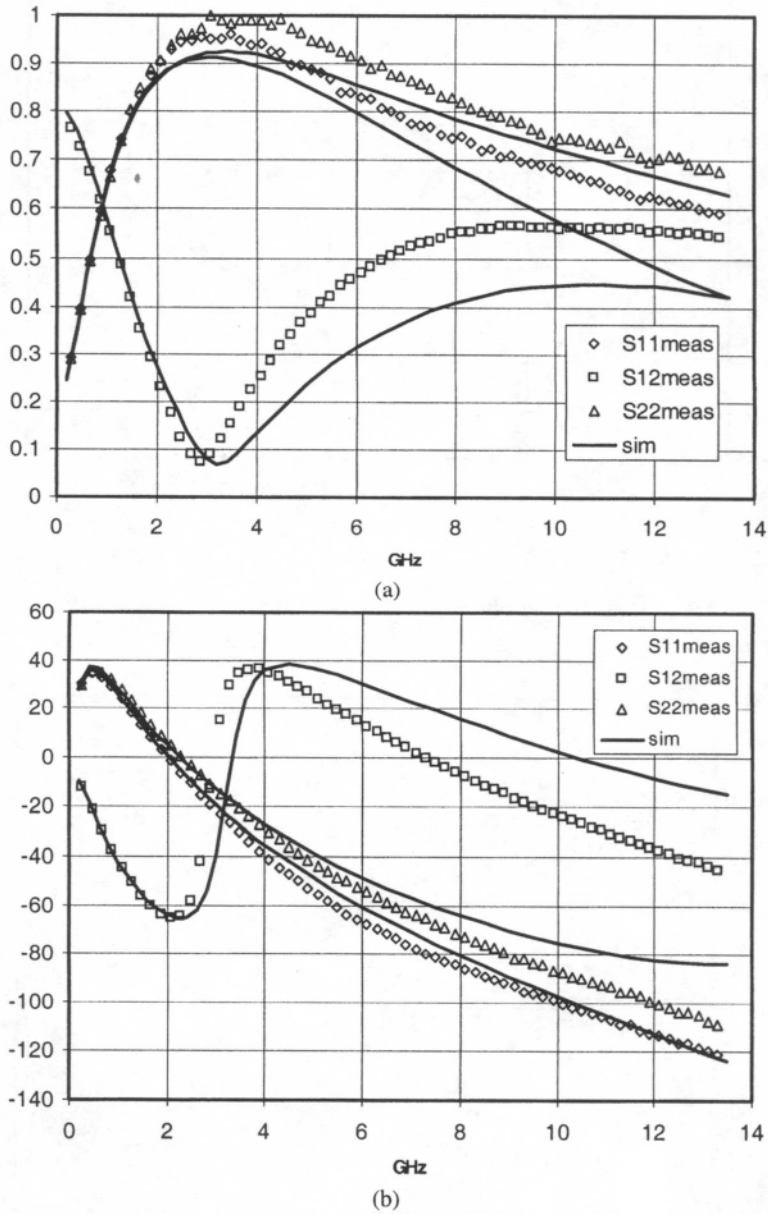


Figure 8.11. Measured and simulated (a) magnitude and (b) phase s -parameters of spiral inductor L19.

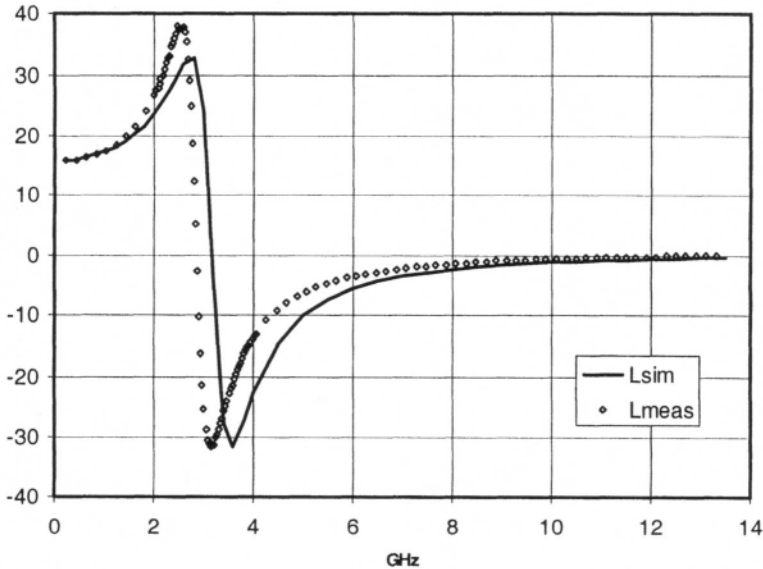


Figure 8.12. Measured and simulated inductance (imaginary component of Y_{21}) of spiral inductor L19.

4. MULTI-LAYER INDUCTOR

Measured s -parameters for inductor L19 are shown in Fig. 8.11. A fairly good match between the simulated and measured is observed, especially below the self-resonant frequency. Due to the large interwinding capacitance intrinsic to this series-connected structure, the self-resonant frequency is low. The self-resonant frequency is predicted at 2.57 GHz and measured at 2.47 GHz.

To gain insight into the data we also plot the series inductance and resistance in Figures 8.12 and 8.13. These curves are dramatically different from the previous device. The differences can be accounted for by noting that a planar device self-resonates through the substrate capacitance whereas a multi-metal device self-resonates through the interwinding capacitance. Since this is a relatively high Q capacitor compared to the lossy substrate capacitance, the behavior of L and R can be modeled by the simple equivalent circuit of Fig. 8.14. As we approach self-resonance the inductance and resistance values peak. The maximum value of resistance is approximately $Q^2 R_{\text{series}}$. Thus, the lower the losses the higher the value of the peak. Again, simulation is able to predict these effects well. The discrepancy is due mainly to the value of oxide thickness used in the simulation. The process parameters were not adjusted at all in the simulations in order to gauge how well one can predict inductor performance *a priori*. Since oxide thickness is not a well-controlled process parameter, and since the oxide thickness has a significant impact on the device performance, it

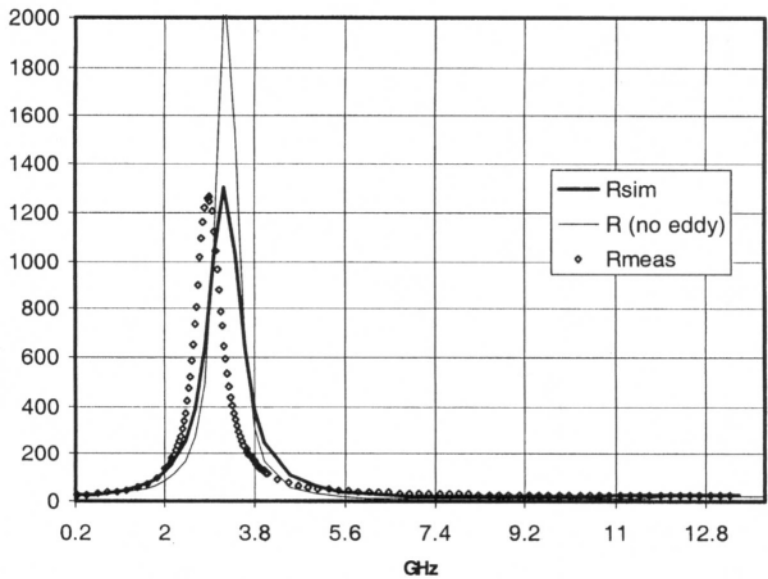


Figure 8.13. Measured and simulated resistance (real component of Y_{21}) of spiral inductor L19.

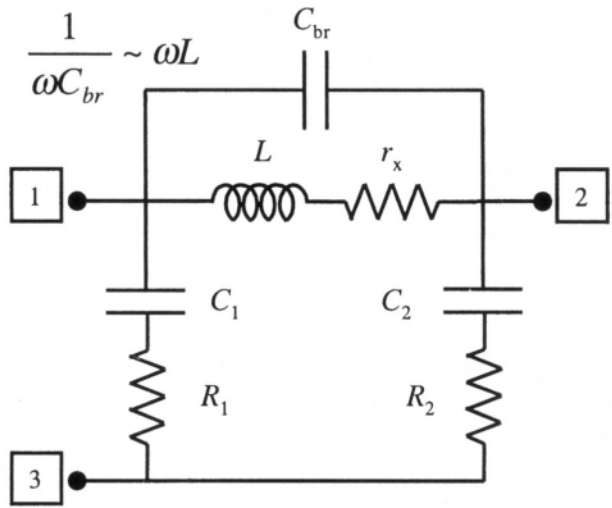


Figure 8.14. Simple equivalent circuit of inductor L19 close to self-resonance.

seems like this device is not as manufacturable as the planar structure, especially close to self-resonance.

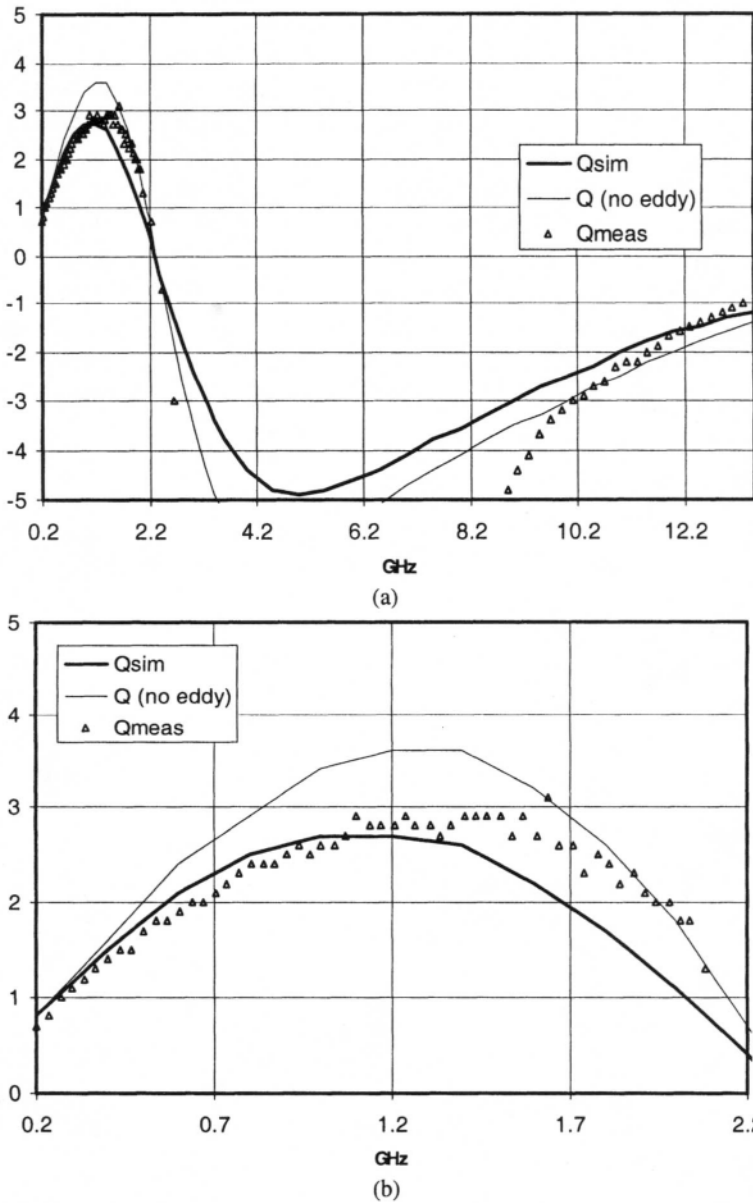


Figure 8.15. (a) Measured and simulated quality factor (imaginary over real component of Y_{21}) of spiral inductor L19. (b) Close-up plot.

Fig. 8.15 shows the quality factor plot for two simulations and the measurements. As before, the simulation results with no eddy currents under-predict the losses, but now the simulations with eddy currents slightly over-predict the losses. This is especially true beyond self-resonance where the device is acting as a capacitor. Fortunately, one is generally not interested as much in frequencies beyond self-resonance. The discrepancy, though, can be easily explained with some physical insight into the problem. Beyond self-resonance the device is acting very much like a metal-insulator-metal capacitor. Since wide metal lines are used to wind the inductor to minimize the low frequency losses, the current distribution in the lines is not constrained to be one-dimensional as we have assumed. In fact, at high frequencies the bottom metal layers act as a solid shield against both the magnetic and electric fields. Thus, eddy currents flow in the shield and prevent the magnetic fields from penetrating the lossy substrate. We could account for this effect by utilizing a two-dimensional mesh but we are less interested in this region of operation.

II

APPLICATIONS OF PASSIVE DEVICES

Attachment 2A

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245 10 Design, simulation and applications of inductors and
transformers for Si RF ICs /|cAli M. Niknejad, Robert G.
Meyer
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100 1 Niknejad, Ali M., \$d 1972-

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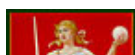
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670 __ |a ASTI: |b p. 1960, under Silicon-on-insulator devices.

670 __ |a EI: |b v. 86, part IX, p. 6460-61, under Silicon-on-insulator circuits, devices, films, (SOI) materials, structures, substrates, systems, and technology.

670 __ |a Encyc. of physical sci. & tech.: |b p. 999.

675 __ |a Chem. abst.; |a Hennepin; |a IAC; |a INSPEC thes.; |a Random House; |a Web. 3

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