UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN INTEGRATED CIRCUITS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING THE SAME**	**Inv. No. 337-TA-1350**

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

Administrative Law Judge Cameron Elliot

(January 19, 2024)

Pursuant to the Notice of Investigation and Rule 210.42(a) of the Rules of Practice and Procedure of the United States International Trade Commission, this is my Initial Determination in the matter of *Certain Integrated Circuits, Components Thereof, and Products Containing the Same*, Investigation No. 337-TA-1350.

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TABLE OF ABBREVIATIONS

CDX	Complainant's Demonstrative Exhibit
CIB	Complainant's Revised Initial Post-Hearing Brief
CPB	Complainant's Pre-Hearing Brief
CPX	Complainant's Physical Exhibit
CRB	Complainant's Reply Post-Hearing Brief
CX	Complainant's Exhibit
Hr'g Tr.	Hearing Transcript
JX	Joint Exhibit
RDX	Respondents' Demonstrative Exhibit
RIB	Respondents' Initial Post-Hearing Brief
RPB	Respondents' Pre-Hearing Brief
RPX	Respondents' Physical Exhibit
RRB	Respondents' Reply Post-Hearing Brief
RX	Respondents' Exhibit

I. INTRODUCTION

A. Procedural Background

Complainant Realtek Semiconductor Corporation ("Realtek") filed the complaint underlying this investigation on December 12, 2022. The complaint alleged respondent Advanced Micro Devices, Inc. ("AMD") imports or sells in connection with an importation certain integrated circuits, components thereof, and products containing the same that infringe one or more claims of U.S. Patent Nos. 7,936,245 ("the 245 patent"), 8,006,218 ("the 218 patent"), and 9,590,582 ("the 582 patent") (together, the "Asserted Patents").

By publication of a notice in the *Federal Register* on January 24, 2023, the U.S. International Trade Commission ordered that:

> Pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, an investigation be instituted to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of products identified in paragraph (2) by reason of infringement of one or more of claims 1, 2, and 8 of the '245 patent; claims 12-18 of the '218 patent; and claims 1-4 and 9 of the '582 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337[.]

88 Fed. Reg. 4206 (Jan. 24, 2023).

On January 19, 2023, the investigation was assigned to me. EDIS Doc. ID 788294. On February 13, 2023, I set a target date of May 23, 2024 for completion of this investigation. Order No. 5. Also on February 13, 2023, I set a *Markman* hearing date of April 25, 2023, and the evidentiary hearing for October 16-20, 2023. Order No. 6. On March 16, 2023, and pursuant to the parties' request, the *Markman* hearing was moved to June 5, 2023. Order No. 8. The parties' claim construction disputes were resolved on July 25, 2023. Order No. 21.

On May 15, 2023, AMD moved (1350-007) for summary determination that the asserted claims of the 218 patent and the 582 patent were invalid for indefiniteness. The motion was denied on July 25, 2023. Order No. 20.

On June 7, 2023, AMD moved (1350-009) for summary determination of no economic prong domestic industry. The motion was denied on June 30, 2023. Order No. 18.

On July 25, 2023, Realtek moved (1350-014) for summary determination on a variety of issues including: that certain products are not prior art to the 218 patent or 582 patent; that the asserted claims of the 218 patent are not invalid as anticipated by certain prior art; and that the economic prong domestic industry was met. The motion was denied on September 7, 2023. Order No. 25.

The evidentiary hearing took place on October 16-20, 2023. Pursuant to the procedural schedule, the parties submitted initial and reply post-hearing briefs on November 6, 2023 and November 17, 2023, respectively.

On October 17, 2023, Realtek moved (1350-042) for partial termination of the investigation by withdrawal of claim 9 of the 582 patent and claim 14 of the 218 patent. The motion was granted via initial determination on October 20, 2023. Order No. 40. On November 14, 2023, the Commission determined not to review Order No. 40. EDIS Doc. ID 808566.

As of the date of this initial determination, three motions remain pending. On October 11, 2023, AMD moved (1350-041) to preclude Realtek from providing Mr. Ying-His Lin as a witness at trial on the topic of a license between Realtek and non-party Avago. On October 13, 2023, Order No. 37 issued which deferred ruling on the motion until after the evidentiary hearing, and otherwise permitted Mr. Lin to provide the challenged testimony. The motion (1350-041) is

hereby denied. As determined below, economic prong domestic industry has not been satisfied on unrelated grounds, so AMD suffers no prejudice from Mr. Lin's testimony.

Additionally, on September 27, 2023, AMD moved (1350-028) *in limine* to preclude Realtek from asserting that the two products it identifies as authorized to practice the asserted patents and as forming the domestic industry in this investigation are in fact licensed. And on October 4, 2023, AMD moved (1350-038) for sanctions against Realtek for failure to timely disclose the existence of a district court litigation relevant to the issue. On October 16, 2023, Order No. 39 issued which determined Realtek had engaged in sanctionable acts during discovery, but otherwise deferred ruling on both motions until after the evidentiary hearing. On November 6, 2023, and pursuant to Order No. 39, AMD filed an accounting of expenses and fees associated with its investigation of the district court litigation (EDIS Doc. ID 807883); and on November 17, 2023, Realtek submitted a response thereto (EDIS Doc. ID 808896). Three days later, on November 20, 2023, Order No. 42 issued which directed AMD to file a response to Realtek's November 17 submission. Order No. 42. That response was filed on November 27, 2023, as directed (EDIS Doc. ID 809330); and, finally, on November 29, 2023, Realtek submitted an unsolicited response thereto (EDIS Doc. ID 809412) which, for the sake of completeness, will be considered.

The two related motions (1350-028, -038) are resolved as follows. AMD's motion *in limine* (1350-028) is denied. Order No. 39 provided the background facts leading to the motion, resolved a portion of the issues, and left open whether the conclusion of the Delaware district court litigation collaterally estops Realtek from asserting in this investigation that non-party Broadcom Corp. is licensed to the asserted patents. *See* Order No. 39. As directed by the order, the parties argue the issue in their post hearing briefing. *Id.* at 8; CIB at 387-395; CRB at 106-108; RIB at

279-282; RRB at 117-120. The Commission has set forth a four-factor test for whether issue preclusion applies, one of which is "3) that the determination of the issue in the prior litigation must have been a critical and necessary part of the judgment in the first action." *Certain Balanced Armature Devices, Products Containing Same, and Components Thereof*, Inv. No. 337-TA-1186, Comm'n Op. at 23 (Oct. 29, 2021) ("*Armature Devices*").

The evidence does not show that the issue of whether "Avago and Broadcom are as AMD frames the disputed question in its motion *in limine*, was a "necessary part" of the judgment in the Delaware actions. Rightly or wrongly, the district court dismissed Case No. 17-1115-GMS for lack of jurisdiction. This is evidenced by both the teleconference in which the dismissal occurred and the published order following that teleconference. RX-1758.13 ("I am just at a loss as to why this case is here in the first place. I think you made a tactical judgment or mistake, quite frankly in filing it here. . . . Again, I don't know why you are here, quite frankly. You shouldn't be here. So you are not going to be here. I am going to dismiss the case. Okay? Anything else? . . . I am dismissing both actions, yes. Anything further?"); RX-1675 ("During a teleconference held on December 19, 2017, the court ordered dismissal of the above-captioned actions."). Indeed, the order explicitly states that it renders "moot" a separate pending motion regarding the status of the Realtek and Broadcom Corp. as or not. *Id.* at 1 n.1 (referring to docket entry D.I. 9). AMD's present assertions—that the only "rational conclusion" is that the case was not dismissed based on jurisdiction (RIB at 280) or that the order was silent as to the grounds for dismissal (*id.* at 280; RRB at 118)—are incorrect.

So it is beside the point that "if in fact the Delaware court somehow dismissed not on the merits, but instead based 'upon an erroneous view or by an erroneous application of the law' of jurisdiction, issue preclusion would nonetheless apply." RIB at 281. Issue preclusion as to some

other issue may apply, but it does not apply to the question of Broadcom's status as an [redacted] of Avago (a question addressed below), because the district court simply did not reach that issue, or any other issue on the merits of Broadcom's motion to dismiss. Accordingly, AMD has not met its burden to show collateral estoppel applies and the remainder of its motion *in limine* is denied.

Turning to AMD's motion for sanctions (1350-038), the remaining issue is the amount and nature of the sanction. As explained in Order No. 39, the misconduct involved Realtek's failure to disclose the existence of the Delaware district court litigation during discovery. Order No. 39 at 1-6. Commission Rule 210.27 permits the administrative law judge to impose an appropriate sanction upon the person who certified the incomplete discovery response, the party on whose behalf the response was made, or both. 19 C.F.R. § 210.27(g)(3)-(5). Having reviewed the parties' filings, an appropriate sanction in this instance is a nominal monetary one against Realtek in the amount of $10,000. This represents a slim portion of the attorney and expert fees sought by AMD because much of that work would have been needed regardless to pursue AMD's affirmative defenses and bears only a tangential relationship to the prior district court litigation. A sizable portion of the requested fees also occurred before September 22, 2023, when AMD or its counsel first learned of that litigation (Order No. 39 at 2), and it has not been shown that that work would have been obviated by an earlier awareness (*e.g.*, collateral estoppel is not present). Further, for that work with a direct connection to the late revelation (*i.e.*, the sanctions motion itself), AMD's counsel seems to have enlisted no less than five partner-level attorneys with near or greater than $1,000/hour billing rates to do the majority of research and drafting. Associate-level attorneys should reasonably have done many of these tasks—associates who are barely present in AMD's

billing records. The appropriate sanction in these circumstances is thus a modest one—$10,000 against Realtek.

Finally, on November 29, 2023, AMD filed a statement indicating that *inter partes* review of the 218 patent had been instituted. EDIS Doc. ID 809420. No other motions remain pending.

B. The Parties

Complainant Realtek Semiconductor Corporation is "a Taiwanese corporation established in 1987." CIB at 1 (citing JX-0813.8). Realtek's principal place of business is in Hsinchu, Taiwan. CPB at 1; RIB at 5.

Respondent Advanced Micro Devices, Inc. is a Delaware corporation headquartered in Santa Clara, CA and founded in 1969. RIB at 5. According to AMD, it is "one of the world's largest integrated circuit developers" and its products "are used in computers, servers, and other applications." *Id.*

C. The Asserted Patents and Claims

The 245 patent, entitled "Stacked Structure of a Spiral Inductor," issued on May 3, 2011 to Kai-Yi Huang, Yuh-Sheng Jean, and Ta-Hsuan Yeh. The 245 patent reports an assignment on its face to Realtek Semiconductor Corp. and claims priority to a foreign application filed May 19, 2009.

The 218 patent, entitled "Power Mesh Arrangement Method Utilized in an Integrated Circuit Having Multiple Power Domains," issued on August 23, 2011 to Chia-Luin Chuang. The 218 patent reports an assignment on its face to Realtek Semiconductor Corp. and claims priority to a foreign application filed November 15, 2007.

The 582 patent, entitled "Semiconductor Device with Inductor-Capacitor Resonant Circuit," issued on March 7, 2017 to Hsiao-Tsung Yen, Yuh-Sheng Jean, and Ta-Hsun Yeh. The

582 patent reports an assignment on its face to Realtek Semiconductor Corp. and claims priority to a foreign application filed April 16, 2014.

The Asserted Patents cover methods for designing integrated circuits. The claims of the 218 patent encompass the use of "local power meshes" and a "global power mesh" to provide power to multiple power domains within the integrated circuit, where the meshes occupy different layers within a vertical stack. *See* 218 patent at cls. 1, 12, 19. The claims of the 245 patent concern another stacked structure for a "spiral inductor" with portions of layers connected to portions of other layers using vias, and with those portions having particular arrangements or dimensions relative to one another. *See* 245 patent at cls. 1, 4, 8. The claims of the 582 patent similarly concern the design of an "inductor-capacitor (LC)" circuit with a variety of layers and conductive segments within those layers having a particular arrangement and connections to one another. *See* 582 patent at cls. 1, 2, 9.

The following patent claims are presently at issue in this investigation, according to Realtek's briefing:

Asserted Patent	Infringement Claims	Domestic Industry Claims
7,936,245	1, 2, 8	1, 2, 8
8,006,218	12-13, 15-18	12-13, 15-18
9,590,582	1-4	1-4

See generally CIB at 7, 16, 18, 19, 23, 24, 67, 218, 300, 326.

D. Products at Issue

1. Domestic Industry Products

The domestic industry articles in this investigation are system-on-chip ("SOC") products; specifically, "Wi-Fi/Bluetooth Chips" from non-party Broadcom Corporation ("Broadcom

Corp.”). CPB at 6. Realtek identifies two models, the BCM4387 and BCM4389, as practicing at least one claim of each asserted patent (hereafter, “DI Products”). CIB at xv.

2. Accused Products

The accused articles in this investigation are, according to Realtek, “system-on-chip (‘SOC’) microprocessors containing inductor-capacitor (‘LC’) resonant circuits” from AMD. CIB at 5. Realtek provides the following classifications and model numbers (“Accused Products”):

Id.

Realtek states that for purposes of infringement under the 218 patent, the parties agree that model numbers within the eight sub-classifications are representative of each other—*i.e.*, there are effectively eight accused products for the 218 patent: . *Id.* at 4-5. Nevertheless, Realtek at times divides the eight sub-classifications into two groups. One group consisting of is referred to as and a second group consisting of is

[redacted]

referred to as [redacted] with both monikers indicating the manufacturer of the articles. *See id.* at xv, xvii, 133-134.

According to Realtek, the parties further agree that for purposes of infringement under the 582 and 245 patents, the same representativeness exists and, further, that certain sub-classifications are representative of one another—*i.e.*, there are effectively five accused products for the 582 and 245 patents: [redacted]. CIB at 4; *see id.* at 317 n.11.

Beyond the Accused Products, AMD argues that an additional thirty-one sub-classifications of processor products exist which "Realtek accused and for which AMD provided extensive discovery, but for which Realtek failed to address in its contentions or at trial." RIB at 295 (citing JX-0036C; RX-1432C; JX-0932C). AMD identifies the products as listed within RX-1432C (RIB at 295, n. 52) (hereafter, "Non-Accused Products") and notes that Realtek has not asserted that any of the eight sub-classifications associated with the Accused Products are representative of any of the thirty-one (*id.*). Thus, AMD reasons, "[a]s Realtek placed those additional thirty-one products at issue in this investigation, obtained discovery on them, and failed to demonstrate infringement, AMD is entitled to a finding of non-infringement." *Id.* (citing *Certain Television Sets, Television Receivers, Television Tuners, and Components Thereof*, Inv. No. 337-TA-910, Initial Determination at 52 (Feb. 27, 2015); *Certain Electrical Connectors and Cages, Components Thereof, and Products Containing the Same*, Inv. No. 337-TA-1241, Comm'n Op. at 37-38 (Sept. 30, 2022)). Realtek does not dispute or even address these positions from AMD. *See generally* CIB; CRB. There being no opposition, and in light of the nature of these devices as falling within the scope of the investigation, the cited evidence of importation, and cited discovery filings (RX-1432C), the Non-Accused Products are determined to be within the scope

of investigation and have not been shown to infringe. *See Certain Human Milk Oligosaccharides and Methods of Producing the Same*, Inv. No. 337-TA-1120, Comm'n Op. at 18 (June 8, 2020) (setting forth four-factor test).

II. STANDARDS OF LAW

A. Standing

Commission Rule 210.12 states in relevant part "[f]or every intellectual property based complaint (regardless of the type of intellectual property involved), [the complaint must] include a showing that at least one complainant is the owner or exclusive licensee of the subject intellectual property." 19 C.F.R. § 210.12(a)(7). In determining whether this rule is met, the Commission looks to the standing requirement used by courts in patent infringement cases. *Certain Audio Processing Hardware, Software, and Products Containing the Same*, Inv. No. 337-TA-1026, Comm'n Op. at 9 (April 18, 2018) (citations omitted).

B. Claim Construction

"The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000). Although most of the disputed claim terms were construed in an earlier order, some of the issues presented below are only resolvable with additional claim construction.

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc); *see also Markman v. Westview Instr., Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc). As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term" as understood by a person of ordinary skill in art at the time of the invention. 415 F.3d at 1313.

"Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). "Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms." *Id.* at 1314; *see Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point [ ] out and distinctly claim [ ] the subject matter which the patentee regards as his invention."). The context in which a term is used in an asserted claim can be "highly instructive." *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.* "Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee." *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1316.

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Phillips*, 415 F.3d at 1317; *see Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can "often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.").

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* "The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

The construction of a claim term is generally guided by its ordinary meaning. However, courts may deviate from the ordinary meaning when: (1) "the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention;" or (2) "the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." *Edwards Lifesciences LLC v. Cook*

Inc., 582 F.3d 1322, 1329 (Fed. Cir. 2009); *see Apple Inc. v. Wi-LAN Inc.*, 25 F.4th 960, 967 (Fed. Cir. 2022); *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."); *Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) ("[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender."); *Rheox, Inc. v. Entact, Inc*., 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution."). Nevertheless, there is a "heavy presumption that a claim term carries its ordinary and customary meaning." *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citations omitted). The standard for deviating from the plain and ordinary meaning is "exacting" and requires "a clear and unmistakable disclaimer." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012); *see Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321, 1334 (Fed. Cir. 2009) (requiring "expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope" to deviate from the ordinary meaning) (citation omitted).

C. Infringement

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman*, 52 F.3d at 976. A patentee may prove infringement either literally or under the doctrine of equivalents. Infringement of either sort must be proven by a preponderance of the evidence. *SmithKline Diagnostics, Inc. v. Helena Labs. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988). A preponderance of the evidence standard "requires

proving that infringement was more likely than not to have occurred." *Warner-Lambert Co. v. Teva Pharm. USA, Inc.*, 418 F.3d 1326, 1341 n.15 (Fed. Cir. 2005).

Literal infringement is a question of fact. *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). "To establish literal infringement, every limitation set forth in a claim must be found in an accused product, exactly." *Microsoft Corp. v. GeoTag, Inc.*, 817 F.3d 1305, 1313 (Fed. Cir. 2016) (quoting *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed. Cir. 1995). If any claim limitation is absent, there is no literal infringement of that claim as a matter of law. *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000).

Doctrine of equivalents is also a form of infringement. One rubric for evaluating if a claimed feature is not literally, but nonetheless equivalent to, a claimed feature is known as the function-way-result test. Under this test, the accused feature is equivalent to the claim limitation when "it performs substantially the same function in substantially the same way to obtain the same result." *Duncan Parking Techs., Inc. v. IPS Grp., Inc.*, 914 F.3d 1347, 1362 (Fed. Cir. 2019) (quoting *Graver Tank & Mfg. Co. v. Linde Air Prods. Co.*, 339 U.S. 605, 608 (1950)). Another is known as the insubstantial differences test, where "[a]n element in the accused device is equivalent to a claim limitation if the only differences between the two are insubstantial." *Voda v. Gordia Corp.*, 536 F.3d 1311, 1326 (Fed. Cir. 2008) (citing *Honeywell Int'l Inc. v. Hamilton Sundstrand Corp.*, 370 F.3d 1131, 1139 (Fed. Cir. 2004)). The Supreme Court has further instructed, "the proper time for evaluating equivalency . . . is at the time of infringement, not at the time the patent was issued." *Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 37 (1997).

In addition to direct infringement, Section 271 of the Patent Act defines two categories of indirect infringement, inducement of infringement and contributory infringement. 35 U.S.C. § 271. For indirect infringement violations under Section 337, the direct infringement element may

occur after importation, so long as all the other elements of indirect infringement are met at the time of importation. *See Certain Vision-Based Driver Assistance System Cameras and Components Thereof*, Inv. No. 337-TA-907, Comm'n Op. at 19 (Dec. 1, 2015) (citing *Suprema, Inc. v. Int'l Trade Comm'n*, 796 F.3d 1338, 1348 (Fed. Cir. 2015)). It is well settled that "[a]bsent direct infringement of the patent claims, there can be neither contributory infringement ... nor inducement of infringement." *Met–Coil Sys. Corp. v. Korners Unltd., Inc.*, 803 F.2d 684, 687 (Fed.Cir.1986) (citations omitted).

As to the first category, "[w]hoever actively induces infringement of a patent shall be liable as an infringer." 35 U.S.C. § 271(b); *see DSU Med. Corp. v. JMS Co.*, 471 F.3d 1293, 1305 (Fed. Cir. 2006) (en banc) ("To establish liability under section 271(b), a patent holder must prove that once the defendants knew of the patent, they actively and knowingly aided and abetted another's direct infringement.") (citations omitted). "The mere knowledge of possible infringement by others does not amount to inducement; specific intent and action to induce infringement must be proven." *Id.* (citations omitted). A defendant's belief regarding patent validity is not a defense to a claim of induced infringement. *Commil USA, LLC v. Cisco Sys., Inc.*, 135 S. Ct. 1920 (2015). A defendant's willful blindness on the question of infringement will satisfy the knowledge requirement. *Global-Tech Appliances, Inc. v. SEB S.A.*, 563 U.S. 754, 765, 768-771 (2011). The requisite intent to induce infringement "may be established through circumstantial evidence" and "'may be inferred from all of the circumstances.'" *See Broadcom Corp. v. Qualcomm, Inc.*, 543 F.3d 683, 699 (Fed. Cir. 2008) (citing *DSU Med. Corp. v. JMS Co.*, 471 F.3d 1293 (Fed. Cir. 2006); *Water Techs. Corp. v. Claco, Ltd.*, 850 F.2d 660, 669 (Fed. Cir. 1988)).

As to the second category, "a party who sells a component with knowledge that the component is especially designed for use in a patented invention, and is not a staple article of

commerce suitable for substantial noninfringing use, is liable as a contributory infringer." *Wordtech Sys., Inc. v. Integrated Networks Solutions, Inc.*, 609 F.3d 1308, 1316 (Fed. Cir. 2010). Contributory infringement is premised upon a finding that: (1) the entity sells, offers to sell, or imports into the United States a component of a product; (2) the component has no substantial non-infringing use; (3) the component constitutes a material part of the claimed invention; (4) the entity was aware of the patent and knew that the product may be covered by a claim of the patent; and (5) the use of the component in the product directly infringes the claim. *See Certain Gaming & Entm't Consoles, Related Software, & Components Thereof*, Inv. No. 337-TA-752, Initial Determination (Remand) at 7-8 (Mar. 22, 2013) (citing 35 U.S.C. § 271(c); *Arris Group v. British Telecomm. PLC*, 639 F.3d 1368, 1376 (Fed. Cir. 2011)), *non-reviewed*, Notice (May 23, 2013). As with inducement, willful blindness on the question of infringement will satisfy the knowledge requirement. *Global-Tech*, 563 U.S. at 765, 768-771.

D. Domestic Industry

In an investigation based on a claim of patent infringement, section 337 requires that an industry in the United States, relating to the articles protected by the patent, exist or be in the process of being established. 19 U.S.C. § 1337(a)(2). Under Commission precedent, the domestic industry requirement has been divided into (i) a "technical prong" (which requires articles covered by the asserted patent) and (ii) an "economic prong" (which requires certain levels of activity with respect to the protected articles or patent itself). *See Certain Video Game Systems and Controllers*, Inv. No. 337-TA-743, Comm'n Op. at 6-7 (April 14, 2011) ("*Video Game Systems*").

1. Technical Prong

The technical prong of the domestic industry requirement is satisfied when the complainant in a patent-based section 337 investigation establishes that it is practicing or exploiting the patents at issue. *See* 19 U.S.C. §§ 1337 (a)(2), (3); *Certain Microsphere Adhesives, Process for Making*

Same and Prods. Containing Same, Including Self-Stick Repositionable Notes, Inv. No. 337-TA-366, Comm'n Op. at 8 (U.S.I.T.C. Jan. 16, 1996). "In order to satisfy the technical prong of the domestic industry requirement, it is sufficient to show that the domestic industry practices any claim of that patent, not necessarily an asserted claim of that patent." *Certain Ammonium Octamolybdate Isomers*, Inv. No. 337-TA-477, Comm'n Op. at 55 (U.S.I.T.C. Aug. 28, 2003). Historically, the Commission permits the complainant's products, and those of its licensees, to be considered for technical prong purposes. *See Certain Magnetic Tape Cartridges and Components Thereof*, Inv. No. 337-TA-1058, Comm'n Op. at 28-29 (April 9, 2019).

The test for claim coverage for the purposes of the technical prong of the domestic industry requirement is the same as that for infringement. *See Certain Doxorubicin and Preparations Containing Same*, Inv. No. 337-TA-300, Initial Determination at 109 (U.S.I.T.C. May 21, 1990), *aff'd*, Views of the Commission at 22 (U.S.I.T.C. Oct. 31, 1990); *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). "First, the claims of the patent are construed. Second, the complainant's article or process is examined to determine whether it falls within the scope of the claims." *Certain Doxorubicin and Preparations Containing Same*, Inv. No. 337-TA-300, Initial Determination at 109. As with infringement, the technical prong of the domestic industry can be satisfied either literally or under the doctrine of equivalents. *Certain Dynamic Sequential Gradient Devices and Component Parts Thereof*, Inv. No. 337-TA-335, ID at 44, Pub. No. 2575 (U.S.I.T.C. May 15, 1992). In short, the patentee must establish by a preponderance of the evidence that the domestic product practices one or more claims of the patent.

2. Economic Prong

The "economic prong" of the domestic industry requirement is satisfied when there exists in the United States, in connection with products practicing at least one claim of the patent at issue: (A) significant investment in plant and equipment; (B) significant employment of labor or capital;

or (C) substantial investment in its exploitation, including engineering, research and development, and licensing. 19 U.S.C. § 1337(a)(3). Establishment of the "economic prong" is not dependent on any "minimum monetary expenditure" and there is no need for complainant "to define the industry itself in absolute mathematical terms." *Certain Stringed Musical Instruments and Components Thereof*, Inv. No. 337-TA-586, Comm'n Op. at 25-26 (May 16, 2008) ("*Stringed Instruments*"). However, a complainant must substantiate the significance of its activities with respect to the articles protected by the patent. *Certain Printing and Imaging Devices and Components Thereof*, Inv. No. 337-TA-690, Comm'n Op. at 30 (Feb. 17, 2011) ("*Imaging Devices*"). Further, a complainant can show that its activities are significant by showing how those activities are important to the articles protected by the patent in the context of the company's operations, the marketplace, or the industry in question. *Id.* at 27-28. That significance, however, must be shown in a quantitative context. *Lelo Inc. v. Int'l Trade Comm'n*, 786 F.3d 879, 886 (Fed. Cir. 2015). The Federal Circuit noted that when the ITC first addressed this requirement, it found the word "'significant' denoted 'an assessment of the *relative* importance of the domestic activities.'" *Id.* at 883-4 (internal citation omitted) (emphasis added). In general, "[t]he purpose of the domestic industry requirement is to prevent the ITC from becoming a forum for resolving disputes brought by foreign complainants whose only connection with the United States is ownership of a U.S. patent." *Certain Battery-Powered Ride-On Toy Vehicles*, Inv. No. 337-TA-314, USITC Pub. No. 2420, Initial Determination at 21 (Aug. 1991); *see Certain Vacuum Insulated Flasks and Components Thereof*, Inv. No. 337-TA-1216, Notice at 3-4 (Oct. 21, 2021) ("Given the nature and extent of [complainant's] investments in plant and equipment as a whole, [complainant] is not a mere importer.").

E. Invalidity

1. 35 U.S.C. § 102

Under the previous version of 35 U.S.C. § 102, a patent claim is invalid as anticipated if:

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant;
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States;

35 U.S.C. § 102 (pre-AIA). Under the current version, a patent claim is invalid as anticipated if:

> (1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention; or
>
> (2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

35 U.S.C. § 102 (AIA). "A patent is invalid for anticipation if a single prior art reference discloses each and every limitation of the claimed invention. Moreover, a prior art reference may anticipate without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference." *Schering Corp. v. Geneva Pharm., Inc.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003) (citations omitted); *see Santarus, Inc. v. Par Pharm., Inc.*, 694 F.3d 1344, 1354 (Fed. Cir. 2012). "A century-old axiom of patent law holds that a product 'which would literally infringe if later in time anticipates if earlier.'" *Upsher-Smith Labs., Inc. v. Pamlab, L.L.C.*, 412 F.3d 1319, 1322 (Fed. Cir. 2005) (citing *Schering Corp.*, 339 F.3d at 1322). Anticipation, and all other grounds of patent invalidity, must be proved by clear and convincing evidence. *Microsoft Corp. v. i4i Ltd. P'ship*, 564 U.S. 91, 95 (2011).

2. 35 U.S.C. § 103

Pursuant to the previous version of 35 U.S.C. § 103:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

35 U.S.C. § 103(a) (pre-AIA). Under the current version:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

35 U.S.C. § 103(a) (AIA). "Obviousness is a question of law based on underlying questions of fact." *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1379 (Fed. Cir. 2008). The underlying factual determinations include: "(1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) objective indicia of non-obviousness." *Id.* (citing *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966)). These factual determinations are often referred to as the "*Graham* factors."

The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-21 (2007). In *KSR*, the Supreme Court rejected the Federal Circuit's rigid application of the teaching-suggestion-motivation test. While the Court stated that "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant

field to combine the elements in the way the claimed new invention does," it described a more flexible analysis:

> Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue . . . . As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 418. Since *KSR*, the Federal Circuit has announced that, where a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device . . . and would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007); *see KSR*, 550 U.S. at 399 ("The proper question was whether a pedal designer of ordinary skill in the art, facing the wide range of needs created by developments in the field, would have seen an obvious benefit to upgrading Asano with a sensor.").

An obviousness determination should also include a consideration of how "secondary considerations" such as "commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." *Graham*, 338 U.S. at 17-18. "For [such] objective evidence to be accorded substantial weight, its proponent must establish a nexus between the evidence and the merits of the claimed invention." *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995); *see Merck & Cie v. Gnosis S.P.A.*, 808 F.3d 829, 837 (Fed. Cir. 2015). "Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no

nexus to the merits of the claimed invention." *In re Huai-Hung Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011); *see Apple Inc. v. Samsung Elecs. Co., Ltd.*, 839 F.3d 1034, 1054-1056 (Fed. Cir. 2016).

3. 35 U.S.C. § 112

The prior version of the Patent Act recites:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

35 U.S.C. § 112 (pre-AIA). Under the current version:

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.
>
> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

35 U.S.C. § 112 (AIA). Pursuant to section 112, a patent claim is invalid for lack of written description if the patent's specification fails to "reasonably convey[] to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). "[T]he test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skilled in the art" (*id.*), and "the level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology" (*id.* (citing *Capon v. Eshar*, 418 F.3d 1349, 1357-58 (Fed. Cir. 2005))).

A patent claim may also be invalid under Section 112 for lack of enablement. To prove that a claim is invalid for lack of enablement, a challenger must show by clear and convincing evidence that a person of ordinary skill in the art would not be able to practice the claimed invention without "undue experimentation." *Alcon Research Ltd. v. Barr Labs., Inc.*, 745 F.3d 1180, 1188 (Fed. Cir. 2014) (citation omitted). "Whether undue experimentation is needed is not a single, simple factual determination, but rather is a conclusion reached by weighting many factual considerations." *In re Wands*, 858 F.2d 731, 736-37 (Fed. Cir. 1988). Those considerations, commonly referred to as the "*Wands* factors," are:

> (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims.

Id. at 737. The Supreme Court has recently explained and held: "If a patent claims an entire class of processes, machines, manufactures, or compositions of matter, the patent's specification must enable a person skilled in the art to make and use the entire class. In other words, the specification must enable the full scope of the invention as defined by its claims. The more one claims, the more one must enable." *Amgen Inc. v. Sanofi*, 598 U.S. 594, 610, (2023).

A patent claim may further be invalid under Section 112 if it is indefinite. The statutory language, "particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention," present in both previous and current versions of the statute, has been interpreted to require the patentee to "be precise enough to afford clear notice of what is claimed, thereby 'apprising the public of what is still open to them.'" *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 909 (citing *Markman*, 517 U.S. at 373). The Court held, "we read § 112, ¶ 2 to require that a patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable

certainty." *Id.* at 910. Thus, a claim is required to "provide objective boundaries for those of skill in the art," and a claim term is indefinite if it "might mean several different things and no informed and confident choice is among the contending definitions." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014). And the Federal Circuit reminds that it is not individual words or even limitations that are judged indefinite, but entire claims. *Cox Commc'ns, Inc. v. Sprint Commc'n Co. LP*, 838 F.3d 1224, 1231-2 (Fed. Cir. 2016) ("As *Nautilus* instructs, the dispositive question in an indefiniteness inquiry is whether the 'claims,' not particular claim terms, 'read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.'").

III. IMPORTATION AND STATUTORY AUTHORITY

Realtek contends, "[t]he Commission has in rem jurisdiction over the Accused Products because AMD has stipulated that they are imported, sold for importation, and sold after importation." CIB at 6 (citing JX-0932C). AMD does not dispute that the Accused Products have been imported, and affirmatively states the Non-Accused Products have as well. *See generally* RIB; RRB.

Accordingly, the importation requirement under 19 U.S.C. § 1337(a)(1)(B) is satisfied, and the Commission has statutory authority over all Accused Products and Non-Accused Products. *See Certain Light-Based Physiological Measurement Devices and Components Thereof*, Inv. No. 337-TA-1276, Comm'n Op. at 15 (Nov. 14, 2023) ("The Commission and ALJs have used the term 'jurisdiction' in the past as a shorthand for statutory authority. Executive agencies, of course, do not have jurisdiction, but rather are creatures of statute that cannot exceed their statutory authority.").

IV. U.S. PATENT NO. 7,936,245

A. Level of Ordinary Skill in the Art

In Order No. 21, I determined that a person having ordinary skill in the art of the 245 patent at the time of invention:

> [W]ould have had at least a bachelor's degree in electrical engineering or an equivalent field, and at least 3-4 years of professional experience in the field of integrated circuit design. . . . Someone with additional education but less professional experience may qualify as a POSITA, such as someone with a master's degree in E.E. and 1-2 years of professional experience in the field of integrated circuit design or someone with a Ph.D. in electrical engineering.
>
> . . . .
>
> [E]xperience may substitute for education and vice versa; thus, graduate studies in electrical engineering or a related field may substitute for work experience and, likewise, additional work experience may substitute for relevant formal education.

Order No. 21 at 7-8. The parties do not challenge this definition (*see generally* CIB; CRB; RIB; RRB), and it is applied throughout this initial determination.

B. Claims-at-Issue

Claims 1, 2, and 8 of the 245 patent are at issue in this investigation, either through allegations of infringement or domestic industry technical prong. *See* CIB at 7, 16, 18, 19, 23, 24. These claims are reproduced below, along with limitation identifiers:

> 1. [1pre] A structure of a spiral inductor, comprising:
>
> [1a] a first metal layer, comprising:
>
> [1b] a first segment;
>
> [1c] a second segment; and
>
> [1d] a third segment, connected to the first segment, wherein a layout direction of the third segment is different from a layout direction of the first segment and a layout direction of the second segment;
>
> [1e] a second metal layer, being positioned under the first metal layer,

[redacted]

[1f] the second metal layer comprising: a fourth segment;

[1g] a fifth segment; and

[1h] a sixth segment, connected to the fifth segment, wherein a layout direction of the sixth segment is different from a layout direction of the fourth segment and a layout direction of the fifth segment;

[1i] a first set of vias, for connecting the first segment with the fourth segment; and

[1j] a second set of vias, for connecting the second segment with the fifth segment;

[1k] wherein the first segment, the fourth segment and the first set of vias construct a first shunt winding; the second segment, the fifth segment and the second set of vias construct a second shunt winding; and the third segment and the sixth segment construct a crossover region.

2. The structure of the spiral inductor of claim 1, wherein the third segment is positioned between the first segment and the second segment; and the sixth segment is positioned between the fourth segment and the fifth segment.

. . . .

8. The structure of the spiral inductor of claim 1, wherein the spiral inductor is a symmetric spiral inductor.

245 patent at cls. 1 (annotated), 2, 8.

C. Claim Construction

As part of the *Markman* process, the following claim terms of the 245 patent were construed, either as-agreed between the parties or determined by Order No. 21:

Claim Term	Construction
"A structure of a spiral inductor, comprising"	Preamble is limiting

See Order No. 21 at 16. Beyond this construction, Realtek explains "[t]he Parties agree all other terms should be given their plain and ordinary meaning." CIB at 6. AMD does not identify particular terms needing construction either. *See generally* RIB at 24; RRB at 6.

[redacted]

D. Infringement

According to Realtek's post-hearing briefing, the use, manufacture, or sale of the Accused Products infringe claims 1, 2, and 8. CIB at 7-18. Of these, claim 1 is independent with claims 2 and 8 each depending from claim 1. For the reasons discussed below, Realtek has shown infringement of these claims by the Accused Products.

1. Claim 1

For reference, claim 1 of the 245 patent requires:

> 1. [1pre] A structure of a spiral inductor, comprising:
>
> [1a] a first metal layer, comprising:
>
> [1b] a first segment;
>
> [1c] a second segment; and
>
> [1d] a third segment, connected to the first segment, wherein a layout direction of the third segment is different from a layout direction of the first segment and a layout direction of the second segment;
>
> [1e] a second metal layer, being positioned under the first metal layer,
>
> [1f] the second metal layer comprising: a fourth segment;
>
> [1g] a fifth segment; and
>
> [1h] a sixth segment, connected to the fifth segment, wherein a layout direction of the sixth segment is different from a layout direction of the fourth segment and a layout direction of the fifth segment;
>
> [1i] a first set of vias, for connecting the first segment with the fourth segment; and
>
> [1j] a second set of vias, for connecting the second segment with the fifth segment;
>
> [1k] wherein the first segment, the fourth segment and the first set of vias construct a first shunt winding; the second segment, the fifth segment and the second set of vias construct a second shunt winding; and the third segment and the sixth segment construct a crossover region.

245 patent at cl. 1 (annotated). In support of its theory and limitation [1pre], Realtek asserts it is met in the Accused Products as per the testimony of Dr. Phinney and the following imagery:

See CIB at 7 (citing CDX-0002C.15; Hr'g Tr. (Phinney) at 76:20-77:4, 86:12-87:4; CPX-0235C; CPX-0375C; CPX-0243C; CDX-0334C; JPX-0206C.10; JPX-0249C.20; CPX-0264C; CPX-0398C; CPX-0282C; CPX-0406C; CPX-0359C; CPX-0367C; CPX-0373C; CPX-0377C; CPX-0718C). As for limitations [1a]-[1d], Realtek contends, pursuant to testimony from Dr. Phinney, that all Accused Products include them as shown in the imagery (using and as exemplary):

[redacted]

[redacted]

See CIB at 7-8 (citing CDX-0002C.20-24, 51-55; Hr'g Tr. (Phinney) at 77:5-78:10, 87:5-88:3; CPX-0237C; CPX-0375C; JX-0024C (Seahra) at 324:15-21, 327:13-24, 331:11-15, 231:10-234:11, 236:16-18; CPX-0048C.21; CPX-0260C; CPX-0398C; JPX-0102C.11-25). As for limitations [1e]-[1h], Realtek contends, pursuant to testimony from Dr. Phinney, that all Accused Products include them as shown in the imagery (using [redacted] and [redacted] as exemplary):

[redacted]

CIB at 9-10 (citing CDX-0002C.25-29, 56-60; Hr'g Tr. (Phinney) at 78:11-80:5, 88:4-89:4; CPX-0238C; CPX-0375C; JX-0024C (Seahra) at 324:15-21, 327:13-24, 331:11-15, 231:10-234:11, 236:16-18; CPX-0048C.21; CPX-0263C; CPX-0398C; JPX-0102C.11-25). As for limitations [1i]-[1j], Realtek contends, pursuant to testimony from Dr. Phinney, that all Accused Products include them as shown in the imagery (using [redacted] and [redacted] as exemplary):

CIB at 10-11 (citing CDX-0002C.30-33, 61-64; Hr'g Tr. (Phinney) at 80:6-81:17, 89:5-90:2; CPX-0235C; CPX-0375C; JX-0024C (Seahra) at 324:15-21, 327:13-24, 331:11-15, 233:11-25; CPX-0048C.21; CPX-0264C; CPX-0398C; JPX-0102C.11-25). AMD does not dispute that the Accused Products meet limitations [1pre]-[1j] (RIB at 24-39; RRB at 6-10), and in light of the testimony of Dr. Phinney, they are determined to be present as alleged.

Limitation [1k] is partially in dispute, however. It can be broken into three clauses: "wherein the first segment, the fourth segment and the first set of vias construct a first shunt winding," "the second segment, the fifth segment and the second set of vias construct a second shunt winding," and "the third segment and the sixth segment construct a crossover region." Realtek first asserts that there is actually no dispute over the last clause, "the third segment and the sixth segment construct a crossover region." CIB at 11. This is confirmed by AMD's briefing (*see generally* RIB at 24-39; RRB at 6-10) and shown in the above imagery.

As to the first two clauses, Realtek contends, as testified by Dr. Phinney, that the first and second "shunt windings" are present, as in the demonstratives shown below for [redacted] and [redacted]:

CIB at 11-12 (citing CDX-0002C.34-37, 65-68; Hr'g Tr. (Phinney) at 81:18-83:4, 90:3-91:1; CPX-0375C; CPX-0235C; CPX-0398C; CPX-0264C). Realtek states that and are "structurally identical" to , and is "structurally identical" to for this limitation (*see* CIB at 12-13), which goes unchallenged by AMD (*see generally* RIB; RRB).

Realtek acknowledges that its identified first, second, fourth, and fifth "segments" are purely straight with no turns, but takes the positions that "the claim language does not require the 'shunt windings' be a complete loop or that the segments be coextensive with the windings" and "Dr. Prucnal has not, and cannot, dispute the windings on both sides of the crossover region of the Accused Products are in shunt." *Id.* at 15. Realtek views AMD as misinterpreting "construct," as used in the claim, with "consist of," which is a distinct concept. CRB at 1-2, 4. Realtek further

points out the 245 patent teaches that the stacked structures shown in its figures "construct" a shunt winding. *Id.* at 2-3 (citing 245 patent at 3:54-4:7, 6:27-28, Figs. 1, 6B).

AMD contends, "[t]he term 'shunt winding' was not construed, and there is no definition in the patent, so the plain and ordinary meaning applies. Dr. Prucnal's unrebutted testimony and associated documentary support shows that a 'shunt winding' is two windings connected in parallel, where a 'winding' consists of a loop or a turn." *See* RIB at 25-26 (citing RX-0326.22; Hr'g Tr. (Phinney) at 114:25-115:3, 108:10-16). AMD continues, "[t]o the extent the 245 patent gives any guidance on the 'shunt winding' term, it is found in Fig. 6B, which, consistent with Dr. Prucnal's interpretation, discloses full windings." *Id.* at 27-28 (citing RDX-0019; 245 patent at 2:45-47, 6:23-28; Hr'g Tr. (Prucnal) at 904:15-907:6). With that construction of "winding" in mind, AMD argues the limitation is not met "because the segments that Dr. Phinney opines construct the 'winding' portion of the 'shunt winding' are mere straight-line segments—with no turn or loop." *Id.* at 29, 34 (citing Hr'g Tr. (Prucnal) at 781:5-783:12, 784:18-785:15, 858:2-8, 901:24-902:6; Hr'g Tr. (Phinney) at 125:7-14)); RRB at 7, 10 ("The claims do not recite a 'shunt-*semi*-winding.'").

The limitation is met as alleged. AMD holds the reasonable view that under a plain and ordinary meaning, a "winding" is a loop or turn. RRB at 10. But the 245 patent clearly uses the term more loosely, in places other than Figure 6B which AMD treats as the only relevant excerpt. RIB at 27 ("To the extent the 245 patent gives any guidance on the 'shunt winding' term, it is found in Fig. 6B"). As one example, Figure 1 is a cross-sectional view of a spiral inductor, and labels delineated vertical stacks of metal segments as "a first shunt winding 130" and "a second shunt winding 140" even though no turns are visible:

[redacted]

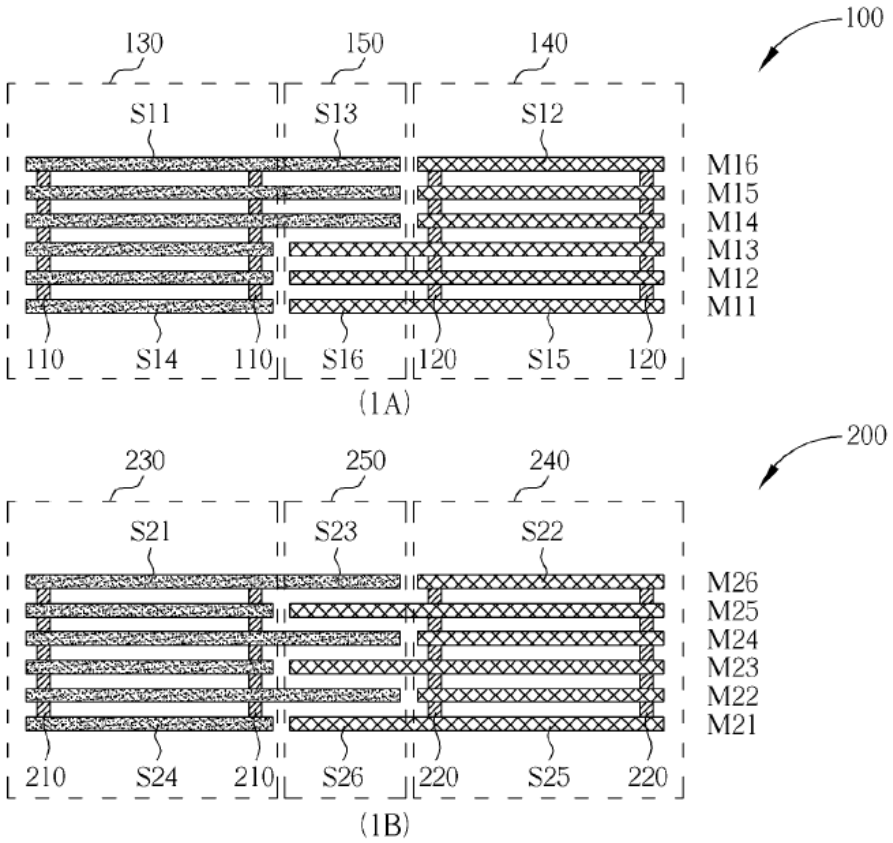


FIG. 1

245 patent at Fig. 1, 3:23-53. AMD dismisses this figure, in particular, with:

> Dr. Prucnal corrected this misguided interpretation, pointing out that box 240 does not depict horizontal segments, but rather a cross-section of the segments (*i.e.*, the segments do not start and end from left to right). Tr. (Prucnal) at 871:10-872:12. These segments extend three-dimensionally into the page and the figure "says nothing about the extent of the segment going into the page." *Id.*

RIB at 38. It is true that Figure 1 is silent on whether extensions exist into or out of the page so as to make the "windings" 130, 140, 230, and 240 compatible with AMD's construction. But there can be no doubt that the next two figures, Figures 2 and 3, are incompatible with that construction:

[redacted]

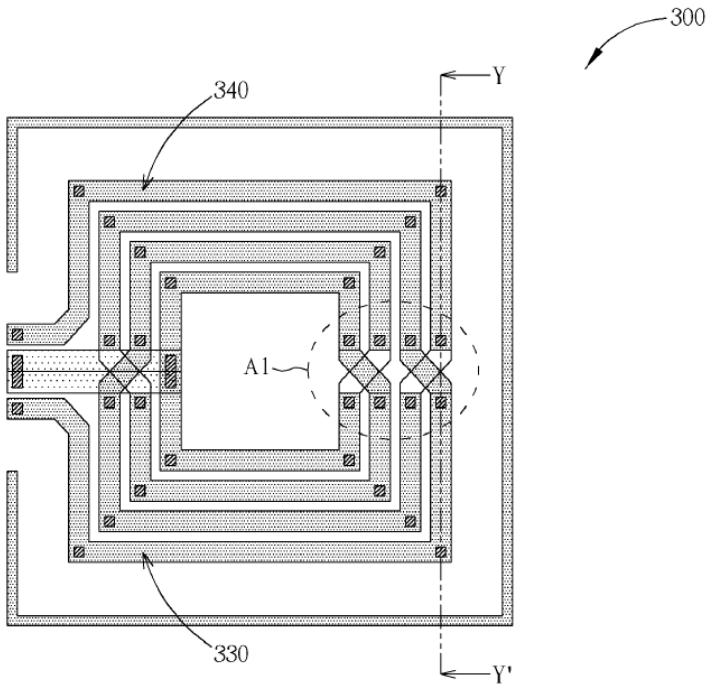


FIG. 2

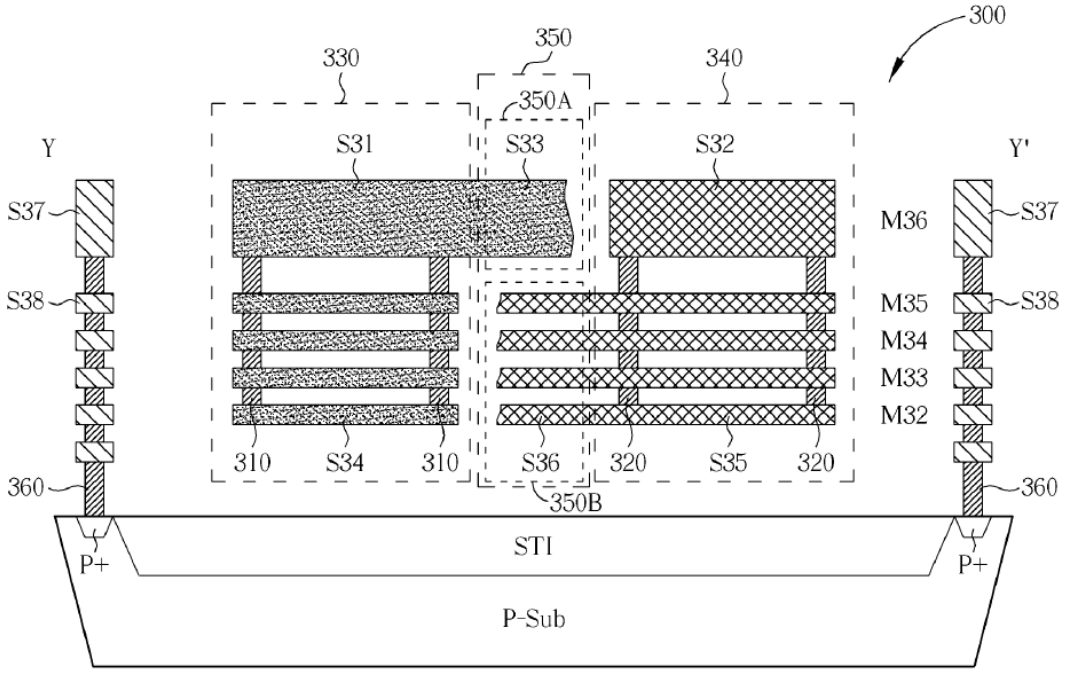


FIG. 3

245 patent at Figs. 2, 3. As is evident, Figure 3 is a cross-section, like Figure 1, and labels similar vertical stacks of metal segments as “a first shunt winding 330” and “a second shunt winding 340”

[redacted]

even though no turns are visible. Figure 3, however, has the added benefit of being taken from a specific location of the spiral inductor of Figure 2—along the Y-Y' line. *See id.* at 4:25-28. That location is straight—with no turns. Moreover, because of that specific location, the "first set of vias 310" and "second set of vias 320" are clearly those that exist at the beginning and end of each straight segment pair: S31/S34 and S32/S35. *See id.* at Fig. 2, 4:28-41. The patent presents the same structures and labels for the embodiments shown in Figures 9-14. *See id.* at Figs. 9-14, 6:64-59.

Thus, the following is clear and unmistakable. The patent identifies straight, no-turn, wire portions as "segments" and views one segment above and one below, with vias connecting the two, as a "shunt winding"—despite an ordinary, customary meaning for "winding" as invoking some amount of turn or loop. To the extent the parties' dispute over this element presents a claim construction issue, this meets the test for inventor lexicography. *Thorner*, 669 F.3d at 1366-67. Infringement of limitation [1k] has been shown.

Accordingly, a preponderance of the evidence shows the Accused Products infringe claim 1.

2. Claim 2

For reference, claim 2 of the 245 patent requires:

> 2. The structure of the spiral inductor of claim 1, wherein the third segment is positioned between the first segment and the second segment; and the sixth segment is positioned between the fourth segment and the fifth segment.

245 patent at cl. 2. Realtek contends, as testified by Dr. Phinney, that the Accused Products include the limitations of claim 2 and offers the following imagery as self-explanatory:

[redacted]

[redacted]

See CIB at 16-17; Hr'g Tr. (Phinney) at 84:21-85:24, 91:15-92:7. AMD does not dispute infringement of claim 2 apart from its dependency on claim 1. RIB at 24-39; RRB at 6-10. In light of the cited evidence and opinion, the additional elements of claim 2 are met in the Accused Products; and the claim is infringed based on claim 1, above.

[redacted]

3. Claim 8

For reference, claim 8 of the 245 patent requires:

> 8. The structure of the spiral inductor of claim 1, wherein the spiral inductor is a symmetric spiral inductor.

245 patent at cl. 8. Realtek contends, as testified by Dr. Phinney, that the Accused Products include the limitations of claim 8 and offers the following imagery as self-explanatory:

[redacted]

[redacted]

See CIB at 18; Hr'g Tr. (Phinney) at 85:25-86:11, 92:8-14. AMD does not dispute infringement of claim 8 apart from its dependency on claim 1. RIB at 24-39; RRB at 6-10. In light of the cited evidence and opinion, the additional elements of claim 8 are met in the Accused Products; and the claim is infringed based on claim 1, above.

[redacted]

E. Domestic Industry – Technical Prong

According to Realtek's post-hearing briefing, the DI Products practice claims 1, 2, and 8 of the 245 patent. CIB at 19-25. For the reasons discussed below, Realtek has shown by a preponderance of the evidence that the DI Products practice these claims.

1. Claim 1

Claim 1 of the 245 patent is presented above in connection with infringement. In support of its theory and limitation [1pre], Realtek asserts it is met in the DI Products as per the testimony of Dr. Phinney and the following imagery:

[redacted]

See CIB at 19-20 (citing CDX-0002C.77-79; Hr'g Tr. (Phinney) at 92:21-93:20; CPX-0178C; CPX-0195C; CPX-0116C; CPX- 0194C; JX-0769C; JX-0770C; JX-0768C; JX-0011C (Chen) at 11:7-14:21, 13:25-23:5). As for limitations [1a]-[1d], Realtek contends, pursuant to testimony from Dr. Phinney, that both DI Products include them as shown below:

See CIB at 20 (citing CDX-0002C.80-84; Hr'g Tr. (Phinney) at 93:21-94:14; CPX-0178C; CPX-0196C; JX-0011C (Chen) at 35:10-36:7, 36:25-37:11; JPX-0120C.11-22; JPX-0123C.10-22). As for limitations [1e]-[1h], Realtek contends, pursuant to testimony from Dr. Phinney, that both DI Products include them as shown below:

Id. at 21 (citing CDX-0002C.85-89; Hr'g Tr. (Phinney) at 94:15-95:8; CPX-0175C; CPX-0196C; JX-0011C (Chen) at 35:10-36:7, 36:25-37:11; JPX-0120C.11-22; JPX-0123C.10-22). As for limitations [1i] and [1j], Realtek contends, pursuant to testimony from Dr. Phinney, that both DI Products include them as shown below:

[redacted]

[redacted]

Id. at 21-22 (citing CDX-0002C.90-92; Hr'g Tr. (Phinney) at 95:9-96:6; CPX-0178C; CPX-0196C; JX-0011C (Chen) at 35:20-24; JPX-0120C.11-22; JPX-0123C.10-22). AMD does not dispute that the DI Products practice limitations [1pre]-[1j] (RIB at 24-39; RRB at 6-10), and in light of the testimony of Dr. Phinney, they are determined to be present as alleged.

Limitation [1k] is, again, partially in dispute. There is no dispute that the DI Products practice "the third segment and the sixth segment construct a crossover region" (*see* CIB at 19, 22-23; RIB at 24-39; RRB at 6-10) which is shown clearly in the imagery above. As for whether the DI Products include first and second "shunt windings," the evidence shows they do. Realtek relies on the testimony of Dr. Phinney and the following imagery:

CIB at 22-23 (citing CDX-0002C.93-96, 97-98; Hr'g Tr. (Phinney) at 96:7-97:5, 97:6-17; CPX-0196C; CPX-0178C; CPX-0191C; CPX-0112C). As determined above, the patent considers straight, no-turn, wire portions as "segments" and views one segment above and one below, with vias connecting the two, as a "shunt winding." *See* 245 patent at Figs. 2, 3, 9-14, 4:15-49, 6:64-8:22. As AMD offers no other grounds of opposition (RIB at 29-39; RRB at 6-10), the limitation is found to be practiced as alleged.

Accordingly, a preponderance of the evidence shows the DI Products practice claim 1.

[redacted]

2. Claim 2

Claim 2 of the 245 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Phinney, that the DI Products practice the limitations of claim 2 and offers the following imagery as self-explanatory:

[redacted]

See CIB at 23-24 (citing CDX-0002C.100-101; Hr'g Tr. (Phinney) at 97:18-98:5, 97:18-98:5; C[P]X-0178C; CPX-0116C; CPX-0175C; CPX-0112C). AMD does not dispute practice of claim

2 apart from its dependency on claim 1. RIB at 24-39; RRB at 6-10. In light of the cited evidence and opinion, the additional elements of claim 2 are practiced by the DI Products; and the claim is practiced based on claim 1, above.

3. Claim 8

Claim 8 of the 245 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Phinney, that the DI Products practice the limitations of claim 8 and offers the following imagery as self-explanatory:

See CIB at 24-25 (citing CDX-0002C.103; Hr'g Tr. (Phinney) at 98:6-13; CDX-0178C; CPX-0116C). AMD does not dispute practice of claim 8 apart from its dependency on claim 1. RIB at 24-39; RRB at 6-10. In light of the cited evidence and opinion, the additional elements of claim 8 are met in the DI Products; and the claim is practiced based on claim 1, above.

F. Validity

AMD identifies the following invalidity theories for the 245 patent:

Claims	Theory
1, 2, 8	Anticipated under 35 U.S.C. § 102 by Qualcomm RFR6122 (JX-0580)

1, 2, 8	Anticipated under 35 U.S.C. § 102 by Marvell 88W8686 (JX-0743)
1, 2, 8	Anticipated under 35 U.S.C. § 102 by Ho-Hsiang (JX-0053)
1, 2, 8	Anticipated under 35 U.S.C. § 102 by Christensen (JX-0080)
1, 2, 8	Rendered obvious under 35 U.S.C. § 103 by Yang (JX-0213) in view of Chang (JX-0176)
1, 2, 8	Indefiniteness under 35 U.S.C. § 112

See generally RIB at 40-115. The parties have several disputes concerning the prior art status of AMD's references, including dates of priority and invention for the 245 patent itself, and pertinent dates for the references themselves. No party disputes that the 245 patent is entitled to a priority date of at least May 19, 2009, when the initial Taiwanese Application No. 98116543 ("TW Application") was filed. CIB at 25; RIB at 5, 7 n.3. Nor does any party dispute that because of this date, the pre-AIA version of the relevant statutes apply. RIB at 7.

Starting with the printed references, AMD implies, but does not directly state, that several are prior art under 35 U.S.C. § 102(b) (pre-AIA). *See* RIB at 7 (discussing requirements for Section 102(b)). U.S. Patent No. 6,794,977 ("Christensen") issued on September 21, 2004, which was more than one year before the May 19, 2009 priority date of the 245 patent (JX-0080), so it qualifies as prior art under this subsection. Similarly, U.S. Patent No. 6,885,275 ("Chang") issued on April 26, 2005, which was more than one year before the priority date of the 245 patent (JX-0176), so it, too, qualifies as prior art under 102(b).

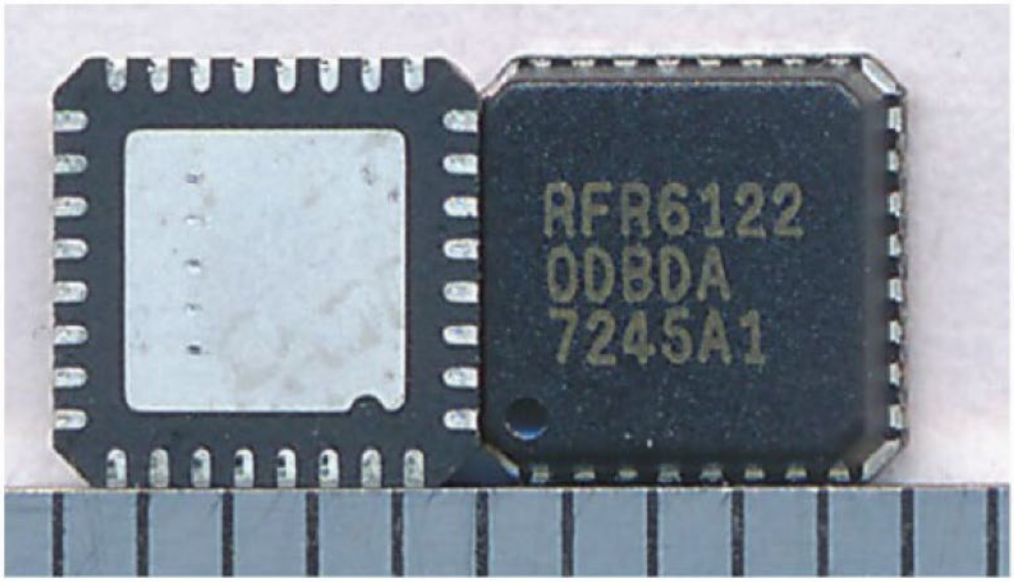
AMD provides no explanation whatsoever as to why U.S. Pub. No. 2009/0002114 ("Yang") is prior art to the 245 patent; nor did Dr. Prucnal at the evidentiary hearing. *See* RIB at

24, 98-109; RRB at 17-20; Hr'g Tr. (Prucnal) at 848:5-16. And, based on its publication date of January 1, 2009, it cannot qualify under Section 102(b), nor does AMD argue that it qualifies under any other subsection of Section 102. *See* RIB at 7-24, 98. So while Realtek does not offer a dispute on Yang's prior art status, it cannot be said AMD has presented a clear and convincing case for invalidity based on Yang. *Microsoft*, 564 U.S. at 95. It will not be considered in the invalidity analysis, and so the proposed obviousness combination with Chang—which actually is prior art under 102(b) because it issued in 2005—is moot. U.S. Patent No. 7,821,372 ("Ho-Hsiang") is another reference for which AMD fails to identify which subsection of 35 U.S.C. § 102 (pre-AIA) confers prior art status (*see* RIB at 7-24, 74-76; RRB at 2-6, 13-16). Based on its issue date of October 26, 2010 it cannot fall under Section 102(b), and AMD does not argue that it qualifies under any other subsection of Section 102. It is similarly not considered for invalidity purposes, and Realtek's assertions regarding an earlier conception and reduction to practice of the 245 patent are therefore moot.

The parties further dispute the 102(b) status of two physical integrated circuit products alleged to have been used or sold more than one year before May 19, 2009: Qualcomm RFR6122 and Marvell 88W8686. AMD presents a collection of third-party technical reports, sales records from Qualcomm and Marvell, and other datasheets in support of their prior art status. *See generally* RIB at 7-22; RRB at 2-5. Realtek argues that AMD has failed to show that the specific chips compared against the asserted claims are the same chips documented in the predating records. *See generally* CIB at 36-37, 39-40; CRB at 13-14, 17-18.

The evidence demonstrates a clear and convincing case that the Qualcomm RFR6122 and Marvell 88W8686 were on sale or publicly used more than one year before May 19, 2009. AMD presents teardown reports from well-known reverse-engineering company TechInsights, dated

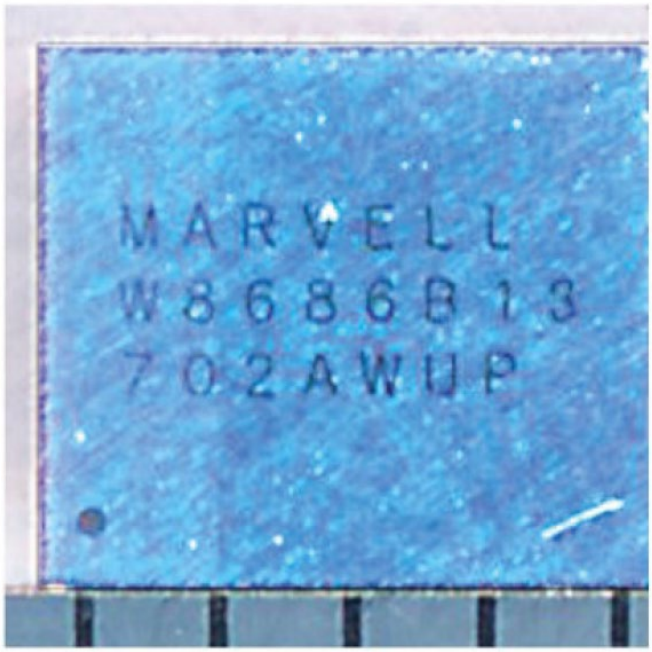
between September 28, 2006 and February 11, 2008, which analyze the RFR6122 and 88W8686 chips. JX-0265; JX-0258; JX-0264; *see* RIB at 8-9. This is strong evidence that those chips were commercially available, for TechInsights to acquire, at least by those report dates. In addition, AMD cites sales sheets produced from Qualcomm and Marvell during fact discovery that bear all the indicia of ordinary business records and list of the RFR6122 and 88W8686—again, with dates far preceding May 19, 2008 and with customers located within the United States . JX-0897C; JX-0914C; *see* RIB at 10-13. AMD further provides press releases and datasheets all confirming the RFR6122 and 88W8686 were well-known and well-adopted into popular consumer electronic products of their time. *See generally* RIB at 14-22. Lastly, AMD, based on the testimony of Dr. Subramanian, explains that the exact chips dissected in the ICmasters' reports and used to compare against the claims of the 245 patent bear markings indicating their manufacture dates—again, well before May 19, 2008:



RFR6122
0DBDA
7245A1

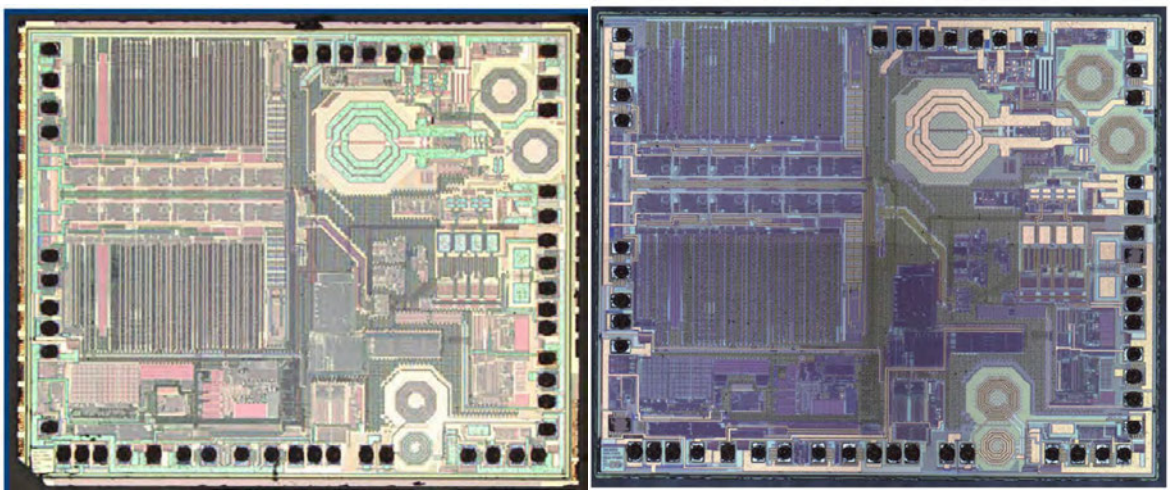
Package

[redacted]

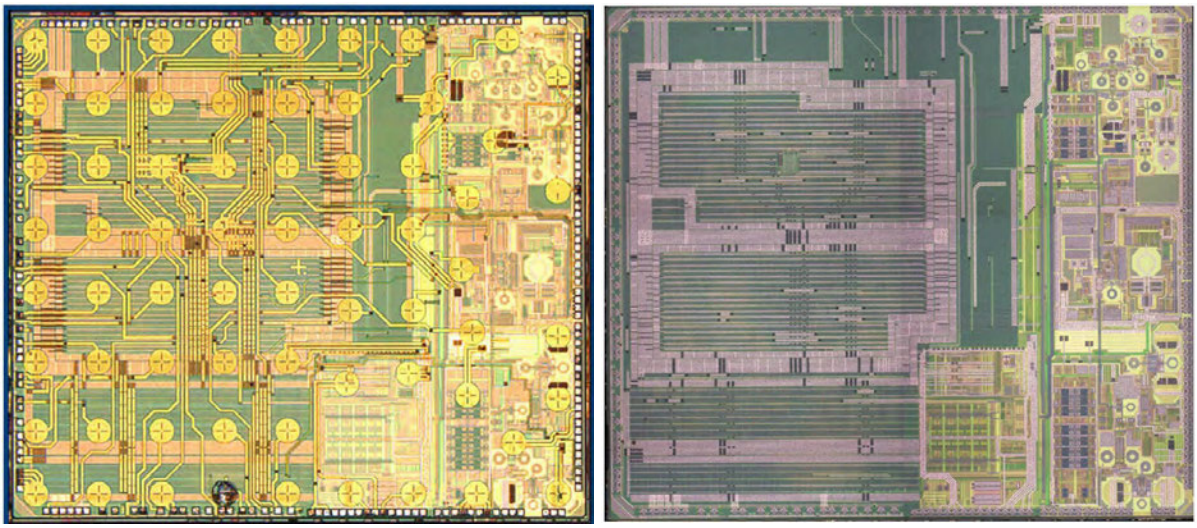


Package

RIB at 16 (citing JX-0580.3; Hr'g Tr. (Subramanian) at 1002:6-23, 1005:9-1006:4 (explaining 724 means 24th week of 2007), 21-22 (citing JX-0743.3; Hr'g Tr. (Subramanian) at 1006:5-1007:3 (explaining 702 means 2nd week of 2007)). It is further valuable to note that the overall chip layouts appear substantially identical between the TechInsights' reports and the ICmasters' reports:



(JX-0265.17 (RFR6122); JX-0580.4 (RFR6122); *see* JX-0756.17 (2006 Portelligent Teardown Report, overall chip));



(JX-0258.35 (88W8686); JX-0743.4 (88W8686)).

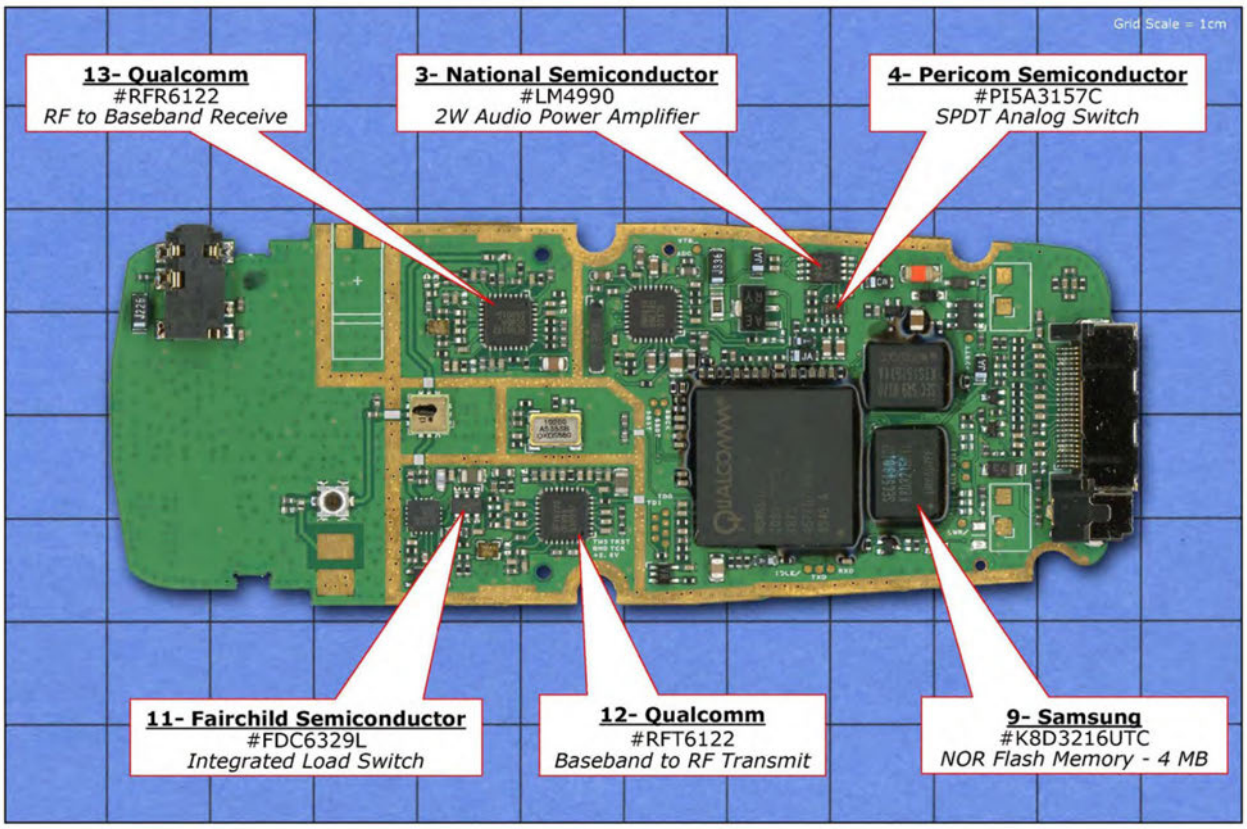
Realtek's opposition here is limited and conclusory. Realtek posits, without expert testimony or other supporting documentary evidence, that the chips commercially available before May 19, 2008 may have been different "versions" from those analyzed by ICmasters. *See* CIB at 36-37 (stating generally "different products have different layouts"), 39-40; CRB at 13-14, 17-18. This is speculative attorney argument and does not overcome the continuity of images between the TechInsights' and ICmasters' reports, nor the individual chip date stamps reproduced above. It is far from persuasive.

Accordingly, the Marvell 88W8686 and Qualcomm RFR6122 are prior art to the 245 patent under 35 U.S.C. § 102(b).

1. Qualcomm RFR6122

According to AMD, the Qualcomm RFR6122 is a "mobile phone cellular receiver" which was introduced in November 2003. RIB at 14 (citing JX-0229). AMD reports, "[b]y November 2004, the RFR6122 was in commercial production, with Qualcomm confirming the product had

received 'broad acceptance' with 'more than 40' mobile devices commercially available with the MSM6000/MSM6025 chipsets containing the RFR6122," among other devices. *Id.* (citing JX-0233). AMD provides the following image from a 2006 teardown report showing its location within an exemplary mobile device:

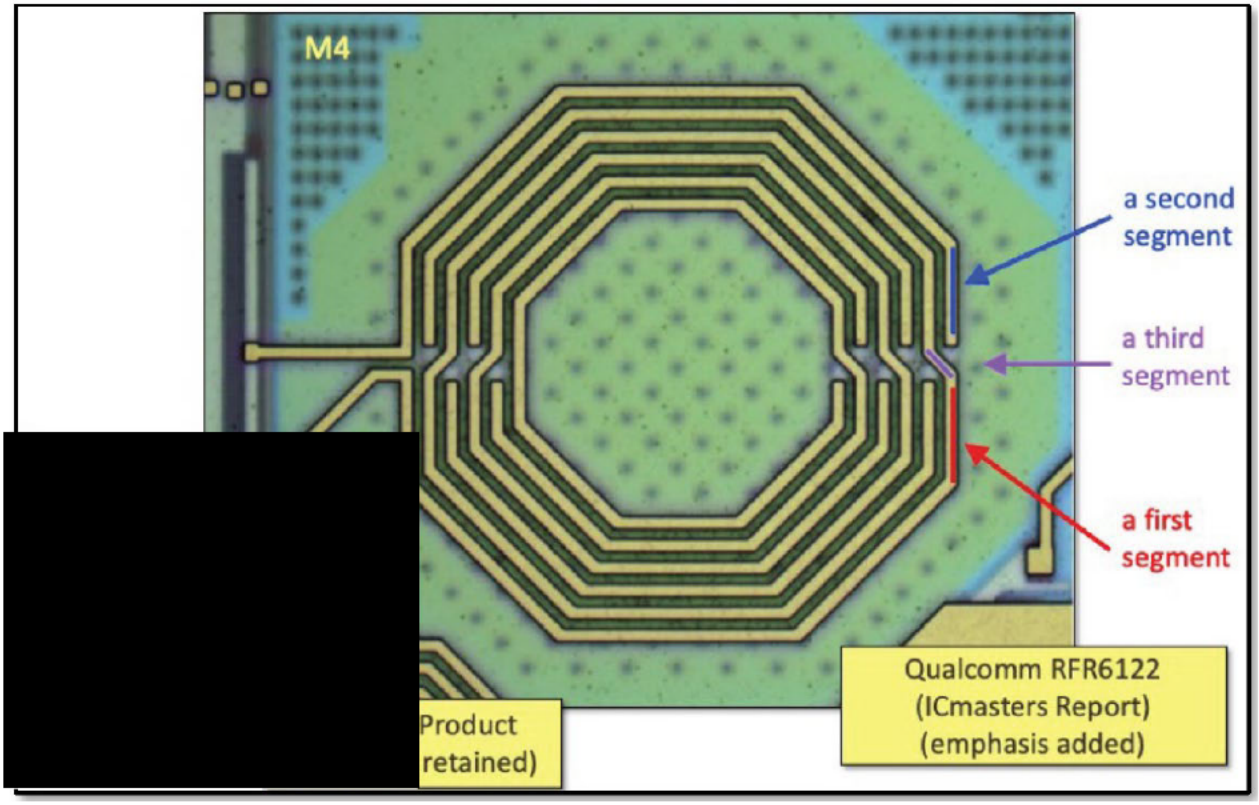


Id. at 14-15 (citing JX-0756). AMD contends the asserted claims are anticipated by the RFR6122. For the reasons discussed below, AMD has shown claims 1, 2, and 8 are anticipated.

a. Claim 1

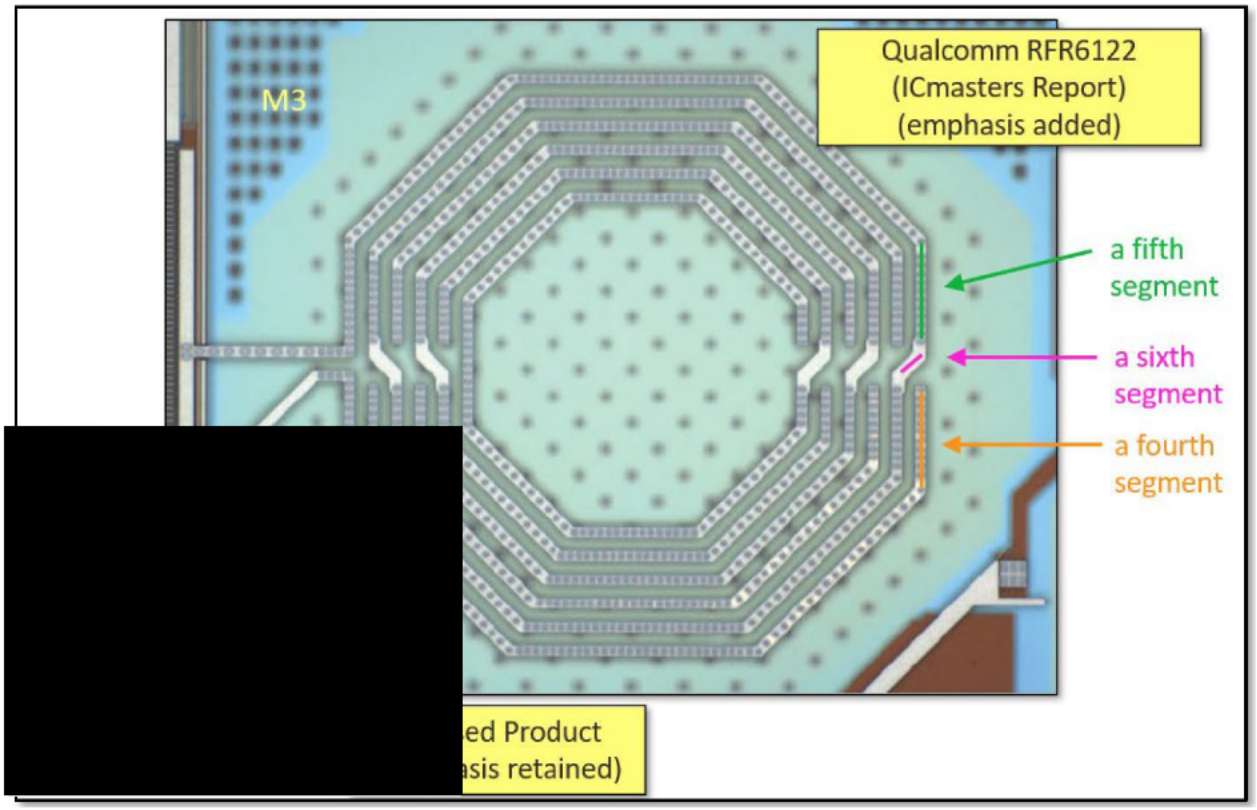
Claim 1 is presented above. AMD contends each limitation is present in the RFR6122 thus anticipating the claim. AMD represents that there is no dispute that the RFR6122 contains a spiral inductor (RIB at 42-43 (citing Hr'g Tr. (Prucnal) at 794:3-14)), nor is there a dispute over a first metal layer (M4) with first through third metal segments (*id.* at 44-46 (citing Hr'g Tr. (Prucnal) at 794:19-795:5)):

[redacted]



RDX-0001C.37. AMD further represents there is no dispute over a second metal layer (M3) with the accompanying fourth through sixth metal segments (RIB at 46-47 (citing Hr'g Tr. (Prucnal) at 796:20-797:14)):

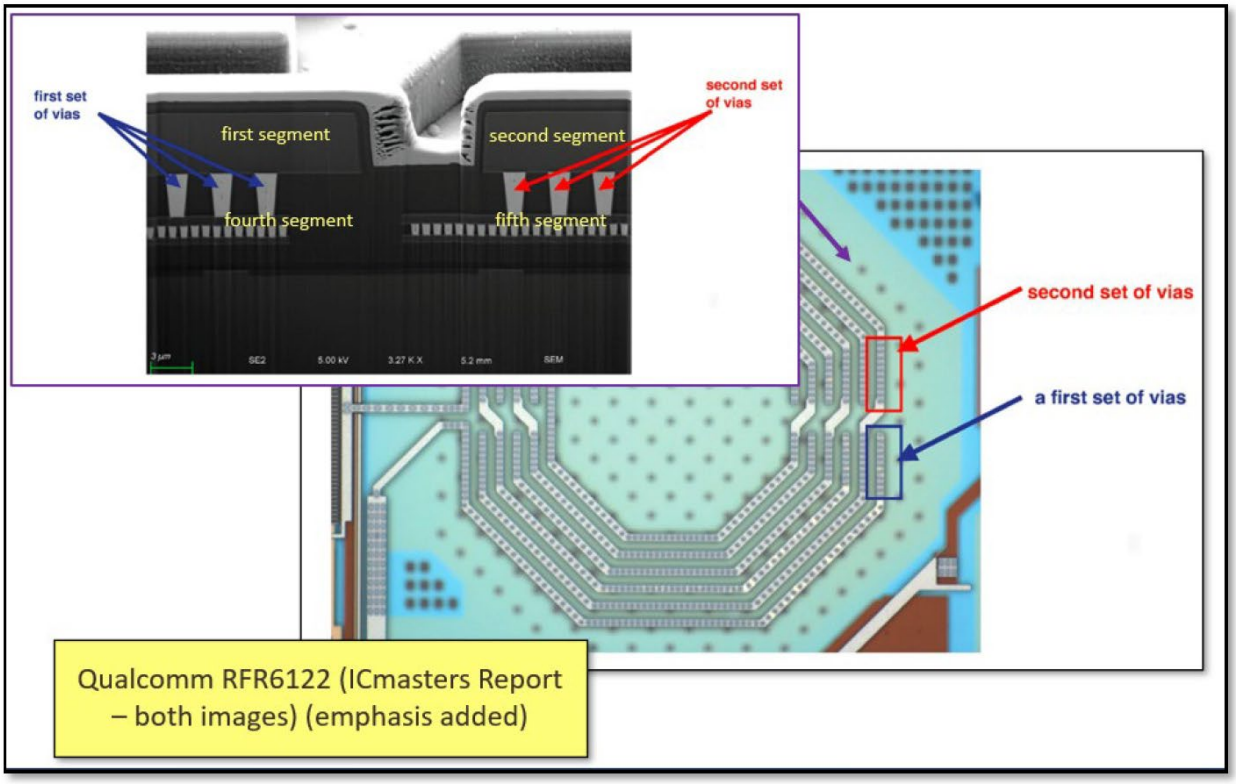
[redacted]



RDX-0001C.40.

AMD then contends, based on the testimony of Dr. Prucnal, that "the RFR6122 includes a first set of vias connecting the first and fourth segments and a second set of vias connecting the second and fifth segments" as shown below with "dotted vias connecting upward to the first metal layer":

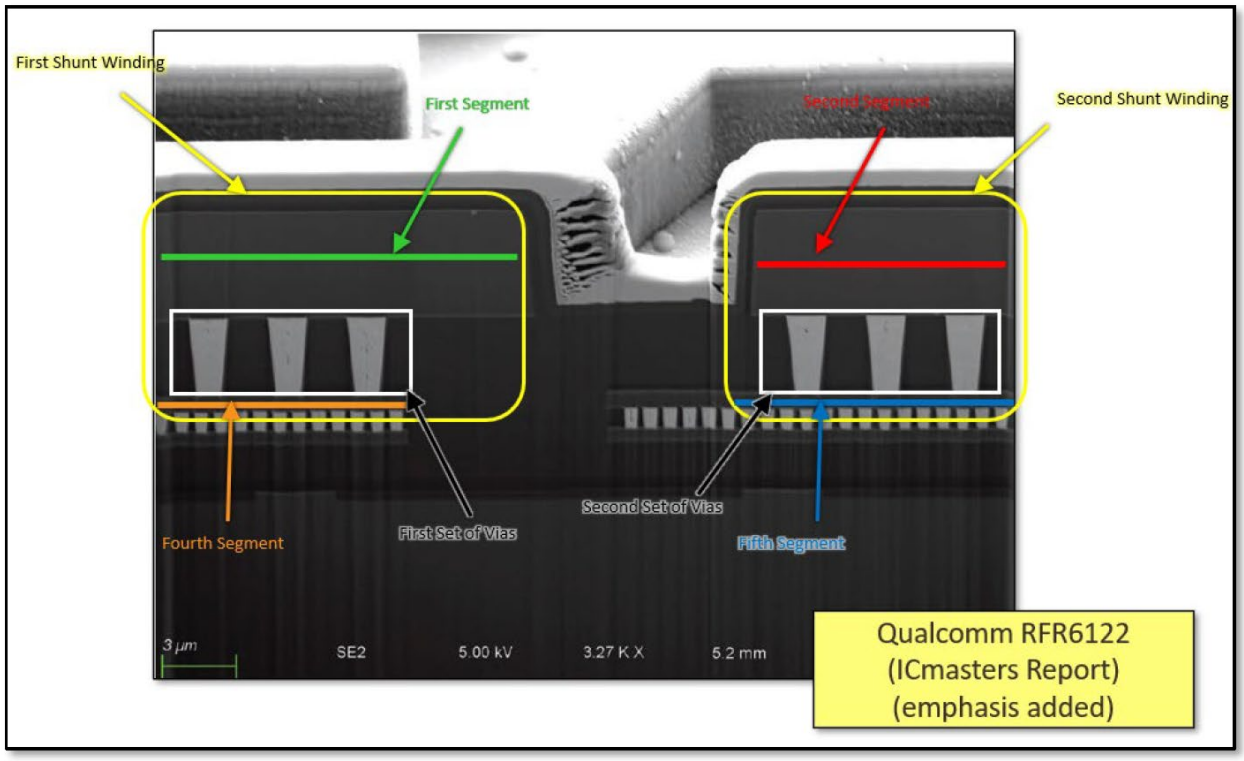
[redacted]



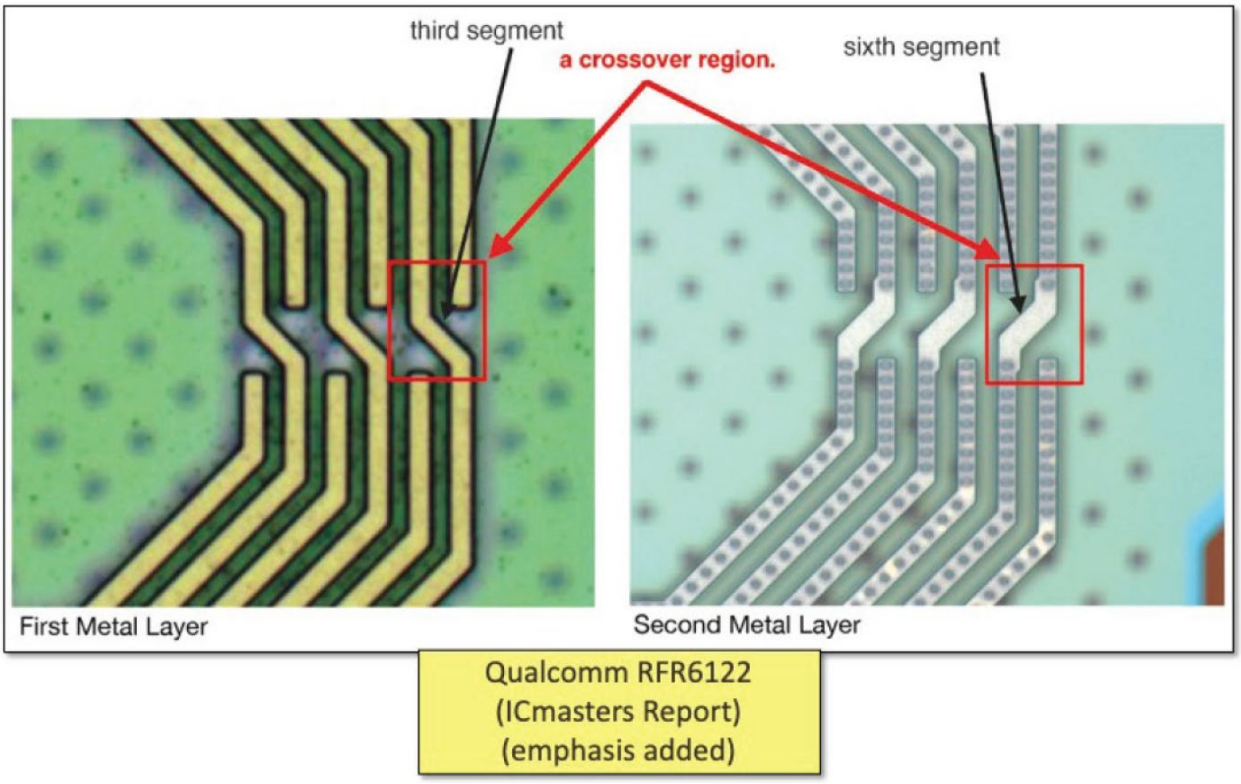
RDX-0001.41. As for the creation of shunt windings, AMD explains:

> Dr. Prucnal testified the first and fourth segments together with the first set of vias construct a first shunt winding, and the second and fifth segments together with the second set of vias construct a second shunt winding under Dr. Phinney's interpretation. Tr. (Prucnal) at 798:20-799:13, 801:8-19. The first and second shunt windings are depicted below in the same manner as what Dr. Phinney identified for the AMD and Broadcom products. *Id.*; *see id.* at 781:6-23.

[redacted]



RIB at 48-49; RDX-0001.42. Finally, AMD provides the following image to show the third and sixth segments creating a crossover region, and represents it is undisputed in the RFR6122:



RIB at 50-53 (citing RDX-0001.43; JX-0580.12-13; Hr'g Tr. (Prucnal) at 802:1-803:2). The limitations are present in the RFR6122 as alleged.

Realtek's points in opposition are not persuasive. It first argues AMD and Dr. Prucnal have failed to show the device in the TechInsights report and the ICmasters device are the same (CIB at 40-41; CRB at 18-19), but as shown above, it is the ICmasters report that demonstrates all features of claim 1. AMD clarifies in its reply brief, "Dr. Prucnal explained that his analysis was focused on high-resolution images of *one* inductor in the *ICmasters Report* not the TechInsights Report." RRB at 29 (citing Hr'g Tr. (Prucnal) at 789:3-790:10) (emphasis in original).

Realtek also criticizes Dr. Prucnal "because he utilizes purported top layers from two different electrical devices on RFR6122." CIB at 41. But it is unclear which electrical devices Realtek refers to here, as Dr. Phinney offered no corroborating opinion (*see* Hr'g Tr. (Phinney) at 1224:2-10) and the imagery above consistently shows the same spiral inductor.

Realtek also complains that the cross-sectional image presented above fails to "show a sixth segment or the construction of a crossover region" (CIB at 41 (citing Hr'g Tr. (Phinney) at 1224:2-10), 44), but the cross-sectional image does show the beginning of the sixth segment, much in the way the 245 patent does. *Compare* JX-0580.12 *with* 245 patent at Fig. 3. This is true despite Dr. Prucnal's admitting on cross-examination that it perhaps cannot be seen. Hr'g Tr. (Prucnal) at 894:9-17; *but see id.* at 894:18-895:8. Regardless, the top-down views show the sixth segment and crossover region clearly. RIB at 53 (citing RDX-0001.45; JX-0580.12). Realtek then argues that "serial SEM cross-sectional images," a "top-view image of an isolated M3 layer," or a "layout/GDS file" are the sort of additional evidence needed to show all elements of claim 1. CIB at 44. But these sorts of assertions require expert explanation and Dr. Phinney's testimony is only conclusory and brief:

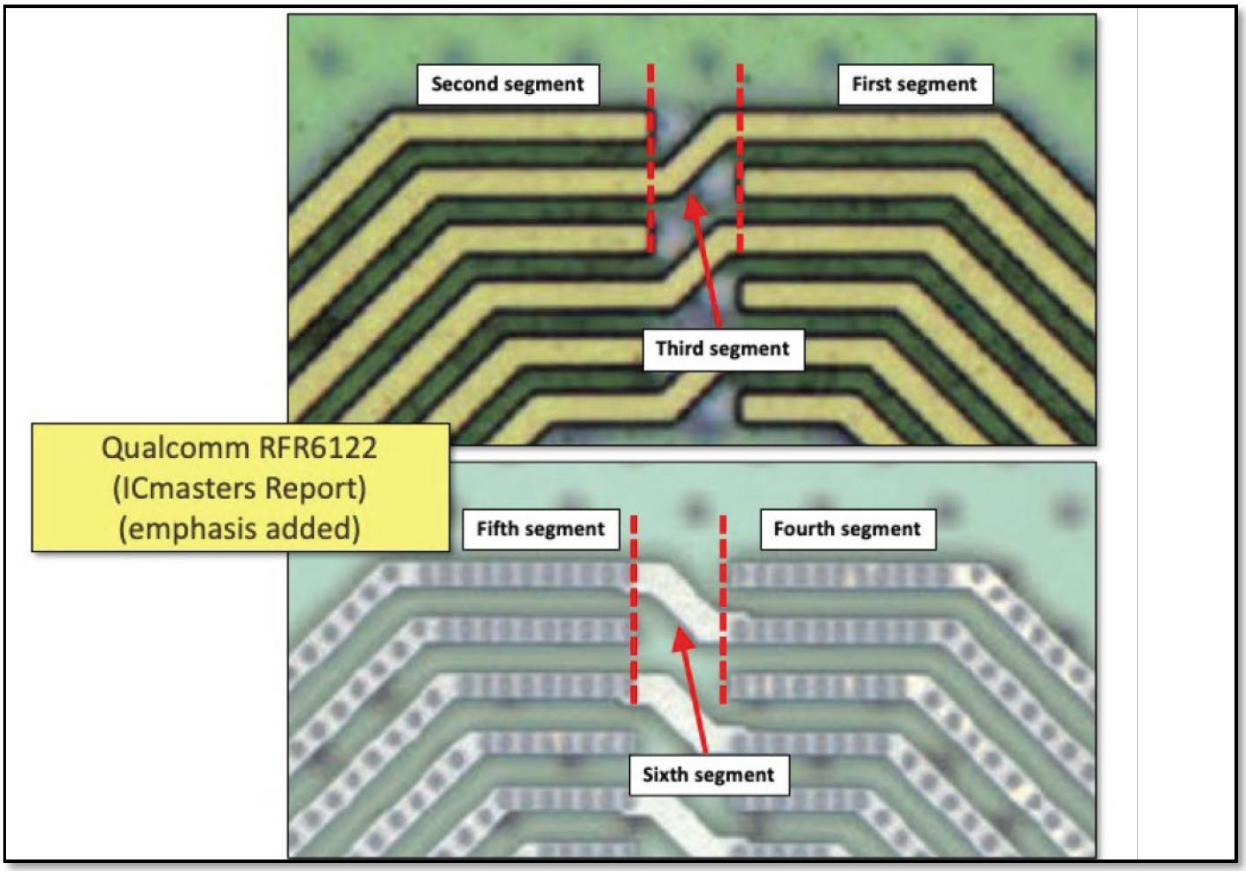
> Q. All right. Moving on to slide 38, which is the Qualcomm RFR6122 product, does this anticipate the '245 patent?
>
> A. It doesn't. It does not depict a sixth segment. I understand Dr. Prucnal to agree with this. Therefore, things like the sixth segment or crossover region constructed from there, I don't – I don't think that we have the evidence to look at those structures one on top of the other in cross-section to demonstrate that.
>
> Q. And if GDS files were provided for the RFR6122 product, would you have been able to confirm whether there was a sixth segment or not?
>
> A. That would be a great way to confirm, but we don't – I didn't see GDS files for this product.
>
> Q. Please move on to slide 40. And can you summarize your overall opinion regarding the Qualcomm product?
>
> A. That the Qualcomm product neither anticipates or renders obvious the asserted claims of the '245.
>
> Mr. Engel: Your Honor, we will pass the witness at this point.

Hr'g Tr. (Phinney) at 1224:2-22. Altogether, the Qualcomm RFR6122 meets the limitations of claim 1 in the same fashion as the Accused Products and DI Products.

Accordingly, claim 1 is invalid as anticipated over the Qualcomm RFR6122.

b. Claim 2

As for claim 2, AMD contends the identified third segment is between the first and second, and the sixth is between the fourth and fifth:



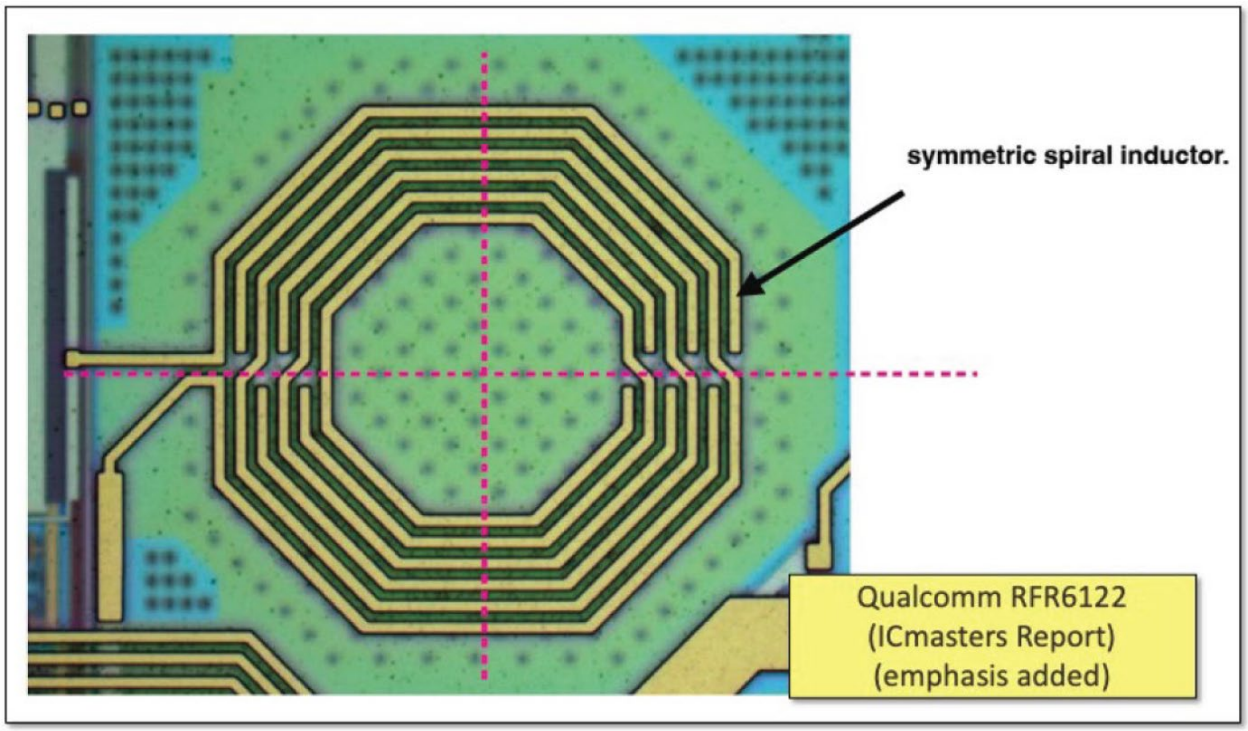
RIB at 53 (citing RDX-0001.46; Hr'g Tr. (Prucnal) at 804:3-16). Realtek does not dispute claim 2 (*see* CIB at 40-44; CRB at 18-21) separately from claim 1, and it is met as alleged.

Accordingly, claim 2 is invalid as anticipated over the Qualcomm RFR6122.

[redacted]

c. Claim 8

As for claim 8, AMD contends the inductor is symmetrical as follows:



RIB at 54-55 (citing RDX-0001.47; Hr'g Tr. (Prucnal) at 804:17-805:12). Realtek does not dispute claim 8 (*see* CIB at 40-44; CRB at 18-21) separately from the other claims, and it is met as alleged.

Accordingly, claim 8 is invalid as anticipated over the Qualcomm RFR6122.

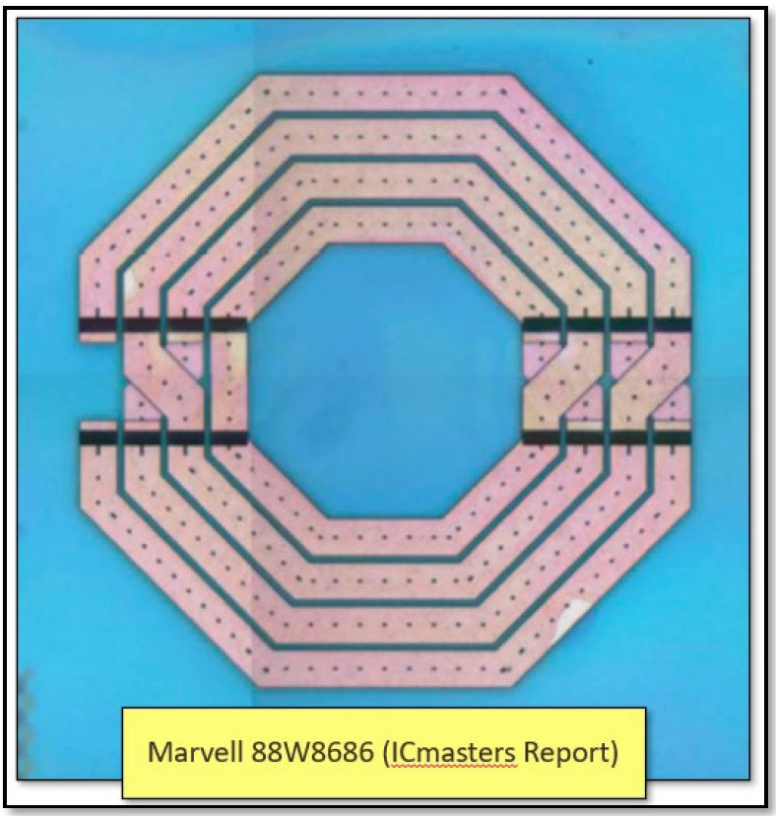
2. Marvell 88W8686

According to AMD, and a 2005 press release from Marvell, the 88W8686 was "the world's first ultra-low-power 90 nm Wireless LAN (WLAN) single chip solution." RIB at 19 (citing JX-0617). AMD cites a 2007 publication which further described the chip as an innovative "RF IC transceiver" and notes "Apple selected the 88W8686 to be the RF transceiver in the first iPhone." *Id.* (citing JX-0887); *see id.* at 19-20 (citing JX-0717; JX-0887). AMD contends the asserted claims are anticipated by the 88W8686. For the reasons discussed below, AMD has shown claims 1, 2, and 8 are invalid.

[redacted]

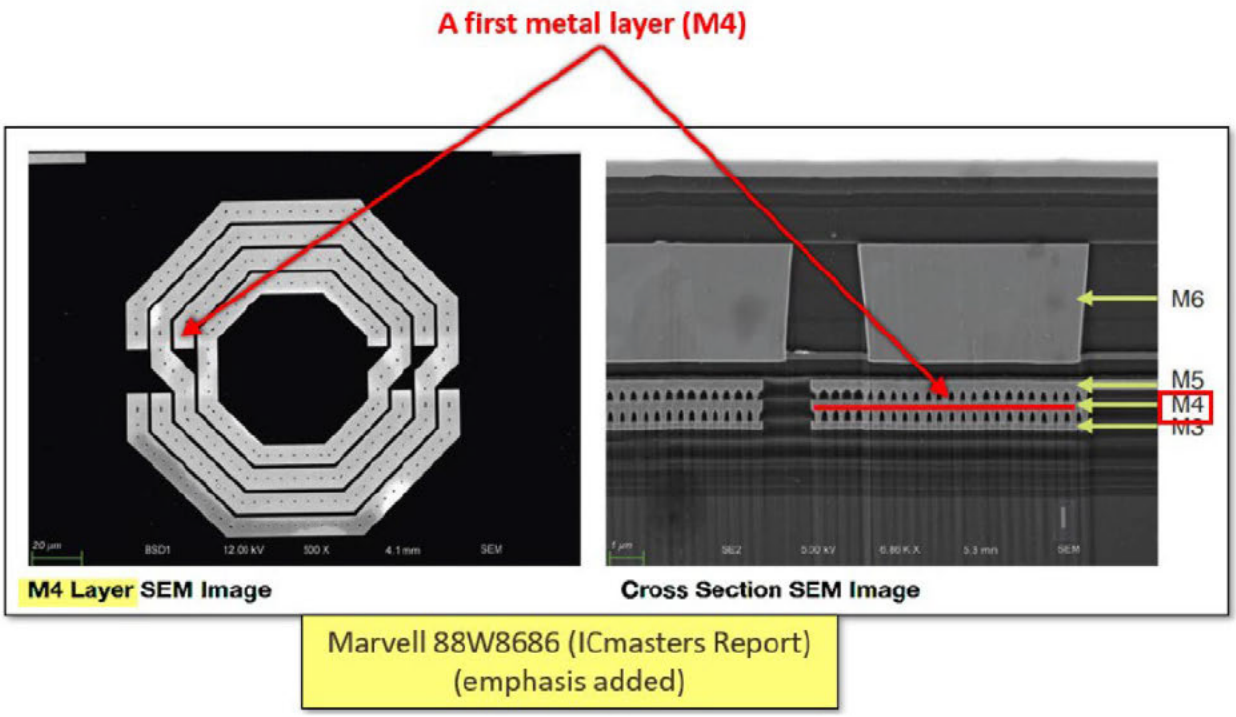
a. Claim 1

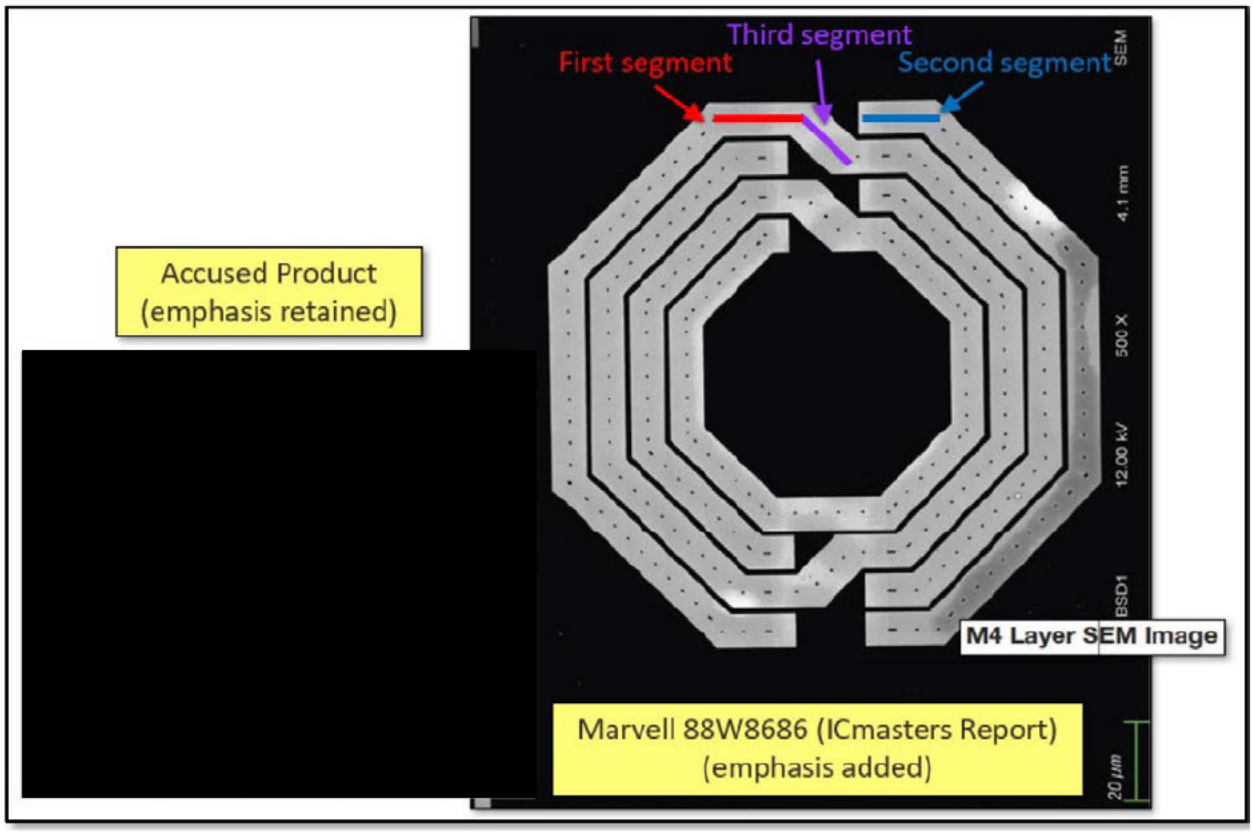
Claim 1 is presented above. As for the preamble, "a spiral inductor," AMD provides the following image taken from the ICmasters report:



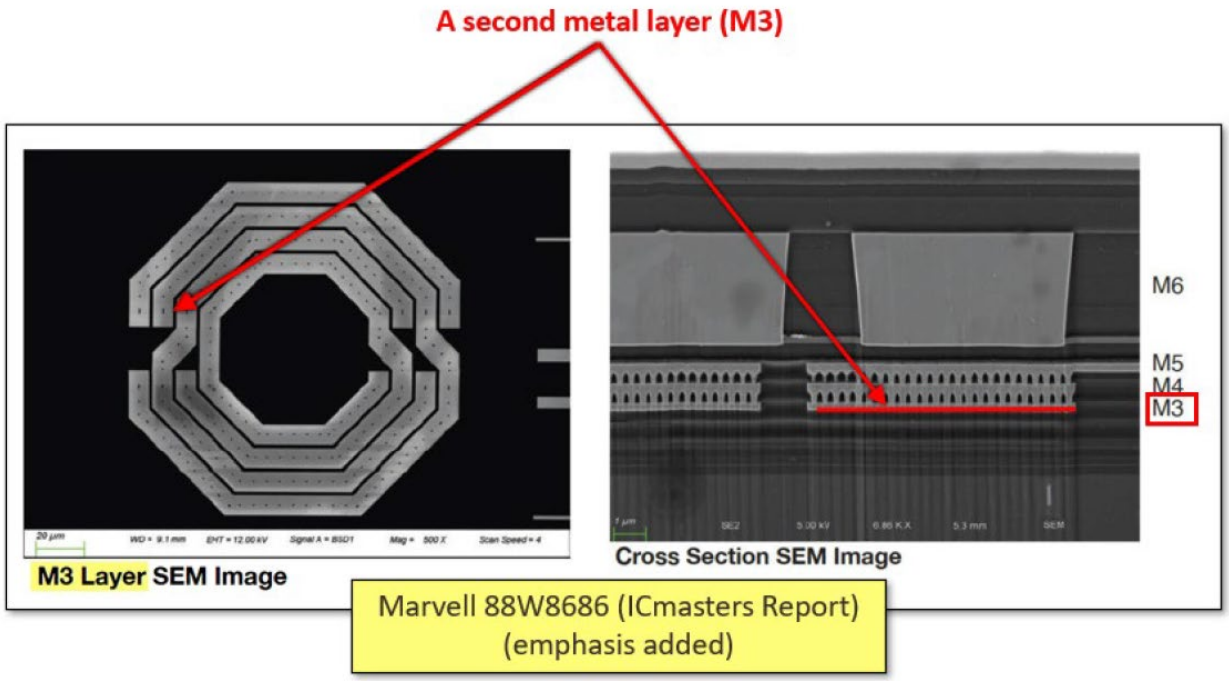
RIB at 59-61 (citing JX-0743.6; Hr'g Tr. (Prucnal) at 807:15-808:1; JX-0258.59). For the limitation reciting a first metal layer (M4) and first, second, and third segments, AMD points to the following imagery:

[redacted]

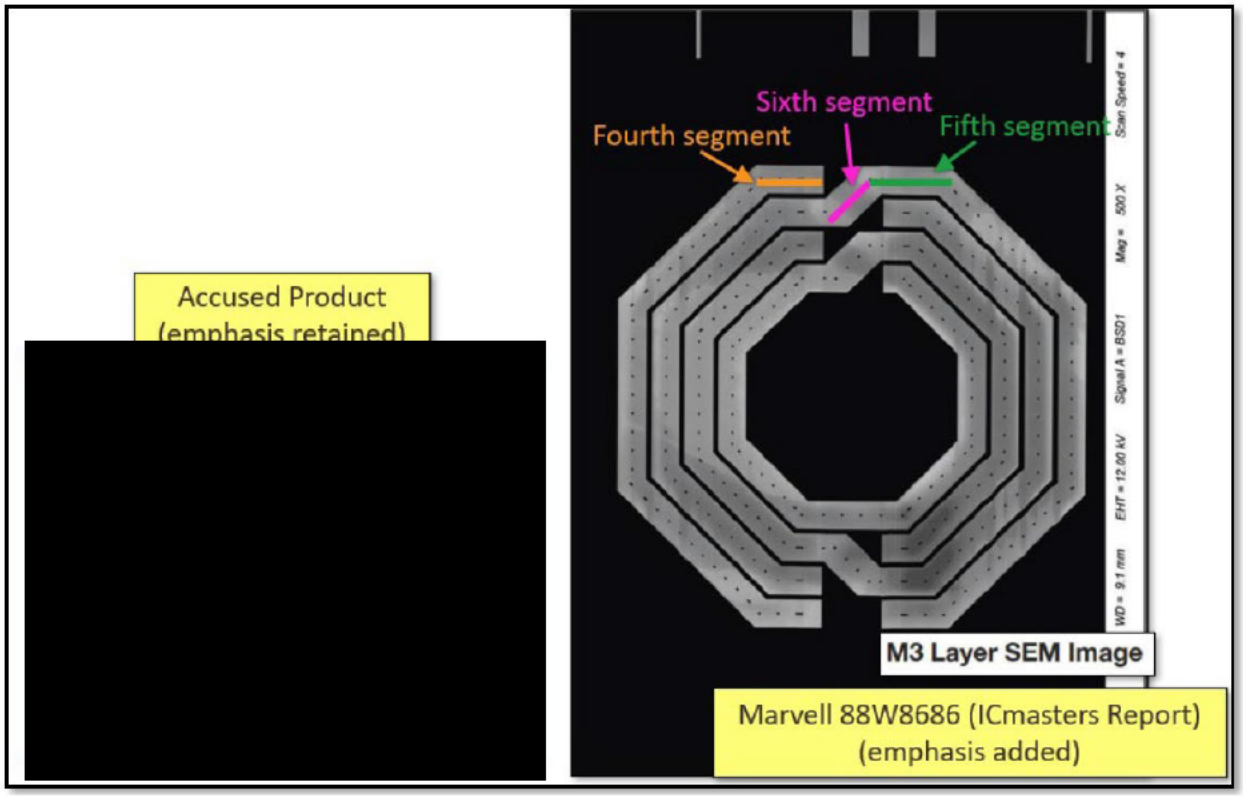

A first metal layer (M4)
M6
M5
M4
M3
M4 Layer SEM Image
Cross Section SEM Image
Marvell 88W8686 (ICmasters Report)
(emphasis added)


Third segment
First segment
Second segment
Accused Product
(emphasis retained)
[redacted]
M4 Layer SEM Image
Marvell 88W8686 (ICmasters Report)
(emphasis added)

RIB at 61-63 (citing RDX-0001.59, 60; Hr'g Tr. (Prucnal) at 809:4-24; JX-0743.8, 9). For the second metal layer (M3) and fourth, fifth, and sixth segments, AMD relies on the following imagery:



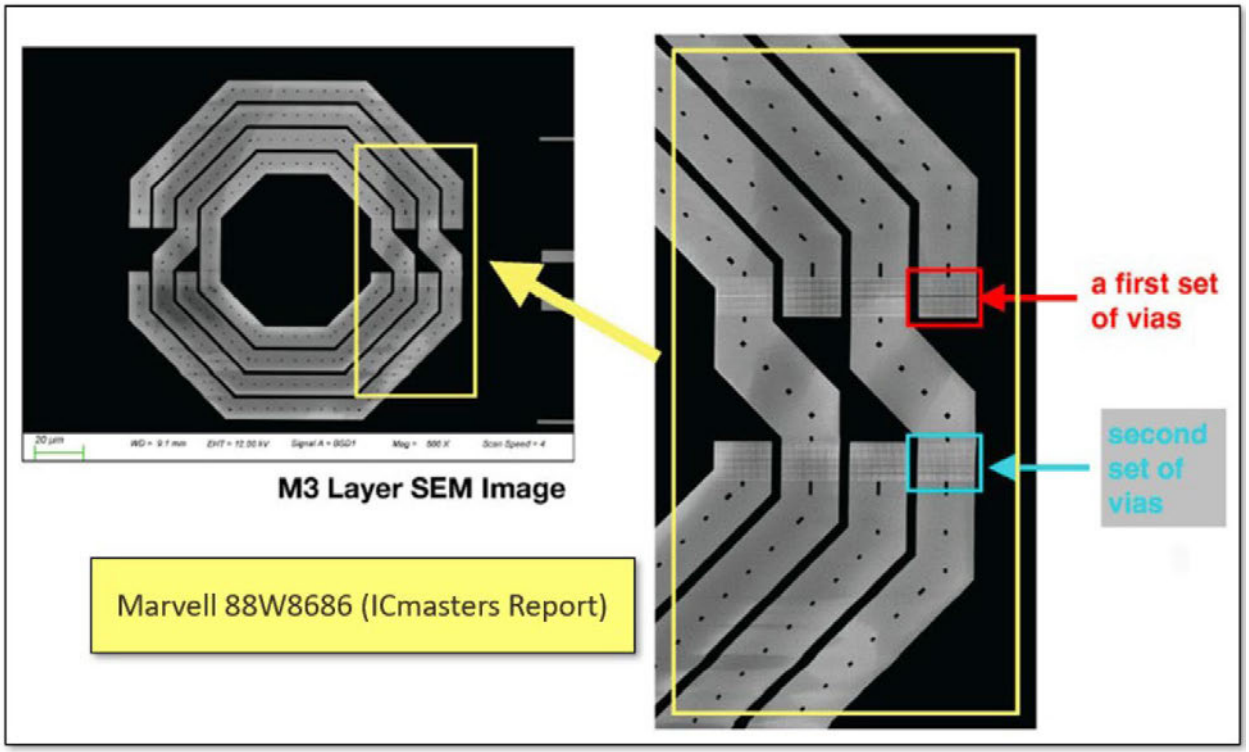
[redacted]

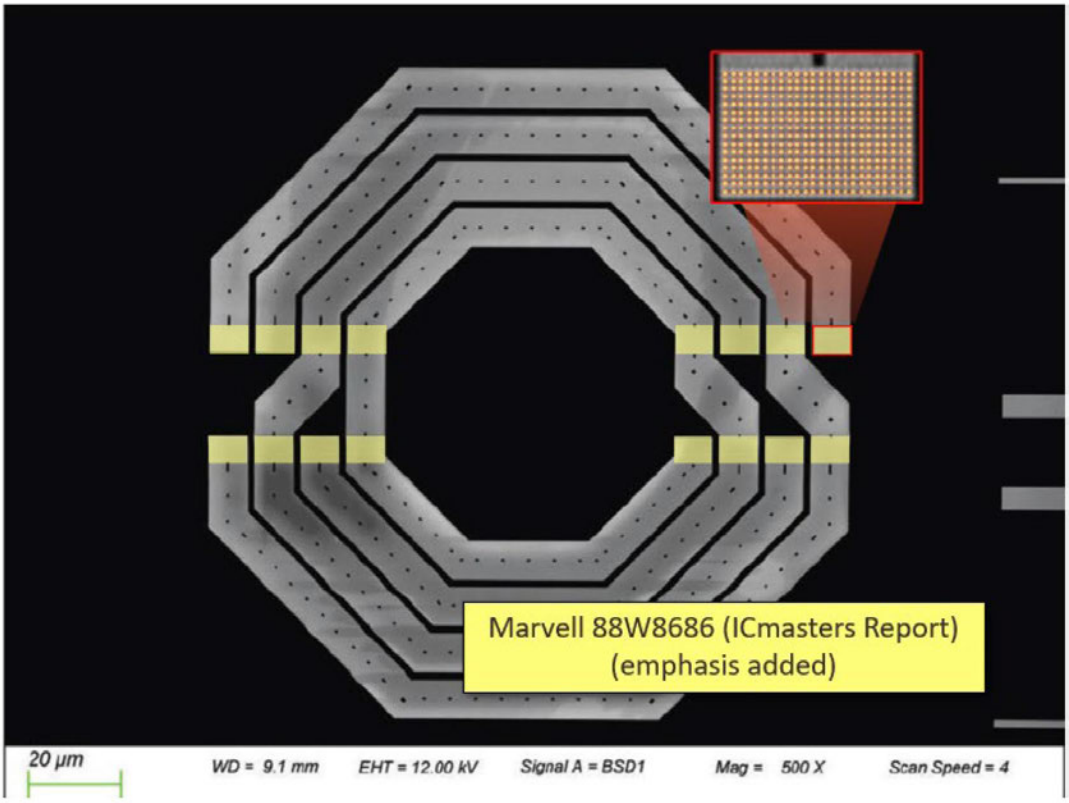


RIB at 63-65 (citing RDX-0001.61, 62; Hr'g Tr. (Prucnal) at 809:25-811:17; JX-0743.10-12).

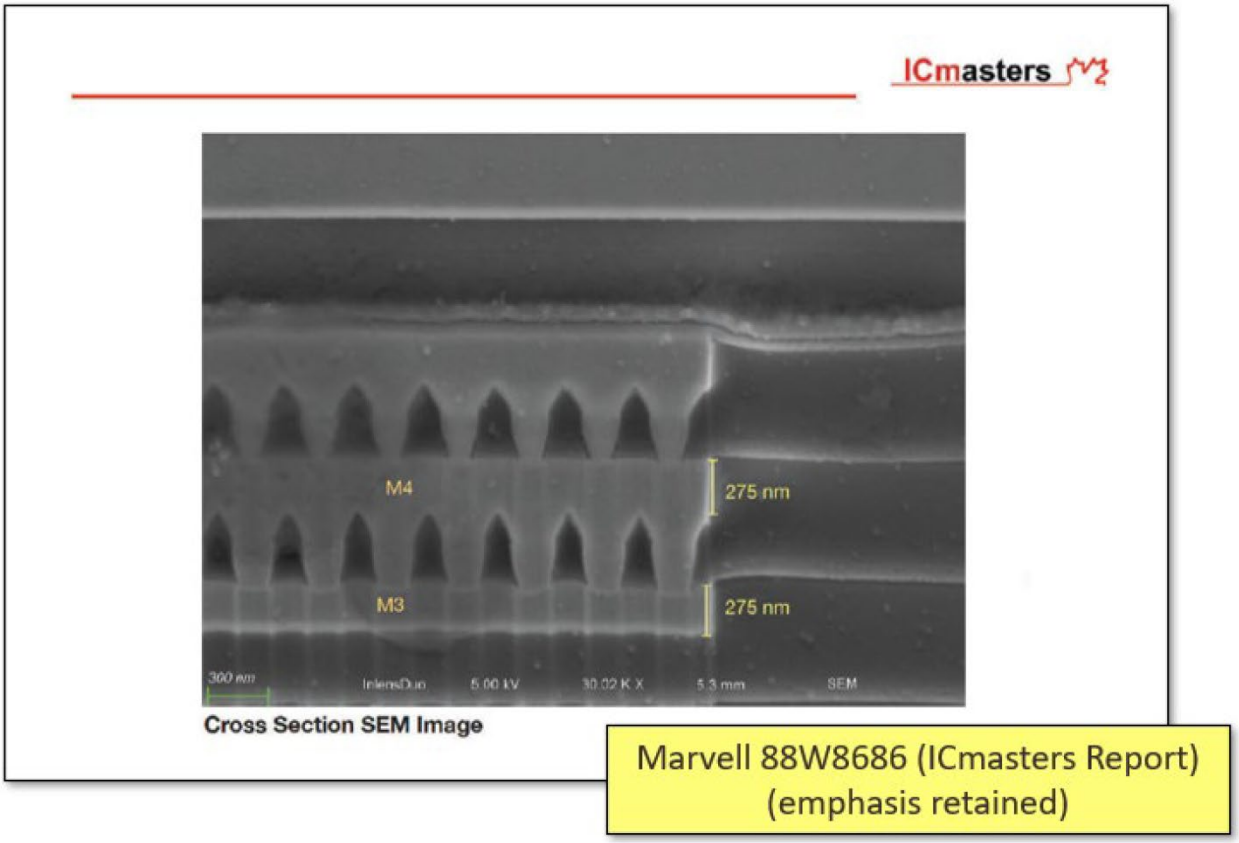
For the limitations concerning first and second sets of vias which connect the first and fourth, and second and fifth segments, respectively, AMD points to the following structures which span the M4 and M3 metal layers:

[redacted]


a first set of vias
second set of vias
M3 Layer SEM Image
Marvell 88W8686 (ICmasters Report)


Marvell 88W8686 (ICmasters Report)
(emphasis added)
20 µm
WD = 9.1 mm
EHT = 12.00 kV
Signal A = BSD1
Mag = 500 X
Scan Speed = 4

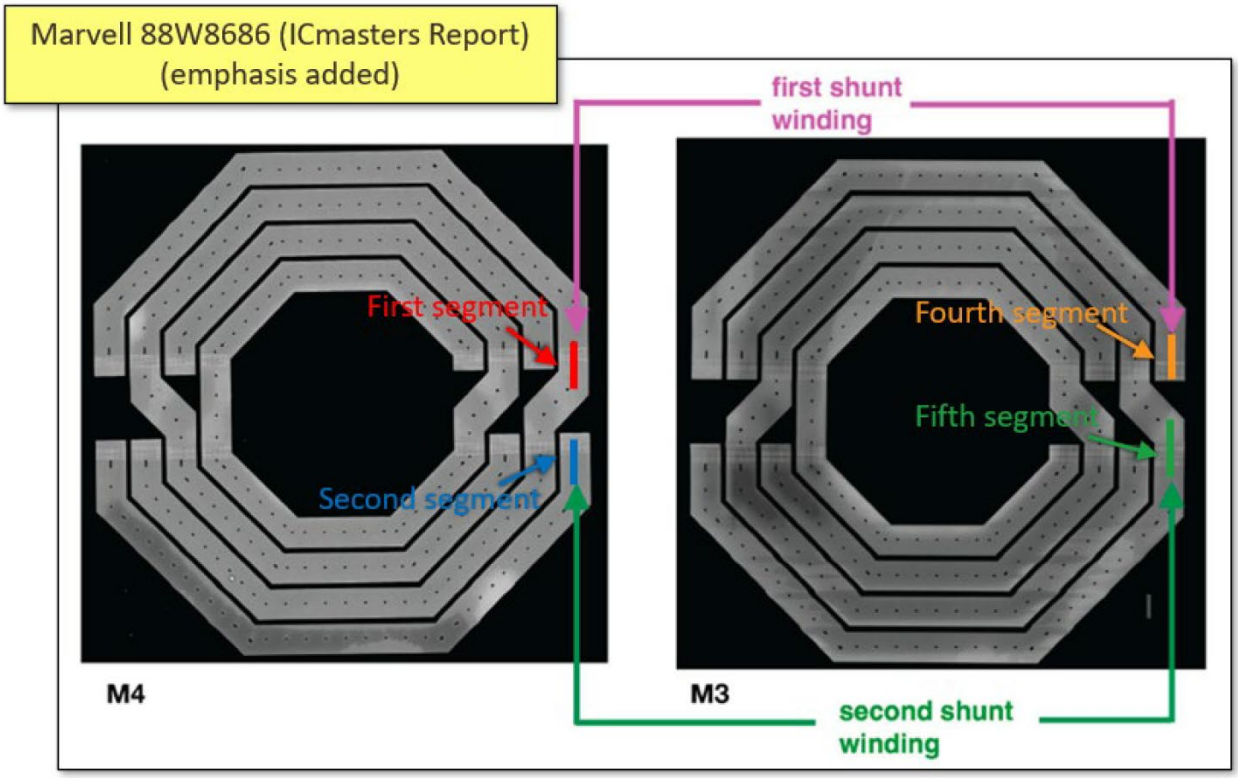
RIB at 66-68 (citing RDX-0001.64, 65; Hr'g Tr. (Prucnal) at 813:3-17, 813:18-814:23; JX-0743.13, 7). Based on these images, AMD continues, "Dr. Prucnal testified there are 16 similar arrays of vias in groupings of 16x24, on M3 of the inductor connecting to M4," and argues the cross-sectional view below, while admittedly taken from an opposite side of the inductor, is representative of all via sets:

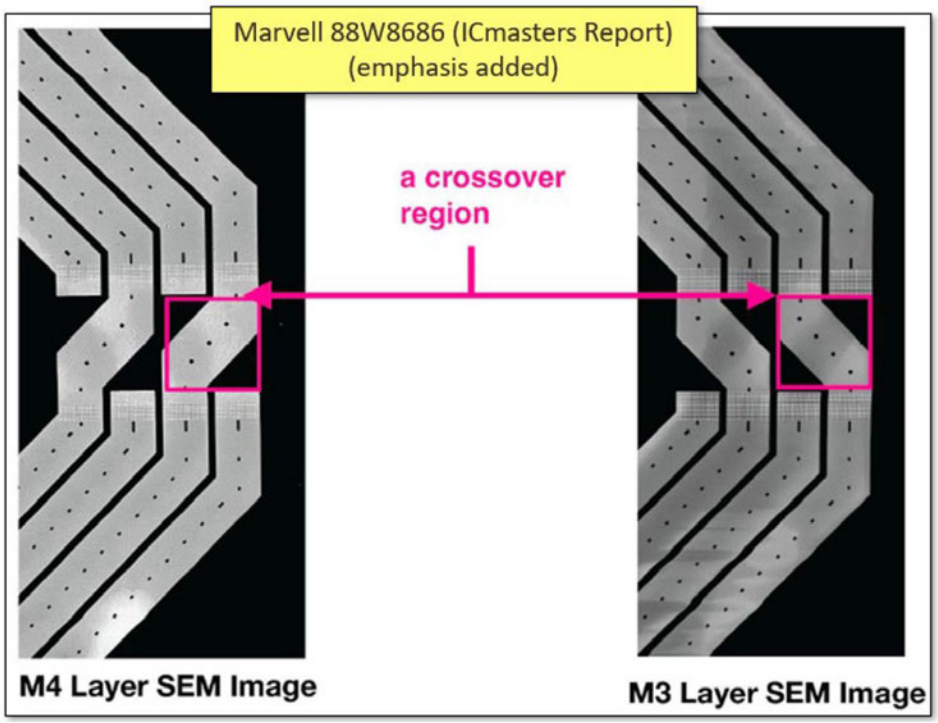


RIB at 65-66 (citing RDX-0001.63; JX-0743.23; Hr'g Tr. (Prucnal) at 811:8-814:17); *see id.* at 69 (citing Hr'g Tr. (Tomkins) at 1160:1162:4). AMD continues, "Dr. Phinney admitted the cross-sectional views showed vias, that they correlate to dots from the top-view as shown in RX-977.1, and that he has seen no evidence to dispute there are *vias on both sides* of M3 connecting to M4." *Id.* at 69 (citing Hr'g Tr. (Phinney) at 1230:2-1232:22) (emphasis in original).

[redacted]

For the shunt winding limitations, and crossover limitation, AMD contends they are again shown in the following figures:





RIB at 70-71 (citing RDX-0001.67, 68; JX-0743.18, 19; Hr'g Tr. (Prucnal) at 814:24-815:13); *see id.* at 72 (citing RDX-0001.69; JX-0743.6). Together, the images show all limitations are met as alleged.

Realtek offers a few points of opposition which are entirely unpersuasive. First, Realtek argues the spiral circuit element in the 88W8686 is a transformer and therefore not "a spiral inductor." CIB at 37 (citing Hr'g Tr. (Phinney) at 1222:24-1223:3); CRB at 14-15. Realtek states, "[t]he evidence is clear that the intended use of Marvell is as a transformer and in order to use it as an inductor, as suggested by Dr. Prucnal, it would need to be modified." *Id.* at 15. In making this argument, Realtek completely avoids discussing that body of evidence and testimony assembled by AMD establishing that transformers consist of two inductors, with the technique being to run a first current through one, creating a magnetic field, thereby inducing a second current in the next inductor, as shown in the following textbook:

10.3 Coupled inductors as transformers

Ideal transformers are an abstraction as all real transformers deviate from ideal behavior in one form or another. As shown in Fig. 10.1b, real transformers are implemented as coupled inductors. As we have learned already, if two inductors are coupled magnetically, then

$$V_1 = j\omega L_1 I_1 + j\omega M I_2 \tag{10.5}$$

$$V_2 = j\omega M I_1 + j\omega L_2 I_2 \tag{10.6}$$

. . . .

[redacted]

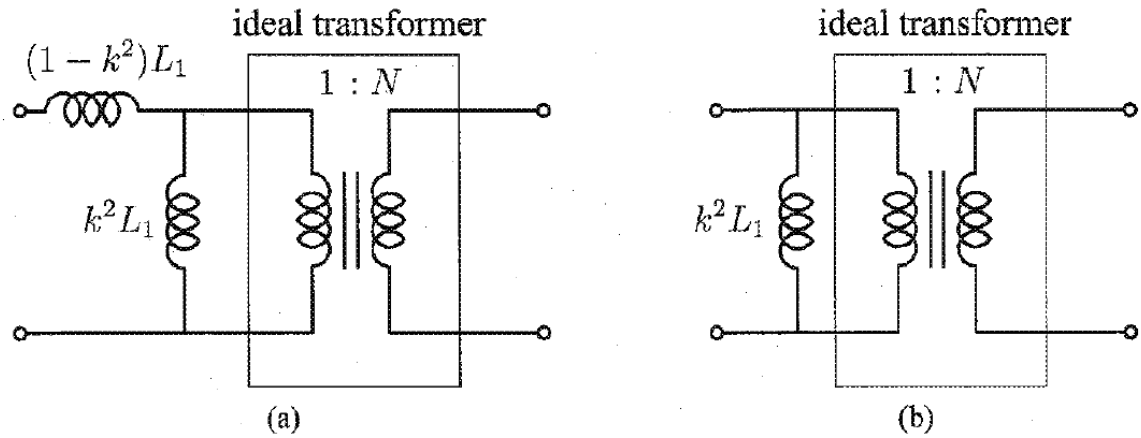


Figure 10.4 (a) Equivalent circuit model for two coupled inductors. (b) Approximation of (a) valid for two tightly coupled inductors ($k \to 1$).

When two inductors are tightly coupled ($k \approx 1$), then it's sometimes useful to view the coupled inductors as a perfect transformer marred by parasitics. In fact, it's not difficult to

RX-0200.99-101; *see* JX-0080 at 1:9-16 ("On-chip transformers are relatively rare in silicon RF integrated circuits and make use of a few well-known layout techniques, *e.g.*, placing the primary and secondary windings one above the other in different interconnect layers. . . . Transformers employing such symmetrical inductors are shown in [references]."); RIB at 56-59 (citations omitted). On cross-examination, Dr. Phinney eventually admitted this basic engineering principle:

> Q. And do you agree that you can put that inductor together with another inductor and create a transformer?
>
> A. You could do that.
>
> Q. And so then do you agree that a transformer can be two inductors?
>
> A. You could build it that way if you wanted.
>
> Q. Well, I'm not asking if you can build it that way. I'm saying do you agree a transformer can be two inductors?
>
> A. Yeah, you could stack, just, one right on top of the other and call one winding and the other a second winding.

. . . .

> Q. Okay. But you agree you can put Figure 2.10 together with another exact same inductor that looks like Figure 2.10 and create a transformer?
>
> A. Yeah, I think you asked me about that, about like putting just one inductor structure and then another one above it, and could you use that as a transformer. Is that what you're asking?
>
> Q. And that's a yes?
>
> A. Yeah, you could put one on top of the other and call one a primary winding and the other a secondary.

Hr'g Tr. (Phinney) at 1237:25-1239:18. Thus, there can be no real dispute that the Marvell 88W8686 discloses the preamble of claim 1, "a structure of a spiral inductor."

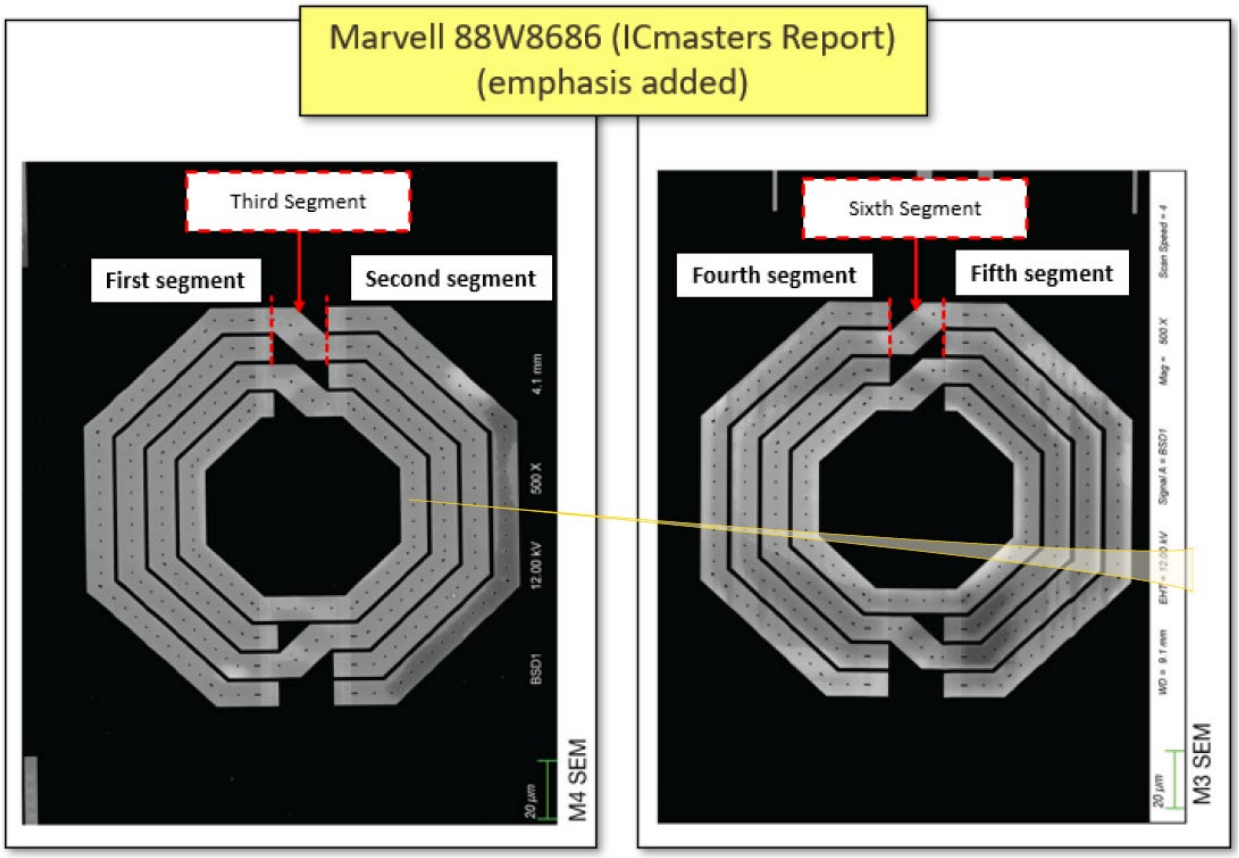
Realtek then complains, much as it did for the Qualcomm RFR6122, that the cross-sectional images used by AMD fail to show certain limitations such as "a crossover region ([1K]), or the third and sixth segments [or] first and fifth segments." CIB at 38-39; CRB at 15-16. But the other images provided by AMD, reproduced above, clearly show all limitations. The cross-sections are merely cumulative evidence of the sets of vias, which are indisputably present on both sides of the inductor spiral as alleged.

Accordingly, claim 1 is invalid as anticipated over the Marvell 88W8686.

b. Claim 2

As for claim 2, AMD contends the identified third segment is between the first and second, and the sixth is between the fourth and fifth:

[redacted]



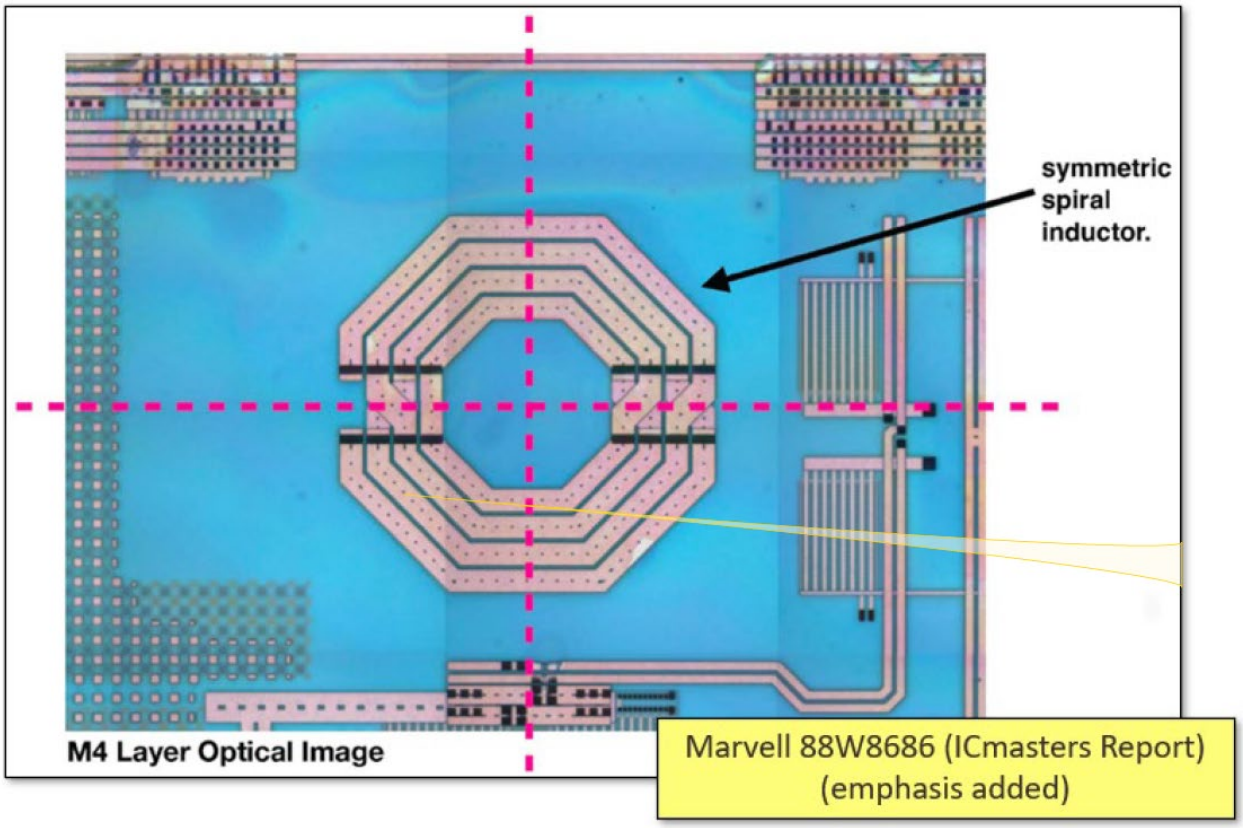
RIB at 73 (citing RDX-0001.70; JX-0743.21; Hr'g Tr. (Prucnal) at 816:6-24). Realtek does not dispute claim 2 (*see* CIB at 39; CRB at 14-16) beyond the elements of claim 1, and claim 2 is met as alleged.

Accordingly, claim 2 is invalid as anticipated over the Marvell 88W8686.

c. Claim 8

As for claim 8, AMD contends the inductor is symmetrical as follows:

[redacted]



RIB at 74 (citing RDX-0001.71; JX-0743.25; Hr'g Tr. (Prucnal) at 816:25-817:7). Realtek does not dispute claim 8 (*see* CIB at 39; CRB at 14-16) separately from the other claims, and it is met as alleged.

Accordingly, claim 8 is invalid as anticipated over the Marvell 88W8686.

3. Christensen

Christensen is U.S. Patent No. 6,794,977, which issued in September 2004. It teaches "a planar transformer" where "a portion of each of the windings are intermingled in an intermingled portion." JX-0080 at Abstract. More particularly, Christensen describes "each full turn of each winding in said intermingled portion is effected by one self-crossing and two crossings of each other winding having turns in said intermingled portion" with the turns of the windings created by "conductive paths" and "the paths forming each winding being untied by vias." *Id.* at 1:38-42. Christensen's figures 1 and 4 show an embodiment of this invention, below:

[redacted]

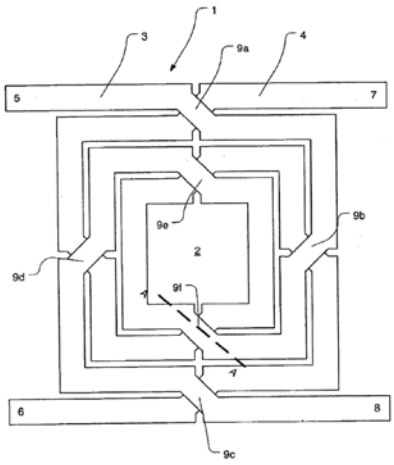


Figure 1

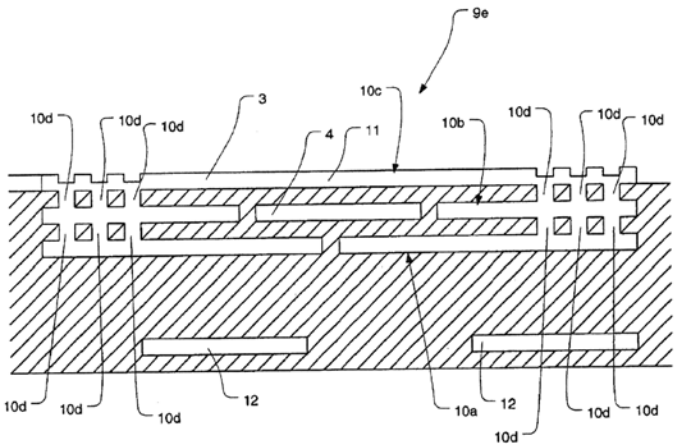


Figure 4

JX-0080 at Figs. 1, 4. AMD contends the asserted claims are invalid as anticipated by Christensen. For the reasons discussed below, AMD has shown claims 1, 2, and 8 to be invalid.

a. Claim 1

Claim 1 is presented above. As for the preamble, "a spiral inductor," AMD refers to the following figures:

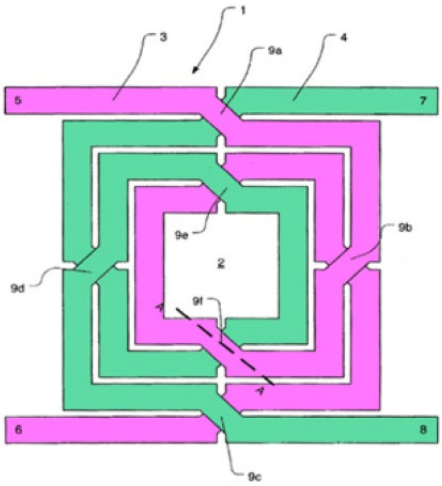


Figure 1

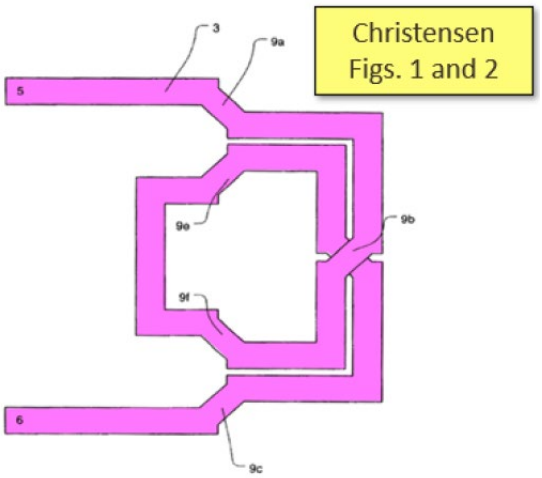


Figure 2

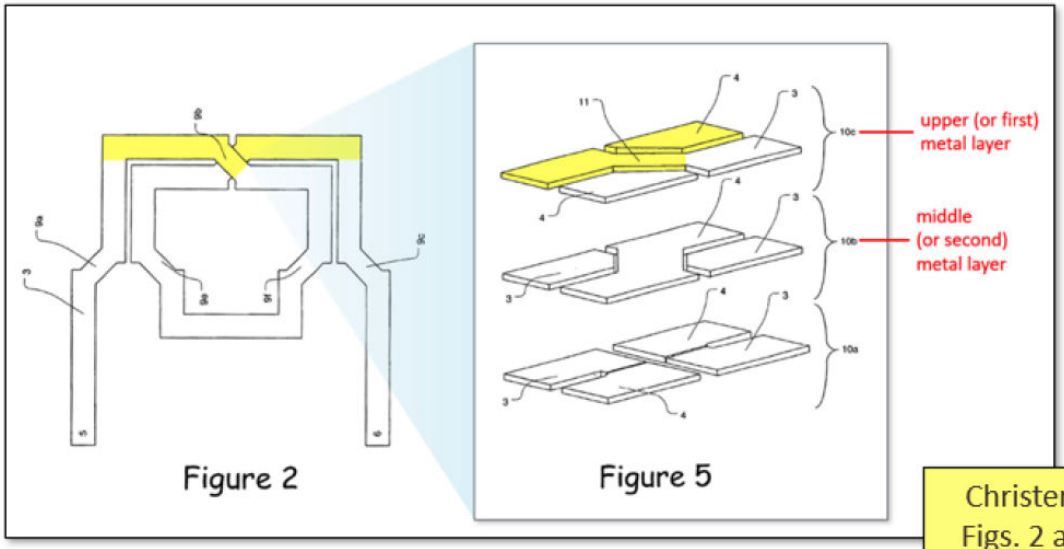
FIG. **1** is a plan view of a 1:1 ratio transformer according to the present invention;

FIG. **2** is a plan view showing the primary winding only of the transformer of FIG. **1**;

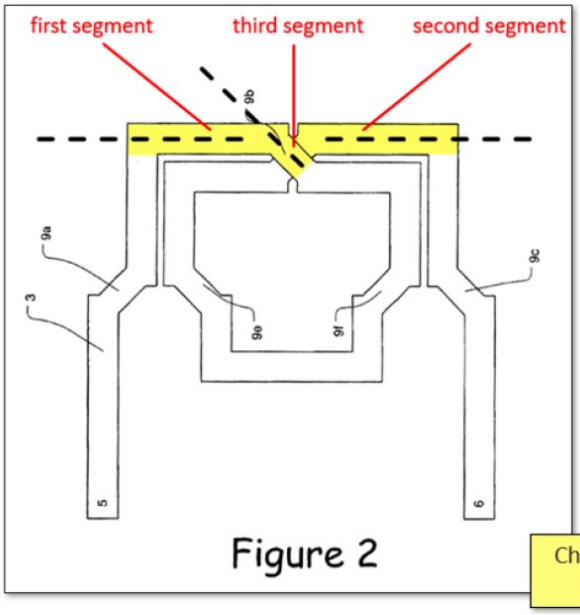
[redacted]

RIB at 87-88 (citing RDX-0001.91; JX-0080 at Figs. 1, 2; Hr'g Tr. (Prucnal) at 840:8-841:16). For the first metal layer and first, second, and third segments, AMD provides the following identification within Christensen:

Referring to FIGS. **1**, **2**, **3** and **4**, an on-chip planar transformer **1** is formed in metal interconnect layers of a silicon integrated circuit **2**. The transformer **1** comprises a



Christensen Figs. 2 and 5



Christensen Fig. 2

[redacted]

RIB at 89-90 (citing RDX-0001.92, 93; JX-0080 at Figs. 2, 5; Hr'g Tr. (Prucnal) at 841:17-842:20). For the second metal layer and corresponding fourth, fifth, and sixth segments, AMD points to the following:

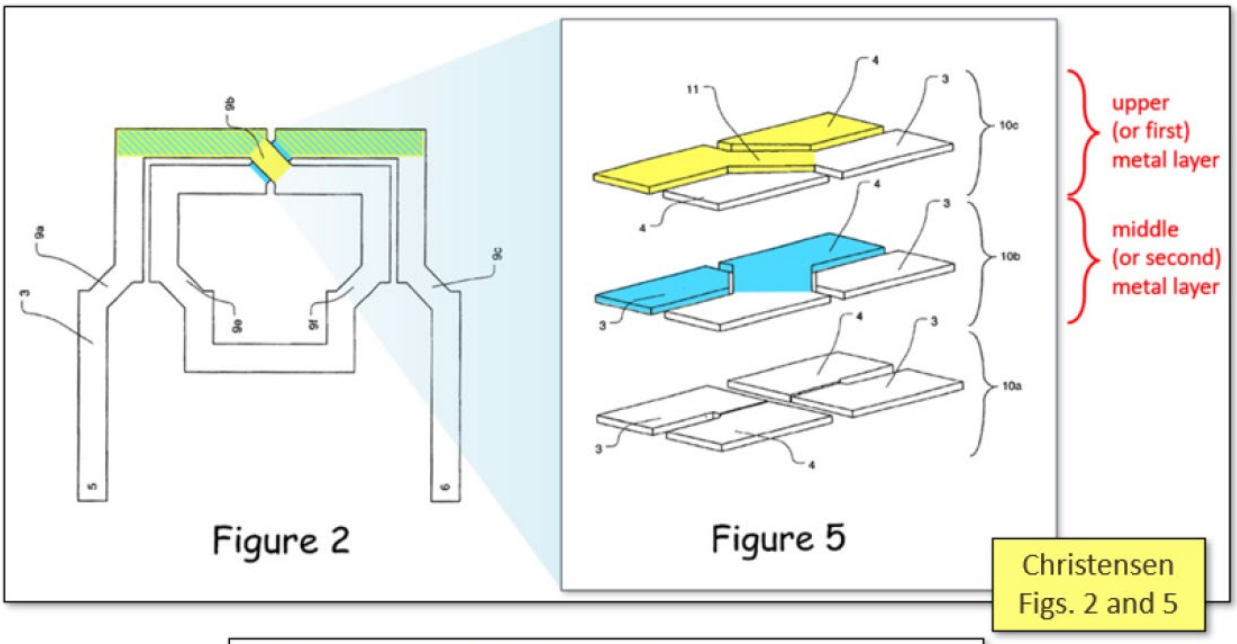
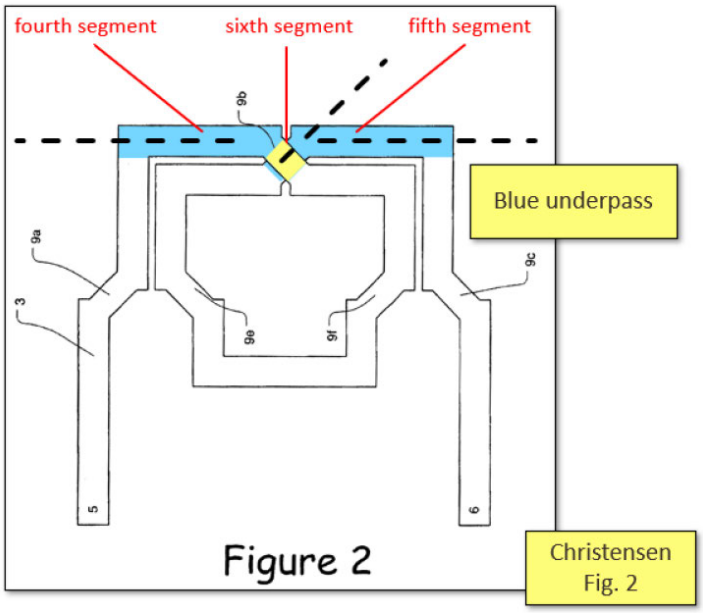
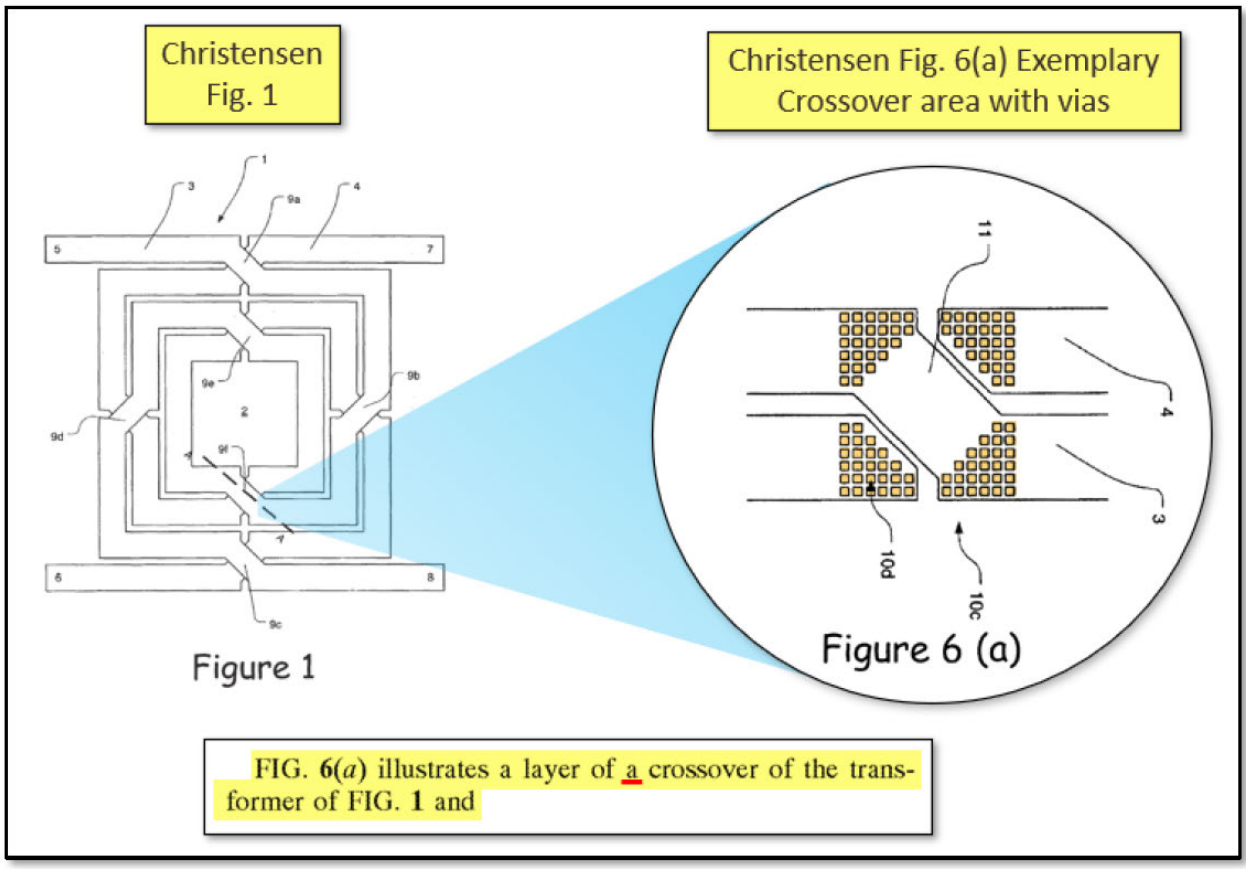


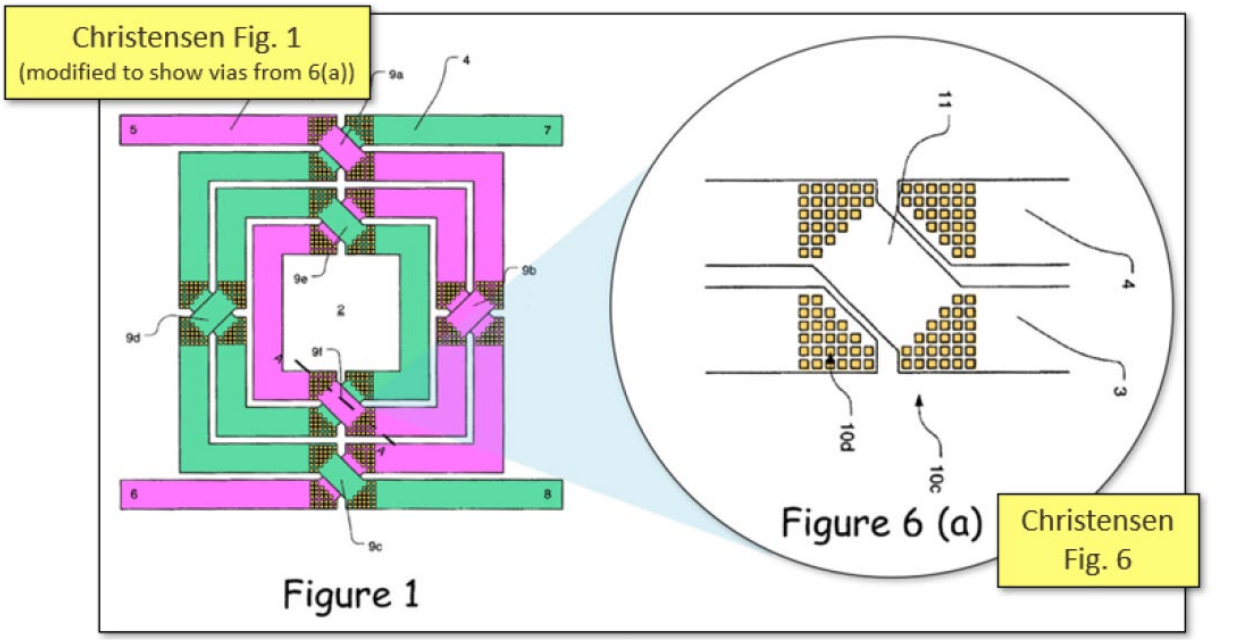
FIG. **5** is an exploded view of a cross-over of the transformer of FIG. **1**;



RIB at 90-92 (citing RDX-0001.94, 95; JX-0080 at Figs. 2, 5; Hr'g Tr. (Prucnal) at 842:21-844:18). For the limitations concerning first and second sets of vias which connect the first and fourth, and second and fifth segments, respectively, AMD points to the following structures and states "Christensen specifically notes that the vias are adjacent to the '*crossovers*,' plural":



[redacted]

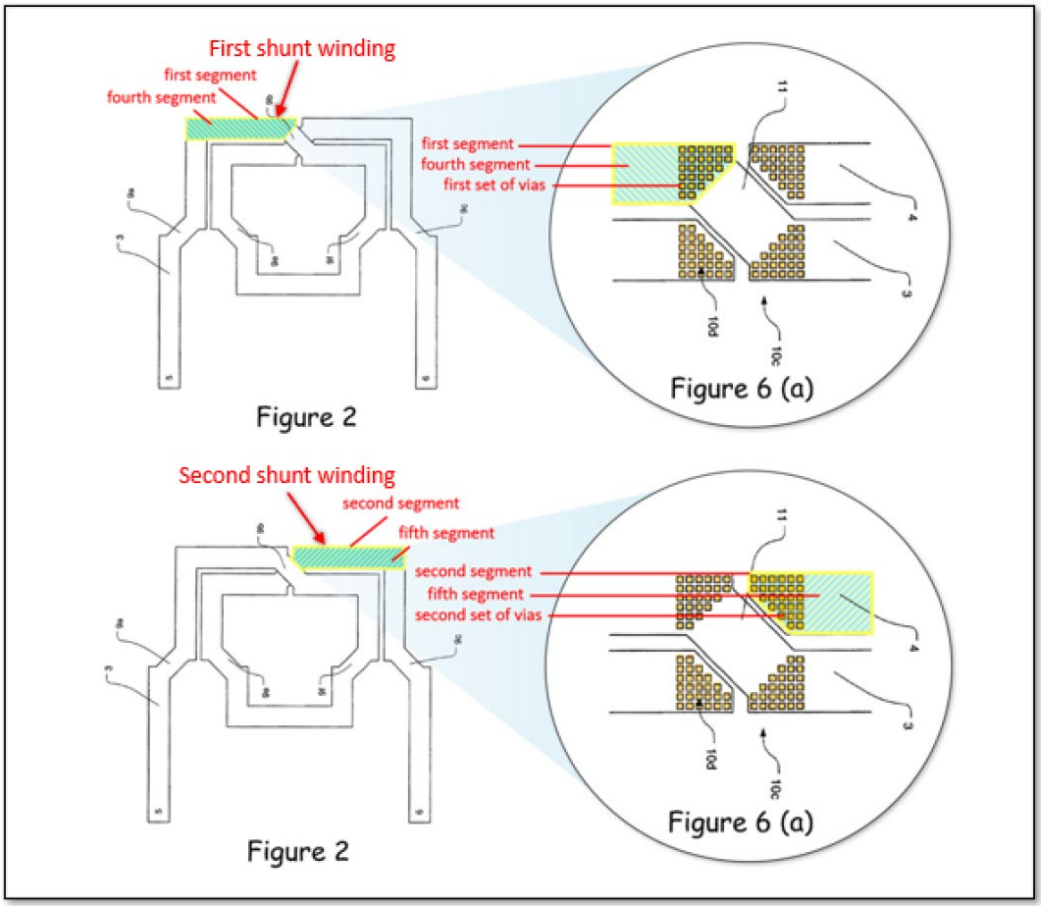


Preferably, uniting vias are located adjacent to said crossings.

crossovers and, optionally at other locations. Similarly, the conductors of the conductor layers **10***a*, **10***b*, **10***c* forming the secondary winding **4** are bonded by arrays of vias **10***d* (see FIG. **4**) adjacent to the crossovers and, optionally at other locations.

RIB at 92-94 (citing RDX-0001.96, 97; JX-0080 at 2:30-31, 3:43-54, Figs. 1, 6; Hr'g Tr. (Prucnal) at 844:19-845:20) (emphasis in original). And for the shunt winding limitations, and crossover limitation, AMD contends they are again shown in the following figures:

[redacted]



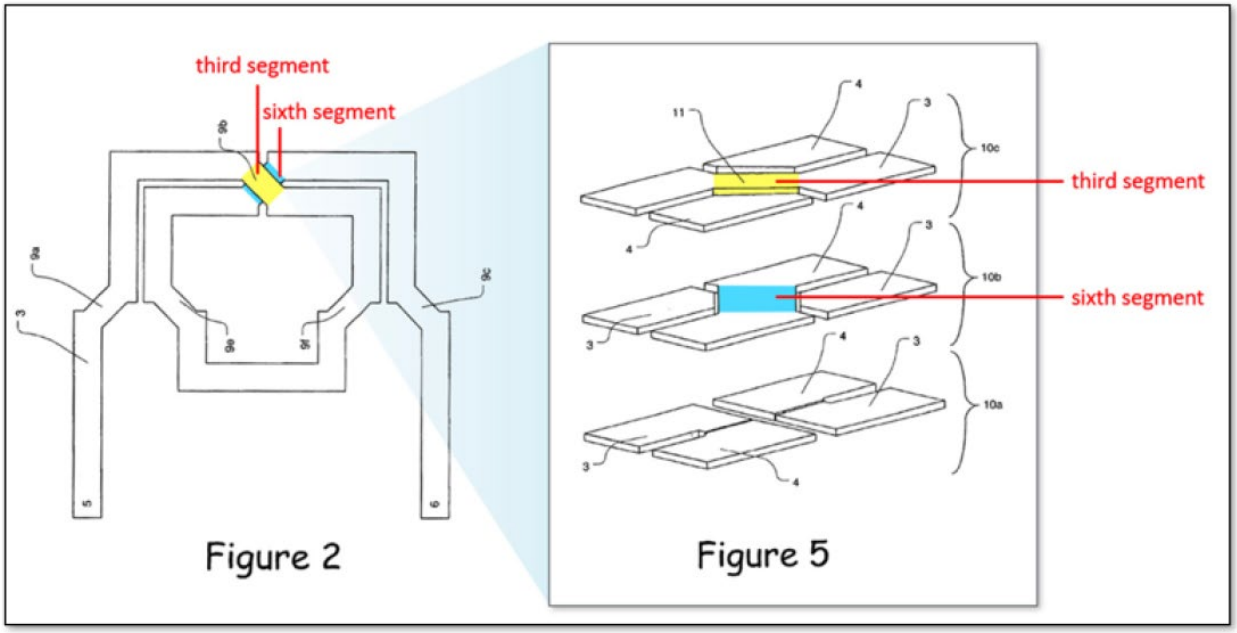


FIG. **5** is an exploded view of a cross-over of the transformer of FIG. **1**;

RIB at 94-96 (citing RDX-0001.98, 99; JX-0080 at Figs. 2:27-28, 3:43-54, 2, 5, 6; Hr'g Tr. (Prucnal) at 845:21-847:3). The limitations are met as alleged.

Realtek challenges Christensen's use of spiral inductors within a transformer as failing to meet the preamble, "a structure of a spiral inductor." CIB at 29-30 ("Christensen does not teach a structure of a spiral inductor. Rather, Christensen is directed to planar transformers with intermingled windings."). *See* CRB at 5-6. For the reasons explained above with respect to the Marvell 88W8686 chip, this is not persuasive. A transformer contains two inductors so as to enable one to induce current in the other. And while Realtek and Dr. Phinney are careful to describe the two paths in Christensen as "windings" and not "inductors," Christensen's disclosure shows the otherwise well-understood identity of these structures:

> On-chip transformers are relatively rare in silicon RF integrated circuits and make use of a few well-known layout techniques, *e.g.* placing the primary and secondary windings one above the other in different interconnect layers. While some of these techniques ensure symmetry in the sense that the primary and secondary parts are identical. Generally, however, the two inductors are not balanced.
>
> A more symmetrical layout comprises inward and outward spiralling paths which cross twice in all but the outer and inner turns which contain only one crossing. Transformers employing such symmetrical inductors are shown in Simburger, W. et al., "A Monolithic 3.7W Silicon Power Amplifier with 59% PAE at 0.9 GHz", 1999 IEEE International Solid-State Circuits Conference, TP 13.6. These transformers comprise the turns of each inductor arranged in one or more blocks, which are arranged coaxially.

JX-0080 at 1:9-25.

Realtek further contends, "Christensen is entirely silent on [1I], [1J], and [1K]," which are the vias, shunt winding, and final crossover limitations. CIB at 30 (citing Hr'g Tr. (Phinney) at 1212:13-1215:4); CRB at 6. This position is untenable given Christensen's figures showing a plurality of vias along the pertinent segments (JX-0080 at Figs. 6a-6c) and accompanying description:

[redacted]

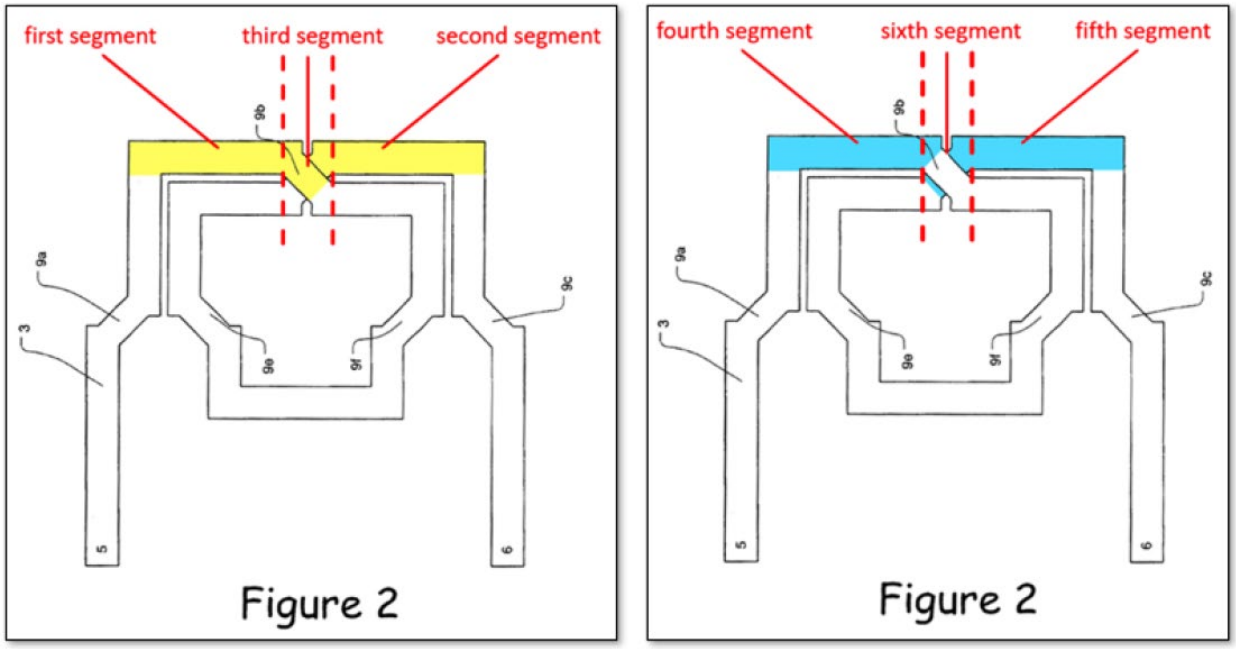
> The conductors of the conductor layers 10 a, 10 b, 10 c forming the primary winding 3 are bonded by arrays of vias 10 d (*see* FIG. 4) adjacent to the crossovers and, optionally at other locations. Similarly, the conductors of the conductor layers 10 a, 10 b, 10 c forming the secondary winding 4 are bonded by arrays of vias 10 d (*see* FIG. 4) adjacent to the crossovers and, optionally at other locations.

JX-0080 at 3:47-55. Indeed, when Christensen later teaches, "[i]t is important to minimise the resistance of the bridge 11 because, at the crossovers, the currents of the primary and secondary windings 3, 4 are carried in respective single conductor layers 10 c, 10 b" (JX-0080 at 4:4-8), it is implied that prior to the crossover, the currents of the primary and secondary windings are carried in more than one conductor layer (*i.e.*, a parallel, shunt, winding).

Accordingly, claim 1 is invalid as anticipated by Christensen.

b. Claim 2

As for claim 2, AMD contends the identified third segment is between the first and second, and the sixth is between the fourth and fifth:



Christensen Fig. 2

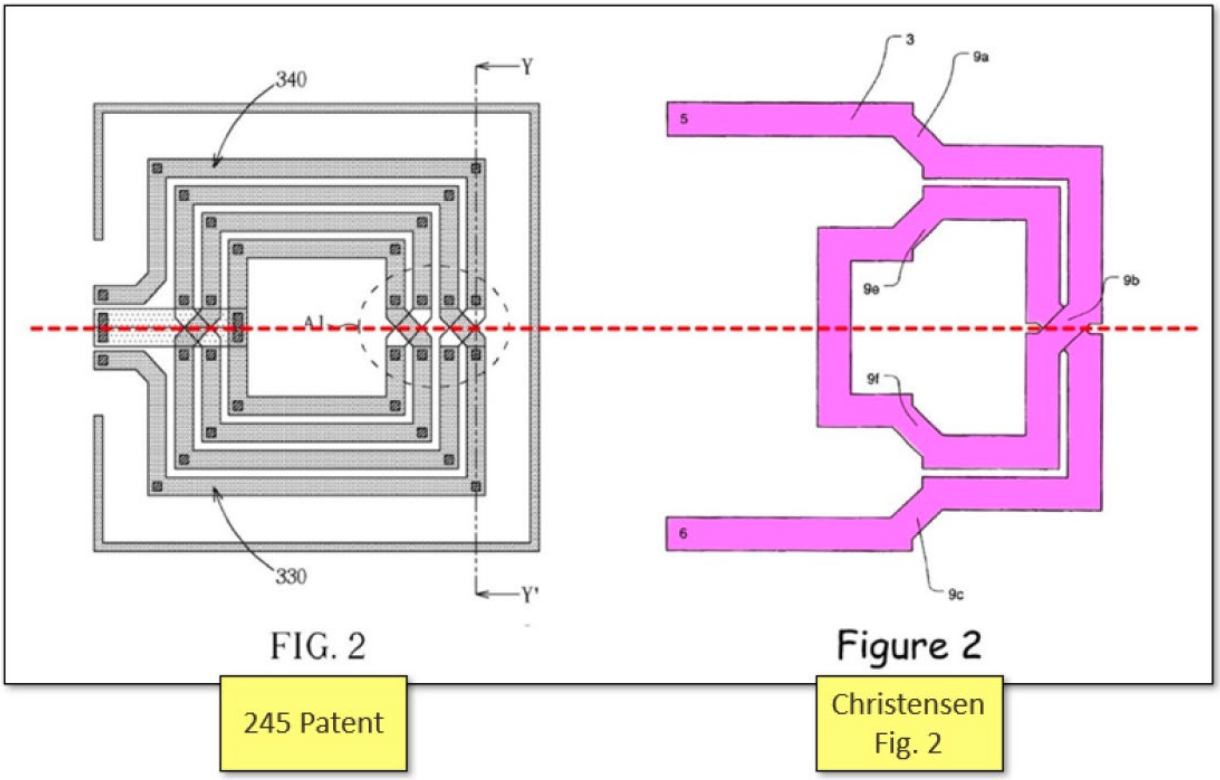
[redacted]

RIB at 96-97 (citing RDX-0001.100; JX-0080 at Fig. 2; Hr'g Tr. (Prucnal) at 847:4-16). Realtek does not dispute claim 2 (*see* CIB at 29-30; CRB at 5-6) separately from claim 1, and it is met as alleged.

Accordingly, claim 2 is invalid as anticipated by Christensen.

c. Claim 8

As for claim 8, AMD contends the inductor is symmetrical as follows:



RIB at 97-98 (citing RDX-0001.101; JX-0080 at Fig. 2; Hr'g Tr. (Prucnal) at 847:17-848:4). Realtek does not dispute claim 8 (*see* CIB at 29-30; CRB at 5-6) beyond the other claims, and it is met as alleged.

Accordingly, claim 8 is invalid as anticipated by Christensen.

[redacted]

4. Indefiniteness

AMD alleges the 245 patent claims are indefinite under 35 U.S.C. § 112, ¶ 2. RIB at 112. AMD describes the problem, generally, as: "The 'first segment' element is found throughout the claims, but the claim limitations are at odds with each other because it is described 'as needing to be a winding,' while also being in a different layout direction from other segments"; and provides the following diagram:

[redacted]

Dr. Phinney Hearing Day 1 Testimony CDX-0002C.0022	Dr. Phinney Alternative Interpretation from Reports. RX-1285C.180

Id. (citing Hr'g Tr. (Prucnal) at 857:3-10; RDX-0001C.121). AMD reasons that the "first segment" on the left "does not construct a 'shunt winding' with the other claim limitations" while the one on the right "is at odds with the claim limitation requiring the third segment to have a 'layout direction . . . different from' that of the first and second segments." *Id.* at 113 (citing Hr'g Tr. (Prucnal) at 858:2-859:17). AMD concludes, "[t]hus, a POSITA would be uncertain what is or is not the first segment." *Id.*; RRB at 41 ("Moreover, the patent fails to assign boundaries to these terms, leaving a POSITA to guess as to their scope.").

AMD has not met its clear and convincing burden. The claim term "segment" is certainly broad, but broad does not equal indefinite. To the contrary, Realtek is persuasive that a "segment" is simply "a piece of something," or, in the context of the 245 patent, "a line or a portion of the winding." CIB at 48 (citing Hr'g Tr. (Phinney) at 121:16-18). And as to how a "segment"—as a single portion of a wire—can meet the limitation "wherein the first segment, the fourth segment and the first set of vias construct a first shunt winding," this has been demonstrated in the contexts of the 245 patent, Accused Products, and DI Products, above, thereby negating AMD's "at odds" indefiniteness theory. Dr. Phinney's difficulty in counting the number of possible shunt windings in an Accused Device (RIB at 114-115 (citing Hr'g Tr. (Phinney) at 121:11-124:8)) is beside the point.

Accordingly, AMD has not shown that a person of ordinary skill would fail to understand or recognize "first segment" within the overall apparatus of claim 1.

V. U.S. PATENT NO. 8,006,218

A. Level of Ordinary Skill in the Art

In Order No. 21, I determined that a person having ordinary skill in the art of the 218 patent at the time of invention:

> [W]ould be someone with a bachelor of science degree in [electrical engineering, computer engineering], or a related field, and approximately two years of experience in the design and development of power distribution networks related to integrated circuits, or the equivalent, with additional education and/or research substituting for experience and vice versa.
>
> . . . .
>
> [E]xperience may substitute for education and vice versa; thus, graduate studies in electrical engineering or a related field may substitute for work experience and, likewise, additional work experience may substitute for relevant formal education.

Order No. 14 at 8. The parties do not challenge this definition (*see generally* CIB; CRB; RIB; RRB), and it is applied throughout this initial determination.

B. Claims-at-Issue

Claims 12, 13, and 15-18 of the 218 patent are at issue in this investigation, either through allegations of infringement or domestic industry technical prong. *See* CIB at 67, 218. They are reproduced below, along with limitation identifiers:

> 12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:
>
> [12a] a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;
>
> [12b] a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and
>
> [12c] a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;
>
> [12d] wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;
>
> [12e] wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and
>
> [12f] wherein the first metal layer and the second metal layer are different layers.
>
> 13. The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh.
>
> . . . .
>
> 15. The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain.
>
> 16. The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the

ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain.

17. The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain.

18. The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh.

218 patent at cls. 12 (annotated), 13, 15-18.

C. Claim Construction

As part of the *Markman* process, the following claim terms of the 218 patent were construed, either as-agreed between the parties or determined by Order No. 21:

Claim Term	Construction
"power mesh"	N/A; construction deferred
"global power mesh"	Power mesh capable of distributing power to multiple power domains

See Order No. 21 at 19, 25. Within their briefing, the parties identify a number of additional claim construction disputes.

1. "power mesh"

"Power mesh" appears in all asserted claims of the 218 patent. Realtek identifies three disputes related to the term—whether it: "(1) must include intersections, (2) must have an overlapping intersection with each and every wire of the power mesh (sometimes requiring power wire intersections), and (3) cannot have overlapping intersections with wires from another mesh without become 'one' mesh." CIB at 53. Realtek rejects all three of these features as "contrary to the intrinsic record and would read out the preferred embodiments, including power mesh 310 of Figure 3" and emphasizes "[a]ll disputes related to this term are resolved if the Court finds that the

term ‘power mesh’ does *not* require intersections.” *Id.* at 54 (emphasis in original); *see generally id.* at 54-58; CRB at 29-33. AMD views the choice as between two constructions: “two sets of parallel conductive metal wires that form a net or web-like structure” (AMD) or “ordinary and customary meaning: a network of wiring capable of distributing power” (Realtek); and argues “Realtek’s construction rests on Dr. Souri’s misunderstanding of Figure 3.” RIB at 128-129 (citing, *inter alia*, Order No. 21 at 17); *see generally id.* at 115-130; RRB at 49-51.

The parties’ disputes are resolved as follows. First, a structure identified as a “mesh” under the 218 patent must contain intersection(s) of wires. As noted in Order No. 21, the ordinary meaning of a “mesh” is a plurality of linear members extending in different directions creating intersections. Order No. 21 at 17. No party presented documentary evidence to the contrary at the hearing. And Realtek’s position is indeed based on a misreading of Figure 3.

More specifically, Realtek declares, “[p]artial local power mesh 310 depicted in Figure 3 shows beyond all doubt that [a] power mesh is a plurality of wires and that a power mesh does not require intersections” and “the intrinsic evidence—power mesh 310 in Figure 3—resolves all ambiguities and resort to extrinsic evidence is improper.” CIB at 54, 56. Realtek leans on the fact that Figure 3 annotates only a single power wire 311 and a single ground wire 312 as belonging to the first partial local mesh 310, and that these wires run in parallel, as shown below:

[redacted]

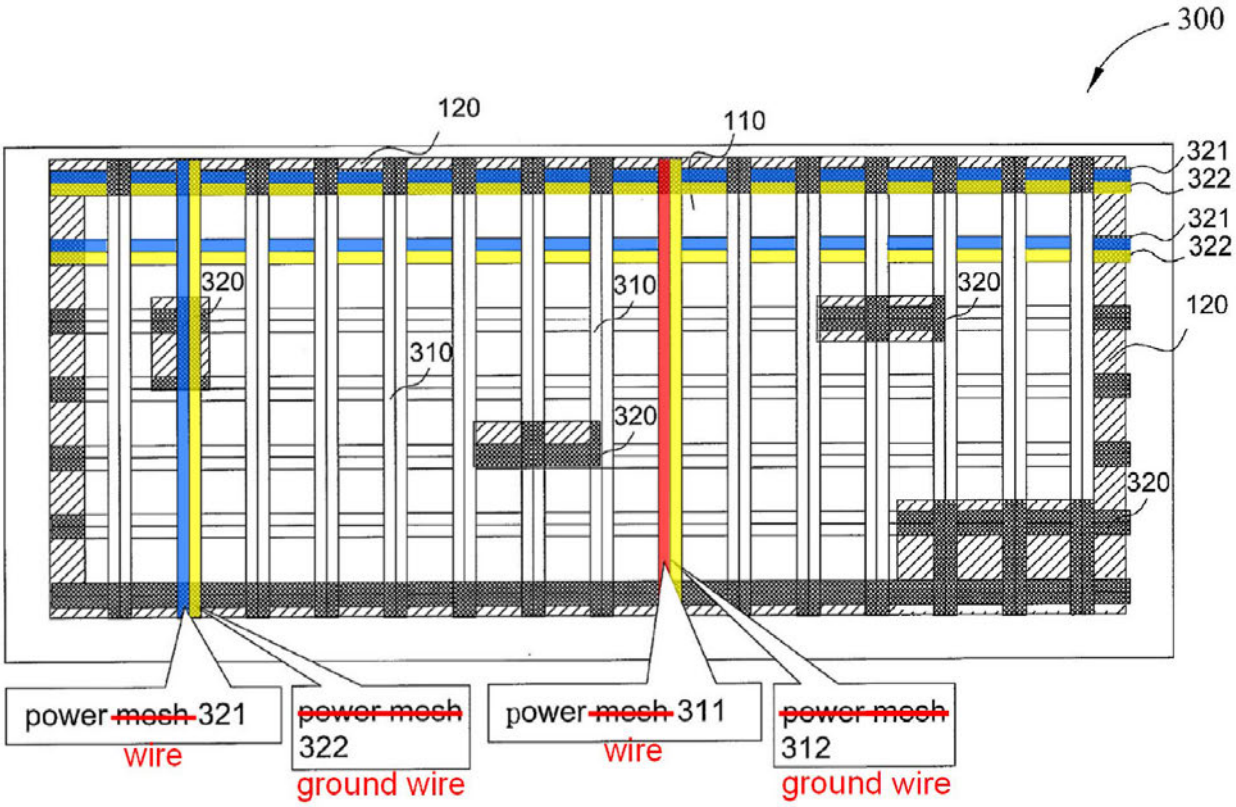


FIG. 3

See CIB at 49 (citing CDX-0003C.[3]1). And because they run in parallel and thus do not create an intersection, Realtek concludes the definition of "mesh" cannot require intersections. *Id.* at 55 ("AMD's construction[,] however, exclude[s] a preferred embodiment of partial local power mesh 310 in Figure 3, as discussed above. Such a construction cannot be correct."). In this way, Realtek effectively contends that partial local power mesh 310 is limited to those two wires.

This conflicts with the overall weight of the intrinsic evidence and is not accepted. First, the vast majority of wires shown in Figure 3 are not annotated in any way:

[redacted]

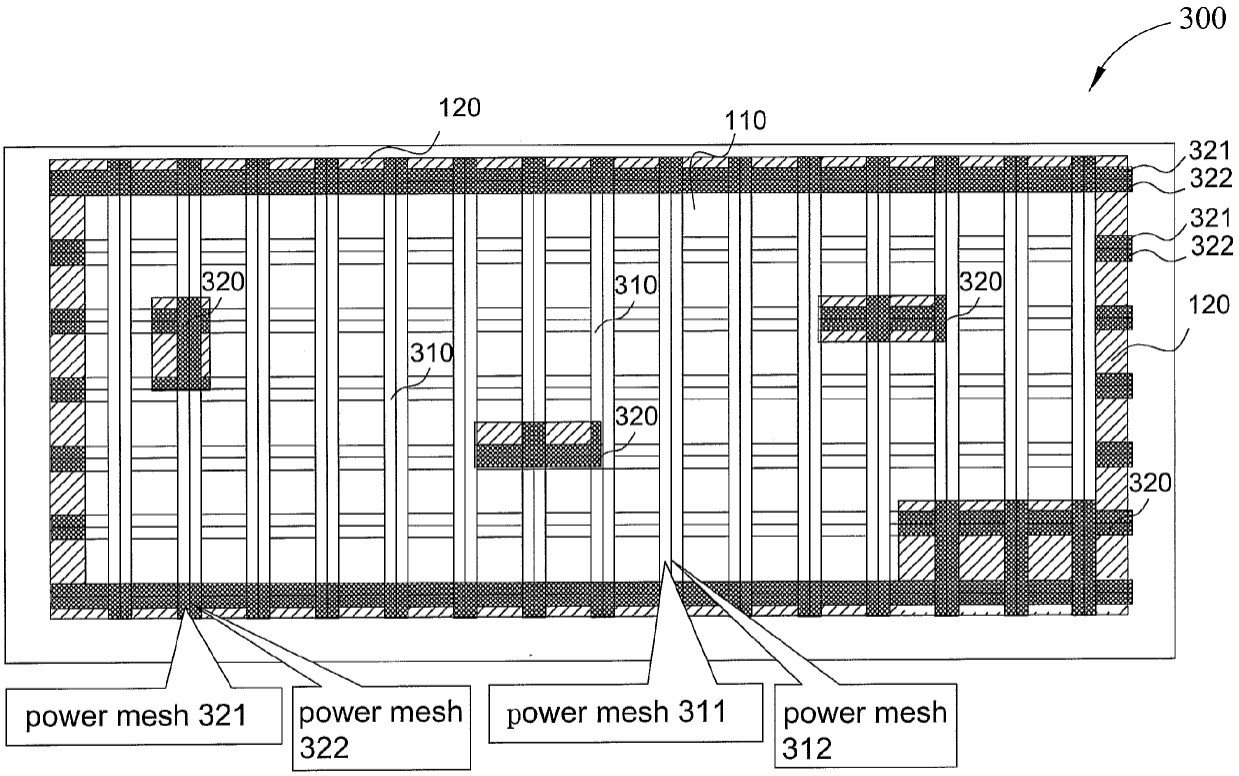


FIG. 3

218 patent at Fig. 3. To treat these wires as not part of either partial local power mesh 310 or partial local power mesh 320 because they are not annotated is unreasonable. The specification explicitly states, "as shown in FIG. 3, the partial local power meshes 310, 320 comprise web-like structures" and "[e]ach of the partial local power meshes 310, 320 comprises a plurality of horizontal power supply wires and a plurality of vertical power supply wires." 218 patent at 3:44-45. The two wires which happen to be annotated 311 and 312, on their own, cannot possibly be viewed as "web-like" and they certainly have no horizontal component. In response to these salient passages, Realtek argues that within Figure 3 "multiple embodiments [are] possible" and "the specification and figure should not be read as limiting." CIB at 55-56 (citing Hr'g Tr. (Subramanian) at 1020:21-24; Hr'g Tr. (Souri) at 1325:2-7). But there is no importation of Figure 3 into the claims here. Figure 3 is simply being compared to the passages of the specification that

[redacted]

explicitly describe it in order to understand what it shows. And it shows web-like intersections comprised of multiple horizontal and vertical wires—one set in white and another in black.

The passages surrounding Figure 5 of the 218 patent are also highly instructive. Figure 5 is described as "a schematic diagram illustrating the relative positions of the local power mesh in FIG. 3 and the global power mesh of FIG. 4":

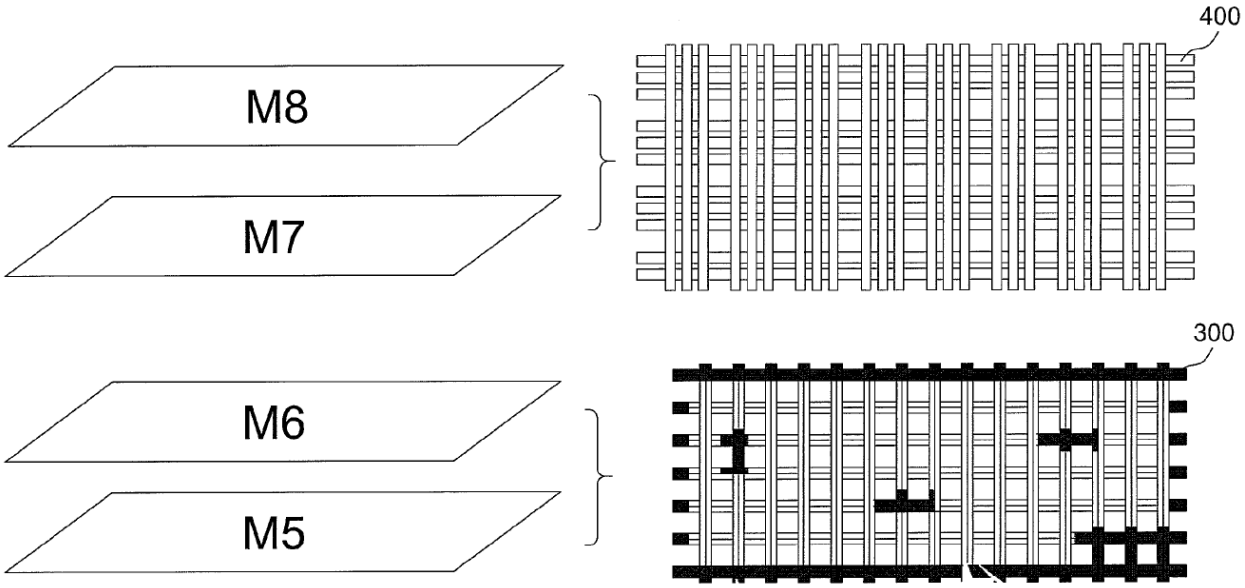


FIG. 5

218 patent at 2:54-56, Fig. 5. Based on this description, and the content of Figure 3, the black and white coloring in the M6 and M5 layers in Figure 5 is highly suggestive of what is meant by partial local mesh 310 (white) and partial local power mesh 320 (black). The patent further notes, in the context of Figure 5, how each of meshes 400 and 300 are made up of at least two layers—one for the vertical wires and one for the horizontal:

> As shown in FIG. 5, the global power mesh 400 is placed above the local power mesh 300 and the partial local power meshes 310, 320 of the local power mesh are placed separately above each power domain.
>
> As mentioned previously, two metal layers are needed to implement either the

> global power mesh 400 or the local power mesh 300. In other words, the embodiments of the invention need at least four metal layers to implement the above mentioned global power mesh 400 and the local power mesh 300. However, at least four metal layers (such as: M5, M6, M7, M8 shown in FIG. 5) are generally reserved for interconnecting the conductive wires of the nodes inside the chip in advanced manufacturing processes. Therefore, the embodiments of the invention can utilize these metal layers to implement the global power mesh 400 and the local power mesh 300. For example, among the metal layers M5˜M8, the local power mesh 300 can be implemented on the lower metal layers M5˜M6 (such as one embodiment of the invention shown in FIG. 3: the horizontal power supply wire is placed on the metal layer M5 and the vertical power supply wire is placed on the metal layer M6). Then, the global power mesh 400 can be implemented on the corresponding metal layer M7˜M8 located above (similarly, such as one embodiment of the invention shown in FIG. 4: the horizontal power supply wire is placed on the metal layer M7 and the vertical power supply wire is placed on the metal layer M8).

218 patent at 4:49-5:7. The concept of a mesh requiring a layer for its horizontal wires and another for its vertical ones is not an isolated occurrence within the patent:

> However, the above mentioned local power mesh 300 can be implemented by those who are skilled in the art without difficulty. Generally speaking, one single metal layer is used to place only one directional routing (such as the above mentioned horizontal power supply wire or the vertical power supply wire) and the routing directions of two adjacent metal layers are mutually different.

Id. at 4:8-14. In sum, the fairest inference to draw from these passages is that "mesh" is used to describe a network of intersecting wires. Realtek's sole reliance on the choice of annotation, or lack thereof, within Figure 3 to find otherwise (*see* CIB at 54-55; CRB at 29-30) is not persuasive.

As to whether a "power mesh" must have an overlapping intersection with each and every one of its wires, the parties appear to agree, correctly, that it does not. In a discussion of Figure 3, AMD acknowledges that the dark grey wire segments on the figure's left and right edges do not form intersections but argues this is immaterial because they simply constitute "part" of a single partial local power mesh 320 which includes all grey segments shown, in toto. RIB at 129. AMD correctly states, "[a]s shown below, the *whole* of partial local power mesh 320 is a non-contiguous area that includes gray wire segments that have overlapping intersections. Thus, the fact that some

gray wire segments in Figure 3 do not overlap does not affect the conclusion that all figures of the patent show power meshes with overlapping intersections." *Id.* (emphasis in original). Realtek agrees. CIB at 56.

As to whether a "power mesh" cannot have overlapping intersections with wires from another mesh (*i.e.*, physical separation), there does not appear to be a claim construction dispute. RRB at 49-50 ("Realtek misrepresents AMD's positions . . . . AMD's construction also does not: . . . preclude a power mesh from having 'overlapping intersections with wires from another mesh.'"); *id.* at 50 (describing the partial local power mesh 320 of Figure 3 as "non-contiguous"). Realtek agrees. CIB at 57-58.

This leaves the question of AMD's "two sets of parallel conductive metal wires that form a net or web-like structure" construction. RIB at 128; RRB at 49. As determined above, it is proper to define a "mesh" as requiring intersections (*i.e.*, a net or web-like structure). It has not been shown, however, that a mesh's wires must be parallel. AMD fails to address this issue in its briefing (*see generally* RIB at 128-130; RRB at 49-51), and it is not impossible in an ordinary sense for a mesh to have non-parallel members (*e.g.*, concentric circles as in a spider web or varied angular crossings). Indeed, the concept of parallelism is not given any importance in the patent—the word is not used at all—and so its inclusion in AMD's construction can only be an improper reading-in of a limitation from the patent's figures. *See, e.g.*, *Bradium Techs. LLC v. Iancu*, 923 F.3d 1032, 1049 (Fed. Cir. 2019) ("[I]t is long-settled that even though 'claims must be read in light of the specification of which they are a part, it is improper to read limitations from the written description into a claim.'") (internal citation omitted). Requiring two sets of wires (as opposed to three or more) is perhaps reasonable, but it, too, finds little support in the specification apart from the patent's figures.

Accordingly, "power mesh" is defined as "a network of intersecting wires capable of distributing power."

2. "global power mesh" and "partial local mesh"

The parties each provide a separate heading for "global power mesh" and "partial local mesh," but note the disputes are subsumed within the discussion of "power mesh," above. CIB at 58-59; RRB at 57-58.

3. "having its position corresponding to"

Claim 12 recites, "a first partial local power mesh having its position corresponding to the position of a first power domain" and "a second partial local power mesh having its position corresponding to the position of a second power domain." 218 patent at cl. 12. The parties dispute the proper meaning of "having its position corresponding to." Realtek views it broadly:

> A POSITA would understand that "having its position corresponding to" allows for relationships or similarities between the position of the partial local power mesh and the power domain, such as being on top of and electrically connected, such that the partial local power mesh can couple to the power domain positioned below by way of the via holes. Tr. (Souri) at 385:18- 386:20; CDX-0003C.0042. Thus, some overlap between the position of the partial local power mesh and the position of the power domain is sufficient to meet this limitation. Tr. (Souri) at 386:9; CDX-0003C.0042.

CIB at 59. AMD argues for "having the same shape and position." RIB at 132.

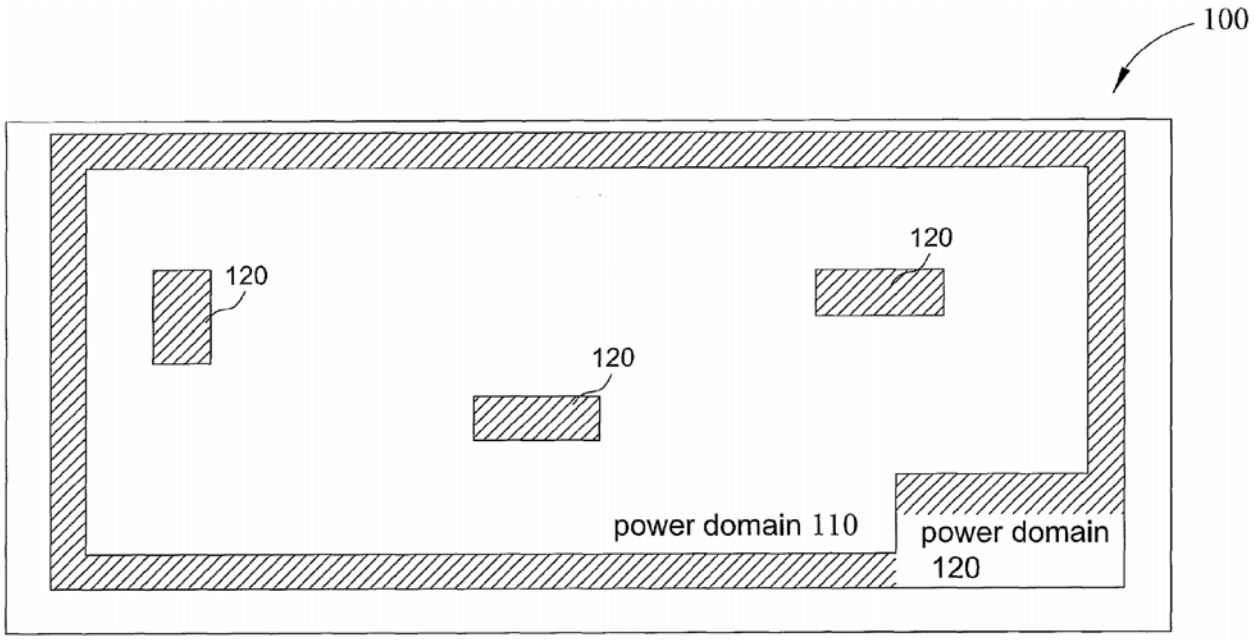
There is insufficient intrinsic support for AMD's restrictive construction, and it is not accepted. No party has argued the patentee acted as its own lexicographer, nor that prosecution disclaimer has occurred. Thus, the plain and ordinary meaning applies. *Kyocera Senco Industrial Tools Inc. v. Int'l Trade Comm'n*, 22 F.4th 1369, 1378 (Fed. Cir. 2022) (citing *Thorner*, 669 F.3d at 1365). And in a plain sense, to describe an object's position as "corresponding" to another object is a loose concept, which falls short of requiring the "same" position, let alone the "same"

shape that AMD urges. Realtek persuasively cites *Broadcom Corp. v. Emulex Corp.*, involving signal rates "corresponding" to frequency offsets, which explained this conceptual difference:

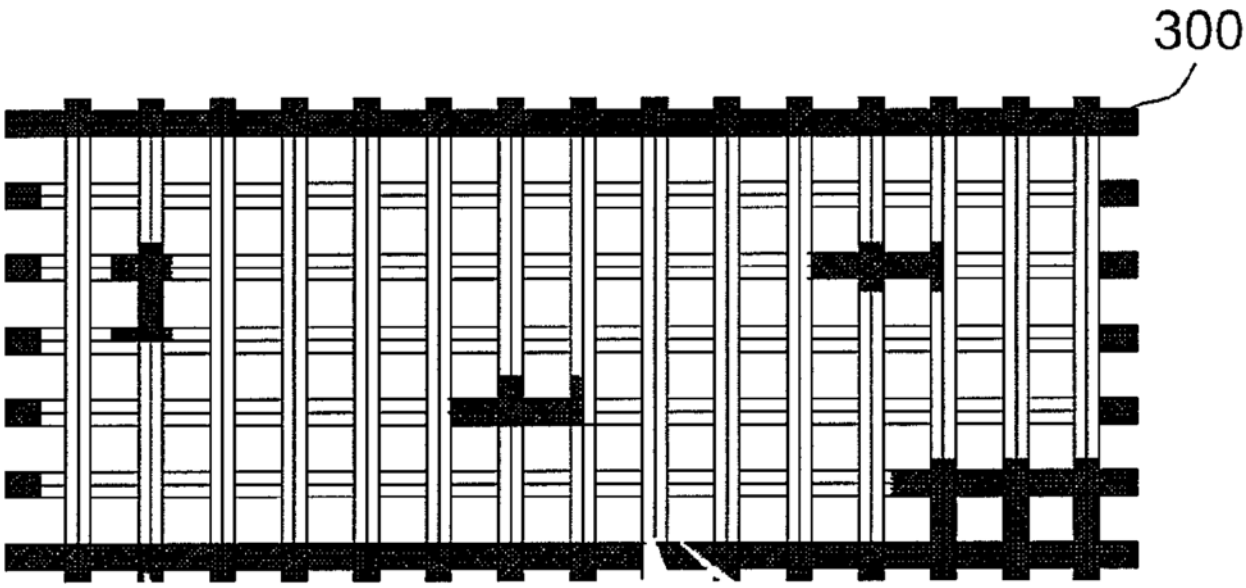
> The record, especially the intrinsic evidence of the patent's meaning, does not support Emulex's argument. The claim language itself does not necessitate that "corresponding to" limits claim 8 to full rate architecture. Indeed the claim does not use language of equation but of correspondence, a much broader concept. Moreover the record does not contain evidence that the patentee acted as his own lexicographer to define "corresponding to" as "equal to."

732 F.3d 1325, 1333 (Fed. Cir. 2013); *see* CIB at 61.

In response, AMD argues that Figures 1 and 3 "make[] it clear that the local power mesh is divided into two partial local power meshes that match the shapes of the power domains below them." RIB at 133. This is not an accurate characterization of the figures. As shown in Figure 3, reproduced above, the partial local power mesh 320 (dark grey color) is constrained by the shape and size of the power domain 120 located below, but it does not match that shape. The power domain is rectangular while the mesh has an intersecting segment shape. This is captured most clearly by a comparison of Figure 1 (power domains) and Figure 5 (local power mesh):



[redacted]



218 patent at Figs. 1, 5 (excerpted). So it cannot be said that the figures show the "same size and shape" between power domains and respective partial local power meshes. AMD nonetheless emphasizes that "the width and height" of the wires matches the "width and height" of the power domain below (RRB at 53), but overall width and height are not the same as "shape," as in the proposed construction.

AMD also highlights that portion of the specification which discloses how partial local power meshes 310 and 320 are "defined" "based on the positions of the power domains 110, 120":

> Firstly, the local power mesh 300 is evenly distributed on top of the entire chip circuitry. Then, the partial local power meshes in the local power mesh 300 corresponding to the power domains 110, 120 are defined (such as partitioning the local power mesh 300 based on the positions of the power domains 110, 120 so that the plurality of partitioned power meshes are not electrically coupled to each other) to form the above mentioned partial local power meshes 310, 320.

218 patent at 5:60-6:1; *see* RIB at 133; RRB at 52. Again, this is suggestive that partial local meshes at least roughly line up with the "positions of the power domains" in the layers below, but the domains are exclusively illustrated in the patent as two-dimensional areas and the meshes as collections of linear elements. This passage is also balanced out by others, including one that

describes how the purpose of positioning the partial mesh "corresponding to" the positions of the power domains is simply to ensure a via can drop down and provide power:

> Please refer to FIG. 3 which shows a schematic diagram illustrating a local power mesh according to one embodiment of the invention. As shown in FIG. 3, the local power mesh can be partitioned into two different partial local power meshes 310, 320 at the positions corresponding to the positions of the power domains 110, 120. In one embodiment of the invention, the partial local power mesh 310 is placed on top of the power domain 110 and the partial local power mesh 320 is place on top of the power domain 120. Thus, the partial local power meshes 310, 320 can couple to the power domains 110, 120 positioned below by way of the via holes ("via").

218 patent at 3:33-43. This connectivity does not require the same size and shape, only partial overlap.

In sum, "corresponding to" is, in a plain and ordinary sense, a broader concept than complete identity, and no party has argued patentee lexicography or disclaimer warrants departing from that plain and ordinary meaning. Nothing in the patent conflicts with this breadth. Accordingly, "a first partial local power mesh having its position corresponding to the position of a first power domain" and "a second partial local power mesh having its position corresponding to the position of a second power domain" require only that the partial mesh overlap to some degree with its respective domain when viewed from above.

4. Limitations [12e] and [12f]

Claim 12 recites, "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and wherein the first metal layer and the second metal layer are different layers." 218 patent at cl. 12 (limitations [12e] and [12f]). The parties dispute whether "these last two claim limitations require that the global power mesh have all its horizontal power supply wires on one layer and all its vertical power supply wires on a different layer" (AMD) or not (Realtek). *See* CIB at 61-63; RIB at 140-143.

In the absence of patentee lexicography or prosecution disclaimer, the plain and ordinary meaning of a claim term controls. *Kyocera*, 22 F.4th at 1378. And when a patent claim uses "comprising," there is a presumption the claim is open-ended so that an infringing apparatus may include more than what is recited. *MagSil Corp. v. Hitachi Global Storage Techs., Inc.*, 687 F.3d 1377, 1383 (citing *Gillete Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1371 (Fed. Cir. 2005)).

It is clear that "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and wherein the first metal layer and the second metal layer are different layers" requires the global mesh to be comprised of some amount of horizontal wires on a first metal layer and some amount of vertical wires on a different, second, metal layer. That is all. AMD's reasoning—that "[t]hose layers would only be 'different' if one layer has the horizontal wires, and the other layer has the vertical wires" (RRB at 56)—does not logically follow. Layers within a semiconductor stack are "different" if they are in a different vertical stratum. They are not defined by what metal components may or may not reside within.

AMD refers to a possible prosecution history disclaimer event involving prior art reference Chen. *See* RIB at 140-142; RRB at 56. But the cited pages do not rise to the "clear and unmistakable" standard. *Thorner*, 669 F.3d at 1366-67. It is true the applicant amended claim 12 to include the present limitations following a rejection, but the applicant's grounds for traversal are hard to follow. The applicant initially stated the prior art fails to teach or suggest the newly added horizontal/vertical limitation, and concludes with that argument; but the body of the response argues Chen's alleged global mesh (power grid 22) is not electrically connected to the alleged local mesh (power grid 21), in contrast to the claim:

[redacted]

(A) Claims 12-18

Independent claim 12 recites (emphasis added):

> 12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:
>
> a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;
>
> a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and
>
> a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;
>
> wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;
>
> **wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and**
>
> **wherein the first metal layer and the second metal layer are different layers**.

It is respectfully submitted that the combination of references cited by the Examiner fails to teach or suggest at least the above-emphasized features of independent claim 12.

As set forth above, Ladanza is silent on the structure of the chip-level connection declaration 501. In the Examiner's rejection of claim 12 (beginning on page 9 of the Office Action), the Examiner equates the global power mesh 400 and the local power mesh 300 of the present application as being comparable to the second power grid 22 and the first power grid 21 of Chen (FIG. 2). Applicant disagrees. In the present application (see paragraph [0020], for example), the global power mesh 400 couples to the external power (such as: by way of the I/O pin of the chip) to conduct the external power into the chip while the local power mesh 300 couples to the global power mesh 400 and the chip circuitry. In other words, the internal circuits of the chip correspond to the power domains 110, 120. Then, the external power will be inputted into the chip circuitry by way of the global power mesh 400 and the local power mesh 300.

In contrast, Chen has no electrical connections between the second power grid 22 and the first power grid 21 and no electrical connections between the VDD_g power network 11 and the VDD_i-VDD_n power networks 15 (see FIGS. 1 and 2). In addition, the VDD_g power network 11 and the VDD_i-VDD_n power networks 15 respectively have their own power sources.

"[E]ach and every element of the claimed invention [must] be taught by the references." *In re Royka.* It is respectfully submitted that Ladanza and Chen fail to teach or suggest that "the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer, and wherein the first metal layer and the second metal layer are different layers" as is recited in independent claim 12 of the present application. Thus, all elements of claim 12 are not taught by the combination of references utilized by the Examiner.

JX-0008.176-177. The electrical connections between meshes, and how the power supply wires are placed within the metal layers, are completely different limitations, however. *See id.* at 176 ("a global mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately"); *see* 218 patent at cl. 12 (same). So it is not at all clear that the applicant viewed Chen as failing to include horizontal wires in one layer and metal wires in another layer, and that the examiner allowed the claims on this basis. *See id.* at 188 (allowance notice). This is insufficient for prosecution history disclaimer, as AMD reasonably admits is a possibility. RIB at 141-142. And the remarks do not otherwise "inform the claim construction" (*id.* (citing Shire, 787 F.3d at 1366)) for the same reason—there is no cognizable connection to the limitation at issue.

AMD also relies on the fact that "[e]very embodiment of the global power mesh in the specification shows all horizontal wires on one layer and all vertical wires on a different layer." RIB at 140 (citing 218 patent at Figs. 4-6). But this is insufficient when the plain meaning is so clear—a global mesh with some amount of horizontal wires on a first metal layer and some amount of vertical wires on a different, second, metal layer. Lastly, AMD suggests that without its

interpretation, the limitation has no meaning. *See* RIB at 142 ("If these claim limitations covered embodiments where both layers of the global power mesh included both horizontal and vertical wires, it is hard to envision what *limitations* these words place on the scope of the claim other than requiring a two-layer global power mesh." (emphasis in original)). Not so. At least one example comes to mind that would fall outside of the scope: a global mesh existing within just one layer.

Accordingly, "wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and wherein the first metal layer and the second metal layer are different layers" means what it says—a global mesh comprised of some amount of horizontal wires on a first metal layer and some amount of vertical wires on a different, second, metal layer.

5. "to provide the power needed by the first power domain and the second power domain"

Claim 12 recites, "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately." 218 patent at cl. 12. Within this limitation, the parties dispute whether "to provide the power needed" encompasses the absence of power (i.e., zero volts). Realtek argues "[t]here is no mechanism contemplated in the patent to not provide power" and "if 'power needed' is zero, then there is nothing 'to provide.'" CIB at 64. AMD argues to the contrary, reasoning "[i]f one or both of the power domains needed zero power, then the global power mesh would still be providing the power *needed* by the first domain *and* the second domain." RIB at 137 (emphasis in original).

No party argues inventor lexicography or prosecution disclaimer has occurred, so the plain and ordinary meaning controls. *Kyocera*, 22 F.4th at 1378. And in a plain and ordinary sense, the provision of nothing is no provision at all; and to need nothing is to not have a need. CRB at 36.

In AMD's view, a keyboard could be said to provide WiFi signals "needed" by a personal computer that uses an ethernet cable to access a network—even though the keyboard squarely does not and no WiFi is needed by the computer. *See* RRB at 54 ("A 'lower voltage' includes zero volts."). So AMD's view that the limitation is met when a global mesh provides zero volts to a partial local mesh at those times when that local mesh needs no power is untenable. And Realtek's observation that "[t]he patent consistently describes operational modes and working voltages which are providing power to the power domains. . . . There is no mechanism contemplated in the patent to not provide power" is correct and goes unrebutted by AMD. CIB at 64 (citing 218 patent at 1:18-34, 4:31-36, 5:10-17); *see* RIB at 136-139; RRB at 54-55. AMD's reference to contradictory attorney argument made by Realtek during the *Markman* hearing (RIB at 138-139) is just that—attorney argument—and does not warrant departing from the clear thrust of the intrinsic evidence and plain and ordinary meaning.

Accordingly, "to provide the power needed by the first power domain and the second power domain" means "to provide the non-zero levels of power needed by the first power domain and second power domain."

6. "separately"

Claim 12 recites, "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately." 218 patent at cl. 12. Within this limitation, the parties dispute the meaning of "separately." Realtek argues it means separate-in-space, stating, "[a] POSITA would understand that the term 'separately' requires a physically distinct path for the voltages to be provided to the first power domain and second domain through the global power mesh." CIB at 64 (citing, *inter alia*, 218 patent at Figs. 3-6; 3:1-4:45; 5:9-20; 6:8-24; 6:8-20; 5:54-6:4, claims 1, 12, 15-18, 19). AMD argues it means anything other than separate wires, such as the same wire

but separate-in-time, stating, "[o]ne way to [accomplish the limitation] would be to deliver a 'normal operating voltage' at some times and a 'lower voltage' (such as zero volts) at other times for a 'sleeping mode operation,' as discussed in the specification." RIB at 140 (citing 218 patent at 1:2-25); *id.* at 139 (citing 218 patent at cl. 15).

No party contends inventor lexicography or prosecution disclaimer has occurred, so the plain and ordinary meaning controls. *Kyocera*, 22 F.4th at 1378. As to that meaning, Realtek has the more persuasive position. The specification uses the term "separate" only once—in a separate-in-space context: "As shown in FIG. 5, the global power mesh 400 is placed above the local power mesh 300 and the partial local power meshes 310, 320 of the local power mesh are placed *separately* above each power domain." 218 patent at 4:49-52 (emphasis added). Its appearance in the claims (the only other appearance) is also focused on a "coupling" and implies that coupling is what is used "to provide the power needed by the first power domain and the second domain separately." *Id.* at cl. 12. This too is suggestive of the path the power takes—*i.e.*, a separate-in-space context. And the patent's figures illustrate how this is accomplished with separate pathing. The global power mesh 400 is laid on top of the local power mesh 300 and connects to different portions of that mesh (*i.e.*, partial local power meshes) through different vertical vias. 218 patent at 5:8-20, Figs. 5, 6. The patent further refers to voltages VDD1 and VDD2 as being supplied to the local mesh from distinct (*i.e.*, separate) wires 401 and 402. *Id.* at 4:31-38. On the whole, then, the intrinsic evidence strongly favors a separate-in-space meaning for "separate."

AMD's separate-in-time interpretation, on the other hand, enjoys no meaningful intrinsic support. AMD cites one passage from the specification: "Therefore, the normal operating voltage is still used by these circuits for its operation while the other circuits of the chip only need a lower voltage for maintaining the sleeping mode operation." 218 patent at 1:22-25; *see* RIB at 140. But

this only reinforces separate-in-space, because a single mesh cannot supply different voltages at the same time unless by different paths. The patent explains as much:

> Therefore, different powers need to be supplied to the different circuits inside the chip so that the circuits can perform different operations during the sleeping mode. Hence, it is common practice[] to arrange multiple power domains in the chip circuitry. In other words, circuits in *different power domains are coupled to different powers respectively* so that the circuits of different power domains use different powers to support the different operations that are just mentioned.

Id. at 1:26-33 (emphasis added). Different respective couplings are strong support for Realtek's interpretation of "separately."

AMD also argues principles of claim differentiation favor its construction. RIB at 139-140. It points specifically to dependent claim 15, which reads:

> 15. The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain.

218 patent at cl. 15. AMD views this claim as "already recit[ing] the 'separate power wires' in Realtek's proposed construction" and reasons, "[t]his makes Realtek's construction improper because dependent claims are 'generally narrower in scope than the claims from which they depend.'" RIB at 139 (citing *Glaxo Grp. Ltd. v. Ranbaxy Pharm. Inc.*, 262 F.3d 1333, 1336 (Fed. Cir. 2001)). This argument has some merit; it is difficult to see how claim 12 might accomplish the provision of power to partial local power meshes "separately" without the use of first and second power wires.

However, using Realtek's construction does not mean the scope of claim 12 is identical to claim 15. As just one example, claim 12 says nothing about the global mesh's need for ground wires. And claim 15 explicitly recites, "wherein the global power mesh comprises: at least one ground wire." 218 patent at cl. 15. This is enough to differentiate the two claims. *World Class*

Tech. Corp. v. Ormco Corp., 769 F.3d 1120, 1125-6 (Fed. Cir. 2014) ("But our construction of "support surface" does not give claim 1 the same scope as claim 6. At a minimum, claim 6 requires that the support surface form a corner (edge) with one side of the slot. That requirement is not implicit in claim 1 under our construction of "support surface."); *Kraft Foods, Inc. v. Int'l Trading Co.*, 203 F.3d 1362, 1368 (Fed. Cir. 2000) ("Moreover, that the claims are presumed to differ in scope does not mean that every limitation must be distinguished from its counterpart in another claim, but only that at least one limitation must differ."). Even then, and contrary to AMD's assertion (RRB at 55), the need to avoid redundancy across claims through claim differentiation is not an inflexible rule that supersedes all other principles of claim construction (*see SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016); *Kraft Foods*, 203 F.3d at 1368 ("That the patentee chose several words in drafting a particular limitation of one claim, but fewer (though similar) words in drafting the corresponding limitation in another, does not mandate different interpretations of the two limitations . . .")). Indeed, there are redundant limitations within claim 12 itself indicative of this particular patentee's drafting style. *See* 218 patent at cl. 12 (reciting horizontal wires on a "first metal layer" and vertical wires on a "second metal layer," then redundantly stating "the first metal layer and the second metal layer are different layers").

AMD finally makes reference to contradictory arguments from Realtek during the *Markman* hearing. RIB at 140; RRB at 55. As with previous claim terms, this possibly conflicting attorney argument is insufficient to override the thrust of the intrinsic evidence.

Accordingly, "separately" means "through separate electrical paths."

7. "power domain"

Realtek identifies "power domain" as having a disputed construction. It states, "[a] POSITA would understand that a 'power domain' is a portion of the integrated circuit that has a

different power requirement from the power requirements of another portion of the integrated circuit" and claims broadly "[t]his understanding is supported by intrinsic and extrinsic evidence." CIB at 66 (citing, *inter alia*, Hr'g Tr. (Souri) at 552:24-3, 1313:12-18; 218 patent at Abstract, 1:12-43; 2:24-4:52, 5:8-6:50, cls. 1-20, Figs. 1-6). Realtek represents that "Dr. Subramanian does not disagree" (*id.* (citing Hr'g Tr. (Subramanian) at 923:4-924:3)), and otherwise rejects the idea that a requirement of zero volts (*i.e.*, no power requirement) qualifies (*id.*; CRB at 38). Realtek further notes that AMD fails to put forward any construction of its own. *Id.*

AMD disagrees. It does not address the testimony of Dr. Subramanian or provide its own construction (*see* RIB at 130-132; RRB at 51-52); but it takes the position that "there is no support anywhere in the specification that one of those 'different powers' cannot be no power or that the [specification's] 'lower voltage' cannot be zero volts" (RIB at 131 (citing 218 patent at 1:16-33; Hr'g Tr. (Subramanian) at 927:14-25)). AMD concludes, "Realtek's construction should not be adopted. But if Realtek's construction is adopted, to avoid further arguments on how to construe the construction, AMD requests that the ALJ make clear that 'different power requirements' can include no power or zero volts." *Id.* at 131-132.

Neither party is persuasive. AMD's "construction" is not a construction but an application of a construction to a given embodiment and need not be addressed at this time. Realtek's construction is, on the other hand, understandable but demonstrably incorrect. To define "power domain" as a portion of a circuit that has a different power requirement than another portion is to exclude all integrated circuits that operate under a single power requirement; *i.e.*, they would have no power domain at all as opposed to a single power domain. Surely, a POSITA would treat such an IC as the latter. This plain and ordinary interpretation is consistent with the specification, which

[redacted]

explicitly uses the word "different" before "power domain" to denote portions of a circuit operating under different power requirements:

> Therefore, different powers need to be supplied to the different circuits inside the chip so that the circuits can perform different operations during the sleeping mode. Hence, it is common practices to arrange multiple power domains in the chip circuitry. In other words, circuits in different power domains are coupled to different powers respectively so that the circuits of different power domains use different powers to support the different operations that are just mentioned.
>
> . . . .
>
> Please refer to FIG. 1 which 1 illustrates a chip 100 having multiple power domains. As shown in FIG. 1, the chip 100 has two different kinds of power domains 110, 120 where the power domain 110 is illustrated by the blank area and the power domain 120 is illustrated by the oblique line area.
>
> As mentioned before, the power domains 110, 120 correspond to different powers that supply different voltages to the different circuits of the different power domains. It should be noted that, in the subsequent disclosure, the invention provides a power routing arrangement method and its related structure so that the user can complete the design of the power routing more easily.

218 patent at 1:26-33, 2:63-3:7.

It is therefore much more reasonable to define "power domain" in terms of what it is than what it is not. And in a plain and ordinary sense, a "power domain" is a "portion of an integrated circuit whose elements have the same power requirement." *See, e.g.*, JX-0043 (a prior art reference contrasting ICs with multi-power-domains (local) and those with single domains (global)). This construction is compatible with the above intrinsic evidence excerpts and further compatible with the patent's explanation of normal operating modes and sleep mode modes. The patent states:

> (b) Description of the Related Art
>
> As the circuitry of the integrated circuit becomes more and more complicate[d], there are possibilities that different portions of the circuitry of a chip need different voltages (powers) at the same time. For example, the chip circuitry may have two kinds of operating modes: the normal operating mode and the sleeping mode. During the normal operating mode, the entire chip circuitry uses the operating voltage for its normal operation. But during the sleeping mode, only part of the chip

> circuitry needs to be maintained in the normal operating mode. Therefore, the normal operating voltage is still used by these circuits for its operation while the other circuits of the chip only need a lower voltage for maintaining the sleeping mode operation.
>
> Therefore, different powers need to be supplied to the different circuits inside the chip so that the circuits can perform different operations during the sleeping mode. Hence, it is common practices to arrange multiple power domains in the chip circuitry. In other words, circuits in different power domains are coupled to different powers respectively so that the circuits of different power domains use different powers to support the different operations that are just mentioned.

218 patent at 1:12-33. As written, the patent considers the hypothetical IC to have multiple power domains even though at some times "the entire chip circuitry uses the operating voltage for its normal operation"; *i.e.*, power requirements are the same across all domains.

Accordingly, "power domain" is construed as "a portion of an integrated circuit whose elements have the same power requirement."

8. "local power mesh"

"Local power mesh," as opposed to "partial local power mesh," appears in claim 12 twice—"first local power mesh" and "second local power mesh." 218 patent at cl. 12. Realtek contends the terms are in fact meant to refer back to their respective "*partial* local power mesh." CIB at 67; CRB at 38. Order No. 20 previously considered and adopted this understanding in evaluating AMD's claims of indefiniteness (Order No. 20 at 7-10) and Realtek argues that "AMD does not dispute this, presenting no evidence at trial and no argument in its pre-hearing brief" (CIB at 67). Indeed, AMD does not present any dispute in its briefing (*see generally* RIB; RRB).

Accordingly, "[first/second] local power mesh" is understood to be "[first/second] partial local power mesh."

D. Infringement

According to Realtek's post-hearing briefing, the use, manufacture, or sale of the Accused Products infringe claims 12, 13, and 15-18. CIB at 67. Of these, claim 12 is independent with

[redacted]

claims 13 and 15-18 all depending (directly or indirectly) from claim 12. For the reasons discussed below, Realtek has shown infringement of these claims by the Accused Products.

1. Claim 12

For reference, claim 12 of the 218 patent requires:

> 12. A power routing structure applied in an integrated circuit having multiple power domains, comprising:
>
> [12a] a first partial local power mesh having its position corresponding to the position of a first power domain and coupling to the first power domain;
>
> [12b] a second partial local power mesh having its position corresponding to the position of a second power domain and coupling to the second power domain; and
>
> [12c] a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately;
>
> [12d] wherein the first partial local power mesh and the second partial local power mesh are positioned on the same metal layer while the global power mesh and the first local power mesh are positioned on different metal layers;
>
> [12e] wherein the global power mesh includes a plurality of horizontal power supply wires placed on a first metal layer and a plurality of vertical power supply wires placed on a second metal layer; and
>
> [12f] wherein the first metal layer and the second metal layer are different layers.

218 patent at cl. 12 (annotated). In support of infringement, Realtek primarily relies on the testimony of Dr. Souri and a series of demonstratives showing top-down views of various metal layers within the stack of each Accused Product. For each limitation, Realtek contends as follows:

> *Element 12[pre]*. AMD asserts that the preamble is not limiting. RPHB at 127. Regardless, the preamble is met because all Accused Products include a power routing structure routing power applied in an integrated circuit having at least two power domains.
>
> . . . .
>
> *Element 12[a]-12[b]*. A First PLPM and a Second PLPM. Each Accused Product includes a first and second partial local power mesh ("PLPM"), which include a network or plurality of metal wires capable of distributing power: the first PLPM includes a plurality of metal wires capable of distributing VDD1 power (and ground

[redacted]

wires) and the second PLPM includes a plurality of metal wires capable of distributing VDD2 power (and ground wires). . . . Each PLPM also includes two sets of parallel conductive metal wires that have overlapping intersections and form a net or web-like structure (if required). . . . Each Accused Products includes a "first power domain" and "second power domain." . . . Exemplary portions of the identified first and second power domains (in cyan and orange, respectively) for each Accused Product are shown below, as explained by Dr. Souri's testimony. . . . The Accused Products have a first and second PLPM having its position corresponding to a first or second power domain respectively. . . . The undisputed evidence shows that the first partial local power mesh and second partial local power mesh are each positioned above, overlap, and can couple to the respective power domain. . . . For all Accused Products, the power domains are in the [redacted] where the PLPMs are present. . . . Dr. Souri explained that the PLPMs and their respective power domains overlap [and] each PLPM and the respective power domain are positioned in such a way and can—and in fact do— couple by vias dropping down through the metal layers. . . . the first partial local power mesh and the second partial local power mesh "coupl[e] to" the respective power domain (or portions of the power domain). . . . Dr. Souri explained his trace-down analysis showing that the coupling limitation is met and provided exemplary images demonstrating coupling are below, in which VDD1 wires are marked in blue and VDD2 wires are marked in red and show coupling by via from the VDD1, VDD2, or ground pad down to the power domains, through the global and partial local power meshes.

. . . .

Element 12[c]. . . . Each Accused Product includes a global power mesh on the top two metal layers of each Accused Product, *e.g.*, [redacted] . . . . Each metal layer of the global power mesh includes a plurality or network of conductive metal wiring capable of distributing power to the power domains (VDD1 and VDD2). . . . Although not necessary (*see supra* at IV.A.1-4), when both metal layers identified for the first partial local power mesh for each Accused Product are viewed from above, the wiring of these metal layers form overlapping "intersections" and a "net-like" or "web-like" structure. . . . The undisputed evidence shows that identified global power mesh in each Accused Product couples to the first partial local power mesh and the second partial local power mesh as Dr. Souri explained in his trace-down analysis from the power pads in the global power mesh. . . . [E]ach Accused Product has a wiring structure in the global power mesh such that power from two different power pads (VDD1 and VDD2) is provided to two different power domains, through distinct wires and via paths.

. . . .

[redacted]

> *Element 12[d]*. . . . In the [redacted], the first PLPM is on [redacted] and the global power mesh is on [redacted] and have a different wiring structure as Dr. Souri testified. . . . In the [redacted], the first PLPM is on [redacted] and the global power mesh is on [redacted] and have a different wiring structure.
>
> . . . .
>
> *Element 12[e]*. . . . As Dr. Souri testified, [redacted] products include horizontal power supply wires on the first layer of the global power mesh ([redacted] and vertical power supply wires on a second layer of the global power mesh ([redacted] and [redacted] and [redacted] are different metal layers. . . . [redacted] products include horizontal power supply wires on the first layer of the global power mesh ([redacted] and vertical power supply wires on the second layer of the global power mesh ([redacted] as shown below and [redacted] are different metal layers.
>
> . . . .
>
> *Element 12[f]*. . . . As discussed above, each Accused Product meets this limitation because the first and second metal layers are different metal layers as shown in the layout files and design rules.

CIB at 68-143 (citing, *inter alia*, Hr'g Tr. (Souri) at 397:22-497:15, 609:18-614:13; CPX-0675C(SC)-CPX-0682C(SC); JPX-0363C(SC)-JPX-0396C(SC); CPX-0525C(SC)-CPX-0528C(SC); CPX-0651C(SC); JX-0023C (Seahra); JX-0024C (Seahra); CPX-0215C(SC); CX-2226; CX-2227). The Accused Products infringe the limitations of claim 12 as alleged in view of the testimony of Dr. Souri and the various image sequences.

AMD raises several challenges, none of which are persuasive. First, AMD complains that Realtek's identification of layers, meshes, and wires in the Accused Products is "results-oriented" in that "Dr. Souri first traces down from two power pads to the circuit layer and then if the wires in the trace-down have some overlapping intersections, he declares them to be one global or two partial local power meshes depending on whatever he needs them to be for infringement." RIB at

143-144. A "results-oriented" approach has no relevance as to whether each and every limitation is present in the accused devices, however. "An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman*, 52 F.3d at 976. A patentee "can employ any method of analysis that is probative of the fact of infringement." *Forest Labs., Inc. v. Abbott Labs.*, 239 F.3d 1305, 1312 (Fed. Cir. 2001)..

Next, AMD argues that "[p]rinciples of claim differentiation, and the specification of the 218 patent, require that there be differences between the global power mesh and the partial local power meshes" but views Dr. Souri as "hopelessly" pointing to what is essentially the same structure and calling it a "global power mesh" in one product and two "partial local power meshes" in another. RIB at 144-146. AMD provides the following images, where the first is alleged by Realtek to show two partial meshes, and the second is a global mesh:

RIB at 145-146 (citing CDX-0003C.425, -1160; Hr'g Tr. (Souri) at 613:7-615:1). AMD complains, "Dr. Souri offers no reasoned explanation for why the wires in the top two demonstratives are *two* partial local power meshes while the wires in the bottom demonstrative are *one* global power mesh." *Id.* at 146 (emphasis in original).

Contrary to AMD's suggestion, there already is a difference in the meanings of "global power mesh" and "partial local power mesh." As recited above, a "global power mesh" must be capable of distributing power to multiple power domains (Order No. 21 at 25), and a partial local power mesh need not be so capable (it lacks the descriptor "global"). The flexibility to otherwise view a collection of wires providing two levels of power as a single global mesh *or* as two partial local meshes is not the fault of Dr. Souri but of the 218 patent itself, which offers no other means of distinguishing between global and local. Tellingly, AMD cites no intrinsic evidence negating the breadth and flexibility of these claim terms. *See* RIB at 146-147; RRB at 57-59.

[redacted]

AMD next contends that Realtek failed to show the partial local meshes have the same size and shape as their underlying power domains (RIB at 147; RRB at 59), but this is based on a faulty claim construction addressed above. Similarly, AMD contends Realtek failed to show "that one layer of the global power mesh has only the vertical wires and a 'different' layer has only the horizontal wires." RIB at 147-148; RRB at 59. This too is based on the faulty claim construction addressed above.

Accordingly, Realtek has shown the Accused Products infringe claim 12.

2. Claim 13

For reference, claim 13 of the 218 patent requires:

> 13. The power routing structure according to claim 12, wherein the global power mesh is positioned above the first local power mesh.

218 patent at cl. 13. Realtek contends, as testified by Dr. Souri, that the claim is met in the TSMC Products because "the first PLPM is on [redacted] and the global power mesh is on AP and [redacted] which are layers above [redacted];" and in the GF Products because "the first PLPM is on [redacted] and the global power mesh is on [redacted], which are layers above [redacted]." CIB at 143; Hr'g Tr. (Souri) at 432:12-433:11, 456:19-25, 464:21-23, 469:12-14, 476:19-22, 481:23-482:1, 487:4-7, 492:12-15, 497:16-20. AMD does not dispute infringement of claim 13 apart from its dependency on claim 12. RIB at 152; RRB at 58-59. In light of the cited evidence and opinion, the additional elements of claim 13 are met in the Accused Products, and the claim is therefore infringed.

3. Claim 15

For reference, claim 15 of the 218 patent requires:

> 15. The power routing structure according to claim 12, wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain.

[redacted]

218 patent at cl. 15. Realtek contends, as testified by Dr. Souri, that the claim is met in all Accused Products because each "has a global power mesh that comprises at least one ground wire on [redacted] or on [redacted]," "the global power mesh of each Accused Product also includes a first, VDD1 power wire," and "[t]he first power wire of each Accused Product is connected to the power pad/supply providing power to the first power domain through the VDD1 wiring (marked in blue) by vias to the first power domain," "the global power mesh of each Accused Product also includes a second, VDD2 power wire," and "the second power wire (marked by red arrow and annotations) of each Accused Product is connected to the power pad/supply providing power to the second power domain through the VDD2 wiring (annotated in red) by vias to the second power domain." CIB at 144-172; Hr'g Tr. (Souri) at 447:24-448:3, 432:25-434:24, 456:19-25, 453:13-455:5, 432:25-435:18, 461:19-462:1, 463:17-465:7, 467:16-19, 468:17-469:23, 474:12-19, 475:22-477:6, 479:19-23, 480:24-482:11, 485:2-487:16, 490:7-13, 491:14-492:24, 495:12-18, 496:22-489:6. AMD does not dispute infringement of claim 15 apart from its dependency on claim 12. RIB at 152; RRB at 58-59. In light of the cited evidence and opinion, the additional elements of claim 15 are met in the Accused Products, and the claim is therefore infringed.

4. Claim 16

For reference, claim 16 of the 218 patent requires:

> 16. The power routing structure according to claim 15, wherein the first partial local power mesh comprises: at least one first local ground wire that couples to the ground wire of the global power mesh; and at least one third power wire that couples to the first power wire and the first power domain.

218 patent at cl. 16. Realtek contends, as testified by Dr. Souri, that the claim is met in all Accused Products because:

> [T]he first PLPM of each Accused Product comprises a first local ground wire (marked by yellow arrow on layer [redacted]

[redacted]

[redacted]), that couples through vias (marked by black arrows and yellow rectangles) to the ground wire of the global power mesh (marked by yellow arrow on layer [redacted] or layer [redacted]).

. . . .

[T]he first PLPM of each Accused Product comprises a third power wire (VDD1) (marked in blue with blue arrows) on layer [redacted] or [redacted] that couples by via (marked by black arrows and blue rectangles) to the first power wire (on layer [redacted]) or [redacted]).

. . . .

[T]he third power wire (VDD1, marked in blue) of each Accused Product also couples to the first power domain. . . .

CIB at 173, 179, 184; Hr'g Tr. (Souri) at 435:19-439:5, 465:9-14, 470:1-7, 477:9-15, 482:14-21, 487:19-25, 493:2-8, 498:9-15. AMD does not dispute infringement of claim 16 apart from its dependency on claim 12. RIB at 152; RRB at 58-59. In light of the cited evidence and opinion, the additional elements of claim 16 are met in the Accused Products, and the claim is therefore infringed based on infringement of claims 12 and 15.

5. Claim 17

For reference, claim 17 of the 218 patent requires:

17. The power routing structure according to claim 16, wherein the second partial local power mesh comprises: at least one second local ground wire that couples to the ground wire of the global power mesh; and at least one fourth power wire that couples to the second power wire and the second power domain.

218 patent at cl. 17. Realtek contends, as testified by Dr. Souri, that the claim is met in all Accused Products because:

[T]he second PLPM of each Accused Product comprises a ground wire (marked in yellow with a yellow arrow) on layer [redacted] or layer [redacted].

. . . .

[redacted]

> each Accused Product includes a second PLPM that comprises a fourth power wire (VDD2 marked in blue with a red arrow) on layer [redacted] or layer [redacted] that couples by via (marked by black arrows and red rectangles) to the second power wire (marked in red with a red arrow) on layer [redacted] or [redacted].
>
> . . . .
>
> the fourth power wire (VDD2, marked in red) of each Accused Product also couples to the second power domain.

CIB at 188, 193, 198; Hr'g Tr. (Souri) at 439:6-442:5, 465:17-24, 470:10-16, 477:18-24, 482:24-483:6, 488:3-10, 493:11-19, 498:18-21. AMD does not dispute infringement of claim 17 apart from its dependency on claim 12. RIB at 152; RRB at 58-59. In light of the cited evidence and opinion, the additional elements of claim 17 are met in the Accused Products, and the claim is therefore infringed based on infringement of claims 12, 15, and 16.

6. Claim 18

For reference, claim 18 of the 218 patent requires:

> 18. The power routing structure according to claim 17, wherein the first local ground wire and the second local ground wire share the same ground wire of the global power mesh.

218 patent at cl. 18. Realtek contends, as testified by Dr. Souri, that the claim is met in all Accused Products because "[t]he first local ground wire (*see* claim 16) (marked in yellow by yellow arrow on layer [redacted] and [redacted]) and the second local ground wire (*see* claim 17) (marked in yellow by yellow wire on layer [redacted] and [redacted]),"and "the shared ground wire of the global power mesh (on [redacted] or [redacted])." CIB at 203, 211; Hr'g Tr. (Souri) at 442:6-443:22, 466:2-23, 470:19-23, 478:2-5, 483:9-13, 488:13-17, 493:22-494:1, 499:5-8. AMD does not dispute infringement of claim 18 apart from its dependency on claim 12. RIB at 152; RRB at 58-59. In light of the cited evidence and opinion, the additional elements of claim 18 are met in the Accused

Products, and the claim is therefore infringed based on infringement of claim 12 and the intervening dependent claims.

E. Domestic Industry – Technical Prong

According to Realtek's post-hearing briefing, the DI Products practice claims 12, 13, and 15-18 of the 218 patent. CIB at 218. For the reasons discussed below, Realtek has shown by a preponderance of the evidence that the DI Products practice these claims.

1. Claim 12

Claim 12 of the 218 patent is presented above in connection with infringement. To show practice by the DI Products, Realtek contends through the testimony of Dr. Souri and a series of demonstratives that:

> *Element 12[pre]*. . . . both DI Products meet the preamble because they include a power routing structure routing power applied in an integrated circuit having at least two power domains.
>
> . . . .
>
> *Element 12[a]-12[b]*. . . . As Dr. Souri explained, each DI Product includes a first and second PLPM, including a network or plurality of wires capable of distributing power: the first PLPM includes a plurality of metal wires capable of distributing VDD1 power (and ground wires) and the second PLPM includes a plurality of metal wires capable of distributing VDD2 power (and ground wires). . . . Each PLPM also includes two sets of parallel conductive metal wires that have overlapping intersections and form a net or web-like structure (if that is required). . . . Dr. Souri confirmed, through his trace-down analysis, that there are two power domains in each DI product that include portions of the integrated circuit in the SDLs that receive power from different power pads and, therefore, have different power requirements from one another. . . . the first and second PLPMs (on [redacted]) are each physically positioned above, overlap, and can couple to the respective power domain [redacted] . . . Dr. Souri explained that the PLPMs and their respective power domains overlap. . . . Dr. Souri also explained that each PLPM and the respective power domain are positioned in such a way and can—and in fact do—couple by vias dropping down through the metal layers. . . . As confirmed by trace-down, the first and second PLPM "coupl[e] to" the respective power domain (or portions of the power domain).
>
> . . . .

[redacted]

> *Element 12[c]*. . . . Each DI Product includes a global power mesh on the top two metal layers of each DI Product ([redacted]). . . . Each metal layer of the global power mesh includes a plurality or network of conductive metal wiring capable of distributing power to multiple power domains (VDD1 and VDD2). *Id*. The wiring and vias allow each DI Product's global power mesh to distribute power from the relevant power pads to corresponding power domains. . . . Although not necessary (*see supra* at IV.A.1-4), when both metal layers identified for the global power mesh for each DI Product are viewed from above, the wiring of these metal layers form overlapping "intersections" and a "net-like" or "web-like" structure. . . . The undisputed evidence shows that global power mesh in each DI Product couples to the first partial local power mesh and the second partial local power mesh through separate vias as Dr. Souri explained in his trace-down analysis from the power pads in the global power mesh. . . . [E]ach Accused Product has a wiring structure in the global power mesh such that power from two different power pads (VDD1 and VDD2) is provided two different power domains, through distinct wires and via paths.
>
> . . . .
>
> *Element 12[d]*. . . . For both products, the PLPMs are on [redacted] and the global power mesh is on [redacted]. . . . [redacted] are different metal layers than [redacted], and all layers are [redacted] and have a different wiring structure as Dr. Souri testified.
>
> . . . .
>
> *Element 12[e]*. . . . As Dr. Souri testified, the DI Products include vertical power supply wires on the first layer of the global power mesh ([redacted] and vertical power supply wires on the second layer of the global power mesh ([redacted]
>
> . . . .
>
> Element 12[f]. . . . Each [DI] Product meets this limitation because the first and second metal layers are different metal layers as shown in the layout files and design rules.

CIB at 218-252 (citing, *inter alia*, Hr'g Tr. (Souri) at 503:5-508:10, 523:7-541:13, 541:16-561:6; CX-1995C-CX-1997C; JX-0023C (Seahra); JX-0024C (Seahra); JX-0029C-JX-0030C; JX-0768C-JX-0770C; CPX-0683C(SC); CPX-0684C(SC); CPX-0062C(SC)-CPX-0188C(SC)). The DI Products practice the limitations of claim 12 as alleged in view of the testimony of Dr. Souri.

[redacted]

AMD raises several challenges, but none are persuasive. As with infringement, AMD argues that Realtek fails to show partial local power meshes with the "same size and shape" as the power domains to which they couple. RIB at 154-155; RRB at 60. This is based on a faulty claim construction as determined above. Similarly, AMD argues the identified global power mesh fails to have all of its horizontal wires in one layer and all of its vertical layers in a different layer. RIB at 155-156; RRB at 60. This too is based on an incorrect claim construction, rejected above. AMD further argues, for the BCM4389 specifically, that "Dr. Souri's opinions regarding the global power mesh in the BCM4389 contradict [his] opinions regarding partial local power meshes." RIB at 152. This too was raised in the context of infringement and is not persuasive. To consider a collection of wires providing two levels of power as a single global mesh or two partial local meshes comes is a flexibility stemming from the 218 patent itself.

Finally, for the BCM4387 product, AMD complains that first and second "partial local power meshes" have not been shown because "Realtek's demonstrative allegedly showing these two meshes also shows [redacted] as in the green boxes below:

[redacted]

[redacted]

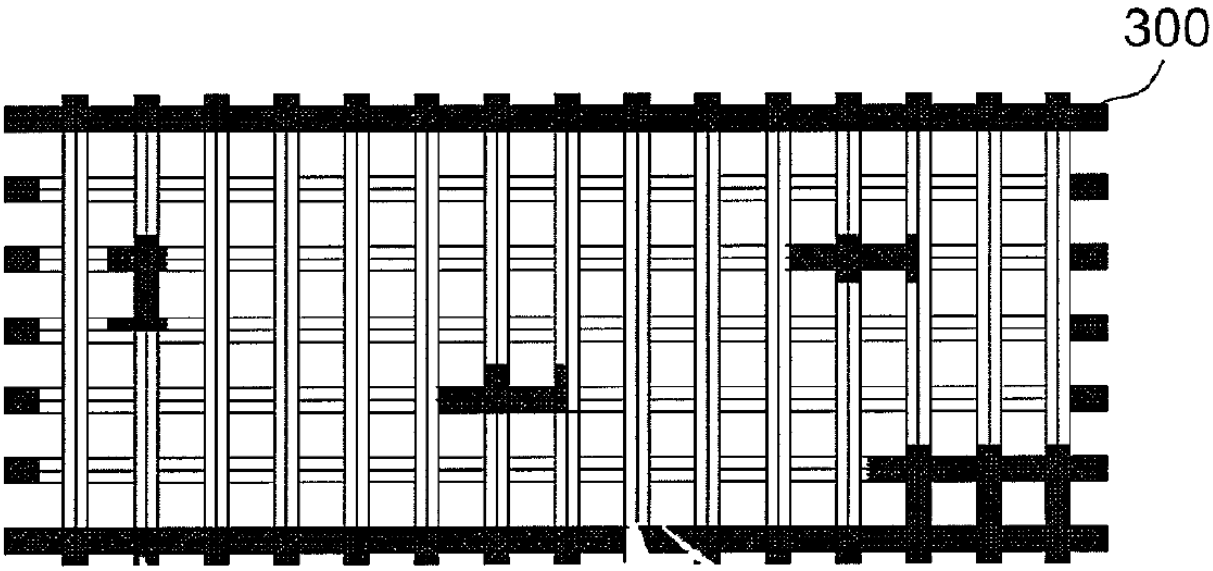
[redacted]

[redacted]

See RIB at 153-154; RDX-0002C.93. Realtek reasonably argues, however, that partial local power meshes are not defined by the box-like boundaries drawn by Dr. Souri but rather "the wires that

[redacted]

comprise it." CIB at 227 (citing Hr'g Tr. (Souri) at 525:5-15, 410:210-411:23; 218 patent at 3:56-64). This view is strongly supported by the black and white color scheme attributed to each partial local mesh as in Figure 5 of the 218 patent:



218 patent at Fig. 5. And Dr. Souri offered undisputed testimony that red wires and blue wires of the [redacted] layers in the BCM4387 product (show in the imagery above) carry different voltages—the attribute which differentiates the meshes. Hr'g Tr. (Souri) at 523:22-524:13; 218 patent at 3:45-49 ("It should be noted that the partial local power meshes 310, 320 are not interconnected (which means that the partial local power meshes 310, 320 are mutually insulated) to avoid mutual short-circuit that induces electrical uncertainty.").

Accordingly, the DI Products have been shown to practice claim 12.

2. Claim 13

Claim 13 of the 218 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Souri, that the claim is met in the DI Products because "the partial local power meshes are [redacted] and the global power mesh is on [redacted] and the [redacted] layers are above [redacted]." CIB at 252; Hr'g Tr. (Souri) at 506:16-18, 544:4-7.

AMD does not dispute practice of claim 13 apart from its dependency on claim 12. RIB at 156; RRB at 59-60. In light of the cited evidence and opinion, the additional elements of claim 13 are met in the DI Products, and the claim is therefore practiced.

3. Claim 15

Claim 15 of the 218 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Souri, that the claim is met in the DI Products because "each DI Product has a global power mesh that comprises at least one ground wire," "the global power mesh of each DI Product also includes a first, VDD1 power wire," "[t]he first power wire of each DI Product is connected to the power pad/supply providing power to the first power domain through the VDD1 wiring (marked in blue) by vias to the first power domain," "the global power mesh of each DI Product also includes a second, VDD2 power wire," "the second power wire (marked by red arrow and annotations) of each DI Product is connected to the power pad/supply providing power to the second power domain through the VDD2 wiring (annotated in red) by vias to the second power domain." CIB at 252, 254-257; Hr'g Tr. (Souri) at 506:21-23, 536:2-21, 544:10-16, 556:6-14. AMD does not dispute practice of claim 15 apart from its dependency on claim 12. RIB at 156; RRB at 59-60. In light of the cited evidence and opinion, the additional elements of claim 15 are met in the DI Products, and the claim is therefore practiced.

4. Claim 16

Claim 16 of the 218 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Souri, that the claim is met in the DI Products because "the first PLPM of each DI Product comprises a first local ground wire (marked by yellow arrow on [redacted] that couples through vias (marked by black arrows and yellow rectangles) to the ground wire of the global power mesh (marked by yellow arrow on layer [redacted] "the first PLPM of each DI Product comprises a third power wire (VDD1) (marked in blue with blue arrows) on layer [redacted] that couples

by via (marked by black arrows and blue rectangles) to the first power wire (on layer and "the first PLPM of each DI Product comprises a third power wire (VDD1) (marked in blue with blue arrows) on layer that couples by via (marked by black arrows and blue rectangles) to the first power wire (on layer CIB at 258, 260, 262; Hr'g Tr. (Souri) at 507:1-3, 537:6-538:19, 544:19-545:1, 557:6-558:17. AMD does not dispute practice of claim 16 apart from its dependency on claim 12. RIB at 156; RRB at 59-60. In light of the cited evidence and opinion, the additional elements of claim 16 are met in the DI Products, and the claim is therefore practiced.

5. Claim 17

Claim 17 of the 218 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Souri, that the claim is met in the DI Products because "the second PLPM of each DI Product comprises a ground wire (marked in yellow with a yellow arrow) on layer "each DI Product includes a second PLPM that comprises a fourth power wire (VDD2 marked in blue with a red arrow) on layer that couples by via (marked by black arrows and red rectangles) to the second power wire (marked in red with a red arrow) on layer and "the fourth power wire (VDD2, marked in red) of each DI Product also couples to the second power domain." CIB at 264, 265, 267; Hr'g Tr. (Souri) at 507:6-8, 538:21-540:12, 545:4-10, 558:18-560:12. AMD does not dispute practice of claim 17 apart from its dependency on claim 12. RIB at 156; RRB at 59-60. In light of the cited evidence and opinion, the additional elements of claim 17 are met in the DI Products, and the claim is therefore practiced.

6. Claim 18

Claim 18 of the 218 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Souri, that the claim is met in the DI Products because "[t]he first local ground wire (marked in yellow-by-yellow arrow on layer and the second local ground wire (marked in yellow-by-yellow wire on layer and "[t]he shared ground wire of the global

[redacted]

power mesh (marked in yellow with yellow arrows) is shown below. *Id.* The location of coupling by via (directly or indirectly) to the shared ground wire are marked by black arrows and yellow rectangles." CIB at 269, 271; Hr'g Tr. (Souri) at 507:11-15, 540:16-541:13, 545:17-20, 560:15-561:5; CDX-0003C.1439-1441, 1583-1585. AMD does not dispute practice of claim 18 apart from its dependency on claim 12. RIB at 156; RRB at 59-60. In light of the cited evidence and opinion, the additional elements of claim 18 are met in the DI Products, and the claim is therefore practiced.

F. Validity

AMD identifies the following invalidity theories for the 218 patent:

Claims	Theory
12, 13, 15-18	Rendered obvious under 35 U.S.C. § 103 by Jiang (JX-0042), Jiang2 (JX-0199), and Jiang3 (JX-0200) in view of Li (JX-0043) or Chiu (JX-0198)
12, 13, 15-18	Rendered obvious under 35 U.S.C. § 103 by Li (JX-0043) in view of Jiang (JX-0042)
12, 13, 15-18	Lack of written description under 35 U.S.C. § 112
12, 13, 15-18	Lack of enablement under 35 U.S.C. § 112

See generally RIB at 156-186. AMD and Realtek agree that the effective filing date of the 218 patent is November 15, 2007, and, in contrast to the 245 patent, Realtek does not offer evidence of an invention date earlier than the filing date. RIB at 156; CIB at 272 n.3. AMD further contends, without opposition from Realtek, that all prior art references applied against the 218 patent "were published and publicly available, patented, or filed prior to" this date and thus qualify as prior art under pre-AIA 35 U.S.C. § 102(a), (b), or (e). RIB at 156 (citing Hr'g Tr. (Subramanian) at 938:3-941:14); *see generally* CIB at 272-288; CRB at 47-56.

AMD is mostly correct. Jiang was published in a 2005 issue of the IEEE International Conference on Computer Design. JX-0042. Jiang2 was published in 2006. JX-0199. Li was also published in 2006 (JX-0043) and Chiu is an issued U.S. Patent with a listed priority date of September 28, 2007 (JX-0198). Although not outright stated by AMD, this is enough to conclude that Jiang qualifies under subsection (b), Jiang2 and Li qualify under at least subsection (a), and Chiu under subsection (e).

Beyond its blanket assertion of prior art status, however, AMD has not explained why Jiang3 qualifies as prior art. *See* RIB at 7-24, 156; RRB at 61-65; *see also* RPB at 123, 126-128. On its face, Jiang3 only notes a copyright date of 2007:

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AMD-ITC-1350-0190465

JX-0200. It is possible the "-7/07" refers to July of 2007, but without elaboration, it is difficult to find by clear and convincing evidence that Jiang3 is prior art to the 218 patent's November 15, 2007 priority date—even if not explicitly disputed by Realtek. *Microsoft*, 564 U.S. at 95.

Accordingly, each of Jiang (JX-0042), Jiang2 (JX-0199), Li (JX-0043), and Chiu (JX-0198) are prior art under 35 U.S.C. § 102 (pre-AIA); but not Jiang3, so it is not considered for purposes of invalidity in this investigation.

1. Jiang

Jiang is a research paper entitled "Benefits and Costs of Power-Gating Technique." JX-0042.1. It discloses a comparison between two power supply mesh systems for an integrated circuit; one in which power is continuously connected to all "macros" of the circuit and one in which power is gated to each macro of the circuit through "sleep-transistors":

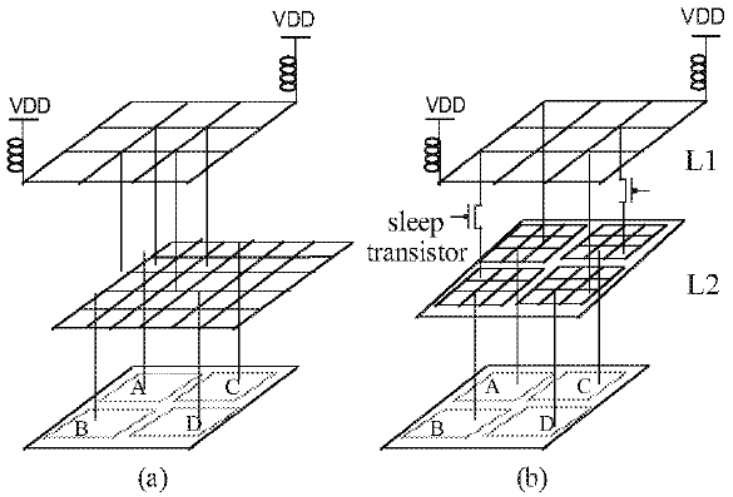


Figure 1. Power supply system (a) normal power supply system (b) power-gating system

JX-0042 at Fig. 1. The article considers power consumption and leakage, among other measurable characteristics, explains its modeling method, and presents additional experimental setups (sleep-transistor size, decoupling capacitor insertion, power mesh granularity, etc.). *See generally id.* Jiang concludes, "by compromising the 4% of total area and 5% of the dynamic power, we can reduce leakage power by 47% while keeping the same performance." *Id.* at .0008. AMD contends the asserted claims of the 218 patent are invalid as obvious over Jiang and other prior art. *See generally* RIB at 156-172. For the reasons discussed below, AMD has shown claims 12 and 13 to be obvious over Jiang, but no others.

a. Claim 12

Claim 12 of the 218 patent is presented above in connection with infringement. In support of its obviousness theory, AMD contends:

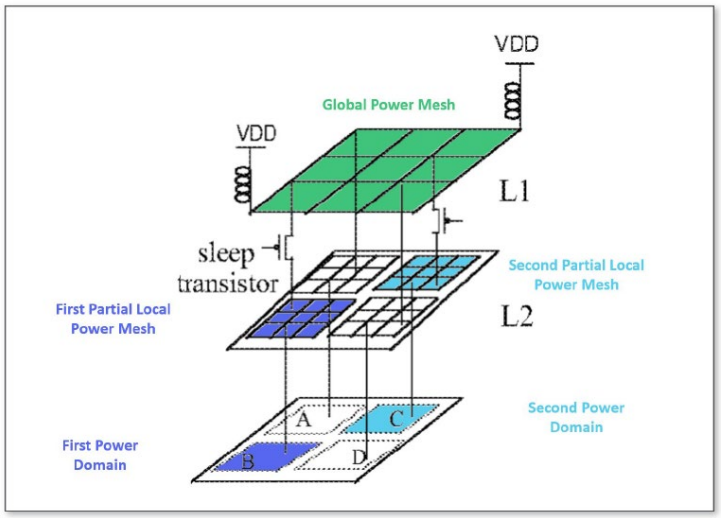
> The preamble of claim 12 is not a limitation. *See* JX-0029C (Souri) at 30:7-15. Regardless, Jiang discloses it. Tr. (Subramanian) at 942:17-943:9; RDX-0002.31; JX-0042.1 ("In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh."). . . . As Dr. Subramanian explained, a POSITA would have understood that Jiang's macros A, B, C, and D are power domains. Tr. (Subramanian) at 944:11-945:12; RDX-0002.32-35. Indeed, Jiang2 and Jiang3 confirm that the Jiang "macros" are

[redacted]

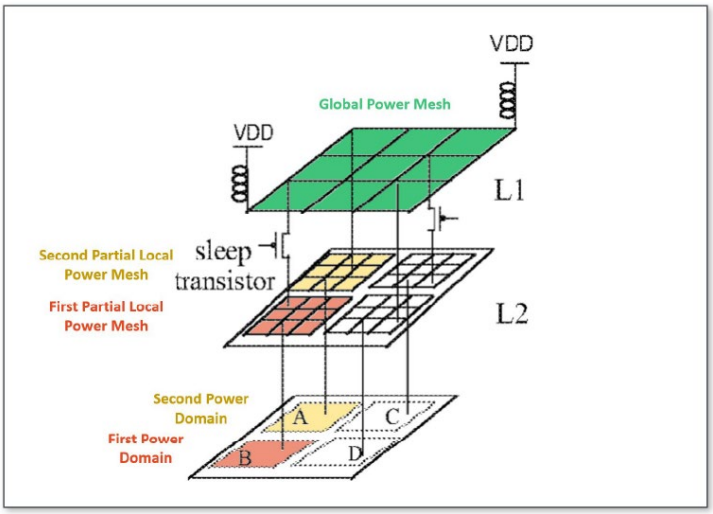
"power domains." Jiang2 describes "divid[ing]" the circuit "into several power domains" where "[e]ach domain is independently controlled by a sleep-transistor." JX-0199.1. Jiang2 describes these same portions of the circuit as "macros." JX-0199.2 ("the sleep transistor … must be sufficient to guarantee that the current drawn by a macro does not cause an excessive voltage drop on a sleep transistor which is turned on…. [I]n the power-gating system, the gated macros are disconnected from the power supply in their idle state ….").

. . . .

Jiang discloses the first and second partial local meshes recited in claim 12. Tr. (Subramanian) at 943:10-944:10. As shown in the annotated versions of figure 1(b), a POSITA would have understood that any of macros A, B, C, and D could be one of the recited power domains. *Id.* Jiang disclosed that there was one partial local power mesh for each macro. JX-0042.1 ("we have local power meshes for all macros …."). And a POSITA would further understand that each partial local power mesh has a position and shape corresponding to one of the macros. Tr. (Subramanian) at 943:10-944:10.



[redacted]



Jiang's "local power meshes" qualify as "power meshes" under any construction of that term. As shown above, the partial local power meshes in Jiang have vertical power supply wires and horizontal power supply wires and thus constitute "two sets of parallel conductive metal wires that form a net or web-like structure" under AMD's construction. They also constitute a "network of wiring capable of distributing power" under Realtek's construction. And they also meet the ordinary meaning of "mesh" discussed in the *Markman* order: "a plurality of linear members extending in different directions creating intersections."

. . . .

Jiang discloses the global power mesh. Tr. (Subramanian) at 949:22-950:15; RDX-0002.39; JX-0042.1 ("In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the ***global mesh***."); JX-0042.2 (Figure 1(b)). Jiang discloses a global mesh that provides the power needed by the macros. *Id*. From Figure 1(b) and these teachings, a POSITA would have understood that Jiang's global power mesh provides power to macros separately because it has separate connections to each of the partial local power meshes, which are in turn connected to the macro power domains. Tr. (Subramanian) at 949:22-950:15; JX-0041.1-2. In particular, the ungated macros are connected to the global mesh through the partial local power meshes and the gated macros are connected to the global mesh through the partial local power meshes and the sleep transistors. *Id.*

. . . .

Jiang's "global mesh" qualifies as a "power mesh" under any proposed construction. As shown above, Jiang's global power mesh has vertical power supply wires and horizontal power supply wires and thus constitutes "two sets of parallel conductive metal wires that form a net or web-like structure" under AMD's construction. Those wires also constitute a "network of wiring capable of

[redacted]

distributing power" under Realtek's construction. And they also meet the ordinary meaning of "mesh" discussed in the *Markman* order, "a plurality of linear members extending in different directions creating intersections." Order No. 21 at 17.

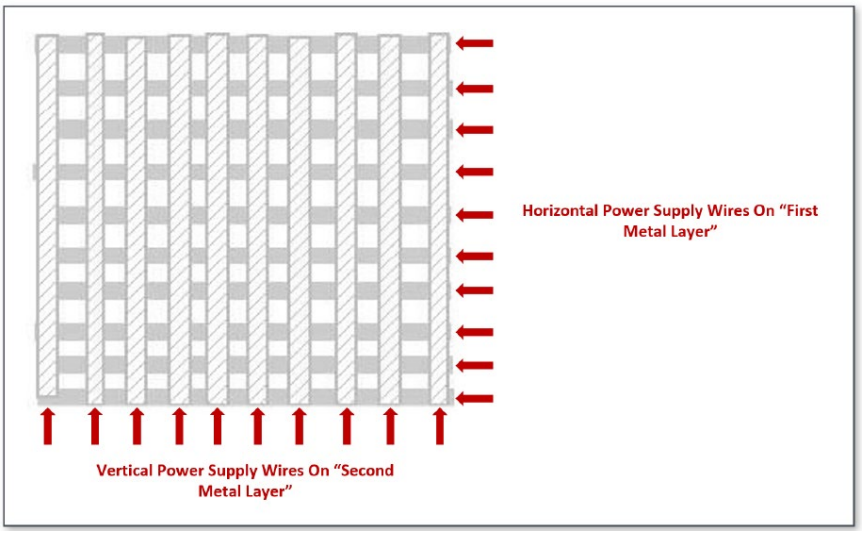
Jiang's "global mesh" also meets the ALJ's construction of "global power mesh" because it is "capable of distributing power to multiple power domains." As discussed above, Jiang teaches a global power mesh that provides the "power needed" by the macro power domains, even when the "power needed" is no power. As a result, a POSITA would understand that Jiang's global power mesh distributes power to multiple power domains under the ALJ's construction of "global power mesh."

. . . .

Jiang discloses the fourth limitation of claim 12 requiring the global power mesh and partial local power meshes to be on different layers. Tr. (Subramanian) at 950:16-951:6; RDX-0002.40. Jiang discloses this because it describes its global mesh as "[t]he upper power mesh" and its local meshes as "[t]he lower power mesh." JX-0042.2.

. . . .

Jiang discloses or would have rendered obvious that the global mesh includes a plurality of horizontal wires on one layer and a plurality of vertical wires on a different layer as recited in the last two limitations of claim 12. Tr. (Subramanian) at 951:7-953:5; RDX-0002.41. As annotated figure 10 shows, Jiang shows the standard way of drawing a plurality of horizontal wires on one layer overlapped by and a plurality of vertical wires on a higher layer. *Id.*



> Even if it is found that Jiang's Figure 1(b) and Figure 10 are unrelated, it would have been obvious to implement Jiang's teaching of a global mesh with a plurality of horizontal wires on one layer and a plurality of vertical wires on another layer because this was an "extremely common" way of implementing power meshes that would have been well within a POSITA's knowledge. Tr. (Subramanian) at 953:1-955:6. Such arrangements are shown in many prior art references, such as Ran, Li, Chiu, Blisson, and Longway. *Id.*; RDX-0002.42-45; JX-0300.2 (Figure 3(a)); JX-0043.5 (Figure 3); JX-0198.6 (Figure 7); JX-0039 [8:57-58]; JX-0044 [9:17-23].

RIB at 156-167 (citing, *inter alia*, RDX-0002.32-33, 41). AMD has persuasively shown the obviousness of claim 12 as alleged.

Realtek unsuccessfully opposes on a number of grounds. First, Realtek states, "Dr. Subramanian fails to show that Jiang, Jiang2, or Jiang3 discloses 'power domains' as the term is used in the patent." CIB at 273. Realtek finds Jiang's "macros" "are collections of cells" and there is "no expert analysis explaining how a collection of cells (or any disclosure in Jiang2 or Jiang3) is a 'power domain' as the term is used in the patent." *Id.* at 273-274 (citing, *inter alia*, JX-0029C). To the contrary, there is no expert analysis supporting Realtek's view of macros. The cited testimony (JX-0029C) comes from Dr. Souri's deposition and not the evidentiary hearing. It is therefore not substantive evidence and is not considered.

And given the determination above, that "power domain" means "a portion of an integrated circuit whose elements have the same power requirement," the macros in Jiang and/or Jiang2 meet the definition. Jiang states:

> Power-gating is a technique for reducing leakage power by shutting off the idle blocks.
>
> . . . .
>
> The entire chip is fully powered at all times. In the power-gated chip, we have local power meshes for all macros, and sleep transistors are used to connect the local mesh to the global mesh.

When a macro is active, the sleep transistor is turned on. Its size must be large enough to guarantee that the current drawn by the macro does not cause excessive voltage drop.

. . . .

In a chip without power-gating, the non-switching part of the circuit serves as a decoupling capacitor and reduces the power grid noise. However, in the power-gated hip, the gated macros are disconnected from the power supply during their idle state, which prevents them from acting as a decap for the active circuit.

. . . .

The purpose of power-gating is to save leakage power when blocks are idle.

JX-0042.1-3. And Jiang discloses one experimental setup as an IC consisting of twenty-six "basic logic blocks" with some gated and some non-gated:

4. Experiments

We implement 26 circuits (from MCNC and ISCAS benchmarks respectively) as the basic logic blocks. The initial floorplan of those blocks is shown as in Fig.7.

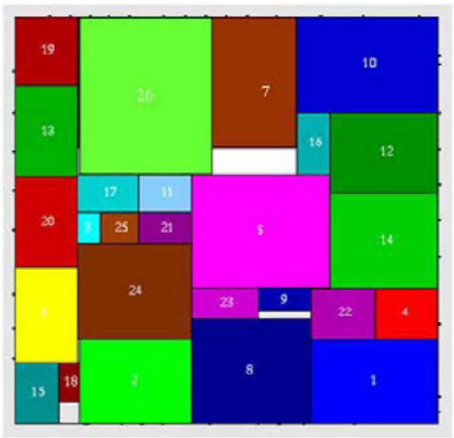


Figure 7. Floorplan of 26 circuits(1x0.9mm^2)

. . . .

In this experiment, we gated half of the circuits (blocks whose geometric centers were on the left half of the chip) and compared it with non-power-gated chip in terms of power and area.

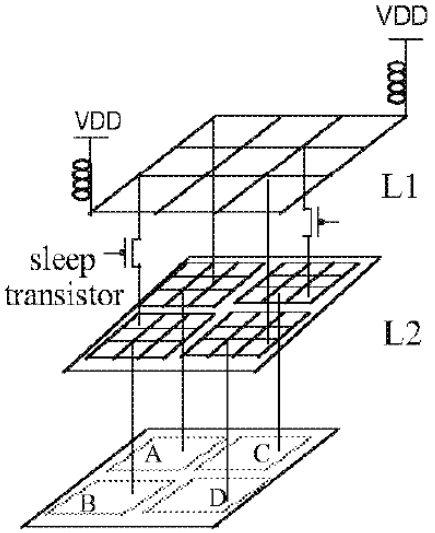
Id. at .0006. Altogether, the disclosure of IC logic "blocks" which consume power and are turned on or off (active or idle) as a single unit is a clear and convincing disclosure of "a portion of an integrated circuit whose elements have the same power requirement" and is entirely consistent with the 218 patent's own "sleep mode" embodiment. Moreover, AMD rightfully points to Jiang2, a follow-on report to Jiang by the same authors, which even more clearly associates macros with power domains:

> Traditionally, the on-chip power distribution is constructed hierarchically. Power is delivered from the top-level metal layer (which is connected to the package), down through the internal layers, and finally to the active device. The entire chip is fully powered at all times. In a power-gating system, a circuit is divided into several power domains. Each domain is independently controlled by a sleep-transistor. The sleep transistors are turned off to reduce the dynamic power and leakage power in a standby mode, and turned on in an active mode for normal operation.

JX-0199.1; *see* RIB at 158. Altogether, the limitation is taught in Jiang. No consideration of modifications to Jiang, obvious or nonobvious in light of other prior art, is necessary.

Next, Realtek argues Jiang does not include limitation [12c], a "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately." CIB at 276-277. Realtek reasons, "Jiang Figure 1(b) does not include separate wiring paths in the global power mesh, and, as Dr. Souri showed, in contrast to the patent [], Jiang only discloses interconnected wires. . . . As a result, the purported global power mesh of Jiang Figure 1(b) does not and cannot provide power separately." *Id.* at 276. This is incorrect. As shown, Jiang's global mesh couples to partial local meshes (which are insulated from each other) which then couple to their respective power domains (also insulated from each other) in a vertical stack. JX-0042 at Fig. 1(b). The fact that the wires of the global mesh are shown as completely interconnected, making them only able to deliver one power level at a time, is only relevant if "power domains" are required to have different power

requirements from one another (multiple wire sets would be needed for multiple power supplies). This construction was rejected above, however, and the claim permits the first and second power domains having the same power requirement as one another. As it stands, when all four macros in the embodiment of Figure 1(b) are active, each is a power domain, and they receive the power they need from four partial local meshes through four separate vias, and those partial local meshes receive their power through four vias as well:



(b)

JX-0042.2. The limitation is met.

Lastly, Realtek challenges limitations [12e] and [12f] concerning the wires of the "global mesh." Realtek contends, "[t]he purported 'global power mesh' is disclosed as a single interconnected layer on 'L1' of Figure 1(b). . . . A POSITA would understand that L1 is one layer because there is no reason to have two layers to distribute one VDD." CIB at 277. Realtek appears to acknowledge that Figure 10 of Jiang shows the horizontal and vertical wire layer arrangement required by the limitations, but argues "as Dr. Souri explained, Figure 10 is a different embodiment and relates to the model of Figure 2." *Id.* (citing Hr'g Tr. (Souri) at 1287:9-1288:23); CRB at 51 ("AMD cites nothing from Jiang to suggest Figure 10 and Figure 1(b) are related."). As to whether

it would have nonetheless been obvious to implement Figure 10 into the embodiment of Figure 1(b), Realtek views AMD as failing to provide a sufficient motivation. CIB at 278 (citing *Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017)); CRB at 51 ("that two-layer power meshes were 'known' [] is legally insufficient").

The limitations are obvious. Realtek is correct in that Jiang fails to explicitly teach that the horizontal and vertical wire layer shown in Figure 10 applies to the upper, global, power mesh shown in Figure 1(b). It refers only to "the power mesh" as having such structure (JX-0042.7); and Realtek fairly posits that "there is no reason to have two layers to distribute one VDD" which is the only voltage level any mesh within Jiang uses (CIB at 277).

And yet, despite there being no apparent need for a dual-layer power mesh, Jiang dedicates an entire section exactly to this and its impact on the experiment:

4. Gating-effect vs. power-mesh-granularity

In this experiment, we studied the impact of the power mesh granularity on power-gating result. We kept the area of power mesh constant and changed the width of horizontal and vertical segments. Fig.10 shows power meshes of various granularity. We used meshes of several granularities on the same gated system. Fig 11 shows the decap insertion results for such meshes. *MxN* stands for a mesh of m rows and n columns. The y-axis data is normalized to the ungated system. The stable curve implies that if we keep the power mesh area constant, the noise incurred by power-gating does not change much with mesh granularity.

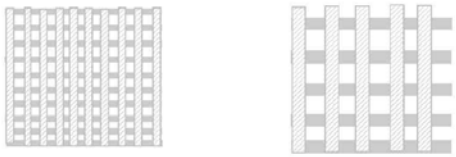


Figure 10. Power mesh granularity

[redacted]

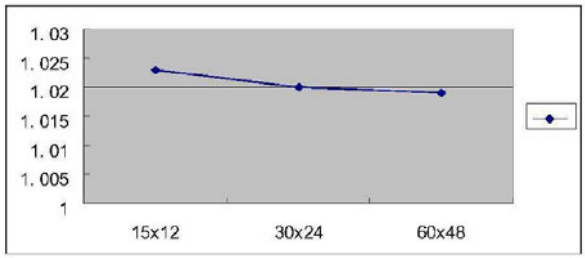


Figure 11. inserted decap

JX-0042.0007. This is in itself a motivation to make either of the upper (global) or lower (local) meshes with this structure, and distinguishes cases like *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.* relied on by Realtek. 694 F.3d at 1312, 1327-28 (Fed. Cir. 2012) (finding expert testimony conclusory due to generic motivations such as "build something better . . . more efficient, cheaper, or . . . had more features," etc.); *see* CRB at 51. And given that there are only two meshes to choose from, the obviousness case becomes even stronger as a matter of limited options. *KSR*, 550 U.S. at 421; *see Uber Techs, Inc. v. X One, Inc.*, 957 F.3d 1334, 1339-40 (Fed. Cir. 2020) (holding claims as obvious "because Okubo's terminal-side plotting and Konishi's server-side plotting were both well known in the art, and were the only two identified, predictable solutions for transmitting a map and plotting locations, it would have been obvious to substitute server-side plotting for terminal-side plotting in a combination of Okubo and Konishi.").

The tone of Jiang's Figure 10 discussion also coincides with Dr. Subramanian's generalized testimony that unidirectional wires on one level and perpendicular wires on another is "extremely common" and "the easiest way to do it." Hr'g Tr. (Subramanian) at 953:1-5. Tellingly, Dr. Souri does not opine that this was not standard in the industry, and neither does the 218 patent. That is, it would have been obvious to a skilled artisan to implement the two-layer structure depicted in Figure 10 in Jiang's top-level, global, mesh.

With that said, Realtek presents several indicia of non-obviousness. It argues the invention provides "lower cost and shorter time to market associated with reduced design times, a routing

structure that is convertible into an algorithm which can be readily developed into new automated placement and routing (APR) tools to further aid in design, and a more efficient use of chip real estate" which "are indisputably appreciated by the industry and end-product consumers of both the Accused and DI Products." CIB at 286 (citations omitted). Realtek adds, "[b]oth AMD and Broadcom have experienced significant commercial success after, and due to, the release of the Accused and DI Products, respectively," the same products "are also praised for the downstream benefits provided by the invention of the patent discussed above," and "[o]thers in the industry have also failed to achieve the benefits offered by the patent." *Id.* at 287 (citations omitted); CRB at 56.

None of Realtek's evidence bears any meaningful nexus to the question at hand, however, which is whether it would have been obvious to include vertical wires on one layer and horizontal wires on a different layer. Realtek cites hundreds of exhibits in its briefing but explores none of them beyond the general assertions quoted above. *See* CIB at 286-288; CRB at 56. At best, it has been shown that the DI Products—the BCM4387 and BCM4389—were adopted into successful consumer electronic devices and are regarded as low-power radio transceivers (*see, e.g.*, JX-0843), and that low power consumption and small die size are also targets of the accused AMD products (*see, e.g.*, JX-0847; JX-0012 (Gayle) at 49:1-22). That the 582 patent also concerns power supplies makes this evidence modestly relevant to the inquiry. But much of it also concerns the benefits of using an Automatic Placement and Routing tool as saving R&D time (*see, e.g.*, JX-0016C (Lin) at 59:5-61:9; Hr'g Tr. (Lin) at 45:22-47:12, 48:13-49:5; Hr'g Tr. (Souri) at 369:12-373:9), which is not germane. Realtek nonetheless argues that all of its evidence, no matter how high-level, has sufficient nexus to the claimed invention because "all that is required is 'a nexus between the *merits of the claimed invention* and the evidence of secondary considerations.'" CIB at 288 (citing

Simmons Fastener Corp. v. Illinois Tool Works, Inc., 739 F.2d 1573, 1575 (Fed. Cir. 1984) (emphasis by Realtek)). But this is not persuasive given the Federal Circuit's more recent holding that when the praise or success is based on technical features found in the prior art, it should be discounted. *ClassCo, Inc. v. Apple, Inc.*, 838 F.3d 1214, 1220 (Fed. Cir. 2016). Thus, Realtek's indicia of non-obviousness are accorded only minimal weight and do not overcome the other *Graham* factors, particularly the motivation to apply Jiang's two-layer structure to Jiang's own grids.

In sum, all four *Graham* factors either favor obviousness or are of minimal weight. The contents of Jiang and Jiang2 capture all claim features even if not arranged exactly as the claim limitation requires; the level of ordinary skill is suitable for the straightforward geometric concepts involved; and indicia of non-obviousness have only partial relevance. Accordingly, claim 12 has been shown to be obvious under 35 U.S.C. § 103 in light of Jiang and Jiang2, even without consideration of Li or Chiu.

b. Claim 13

Claim 13 adds the requirement that the global mesh be located above the first local power mesh. *See* 218 patent at cl. 13. This is shown in Figure 1(b) of Jiang. JX-0042 at Fig. 1(b); RIB at 167. Realtek does not dispute this disclosure, or offer any other evidence relevant to obviousness. *See* CIB at 278; CRB at 51. Accordingly, claim 13 has been shown to be obvious under 35 U.S.C. § 103 in light of Jiang and Jiang2.

c. Claims 15-18

Claim 15 requires the global mesh to have first and second power wires for powering the first and second domains, along with at least one ground wire. *See* 218 patent at cl. 15. Claims 16 and 17 require the first and second partial local power meshes to have the same components, respectively. *Id.* at cls. 16, 17. Claim 18 requires the two ground wires of the partial meshes to

"share the same ground wire of the global power mesh." *Id.* at cl. 18. There is no dispute that Jiang's Figure 1(b) shows the requisite power wires for each mesh. *See* RIB at 168 (citing RDX-0002.47); CIB at 278-281; CRB at 48-49; JX-0042 at Fig. 1(b). And AMD acknowledges that Jiang fails to disclose the ground wires. RIB at 168.

Nevertheless, AMD argues including a ground wire within the global power mesh and both partial local power meshes would have been obvious to a POSITA, based largely on the opinion of Dr. Subramanian:

> A POSITA would have known that "ground connections are necessary for such circuits to function." Tr. (Subramanian) at 959:18-960:3; *see* Tr. (Souri) at 1323:20-23 (delivering power requires ground connectivity). And it would have been obvious to a POSITA that this necessary ground was part of the power meshes recited in the claims because "that is the most obvious way and the most straightforward way to route ground down to the chip" and a POSITA would have had "a high expectation of success" in incorporating ground wires into Jiang's power meshes. Tr. (Subramanian) at 960:4-20.

RIB at 168; *see* RRB at 63. AMD further argues that the obviousness is shown "through multiple state of the art references depicting ground wires as part of power meshes, including Morton, Chan, and Schoellkopf." RIB at 168-169 (citing JX-0038; JX-0046; JX-0197).

Realtek largely contends that AMD has failed to explain motivation—"[j]ust because a ground wire was known to be part of a generic purported 'power mesh' is not sufficient to provide a motivation to modify to reach the claimed invention." CIB at 279 (citing *Pers. Web Techs., LLC v. Apple Inc.*, 848 F.3d 987, 991 (Fed. Cir. 2017); *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 668 F.3d 1342, 1369 (Fed. Cir. 2012)). Realtek points out the opinion of Dr. Souri, which is that Jiang's Figure 2 actually teaches grounding the circuit through the substrate (*id.* at 279-280 (citing Hr'g Tr. (Souri) at 1290:2-19), and this disclosure "would lead a POSITA to a different routing configuration tha[n] the claimed configuration" (*id.* at 280; CRB at 51).

AMD has not met its clear and convincing burden. Dr. Subramanian fails to present a clear and convincing motivation to include a connective series of ground wires in each mesh. His closest testimony is that this arrangement "is the most obvious way and the most straightforward way to route ground down to the chip." Hr'g Tr. (Subramanian) at 960:5-7. He repeats moments later, "[a]nd even if the ground wire is not explicitly shown in the power mesh, it would have been abundantly straightforward to do. In fact, it is the most obvious way to do it." *Id.* at 960:15-18. Yet calling the arrangement "straightforward" is synonymous with "obvious" and lacks any technical underpinning. Perhaps the technique requires little extra design consideration, is inexpensive, simplest to manufacture, or ensures greatest reliability as compared to other grounding methods—but Dr. Subramanian stops at simply showing ground wires exist. *See* RDX-0002.48-52; *see generally* JX-0038 at Figs. 2A-1, 2A-2, 2A-3, 2B; JX-0197 at 10:42-52; JX-0046 at [0035], Fig. 5. He does cite Chiu as an example of a mesh with vertical power wires and horizontal ground wires, but he fails to provide a motivation to combine that feature of Chiu with Jiang and/or Jiang2. *See* RDX-0002.52; RIB at 170. Courts have routinely emphasized motivation as a necessary showing for obviousness (*KSR*, 550 U.S. at 399) and it is missing here.

Accordingly, AMD has not shown that any of claims 15-18 are invalid for obviousness over Jiang, Jiang2, Li, and Chiu.

2. Li

Li is a research paper entitled "LVS Verification across Multiple Power Domains for a Quad-Core Microprocessor." JX-0043.1. The paper concerns a method of layout-versus-schematic ("LVS") verification which is intended to "verify that the layout matches the schematic . . . . which involves checking the consistency between the original schematic netlist and the one extracted from the layout." *Id.* at .0002. It notes certain difficulties in performing the

method on multi-core chips, such as the Broadcom BCM1280, due to the presence of multiple power/ground domains. *Id.* at .0003. The paper explains:

> In this quad-core microprocessor, four CPU cores are identical and each sits in a separate triple-well region. Each single core, isolated from the others by a triple-well, forms a separate processor region. Therefore, under the full-chip context, each core is now built in a unique voltage region. In addition to the complexity of the multiple ground domains, the chip is divided into two logic voltage regions (1.1V). The previous generation chip., from which BCM1280 is migrated, was designed with one power supply only.

Id. at .0002. The structure of the BCM1280 is described as follows:

> On the BCM1280, Metal-6 and metal-7 are extensively used in distributing power and ground across the chip. Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction. This forms the power grid structure at the chip top level. The power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level. The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level power grid, to implement a complete full-chip power distribution network.

. . . .

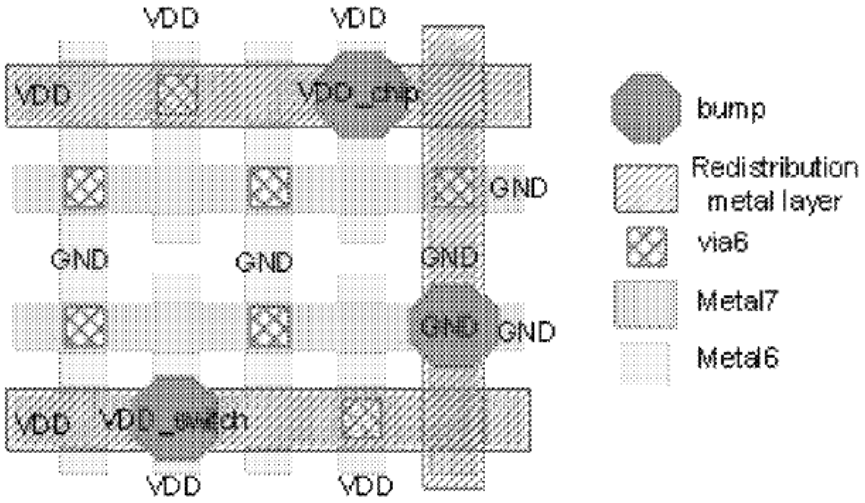


Fig. 3. Power and ground are distributed from the bumps onto the chip-level power grid through a redistribution metal layer.

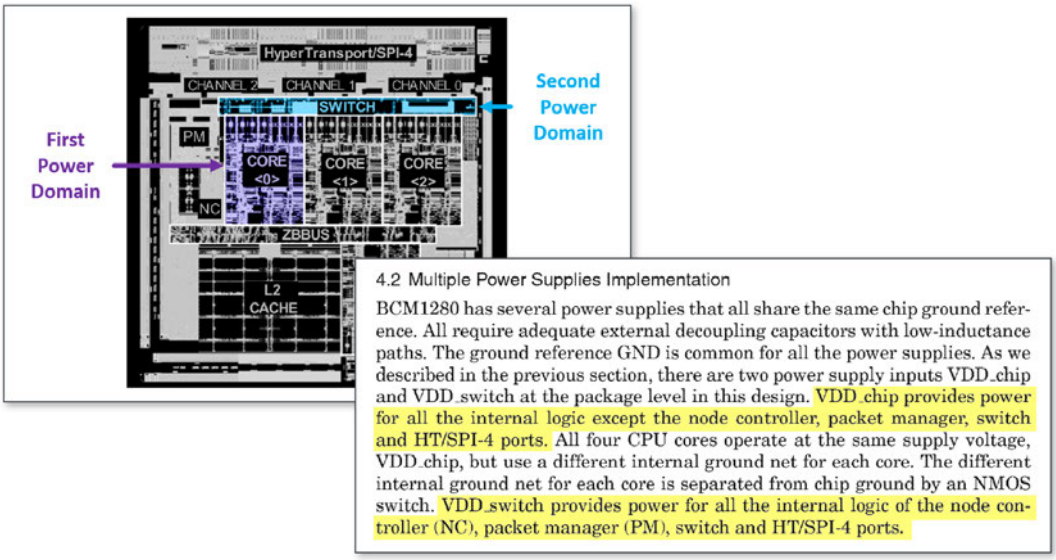
Id. at .0004. And it is noted that with the BCM1280, "[l]arge blocks of a chip can be disabled when they are not needed in order to save energy by reducing leakage current" (*id.* at .0003) and "for some applications where power consumption is a major concern, two of the four CPU cores and the correlated peripheral logic circuitry could be shut-off to achieve power efficiency" (*id.* at .0004). AMD contends the asserted claims of the 218 patent are invalid as obvious over Li and other prior art. *See generally* RIB at 172-181. For the reasons discussed below, AMD has shown claims 12, 13, and 15-18 to be obvious over Li.

a. Claim 12

Claim 12 of the 218 patent is presented above in connection with infringement. In support of its obviousness theory, AMD contends:

> Even if the preamble of claim 12 were a limitation, Li discloses it. Tr. (Subramanian) at 965:22-966:5; RDX-0002.56. Li describes a multi-layer power routing structure. JX-0043.4. This power routing structure is used to provide two different voltages ("VDD_chip" and "VDD_switch") to different chip areas. JX-0043.6. Further, the "CPU cores and [their] correlated peripheral logic circuitry could be shut-off to achieve power efficiency." JX-0043.4. Sections of a chip that receive different voltages and can be independently powered are different power domains under any proposed construction of that term. Tr. (Subramanian) at 965:22-966:5.
>
> . . . .
>
> Li discloses or, in combination with Jiang, at least renders obvious the first and second partial local meshes in claim 12. Tr. (Subramanian) at 966:6-969:9; RDX-0002.57-59. First, as discussed for the preamble, Li discloses at least two power domains. Each core receives the "VDD_chip" voltage and the "switch" circuitry receives power from the "VDD_switch" voltage. JX-0043.6 ("VDD_chip provides power for all the internal logic except the node controller, packet manager, switch and HT/SPI-4 ports"). As shown below, this makes each core region a separate power domain from the switch region. Tr. (Subramanian) at 966:6-967:6.

[redacted]



. . . .

Li also discloses partial local power meshes associated with each of the power domains. Tr. (Subramanian) at 967:7-968:3; RDX-0002.55, 57-58. Li teaches a plurality of "local power grids" in the "local sections" on metal layers 2-5. JX-0043.4; *see* Tr. (Souri) at 1296:19-22 (admitting that a POSITA would understand the local power grids are only in the local sections). These local power grids "are formed at the block level" and comprise "power and ground lines that are grided on Metal-2 through Metal-5." JX0043.4. . . . A POSITA would also have understood that each of Li's local grids would have their position corresponding to the position of the power domain to which they are coupled because Li discloses that the local grids are "at the block level." Tr. (Subramanian) at 968:4-9; JX-0043.4. And, even if it is found that Li did not disclose this, it would have been obvious in view of the combined teachings of Li and Jiang. Tr. (Subramanian) at 968:10-969:9. A POSITA would have been motivated to combine these teachings and would have had a high expectation of success in doing so "because it is essentially using the gridding architecture that is already talked about in Li and using the specific of Jiang to implement it." *Id.*

. . . .

Li discloses the global power mesh of claim 12. Tr. (Subramanian) at 969:10-971:3; RDX-0002.60. Li discloses a "top-level power grid" on metal layers 6-7 for "distributing power and ground across the chip," which constitutes a global power mesh. JX-0043.4. Li also discloses that "[t]he local power grids are left floating until final assembly [when] an in-house automated procedure … connect[s] local logic to the top-level power grid, to implement a complete full-chip power distribution network." *Id.* As discussed above, this disclosure necessarily includes connecting the local power grids to the top-level power grid and the local logic, otherwise, the local grids would remain "floating." Tr. (Subramanian) at 969:10-

[redacted]

> 970:21. Li thus describes coupling the first partial local power mesh and the second partial local power mesh to the global power mesh. *Id.* And, as discussed above, because different areas of the chip need different voltages, this coupling would provide the power needed by the first power domain and the second power domain "separately." *Id.* at 970:22-971:3.
>
> . . . .
>
> Li discloses or, in combination with Jiang, at least renders obvious the fourth element of claim 12 that requires the global power mesh and partial local power meshes to be on different layers. Tr. (Subramanian) at 971:4-972:6; RDX-0002.61-62. Li discloses that the "local power grids" are on the same metal layers ("Metal-2 through 5"), while the "top-level power grid" is on different metal layers ("Metal-6 and [M]etal-7"). JX-0043.4.
>
> . . . .
>
> Li discloses that the global mesh includes a plurality of horizontal wires on one layer and a plurality of vertical wires on a different layer as recited in the last two limitations. Tr. (Subramanian) at 972:7-21; RDX-0002.63. Li discloses that in the "top-level power grid," which is a global power mesh, "Ground (GND) and power (VDD_chip, VDD_switch) lines are routed alternately on Metal-6 in the vertical direction and Metal-7 in the horizontal direction." JX-0043.4. As shown below, this arrangement of horizontal and vertical power supply wires on the different "Metal-6" and "Metal-7" layers is shown in Figure 3.

RIB at 174-179. AMD has persuasively shown the obviousness of claim 12 as alleged.

Realtek opposes on a number of grounds. First, Realtek complains that "AMD fails to properly analyze the term 'power domain' because there is no analysis under the proposed claim constructions. . . . Thus, the testimony is too conclusory to be entitled to any weight." CIB at 281 (citing Hr'g Tr. (Subramanian) at 965:22-967:6). To the contrary, as AMD argues, "[s]ections of a chip that receive different voltages and can be independently powered are different power domains under any proposed construction of that term." RIB at 174. And as determined above, "power domain" is broad and simply means "a portion of an integrated circuit whose elements have the same power requirement"—a construction met by a portion of a chip that receives and is

[redacted]

powered by the same delivered voltage, as in the core (VDD_chip) and switch (VDD_switch) regions of Li. JX-0043.4.

Realtek next argues, "Li does not disclose any PLPM coupled to or having its position corresponding to any purported power domain." CIB at 281 (citing Hr'g Tr. (Souri) at 1294:5-1296:22). Realtek acknowledges Li's disclosure of "power and ground lines in the local sections are grided on Metal-2 through Metal-5, on which the local power grids are formed at the block level" but nevertheless argues, "Li does not disclose where the 'local sections' are and silence is not a disclosure." *Id.* Realtek explains, " 'block level' means that the local power grids are not at the full chip level. . . . A POSITA would also understand that "at block level" also does not change that the local power grids are "in the local sections." *Id.* at 282.

Li is not so silent, however. As noted above, Li uses the term "block" in several places including, "[l]arge blocks of a chip can be disabled when they are not needed in order to save energy by reducing leakage current." JX-0043.3. Li then gives the example of "two of the CPU cores and the correlated peripheral logic circuitry could be shut-off to achieve power efficiency." *Id.* at .0004. Thus, it is fair to infer that "block" corresponds to a logical block of chip circuitry; and then "local power grids are formed at the block level" strongly suggests those grids (*i.e.*, the PLPMs) are created in the region of the underlying logical circuitry. *See* RIB at 175 (citing Hr'g Tr. (Subramanian) at 968:4-9). This is why they are described as "local." This meets Realtek's broad construction for "having its position corresponding to" as adopted above.

Even if not clearly disclosed, placing Li's "local power grids" in a location so that they at least partially overlap the corresponding logic circuitry would have been obvious given Li's teachings and Figure 1 of Jiang which visually demonstrates the concept:

[redacted]

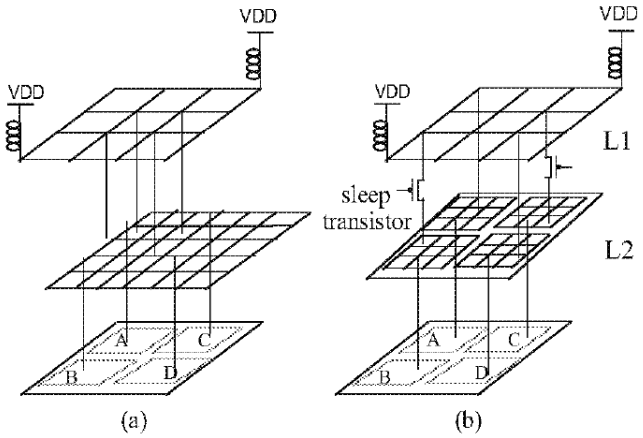


Figure 1. Power supply system (a) normal power supply system (b) power-gating system

JX-00042.2. As with the discussion of Jiang and limitations [12e] and [12f], above, the motivation to make this combination comes from Li itself—Li teaches a POSITA to form local power grids at the block level. *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023) (holding a claim obvious in light of a prior art reference that disclosed by itself the known benefit for the feature it provided to the combination); *Uber Techs.*, 957 F.3d at 1341 ("Rather, the question is 'whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole.'") (internal citation omitted); *see also Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) ("anticipation is the epitome of obviousness") (internal citation omitted).

Realtek opposes, urging that "Li teaches away from the proposed combination by disclosing a direct connection from the top metal layers down to the logic to provide power." CIB at 282 (citing JX-0043.4; Hr'g Tr. (Souri) at 1297:19-1298:13); *see id.* at 283 ("Li is silent as to whether the global power mesh is coupled to a local power grid in the claimed location (and whether a local power grid is coupled to its power domain). Li actually discloses the opposite—connections between the circuitry and the top level."). The teaching actually reads: "The local power grids are left floating until final assembly at the full-chip level. At the final stage of the layout design, an in-house automated procedure is applied, connecting local logic to the top-level

power grid, to implement a complete full-chip power distribution network." JX-0043.4. This passage is preceded by a discussion of Metal-6 and metal-7 layers forming "the chip top level" and then Metal-2 through Metal-5 layers forming the local grids "at the block level." *Id.* A fair reading of the entire passage is that the local power grids are in place but unconnected to both the Metal-6/7 layers and the local logic until "the final stage of the layout design," whereupon the local grids are so connected "to implement a complete full-chip power distribution network." *See* RRB at 67 (citing Hr'g Tr. (Subramanian) at 966:6-968:9). Realtek's interpretation, that the local power grids are somehow skipped over and deliver no power to the underlying local logic circuits is unreasonable. Realtek mischaracterizes the reference and in any event there is no teaching away. *In re Urbanski*, 809 F.3d 1237, 1244 (Fed. Cir. 2016) (finding no teaching away when prior art did not "criticize or discredit" the combined feature).

Realtek also argues, "[a] POSITA would not be motivated to combine Li and Jiang because their designs are incompatible and would create redundancies requiring a redesign." CIB at 282. Realtek continues, "[f]or example, Jiang discloses PMOS power switches and Jiang discloses NMOS ground switches. . . . A POSITA would not use two different switches to perform the same switching because it takes up valuable silicon space for no reason." *Id.* (citing Hr'g Tr. (Souri) at 1298:14-1301:4). Yet the pertinent combination (placing a local power grid above corresponding local logic circuitry) has nothing to do with switches. *See* RIB at 160 (citing *Uber Techs*, 957 F.3d at 1341 (finding it immaterial that one reference disclosed a limitation while the other did not, because the combination would include the limitation); *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) ("[T]he criterion being not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole."); *but see* CRB at 54 (citing *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988) ("One cannot use hindsight

reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1331–32 (Fed. Cir. 2019) ("That is consistent with the longstanding principle that the prior art must be considered for all its teachings, not selectively."). As far as indicia of non-obviousness, Realtek presents the same argument for Li as for Jiang, and that body of evidence only minimally favors Realtek, as explained above.

In sum, the *Graham* factors favor obviousness here. The content of Li viewed in light of Jiang captures all claim features; the level of ordinary skill is suitable for the concepts involved; and indicia of non-obviousness have only partial relevance at best. Accordingly, claim 12 has been shown to be obvious under 35 U.S.C. § 103 over Li in light of Jiang.

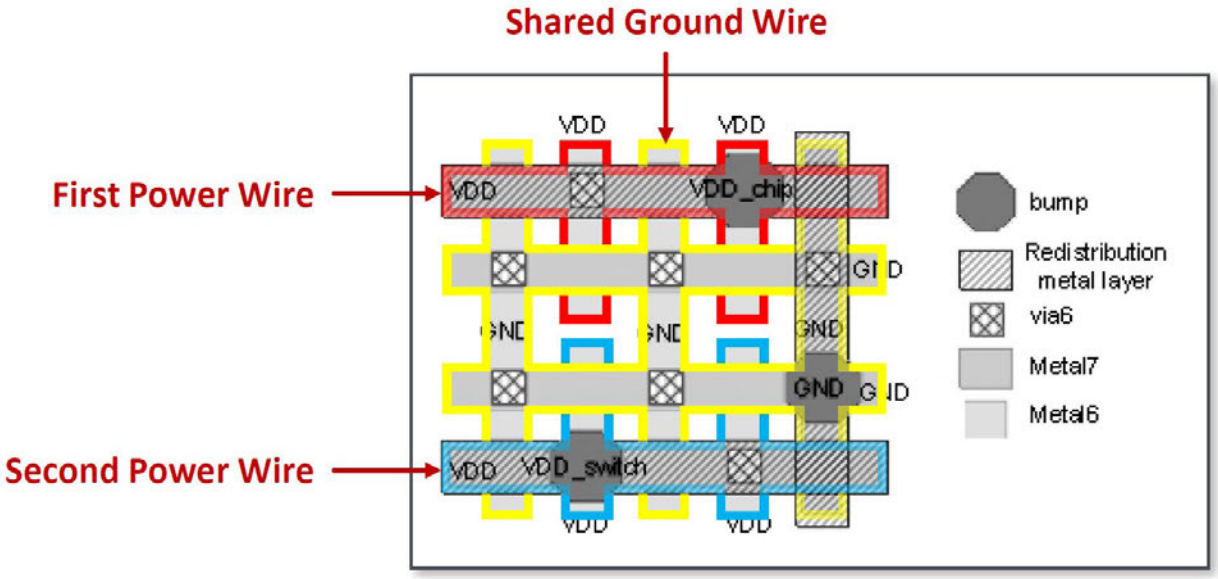
b. Claim 13

Claim 13 adds the requirement that the global mesh be located above the first local power mesh. *See* 218 patent at cl. 13. This is described in Li. JX-0043.4, Fig. 3; RIB at 179. Realtek does not dispute this disclosure. *See* CIB at 283 (discussing only claims 15-18); CRB at 55-56 (same). Accordingly, claim 13 has been shown to be obvious under 35 U.S.C. § 103 over Li in light of Jiang.

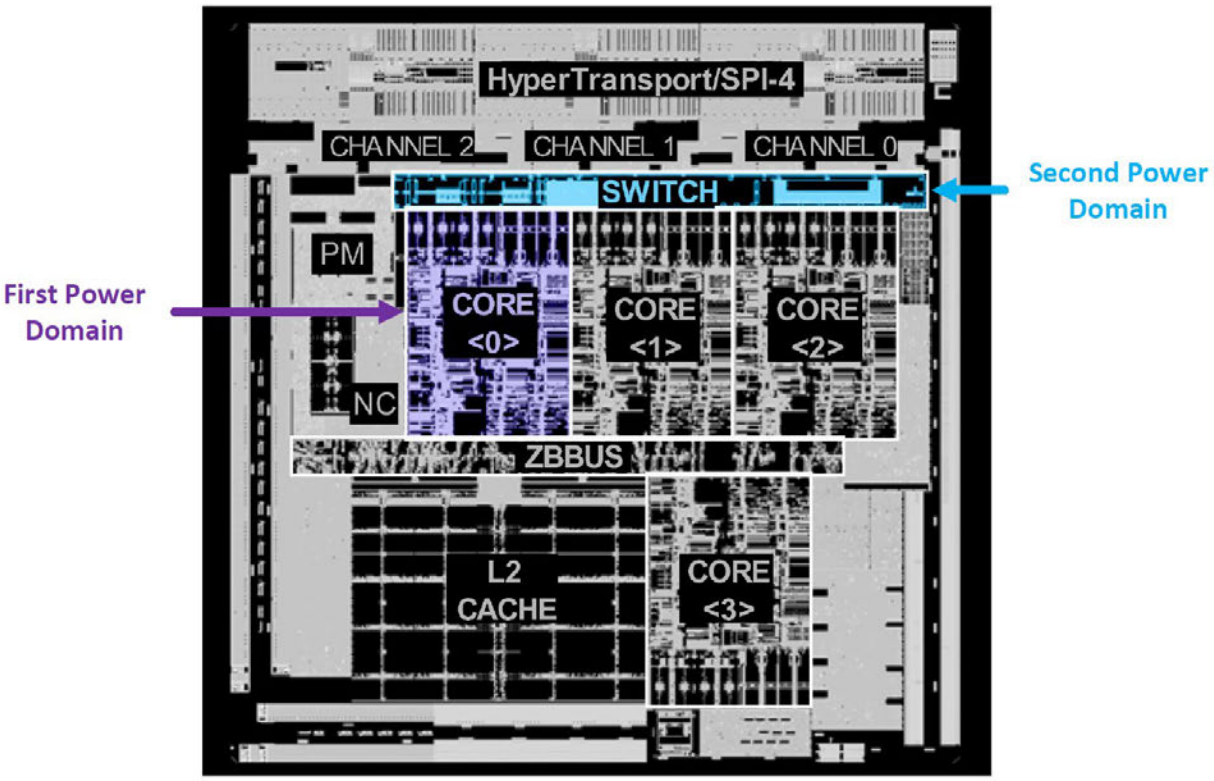
c. Claim 15

Claim 15 requires the global mesh to have first and second power wires for powering the first and second domains, along with at least one ground wire. *See* 218 patent at cl. 15. AMD points to Li's Figure 3 and contends "Li discloses a plurality of power and ground wires in its top-level mesh ('Ground (GND) and power (VDD_chip, VDD_switch) on layers Metal6 and Metal7":

[redacted]



RIB at 179 (citing RDX-0002.65); JX-0043.5 (Fig. 3). For background, AMD identifies core and switch logic circuit blocks as the first and second power domains:



RIB at 174-175; RDX-0002.56; JX-0043.2 (Fig. 1); Hr'g Tr. (Subramanian) at 966:6-967:2. The limitations of claim 15 are disclosed in Li as alleged.

Realtek contends claim 15 is not disclosed, relying on the claim "requir[ing] specific wires in the global power mesh to provide the power needed to the first and second power domains." CIB at 283. In light of this construction, Realtek continues, "Dr. Subramanian has not and cannot trace these wires to the power domains. Even if a VDD chip wire or a VDD switch wire provide power to the purported power domains, there is no disclosure that the specific wires identified in Figure 3 (RDX-0002.65) do so." *Id.* at 283-284.

Realtek is not persuasive. The test is not whether the specific wires shown in the illustration of Figure 3 of Li exist in reality within the Broadcom BCM1280 chip. Rather, the test is whether Li, as a publication, teaches "wherein the global power mesh comprises: at least one ground wire; at least one first power wire that provides the power needed by the first power domain; and at least one second power wire that provides the power needed by the second power domain." 218 patent at cl. 15; *Uber Techs.*, 957 F.3d at 1341. And Li does this. Figure 3 is a representation of the structure of the power grid which resides in Metal Layers 6 and 7. As shown, there are two separate power wires (VDD_chip, VDD_switch) which Li explicitly teaches are "routed alternatively on Metal-6 in the vertical direction and Metal-7 in the horizontal direction." JX-0043.4. Li thereafter states, "[t]his forms the power grid structure at the chip top level," and in the final stage local logic is connected to the top-level power grid. *Id.* Similarly, Li discloses that ground is supplied to the BCM1280 package through the GND lines. *Id.* The limitation is met.

Accordingly, claim 15 has been shown to be obvious under 35 U.S.C. § 103 over Li in light of Jiang.

d. Claims 16-17

Claims 16 and 17 require the first and second partial local power meshes to have first and second power wires for powering the first and second domains, along with at least one ground

wire, respectively. *Id.* at cls. 16, 17. Drawing on the concepts discussed above, Dr. Subramanian persuasively testified that the local grids in Li are left floating until final assembly and then serve to connect the local logic to the top-level power grid shown in Figure 3. *See* Hr'g Tr. (Subramanian) at 970:10-21, 973:10-22. It logically follows that to do so, each local grid must have a wire for the power which its associated logic block requires (*i.e.*, "power domain"), either VDD_chip or VDD_switch, and then must also have a wire for ground to complete the "full-chip power distribution network." JX-0043.4 ("Power and ground are supplied to the package through two VDD inputs (VDD_switch) and VDD_chip) and one GND input."). Li further notes the BCM1280 uses the "on-chip power and ground distribution system" so that "power/ground is delivered wherever needed." *Id.* The wires of the local grids must connect to the top-level grid to accomplish this, so the limitations of claim 16 and 17 are met. Realtek's opposition ignores all these teachings. *See* CIB at 284; CRB at 55-56.

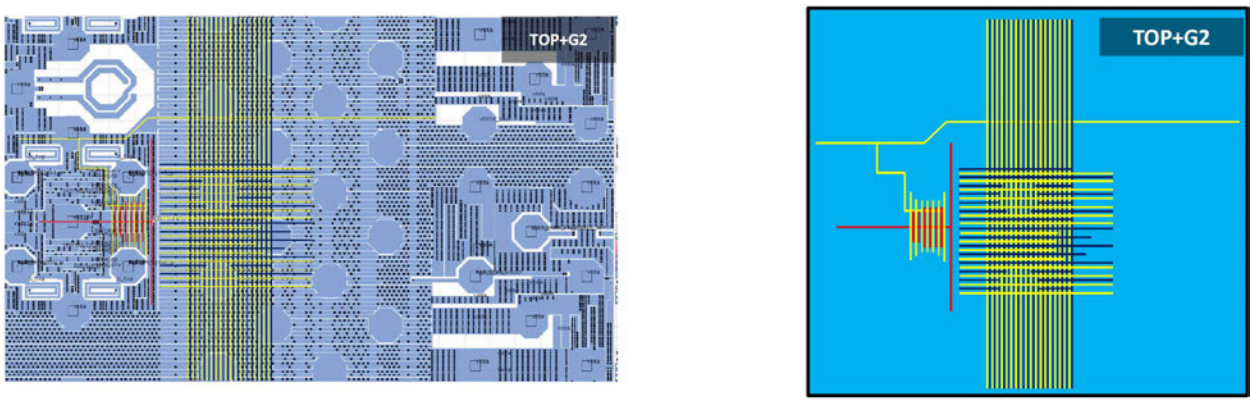
Accordingly, claims 16 and 17 have been shown to be obvious under 35 U.S.C. § 103 over Li in light of Jiang.

e. Claim 18

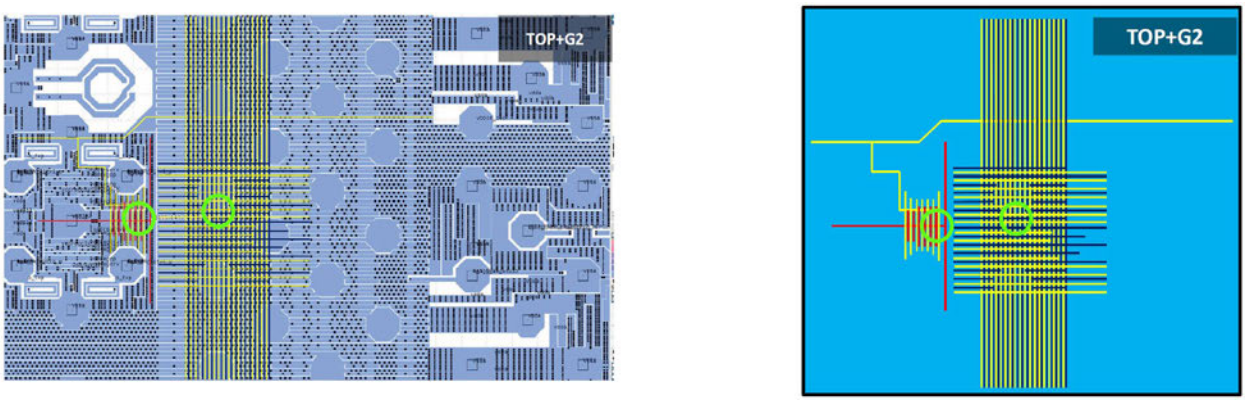
Claim 18 requires the two ground wires of the partial meshes to "share the same ground wire of the global power mesh." 218 patent at cl. 18. Unlike other claims, this one does require, in Realtek's phrasing, "specific wiring"—that is, Li must disclose that the ground wires of the local grids connect to the *same* ground wire within the top-level grid (whichever ground wire that may be). CRB at 55; *see* CIB at 283. AMD contends, "Li also discloses, or at least renders obvious, that the ground wires of the two local grids share the same ground wire of the global grid." RIB at 181. In his testimony, Dr. Subramanian opines that Realtek is quite flexible with its interpretation of "same ground wire" in the context of infringement, pointing specifically to the Starship accused product, and its multi-branch, convoluted ground wire which contains the vias

[redacted]

connecting down to the first and second local power meshes. Hr'g Tr. (Subramanian) at 976:3-977:4. That wire, as presented by Dr. Souri, is the yellow trace in the figures below:



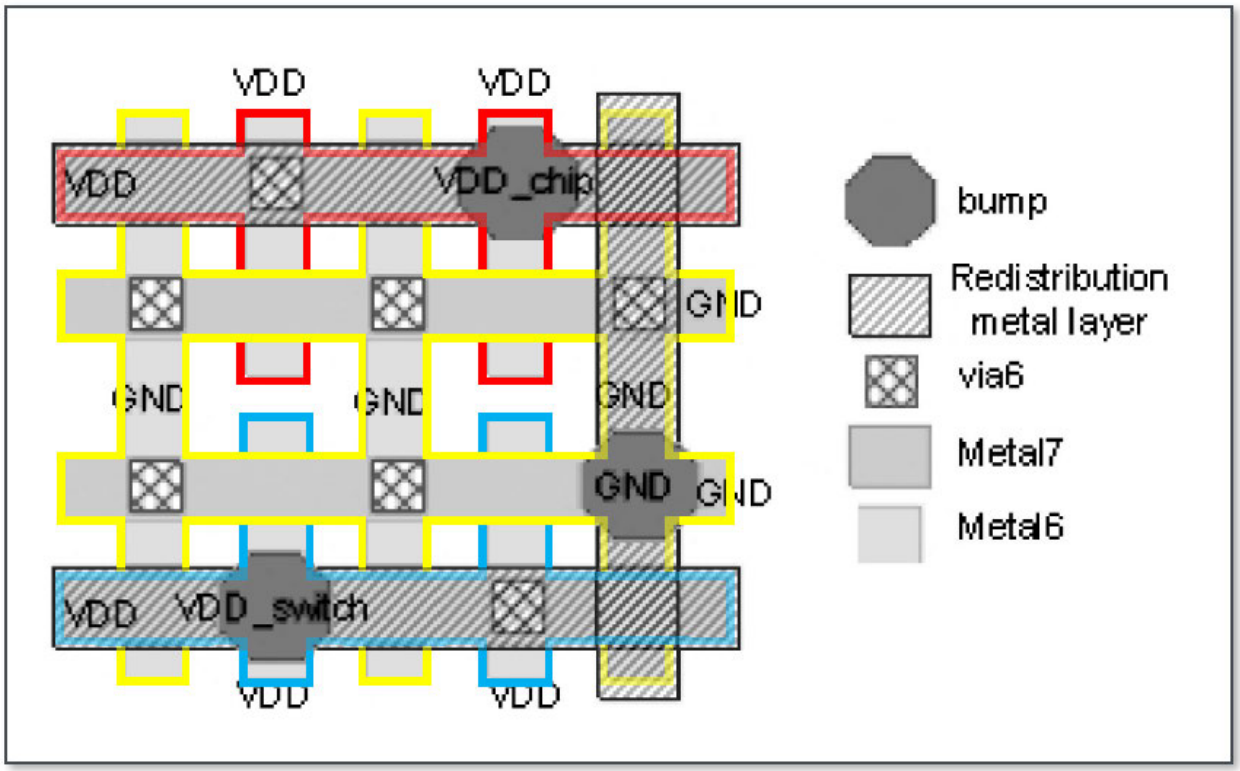
CDX-0003C.855; *see* CRB at 52-53. And although not clear in any single demonstrative of Dr. Souri, it can be determined through comparing several that the vias connecting to the local ground wires are located on opposite ends of this complicated ground wire, as in the green annotation circles:



CDX-0003C.855 (annotated); *see* CDX-0003C.851 (location of black arrow in "TOP" metal layer); CDX-0003C.852 (location of black arrow in "TOP" metal layer).

The shared ground wire in Starship is essentially the same as the shared ground wire shown in Figure 3 of Li, where all ground lines are connected to one another, creating a "super" wire of sorts:

[redacted]



RDX-0002.60 (annotated by AMD). Li further discloses that "[p]ower and ground are supplied to the package through two VDD inputs . . . and *one GND input*" (JX-0043.4 (emphasis added)) which is a clear suggestion that the local grid ground lines are connected somewhere along this one ground "super" wire. Realtek does not dispute the similarity between Li's Figure 3 and the accused ground wire in Starship (*see* CIB at 281-286; CRB at 53-56), so the limitation is met as alleged.

Accordingly, claim 18 has been shown to be obvious under 35 U.S.C. § 103 over Li in light of Jiang.

3. Lack of Written Description

AMD argues that each of claims 12, 13, and 15-18 are invalid under 35 U.S.C. § 112 for lack of written description. AMD begins with consideration of unasserted dependent claim 14, which reads: "14. The power routing structure according to claim 13, wherein the first local power

mesh and the second local power mesh are not electrically coupled." 218 patent at cl. 14. AMD reasons that: because this claim is dependent, it is presumed to have a narrower scope than the claims it depends from; it explicitly recites that the first partial local power mesh and second partial local power mesh are not electrically coupled; therefore, all other claims (12, 13, and 15-18) must cover embodiments in which the two partial meshes are electrically coupled. *See* RIB at 182-83. This is a problem, according to AMD, because such embodiments are not described in the specification:

> The asserted claims are invalid unless there is written support in the specification for both sets of embodiments. But there are no embodiments in the 218 patent where the two local power meshes are electrically coupled. Tr. (Subramanian) at 982:4-987:4. In fact, the specification makes clear that in the only disclosed embodiments, the first and second partial local power meshes are *not* electrically coupled. JX-0002 [5:54-59] ("the partial local power meshes 310, 320 … are not electrically coupled"). Because the specification does not provide any embodiments where the first and second partial local power meshes are electrically coupled, the specification fails to provide written support for the full scope of claims 12, 13, and 15-18. Those claims are, thus, invalid for failing to comply with the written description requirement.

RIB at 183 (emphasis in original); *see generally id.* at 182-186 (citing, *inter alia*, *Glaxo*, 262 F.3d at 1336; *Juno Therapeutics, Inc. v. Kite Pharma., Inc.*, 10 F.4th 1330, 1337 (Fed. Cir. 2021)); RRB at 68-69.

Unlike the claims in *Juno Therapeutics*, claim 12 of the 218 patent is not a "genus claim using functional language," so it is not clear that "both sets of embodiments" allegedly covered by claim 12 must meet the written description test applicable to genus/species claims. *See* RIB at 183; 10 F.4th at 1335. Assuming they do, though, the written description is adequate. As Dr. Souri explained, "shorting ground wires together" does "provide electrical coupling." Hr'g Tr. (Souri) at 1334:24-1335:5. And the specification expressly states that "the common ground wire 403 is used to supply the ground potential V_{GND} needed by the local power meshes 310, 320." 218

[redacted]

patent at 4:34-36. The written description thus discloses an embodiment where "the ground wires of the [partial local power meshes] are electrically coupled," and a skilled artisan would recognize that. CIB at 289. Accordingly, no claim has been shown to be invalid for lack of written description.

4. Lack of Enablement

Next, AMD challenges claims 12, 13, and 15-18 for a lack of enablement, also predicated on a finding that the claims encompass embodiments that are electrically coupled, and that a global power mesh cannot provide power "separately" to two meshes which are so coupled:

> Likewise, because claims must enable the full scope of their claims, the asserted claims are invalid unless there is enablement support for both sets of embodiments. But any embodiments where the first and second partial local power meshes are electrically coupled would be physically impossible and are not enabled under Realtek's proposed constructions. This is because claim 12 also recites "a global power mesh, coupling to the first local power mesh and the second local power mesh, to provide the power needed by the first power domain and the second domain separately." JX-0002 [7:64-67]. Under Realtek's construction of "separately," there is no way for an integrated circuit to both 1) contain a first local power mesh and a second local power mesh that are electrically coupled and 2) contain a first local power mesh and a second local power mesh that "separately" receive from the global power mesh the power needed by the power domains. If the local meshes are electrically coupled, then providing power to one necessarily provides power to the other, which means they are not receiving power separately. Likewise, if they are receiving power separately, then that means they are not electrically coupled, at least under Realtek's construction of "separately." *See* Tr. (Subramanian) at 982:5-987:4. Because the specification does not provide any embodiments where the first and second partial local power meshes are electrically coupled, the specification fails to enable the full scope of claims 12, 13, and 15-18, at least under Realtek's construction of "separately." Those claims are, thus invalid for failing to comply with § 112's enablement requirement.

RIB at 183-184.

AMD's theory fails for essentially the same reason as its lack of written description theory: a skilled artisan surely knows how to connect the ground wires of the local power meshes to achieve electrical coupling, as described in the specification. *See* 218 patent at 4:34-36. Accordingly, no claim has been shown to be invalid for lack of enablement.

VI. U.S. PATENT NO. 9,590,582

A. Level of Ordinary Skill in the Art

In Order No. 21, I determined that a person having ordinary skill in the art of the 582 patent at the time of invention:

> [W]ould have had at least a bachelor's degree in electrical engineering or an equivalent field, and at least 3-4 years of professional experience in the field of integrated circuit design. . . . Someone with additional education but less professional experience may qualify as a POSITA, such as someone with a master's degree in E.E. and 1-2 years of professional experience in the field of integrated circuit design or someone with a Ph.D. in electrical engineering.
>
> . . . .
>
> [E]xperience may substitute for education and vice versa; thus, graduate studies in electrical engineering or a related field may substitute for work experience and, likewise, additional work experience may substitute for relevant formal education.

Order No. 21 at 7-8. The parties do not challenge this definition (*see generally* CIB; CRB; RIB; RRB), and it is applied throughout this initial determination.

B. Claims-at-Issue

Claims 1-4 of the 582 patent are at issue in this investigation, either through allegations of infringement or domestic industry technical prong. *See* CIB at 300, 326. They are reproduced below, along with limitation identifiers:

> 1. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:
>
> [1a] a first insulation layer;
>
> [1b] an inductor component, comprising:
>
> [1c] a coil-conductor segment, located on a surface of the first insulation layer; and
>
> [1d] two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

[1e] a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,

[1f] wherein the capacitor component comprises: a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and

[1g] a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

2. The semiconductor device with an LC resonant circuit according to claim 1, further comprising:

[2a] a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and

[2b] an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

3. The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

4. The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

582 patent at cls. 1 (annotated), 2 (annotated), 3, 4.

C. Claim Construction

As part of the *Markman* process, the following claim terms of the 582 patent were construed, either as-agreed between the parties or determined by Order No. 21:

Claim Term	Construction
"two extension-conductor segments"	N/A; construction deferred
"coil-conductor segment"	N/A; construction deferred

"capacitor component"	"a component that includes one or more capacitors"
"plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction"	"at least a first connecting segment of the plurality of connecting segments overlaps one extension-conductor segment in a vertical direction, and at least a second connecting segment of the plurality of connecting segments overlaps the other extension-conductor segment in a vertical direction"

See Order No. 21 at 27, 28, 34, 36. The parties identify a number of additional claim construction disputes. One set of disputes, over the definition of, and demarcation between, the coil-conductor segments relative to the extension-conductor segments, does not appear to be material because it has no bearing on infringement, DI technical prong, or invalidity. *See* CIB at 296-98; RIB at 186-90. It would have been material to one of AMD's invalidity theories, but that theory, relating to a publication by Muh, is rejected because the publication has not been shown to be prior art.

As for the meaning of "coupled to," the parties appear to agree that it encompasses direct and indirect coupling, including by via, so there is no actual dispute. *See* CIB at 300; RRB at 81. The remaining genuine disputes are addressed below.

1. "capacitor component, arranged corresponding to the first region"

The parties identify "capacitor component" as needing construction. As noted above, Order No. 21 already resolved one dispute and construed the term as "a component that includes one or more capacitors." Order No. 21 at 34. Now, Realtek explains, "AMD has not articulated any new claim construction position but evidently argues that 'capacitor component' includes every capacitor within an arbitrary 'capacitor bank.' Tr. (Prucnal) at 1112:8-12. That position is contrary to the teaching of the '582 [patent] and the claim construction order." CIB at 290; *see id.* at 291-293. Realtek argues, "[t]here is nothing unusual or improper about having additional

capacitors connected to the claimed capacitor component. These are "comprising" claims, which permit additional elements so long as the claimed elements are found." *Id.* at 291 (citing *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997)).

AMD, for its part, takes the position in its rebuttal brief that "[t]he construction of [']capacitor component['] includes all capacitors that form the 'C' portion of the LC resonant circuit." RRB at 72 (citing 582 patent at 1:63-2:3, 12:40-47, 4:24-33). Put another way, AMD states, "according to the patent, however many capacitors form the C in the LC circuit, they all must be within (between/below) the outer edges of the extension-conductor segments." *Id.* at 74 (citing 582 patent at Figs. 1-17, 4:14-33, 12:28-36). Additionally, AMD acknowledges that the claim uses "comprises" but warrants the patent nevertheless "teaches against the 'capacitor component' extending beyond the extension-conductor segments." *Id.* (citing Order No. 20 at 4; 582 patent at 1:40-41, 2:1-3).

Relatedly, the parties identify "arranged corresponding to the first region" as needing construction. Realtek views AMD as "seek[ing] to append a negative limitation to 'corresponding to the first region'—that the capacitor component cannot extend beyond the first region." CIB at 293. Realtek rejects this interpretation, finding the specification teaching that "corresponding to" is met so long as the capacitor component is below the first region. *Id.* (citing 582 patent at 3:48-55); CRB at 65-66. Realtek claims, "[t]he specification explains that the benefits of the invention are achieved when one or more resonant capacitors 'correspond to' and therefore make use of what Dr. Phinney called the 'prime real estate.'" CRB at 66 (citing 582 patent at 1:66-2:3, 12:40-47; Hr'g Tr. (Phinney) at 133:5-10, 160:4-161:7, 197:23-198:7, 199:11-19, 202:114-24). Realtek further points to the specification's description of a "second region 122" also "defined by" certain

lines, but shown in the figures as crossing over those lines, at least partially. CRB at 67 (citing 582 patent at Fig. 15).

Realtek does acknowledge the issue came up during prosecution of the 582 patent, and that the applicant had attempted to distinguish prior art reference Daley (see below) on the grounds its capacitor extended in directions exceeding what would have been the first region. *See* CIB at 294 (citing JX-0009). Yet, Realtek urges this was unsuccessful and, ultimately, it was the limitation, "the capacitor component is not substantially overlapped with the coil-conductor segment" that traversed the rejection. *Id.*; *see* CRB at 65. According to Realtek, "[i]n such cases, there is no disclaimer." CIB at 294 (citing *Malvern Panalytical Inc. v. TA Instruments-Waters LLC*, 85 F.4th 1365 (Fed. Cir. 2023) ("*Malvern*")); CRB at 68.

AMD, on the other hand, contends, "[the] limitation requires that the capacitor component be located below the first region and entirely within the outer edges/sides of the extension-conductor segments." RIB at 190. AMD urges "[t]his is the only construction that conforms to the commonly understood meaning and is consistent with the intrinsic evidence." *Id.* (citing *Eon Corp. IP Holdings LLC v. Silver Spring Networks, Inc.*, 815 F.3d 1314, 1320 (Fed. Cir. 2016)). As for that evidence, AMD refers to Order No. 20 which recognized the overall purpose of the 582 patent invention, the consistency across embodiments shown in the figures and described in the specification, and the prosecution history. *See generally id.* at 190-197.

The weight of the intrinsic evidence favors AMD, although modifications to its proposal are warranted. As for the patent itself, its teachings are murky. In discussing possible indefiniteness, Order No. 20 recognized that the purported benefit of the invention is to limit the overall size of the circuit and to limit the location of the capacitor component as compared to the inductor component. Order No. 20 at 4. The patent states in its background, "a resonant capacitor

is arranged corresponding to an input/output part of the inductor component, so as to reduce generation of phase noise, arrangement of interconnecting wires, and an overall size" (582 patent at 1:66-2:3); and Dr. Phinney opined that placing the capacitor below the inductor "could introduce unwanted currents that leak into the substrate, into the capacitor, and it could also introduce additional loss. And that's what's called the parasitics" (Hr'g Tr. (Phinney) at 132:16-23). As noted in AMD's brief, every embodiment of the figures shows the capacitor component not exceeding the outer edges of the extension-conductor segments. RIB at 192 (citing 582 patent at Figs. 2, 5, 11, 15). But when the "first region 120" is identified in a figure, every embodiment also shows the capacitor component as exceeding the outer edges of that region, because first region 120 is always shown as between the inside edges of the extension-conductor segments. *Compare* 582 patent at Figs. 5, 8 *with id.* at Fig. 6, 9; *see generally id.* at Fig. 15. Thus, it cannot be that "arranged corresponding to the first region" means located entirely within the first region, or not to exceed the first region. *See* RIB at 190.

It is important to appreciate, however, that a construction of "vertically below the first region," as Realtek urges, causes its own problems. CIB at 296. For example, claim 1 recites "a first region is defined by the two extension-conductor segments and the coil-conductor segment," which implies a region bounded by, perhaps, the outer edges of the enumerated segments. 582 patent at cl. 1; *see id.* at 4:14-23 (identifying three possibilities: outer-outer, outer-inner, inner-inner), 7:19-28 (same). But then dependent claim 4 narrows that region with "wherein the first region is defined between the two extension-conductor segments." *Id.* at cl. 4. It is difficult to see how this language amounts to a difference for a POSITA designing a circuit if the first region is not a reasonably strict width-based boundary for the capacitor component. Increasing this difficulty is dependent claim 5, which depends from claim 4 and purportedly further narrows its

scope with "wherein the first region is defined between the two extension-conductor segments and the coil-conductor segment." *Id.* at cl. 5. The first portion of claim 5 ("defined between the two extension-conductor segments") repeats the limitation of claim 4, and the latter portion ("defined between . . . the coil-conductor segment") repeats a limitation of claim 1. There is no need to define the first region in this way if the capacitor component is free to escape it.

Fortunately, the prosecution history clears up the issue. At one point, the examiner rejected the applicant's claims as anticipated by U.S. Pub. No. 2009/0322447 ("Daley"). JX-0009.119-121. In relevant part, Daley disclosed an "on-chip inductor and an on-chip capacitor constructed in accordance with an embodiment of the invention and in which the capacitor is arranged between the inductor and the substrate" as shown below:

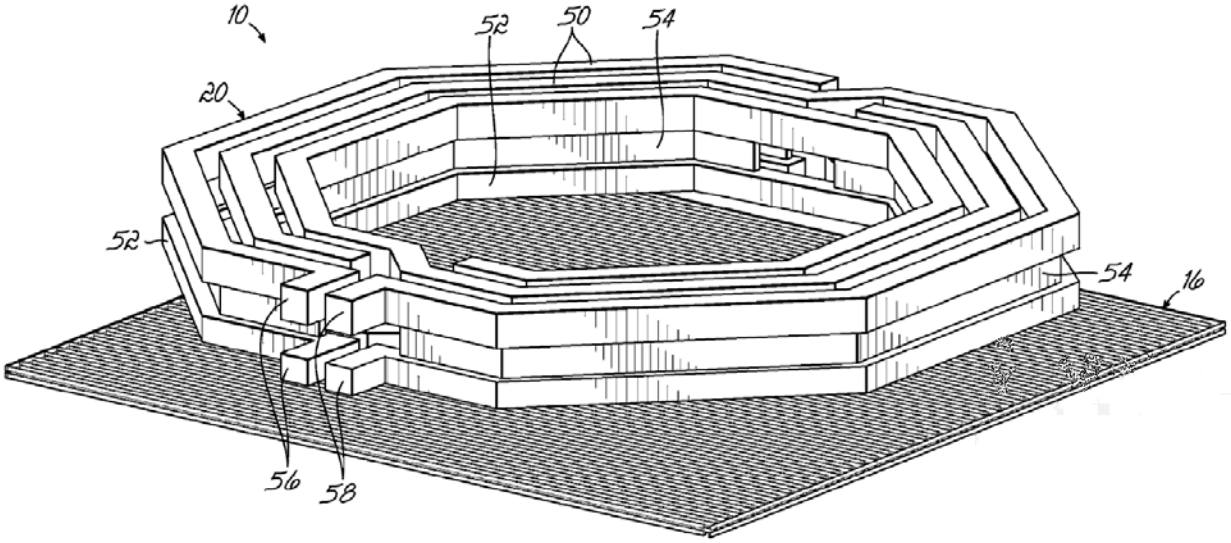


FIG. 1

JX-1017 at [0012], Fig. 1. The applicant then amended claim 1, among others, as follows:

[redacted]

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer,

wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment.

JX-0009.132. Along with the amendment, the applicant distinguished Daley for its failure to teach "a capacitor component, arranged corresponding to the first region" because of how Daley "covers the whole of the inductor 20," and stated "[t]hat is, in exemplary embodiments of the present invention, the capacitor component is substantially un-overlapped with the coil-conductor segment":

In Daley, the capacitor 16 covers the whole of the inductor 20. Furthermore, in order to operate as a Faraday shield and provide the isolation, **the capacitor 16 of Daley must be overlapped with the coil-conductor segment of the inductor 20 of Daley.**

The specification of the present application discloses:

> "in the semiconductor device with an LC resonant circuit according to the present invention, an LC resonant circuit may be integrated on a semiconductor substrate by means of a 3D die stacking technology, and a resonant capacitor is arranged corresponding to an input/output part of an inductor component, so as to ***reduce generation of phase noise, arrangement of interconnecting wires, and an overall size***. In some embodiments, in the semiconductor device with an LC resonant circuit according to the present invention, other electronic components are arranged corresponding to the input/out part or a staggered part of the inductor component, so as to further ***reduce generation of phase noise, arrangement of interconnecting wires, parasitic RLC (Resistance-Inductance- Capacitance) and an overall size***."

Claim 1 recites "***a first region is defined by the two extension-conductor segments and the coil-conductor segment***" "a capacitor component, ***arranged corresponding to the first region***" and "the capacitor component is correspondingly configured ***outwards relative to the coil-conductor segment***."

That is, in exemplary embodiments of the present invention, the capacitor component is substantially un-overlapped with the coil-conductor segment.

Id. at .0136. The applicant continued:

Therefore, Daley fails to teach or suggest, "***a first region is defined by the two extension-conductor segments and the coil-conductor segment***" "*a capacitor component,* ***arranged corresponding to the first region***" and "*the capacitor component is correspondingly configured* ***outwards relative to the coil-conductor segment***," as recited in claim 1.

Therefore, Daley fails to teach or suggest each and every feature of the claimed invention. Accordingly, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Allowable Subject Matter

Applicants gratefully acknowledge that the Examiner considers claim 5 to contain allowable subject matter. In view of the foregoing amendments and/or remarks, it is respectfully submitted that all claims should be fully in condition for allowance.

Id. at .0137.

From the figure above, it is clear that Daley teaches a "first region," a capacitor component located beneath that region, and that capacitor component extending "outwards" from the inductor spiral, because it extends in all directions. JX-1017 at Fig. 1. Thus, logically, for Daley to fail to teach these limitations (as the applicant argued) it must be because "arranged corresponding to the first region" was intended to define where the capacitor should not be as opposed to where it must be—what the Federal Circuit calls a "negative claim limitation." *See, e.g.*, *Imaginal Systematic, LLC v. Leggett & Platt, Inc.*, 805 F.3d 1102, 1111 (Fed. Cir. 2015); *N. Am. Container, Inc. v. Plastipak Packaging, Inc.*, 415 F.3d 1335, 1346 (Fed. Cir. 2005). This is essentially confirmed by the applicant's subsequent statement: "That is, in exemplary embodiments of the present invention, the capacitor component is substantially un-overlapped with the coil-conductor segment." JX-0009.136. Notably, lack of overlap was not yet a claim limitation at this time in the prosecution.

Despite this, the examiner rejected the claims again over Daley. JX-0009.146-149. Within Daley, the examiner continued to find a capacitor component arranged corresponding to a the first region:

> circular area within inductor 20)**; and a capacitor component** (Fig. 1, on-chip capacitor 16)**, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer** (Fig. 2a; Capacitor 16 is embedded within wiring structure 10 directly below the "first region" on the opposite surface (i.e. bottom surface) of dielectric 18.)**, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment** (Annotated Fig. 1 below; As shown, each of four corners of capacitor 16 all extend outwards in respective directions annotated as W-Z from signal lines 50 and 52.)**;**

Id. at .0147. The examiner disagreed with the applicant's understanding that the claim *as written* invoked the negative limitation of "un-overlapped":

> The Applicant states that Daley does not teach "the capacitor component is correspondingly configured outwards relative to the coil-conductor segment". That is, the capacitor component is substantially un-overlapped with the coil-conductor segment. The Examiner respectfully disagrees with the Applicant. As shown in the annotated Fig. 1 above, the four corners of capacitor 16 extend outwards from a perimeter of signal lines 50 and 52 in the directions annotated as W-Z. Thus, "the capacitor component" 16 is configured "outwards" relative to the "coil-conductor segment" 50 and 52. Further, whether or not the capacitor component is un-overlapped with the coil-conductor segment is true, this limitation is not commensurate with the claimed language in claim 1 and thus the related Applicant's arguments are not germane. Claims 1-4 and 6-10 have been repeated and sustained above with a new interpretation of "pair of staggered parts" as described above.
>
> ***Conclusion***
>
> 9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAKESH PATEL whose telephone number is (571)272-0961. The examiner can normally be reached on Monday-Friday 7:30 am-5:00 pm ET, ALT Fridays.

Id. at .0149-0150.

In response, the applicant amended the claim to make "un-overlapped" explicit:

[redacted]

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:

a first insulation layer;

an inductor component, comprising:

a coil-conductor segment, located on a surface of the first insulation layer; and

two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and

a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment.

JX-0009.156. But, most importantly, the applicant repeated, bolded, and all-capitalized its previous argument that Daley's full-span capacitor did not meet the "arranged corresponding to the first region" limitation:

Figure 1 of Daley clearly recites that the capacitor 16 covers with the ***WHOLE*** of the inductor 20.

In other words, in Daley, the four corners of capacitor 16 are ***NOT*** **arranged corresponding to the region defined by *TWO* conductor segments** (annotated as A shown in following FIG. 1) **and the coil-conductor segment** (the signal line 50 shown in following FIG.

1).

Moreover, in order to operate as a Faraday shield and provide the isolation, the capacitor 16 of Daley ***BE* overlapped with** the coil-conductor segment of the inductor 20 of Daley.

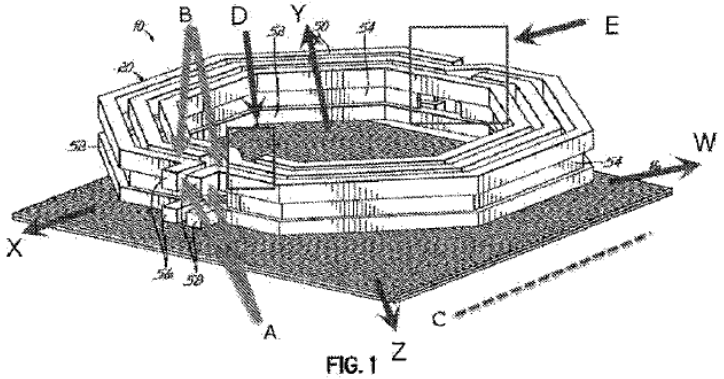


FIG. 1

In the present invention, the specification of the application discloses:

> "in the semiconductor device with an LC resonant circuit according to the present invention, an LC resonant circuit may be integrated on a semiconductor substrate by means of a 3D die stacking technology, and a resonant capacitor is arranged corresponding to an input/output part of an inductor component, so as to ***reduce generation of phase noise, arrangement of interconnecting wires, and an overall size***. In some embodiments, in the semiconductor device with an LC resonant circuit according to the present invention, other electronic components are arranged corresponding to the input/out part or a staggered part of the inductor component, so as to further ***reduce generation of phase noise, arrangement of interconnecting wires, parasitic RLC (Resistance-Inductance- Capacitance) and an overall size***."

Therefore, Daley fails to teach or suggest, "**a first region is *defined by the two extension-conductor segments* and the coil-conductor segment**" "**a capacitor component, *arranged corresponding to the first region***" "the capacitor component is correspondingly configured **outwards relative to the coil-conductor segment**" and "the capacitor component is substantially ***un***-overlapped with the coil-conductor segment," as recited in claim 1.

Therefore, Daley fails to anticipate the claimed invention. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

JX-0009.159-160. Thereafter, the prosecution continued without further relevant discussion.

Given the ambiguity in the patent's specification, a POSITA would find this prosecution history especially informative on the meaning of "a capacitor component, arranged corresponding to the first region." It fits squarely within *Phillips'* guidance that "the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution." 415 F.3d at 1317. Realtek's suggestion that these events are ineffective as disclaimer because the applicant "abandoned its prior argument" (CIB at 294) is wrong for two reasons. First, AMD does not allege prosecution history disclaimer (RRB at 75). Second, there was no abandonment of the argument. As shown, the applicant doubled down on its belief that "arranged corresponding to the first region" was not met in Daley. This readily distinguishes Realtek's cited case, *Malvern*, which hinged upon a clear abandonment of an "unviable argument":

> Here, although the '782 patent applicant argued that the '968 application discloses only a manual guiding mechanism, J.A. 2919, the examiner clearly stated its rejection of this argument several times. J.A. 2858, 2872–73, 2893, 2906–07, 2926–27. The '782 patent applicant then abandoned this unviable argument that the '968 application only discloses a manual guiding mechanism and instead successfully argued that the '968 application did not qualify as prior art. J.A. 2842, 2852. A reasonable interpretation of this colloquy with the examiner is that by abandoning its argument that the '968 application discloses only a manual guiding mechanism, the '782 patent applicant acquiesced to the examiner's views regarding the scope of the '968 application.
>
> In these circumstances, where an applicant abandons its unsuccessful argument, we conclude that the prosecution history lacks the clarity necessary to establish prosecution disclaimer. We have previously declined to find prosecution disclaimer where an applicant made an allegedly disclaiming argument to overcome prior art, the examiner disagreed, and the applicant "never repeated the allegedly disclaiming statements and instead offered alternative reasons to overcome" the prior art. *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1343 (Fed. Cir. 2009). The circumstances here are similar to the circumstances in Ecolab. By abandoning its arguments about the scope of the '968 application, "a reasonable reader" of the '782 patent prosecution history could conclude that the '782 patent applicant "recognized its error and never again repeated or relied upon the erroneous rationale." *Id.* In such circumstances, an applicant's statements "simply are not clear and unmistakable enough to invoke the doctrine of prosecution history disclaimer." *Id.*;

> *see also Mass. Inst. of Tech. v. Shire Pharms., Inc.*, 839 F.3d 1111, 1120–21 (Fed. Cir. 2016) (concluding no unambiguous prosecution disclaimer where a patent applicant attempted to add a limitation, the examiner rejected the added limitation under § 112 as new matter, and the applicant "never again sought to limit the claims" with the additional limitation).

Malvern, 85 F.4th at 1376. Equally false is Realtek's assertion the benefits of the invention are achieved simply by "mak[ing] use" of the "prime real estate" under the extension-conductor segments. CRB at 66. Daley had already done this, and to avoid rejection the applicant argued that the first region is defined by "the two extension-conductor segments," that is, by width. JX-1017 at Figs. 1, 3, 4; JX-0009.159 (emphasis omitted).

Accordingly, given the 582 patent specification and prosecution history, a POSITA would understand "a capacitor component, arranged corresponding to the first region" to mean "a capacitor component substantially limited to the first region," as exemplified in the patent's figures.

2. "insulation layer"

Claim 1 recites, "a first insulation layer" with the coil-conductor and extension-conductor segments each located on the same "surface of the first insulation layer," and then also a "capacitor component, arranged . . . in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer." 582 patent at cl. 1. The parties appear to dispute the extent to which a stack of patterned layers within a chip can be considered together as the claimed "first insulation layer." Realtek argues, "[t]he intrinsic record leaves no doubt that an insulation layer can include, within it, multiple metal layers and can be formed from multiple layers of insulating materials." CIB at 299. In its initial post-hearing brief AMD does not present a claim construction argument regarding this term, and neither side proposes an actual construction for it. *See id.*; RIB at 186-97.

The specification is clear that the "first insulation layer" has a broad meaning, because it can include multiple sub-layers of either insulative or metallic materials. *See, e.g.*, 582 patent at Fig. 10. AMD is correct that every disclosed embodiment shows the claimed conductor component on the "other surface," that is, the bottom surface of the first insulation layer, however many sub-layers it has, but concedes that some disclosed embodiments include an inductor component formed in multiple sub-layers. *See* RRB at 78-80 (citing 582 patent at Figs. 7, 10). So inasmuch as "first insulation layer" implicates claim construction—for instance, because AMD argues that one such identified layer "includes at least six different layers"—the term is construed as "a stack of material that acts overall as an insulator but may incorporate conductive components." RIB at 203.

AMD seemingly advances a second claim construction dispute involving this term in its reply brief. *See* RRB at 76-81. AMD argues that the "first insulation layer ends at the capacitor component," and that the specification "do[es] not teach that the first insulation layer includes a capacitor component therein." *Id*. at 78, 81. In view of the construction above, a capacitor component is a "conductive component," so inasmuch as AMD's argument pertains just to the first insulation layer, it is beside the point. But AMD also cites claim 1's requirement that the capacitor component be "'on the other surface' in an embedded manner" in arguing that claim 1 does not encompass a "capacitor component embedded in the middle of an insulation layer." *Id*. at 76, 80.

To be sure, most disclosed embodiments avoid this issue because their capacitor components are formed in a single layer, so every capacitor component is simply embedded in the bottom sub-layer of the first insulating layer, with no penetration into higher sub-layers. *See* 582 patent at Fig. 10. But the specification is clear that the claimed capacitor component "may be formed [as] . . . a multi-layer metal stack." *Id*. at 12:35-36. It would appear impossible for a multi-

[redacted]

layer capacitor component to be simultaneously "embedded" in the first insulation layer "on the [bottom] surface," as required by claim 1, and "sandwiched between" the first and second insulation layers, as required by claim 2, without some of the capacitor component's layers penetrating the first insulation layer, or the second insulation layer, or both. So inasmuch as AMD argues, as a matter of claim construction, that no layers of a multi-layer capacitor component may be "embedded in the middle of an insulation layer," that argument is unpersuasive because it rules out a preferred embodiment. RIB at 80.

Instead, to accommodate the 582 patent's contemplated multi-layer capacitor component, "in an embedded manner on the other surface" is construed to mean "at least partially on the other surface," and "is sandwiched between" is construed to mean "includes at least a portion between."

D. Infringement

According to Realtek's post-hearing briefing, the use, manufacture, or sale of the Accused Products generally infringe claims 1-4. Specifically, it contends, "all Accused Products infringe claims 1-3 of the '582 patent, and [redacted] infringe [c]laim 4." CIB at 300. Of these, claim 1 is independent and claims 2-4 depend from claim 1. For the reasons discussed below, Realtek has not shown infringement of these claims by the Accused Products.

1. Claim 1

For reference, claim 1 of the 582 patent requires:

> 1. A semiconductor device with an inductor-capacitor (LC) resonant circuit, comprising:
>
> [1a] a first insulation layer;
>
> [1b] an inductor component, comprising:
>
> [1c] a coil-conductor segment, located on a surface of the first insulation layer; and
>
> [1d] two extension-conductor segments, located on the surface of the first insulation layer, coupled to two ends of the coil-conductor segment respectively, arranged at

> an interval, and extending outwards relative to the coil-conductor segment, wherein a first region is defined by the two extension-conductor segments and the coil-conductor segment; and
>
> [1e] a capacitor component, arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer, wherein the capacitor component is correspondingly configured outwards relative to the coil-conductor segment, and the capacitor component is not substantially overlapped with the coil-conductor segment,
>
> [1f] wherein the capacitor component comprises: a plurality of connecting segments, extending corresponding to the two extension-conductor segments in a same direction, wherein the plurality of connecting segments are respectively overlapped with the two extension-conductor segments in a vertical direction; and
>
> [1g] a plurality of electrode segments, located below the first region, wherein one end of each of the plurality of electrode segments is coupled to one of the plurality of connecting segments, and each of the plurality of electrode segments extends laterally relative to the respective coupled connecting segment of the plurality of connecting segments.

582 patent at cl. 1 (annotated). In support of infringement, Realtek primarily relies on the testimony of Dr. Phinney and a series of demonstratives showing various metal layers within the stack of each Accused Product. Realtek represents that a number of limitations are present in the Accused Products and not disputed by AMD, including: [1pre], [1b], [1c], portions of [1d], portions of [1e], portions of [1f], and [1g]. *See* CIB at 316-324; *see also* RIB at 197-207; RRB at 81-88. Even for these, however, AMD observes a flaw in Realtek's briefing:

> 2. Realtek Has Failed Its Burden of Proof
>
> For many claim limitations, Realtek fails to cite its expert's trial testimony. Instead, Realtek cites only demonstratives, which are not evidence. CPoTB, 317-325. This is true for its DI analysis as well. *Id*., 336-342. This is no better than relying on attorney argument and cannot meet Realtek's burden.

RRB at 88. AMD is correct. Throughout its discussion of infringement under the 582 patent, Realtek surprisingly fails to cite any testimony of Dr. Phinney despite routinely stating, "Dr. Phinney established . . . that the Accused Products . . .." *See generally* CIB at 317-325. In its reply brief, Realtek cites to Dr. Phinney for infringement a total of *two* times. CRB at 69 (citing

Hr'g Tr. (Phinney) at 140:1-141:10), 70 (citing Hr'g Tr. (Phinney) at 149:14-23). Nevertheless, it is clear from a review of Dr. Phinney's testimony at the hearing that these limitations were addressed and are present in the Accused Products as alleged. *See generally* Hr'g Tr. (Phinney) at 138:18-139:19 ([1pre]), 146:7-21 ([1b]), 146:22-150:1 ([1c]), 155:11-159:20 (portions of [1d]), 161:8-168:24 (portions of [1e]), 172:6-176:17 (portions of [1f]).

AMD does contest the presence of certain elements, though. Its first basis for non-infringement is persuasive—that "AMD's capacitor component is arranged beyond the claimed first region and the outer edges of the extension-conductor segments." RIB at 197. As shown below, using AMD's demonstratives for each accused product grouping, , placing it outside any of the three options for the "first region" laid out in the 582 patent specification and discussed above:

RDX-0007C.38 (citing RX-1286C.640) ( );

RDX-0007C.39 (citing RX-1286C.771) ;

RDX-0007C.40 (citing RX-1286C.855) ( );

RDX-0007C.41 (citing RX-1286C.927) AMD's black-box identification of the "capacitor component" is reasonable because it matches the extent of Properly construed, the asserted claims of the 582 patent require this capacitor component to fall substantially within the area of the extension-conductor segments, and it does not. And AMD and Dr. Prucnal offer a credible explanation for why the components go too far—"a larger capacitor component to provide greater flexibility in tuning the LC circuit." RIB at 198 (citing Hr'g Tr. (Prucnal) at 1112:13-24). Dr. Phinney acknowledged the need for this capability in his re-direct testimony. Hr'g Tr. (Phinney) at 360:3-13 ("So the whole point of a lot of [capacitors] is to be able to tune or switch your frequency. So you need many capacitors. There's actually intervening switches to engage different capacitors. So there's that control knob aspect.").

Realtek attempts to rebut this conclusion by alleging that the "capacitor component" is just a subset of the capacitors shown in the banks above, as shown below for :

First region

CIB at 302 (citing CDX-0002C.251; CPX-0215C.619, 614). But as explained, "a capacitor component, arranged corresponding to the first region" means that the capacitive structures of the LC circuit overall must be "substantially limited to the first region." Realtek is not free to

arbitrarily select a subset of capacitors to meet this element because, again, the prosecution prior art reference Daley teaches the limitation—it too has a subset of capacitors located within its "first region"—and the applicant adamantly argued such was not the case during prosecution:

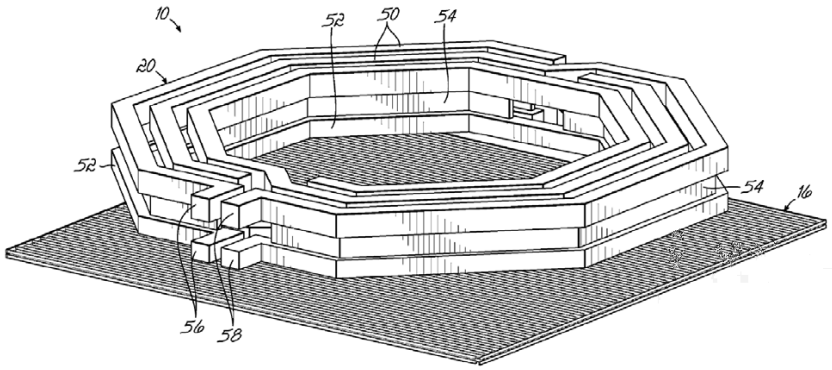


FIG. 1

JX-1071 at Fig. 1; JX-0009.141. Put another way, "a capacitor component, arranged corresponding to the first region" is not met simply by placing some but not all capacitors in the "prime real estate." CIB at 307. The prior art already did this.

AMD offers a number of other non-infringement arguments which are not as persuasive. First, AMD takes issue with each of Realtek's two theories for "a first insulation layer." The two are presented below using the Starship accused product as an example, one thick, one thin:

CDX-0002C.219, 220; *see* CPX-0215C.1806, 1798; CIB at 310-312 (citing Hr'g Tr. (Phinney) at 152:19-155:10). The record is clear, regardless of these layer identifications, that insulating material exists in-between all metal structures in the semiconductor stack (*i.e.*, there is no empty space). As Realtek puts it, "insulating material extends around the metal within an insulation layer (including between the fingers of a finger capacitor)." *Id.* at 309 (citing, *inter alia*, Hr'g Tr. (Phinney) at 141:11-146:1; JX-0023C (Seahra) at 29:4-7, 43:4-16, 48:23-25; JX-0015C (Jing) at 101:15-24, 102:4-7).

In light of this reality, and the broad construction for "insulation layer" determined above ("a stack of material that acts overall as an insulator but may incorporate conductive components"), the first of Realtek's theories is sufficient— *See* RIB at 203. AMD's only argument against this first theory is that the claim cannot be met "because it includes at least ." *Id.* at 203-204 (citing Hr'g Tr. (Prucnal) at 1116:2-21); RRB at 84 n. 34. But the construction allows for this—" a stack of material that acts overall as an insulator but may incorporate conductive components." The limitation is met as alleged.

Relatedly, AMD argues that the accused capacitor component in each Accused Product is not "arranged corresponding to the first region in an embedded manner on the other surface, opposite to the inductor component, of the first insulation layer." RIB at 204-206. AMD points out that the alleged component is made up of several different structures and "these structures are all on " thereby precluding their ability to "*all* be arranged in an embedded manner, 'on the other surface' of the first insulation layer." *Id.* at 204 (citing Hr'g Tr. (Prucnal) at 1117:20-1118:20) (emphasis in original). AMD provides the following example of the multi-layer structures making up the "capacitor component" in the accused product:

Id. at 205 (citing RDX-0004C.86; JPX-0211C.SC-AMD-ITC-1350_00001245). AMD clarifies its position in its reply brief:

> AMD never contended that, to satisfy the limitation "embedded…on the other surface," "every portion of the capacitor component [must be] on the same surface opposite the inductor component." CPoTB, 312. For instance, the RFR6122 has a capacitor component with portions on different surfaces/layers (*e.g.*, MIM capacitor bottom plate on M3 and top plates on M3+), but RFR6122 still satisfies this limitation because RFR6122 has both claimed "connecting segments" and "electrode segments" embedded on the same surface/layer M3. *See* Section V.D.2 infra; *see also* Section V.D.1 (RBR1000 having multi-layer (M3-M1) VPP capacitors that satisfy the claimed "capacitor component"). Therefore, the claimed capacitor component can be multi-layer if it has the claimed "connecting segments"

[redacted]

> and "electrode segments" embedded on the same surface/layer. CPoTB, 312 (wrongly asserting that "[AMD's] argument would preclude a multi-layer capacitor component.").35 But this is not true for AMD's products. CDX-0002C.0266, .0276; Tr. (Phinney) at 171:17-172:5, 177:3-178:8 ([redacted]).

RRB at 86.

AMD's understanding—that the "connecting segments" and "electrode segments" of the claimed capacitor component must be on the same surface/layer—is not supported by the claim language. Unlike for the inductor component limitation, where the "coil-conductor segment" and "two extension-conductor segments" are called out, individually, as being positioned on a particular surface, the "connecting segments" and "electrode segments" are not. 582 patent at cl. 1. Only the overall "capacitor component" must be "arranged . . . in an embedded manner on the other surface." *Id.* And properly construed, the claim language is satisfied because [redacted] (altogether making up the "capacitor component") are "at least partially on the other surface," that is, [redacted] Hr'g Tr. (Phinney) at 142:19-22. This is true for all Accused Products. *See* RDX-0004C.88.

AMD next contends that Realtek has identified too many structures for the "capacitor component" in that the [redacted] are simply interconnect elements and not truly part of the capacitor component. *See* RIB at 206-207; RRB at 87-88. This argument directly conflicts with AMD's identification of all capacitor units tied together as one "capacitor component"—which visibly includes [redacted] that create the overall parallel connection and define the component:

RDX-0004C.76; *see* RIB at 198-200; CPX-0215C.1806, 1798, 1257, 1729. Moreover, as Order No. 21 determined, the construction for "capacitor component" is broad—"a component that includes one or more capacitors"—and can include multiple capacitors and their associated interconnections. Order No. 21 at 30-34. Naturally, this covers the interconnecting segments.

AMD lastly argues that Realtek and Dr. Phinney have not met their burden to show that the are "electrode segments" under limitation [1g] for just the product. RIB at 207 n.30 (citing Hr'g Tr. (Phinney) at 177:3-178:8; Hr'g Tr. (Prucnal) at 1119:11-21)); RRB at 87-88. These are important structures because the claims require the electrode segments to "extend[] laterally relative to the respective coupled connecting segment" (582 patent at cl. 1) and "electrode segment" has so far gone unconstrued. Realtek counters:

> AMD also argues, in a footnote, that certain portions of the are not resonant. RPostHB at 207 n.30. Even if that were true, it is irrelevant. The are "the capacitive part" and therefore the electrode segments. JX-0015C.0054:4-55:19; JPX-0229C.25, .26 (SC-AMDITC-1350_00001814, 1815). There is no requirement for the electrode segments to be coupled to the connecting segments or be resonant.

[redacted]

CRB at 71.

The weight of the evidence favors Realtek. The patent specification distinguishes between capacitor electrodes and capacitor connecting segments with: "The electrode segments 155 and 156 serve as electrode plates of the capacitor, capacitive induction is generated between the electrode segments 155 and 156. The connecting segments 151 and 152 are used for receiving or transmitting a signal." 582 patent at 4:41-45. In [redacted] are interdigitated just like the [redacted], and they extend out from what even AMD acknowledges is a [redacted] as shown below:

[redacted]

CDX-0002C.277 (citing CPX-0215C.609, 1804); RIB at 207 n.30. And in shape, arrangement, and location, for which there is no dispute:

CDX-0002C.279 ( ) (citing CPX-0215C.1499, 2212); *see also* CDX-0002C.282 ( ); CDX-0002C.285 ( ). This strongly suggests the contribute to "capacitive induction." AMD witness, Dr. Kevin Jing, also explained that

[redacted]

[redacted] *Id.* at 54:19-55:19. While Dr. Phinney was rather conclusory on this point (Hr'g Tr. (Phinney) at 177:13-17 (referring to "comb" and "teeth")), the overall thrust is that the [redacted] are "electrode segments" as understood by the patent. So this portion of limitation [1g] has been sufficiently shown for the [redacted] product.

Nevertheless, and as determined above, claim 1 is not infringed by the Accused Products because their capacitor components are not substantially limited to the claimed first regions.

2. Claim 2

For reference, claim 2 of the 582 patent requires:

> 2. The semiconductor device with an LC resonant circuit according to claim 1, further comprising:
>
> [2a] a second insulation layer, wherein the capacitor component is sandwiched between the first insulation layer and the second insulation layer; and
>
> [2b] an electronic component, arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer.

582 patent at cl. 2 (annotated). Realtek contends, based on the testimony of Dr. Phinney, that the Accused Products include the limitations of claim 2, and offers the following image of [redacted] as self-explanatory and exemplary of all products:

CIB at 324; *see* CDX-0002C.288; CPX-0215C.1501; Hr'g Tr. (Phinney) at 183:3-186:15. AMD does not dispute infringement of claim 2 apart from its dependency on claim 1. RIB at 207; *see* RRB at 81-88. In light of the cited evidence and opinion, the additional elements of claim 2 are met in the Accused Products; but the claim is not infringed based on claim 1, above.

3. Claim 3

For reference, claim 3 of the 582 patent requires:

> 3. The semiconductor device with an LC resonant circuit according to claim 2, wherein the electronic component is one of another capacitor component, a transistor component, a diode component, and a resistor component.

582 patent at cl. 3. Realtek contends, based on the testimony of Dr. Phinney, that the Accused Products include the limitations of claim 3 and offers the following image of as self-explanatory and exemplary of all products:

CIB at 325; *see* CDX-0002C.291; CPX-0215C.1501; Hr'g Tr. (Phinney) at 186:16-187:5. AMD does not dispute infringement of claim 3 apart from its dependency on claim 1. RIB at 207; *see* RRB at 81-88. In light of the cited evidence and opinion, the additional elements of claim 3 are met in the Accused Products; but the claim is not infringed based on claim 1, above.

4. Claim 4

For reference, claim 4 of the 582 patent requires:

> 4. The semiconductor device with an LC resonant circuit according to claim 1, wherein the first region is defined between the two extension-conductor segments.

582 patent at cl. 4. Realtek contends, based on the testimony of Dr. Phinney, that only the Accused Products include the limitations of claim 4 and offers the following image of as self-explanatory and exemplary of all products:

[redacted]

[redacted]

CIB at 325; *see* CDX-0002C.297; CPX-0215C.1185, 2109; Hr'g Tr. (Phinney) at 187:6-189:12. AMD correctly contends claim 4 is not met for the same reasons as limitation [1e] above. RIB at 207. For those reasons, the additional limitations of claim 4 are not met.

E. Domestic Industry – Technical Prong

According to Realtek's post-hearing briefing, the DI Products practice claims 1-4 of the 582 patent. CIB at 326. For the reasons discussed below, Realtek has shown by a preponderance of the evidence that the DI Products practice claims 1-3, but not claim 4.

1. Claim 1

Claim 1 of the 582 patent is presented above in connection with infringement. In support of its theory, Realtek again fails to cite the pertinent expert testimony from Dr. Phinney for most limitations. *See generally* CIB at 326-42. Nevertheless, that testimony can be found and is cited below, and Realtek's briefing, in totality, alleges the following.

Realtek asserts limitation [1pre] is met in the DI Products per the testimony of Dr. Phinney and the following imagery:

CIB at 336 (citing JPX-0420.65C; JPX-0419C.57); *see* CDX-0002C.300; Hr'g Tr. (Phinney) at 190:2-192:2. For limitation [1a], Realtek contends, much like in the Accused Products, " as shown in the imagery below:

CIB at 328 (citing, *inter alia*, CDX-0002C.329; CPX-0195C; CPX-0194C; Hr'g Tr. (Phinney) at 192:3-193:7).

For limitation [1b], Realtek contends, pursuant to testimony from Dr. Phinney, that both DI Products include it as shown below:

CIB at 337 (citing CPX-0195C); *see* CDX-0002C.308-309; Hr'g Tr. (Phinney) at 193:8-17. As for limitation [1c], Realtek contends, pursuant to testimony from Dr. Phinney, that the DI Products include it as shown below:

CIB at 337 (citing CPX-0175C; CPX-0178C; CPX-0195C; CX-0197C); CDX-0002C.310; Hr'g Tr. (Phinney) at 193:18-194:7.

[redacted]

As for limitation [1d], Realtek contends, pursuant to testimony from Dr. Phinney, that the DI Products include it as shown below:

[redacted]

CIB at 338 (citing CPX-0175C; CPX-0178C; CPX-0194C); *see* CDX-0002C.318; Hr'g Tr. (Phinney) at 194:8-200:21. Realtek presents several theories as to which structure(s) constitute the "extension-conductor segments," including: 1) the [redacted], 2) the [redacted], or 3) both [redacted] as "contiguous 'two-layer structures.'" *See generally* CIB at 329-335. Realtek further contends that the [redacted] qualify as "extension-conductor segments," in whole or in part, both literally and under the doctrine of equivalents. *See id.* Further, and while not mentioned in Realtek's brief for this limitation (*see* CIB at 338), Dr. Phinney opined that one possible "first region" is shown in the below images when those [redacted] treated as the "extension-conductor segments":

CDX-0002C.321; Hr'g Tr. (Phinney) at 200:14-201:20; JPX-0420C; CPX-0194C. As explained further below, at least the literally satisfy the "extension-conductor segments" limitation.

As for limitation [1e], Realtek contends, pursuant to testimony from Dr. Phinney, that the DI Products include it as shown below:

CIB at 339 (citing JPX-0420C; CPX-0194C; CPX-0179.2C); *see* CDX-0002C.325; Hr'g Tr. (Phinney) at 201:21-205:6.

For limitation [1f], Realtek contends, pursuant to testimony from Dr. Phinney, that the DI Products include it as shown below:

CIB at 340 (citing CPX-0179.2C; CPX-0194C); *see* CDX-0002C.331; Hr'g Tr. (Phinney) at 205:7-206:15. The following additional image shows the "connecting segments" of the capacitor component more clearly:

CDX-0002C.332; *see* Hr'g Tr. (Phinney) at 205:7-206:15; CPX-0120C.2; CPX-0194C.

For limitation [1g], Realtek contends, pursuant to testimony from Dr. Phinney, that the DI Products include it as shown below:

CIB at 340-341 (citing CPX-0120C.2; CPX-0194C; CPX-0179C.3); CDX-0002C.336; Hr'g Tr. (Phinney) at 206:16-208:14. Again, the following shows the :

CDX-0002C.331; Hr'g Tr. (Phinney) at 206:16-208:14; CPX-0120C.2; CPX-0194C. The limitations of claim 1 are therefore met in the DI Products as alleged.

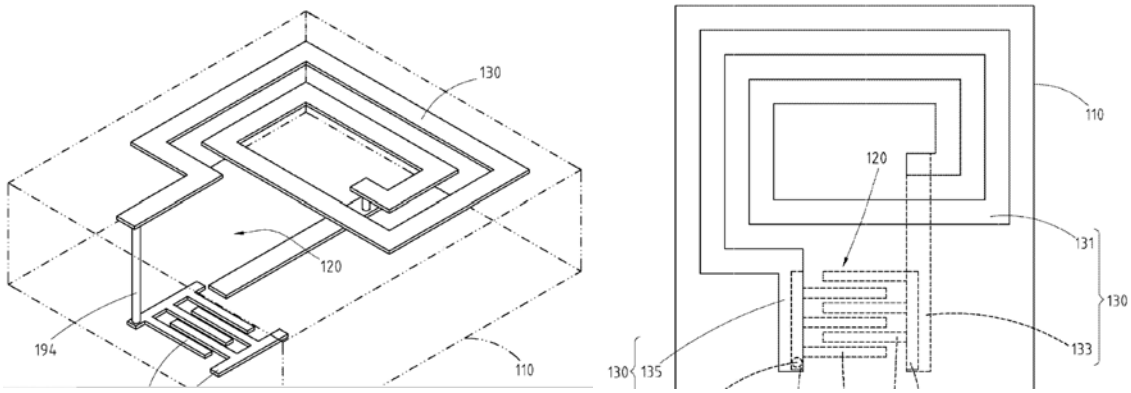
Several of AMD's arguments for technical prong domestic industry have been addressed above for infringement, as AMD acknowledges. RIB at 208; RRB at 88. AMD contends that "first insulation layer" has not been shown because "[t]he alleged insulation layer includes multiple

different metal/insulation layers." *Id.* (citing Hr'g Tr. (Prucnal) at 1121:22-1122:10). As determined above, the term is broad enough to cover the overall insulation thickness between layers Also contrary to AMD's argument and as determined above, "capacitor component" is broad—"a component that includes one or more capacitors"—and can include, for example, multiple capacitors and their interconnecting parts (RIB at 209-210); and not all of those parts need be on the same layer (*see id.* at 209).

AMD further identifies "[a]n additional issue [] unique to cannot constitute "extension-conductor segments" because they are not properly a part of the inductor, which, according to a Broadcom witness, . RIB at 210 (citing JX-0022C.21:24-22:8, 22:23-23:8); RRB at 89-90. The test is not whether the segments fall within of its own "inductor," however. The test is whether they (otherwise meeting the construction for "extension-conductor segments") fall within the plain and ordinary meaning of "inductor component." And as with "capacitor component" above, it is natural to treat "inductor component" as encompassing both the segments creating the inductive effects and their interconnecting parts (

The evidence shows the are interconnecting parts of the inductor circuit element, both in structure and function. The structural similarity between extension-conductor segment 133 in the 582 patent and is striking:

[redacted]



[redacted]

582 patent at Figs. 1, 2; RIB at 208 (citing RDX-0004C.90; JPX-0427C.BCM0000772). And the patent explains the purpose of the "extension-conductor segments" is to simply be the "input/output part for receiving or transmitting a signal," and shows an embodiment where an extension-conductor segment is connected by a via to the inductive elements. 582 patent at 3:27-32, 3:58-61, Fig. 1. The [redacted] in the DI Products appear to have this purpose—they [redacted]

CDX-0002C.321; JPX-0420C; CPX-0194C. Dr. Phinney offers credible and persuasive testimony here—that the

> A. Yes. So what I would really like to point out here is how I see this shape that's in the DI products as really precisely embodying this management of parasitics as it relates to the capacitor component and its connection to the, you know, how it – and its connection to the extension-conductor segments.
>
> . . . .
>
> And tracking the So it's like this shape has been sculpted precisely to track where . And that – this is like exactly embodying the idea of overlap, of the connecting – of the connecting segments by the extension-conductor segment and those two having a .

Hr'g Tr. (Phinney) at 196:16-197:14; *see id.* at 198:4 ("This is not a happenstance."). AMD does not present any technical considerations that refute these conclusions. *See generally* RRB at 89-93.

Accordingly, this limitation and all of claim 1 has been shown to be practiced by the DI Products.

2. Claim 2

Claim 2 of the 582 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Phinney, that the DI Products practice the limitations of claim 2 and cites the following imagery:

[redacted]

See CIB at 341 (citing CDX-0002C.337, 340); CPX-0197C; CPX-0194C; CPX-0120.2C; CPX-0119.3C; Hr'g Tr. (Phinney) at 208:15-210:20. AMD does not dispute practice of claim 2 apart from its dependency on claim 1. RIB at 215; RRB at 88-93. In light of the cited evidence and opinion, the additional elements of claim 2 are practiced by the DI Products, and the claim is therefore practiced.

3. Claim 3

Claim 3 of the 582 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Phinney, that the DI Products practice the limitations of claim 3 and cites the following imagery:

[redacted]

CIB at 341-342 (showing CDX-0002C.341); CPX-0197C; CPX-0194C; Hr'g Tr. (Phinney) at 210:21-211:12. AMD does not dispute practice of claim 3 apart from its dependency on claim 1. RIB at 215; RRB at 88-93. In light of the cited evidence and opinion, the additional elements of claim 3 are practiced by the DI Products, and the claim is therefore practiced.

[redacted]

4. Claim 4

Claim 4 of the 582 patent is presented above in connection with infringement. Realtek contends, as testified by Dr. Phinney, that the DI Products practice the limitations of claim 4 and cites the following imagery:

[redacted]

CIB at 342 (citing CDX-0002C.344; JPX-0420C; CPX-0179.2C); Hr'g Tr. (Phinney) at 211:13-212:22. AMD does not dispute practice of claim 4 apart from its dependency on claim 1. RIB at 215; RRB at 88-93. Nonetheless, there do not appear to be any connecting segments falling "between the two extension-conductor segments," and a [redacted], clearly fall outside the "first region" of claim 4. And Dr. Phinney makes little effort to show how the capacitor components of the DI Products satisfy both claim 1 and claim 4, other than to observe that [redacted] Hr'g Tr. (Phinney) at 212:16-22. So Realtek has not

shown that the identified capacitor components are "substantially limited to the first region," and claim 4 is therefore not practiced.

F. Validity

Respondents identify the following invalidity theories for the 582 patent:

Claims	Theory
1-4	Anticipated under 35 U.S.C. § 102 and/or rendered obvious under 35 U.S.C. § 103 by Qualcomm RBR1000 (JX-0745)
1-4	Anticipated under 35 U.S.C. § 102 and/or rendered obvious under 35 U.S.C. § 103 by Qualcomm RFR6122 (JX-0761)
1-4	Rendered obvious under 35 U.S.C. § 103 by Muh (JX-0174) in view of Niknejad (JX-0175)
1-4	Lack of written description under 35 U.S.C. § 112

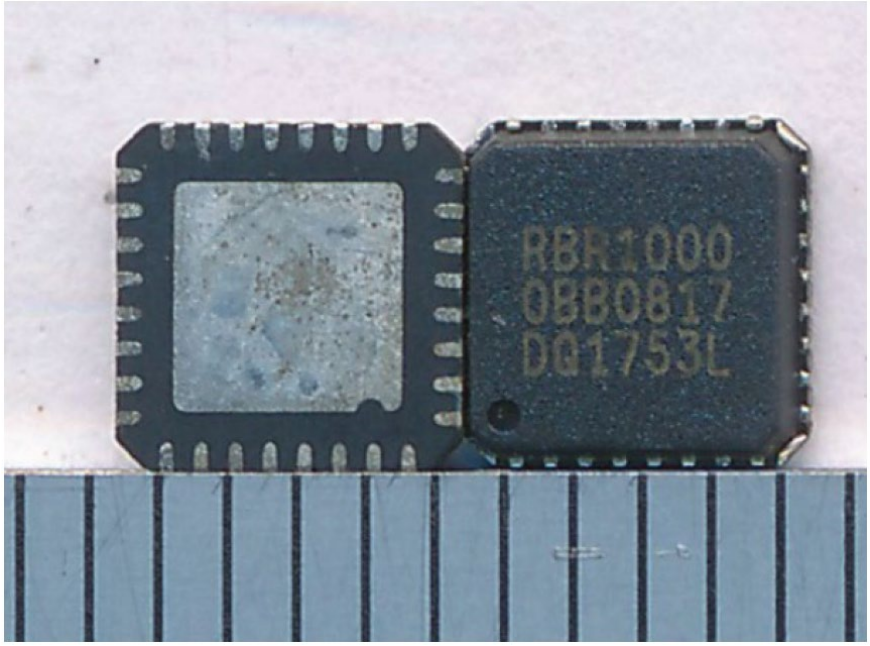
See generally RIB at 215-263. AMD identifies April 16, 2014 as the applicable priority date of the 582 patent, based on the filing of its Taiwanese application, to which Realtek offers no dispute. RIB at 7. As with the 245 patent, the parties dispute whether AMD has met its burden to show several references qualify as prior art. No party, however, disputes that because of this date, the current AIA version of the relevant statutes apply. *See id.* at 7, 7 n.4.

As for the Qualcomm RFR6122, this was addressed above in connection with the 218 patent and has been found to be prior art against that patent. The priority date for the 582 patent is several years after the 245 patent, so the RFR6122 qualifies under 35 U.S.C. § 102 (AIA). As for the publication, "mm-Wave Silicon Technology 60 GHz and Beyond" by Niknejad et al., this was published at least by 2008 (JX-0175.4), and its prior art status under 35 U.S.C. § 102 (AIA) is not challenged by Realtek. *See generally* CIB at 352-356; CRB at 85-89.

Realtek does dispute that the Qualcomm RBR1000 qualifies as prior art. AMD argues it was on sale or in public use well before April 16, 2014, thereby presumably qualifying under at least 35 U.S.C. § 102 (AIA). RIB at 8. Similar to its evidence for the Marvell 88W8686 and Qualcomm RFR6122, AMD presents a third-party technical report, sales records from Qualcomm, and other publications in support of RBR1000's prior art status. *See generally id.* at 11-14, 16-18; RRB at 2-5. Realtek opposes, largely on the grounds that AMD has failed to show that the specific chip compared against the asserted claims is the same chip documented in the other records. *See generally* CIB at 343-345; CRB at 78.

The evidence demonstrates a clear and convincing case that the Qualcomm RBR1000, as in the model analyzed by ICmasters and compared against the asserted claims in this investigation, was on sale or publicly used before April 16, 2014. AMD explains that the RBR1000 was announced in 2004 and was employed in wireless communication devices between 2006 and 2009. *See* RIB at 16-17. AMD provides sales records from Qualcomm showing t (*id.* at 13 (citing JX-0914C)), and the face of the actual chip torn down by ICmasters for this investigation is consistent therewith, having a manufacture date of the 17th week of 2008:

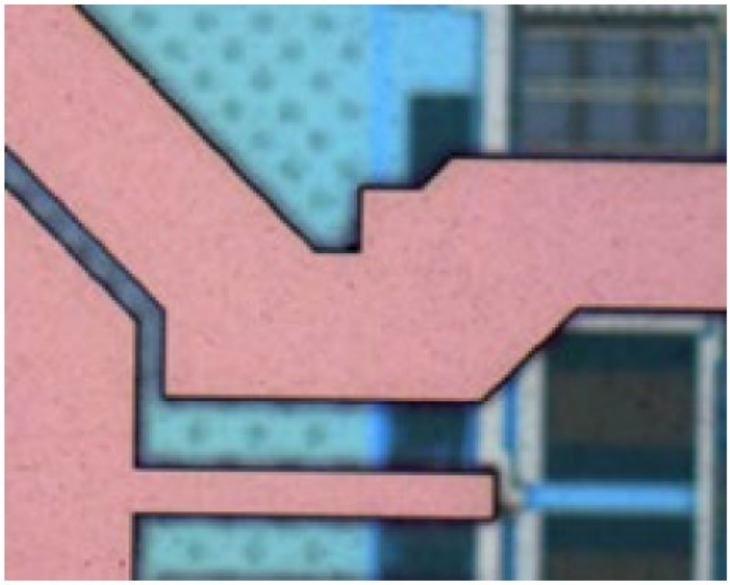
[redacted]

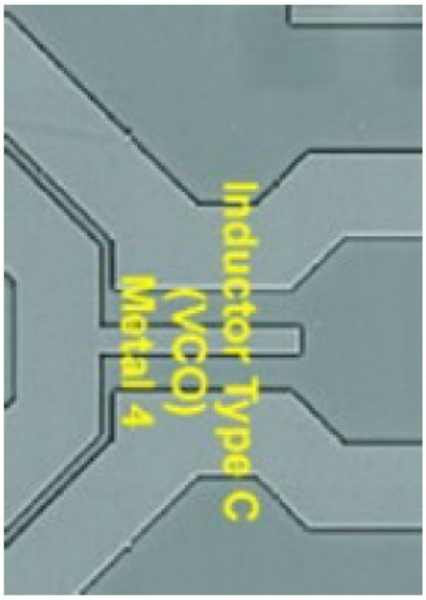


RIB at 18 (citing JX-0745.3; Hr'g Tr. (Subramanian) at 1002:6-23, 1004:23-1005:8). This is convincing evidence that the RBR1000, as in the model specifically analyzed here, was commercially available prior to 2014.

Realtek highlights a 2007 TechInsights report (similar to those referenced in the discussions of the RFR6122 and 88W8686 chips) which shows different shapes for two pairs of segments extending off the inductor coil as compared to the product analyzed by ICmasters:

[redacted]



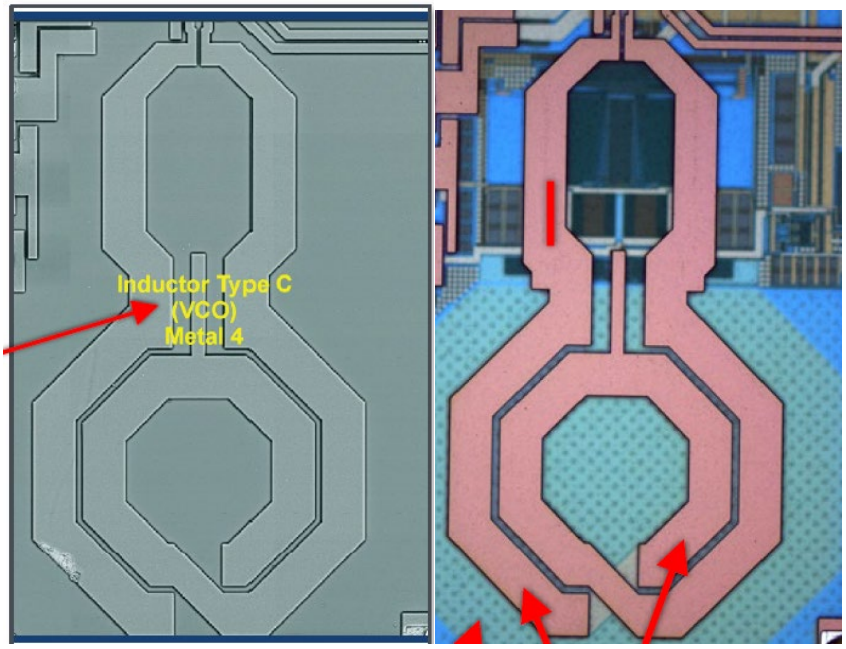


CIB at 343 (citing JX-0745.38 (left, ICmasters); JX-0628.38 (right, TechInsights));

id. at 344 (citing JX-0745.38 (left, ICmasters); JX-0628.38 (right, TechInsights)). Because of these differences, Realtek reasons "ICMasters and TechInsights analyzed two entirely different versions of the purported 'prior art product.'" *Id.* at 343.

These small differences are not enough to conclude that the TechInsights and ICmasters products are "entirely different," however. For example, every other feature in a zoomed-out view appears to be the same:

[redacted]



RRB at 96-97 (citing RDX-0004.15, 18); *compare* JX-0757.41 (2008 Portelligent Teardown Report, overall chip) *with* JX-0745.4 (ICmasters Report, overall chip). And Realtek has not otherwise explained why the differing contours might make a difference to the claims—it only uses them to conclude "[t]he two products named RBR1000 are undeniably different." CRB at 78; *see* RRB at 93. Moreover, Realtek provides no evidence or assertion that, assuming there is a meaningful difference between the products, it is the TechInsights version that accurately reflects all the [redacted] and not the ICmasters version. Regardless, no aspect of the TechInsights chip takes away from the fact that the ICmasters chip was produced in 2008 and was highly unlikely to have been completely concealed by Qualcomm all the way through April 14, 2014—as would be necessary to prevent its status as prior art against the 582 patent. 35 U.S.C. § 102 (AIA).

Accordingly, it has been shown that the Qualcomm RBR1000 is prior art to the 582 patent.

Realtek further disputes the status of a thesis entitled "Design of a FinFET static frequency divider and a millimeter-wave CMOS push-push VCO" written in the early 2000's by Matthew

Muh, an electrical engineering master's candidate at the University of California, Berkeley ("Muh"). *See* CIB at 352-53; RIB at 22; JX-0174. AMD contends:

> Any doubt concerning the Muh thesis's public accessibility before the 582 patent filing date was resolved by AMD's expert Dr. Sylvia Hall-Ellis. Her testimony confirmed that the Muh thesis was assigned a MARC record on July 8, 2005, and was publicly accessible through at least OCLC online searching by that date. Tr. (Hall-Ellis) at 1171:23-1176:13; 1180:23-1181:25; 1186:8-1187:17; RX-1770; RDX-0012.2-5, .12; JX-0013.80:10-91:3. Moreover, the Muh thesis was available shortly thereafter through Google Scholar, using key words from the title such as "VCO" and "FinFET." Tr. (Hall-Ellis) at 1181:8-25; RDX-0012.12. Realtek offered no testimony, expert or otherwise, to rebut Dr. Hall-Ellis's analysis.
>
> . . . .
>
> As Dr. Hall-Ellis testified, once the Muh thesis was cataloged on July 8, 2005, using the MARC standard, it was discoverable online through OCLC or any library that was MARC-compatible. It also at that point was available through an internet search on Google and Google Scholar. The Muh thesis title is descriptive and includes the term "VCO," which is directly pertinent to the 582 patent. *See* Order No. 25 at 10. Thus, as of July 8, 2005, a skilled artisan using reasonable diligence could have found the Muh thesis using search terms like VCO.

RIB at 22-24; RRB at 5 ("Dr. Hall-Ellis provided unrebutted testimony that by 2005, a POSITA could have located Muh using MARC records *or* through a Google search (*e.g.*, Google Scholar).") (emphasis in original). AMD argues this meets the "sufficiently accessible" standard under Section 102. RIB at 23 (citing *Voter Verified Inc. v. Premier Election Solns., Inc.*, 698 F.3d 1374, 1380 (Fed. Cir. 2012)).

Realtek disagrees, stating "[a]t trial, the evidence showed that even a person having greater than ordinary skill in the art would not have relied upon MARC records to identify any reference." CIB at 352 (citing Hr'g Tr. (Prucnal) at 1153:7-11). Realtek continues, "[o]ther than the indexing (which AMD's evidence simply establishes that a POSITA and a member of the relevant public would not have used), AMD provides no other evidence that Muh was available. . . . Dr. Hall-Ellis confirmed that proper indexing by subject heading is necessary to perform a search using

MARC data." *Id.* at 352-353 (citing Hr'g Tr. (Hall-Ellis) at 190:1-1191:16); CRB at 85 ("There is no evidence that an *interested researcher* would have known how to use the MARC records AMD relies [on].").

AMD has not met its burden. Dr. Hall-Ellis's testimony would be sufficient to show Muh was more likely than not to be publicly accessible, but it is too generalized for a clear and convincing standard. For example, as it concerns Google Scholar, AMD argues "once the Muh thesis was cataloged on July 8, 2005, using the MARC standard . . . It also at that point was available through an internet search on Google and Google Scholar." RIB at 24. Yet Dr. Hall-Ellis did not offer this opinion. Rather, she loosely testified, "[i]t was also later available in Google Scholar" and implied that she had used that tool to find the reference as part of her efforts for this investigation. *See* Hr'g Tr. (Hall-Ellis) at 1181:5-18. Then she opined that Google came into existence in about 1998 and Google Scholar "about six years later." *Id.* at 1181:19-22. Put together, these are not effective as an opinion that prior to April 16, 2014, Muh would have been indexed by Google Scholar and therefore locatable by persons interested in the field of art and running searches in it. The Federal Circuit has explicitly identified this additional fact as material to inquiries involving Google. *Voter Verified*, 698 F.3d at 1381 ("On the other hand, although commercial internet search engines were available by 1999, the record is devoid of evidence indicating whether or not the Risks Digest website had been indexed by any such services as of the critical date. The district court credited each of the preceding factual assertions, as it was entitled to do."); *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1349-50 (Fed. Cir. 2016) ("The record is devoid of any evidence that a query of a search engine before the critical date, using any combination of search words, would have led to Ratsimor appearing in the search results.").

As it concerns the library belonging to the University of California at Berkeley, Dr. Hall-Ellis's testimony is, again, too generalized to meet AMD's clear and convincing burden. AMD contends "[Muh] was publicly accessible through at least OCLC online searching by that date." RIB at 22. Yet Dr. Hall-Ellis did not offer this opinion. She testified that "OCLC is the largest bibliographic database in the world" and is a "consortium of libraries around the world national libraries, public libraries, academics, special research, and others." Hr'g Tr. (Hall-Ellis) at 1173:7-18. And she testified that a person can access MARC records from an OCLC member library as well as something called WorldCat, "the public version of the OCLC bibliographic database." *Id.* at 1174:13-1175:2, 1175:13-20. But she did not offer the simple opinion that all of this would have been available and established prior to the 2014 critical date, such that Muh would have been locatable. She also offered no information on the mechanics of running an OCLC search as it pertains to a MARC record, which has only author and title information (*i.e.*, no subject index).

Thus, all the record shows is that Muh was received in 2005 by the university's library and a MARC record was created with author's name, university program, and thesis title (RX-1770), and Google Scholar started to exist around the same time. There are no additional facts to support a clear and convincing case that persons of ordinary skill exercising reasonable diligence could have accessed the reference—facts such as an awareness of those persons to search the records of Berkeley as a prominent electrical engineering program (*Voter Verified*, 698 F.3d at 1381 ("the uncontested evidence indicates that a person of ordinary skill interested in electronic voting would have been independently aware of the Risks Digest as a prominent forum for discussing such technologies"); *Blue Calypso*, 815 F.3d at 1349-50 ("there was no evidence that the ordinarily skilled artisan would know of Dr. Ratsimor's personal webpage or its web address.")), or that the thesis was downloaded and viewed by persons outside of the department's review team (*id.* at 1350

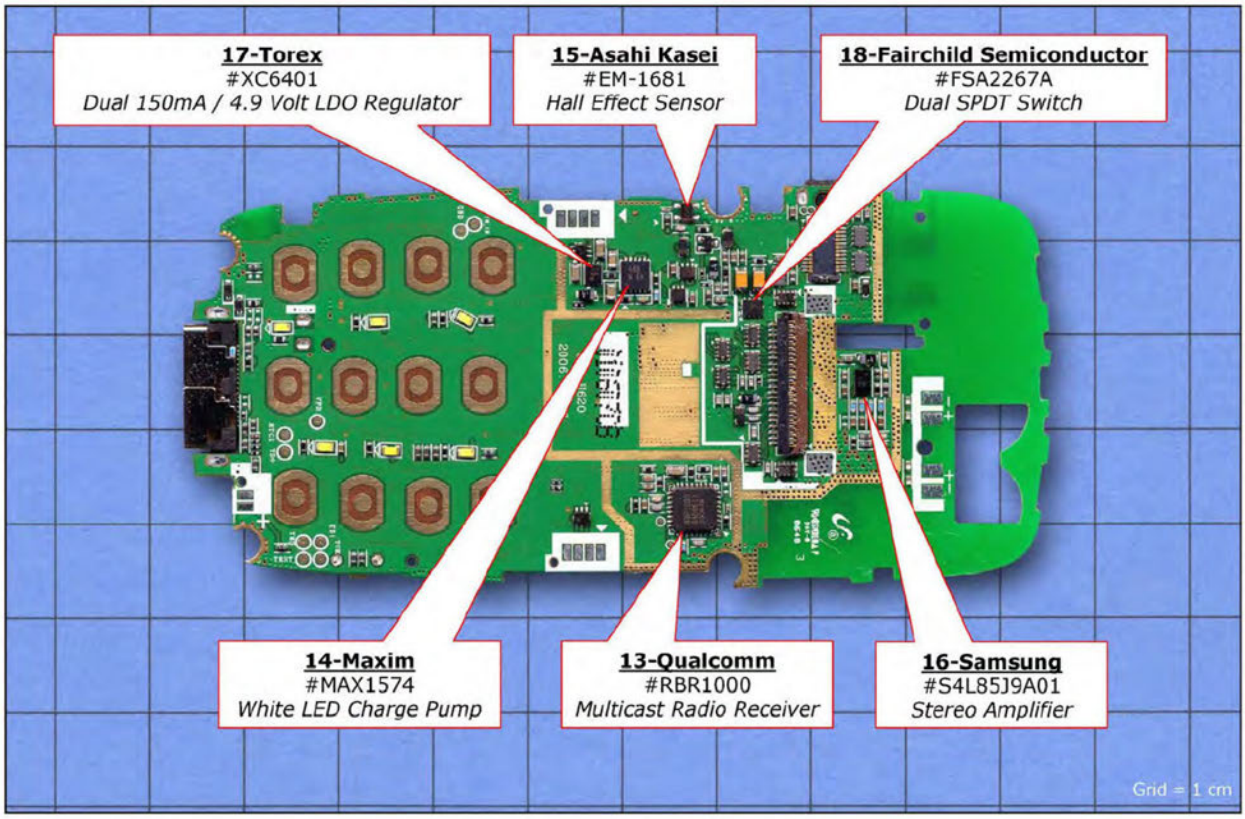
("Even if we assume that Ratsimor was available online on Dr. Ratsimor's personal page before the critical date, Groupon does not point to any evidence indicating that Ratsimor was viewed or downloaded"); *Application of Bayer*, 568 F.2d 1357, 1361 (C.C.P.A. 1978) ("Accessibility to appellant's thesis by the three members of the graduate committee under the circumstances of the present case does not raise such a presumption.")). And although the 582 patent uses the term "VCO" as an abbreviation for "voltage-controlled oscillator," the overall subject matter of the 582 patent is LC resonant circuits, not VCOs, so it is not clear that a skilled artisan would have been alerted to Muh's relevance based on the term "VCO" in its title, or based on the even more general term "FinFET." 582 patent at 1:34. AMD has thus not presented clear and convincing evidence that reasonable diligence would have granted a member of the public interested in the art access to Muh at the relevant time.

Accordingly, Muh has not been shown to be prior art to the 582 patent under 35 U.S.C. § 102 (AIA), and the obviousness combination of Muh and Niknejad will not be considered.

1. Qualcomm RBR1000

AMD states that the RBR1000 was announced by Qualcomm in 2004 as a "'radio receiver'" which "'seamlessly interfaces with both CDMA2000 and WCDMA chipsets in Qualcomm's Enhanced Multimedia Platform.'" RIB at 16 (citing JX-0578.29). AMD cites its 2006 user guide, further describing the chip as a [redacted] *Id.* at 16-17 (citing JX-0779C.6. AMD adds that the chip was "included in the LG Voyager VX1000 'cell phone with TV' in 2008, and the Samsung SCH u620 'camera/TV phone' available through Verizon in 2007." *Id.* at 17 (citing JX-0757; JX-0758). An image taken from a teardown report shows the location of the chip within the Samsung device:

[redacted]



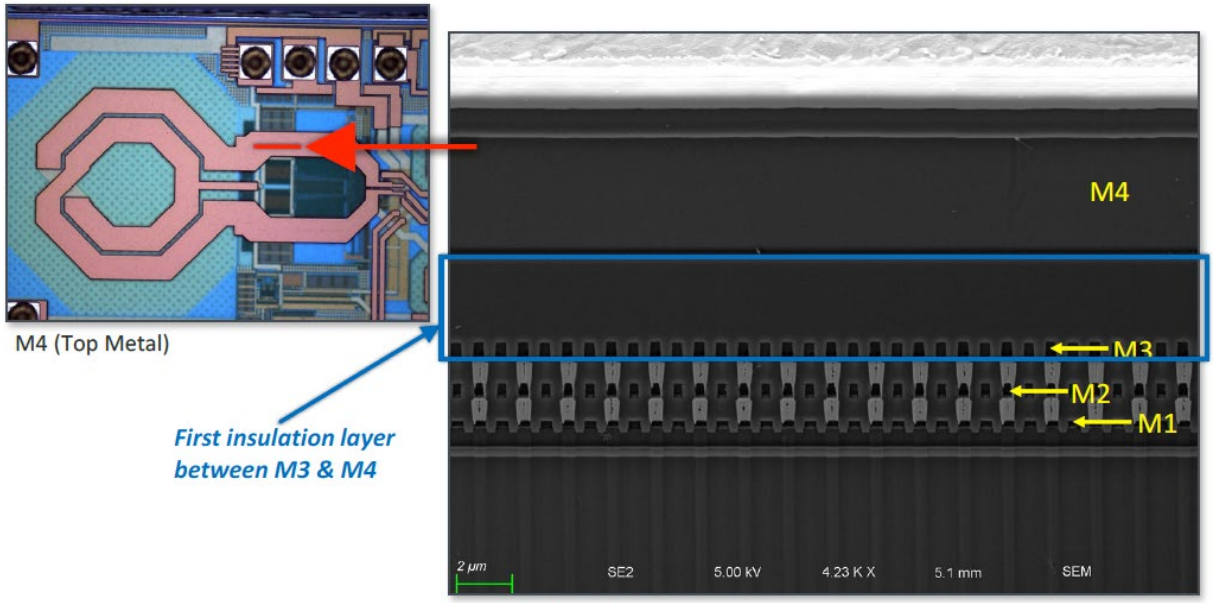
JX-0758.75. AMD contends the asserted claims of the 582 patent are invalid as anticipated by the RBR1000. *See generally* RIB at 216-233. AMD also contends, summarily, that the RBR1000 invalidates under obviousness (RIB at 216; RRB at 93) but includes no supporting argument, so it has not met its burden under Section 103. For the reasons discussed below, AMD has shown claims 1-3, but not claim 4, to be anticipated.

a. Claim 1

Claim 1 is presented above. AMD contends each limitation is present in the RBR1000, thus anticipating the claim. As for the preamble, "[a] semiconductor device with an inductor-capacitor (LC) resonant circuit," AMD suggests it is not limiting. RIB at 219; RRB at 95. Regardless, AMD looks to the testimony of Dr. Prucnal and a TechInsights report which characterizes the circuit as "an LC tank-based oscillator." RIB at 219 (citing JX-0628.78; Hr'g Tr. (Prucnal) at 1028:22-1030:15).

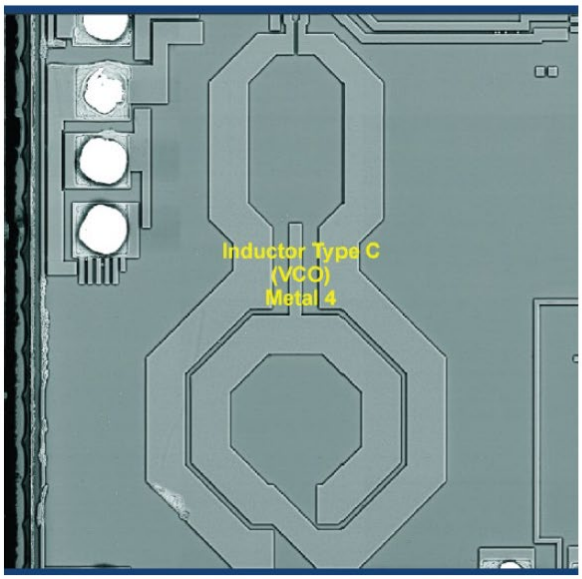
[redacted]

For limitation [1a], AMD contends there is a "first insulation layer" "between metal layers M3 and M4" (*e.g.*, from bottom of M3 to bottom of M4), as shown below in images from the ICmasters report:

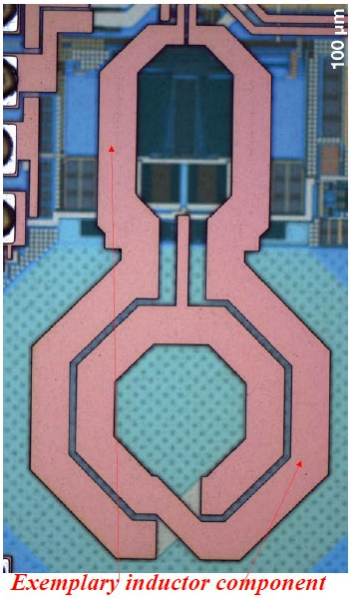


SEM Cross-Section

RIB at 220-221 (citing Hr'g Tr. (Prucnal) at 1030:18-1031:6; RDX-0004.16; JX-0745.7). For limitation [1b], AMD argues there is a "tank inductor" as in the following images:



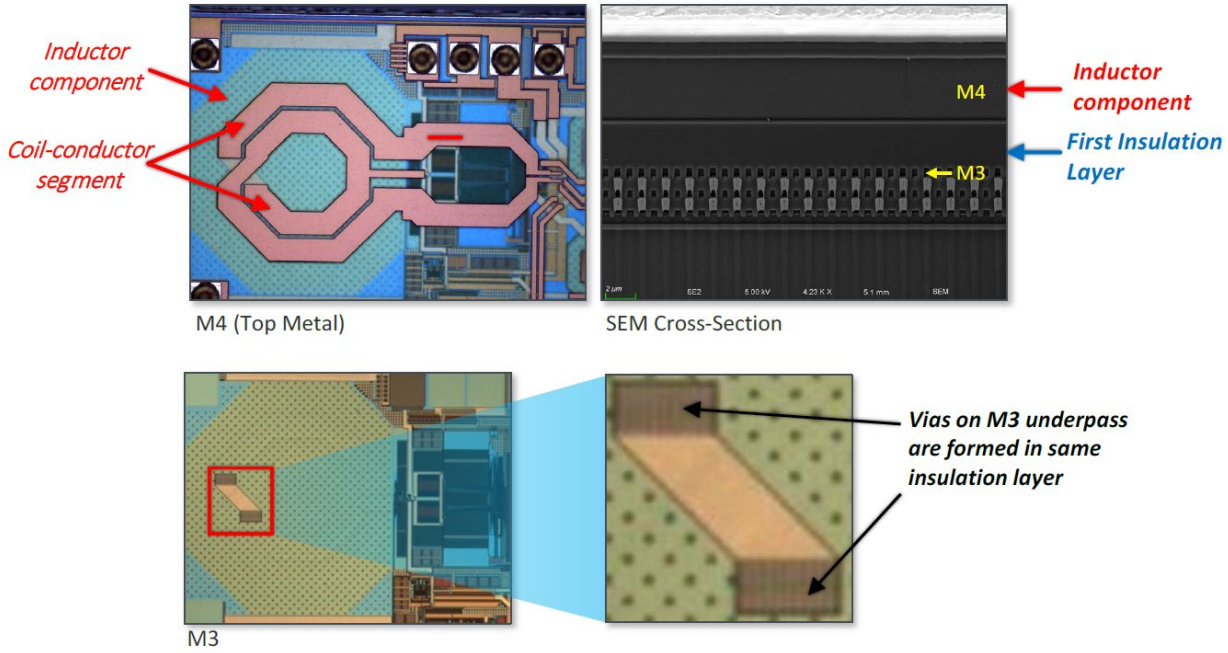
Photograph 2.3.9: SEM image of inductor type C- metal 4.



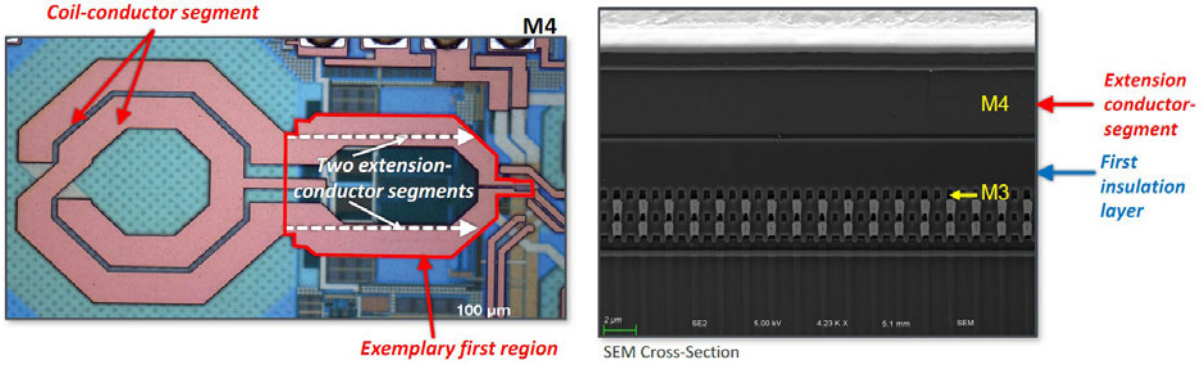
Exemplary inductor component

Id. at 221 (citing Hr'g Tr. (Prucnal) at 1031:19-1032:7; JX-0628.31, 78-80; JX-0745.31).

For limitation [1c], AMD contends, "[t]he inductor includes a coil-conductor segment formed in M4 on a surface of the first insulation layer between M3 and M4. This coil-conductor segment is part of the inductor that forms an inductor coil," and provides the following imagery:

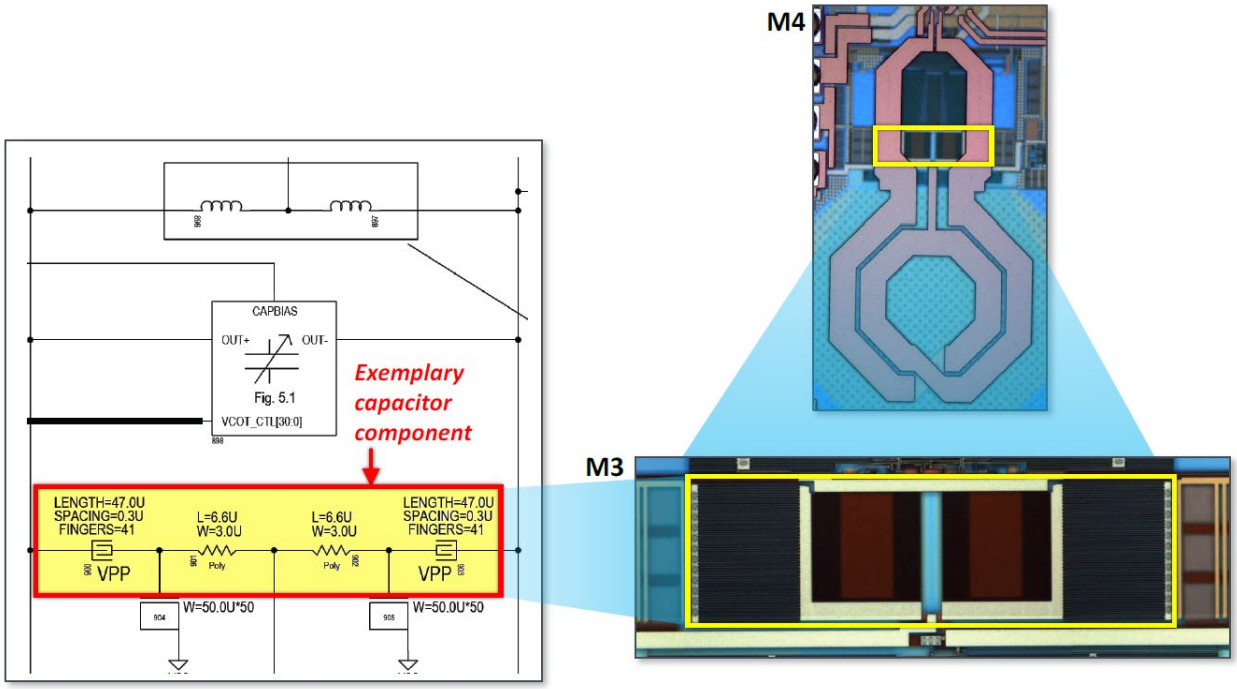


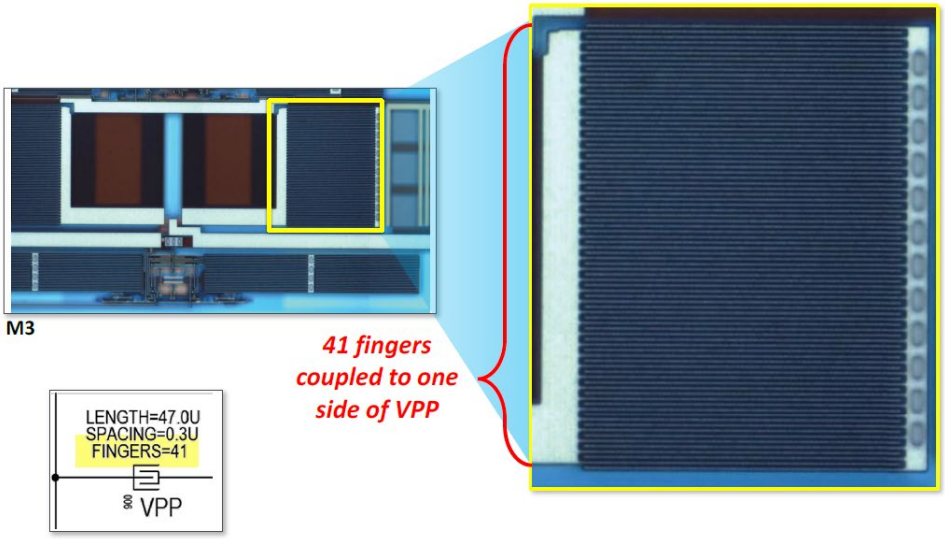
RIB at 222 (citing Hr'g Tr. (Prucnal) at 1031:7-1033:6; RDX-0004.18; JX-0745.7, 28). For limitation [1d] and the "extension-conductor segments," AMD explains "a first region is defined by the two extension-conductor segments and the coil-conductor segment" as in the imagery below:



RIB at 223-224 (citing Hr'g Tr. (Prucnal) at 1033:25-1035:3; RDX-0004.20; JX-0745.7-8).

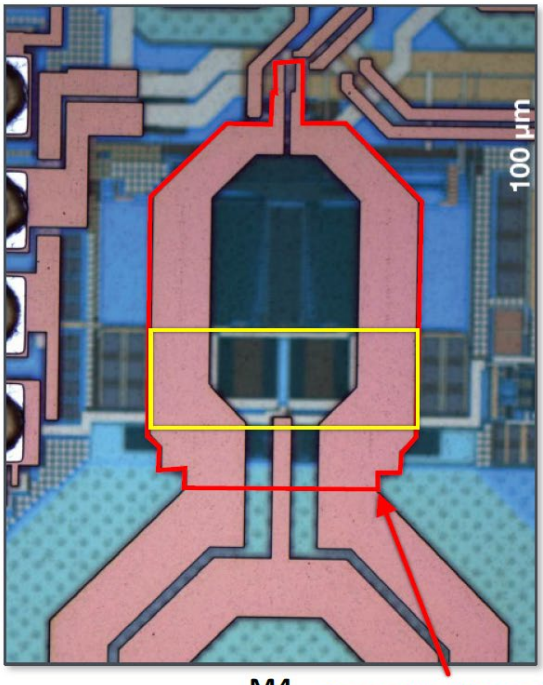
For limitation [1e], and the "capacitor component," AMD highlights several regions. AMD contends "RBR1000 includes VPP capacitors, two of which are shown below with each VPP capacitor having 41 fingers on one side of the capacitor ('fingers=41')" and points to excerpts from both the TechInsights and ICmasters reports:



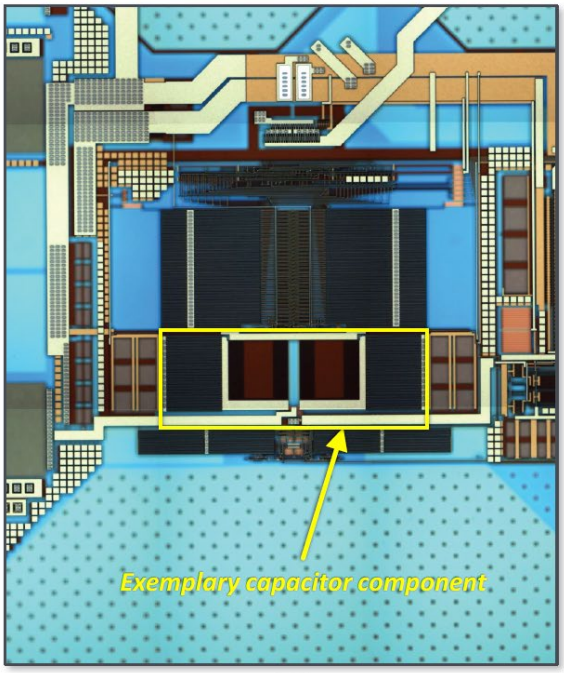


[redacted]

RIB at 224-225 (citing Hr'g Tr. (Prucnal) at 1038:11-1039:25; JX-0628.38-39, 80; JX-0745.31, 33, 34; RDX-0004.23, 24). AMD then provides the following two images to show the capacitor component "arranged corresponding to the first region":



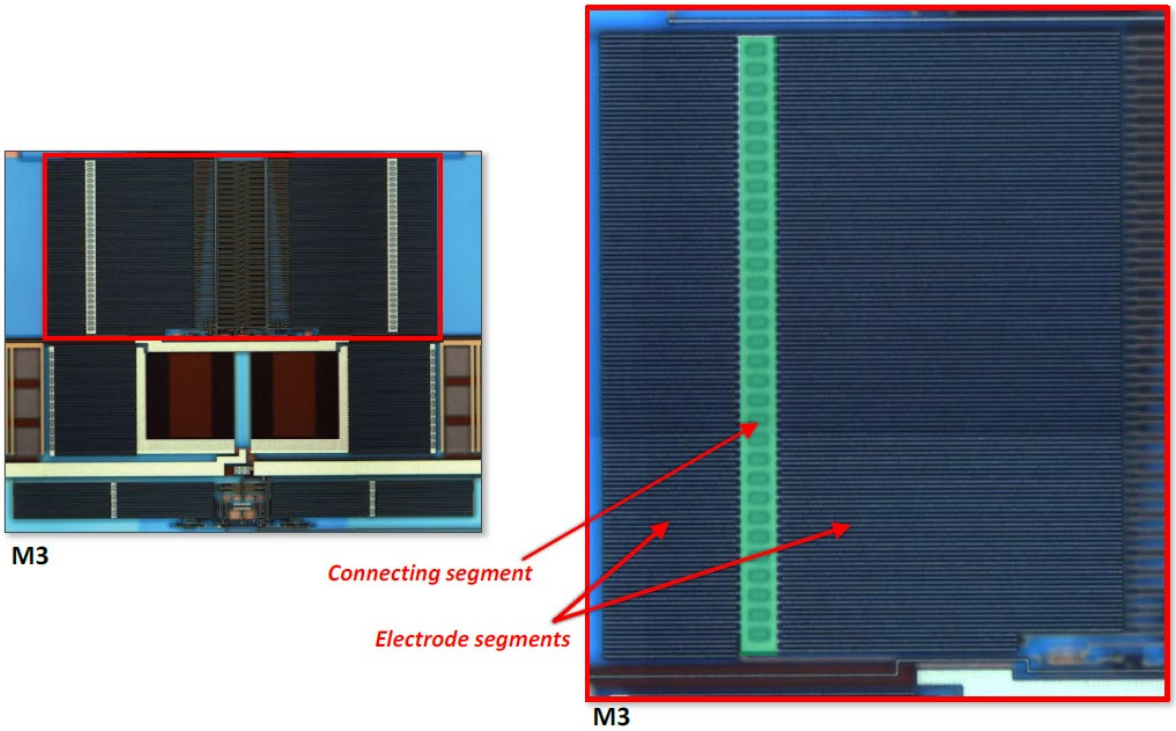
M4 *Exemplary first region*

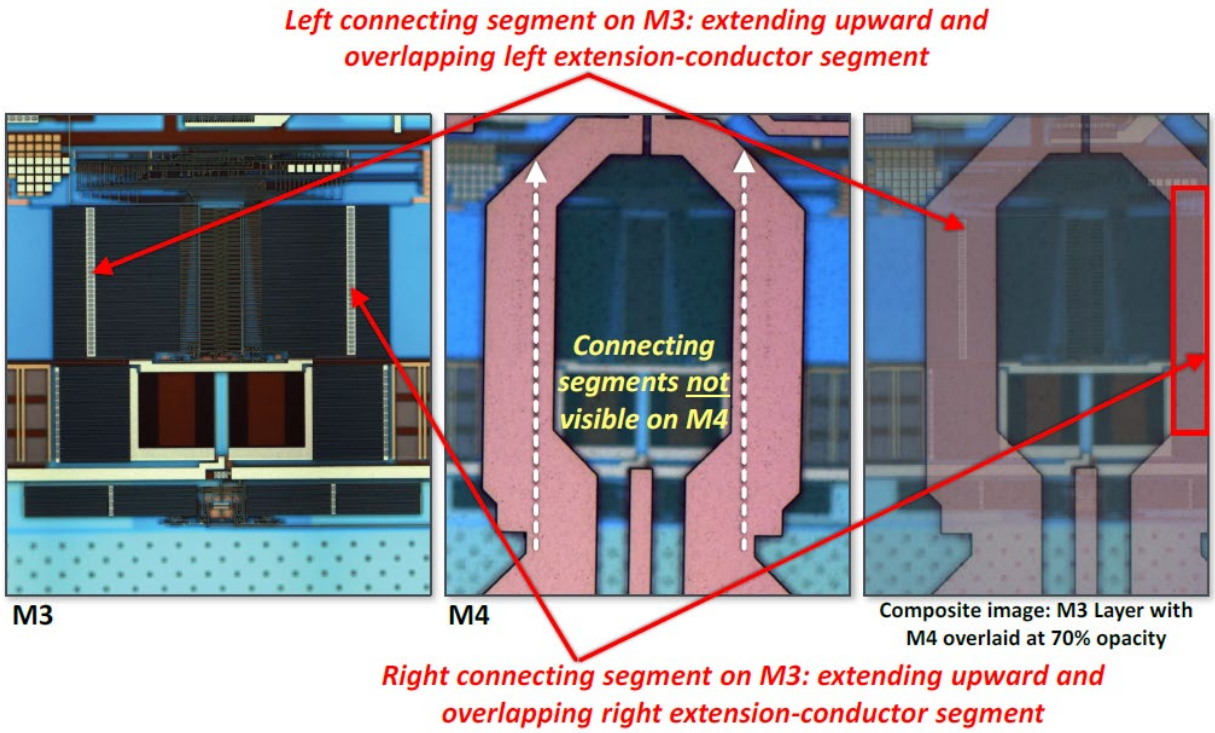


M3

RIB at 226 (citing Hr'g Tr. (Prucnal) at 1040:5-1041:15; RDX-0004.25; JX-0745.31, 33). In a later claim limitation, AMD acknowledges the presence of additional capacitors belonging to the "capacitor component," which are also arranged corresponding to the first region:

[redacted]

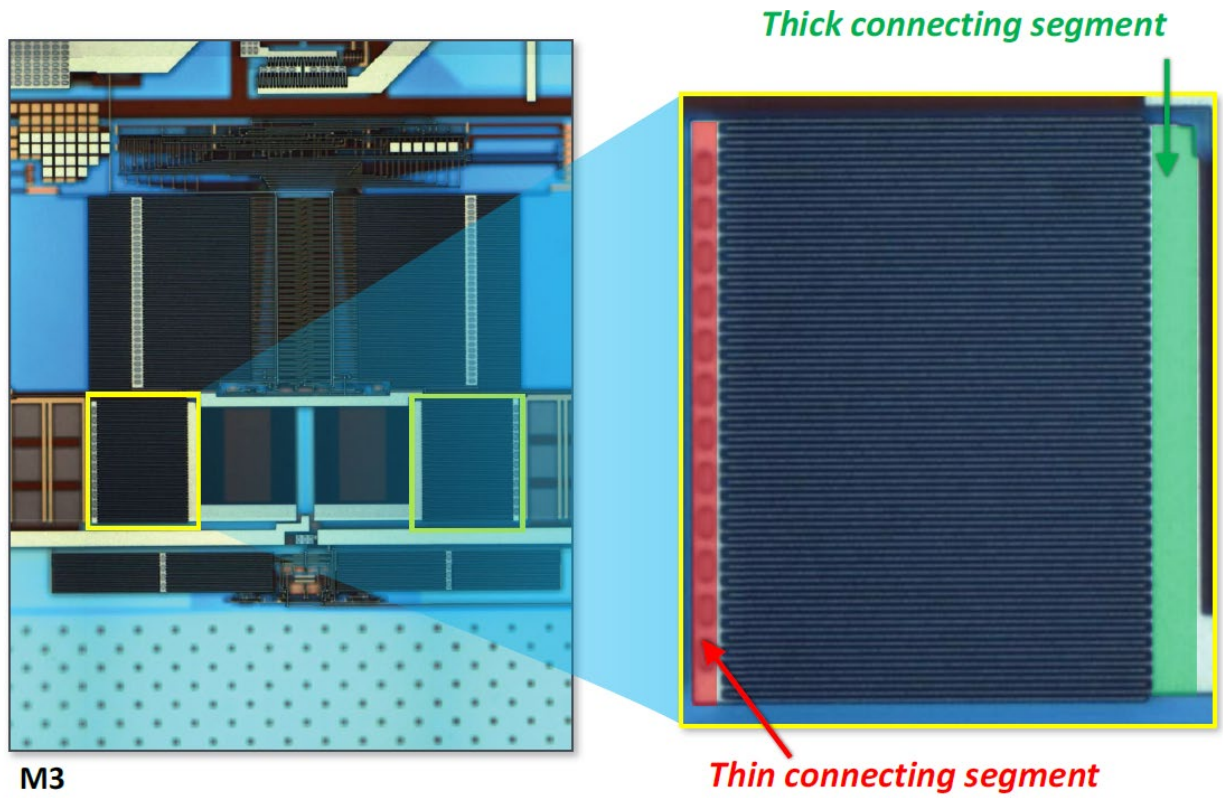


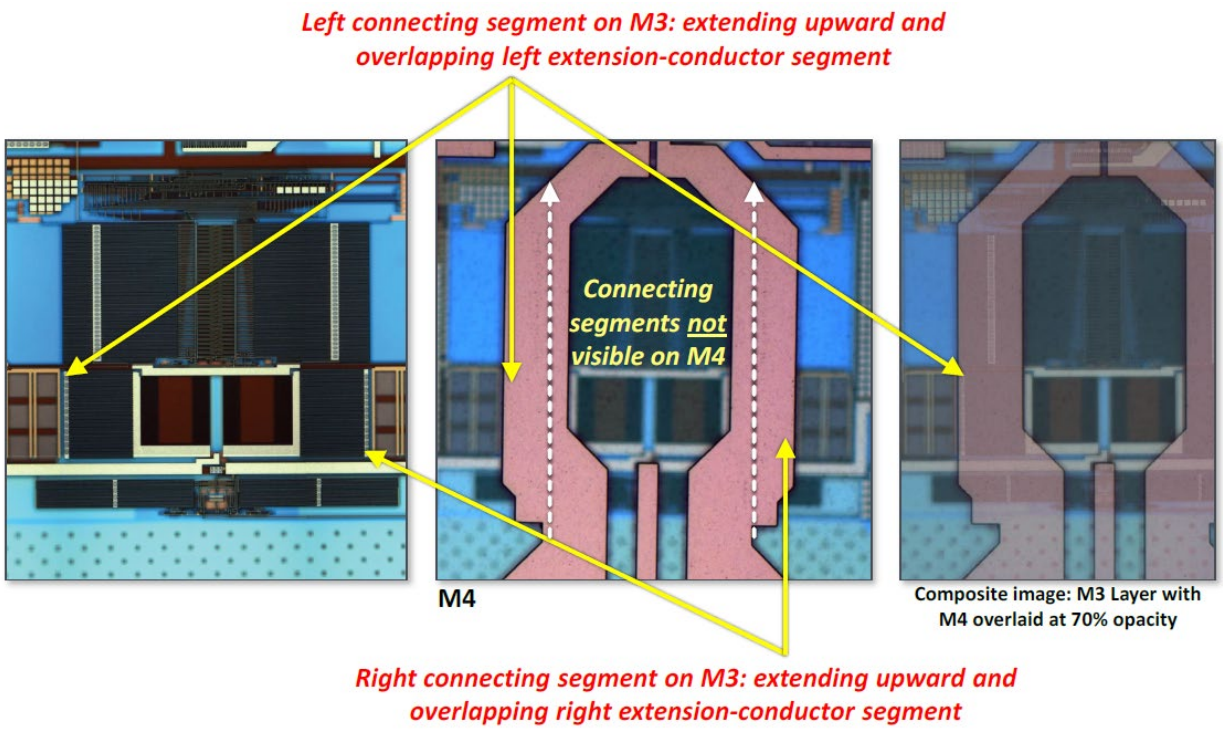


RIB at 230-231 (citing Hr'g Tr. (Prucnal) at 1045:7-1047:9; JX-0628.80-82; JX-0745.16, 31, 33-34; RDX-0004.30, 31).

[redacted]

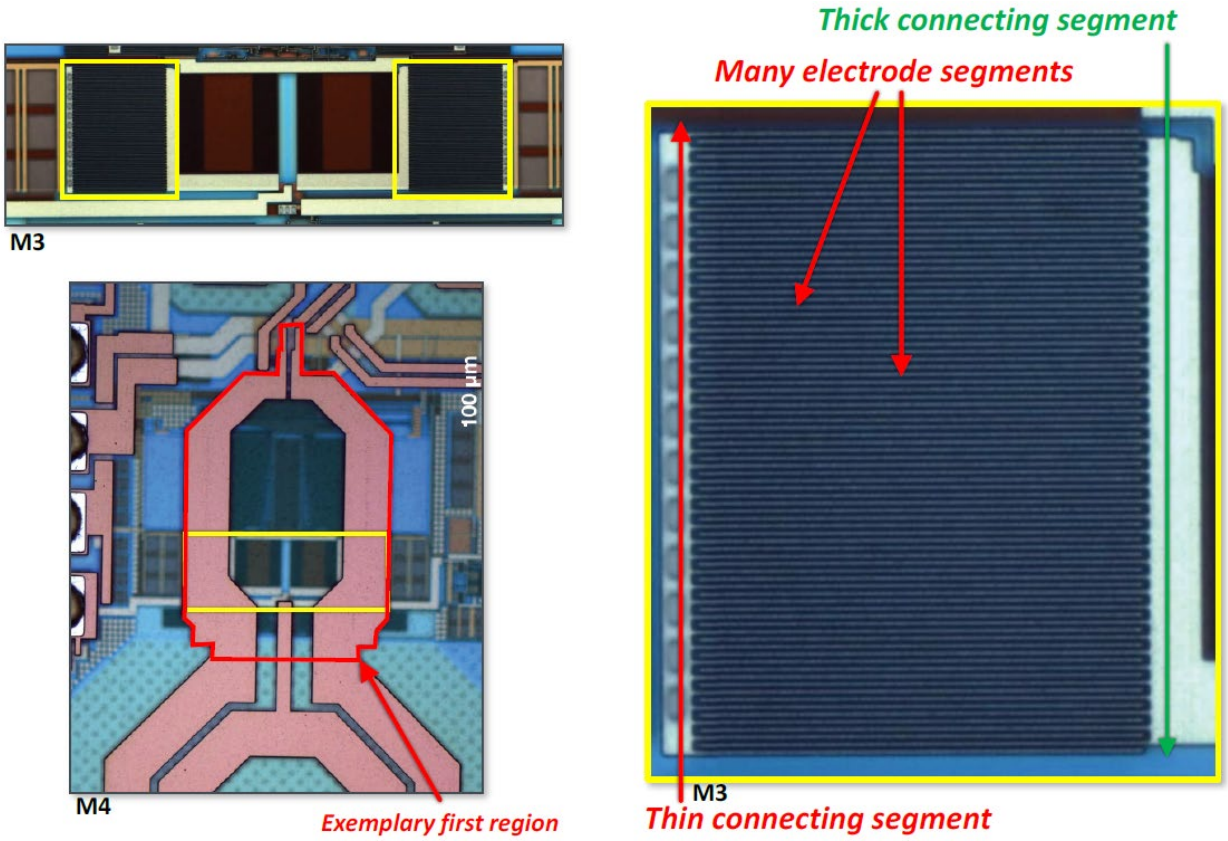
For limitation [1f], AMD provides the following annotated imagery taken from the ICmasters report:





RIB at 227-228 (citing Hr'g Tr. (Prucnal) at 1041:19-1043:22; RDX-0004.27, 28; JX-0745.16, 31, 33). AMD adds, "[i]n the capacitor component comprising two symmetrical VPP capacitors shown above, consistent with the ALJ's claim construction, a left connecting segment is overlapped by the left extension-conductor segment, and a right connecting segment is overlapped by the right extension-conductor segment, both in a vertical direction." *Id.* at 229 (citing Hr'g Tr. (Prucnal) at 1042:9-1044:6).

For limitation [1g], AMD contends the images below show "two VPP capacitors ha[ving] a plurality of electrode segments ('fingers or the teeth of the comb') located below the first region":



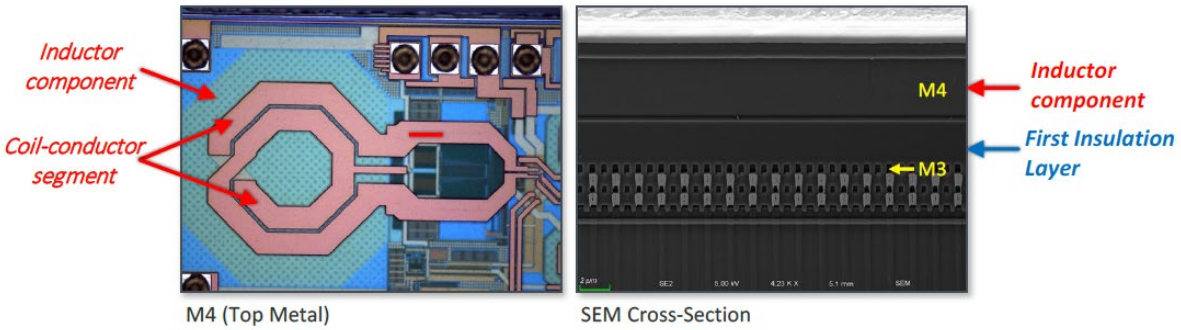
RIB at 229-230 (citing Hr'g Tr. (Prucnal) at 1044:7-1045:8; RDX-0004.29; JX-0745.31, 33-34). These limitations are present in the RBR1000 as alleged.

Realtek offers a few points in opposition which are not persuasive. First, Realtek contends that the preamble, "an inductor-capacitor (LC) resonant circuit" has not been shown because there is no evidence of a "connection between the inductor component (M4) and the capacitors located at M3 and M2." CIB at 344 (citing JX-0745.7); CRB at 80-81. But claim preambles are generally non-limiting (*Am. Med. Sys. V. Biolitec, Inc.*, 618 F.3d 1354, 1358 (Fed. Cir. 2010)), and Realtek did not argue in its pre-hearing brief why this preamble would be limiting under the relevant standards (*see* CPB at 191-192, 227-228, 246-248). That argument is thus waived under Ground Rule 9.2. Order No. 2. Regardless, the circuit schematic from the TechInsights report shows connectivity between the inductor component and VPP capacitor components (JX-0628.80) and Dr. Phinney offered no expert testimony that the two were unconnected.

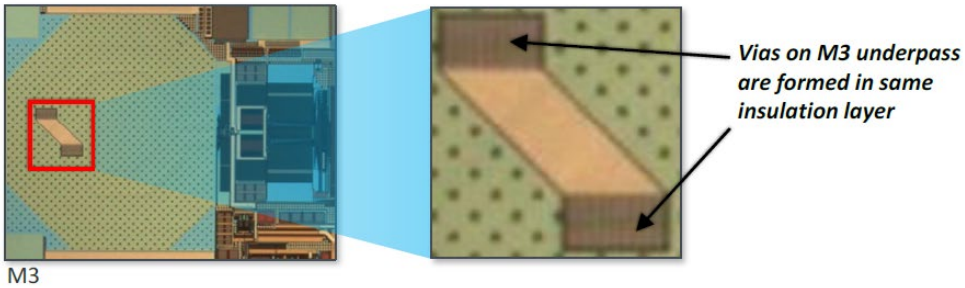
Realtek next argues that AMD has filed to show an insulation layer below the coil-conductor segment of the inductor as recited via the claim limitation, "a coil-conductor segment, located on a surface of the first insulation layer." CIB at 345. Realtek is correct that the single cross-sectional photograph provided by AMD is taken from within the extension-conductor segments and not the coil-conductor segments (*id.* (citing JX-0745 at 7-8)), yet AMD clearly and convincingly explains that vias stretching between the M3 and M4 layers, which connect windings of coil-conductor segments, must be formed in an insulation layer thereby satisfying the limitation:

[redacted]

- Entire inductor component, including its coil-conductor segment, has a first insulation layer under it:



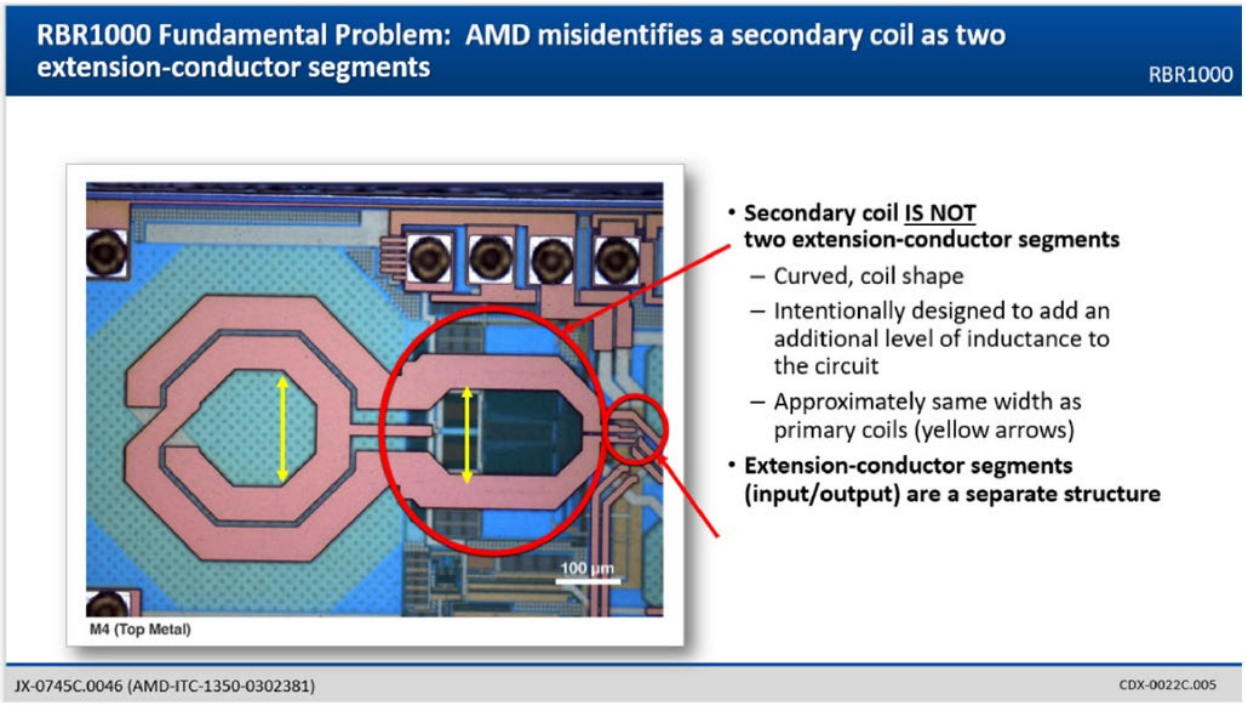
- Staggered part of inductor component with underpass:



RRB at 96 (citing RDX-0004.18; JX-0745.7, 28). Added to this is the testimony of Dr. Prucnal who acknowledged the missing cross-sectional photograph but otherwise stated that the same insulation layer existing between M3 and M4 under the extension-conductor segments exists under the coil-conductor segments. Hr'g Tr. (Prucnal) at 1031:7-1033:6. Realtek, on the other hand, makes its argument without any support from Dr. Phinney (*see* CIB at 345).

Realtek lastly argues that "the capacitor component is not substantially overlapped with the coil-conductor segment" is not met in the RBR1000. CIB at 346-347; CRB at 78-80. The premise for this argument is that "AMD mis-identifies a coil as the alleged extension-conductor segment" and because that segment overlays the capacitor component, the element is not met. CIB at 346. Realtek asserts the segments constitute a "sister coil" because they are similar in size and shape to the primary coil:

[redacted]



CRB at 79 (citing CDX-0022.105; Hr'g Tr. (Phinney) at 1247:13-1249:5).

This position, which is supported by the opinion of Dr. Phinney, is not convincing for four reasons. One, the segments bear the same hallmarks as the DI Products as being intentionally shaped to match the positions of the capacitor circuitry below, which indicates their purpose is to serve as a connection to those circuits. RDX-0004.27, 28; JX-0745.16, 31, 33. Two, as noted by AMD, the schematic drawing from TechInsights models the circuit and identifies the "center tap" with "Turns: 2.0" and outer diameter of 400 microns (*i.e.*, the primary coil) as the only inductor. RIB at 218 (citing JX-0628.80).

Three, it is difficult to believe the extension segments are intended and do create an inductance as windings just based on appearances. As shown in Dr. Phinney's demonstrative above (CDX-0022.105), the primary coil is situated on a conspicuously blank insulating background, while the alleged "sister coil" is located above a plethora of capacitors and other switches. Dr. Phinney himself testified that this causes problems "because of the flux in that sister

coil. And that goes down into the substrate and would introduce additional loss and so forth." Hr'g Tr. (Phinney) at 1248:23-1249:1. While prior art references such as Daley show the possibility of designers overlapping sensitive components in this way (JX-1017 at Fig. 1), the primary coil's plain background demonstrates appreciation and intentional avoidance of this problem. This makes it less likely that the extensions contribute to inductance. And Dr. Phinney provides no technical explanation or experimental results as to why the segments do so contribute.

And four, it should be respected that the claims only require the capacitor component to be not substantially overlapped with "*the* coil-conductor segment," not any and all coil-conductor segments. 582 patent at cl. 1 (emphasis added). So even if a "sister coil" existed, it is irrelevant when a separate "coil-conductor segment" exists with no overlap. And the identified wires are conductive segments that extend in a direction, which satisfies the plain and ordinary meaning of "extension-conductor segments."

Accordingly, all limitations of claim 1 are met in the Qualcomm RBR1000 and claim 1 is invalid as anticipated under 35 U.S.C. § 102 (AIA).

b. Claim 2

As for claim 2, AMD contends "[t]he capacitor component (M3 portions of VPP capacitors) is sandwiched between the first insulation layer (between M4 and M3) and the second insulation layer. . . . RBR1000's VPP capacitor M2 portions comprise an electronic component that is arranged corresponding to the first region in an embedded manner on a surface, opposite to the capacitor component, of the second insulation layer," as shown below:

[redacted]

RIB at 232 (citing Hr'g Tr. (Prucnal) at 1047:15-1049:1; RDX-0004.32; JX-0745.7, 21-23; JX-0628.38-39). Realtek does not dispute claim 2 (*see* CIB at 343-347; CRB at 78-81) and it is met as alleged.

Accordingly, claim 2 is invalid as anticipated over the Qualcomm RBR1000.

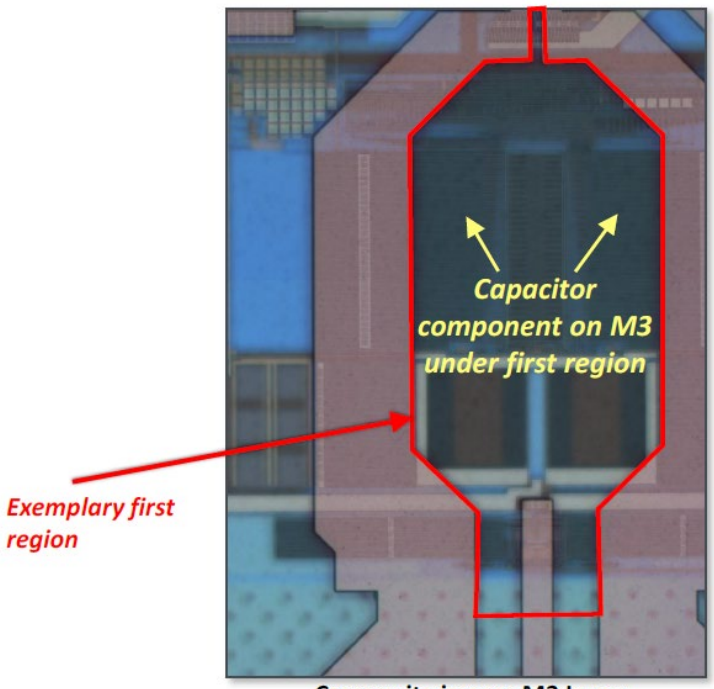
c. Claim 3

As for claim 3, AMD states, "[t]he electronic component is a capacitor component (VPP capacitor M2 portions)." CIB at 232 (citing Hr'g Tr. (Prucnal) at 1048:20-1049:1; JX-0745.7). Realtek does not dispute claim 3 (*see* CIB at 343-347; CRB at 78-81) and it is met as alleged.

Accordingly, claim 3 is invalid as anticipated over the Qualcomm RBR1000.

d. Claim 4

As for claim 4, AMD states, "[t]he invalidity analysis above still applies when the first region is defined between the two extension-conductor segments," and provides the following image:



Composite image: M3 Layer
with M4 overlaid at 70% opacity

RIB at 233 (citing Hr'g Tr. (Prucnal) at 1049:16-1050:13; RDX-0004.33; JX-0745.16). As determined above, "a capacitor component, arranged corresponding to the first region" means that the capacitor component must be substantially limited to the "first region," which allows for a limited amount of overreach beyond the "first region." But in the RBR1000, large swathes of the "capacitor component," including the connecting segments, extend past the inner boundary of extension-conductor segments. So although Realtek does not otherwise dispute claim 4 (*see* CIB at 343-347; CRB at 78-81), AMD has not carried its burden here.

Accordingly, claim 4 is not invalid as anticipated over the Qualcomm RBR1000.

2. Qualcomm RFR6122

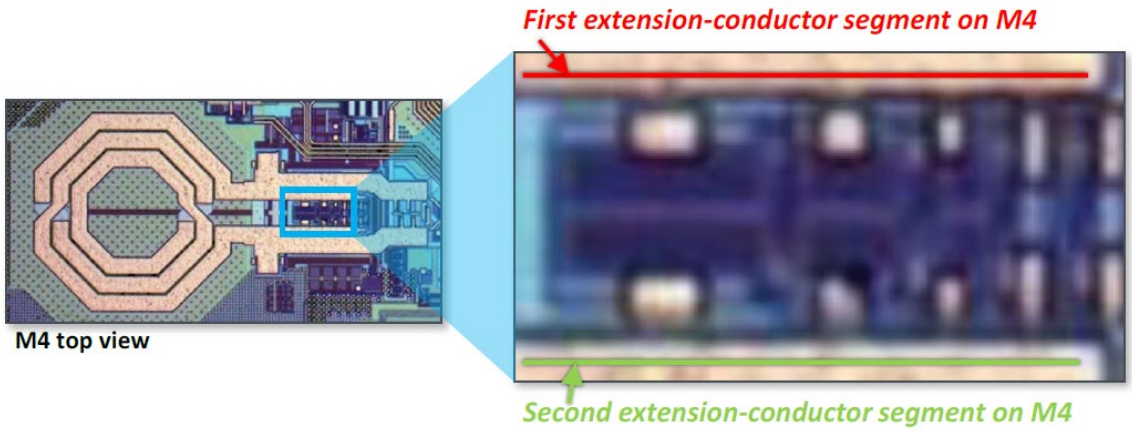
The Qualcomm RFR6122 product was introduced in connection with the invalidity of the 218 patent, above. AMD contends the asserted claims of the 582 patent are invalid as anticipated by the RFR6122. *See generally* RIB at 233-248. And as with the RBR1000, AMD asserts obviousness without supporting argument, which is insufficient to carry its burden. *See* RIB at

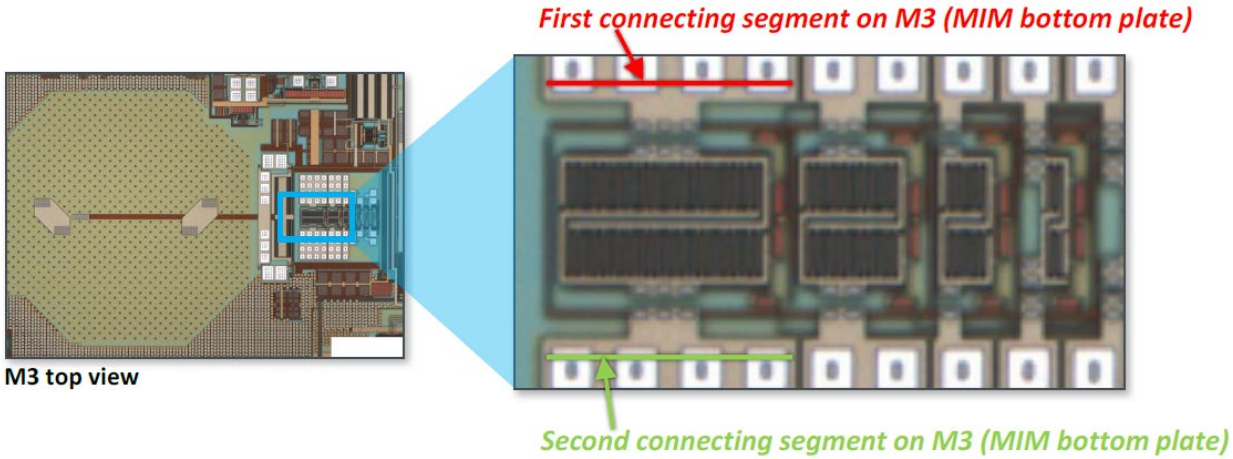
233. AMD has not shown claim 1 is anticipated by this reference nor, by extension, dependent claims 2-4.

AMD contends each limitation of claim 1 is present in the RFR6122. Realtek disputes whether several limitations are met, but both parties focus their discussions on the "connecting segments" of the "capacitor component." For background, there are several requirements for the "connecting segments" including that they "extend[] corresponding to the two extension-conductor segments in a same direction" and be "respectively overlapped with the two extension-conductor segments in a vertical direction." 582 patent at cl. 1.

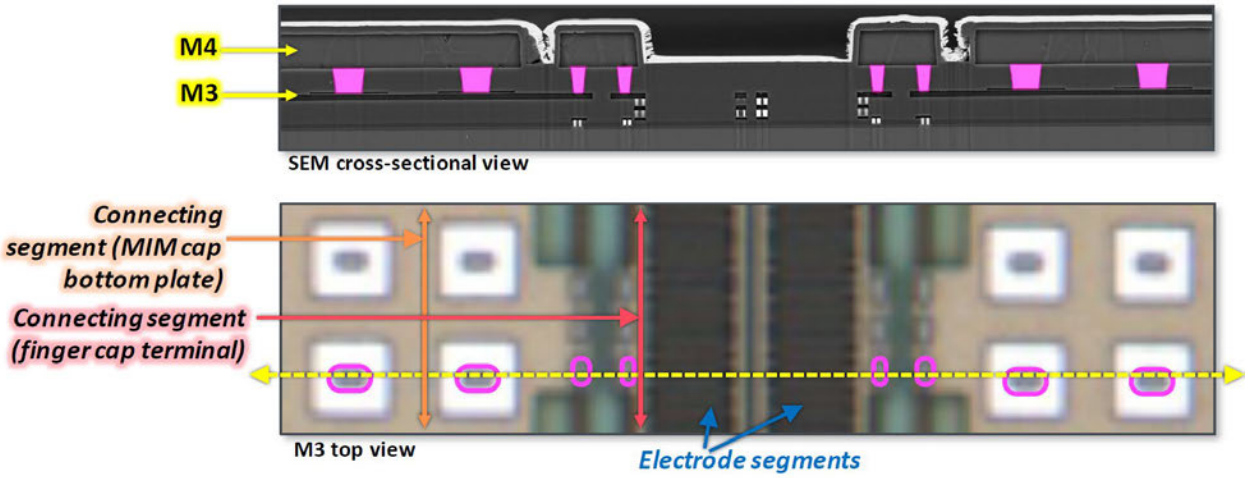
In support of its theory, AMD presents two reads on "connecting segments" within the RFR6122. First, AMD points to the leading edges of large, flat structures on the M3 layer which exist underneath the thick metal M4 layer that makes up the extension-conductor segments as in the images below:

[redacted]



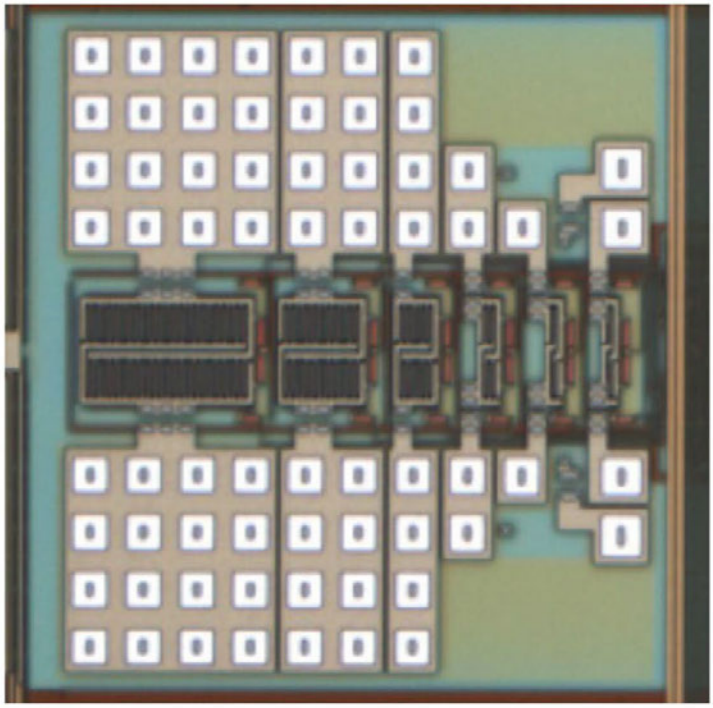


RIB at 233-234 (citing Hr'g Tr. (Prucnal) at 1054:18-61:16; RDX-0004.43; JX-0761.7-10). This segment is marked in orange below, along with a cross-sectional view taken along the dashed yellow line:



RDX-0004.45 (citing JX-0761.10, 14, 15).

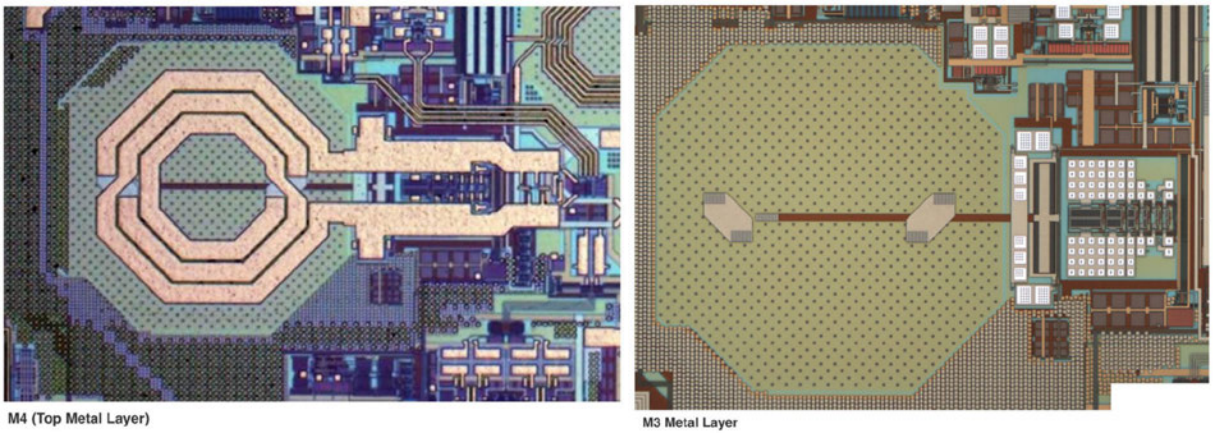
AMD's first read is unpersuasive. The identified bottom plates are large rectangular, tan shapes as shown below:



M3 Metal Layer

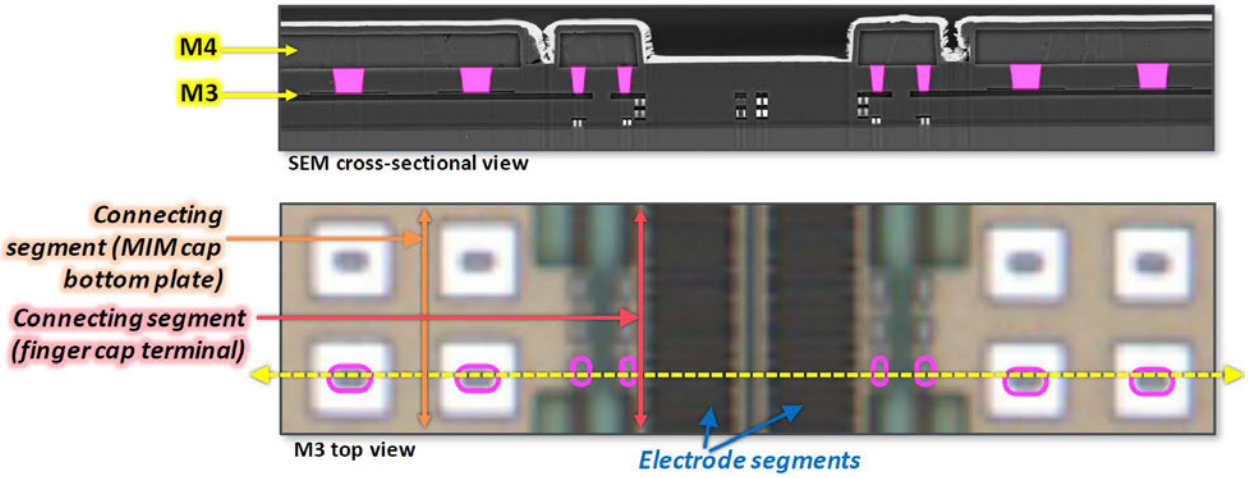
JX-0761.10. As shown, the leftmost plate is a square shape. The next is rectangular and extends in a vertical (as viewed) direction, as does the next plate, and the next after that. The fifth plate is again a square, as are the final set of two on the far right. None of these possible "connecting segments" are "extending corresponding to the two extension-conductor segments in a same direction" as required by the claim—most of the identified "connecting segments" clearly extend perpendicular (vertical as viewed) to the extension-conductor segments, and the left-most, square structure at best has no direction:

[redacted]



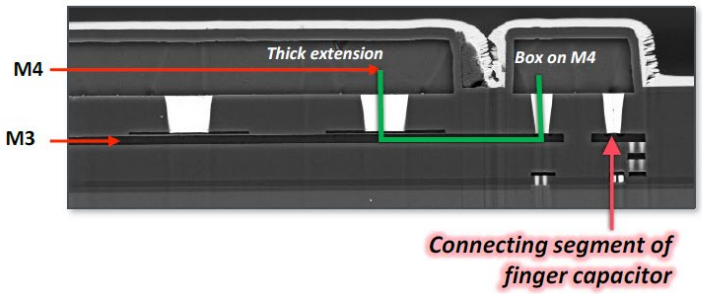
JX-0761.7, 9. Thus, the claim is not met by these structures.

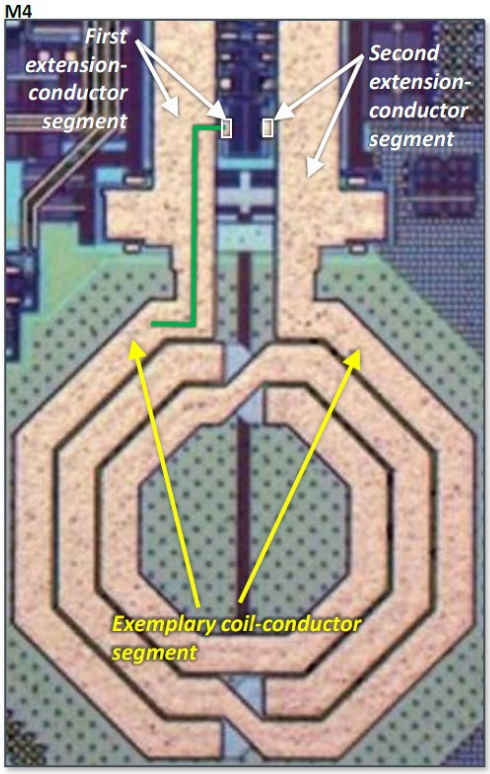
AMD's second read for "connecting segment" is what Dr. Prucnal refers to as the "finger cap terminal" indicated by the red line below:



RDX-0004.45; *see* RIB at 234-235 (citing Hr'g Tr. (Prucnal) at 1065:6-1067:13; RDX-0004.47). AMD explains that these segments, extending in the same direction as the "extension-conductor segments," are also "overlapped with the two extension-conductor segments" because they are covered by the squarish metal islands in white annotation boxes below:

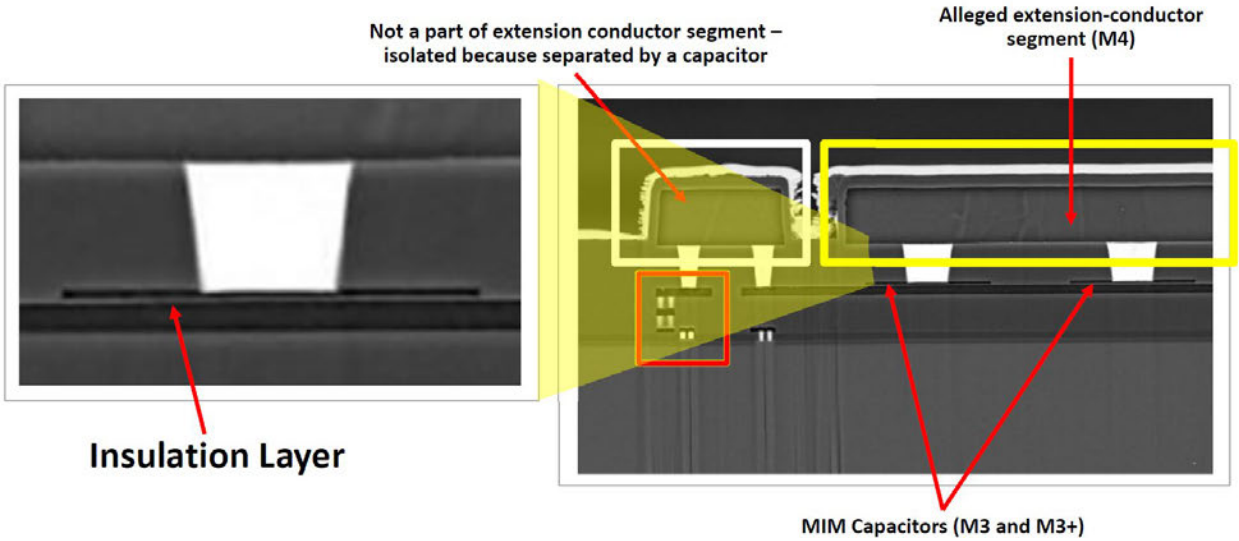
[redacted]





Id. at 235 (citing RDX-0004.47; JX-0761.7, 14). A top-down view, as well as the cross-section image, clearly show, however, that these are discrete structures from the "extension-conductor segments." They exist in the M4 layer, as do the "extension-conductor segments," and are in close physical proximity, but they are physically separated from them and so are not of the same "segment," and they are discrete structures that do not "extend[] outwards relative to the coil-conductor segment." 582 patent at cl. 1. As Realtek notes, they are not directly coupled, either because "[t]he two pieces (yellow and white boxes [below]) are electrically separated by the aforementioned MIM capacitors":

[redacted]



CIB at 349 (citing CDX-0022C.118; JX-0761.7, 14). Realtek persuasively reasons, "[m]etal separated by a capacitor cannot be a single extension-conductor segment." And in fact, they are separated by that capacitor as well as two different sets of vias. Neither AMD nor Dr. Prucnal offer an explanation as to why structures so separated would still be the same "segment." *See* RRB at 102 (citing Hr'g Tr. (Prucnal) at 1147:12-1148:21). The limitation is not met.

Accordingly, it has not been shown by clear and convincing evidence that the Qualcomm RFR6122 meets all limitations of claim 1, and none of claims 1-4 is invalidated by this reference.

3. Lack of Written Description

AMD argues that each of claims 1-4 are invalid under 35 U.S.C. § 112 for lack of written description. It alleges that "the patent only describes the first region (*e.g.*, 120 annotated in pink in Fig. 6 below) 'as a hollow region' that 'does not cover the extension-conductor segments' (annotated in green)." RIB at 261 (citing Hr'g Tr. (Prucnal) at 1093:22-0194:12). Assuming such is the case, AMD contends the "first region" used by Realtek to show infringement and technical prong domestic industry "go beyond what is described in the patent" since they include "non-hollow first regions that include the extension conductor segments" as below:

[redacted]

[redacted]

RIB at 262-263.

AMD is not persuasive. The specification demonstrates the inventors had possession of a "first region" that encompassed the area of the extension-conductor segments themselves, in addition to the space between. In fact, the specification describes three options—in-between both segments, overlapping one but not the other, or overlapping both:

> Here, the capacitor component 150 may be entirely and correspondingly arranged between the outer sides of the extension-conductor segments 133 and 135. Moreover, the capacitor component 150 may also be correspondingly located between the outer side of one of the extension-conductor segments 133 and 135 and an inner side of the other of the extension-conductor segments 133 and 135. In addition, the capacitor component 150 may be entirely and correspondingly arranged between the inner sides of the extension-conductor segments 133 and 135.

582 patent at 4:14-23; *see id.* at 7:29-28 (same). And although "region 120" is not mentioned in this excerpt, there is only ever one feature to which the capacitor component is said to be "correspondingly arranged," and first region 120 is discussed in the immediately preceding sentences, so the context is clear: "The first region 120 is located between the coil-conductor segment 131 and the two extension-conductor segments 133 and 135. Here, the coil-conductor segment 131 and the two extension-conductor segments 133 and 135 are formed by patter[n]ing a metal layer." *Id.* at 4:9-13. Overall, these disclosures reasonably convey to those skilled in the art that the inventor had possession of "first region" as of the filing date. *Ariad Pharm.*, 598 F.3d at 1351.

Accordingly, AMD has not shown any of claims 1-4 to be invalid for lack of written description.

VII. DOMESTIC INDUSTRY - ECONOMIC PRONG

In a patent-based complaint, a violation of Section 337 can be found "only if an industry in the United States, relating to the articles protected by the patent ... concerned, exists or is in the process of being established." 19 U.S.C. § 1337(a)(2). Under Commission precedent, this "domestic industry requirement" of Section 337 consists of an economic prong and a technical prong. *Stringed Instruments*, Inv. No. 337-TA-586, Comm'n Op. at 12-14. The complainant bears the burden of establishing that the domestic industry requirement is satisfied. *See Certain Set-Top Boxes and Components Thereof*, Inv. No. 337-TA-454, Initial Determination at 294 (June 21, 2002) (not reviewed in relevant part).

The economic prong of the domestic industry requirement is defined in subsection (a)(3) of Section 337 as follows:

> (3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark or mask work concerned --
>
> (A) Significant investment in plant and equipment;
>
> (B) Significant employment of labor or capital; or
>
> (C) Substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(3). The economic prong of the domestic industry requirement is satisfied by meeting the criteria of any one of the three factors listed above. Importantly, the Commission has clarified that investments in plant and equipment, labor, and capital that may fairly be considered investments in research and development are eligible for consideration under subsections (A) and (B), in addition to subsection (C). *See Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097, Comm'n Op. at 14 (June 29, 2018).

Realtek contends the economic prong is met under subsections (B) and (C) through the engineering investments of third-party Broadcom Corp. CIB at 359. The basis of Realtek's contention is the combined effect of: (1) a 2015 patent cross-license between Realtek and Avago Technologies General IP (Singapore) Pte. Ltd. ("Avago Licensee"); and (2) a subsequent merger event in which Avago Licensee and Broadcom Corp. became a corporate family, now including Broadcom Inc. (parent), Broadcom Corp. (subsidiary), and Avago Technologies International Sales Pte. Limited ("Avago Sales") among others. *See* JX-0784C ("Avago-Realtek License"); CX-1762 ("Merger Plan"). With these transactions and entities in mind, Realtek presents three alternative theories for why the DI Products are licensed under the Asserted Patents:

> (1) Broadcom, Inc. and Avago Sales are licensed under the License Agreement, and they themselves made and sold the DI products expressly acting in concert with additional Broadcom entities; (2) Broadcom, Inc. and Avago Sales exercised their [redacted] rights with regard to the DI products; and separate independent theory

that (3) Broadcom Corp. is itself a licensed "[redacted] under the License Agreement because it was not "[redacted]

CIB at 359-360. There are several interrelated disputes between the parties, including whether the investments are supported by reliable evidence, whether they are significant or substantial, which entities hold a license to the Asserted Patents, and whether the DI Products fall under the scope of that license (*i.e.*, "protected by the patent[s]"). The issues of license holders and authorized products is discussed first below, and then an analysis of the proffered investment amounts. For the reasons given, Realtek has not satisfied the economic prong.

A. Licensed Entities

As noted, Realtek's theories involve three non-parties that purportedly hold a license to the Asserted Patents: Broadcom Inc., Avago Sales, and Broadcom Corp. As for Avago Sales, Realtek explains in a footnote, "[redacted]" CIB at 361 n.21 (citing Hr'g Tr. (Phillips) at 263:9-24; JX-0784C at § 8.02(b)). AMD does not dispute this characterization nor Avago Sales' status as a licensee (*see generally* RIB at 267-278; RRB at 112-117), and it is consistent with descriptions given during summary determination motions practice (*see* EDIS Doc. ID 798390 at 2 n.2). Accordingly, Avago Sales is determined to hold a license to the Asserted Patents under the Avago-Realtek License (JX-0784C).

As for Broadcom Inc., Realtek explains that at the time of the license, Avago Technologies Ltd. ("Avago Parent") was the parent of Avago Licensee, and following the license, "Broadcom Inc. succeeded Avago Technologies Ltd. in interest," much like [redacted] CIB at 361-362 (citing Hr'g Tr. (Phillips) at 264:11-265:12). Realtek adds, "[i]t is [] beyond dispute that, for the reasons expressed above, Broadcom Inc. controls Avago Sales, and is therefore an [redacted] thereof. As such, both Avago Sales and Broadcom Inc. each

received a license under the [redacted] *Id.* at 363 (citing JX-0784C at § 3.01(b)). By way of background, Realtek refers to "[redacted] status for Broadcom Inc. in reference to the Avago-Realtek License which, under its grant clauses, granted a license to Realtek's patents to [redacted]." JX-0784C at § 3.01(b).

Broadcom Inc. does not meet the contract's definition of "[redacted] however. *See* RIB at 273 n.42; RRB at 114. The Avago-Realtek License defines "[redacted] as [redacted]

JX-784C at App'x A (annotated). This definition provides for exceptions, "including without limitation [redacted] (JX-0784C at App'x A), but as discussed below, [redacted] and there are no other pertinent exceptions in the document.

While it is true that, prior to the Merger Plan, Avago Parent owned and controlled Avago Licensee, Realtek affirmatively represents that Broadcom Inc. became owner of Avago Sales afterwards through a separate transaction, the details of which are not in the record:

> None of the entities identified in the scheme of acquisition was a party to the License Agreement. . . There is no evidence that they became affiliated with Avago

> until *after* the conclusion of the scheme of arrangement, when Pavonia later became Broadcom Inc. and *when*

CIB at 373 (long emphasis added). Avago Sales becoming "controlled by Broadcom Inc." after the Merger Plan necessarily means after the :

JX-0784C at App'x A (annotated). The conversion of Avago Parent to some intermediary (*e.g.*, Pavonia Ltd. (*see* RRB at 114)) before further conversion to Broadcom Inc. also would not fall under the agreement's — *i.e.*, Avago Licensee/Avago Sales or, as the case may be, Realtek Semiconductor Corporation. *See id.* at § 8.02(b). In fact, this all appears to be consistent with the license's explanation of what happens when

[redacted]

Id. at § 6.01(c).

In response, Realtek contends that "[u]nder California law, it is AMD's burden to establish that an exclusion applies." CIB at 373 (citing *Simpson Strong-Tie Co., Inc. v. Gore*, 49 Cal. 4th 12, 23 (Cal. 2010); *Sun Pacific Marketing Co-op., Inc. v. Dimare Fresh, Inc.*, 592 F. App'x. 564, 564-65 (9th Cir. 2015)). But even accepting this contention, the clear language of the license and Realtek's admission is sufficient to meet that burden, and the overall burden on Realtek to show a domestic industry is otherwise undisturbed and unmet. *Certain Artificial Eyelash Extension Systems, Products, and Components Thereof*, Inv. No. 337-TA-1226, Comm'n Op. at 48 (Oct. 24, 2022) ("*Eyelash Systems*") ("The complainant bears the burden of establishing that a domestic industry exists. . . . Further, a complainant must present credible and reliable evidence in order to meet its burden.") (citing, *inter alia*, *Lelo*, 786 F.3d at 883). Accordingly, Broadcom Inc. has not been shown to hold a license to the Asserted Patents under the Avago-Realtek License.

The last entity is Broadcom Corp. Realtek contends that Broadcom Corp. properly qualifies as an [redacted] to Avago Sales under the license because, contrary to AMD's position, it was not '[redacted]

> The third and final DI theory, which is not a prerequisite for the two earlier theories, is that Broadcom Corp. is an [redacted] under the License Agreement, and therefore holds a license to the Asserted Patents under the License Agreement. It is undisputed that Broadcom Corp. [became] [associated] with Avago after the Effective Date of that agreement, and the consideration received by Broadcom Corp. [redacted]. But the evidence shows that Broadcom Corp. was not [redacted] as that term is defined in that agreement.

[redacted]

CIB at 371. Realtek views the relevant evidence as the explicit terms of the Merger Plan on the one hand, and "the fuzzy recollection of Mr. Phillips" on the other. *Id.* For reference, Mr. Ryan Phillips testified at the hearing on behalf of Broadcom Corp. and took the position that Avago Parent acquired Broadcom Corp. "as far as the big picture" is concerned, but acknowledged he was unsure of the "lower-level mechanics" and would defer to the Merger Plan as compared to his memory. *See* CIB at 374 (citing Hr'g Tr. (Phillips) at 271:1-7, 288:7-9, 289:13-17); *but see* RIB at 277 (citing Hr'g Tr. (Phillips) at 271:1-15, 288:12-289:7). Realtek views the Merger Plan as "the only accurate evidence of the complex transaction." *Id.* at 371-372 (citing CX-1762C).

The Merger Plan does not support Realtek's claim, however. As cited above, Realtek admits that "the consideration by Broadcom Corp. [redacted]. And the Merger Plan, while not identifying the exact dollar figure, outlines that Avago Parent is the entity which provided the "cash" to buy out shareholders of Broadcom Corp.:

> Section 3.5 Exchange Procedures for Broadcom Common Shares.
>
> (a) At or immediately after the Cash/Stock Effective Time, Avago shall cause Holdco and New LP to respectively deposit with the Exchange Agent, acting as exchange agent and solely for the account and benefit of the former holders of Broadcom Common Shares at the Broadcom Effective Times, for exchange in accordance with this Article III, certificates or book entry shares representing the full number of Holdco Ordinary Shares and Units issuable pursuant to this Article III in exchange for outstanding Broadcom Common Shares. At or immediately after the Broadcom Effective Times, Avago shall provide or shall cause to be provided to the Exchange Agent all of the cash necessary to pay the aggregate amount of the Broadcom Merger Consideration payable pursuant to this Article III, including the aggregate amount of the Holdco Ordinary Shares and Units and the Aggregate Cash Consideration payable pursuant to this Article III (such Holdco Ordinary Shares, Units and Aggregate Cash Consideration, the "Consideration Fund"). In addition, Avago shall make available as necessary cash in an amount sufficient for payment in lieu of fractional shares pursuant to Section 3.3. In the event the Consideration Fund shall be insufficient to pay the aggregate amount of the

CX-1762C.42 (annotated). A 2015 SEC Form 10-K from Avago Parent similarly explains that, from its perspective, the merger "is anticipated to result in payment, in the aggregate, of approximately $17 billion in cash consideration." RX-1277.2.

And Realtek's focus on the minutiae of the Merger Agreement defies common sense. There were, to be sure, many shell corporations and special purpose vehicles established to execute the Merger Agreement, some of which bought and sold themselves to each other. *See* CIB at 371-

74. But the net result of the complicated, tax-driven series of transactions was that Avago Parent paid consideration for Broadcom Corp. *See id*. And surely to have the obligation, and to actually provide the cash "necessary to pay the aggregate amount of the Broadcom Merger Consideration" so as to effect the merger, is to ," as defined in the Avago-Realtek License. JX-0784C at App'x A (definition of covering " . Realtek completely fails to address this aspect of the Merger Plan, or the factual matter of where the billions of dollars paid to the shareholders of Broadcom Corp. went. *See generally* CIB at 371-374; CRB at 97-99. Consequently, Realtek's view of the complex transactions is unpersuasive. The license's definition of excludes (JX-0784C.14), so Broadcom Corp. cannot be deemed an under the agreement.

With that said, there is another path for Broadcom Corp. to hold a license to the Asserted Patents. of the Avago-Realtek License is entitled ," and while this article is referenced in the definition of (shown above), and the parties generally treat it as altering the scope of there is actually no pertinent mention of within the section. JX-0784C at § 6.01 (stating only, " " as a requirement to an exception). So does not actually affect the definition or scope of " JX-0784C at §§ 6.01(a)-(c).

Rather, it provides that :

JX-0784C at §§ 6.01(a)-(c). The problem, however, is that the consideration paid to Broadcom Corp. to complete the merger was [redacted]—around $36,000,000,000, as Realtek acknowledges. Hr'g Tr. (Phillips) at 273:6-11; RIB at 268; CIB at 371; RX-1277.2. Having found that the Merger Plan reflects an [redacted] of Broadcom

[redacted]

Corp., above, [redacted] and the license cannot "extend" to Broadcom Corp. This forecloses the second path.

Accordingly, Broadcom Corp. does not hold a license to the Asserted Patents.

B. Products Falling Under the License

The next question is whether the DI Products (BCM4387 and BCM4389) are properly considered "[redacted]" under the Avago-Realtek License. This is important because the contract [redacted] JX-0784C at App'x A. Realtek's briefing suggests that the DI Products are of Avago Sales and/or of Broadcom Inc. under the assumption that Broadcom Inc. is an [redacted] *See* CIB at 361-363; CRB at 90, 93-94. But Broadcom Inc. is not an [redacted] so only those portions of Realtek's argument and evidence tending to show that the products are of Avago Sales, along with AMD's rebuttal, are considered.

First, Realtek argues that Avago Sales' connection to the DI Products is rooted in their [redacted]

[redacted].

[redacted]

CIB at 362; *id.* at 368 ("[redacted] CRB at 90. Realtek acknowledges that it was [redacted] who developed the DI Products but asserts they did so "as [redacted] CIB at 367 (citing Hr'g Tr. (Phillips) at 284:11-20). Similarly, Realtek identifies [redacted] as arranging for the manufacture of the [redacted]. *Id.* at 367-368 (citing Hr'g Tr. (Phillips) at 258:16-259:22; Hr'g Tr. (Singh) at 307:20-308:2; CX-1878.10); *see id.* at 368 ("[redacted]").

Second, as a matter of contract interpretation, Realtek argues the test is one of a "meaningful and relevant connection":

> Under California law (the governing law of the License Agreement), contract interpretation requires a commonsense interpretation that avoids absurd results. *See, e.g.*, *Mount Vernon Fire Ins. Co. v. Busby*, 219 Cal. App.4th 876, 882 (2013). It would be nonsensical to characterize products sold by Avago Sales under the direction and control of Broadcom Inc. as other than "[redacted]." At the very least, under the circumstances, the DI Products have a meaningful and relevant connection to Broadcom Inc. (a licensed [redacted] under the License Agreement) and Avago Sales (a Party to the License Agreement).

CIB at 362; CRB at 90. As compared to this standard, Realtek reasons "it would be counterintuitive to conclude that a product sold by, [redacted] an entity and attributed to that entity as part of the consolidated financials, has no 'meaningful' or 'relevant connection' therewith." *Id.* at 90-91. Realtek further rejects the idea that a product can only be [redacted]; and observes that AMD offers no alternative interpretation of its own. CRB at 90.

[redacted]

AMD opposes and views the DI Products as entirely "of" Broadcom Corp. RIB at 276. AMD argues the development history establishes this as [redacted] *Id.* at 270-271 (citing Hr'g Tr. (Phillips) at 279:11-13, 279:14-280:14; RX-0730.4; RX-0734.1). Relying on the testimony of Mr. Phillips and other documents, AMD further notes that "at the time of Avago's subsequent acquisition of Broadcom, Avago did not make Wi-Fi and Bluetooth products like the DI Products" and all those engineers and employees "[redacted]" *See id.* at 271-272 (citing, *inter alia*, Hr'g Tr. (Phillips) at 280:15-282:12; RX-1329.9; RX-1364.1).

Turning to Avago Sales, AMD urges that merely [redacted] is not sufficient to make them "of" Avago Sales:

> Thus, in view of the product development history and Avago's lack of any role in bringing the DI Products to market, the DI Products are not [redacted] Nor are the DI Products [redacted] because, as established above, the "[redacted] definition [redacted] Indeed, the only role of Avago Sales is [redacted]. *Id.* at 281:15-18, 257:18-258:4. But as the ALJ stated, [redacted] Order No. 25 at 7. Accordingly, the [redacted] of the DI Products by Avago Sales are unauthorized.

Id. at 272; *see* RRB at 113. In at least one respect, AMD agrees with Realtek that the record shows [redacted] manufactures the DI Products but does not show which entity engages [redacted] to do so. RIB at 276 (citing Hr'g Tr. (Phillips) at 259:6-21, 283:6-284:10); RRB at 114. AMD then refers to the current position of the Broadcom entities, provided via Mr. Phillips, [redacted]. *Id.* at 113 (citing Hr'g Tr. (Phillips) at 278:22-279:2, 283:6-22; 282:7-12), 114.

Resolution of this issue would have been aided by evidence on the procurement and dissemination of the DI Products amongst the Broadcom entities and then out to the marketplace.

What appears undisputed is that, of the total amount of DI Products manufactured by , *See generally* Hr'g Tr. (Phillips) at 257:18-258:15, 280:25-281:24. Additionally, although Avago Sales had no role in their development, the actual DI Products in question, BCM4387 and BCM4389, — several years after the acquisition of Broadcom Corp. by Avago entities. *See generally id.* at 279:3-281:14. AMD raises the point that if selling a product automatically means that product is "of" the seller, then would seem to be readily circumvented. *See* RIB at 278; RRB at 115. But it is equally notable how the agreement fails to provide any restrictions whatsoever on the meaning to avoid the obvious workaround. *See, e.g.*, JX-0784C at App'x A (providing several restrictions for , § 6.01(c) (introducing concepts of .

On balance, the passage of time between the merger and the development of the DI Products, during which time Broadcom Corp. was controlled by Broadcom Inc., Avago Parent's successor in interest, coupled with the fact that Avago Sales has its own suggests that the products so sold are "of" Avago Sales, even if the product line was not originally. So the portion of the DI Products sold by Avago Sales are properly "

[redacted]

C. Significant or Substantial Investment

The Federal Circuit has held that the investment supporting a section 337 domestic industry must be expressed quantitatively. *Lelo*, 786 at 886. For this, Realtek looks to monetary expenditures made by "Broadcom," generally, but testimony from Mr. Phillips indicates all [redacted]. *See* CIB at 375-387; Hr'g Tr. (Phillips) at 280:25-281:14 [redacted]

1. Subsection (B)

Starting with subsection (B), "significant employment of labor or capital," Realtek, aided by the analysis of its expert, Dr. Sean Sheridan, calculates a [redacted] labor investment from two groups of employees (Engineering and Operations) as follows:

> Broadcom has produced information showing domestic labor and capital investments in dollars and headcount for the two DI Products on a fiscal year basis between 2020 and the present. CX-1801C; Tr. (Singh) at 296:3-11; Tr. (Sheridan) at 666:21-668:9. There are no foreign employees included in these FTE numbers. Tr. (Singh) at 301:16-18. The employees corresponding to the captured FTEs are mostly based in Broadcom's San Jose and Irvine facilities. *Id.* at 301:19-23.
>
> The U.S. headcount numbers were primarily provided by the General Manager of Broadcom's Mobility Division, Mark Gonikberg. *Id.* at 298:1-3; Tr. (Sheridan) at 667:20-24. Mr. Gonikberg was able to consult weekly time data recording the projects (chips) on which each employee corresponding to the captured FTEs was working. Tr. (Singh) at 298:6-299:6; Tr. (Sheridan) at 667:20-668:3. The employees corresponding to the FTEs calculated by Mr. Gonikberg were engineers engaged in post-release support, such as software development and additional debugging activities. Tr. (Singh) at 299:7-23; Tr. (Sheridan) at 671:1-9. Such software developments allowing a patented device to "continue to operate correctly," are cognizable investments for domestic industry purposes. *Certain Handheld Electronic Computing Devices, Related Software, and Components Thereof*, Inv. No. 337-TA-769, Order No. 34, 2012 ITC LEXIS 380, at *20-21 (Feb. 6, 2012).
>
> Also included in the captured FTEs were operational employees (comprising less than [redacted] of the FTE totals) supporting the DI Products identified by the Operational Lead, Donald Reisinger. Tr. (Singh) at 300:7-20; Tr. (Sheridan) at 671:10-18. Mr. Reisinger was able to identify these FTEs as they correspond to

[redacted]

people that he supervises. Tr. (Singh) at 300:25-301:7. These FTEs correspond to employees that provide test time improvements, yield improvements, and test program writing for the DI Products. Tr. (Singh) at 301:8-15; Tr. (Sheridan) at 671:19-24.

. . . .

As for the FTE numbers themselves, while Mr. Bakewell used terms such as "limited" to describe post "tape out" investments, he did not, and could not, say that the [redacted] Tr. (Bakewell) at 728:25-729:10. The actual data regarding FTEs that Broadcom produced show that headcount investments in the DI Products have continued:

Year	FY2020	FY2021	FY2021	FY2023[3]
FTEs	[redacted]			

CX-1801C.

Broadcom also calculated dollar amount of its investments in labor using the following formula: [redacted] Tr. (Singh) at 301:24-302:14; Tr. (Sheridan) at 671:25-672:11; *see also* CX-1798C at 21:9-12. [redacted] CX-1798C at 19:17-24; CX1800 at 81:21-82:3. Broadcom's calculation yielded the following labor investment numbers, totaling approximately [redacted] for the time periods in question:

Year	FY2020	FY2021	FY2021	FY2023[28]
Labor Expense	[redacted]			

CX-1801C.

CIB at 376-377, 379-380. Realtek also calculates a [redacted] capital investment behind the DI Products, as follows:

Also under sub-prong (B) are Broadcom's project engineering expenses, which are [redacted] the DI Products, i.e., expenses incurred in the United States. Tr. (Singh) at 302:15-19 & 303:2-11; Tr. (Sheridan) at 672:15-673:3. Broadcom (as opposed to Dr. Sheridan, or anyone else associated with Realtek) selected these expenses for inclusion in the domestic industry calculus. Tr. (Sheridan) at 673:4-9. [redacted] CX-1798C at 31:12-15.

[redacted]

. . . .

> The following are the project engineering expenses ("PEP") attributed to the DI Products by Broadcom, totaling approximately [redacted] for the time period in question:

Year	FY2020	FY2021	FY2021	FY2023[31]
PEP	[redacted]			

> CX-1801C.

CIB at 380-381. According to Realtek, the total attributable to subsection (B) is [redacted]. *Id.* at 381.

As alluded above, there are several allocation problems that render Realtek's calculations unreliable for economic prong purposes. The first involves the "Labor expense" data. As described above, this was collected by Mr. Singh via other Broadcom managers and produced to this investigation in the form of a single, cursory, table:

RealTek ITC subpoena - Estimated US Spending				
BCM4387 and BCM4389 estimate	Fiscal 2020 (Nov'19 - Oct'20)	Fiscal 2021 (Nov'20 - Oct'21)	Fiscal 2022 (Nov'21 - Oct'22)	Fiscal 2023 May YTD (Nov'22-May'23))
US Only Headcount	[redacted]			
Labor expense				
Project Engineering expense				
Capital Investment (Mobile Connectivity)				

CX-1801C. AMD argues that the data is unreliable for many reasons, including: "Broadcom provided not a single supporting document that could be used to verify any of the investment data"; "Dr. Sheridan was uninterested in obtaining any further documents, nor did he ask to speak with anyone at Broadcom"; a change from an earlier, global, version of the spreadsheet implies an incredulous, nearly perfect [redacted] between foreign and U.S. labor costs; and that a Broadcom [redacted] was occurring on the DI

Products at all. *See* RIB at 284, 286-288 (citations omitted); RRB at 121, 122-124 (citations omitted). These observations are relevant and provide good context in which to evaluate Mr. Singh's table, but AMD provides no evidence of its own to show the alleged failures are material to the inquiry (*e.g.*, no foreign salary data, no project documents showing nature of activity, no testimony from further Broadcom personnel). And a single financial table on its own is not necessarily problematic. *See, e.g.*, *Certain Wet Dry Surface Cleaning Devices*, Inv. No. 337-TA-1304, Comm'n Op. at 83-84 (Jan. 8. 2024).

AMD further questions, however, how it is possible that "Broadcom allegedly spent over from November 2020 through May 2023 on the two DI Products, after the products had already been designed, manufactured, and sold." RIB at 284 (citing [CX-1801C]). This would seem to be a lot for "post-release support, such as software development and additional debugging activities" for just these two products, and in fact the figure is closer to is only the U.S. activity. *See* CX-1605C (same data as CX-1801C but worldwide); CIB at 380 (representing CX-1605C as accurate). is an even harder number to accept, but AMD provides no evidence to disprove the reliability of the per-project/per-product time records ordinarily kept by Broadcom and accessed by Mr. Gonikberg to generate the amounts. CIB at 376 (citing Hr'g Tr. (Singh) at 298:6-299:6; Hr'g Tr. (Sheridan) at 667:20-668:14).

Nevertheless, otherwise accurate time records could still be overinflated for present purposes if the post-release support, software development, and debugging supported products beyond those shown to practice the Asserted Patents (*i.e.*, the DI Products). This is a necessary allocation for section 337 purposes but is not commonly captured in ordinary business records. 19 U.S.C. § 1337(a)(3) ("an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent . . ."); *Certain Electronic Stud*

Finders, Metal Detectors and Electrical Scanners, Inv. No. 337-TA-1221, Comm'n Op. at 50-51 (Mar. 14, 2022) ("The Commission notes that this is not the first time that it has explained that aggregating investments in articles that *are* protected by a particular patent with investments in articles that *are not* protected by that patent may preclude meaningful consideration of those investments under the statutory framework required by section 337."); *Eyelash Systems*, Inv. No. 337-TA-1226, Comm'n Op. at 50, 53 (finding inclusion of non-cognizable expenses fatal to subsections (A) and (B)).

AMD questions whether non-practicing products were removed from Broadcom's calculus, and rightly so. RIB at 288. The collection of the labor data in CX-1801C started with Mr. Singh who, lacking personal knowledge, directed Mr. Gonikberg to access time records with which he was familiar:

> Q. Let's start with the engineering employees. Who made the calculation of the FTEs corresponding to them?
>
> A. The divisional general manager, Mark Gonikberg.
>
> Q. And did he do that at your direction?
>
> A. Yes. I required this information from him.

Hr'g Tr. (Singh) at 298:1-5; *see id.* at 299:14-16 ("Q. And how do those kind of projects related to the continued viability of these products, if you know? A. I don't know."), 299:24-300:6 ("Q. And where did you gain the information about what these engineers were doing? A. From the general manager. Q. From Mr. Gonikberg? A. Yes. Q. So he is the one that told you generally what they were engaged in? A. Yeah."), 308:18-309:10. As evidenced by Broadcom Corp.'s update to the summary table during discovery, Mr. Singh knew to look out for and exclude foreign personnel:

> Q. Mr. Singh, what is CX-1605C?

A. So this was the prior estimate of the U.S.-based expense and headcount to support these two projects from November 2019 through October 2022. But subsequent to that, when you asked to update this expense list through May 2023, we found out this expense and headcount was overstated in the sense that we also included the foreign-based headcount. So we corrected that in the prior -- prior spreadsheet.

Q. So just to be clear, then, the U.S.-only headcount was actually worldwide?

A. In this case, yes. Inadvertently, I guess, captured as worldwide, yes.

. . . .

Q. And so who actually noticed that there was an error in this original spreadsheet?

A. Mark Gonikberg did when we went back to him to expand this analysis to – to May '23. That's when he realized he had inadvertently also included foreign headcount in those numbers that he gave us.

Q. And what did Broadcom do when Mr. Gonikberg noticed the mistake?

A. We corrected it, and we provided the estimate that you previously showed us and showed – put up here.

Q. Without anyone asking you to do that?

A. Yes. Since we were holding up a new estimate, so as part of the new estimate, we did – we did provide the corrected estimate on that.

Id. at 304:6-305:11.

Critically though, Mr. Singh did not seem to know that he needed to also exclude FTE time in support of non-DI Products:

Q. And for the people that these FTEs represent, you don't know if they work on products other than the domestic industry products, right?

A. Ask the question again, please?

Q. The people that are represented by these FTEs in the spreadsheet, you don't know if those people also work on other products, other than the two – two DI chips?

A. I do not know that.

Q. And you don't know if they spent all their time working on the DI chips versus other products?

A. Correct, I do not [know] the breakdown of time.

Hr'g Tr. (Singh) at 313:7-17; *see id.* at 312:11-17 ("Q.

A. I do not know that."). This testimony is particularly probative of the issue because Mr. Singh is the one who directed Mr. Gonikberg on what sort of data to collect. If Mr. Singh had instructed Mr. Gonikberg to exclude FTE activity supporting non-DI Products, as he did for foreign labor and must for section 337 purposes, then the answer to these questions would not have been "I don't know." Without any testimony from Mr. Gonikberg, or evidence or information on the timecard system used by his employees, and in light of the massive investment amount alleged (approximately), coupled with the fact that software routinely affects multiple products within a family and Broadcom likely has other products and continues to develop wireless communication chipsets, there is little reason to find the amount claimed is limited to "the articles protected by the patent." *See* Hr'g Tr. (Sheridan) at 666:8-669:14 (relying only on CX-1801C and Mr. Singh's representations); JX-0919.5-6 (10-K mentioning families of Wi-Fi and Bluetooth products). Realtek offers no rehabilitation of this admission by Mr. Singh and instead argues it is "irrelevant" (CRB at 102), which is contrary to the Commission precedent cited above.

Accordingly, the post-release support, software development, and debugging labor figures are not sufficiently tied to the DI Products and are not accepted for economic prong purposes. Those additional employees working in operations, as reported to Mr. Singh by Mr. Reisinger, are questionable for the same reason, if not more so because they are rough estimates and not generated from a timecard system. Hr'g Tr. (Singh) at 300:17-301:15 ("I spoke with him, and his was much

more of a high-level, directional estimate . . . . the reason it's a high-level directional estimate is because he [doesn't] have the system that Mr. Gonikberg has.").

A second missing allocation compounds the problem—that is, the portion of DI Products that belong to Avago Sales as opposed to Broadcom Corp. As determined above, the former is licensed while the latter is not; and this is important because only licensed products (those "protected by the patent"), and investments in support thereof, can form a basis for section 337 domestic industry. 19 U.S.C. § 1337(a)(3); *Electronic Stud Finders*, Inv. No. 337-TA-1221, Comm'n Op. at 50-51; *Eyelash Systems*, Inv. No. 337-TA-1226, Comm'n Op. at 50.

Realtek provides no data, and there appears to be none in the record, indicating the relative amount of licensed-to-unlicensed DI Products manufactured and sold. In the absence of exact sales figures (which are ordinary business records and frequently produced in section 337 investigations), it could suffice to show through other records that the amount attributable to Broadcom Corp. is trivial. But even this high-level estimate is missing from the record. So in addition to the failure to allocate out non-BCM4387 and BCM4389 products from the labor expenses, there is a failure to allocate out unlicensed DI Products. This places Realtek's economic prong theory even further from the Commission's standards. *See, e.g.*, *Eyelash Systems*, Inv. No. 337-TA-1226, Comm'n Op. at 55 (finding 100% allocation of facility costs is over-inclusive based on the evidence); RRB at 128 (citing *Certain Polymide Films, Products Containing Same, and Related Methods*, Inv. No. 337-TA-772, Initial Determination at 277-280 (May 10, 2012) (not reviewed in relevant part)).

Moving away from labor, Realtek's capital investments, shown in the table as "Project Engineering expense," suffer similarly. Realtek contends that "Broadcom (as opposed to Dr. Sheridan, or anyone else associated with Realtek) selected these expenses for inclusion in the

[redacted]

domestic industry calculus" and that it is comprised of consumable expenses allocated by the same FTE headcount used for labor and then mask expenses "[redacted] CIB at 380-381 (citing Hr'g Tr. (Singh) at 302:15-19, 303:2-11; Hr'g Tr. (Sheridan) at 672:15-673:9; CX-1798C (Singh) at 31:12-15); see CX-1798C at 48:6-18. Mr. Singh testified that [redacted] Hr'g Tr. (Singh) at 303:2-11. AMD raises a number of reasonable questions here such as whether the consumables and mask costs were truly spent in the United States given the DI Products' [redacted] and how the revenue allocation was effected to limit mask costs to the DI Products. *See* RIB at 290-292 (citing, *inter alia*, *Certain Integrated Circuits, Chipsets, & Products Containing Same Including Televisions*, Inv. No. 337-TA-786, Initial Determination, 2012 WL 3610787 at *86 (July 12, 2012) (*aff'd* in relevant part, Comm'n Op., Oct. 10, 2012)). And Realtek fails to answer either question convincingly. *See* CRB at 104 (arguing "the only logical conclusion" is that Broadcom is the one who uses the masks despite [redacted] of the DI Products). But the two allocation problems identified above for labor apply equally to capital expenses (*see* CIB at 381 ("Broadcom's engineering expenses are apportioned based upon the FTE headcount")) and are enough to find them not sufficiently reliable.

Accordingly, Realtek has not met its burden to show economic prong under Subsection (B).

2. Subsection (C)

Realtek contends economic prong is also met under subsection (C) due to the same post-release support, software development, debugging, and operations activities identified for subsection (B), totaling approximately [redacted]. CIB at 384, 385. Different from subsection (B), Realtek explains, is that under subsection (C) a nexus needs to be shown between investment and the Asserted Patents, as opposed to between investment and the DI Products. *Id.* at 384-385,

386. Critically, Realtek argues this nexus is presumed when the domestic industry products are shown to practice the patents:

> Additionally, Realtek has shown that there is a domestic industry under sub-prong (C) related to the research, development, and engineering of the DI Products. Unique to sub-prong (C) investments is the required nexus between such investments and the asserted patents, which is presumed where the products in question practice such patents. *See, e.g.*, *Certain Gas Spring Nailer Products and Components Thereof*, Inv. No. 337-TA-1082, Comm'n Op., 2020 WL 2093834, at 40 (Apr. 28, 2020), reversed and remanded on other grounds sub nom. *Kyocera Senco Industrial Tools Inc. v. Int'l Trade Comm'n*, 22 F.4th 1369 (2022) (citing *Certain Digital Video Receivers and Hardware and Software Components Thereof*, Inv. No. 337-TA-1001, Initial Det., 2017 WL 3485153, at *389-90 (May 26, 2017) (relevant portions unrev'd) (nexus exists where domestic industry products "practice certain of the asserted patents"); *Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm'n Op., 2014 WL 12796437, at *22-24 (Aug. 22, 2014) ("nexus may readily be inferred based on evidence that the claimed investment is in the domestic industry article, which itself is the physical embodiment of the asserted patent"); and *Certain Nonvolatile Memory Devices and Products Containing Same*, Inv. No. 337-TA-1046, Comm'n Op., 2018 WL 6012622, at *18 (Oct. 26, 2018) (complainant urging presumed nexus retained Mr. Bakewell)).

Id. at 384. Realtek reasons that because AMD's expert, Mr. Bakewell, failed to put forth any evidence—and in fact had no opinion one way or the other—that the research efforts did not have a nexus to the Asserted Patents, the presumption is maintained and determinative of the issue. *Id.* at 386-387; CRB at 105 ("AMD offered nothing approaching *evidence* of a disconnect between Broadcom's investments and the asserted patents."), 106 ("In short, Realtek has presented 'evidence of investment in the patented article . . . to support an inference that the investment also exploits the patent.'").

AMD disputes that the requisite nexus has been shown, primarily on the grounds that there is no presumption:

> Realtek's reliance on a presumption of a nexus rather than attempting to connect the investments to the patents is legally flawed.
>
> . . . .

> That is wrong. As Realtek should know, having made and lost this argument before, "an investment in the article is not automatically an investment in the asserted patent." *Integrated Circuit Chips*, Inv. No. 337-TA-859, 2014 WL 12796437 at *23 (finding that Realtek failed to show a nexus). Instead, a nexus can only be inferred when the domestic industry product "is the physical embodiment of the asserted patent." Id. at *28. Absent that showing, as here, the complainant must demonstrate a specific connection between the investments and the asserted patents. *Id.* at *29; *Certain Electronic Candle Products and Components Thereof*, Inv. No. 337-TA-1195, Comm'n Op. at 21, 29 (Oct. 4, 2022) ("[C]omplainant must show the connection between its investments and the patented invention that it is exploiting. . . . Complainants have failed to meet their burden of proof to show that these investments meet the nexus requirement that sufficiently ties the investments to the exploitation of the asserted patent claims."). As Mr. Bakewell explained, no such showing was made. Tr. (Bakewell) at 706:21-708:3, 730:6-25. Accordingly, Realtek failed to satisfy sub-prong (C).

RIB at 292-293. AMD clarifies, "[t]here is only a presumption of nexus upon complainant showing that the DI products are the commercial embodiments of the patents." RRB at 125-126. And when viewed in that light, it argues there is no nexus "because the DI Products are Wi-Fi/Bluetooth combination chipsets, whereas the patents are directed to low-level features in the product circuity." *Id.* at 126 (citing Hr'g Tr. (Bakewell) at 707:19-708:3).

AMD has the correct position on the law. Realtek primarily relies on *Gas Spring Nailers* in which the Commission did state that "[t]he requisite nexus between Kyocera's exploitation activities and the '718 patent is met here because the activities here go toward developing DI products that embody and practice the asserted claims." Inv. No. 337-TA-1082, Comm'n Op. at 80 (citing, *inter alia*, *Integrated Circuit Chips*, Inv. No. 337-TA-859, Comm'n Op. at 38-40). Yet the Commission has more recently clarified that this presumption of nexus between investment and patent only comes about "if the domestic industry article is 'the physical embodiment of the asserted patent,' that is, if the domestic article is coextensive with the patented invention." *Electronic Candle Products*, Inv. No. 337-TA-1195, Comm'n Op. at 15-16 (citing, again, *Integrated Circuit Chips*, Inv. No. 337-TA-859, Comm'n Op. at 38-41). The Commission

continued, "[t]hat said, 'there may be circumstances in which the domestic investment is so unrelated to the asserted patent that no nexus can be imputed" (*id.* (citing, again, *Integrated Circuit Chips*, Inv. No. 337-TA-859, Comm'n Op. at 42-43)) and proceeded to compare the specific structural aspects of the electronic candle claimed by each asserted patent to the complainant's description of its research and development activities (*id.* at 16, 16 n.19).

Realtek does not attempt to address this precedent, despite it appearing in AMD's initial briefing. *See* CRB at 15-106. Thus, the presumption does not exist, and Realtek has not met its burden. And when the correct standard is applied, it is still not met. AMD persuasively points out—without any opposing argument from Realtek—that two asserted patents are directed to specific inductor shapes and layouts, with one including a capacitor bank (245 and 582 patents), and one is directed to low-level metal wiring (218 patent), whereas the protected articles in commerce are the entire Wi-Fi/Bluetooth combination chipsets which contain these distinct elements. *See generally* RRB at 126; 245 patent at cl.1; 218 patent at cl. 12; 582 patent at cl. 1. None of the Asserted Claims of any Asserted Patent reach the scope of, and thus become "coextensive" with, entire chipset articles. This makes the present circumstances most similar to *Electronic Candle Products* and *Integrated Circuit Chips*, where no nexus was found. Inv. No. 337-TA-1195, Comm'n Op. at 16-17 n.19; Inv. No. 337-TA-859, Comm'n Op. at 44-50. And for the avoidance of any doubt, there is essentially no information in the record about the nature of the identified Broadcom Corp. R&D activities beyond the descriptor, "post-release support, software development, and debugging." Hr'g Tr. (Singh) at 311:4-313:20. Based on their plain meanings, these could reasonably apply to any portion of the chipsets, not just those structures embodying the Asserted Claims. The "software development" and "debugging" activities, in fact, probably cannot directly apply to the structures embodying the Asserted Claims because such structures

lack processors, memory, application interfaces, or any other feature that would employ software or require debugging.

Accordingly, Realtek has not met its burden to show economic prong under Subsection (C).

VIII. CONCLUSIONS OF LAW

1. Realtek has proven infringement of claims 1, 2, and 8 of U.S. Patent No. 7,936,245.

2. Realtek has proven infringement of claims 12, 13, and 15-18 of U.S. Patent No. 8,006,218.

3. Realtek has not proven infringement of any claim of U.S. Patent No. 9,590,582.

4. AMD has proven the invalidity of claims 1, 2, and 8 of U.S. Patent No. 7,936,245.

5. AMD has proven the invalidity of claims 12, 13, and 15-18 of U.S. Patent No. 8,006,218.

6. AMD has proven the invalidity of claims 1-3 of U.S. Patent No. 9,590,582, but not claim 4.

7. Realtek has proven the existence of articles protected by claims 1, 2, and 8 of U.S. Patent No. 7,936,245, except that the claims are invalid.

8. Realtek has proven the existence of articles protected by claims 12, 13, and 15-18 of U.S. Patent No. 8,006,218, except that the claims are invalid.

9. Realtek has proven the existence of articles protected by claims 1-3 of U.S. Patent No. 9,590,582, except that the claims are invalid.

10. Realtek has not proven the existence of an economic domestic industry as required by 19 U.S.C. § 1337(a)(2) for U.S. Patent No. 7,936,245, U.S. Patent No. 8,006,218, and U.S. Patent No. 9,590,582.

11. There is no violation of section 337 with respect to U.S. Patent No. 7,936,245.

12. There is no violation of section 337 with respect to U.S. Patent No. 8,006,218.

13. There is no violation of section 337 with respect to U.S. Patent No. 9,590,582.

IX. RECOMMENDED DETERMINATION ON REMEDY AND BOND

The Commission's Rules provide that subsequent to an initial determination on the question of violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, the administrative law judge shall issue a recommended determination concerning the appropriate remedy in the event that the Commission finds a violation of section 337, and the amount of bond to be posted by respondent during Presidential review of the Commission action under section 337(j). *See* 19 C.F.R. § 210.42(a)(1)(ii).

The Commission has broad discretion in selecting the form, scope, and extent of the remedy in a section 337 proceeding. *Viscofan, S.A. v. Int'l Trade Comm'n*, 787 F.2d 544, 548 (Fed. Cir. 1986). Under Section 337(d)(1), if the Commission determines as a result of an investigation that there is a violation of section 337, the Commission is authorized to enter either a limited or a general exclusion order. 19 U.S.C. § 1337(d)(1). A limited exclusion order instructs the U.S. Customs and Border Protection ("CBP") to exclude from entry all articles that are covered by the patent at issue and that originate from a named respondent in the investigation. A general exclusion order instructs the CBP to exclude from entry all articles that are covered by the patent at issue, without regard to source. *Certain Purple Protective Gloves*, Inv. No. 337-TA-500, Comm'n Op. at 5 (Dec. 22, 2004). Under section 337(f)(1), the Commission may issue a cease and desist order in addition to, or instead of, an exclusion order. 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold, thereby undercutting the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof*

and Prods. Containing Same, Including Air Conditioners for Automobiles, Inv. No. 337-TA-334 (Remand), Comm'n Op. at 26-28 (Sept. 10, 1997).

Additionally, during the 60-day period of Presidential review under 19 U.S.C. § 1337(j), "articles directed to be excluded from entry under subsection (d) . . . shall . . . be entitled to entry under bond prescribed by the Secretary in an amount determined by the Commission to be sufficient to protect the complainant from any injury." *See* 19 U.S.C. § 1337(j)(3). "The Commission typically sets the bond based on the price differential between the imported infringing product and the domestic industry article or based on a reasonable royalty. However, where the available pricing or royalty information is inadequate, the bond may be set at one hundred (100) percent of the entered value of the infringing product." *Certain Industrial Automation Systems and Components Thereof Including Control Systems, Controllers, Visualization Hardware, Motion and Motor Control Systems, Networking Equipment, Safety Devices, and Power Supplies*, Inv. No. 337-TA-1074, Comm'n Op. at 13 (Apr. 23, 2019) ("*Automation Systems*") (public version) (citation omitted).

A. Limited Exclusion Order

Should a violation be found, there is no dispute that a limited exclusion order ("LEO") should issue against AMD. *See* CIB at 396; RIB at 294-297. AMD further requests exemptions for "debugging, warranty, service, and repair activities" because "[a]bsent such an exemption, AMD's customers would be unduly harmed and unable to service or replace products already purchased. AMD maintains only limited inventory." *Id.* at 294-295 (citing JX-0932C; Hr'g Tr. (Bakewell) at 711:6-12). AMD further requests a certification provision at least for the purpose of certifying that the Non-Accused Products (discussed above) and "field-programmable gate array ('FPGA') products" may be imported regardless of whether a violation is found. *Id.* at 295-296

(citing JX-1010C). Lastly, AMD contends, "[a]ny remedy should also not extend to future products not yet imported and not specifically adjudicated in the Investigation. . . [or] not taped out and imported by the evidentiary hearing." *Id.* at 296.

AMD's request for a certification provision is granted, as these are standard and used to "aid U.S. Customs and Border Protection ('CBP') in enforcing Commission orders but 'do not mandate that CBP accept certification as proof that the articles in question are not covered' by the limited exclusion order." *Certain Robotic Vacuum Cleaning Devices and Components Thereof Such as Spare Parts*, Inv. No. 337-TA-1057, Comm'n Op. at 55 (Feb. 1, 2019); *see, e.g.*, *Certain Wearable Electronic Devices with ECG Functionality and Components Thereof*, Inv. No. 337-TA-1266, Limited Exclusion Order at 3 (Dec. 22, 2022). As "it has been Commission practice for the past several years to include certification provisions in its exclusion orders to aid CBP" (*see Certain Road Milling Machines and Components Thereof*, Inv. No. 337-TA-1067, Comm'n Op. at 15, 15 n. 5 (Aug. 7, 2019) (citations omitted)), it is my recommendation that any issuing limited exclusion order should include the Commission's standard certification provision. As it concerns the Non-Accused Products and FPGA products, these would appear to be rightful circumstances to employ the provision.

AMD's request that any remedy not extend to products not adjudicated or taped out, or still in development, as a general matter, is not recommended. If a patent is found to be infringed, a limited exclusion order will issue against any and all products that both infringe and fall under the scope of the investigation, as is standard. *See, e.g.*, *Wearable Electronic Devices*, Inv. No. 337-TA-1266, Limited Exclusion Order at 2 (Dec. 22, 2022). The exclusion order will not be directed only to the products which were at issue in the present investigation. As for a "debugging, warranty, service, and repair" exemption, the request turns on public interest concerns which were

not instituted for this stage of the investigation. *See* 88 Fed. Reg. 4206 (Jan. 24, 2023); RIB at 295 ("so as not to adversely impact existing customers"). Nevertheless, it would appear AMD's basis for this exemption to the limited exclusion order—that it "maintains only limited inventory"—is dubious as it cites no evidence (*id.* at 295) and had stipulated early in the investigation that it maintains commercially significant inventory within the United States (CX-1809C).

B. Cease and Desist Order

Should a violation be found, Realtek argues a cease and desist order ("CDO") should issue against AMD. CIB at 397. Realtek contends, "[t]he parties have stipulated that AMD maintains commercially significant quantities of Accused Products." *Id.* (citing CX-1670C at 2). AMD offers no opposition. *See* RIB at 294-296; RRB at 128.

Complainants bear the burden on the issue of cease and desist orders. *Certain Microfluidic Devices*, Inv. No. 337-TA-1068, Comm'n Op. at 23 (Jan. 10, 2020). Such orders "are generally issued when, with respect to the imported infringing products, respondents maintain commercially significant inventories in the United States or have significant domestic operations that could undercut the remedy provided by an exclusion order." *Id.* at 22-23 (citations omitted). Realtek has shown, through stipulation, that the volume and dollar value of AMD's domestic inventory is commercially significant. Accordingly, it is recommended that a CDO issue against AMD should a violation be found, although it may be that public interest factors justify a warranty and repair exemption for disposition of the domestic inventory.

C. Bond

The Commission has held that "[t]he complainant bears the burden of establishing the need for a bond" during the Presidential Review period. *See Robotic Vacuums*, Inv. No. 337-TA-1057, Comm'n Op. at 68. The amount of the bond is, generally, set "to be sufficient to protect the

complainant from any injury." 19 U.S.C. § 1337(e)(1), (j3). Realtek contends "there is no evidence from AMD regarding a price differential, or any license agreements tending to prove what a royalty rate should be in this case, and the bond should be set at 100%." CIB at 397 (citing Hr'g Tr. (Sheridan) at 678:23-679:12. AMD argues for zero bond because there is no injury. RIB at 297. AMD states, "AMD imports [redacted] of dollars of the accused products annually, whereas Realtek has identified [redacted] of its own products.. . . Realtek has therefore suffered no injury and has lost no customers or sales." *Id.* (citations omitted). AMD further suggests that a bond should not be used to protect the products of alleged licensees, like Broadcom Corp. *Id.*

AMD is persuasive in that Realtek has not met its burden. A bond is not an automatic remedy. *See Certain Table Saws Incorporating Active Injury Mitigation Technology and Components Thereof*, Inv. No. 337-TA-965, Comm'n Op. at 15-16 (Feb. 1, 2017). And there would appear to be no competition between the Bluetooth/Wi-Fi chips that are the DI Products and the CPU/GPU Accused Products, if the DI Products can even be considered the interest of Realtek. Thus, no injury is shown or implied by the record evidence. Accordingly, it is not recommended that a bond issue in the event of a violation.

X. INITIAL DETERMINATION AND ORDER

Based on the foregoing,[1] it is my Initial Determination that there is no violation of Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits, components thereof, and products containing the same in connection with the

[1] The failure to discuss any matter raised by the parties or any portion of the Record herein does not indicate that said matter was not considered. Rather, any such matter(s) or portion(s) of the Record has/have been determined to be irrelevant, immaterial or meritless. Arguments made on brief which were otherwise unsupported by Record evidence or legal precedent have been accorded no weight.

asserted claims of U.S. Patent No. 7,936,245, U.S. Patent No. 8,006,218, or U.S. Patent No. 9,590,582.

The undersigned hereby certifies to the Commission this Initial Determination, together with the Record of the hearing in this investigation consisting of the following: the transcript of the evidentiary hearing, with appropriate corrections as may hereafter be ordered; and the exhibits accepted into evidence in this investigation.[2]

Pursuant to 19 C.F.R. § 210.42(h), this Initial Determination shall become the determination of the Commission sixty (60) days after the date of service of the Initial Determination, unless a party files a petition for review of the Initial Determination within twelve (12) days after service of the Initial Determination pursuant to 19 C.F.R. § 210.43(a) or the Commission, pursuant to 19 C.F.R. § 210.44, orders on its own motion, a review of the Initial Determination or certain issues therein. Any issue or argument not raised in a petition for review, or response thereto, will be deemed to have been abandoned and may be disregarded by the Commission in reviewing the Initial Determination pursuant to 19 C.F.R. § 210.43(b) and (c).

[2] The pleadings of the parties filed with the Secretary need not be certified as they are already in the Commission's possession in accordance with Commission rules.

Confidentiality Notice:

This Initial Determination is being issued as confidential, and a public version will be issued pursuant to Commission Rule 210.5(f). Within seven (7) days of the date of this Initial Determination, the parties shall jointly submit: (1) a proposed public version of this opinion with any proposed redactions bracketed in red; and (2) a written justification for any proposed redactions specifically explaining why the piece of information sought to be redacted is confidential and why disclosure of the information would be likely to cause substantial harm or likely to have the effect of impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions.[3]

SO ORDERED.

Cameron Elliot
Administrative Law Judge

[3] Under Commission Rules 210.5 and 201.6(a), confidential business information includes: information which concerns or relates to the trade secrets, processes, operations, style of works, or apparatus, or to the production, sales, shipments, purchases, transfers, identification of customers, inventories, or amount or source of any income, profits, losses, or expenditures of any person, firm, partnership, corporation, or other organization, or other information of commercial value, the disclosure of which is likely to have the effect of either impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions, or causing substantial harm to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained, unless the Commission is required by law to disclose such information. *See* 19 C.F.R. § 201.6(a). Thus, to constitute confidential business information the disclosure of the information sought to be designated confidential must likely have the effect of either: (1) impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions; or (2) causing substantial harm to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained.