US006130602A

United States Patent [19]

O'Toole et al.

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[45] Date of Patent: *Oct. 10, 2000

[54] **RADIO FREQUENCY DATA COMMUNICATIONS DEVICE**

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[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/705,043**

[22] Filed: **Aug. 29, 1996**

Related U.S. Application Data

[60] Provisional application No. 60/017,900, May 13, 1996.

[51] **Int. Cl.**[7] **H04Q 7/00**

[52] **U.S. Cl.** **340/10.33**; 342/42; 342/44; 342/51

[58] **Field of Search** 340/825.54, 825.34, 340/572, 572.1, 10.33; 342/42, 44, 51; 455/343, 20; 375/21

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,299,424	1/1967	Vinding .	
3,852,755	12/1974	Works et al. .	
4,075,632	2/1978	Baldwin et al. .	
4,572,976	2/1986	Fockens	307/524
4,656,463	4/1987	Anders et al.	340/572
4,700,179	10/1987	Fancher .	
4,724,427	2/1988	Carroll	340/572
4,743,864	5/1988	Nakagawa et al.	455/343 X
4,800,543	1/1989	Lyndon-James et al. .	
4,816,839	3/1989	Landt .	
4,827,395	5/1989	Anders et al. .	
4,853,705	8/1989	Landt .	
4,854,328	8/1989	Pollack	128/736
4,857,893	8/1989	Carroll	340/572
4,862,160	8/1989	Ekchian et al.	340/825.54

(List continued on next page.)

OTHER PUBLICATIONS

"Micron RFID Communications Protocol Manual," Jul. 22, 1993, Pre–Release Version 0.95, pp. 1–71.

Provisional Application, Ser. No. 60/023,321, Filed Jul. 30, 1996.

Provisional Application, Ser. No. 60/023,318, Filed Jul. 30, 1996.

"CMOS Analog Integrated Circuits Based on Weak Inversion Operation", Eric Vittoz and Jean Fellrath, IEEE Journal of Solid State Circuits, vol. SC–12, No. 3, Jun. 1977.

Mitsubishi Motors Corporation Web Page, 1995, "Eclipse" Safety and Security http://www.mitsubishi–motors.co.jp . . .r/products/ECLIPSE/eclipse_04.html.

"Digital RF/ID Enhances GPS", by John R. Tuttle, Proceedings of the Second Annual Wireless Symposium, pp.406–411, Feb. 15–18, 1994, Santa Clara, CA.

"*Micron Morning Report*", The Idaho Statesman, Jul. 16, 1993.

"*A Low–Power Spread Spectrum CMOS RFIC for Radio Identification Applications*", by John R. Tuttle, Conference Proceedings from RF Expo West, pp. 216–222, Mar. 22–24, 1994, San Jose, CA.

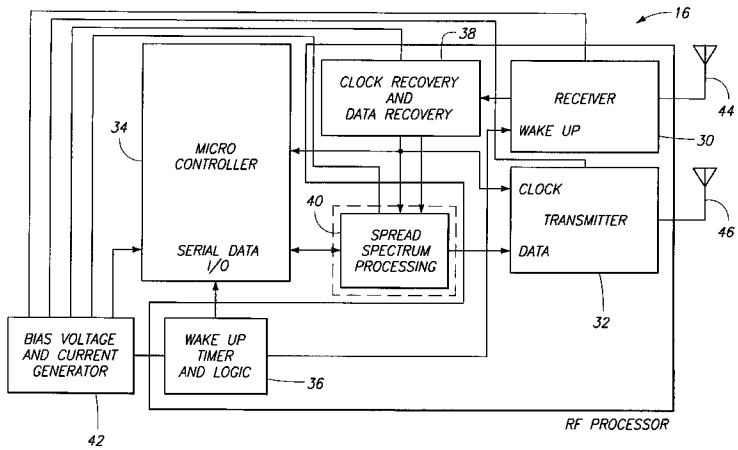
Primary Examiner—Edwin C. Holloway, III

Attorney, Agent, or Firm—Wells, St. John, Roberts, Gregory & Matkin, P.S.

[57] **ABSTRACT**

A radio frequency identification device comprises an integrated circuit including a receiver, a transmitter, and a microprocessor. The receiver and transmitter together define an active transponder. The integrated circuit is preferably a monolithic single die integrated circuit including the receiver, the transmitter, and the microprocessor. Because the device includes an active transponder, instead of a transponder which relies on magnetic coupling for power, the device has a much greater range.

17 Claims, 3273 Drawing Sheets



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Apple EX1023 Page 1

U.S. PATENT DOCUMENTS

4,870,419	9/1989	Baldwin et al.	342/50
4,888,591	12/1989	Landt et al.	342/44
4,890,072	12/1989	Espe et al.	331/11
4,912,471	3/1990	Tyburski et al.	342/42
4,926,182	5/1990	Ohta et al.	342/44
5,030,807	7/1991	Landt et al. .	
5,075,691	12/1991	Garay et al. .	
5,081,458	1/1992	Meunier	342/44
5,086,389	2/1992	Hassett et al.	364/401
5,128,938	7/1992	Borras	455/343 X
5,130,668	7/1992	Emslie et al.	330/281
5,134,085	7/1992	Gilgen et al.	437/52
5,142,292	8/1992	Chang .	
5,144,314	9/1992	Malmberg et al.	342/44
5,153,583	10/1992	Murdoch	340/825.54
5,164,985	11/1992	Nysen et al.	380/9
5,175,774	12/1992	Truax et al.	382/8
5,231,273	7/1993	Caswel	235/385
5,272,367	12/1993	Dennison et al.	257/306
5,287,112	2/1994	Schuermann	342/42
5,300,875	4/1994	Tuttle	320/20
5,311,186	5/1994	Utsu et al.	342/51
5,323,150	6/1994	Tuttle	340/825.54
5,355,513	10/1994	Clarke et al.	455/20
5,365,551	11/1994	Snodgrass et al.	375/1
5,374,930	12/1994	Schuermann	342/42
5,394,444	2/1995	Silvey et al.	327/156
5,406,263	4/1995	Tuttle	340/572
5,420,757	5/1995	Eberhardt et al.	361/813
5,430,441	7/1995	Bickley et al. .	
5,444,223	8/1995	Blama .	
5,448,110	9/1995	Tuttle et al. .	
5,448,242	9/1995	Sharpe et al.	342/42
5,450,087	9/1995	Hurta et al.	342/42
5,461,385	10/1995	Armstrong	342/42
5,471,212	11/1995	Sharpe et al.	342/51
5,478,991	12/1995	Watanabe et al. .	
5,489,546	2/1996	Ahmad et al.	437/57
5,499,214	3/1996	Mori et al.	365/222
5,500,650	3/1996	Snodgrass et al.	342/42
5,525,992	6/1996	Froschermeier	342/42
5,541,583	7/1996	Mandelbaum .	
5,541,585	7/1996	Duhame et al. .	
5,568,512	10/1996	Rotzoll	375/211
5,606,323	2/1997	Heinrich et al.	342/51
5,621,412	4/1997	Sharpe et al.	342/51
5,649,296	7/1997	MacLellan et al.	455/38.2
5,657,359	8/1997	Sakae et al.	327/157
5,677,667	10/1997	Lesesky et al.	340/431
5,686,864	11/1997	Martin et al.	327/159
5,686,920	11/1997	Hurta et al.	342/42
5,719,550	2/1998	Bloch et al.	340/426
5,721,678	2/1998	Widl	364/424.04
5,721,783	2/1998	Anderson	381/68.6
5,726,630	3/1998	Marsh et al.	340/572
5,815,042	9/1998	Chow et al.	331/57

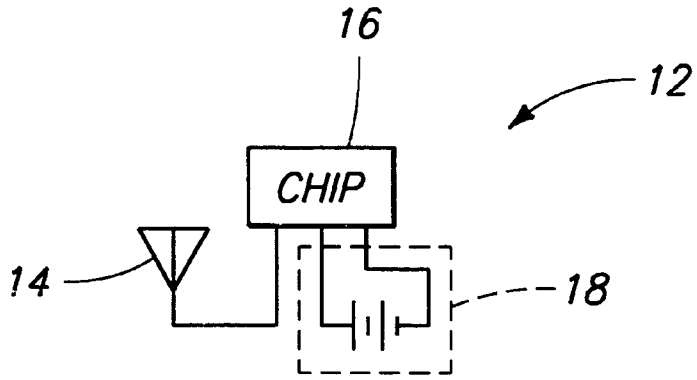


Fig. 1

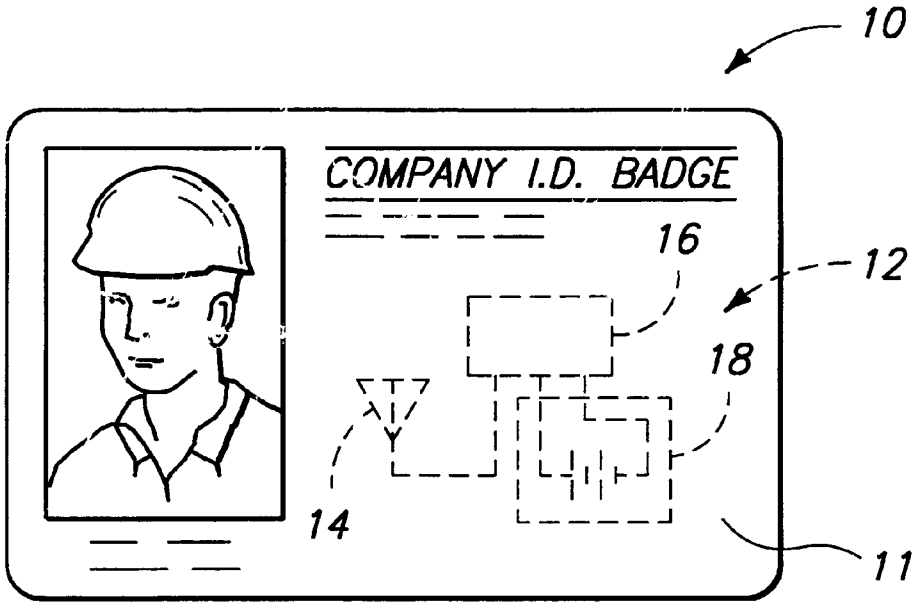


Fig. 2

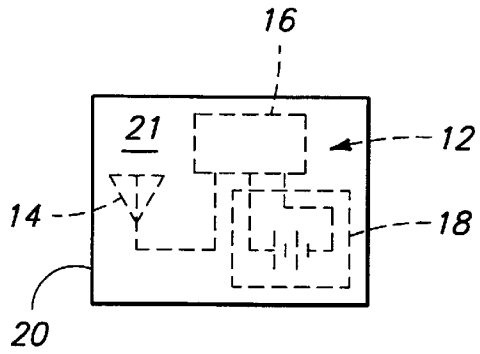

16
21
12
14
18
20

Fig. 3

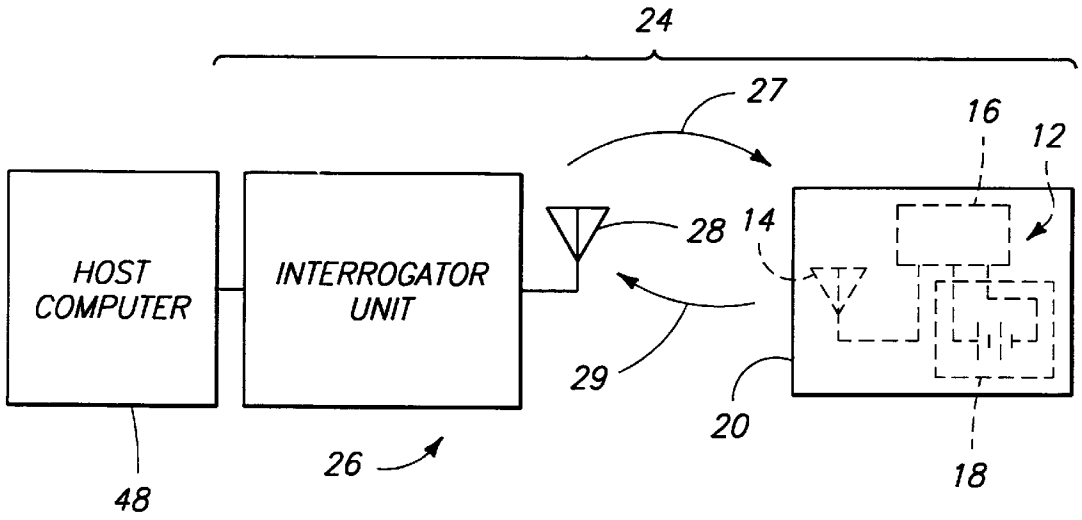

24
27
16
12
28
14
HOST COMPUTER
INTERROGATOR UNIT
29
20
26
48
18

Fig. 4

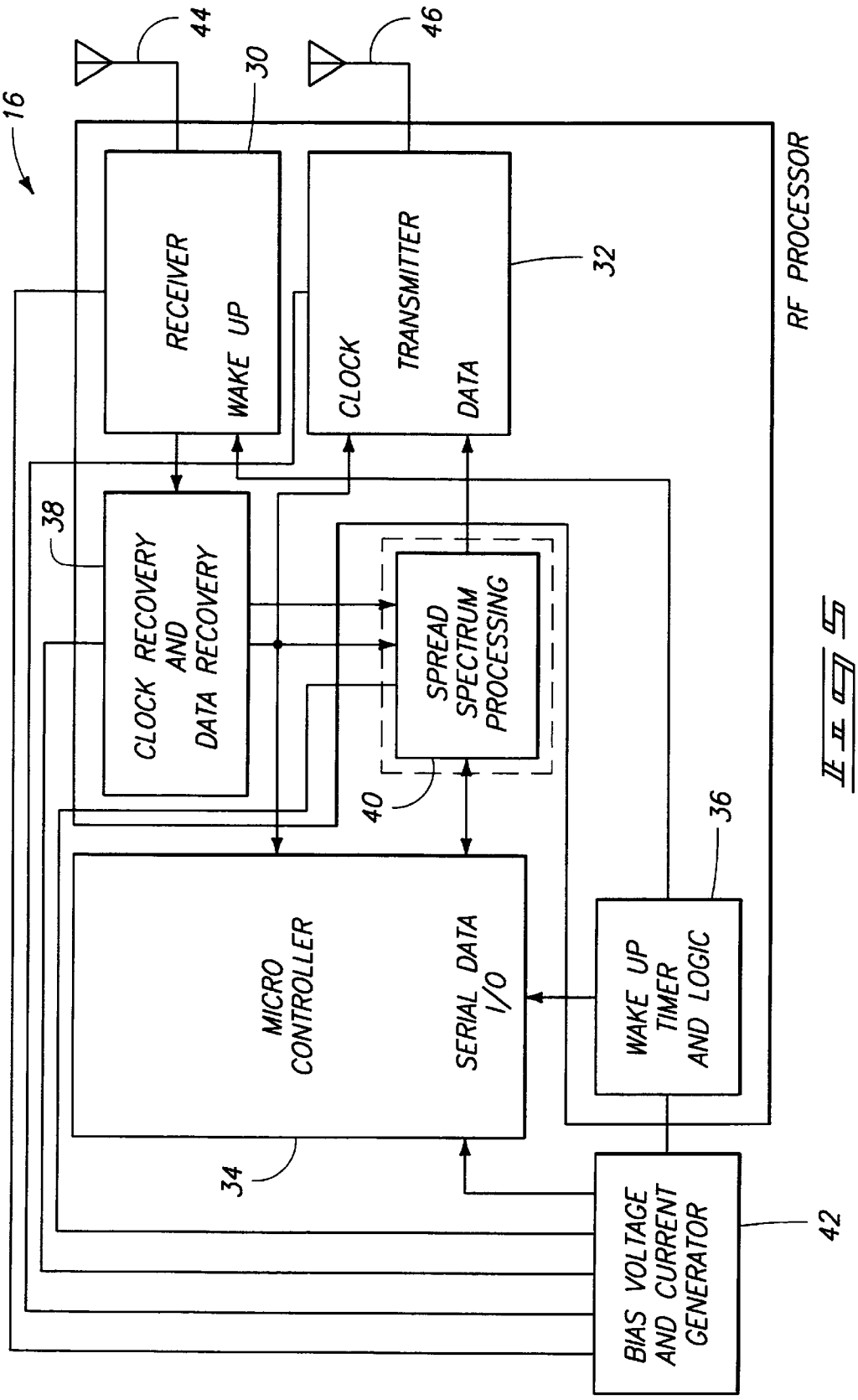
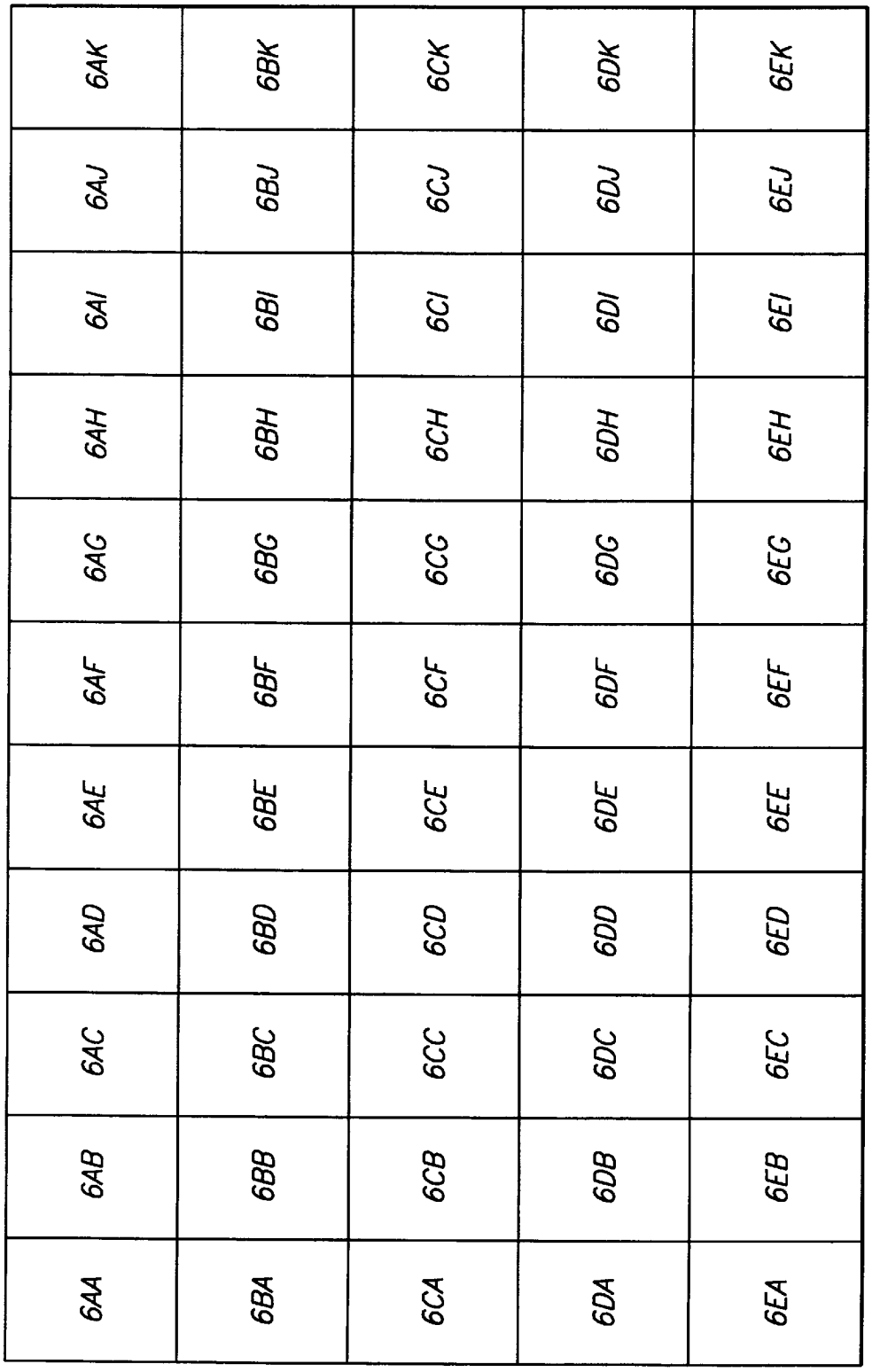

16
44
46
30
RECEIVER
WAKE UP
CLOCK
TRANSMITTER
DATA
32
RF PROCESSOR
38
CLOCK RECOVERY AND DATA RECOVERY
SPREAD SPECTRUM PROCESSING
40
36
MICRO CONTROLLER
SERIAL DATA I/O
WAKE UP TIMER AND LOGIC
34
BIAS VOLTAGE AND CURRENT GENERATOR
42

FIG 5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6BA 6BB 6BC 6BD 6BE 6BF 6BG 6BH 6BI 6BJ 6BK
6CA 6CB 6CC 6CD 6CE 6CF 6CG 6CH 6CI 6CJ 6CK
6DA 6DB 6DC 6DD 6DE 6DF 6DG 6DH 6DI 6DJ 6DK
6EA 6EB 6EC 6ED 6EE 6EF 6EG 6EH 6EI 6EJ 6EK

FIG 6

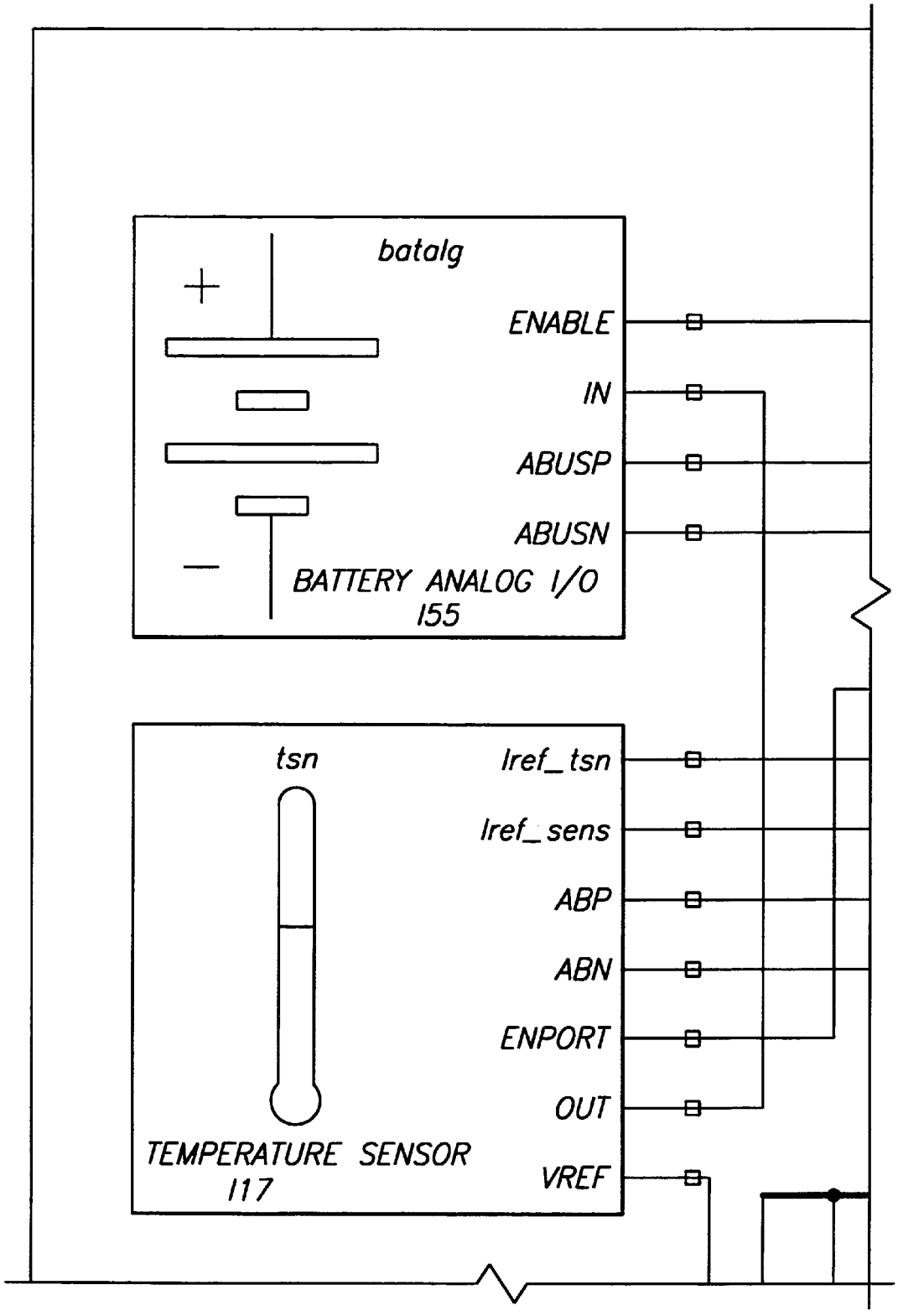

batalg
ENABLE
IN
ABUSP
ABUSN
BATTERY ANALOG I/O
155
tsn
Iref_tsn
Iref_sens
ABP
ABN
ENPORT
OUT
VREF
TEMPERATURE SENSOR
117

Fig 6AA

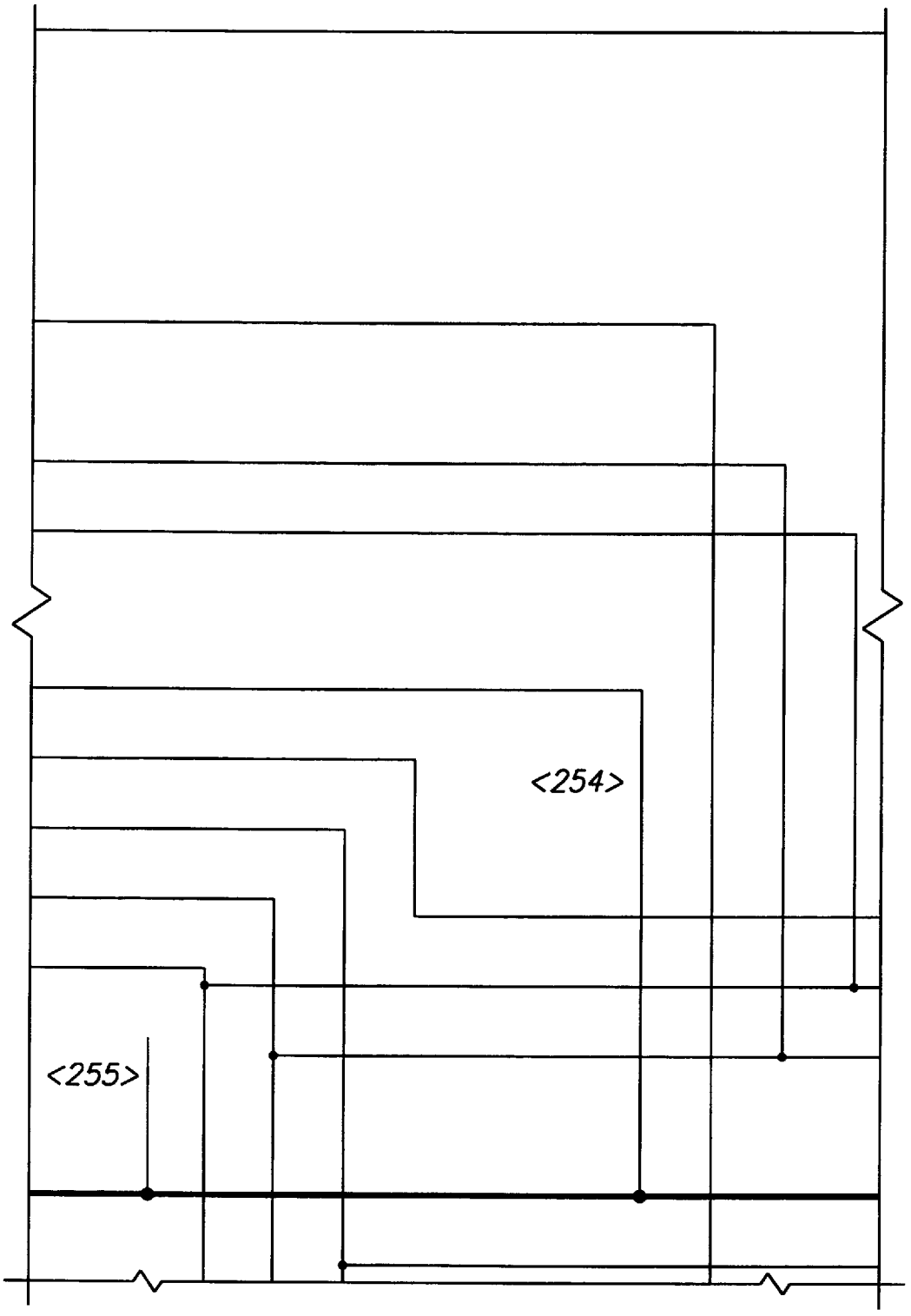


Fig 6AB

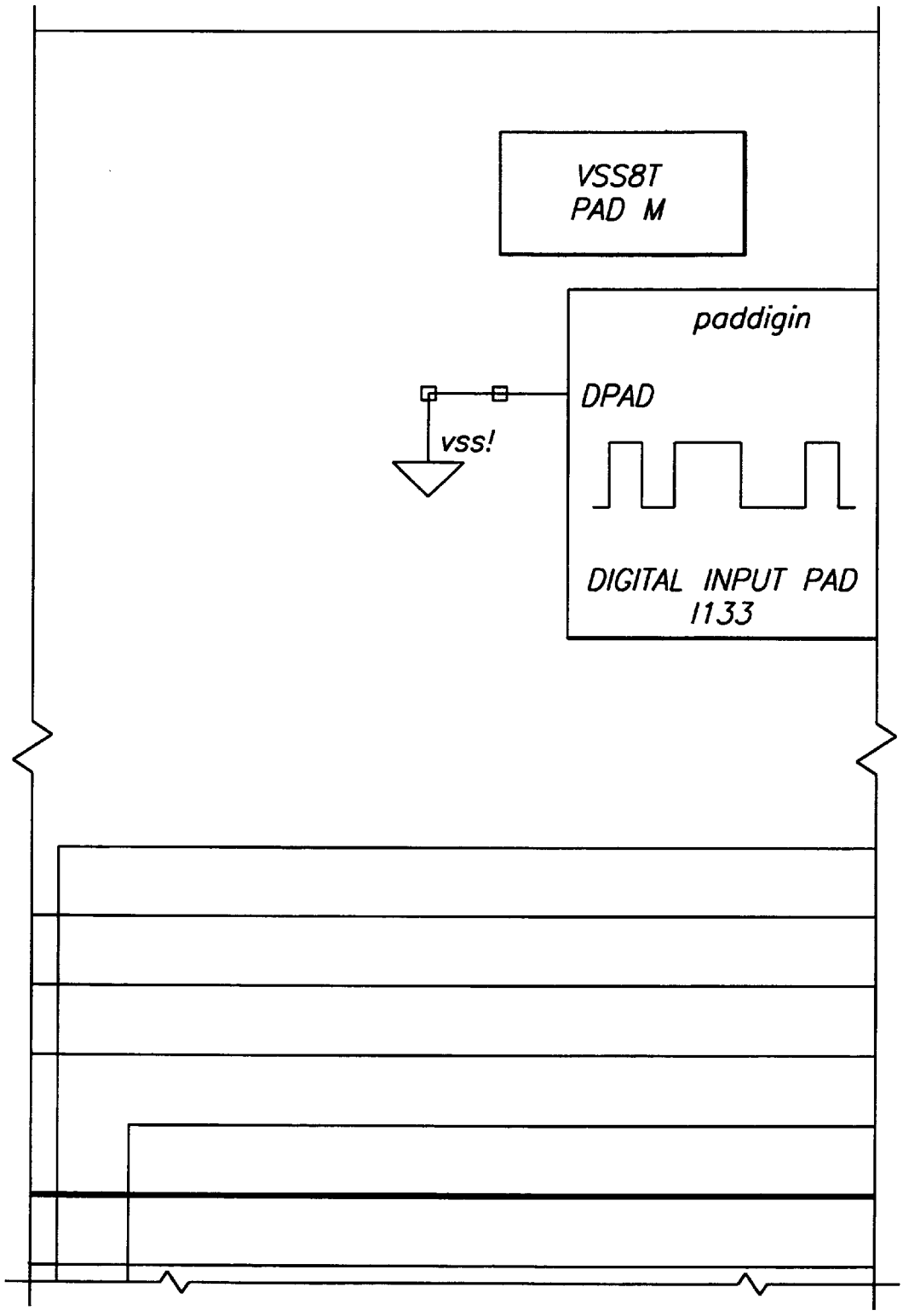


Fig 6AC

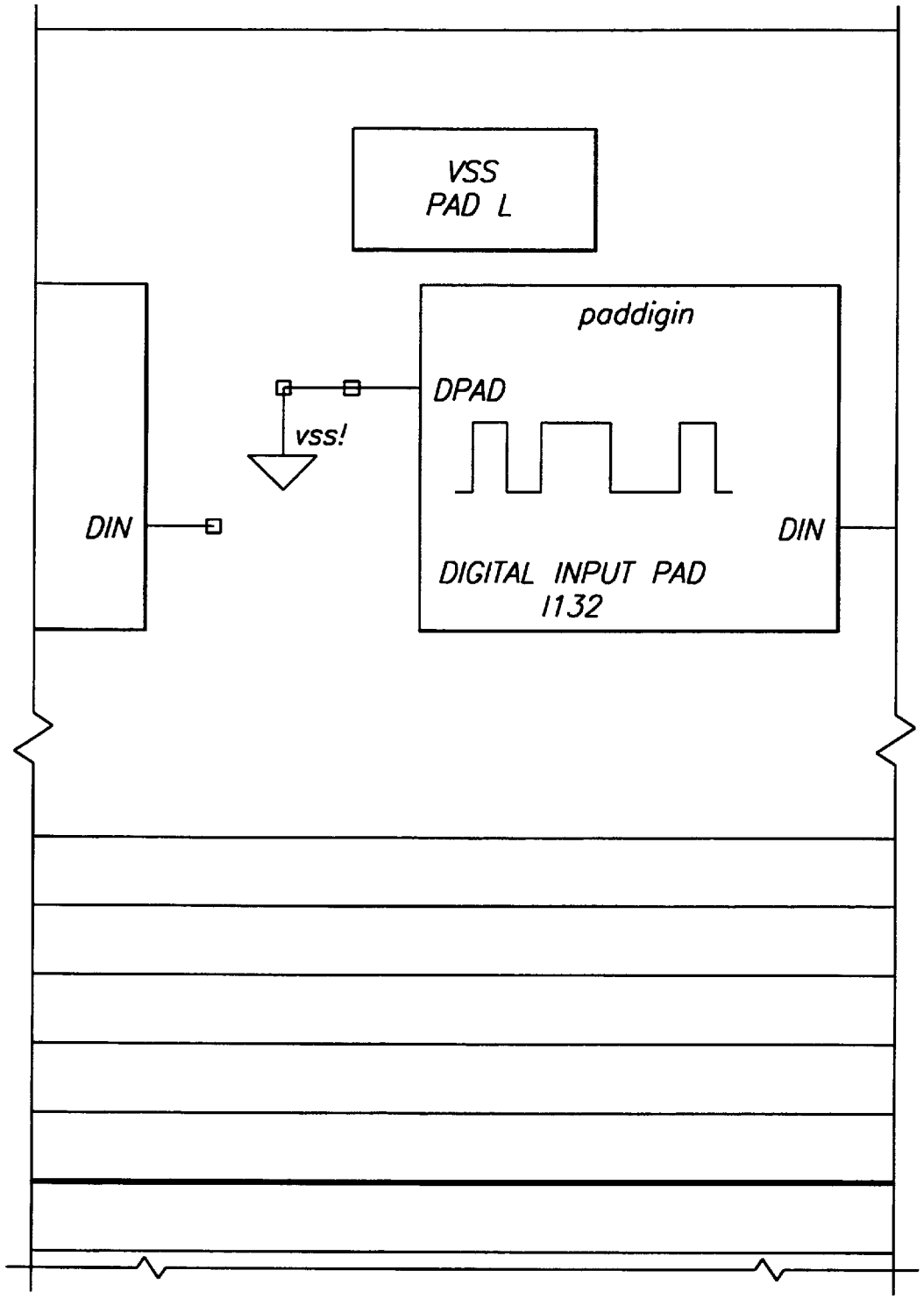


FIG 6AD

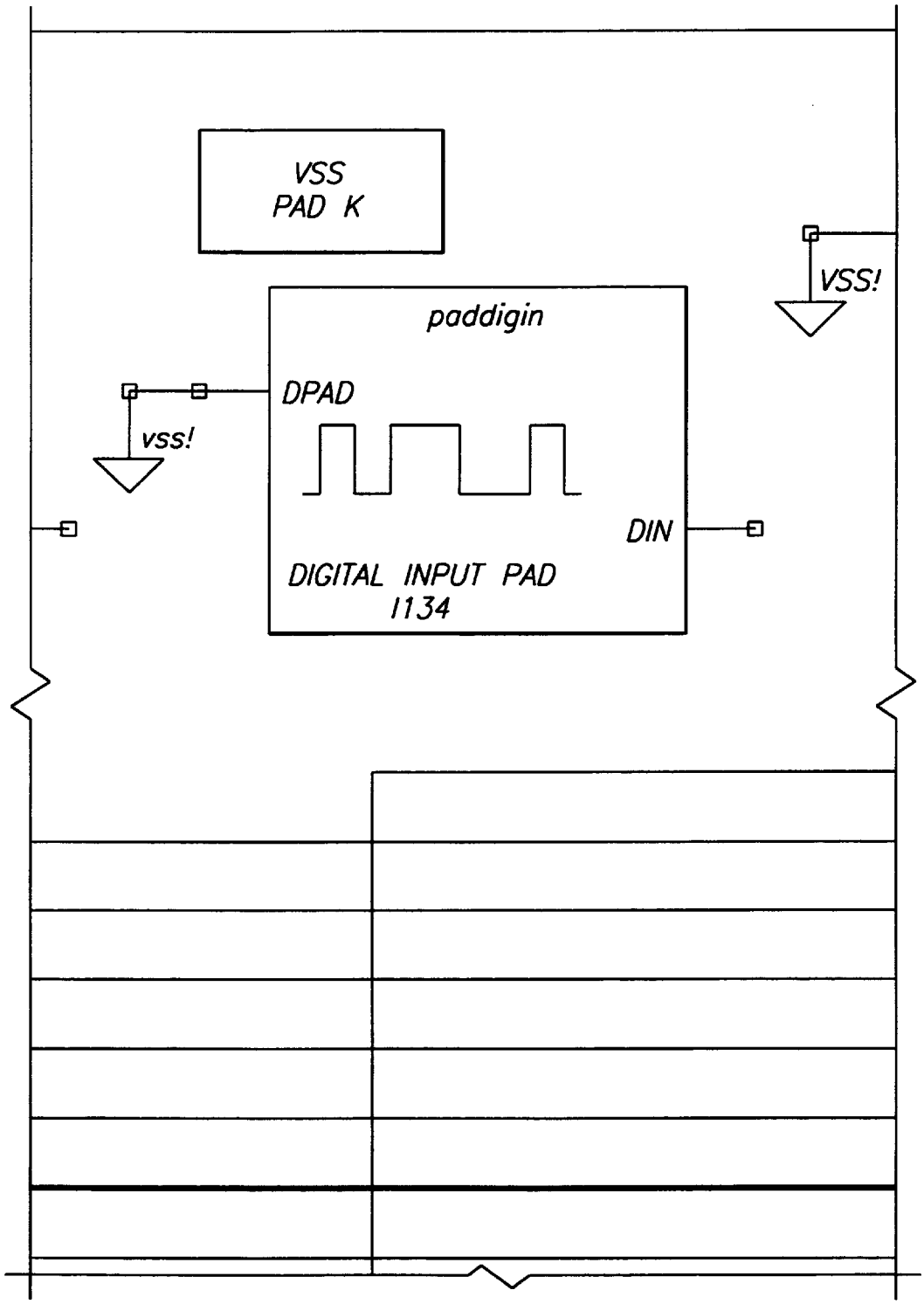


Fig 6AE

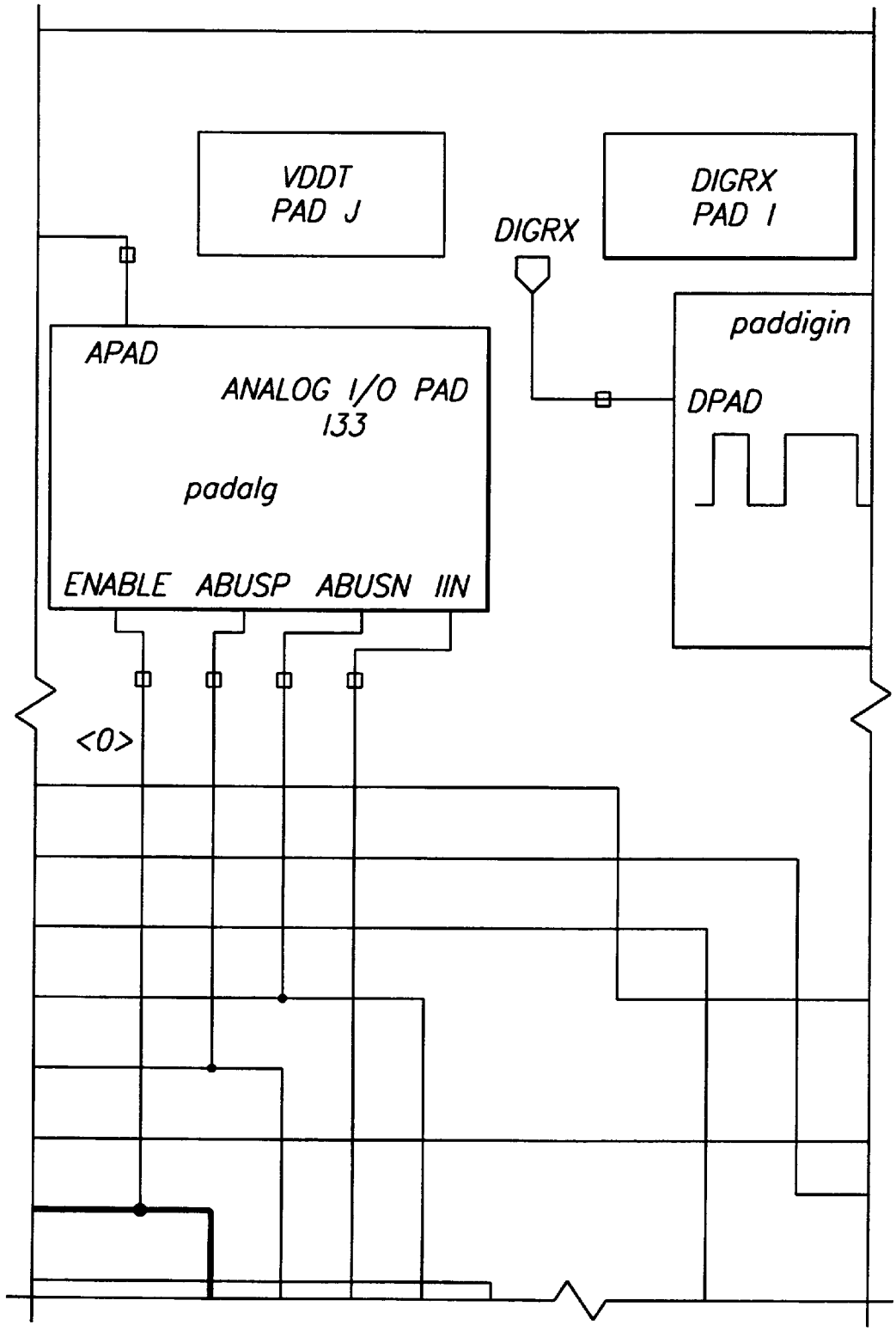

VDDT
PAD J
DIGRX
PAD I
DIGRX
paddigin
APAD
ANALOG I/O PAD
133
padalg
DPAD
ENABLE ABUSP ABUSN IIN
<0>

FIG 6AF

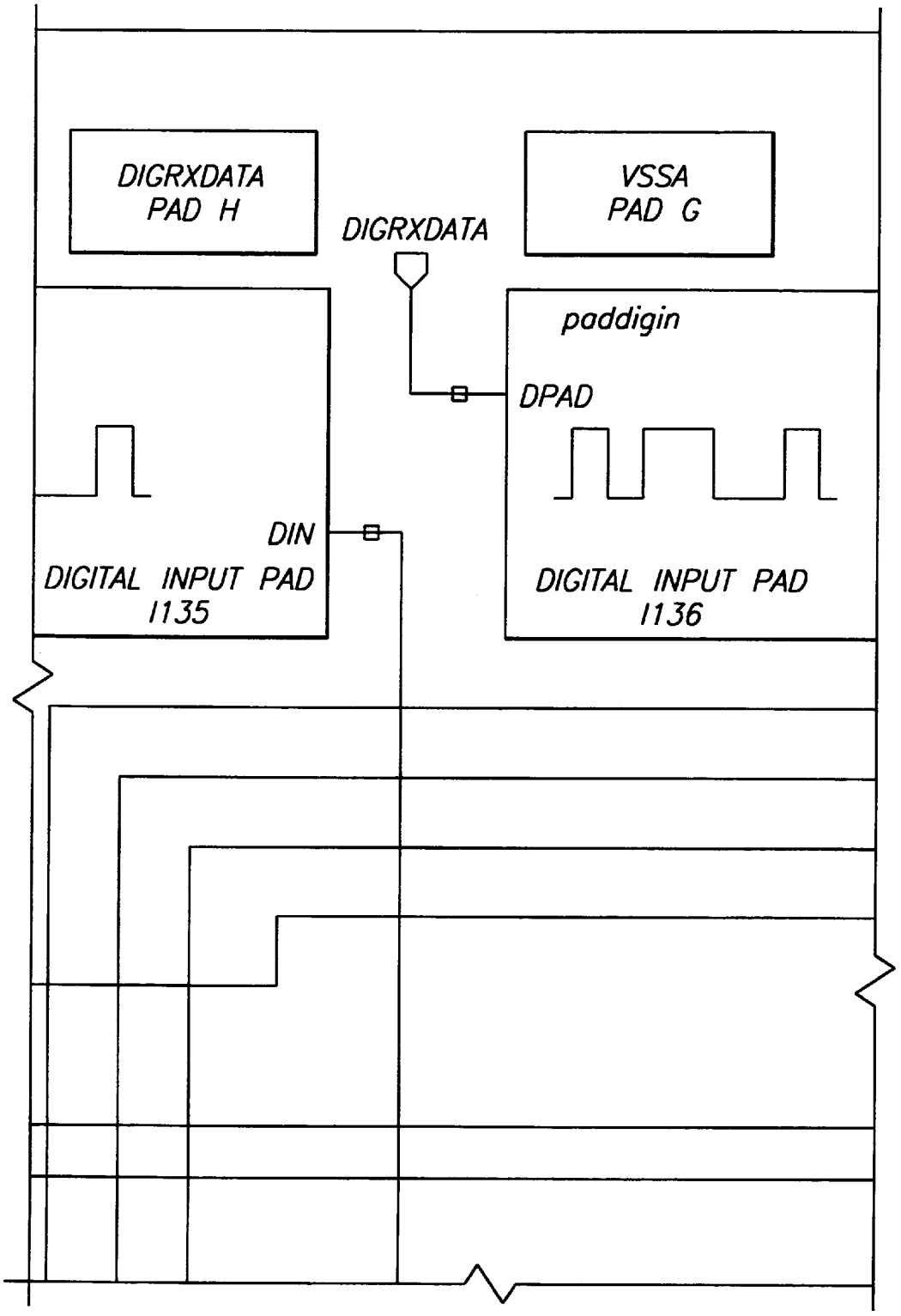

DIGRXDATA
PAD H
DIGRXDATA
VSSA
PAD G
paddigin
DPAD
DIN
DIGITAL INPUT PAD
1135
DIGITAL INPUT PAD
1136

Fig 6AG

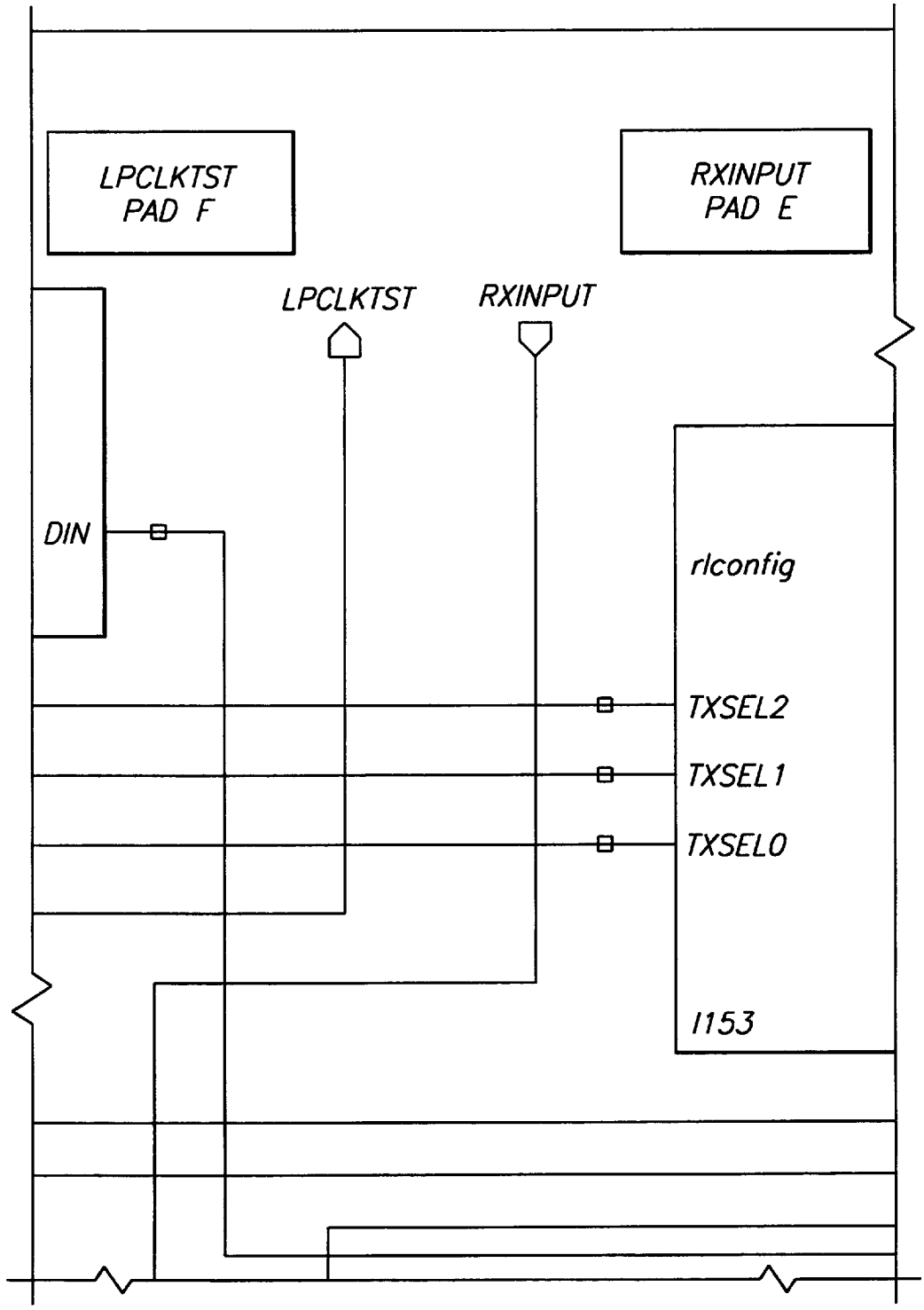

LPCLKTST
PAD F
RXINPUT
PAD E
LPCLKTST
RXINPUT
DIN
rlconfig
TXSEL2
TXSEL1
TXSEL0
1153

Fig 6AH

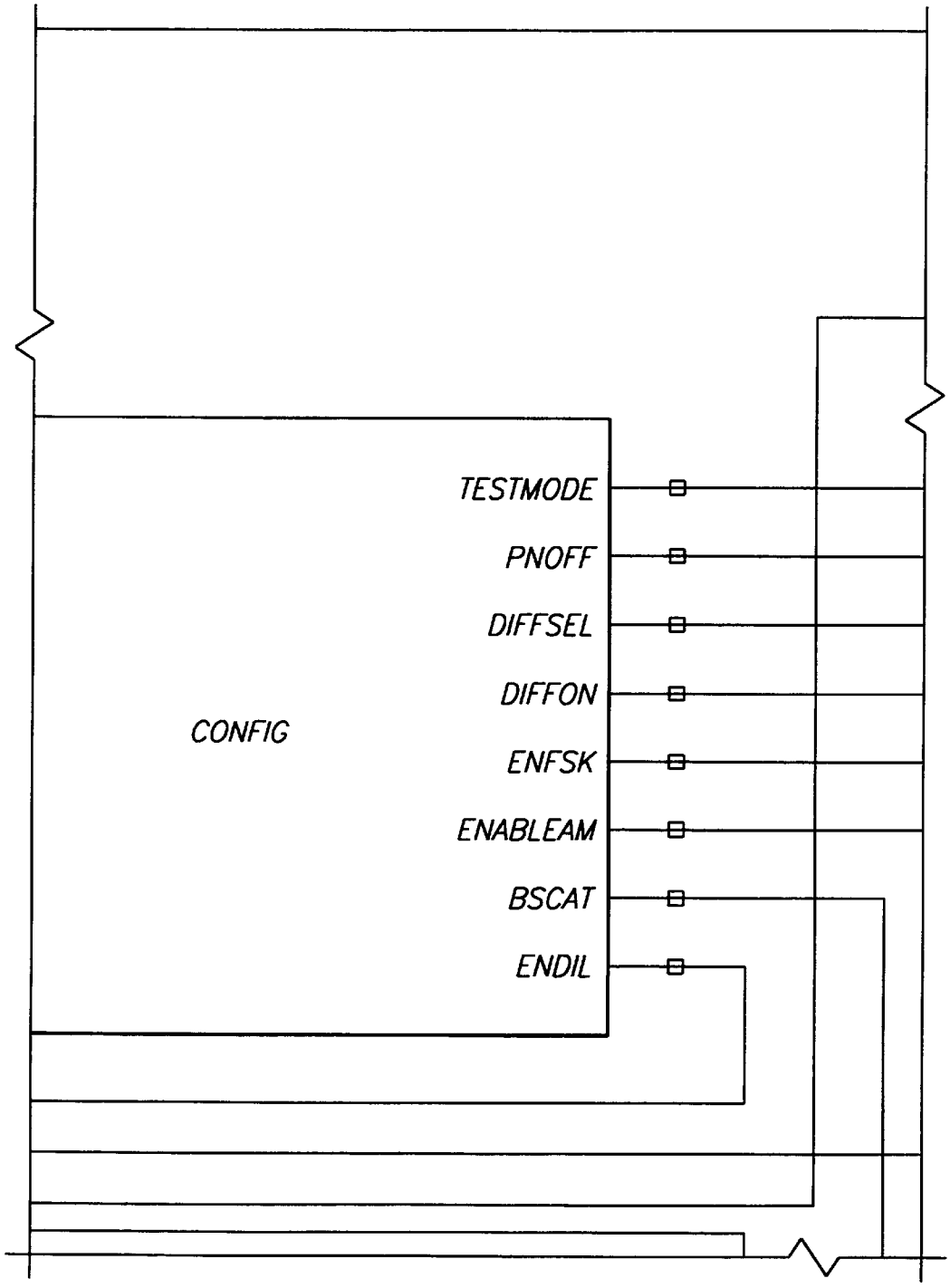

CONFIG
TESTMODE
PNOFF
DIFFSEL
DIFFON
ENFSK
ENABLEAM
BSCAT
ENDIL

Fig 6A II

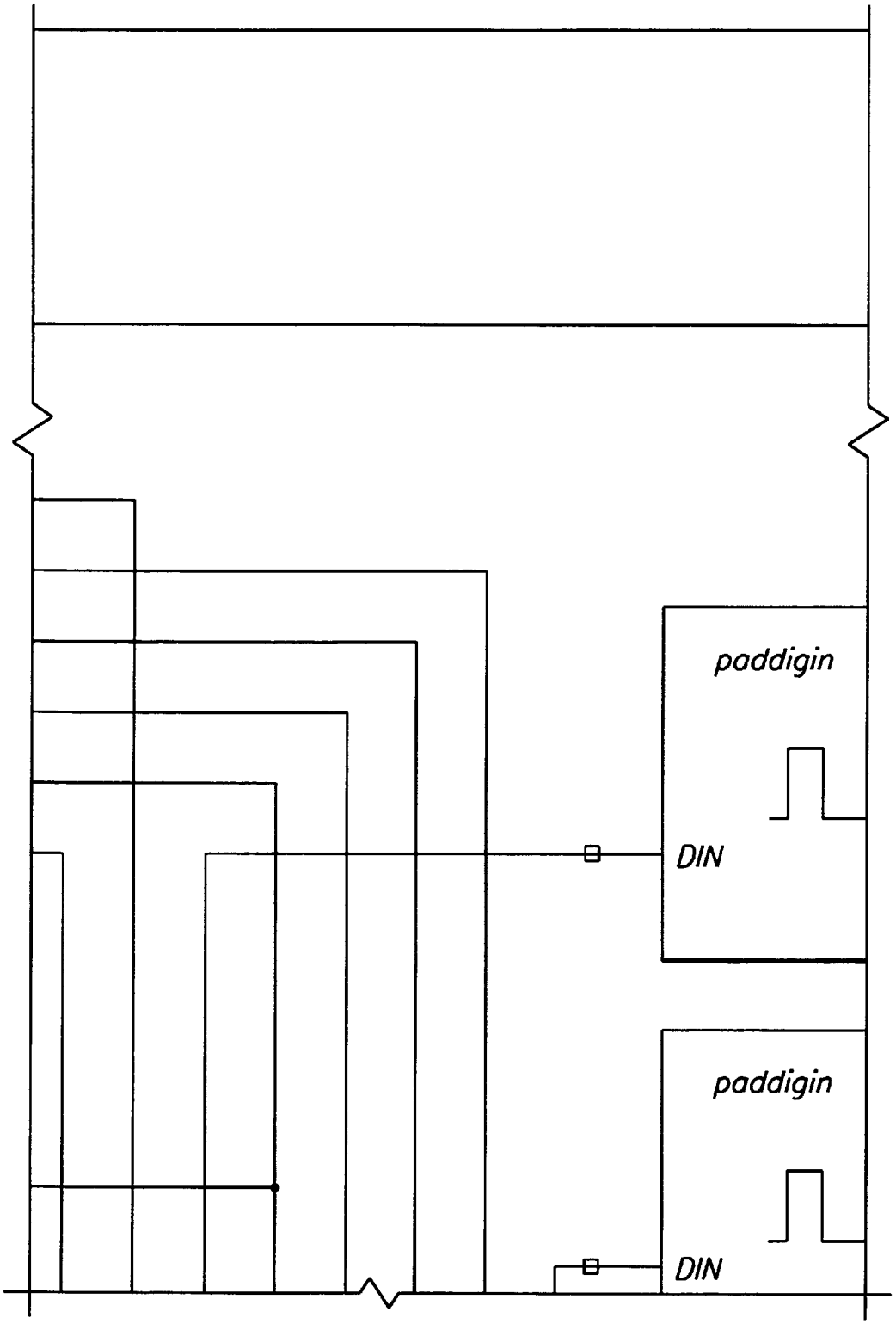


Fig 6Ad

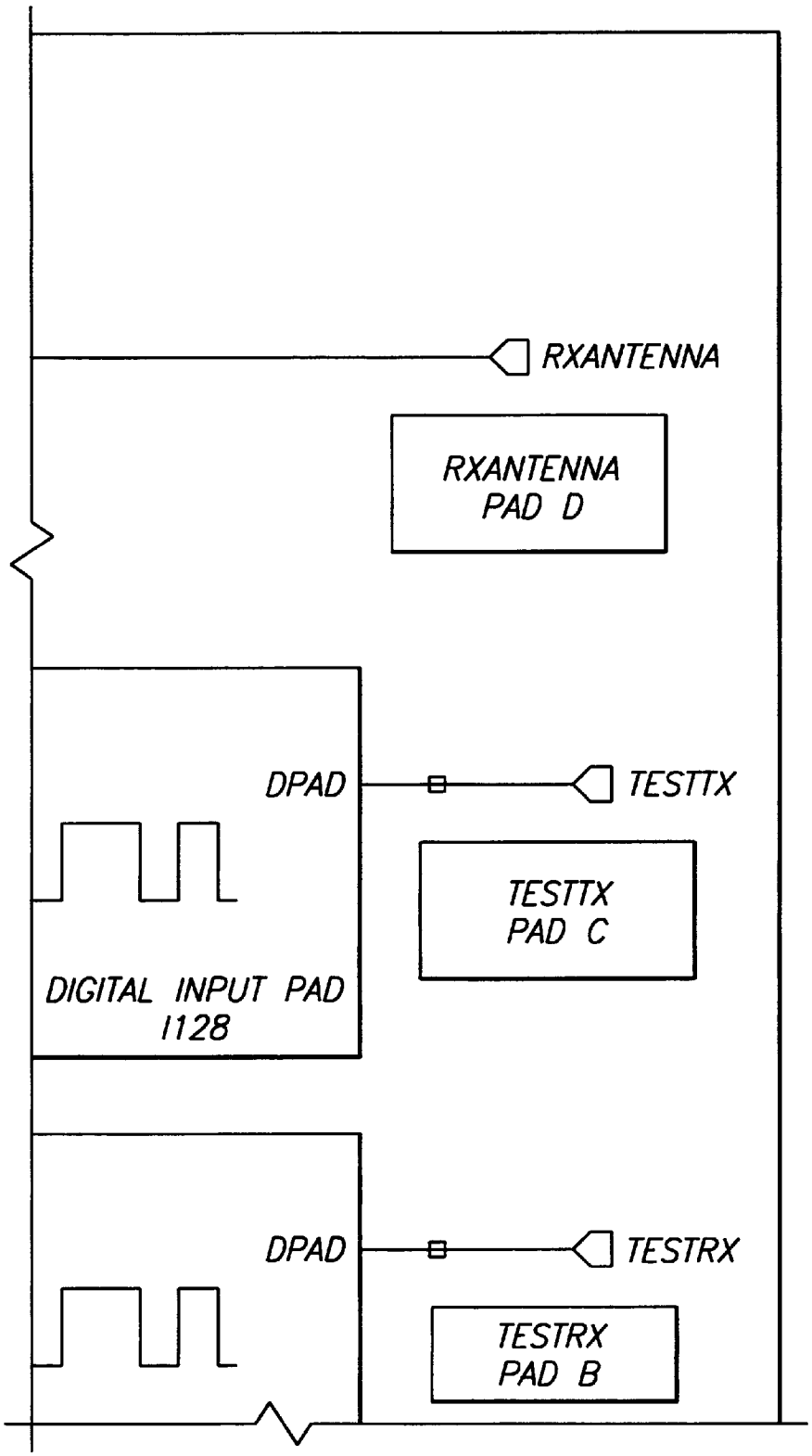

RXANTENNA
RXANTENNA
PAD D
DPAD
TESTTX
TESTTX
PAD C
DIGITAL INPUT PAD
1128
DPAD
TESTRX
TESTRX
PAD B

Fig 64K

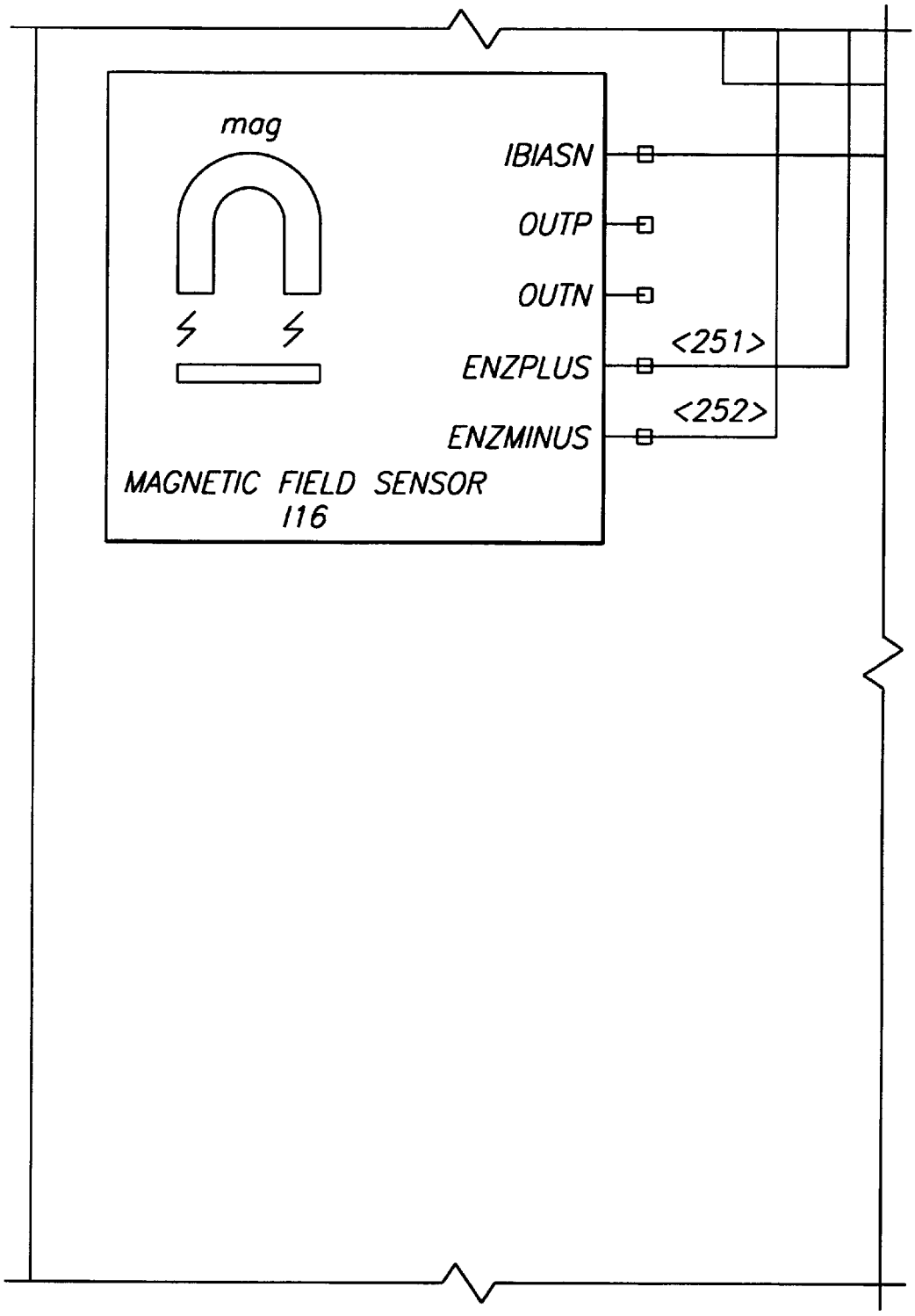

mag
IBIASN
OUTP
OUTN
<251>
ENZPLUS
<252>
ENZMINUS
MAGNETIC FIELD SENSOR
116

FIG 6BA

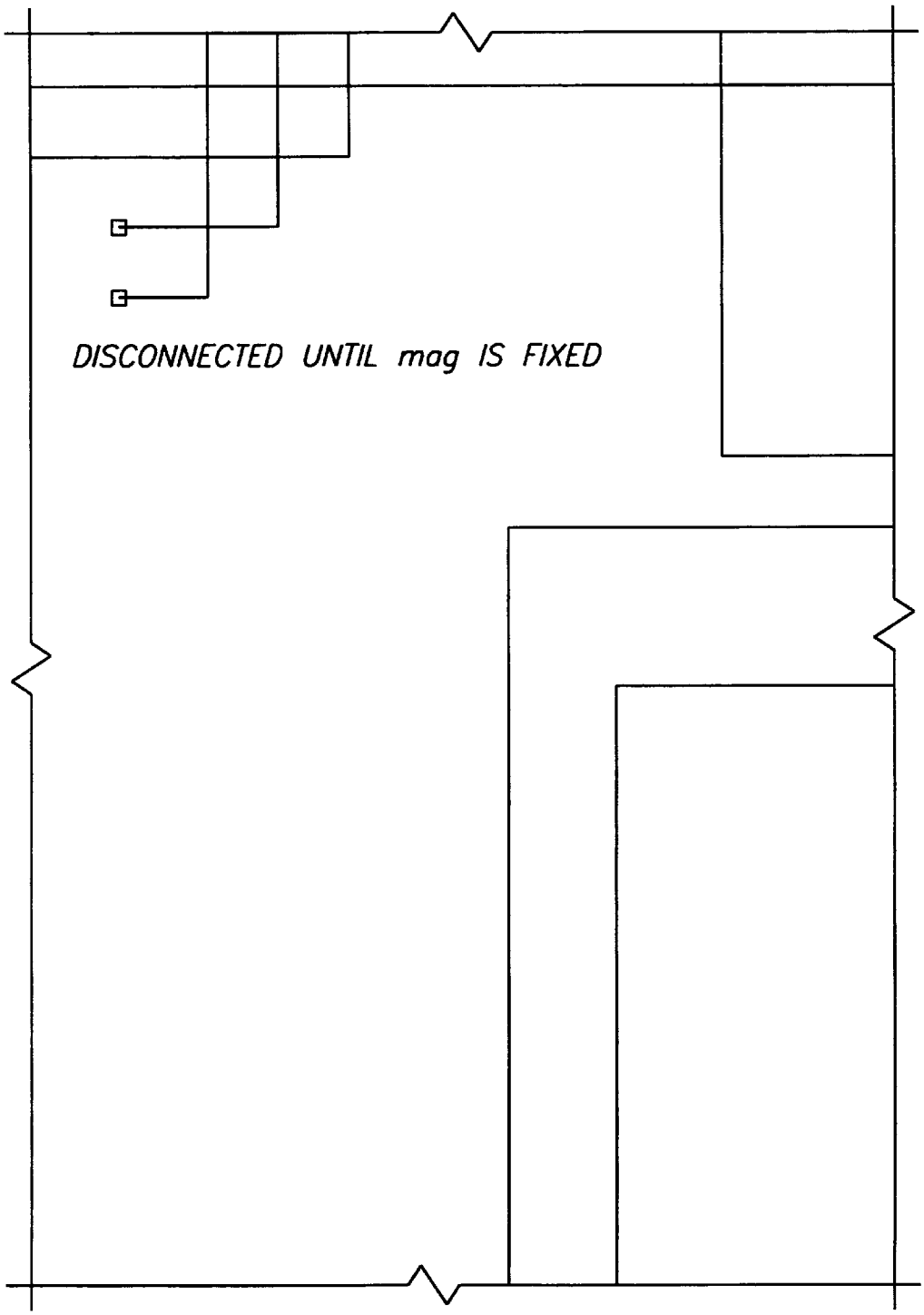


Fig 6BB

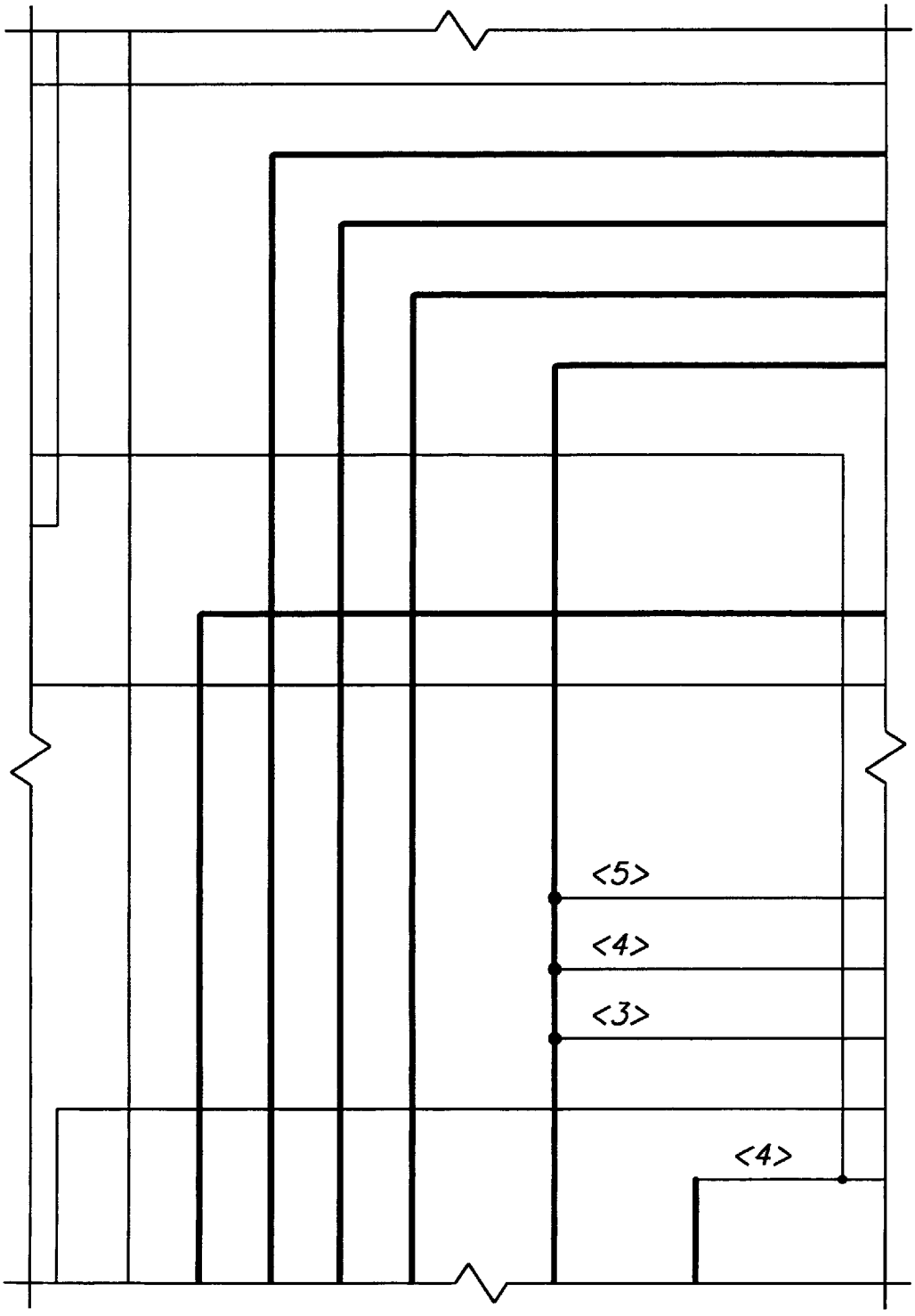


Fig 6BC

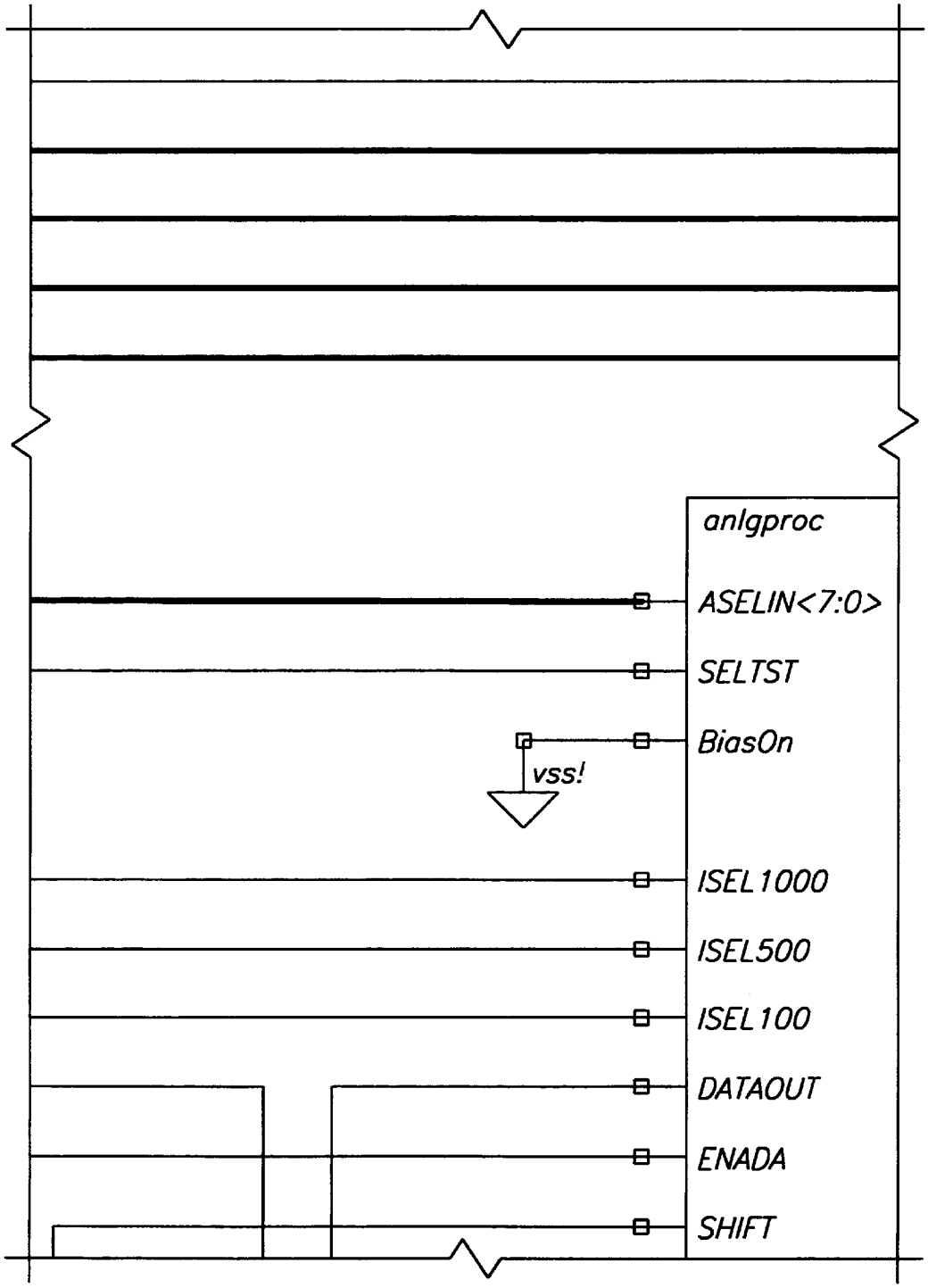

anlgproc
ASELIN<7:0>
SELTST
BiasOn
vss!
ISEL1000
ISEL500
ISEL100
DATAOUT
ENADA
SHIFT

Fig 6BD

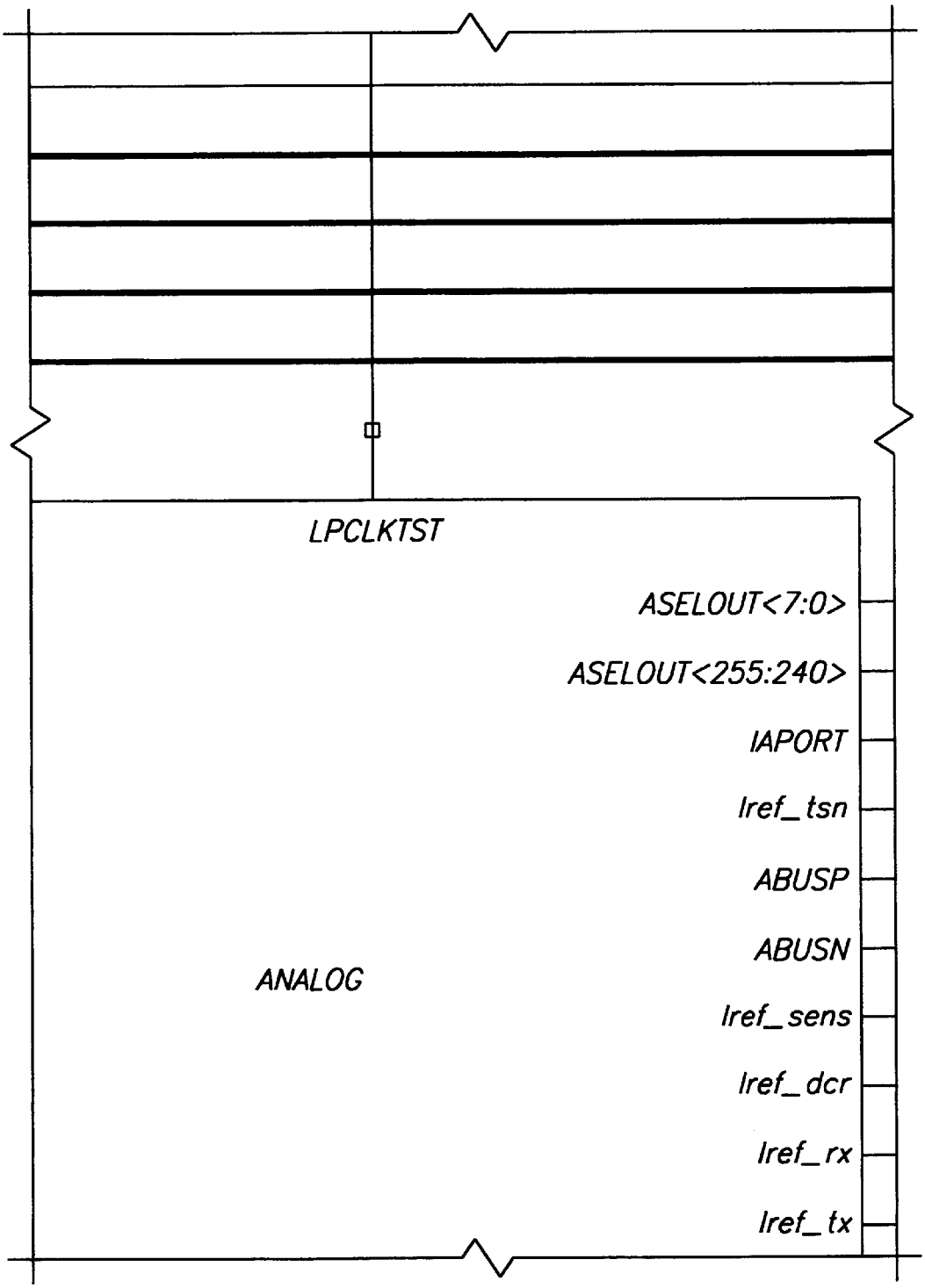

LPCLKTST
ASELOUT<7:0>
ASELOUT<255:240>
IAPORT
Iref_tsn
ABUSP
ABUSN
ANALOG
Iref_sens
Iref_dcr
Iref_rx
Iref_tx

Fig 6BE

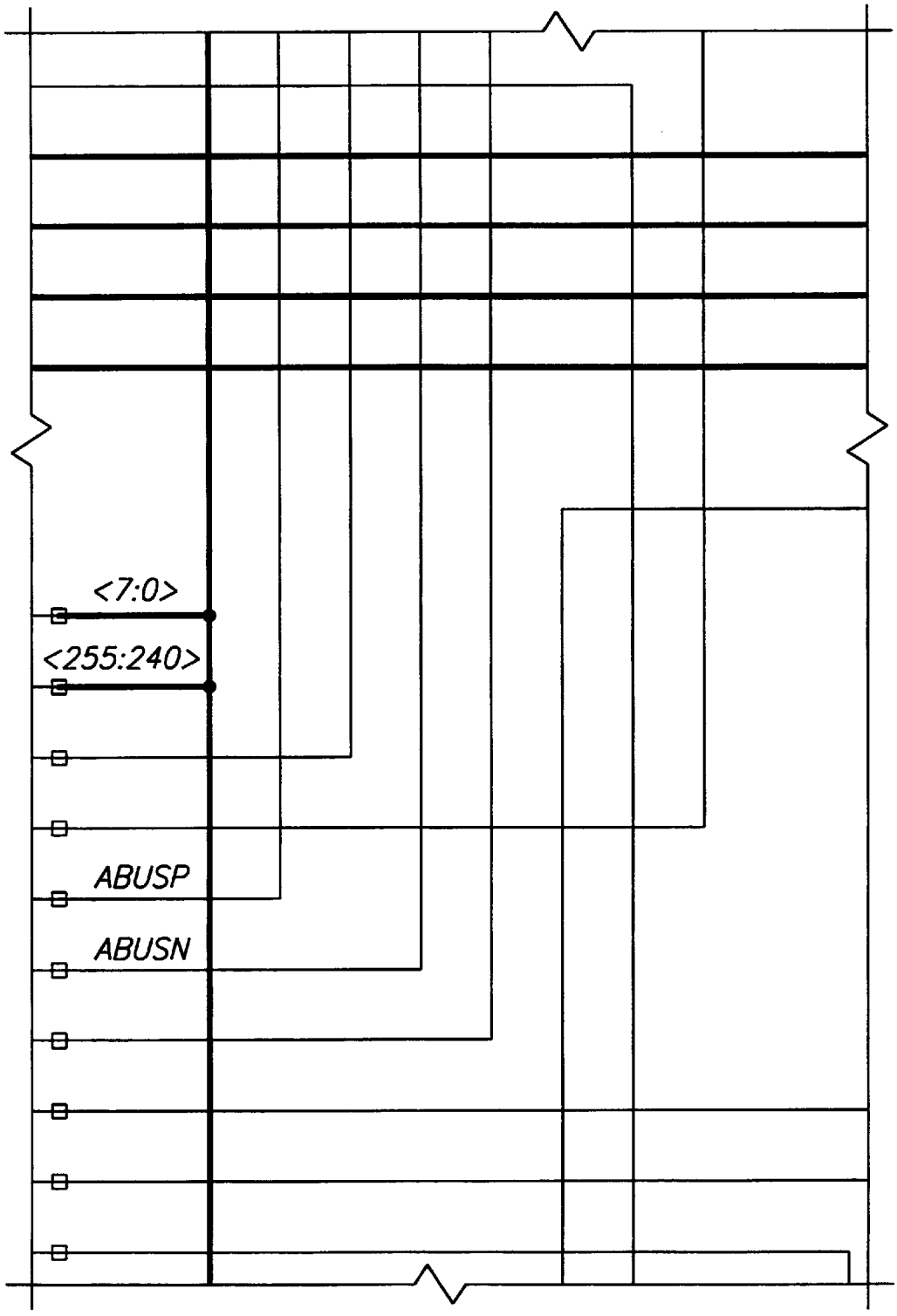


Fig 6BF

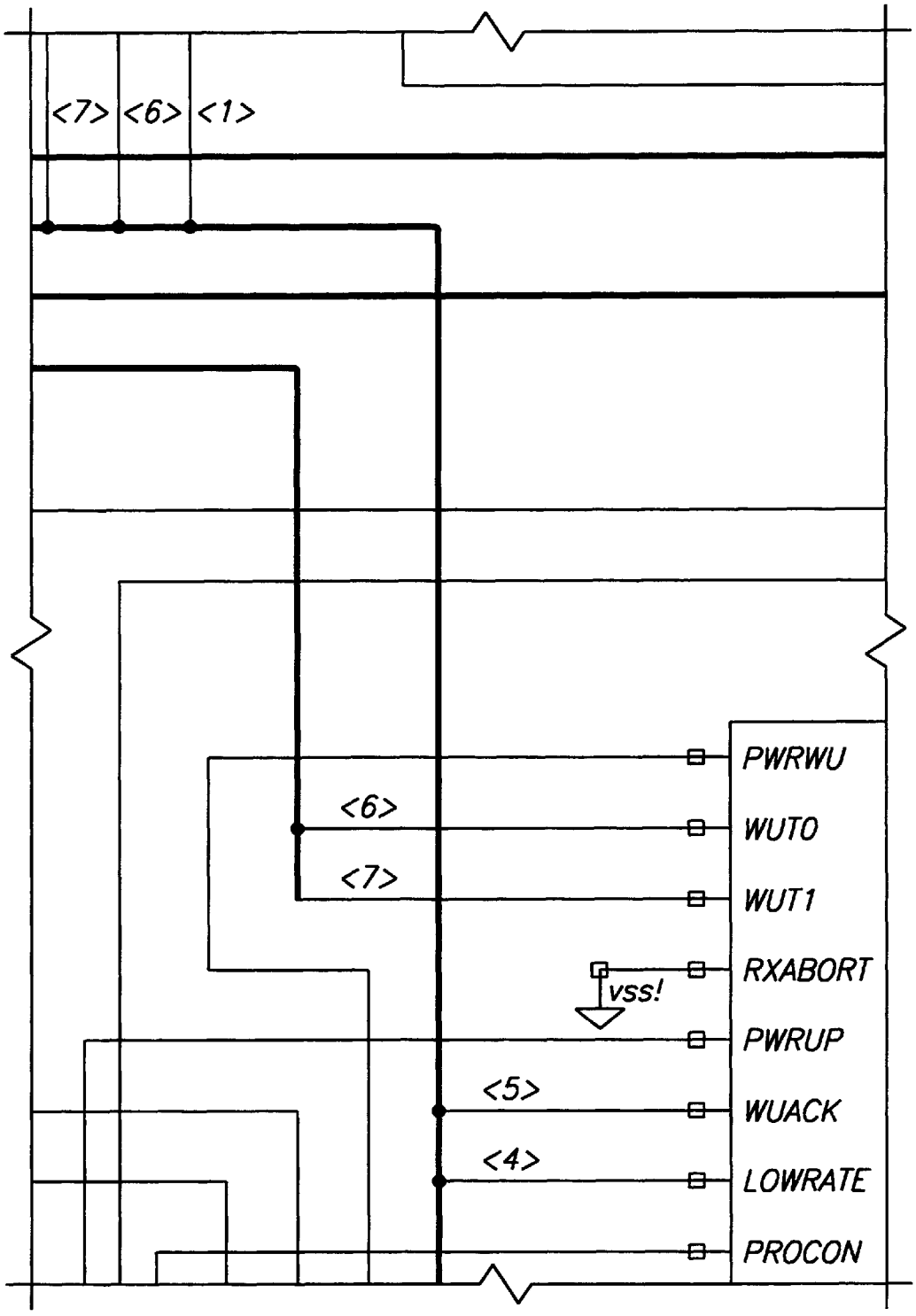

<7>
<6>
<1>
PWRWU
<6>
WUT0
<7>
WUT1
RXABORT
vss!
PWRUP
<5>
WUACK
<4>
LOWRATE
PROCON

Fig 6B6

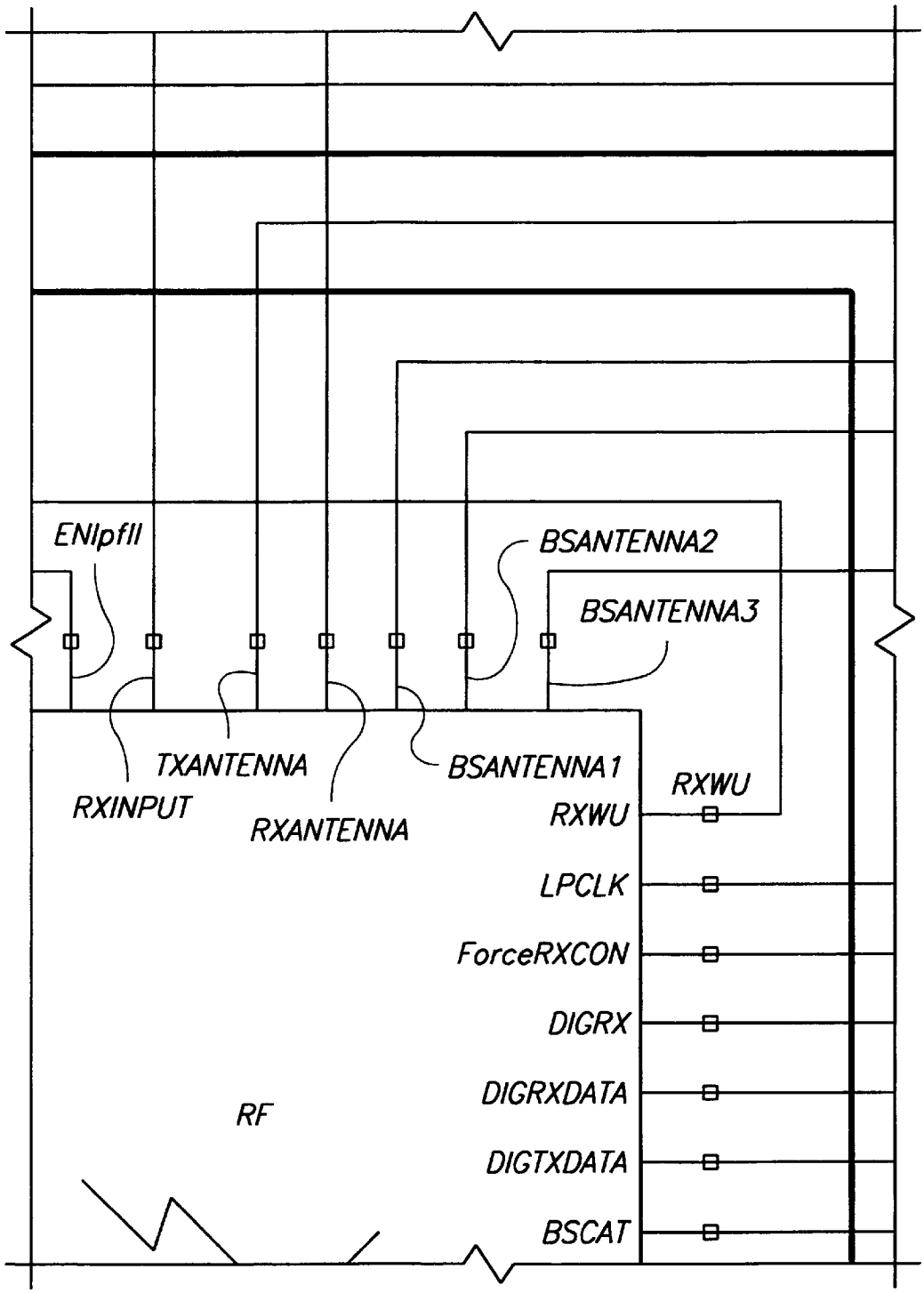

ENlpfll
BSANTENNA2
BSANTENNA3
TXANTENNA
RXINPUT
RXANTENNA
BSANTENNA1
RXWU
RXWU
LPCLK
ForceRXCON
DIGRX
DIGRXDATA
DIGTXDATA
BSCAT
RF

Fig 6BH

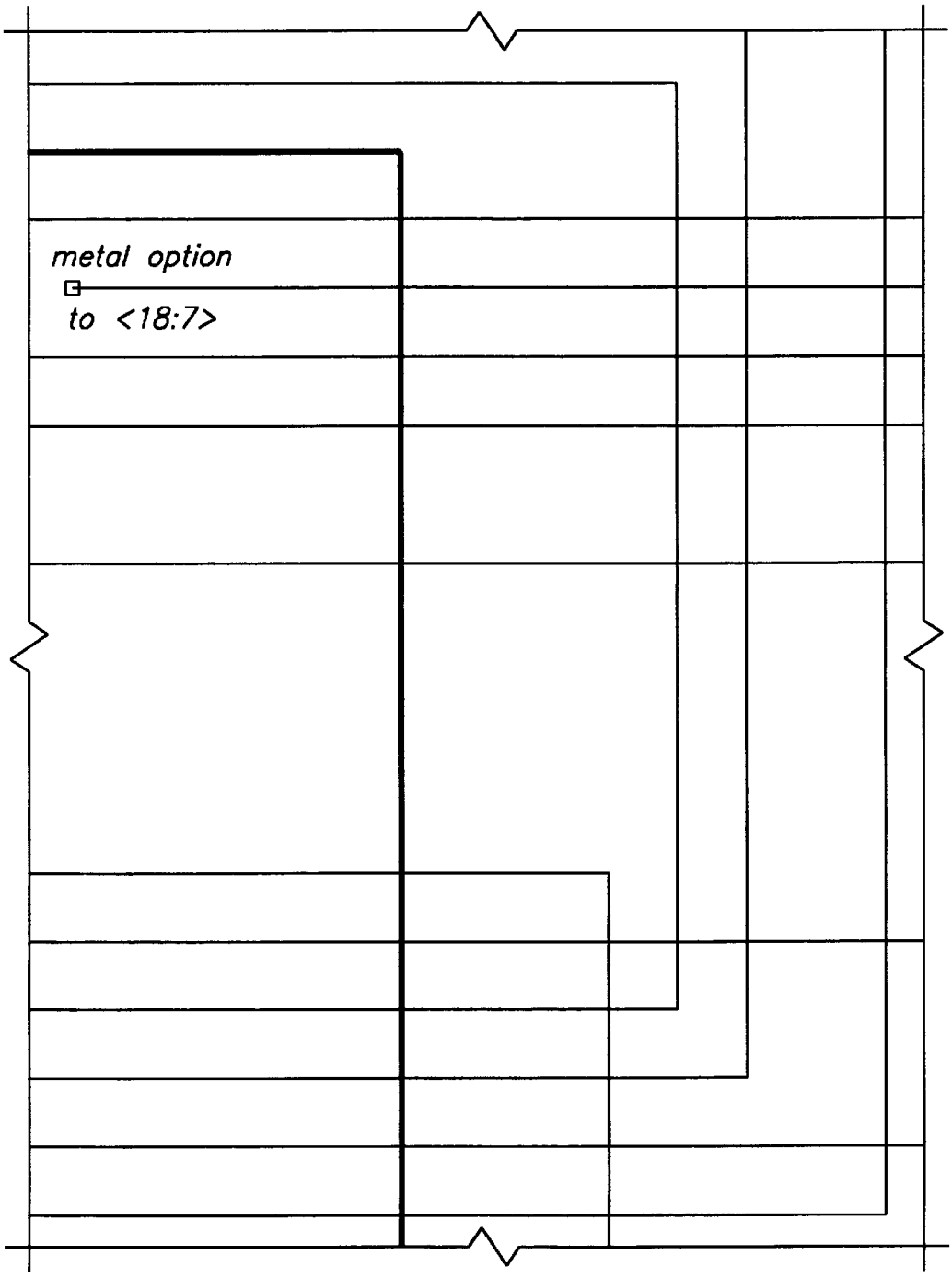


Fig 6BI

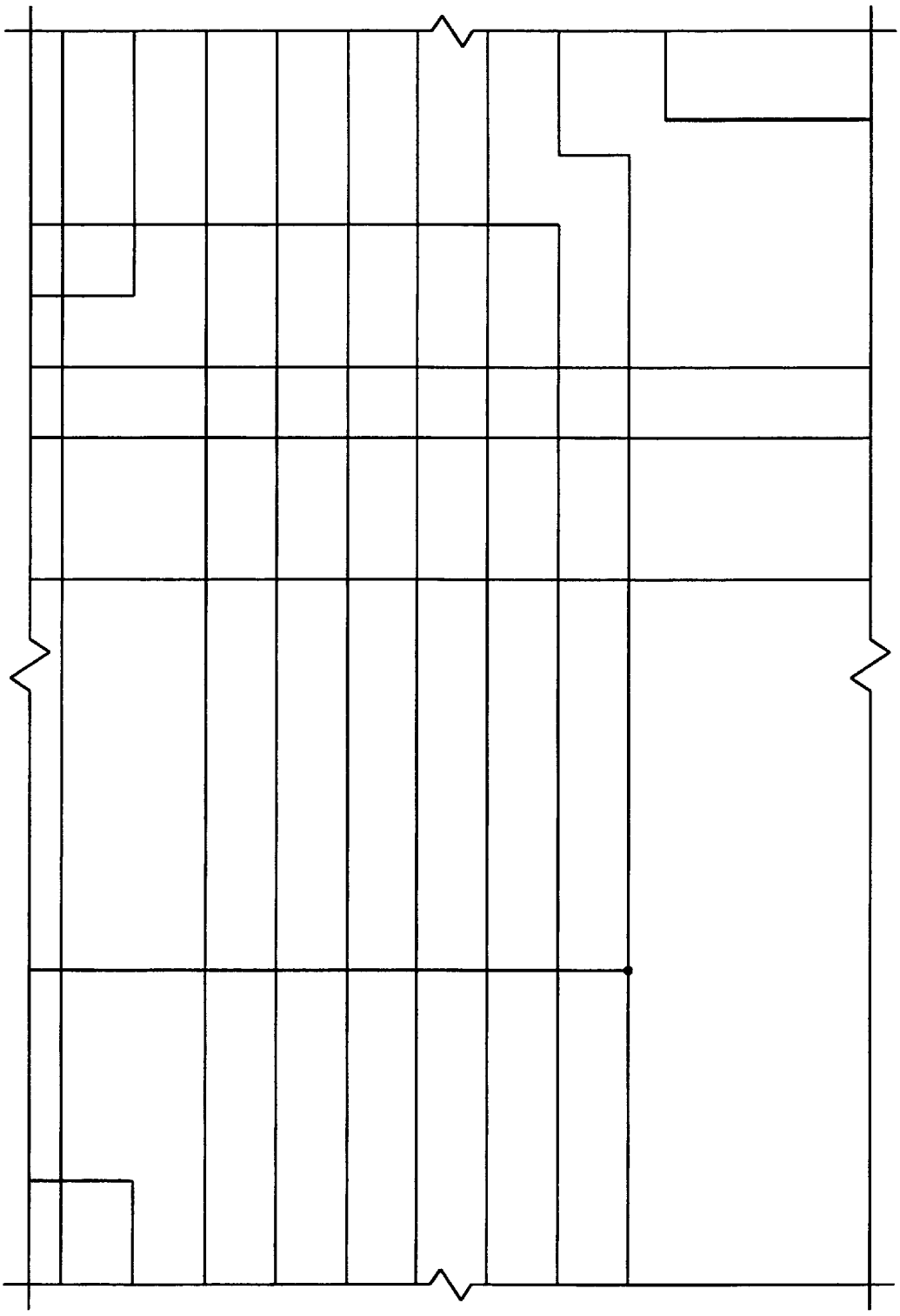


Fig 6Bd

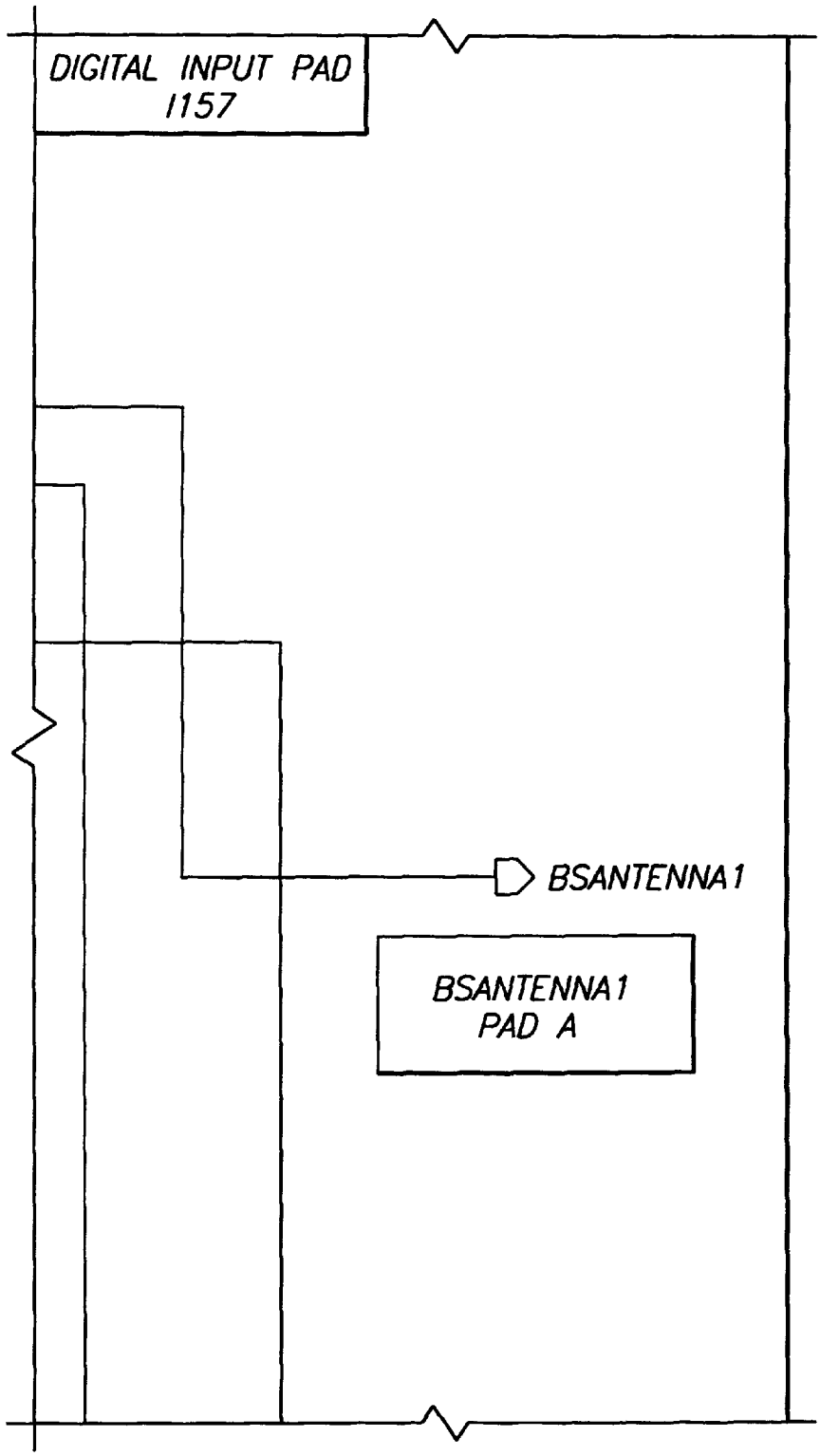


FIG 6BK

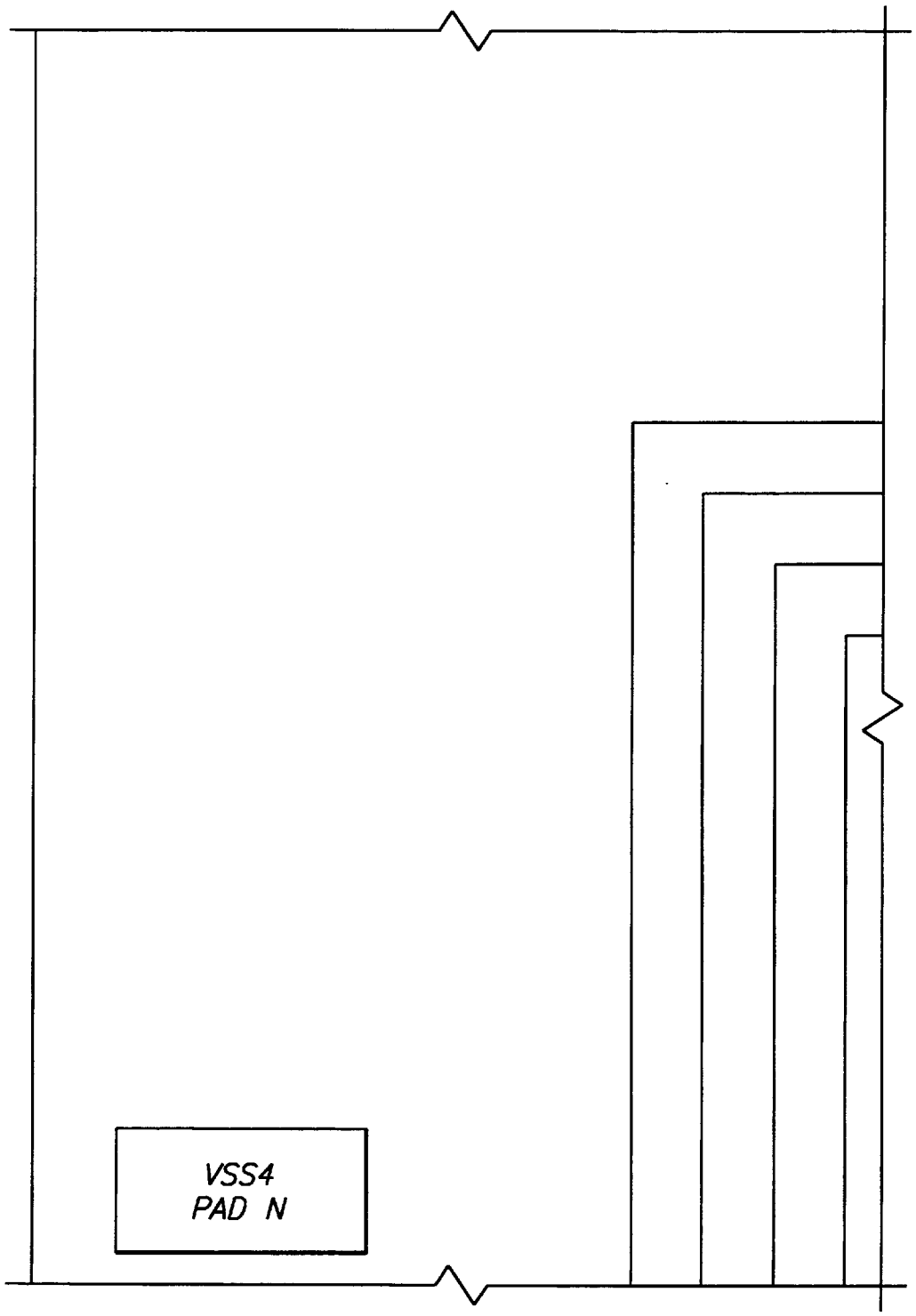
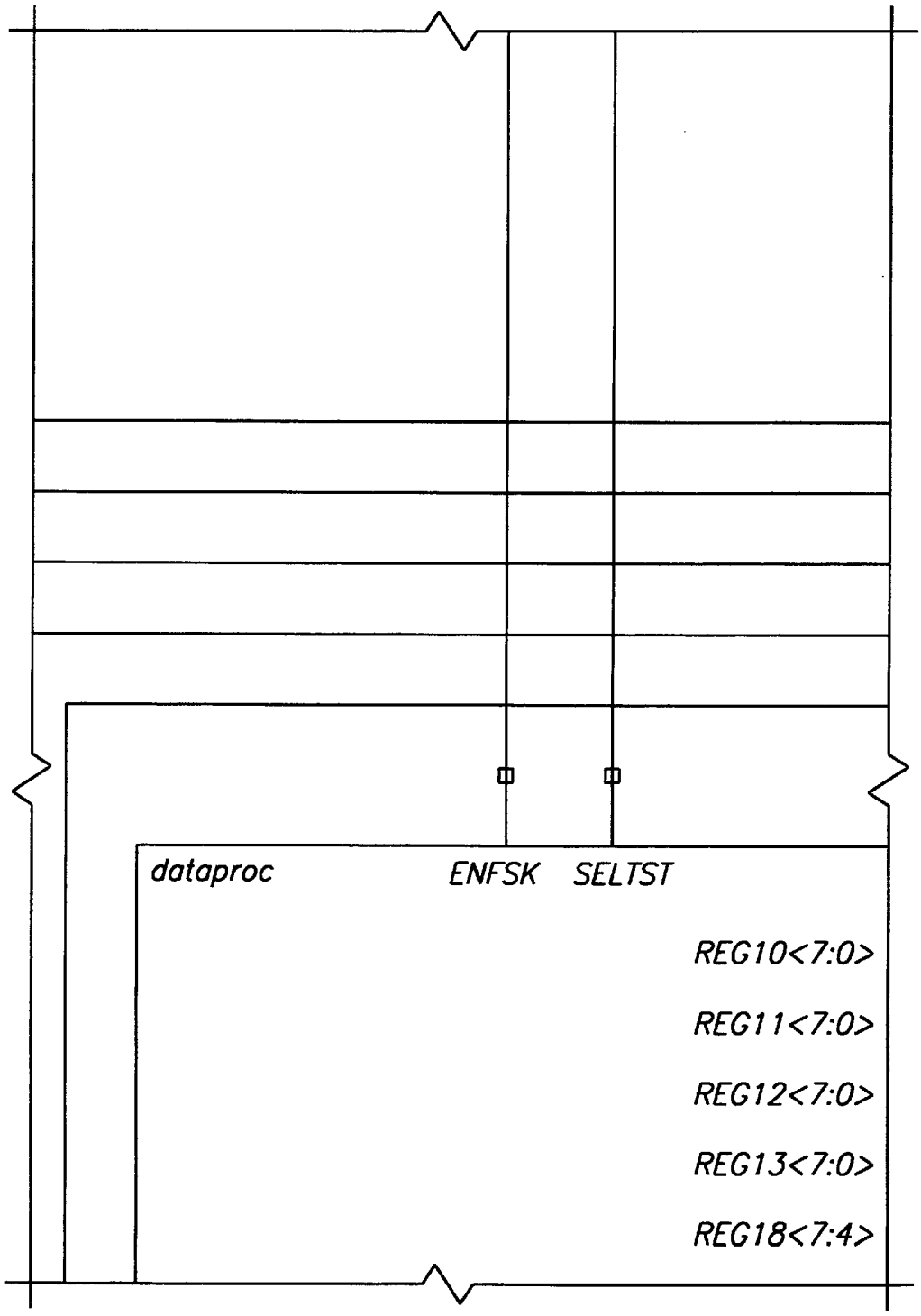


Fig 6CA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ENFSK
SELTST
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REG11<7:0>
REG12<7:0>
REG13<7:0>
REG18<7:4>

Fig 6CB

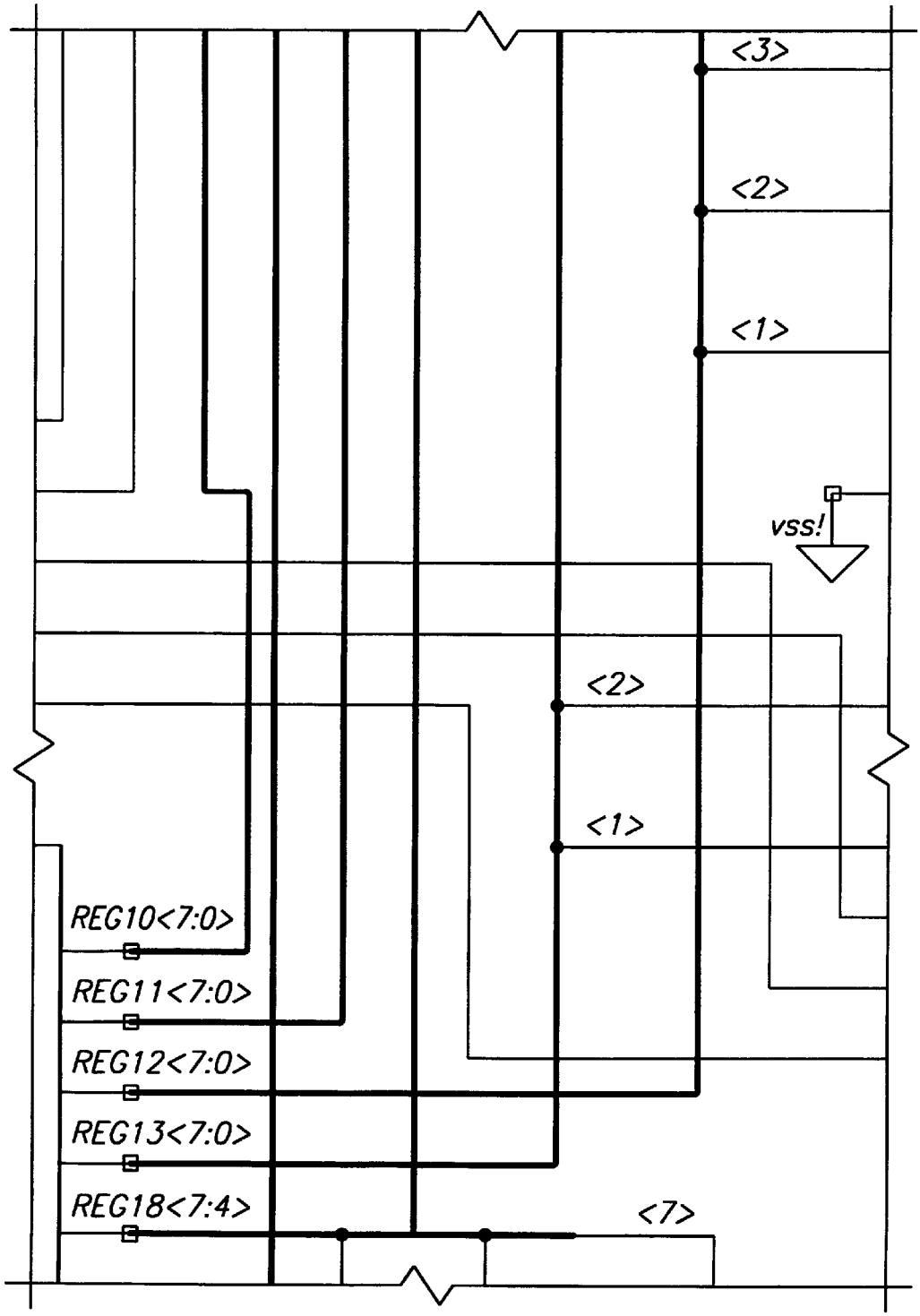


Fig 6CC

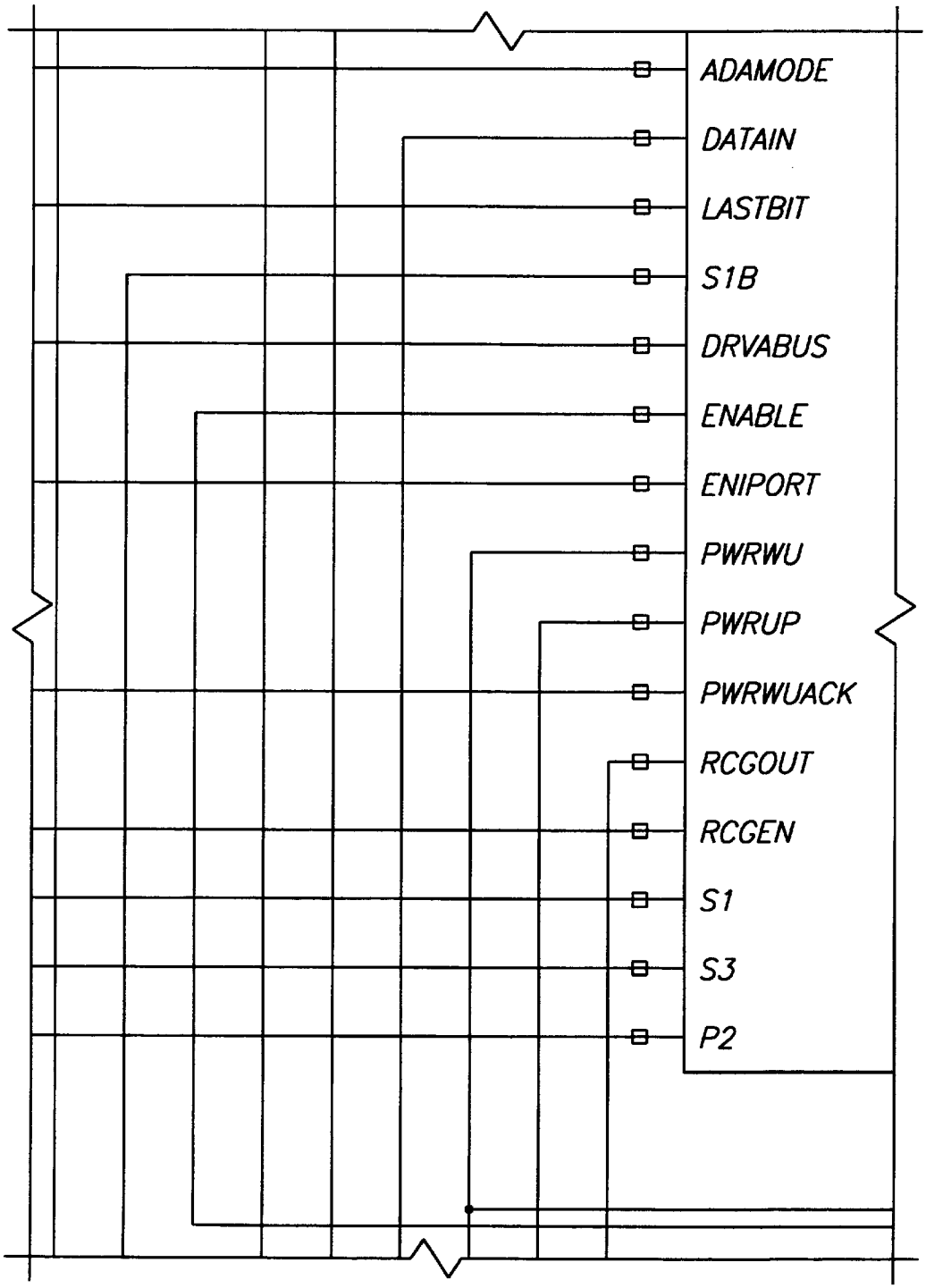

ADAMODE
DATAIN
LASTBIT
S1B
DRVABUS
ENABLE
ENIPORT
PWRWU
PWRUP
PWRWUACK
RCGOUT
RCGEN
S1
S3
P2

Fig 6CD

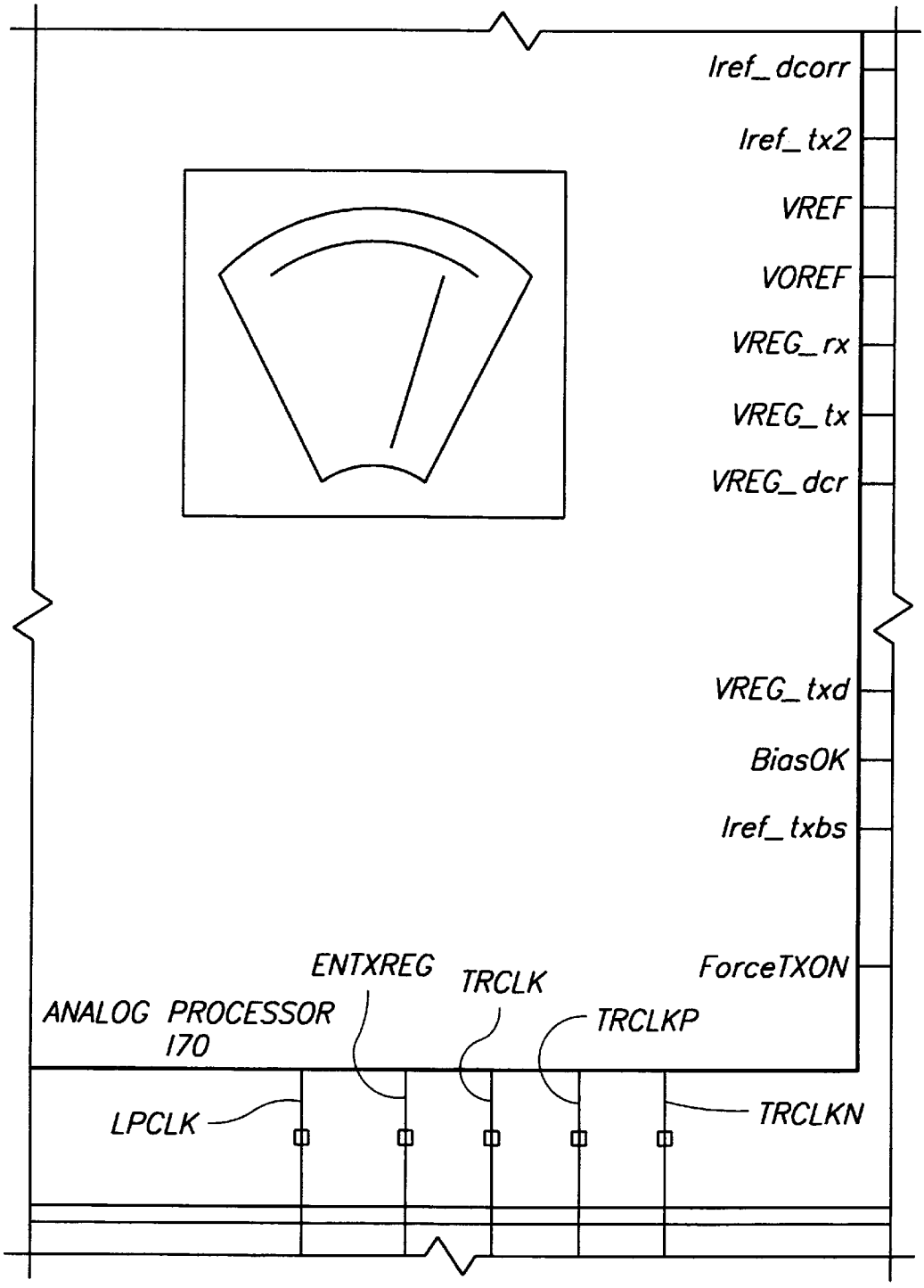

Iref_dcorr
Iref_tx2
VREF
VOREF
VREG_rx
VREG_tx
VREG_dcr
VREG_txd
BiasOK
Iref_txbs
ForceTXON
ENTXREG
TRCLK
TRCLKP
ANALOG PROCESSOR
170
LPCLK
TRCLKN

Fig 6CE

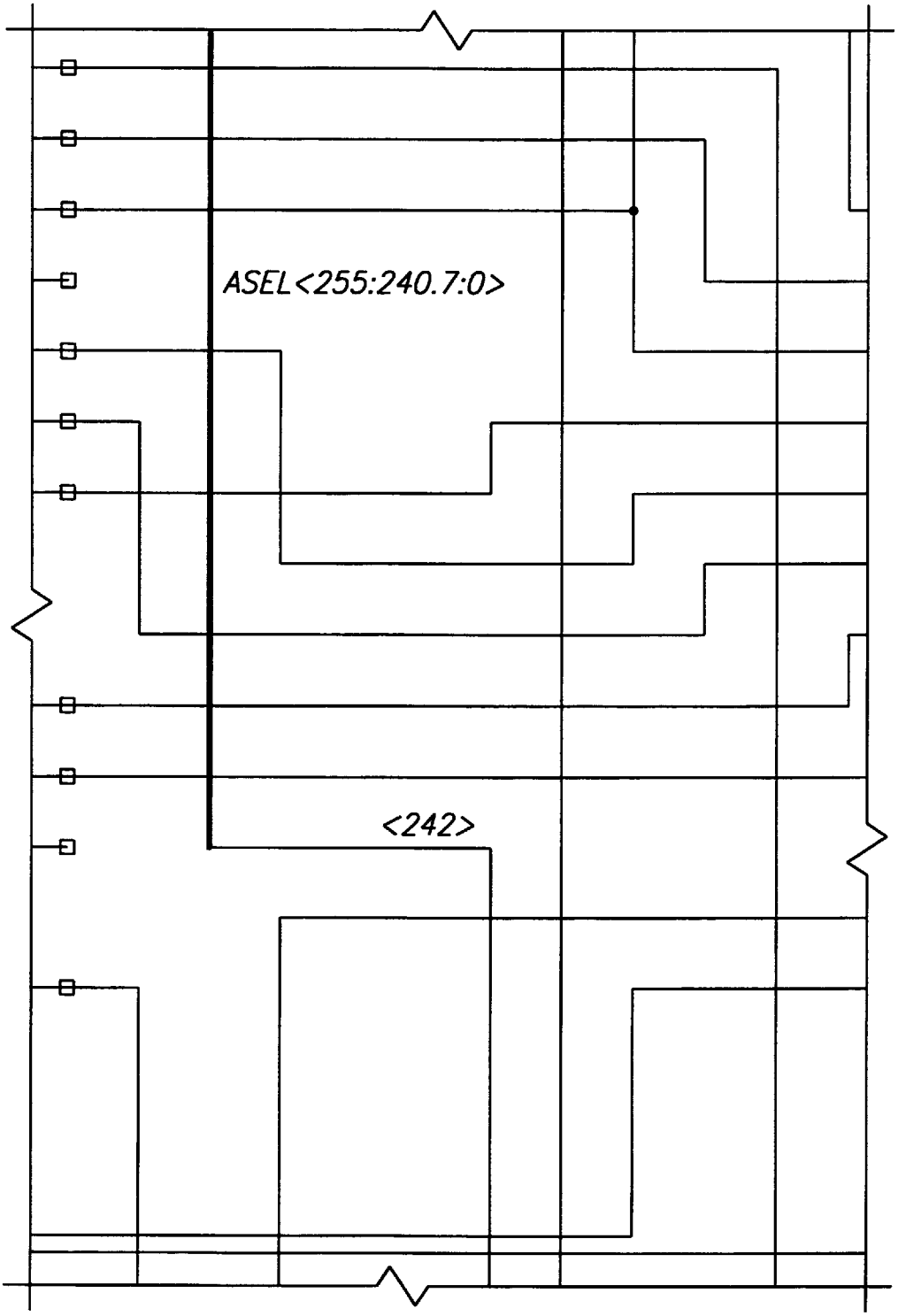


Fig 6CF

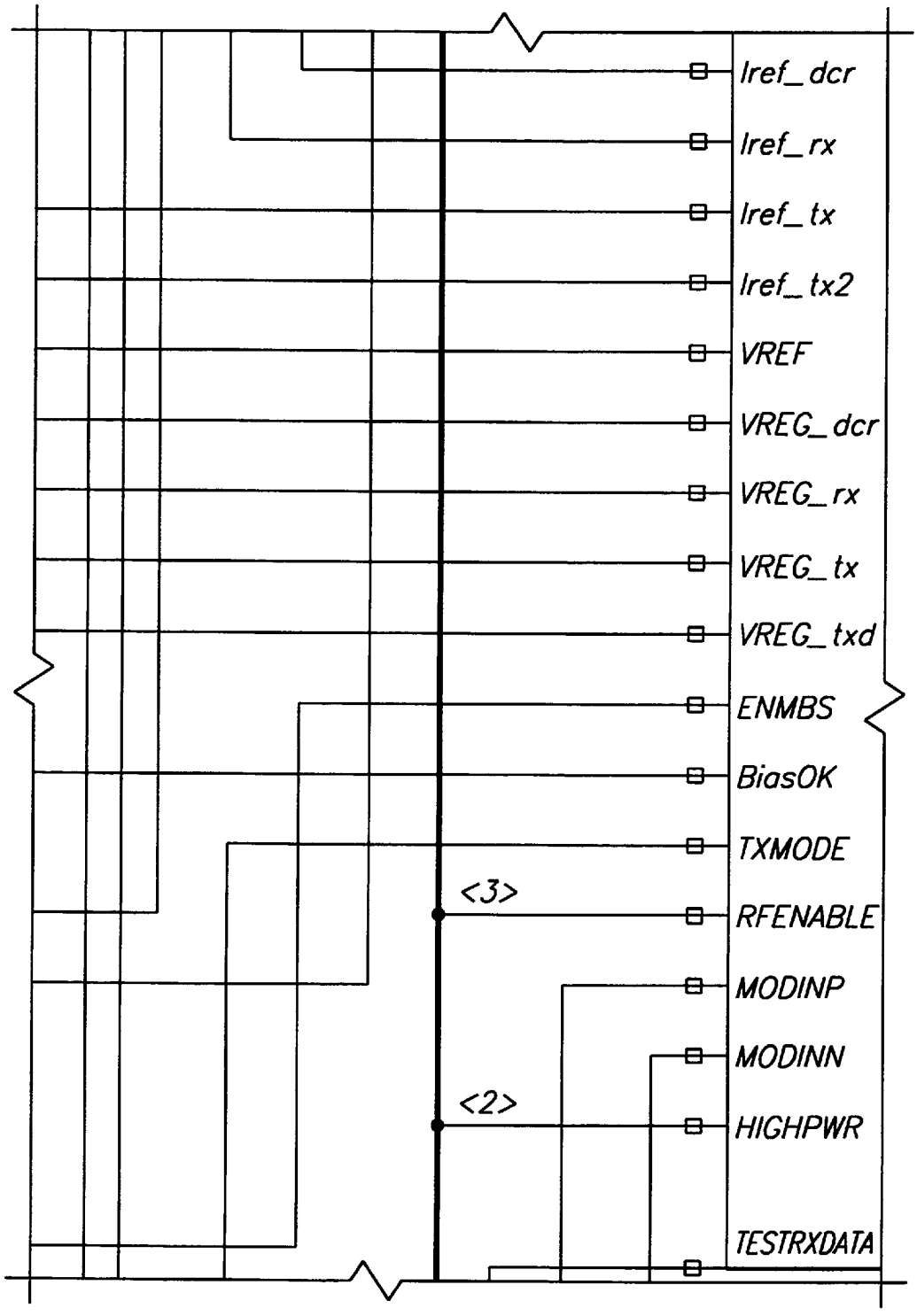

Iref_dcr
Iref_rx
Iref_tx
Iref_tx2
VREF
VREG_dcr
VREG_rx
VREG_tx
VREG_txd
ENMBS
BiasOK
TXMODE
<3>
RFENABLE
MODINP
MODINN
<2>
HIGHPWR
TESTRXDATA

Fig 6C6

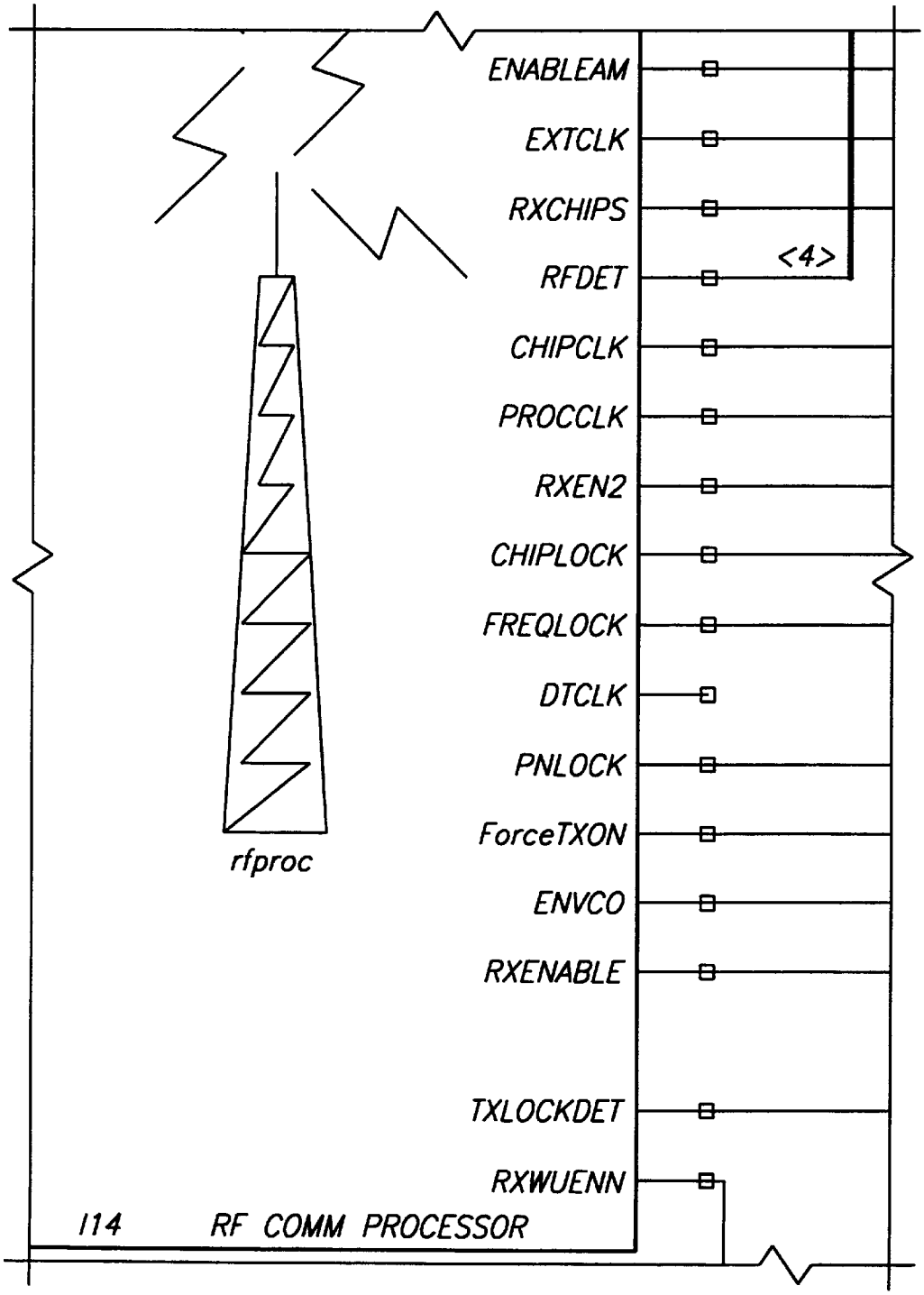

ENABLEAM
EXTCLK
RXCHIPS
<4>
RFDET
CHIPCLK
PROCCLK
RXEN2
CHIPLOCK
FREQLOCK
DTCLK
PNLOCK
ForceTXON
ENVCO
RXENABLE
TXLOCKDET
RXWUENN
rfproc
114 RF COMM PROCESSOR

Fig 6CH

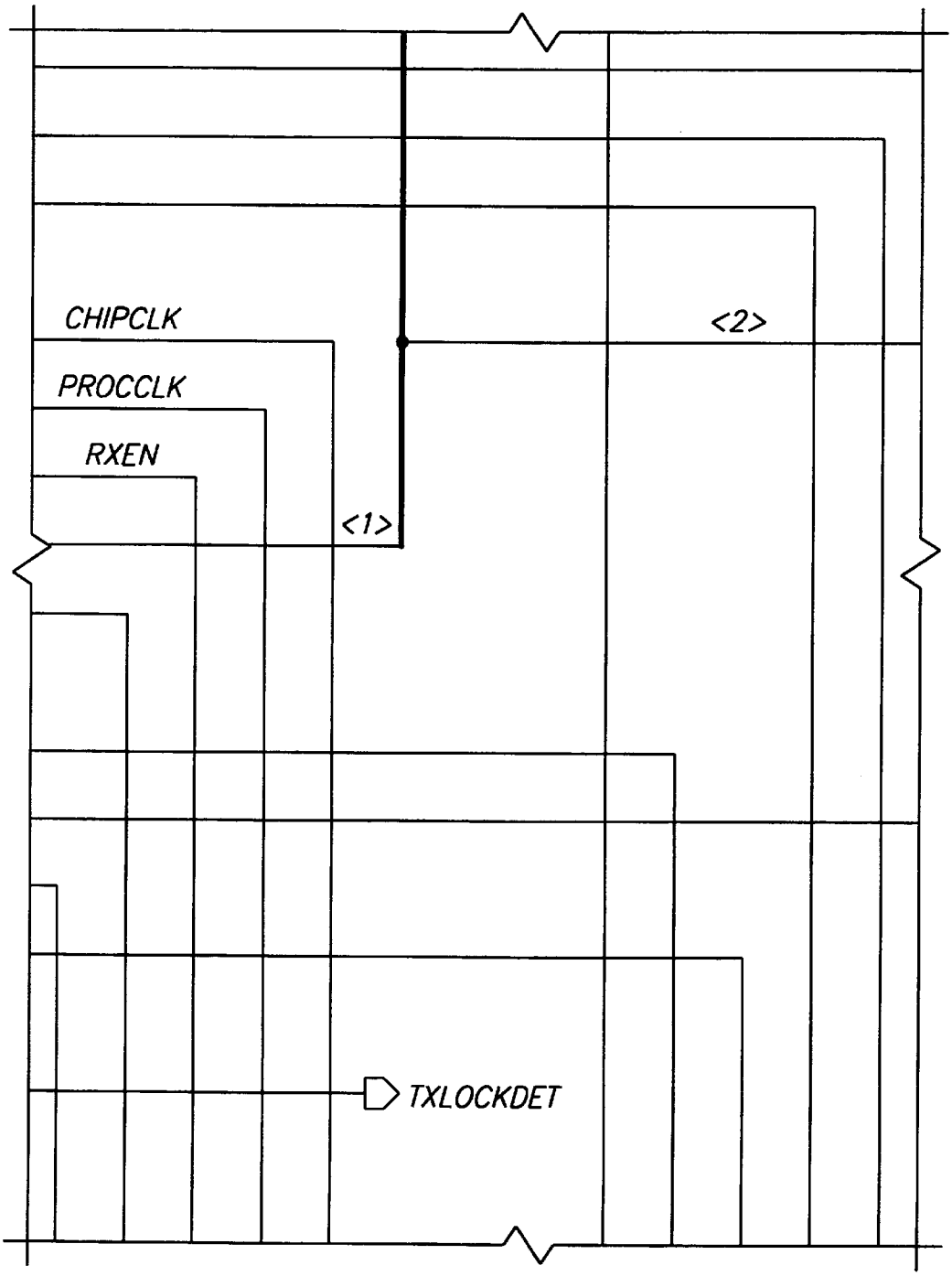


Fig 6C II

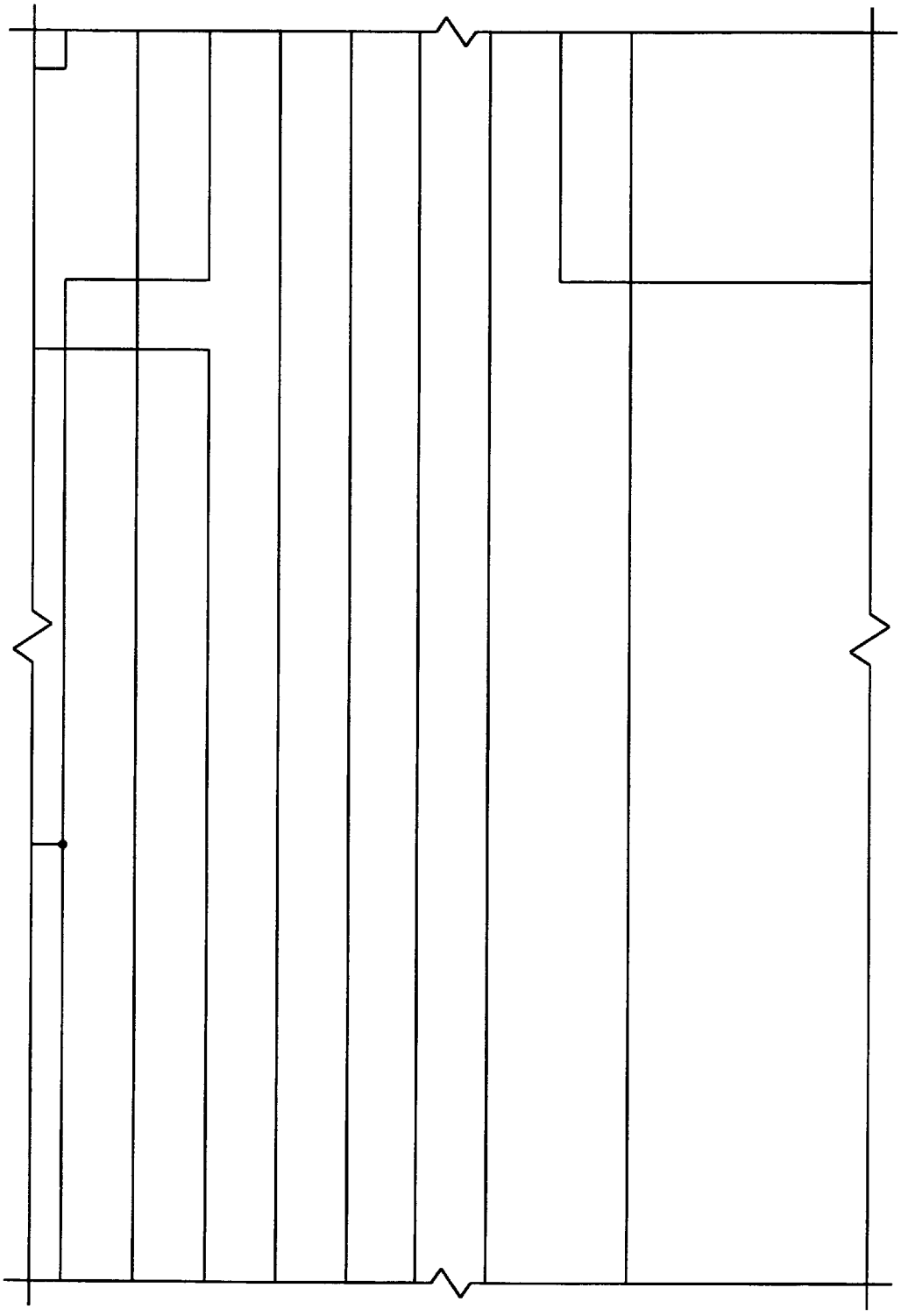


Fig 6Cd

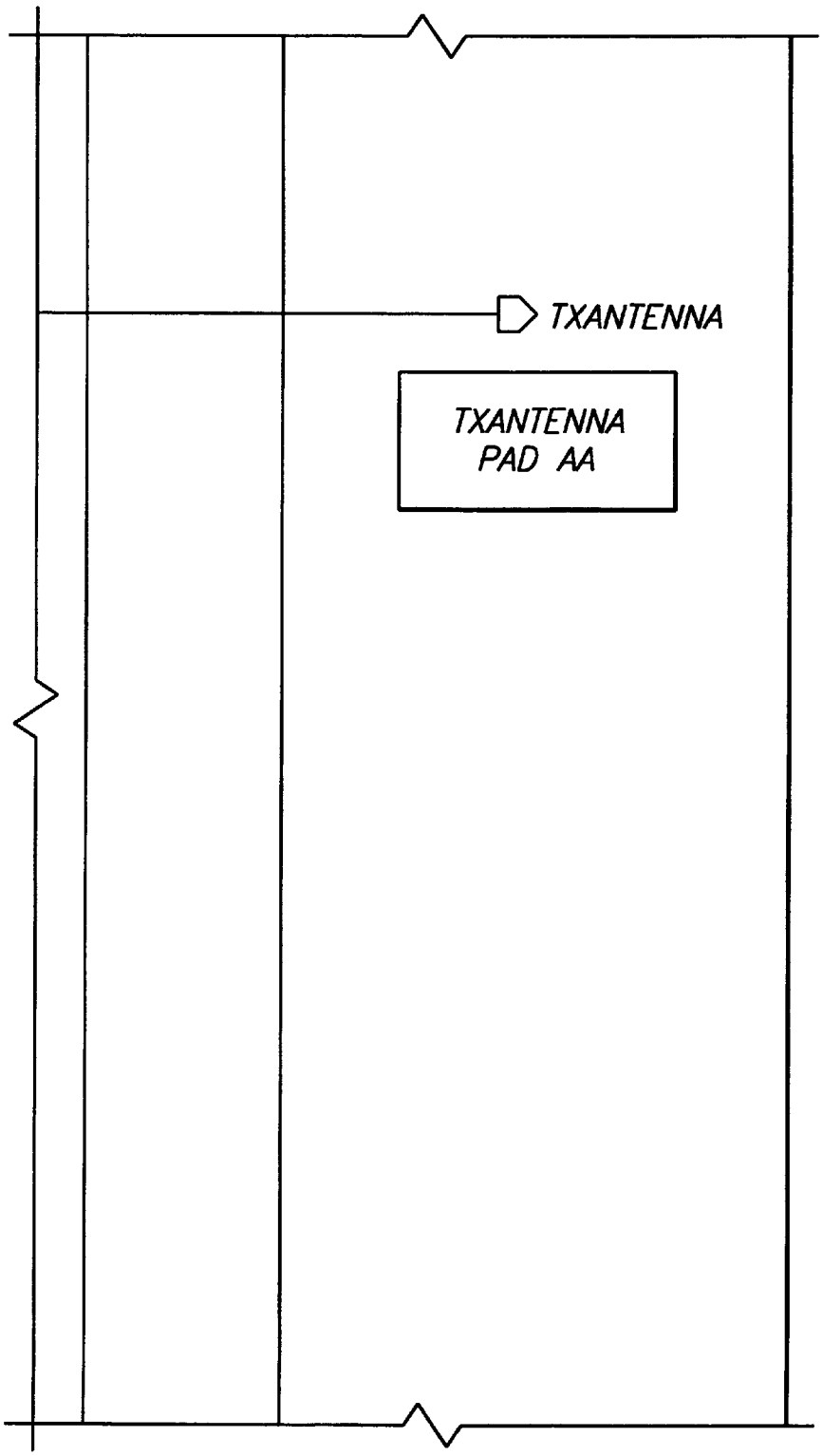


Fig 6CK

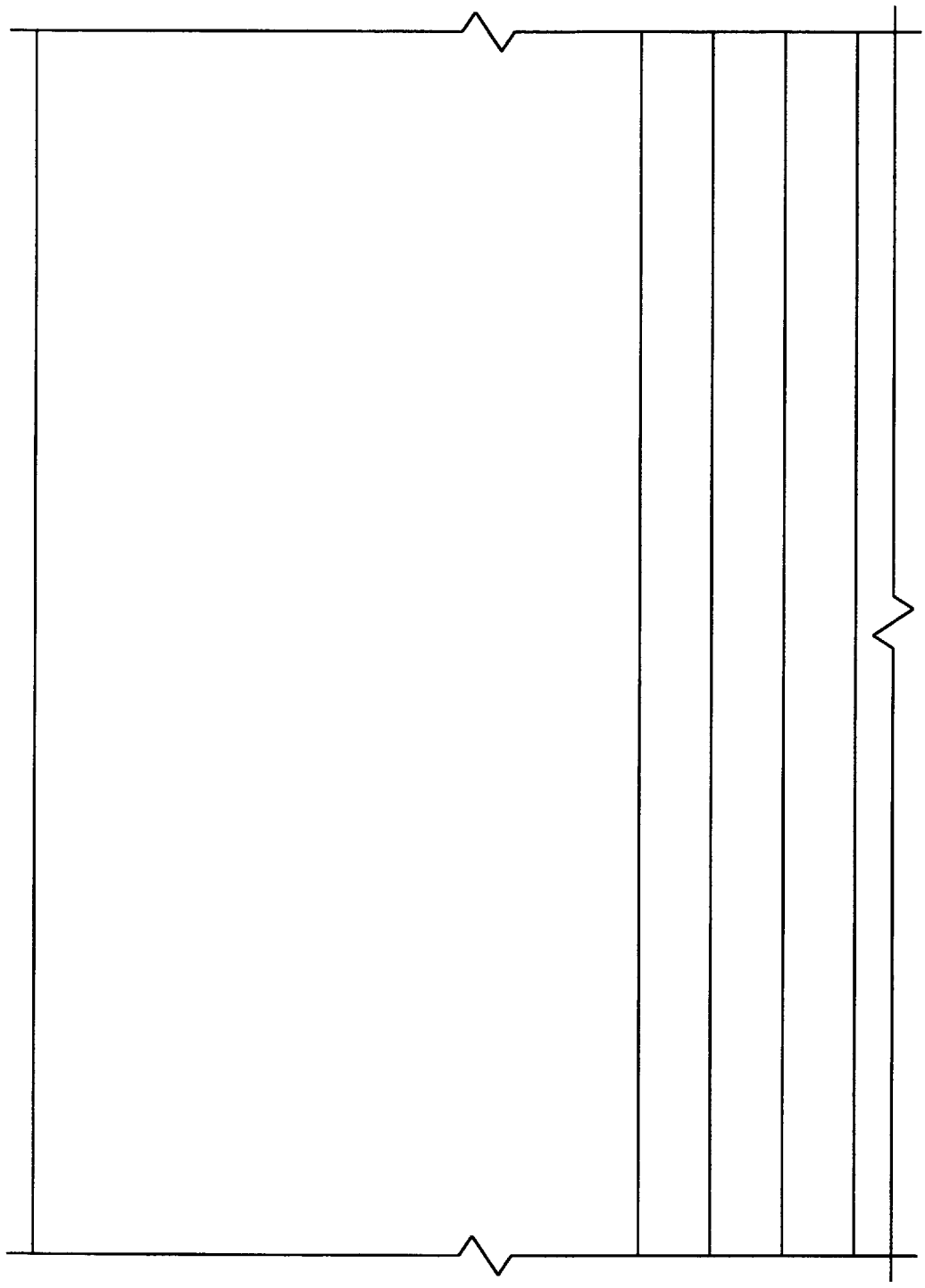


Fig 60A

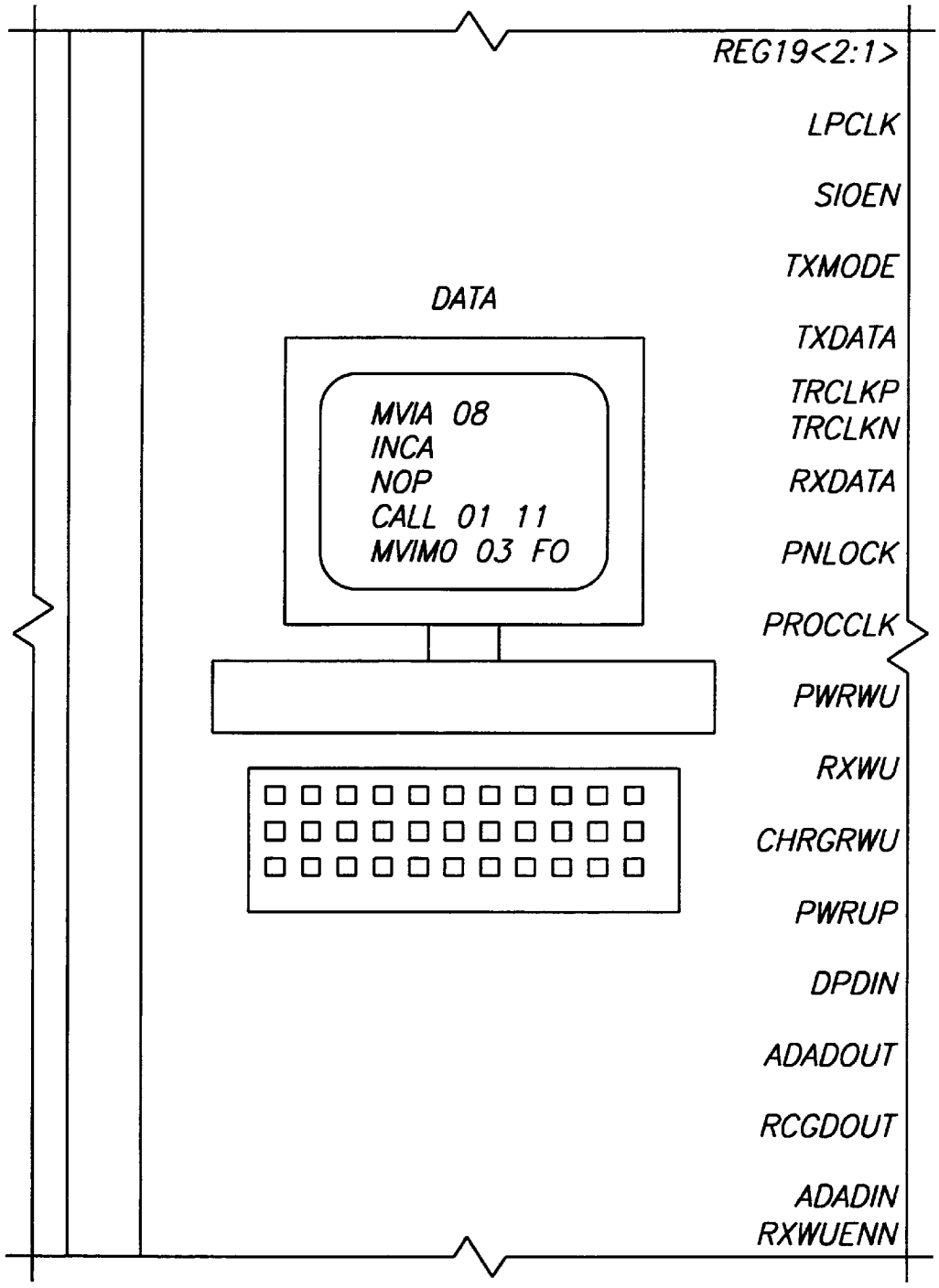

REG19<2:1>
LPCLK
SIOEN
TXMODE
DATA
TXDATA
TRCLKP
TRCLKN
MVIA 08
INCA
NOP
CALL 01 11
MVIM0 03 F0
RXDATA
PNLOCK
PROCCLK
PWRWU
RXWU
CHRGRWU
PWRUP
DPDIN
ADADOUT
RCGDOUT
ADADIN
RXWUENN

Fig 60B

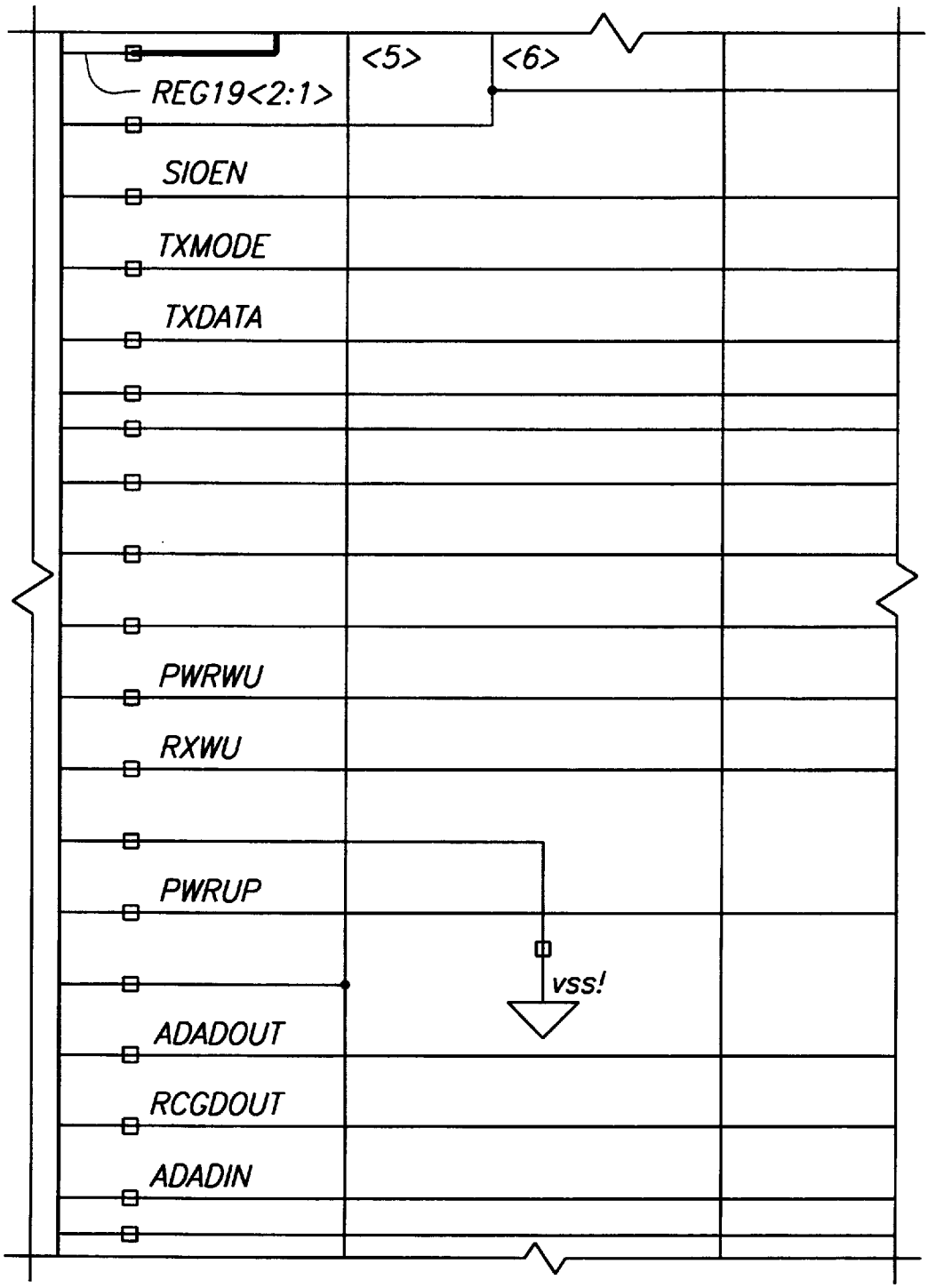

<5>
<6>
REG19<2:1>
SIOEN
TXMODE
TXDATA
PWRWU
RXWU
PWRUP
vss!
ADADOUT
RCGDOUT
ADADIN

Fig 60C

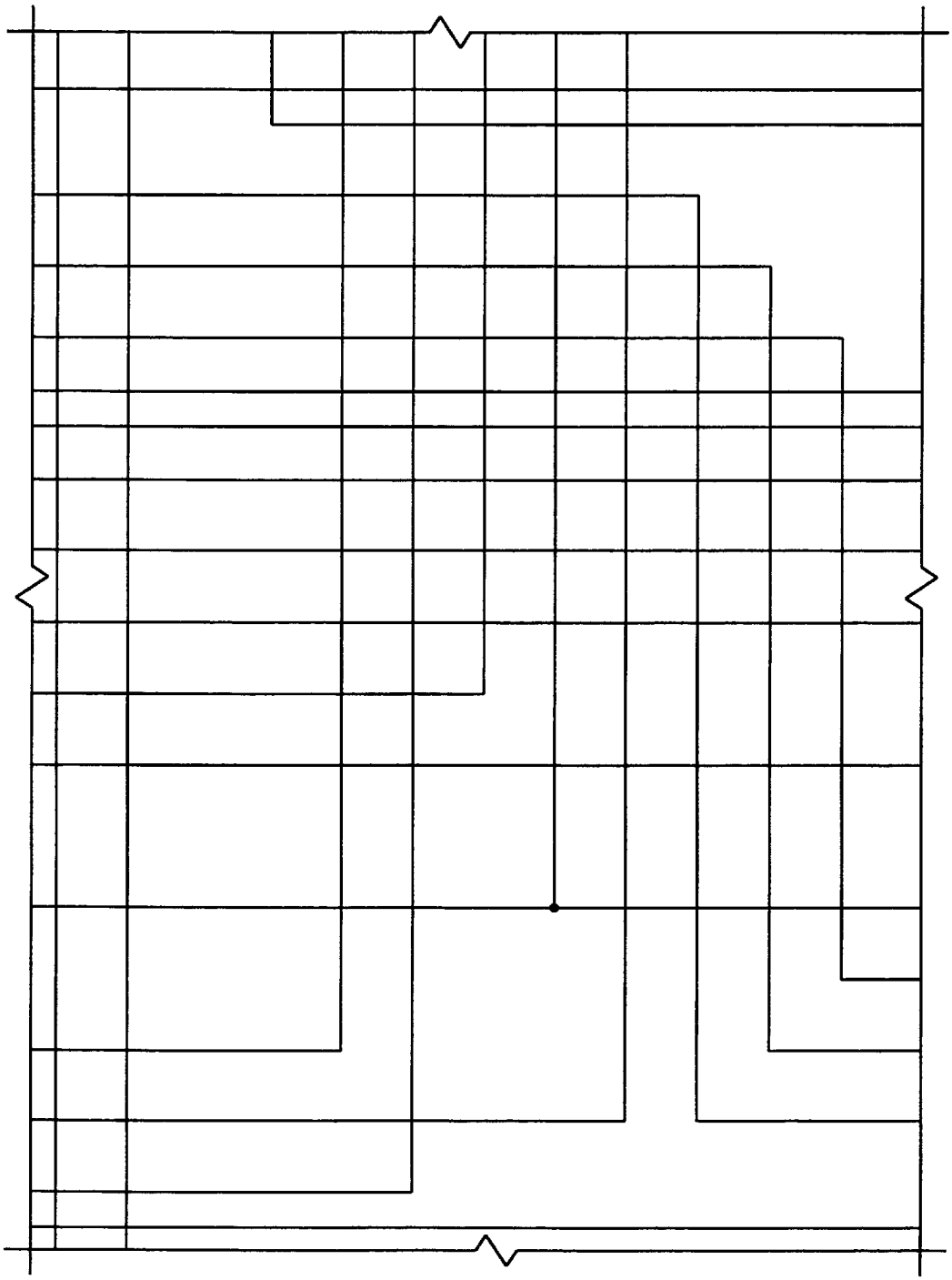


Fig 600

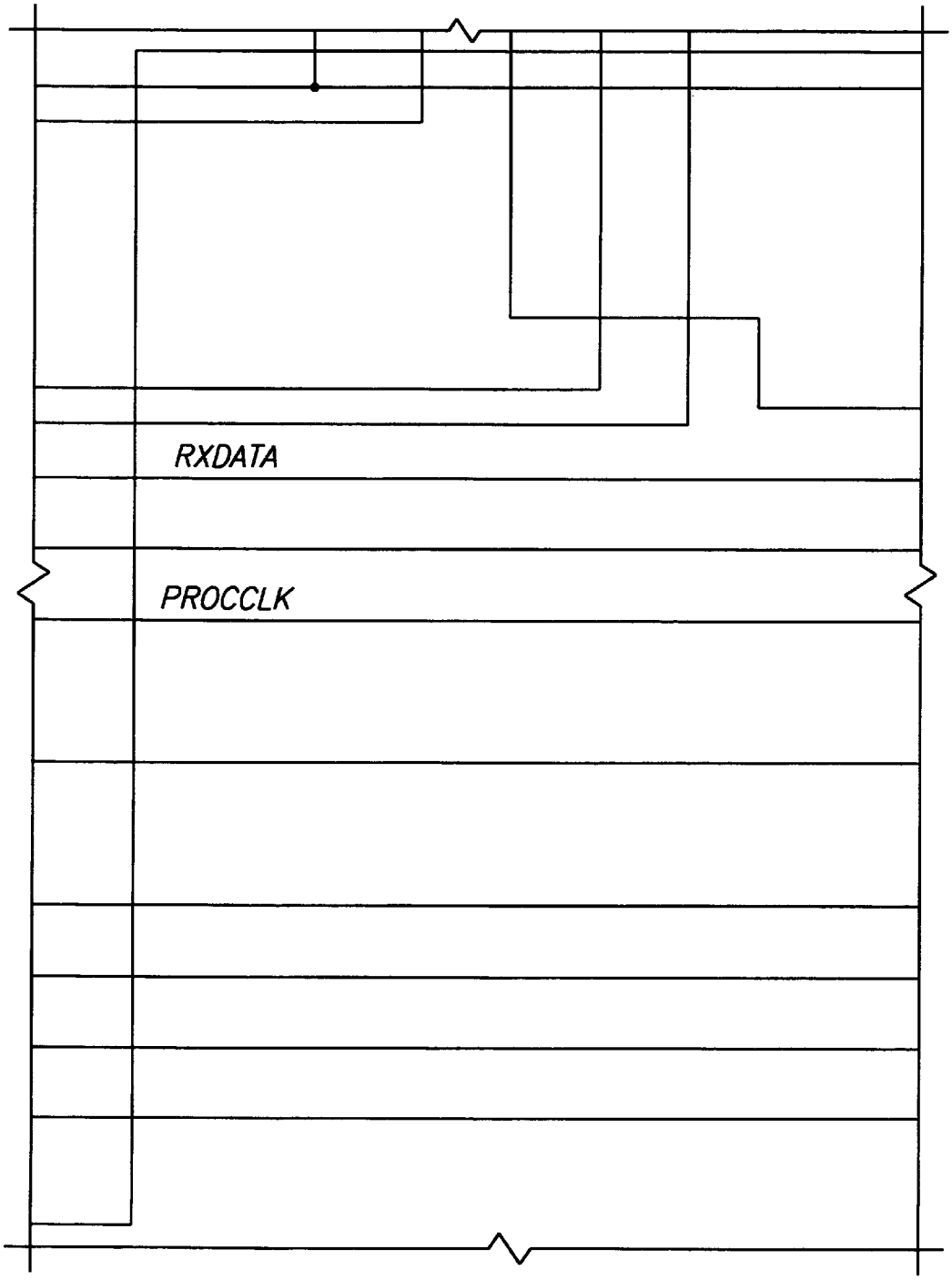


Fig 6DE

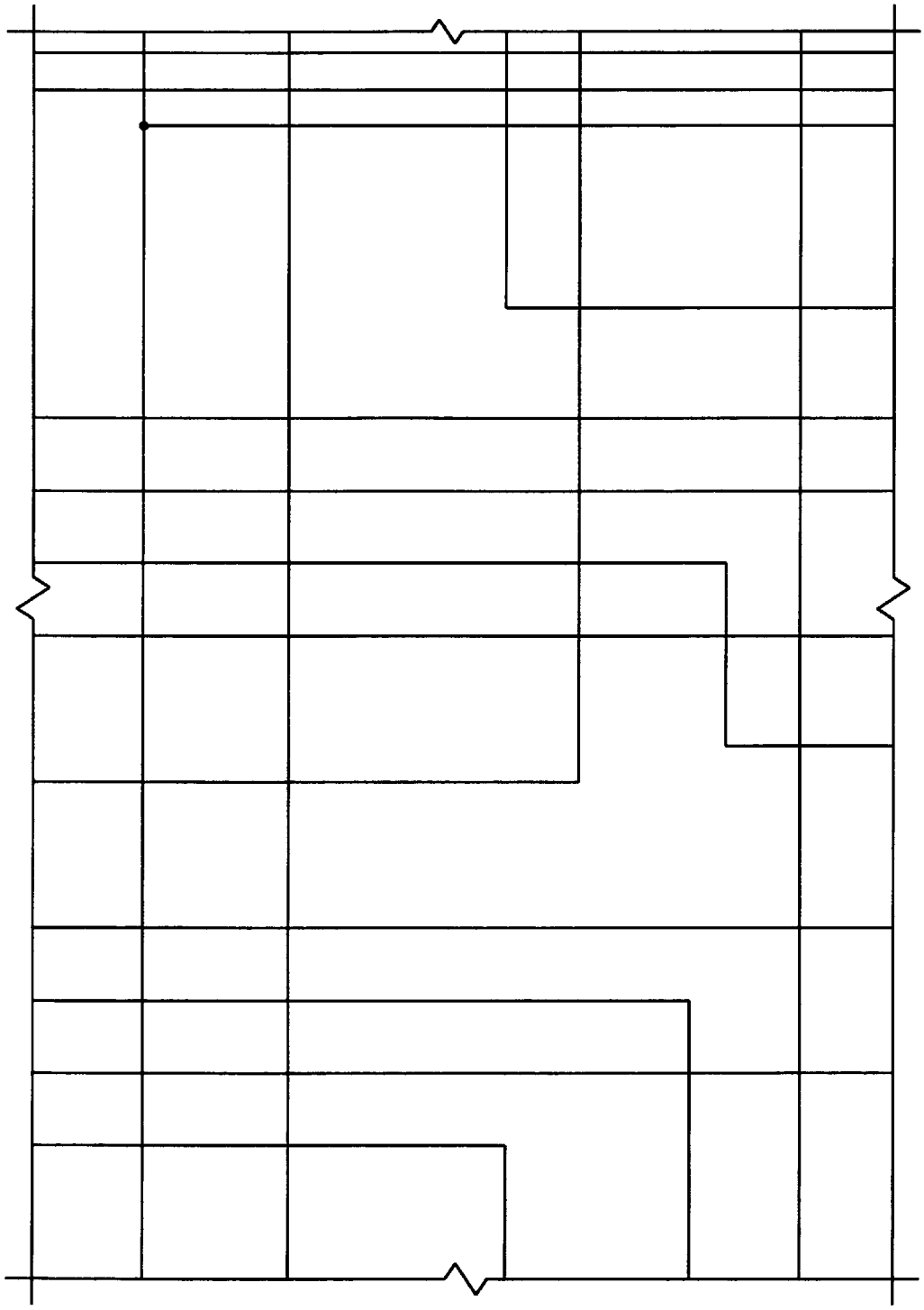


Fig 60F

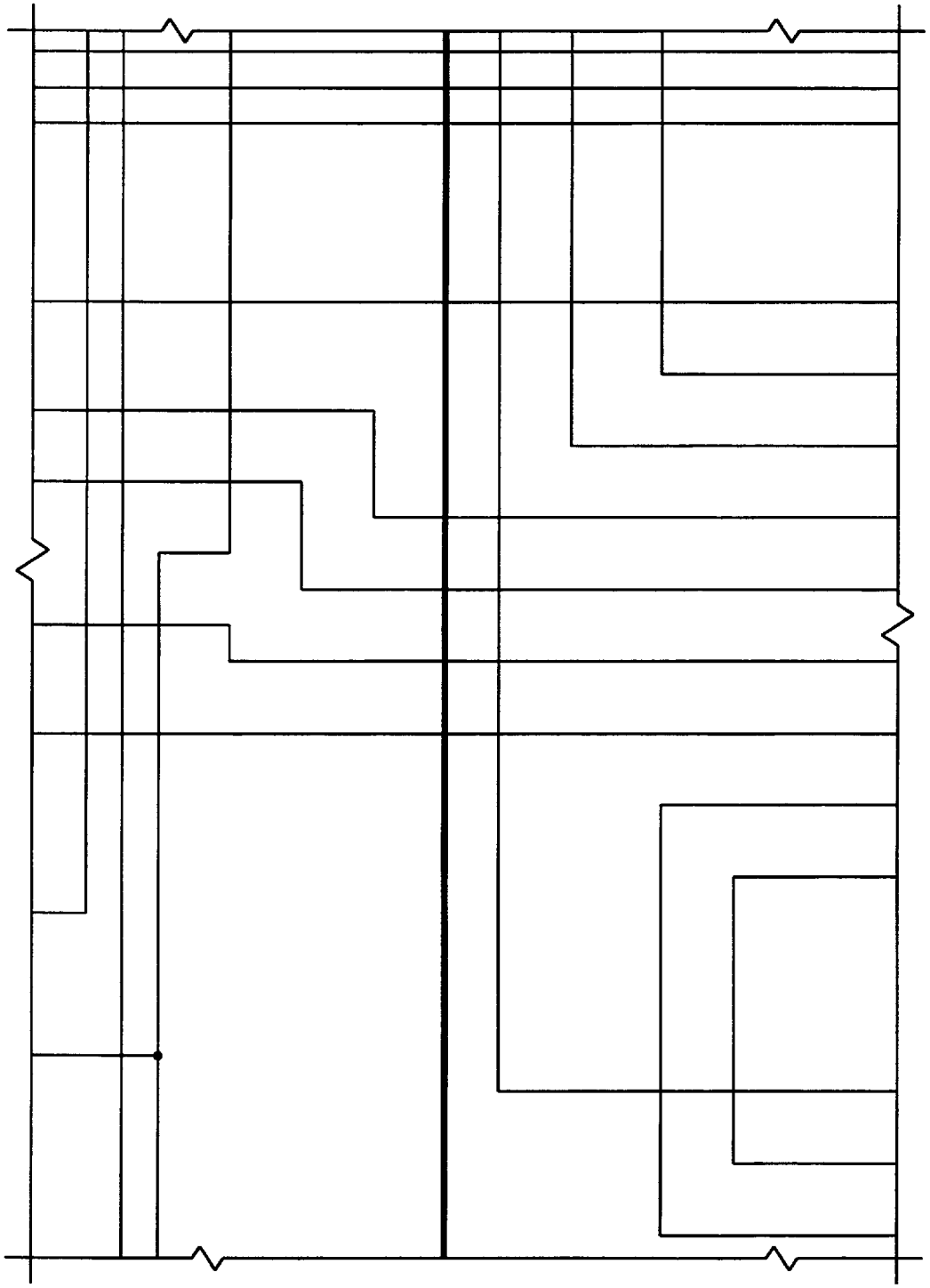


Fig 606

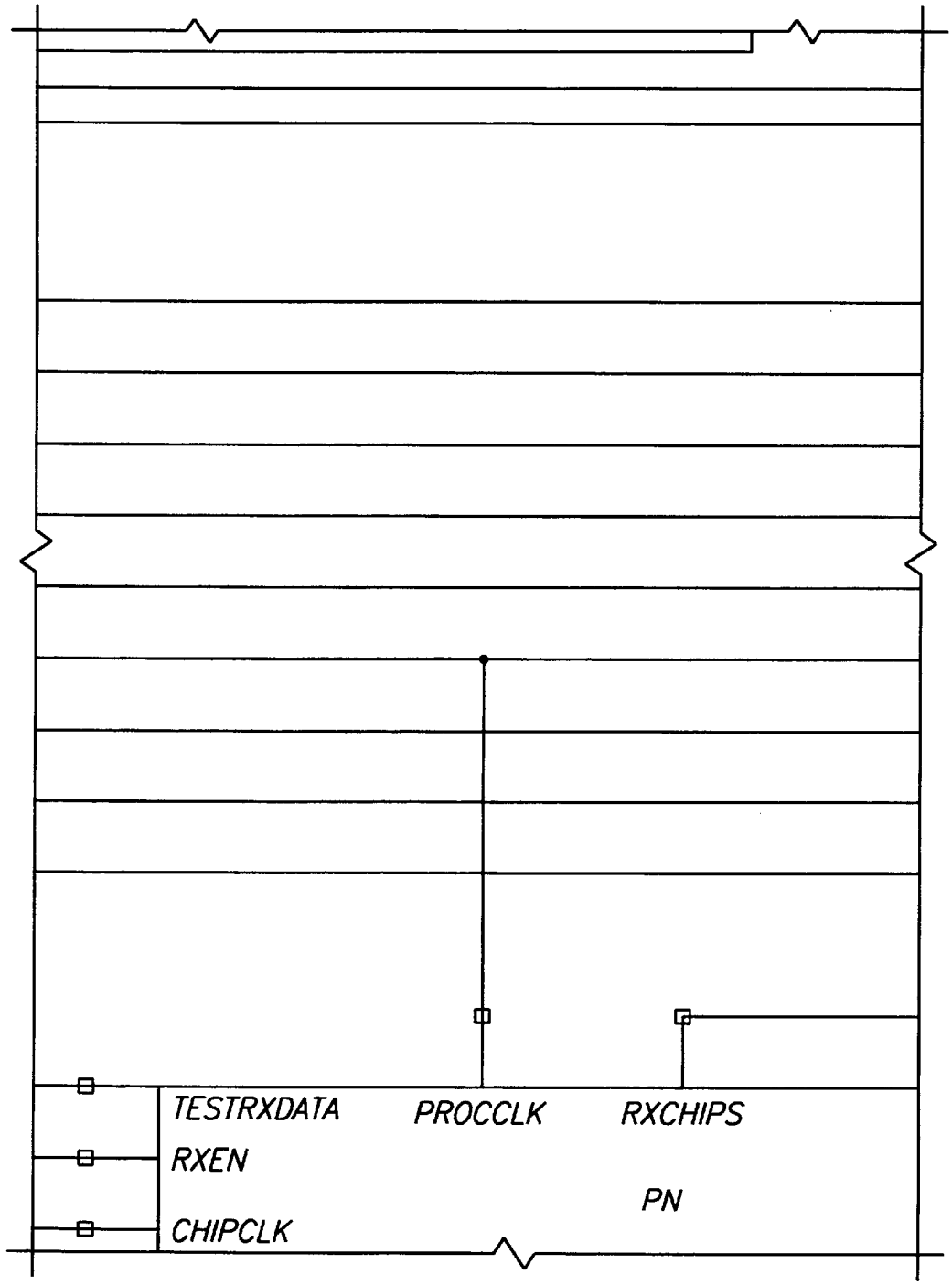


Fig 60H

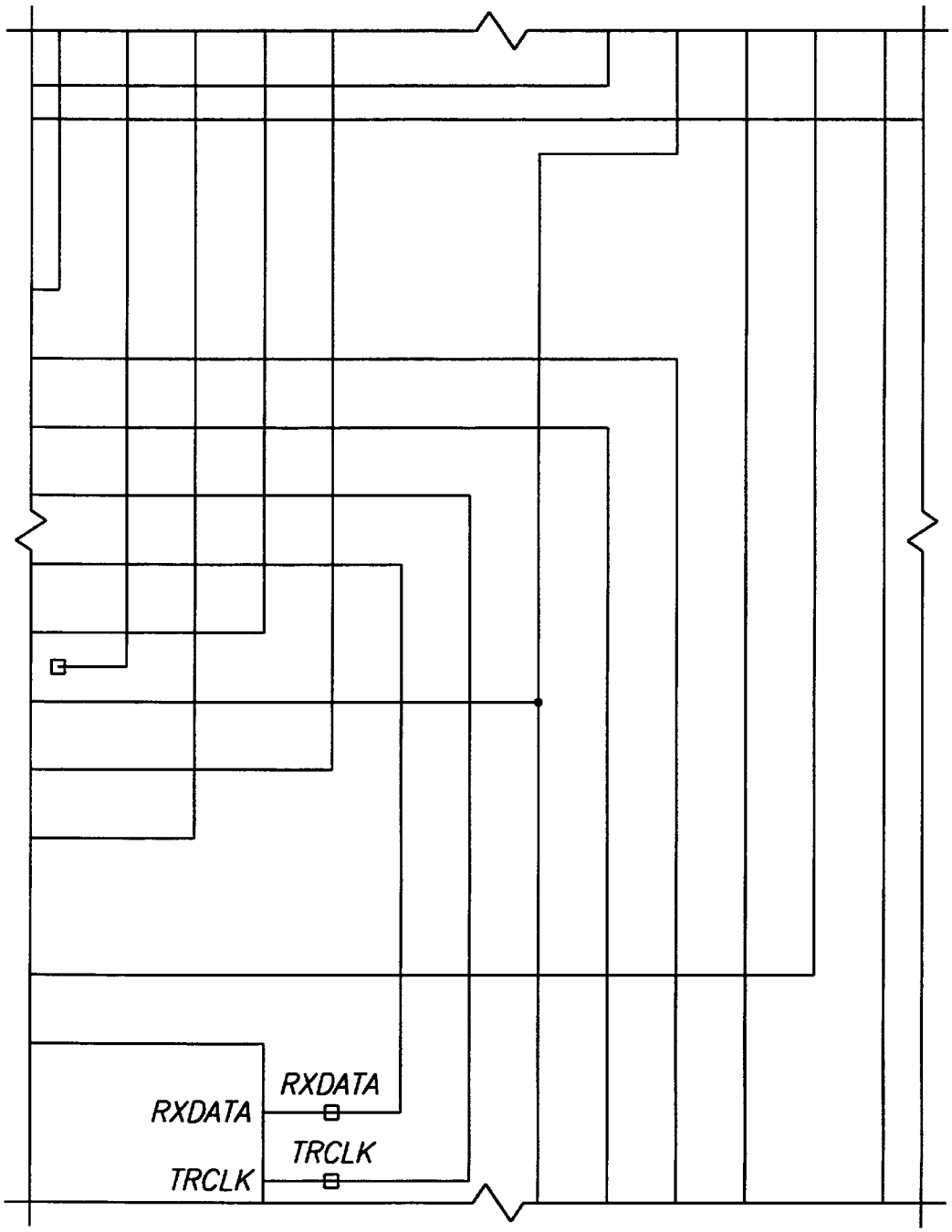


Fig 60II

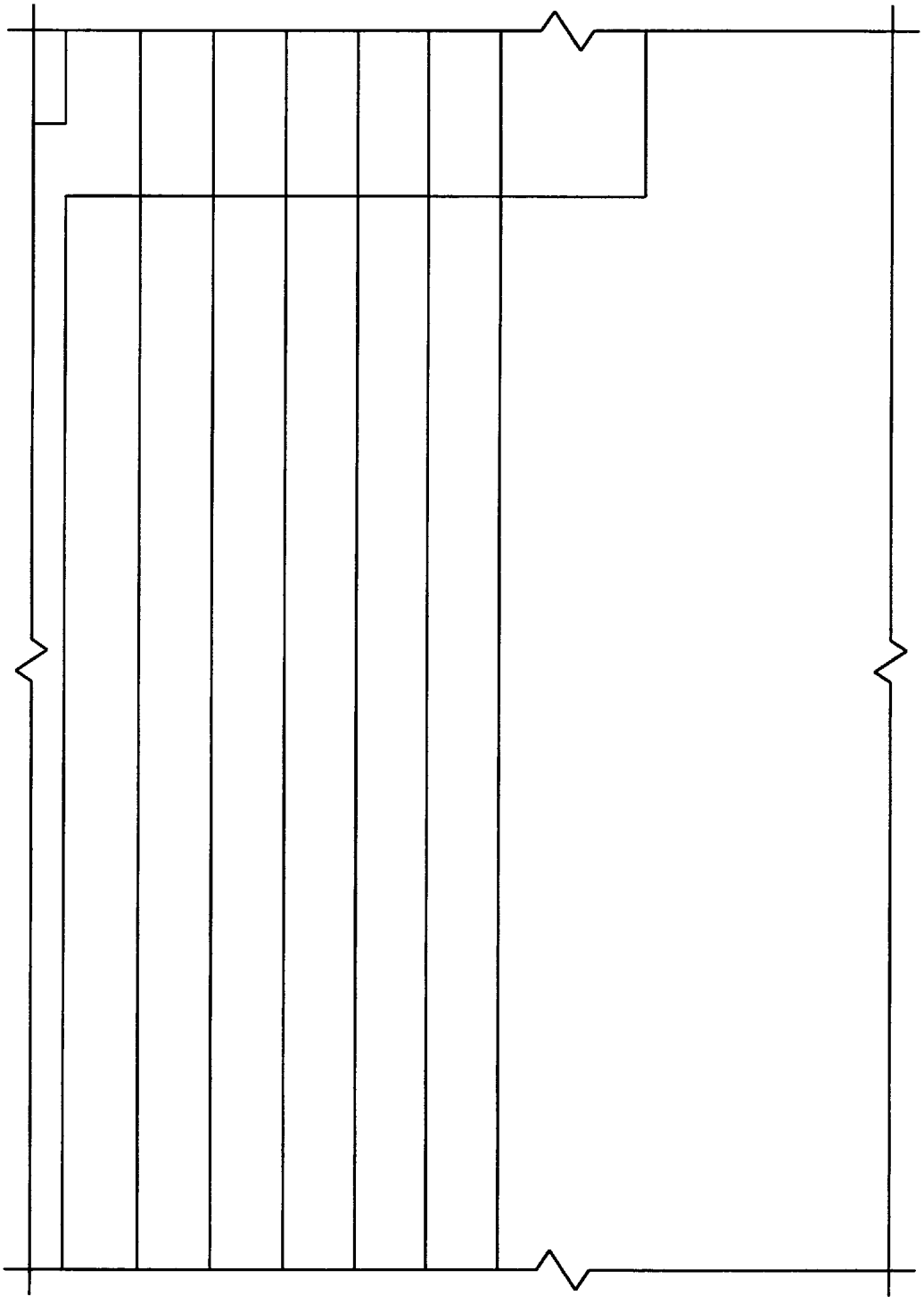


Fig 60d

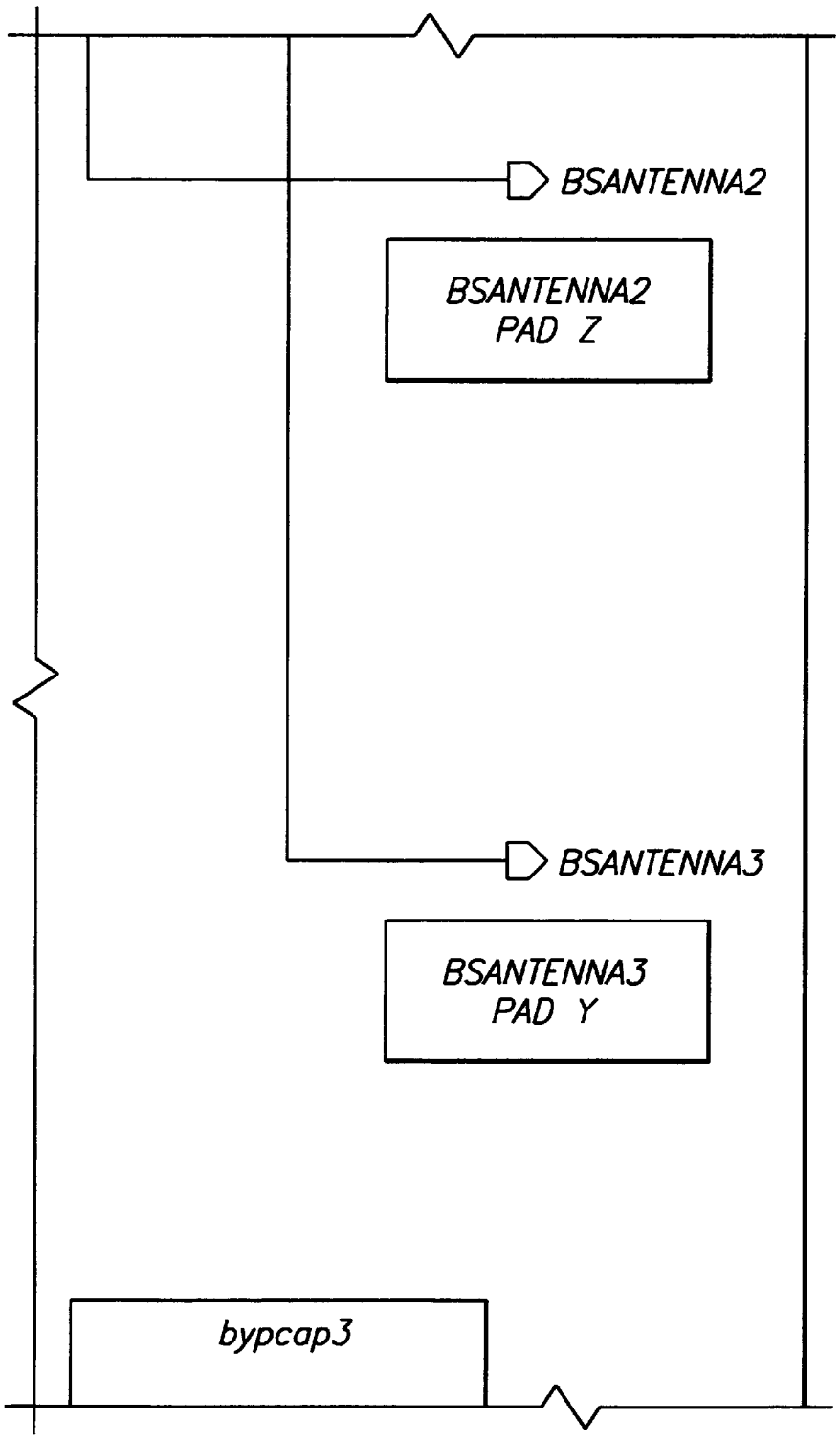

BSANTENNA2
BSANTENNA2
PAD Z
BSANTENNA3
BSANTENNA3
PAD Y
bypcap3

Fig 60K

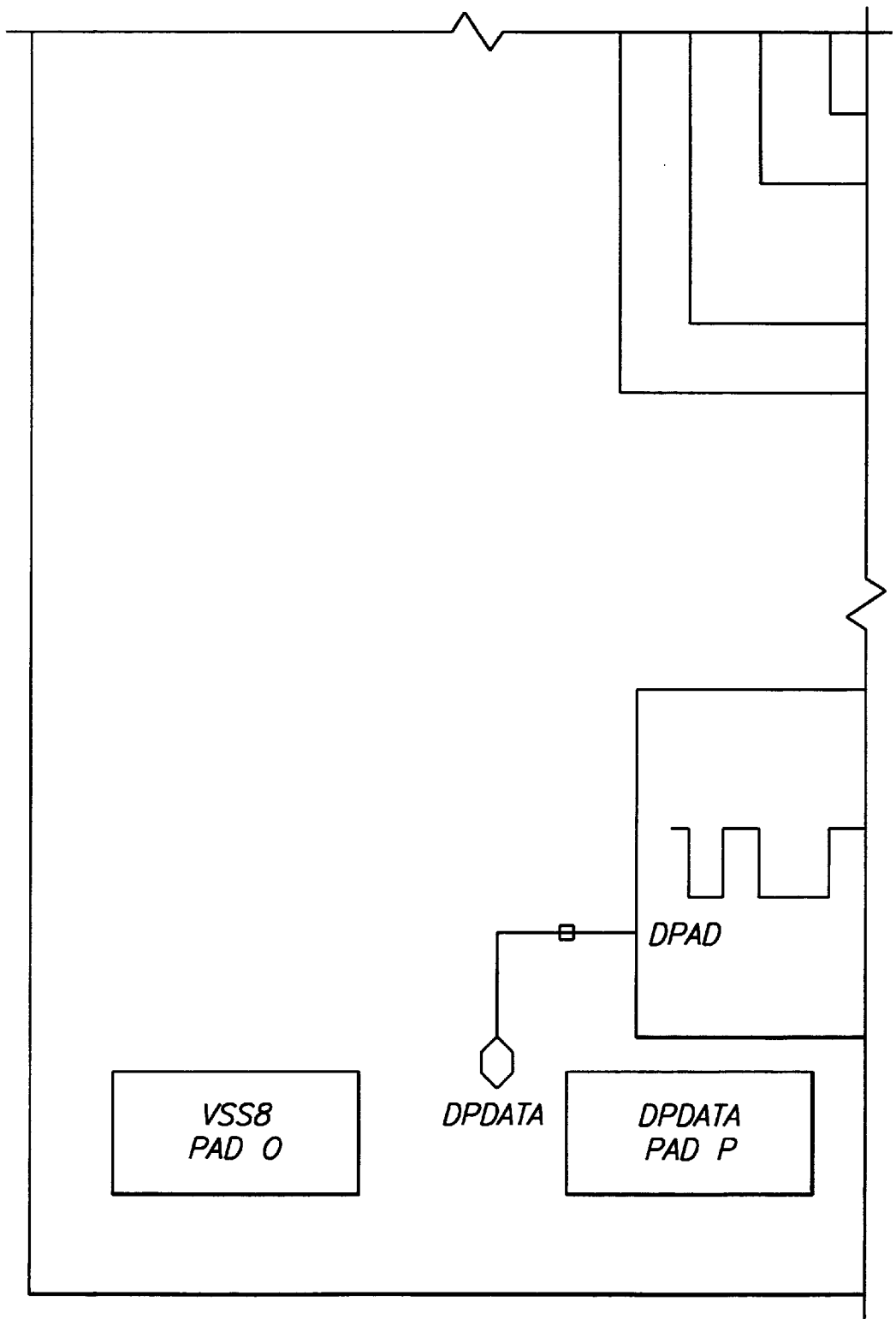


FIG 6EA

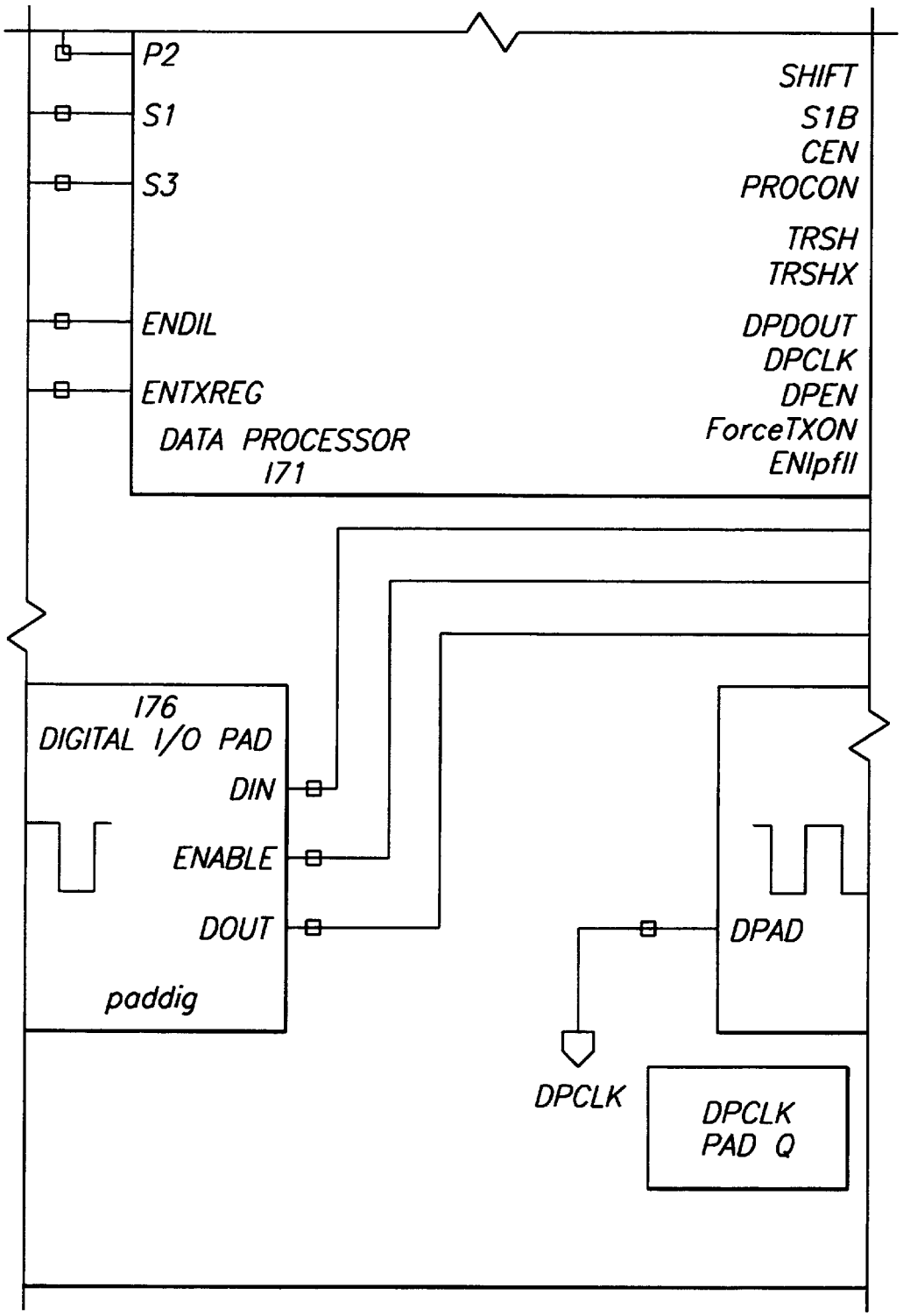

P2
S1
S3
ENDIL
ENTXREG
DATA PROCESSOR
171
SHIFT
S1B
CEN
PROCON
TRSH
TRSHX
DPDOUT
DPCLK
DPEN
ForceTXON
ENIpfII
176
DIGITAL I/O PAD
DIN
ENABLE
DOUT
paddig
DPAD
DPCLK
DPCLK
PAD Q

Fig 6EB

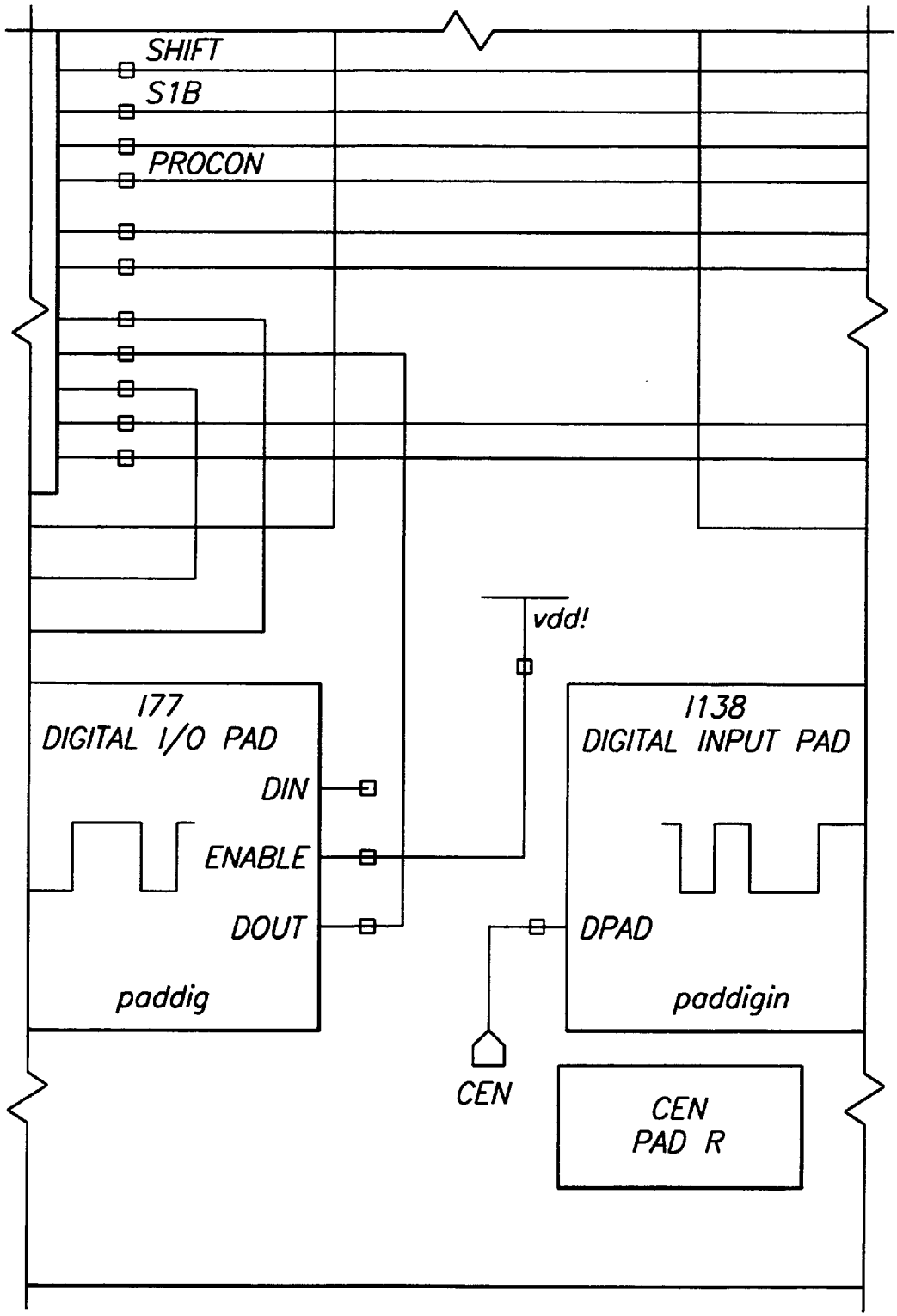

SHIFT
S1B
PROCON
vdd!
177
DIGITAL I/O PAD
DIN
ENABLE
DOUT
paddig
1138
DIGITAL INPUT PAD
DPAD
paddigin
CEN
CEN
PAD R

FIG 6EC

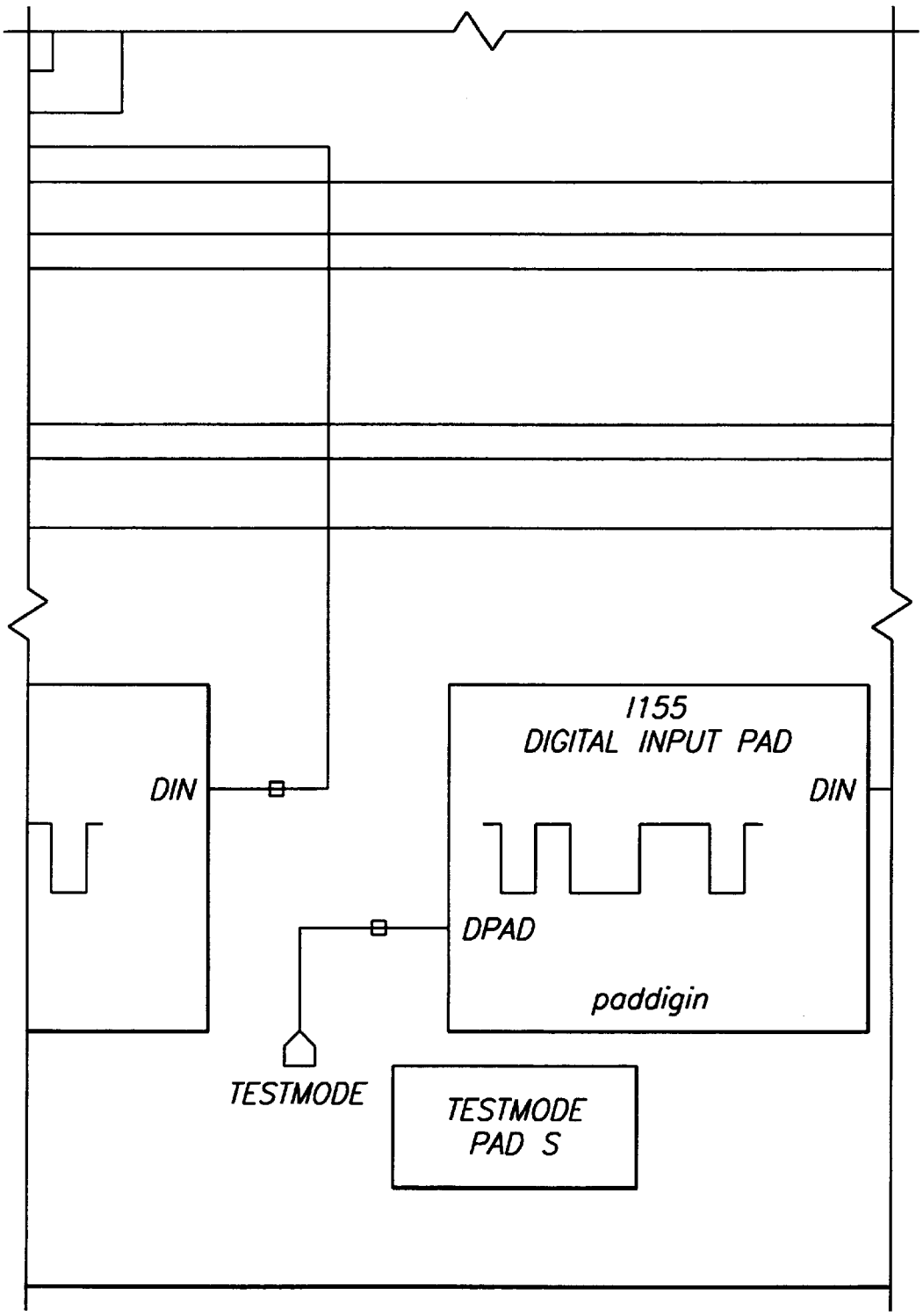

1155
DIGITAL INPUT PAD
DIN
DIN
DPAD
paddigin
TESTMODE
TESTMODE
PAD S

FIG 6ED

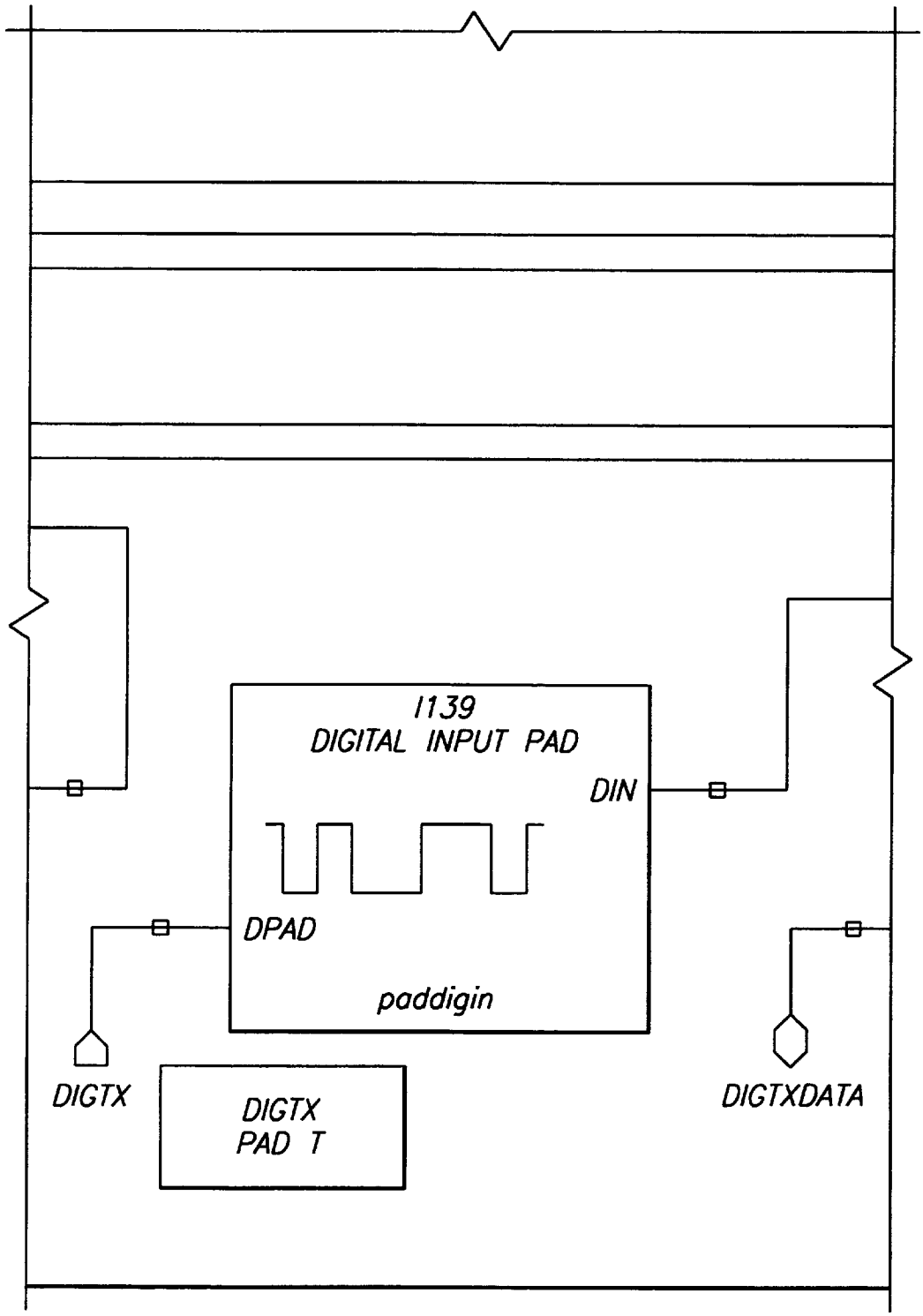

1139
DIGITAL INPUT PAD
DIN
DPAD
paddigin
DIGTX
DIGTX
PAD T
DIGTXDATA

Fig 6EE

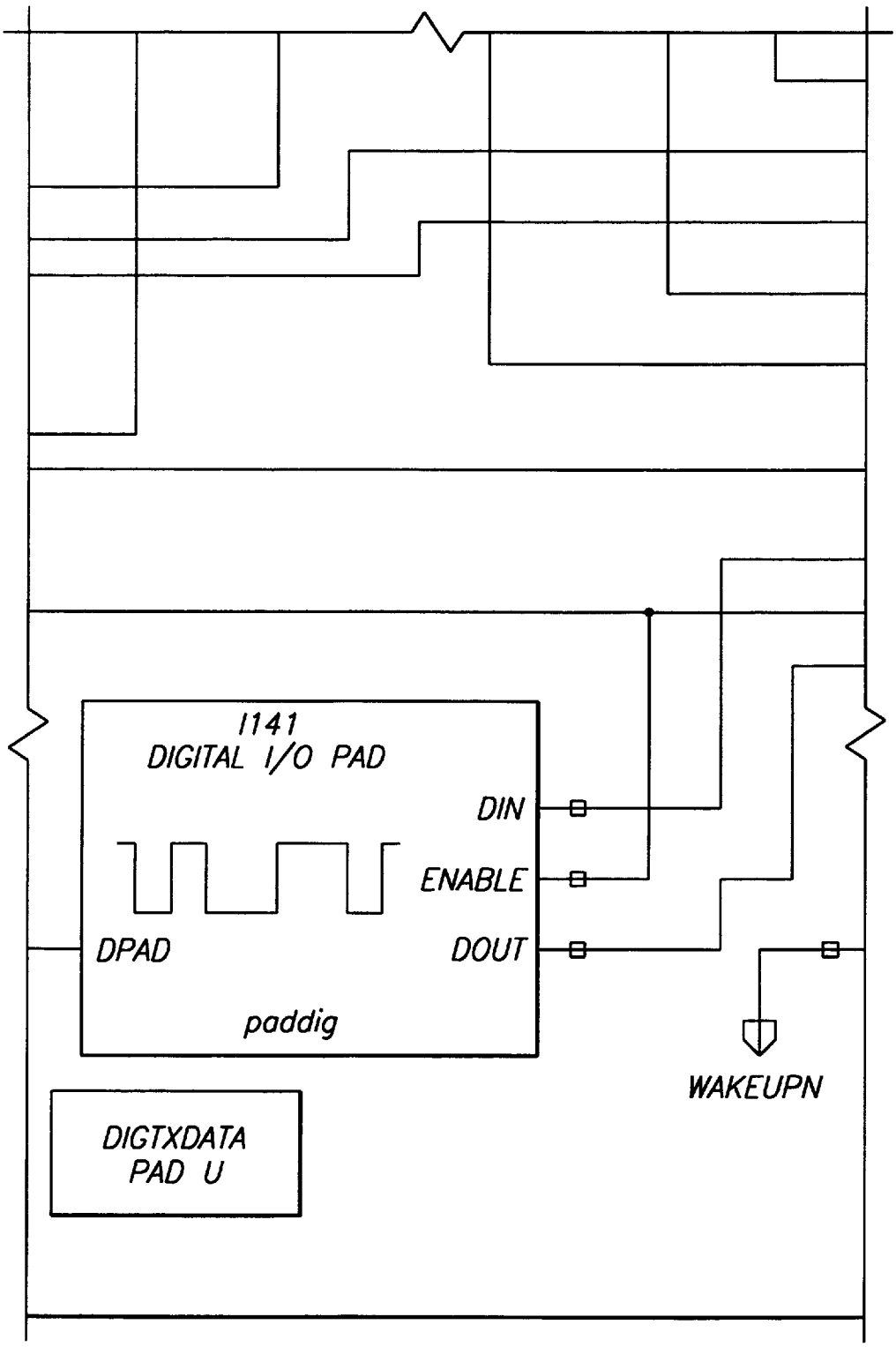

1141
DIGITAL I/O PAD
DIN
ENABLE
DPAD
DOUT
paddig
WAKEUPN
DIGTXDATA
PAD U

Fig 6EF

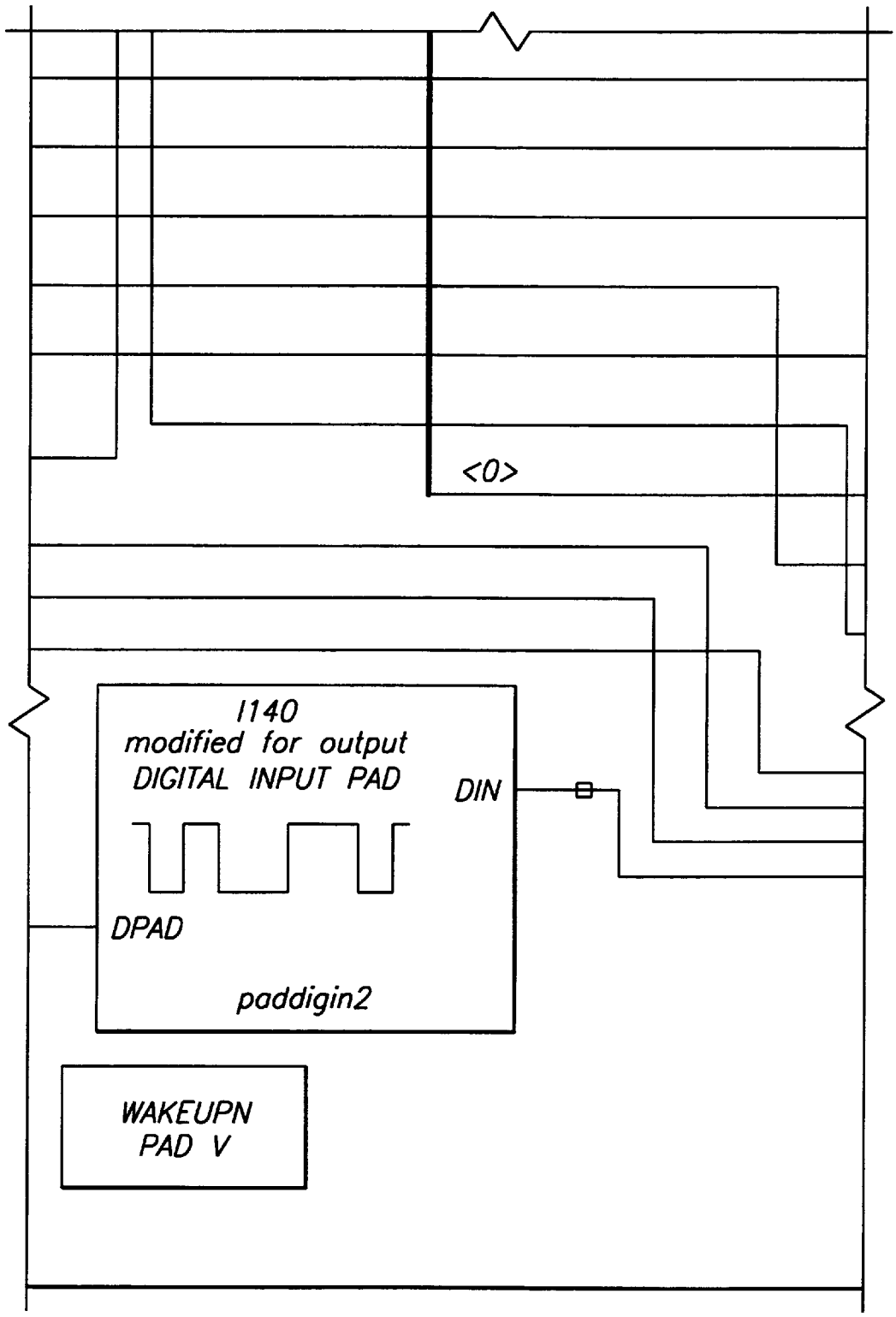

<0>
I140
modified for output
DIGITAL INPUT PAD
DIN
DPAD
paddigin2
WAKEUPN
PAD V

Fig 66G

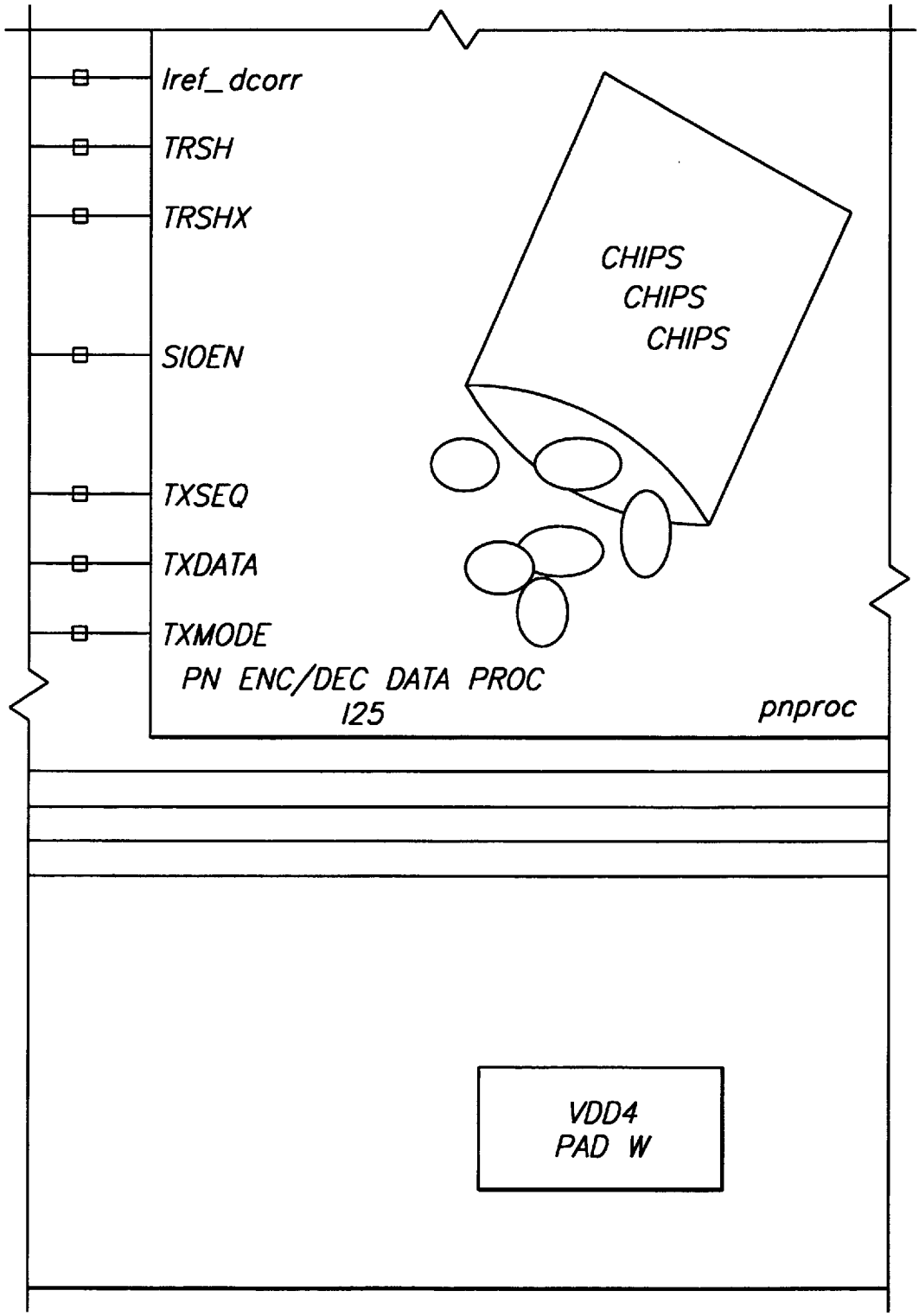

Iref_dcorr
TRSH
TRSHX
SIOEN
TXSEQ
TXDATA
TXMODE
CHIPS
CHIPS
CHIPS
PN ENC/DEC DATA PROC
125
pnproc
VDD4
PAD W

FIG 6EH

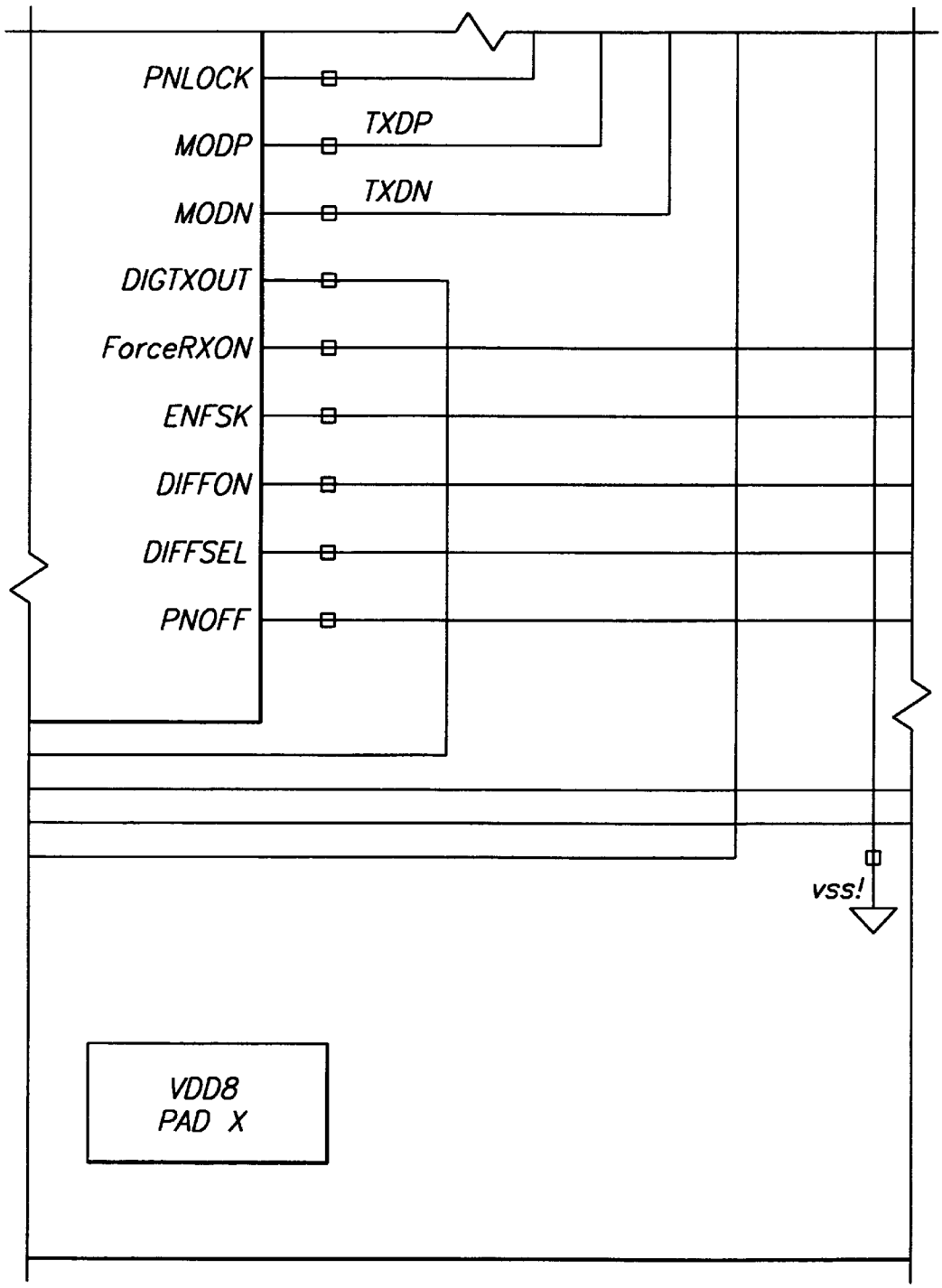

PNLOCK
MODP
TXDP
MODN
TXDN
DIGTXOUT
ForceRXON
ENFSK
DIFFON
DIFFSEL
PNOFF
vss!
VDD8
PAD X

Fig 6E1

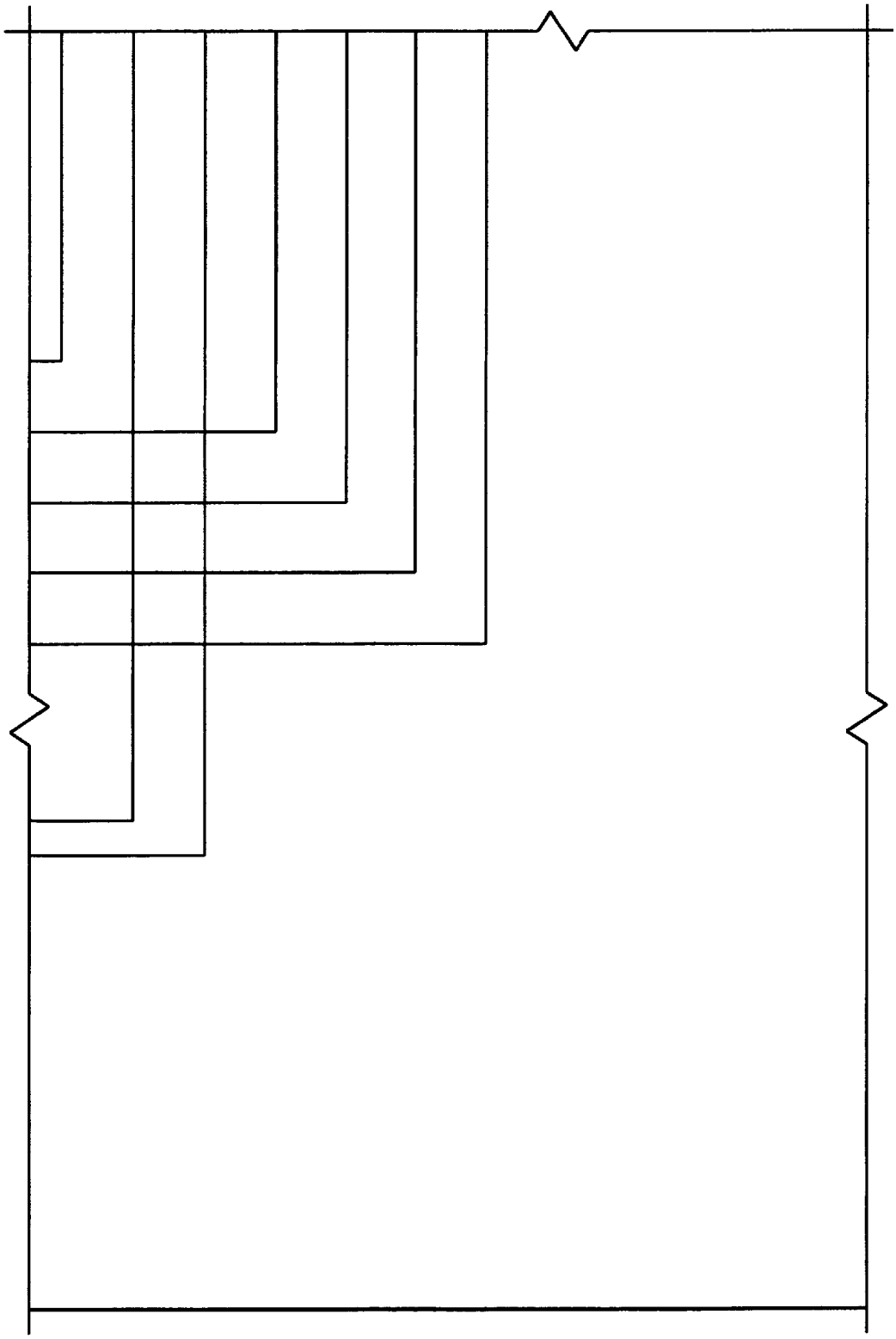


Fig 6Ed

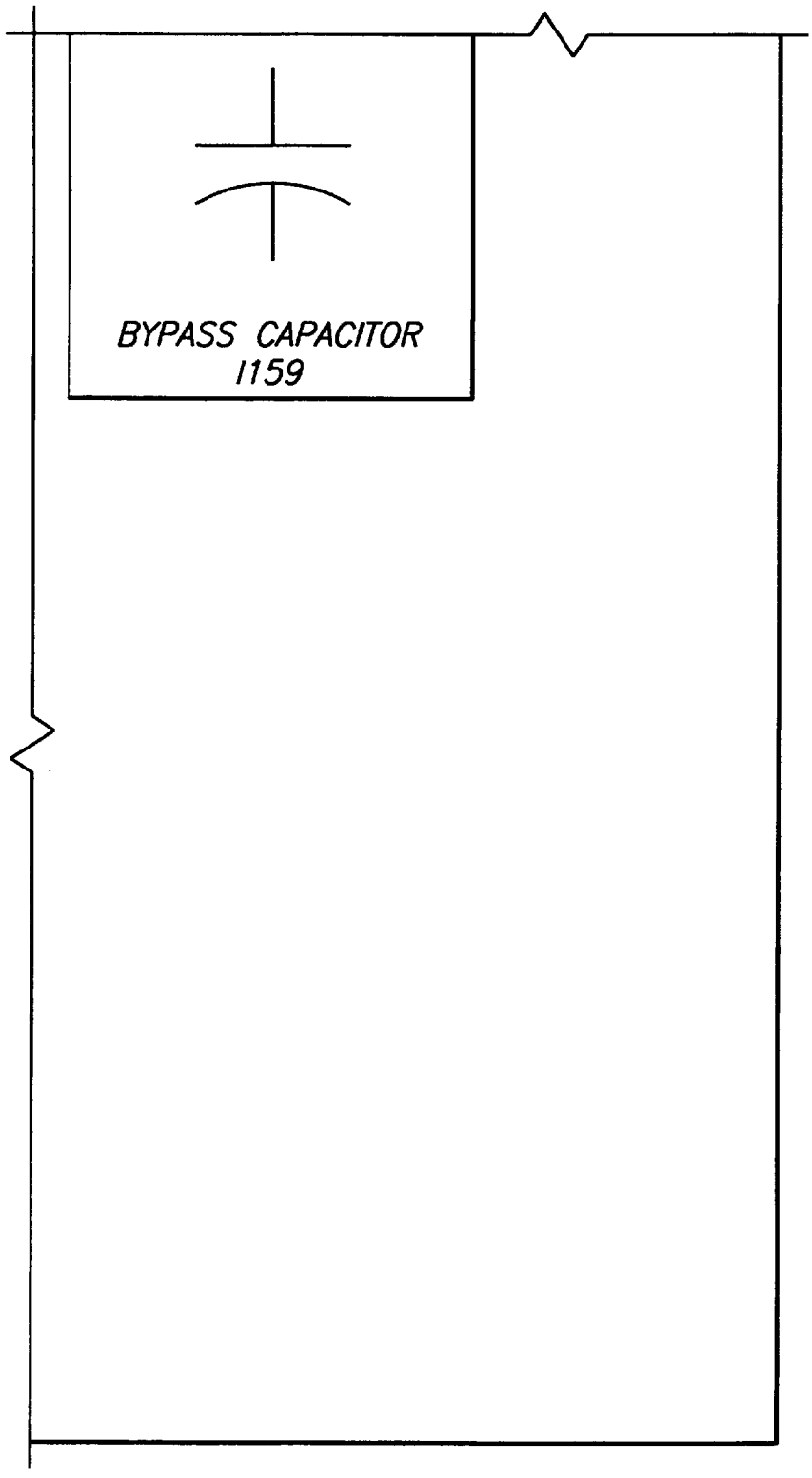


FIG 6EK

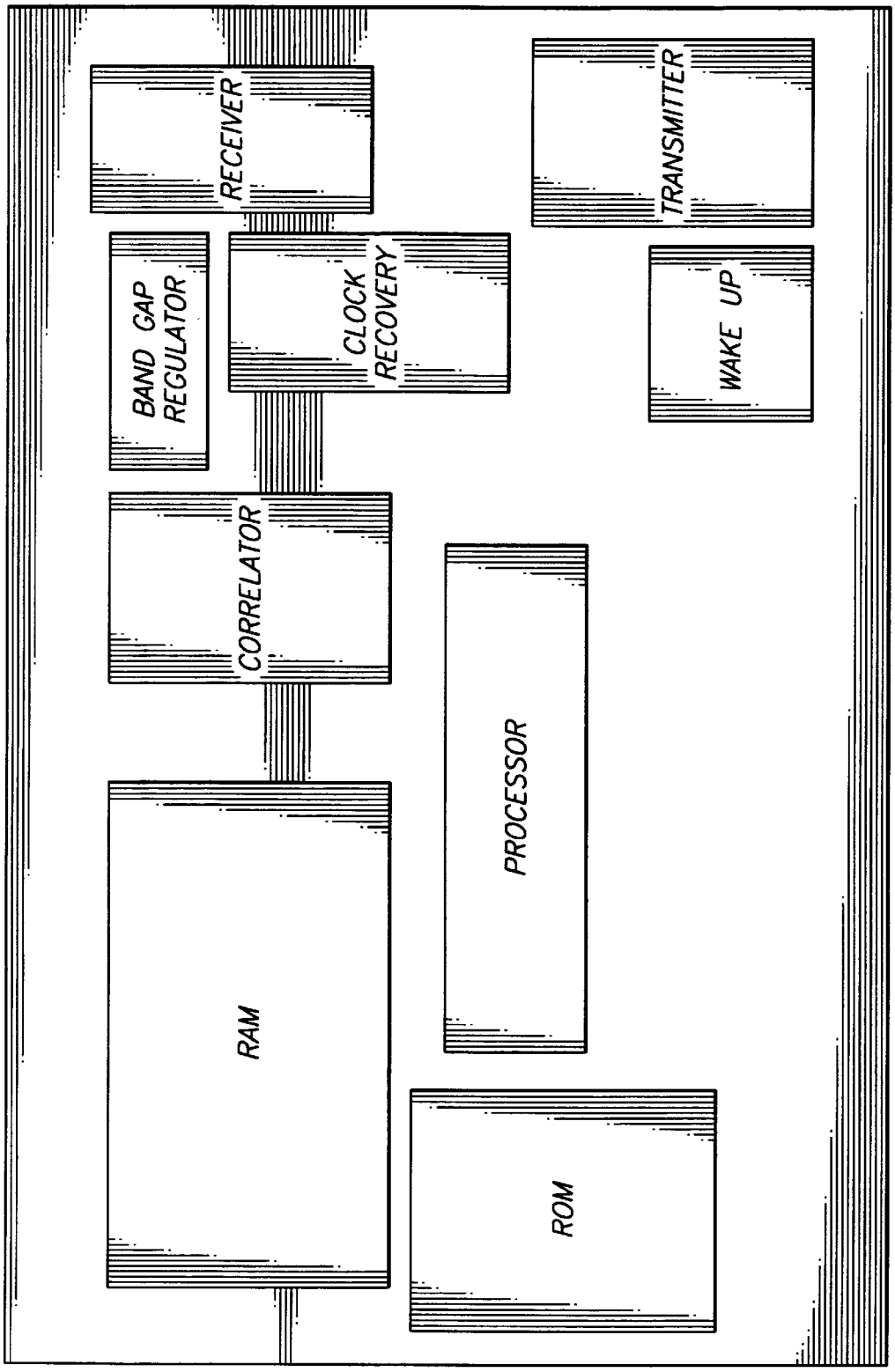


FIG. 59 (SHEET 60)

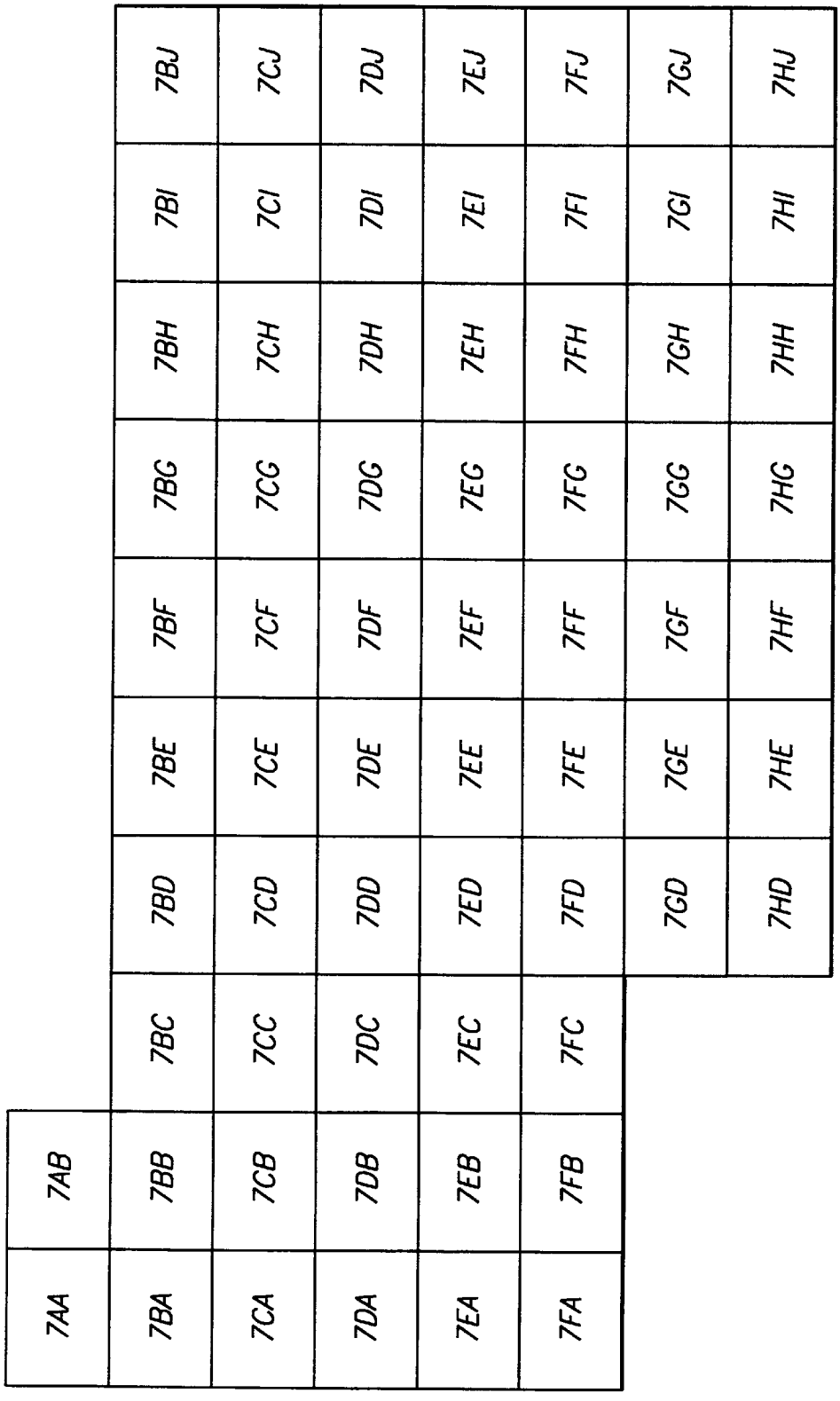
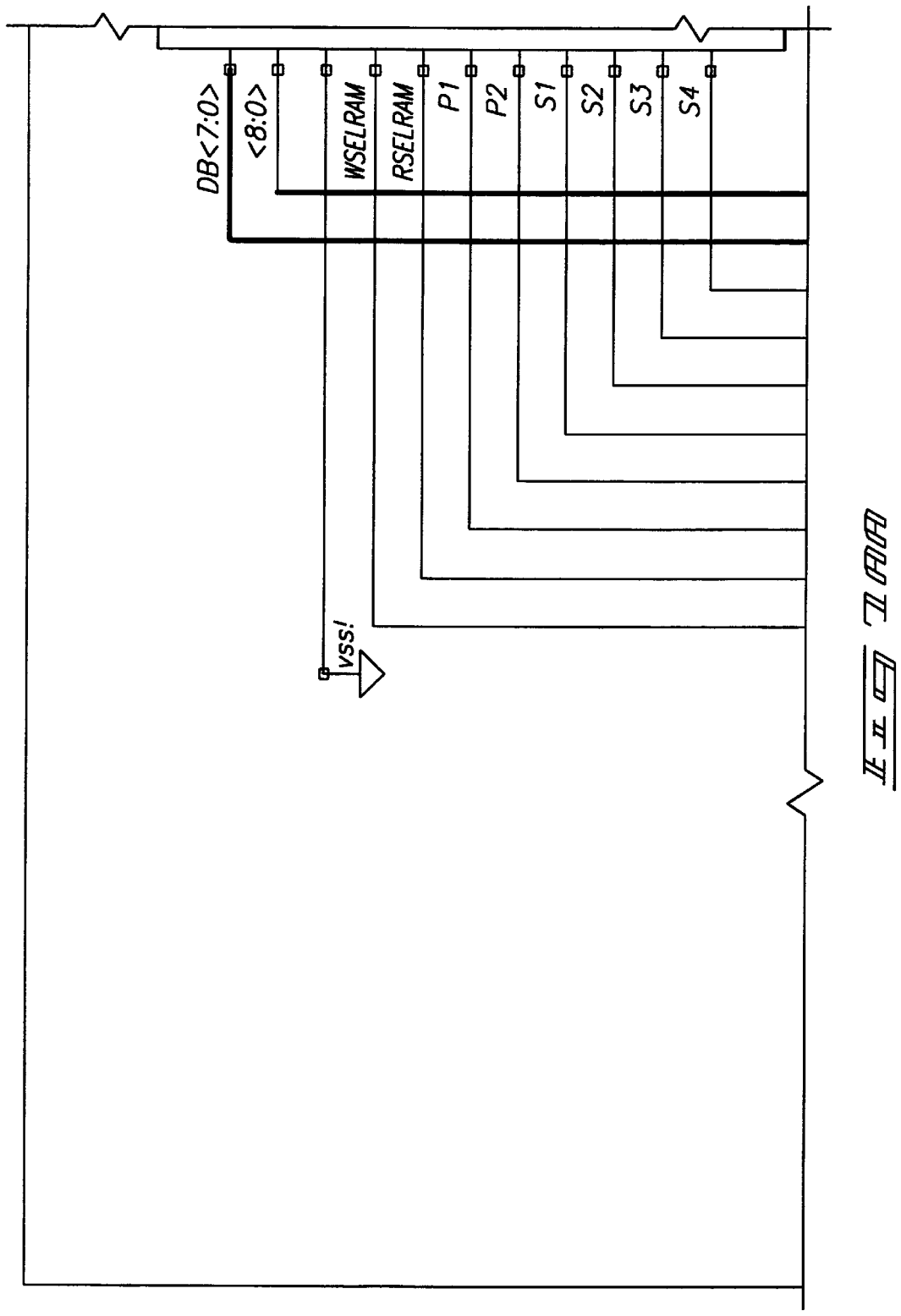

7AA
7AB
7BA
7BB
7BC
7BD
7BE
7BF
7BG
7BH
7BI
7BJ
7CA
7CB
7CC
7CD
7CE
7CF
7CG
7CH
7CI
7CJ
7DA
7DB
7DC
7DD
7DE
7DF
7DG
7DH
7DI
7DJ
7EA
7EB
7EC
7ED
7EE
7EF
7EG
7EH
7EI
7EJ
7FA
7FB
7FC
7FD
7FE
7FF
7FG
7FH
7FI
7FJ
7GD
7GE
7GF
7GG
7GH
7GI
7GJ
7HD
7HE
7HF
7HG
7HH
7HI
7HJ

FIG. 7H


DB<7:0>
<8:0>
WSELRAM
RSELRAM
P1
P2
S1
S2
S3
S4
vss!
VDD

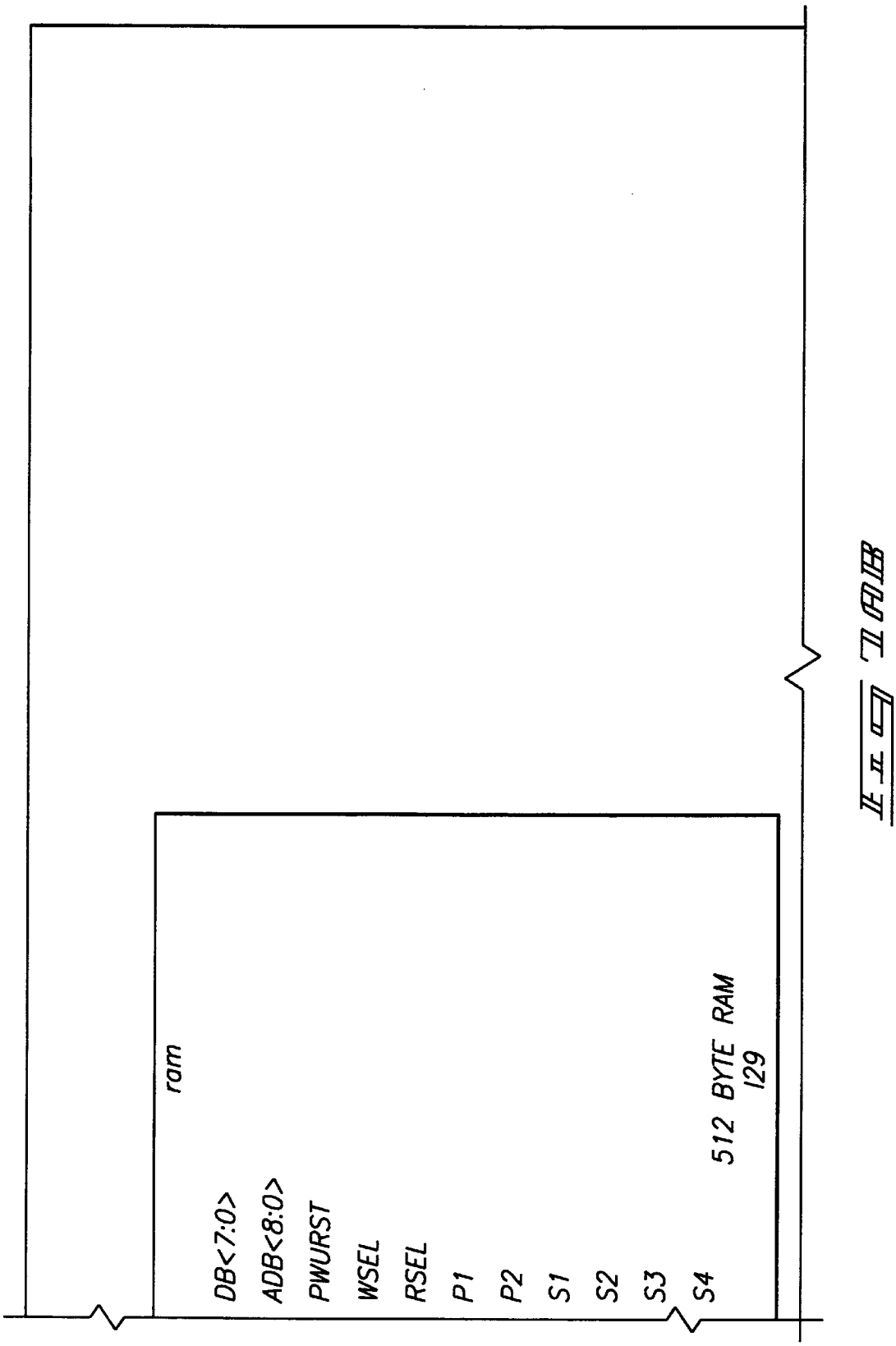
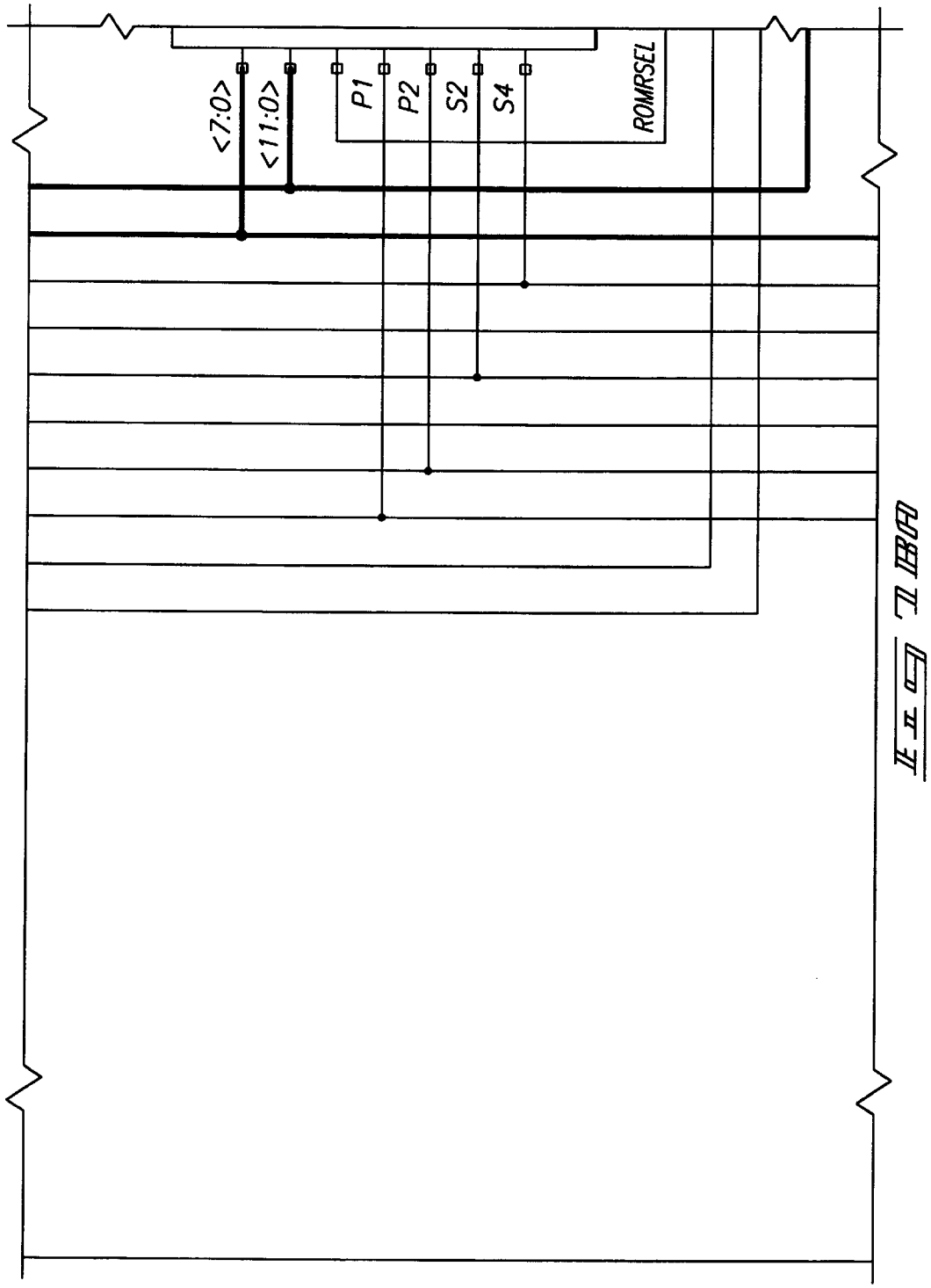


FIG. 63A
ram
DB<7:0>
ADB<8:0>
PWURST
WSEL
RSEL
P1
P2
S1
S2
S3
S4
512 BYTE RAM
129


<7:0>
<11:0>
P1
P2
S2
S4
ROMRSEL
БАЙТ

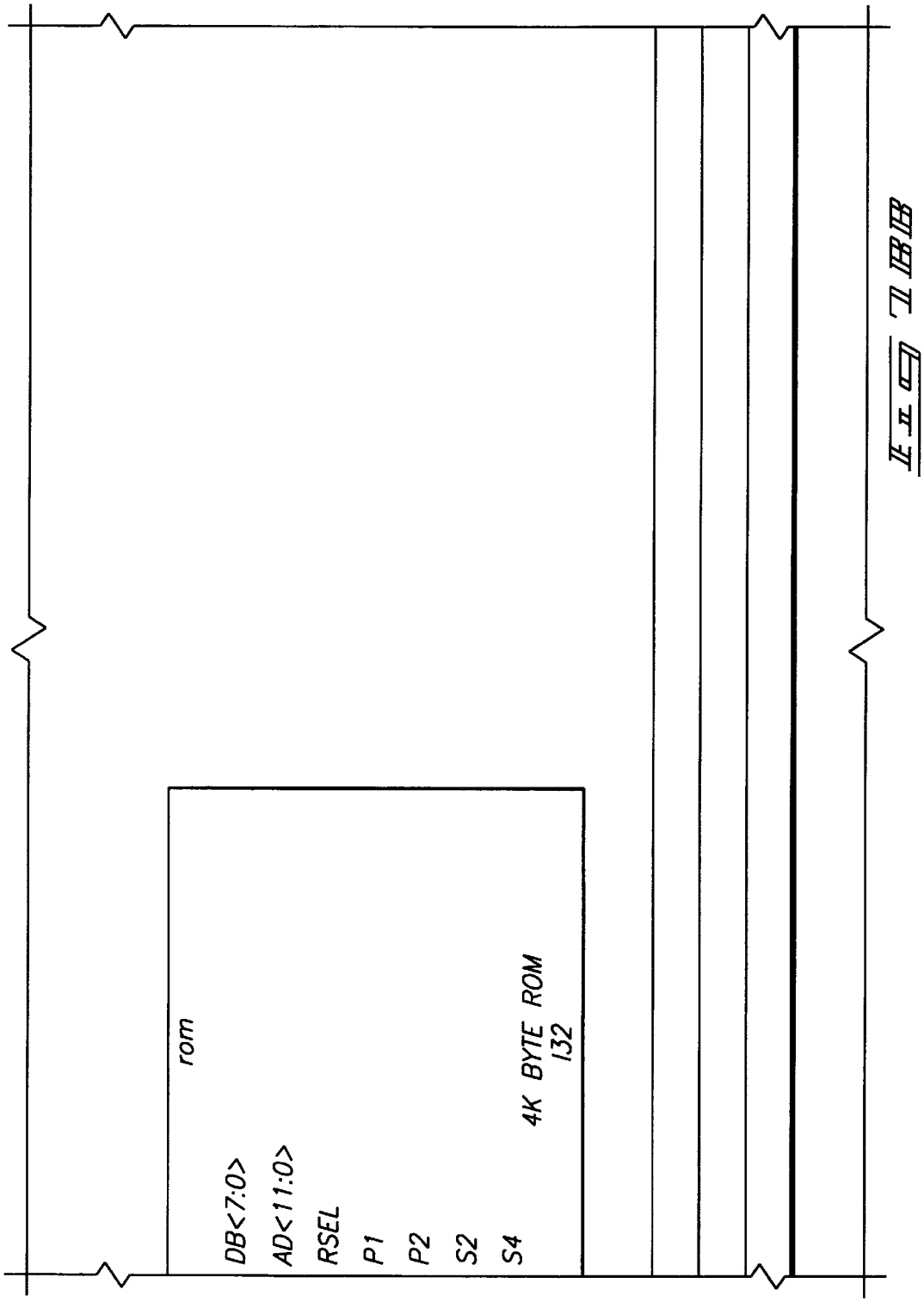
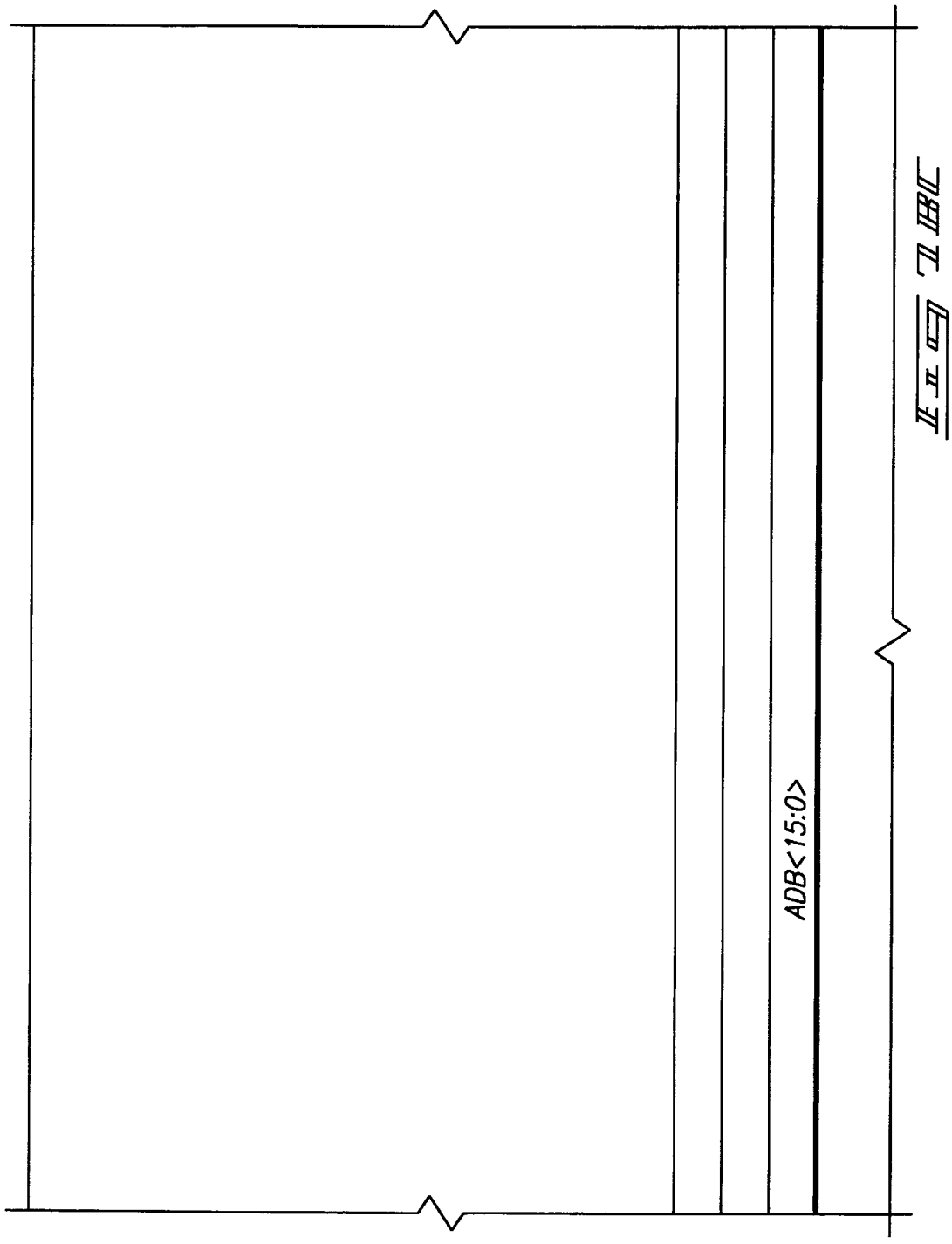


FIG 11B
4K BYTE ROM
132
rom
DB<7:0>
AD<11:0>
RSEL
P1
P2
S2
S4


ADB<15:0>

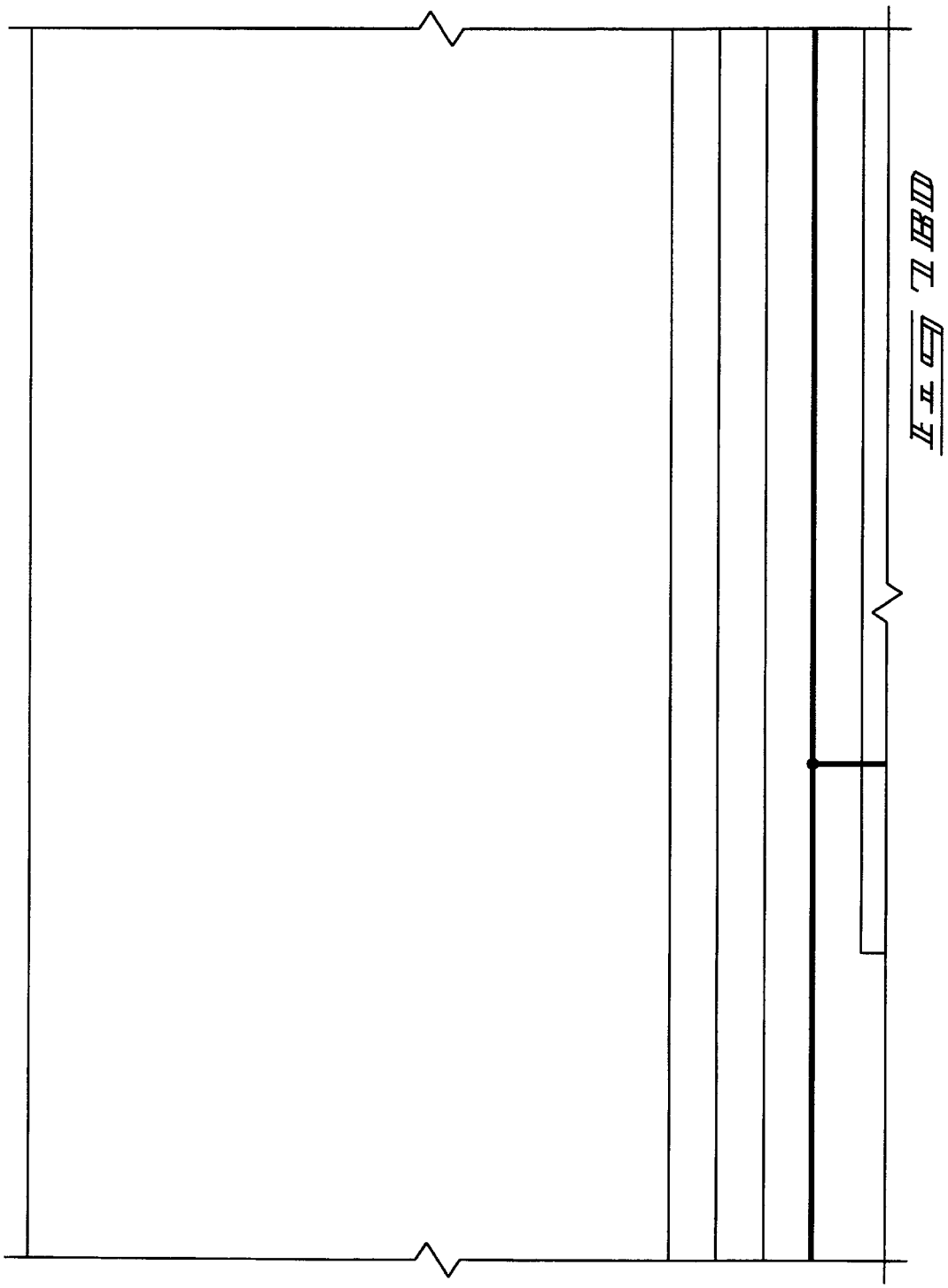


FIG. 67L

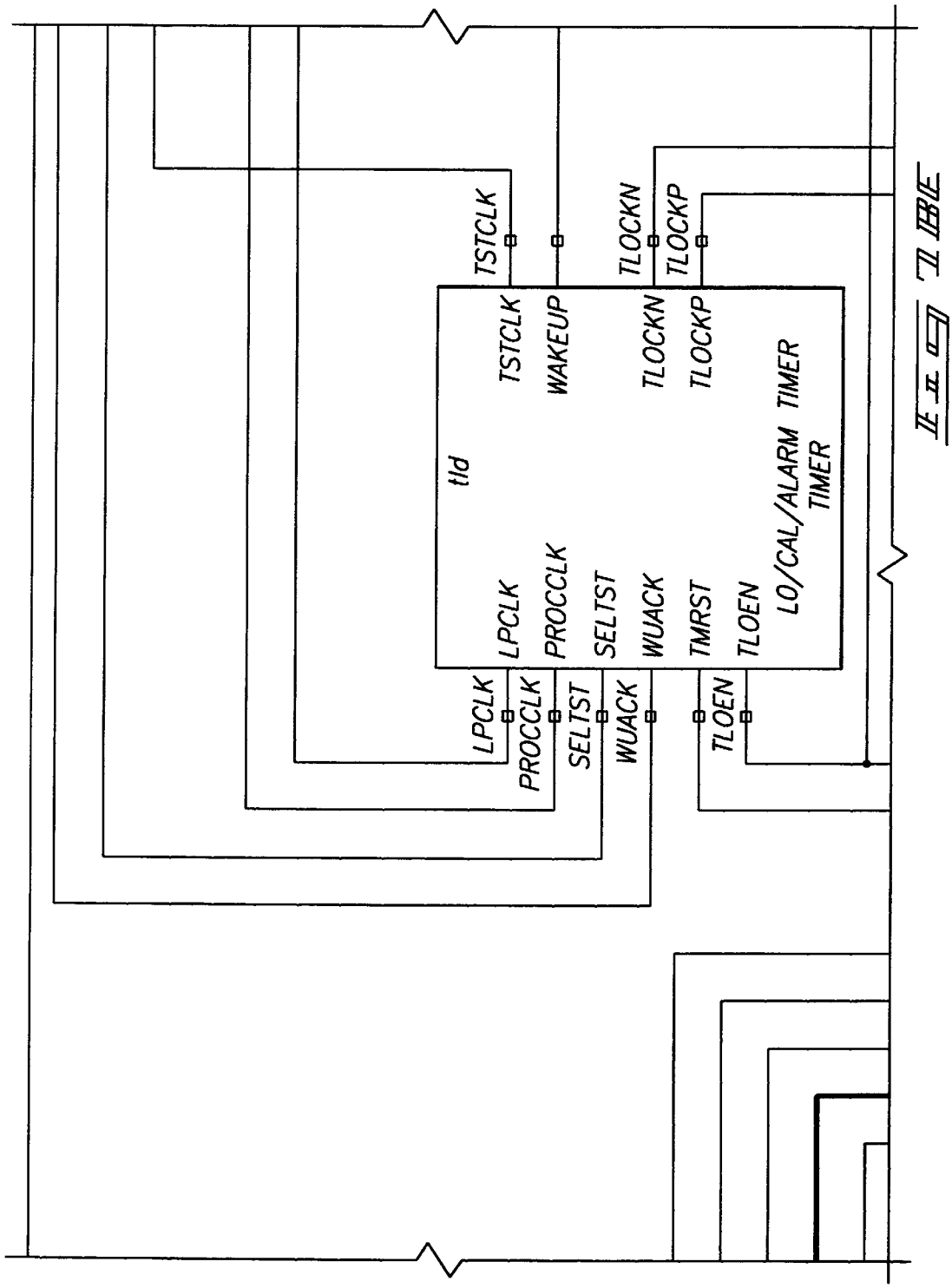
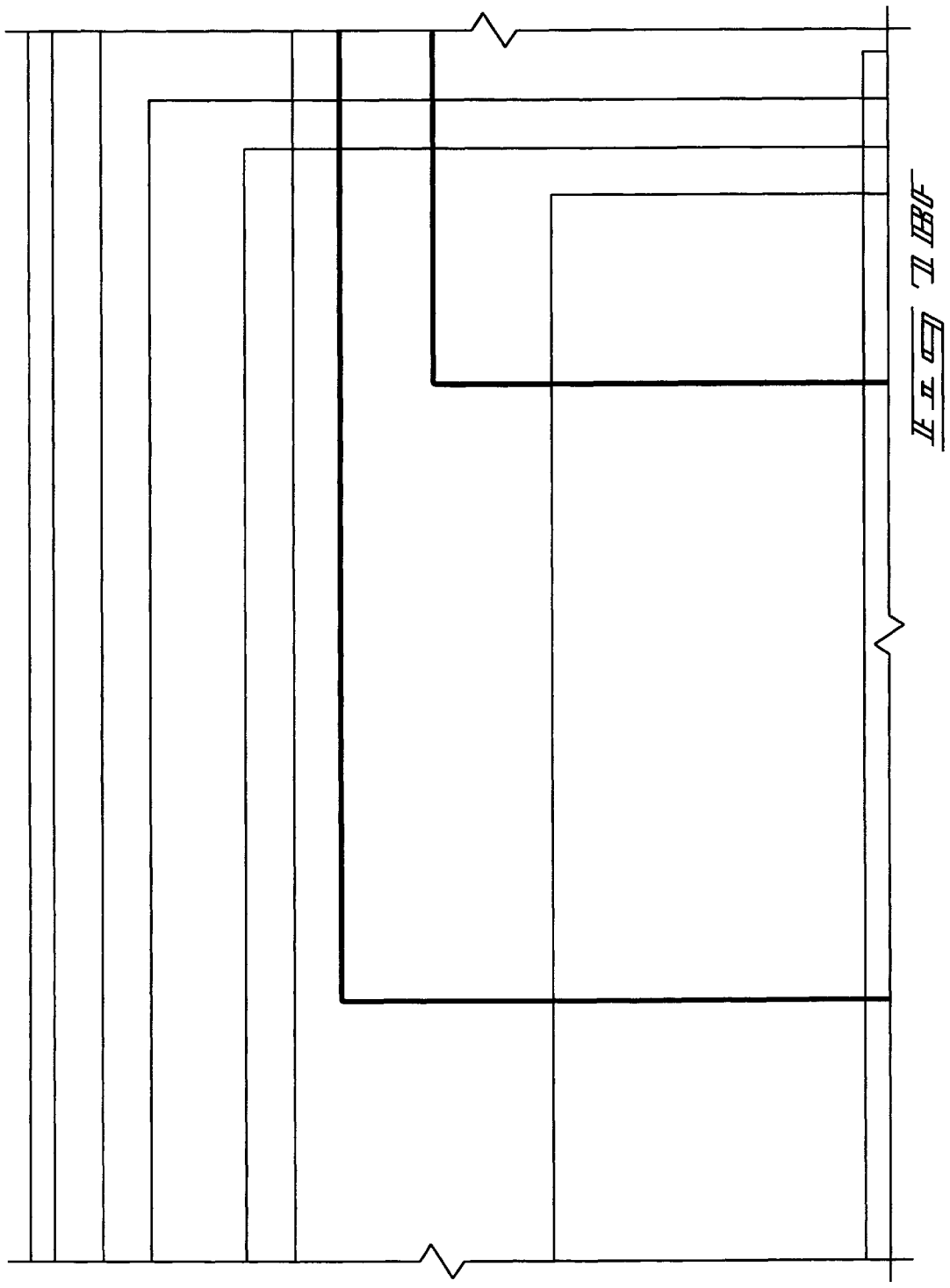
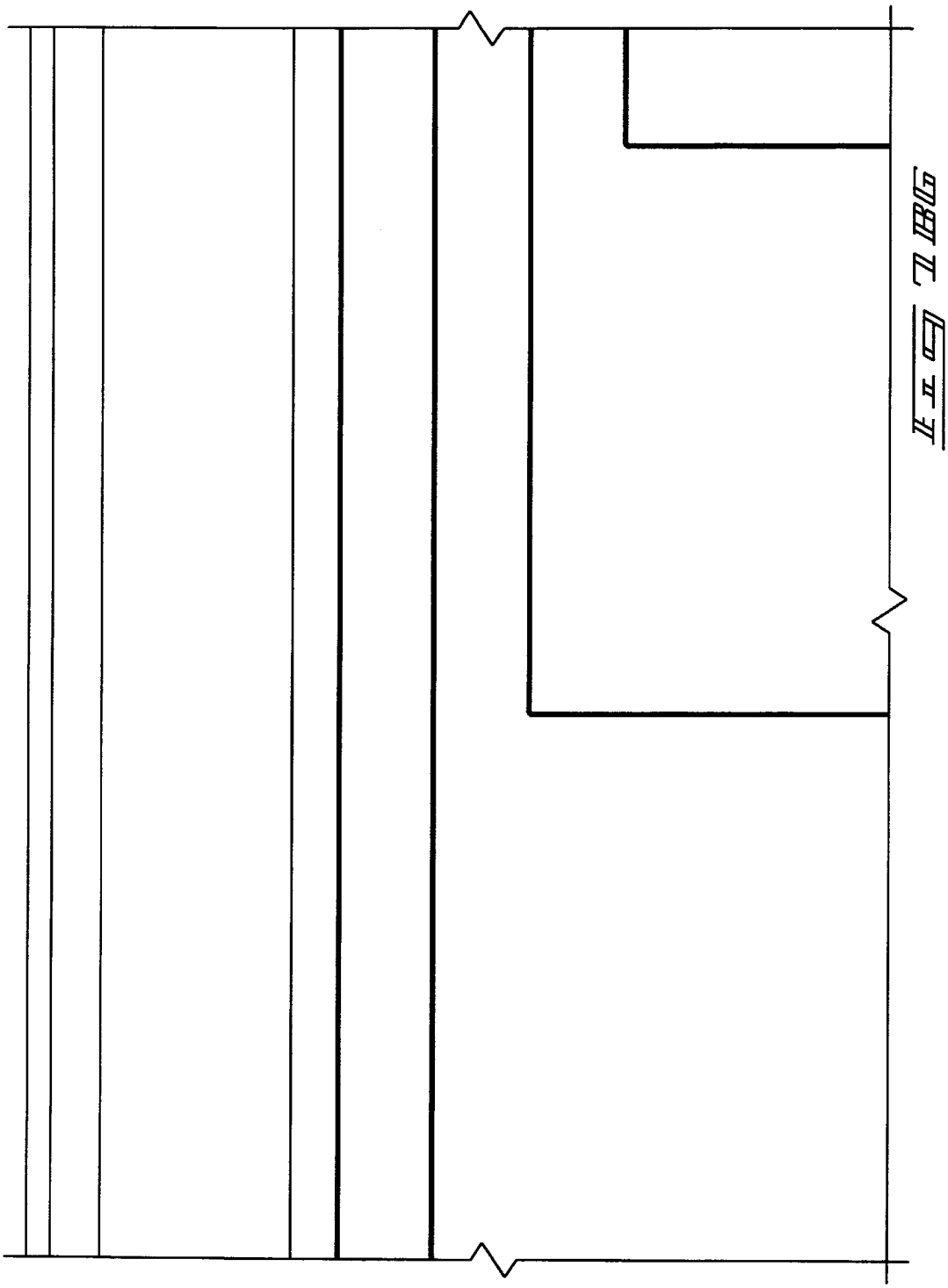
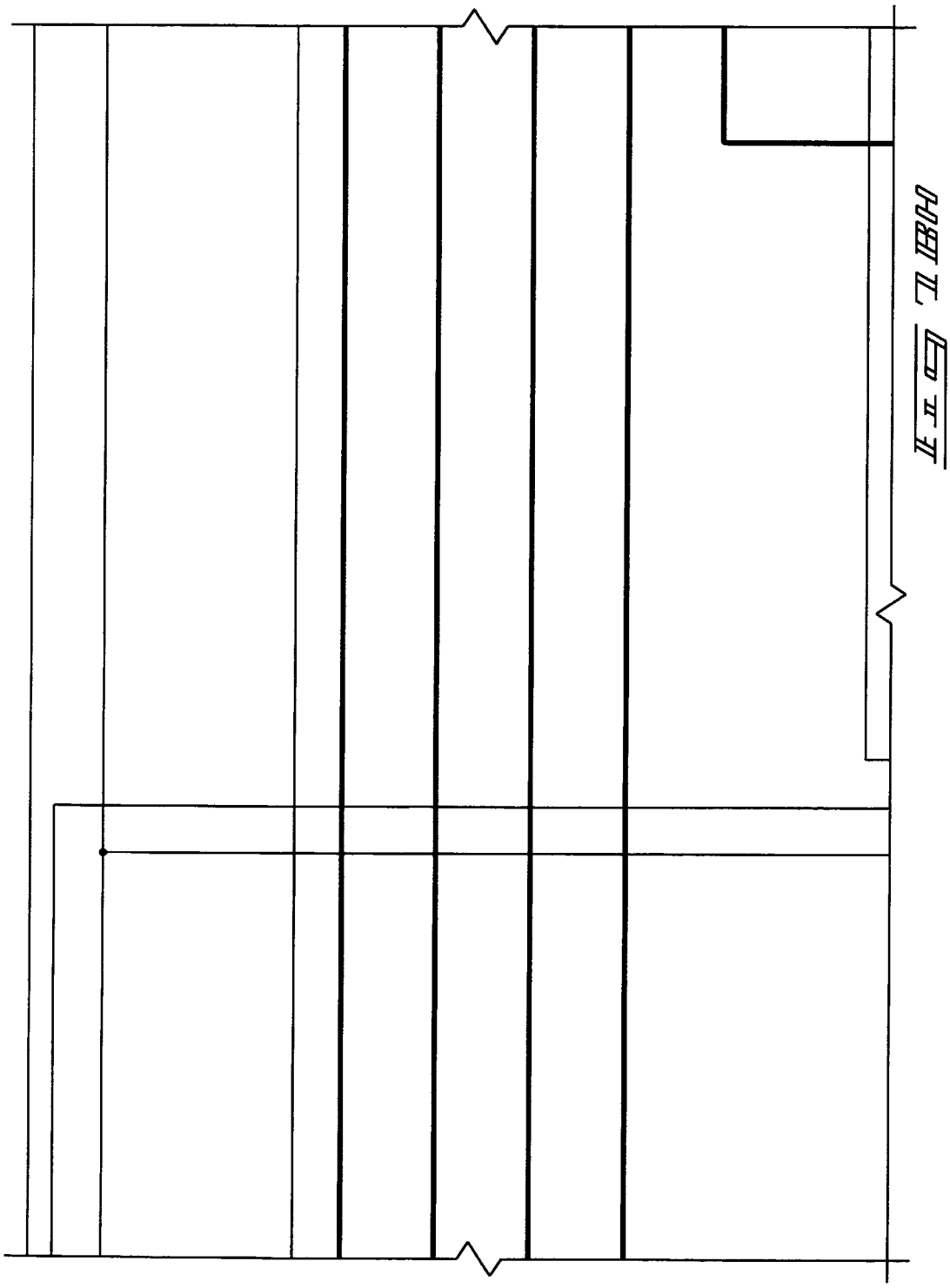


FIG. 11E
TSTCLK
TLOCKN
TLOCKP
tld
TSTCLK
WAKEUP
TLOCKN
TLOCKP
TIMER
LO/CAL/ALARM
TIMER
LPCLK
PROCCLK
SELTST
WUACK
TMRST
TLOEN
LPCLK
PROCCLK
SELTST
WUACK
TLOEN




SHEET 69 OF



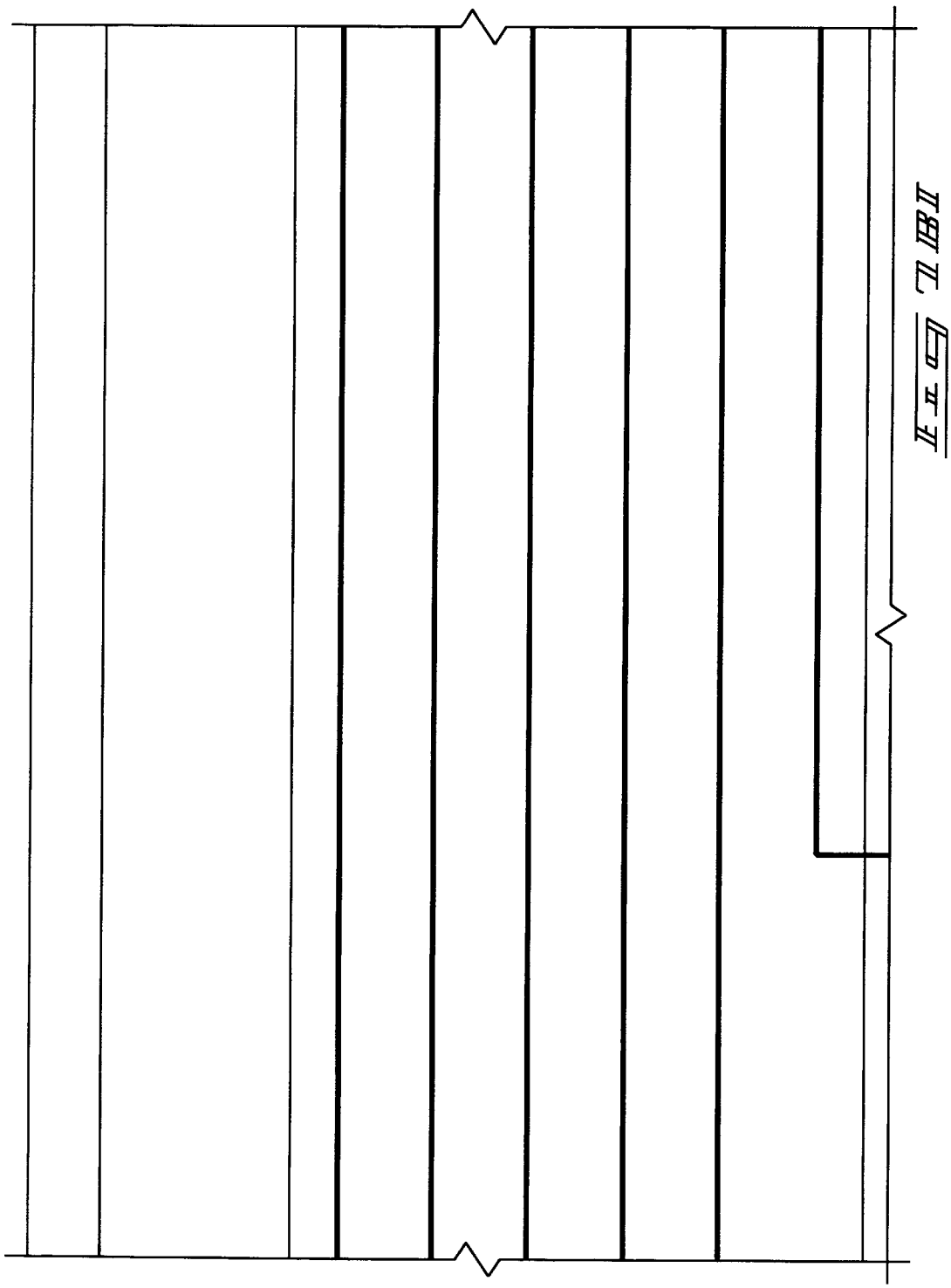
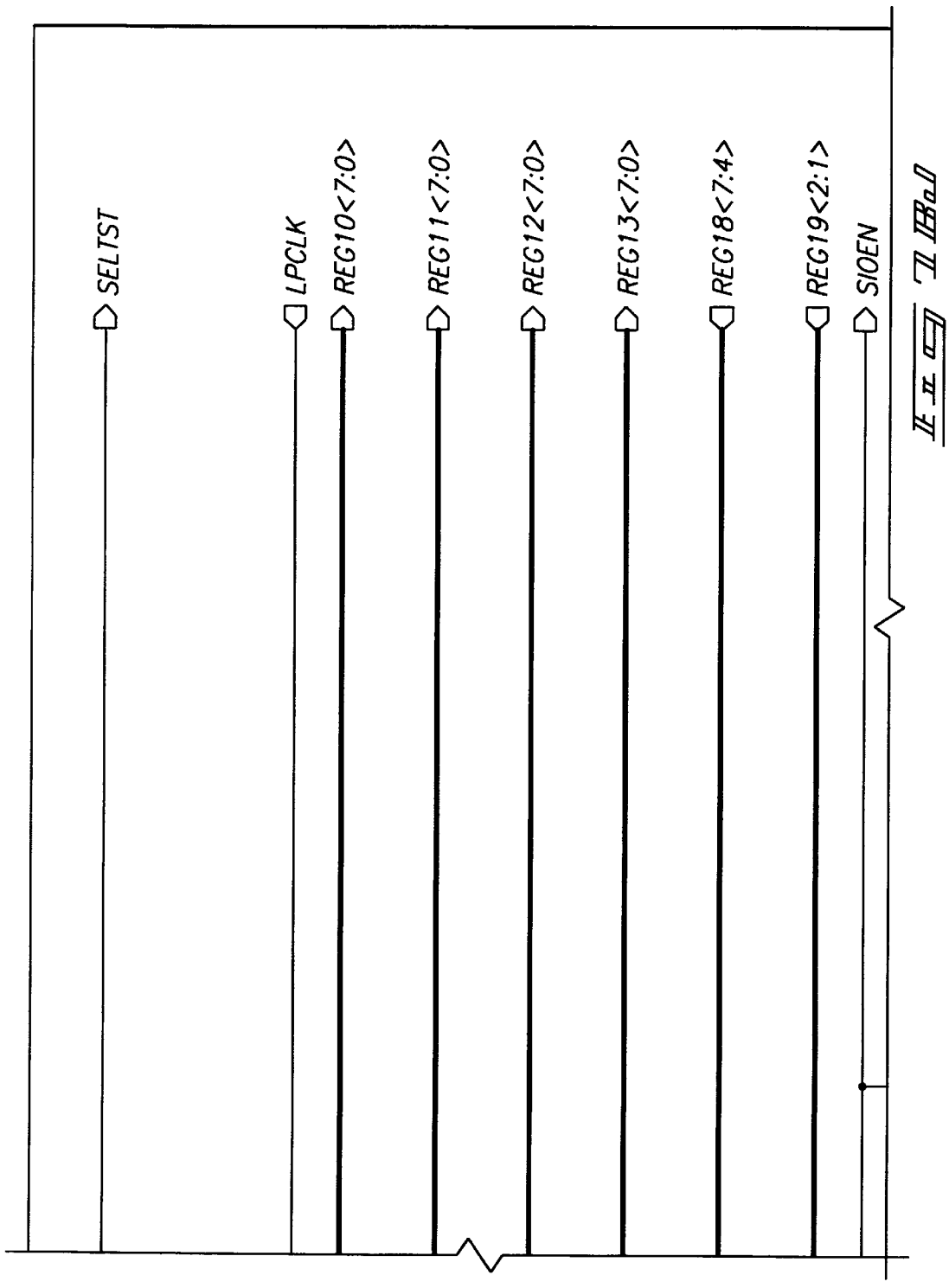
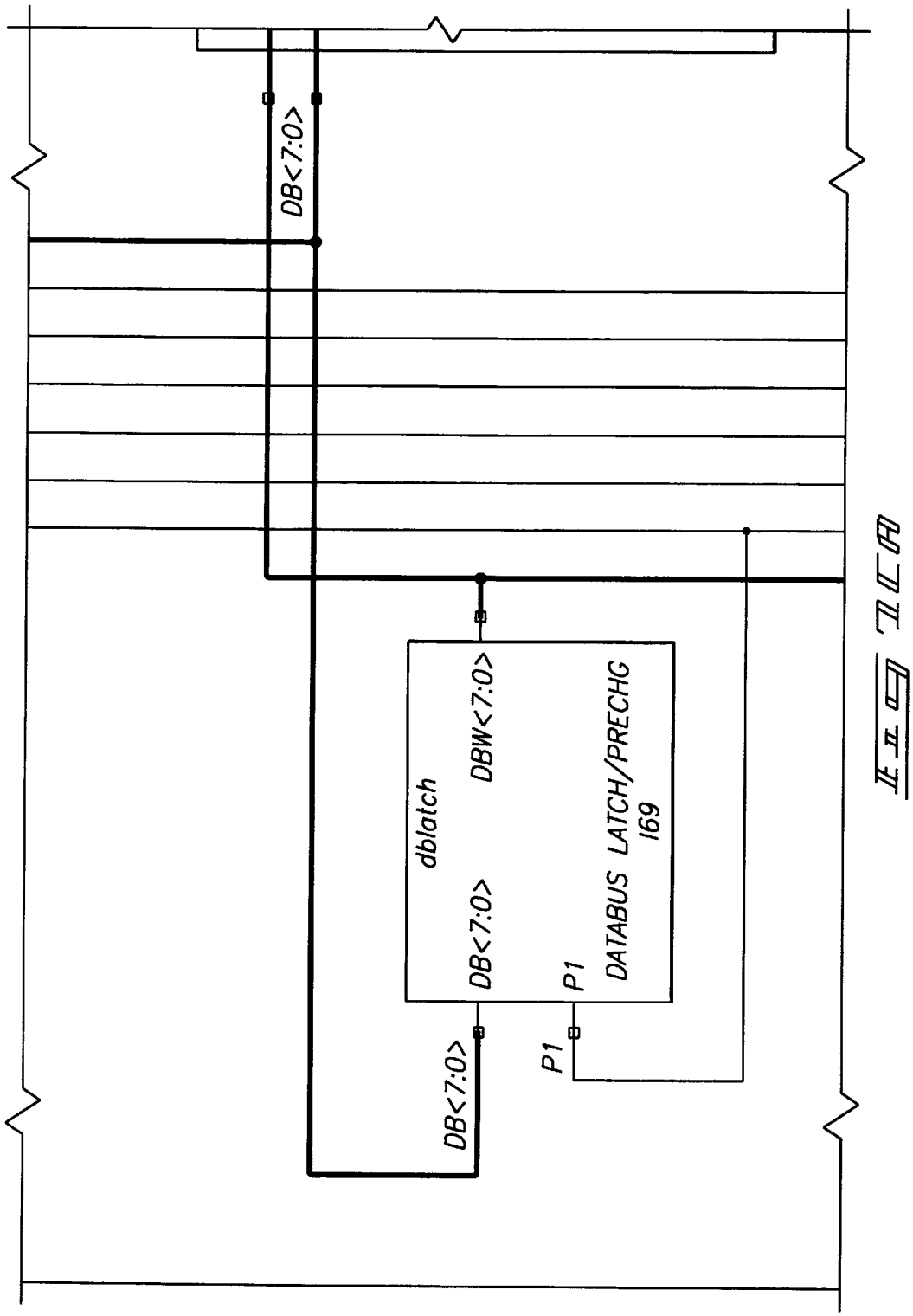


FIG. 72


SELTST
LPCLK
REG10<7:0>
REG11<7:0>
REG12<7:0>
REG13<7:0>
REG18<7:4>
REG19<2:1>
SIOEN


DB<7:0>
dblatch
DBW<7:0>
DB<7:0>
P1
DATABUS LATCH/PRECHG
169
DB<7:0>
P1
BUFFER

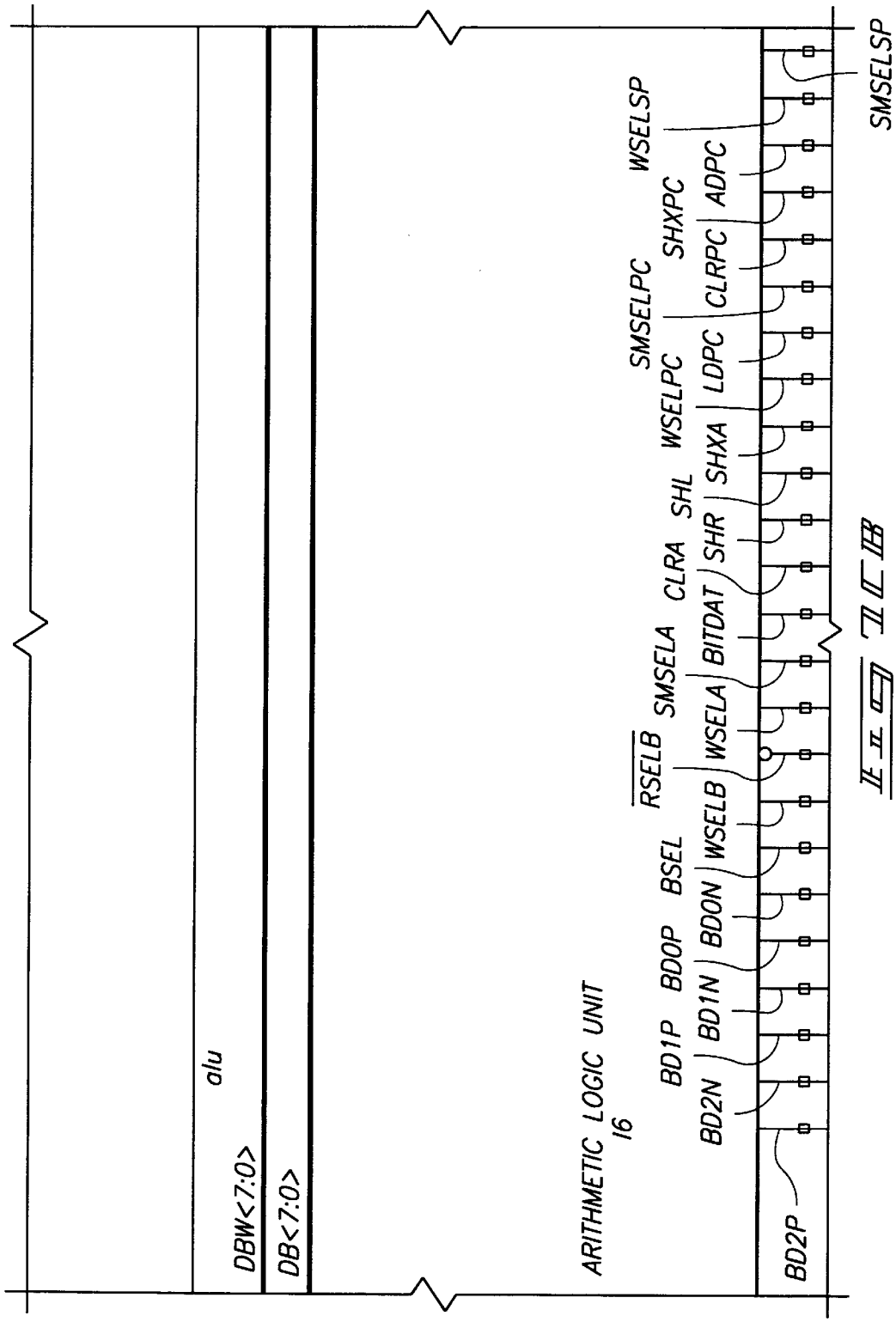
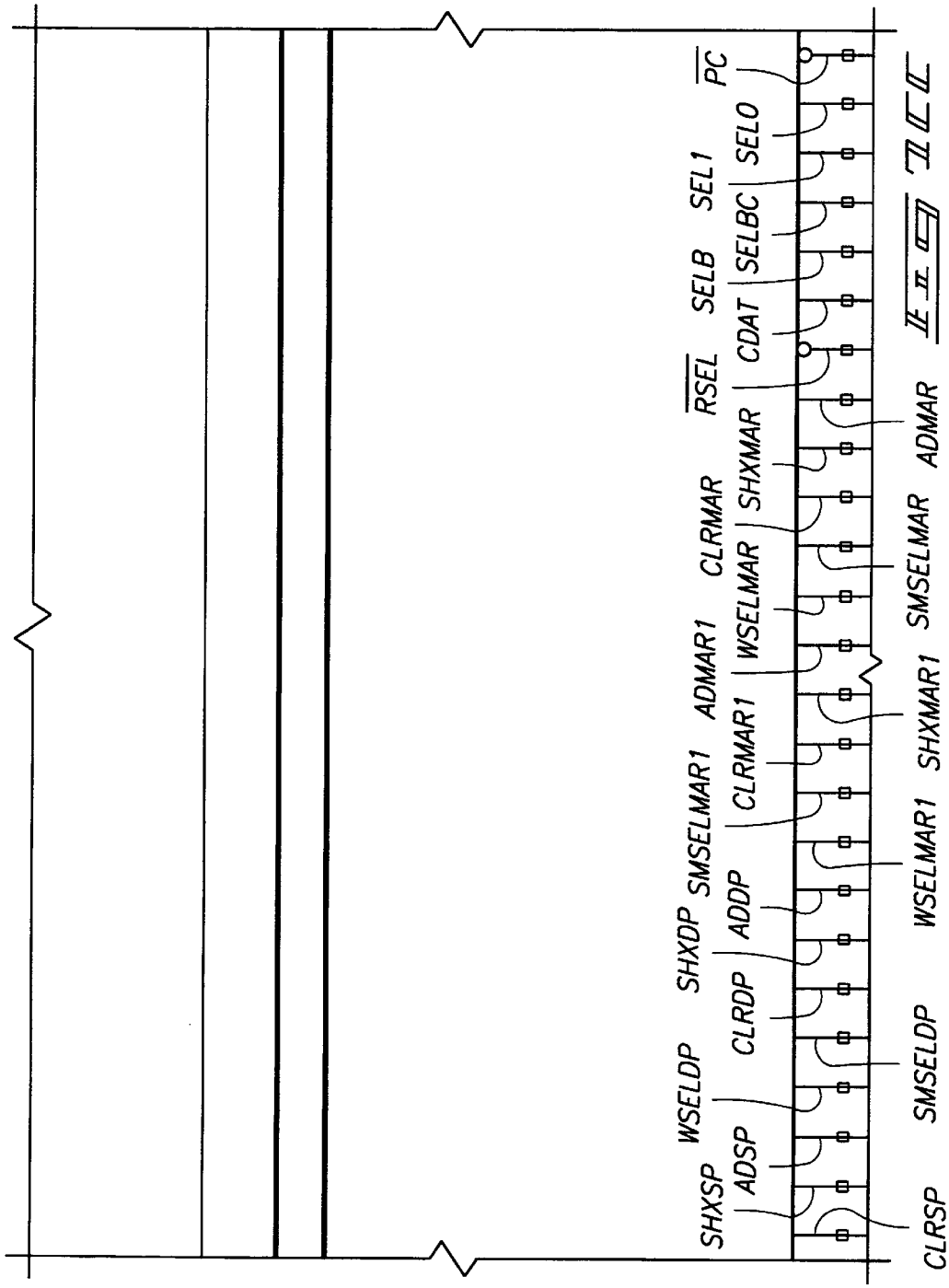
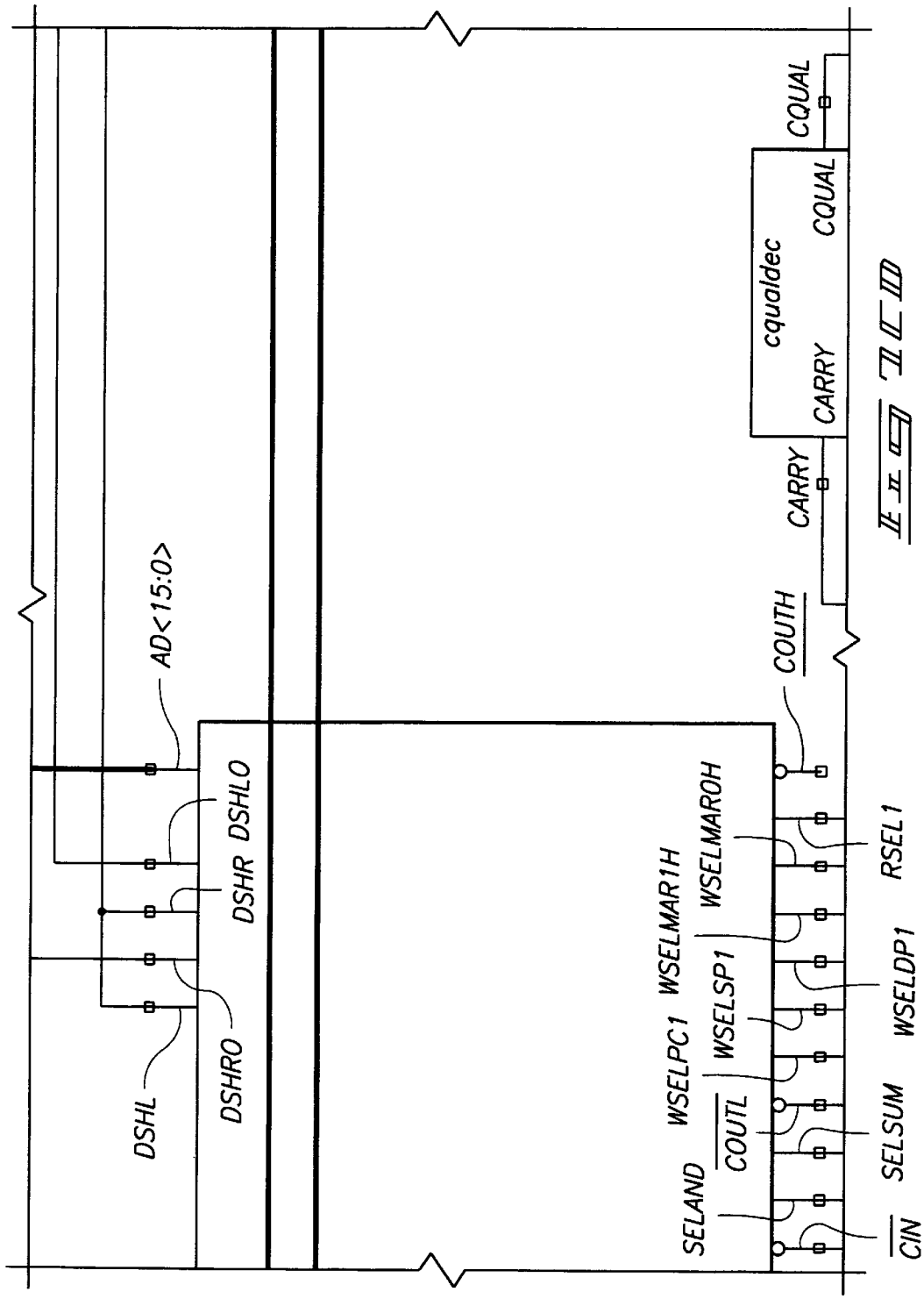
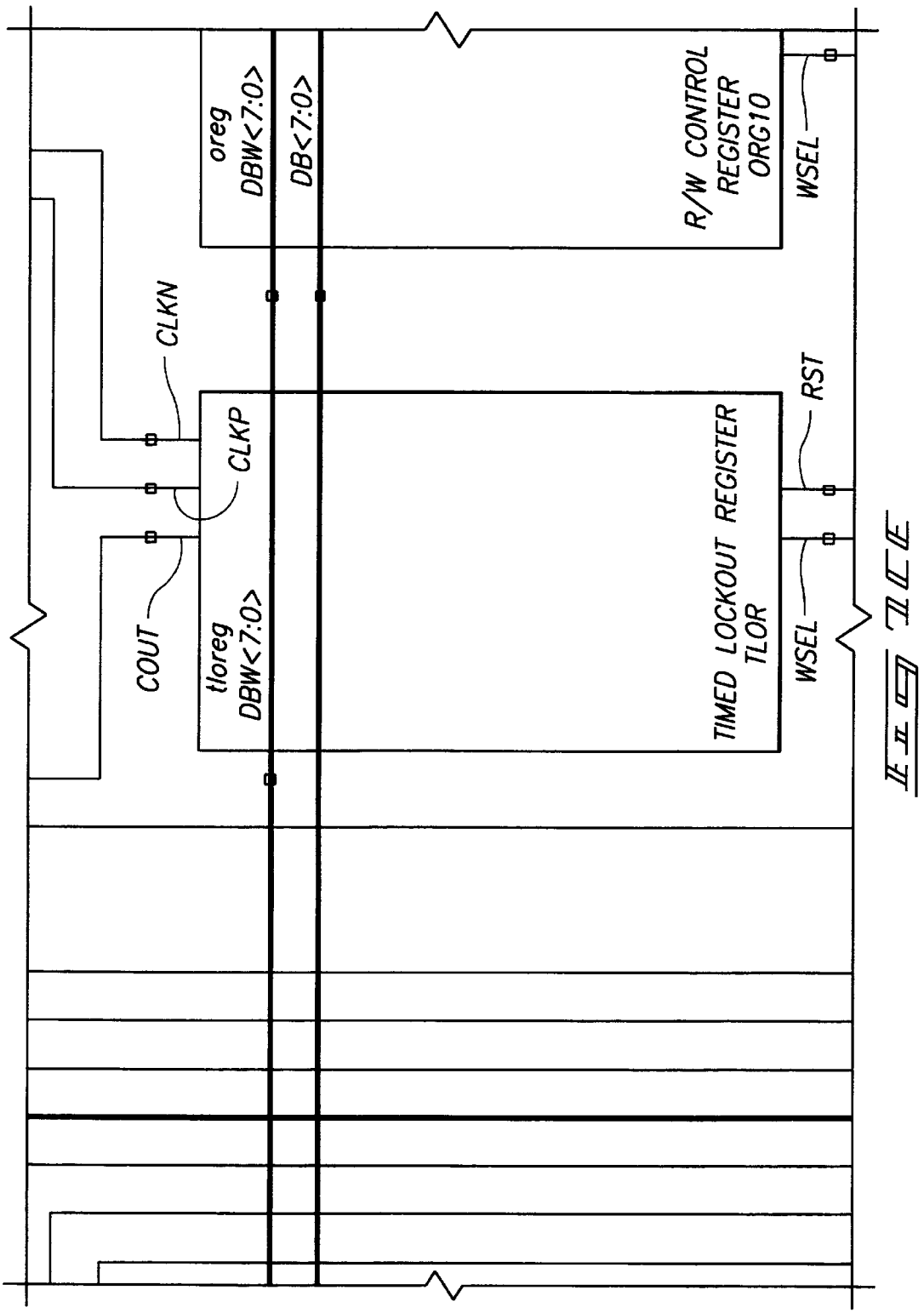
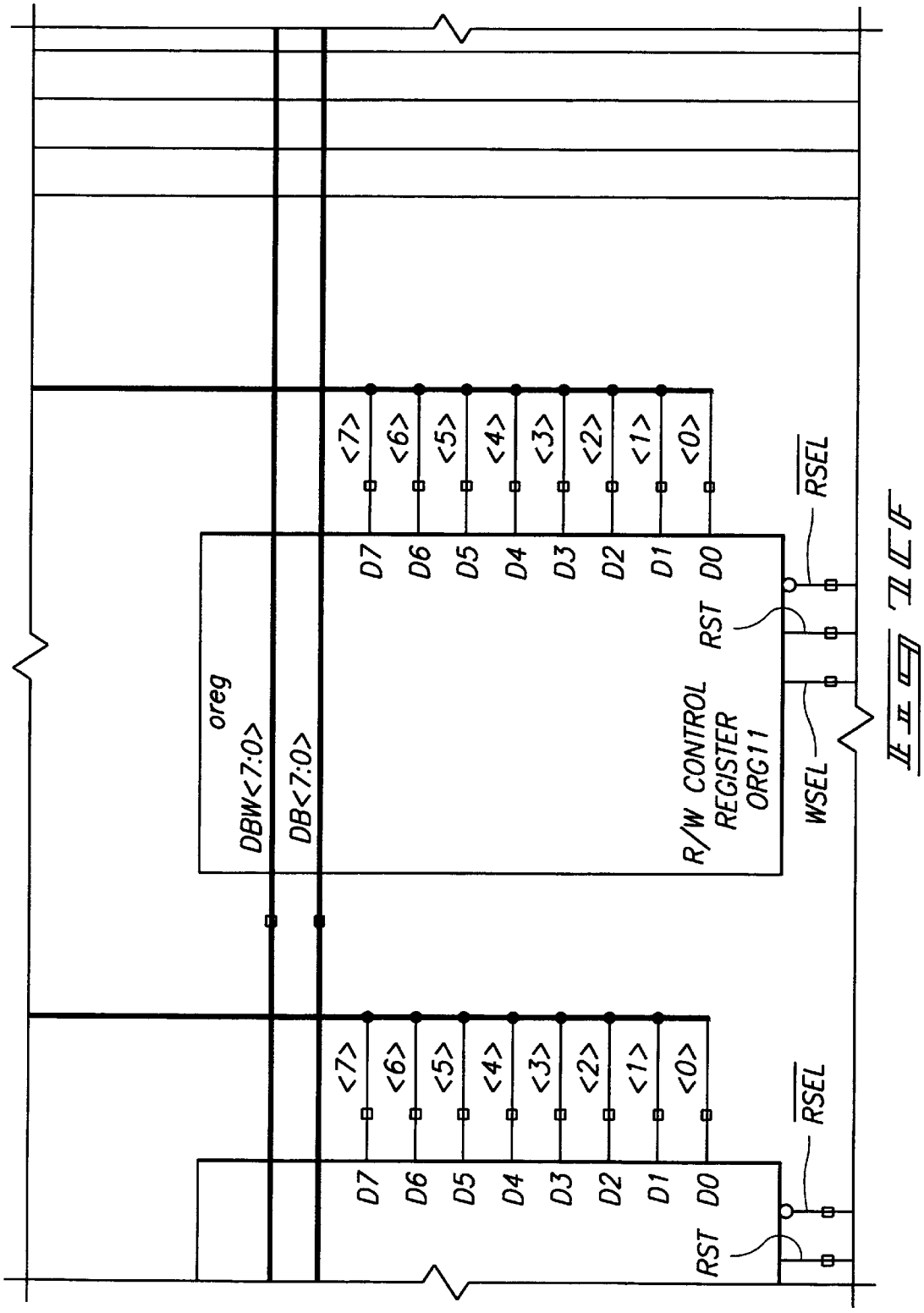

alu
DBW<7:0>
DB<7:0>
ARITHMETIC LOGIC UNIT
16
BD1P
BD2N
BDOP
BD1N
BSEL
BDON
RSELB
WSELB
SMSELA
WSELA
CLRA
BITDAT
SHL
SHR
WSELPC
SHXA
SMSELPC
LDPC
SHXPC
CLRPC
WSELSP
ADPC
SMSELSP
BD2P

FIG 11B


PC
SEL0
SEL1
SELB
SELBC
CDAT
RSEL
SHXMAR
CLRMAR
WSELMAR
ADMAR1
SMSELMAR
CLRMAR1
SHXMAR1
ADDP
WSELMAR1
CLRDP
SMSELDP
SHXDP
WSELDP
ADSP
CLRSP
SHXSP


AD<15:0>
DSHL
DSHRO
DSHR
DSHLO
COUTH
CARRY
cqualdec
CARRY
CQUAL
CQUAL
WSELPC1
WSELMAR1H
SELAND
COUTL
WSELSP1
WSELMAR0H
RSEL1
WSELDP1
SELSUM
CIN


oreg
DBW<7:0>
DB<7:0>
R/W CONTROL
REGISTER
ORG10
WSEL
CLKN
CLKP
RST
TIMED LOCKOUT REGISTER
TLOR
WSEL
COUT
tloreg
DBW<7:0>
FIG 11E


<7>
<6>
<5>
<4>
<3>
<2>
<1>
<0>
D7
D6
D5
D4
D3
D2
D1
D0
RSEL
RST
WSEL
R/W CONTROL REGISTER ORG11
oreg
DBW<7:0>
DB<7:0>
IF

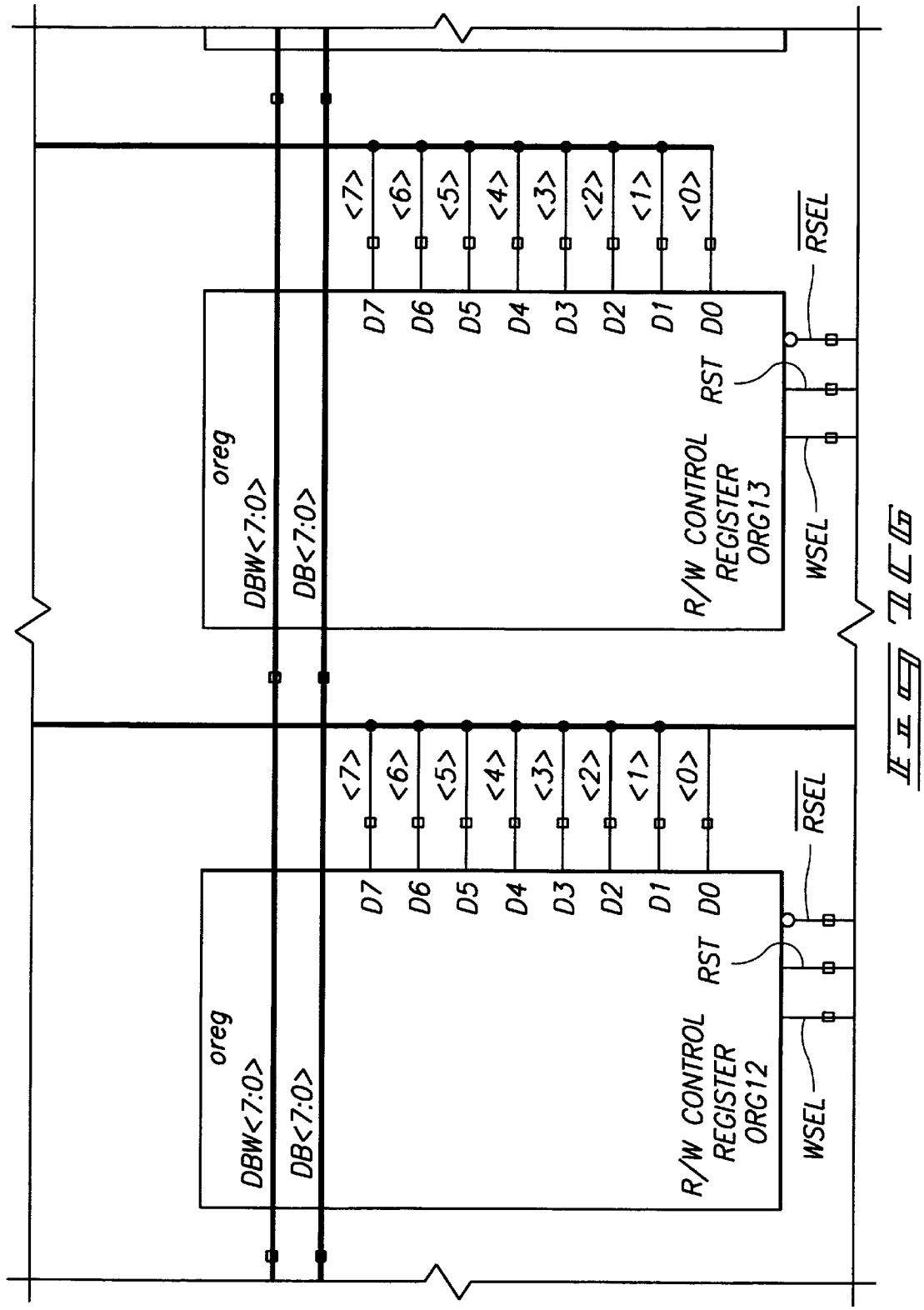

<7>
<6>
<5>
<4>
<3>
<2>
<1>
<0>
D7
D6
D5
D4
D3
D2
D1
D0
RSEL
RST
WSEL
R/W CONTROL REGISTER ORG13
oreg
DBW<7:0>
DB<7:0>
R/W CONTROL REGISTER ORG12

FIG. 85

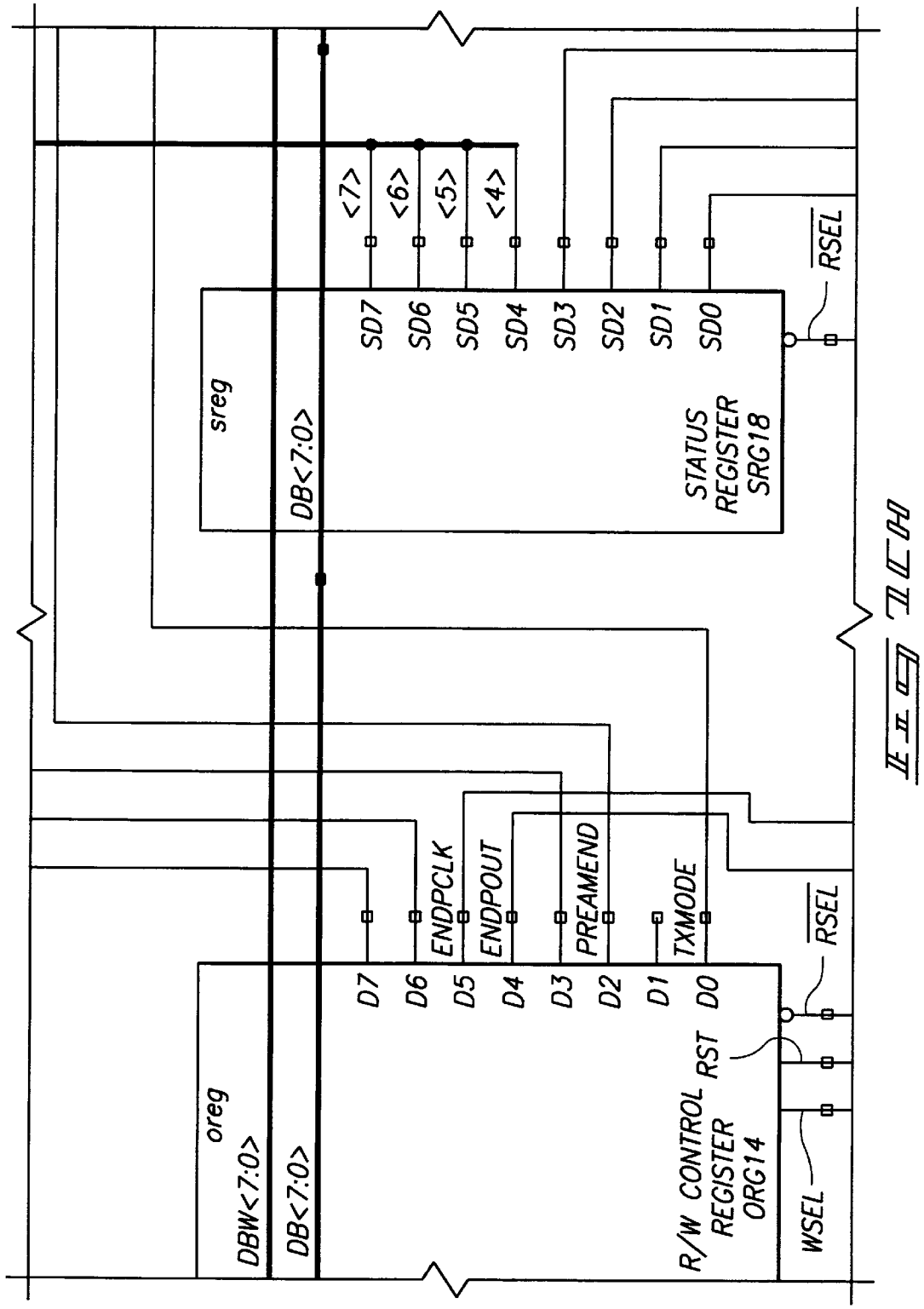


FIG 69
<7>
<6>
<5>
<4>
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
RSEL
sreg
DB<7:0>
STATUS REGISTER SRG18
D7
D6
D5
D4
D3
D2
D1
D0
ENDPCLK
ENDPOUT
PREAMEND
TXMODE
RSEL
RST
WSEL
oreg
DBW<7:0>
DB<7:0>
R/W CONTROL REGISTER ORG14

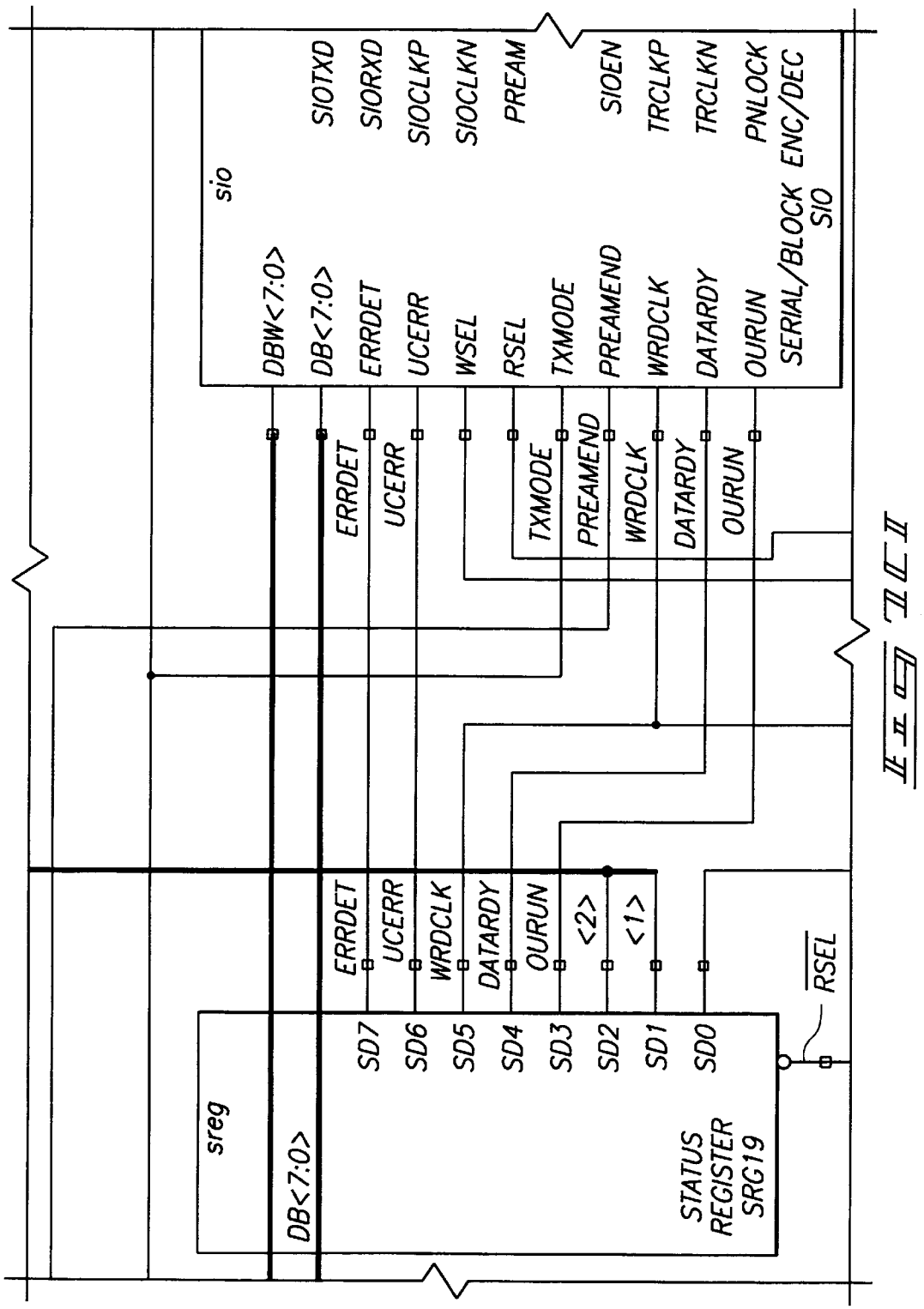

sio
SIOTXD
SIORXD
SIOCLKP
SIOCLKN
PREAM
SIOEN
TRCLKP
TRCLKN
PNLOCK
ENC/DEC
SIO
DBW<7:0>
DB<7:0>
ERRDET
UCERR
WSEL
RSEL
TXMODE
PREAMEND
WRDCLK
DATARDY
OURUN
SERIAL/BLOCK
sreg
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
<2>
<1>
STATUS REGISTER SRG19
RSEL

FIG. 11

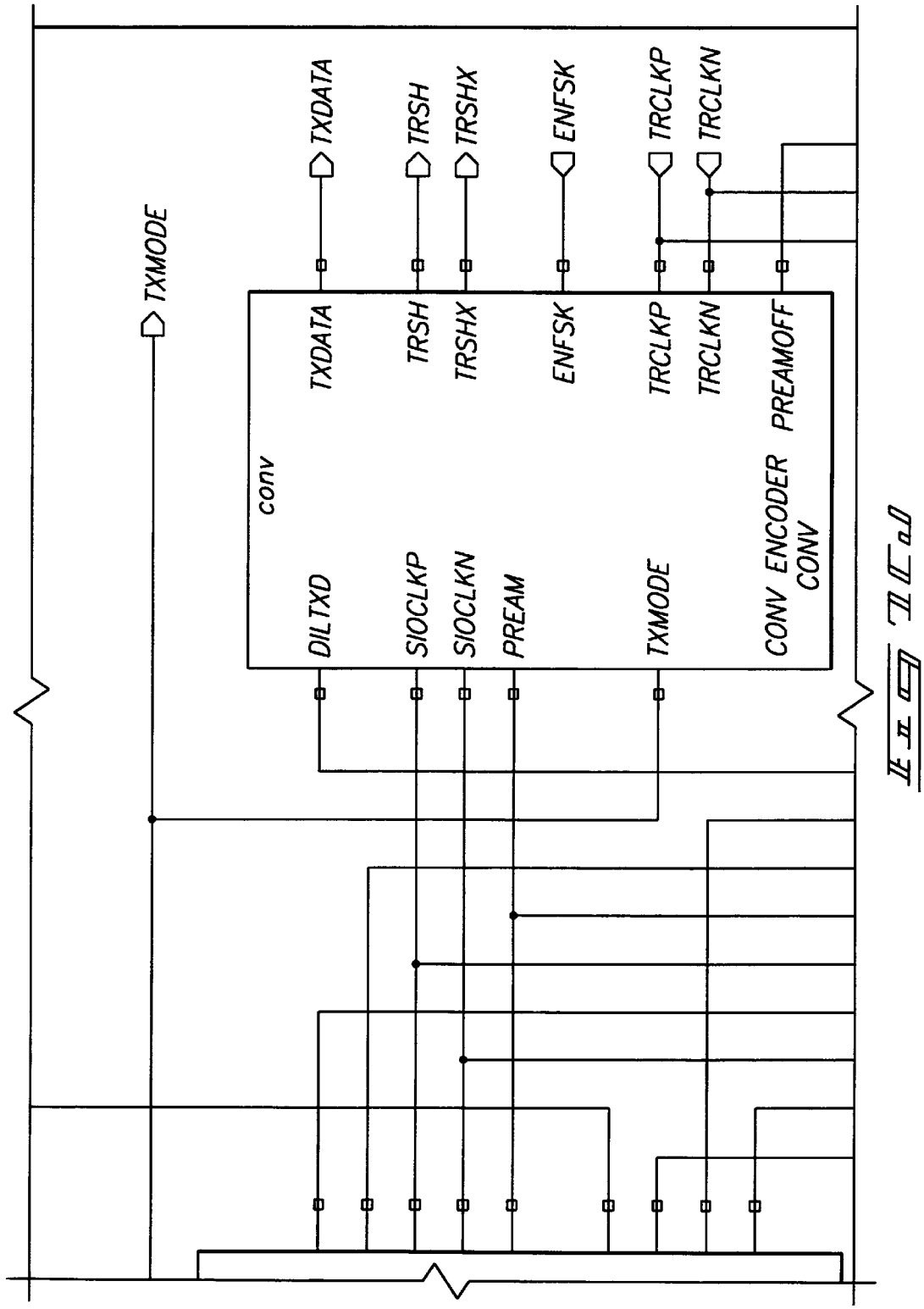
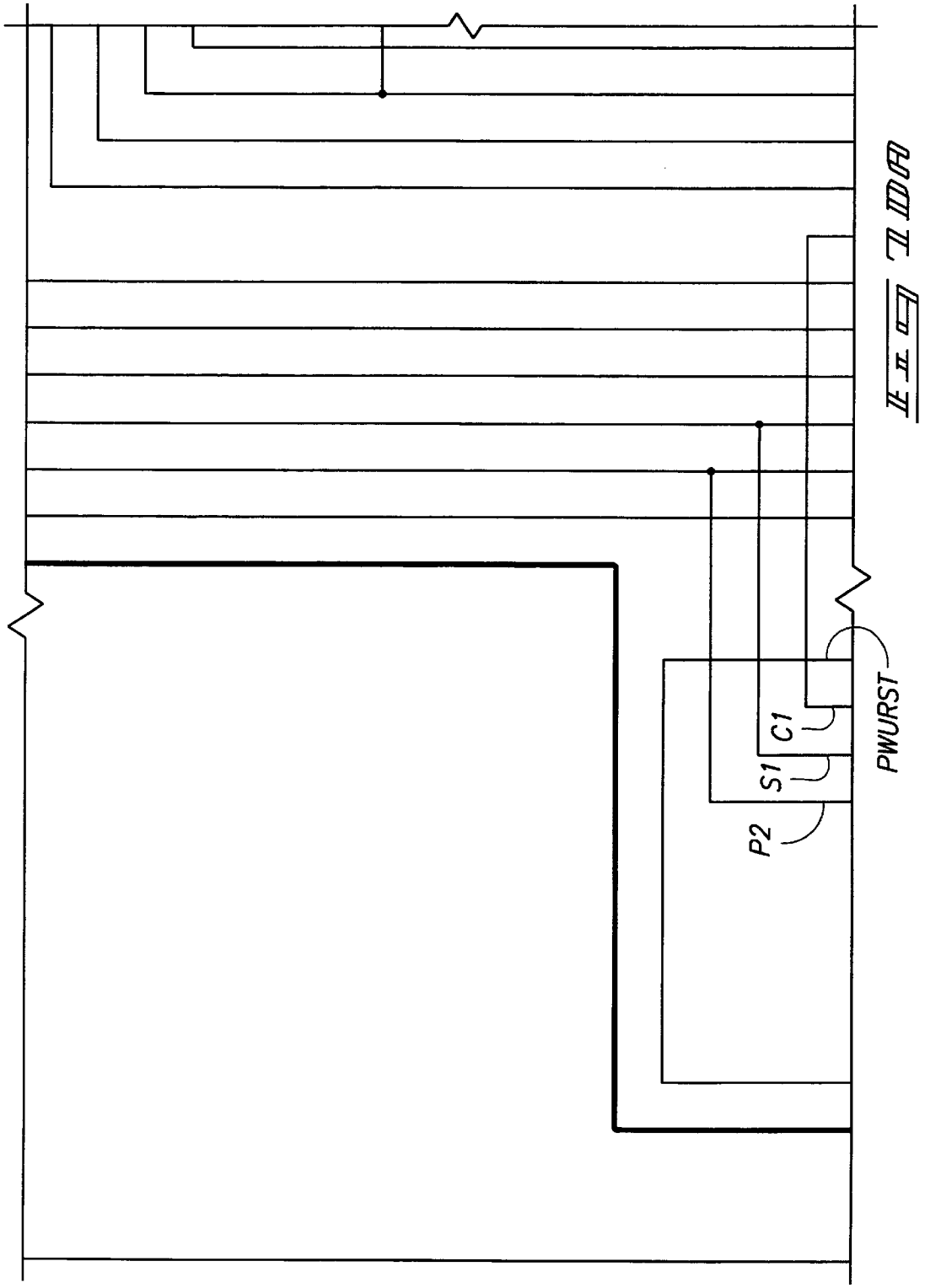

TXMODE
TXDATA
TRSH
TRSHX
ENFSK
TRCLKP
TRCLKN
conv
TXDATA
TRSH
TRSHX
ENFSK
TRCLKP
TRCLKN
PREAMOFF
DILTXD
SIOCLKP
SIOCLKN
PREAM
TXMODE
CONV ENCODER
CONV

FIG 83


PWURST
C1
S1
P2

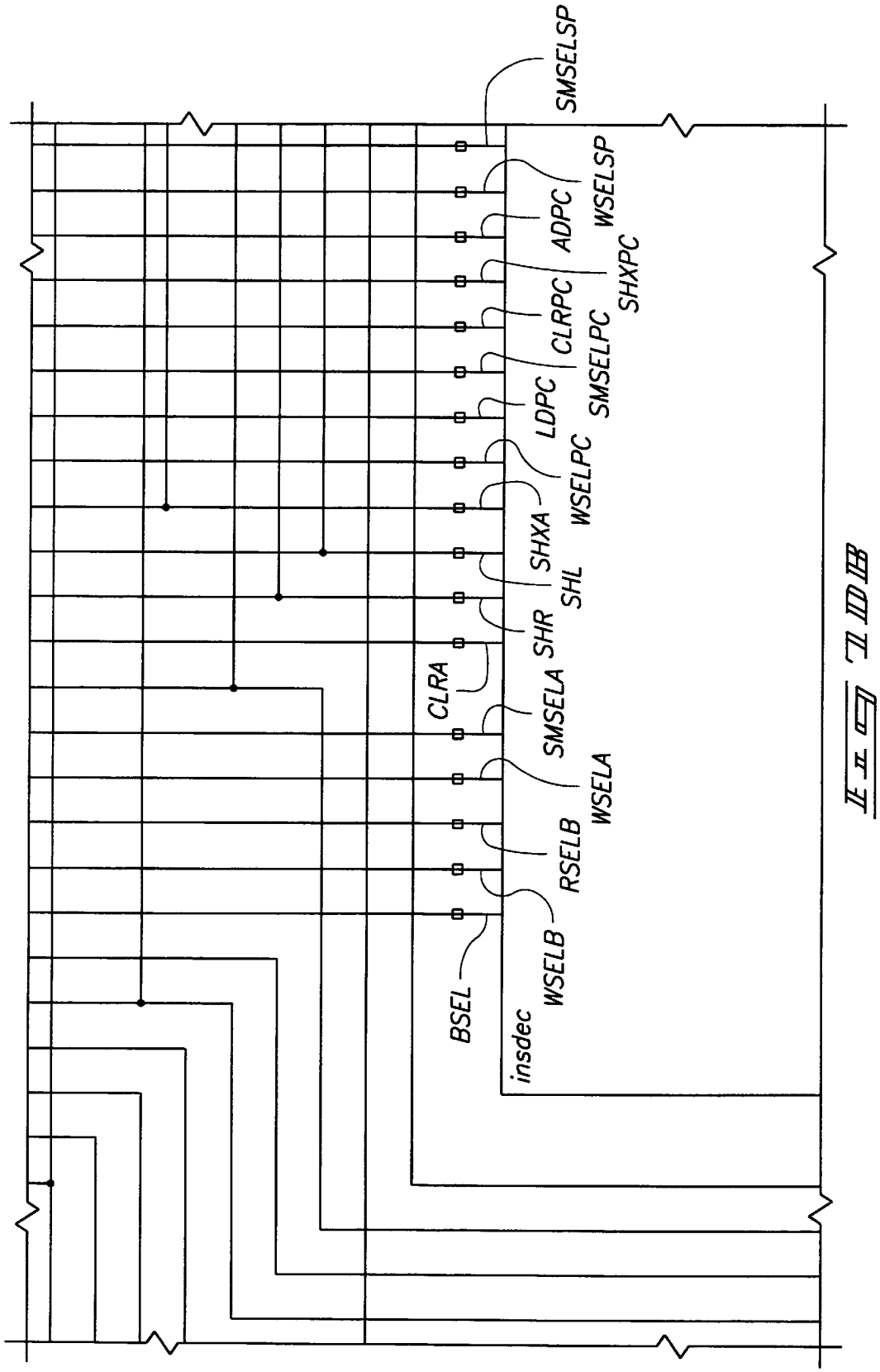

SMSELSP
WSELSP
ADPC
SHXPC
CLRPC
SMSELPC
LDPC
WSELPC
SHXA
SHL
SHR
SMSELA
CLRA
WSELA
RSELB
WSELB
BSEL
insdec

FIG. 85

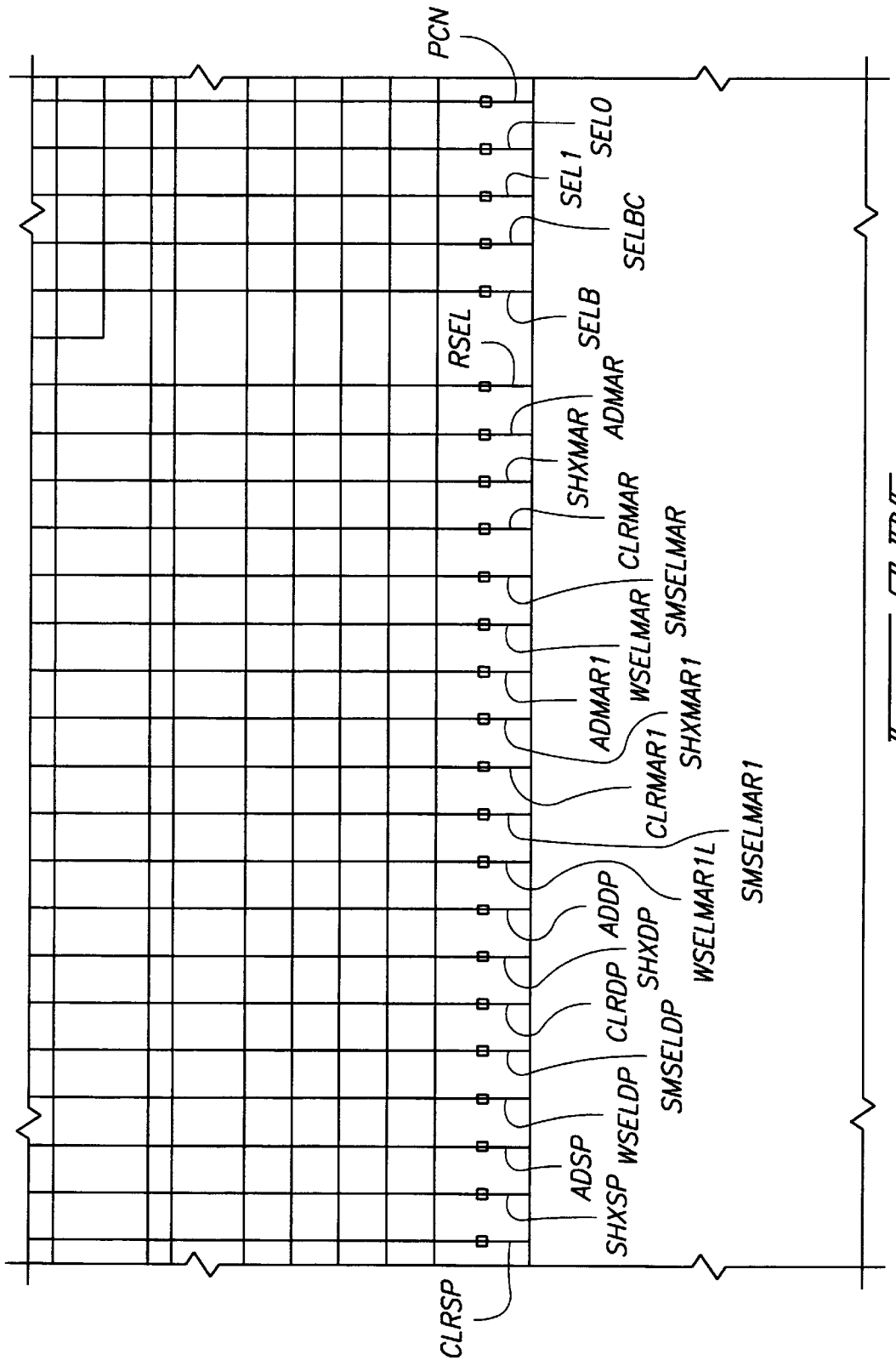

PCN
SEL0
SEL1
SELBC
SELB
RSEL
ADMAR
SHXMAR
CLRMAR
SMSELMAR
WSELMAR
ADMAR1
SHXMAR1
CLRMAR1
SMSELMAR1
WSELMAR1L
ADDP
SHXDP
CLRDP
SMSELDP
WSELDP
ADSP
SHXSP
CLRSP

FIG. 11DL

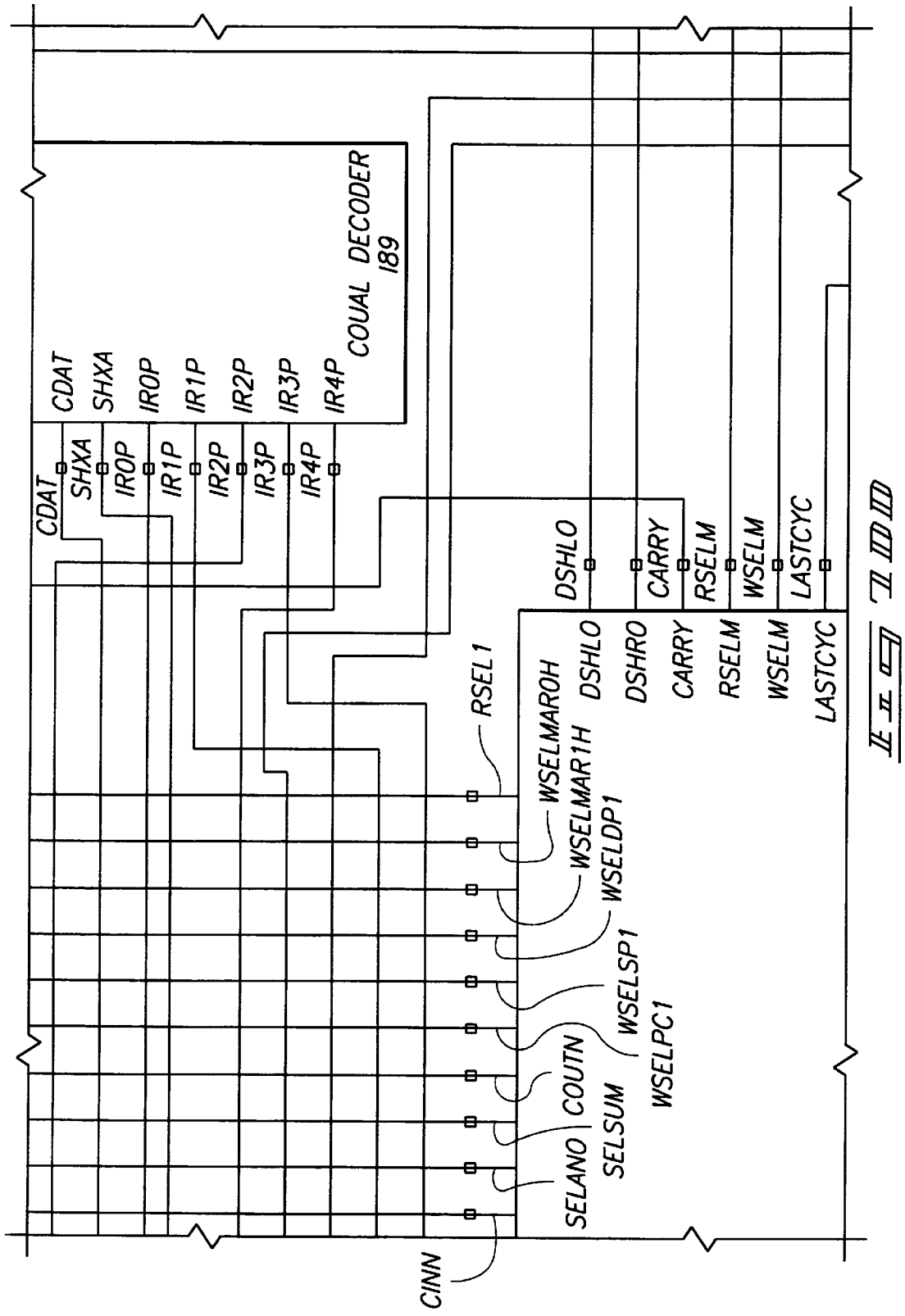

COUAL DECODER
189
CDAT
SHXA
IR0P
IR1P
IR2P
IR3P
IR4P
DSHLO
CARRY
RSELM
WSELM
LASTCYC
RSEL1
WSELMAR0H
WSELMAR1H
WSELDP1
WSELSP1
WSELPC1
COUTN
SELSUM
SELANO
CINN

FIG 89

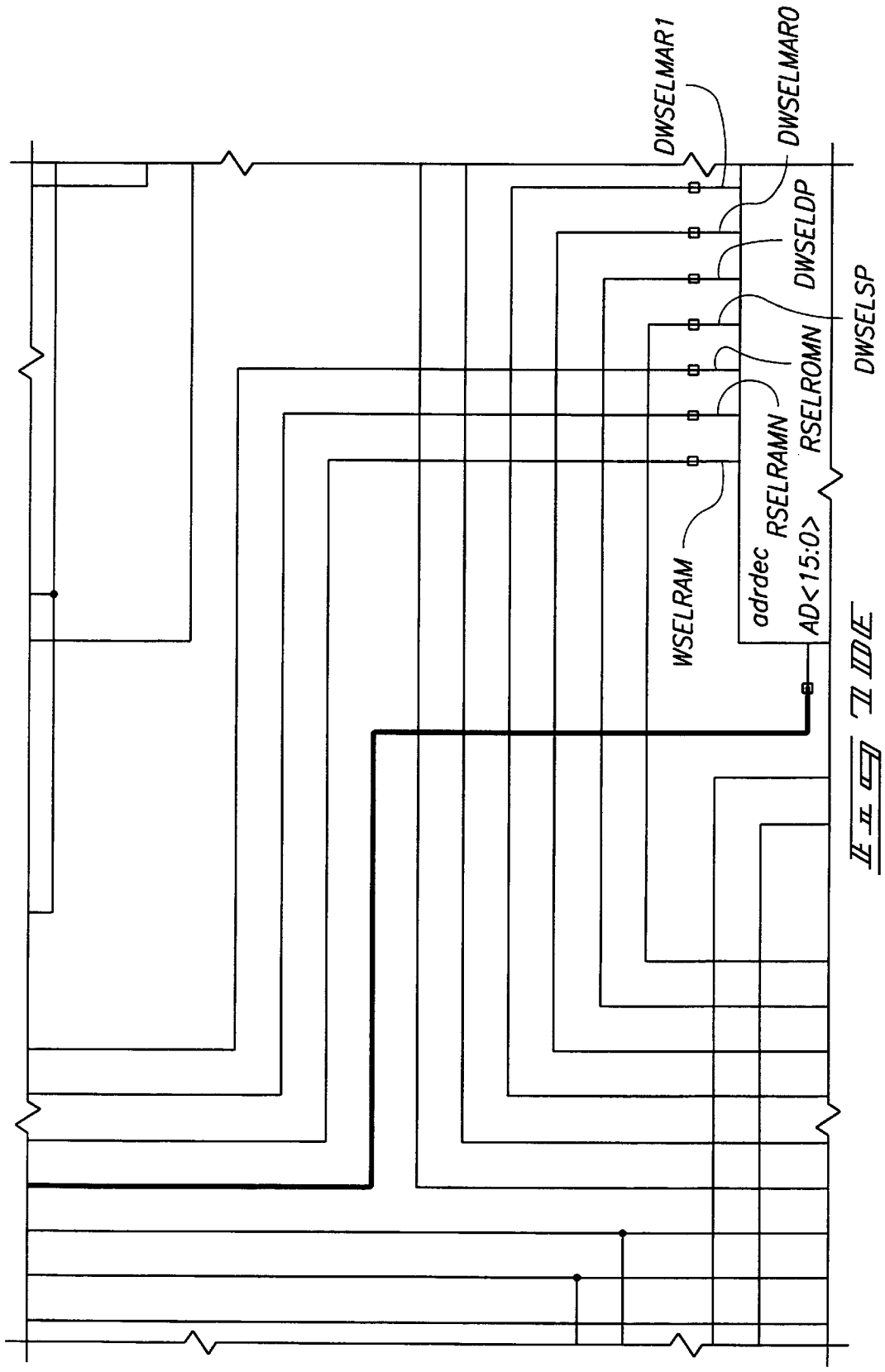

DWSELMAR1
DWSELMAR0
DWSELDP
DWSELSP
RSELROMN
RSELRAMN
adrdec
AD<15:0>
WSELRAM

FIG. 88

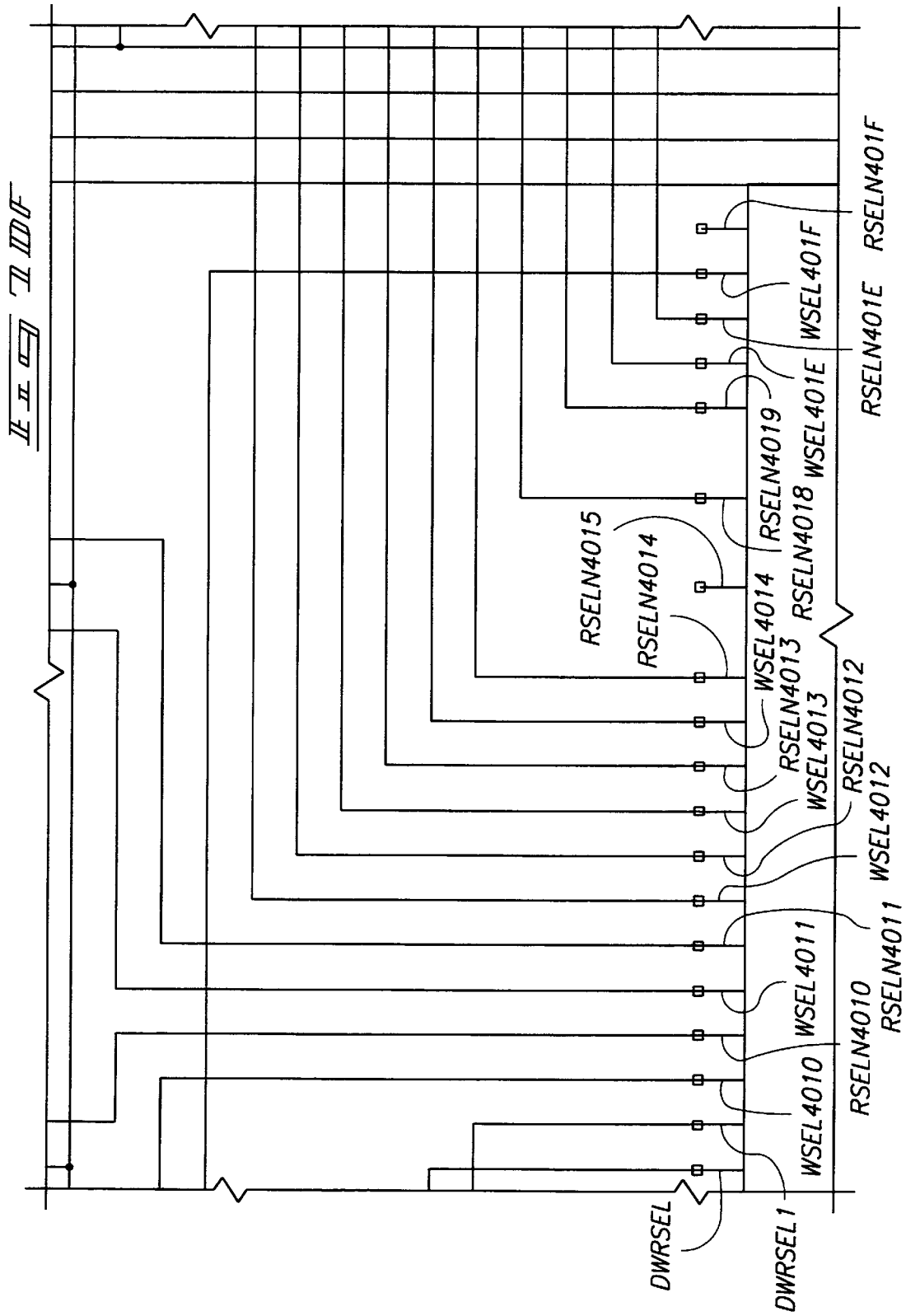


FIG 1DF
RSELN401F
WSEL401F
RSELN401E
WSEL401E
RSELN4019
RSELN4018
RSELN4015
RSELN4014
WSEL4014
WSEL4013
RSELN4013
RSELN4012
WSEL4012
WSEL4011
RSELN4011
RSELN4010
WSEL4010
DWRSEL
DWRSEL1

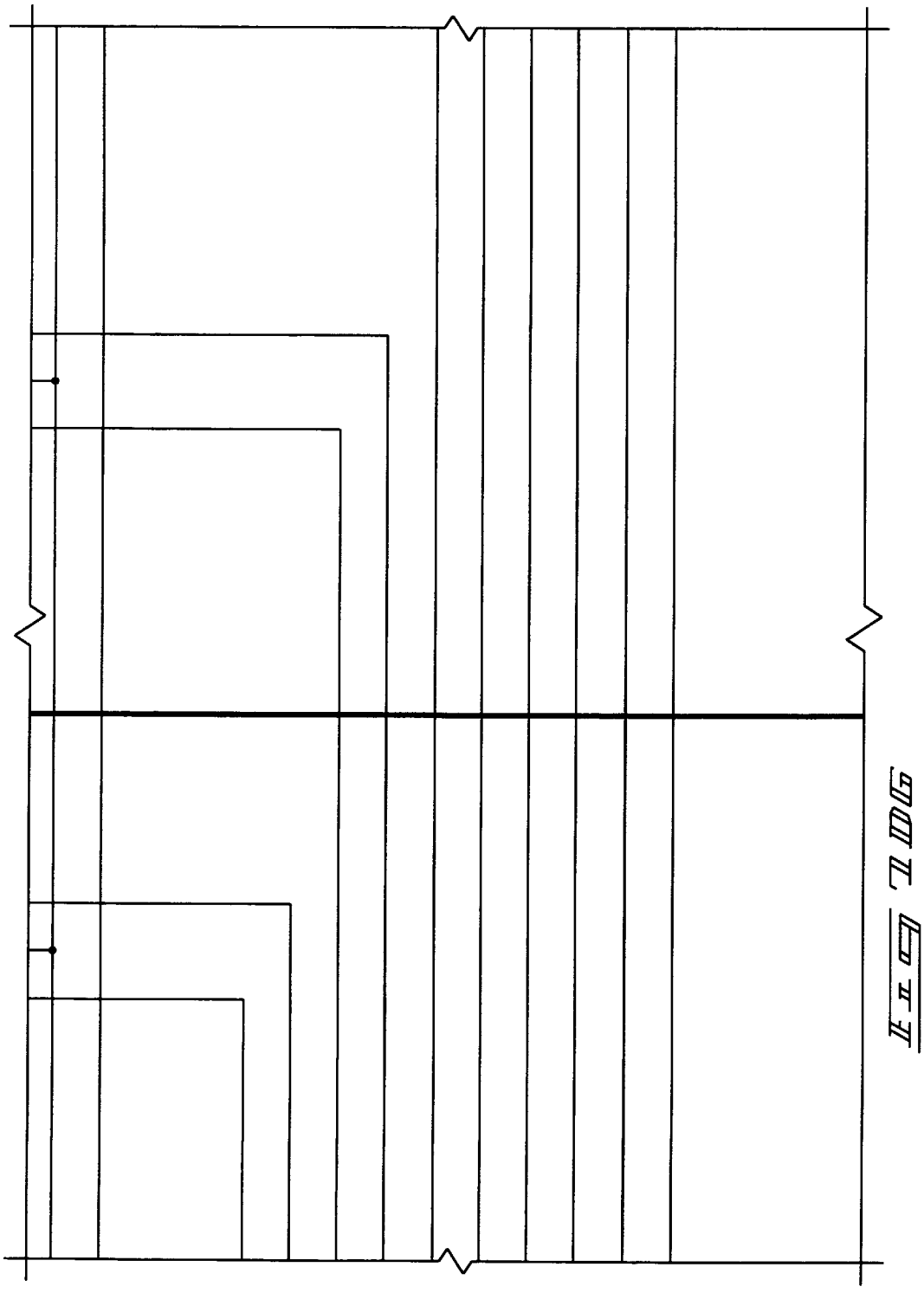


FIG. 90L

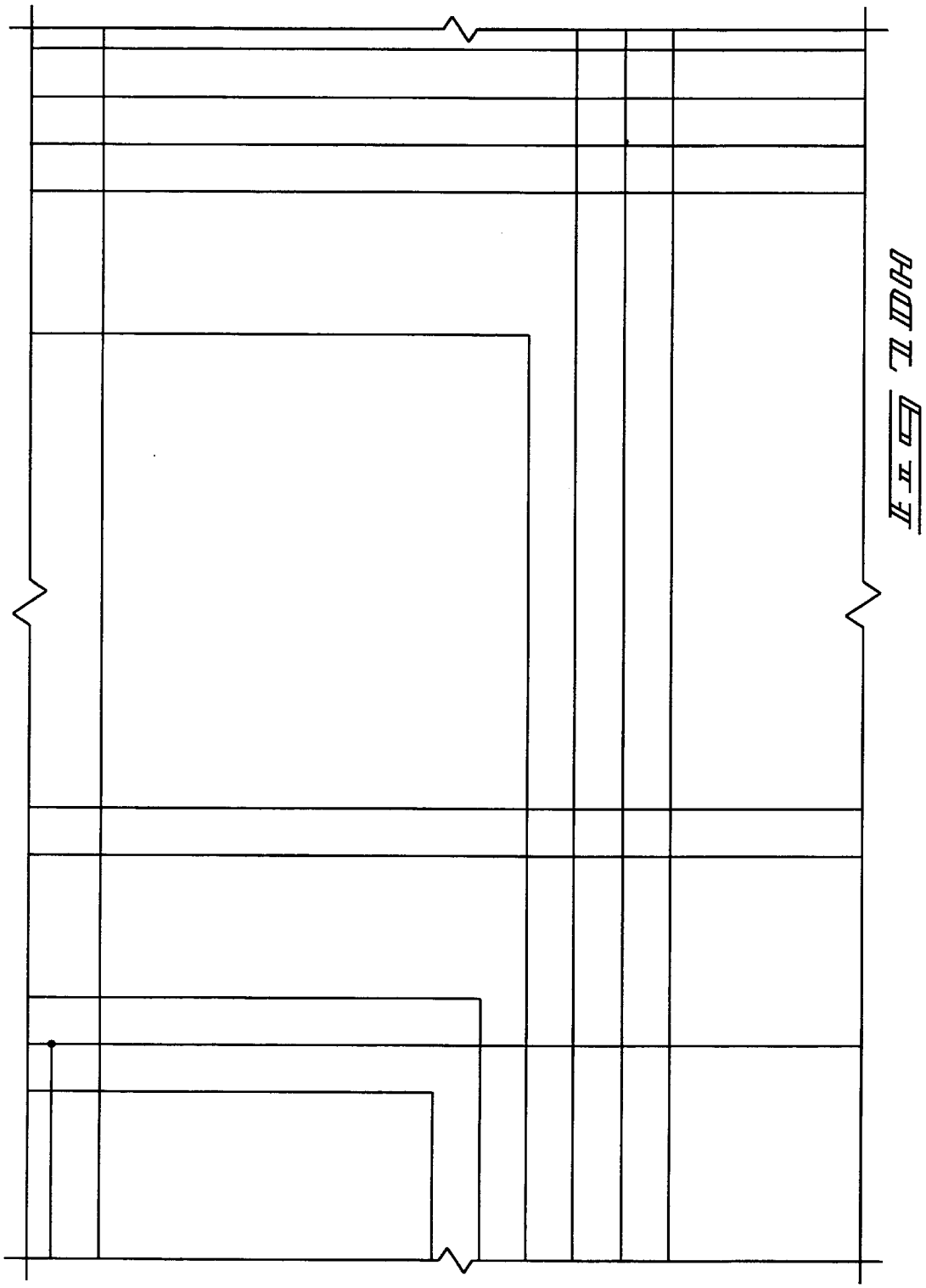


FIG. 91

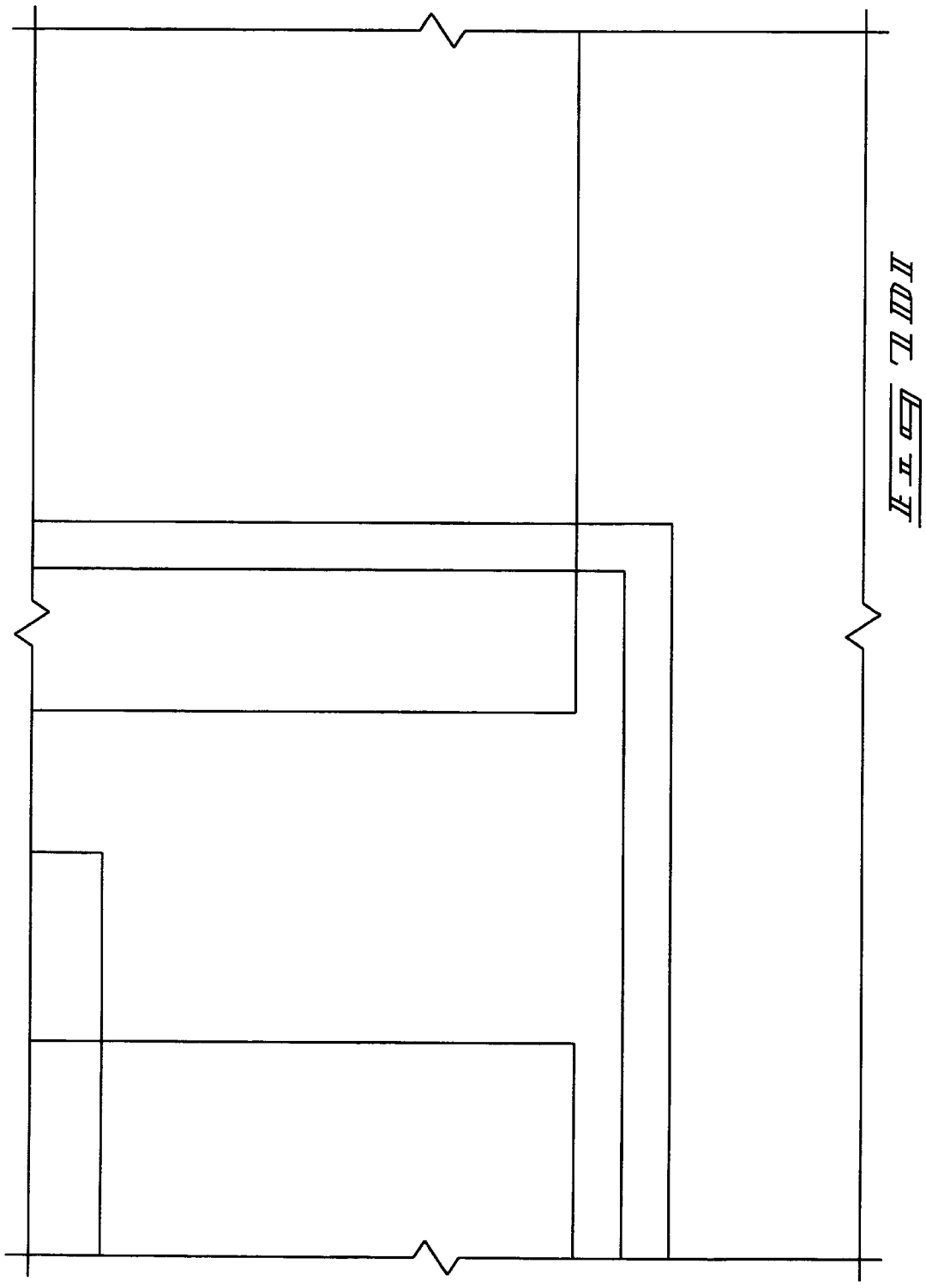
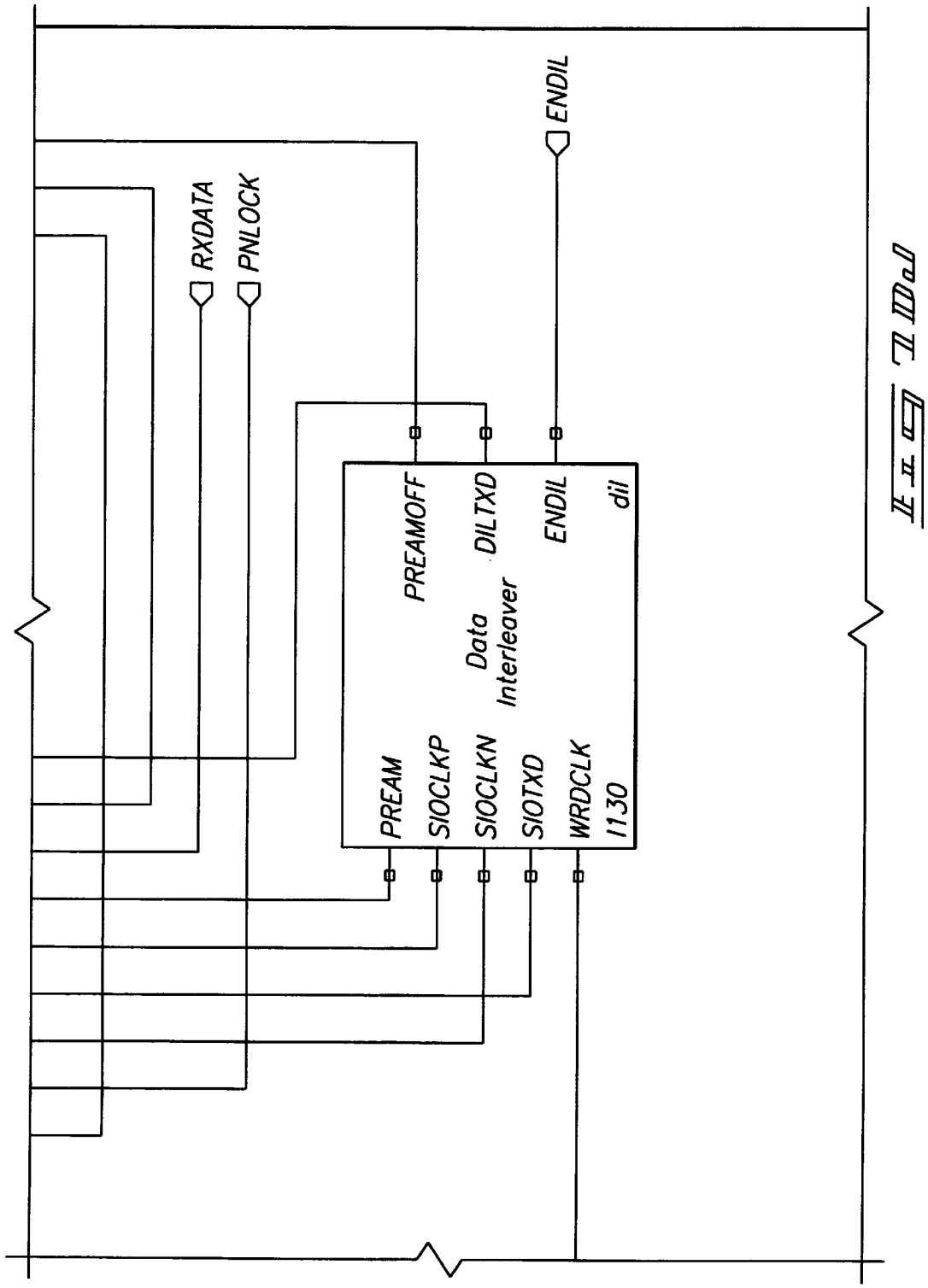


FIG 92


ENDIL
RXDATA
PNLOCK
PREAMOFF
DILTXD
ENDIL
dil
Data Interleaver
PREAM
SIOCLKP
SIOCLKN
SIOTXD
WRDCLK
1130

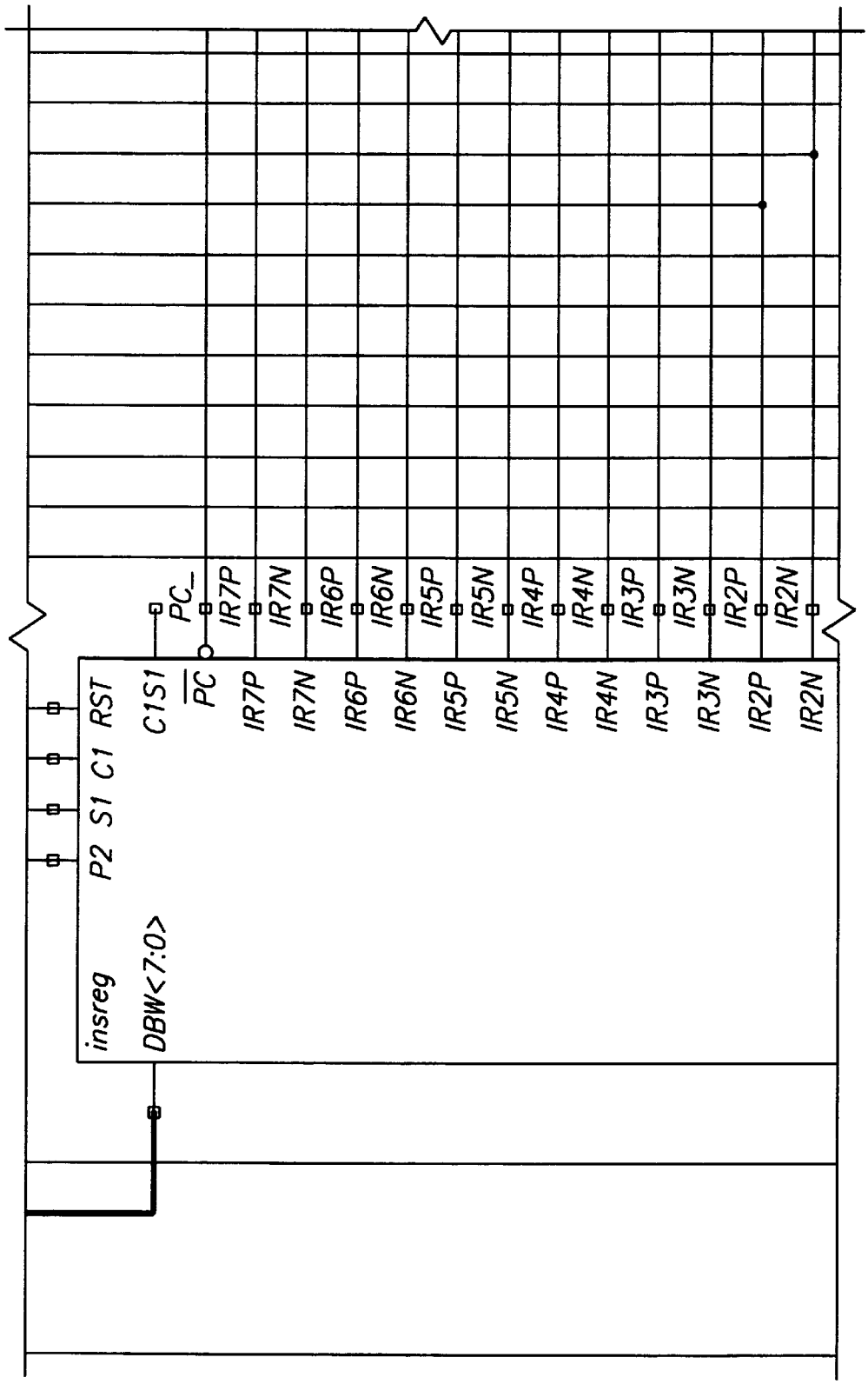

insreg
DBW<7:0>
P2 S1 C1 RST
C1S1
PC
PC_
IR7P
IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
IR4N
IR3P
IR3N
IR2P
IR2N

FIG 11E

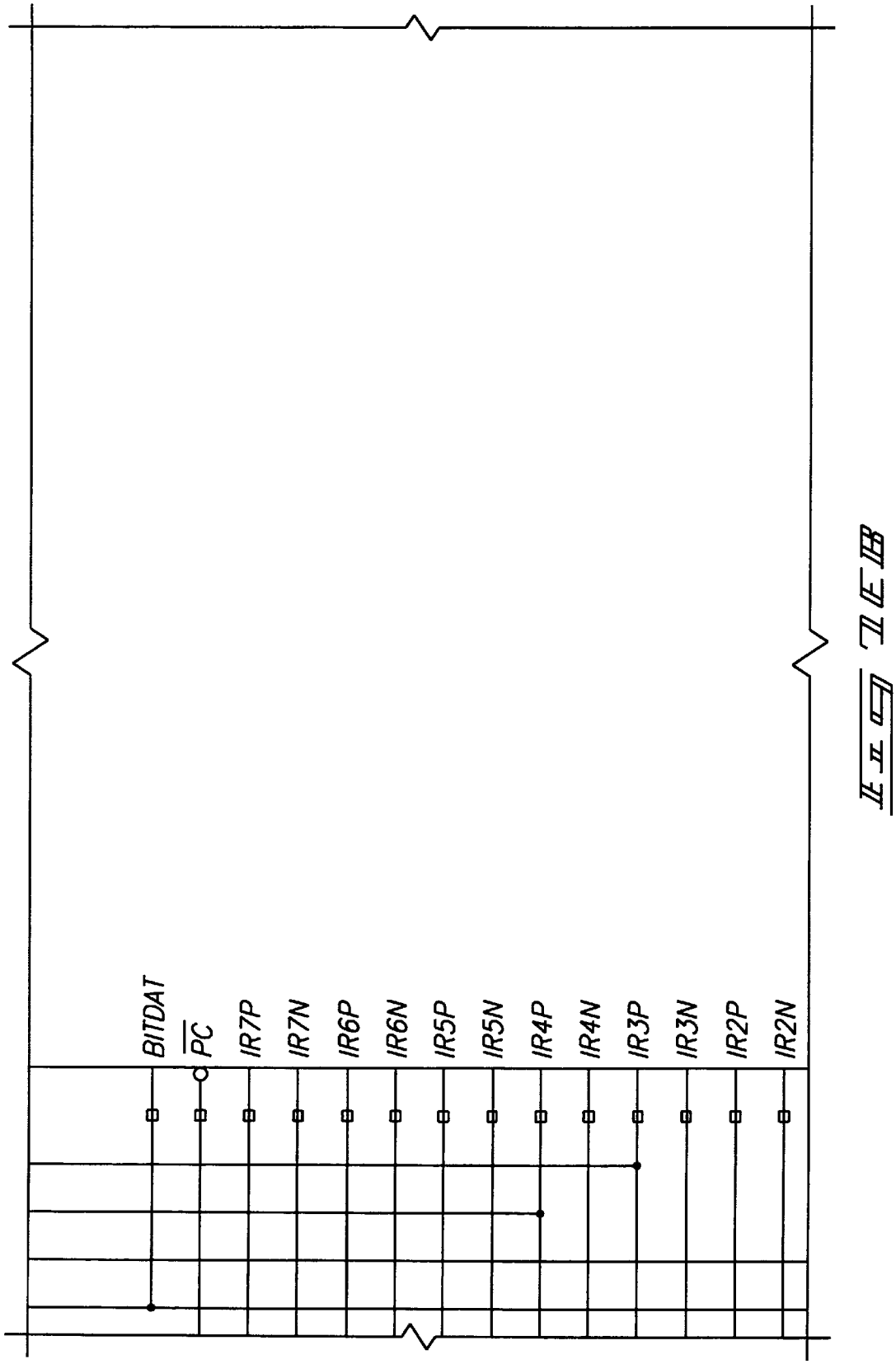

BITDAT
PC
IR7P
IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
IR4N
IR3P
IR3N
IR2P
IR2N

FIG 3IL

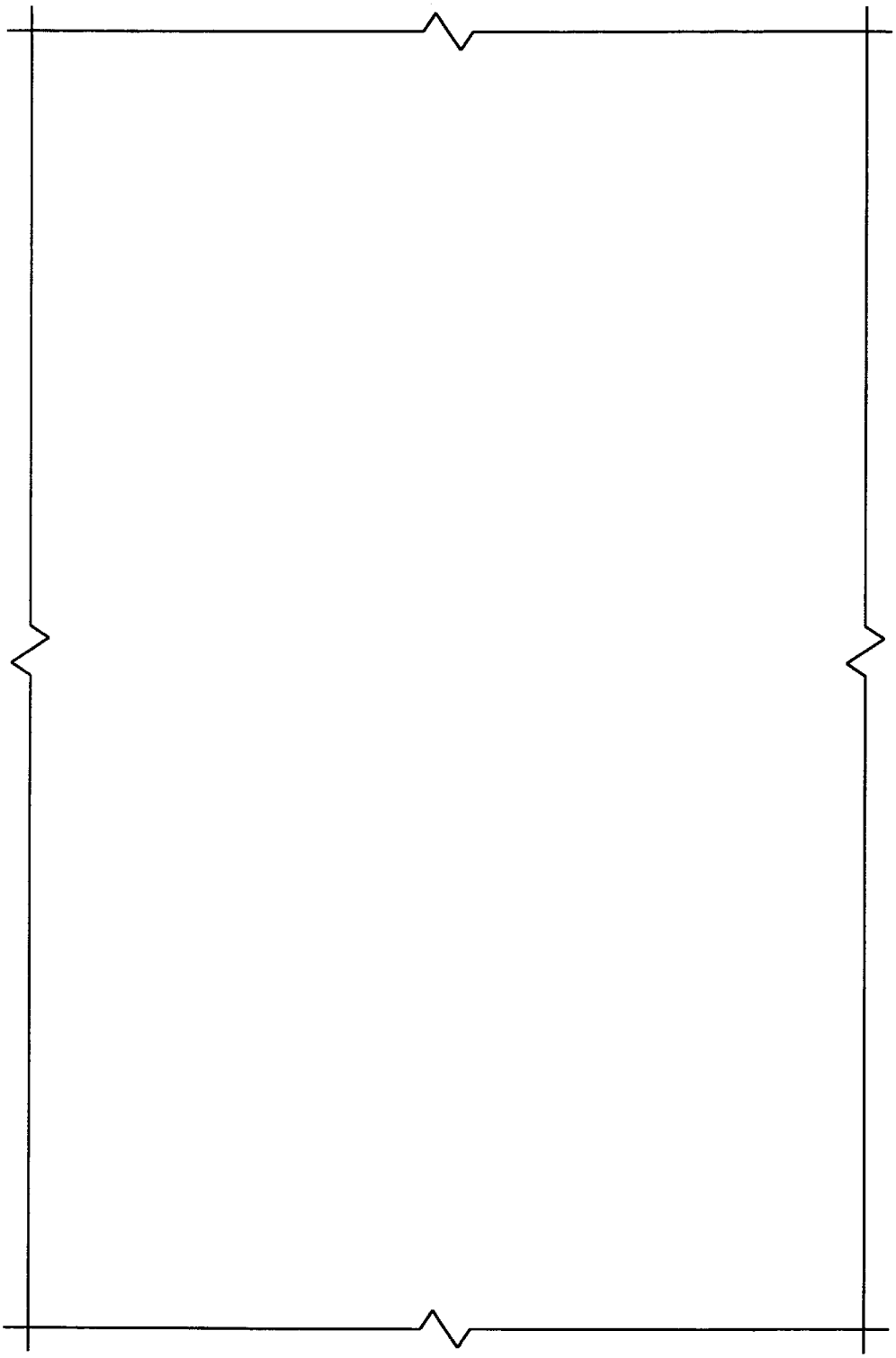
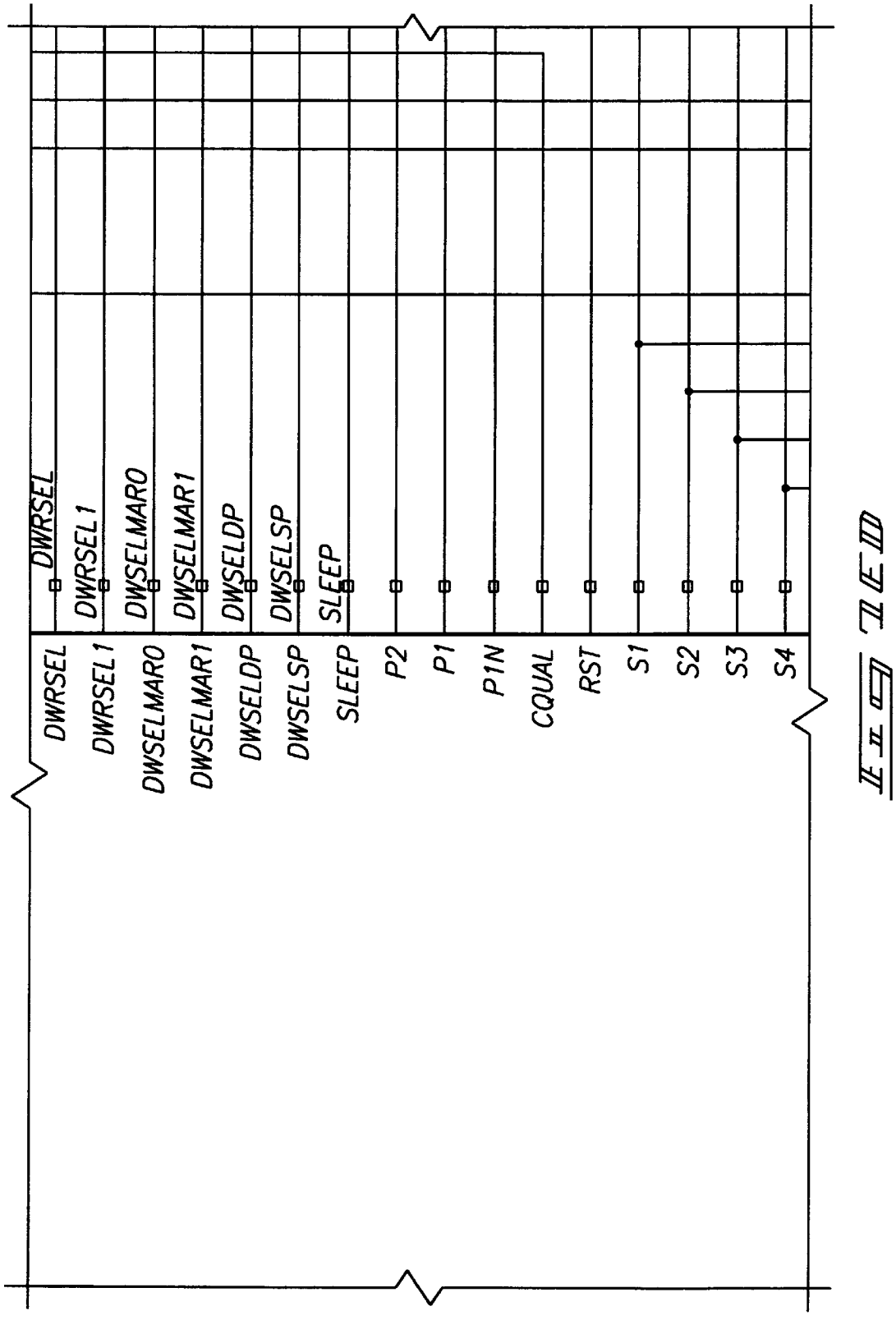


FIG. 95E


DWRSEL
DWRSEL1
DWSELMAR0
DWSELMAR1
DWSELDP
DWSELSP
SLEEP
P2
P1
P1N
CQUAL
RST
S1
S2
S3
S4
FIG. 97

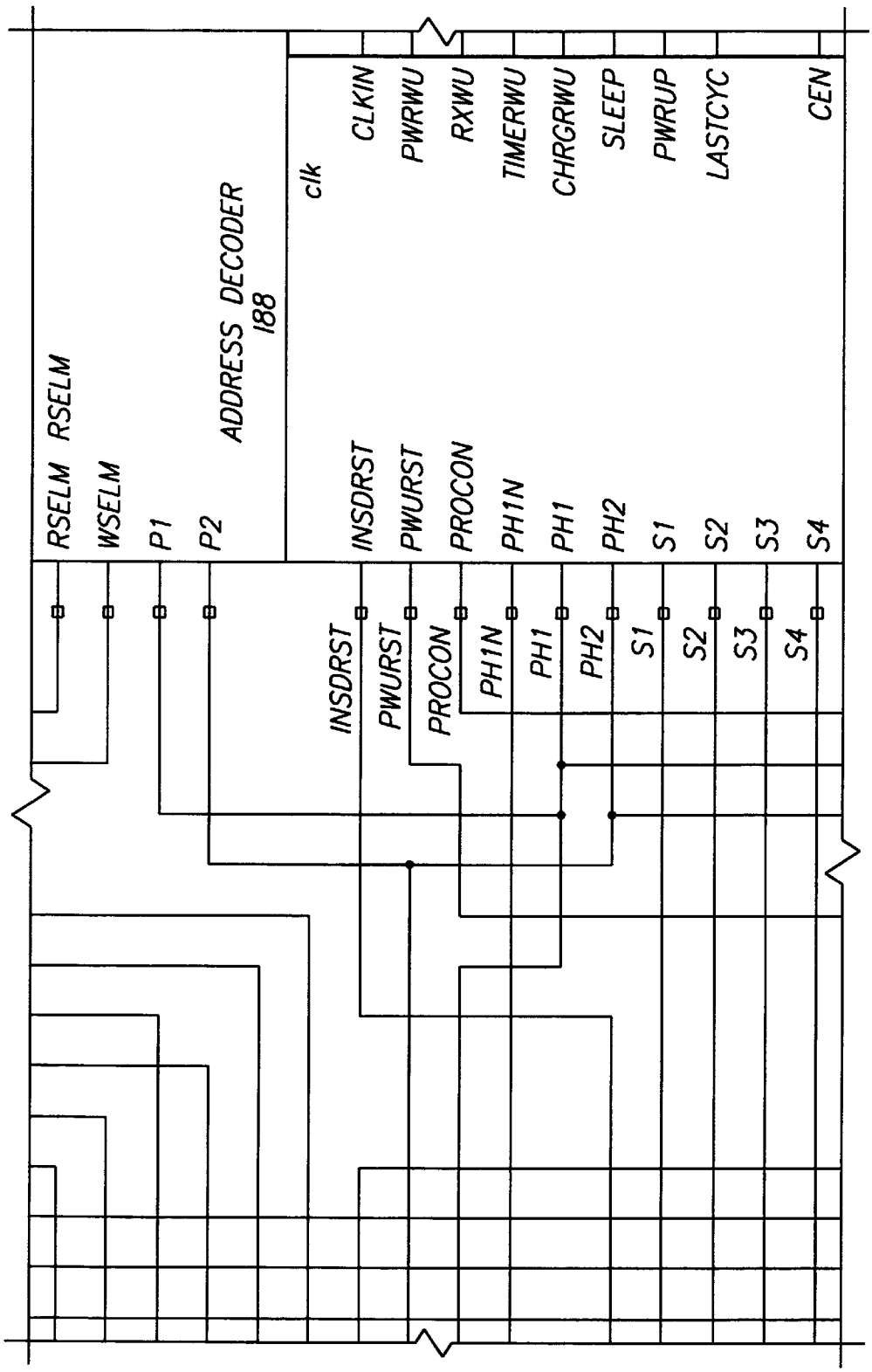
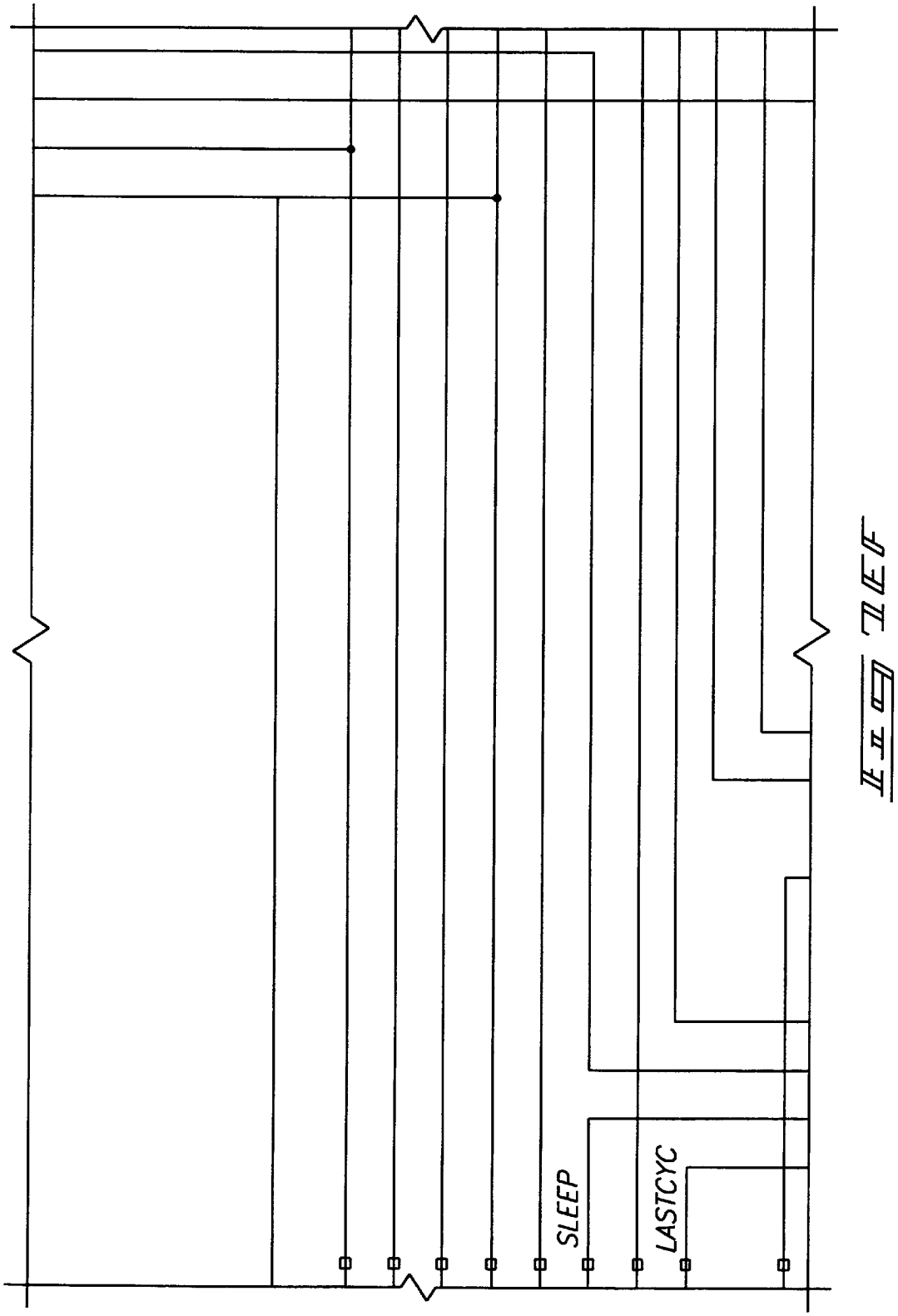

RSELM
WSELM
P1
P2
ADDRESS DECODER
188
clk
CLKIN
PWRWU
RXWU
TIMERWU
CHRGRWU
SLEEP
PWRUP
LASTCYC
CEN
INSDRST
PWURST
PROCON
PH1N
PH1
PH2
S1
S2
S3
S4

FIG 11E


SLEEP
LASTCYC
SLEEP

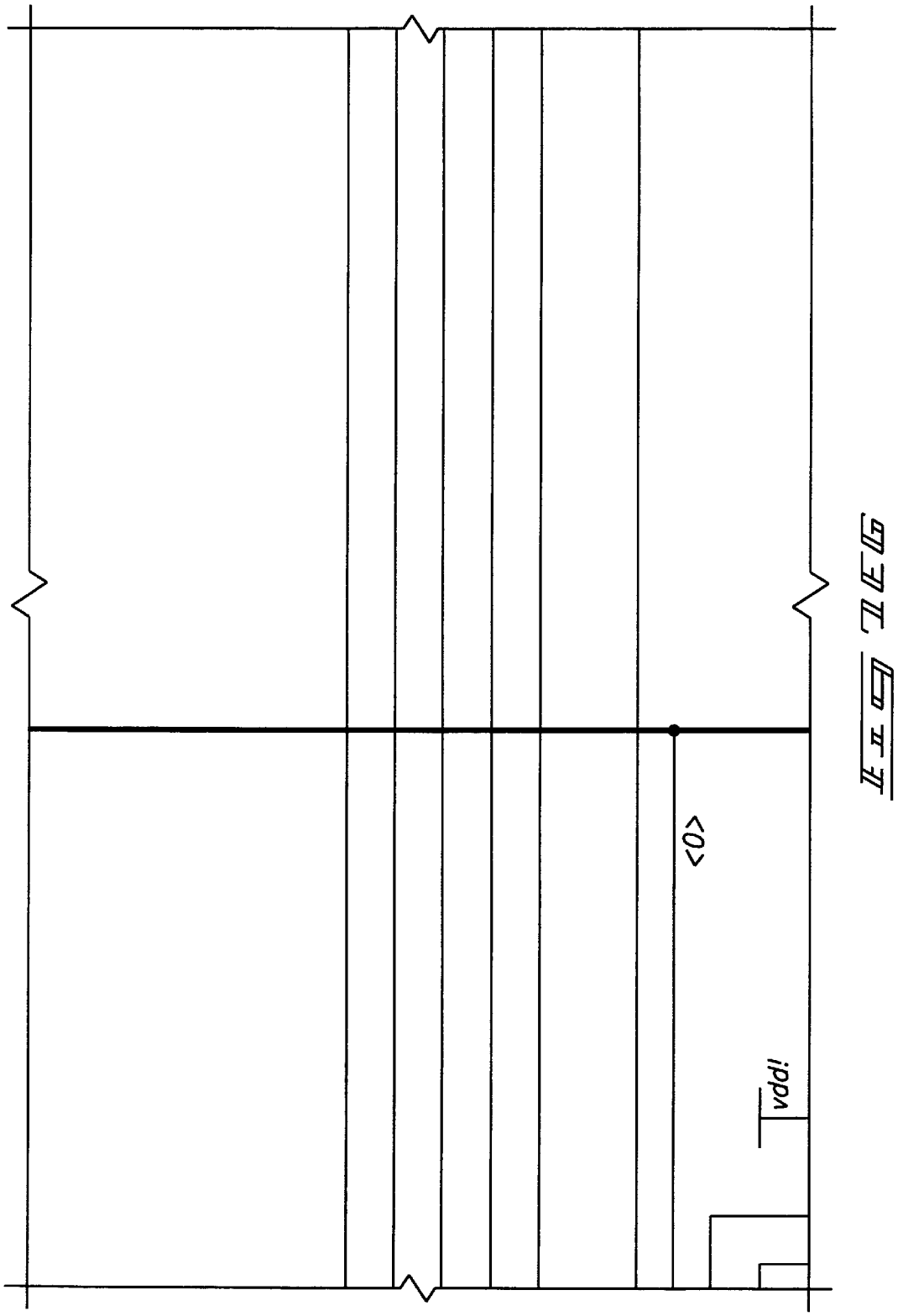


FIG. 93L
<0>
vdd!

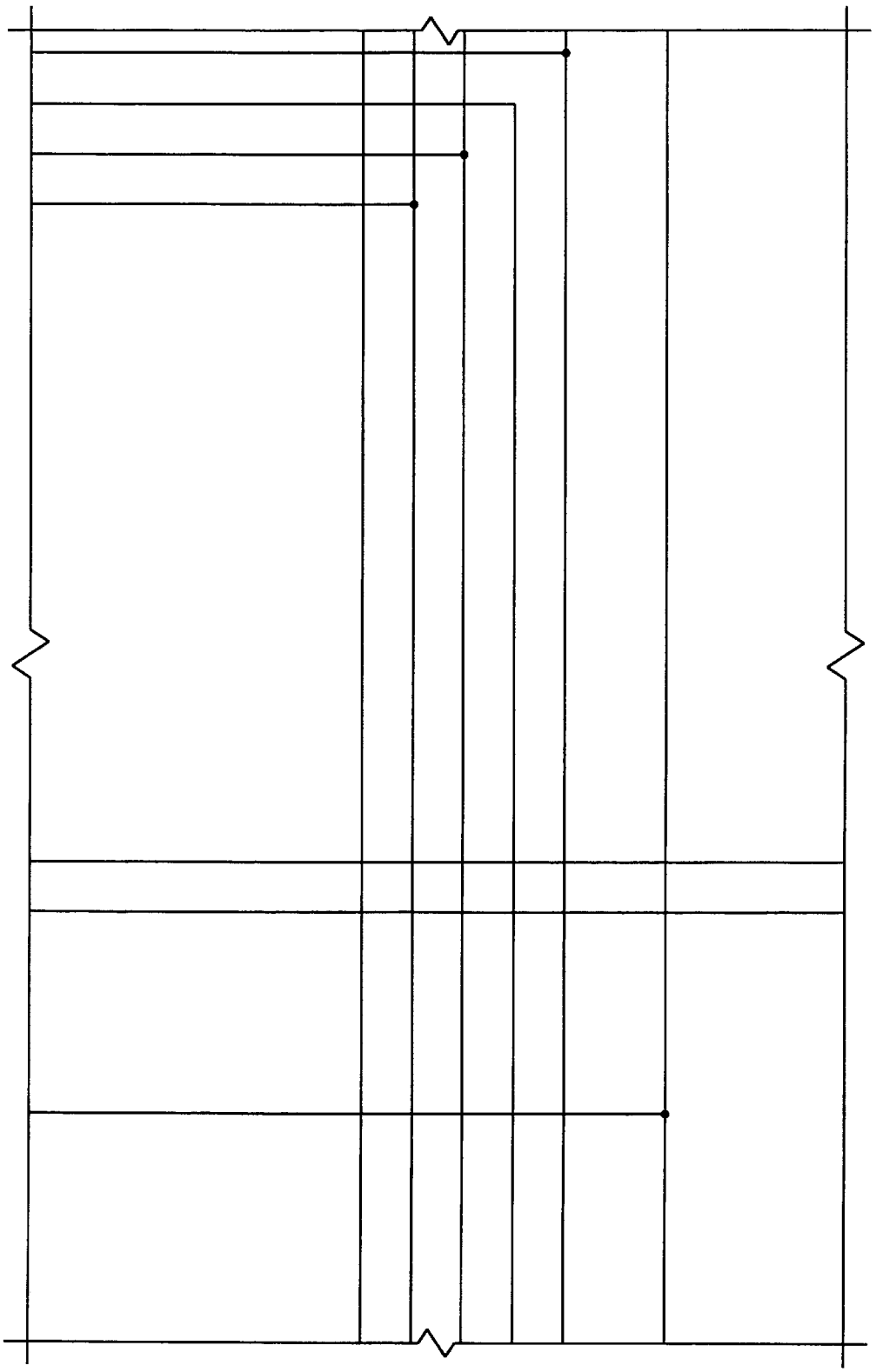


FIG. 69H

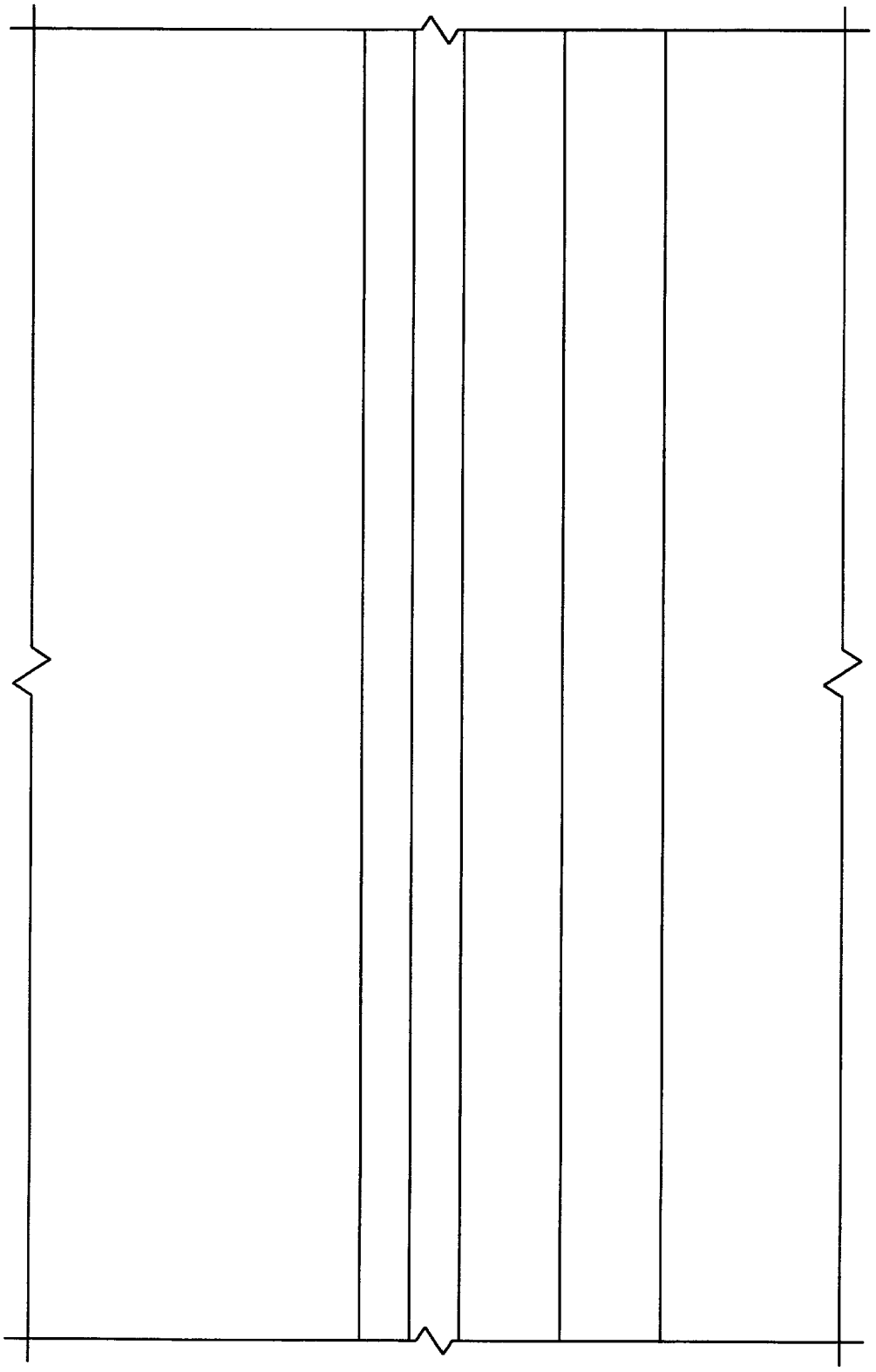


FIG 102

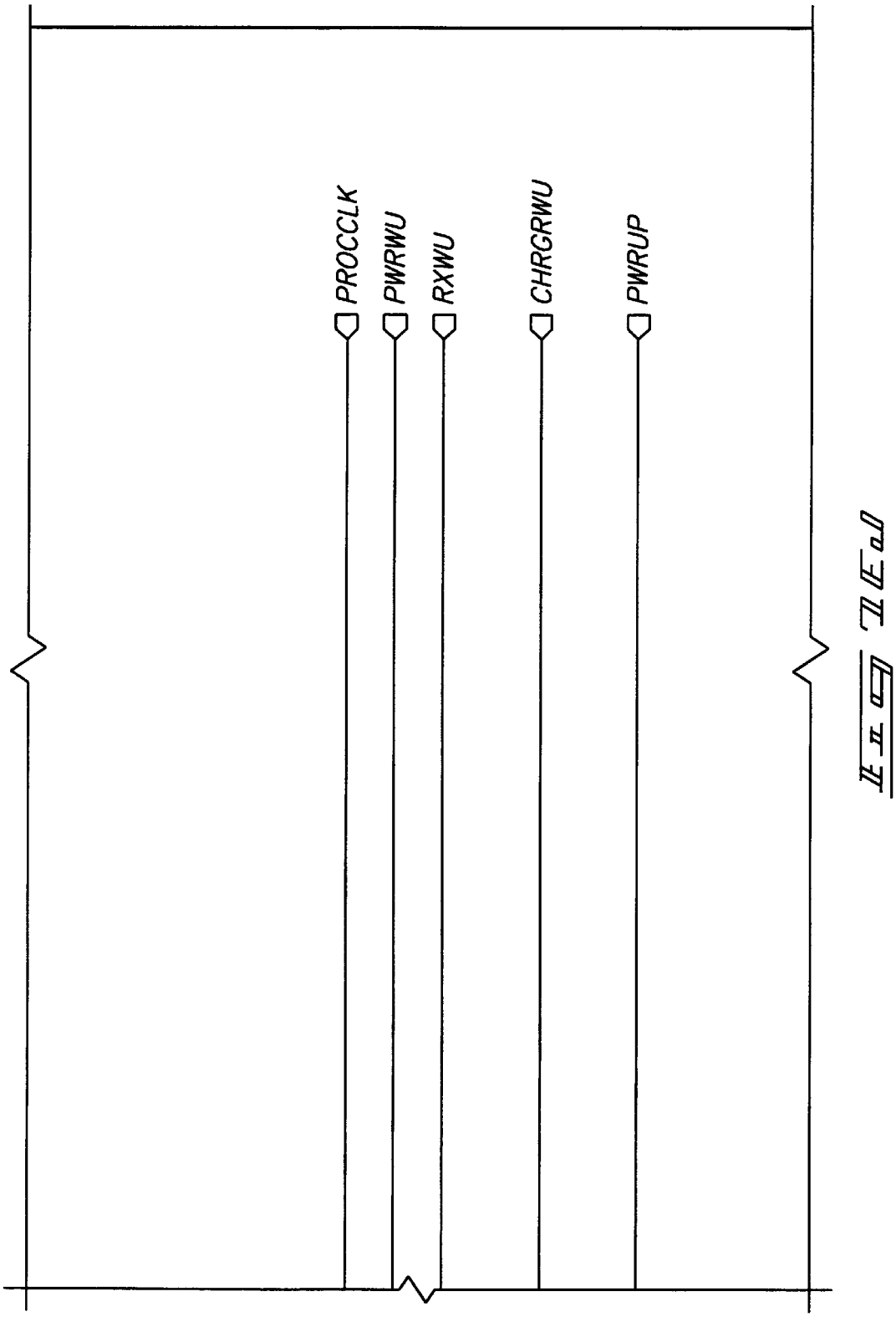


FIG. 69L

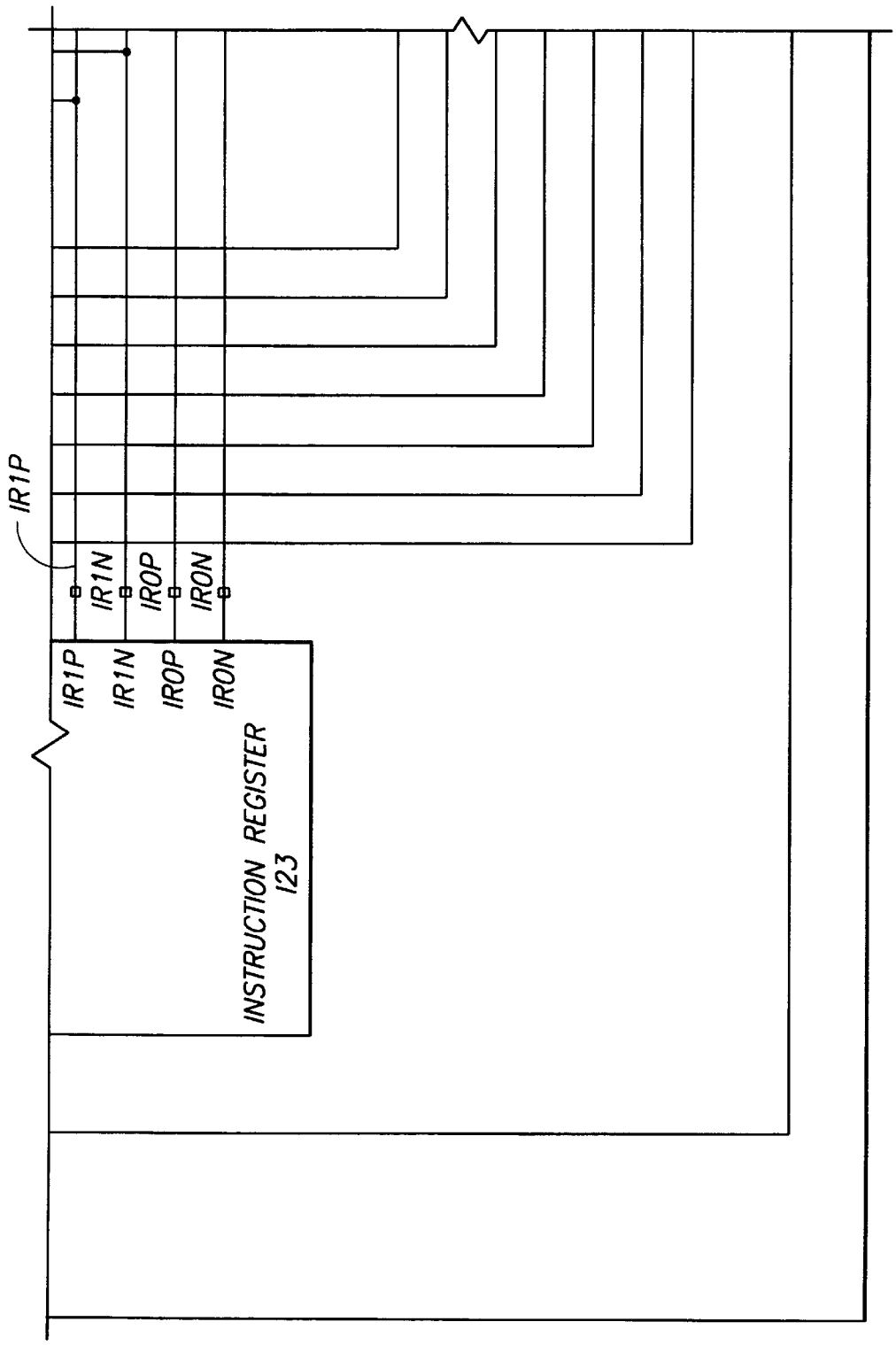

IR1P
IR1N
IROP
IRON
IR1P
IR1N
IROP
IRON
INSTRUCTION REGISTER
123

FIG. 11A

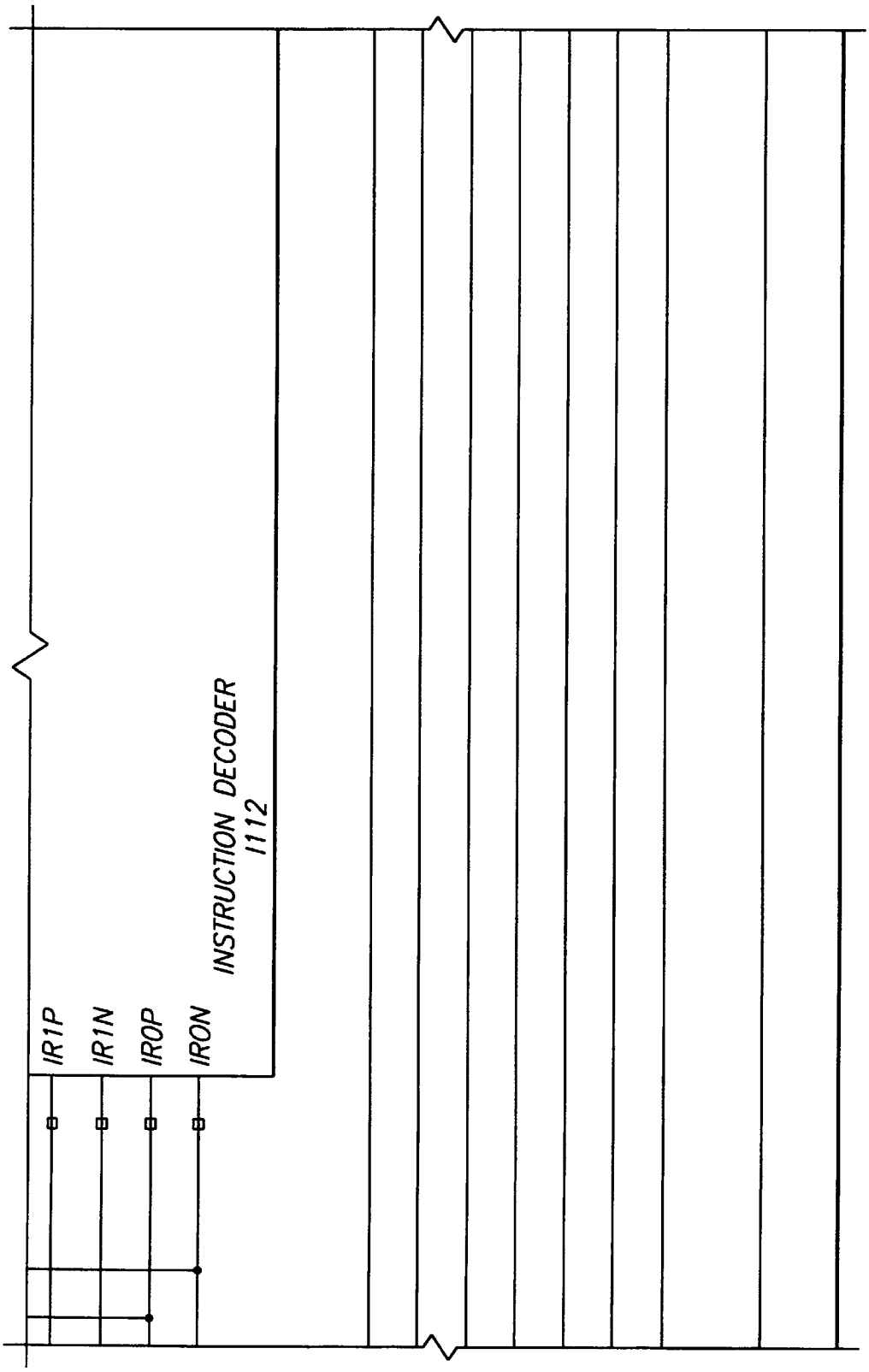


FIG 1B

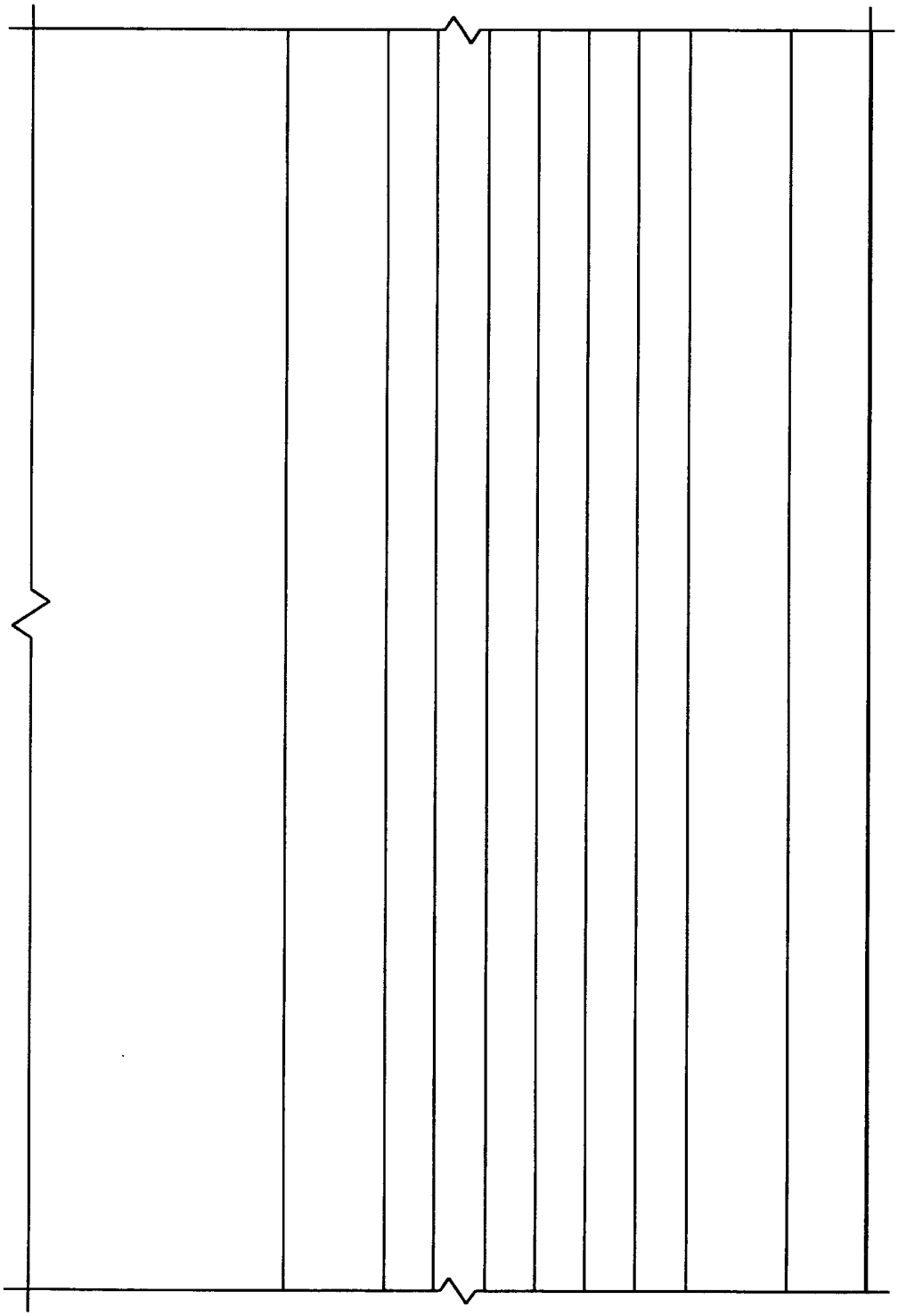


FIG 53

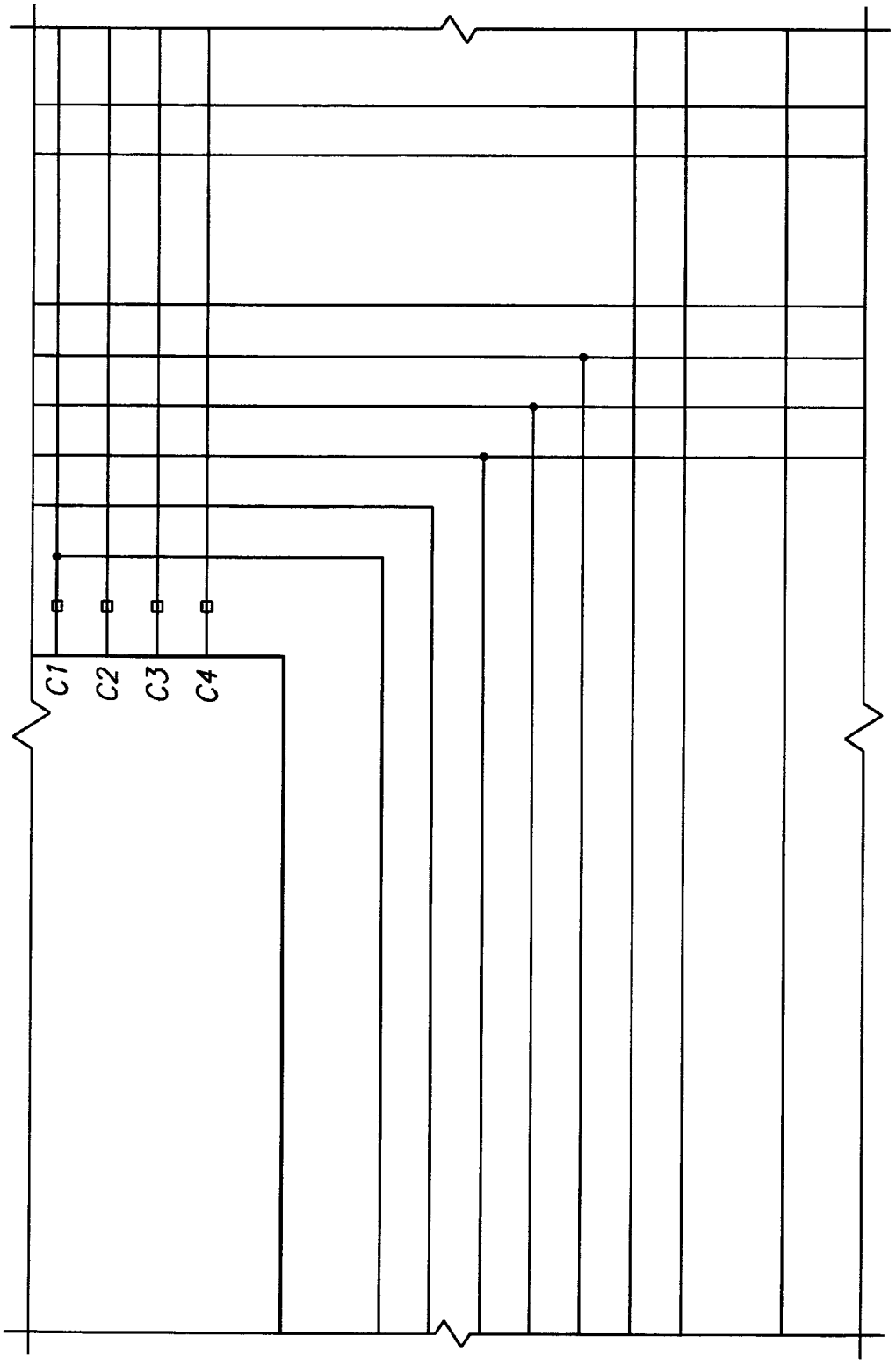


FIG 107

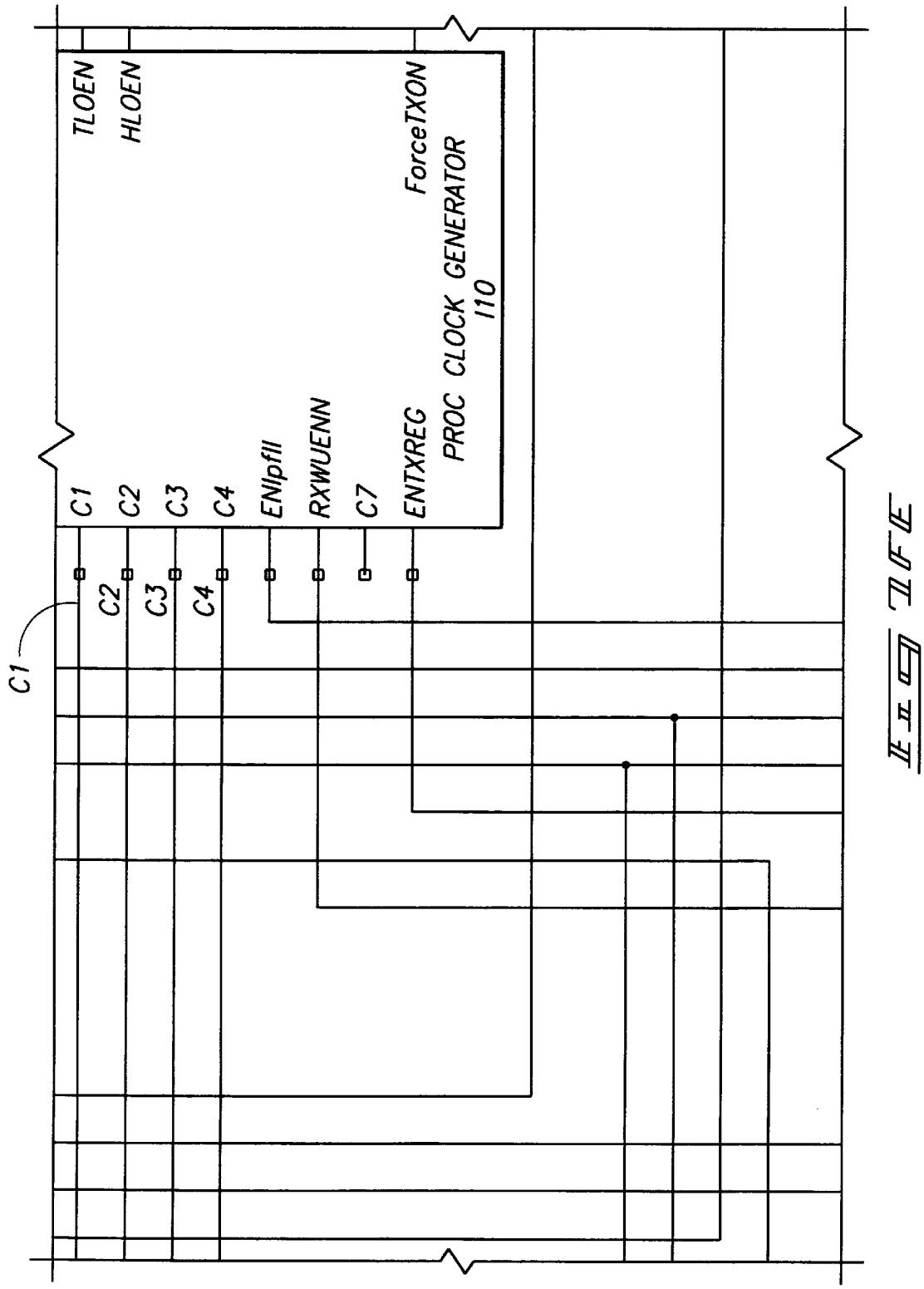

TLOEN
HLOEN
ForceTXON
PROC CLOCK GENERATOR
110
C1
C2
C3
C4
ENIpfll
RXWUENN
C7
ENTXREG
C1
C2
C3
C4

FIG 11E

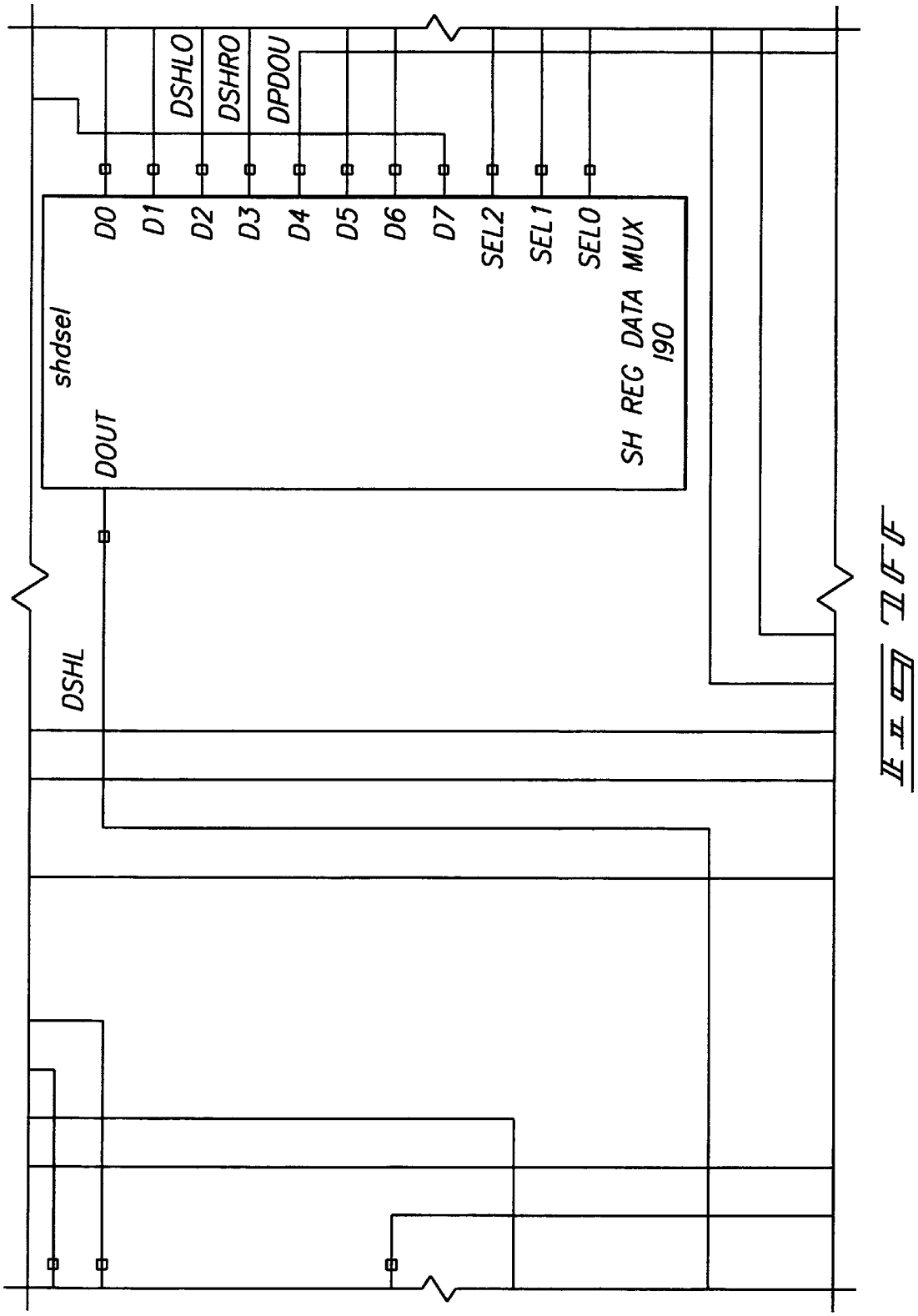

DSHLO
DSHRO
DPDOU
D0
D1
D2
D3
D4
D5
D6
D7
SEL2
SEL1
SEL0
shdsel
DOUT
SH REG DATA MUX
190
DSHL

FIG 111

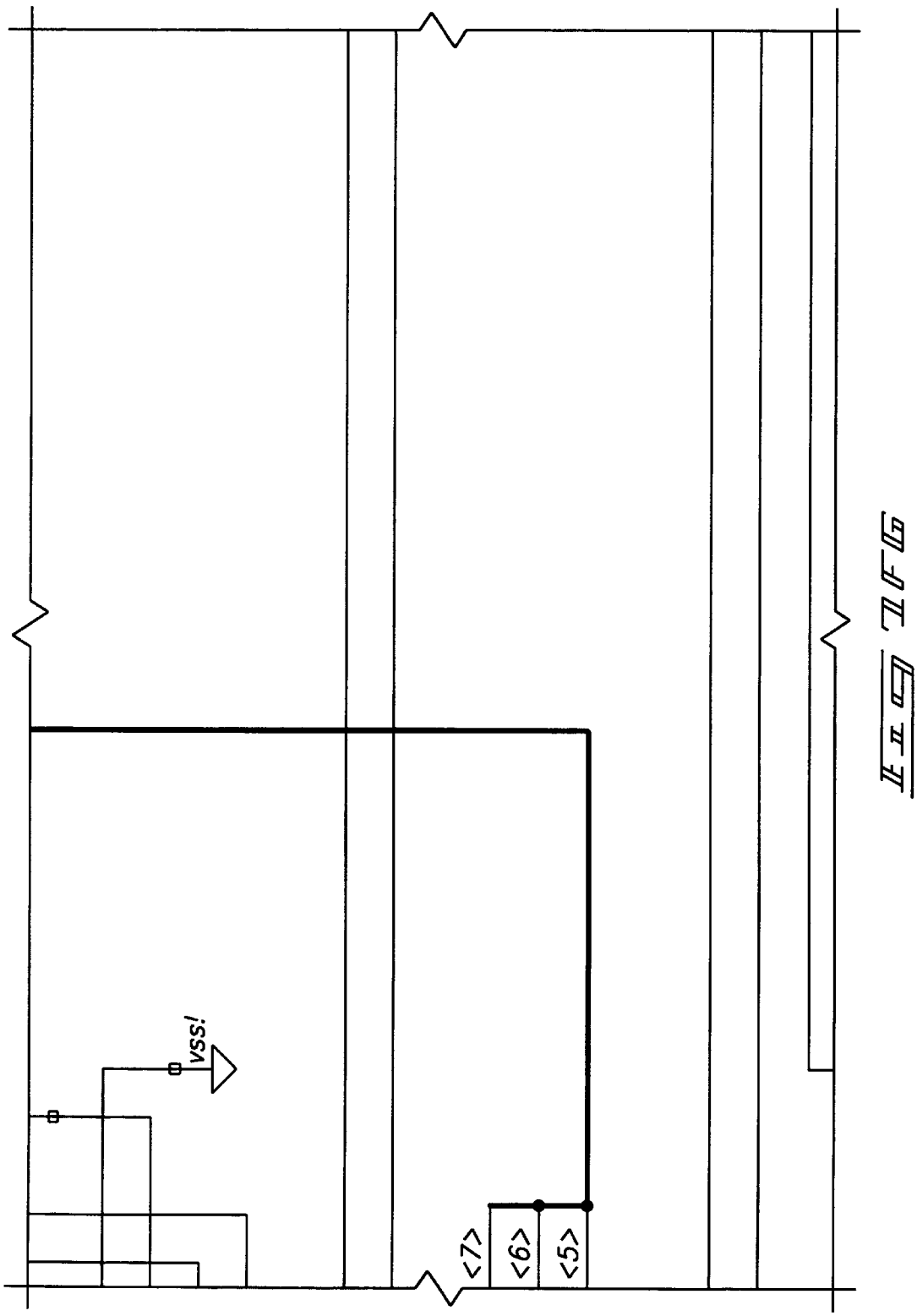


FIG 87A
vss!
<7>
<6>
<5>

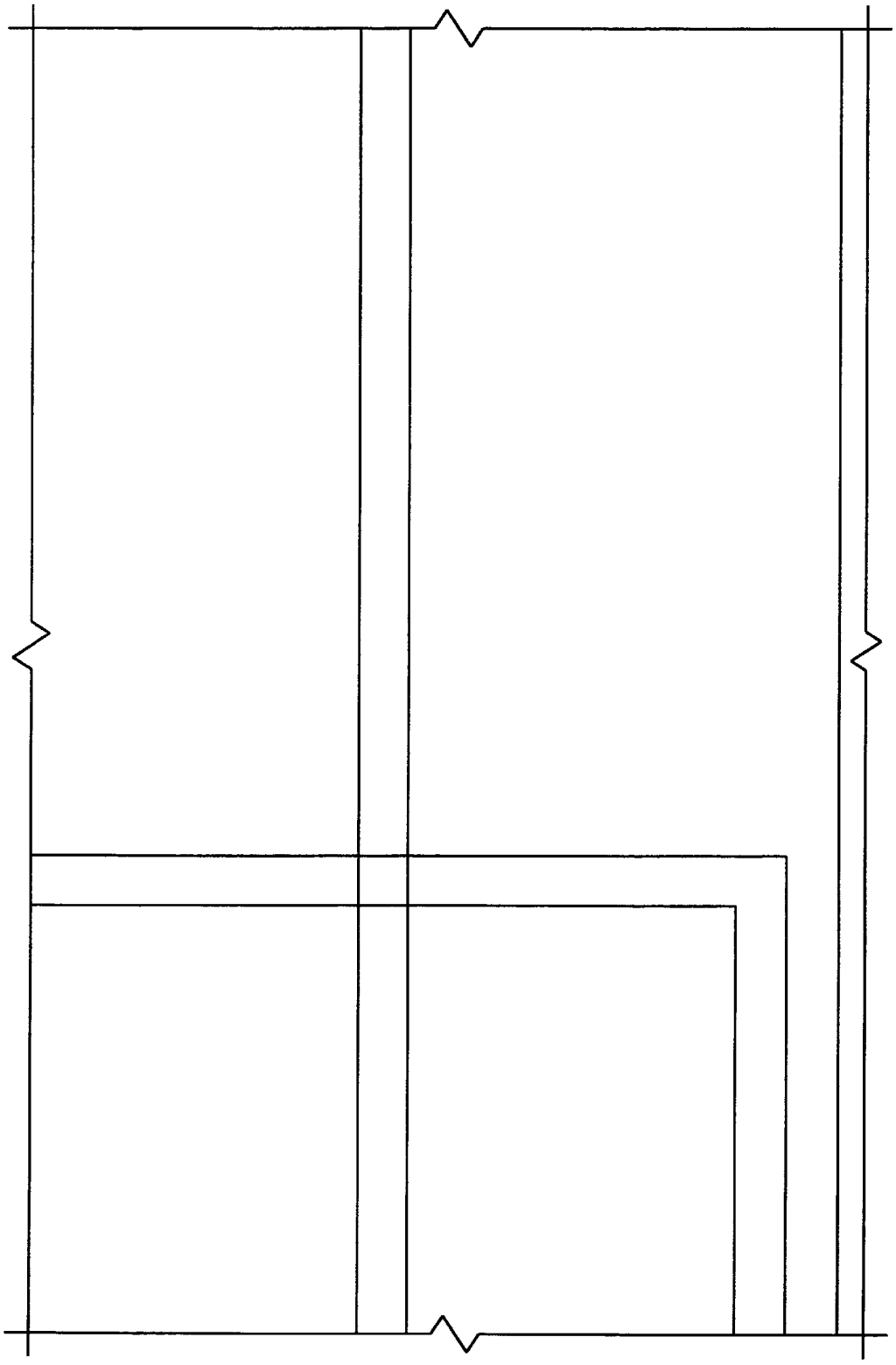


FIG 111

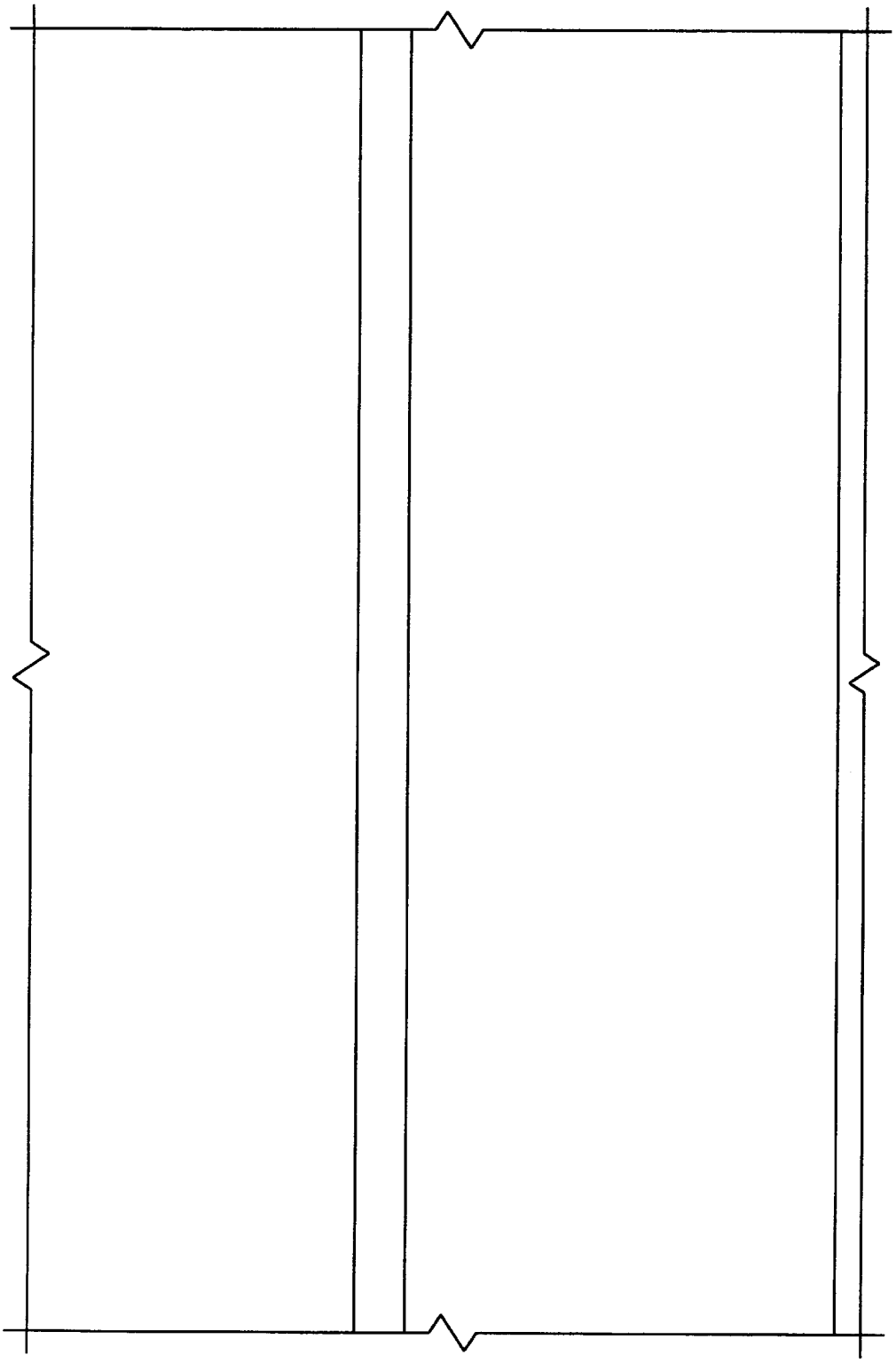


FIG. 55AII

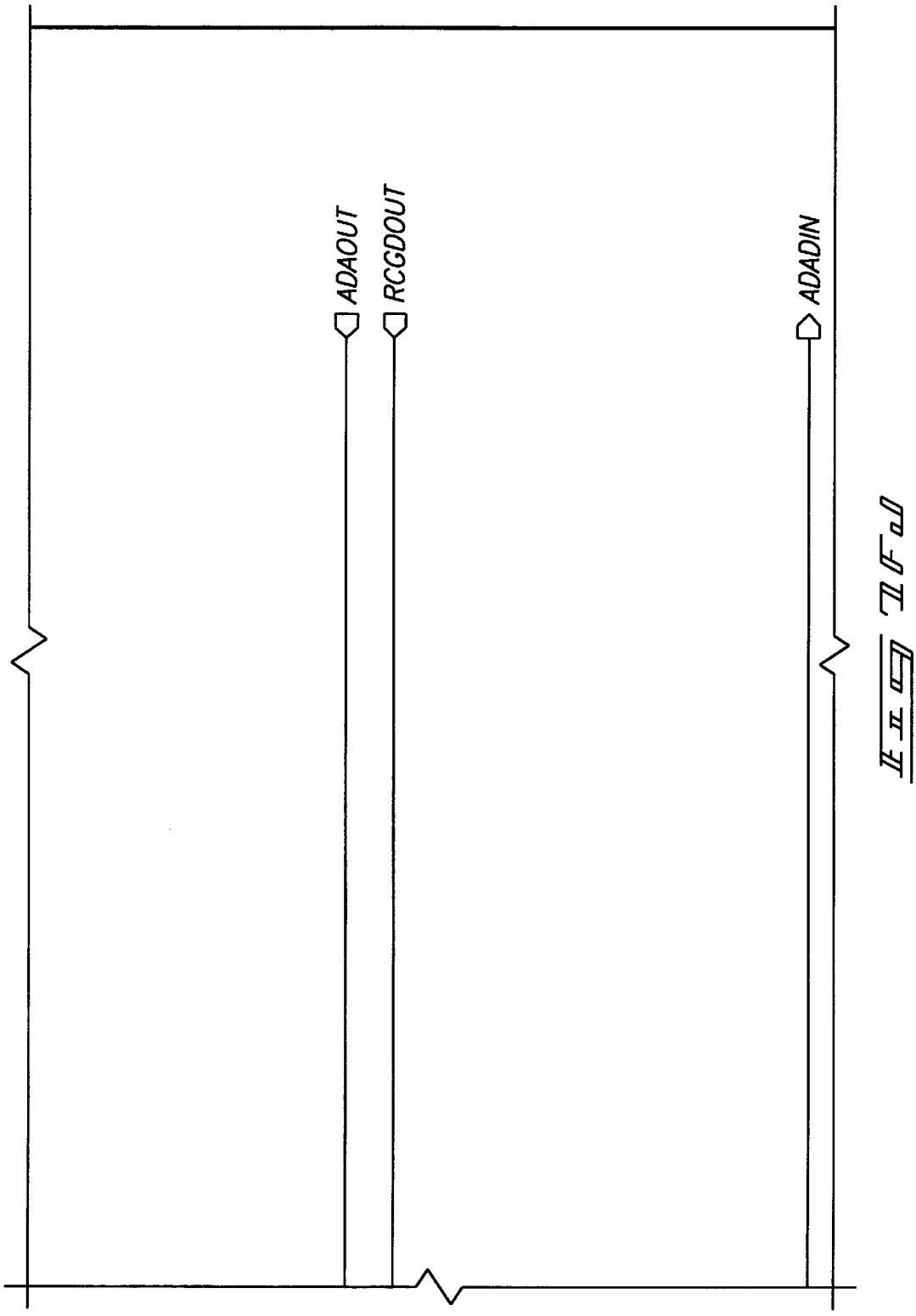


FIG 11F

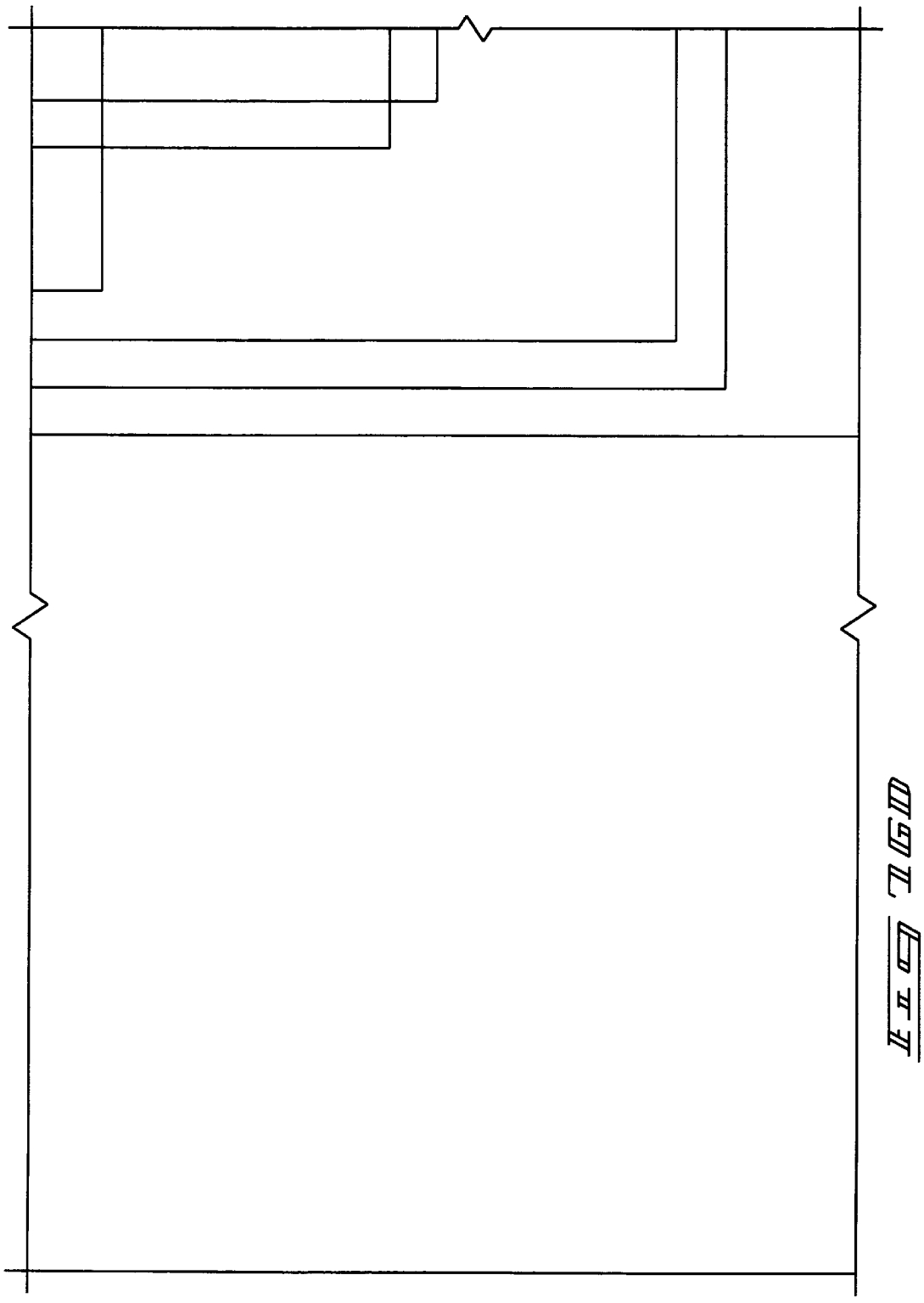


FIG 1150

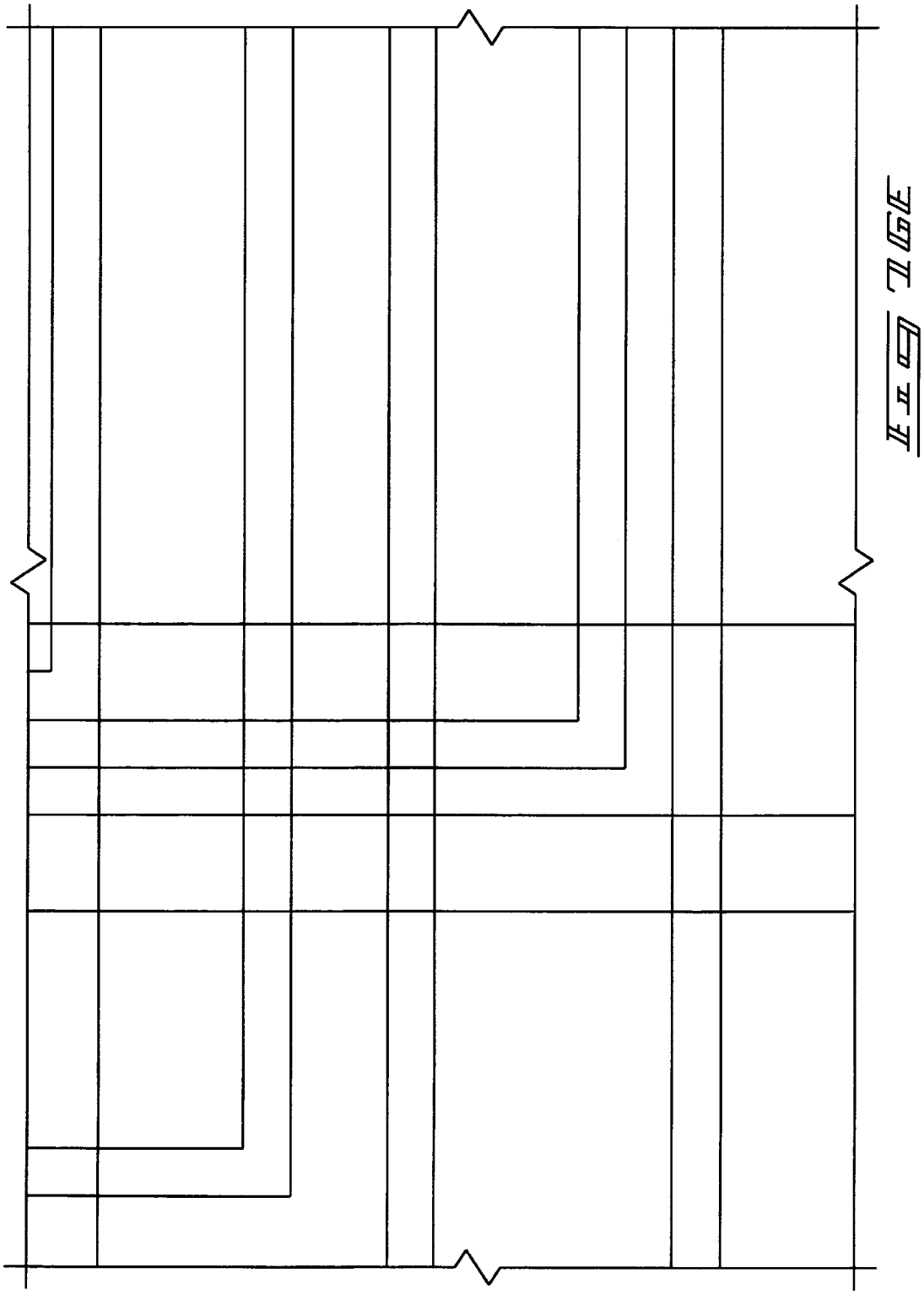


FIG 391

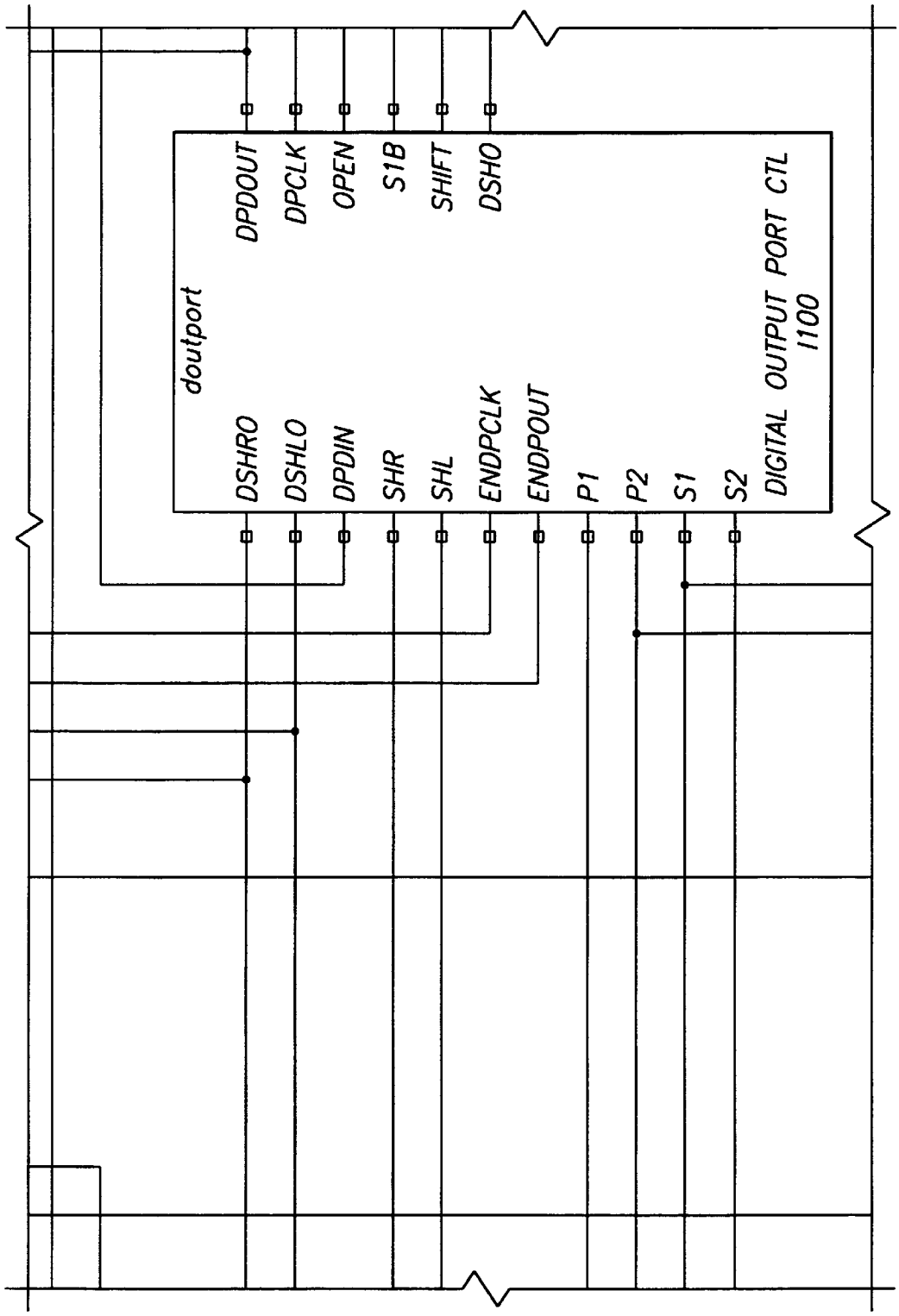

doutport
DPDOUT
DPCLK
OPEN
S1B
SHIFT
DSHO
DSHRO
DSHLO
DPDIN
SHR
SHL
ENDPCLK
ENDPOUT
P1
P2
S1
S2
DIGITAL OUTPUT PORT CTL
1100

FIG 116

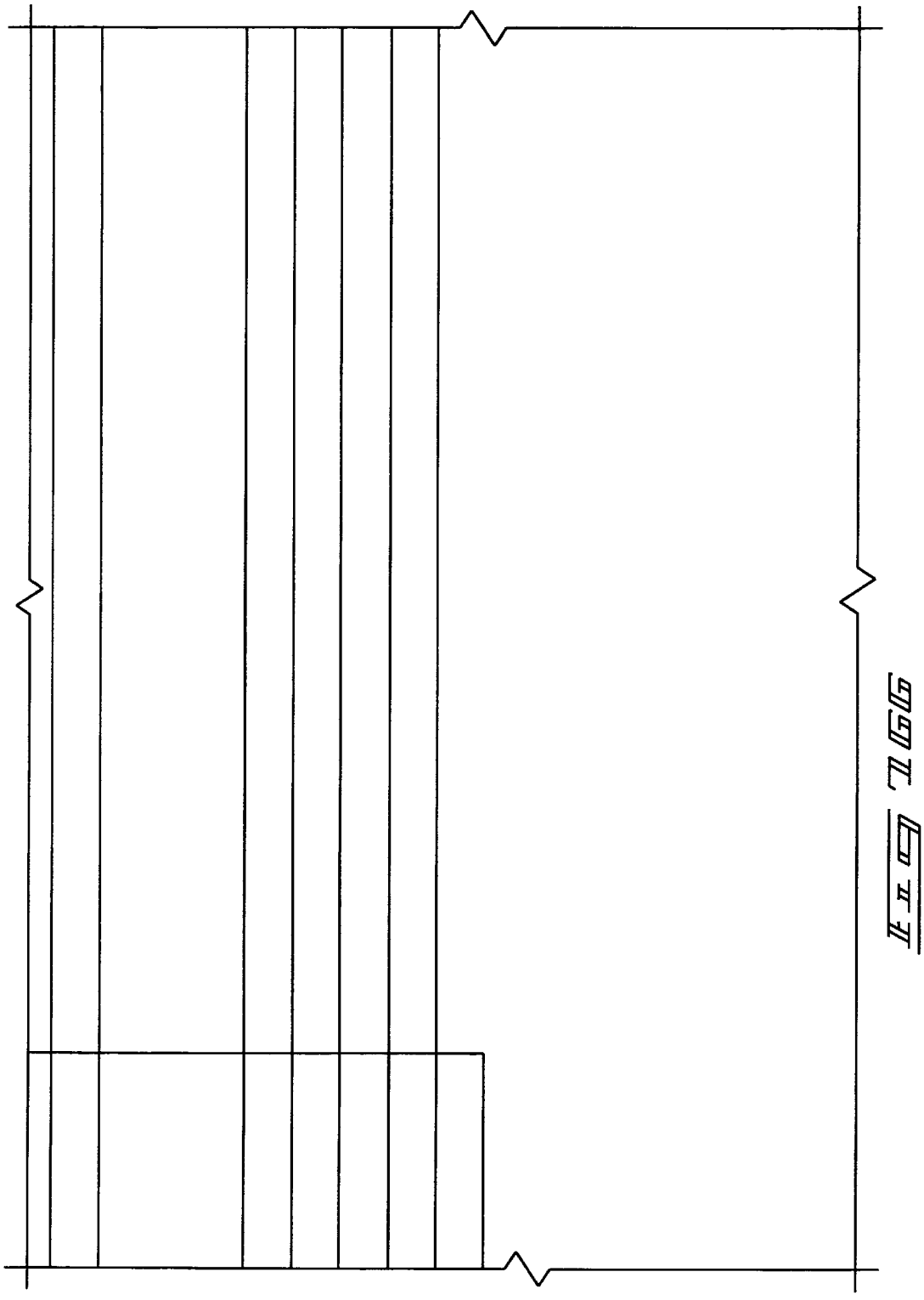


FIG 117

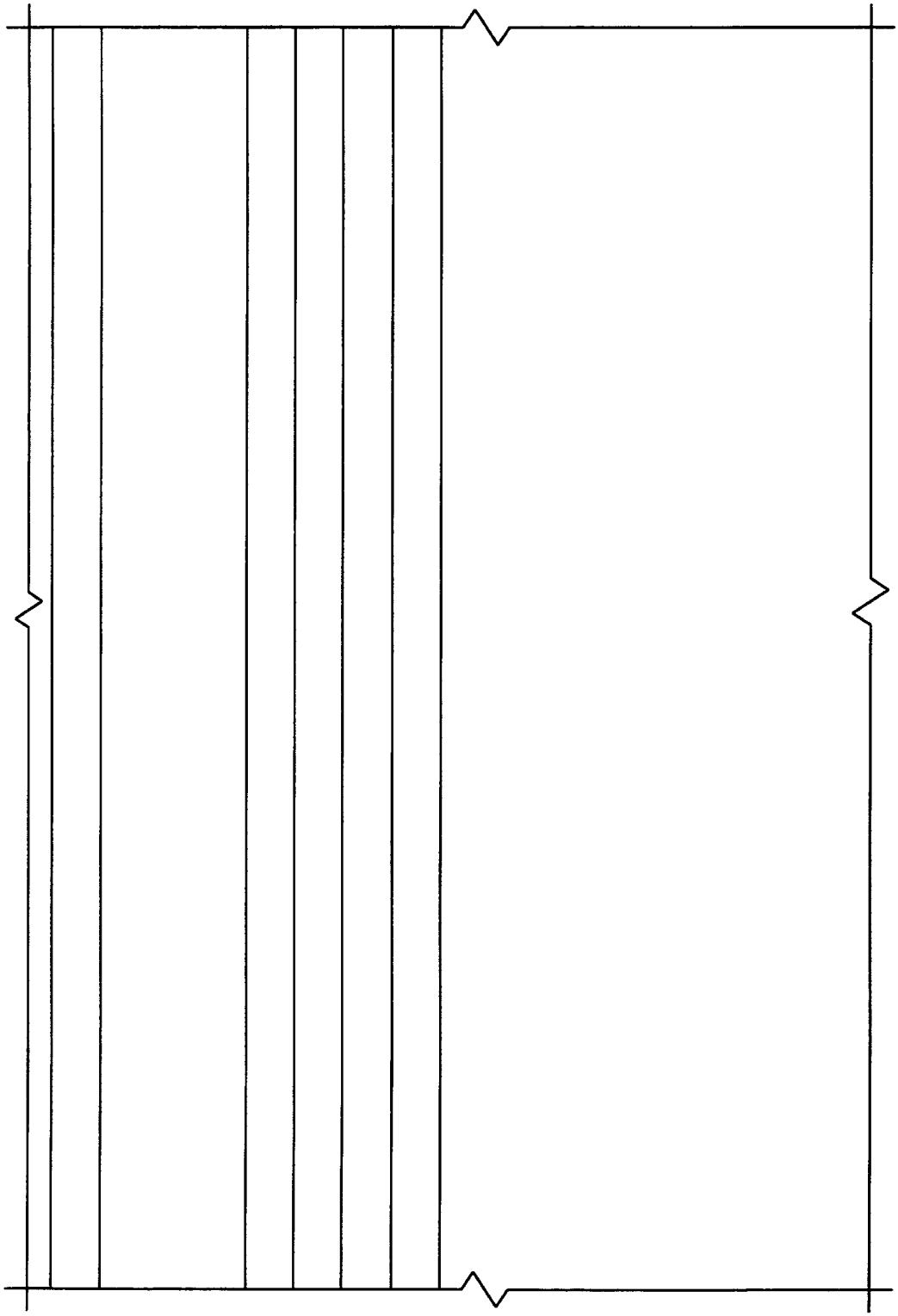


FIG. 59H

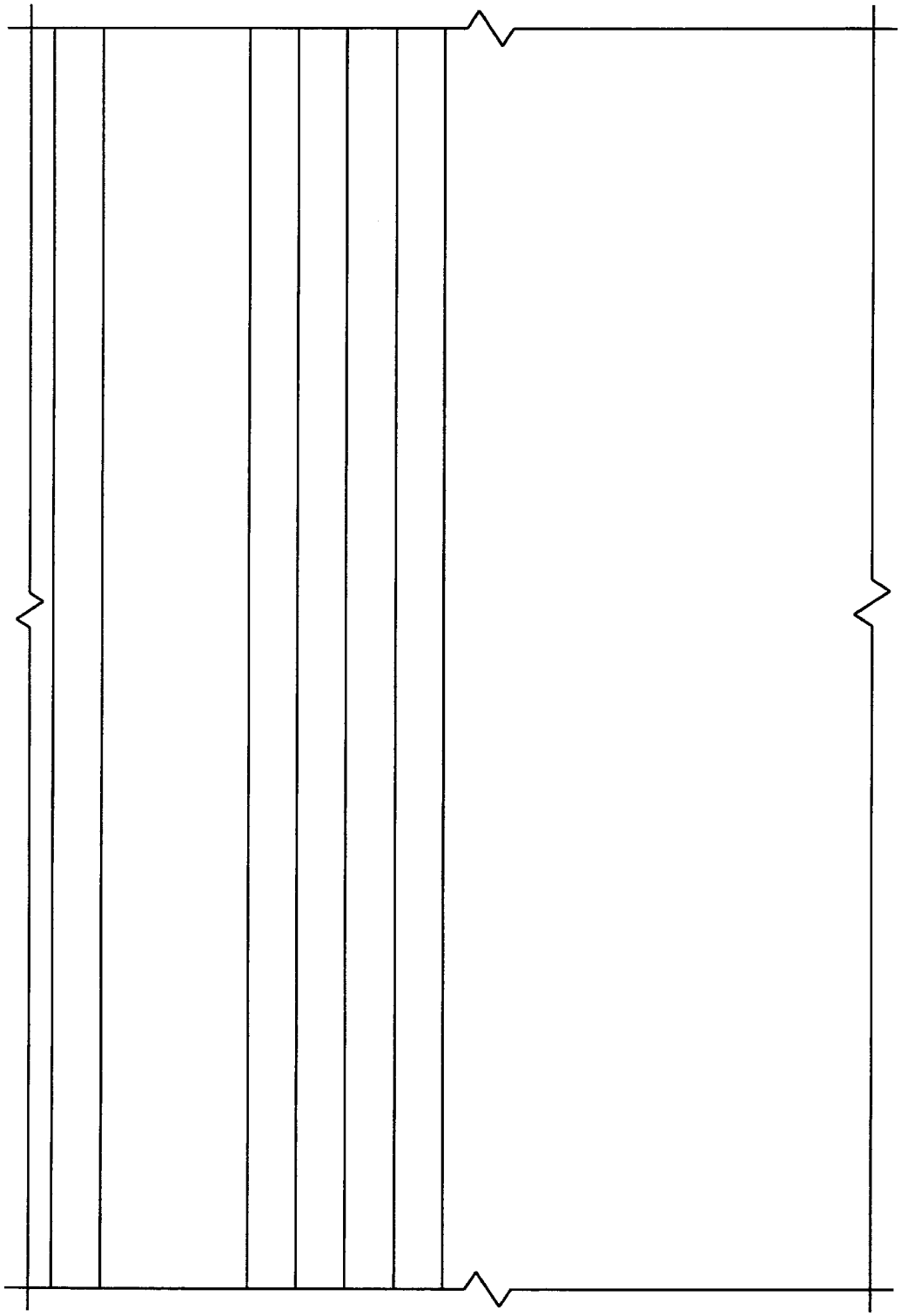


FIG. 59L

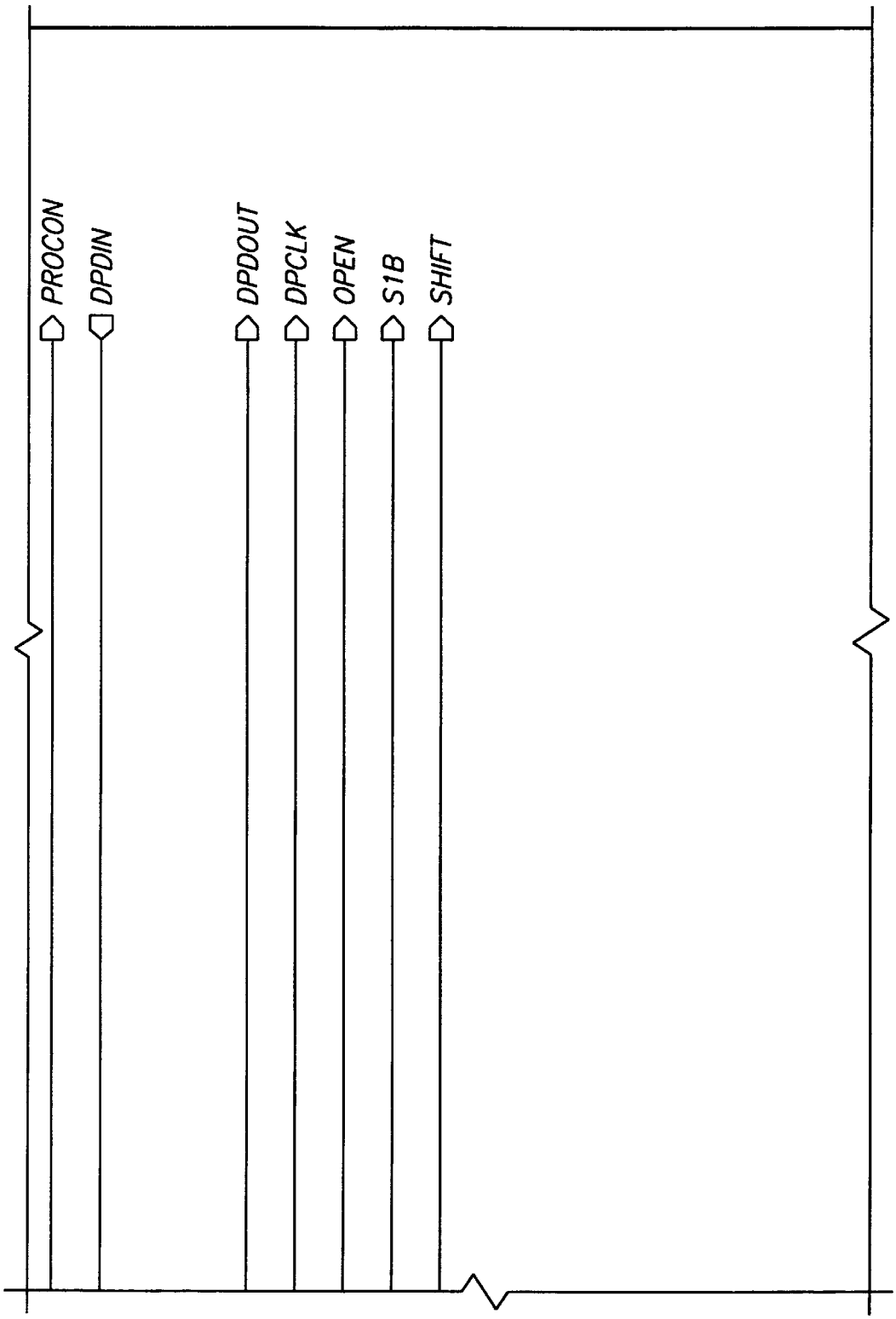


FIG. 119

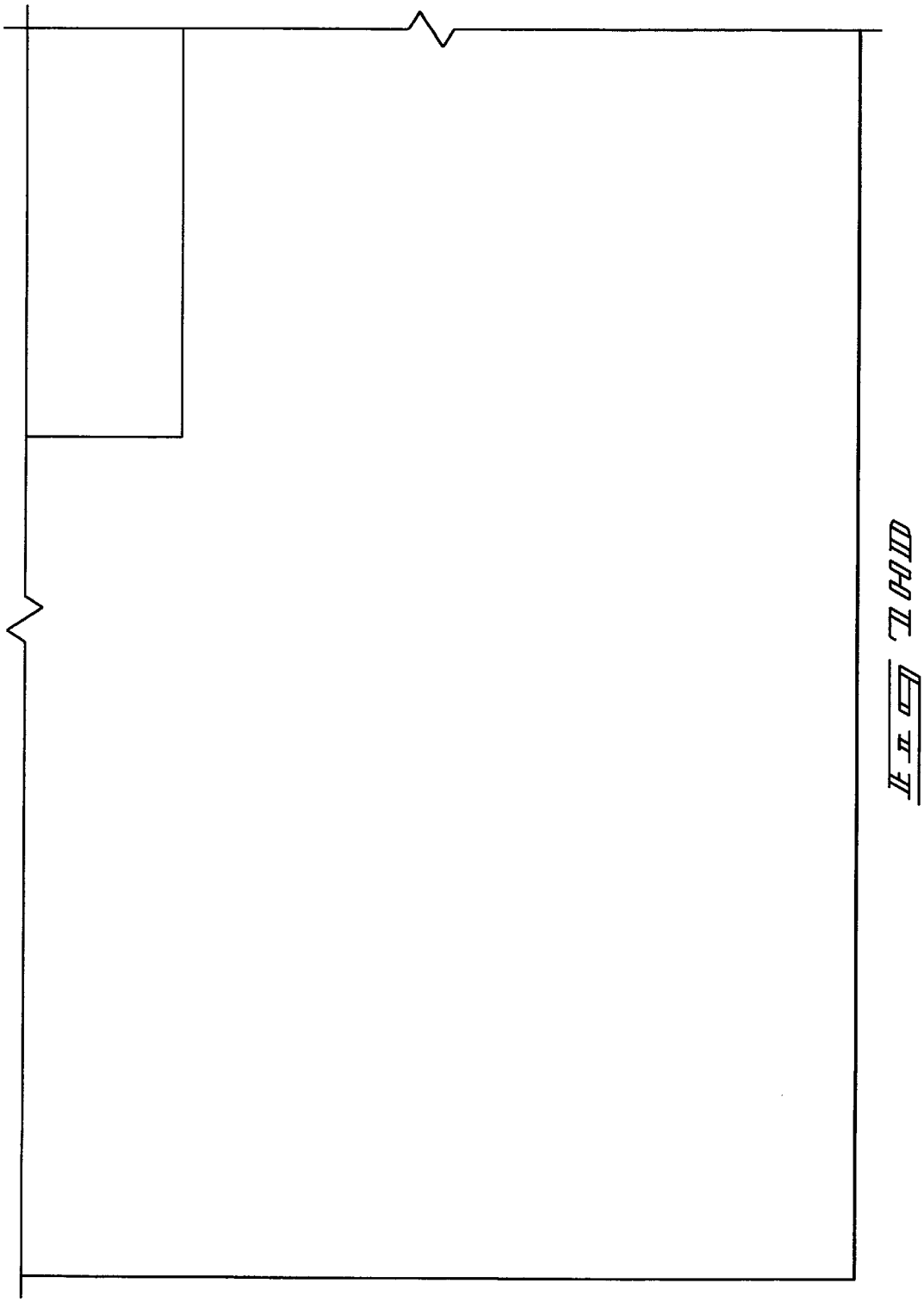


FIG. 59

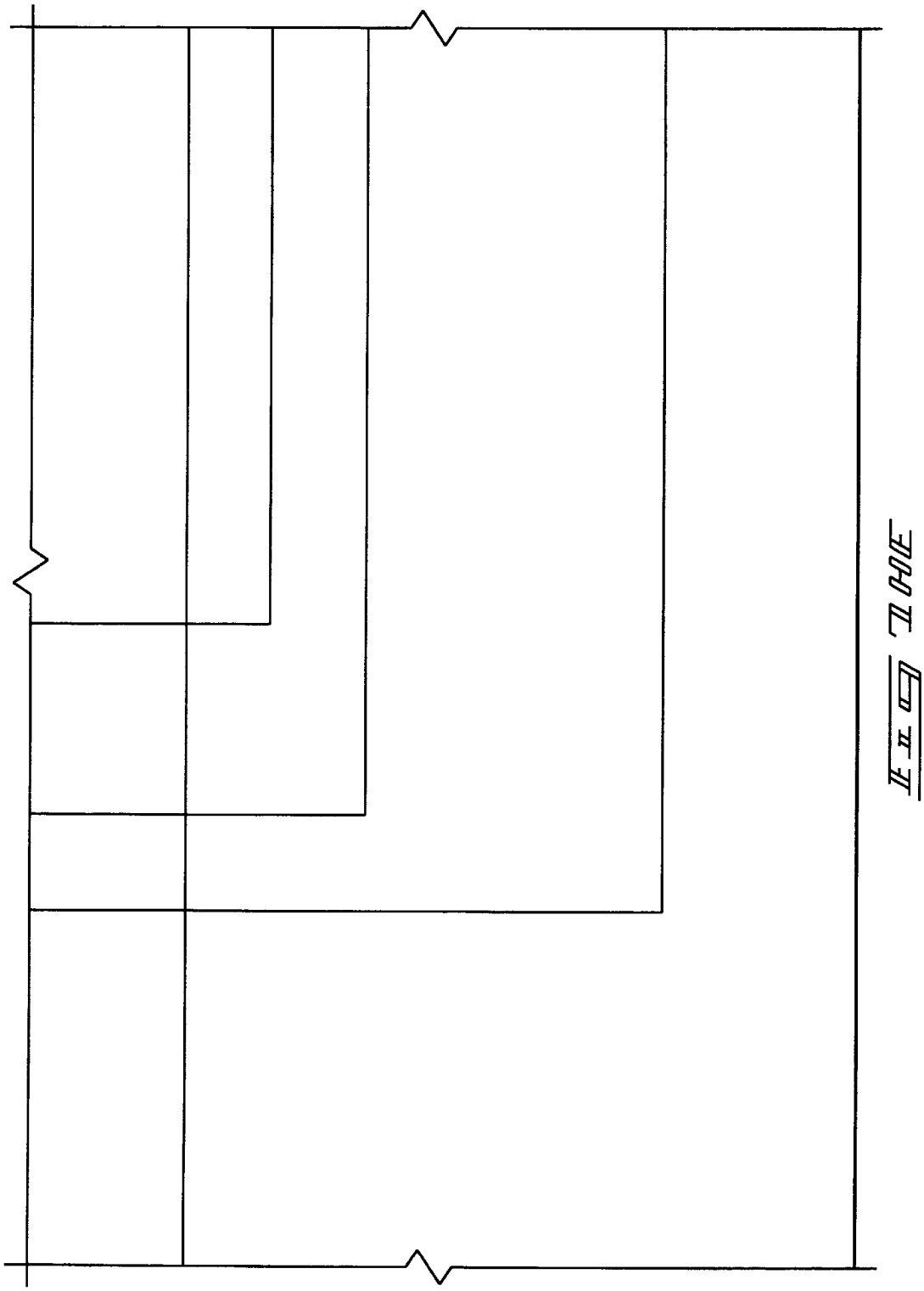


FIG. 122

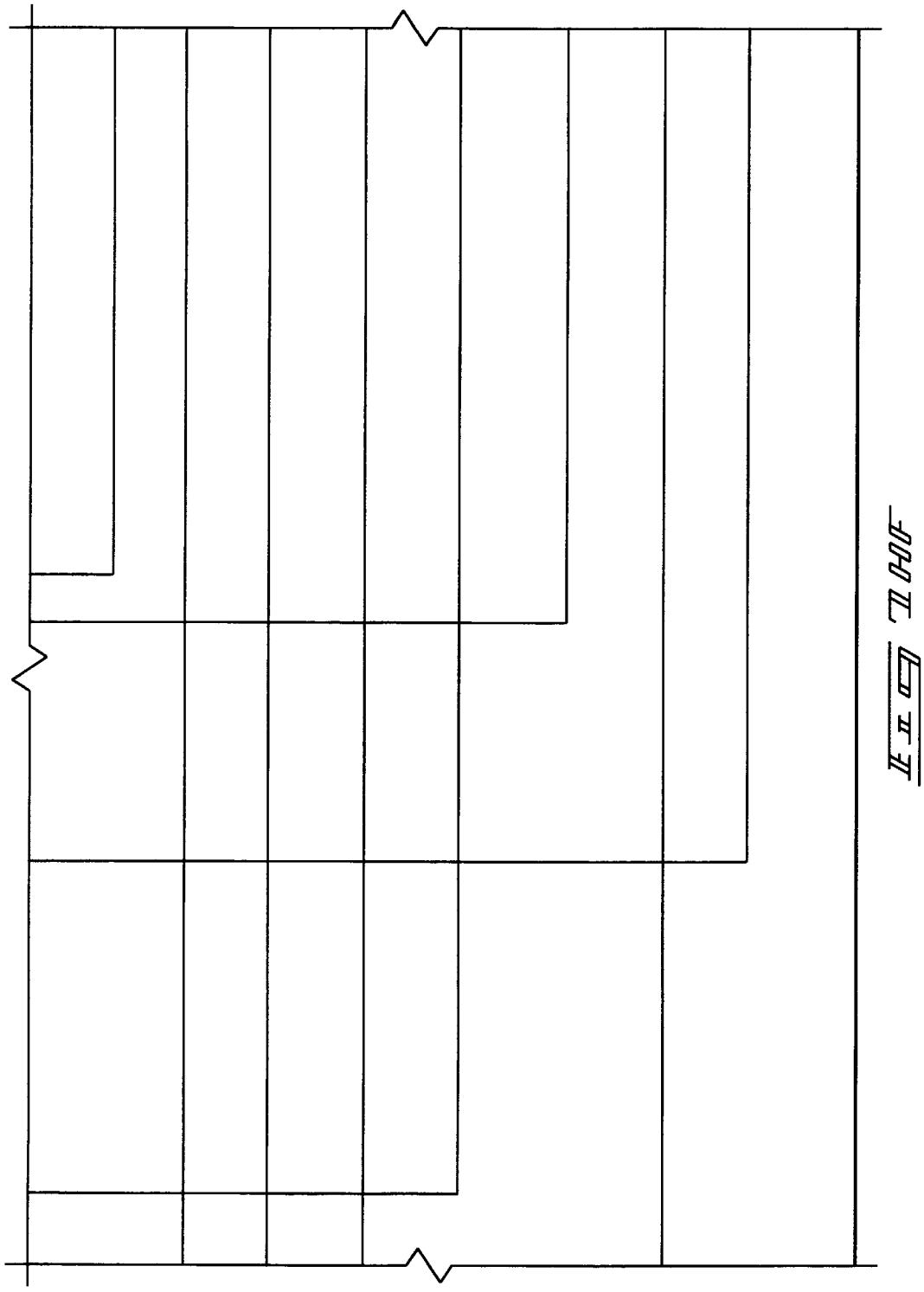


FIG. 11AF

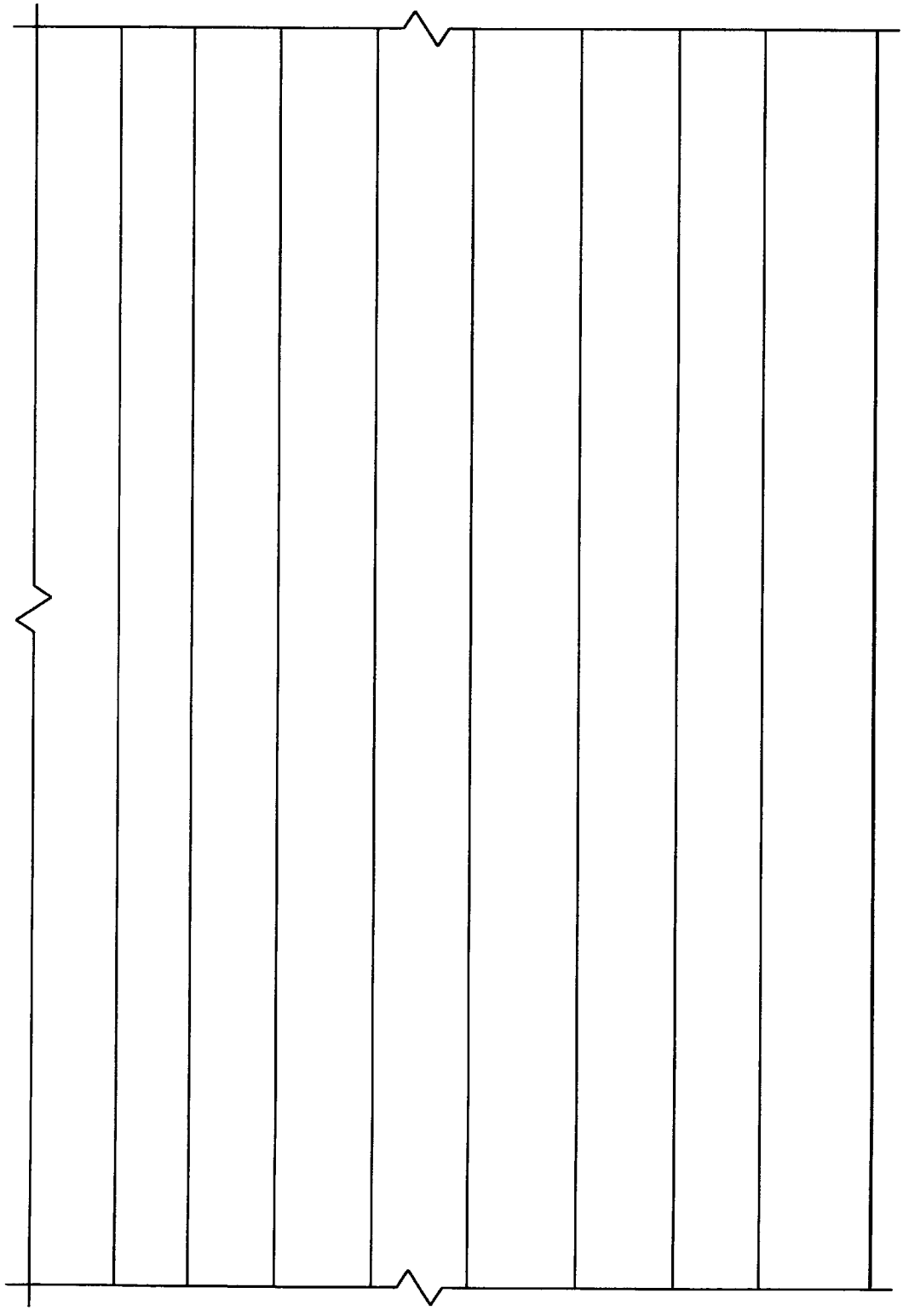


FIG 124

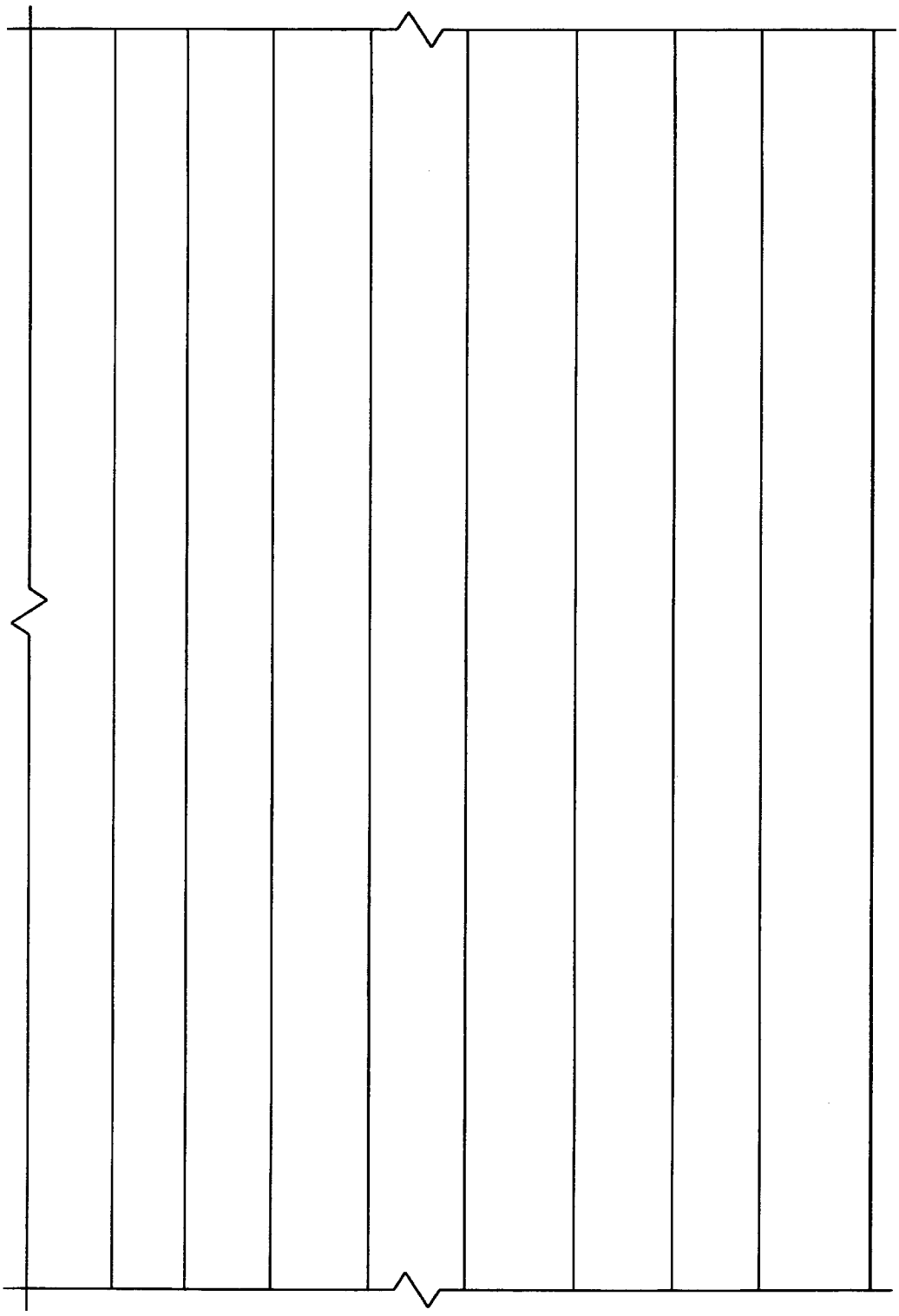


FIG. 11A

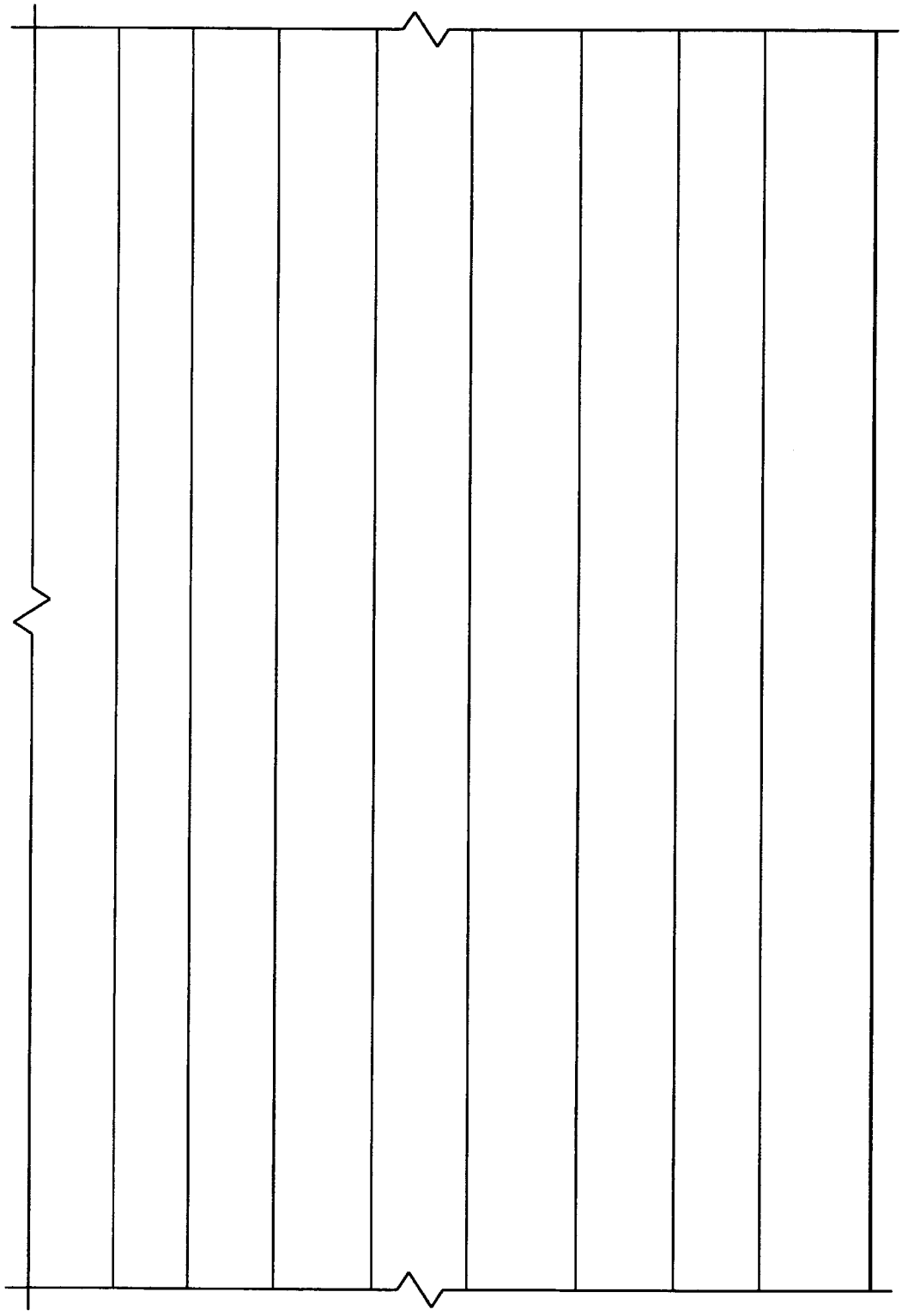


FIG. 126

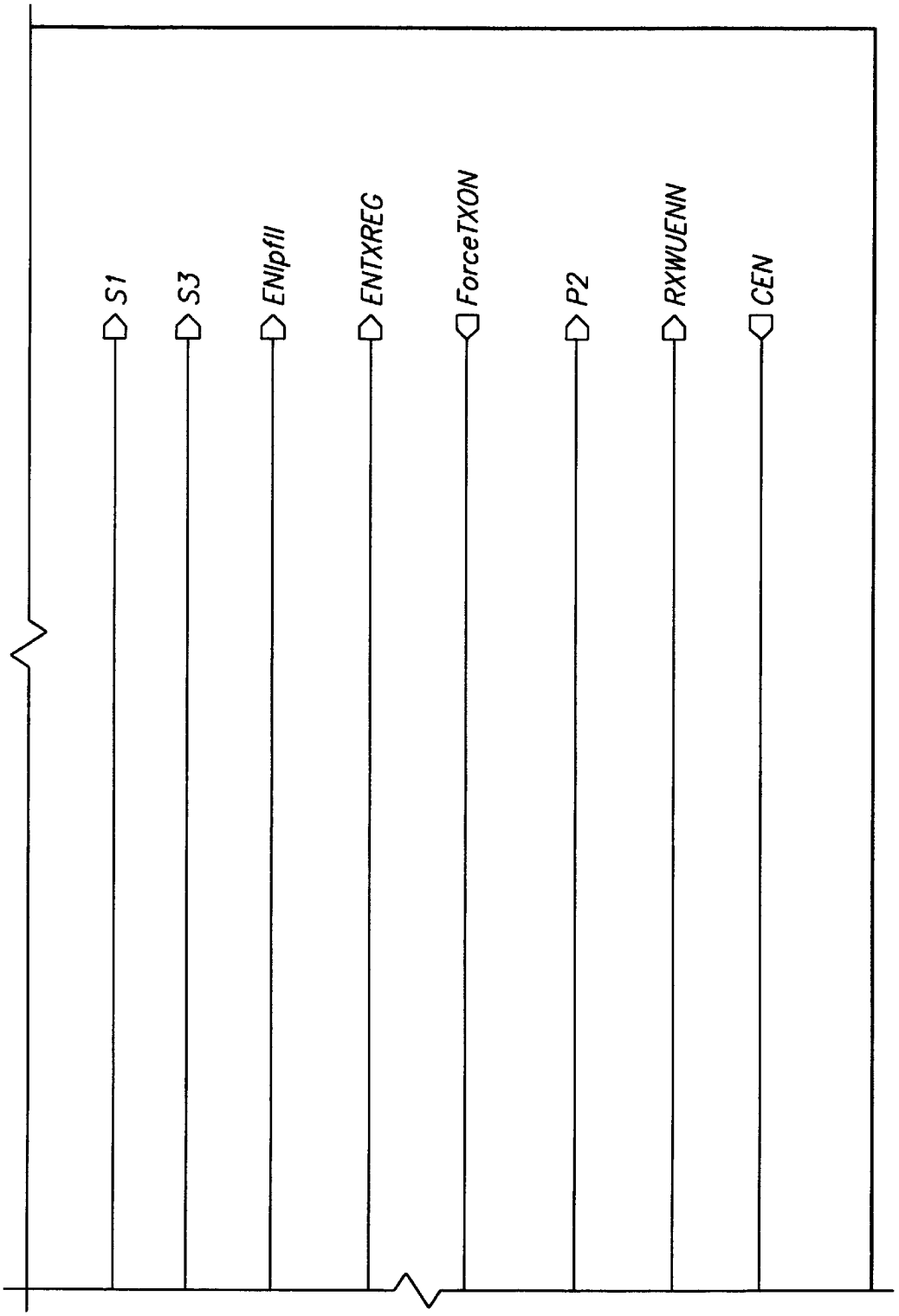


FIG 11

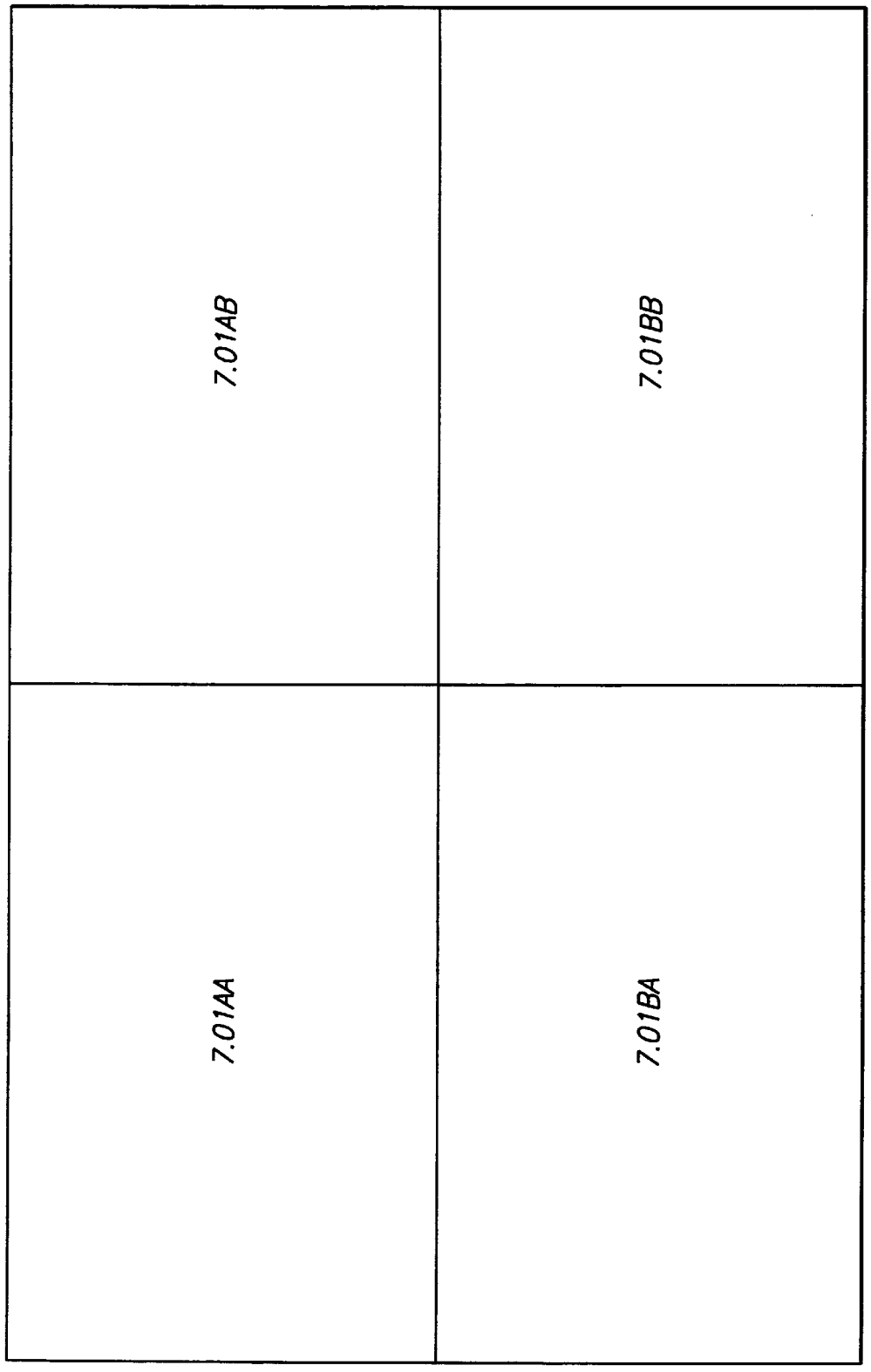


FIG. 7.01

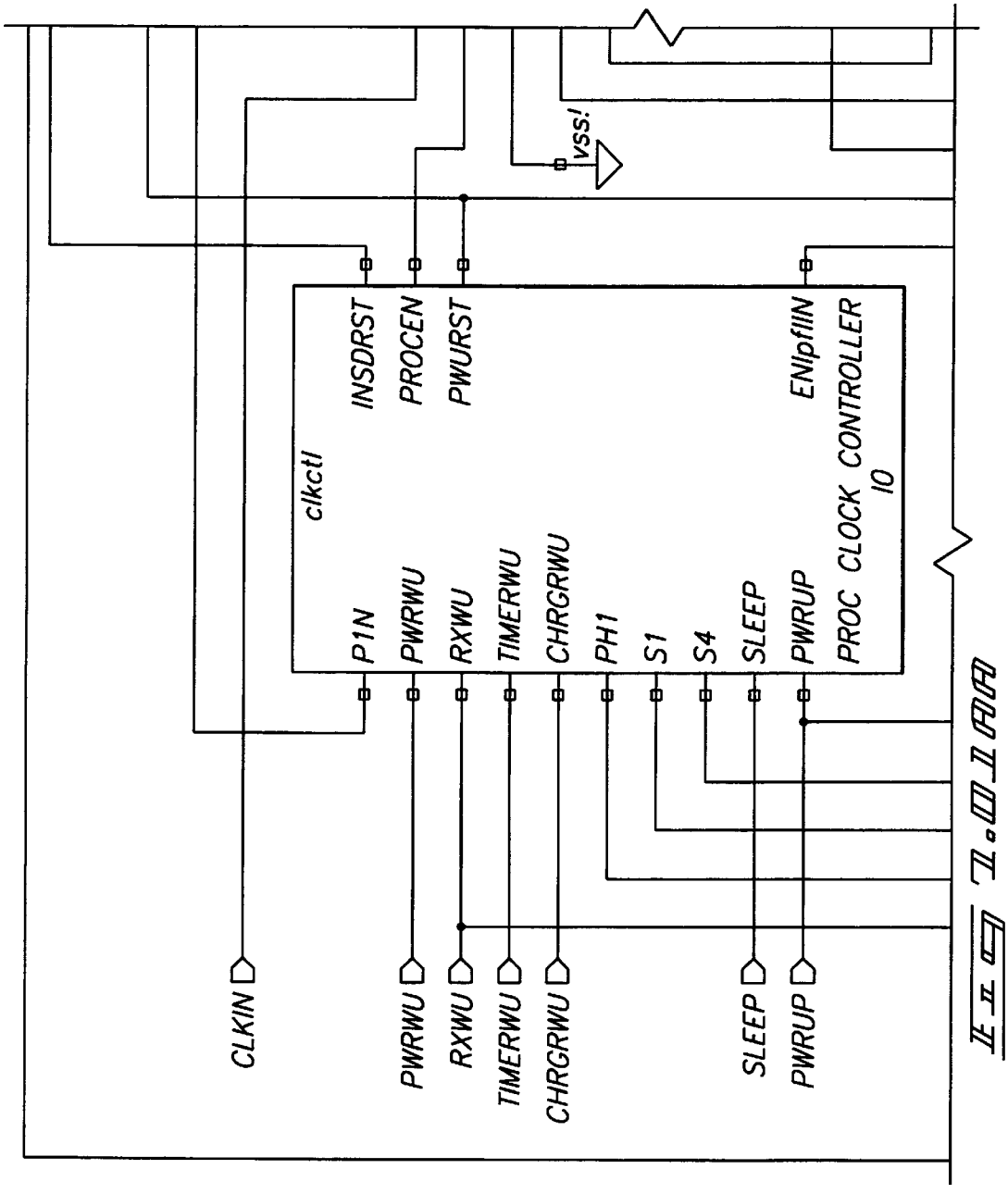

vss!
clkctl
INSDRST
PROCEN
PWURST
ENIpfIIN
CONTROLLER
CLOCK
PROC
I0
P1N
PWRWU
RXWU
TIMERWU
CHRGRWU
PH1
S1
S4
SLEEP
PWRUP
CLKIN
PWRWU
RXWU
TIMERWU
CHRGRWU
SLEEP
PWRUP

FIG. 1.00 IA

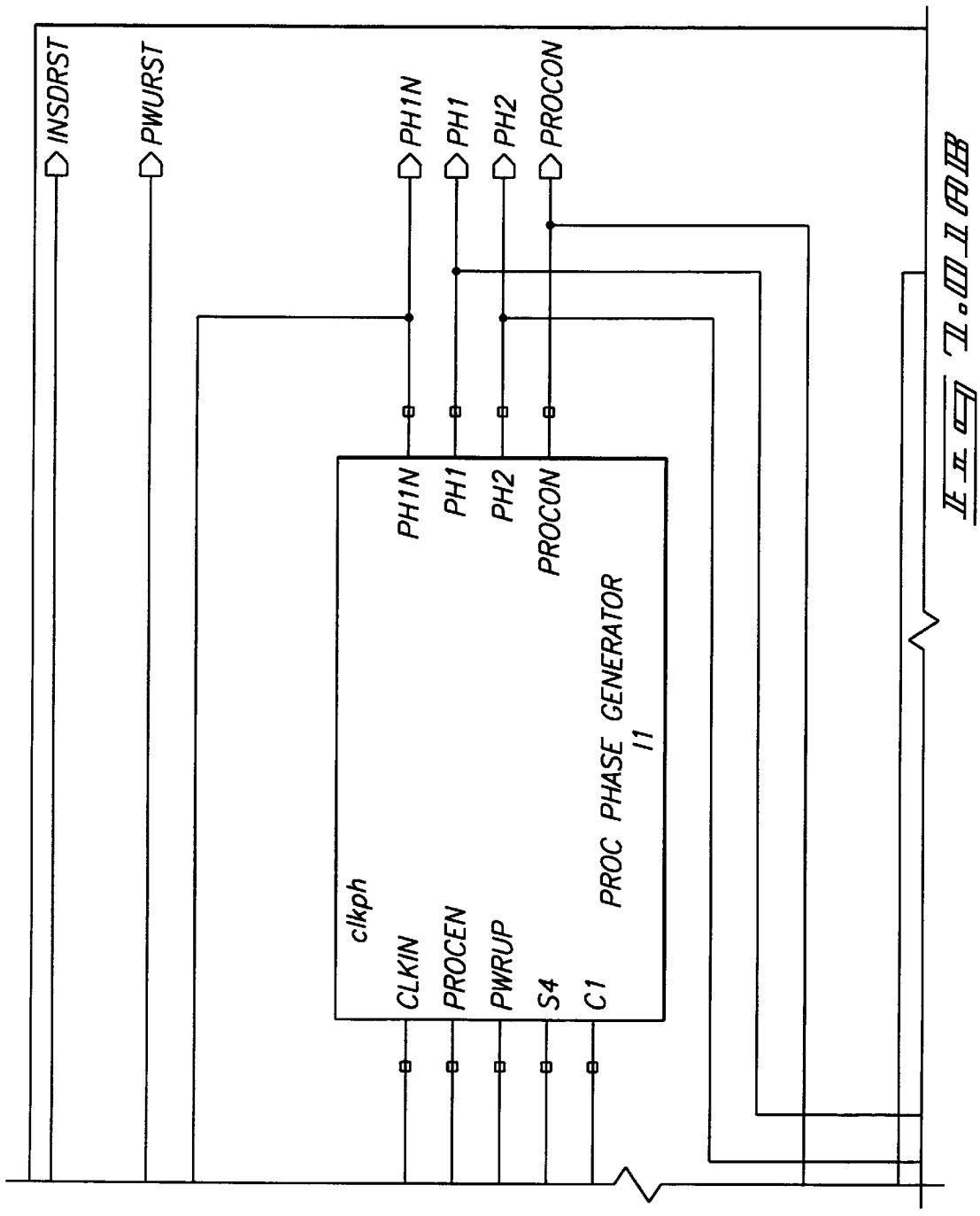

INSDRST
PWURST
PH1N
PH1
PH2
PROCON
clkph
CLKIN
PROCEN
PWRUP
S4
C1
PROC PHASE GENERATOR
I1

FIG. 1.00.1A/1B

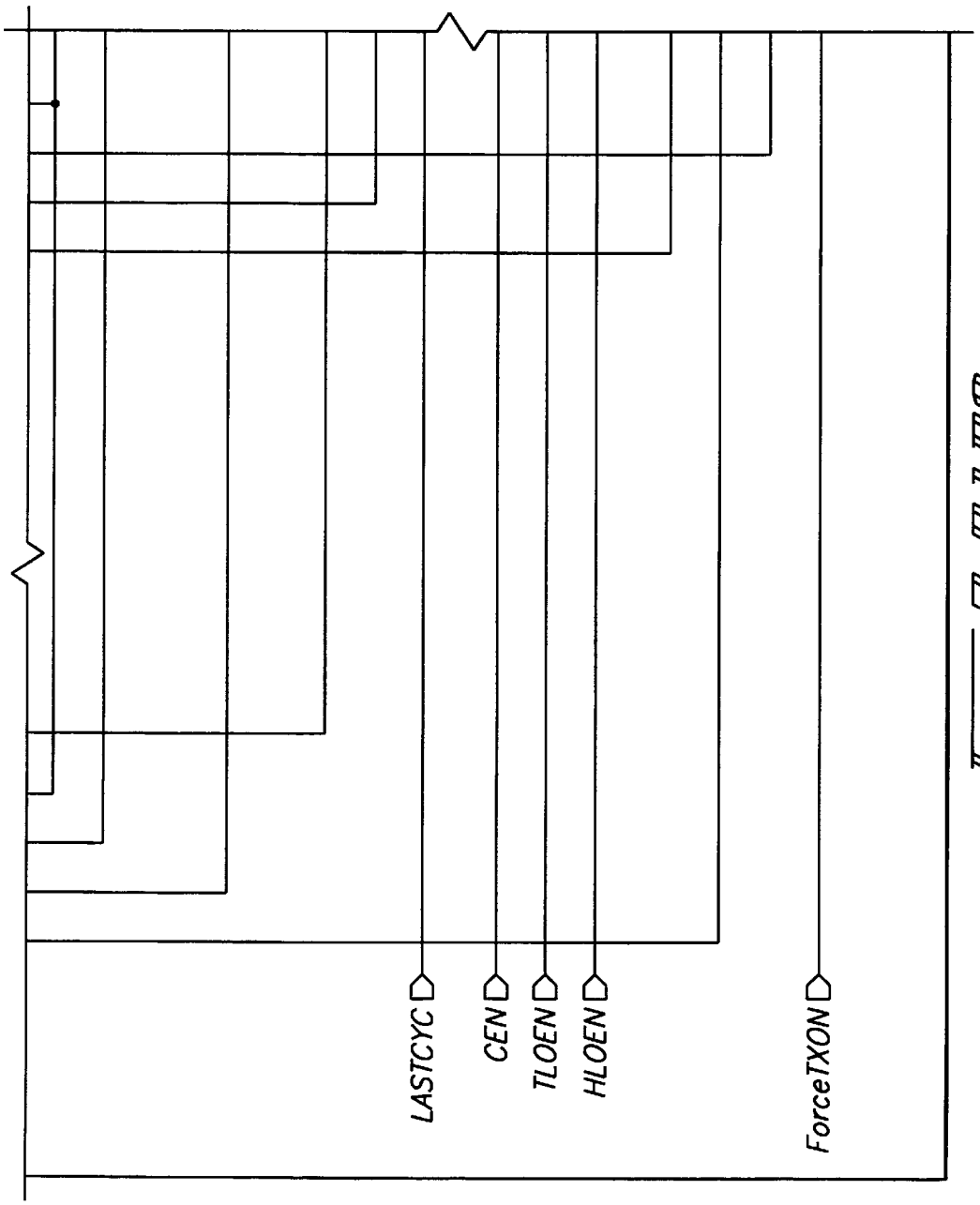


FIG 1.00 IBIA

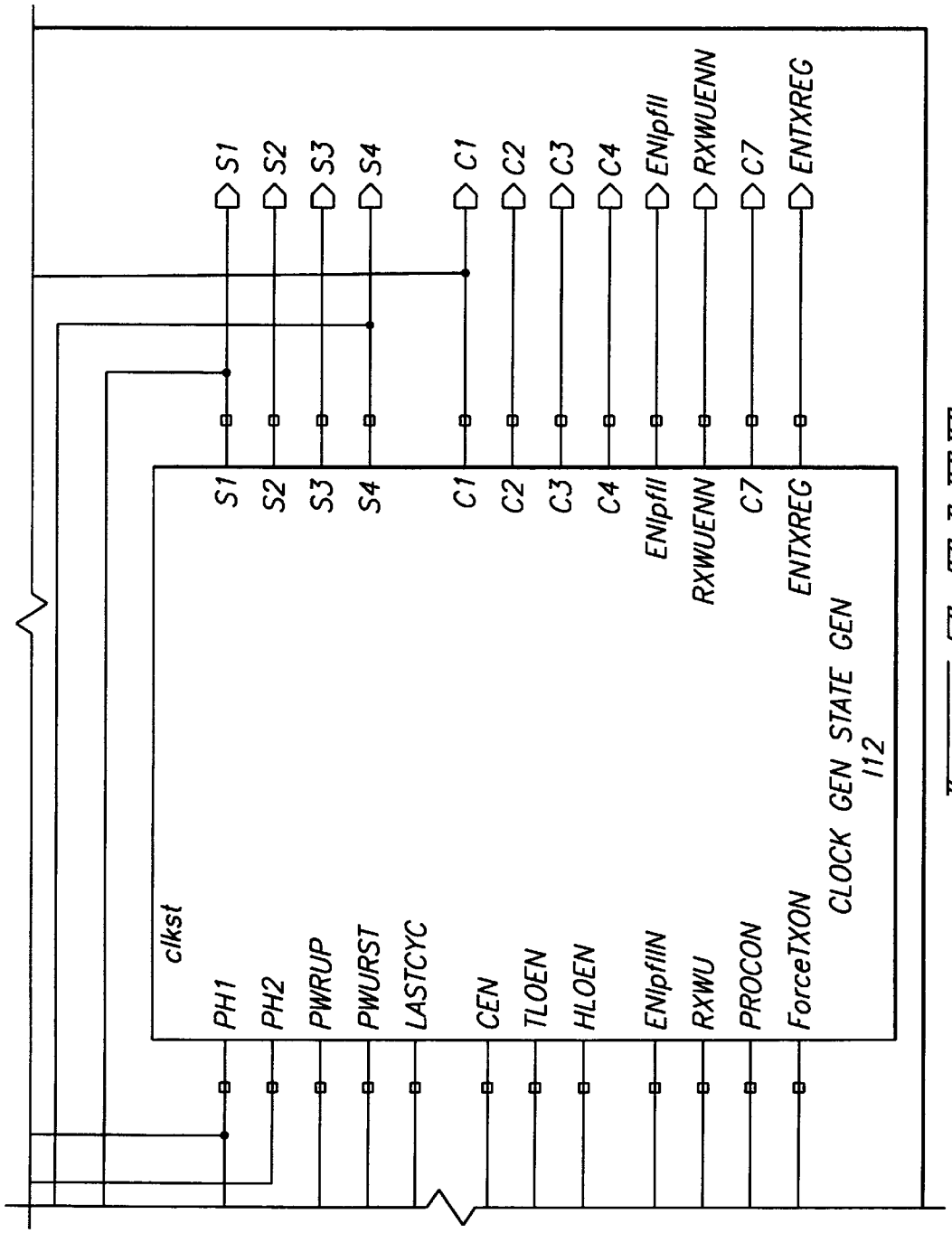

S1
S2
S3
S4
C1
C2
C3
C4
ENIpfIII
RXWUENN
C7
ENTXREG
clkst
PH1
PH2
PWRUP
PWURST
LASTCYC
CEN
TLOEN
HLOEN
ENIpfIIIN
RXWU
PROCON
ForceTXON
CLOCK GEN STATE GEN
112

FIG. 112

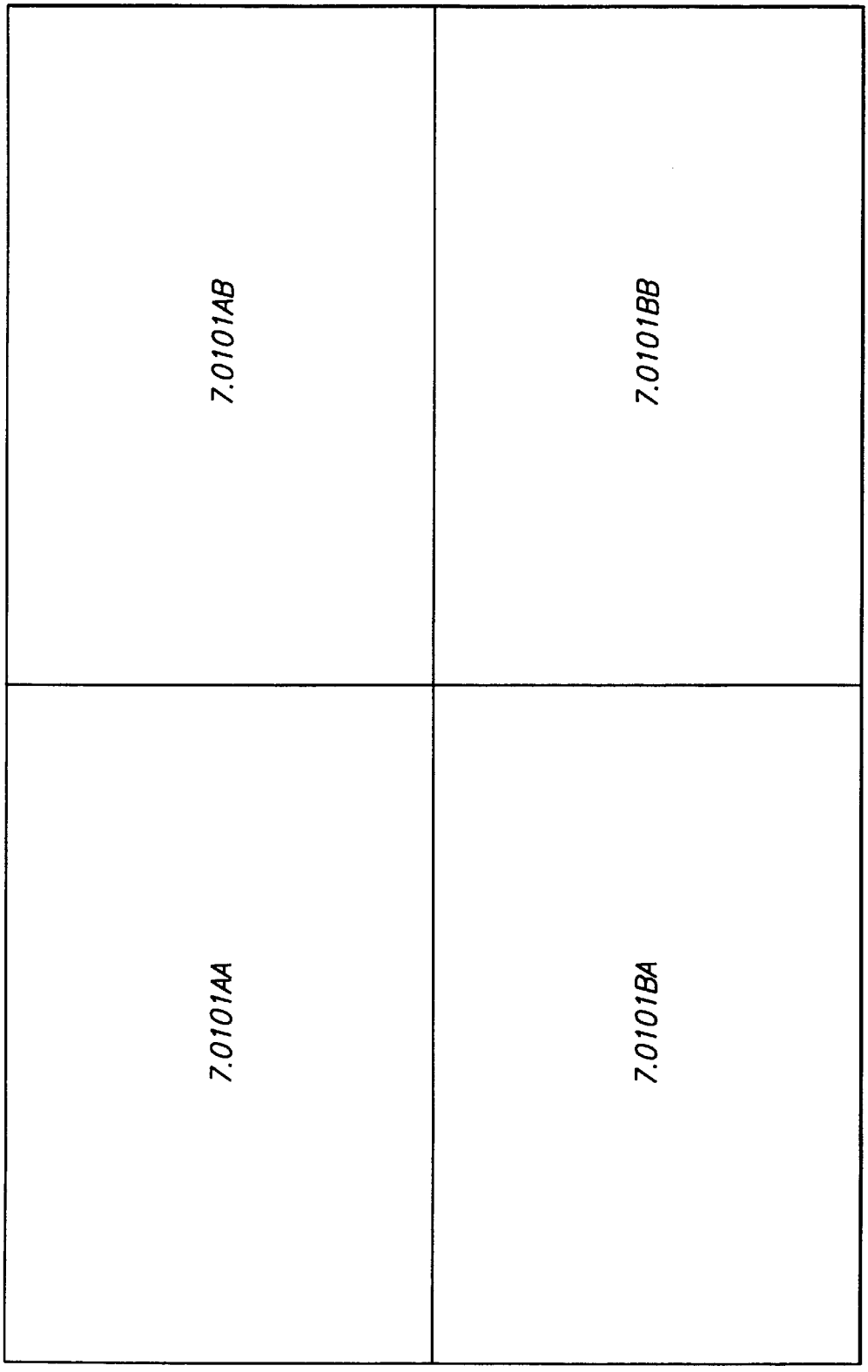


FIG. 7.0101

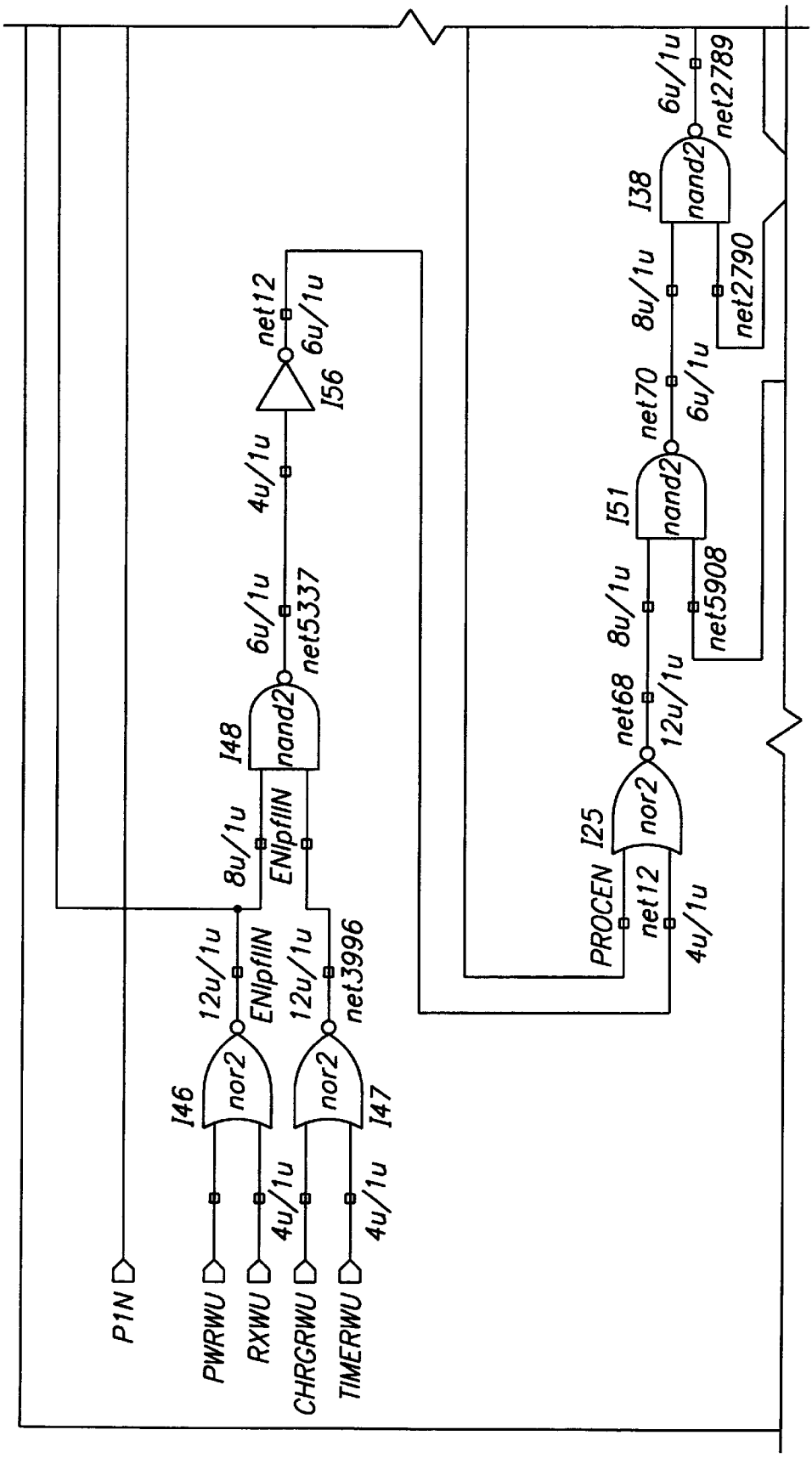

P1N
PWRWU
RXWU
CHRGRWU
TIMERWU
I46
nor2
I47
nor2
12u/1u
ENIpfIIN
4u/1u
12u/1u
net3996
4u/1u
8u/1u
ENIpfIIN
I48
nand2
6u/1u
net5337
4u/1u
net12
I56
6u/1u
PROCEN
I25
nor2
net68
8u/1u
12u/1u
net12
4u/1u
I51
nand2
net70
8u/1u
6u/1u
net5908
I38
nand2
6u/1u
net2789
net2790

FIG. 1.0011AA

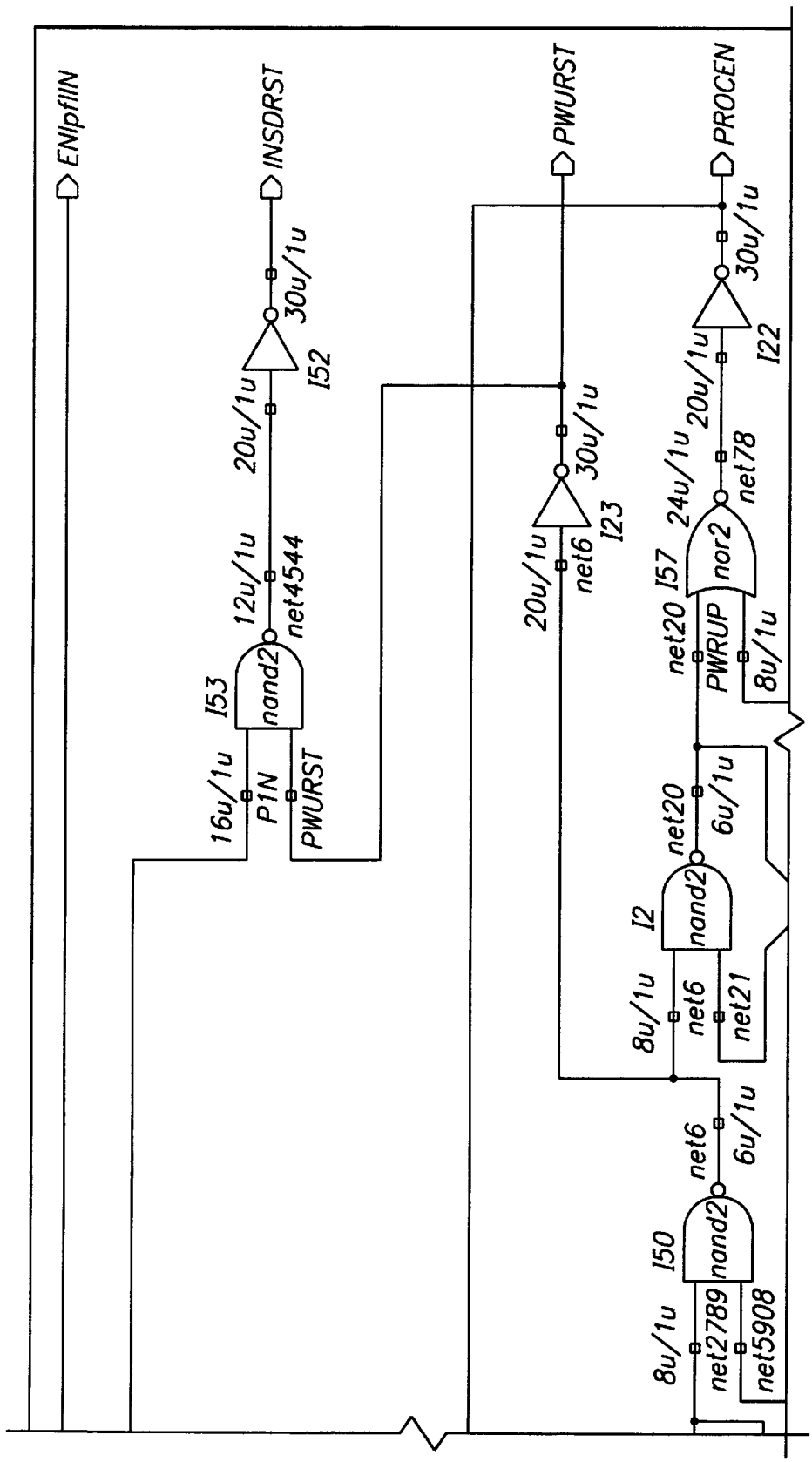

ENIpfIIN
INSDRST
PWURST
PROCEN
30u/1u
I52
20u/1u
12u/1u
net4544
I53
nand2
16u/1u
P1N
PWURST
30u/1u
I23
20u/1u
net6
24u/1u
20u/1u
net78
I57
nor2
net20
PWRUP
8u/1u
I22
6u/1u
net20
I2
nand2
8u/1u
net6
net21
6u/1u
net6
I50
nand2
8u/1u
net2789
net5908

FIG. 1.0011AB

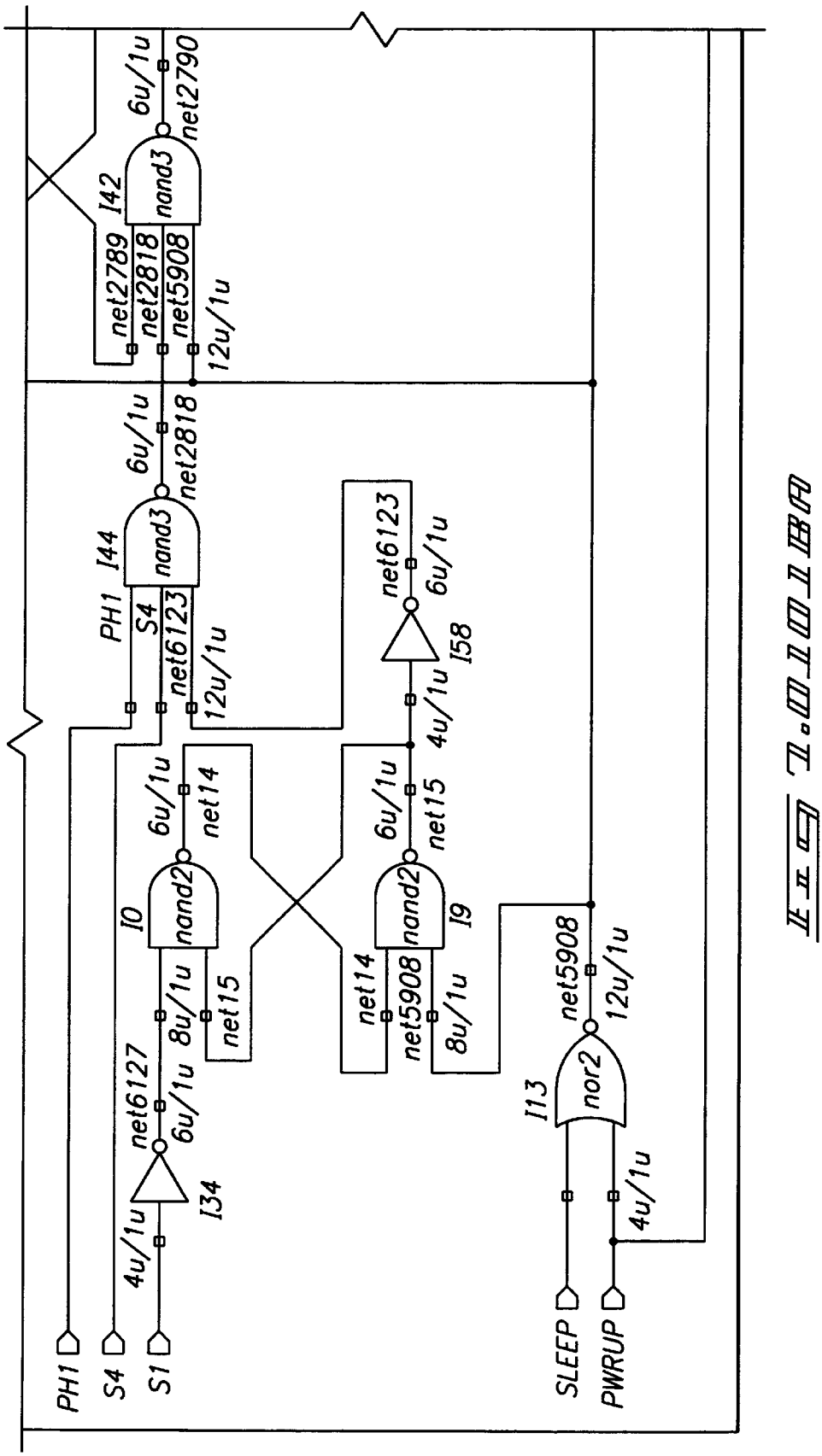

PH1
S4
S1
SLEEP
PWRUP
I34
I0
I9
I58
I42
I44
I13
nand2
nand3
nor2
net6127
net6123
net14
net15
net5908
net2789
net2818
net2790
6u/1u
8u/1u
4u/1u
12u/1u

FIG. 1.00 BB

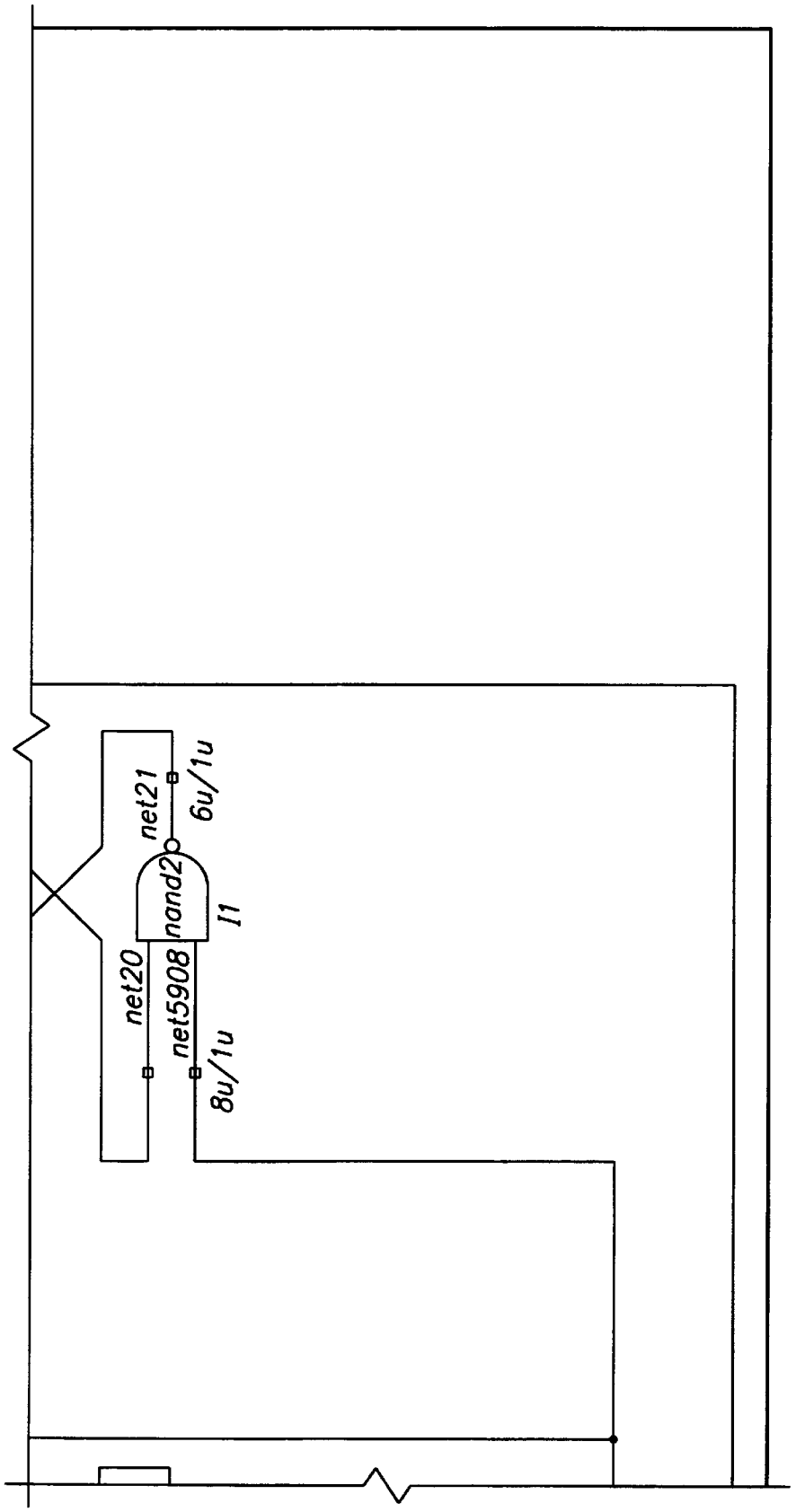


FIG. 137

7.0102AE	7.0102AF	7.0102AG	7.0102AH	7.0102AI	7.0102AJ						
7.0102BE	7.0102BF	7.0102BG	7.0102BH	7.0102BI	7.0102BJ						
7.0102CE	7.0102CF	7.0102CG	7.0102CH	7.0102CI	7.0102CJ						
7.0102DE	7.0102DF	7.0102DG	7.0102DH	7.0102DI	7.0102DJ						
7.0102BD	7.0102BC	7.0102BB	7.0102BA								
7.0102CD	7.0102CC	7.0102CB	7.0102CA								
7.0102DD	7.0102DC	7.0102DB	7.0102DA								

FIG. 7.0102

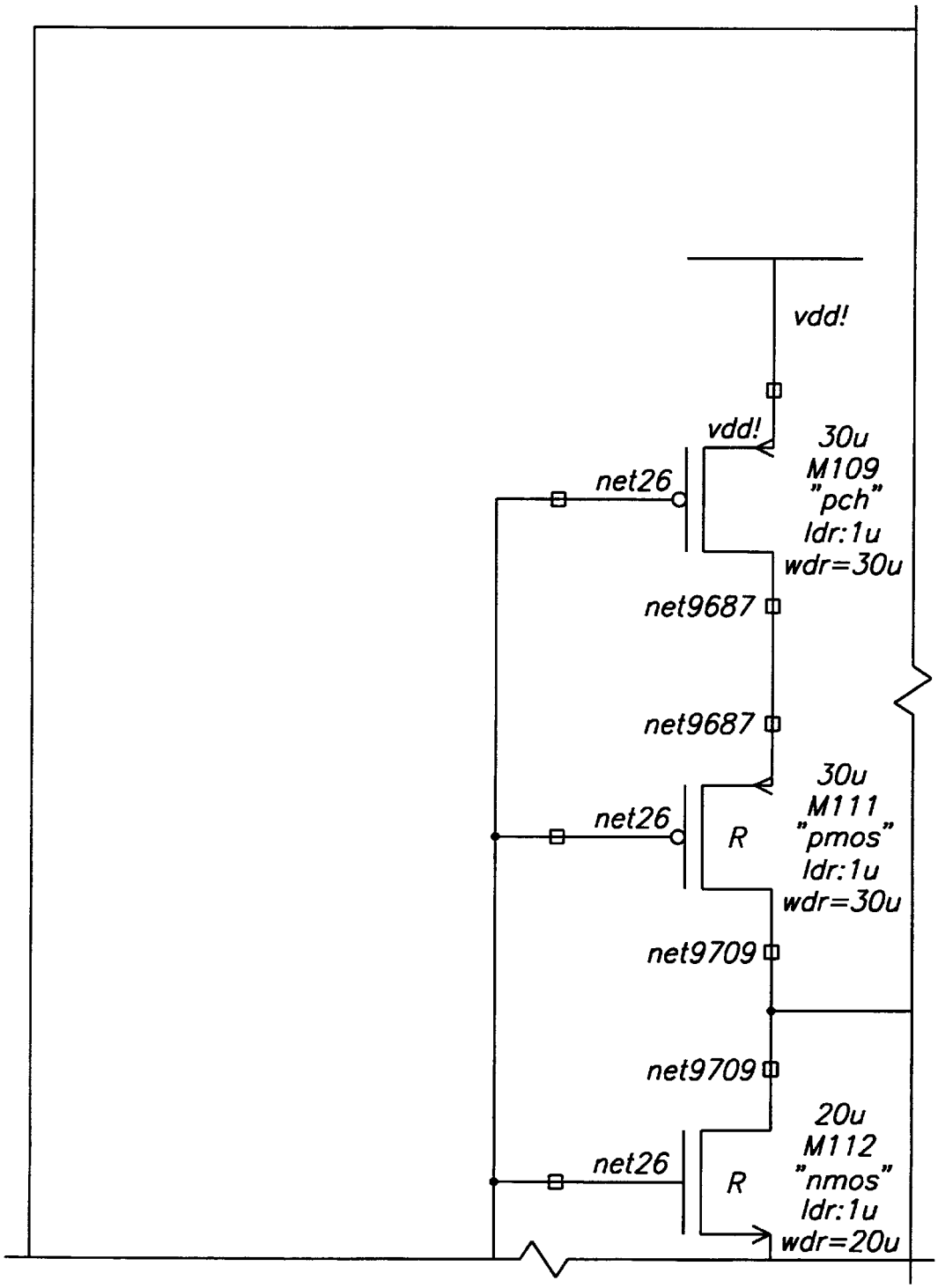

vdd!
vdd!
30u
M109
"pch"
ldr:1u
wdr=30u
net26
net9687
net9687
30u
M111
"pmos"
ldr:1u
wdr=30u
net26
R
net9709
net9709
20u
M112
"nmos"
ldr:1u
wdr=20u
net26
R

Fig 1.0102AE

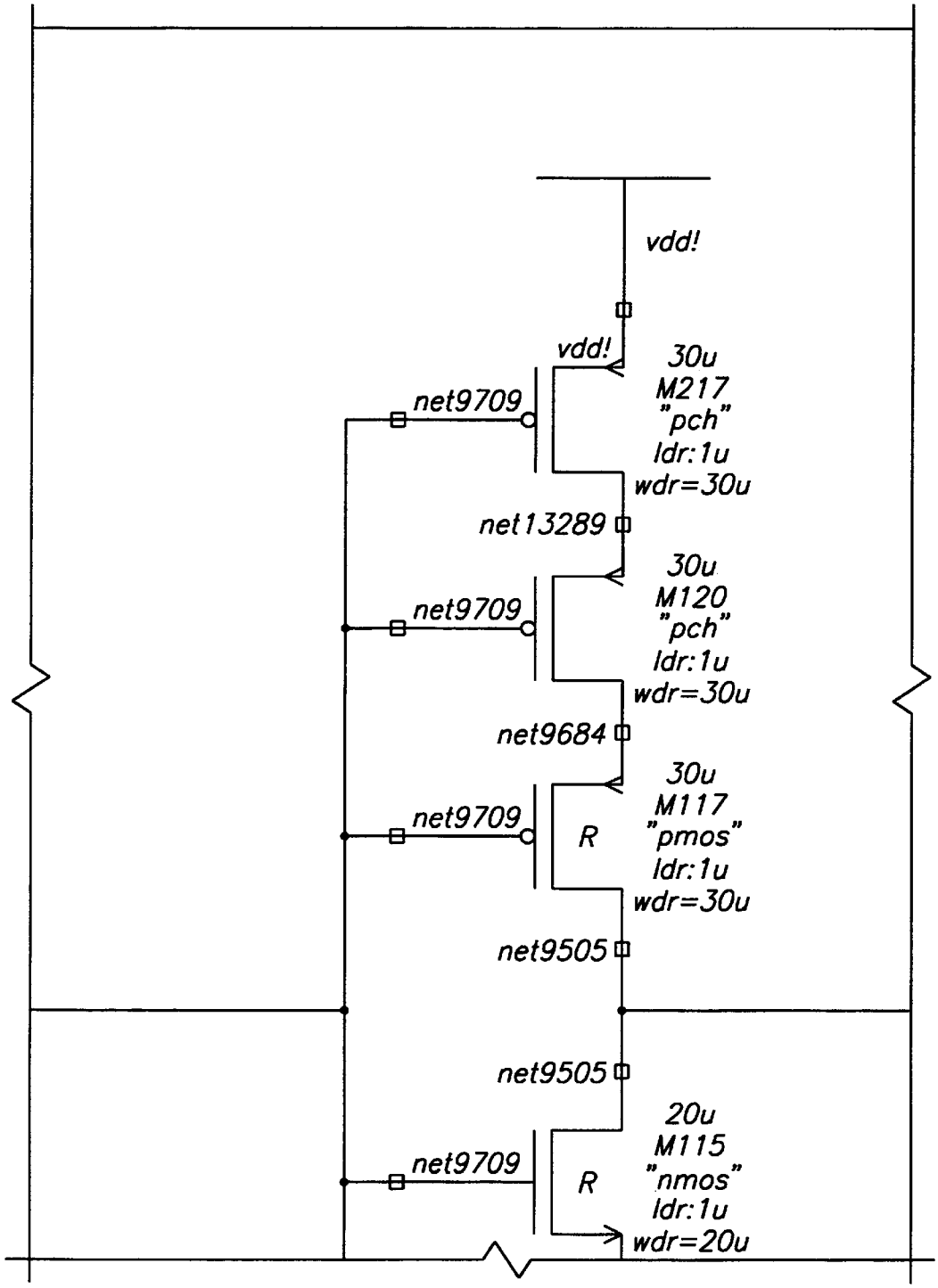

vdd!
vdd!
30u
M217
"pch"
ldr:1u
wdr=30u
net9709
net13289
30u
M120
"pch"
ldr:1u
wdr=30u
net9709
net9684
30u
M117
"pmos"
ldr:1u
wdr=30u
net9709
R
net9505
net9505
20u
M115
"nmos"
ldr:1u
wdr=20u
net9709
R

Fig 1.0102AF

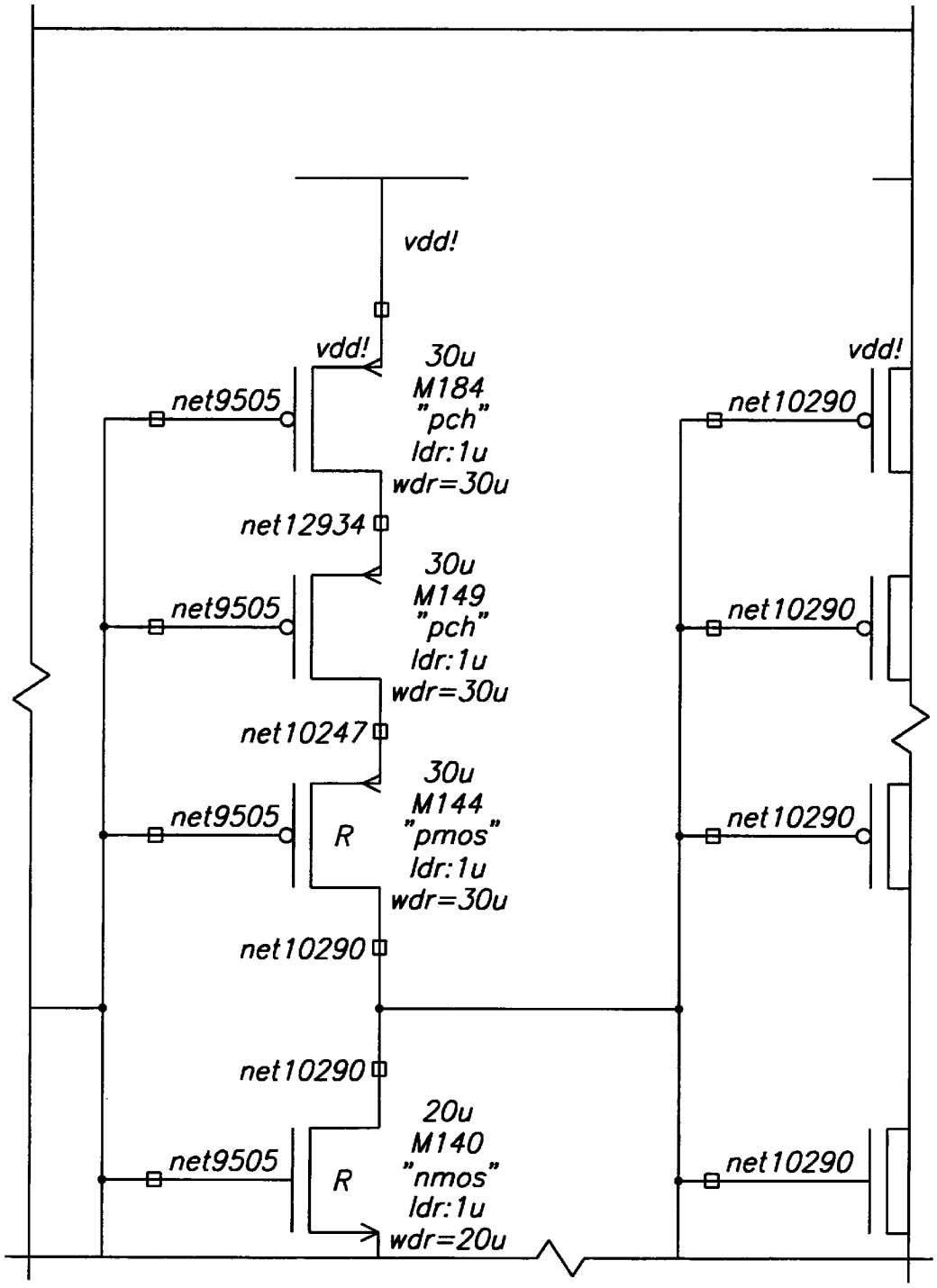

vdd!
vdd!
30u
M184
"pch"
ldr:1u
wdr=30u
net9505
net12934
30u
M149
"pch"
ldr:1u
wdr=30u
net9505
net10247
30u
M144
"pmos"
ldr:1u
wdr=30u
net9505
R
net10290
net10290
20u
M140
"nmos"
ldr:1u
wdr=20u
net9505
R
vdd!
net10290
net10290
net10290
net10290

Fig 1.0102AG

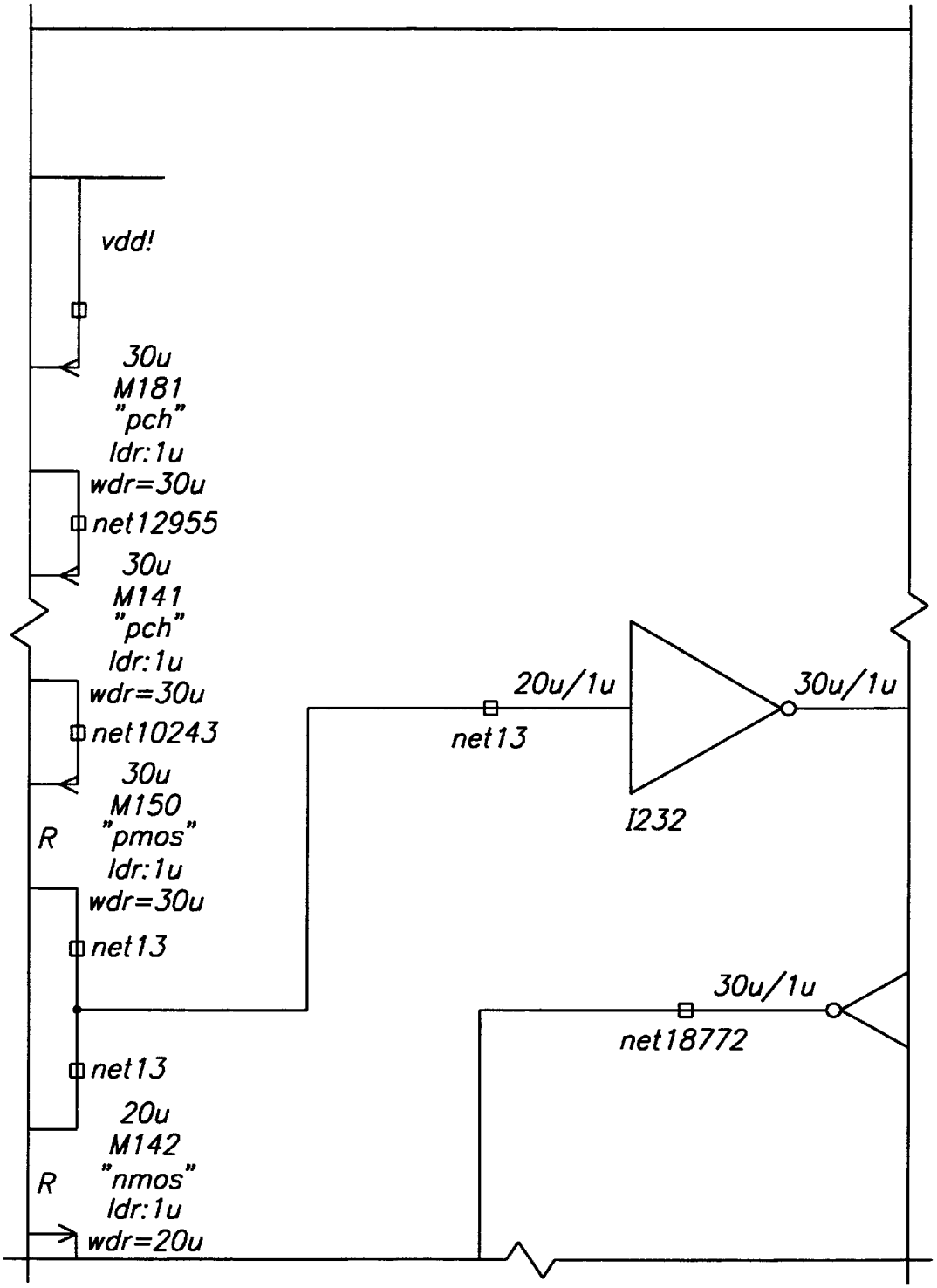

vdd!
30u
M181
"pch"
ldr:1u
wdr=30u
net12955
30u
M141
"pch"
ldr:1u
wdr=30u
net10243
30u
M150
"pmos"
ldr:1u
wdr=30u
net13
net13
20u
M142
"nmos"
ldr:1u
wdr=20u
R
R
20u/1u
net13
30u/1u
I232
30u/1u
net18772

FIG 1.0102AH

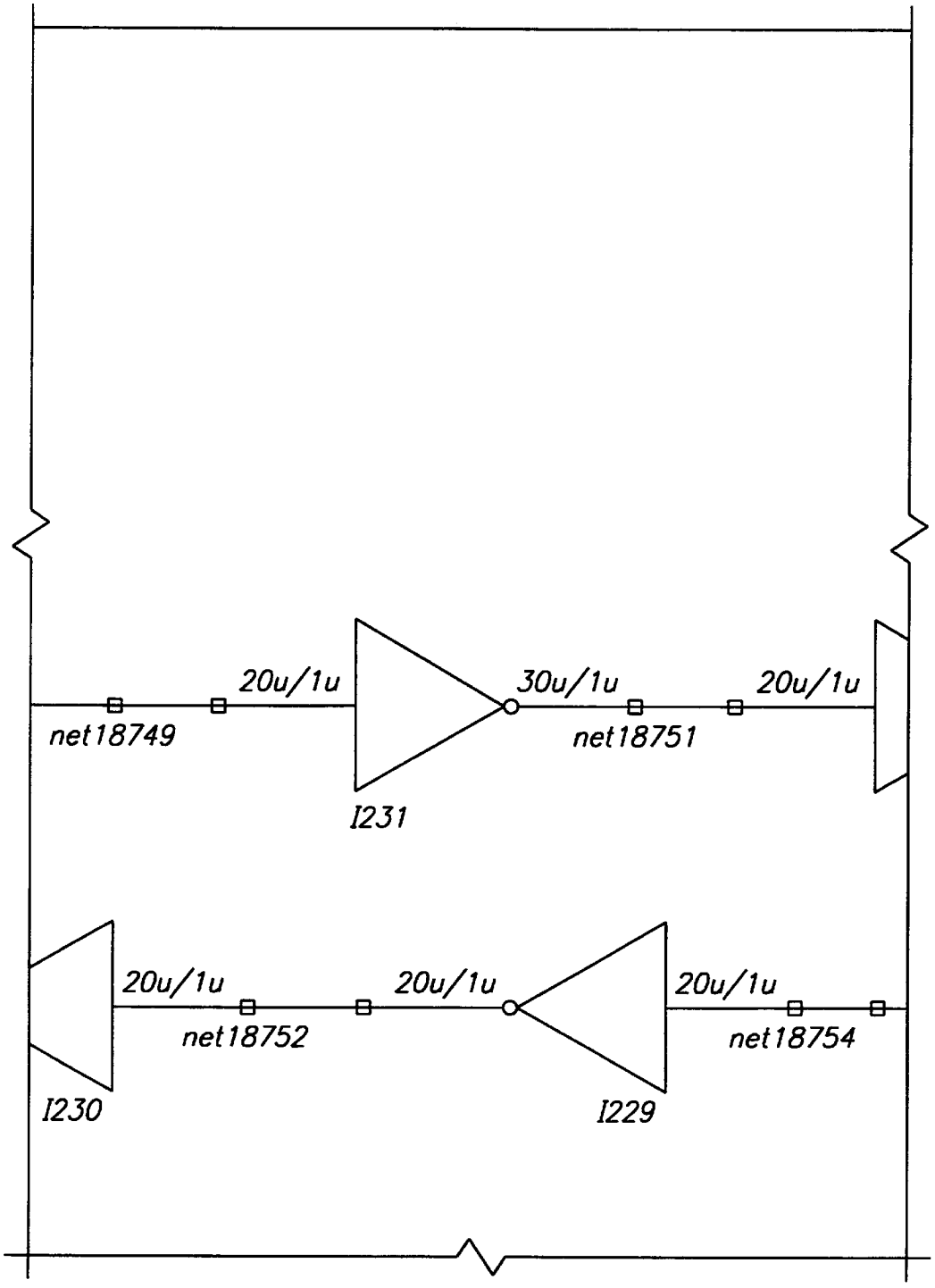

20u/1u
30u/1u
20u/1u
net18749
net18751
I231
20u/1u
20u/1u
20u/1u
net18752
net18754
I230
I229

FIG 1.0102AI

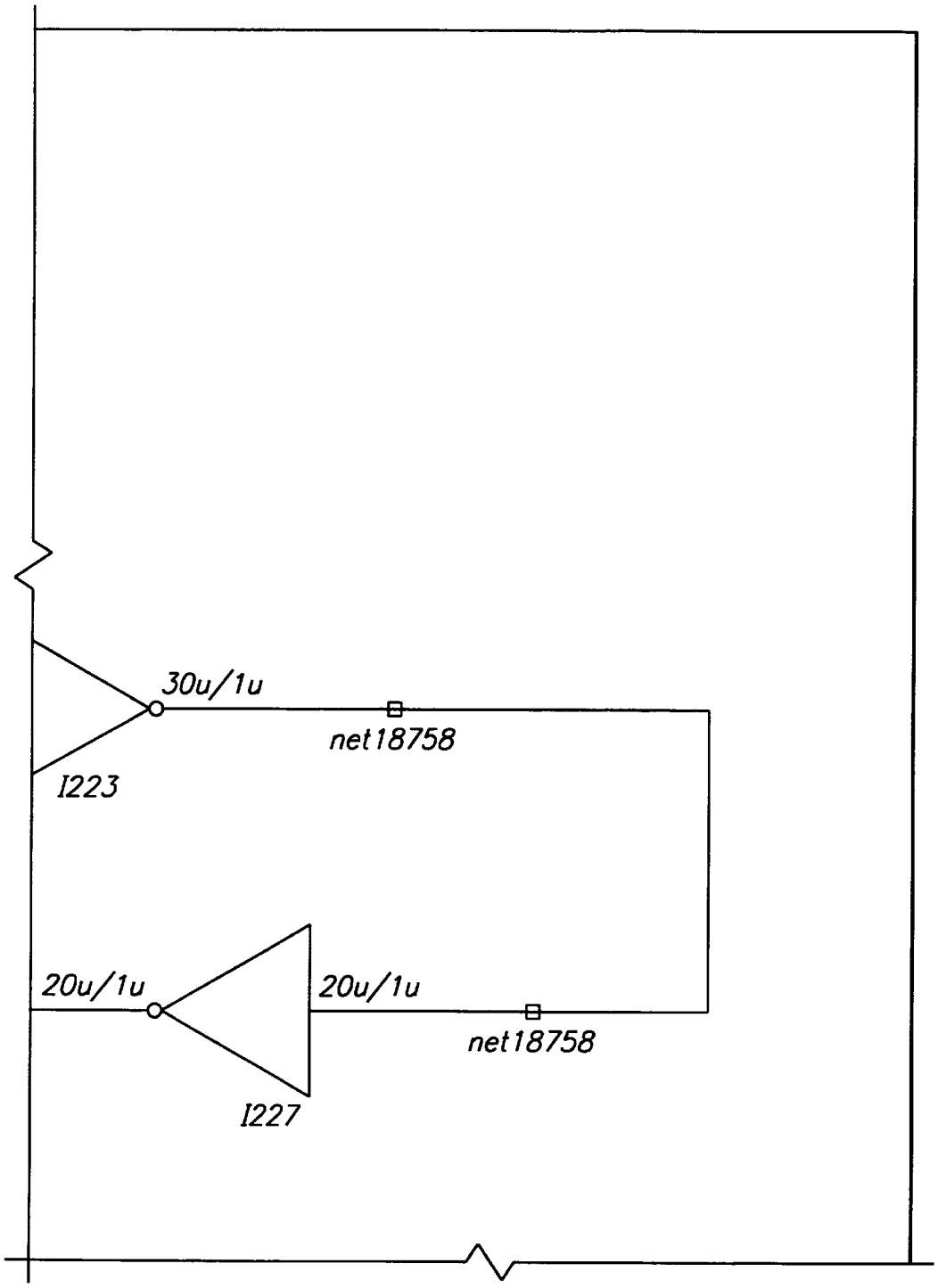


Fig 1.0102A

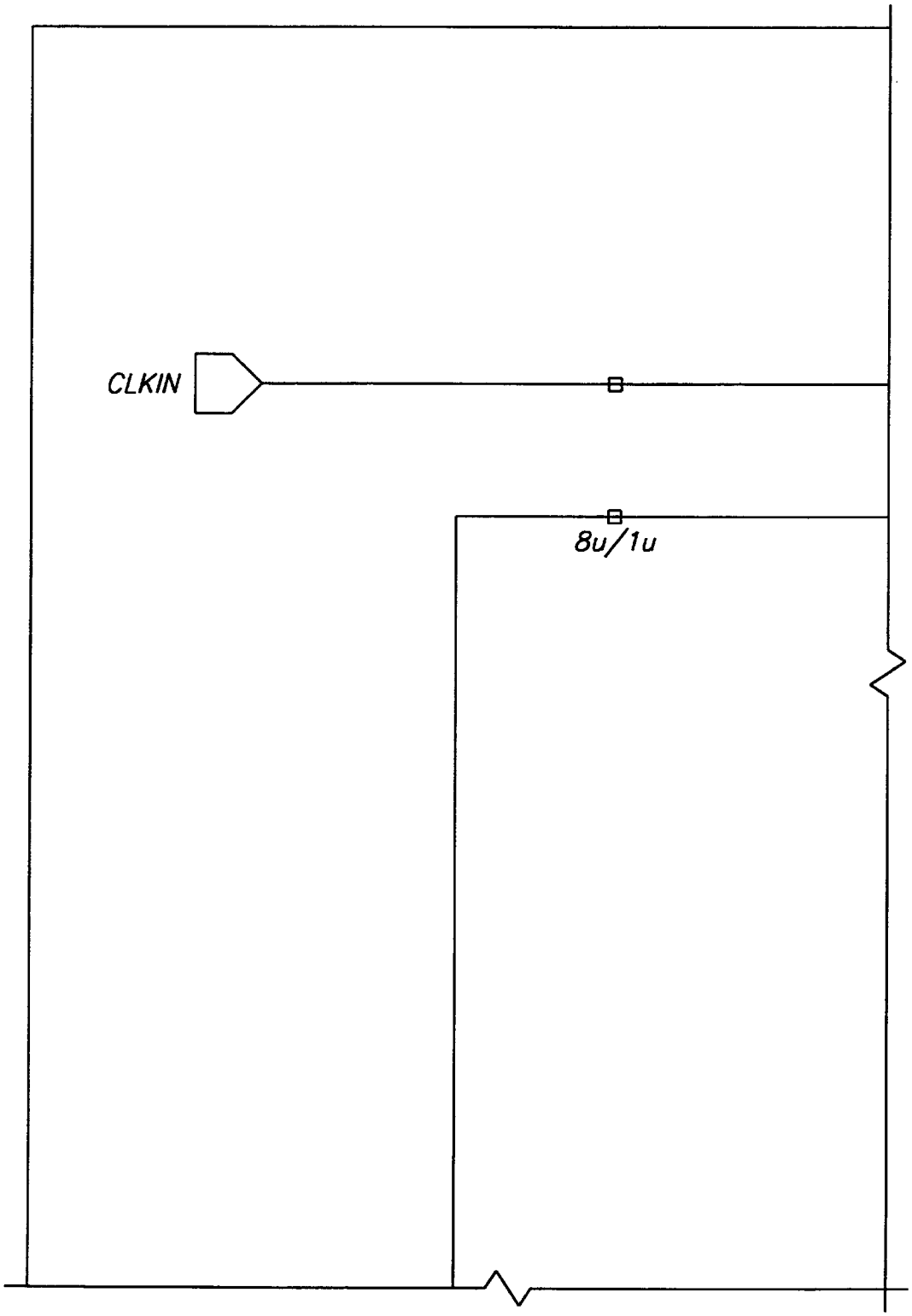


Fig 1.0102BA

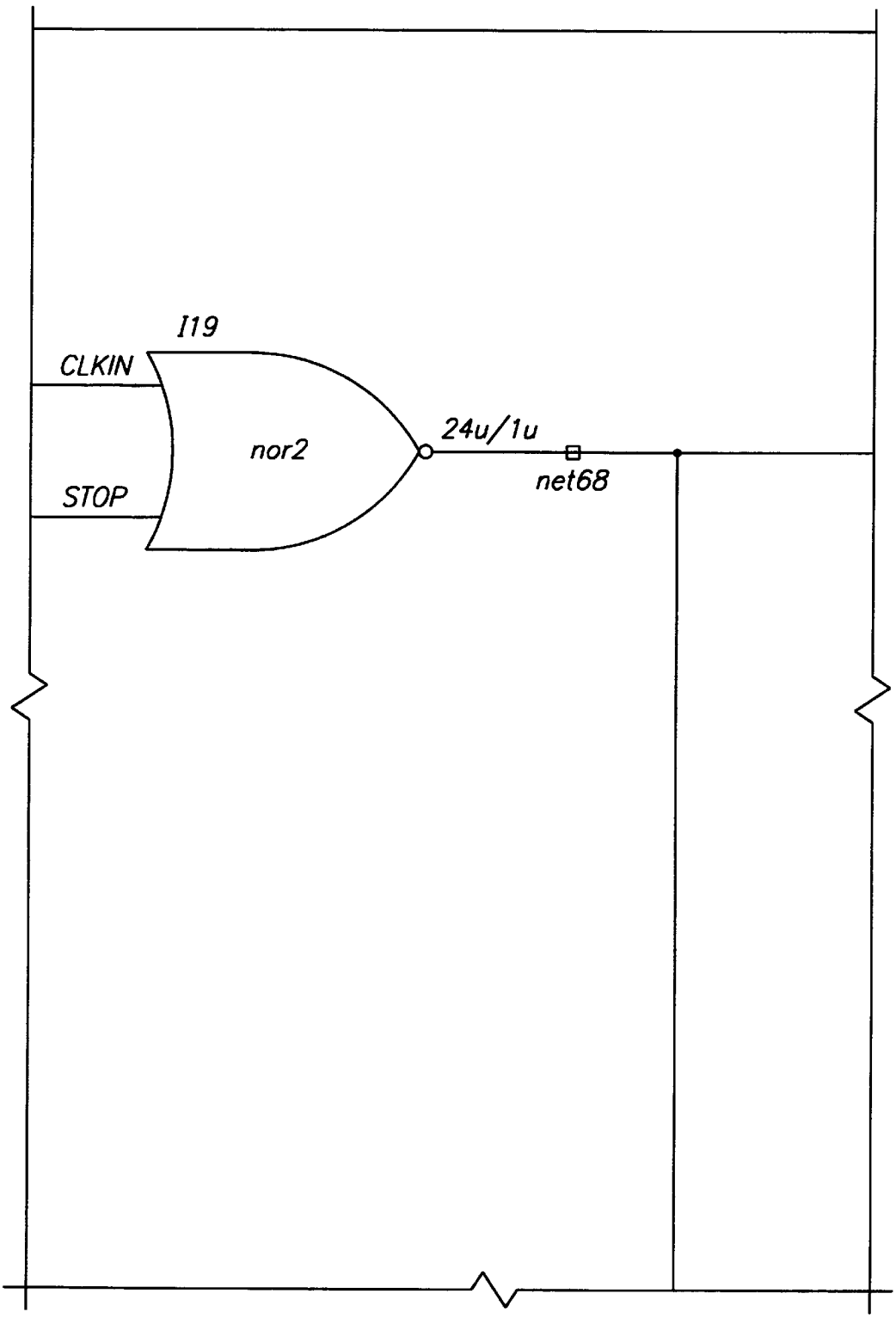


Fig 1.0102BB

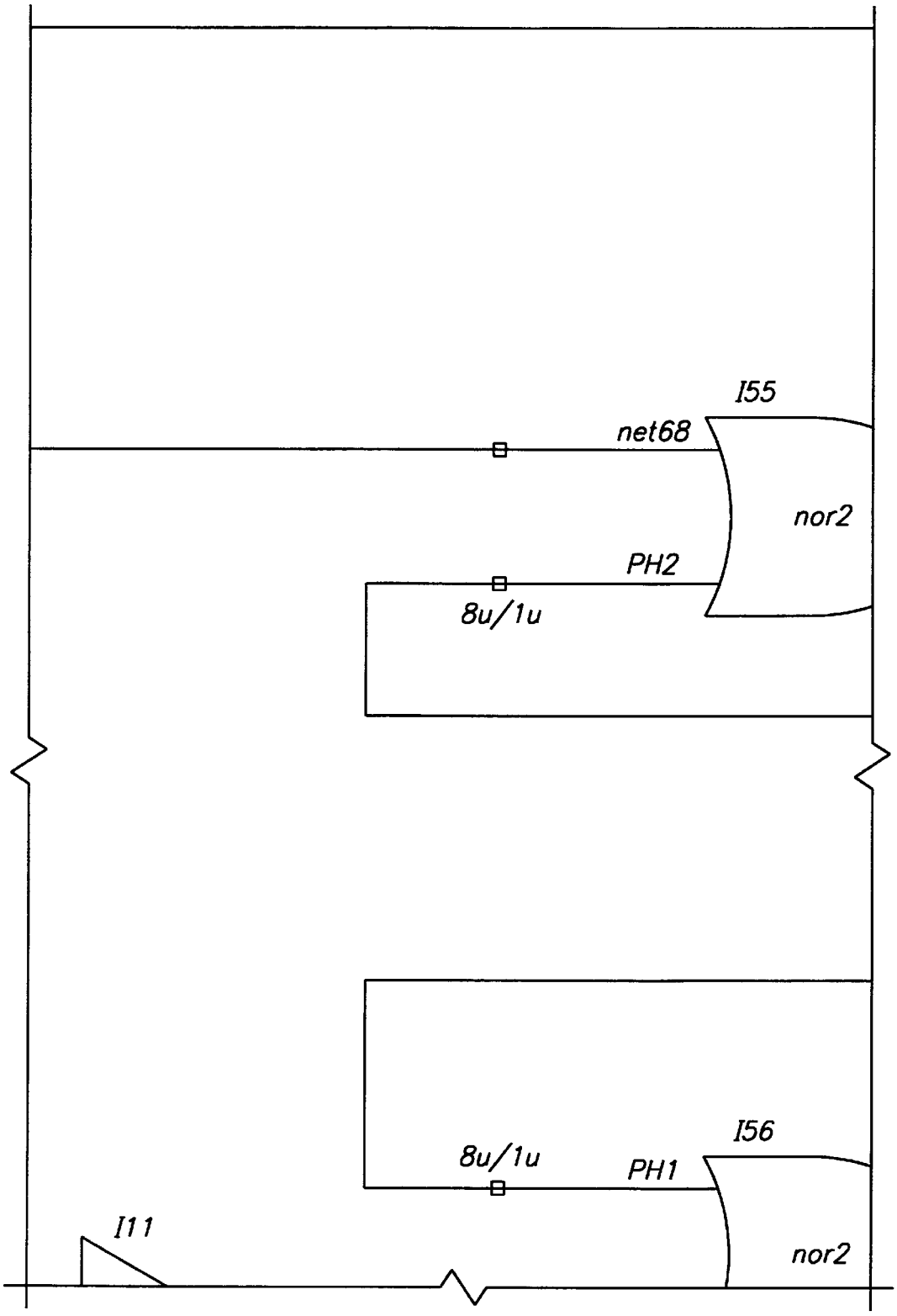


Fig 1.0102BC

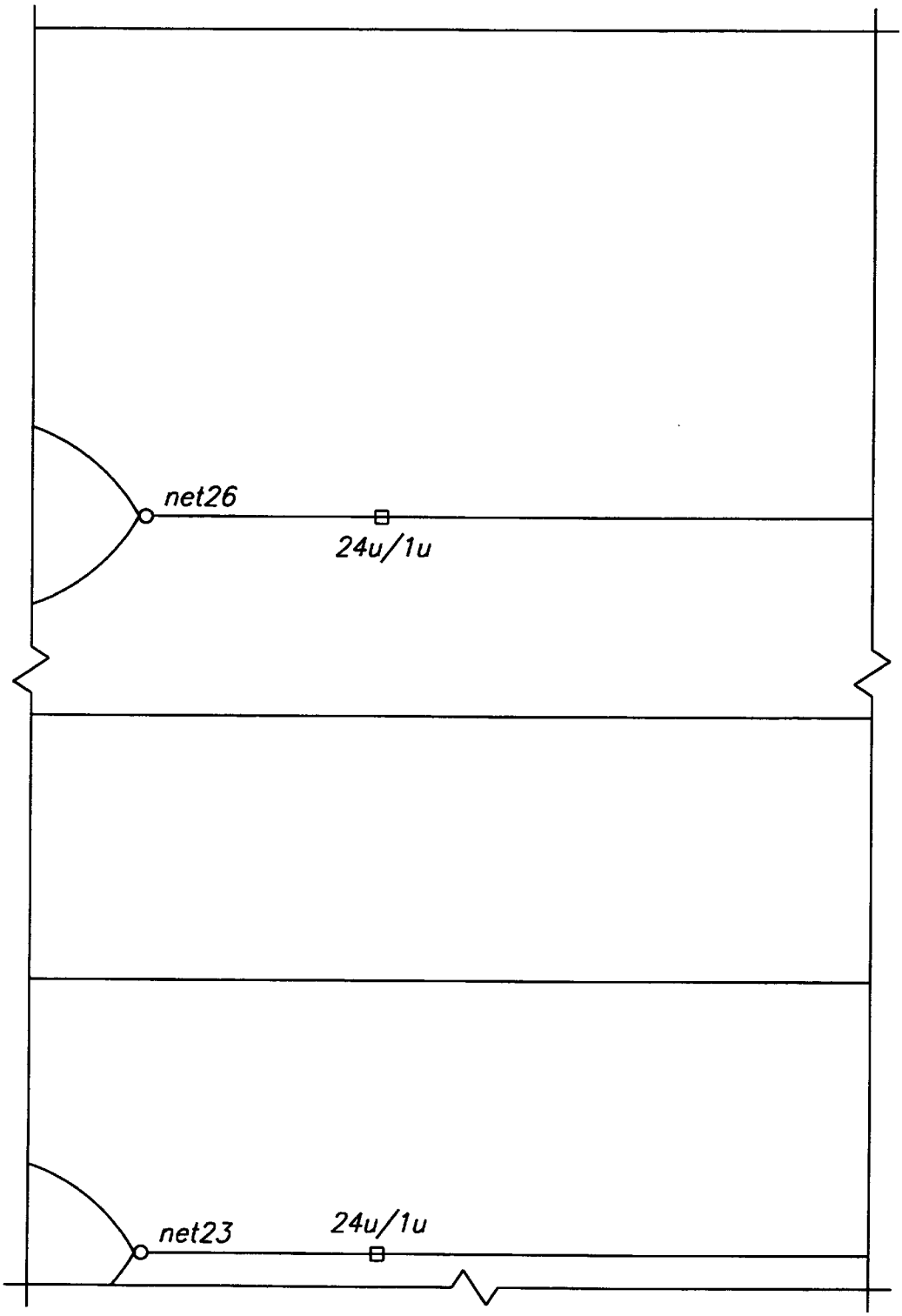


Fig 1.0102BD

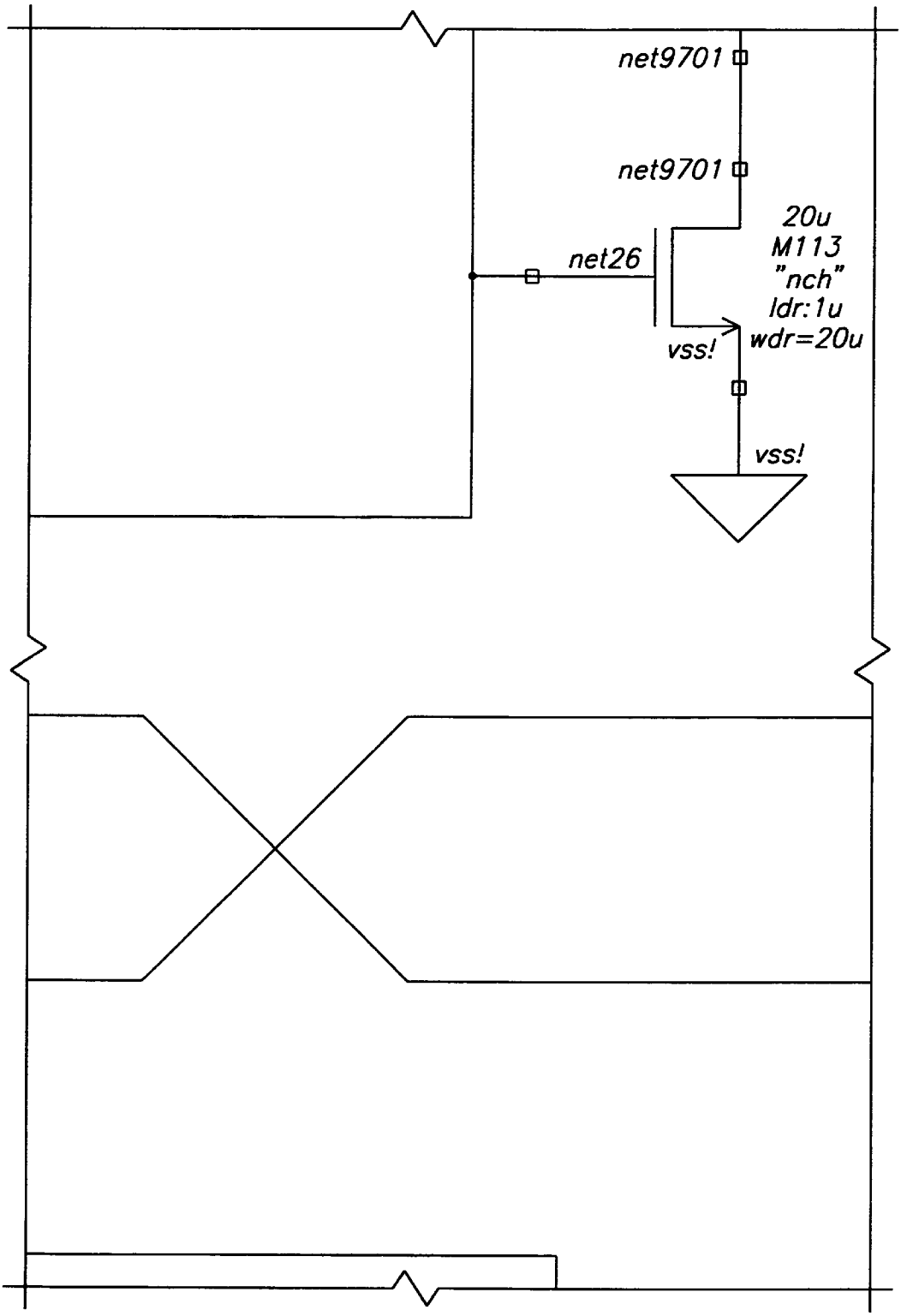
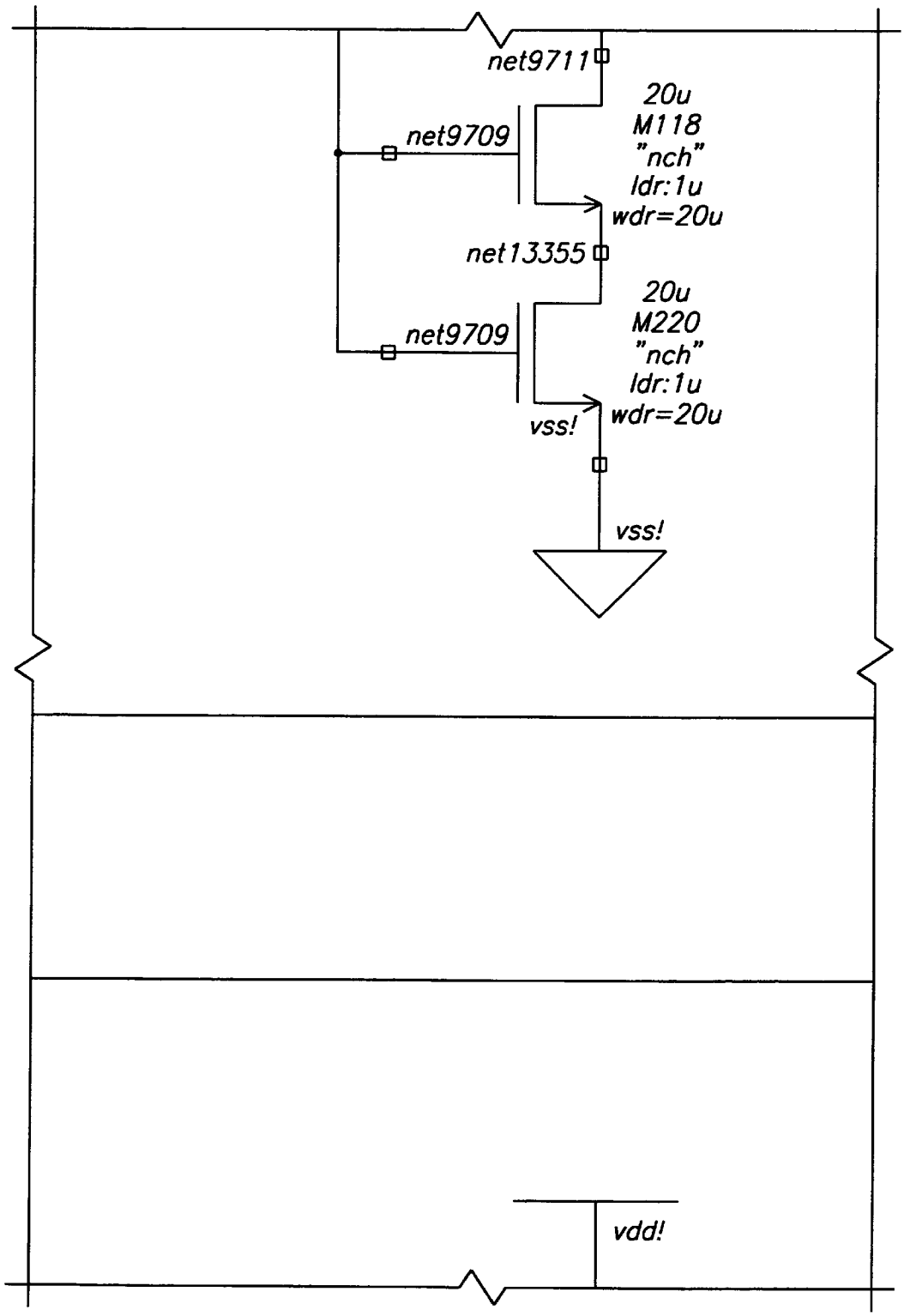


Fig 1.0102BE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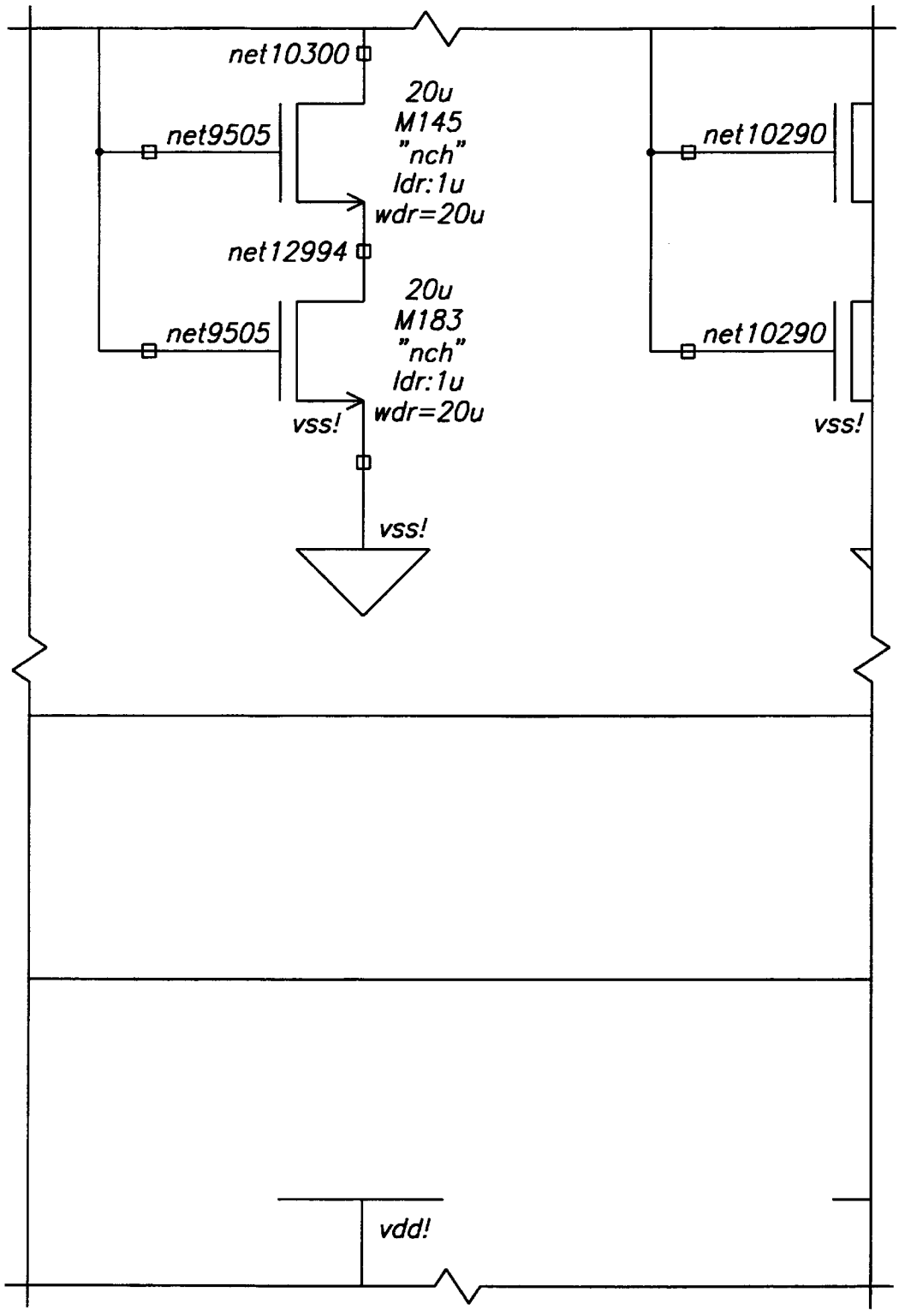
20u
M118
"nch"
ldr:1u
wdr=20u
net9709
net13355
20u
M220
"nch"
ldr:1u
wdr=20u
net9709
vss!
vss!
vdd!

Fig 1.0102BF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20u
M145
"nch"
ldr:1u
wdr=20u
net9505
net10290
net12994
20u
M183
"nch"
ldr:1u
wdr=20u
net9505
net10290
vss!
vss!
vss!
vdd!

Fig 1.0102B6

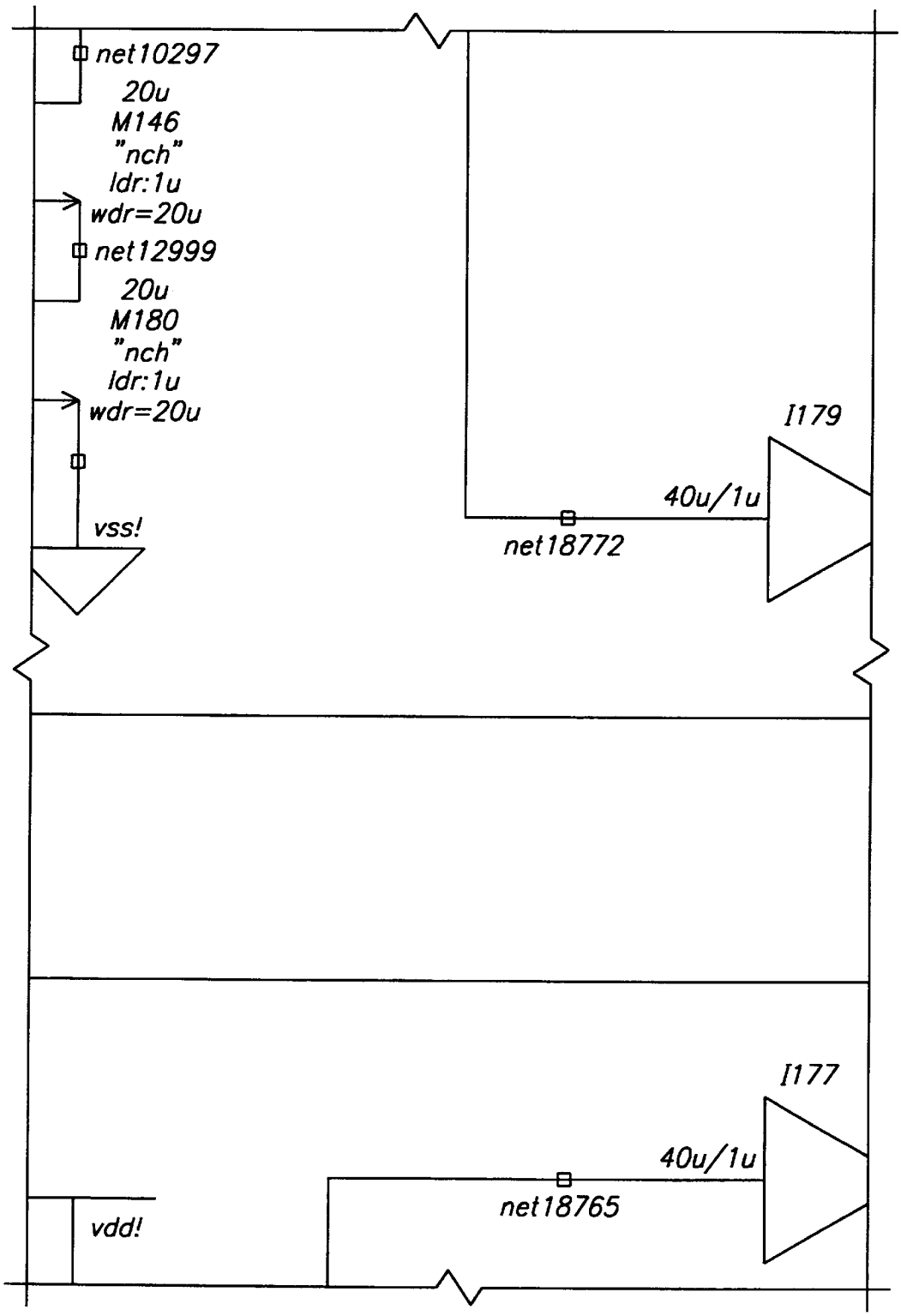

net10297
20u
M146
"nch"
ldr:1u
wdr=20u
net12999
20u
M180
"nch"
ldr:1u
wdr=20u
vss!
I179
40u/1u
net18772
I177
40u/1u
net18765
vdd!

Fig 1.0102BH

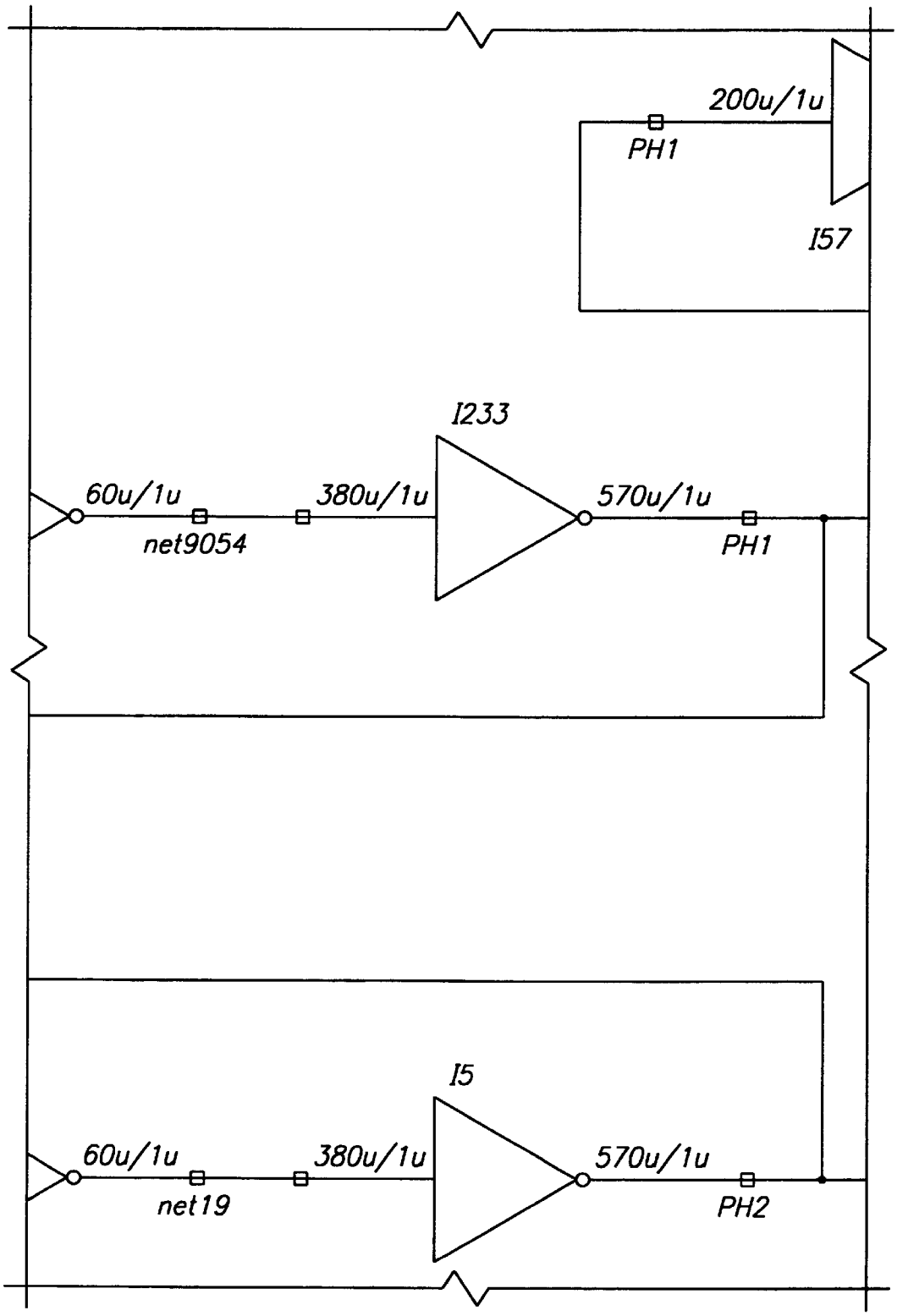

200u/1u
PH1
I57
I233
60u/1u
380u/1u
570u/1u
net9054
PH1
I5
60u/1u
380u/1u
570u/1u
net19
PH2

Fig 1.0102BI

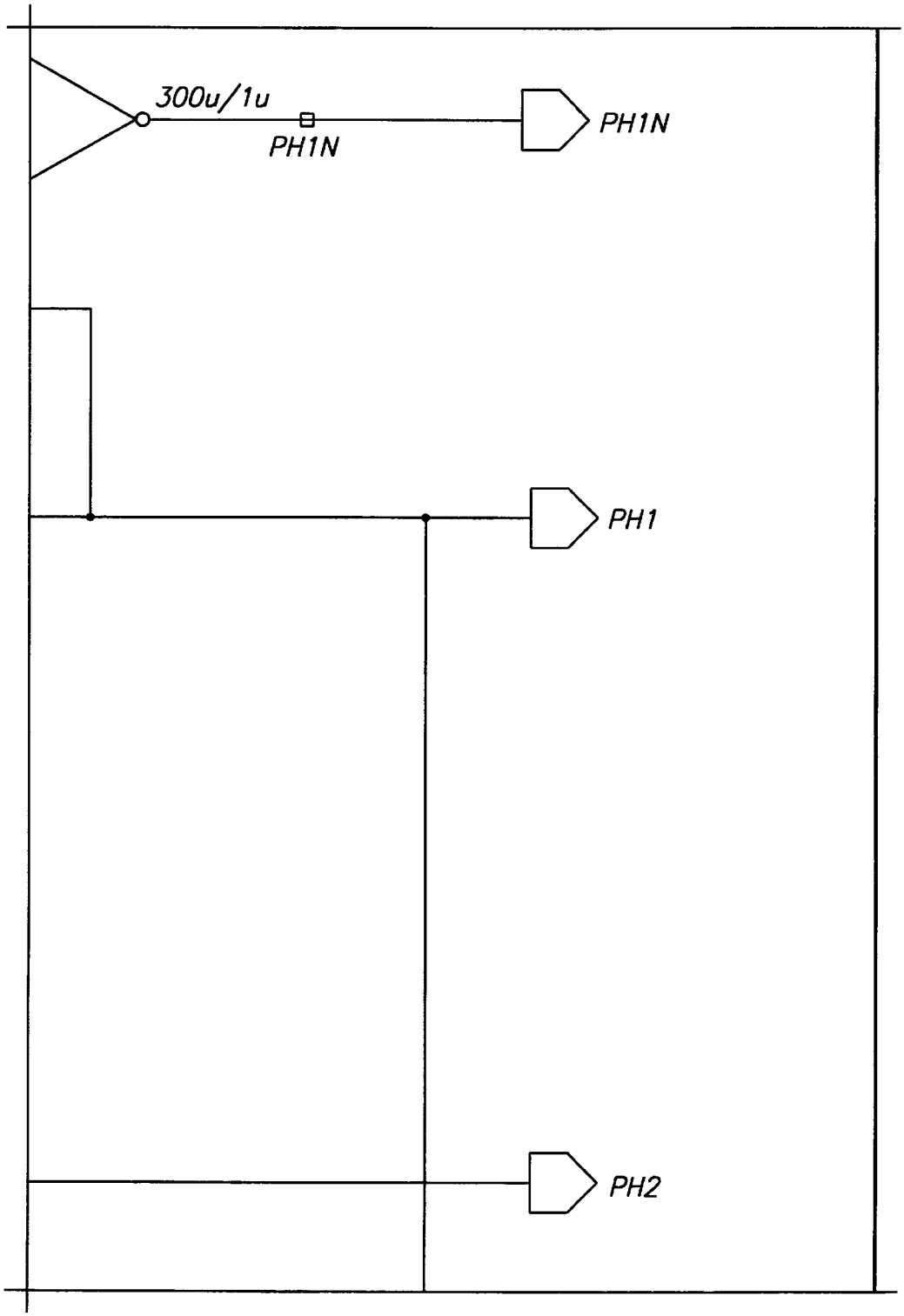


Fig 1.0110Bd

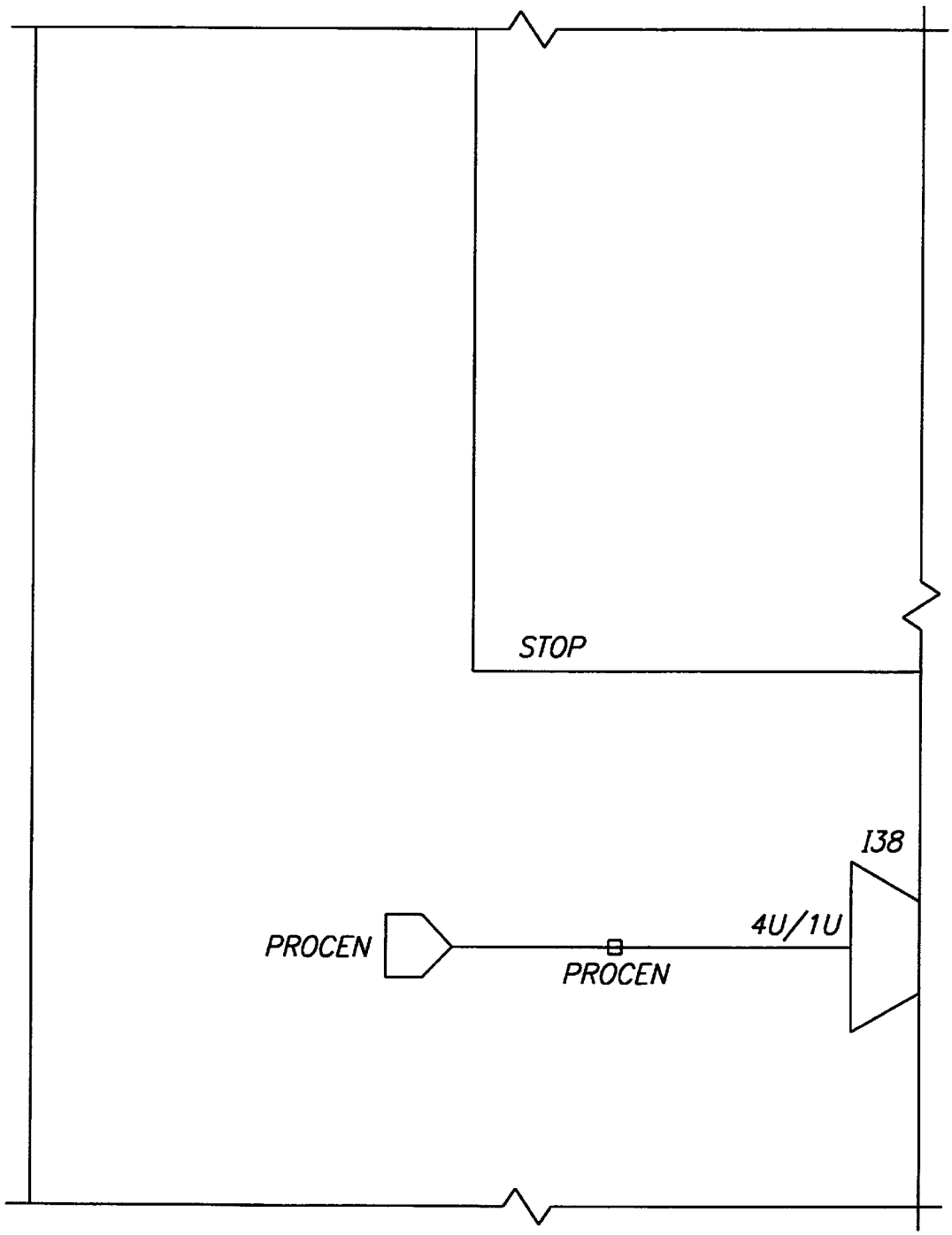


Fig 1.0102CA

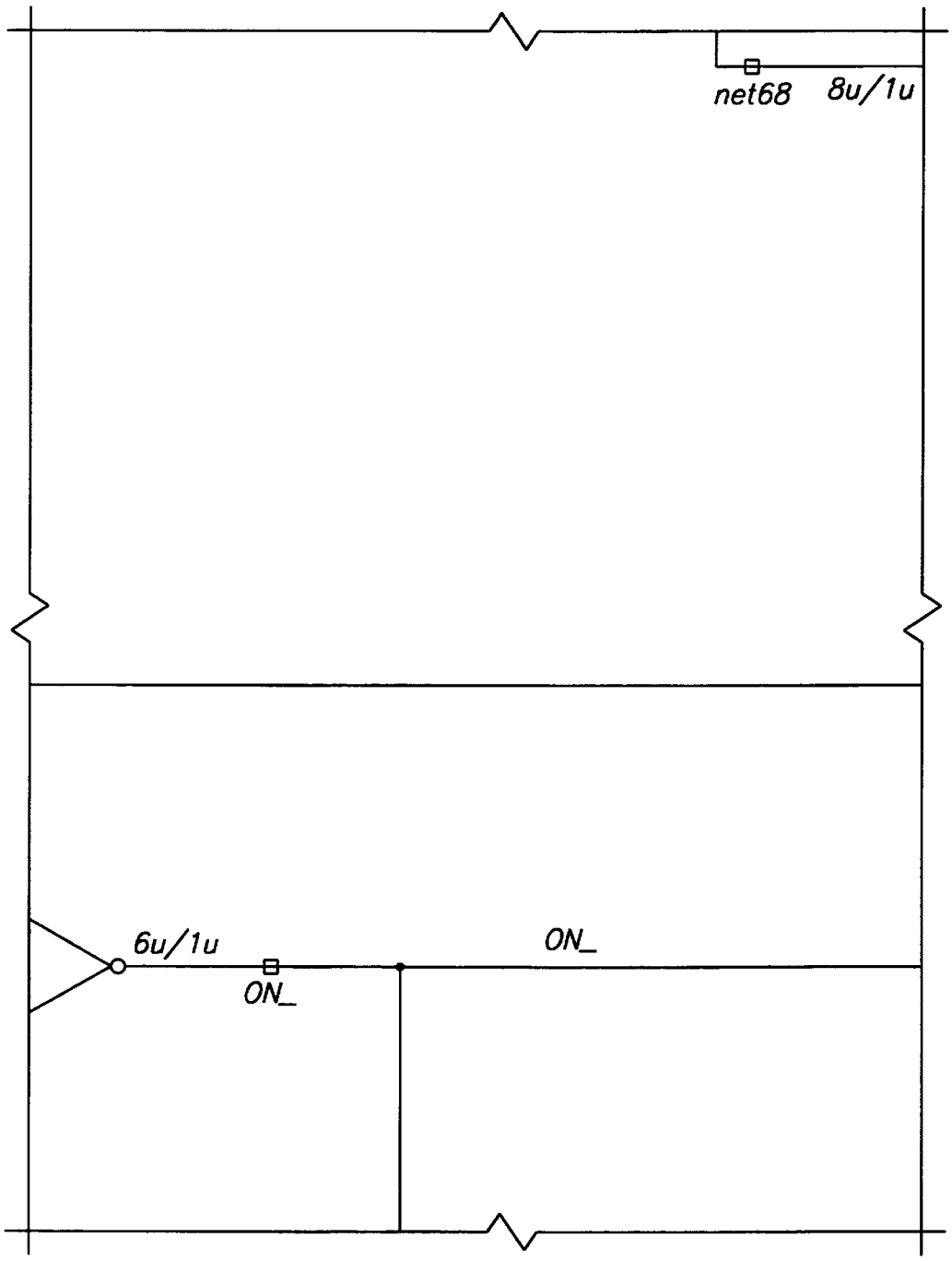


Fig 1.0102CB

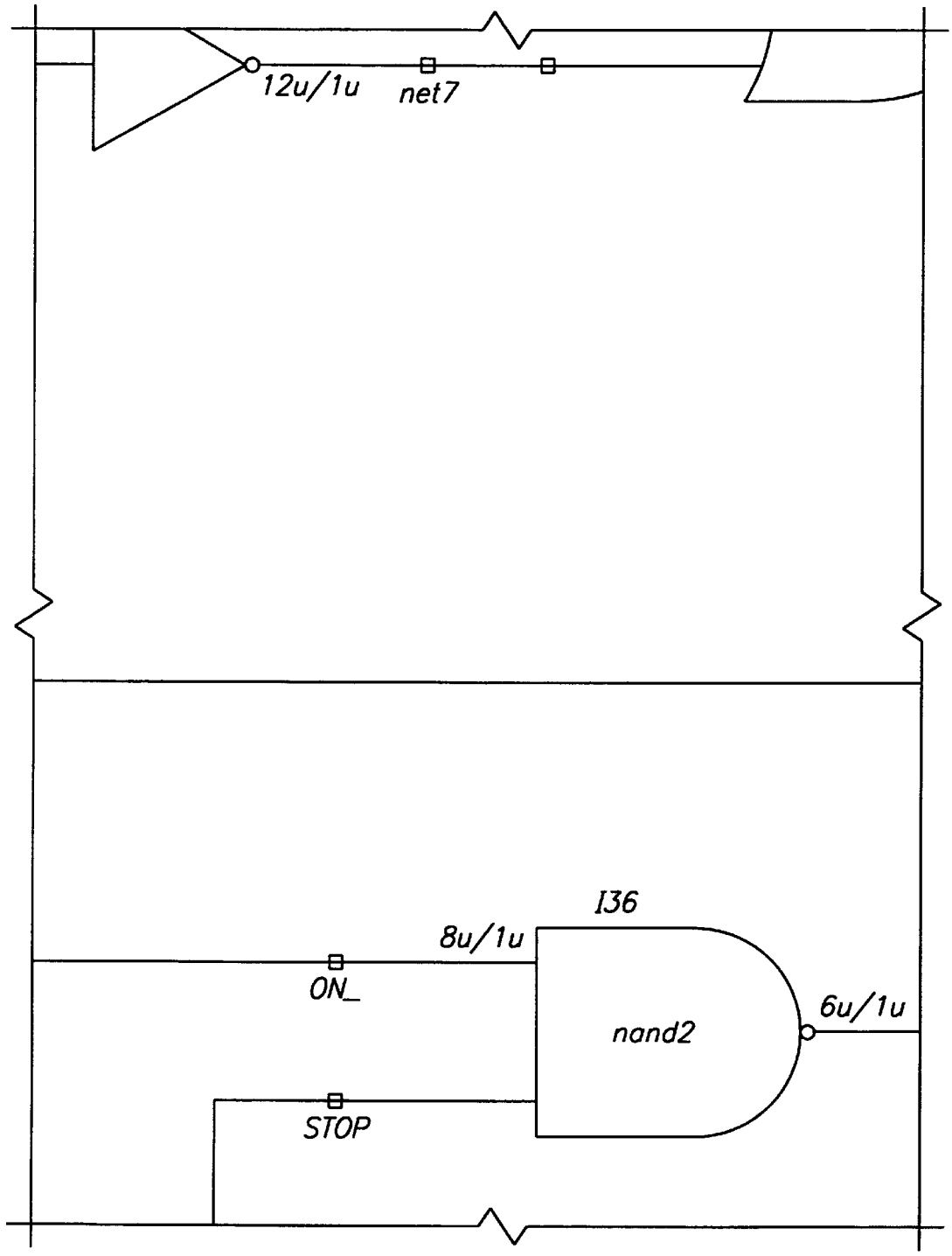


Fig 1.0102CC

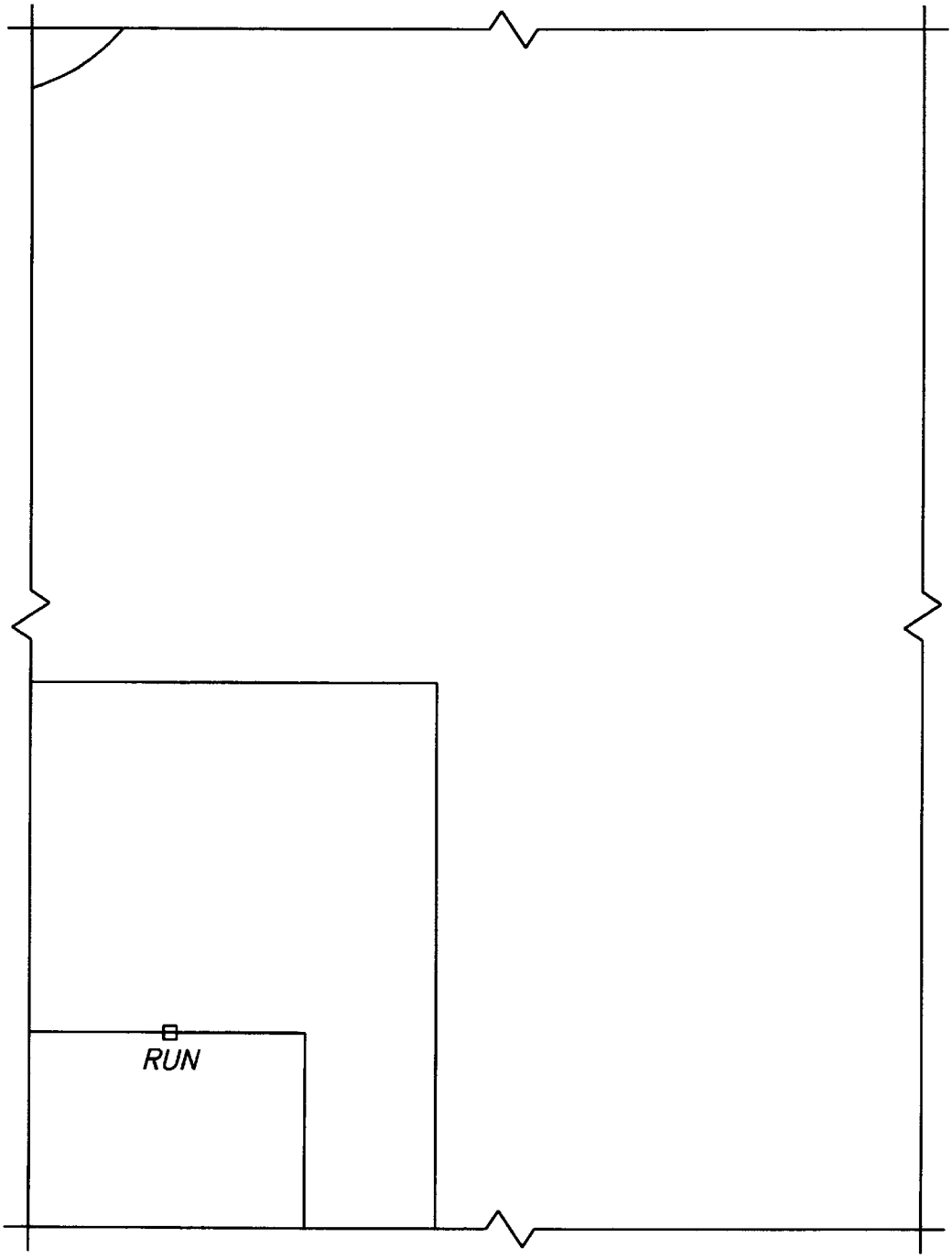


Fig 1.0102CD

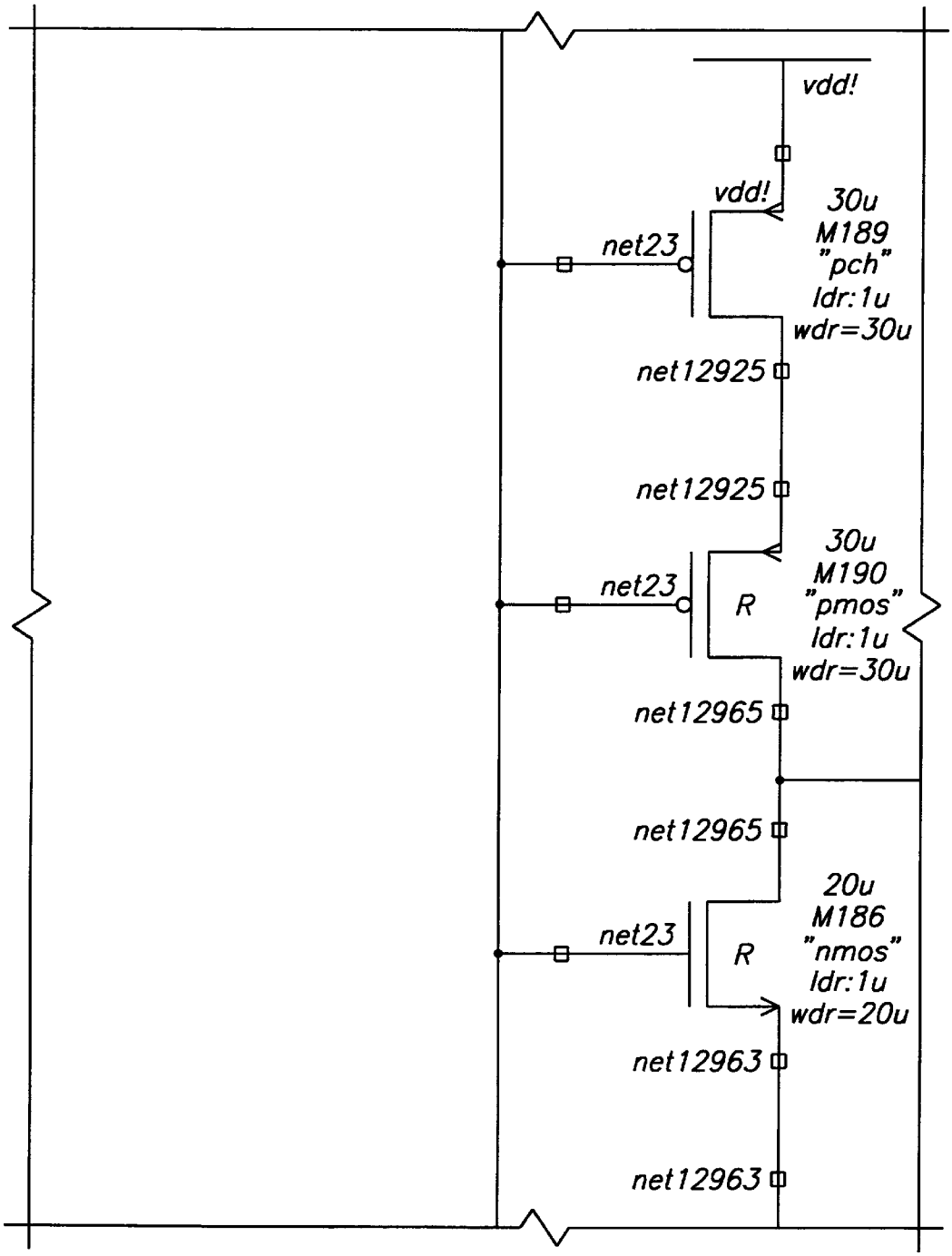

vdd!
vdd!
30u
M189
"pch"
ldr:1u
wdr=30u
net23
net12925
net12925
30u
M190
"pmos"
ldr:1u
wdr=30u
net23
R
net12965
net12965
20u
M186
"nmos"
ldr:1u
wdr=20u
net23
R
net12963
net12963

Fig 1.0102CE

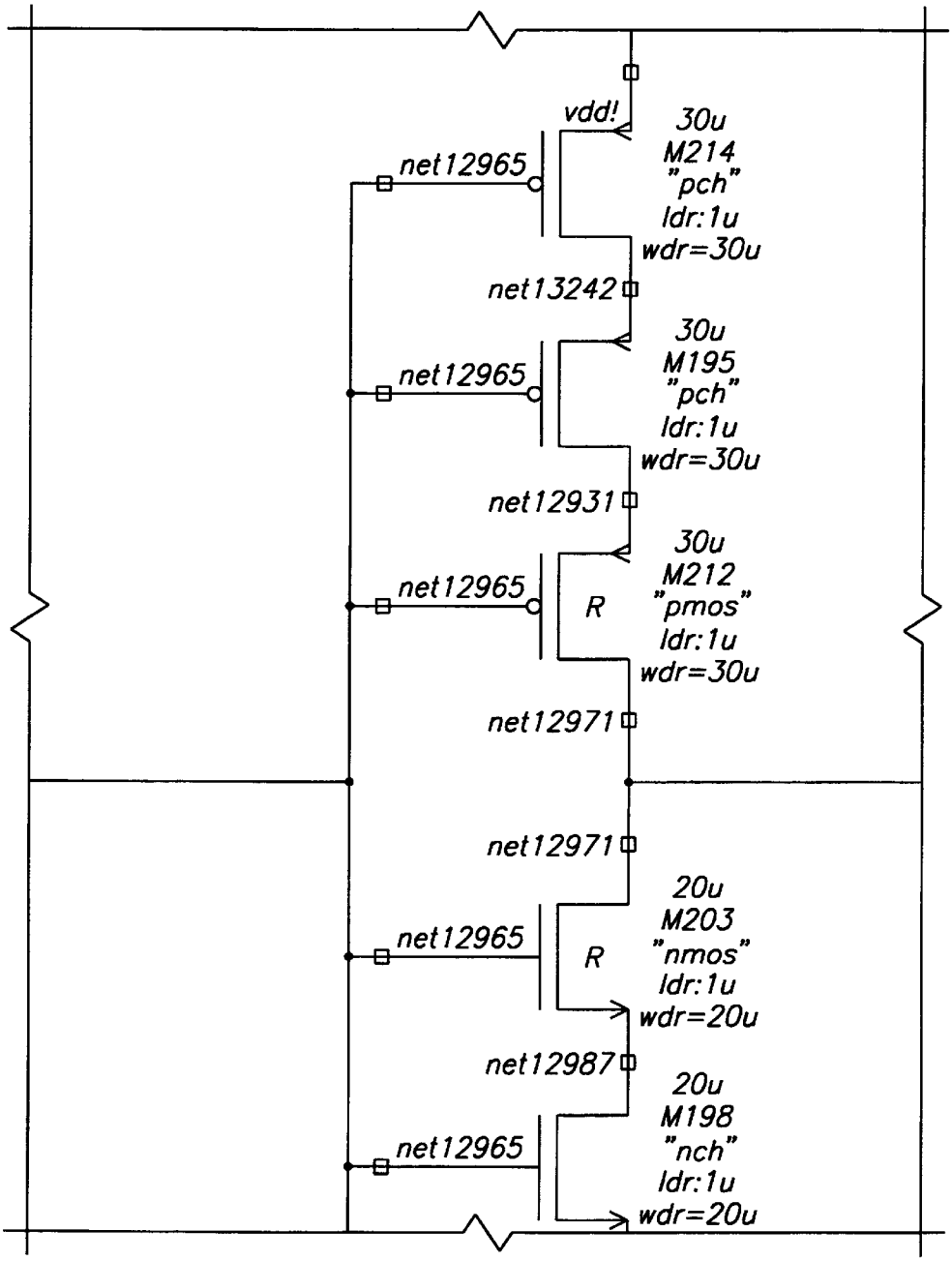

vdd!
30u
M214
"pch"
ldr:1u
wdr=30u
net12965
net13242
30u
M195
"pch"
ldr:1u
wdr=30u
net12965
net12931
30u
M212
"pmos"
ldr:1u
wdr=30u
net12965
R
net12971
net12971
20u
M203
"nmos"
ldr:1u
wdr=20u
net12965
R
net12987
20u
M198
"nch"
ldr:1u
wdr=20u
net12965

Fig 3.0100CF

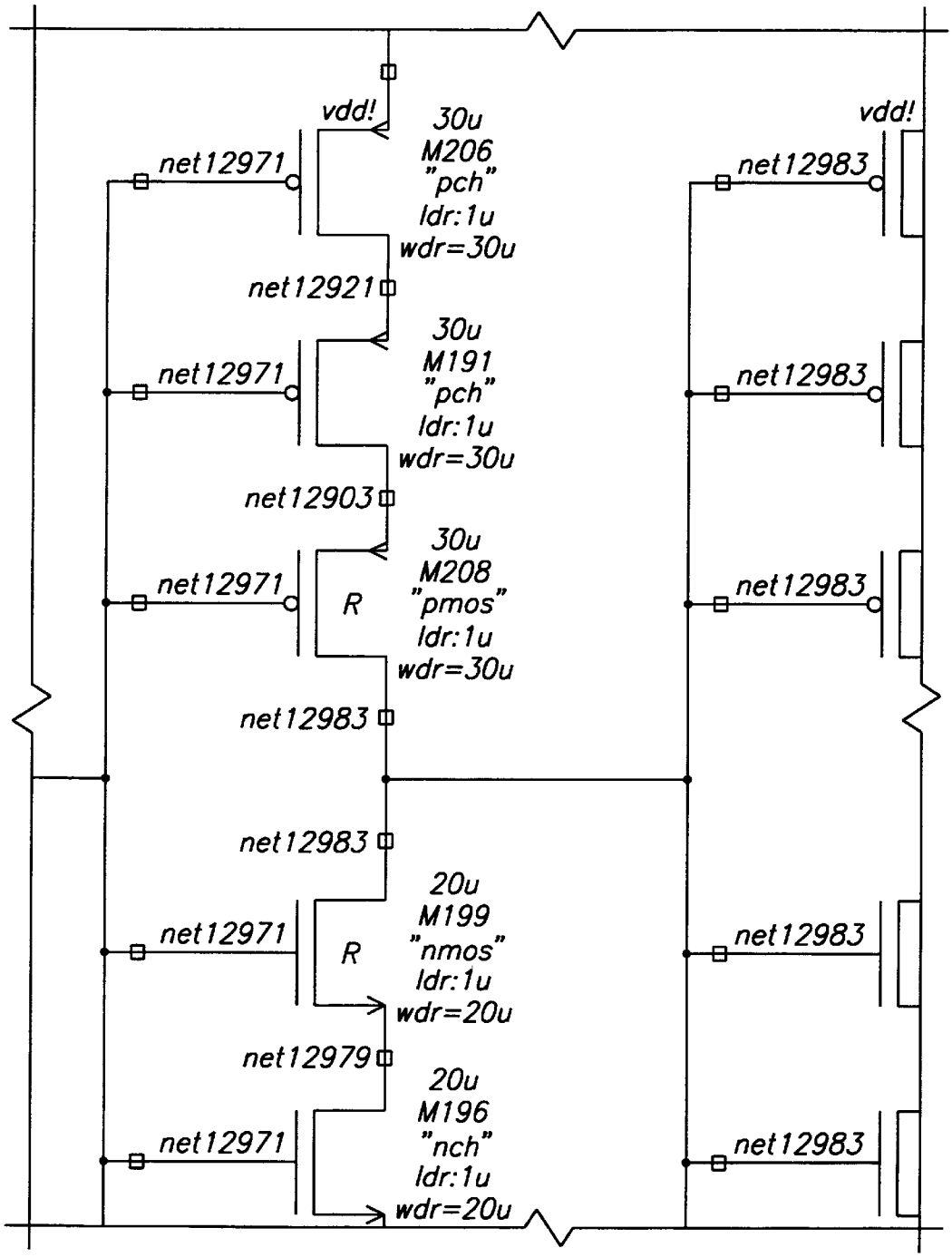

vdd!
30u
M206
"pch"
ldr:1u
wdr=30u
net12971
net12921
30u
M191
"pch"
ldr:1u
wdr=30u
net12903
30u
M208
"pmos"
ldr:1u
wdr=30u
R
net12983
20u
M199
"nmos"
ldr:1u
wdr=20u
net12979
20u
M196
"nch"
ldr:1u
wdr=20u
vdd!
net12983

Fig 1.0102G

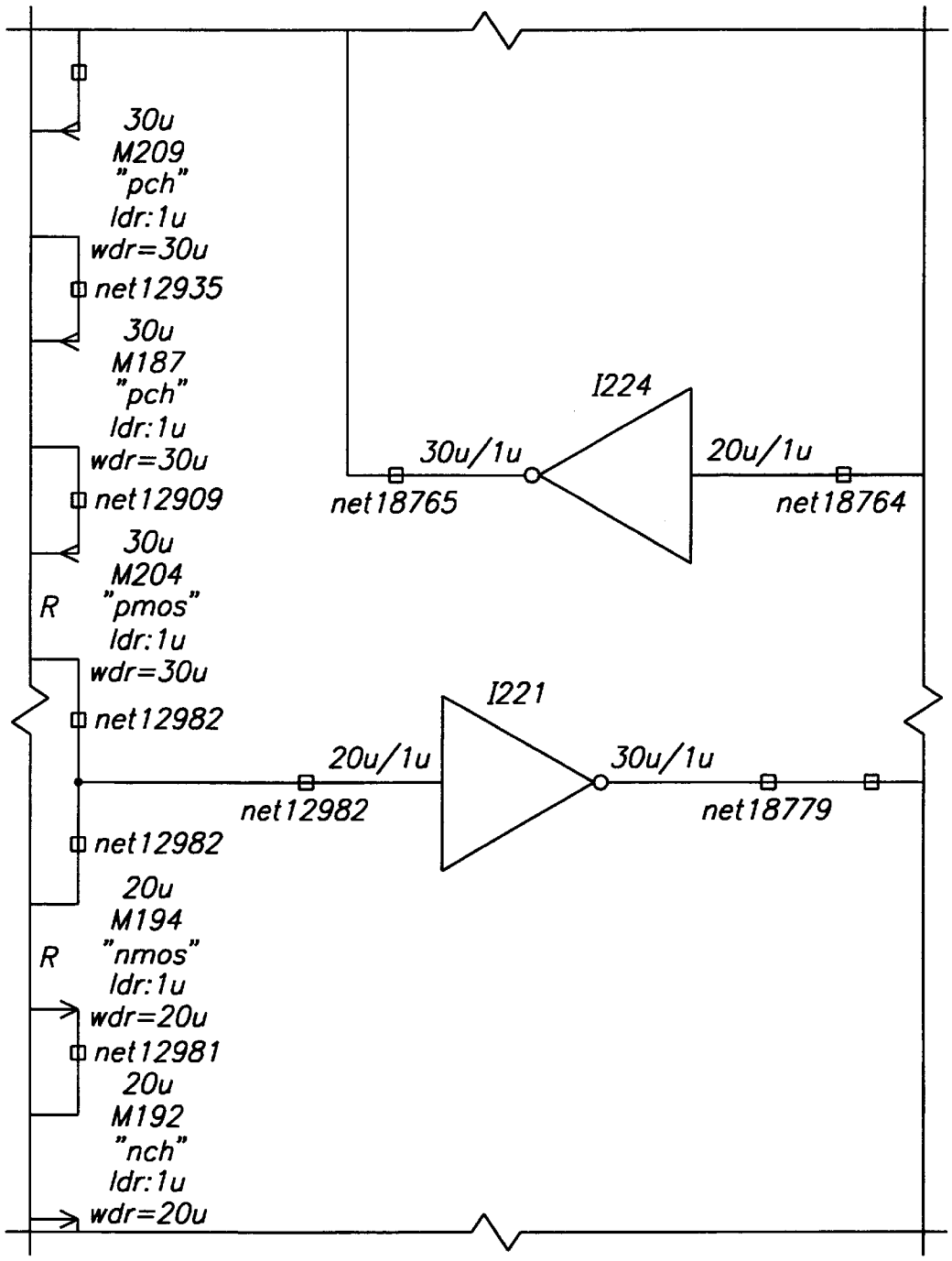

30u
M209
"pch"
ldr:1u
wdr=30u
net12935
30u
M187
"pch"
ldr:1u
wdr=30u
net12909
30u
M204
R
"pmos"
ldr:1u
wdr=30u
net12982
net12982
20u
M194
R
"nmos"
ldr:1u
wdr=20u
net12981
20u
M192
"nch"
ldr:1u
wdr=20u
I224
30u/1u
20u/1u
net18765
net18764
I221
20u/1u
30u/1u
net12982
net18779

FIG 1.0102CH

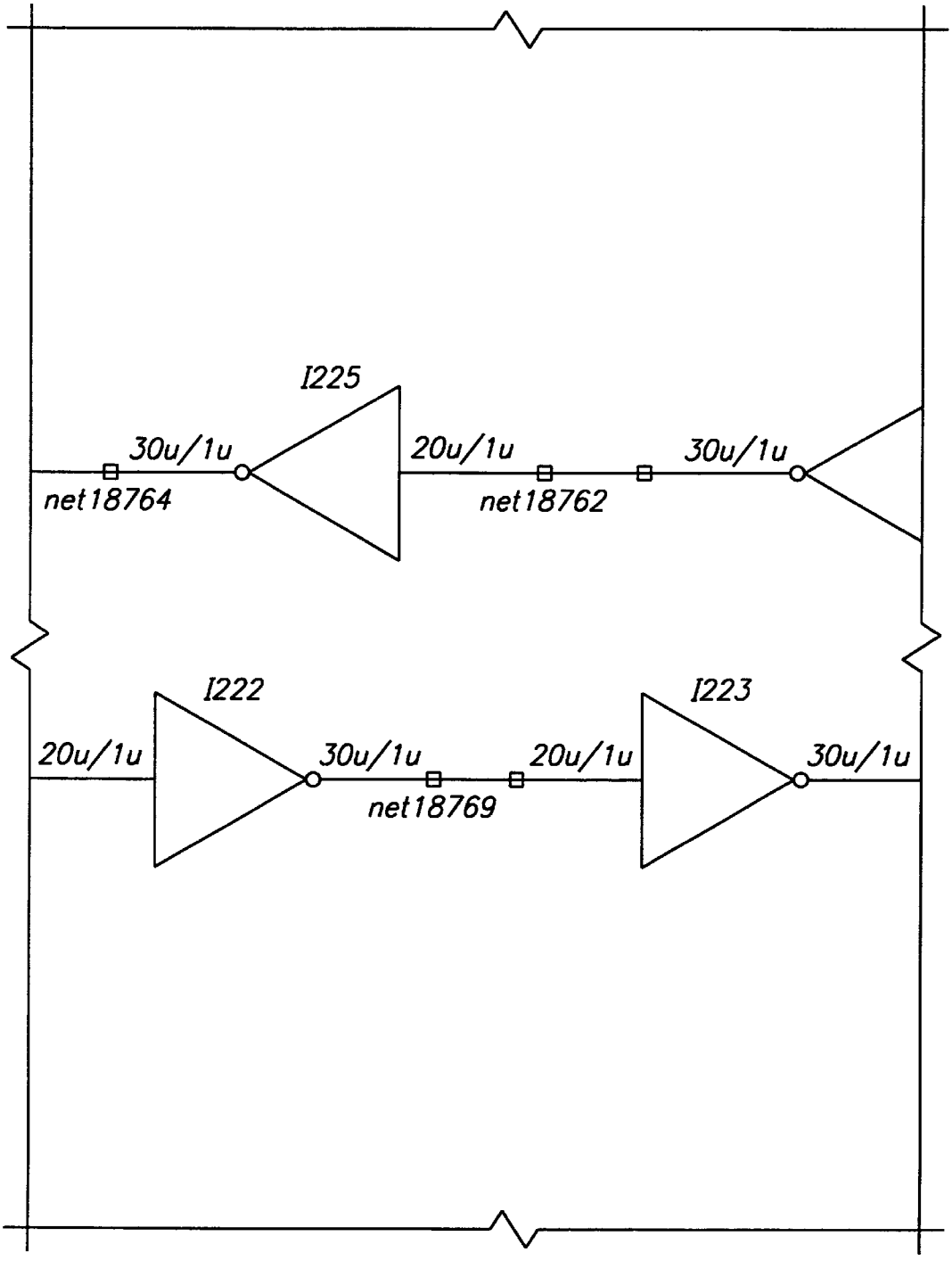

I225
30u/1u
20u/1u
30u/1u
net18764
net18762
I222
I223
20u/1u
30u/1u
20u/1u
30u/1u
net18769

Fig 1.0102CI

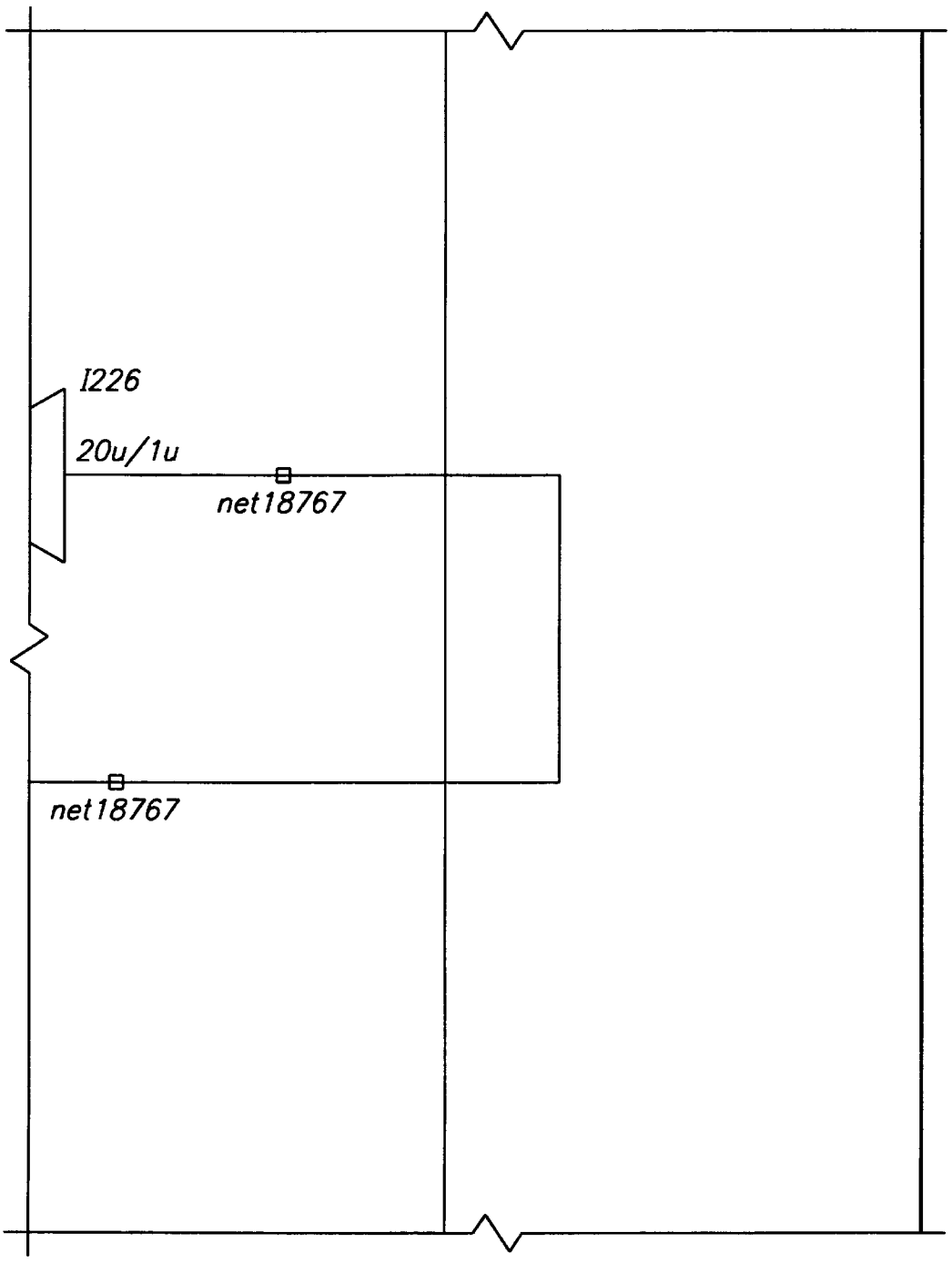


Fig 1.0102Cal

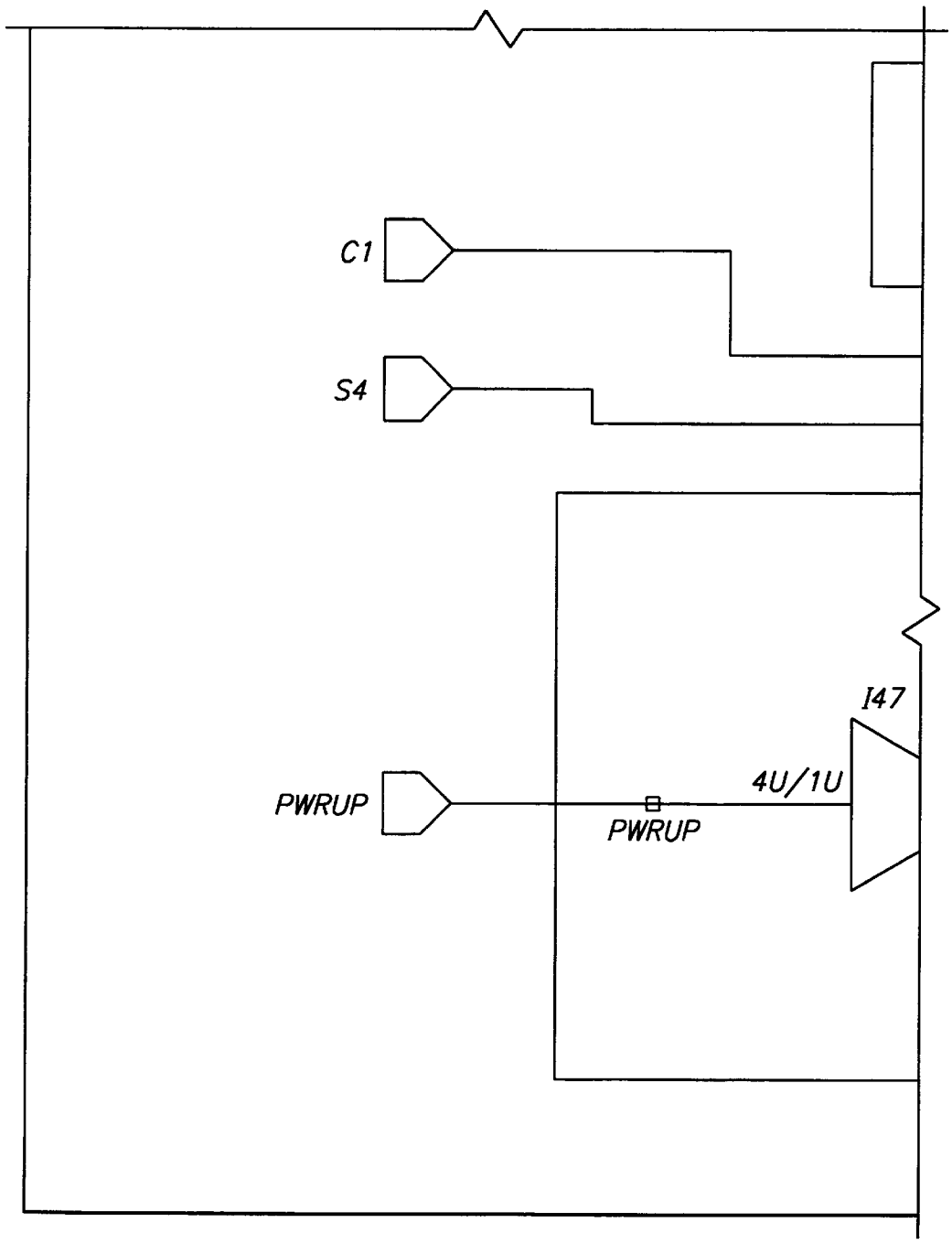


Fig 1.0102DA

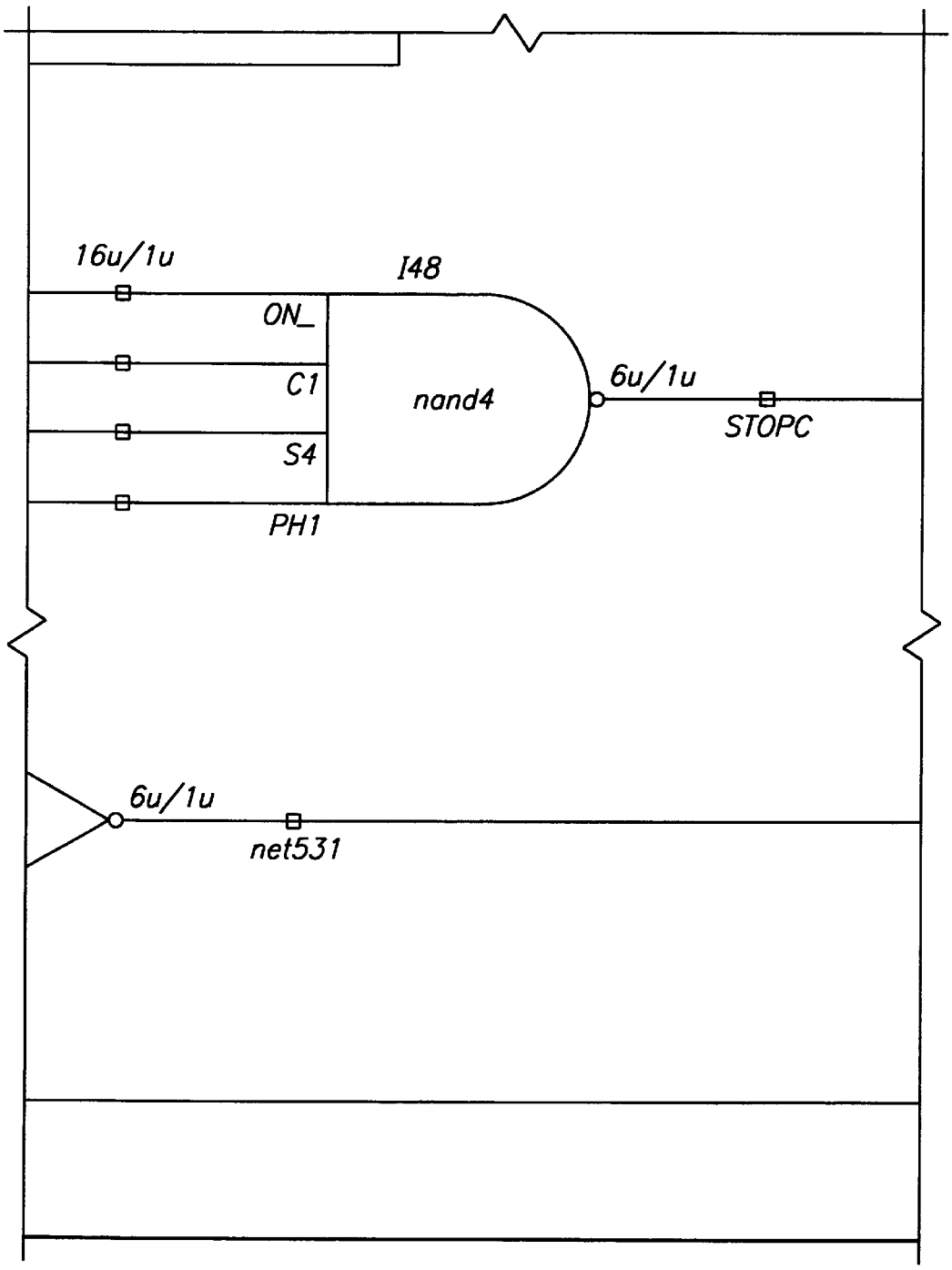


Fig 1.0102DB

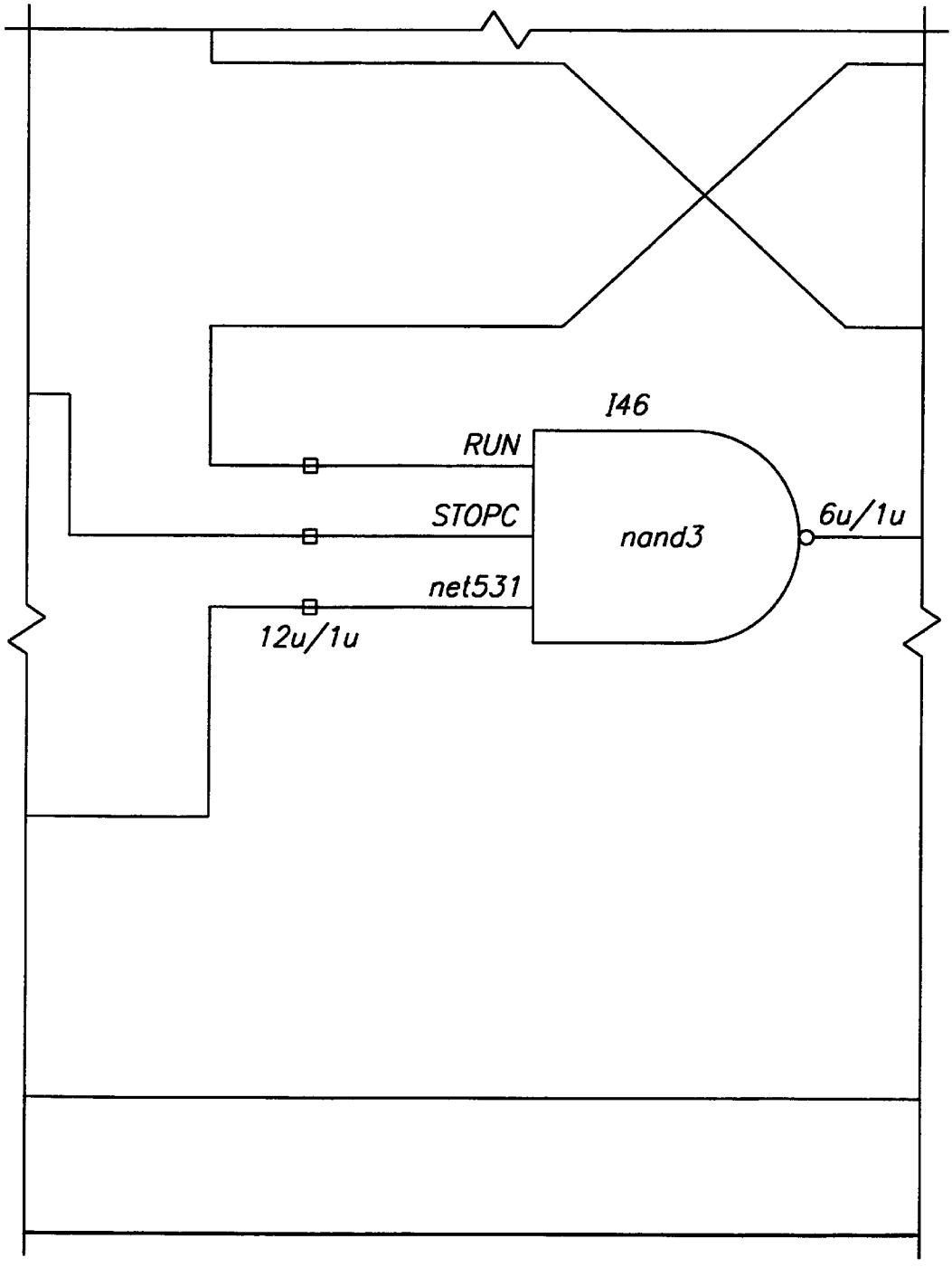


Fig 1.0102DC

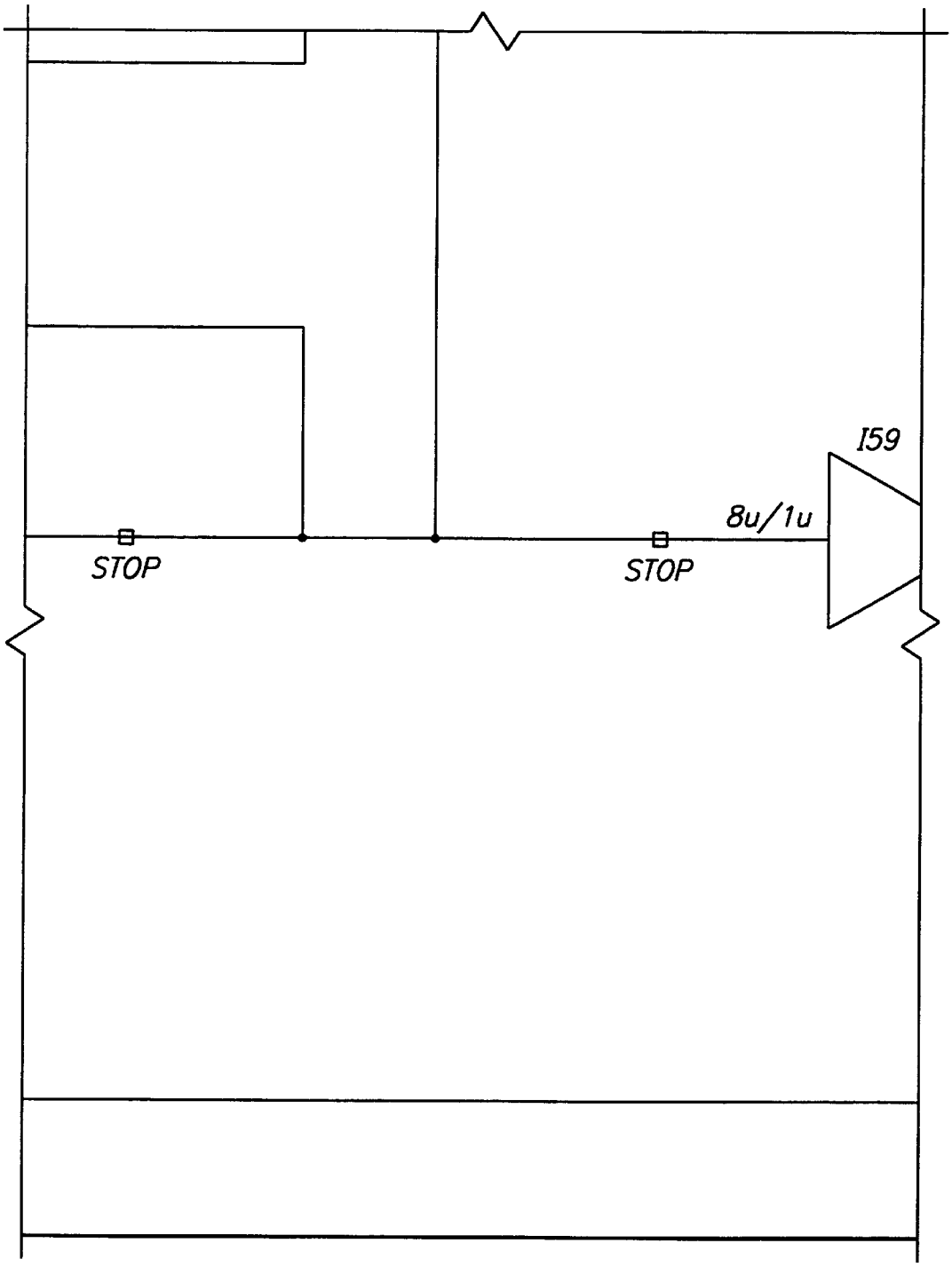


Fig 1.0102000

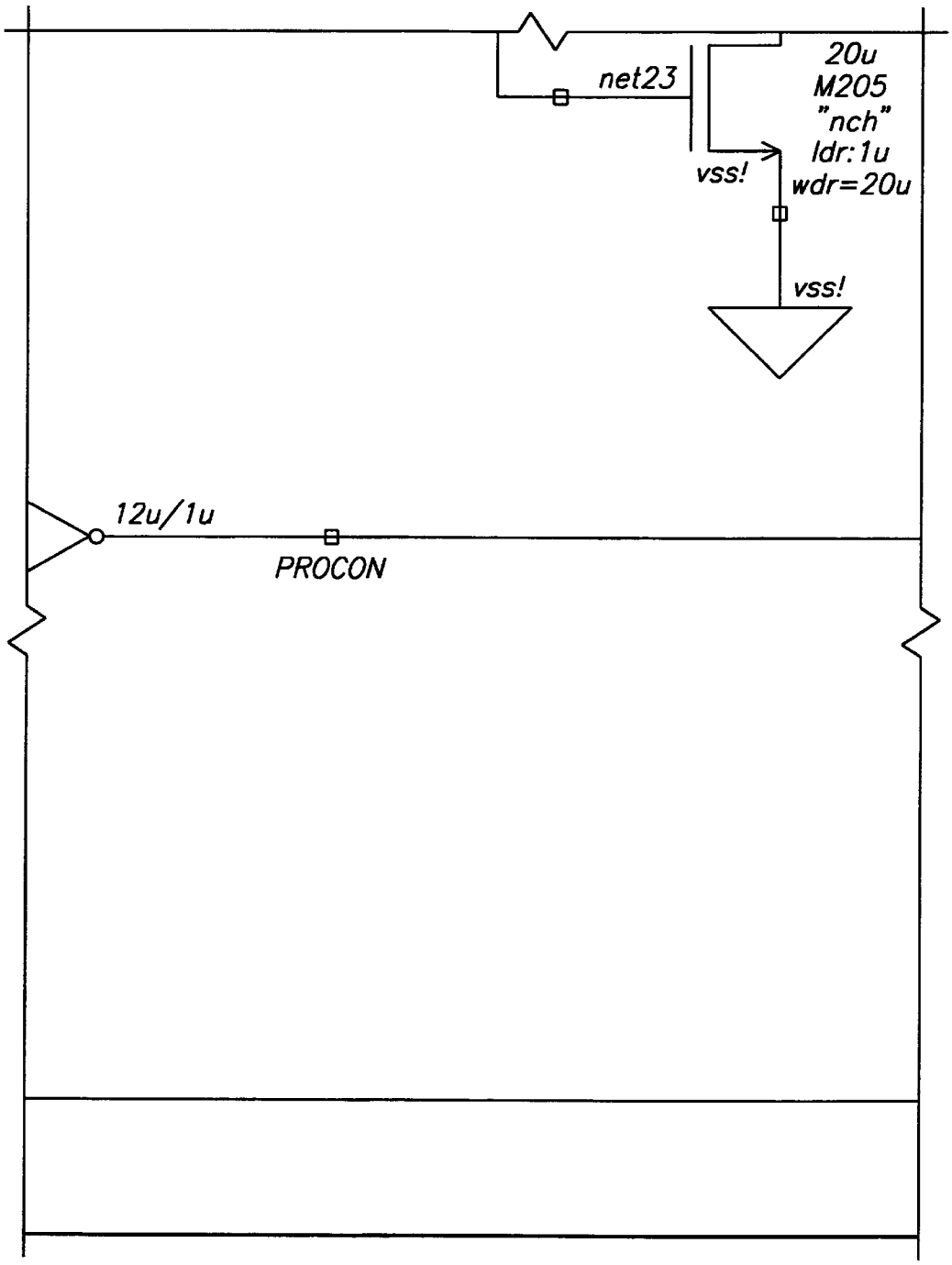


Fig 1.0102DE

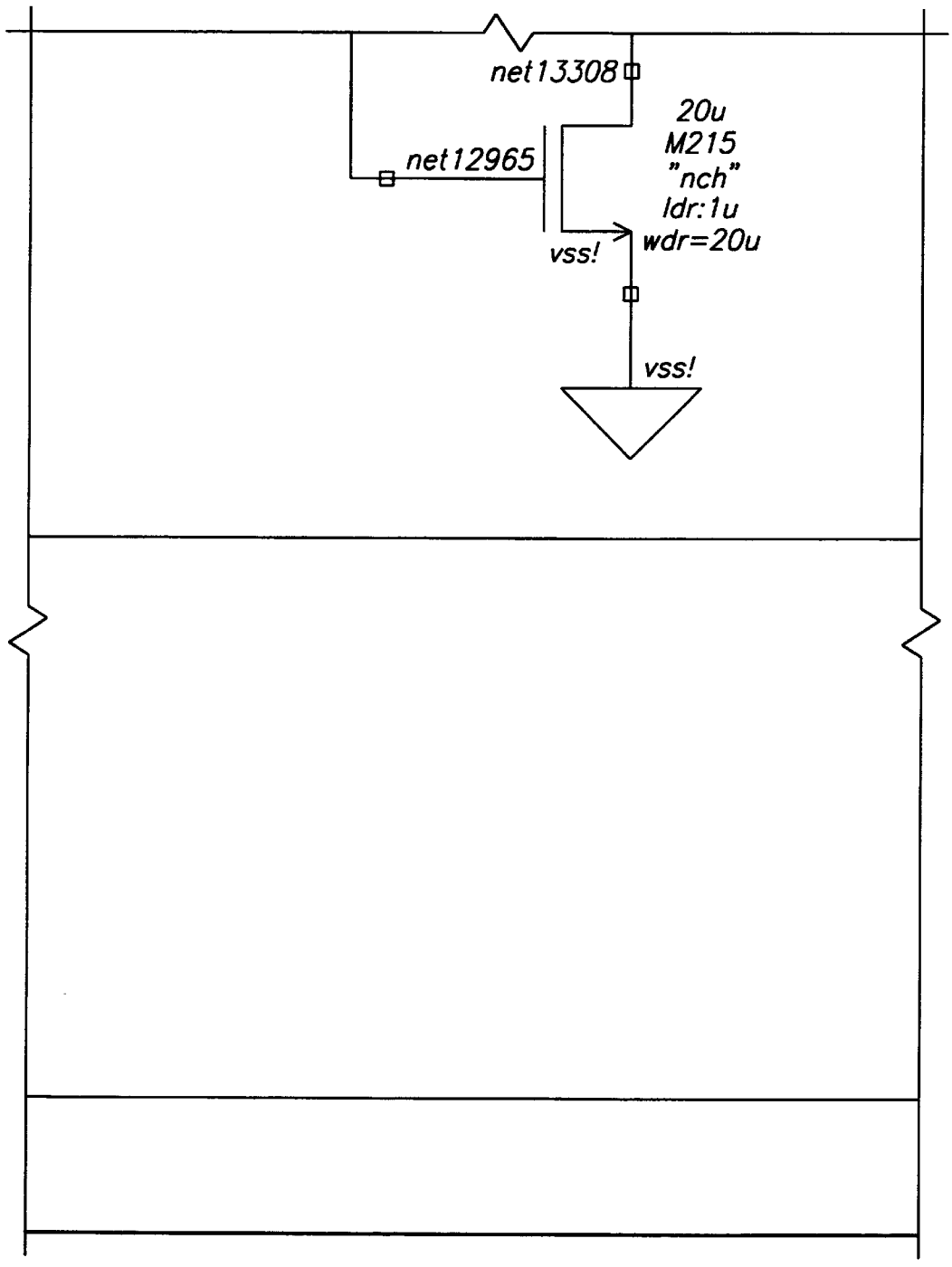


Fig 1.0102DF

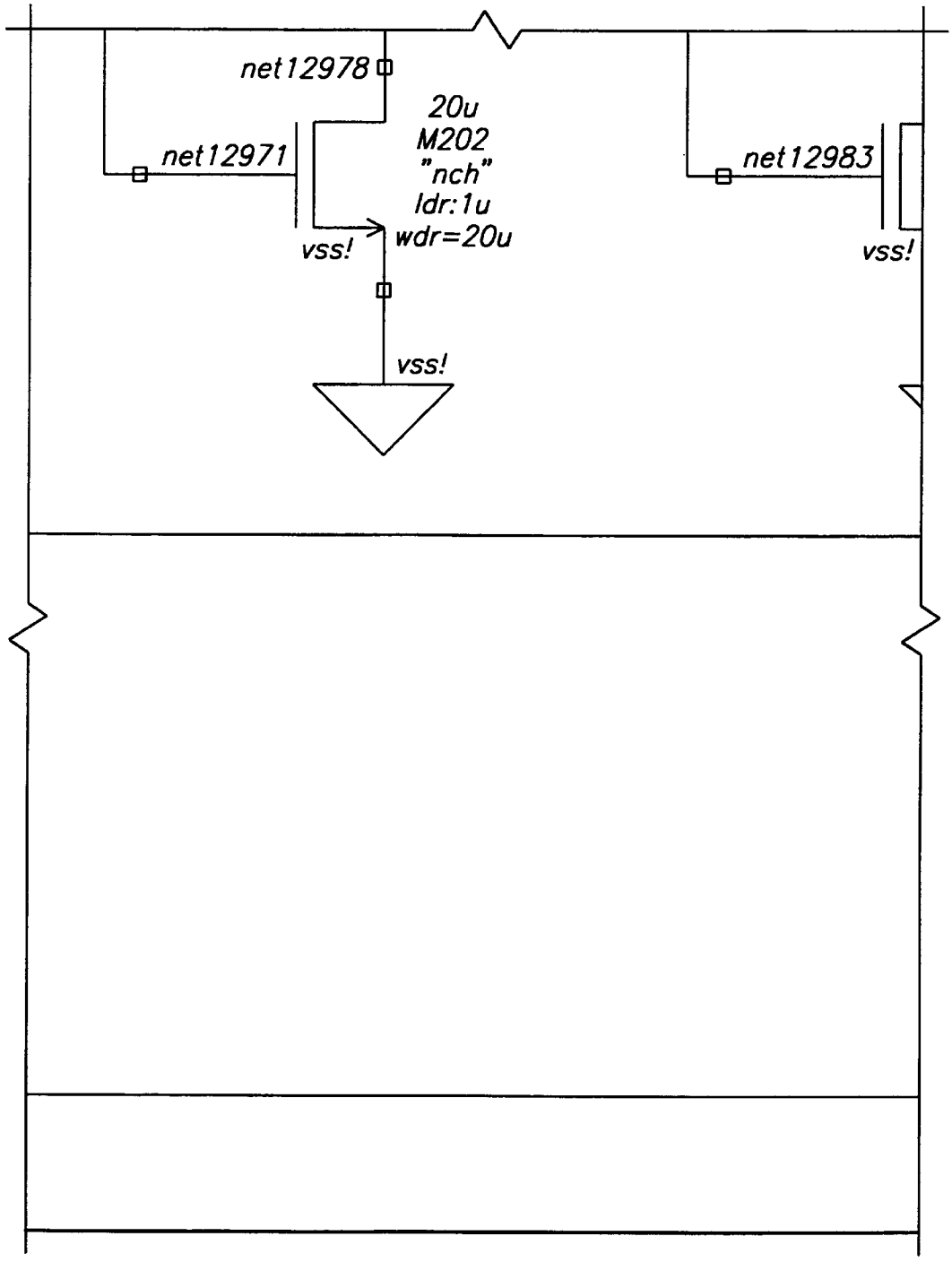


Fig 1.0100206

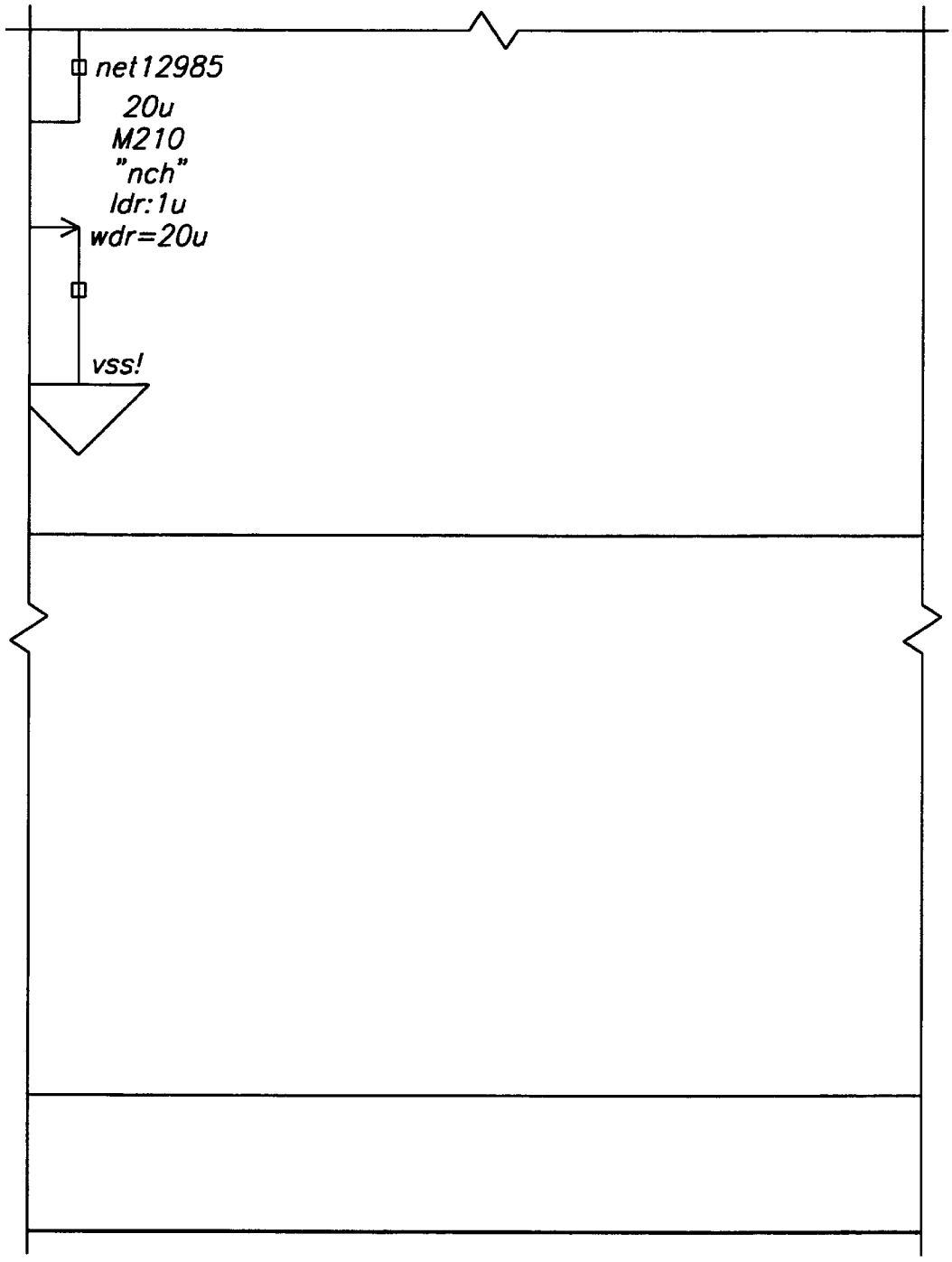


Fig 1.0102DH

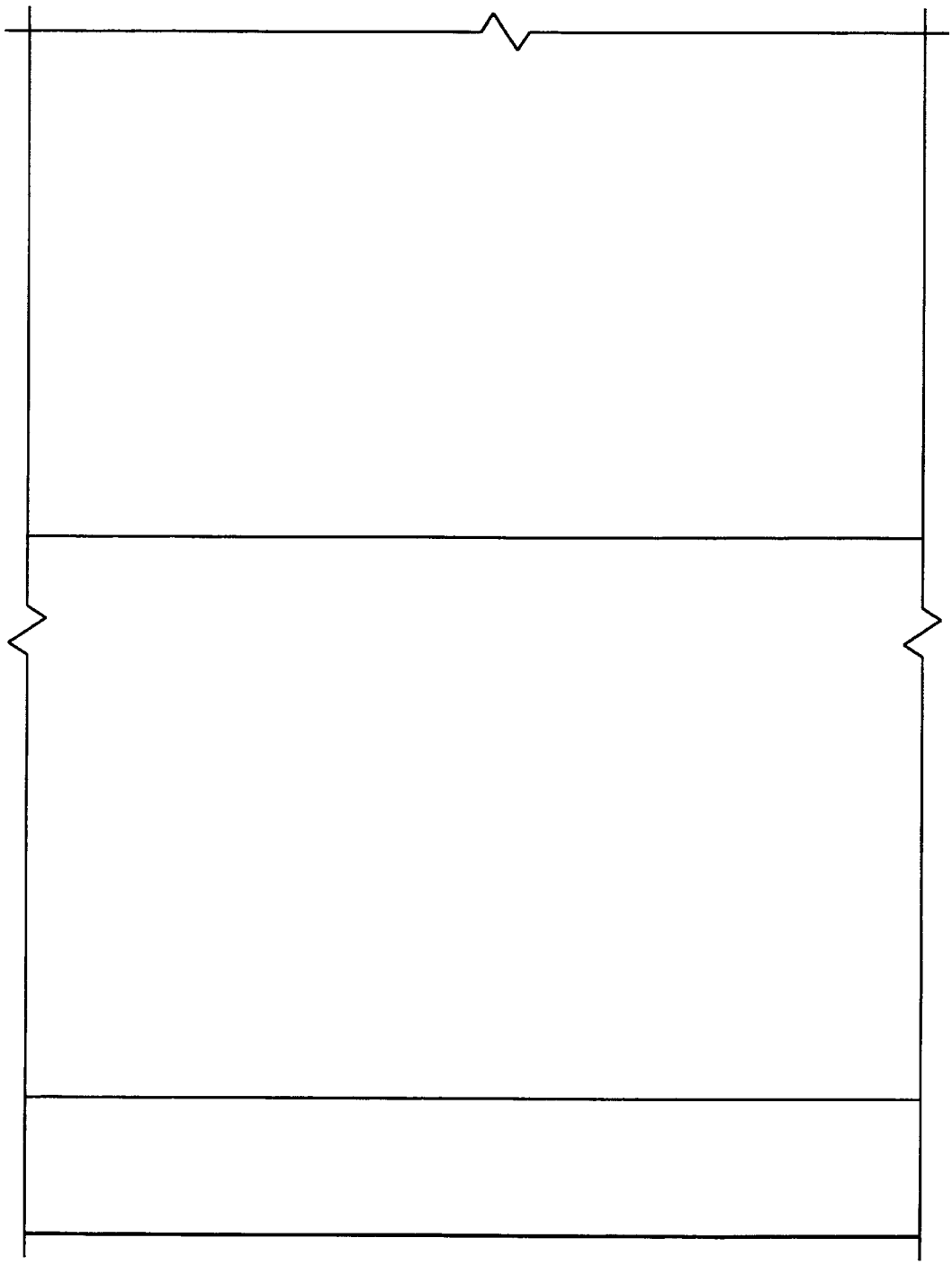


Fig 1.0110201

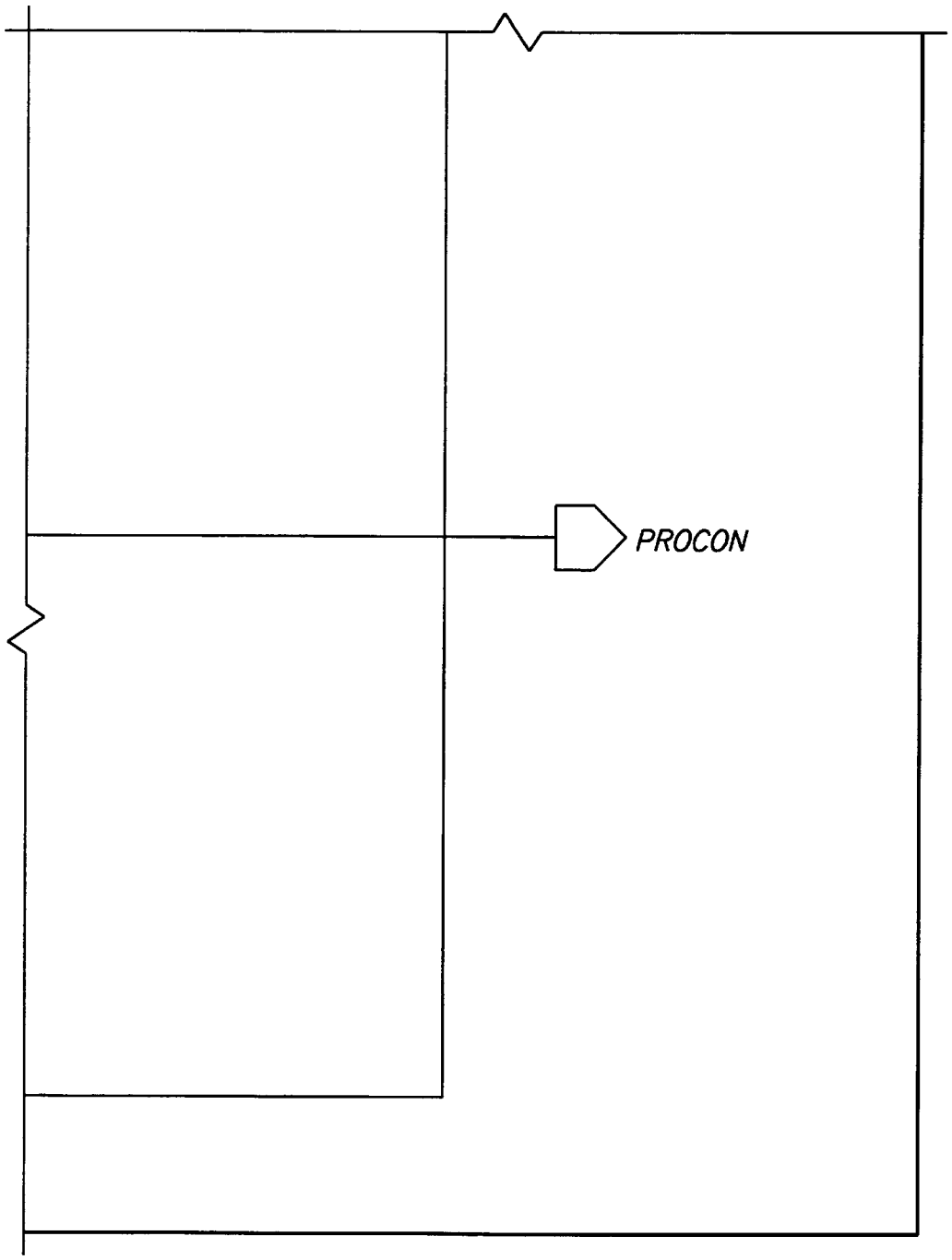


Fig 1.0102D.1

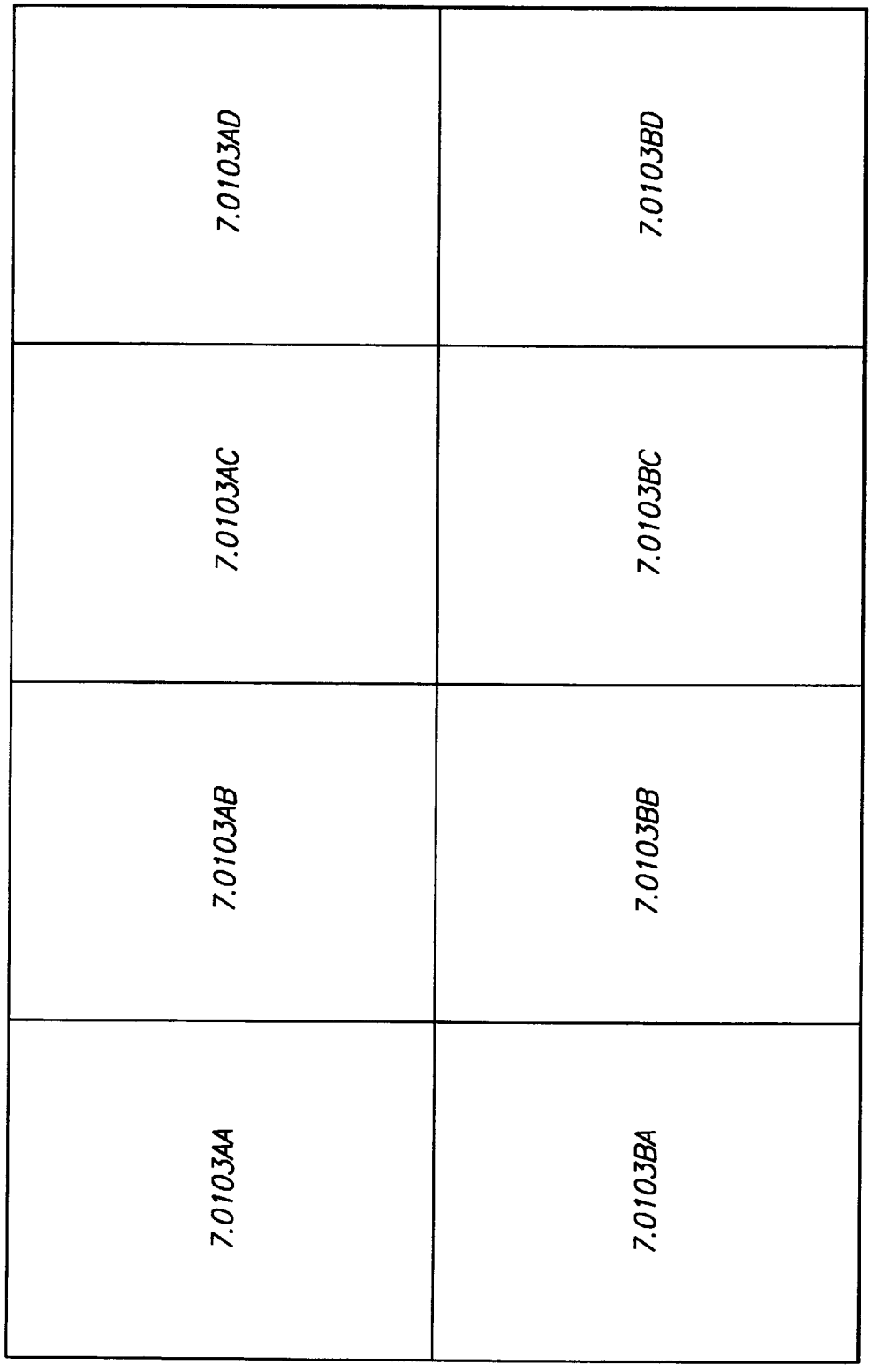

7.0103AD
7.0103BD
7.0103AC
7.0103BC
7.0103AB
7.0103BB
7.0103AA
7.0103BA

FIG. 7.0103

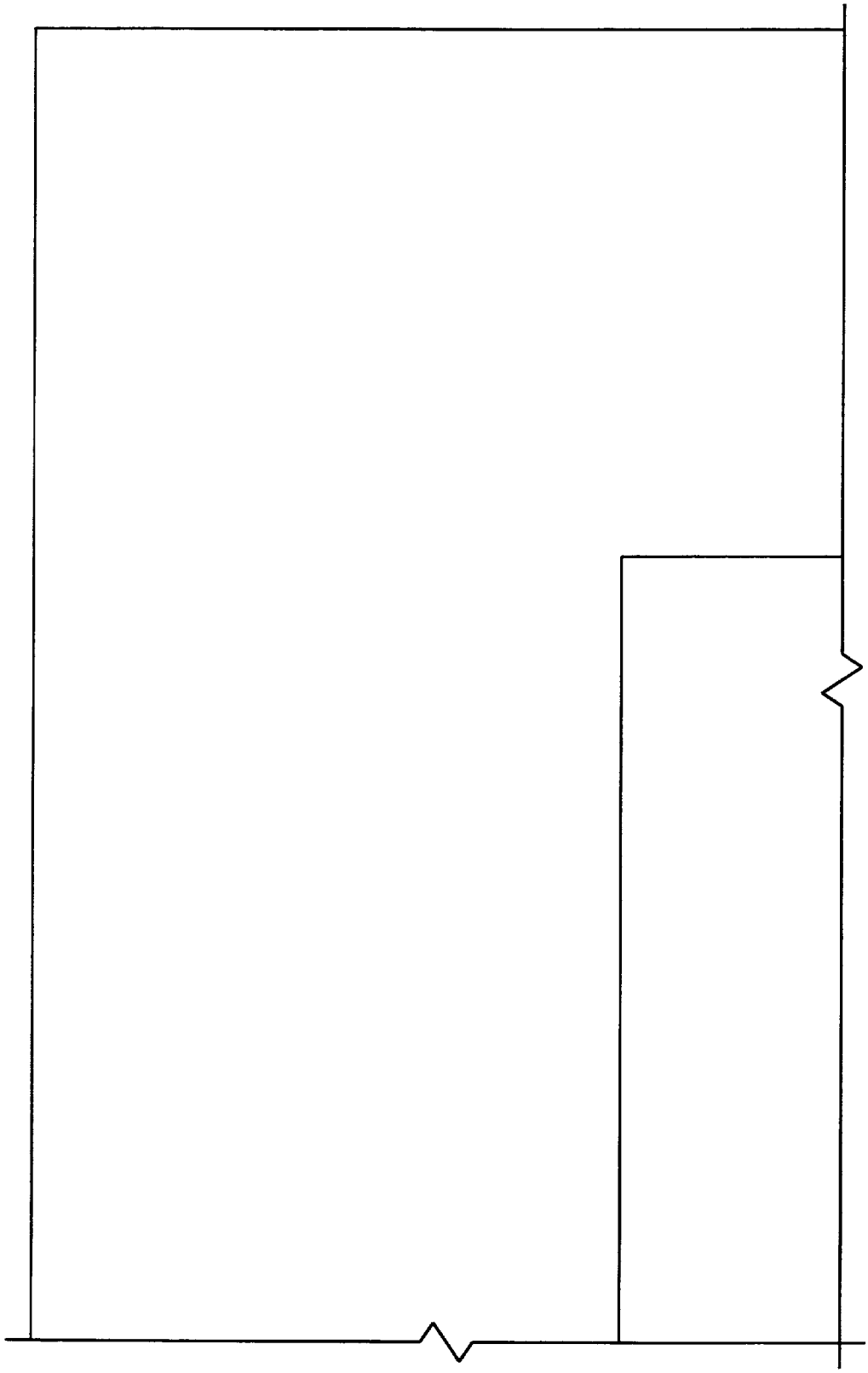


Fig 1.0103AA

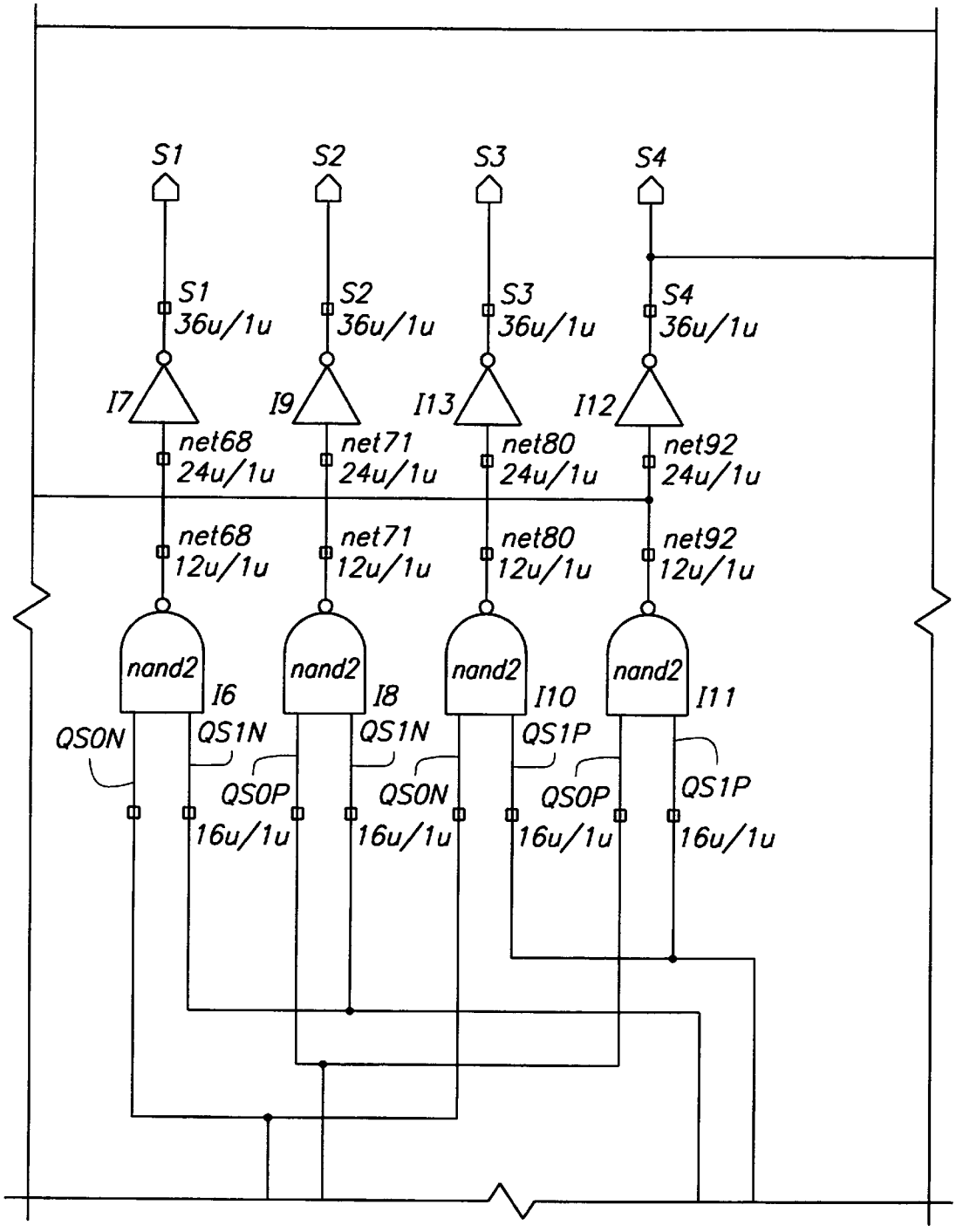

S1
S2
S3
S4
S1
36u/1u
S2
36u/1u
S3
36u/1u
S4
36u/1u
I7
I9
I13
I12
net68
24u/1u
net71
24u/1u
net80
24u/1u
net92
24u/1u
net68
12u/1u
net71
12u/1u
net80
12u/1u
net92
12u/1u
nand2
I6
nand2
I8
nand2
I10
nand2
I11
QS0N
QS1N
QS1N
QS1P
QS0P
16u/1u
QS0N
16u/1u
QS0P
16u/1u
QS1P
16u/1u

FIG 1.0110AB

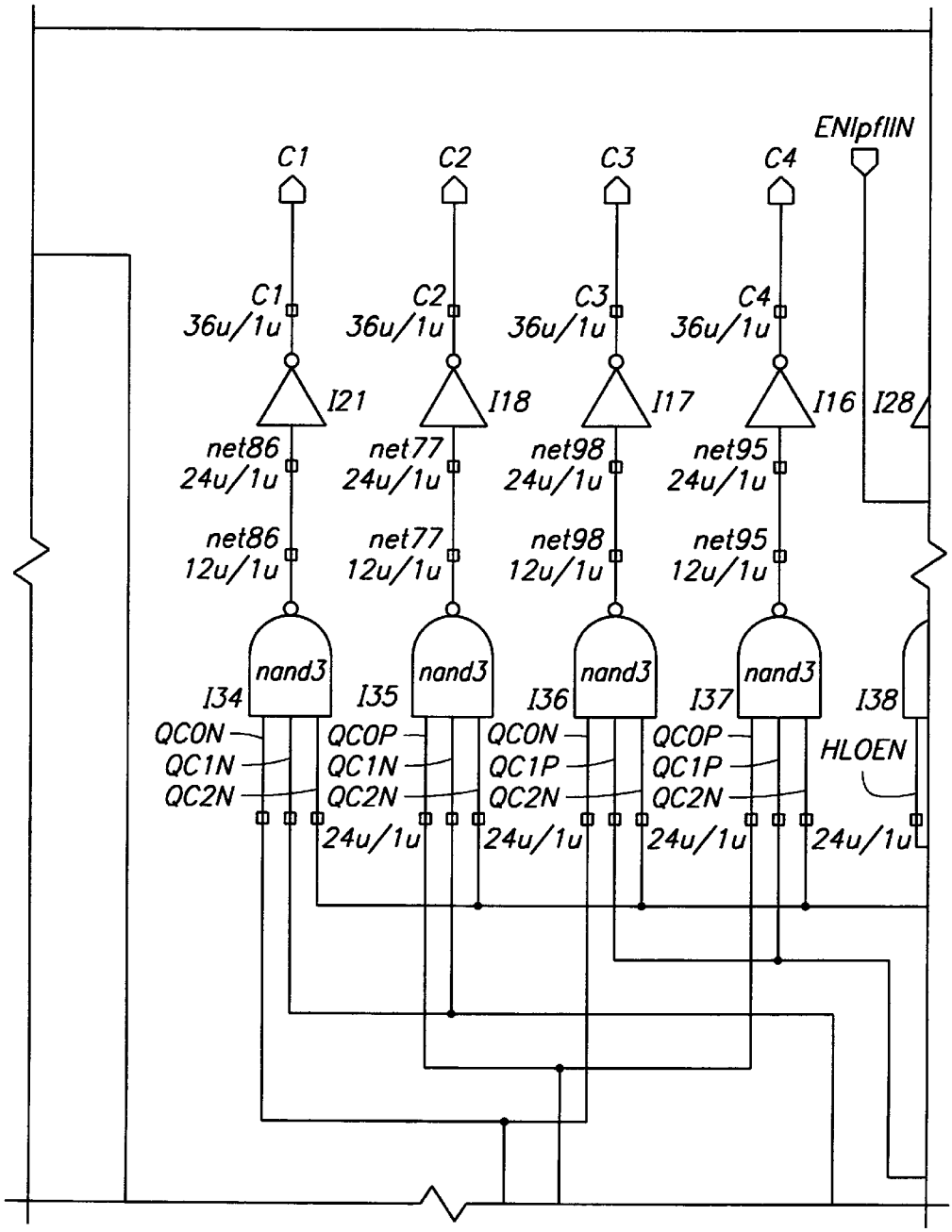

ENIpfIIN
C1
C2
C3
C4
C1
36u/1u
C2
36u/1u
C3
36u/1u
C4
36u/1u
I21
I18
I17
I16
I28
net86
24u/1u
net77
24u/1u
net98
24u/1u
net95
24u/1u
net86
12u/1u
net77
12u/1u
net98
12u/1u
net95
12u/1u
nand3
nand3
nand3
nand3
I34
I35
I36
I37
I38
QC0N
QC1N
QC2N
QC0P
QC1N
QC2N
QC0N
QC1P
QC2N
QC0P
QC1P
QC2N
HLOEN
24u/1u
24u/1u
24u/1u
24u/1u

Fig 1.0103AC

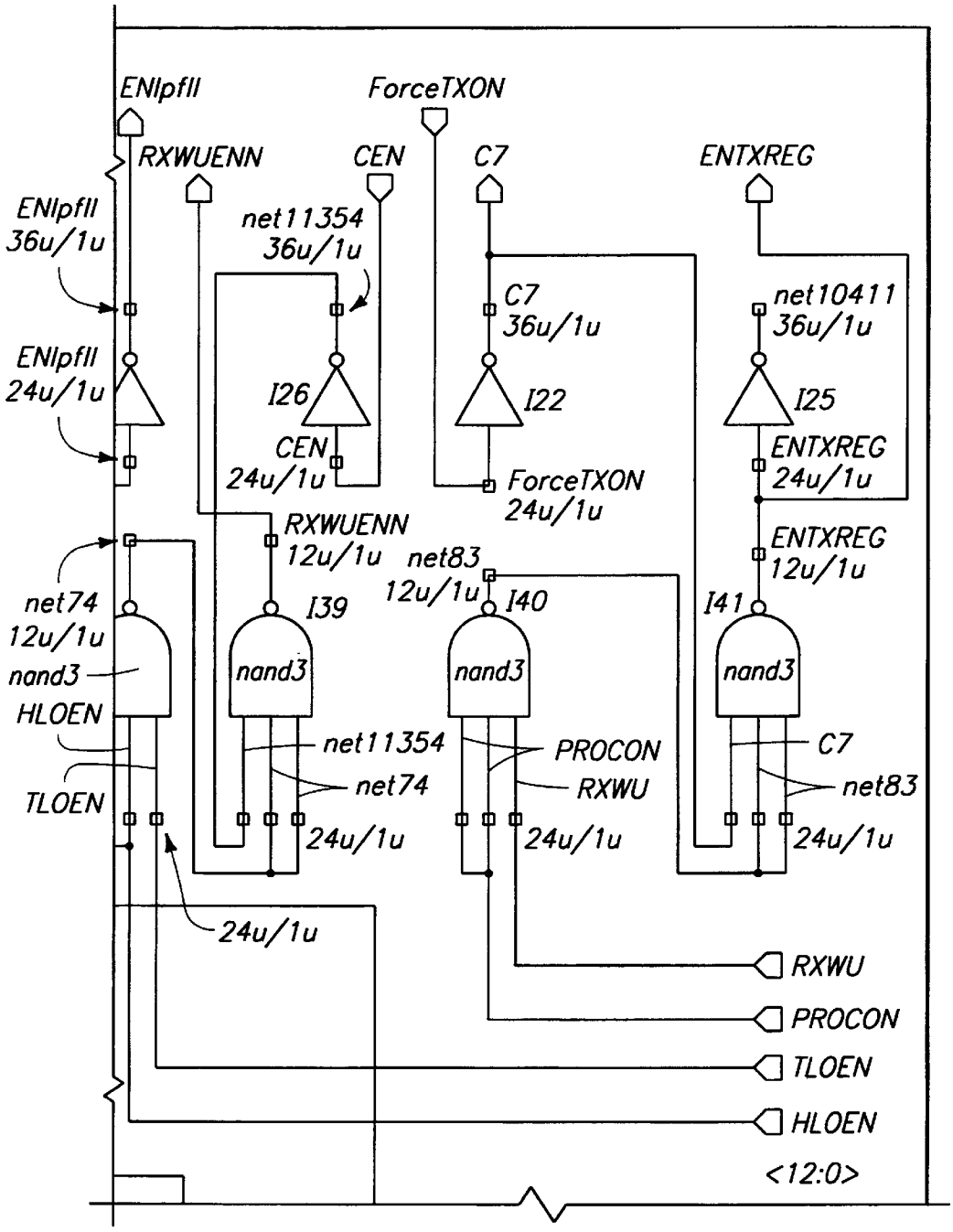

ENIpfII
ForceTXON
RXWUENN
CEN
C7
ENTXREG
ENIpfII
36u/1u
net11354
36u/1u
C7
36u/1u
net10411
36u/1u
ENIpfII
24u/1u
I26
I22
I25
CEN
24u/1u
ForceTXON
24u/1u
ENTXREG
24u/1u
RXWUENN
12u/1u
net83
12u/1u
ENTXREG
12u/1u
net74
12u/1u
I39
I40
I41
nand3
nand3
nand3
nand3
HLOEN
TLOEN
net11354
net74
PROCON
RXWU
C7
net83
24u/1u
24u/1u
24u/1u
24u/1u
RXWU
PROCON
TLOEN
HLOEN
<12:0>

Fig 1.0103AD

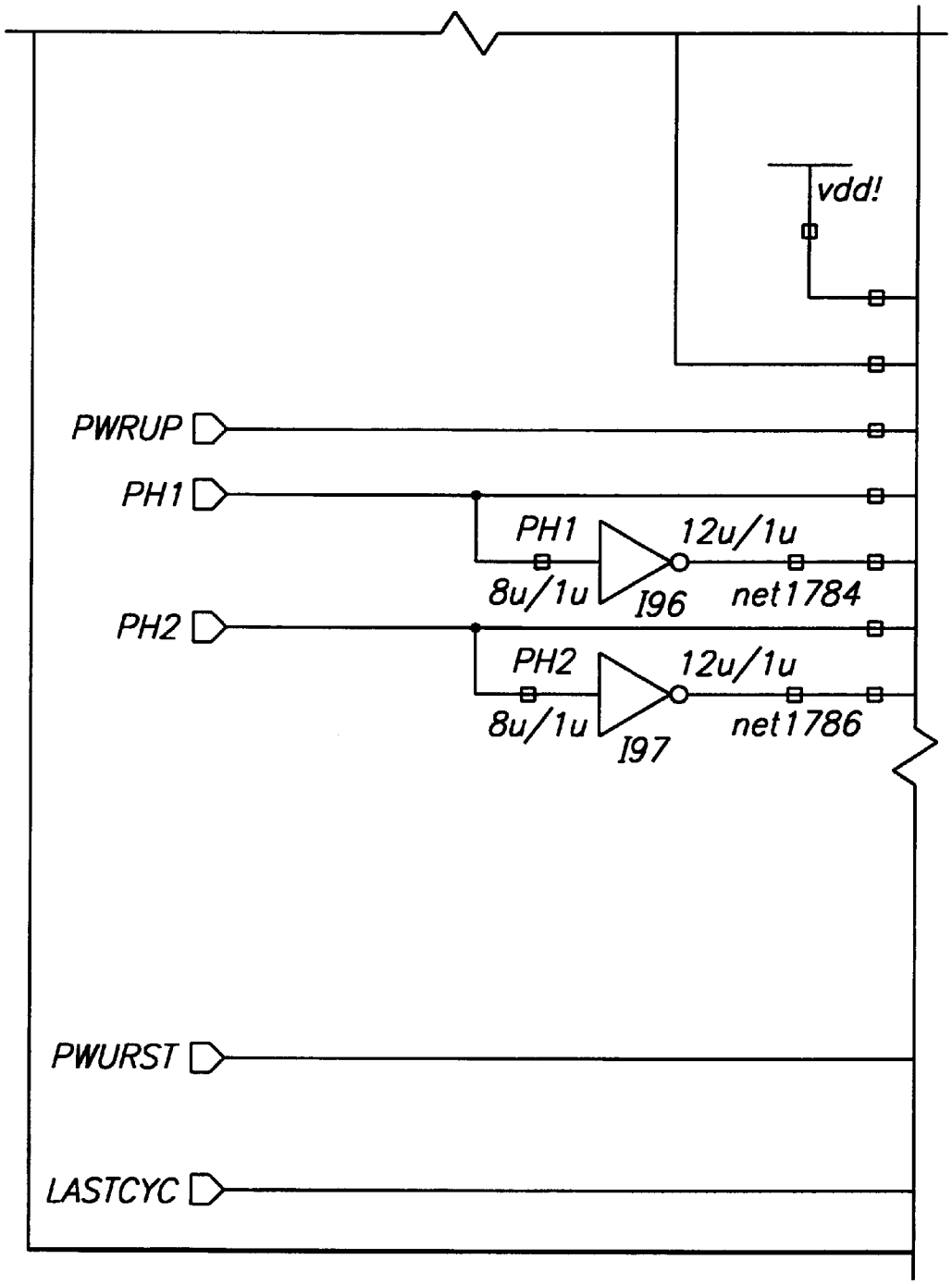

vdd!
PWRUP
PH1
PH1
12u/1u
8u/1u
I96
net1784
PH2
PH2
12u/1u
8u/1u
net1786
I97
PWURST
LASTCYC

Fig 1.0103BA

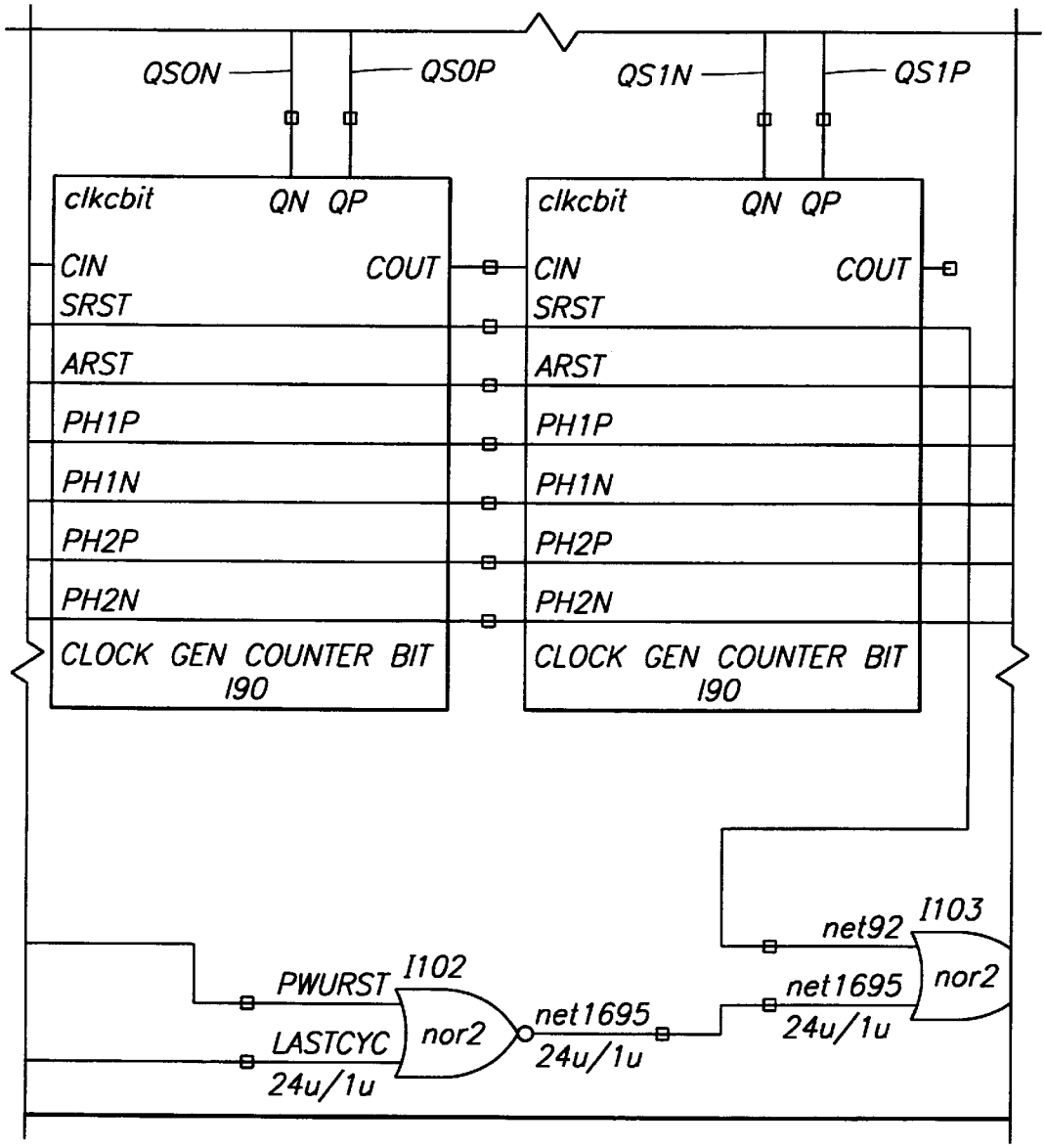


Fig 1,011,038B

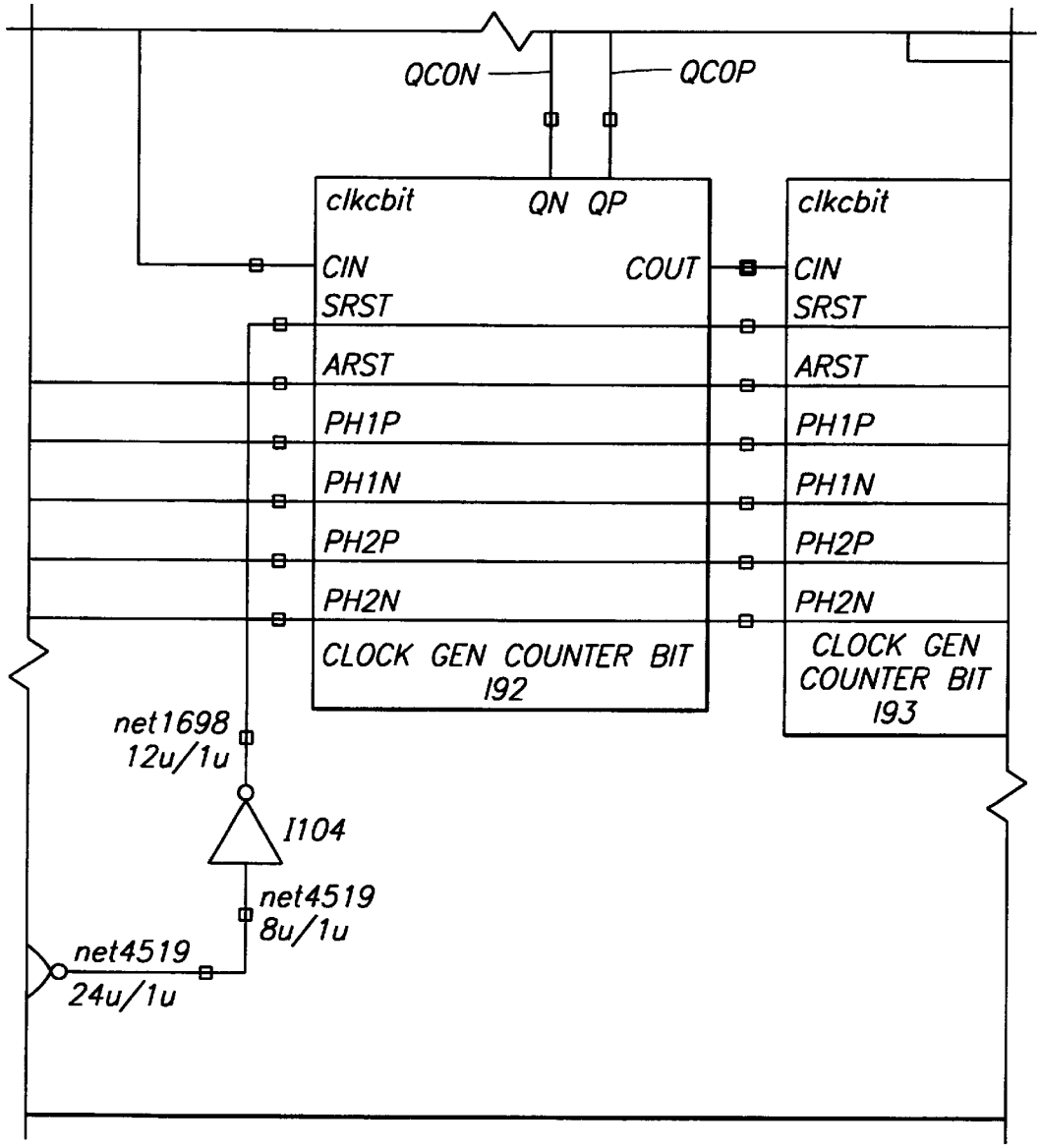

QCON
QCOP
clkcbit
QN QP
CIN
COUT
SRST
ARST
PH1P
PH1N
PH2P
PH2N
CLOCK GEN COUNTER BIT
I92
clkcbit
CIN
SRST
ARST
PH1P
PH1N
PH2P
PH2N
CLOCK GEN COUNTER BIT
I93
net1698
12u/1u
I104
net4519
8u/1u
net4519
24u/1u

Fig 7.0010BC

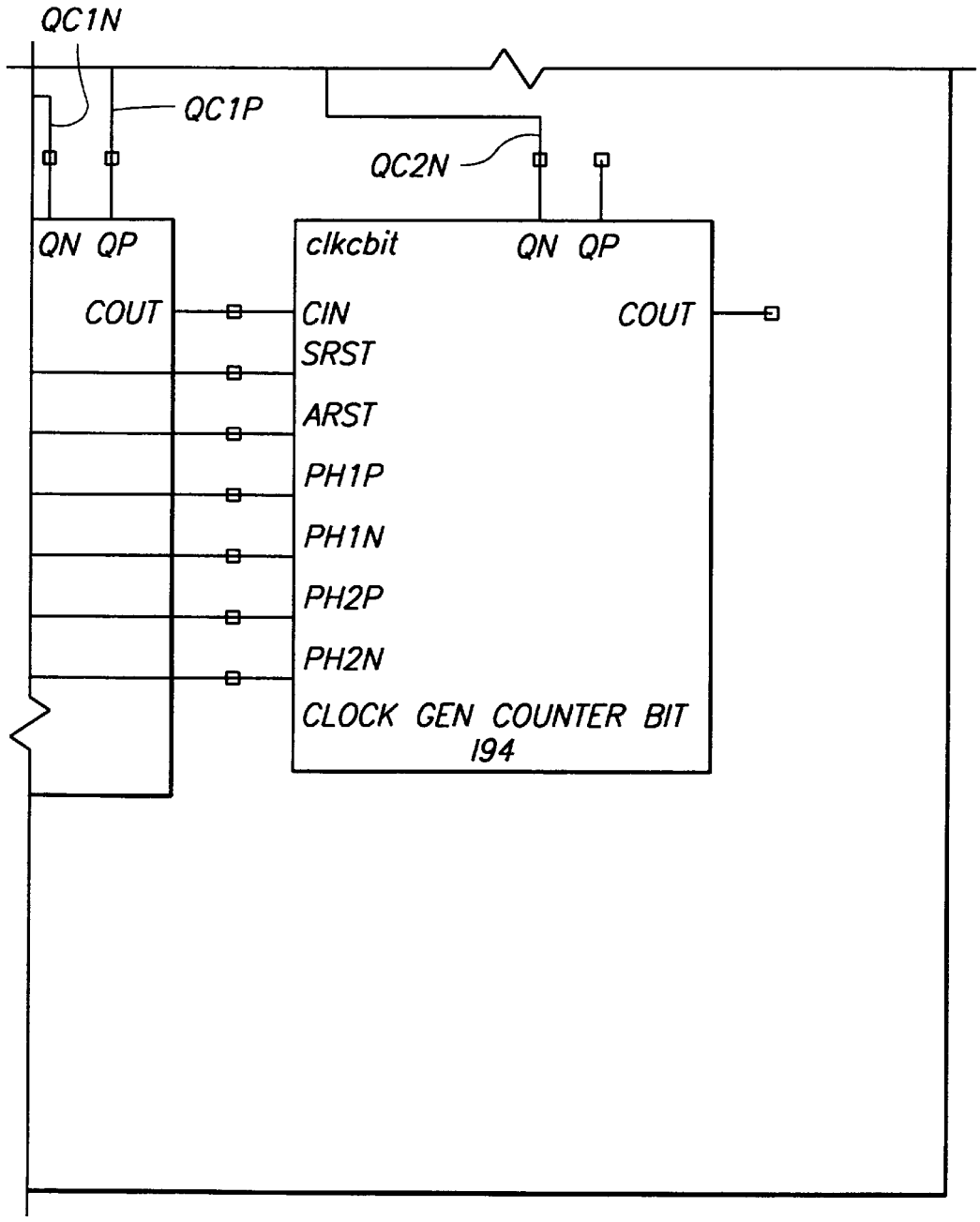

QC1N
QC1P
QC2N
QN QP
COUT
clkcbit
QN QP
CIN
COUT
SRST
ARST
PH1P
PH1N
PH2P
PH2N
CLOCK GEN COUNTER BIT
194

Fig 1.0103BD

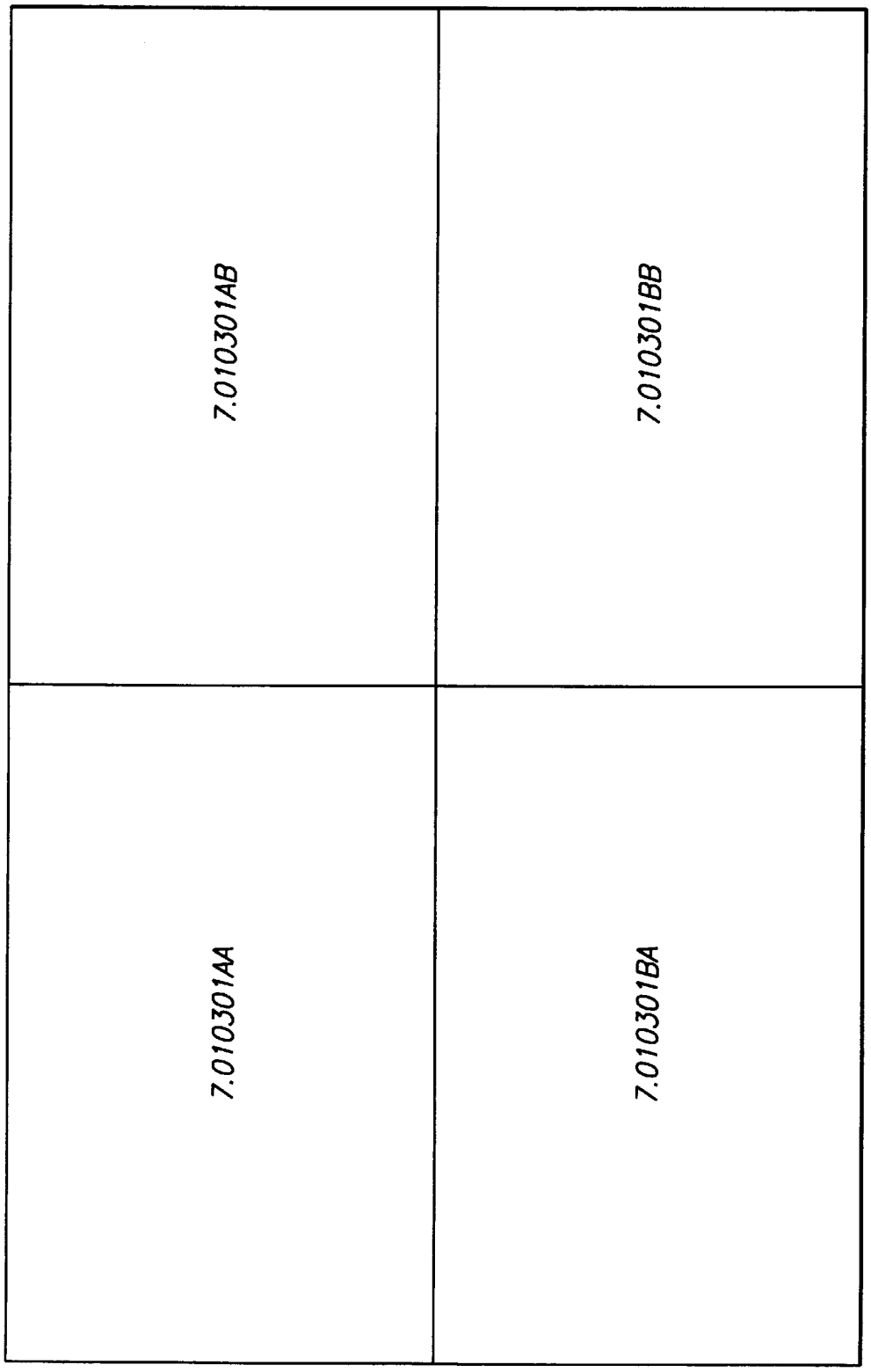


FIG 71

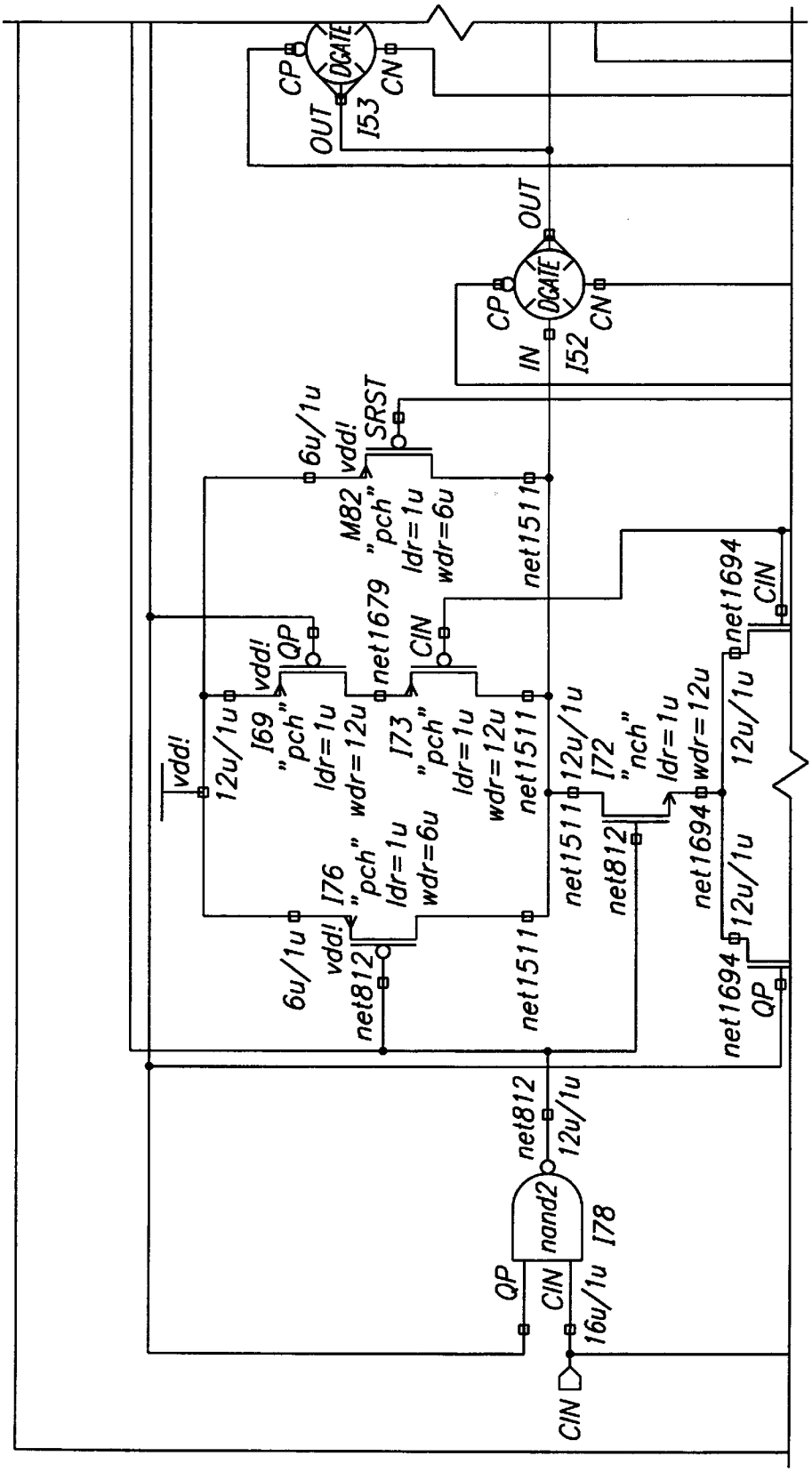


FIG. 11.00E 00 11 AA

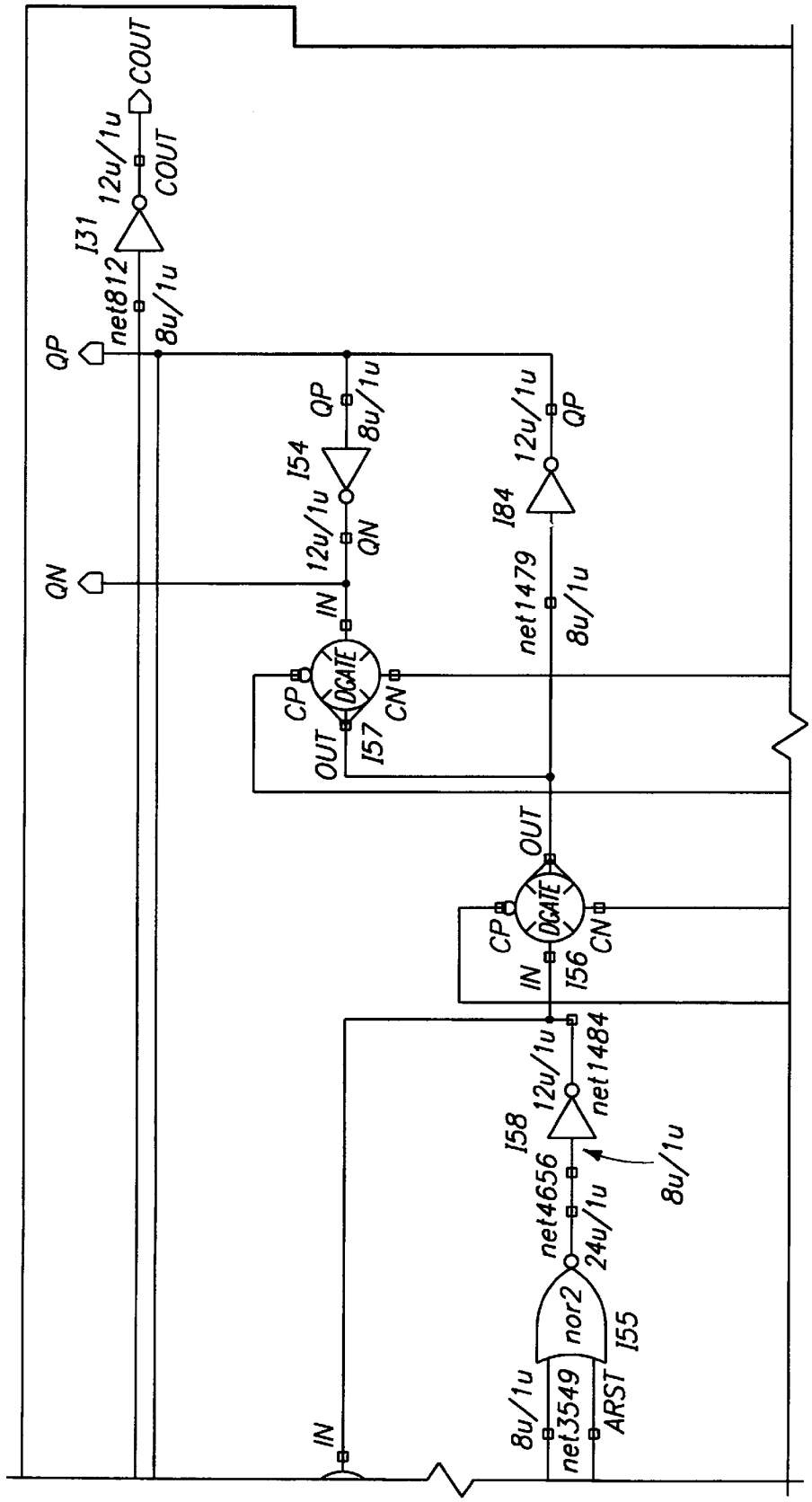

COUT
12u/1u
COUT
I31
net812
8u/1u
QP
QN
I54
QP
8u/1u
12u/1u
QN
IN
I84
12u/1u
QP
net1479
8u/1u
CP
OCAIE
CN
OUT
I57
OUT
CP
OCAIE
CN
IN
I56
I58
12u/1u
net1484
net4656
24u/1u
8u/1u
nor2
I55
8u/1u
net3549
ARST
IN

FIG. 1L

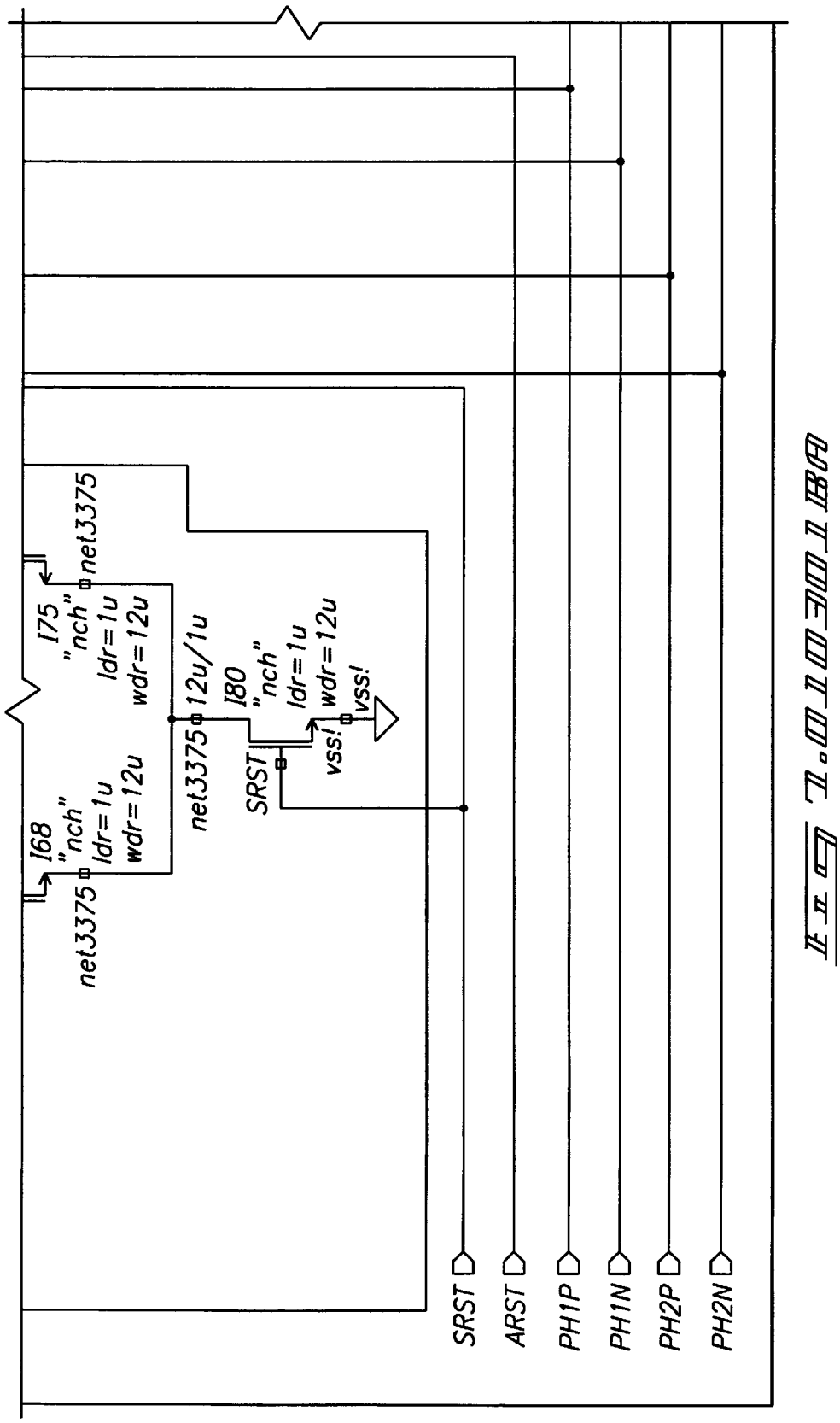

I68
"nch"
ldr=1u
wdr=12u
net3375
I75
"nch"
ldr=1u
wdr=12u
net3375
net3375
12u/1u
I80
"nch"
ldr=1u
wdr=12u
SRST
vss!
vss!
SRST
ARST
PH1P
PH1N
PH2P
PH2N

Fig. 187

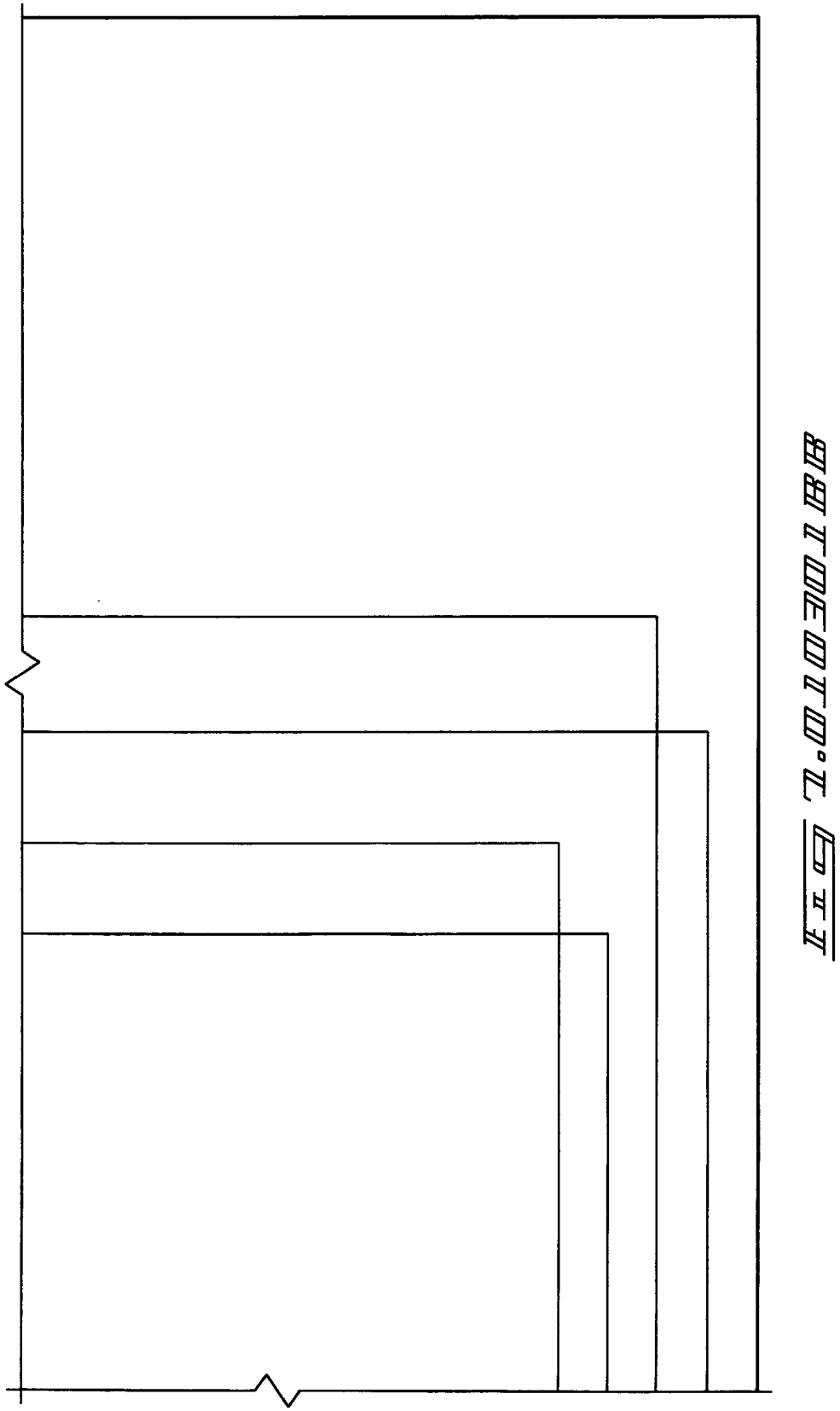


FIG. 7C

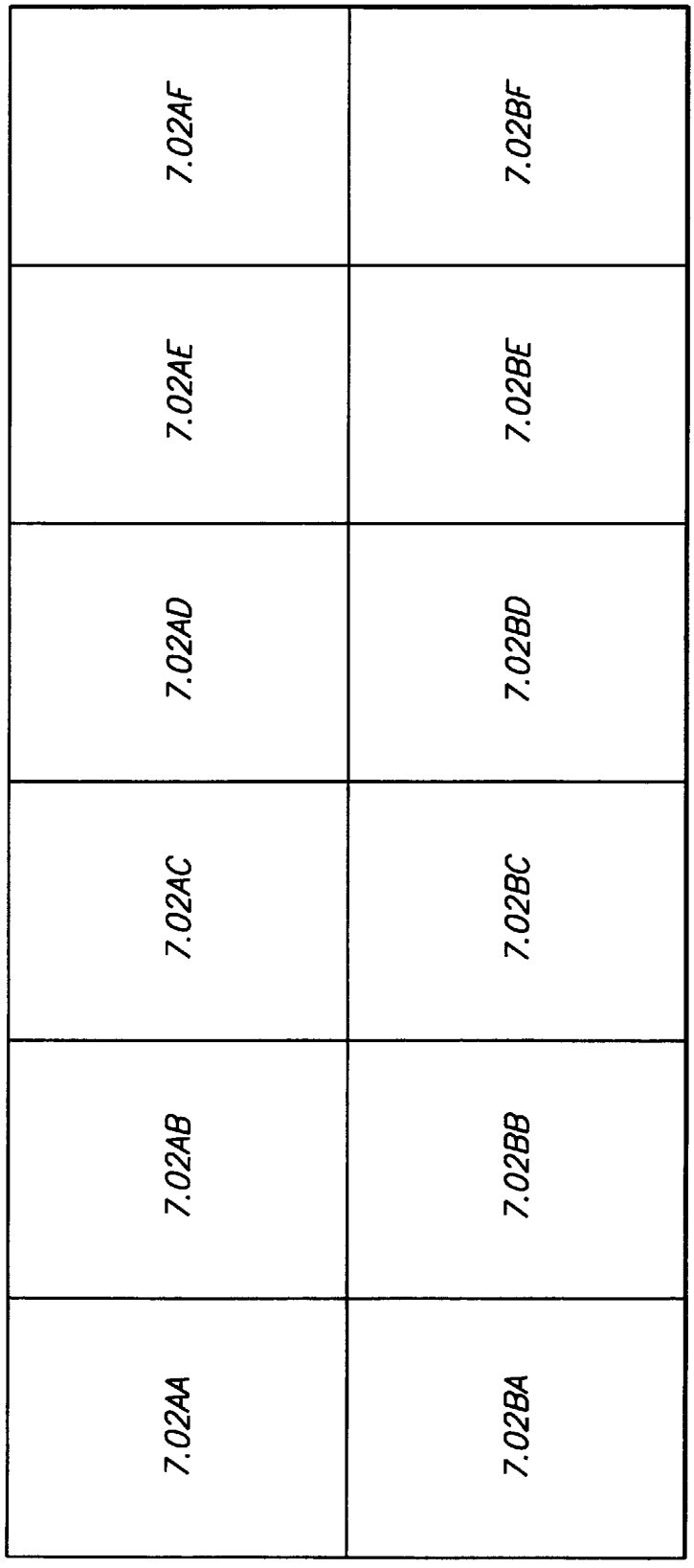

7.02AF
7.02BF
7.02AE
7.02BE
7.02AD
7.02BD
7.02AC
7.02BC
7.02AB
7.02BB
7.02AA
7.02BA

FIG. 7.02

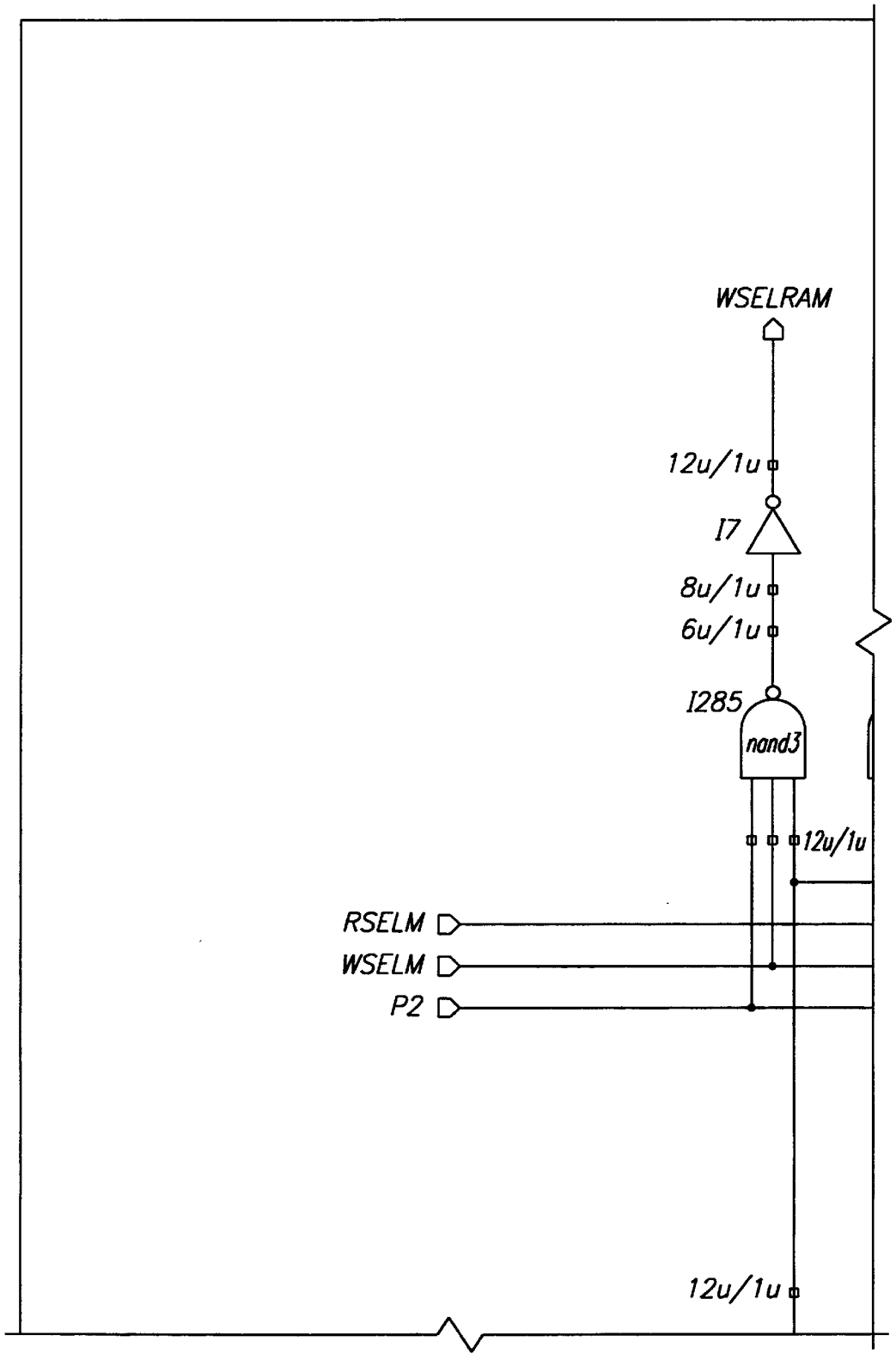

WSELRAM
12u/1u
I7
8u/1u
6u/1u
I285
nand3
12u/1u
RSELM
WSELM
P2
12u/1u

Fig 1.02AA

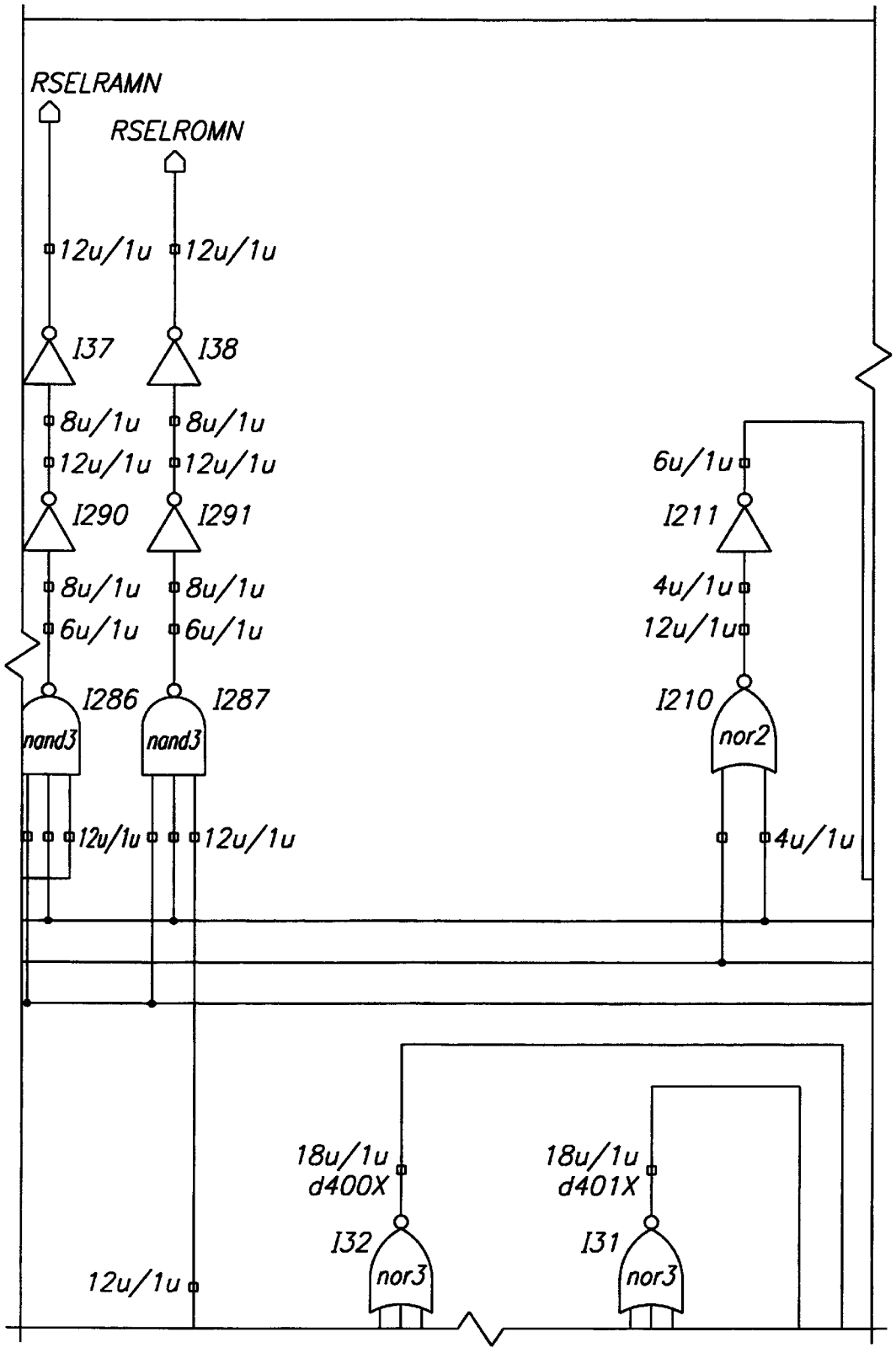

RSELRAMN
RSELROMN
12u/1u
12u/1u
I37
I38
8u/1u
8u/1u
12u/1u
12u/1u
I290
I291
8u/1u
8u/1u
6u/1u
6u/1u
I286
I287
nand3
nand3
12u/1u
12u/1u
6u/1u
I211
4u/1u
12u/1u
I210
nor2
4u/1u
18u/1u
d400X
18u/1u
d401X
I32
I31
nor3
nor3
12u/1u

Fig 1.02AB

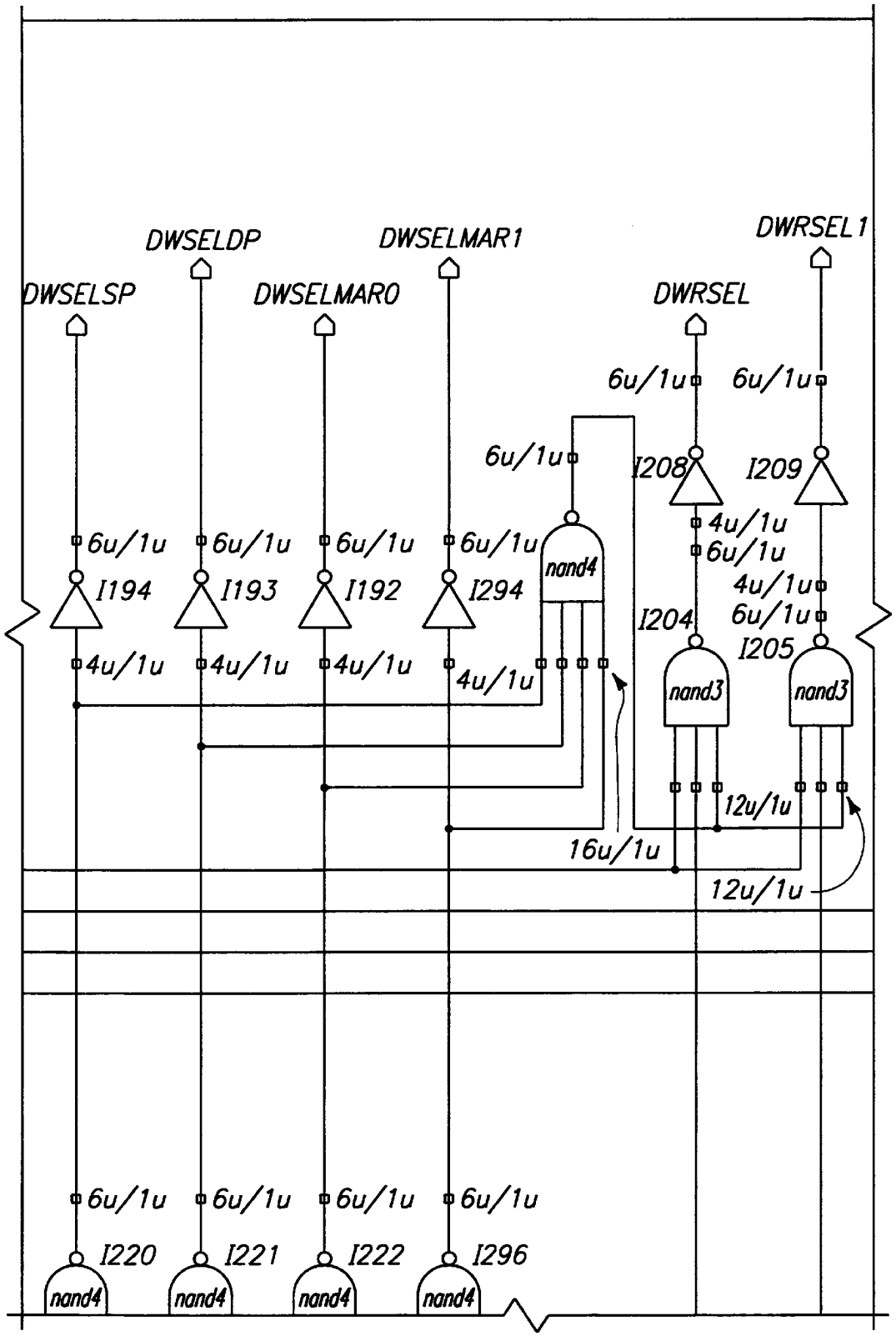
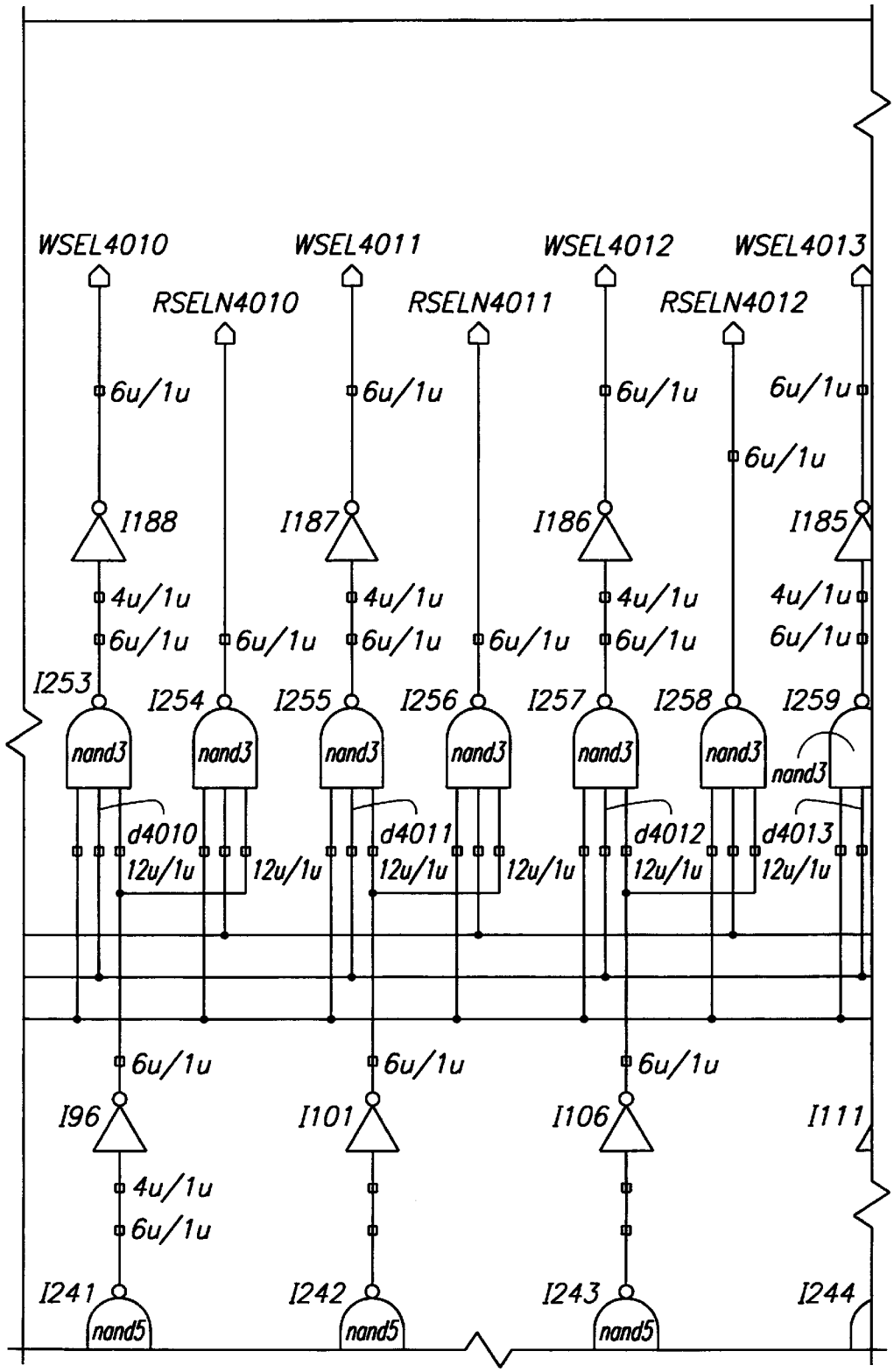

DWSELDP
DWSELMAR1
DWRSEL1
DWSELSP
DWSELMAR0
DWRSEL
6u/1u
6u/1u
6u/1u
I208
I209
6u/1u
6u/1u
6u/1u
6u/1u
nand4
4u/1u
6u/1u
I194
I193
I192
I294
4u/1u
6u/1u
I204
I205
4u/1u
4u/1u
4u/1u
4u/1u
nand3
nand3
12u/1u
16u/1u
12u/1u
6u/1u
6u/1u
6u/1u
6u/1u
I220
I221
I222
I296
nand4
nand4
nand4
nand4

Fig 1.02AC


WSEL4010
WSEL4011
WSEL4012
WSEL4013
RSELN4010
RSELN4011
RSELN4012
6u/1u
I188
I187
I186
I185
4u/1u
I253
I254
I255
I256
I257
I258
I259
nand3
d4010
d4011
d4012
d4013
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I106
I111
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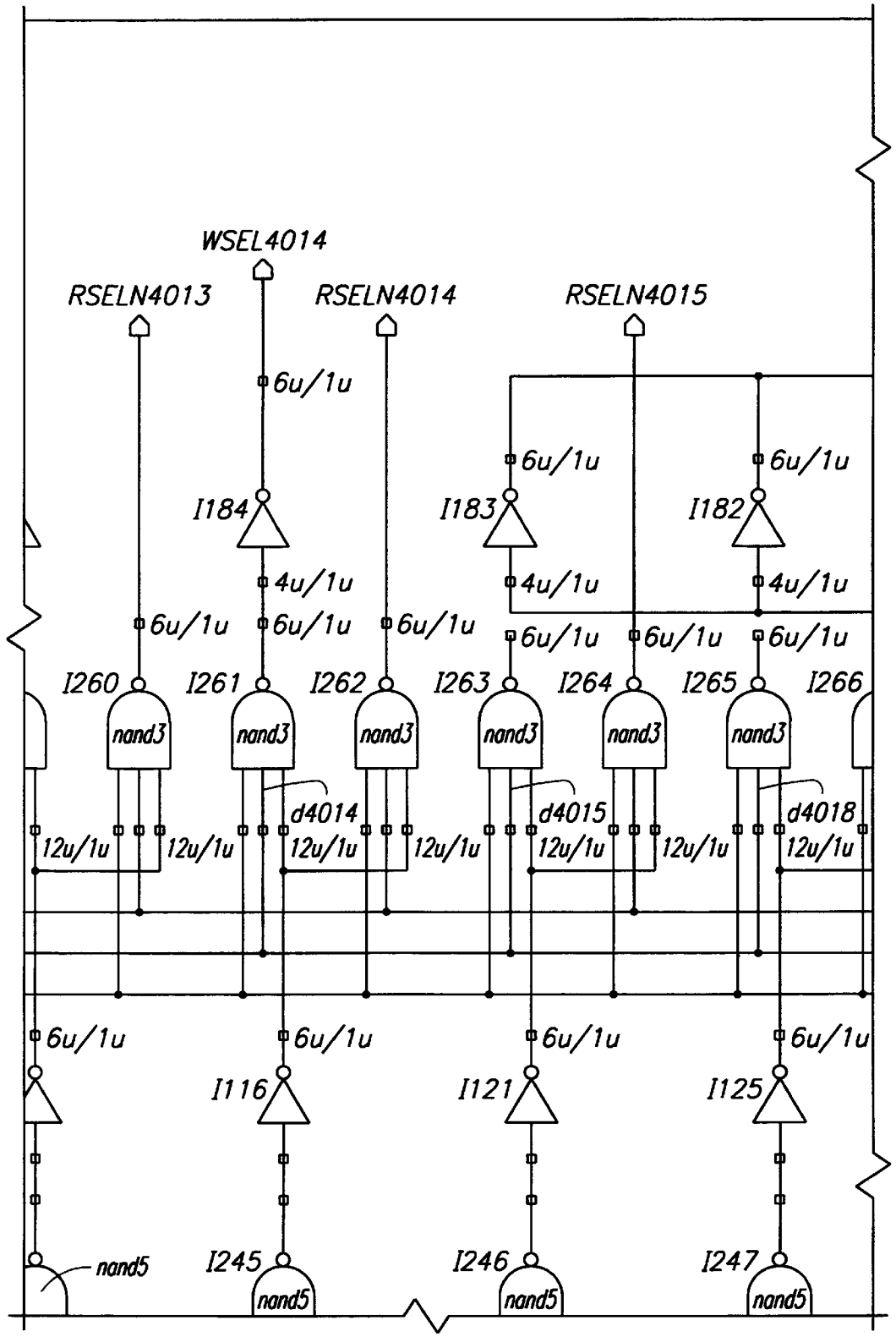
I243
I244
nand5

Fig 1.02AD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4u/1u
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I262
I263
I264
I265
I266
nand3
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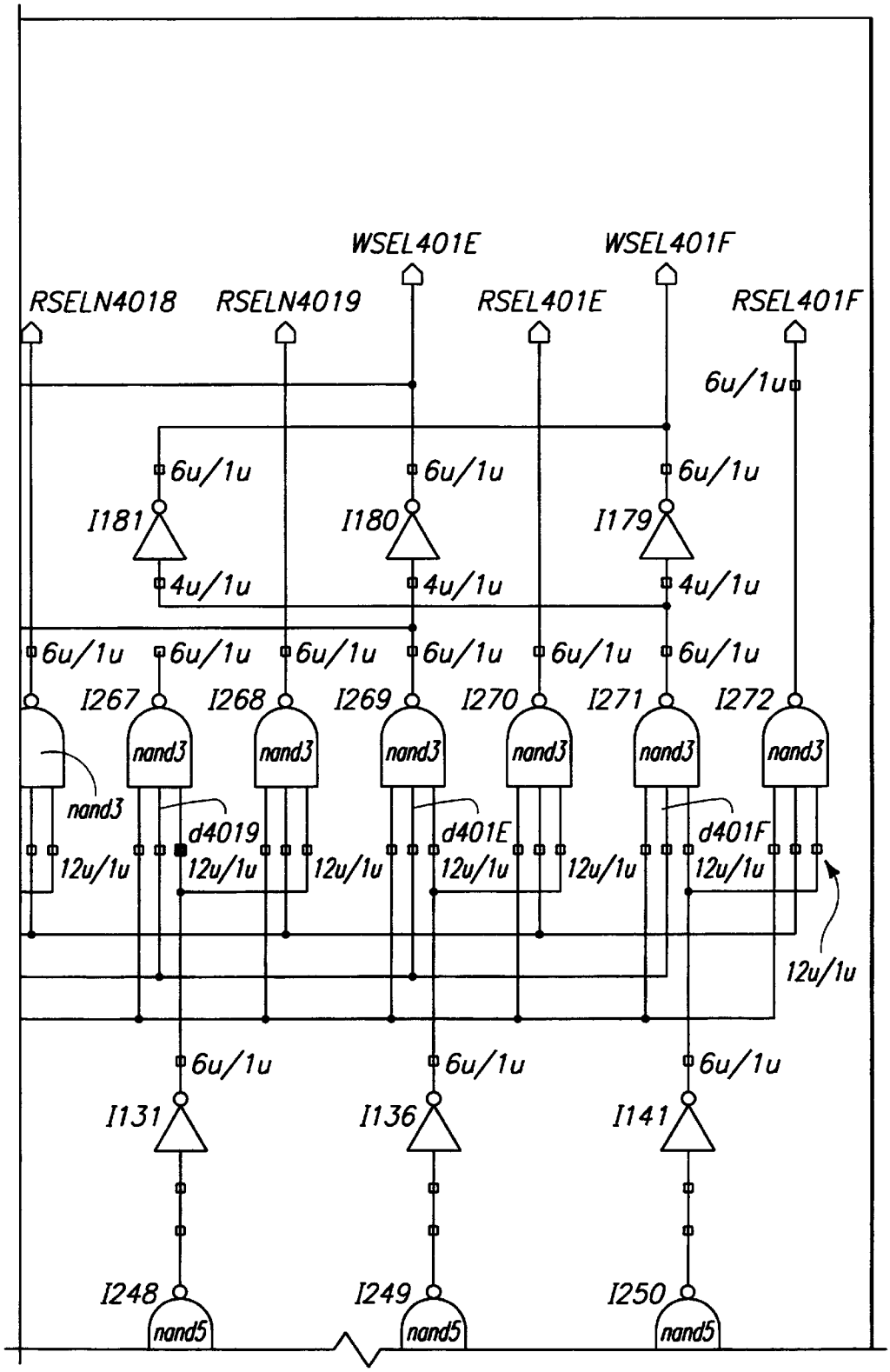
I121
I125
nand5
I245
I246
I247

FIG 1.02AE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I267
I268
I269
I270
I271
I272
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I141
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I249
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Fig 1 02AF

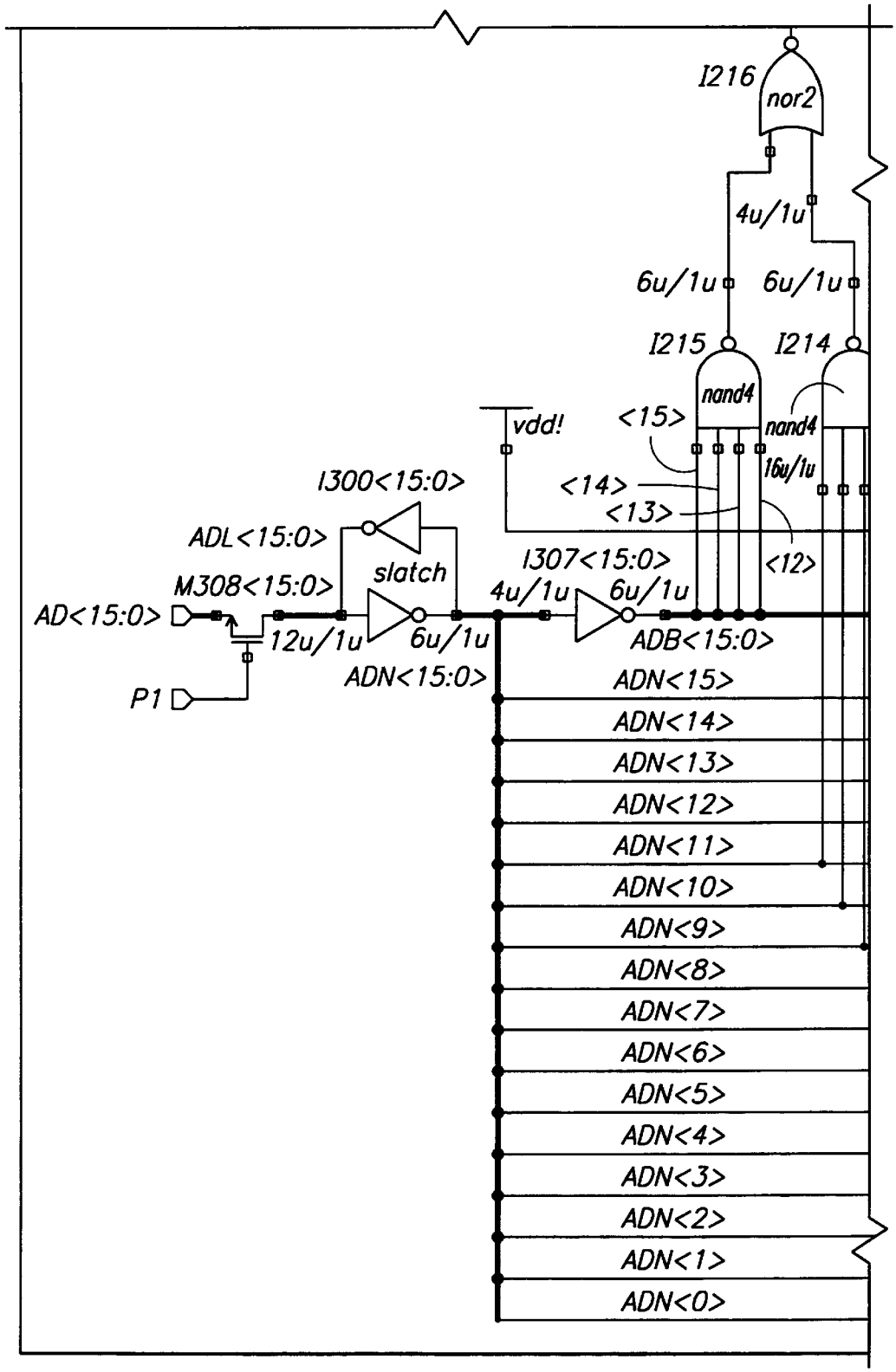
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Fig 1.02BA

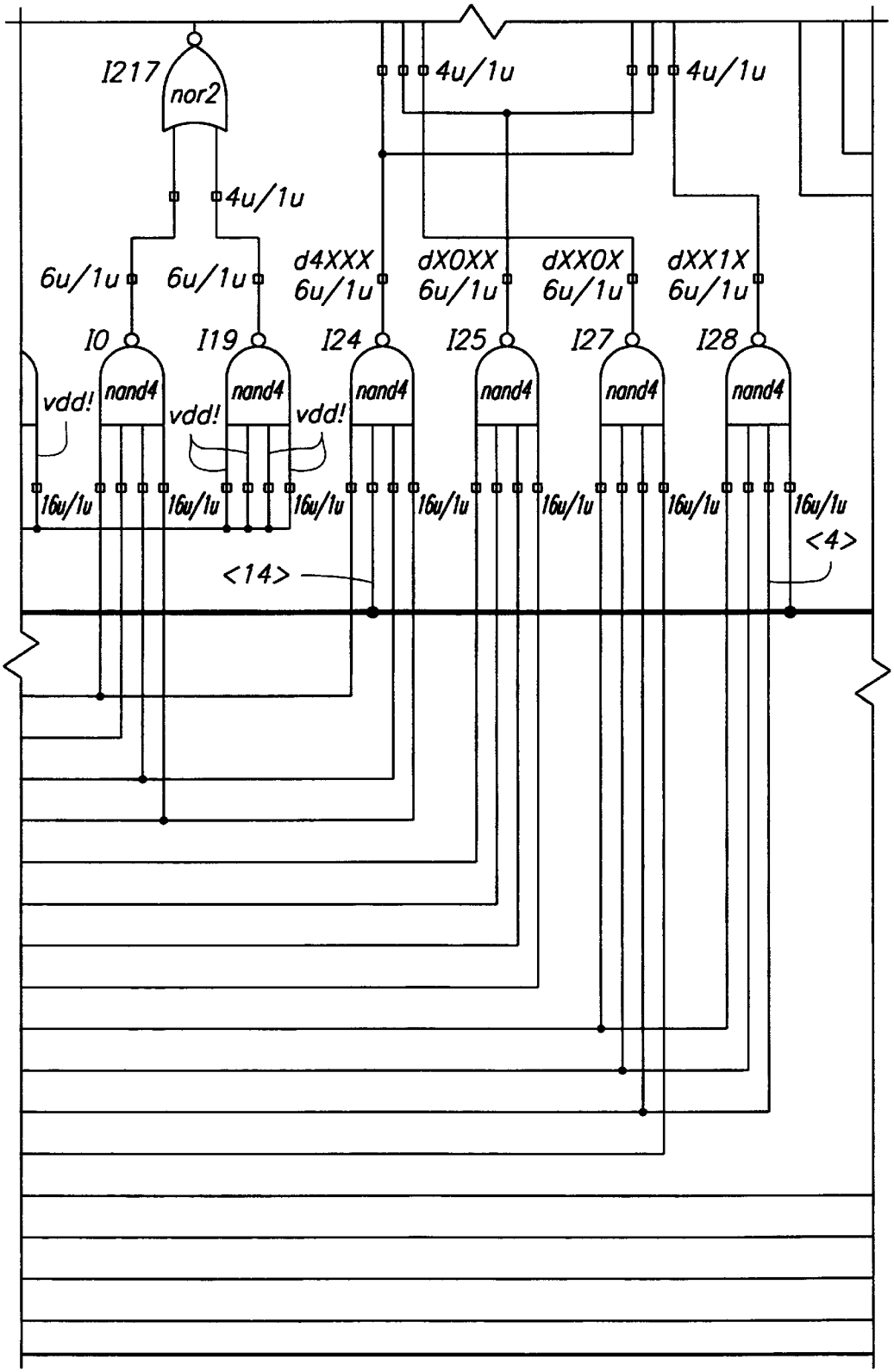
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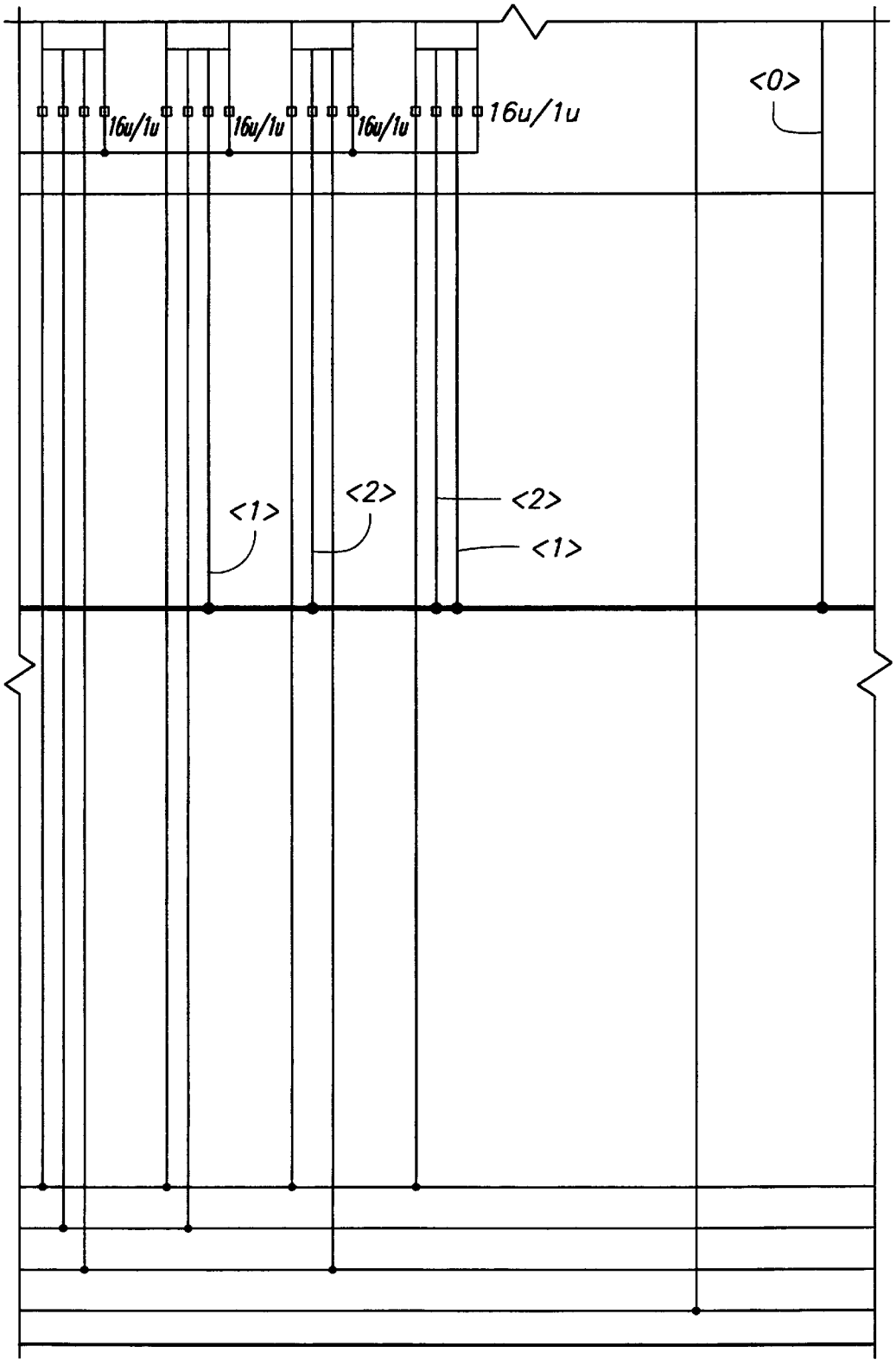
Fig 1.02BB



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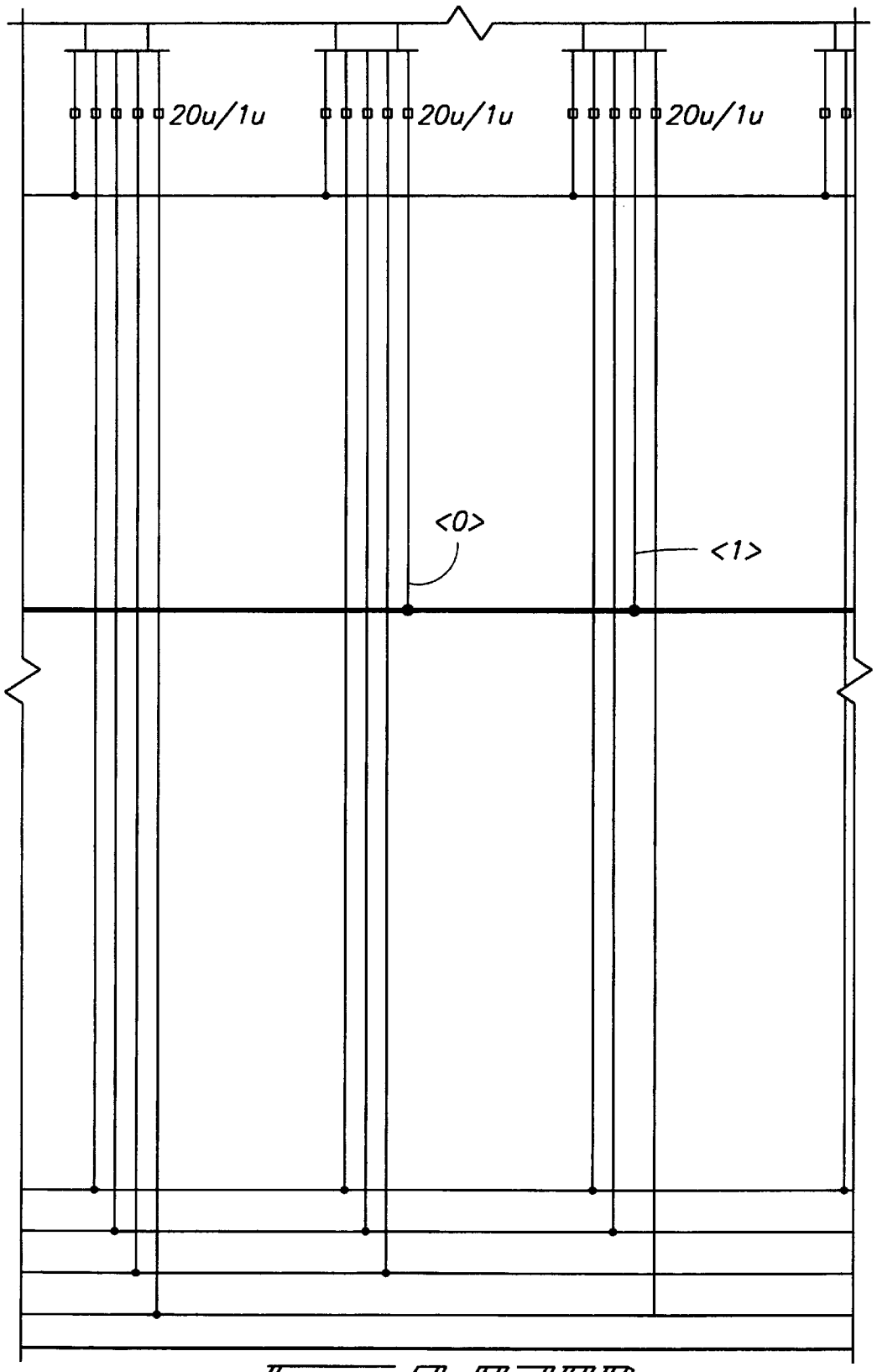

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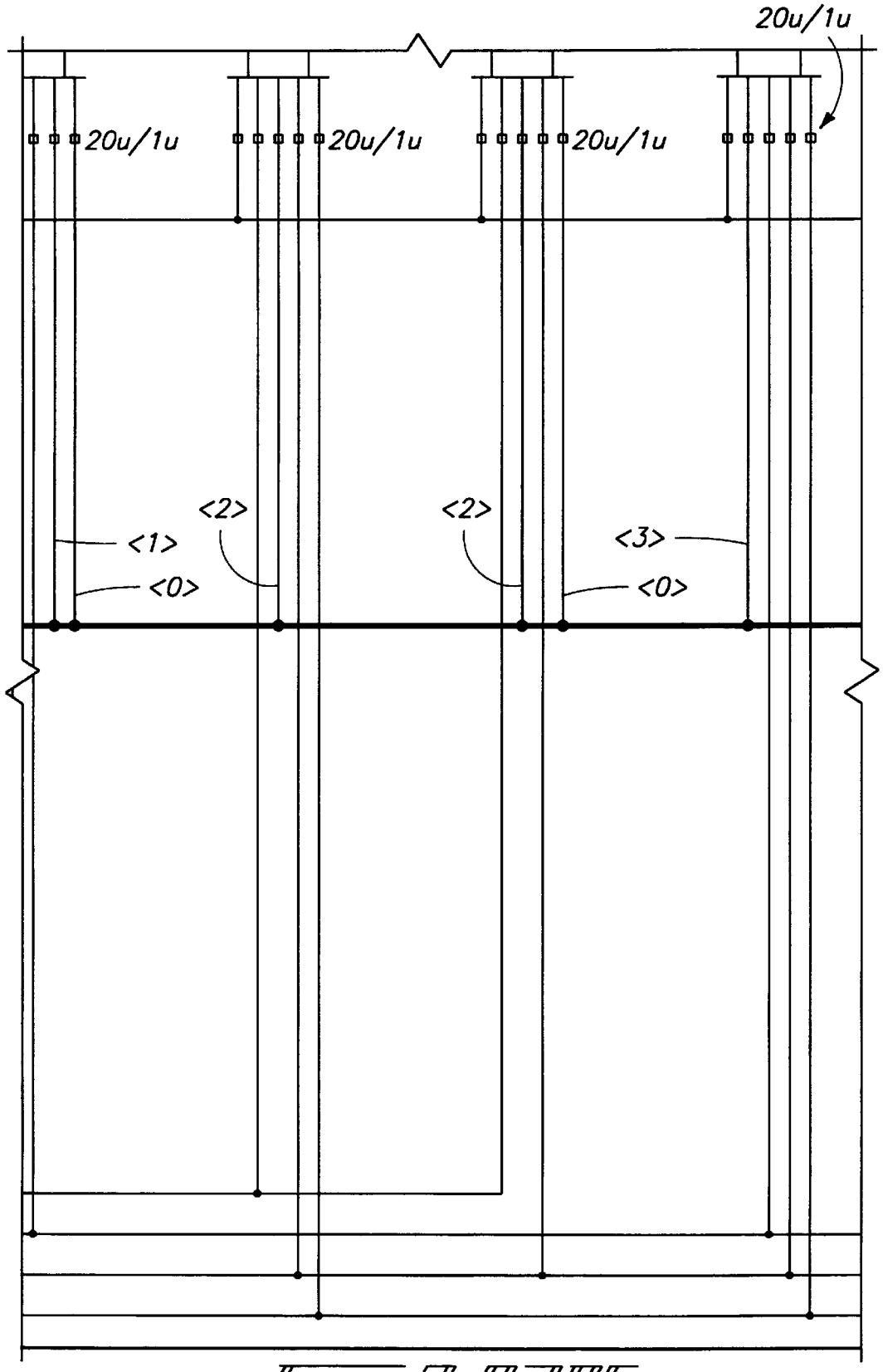

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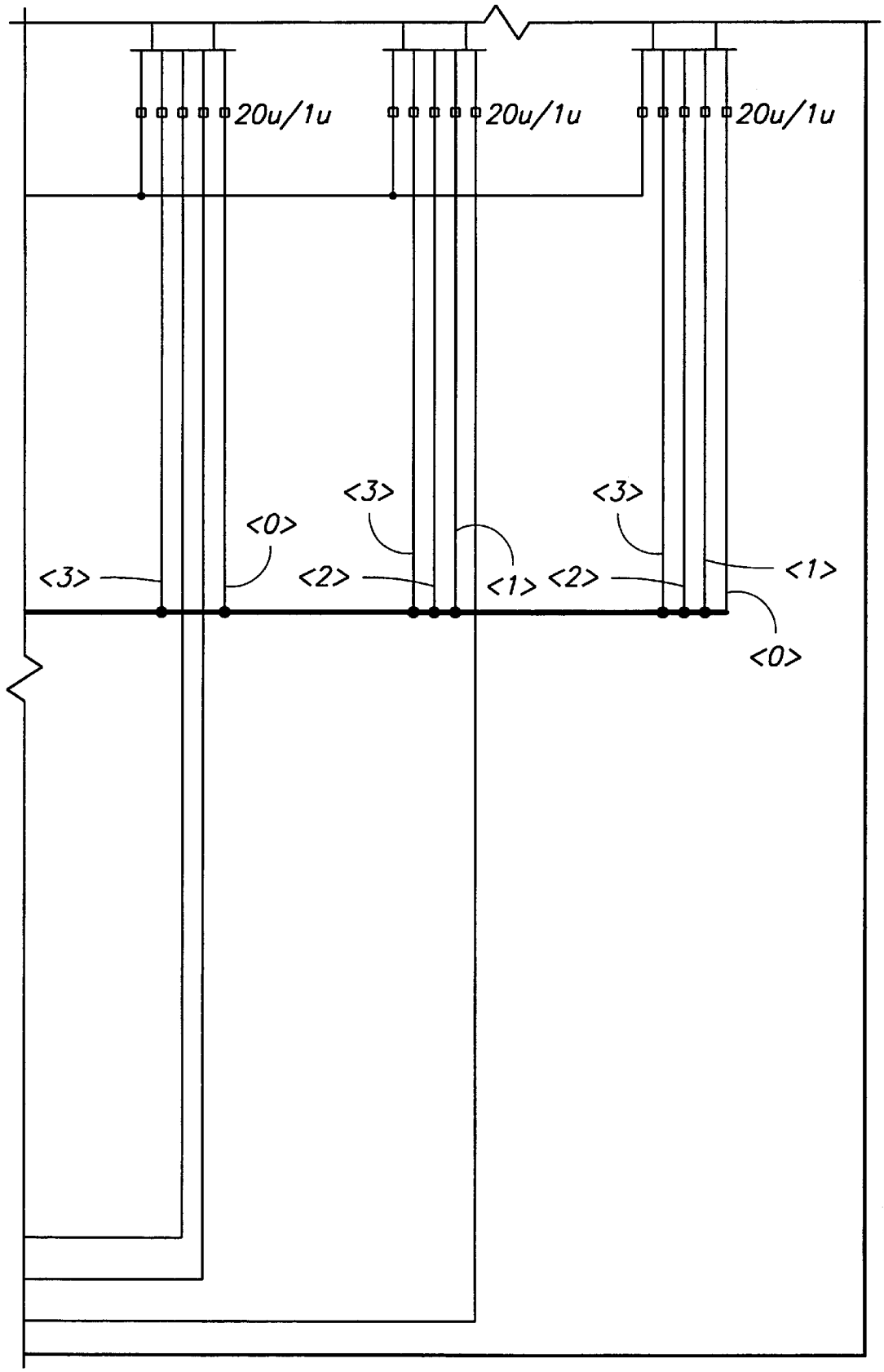

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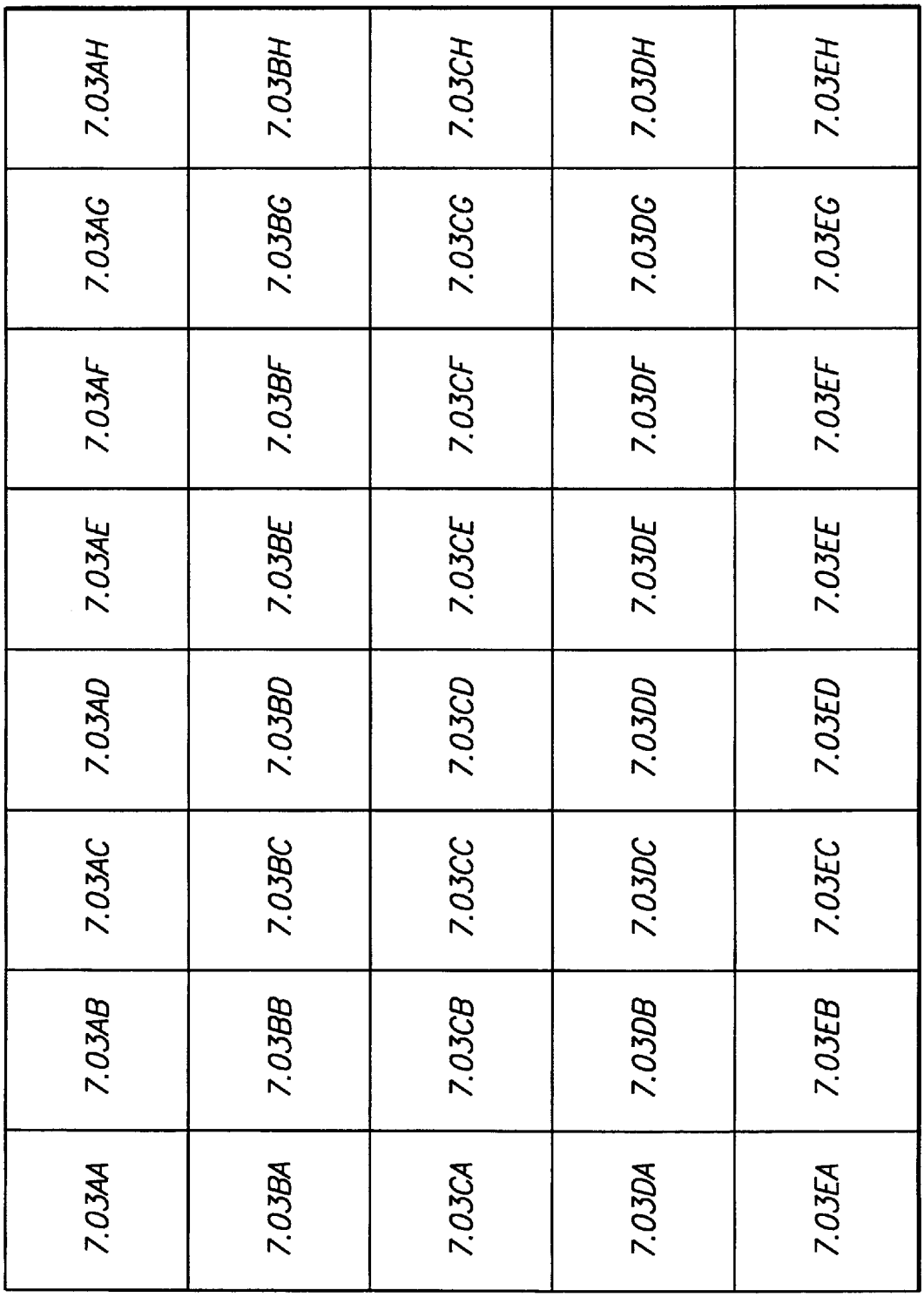
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7.03EG
7.03EH

FIG. 7.03E

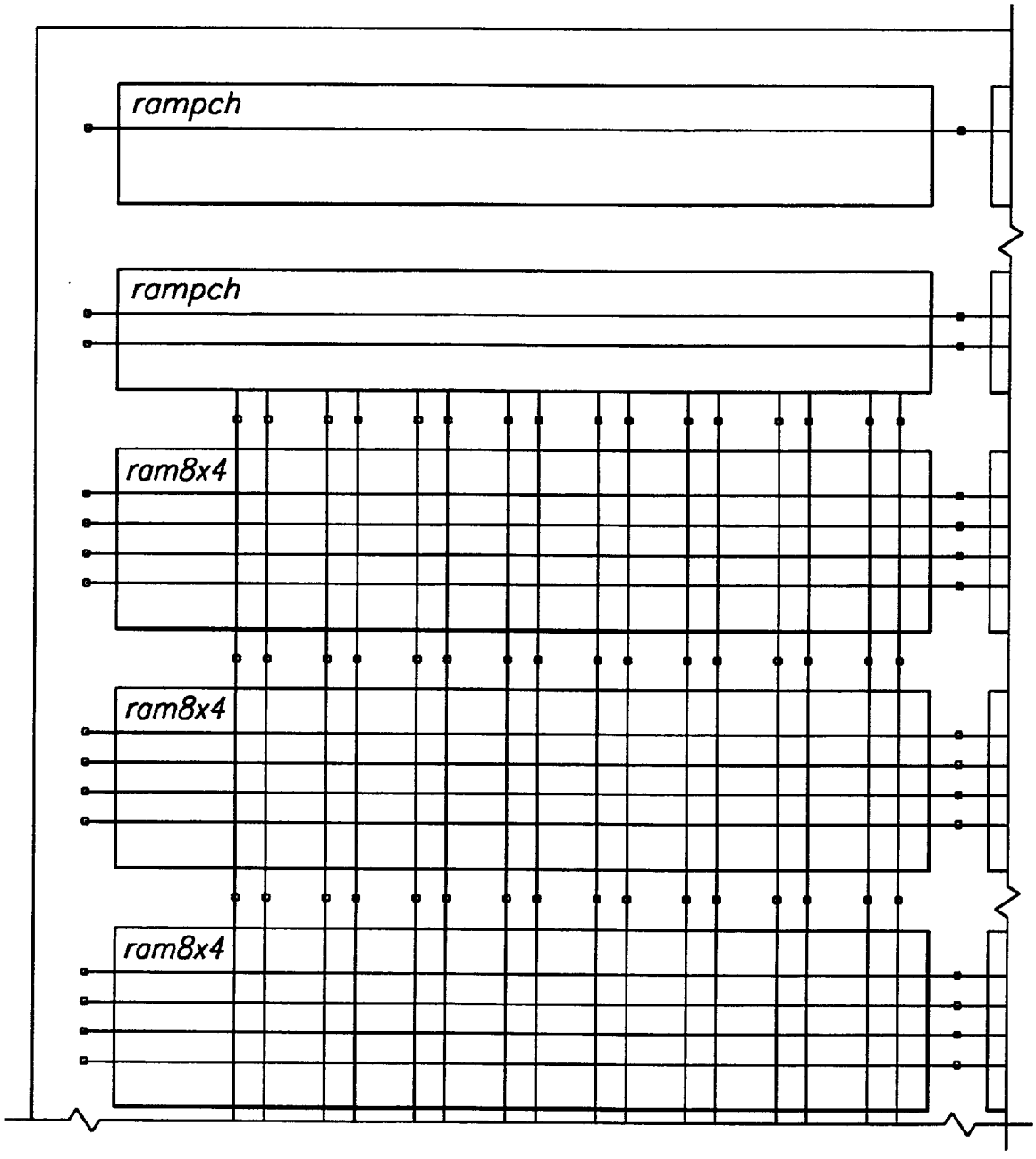

Fig 1.03AA

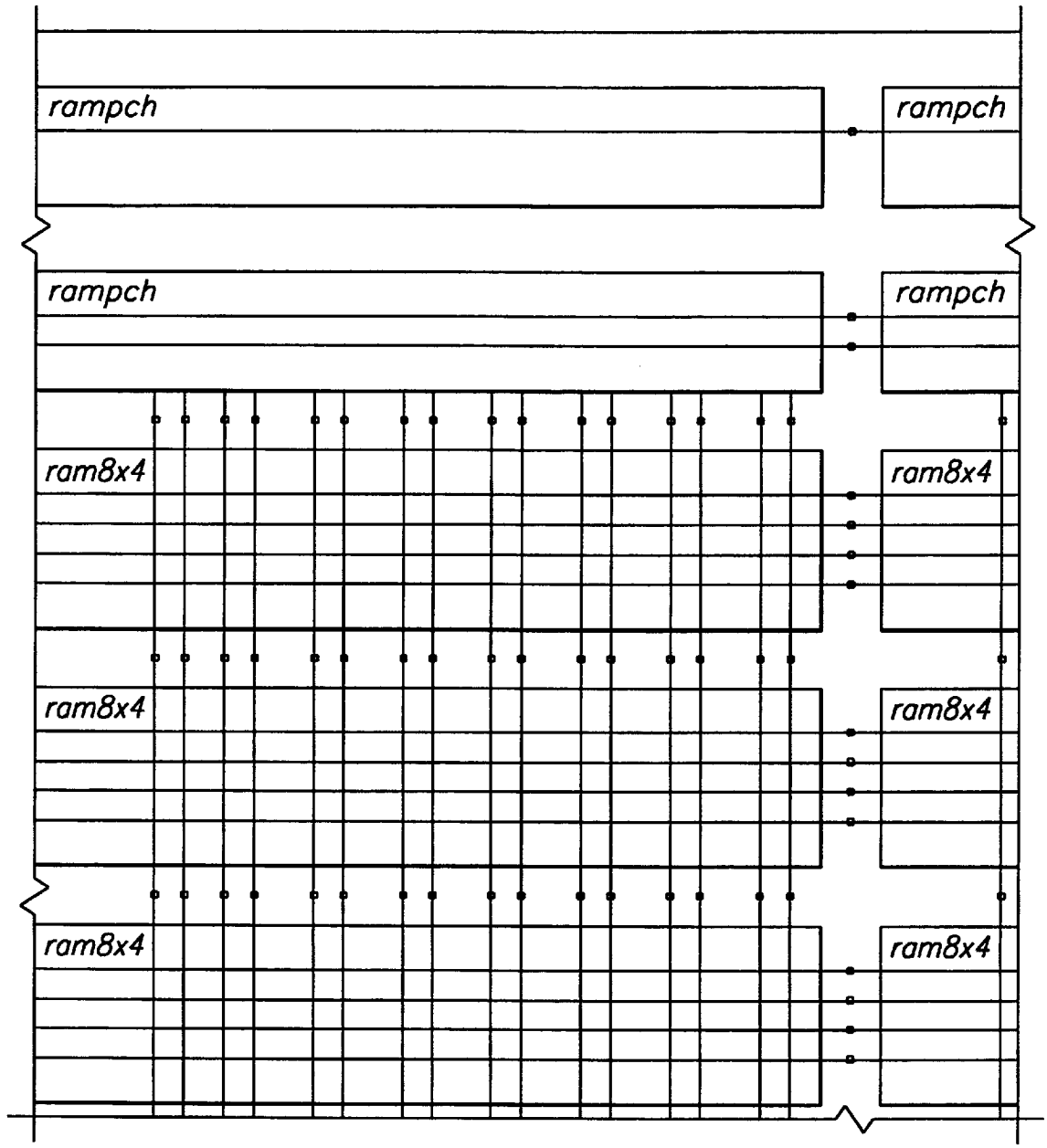
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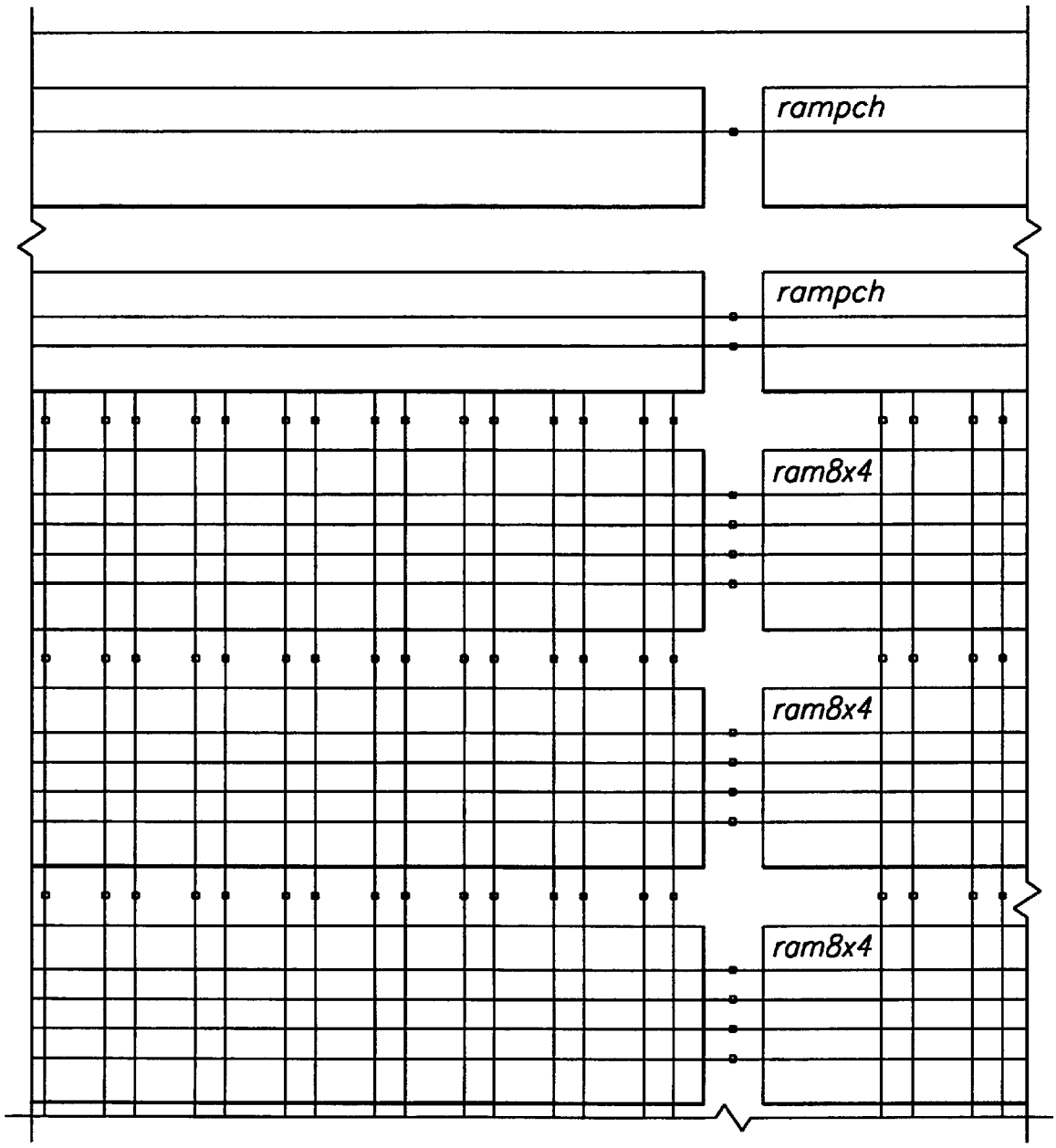
Fig 7.03AB



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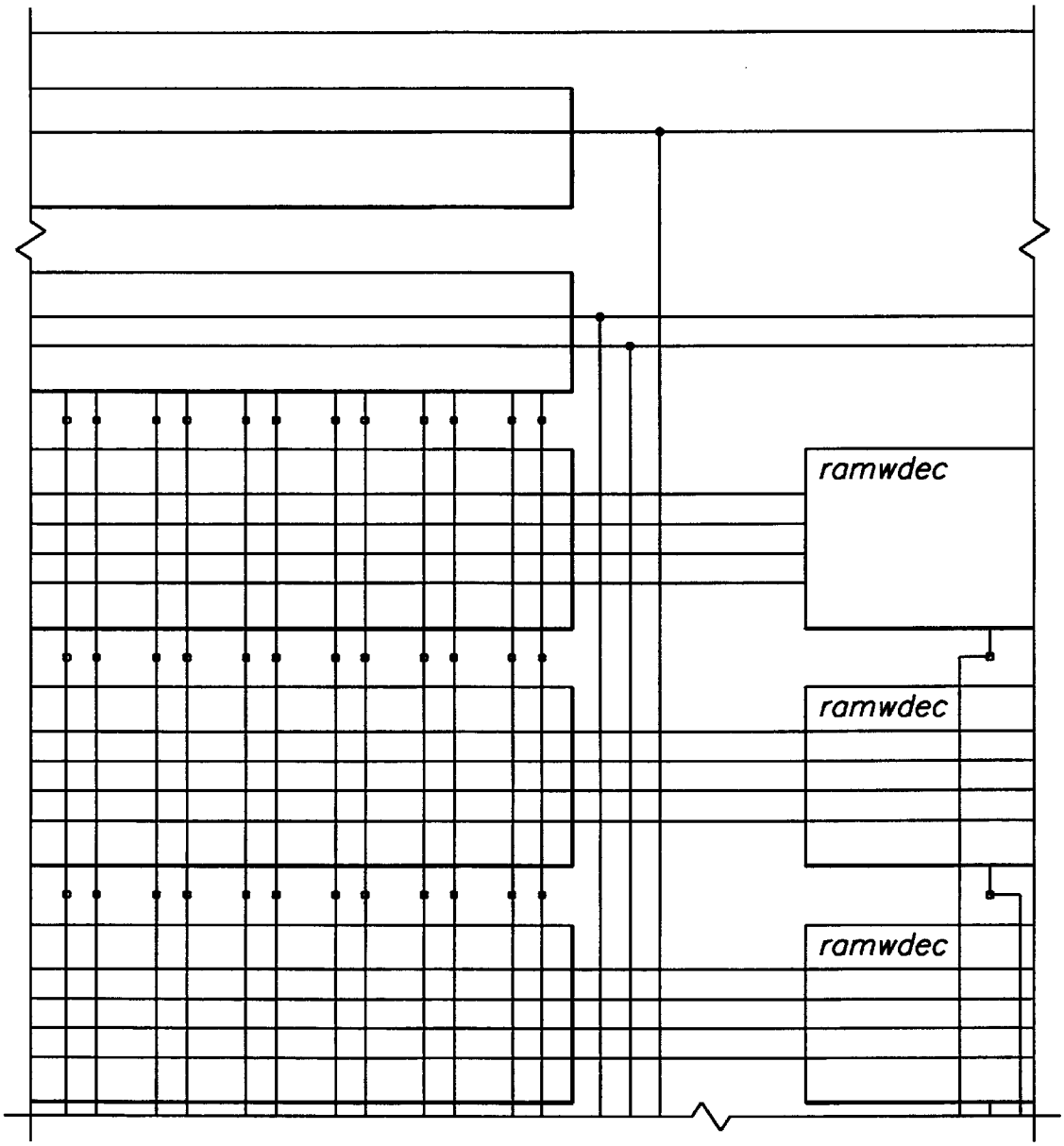

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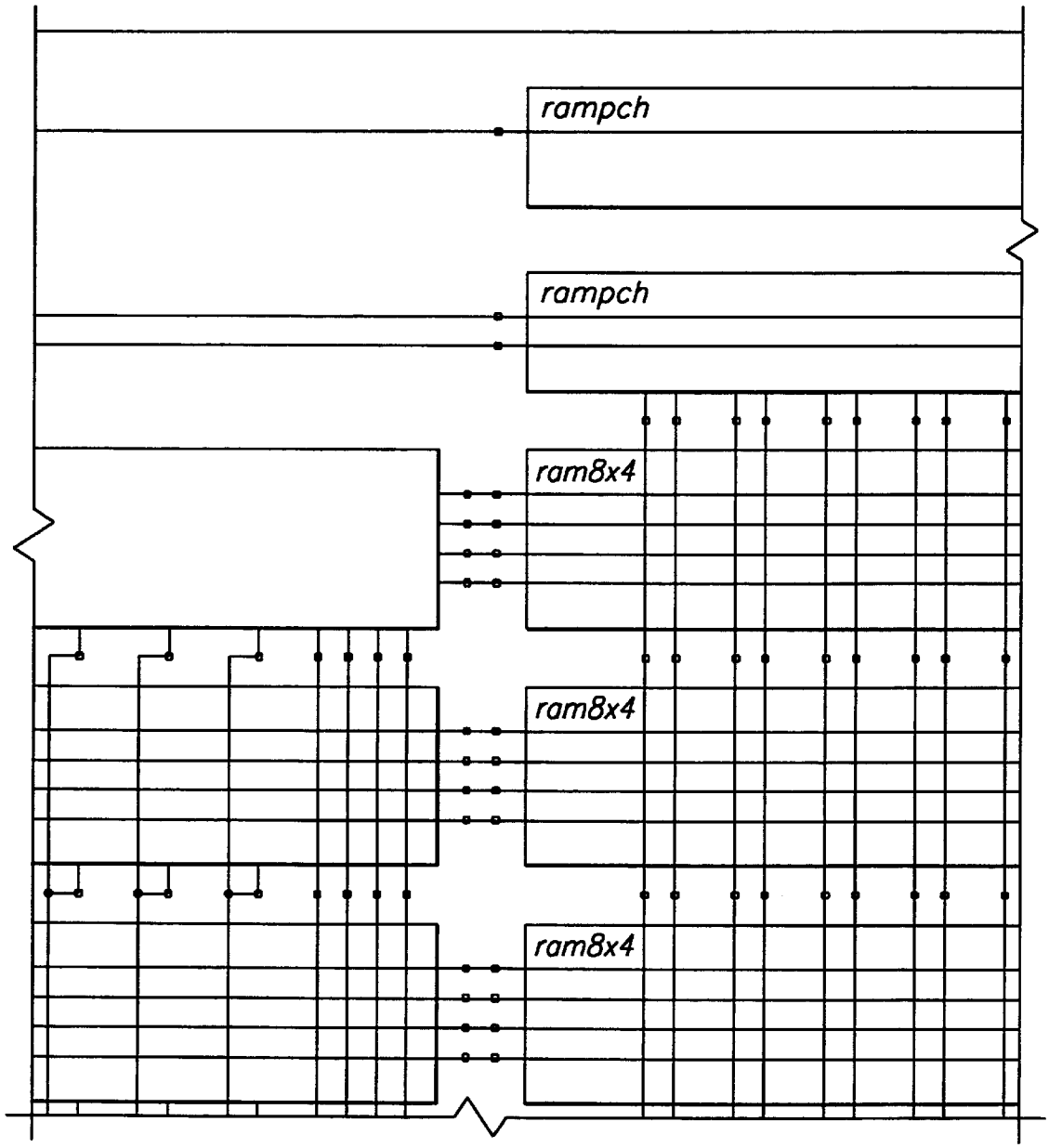

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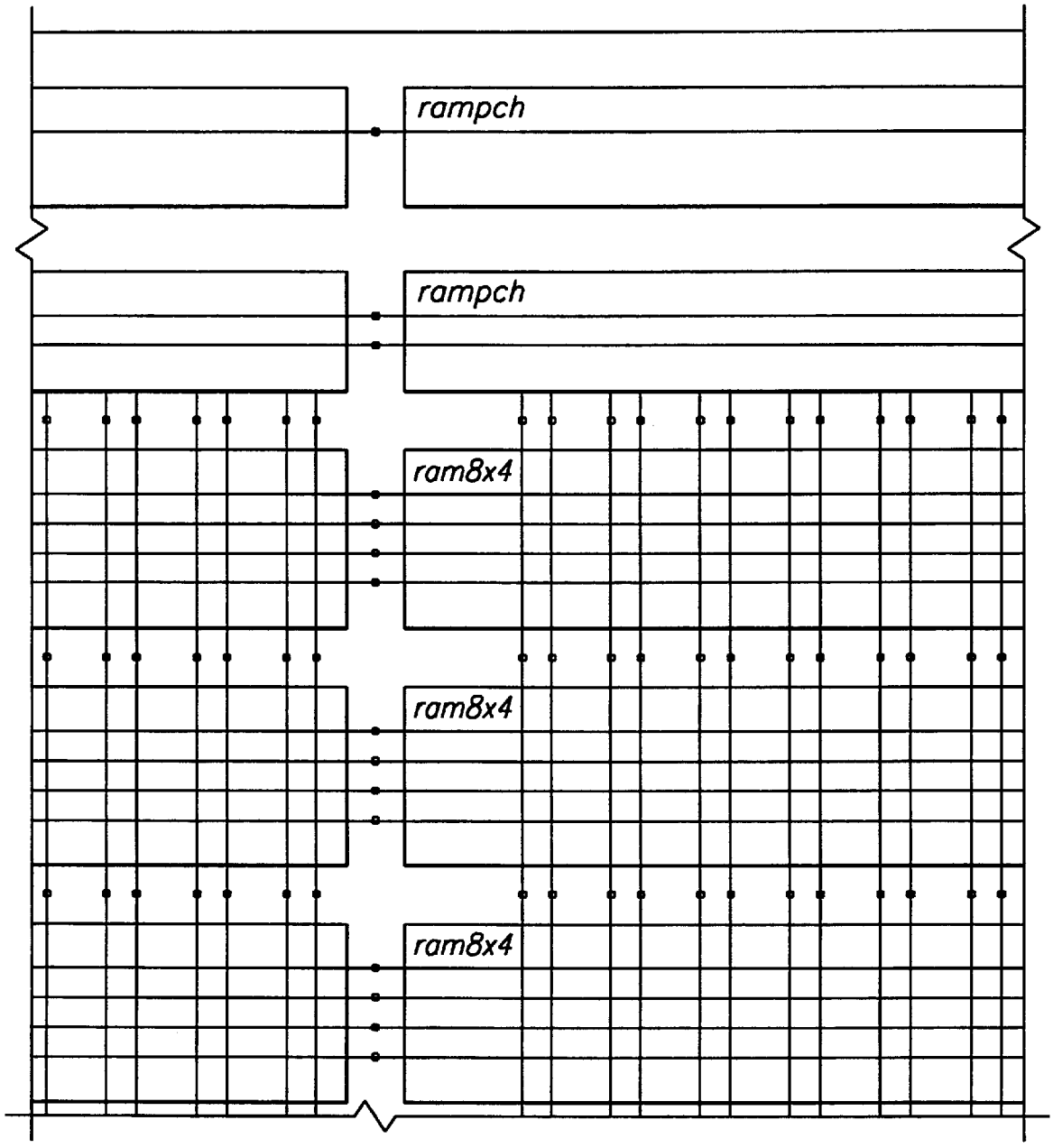

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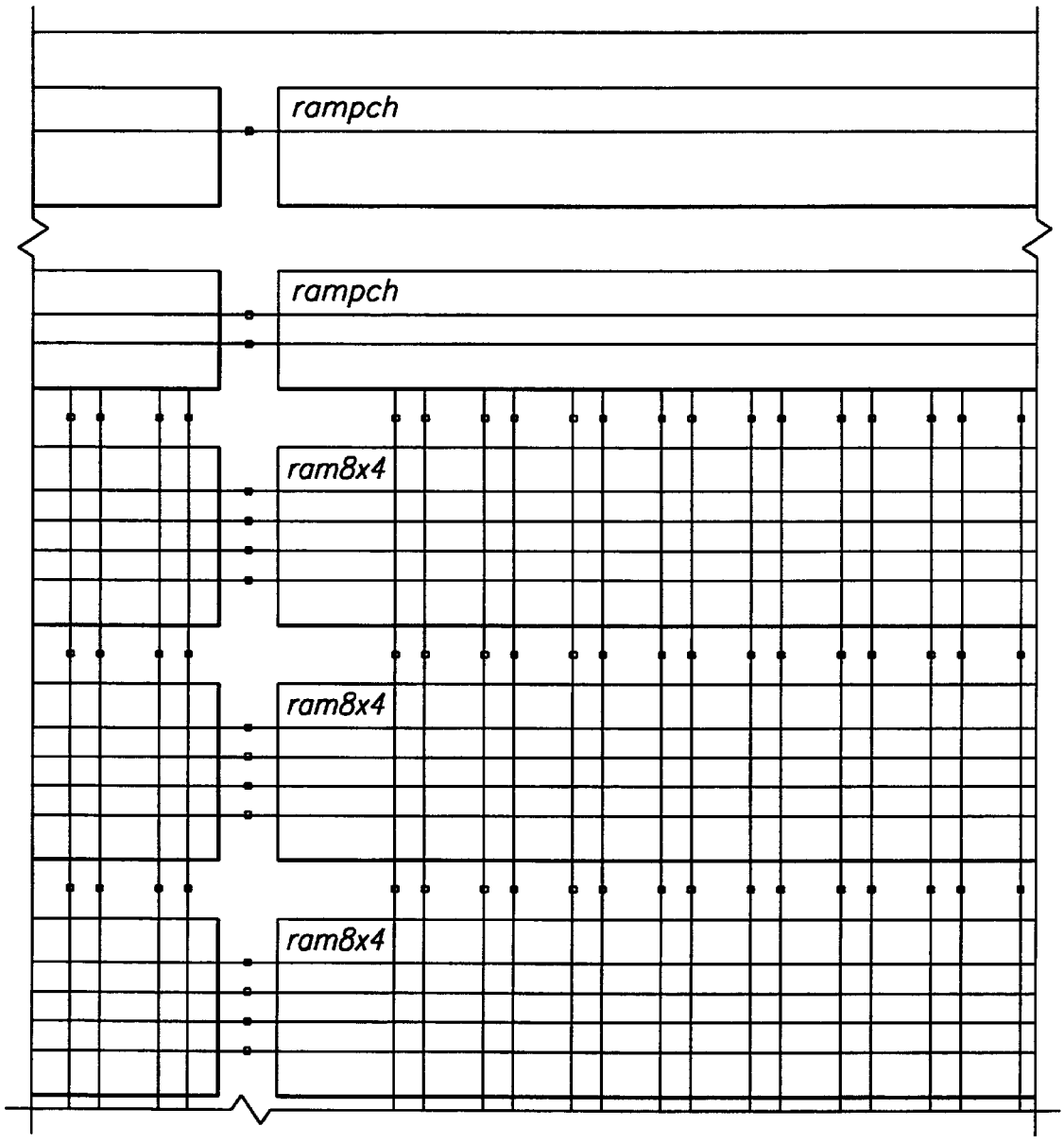

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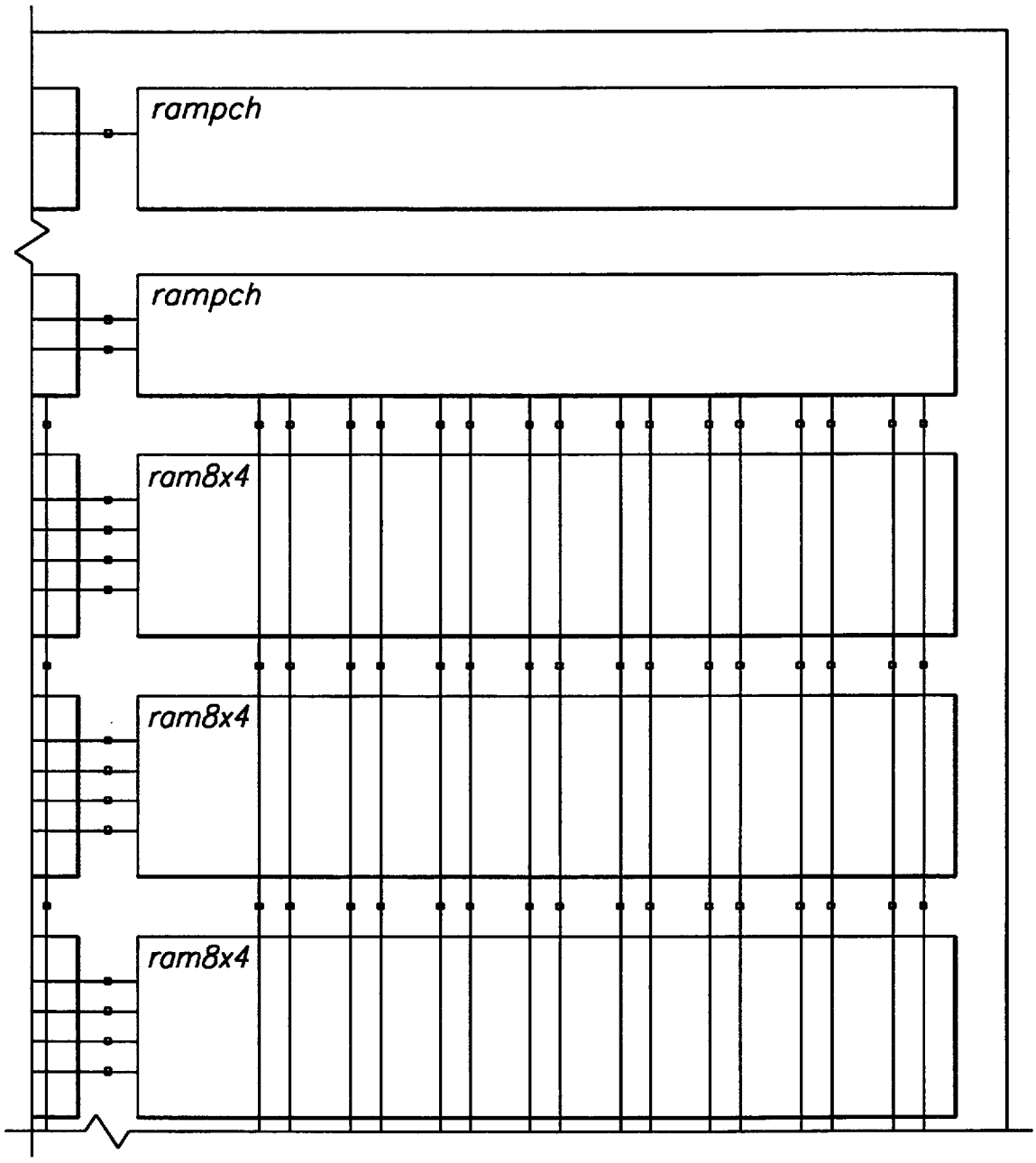

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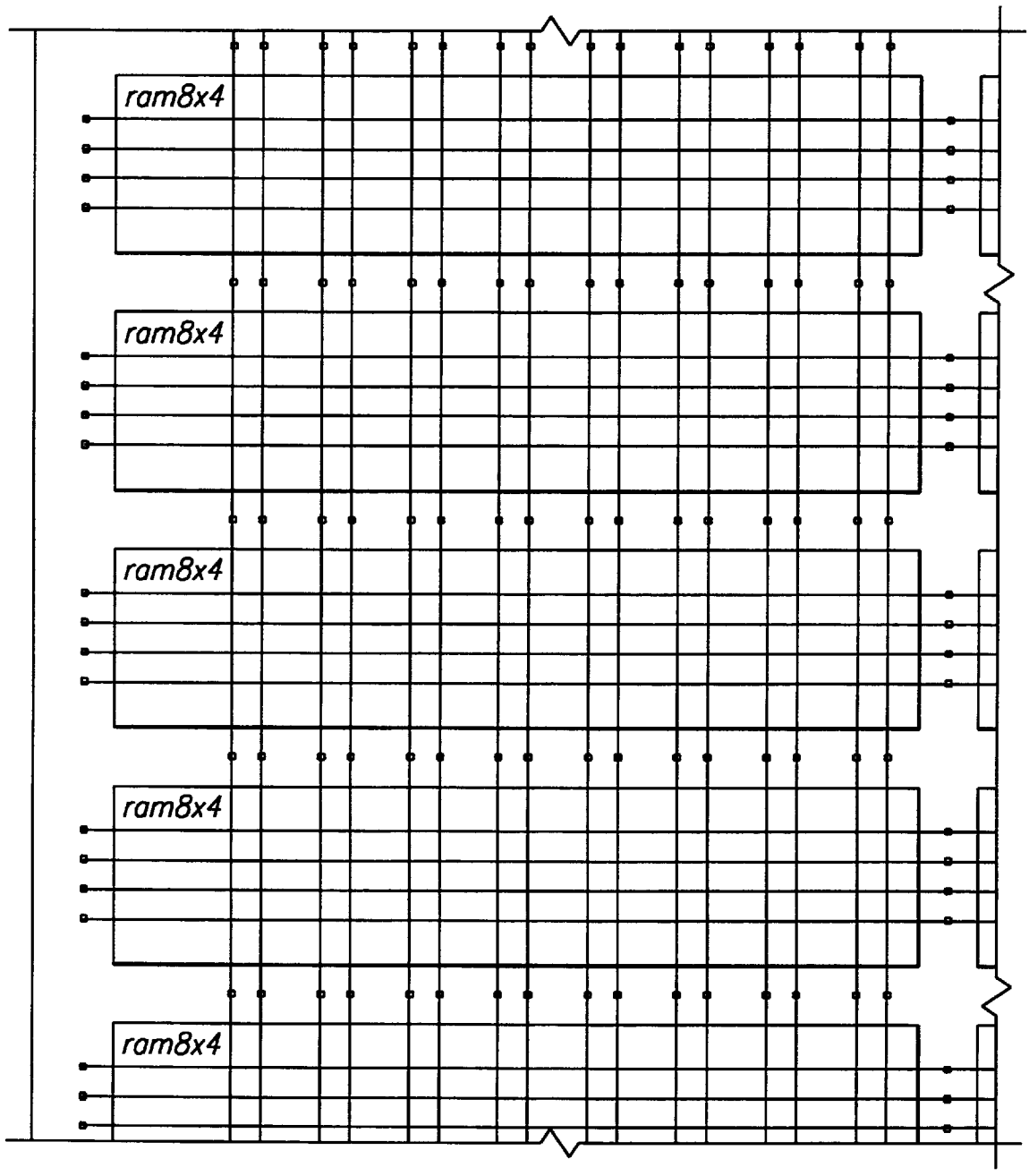

Fig 7.03BA

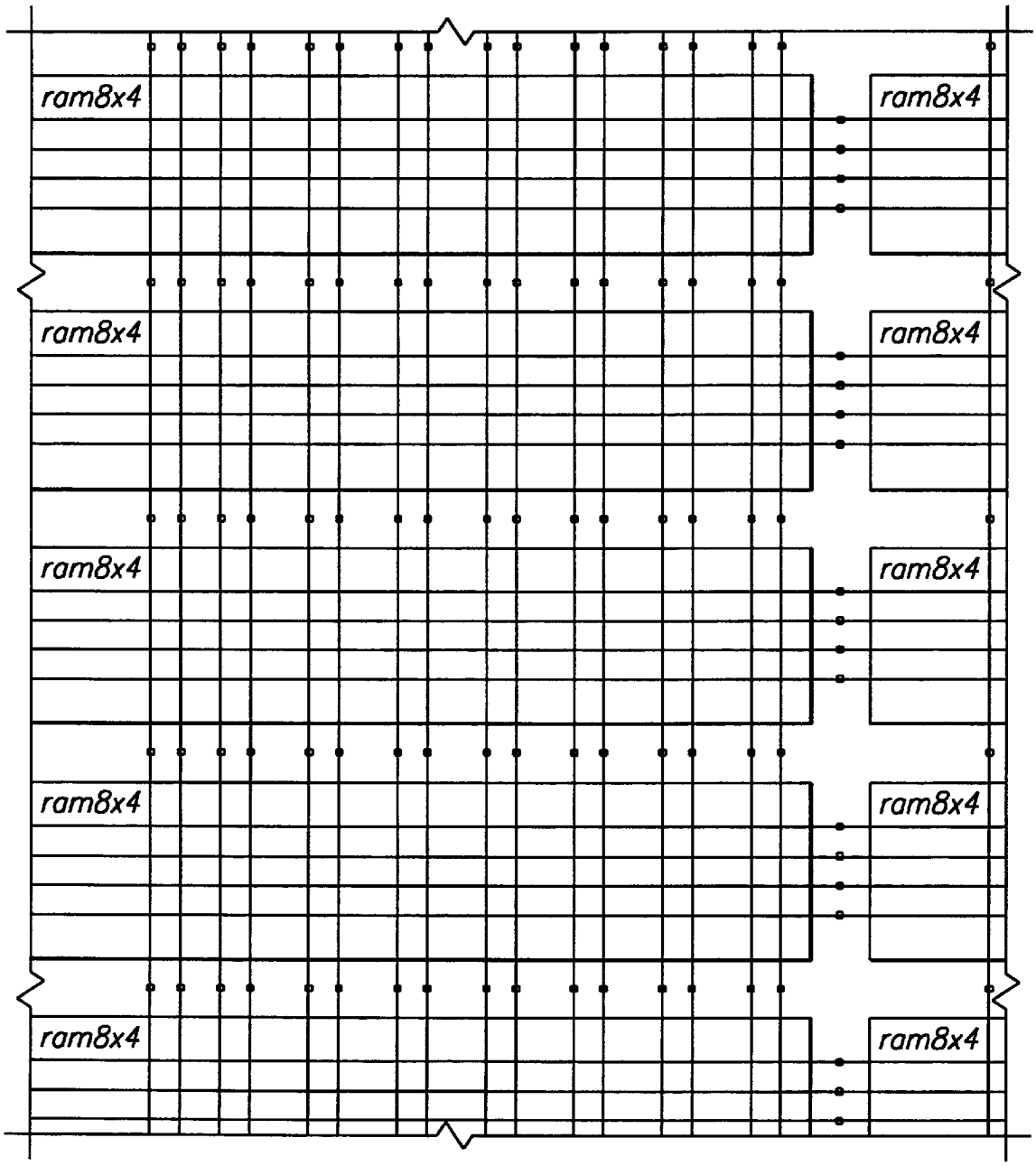
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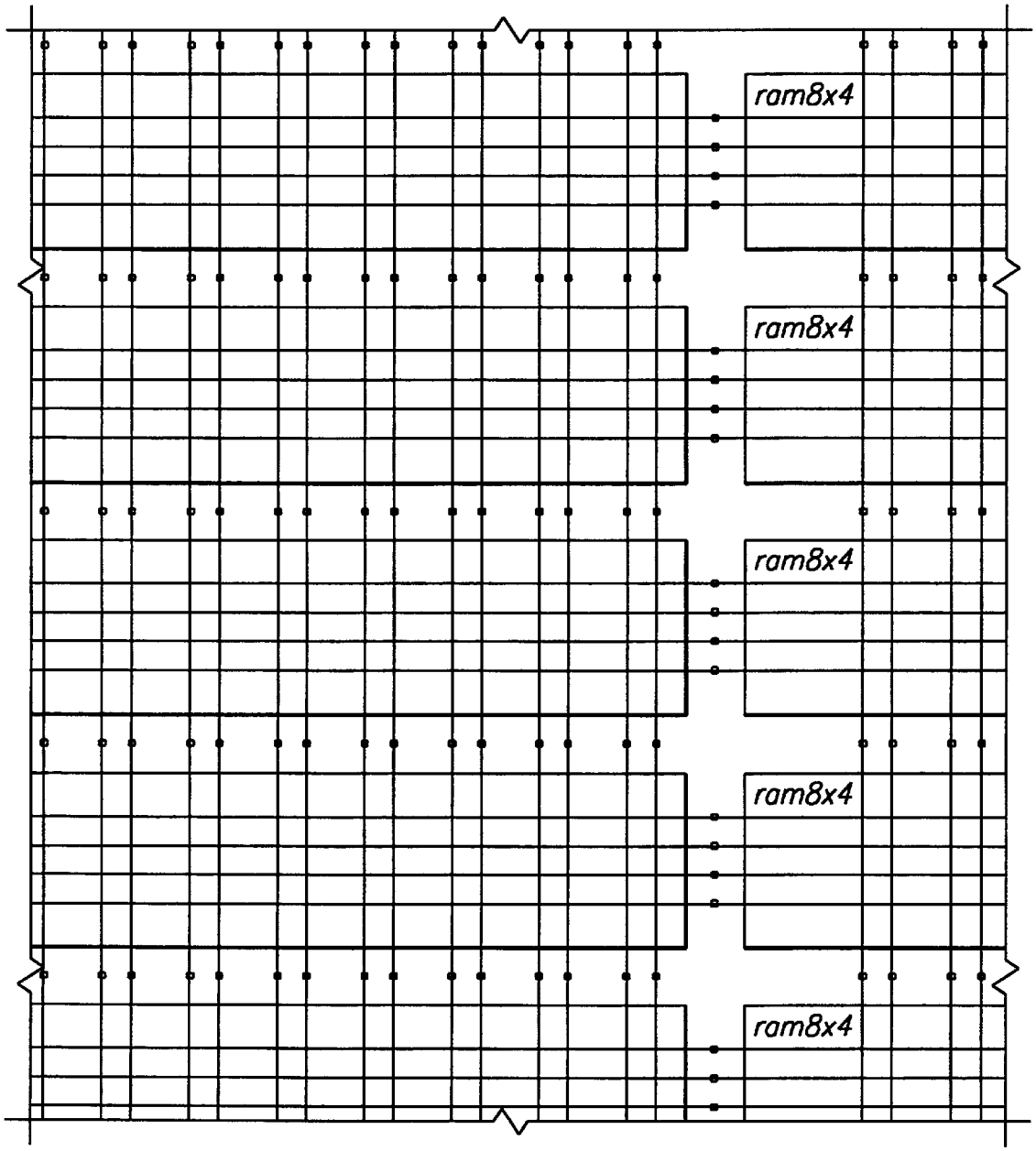
Fig 1.0388



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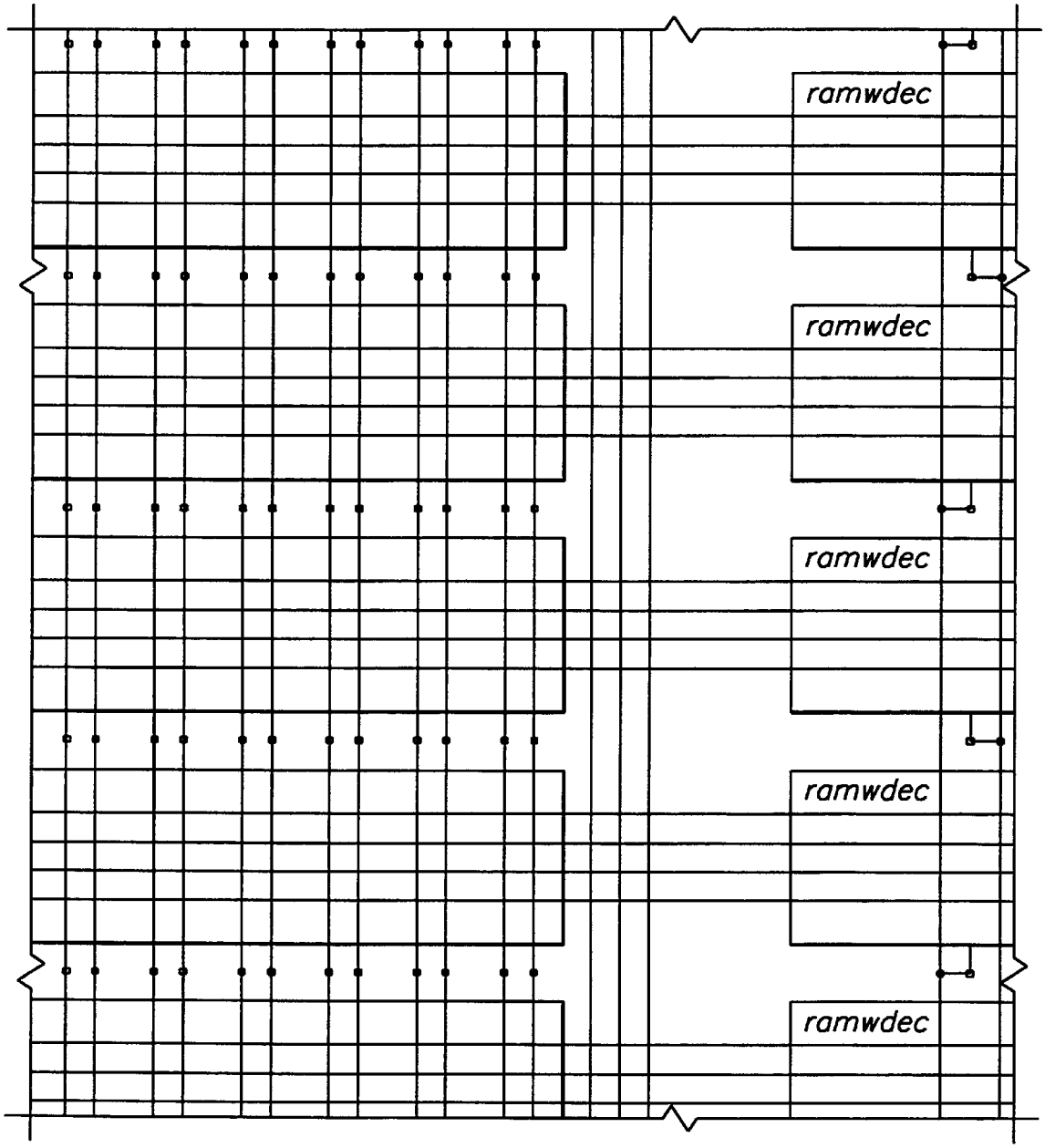

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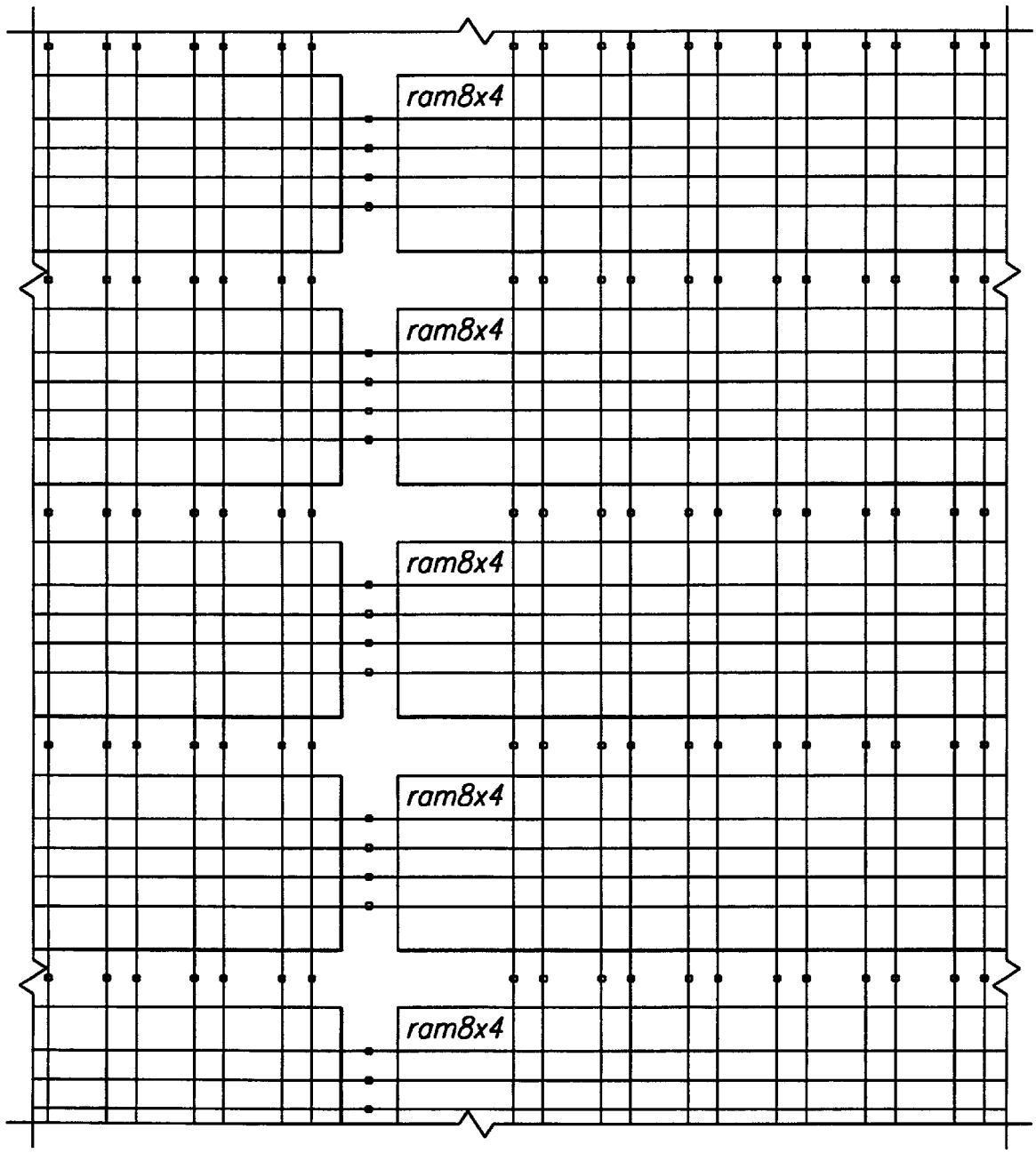

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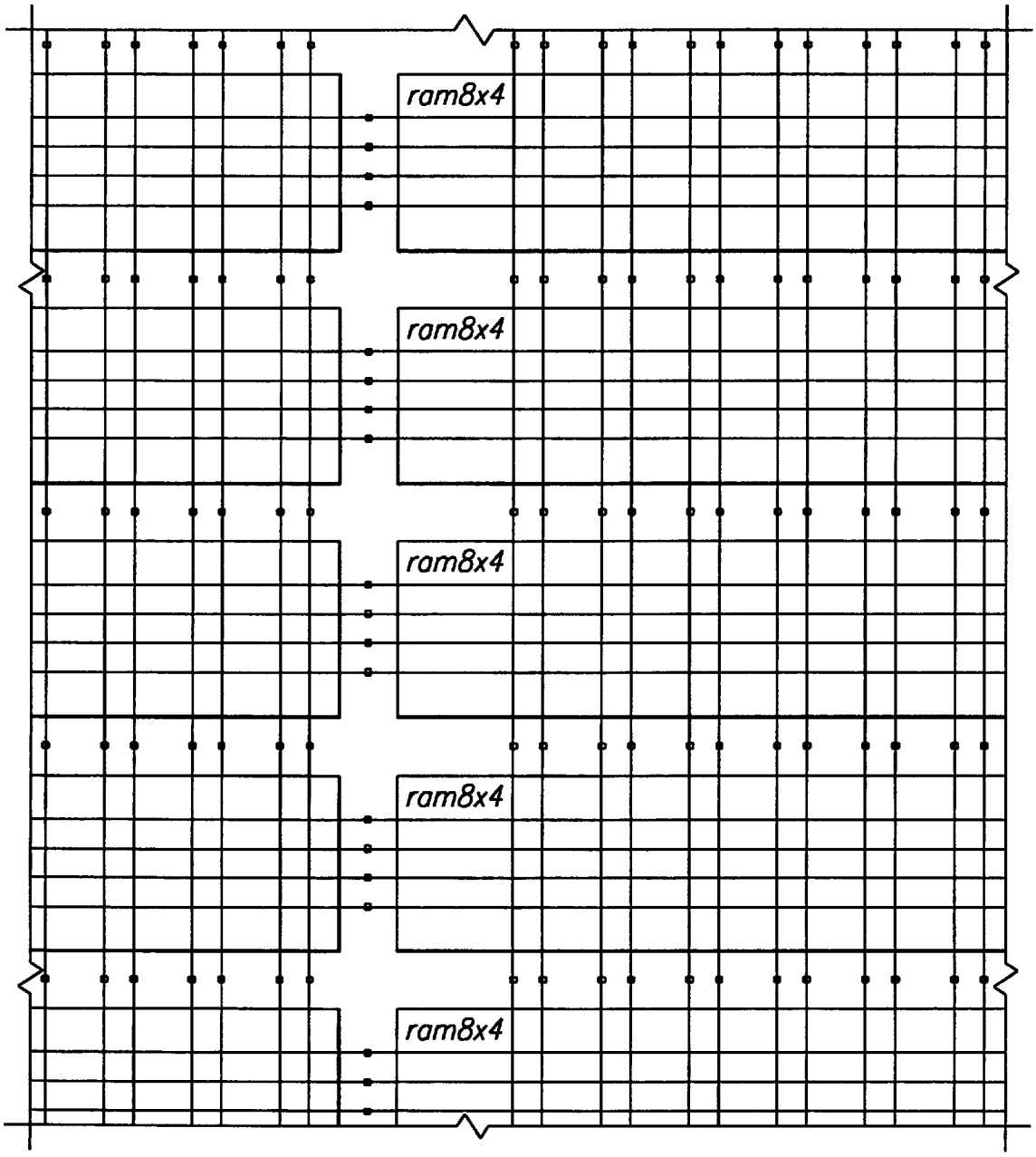

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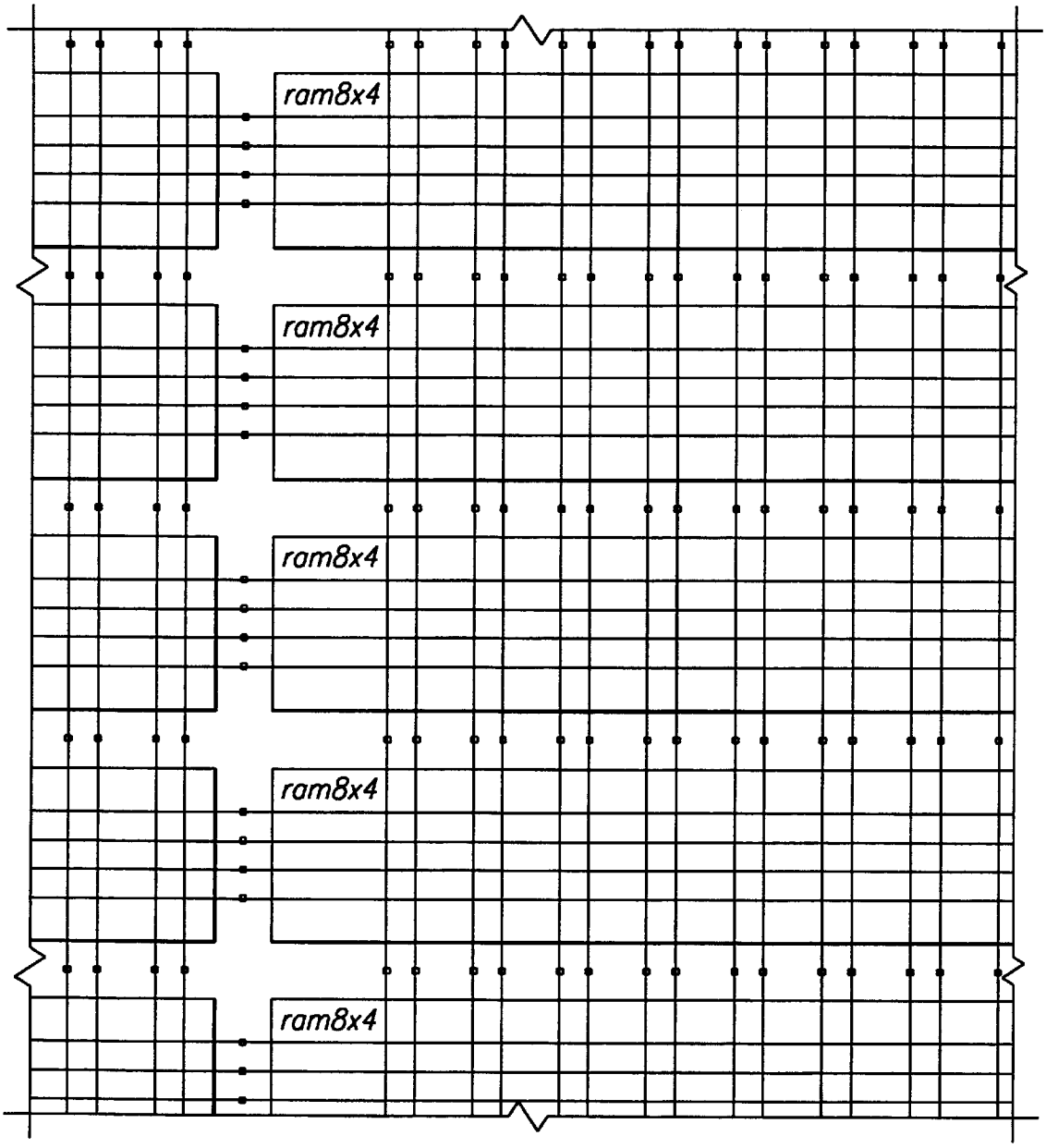
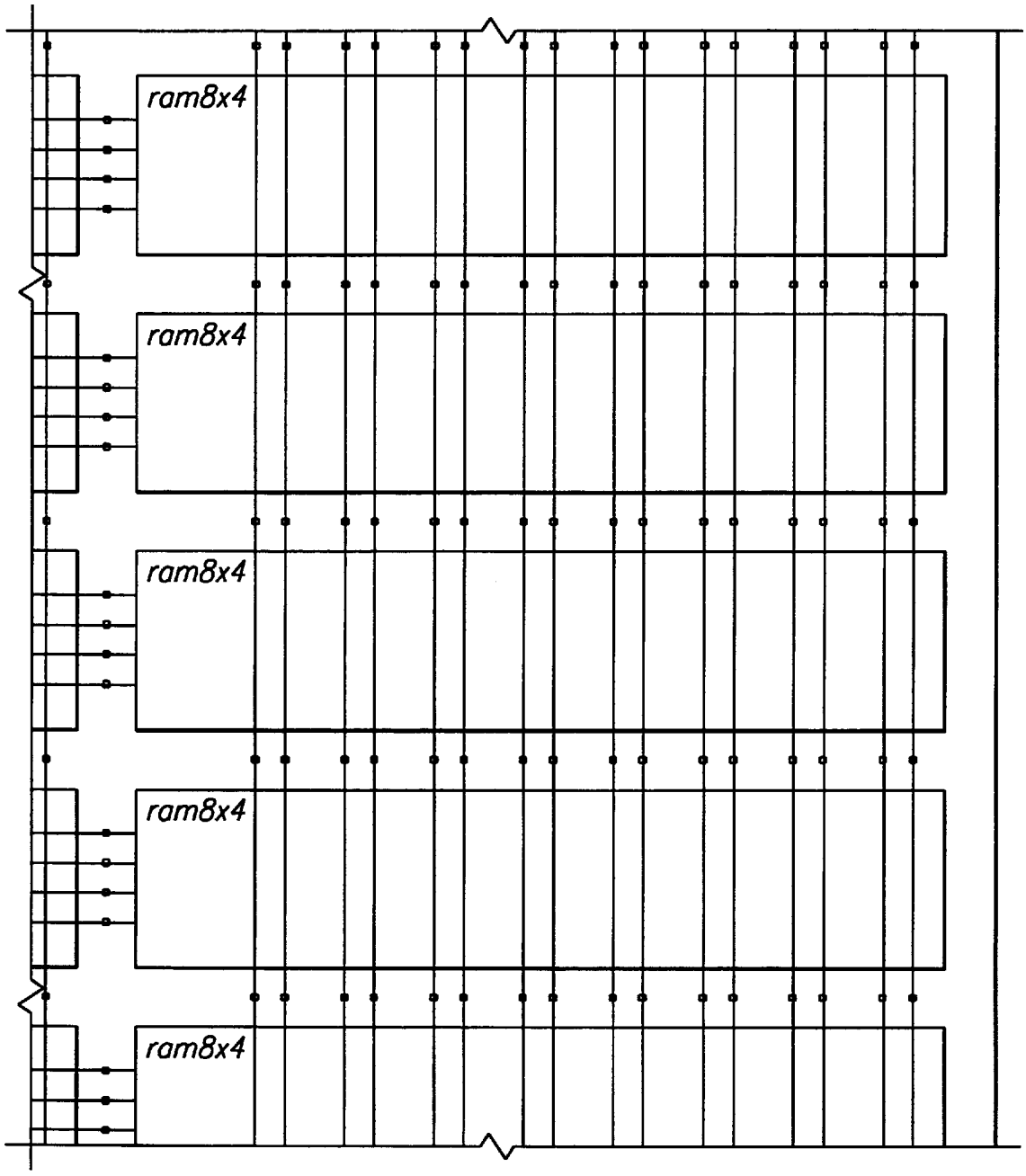


Fig 1.03BG



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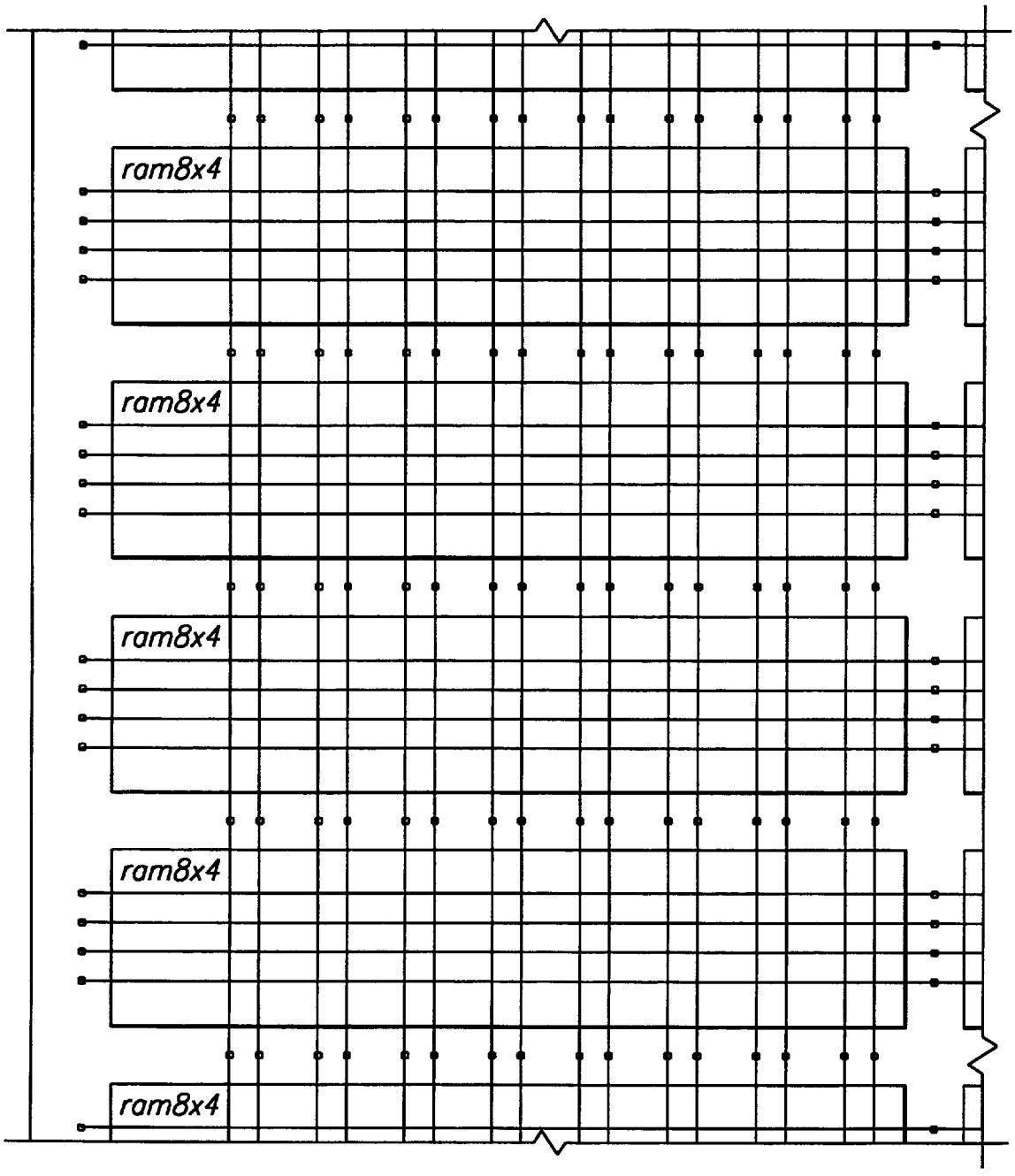

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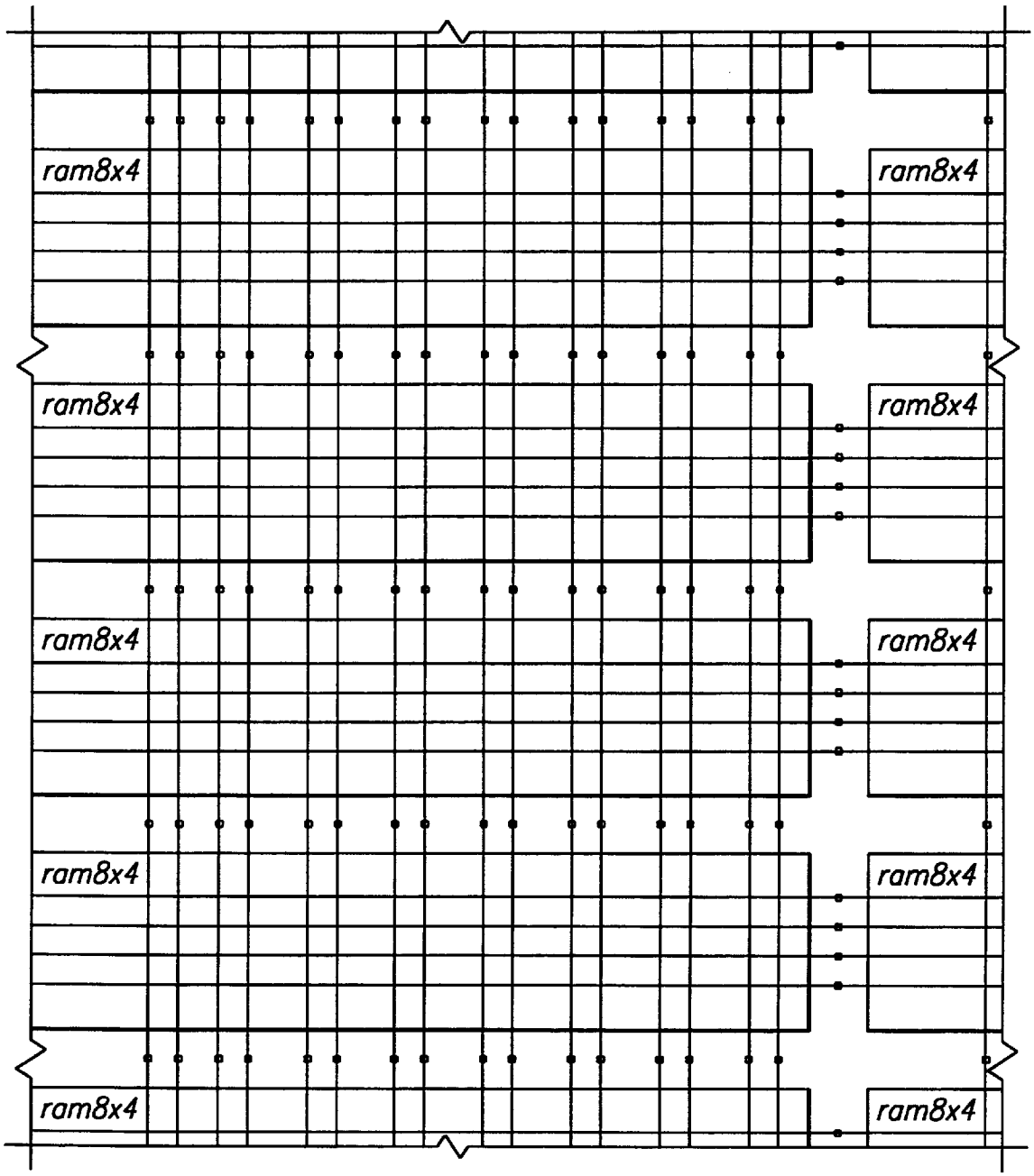
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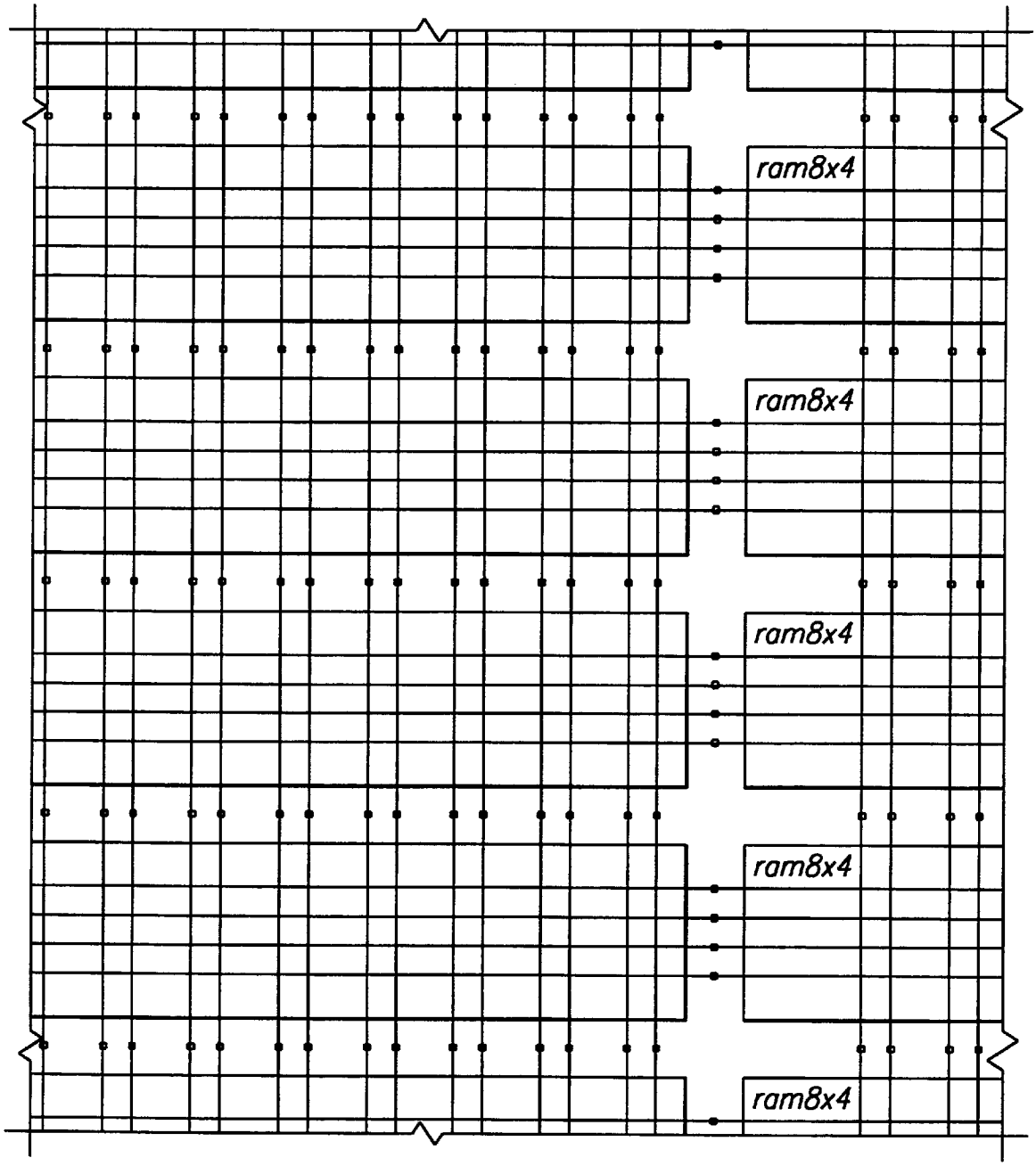
Fig 1.03CB



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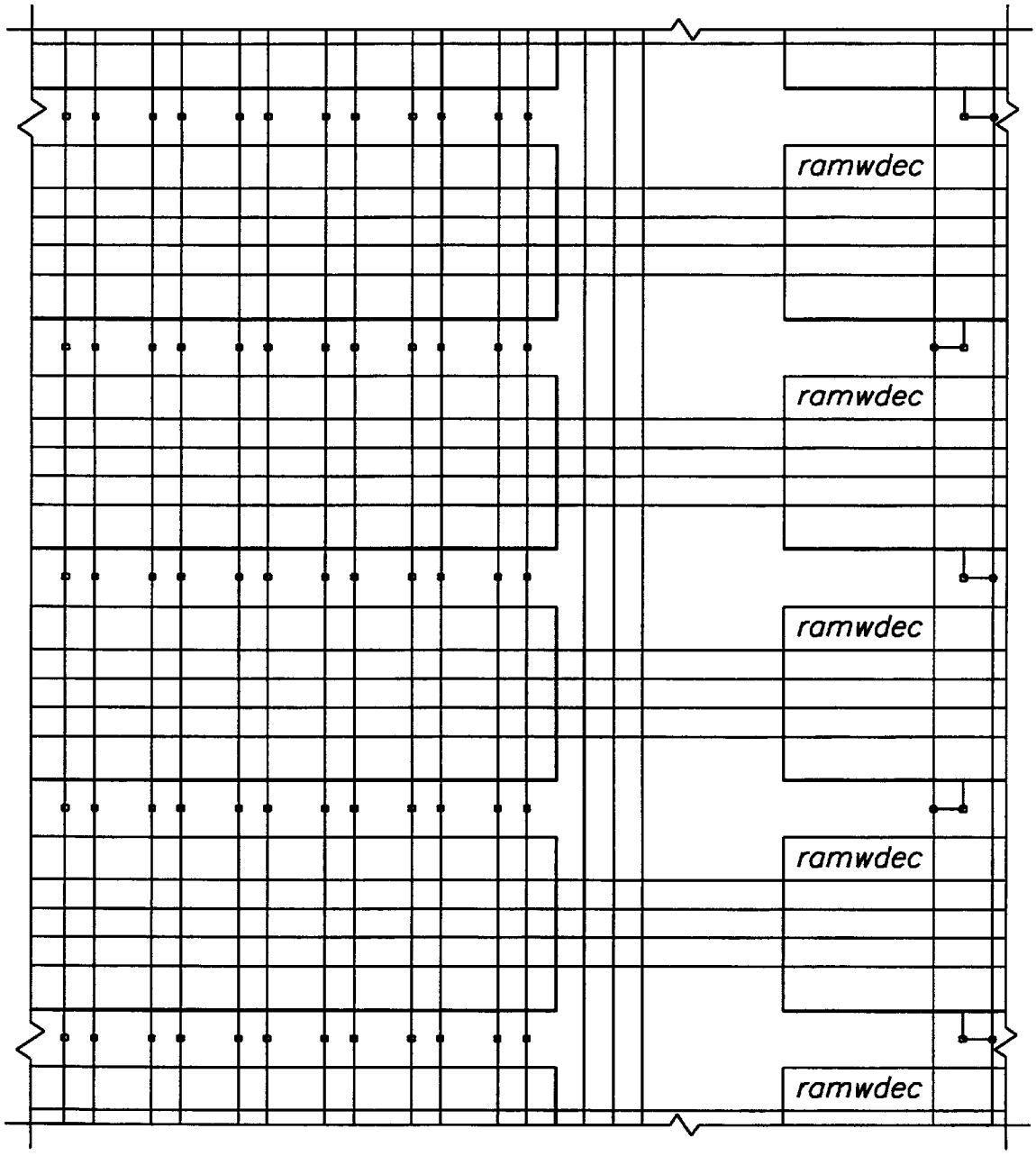

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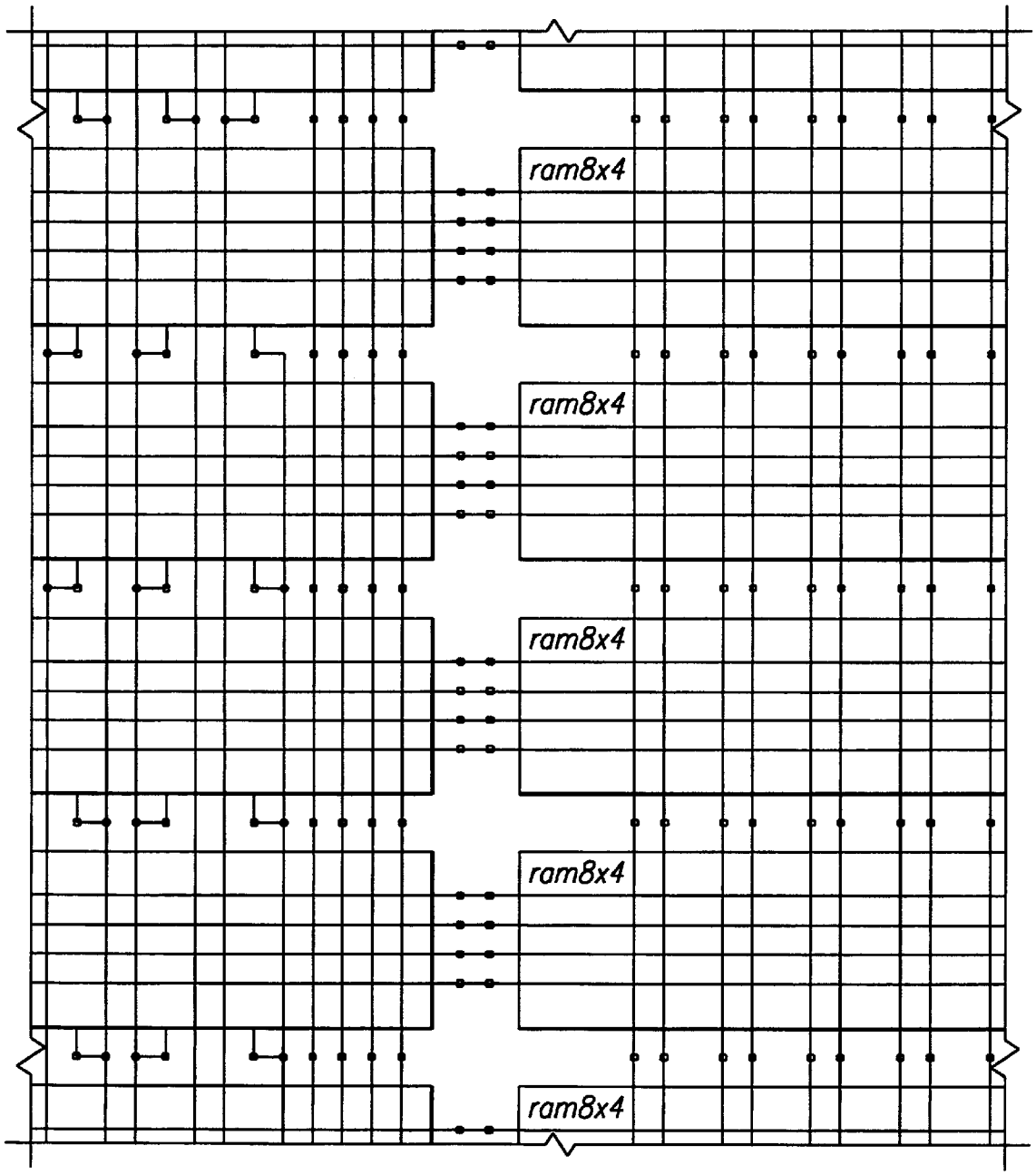

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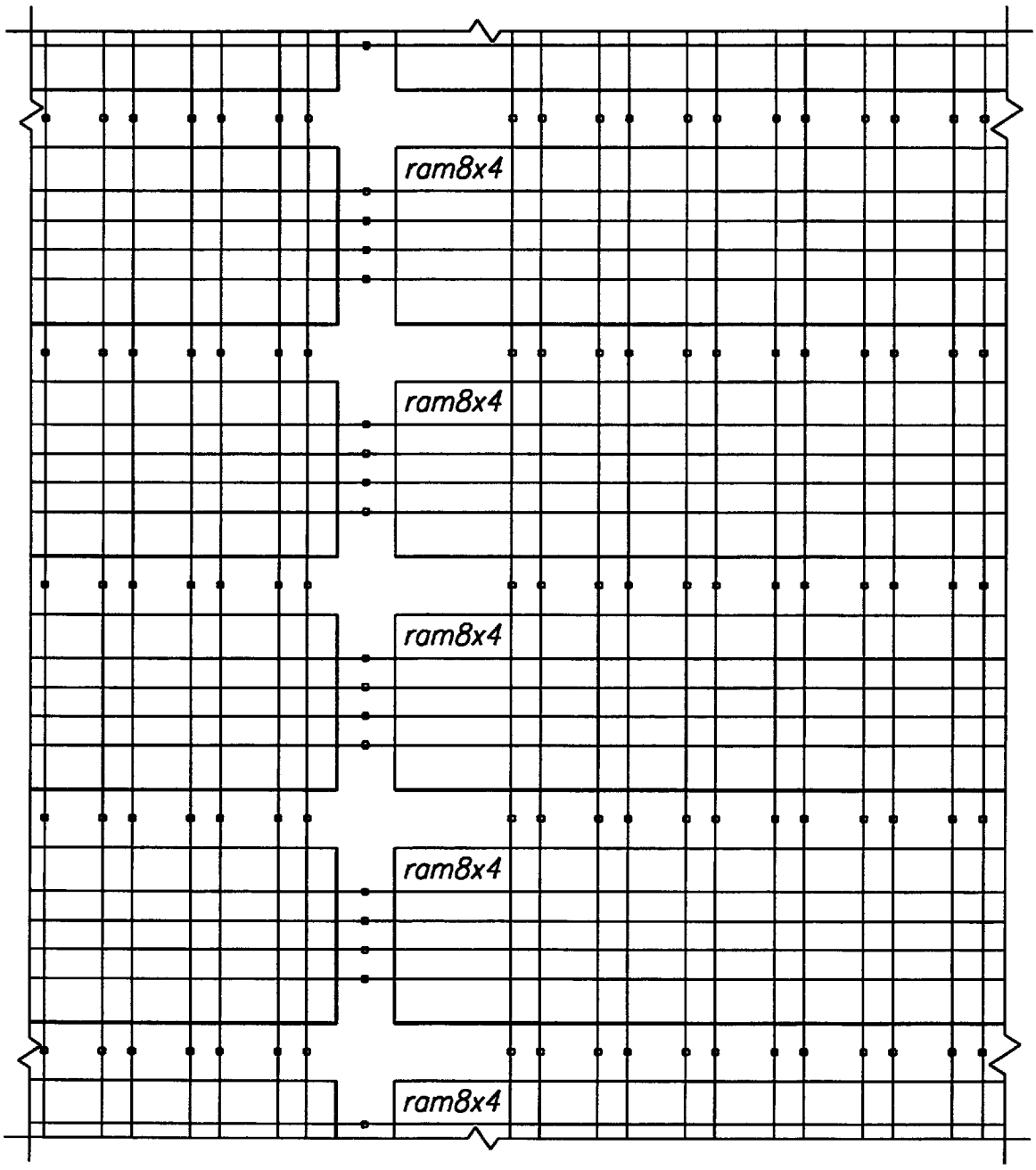

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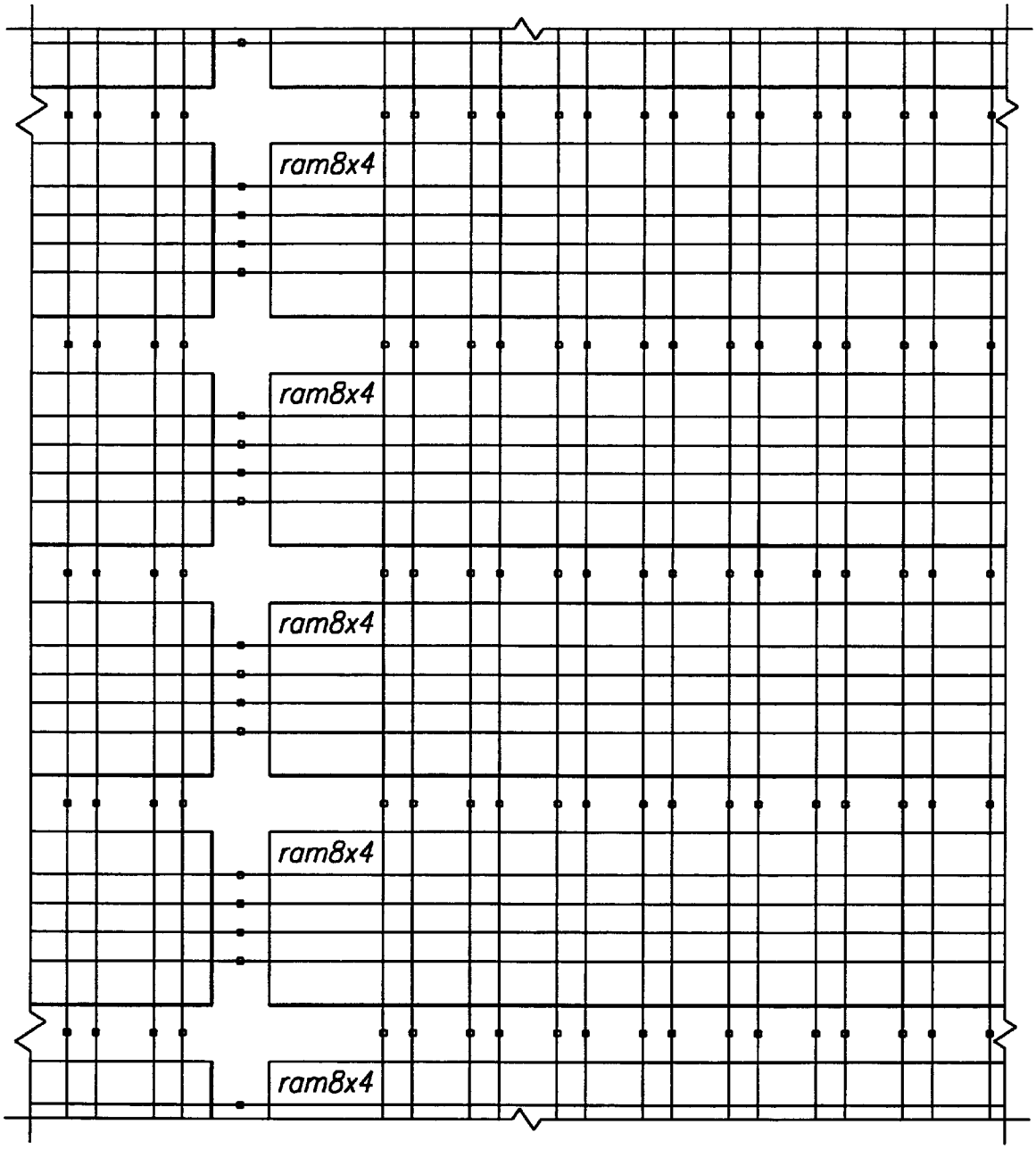

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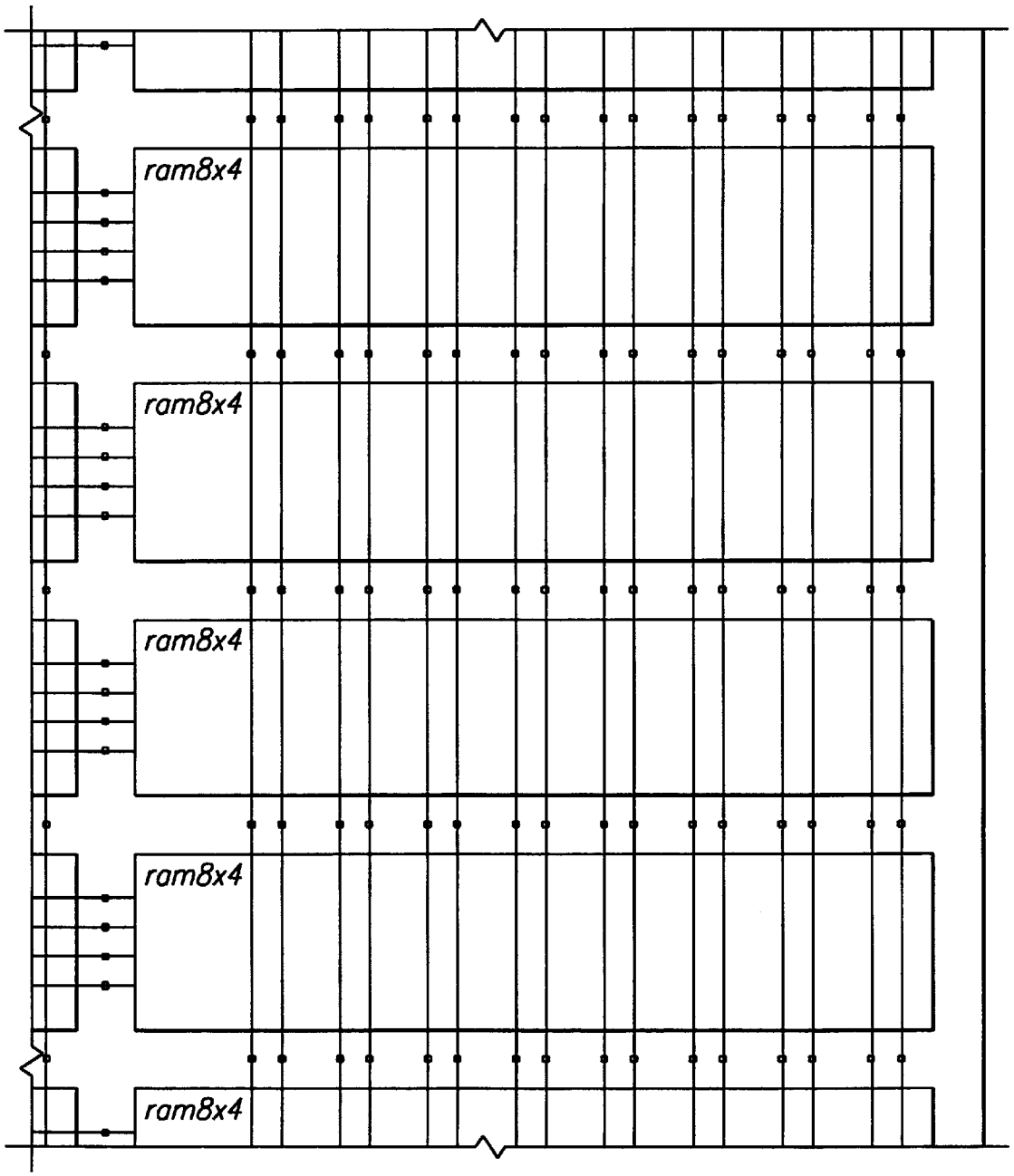

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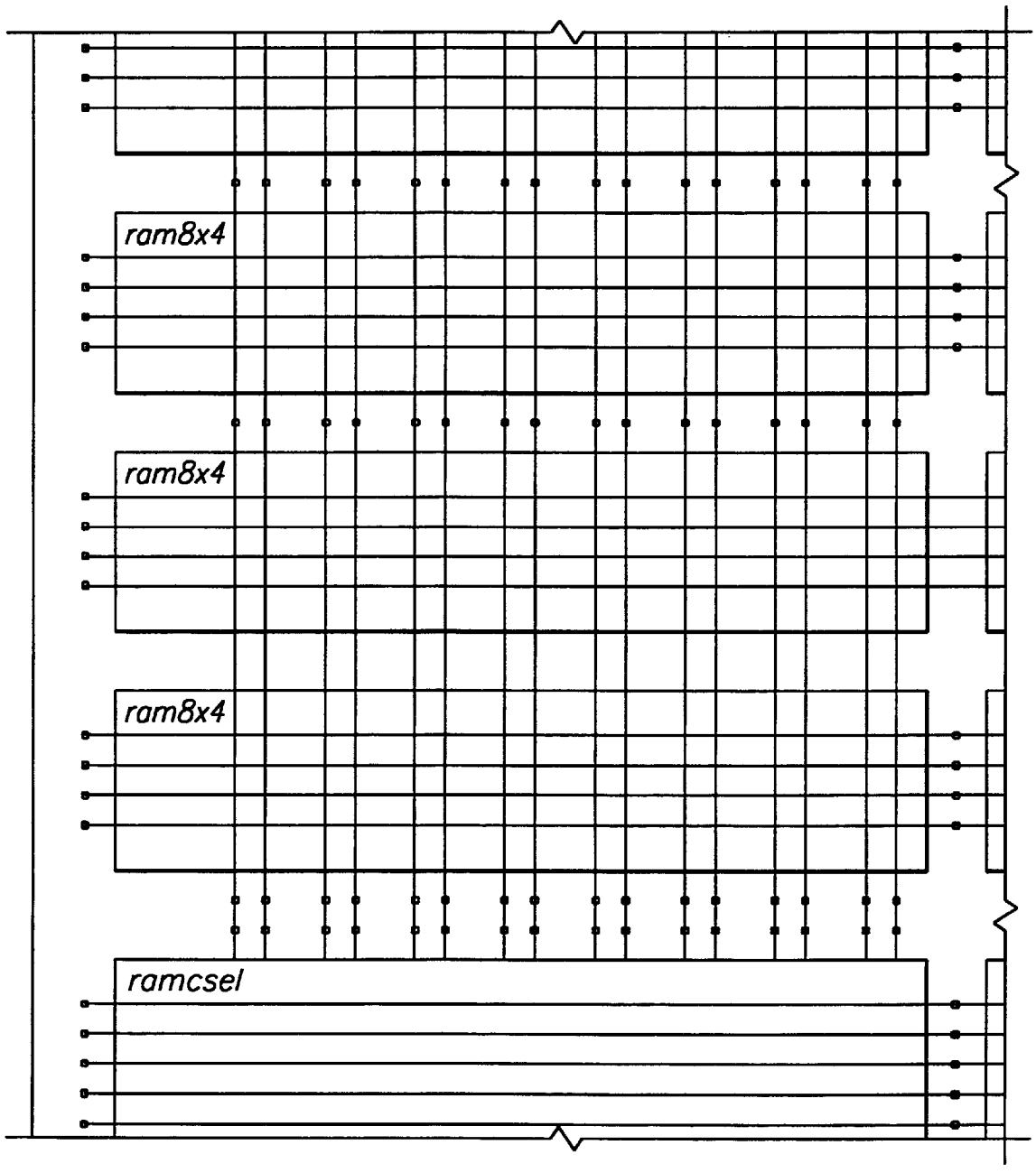

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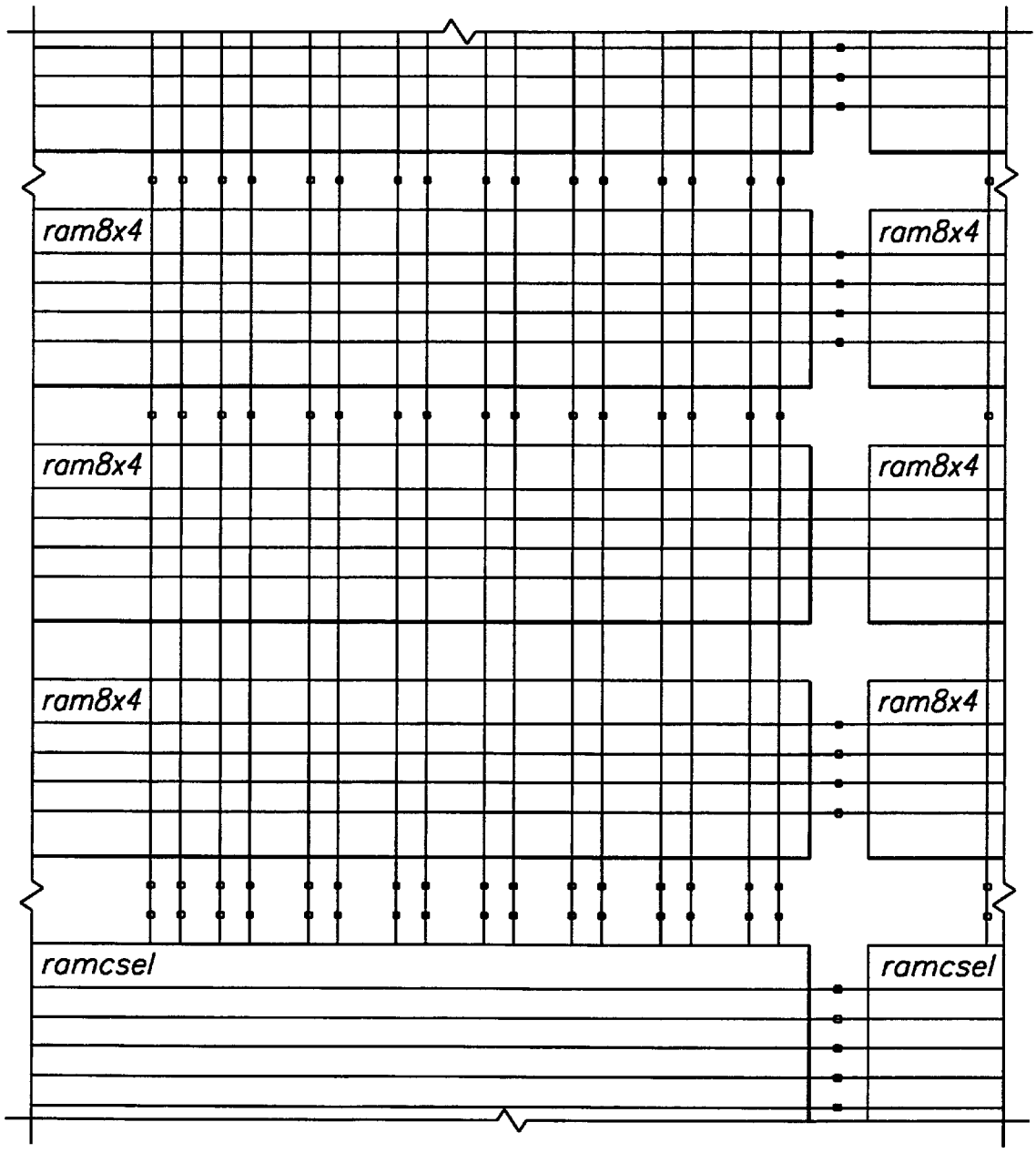
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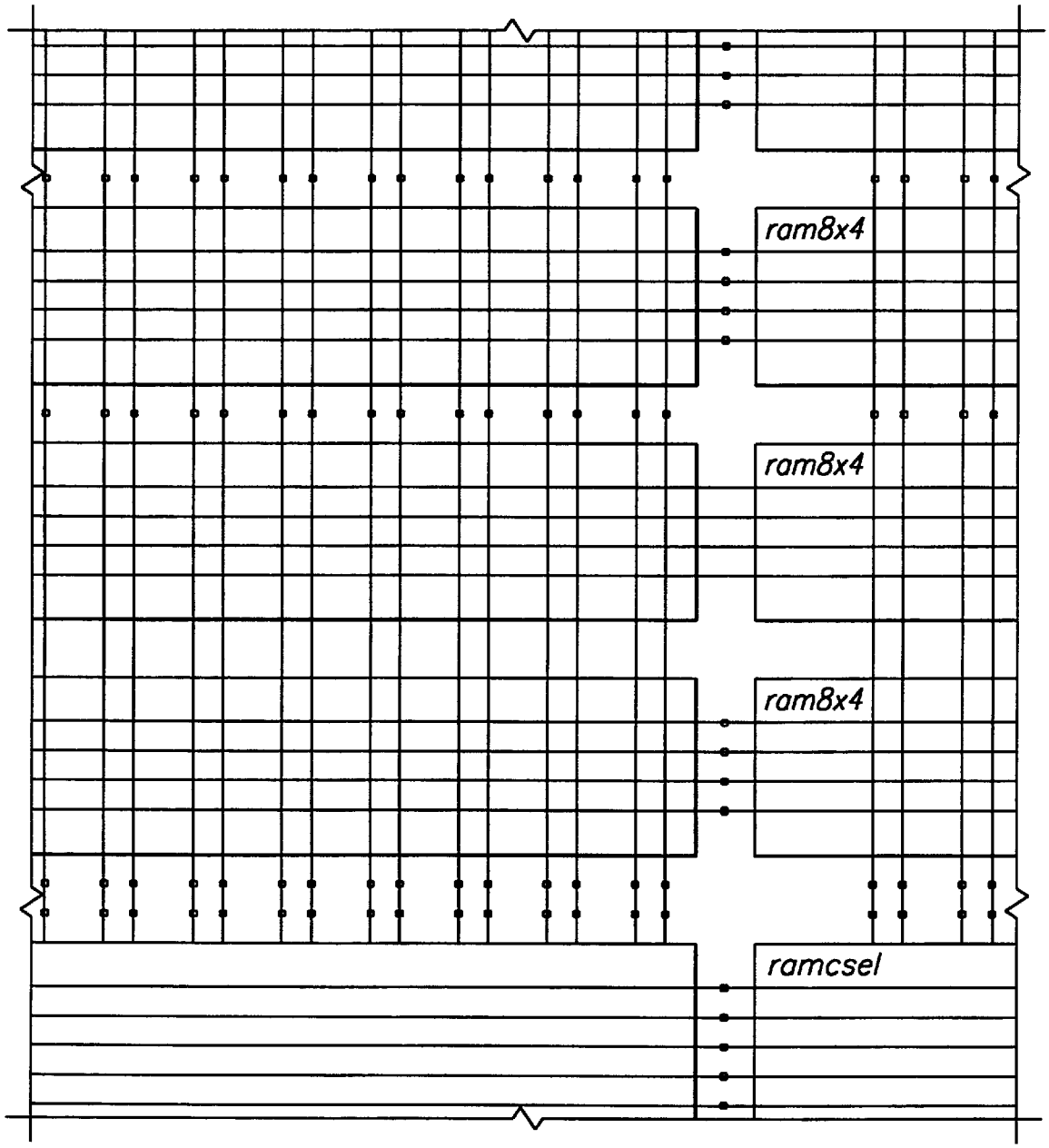
Fig 7.0300B



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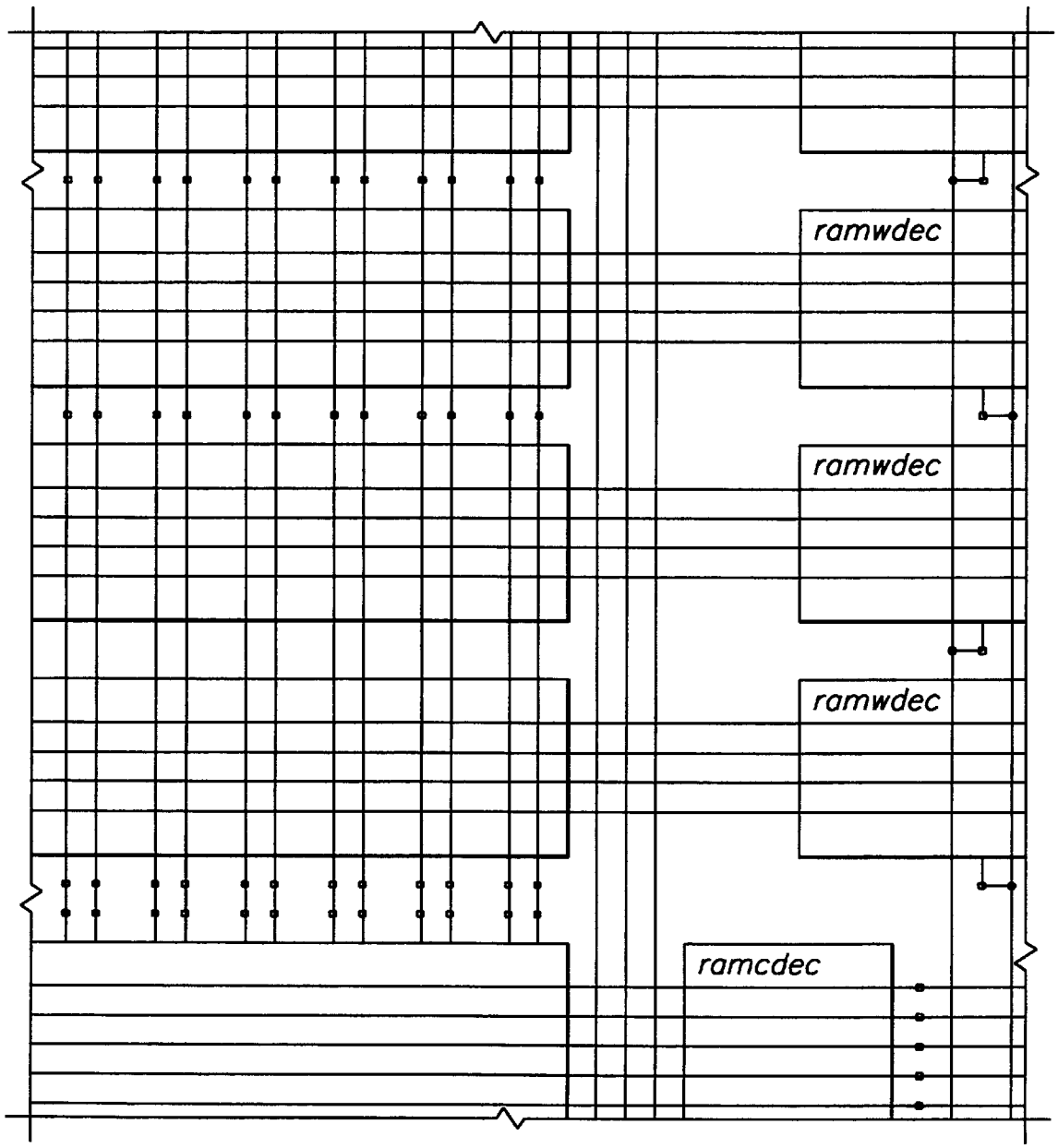

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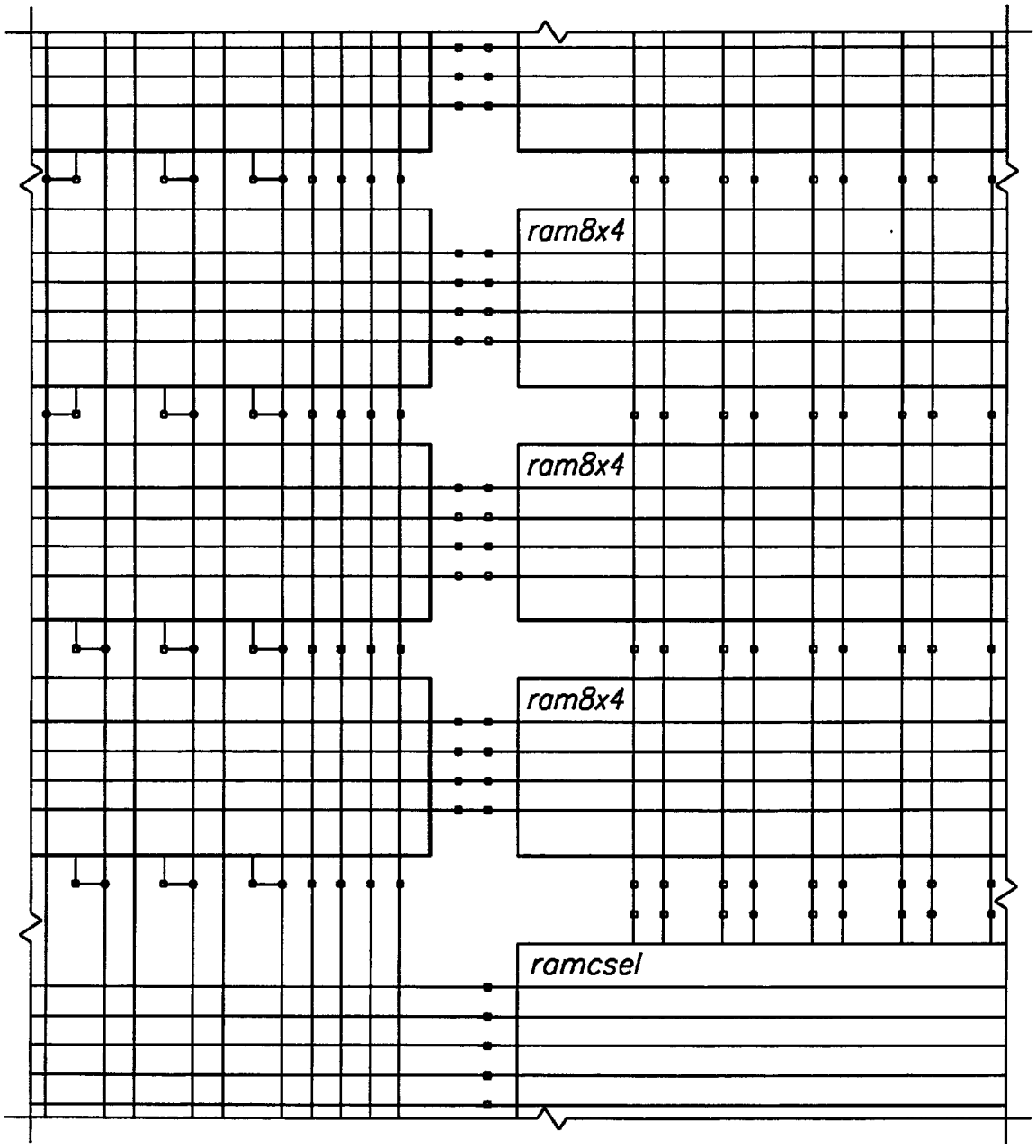

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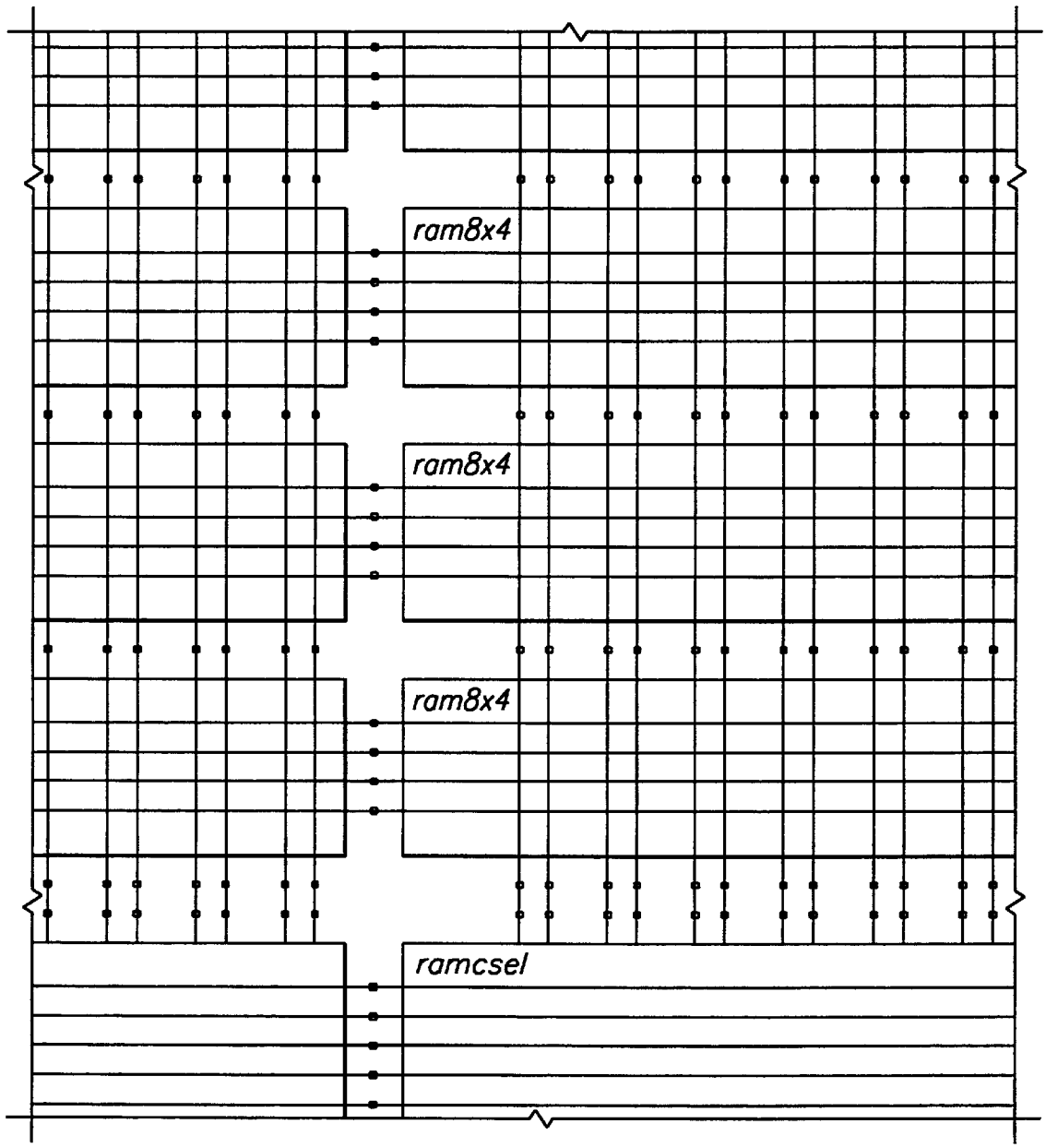

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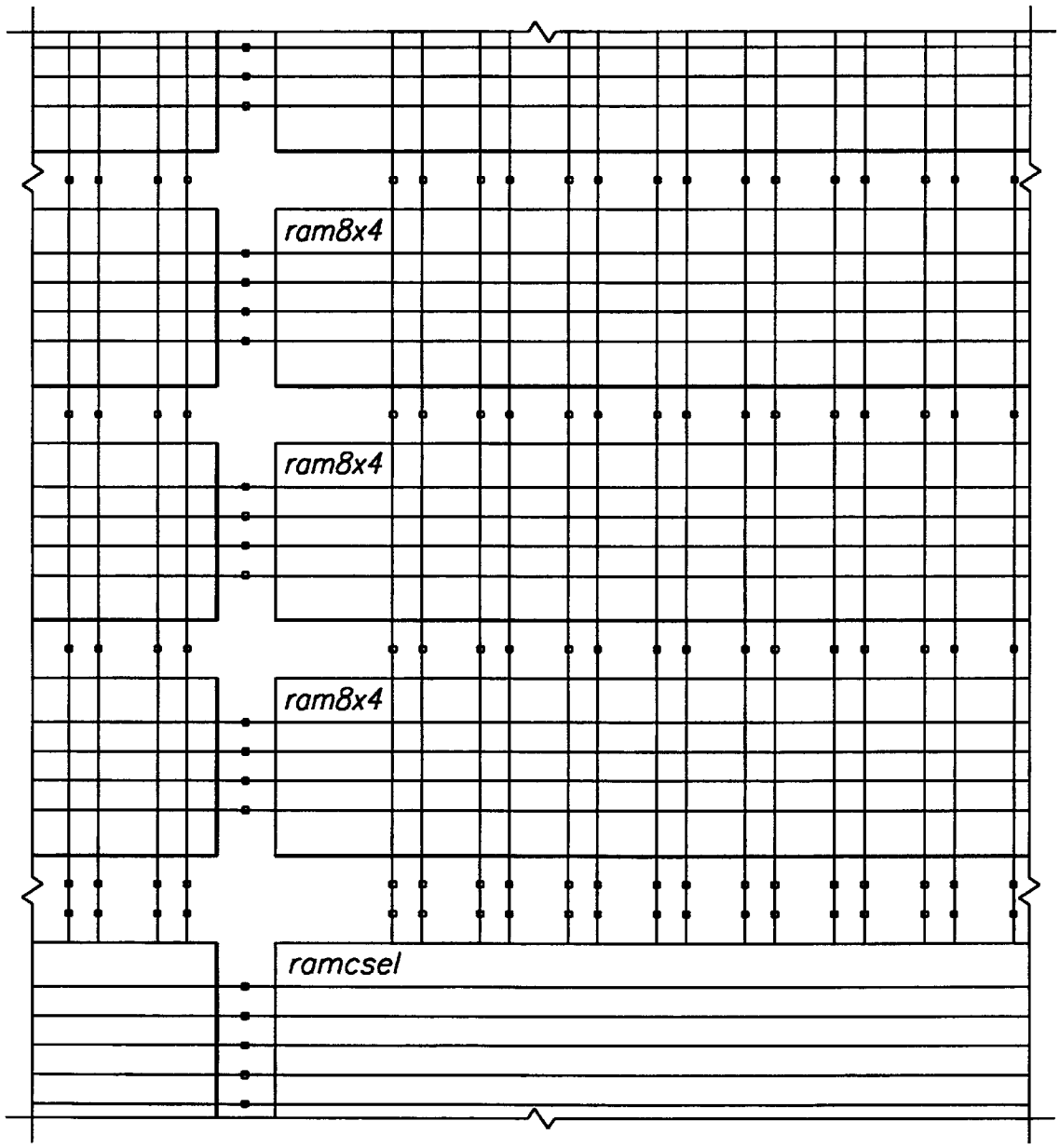

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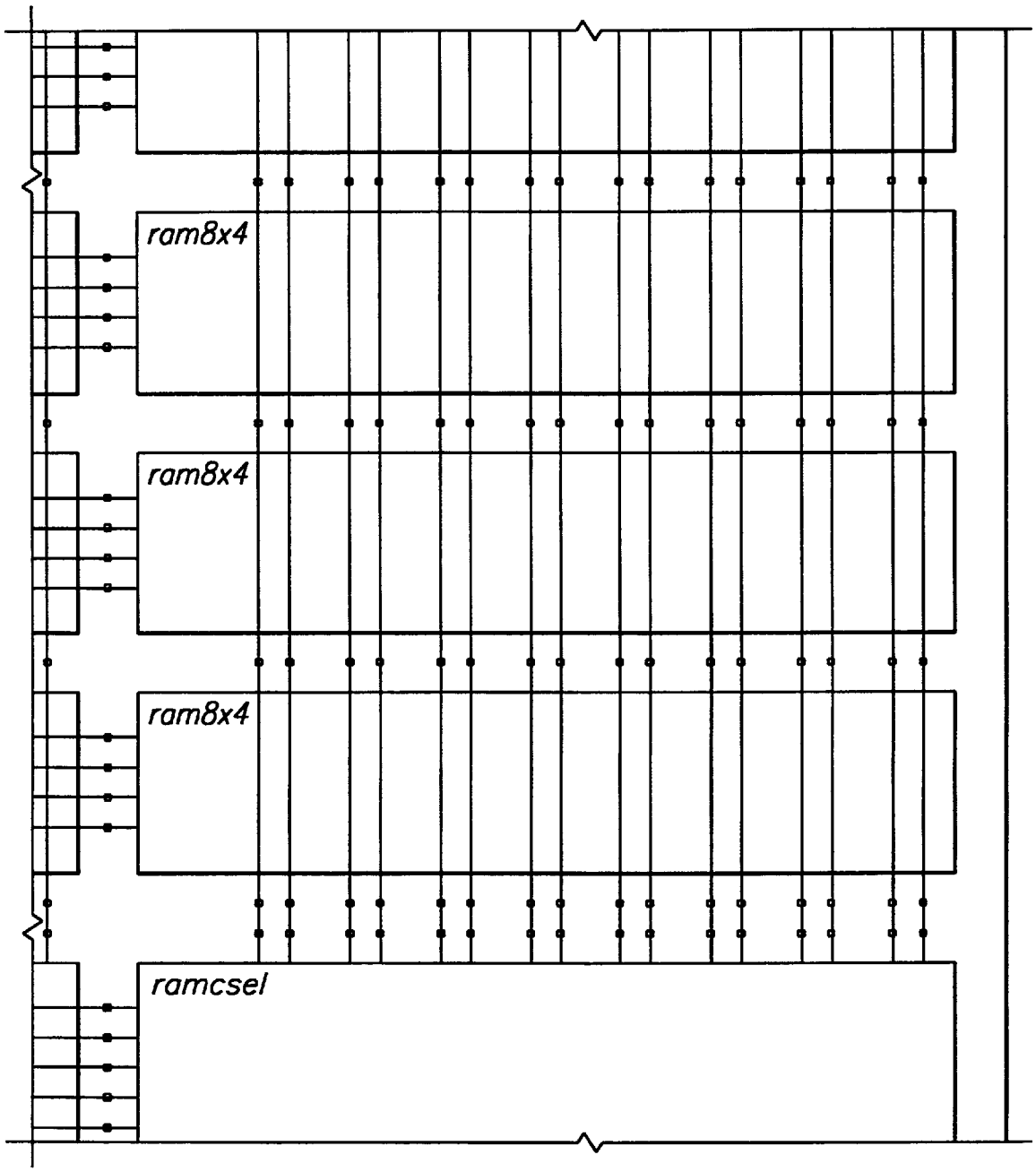

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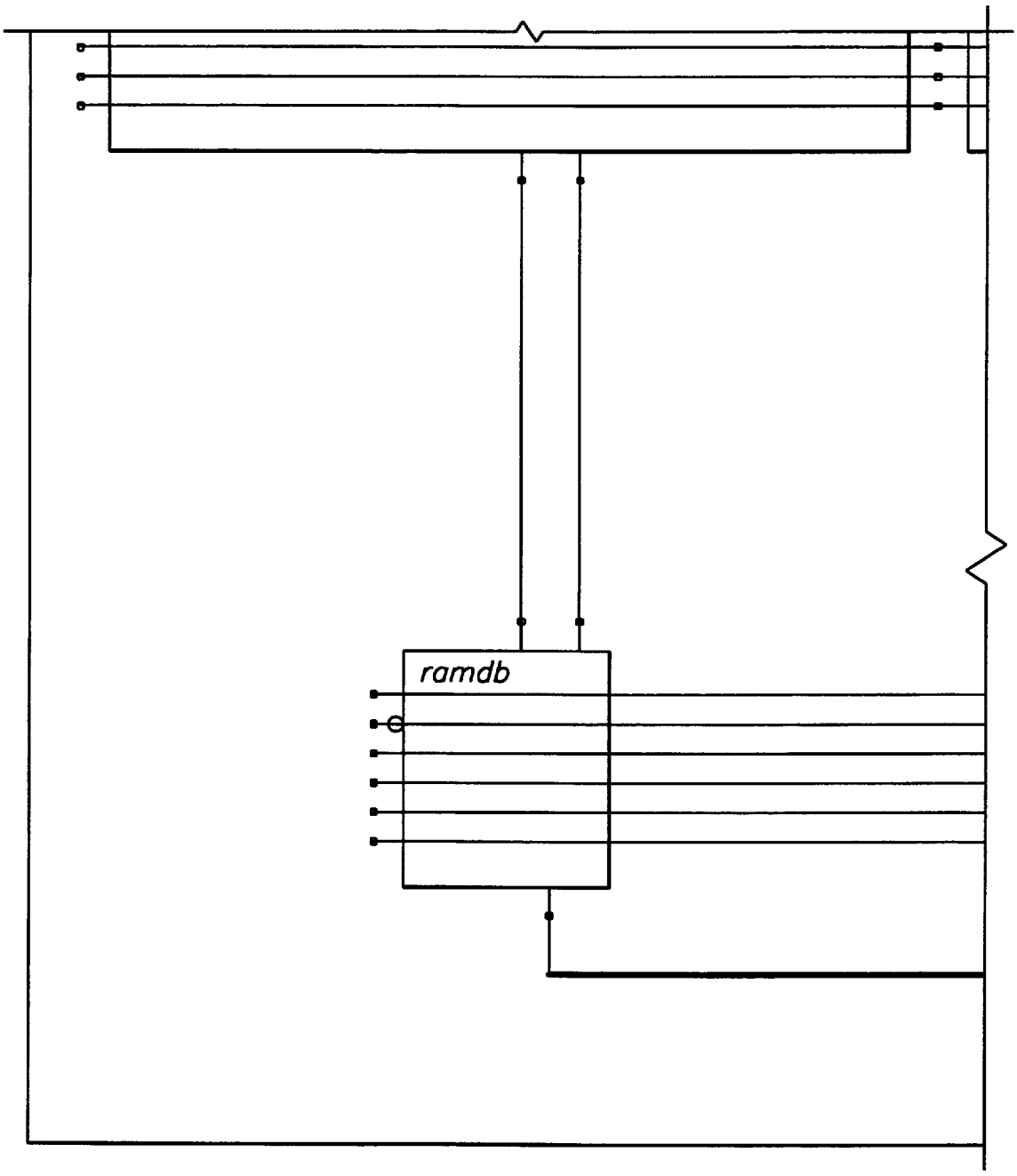
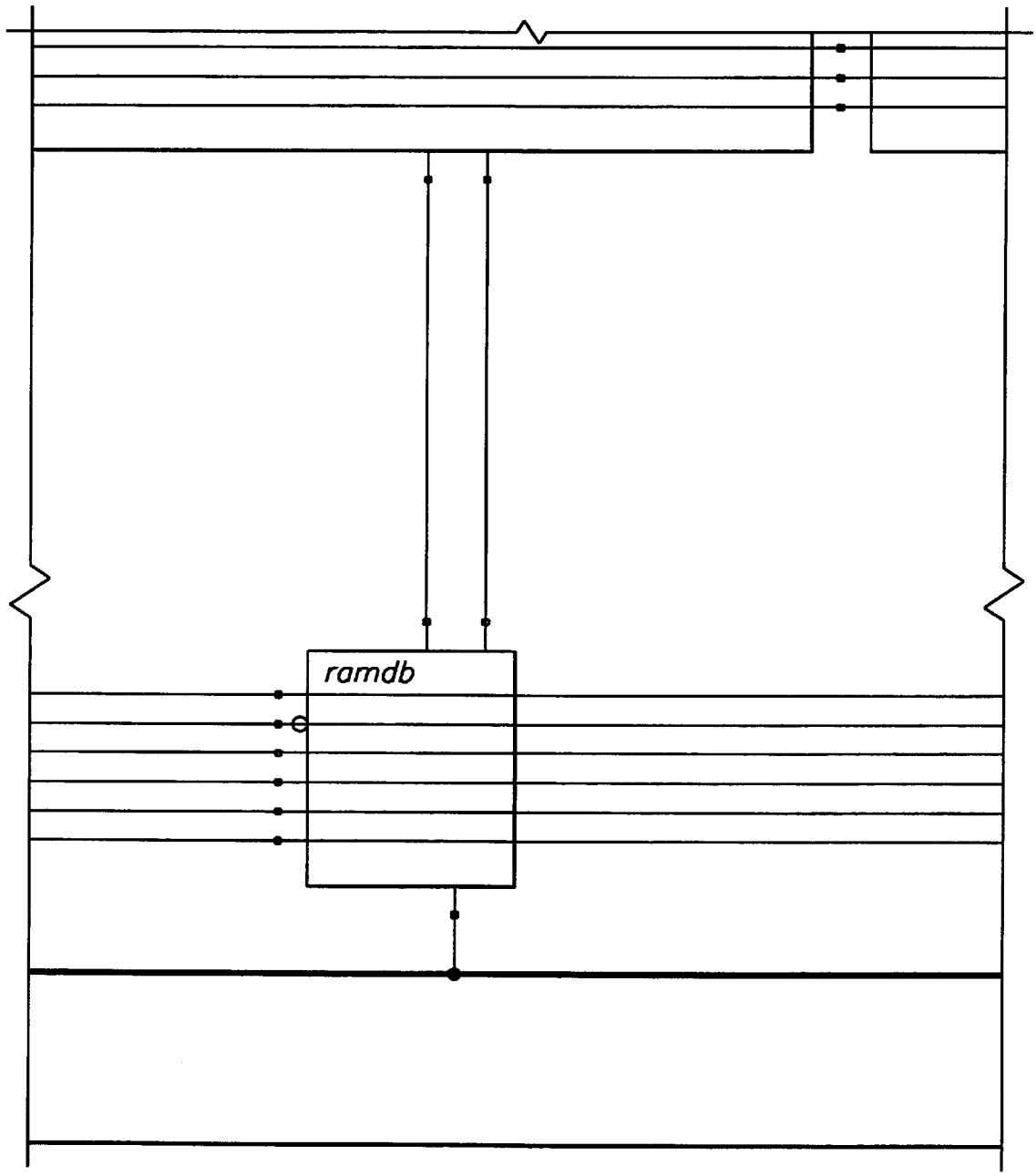


Fig 1.03EA



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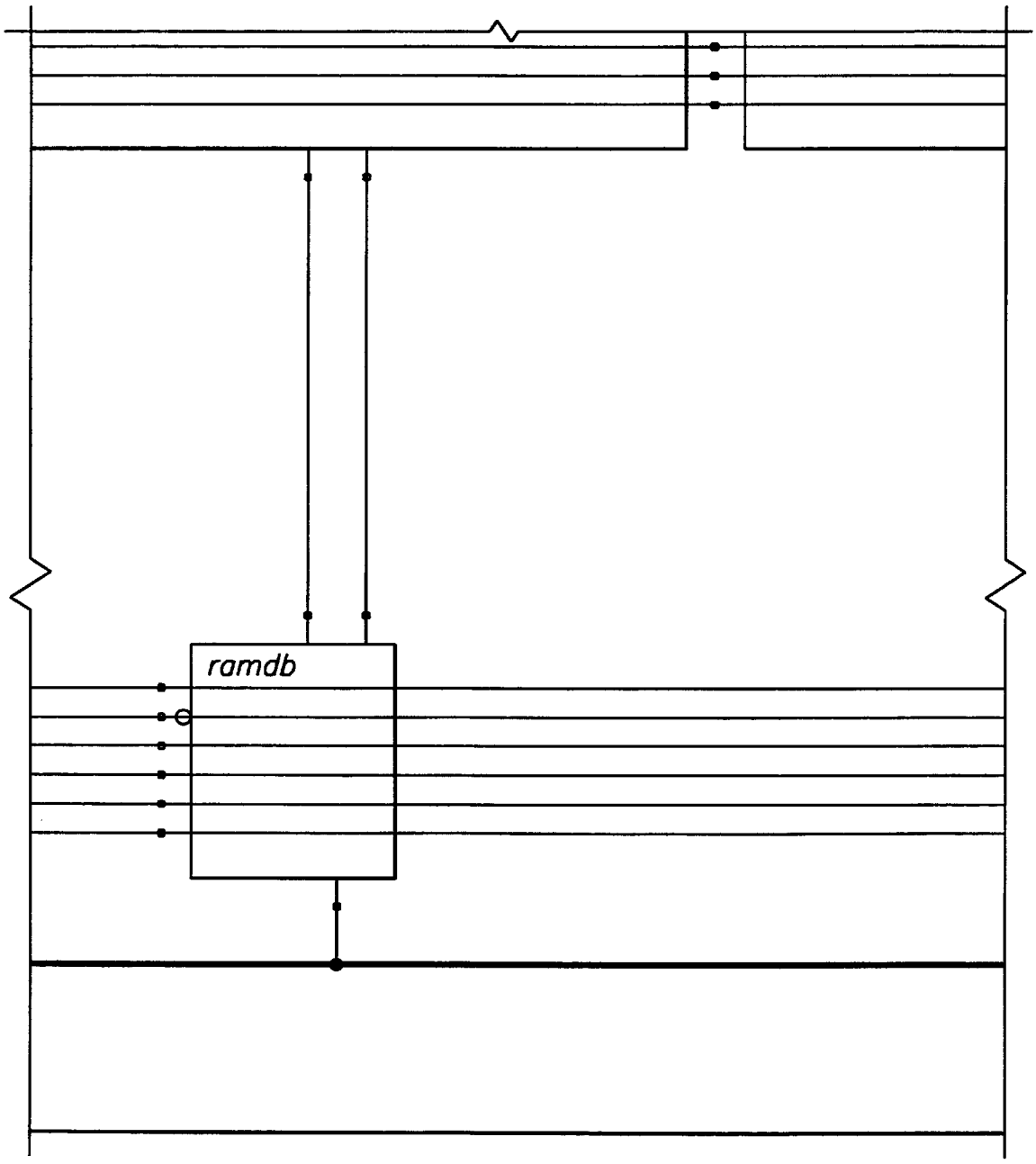

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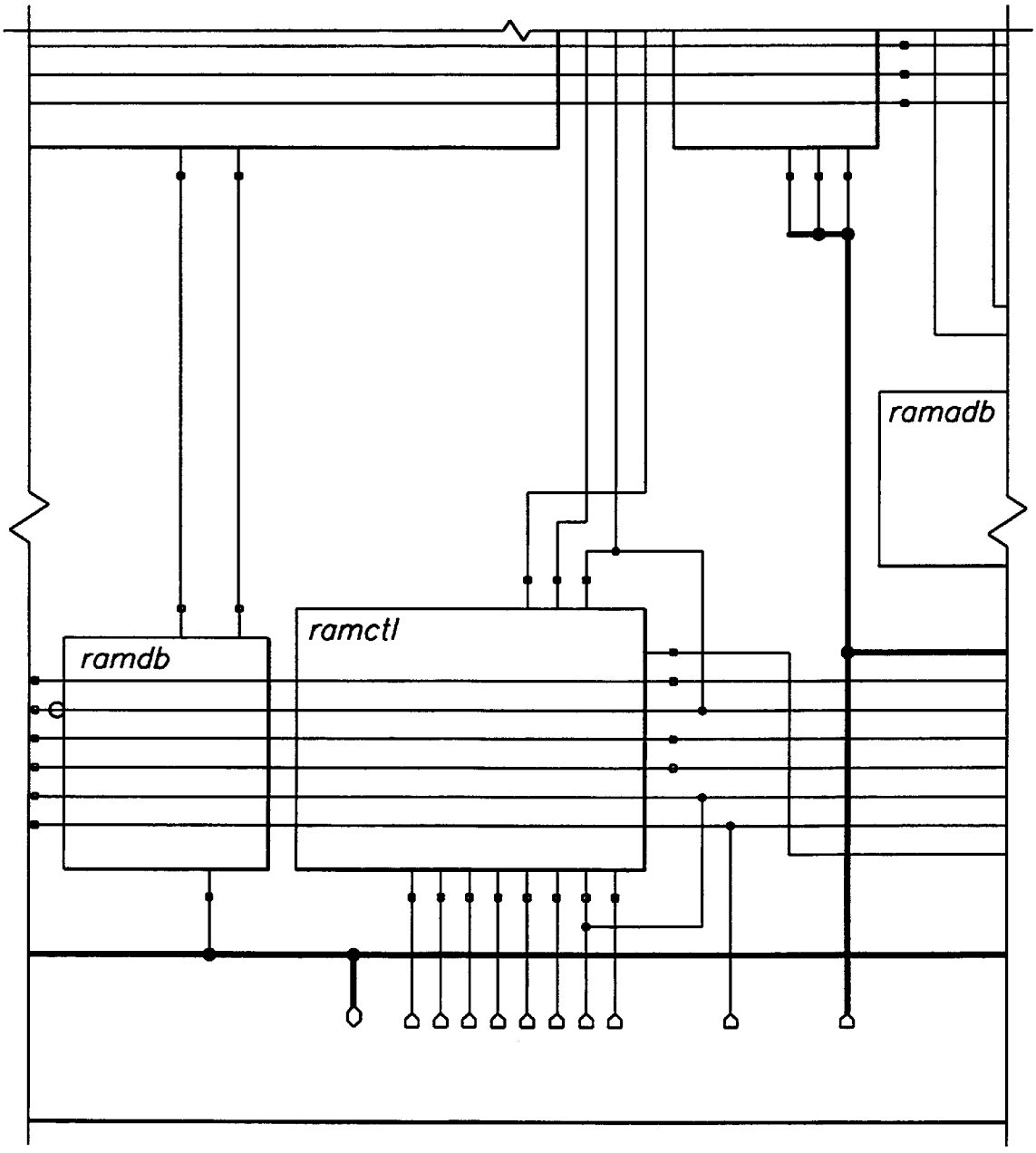

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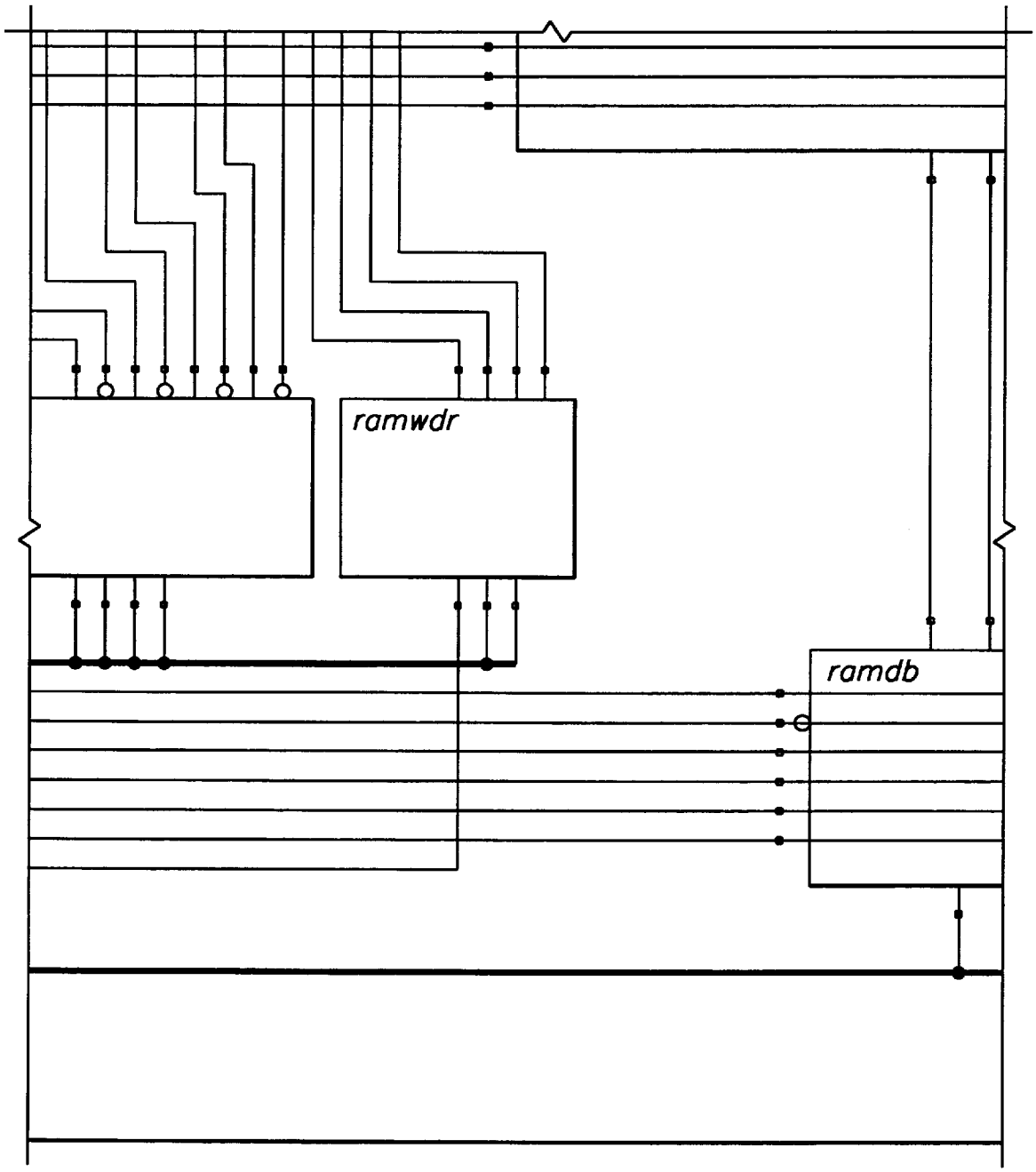

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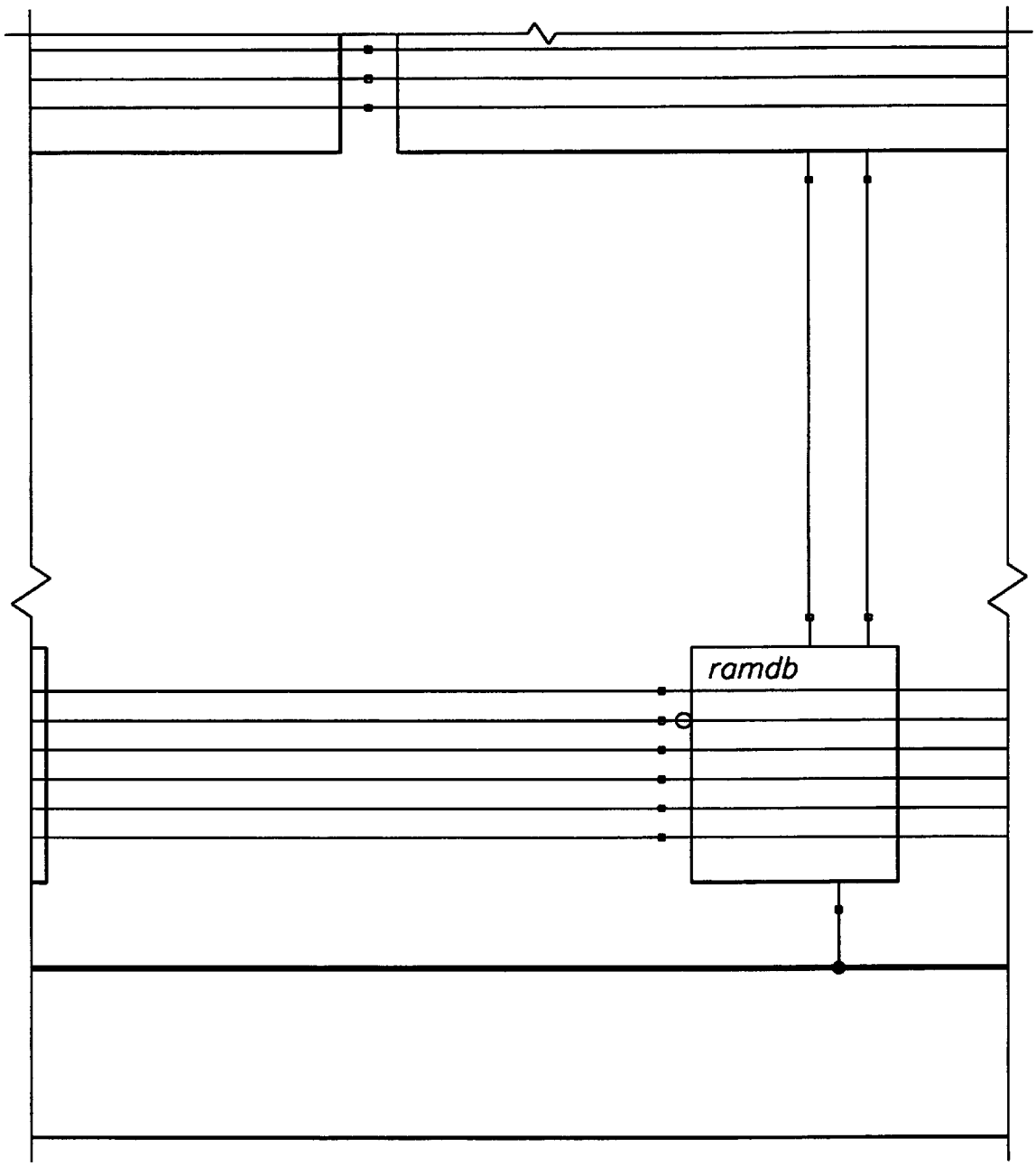

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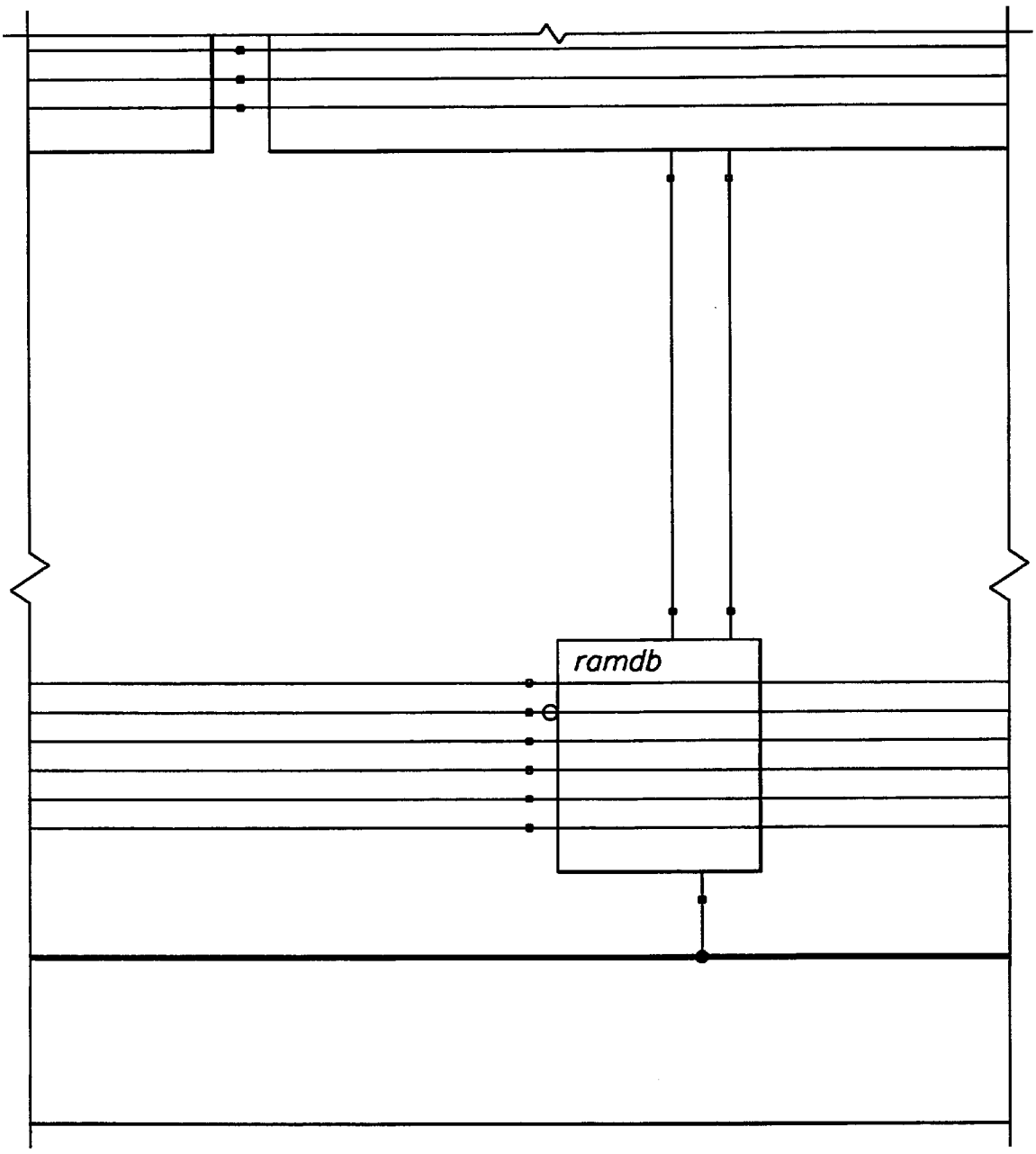


Fig 7.03E6

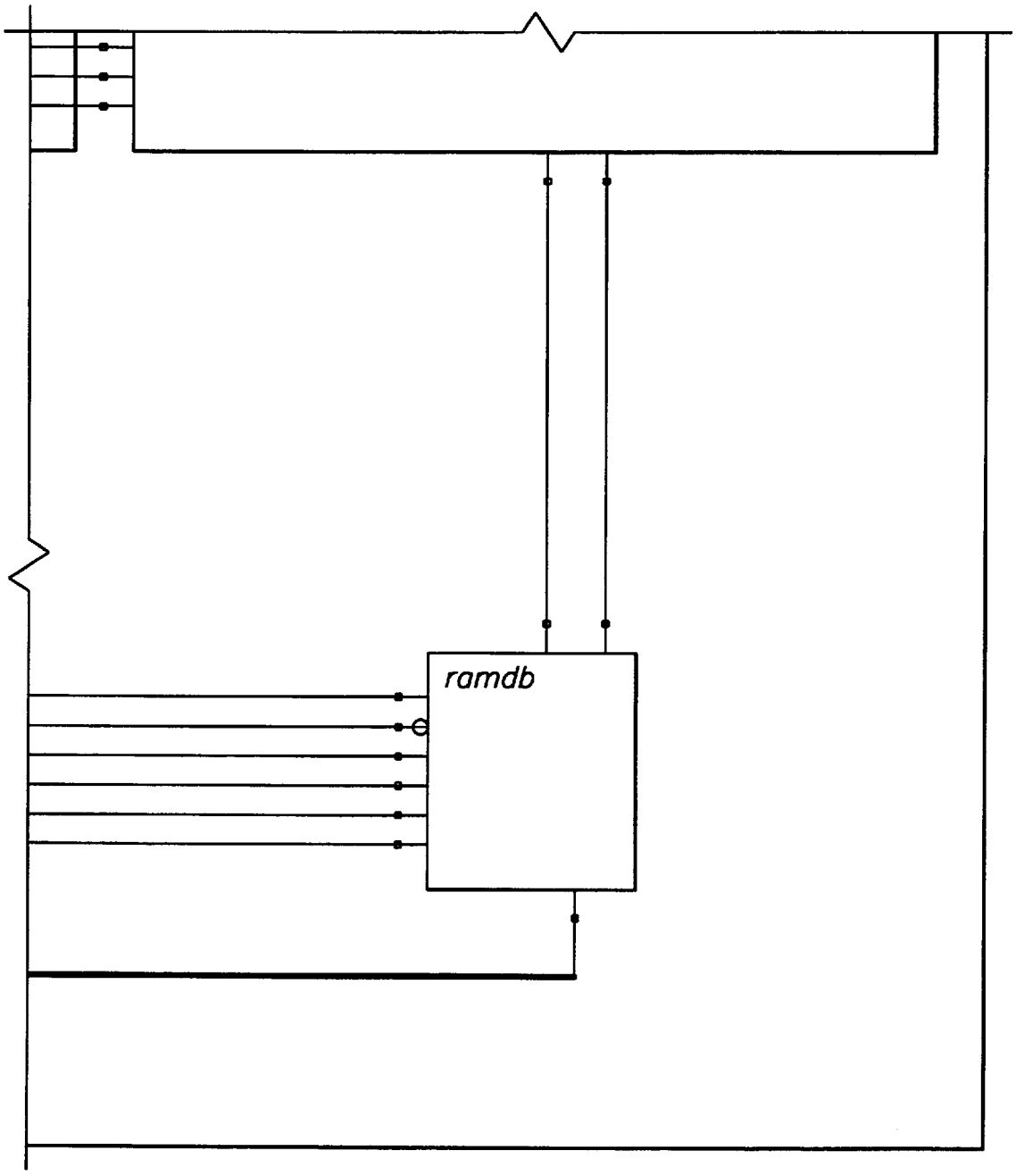


Fig 1.03EH

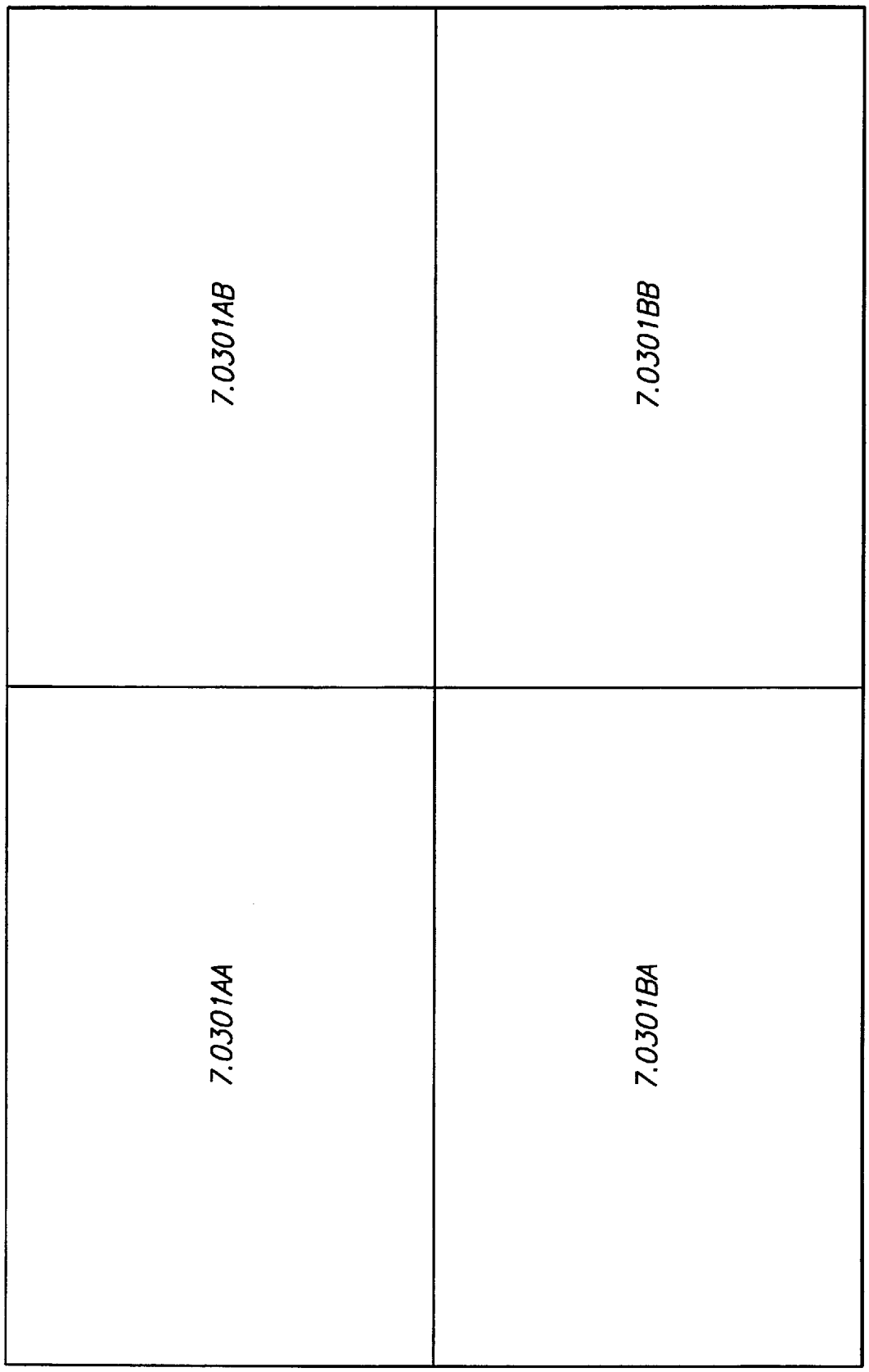


FIG. 7.0301

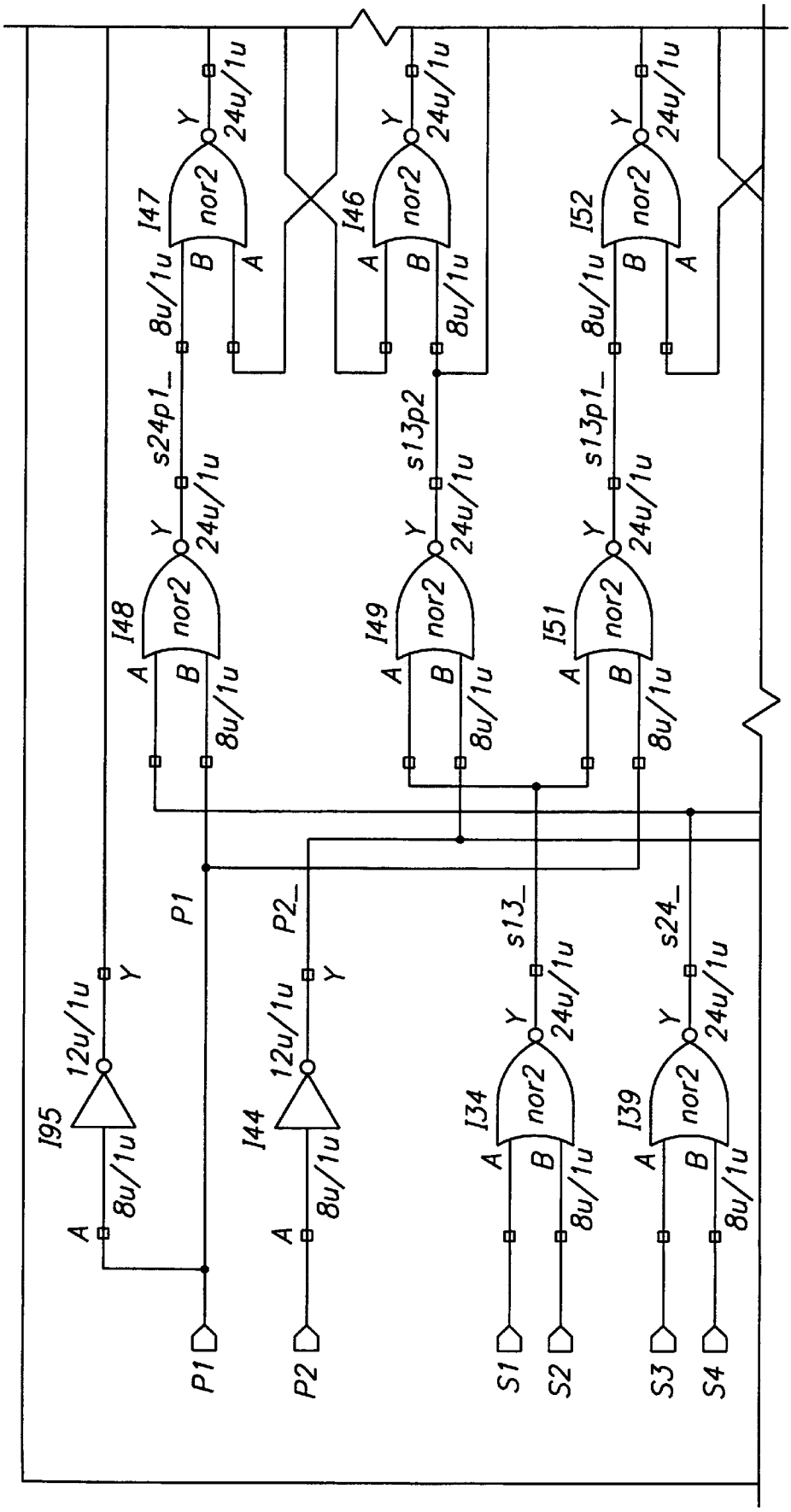


FIG 11.00E 00 VAA

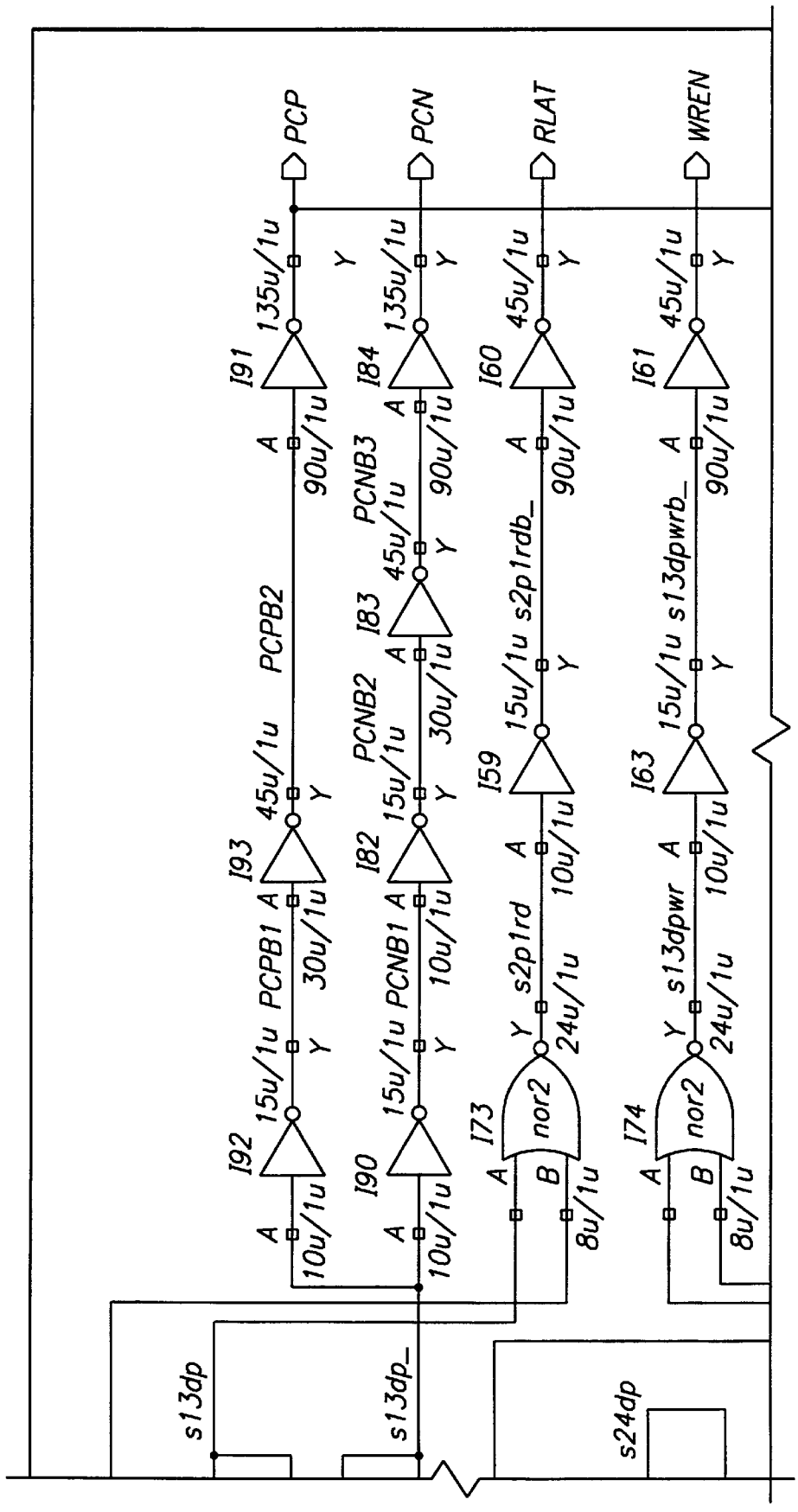


FIG. 11.0011 11A 11B

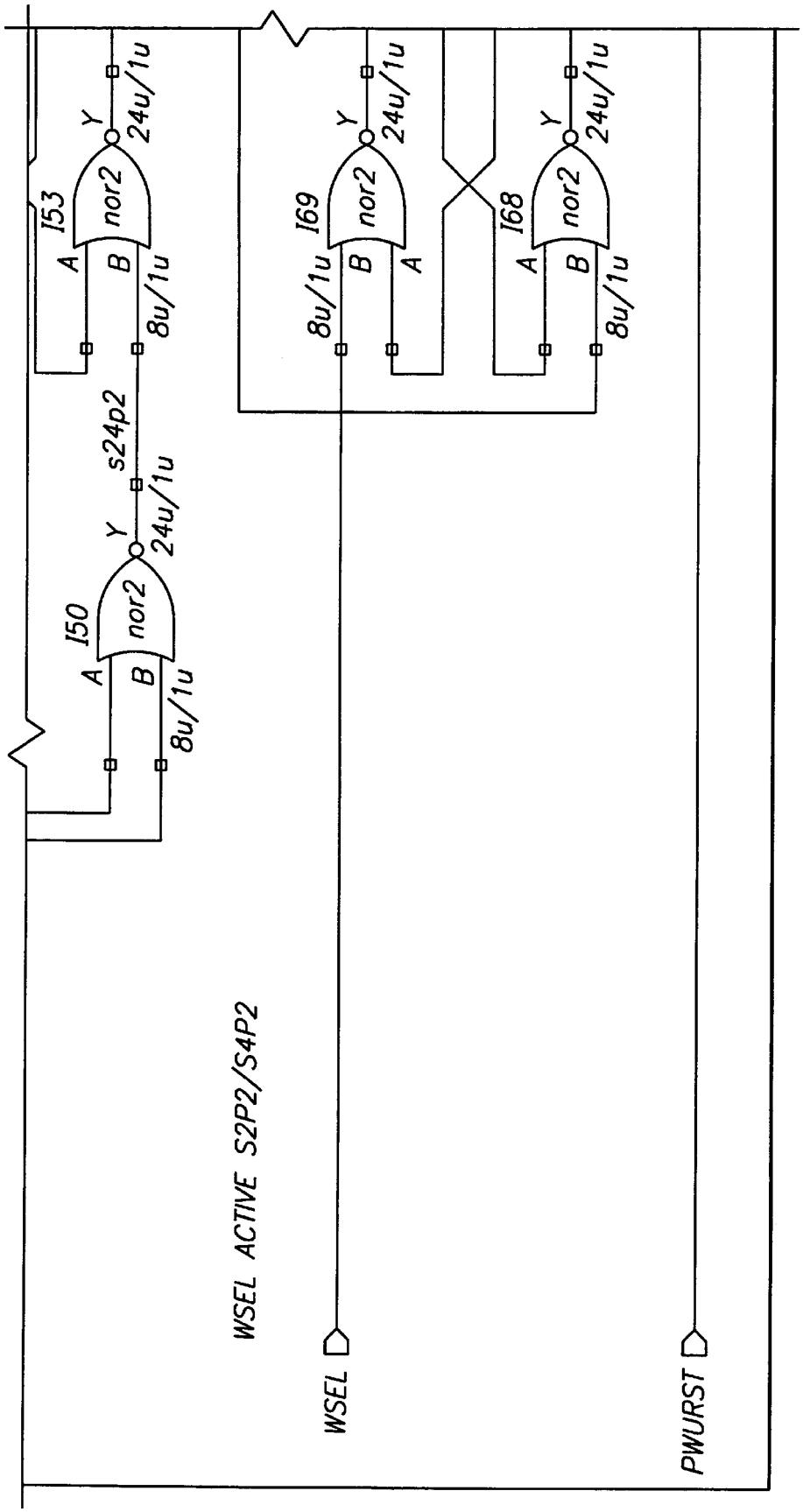

I53
nor2
A
B
Y
24u/1u
8u/1u
s24p2
I50
I69
I68
WSEL ACTIVE S2P2/S4P2
WSEL
PWURST

FIG 3L

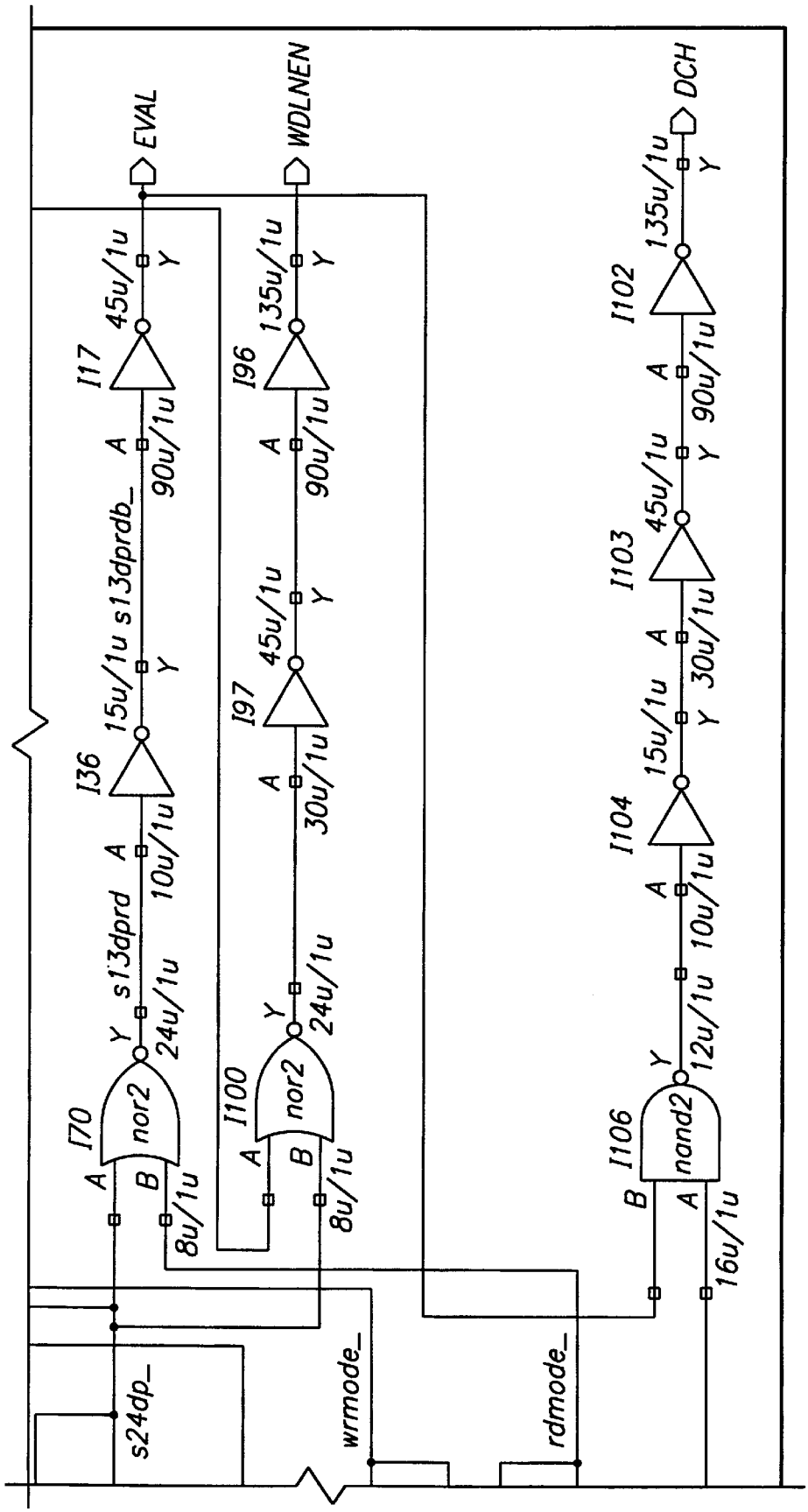
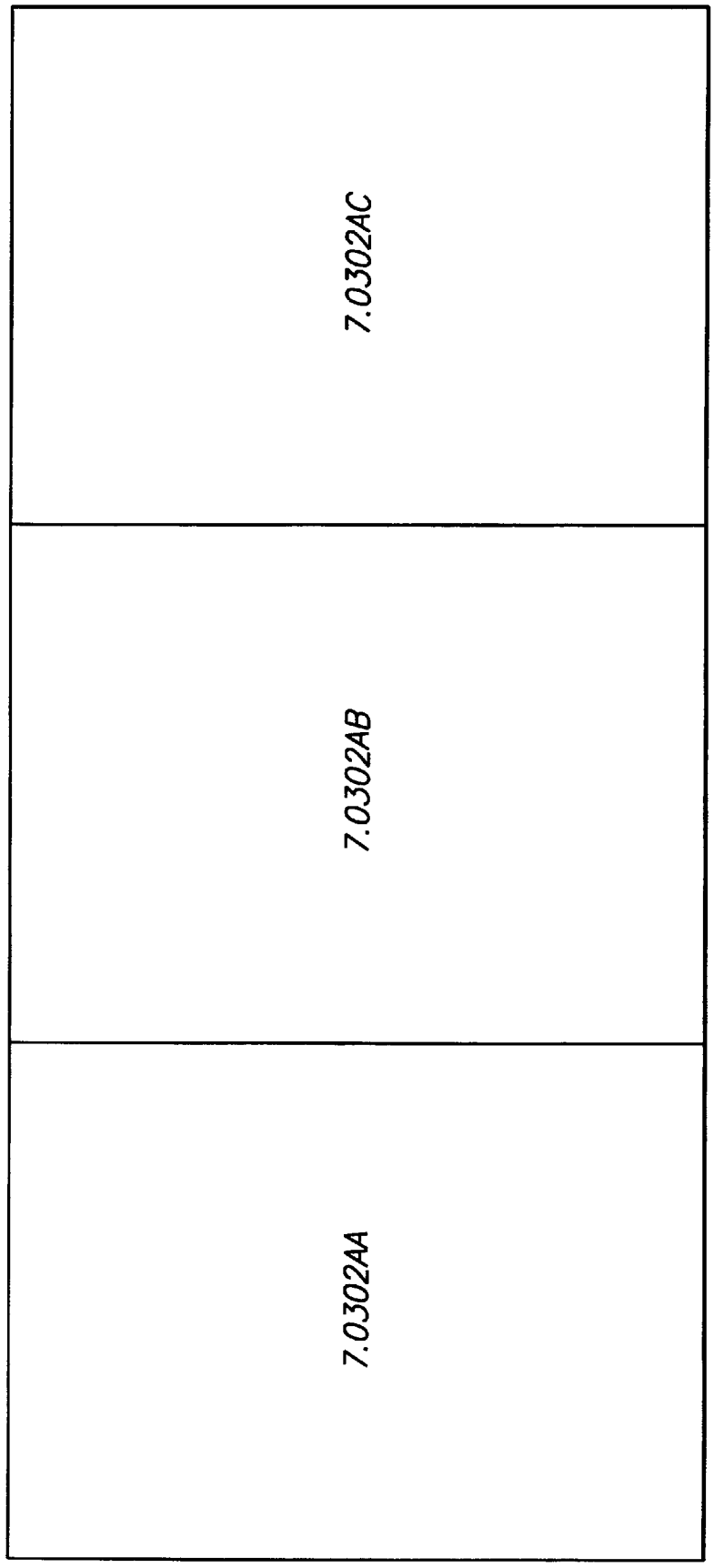

EVAL
WDLNEN
DCH
I17
I96
I102
I36
I97
I103
I70
I100
I104
I106
nor2
nand2
s13dprd
s13dprdb_
s24dp_
wrmode_
rdmode_

FIG. 11.00E


7.0302AC
7.0302AB
7.0302AA
FIG. 7.0302

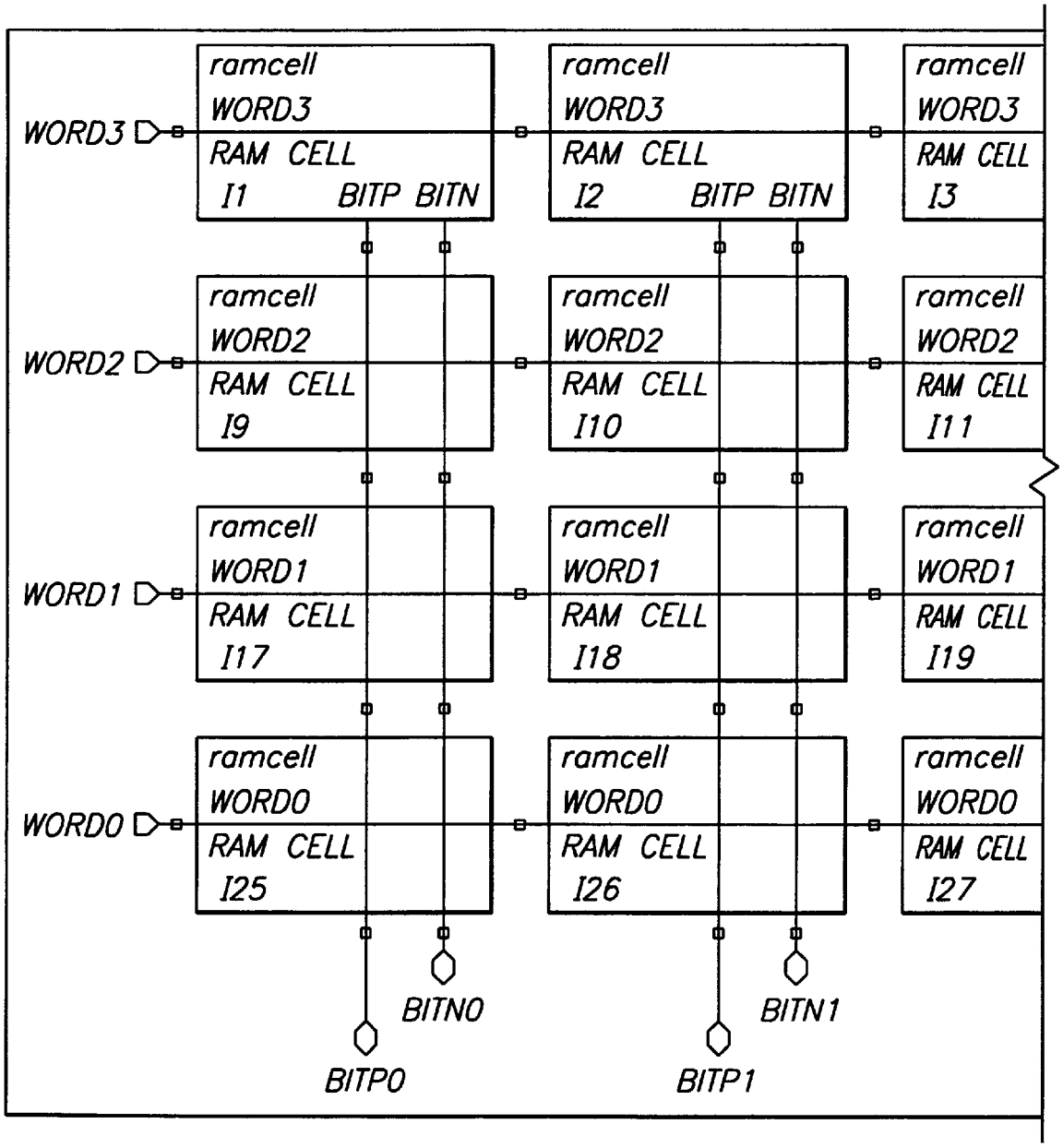

ramcell
WORD3
RAM CELL
I1
BITP BITN
ramcell
WORD3
RAM CELL
I2
BITP BITN
ramcell
WORD3
RAM CELL
I3
WORD3
ramcell
WORD2
RAM CELL
I9
ramcell
WORD2
RAM CELL
I10
ramcell
WORD2
RAM CELL
I11
WORD2
ramcell
WORD1
RAM CELL
I17
ramcell
WORD1
RAM CELL
I18
ramcell
WORD1
RAM CELL
I19
WORD1
ramcell
WORD0
RAM CELL
I25
ramcell
WORD0
RAM CELL
I26
ramcell
WORD0
RAM CELL
I27
WORD0
BITN0
BITN1
BITP0
BITP1

Fig 1.0302AA

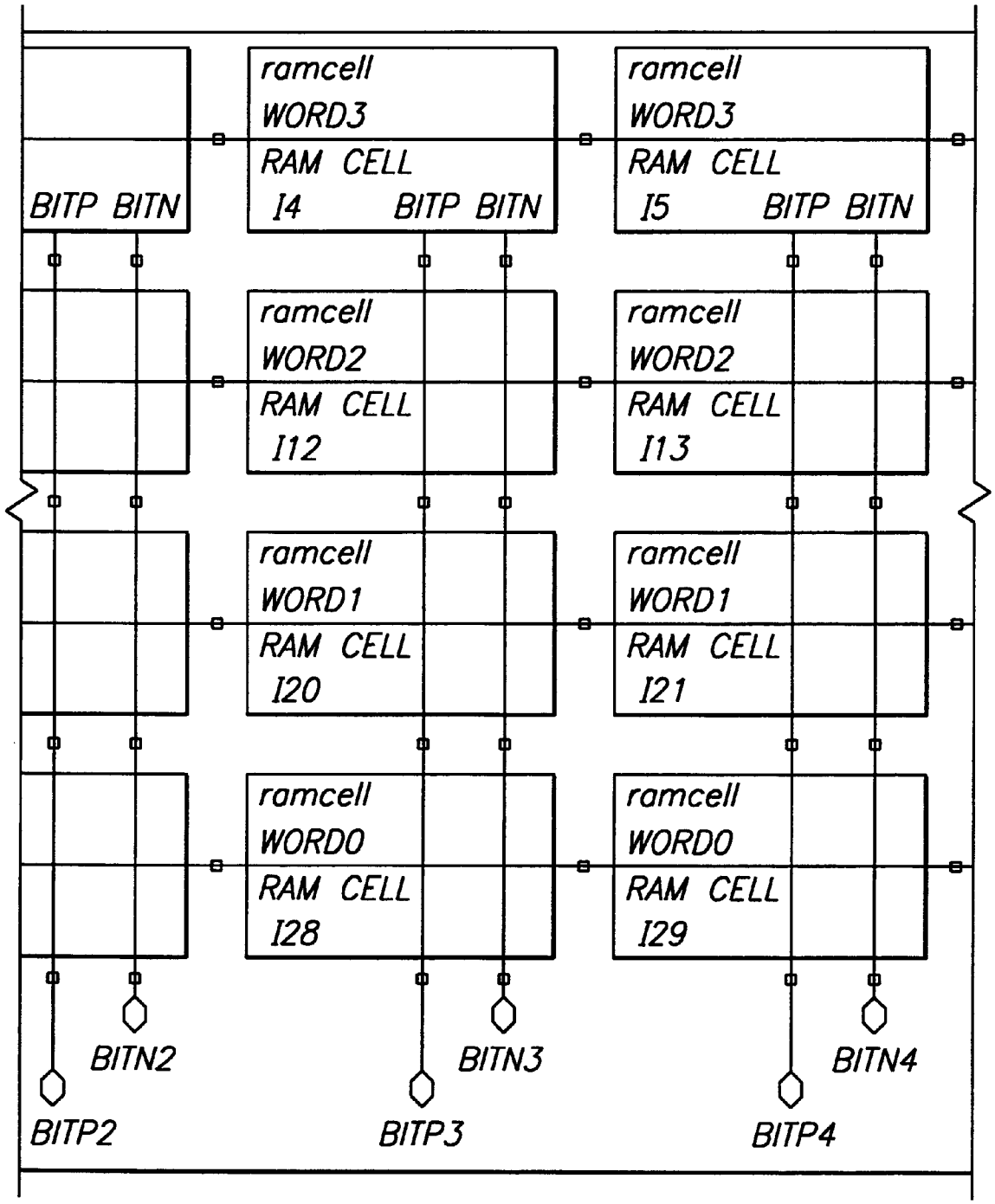

ramcell
WORD3
RAM CELL
I4
BITP BITN
ramcell
WORD3
RAM CELL
I5
BITP BITN
BITP BITN
ramcell
WORD2
RAM CELL
I12
ramcell
WORD2
RAM CELL
I13
ramcell
WORD1
RAM CELL
I20
ramcell
WORD1
RAM CELL
I21
ramcell
WORD0
RAM CELL
I28
ramcell
WORD0
RAM CELL
I29
BITN2
BITN3
BITN4
BITP2
BITP3
BITP4

Fig 1.0300AB

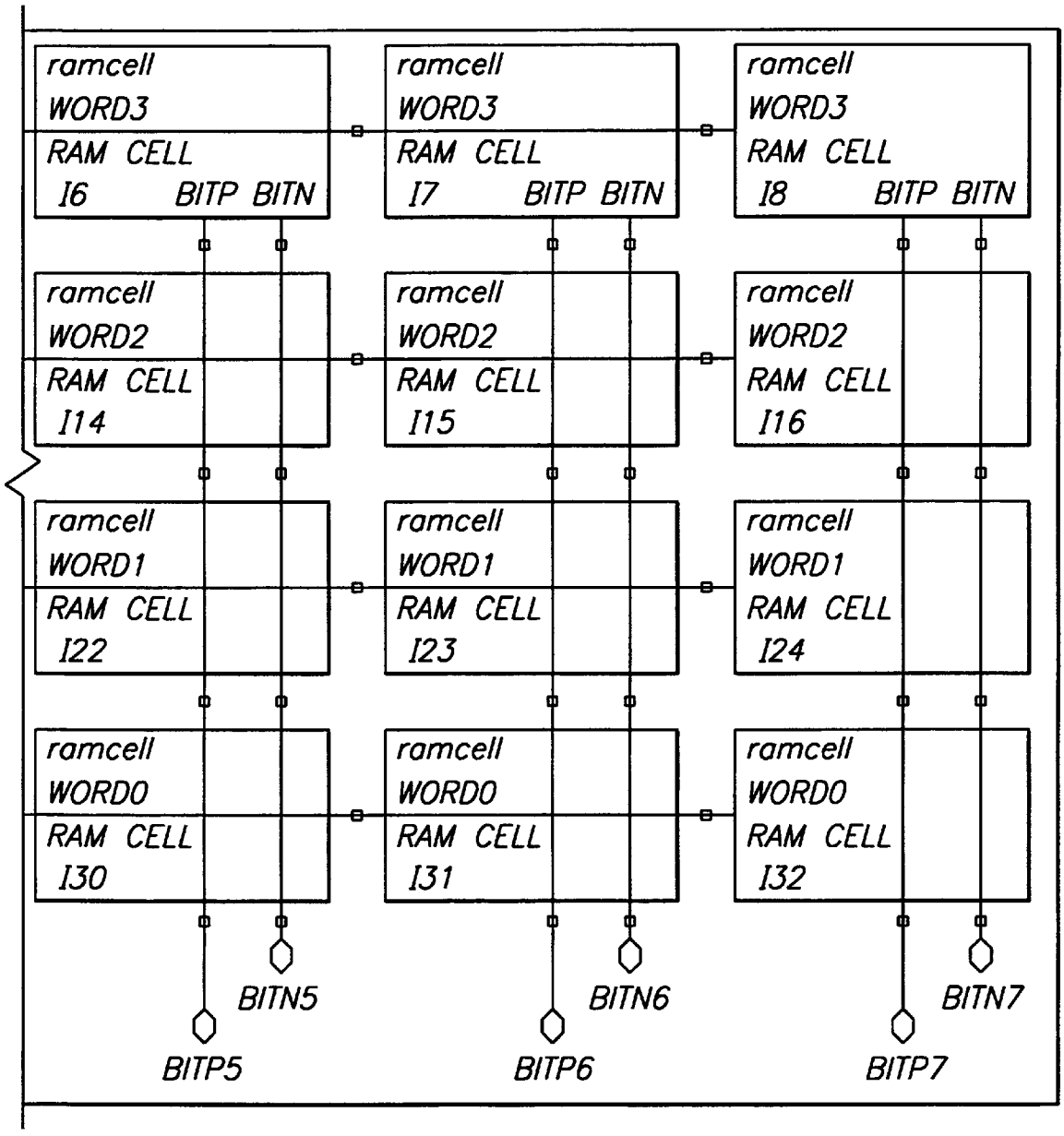
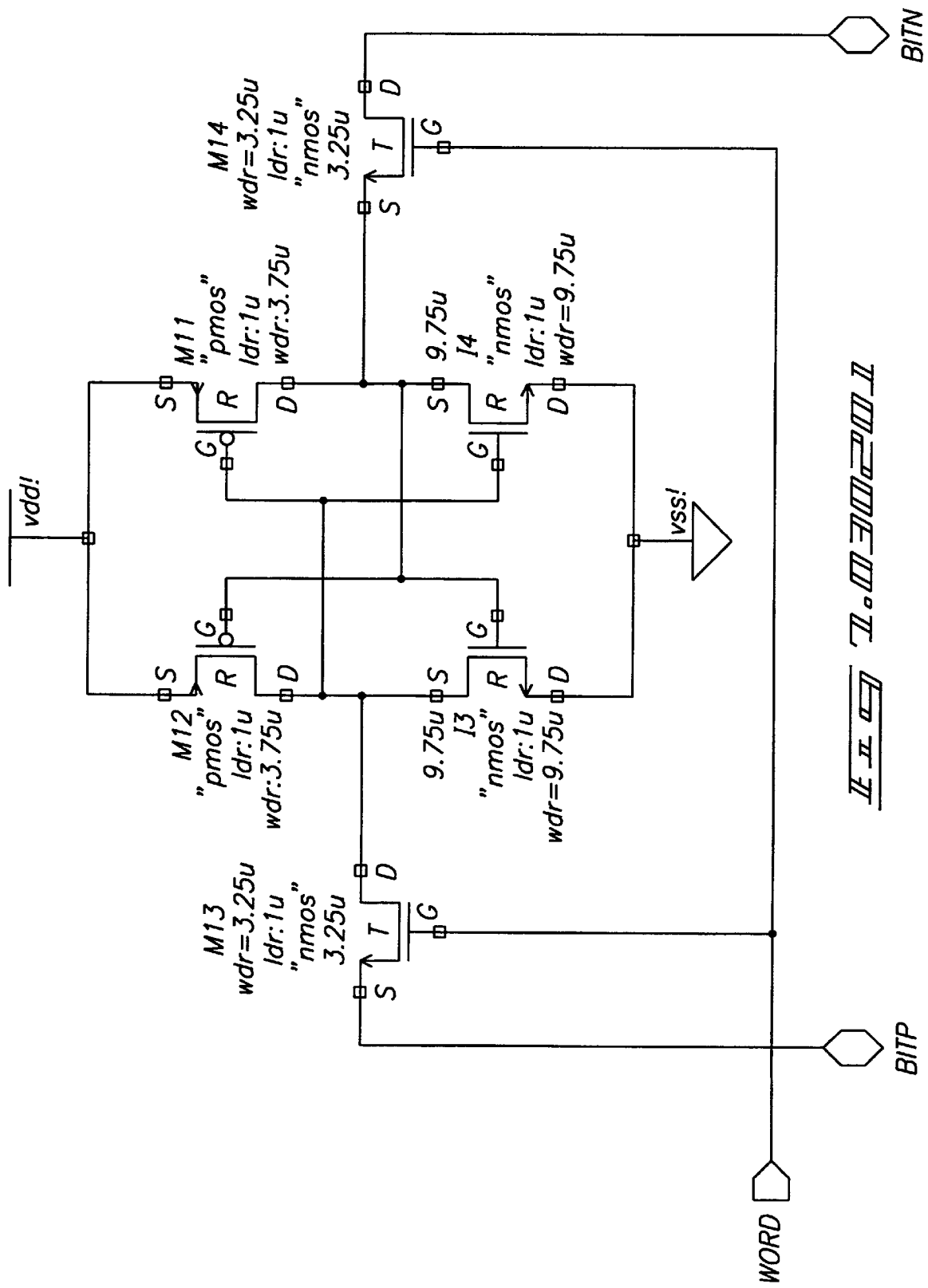

ramcell
WORD3
RAM CELL
I6
BITP BITN
ramcell
WORD3
RAM CELL
I7
BITP BITN
ramcell
WORD3
RAM CELL
I8
BITP BITN
ramcell
WORD2
RAM CELL
I14
ramcell
WORD2
RAM CELL
I15
ramcell
WORD2
RAM CELL
I16
ramcell
WORD1
RAM CELL
I22
ramcell
WORD1
RAM CELL
I23
ramcell
WORD1
RAM CELL
I24
ramcell
WORD0
RAM CELL
I30
ramcell
WORD0
RAM CELL
I31
ramcell
WORD0
RAM CELL
I32
BITN5
BITN6
BITN7
BITP5
BITP6
BITP7

Fig 1.0302AC


BITN
M14
wdr=3.25u
ldr:1u
"nmos"
3.25u
M11
"pmos"
ldr:1u
wdr:3.75u
9.75u
I4
"nmos"
ldr:1u
wdr=9.75u
vdd!
vss!
M12
"pmos"
ldr:1u
wdr:3.75u
9.75u
I3
"nmos"
ldr:1u
wdr=9.75u
M13
wdr=3.25u
ldr:1u
"nmos"
3.25u
BITP
WORD
FIG. 3E

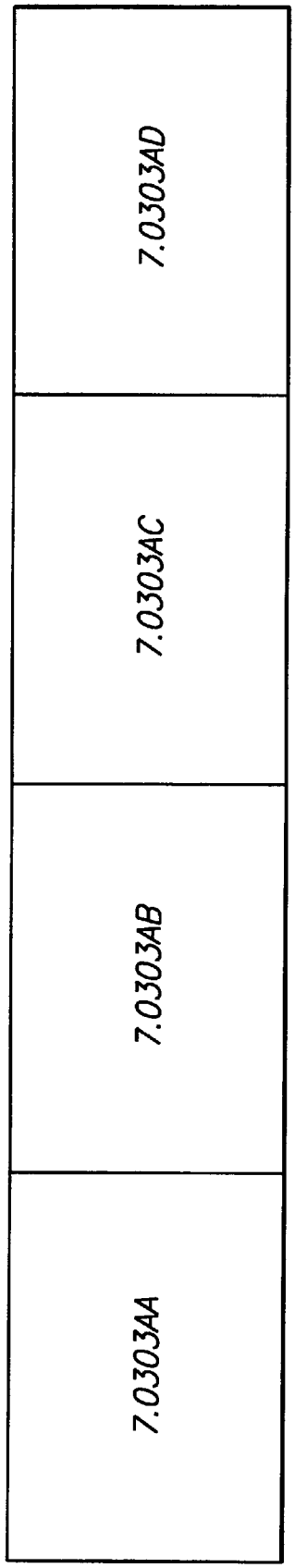


FIG. 7.0303AE

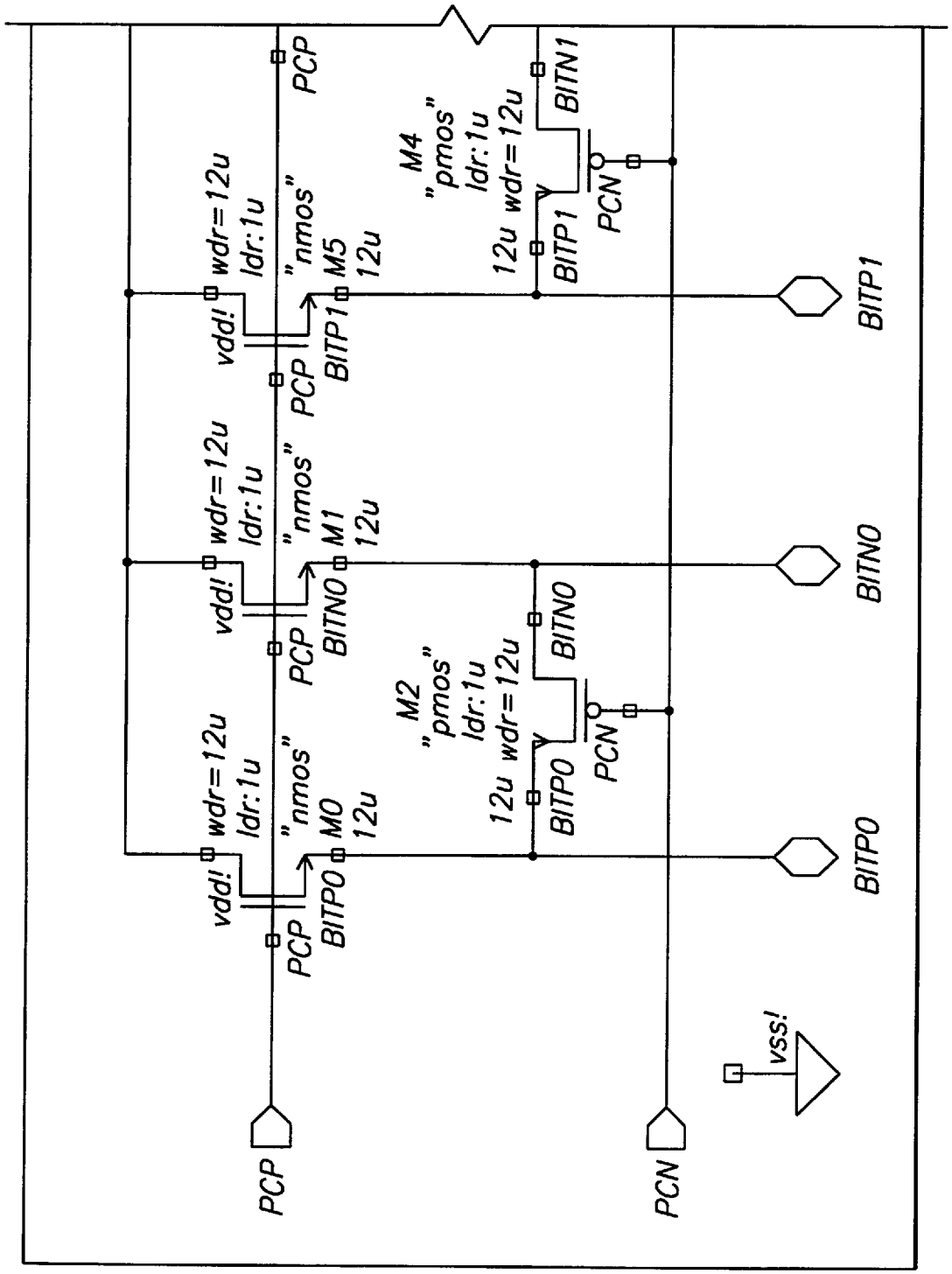

PCP
PCN
vss!
vdd!
"nmos"
"pmos"
wdr=12u
ldr:1u
12u
M0
M1
M2
M4
M5
BITP0
BITP1
BITN0
BITN1
PCP
PCN

FIG. 11E

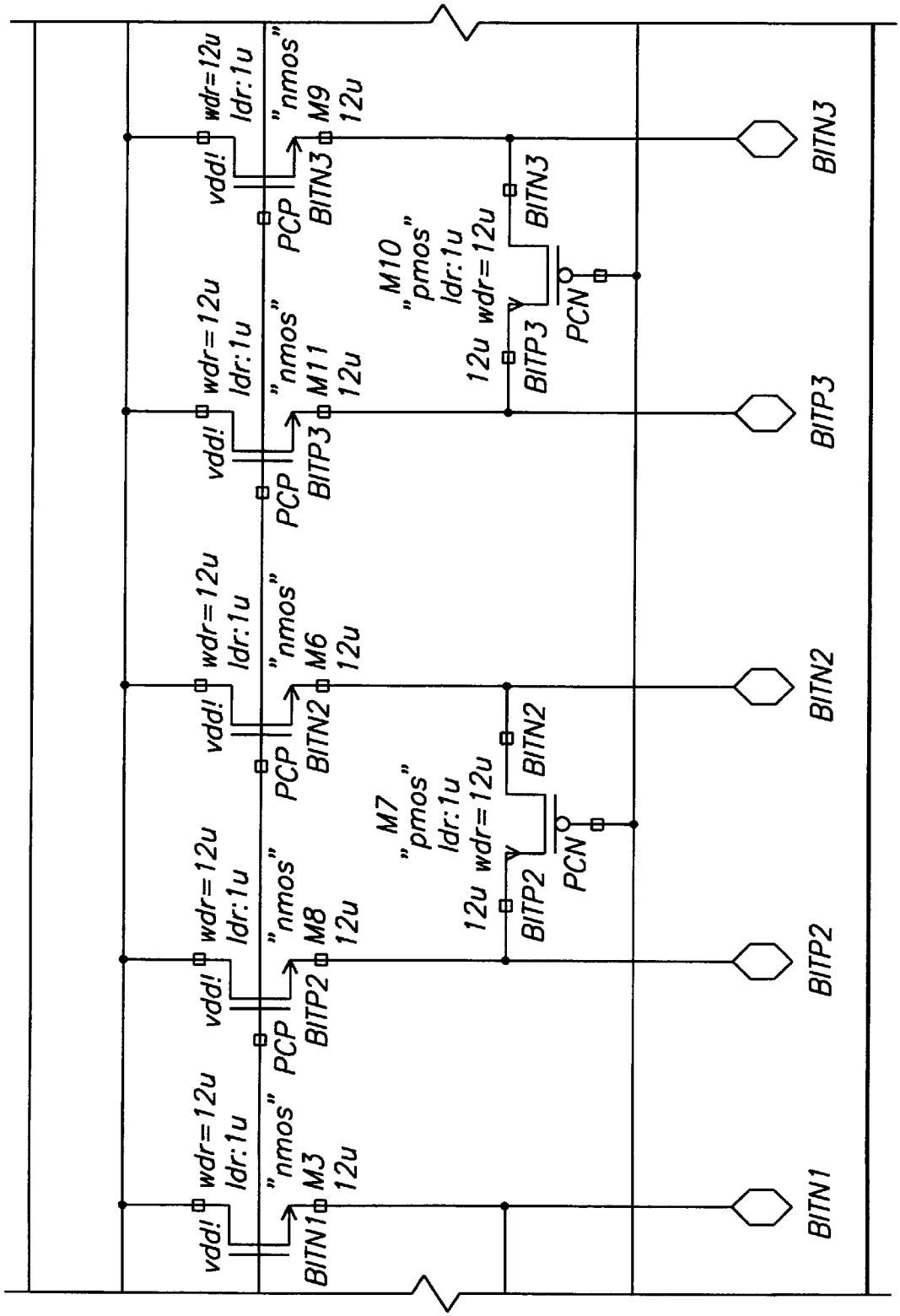
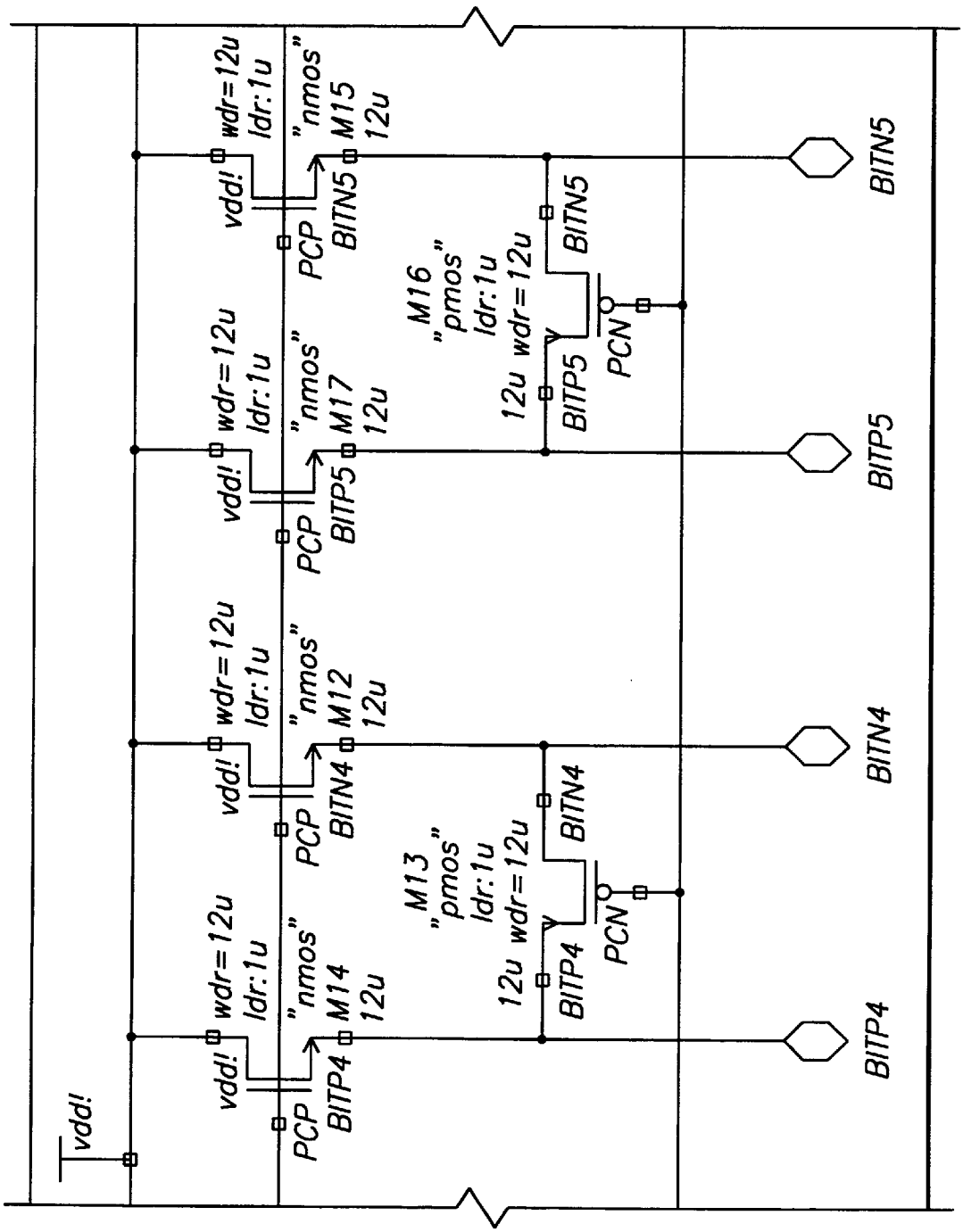

vdd!
wdr=12u
ldr:1u
"nmos"
M3
12u
BITN1
PCP
BITP2
M8
M7
"pmos"
M6
BITN2
BITP3
M11
M10
BITN3
M9
PCN
BITP1
BITP2
BITP3
BITN1
BITN2
BITN3

FIG. 11


vdd!
vdd!
wdr=12u
ldr:1u
"nmos"
M14
12u
PCP
BITP4
"pmos"
ldr:1u
wdr=12u
M13
12u
BITP4
PCN
BITN4
BITN4
vdd!
wdr=12u
ldr:1u
"nmos"
M12
12u
PCP
BITN4
"pmos"
ldr:1u
wdr=12u
M16
12u
BITP5
PCN
BITN5
BITN5
vdd!
wdr=12u
ldr:1u
"nmos"
M17
12u
PCP
BITP5
BITP5
vdd!
wdr=12u
ldr:1u
"nmos"
M15
12u
PCP
BITN5

ФИГ. 11

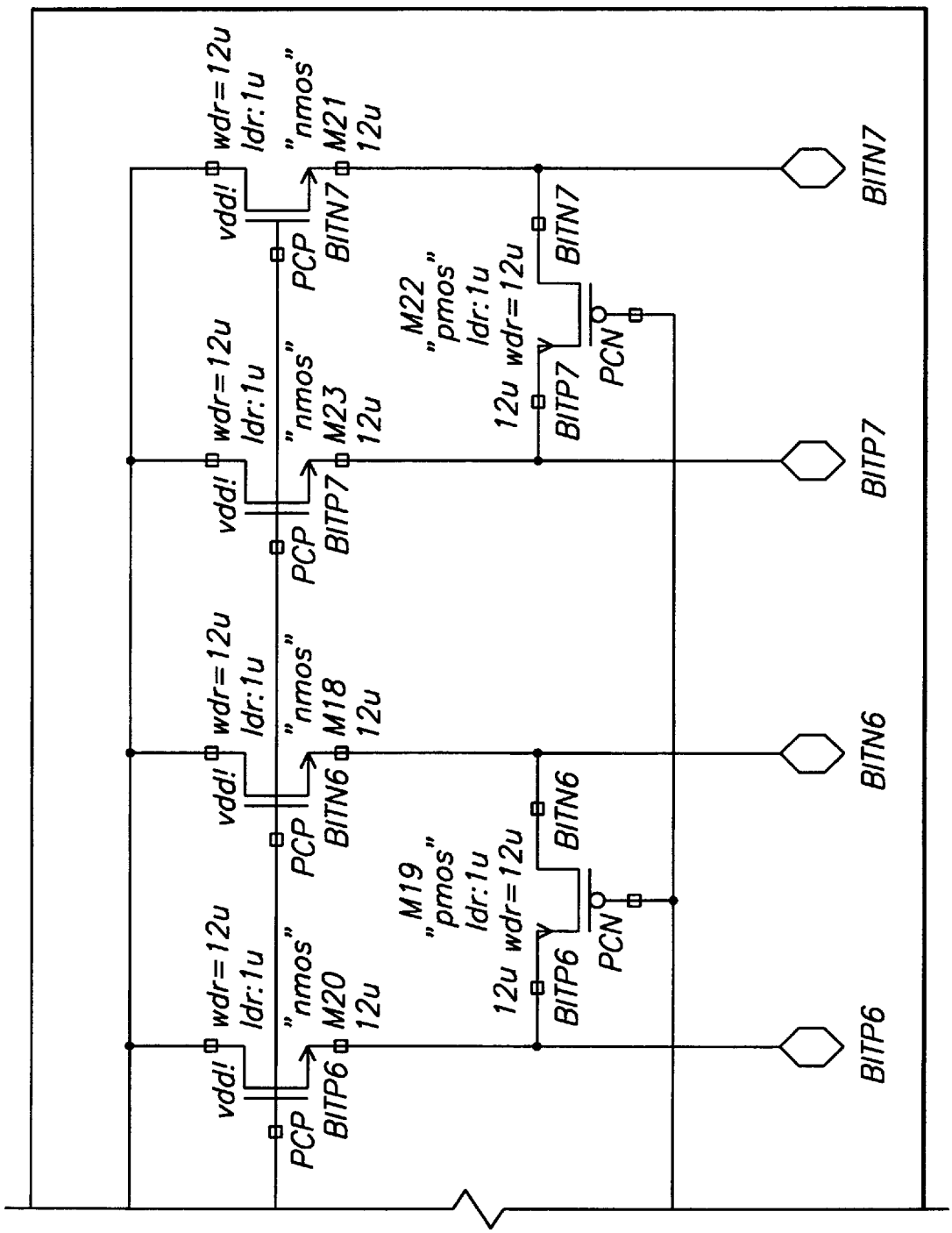


FIG. 7.0E0E0E0

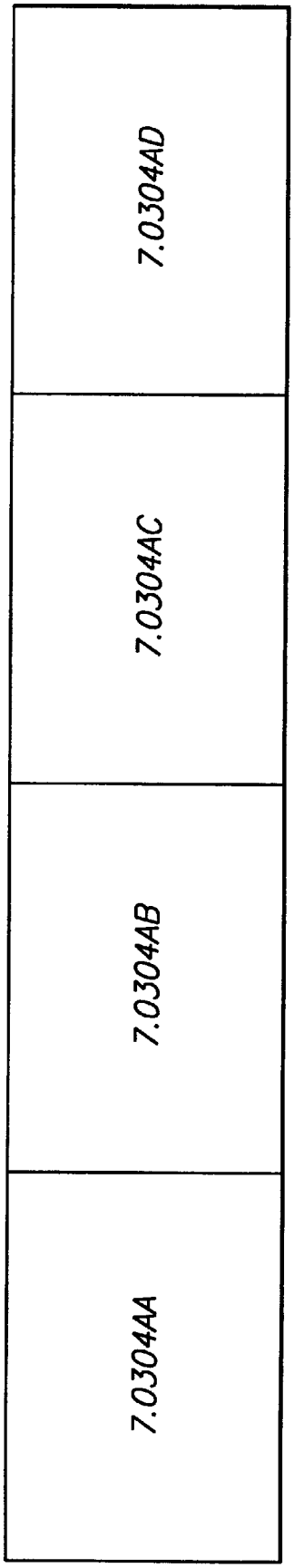


FIG. 7.0304C

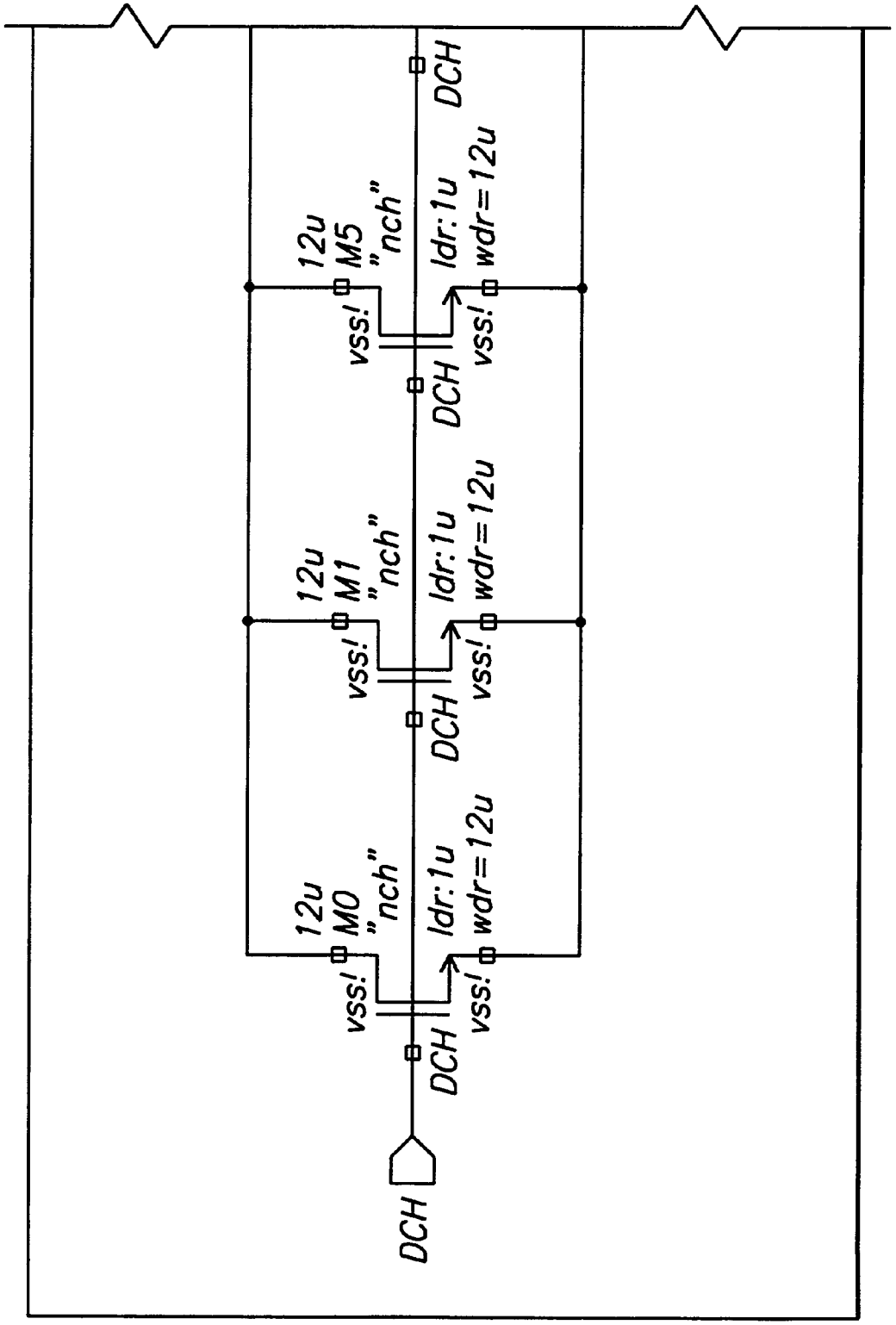

DCH
12u
M5
"nch"
ldr:1u
wdr=12u
vss!
DCH
vss!
12u
M1
"nch"
ldr:1u
wdr=12u
vss!
DCH
vss!
12u
M0
"nch"
ldr:1u
wdr=12u
vss!
DCH
vss!
DCH

FIG. 6.0E.11

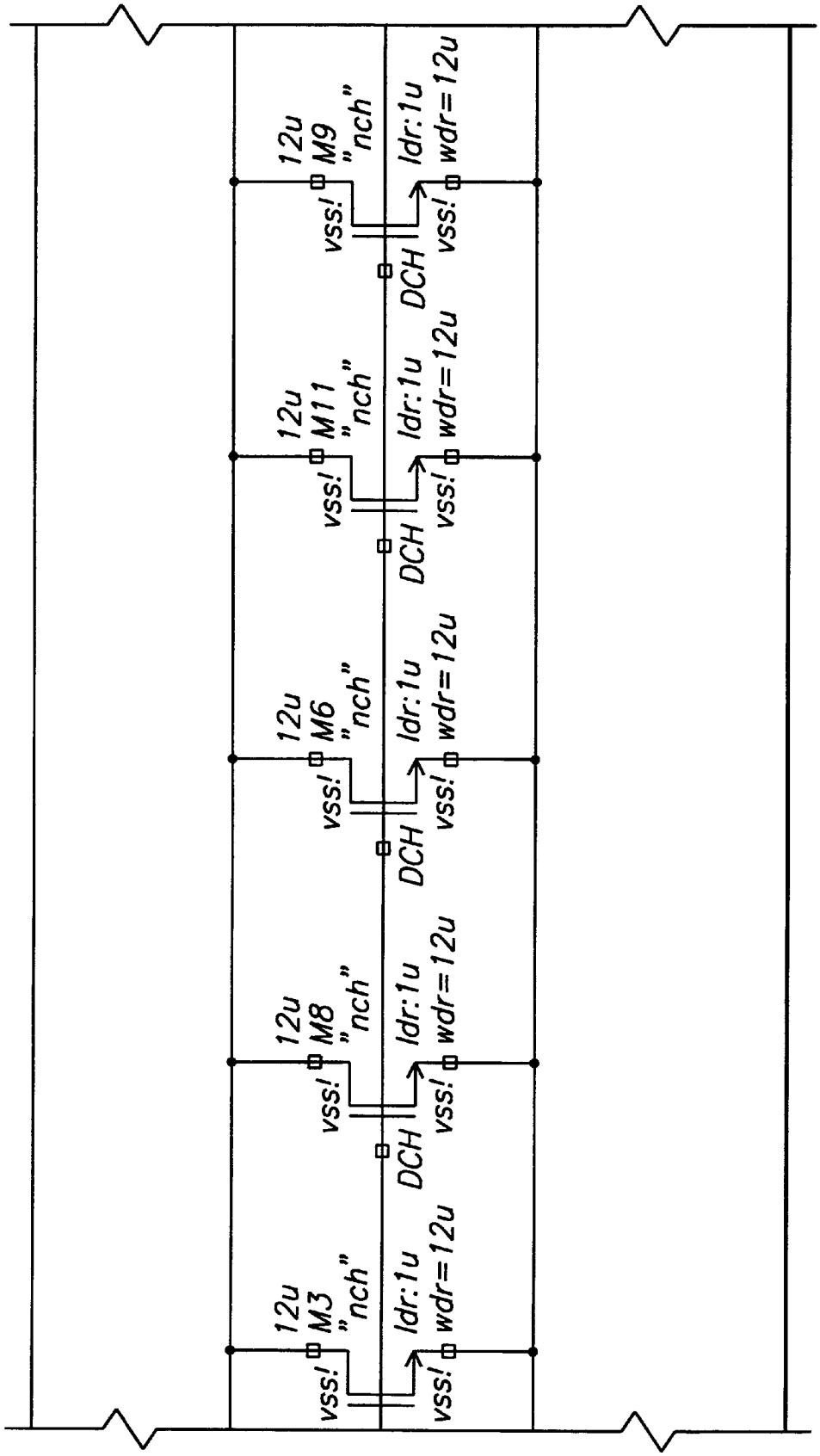

12u
M9
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M11
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M6
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M8
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M3
"nch"
ldr:1u
wdr=12u
vss!

Fig. 11.00E

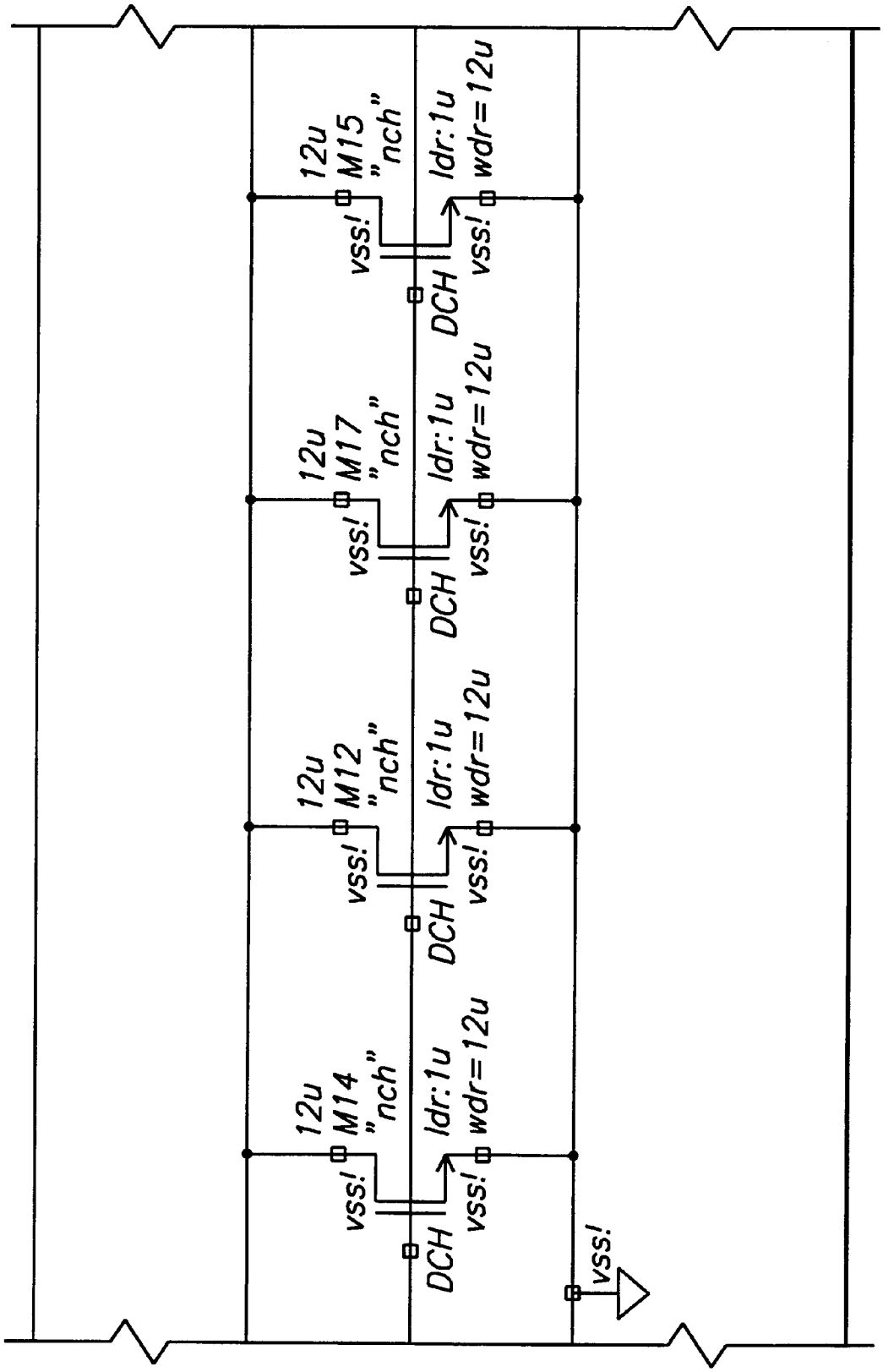

12u
M15
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M17
"nch"
ldr:1u
wdr=12u
12u
M12
"nch"
ldr:1u
wdr=12u
12u
M14
"nch"
ldr:1u
wdr=12u

FIG. 261

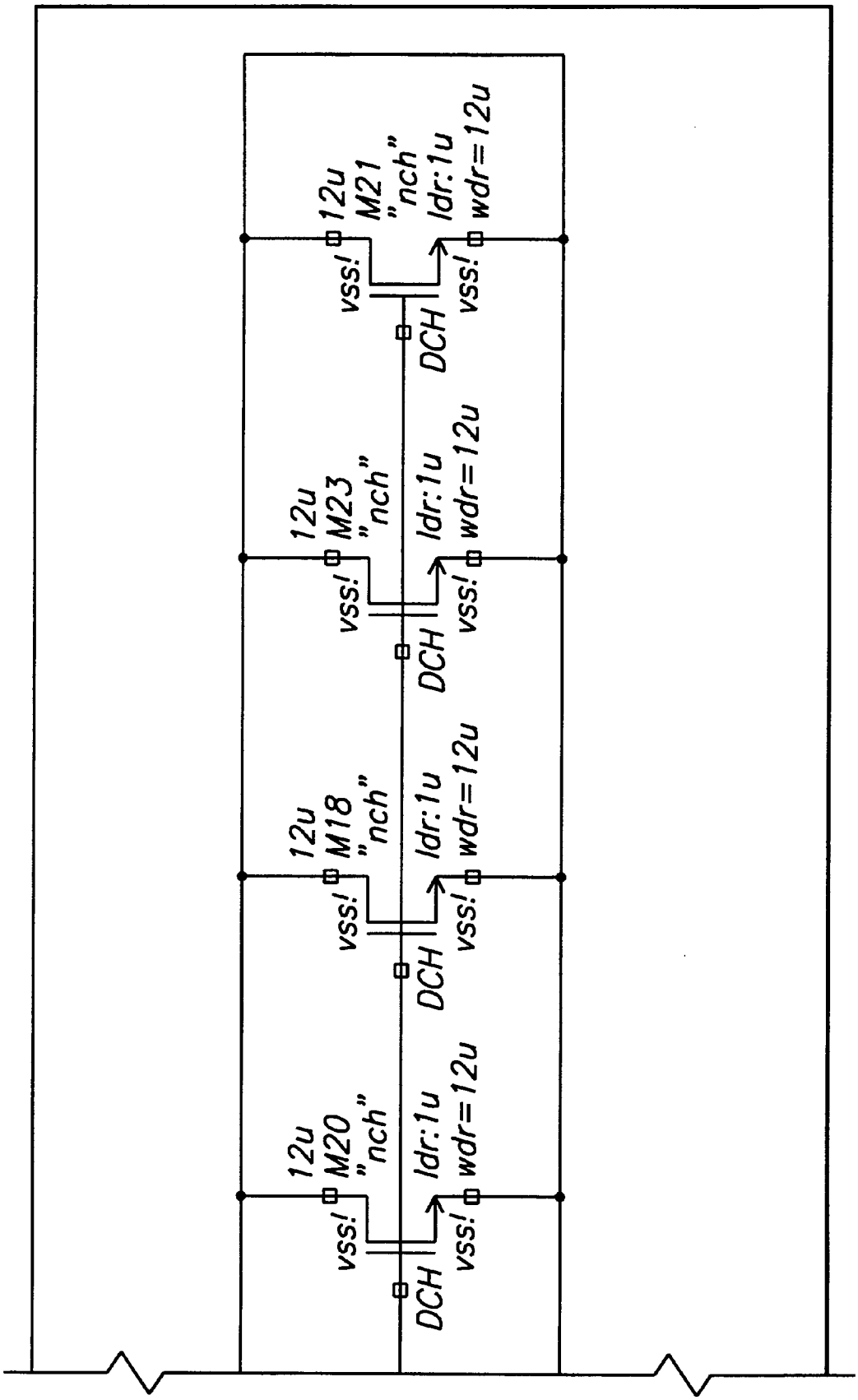

12u
M21
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M23
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M18
"nch"
ldr:1u
wdr=12u
vss!
DCH
12u
M20
"nch"
ldr:1u
wdr=12u
vss!
DCH

FIG. 262

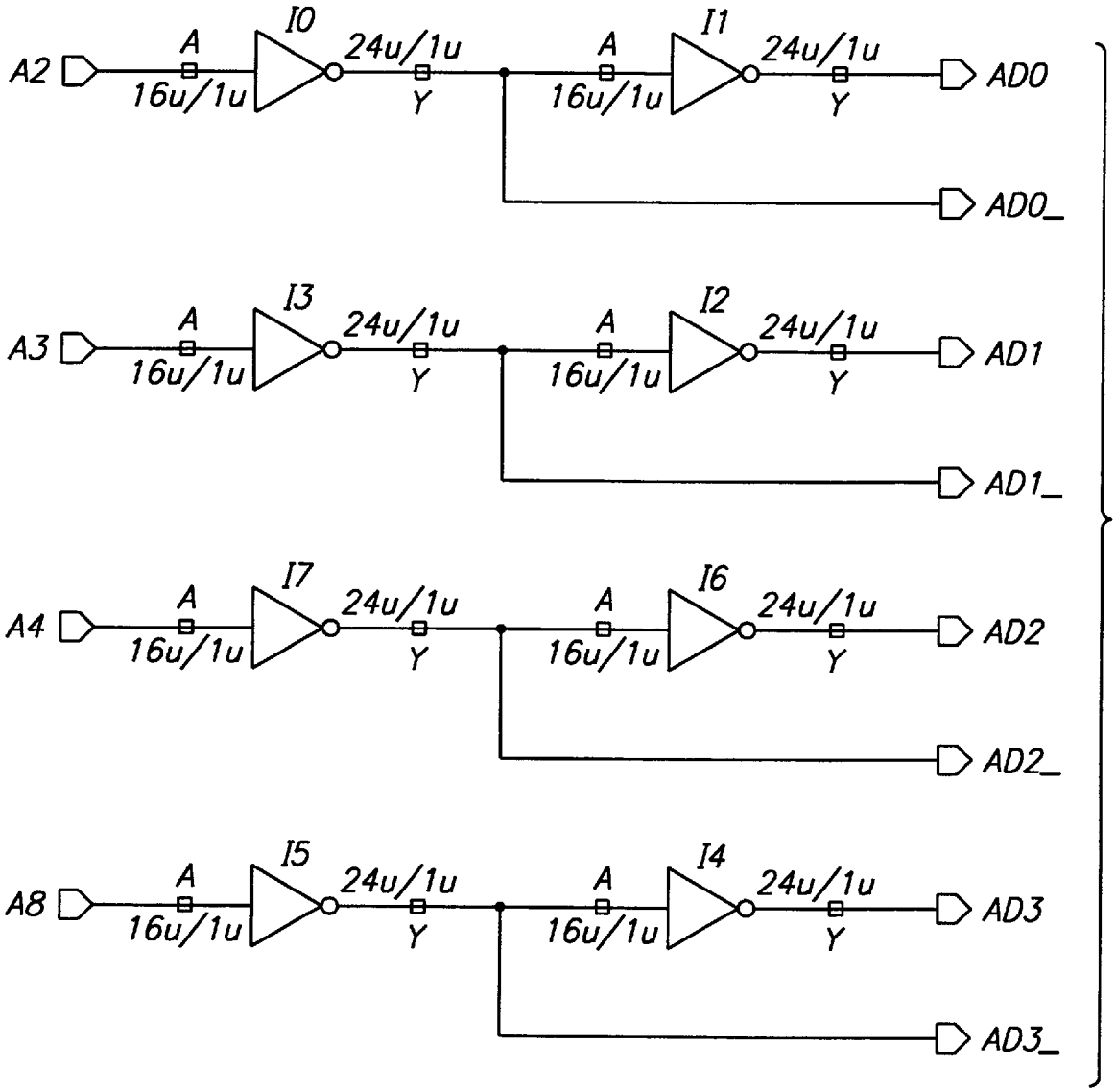

A2
A
16u/1u
I0
24u/1u
Y
A
16u/1u
I1
24u/1u
Y
AD0
AD0_
A3
A
16u/1u
I3
24u/1u
Y
A
16u/1u
I2
24u/1u
Y
AD1
AD1_
A4
A
16u/1u
I7
24u/1u
Y
A
16u/1u
I6
24u/1u
Y
AD2
AD2_
A8
A
16u/1u
I5
24u/1u
Y
A
16u/1u
I4
24u/1u
Y
AD3
AD3_

Fig 1.0305

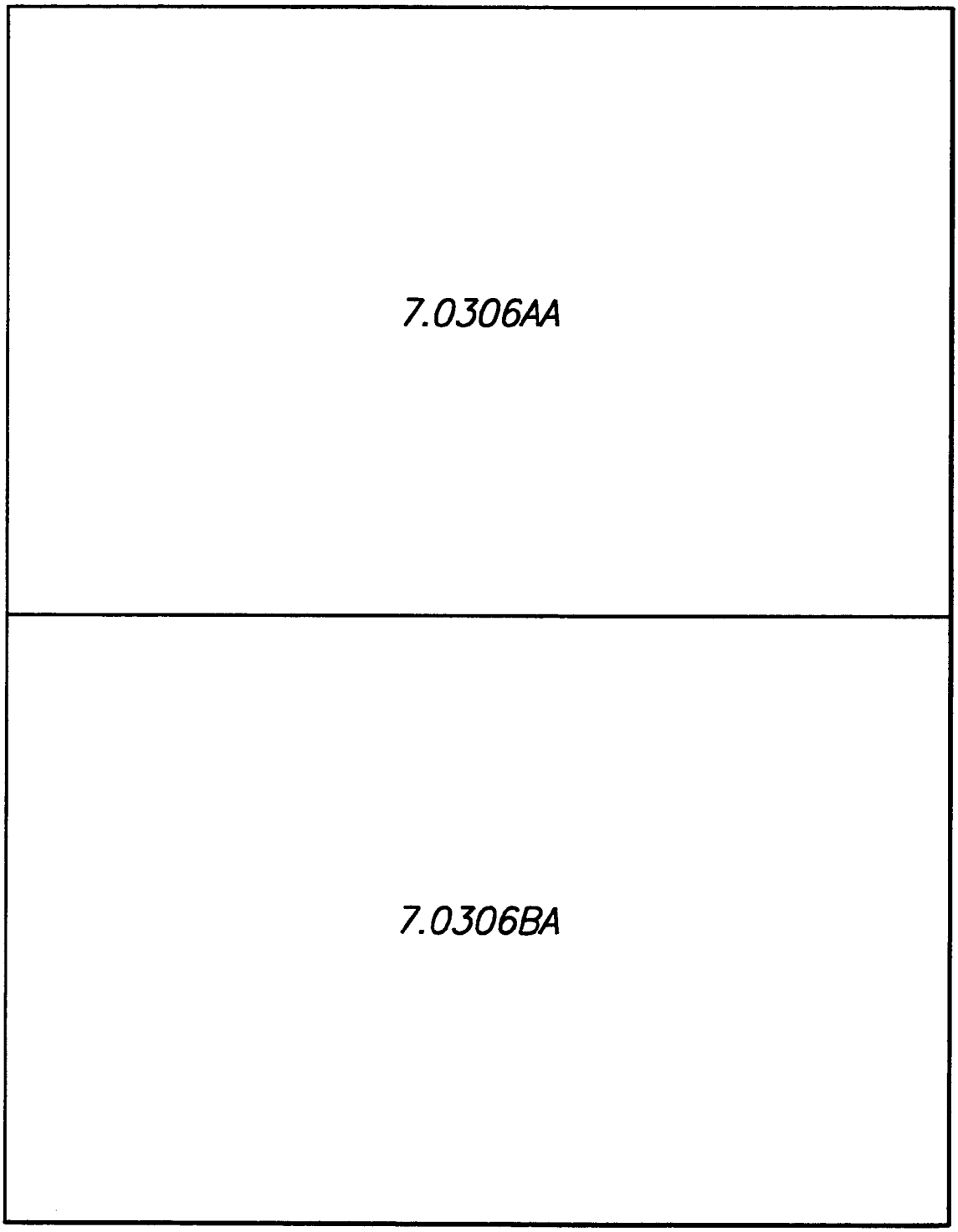


Fig 7.0306

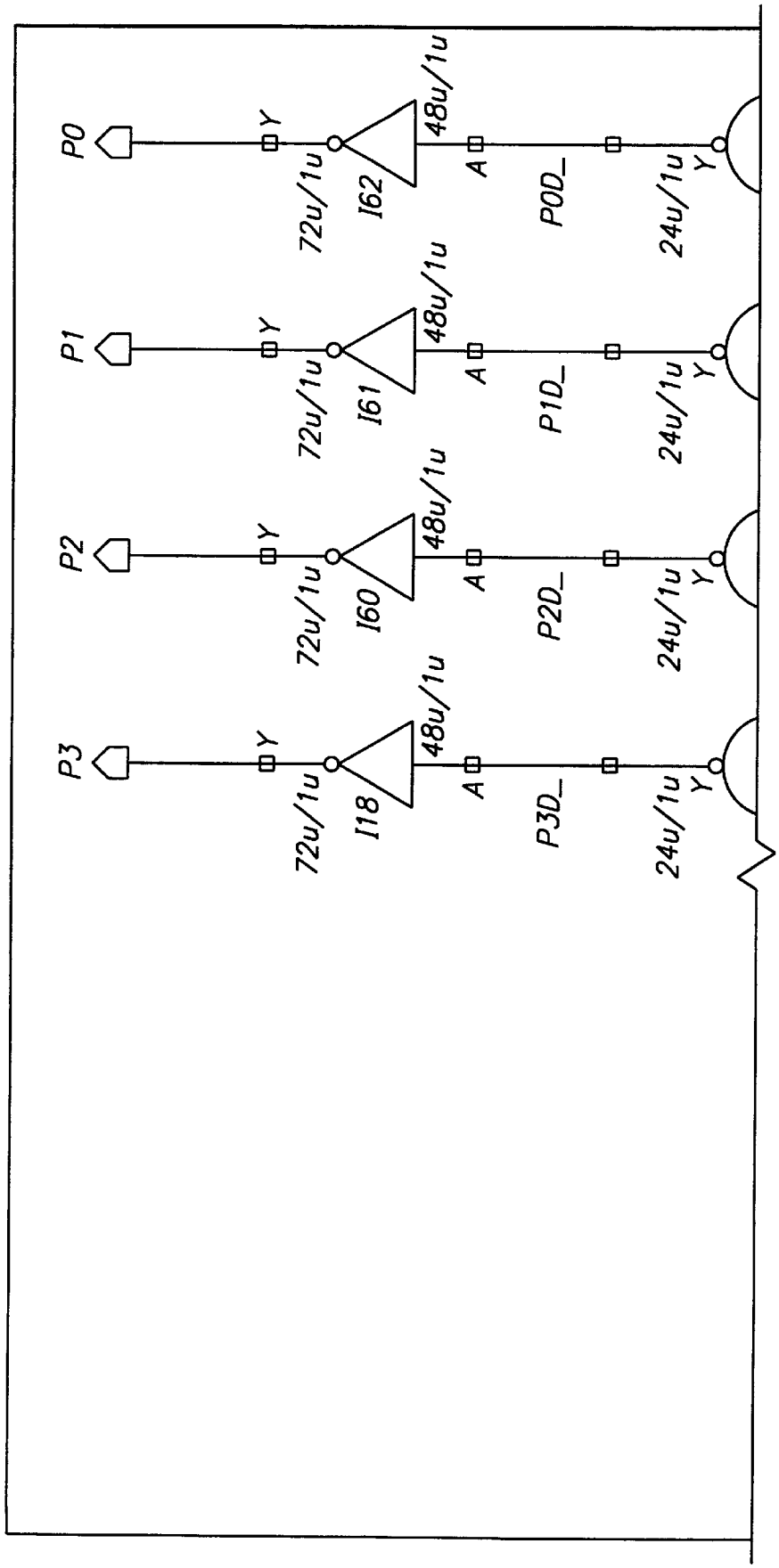


FIG. 11.00SHEET

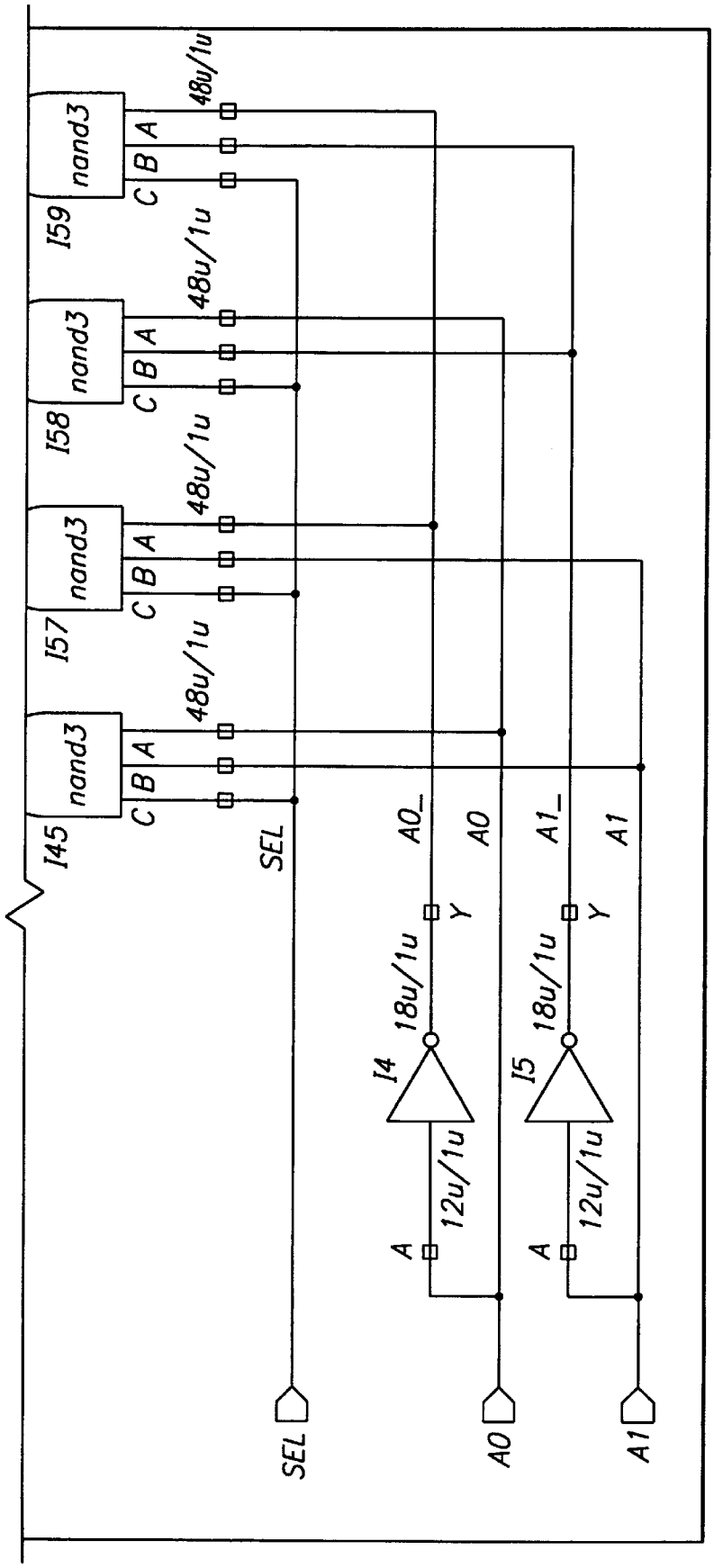

I45
nand3
A
B
C
48u/1u
SEL
I57
I58
I59
A0_
A0
A1_
A1
I4
I5
18u/1u
Y
12u/1u
A

FIG. 7L

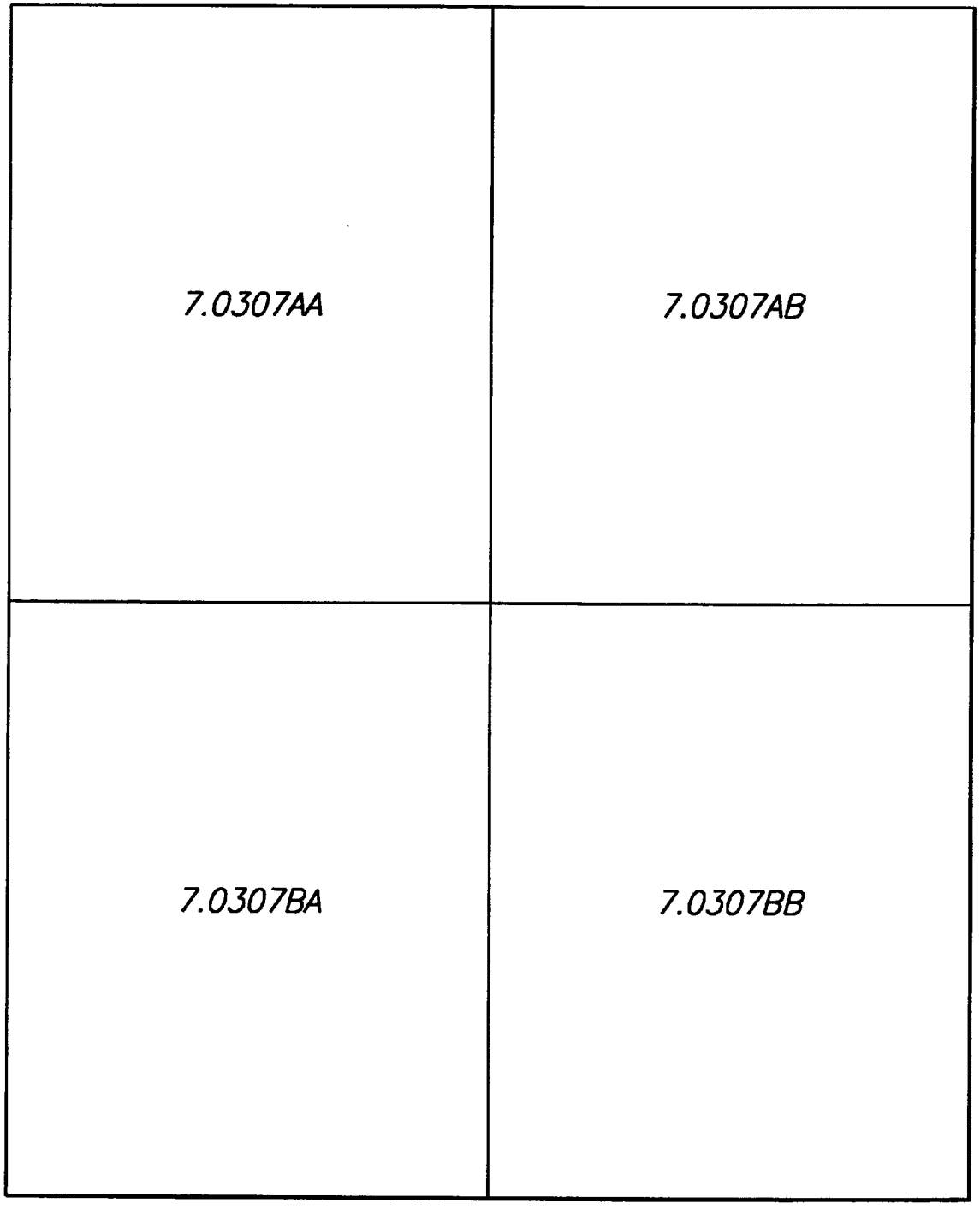


Fig 7.0307

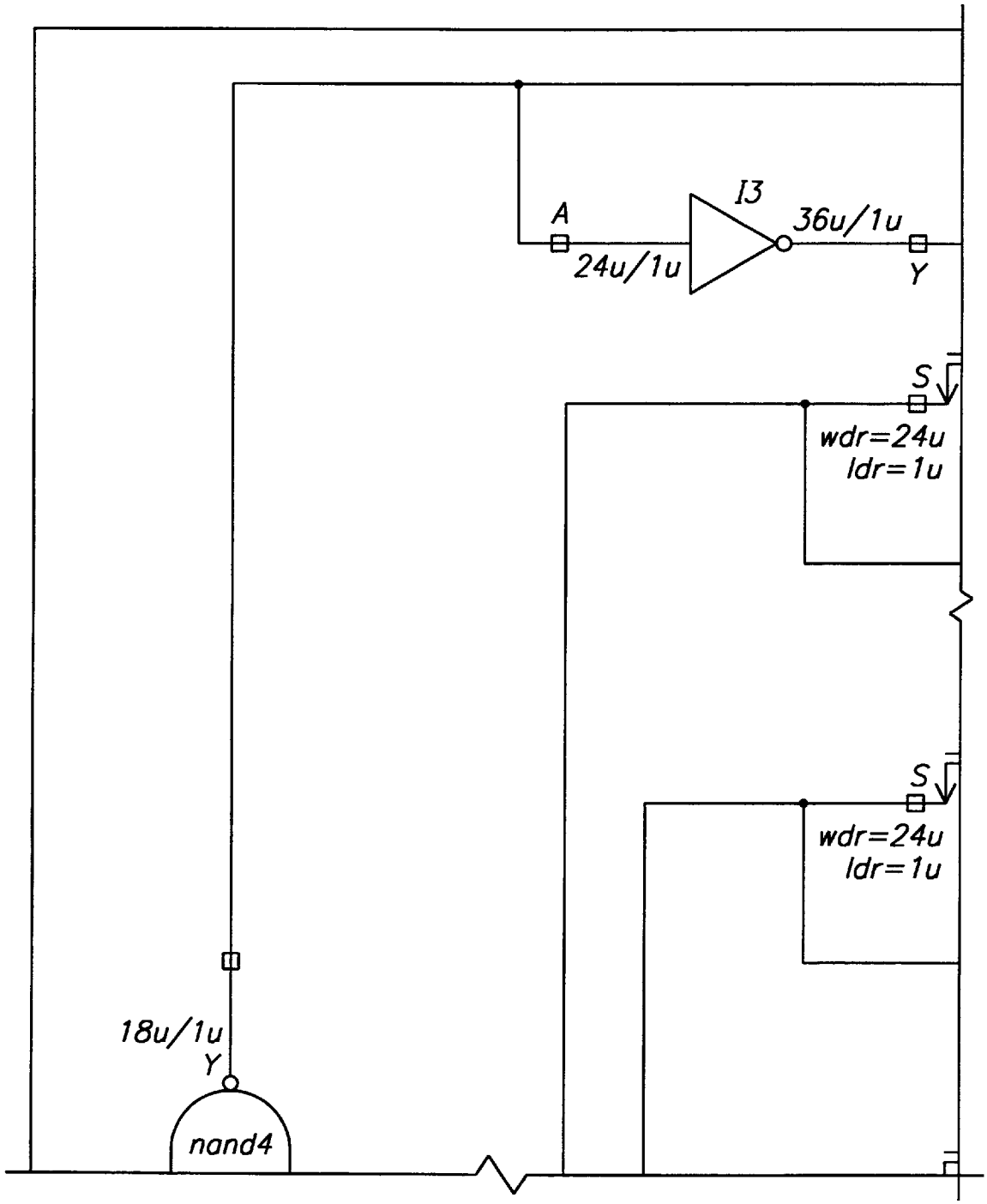


Fig 1.0301AA

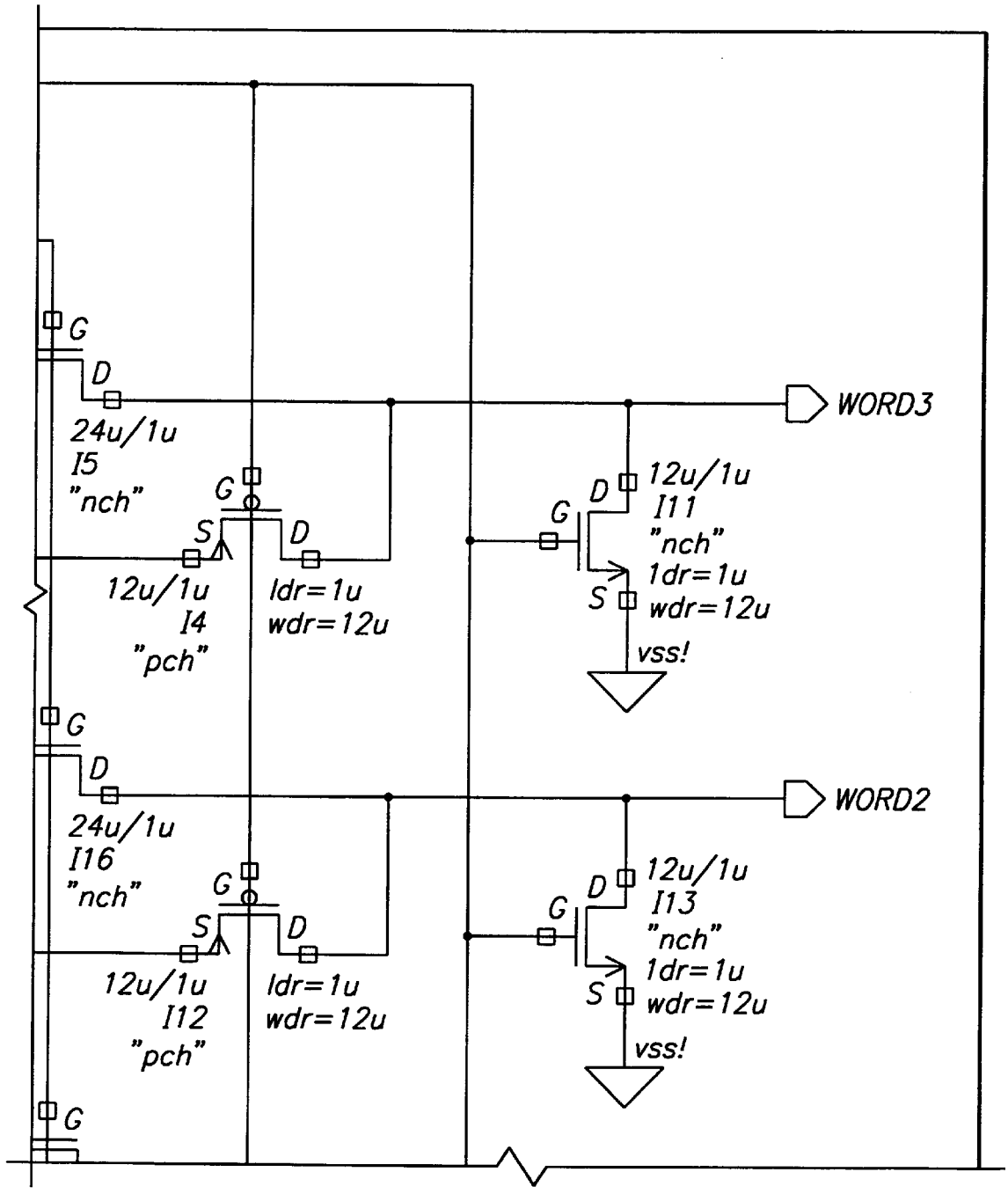

G
D
24u/1u
I5
"nch"
G
S
D
12u/1u
I4
"pch"
ldr=1u
wdr=12u
WORD3
G
D
12u/1u
I11
"nch"
1dr=1u
S
wdr=12u
vss!
G
D
24u/1u
I16
"nch"
G
S
D
12u/1u
I12
"pch"
ldr=1u
wdr=12u
WORD2
G
D
12u/1u
I13
"nch"
1dr=1u
S
wdr=12u
vss!
G

Fig 1.0301AB

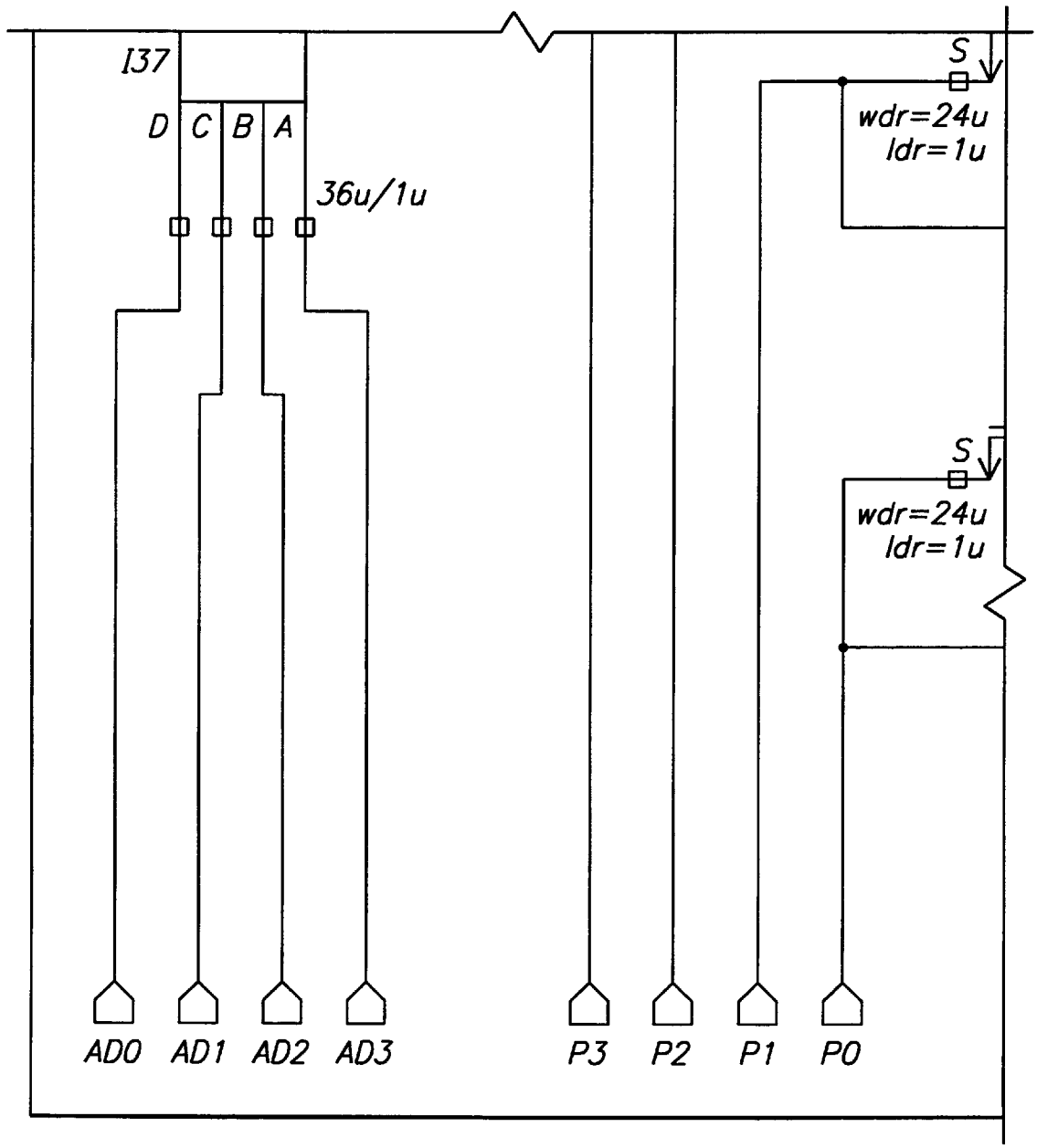

I37
D
C
B
A
36u/1u
S
wdr=24u
ldr=1u
S
wdr=24u
ldr=1u
AD0
AD1
AD2
AD3
P3
P2
P1
P0

Fig 1.0301BA

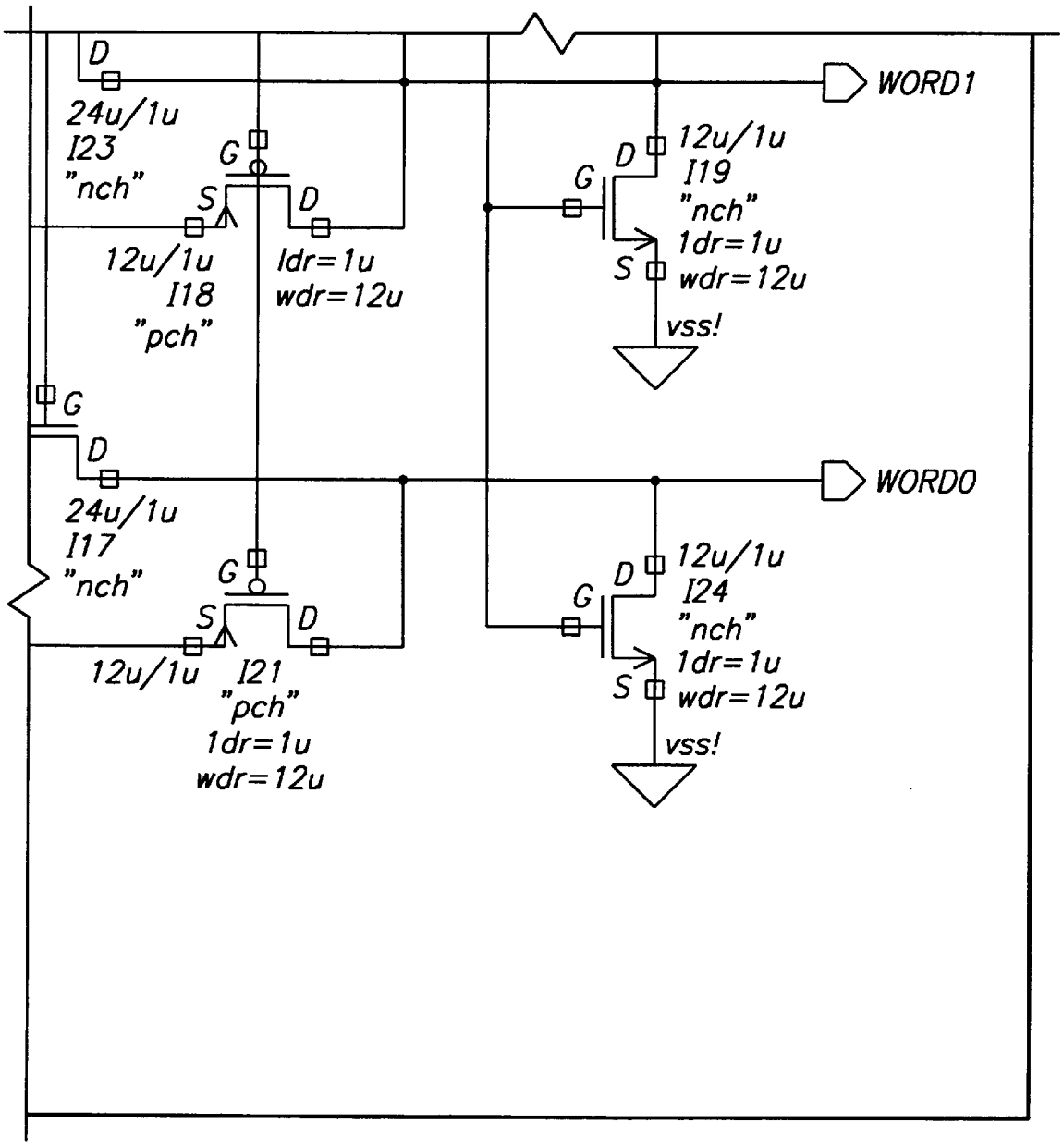

D
24u/1u
I23
"nch"
G
S
D
12u/1u
I18
"pch"
ldr=1u
wdr=12u
WORD1
12u/1u
I19
"nch"
1dr=1u
wdr=12u
vss!
G
D
24u/1u
I17
"nch"
WORD0
12u/1u
I21
"pch"
1dr=1u
wdr=12u
12u/1u
I24
"nch"
1dr=1u
wdr=12u
vss!

Fig 1.0301BB

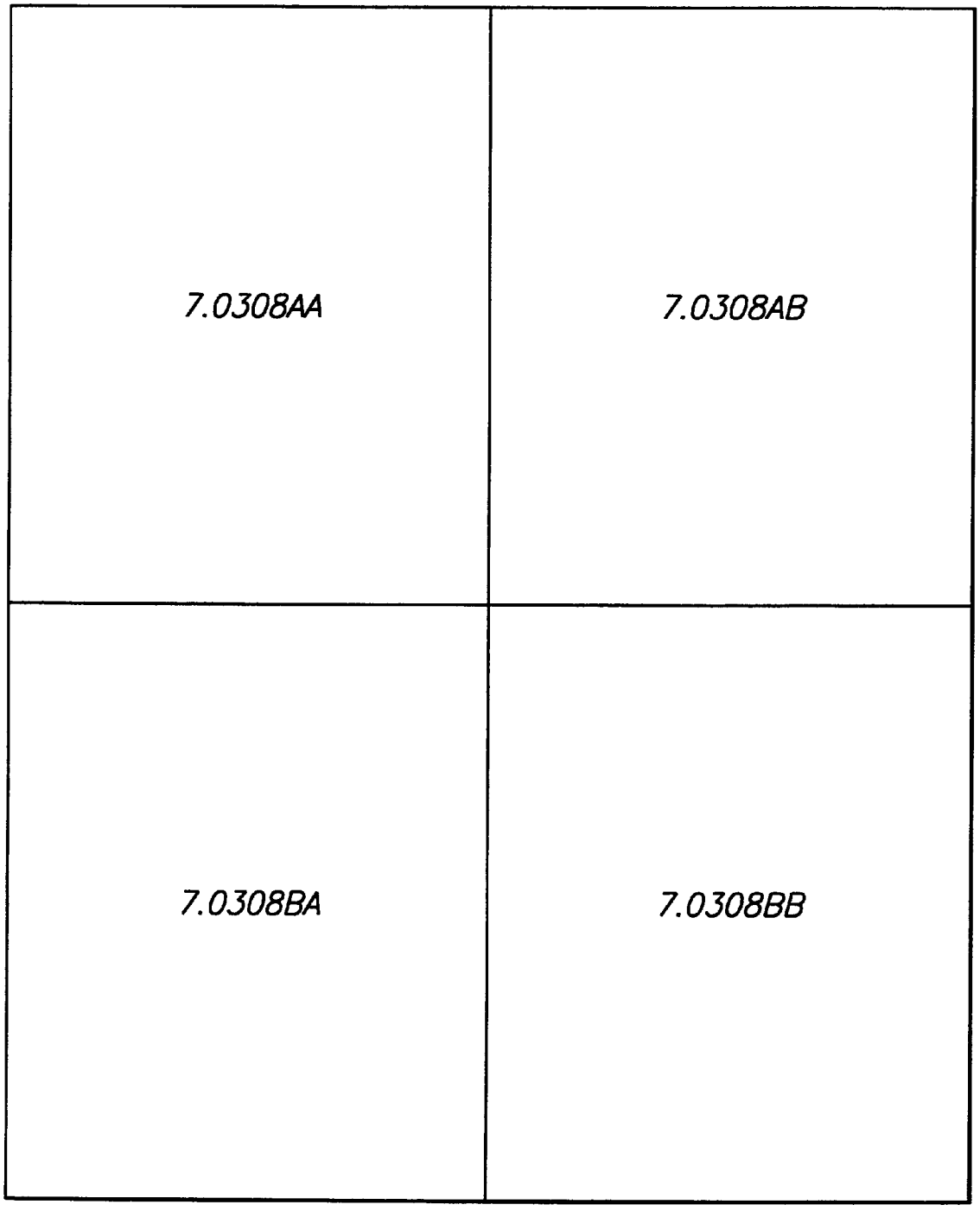


Fig 7.0308B

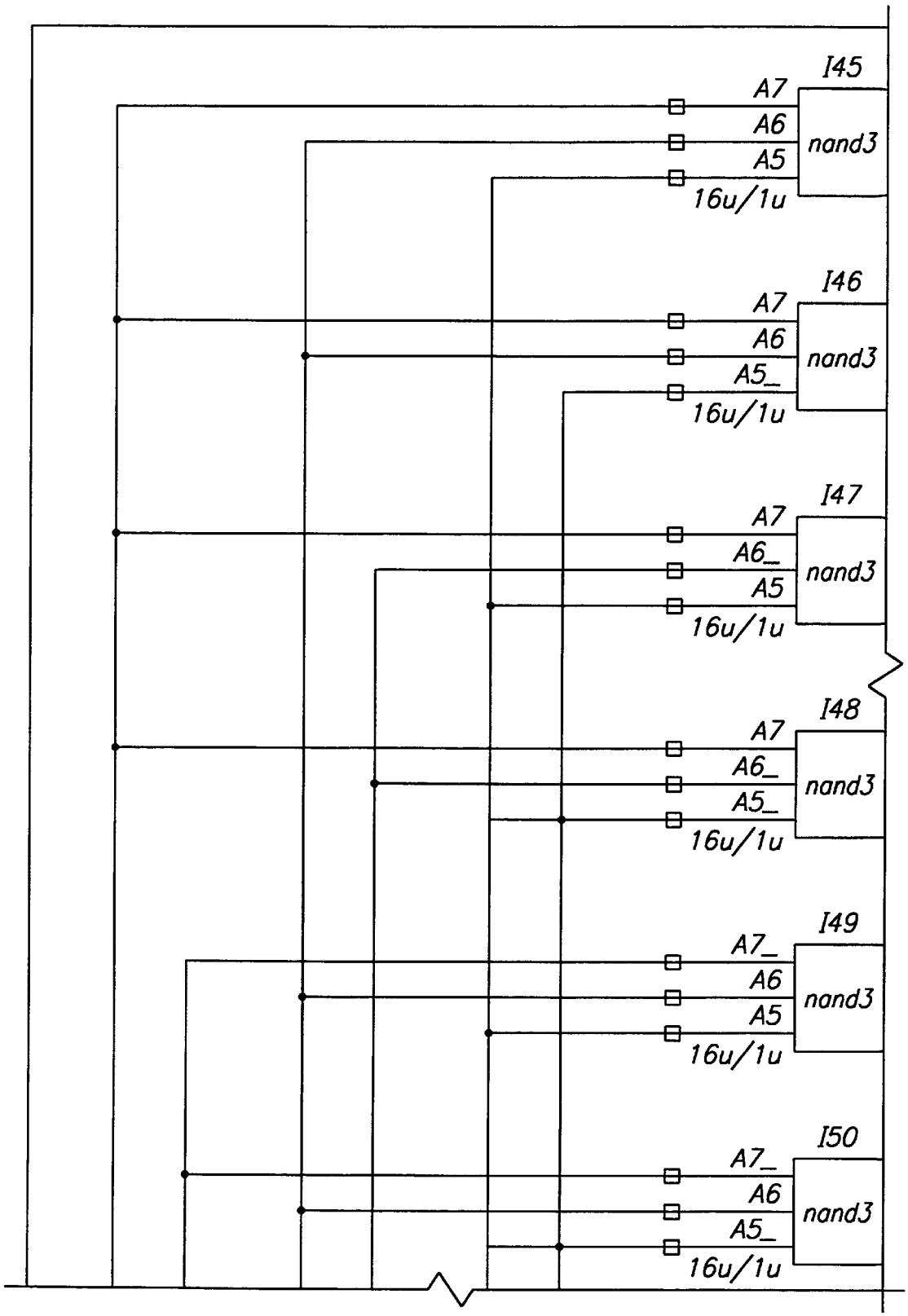

I45
A7
A6
A5
nand3
16u/1u
I46
A7
A6
A5_
nand3
16u/1u
I47
A7
A6_
A5
nand3
16u/1u
I48
A7
A6_
A5_
nand3
16u/1u
I49
A7_
A6
A5
nand3
16u/1u
I50
A7_
A6
A5_
nand3
16u/1u

Fig 1.0308AA

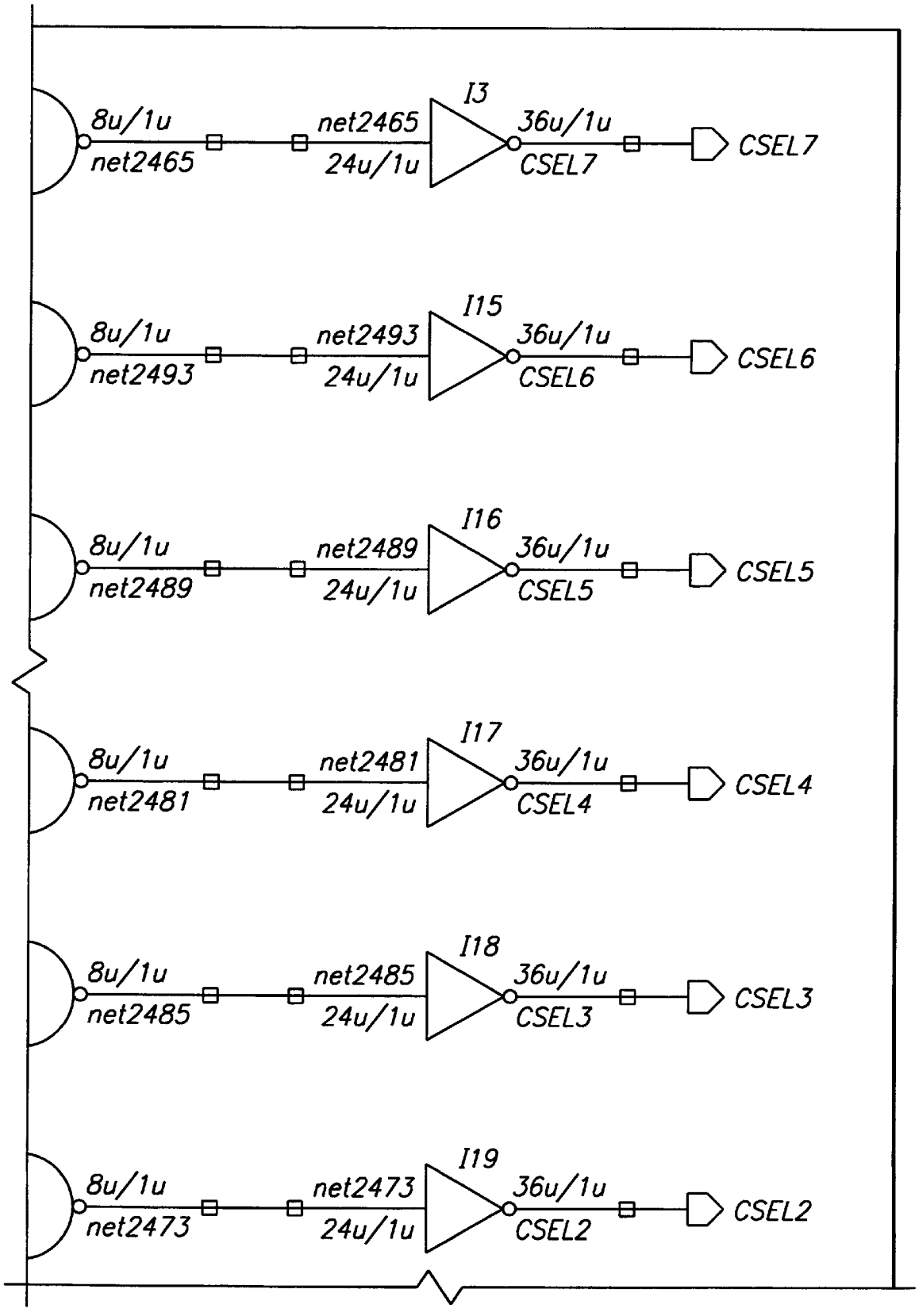

I3
8u/1u
net2465
net2465
24u/1u
36u/1u
CSEL7
CSEL7
I15
8u/1u
net2493
net2493
24u/1u
36u/1u
CSEL6
CSEL6
I16
8u/1u
net2489
net2489
24u/1u
36u/1u
CSEL5
CSEL5
I17
8u/1u
net2481
net2481
24u/1u
36u/1u
CSEL4
CSEL4
I18
8u/1u
net2485
net2485
24u/1u
36u/1u
CSEL3
CSEL3
I19
8u/1u
net2473
net2473
24u/1u
36u/1u
CSEL2
CSEL2

Fig 1,030,848

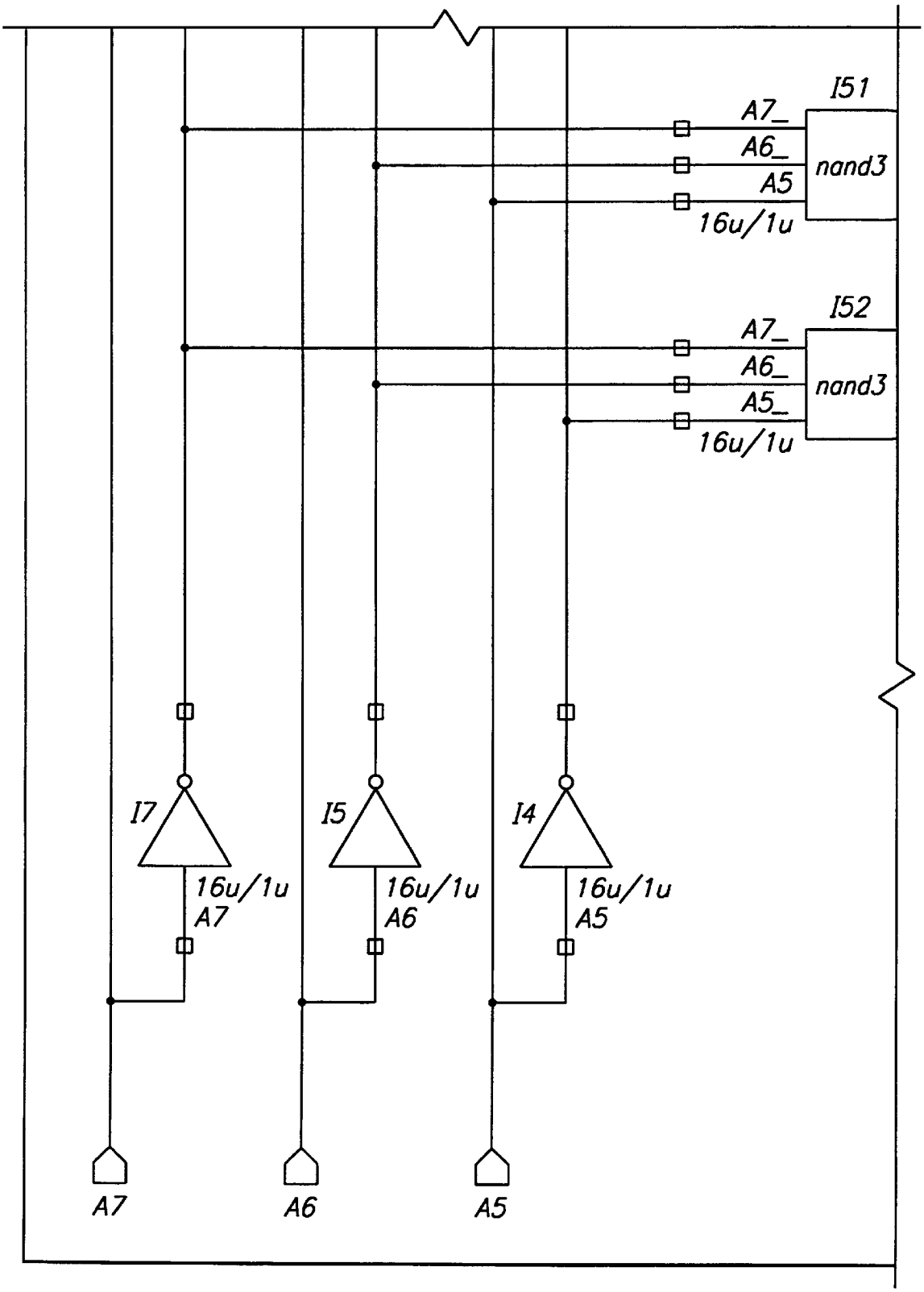

I51
A7_
A6_
A5
nand3
16u/1u
I52
A7_
A6_
A5_
nand3
16u/1u
I7
16u/1u
A7
I5
16u/1u
A6
I4
16u/1u
A5
A7
A6
A5

Fig 1.0308BA

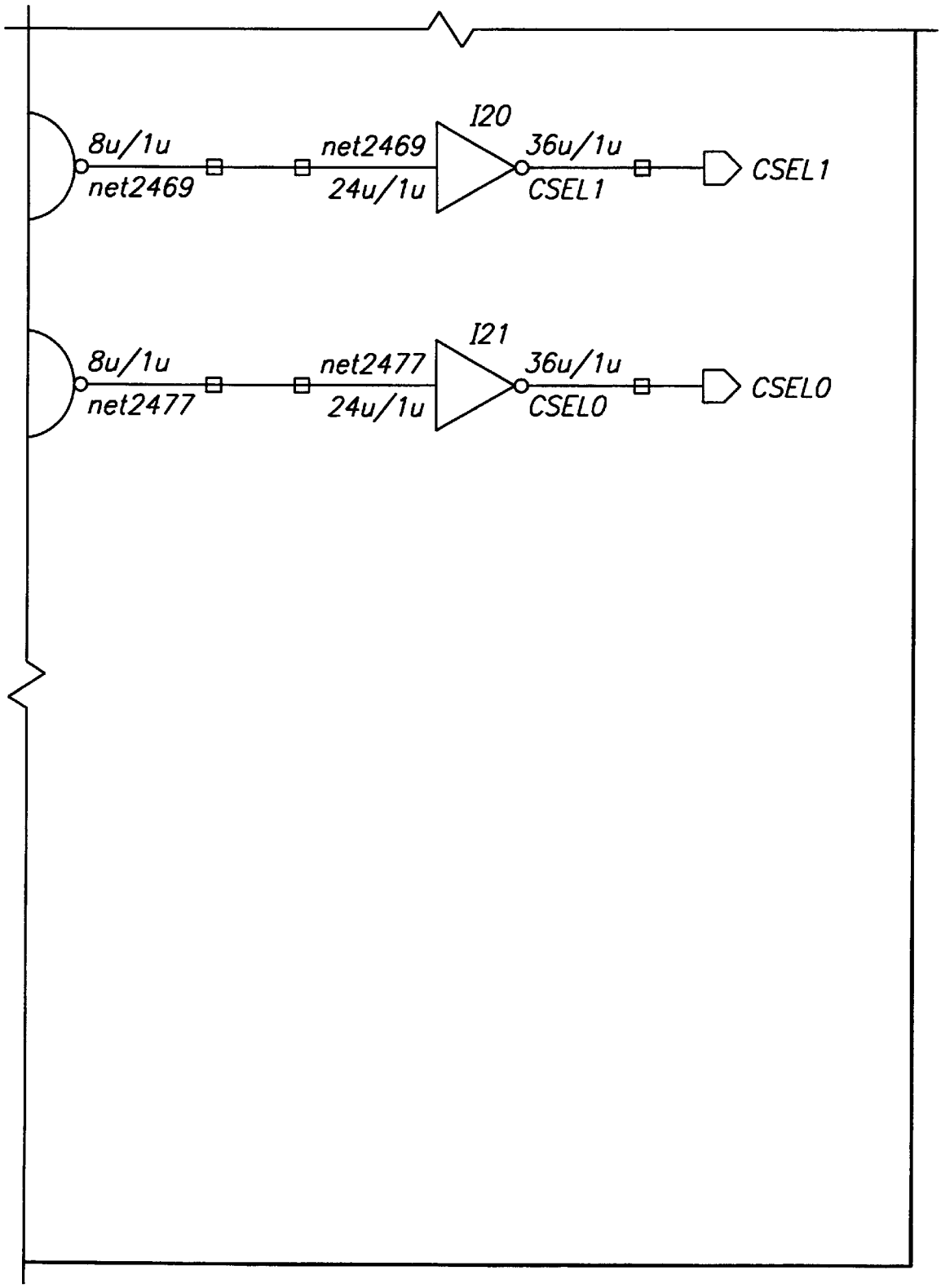

I20
8u/1u
net2469
net2469
24u/1u
36u/1u
CSEL1
CSEL1
I21
8u/1u
net2477
net2477
24u/1u
36u/1u
CSEL0
CSEL0

FIG 1.0300

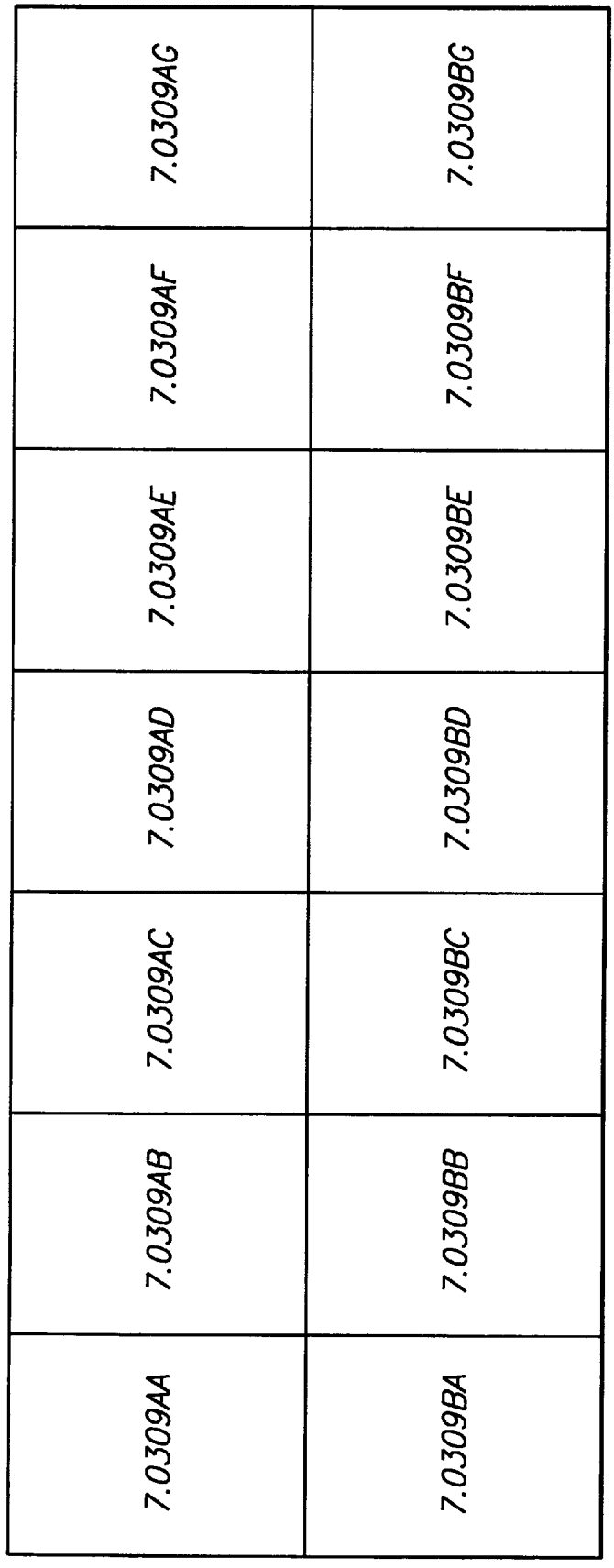

7.0309AA
7.0309AB
7.0309AC
7.0309AD
7.0309AE
7.0309AF
7.0309AG
7.0309BA
7.0309BB
7.0309BC
7.0309BD
7.0309BE
7.0309BF
7.0309BG

FIG. 7.0309E

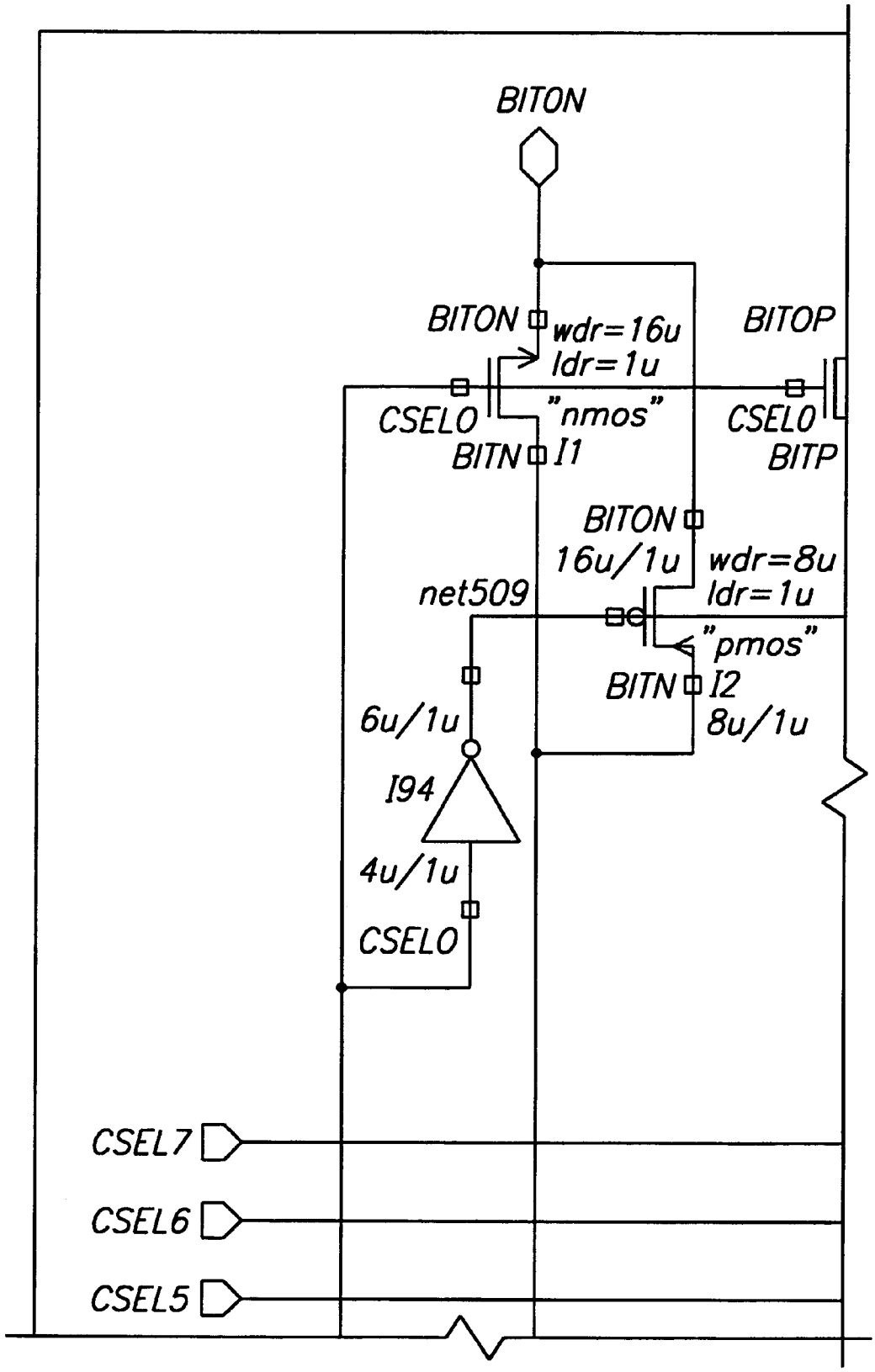


Fig 1.03099AA

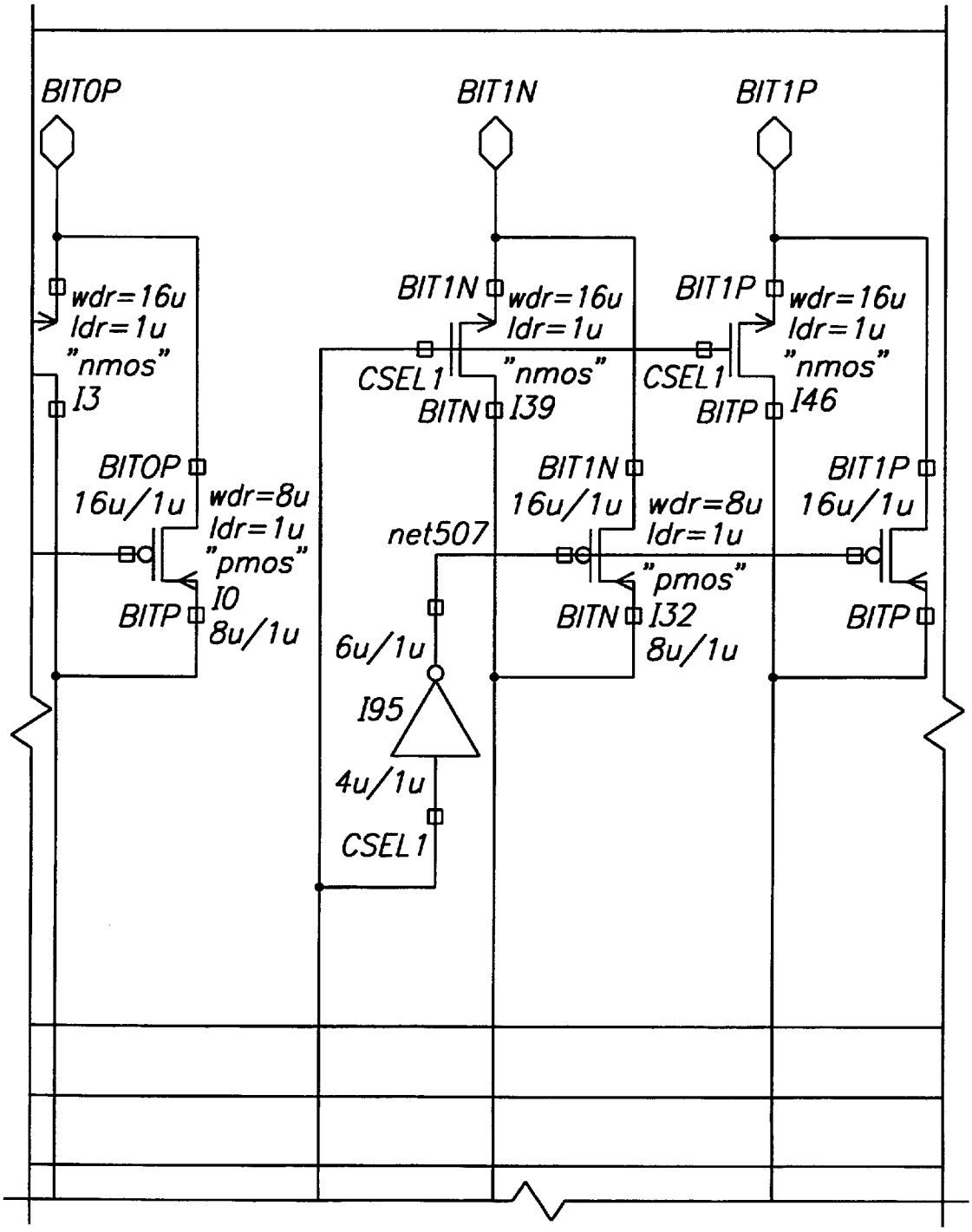


Fig 1.03095AB

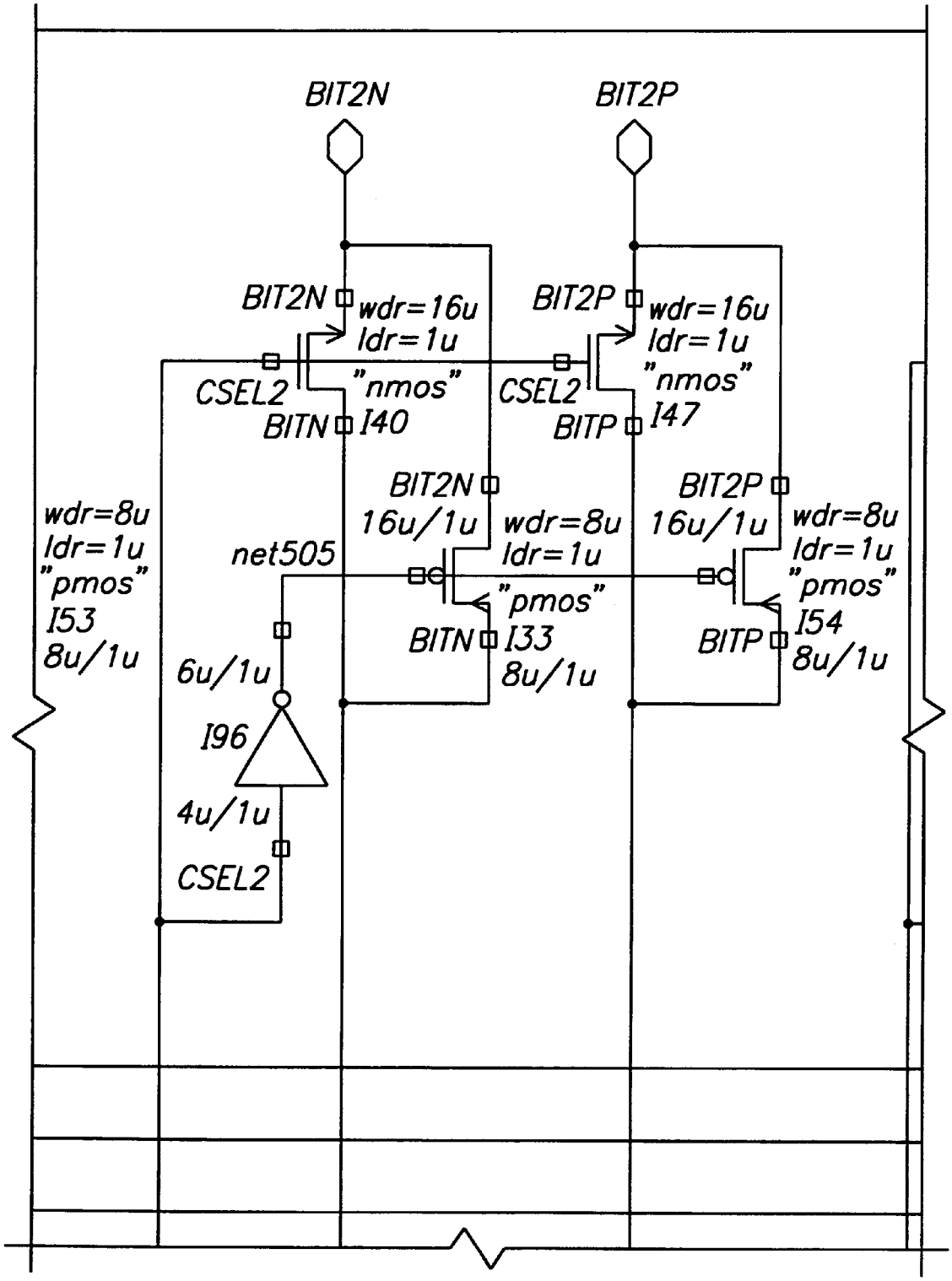

BIT2N
BIT2P
BIT2N
wdr=16u
ldr=1u
"nmos"
I40
CSEL2
BITN
BIT2P
wdr=16u
ldr=1u
"nmos"
I47
CSEL2
BITP
wdr=8u
ldr=1u
"pmos"
I53
8u/1u
net505
BIT2N
16u/1u
wdr=8u
ldr=1u
"pmos"
I33
8u/1u
BITN
BIT2P
16u/1u
wdr=8u
ldr=1u
"pmos"
I54
8u/1u
BITP
6u/1u
I96
4u/1u
CSEL2

Fig 1.0309AC

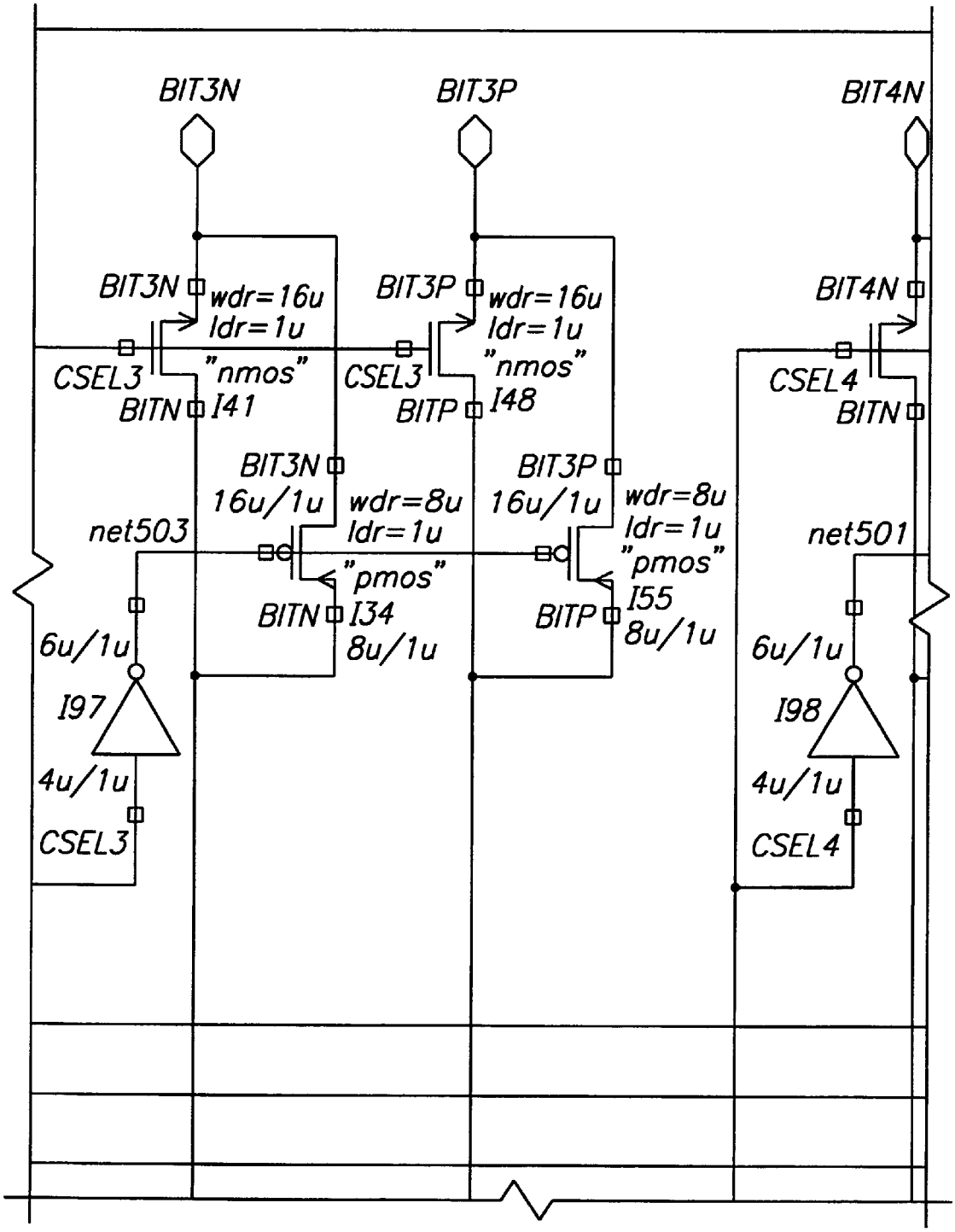


Fig 1.03095AD

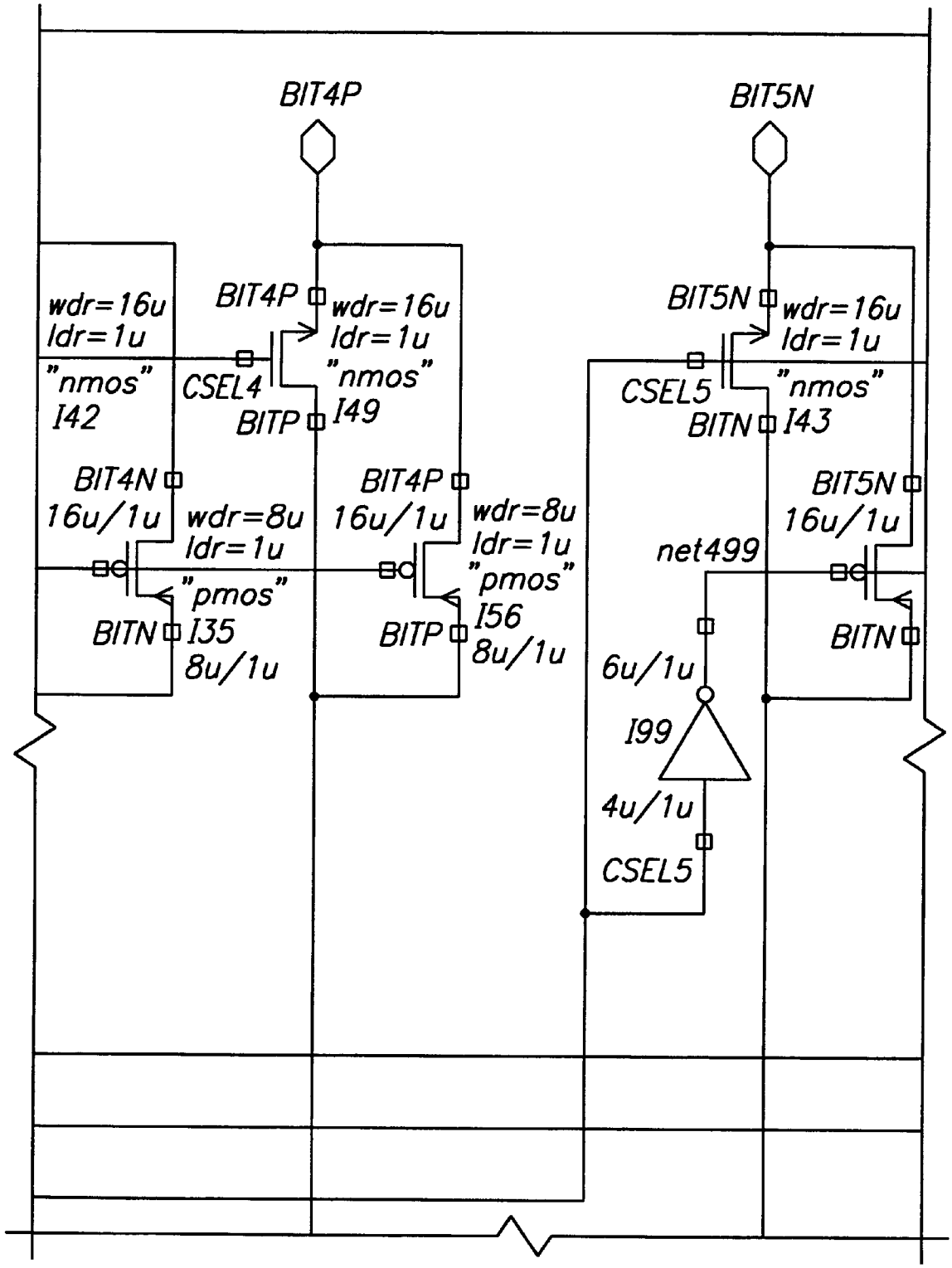


Fig 1.03009AE

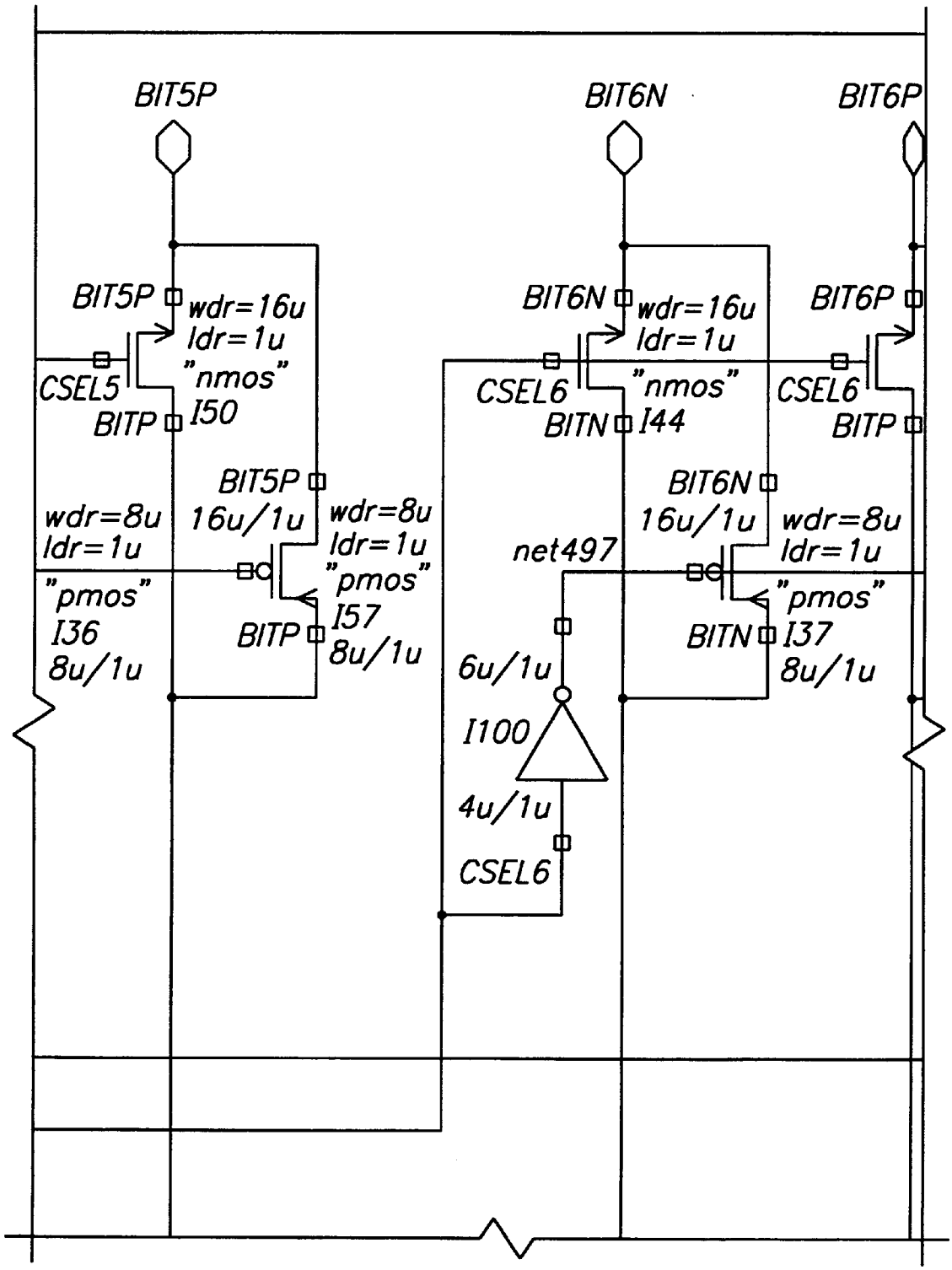

BIT5P
BIT6N
BIT6P
BIT5P
wdr=16u
ldr=1u
"nmos"
I50
CSEL5
BITP
BIT6N
wdr=16u
ldr=1u
"nmos"
I44
CSEL6
BITN
BIT6P
CSEL6
BITP
BIT5P
16u/1u
wdr=8u
ldr=1u
"pmos"
I57
8u/1u
BITP
wdr=8u
ldr=1u
"pmos"
I36
8u/1u
BIT6N
16u/1u
wdr=8u
ldr=1u
"pmos"
I37
8u/1u
BITN
net497
6u/1u
I100
4u/1u
CSEL6

Fig 1.0309AF

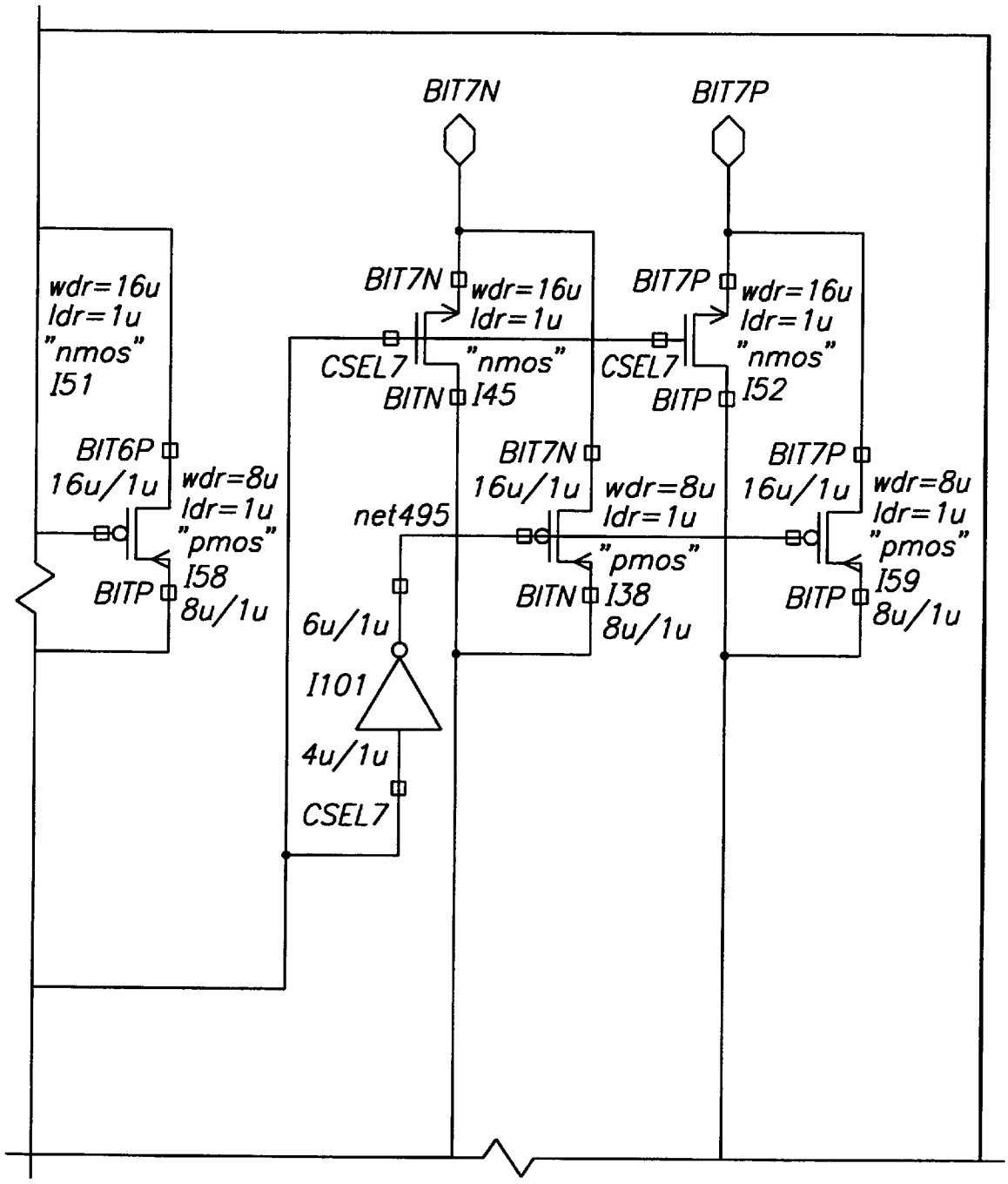

BIT7N
BIT7P
wdr=16u
ldr=1u
"nmos"
I51
BIT7N
wdr=16u
ldr=1u
"nmos"
I45
CSEL7
BITN
BIT7P
wdr=16u
ldr=1u
"nmos"
I52
CSEL7
BITP
BIT6P
16u/1u
wdr=8u
ldr=1u
"pmos"
I58
8u/1u
BITP
BIT7N
16u/1u
wdr=8u
ldr=1u
"pmos"
I38
8u/1u
BITN
net495
BIT7P
16u/1u
wdr=8u
ldr=1u
"pmos"
I59
8u/1u
BITP
6u/1u
I101
4u/1u
CSEL7

Fig 1.0309A6

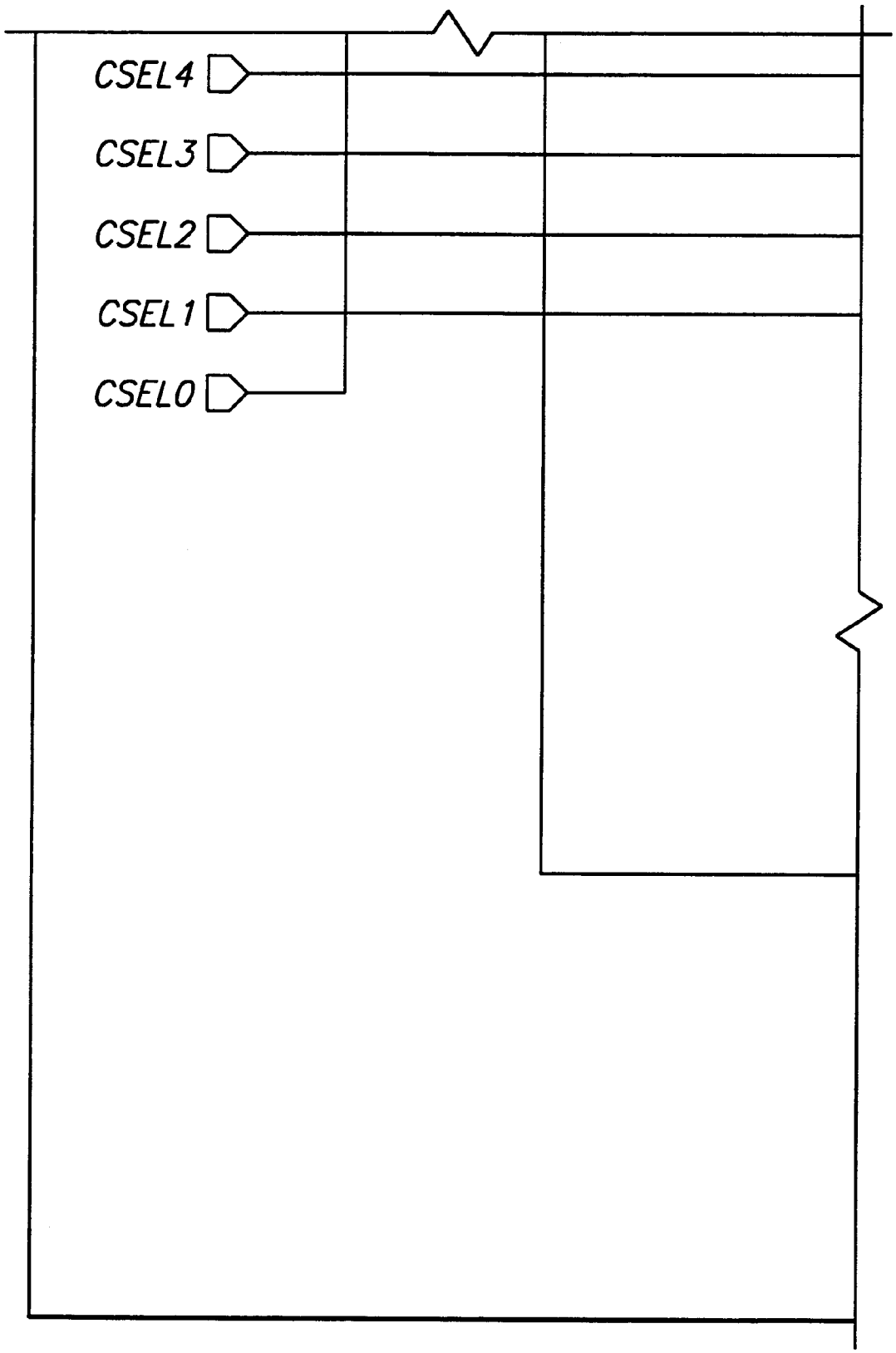


Fig 1.0309BA

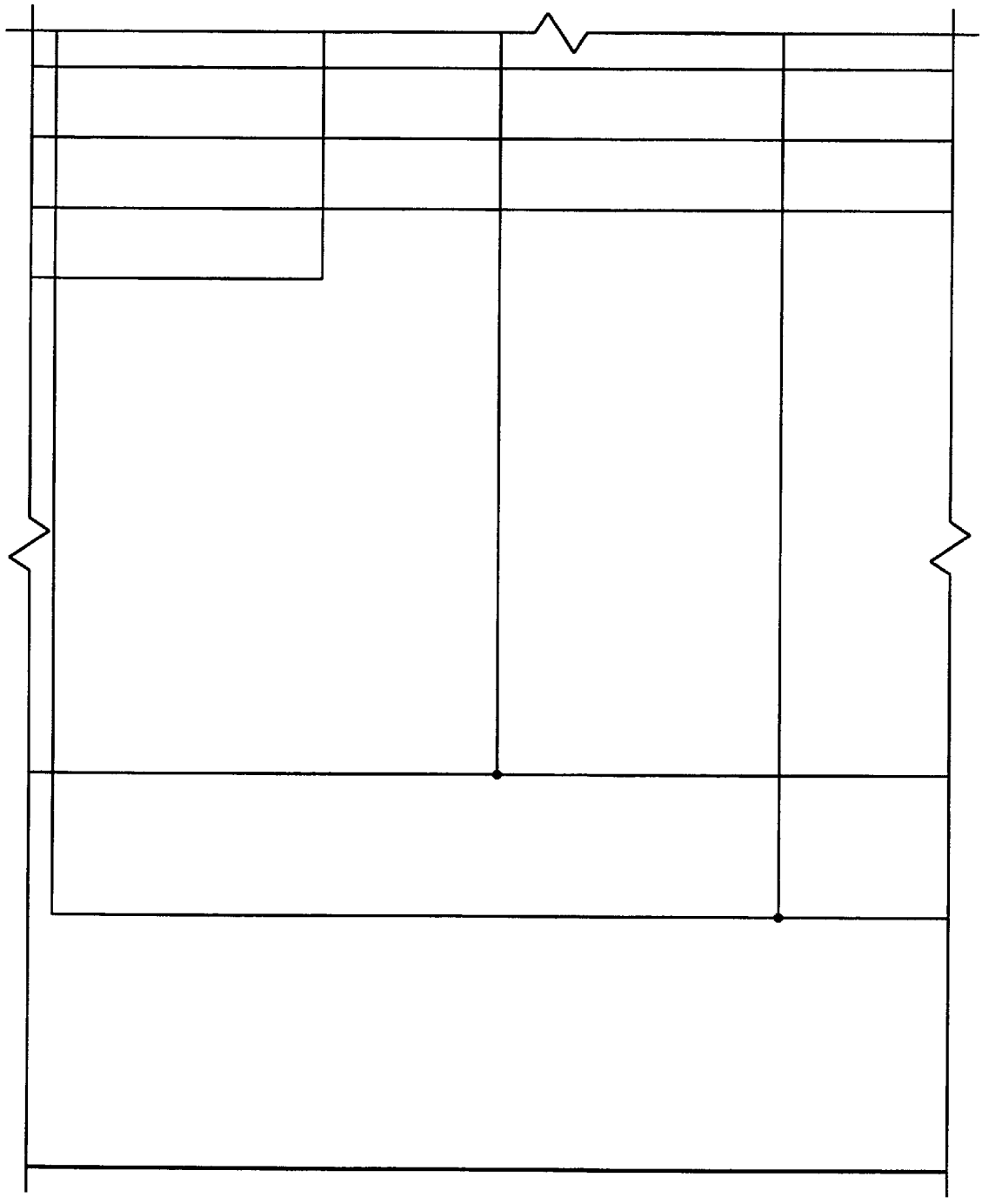


Fig 1.0300BB

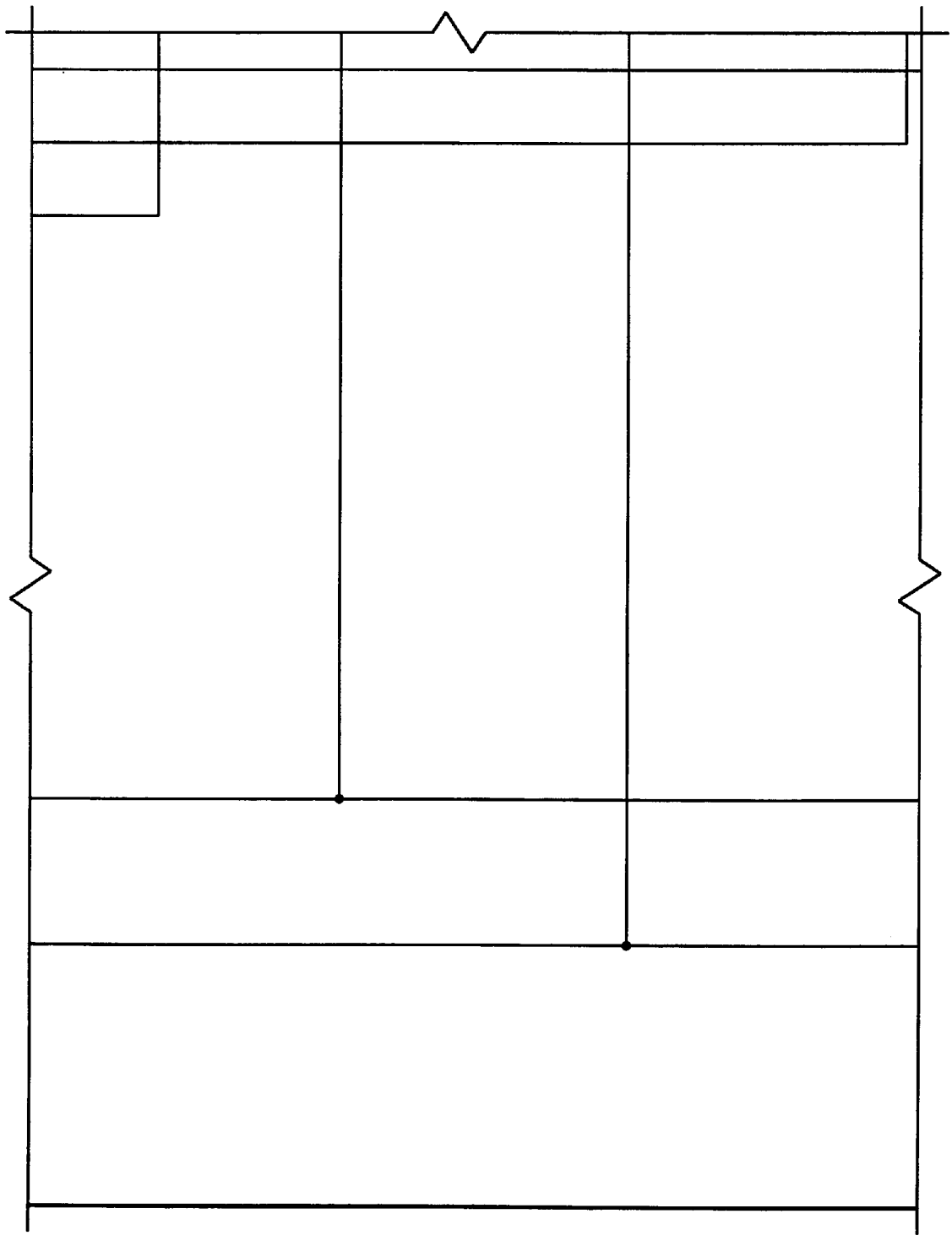


Fig 1.0309BC

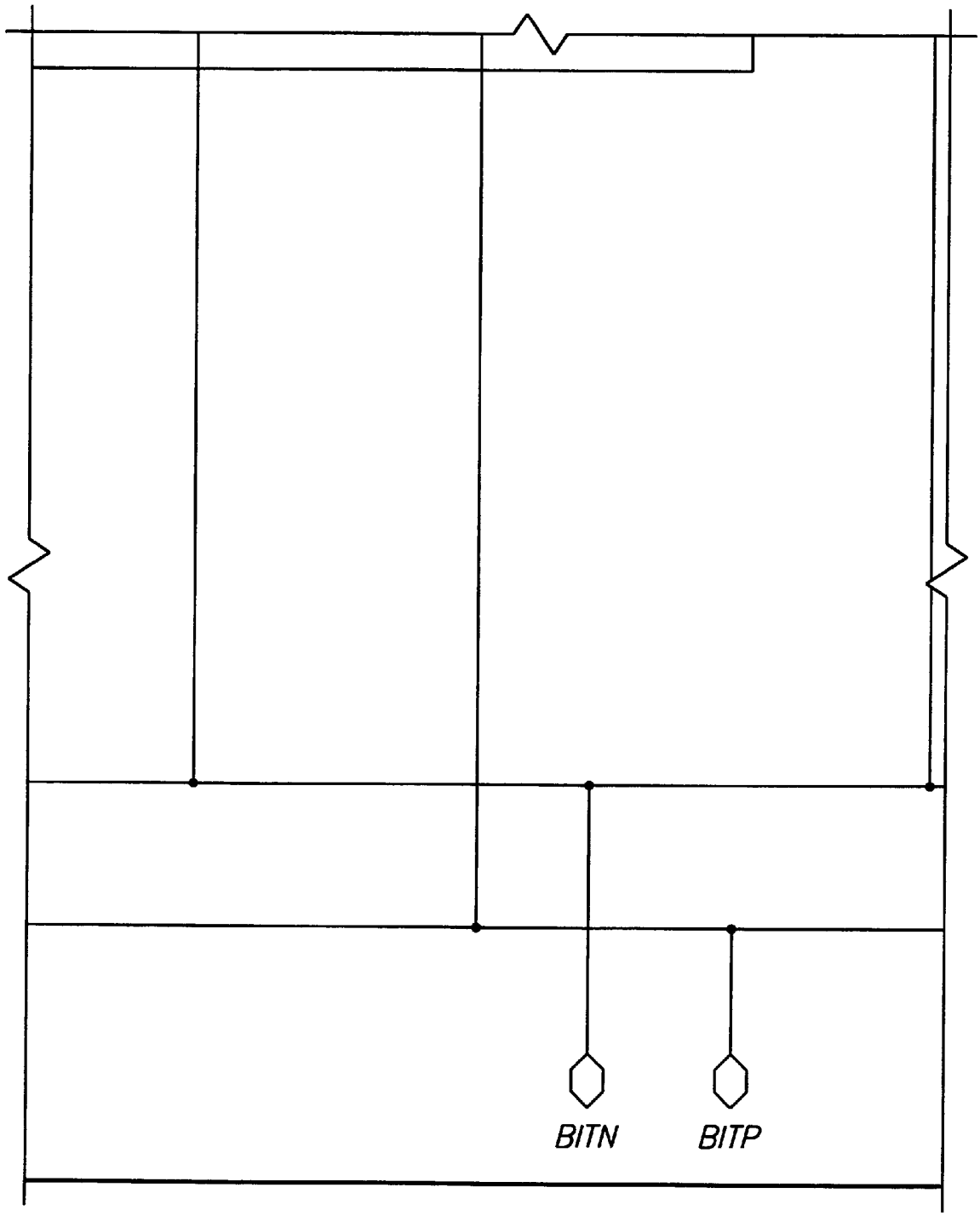


Fig 1.0309BD

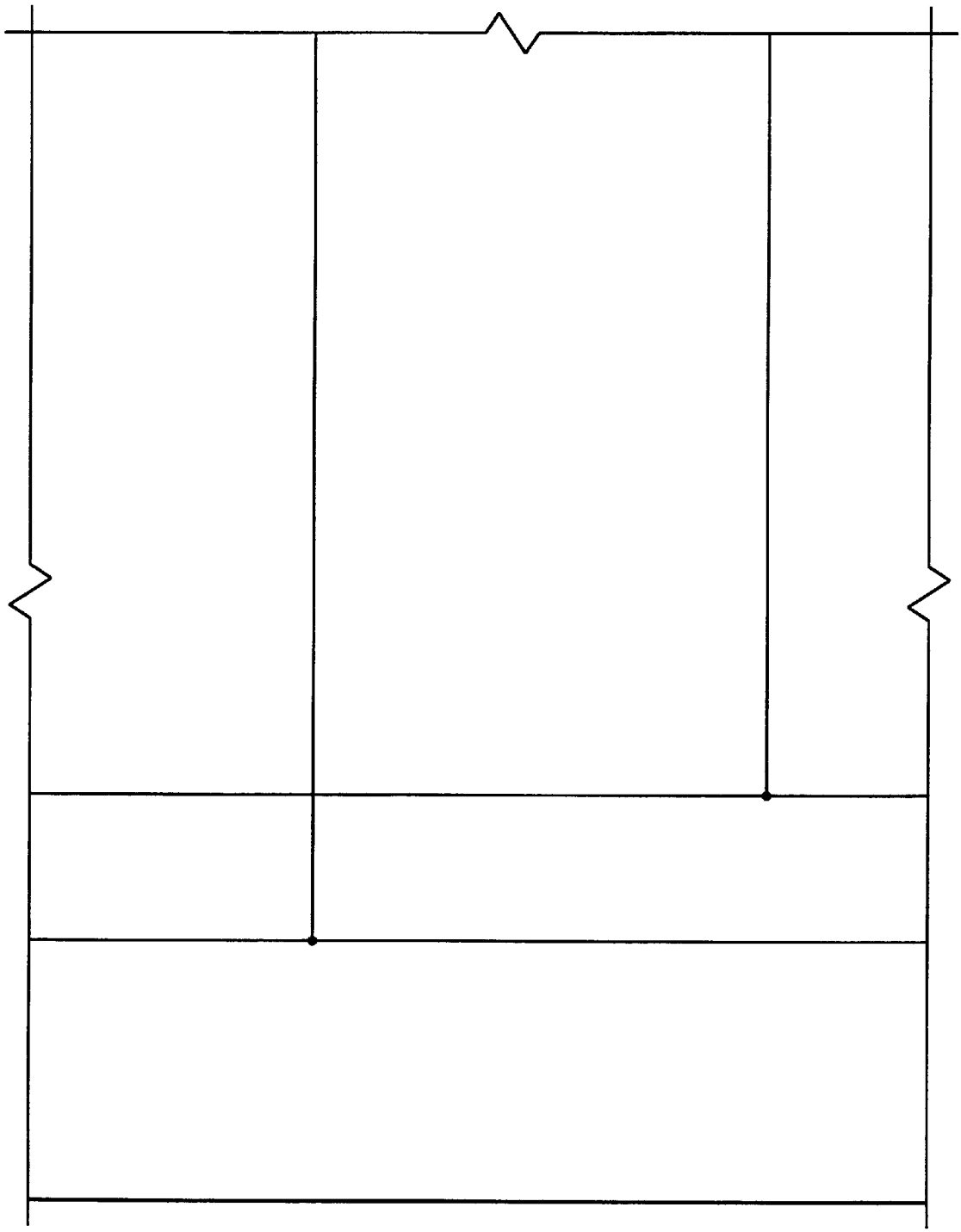


Fig 1.03098E

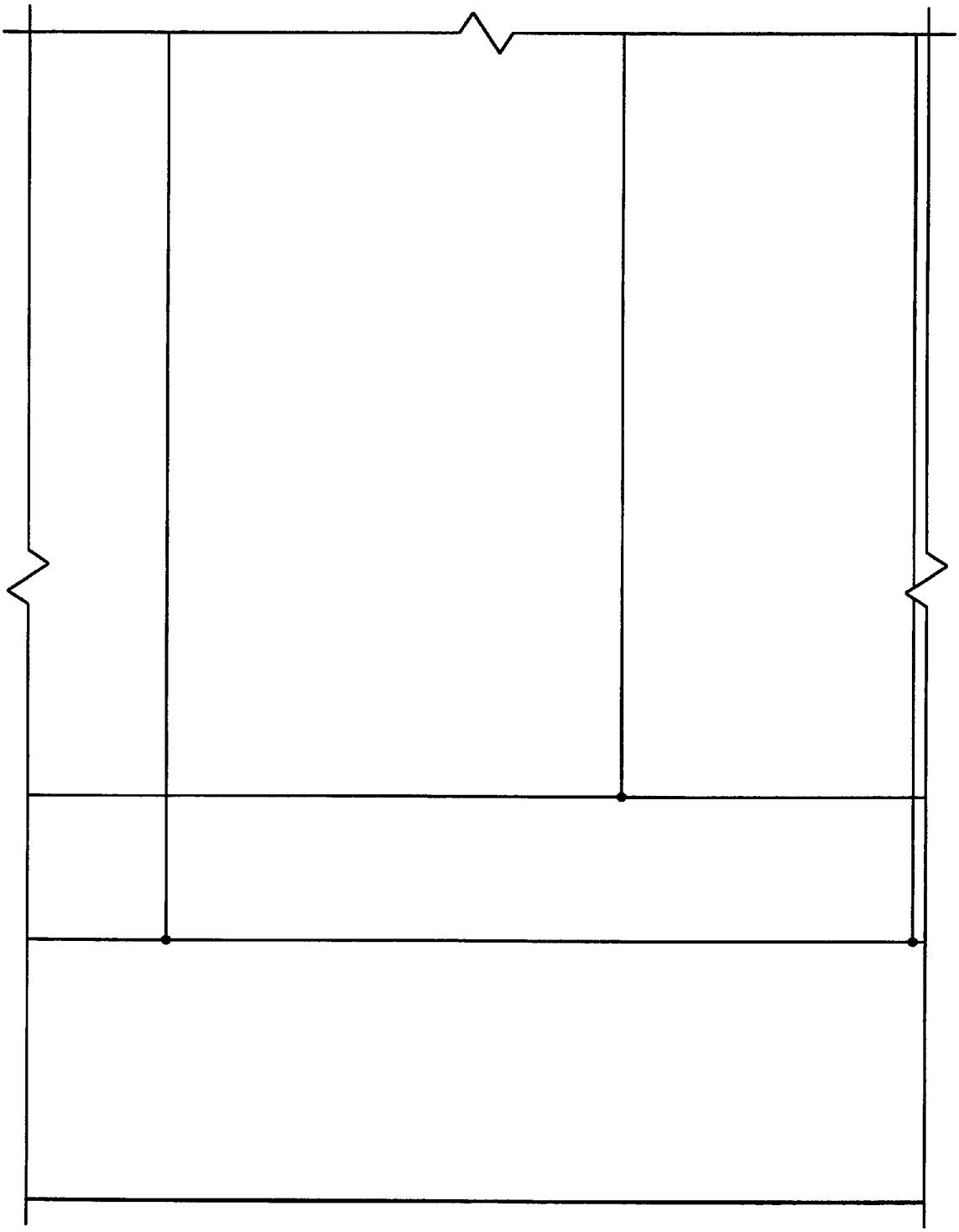


FIG 1.03098F

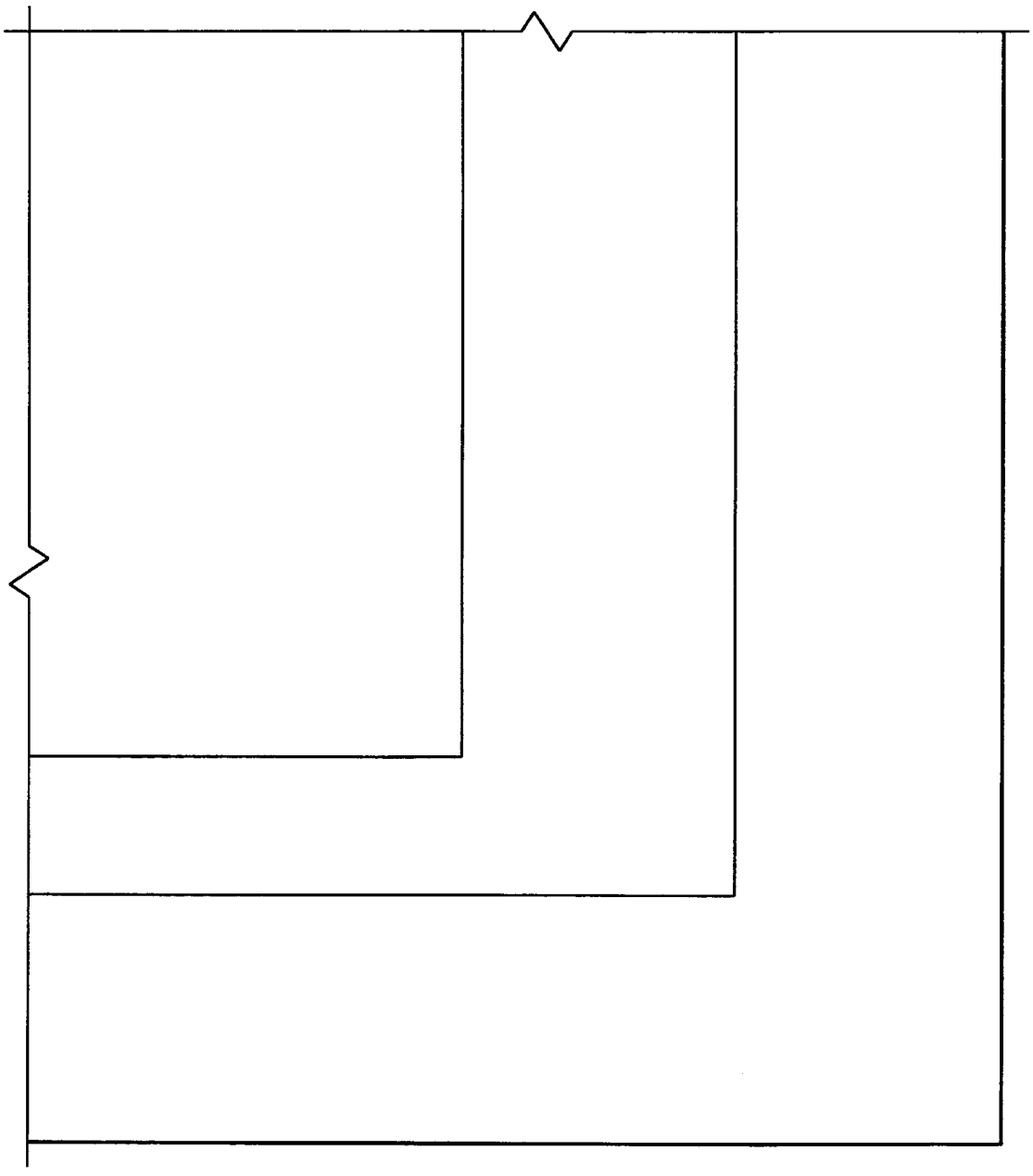


Fig 1.030986

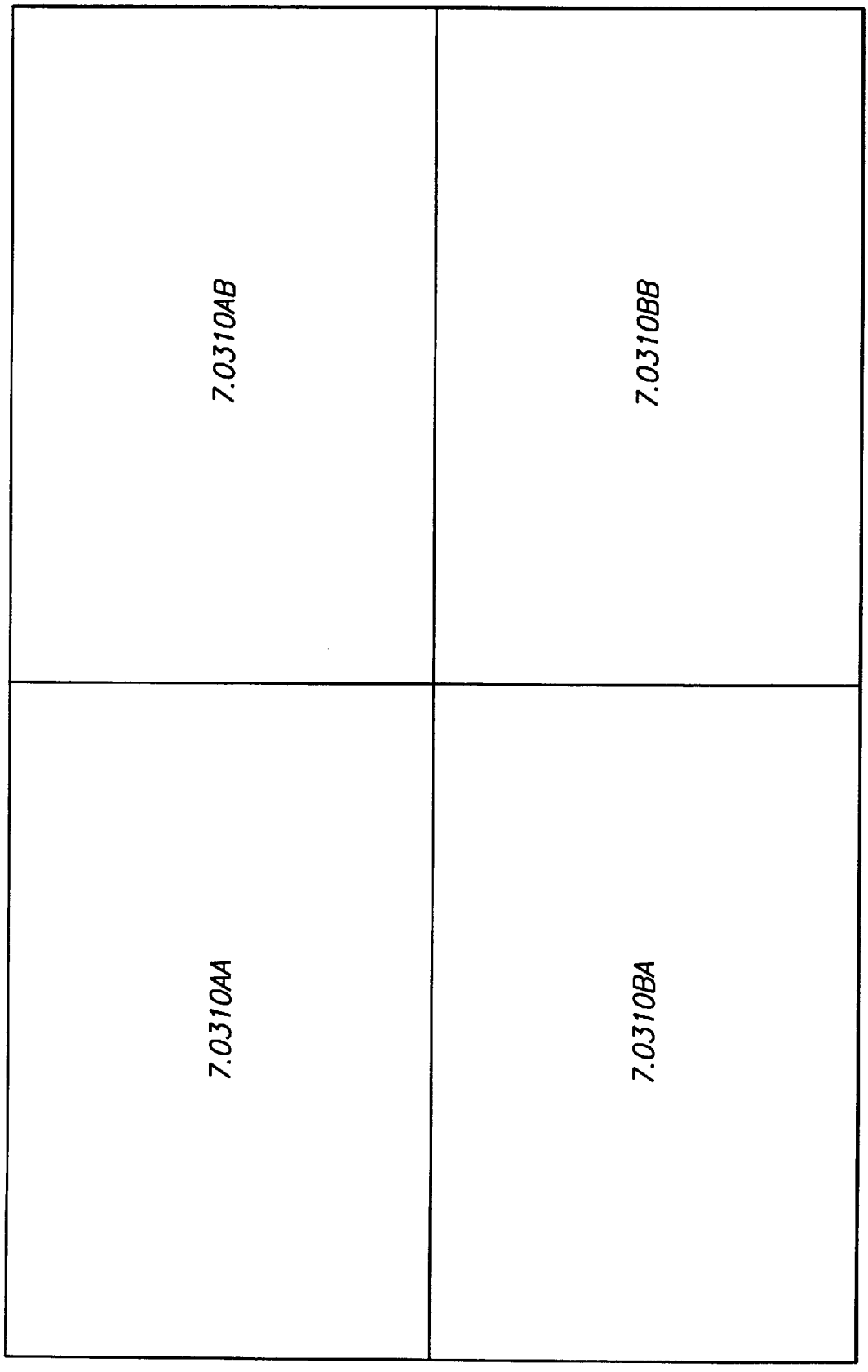


FIG. 7.0310

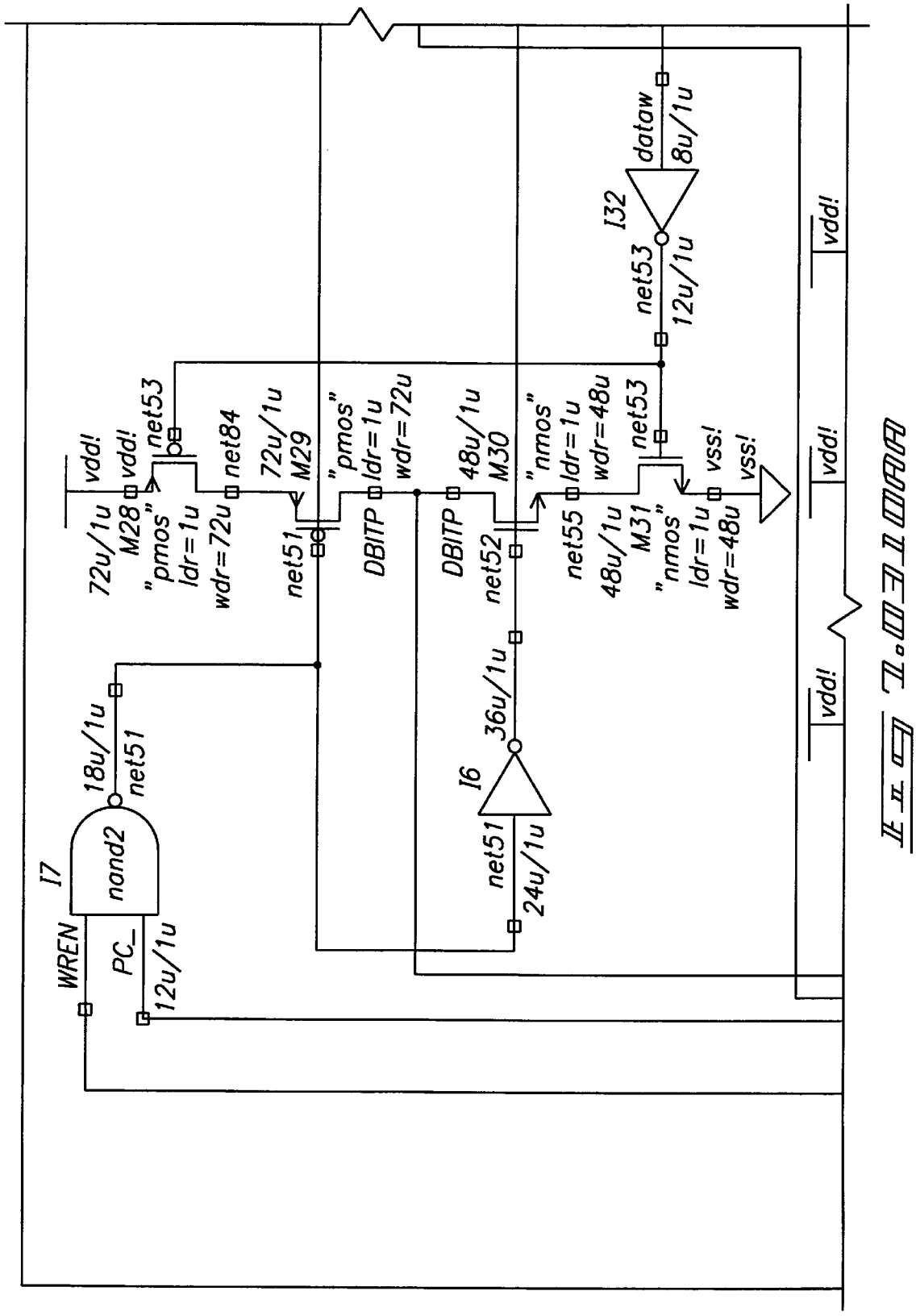
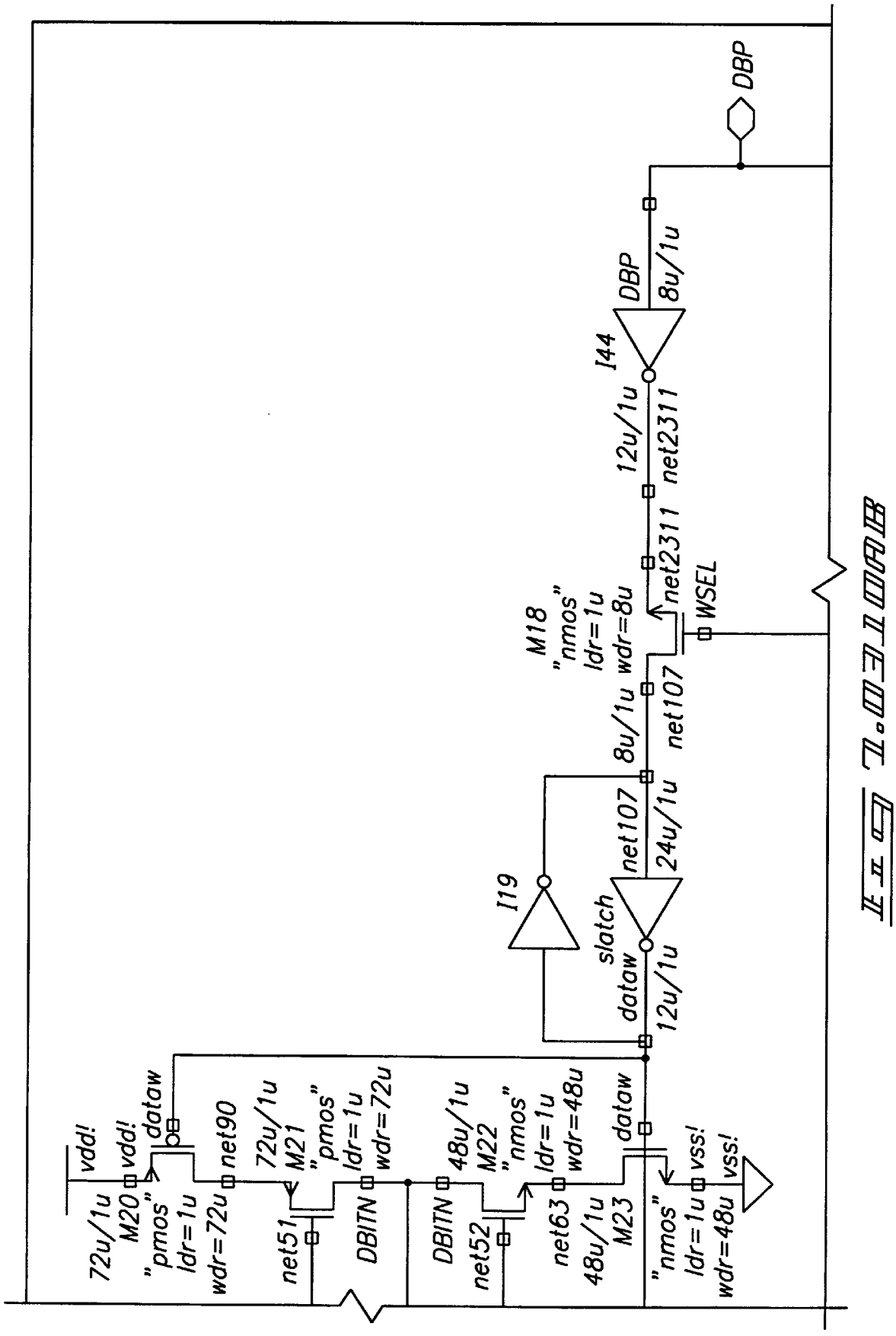

I7
nand2
18u/1u
net51
WREN
PC_
12u/1u
I6
36u/1u
net51
24u/1u
I32
datax
8u/1u
net53
12u/1u
vdd!
vss!
M28
"pmos"
ldr=1u
wdr=72u
72u/1u
net84
M29
"pmos"
ldr=1u
wdr=72u
72u/1u
DBITP
net51
M30
"nmos"
ldr=1u
wdr=48u
48u/1u
DBITP
net52
net55
M31
"nmos"
ldr=1u
wdr=48u
48u/1u
net53
vss!

FIG. 1E


DBP
I44
DBP
8u/1u
12u/1u
net2311
net2311
M18
"nmos"
ldr=1u
wdr=8u
WSEL
8u/1u
net107
I19
net107
24u/1u
slatch
dataw
12u/1u
72u/1u
M20
"pmos"
ldr=1u
wdr=72u
vdd!
vdd!
dataw
net90
72u/1u
M21
"pmos"
ldr=1u
wdr=72u
net51
DBITN
48u/1u
M22
"nmos"
ldr=1u
wdr=48u
DBITN
net52
net63
48u/1u
M23
dataw
"nmos"
ldr=1u
wdr=48u
vss!
vss!

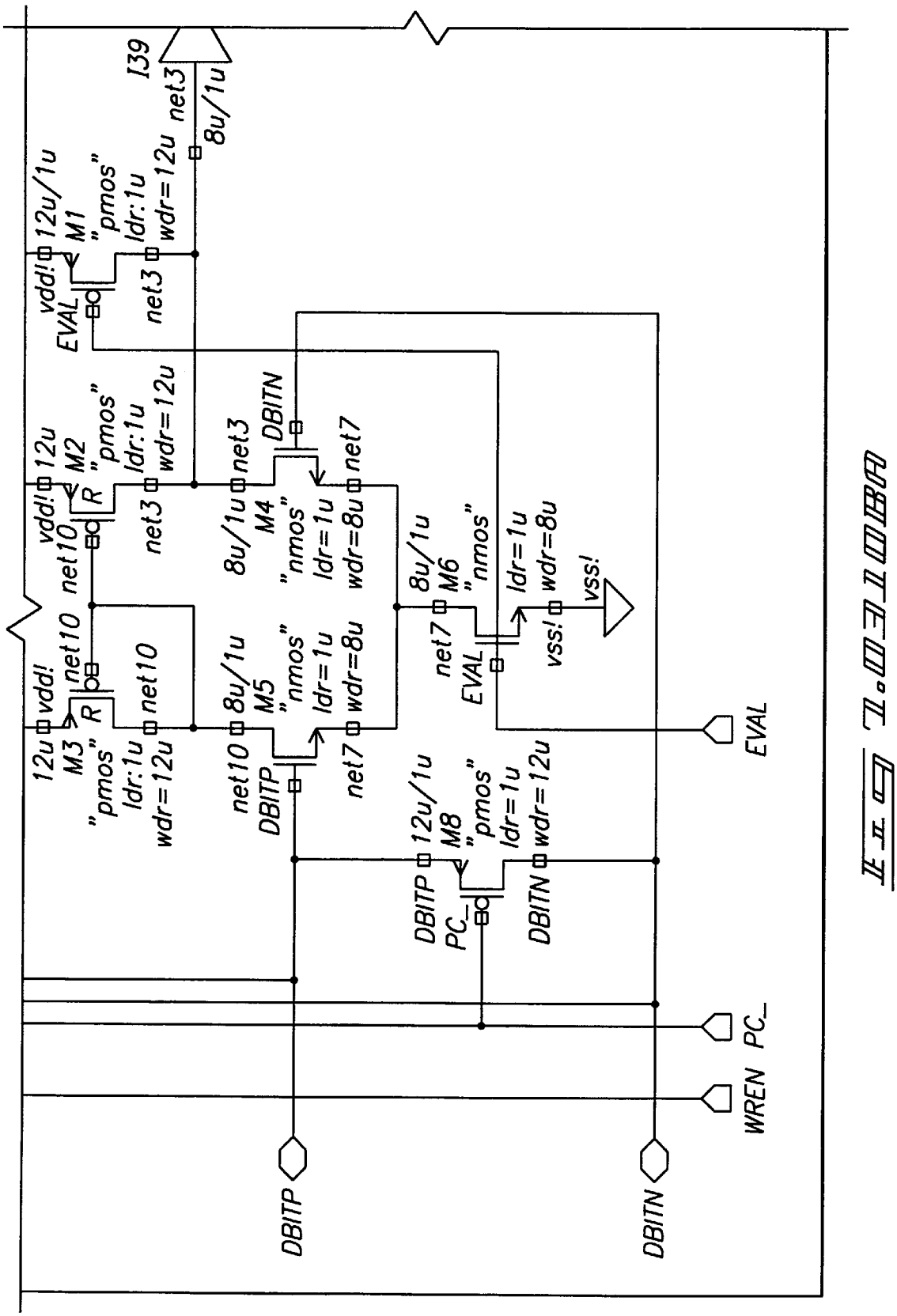

I39
net3
8u/1u
12u/1u
M1
"pmos"
ldr:1u
wdr=12u
vdd!
EVAL
net3
12u
M2
"pmos"
ldr:1u
wdr=12u
vdd!
net10
R
net3
net3
DBITN
8u/1u
M4
"nmos"
ldr=1u
wdr=8u
net7
8u/1u
M6
"nmos"
ldr=1u
wdr=8u
net7
EVAL
vss!
vss!
vdd!
net10
R
net10
12u
M3
"pmos"
ldr:1u
wdr=12u
net10
DBITP
8u/1u
M5
"nmos"
ldr=1u
wdr=8u
net7
12u/1u
M8
"pmos"
ldr=1u
wdr=12u
DBITP
PC_
DBITN
EVAL
PC_
WREN
DBITP
DBITN

FIG. 6.0L

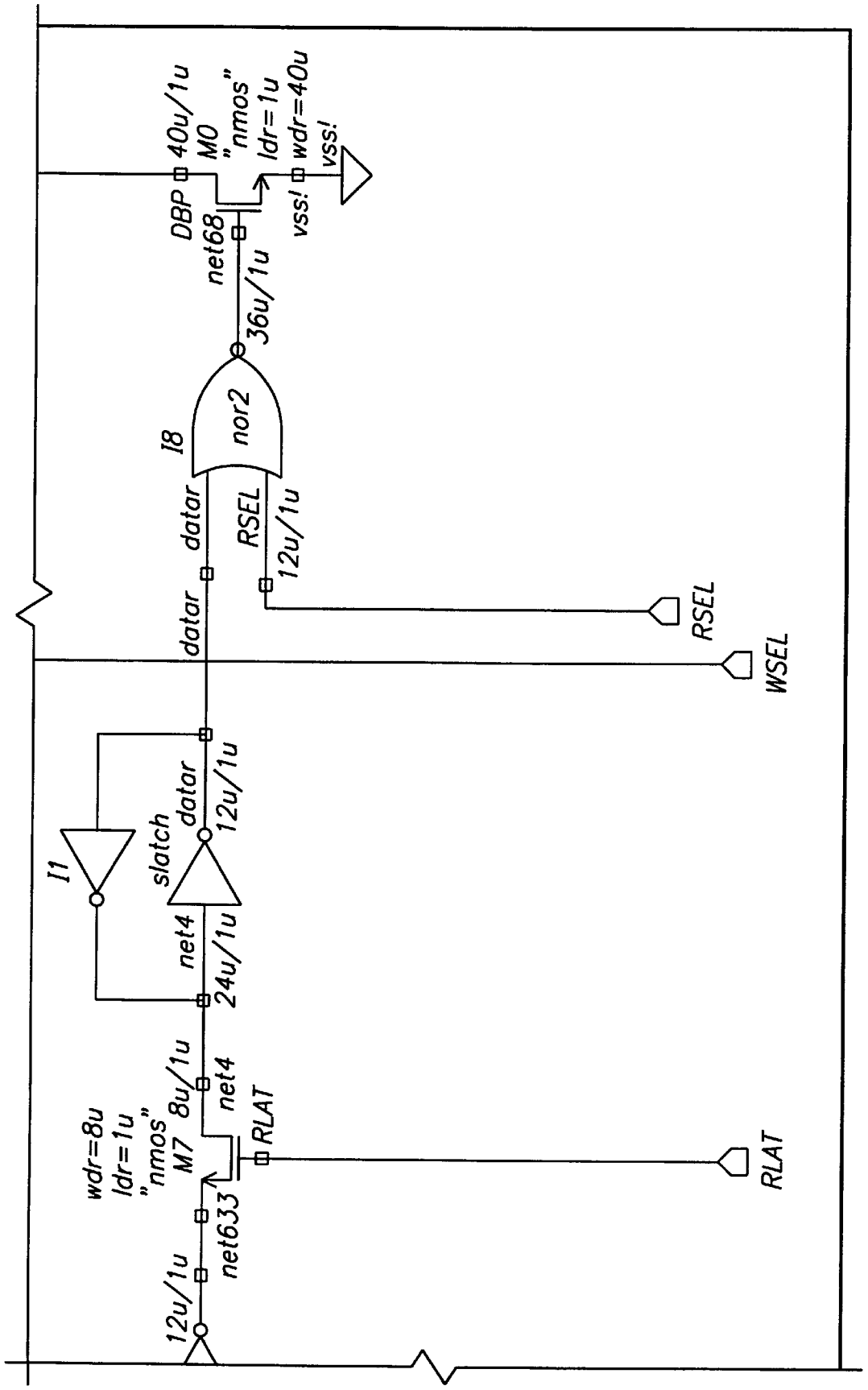

40u/1u
M0
"nmos"
ldr=1u
wdr=40u
vss!
DBP
net68
vss!
36u/1u
I8
nor2
datar
RSEL
12u/1u
datar
RSEL
WSEL
I1
slatch
datar
12u/1u
net4
24u/1u
wdr=8u
ldr=1u
"nmos"
M7
8u/1u
net4
RLAT
RLAT
net633
12u/1u

FIG. 11E0011

7.04AA	7.04AB	7.04AC	7.04AD	7.04AE	7.04AF	7.04AG	7.04AH	7.04AI	7.04AJ
7.04BA	7.04BB	7.04BC	7.04BD	7.04BE	7.04BF	7.04BG	7.04BH	7.04BI	7.04BJ
7.04CA	7.04CB	7.04CC	7.04CD	7.04CE	7.04CF	7.04CG	7.04CH	7.04CI	7.04CJ
7.04DA	7.04DB	7.04DC	7.04DD	7.04DE	7.04DF	7.04DG	7.04DH	7.04DI	7.04DJ
7.04EA	7.04EB	7.04EC	7.04ED	7.04EE	7.04EF	7.04EG	7.04EH	7.04EI	7.04EJ
7.04FA	7.04FB	7.04FC	7.04FD	7.04FE	7.04FF	7.04FG	7.04FH	7.04FI	7.04FJ
7.04GA	7.04GB	7.04GC	7.04GD	7.04GE	7.04GF	7.04GG	7.04GH	7.04GI	7.04GJ
7.04HA	7.04HB	7.04HC	7.04HD	7.04HE	7.04HF	7.04HG	7.04HH	7.04HI	7.04HJ

FIG. 7.04

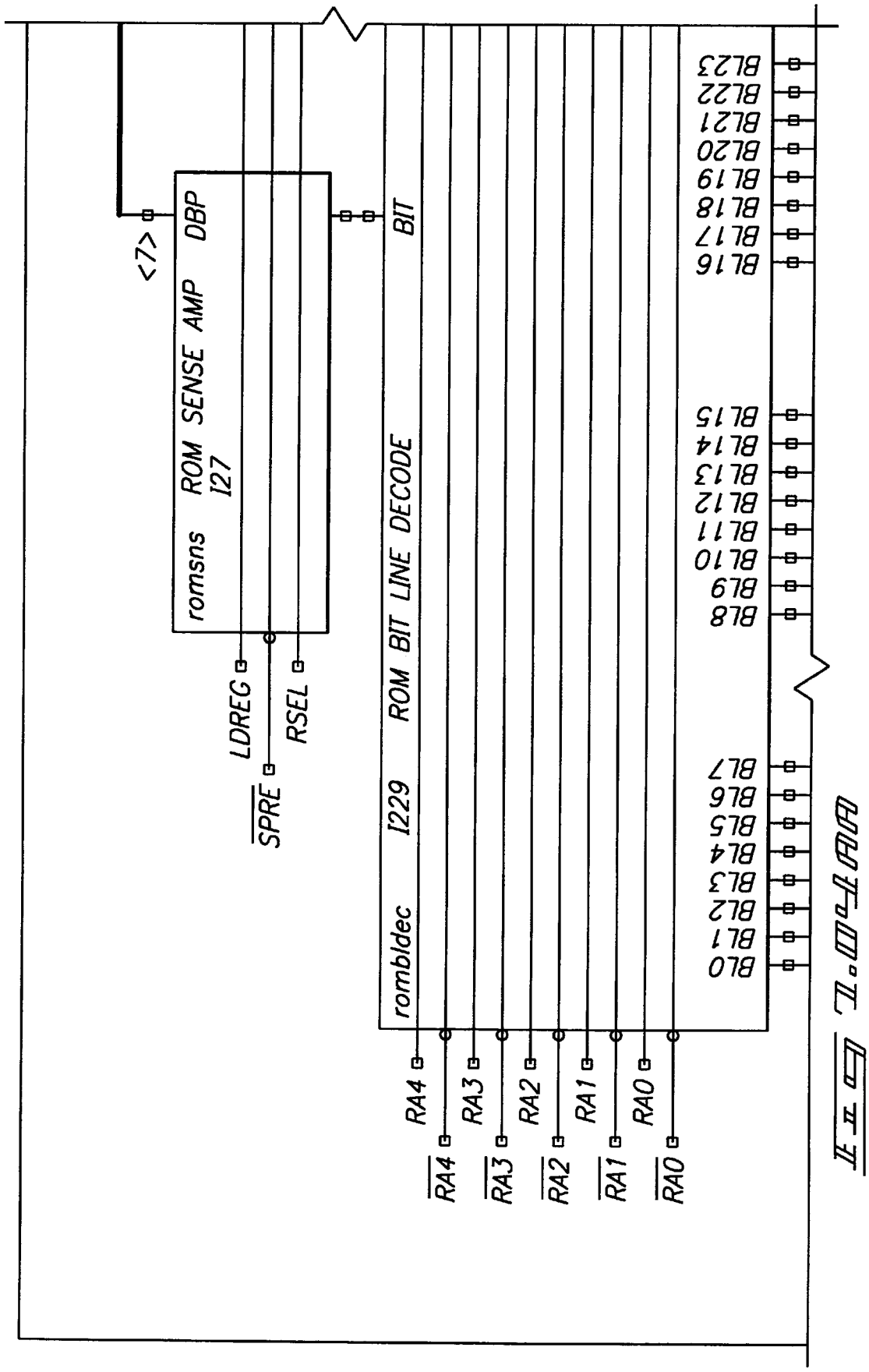

romsns ROM SENSE AMP DBP
I27
<7>
LDREG
SPRE
RSEL
BIT
rombldec I229 ROM BIT LINE DECODE
RA4
RA3
RA2
RA1
RA0
BL23
BL22
BL21
BL20
BL19
BL18
BL17
BL16
BL15
BL14
BL13
BL12
BL11
BL10
BL9
BL8
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0

FIG. 6.11

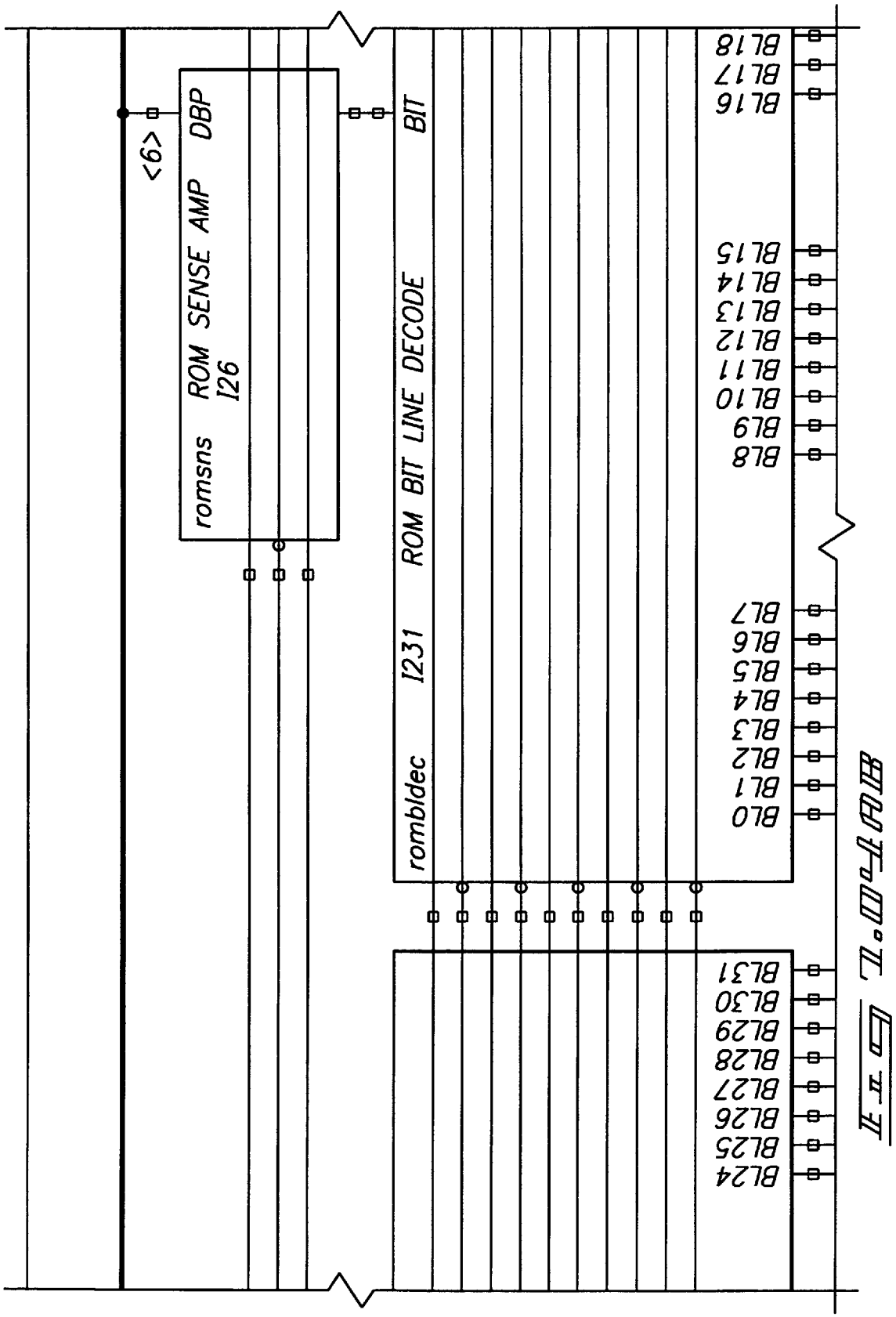
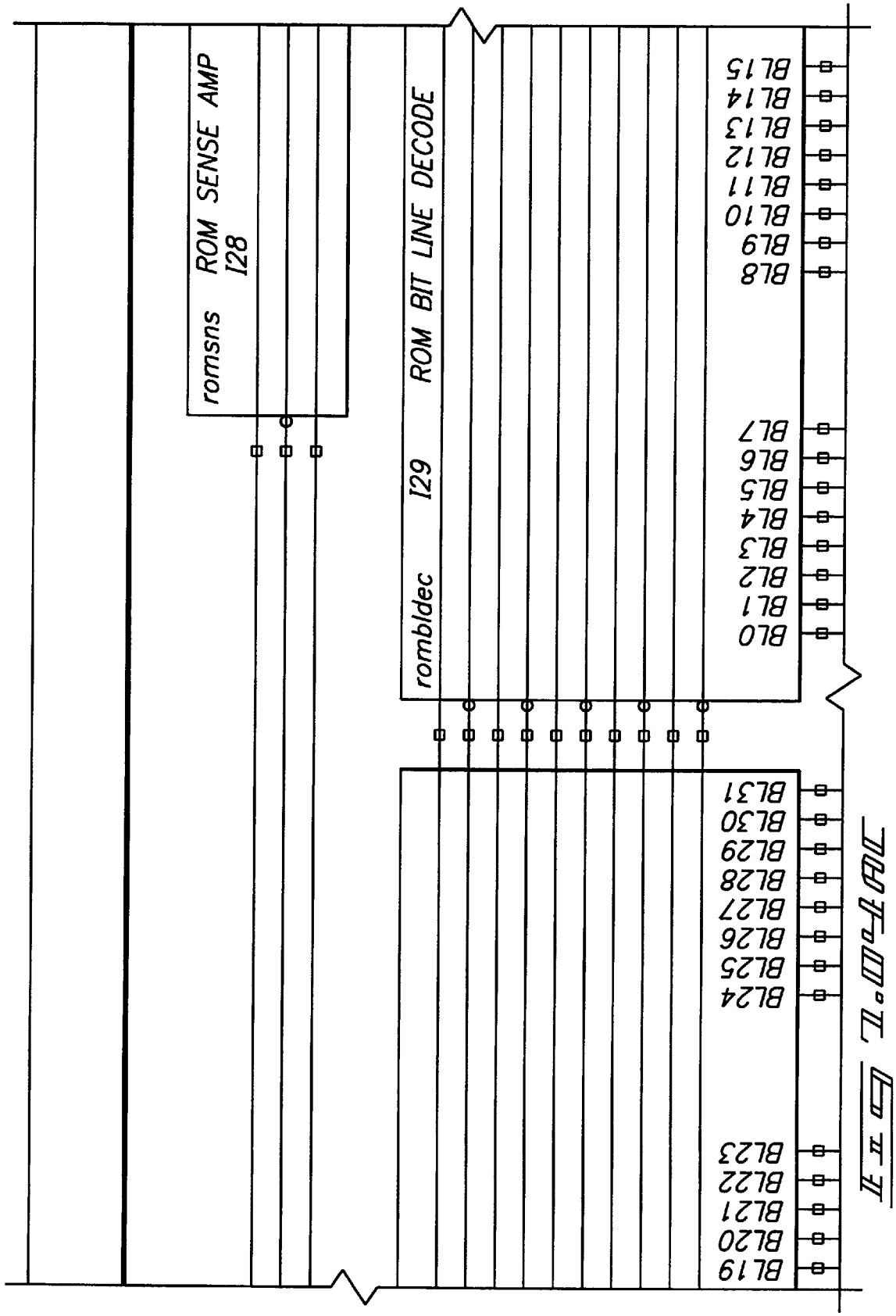

romsns ROM SENSE AMP DBP
I26
<6>
rombldec I231 ROM BIT LINE DECODE BIT
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
BL9
BL10
BL11
BL12
BL13
BL14
BL15
BL16
BL17
BL18
BL24
BL25
BL26
BL27
BL28
BL29
BL30
BL31

FIG. 6.00.L


romsns ROM SENSE AMP I28
rombldec I29 ROM BIT LINE DECODE
BL15
BL14
BL13
BL12
BL11
BL10
BL9
BL8
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
BL31
BL30
BL29
BL28
BL27
BL26
BL25
BL24
BL23
BL22
BL21
BL20
BL19

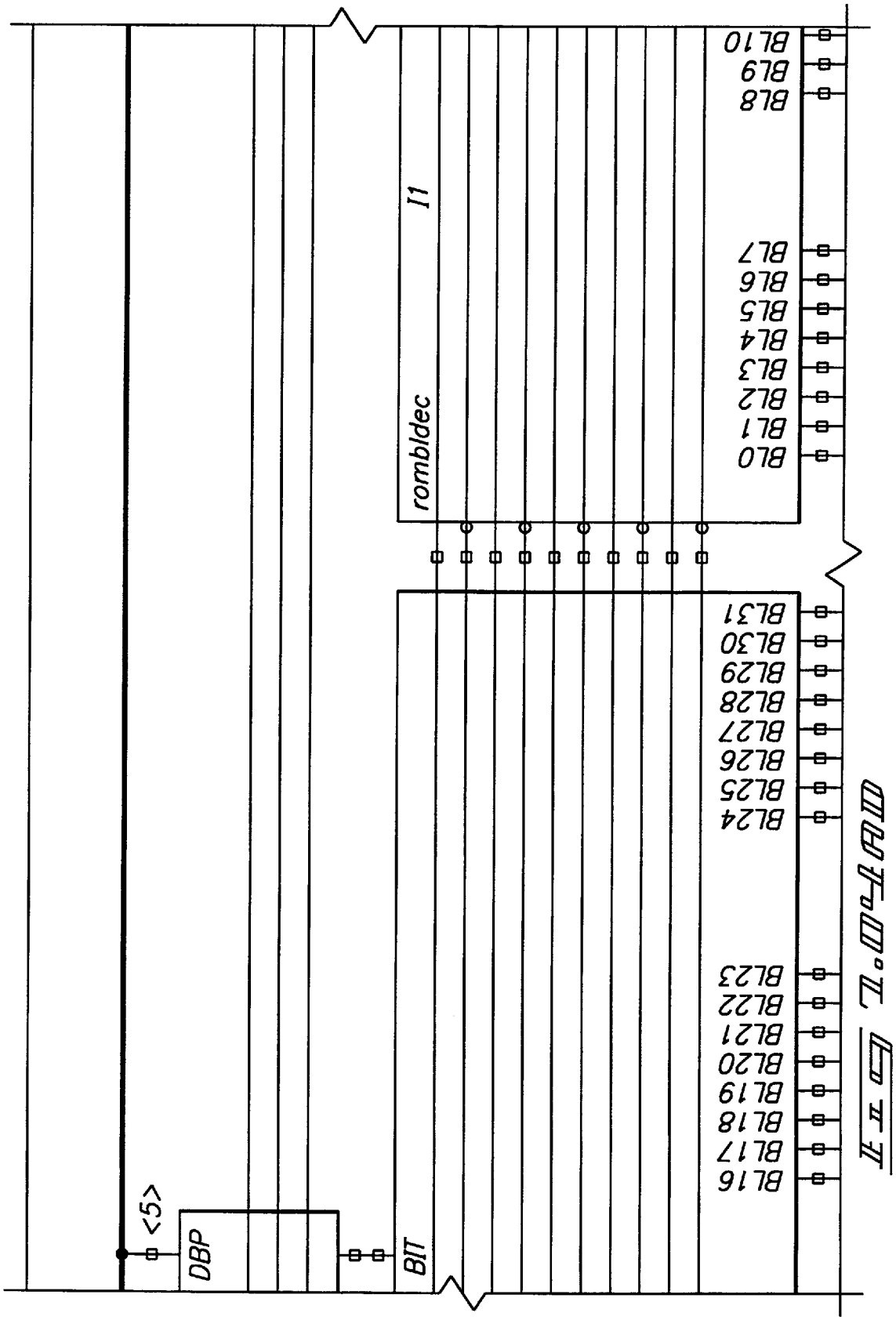
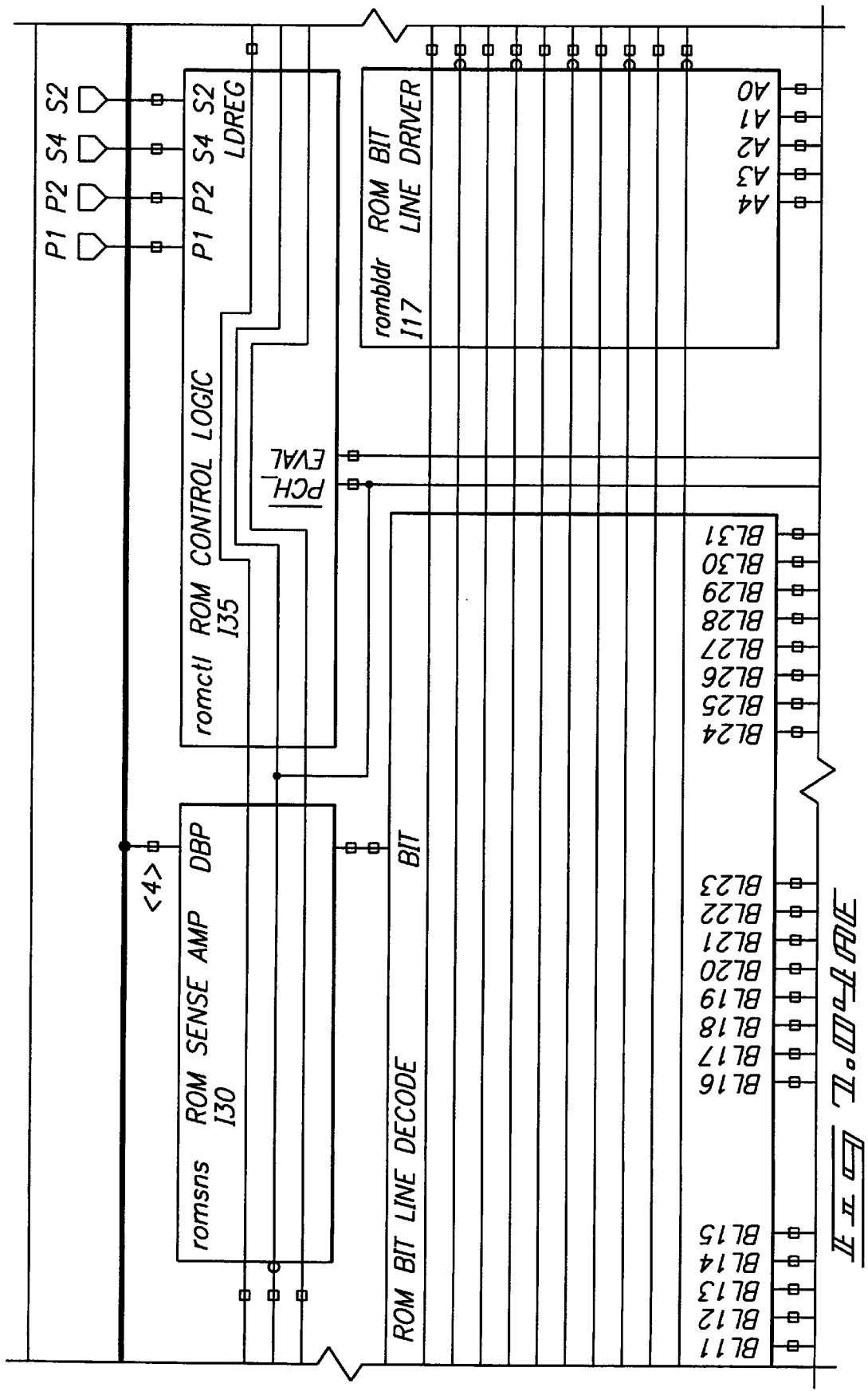

BL10
BL9
BL8
I1
rombldec
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
BL31
BL30
BL29
BL28
BL27
BL26
BL25
BL24
BL23
BL22
BL21
BL20
BL19
BL18
BL17
BL16
<5>
DBP
BIT

FIG. 301


P1 P2 S4 S2
P1 P2 S4 S2 LDREG
romctl ROM CONTROL LOGIC I35
PCH_EVAL
rombldr ROM BIT LINE DRIVER I17
A0
A1
A2
A3
A4
BL31
BL30
BL29
BL28
BL27
BL26
BL25
BL24
BL23
BL22
BL21
BL20
BL19
BL18
BL17
BL16
BL15
BL14
BL13
BL12
BL11
<4>
romsns ROM SENSE AMP DBP I30
ROM BIT LINE DECODE BIT
FIG. 3A

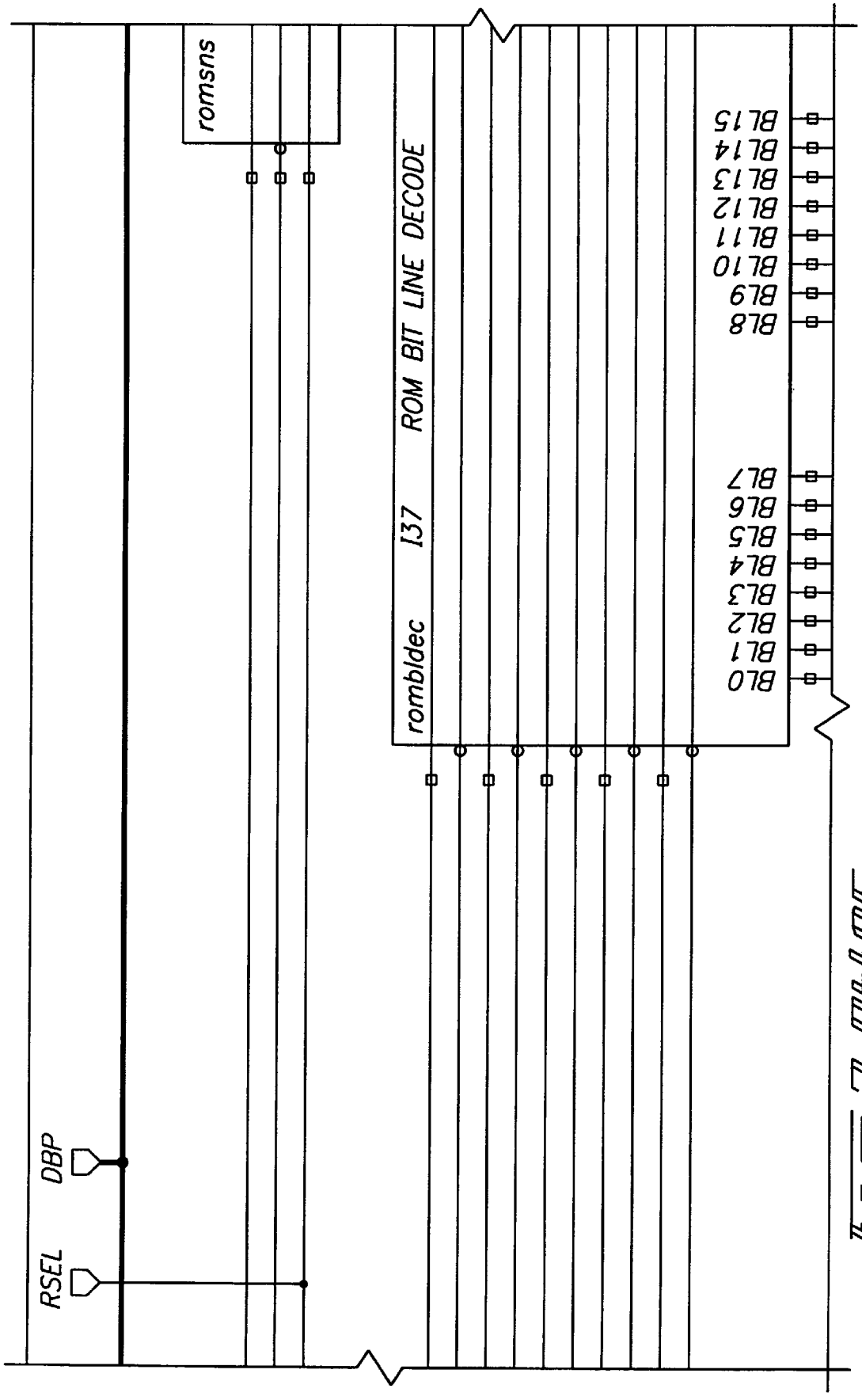
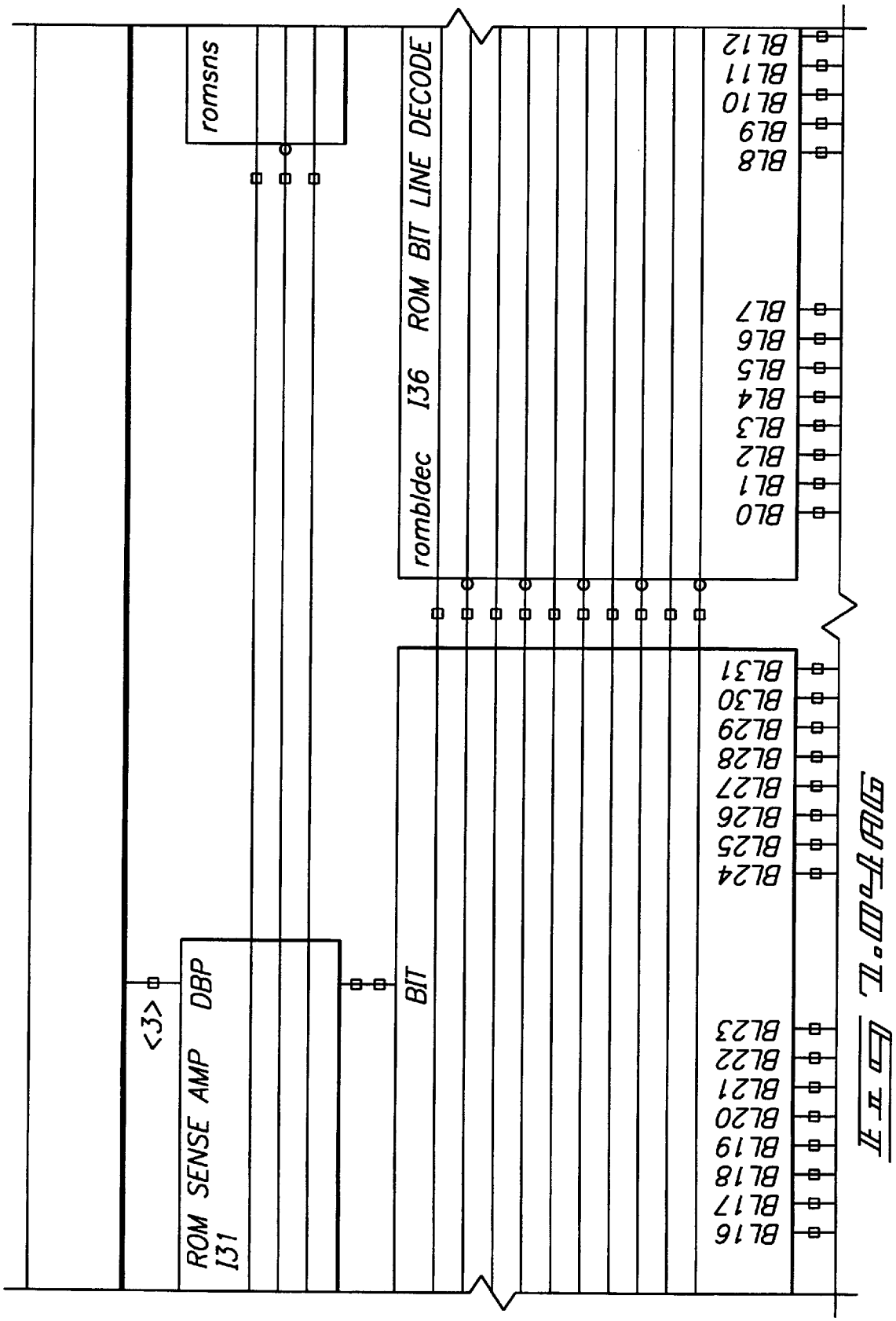
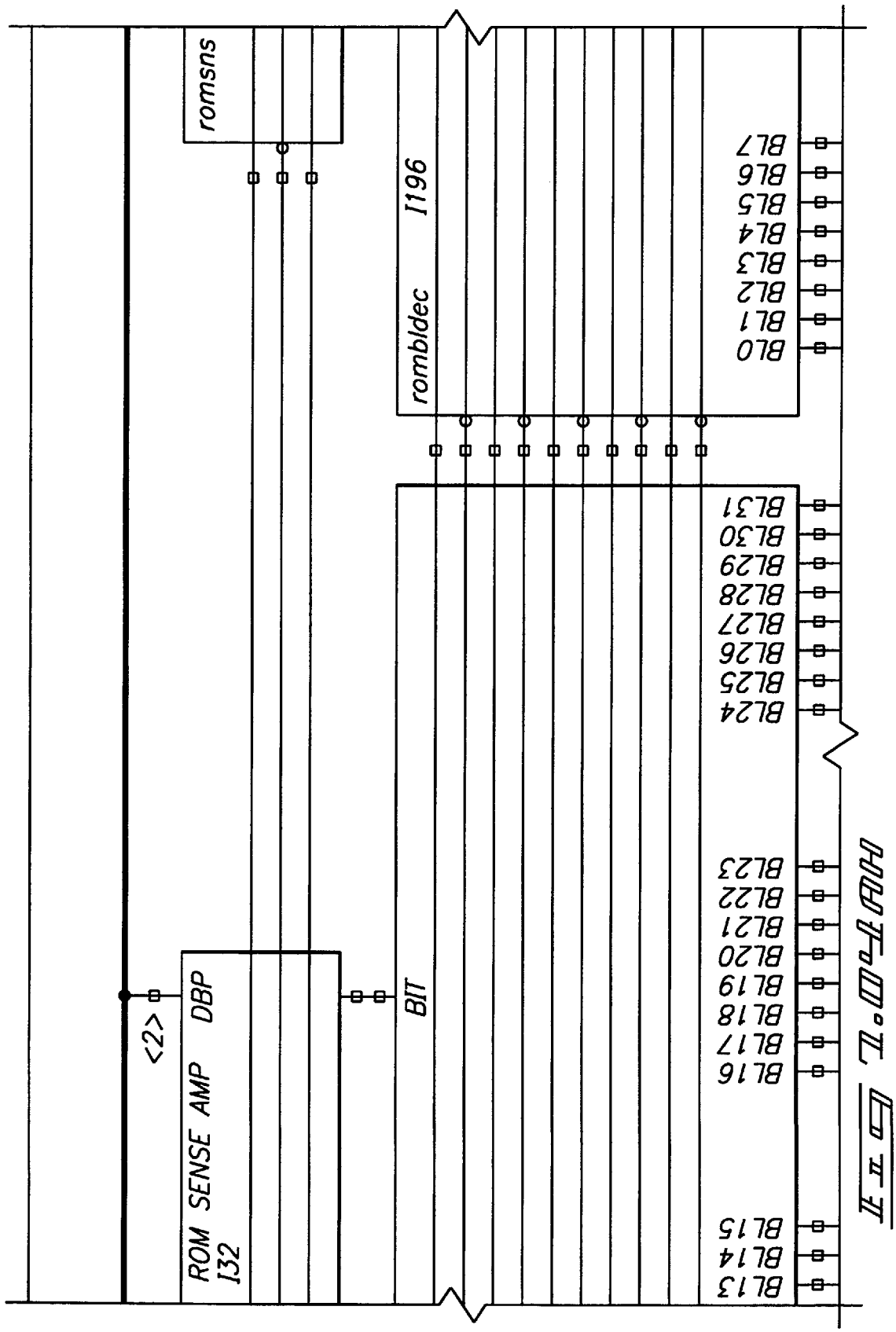
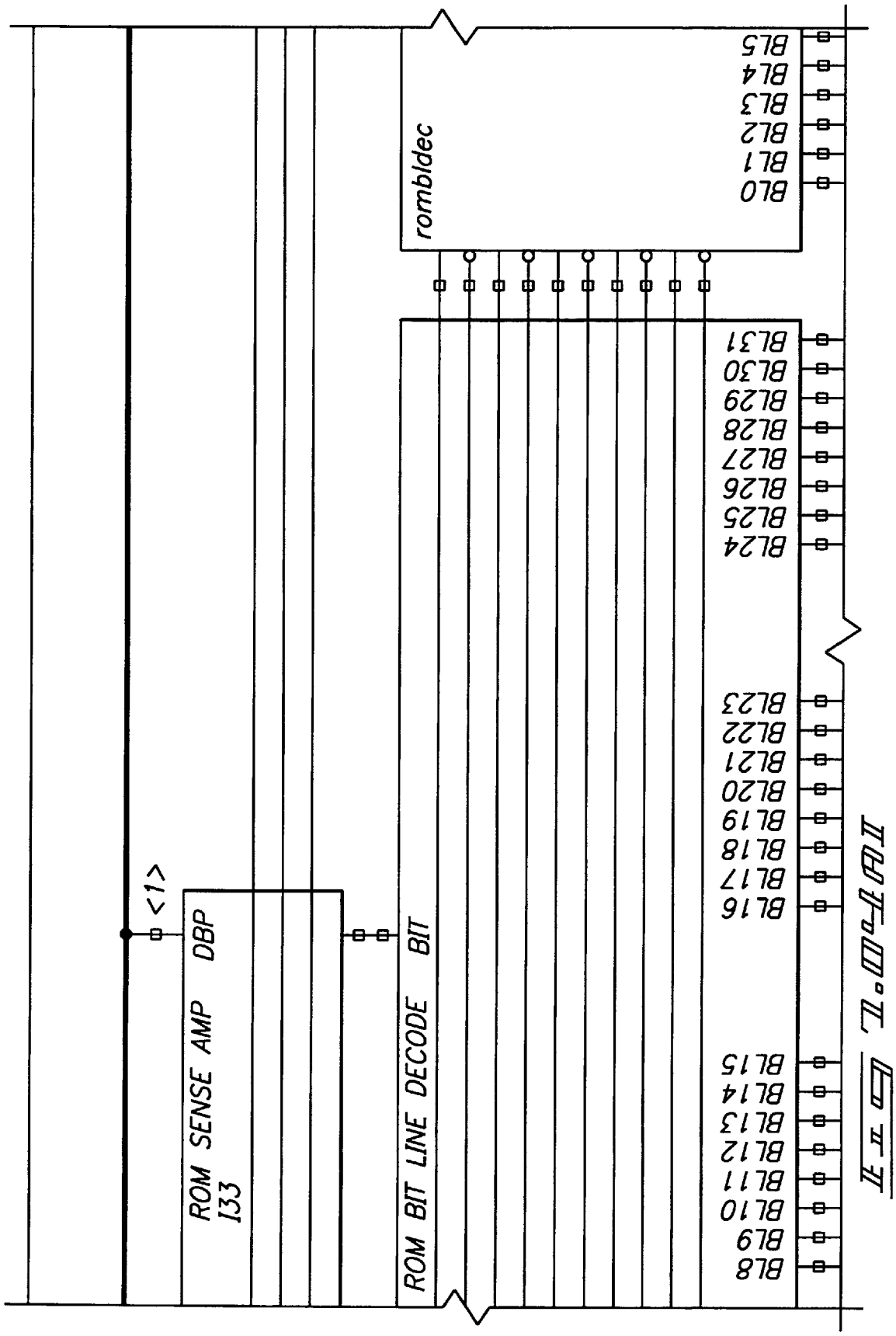

romsns
ROM BIT LINE DECODE
I37
rombldec
BL15
BL14
BL13
BL12
BL11
BL10
BL9
BL8
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
DBP
RSEL

FIG. 137


romsns
rombldec I36 ROM BIT LINE DECODE
BL12
BL11
BL10
BL9
BL8
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
BL31
BL30
BL29
BL28
BL27
BL26
BL25
BL24
BL23
BL22
BL21
BL20
BL19
BL18
BL17
BL16
<3>
ROM SENSE AMP DBP I31
BIT


romsns
rombldec 1196
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
BL31
BL30
BL29
BL28
BL27
BL26
BL25
BL24
BL23
BL22
BL21
BL20
BL19
BL18
BL17
BL16
BL15
BL14
BL13
BIT
<2>
DBP
ROM SENSE AMP
132


rombldec
BL5
BL4
BL3
BL2
BL1
BL0
BL31
BL30
BL29
BL28
BL27
BL26
BL25
BL24
BL23
BL22
BL21
BL20
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ROM SENSE AMP DBP
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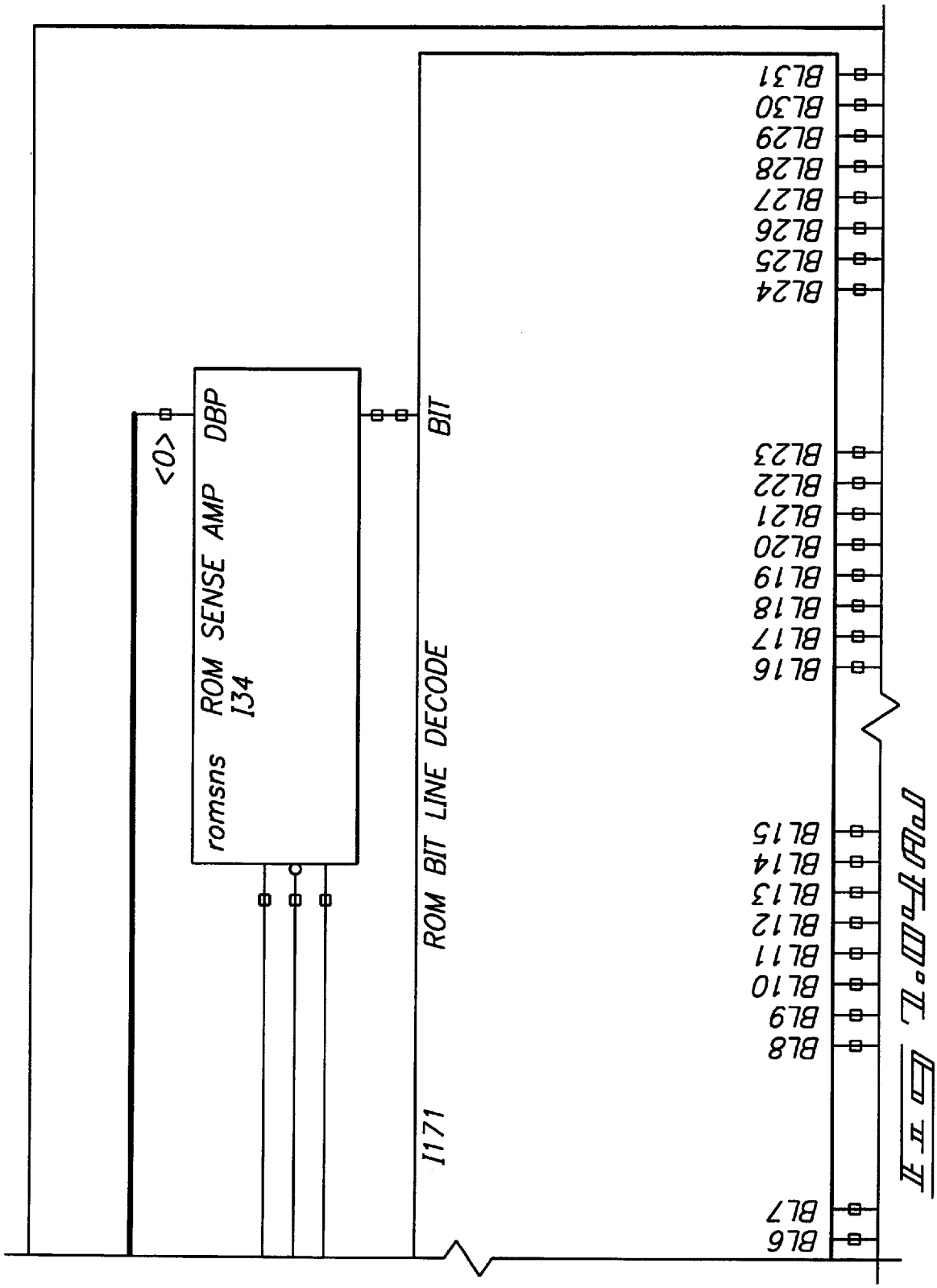
FIG. 133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ROW 1.00 FIG
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ROM BIT LINE DECODE
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DBP
ROM SENSE AMP
I34
romsns

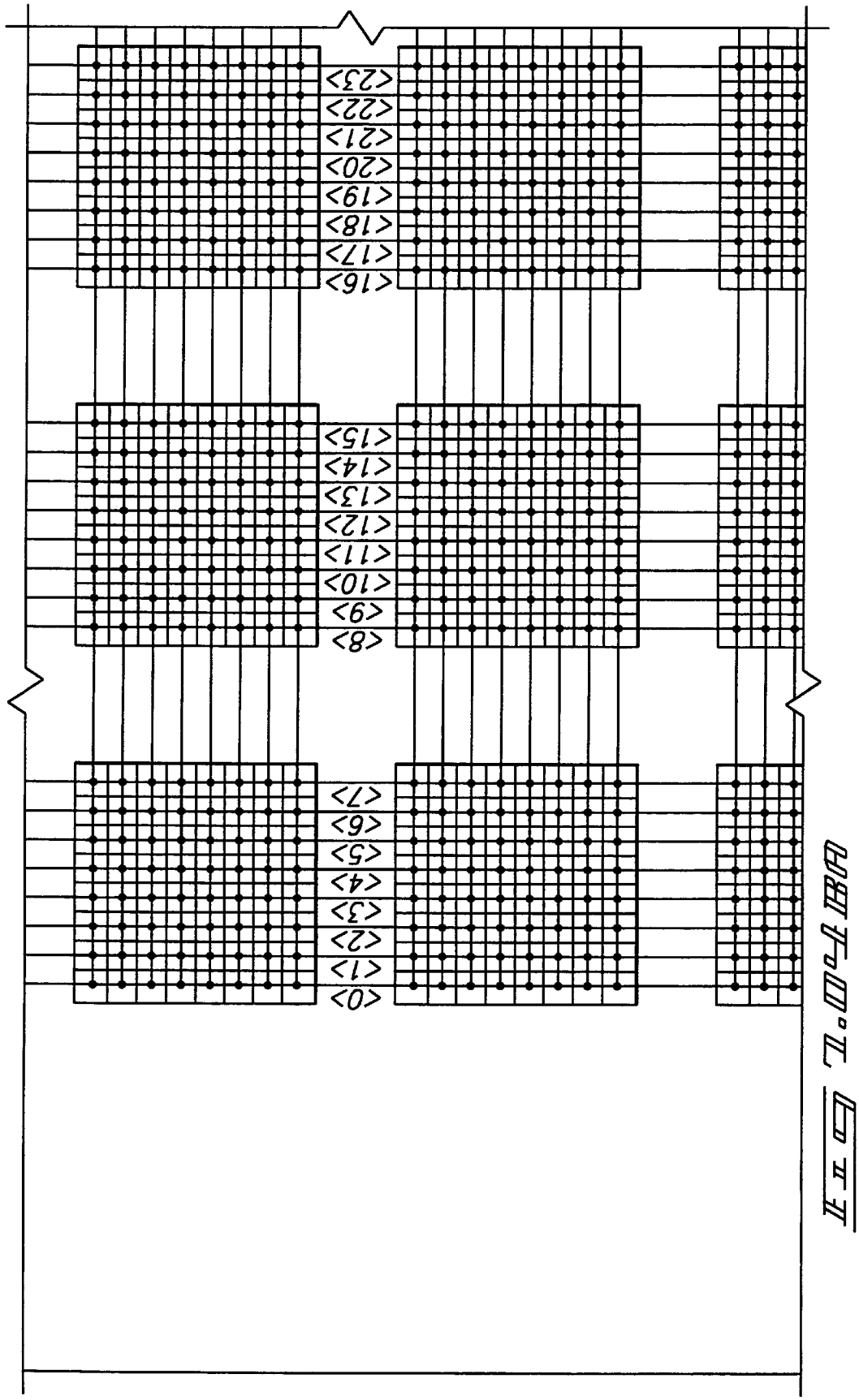
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FIG. 308A

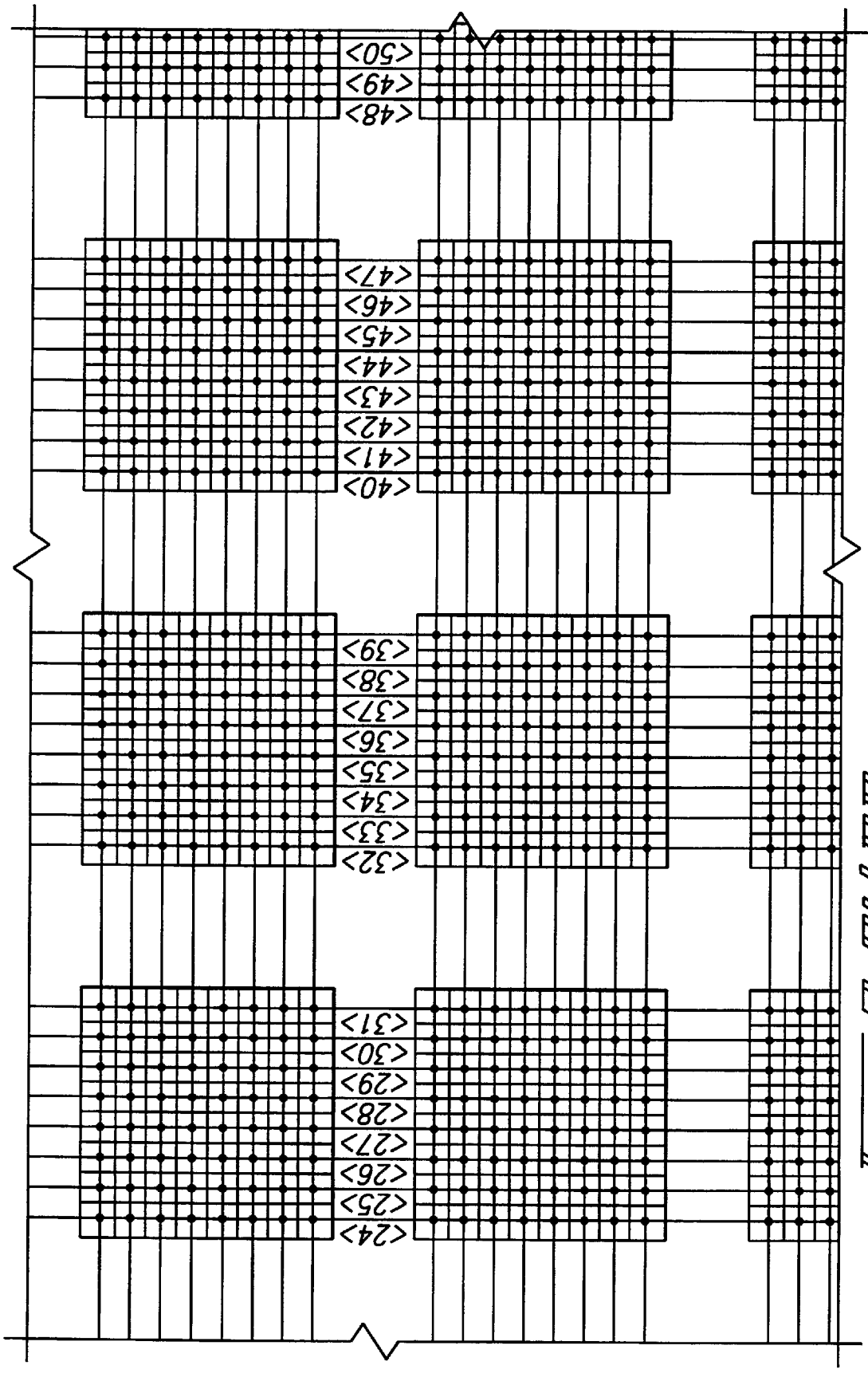
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FIG. 31

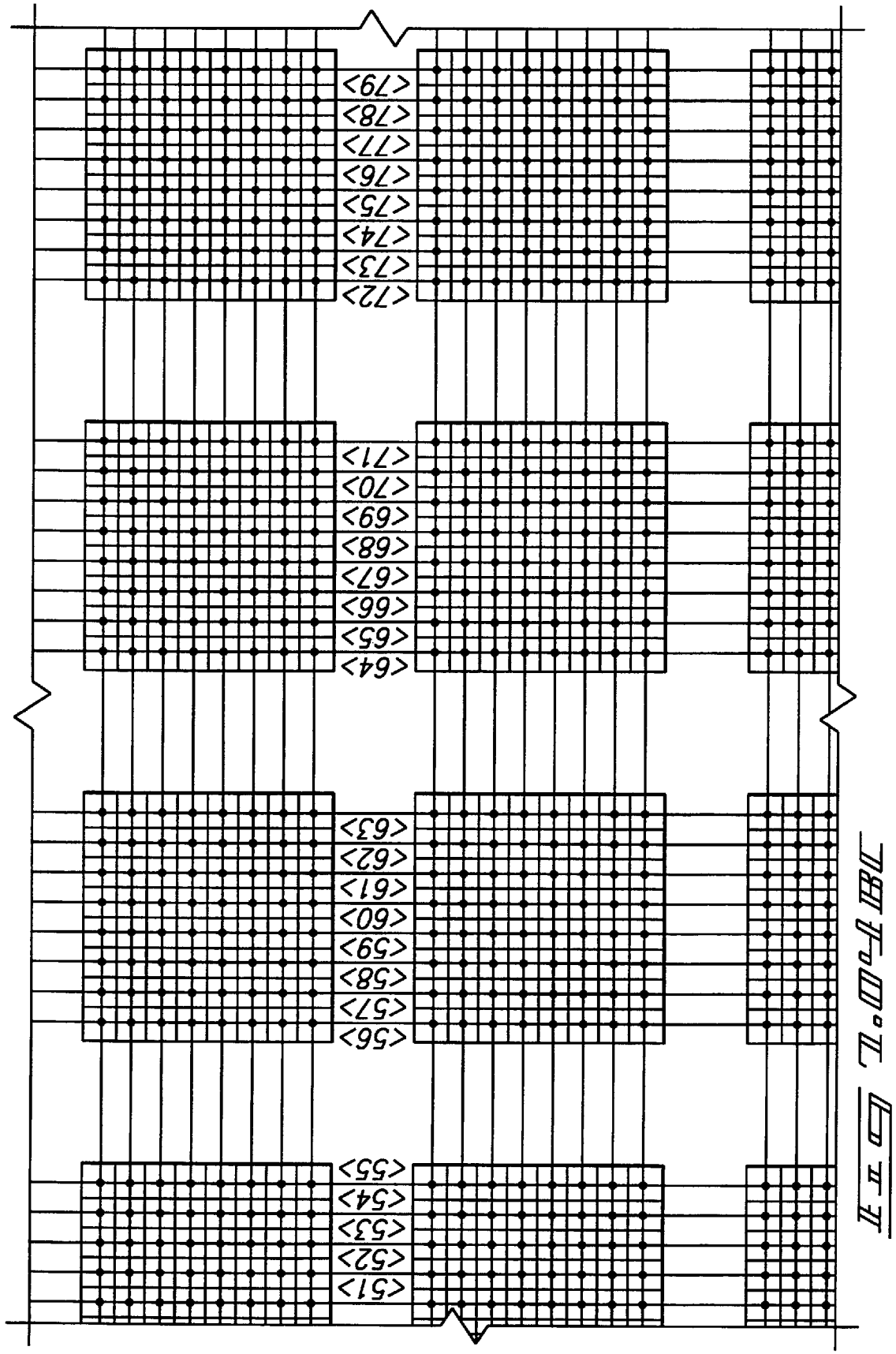
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FIG. 308

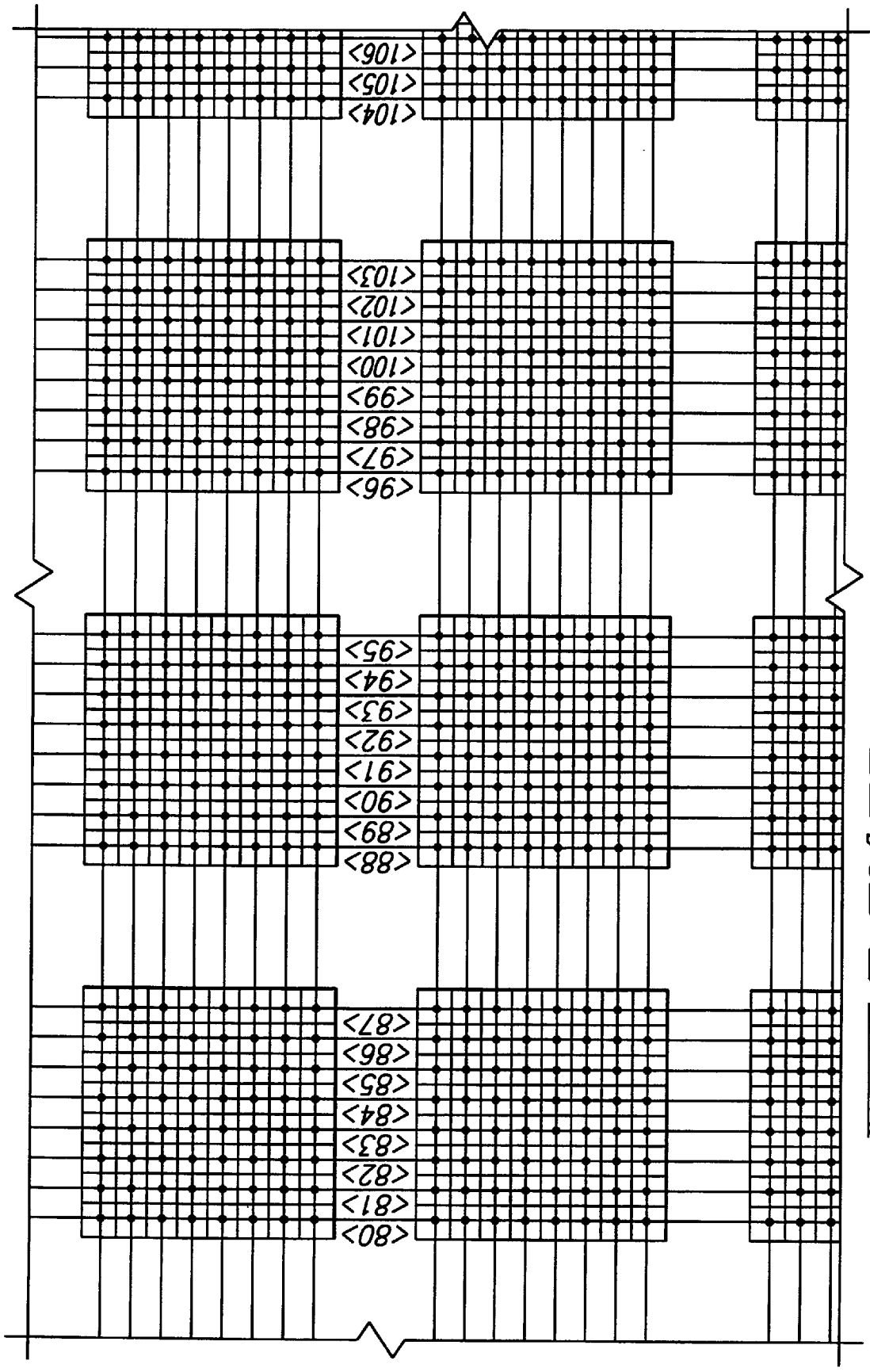
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FIG. 1080

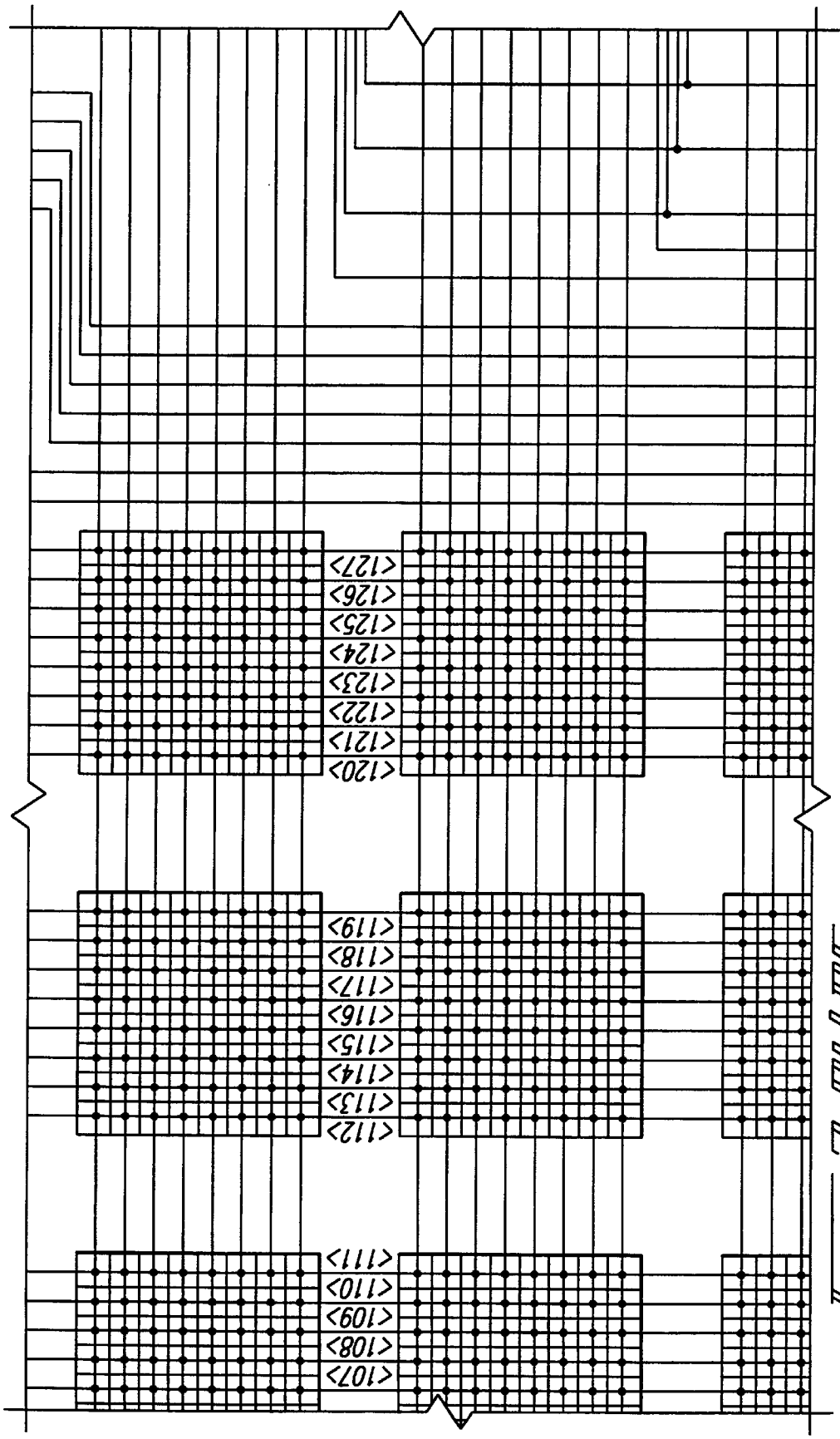
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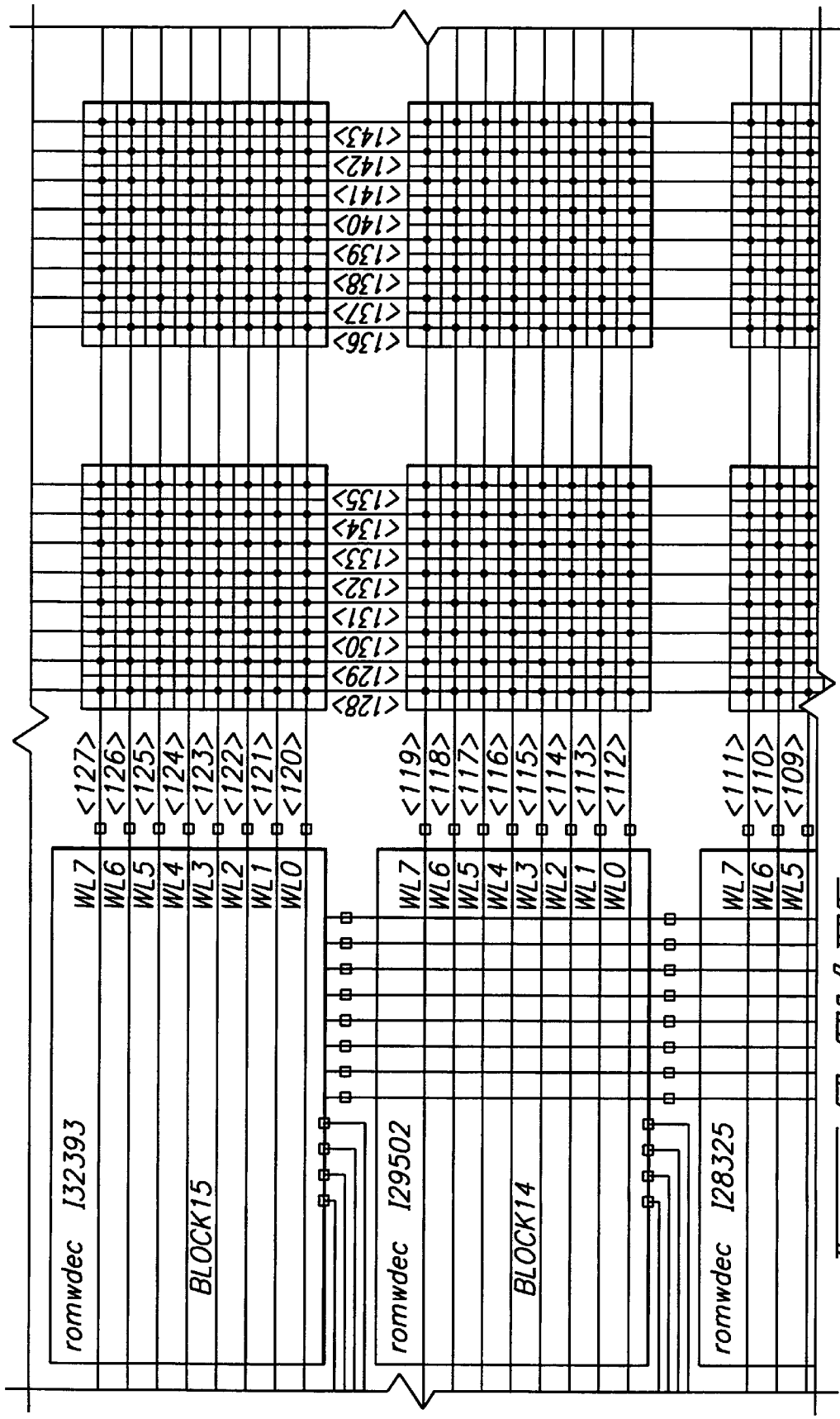
FIG. 70L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romwdec I29502
BLOCK14
romwdec I28325

FIG. 1104A

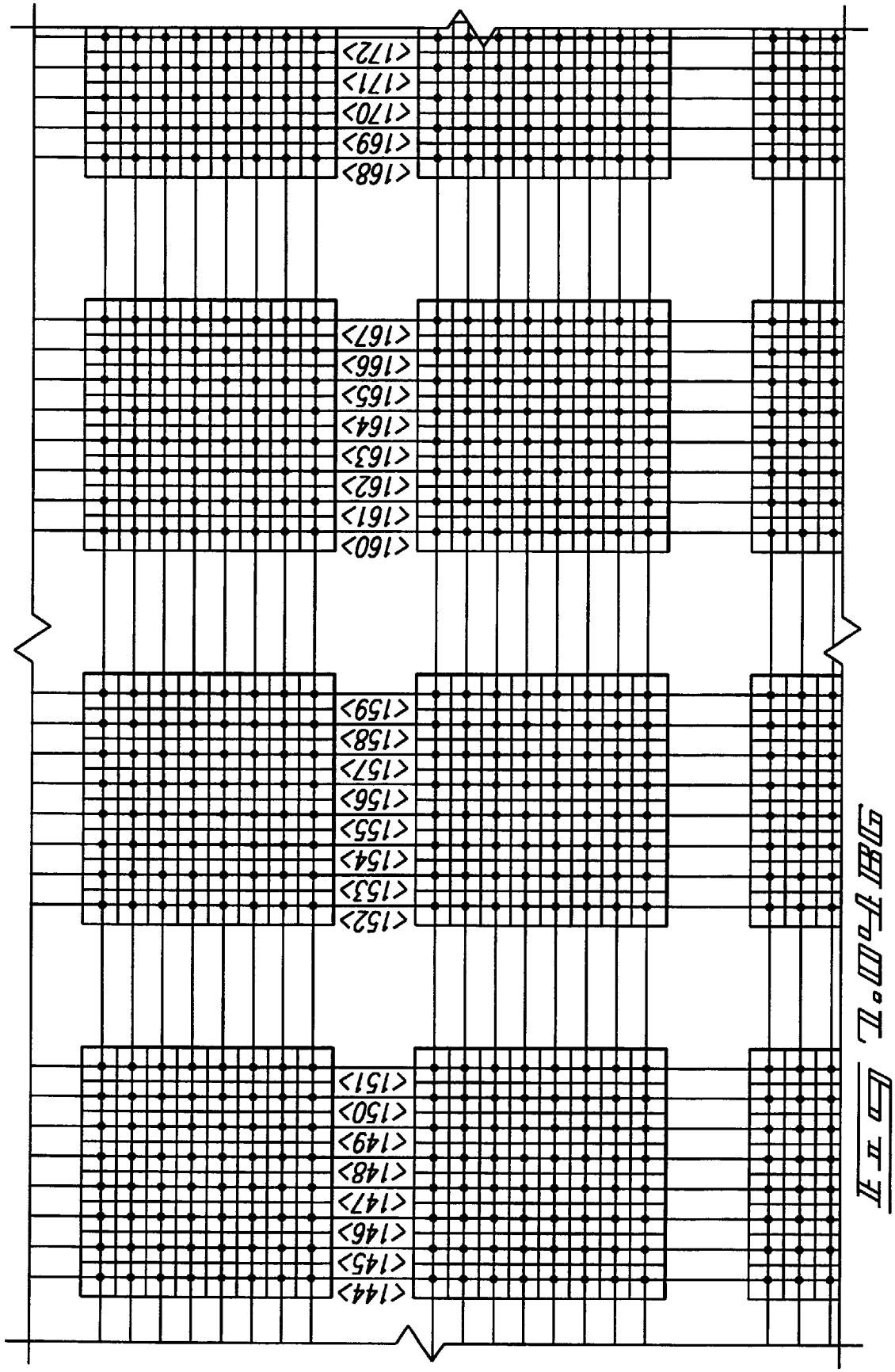
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FIG. 150L

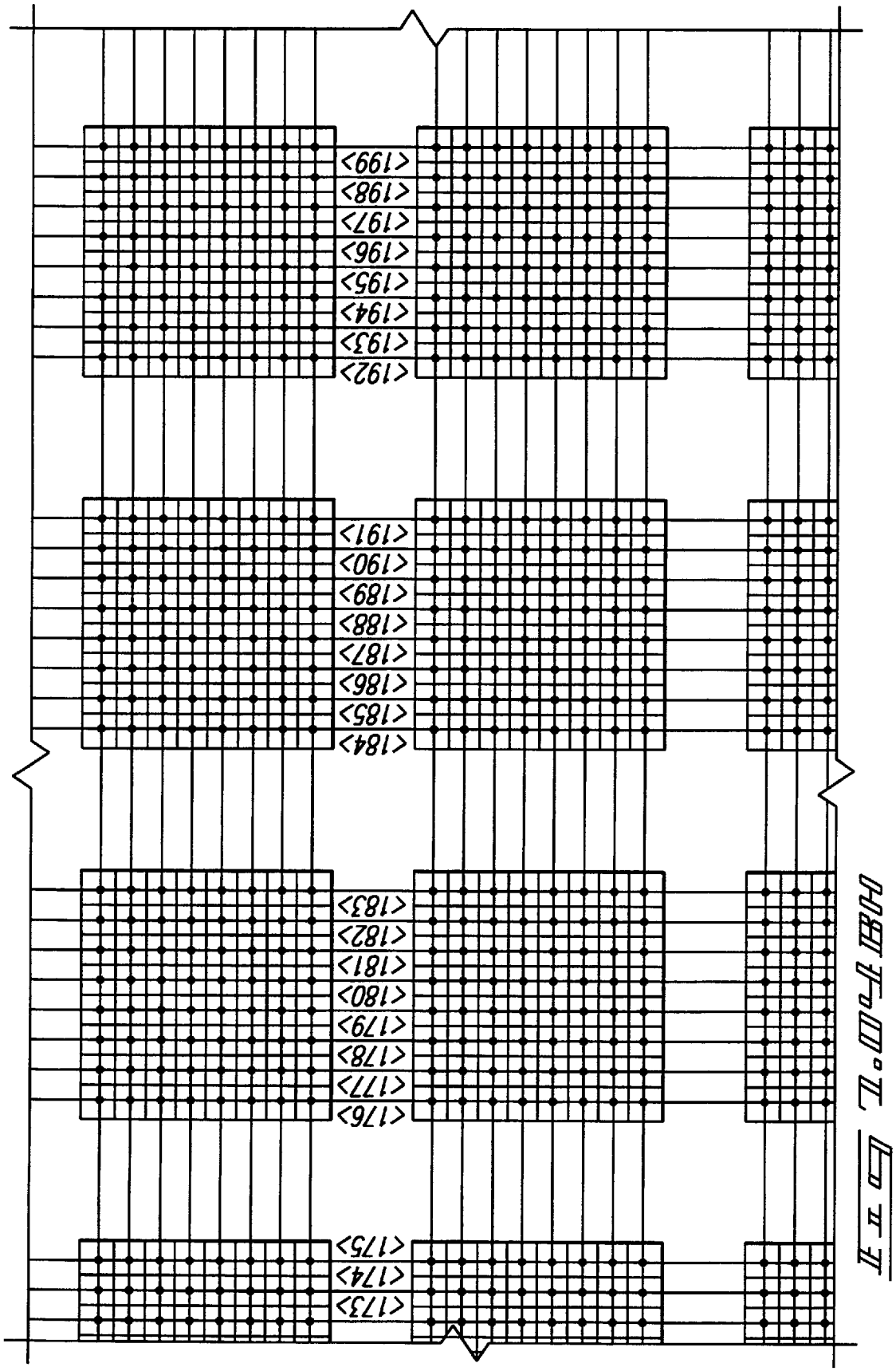
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FIG. 315

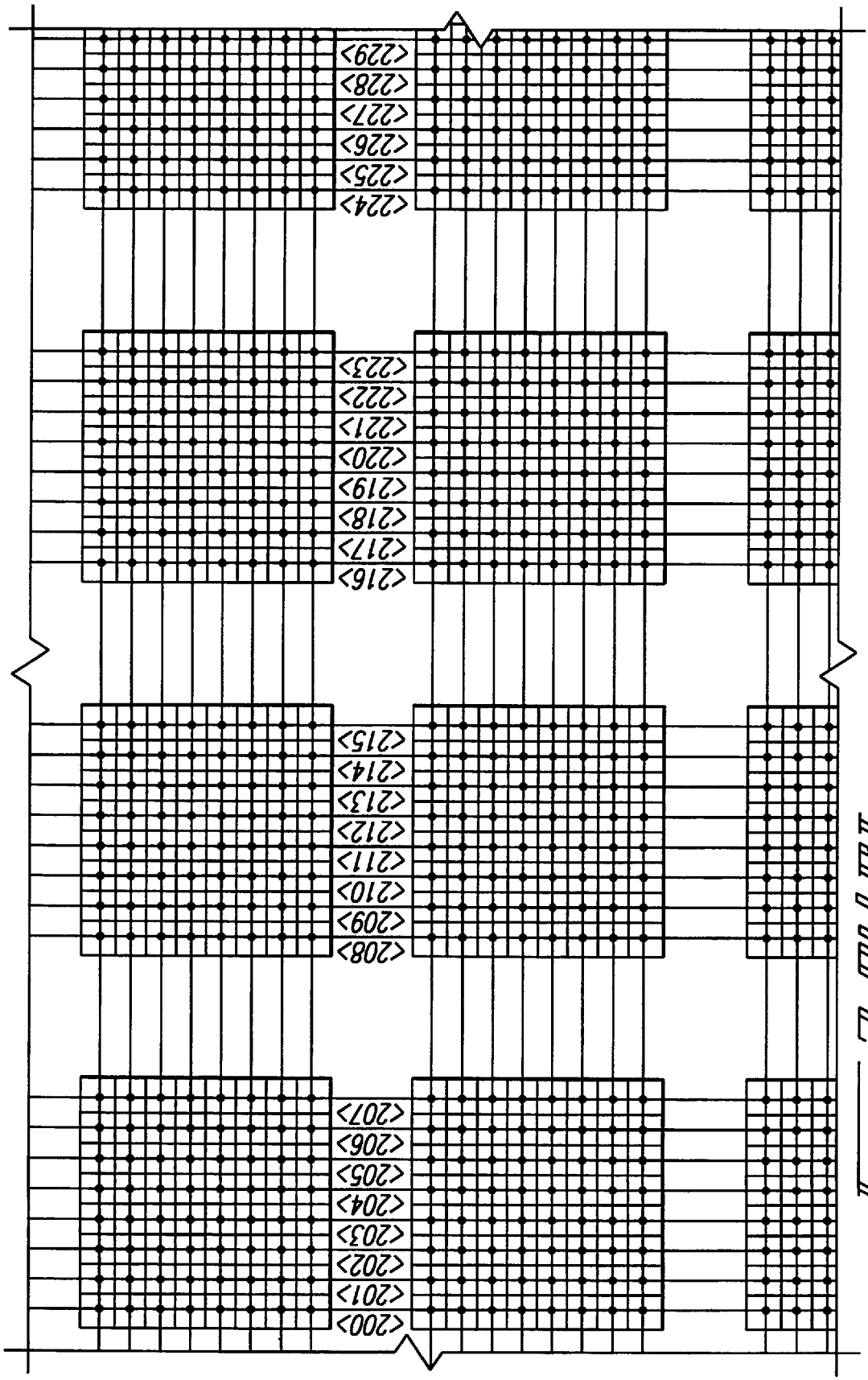
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FIG. 405L

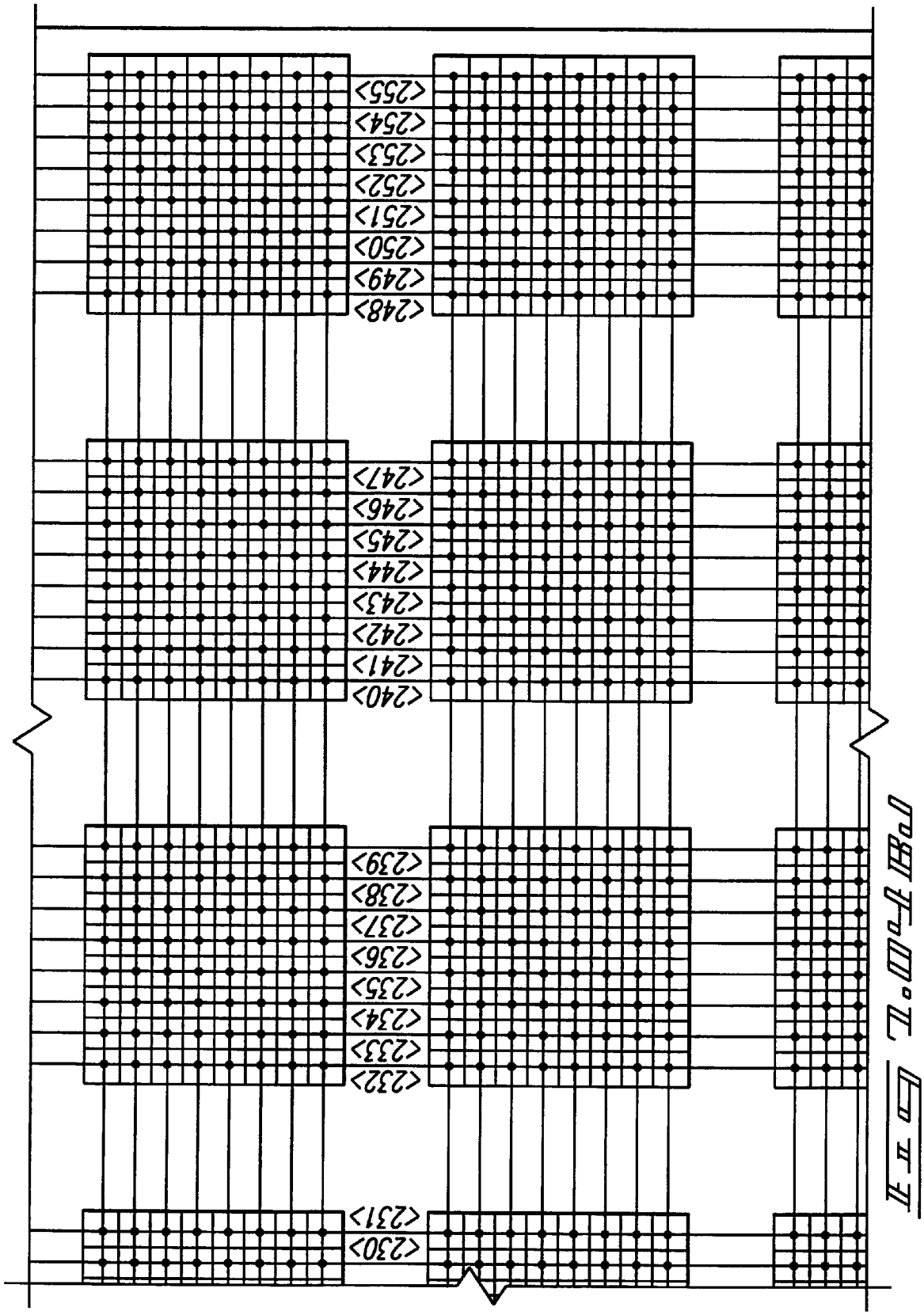
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FIG. 317

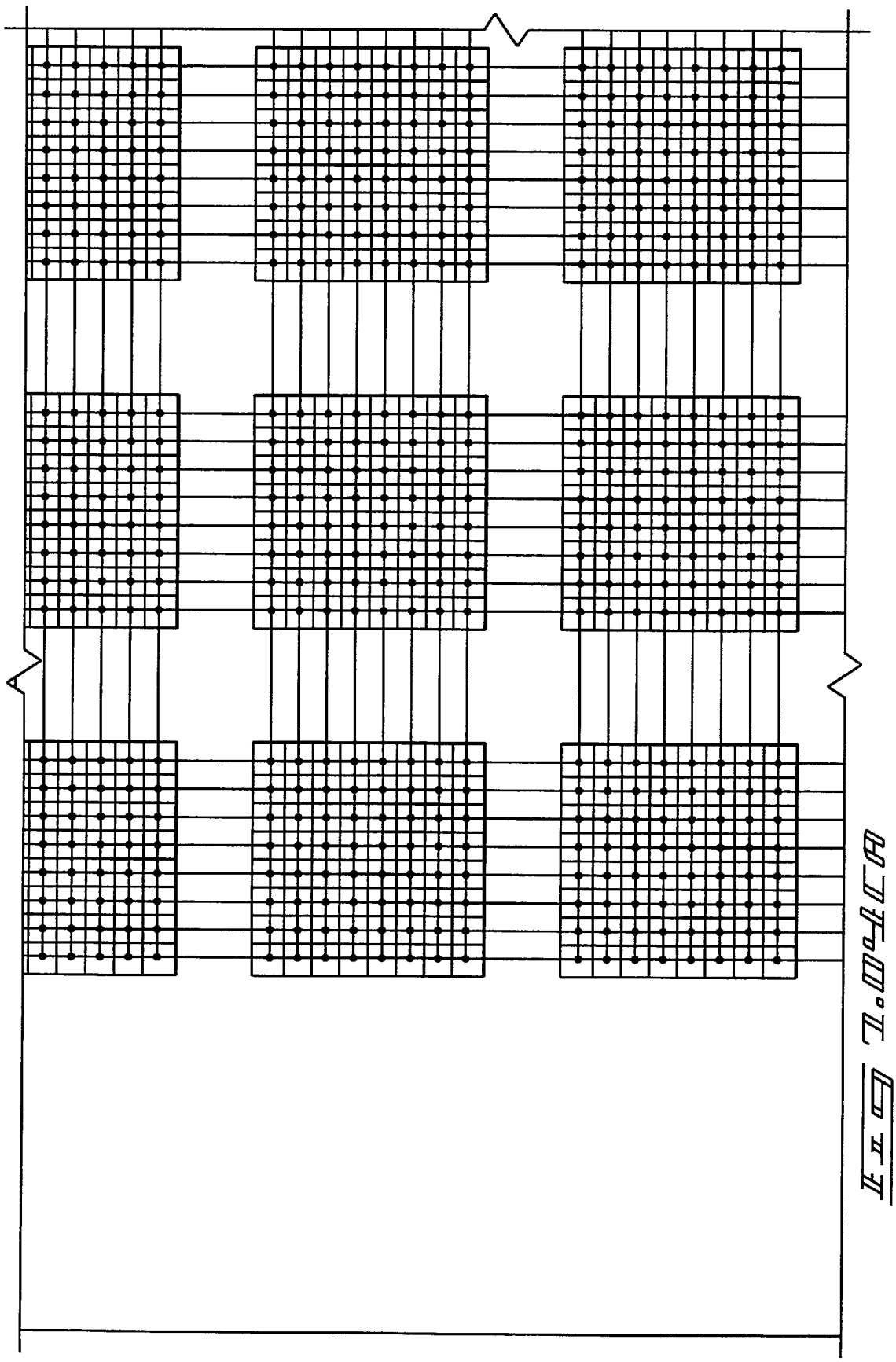


FIG 11,604A

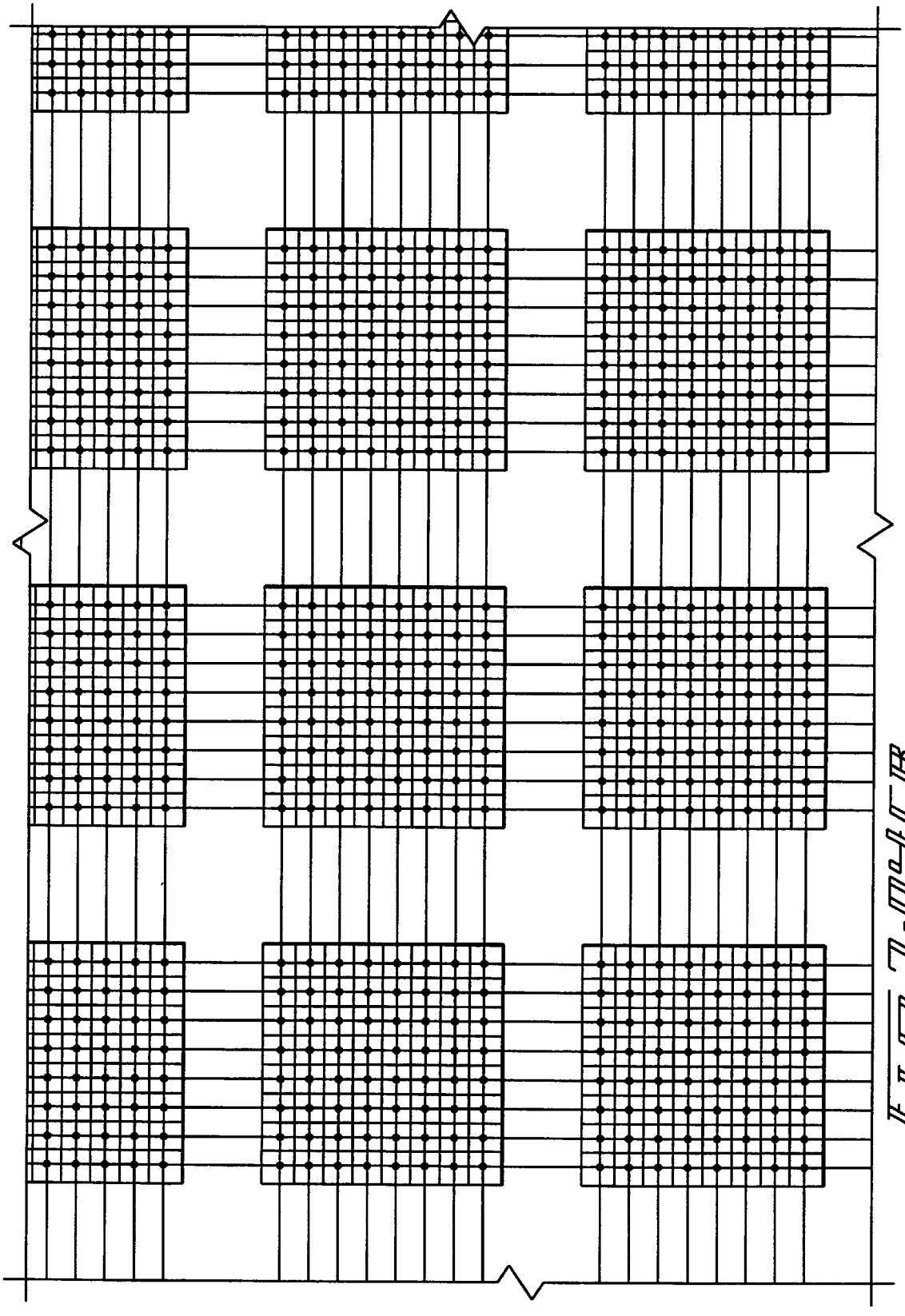
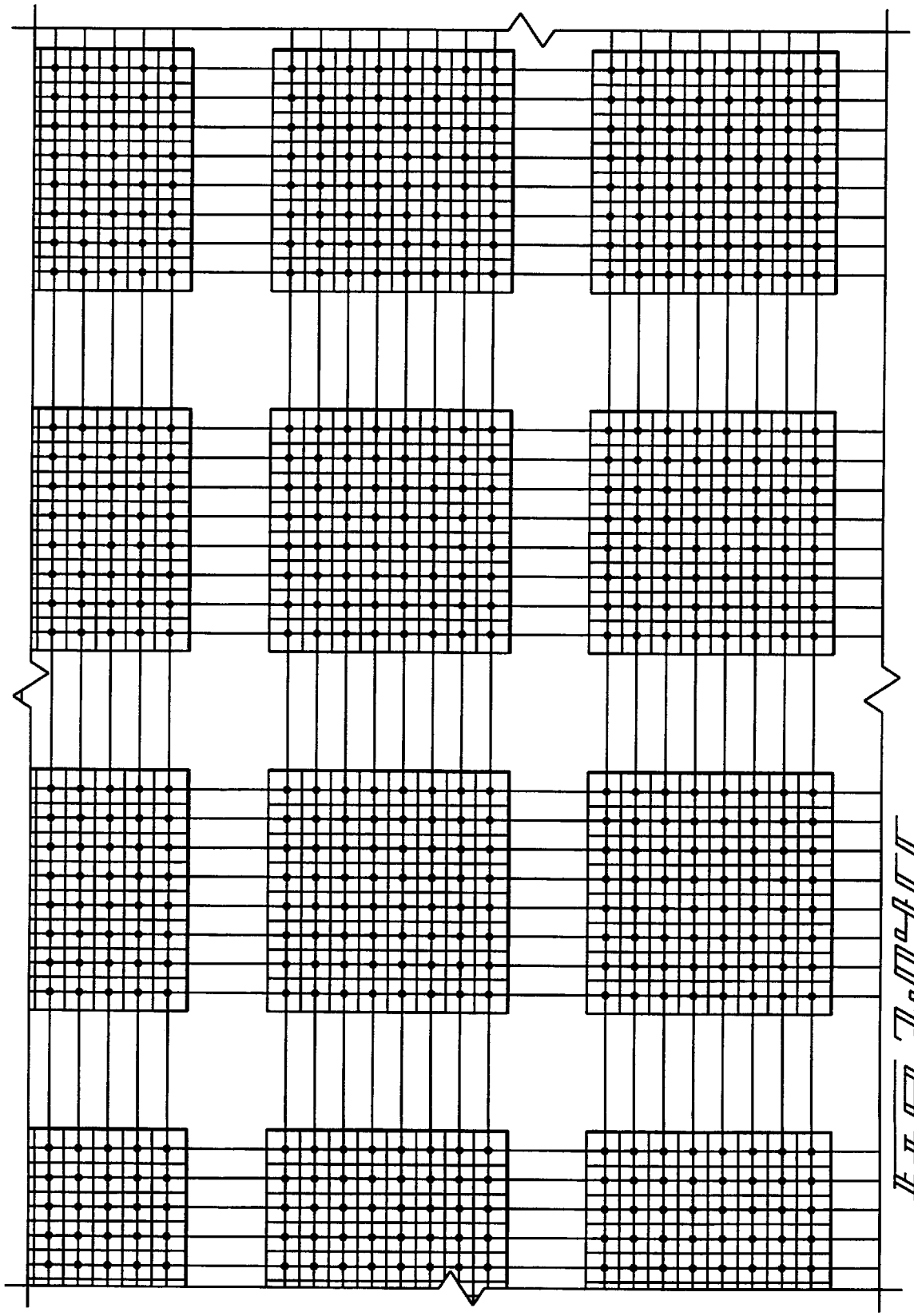


FIG. 7.00.BLAT



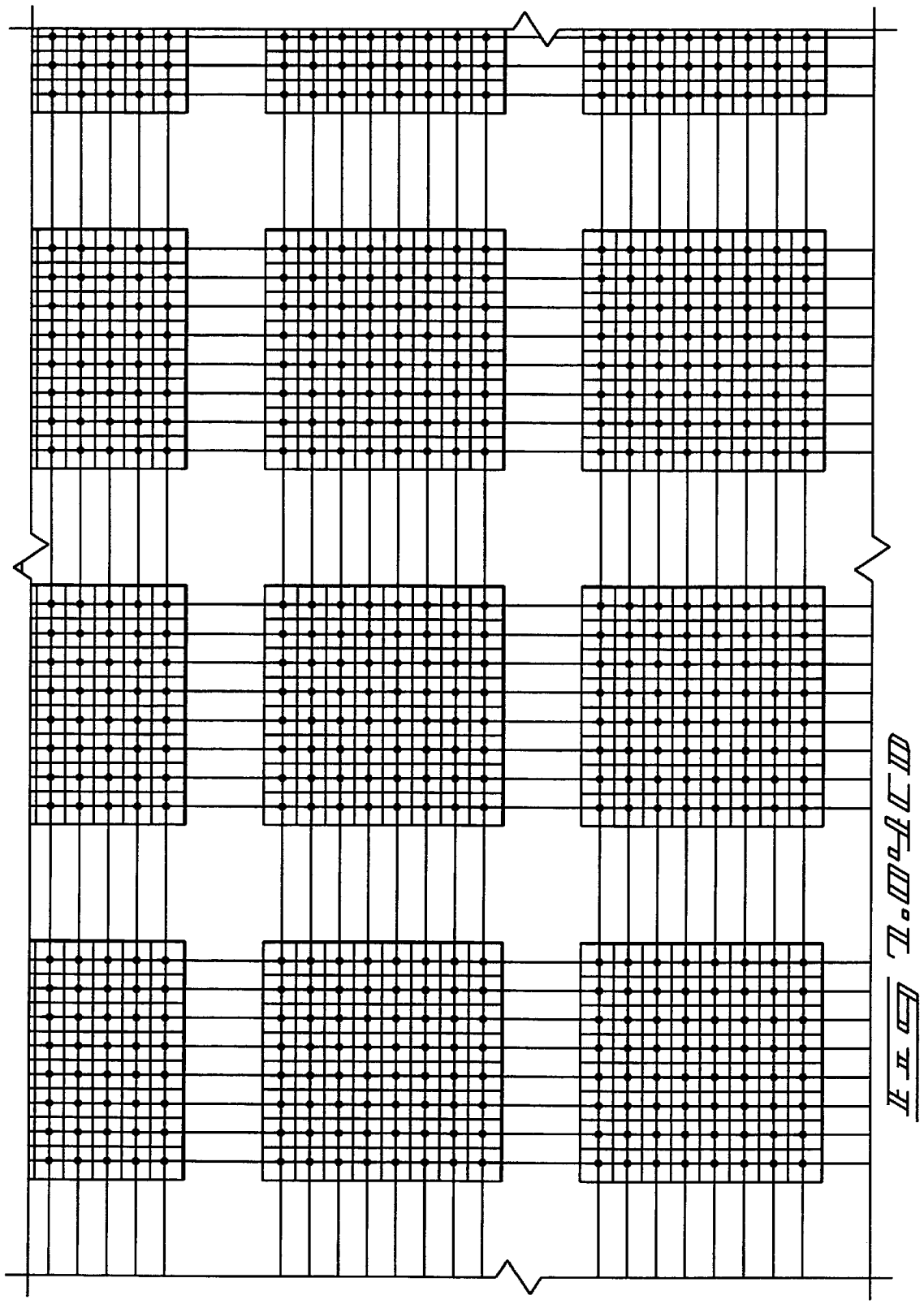


FIG. 7.0746

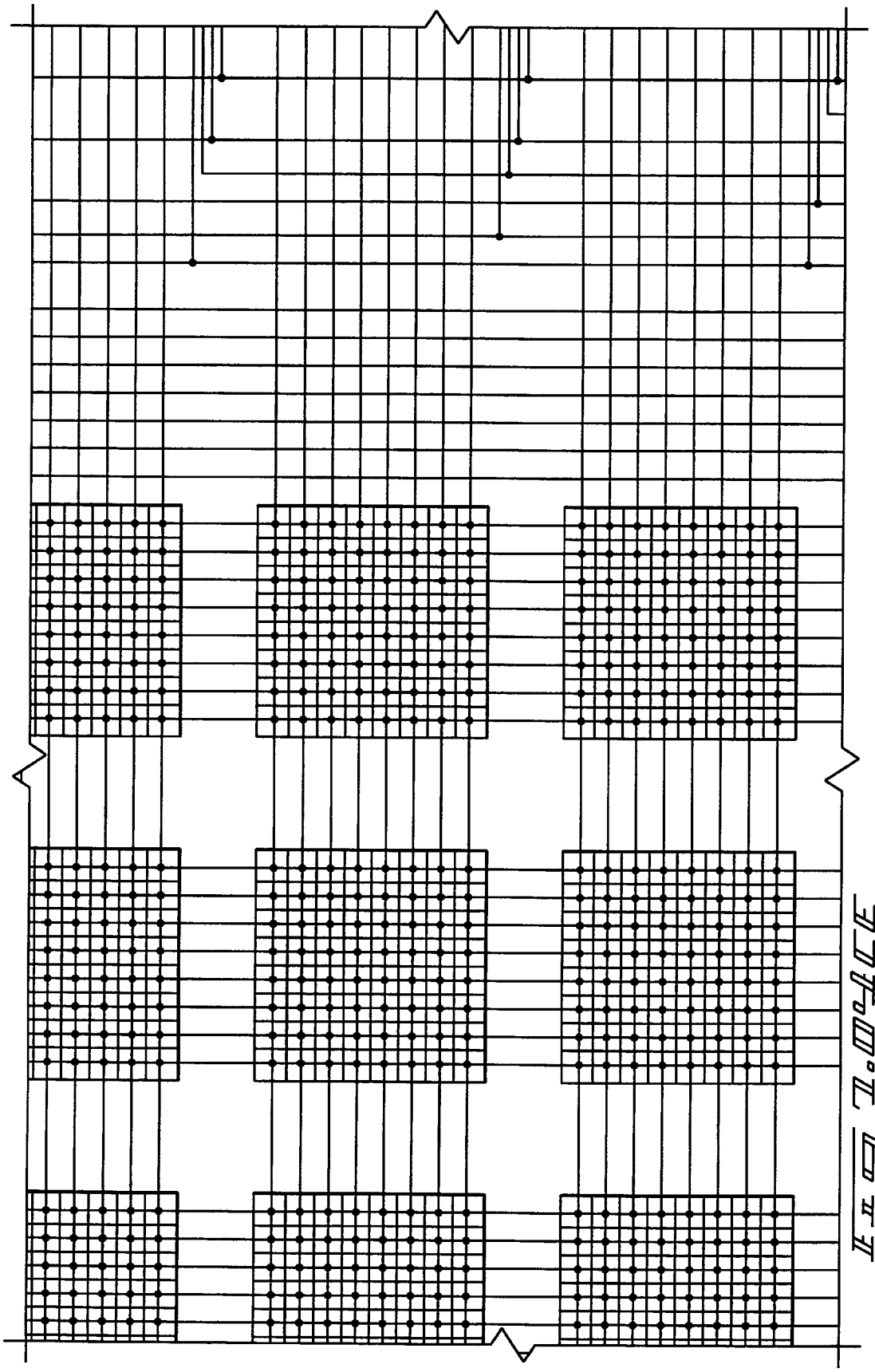
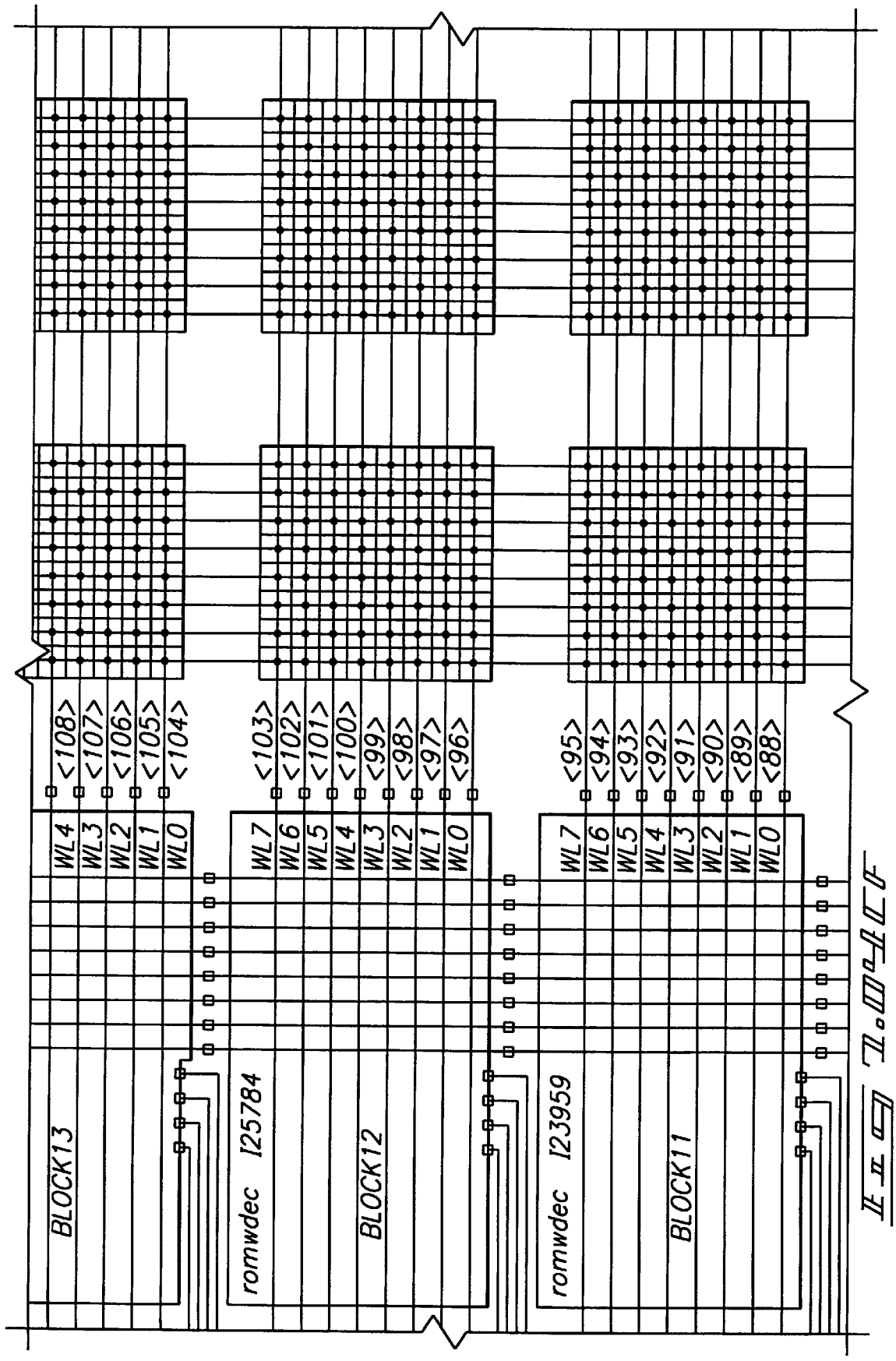


FIG 3048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WL4 WL3 WL2 WL1 WL0
WL7 WL6 WL5 WL4 WL3 WL2 WL1 WL0
WL7 WL6 WL5 WL4 WL3 WL2 WL1 WL0
BLOCK13
romwdec I25784
BLOCK12
romwdec I23959
BLOCK11

Fig. 59

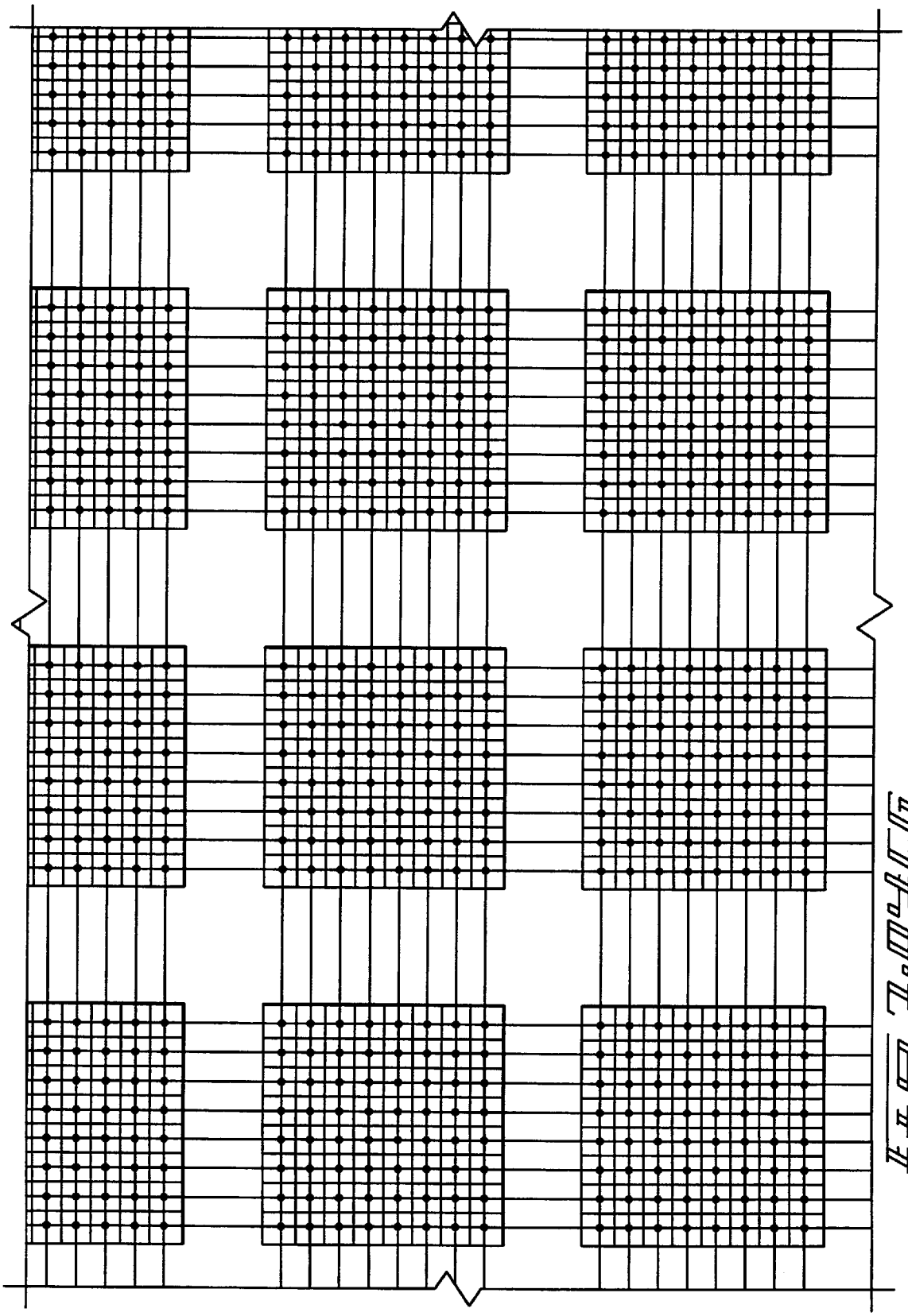


FIG. 7,600'L

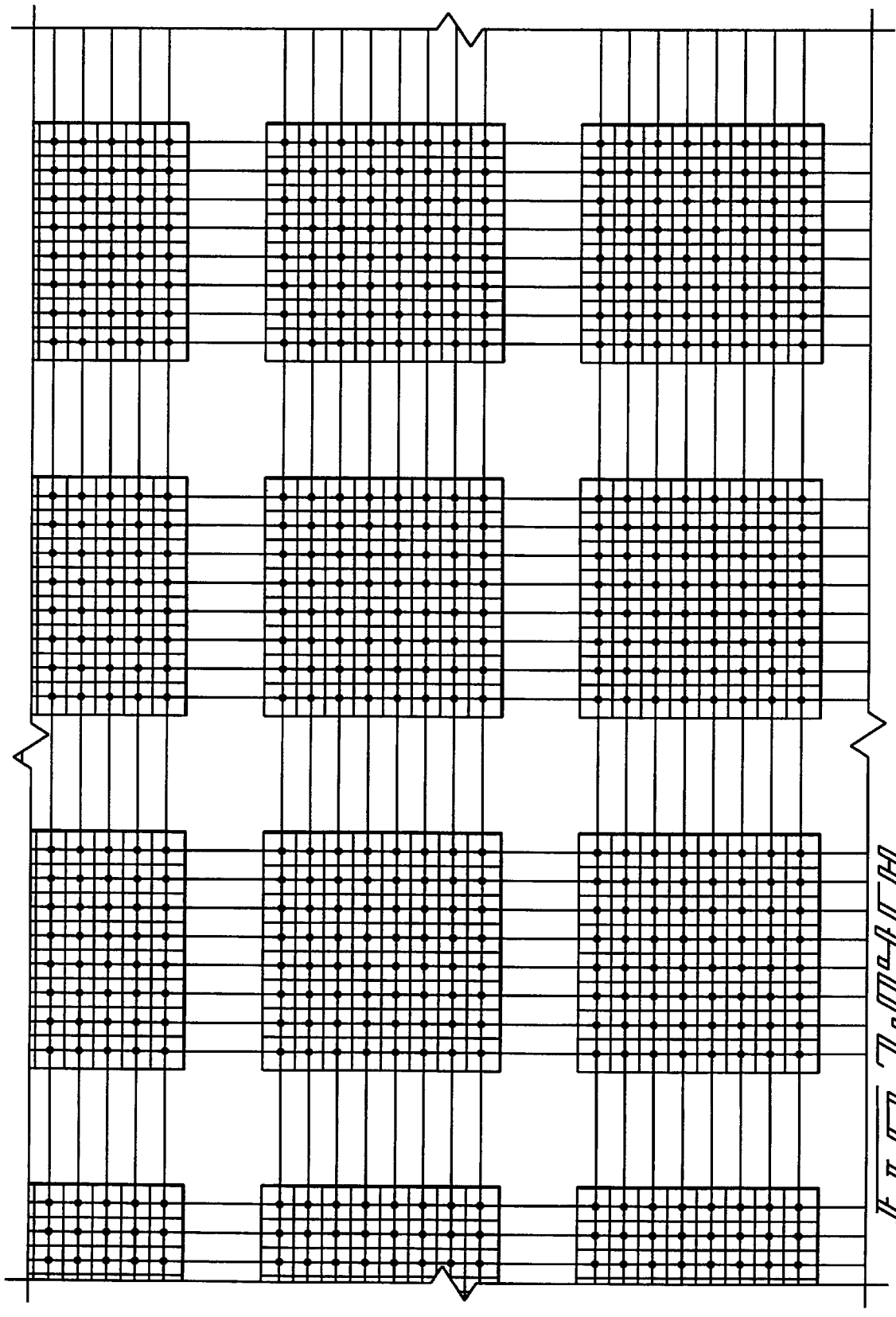


FIG. 325

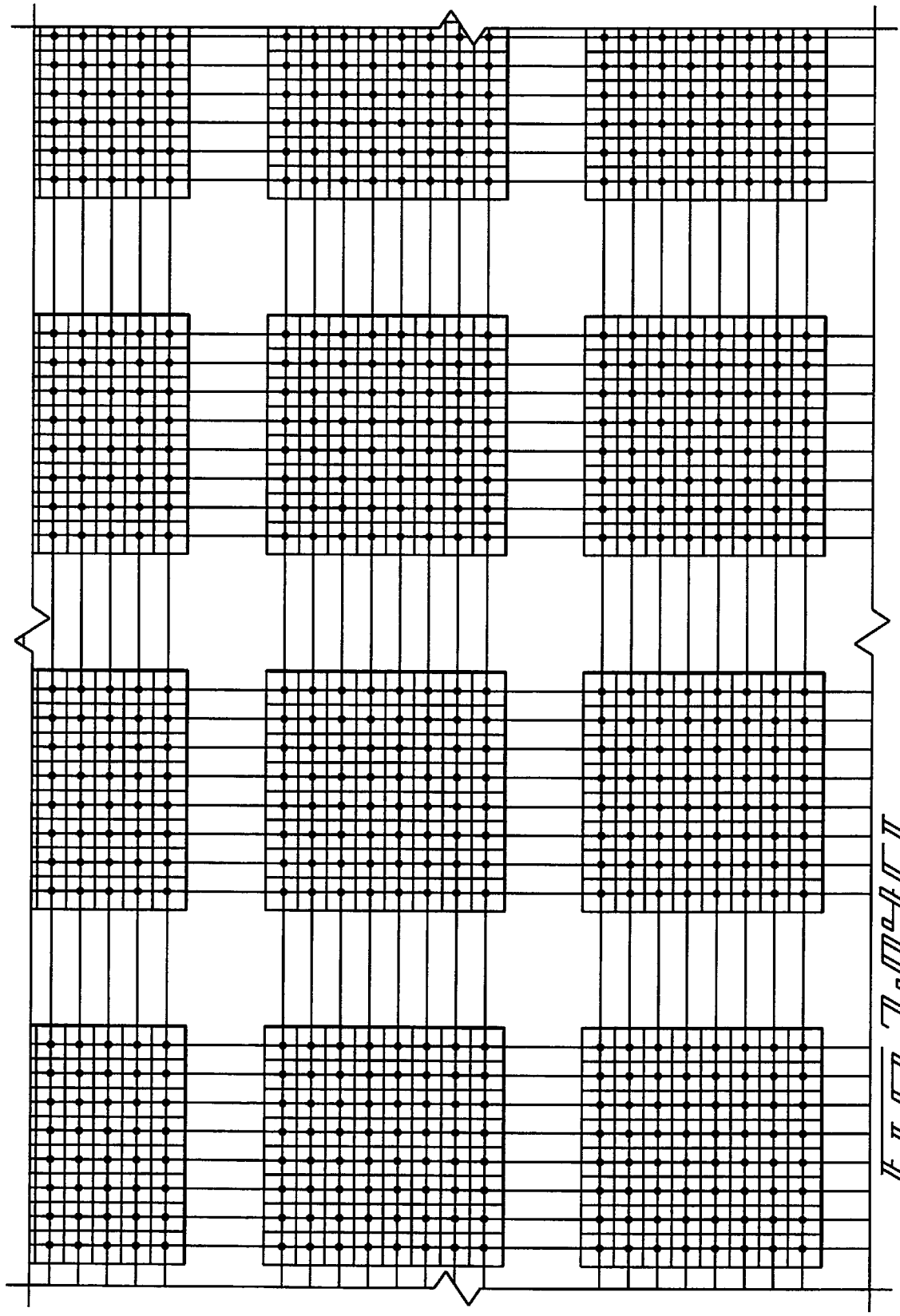


FIG. 1378

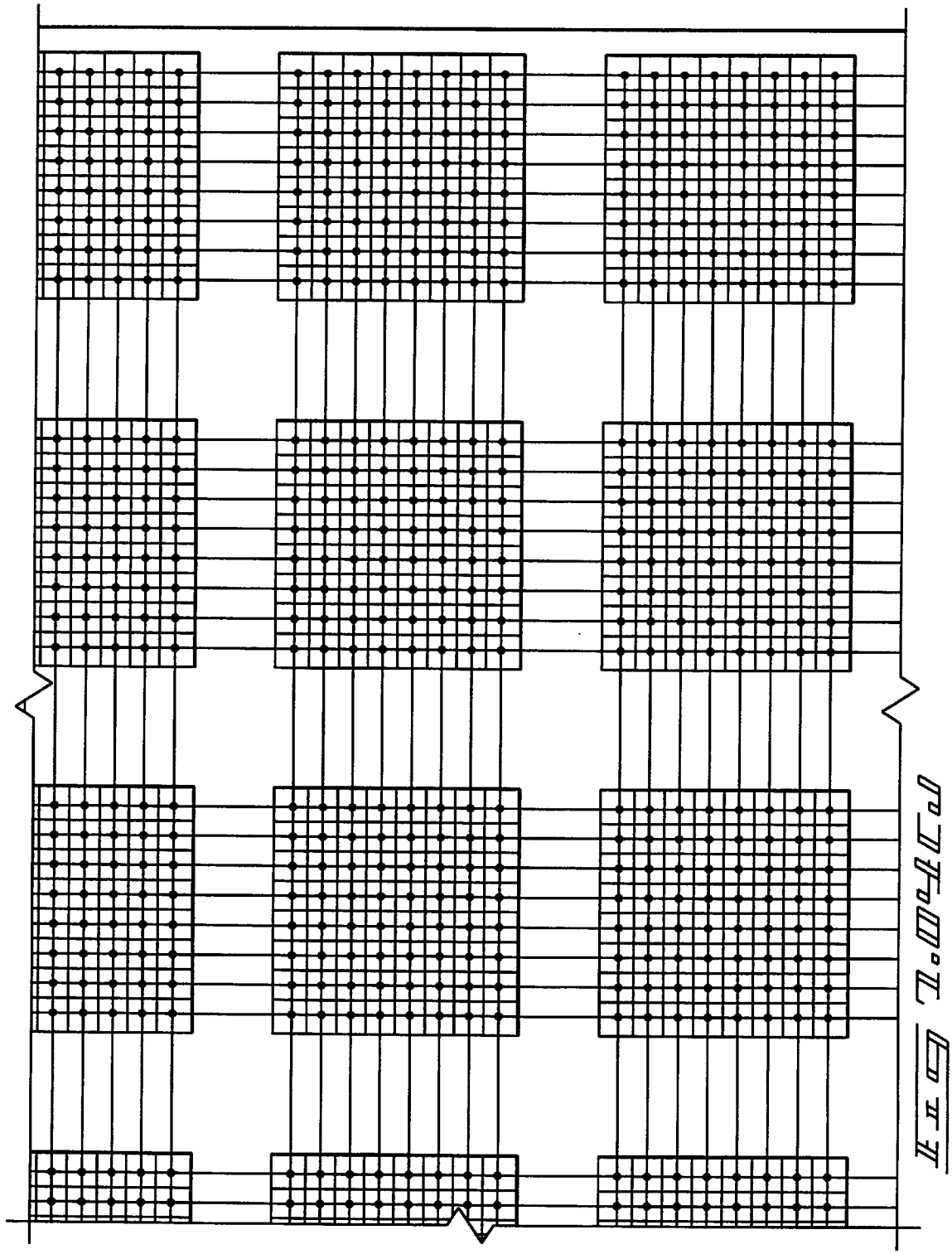


FIG. 327

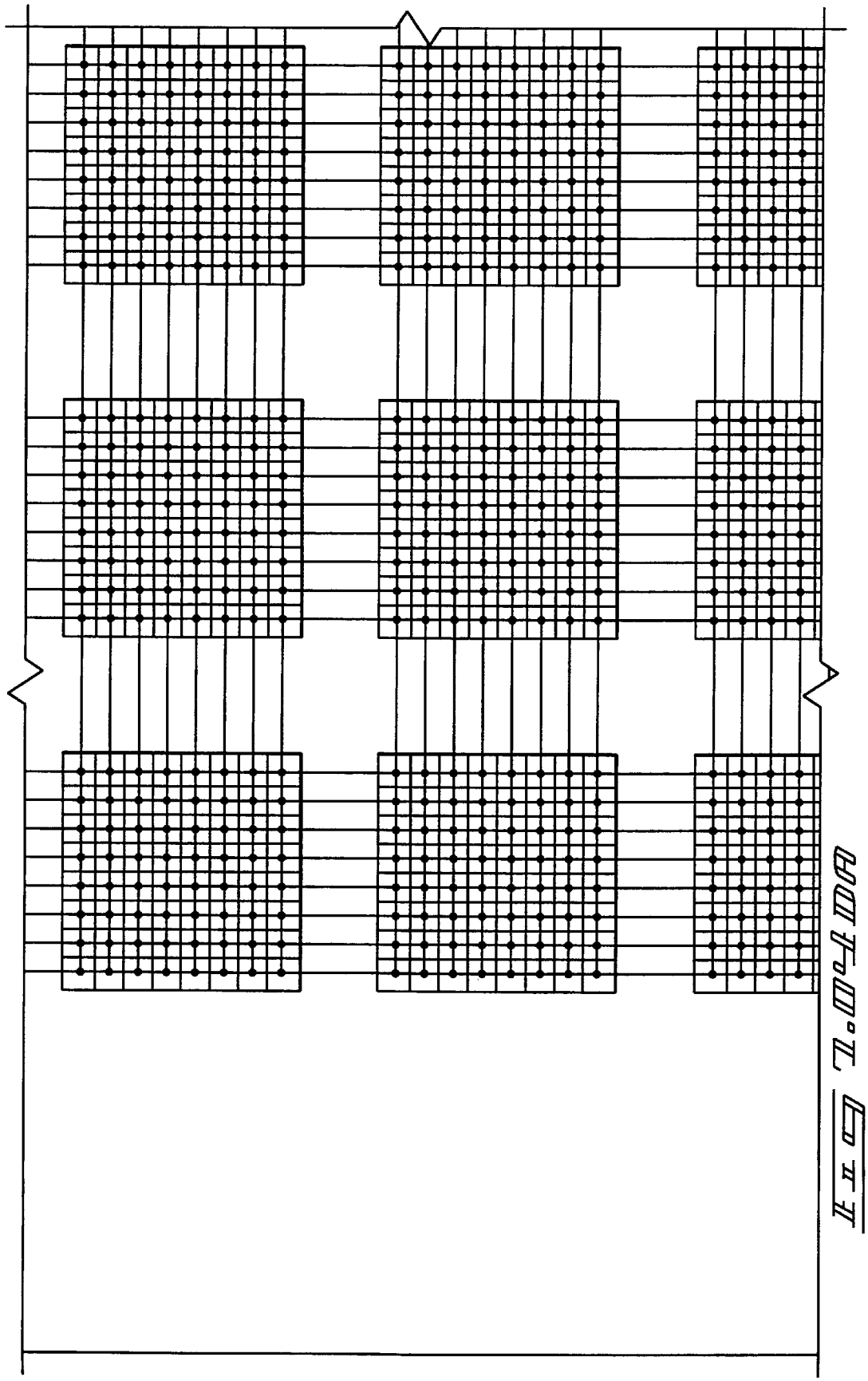


FIG. 328

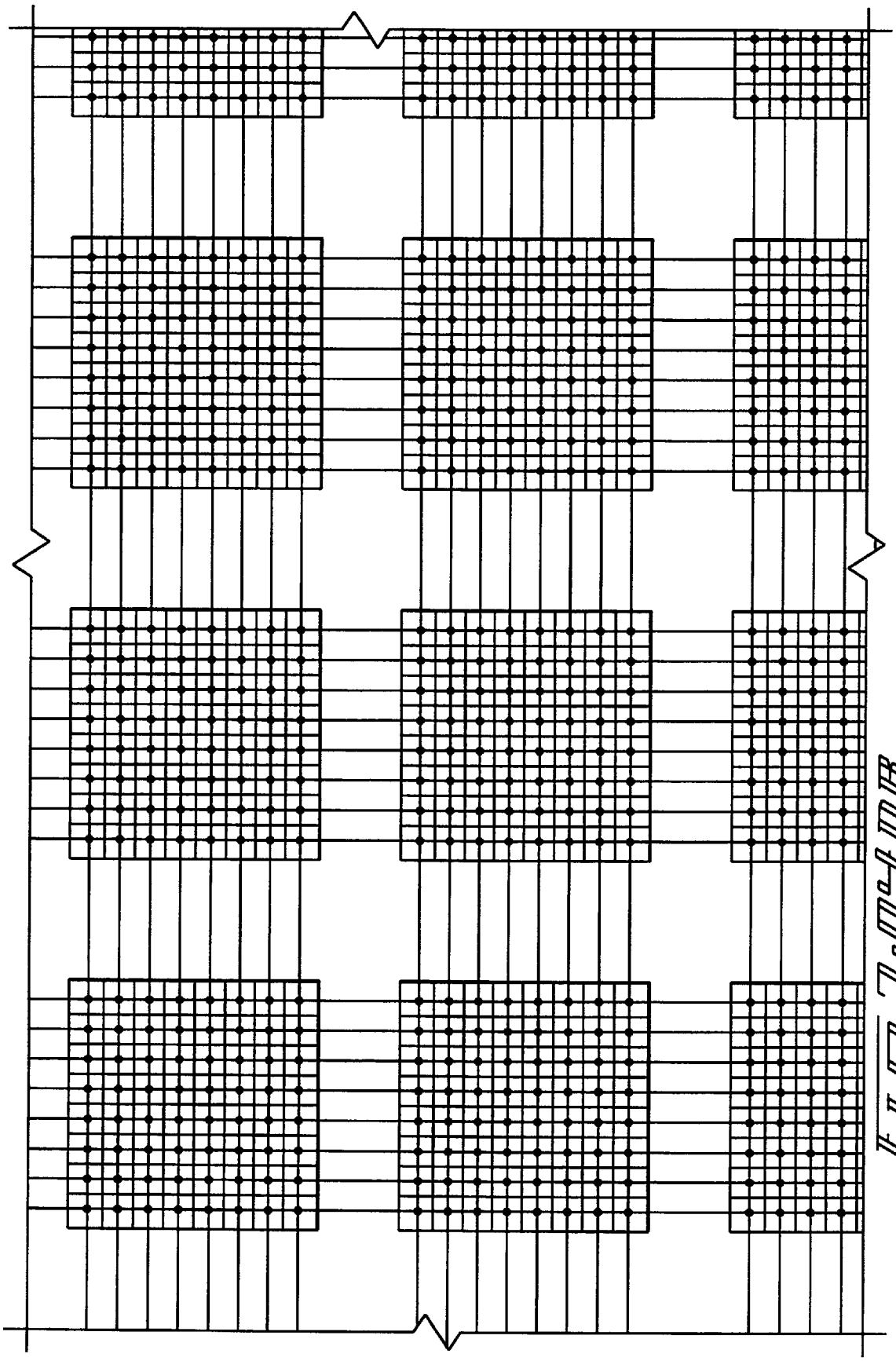


FIG. 404B

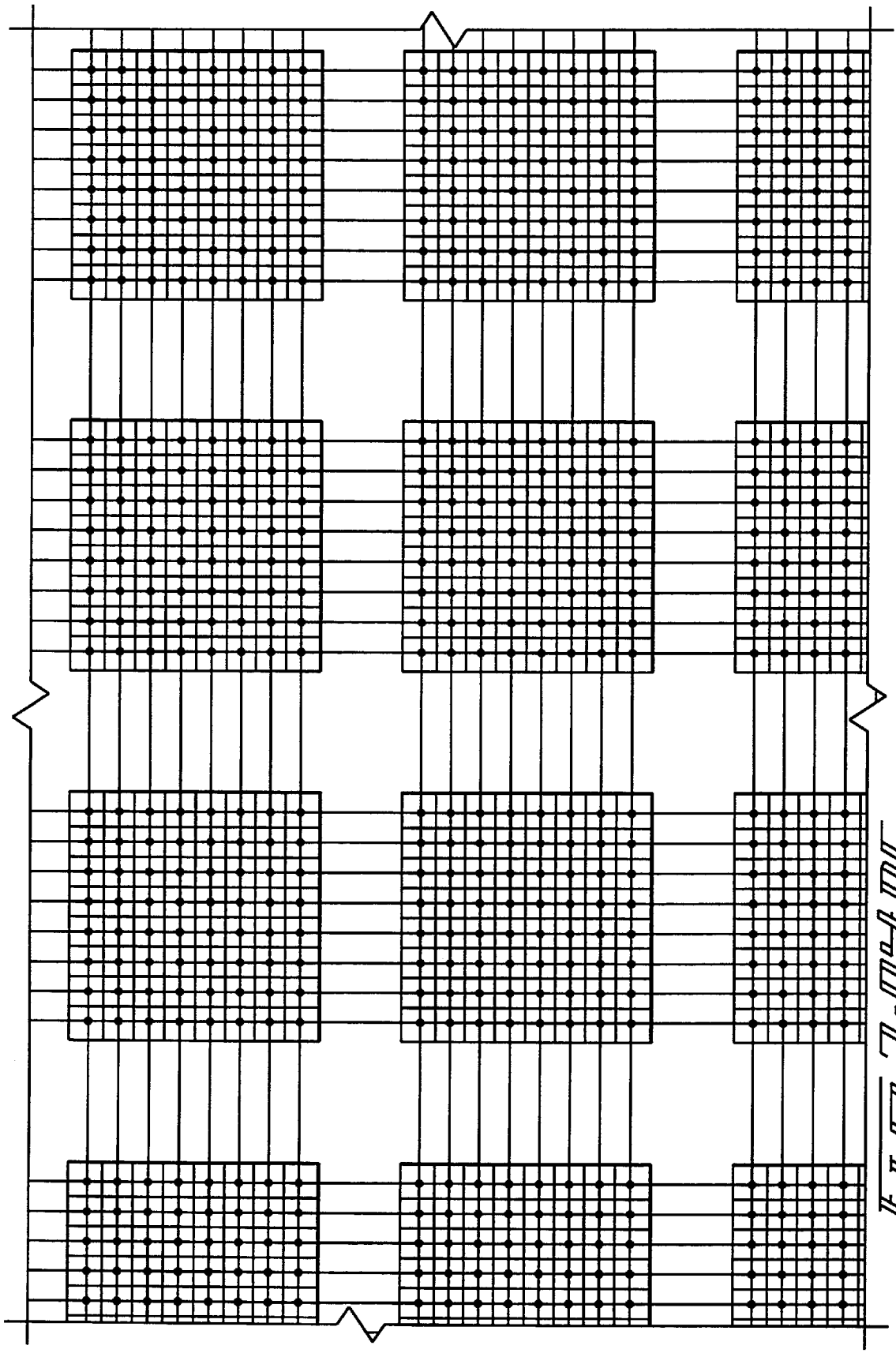


FIG. 704.0L

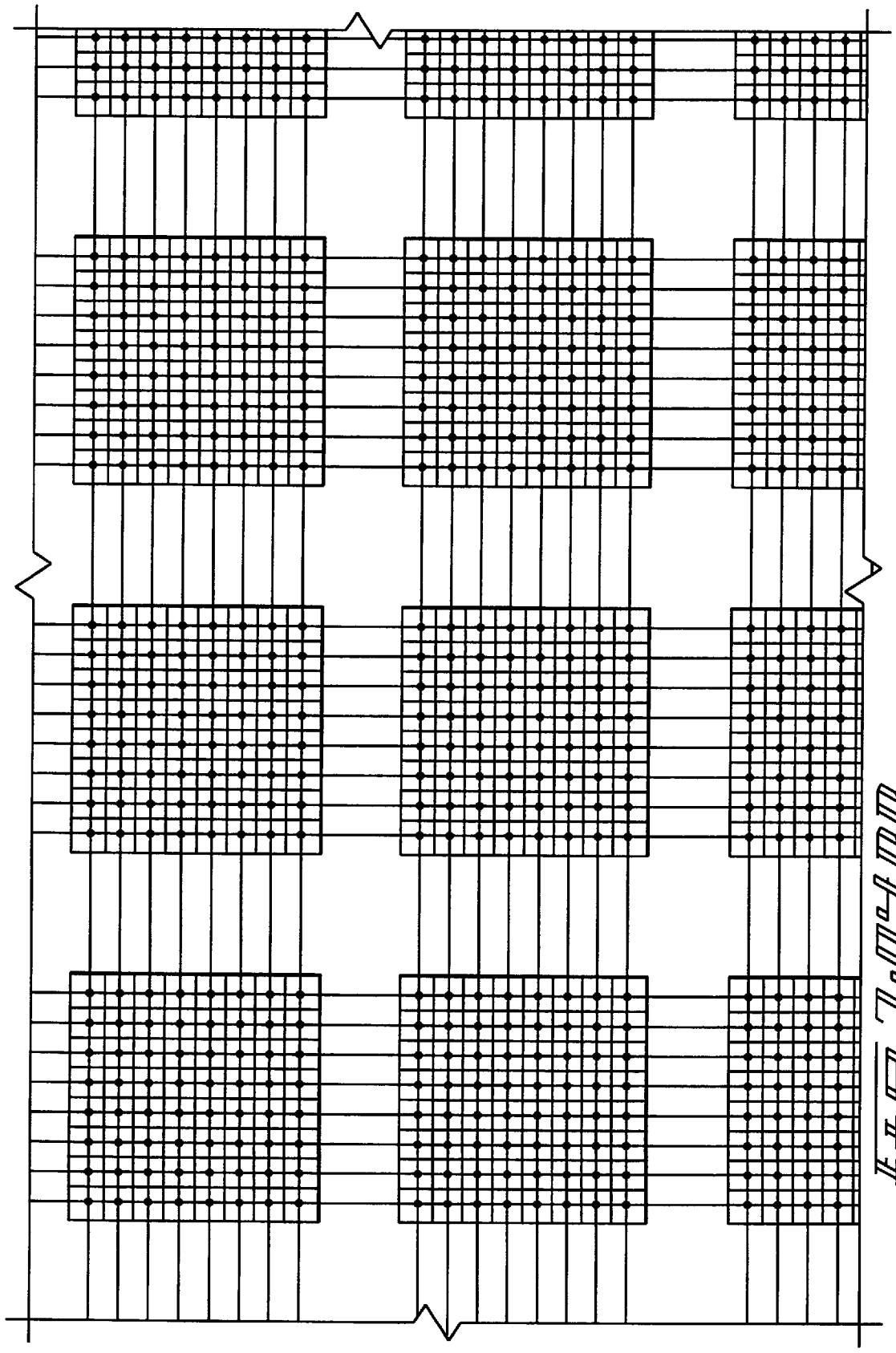


FIG. 640L

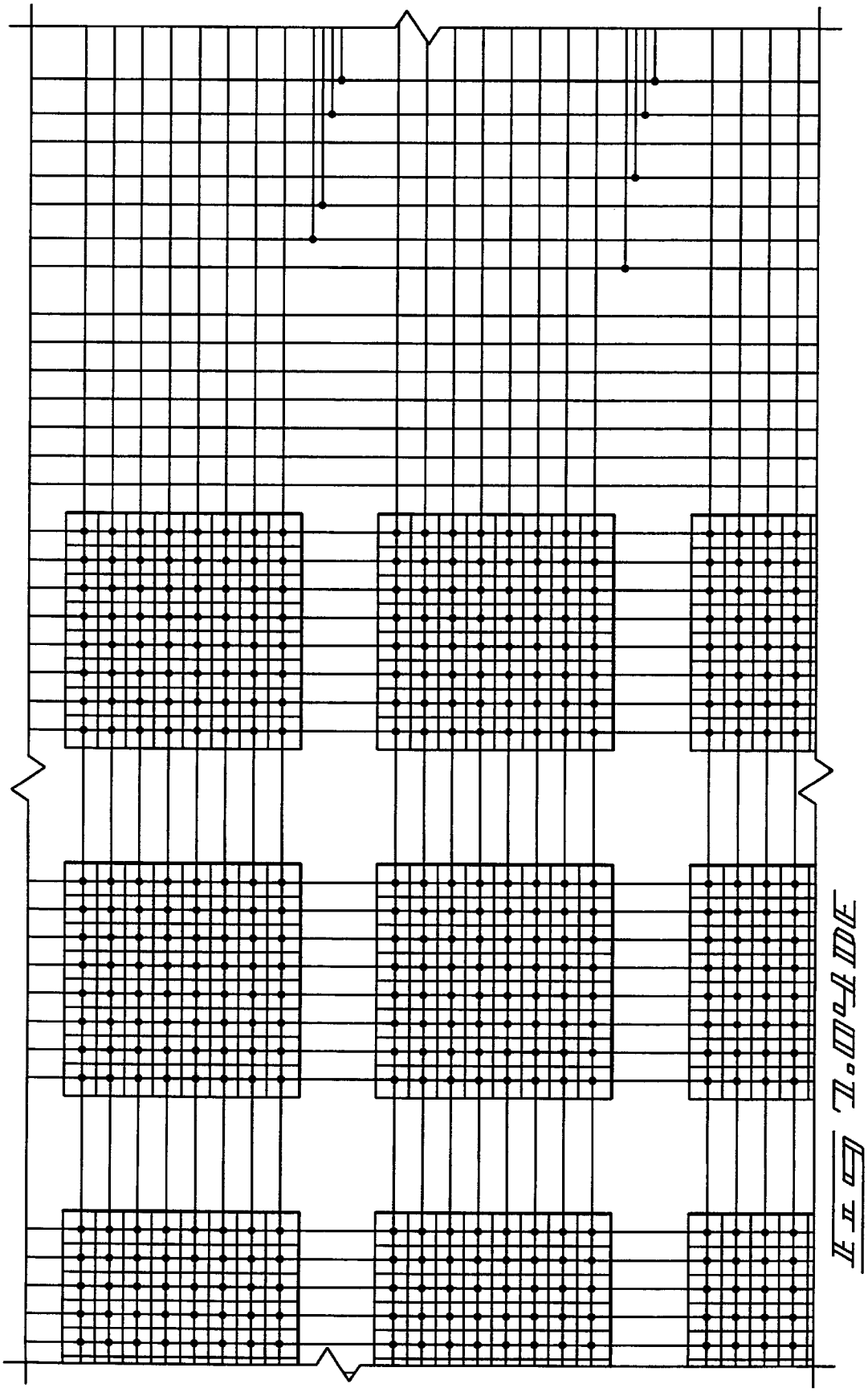
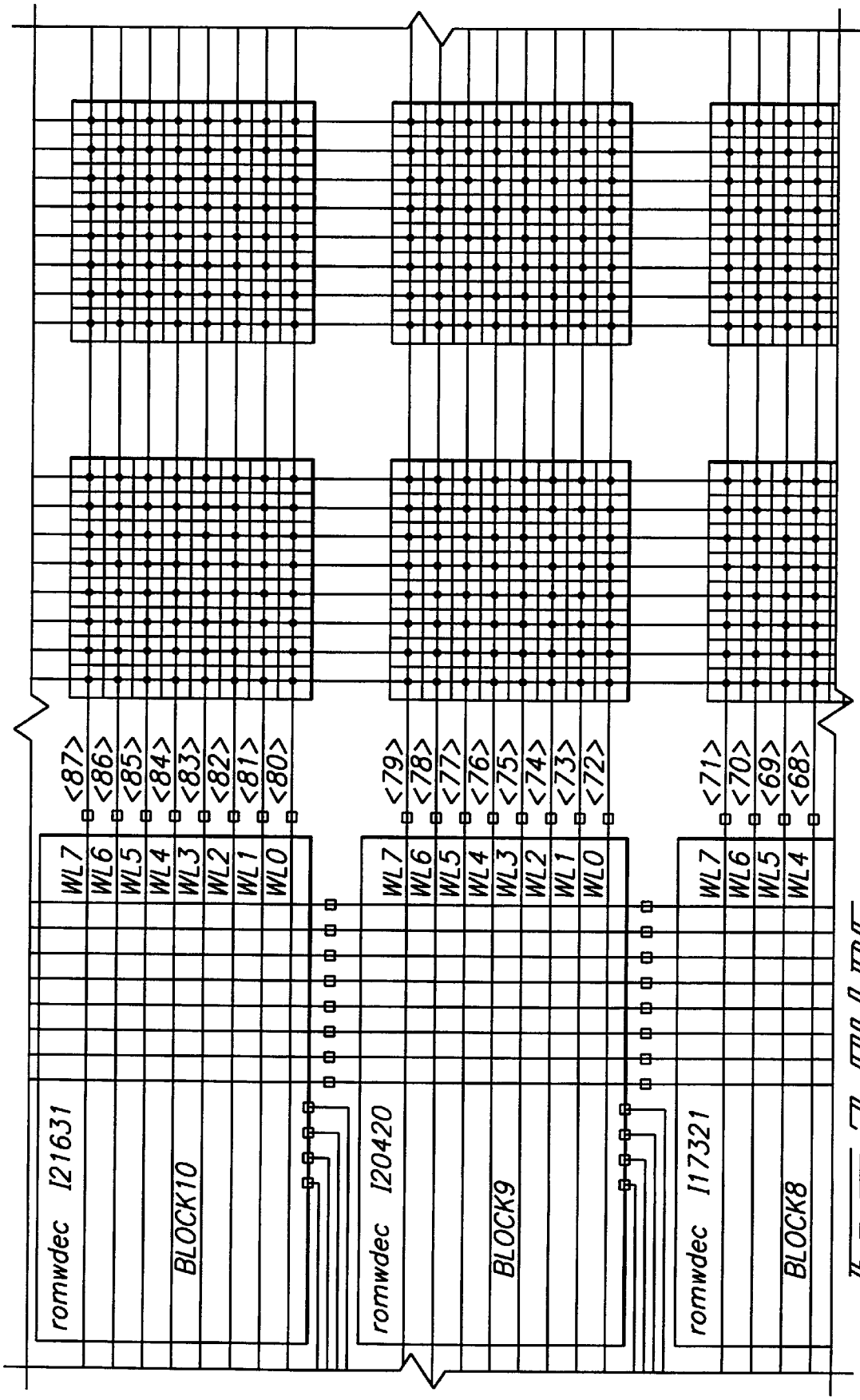


FIG. 332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romwdec I20420
BLOCK9
romwdec I17321
BLOCK8
WL7
WL6
WL5
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FIG. 4Fa0.4Fa0

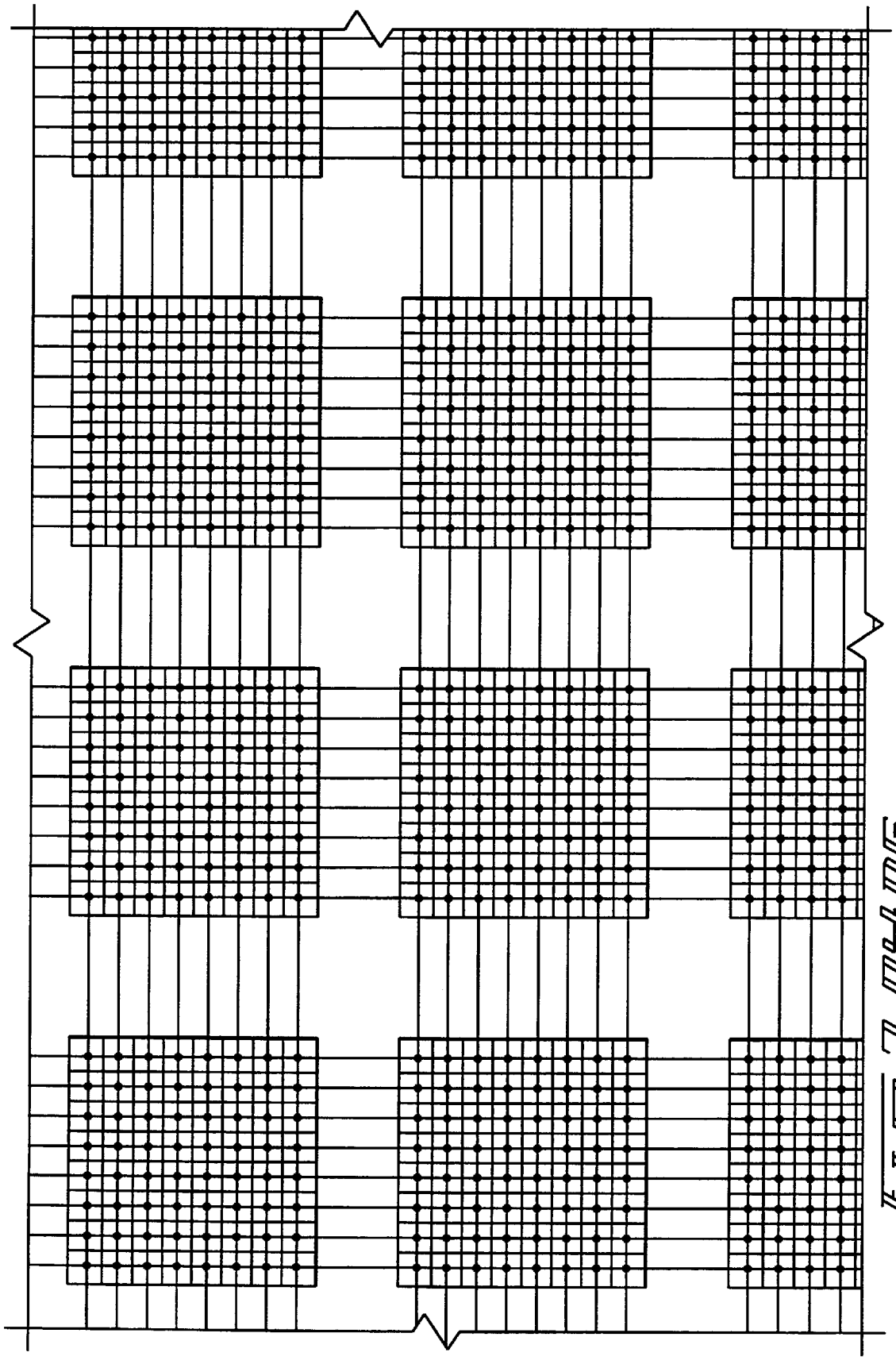


FIG 1,004

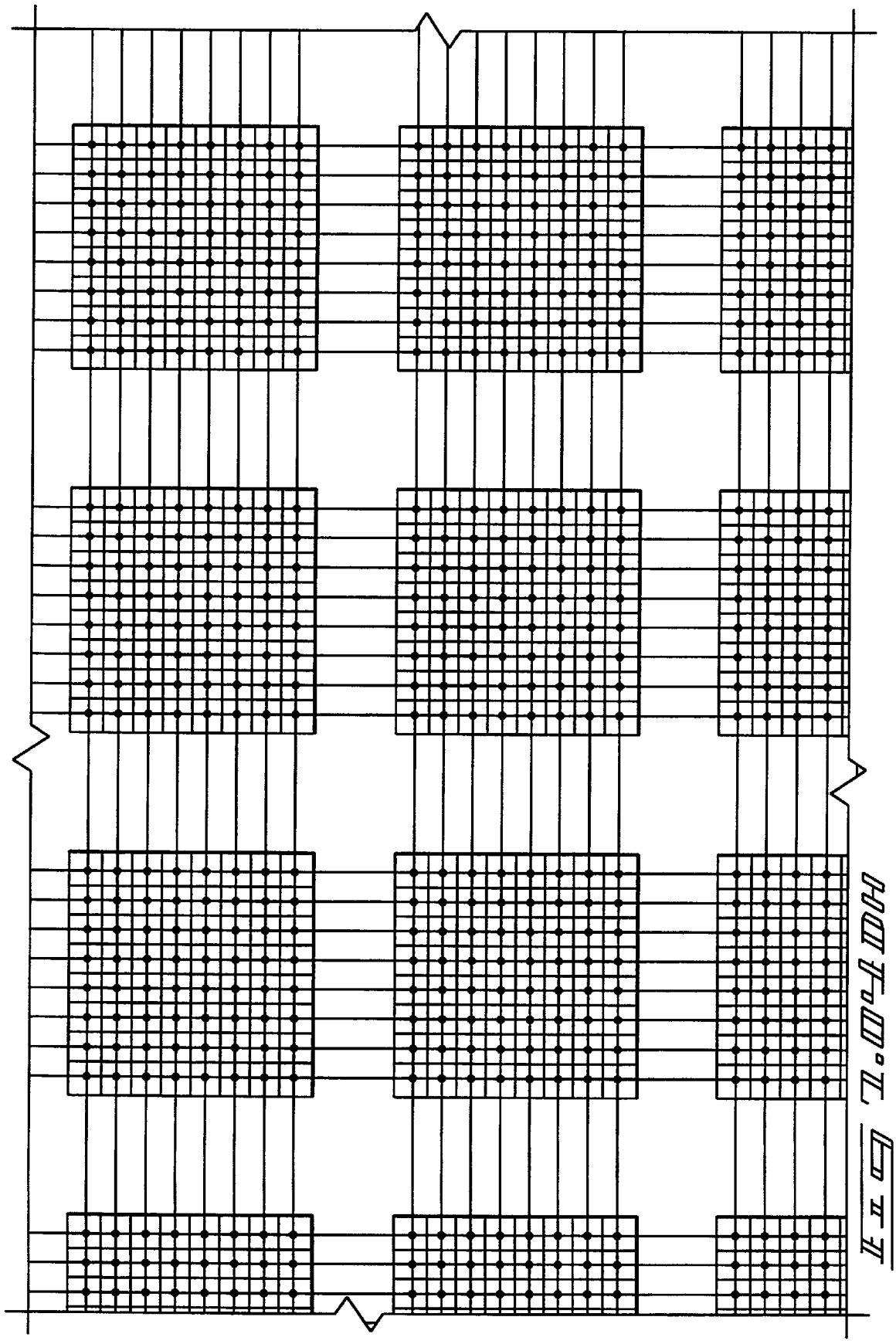


FIG. 400L

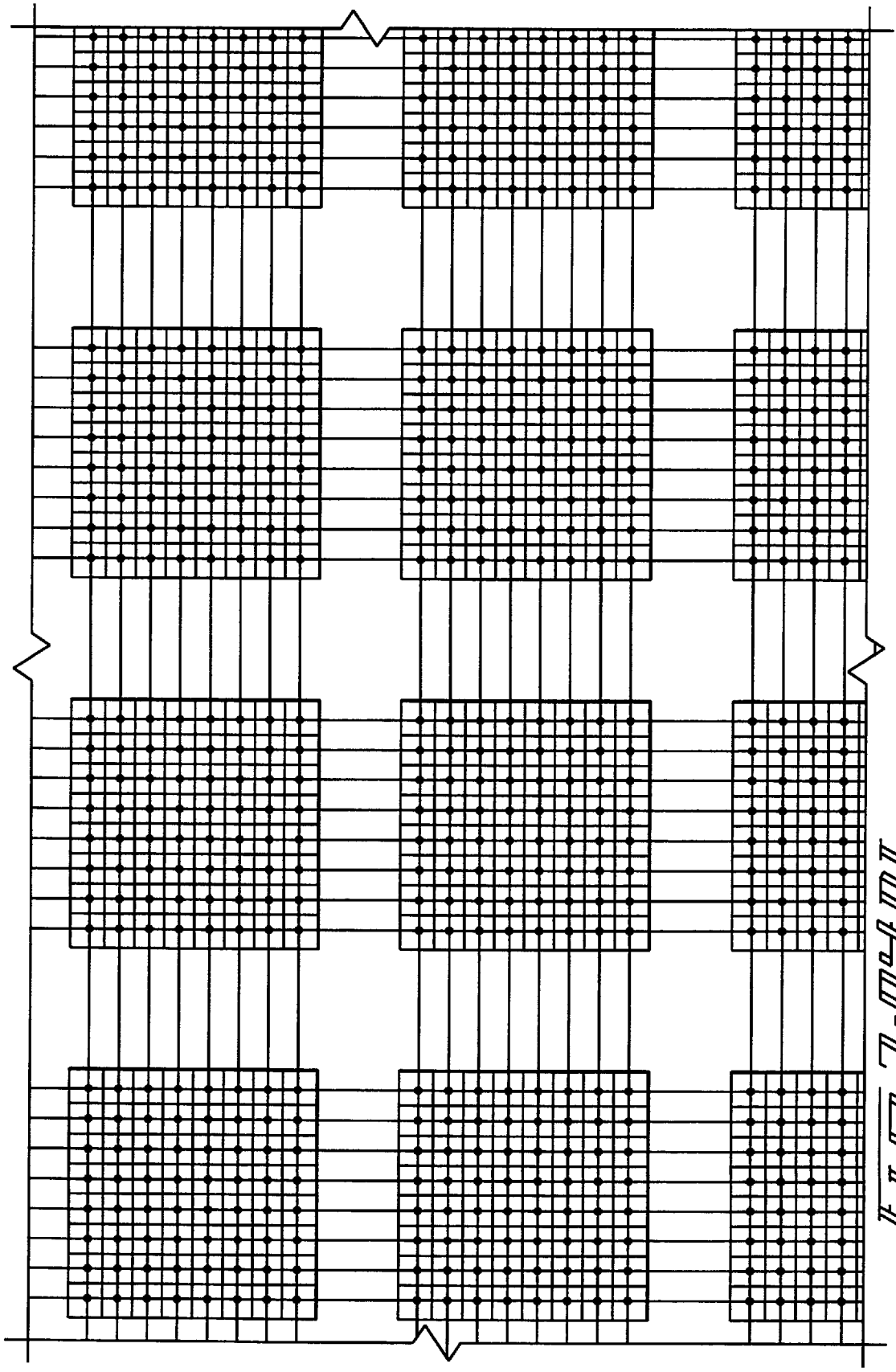


FIG. 6,040A

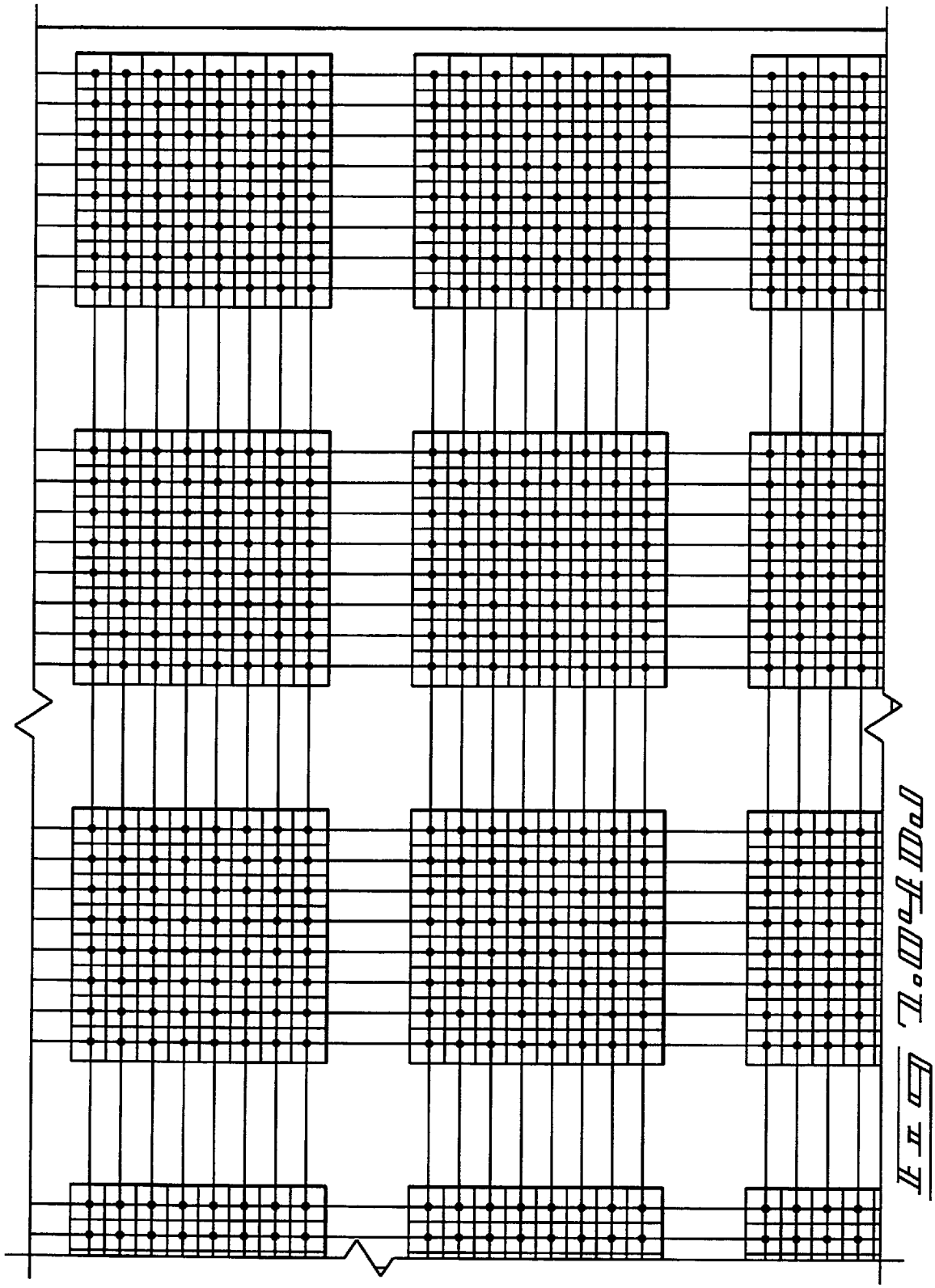


FIG. 337

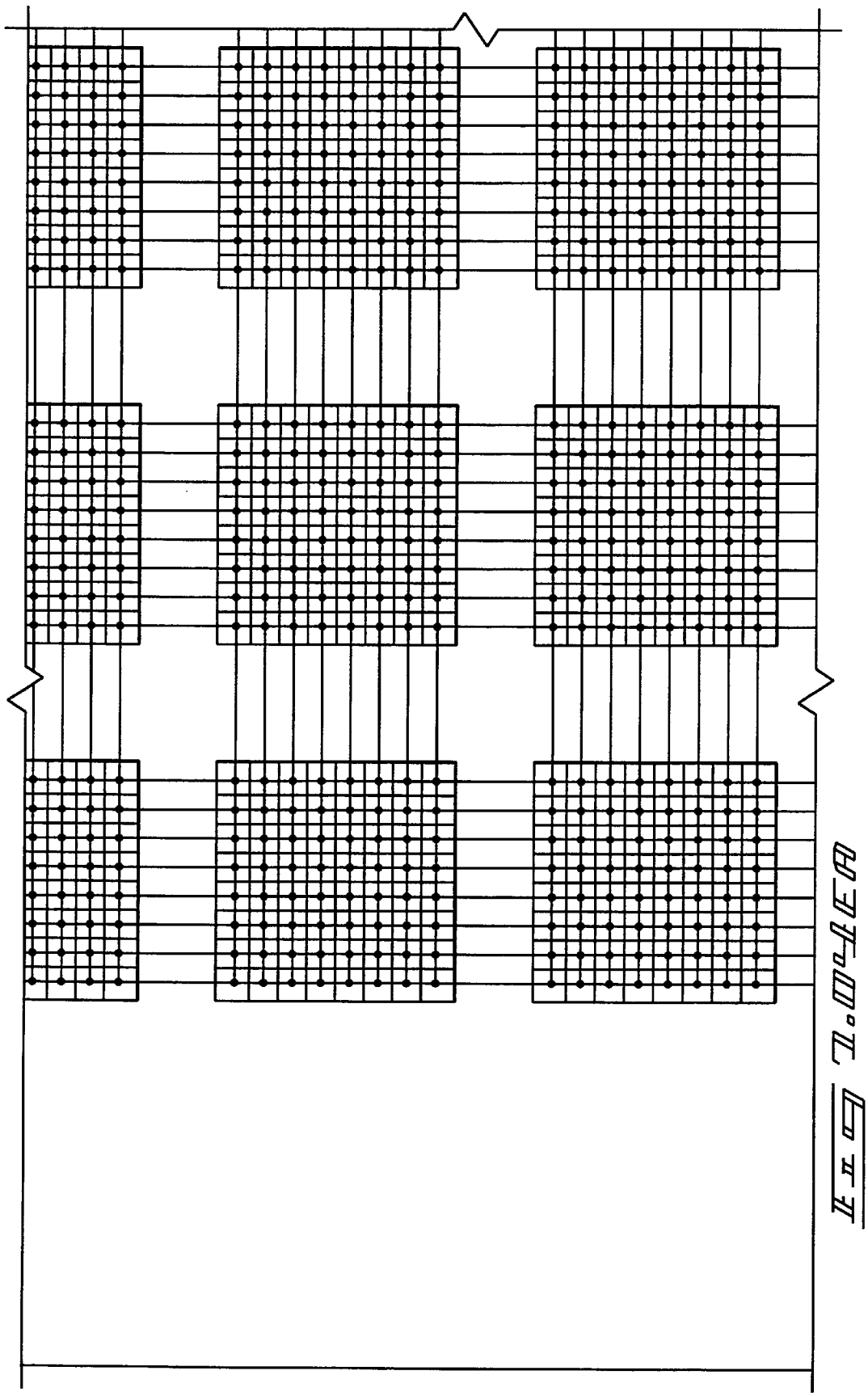


FIG. 1.0AEA

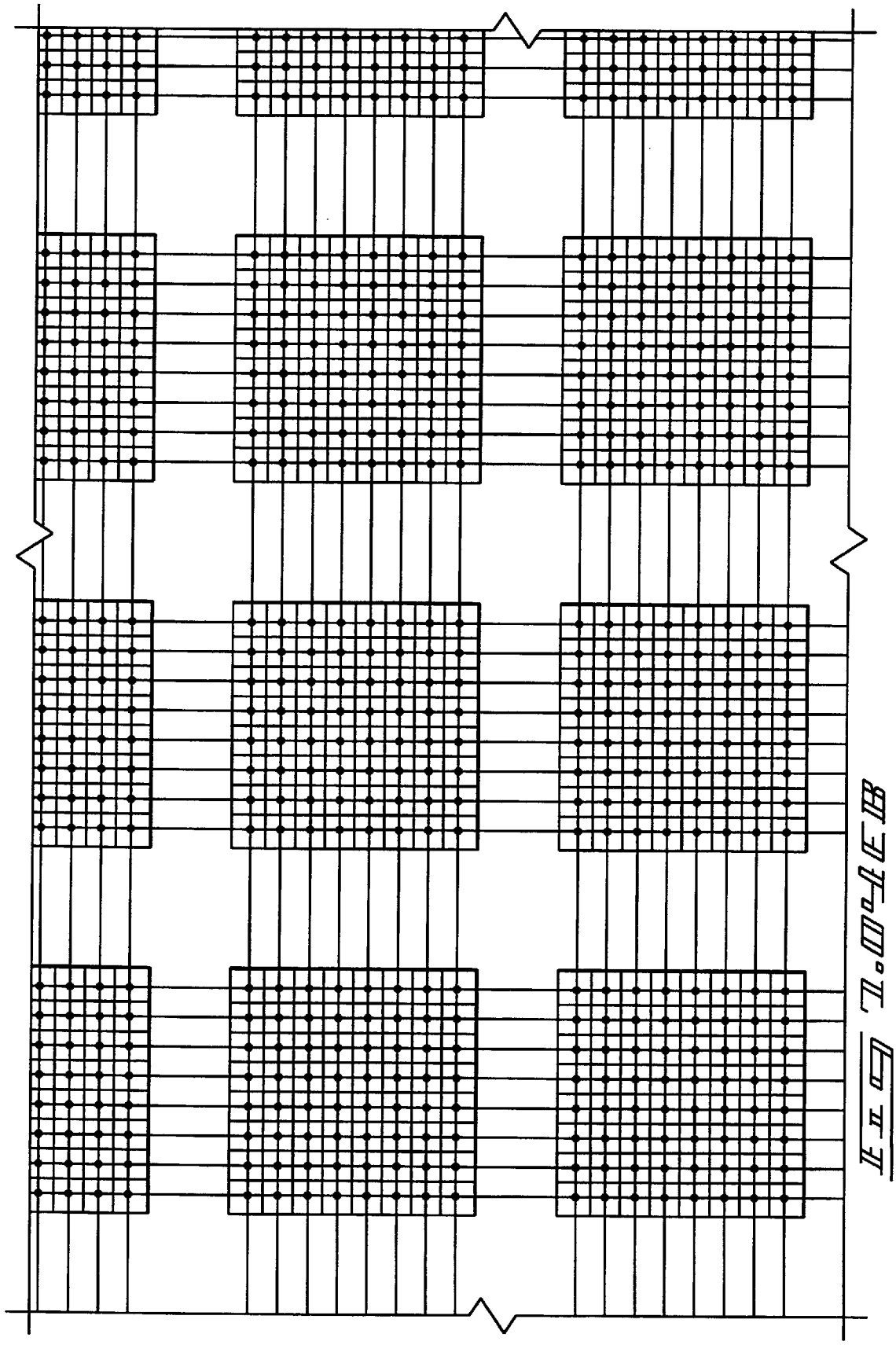


FIG 7,047B

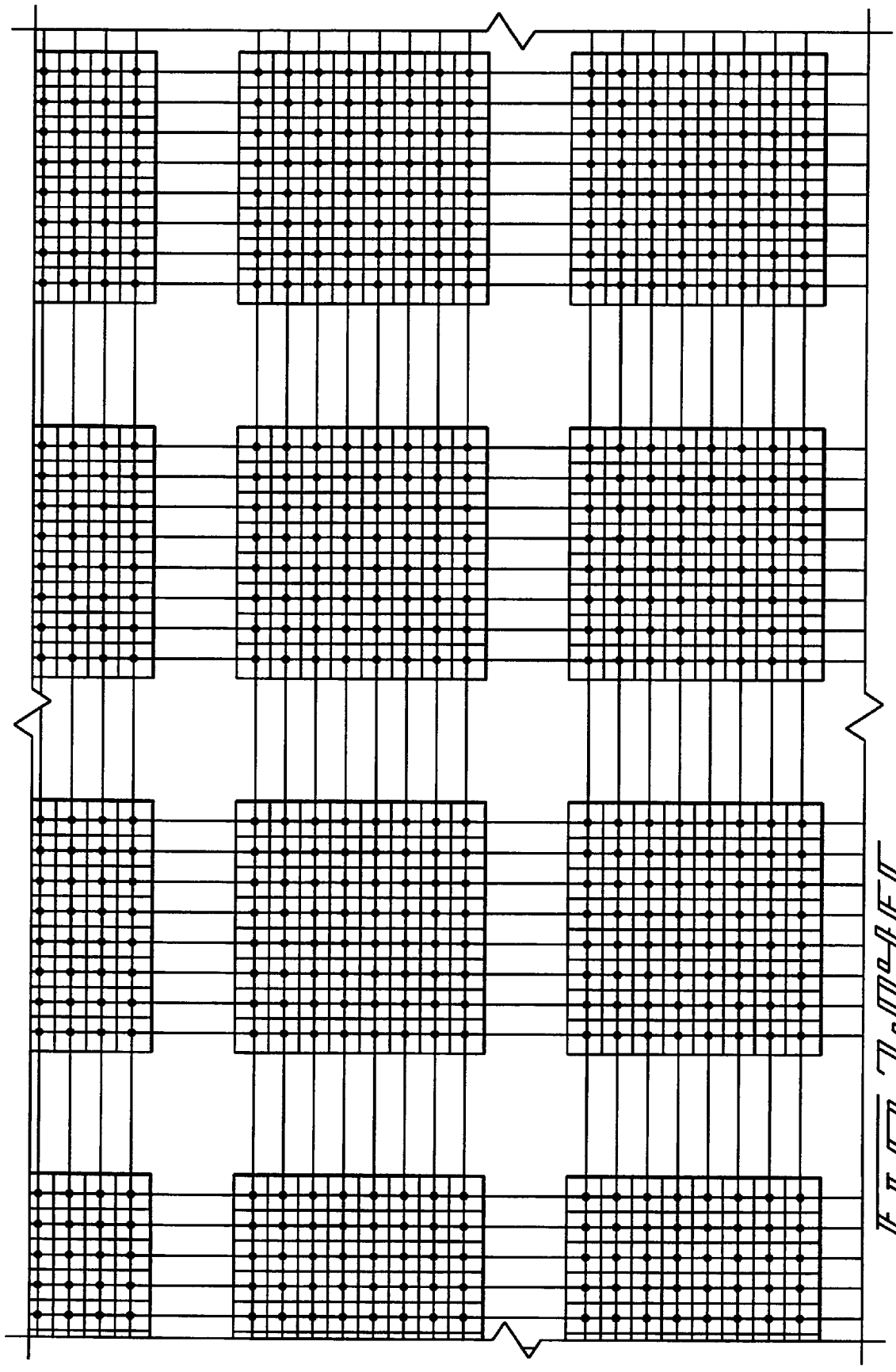


FIG. 340

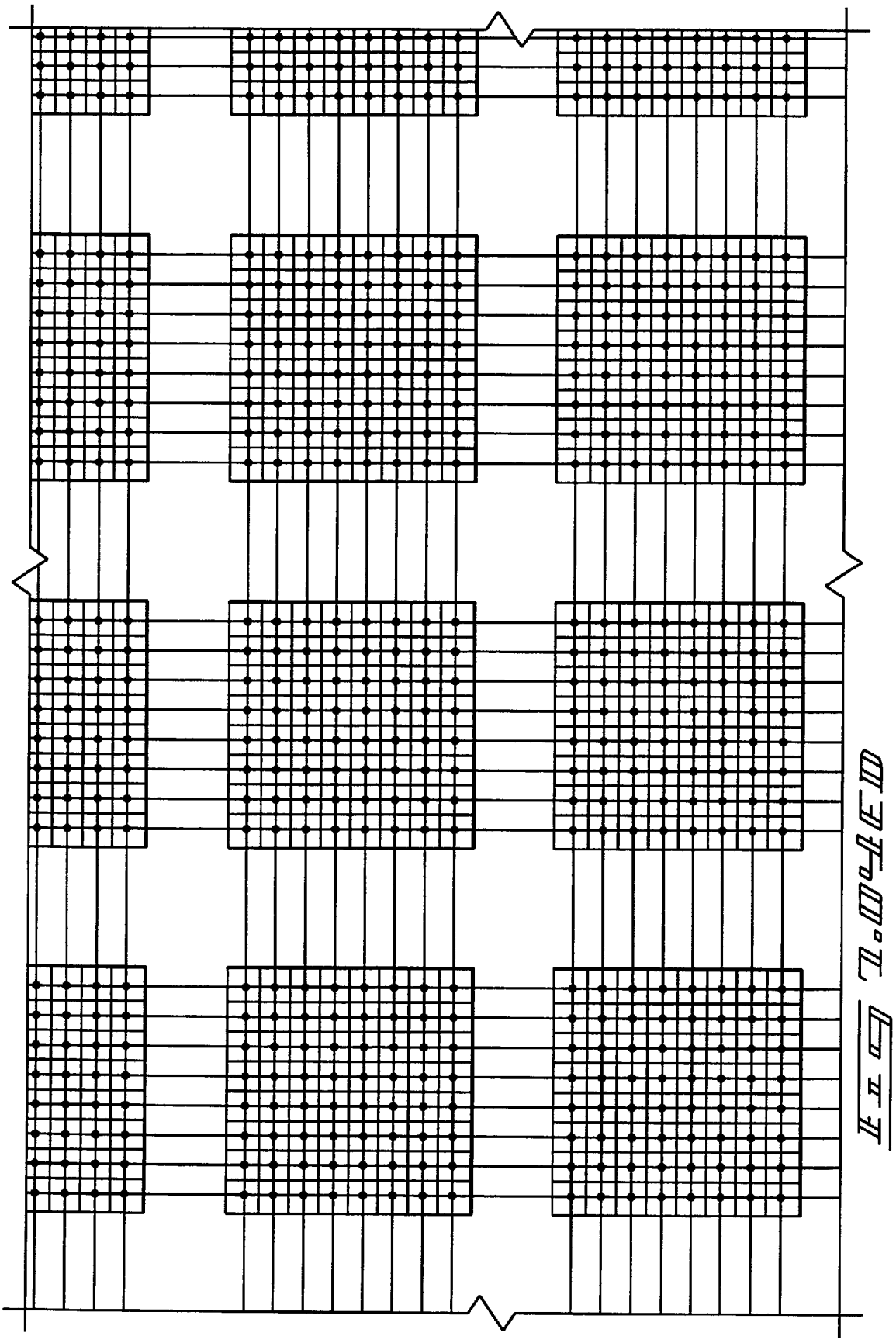


FIG. 340L

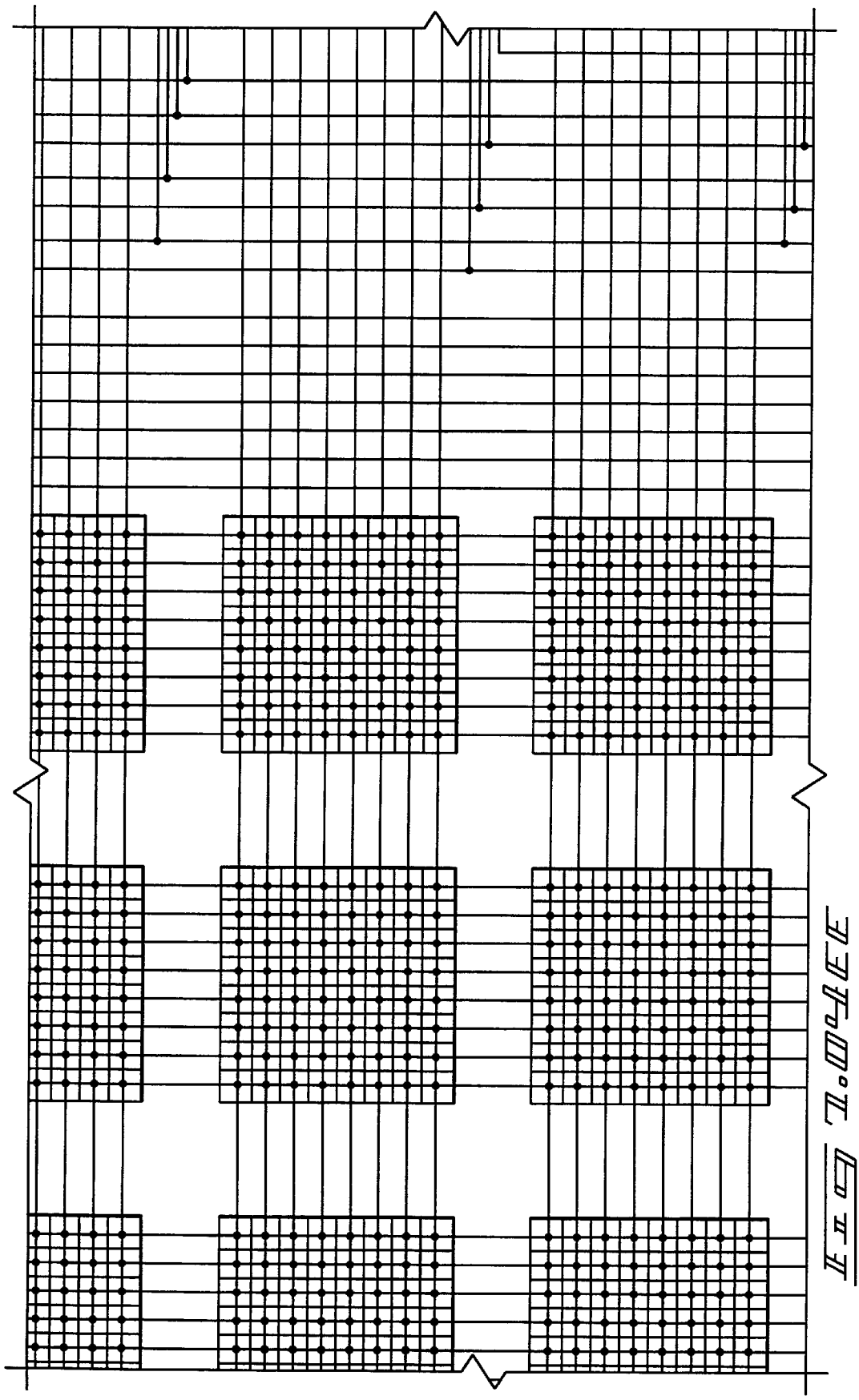
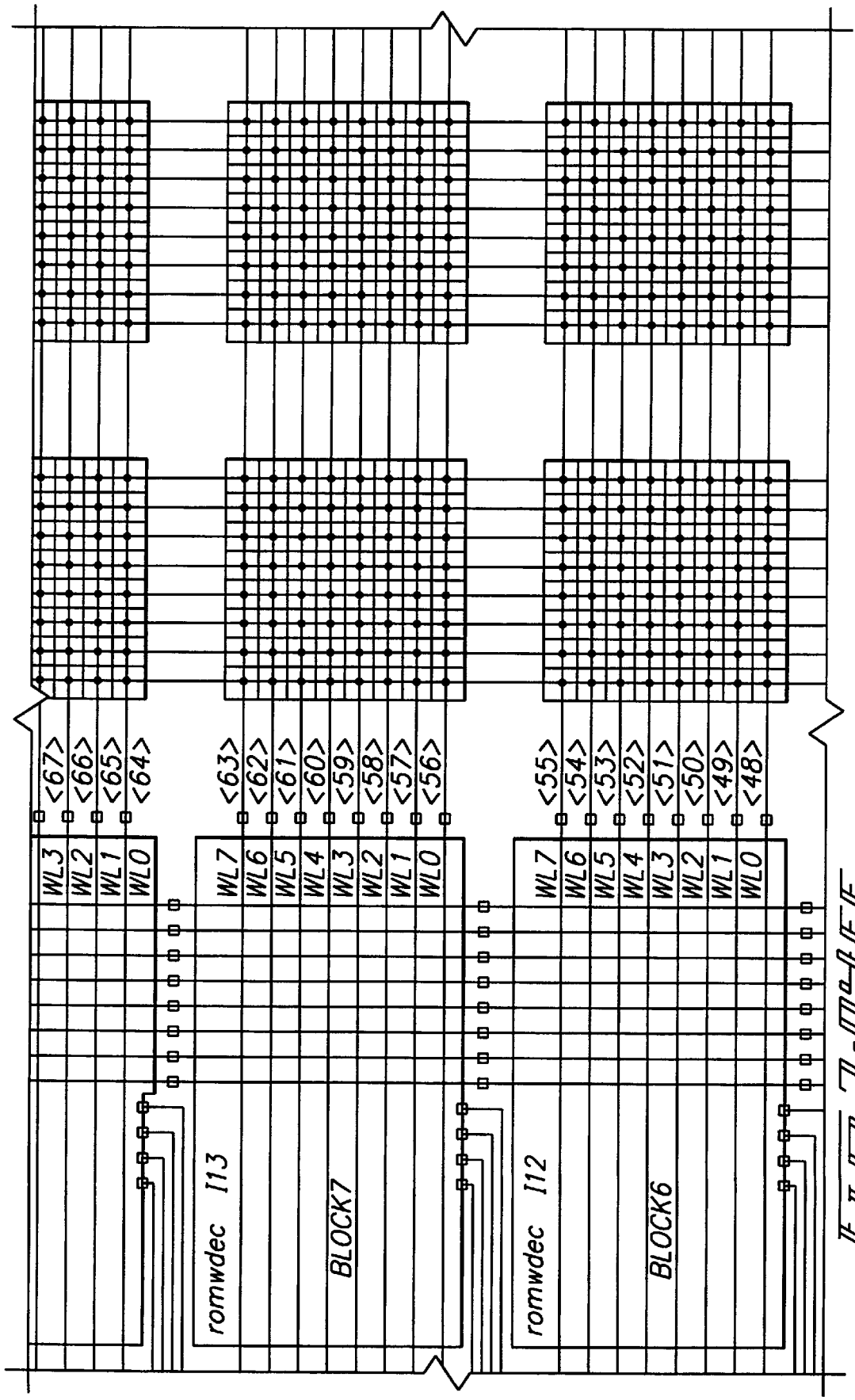


FIG. 340'L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WL3 WL2 WL1 WL0
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WL7 WL6 WL5 WL4 WL3 WL2 WL1 WL0
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WL7 WL6 WL5 WL4 WL3 WL2 WL1 WL0
romwdec I13
BLOCK7
romwdec I12
BLOCK6

Fig. 1,001E

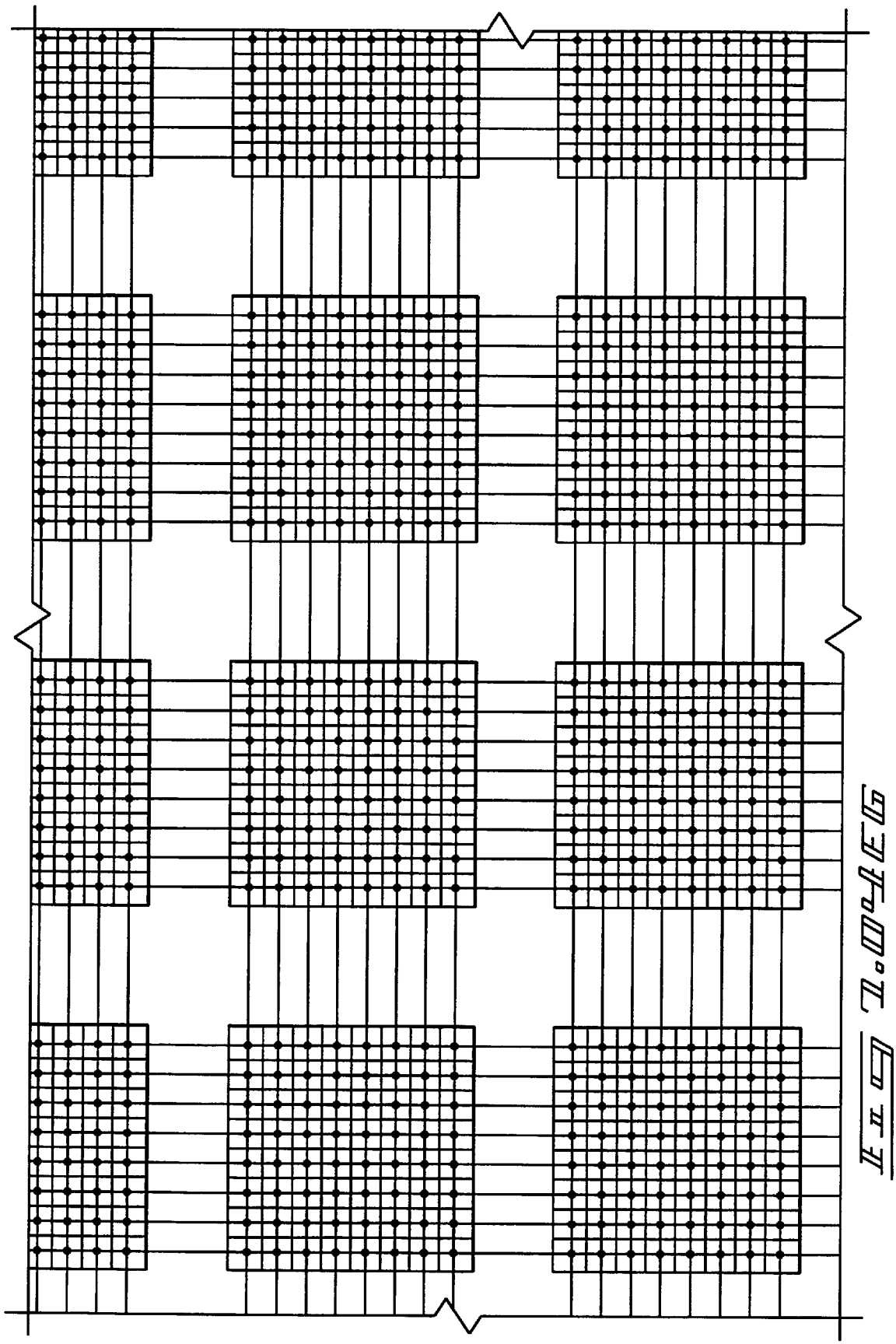


FIG. 340L

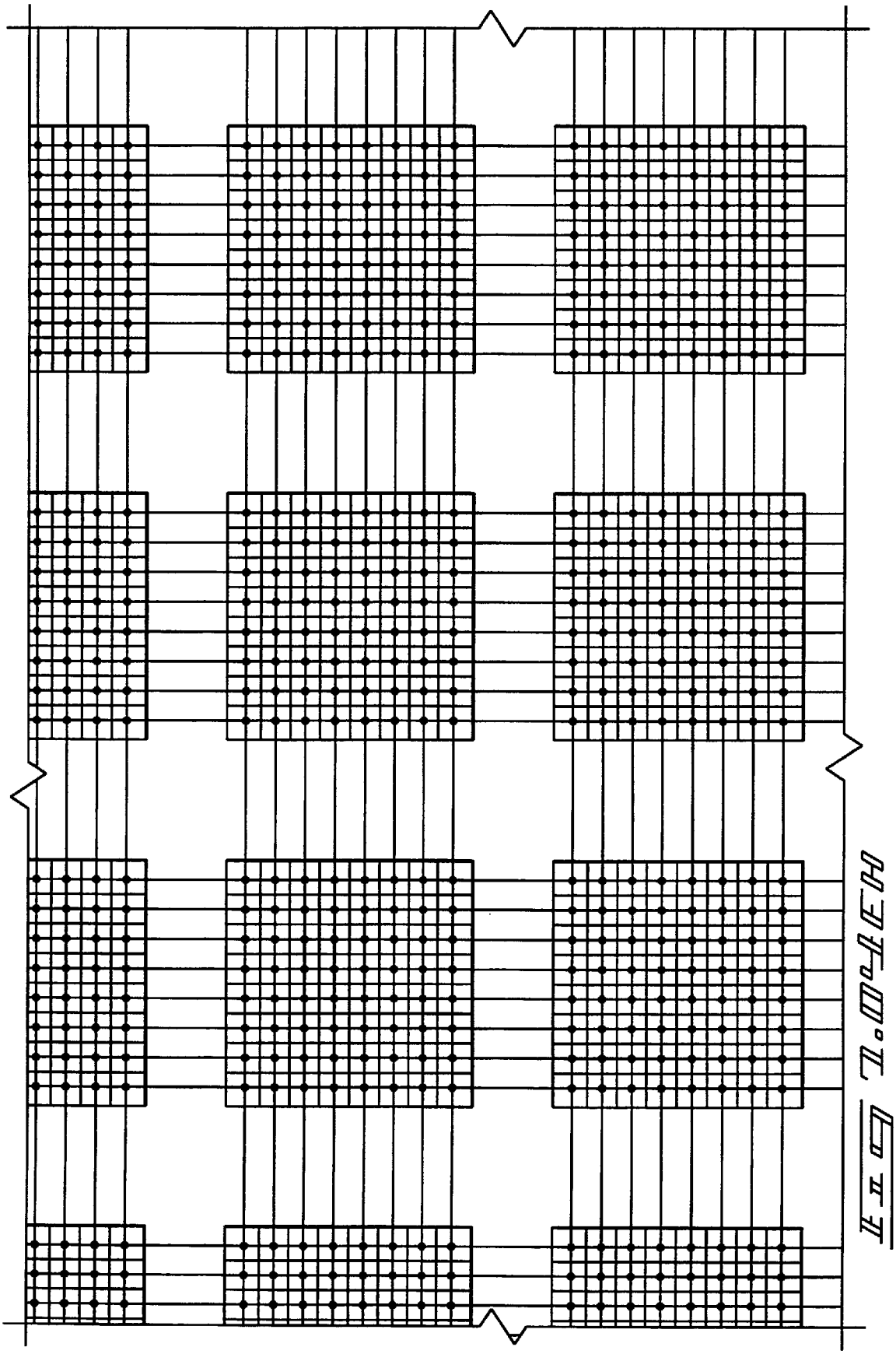
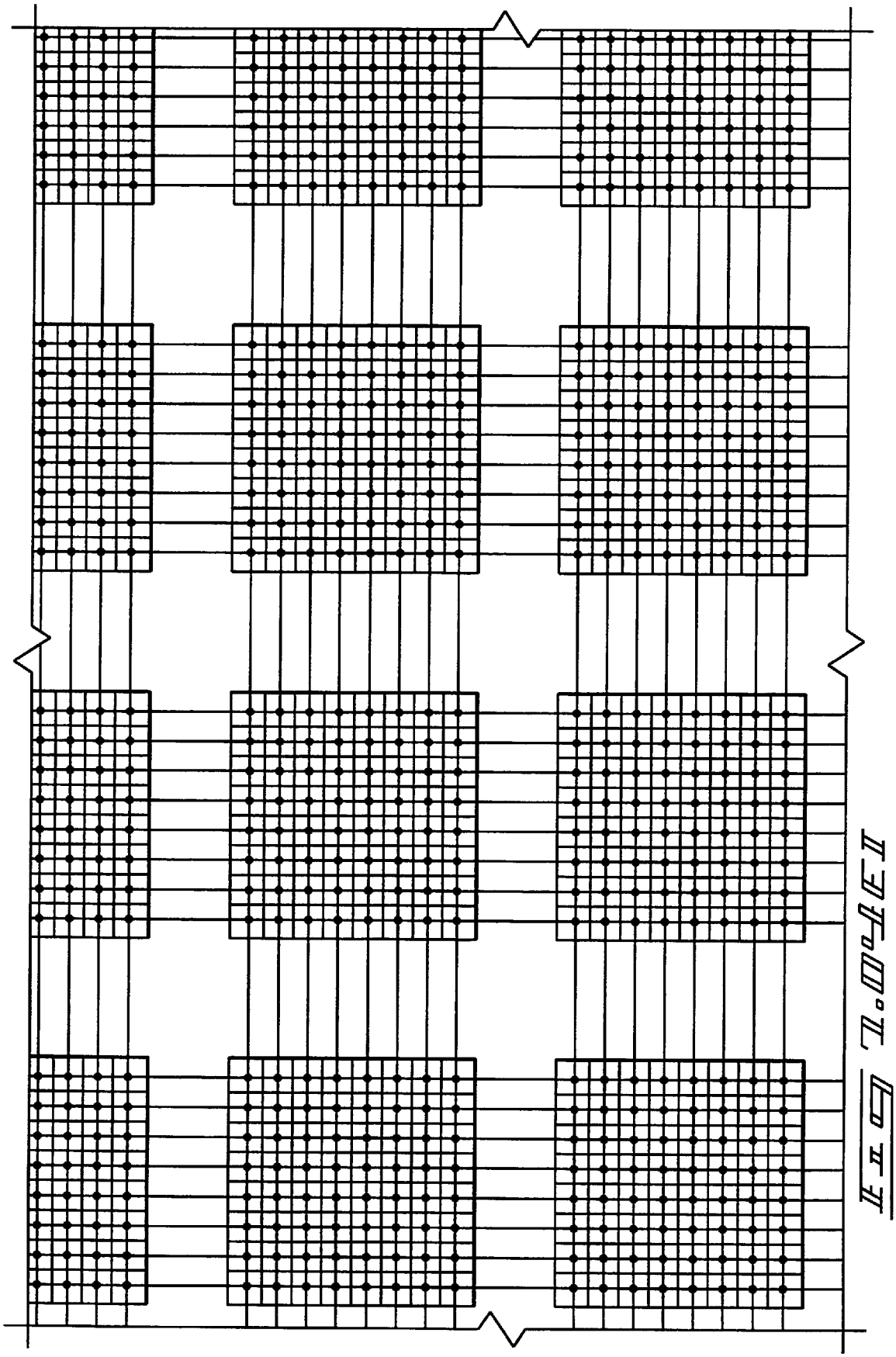


FIG. 6.00.L



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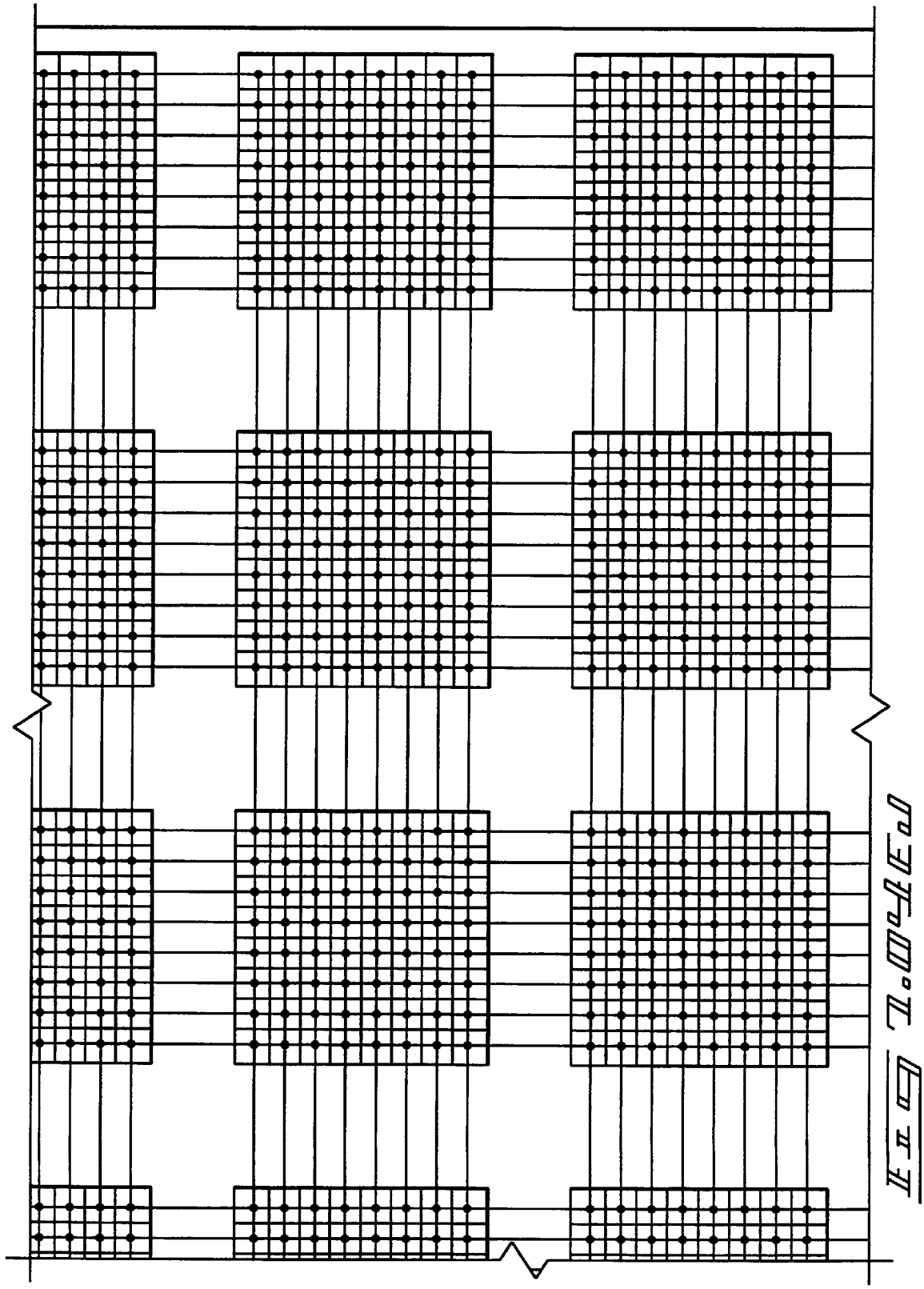


FIG. 347

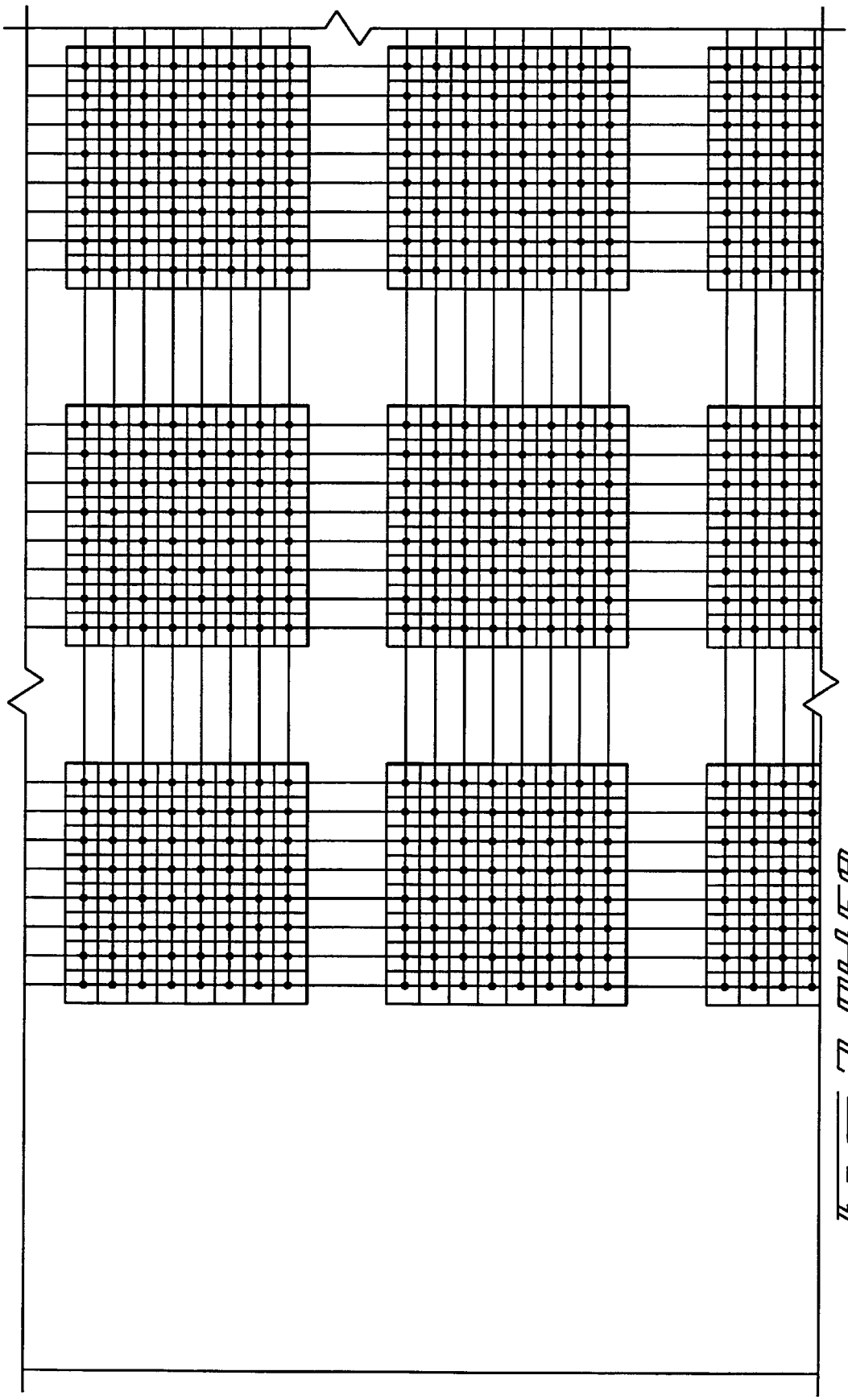


FIG. 7.0FA

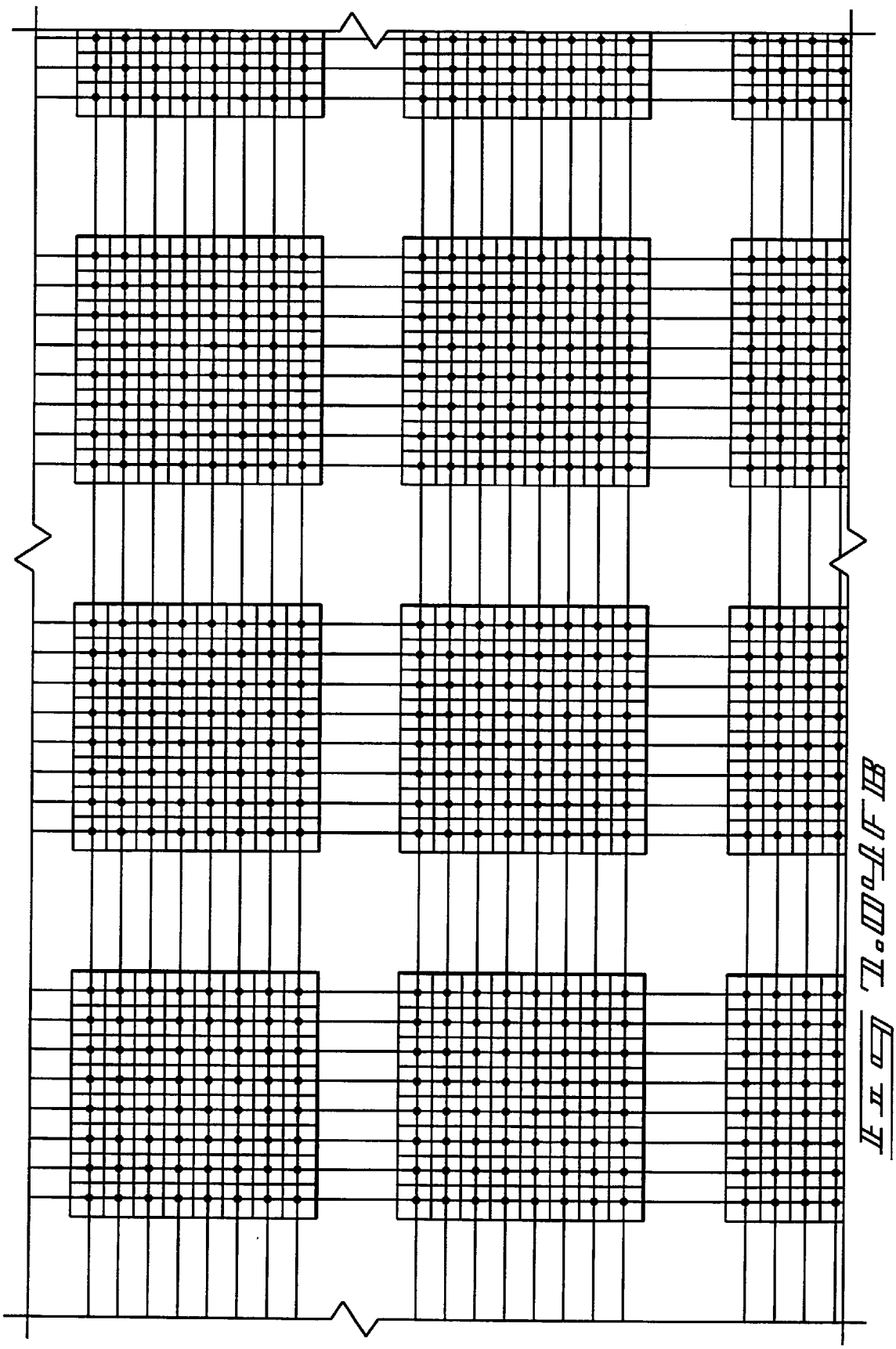


FIG. 600'L

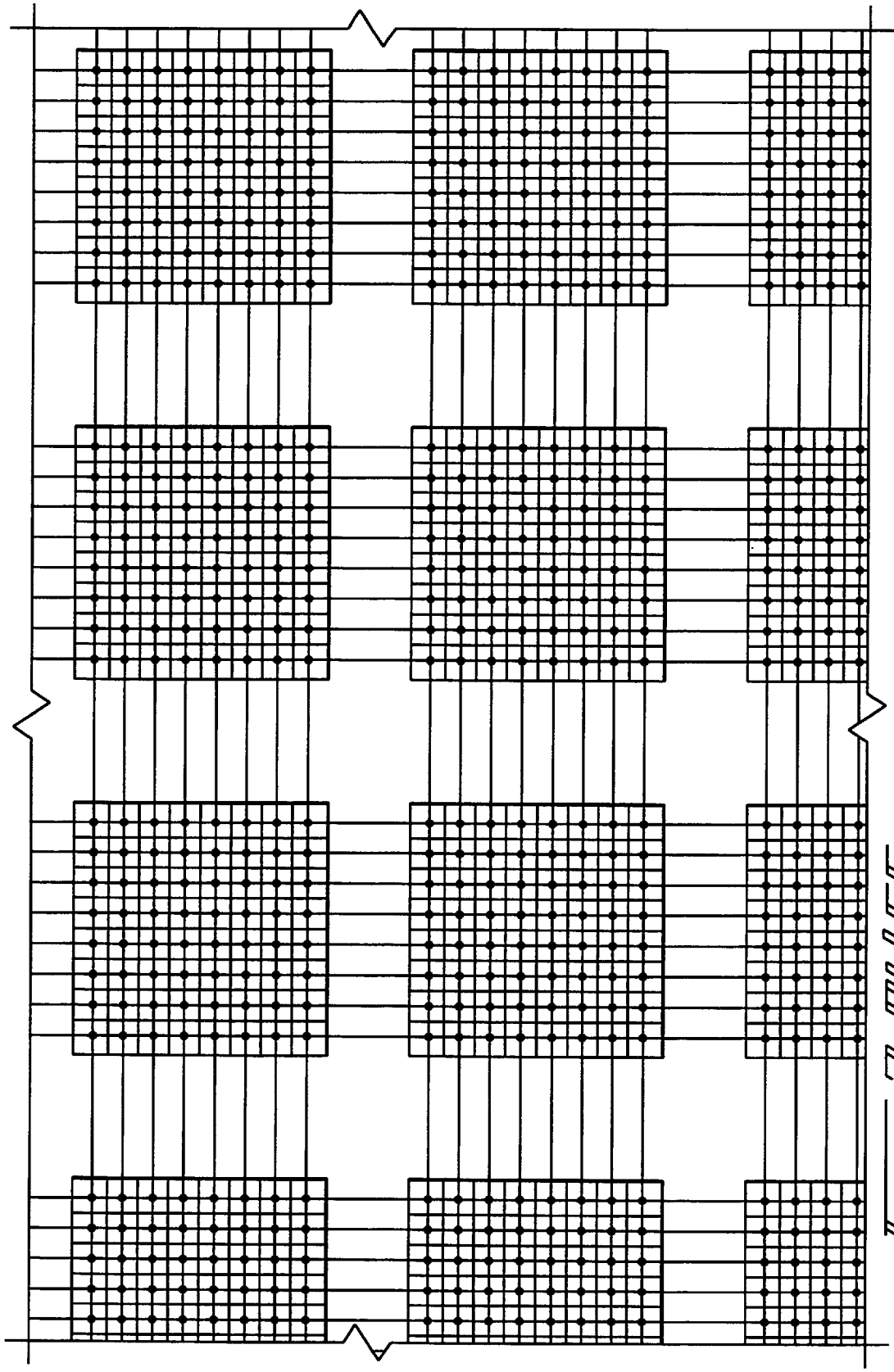


FIG 1,004F

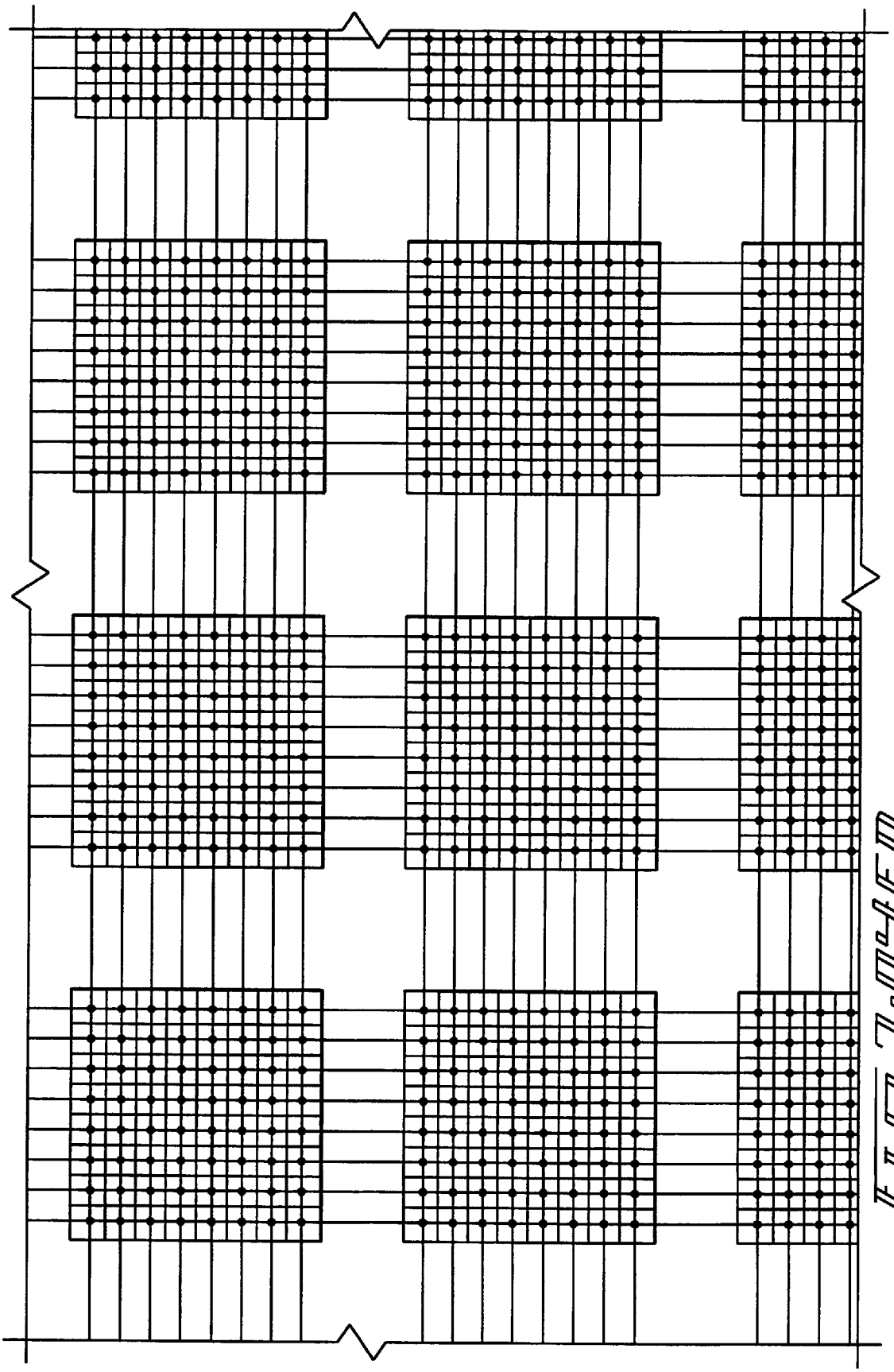


FIG. 704L

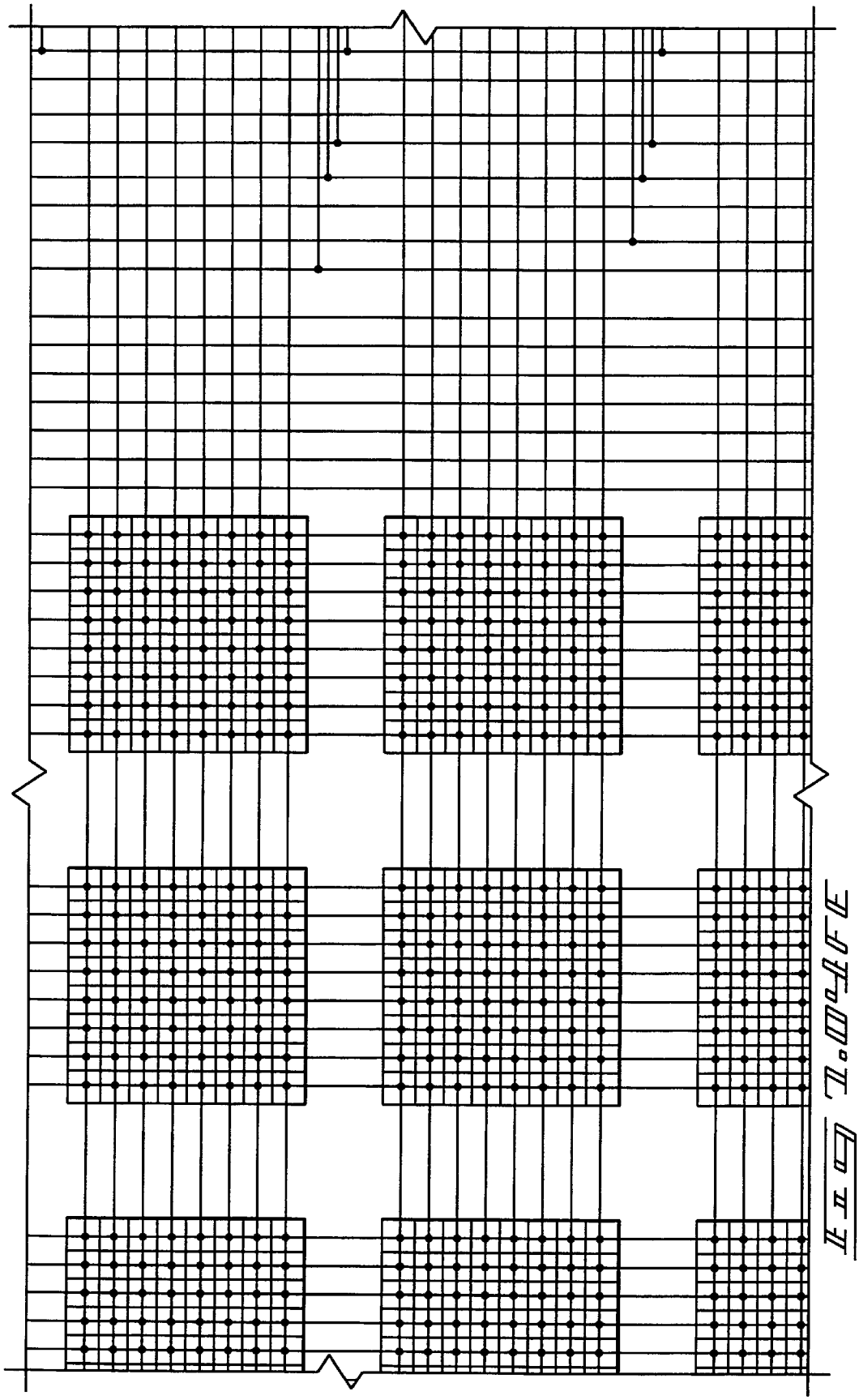


FIG. 352A

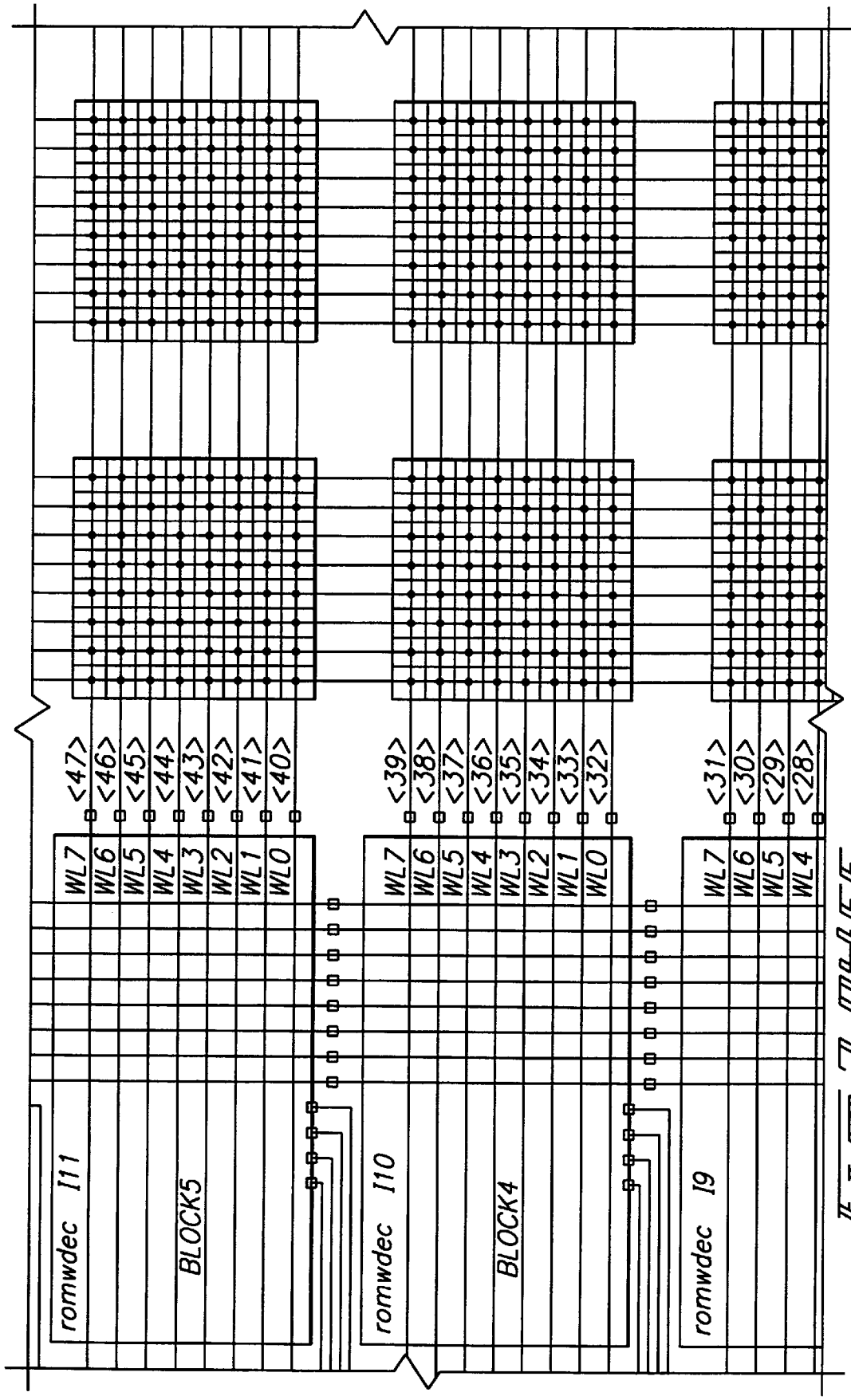

<47>
<46>
<45>
<44>
<43>
<42>
<41>
<40>
<39>
<38>
<37>
<36>
<35>
<34>
<33>
<32>
<31>
<30>
<29>
<28>
WL7
WL6
WL5
WL4
WL3
WL2
WL1
WL0
romwdec I11
BLOCK5
romwdec I10
BLOCK4
romwdec I9

FIG 11.00 OF F

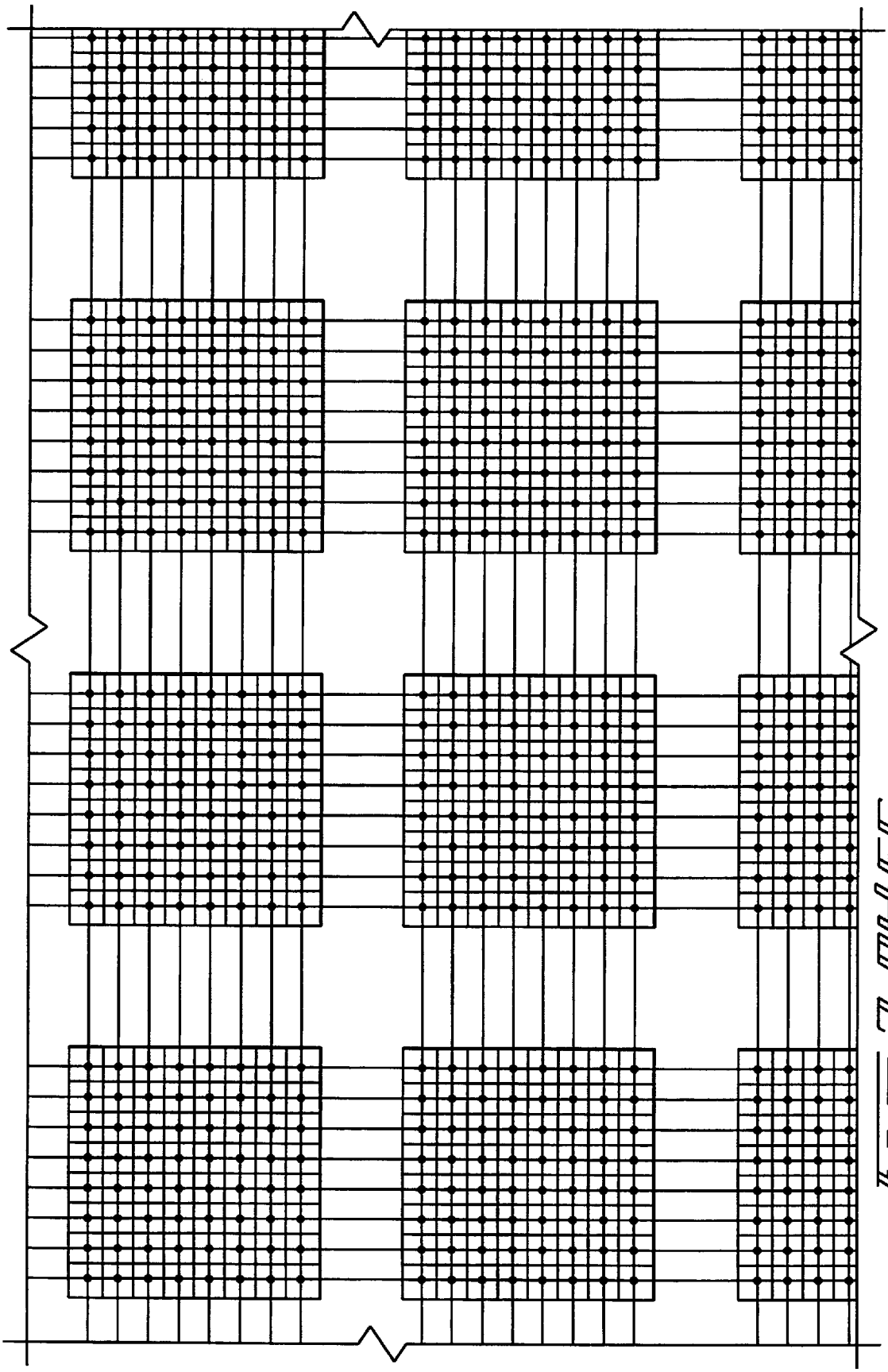


FIG 10.0L 5a-5f

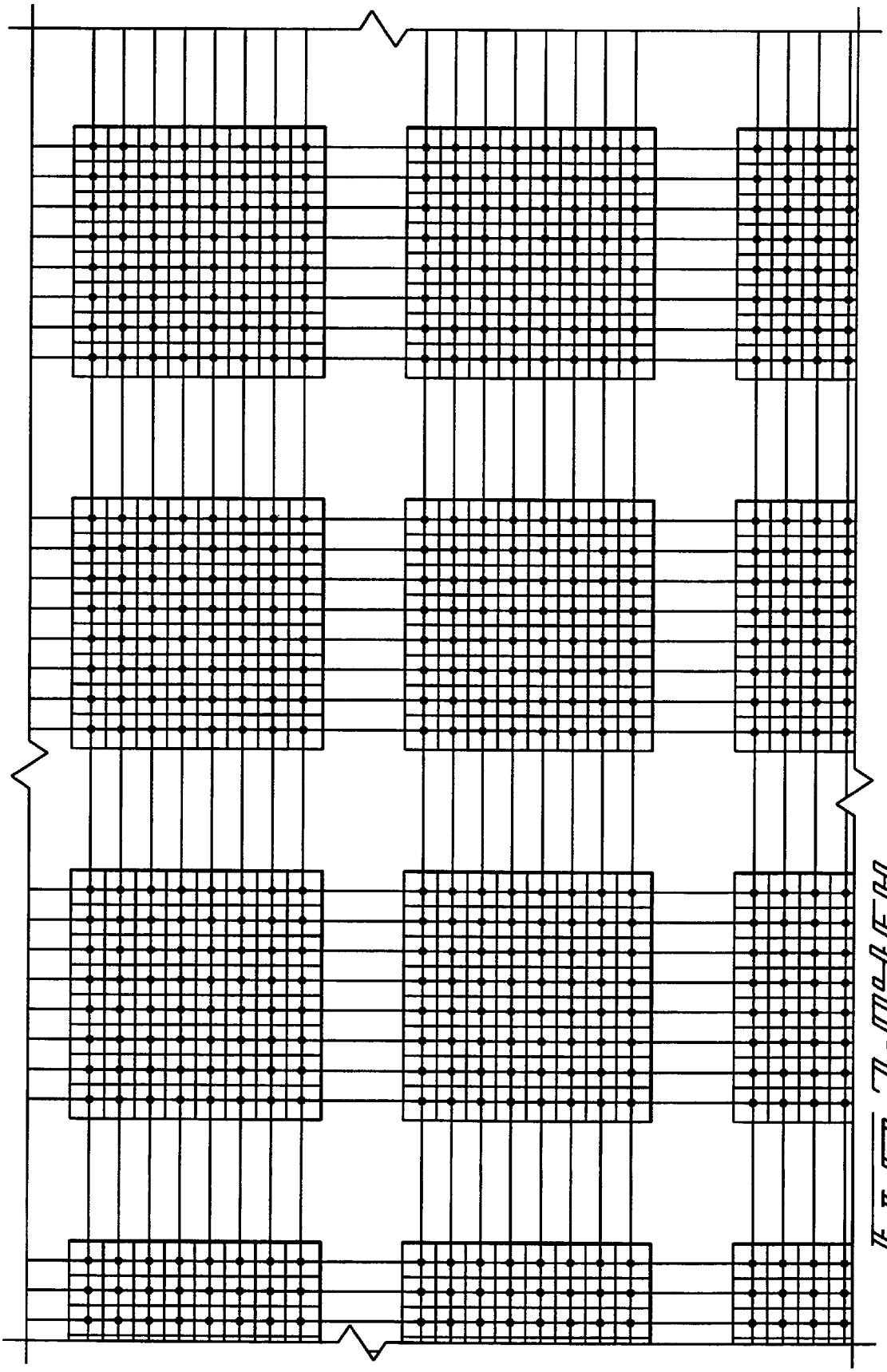


FIG. 355A

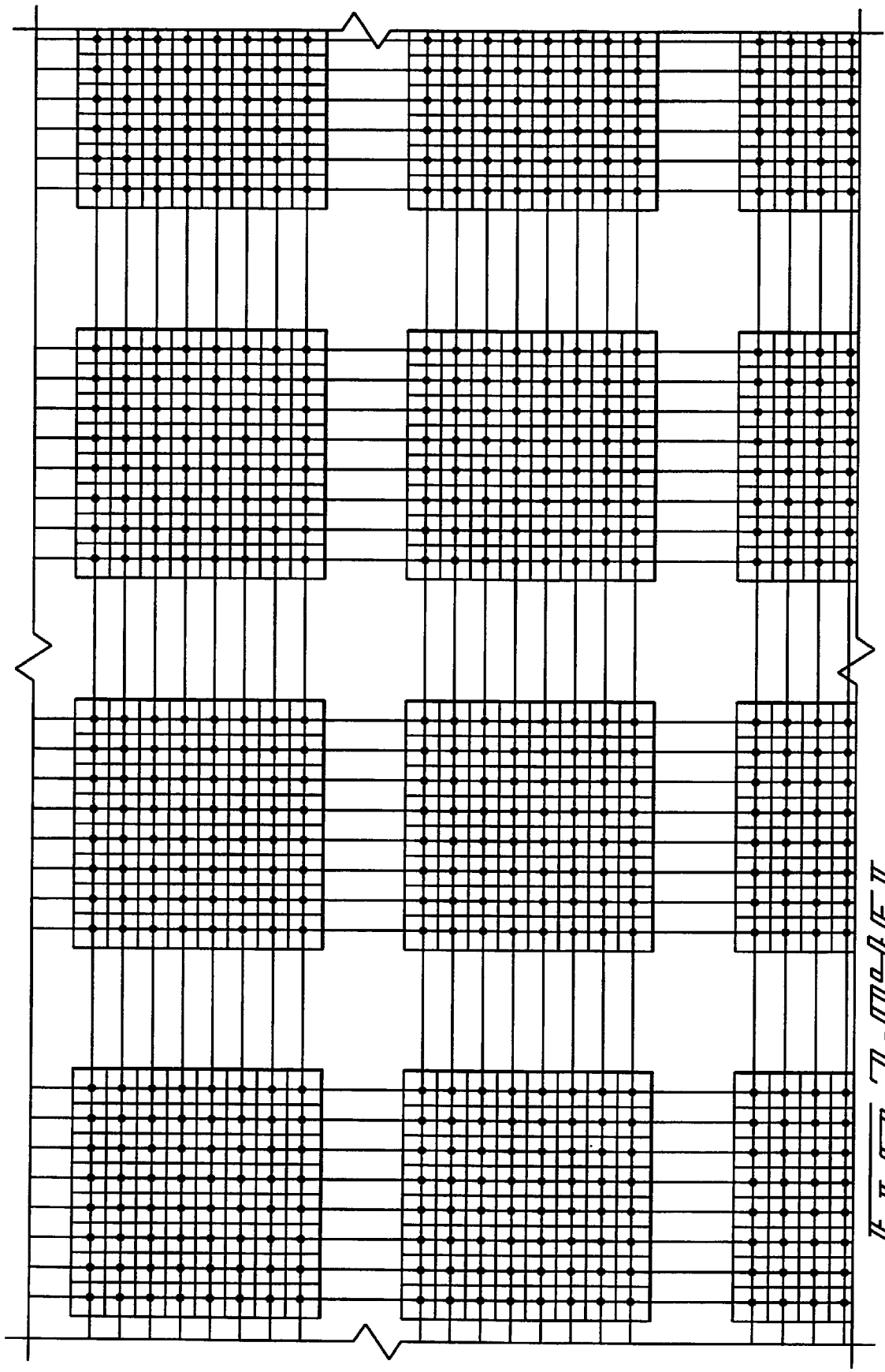


FIG. 600L

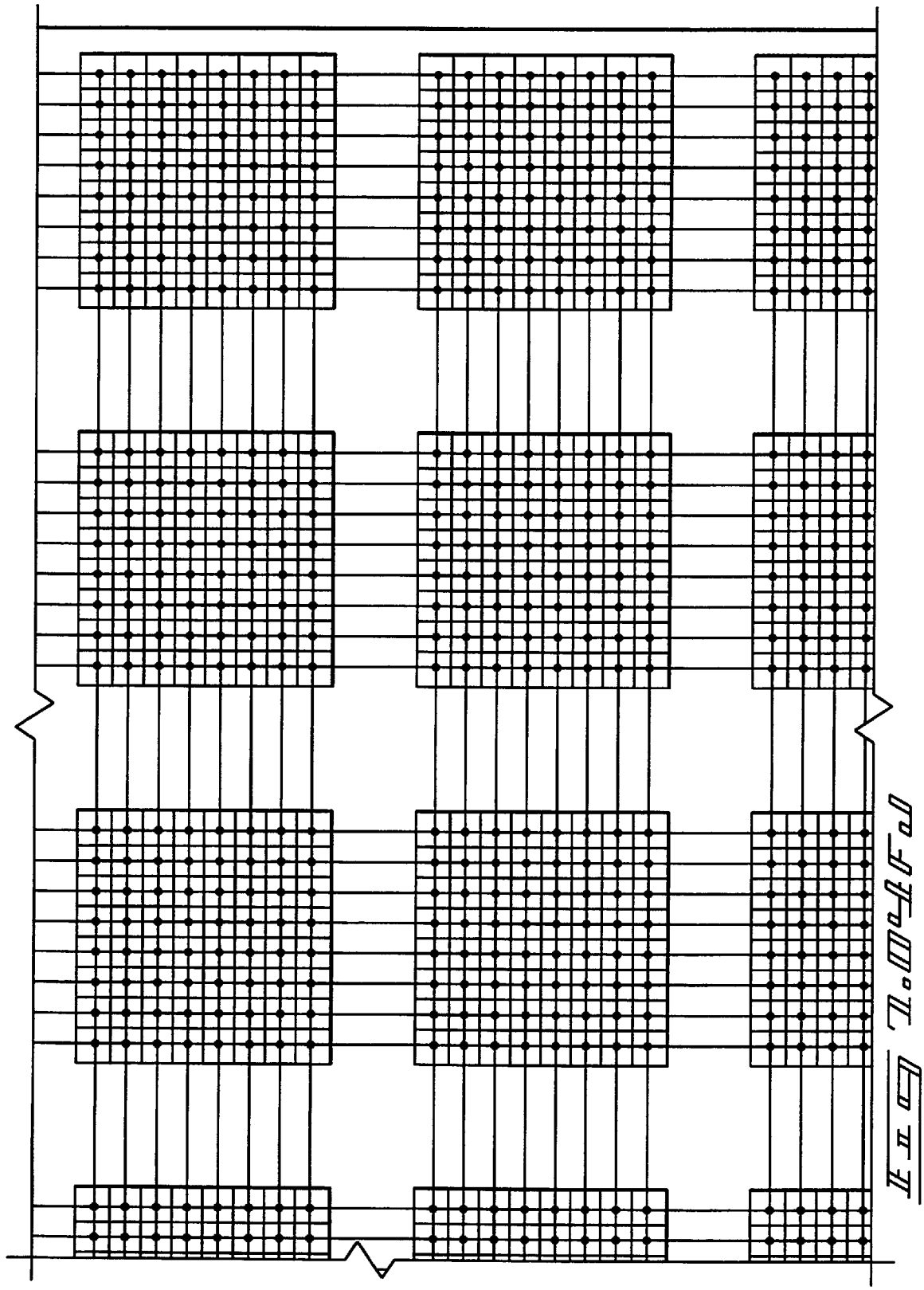


FIG. 357

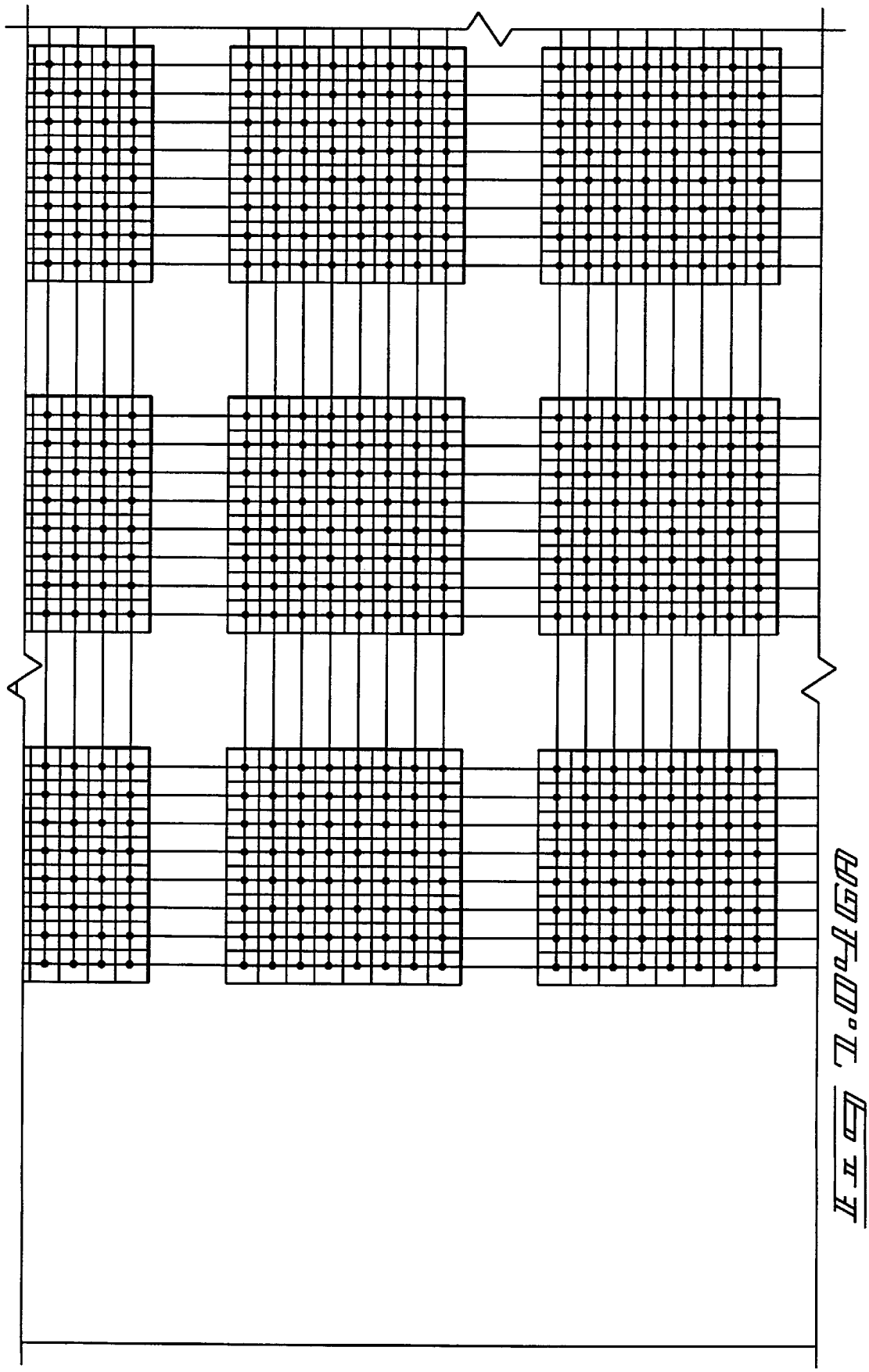


FIG. 358

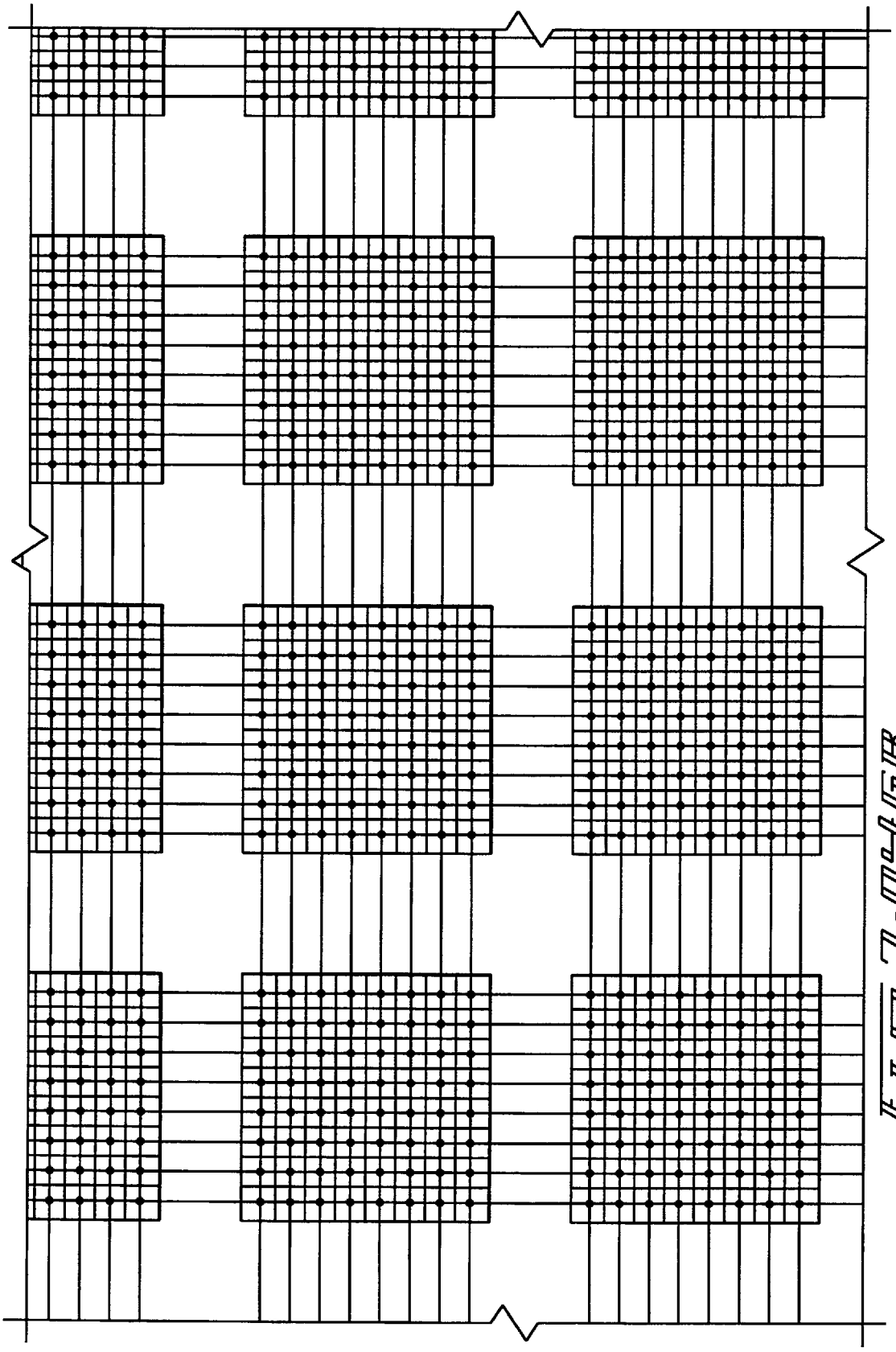
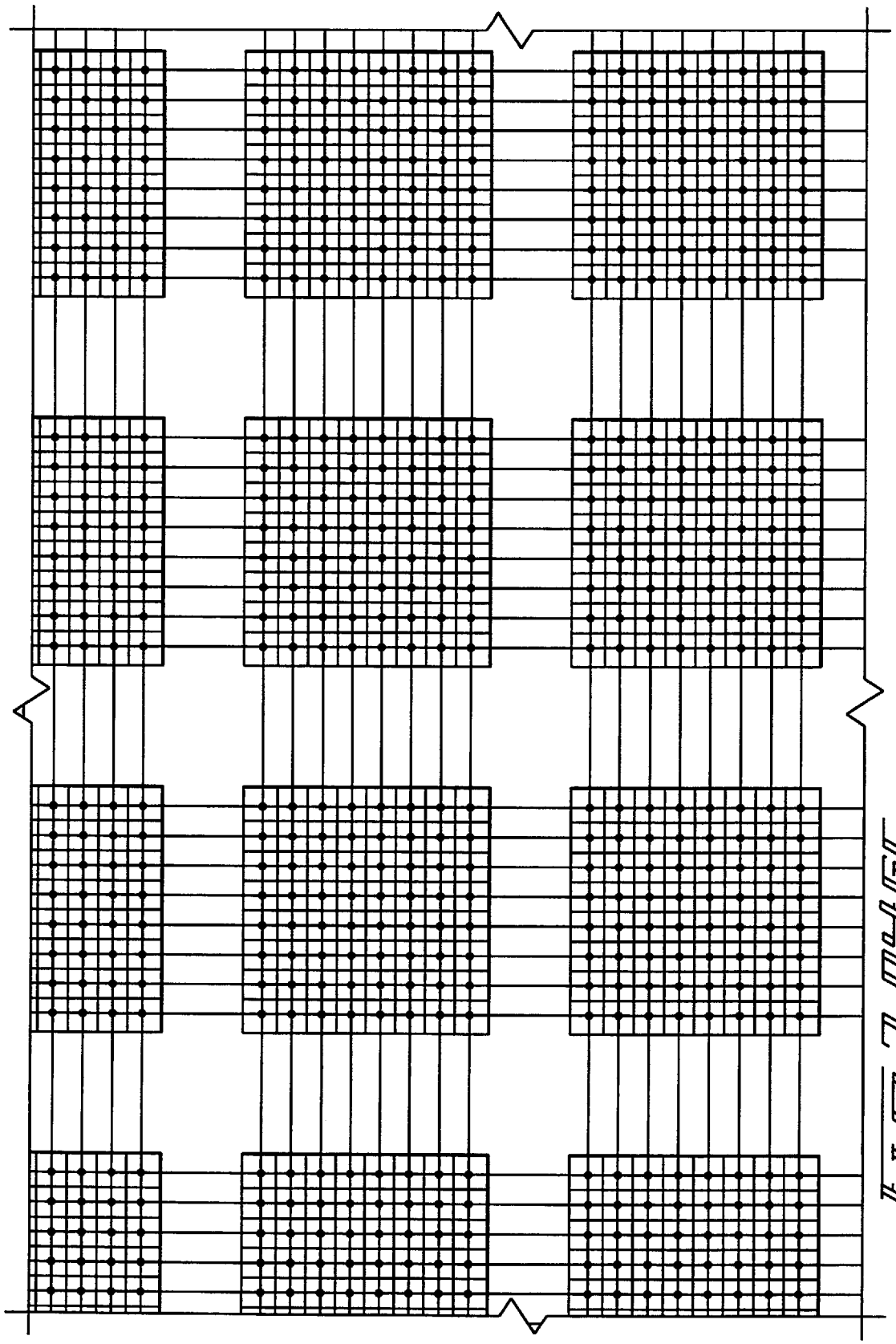


FIG. 1,004B



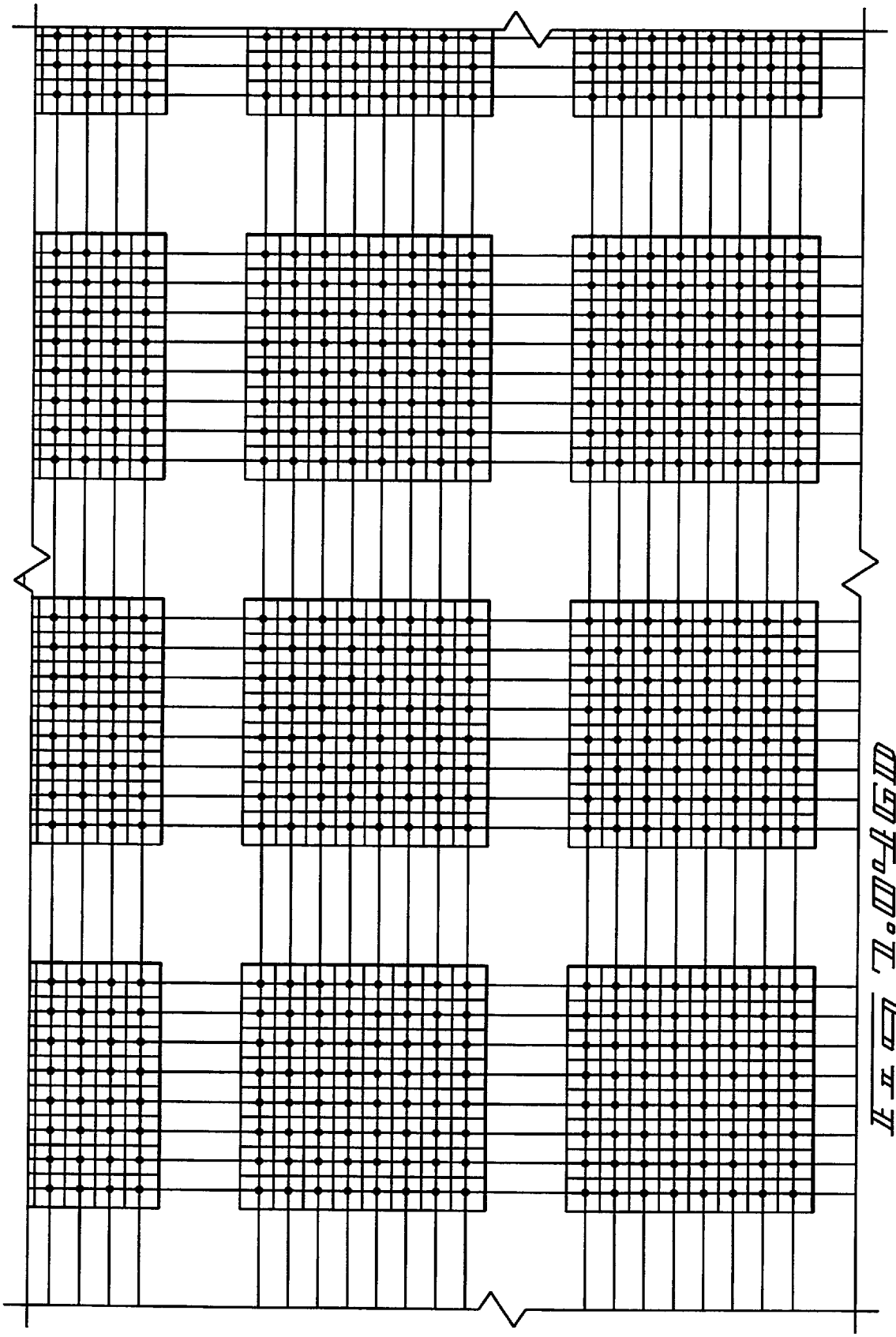
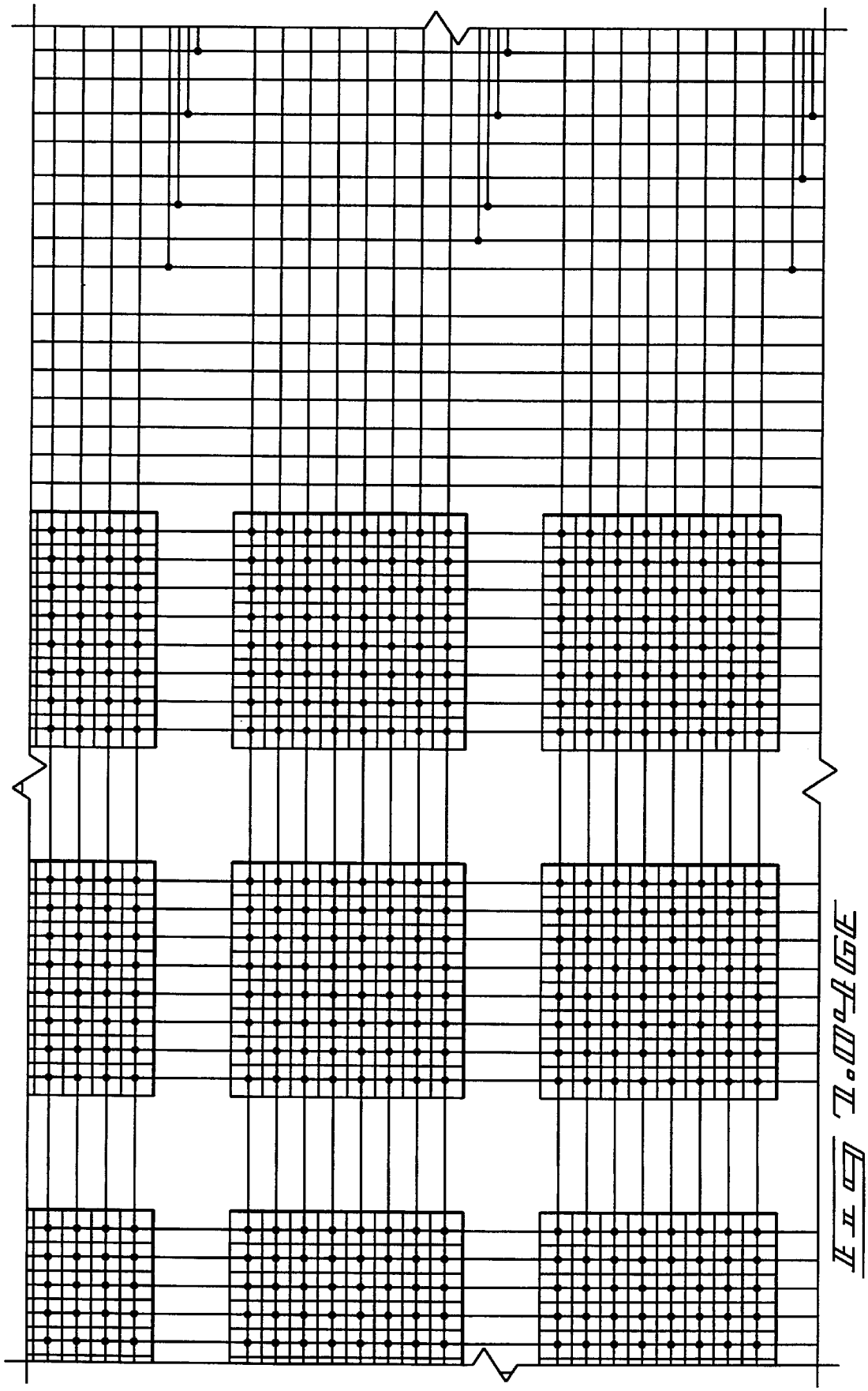


FIG. 7.0476



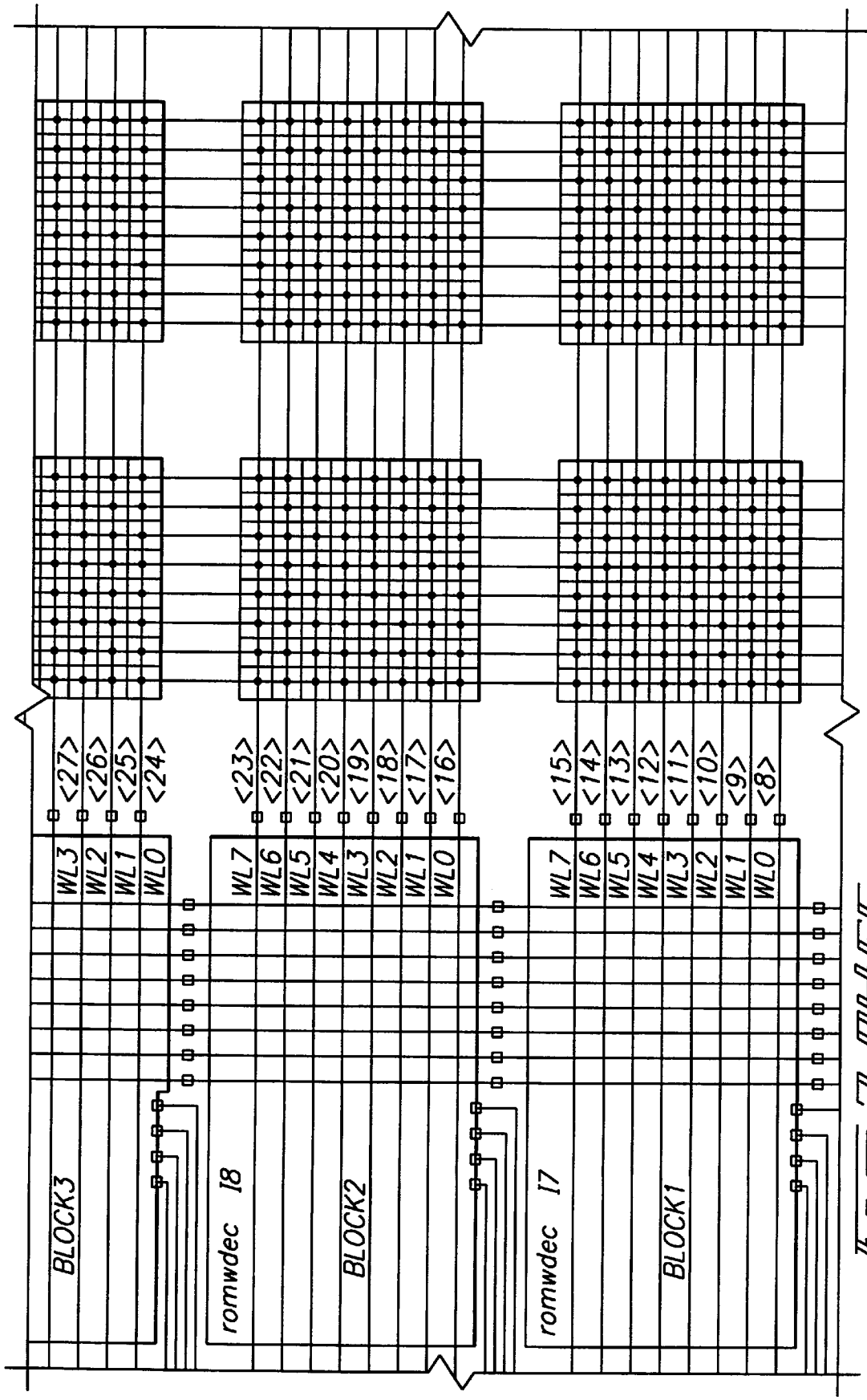

BLOCK3
BLOCK2
BLOCK1
romwdec I8
romwdec I7
WL3 WL2 WL1 WL0
WL7 WL6 WL5 WL4 WL3 WL2 WL1 WL0
WL7 WL6 WL5 WL4 WL3 WL2 WL1 WL0
<27> <26> <25> <24>
<23> <22> <21> <20> <19> <18> <17> <16>
<15> <14> <13> <12> <11> <10> <9> <8>

Fig. 11

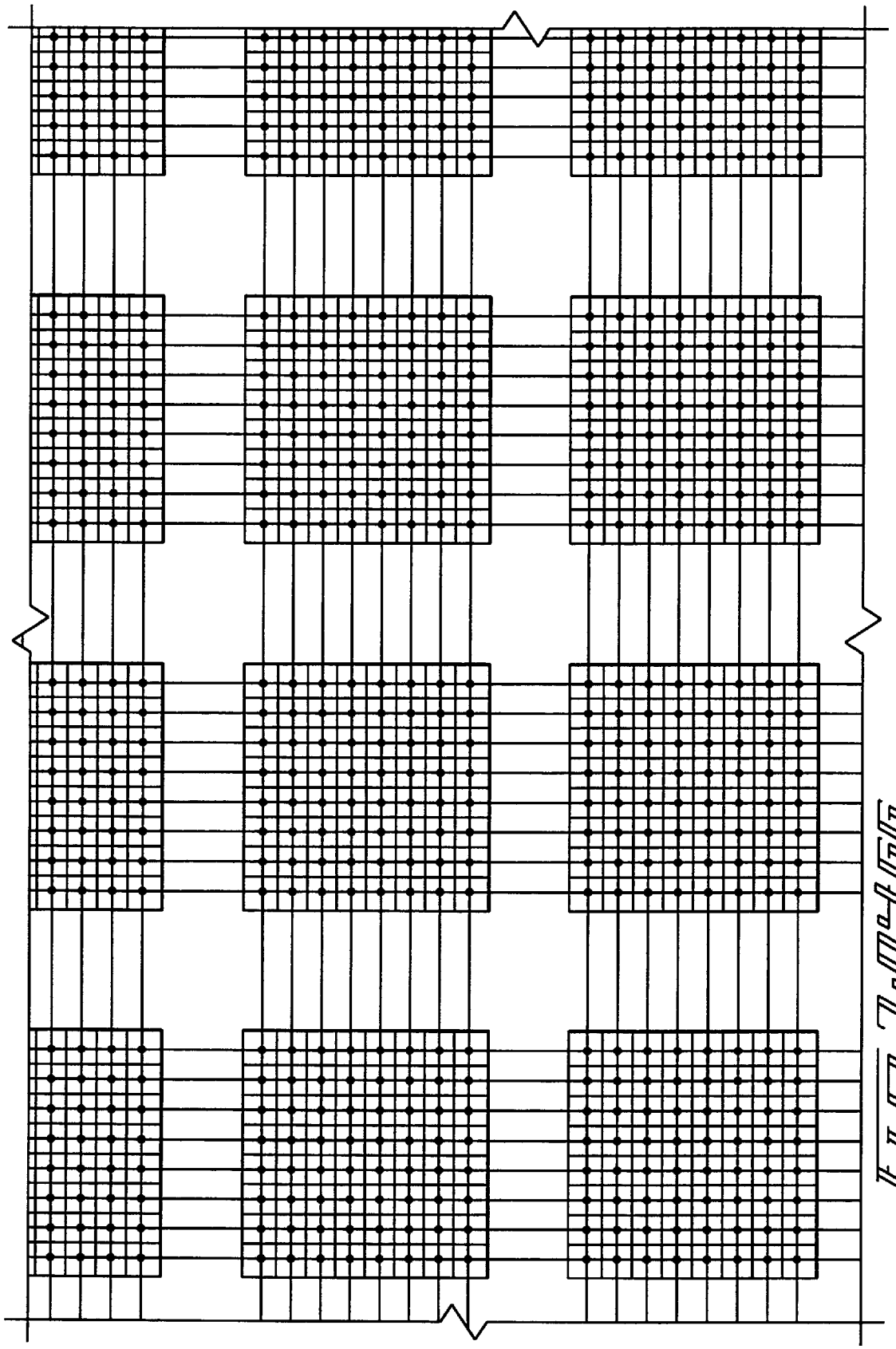


FIG. 59F00.L

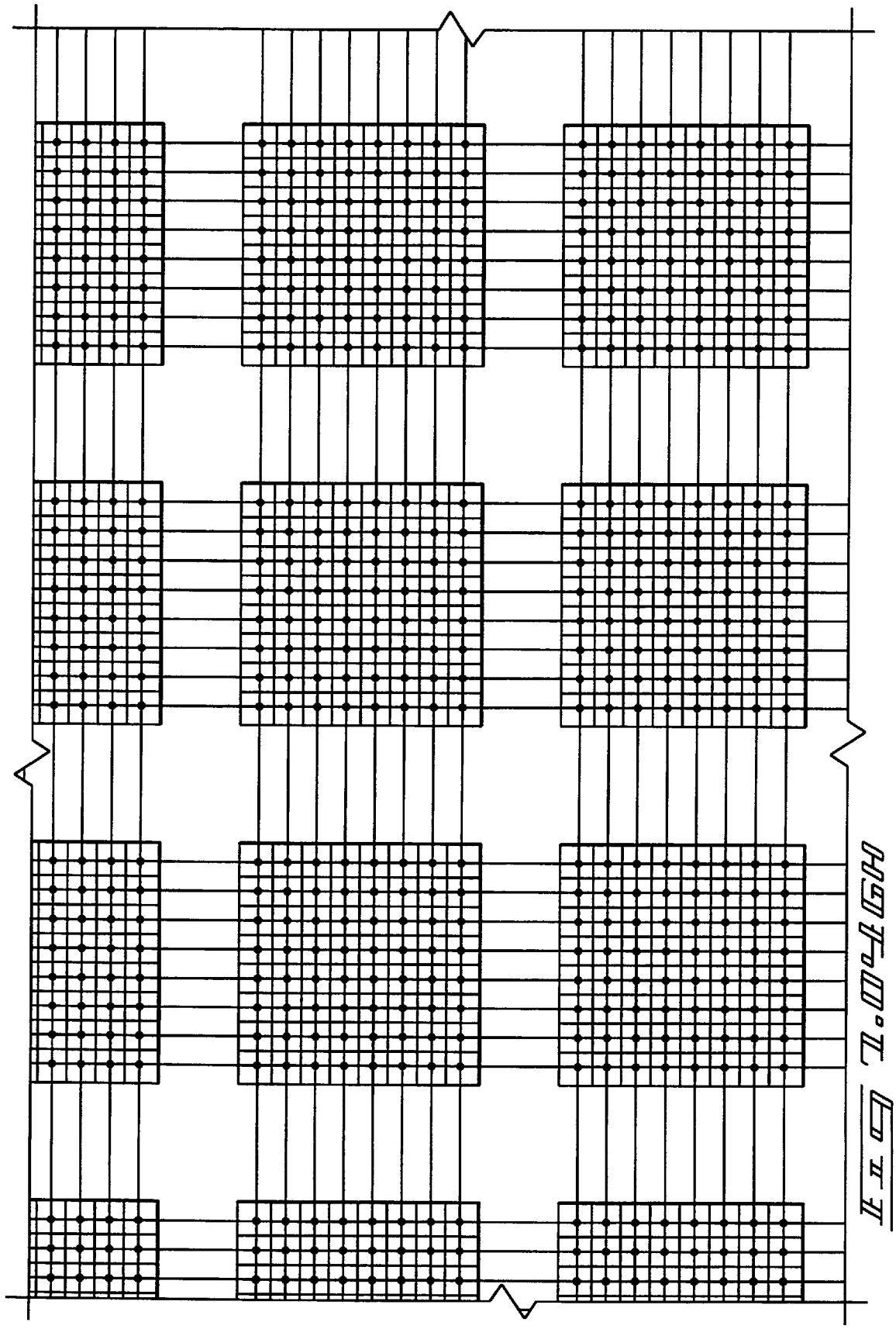


FIG 600.1

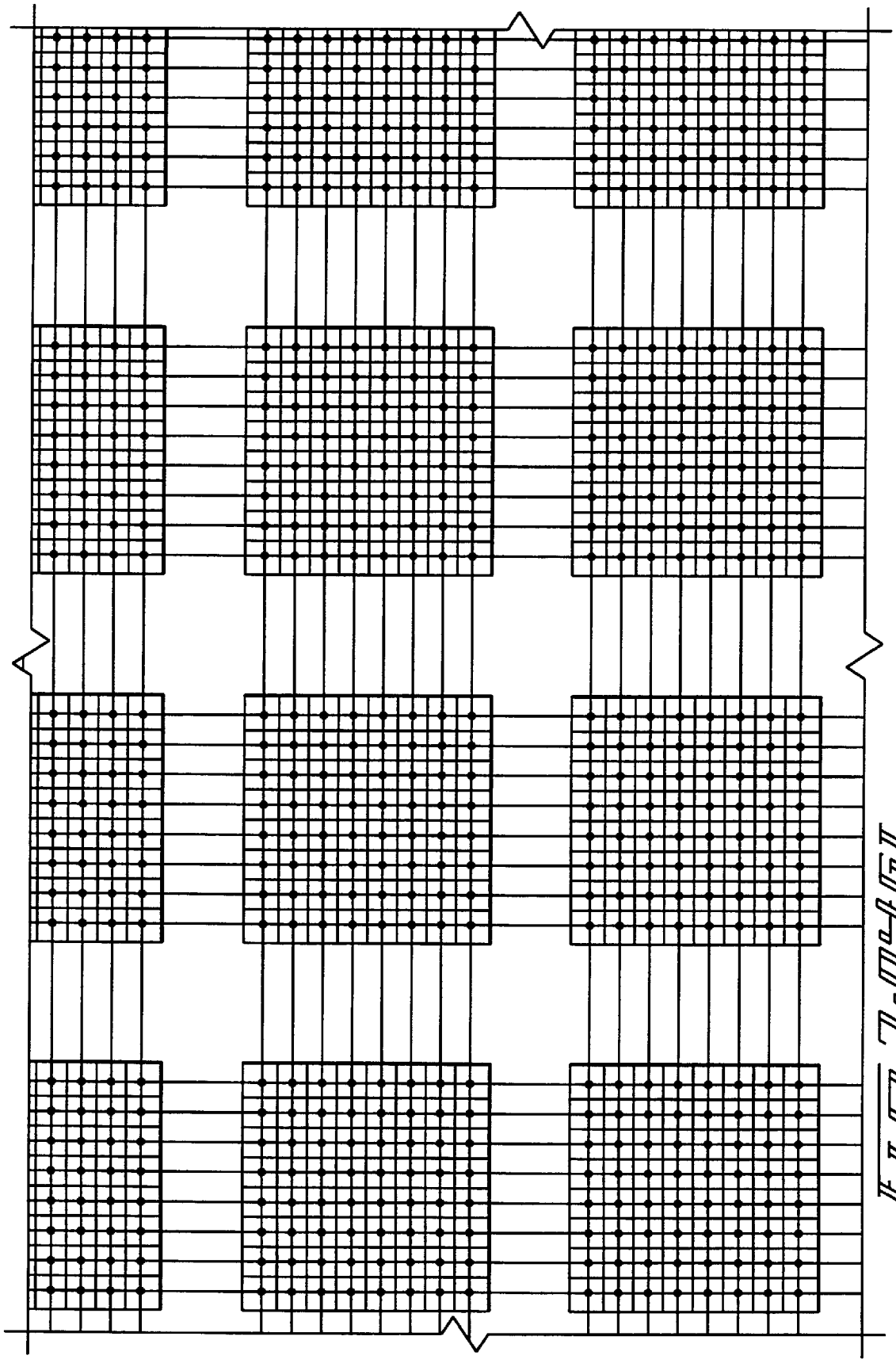


FIG. 1,004

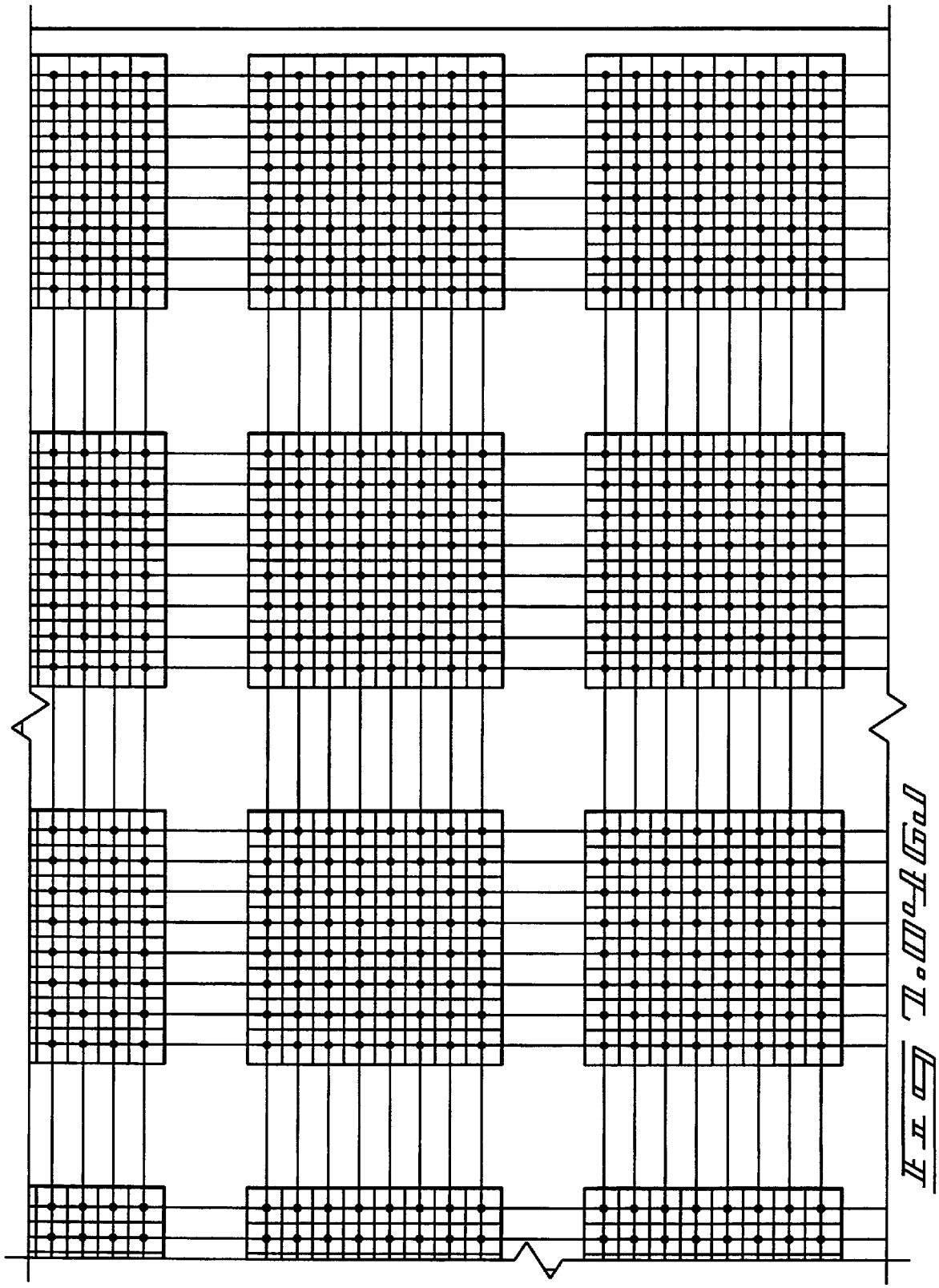


FIG. 7,004

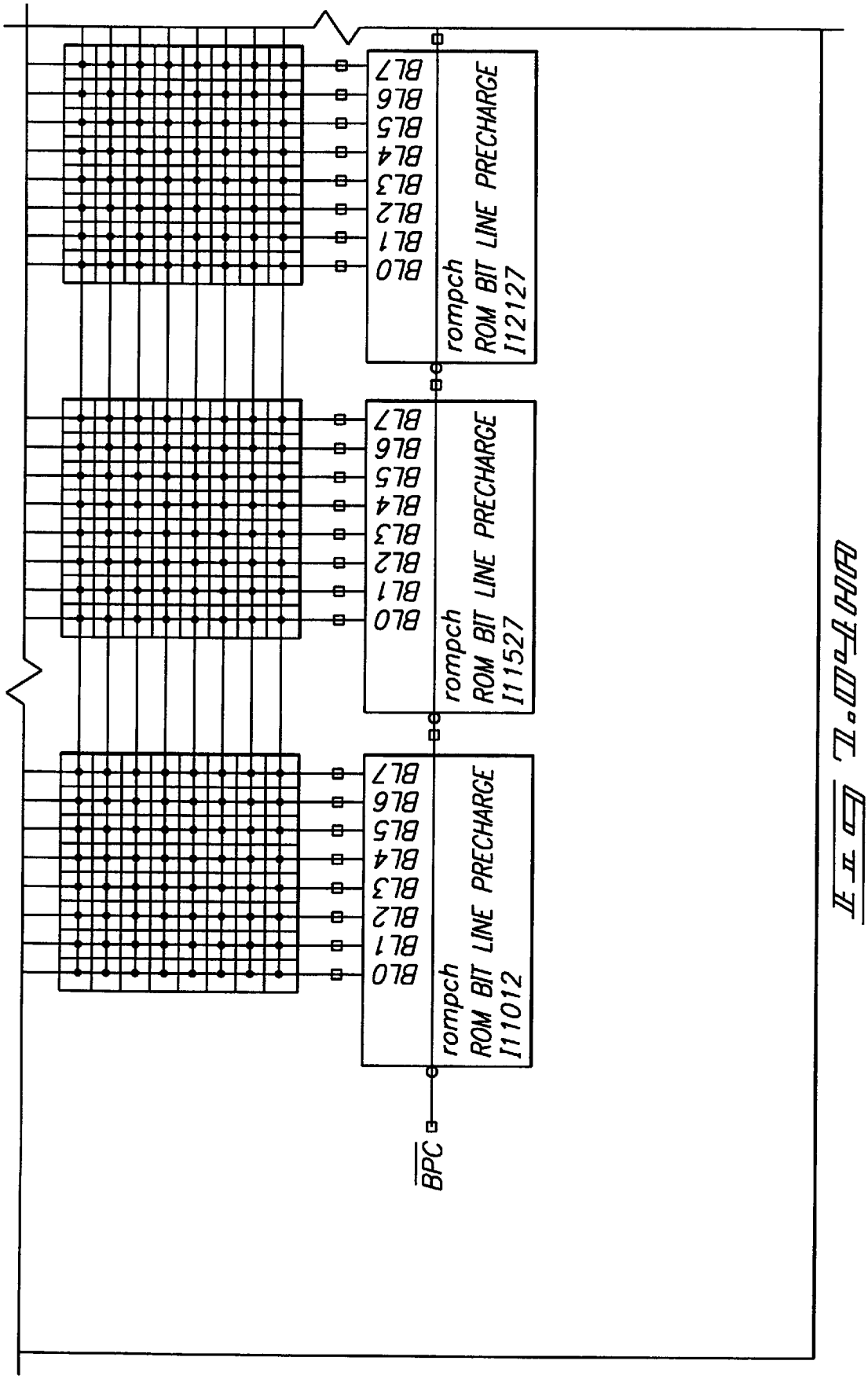

BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
I12127
I11527
I11012
BPC

FIG. 6.6H

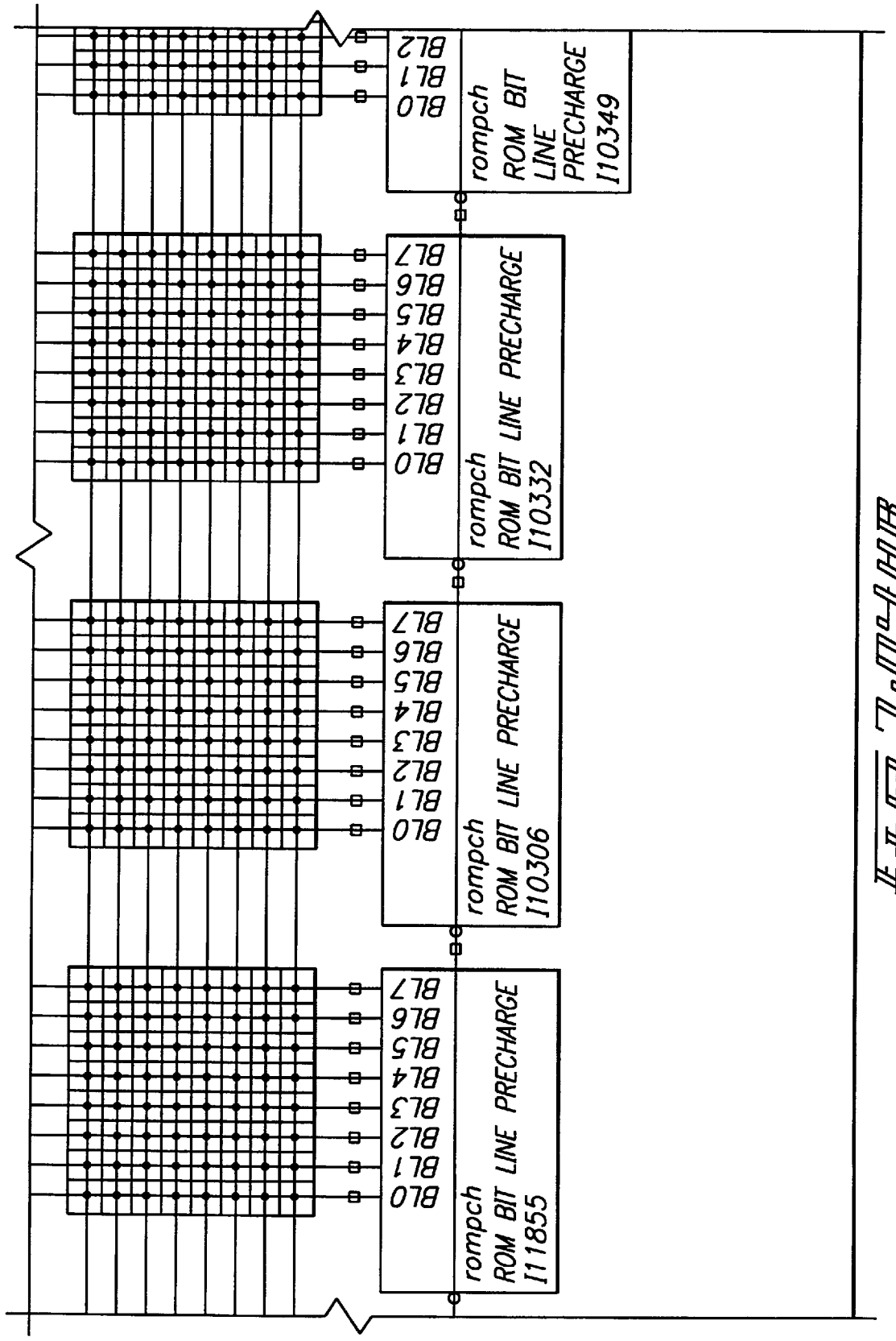

BL0
BL1
BL2
rompch
ROM BIT LINE PRECHARGE
I10349
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I10332
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I10306
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I11855

FIG. 10.11

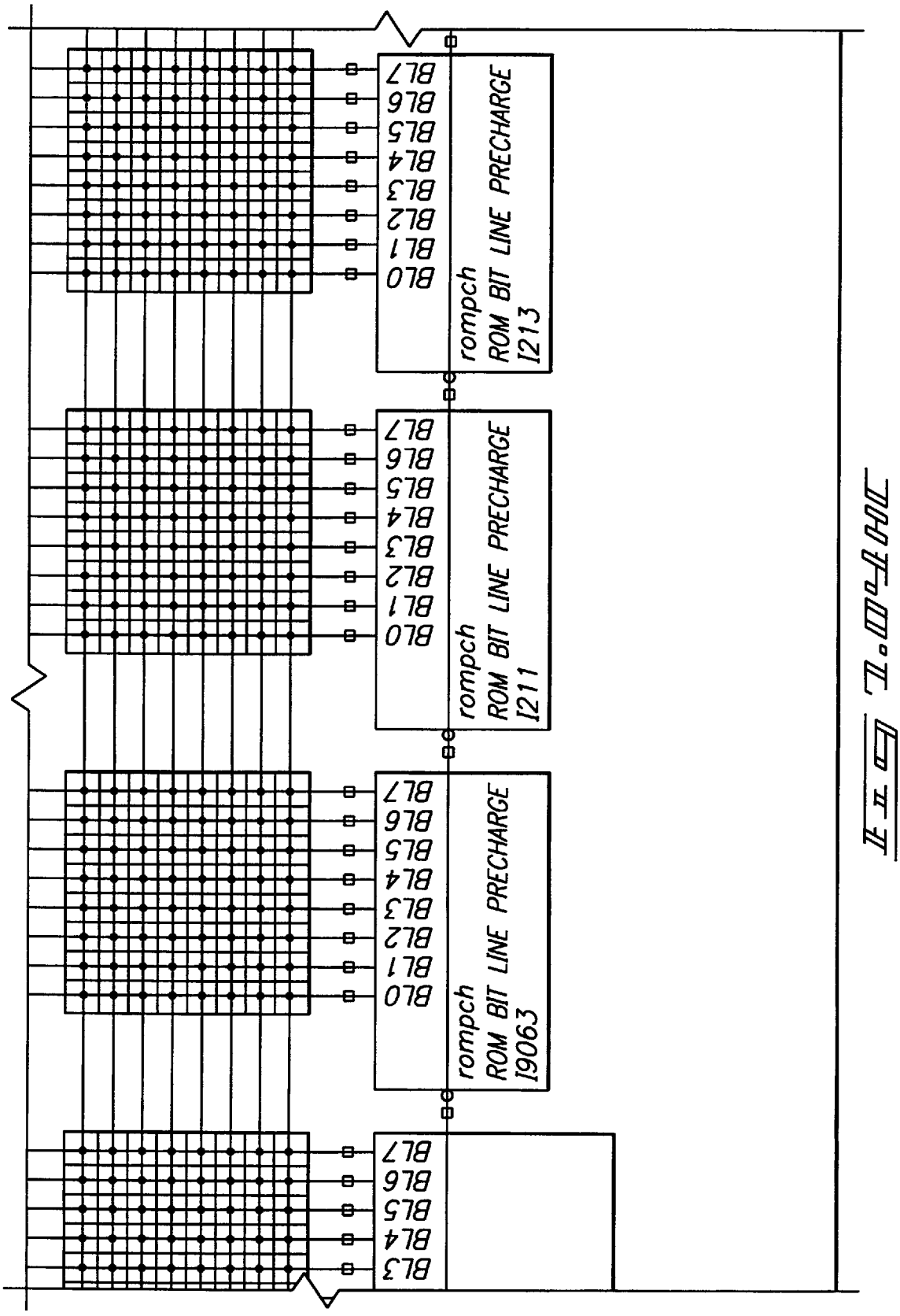

BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
I213
I211
I9063

FIG. 370

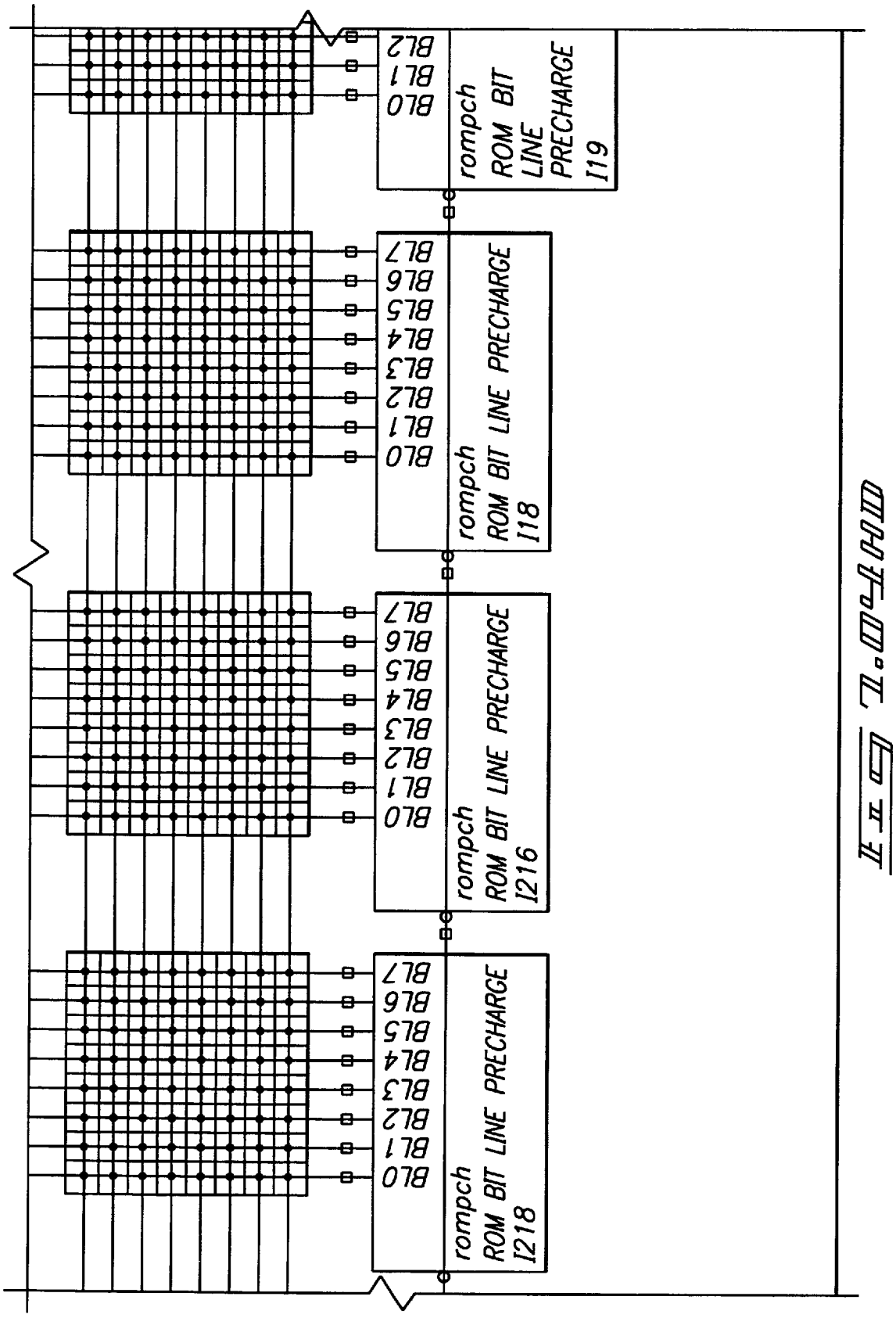
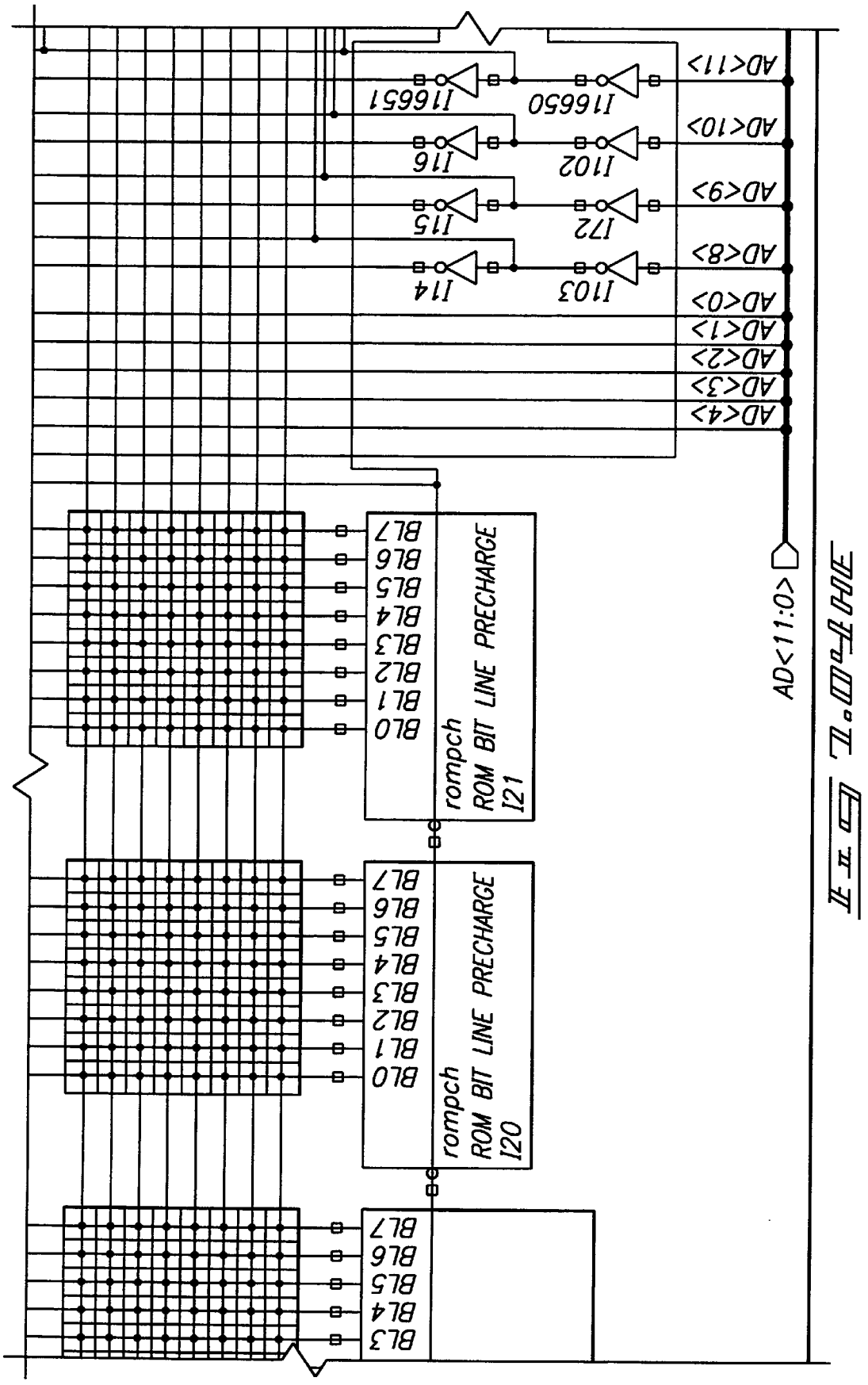

BL0
BL1
BL2
rompch
ROM BIT
LINE
PRECHARGE
I19
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I18
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I216
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I218

FIG. 6.04H


AD<11>
AD<10>
AD<9>
AD<8>
AD<0>
AD<1>
AD<2>
AD<3>
AD<4>
I16651
I16650
I16
I102
I15
I72
I14
I103
AD<11:0>
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
I21
I20

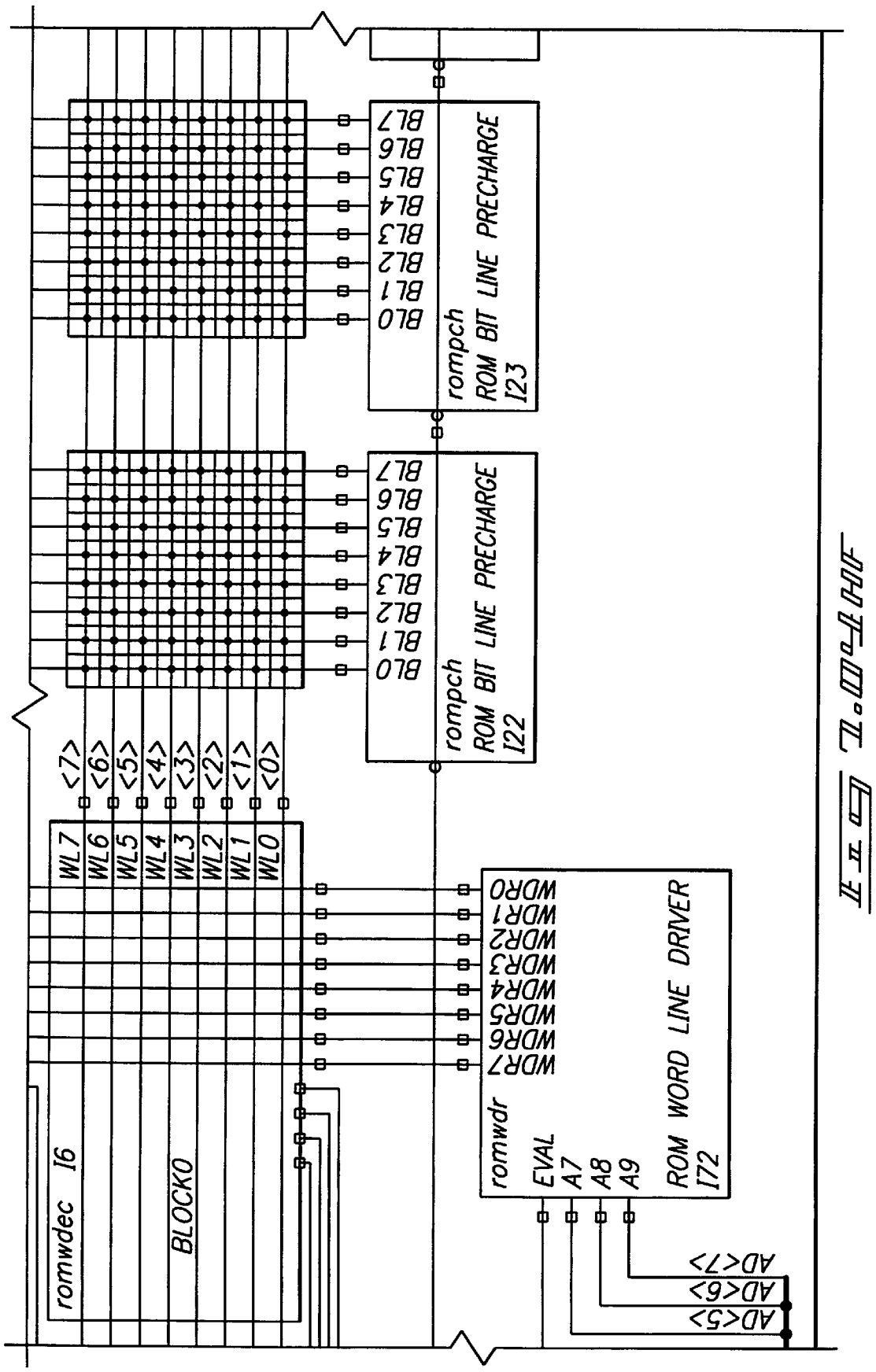

romwdec I6
BLOCK0
WL7
WL6
WL5
WL4
WL3
WL2
WL1
WL0
<7>
<6>
<5>
<4>
<3>
<2>
<1>
<0>
rompch
ROM BIT LINE PRECHARGE
I22
rompch
ROM BIT LINE PRECHARGE
I23
romwdr
ROM WORD LINE DRIVER
I72
EVAL
A7
A8
A9
AD<7>
AD<6>
AD<5>

FIG. 11HF

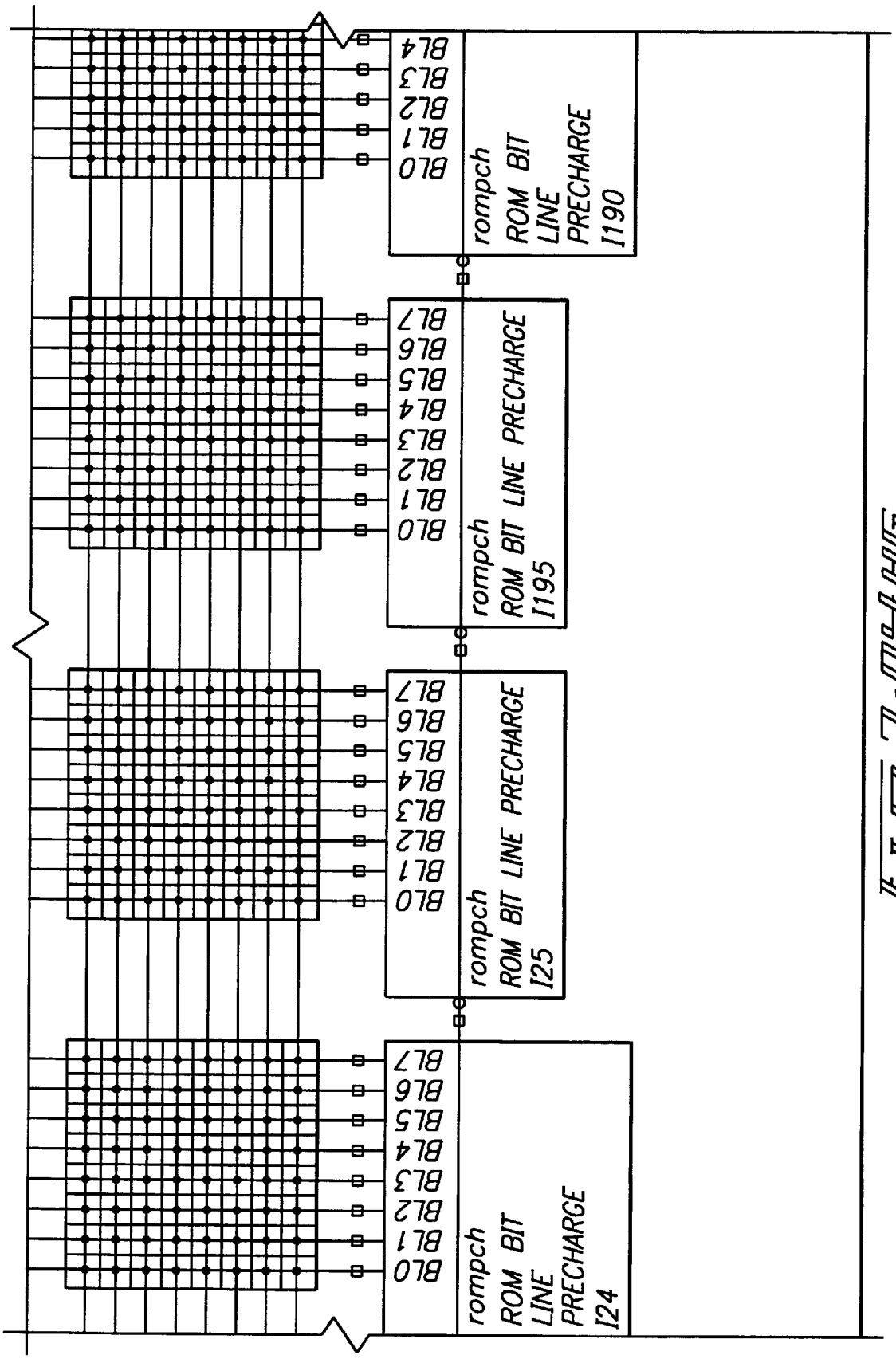

BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT
LINE
PRECHARGE
1190
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
1195
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
125
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT
LINE
PRECHARGE
124

FIG. 1100L

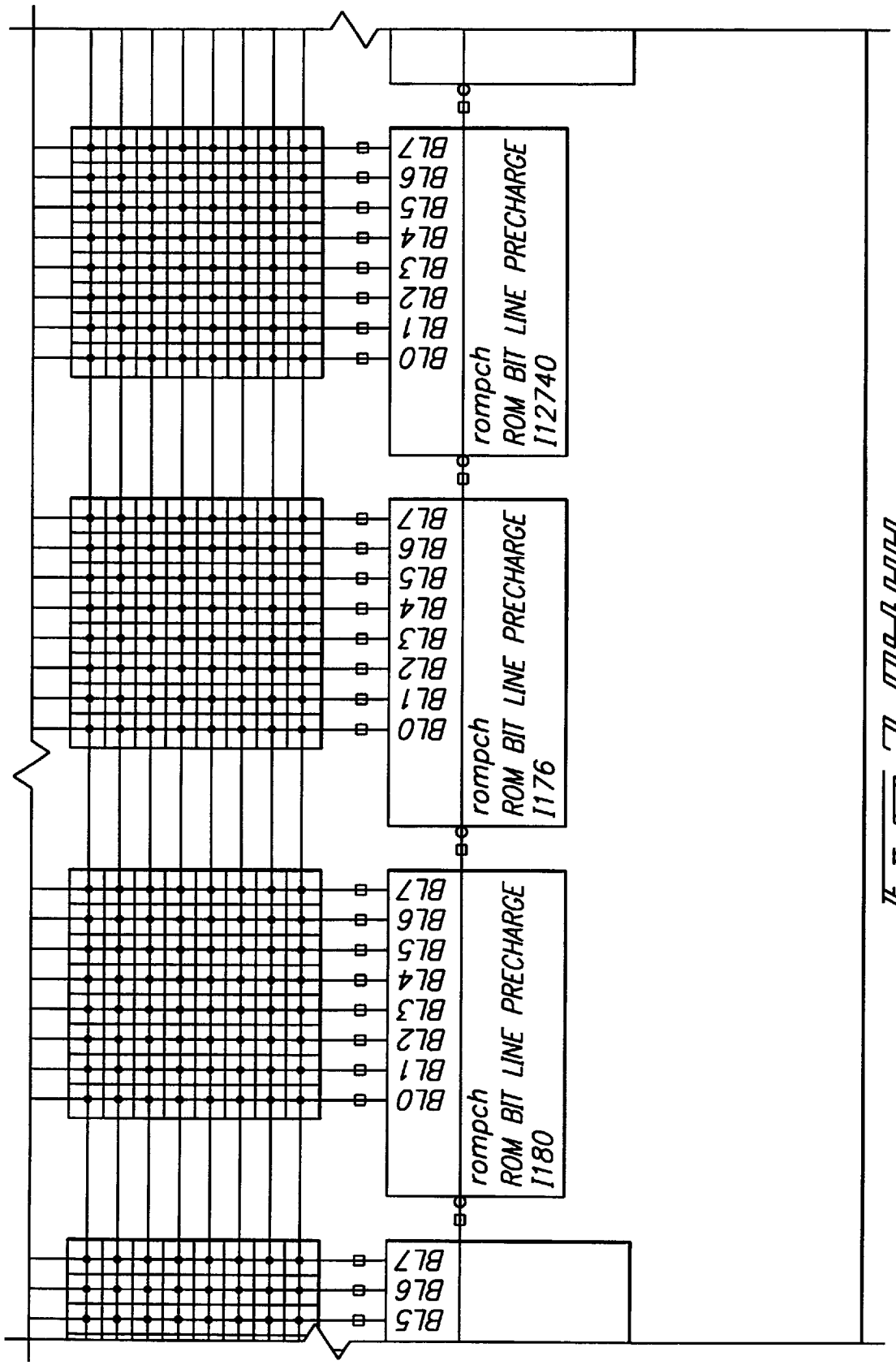

BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
I12740
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
I1176
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
I1180
BL7
BL6
BL5

FIG. 6.00.L

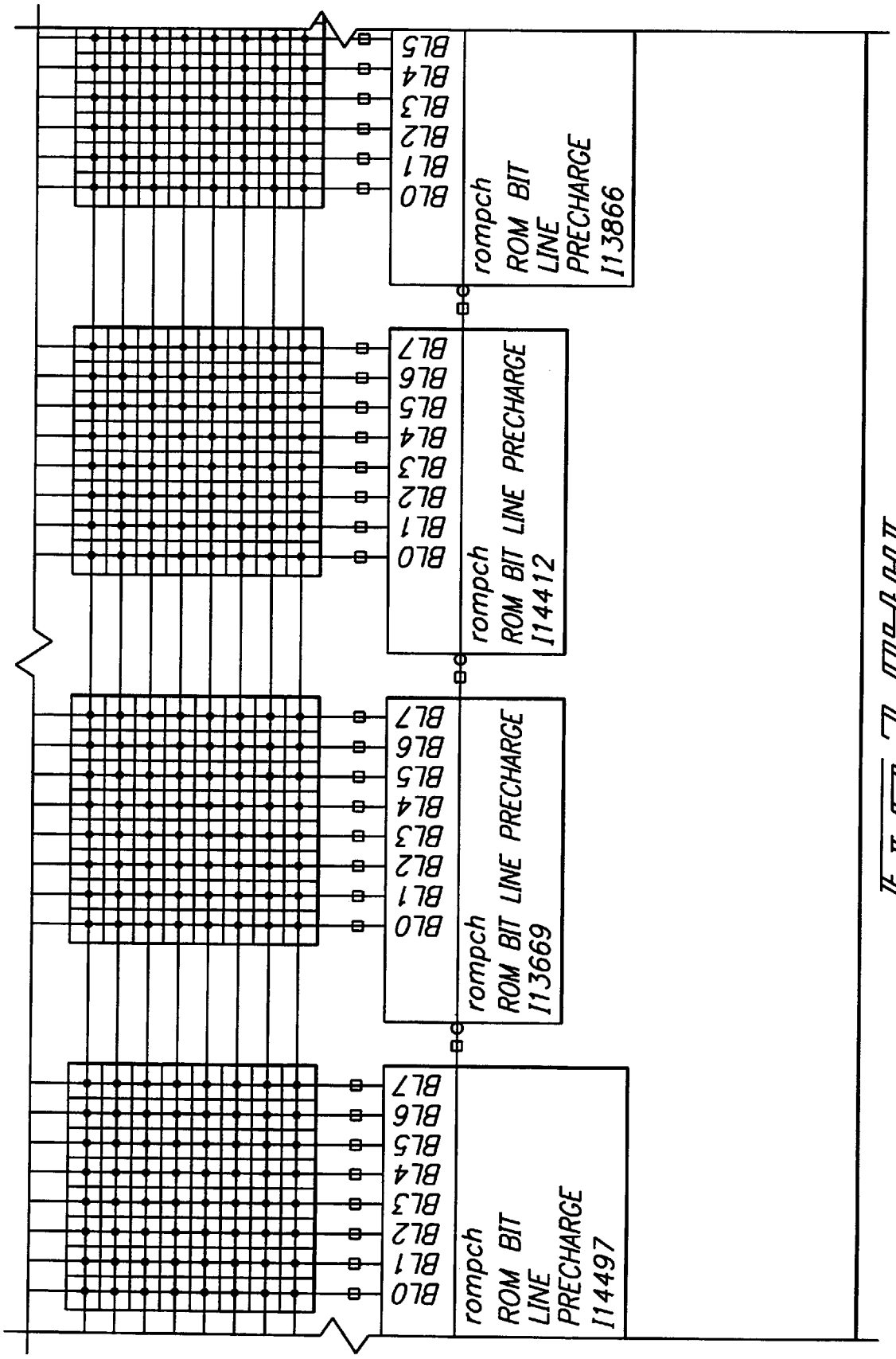

BL0
BL1
BL2
BL3
BL4
BL5
rompch
ROM BIT
LINE
PRECHARGE
I13866
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I14412
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT LINE PRECHARGE
I13669
BL0
BL1
BL2
BL3
BL4
BL5
BL6
BL7
rompch
ROM BIT
LINE
PRECHARGE
I14497

FIG. 6.0711

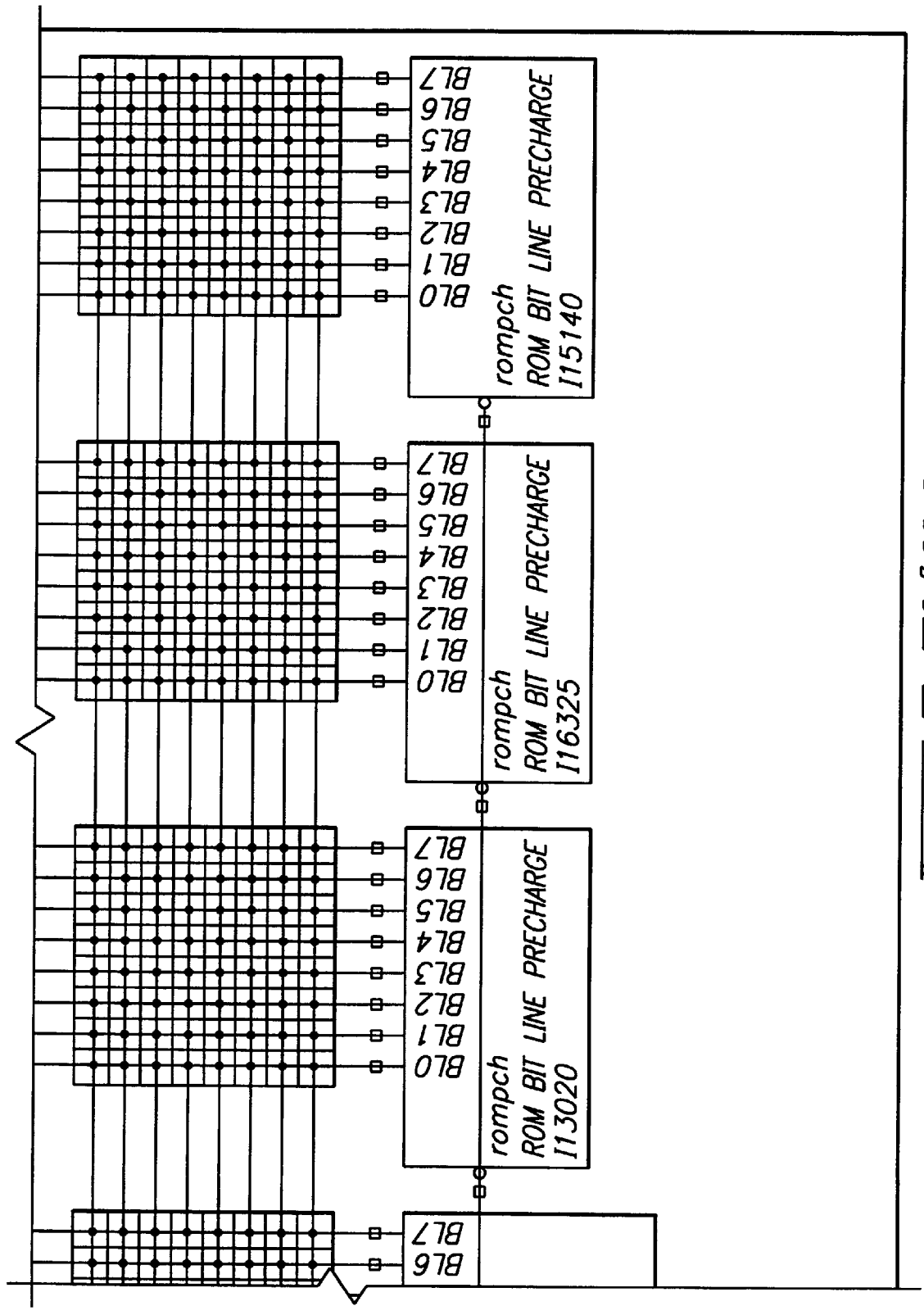
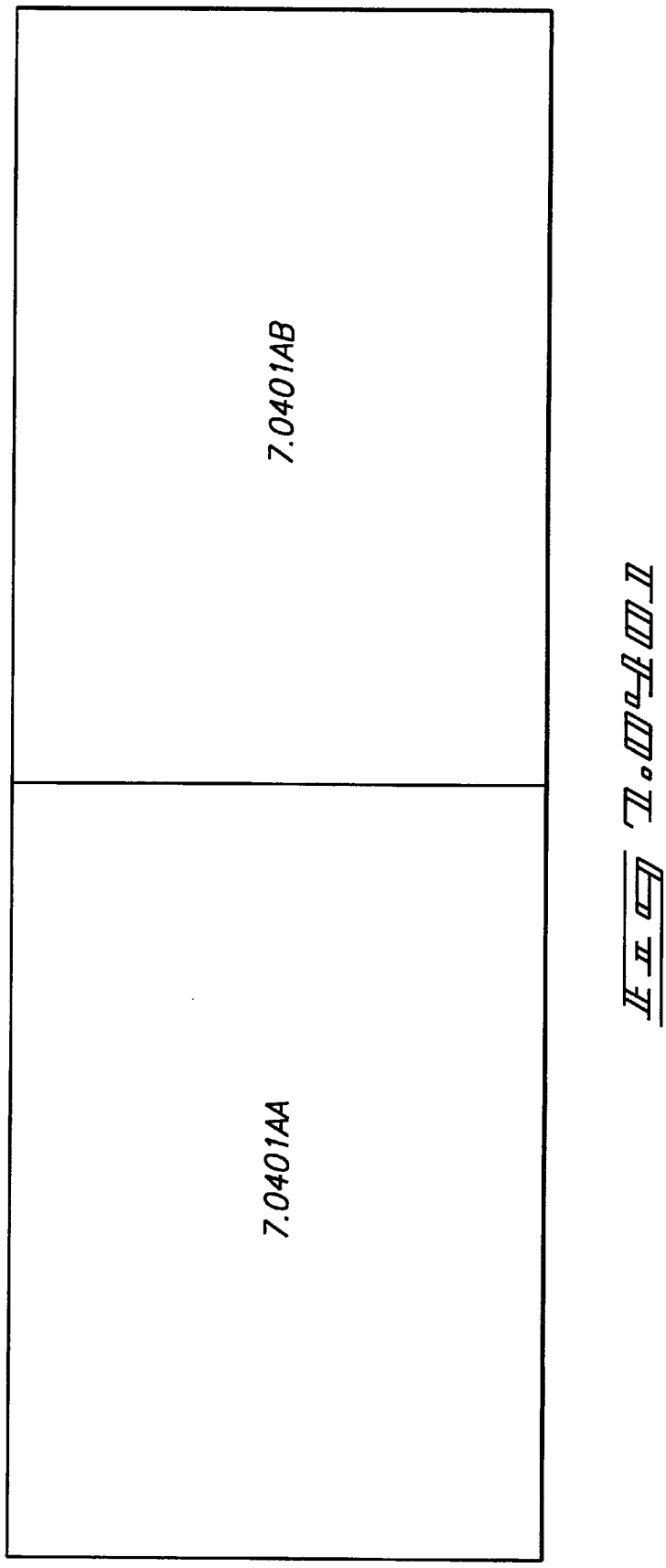

BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
rompch
ROM BIT LINE PRECHARGE
I15140
rompch
ROM BIT LINE PRECHARGE
I16325
rompch
ROM BIT LINE PRECHARGE
I13020

FIG. 1,000,611


7.0401AB
7.0401AA
FIG. 7.0401

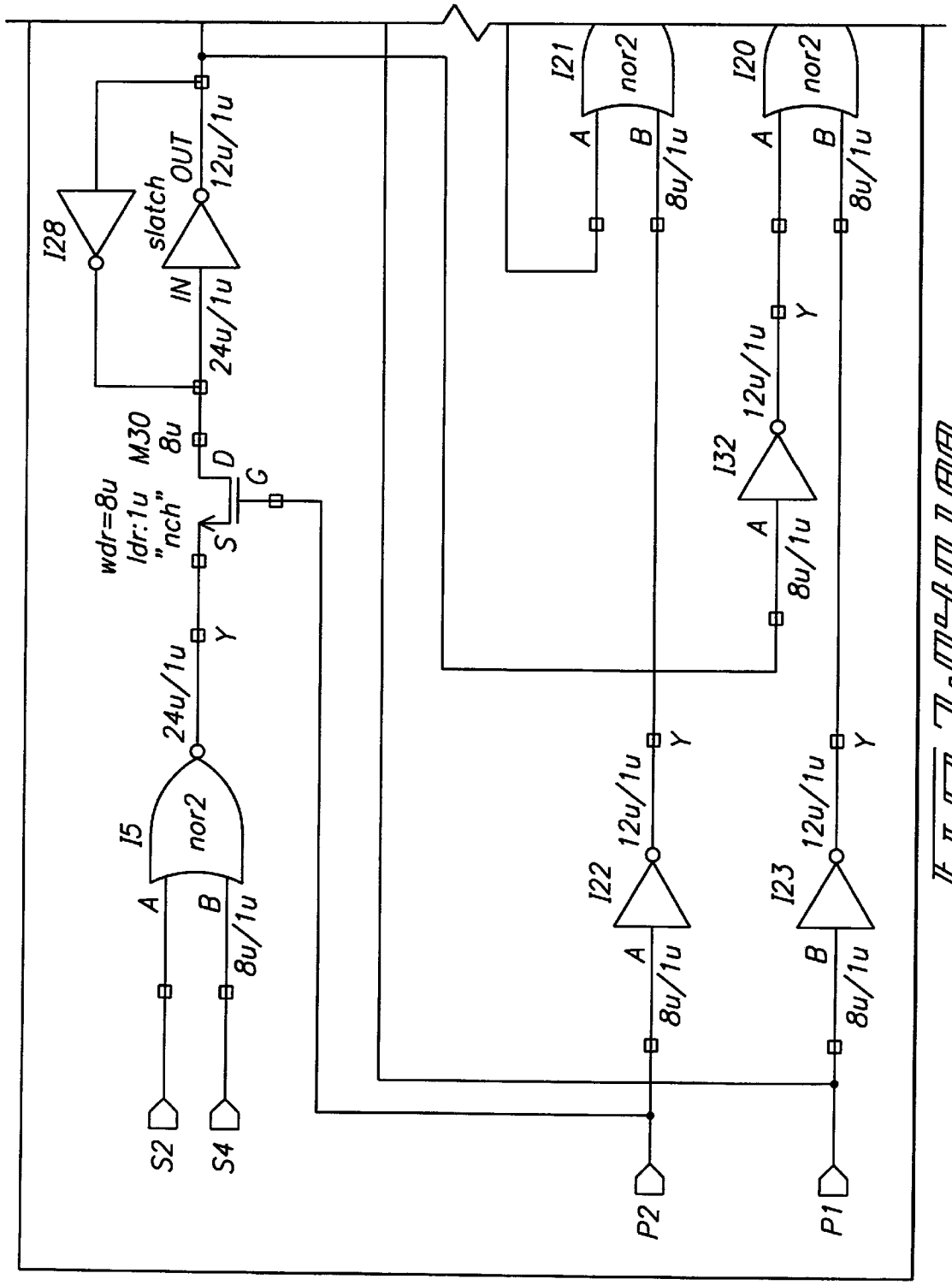

I28
slatch
OUT
IN
12u/1u
24u/1u
M30
8u
wdr=8u
ldr:1u
"nch"
D
G
S
Y
24u/1u
I5
nor2
A
B
8u/1u
S2
S4
I21
nor2
I20
nor2
12u/1u
I32
I22
I23
P2
P1

FIG. 1,004,044

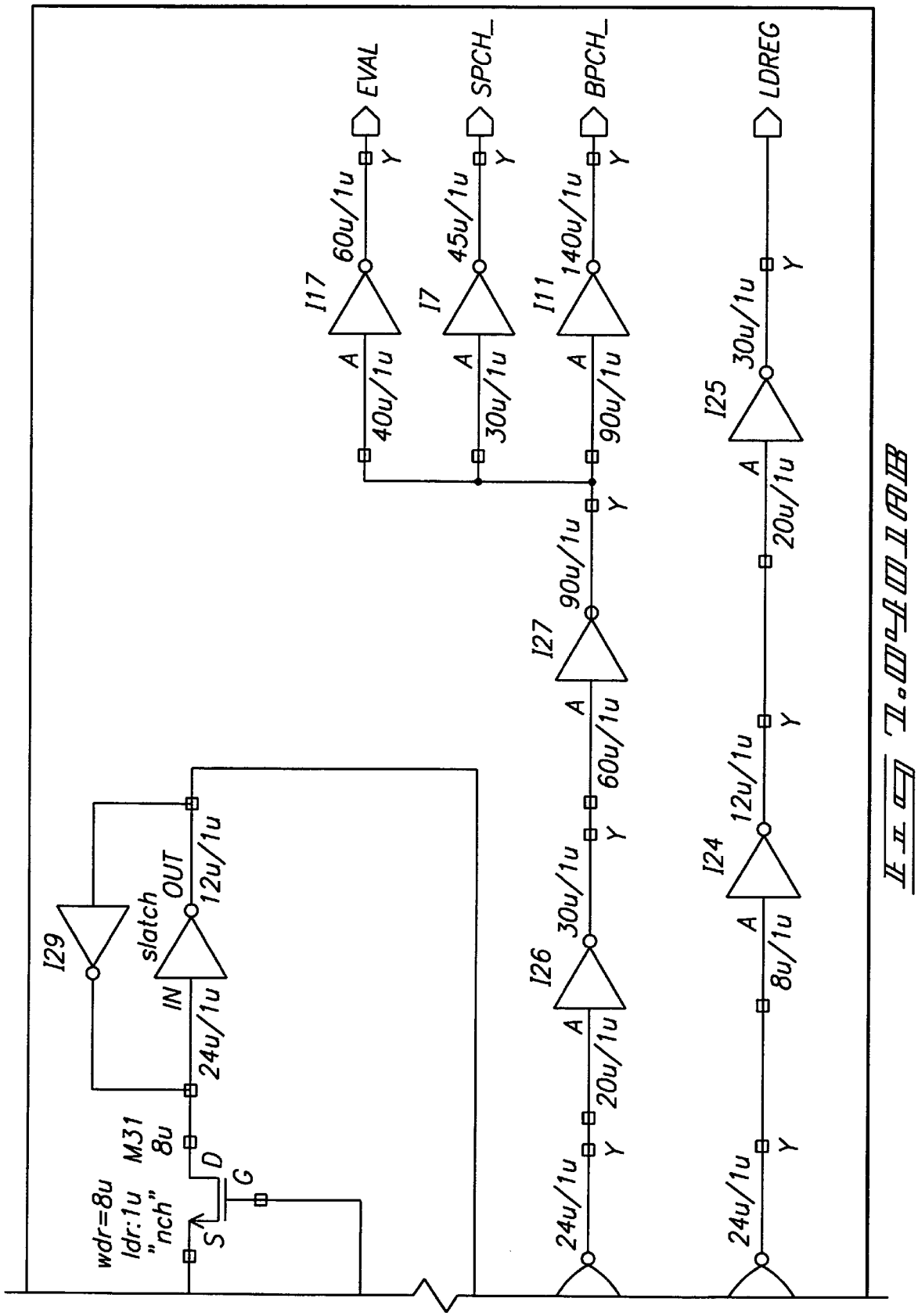
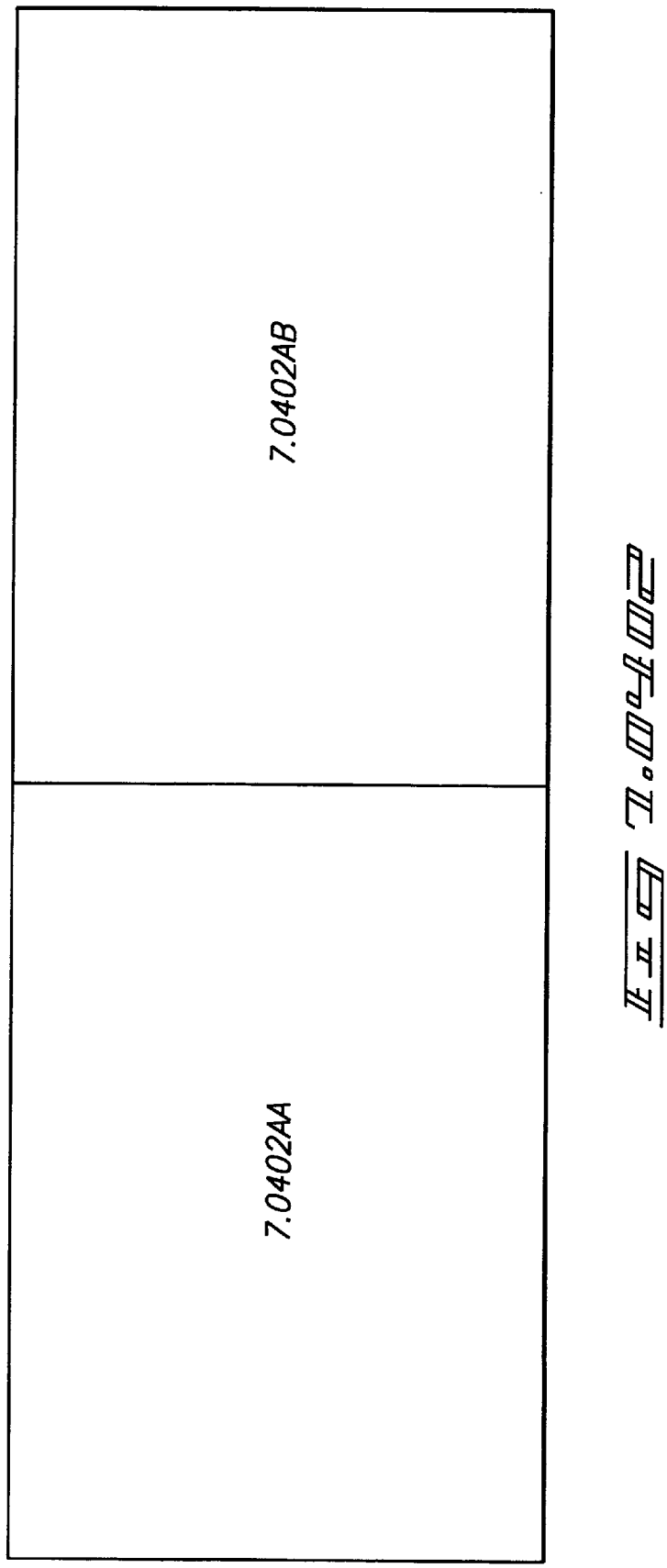

I29
slatch
OUT
IN
12u/1u
24u/1u
M31
8u
wdr=8u
ldr:1u
"nch"
D
G
S
I17
60u/1u
40u/1u
EVAL
I7
45u/1u
30u/1u
SPCH_
I11
140u/1u
90u/1u
BPCH_
I27
90u/1u
60u/1u
I26
30u/1u
20u/1u
24u/1u
I25
30u/1u
20u/1u
LDREG
I24
12u/1u
8u/1u
24u/1u
A
Y

FIG. 11


7.0402AB
7.0402AA
FIG. 7.0402

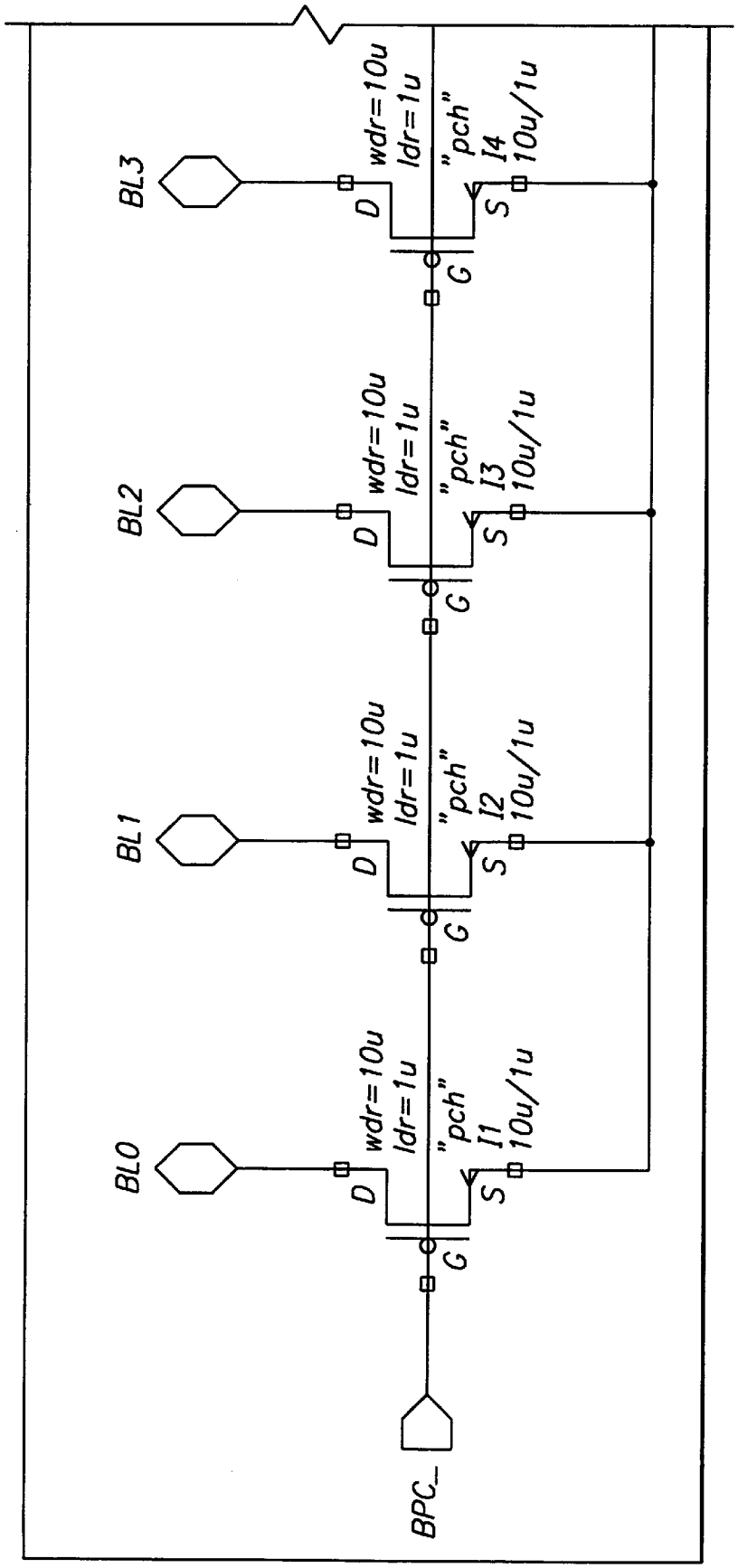


FIG. 7.00 WAVEFORM

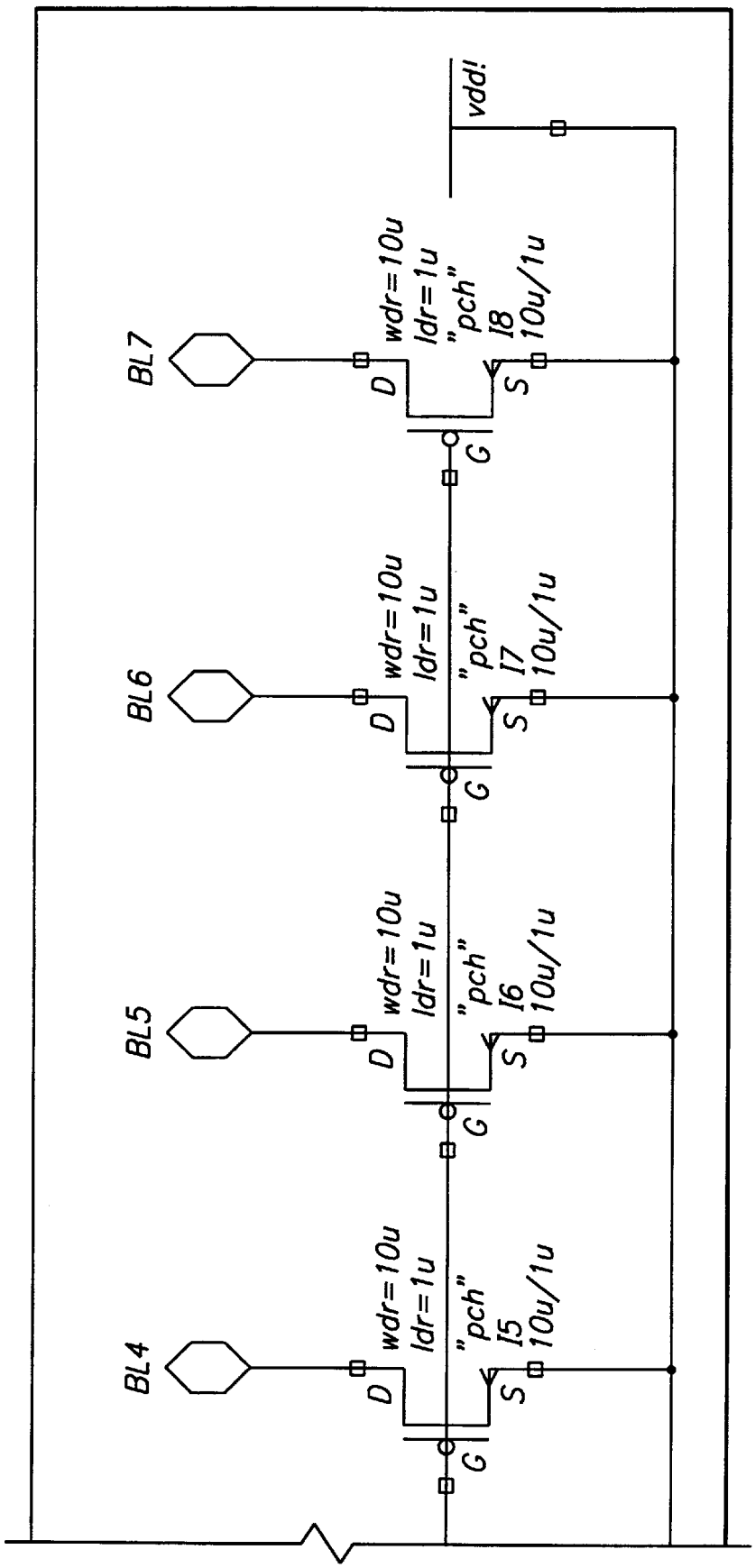

vdd!
BL7
BL6
BL5
BL4
D
G
S
wdr=10u
ldr=1u
"pch"
I8 10u/1u
I7 10u/1u
I6 10u/1u
I5 10u/1u

FIG. 1.004AB

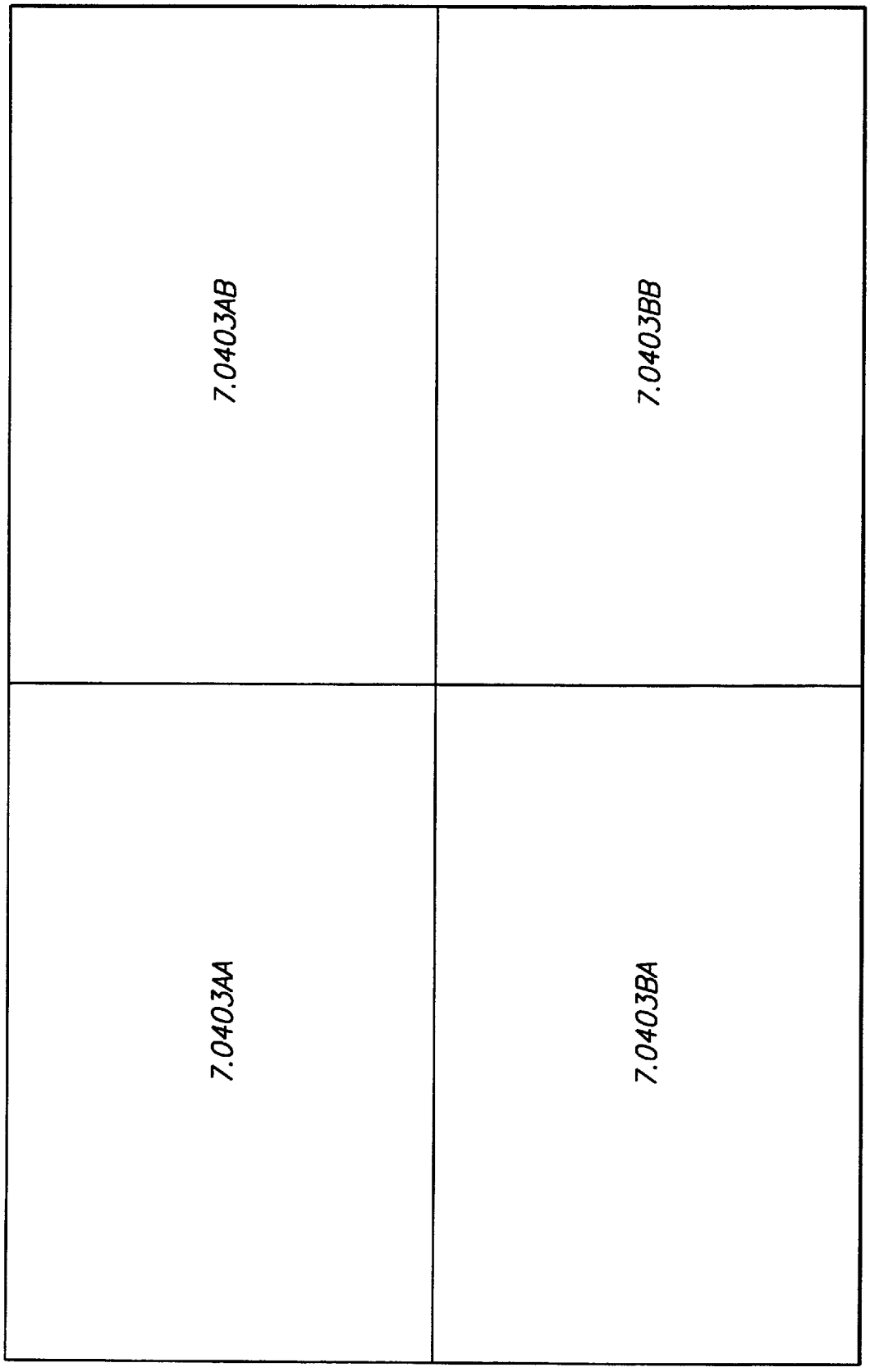


FIG 7.0403

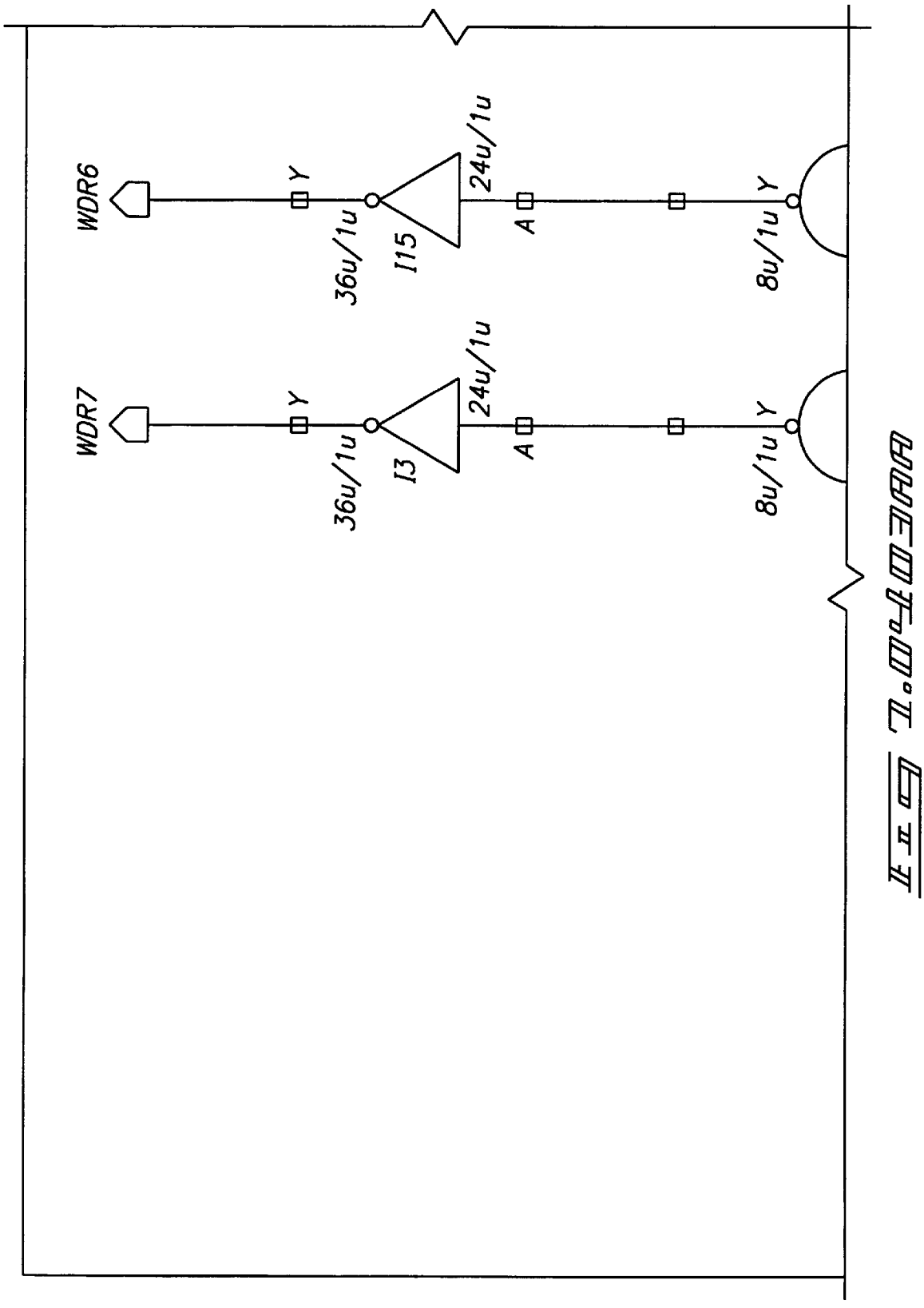


FIG. 70.01

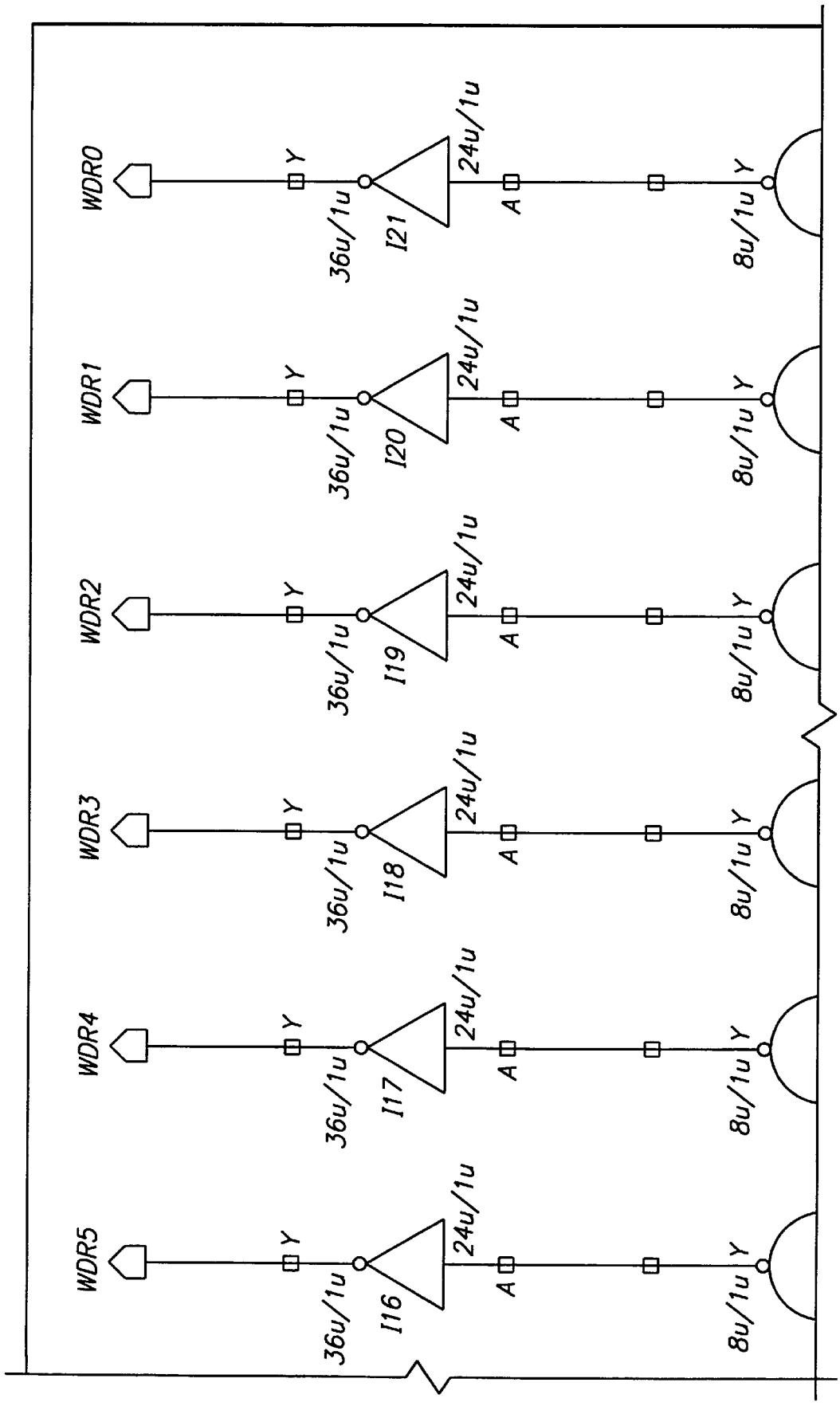

WDR0
WDR1
WDR2
WDR3
WDR4
WDR5
Y
A
36u/1u
24u/1u
8u/1u
I21
I20
I19
I18
I17
I16

FIG. 1.0047E

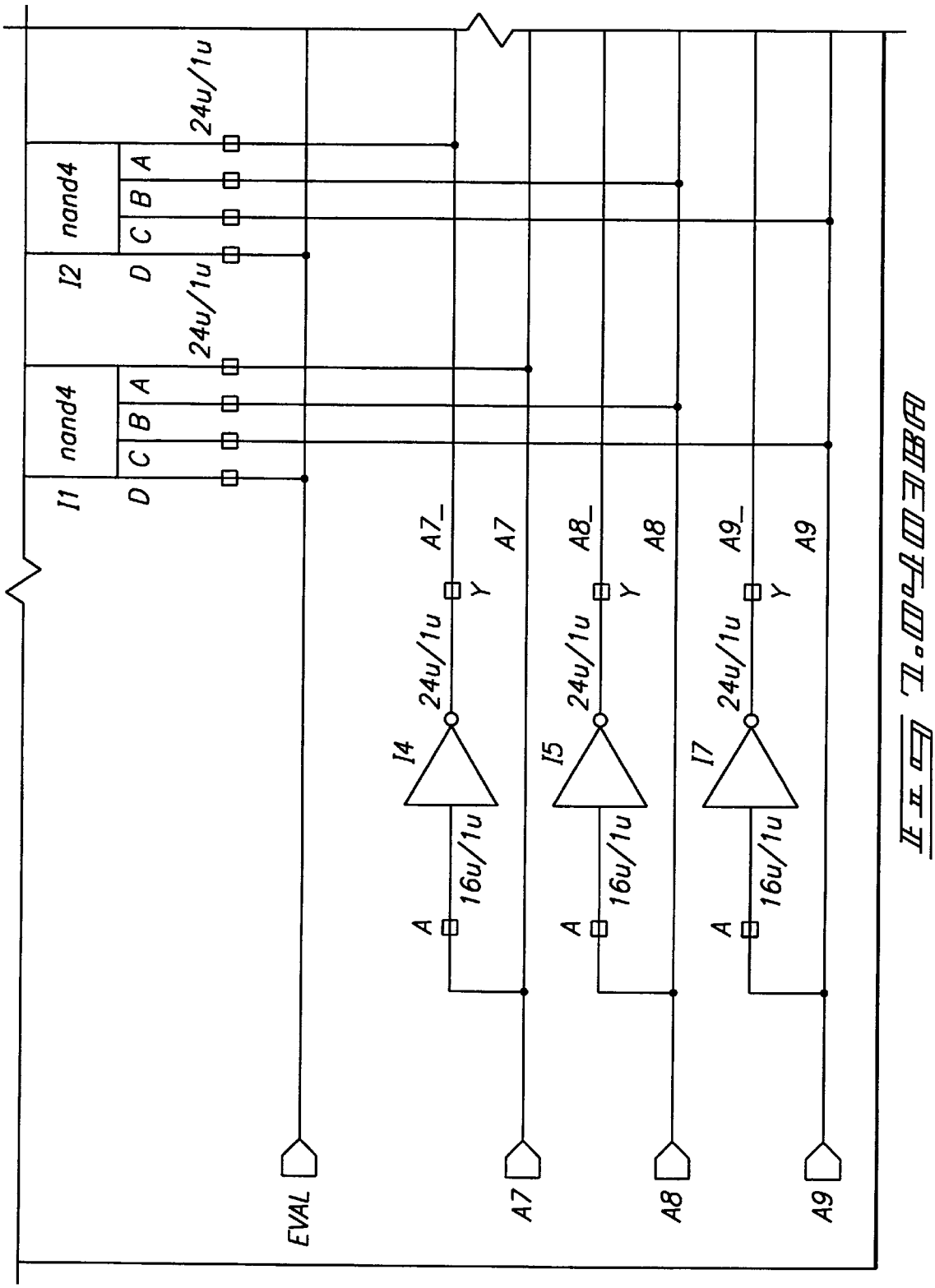

I1
nand4
A
B
C
D
24u/1u
I2
nand4
A
B
C
D
24u/1u
I4
I5
I7
24u/1u
16u/1u
A
Y
A7_
A8_
A9_
A7
A8
A9
EVAL
A7
A8
A9

FIG. 11

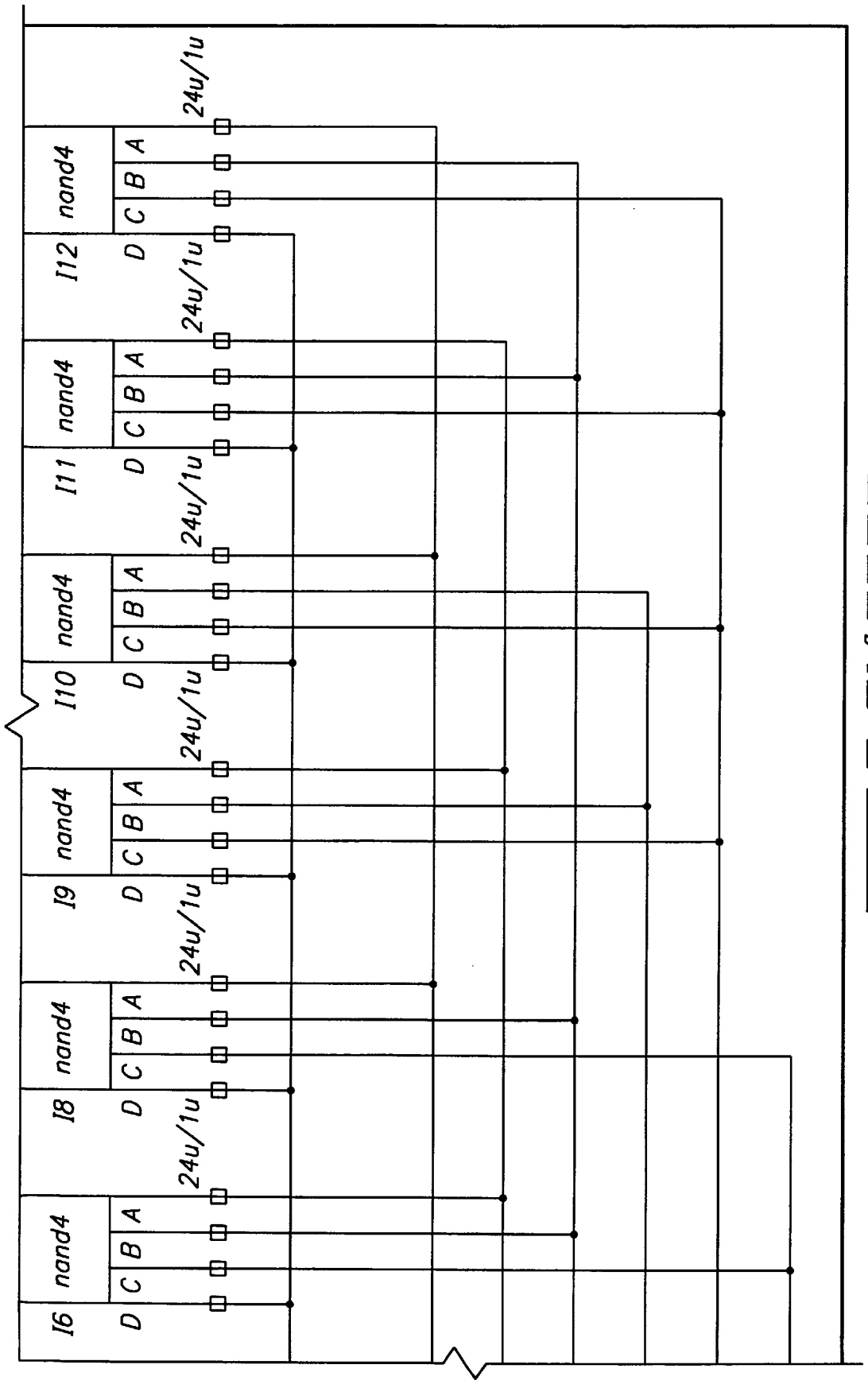

I16 nand4 A B C D 24u/1u
I8 nand4 A B C D 24u/1u
I9 nand4 A B C D 24u/1u
I10 nand4 A B C D 24u/1u
I11 nand4 A B C D 24u/1u
I12 nand4 A B C D 24u/1u

FIG. 388

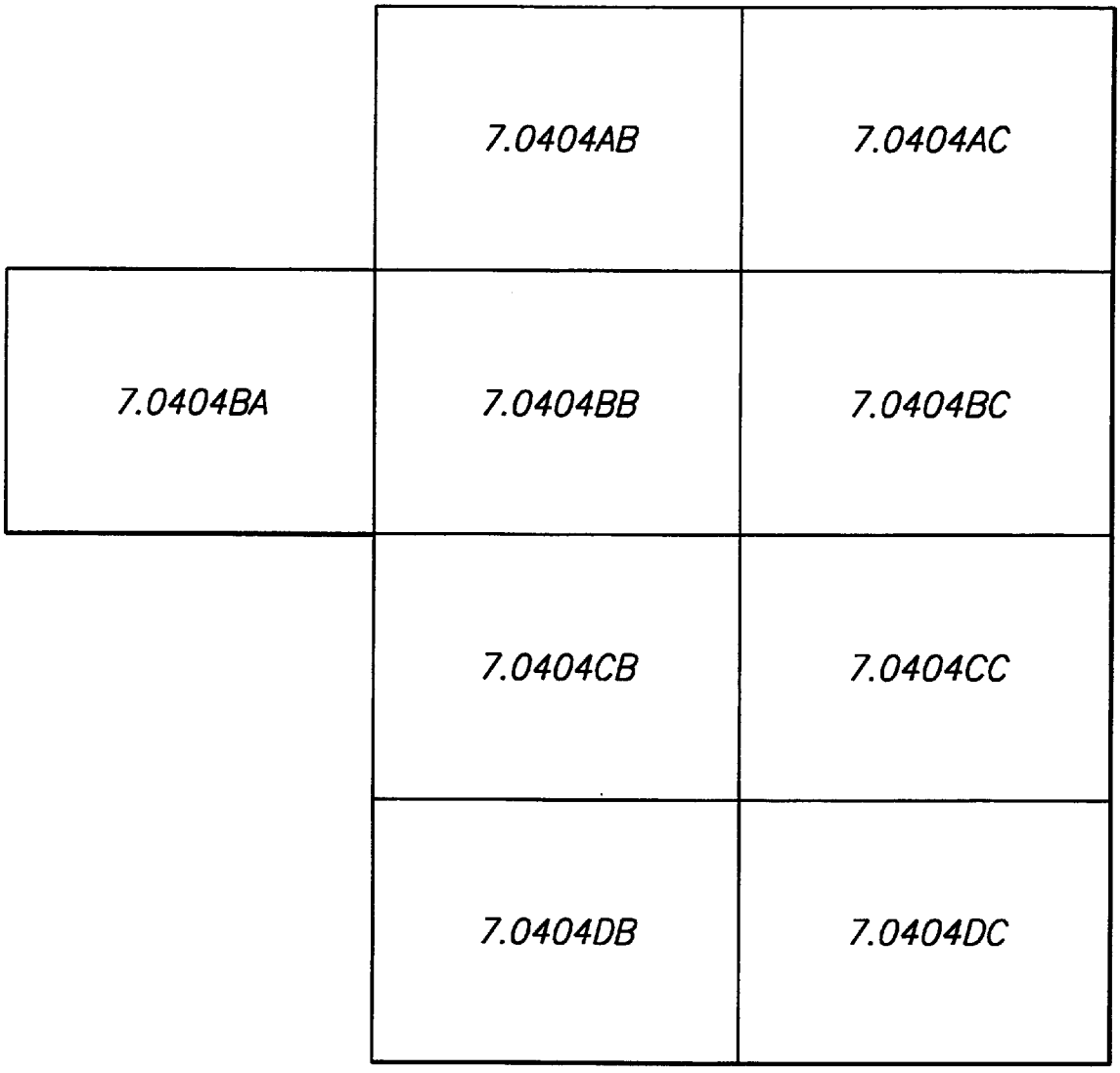

7.0404AB
7.0404AC
7.0404BA
7.0404BB
7.0404BC
7.0404CB
7.0404CC
7.0404DB
7.0404DC

Fig 7.0404

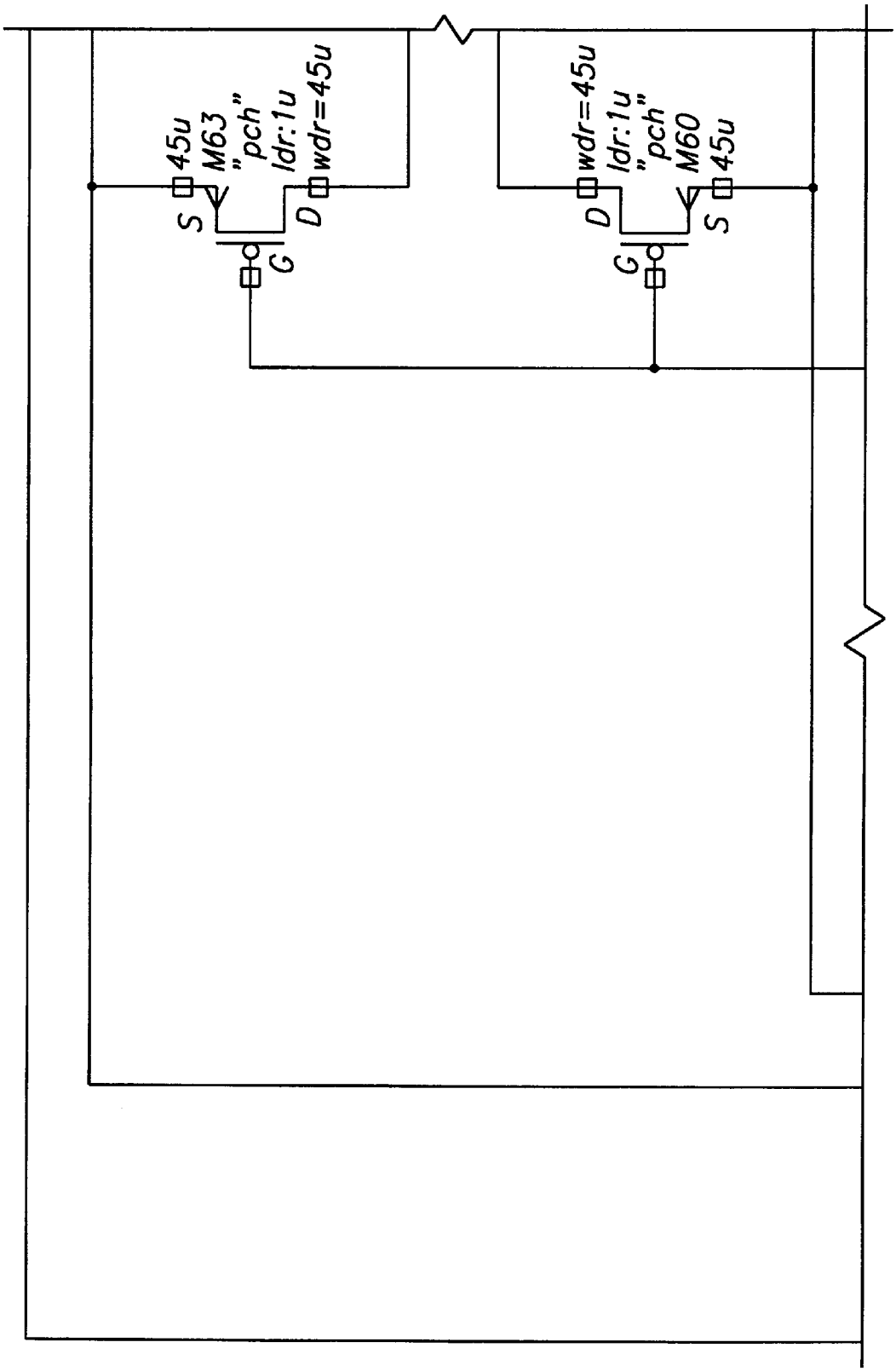
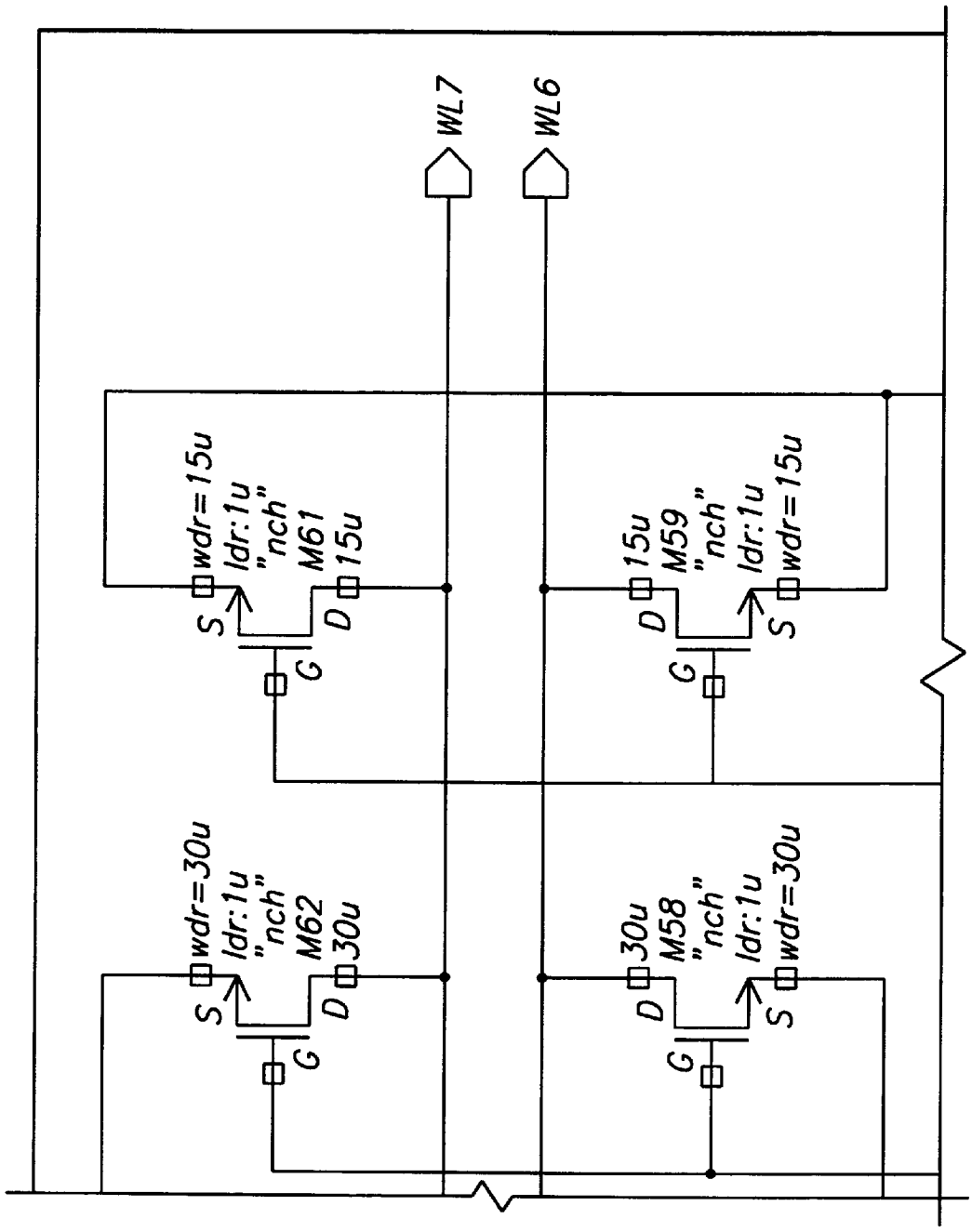


FIG. 390.1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WL6
wdr=15u
ldr:1u
"nch"
M61
15u
S
G
D
15u
M59
"nch"
ldr:1u
wdr=15u
wdr=30u
ldr:1u
"nch"
M62
30u
30u
M58
"nch"
ldr:1u
wdr=30u

ФИГ. 6.00.11

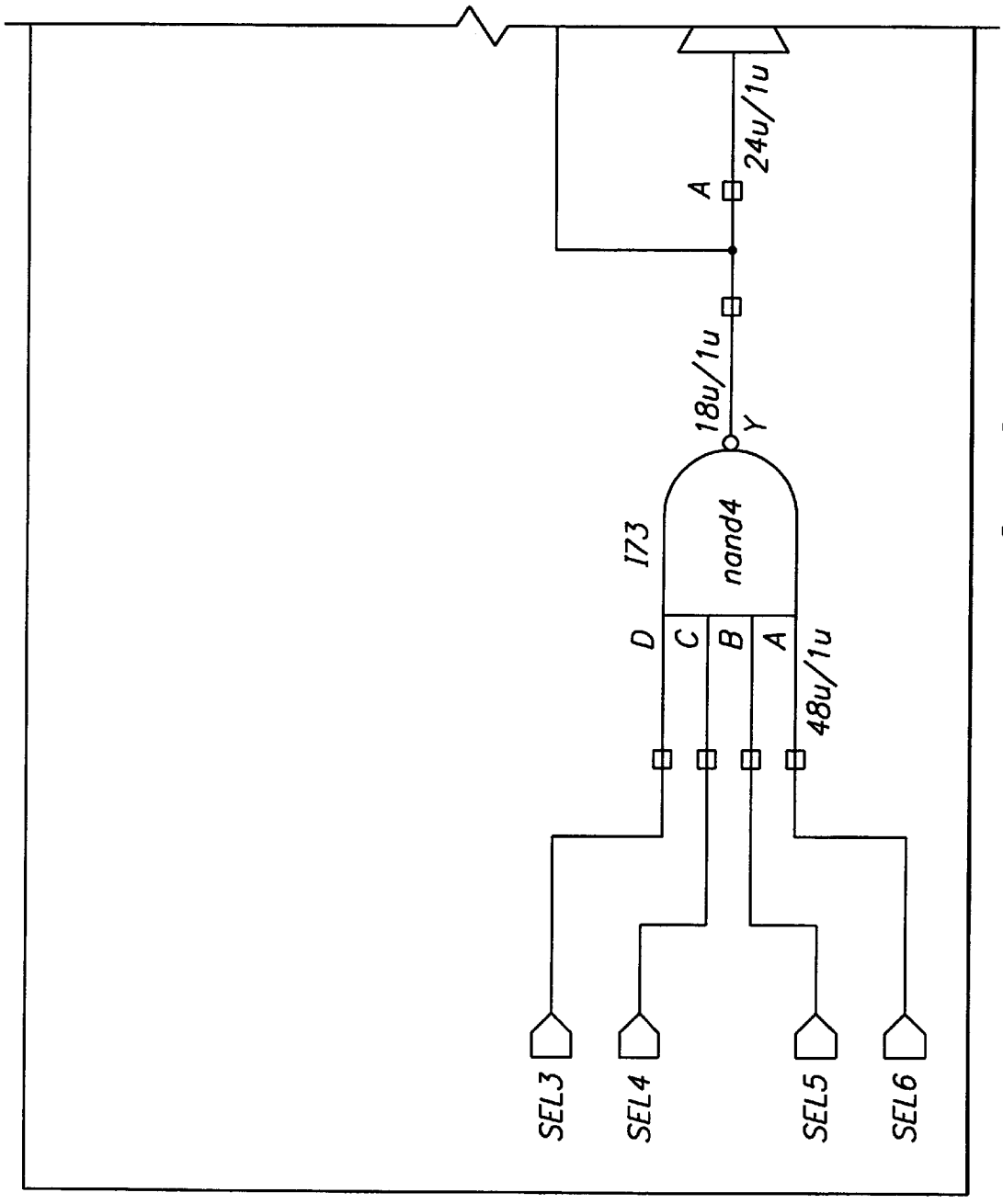
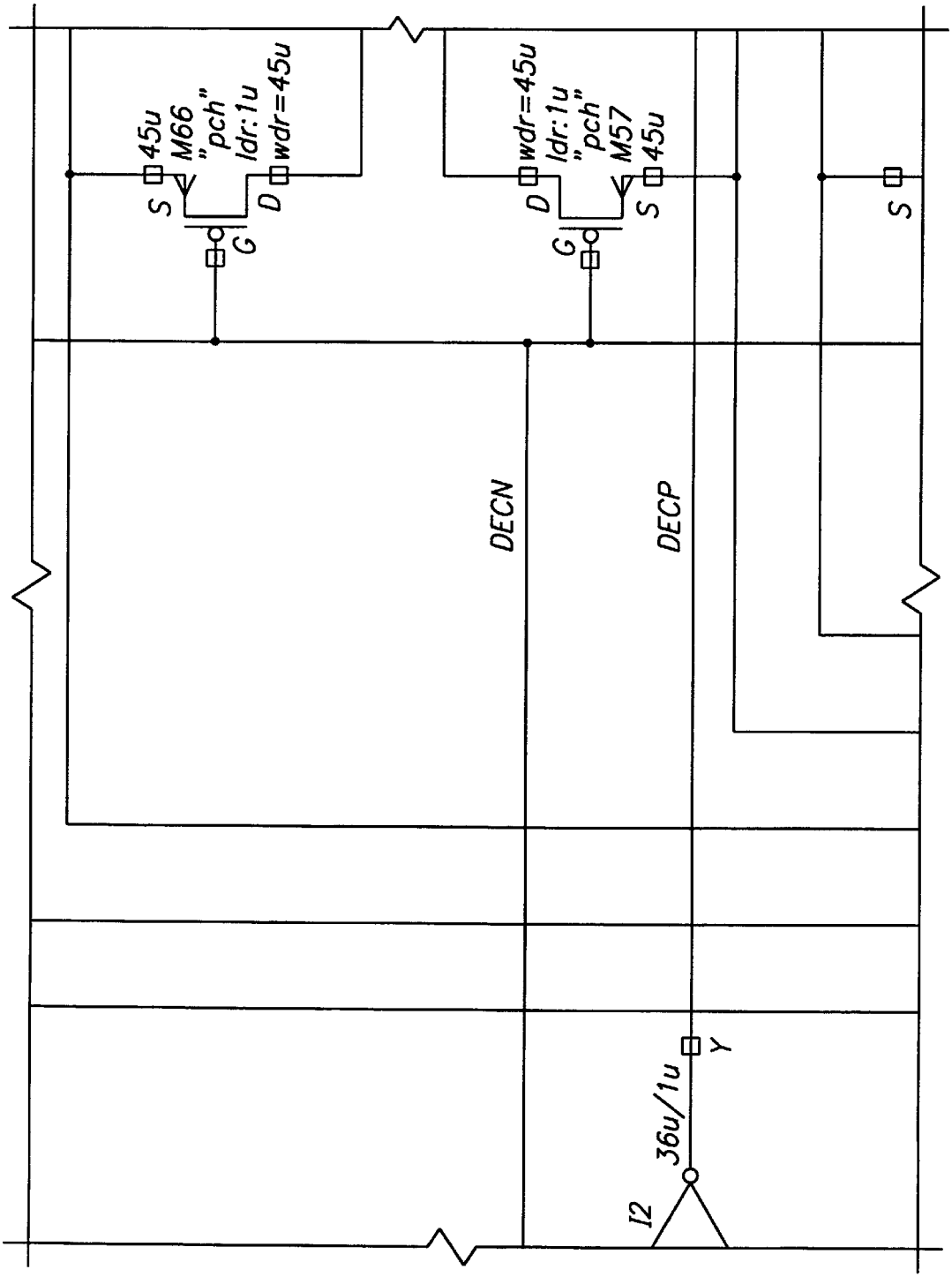
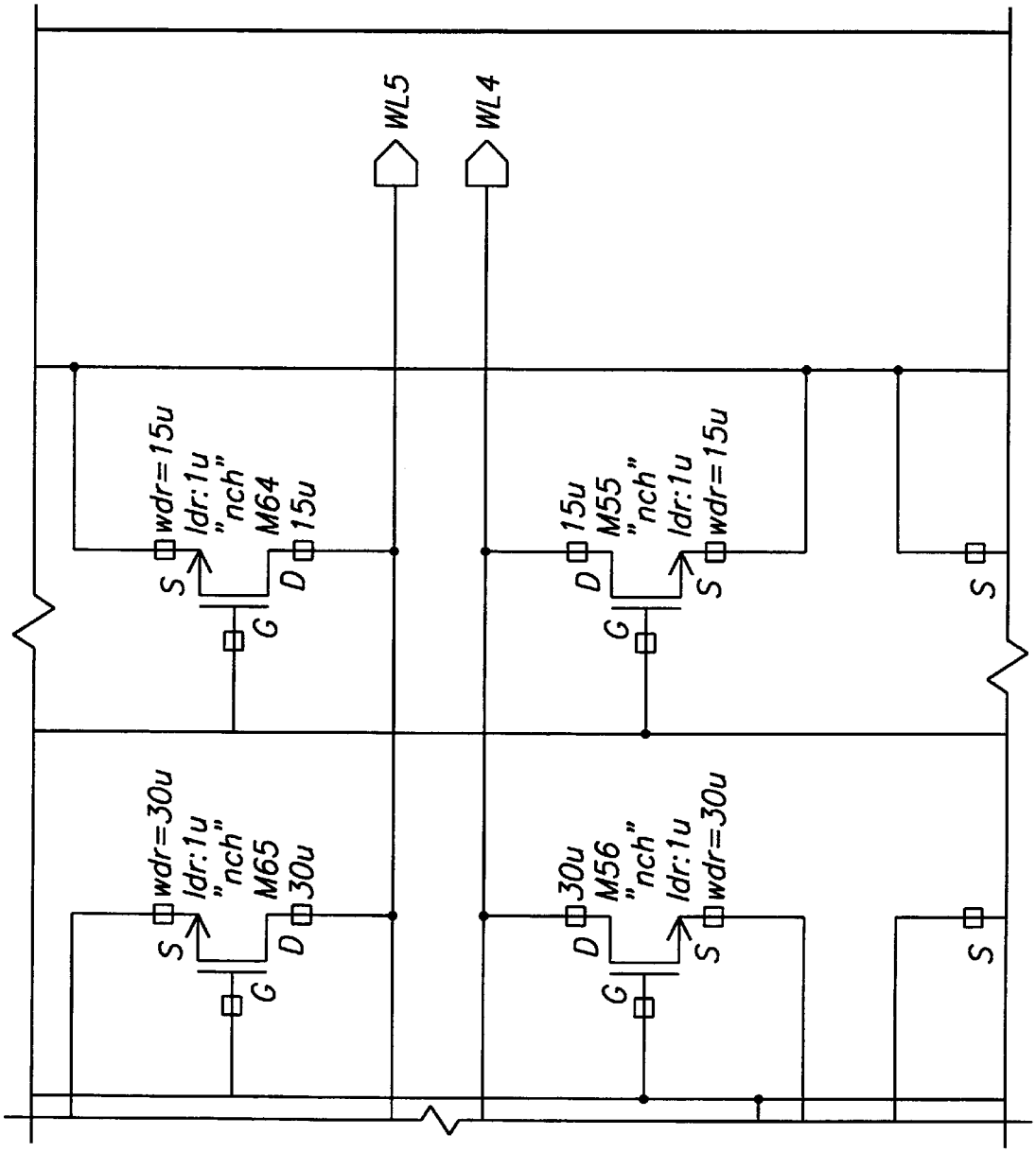


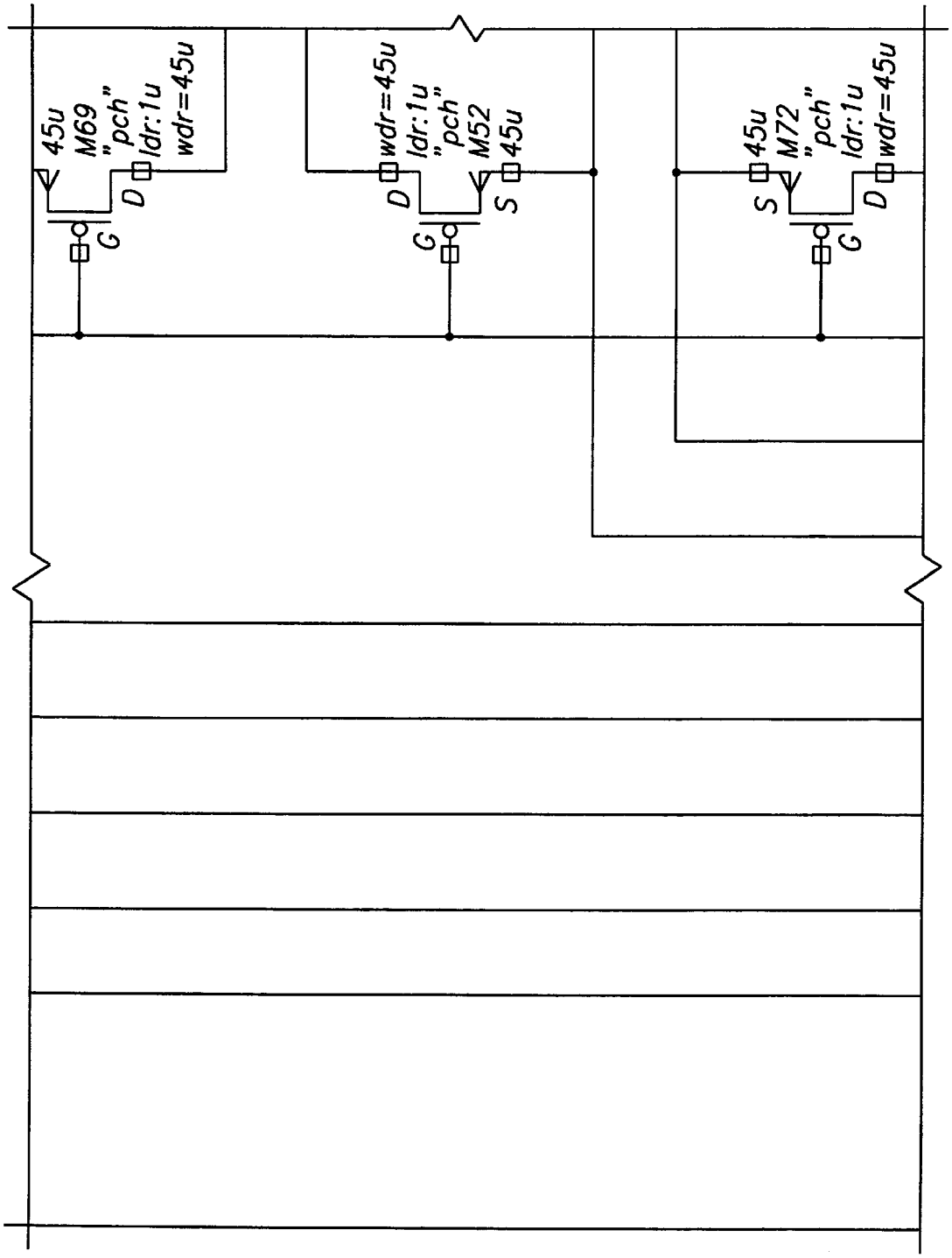
Fig. 1,004,804A


45u
M66
"pch"
ldr:1u
wdr=45u
S
D
G
wdr=45u
ldr:1u
"pch"
M57
45u
D
S
G
S
DECN
DECP
36u/1u
Y
I2

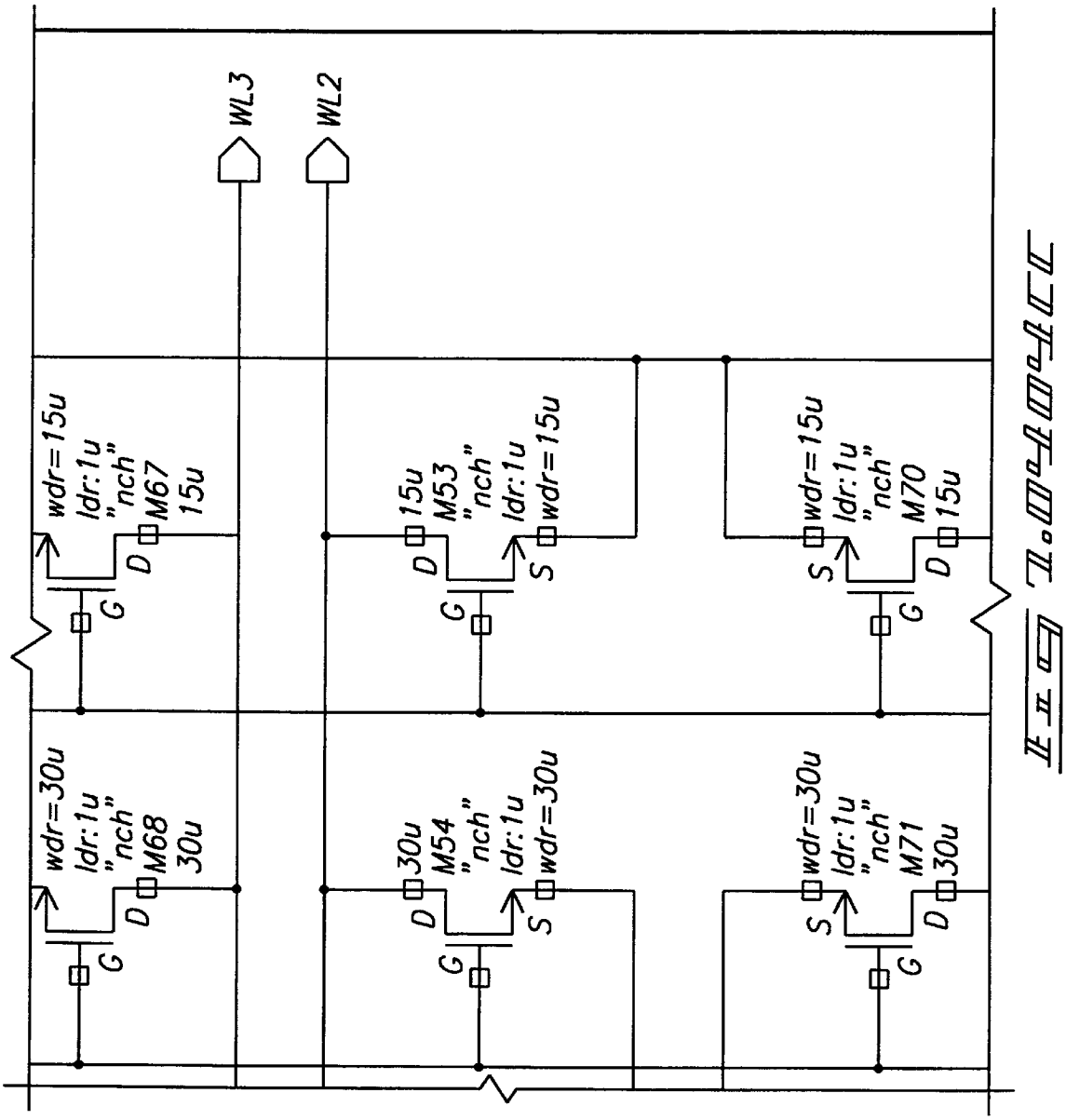
Фиг. 6.04Ф00.Г



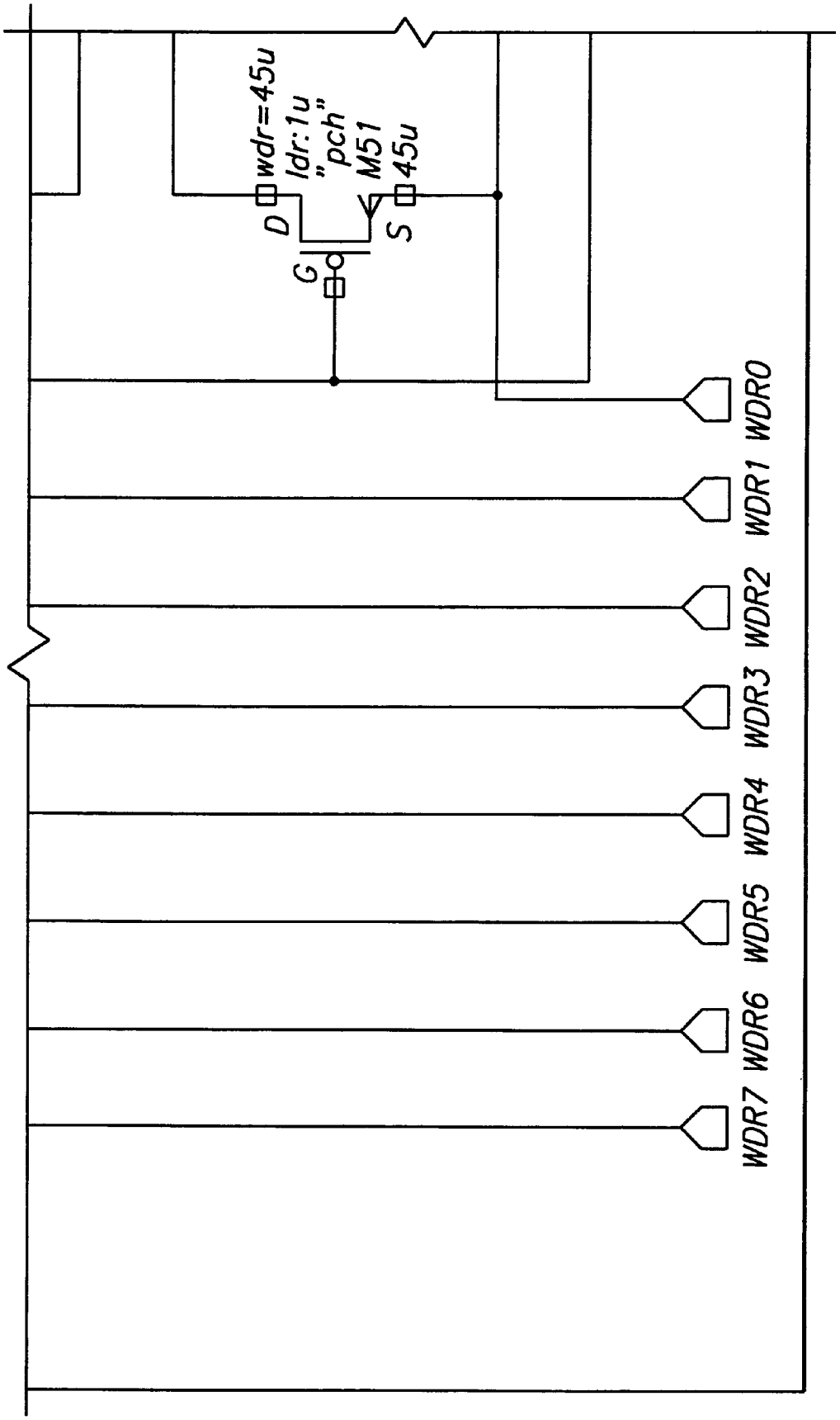
ФИГ 60Ф0.0Е


45u
M69
"pch"
ldr:1u
wdr=45u
D
G
wdr=45u
ldr:1u
"pch"
M52
45u
D
G
S
45u
M72
"pch"
ldr:1u
wdr=45u
S
G
D

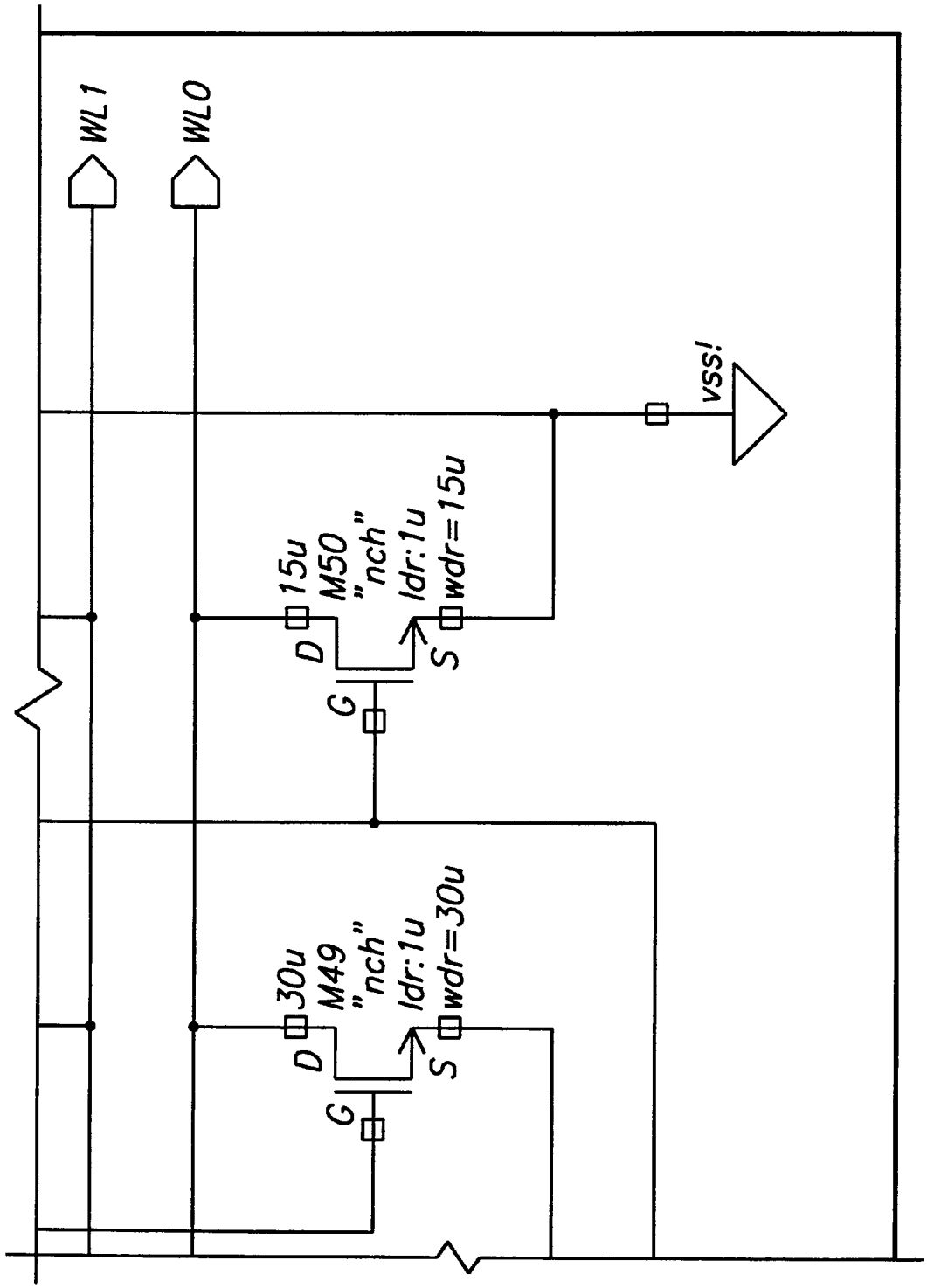
Фиг. 11,004


WL3
WL2
wdr=15u
ldr:1u
"nch"
M67
15u
D
G
15u
M53
"nch"
ldr:1u
wdr=15u
S
wdr=15u
ldr:1u
"nch"
M70
15u
wdr=30u
ldr:1u
"nch"
M68
30u
30u
M54
"nch"
ldr:1u
wdr=30u
wdr=30u
ldr:1u
"nch"
M71
30u

Фиг. 6.00.0L


wdr=45u
ldr:1u
"pch"
M51
45u
D
G
S
WDR0
WDR1
WDR2
WDR3
WDR4
WDR5
WDR6
WDR7

ФИГ. 1,004


WL1
WL0
vss!
15u
M50
"nch"
ldr:1u
wdr=15u
D
G
S
30u
M49
"nch"
ldr:1u
wdr=30u
D
G
S

Фиг. 6.00.11

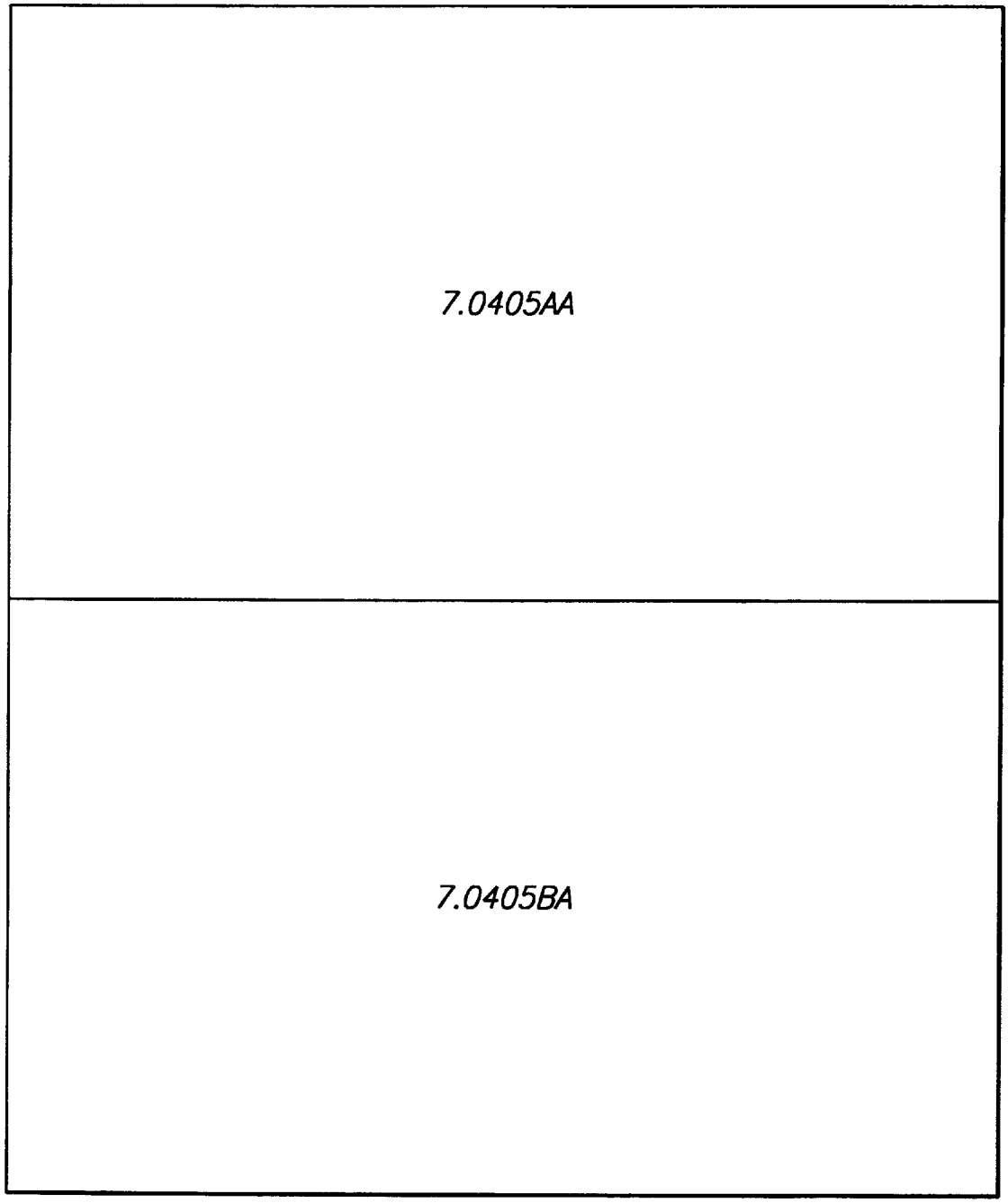
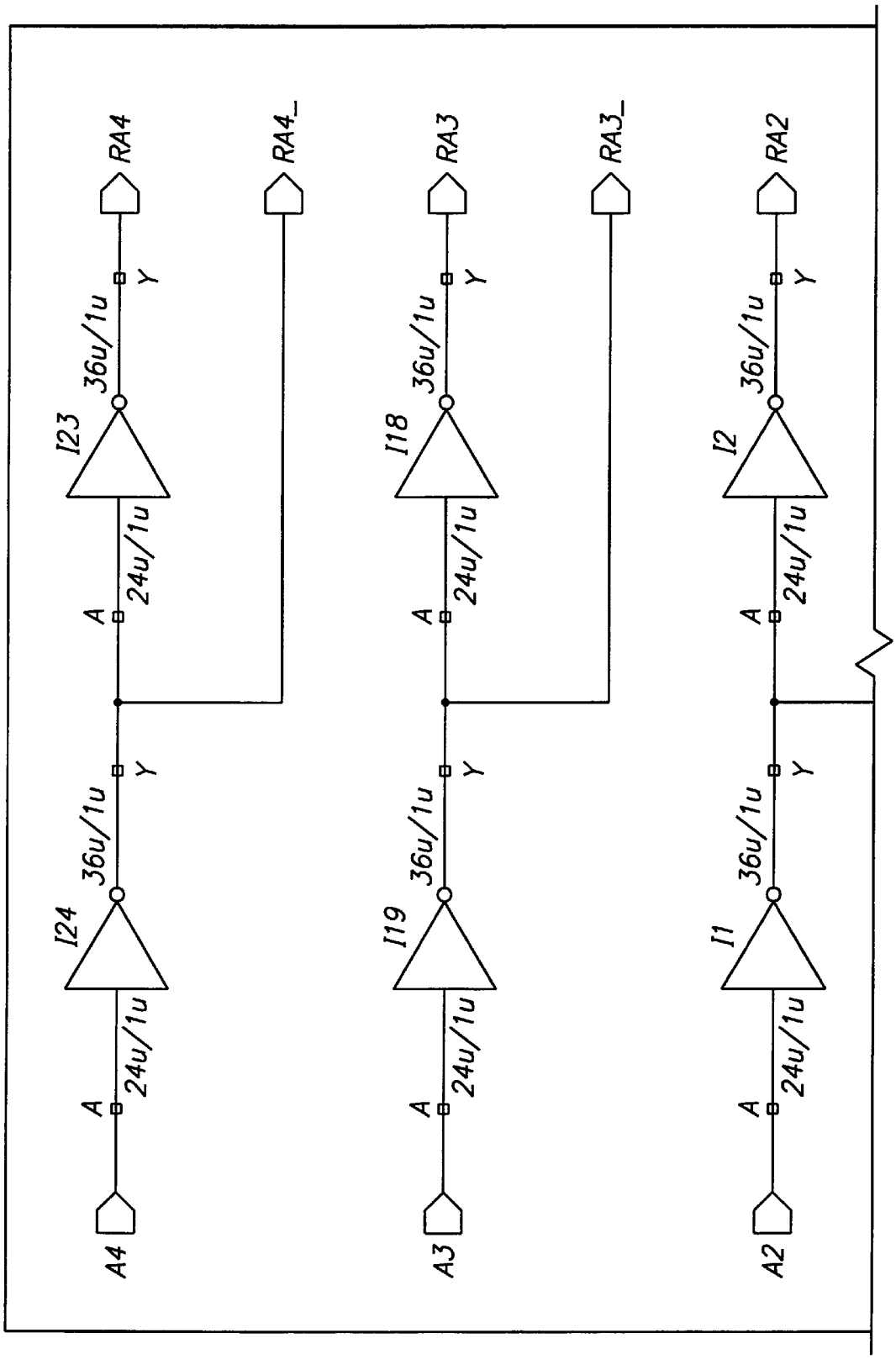


Fig 7.0405



Фиг. 400.2

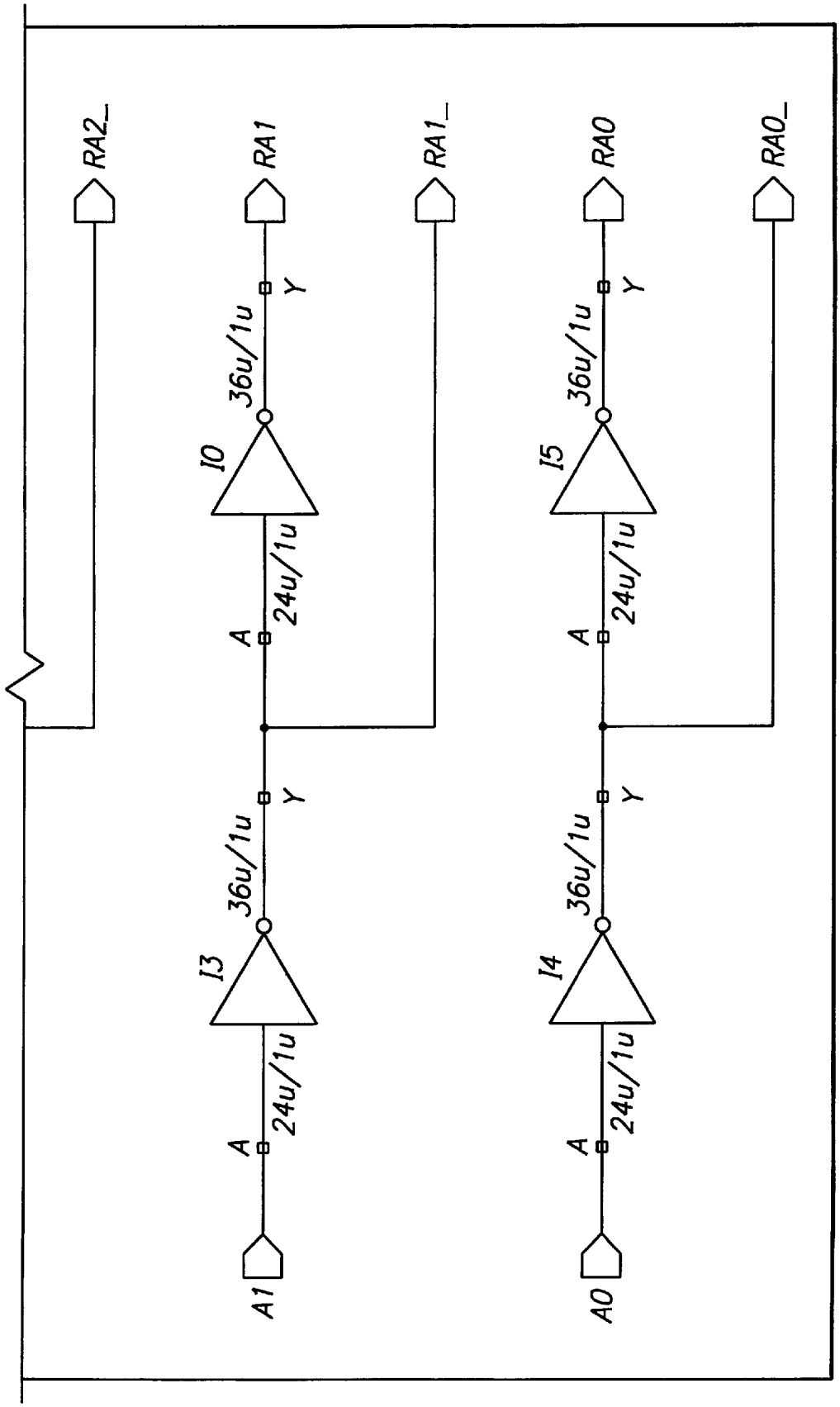


FIG 6A0.1

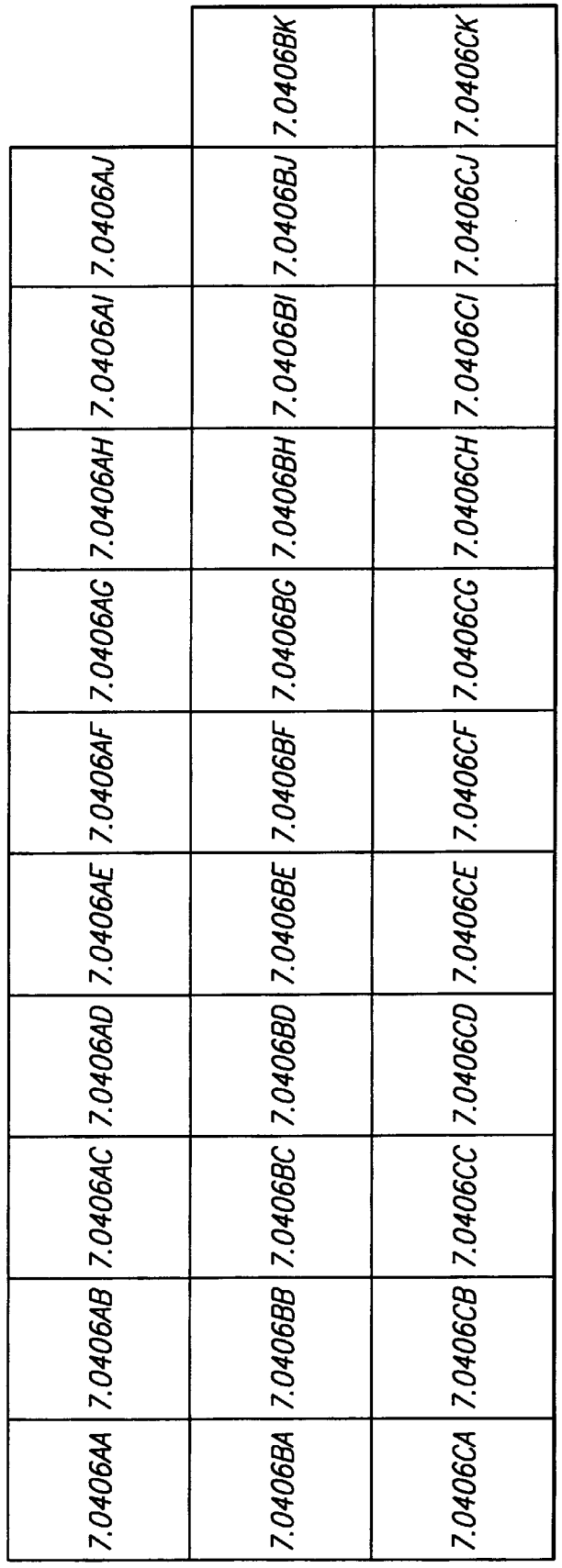

7.0406AA
7.0406AB
7.0406AC
7.0406AD
7.0406AE
7.0406AF
7.0406AG
7.0406AH
7.0406AI
7.0406AJ
7.0406BA
7.0406BB
7.0406BC
7.0406BD
7.0406BE
7.0406BF
7.0406BG
7.0406BH
7.0406BI
7.0406BJ
7.0406BK
7.0406CA
7.0406CB
7.0406CC
7.0406CD
7.0406CE
7.0406CF
7.0406CG
7.0406CH
7.0406CI
7.0406CJ
7.0406CK

FIG. 7.0406

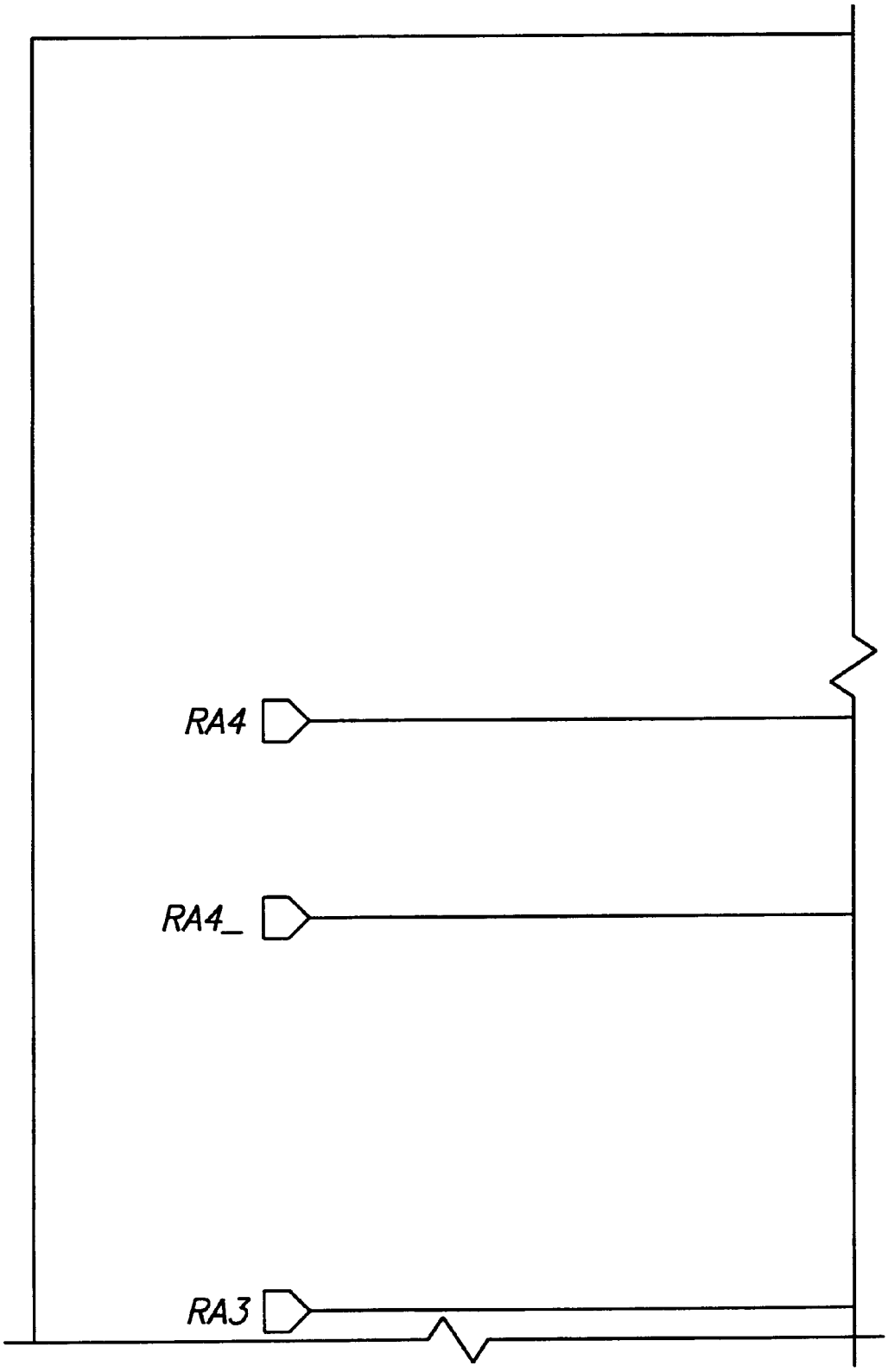


Fig 1.0406AA

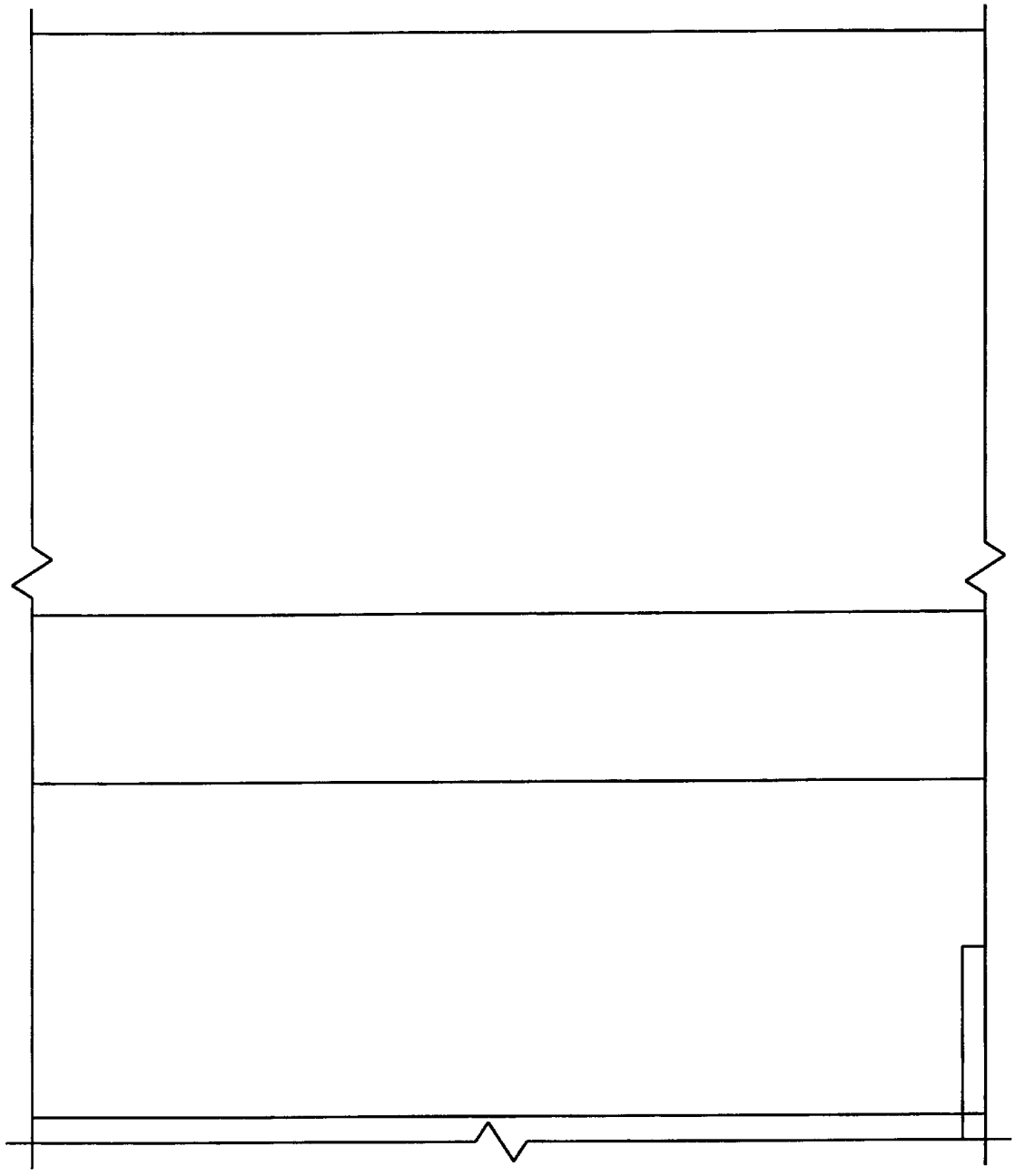


Fig 1.04106AB

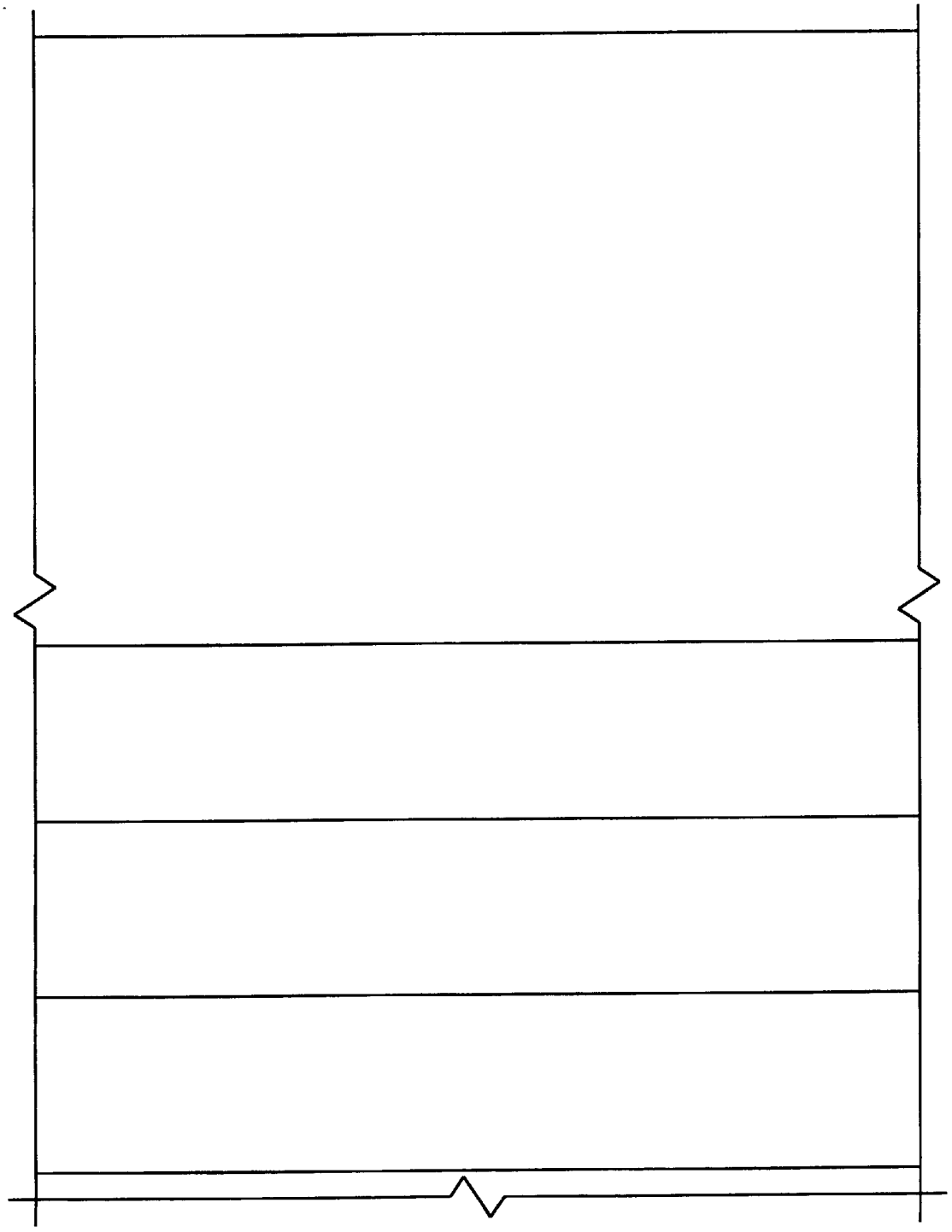


Fig 1.04068AC

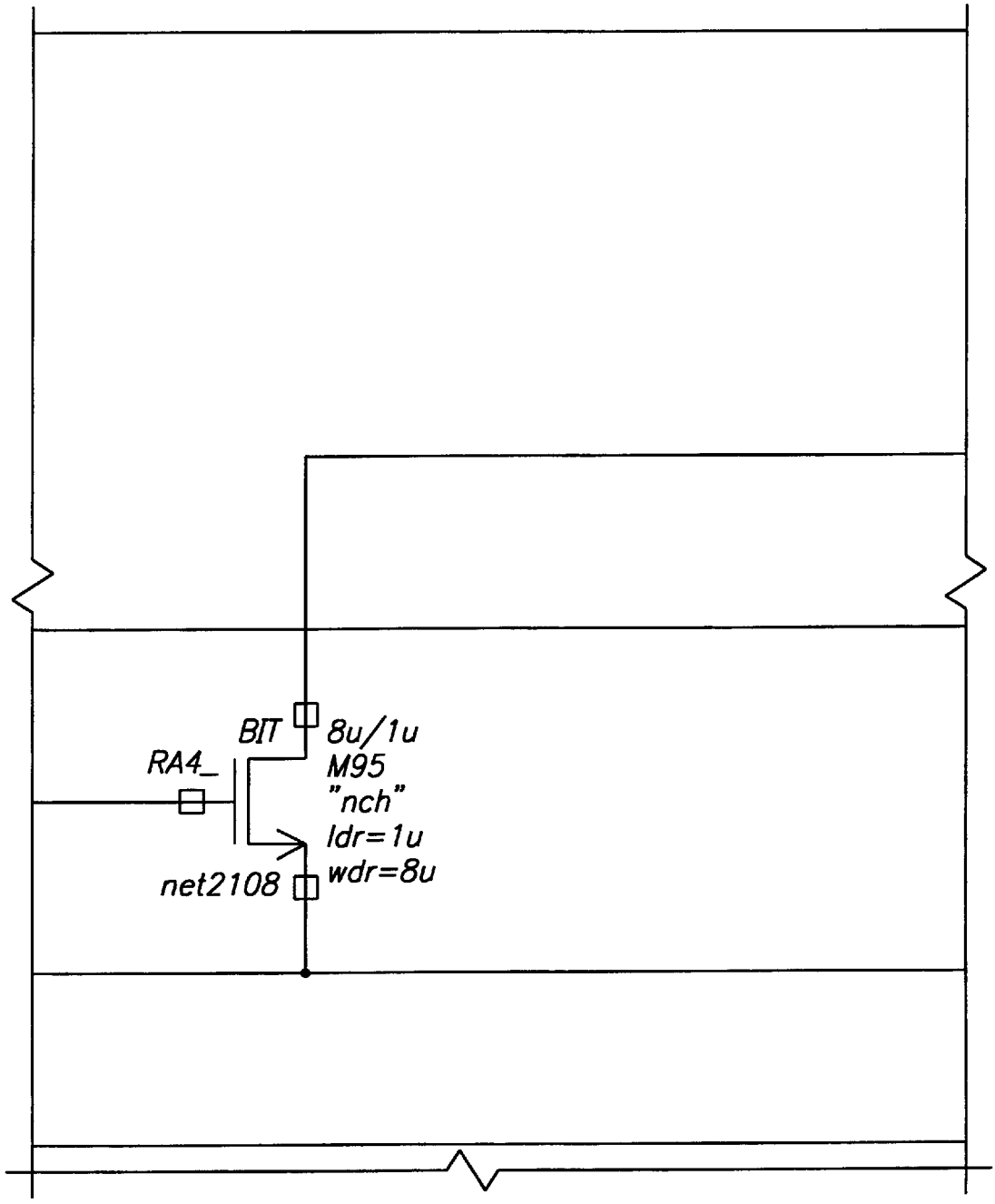


Fig 1.0406AD

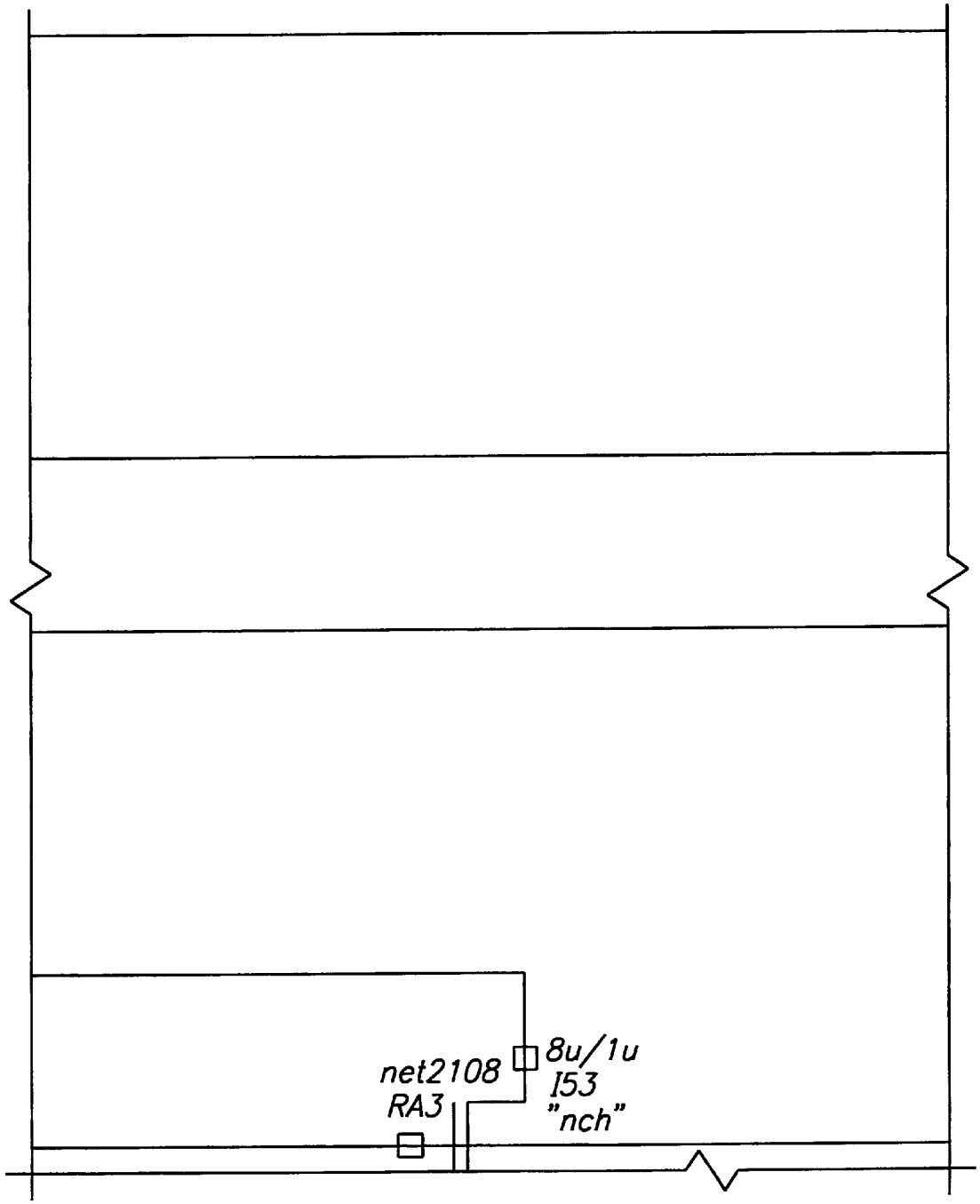


Fig 1.0406AE

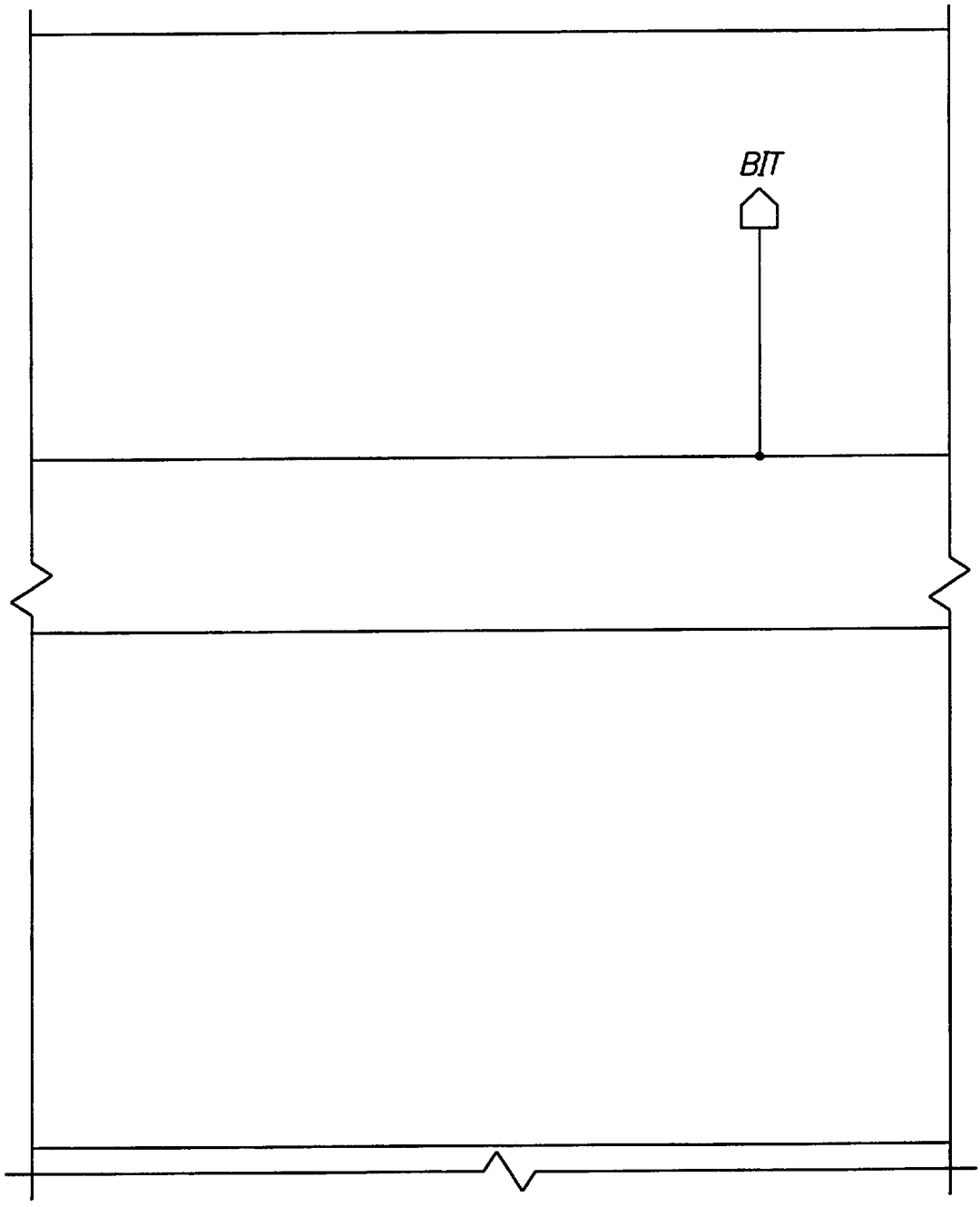


Fig 1.04106AF

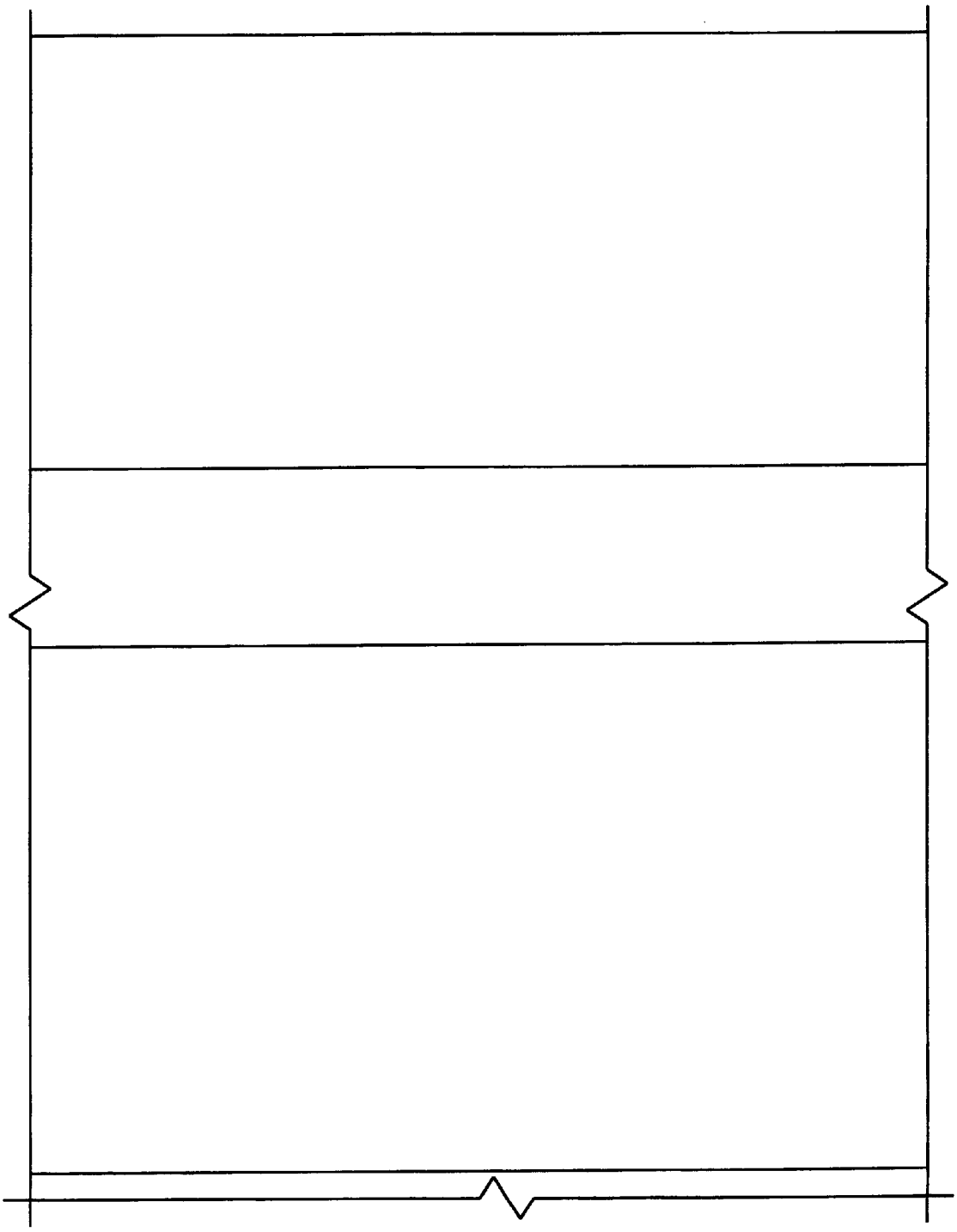


Fig 1.04066AG

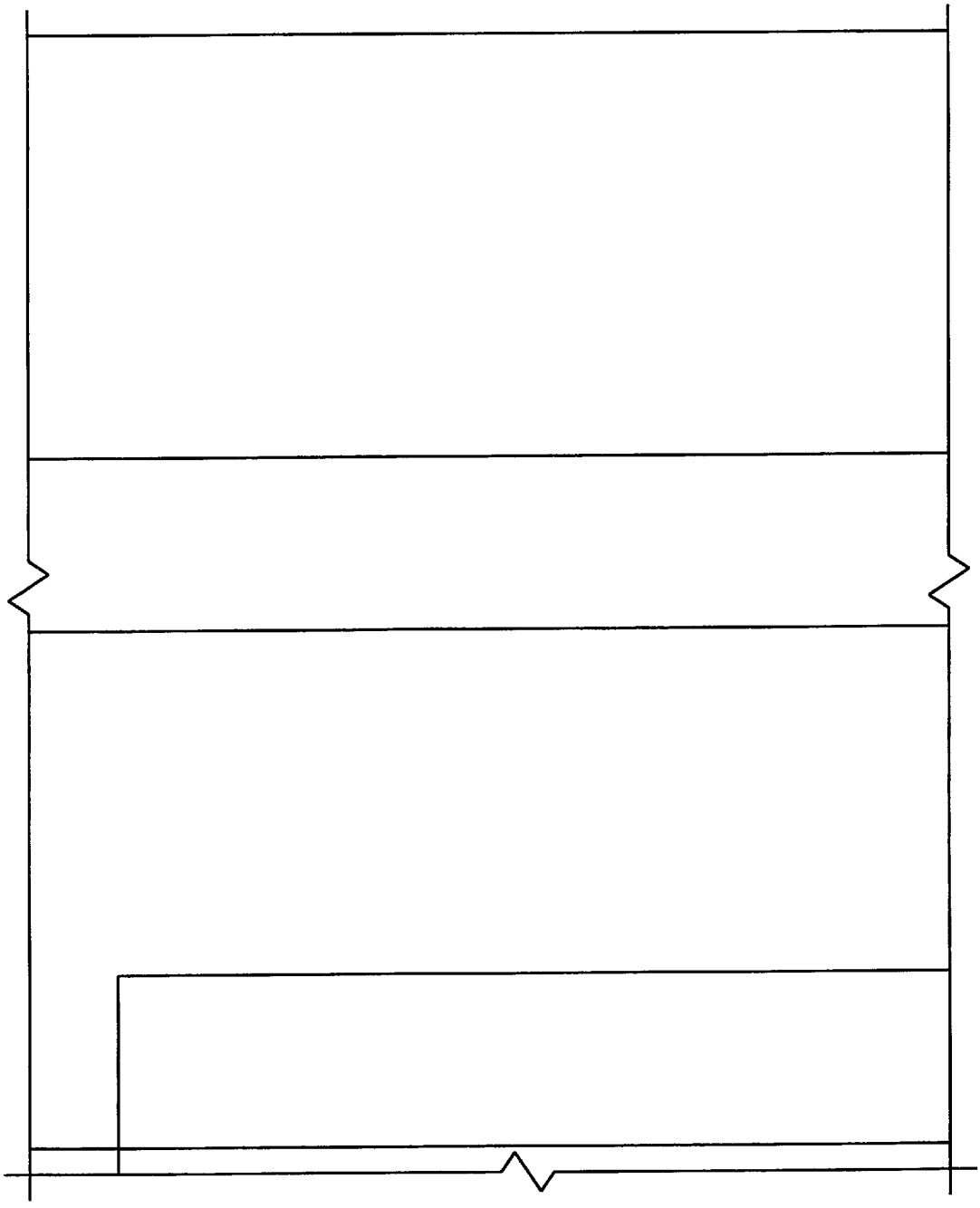


Fig 1.04106AH

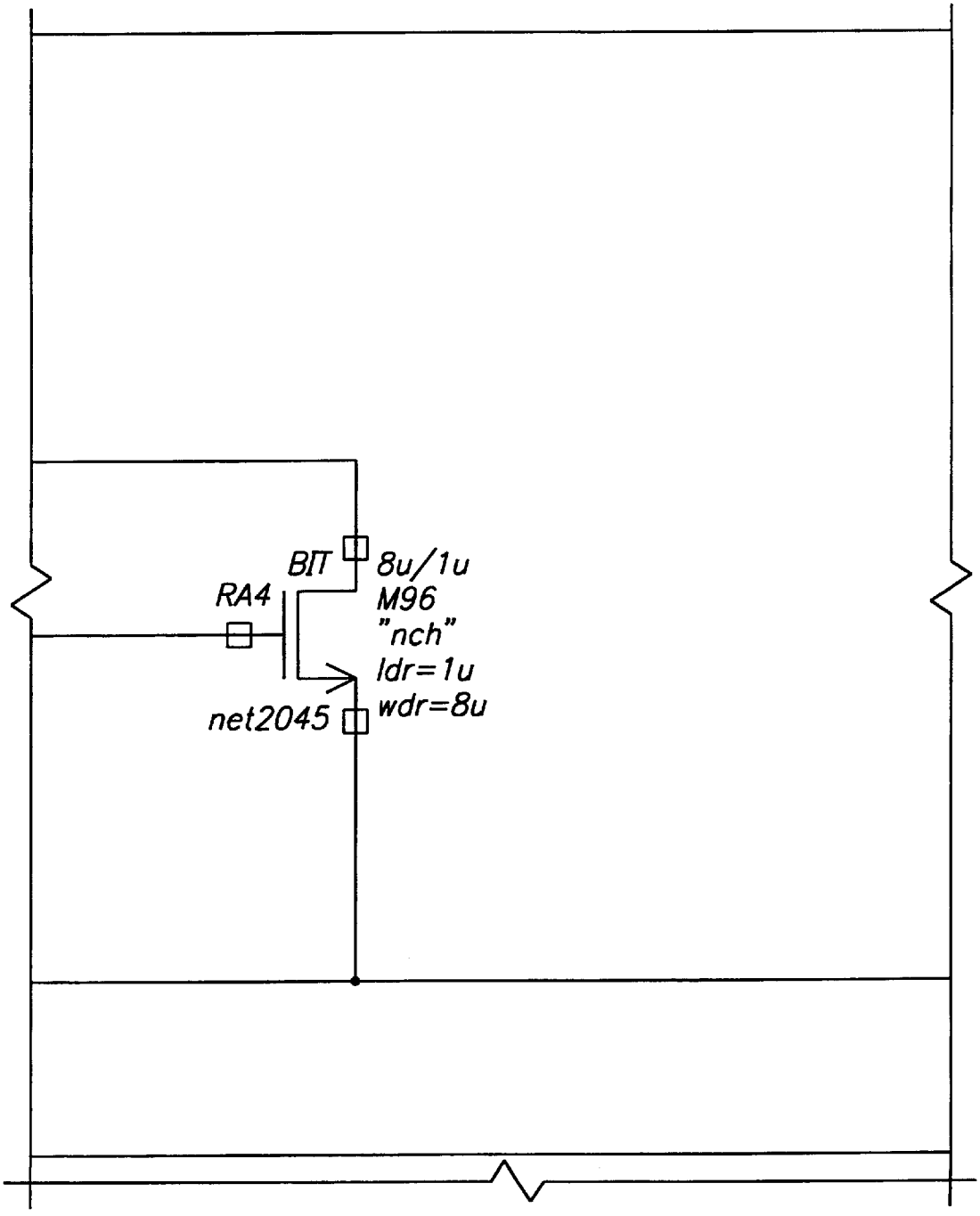


Fig 1.0406AI

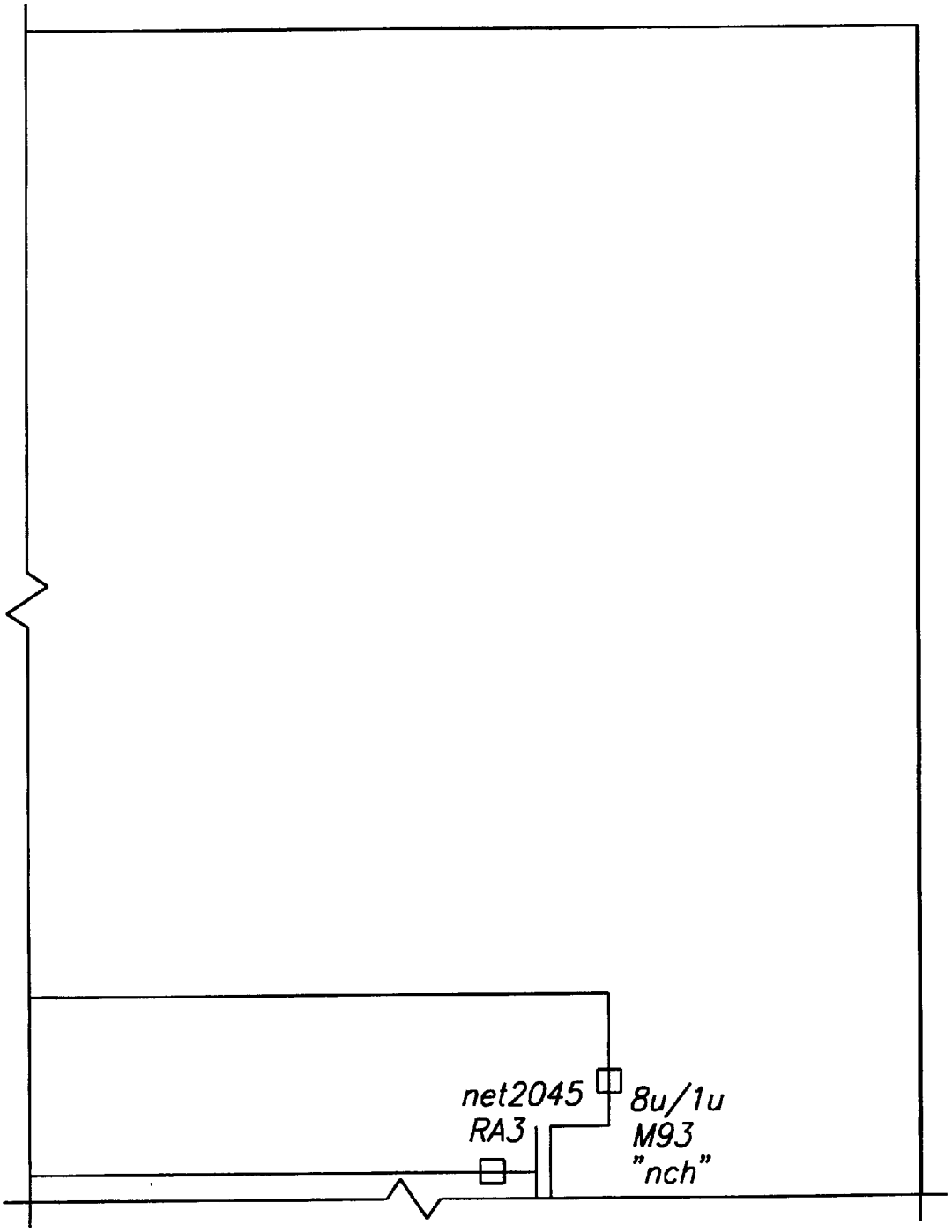


Fig 1.0410Aal

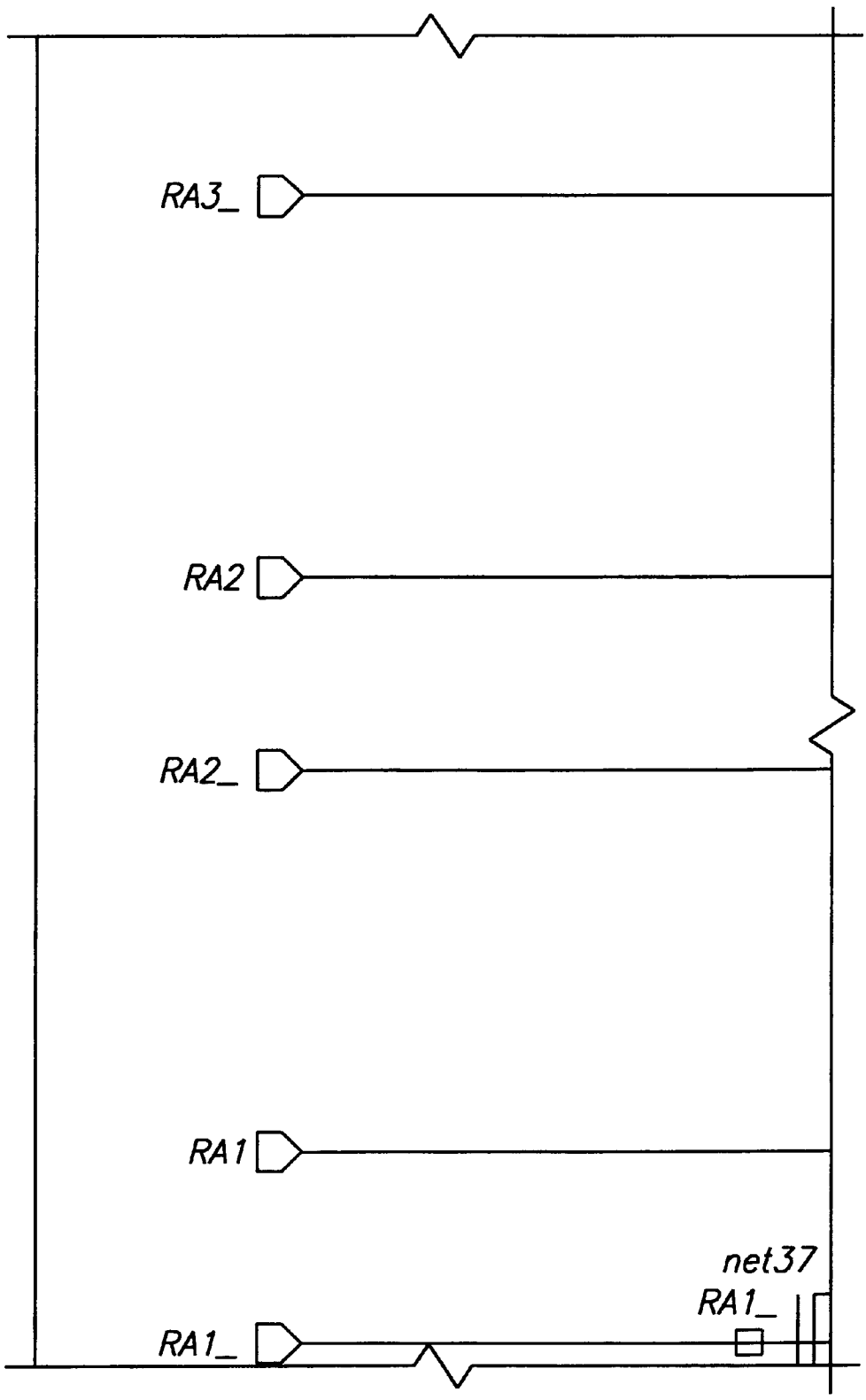


Fig 1.04068A

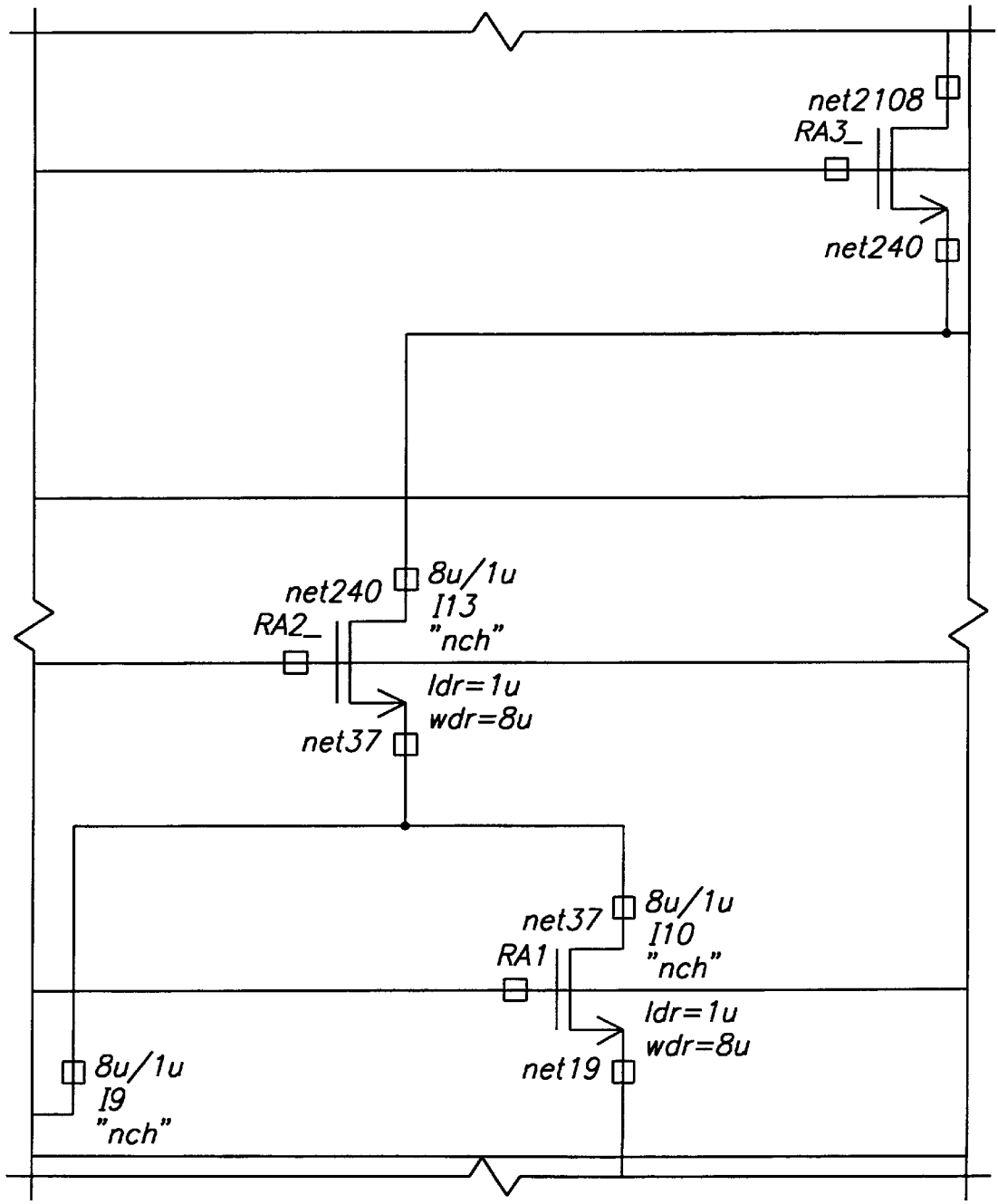

net2108
RA3_
net240
net240
RA2_
8u/1u
I13
"nch"
ldr=1u
wdr=8u
net37
net37
RA1
8u/1u
I10
"nch"
ldr=1u
wdr=8u
net19
8u/1u
I9
"nch"

Fig 1,041,068

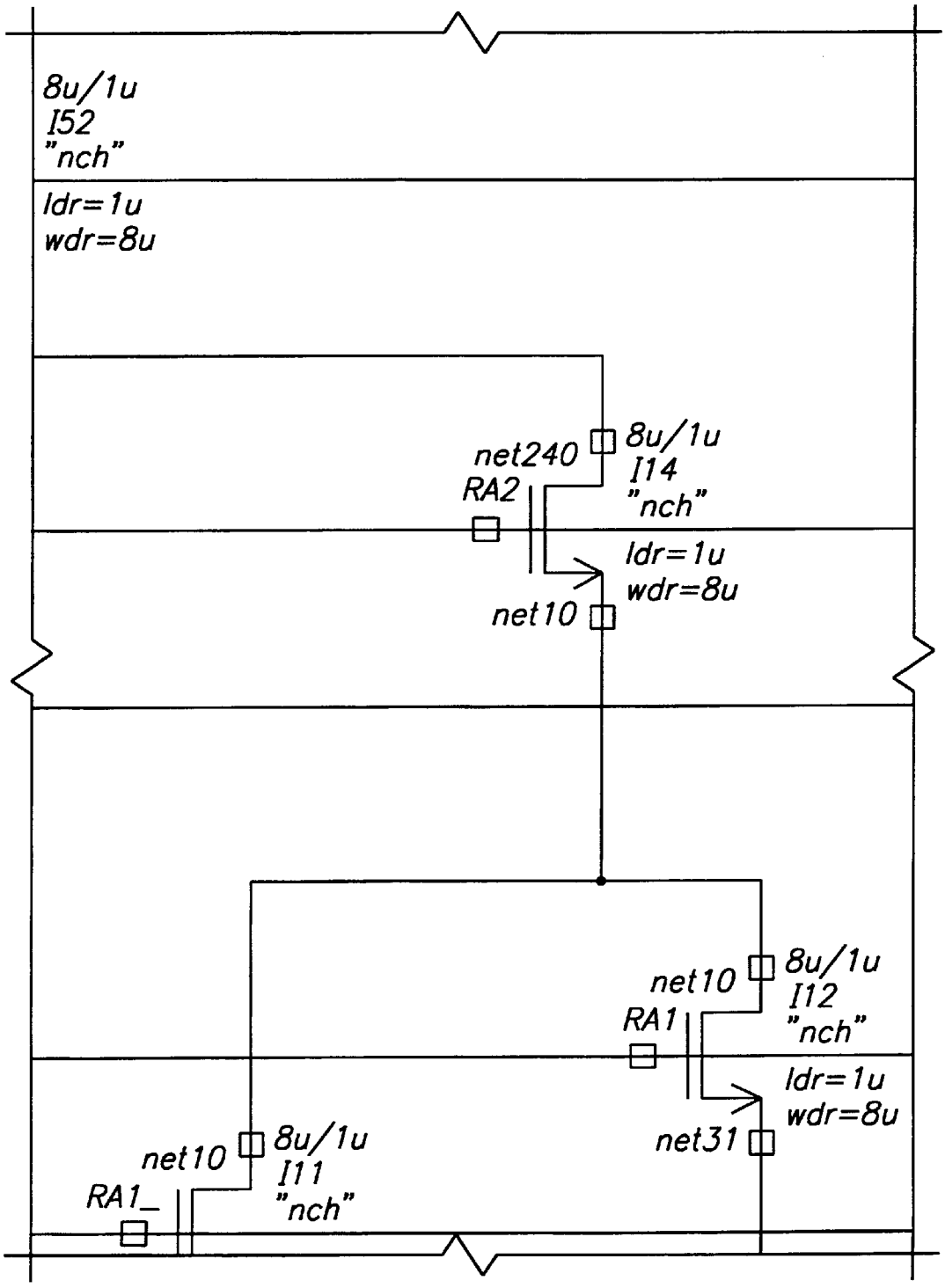

8u/1u
I52
"nch"
ldr=1u
wdr=8u
net240
RA2
8u/1u
I14
"nch"
ldr=1u
wdr=8u
net10
net10
8u/1u
I12
"nch"
RA1
ldr=1u
wdr=8u
net31
net10
8u/1u
I11
"nch"
RA1_

Fig 1,004,068

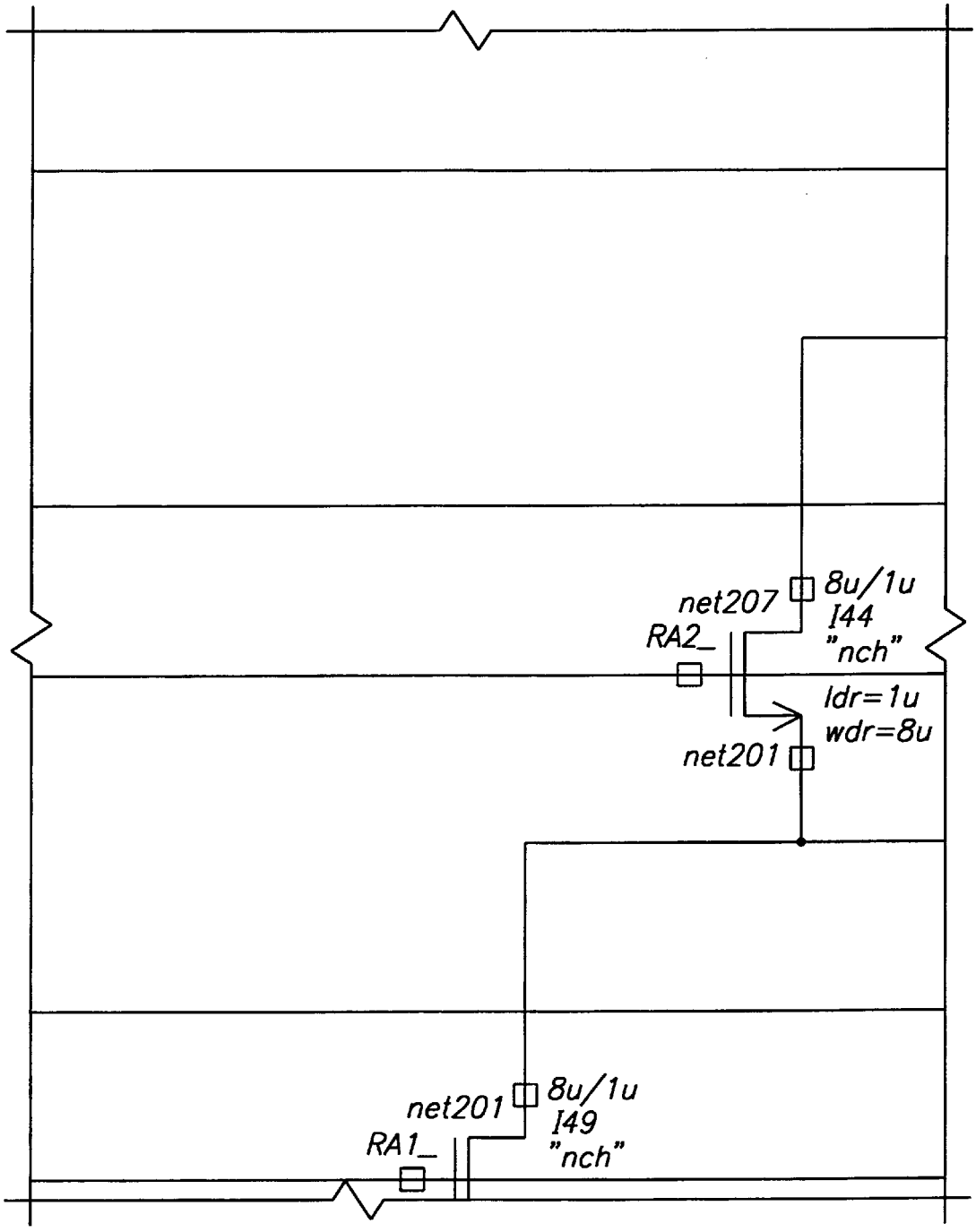

net207
8u/1u
I44
"nch"
RA2_
ldr=1u
wdr=8u
net201
net201
8u/1u
I49
"nch"
RA1_

Fig 1,043,610

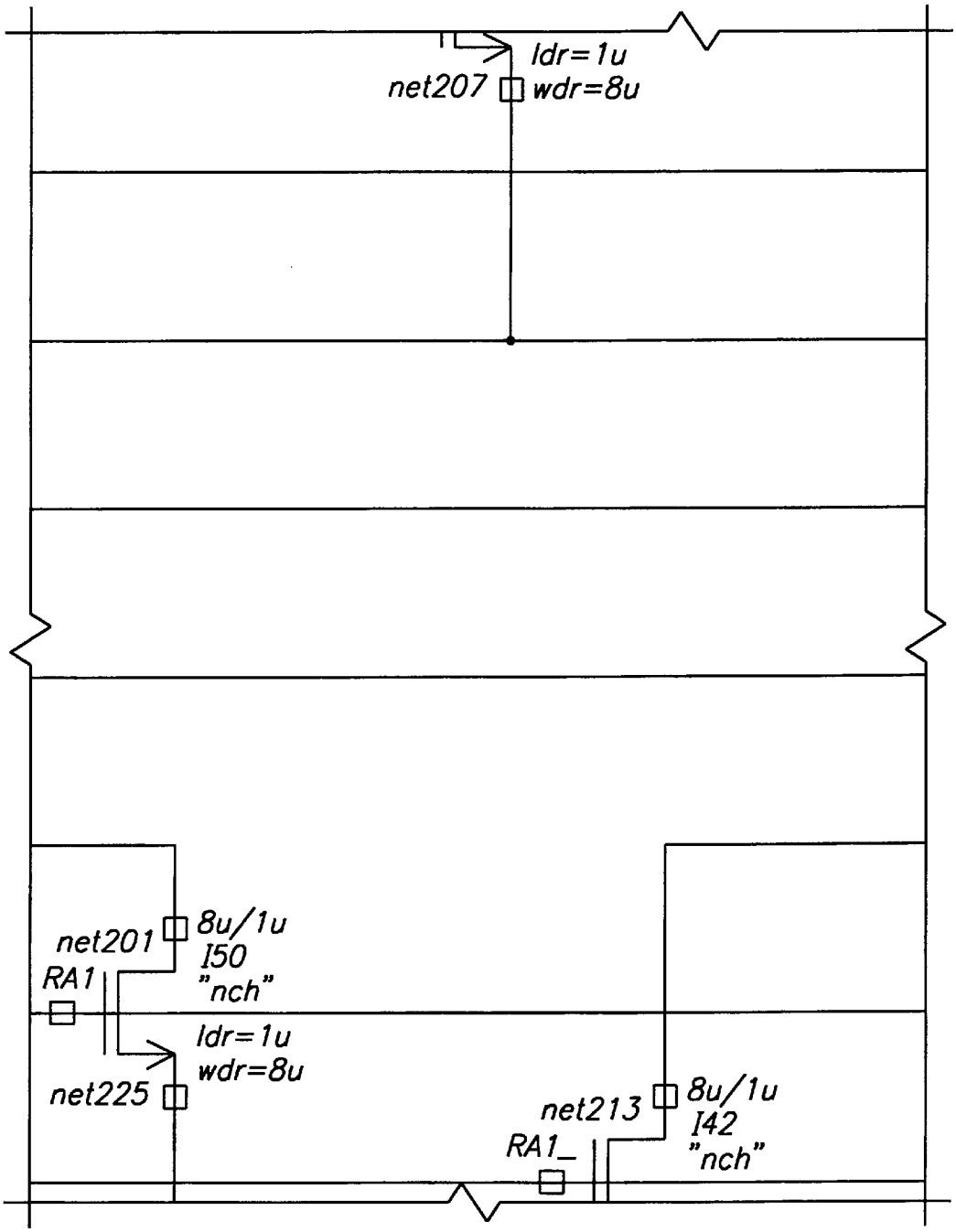


Fig 1,041,066E

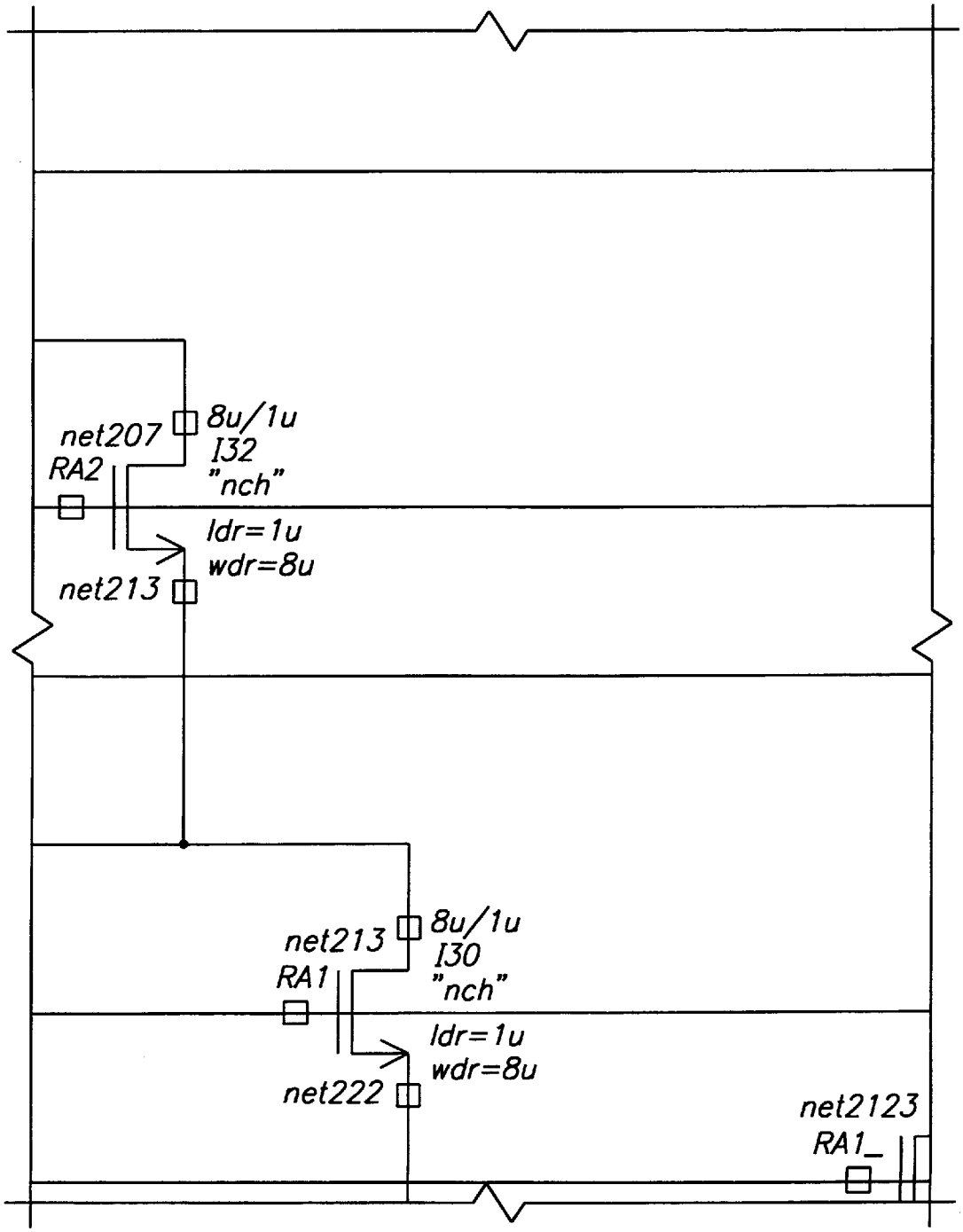


Fig 7.0041068F

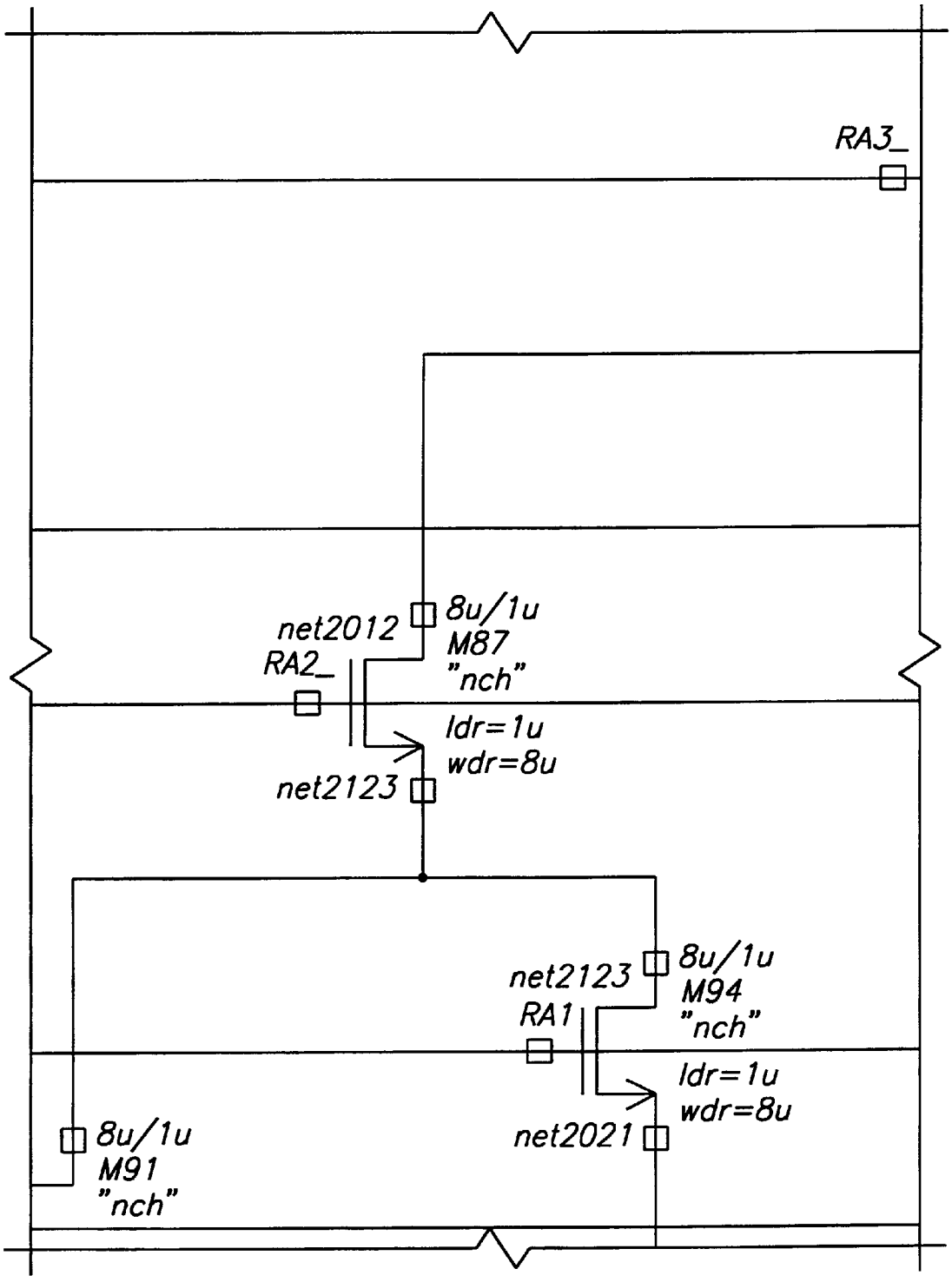

RA3_
net2012
RA2_
8u/1u
M87
"nch"
ldr=1u
wdr=8u
net2123
net2123
RA1
8u/1u
M94
"nch"
ldr=1u
wdr=8u
net2021
8u/1u
M91
"nch"

Fig 1,041,086

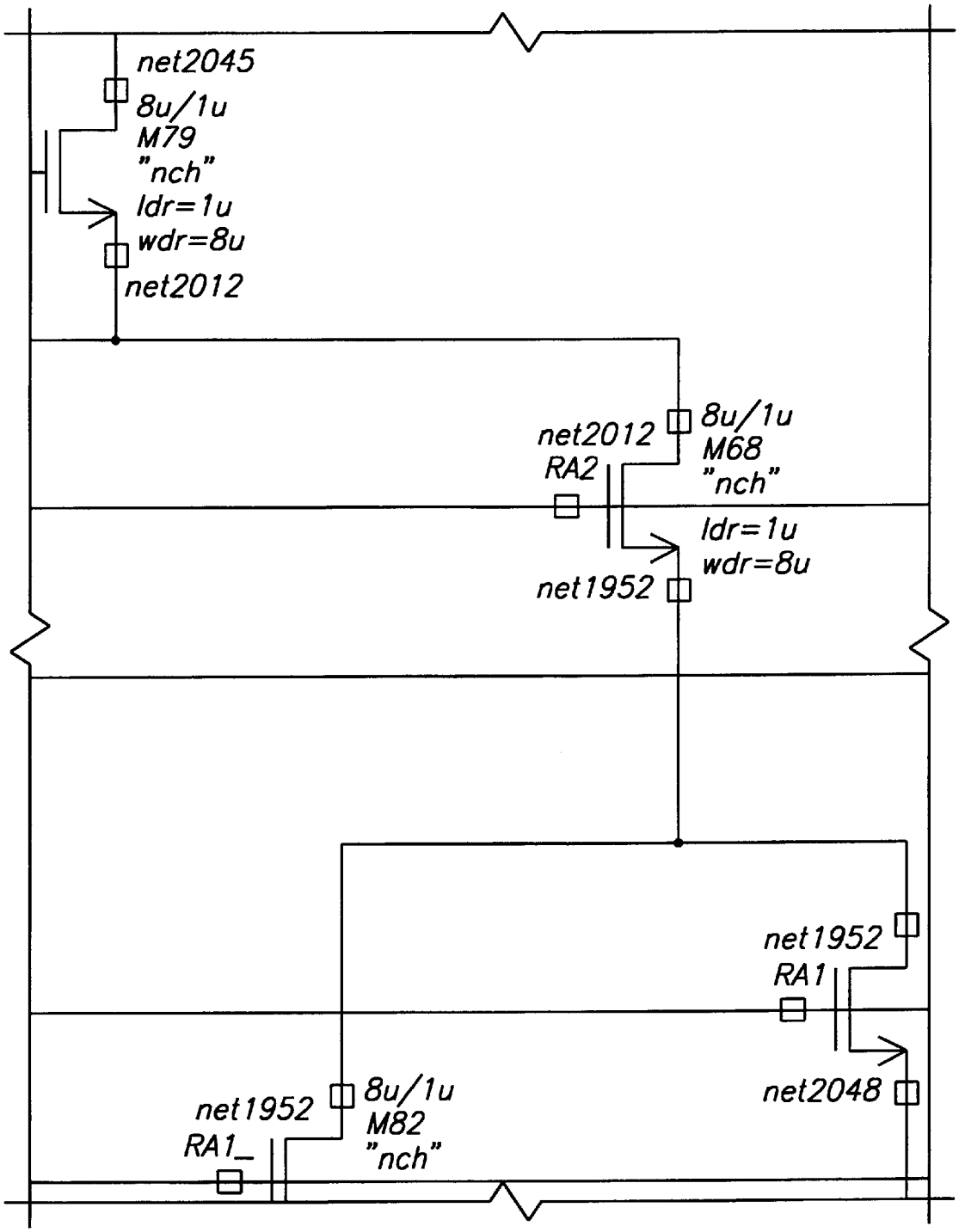

net2045
8u/1u
M79
"nch"
ldr=1u
wdr=8u
net2012
net2012
RA2
8u/1u
M68
"nch"
ldr=1u
wdr=8u
net1952
net1952
RA1
net2048
net1952
RA1_
8u/1u
M82
"nch"

Fig 1,044,038

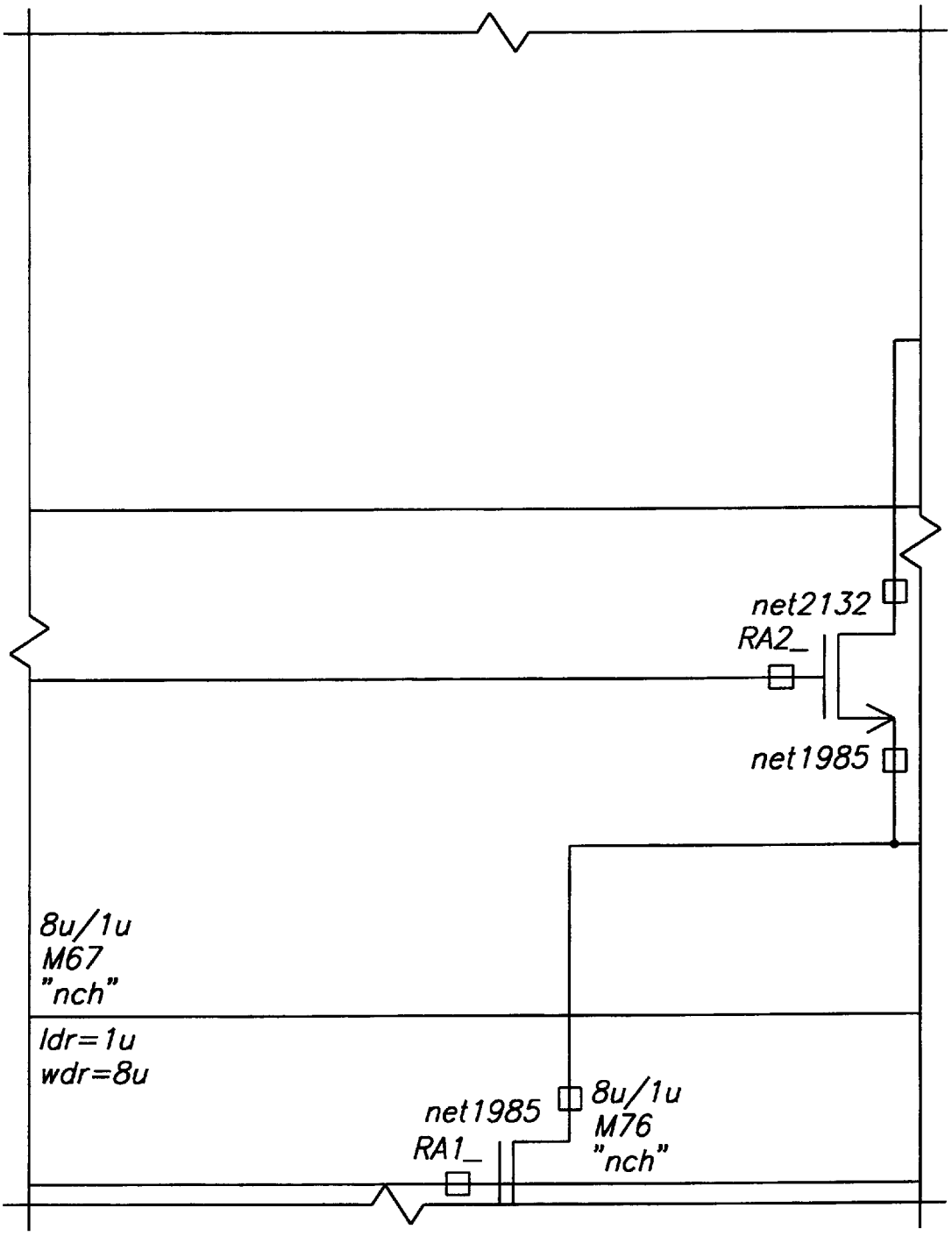

net2132
RA2_
net1985
8u/1u
M67
"nch"
ldr=1u
wdr=8u
net1985
RA1_
8u/1u
M76
"nch"

Fig 1,041,681

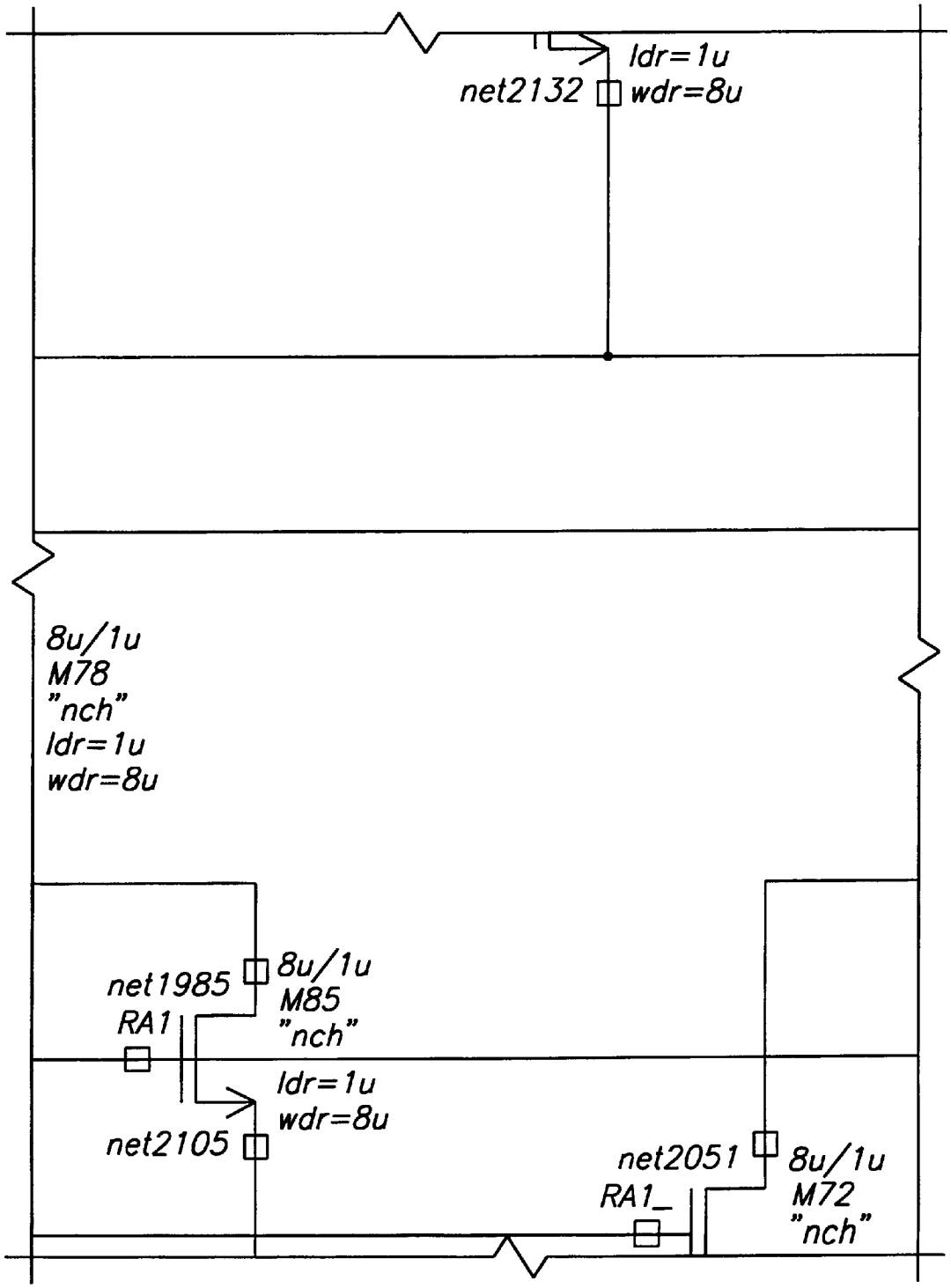

ldr=1u
net2132
wdr=8u
8u/1u
M78
"nch"
ldr=1u
wdr=8u
net1985
RA1
8u/1u
M85
"nch"
ldr=1u
wdr=8u
net2105
net2051
RA1_
8u/1u
M72
"nch"

Fig 1,041,061

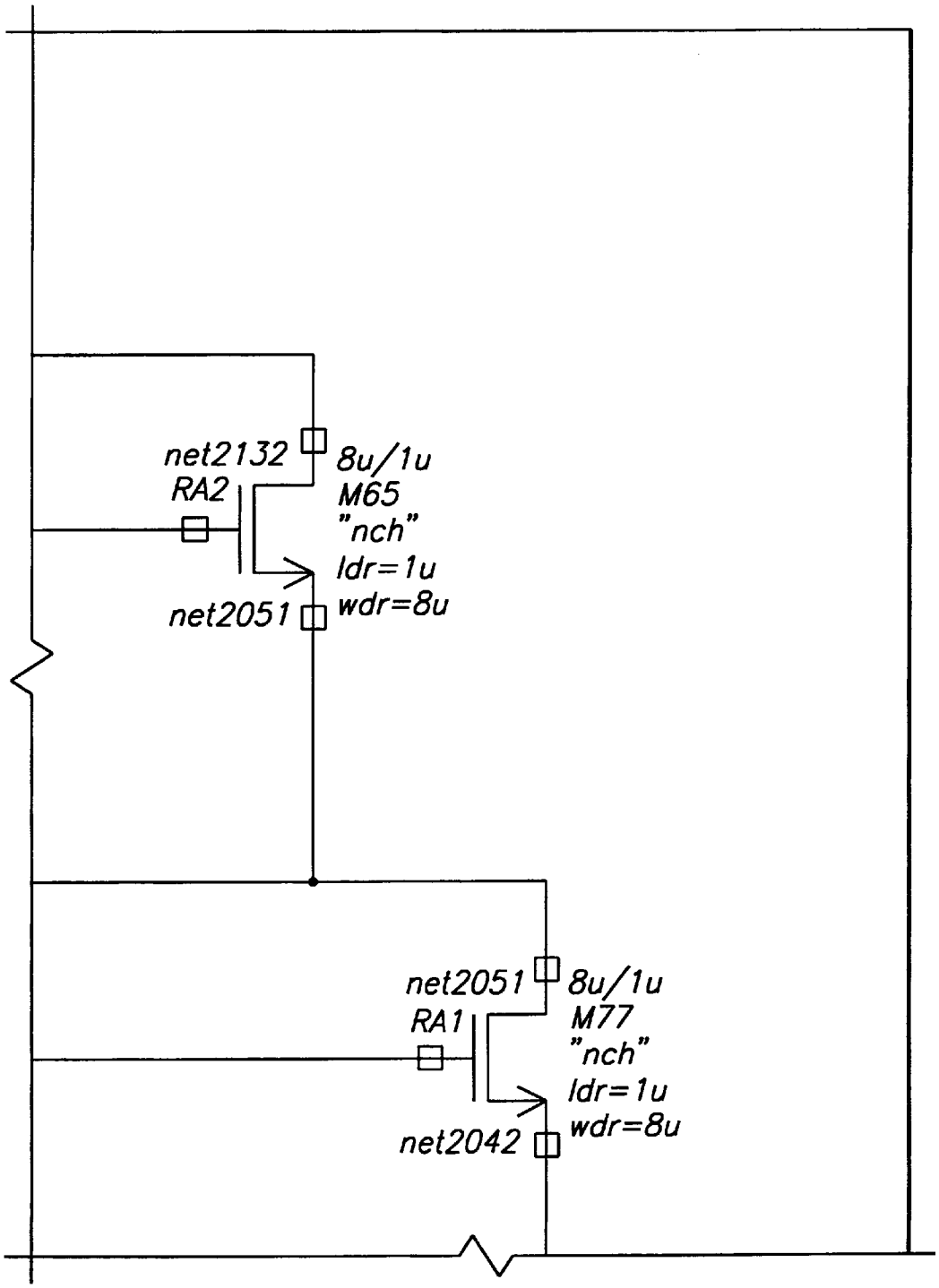

net2132
RA2
8u/1u
M65
"nch"
ldr=1u
wdr=8u
net2051
net2051
RA1
8u/1u
M77
"nch"
ldr=1u
wdr=8u
net2042

Fig 1,041,068

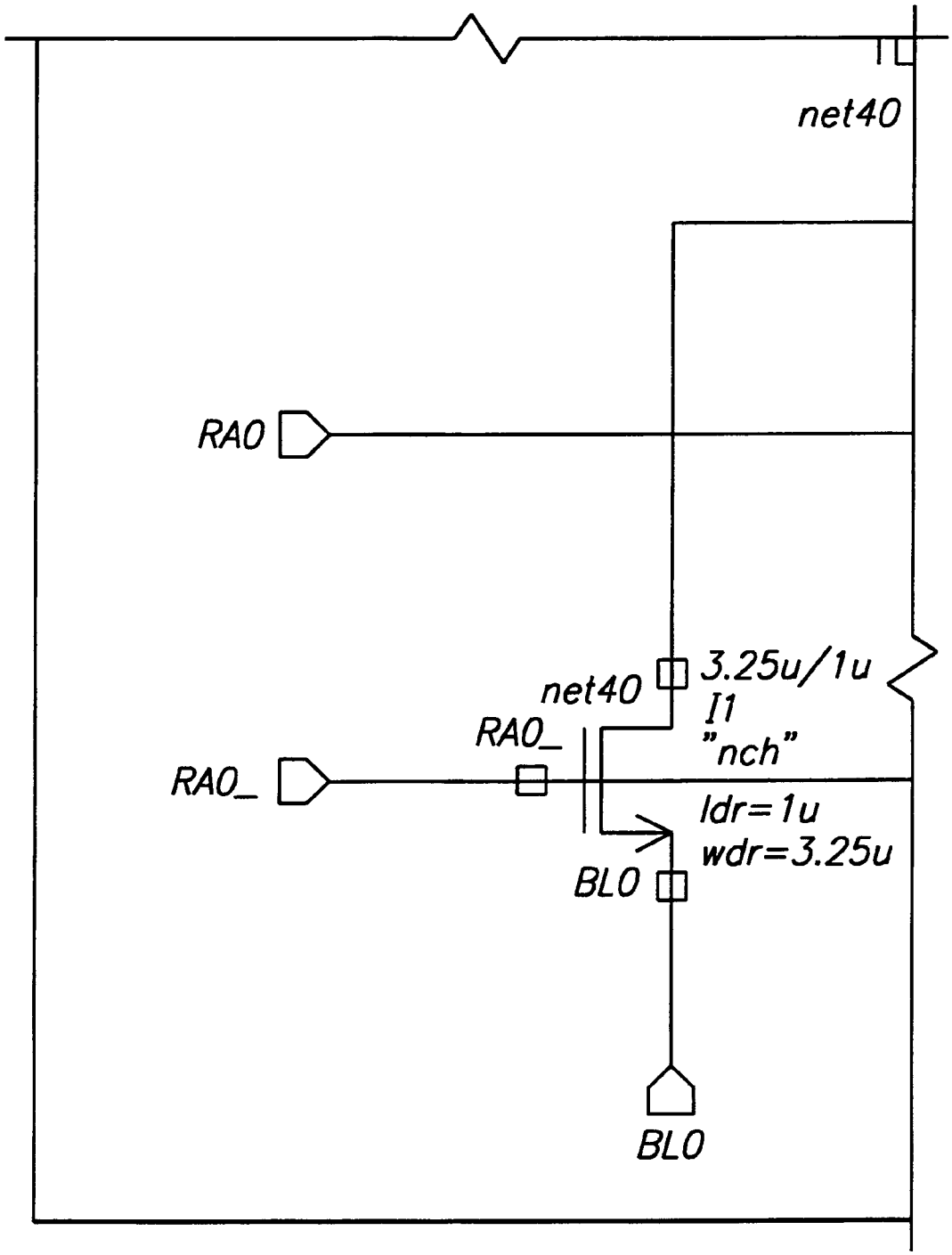


Fig 1,094,056A

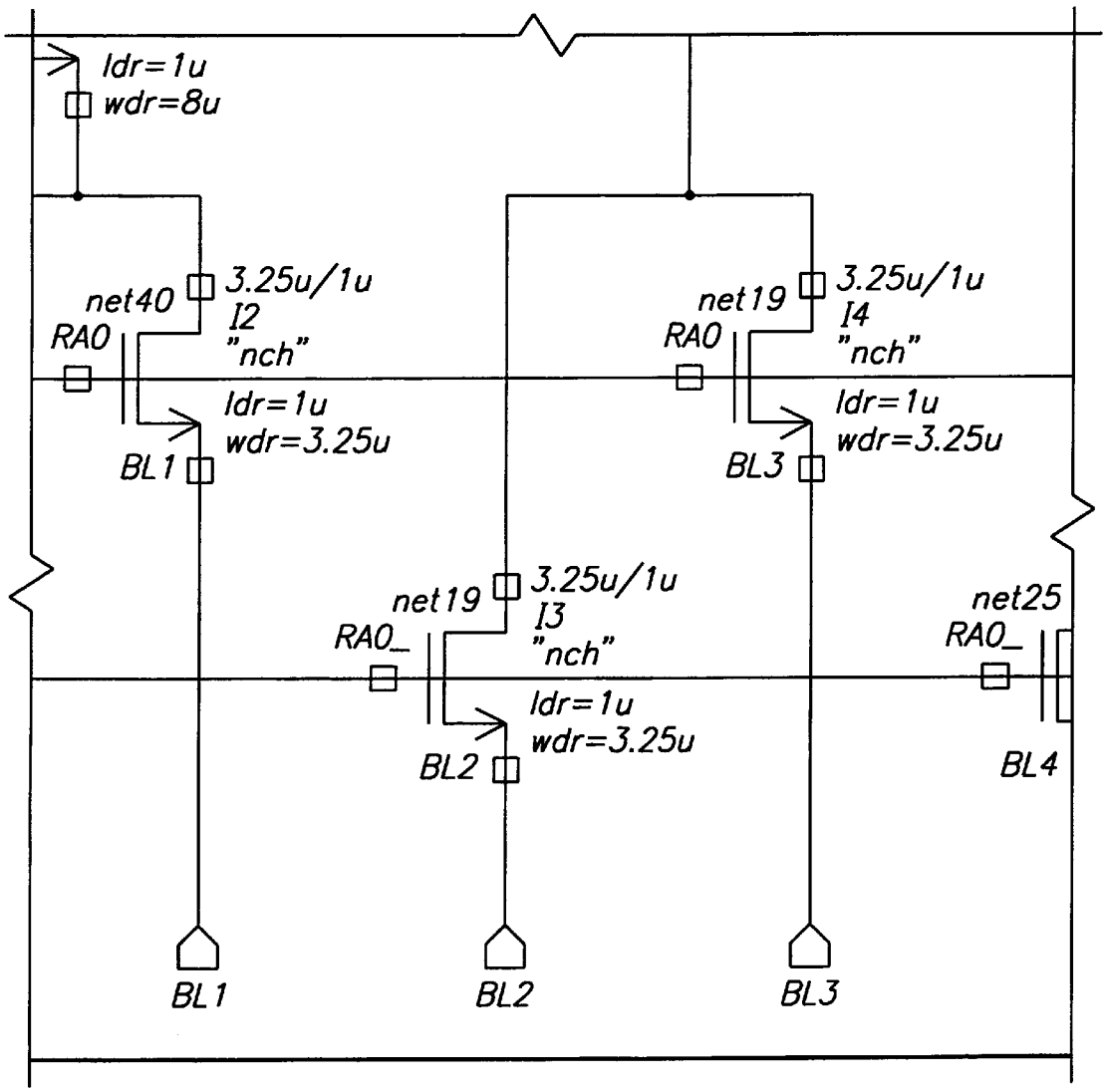

ldr=1u
wdr=8u
net40
RA0
3.25u/1u
I2
"nch"
ldr=1u
wdr=3.25u
BL1
net19
RA0
3.25u/1u
I4
"nch"
ldr=1u
wdr=3.25u
BL3
net19
RA0_
3.25u/1u
I3
"nch"
ldr=1u
wdr=3.25u
BL2
net25
RA0_
BL4
BL1
BL2
BL3

Fig 1,041,068

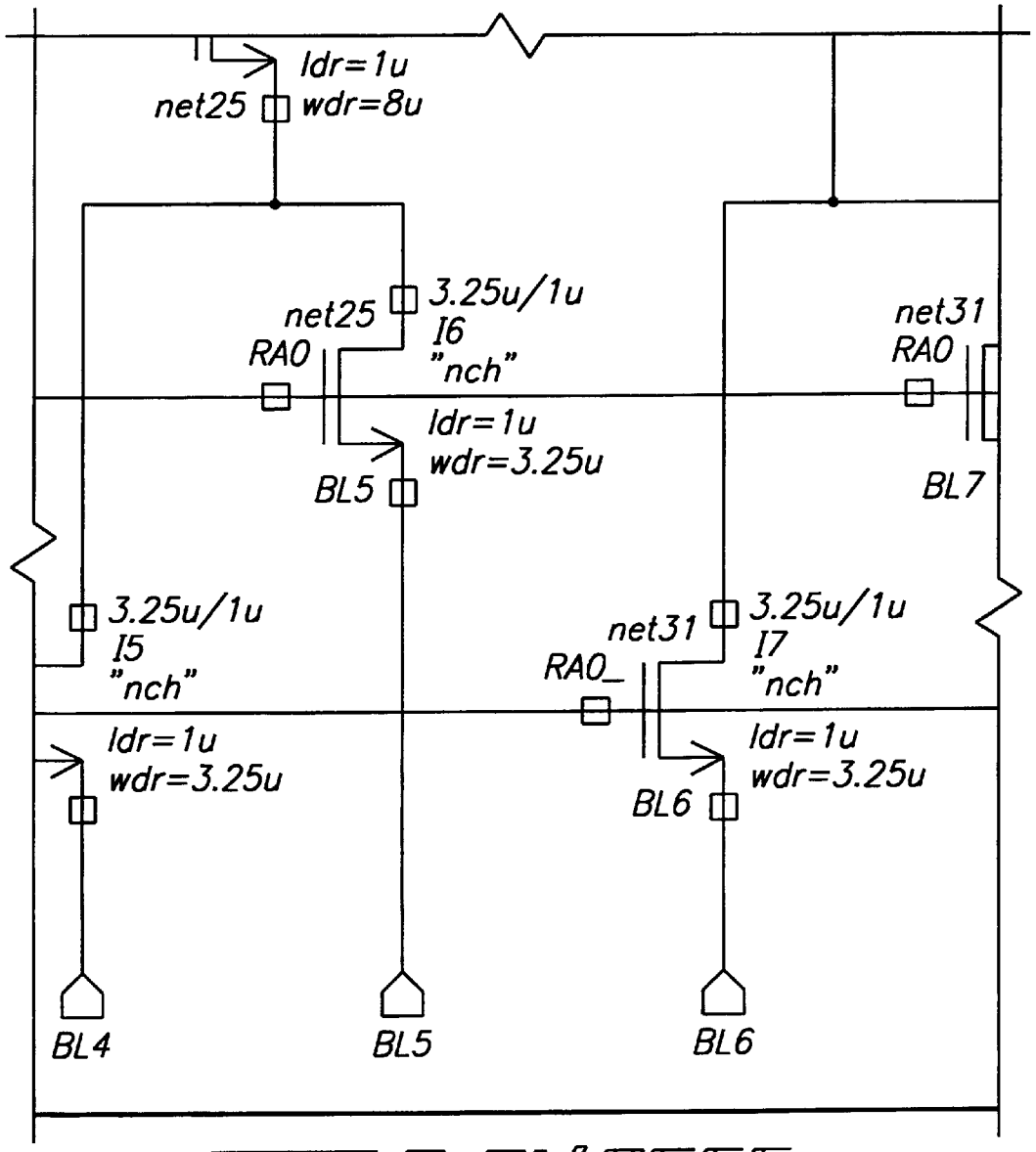

ldr=1u
net25
wdr=8u
net25
3.25u/1u
I6
"nch"
RA0
net31
RA0
ldr=1u
wdr=3.25u
BL5
BL7
3.25u/1u
I5
"nch"
net31
3.25u/1u
I7
"nch"
RA0_
ldr=1u
wdr=3.25u
ldr=1u
wdr=3.25u
BL6
BL4
BL5
BL6

Fig 1.0406CC

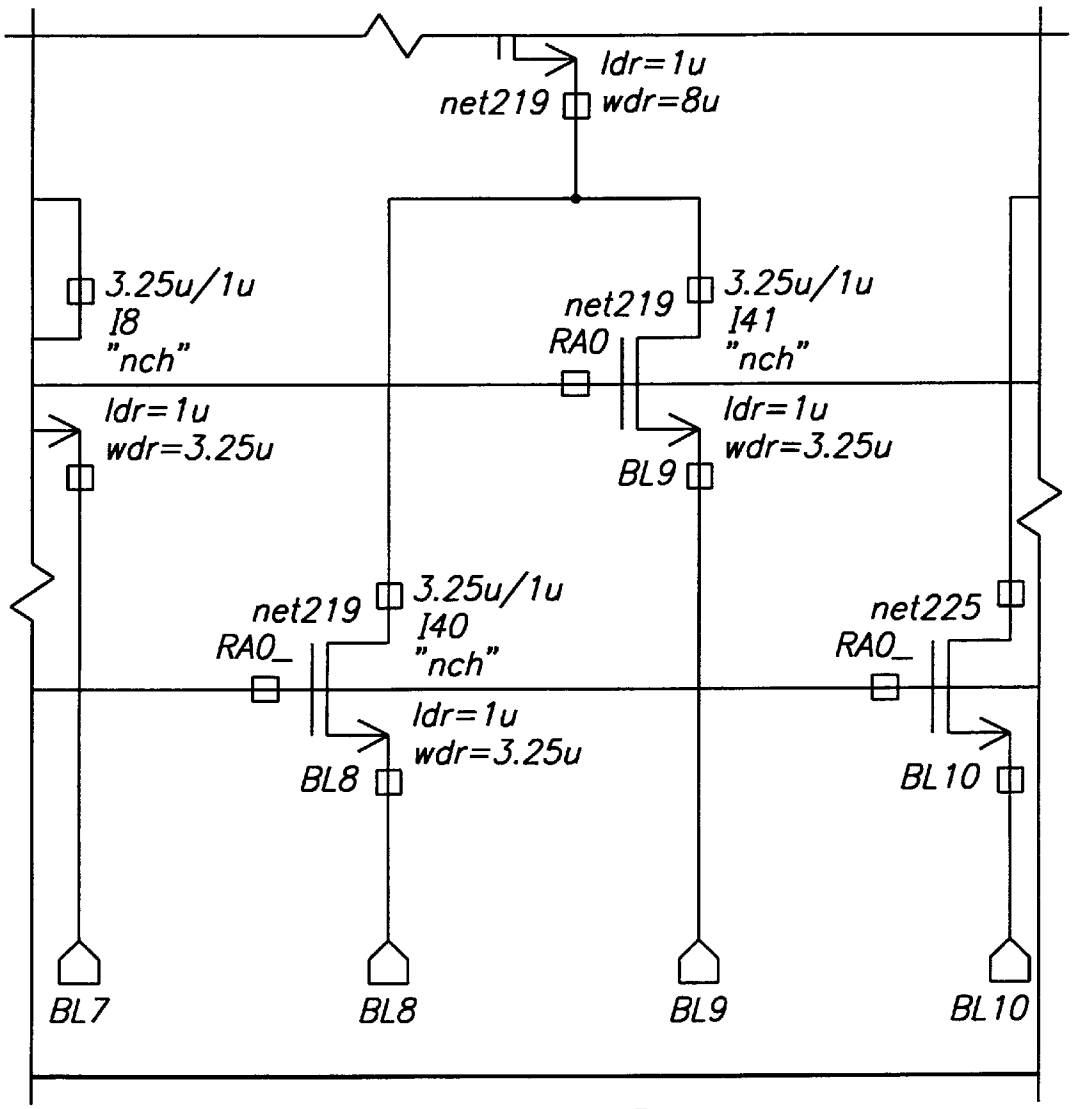

ldr=1u
net219
wdr=8u
3.25u/1u
I8
"nch"
net219
RA0
3.25u/1u
I41
"nch"
ldr=1u
wdr=3.25u
ldr=1u
wdr=3.25u
BL9
net219
RA0_
3.25u/1u
I40
"nch"
net225
RA0_
ldr=1u
wdr=3.25u
BL8
BL10
BL7
BL8
BL9
BL10

Fig 1.0406CD

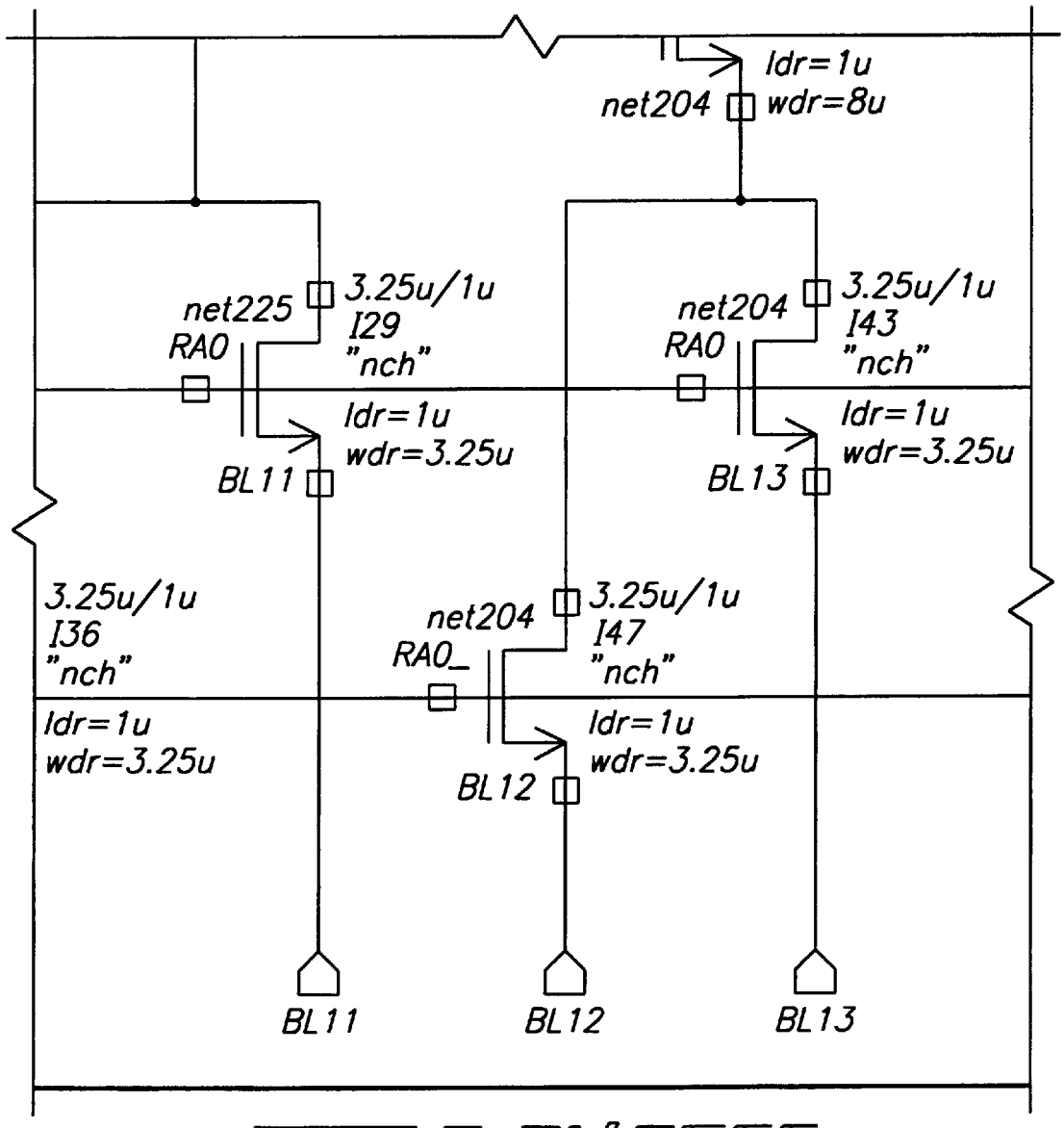

ldr=1u
net204
wdr=8u
net225
RA0
3.25u/1u
I29
"nch"
net204
RA0
3.25u/1u
I43
"nch"
ldr=1u
wdr=3.25u
BL11
ldr=1u
wdr=3.25u
BL13
3.25u/1u
I36
"nch"
net204
RA0_
3.25u/1u
I47
"nch"
ldr=1u
wdr=3.25u
ldr=1u
wdr=3.25u
BL12
BL11
BL12
BL13

Fig 10464CE

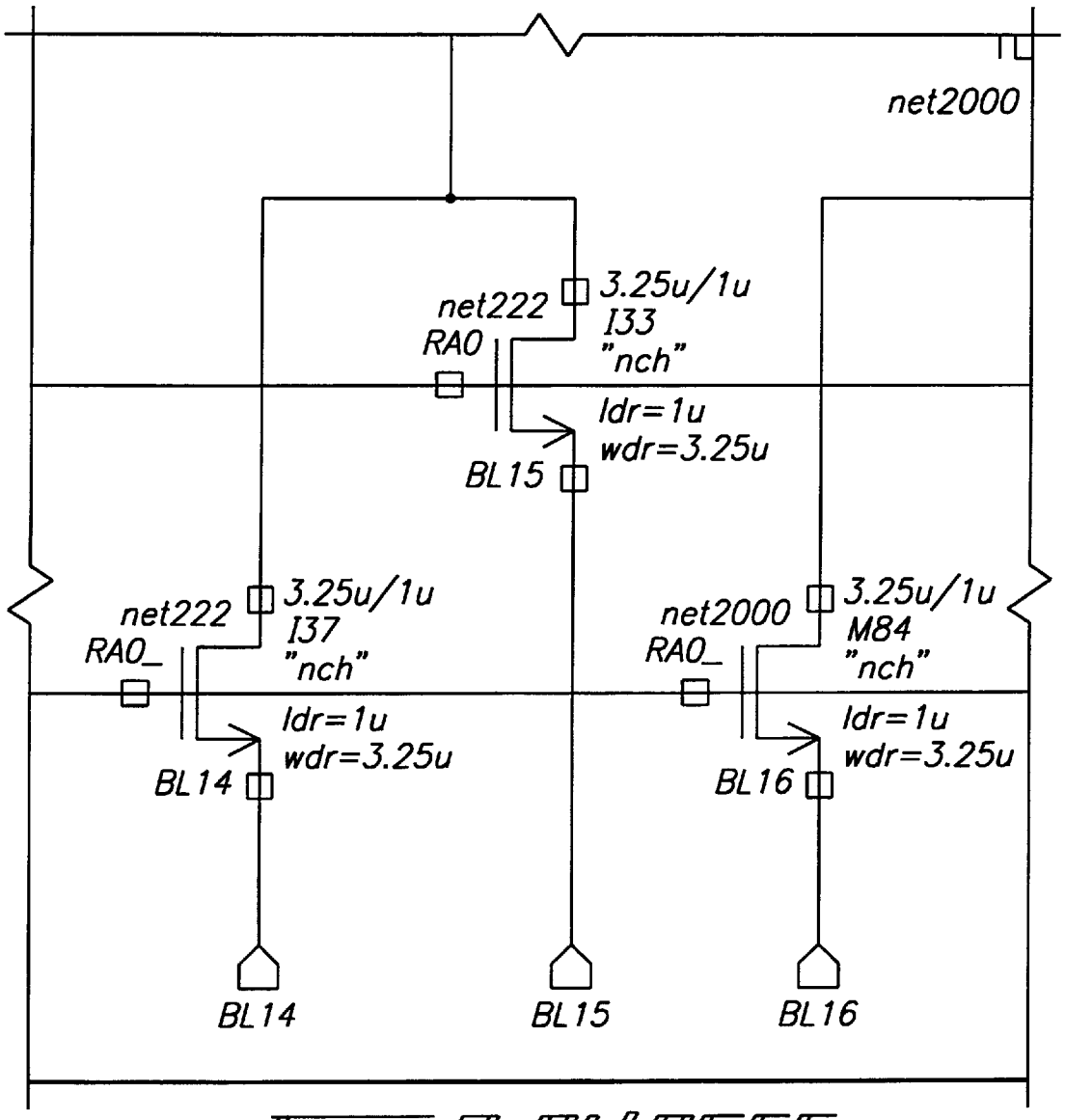

net2000
net222
RA0
3.25u/1u
I33
"nch"
ldr=1u
wdr=3.25u
BL15
net222
RA0_
3.25u/1u
I37
"nch"
ldr=1u
wdr=3.25u
BL14
net2000
RA0_
3.25u/1u
M84
"nch"
ldr=1u
wdr=3.25u
BL16
BL14
BL15
BL16

Fig 1.0+1065F

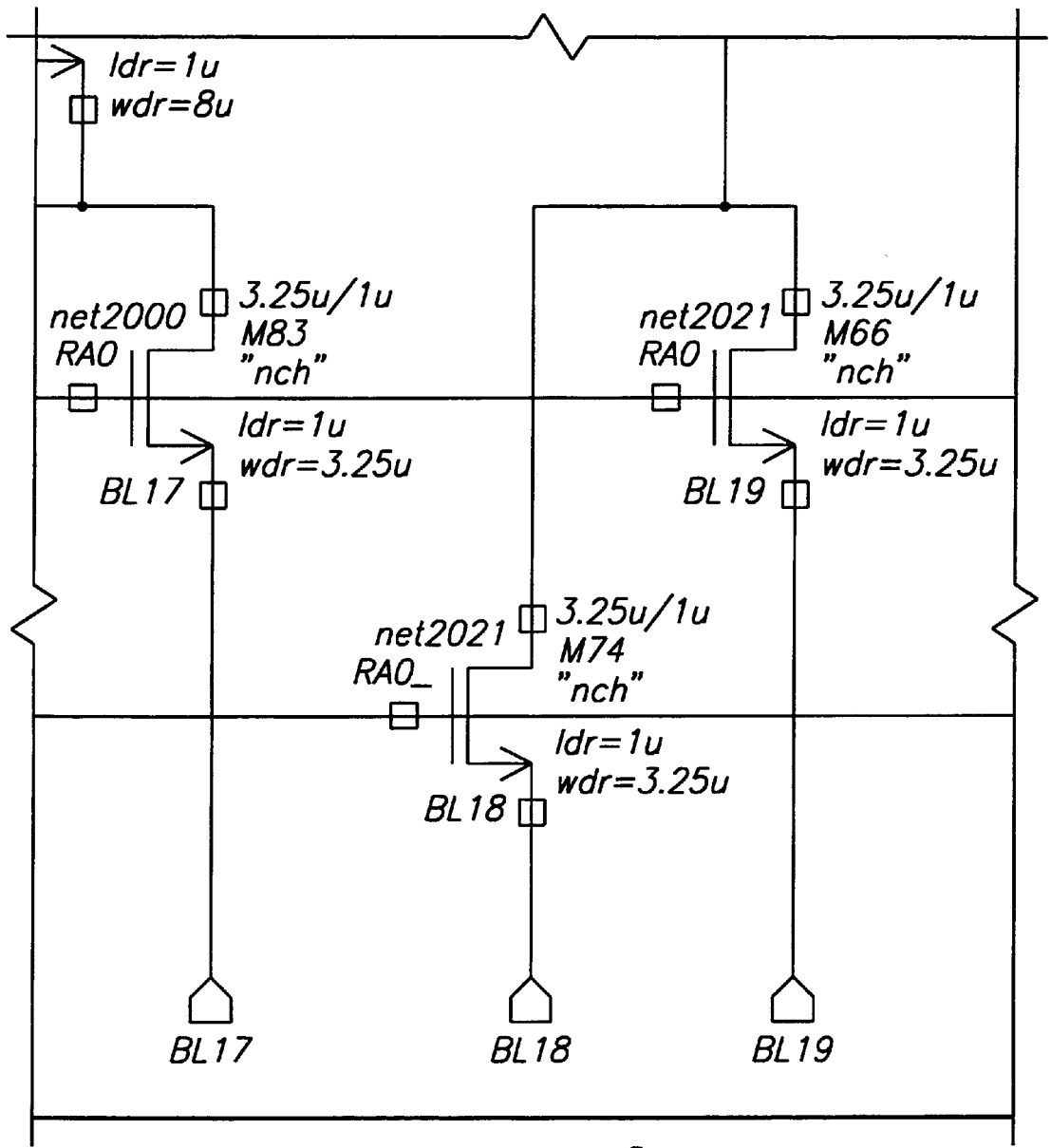

ldr=1u
wdr=8u
net2000
RA0
3.25u/1u
M83
"nch"
ldr=1u
wdr=3.25u
BL17
net2021
RA0
3.25u/1u
M66
"nch"
ldr=1u
wdr=3.25u
BL19
net2021
RA0_
3.25u/1u
M74
"nch"
ldr=1u
wdr=3.25u
BL18
BL17
BL18
BL19

Fig 1,094,066

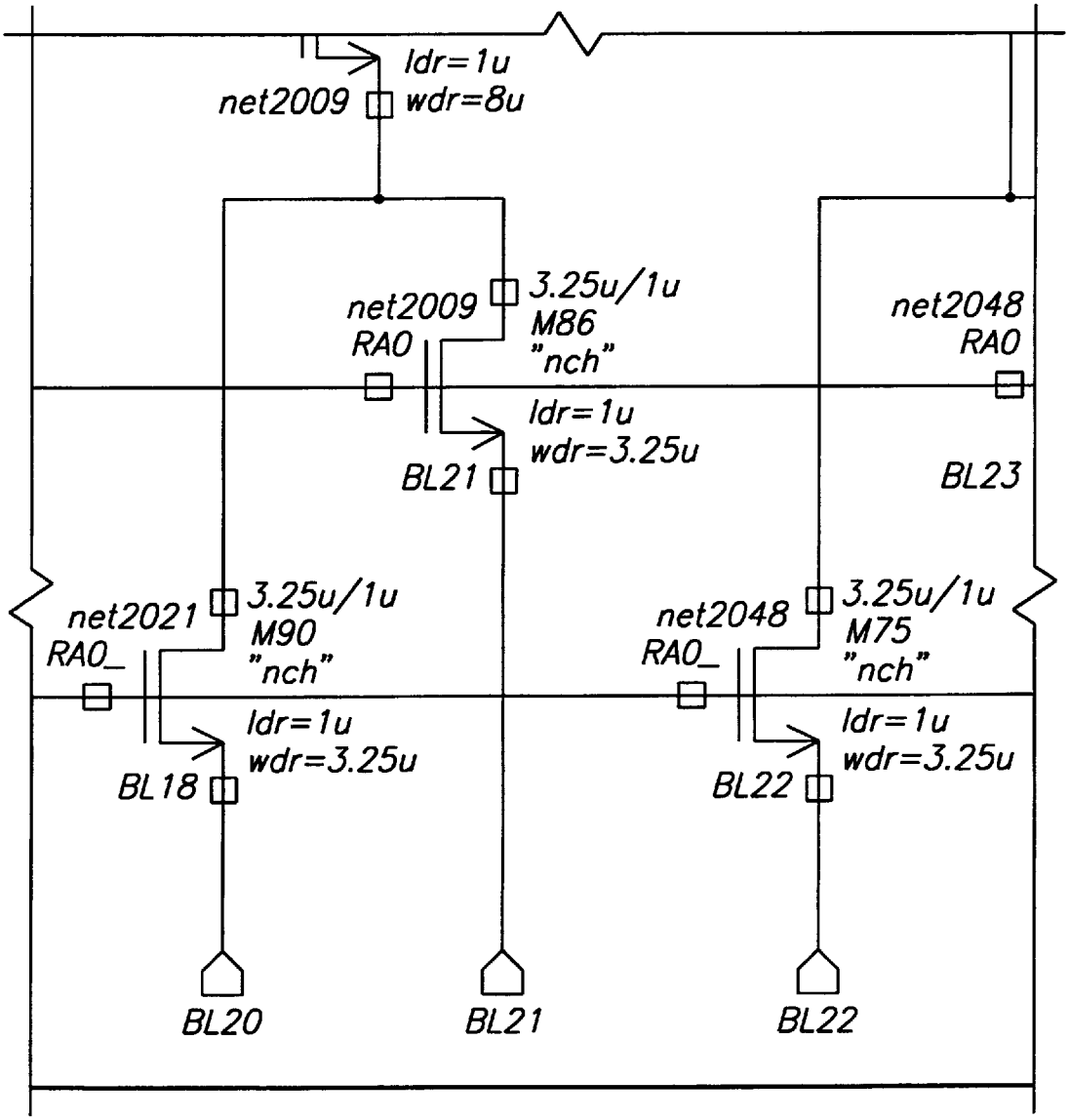


Fig 1,041,061H

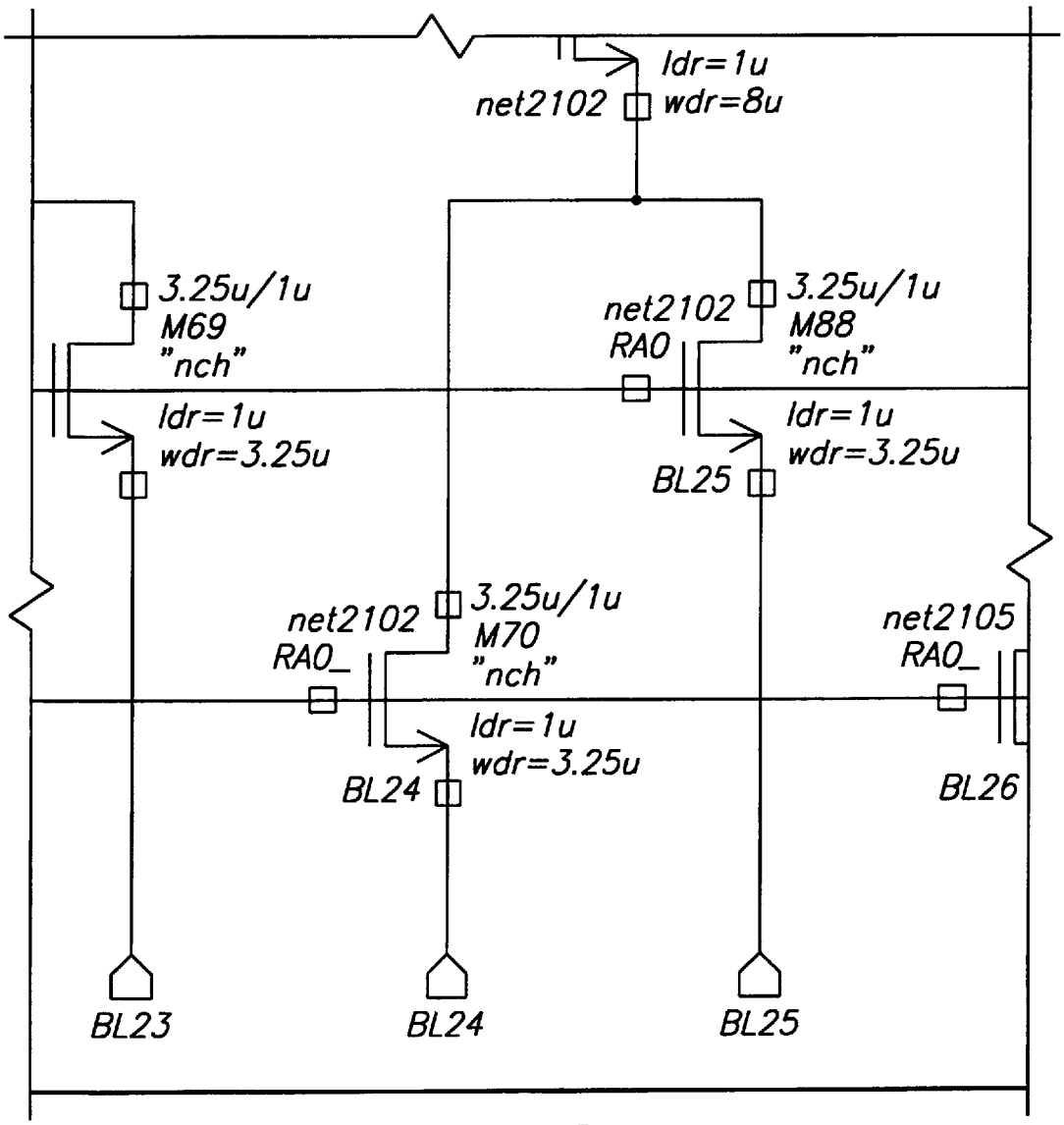

ldr=1u
net2102
wdr=8u
3.25u/1u
M69
"nch"
ldr=1u
wdr=3.25u
net2102
RA0
3.25u/1u
M88
"nch"
ldr=1u
wdr=3.25u
BL25
net2102
RA0_
3.25u/1u
M70
"nch"
ldr=1u
wdr=3.25u
BL24
net2105
RA0_
BL26
BL23
BL24
BL25

Fig 1,041,061

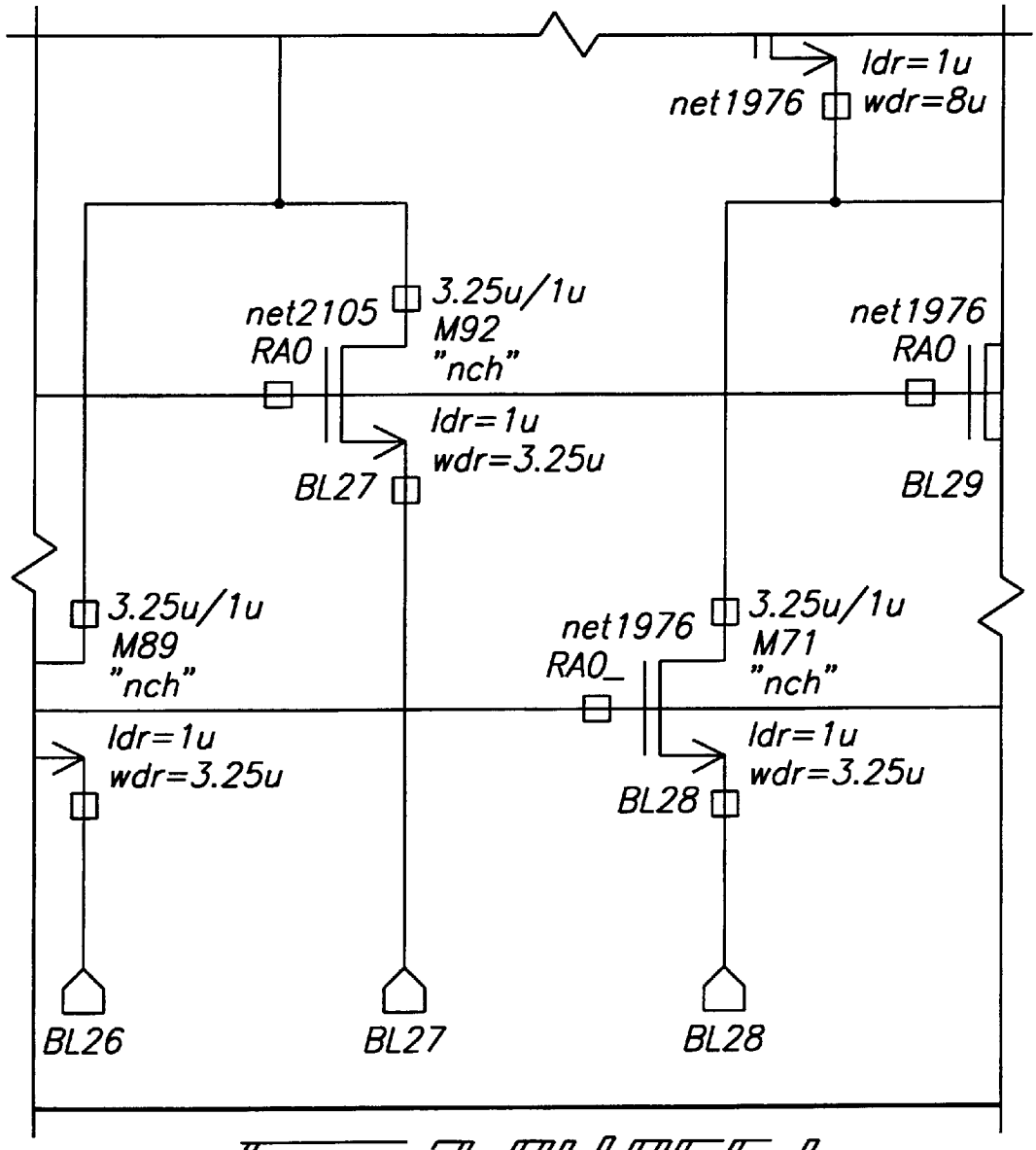

ldr=1u
net1976
wdr=8u
net2105
RA0
3.25u/1u
M92
"nch"
net1976
RA0
ldr=1u
wdr=3.25u
BL27
BL29
3.25u/1u
M89
"nch"
net1976
RA0_
3.25u/1u
M71
"nch"
ldr=1u
wdr=3.25u
ldr=1u
wdr=3.25u
BL28
BL26
BL27
BL28

Fig 1,004,060

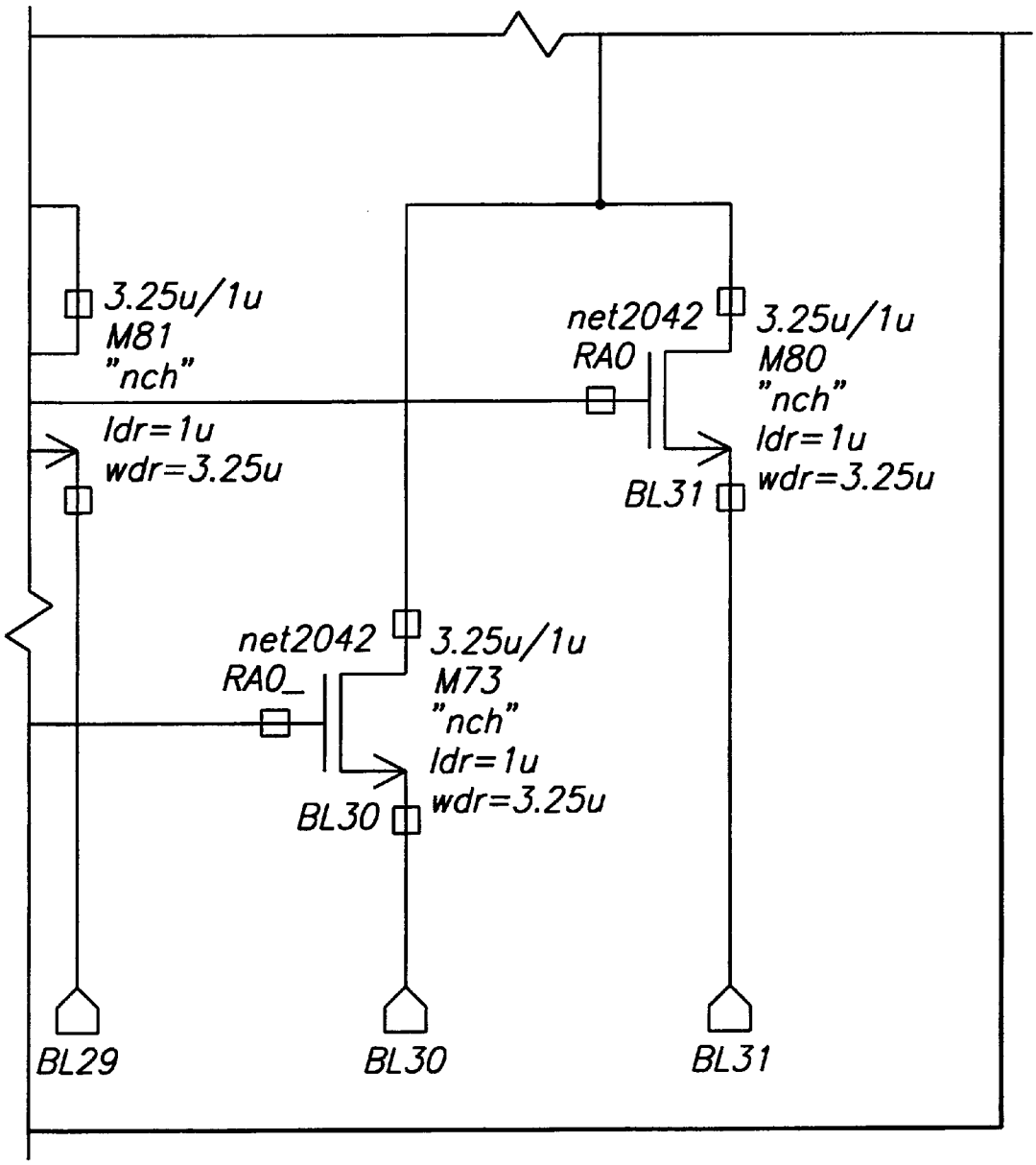
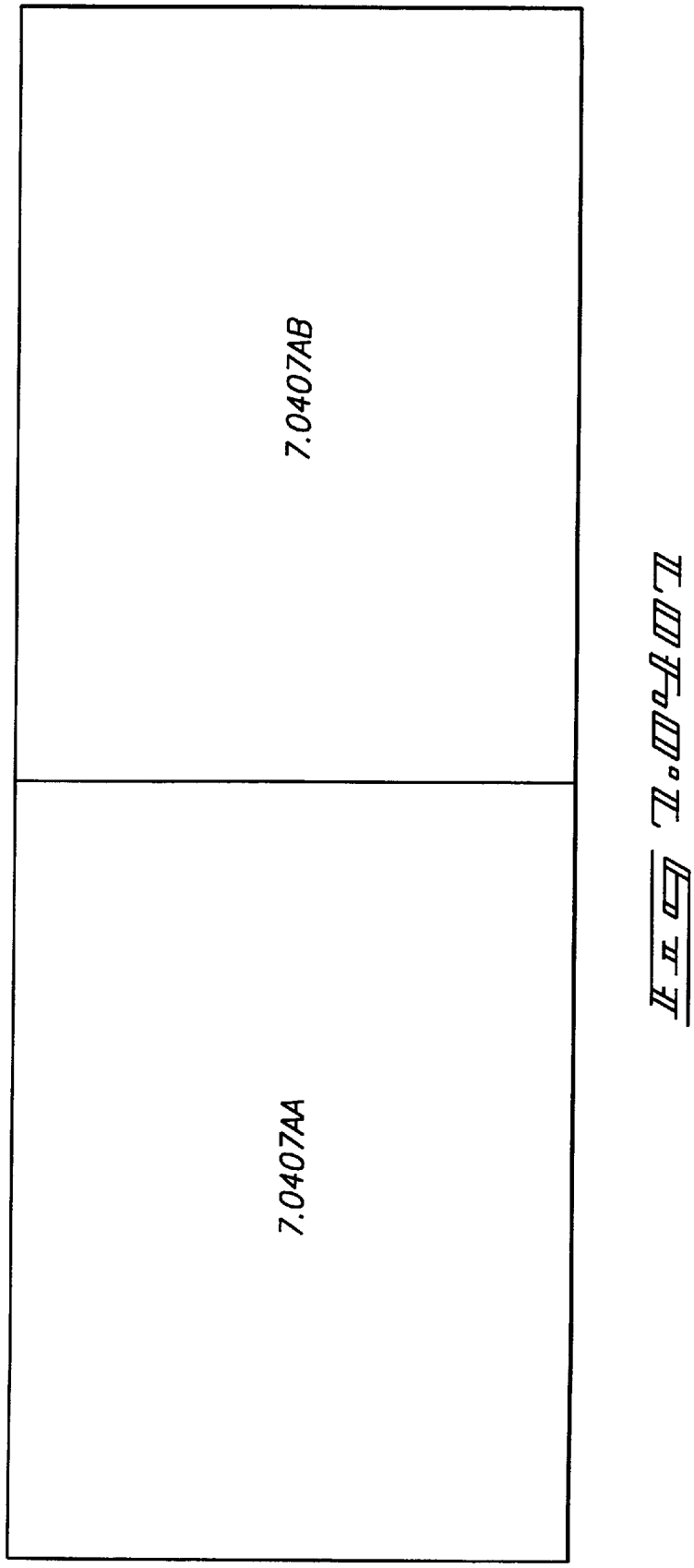

3.25u/1u
M81
"nch"
ldr=1u
wdr=3.25u
net2042
RA0
3.25u/1u
M80
"nch"
ldr=1u
wdr=3.25u
BL31
net2042
RA0_
3.25u/1u
M73
"nch"
ldr=1u
wdr=3.25u
BL30
BL29
BL30
BL31

Fig 1,044,066


7.0407AB
7.0407AA
FIG. 7.0407L

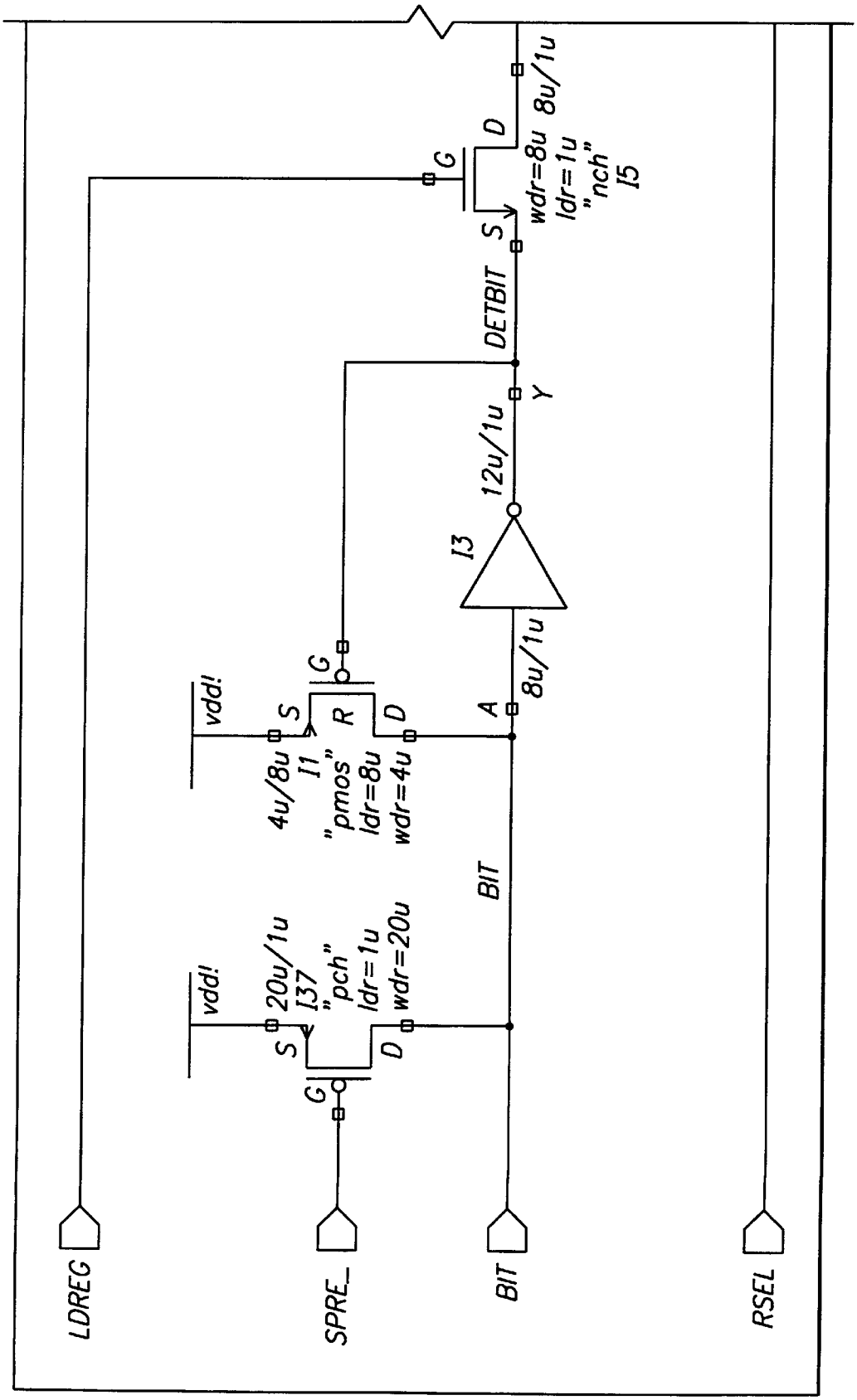

LDREG
SPRE_
BIT
RSEL
vdd!
vdd!
I37
"pch"
ldr=1u
wdr=20u
20u/1u
I1
"pmos"
ldr=8u
wdr=4u
4u/8u
I3
12u/1u
I5
"nch"
ldr=1u
wdr=8u
8u/1u
8u/1u
DETBIT
BIT
A
Y
S
D
G
R

FIG 6,130,602

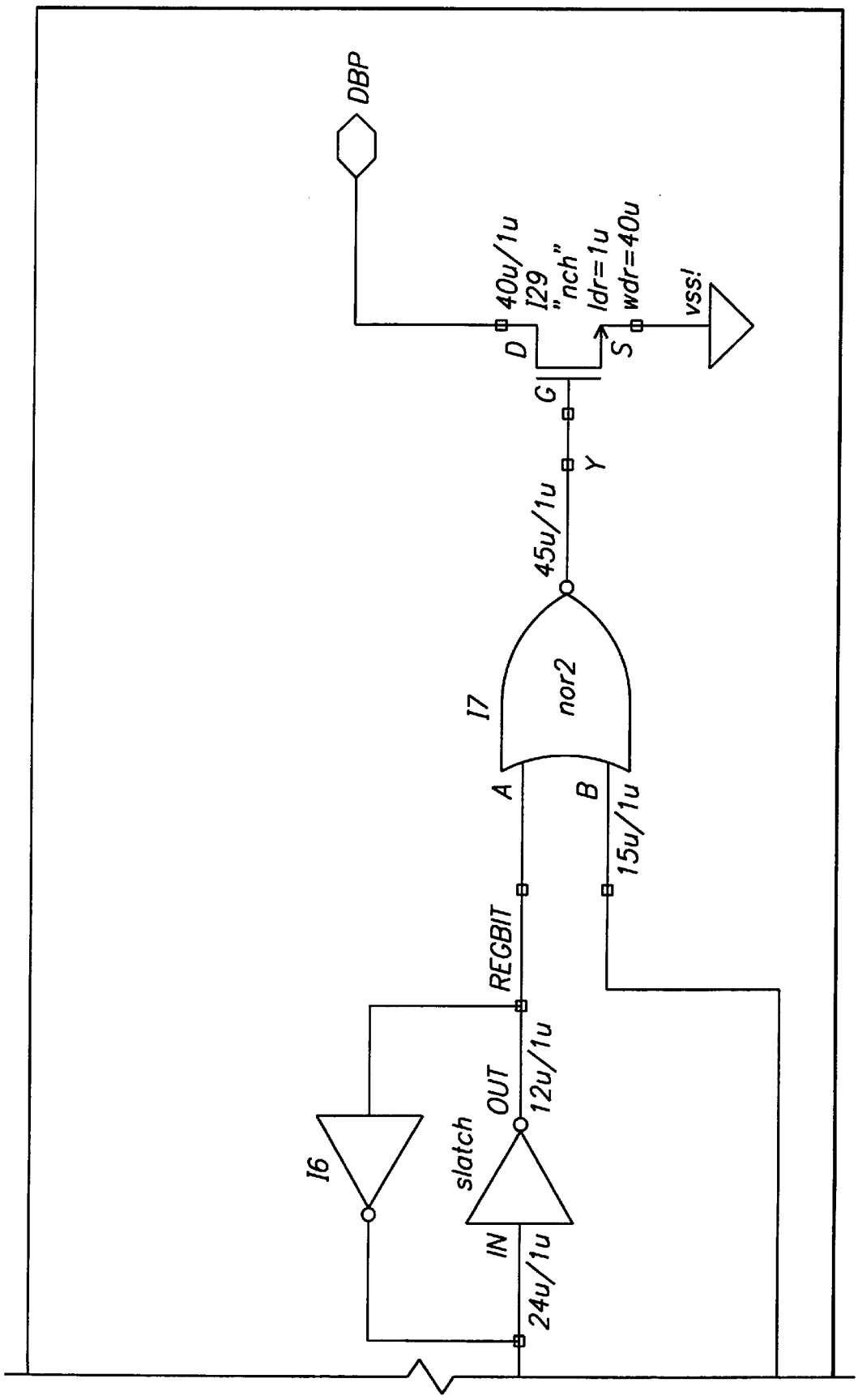

DBP
40u/1u
I29
"nch"
ldr=1u
wdr=40u
vss!
D
S
G
Y
45u/1u
I7
nor2
A
B
15u/1u
REGBIT
12u/1u
OUT
slatch
I6
IN
24u/1u

FIG 1.0047AA

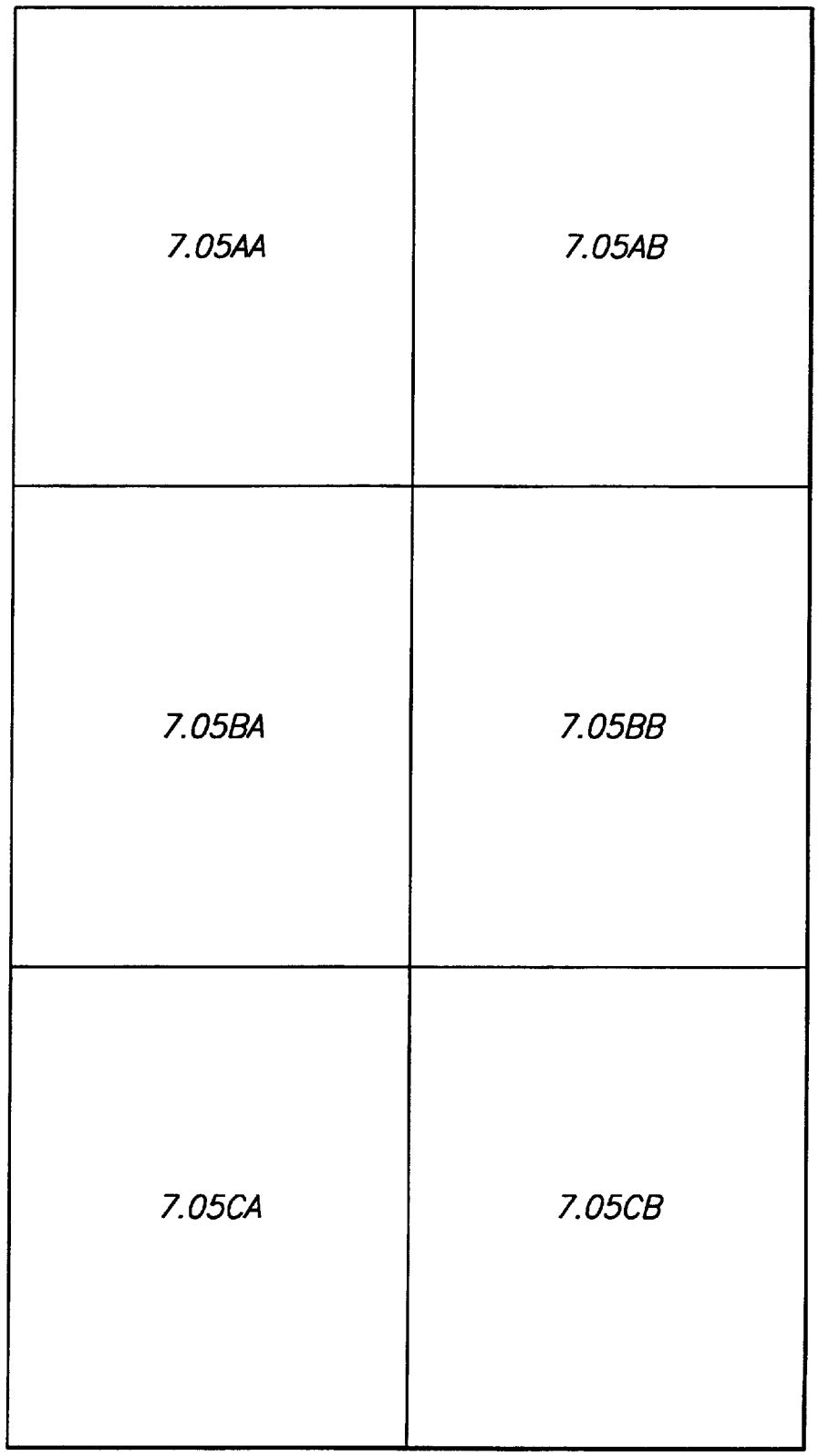


Fig 7.05

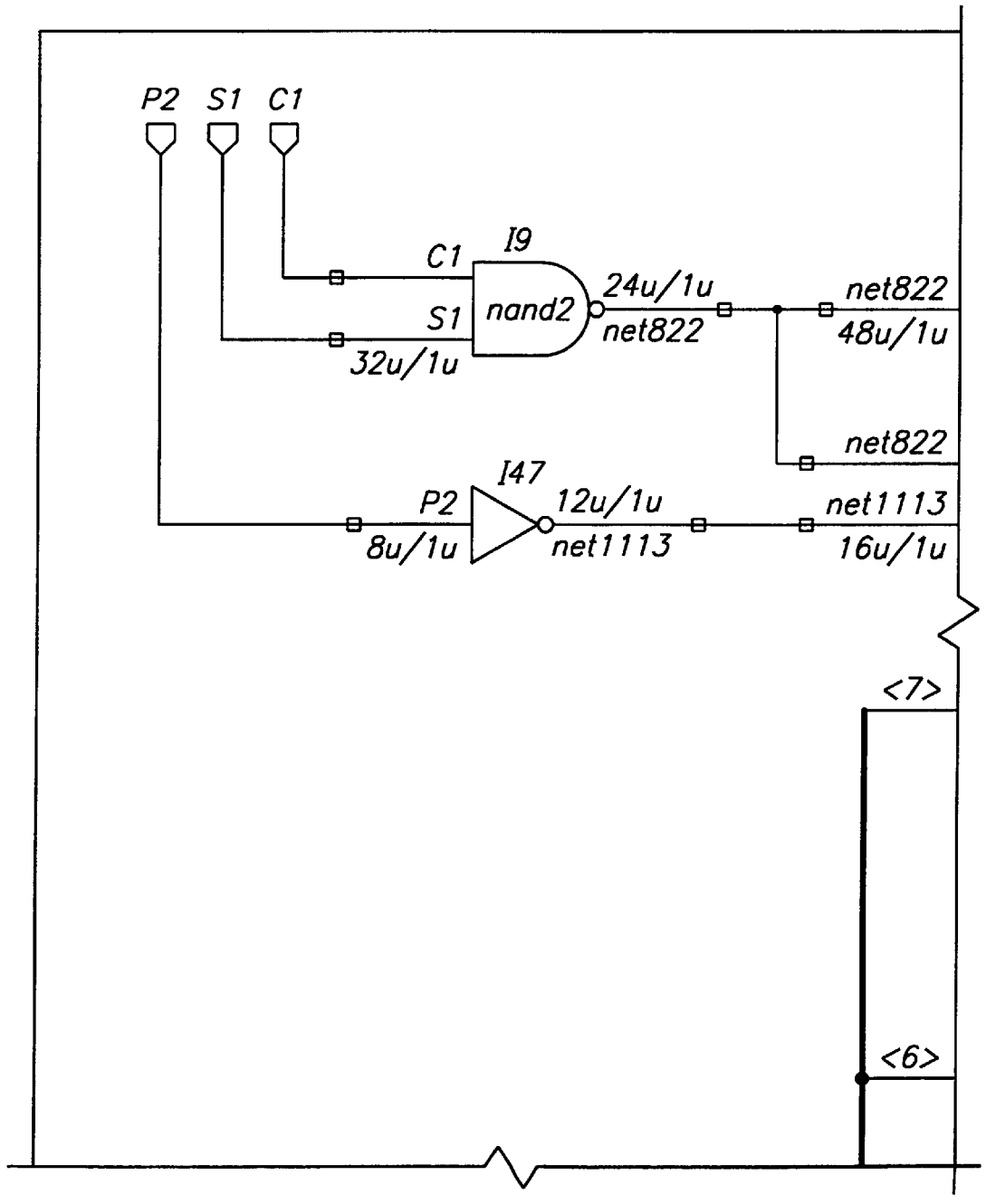

P2
S1
C1
I9
C1
S1
nand2
24u/1u
net822
32u/1u
net822
48u/1u
net822
I47
P2
12u/1u
net1113
8u/1u
net1113
16u/1u
<7>
<6>

Fig 1.05AA

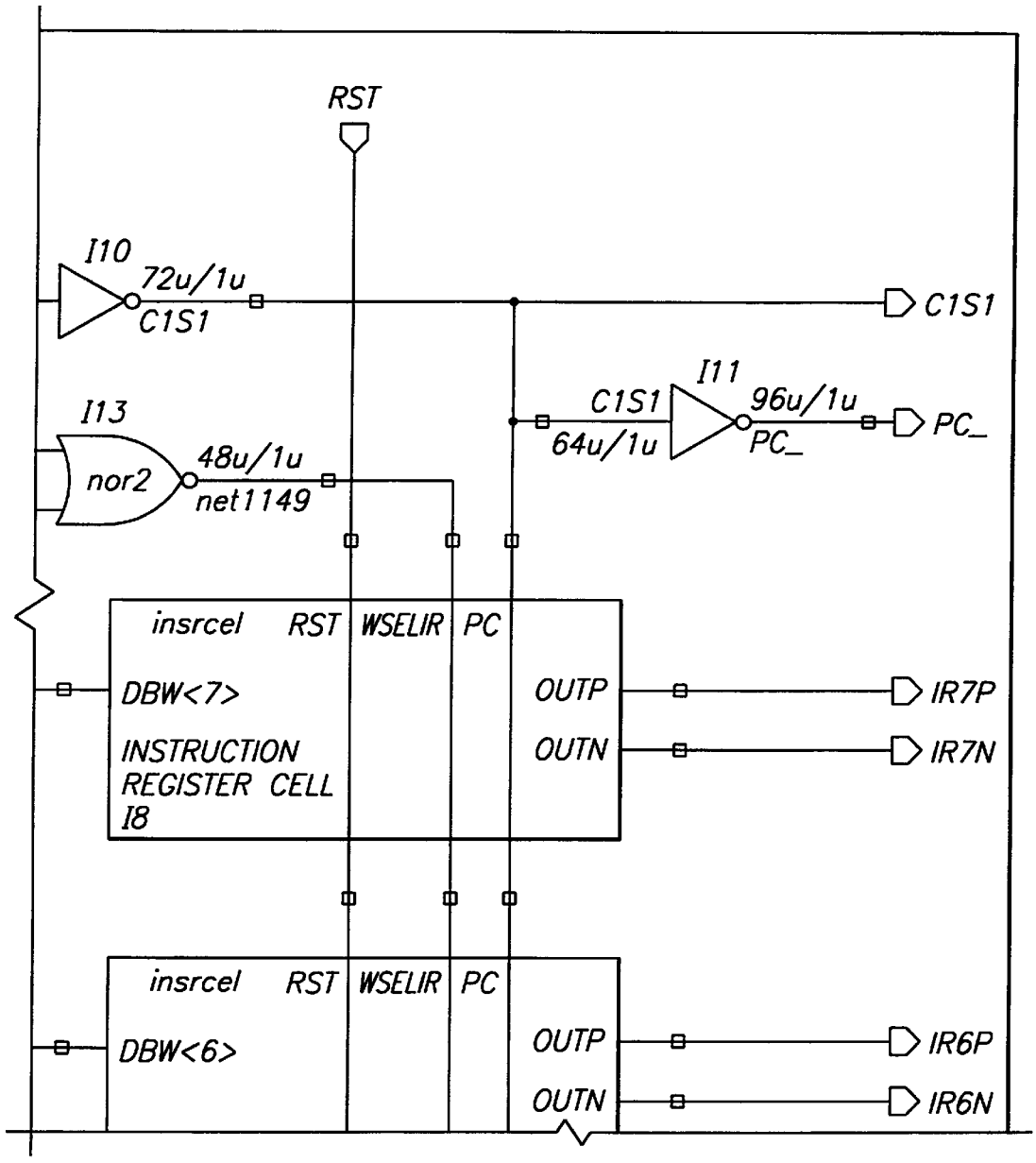

RST
I10
72u/1u
C1S1
C1S1
I11
C1S1
96u/1u
PC_
64u/1u
PC_
I13
nor2
48u/1u
net1149
insrcel
RST
WSELIR
PC
DBW<7>
OUTP
OUTN
IR7P
IR7N
INSTRUCTION
REGISTER CELL
I8
insrcel
RST
WSELIR
PC
DBW<6>
OUTP
OUTN
IR6P
IR6N

Fig 1.05AB

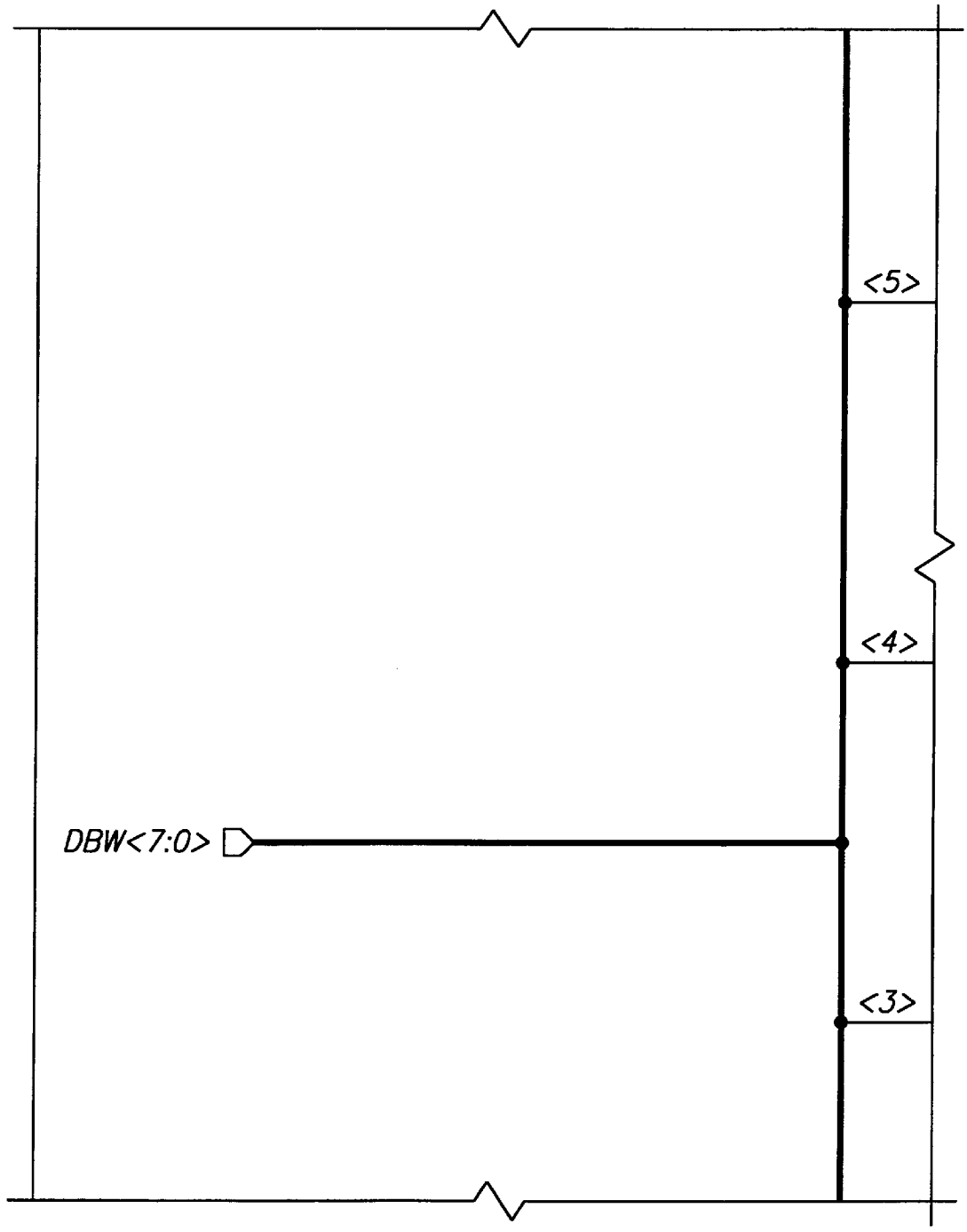


Fig 1.05BA

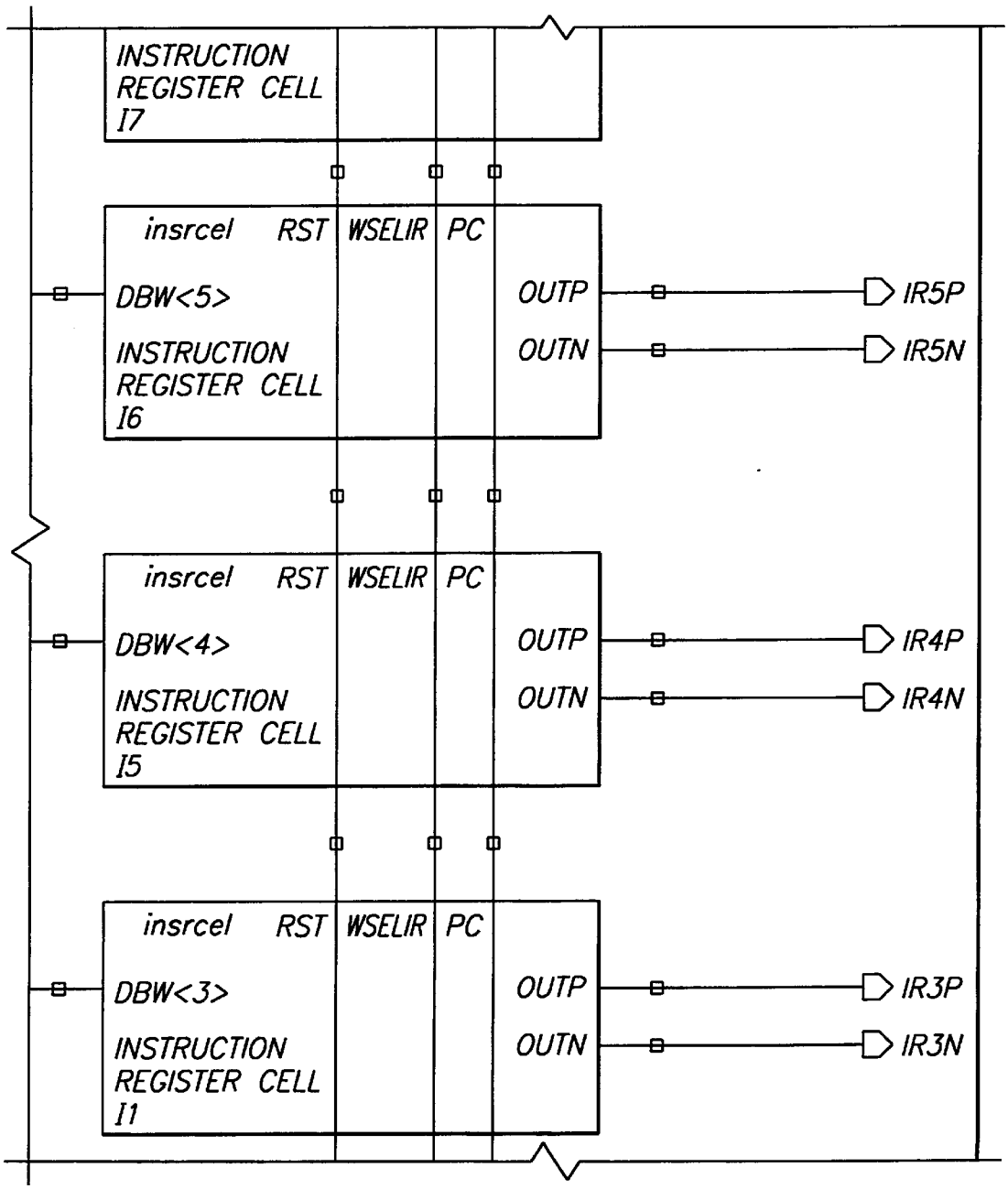

INSTRUCTION REGISTER CELL I7
insrcel
RST
WSELIR
PC
DBW<5>
INSTRUCTION REGISTER CELL I6
OUTP
OUTN
IR5P
IR5N
insrcel
RST
WSELIR
PC
DBW<4>
INSTRUCTION REGISTER CELL I5
OUTP
OUTN
IR4P
IR4N
insrcel
RST
WSELIR
PC
DBW<3>
INSTRUCTION REGISTER CELL I1
OUTP
OUTN
IR3P
IR3N

Fig 1.05BB

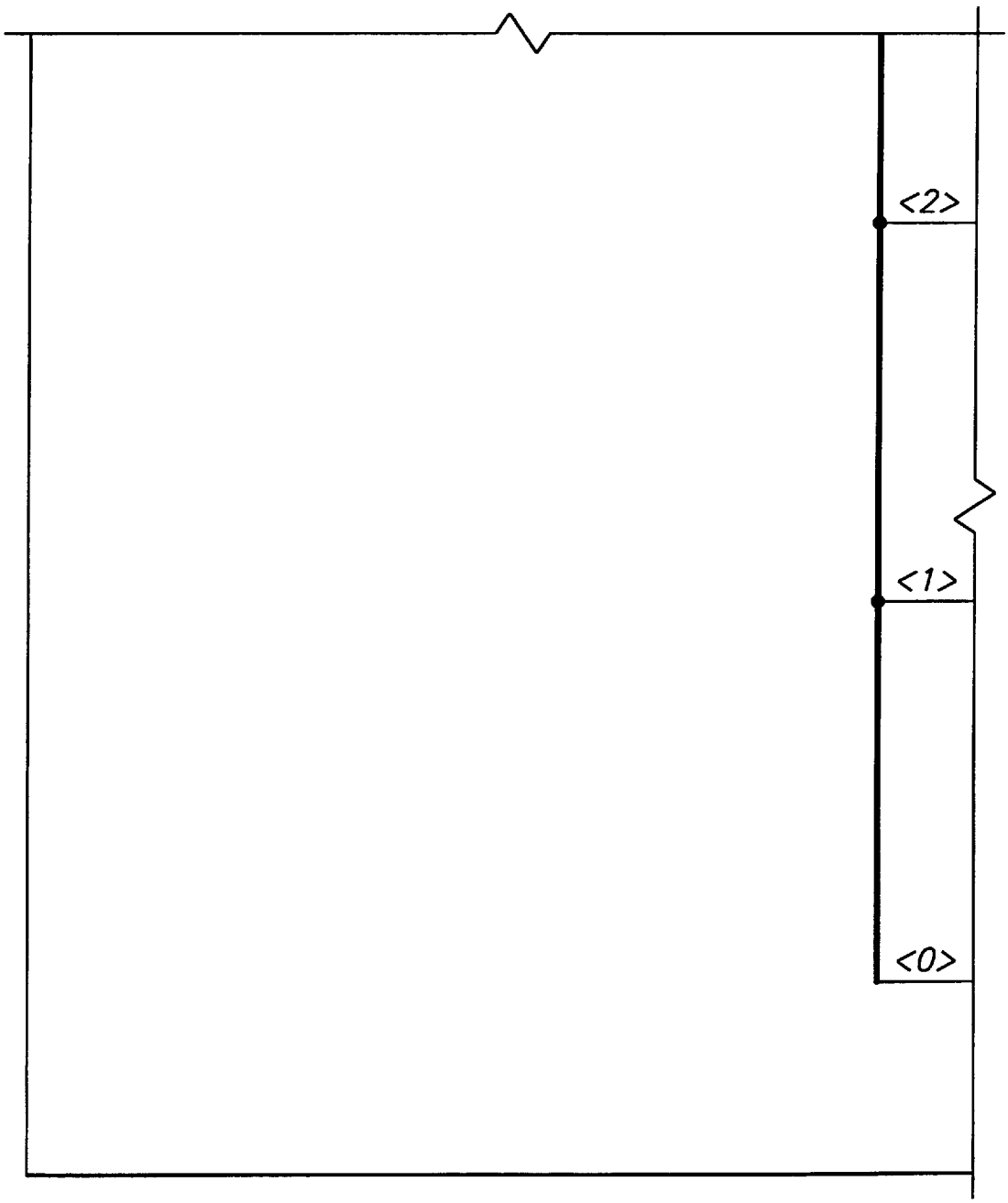


Fig 1.05CA

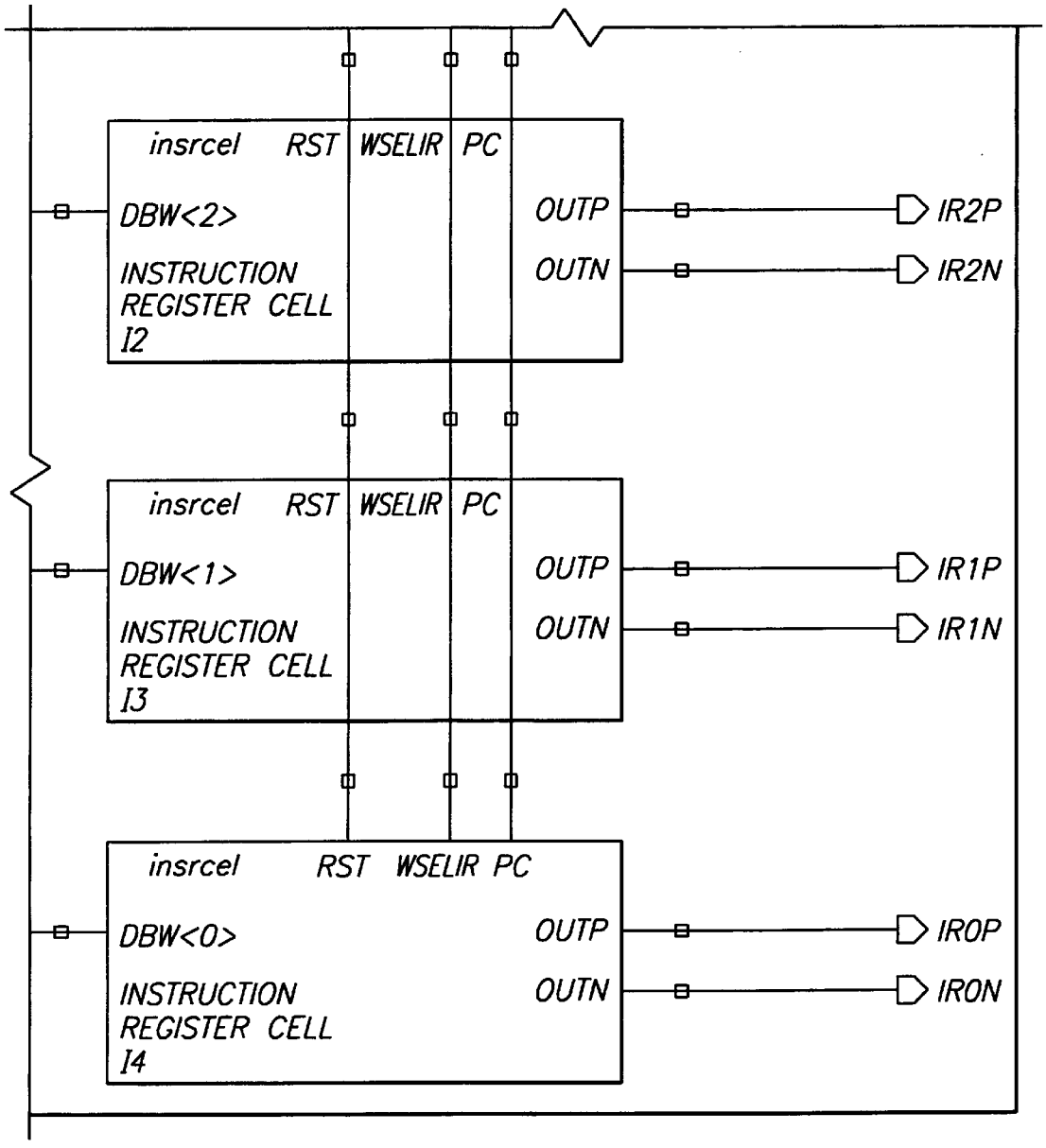
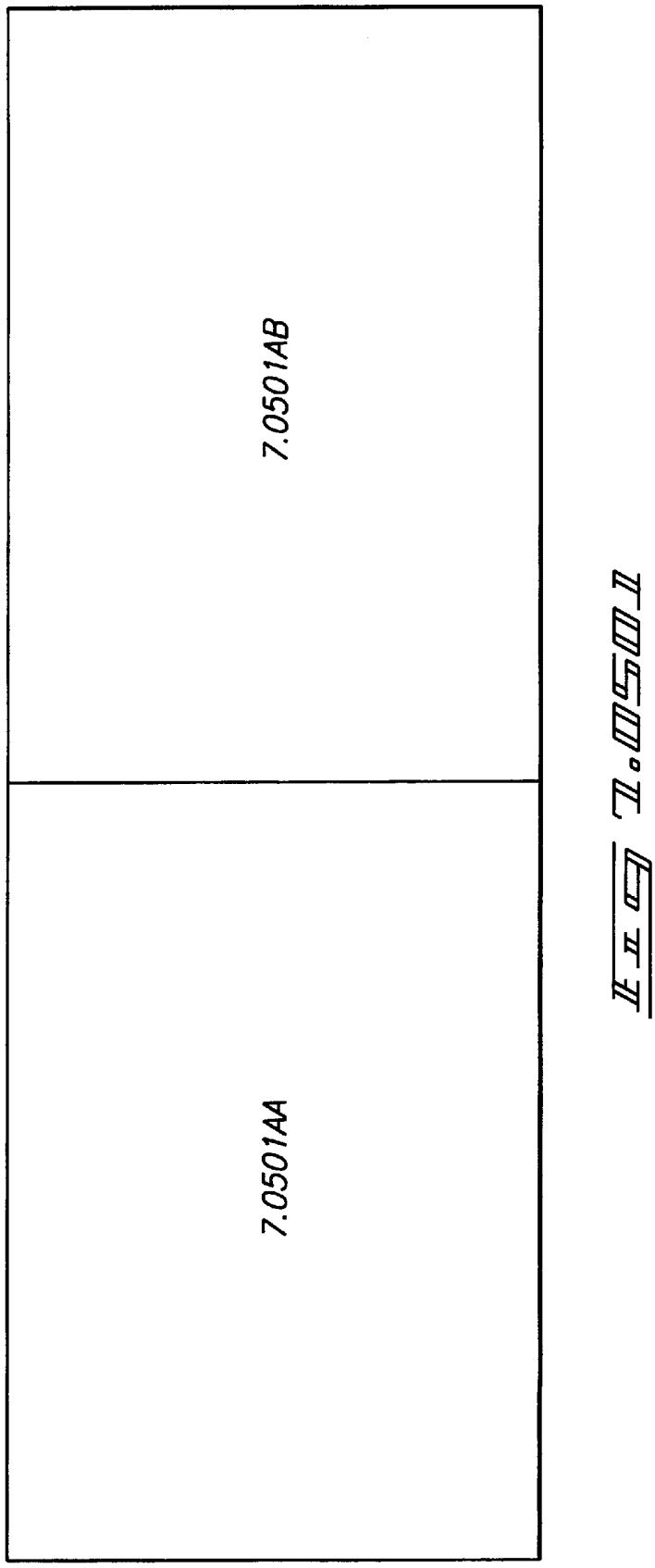

insrcel
RST
WSELIR
PC
DBW<2>
INSTRUCTION REGISTER CELL I2
OUTP
OUTN
IR2P
IR2N
insrcel
RST
WSELIR
PC
DBW<1>
INSTRUCTION REGISTER CELL I3
OUTP
OUTN
IR1P
IR1N
insrcel
RST
WSELIR
PC
DBW<0>
INSTRUCTION REGISTER CELL I4
OUTP
OUTN
IR0P
IR0N

Fig 1.05CB


7.0501AB
7.0501AA
FIG 7.0501

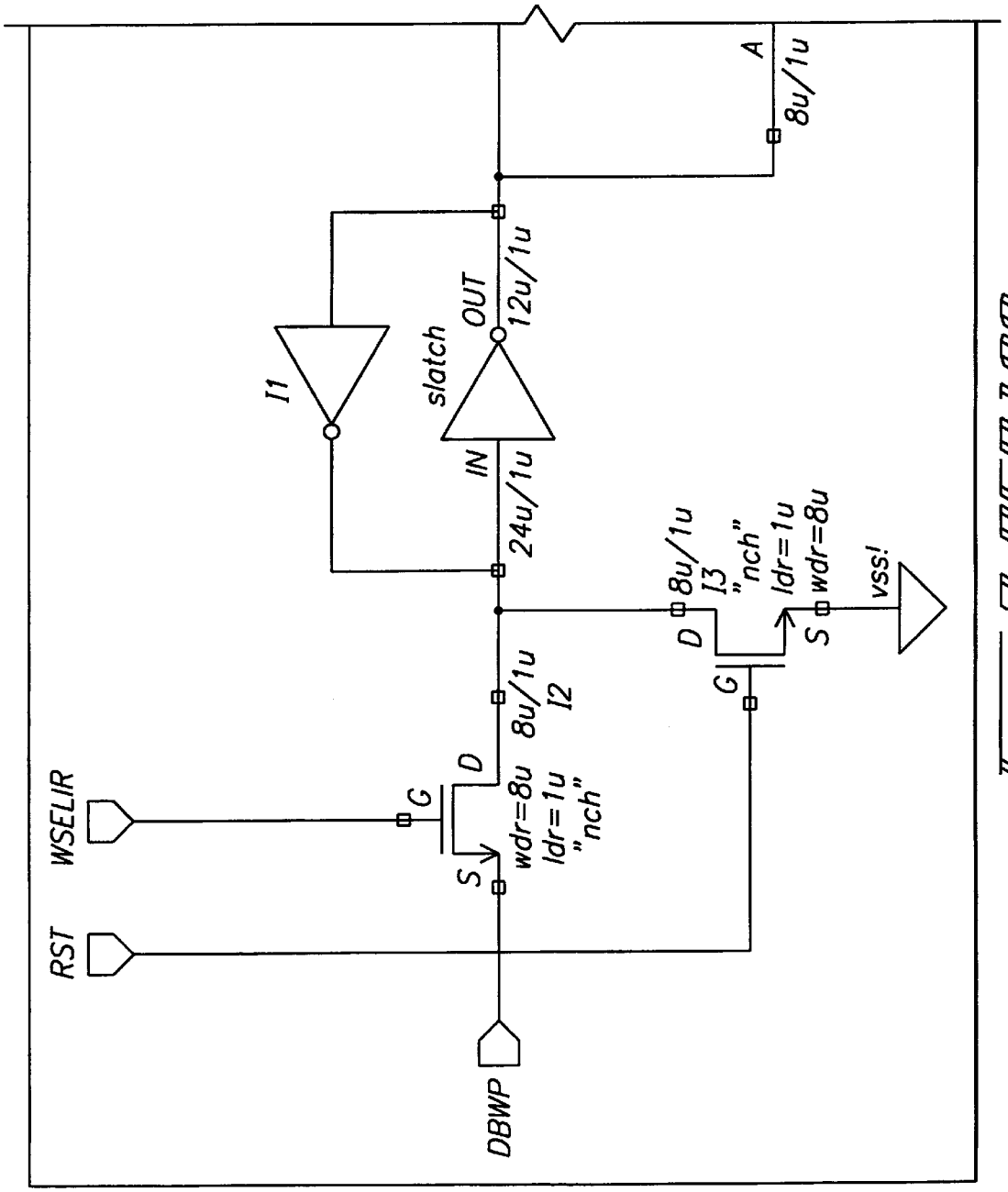


Fig. 11.0511AA

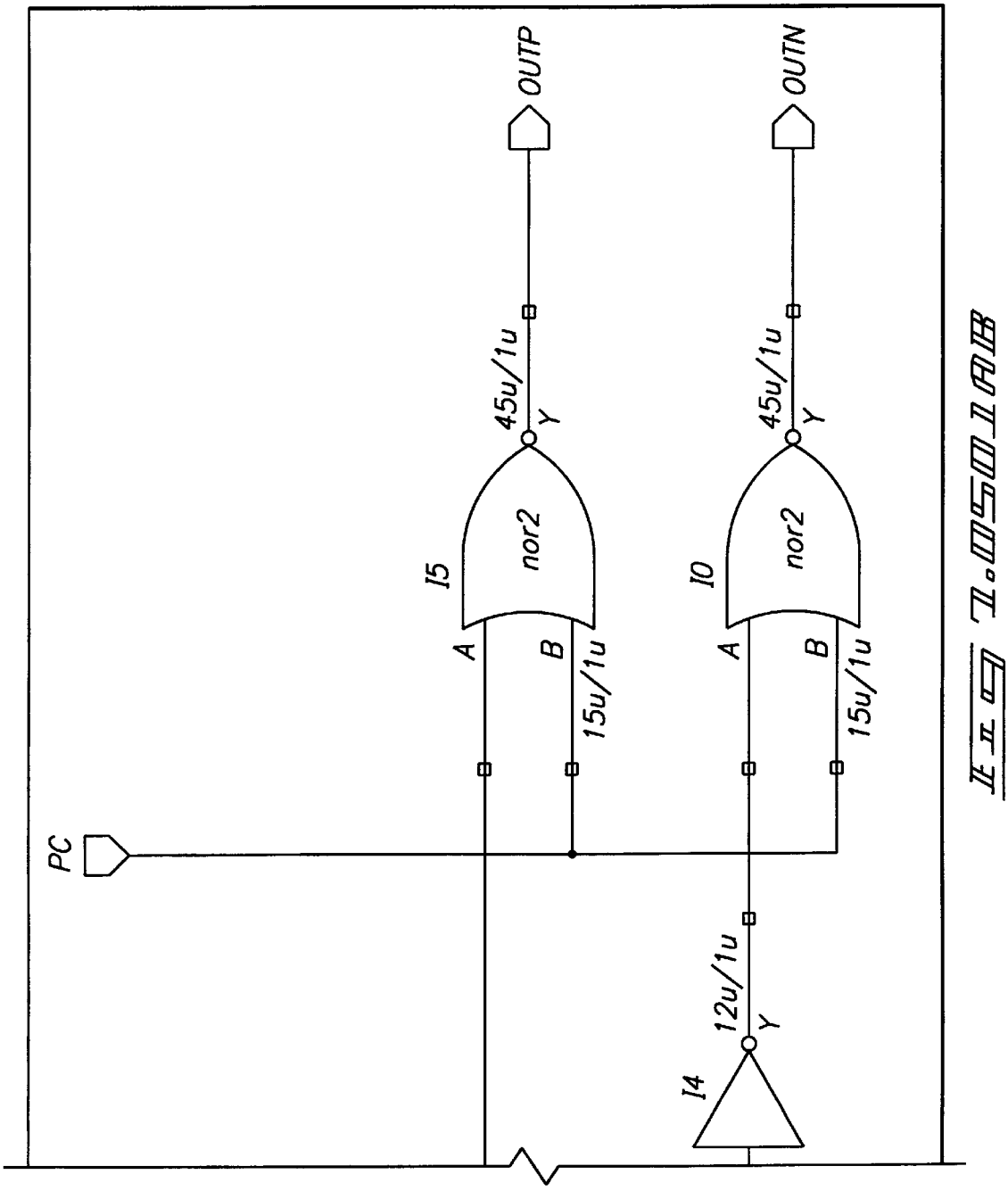


FIG 11.0501AB

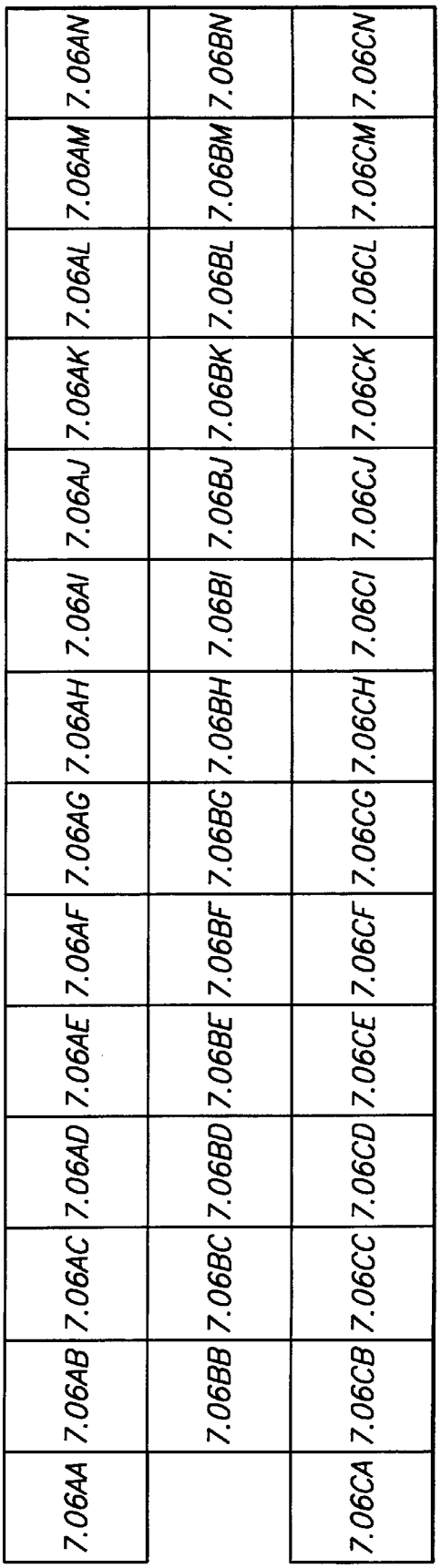

7.06AA
7.06AB
7.06AC
7.06AD
7.06AE
7.06AF
7.06AG
7.06AH
7.06AI
7.06AJ
7.06AK
7.06AL
7.06AM
7.06AN
7.06BB
7.06BC
7.06BD
7.06BE
7.06BF
7.06BG
7.06BH
7.06BI
7.06BJ
7.06BK
7.06BL
7.06BM
7.06BN
7.06CA
7.06CB
7.06CC
7.06CD
7.06CE
7.06CF
7.06CG
7.06CH
7.06CI
7.06CJ
7.06CK
7.06CL
7.06CM
7.06CN

FIG. 7.06S

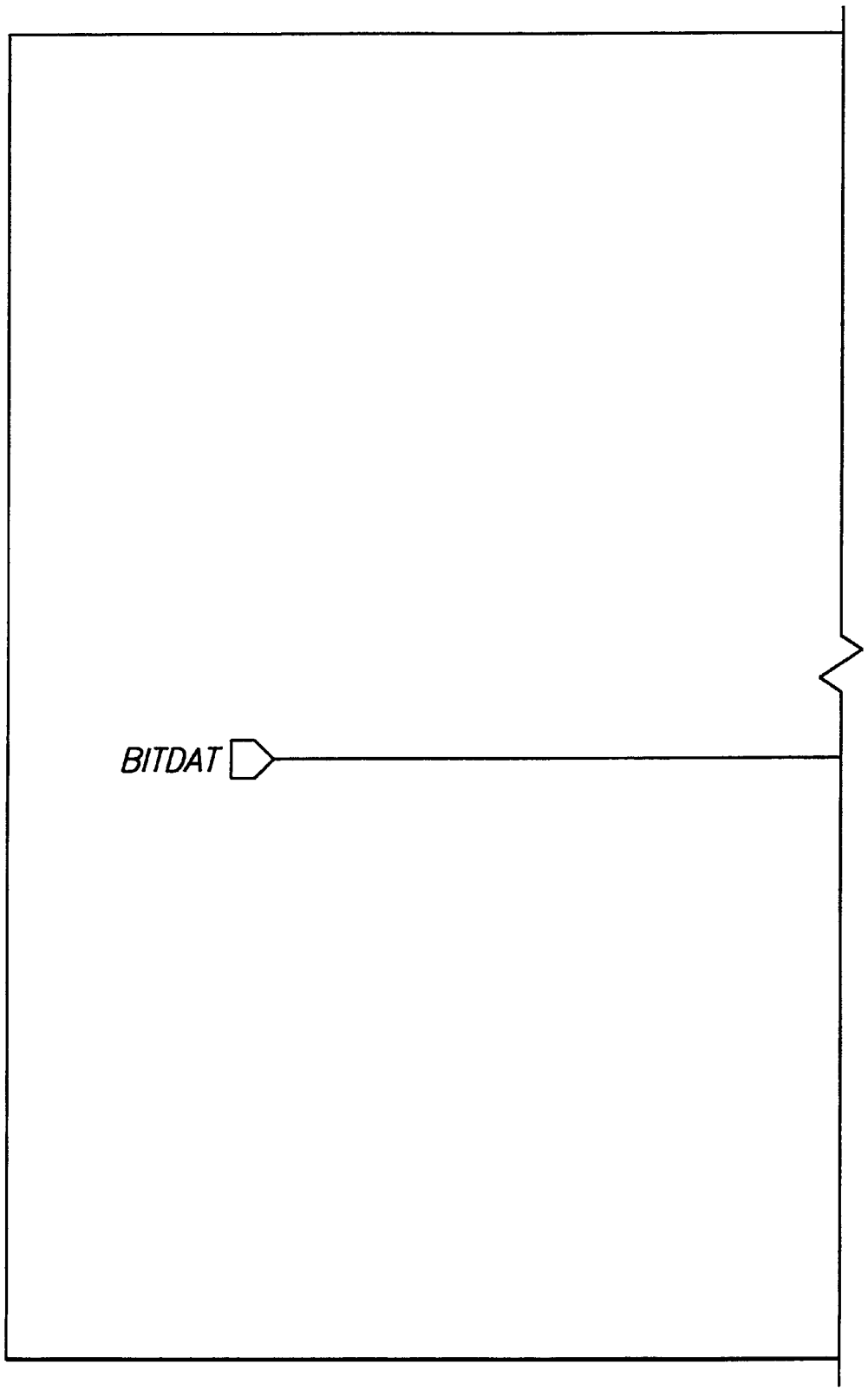


Fig 1.06AA

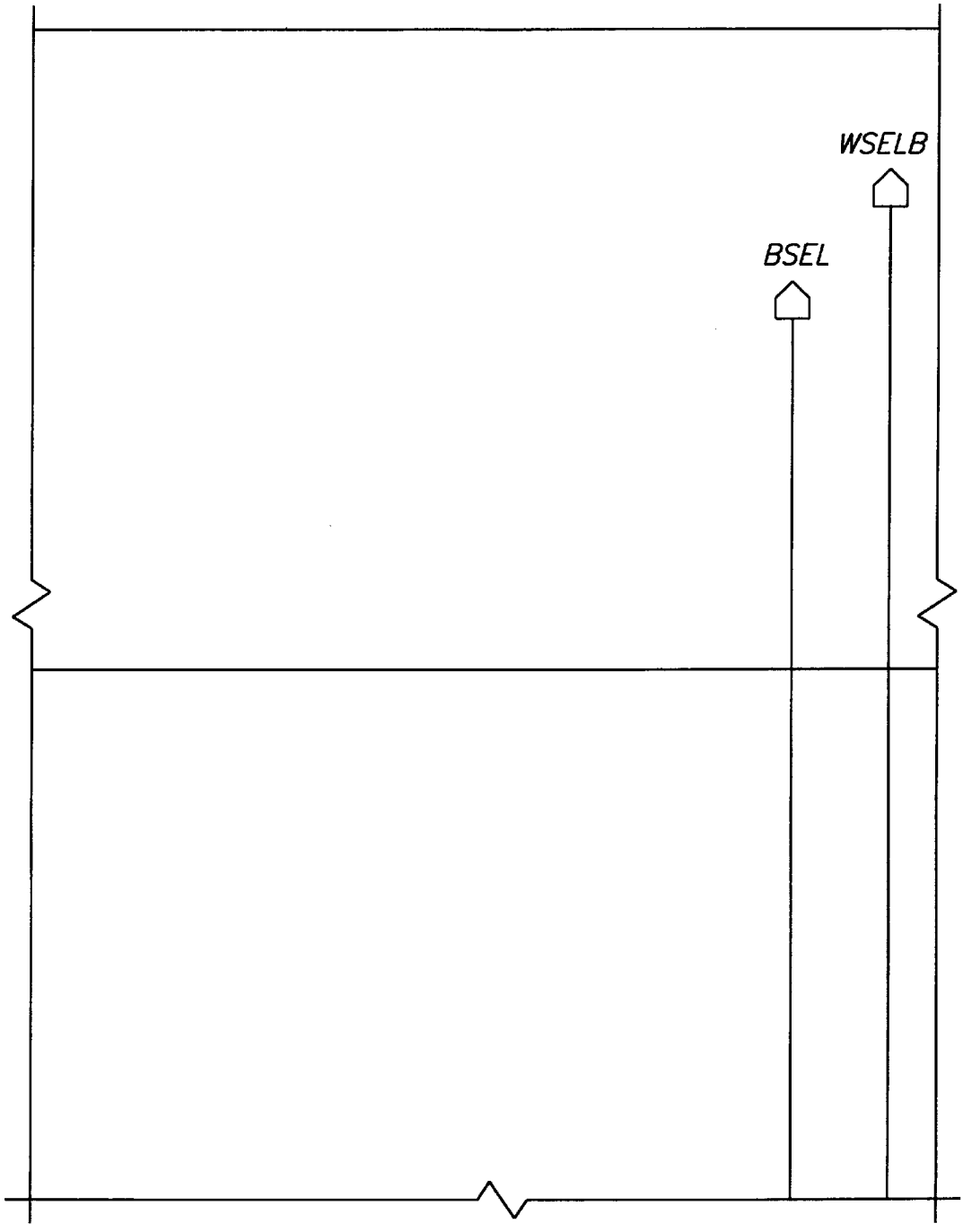


Fig 1.06AB

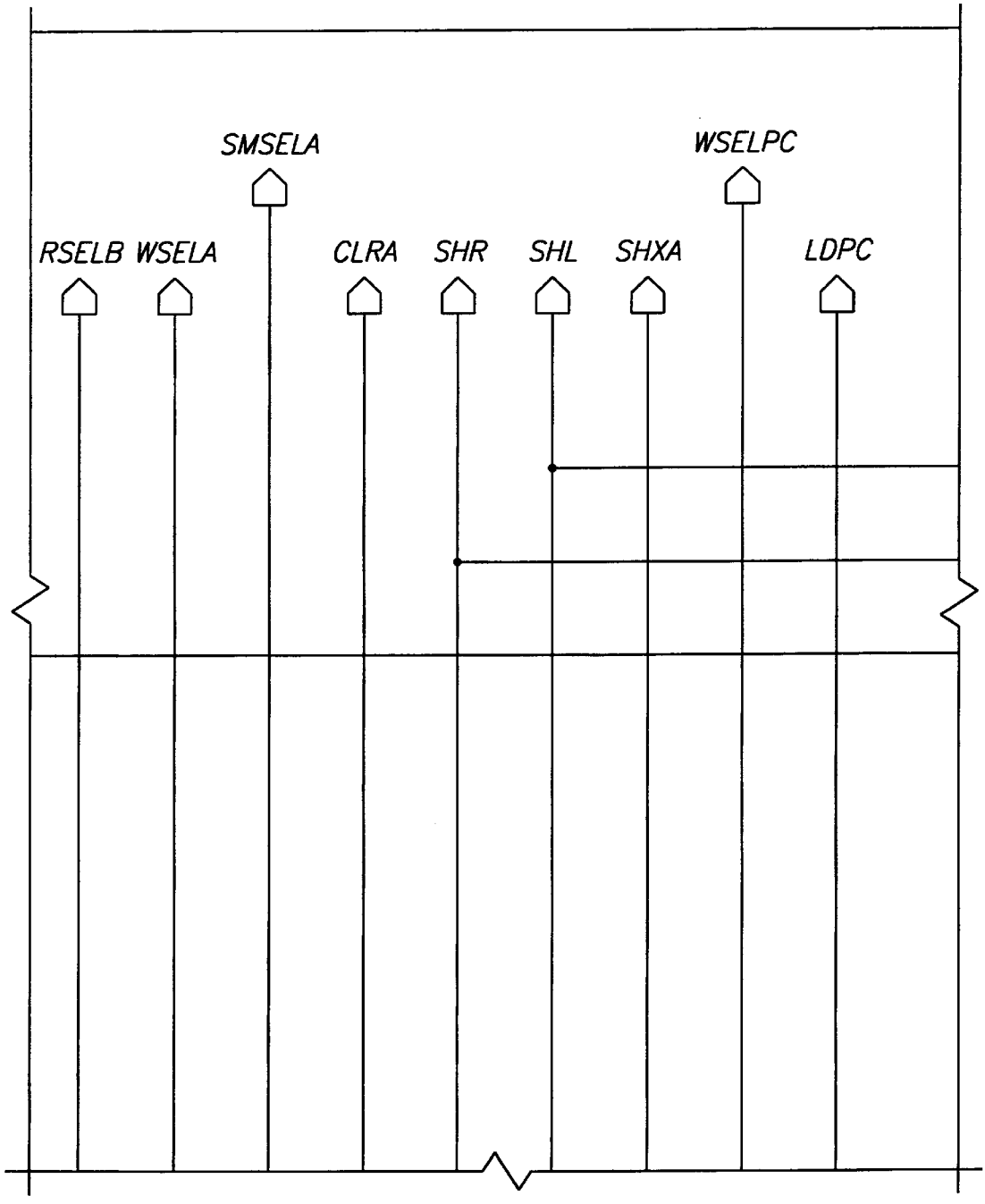


Fig 1.06AC

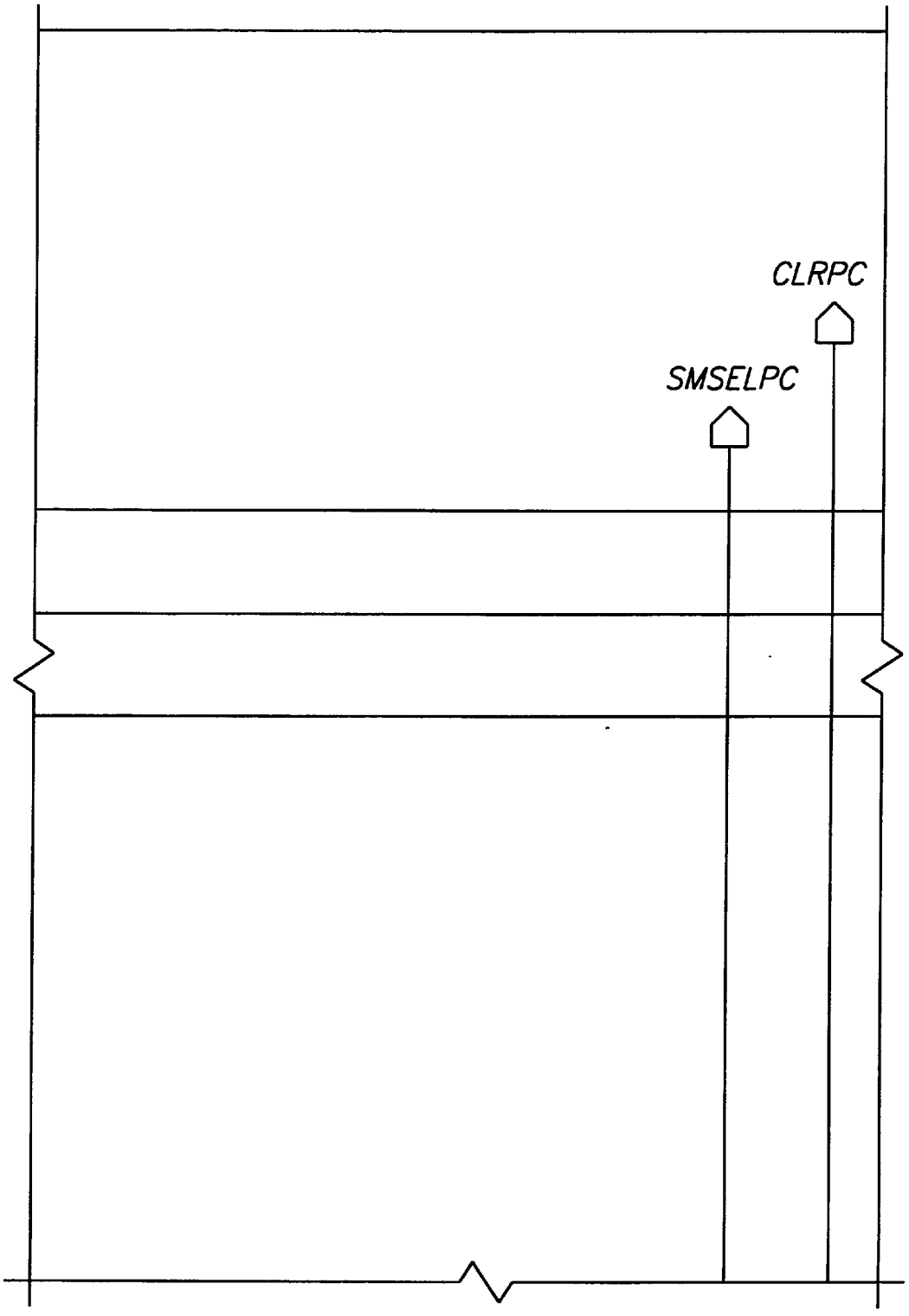


Fig 1.06AD

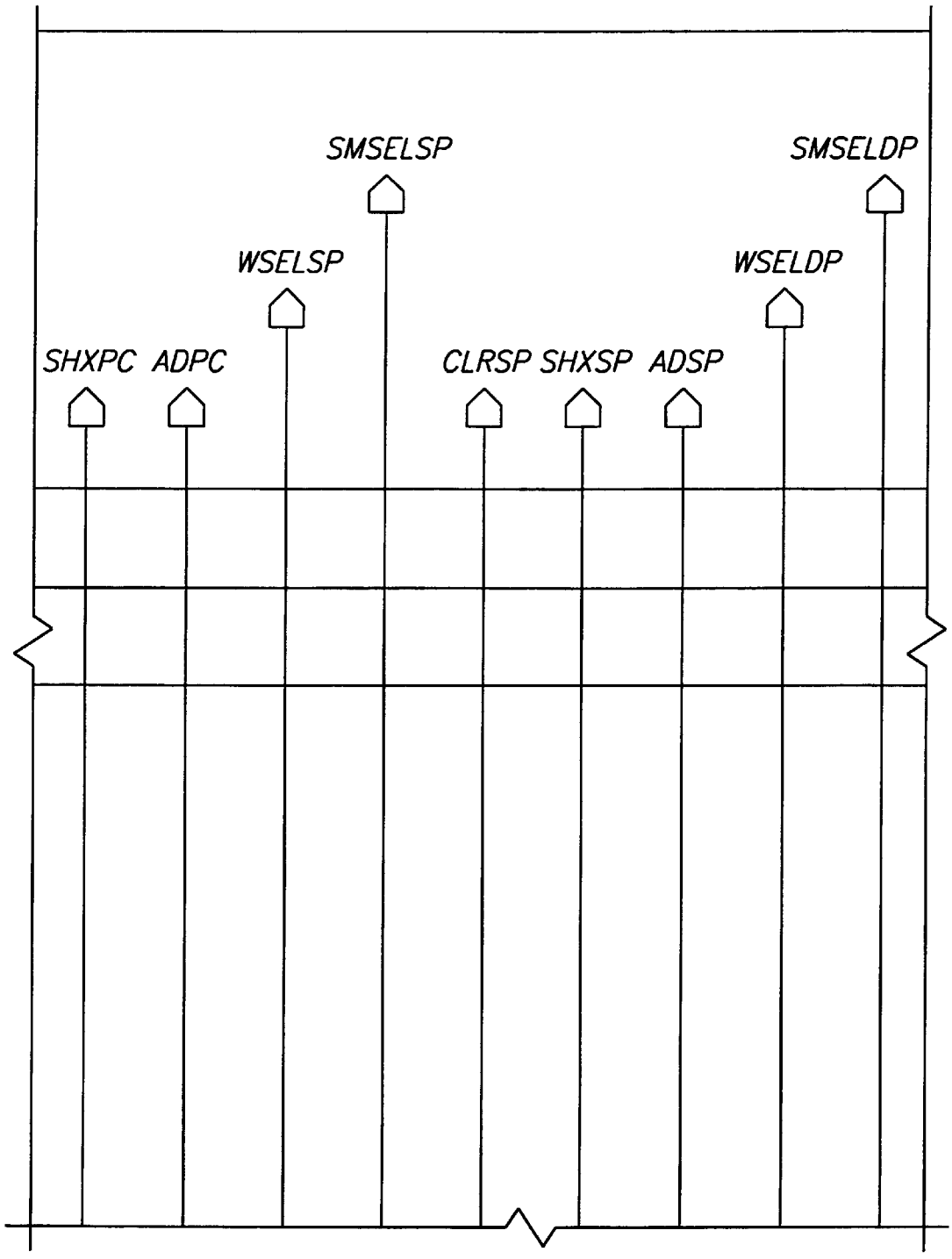


Fig 1.06AE

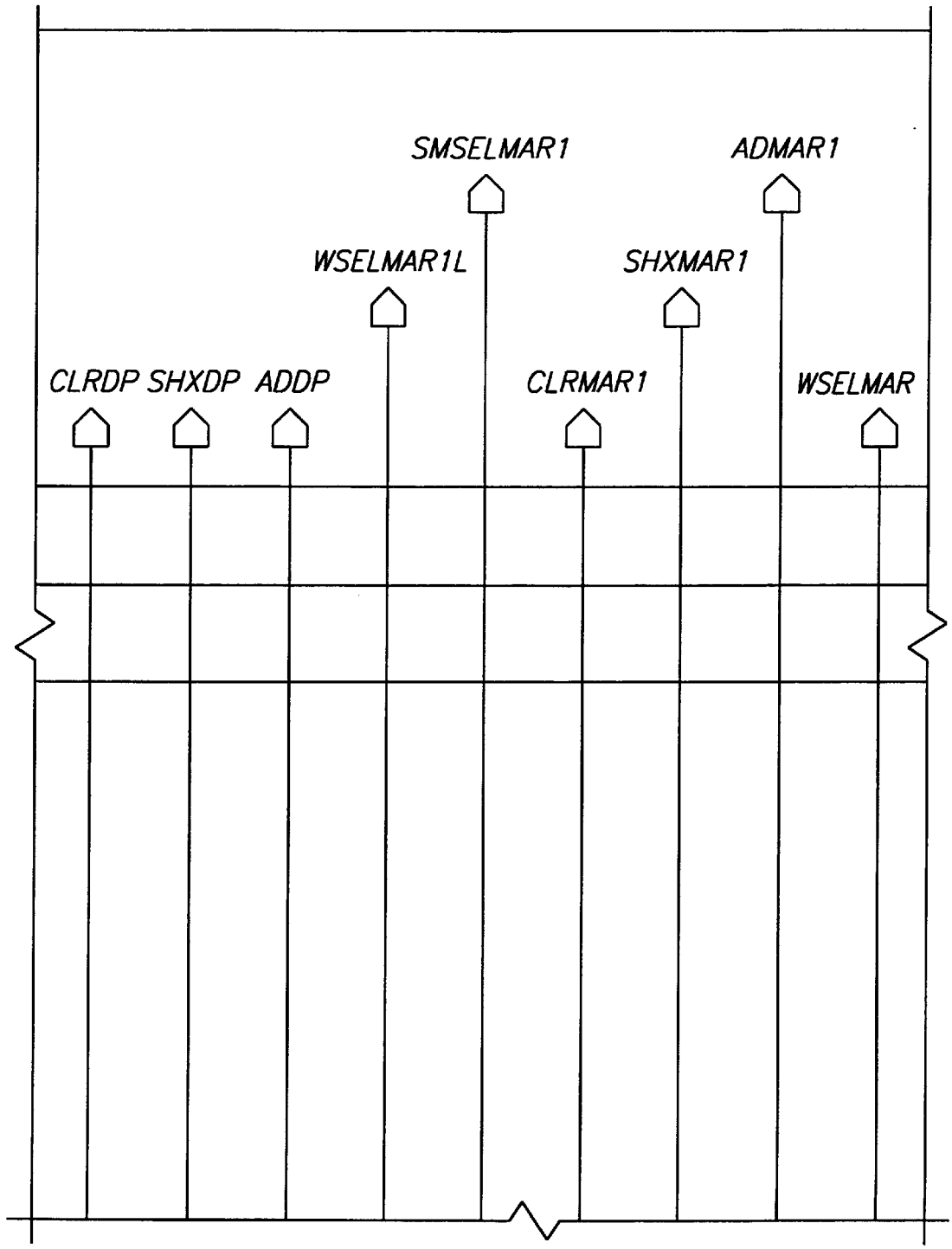

SMSELMAR1
ADMAR1
WSELMAR1L
SHXMAR1
CLRDP
SHXDP
ADDP
CLRMAR1
WSELMAR

Fig 1.06AF

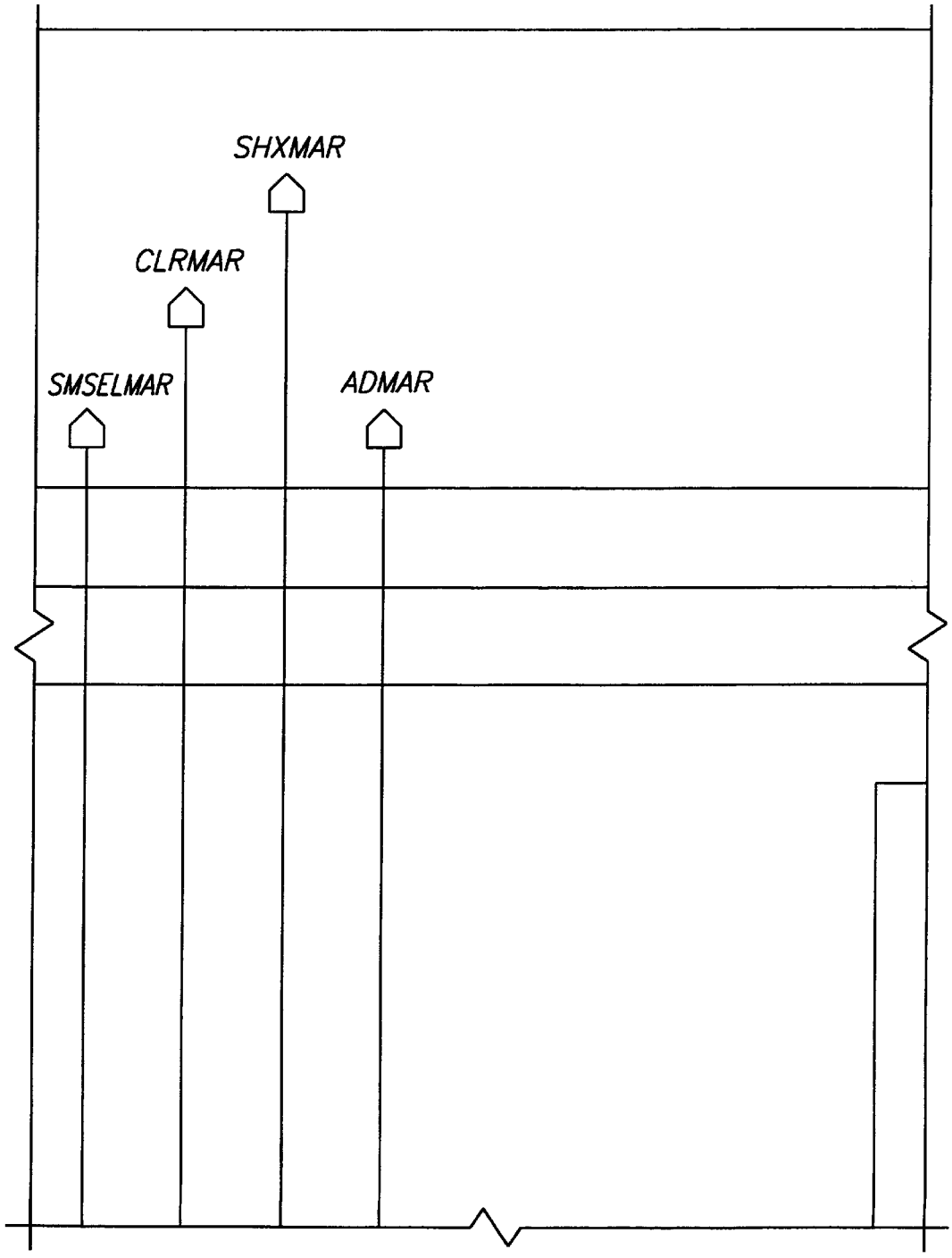


Fig 1.06A6

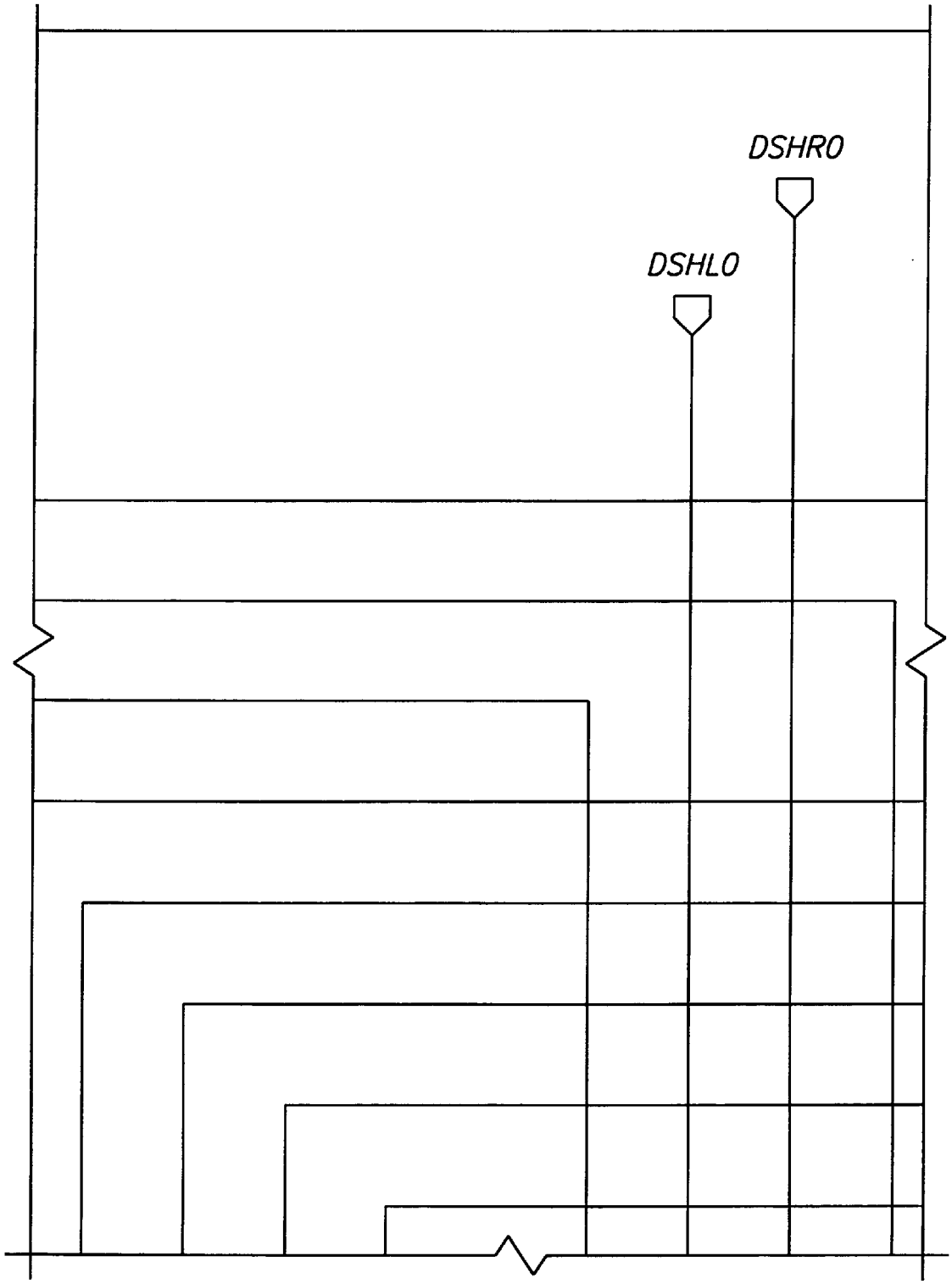


Fig 1.06AH

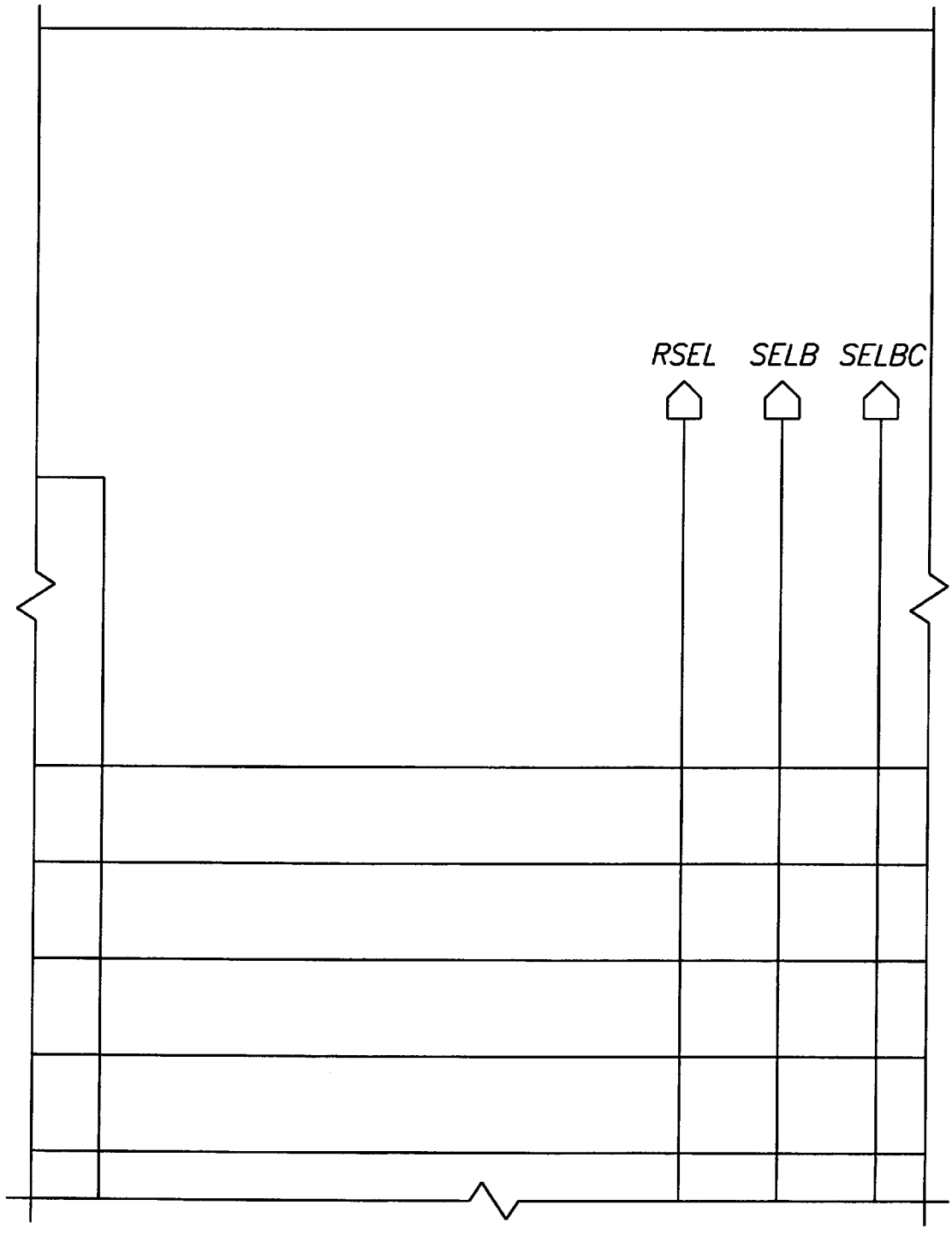


Fig 1.06AII

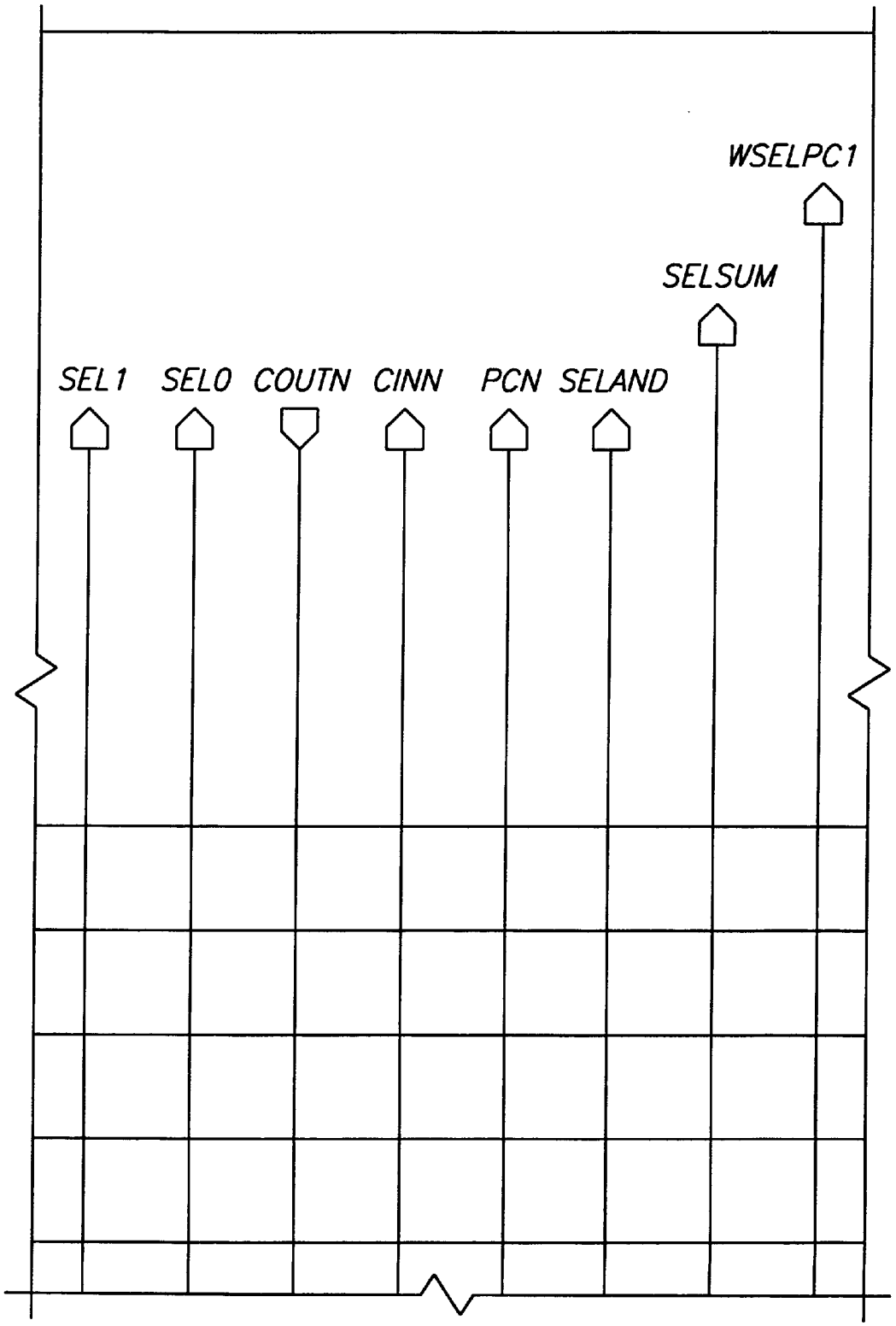


Fig 1.0604

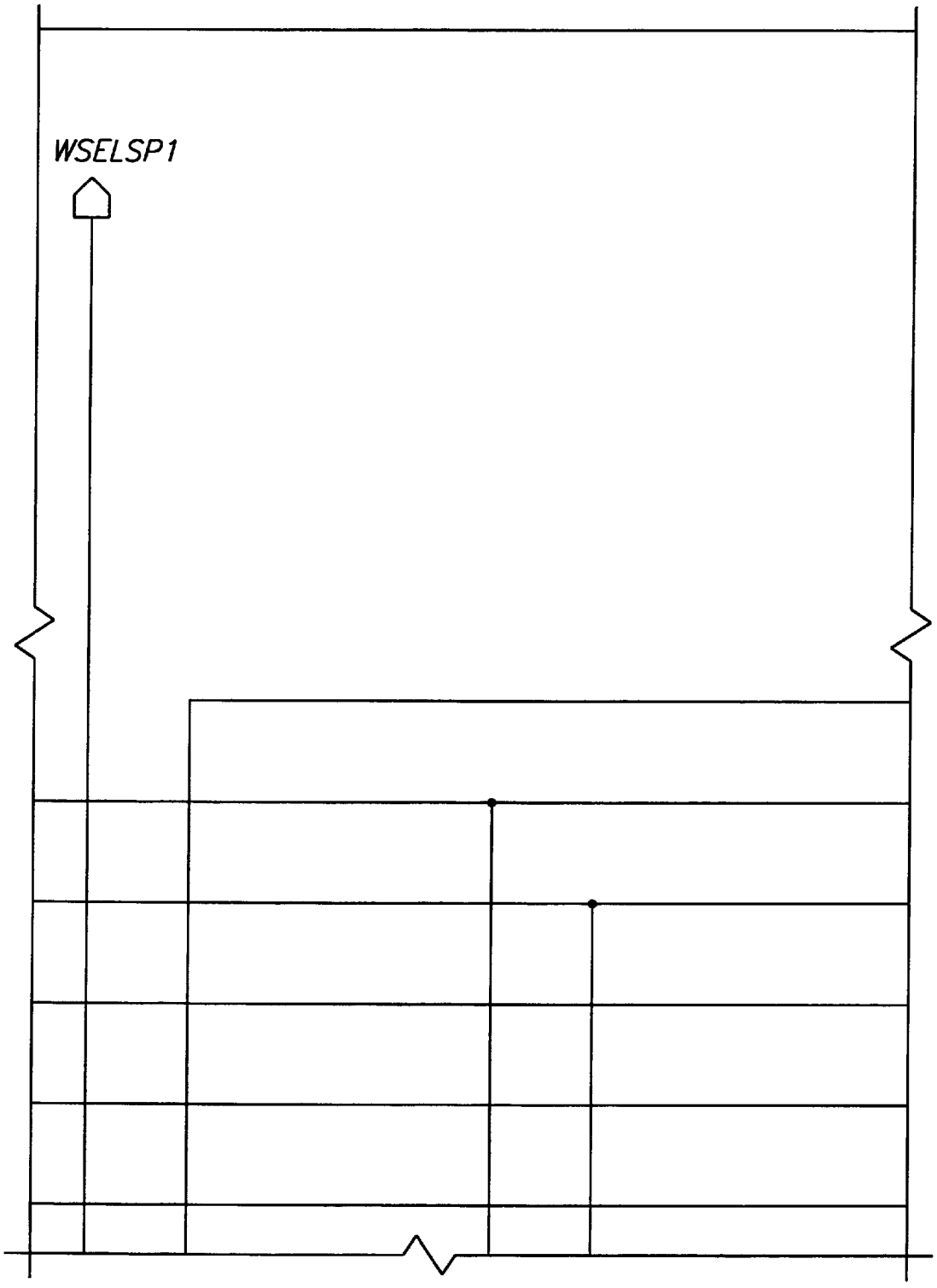


Fig 1.06AK

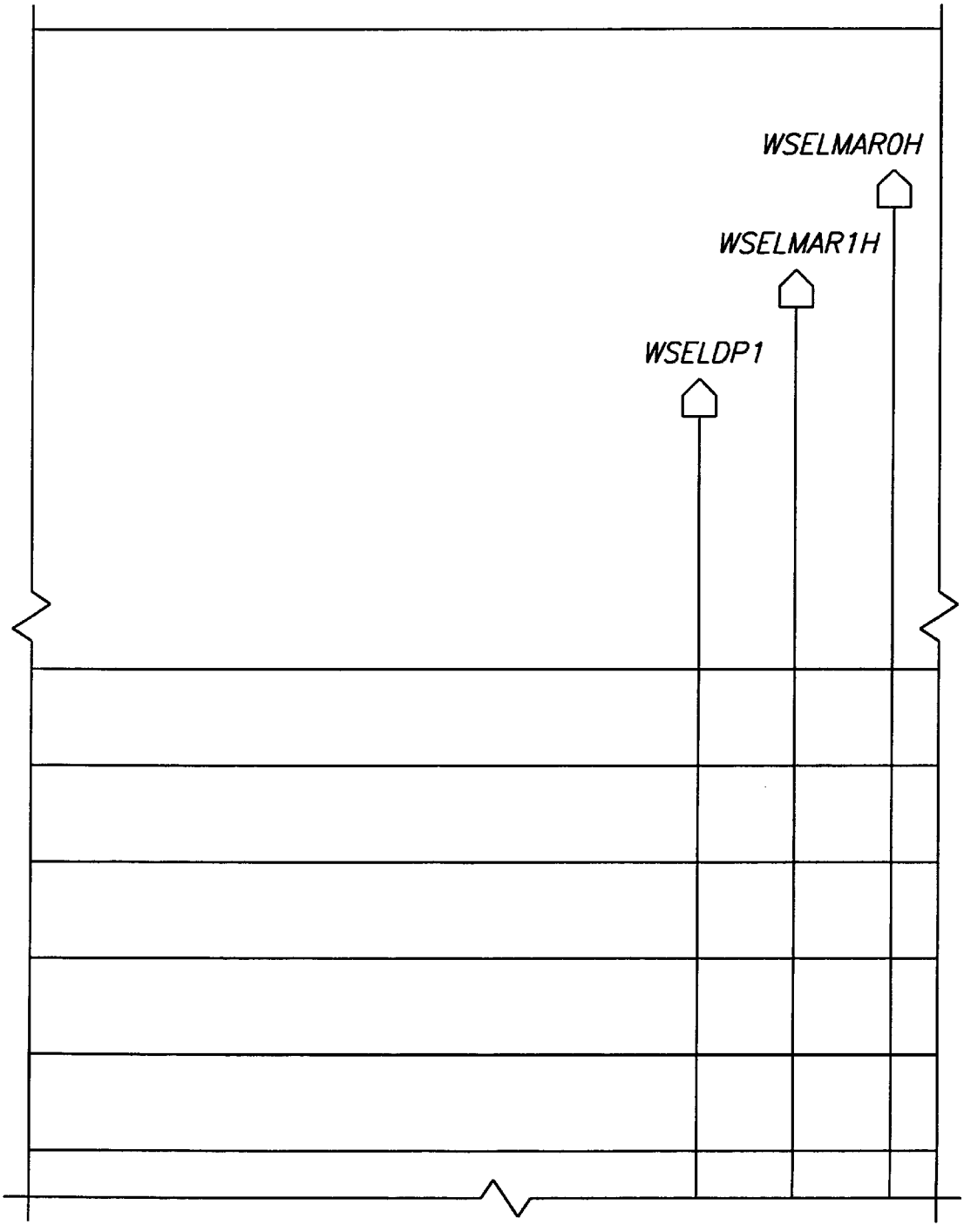


Fig 1.06AL

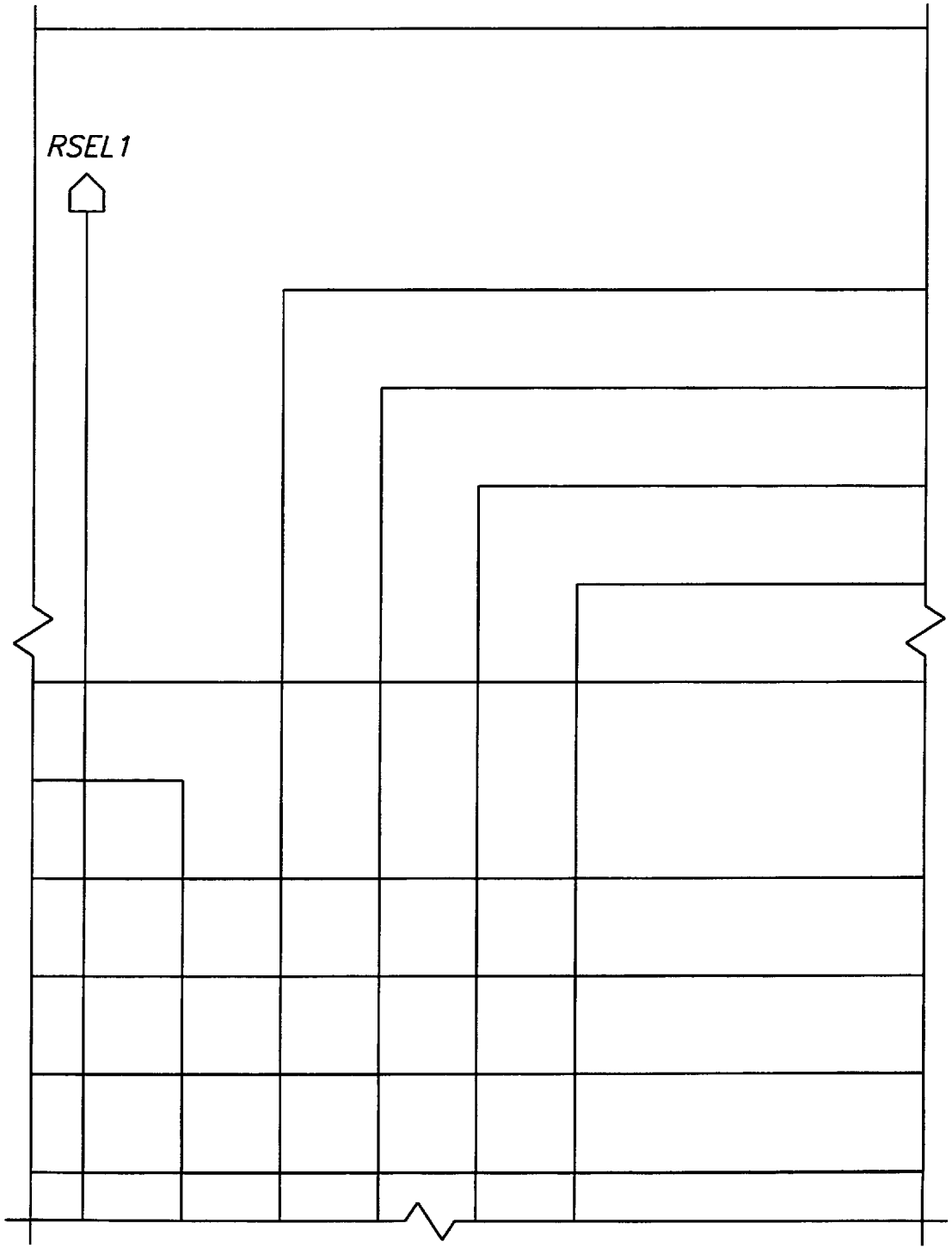


Fig 1.06AM

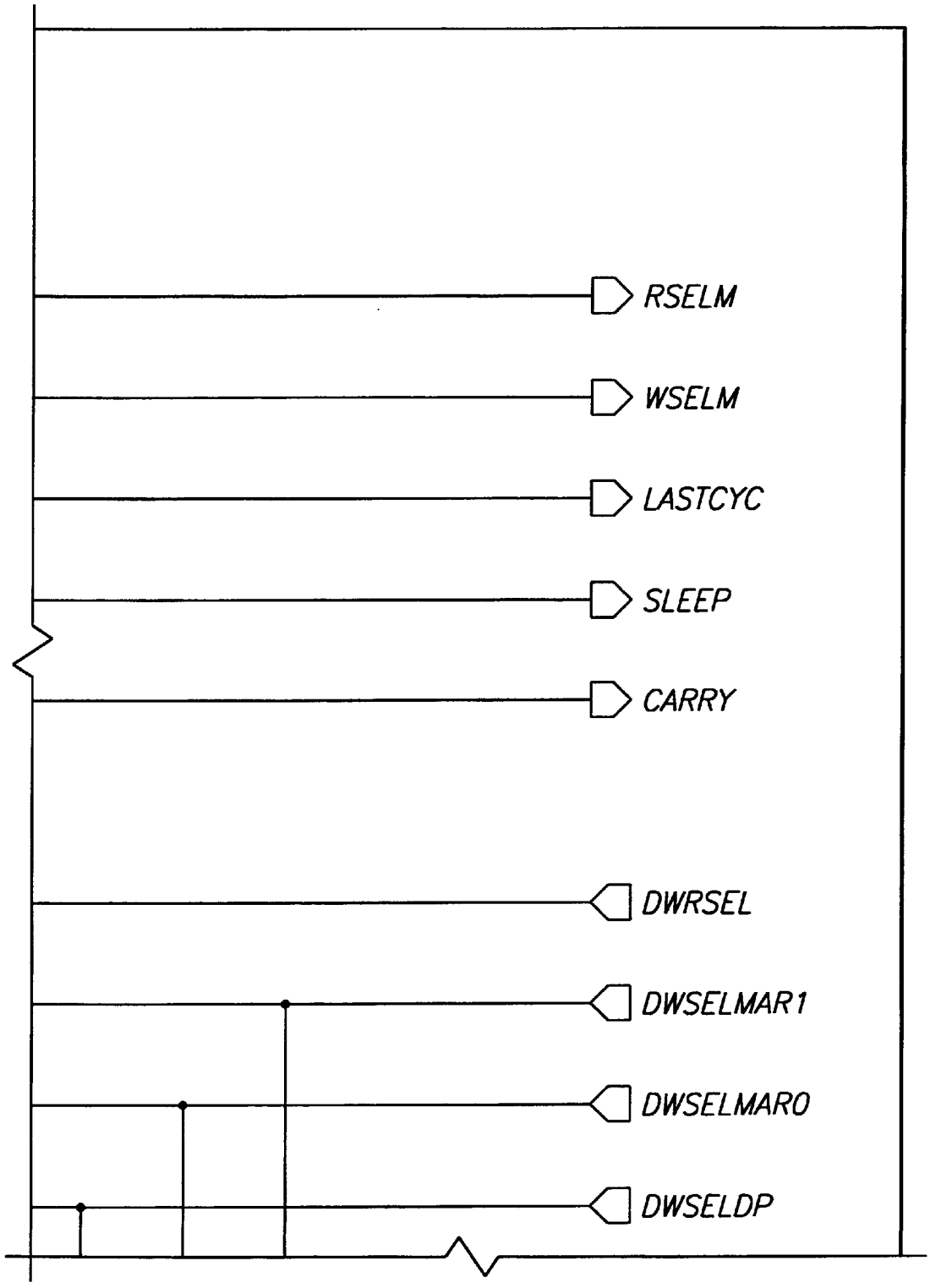

RSELM
WSELM
LASTCYC
SLEEP
CARRY
DWRSEL
DWSELMAR1
DWSELMAR0
DWSELDP

Fig 1.06AN

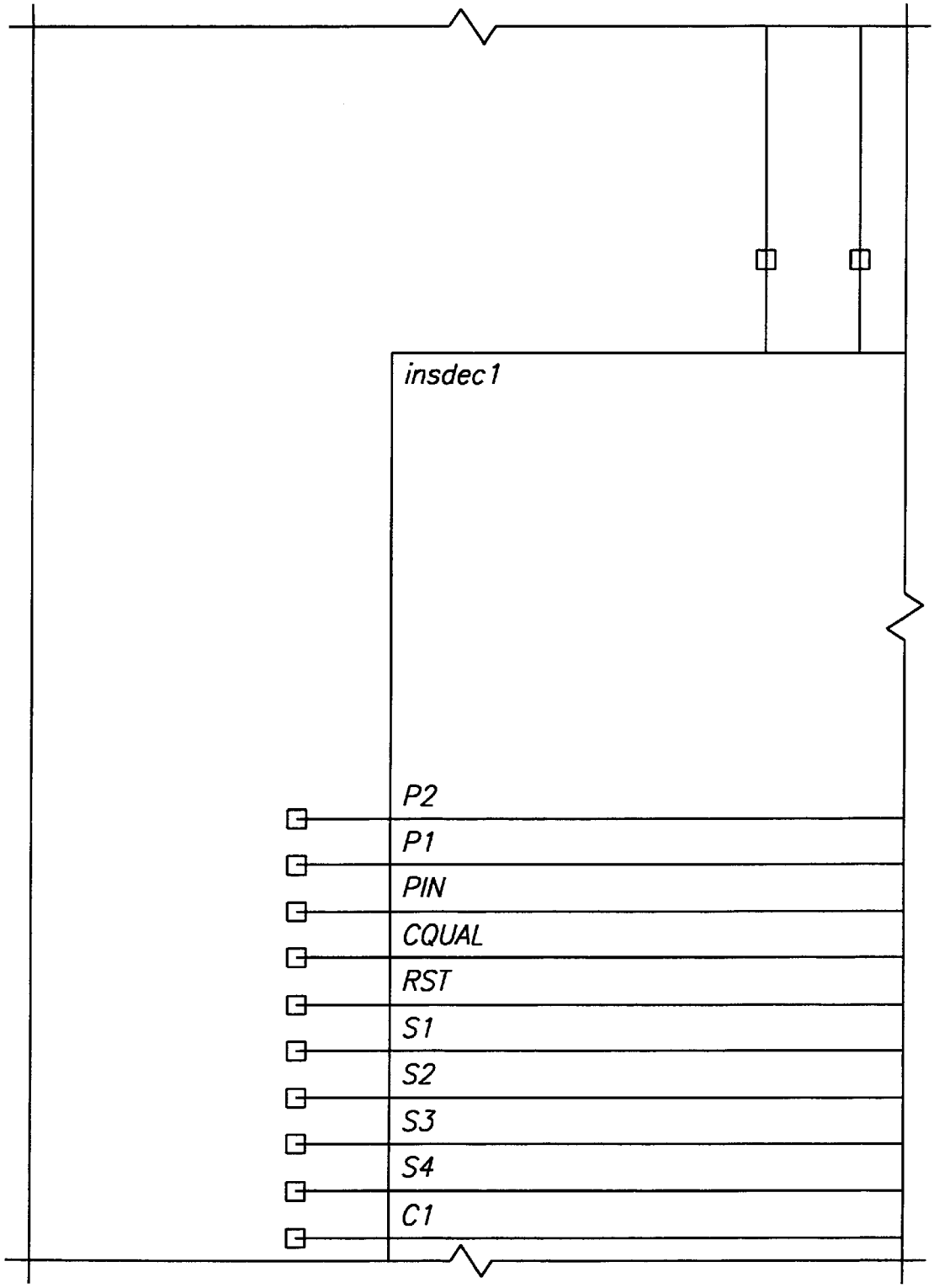


Fig 1.0688

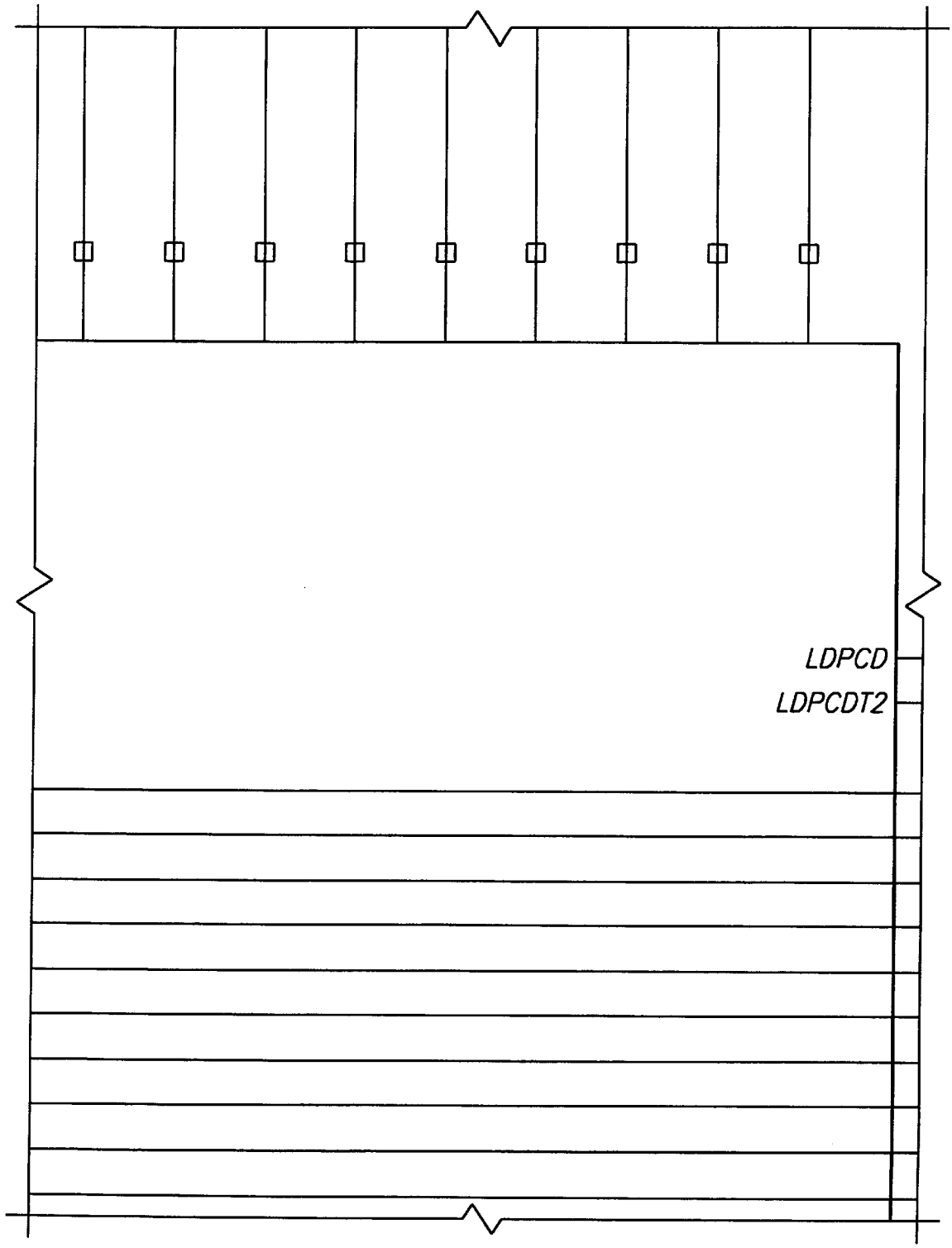


Fig 1.06BC

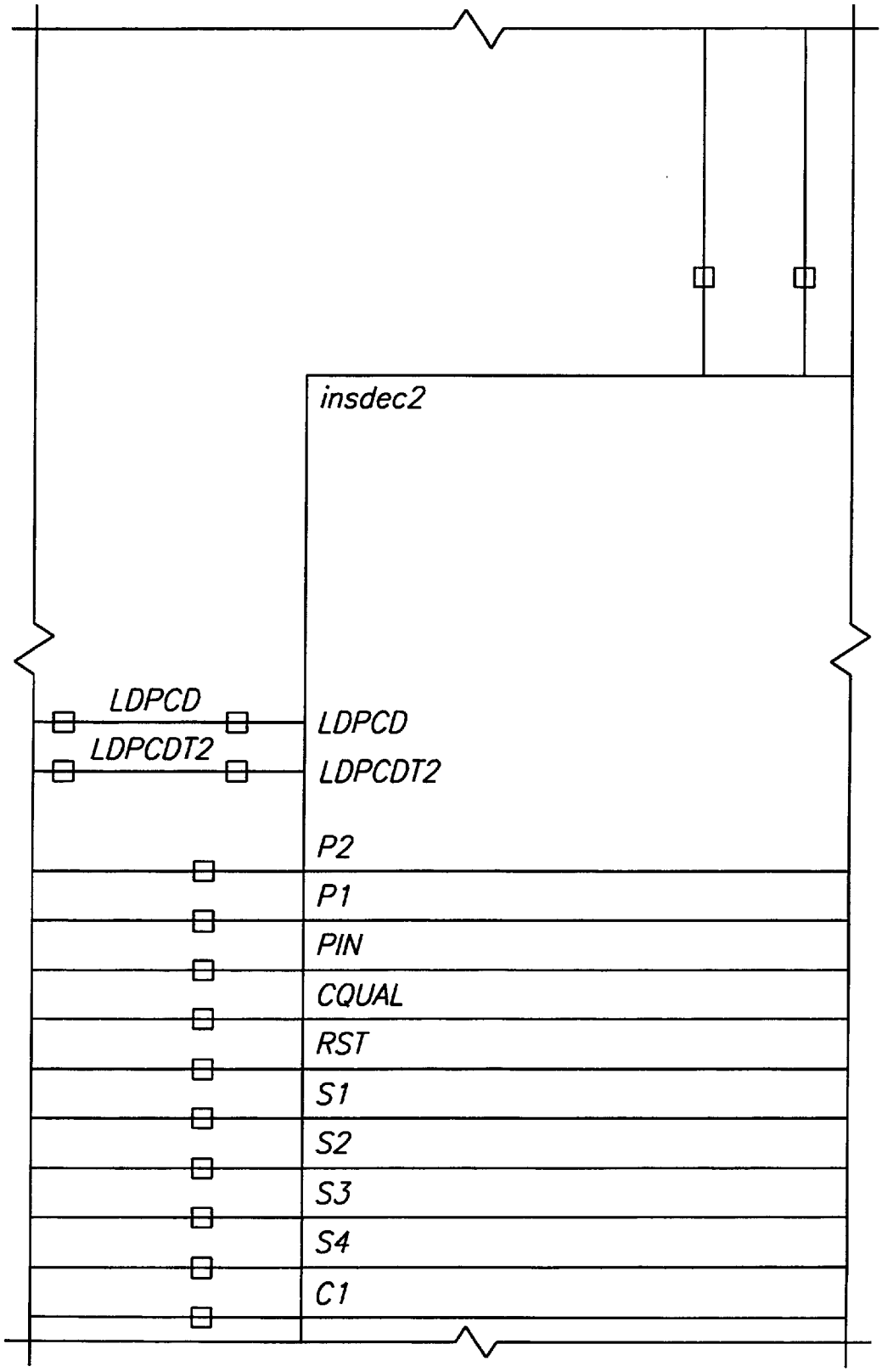

insdec2
LDPCD
LDPCDT2
LDPCD
LDPCDT2
P2
P1
PIN
CQUAL
RST
S1
S2
S3
S4
C1

Fig 1.0680

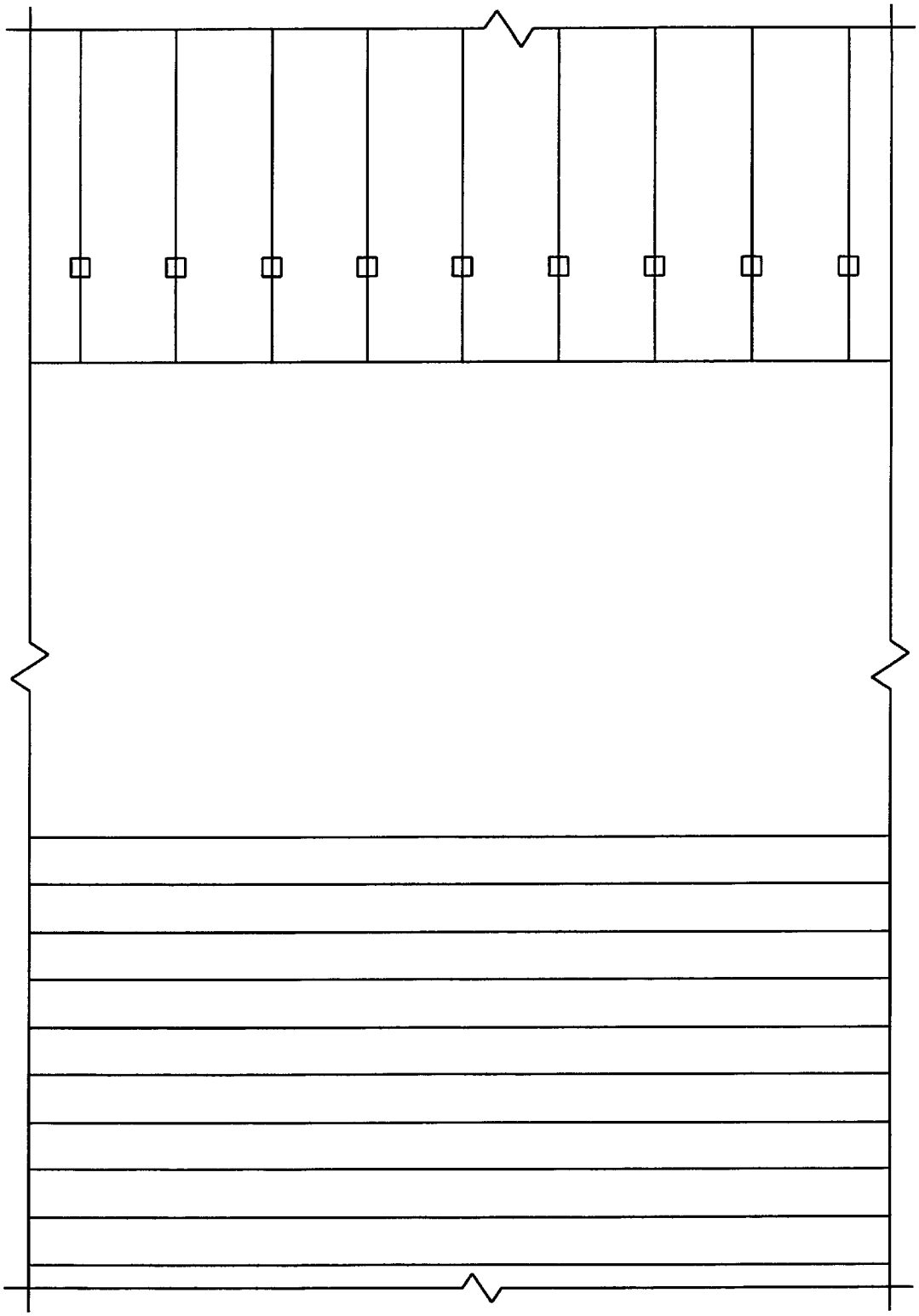


Fig 1.06BE

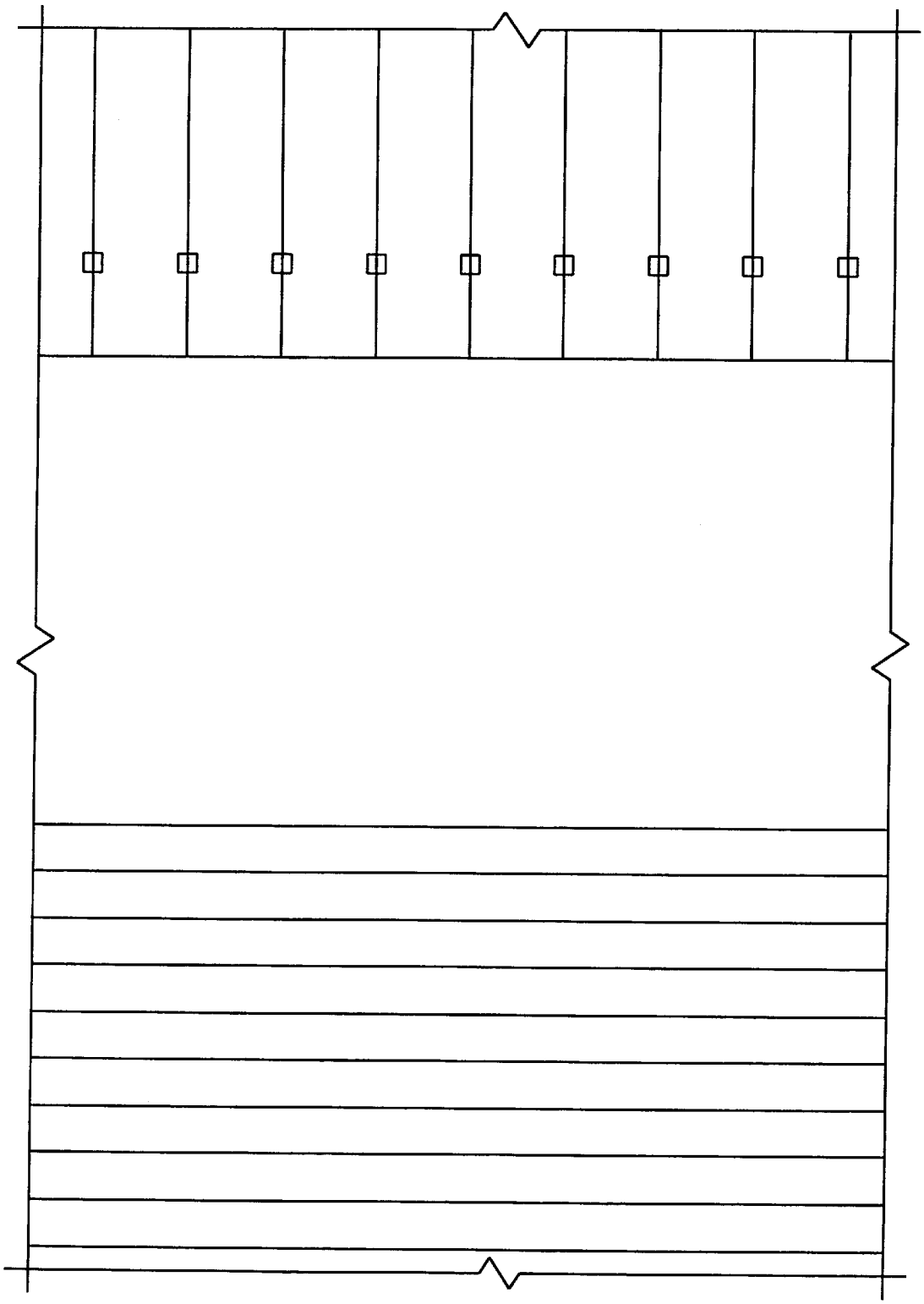


Fig 1.06BF

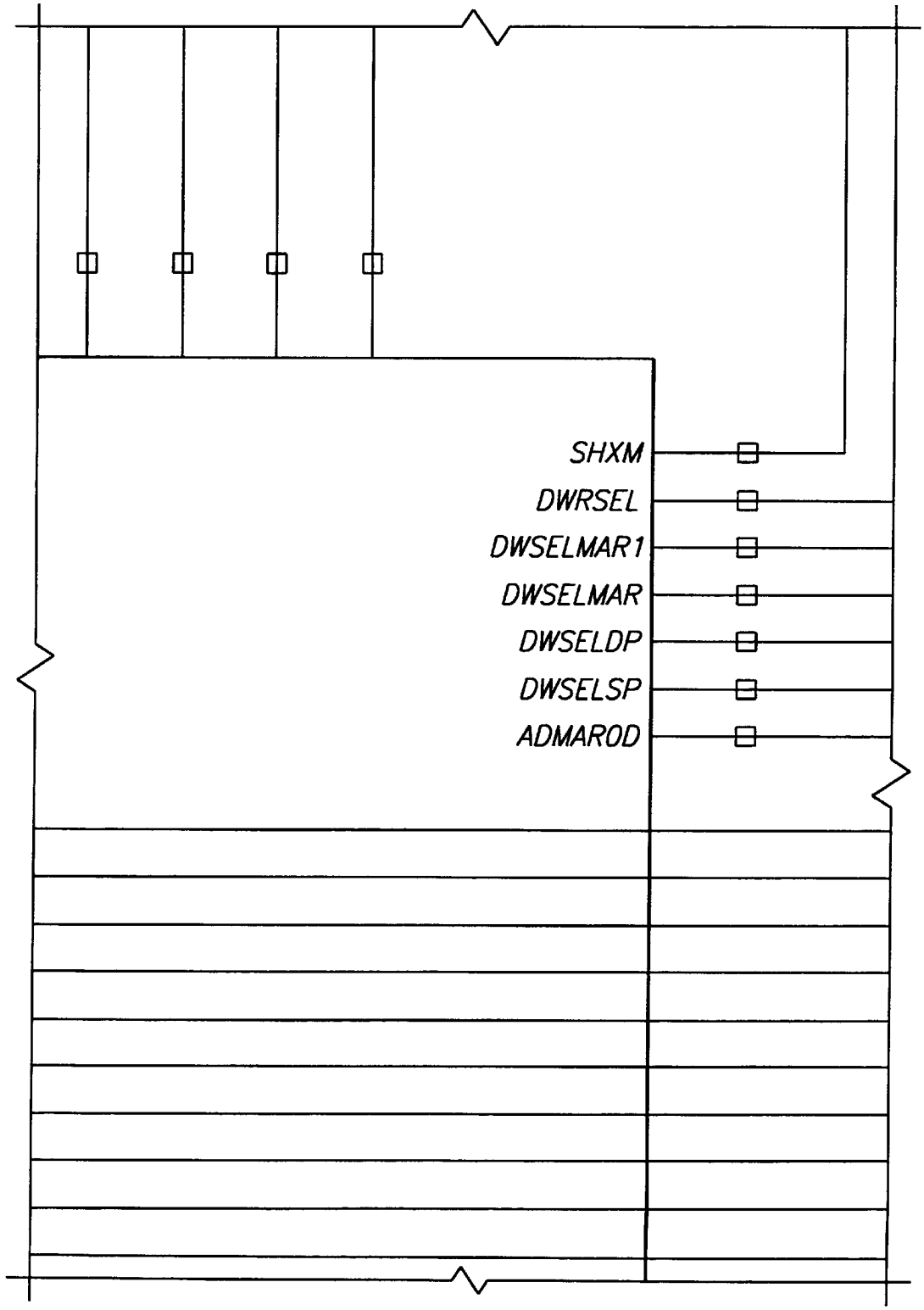


Fig 1.0686

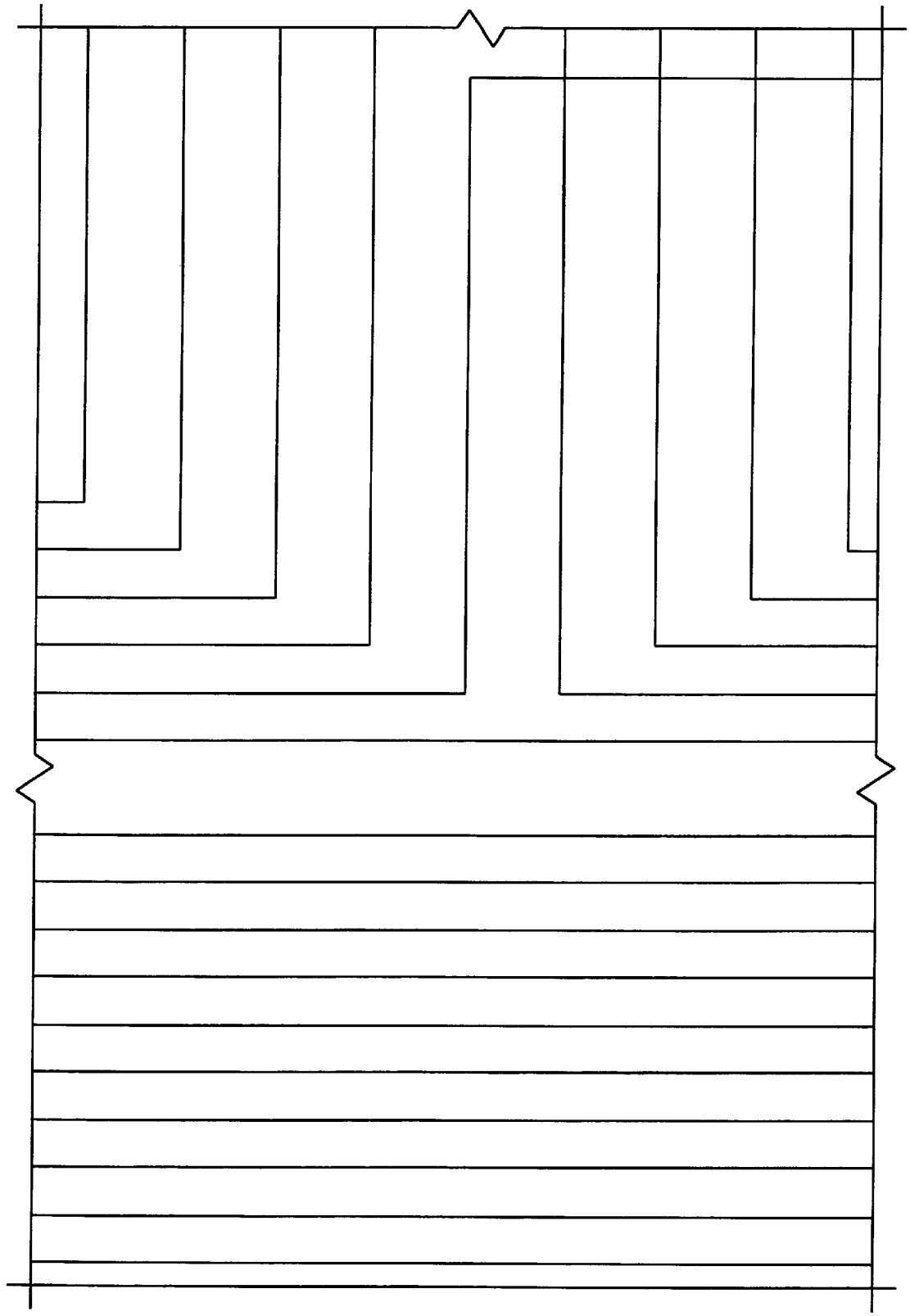
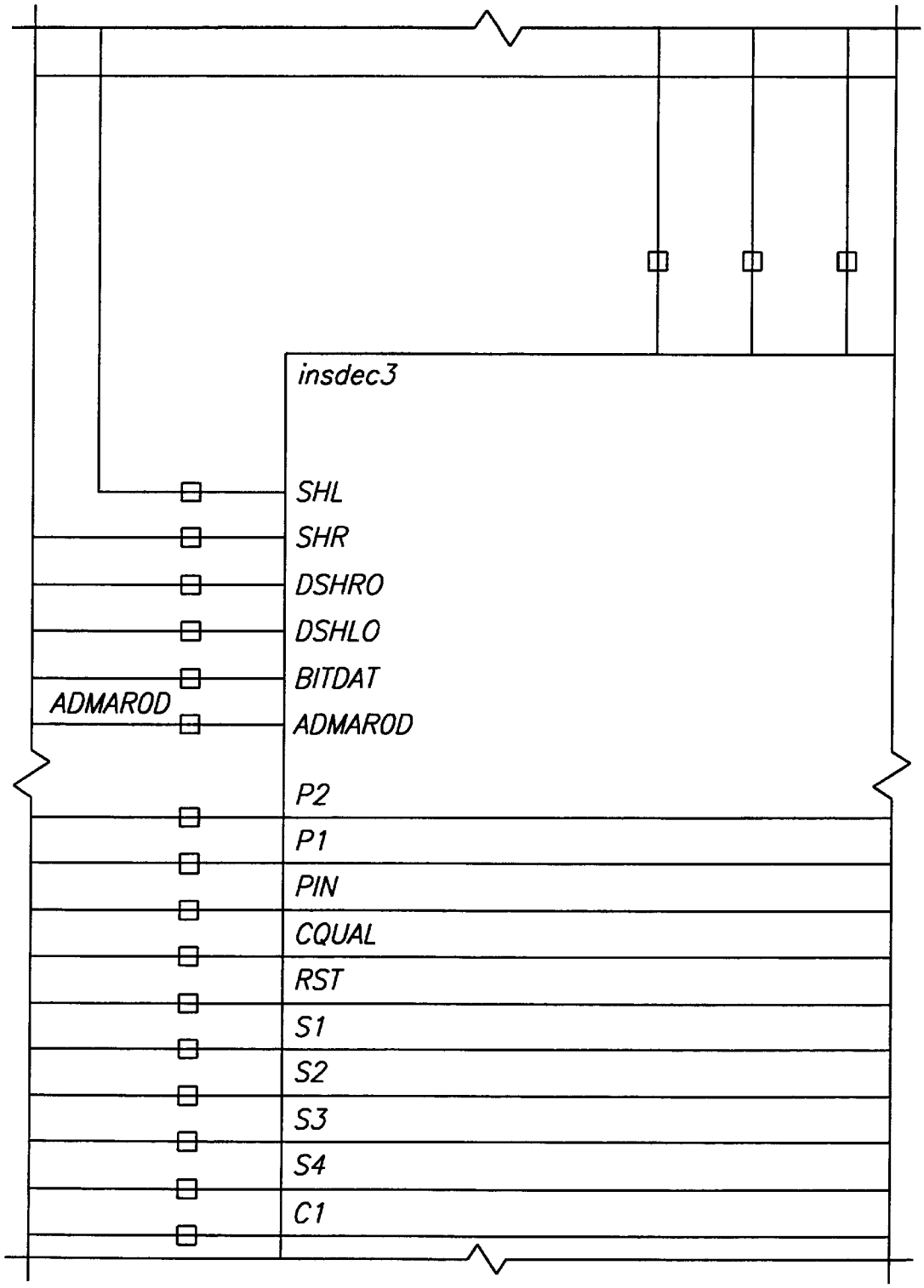


Fig 7.06BH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SHR
DSHRO
DSHLO
BITDAT
ADMAROD
ADMAROD
P2
P1
PIN
CQUAL
RST
S1
S2
S3
S4
C1

Fig 1.06B1

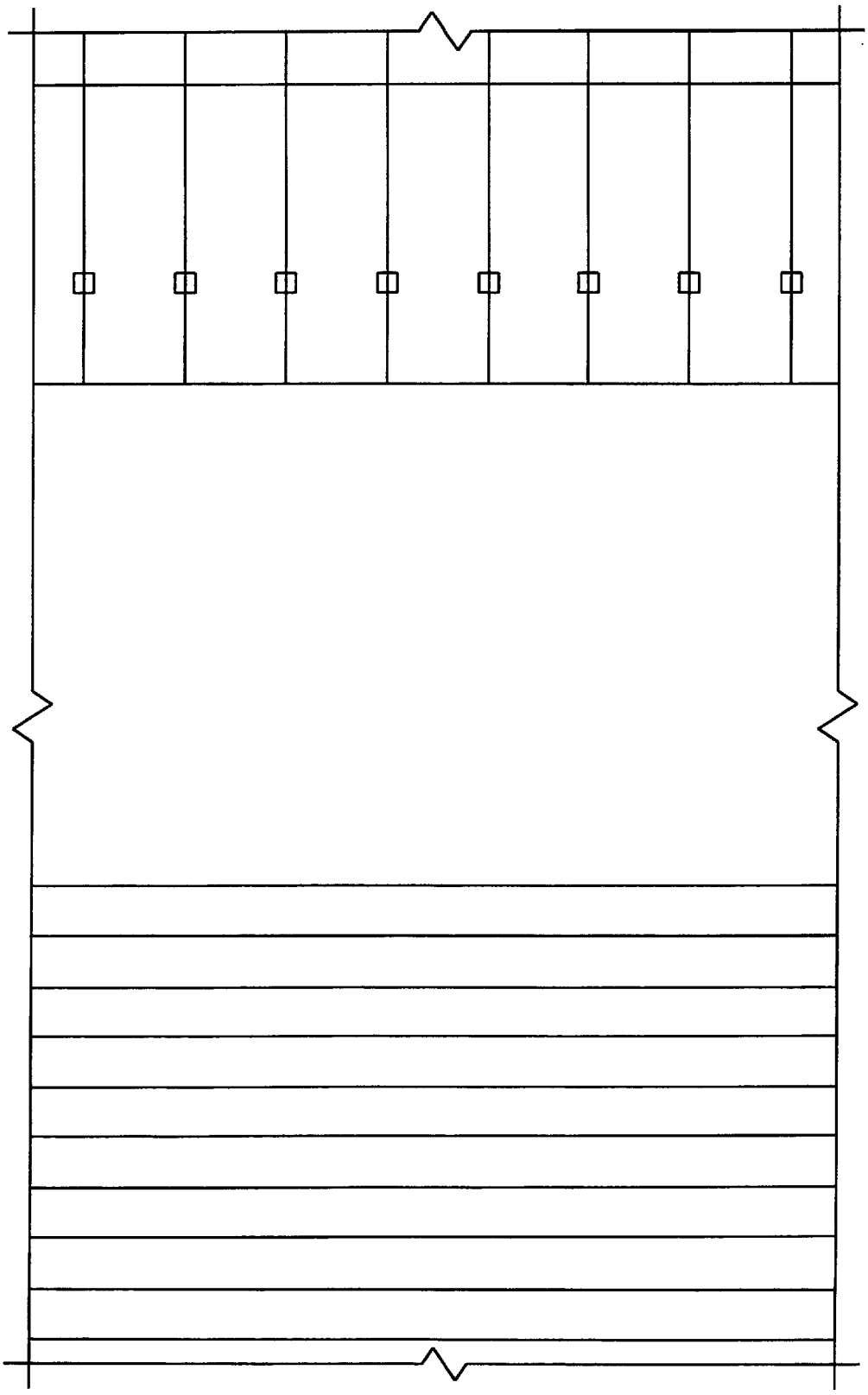
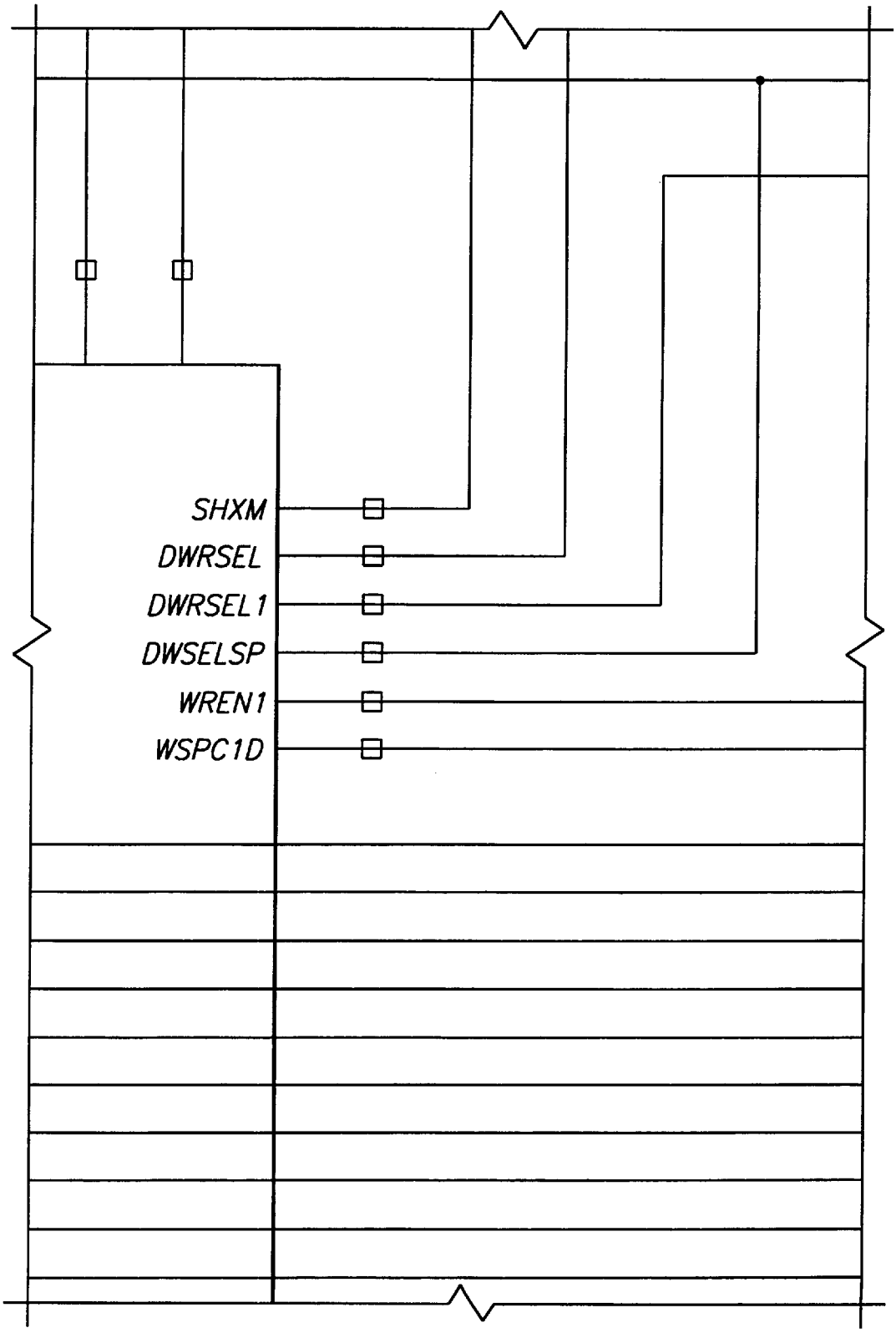


Fig 1.0680J



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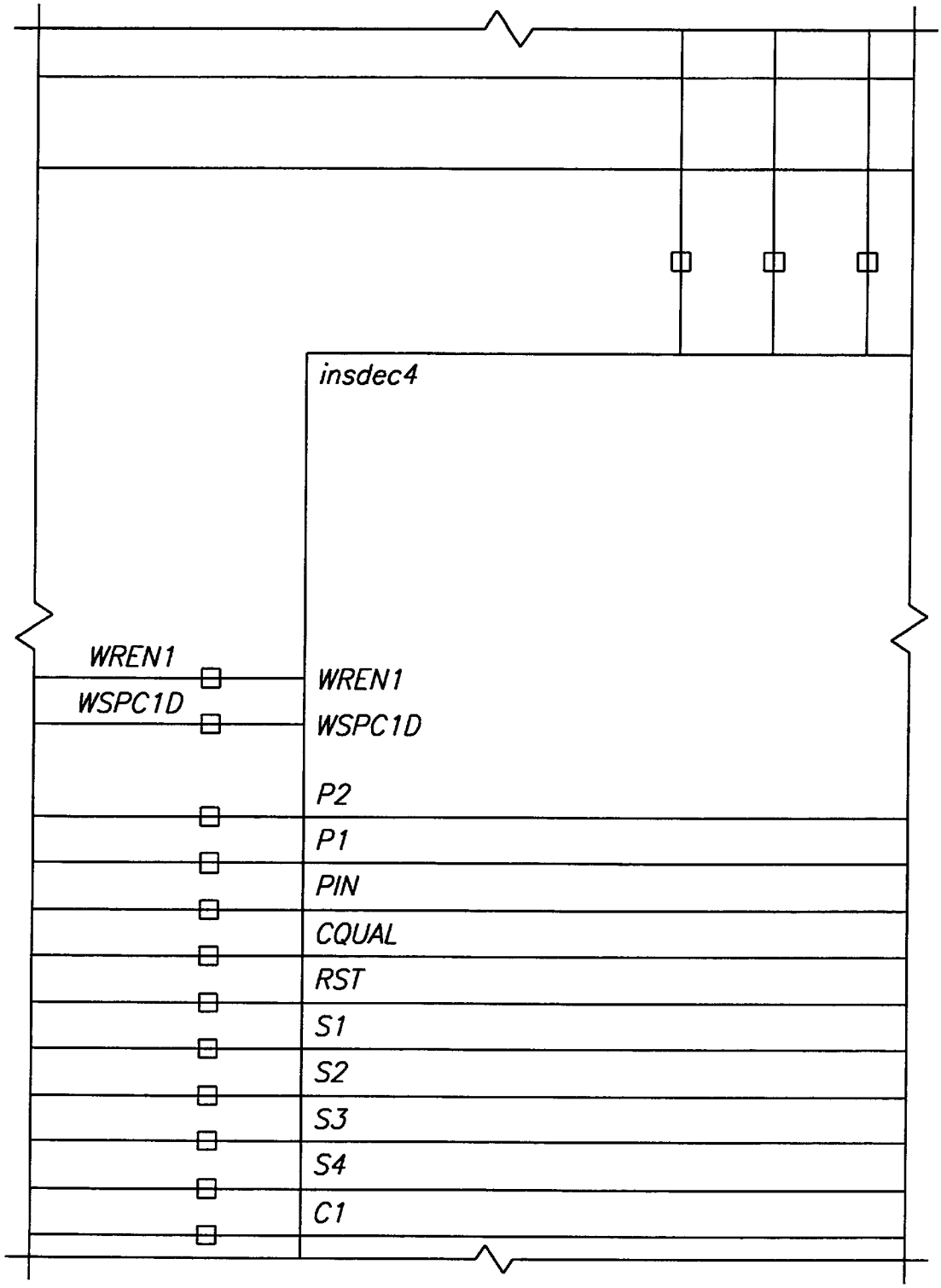
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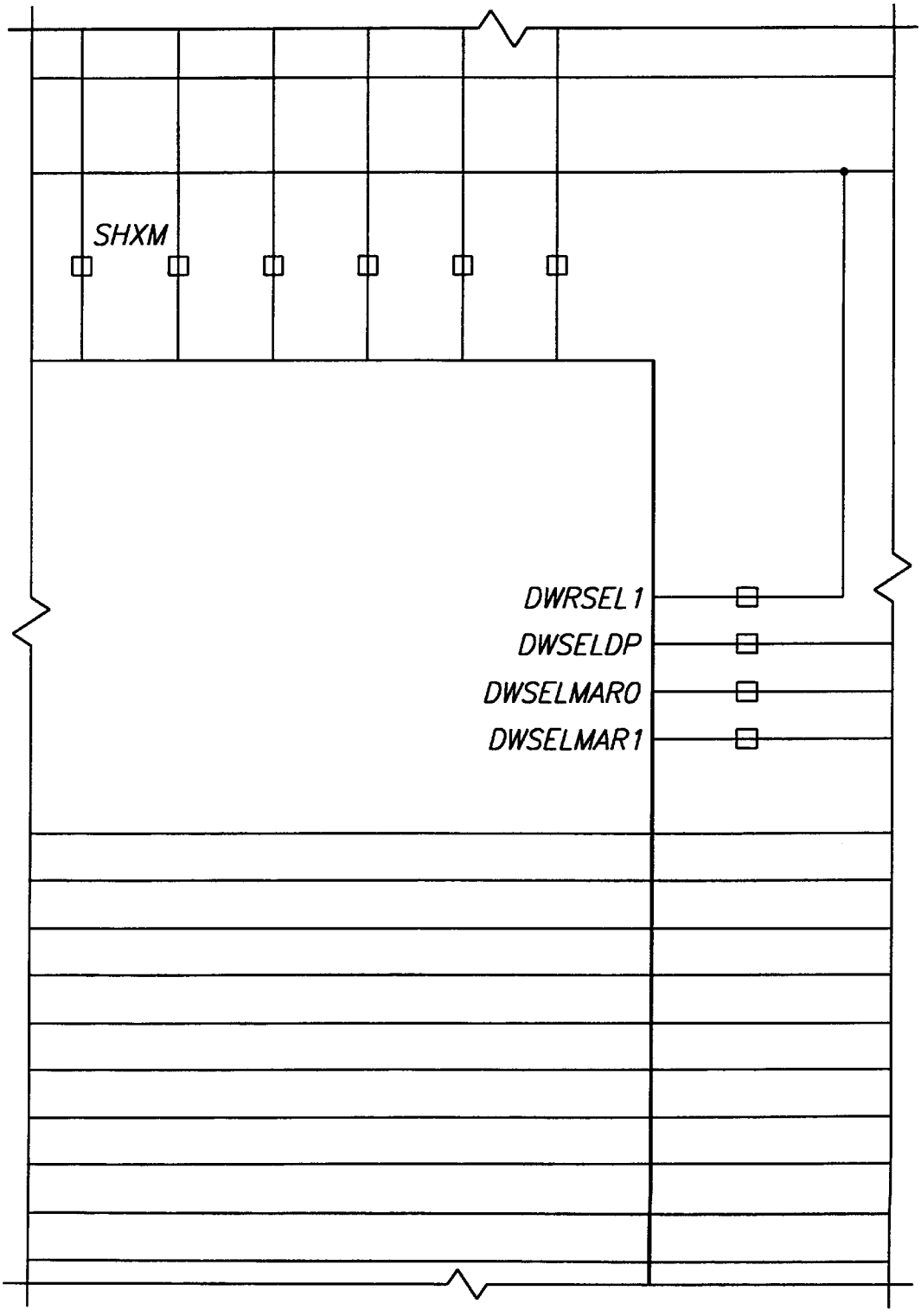
PIN
CQUAL
RST
S1
S2
S3
S4
C1

Fig 1.06BL



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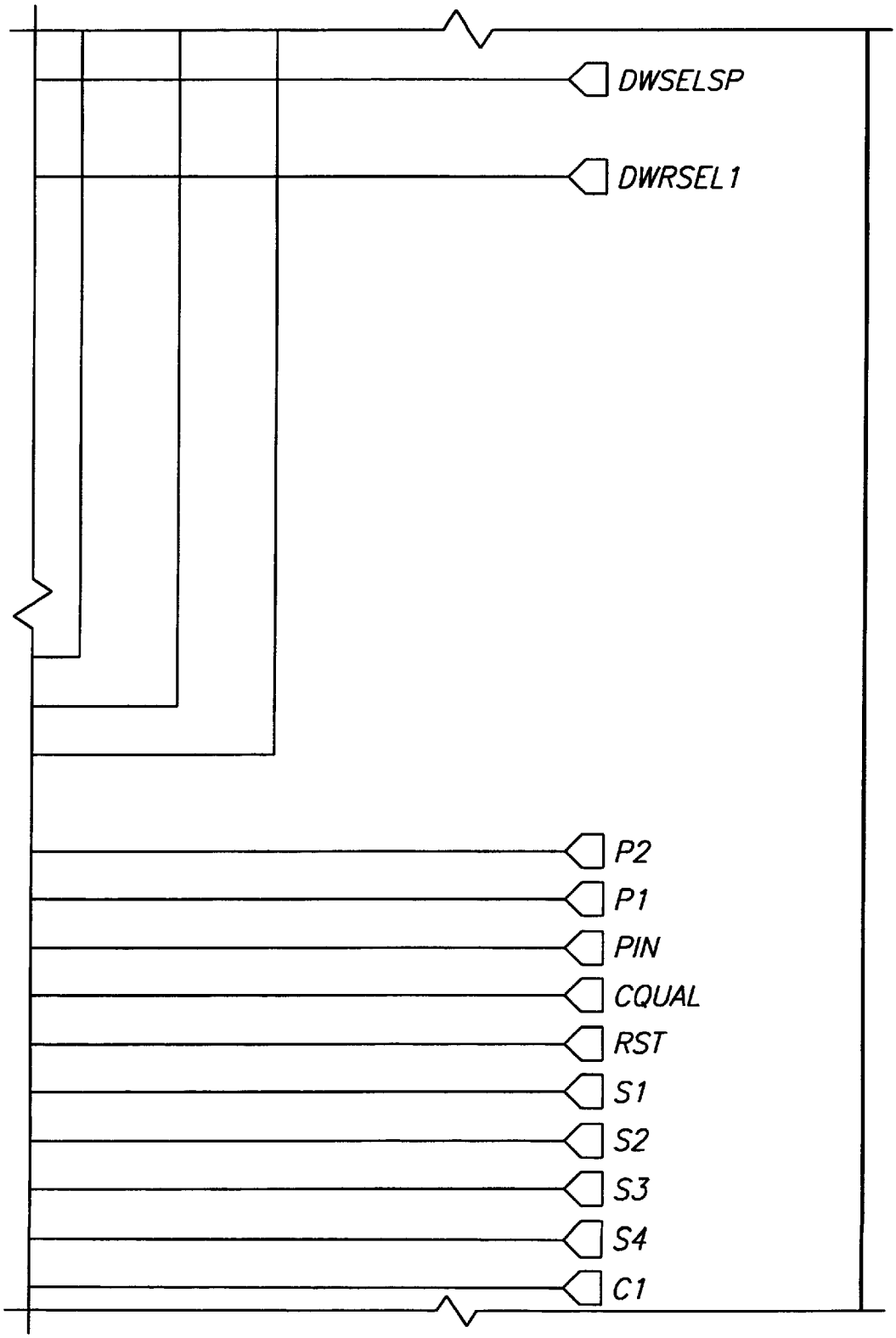
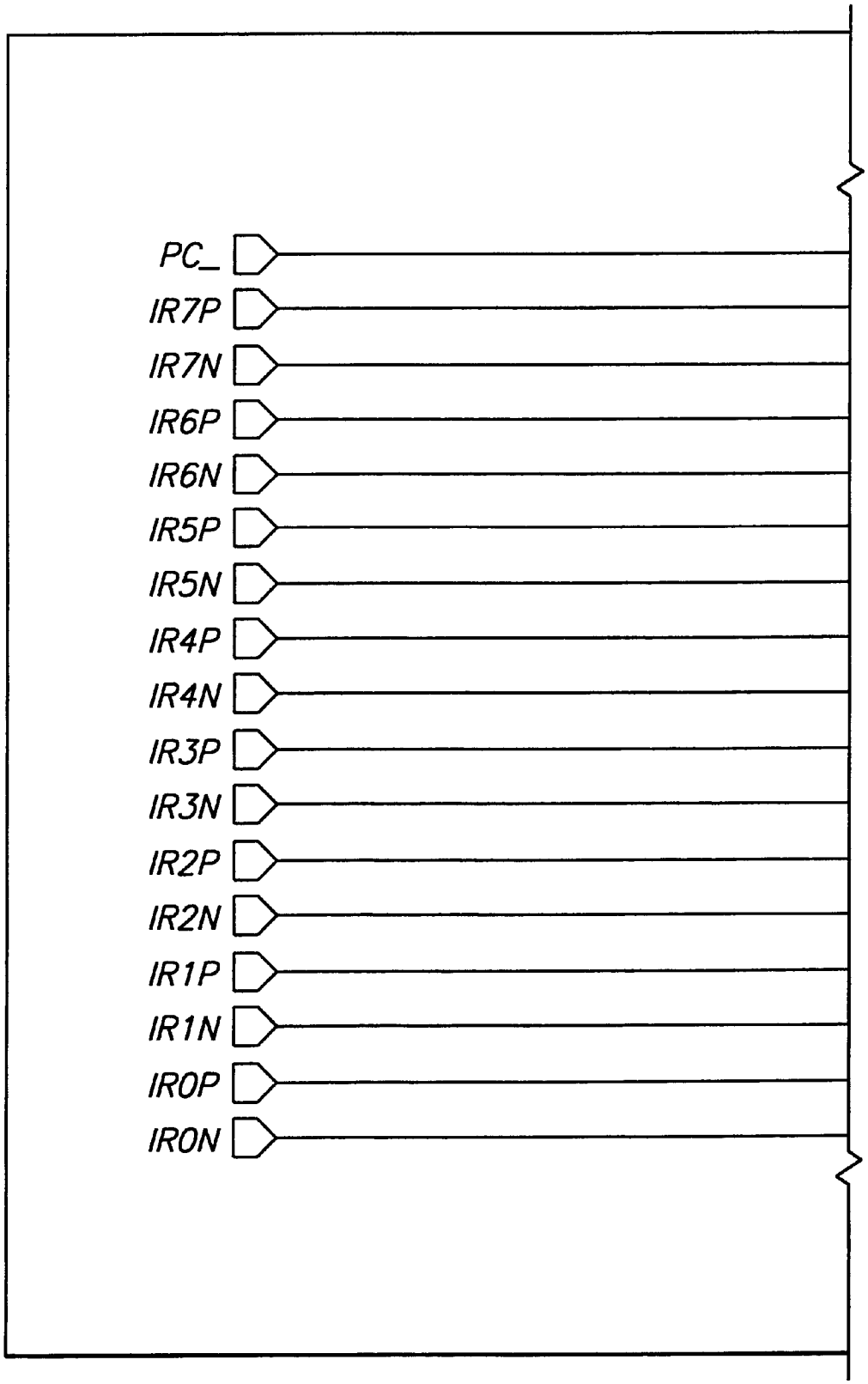


FIG 1.06BN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IR5P
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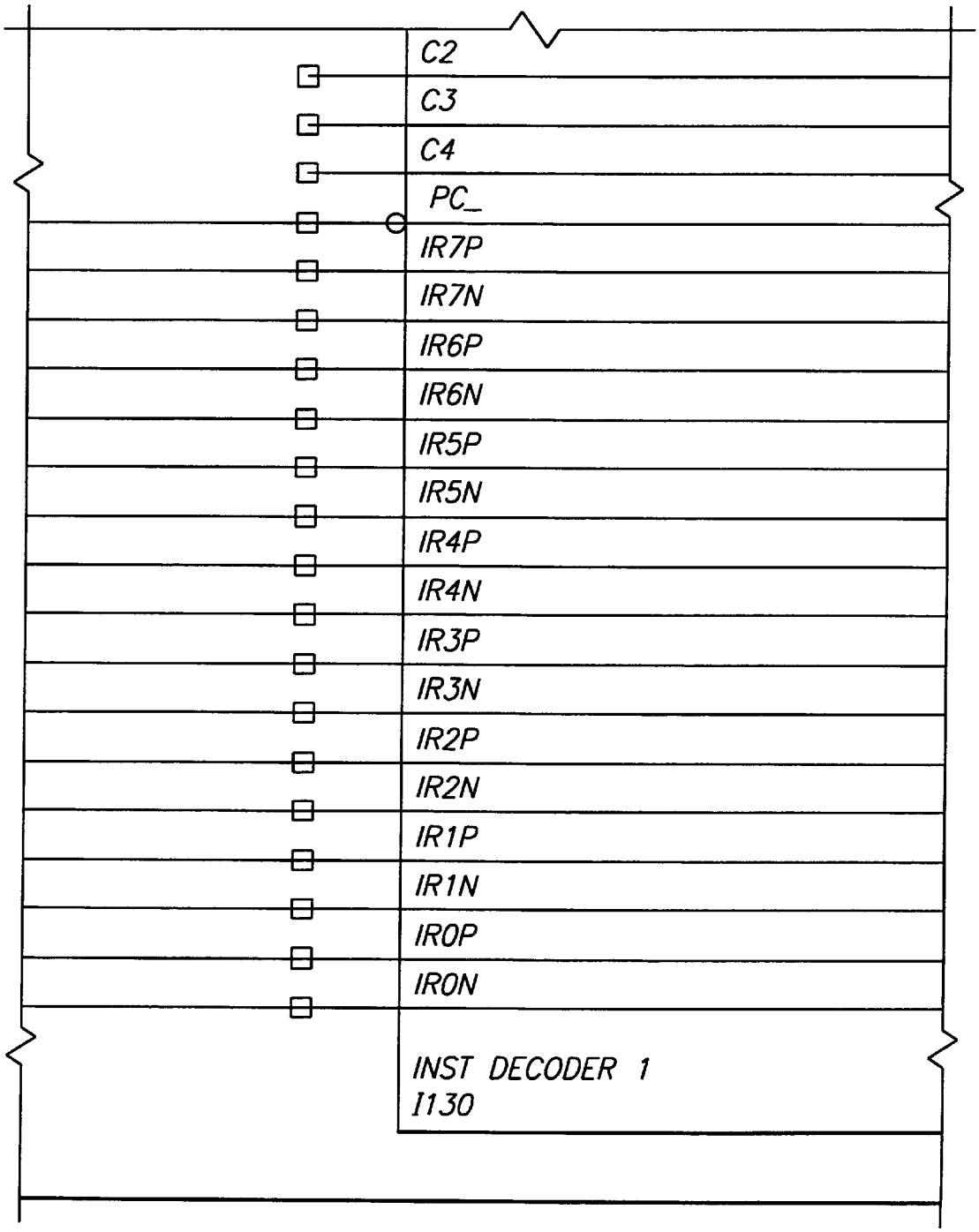
IR0N

Fig 1.06CA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C3
C4
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IR5P
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IR4P
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INST DECODER 1
I130

Fig 7.065CB

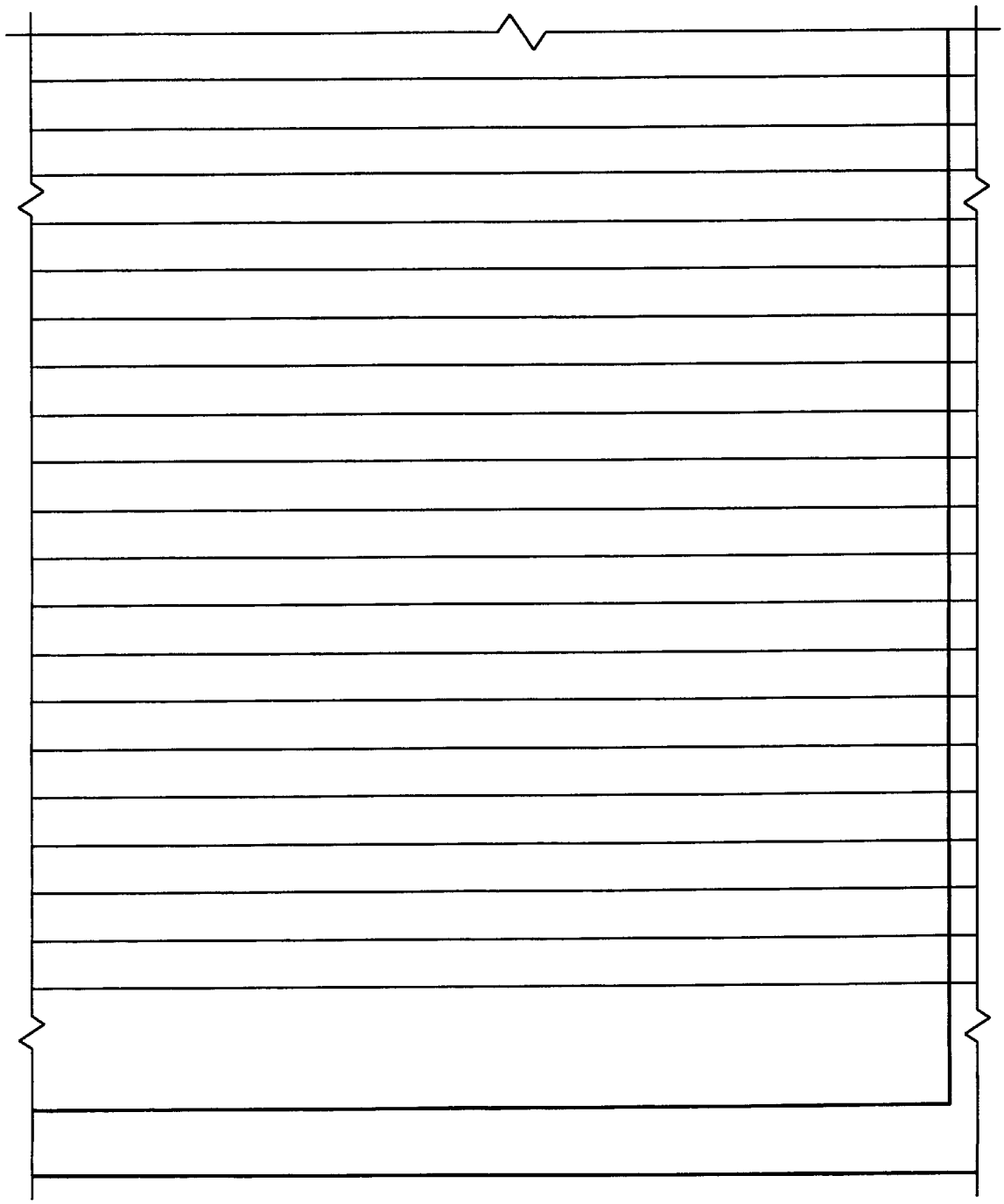
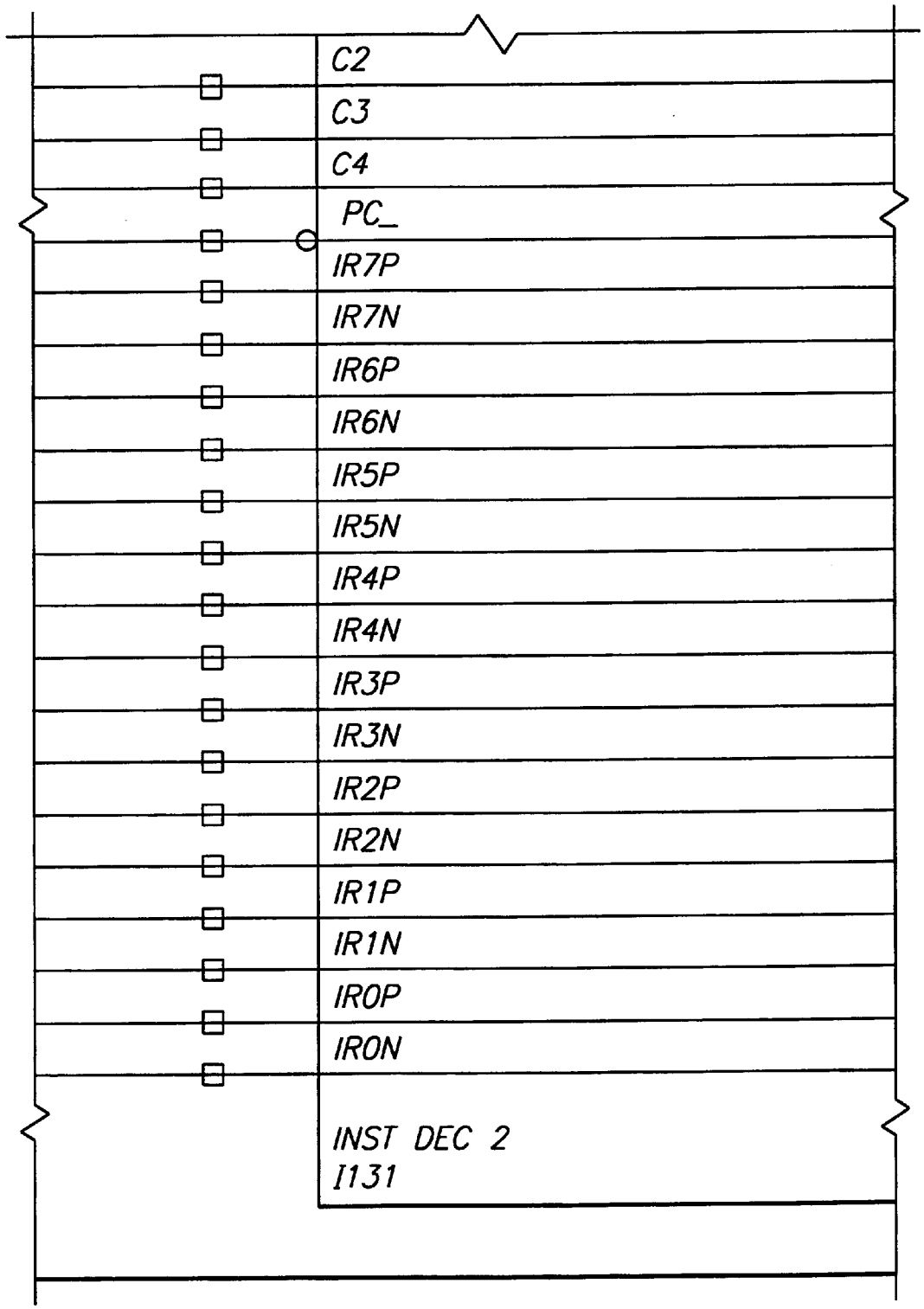


Fig 1.06CC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C3
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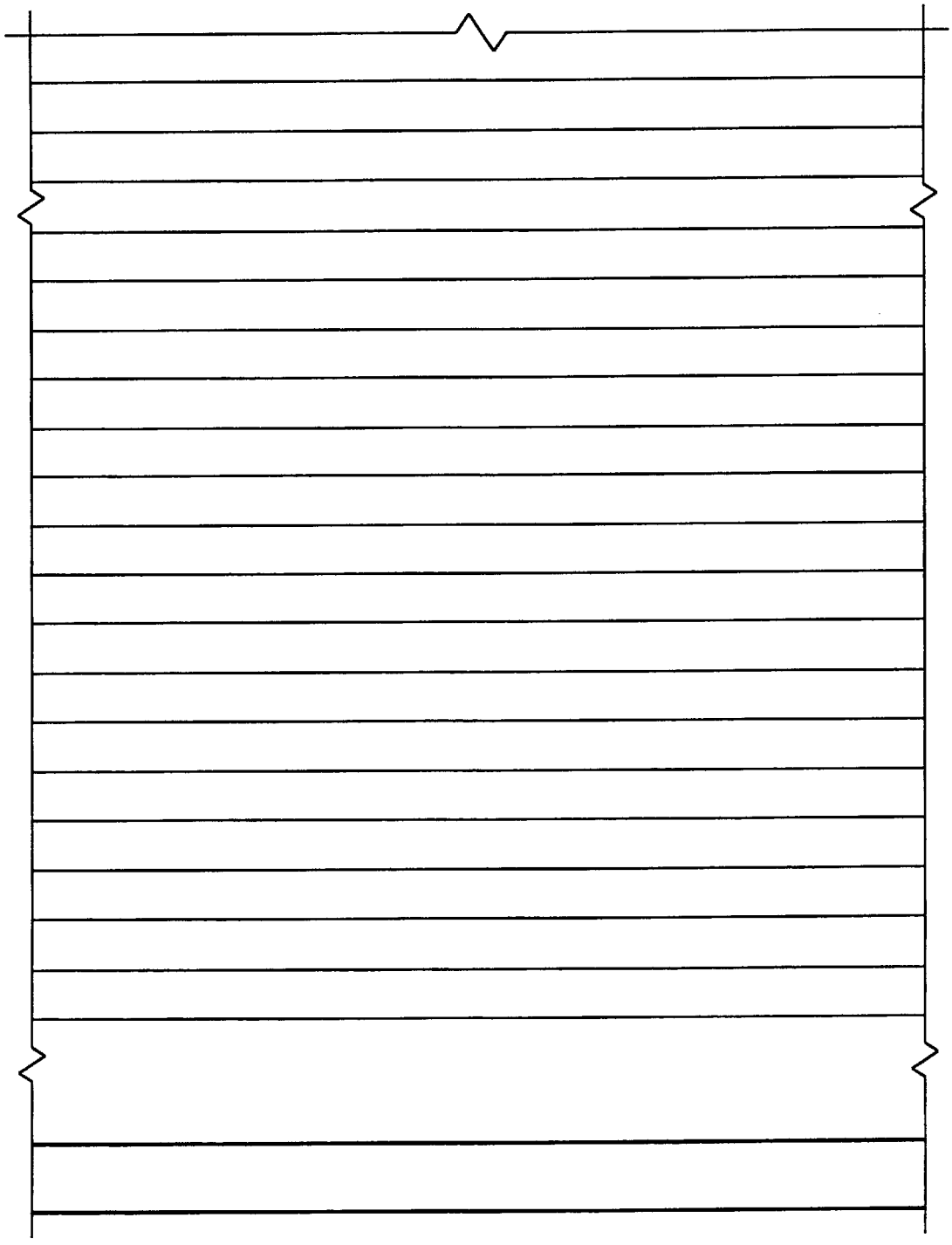
INST DEC 2
I131

Fig 1.06CD



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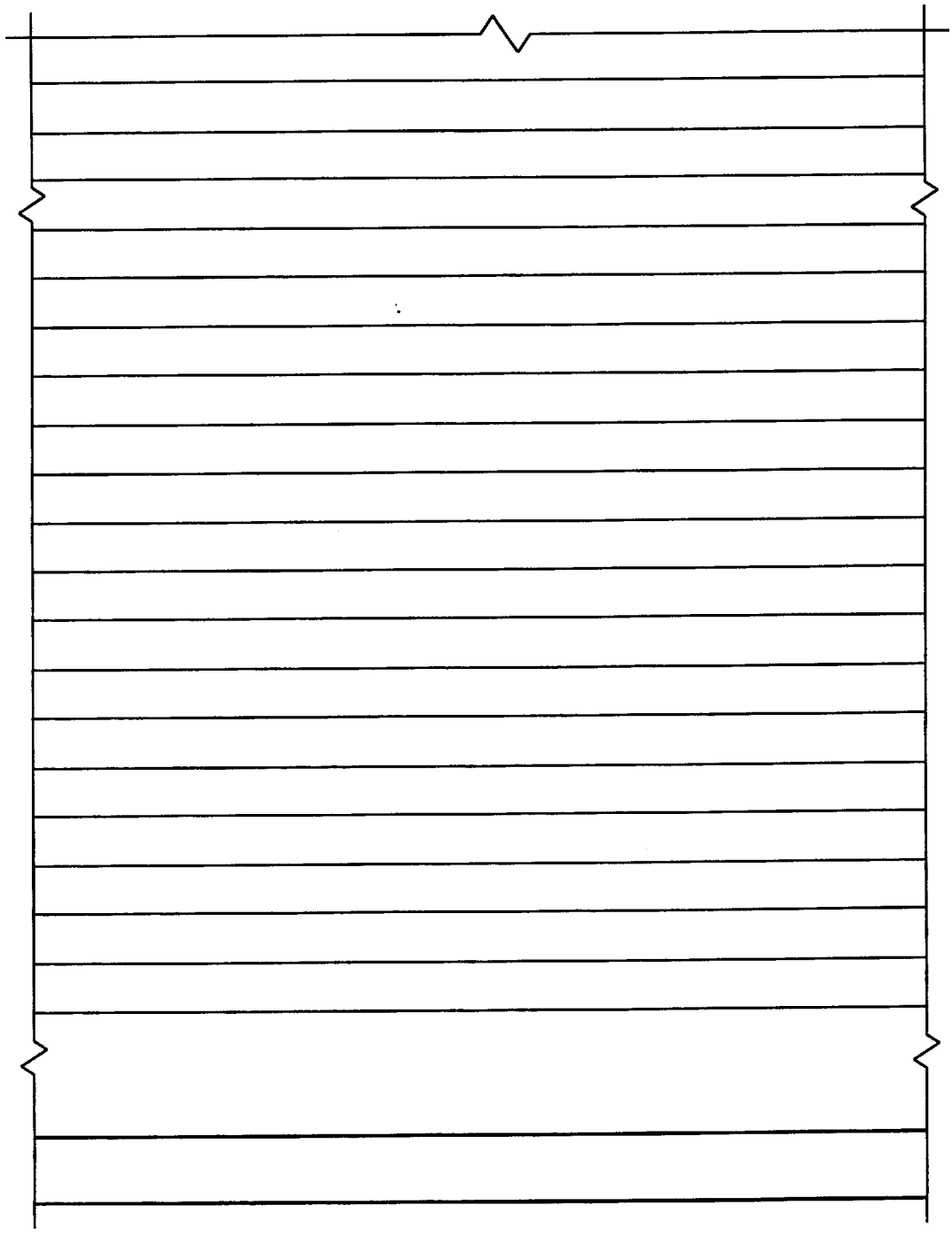
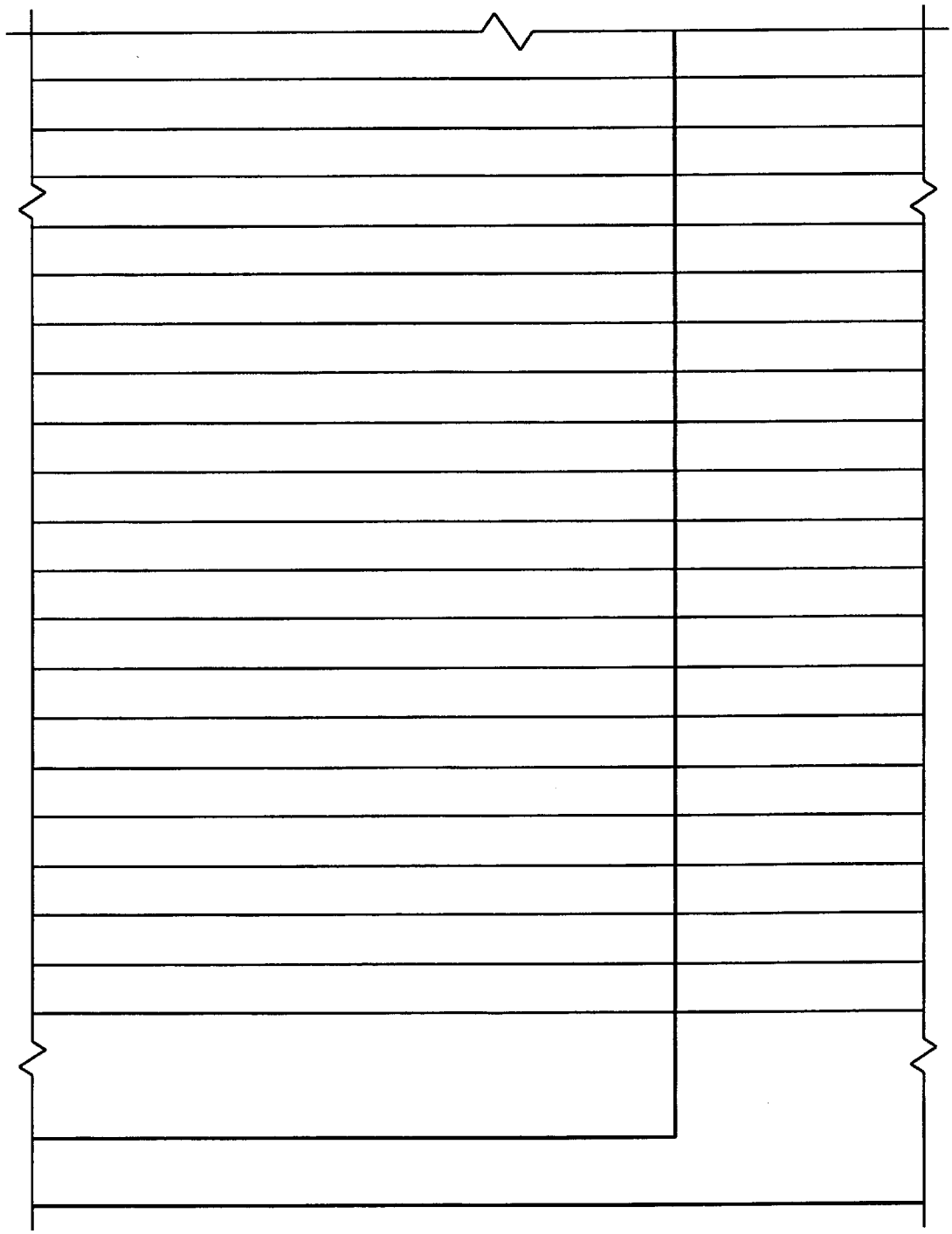


Fig 7.06CF



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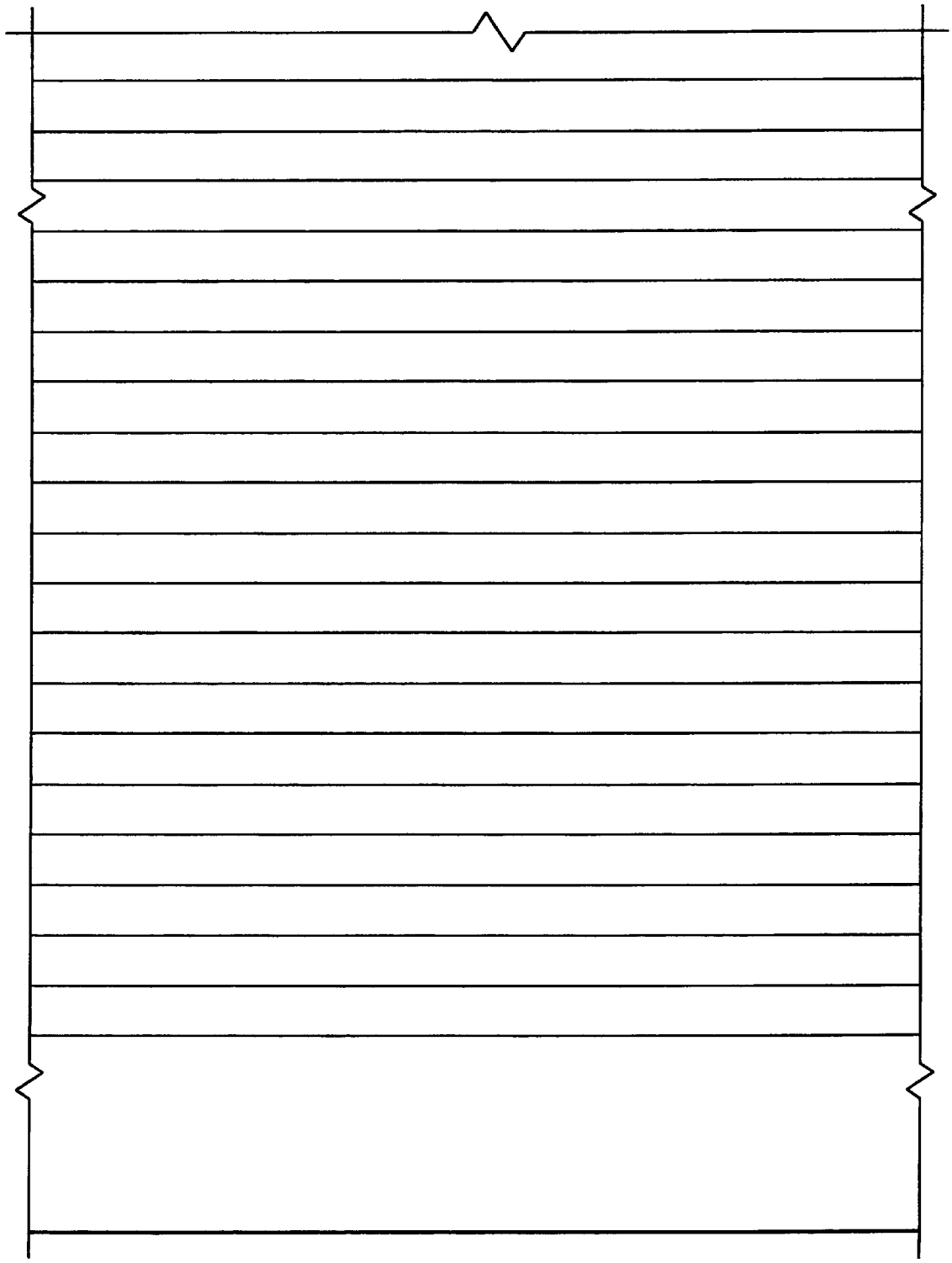

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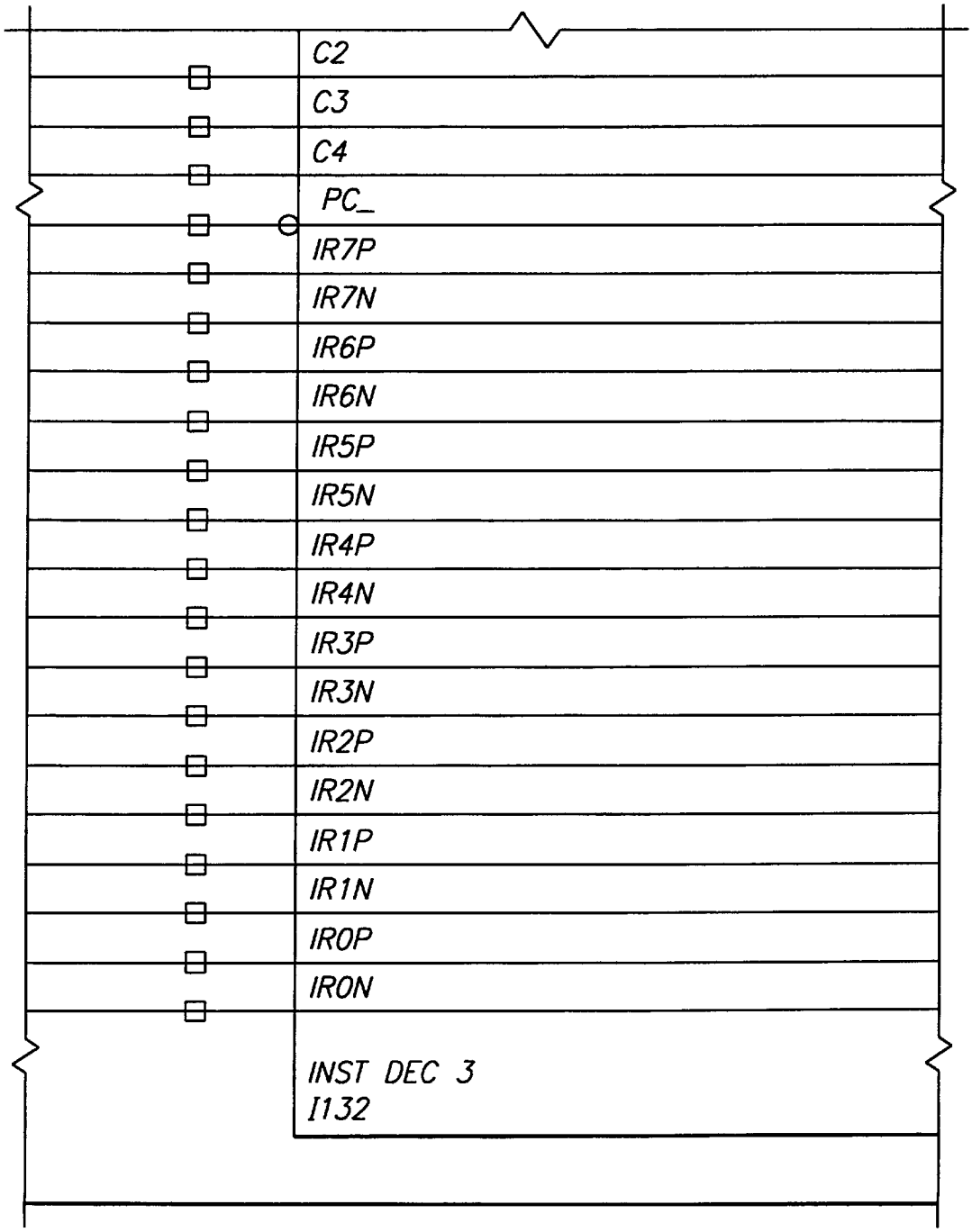
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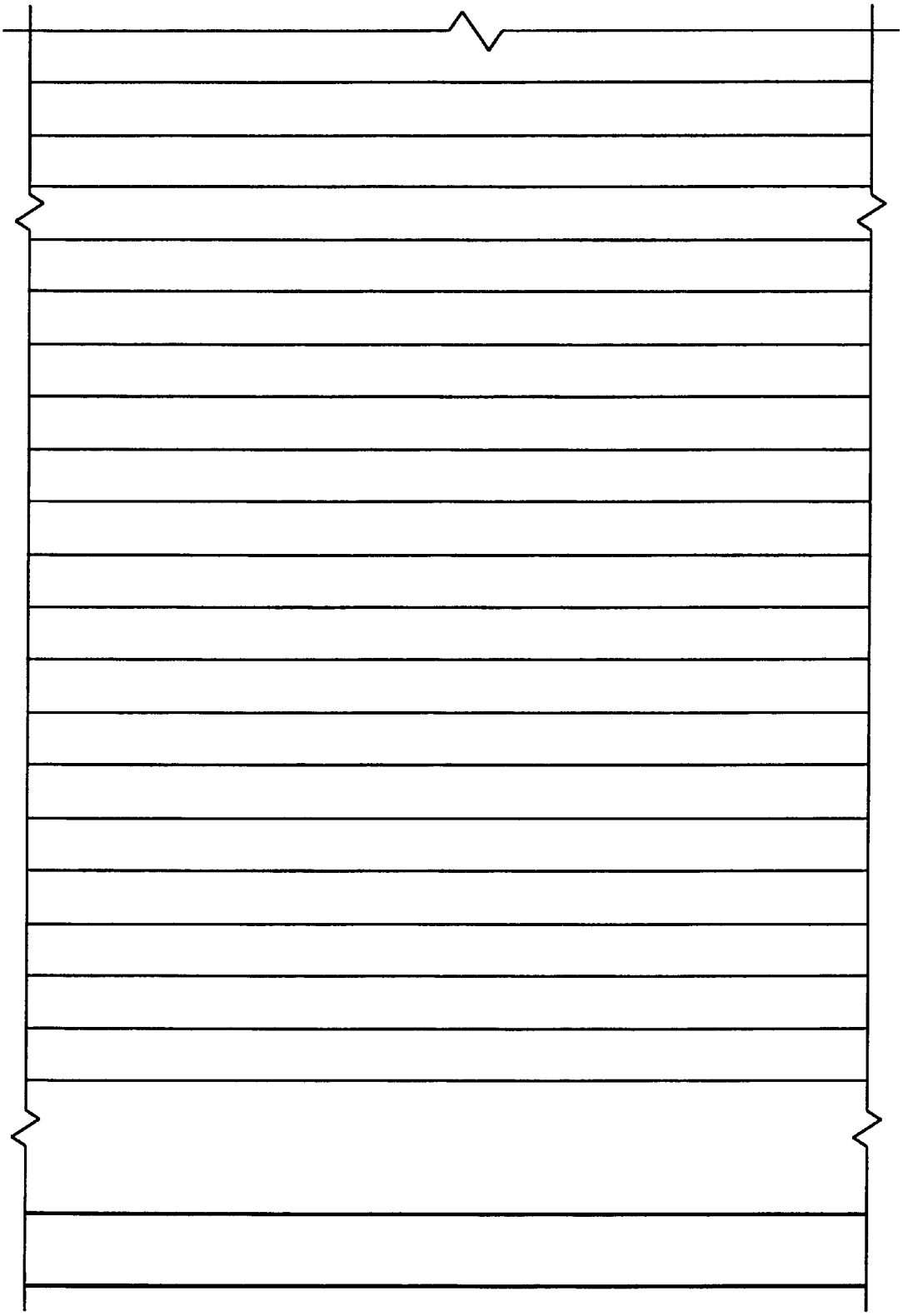
INST DEC 3
I132

Fig 1.066II



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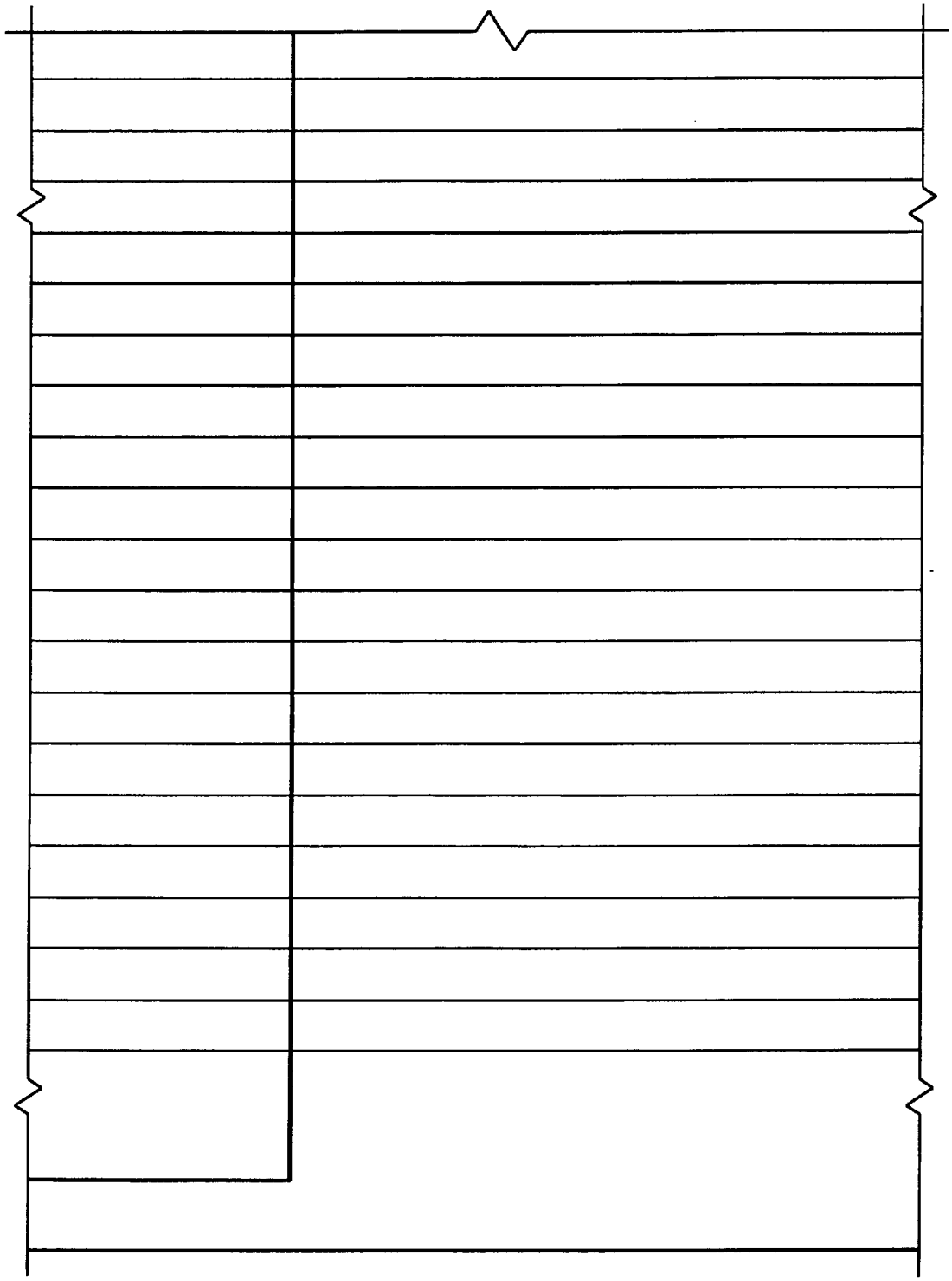

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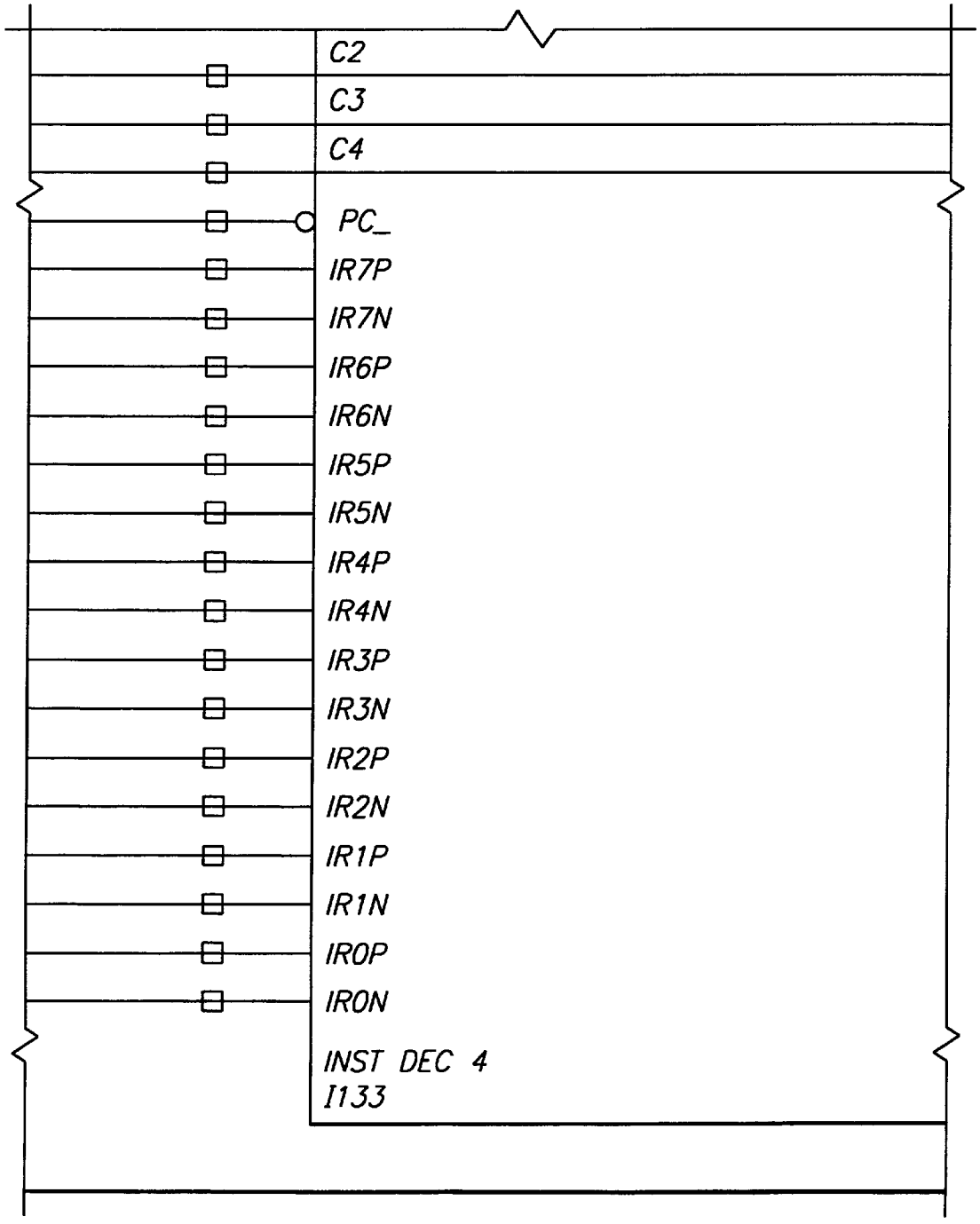
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IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
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IR1P
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IR0P
IR0N
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I133

Fig 1.066L

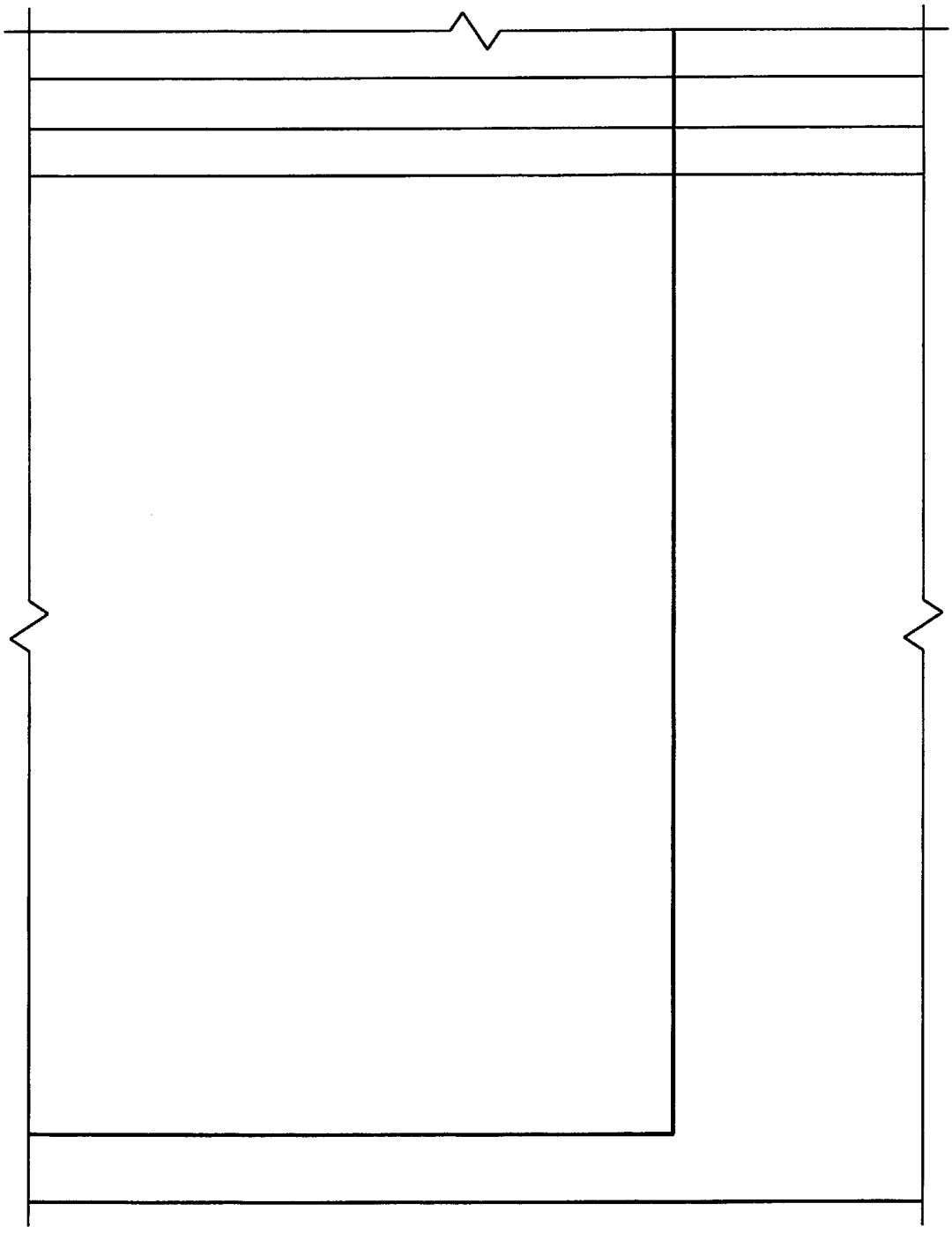


Fig 1.06CM

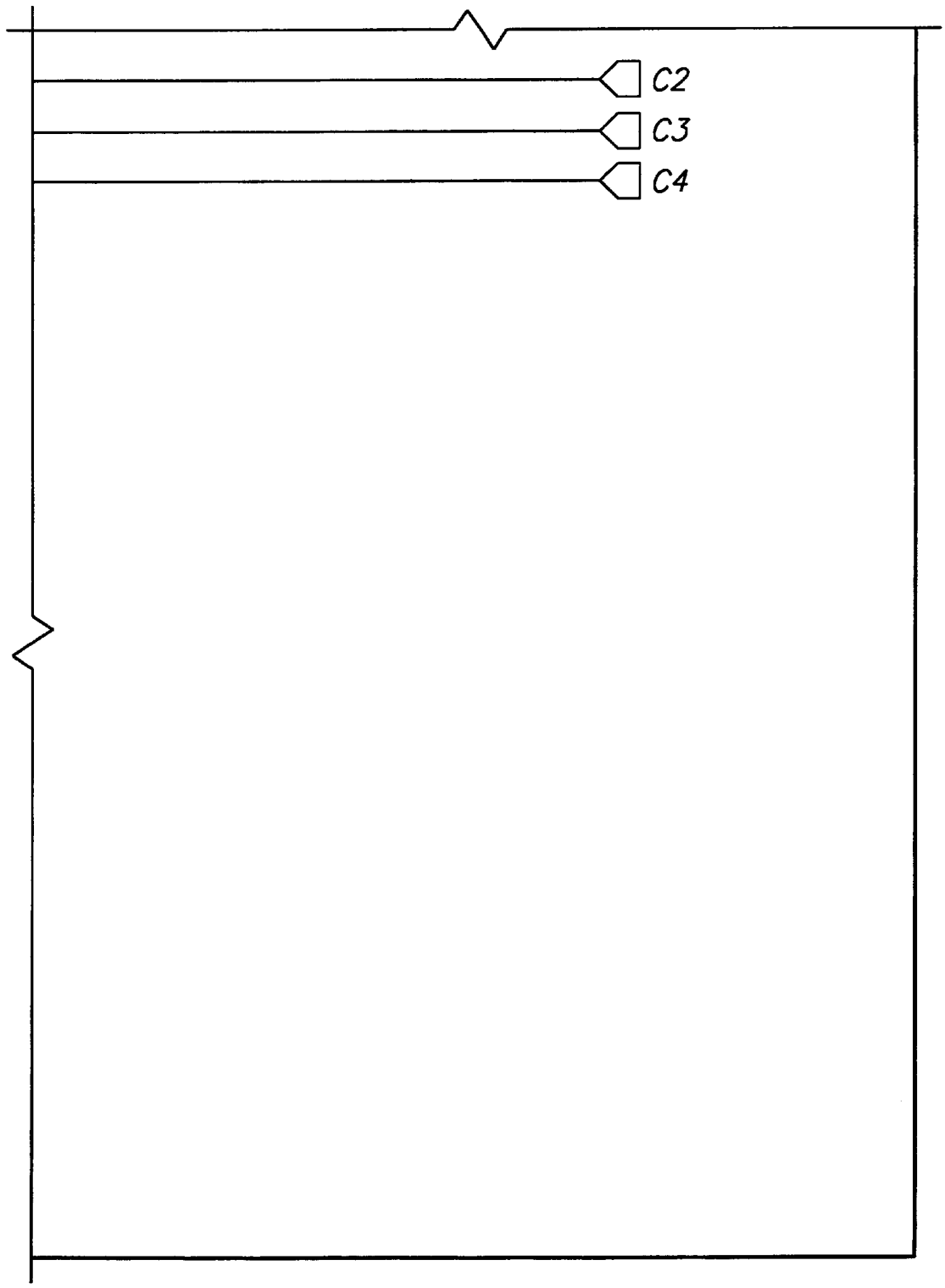


Fig 1.06CN

7.0601AA	7.0601AB	7.0601AC	7.0601AD	7.0601AE	7.0601AF	7.0601AG	7.0601AH	7.0601AI
7.0601BA	7.0601BB	7.0601BC	7.0601BD	7.0601BE	7.0601BF	7.0601BG	7.0601BH	7.0601BI
7.0601CA	7.0601CB	7.0601CC	7.0601CD	7.0601CE	7.0601CF	7.0601CG	7.0601CH	7.0601CI
7.0601DA	7.0601DB	7.0601DC	7.0601DD	7.0601DE	7.0601DF	7.0601DG	7.0601DH	7.0601DI
7.0601EA	7.0601EB	7.0601EC	7.0601ED	7.0601EE	7.0601EF	7.0601EG	7.0601EH	7.0601EI
7.0601FA	7.0601FB	7.0601FC	7.0601FD	7.0601FE	7.0601FF	7.0601FG	7.0601FH	7.0601FI
7.0601GA	7.0601GB	7.0601GC	7.0601GD	7.0601GE	7.0601GF	7.0601GG	7.0601GH	7.0601GI
7.0601HA	7.0601HB	7.0601HC	7.0601HD	7.0601HE	7.0601HF	7.0601HG	7.0601HH	7.0601HI

Fig 7.0601

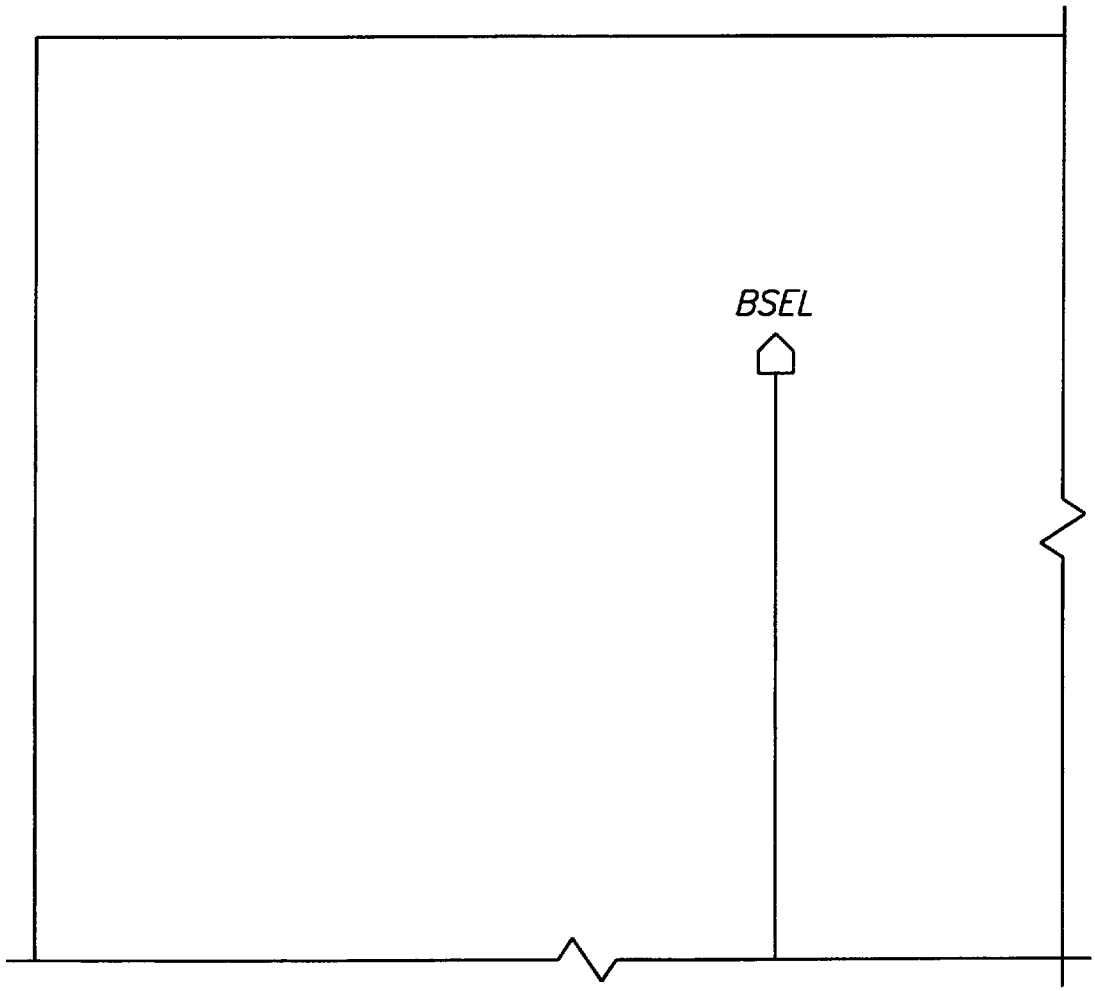


Fig 1.0601AA

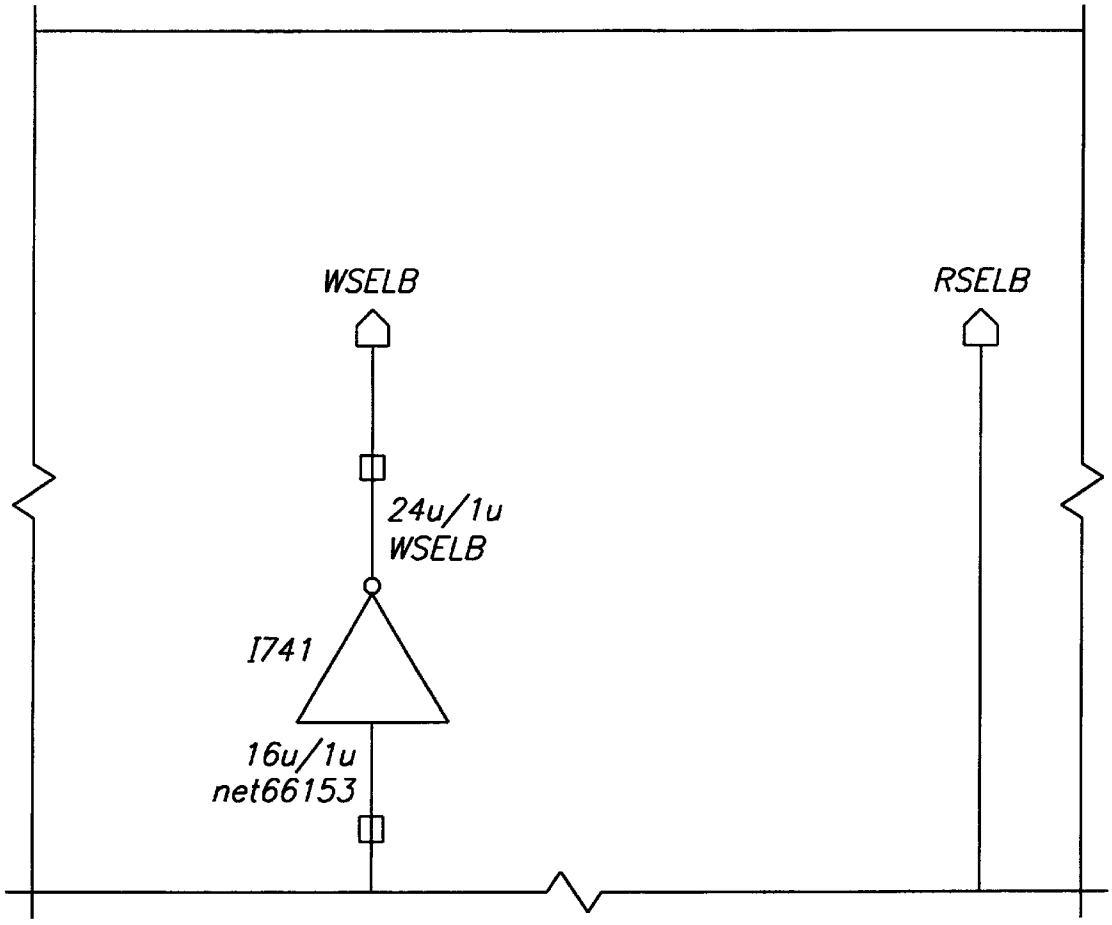


Fig 1.0601AB

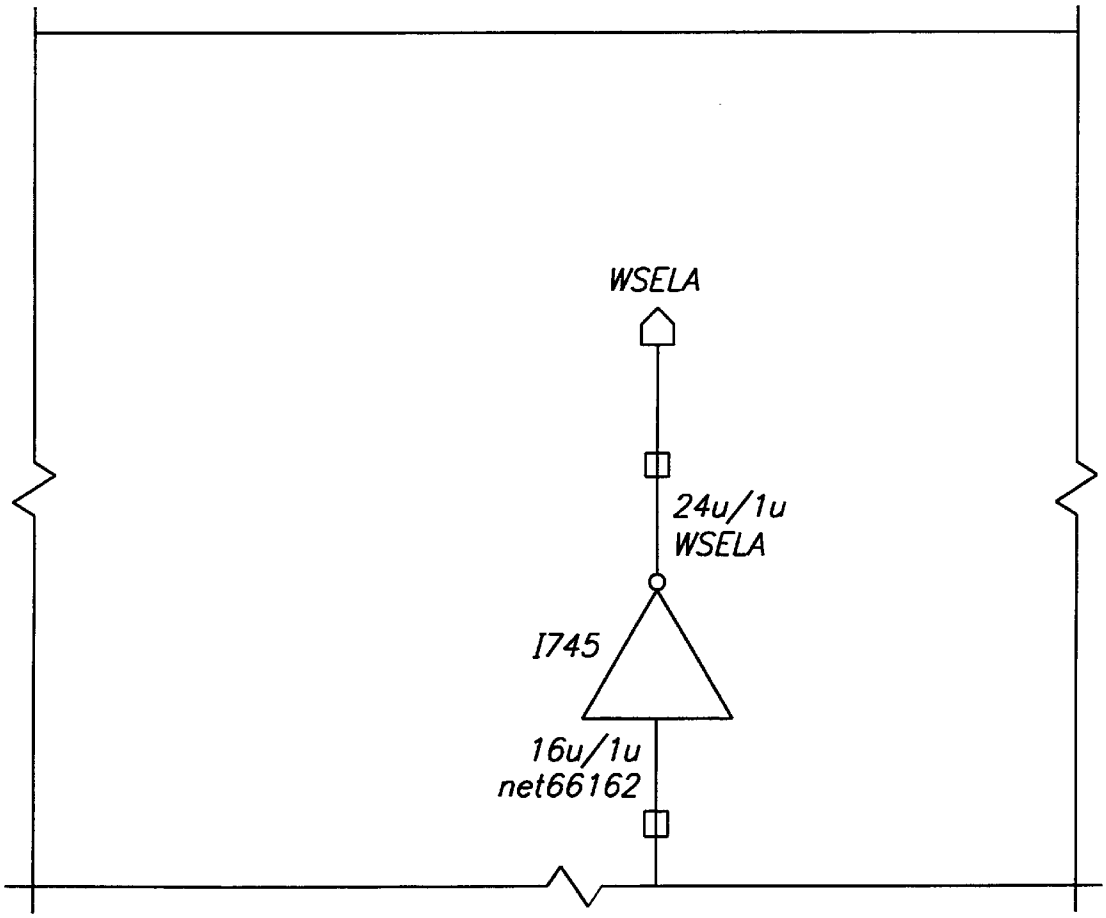


Fig 1.0601AC

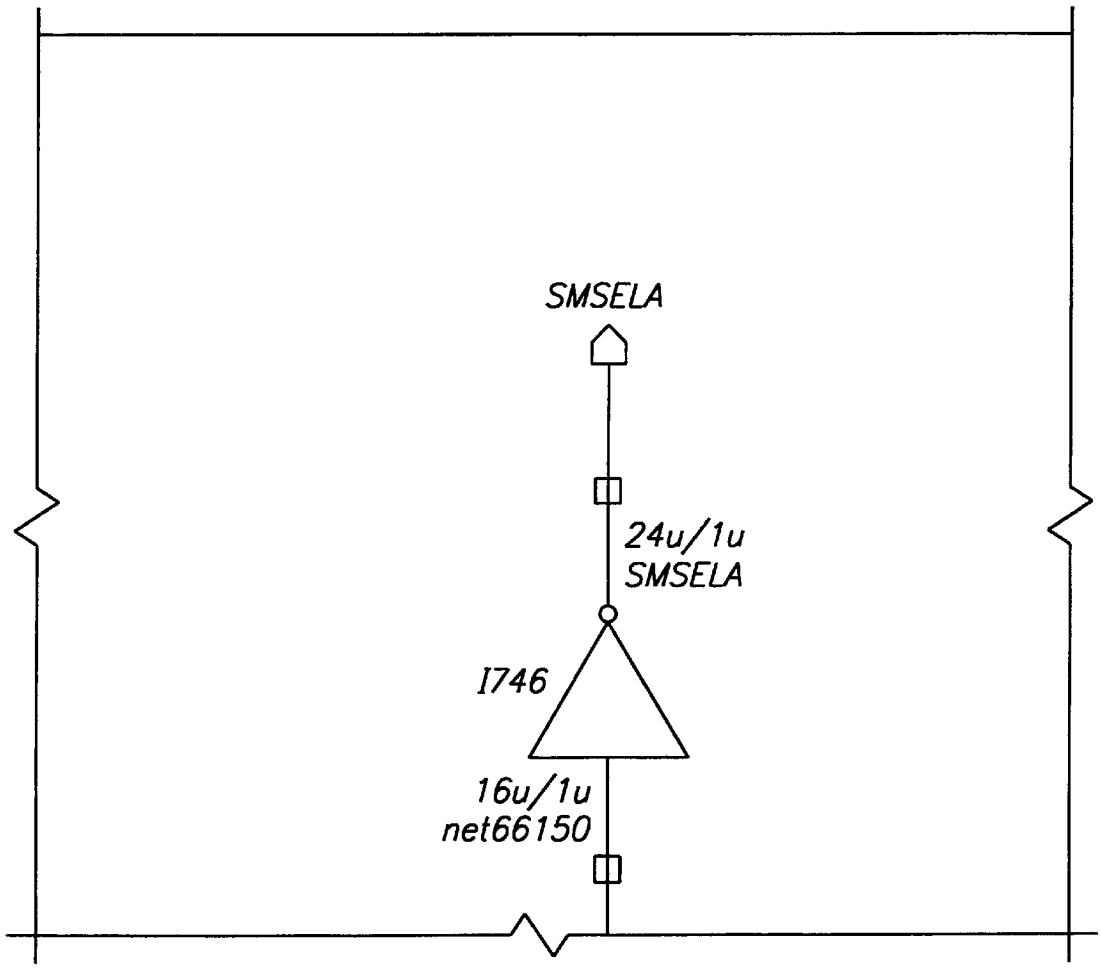
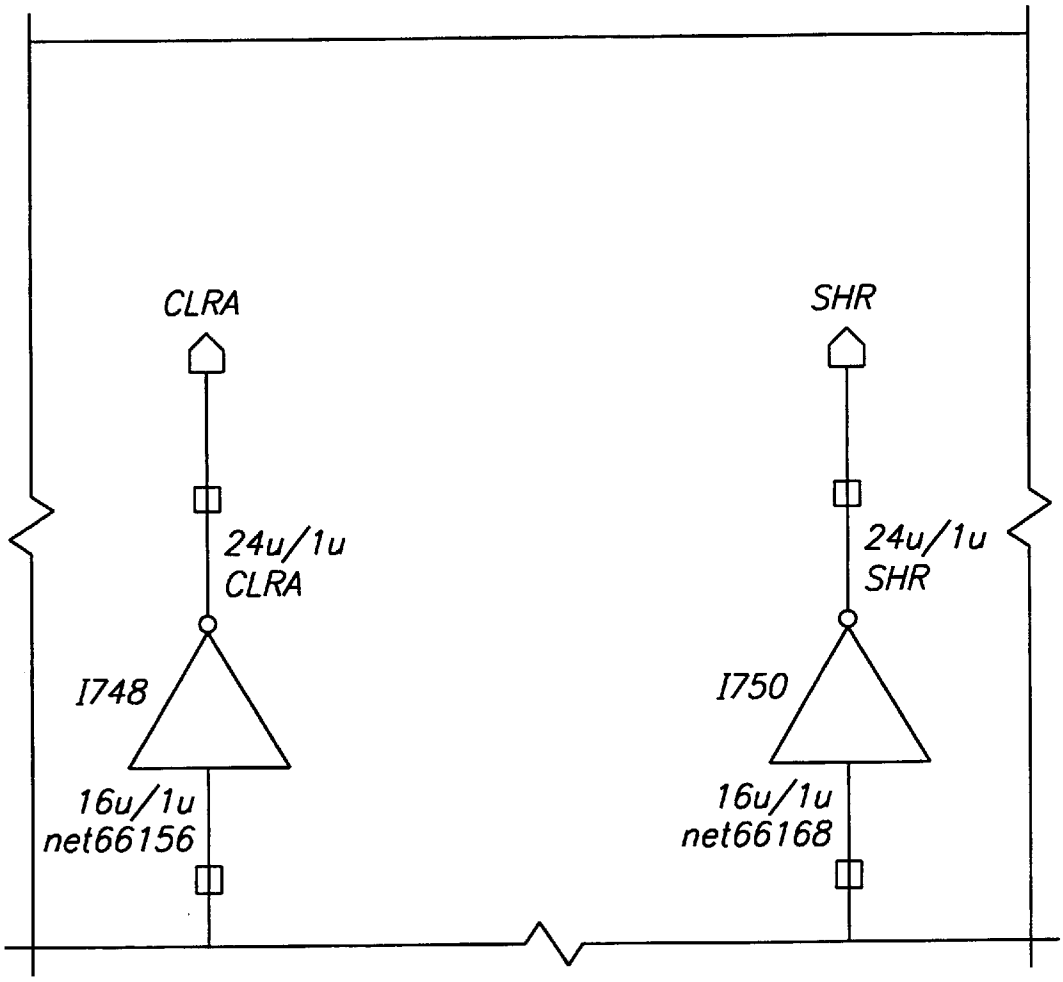


Fig 1.060140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SHR
24u/1u
SHR
I750
16u/1u
net66168

Fig 1.0601AE

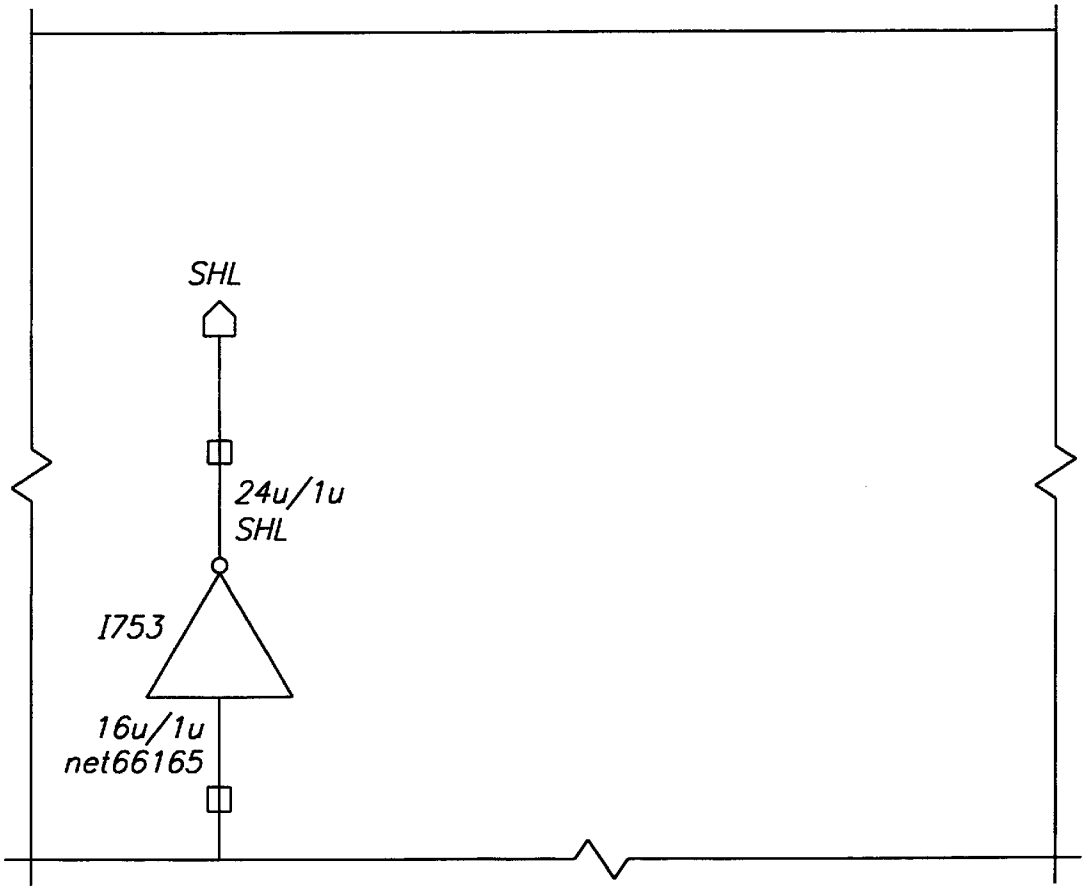


Fig 1.0601AF

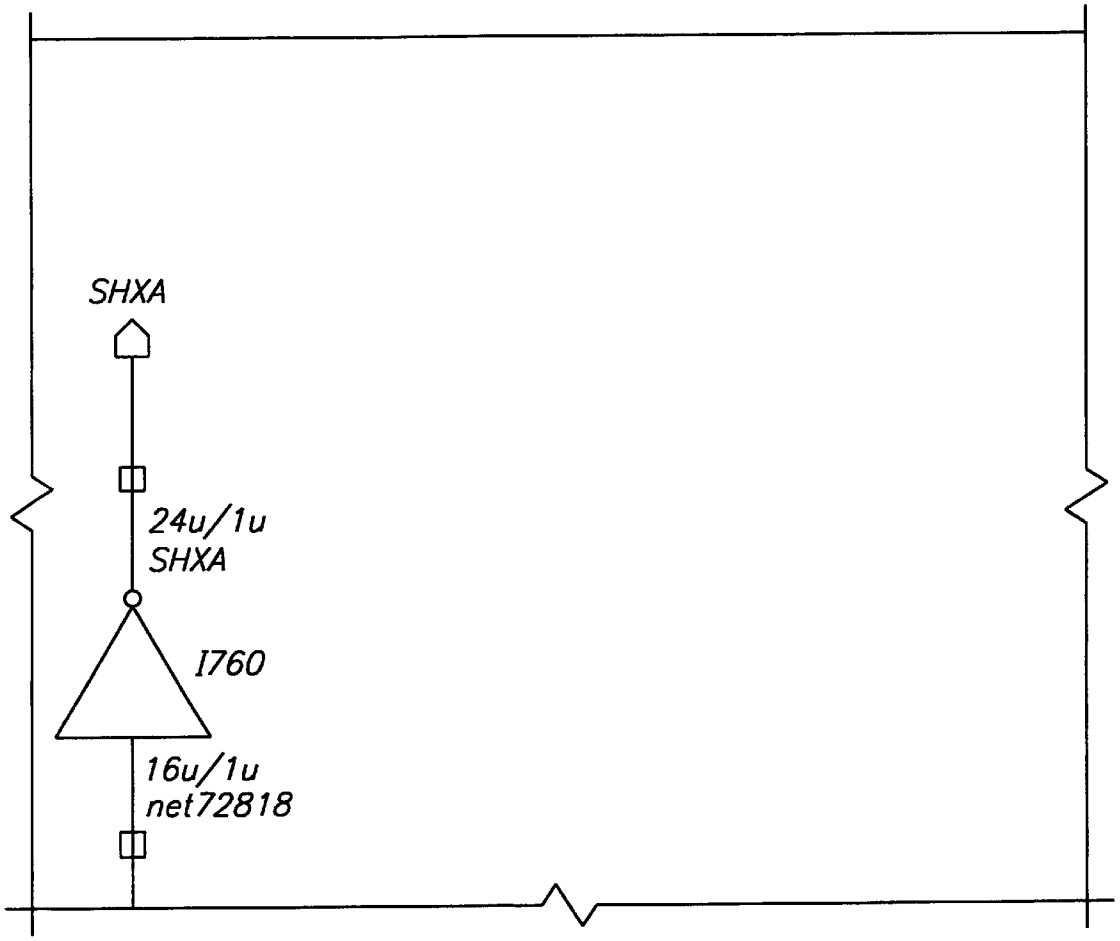
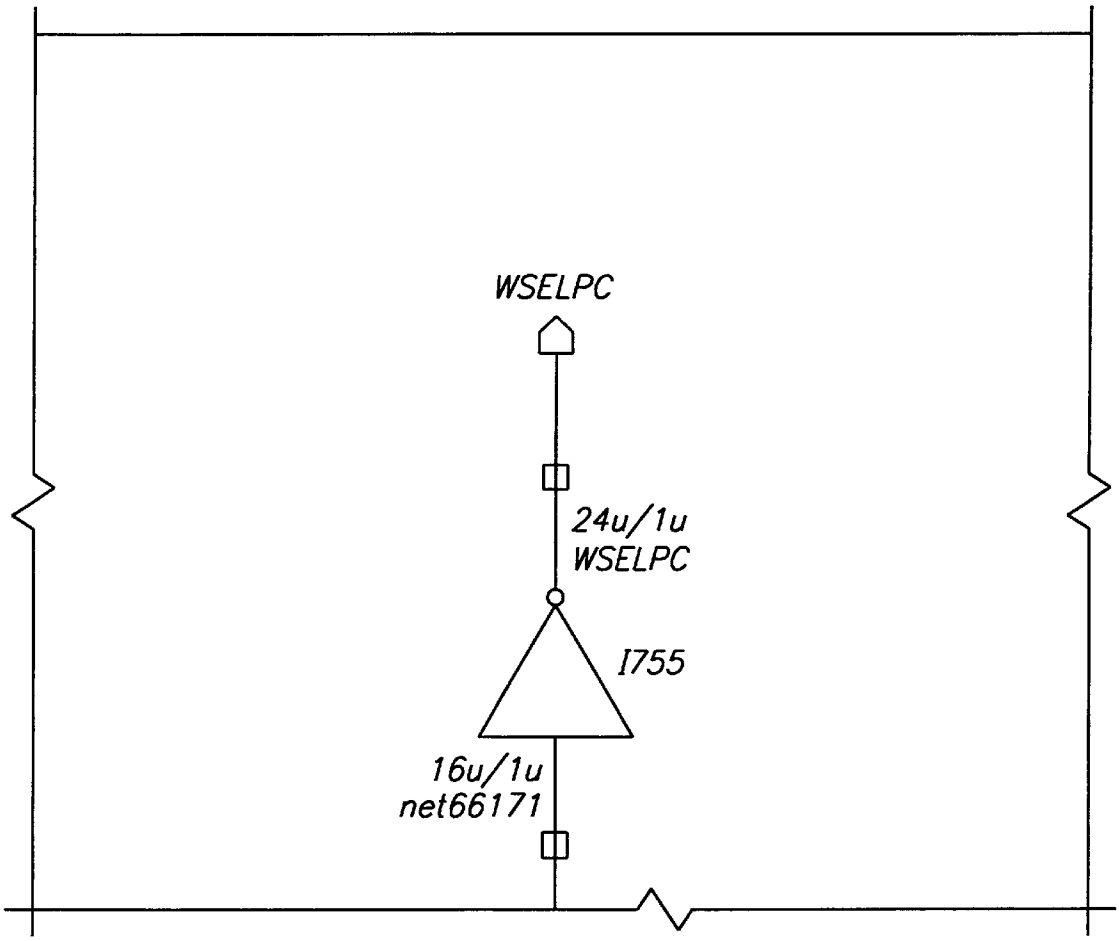


Fig 1.06016



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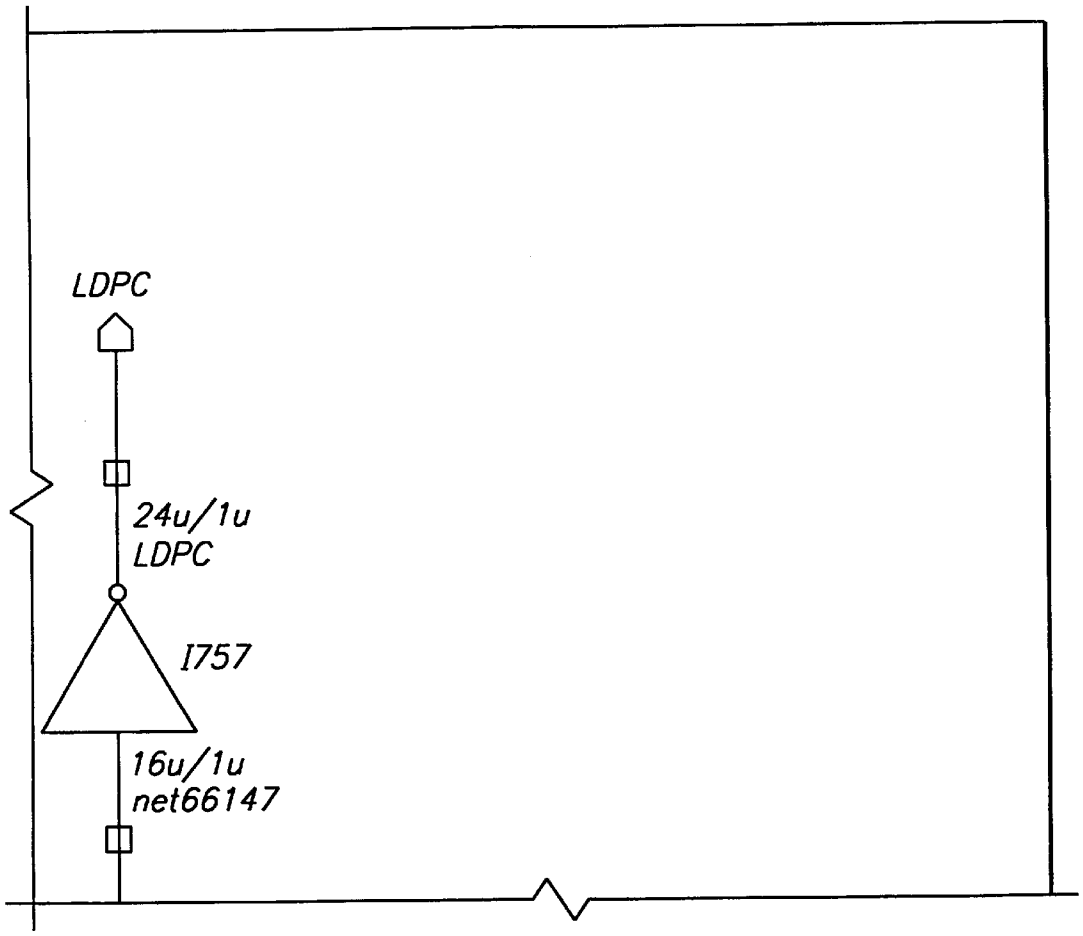
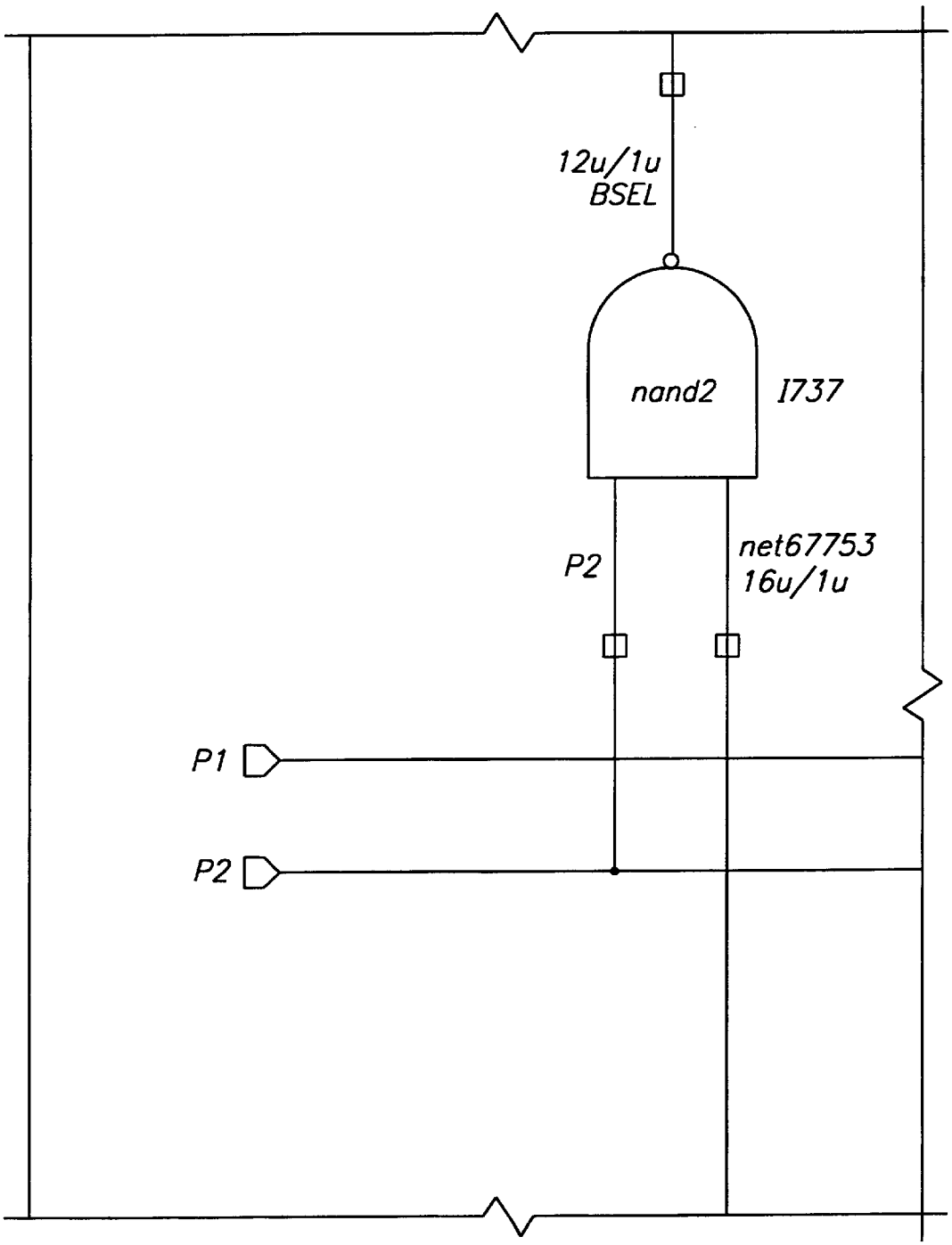


Fig 1.0601AI



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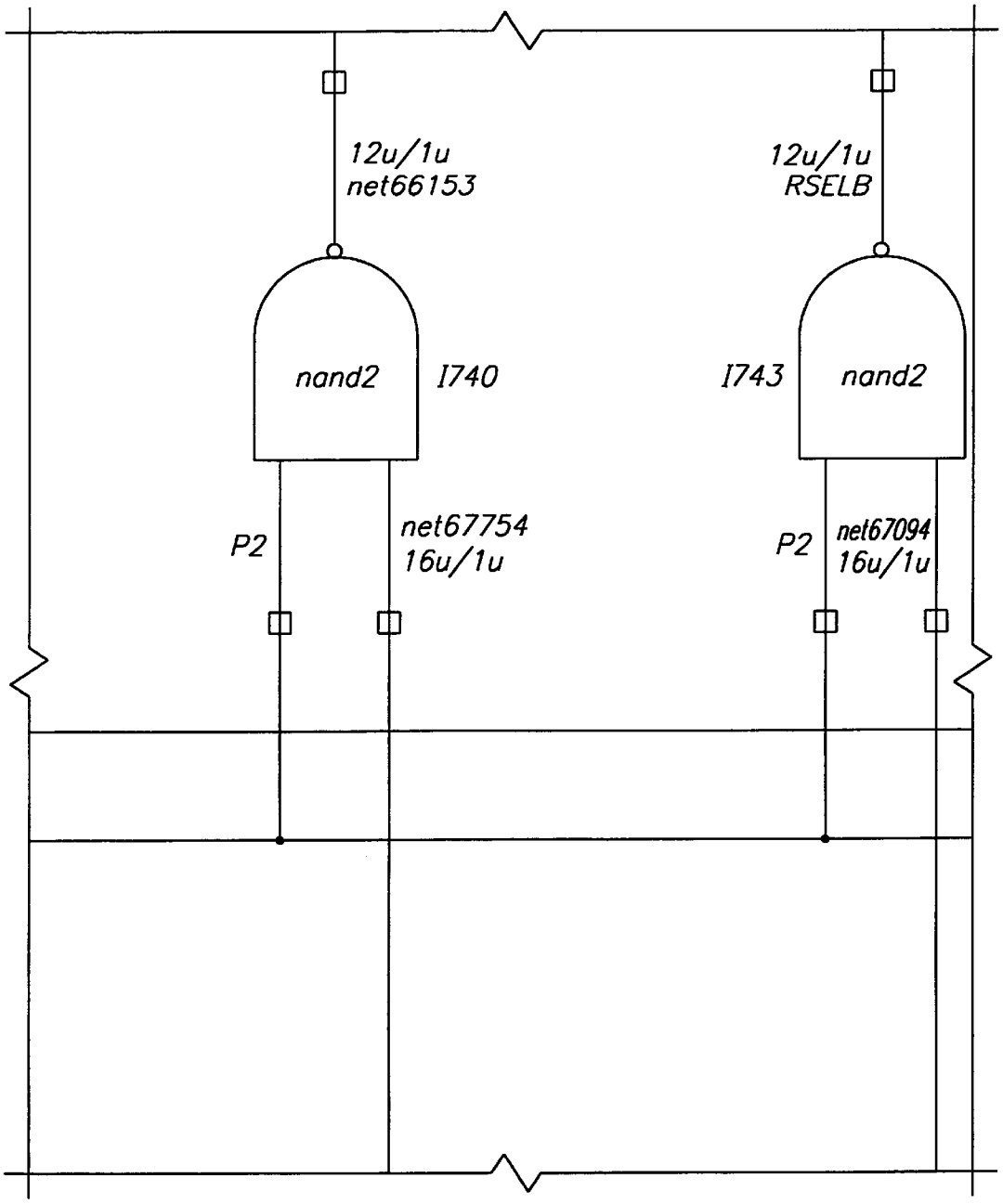
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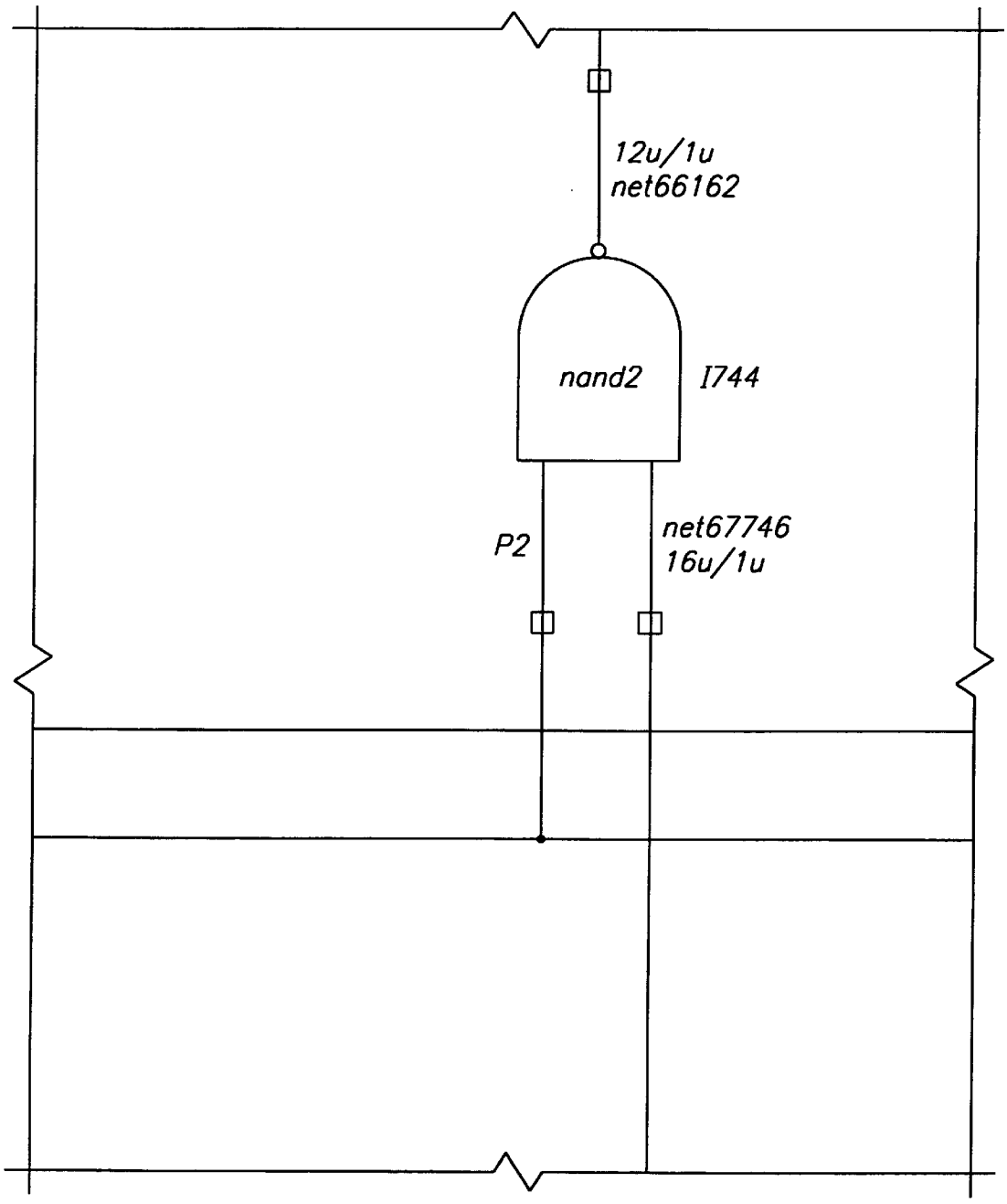
16u/1u

Fig 1,060,188



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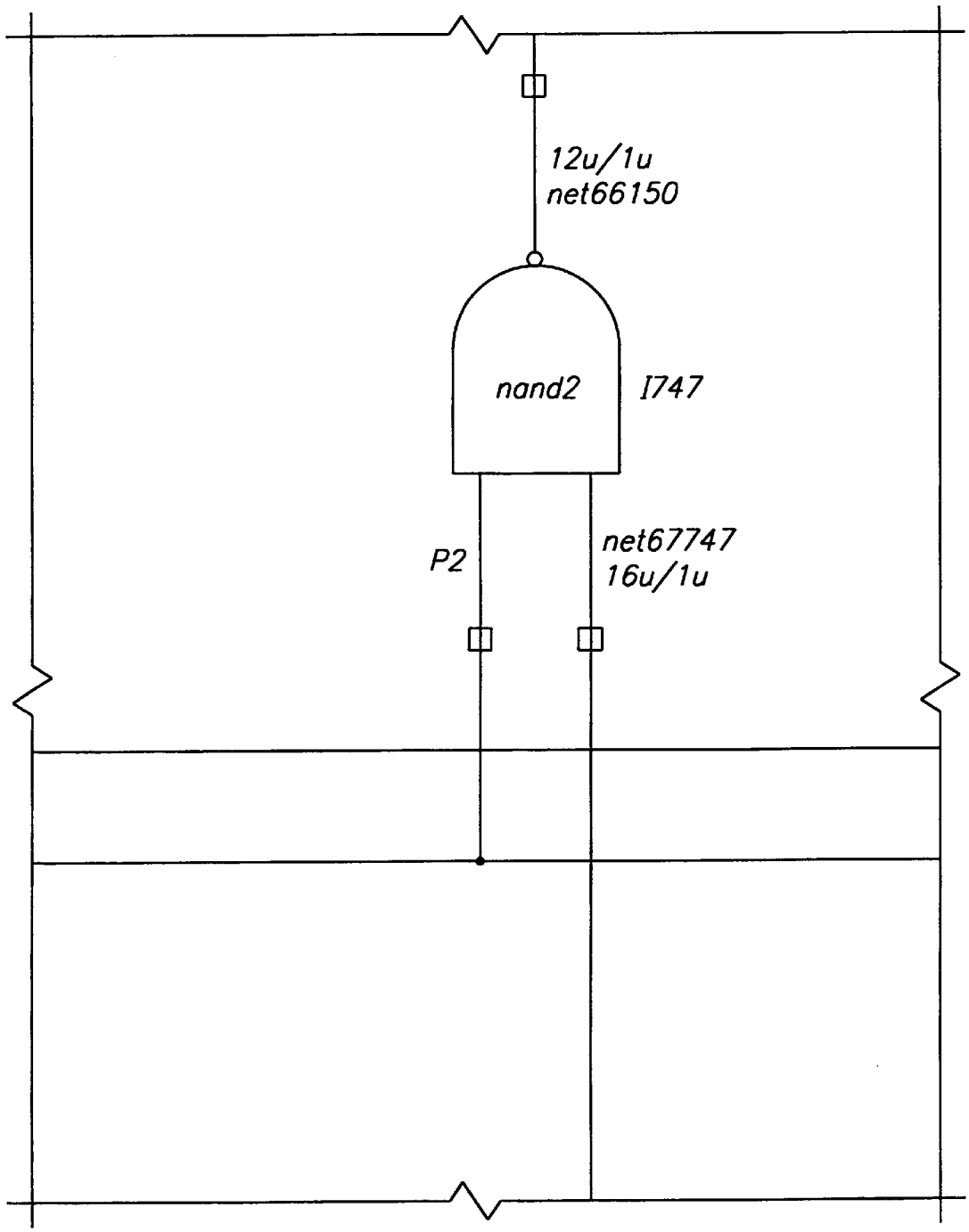
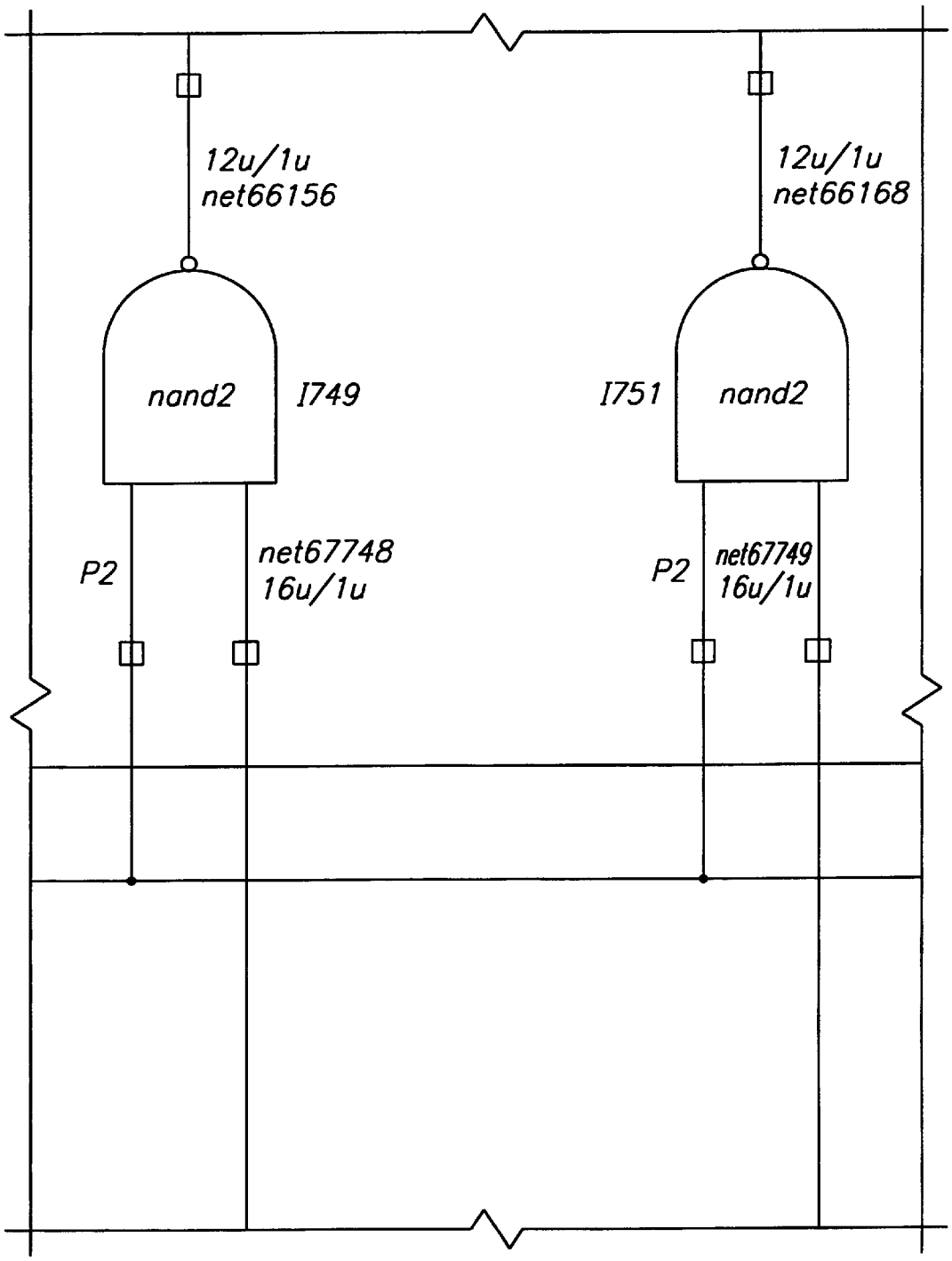


Fig 7.0601BD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P2
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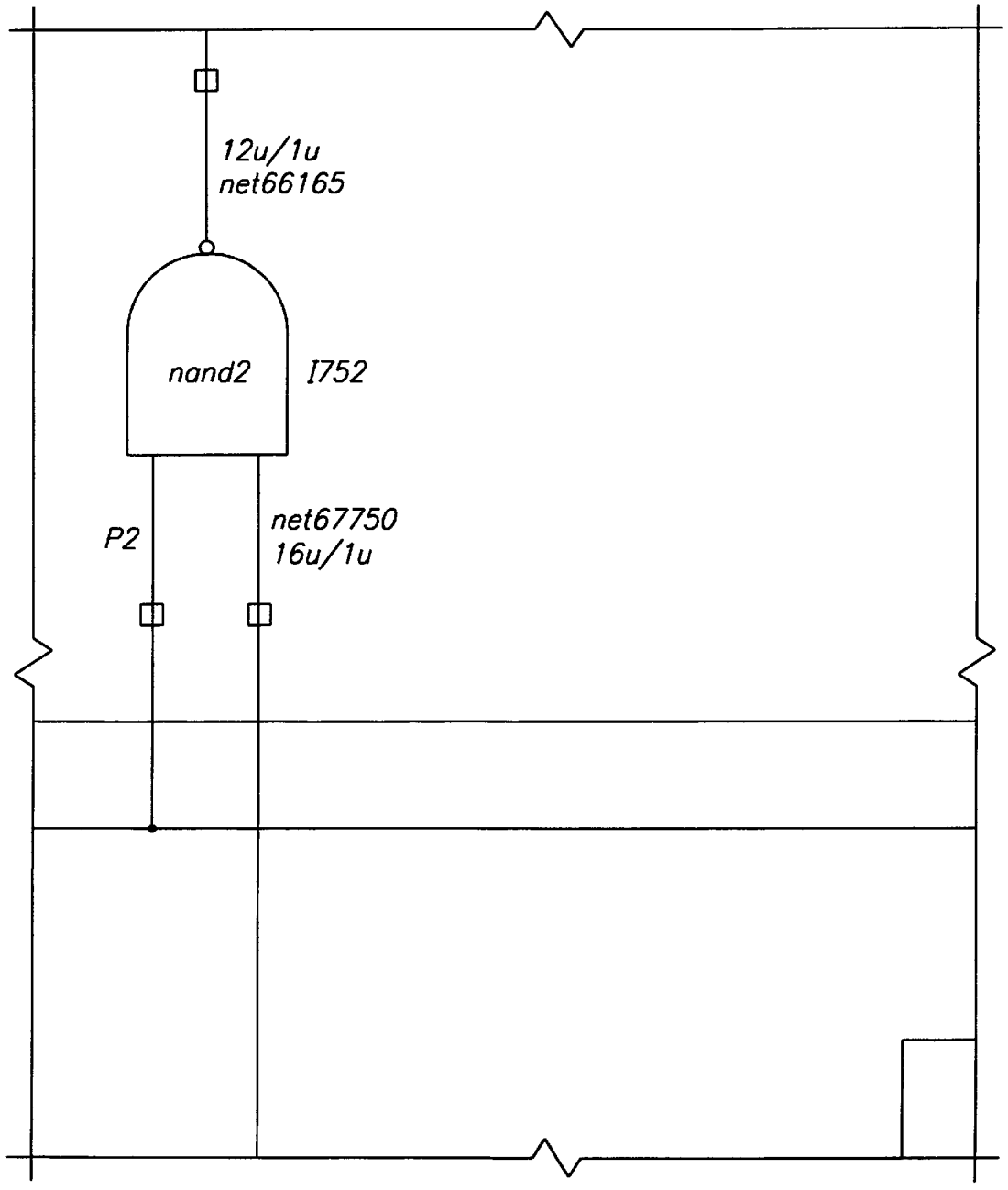
16u/1u

Fig 1.0601BE



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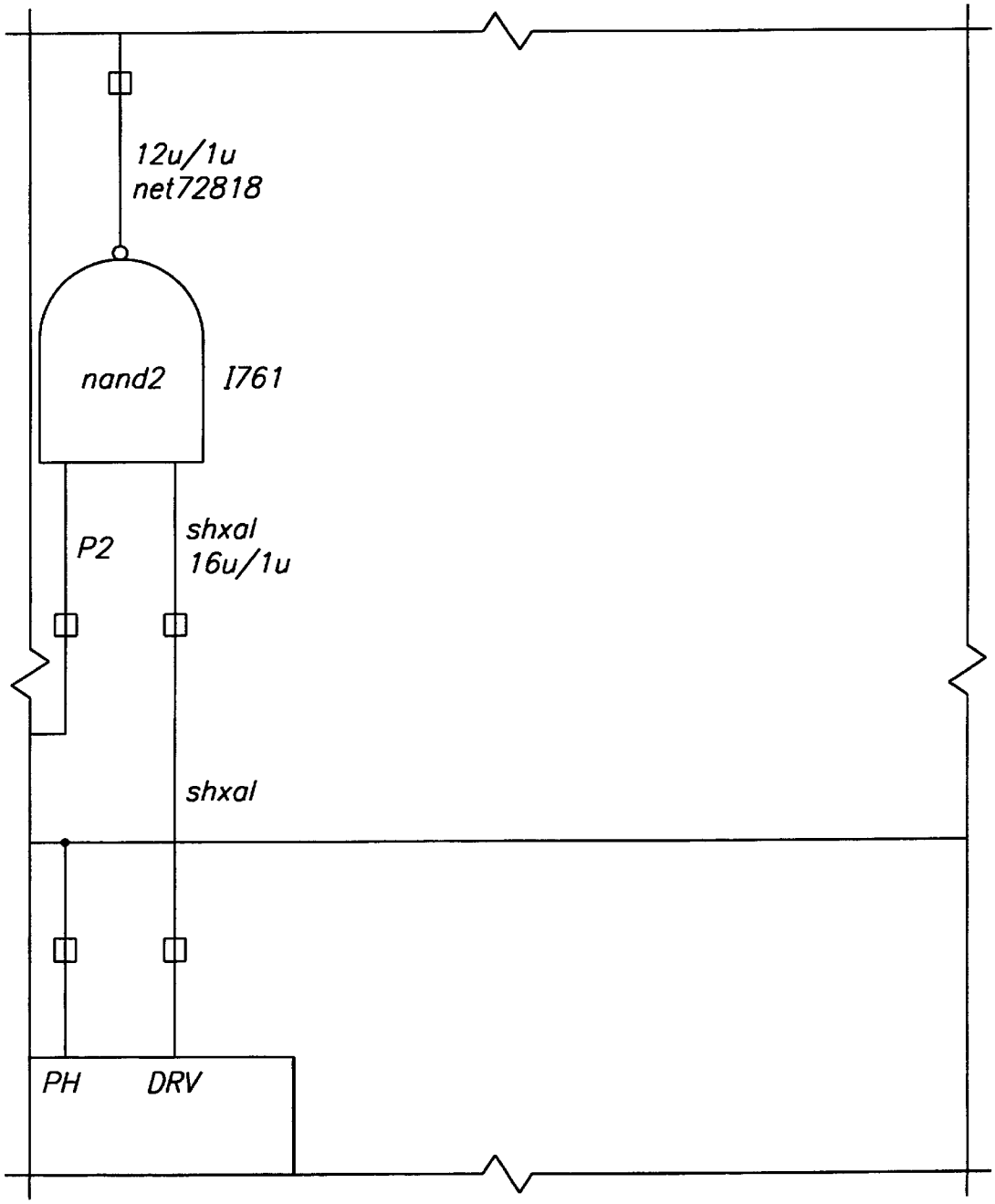

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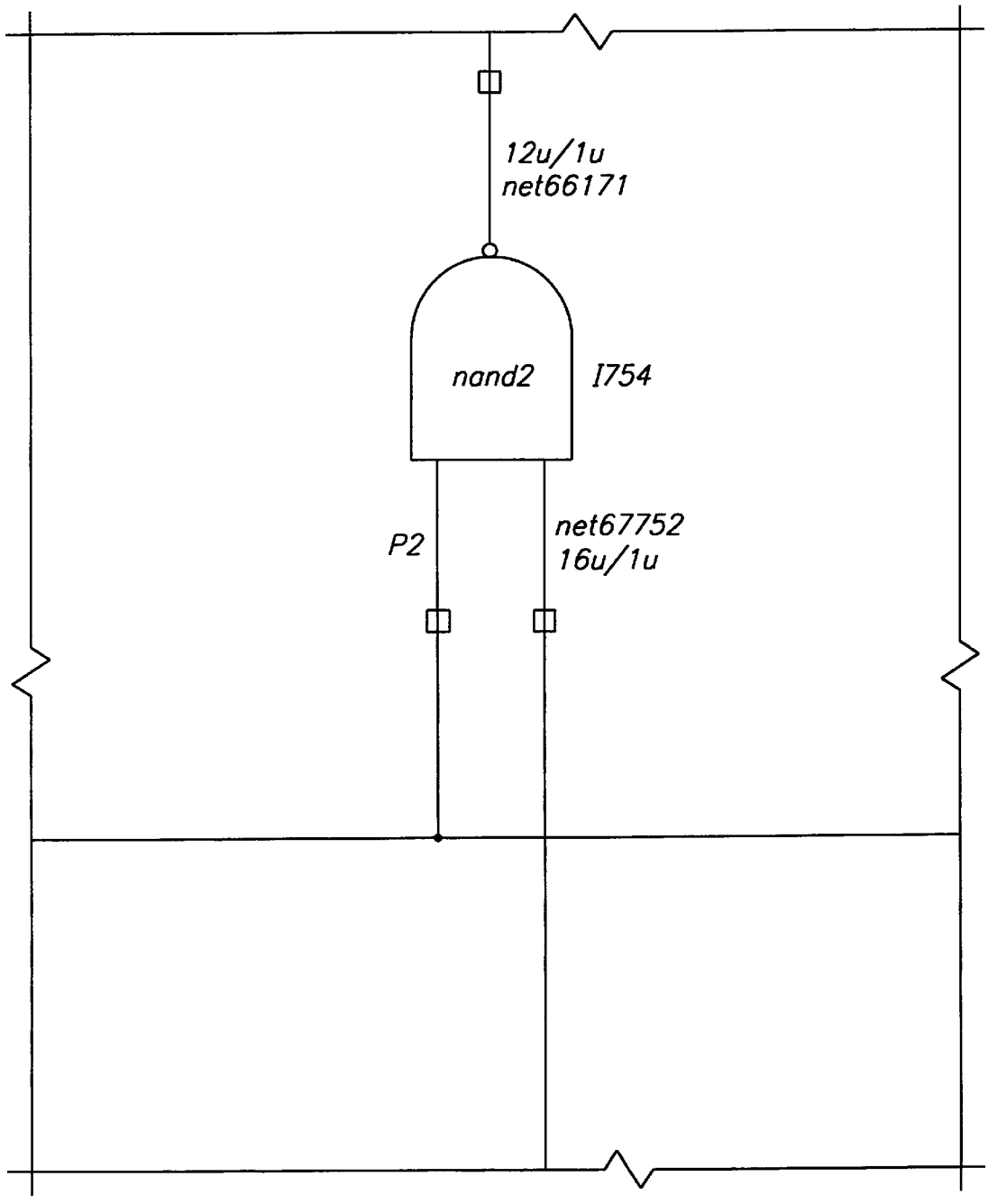


FIG 1.0601BH

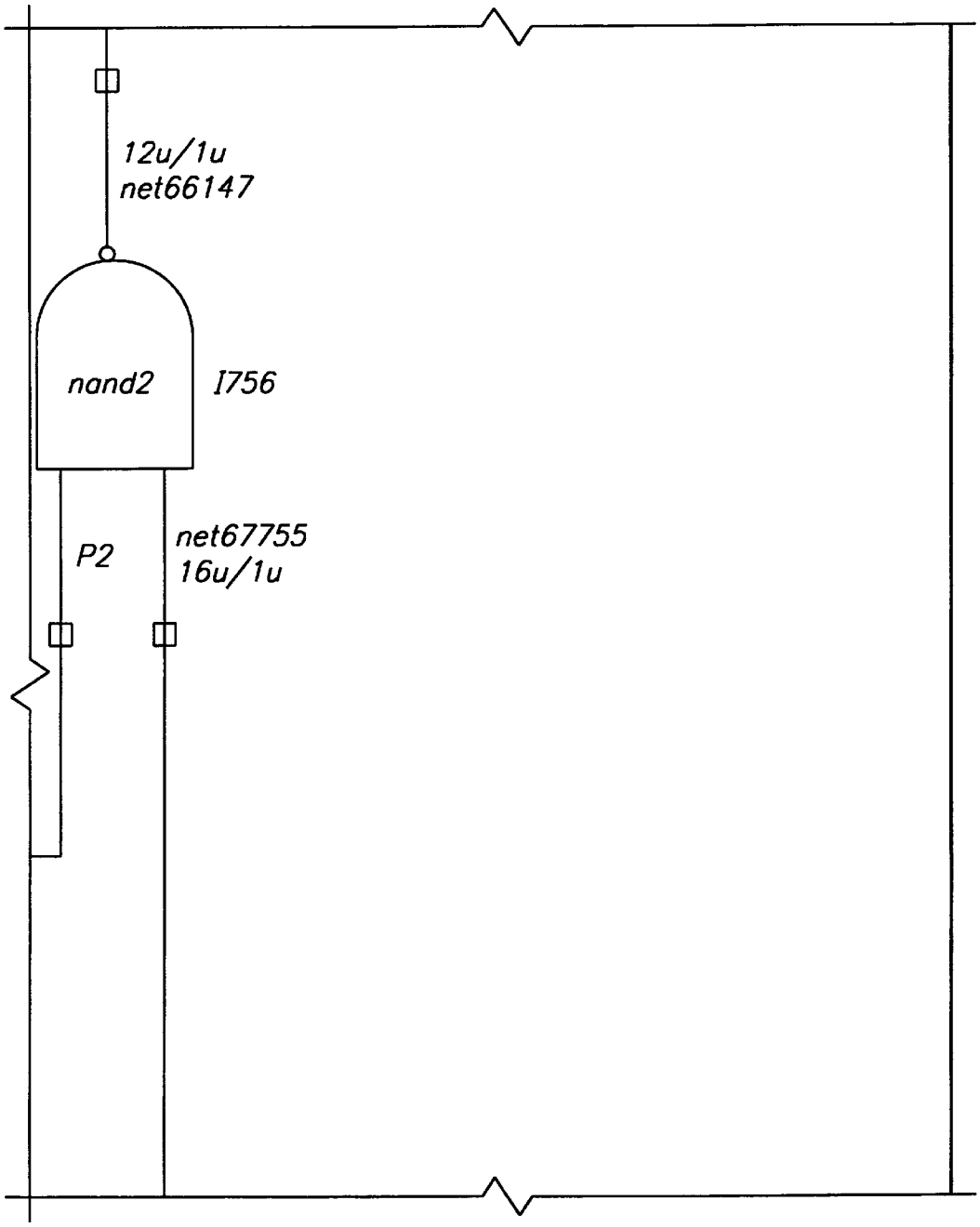
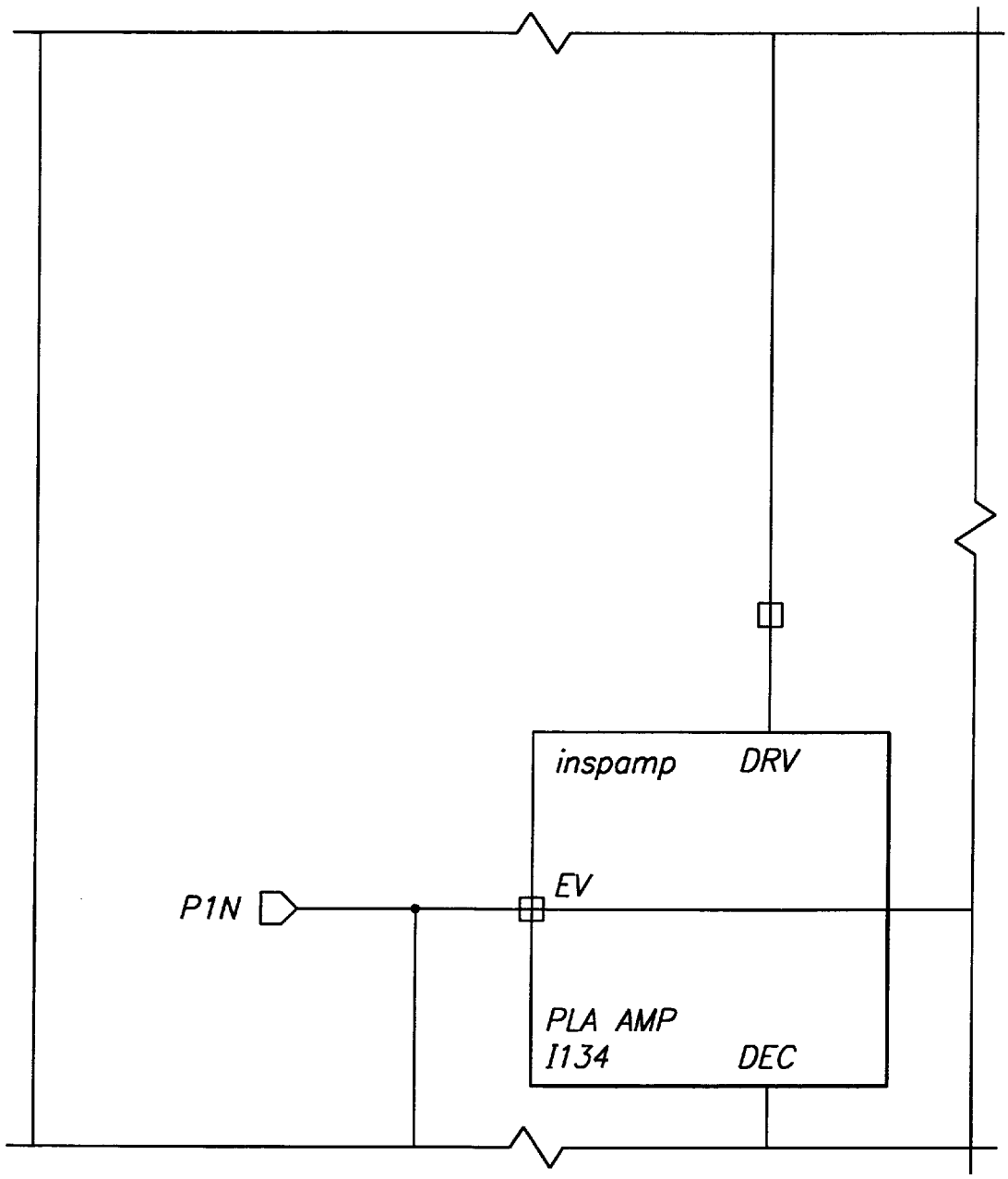


Fig 7.0601BI



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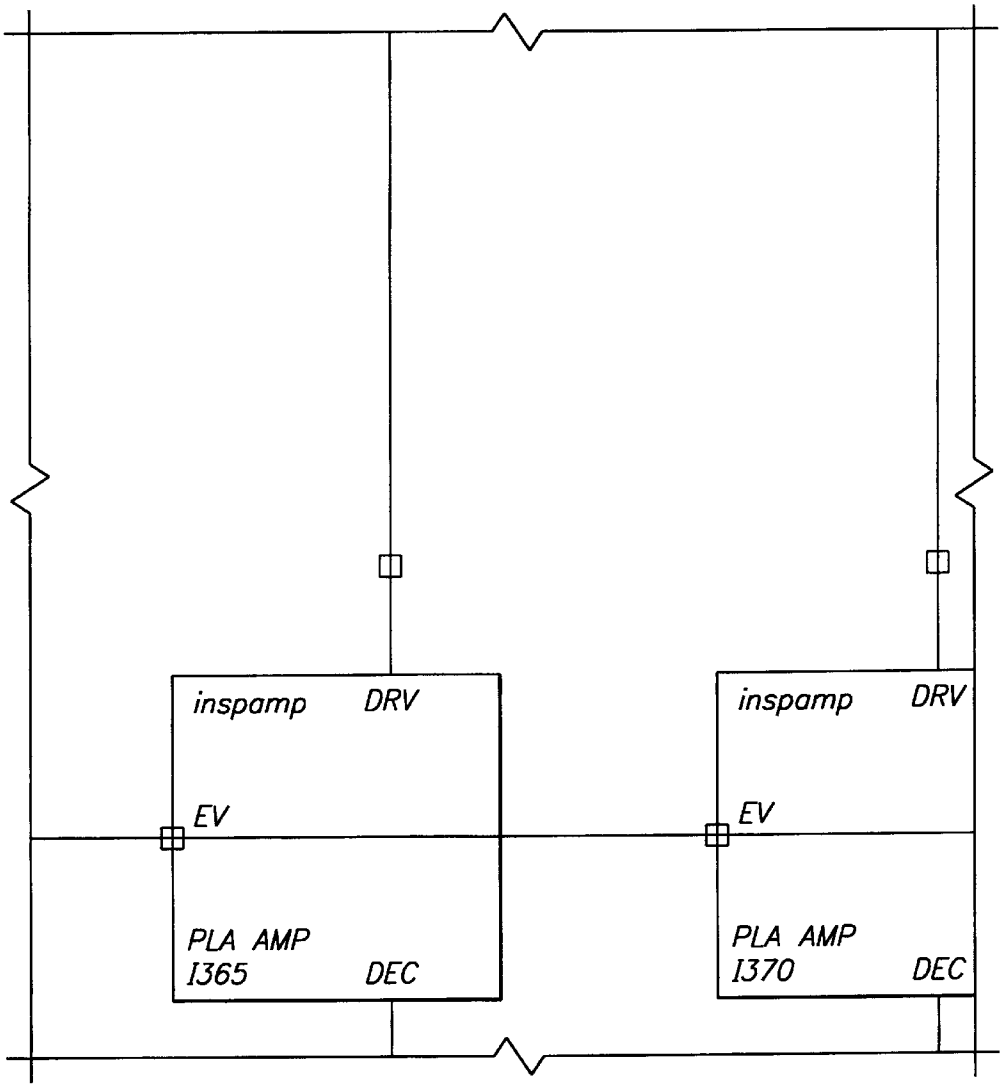
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DEC

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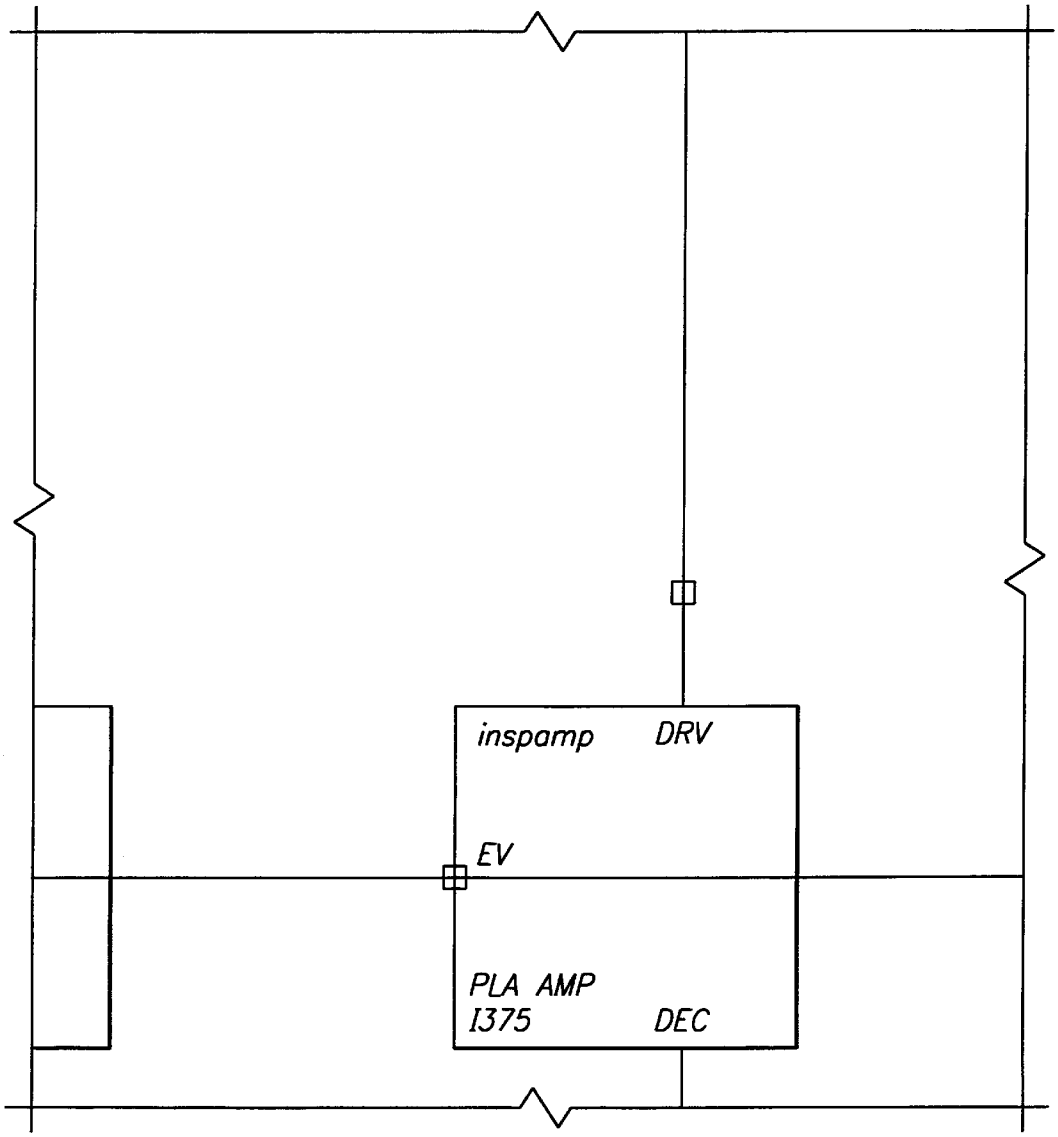

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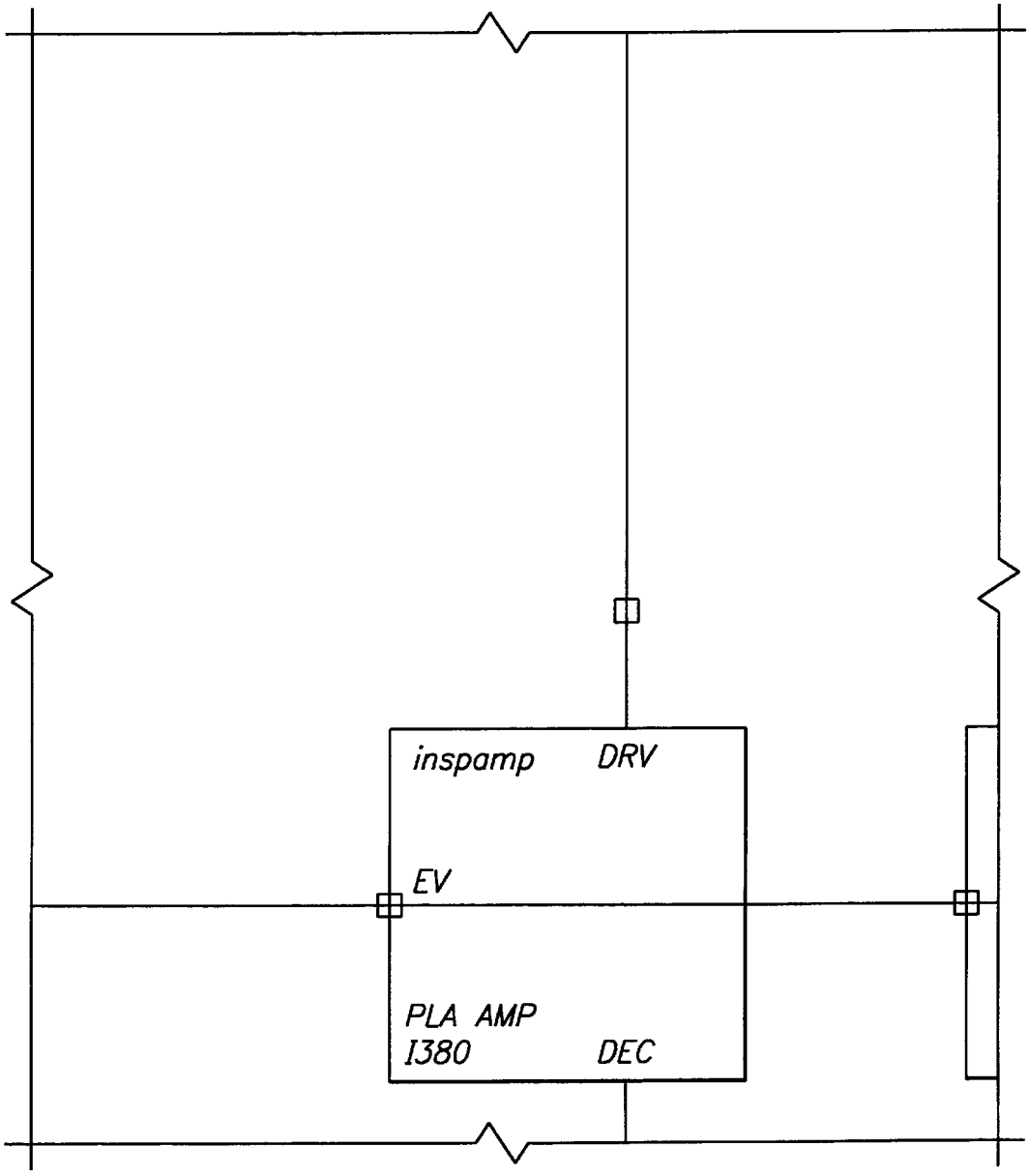

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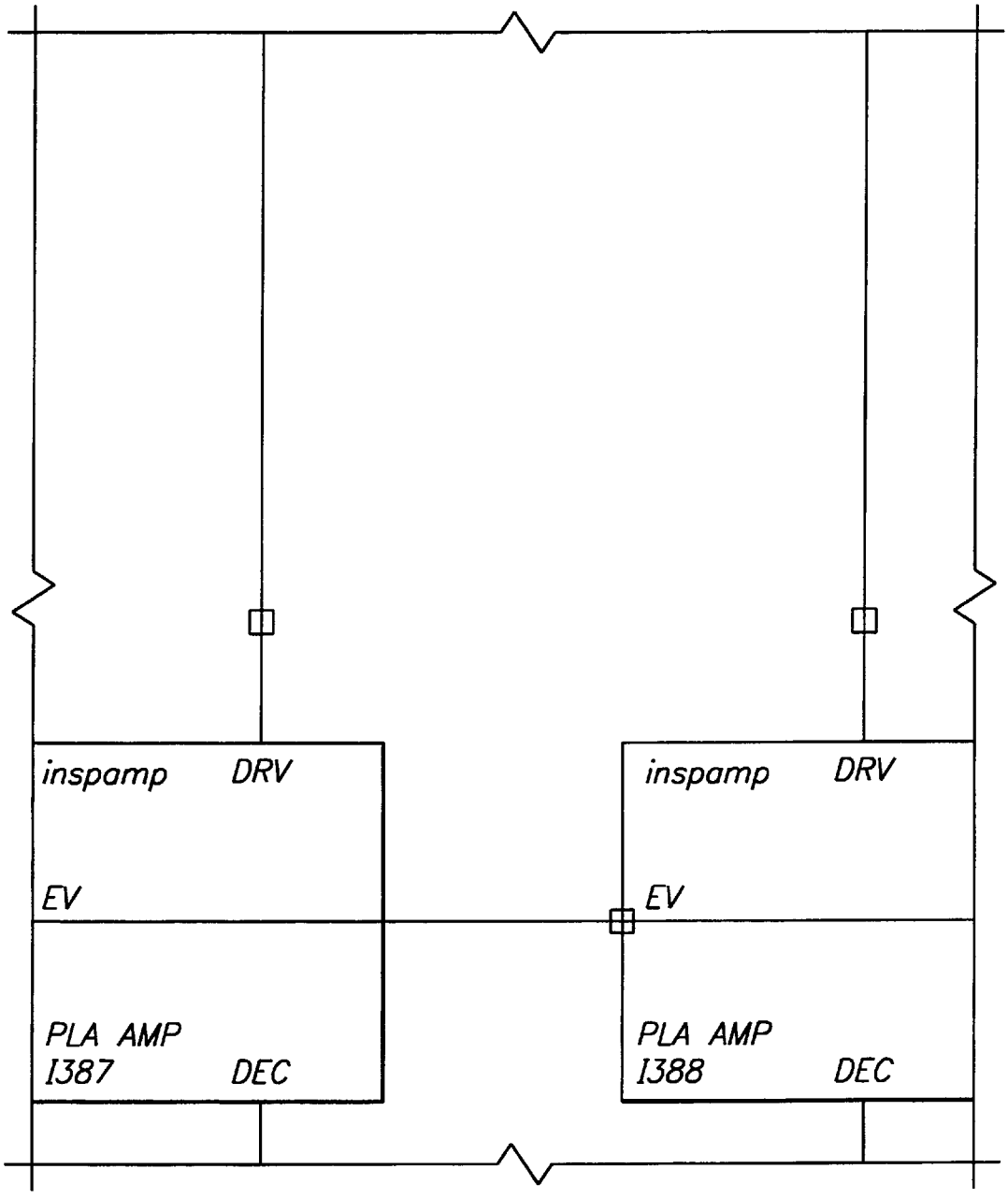
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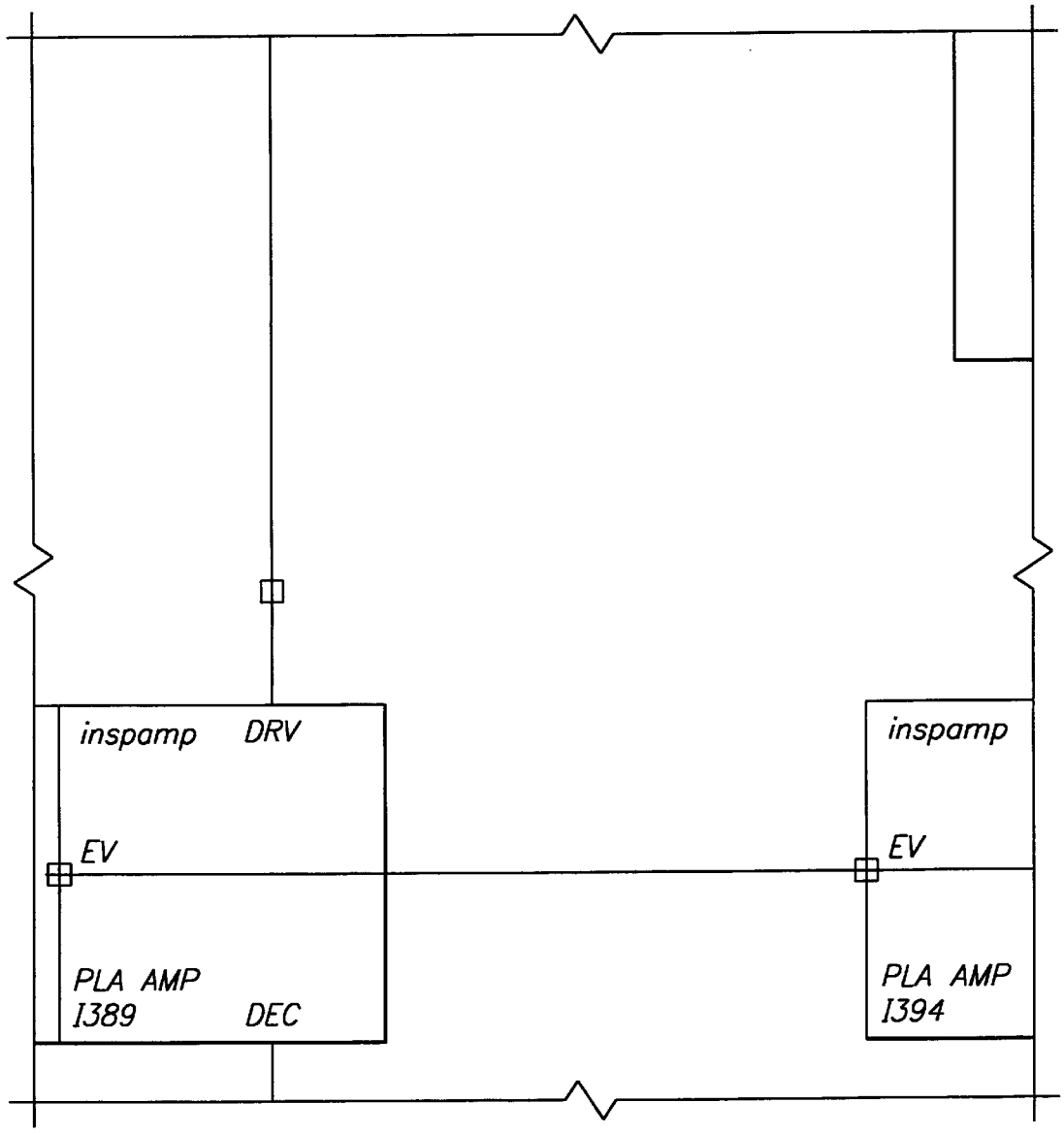
Fig 1.0601CE



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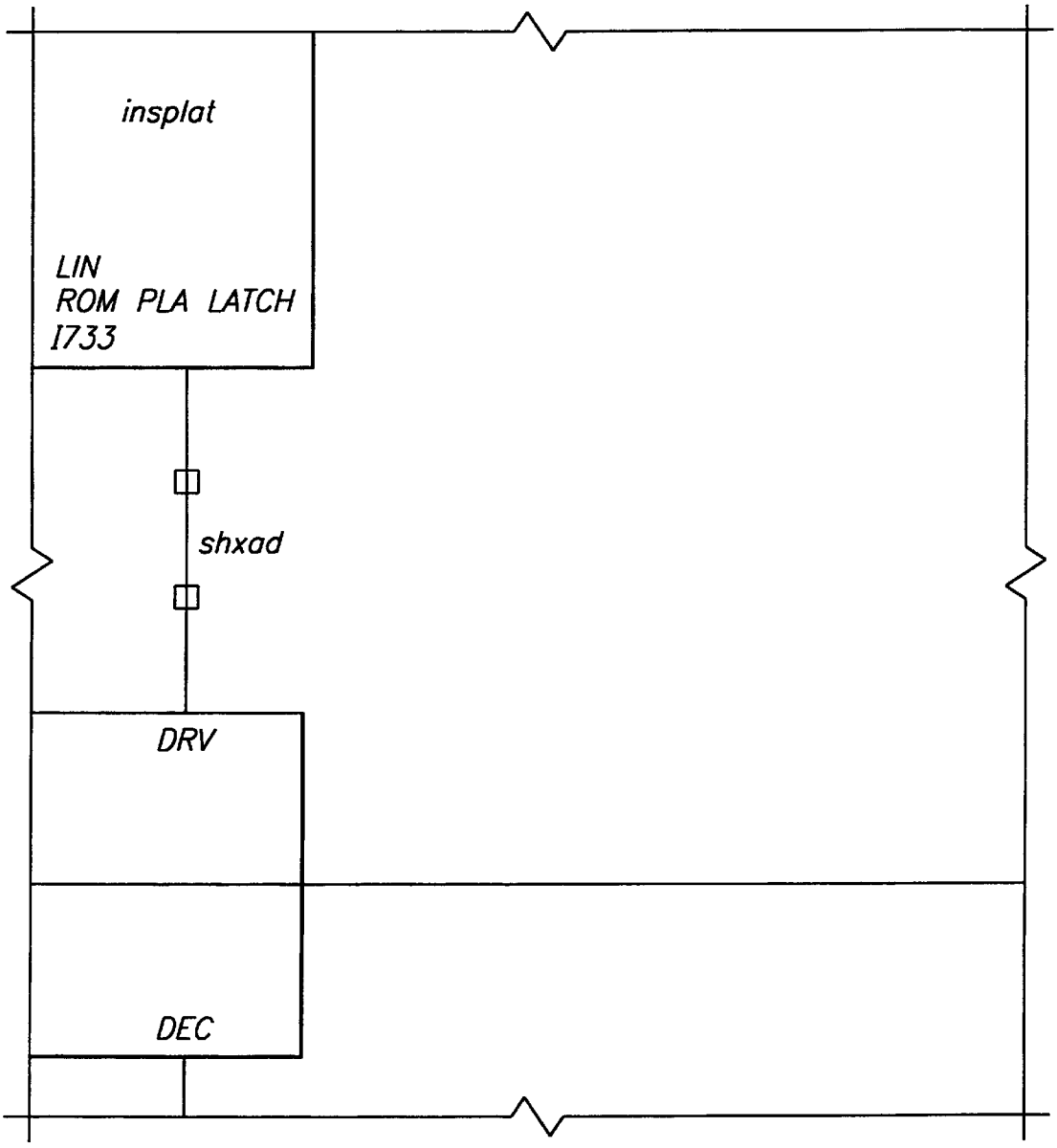

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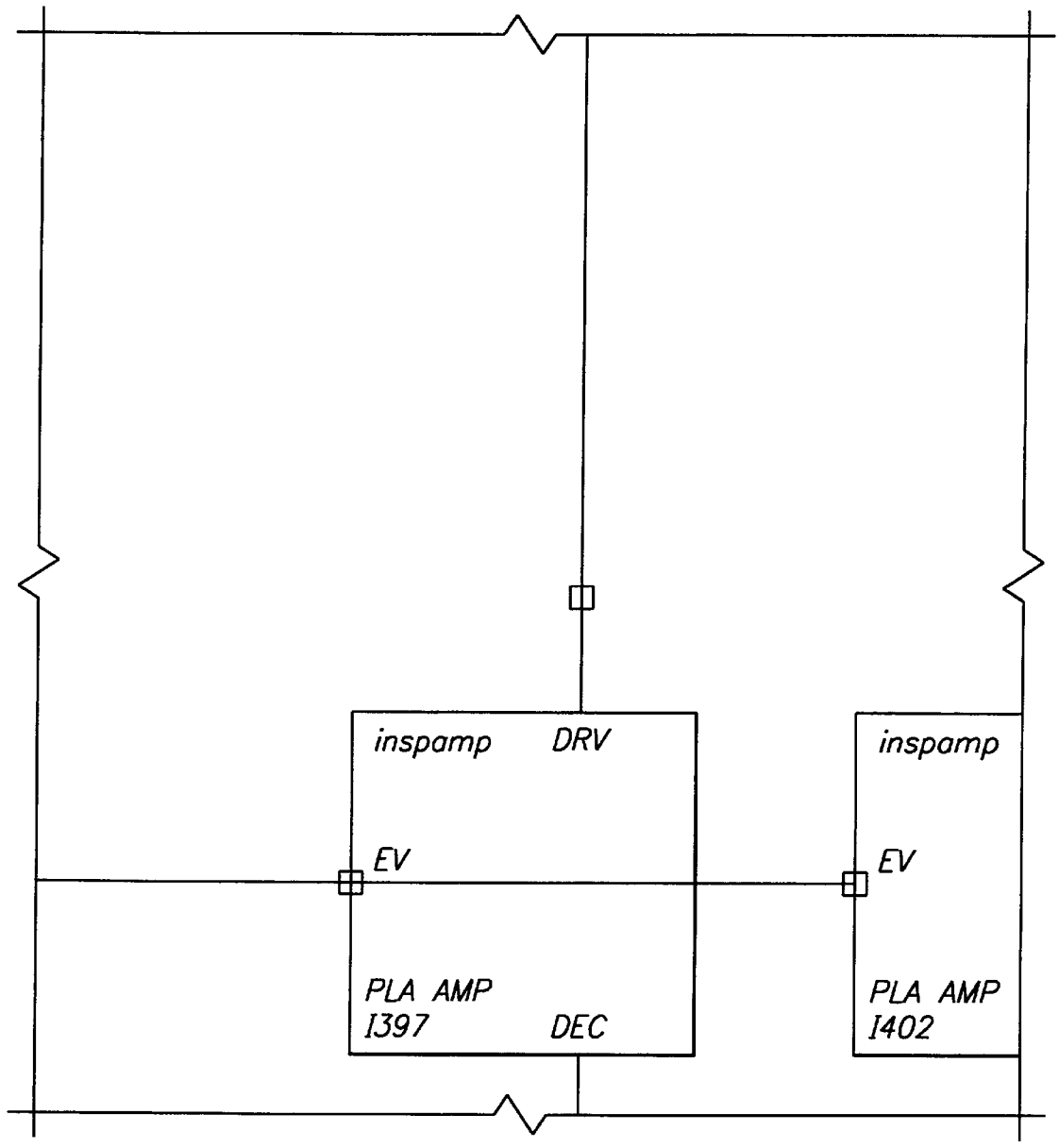


Fig 1.060ICH

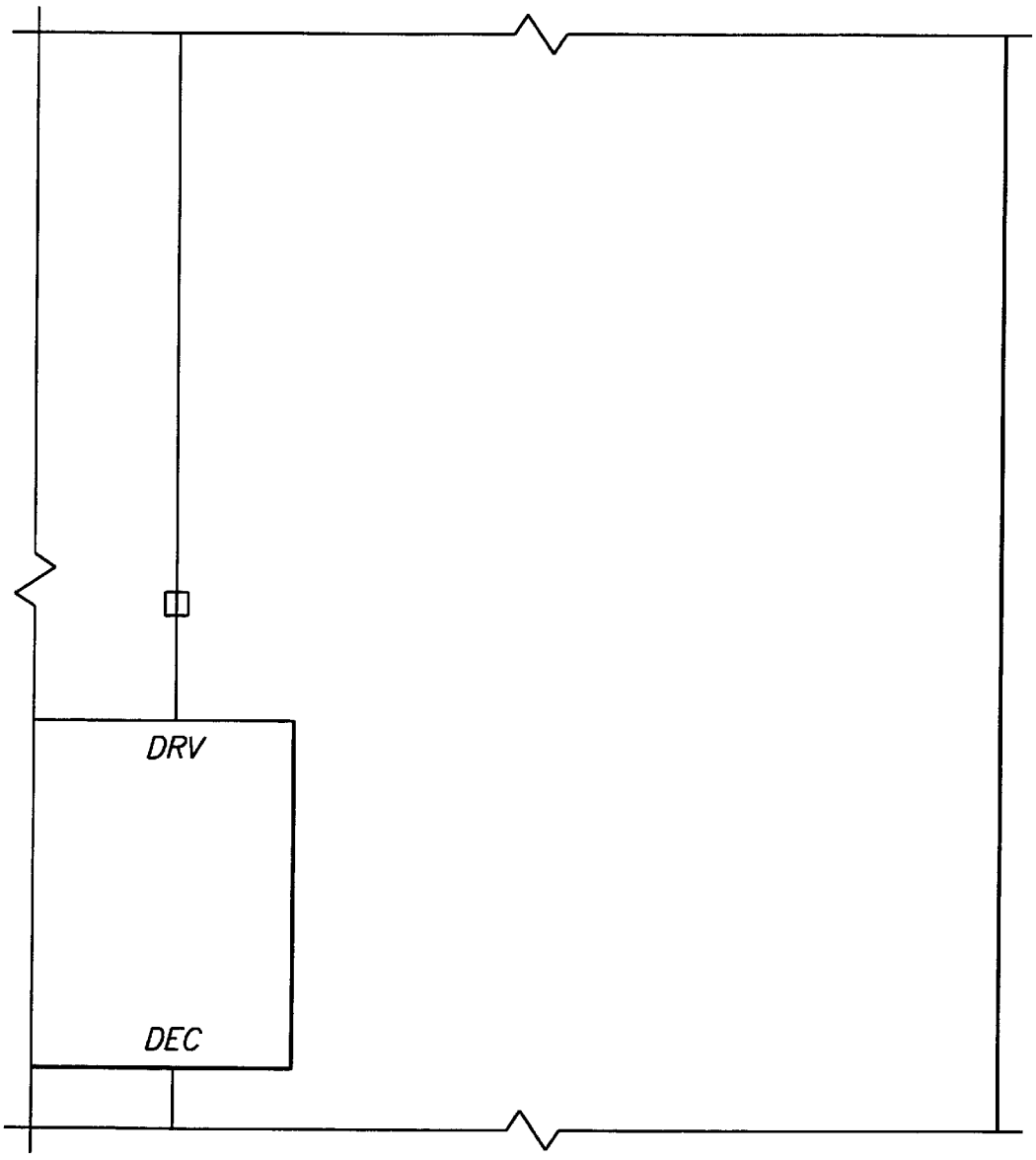


Fig 1.060ICI

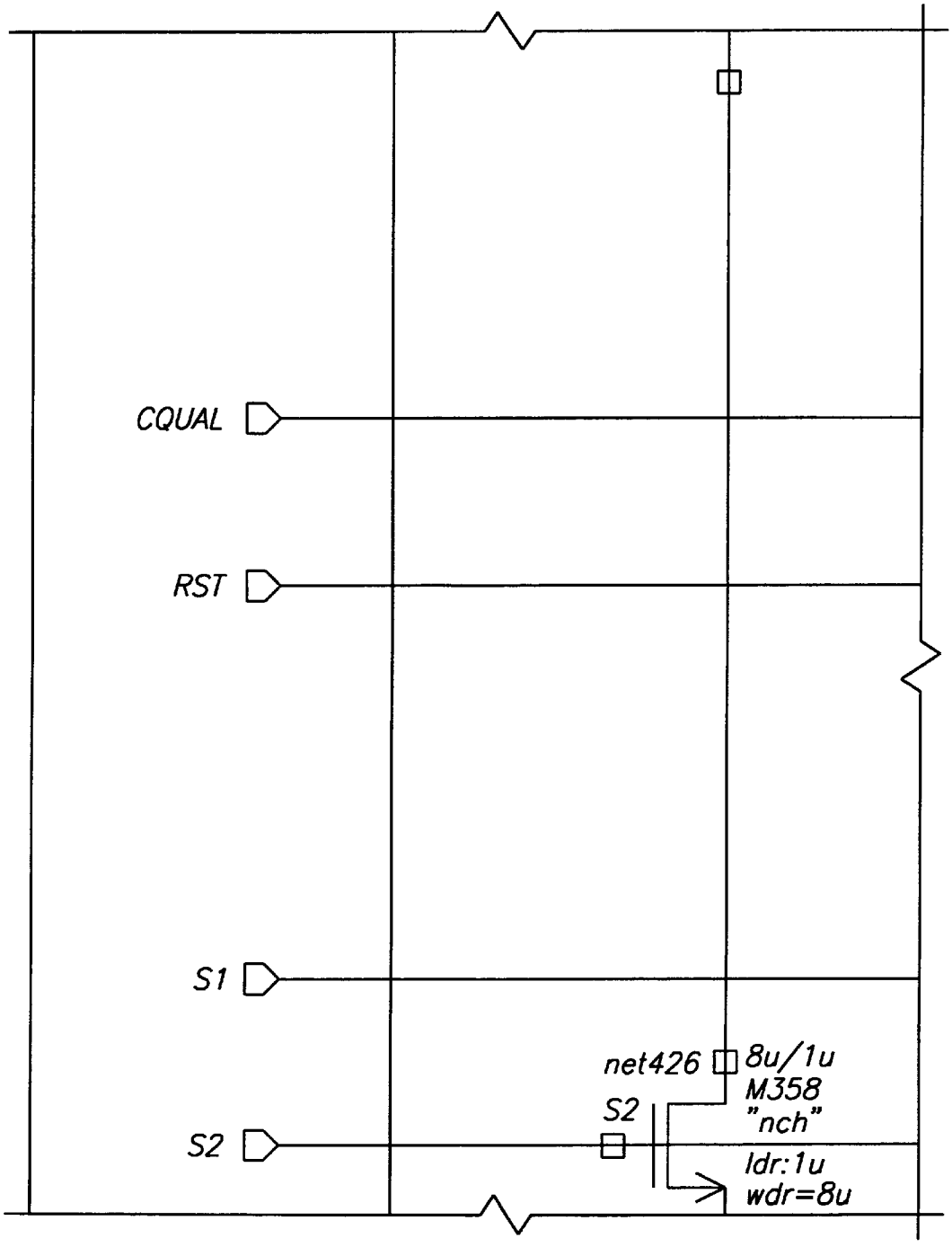


Fig 1.0601DA

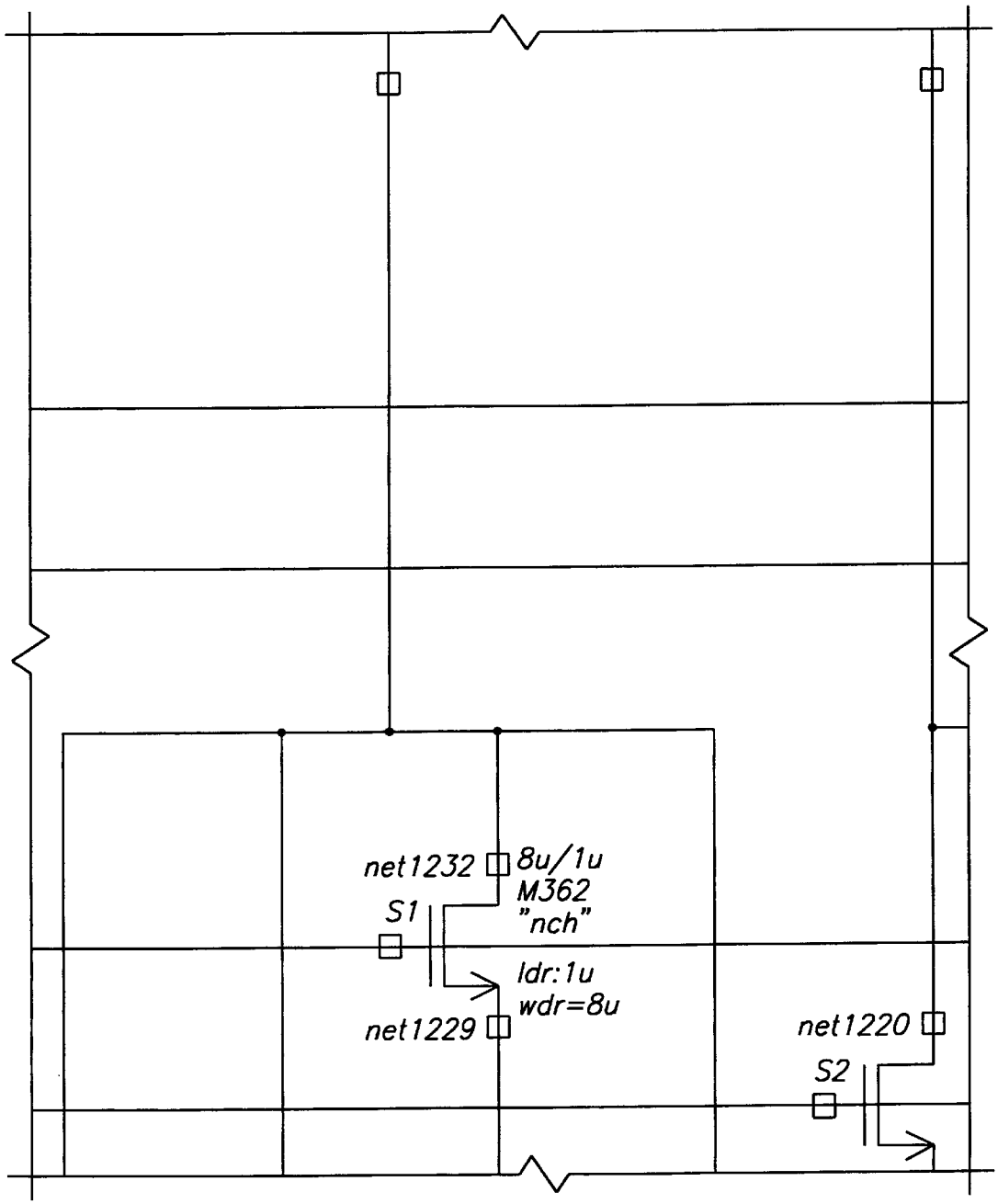


Fig 1.0601DB

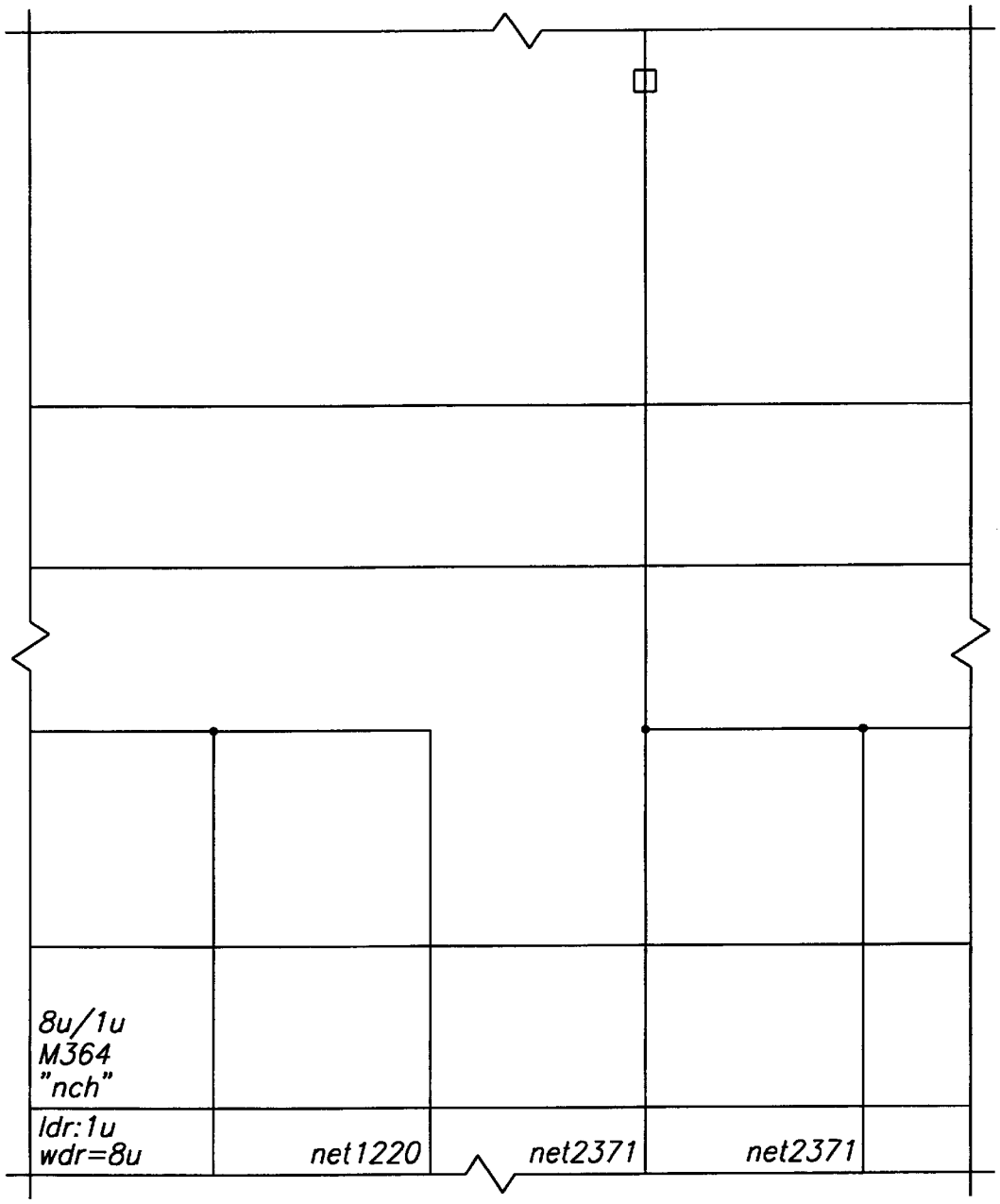


Fig 1.060110C

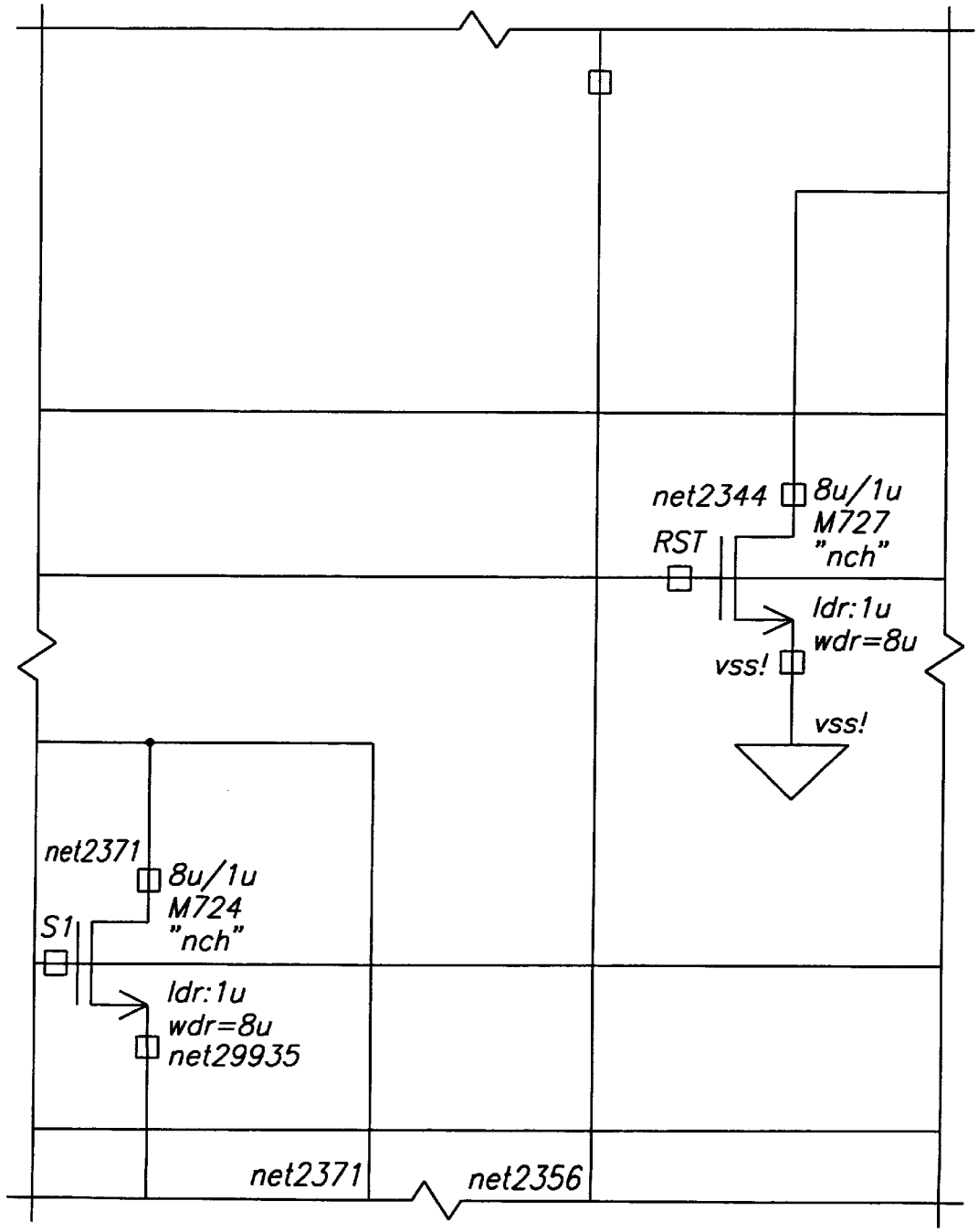

net2344
8u/1u
M727
"nch"
RST
ldr:1u
wdr=8u
vss!
vss!
net2371
8u/1u
M724
"nch"
S1
ldr:1u
wdr=8u
net29935
net2371
net2356

Fig 1,060,100

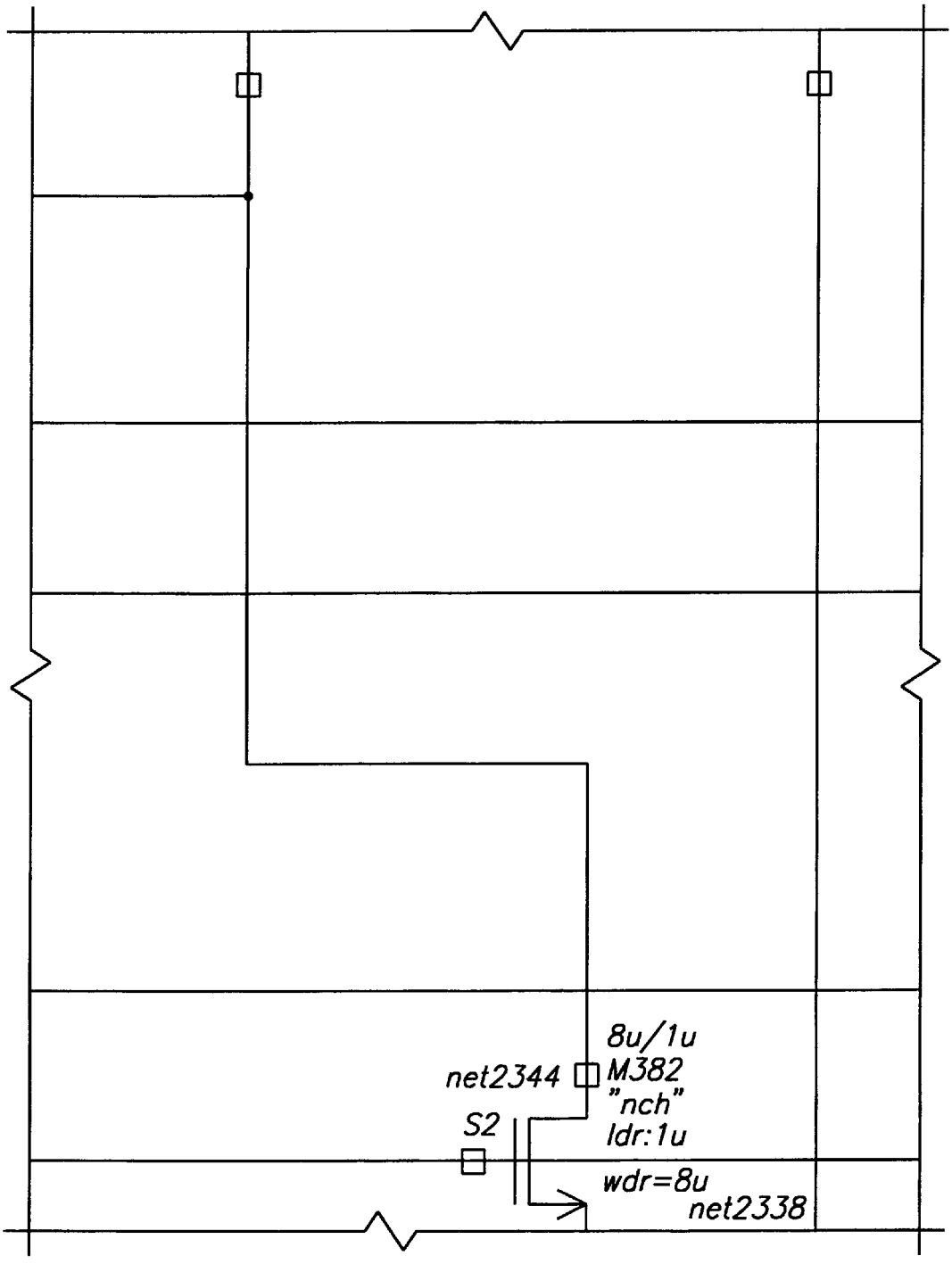


Fig 1,060,10E

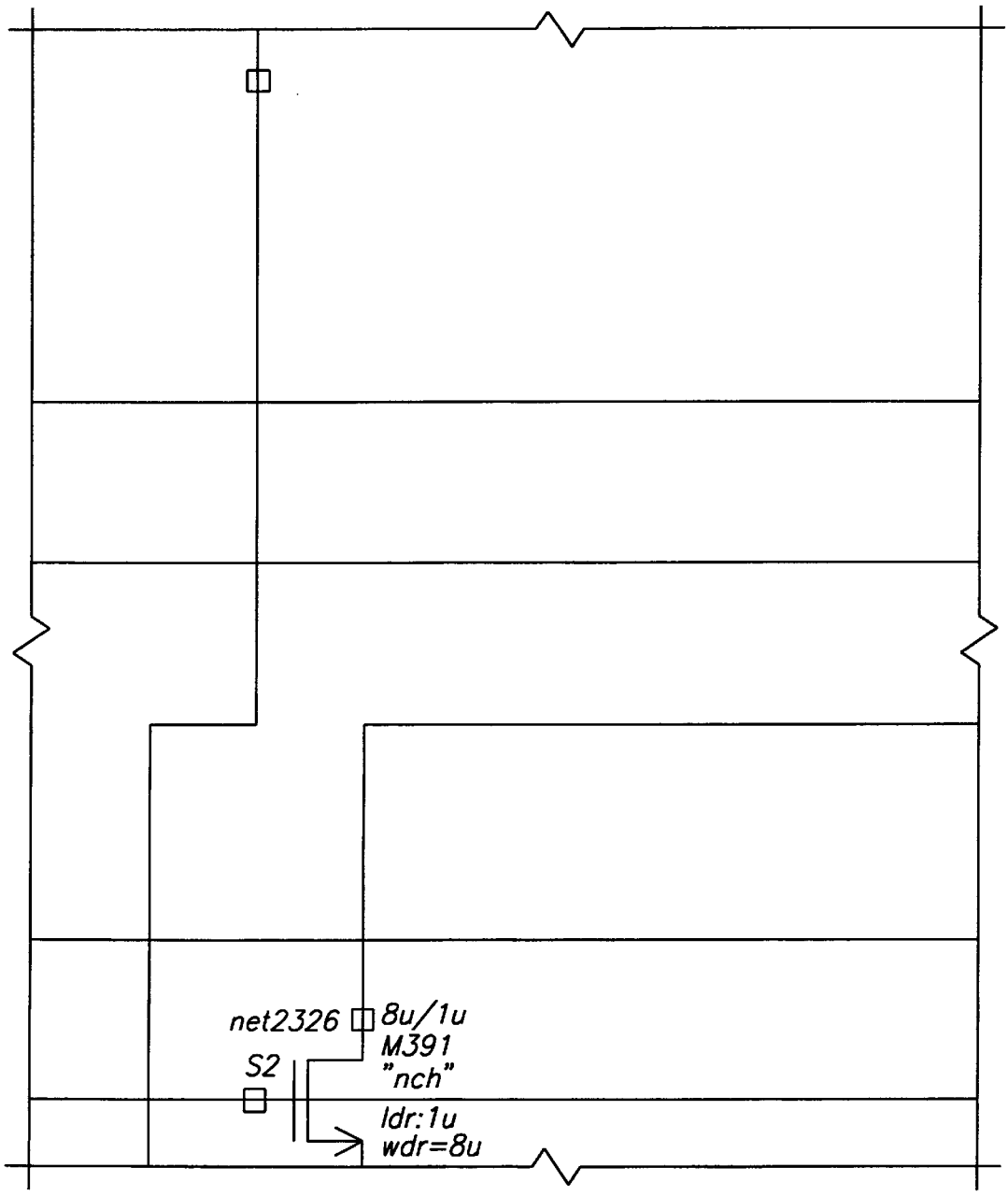


Fig 1.0601DF

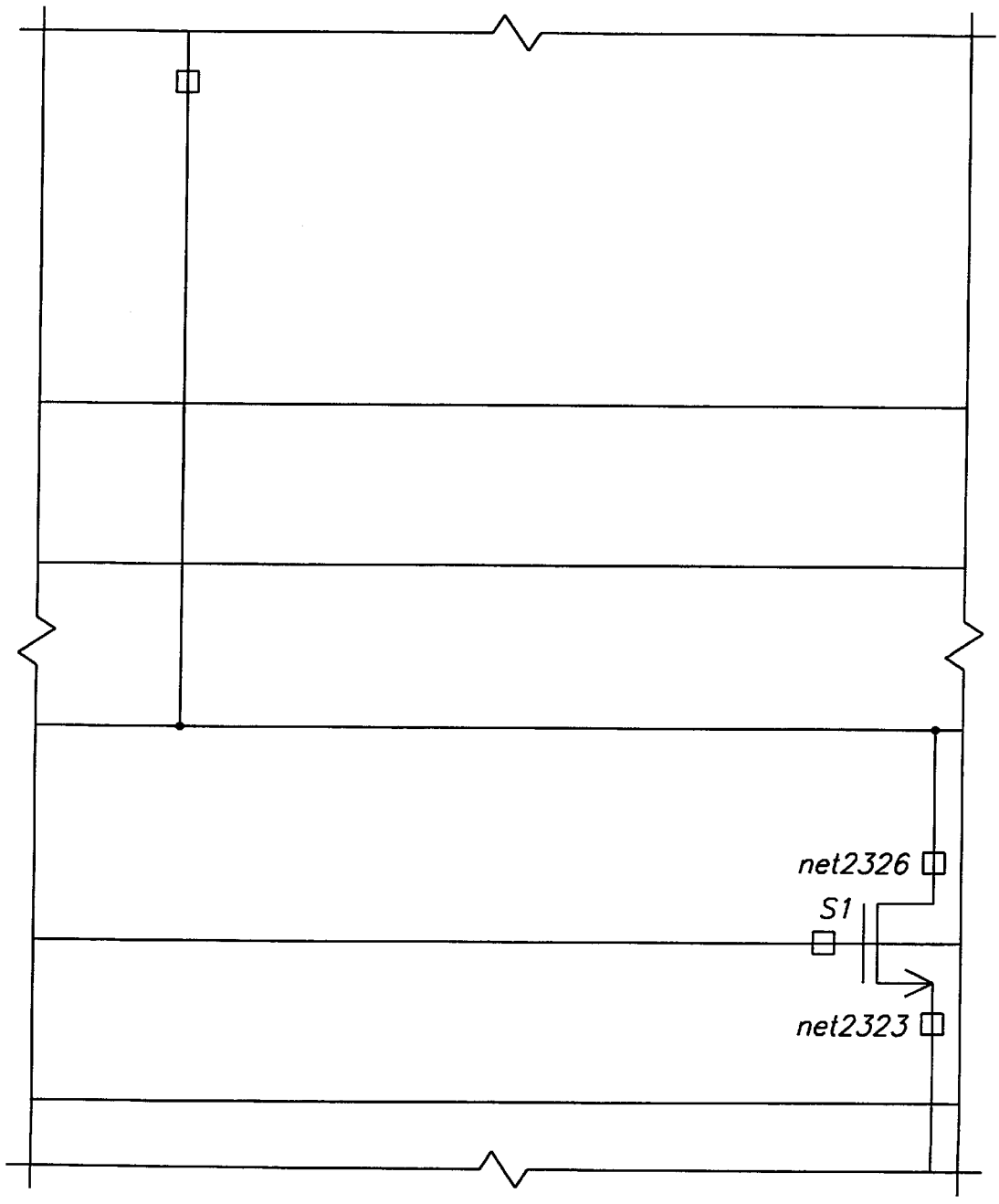


Fig 1.060106

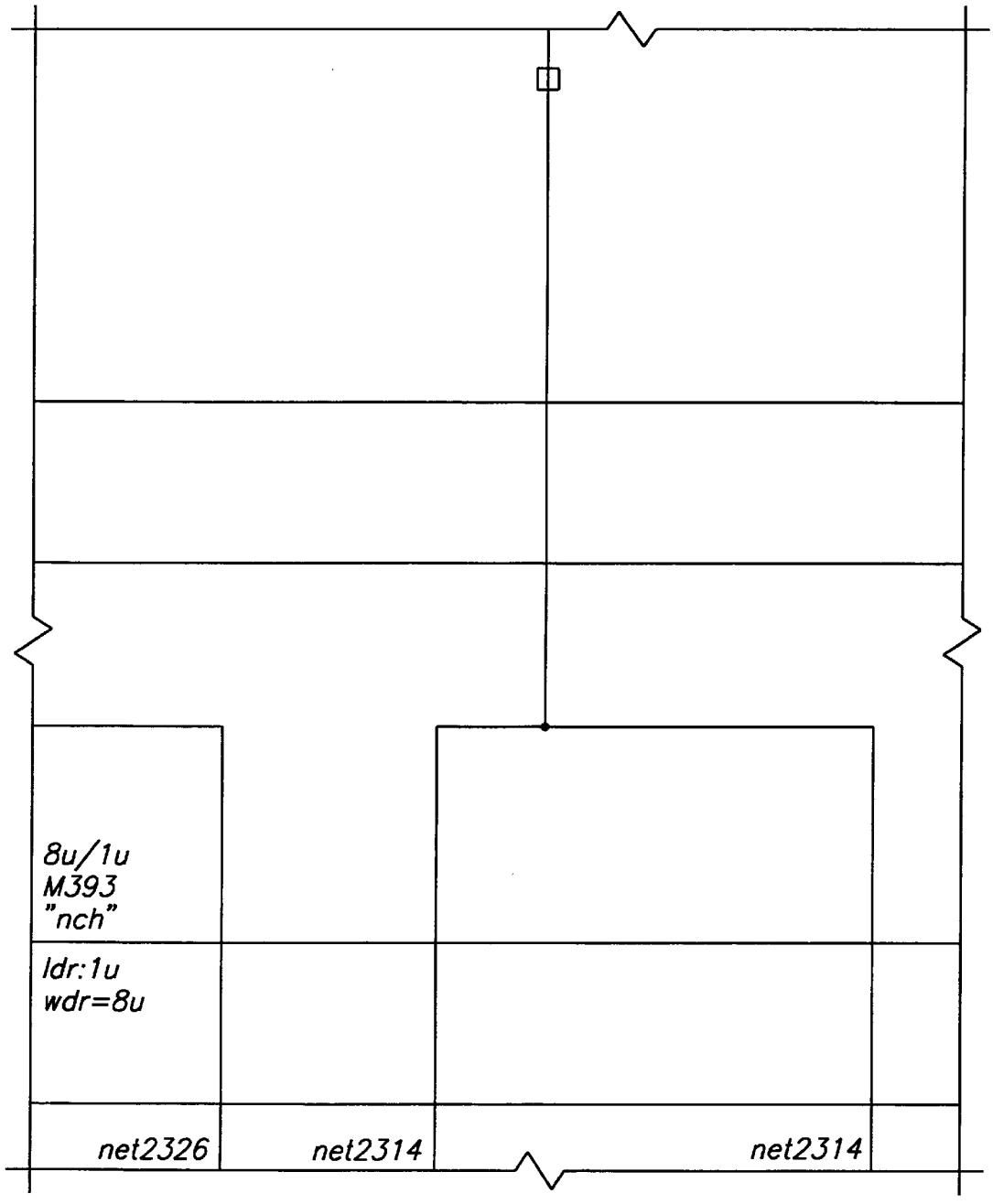


Fig 1.0601DH

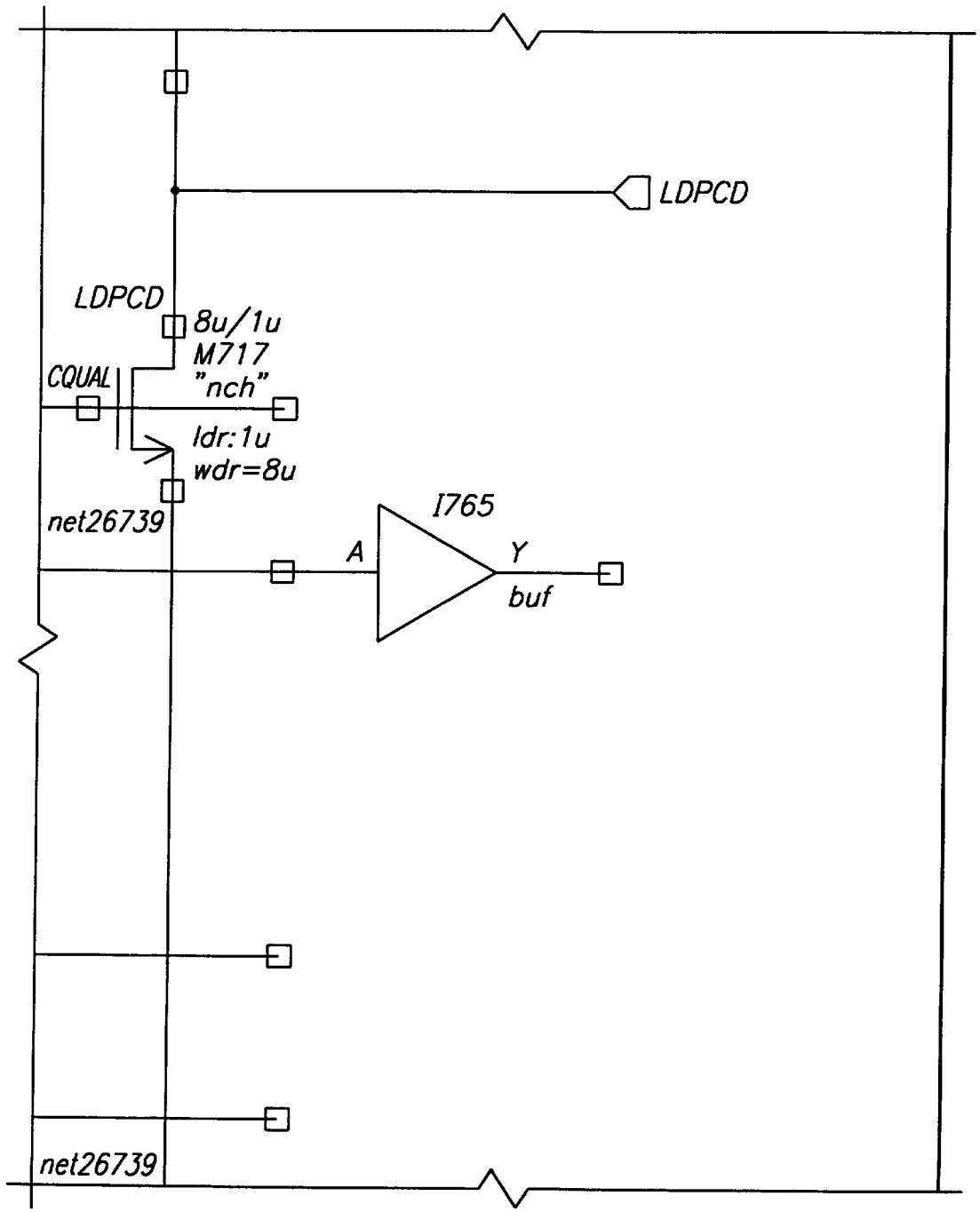

LDPCD
LDPCD
8u/1u
M717
"nch"
CQUAL
ldr:1u
wdr=8u
net26739
I765
A
Y
buf
net26739

Fig 1.060101

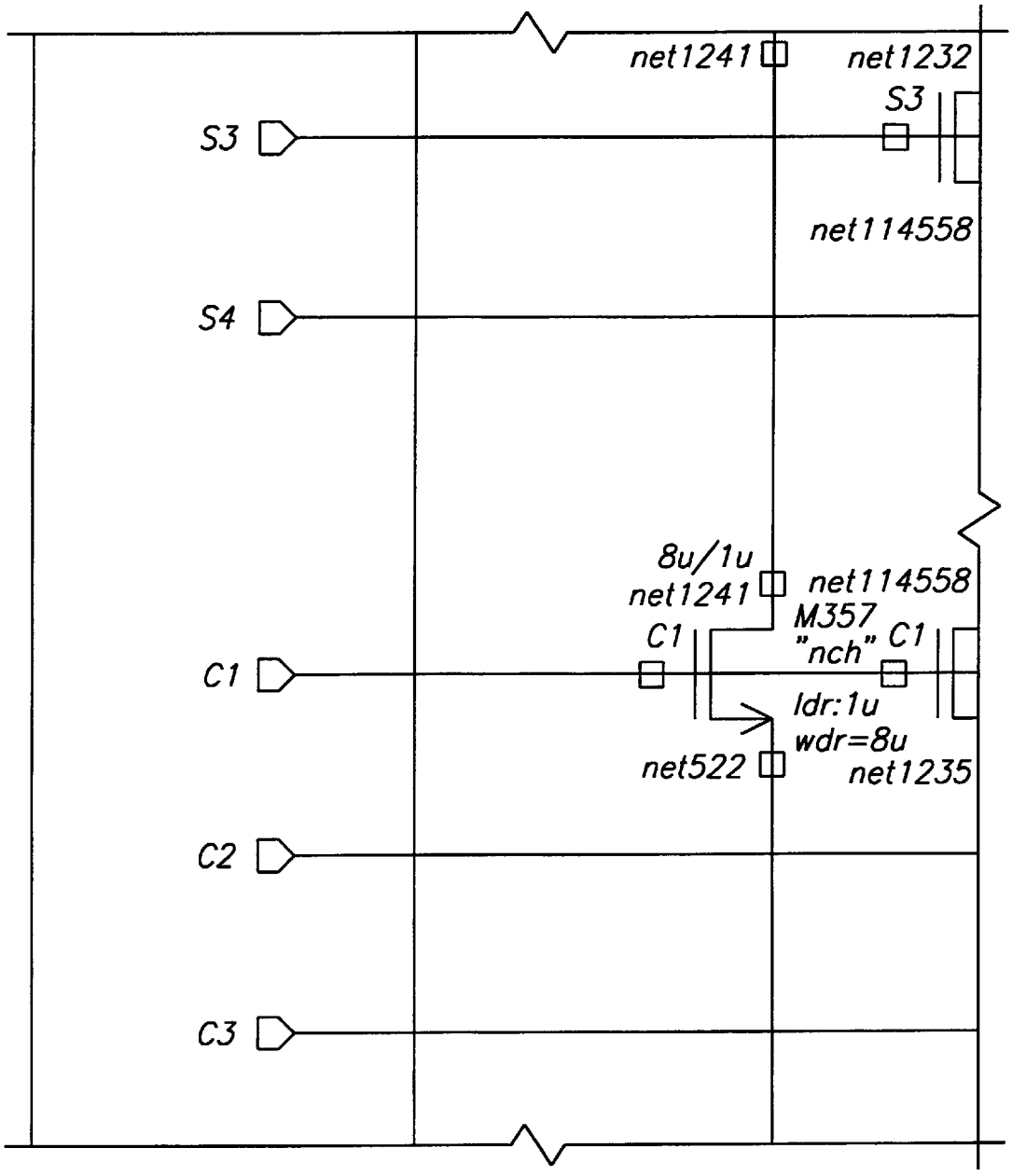

net1241
net1232
S3
S3
net114558
S4
8u/1u
net1241
net114558
M357
"nch"
C1
C1
C1
ldr:1u
wdr=8u
net522
net1235
C2
C3

Fig 1.0601EA

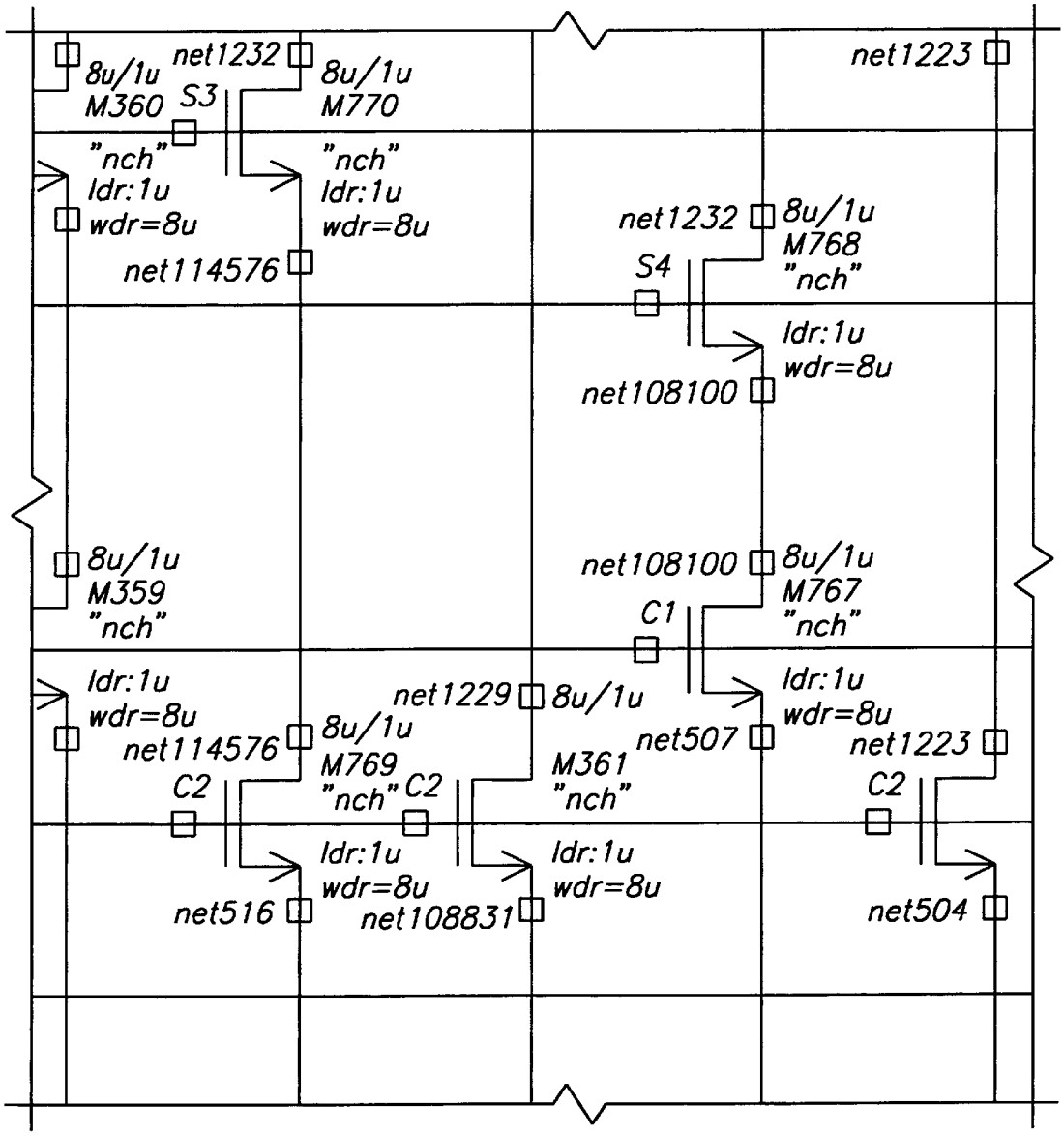

8u/1u
M360
net1232
S3
8u/1u
M770
net1223
"nch"
ldr:1u
wdr=8u
"nch"
ldr:1u
wdr=8u
net114576
net1232
8u/1u
M768
"nch"
S4
ldr:1u
wdr=8u
net108100
8u/1u
M359
"nch"
net108100
8u/1u
M767
"nch"
C1
ldr:1u
wdr=8u
net1229
8u/1u
M361
"nch"
net507
ldr:1u
wdr=8u
net1223
net114576
8u/1u
M769
"nch"
C2
C2
C2
ldr:1u
wdr=8u
ldr:1u
wdr=8u
net516
net108831
net504

Fig 1.0601EB

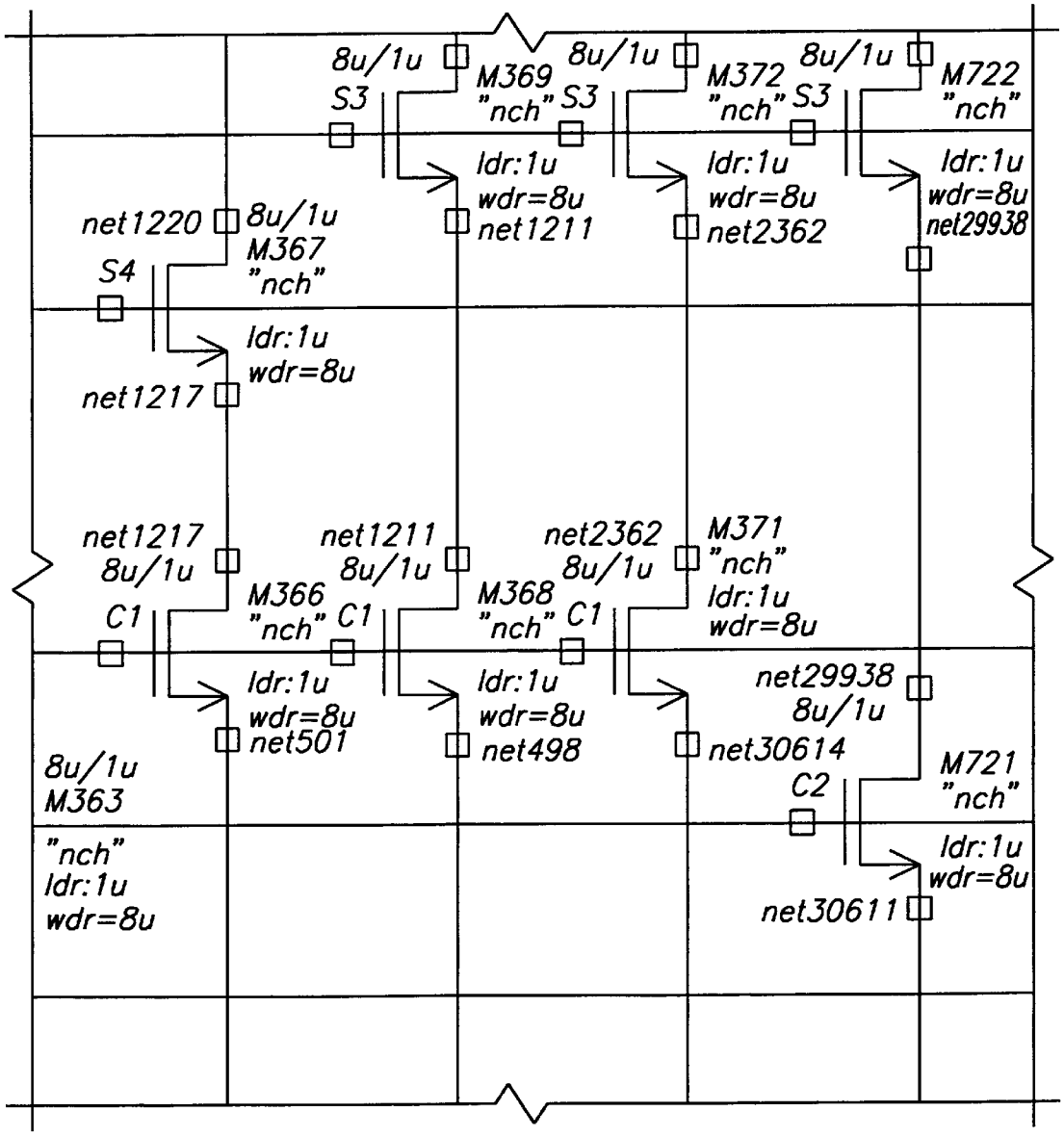
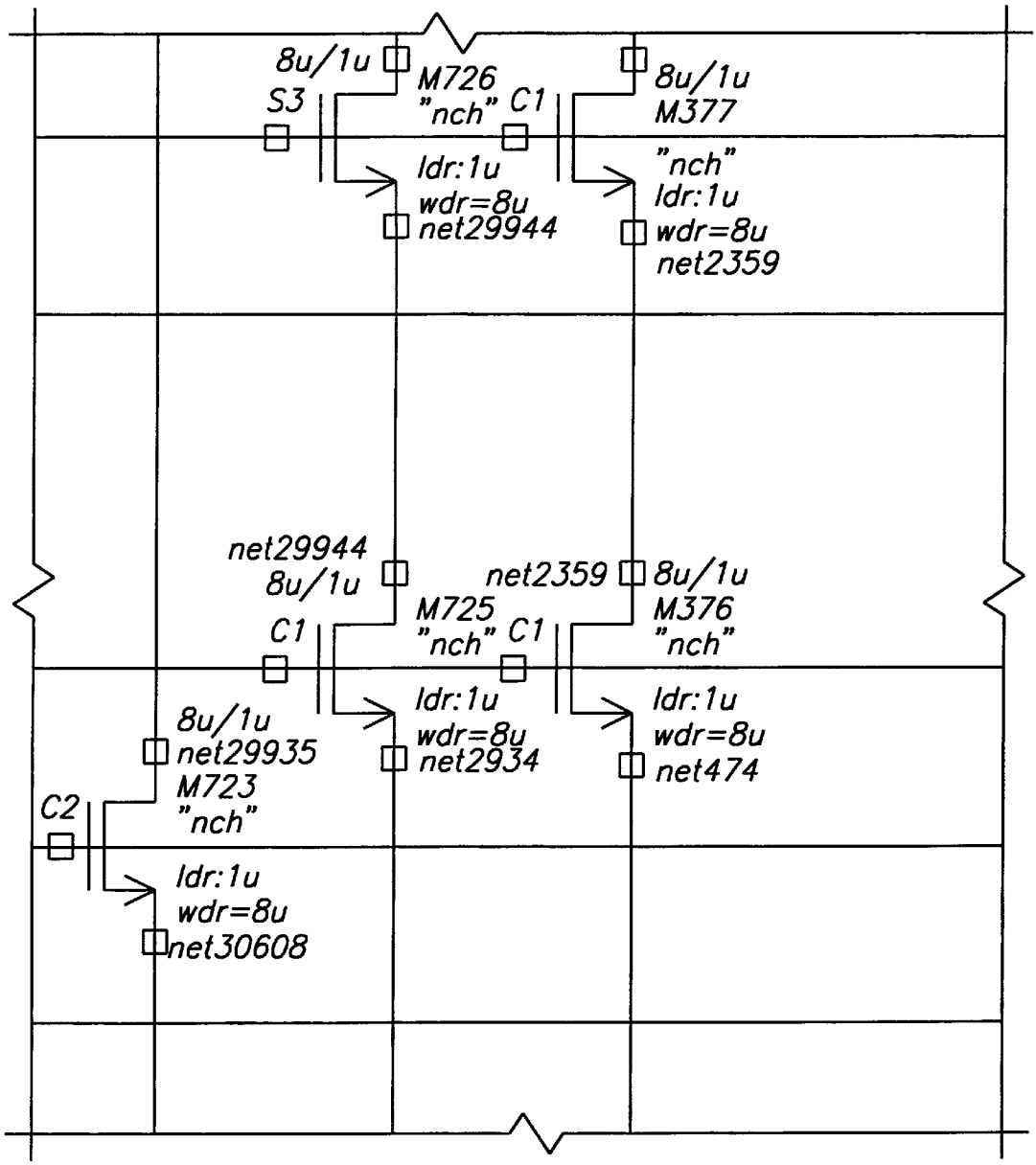


Fig 1.0600IEC


8u/1u
S3
M726
"nch"
C1
8u/1u
M377
ldr:1u
wdr=8u
net29944
"nch"
ldr:1u
wdr=8u
net2359
net29944
8u/1u
C1
M725
"nch"
C1
net2359
8u/1u
M376
"nch"
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wdr=8u
net2934
ldr:1u
wdr=8u
net474
8u/1u
net29935
M723
"nch"
C2
ldr:1u
wdr=8u
net30608

Fig 1.06UIED

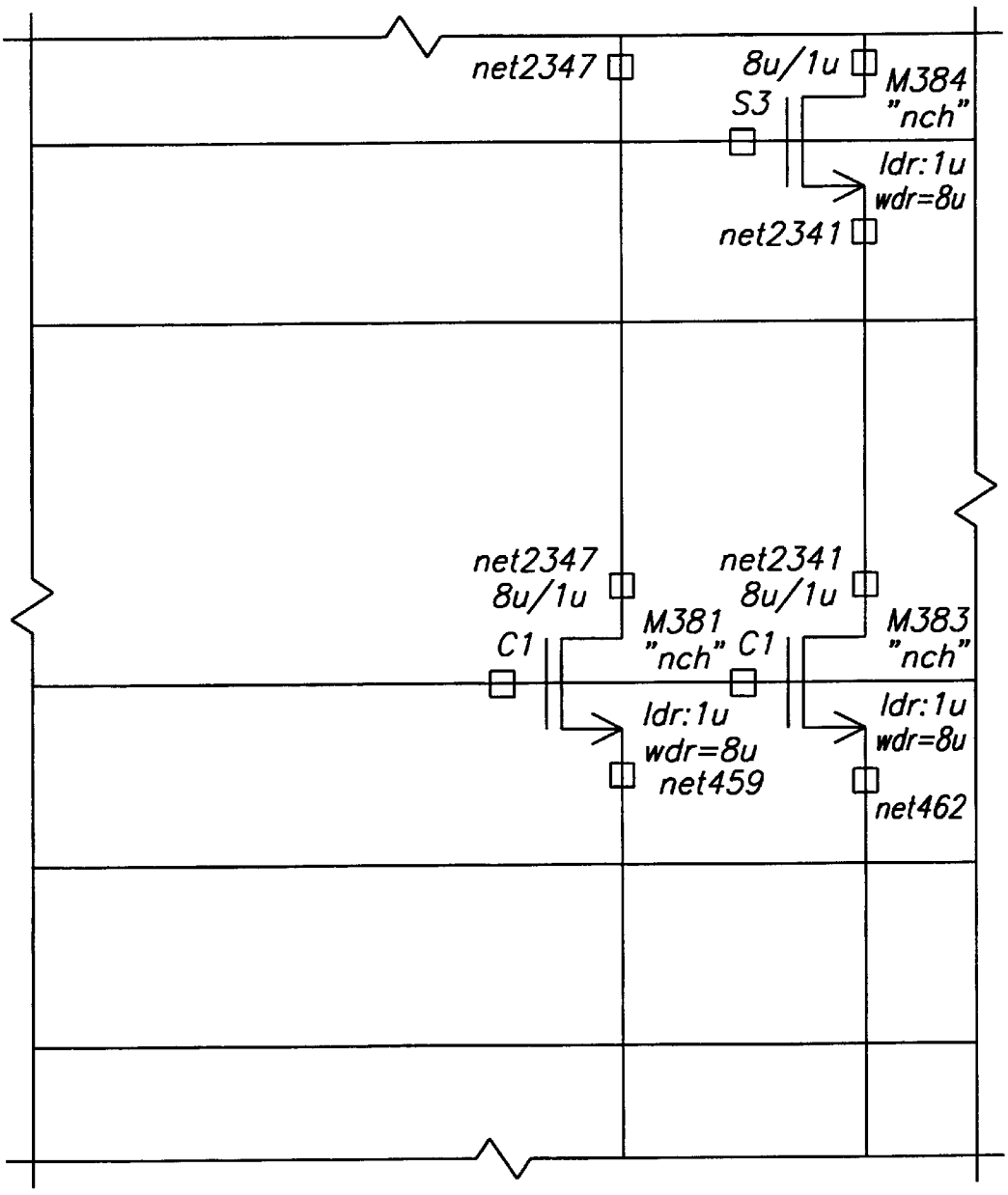

net2347
8u/1u
M384
"nch"
S3
ldr:1u
wdr=8u
net2341
net2347
8u/1u
M381
"nch"
C1
net2341
8u/1u
C1
M383
"nch"
ldr:1u
wdr=8u
net459
ldr:1u
wdr=8u
net462

FIG. 1,060,116

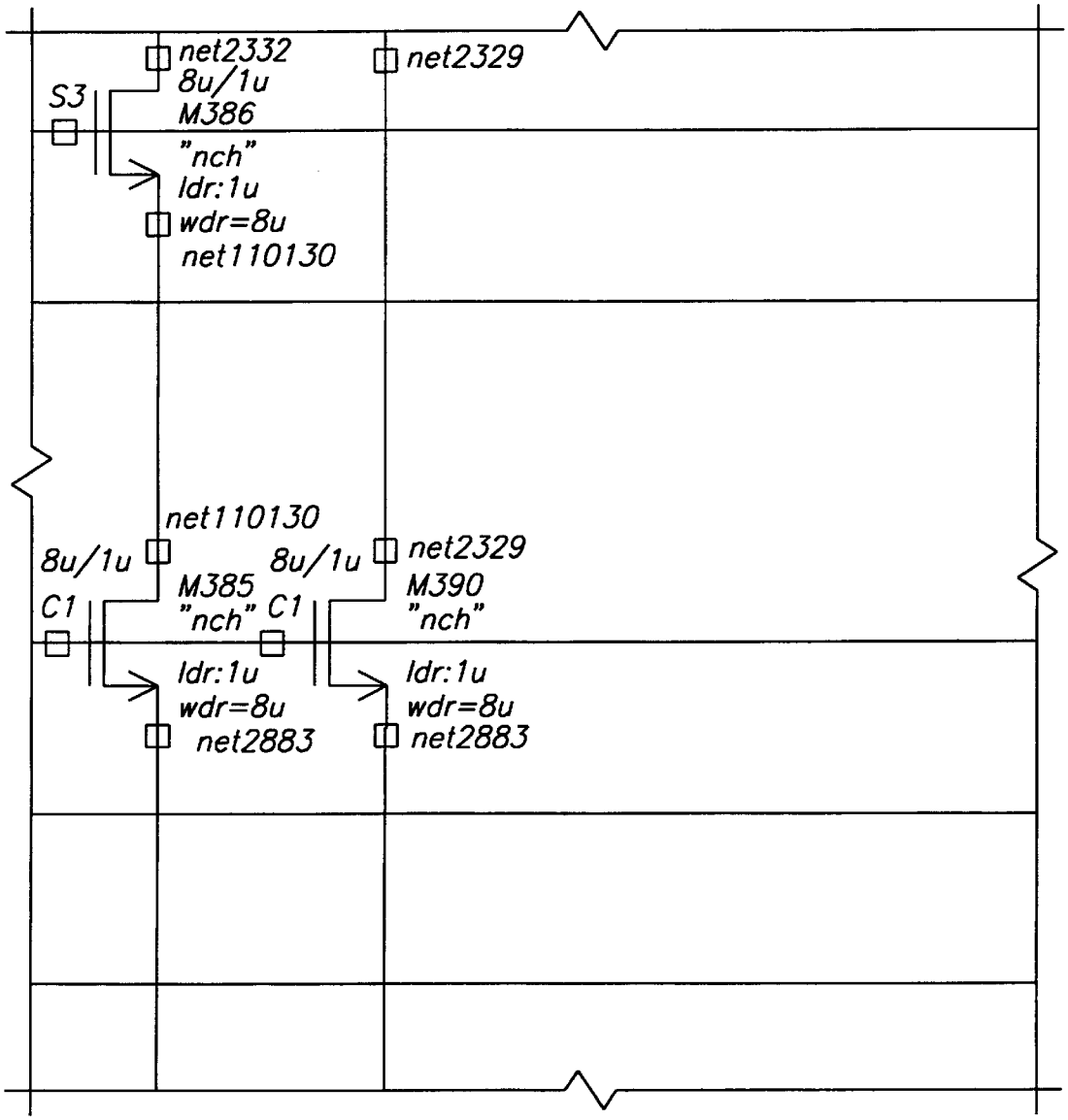

net2332
8u/1u
M386
"nch"
ldr:1u
wdr=8u
net110130
S3
net2329
net110130
8u/1u
C1
M385
"nch"
ldr:1u
wdr=8u
net2883
8u/1u
C1
net2329
M390
"nch"
ldr:1u
wdr=8u
net2883

Fig 1.060IEF

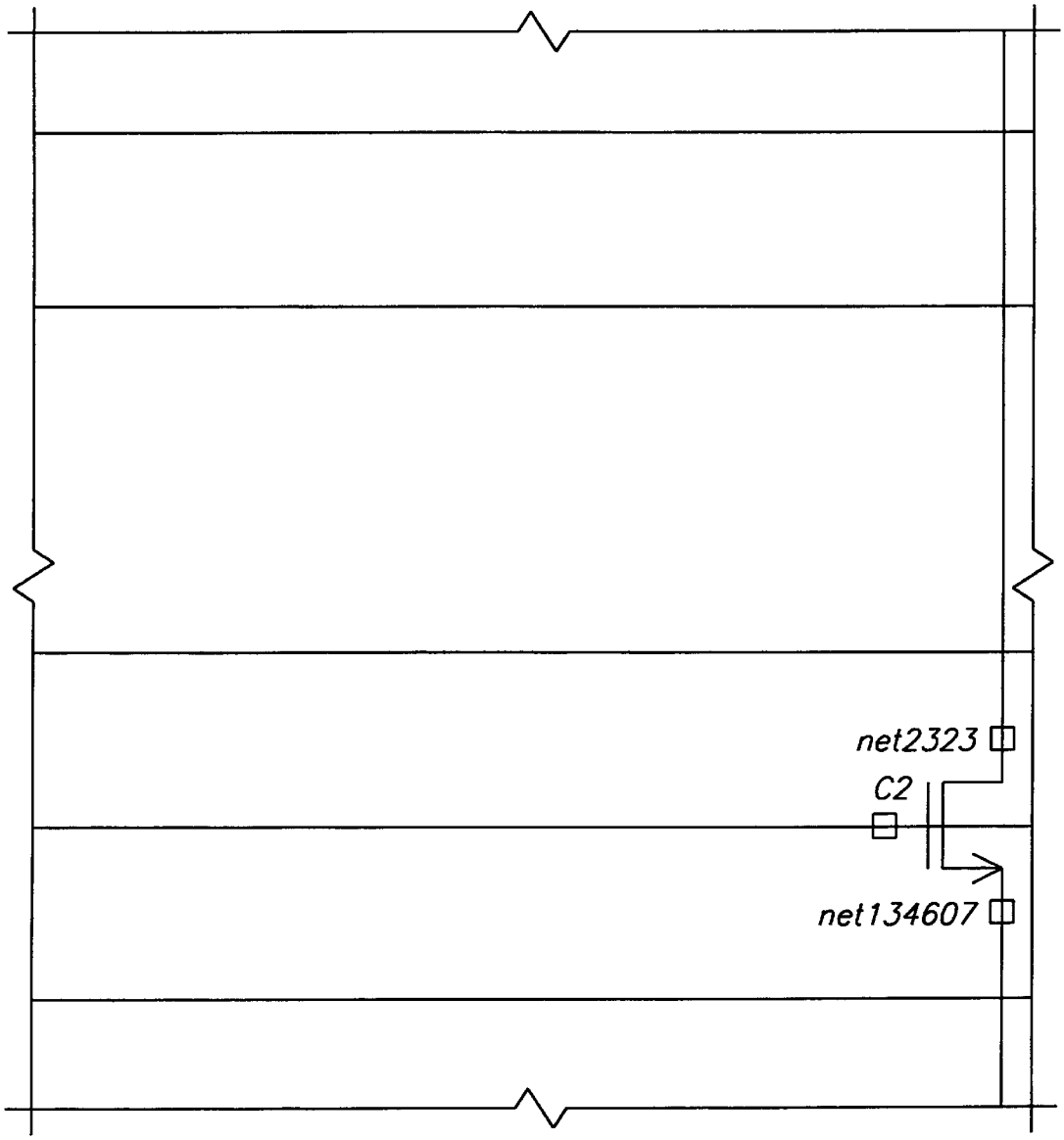


Fig 7.0601EG

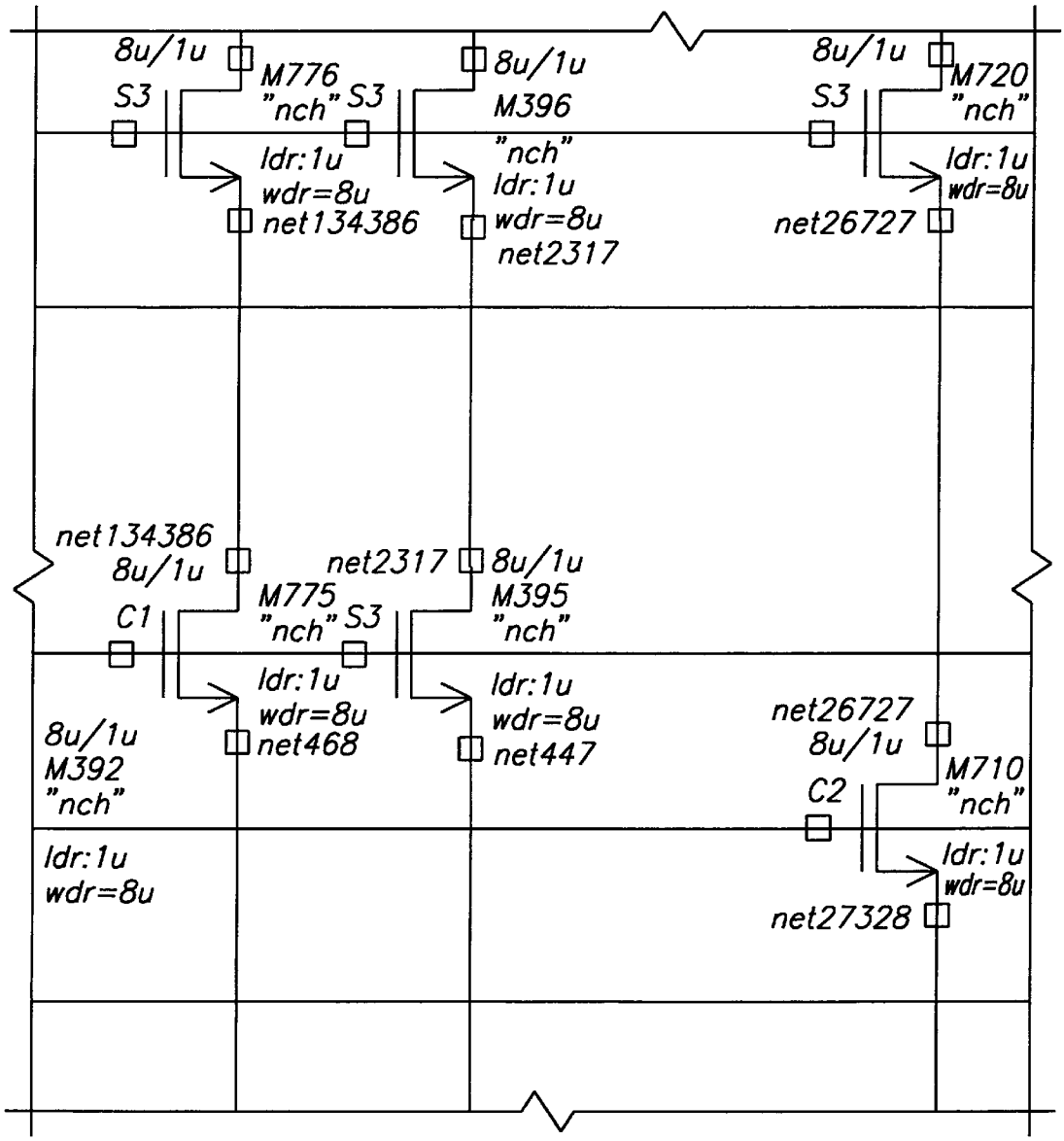

8u/1u
M776
"nch"
S3
S3
ldr:1u
wdr=8u
net134386
8u/1u
M396
"nch"
ldr:1u
wdr=8u
net2317
8u/1u
M720
"nch"
S3
ldr:1u
wdr=8u
net26727
net134386
8u/1u
C1
M775
"nch"
S3
net2317
8u/1u
M395
"nch"
ldr:1u
wdr=8u
net468
ldr:1u
wdr=8u
net447
8u/1u
M392
"nch"
ldr:1u
wdr=8u
net26727
8u/1u
C2
M710
"nch"
ldr:1u
wdr=8u
net27328

FIG 1.0601EH

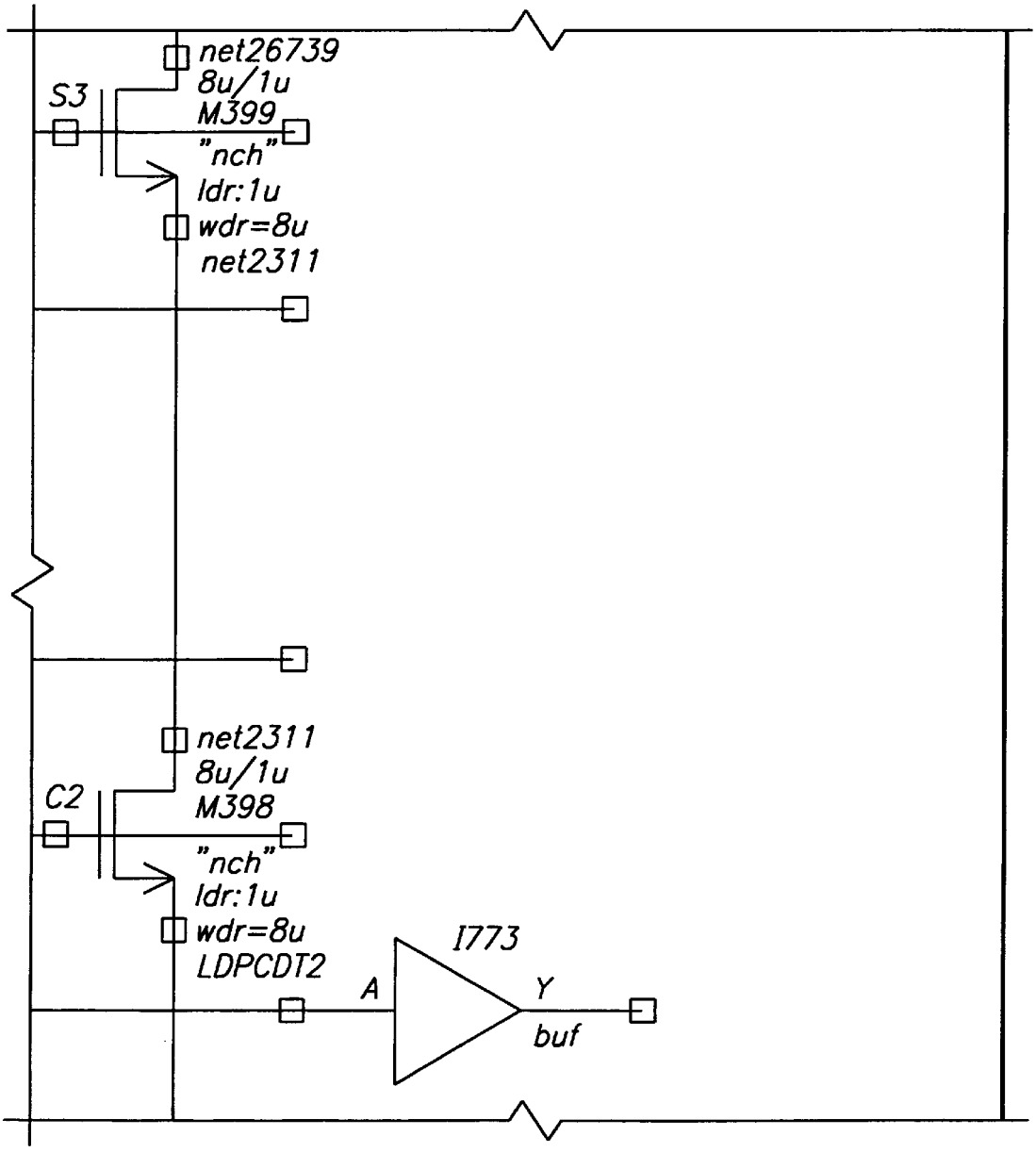

net26739
8u/1u
M399
"nch"
ldr:1u
wdr=8u
net2311
S3
net2311
8u/1u
M398
"nch"
ldr:1u
wdr=8u
LDPCDT2
C2
I773
A
Y
buf

FIG. 1.06(11)

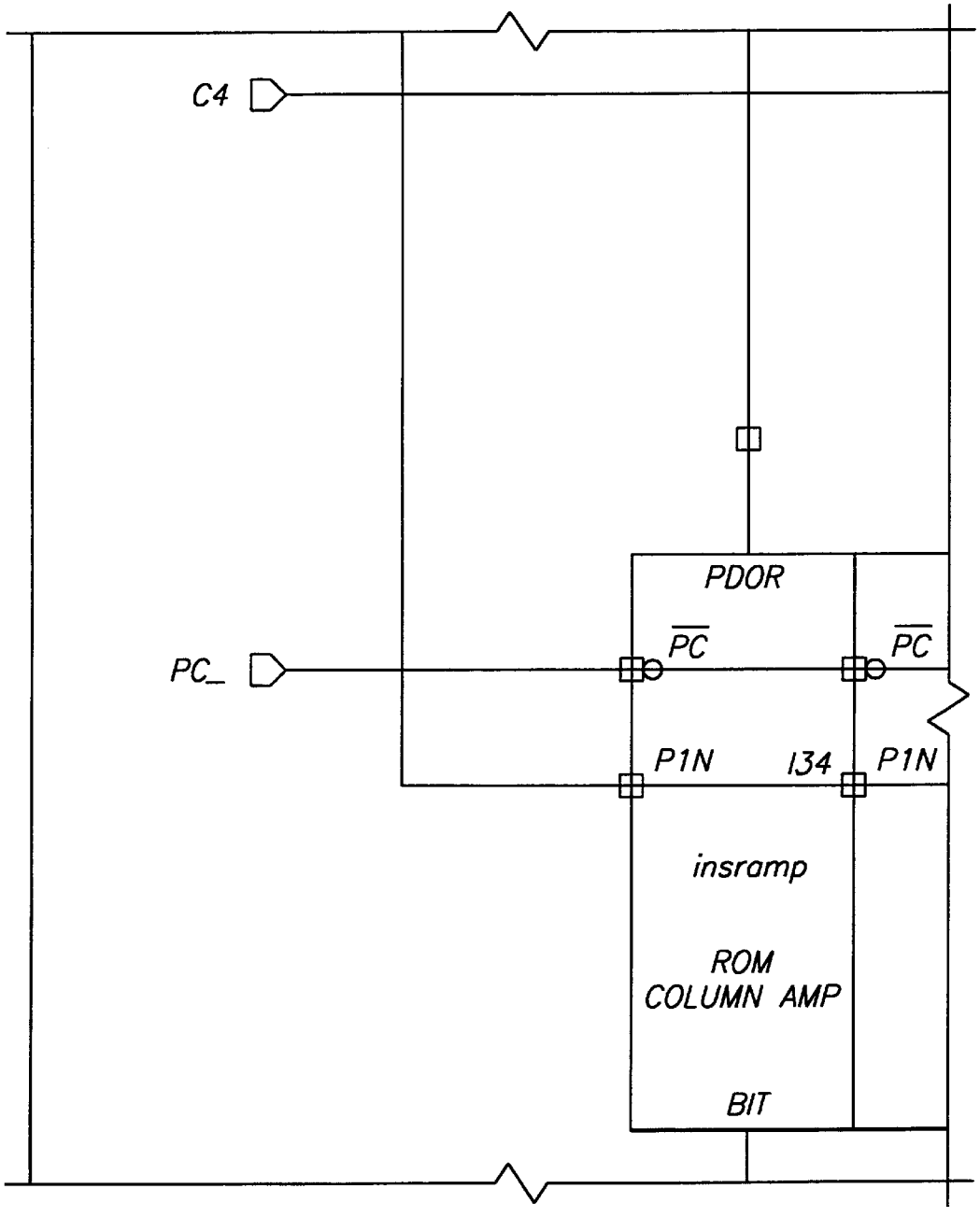


Fig 1.06011A

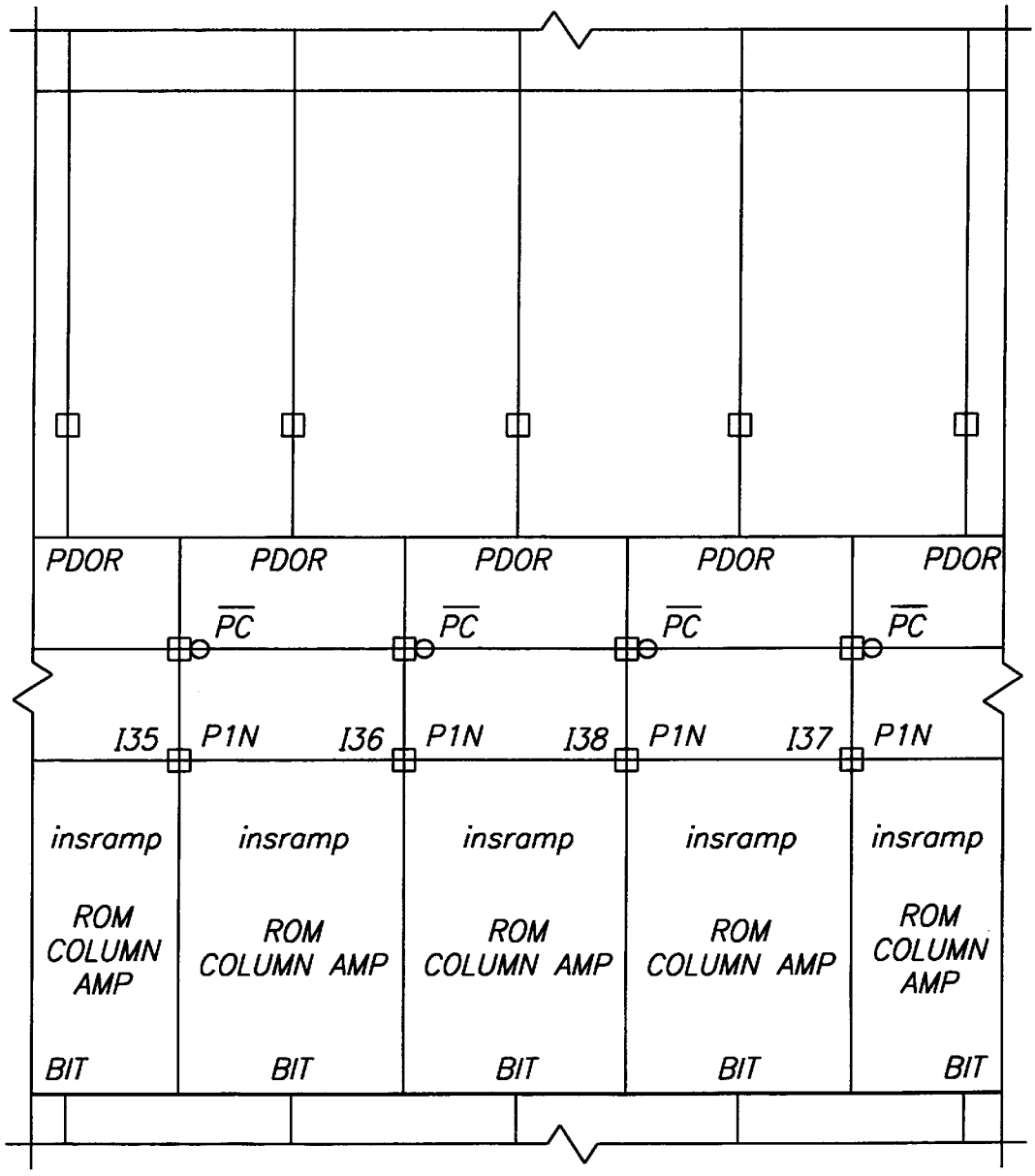

PDOR
PDOR
PDOR
PDOR
PDOR
PC
PC
PC
PC
I35
P1N
I36
P1N
I38
P1N
I37
P1N
insramp
insramp
insramp
insramp
insramp
ROM COLUMN AMP
ROM COLUMN AMP
ROM COLUMN AMP
ROM COLUMN AMP
ROM COLUMN AMP
BIT
BIT
BIT
BIT
BIT

Fig 1.0601FB

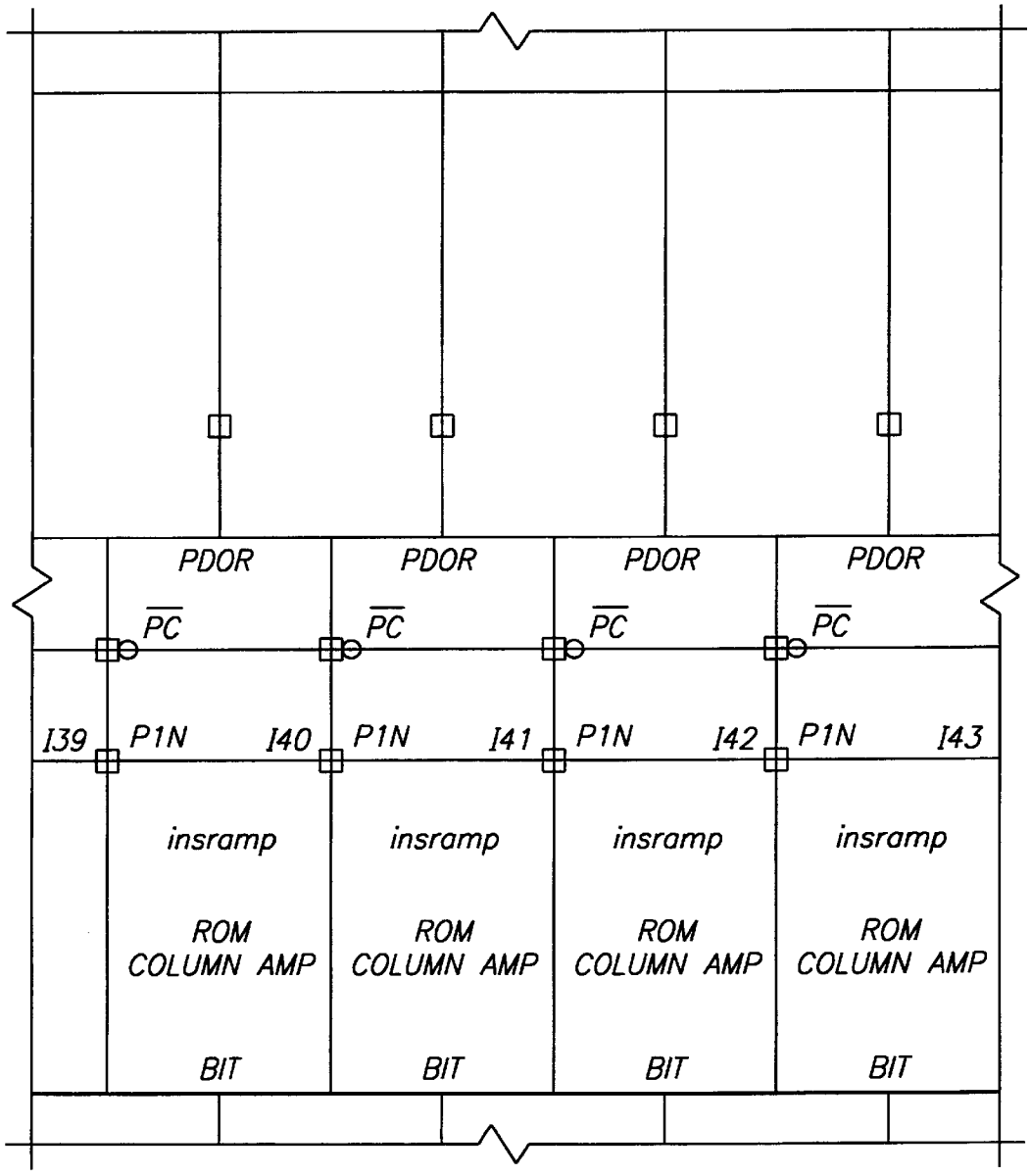


Fig 1.06011FC

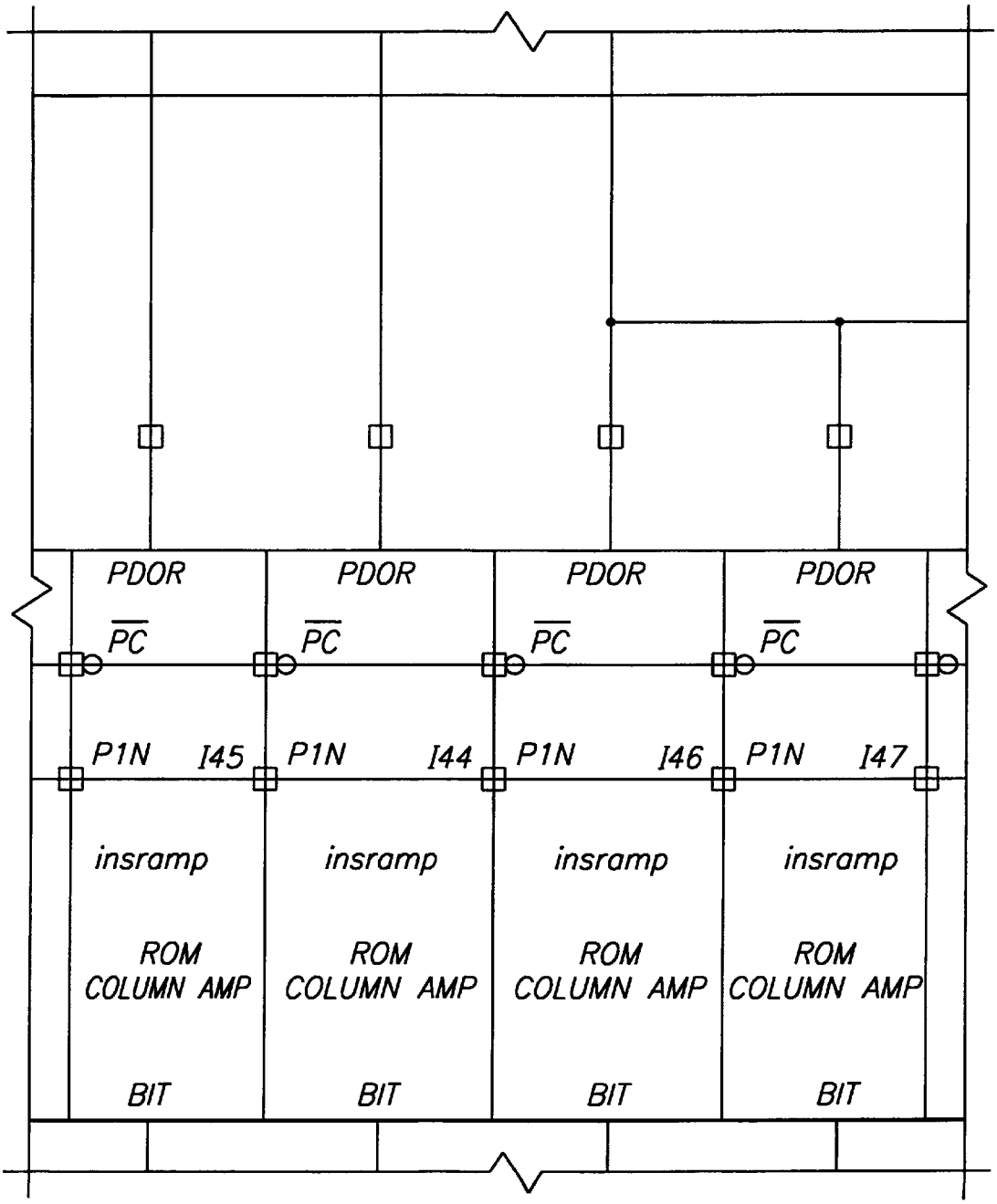

PDOR
PDOR
PDOR
PDOR
$\overline{PC}$
$\overline{PC}$
$\overline{PC}$
$\overline{PC}$
P1N
I45
P1N
I44
P1N
I46
P1N
I47
insramp
insramp
insramp
insramp
ROM
COLUMN AMP
ROM
COLUMN AMP
ROM
COLUMN AMP
ROM
COLUMN AMP
BIT
BIT
BIT
BIT

Fig 1.0601FD

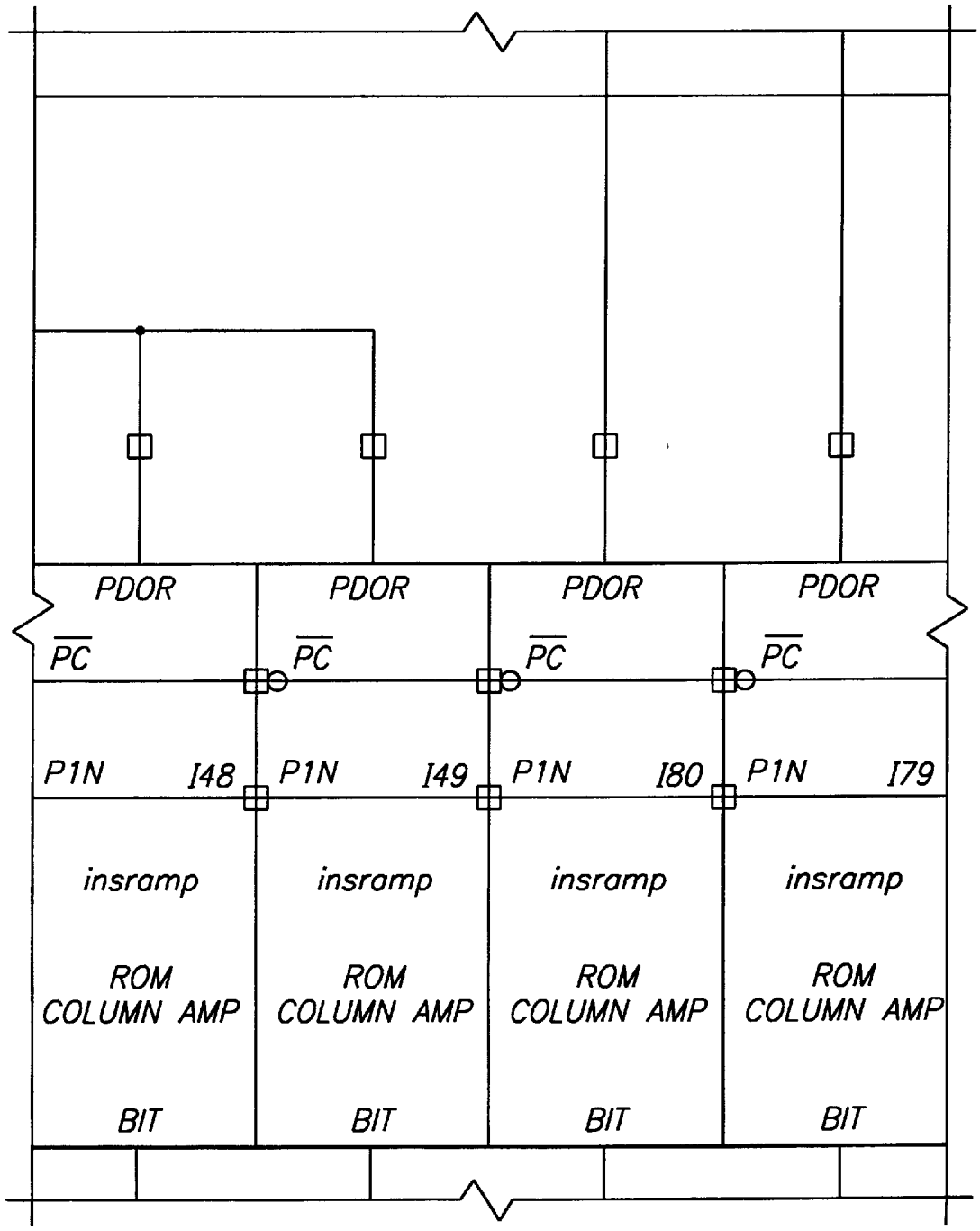


Fig 1.060ILFE

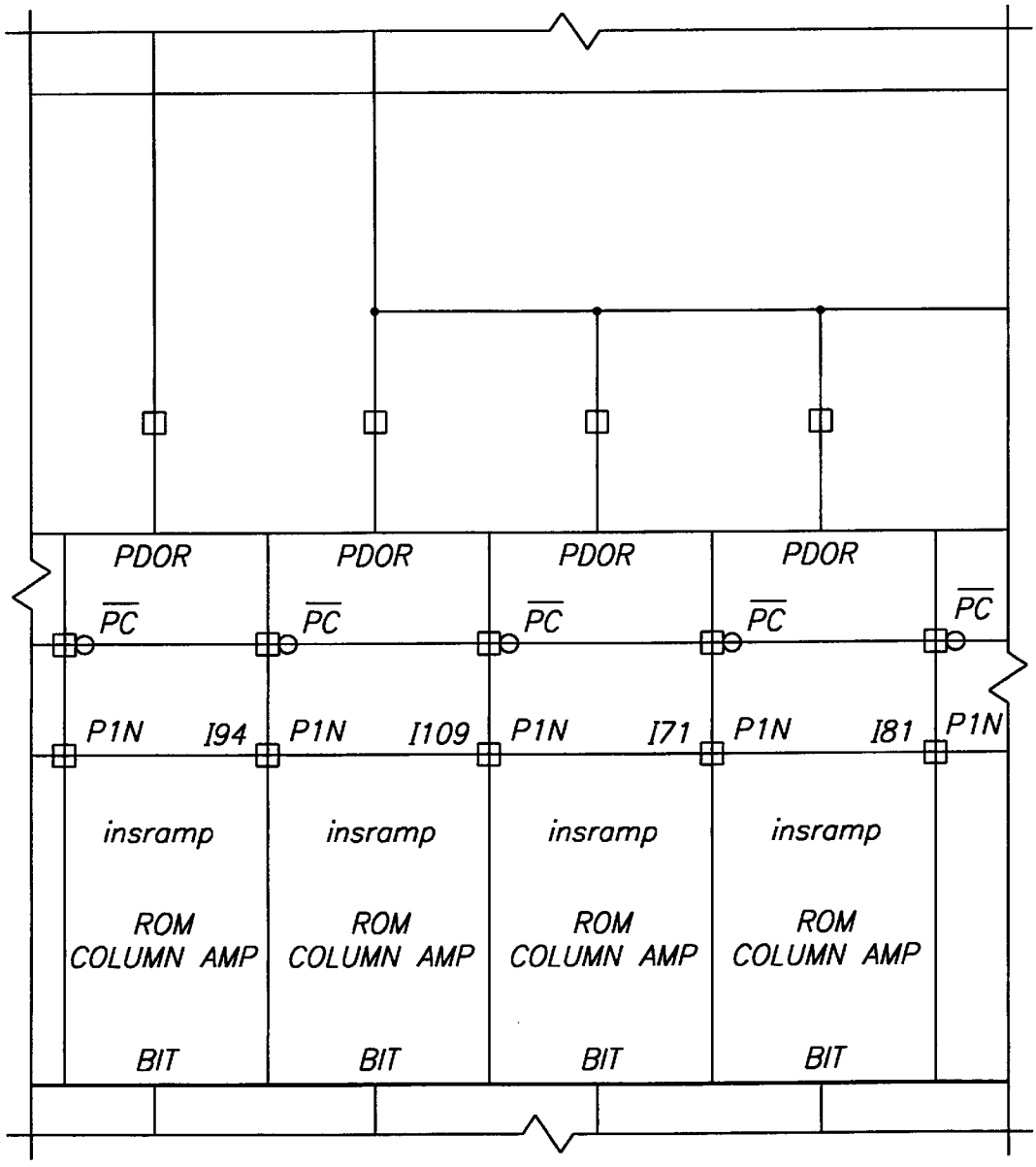

PDOR
PDOR
PDOR
PDOR
$\overline{PC}$
$\overline{PC}$
$\overline{PC}$
$\overline{PC}$
$\overline{PC}$
P1N
I94
P1N
I109
P1N
I71
P1N
I81
P1N
insramp
insramp
insramp
insramp
ROM
COLUMN AMP
ROM
COLUMN AMP
ROM
COLUMN AMP
ROM
COLUMN AMP
BIT
BIT
BIT
BIT

Fig 1.0600IF

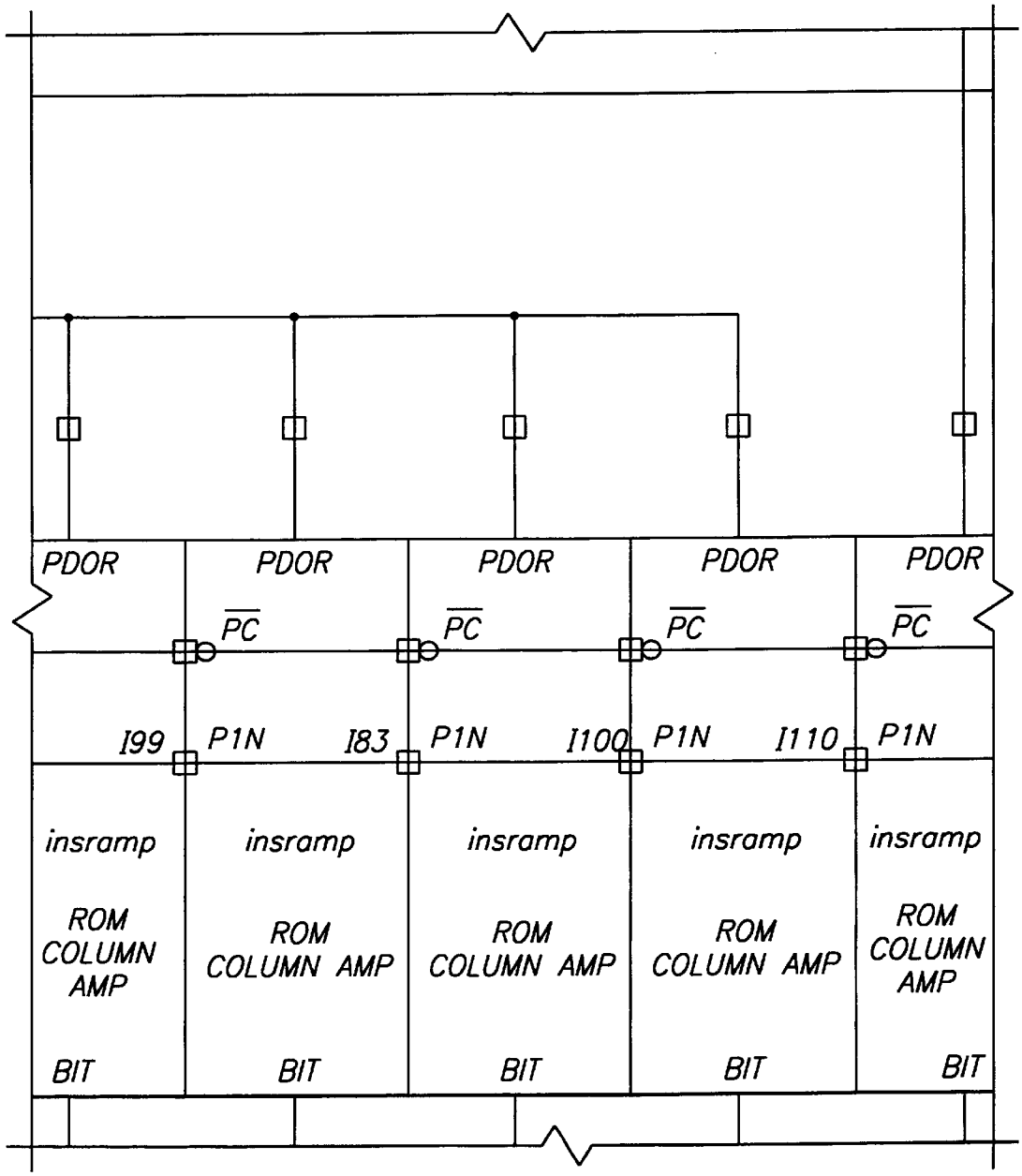


Fig 1.06011F6

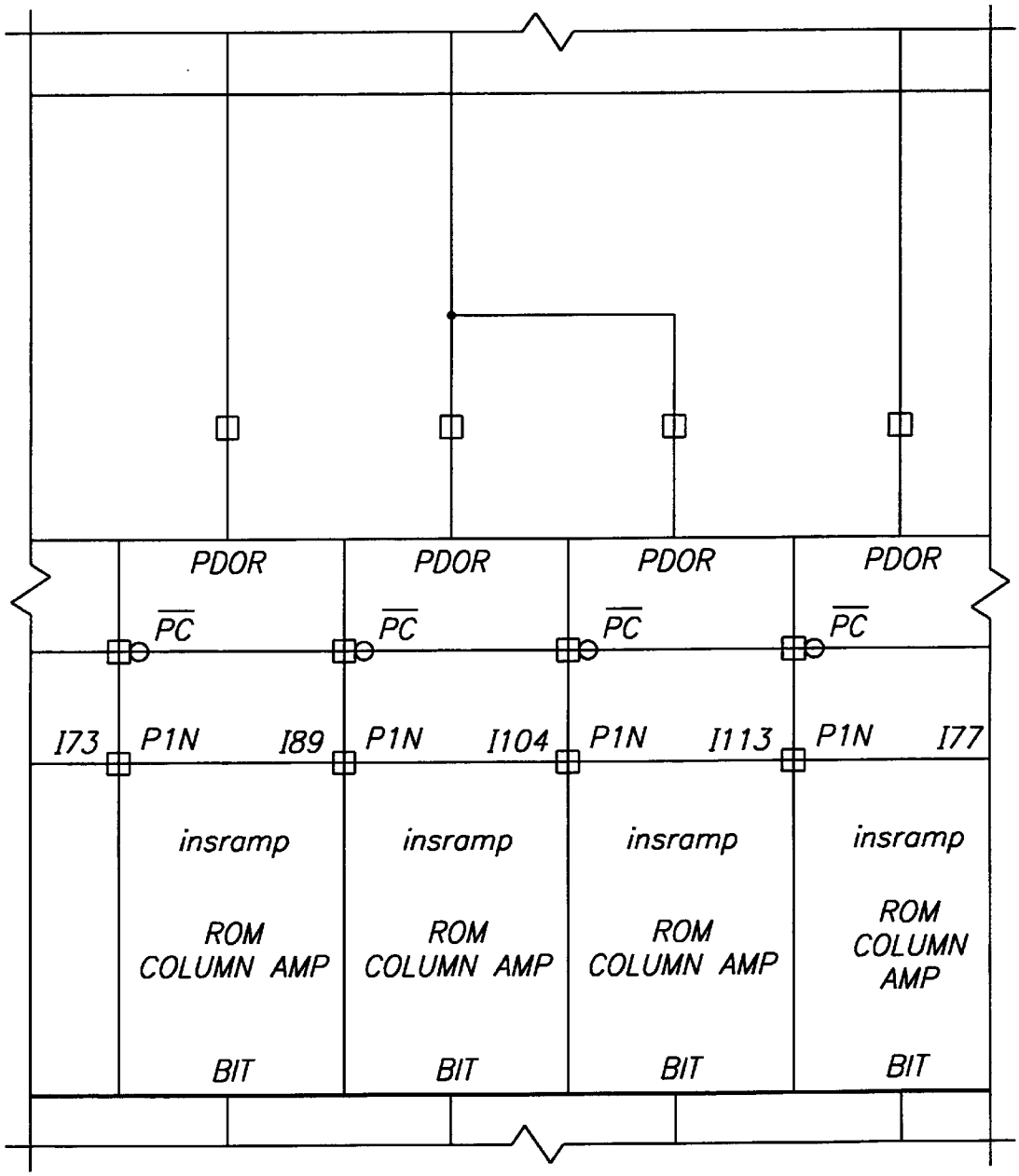

PDOR
PDOR
PDOR
PDOR
PC
PC
PC
PC
I73
P1N
I89
P1N
I104
P1N
I113
P1N
I77
insramp
insramp
insramp
insramp
ROM
COLUMN AMP
ROM
COLUMN AMP
ROM
COLUMN AMP
ROM
COLUMN
AMP
BIT
BIT
BIT
BIT

Fig 1.0601FH

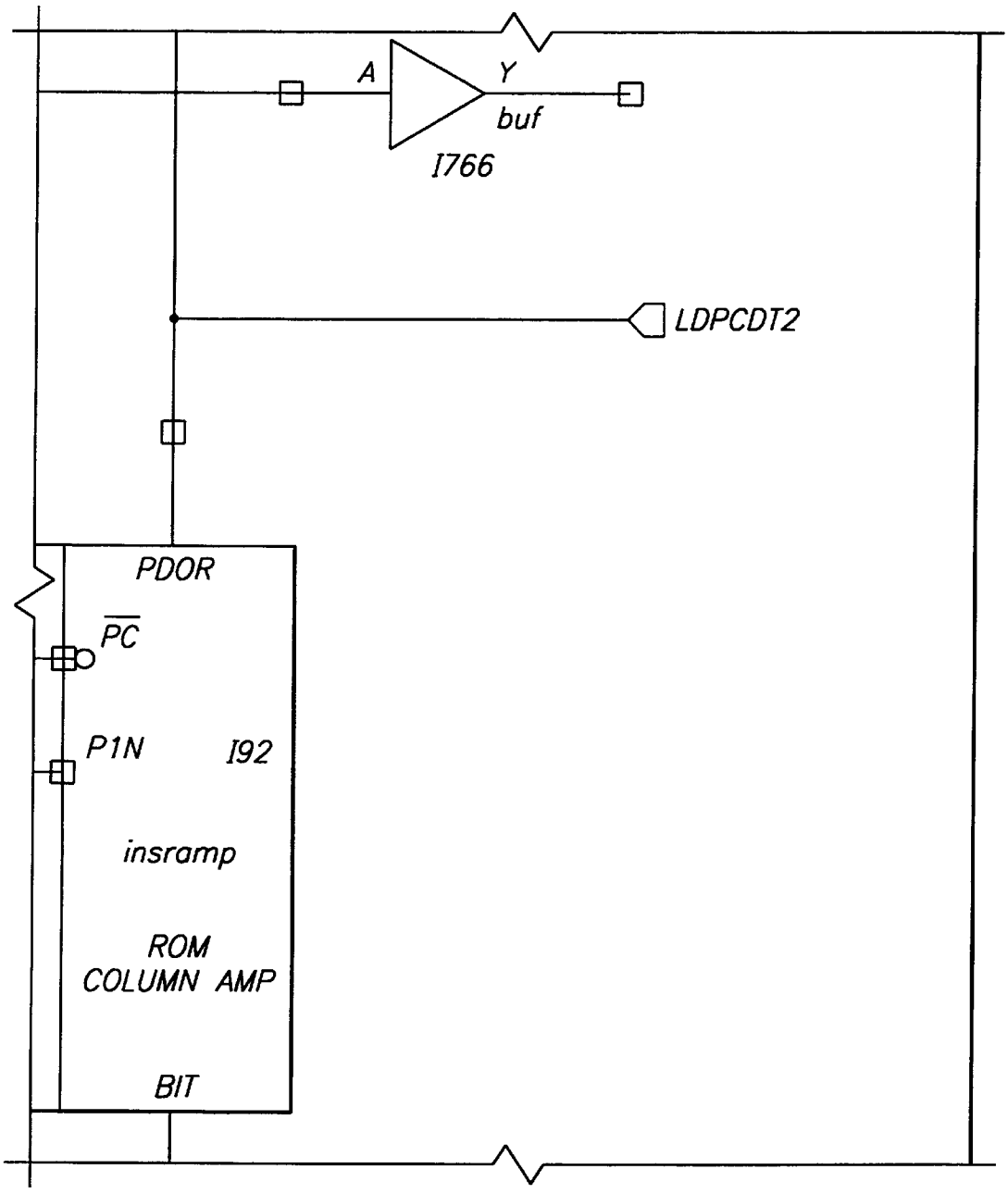

A
Y
buf
I766
LDPCDT2
PDOR
PC
P1N
I92
insramp
ROM
COLUMN AMP
BIT

Fig 1.0601F1

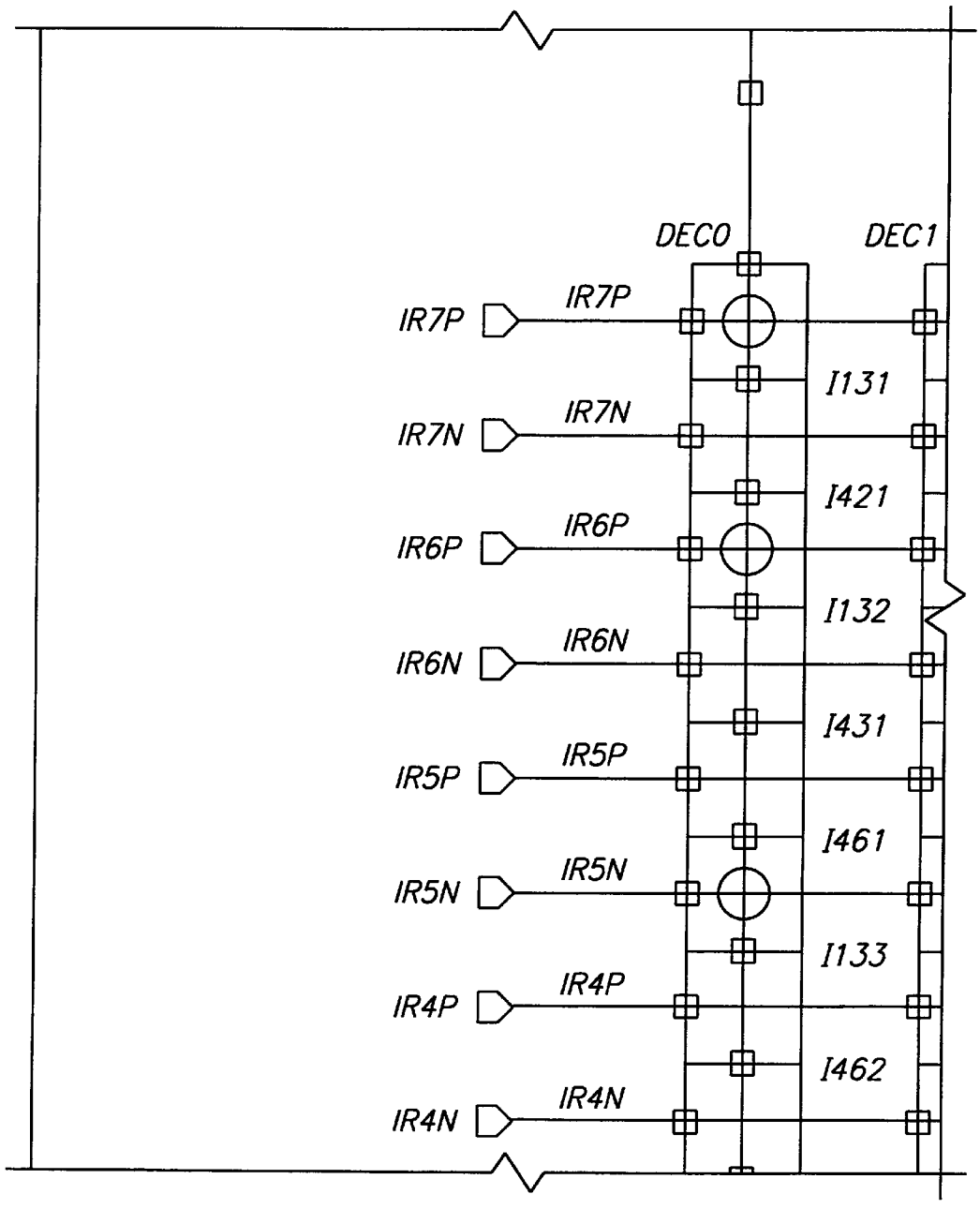

DEC0
DEC1
IR7P
IR7P
I131
IR7N
IR7N
I421
IR6P
IR6P
I132
IR6N
IR6N
I431
IR5P
IR5P
I461
IR5N
IR5N
I133
IR4P
IR4P
I462
IR4N
IR4N

Fig 1.06010A

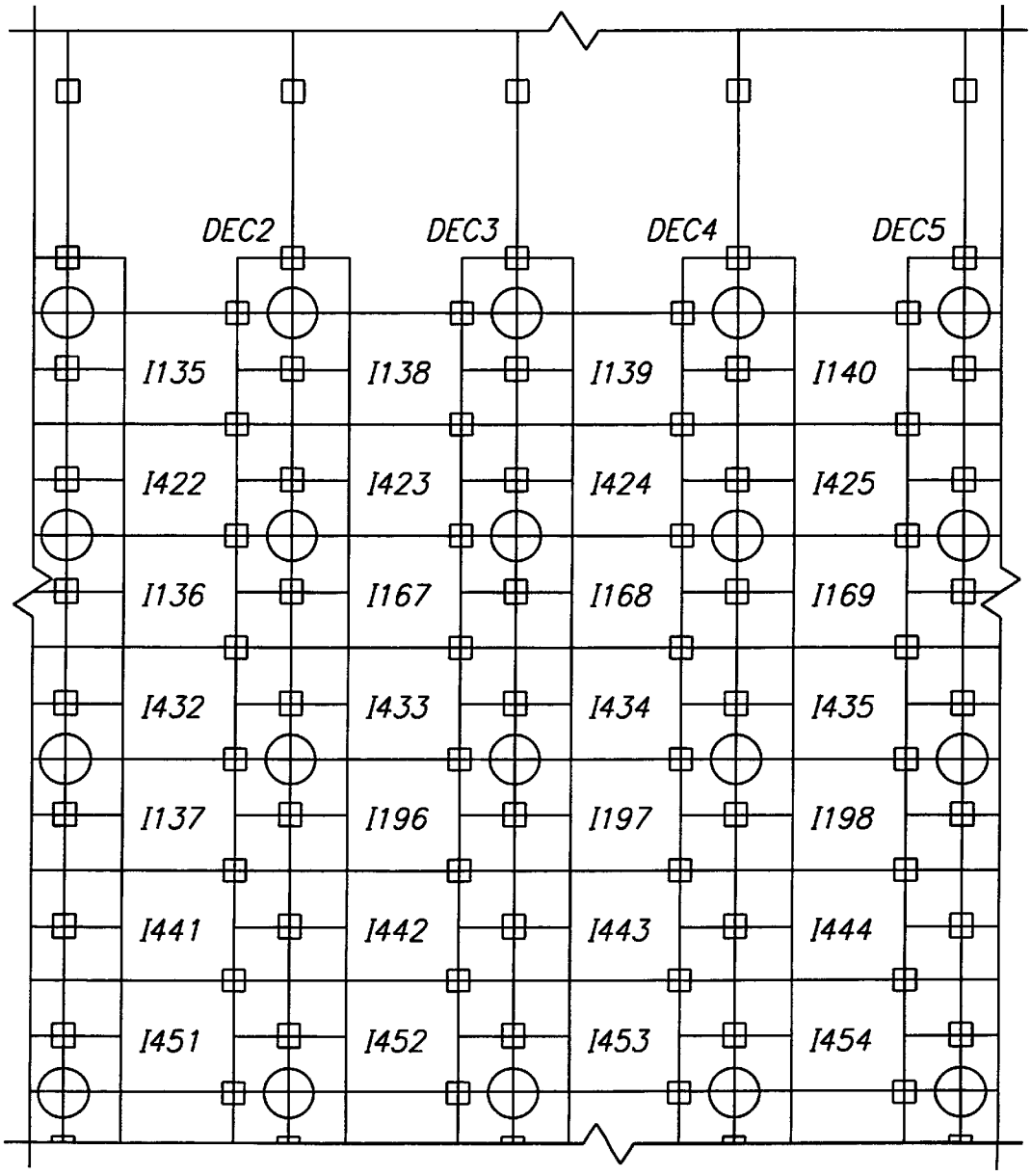

DEC2
DEC3
DEC4
DEC5
I135
I138
I139
I140
I422
I423
I424
I425
I136
I167
I168
I169
I432
I433
I434
I435
I137
I196
I197
I198
I441
I442
I443
I444
I451
I452
I453
I454

Fig 1.0601GB

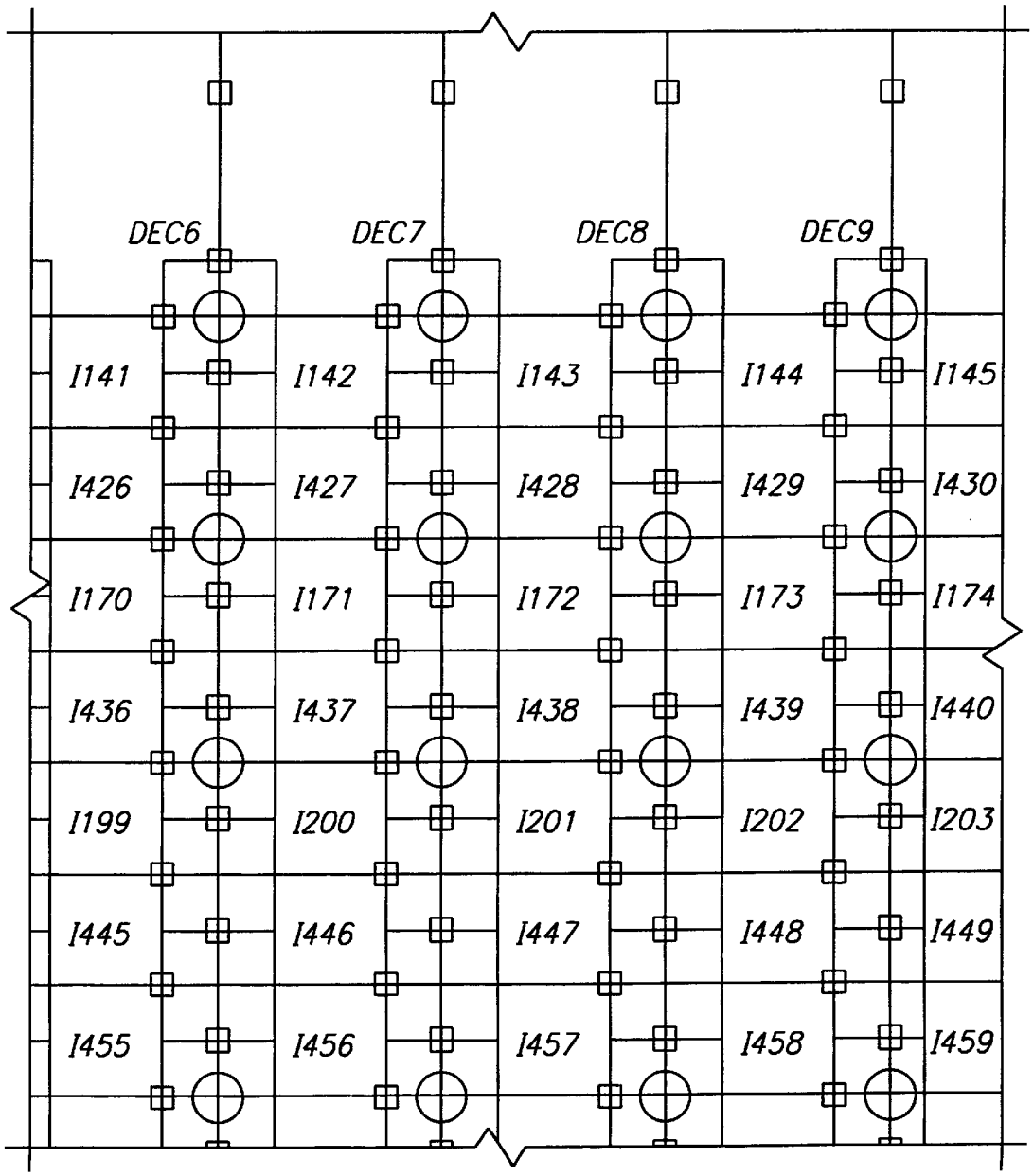

DEC6
DEC7
DEC8
DEC9
I141
I142
I143
I144
I145
I426
I427
I428
I429
I430
I170
I171
I172
I173
I174
I436
I437
I438
I439
I440
I199
I200
I201
I202
I203
I445
I446
I447
I448
I449
I455
I456
I457
I458
I459

Fig 1,060,160

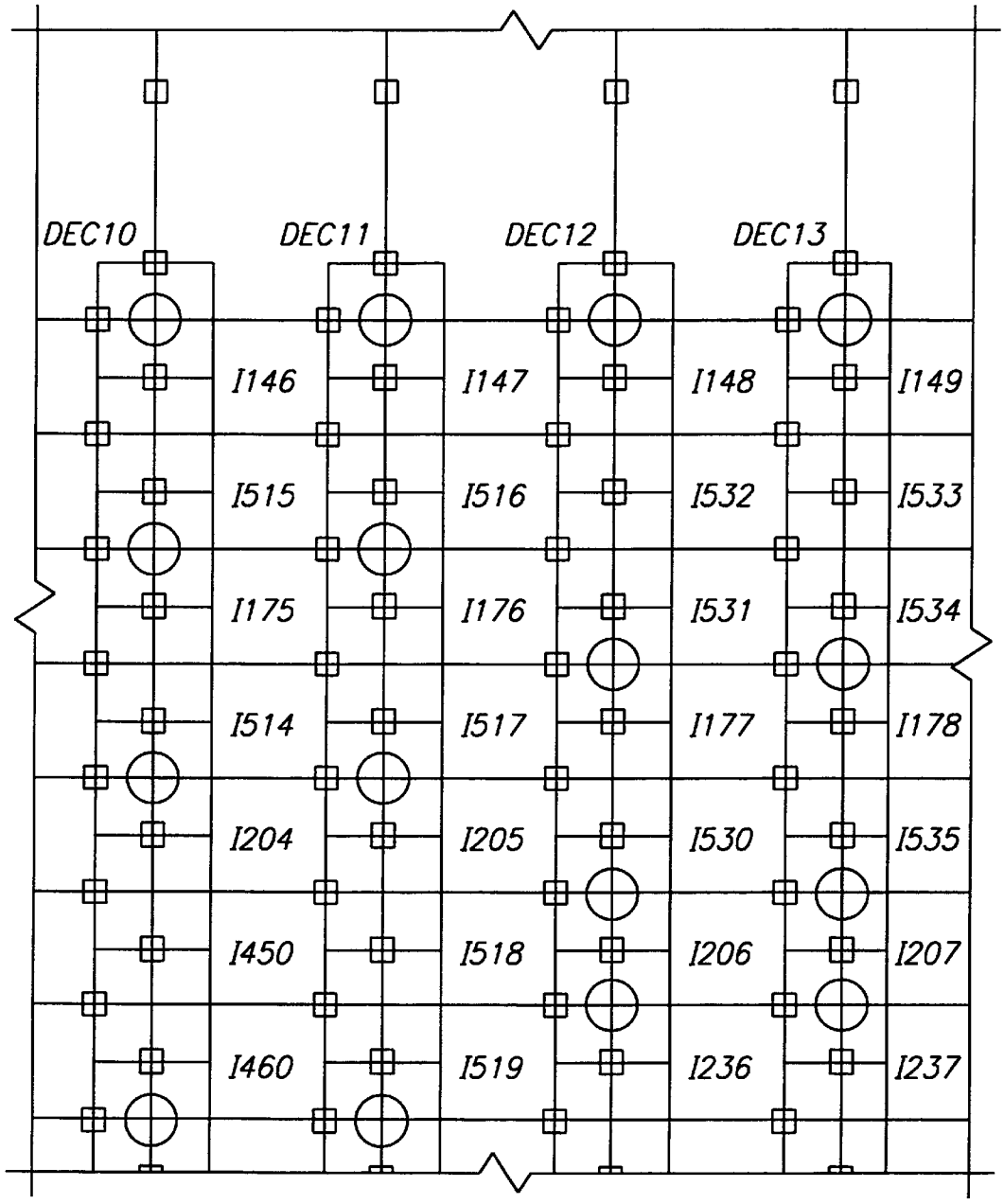
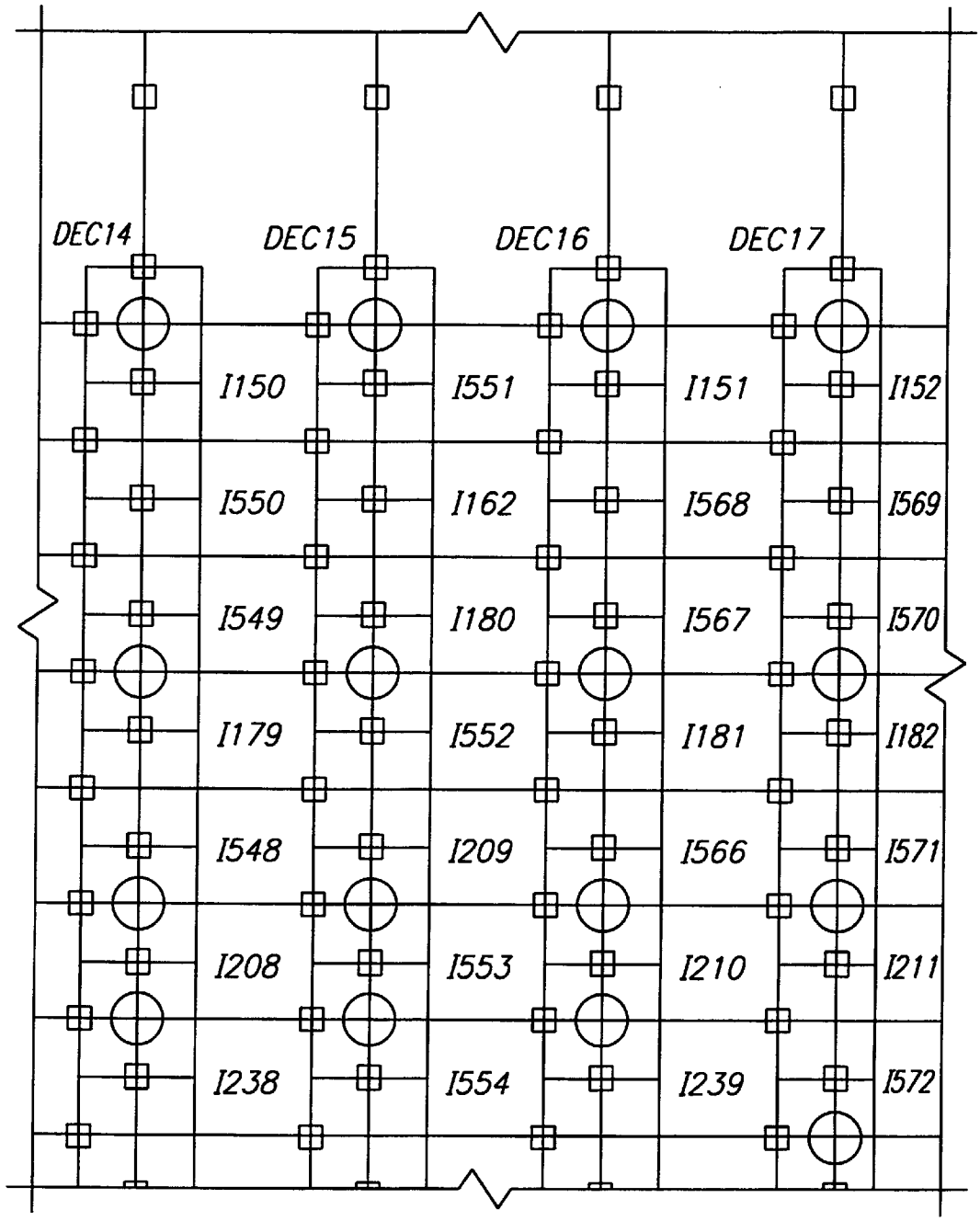

DEC10
DEC11
DEC12
DEC13
I146
I147
I148
I149
I515
I516
I532
I533
I175
I176
I531
I534
I514
I517
I177
I178
I204
I205
I530
I535
I450
I518
I206
I207
I460
I519
I236
I237

Fig 1,060,160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DEC15
DEC16
DEC17
I150
I551
I151
I152
I550
I162
I568
I569
I549
I180
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I570
I179
I552
I181
I182
I548
I209
I566
I571
I208
I553
I210
I211
I238
I554
I239
I572

Fig 1.0601GE

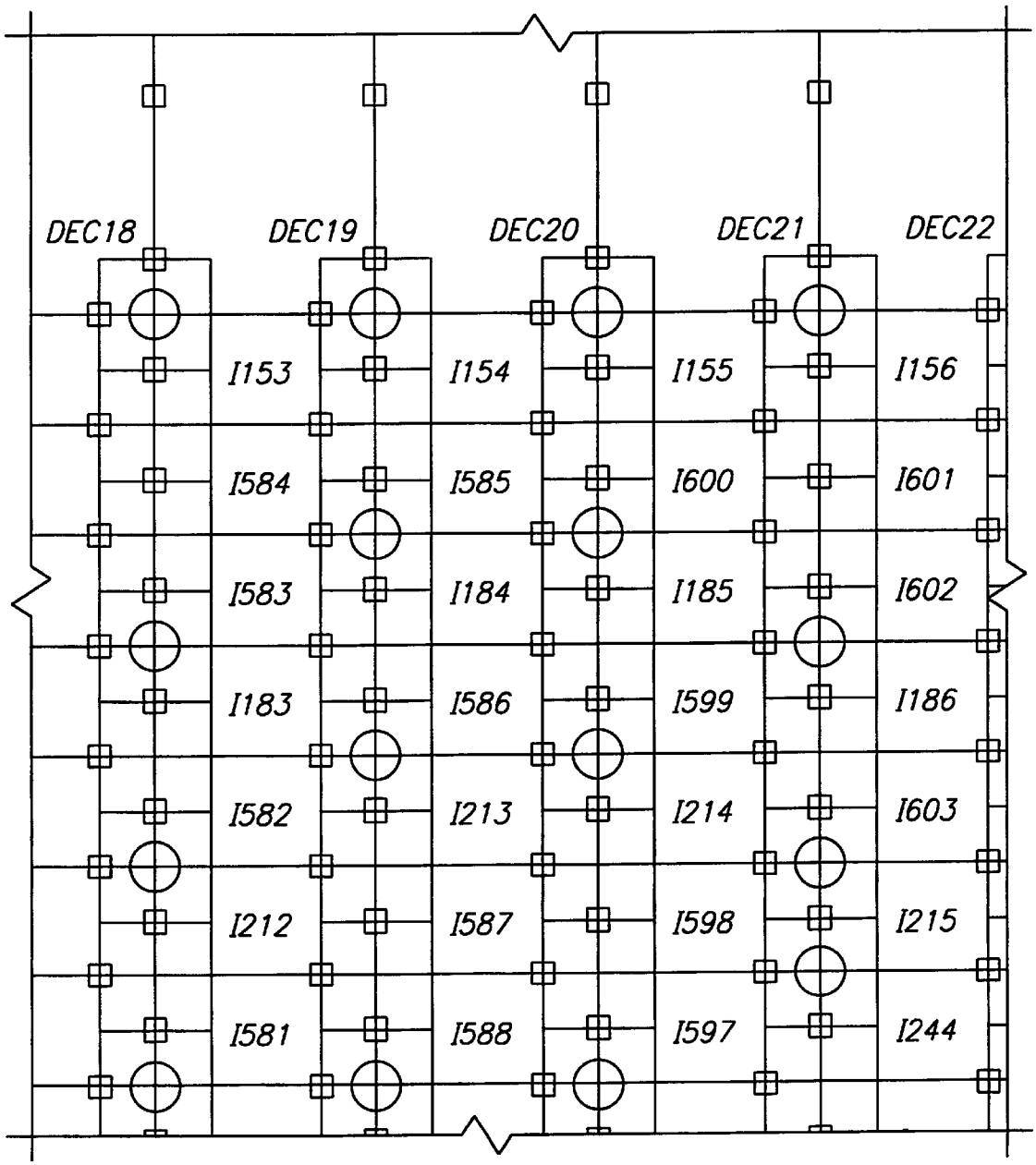


Fig 1.0601.16F

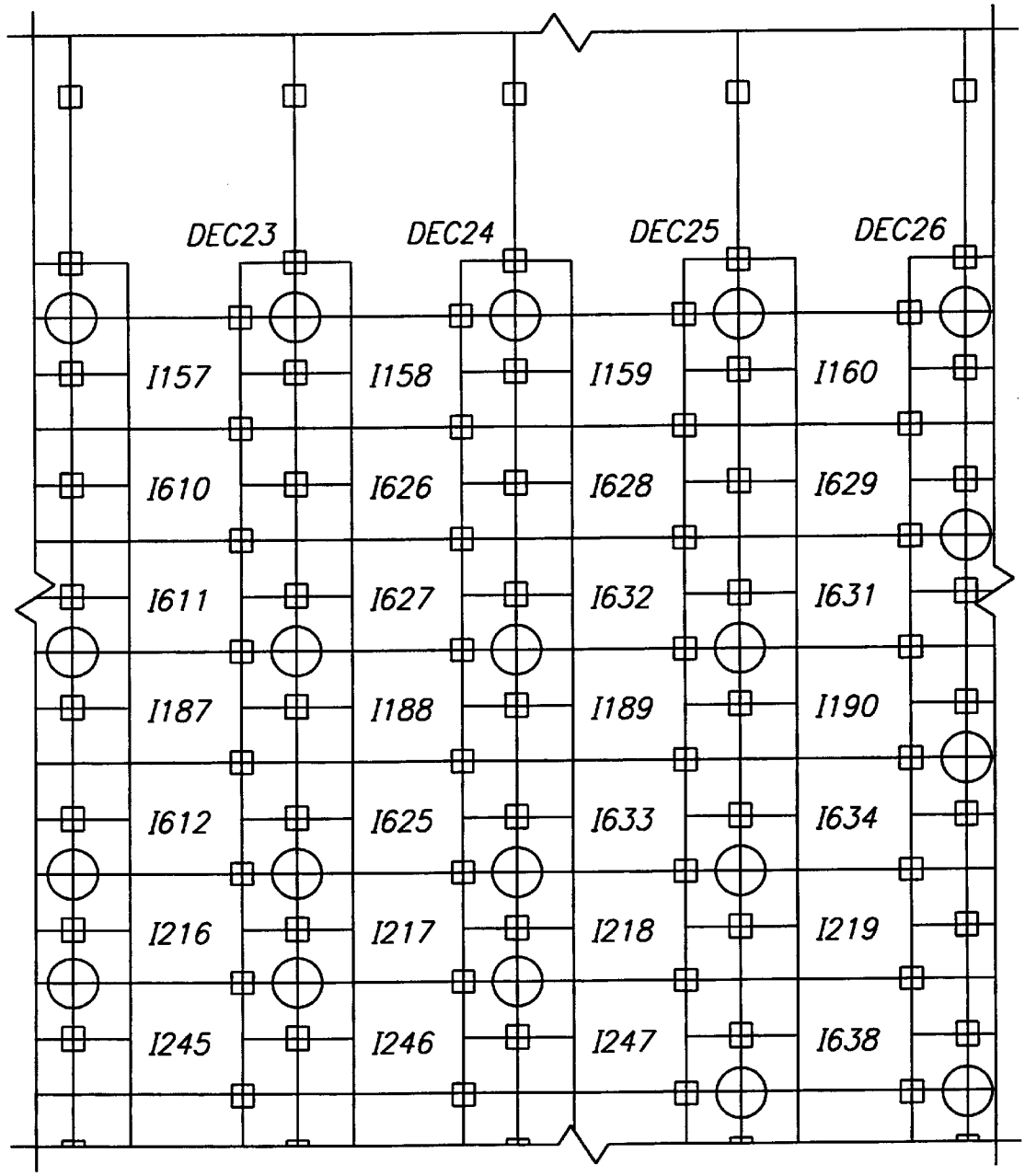

DEC23
DEC24
DEC25
DEC26
I157
I158
I159
I160
I610
I626
I628
I629
I611
I627
I632
I631
I187
I188
I189
I190
I612
I625
I633
I634
I216
I217
I218
I219
I245
I246
I247
I638

Fig 1,060,166

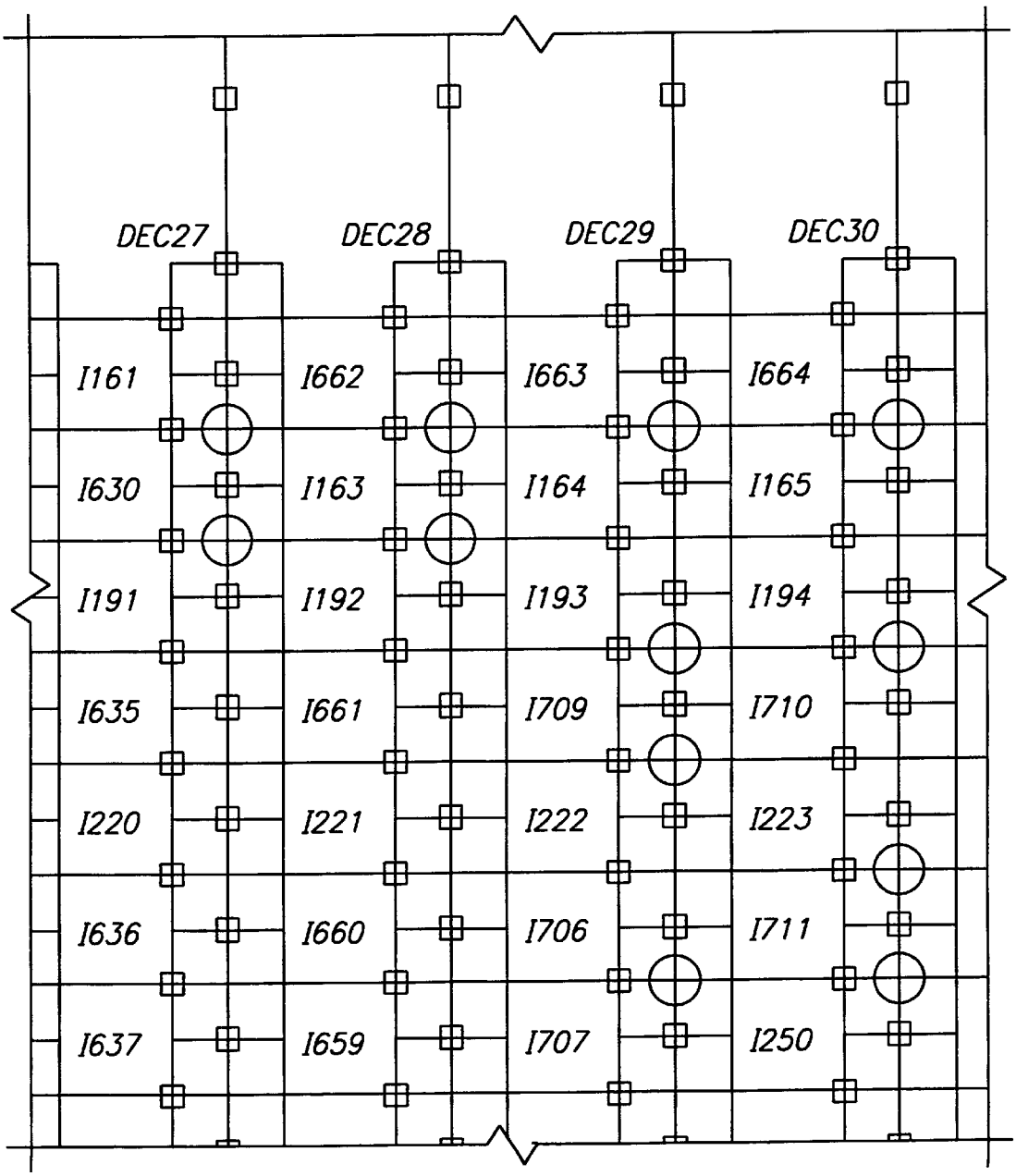


Fig 1.06010GH

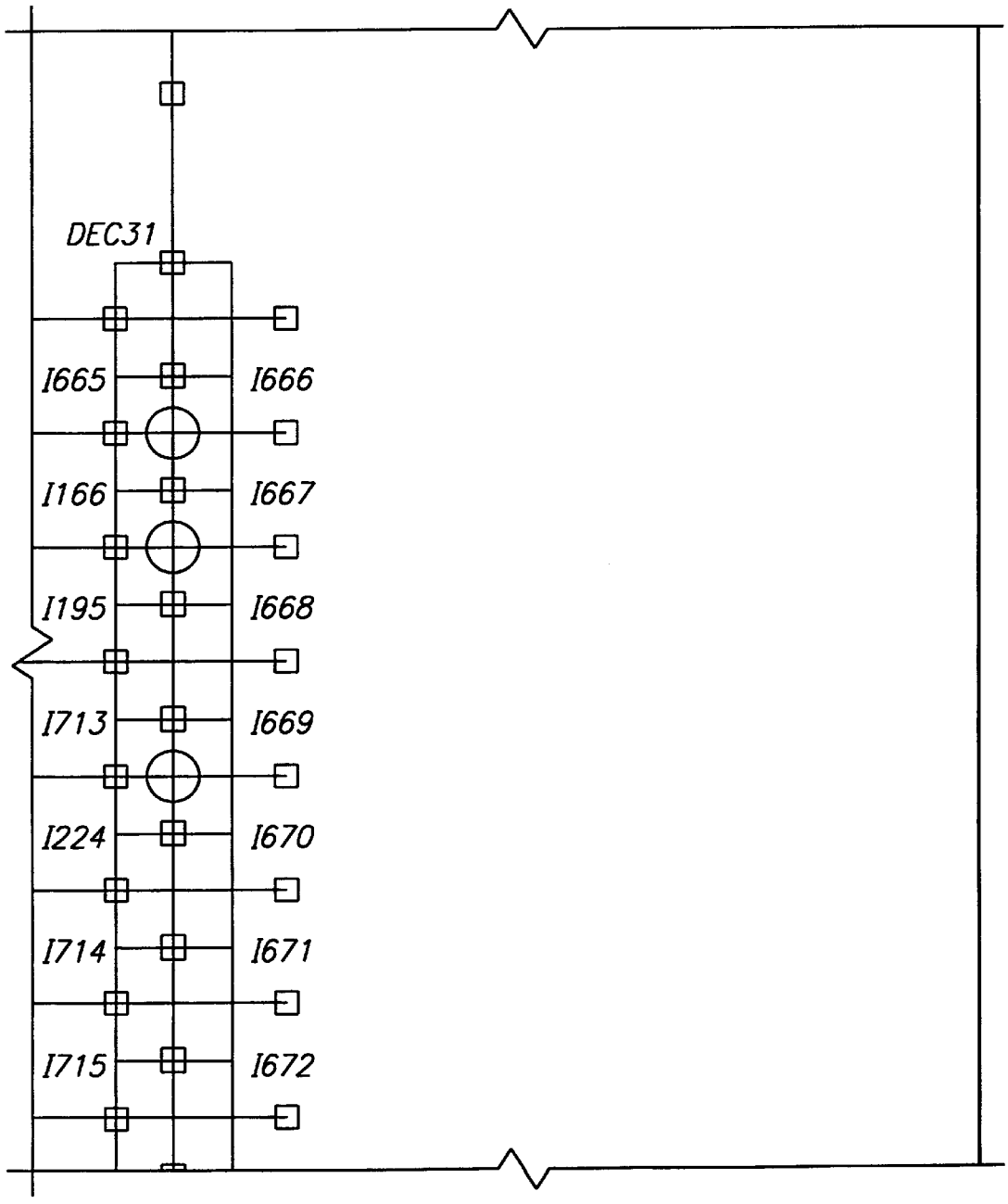

DEC31
I665
I666
I166
I667
I195
I668
I713
I669
I224
I670
I714
I671
I715
I672

Fig 1.060161

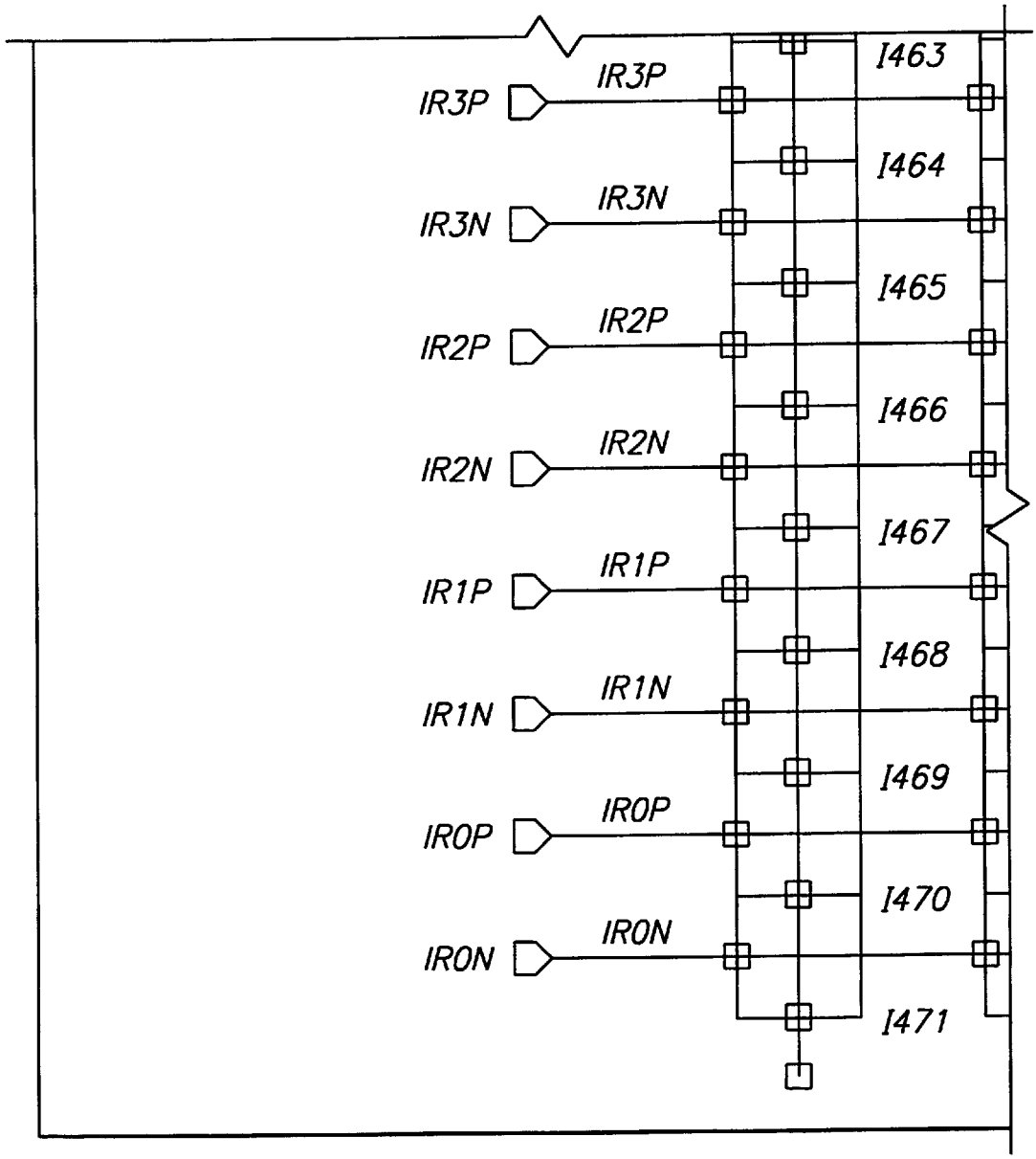

IR3P
IR3P
IR3N
IR3N
IR2P
IR2P
IR2N
IR2N
IR1P
IR1P
IR1N
IR1N
IR0P
IR0P
IR0N
IR0N
I463
I464
I465
I466
I467
I468
I469
I470
I471

Fig 1.0601HA

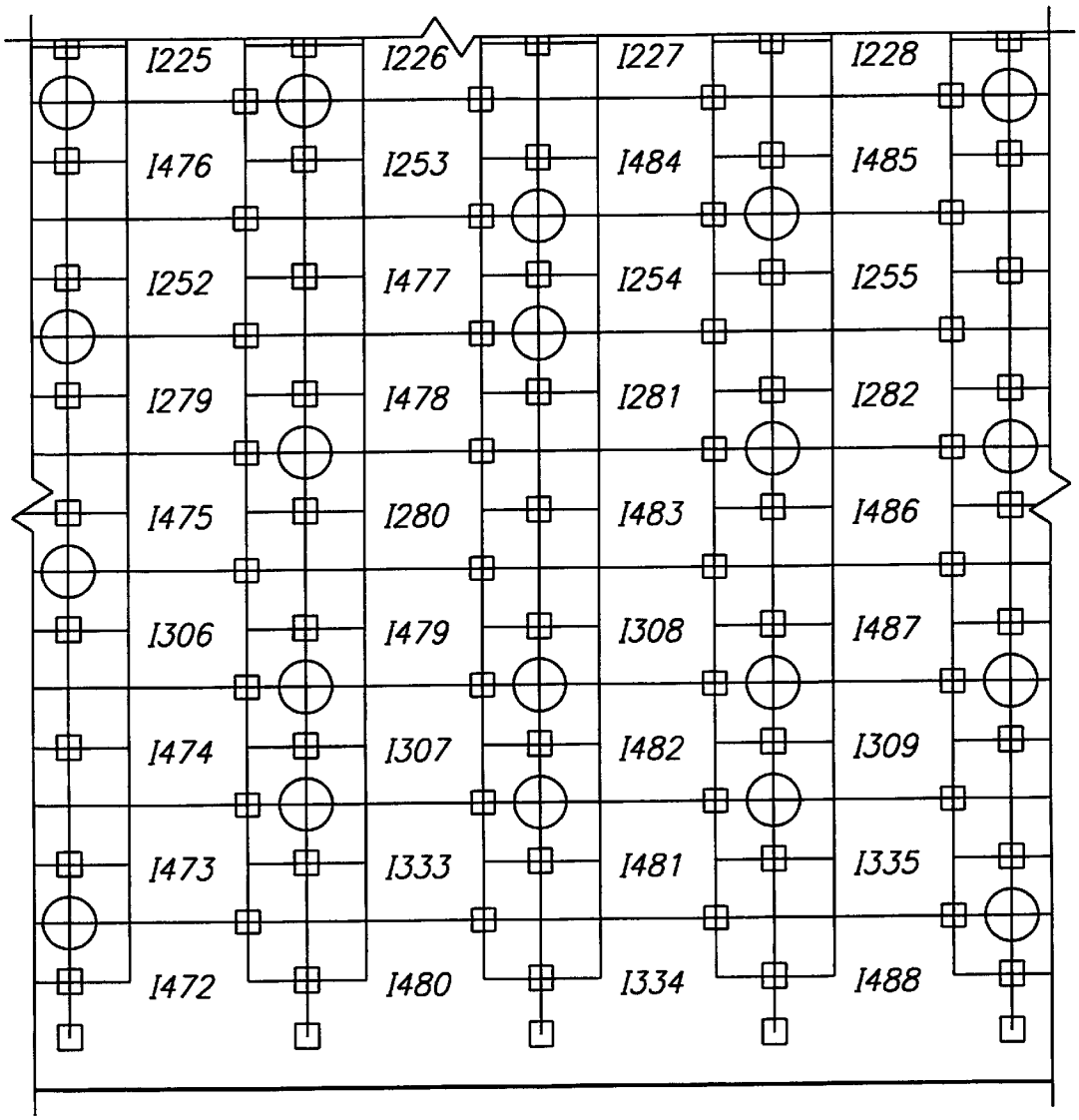

I225
I226
I227
I228
I476
I253
I484
I485
I252
I477
I254
I255
I279
I478
I281
I282
I475
I280
I483
I486
I306
I479
I308
I487
I474
I307
I482
I309
I473
I333
I481
I335
I472
I480
I334
I488

Fig 1,060,118

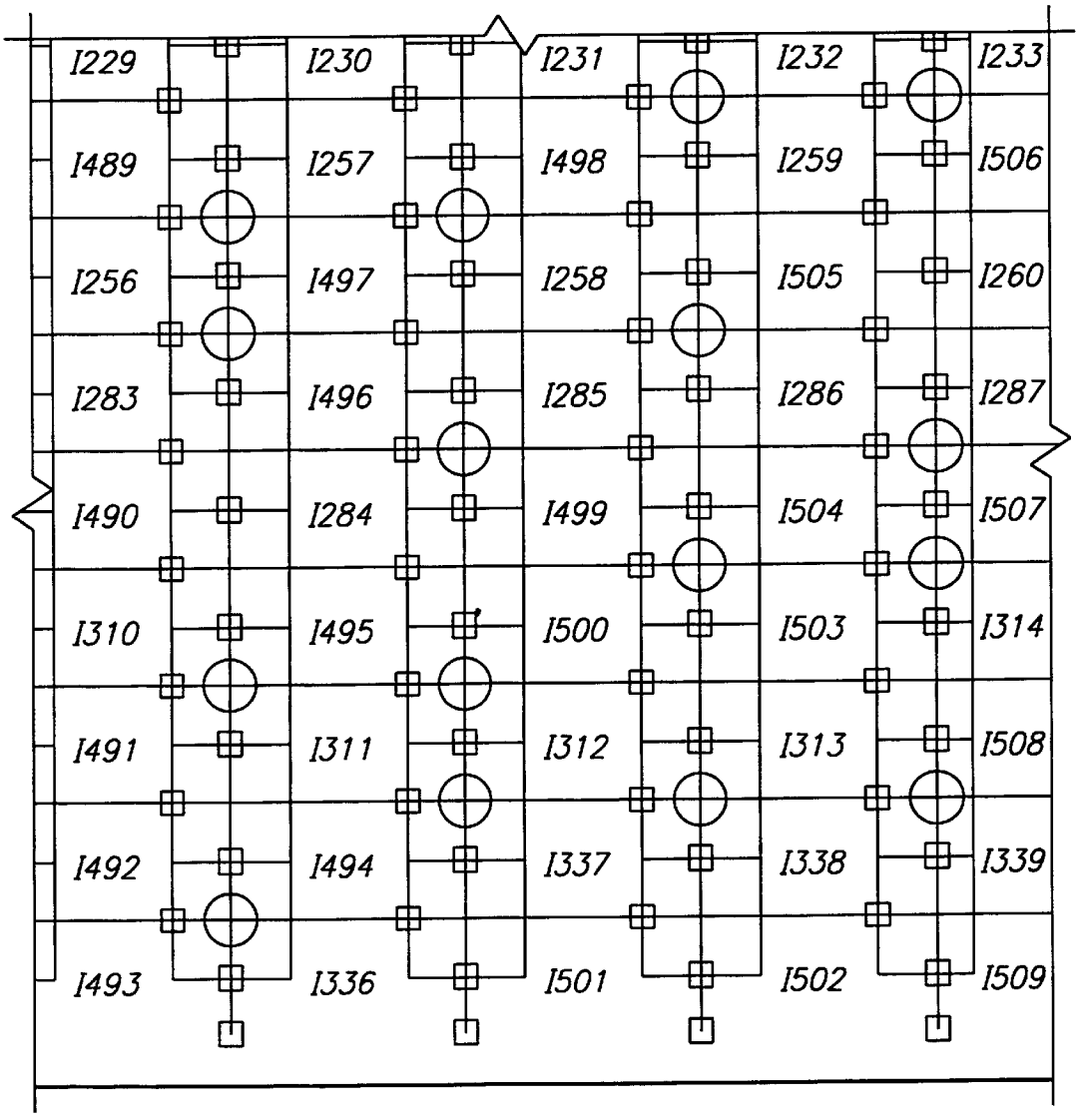

I229
I230
I231
I232
I233
I489
I257
I498
I259
I506
I256
I497
I258
I505
I260
I283
I496
I285
I286
I287
I490
I284
I499
I504
I507
I310
I495
I500
I503
I314
I491
I311
I312
I313
I508
I492
I494
I337
I338
I339
I493
I336
I501
I502
I509

Fig 1.0601HC

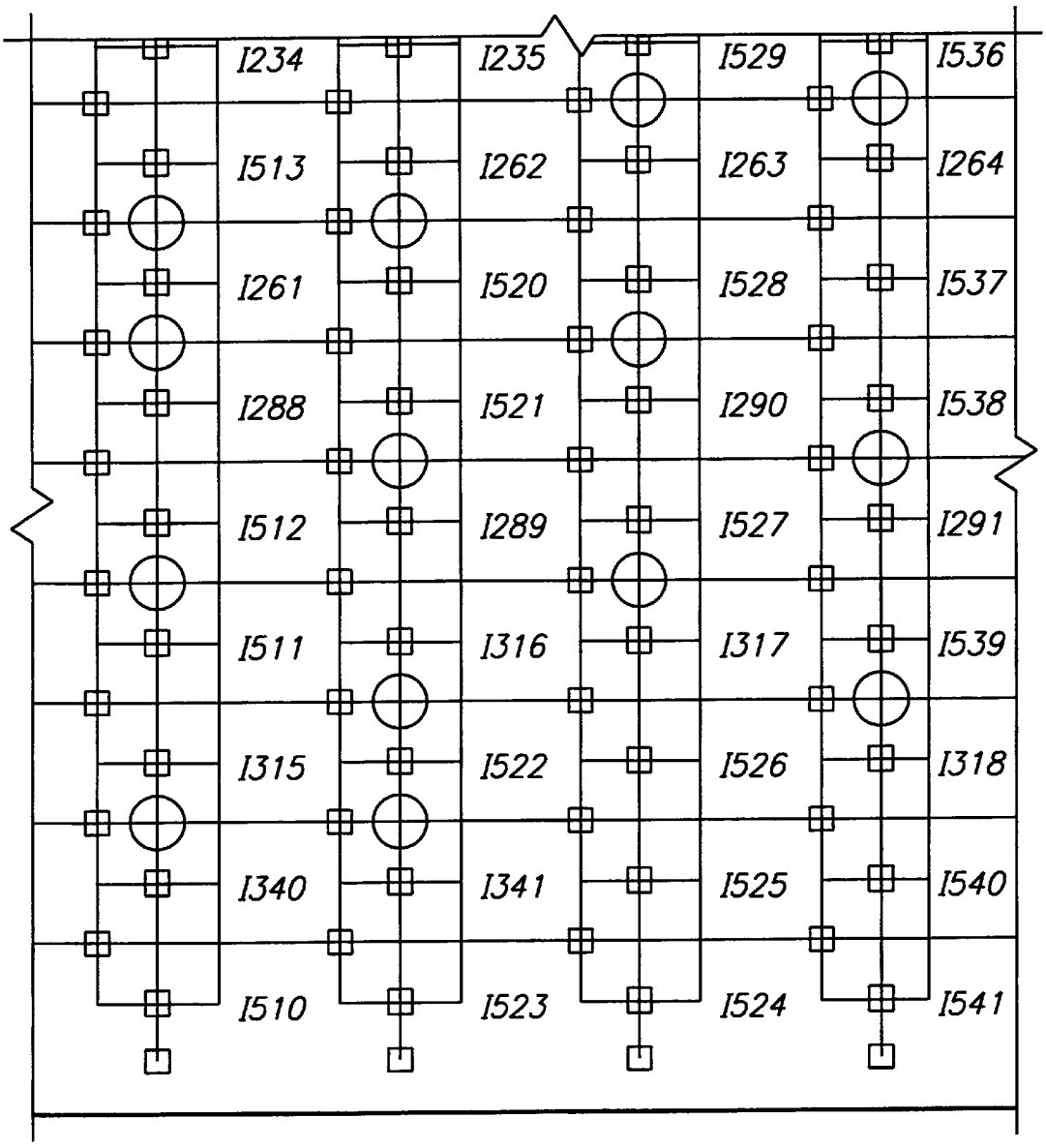

I234
I235
I529
I536
I513
I262
I263
I264
I261
I520
I528
I537
I288
I521
I290
I538
I512
I289
I527
I291
I511
I316
I317
I539
I315
I522
I526
I318
I340
I341
I525
I540
I510
I523
I524
I541

Fig 1,060,1HD

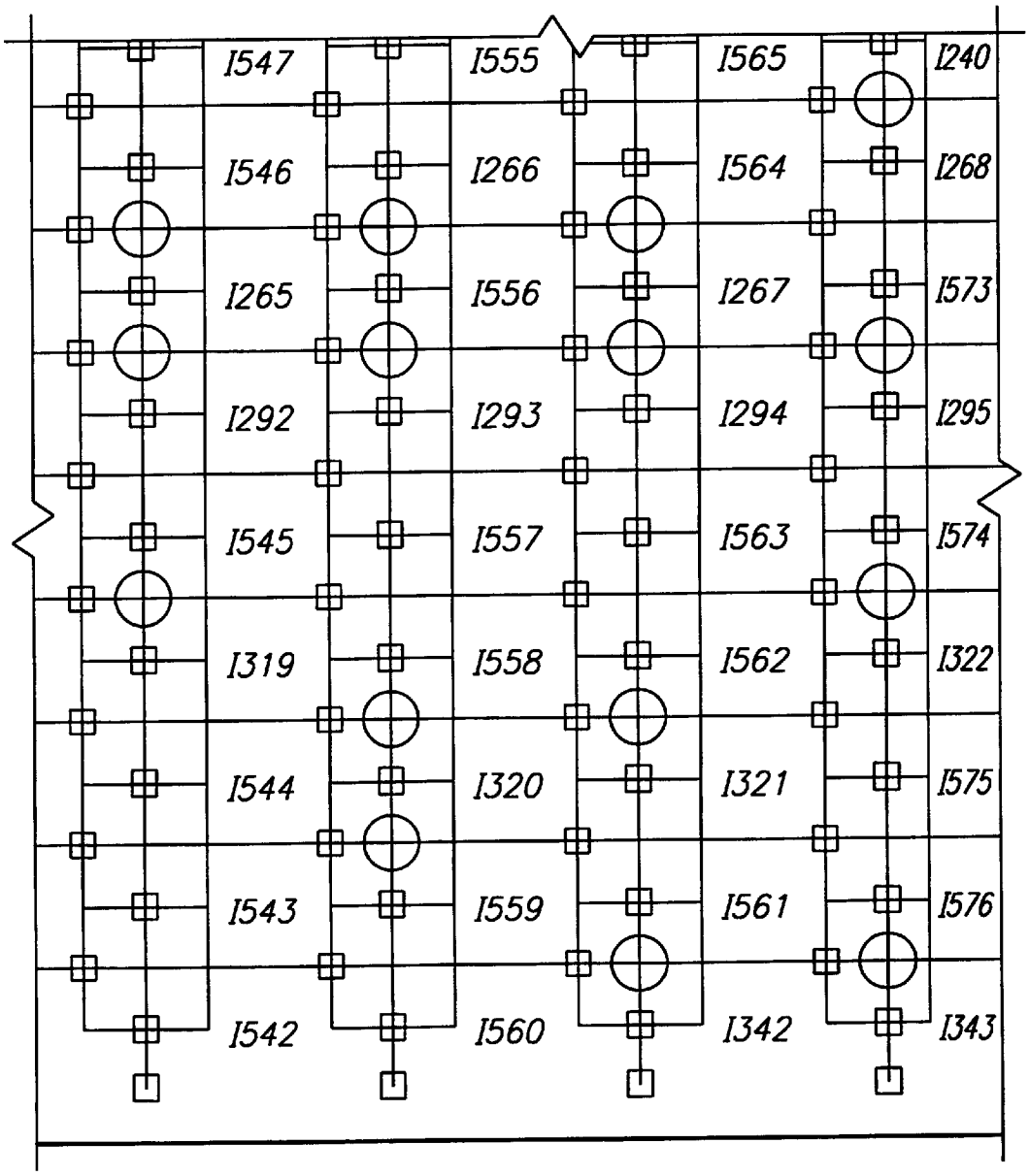

I547
I555
I565
I240
I546
I266
I564
I268
I265
I556
I267
I573
I292
I293
I294
I295
I545
I557
I563
I574
I319
I558
I562
I322
I544
I320
I321
I575
I543
I559
I561
I576
I542
I560
I342
I343

Fig 1,060,116

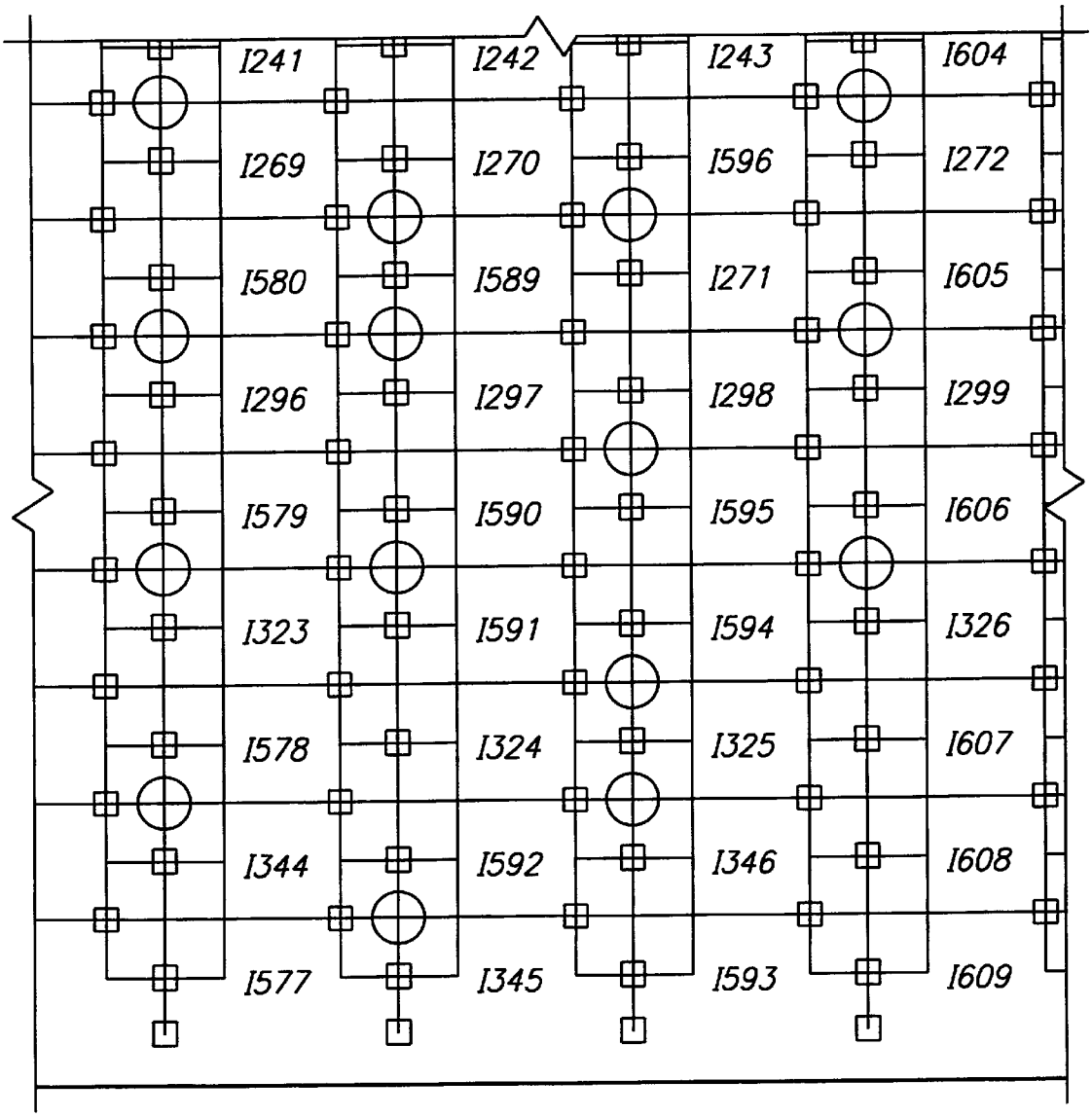

I241
I242
I243
I604
I269
I270
I596
I272
I580
I589
I271
I605
I296
I297
I298
I299
I579
I590
I595
I606
I323
I591
I594
I326
I578
I324
I325
I607
I344
I592
I346
I608
I577
I345
I593
I609

Fig 1.0601HF

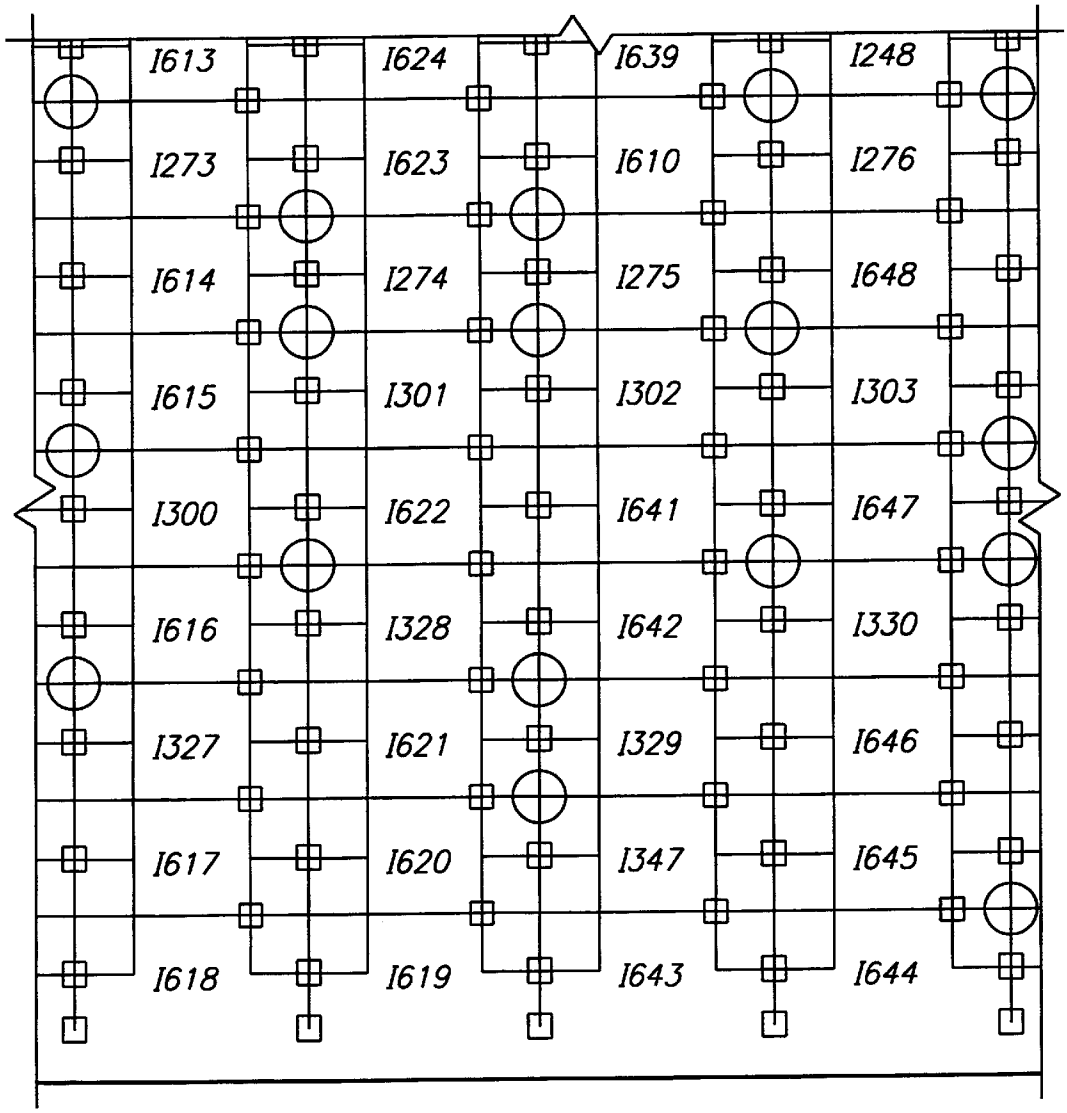

I613
I624
I639
I248
I273
I623
I610
I276
I614
I274
I275
I648
I615
I301
I302
I303
I300
I622
I641
I647
I616
I328
I642
I330
I327
I621
I329
I646
I617
I620
I347
I645
I618
I619
I643
I644

Fig 1,060,116

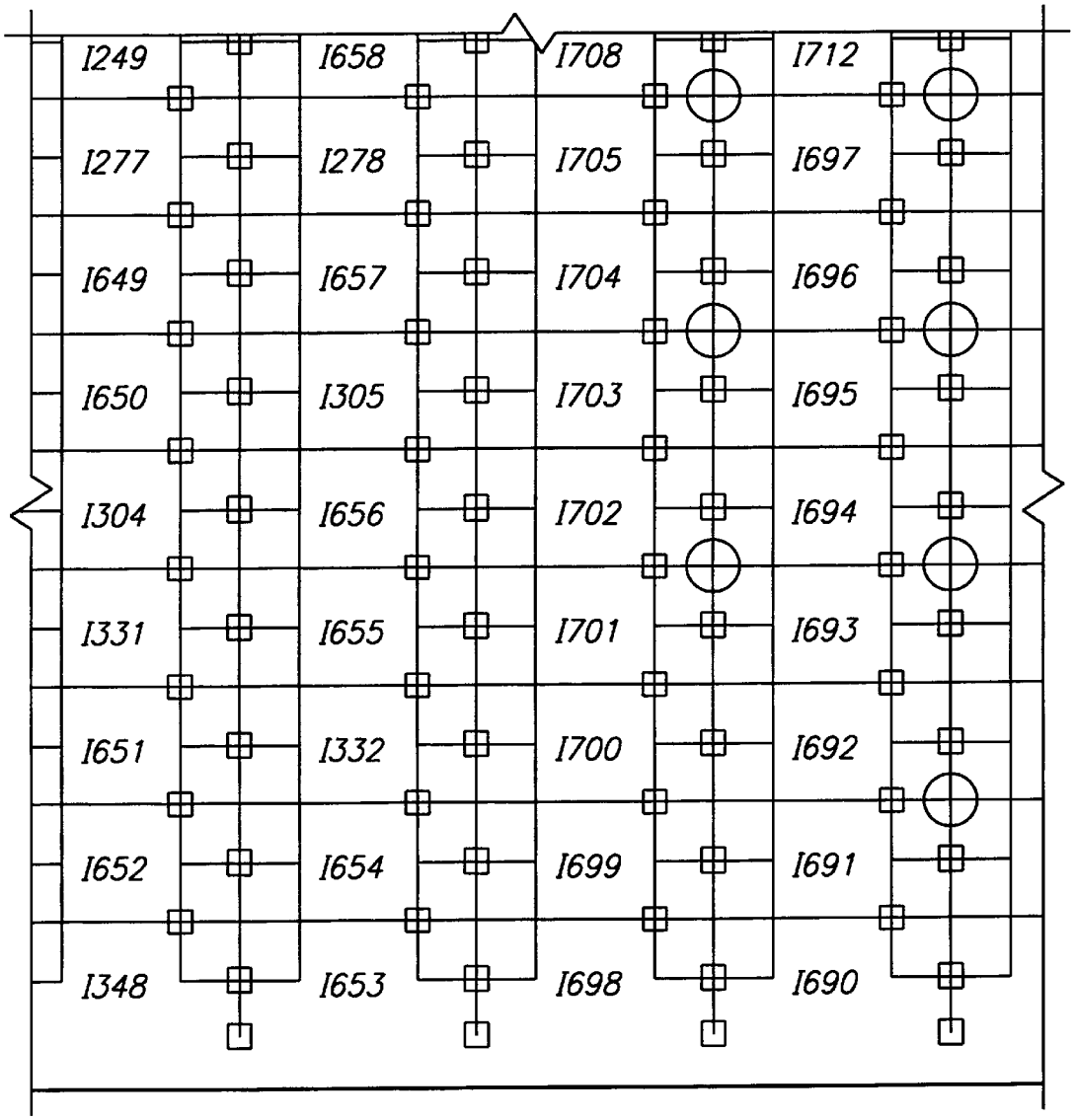

I249
I658
I708
I712
I277
I278
I705
I697
I649
I657
I704
I696
I650
I305
I703
I695
I304
I656
I702
I694
I331
I655
I701
I693
I651
I332
I700
I692
I652
I654
I699
I691
I348
I653
I698
I690

Fig 1,060,114

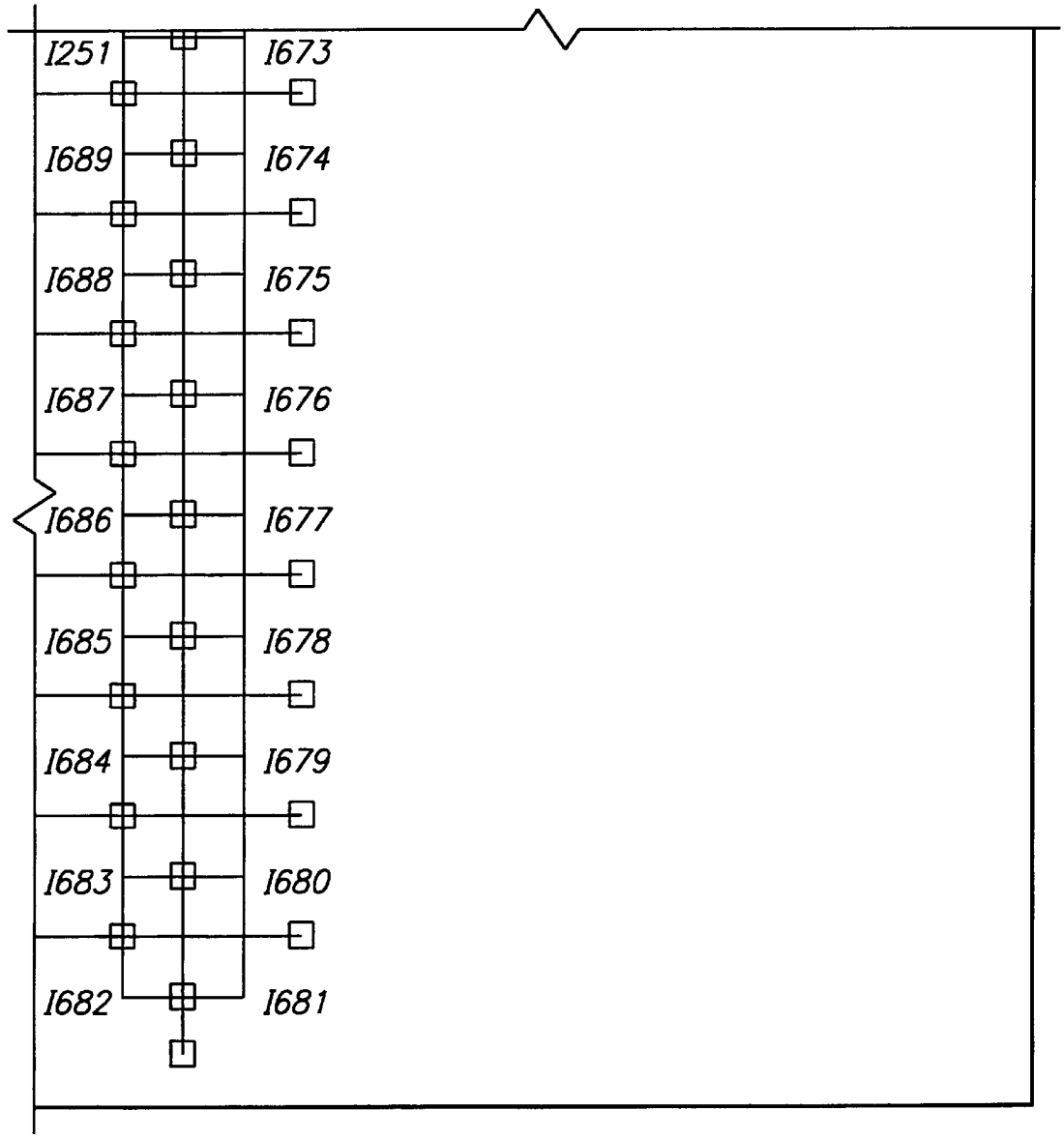

I251
I673
I689
I674
I688
I675
I687
I676
I686
I677
I685
I678
I684
I679
I683
I680
I682
I681

Fig 1.060111

7.0602AA	7.0602AB	7.0602AC	7.0602AD	7.0602AE	7.0602AF	7.0602AG	7.0602AH
7.0602BA	7.0602BB	7.0602BC	7.0602BD	7.0602BE	7.0602BF	7.0602BG	7.0602BH
7.0602CA	7.0602CB	7.0602CC	7.0602CD	7.0602CE	7.0602CF	7.0602CG	7.0602CH
7.0602DA	7.0602DB	7.0602DC	7.0602DD	7.0602DE	7.0602DF	7.0602DG	7.0602DH
7.0602EA	7.0602EB	7.0602EC	7.0602ED	7.0602EE	7.0602EF	7.0602EG	7.0602EH
7.0602FA	7.0602FB	7.0602FC	7.0602FD	7.0602FE	7.0602FF	7.0602FG	7.0602FH
7.0602GA	7.0602GB	7.0602GC	7.0602GD	7.0602GE	7.0602GF	7.0602GG	7.0602GH
7.0602HA	7.0602HB	7.0602HC	7.0602HD	7.0602HE	7.0602HF	7.0602HG	7.0602HH
		7.0602IC	7.0602ID	7.0602IE	7.0602IF	7.0602IG	7.0602IH
		7.0602JC	7.0602JD	7.0602JE	7.0602JF	7.0602JG	7.0602JH

Fig 7.0602

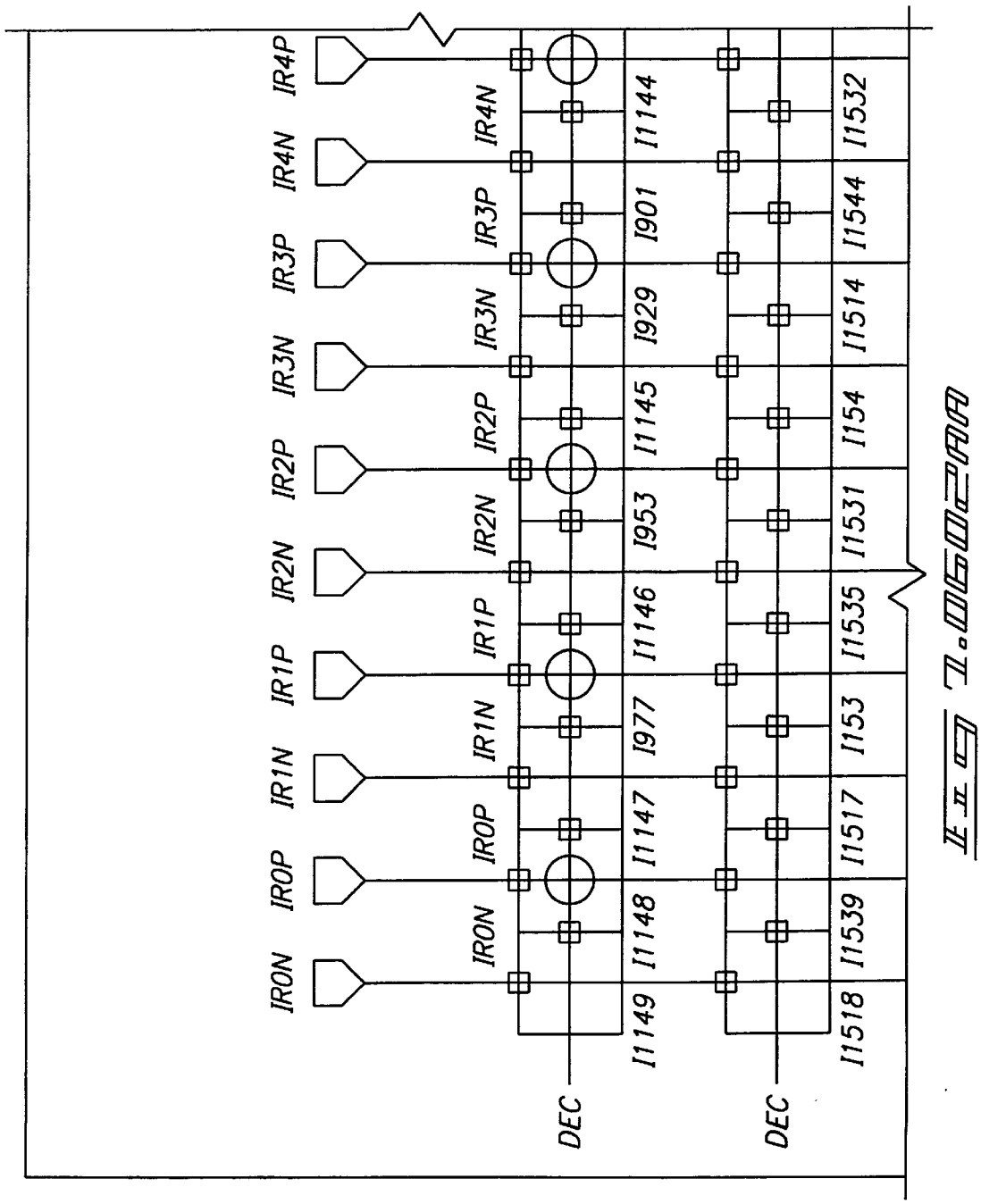


Fig. 11.00520AA

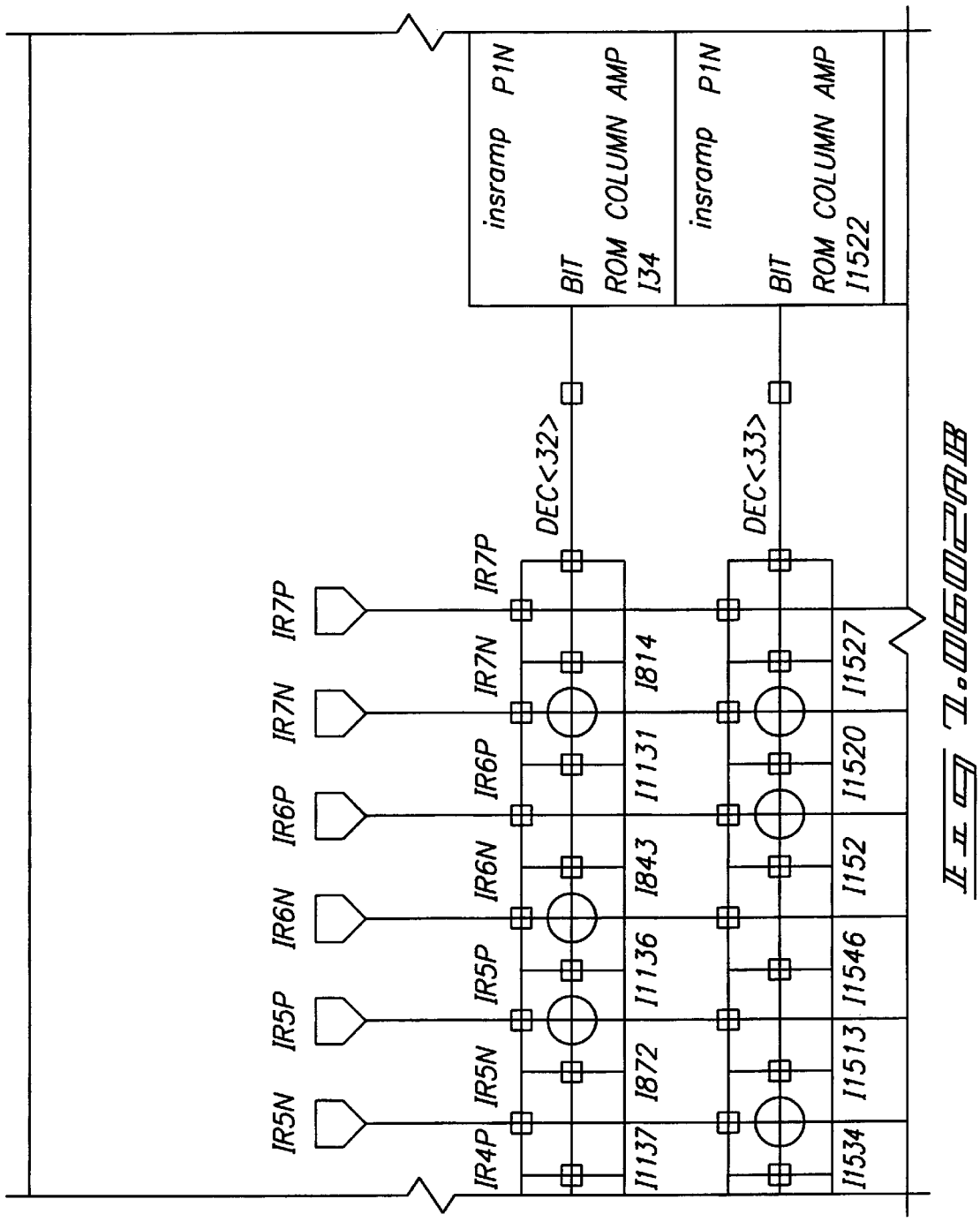

insramp P1N
BIT ROM COLUMN AMP
I34
insramp P1N
BIT ROM COLUMN AMP
I1522
DEC<32>
DEC<33>
IR7P
IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
I814
I1131
I843
I1136
I872
I1137
I1527
I1520
I1152
I1546
I1513
I1534

FIG 1.0602AB

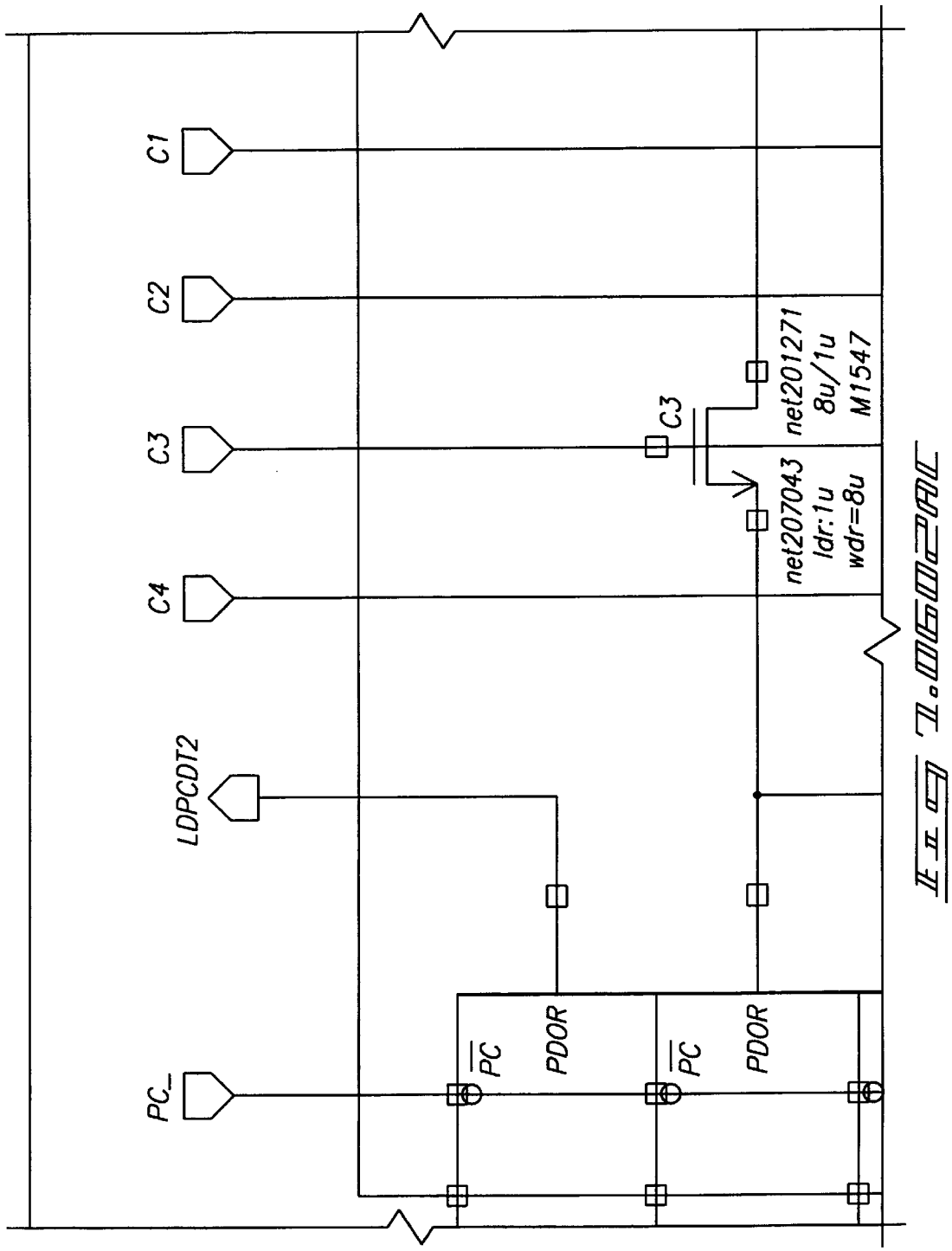

C1
C2
C3
C4
LDPCDT2
PC_
C3
net201271
8u/1u
M1547
net207043
ldr:1u
wdr=8u
PC
PDOR
PC
PDOR

Fig 1,006,242

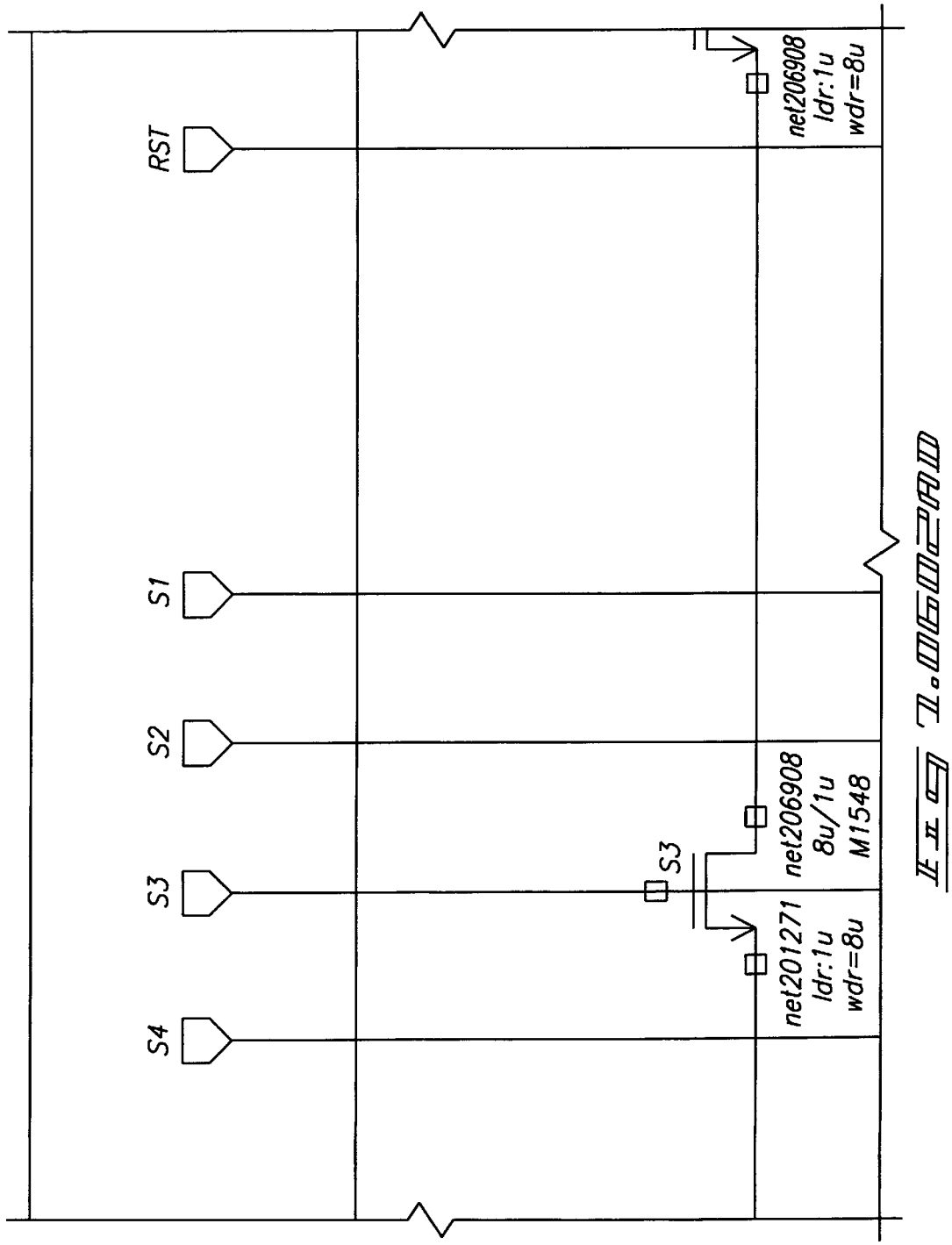

RST
S1
S2
S3
S4
S3
net206908
ldr:1u
wdr=8u
net206908
8u/1u
M1548
net201271
ldr:1u
wdr=8u

Fig. 1,000,572

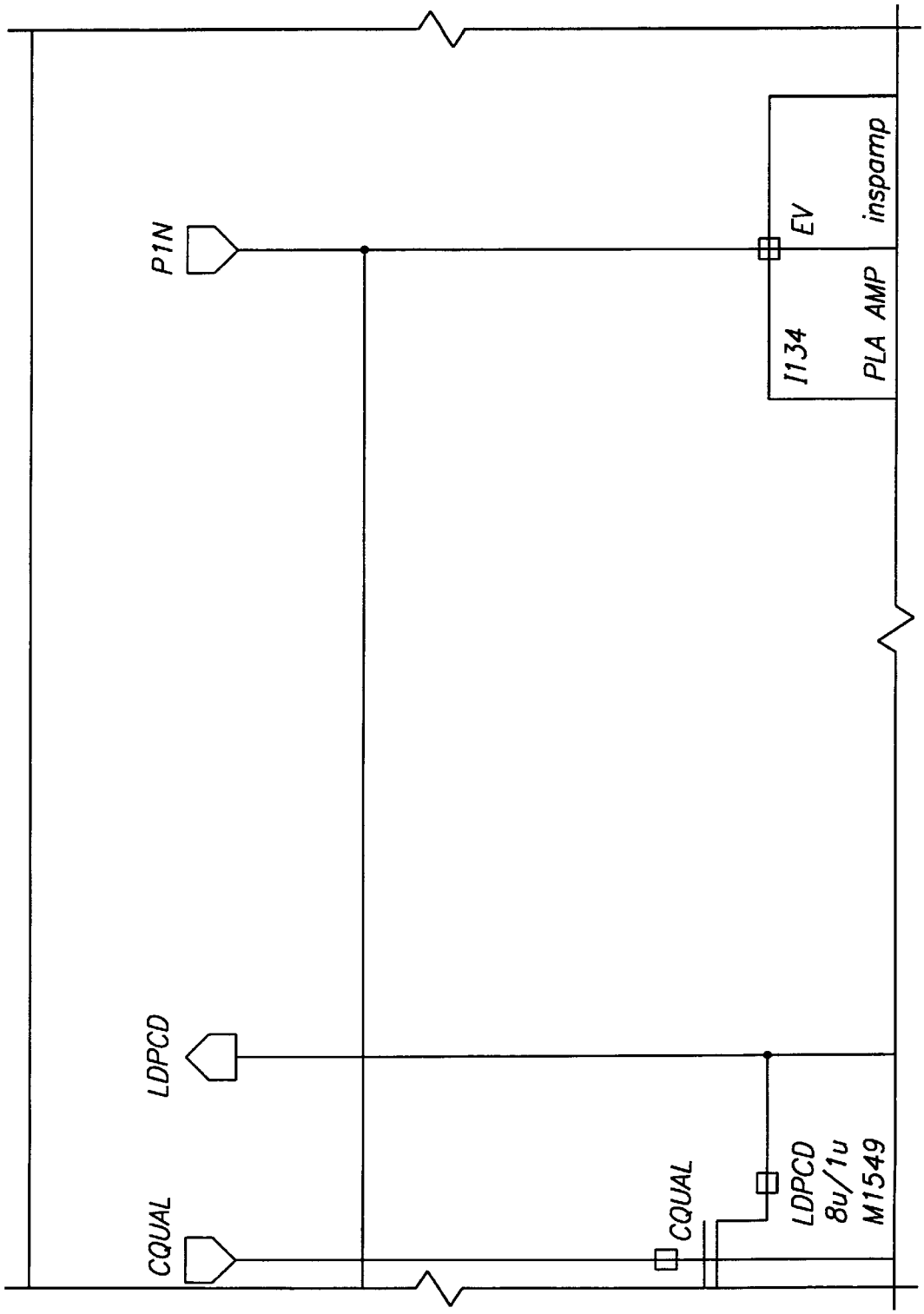


FIG 11.0502AE

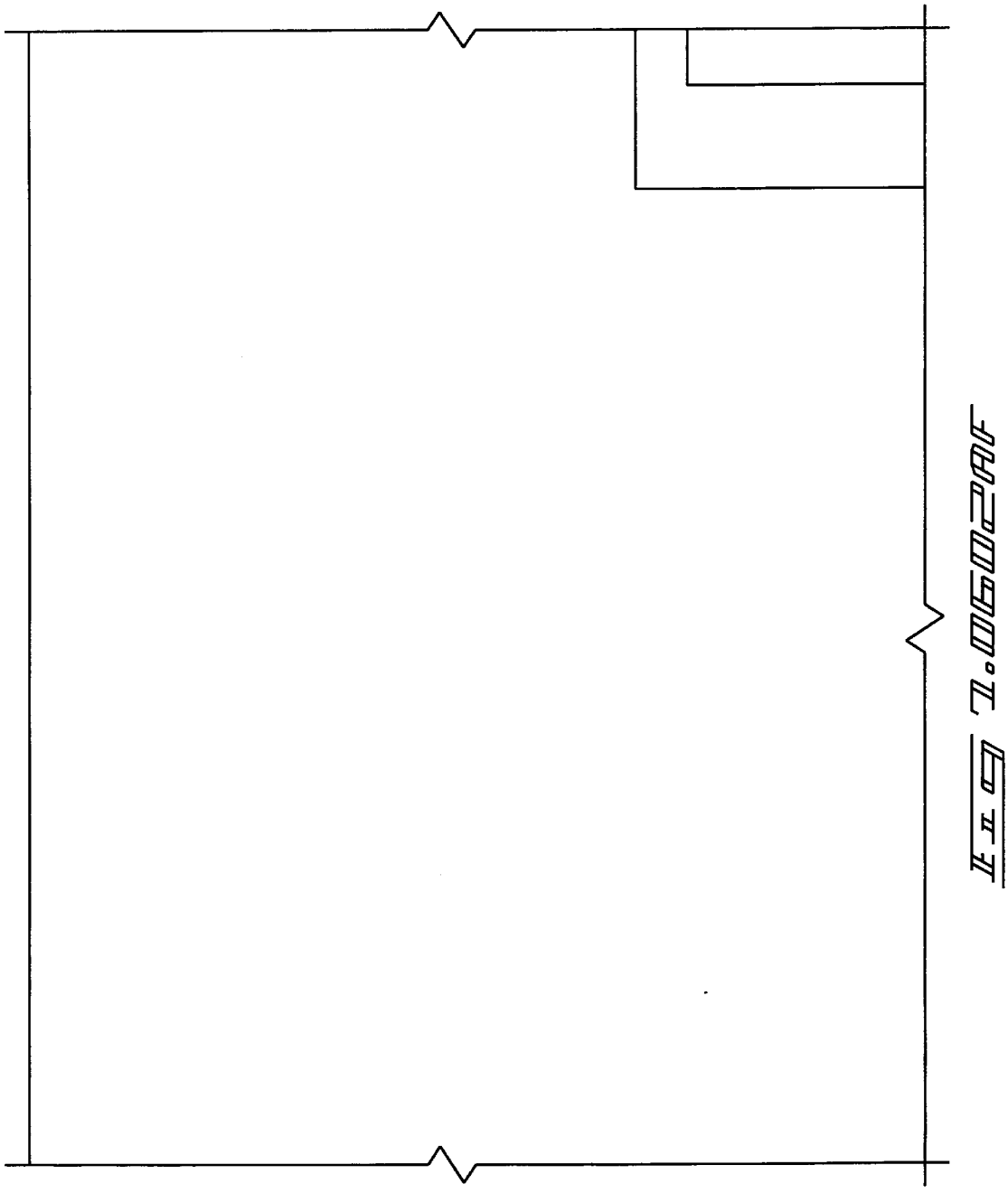
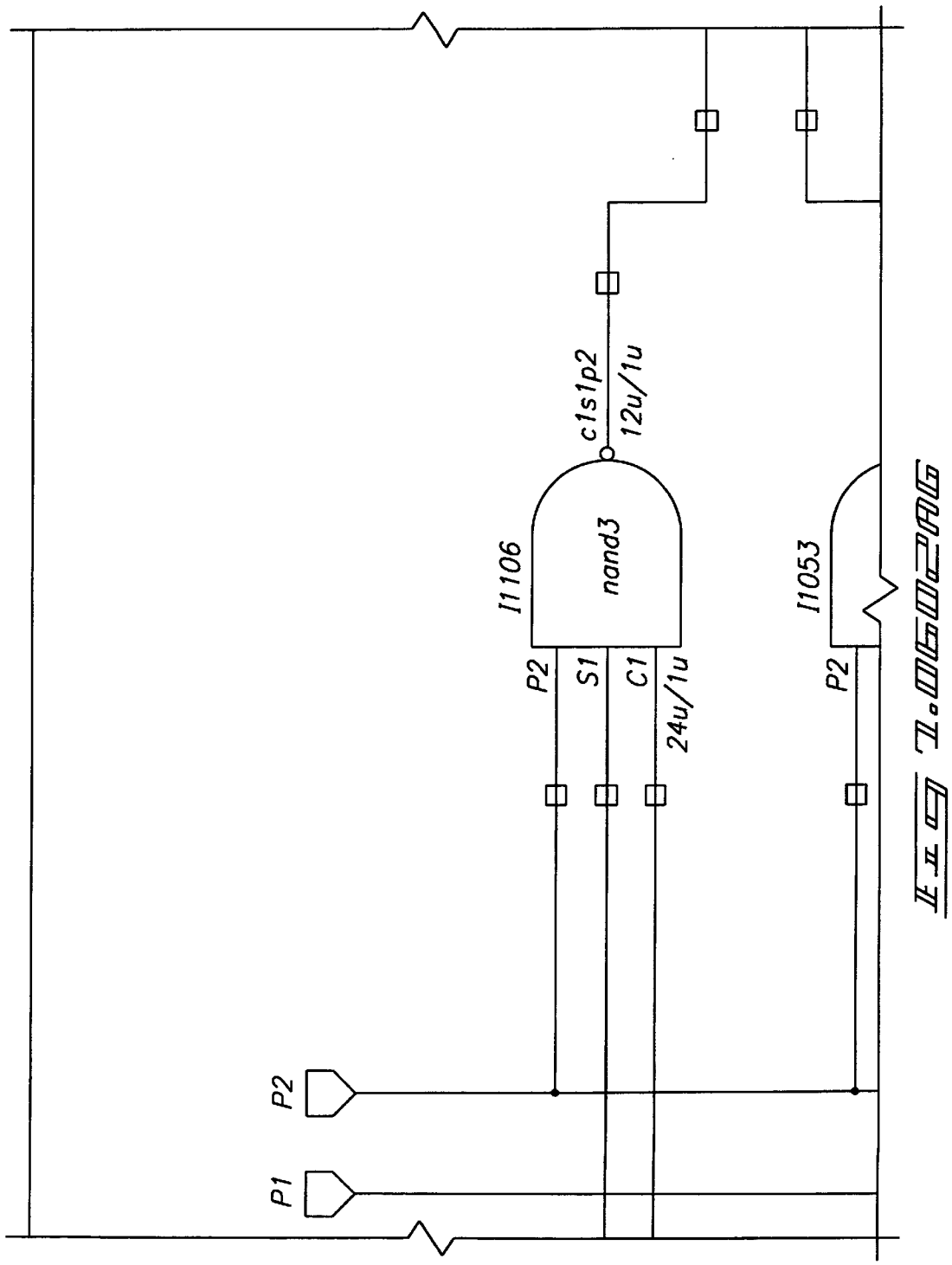


FIG 1,050,249


c1s1p2
12u/1u
I1106
nand3
I1053
P2
S1
C1
24u/1u
P2
P2
P1

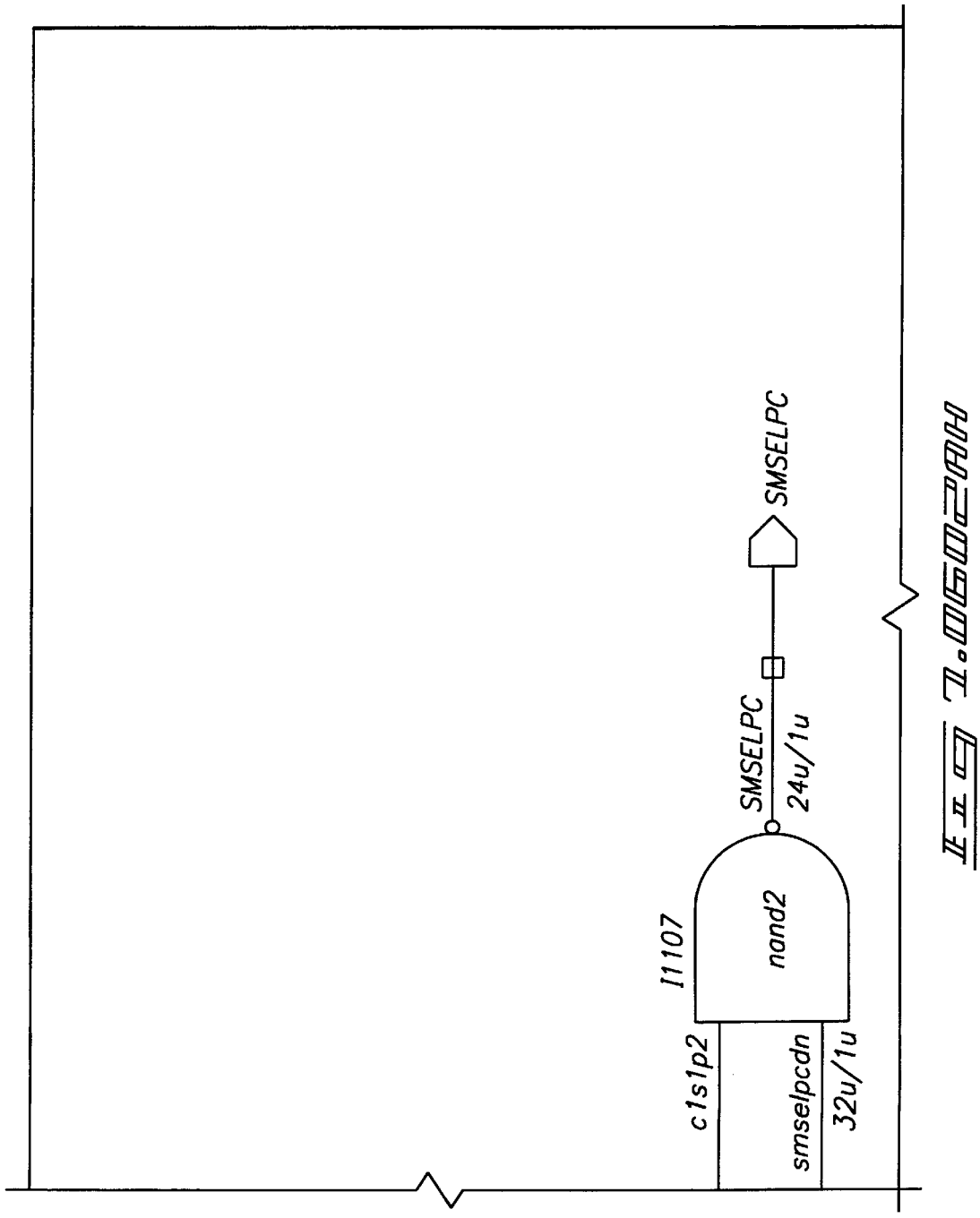


FIG 1,060,244

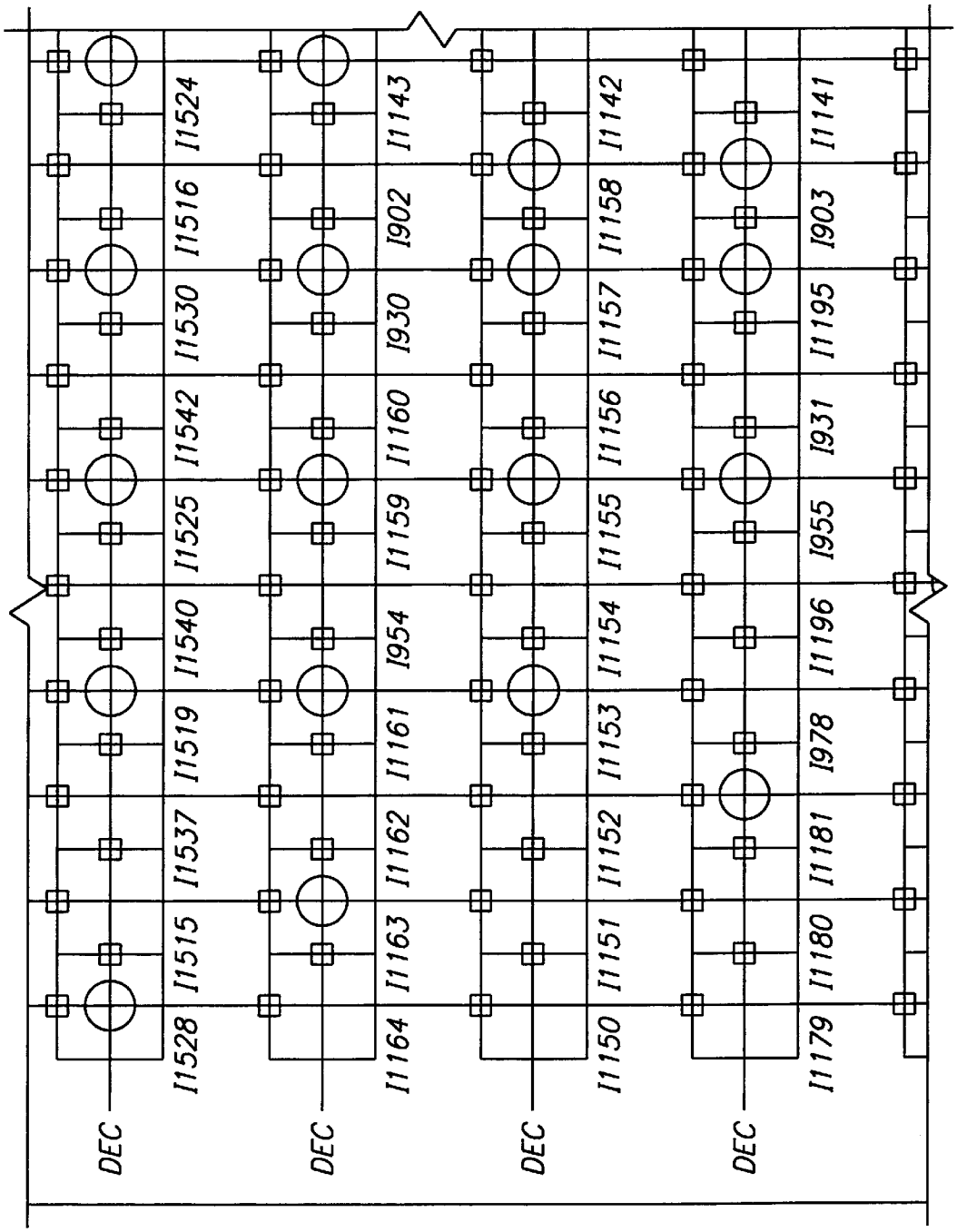

DEC
DEC
DEC
DEC
I1528
I1515
I1537
I1519
I1540
I1525
I1542
I1530
I1516
I1524
I1164
I1163
I1162
I1161
I954
I1159
I1160
I930
I902
I1143
I1150
I1151
I1152
I1153
I1154
I1155
I1156
I1157
I1158
I1142
I1179
I1180
I1181
I978
I1196
I955
I931
I1195
I903
I1141

FIG. 1600A

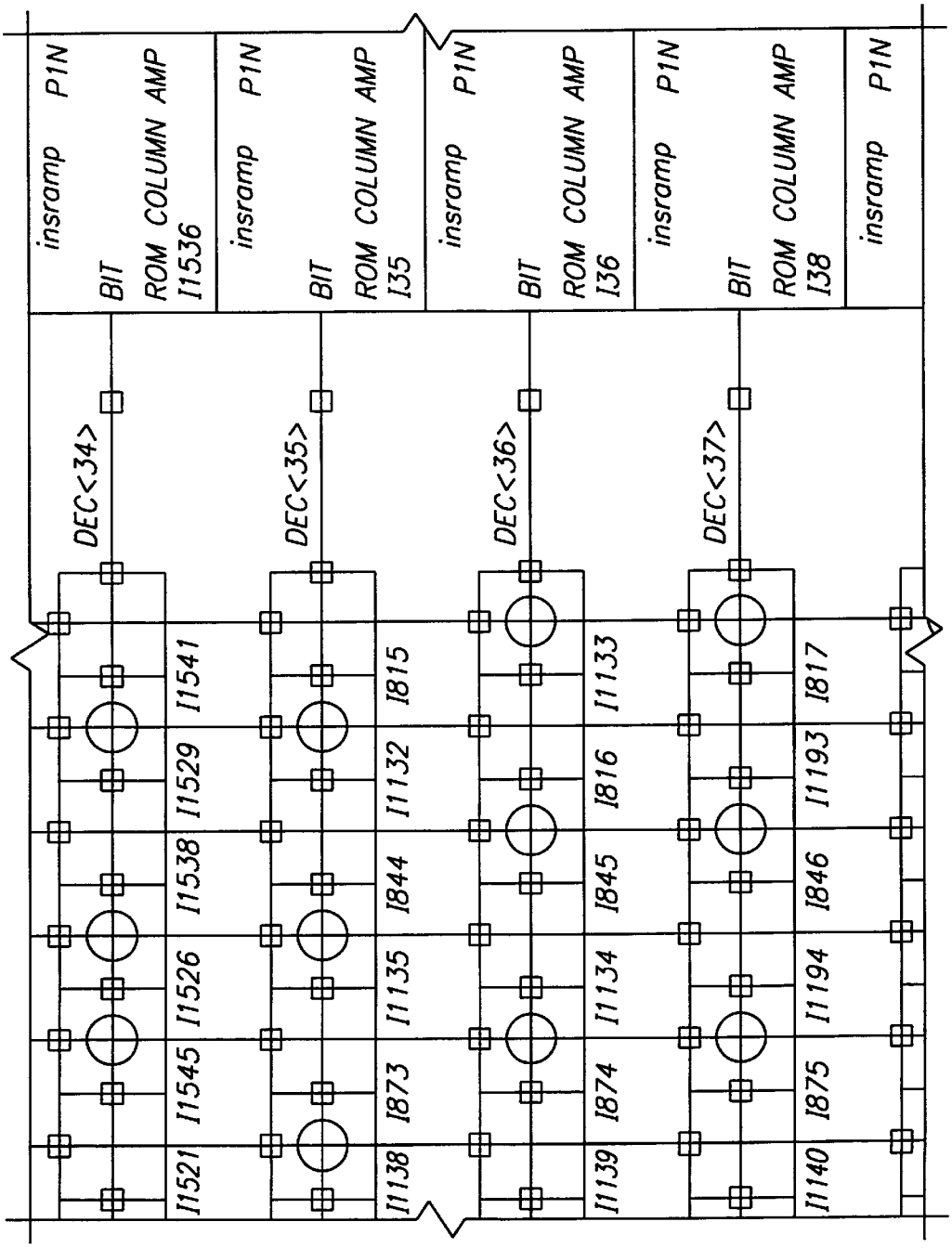

insramp P1N
BIT ROM COLUMN AMP I1536
insramp P1N
BIT ROM COLUMN AMP I35
insramp P1N
BIT ROM COLUMN AMP I36
insramp P1N
BIT ROM COLUMN AMP I38
insramp P1N
DEC<34>
DEC<35>
DEC<36>
DEC<37>
I1521 I1545 I1526 I1538 I1529 I1541
I1138 I873 I1135 I844 I1132 I815
I1139 I874 I1134 I845 I816 I1133
I1140 I875 I1194 I846 I1193 I817

Fig 1.0502BB

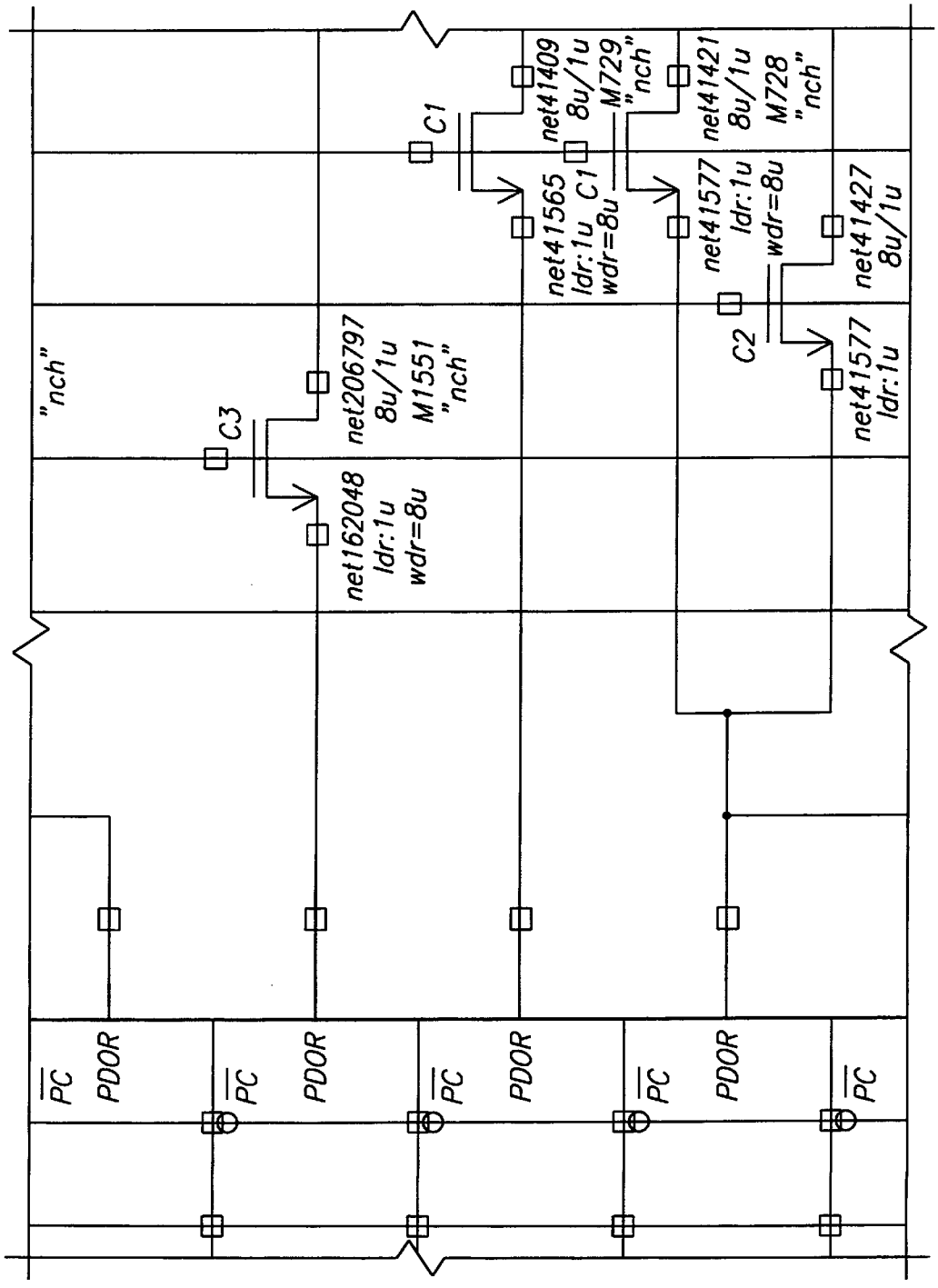


FIG. 1,005,281C

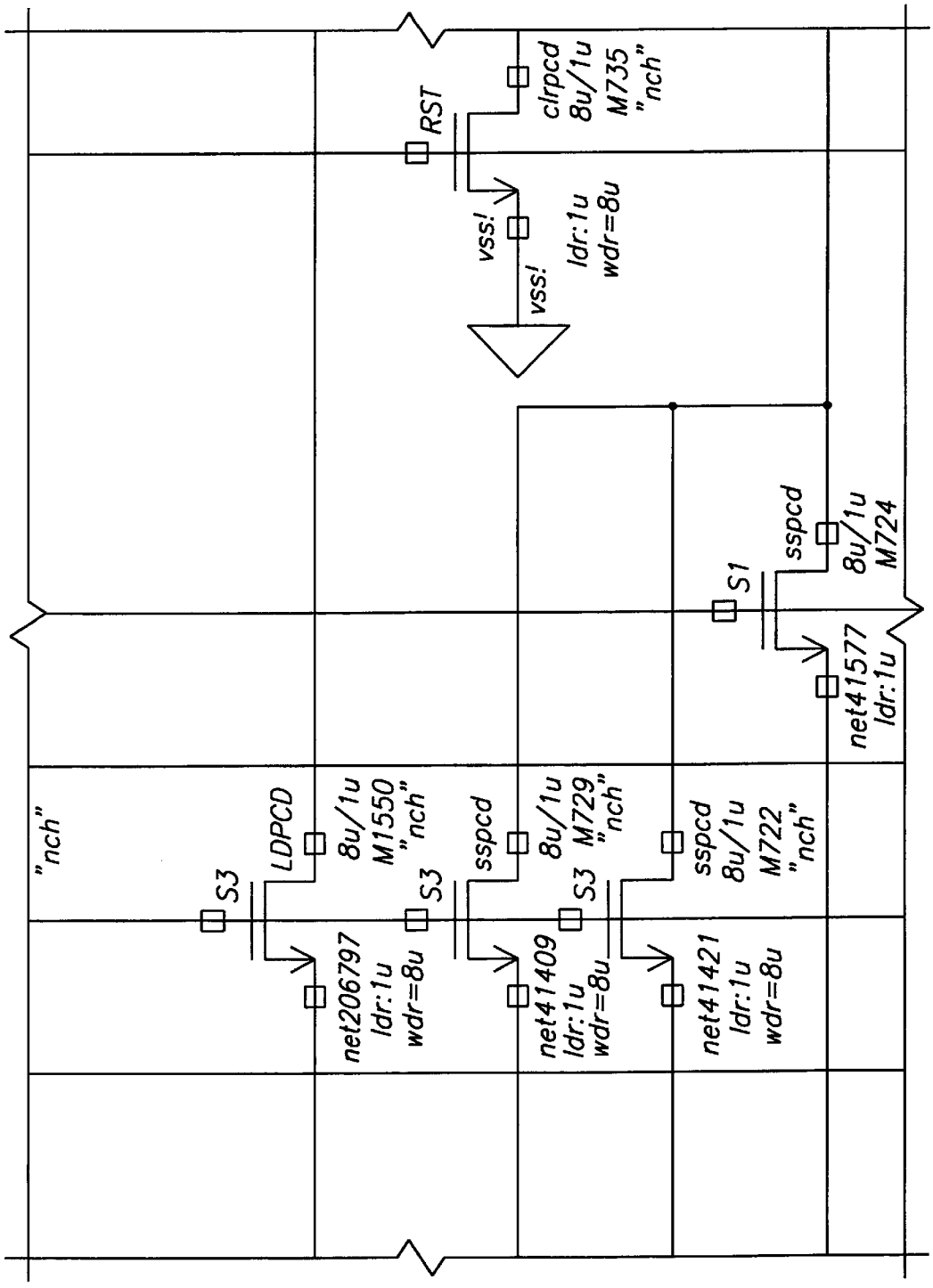


FIG. 1L.0056200

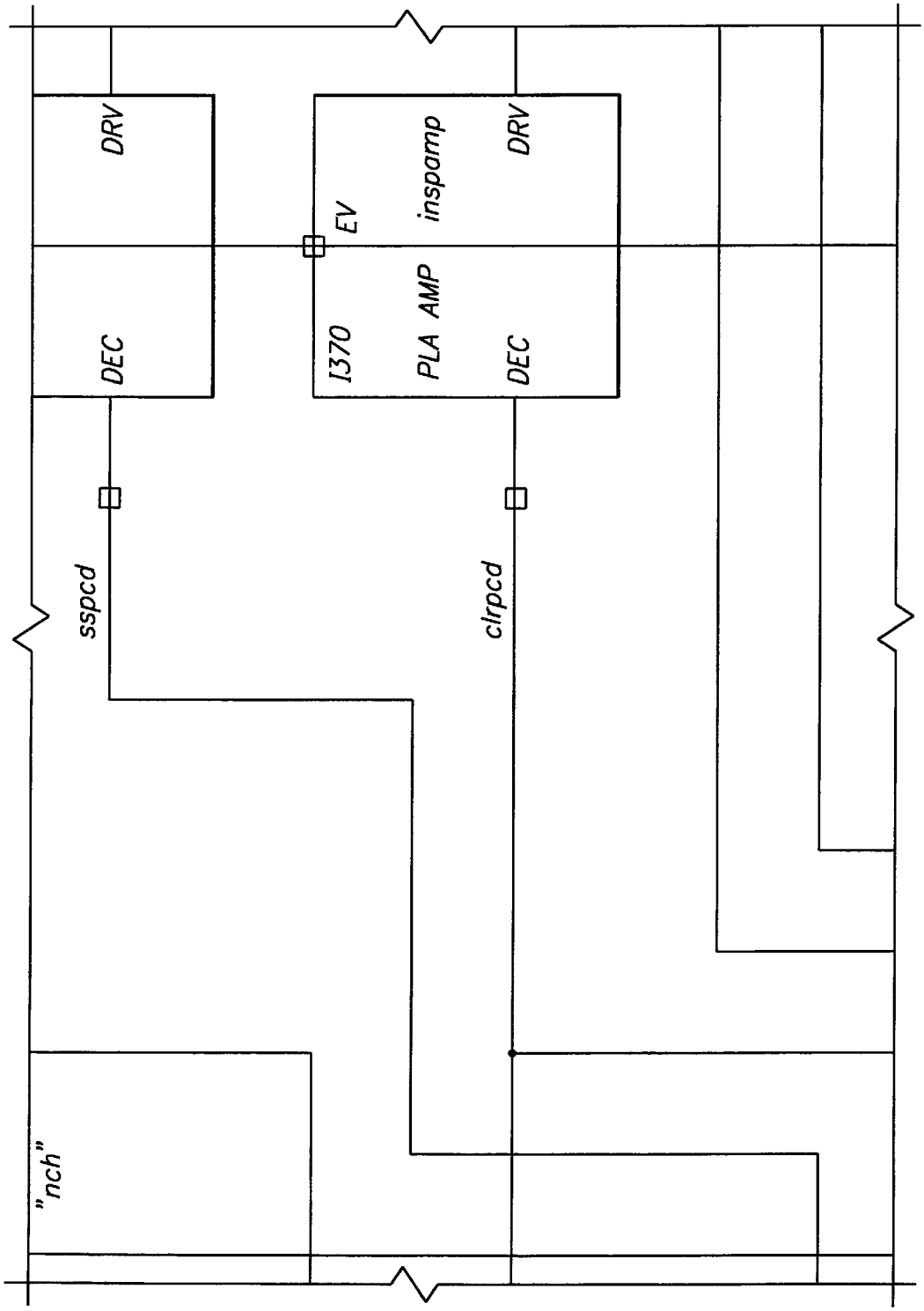


FIG 1.0602BE

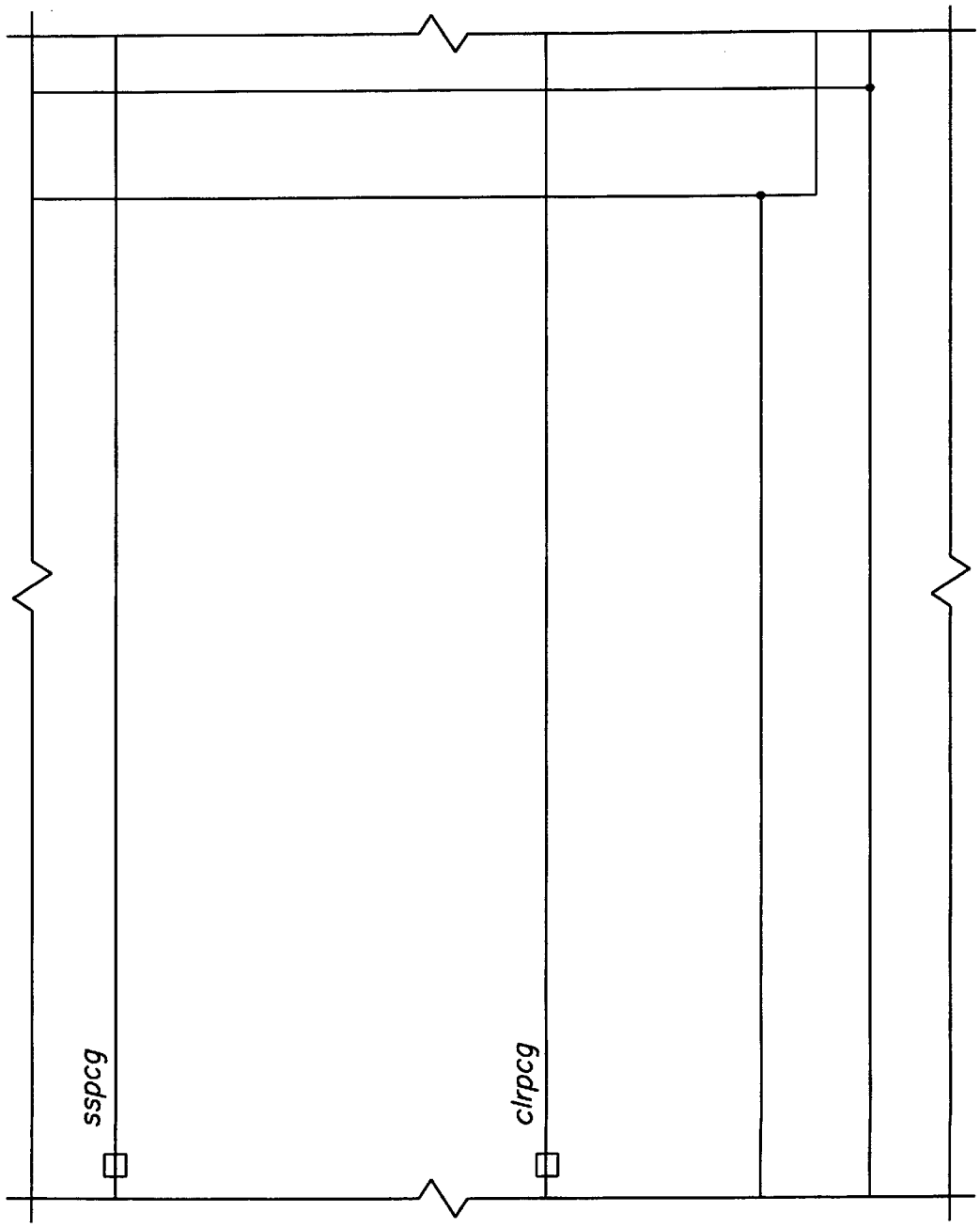


FIG 1,060,218

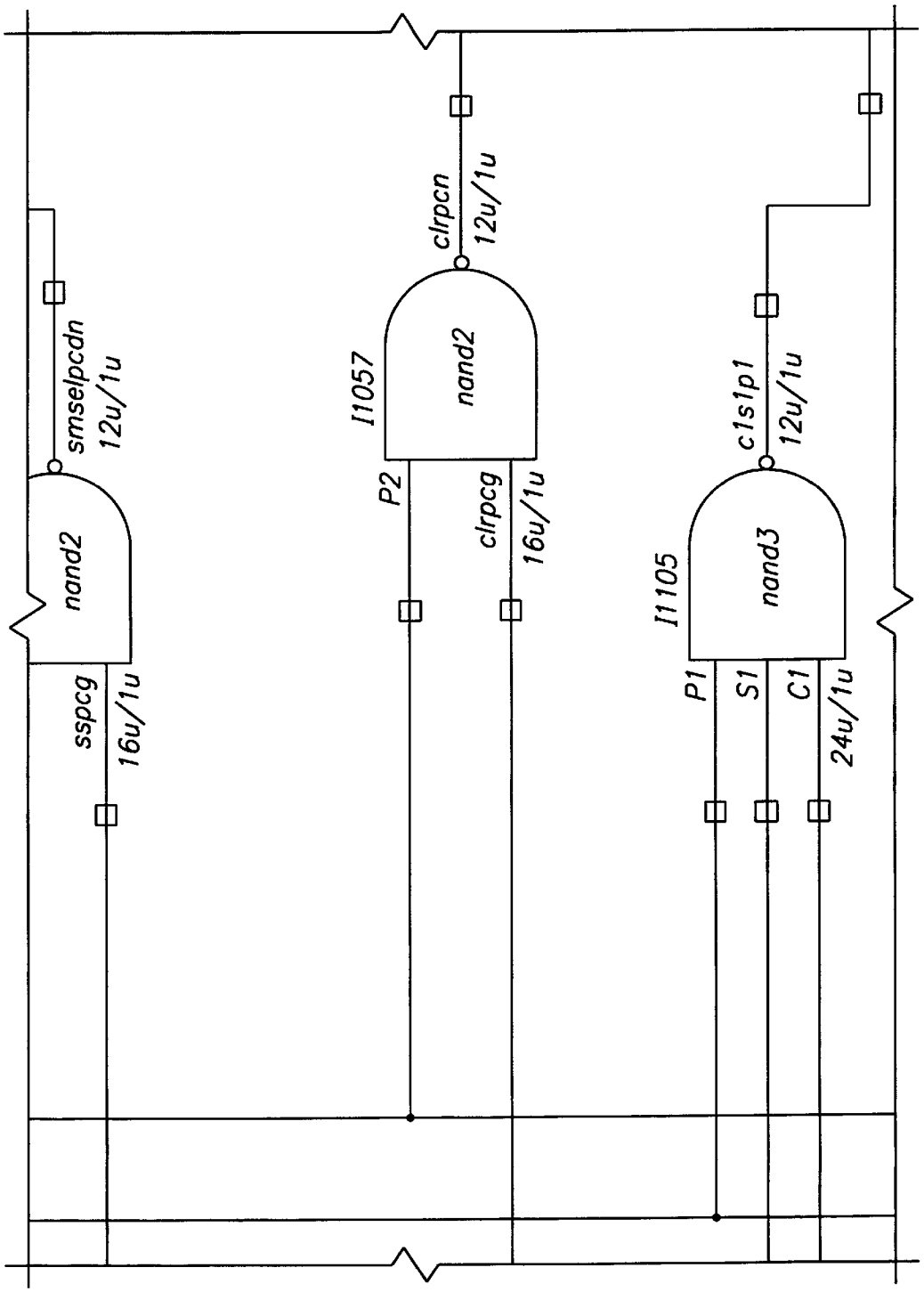

smselpcdn
12u/1u
nand2
sspcg
16u/1u
I1057
nand2
clrpcn
12u/1u
P2
clrpcg
16u/1u
I1105
nand3
c1s1p1
12u/1u
P1
S1
C1
24u/1u

FIG 7.006,208

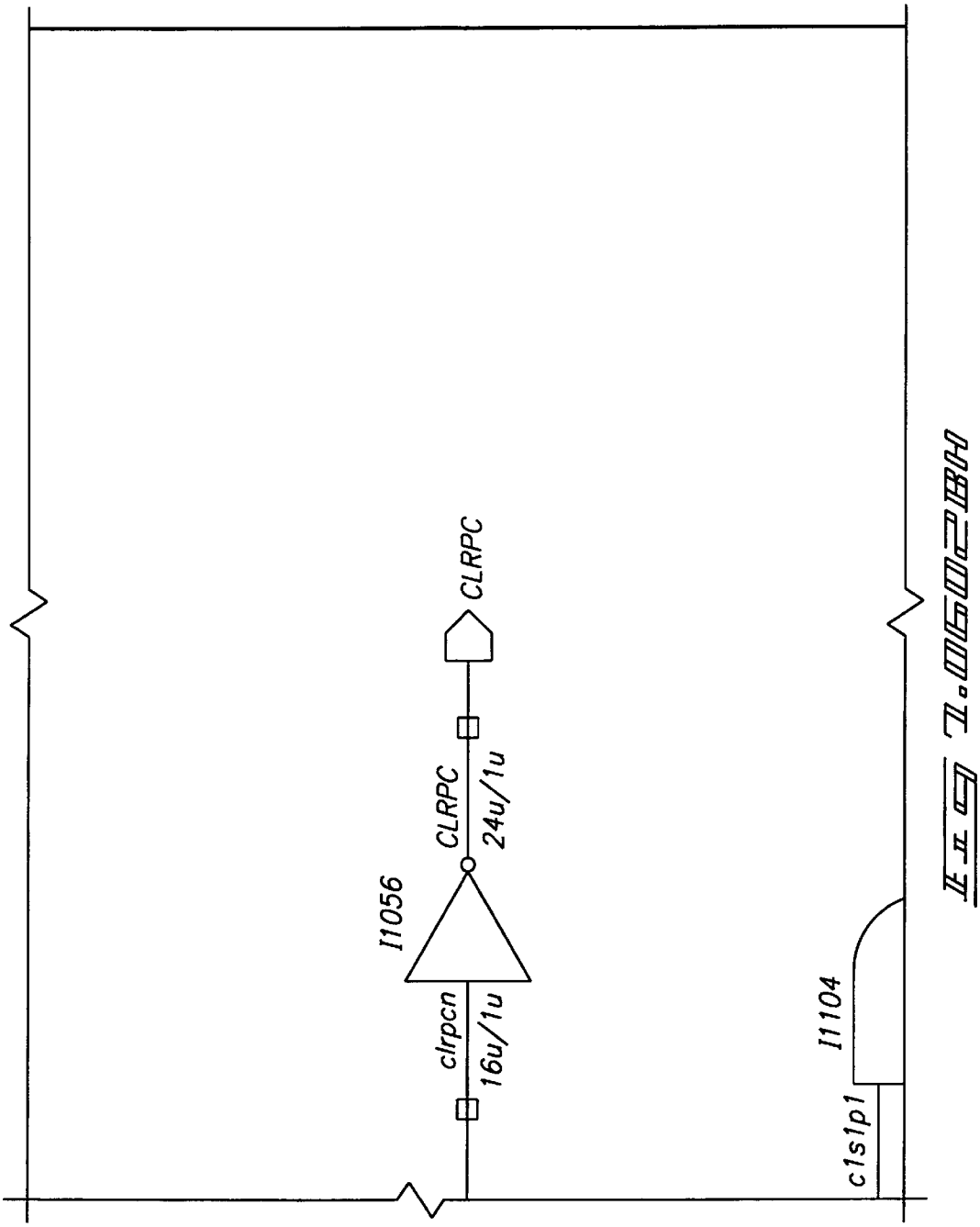


FIG 1,060,284

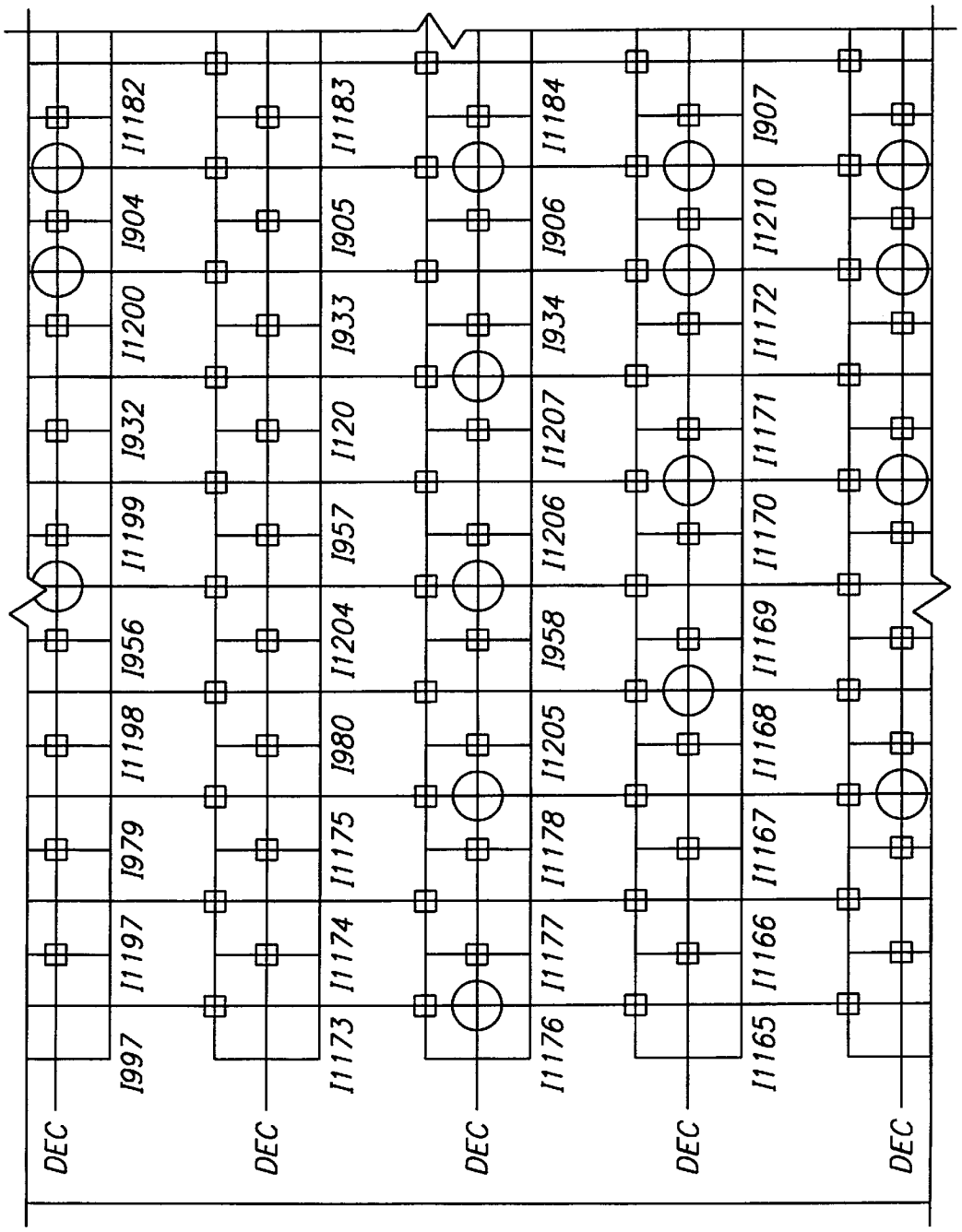

DEC
DEC
DEC
DEC
DEC
I997
I1197
I979
I1198
I956
I1199
I932
I1200
I904
I1182
I1173
I1174
I1175
I980
I1204
I957
I120
I933
I1183
I905
I1176
I1177
I1178
I1205
I958
I1206
I1207
I934
I1184
I906
I1165
I1166
I1167
I1168
I1169
I1170
I1171
I1172
I1210
I907

FIG. 1L

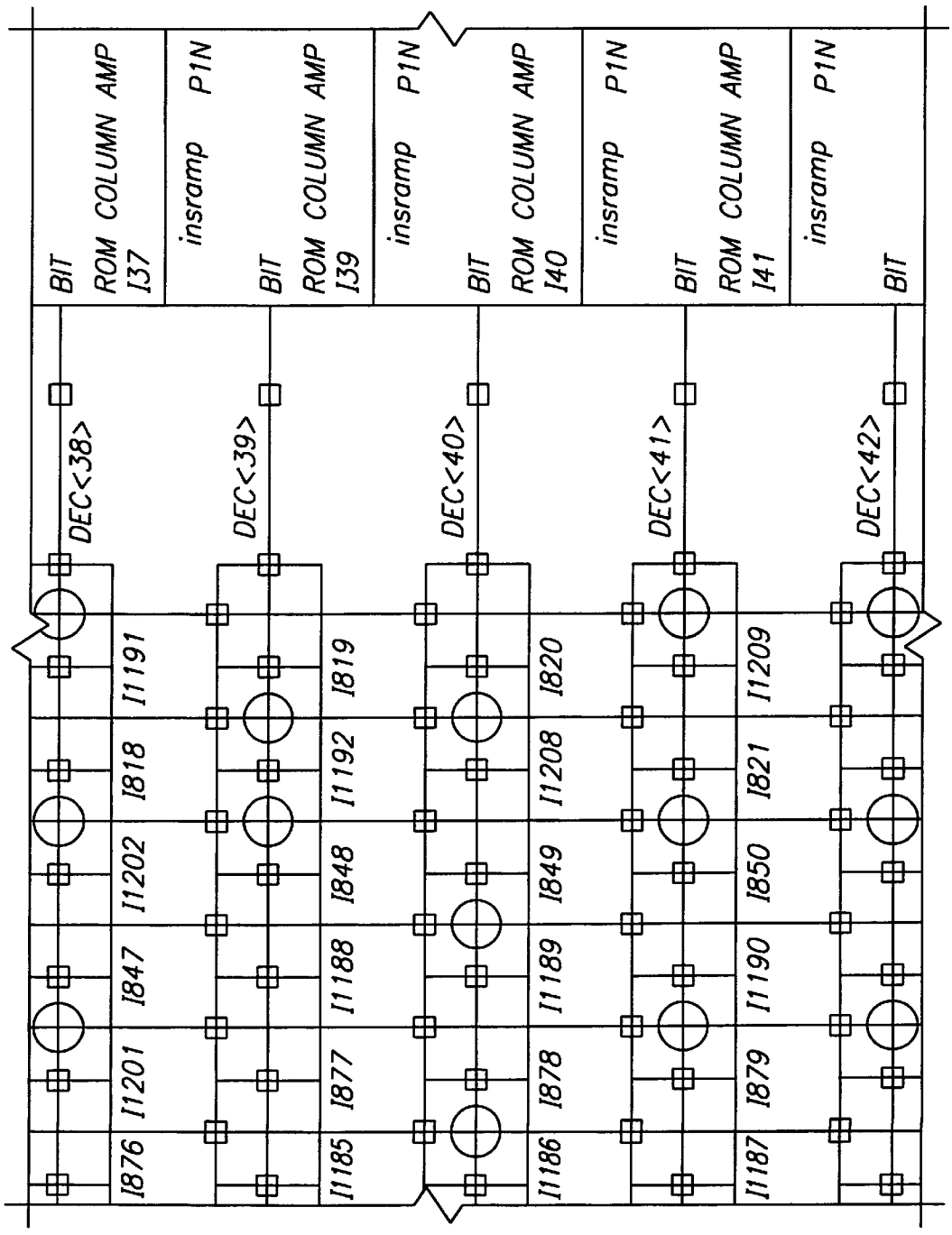

BIT
ROM COLUMN AMP
I37
insramp P1N
BIT
ROM COLUMN AMP
I39
insramp P1N
BIT
ROM COLUMN AMP
I40
insramp P1N
BIT
ROM COLUMN AMP
I41
insramp P1N
BIT
DEC<38>
DEC<39>
DEC<40>
DEC<41>
DEC<42>
I1191
I818
I1202
I847
I1201
I876
I819
I1192
I848
I1188
I877
I1185
I820
I1208
I849
I1189
I878
I1186
I1209
I821
I850
I1190
I879
I1187

FIG 1.0500.2E

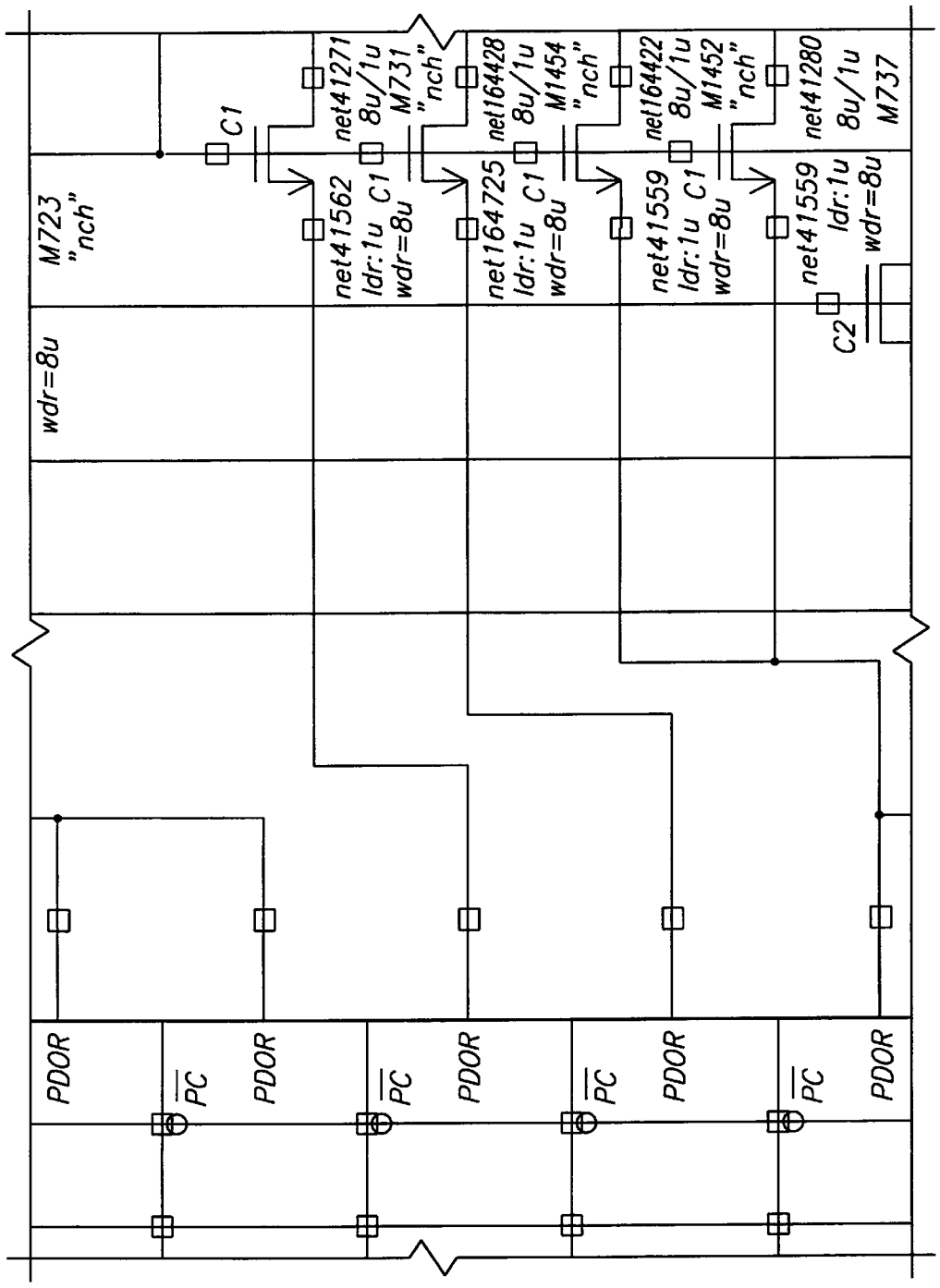

M723
"nch"
wdr=8u
C1
net41562
ldr:1u
wdr=8u
net41271
8u/1u
M731
"nch"
net164725
ldr:1u
wdr=8u
net164428
8u/1u
M1454
"nch"
net41559
ldr:1u
wdr=8u
net164422
8u/1u
M1452
"nch"
C2
net41559
ldr:1u
wdr=8u
net41280
8u/1u
M737
PDOR
PC
PDOR
PC
PDOR
PC
PDOR
PC
PDOR

FIG. 1,600,811

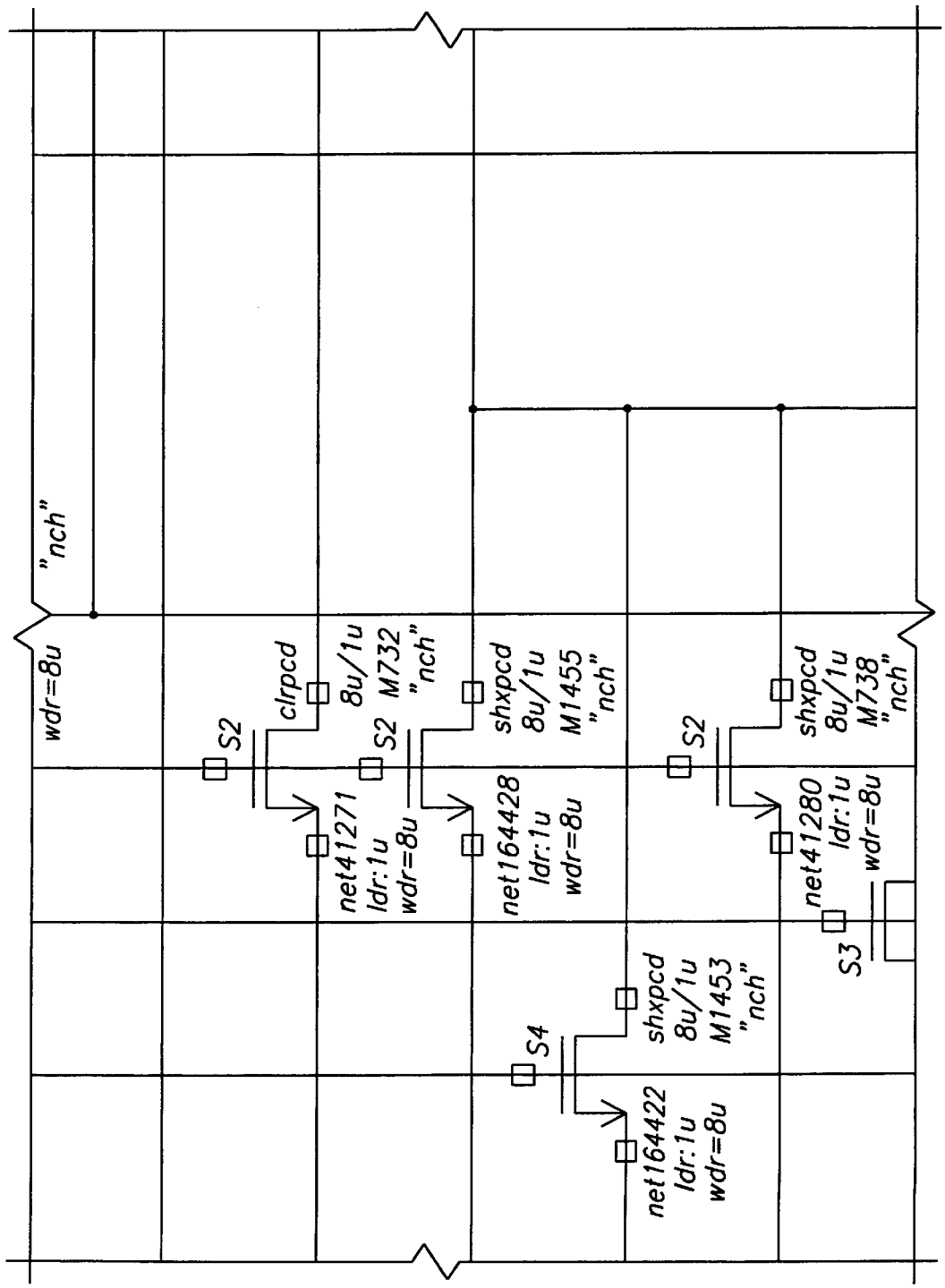

wdr=8u
"nch"
S2
clrpcd
8u/1u
S2
M732
"nch"
shxpcd
8u/1u
M1455
"nch"
S2
shxpcd
8u/1u
M738
"nch"
net41271
ldr:1u
wdr=8u
net164428
ldr:1u
wdr=8u
net41280
ldr:1u
wdr=8u
S3
S4
shxpcd
8u/1u
M1453
"nch"
net164422
ldr:1u
wdr=8u

FIG. 1,005,210

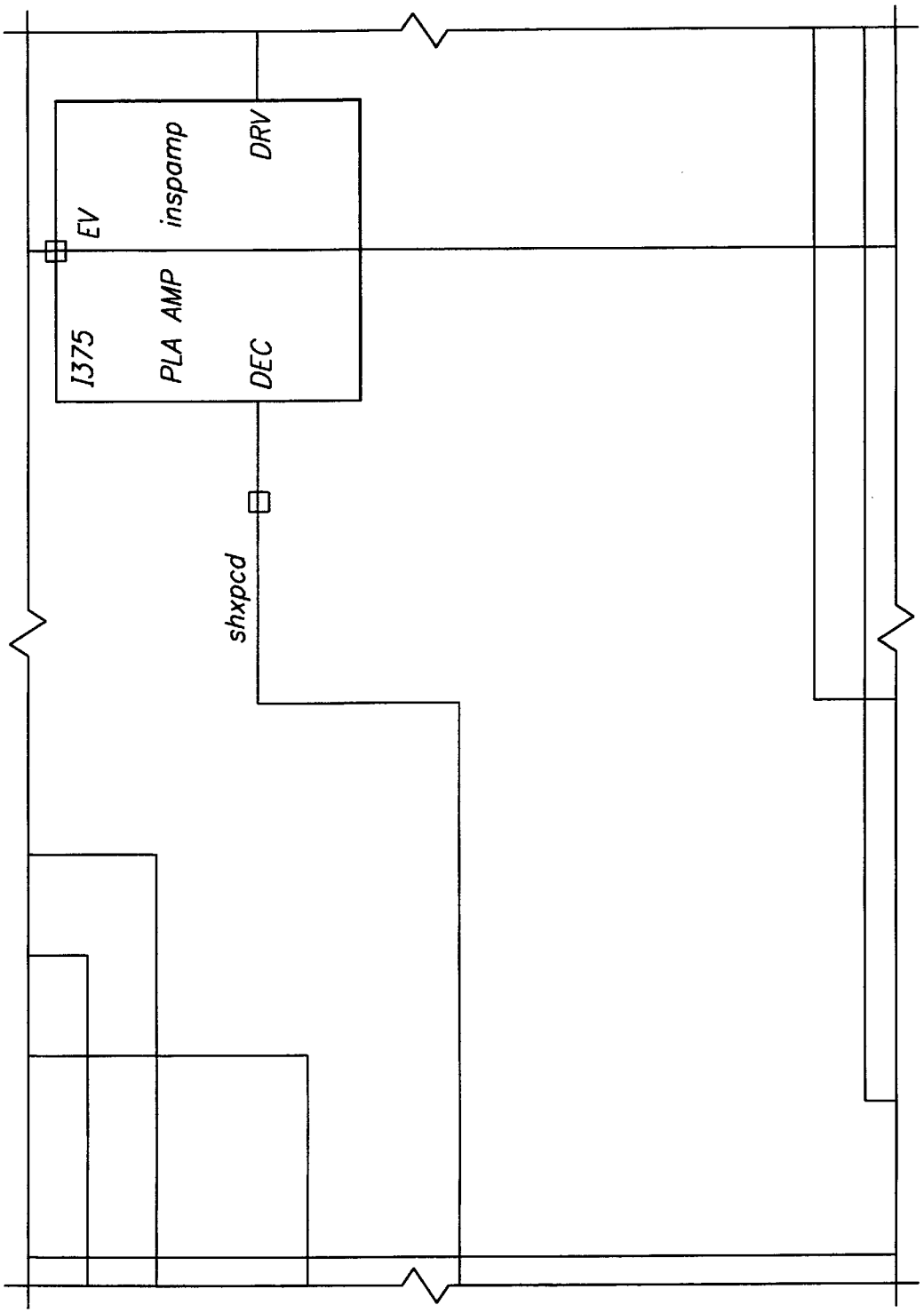


FIG 1.0602E

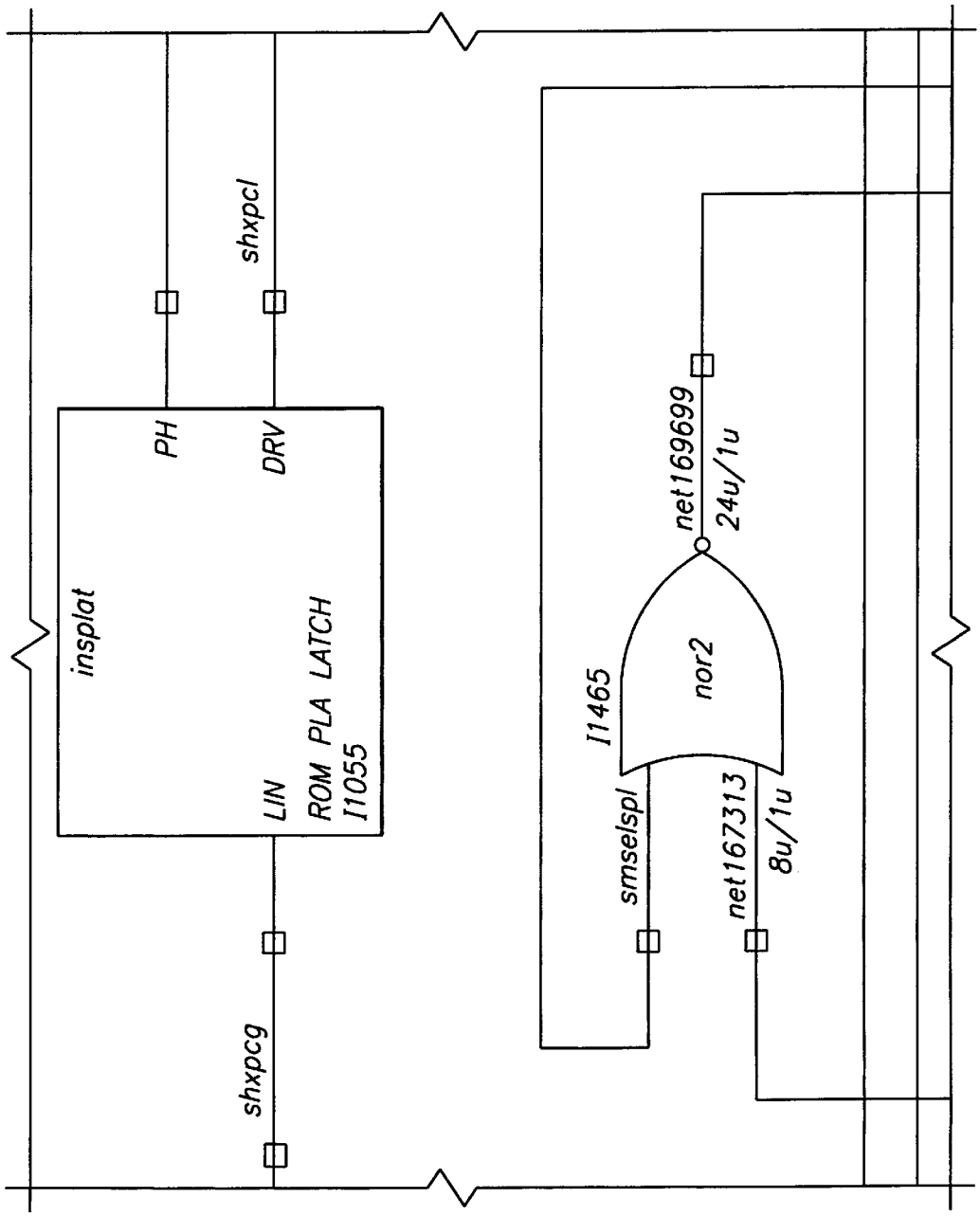

shxpcl
PH
DRV
insplat
ROM PLA LATCH
I1055
LIN
shxpcg
net169699
24u/1u
I1465
nor2
smselspl
net167313
8u/1u

FIG 1,060,2CF

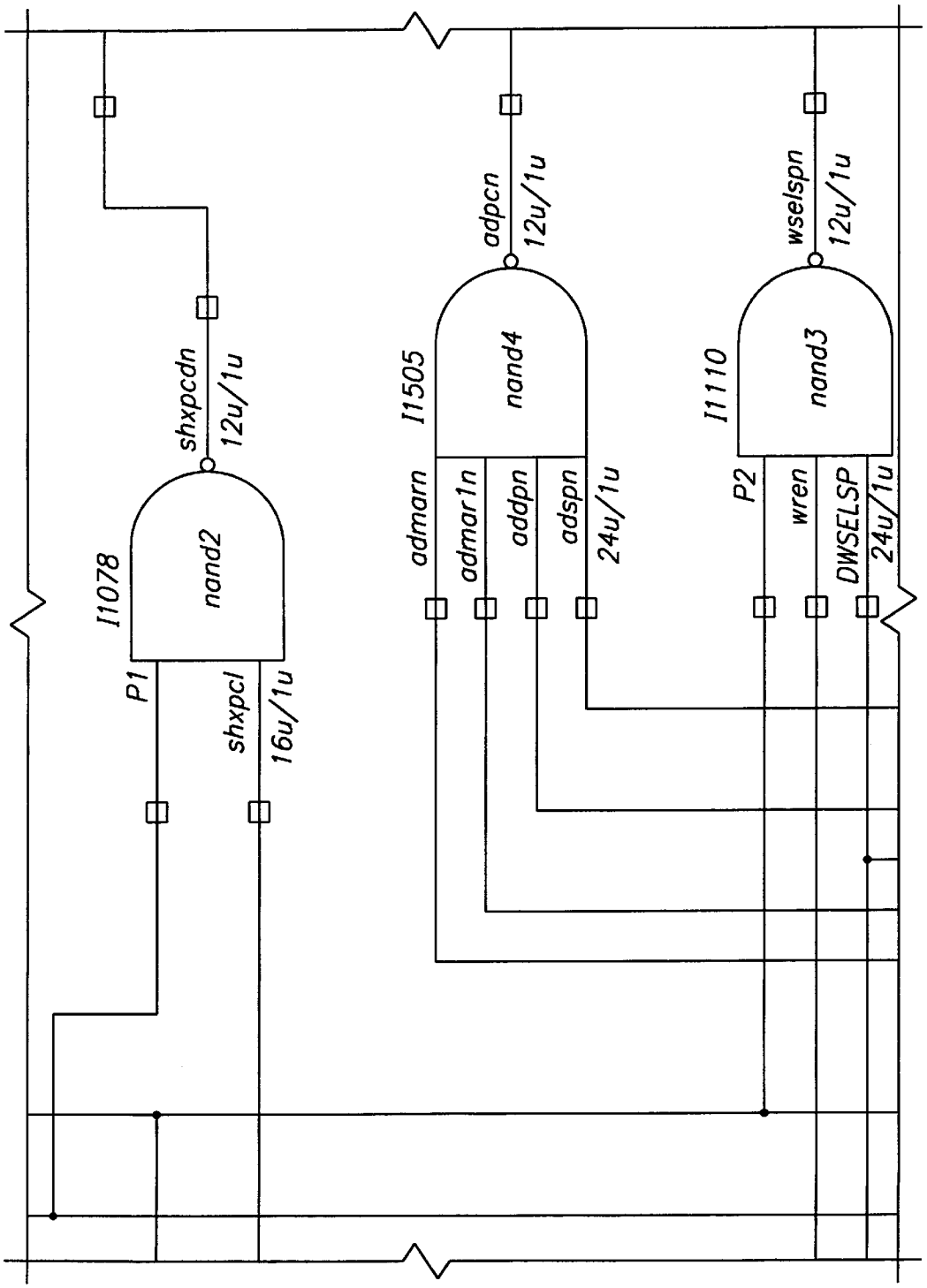

I1078
nand2
P1
shxpcdn
12u/1u
shxpcl
16u/1u
I1505
nand4
admarn
admar1n
addpn
adspn
adpcn
12u/1u
24u/1u
I1110
nand3
P2
wren
DWSELSP
wselspn
12u/1u
24u/1u

FIG. 6,130,602

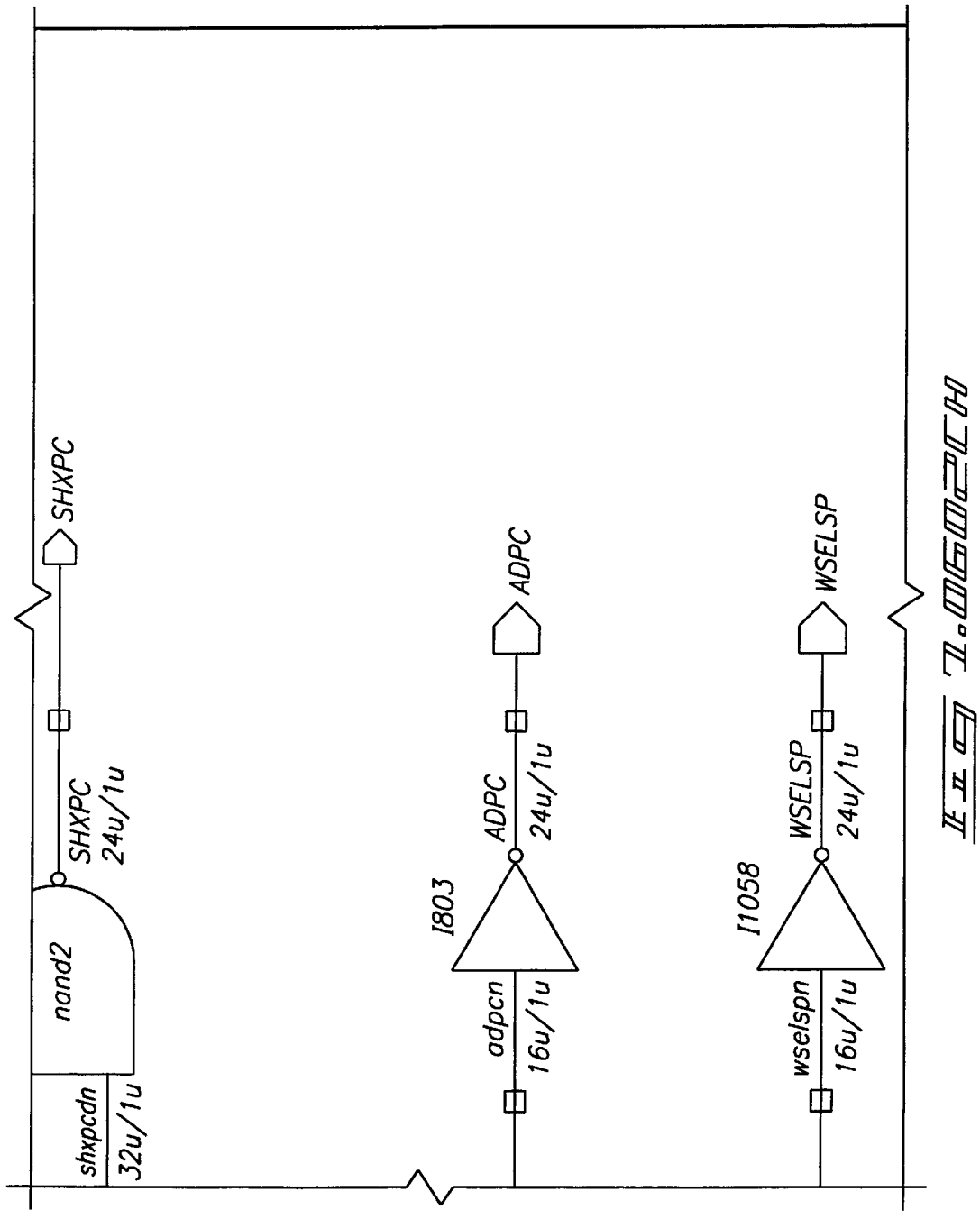

SHXPC
SHXPC
24u/1u
nand2
shxpcdn
32u/1u
ADPC
ADPC
24u/1u
I803
adpcn
16u/1u
WSELSP
WSELSP
24u/1u
I1058
wselspn
16u/1u

FIG. 6.00912

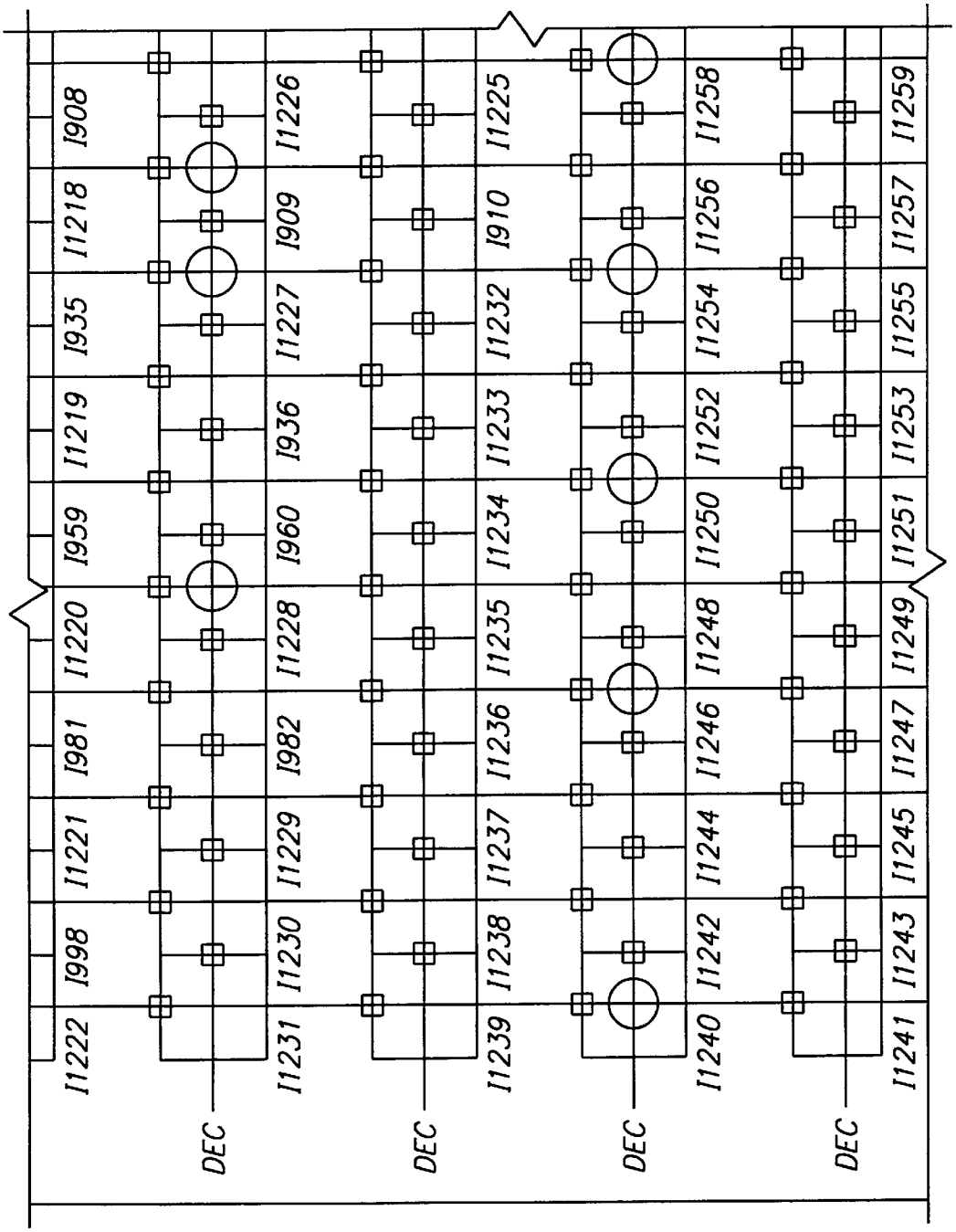


FIG. 1,005,011A

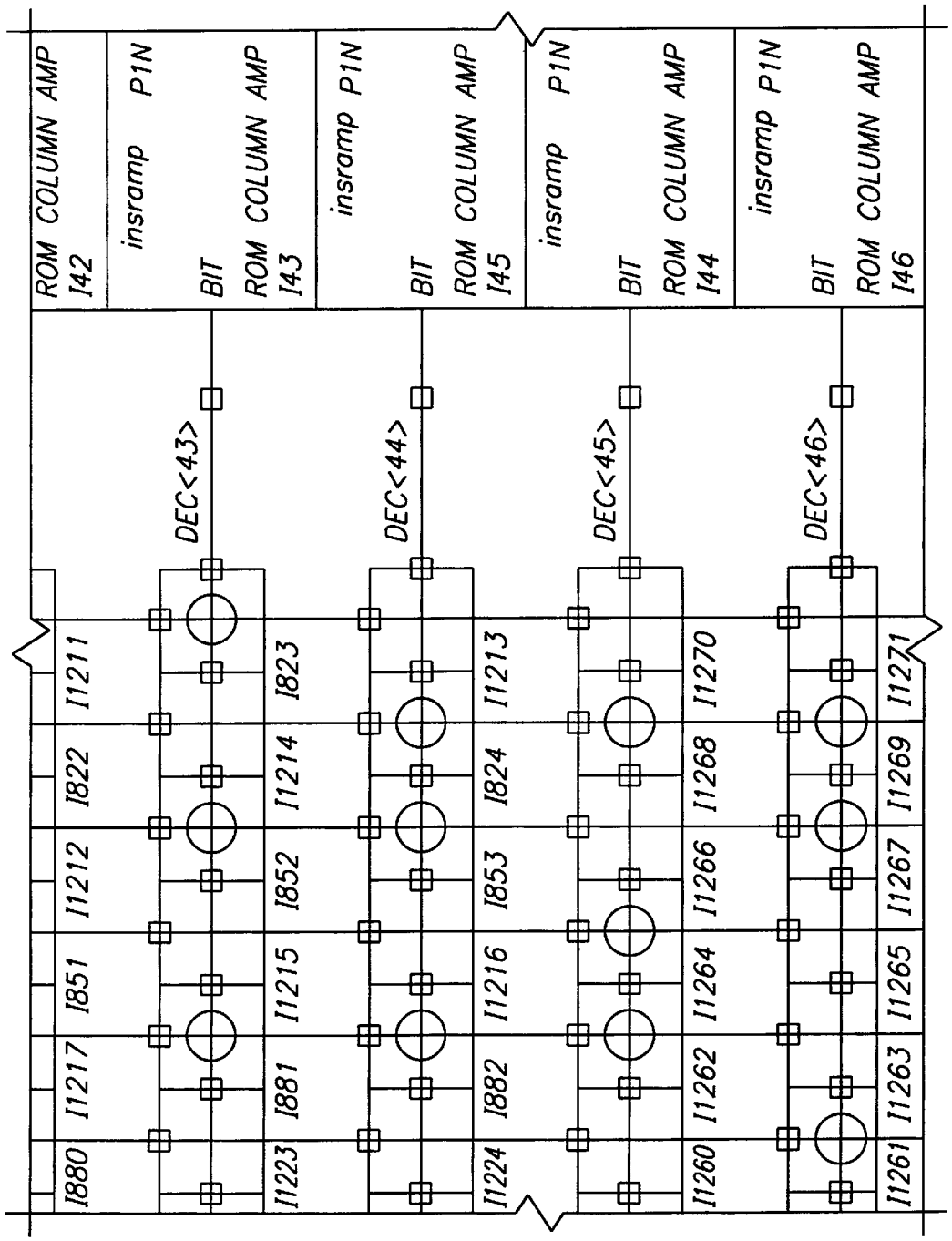


FIG. 11,006,008

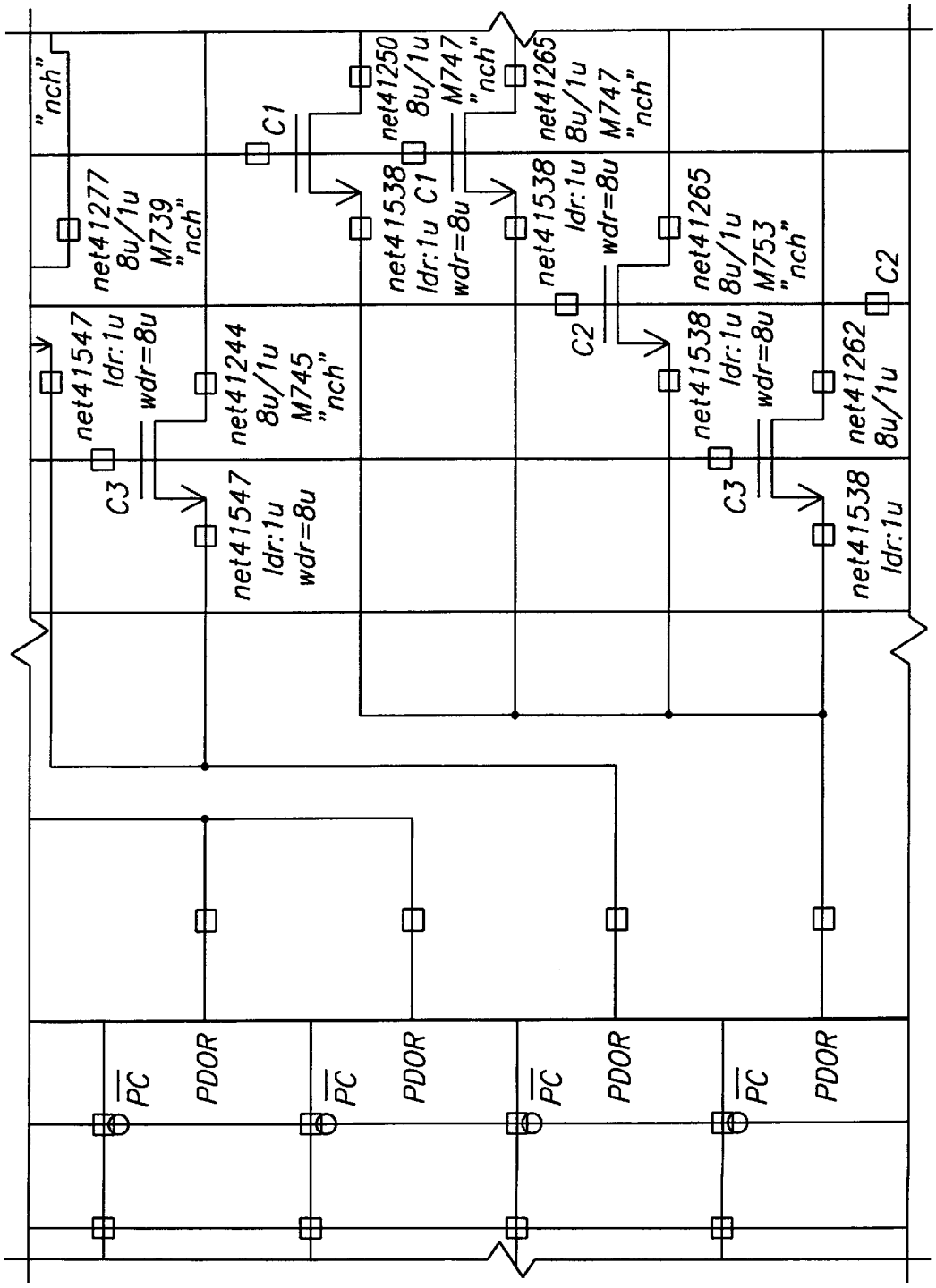

"nch"
net41277
8u/1u
M739
"nch"
C1
net41250
8u/1u
M747
"nch"
net41265
8u/1u
M747
"nch"
net41538
ldr:1u C1
wdr=8u
net41538
ldr:1u
wdr=8u
net41265
8u/1u
M753
"nch"
C2
net41547
ldr:1u
wdr=8u
net41244
8u/1u
M745
"nch"
C2
net41538
ldr:1u
wdr=8u
net41262
8u/1u
C3
C3
net41547
ldr:1u
wdr=8u
net41538
ldr:1u
PC
PDOR
PC
PDOR
PC
PDOR
PC
PDOR

FIG 1,005,200

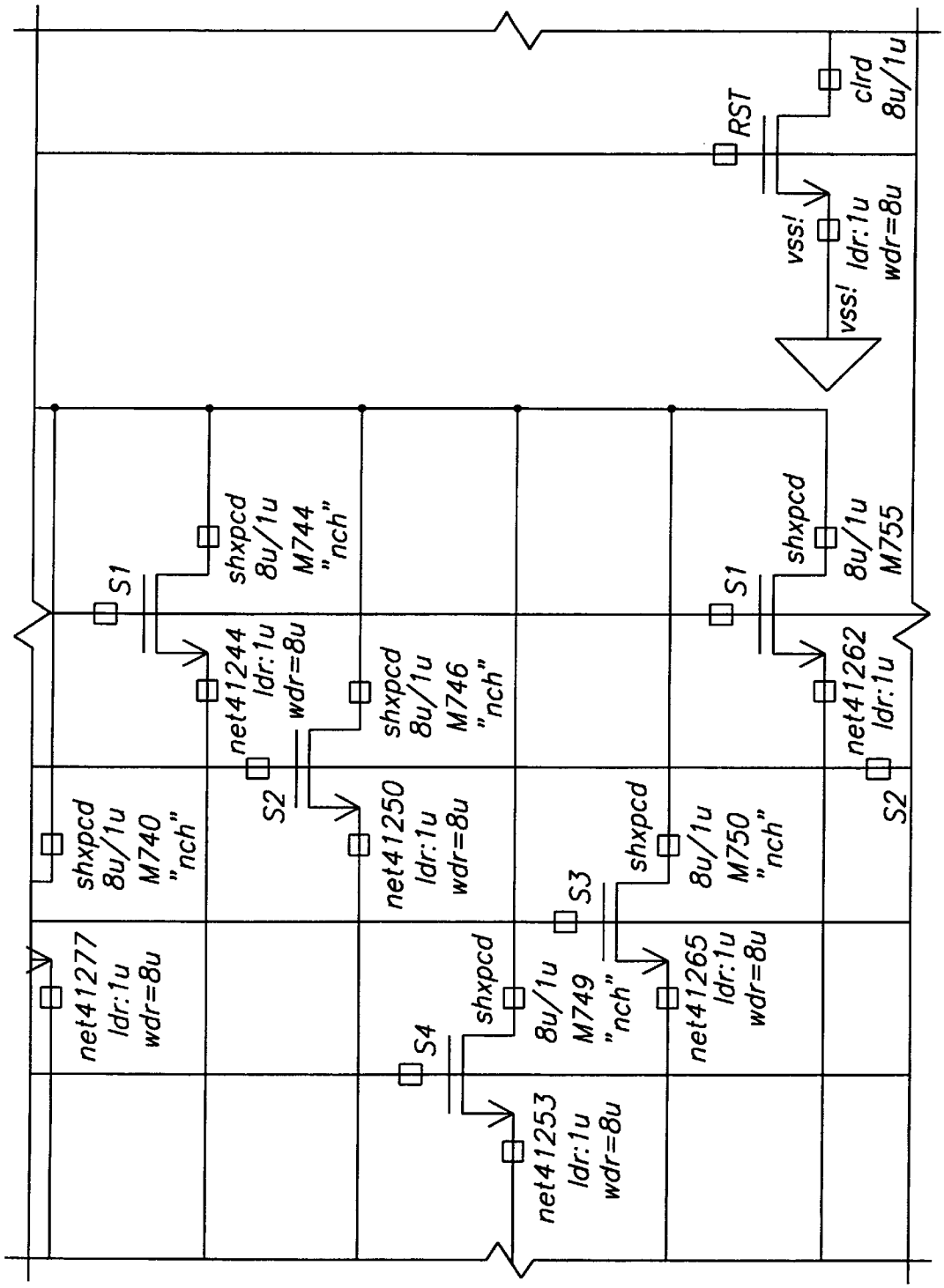

RST
clrd
8u/1u
vss!
ldr:1u
wdr=8u
vss!
S1
shxpcd
8u/1u
M744
"nch"
net41244
ldr:1u
wdr=8u
shxpcd
8u/1u
M746
"nch"
S1
shxpcd
8u/1u
M755
net41262
ldr:1u
S2
shxpcd
8u/1u
M740
"nch"
net41277
ldr:1u
wdr=8u
S2
net41250
ldr:1u
wdr=8u
S3
shxpcd
8u/1u
M750
"nch"
net41265
ldr:1u
wdr=8u
S4
shxpcd
8u/1u
M749
"nch"
net41253
ldr:1u
wdr=8u

FIG. 1.0602D

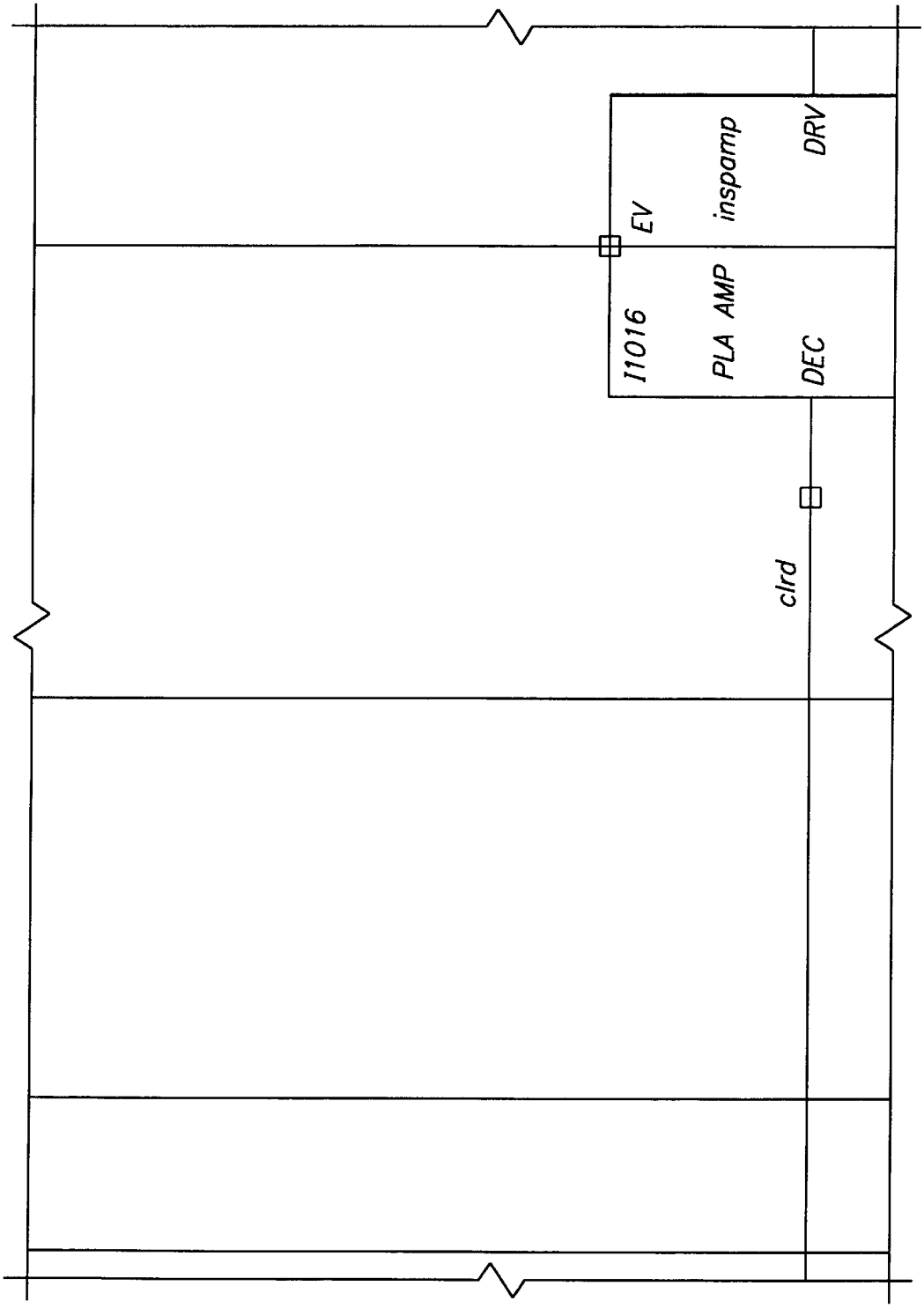


FIG 11,059,602E

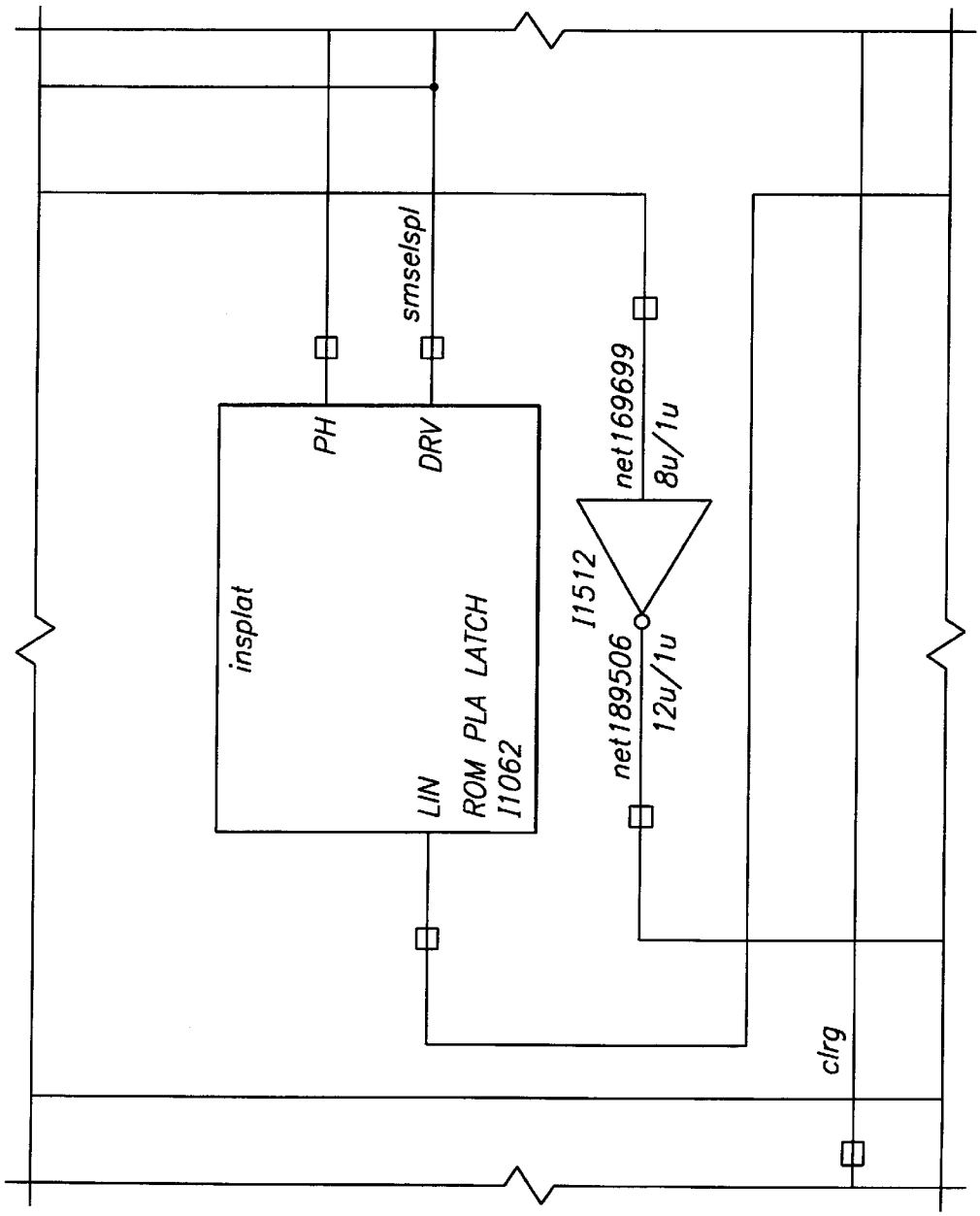

smselspl
PH
DRV
net169699
8u/1u
I1512
net189506
12u/1u
insplat
LIN
ROM PLA LATCH
I1062
clrg

FIG 1.0502DF

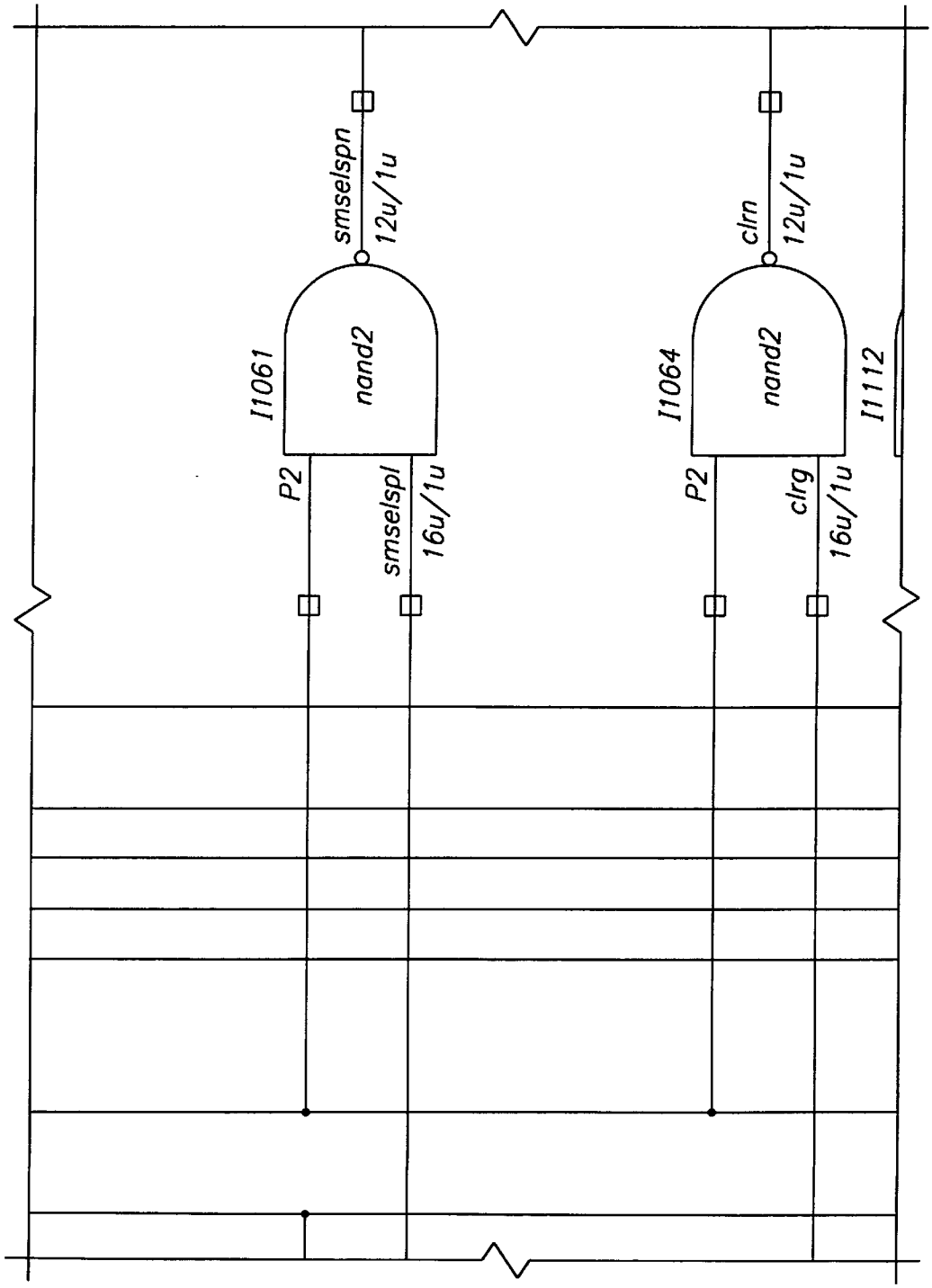

smselspn
12u/1u
I1061
nand2
P2
smselspl
16u/1u
clrn
12u/1u
I1064
nand2
I1112
P2
clrg
16u/1u

FIG 1.0502DS

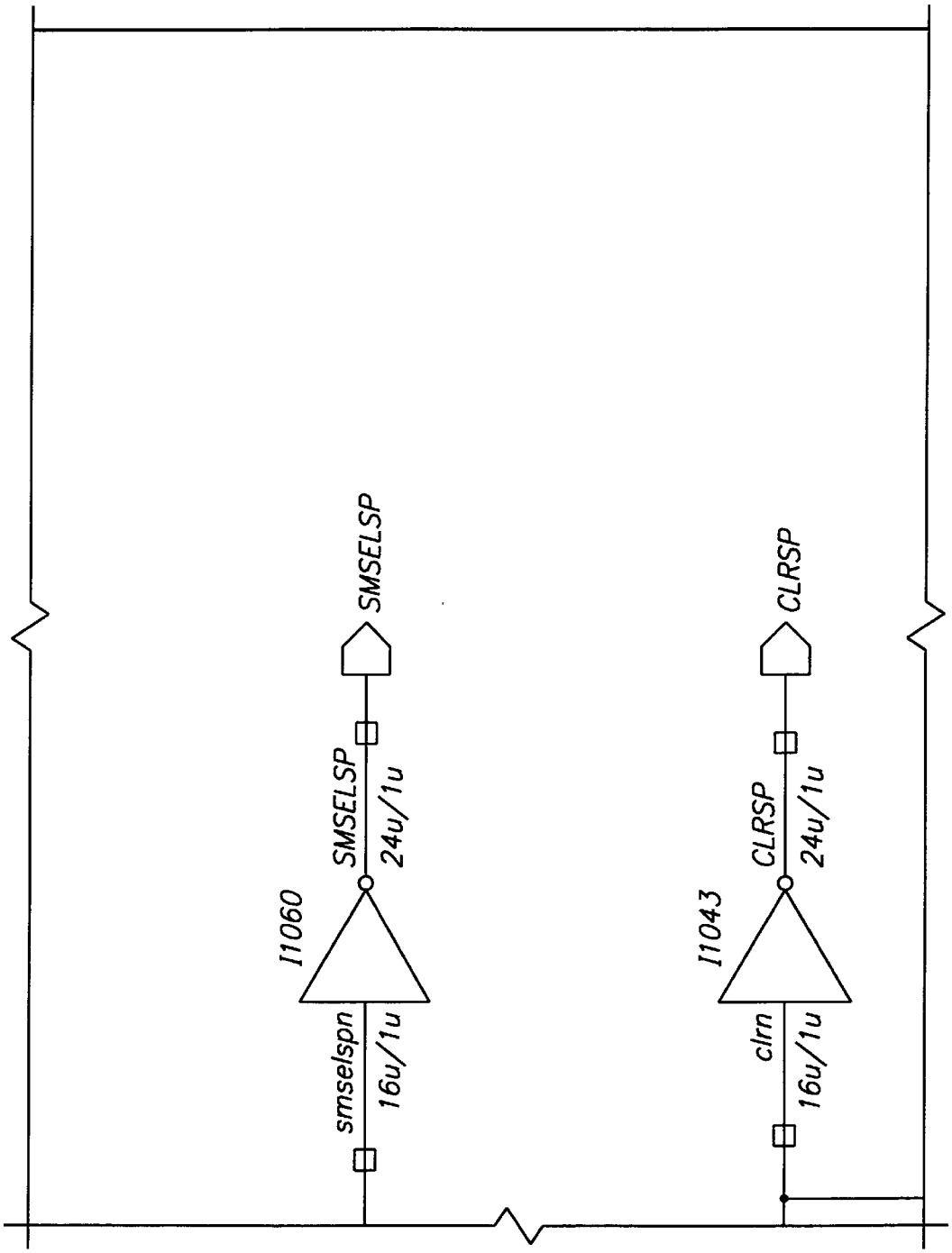

SMSELSP
SMSELSP
24u/1u
I1060
smselspn
16u/1u
CLRSP
CLRSP
24u/1u
I1043
clrn
16u/1u

FIG 1,060,211

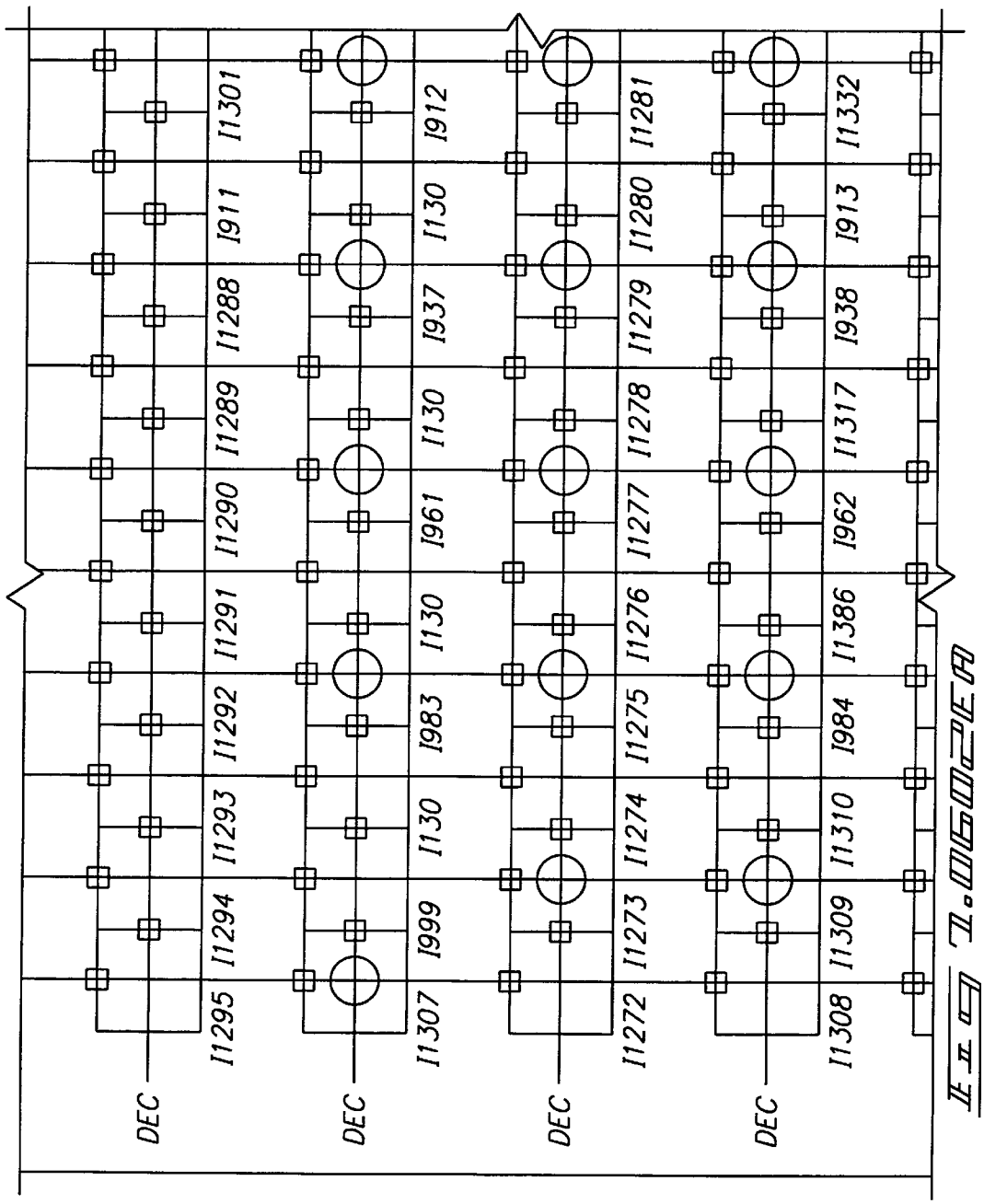
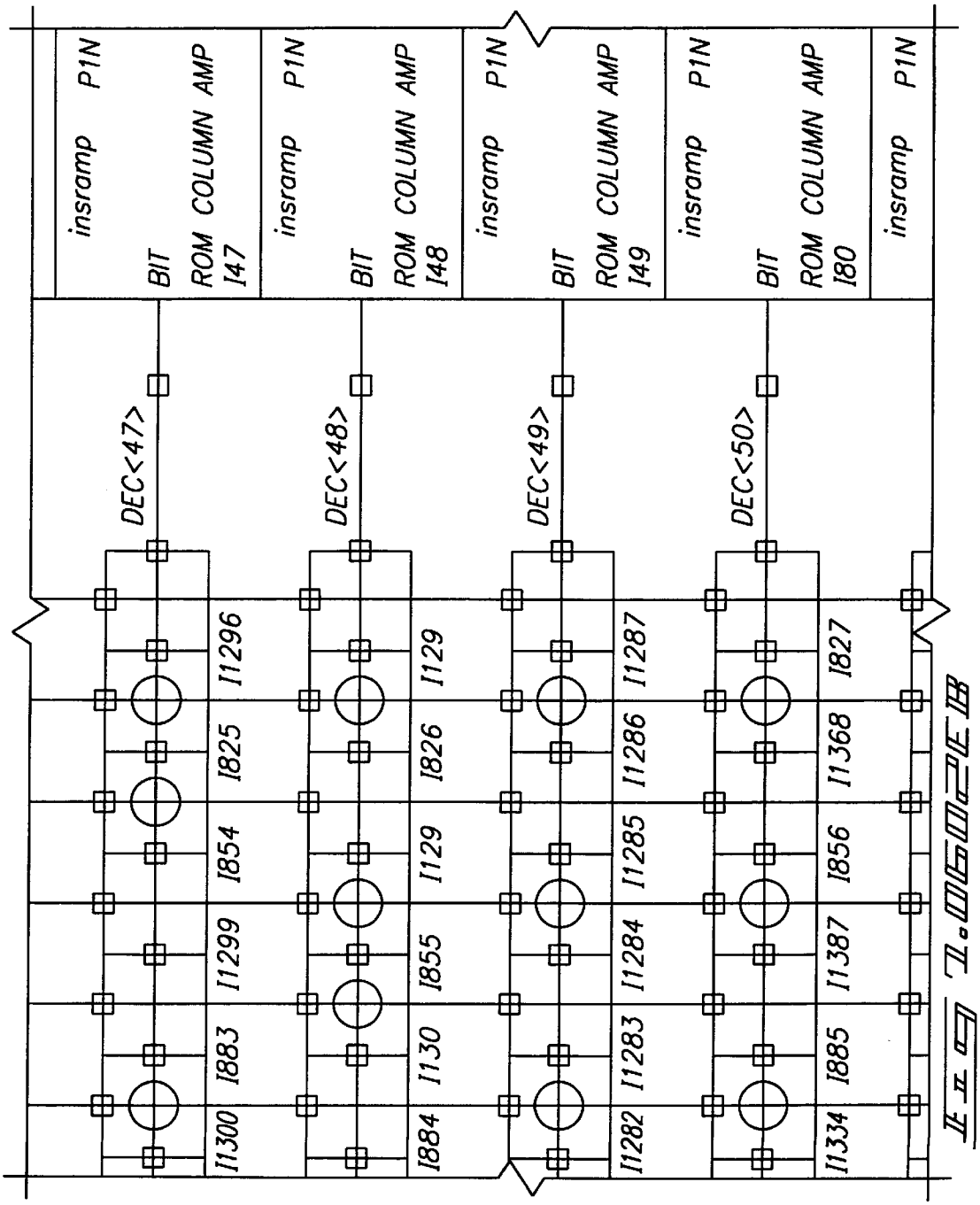


FIG 1.0600E+00


insramp P1N
BIT ROM COLUMN AMP I47
insramp P1N
BIT ROM COLUMN AMP I48
insramp P1N
BIT ROM COLUMN AMP I49
insramp P1N
BIT ROM COLUMN AMP I80
insramp P1N
DEC<47>
DEC<48>
DEC<49>
DEC<50>
I1300 I883 I1299 I854 I825 I1296
I884 I130 I855 I129 I826 I129
I1282 I1283 I1284 I1285 I1286 I1287
I1334 I885 I1387 I856 I1368 I827

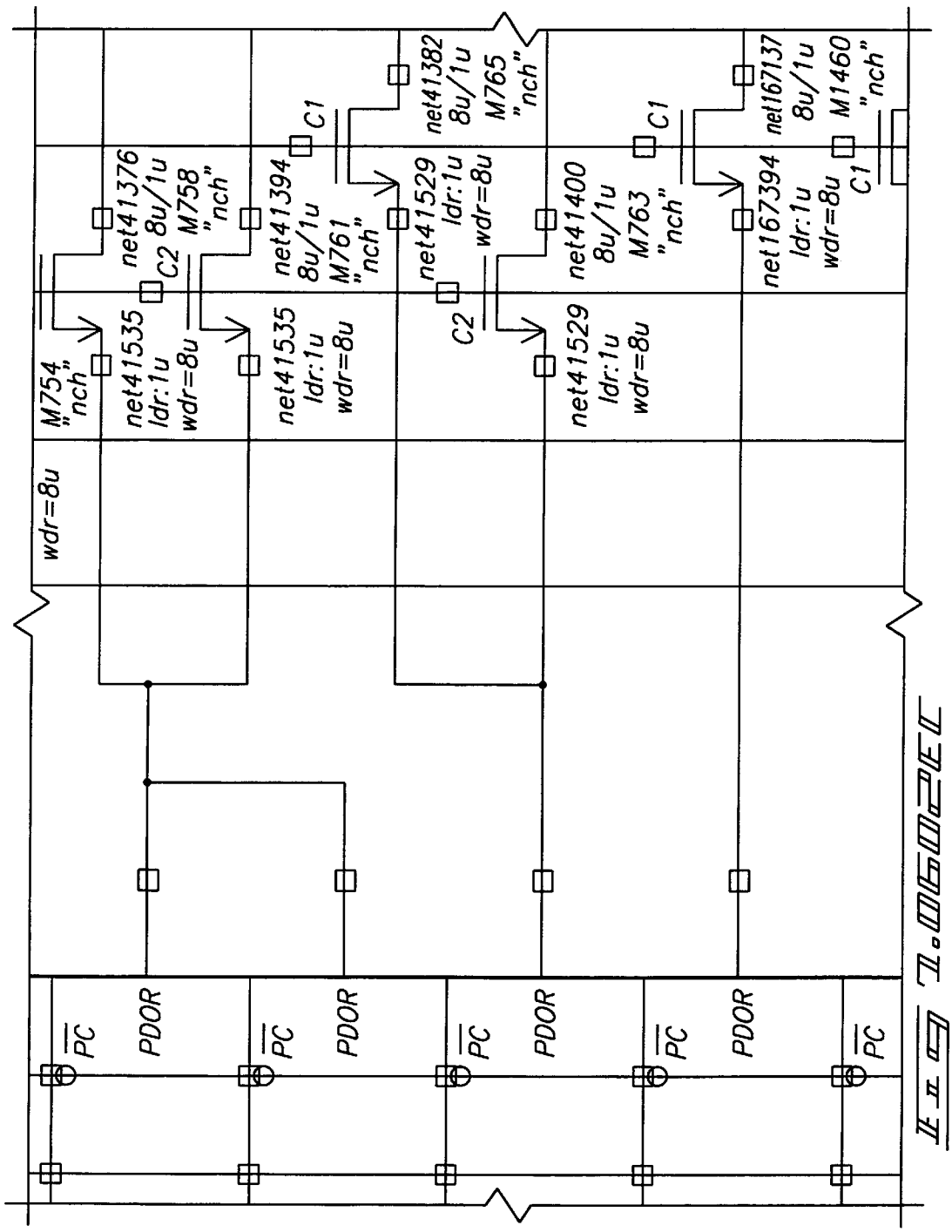

M754 "nch"
net41535 ldr:1u wdr=8u
C2 8u/1u M758 "nch"
net41376
net41535 ldr:1u wdr=8u
C1 8u/1u M761 "nch"
net41394
net41529 ldr:1u wdr=8u
C2
C1 8u/1u M765 "nch"
net41382
net41529 ldr:1u wdr=8u
C1 8u/1u M763 "nch"
net41400
net167394 ldr:1u wdr=8u
C1 8u/1u M1460 "nch"
net167137
wdr=8u
PC PDOR
PC PDOR
PC PDOR
PC PDOR
PC

FIG. 6,130,602

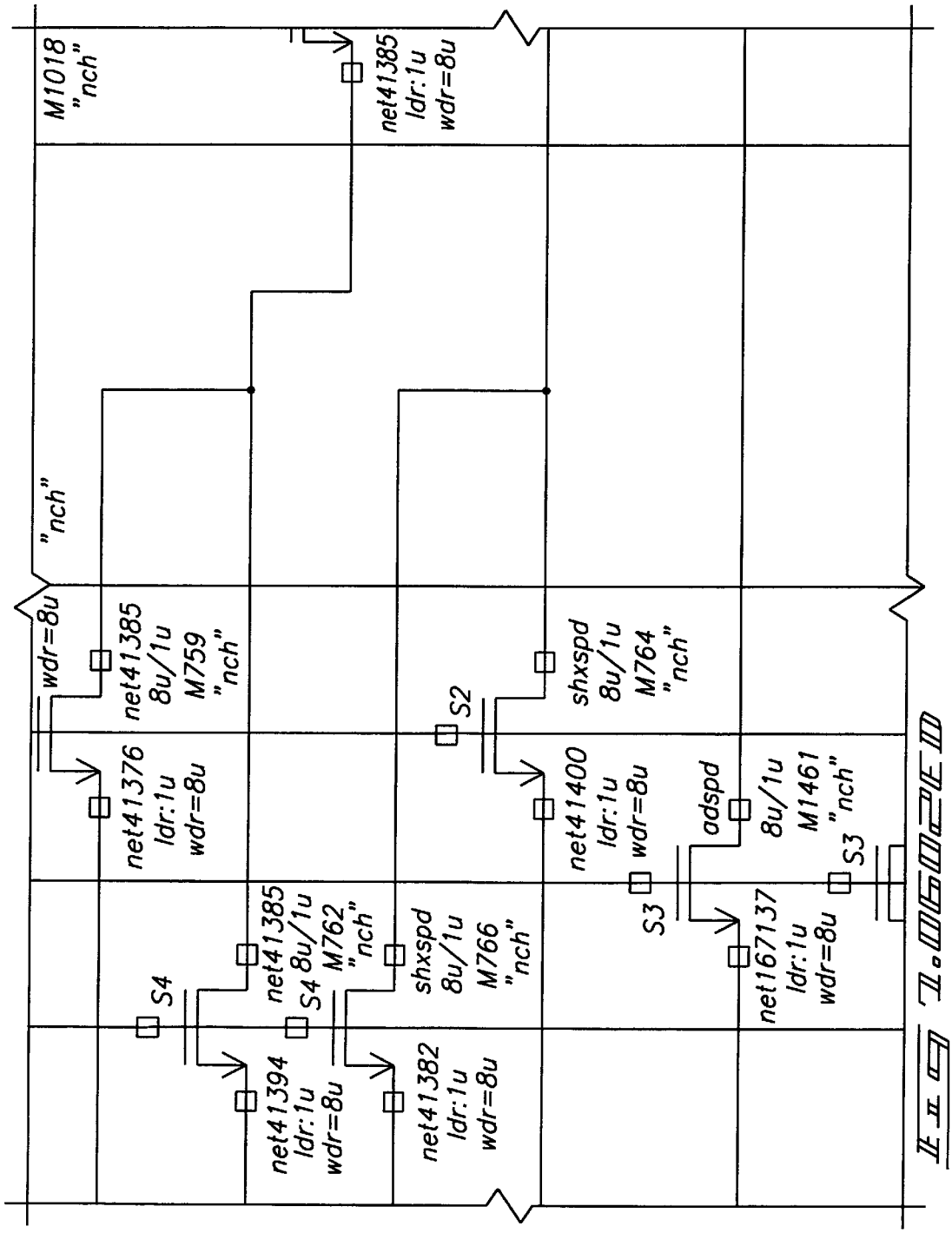
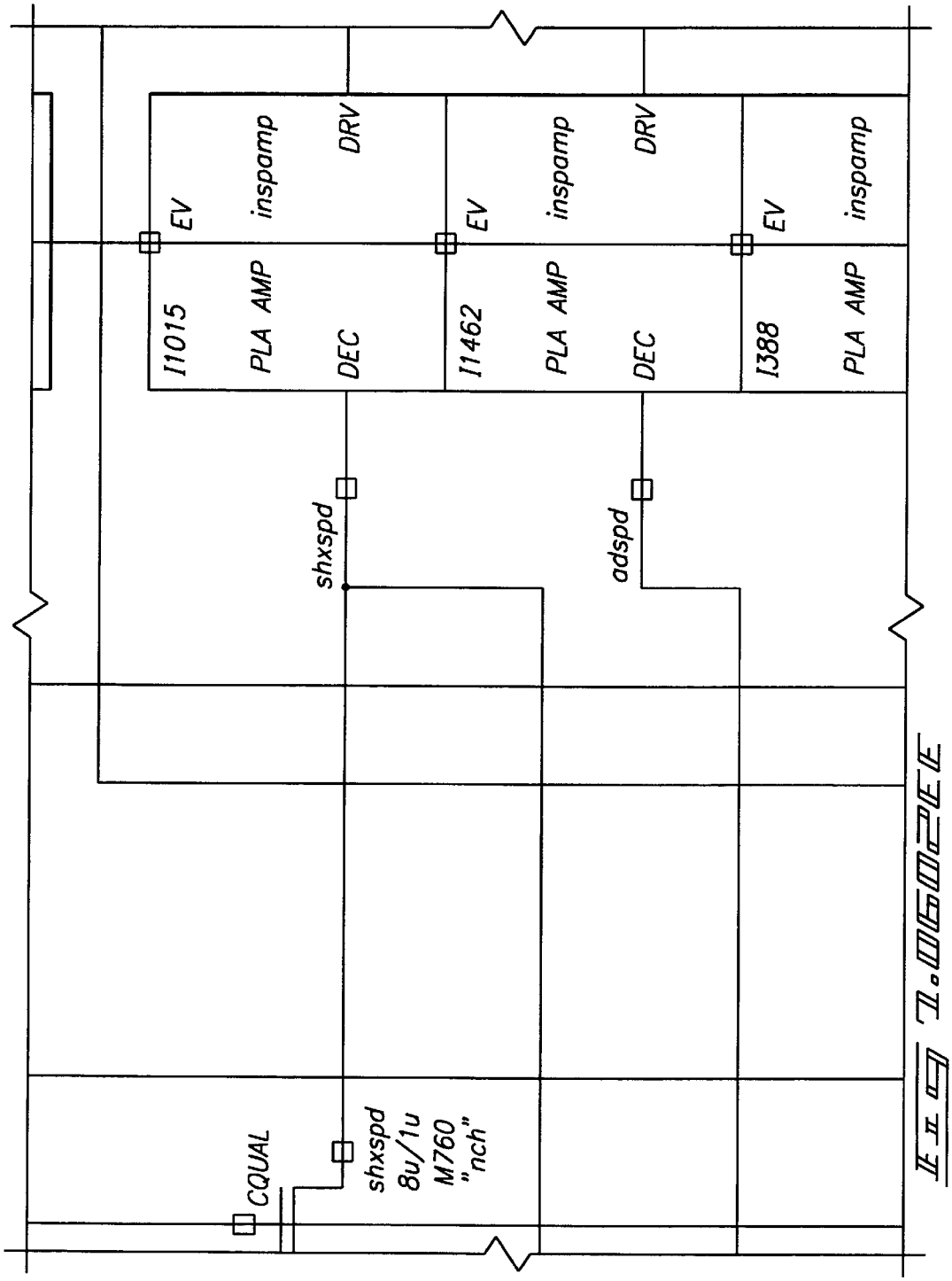

M1018
"nch"
net41385
ldr:1u
wdr=8u
"nch"
wdr=8u
net41385
8u/1u
M759
"nch"
S2
shxspd
8u/1u
M764
"nch"
net41376
ldr:1u
wdr=8u
net41400
ldr:1u
wdr=8u
adspd
8u/1u
M1461
"nch"
S3
S4
net41385
8u/1u
M762
"nch"
shxspd
8u/1u
M766
"nch"
net167137
ldr:1u
wdr=8u
net41394
ldr:1u
wdr=8u
net41382
ldr:1u
wdr=8u

Fig. 1,600,000


I1015
PLA AMP
DEC
EV
inspamp
DRV
I1462
PLA AMP
DEC
EV
inspamp
DRV
I388
PLA AMP
EV
inspamp
shxspd
adspd
CQUAL
shxspd
8u/1u
M760
"nch"

Фиг. 1.0500E

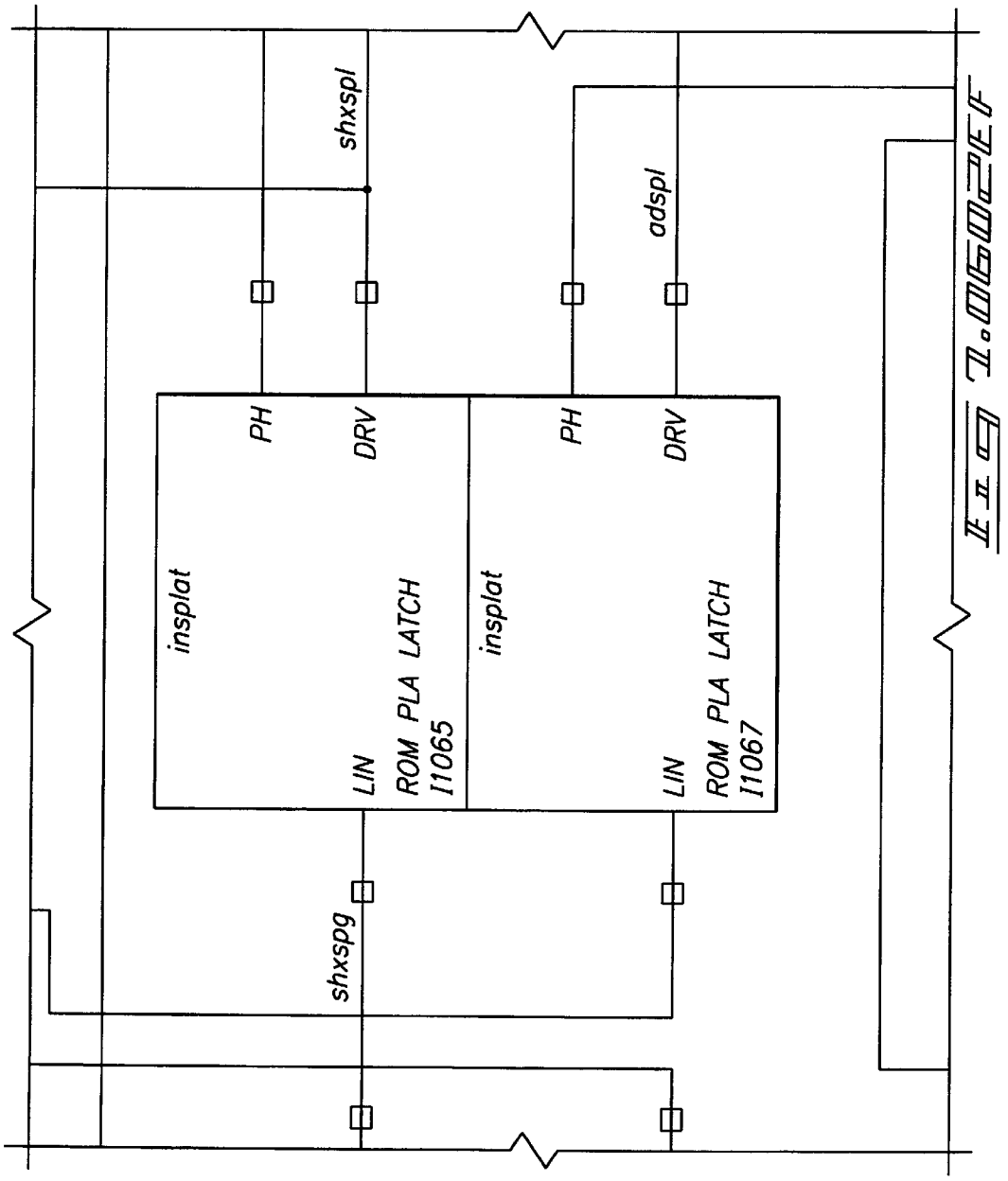

shxspl
adspl
PH
DRV
PH
DRV
insplat
ROM PLA LATCH
I1065
LIN
insplat
ROM PLA LATCH
I1067
LIN
shxspg

Fig 11.0502F

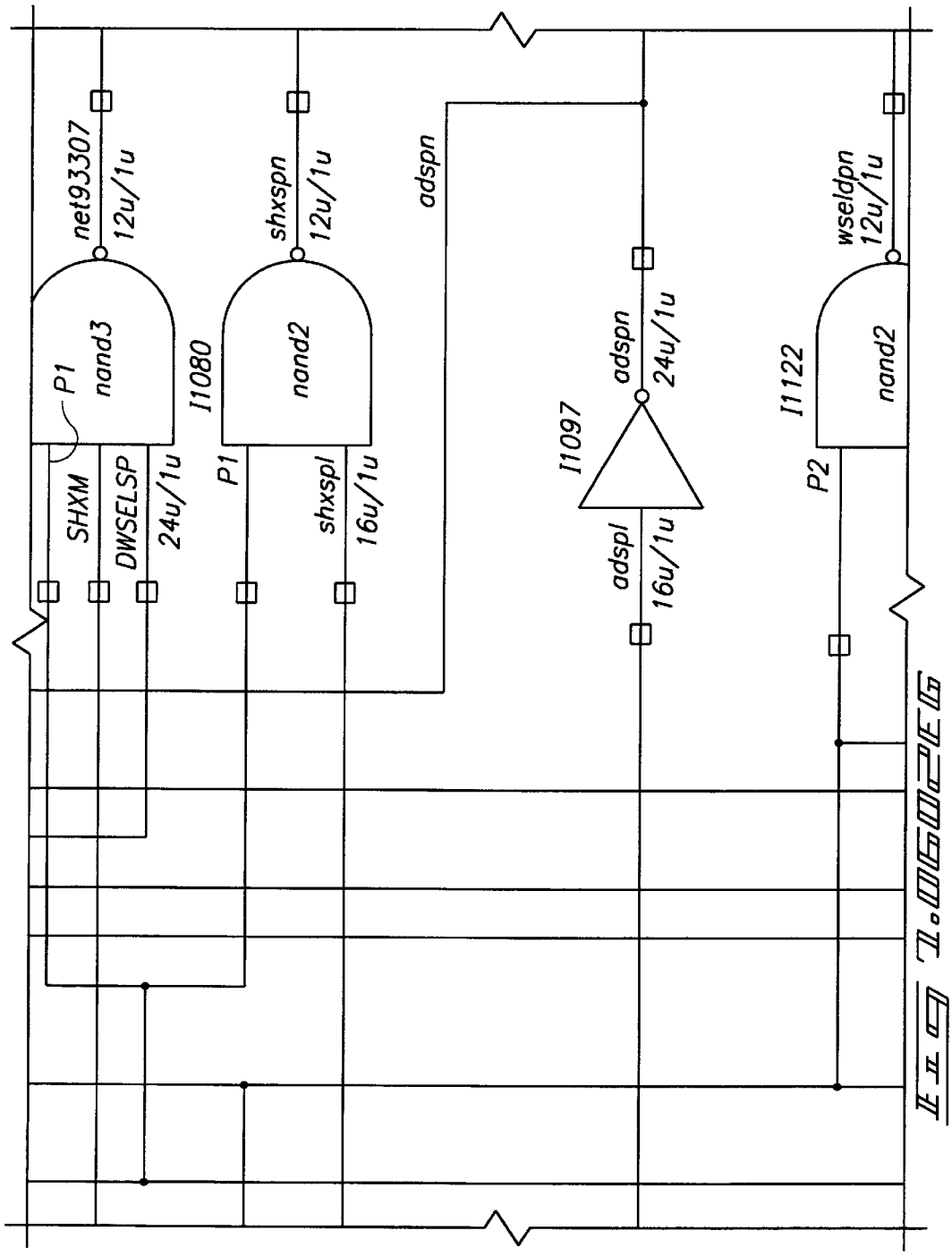

net93307
12u/1u
shxspn
12u/1u
adspn
wseldpn
12u/1u
P1
nand3
I1080
nand2
I1097
adspn
24u/1u
I1122
nand2
SHXM
DWSELSP
24u/1u
P1
shxspl
16u/1u
adspl
16u/1u
P2

FIG 59E

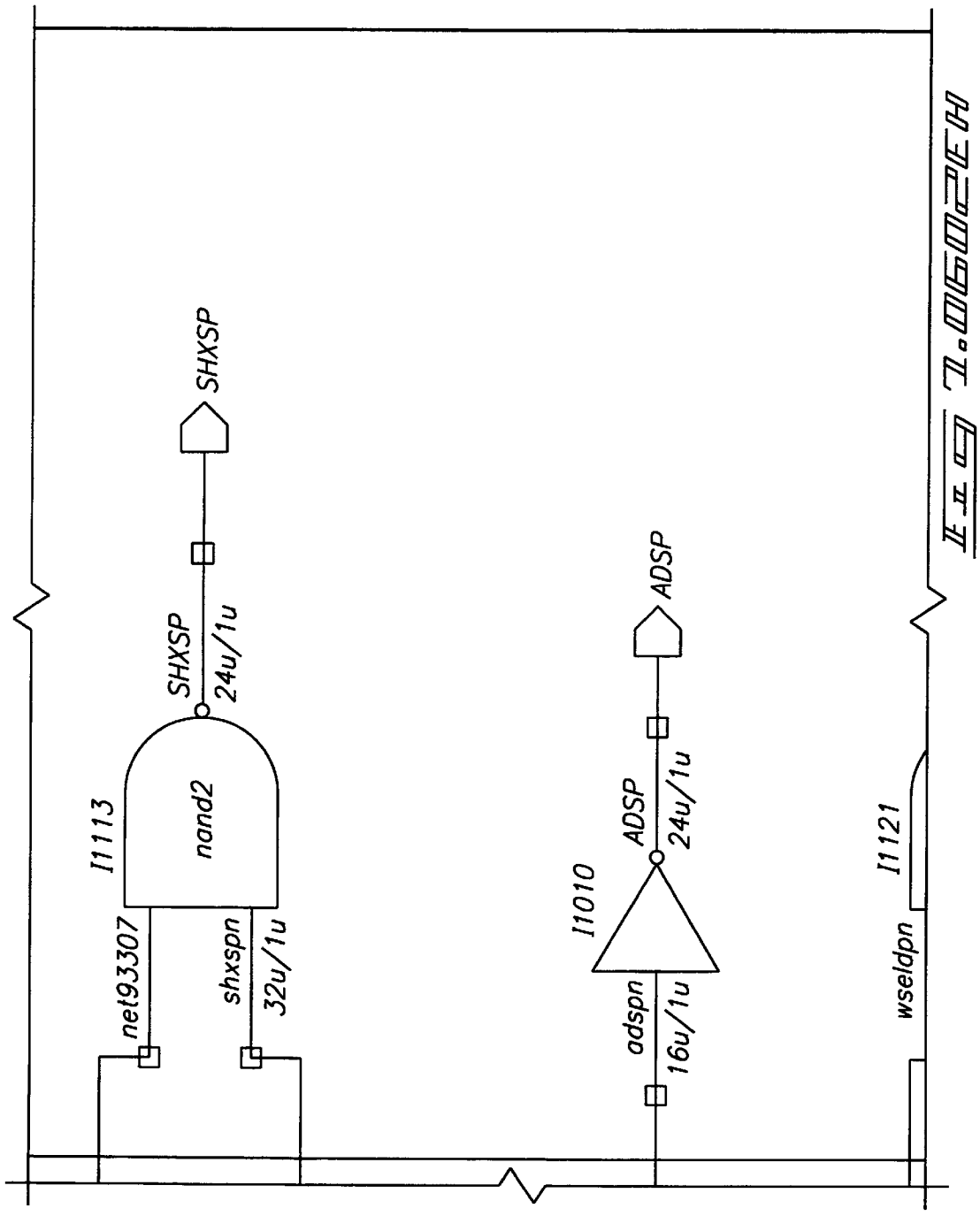


FIG. 603A
SHXSP
SHXSP
24u/1u
I1113
nand2
net93307
shxspn
32u/1u
ADSP
ADSP
24u/1u
I1010
adspn
16u/1u
I1121
wseldpn

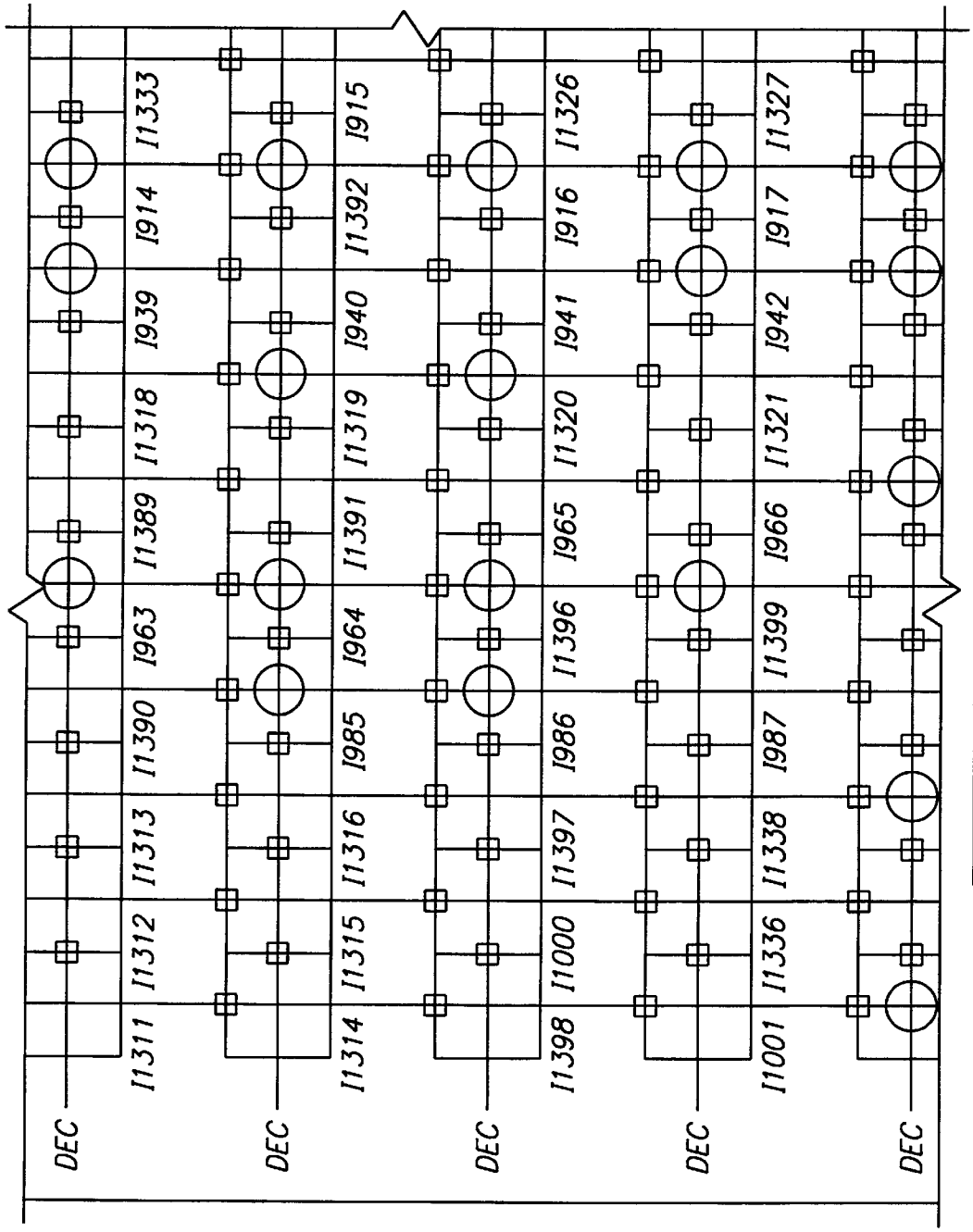

DEC
DEC
DEC
DEC
DEC
I1311
I1312
I1313
I1390
I963
I1389
I1318
I939
I914
I1333
I1314
I1315
I1316
I985
I964
I1391
I1319
I940
I1392
I915
I1398
I1000
I1397
I986
I1396
I965
I1320
I941
I916
I1326
I1001
I1336
I1338
I987
I1399
I966
I1321
I942
I917
I1327

FIG. 604

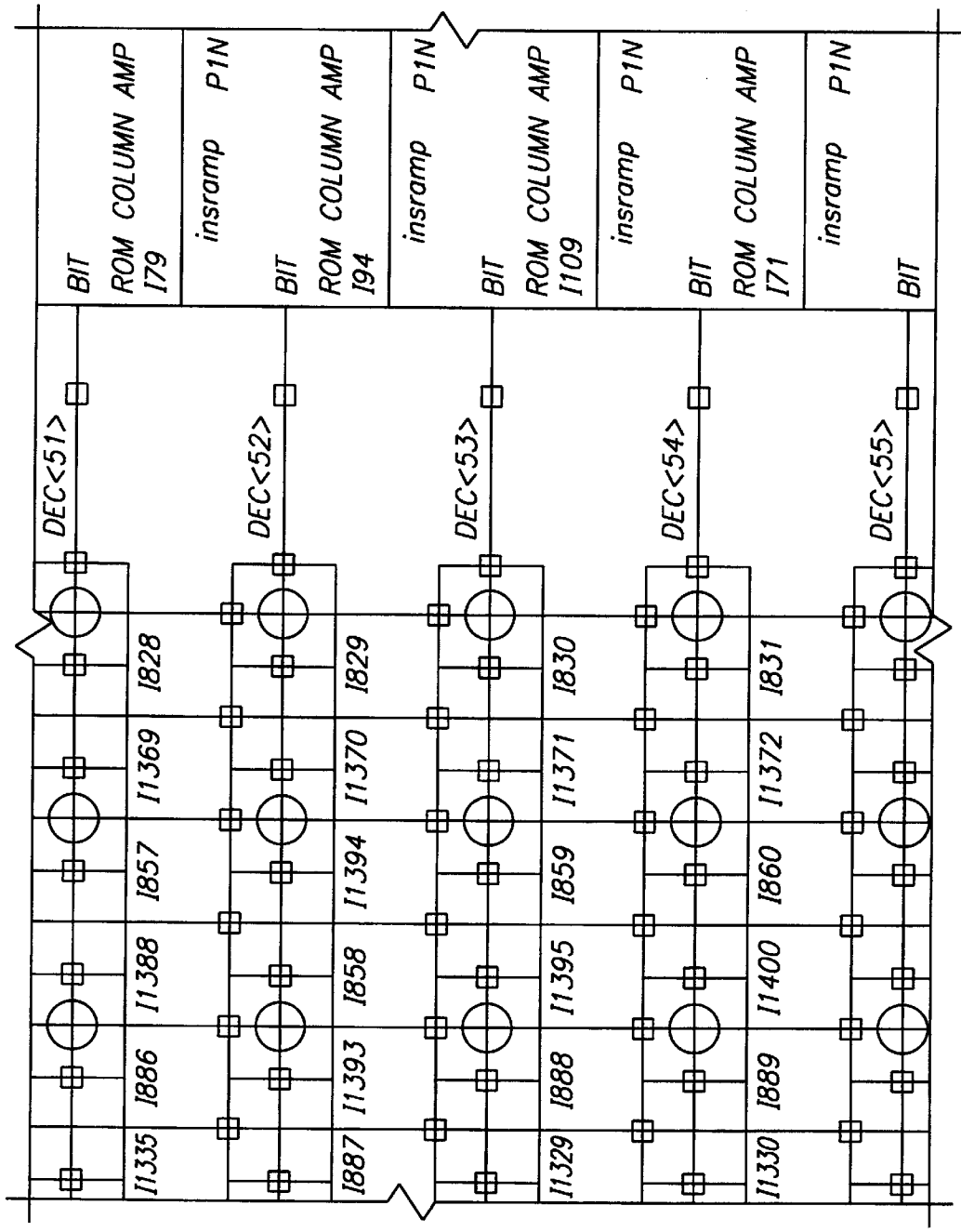


FIG 1.005DF1B

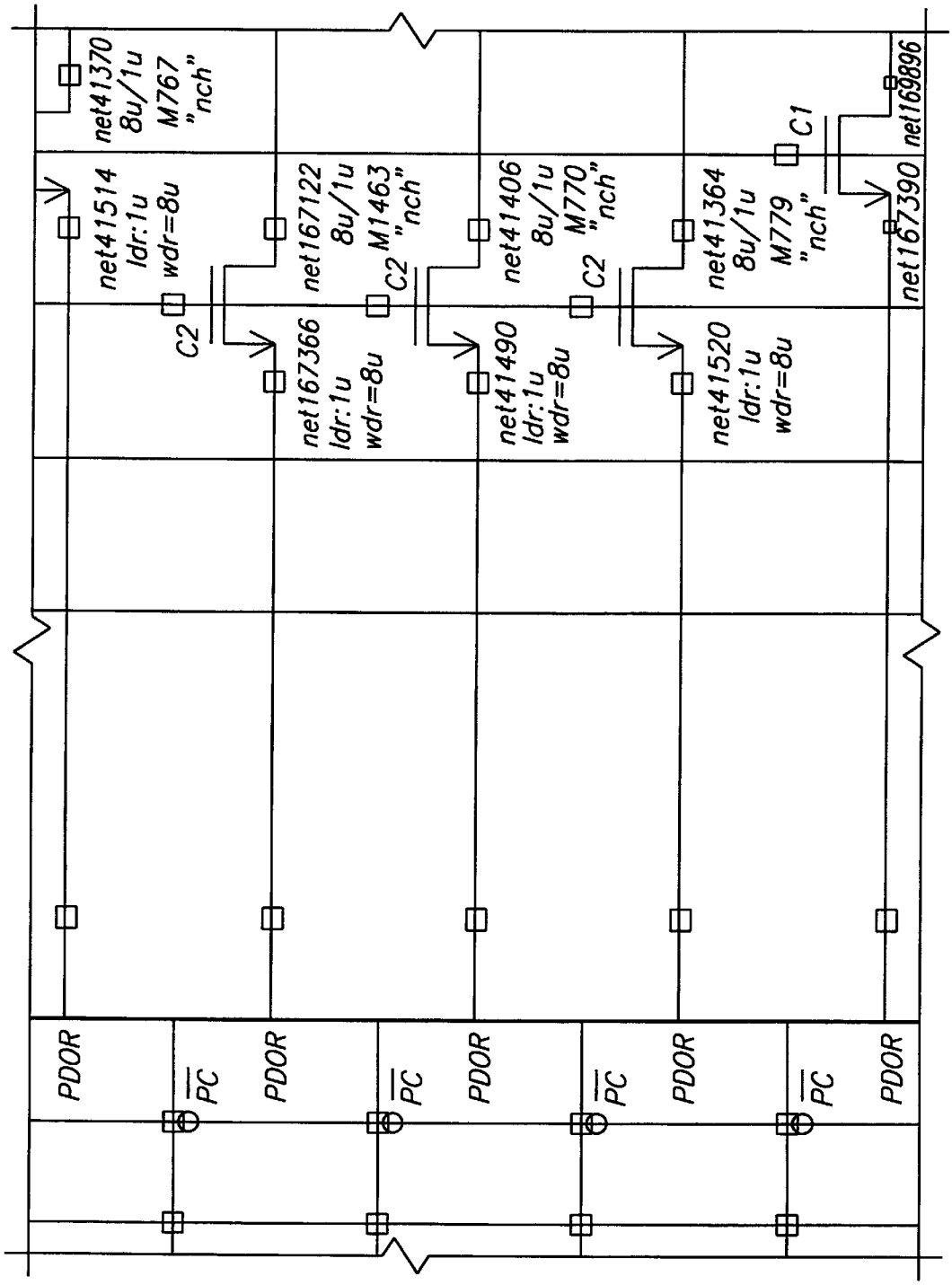

net41370
8u/1u
M767
"nch"
net41514
ldr:1u
wdr=8u
C2
net167122
8u/1u
M1463
"nch"
C2
net41406
8u/1u
M770
"nch"
C2
net41364
8u/1u
M779
"nch"
C1
net169896
net167390
net167366
ldr:1u
wdr=8u
net41490
ldr:1u
wdr=8u
net41520
ldr:1u
wdr=8u
PDOR
PC
PDOR
PC
PDOR
PC
PDOR
PC
PDOR

FIG. 6,130,602

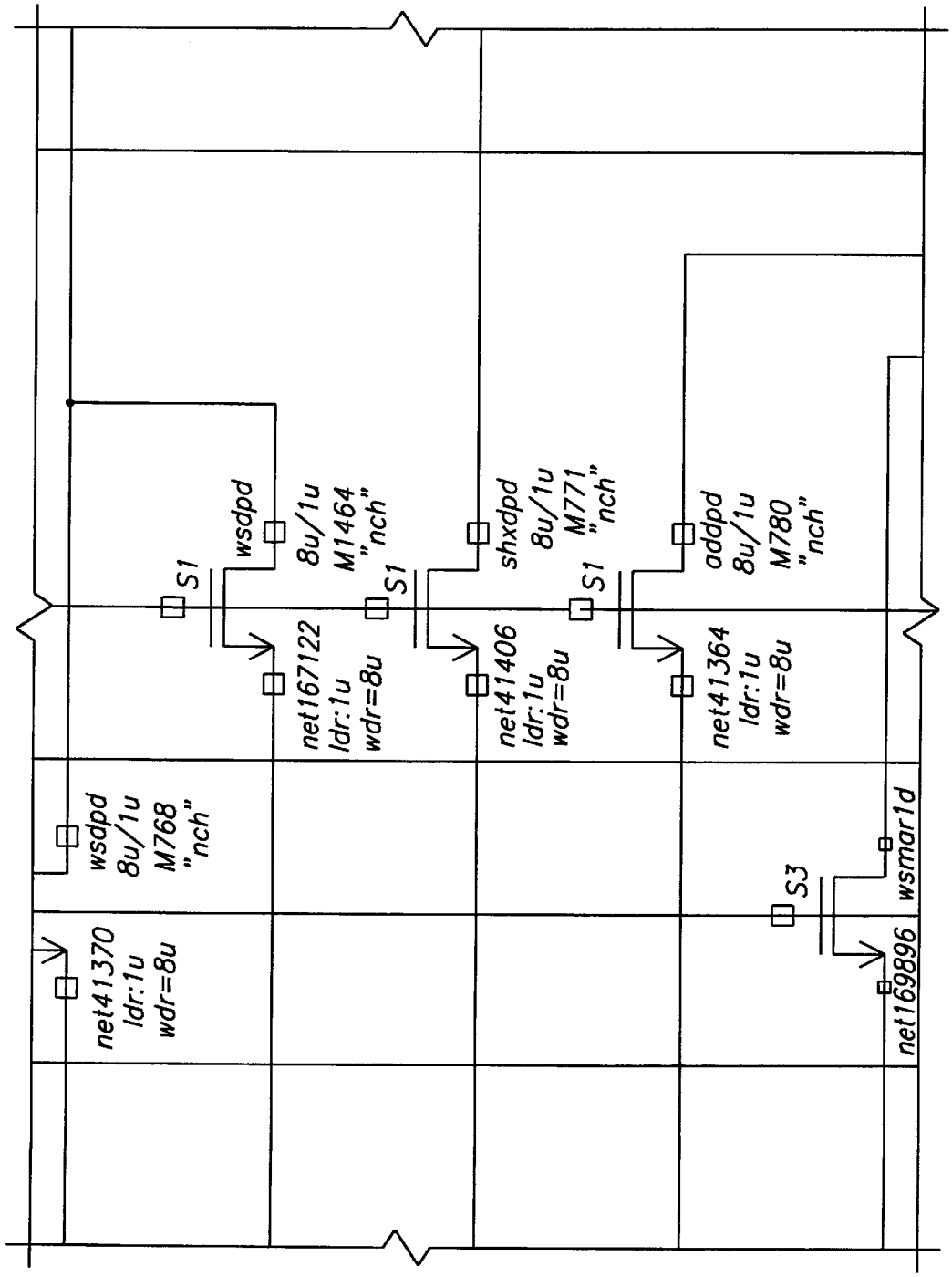

wsdpd
8u/1u
M1464
"nch"
S1
net167122
ldr:1u
wdr=8u
shxdpd
8u/1u
M771
"nch"
net41406
ldr:1u
wdr=8u
addpd
8u/1u
M780
"nch"
net41364
ldr:1u
wdr=8u
wsdpd
8u/1u
M768
"nch"
net41370
ldr:1u
wdr=8u
S3
wsmar1d
net169896

FIG. 6,130,602

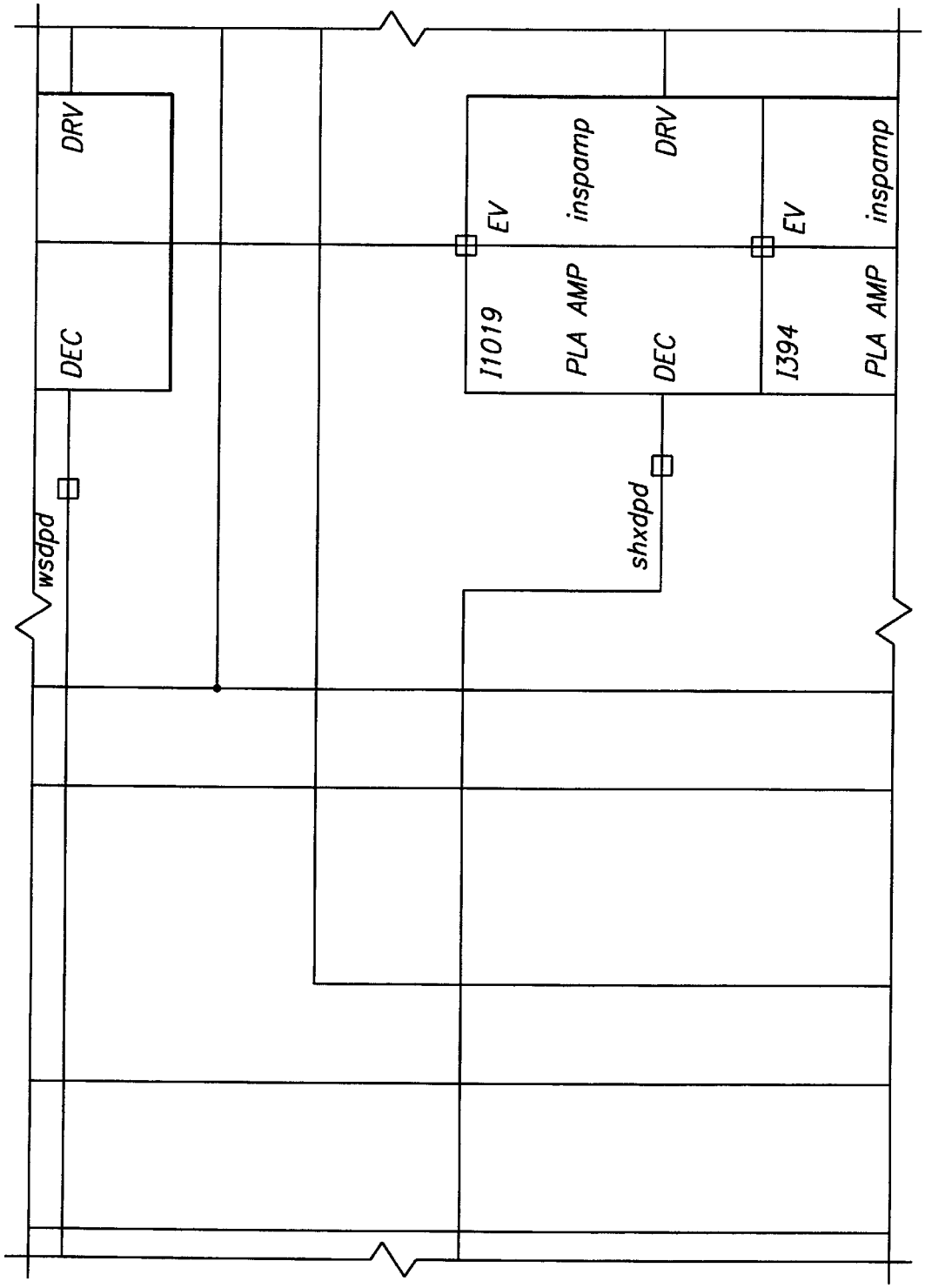

DRV
DEC
wsdpd
EV
inspamp
DRV
I1019
PLA AMP
DEC
shxdpd
EV
inspamp
I394
PLA AMP

FIG. 1.0600E

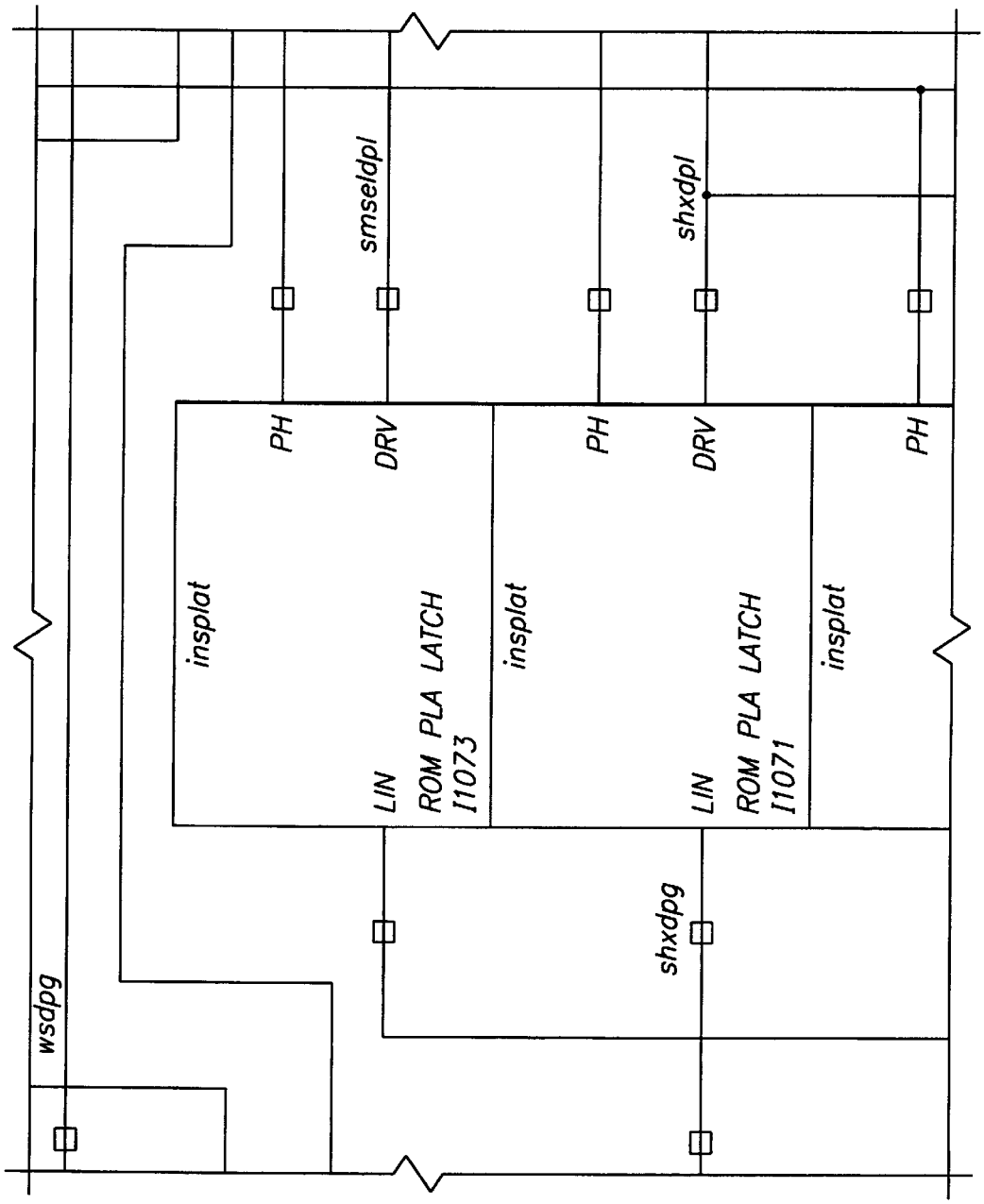


FIG 11,605,602F

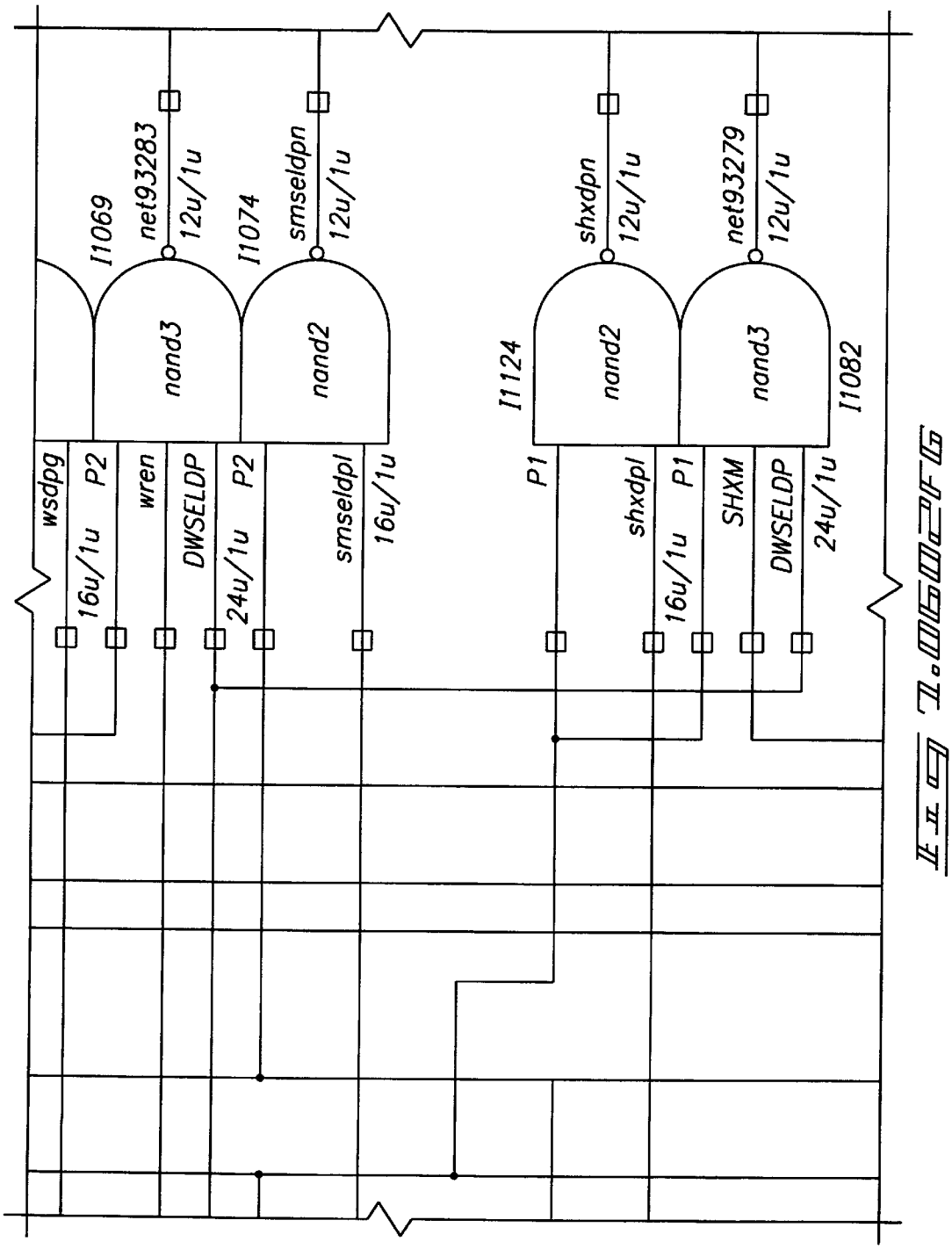

I1069
net93283
12u/1u
I1074
smseldpn
12u/1u
shxdpn
12u/1u
net93279
12u/1u
nand3
nand2
I1124
nand2
nand3
I1082
wsdpg
16u/1u
P2
wren
DWSELDP
24u/1u
P2
smseldpl
16u/1u
P1
shxdpl
16u/1u
P1
SHXM
DWSELDP
24u/1u

FIG. 1,005,872

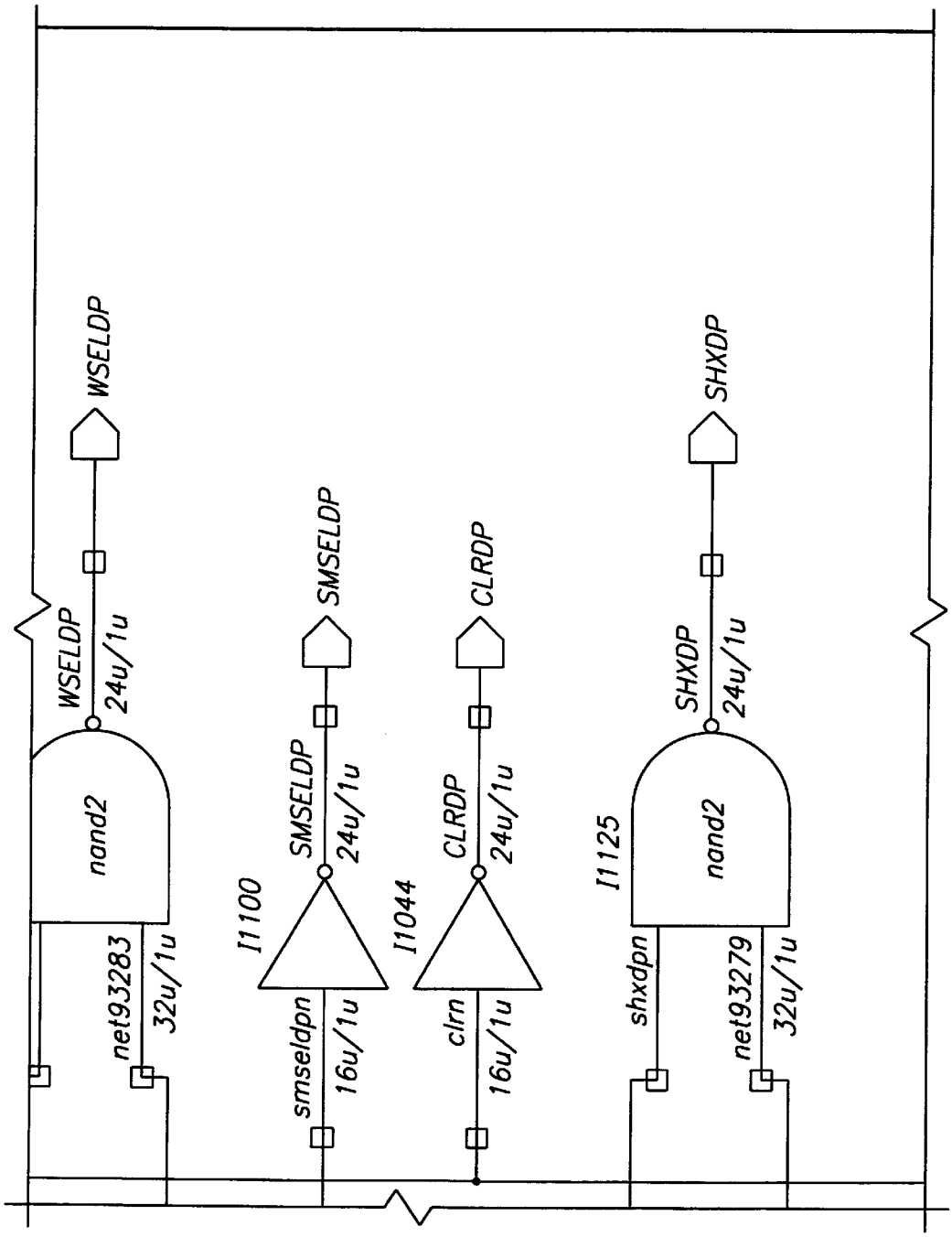

WSELDP
WSELDP
24u/1u
nand2
net93283
32u/1u
SMSELDP
SMSELDP
24u/1u
I1100
smseldpn
16u/1u
CLRDP
CLRDP
24u/1u
I1044
clrn
16u/1u
SHXDP
SHXDP
24u/1u
I1125
nand2
shxdpn
net93279
32u/1u

FIG 1.0500.FM

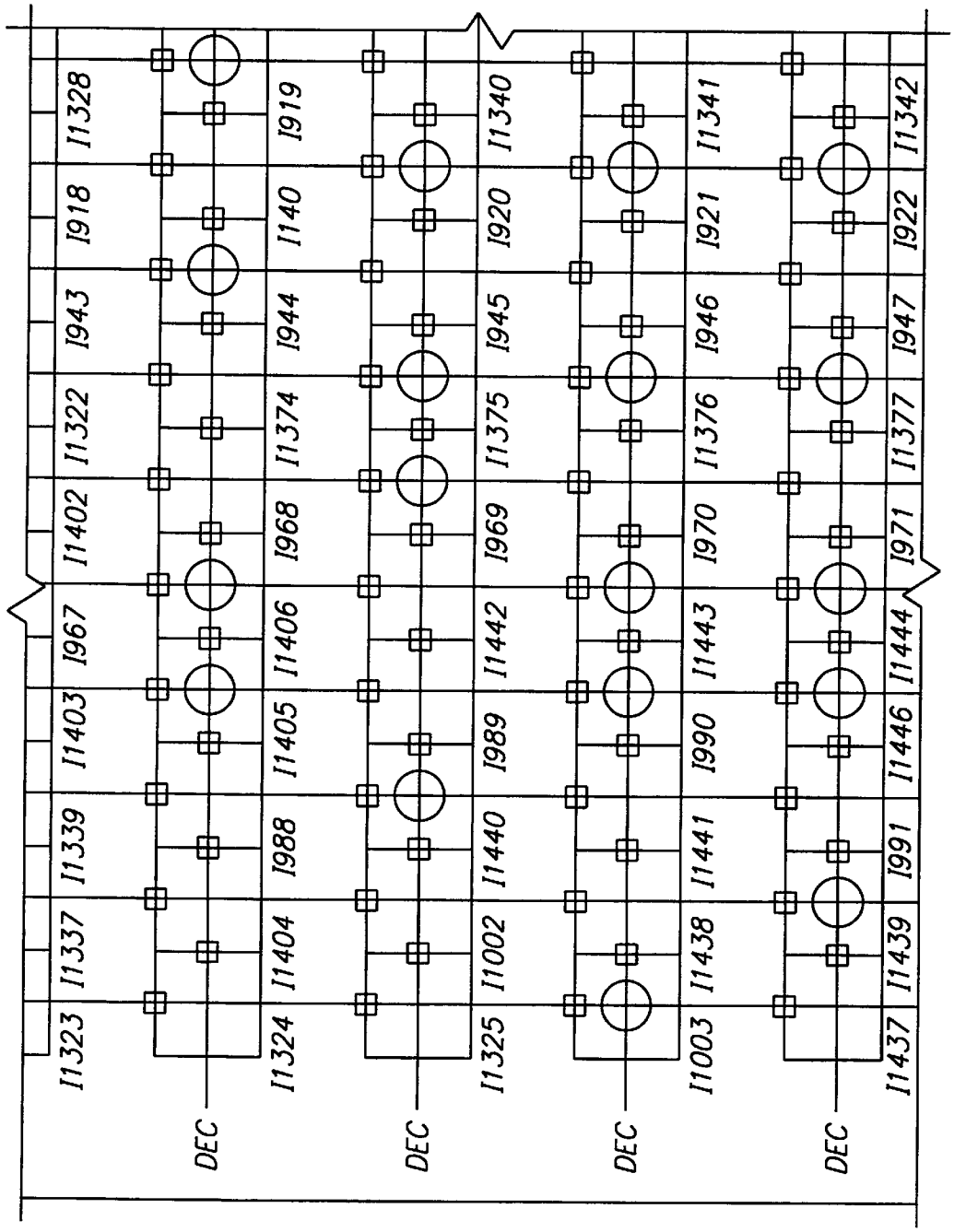


FIG. 1130602A

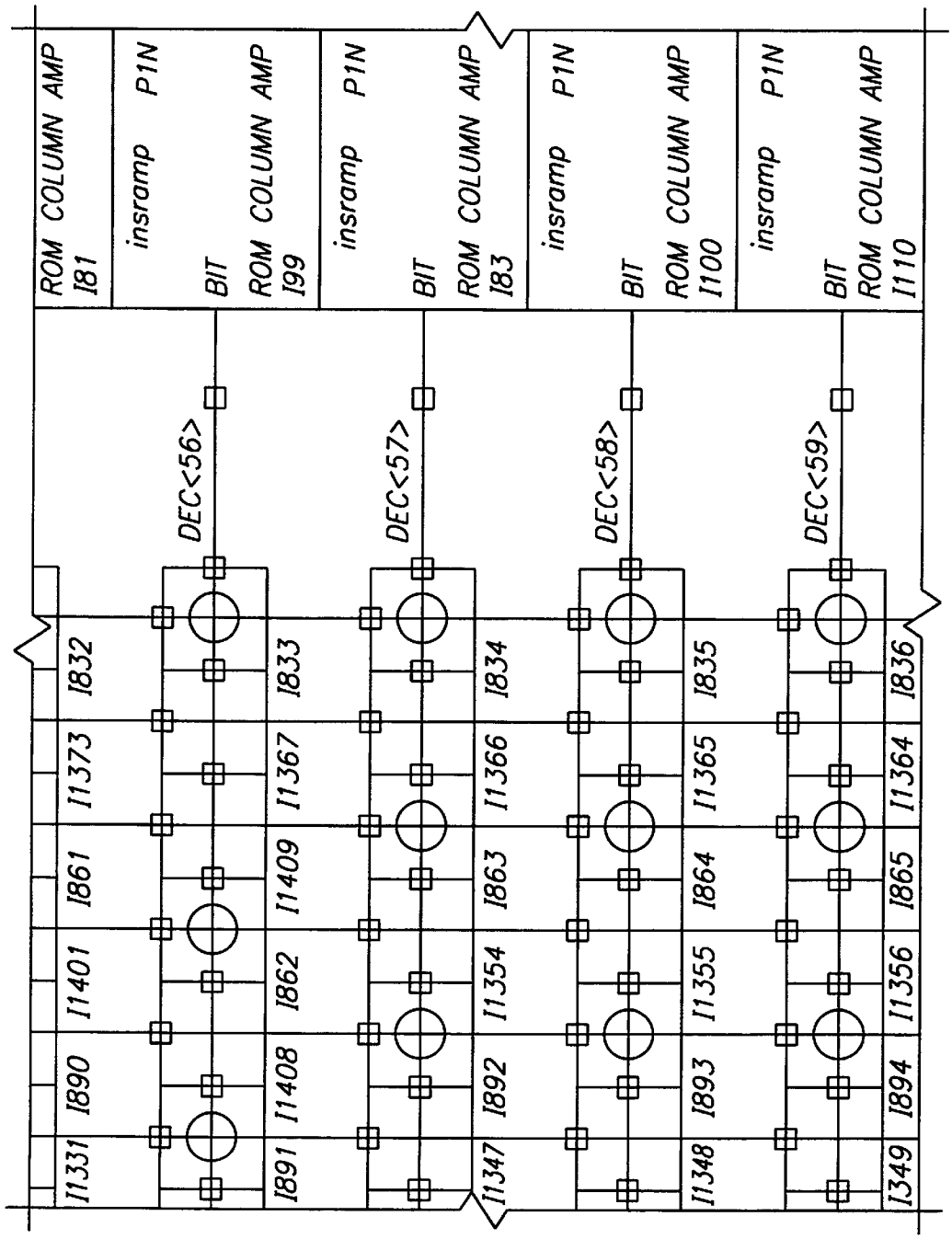

ROM COLUMN AMP
I81
insramp P1N
BIT
ROM COLUMN AMP
I99
insramp P1N
BIT
ROM COLUMN AMP
I83
insramp P1N
BIT
ROM COLUMN AMP
I100
insramp P1N
BIT
ROM COLUMN AMP
I110
DEC<56>
DEC<57>
DEC<58>
DEC<59>
I1331
I890
I1401
I861
I1373
I832
I891
I1408
I862
I1409
I1367
I833
I1347
I892
I1354
I863
I1366
I834
I1348
I893
I1355
I864
I1365
I835
I1349
I894
I1356
I865
I1364
I836

FIG. 1,060,268

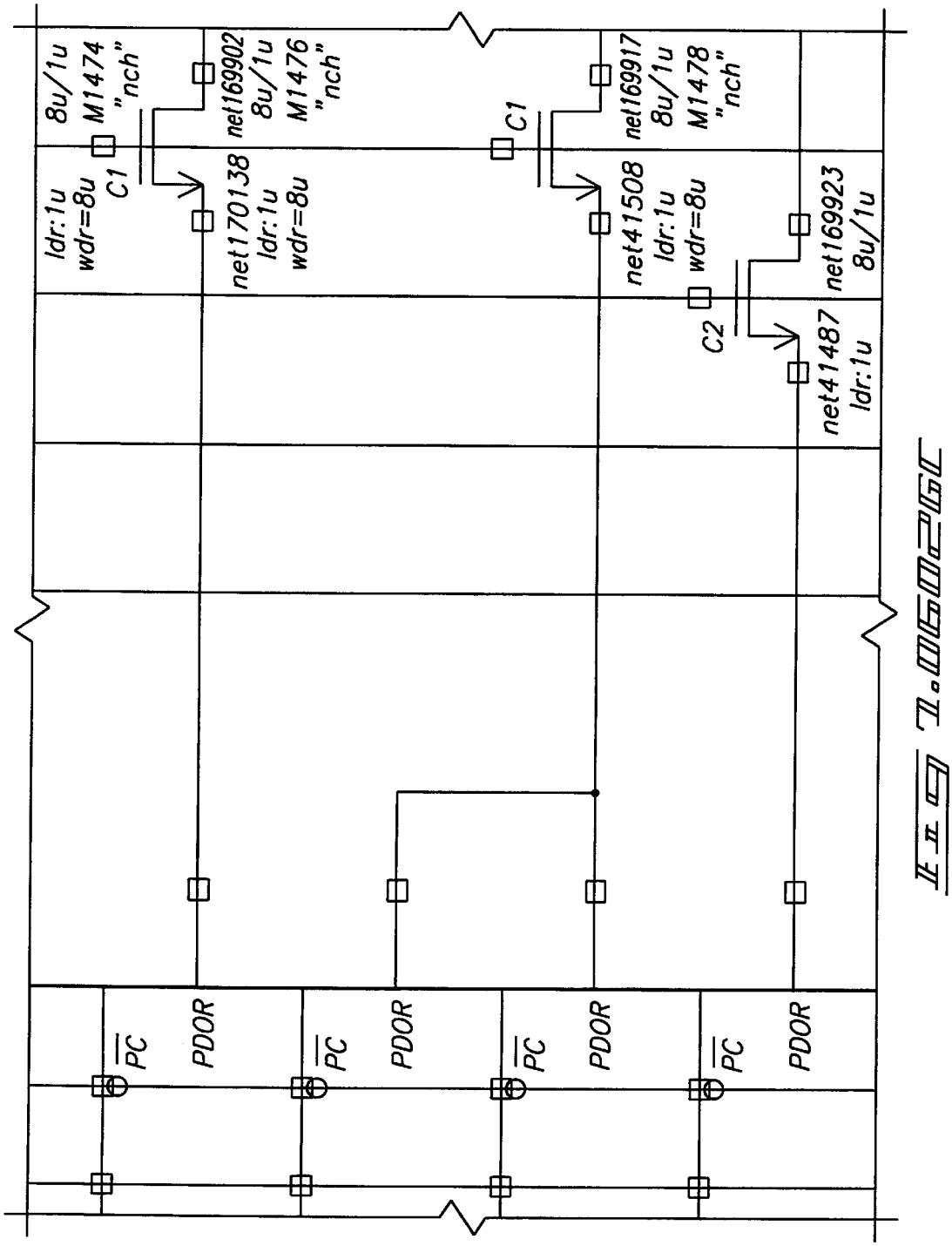

8u/1u
M1474
"nch"
net169902
8u/1u
M1476
"nch"
C1
net169917
8u/1u
M1478
"nch"
ldr:1u
wdr=8u
C1
net170138
ldr:1u
wdr=8u
net41508
ldr:1u
wdr=8u
C2
net169923
8u/1u
net41487
ldr:1u
PC
PDOR
PC
PDOR
PC
PDOR
PC
PDOR

FIG. 6,130,602

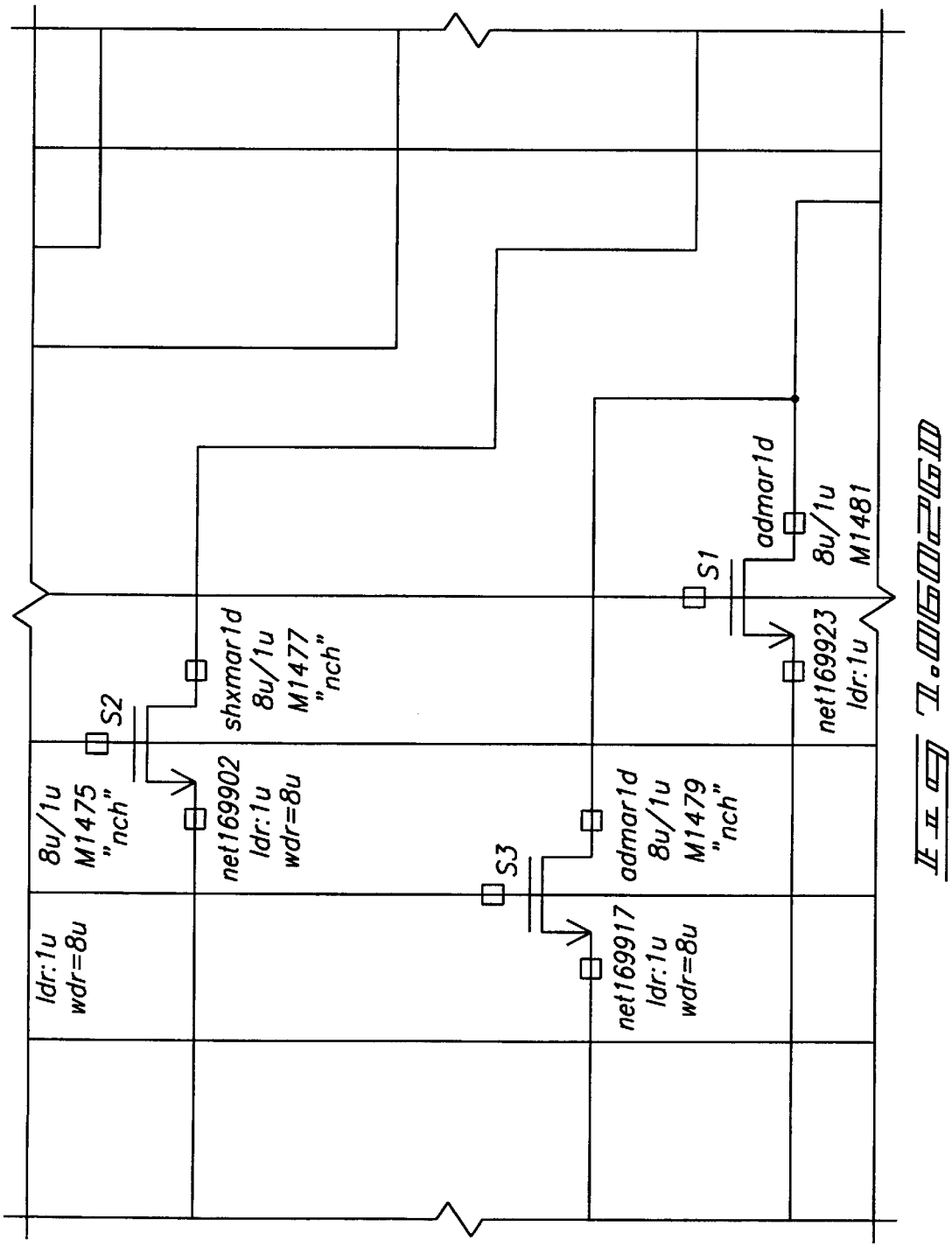

admar1d
8u/1u
M1481
S1
net169923
ldr:1u
shxmar1d
8u/1u
M1477
"nch"
S2
8u/1u
M1475
"nch"
net169902
ldr:1u
wdr=8u
admar1d
8u/1u
M1479
"nch"
S3
net169917
ldr:1u
wdr=8u
ldr:1u
wdr=8u

Fig. 1,605,210

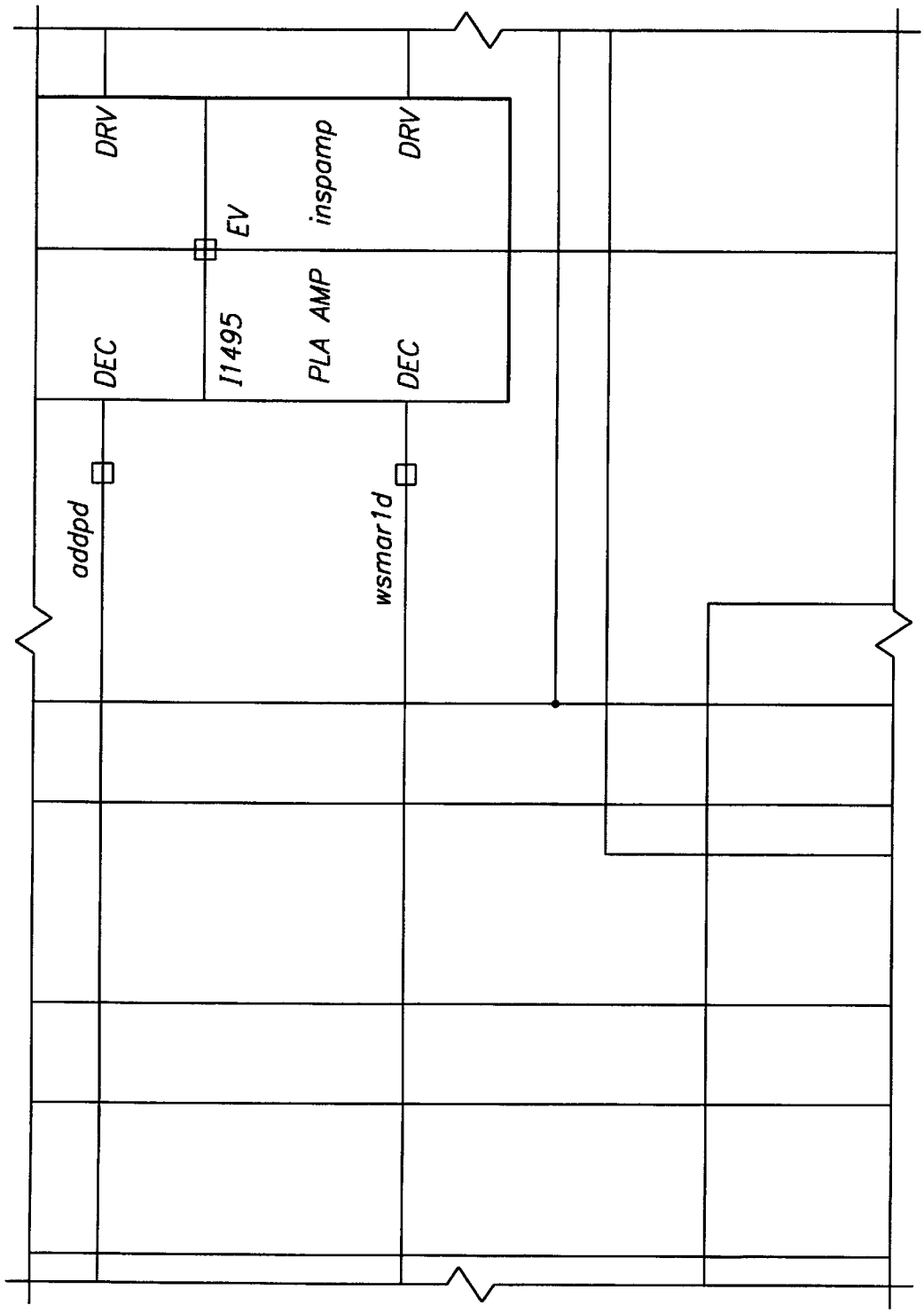


FIG 7L 3902056

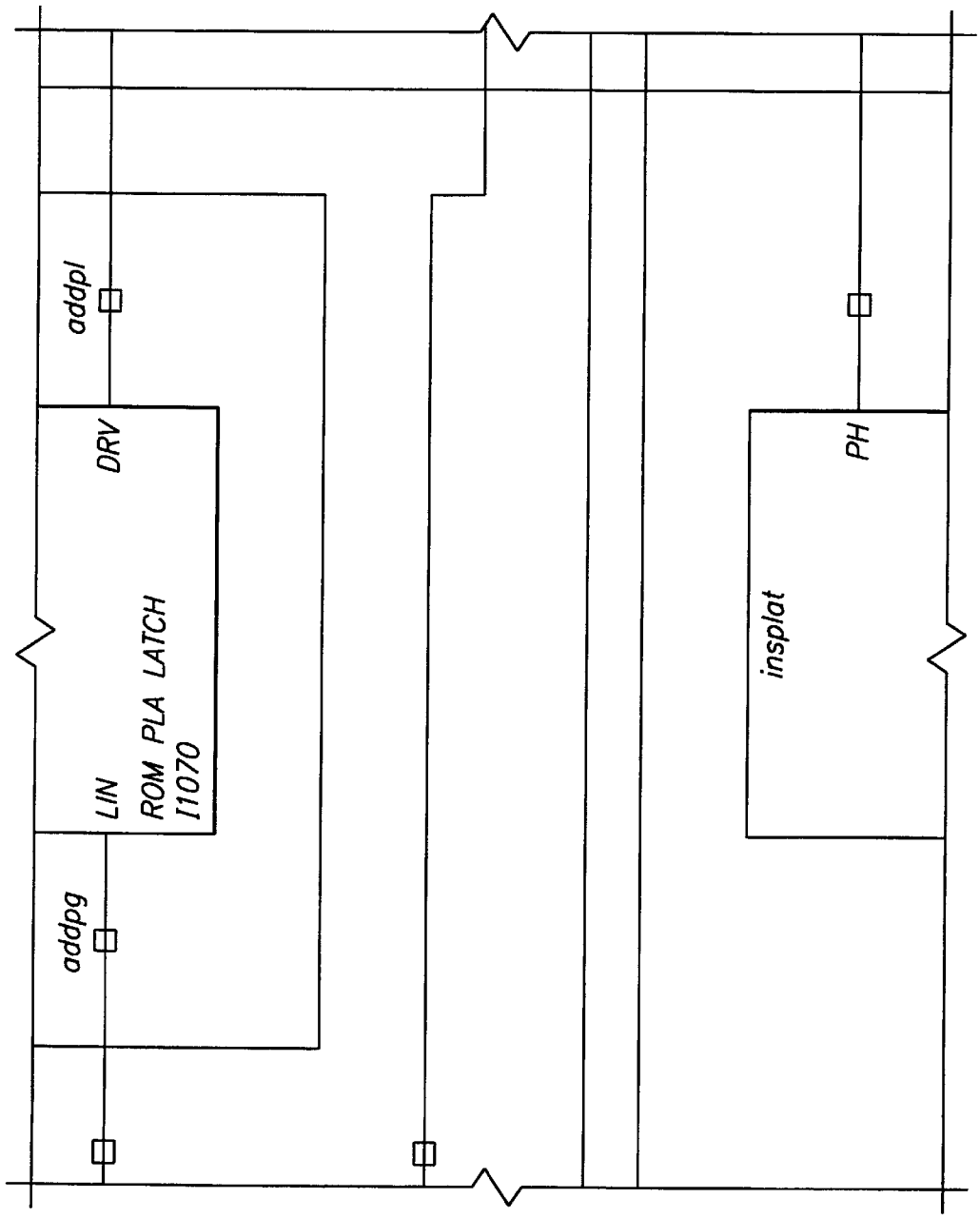


Fig 11.006296F

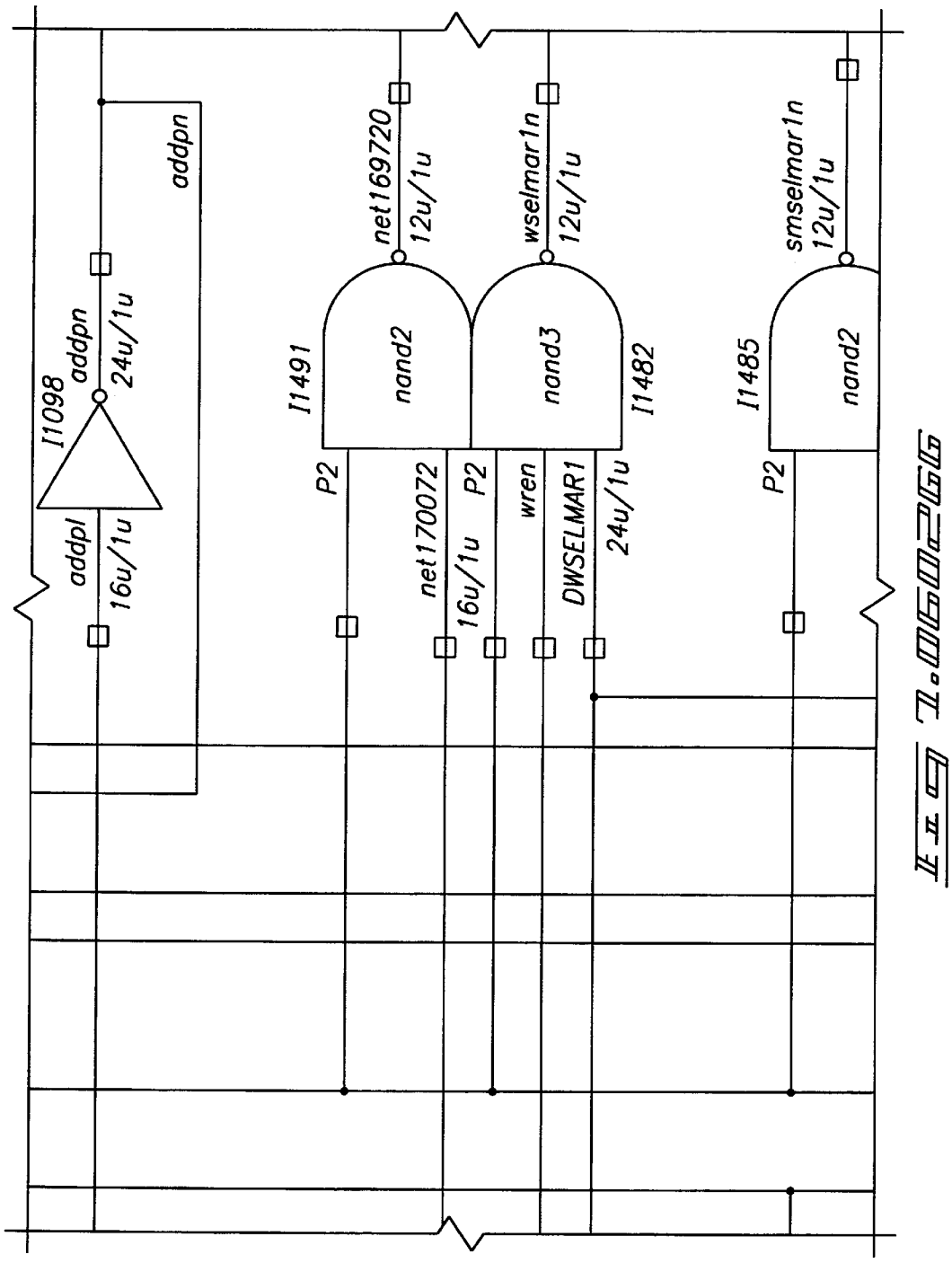

addpn
I1098
addpn
24u/1u
addpl
16u/1u
net169720
12u/1u
wselmar1n
12u/1u
smselmar1n
12u/1u
I1491
nand2
nand3
I1482
I1485
nand2
P2
net170072
16u/1u
P2
wren
DWSELMAR1
24u/1u
P2

FIG 7.005,205

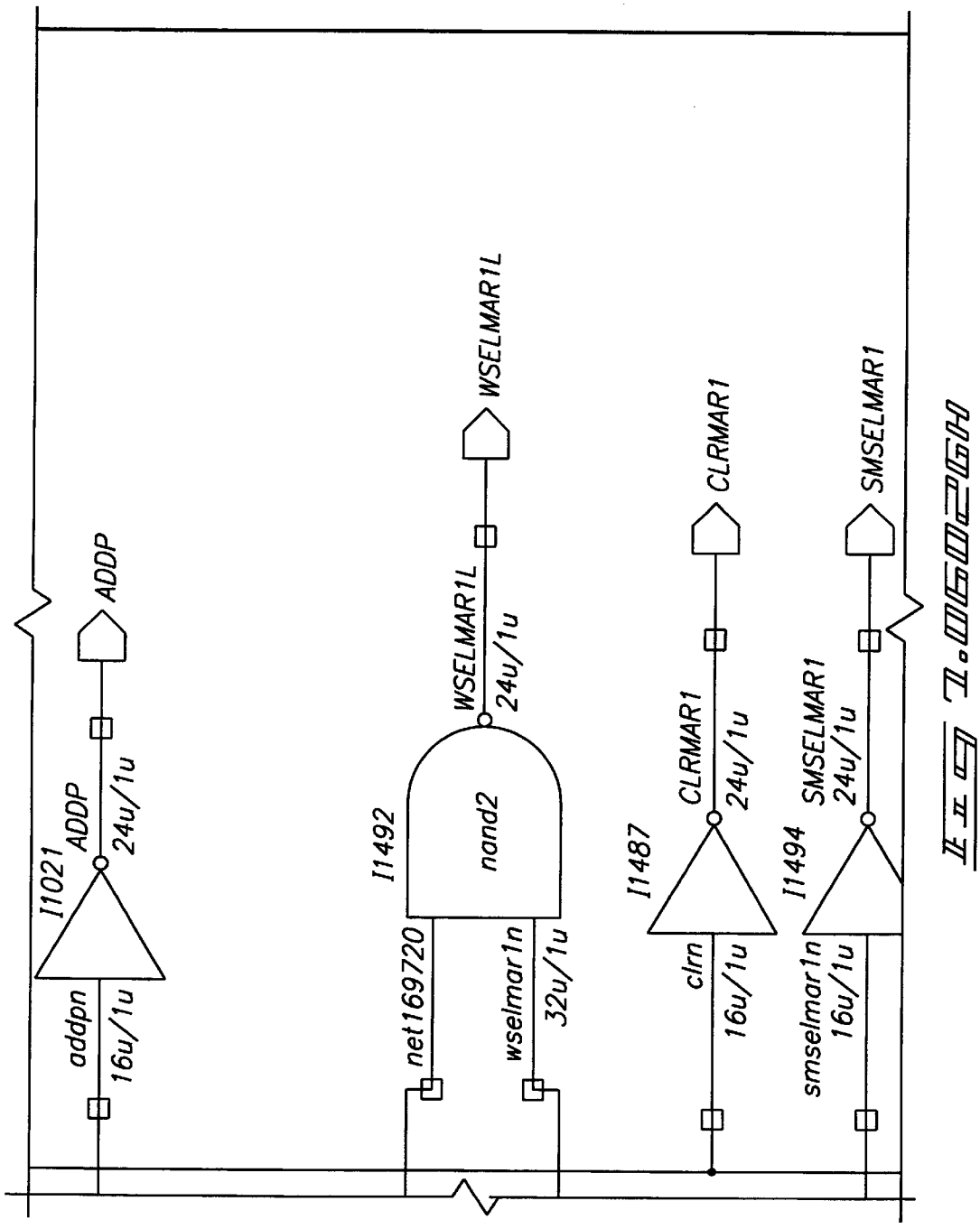

I1021
ADDP
24u/1u
addpn
16u/1u
I1492
nand2
WSELMAR1L
24u/1u
net169720
wselmar1n
32u/1u
I1487
CLRMAR1
24u/1u
clrn
16u/1u
I1494
SMSELMAR1
24u/1u
smselmar1n
16u/1u

FIG. 1.0602H

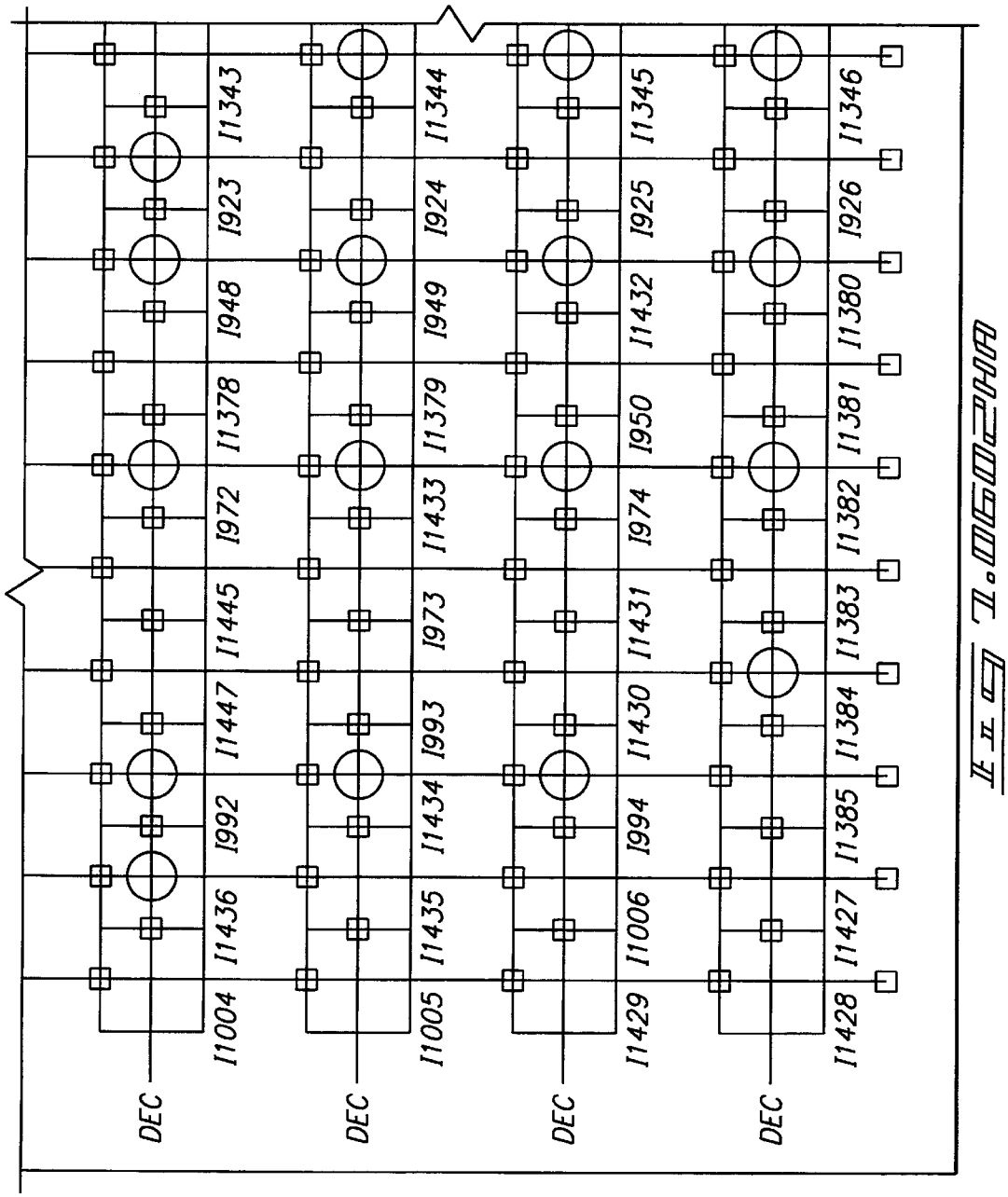

DEC
DEC
DEC
DEC
I1004
I1436
I992
I1447
I1445
I972
I1378
I948
I923
I1343
I1005
I1435
I1434
I993
I973
I1433
I1379
I949
I924
I1344
I1429
I1006
I994
I1430
I1431
I974
I950
I1432
I925
I1345
I1428
I1427
I1385
I1384
I1383
I1382
I1381
I1380
I926
I1346

FIG. 1L

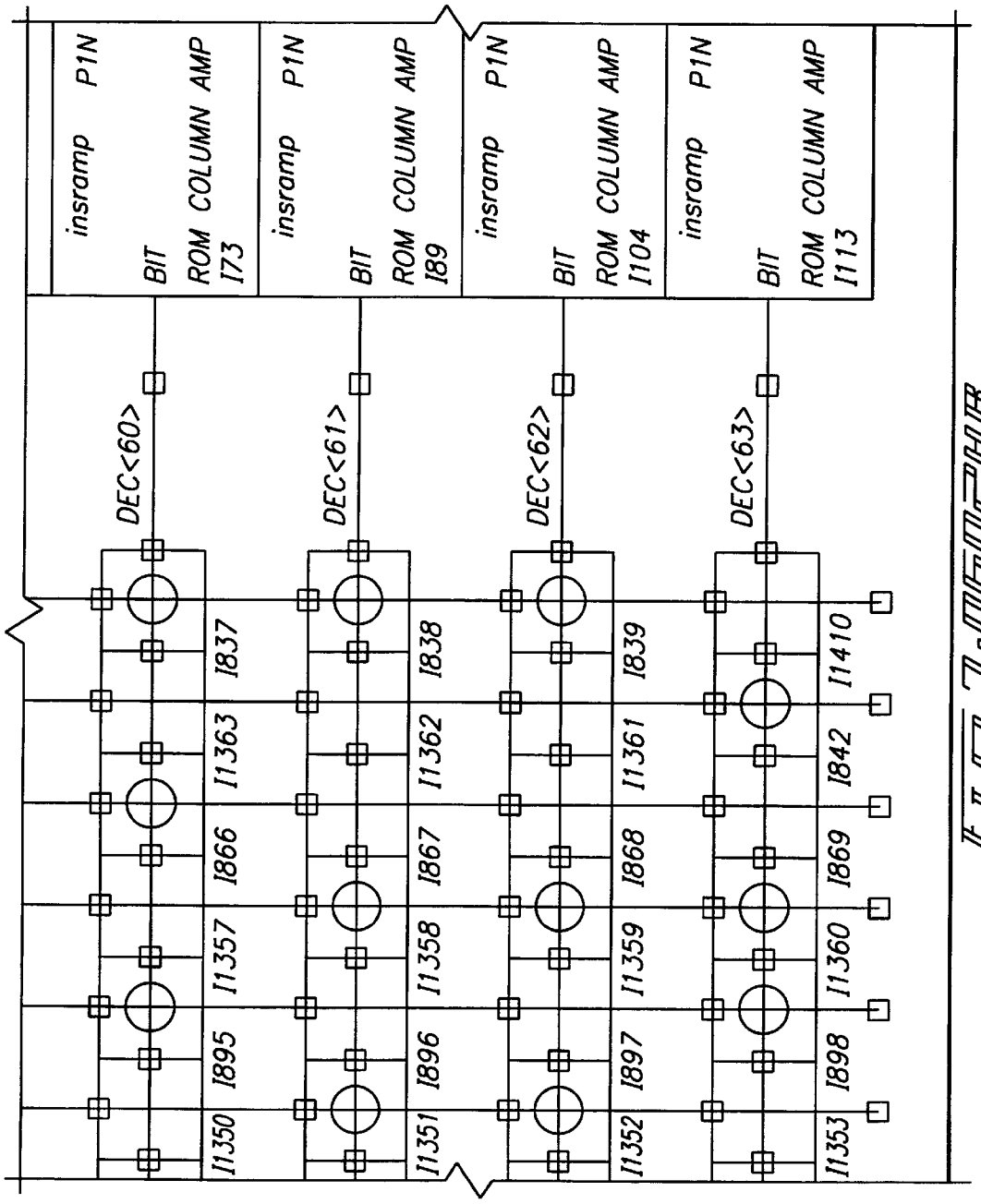
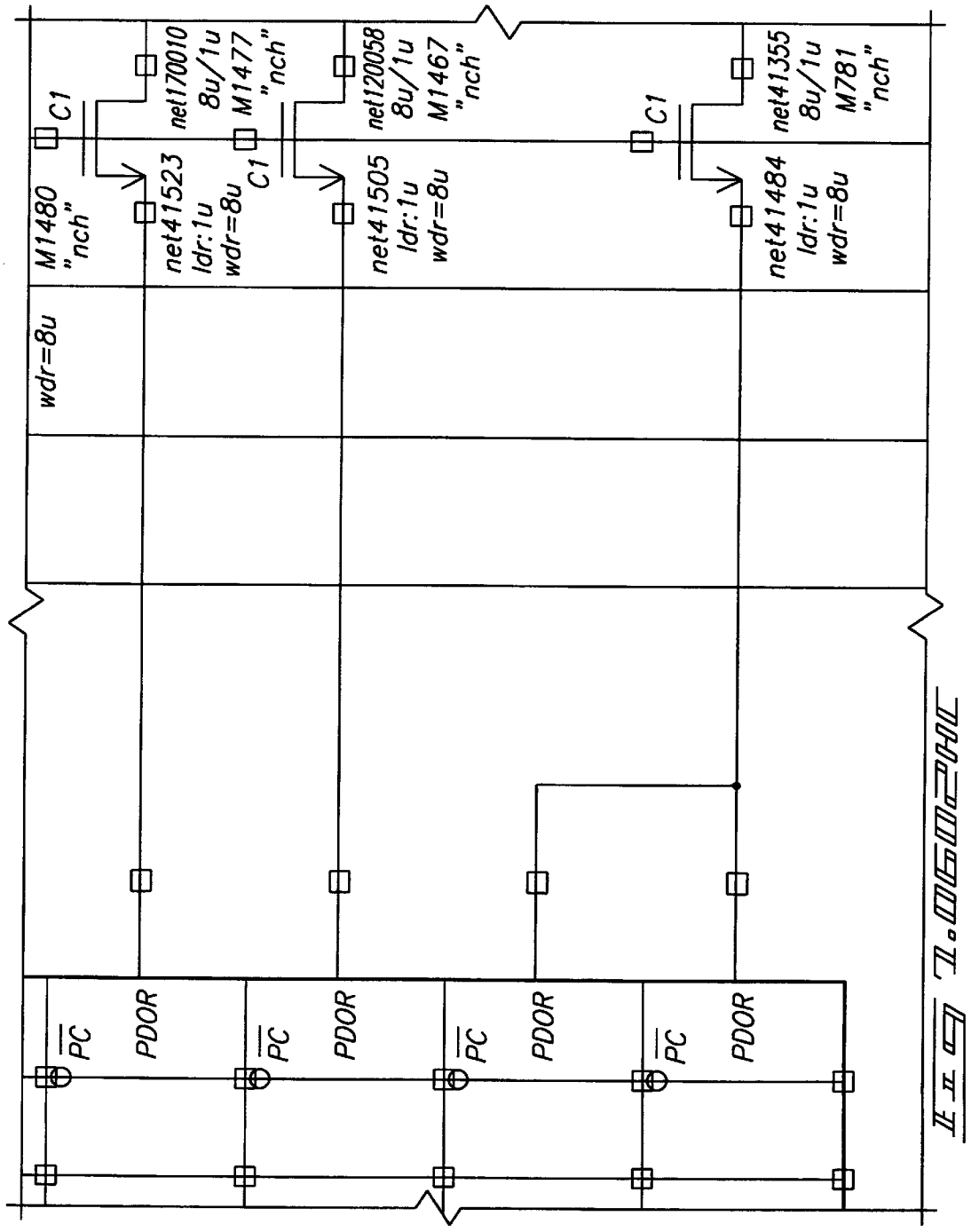
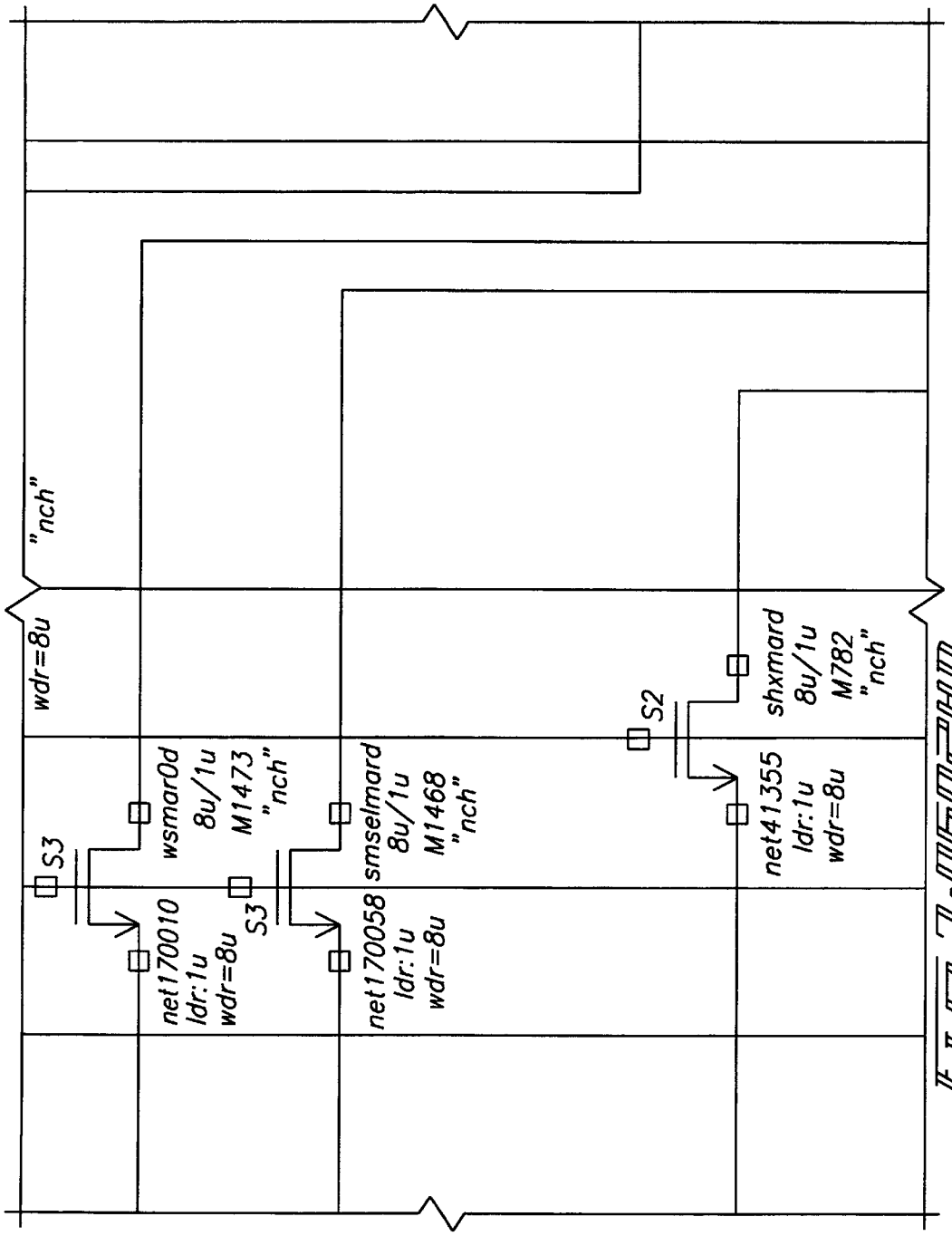


FIG 11.00602HB


C1
net170010
8u/1u
M1477
"nch"
net120058
8u/1u
M1467
"nch"
C1
net41355
8u/1u
M781
"nch"
M1480
"nch"
net41523
ldr:1u
wdr=8u
C1
net41505
ldr:1u
wdr=8u
net41484
ldr:1u
wdr=8u
wdr=8u
PC
PDOR
PC
PDOR
PC
PDOR
PC
PDOR

Фиг. 6.005.0L


"nch"
wdr=8u
S3
wsmar0d
8u/1u
M1473
"nch"
net170010
ldr:1u
wdr=8u
S3
smselmard
8u/1u
M1468
"nch"
net170058
ldr:1u
wdr=8u
S2
shxmard
8u/1u
M782
"nch"
net41355
ldr:1u
wdr=8u

Фиг. 6,130,602

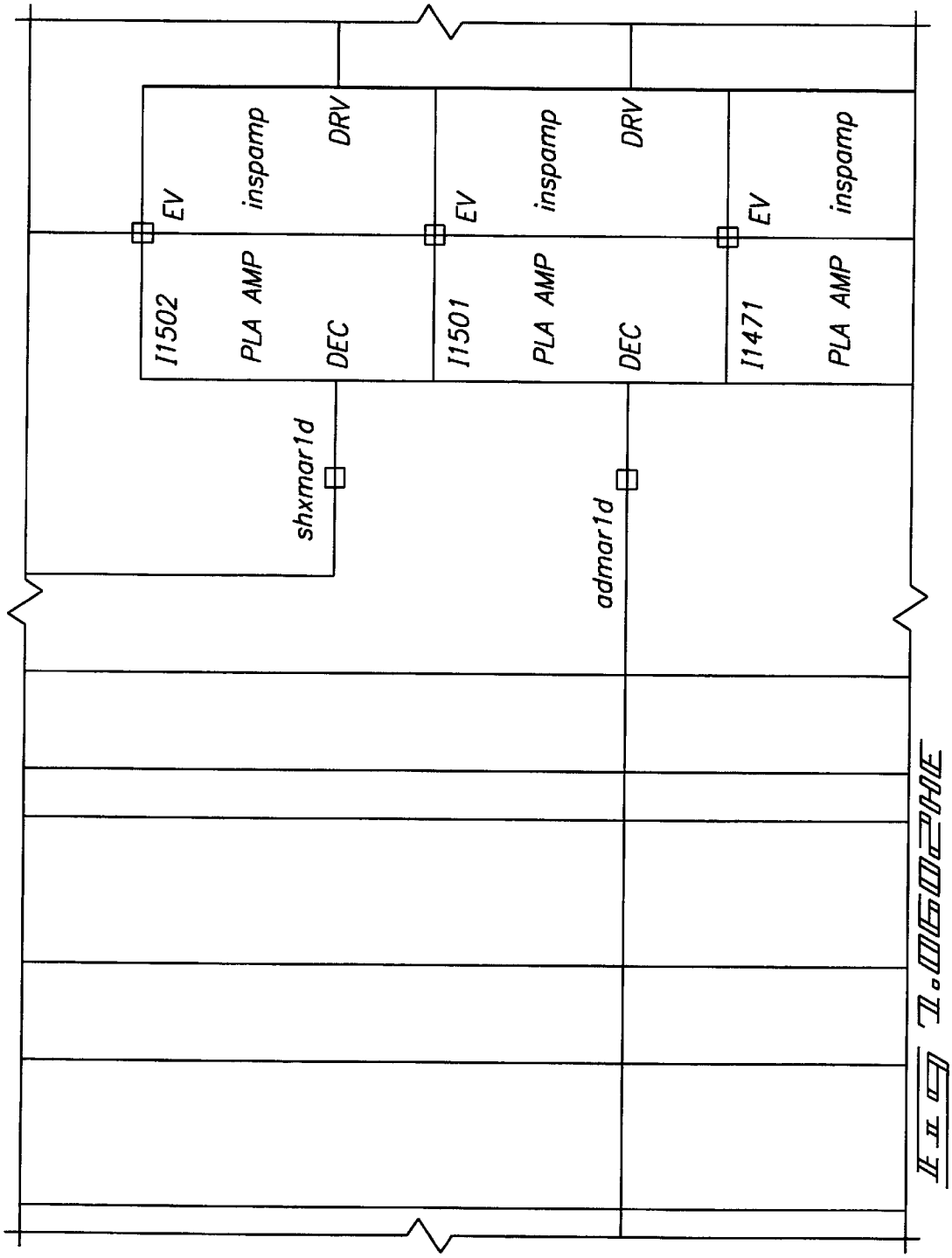
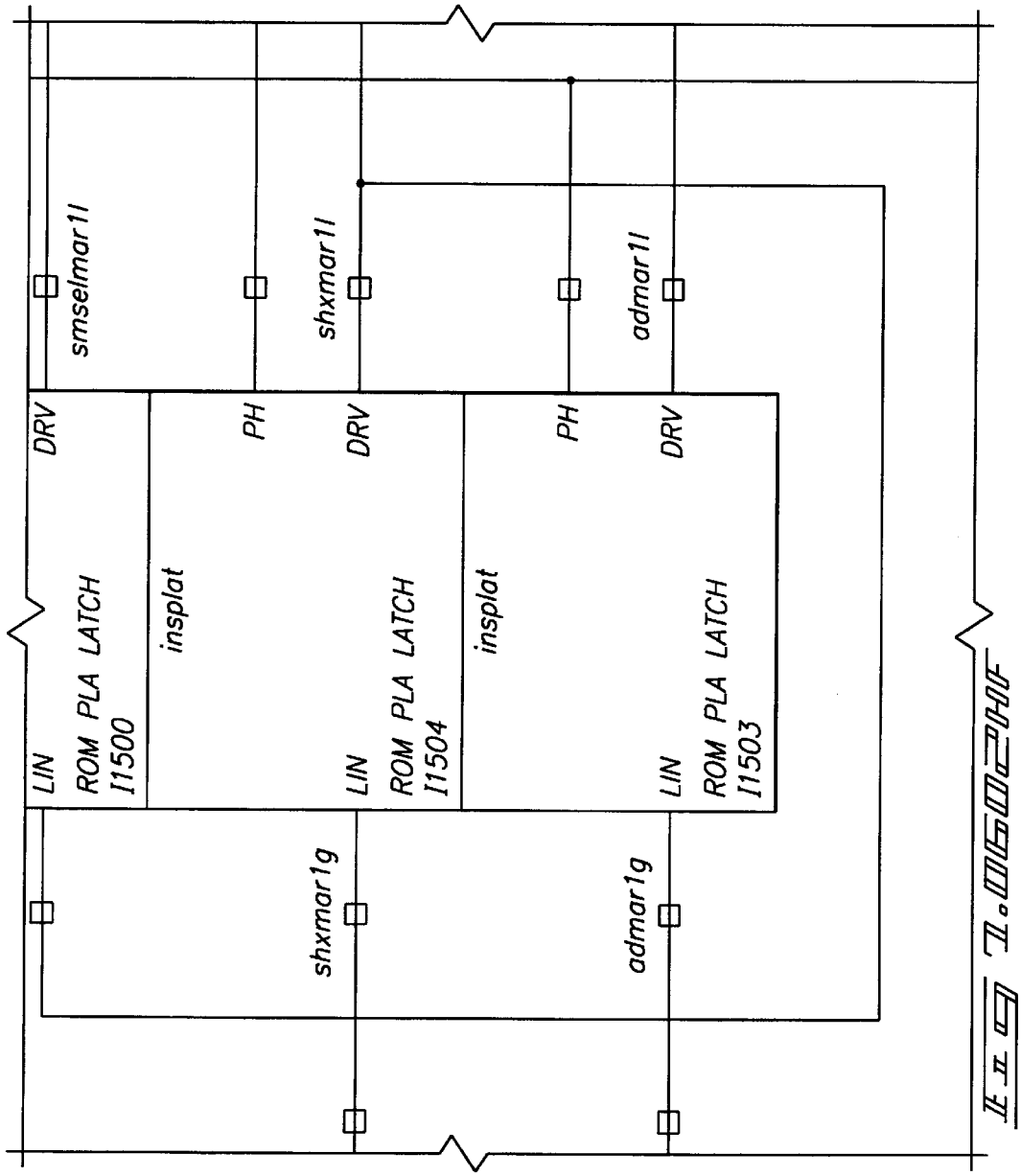

I1502
PLA AMP
DEC
I1501
PLA AMP
DEC
I1471
PLA AMP
EV
inspamp
DRV
shxmar1d
admar1d

FIG. 1.0600E


smselmar11
shxmar11
admar11
DRV
PH
DRV
PH
DRV
LIN
ROM PLA LATCH
I1500
insplat
LIN
ROM PLA LATCH
I1504
insplat
LIN
ROM PLA LATCH
I1503
shxmar1g
admar1g

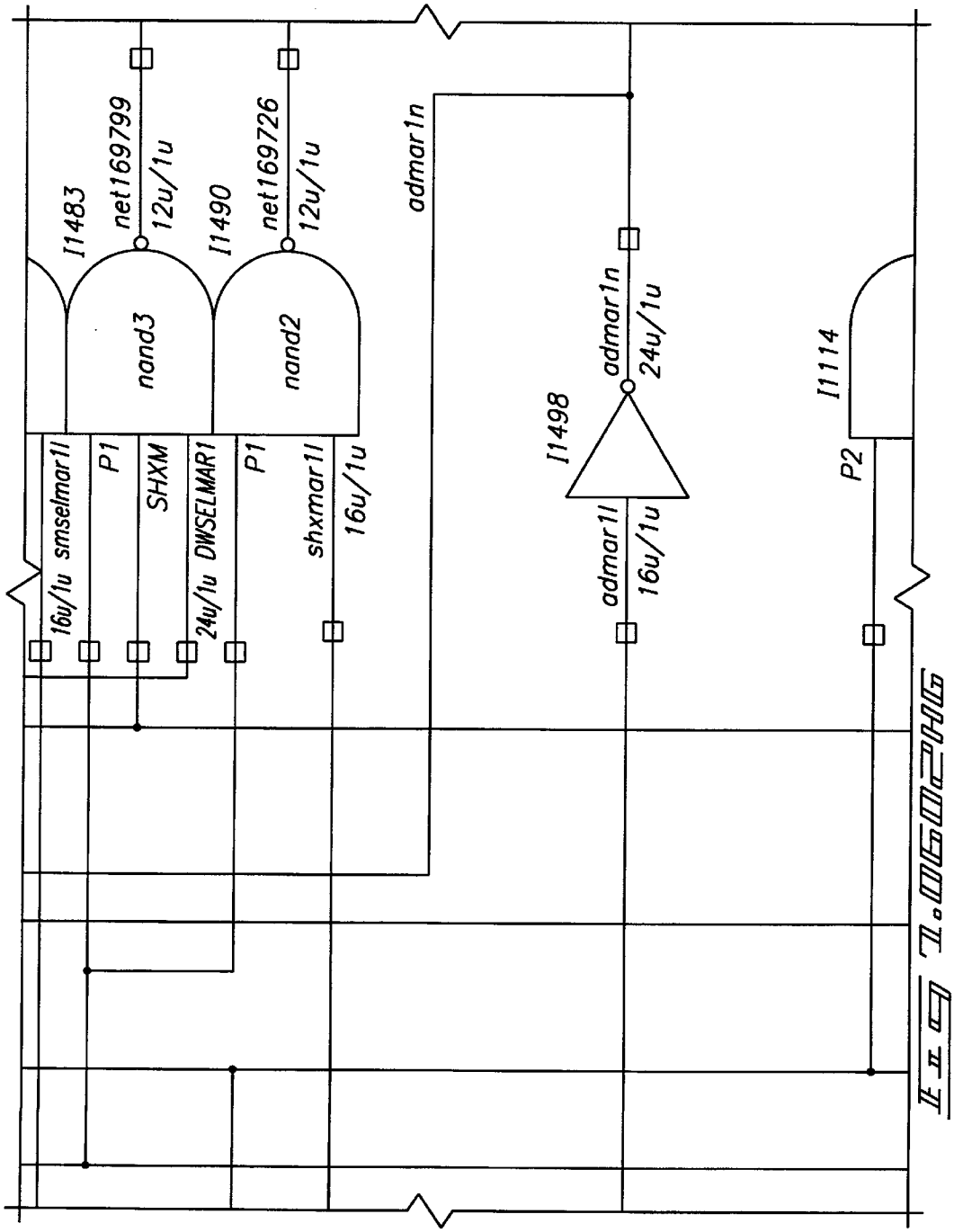


FIG 1.0502345

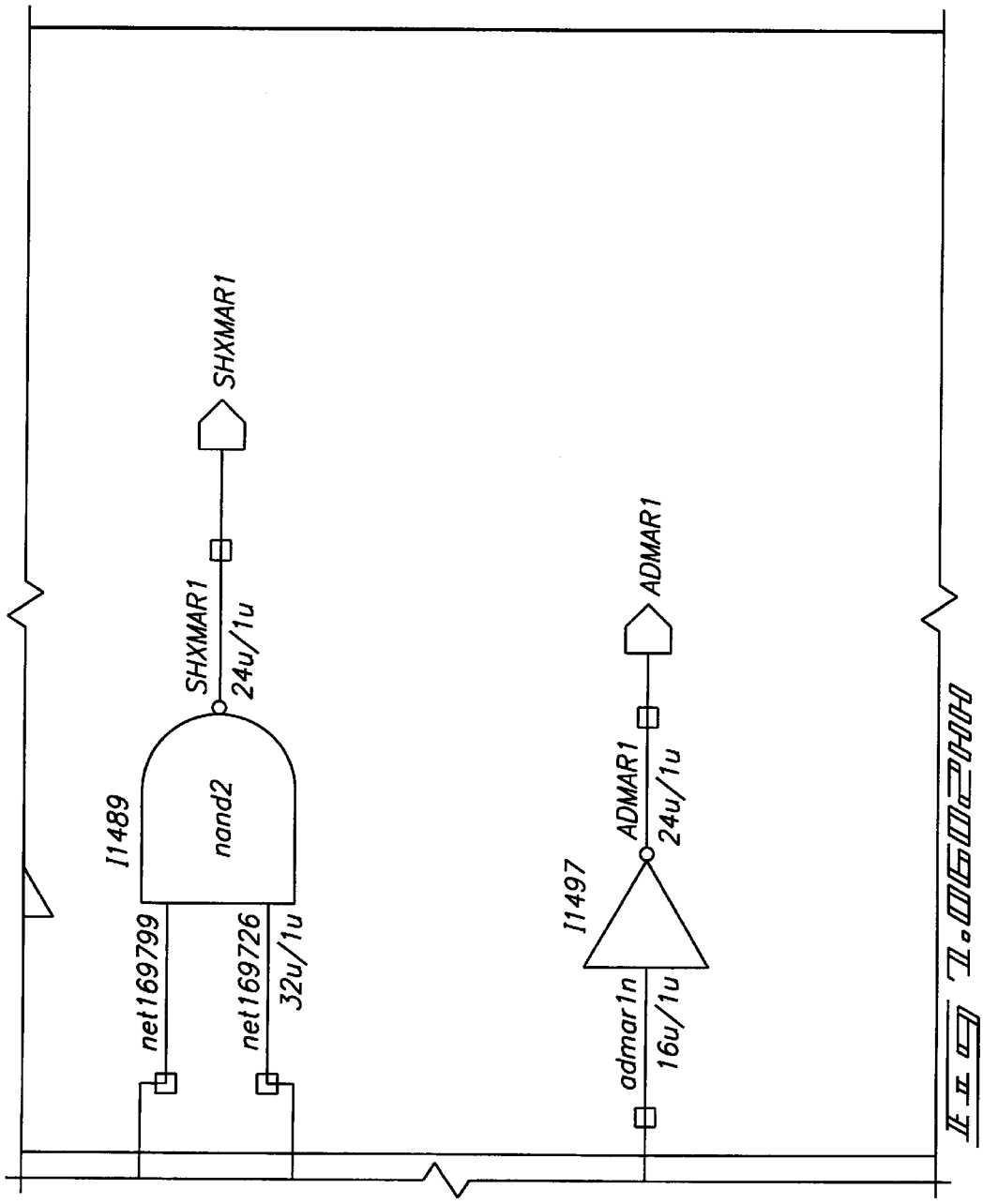

SHXMAR1
SHXMAR1
24u/1u
I1489
nand2
net169799
net169726
32u/1u
ADMAR1
ADMAR1
24u/1u
I1497
admar1n
16u/1u

Fig. 6,130,602

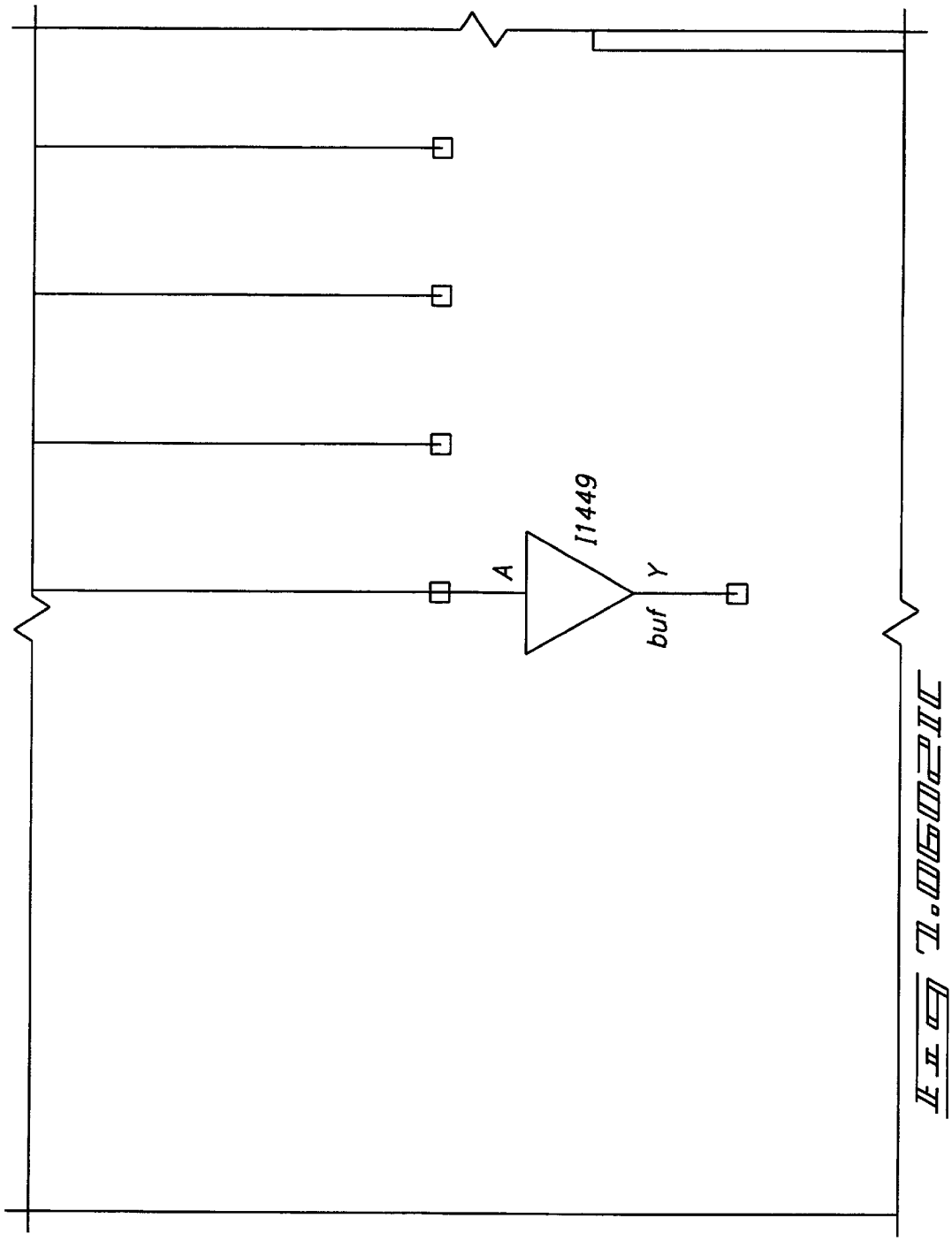


FIG. 1,600,628

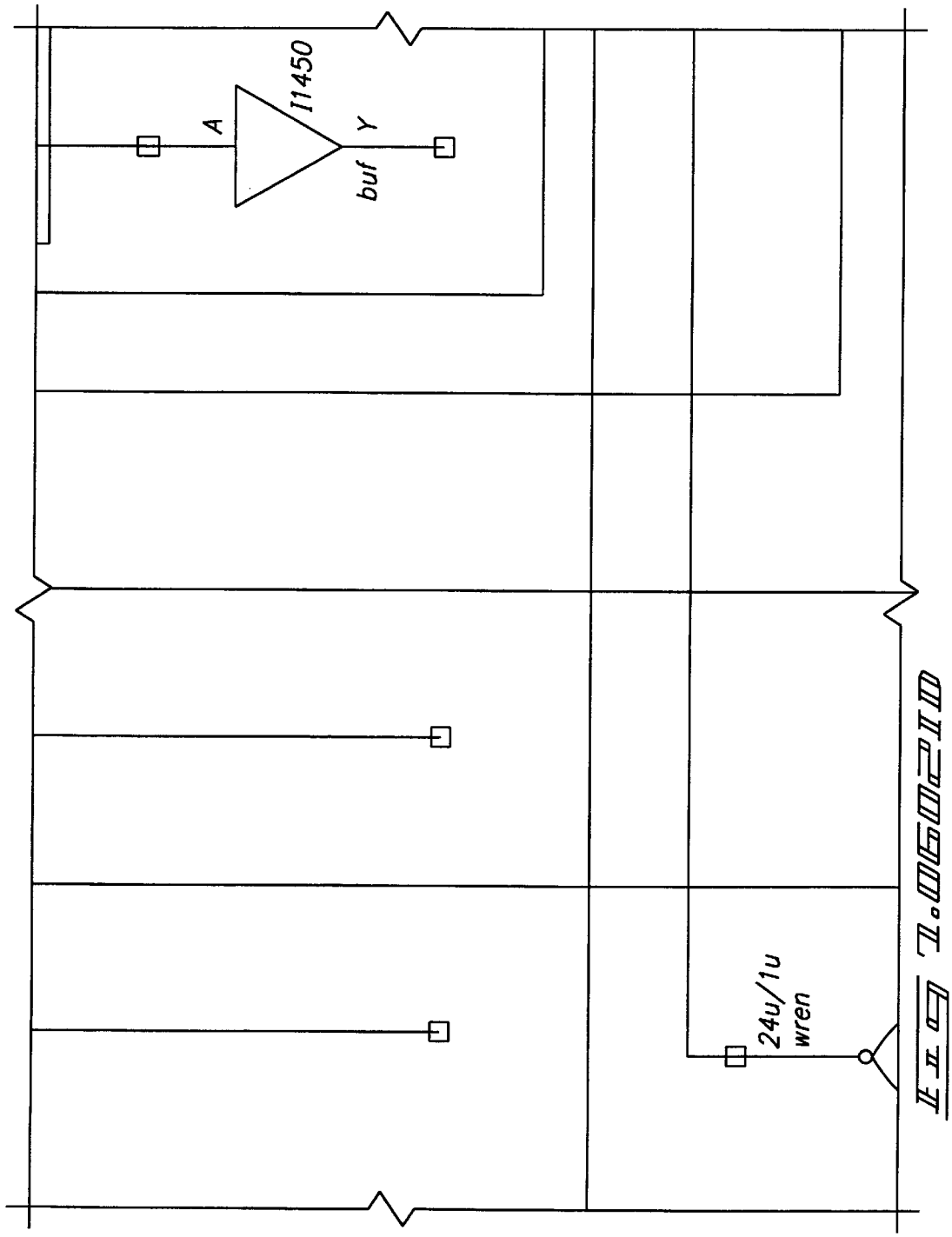


Fig 11.0502D

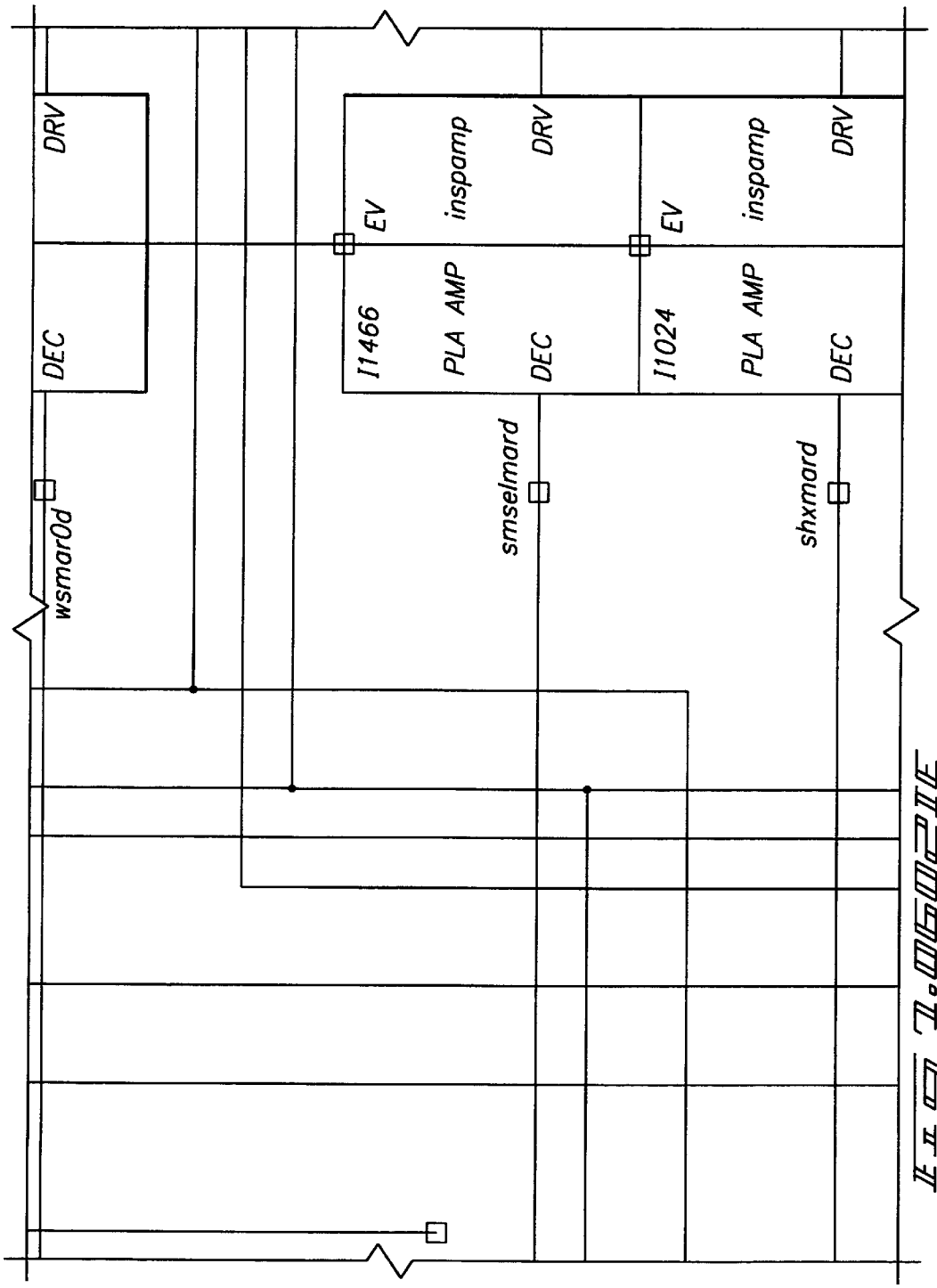
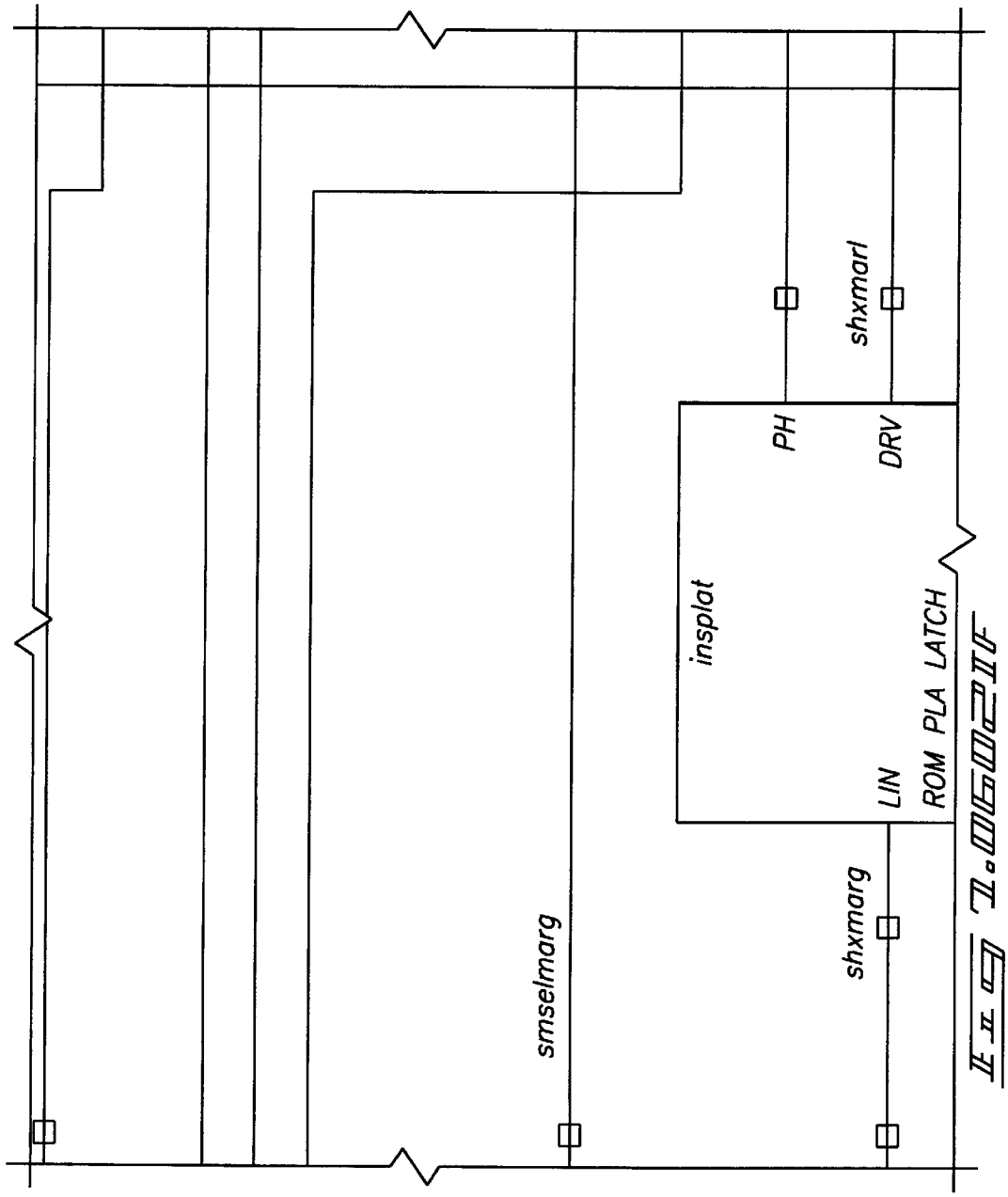

DRV
DEC
wsmar0d
EV
inspamp
DRV
I1466
PLA AMP
DEC
smselmard
EV
inspamp
DRV
I1024
PLA AMP
DEC
shxmard

FIG 7.0602E


shxmarl
PH
DRV
insplat
LIN
ROM PLA LATCH
shxmarg
smselmarg
FIG. 11.0602IF

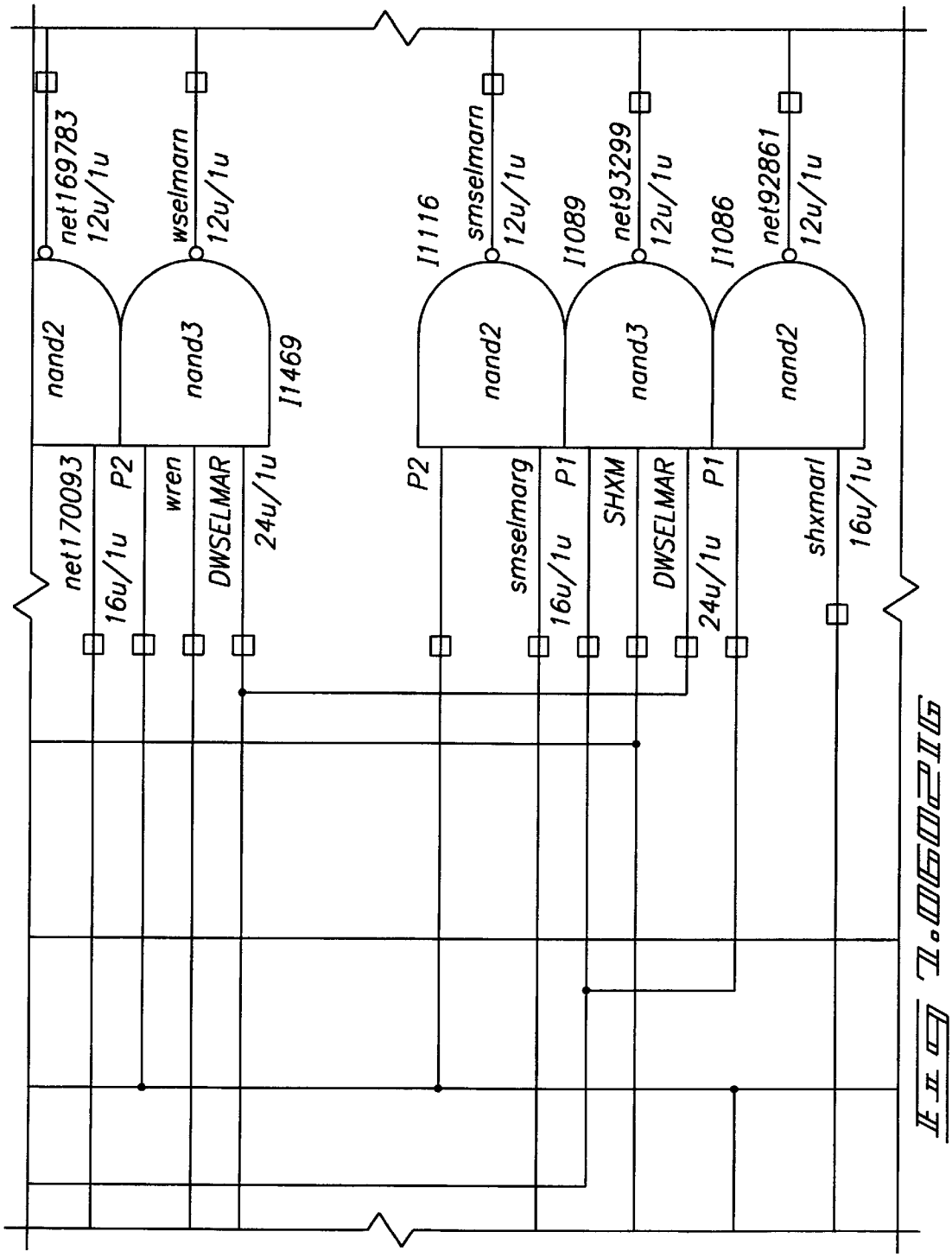
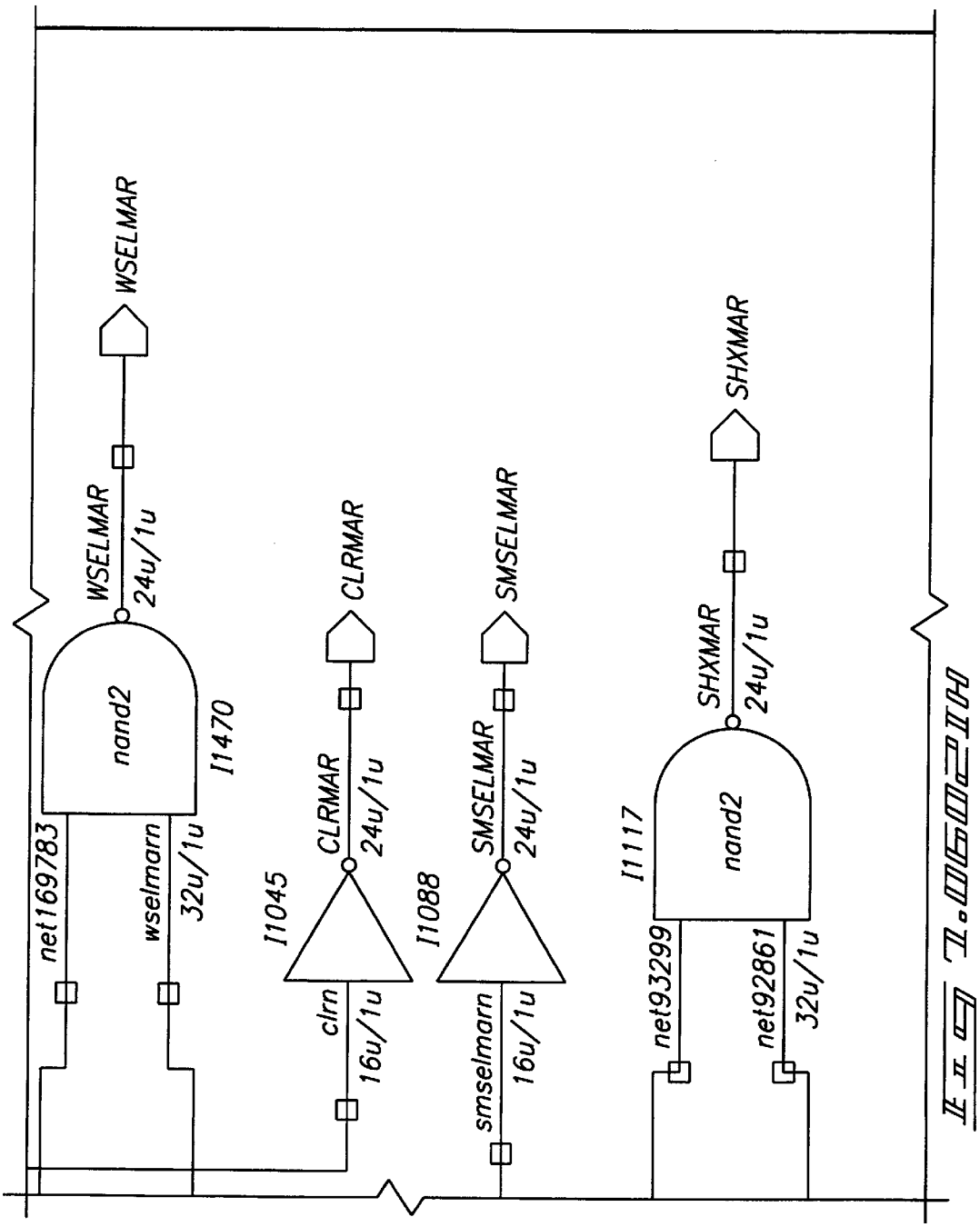


FIG 1.0602115


WSELMAR
WSELMAR
24u/1u
nand2
I1470
net169783
wselmarn
32u/1u
CLRMAR
CLRMAR
24u/1u
I1045
clrn
16u/1u
SMSELMAR
SMSELMAR
24u/1u
I1088
smselmarn
16u/1u
SHXMAR
SHXMAR
24u/1u
I1117
nand2
net93299
net92861
32u/1u

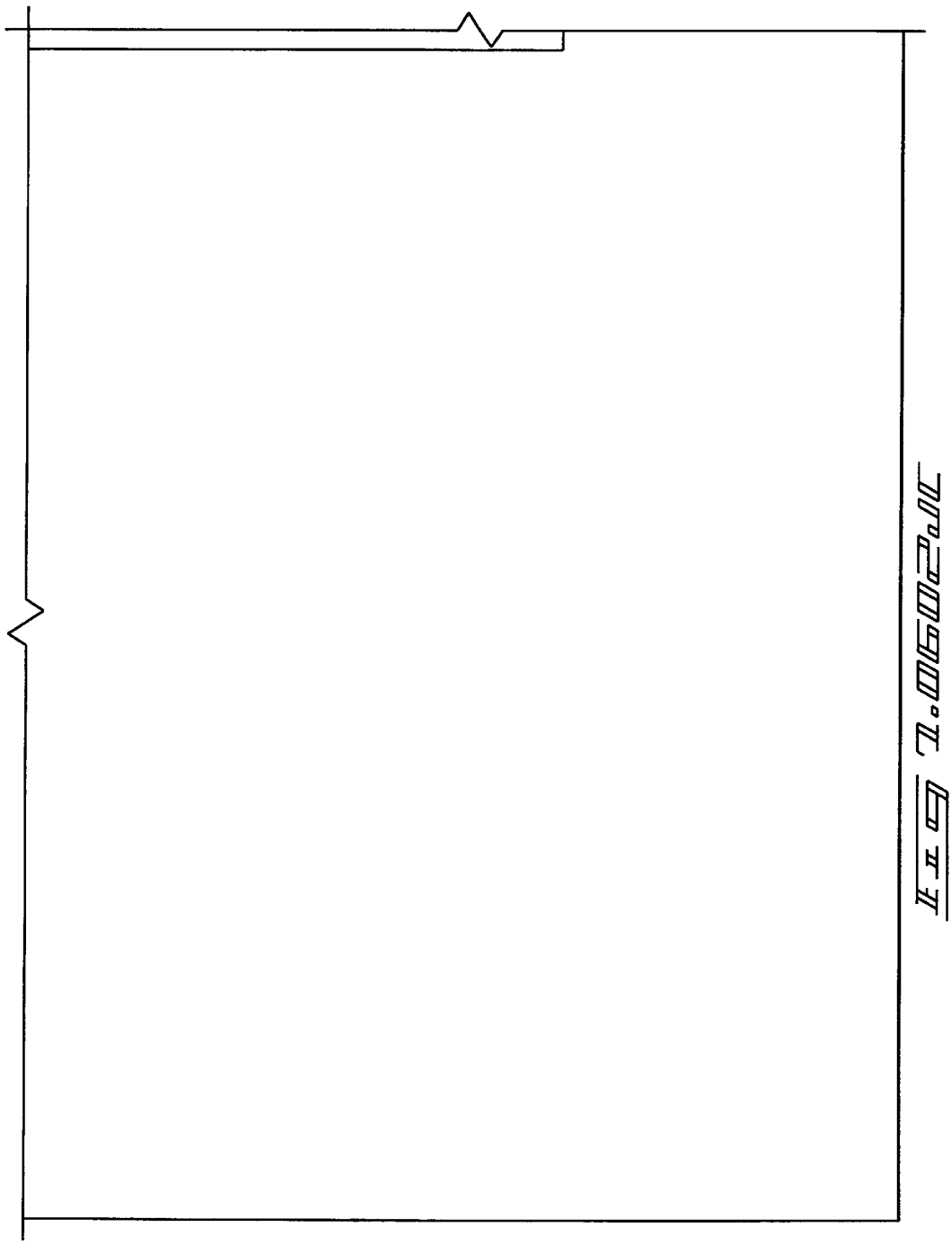


FIG. 7.0690E

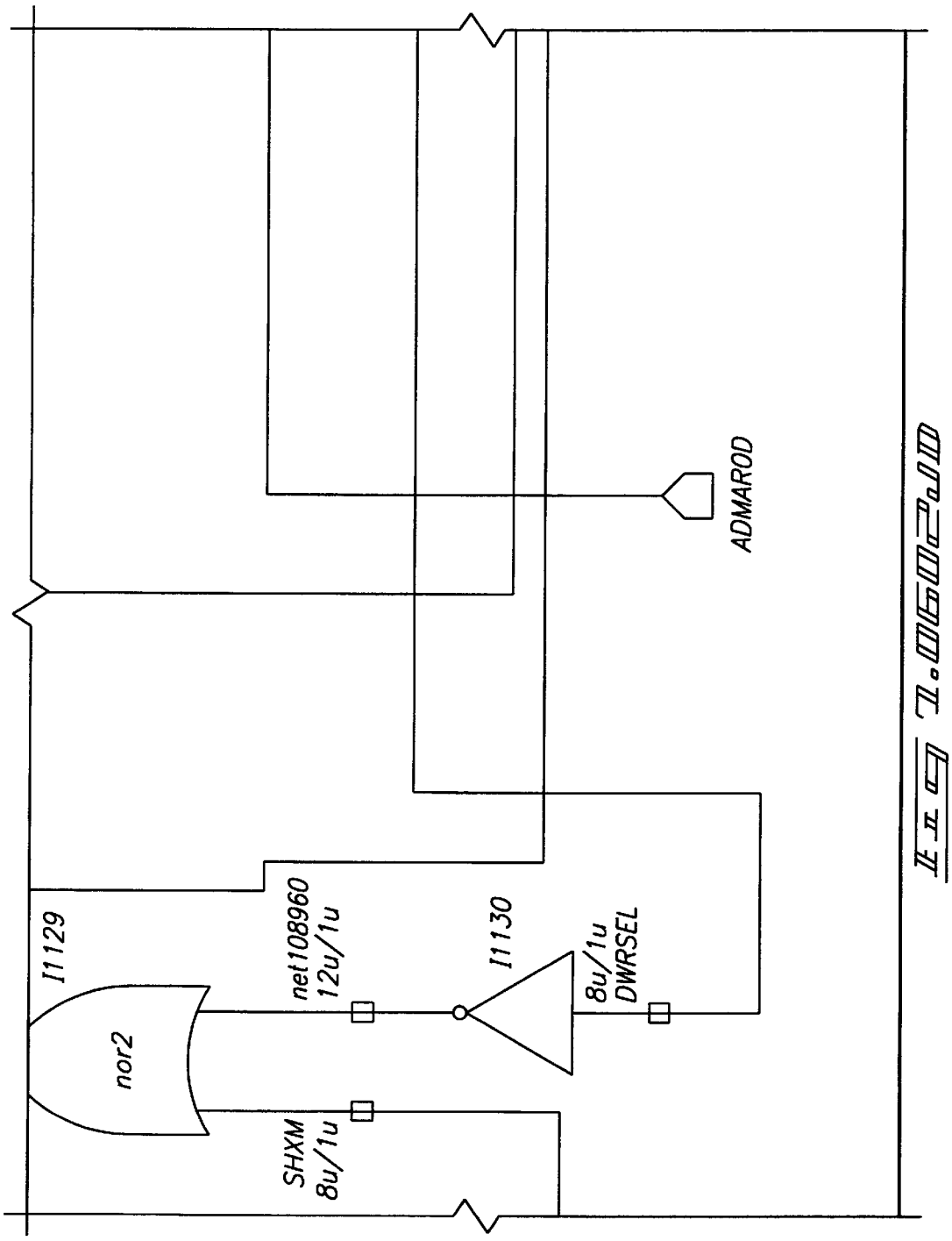

ADMAROD
I1129
nor2
net108960
12u/1u
I1130
8u/1u
DWRSEL
SHXM
8u/1u

FIG. 1.0600.11

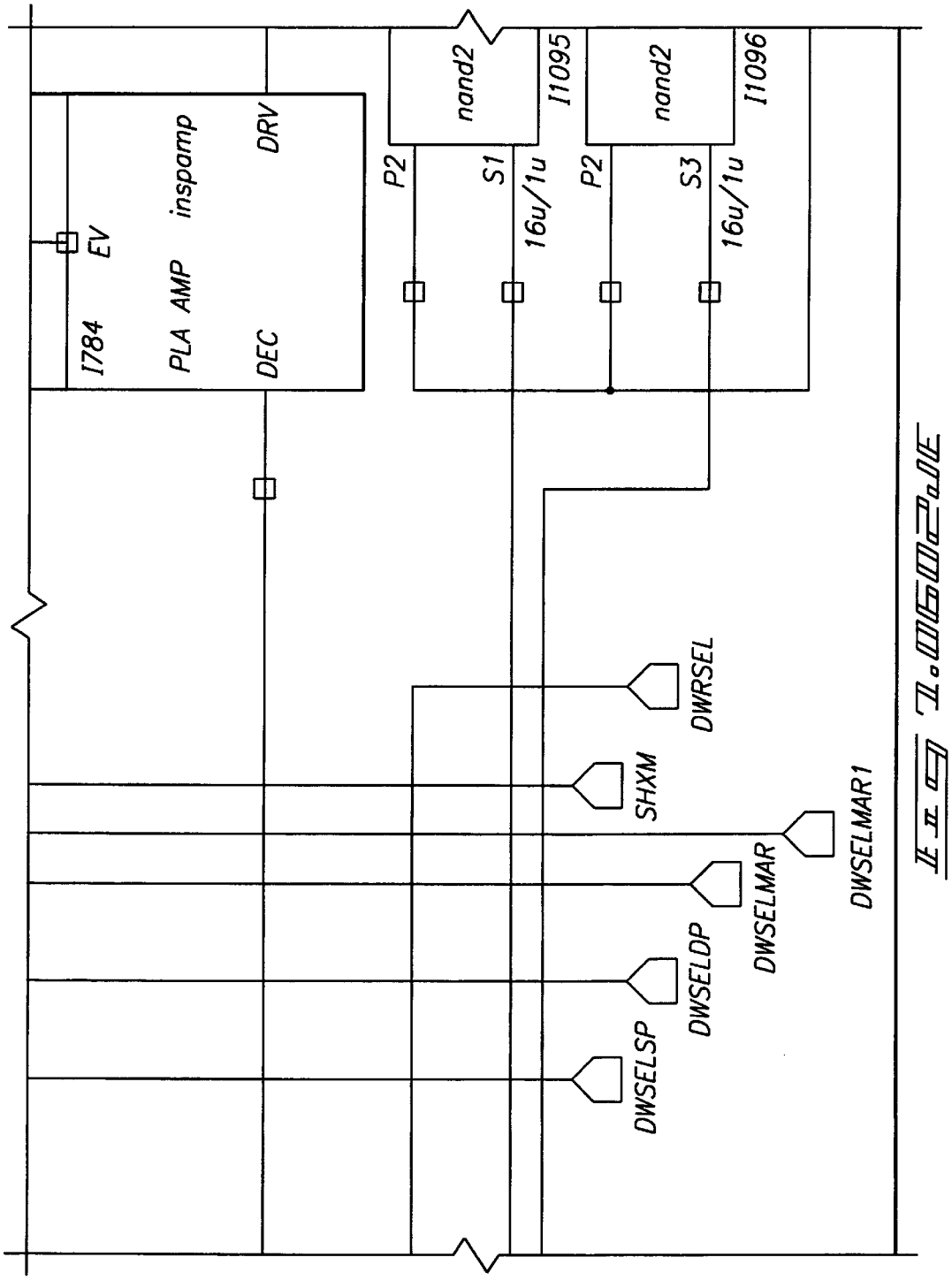

I784
EV
PLA AMP
inspamp
DEC
DRV
nand2
I1095
P2
S1
16u/1u
nand2
I1096
P2
S3
16u/1u
DWRSEL
SHXM
DWSELMAR1
DWSELMAR
DWSELDP
DWSELSP

FIG 1,006,208

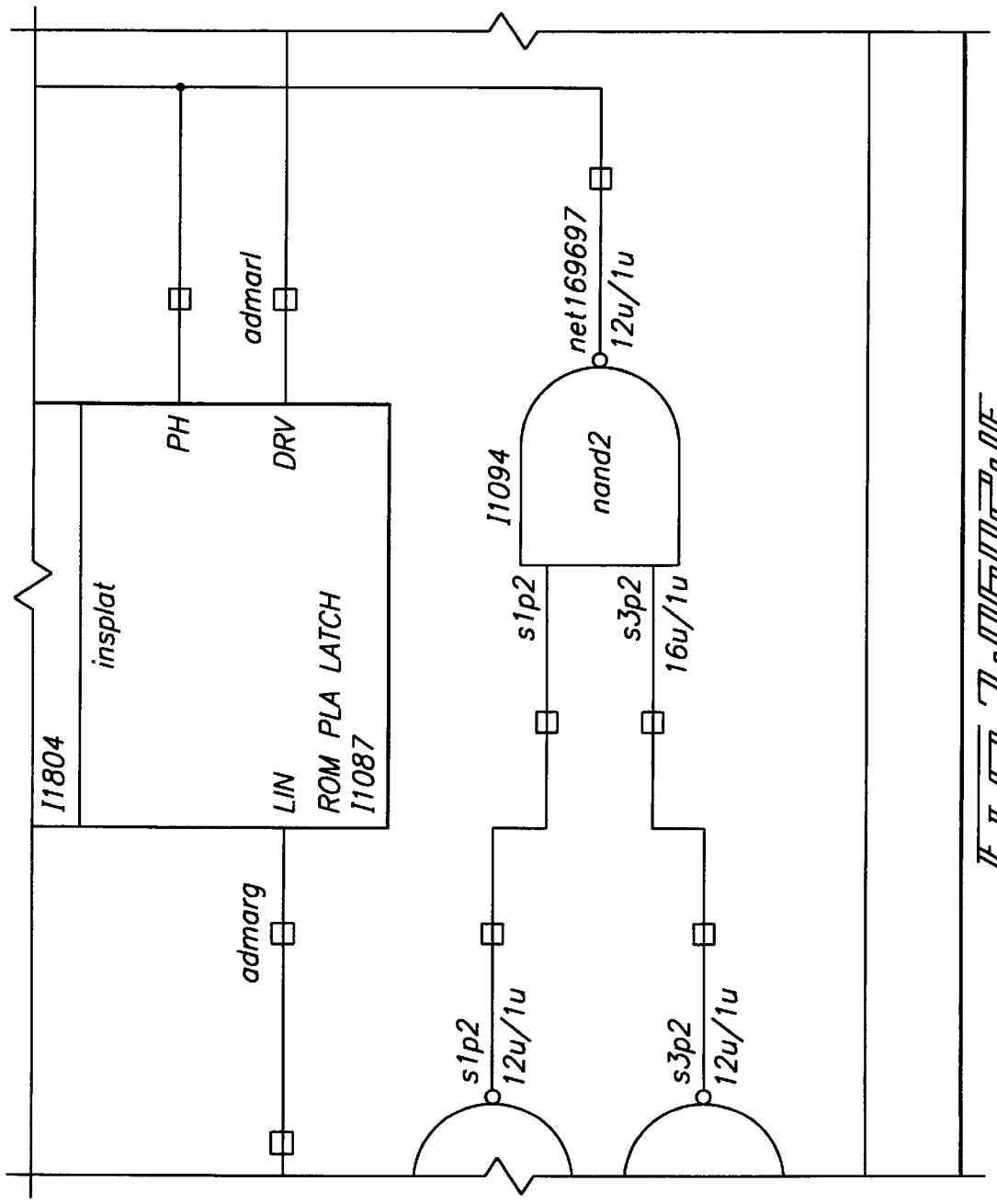
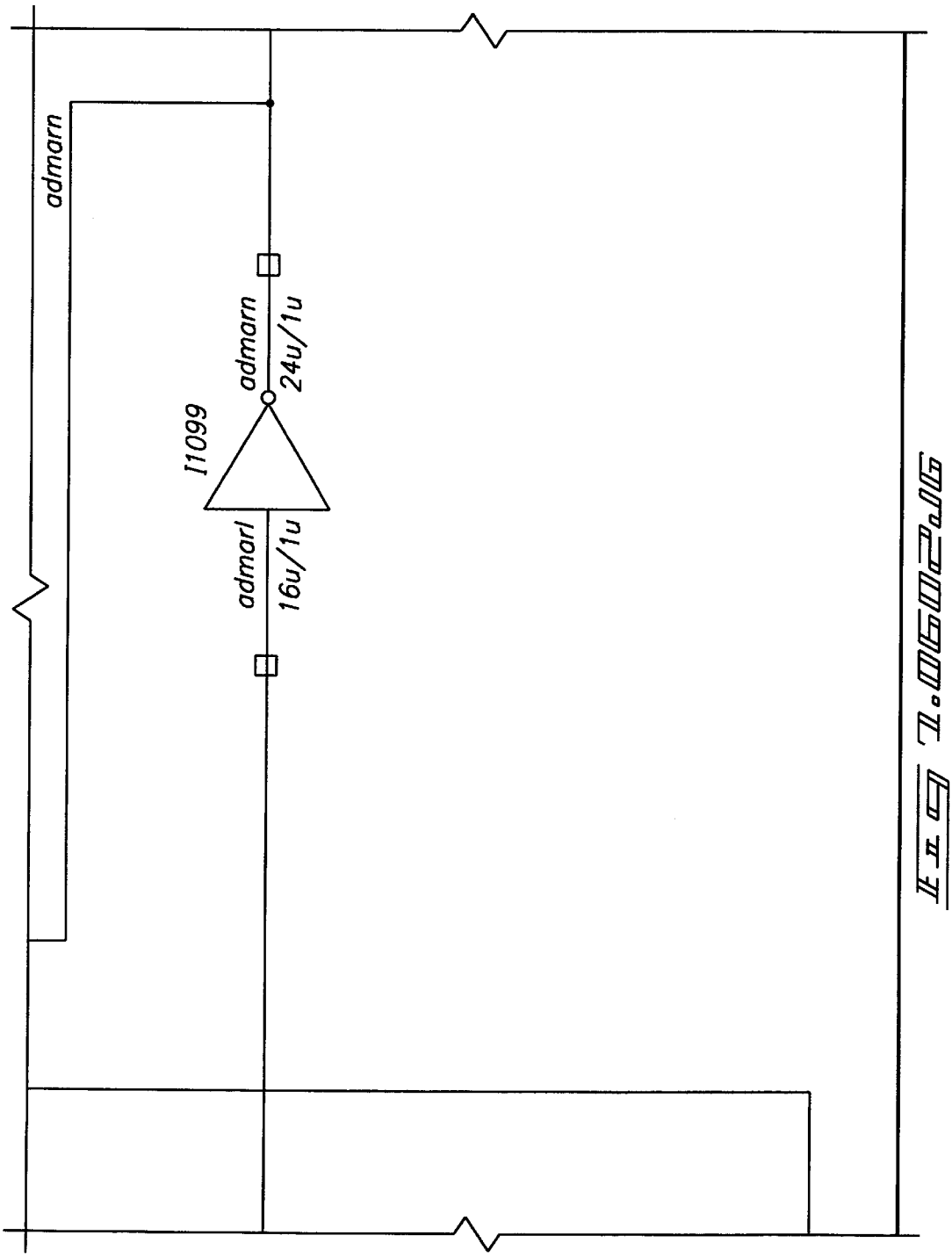

admarl
net169697
12u/1u
PH
DRV
I1094
nand2
insplat
s1p2
s3p2
16u/1u
I1804
LIN
ROM PLA LATCH
I1087
admarg
s1p2
12u/1u
s3p2
12u/1u

FIG 1.0600AF


admarn
admarn
24u/1u
I1099
admarl
16u/1u
FIG 7,060,602

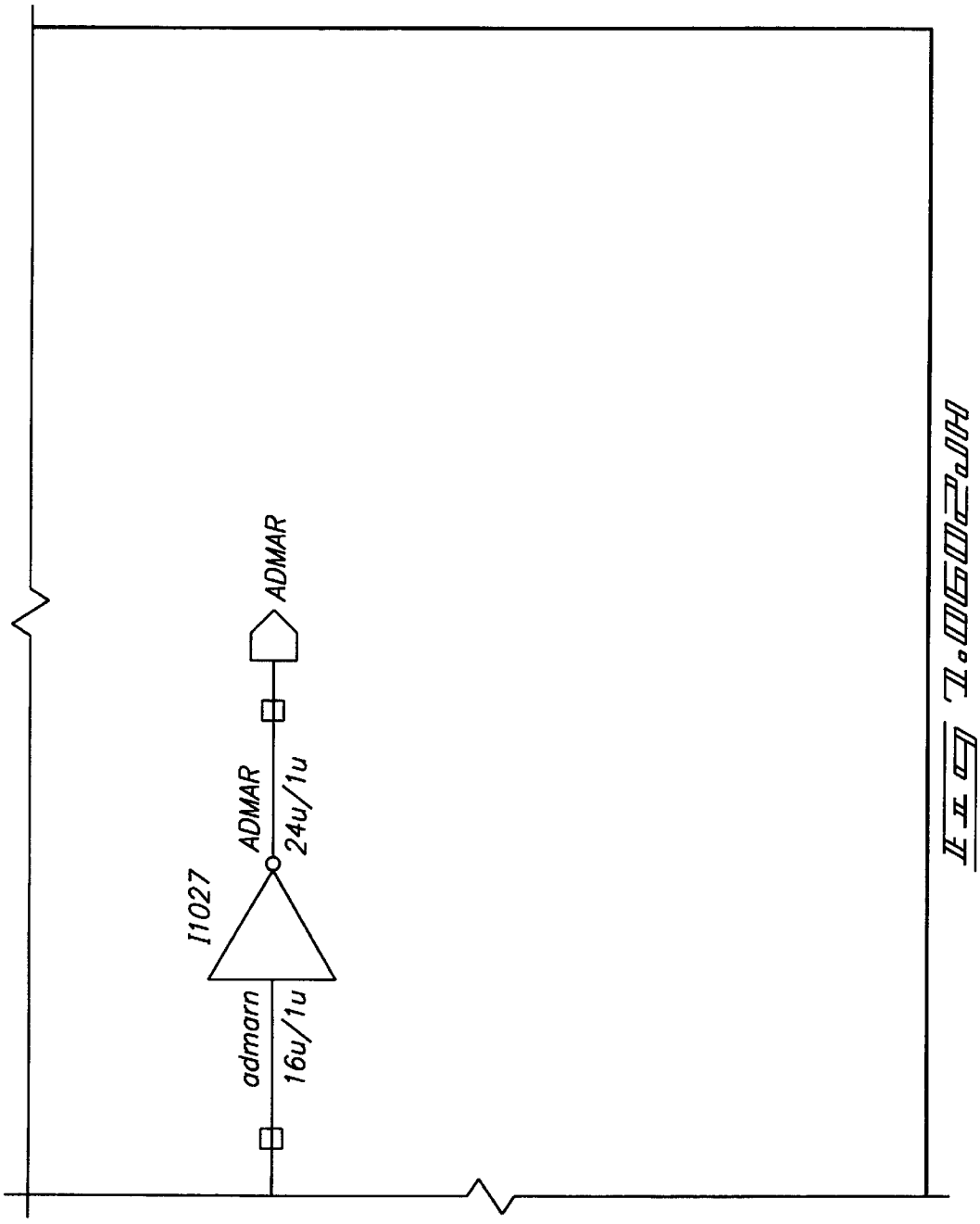


FIG 7,059,L

7.0603AA	7.0603AB	7.0603AC	7.0603AD	7.0603AE	7.0603AF		7.0603AH	7.0603AI	7.0603AJ		
7.0603BA	7.0603BB	7.0603BC	7.0603BD	7.0603BE	7.0603BF	7.0603BG	7.0603BH	7.0603BI	7.0603BJ	7.0603BK	
7.0603CA	7.0603CB	7.0603CC	7.0603CD	7.0603CE	7.0603CF	7.0603CG	7.0603CH	7.0603CI	7.0603CJ		
7.0603DA	7.0603DB	7.0603DC	7.0603DD	7.0603DE	7.0603DF	7.0603DG	7.0603DH	7.0603DI	7.0603DJ		
7.0603EA	7.0603EB	7.0603EC	7.0603ED	7.0603EE	7.0603EF	7.0603EG	7.0603EH	7.0603EI	7.0603EJ		
7.0603FA	7.0603FB	7.0603FC	7.0603FD	7.0603FE	7.0603FF	7.0603FG	7.0603FH	7.0603FI	7.0603FJ		
7.0603GA	7.0603GB	7.0603GC	7.0603GD	7.0603GE	7.0603GF	7.0603GG	7.0603GH	7.0603GI	7.0603GJ		
7.0603HA	7.0603HB	7.0603HC	7.0603HD	7.0603HE	7.0603HF	7.0603HG	7.0603HH	7.0603HI	7.0603HJ		
7.0603IA	7.0603IB	7.0603IC	7.0603ID	7.0603IE	7.0603IF	7.0603IG	7.0603IH	7.0603II	7.0603IJ		
		7.0603JC	7.0603JD	7.0603JE	7.0603JF	7.0603JG		7.0603JI			

FIG. 7.0603.IL

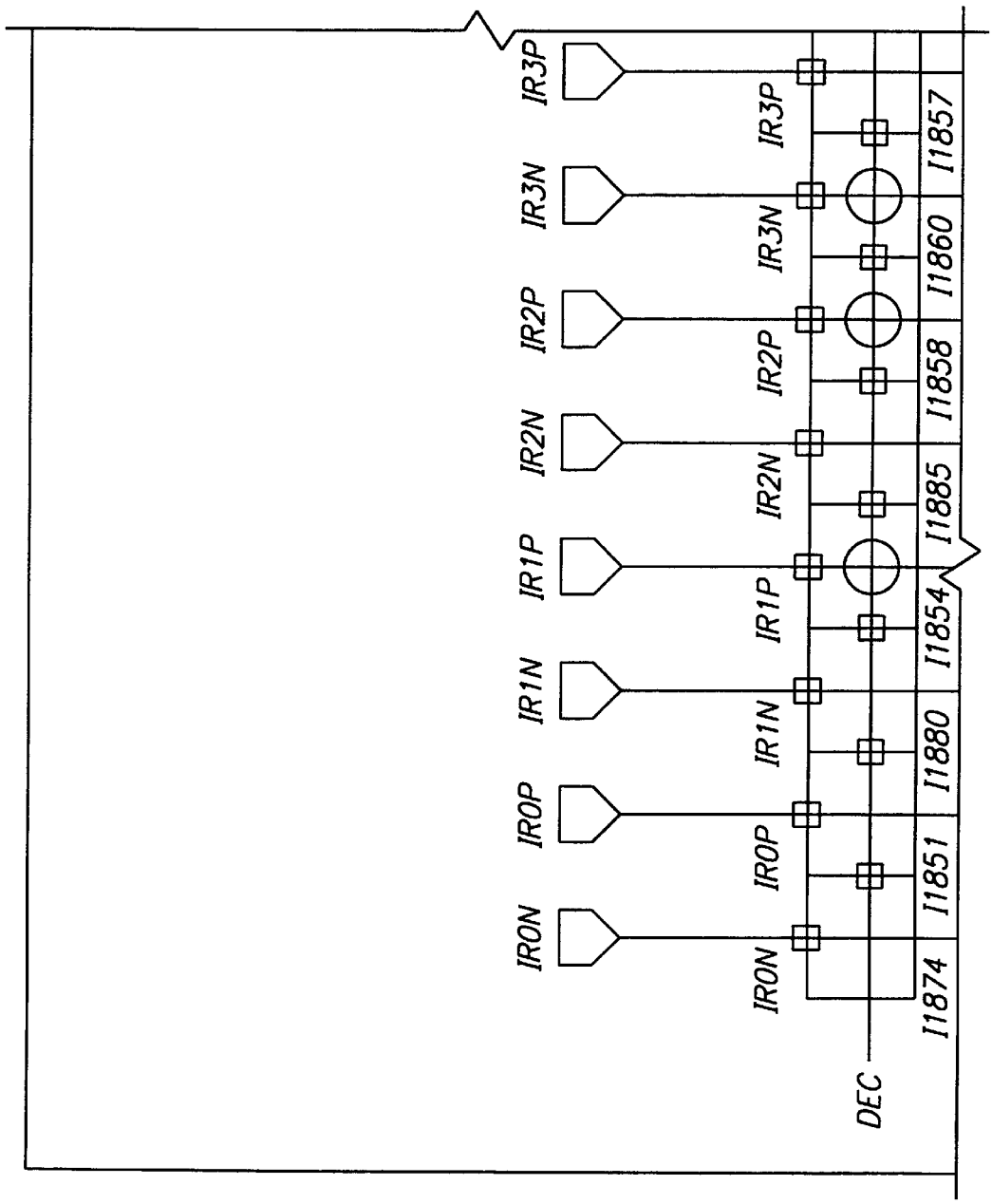

IR3P
IR3N
IR2P
IR2N
IR1P
IR1N
IR0P
IR0N
I1857
I1860
I1858
I1885
I1854
I1880
I1851
I1874
DEC

FIG. 1L

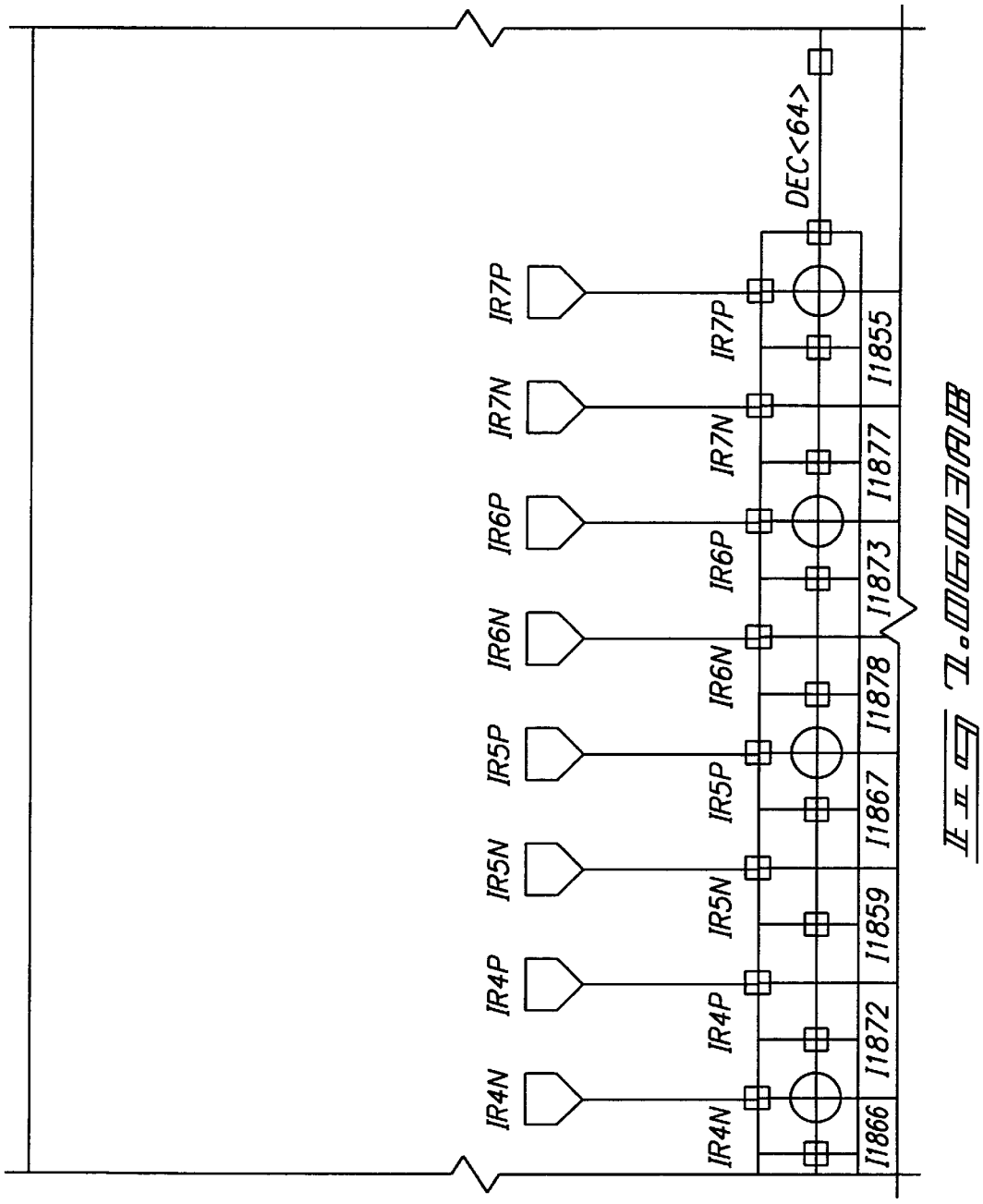

DEC<64>
IR7P
IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
IR4N
I1855
I1877
I1873
I1878
I1867
I1859
I1872
I1866

FIG. 1L

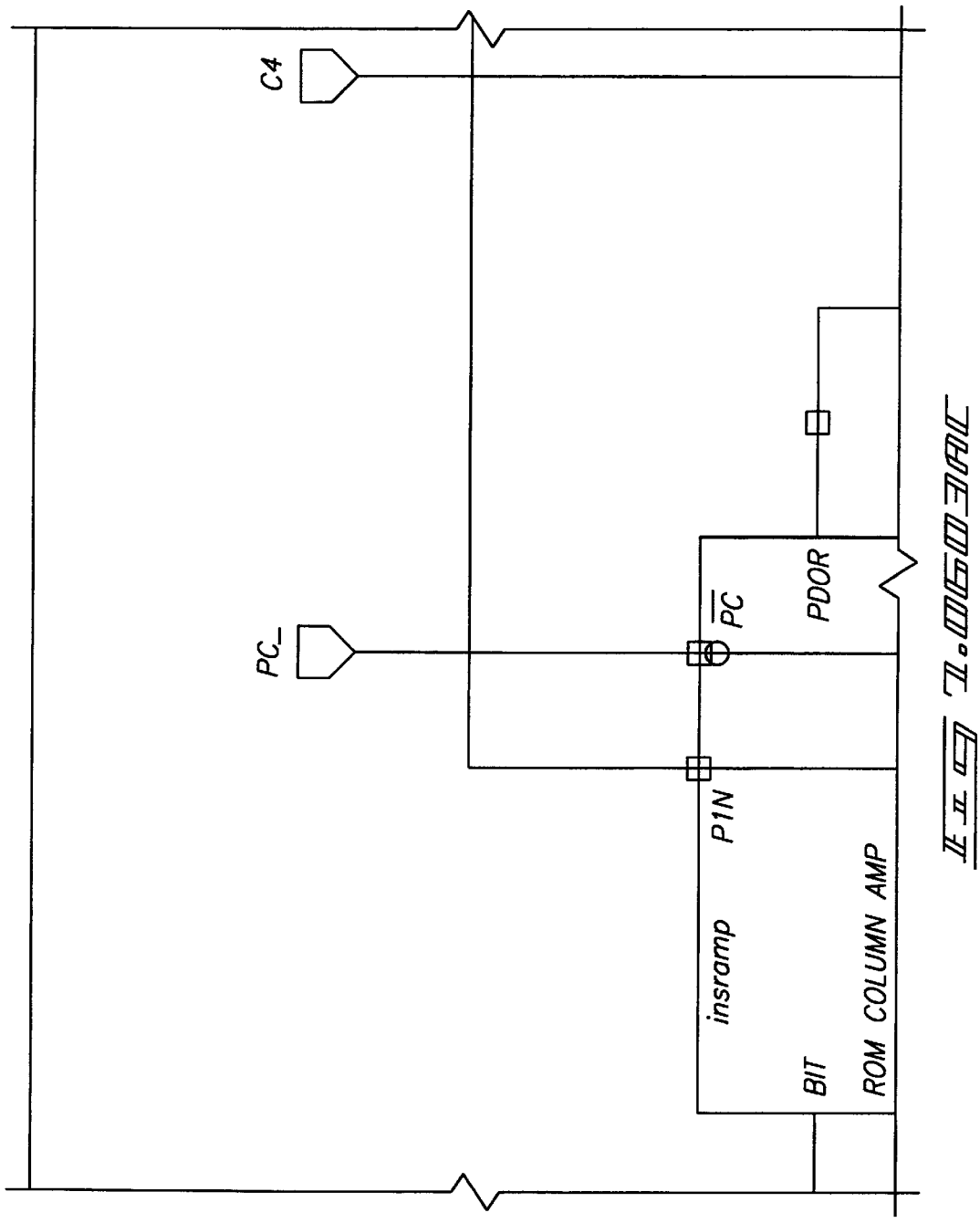
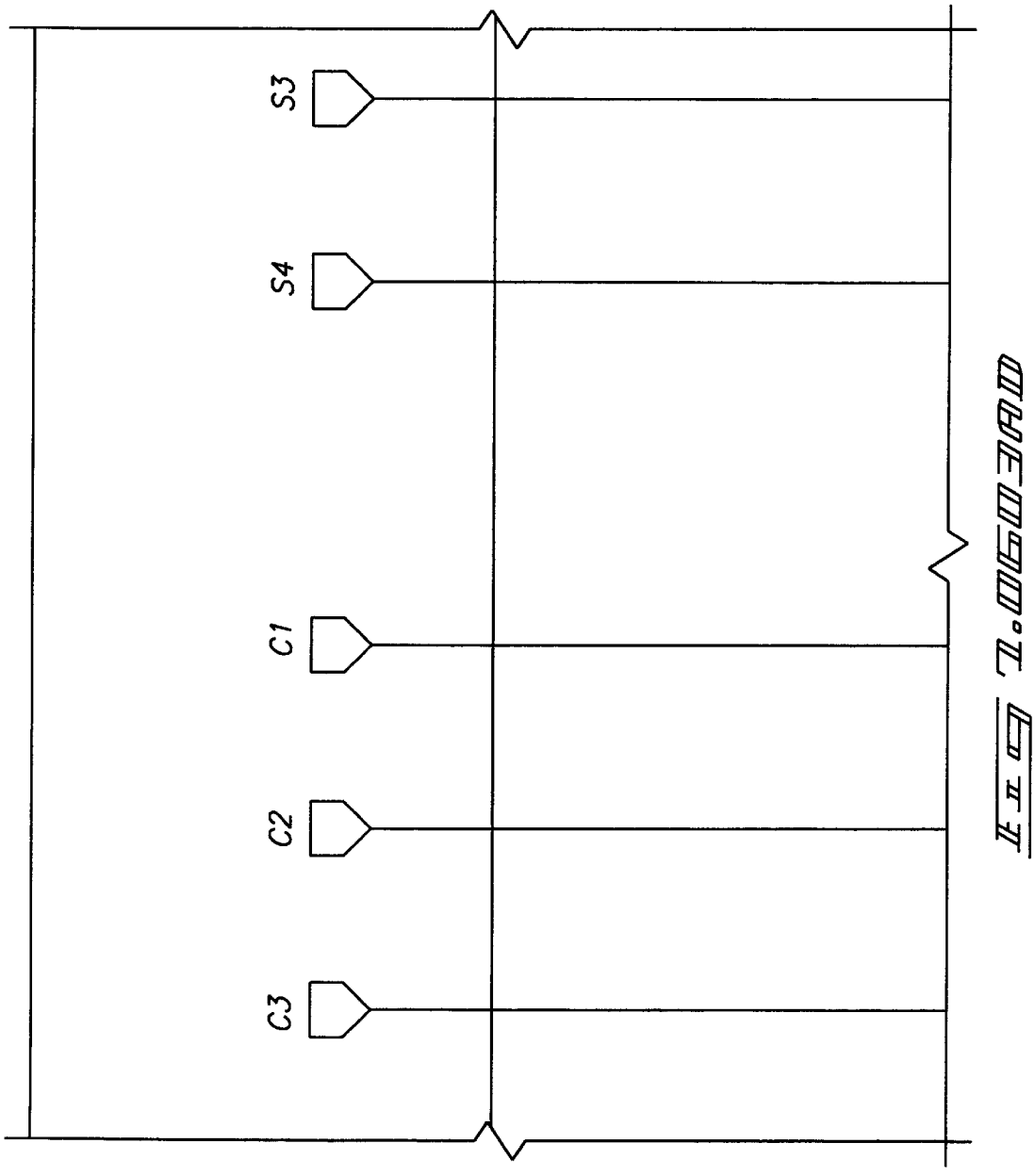


FIG. 643


S3
S4
C1
C2
C3
FIG. 1,050,000

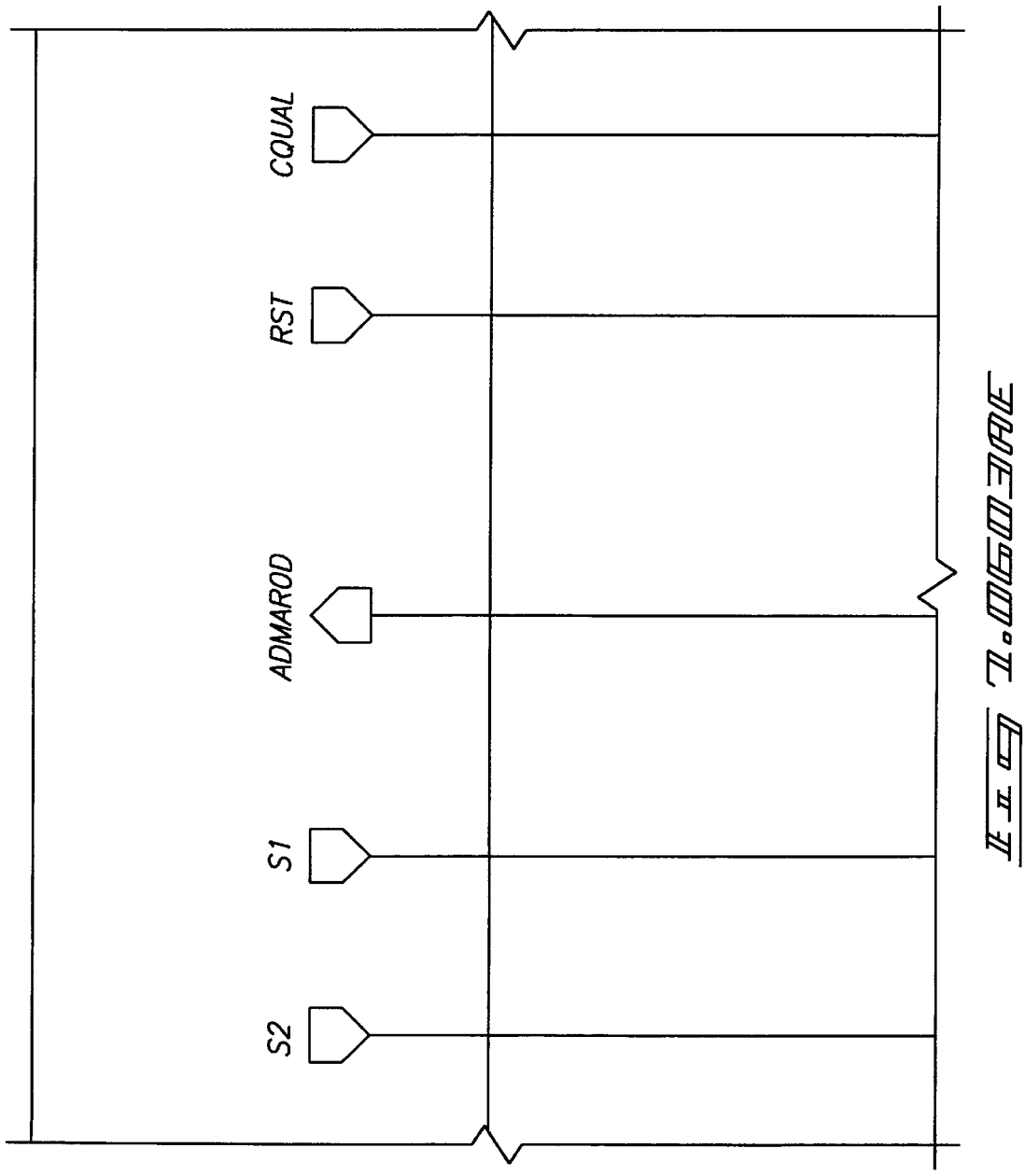
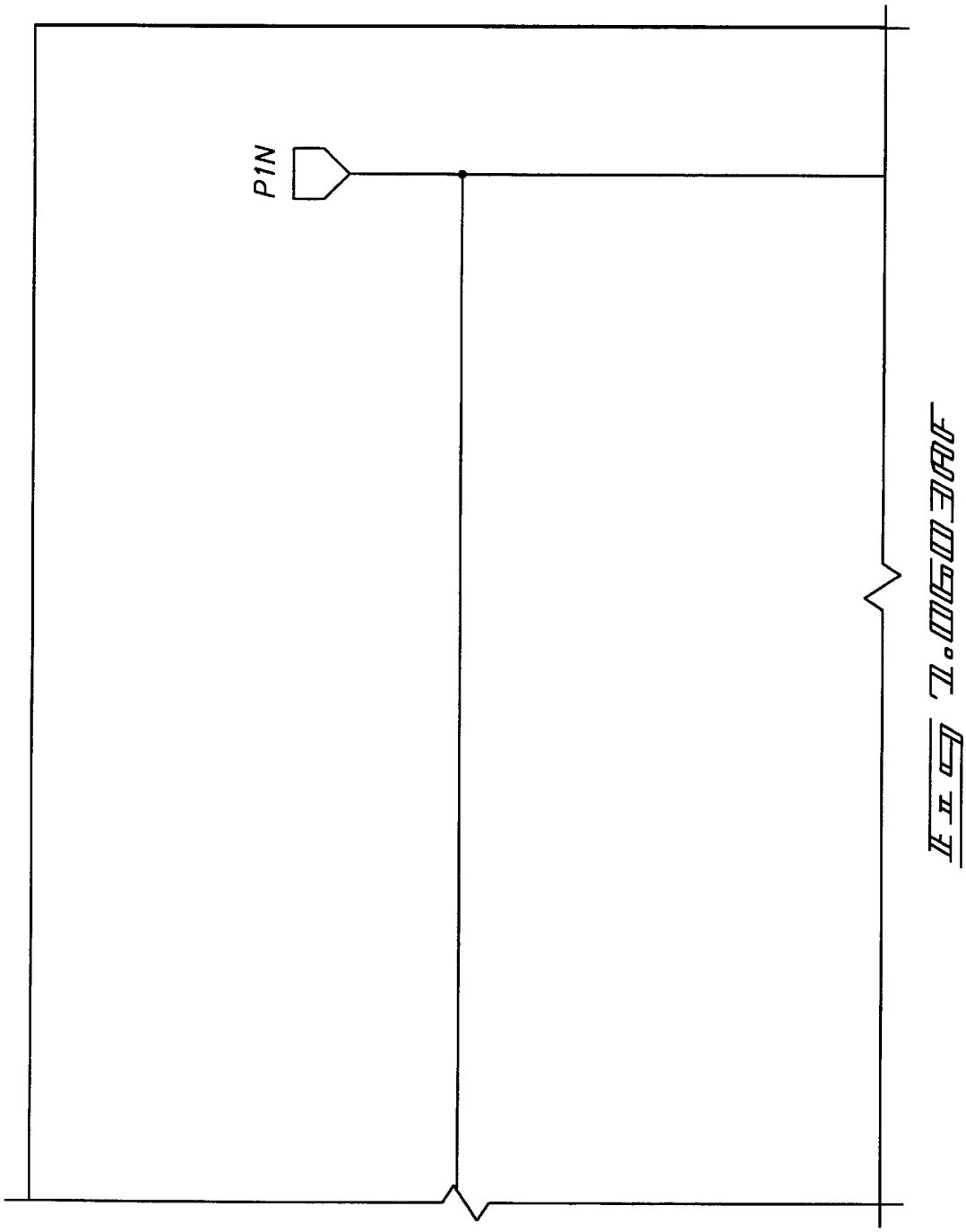
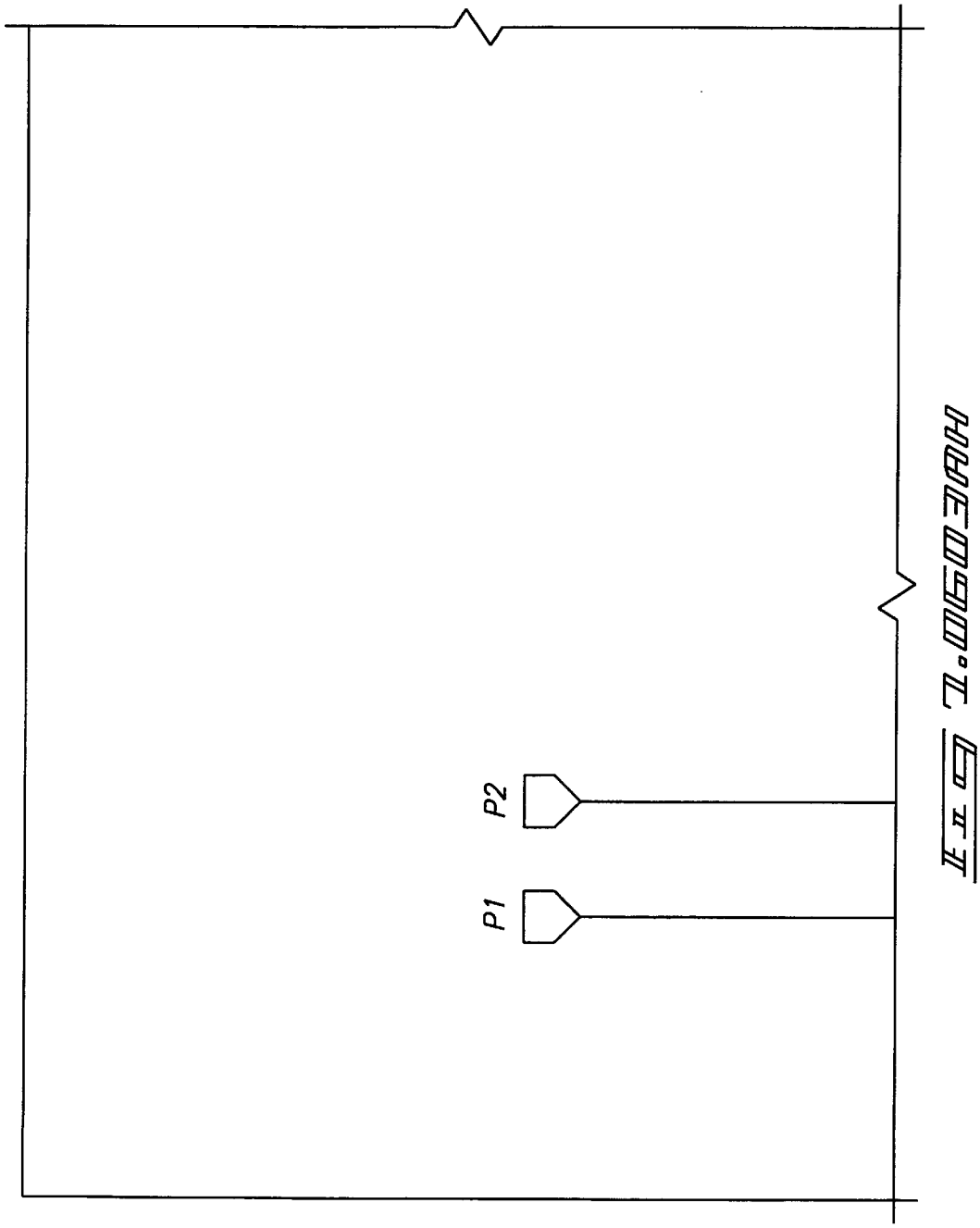


FIG 645.1


PIN
FIG. 1,050,000


P2
P1
FIG. 705

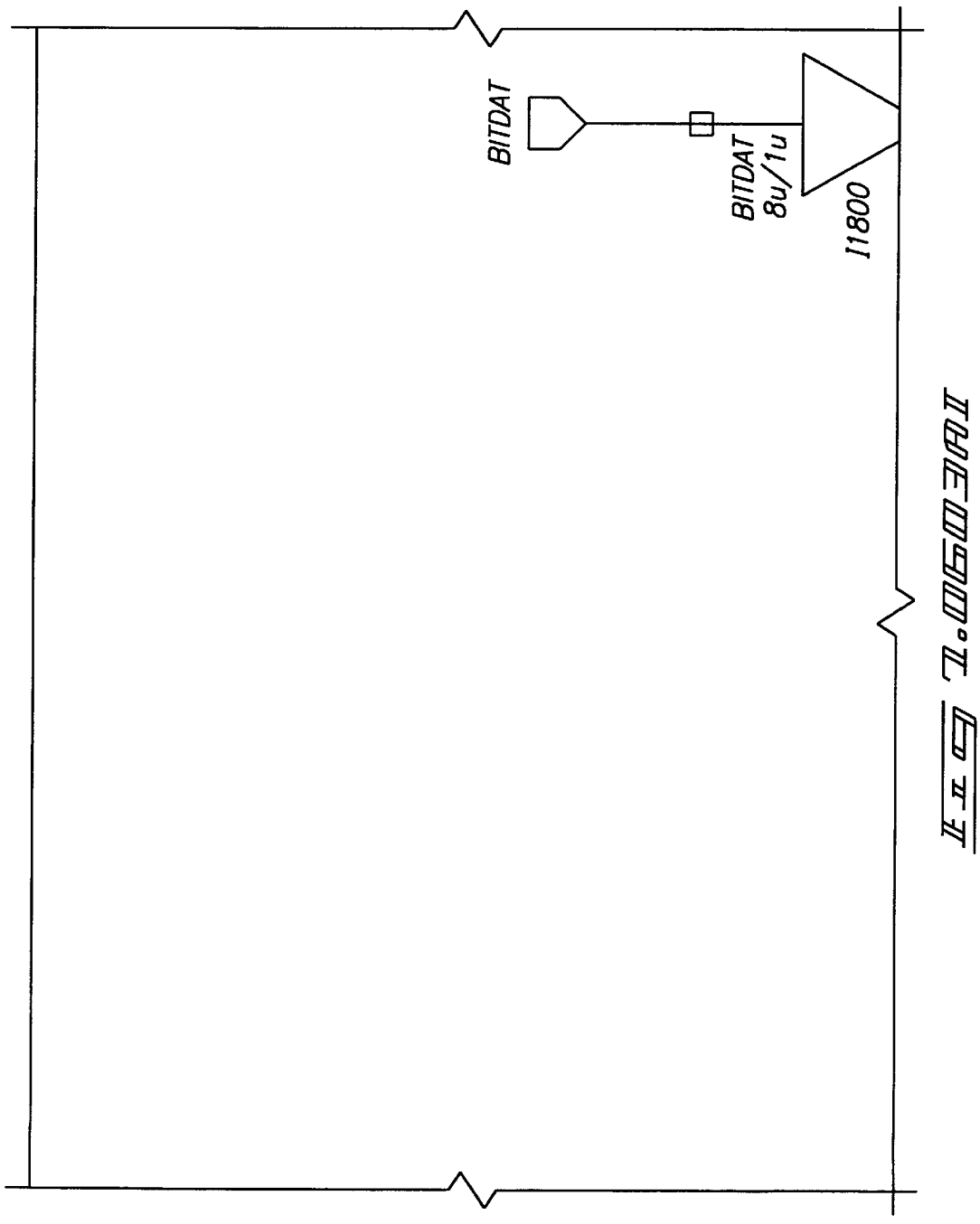


FIG. 11850

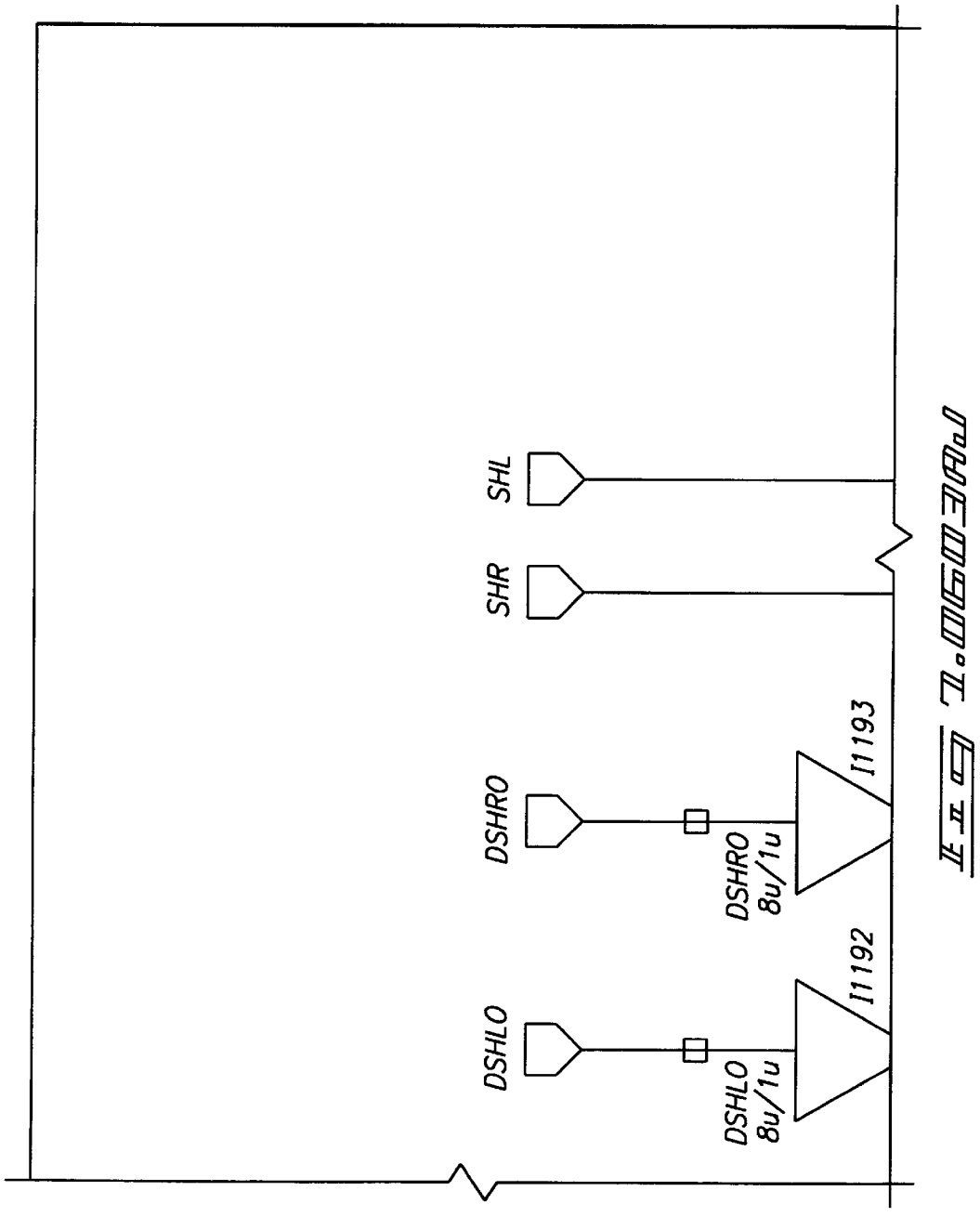


FIG 649

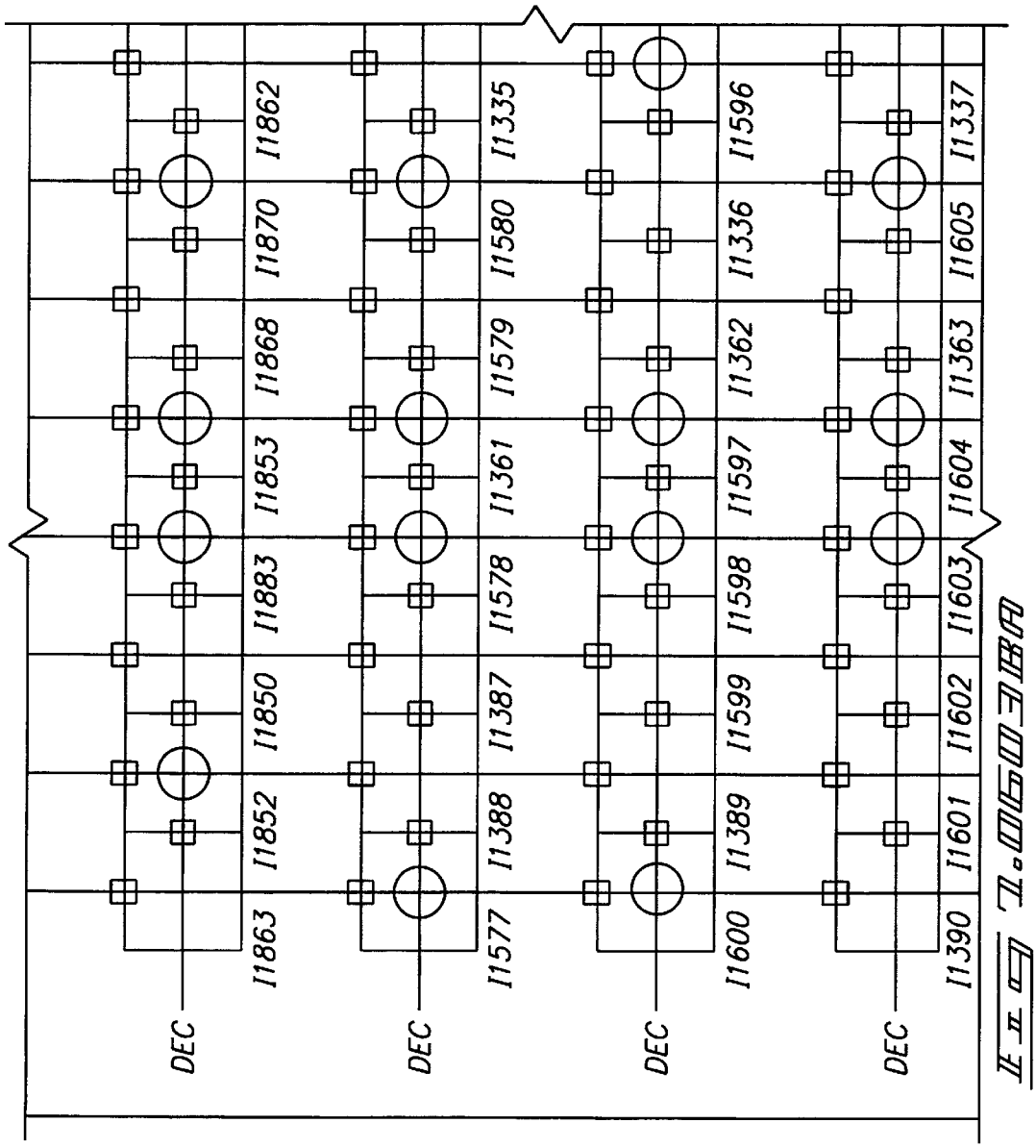
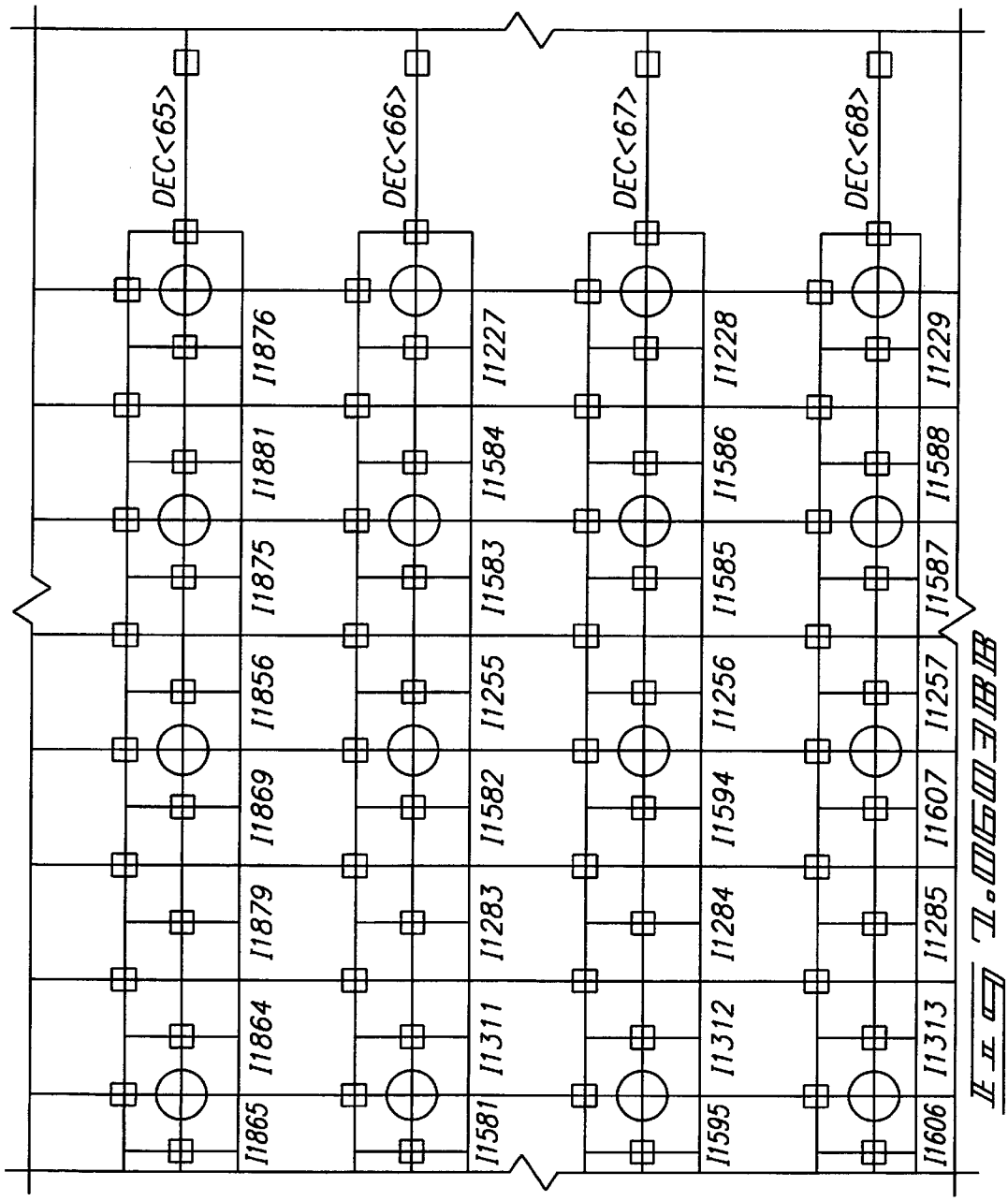

DEC
DEC
DEC
DEC
I1862
I1870
I1868
I1853
I1883
I1850
I1852
I1863
I1335
I1580
I1579
I1361
I1578
I1387
I1388
I1577
I1596
I1336
I1362
I1597
I1598
I1599
I1389
I1600
I1337
I1605
I1363
I1604
I1603
I1602
I1601
I1390

FIG. 650.11


DEC<65>
DEC<66>
DEC<67>
DEC<68>
I1876
I1881
I1875
I1856
I1869
I1879
I1864
I1865
I1227
I1584
I1583
I1255
I1582
I1283
I1311
I1581
I1228
I1586
I1585
I1256
I1594
I1284
I1312
I1595
I1229
I1588
I1587
I1257
I1607
I1285
I1313
I1606

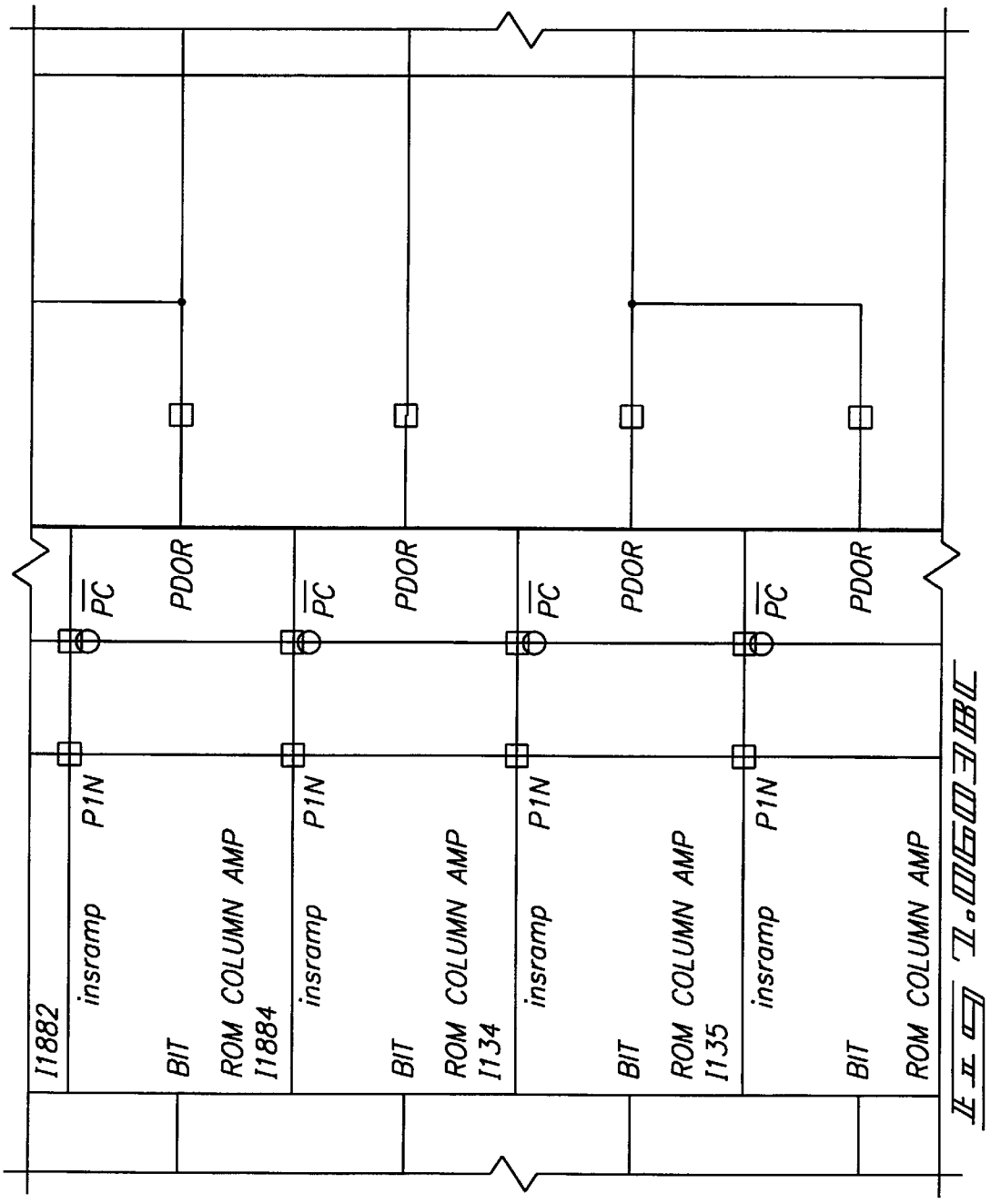
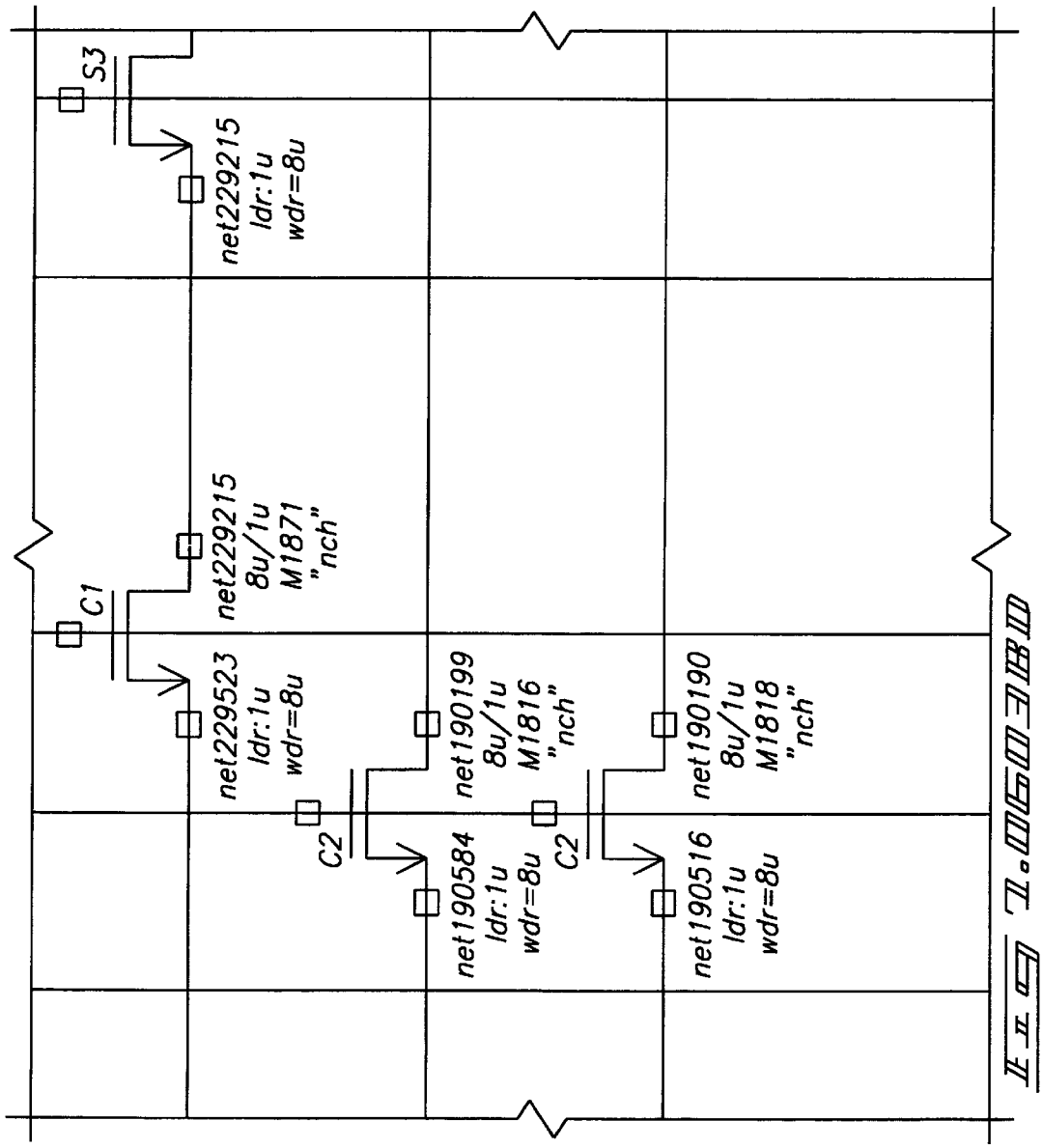
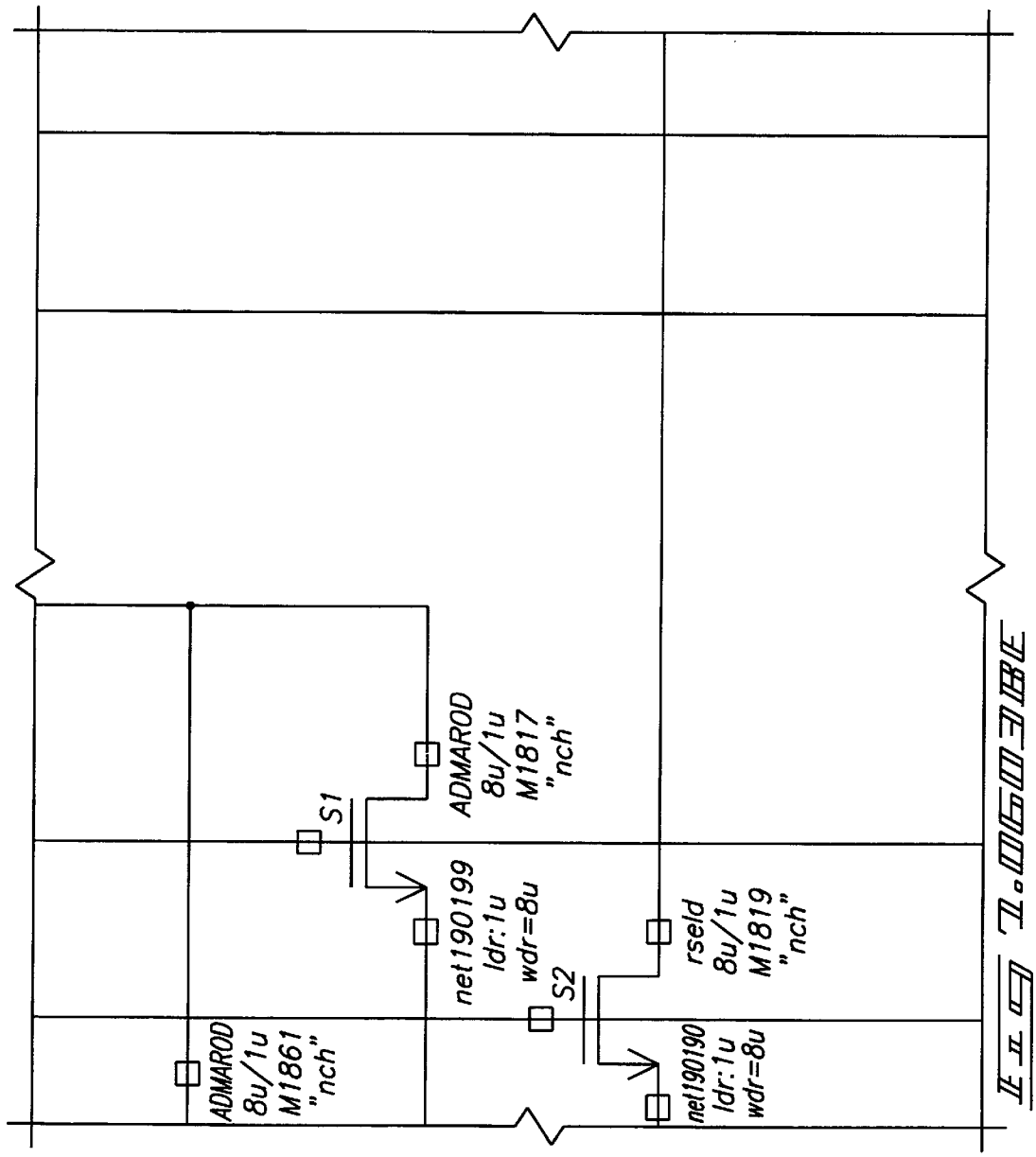
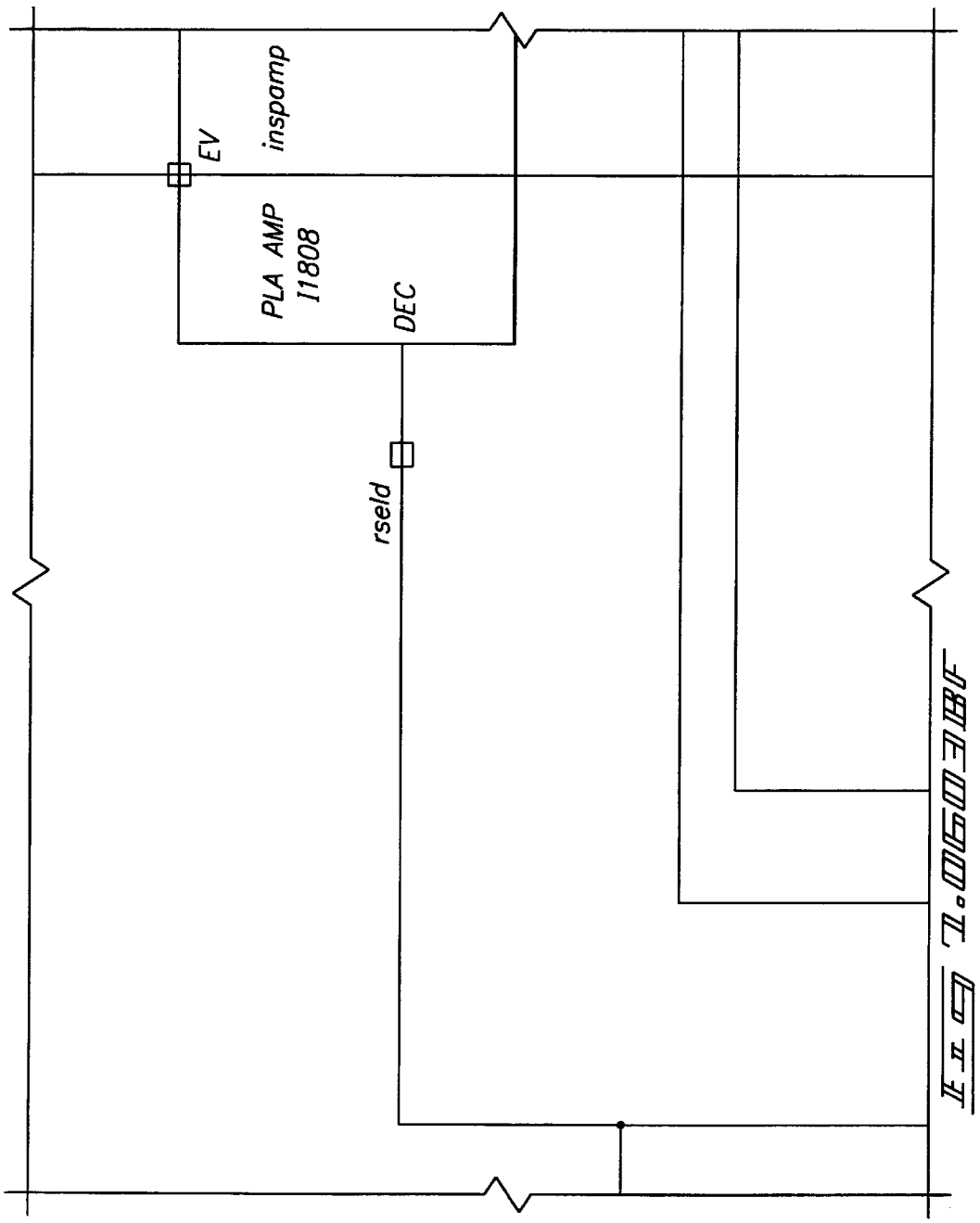
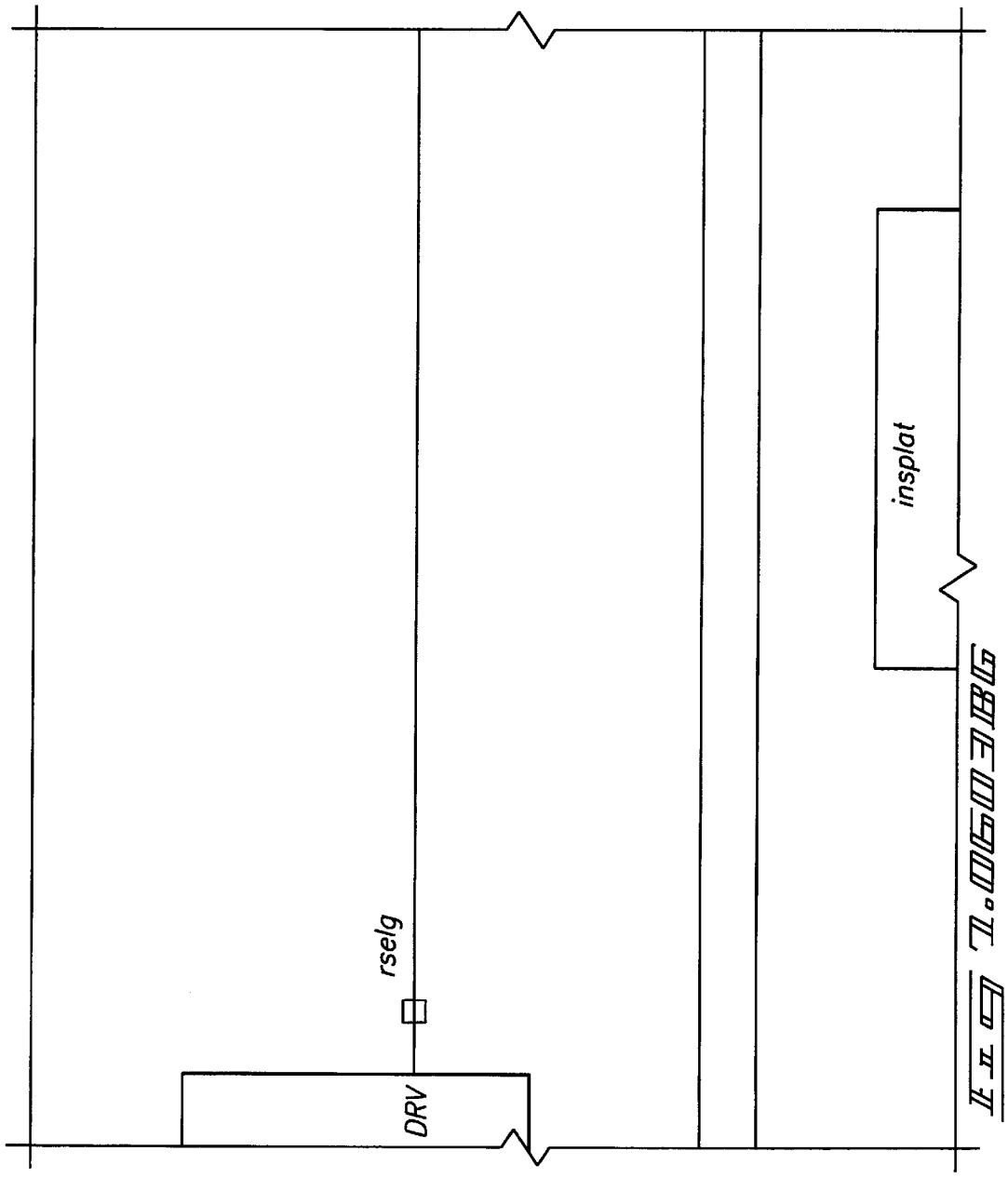


FIG. 652


S3
net229215
ldr:1u
wdr=8u
C1
net229215
8u/1u
M1871
"nch"
net229523
ldr:1u
wdr=8u
C2
net190584
ldr:1u
wdr=8u
net190199
8u/1u
M1816
"nch"
C2
net190516
ldr:1u
wdr=8u
net190190
8u/1u
M1818
"nch"


ADMAROD
8u/1u
M1817
"nch"
S1
net190199
ldr:1u
wdr=8u
S2
rseld
8u/1u
M1819
"nch"
ADMAROD
8u/1u
M1861
"nch"
net190190
ldr:1u
wdr=8u


EV
inspamp
PLA AMP
11808
DEC
rseld
FIG. 655A


insplat
rselg
DRV

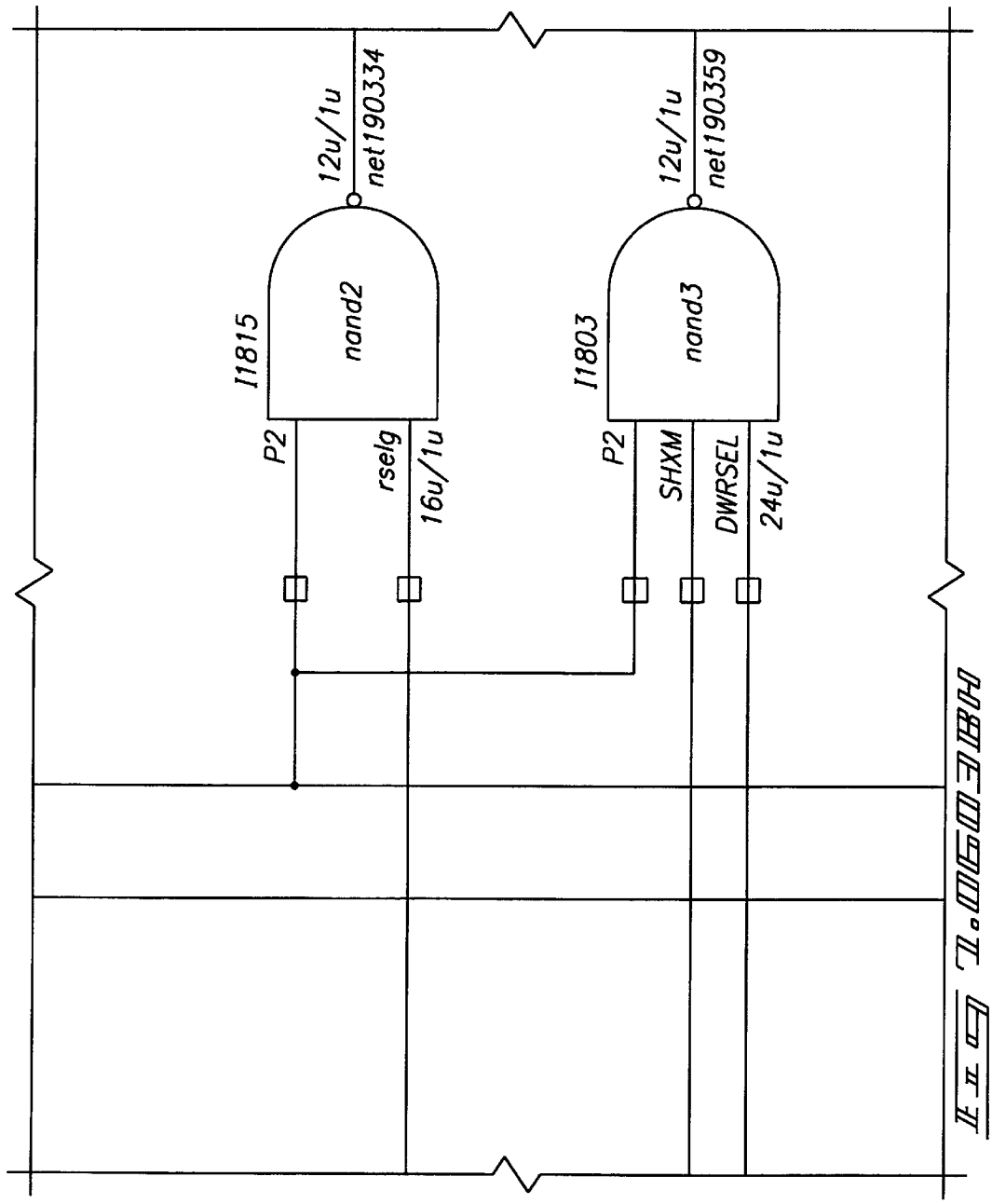

12u/1u
net190334
12u/1u
net190359
I1815
nand2
I1803
nand3
P2
rselg
16u/1u
P2
SHXM
DWRSEL
24u/1u

FIG. 659

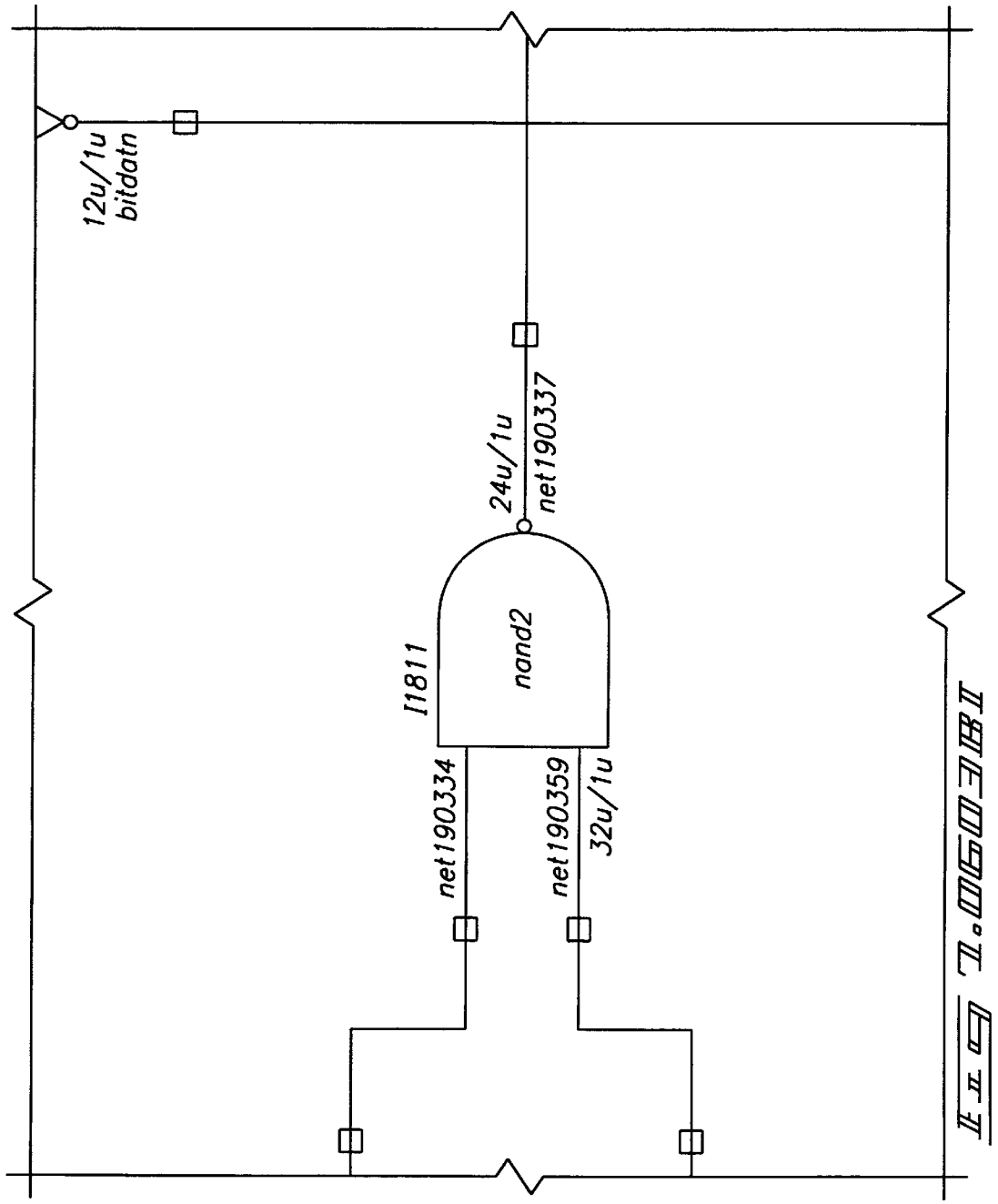
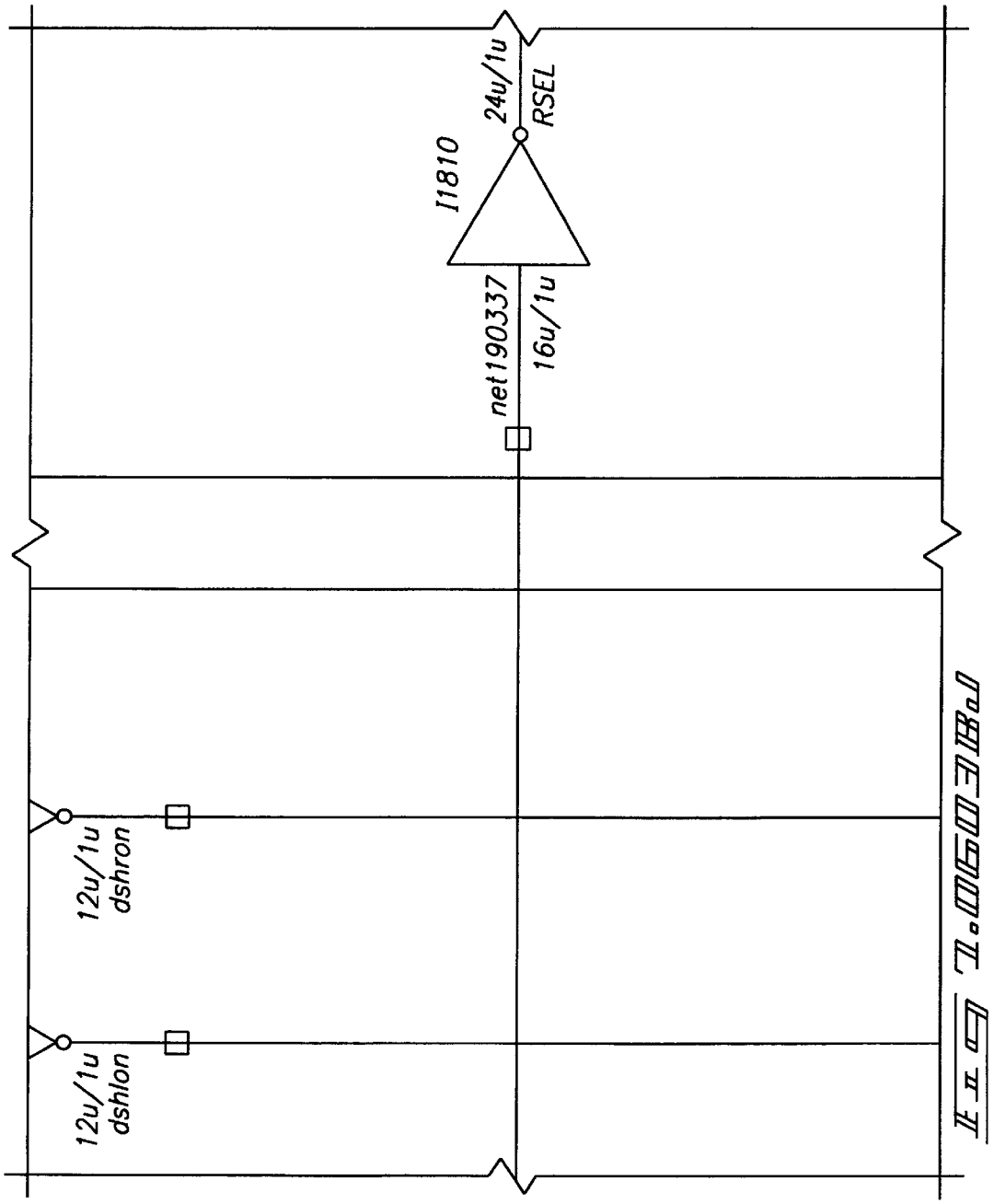
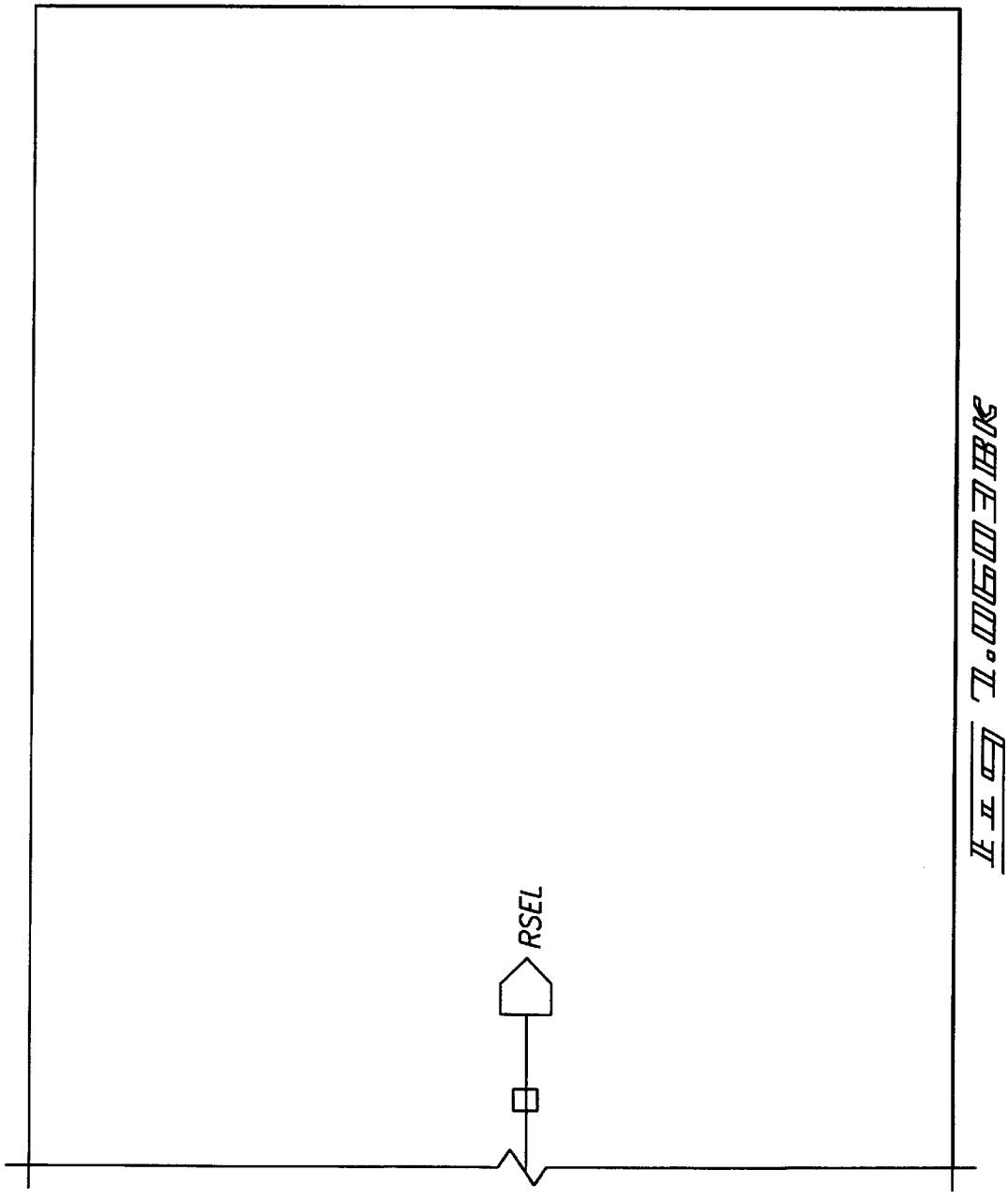
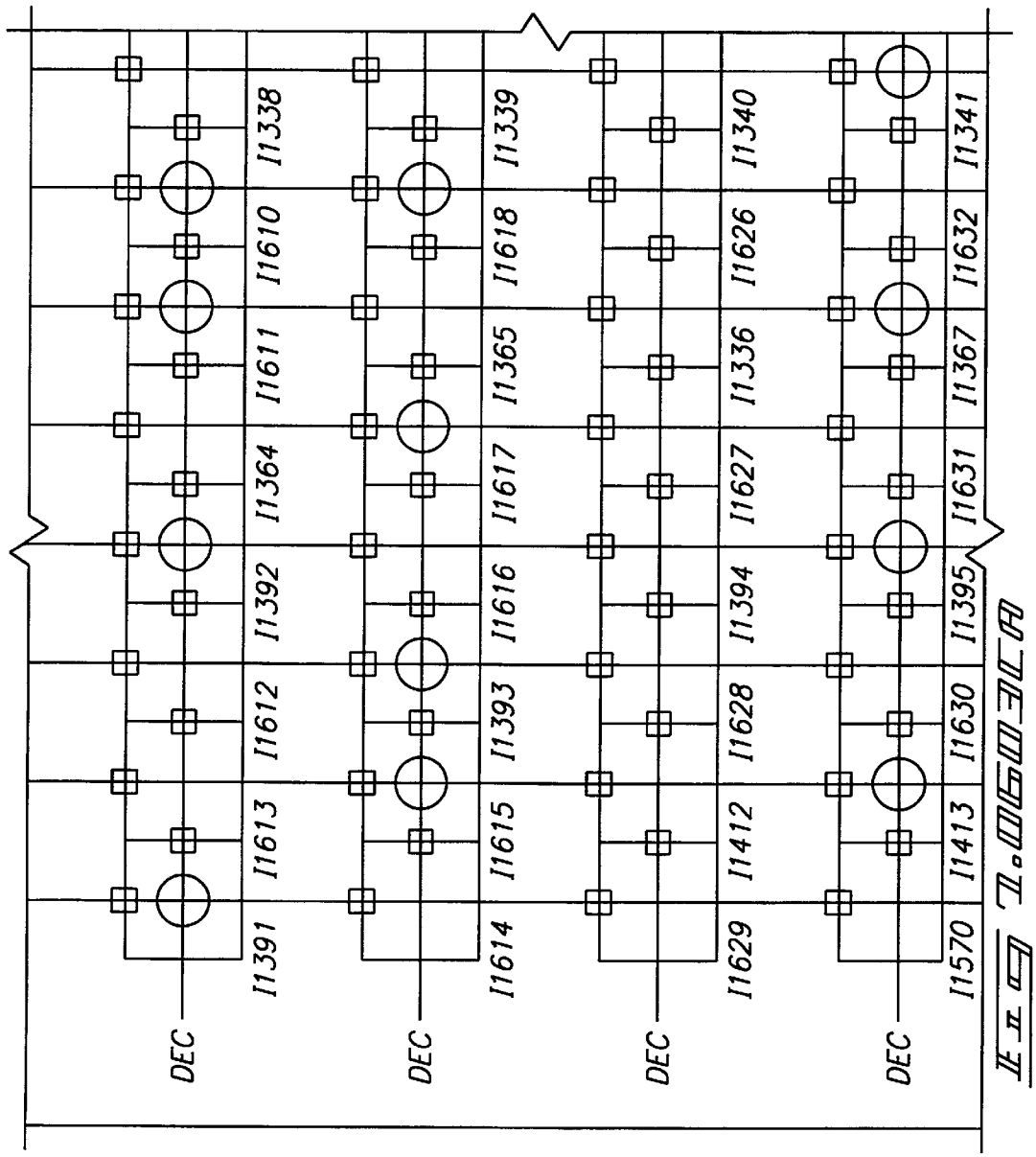
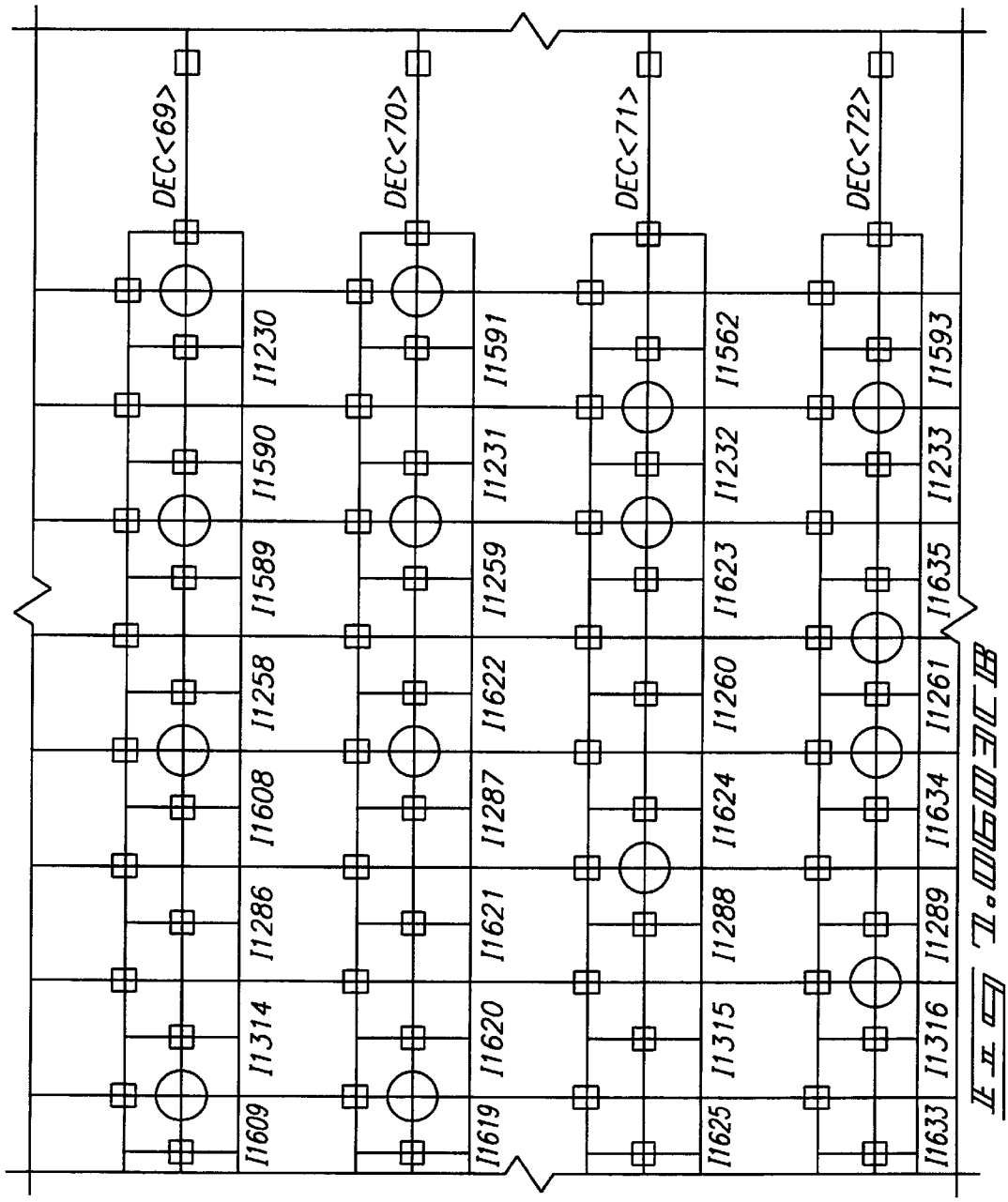

12u/1u
bitdatn
24u/1u
net190337
I1811
nand2
net190334
net190359
32u/1u

FIG. 1BE05M.L


I1810
24u/1u
RSEL
net190337
16u/1u
12u/1u
dshron
12u/1u
dshlon
FIG. 659


RSEL
FIG. 605.11


DEC
DEC
DEC
DEC
I1391
I1613
I1612
I1392
I1364
I1611
I1610
I1338
I1614
I1615
I1393
I1616
I1617
I1365
I1618
I1339
I1629
I1412
I1628
I1394
I1627
I1336
I1626
I1340
I1570
I1413
I1630
I1395
I1631
I1367
I1632
I1341
FIG. 1163


DEC<69>
DEC<70>
DEC<71>
DEC<72>
I1230
I1590
I1589
I1258
I1608
I1286
I1314
I1609
I1591
I1231
I1259
I1622
I1287
I1621
I1620
I1619
I1562
I1232
I1623
I1260
I1624
I1288
I1315
I1625
I1593
I1233
I1635
I1261
I1634
I1289
I1316
I1633
БЛОК ДЕКОДЕРА

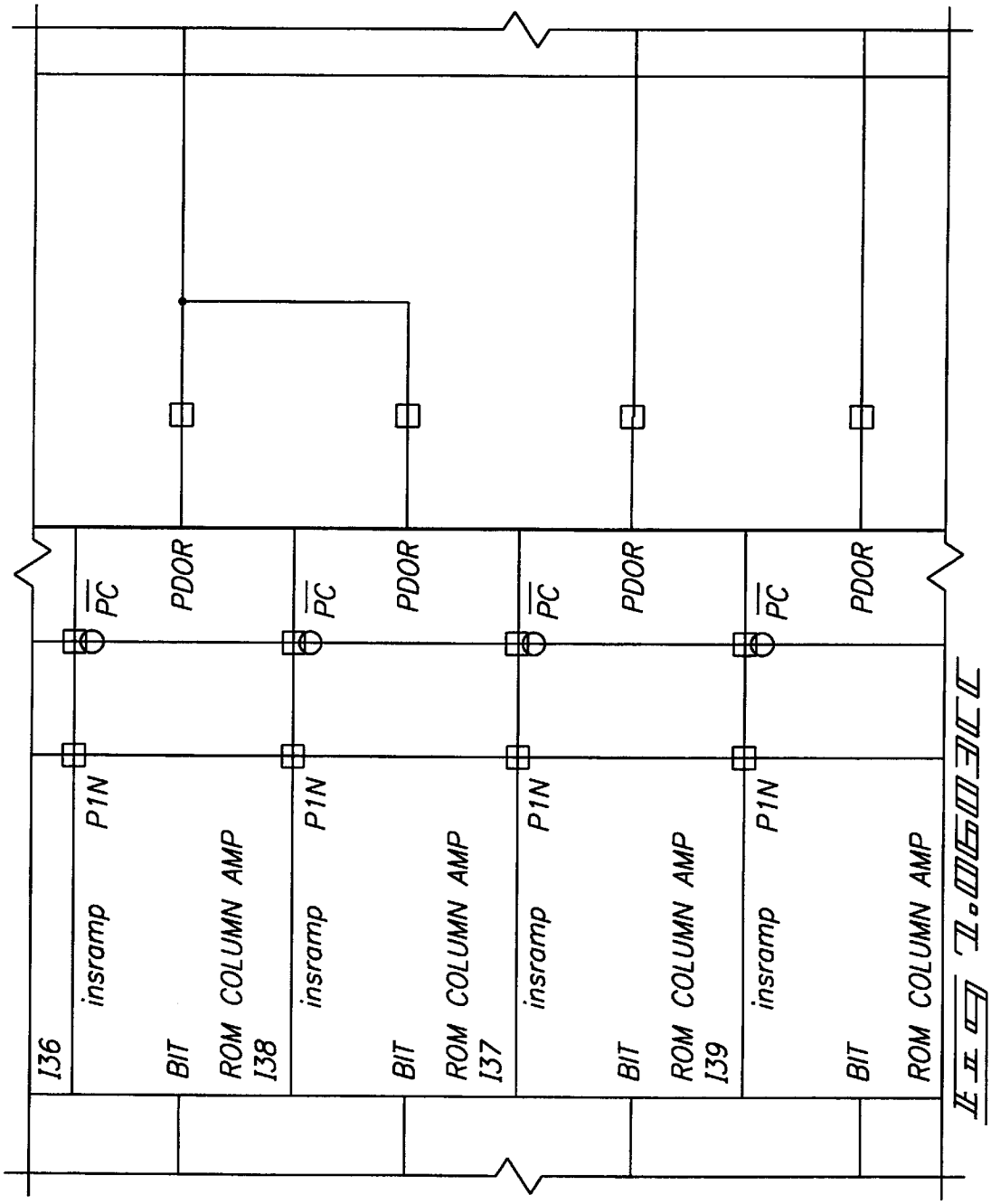
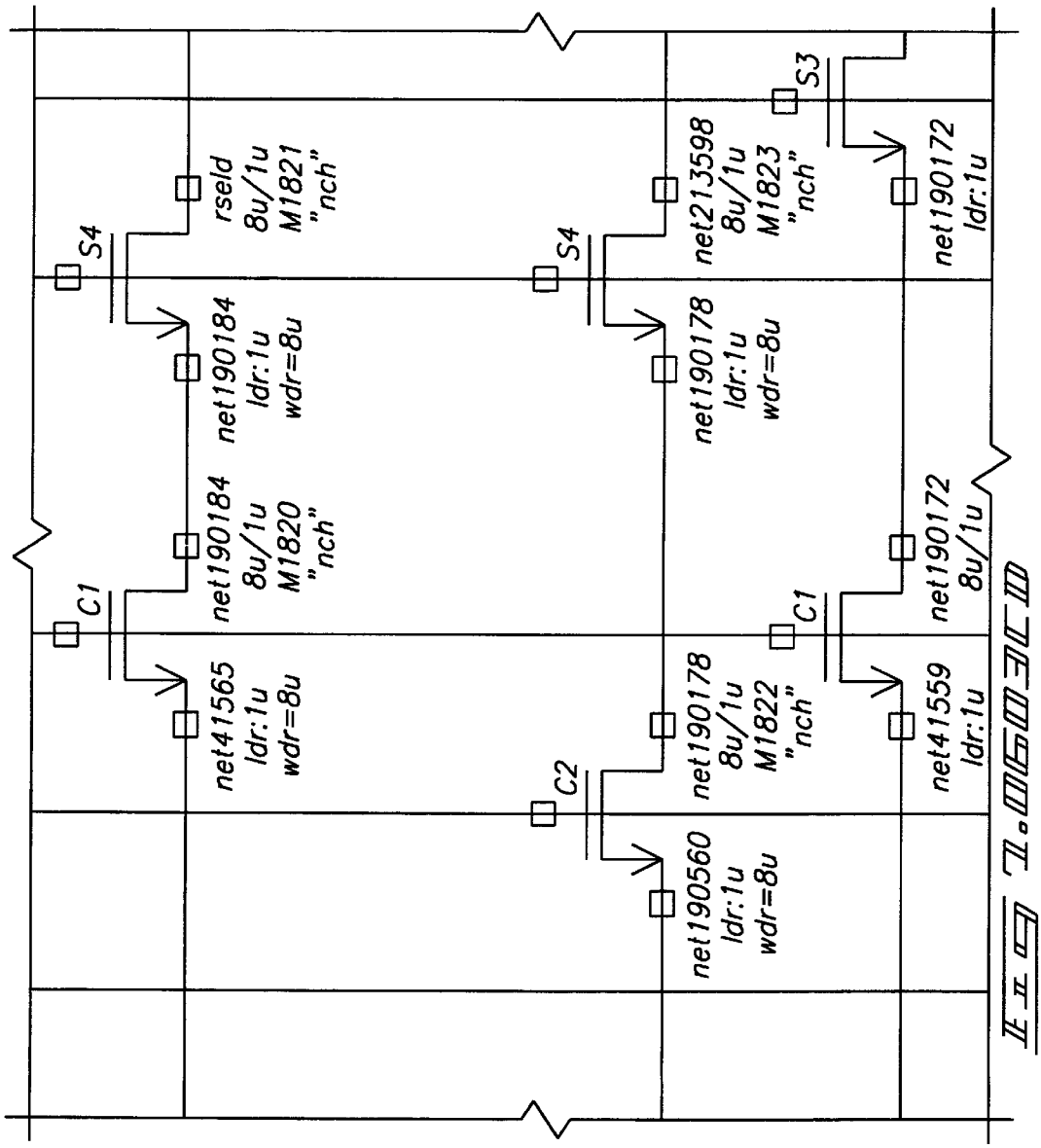

136
BIT
ROM COLUMN AMP
I38
insramp
P1N
PDOR
$\overline{PC}$
BIT
ROM COLUMN AMP
I37
insramp
P1N
PDOR
$\overline{PC}$
BIT
ROM COLUMN AMP
I39
insramp
P1N
PDOR
$\overline{PC}$
BIT
ROM COLUMN AMP
insramp
P1N
PDOR
$\overline{PC}$

FIG. 638


S4
rseld
8u/1u
M1821
"nch"
net190184
ldr:1u
wdr=8u
net190184
8u/1u
M1820
"nch"
C1
net41565
ldr:1u
wdr=8u
S4
net213598
8u/1u
M1823
"nch"
net190178
ldr:1u
wdr=8u
net190178
8u/1u
M1822
"nch"
C2
net190560
ldr:1u
wdr=8u
S3
net190172
ldr:1u
net190172
8u/1u
C1
net41559
ldr:1u

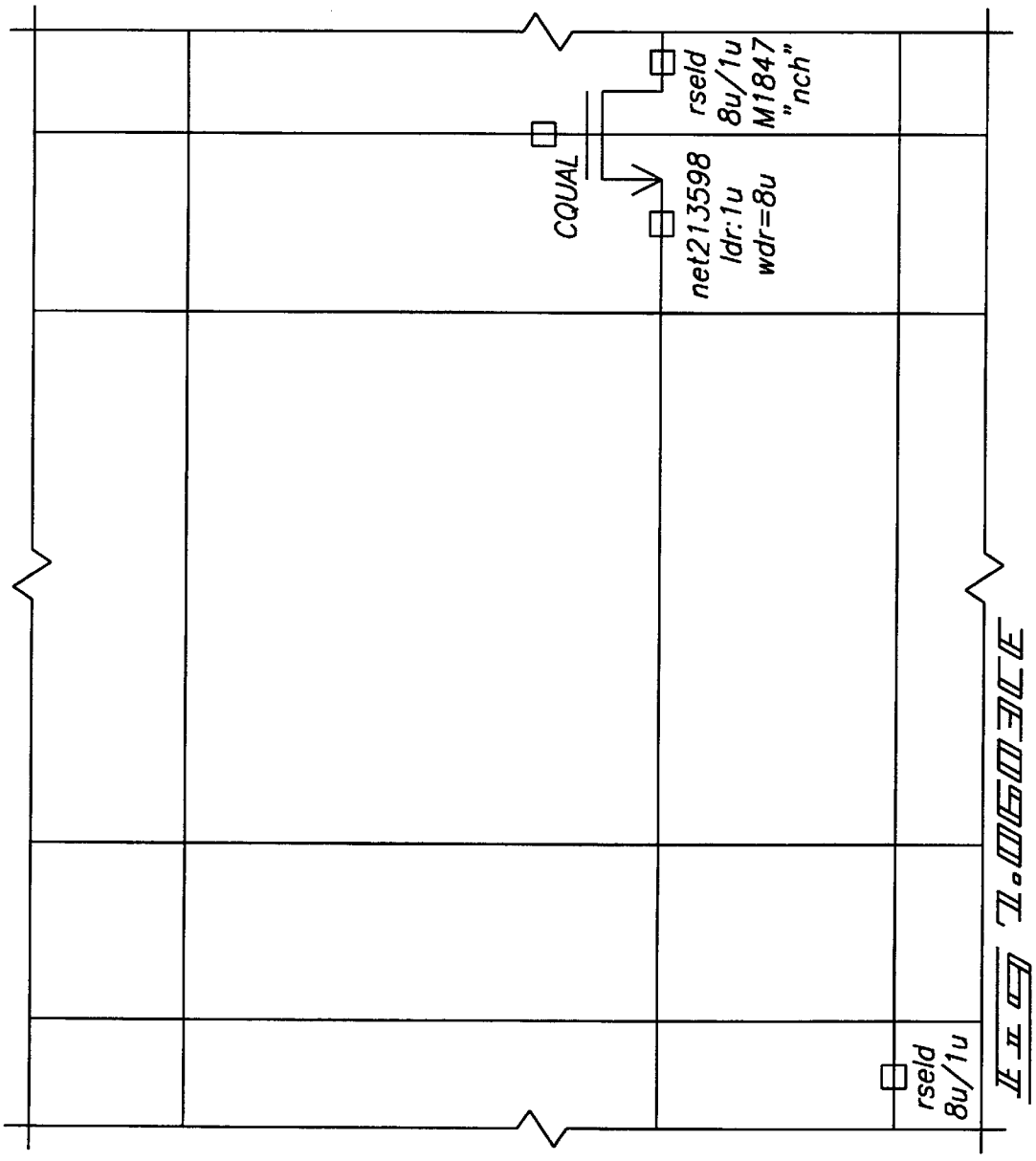
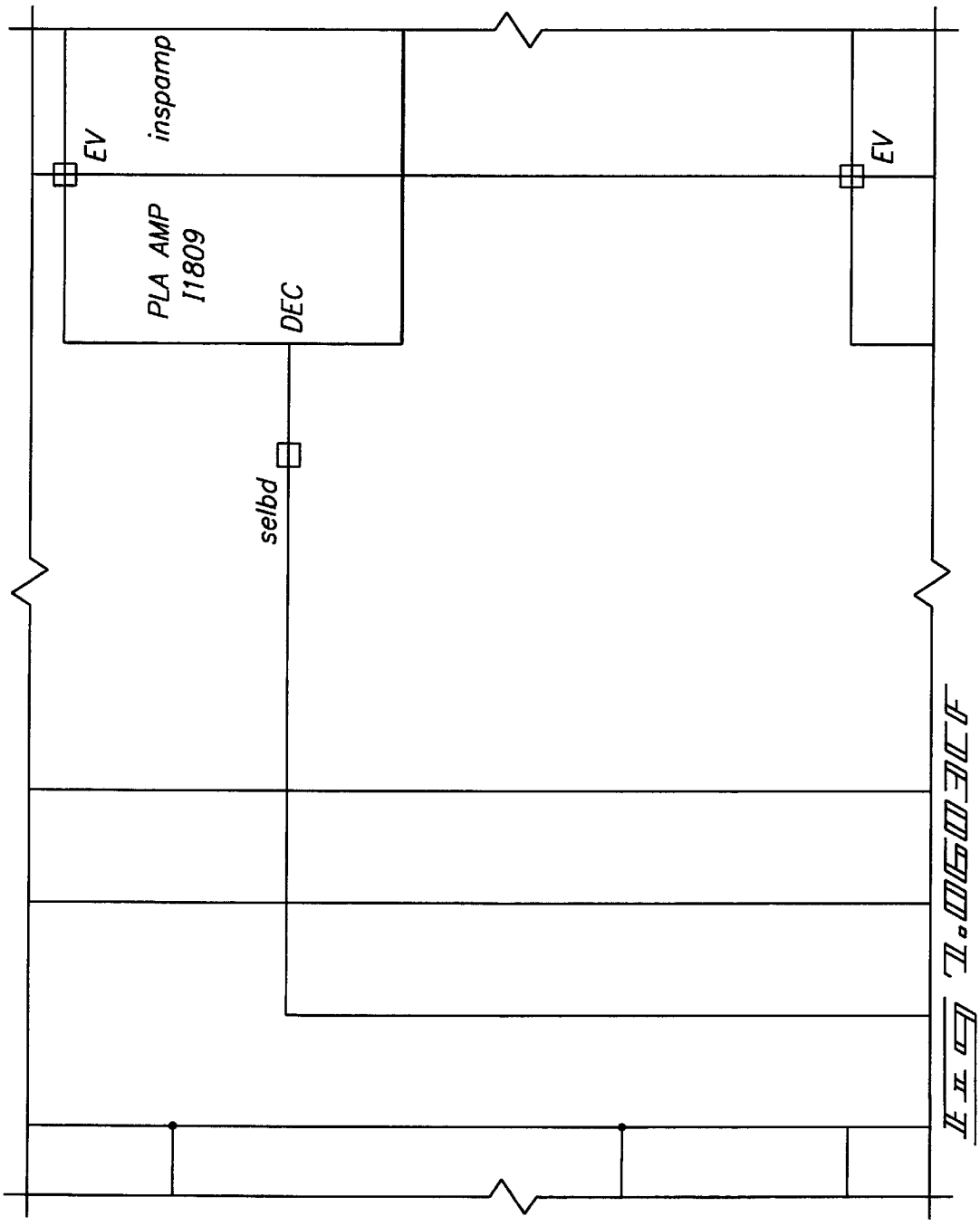

rseld
8u/1u
M1847
"nch"
CQUAL
net213598
ldr:1u
wdr=8u
rseld
8u/1u

FIG 605.7E


EV
inspamp
EV
PLA AMP
I1809
DEC
selbd

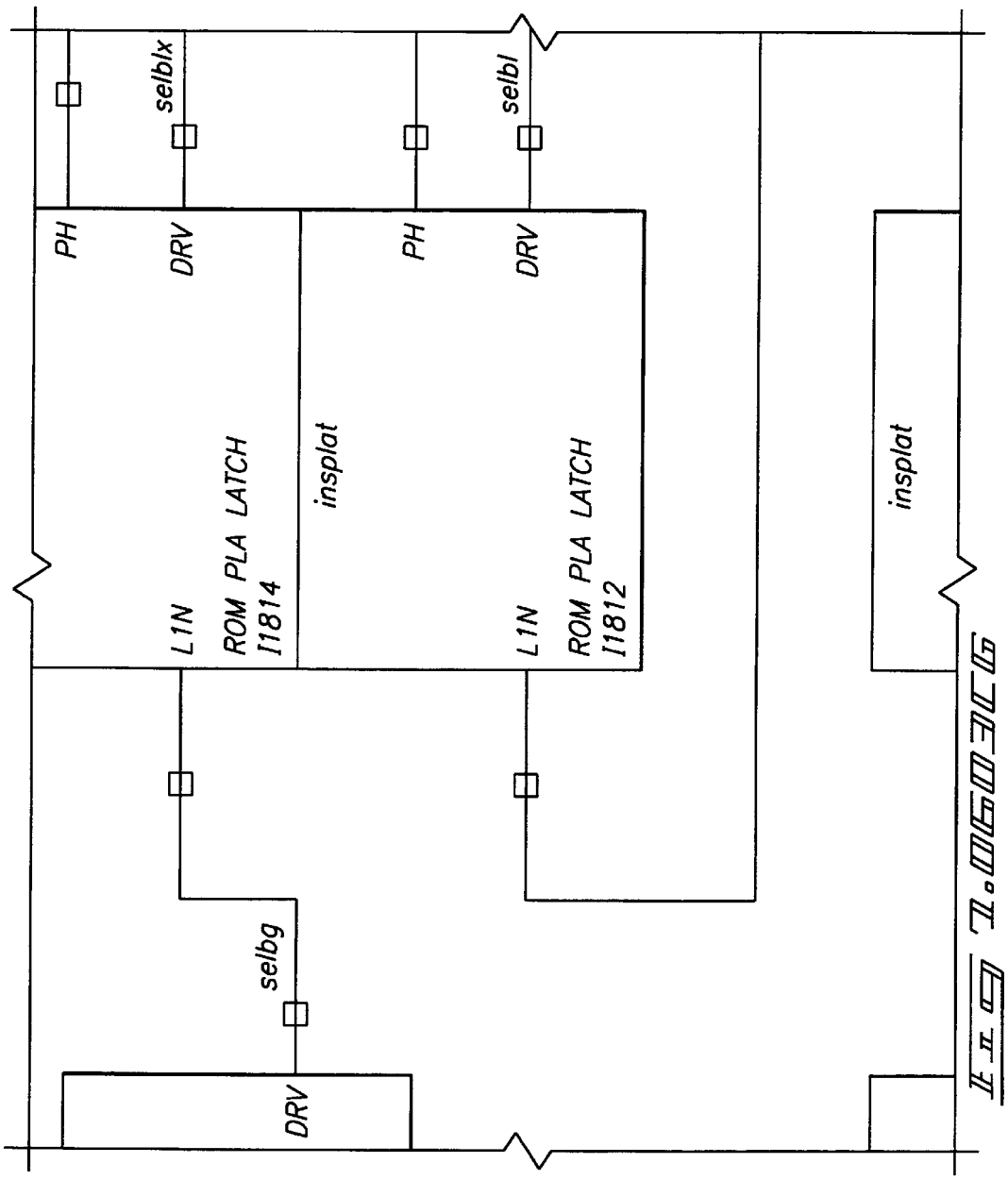
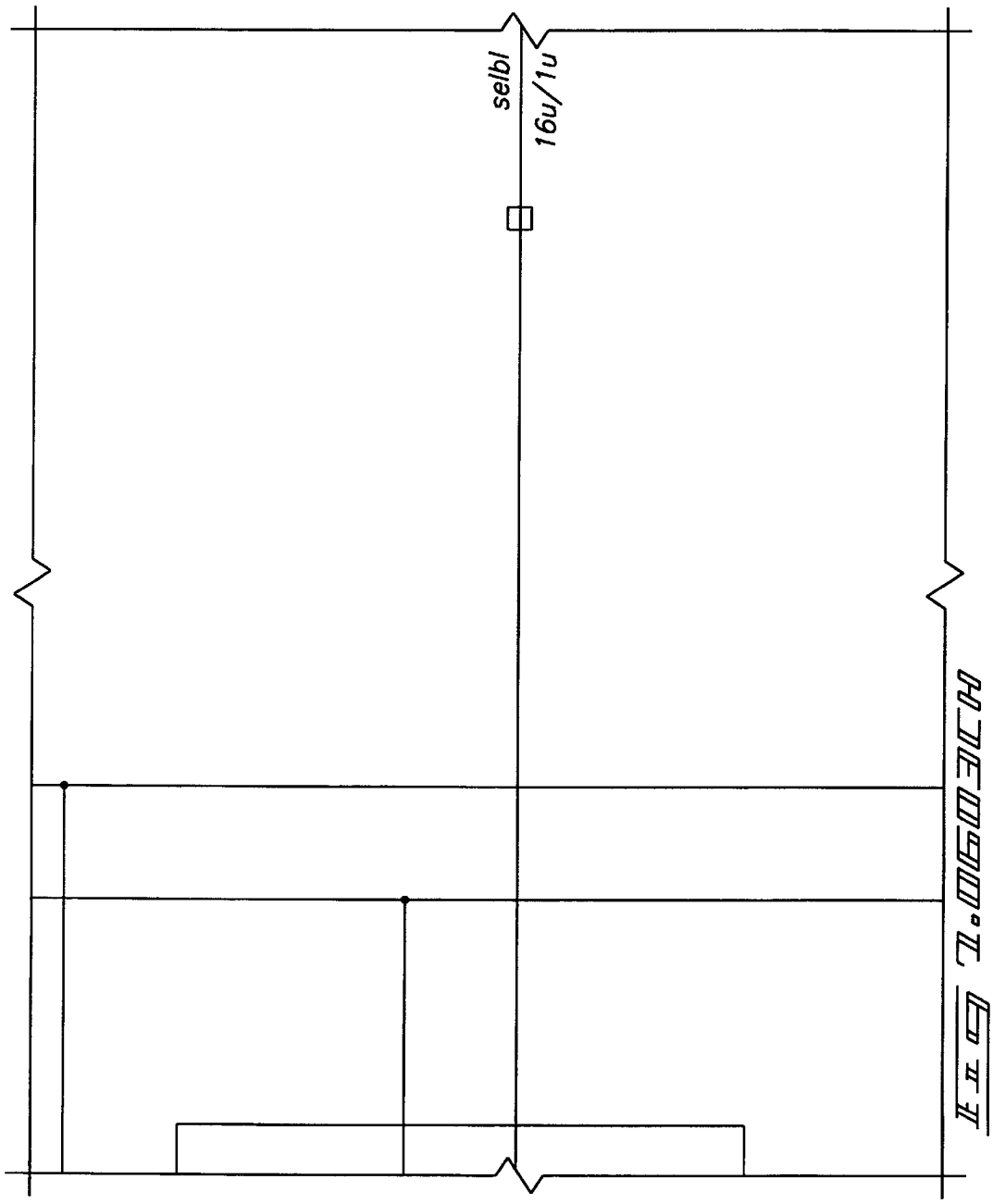
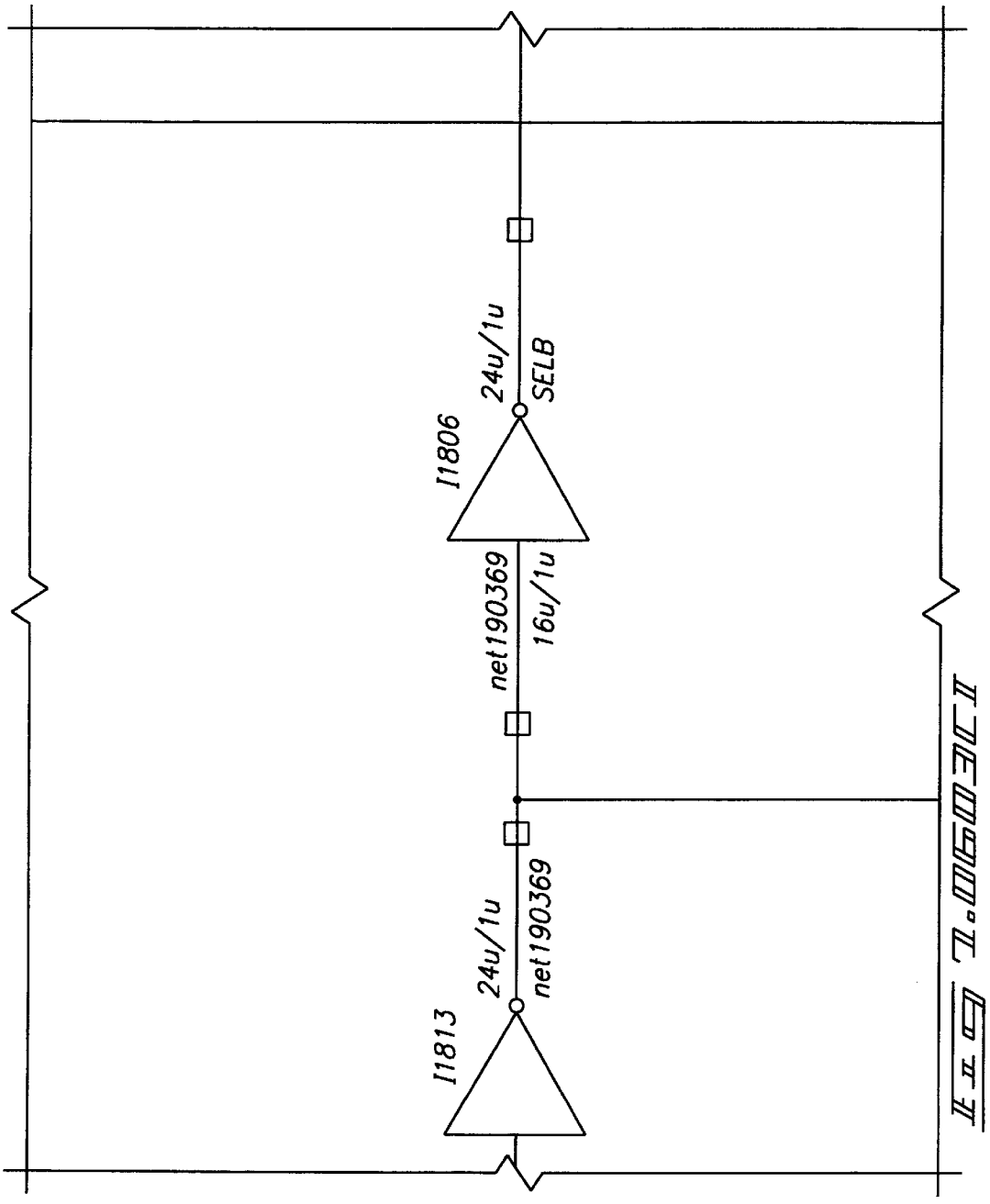
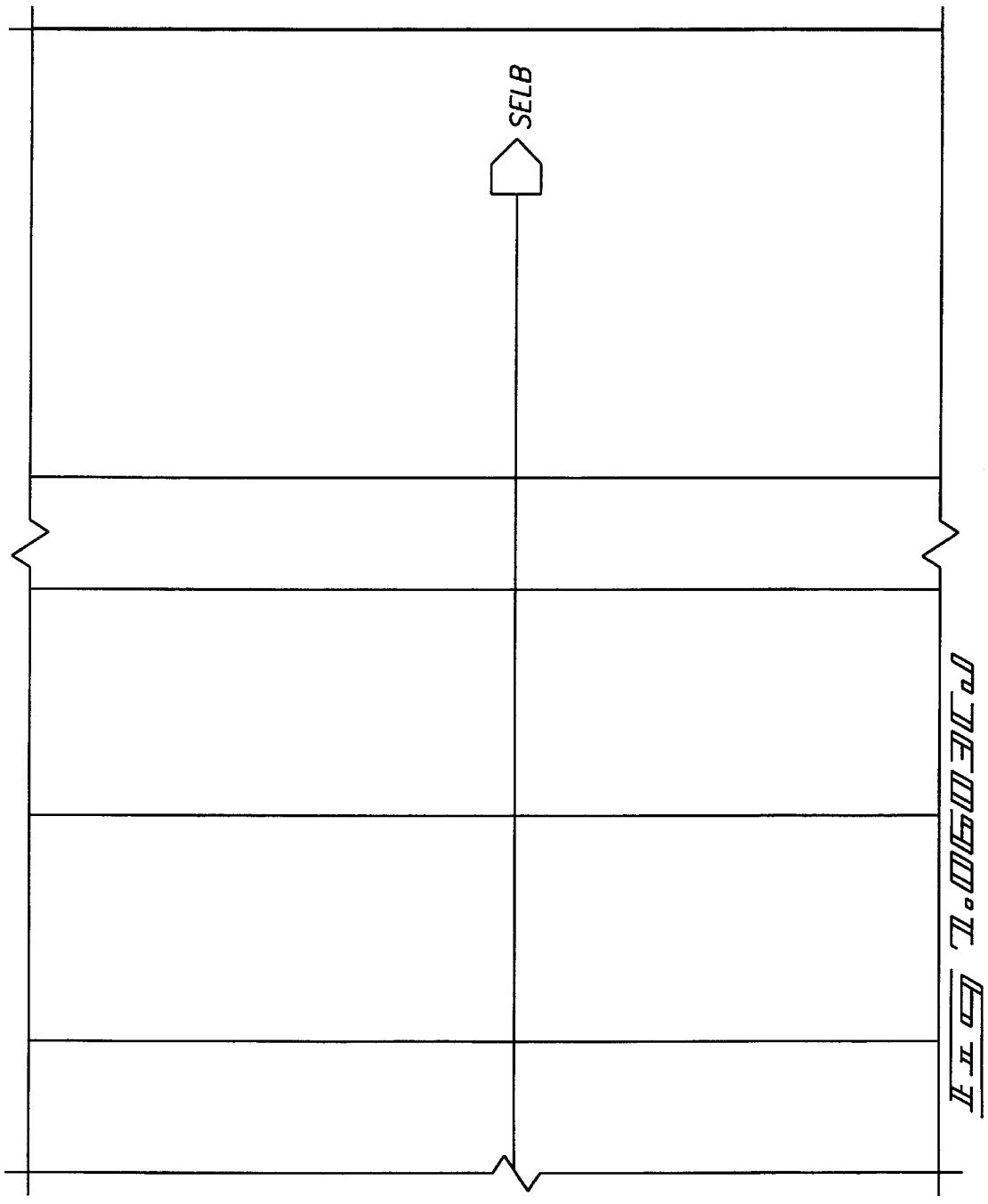

selblx
selbl
PH
DRV
PH
DRV
insplat
L1N
ROM PLA LATCH
I1814
L1N
ROM PLA LATCH
I1812
insplat
selbg
DRV

FIG 59E.1


selbl
16u/1u
FIG. 5


I1806
24u/1u
SELB
net190369
16u/1u
I1813
24u/1u
net190369
VDD!


SELB
FIG 5900.1

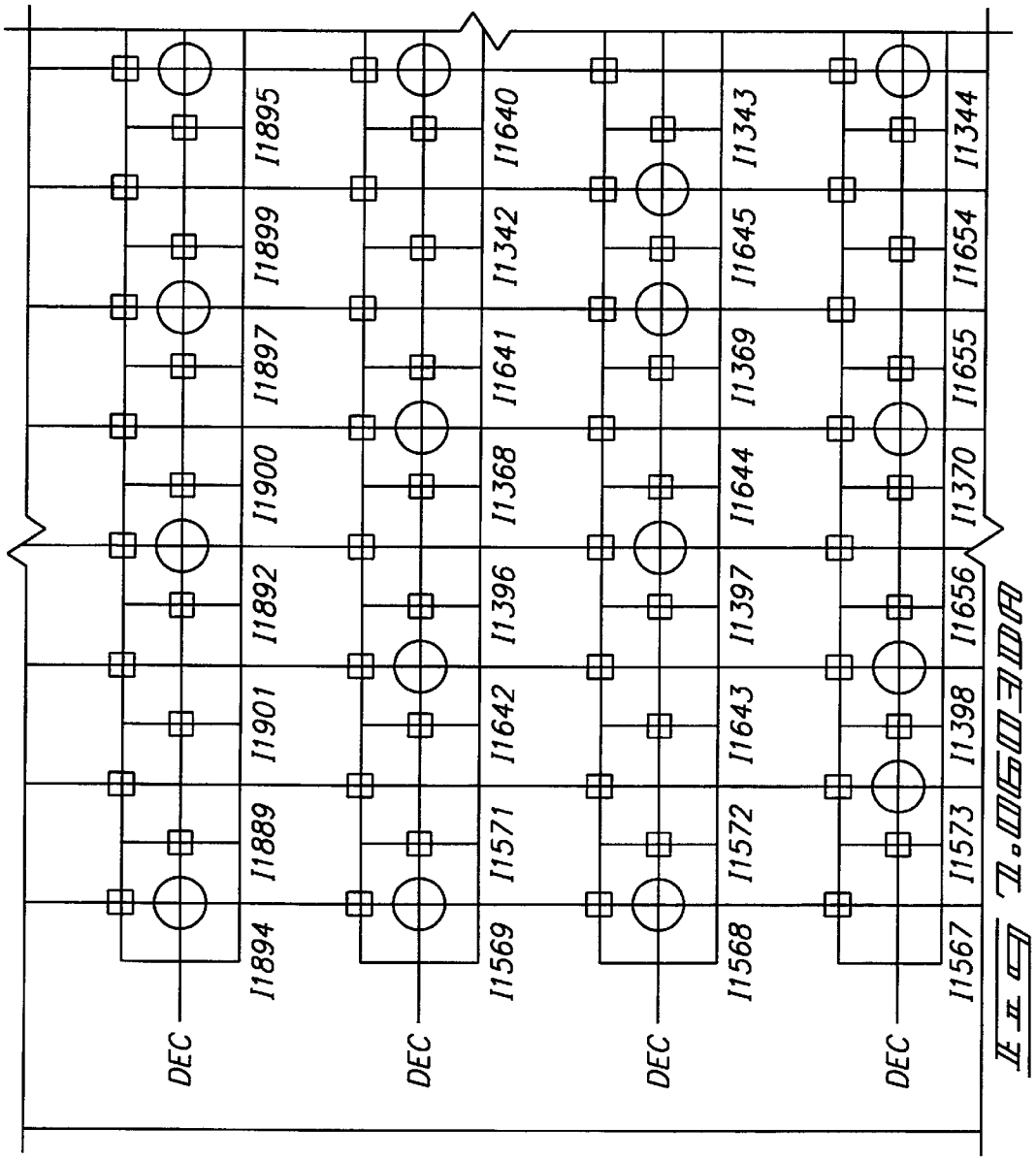
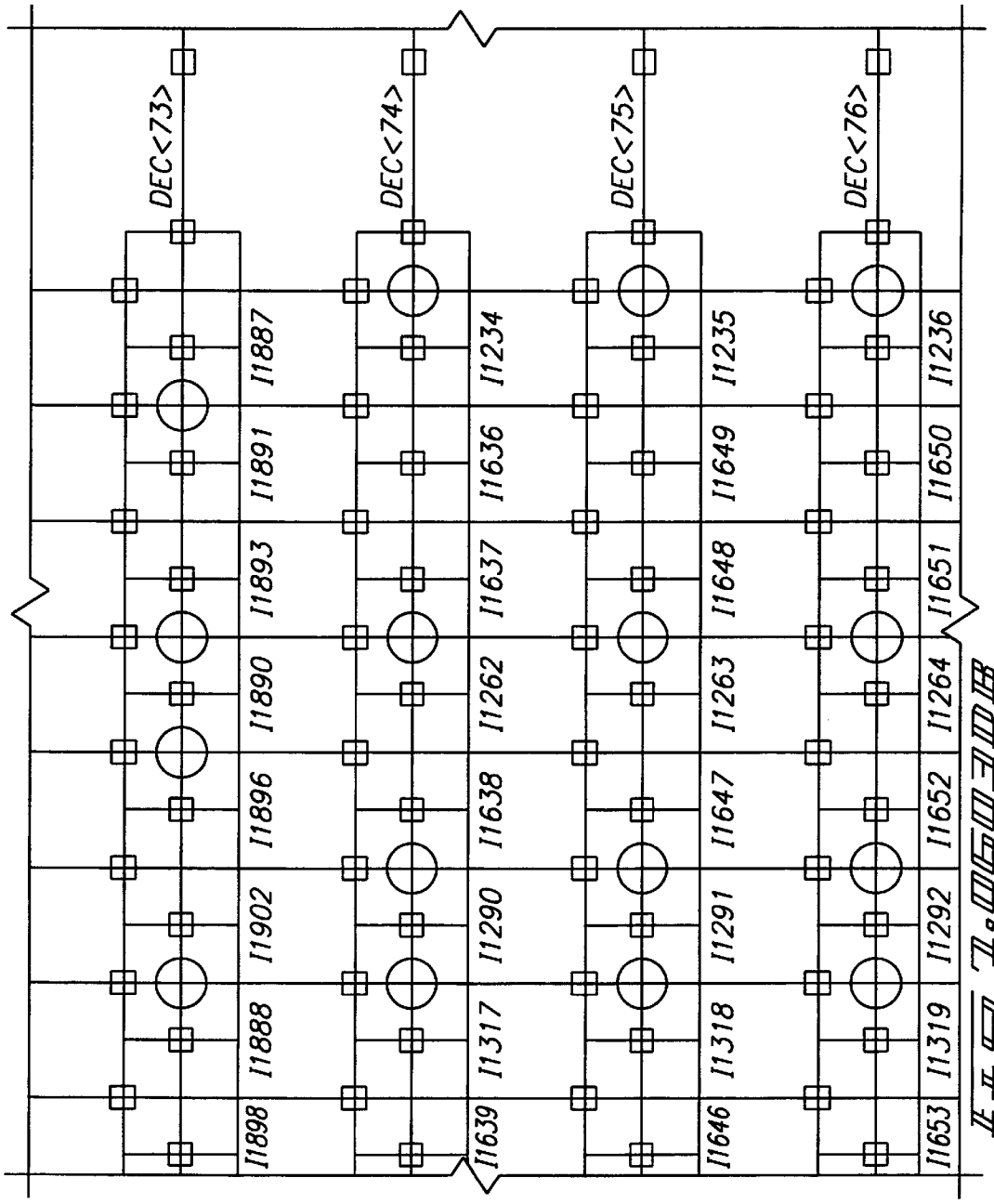

DEC
DEC
DEC
DEC
I1894
I1889
I1901
I1892
I1900
I1897
I1899
I1895
I1569
I1571
I1642
I1396
I1368
I1641
I1342
I1640
I1568
I1572
I1643
I1397
I1644
I1369
I1645
I1343
I1567
I1573
I1398
I1656
I1370
I1655
I1654
I1344

FIG. 671


DEC<73>
DEC<74>
DEC<75>
DEC<76>
I1887
I1891
I1893
I1890
I1896
I1902
I1888
I1898
I1234
I1636
I1637
I1262
I1638
I1290
I1317
I1639
I1235
I1649
I1648
I1263
I1647
I1291
I1318
I1646
I1236
I1650
I1651
I1264
I1652
I1292
I1319
I1653

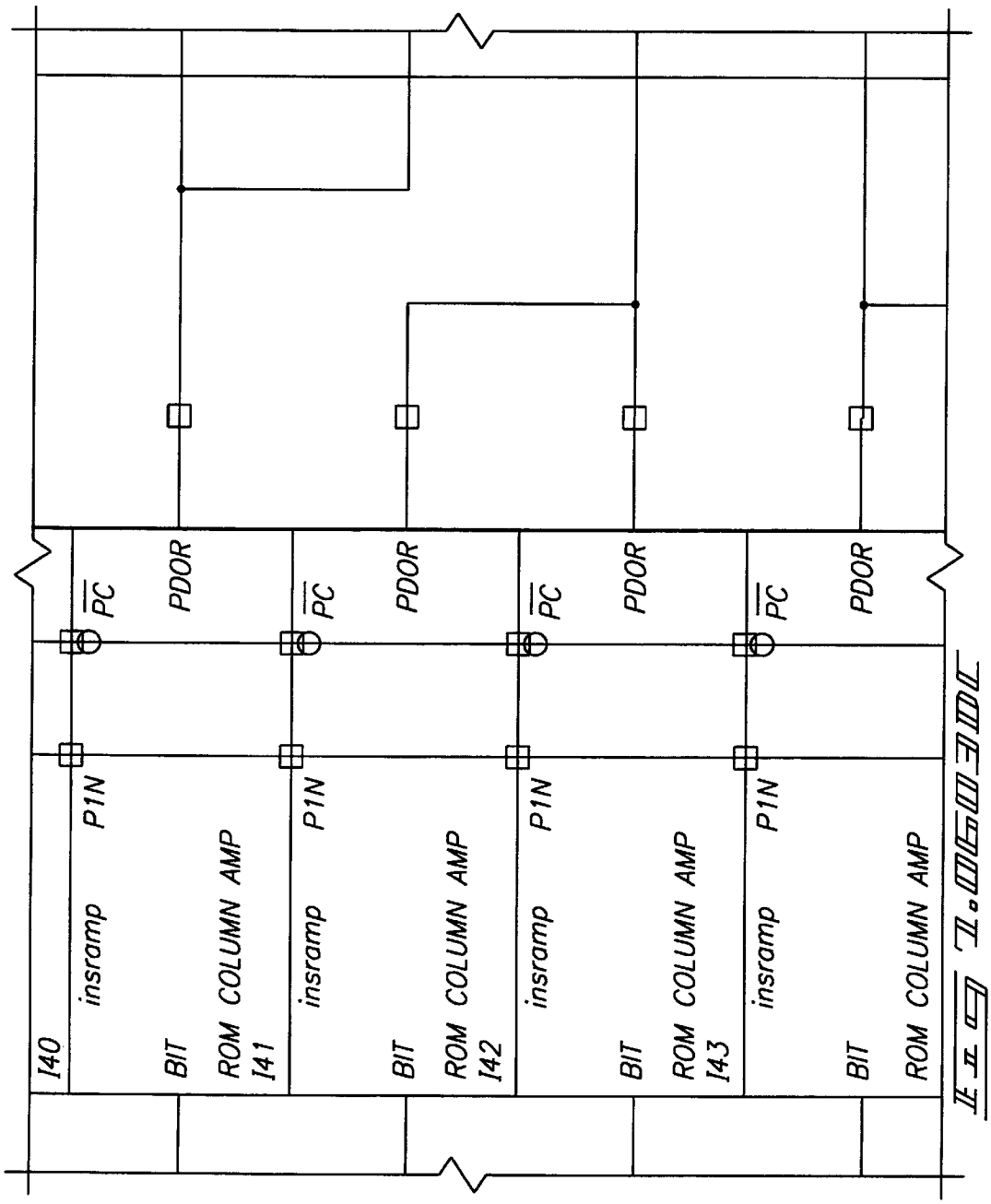
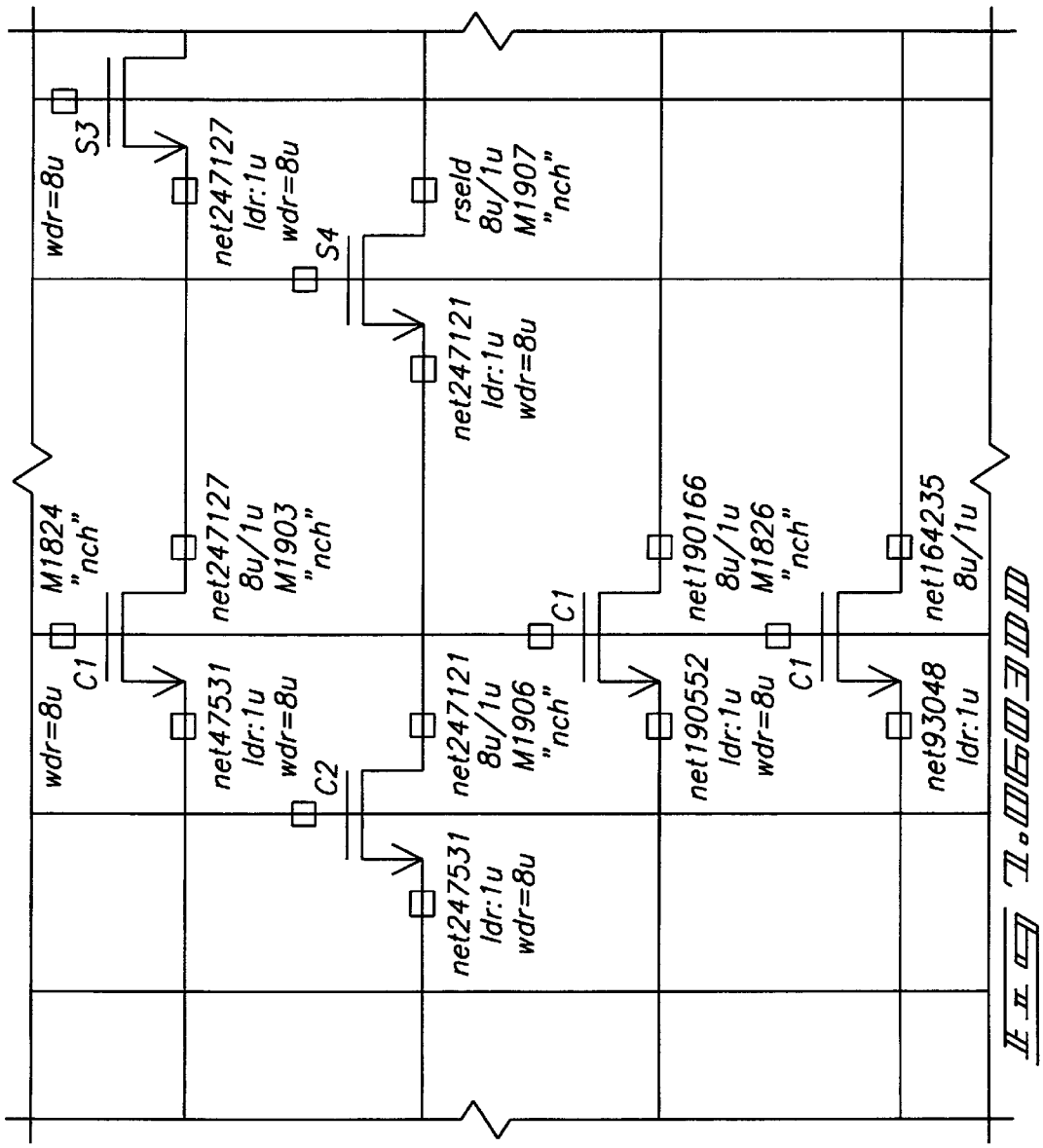
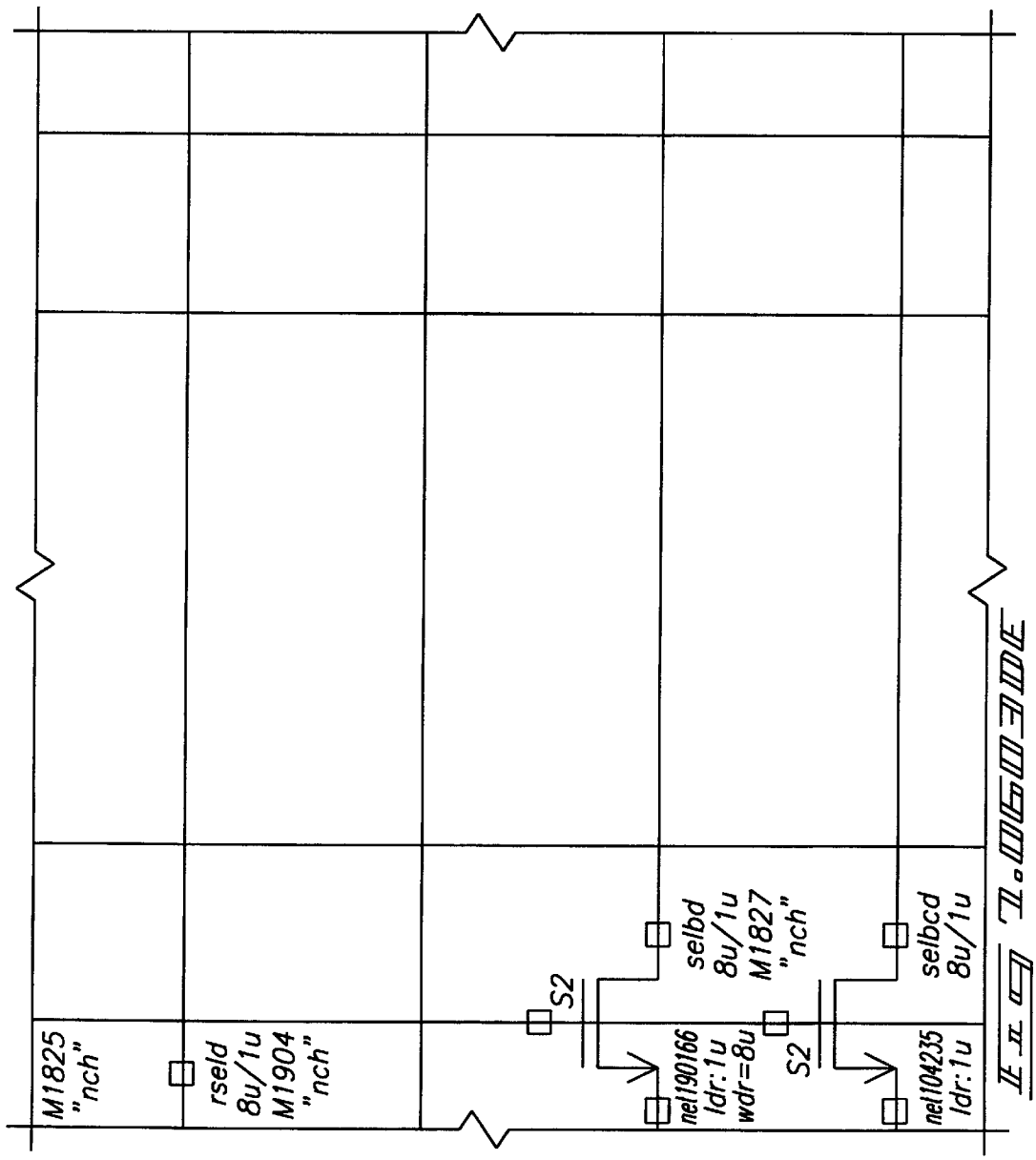
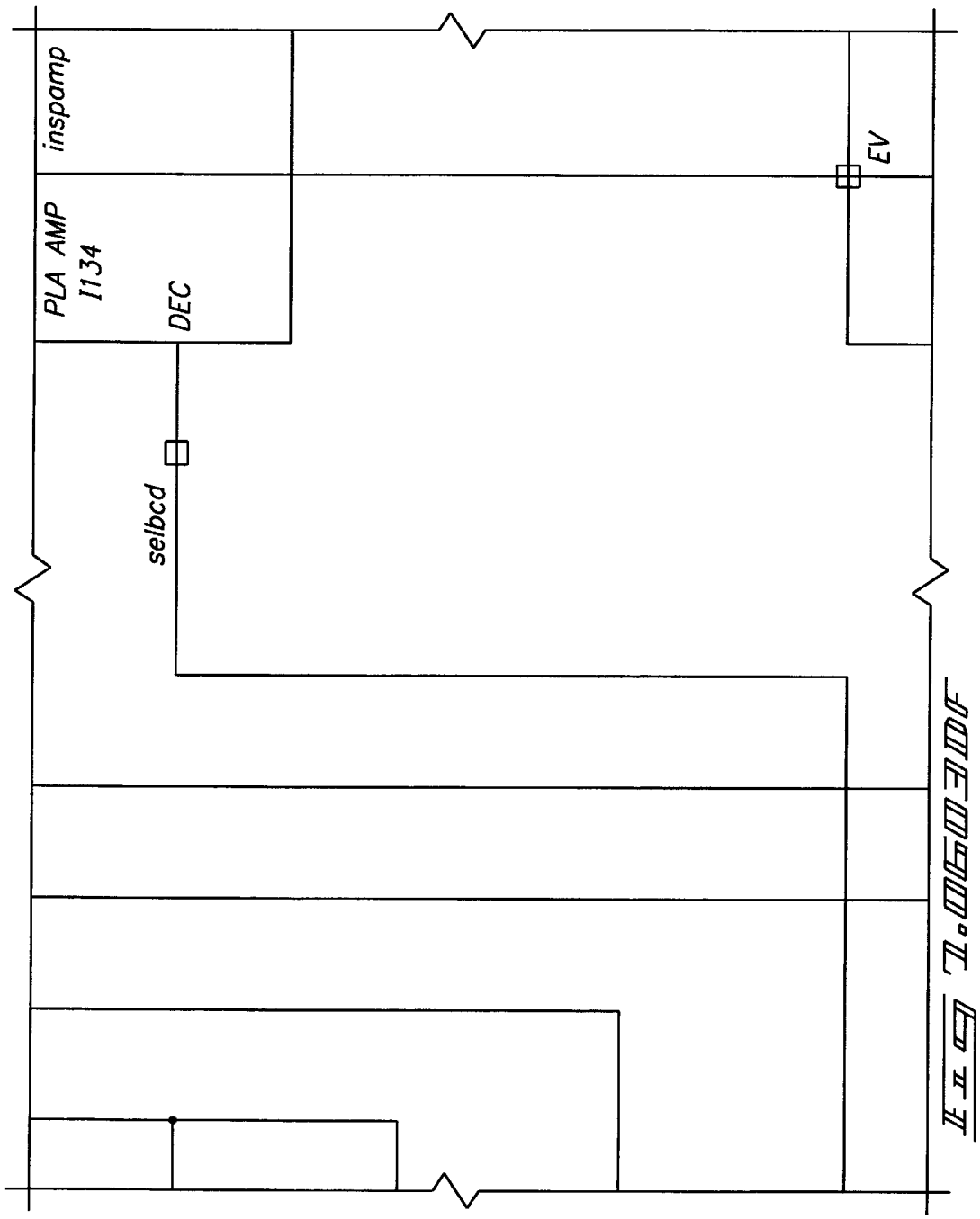
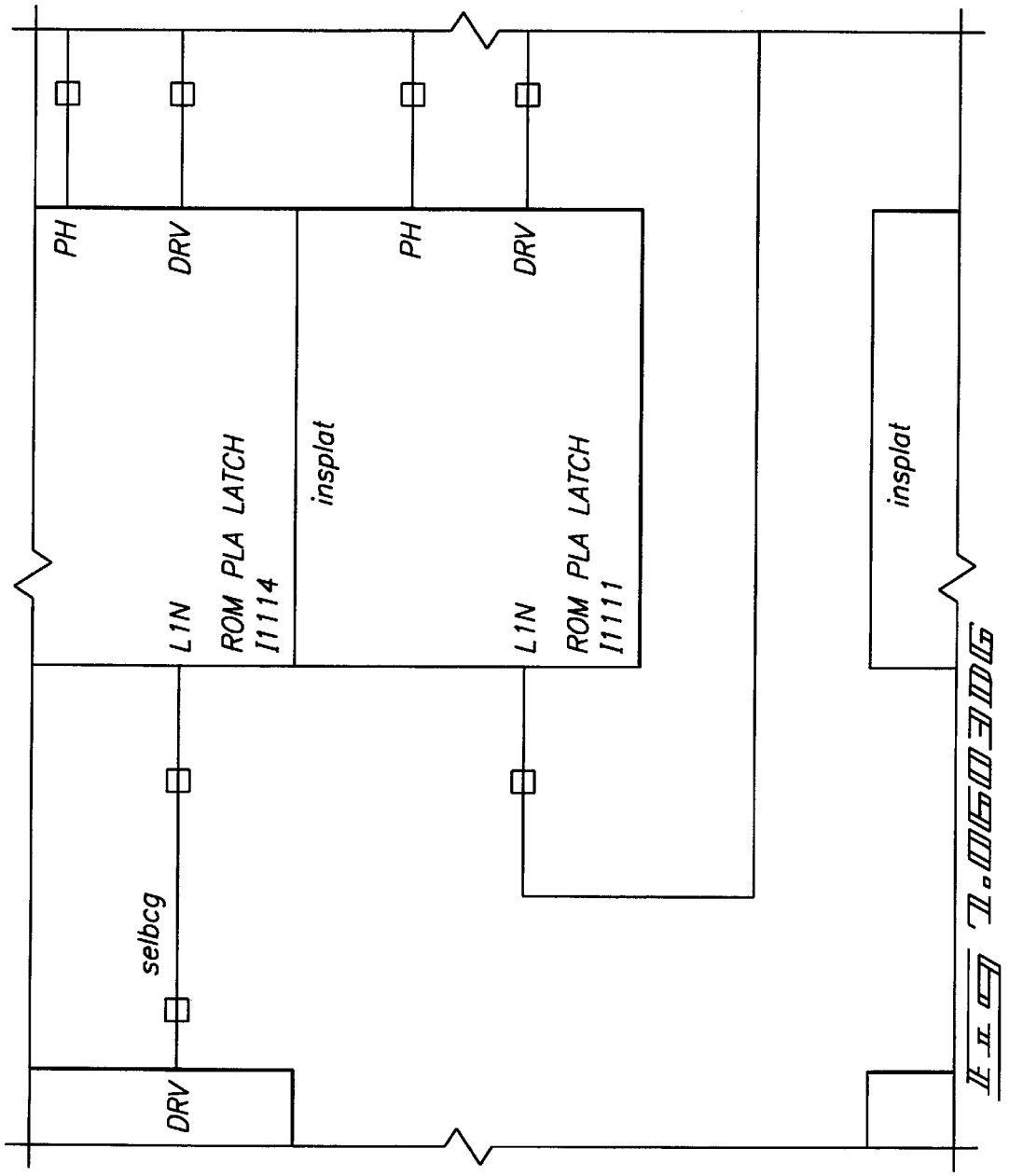

I40
BIT
ROM COLUMN AMP
I41
BIT
ROM COLUMN AMP
I42
BIT
ROM COLUMN AMP
I43
BIT
ROM COLUMN AMP
insramp
P1N
PC
PDOR

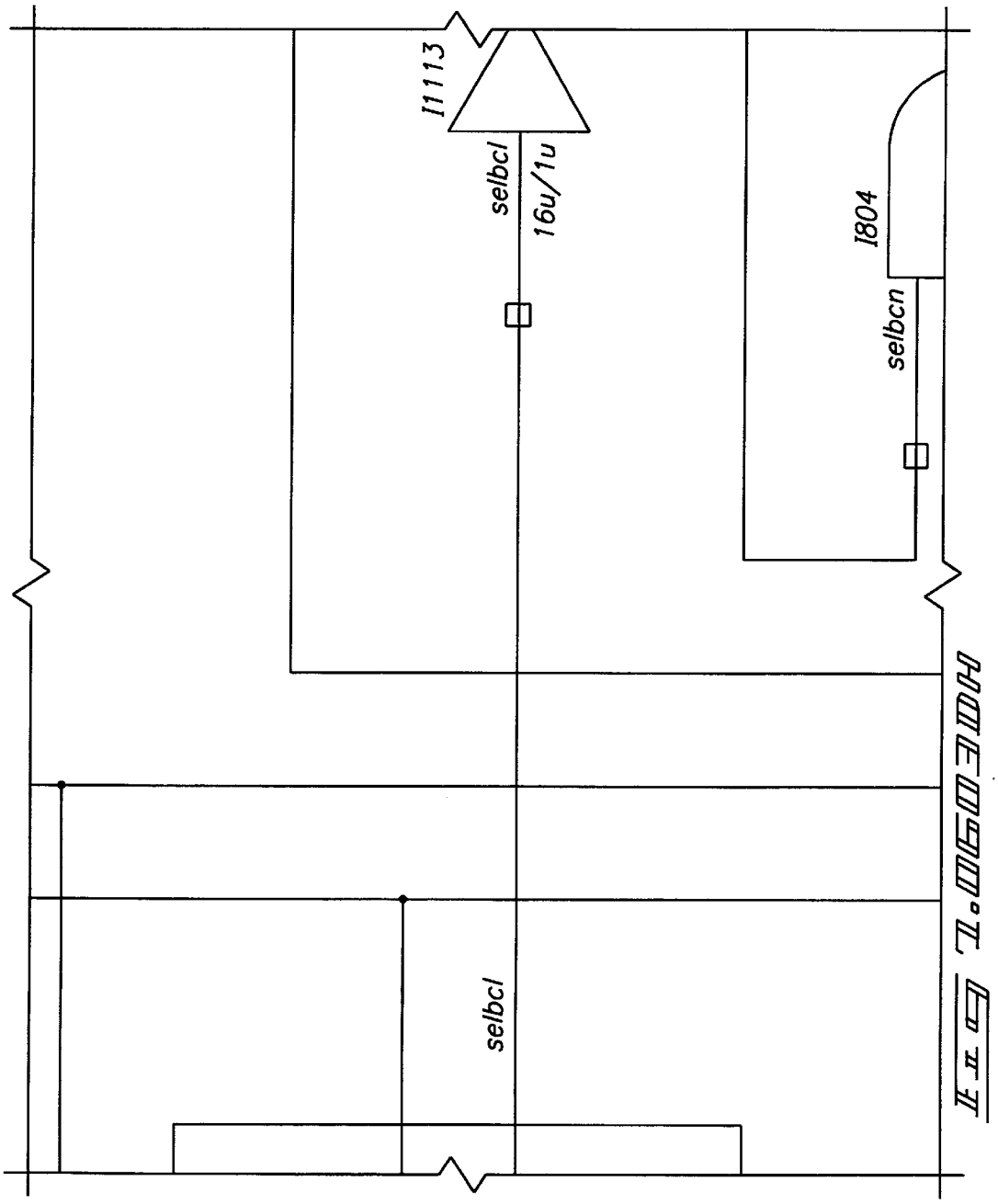
FIG. 673.

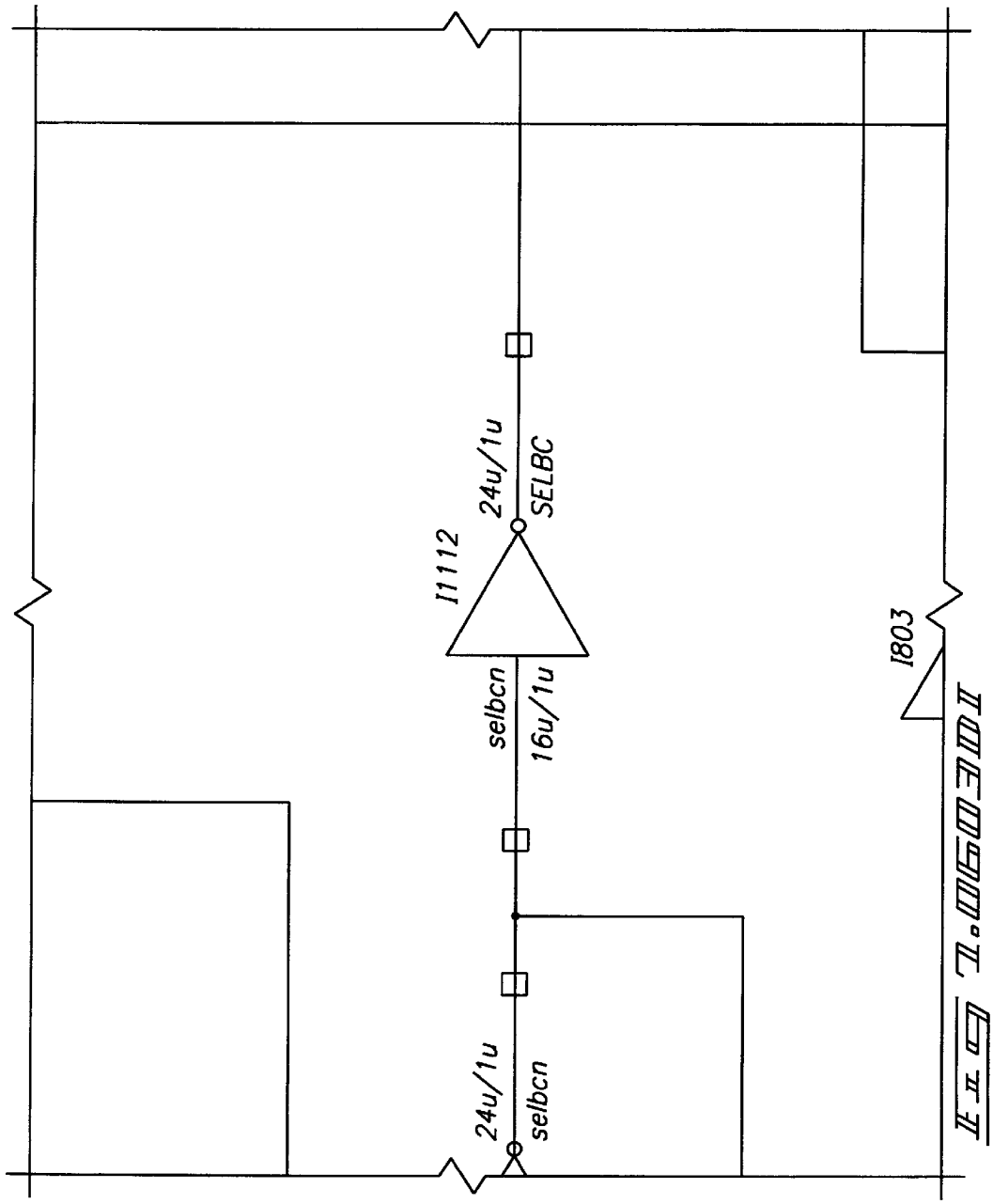

wdr=8u
S3
net247127
ldr:1u
wdr=8u
S4
rseld
8u/1u
M1907
"nch"
net247121
ldr:1u
wdr=8u
M1824
"nch"
net247127
8u/1u
M1903
"nch"
C1
net190166
8u/1u
M1826
"nch"
net164235
8u/1u
wdr=8u
C1
net47531
ldr:1u
wdr=8u
C2
net247121
8u/1u
M1906
"nch"
net190552
ldr:1u
wdr=8u
C1
net93048
ldr:1u
net247531
ldr:1u
wdr=8u

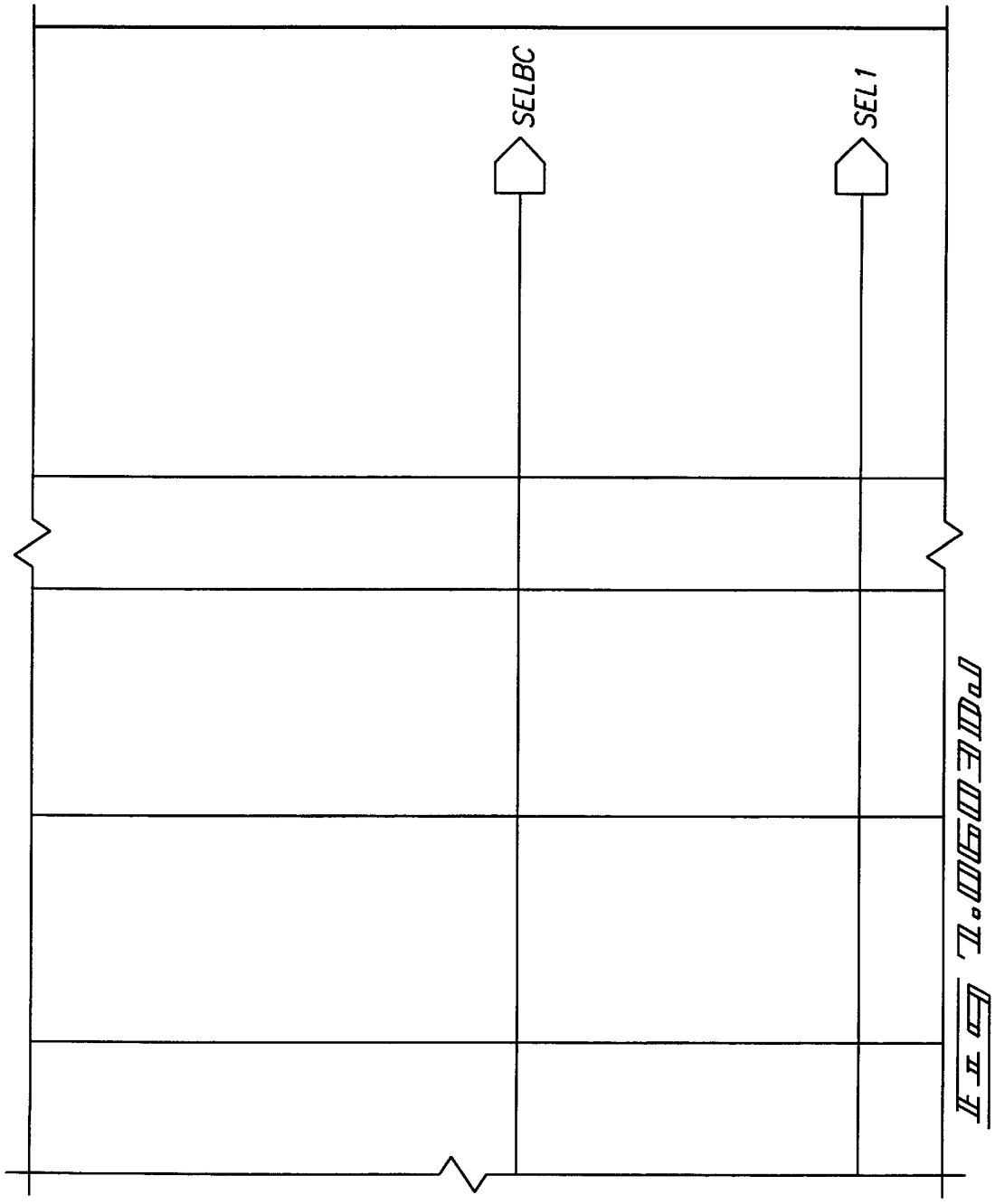

M1825
"nch"
rseld
8u/1u
M1904
"nch"
S2
selbd
8u/1u
M1827
"nch"
S2
selbcd
8u/1u
nel190166
ldr:1u
wdr=8u
nel104235
ldr:1u

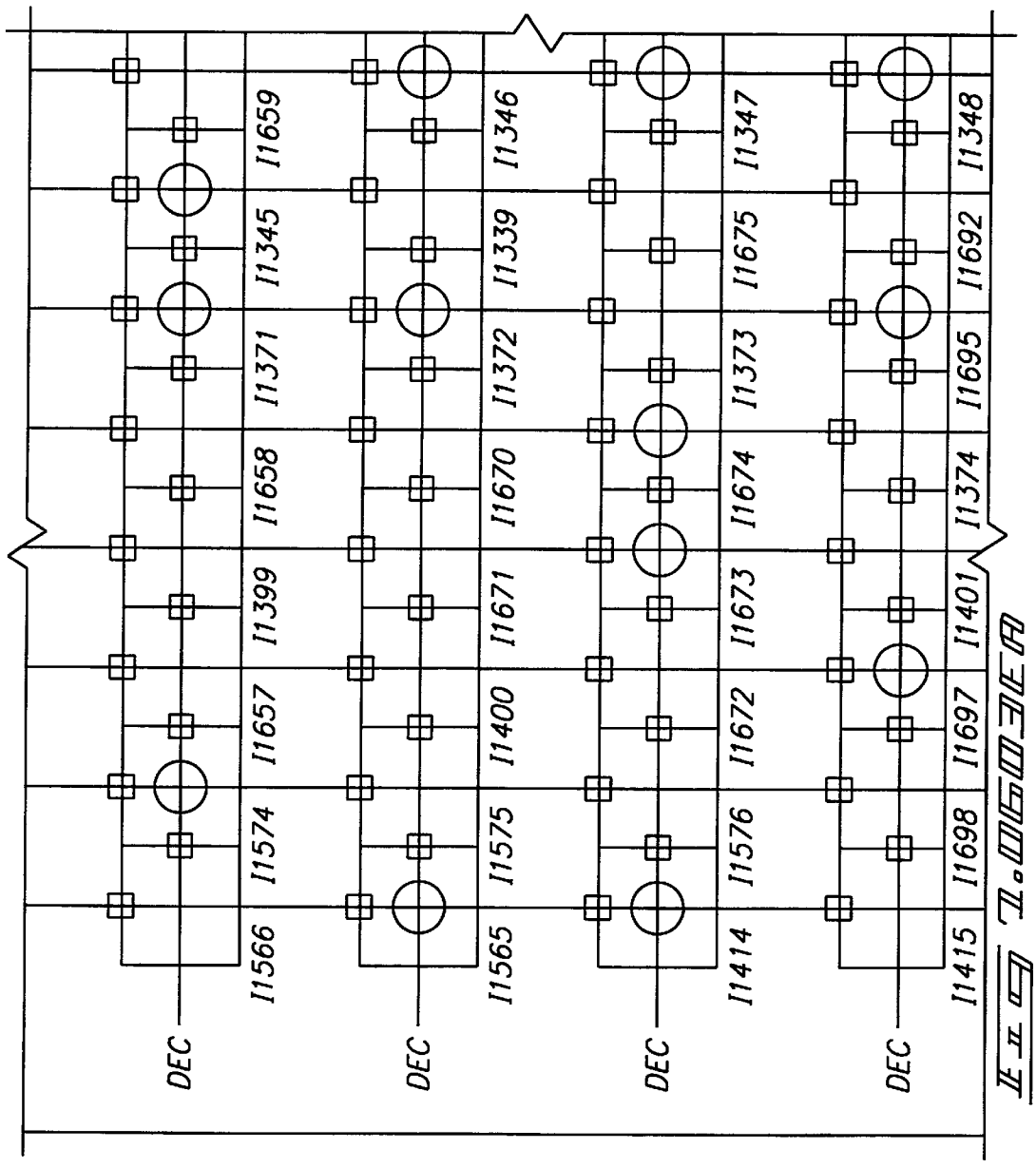

inspamp
PLA AMP
I134
DEC
selbcd
EV
FIG. 676

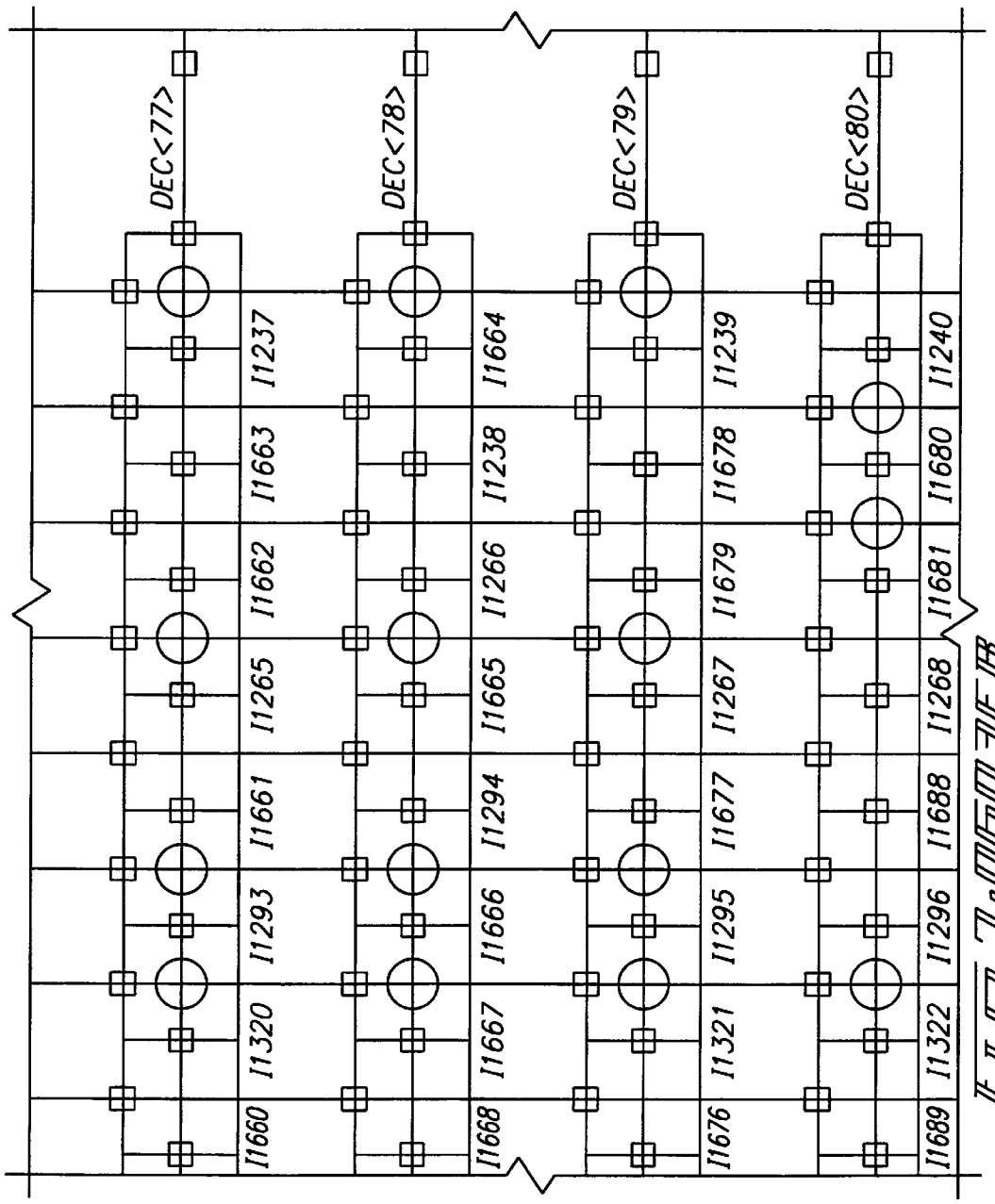

PH
DRV
PH
DRV
L1N
ROM PLA LATCH
I1114
insplat
L1N
ROM PLA LATCH
I1111
insplat
selbcg
DRV
FIG. 677


I1113
selbcl
16u/1u
I804
selbcn
selbcl
HOLDOM, LEE


24u/1u
SELBC
I1112
selbcn
16u/1u
I803
24u/1u
selbcn


SELBC
SEL1
FIG. 63L


DEC
DEC
DEC
DEC
I1566
I1574
I1657
I1399
I1658
I1371
I1345
I1659
I1565
I1575
I1400
I1671
I1670
I1372
I1339
I1346
I1414
I1576
I1672
I1673
I1674
I1373
I1675
I1347
I1415
I1698
I1697
I1401
I1374
I1695
I1692
I1348
FIG. 1600.1E


DEC<77>
DEC<78>
DEC<79>
DEC<80>
I1237
I1663
I1662
I1265
I1661
I1293
I1320
I1660
I1664
I1238
I1266
I1665
I1294
I1666
I1667
I1668
I1239
I1678
I1679
I1267
I1677
I1295
I1321
I1676
I1240
I1680
I1681
I1268
I1688
I1296
I1322
I1689

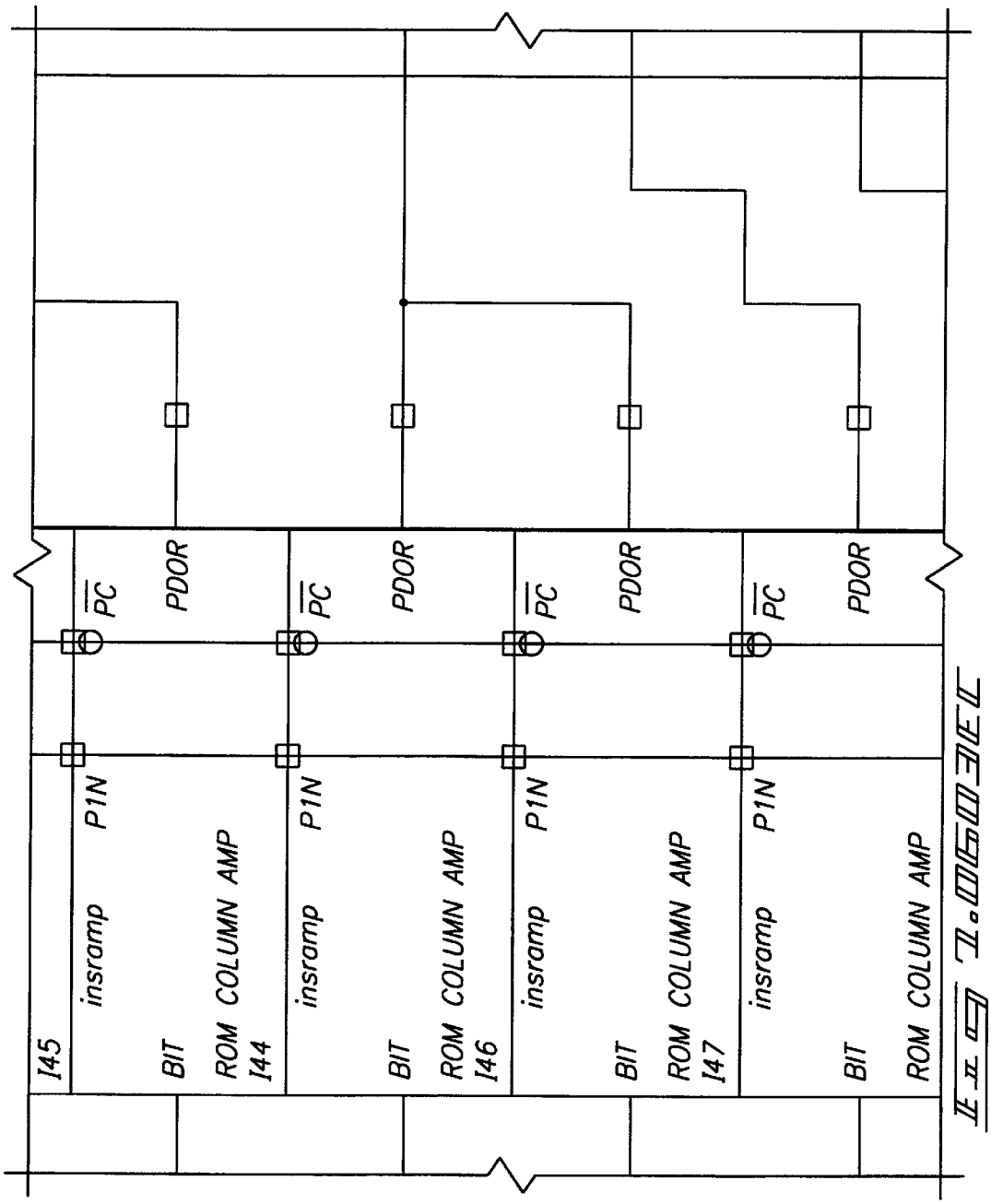
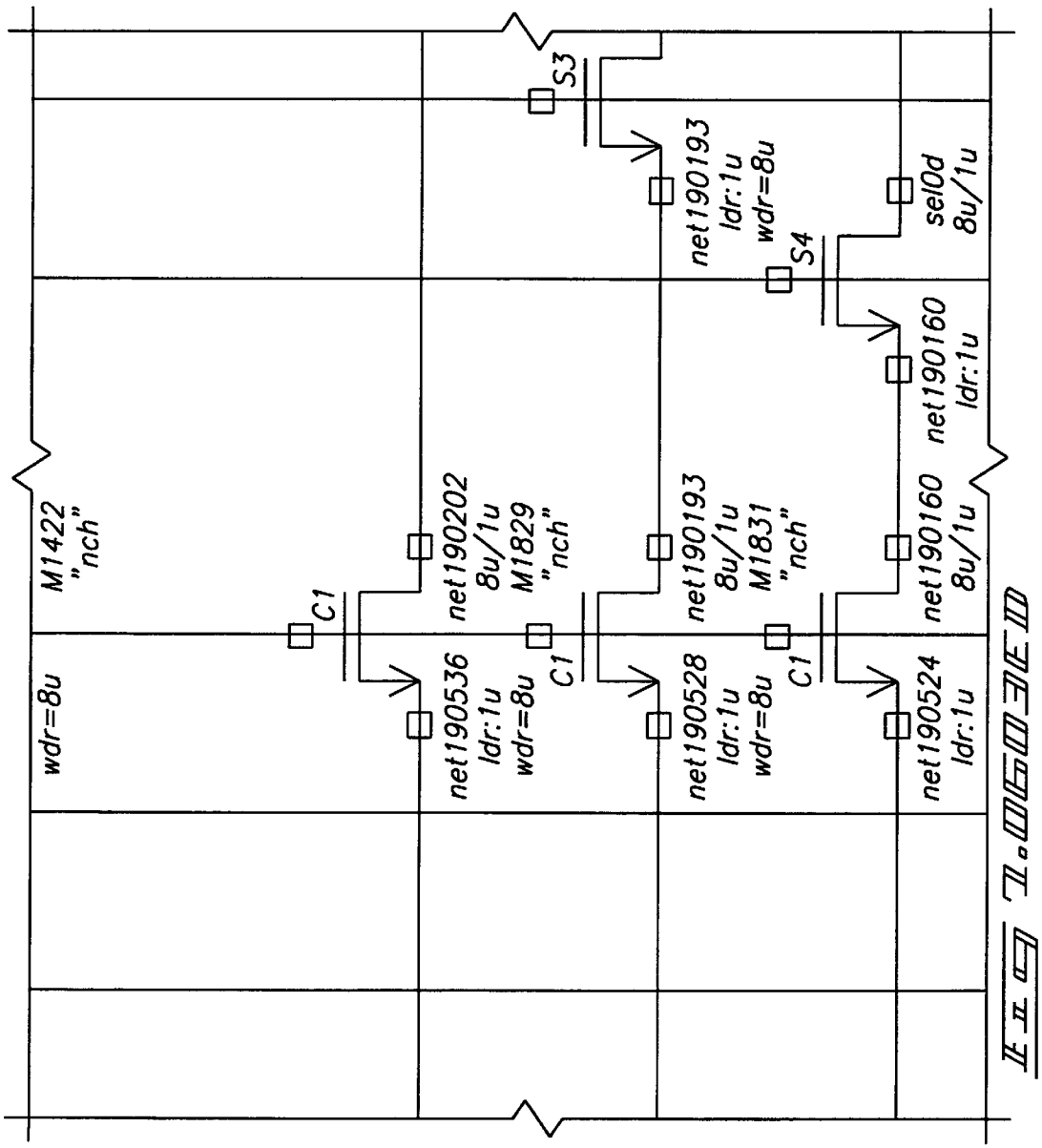
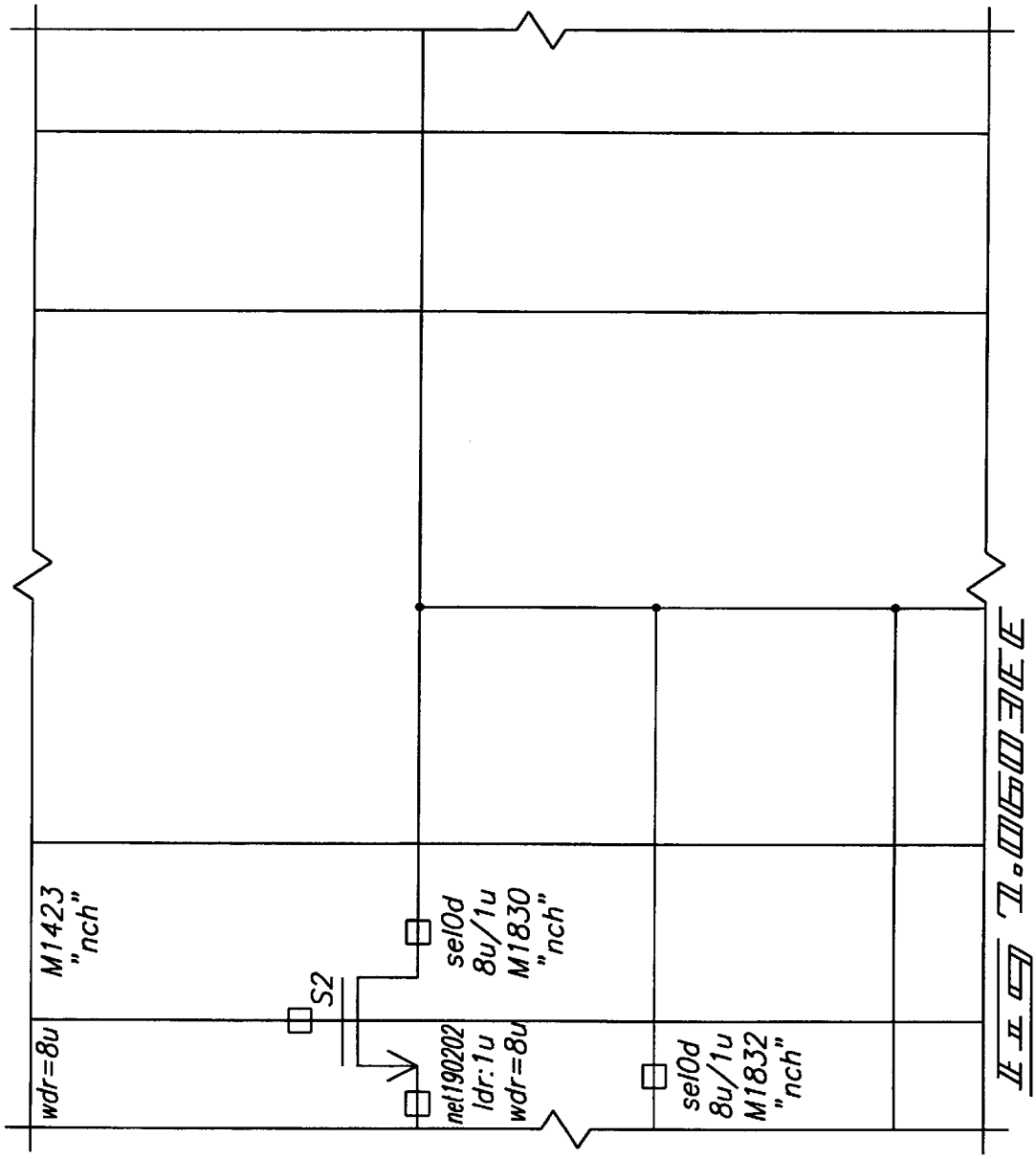
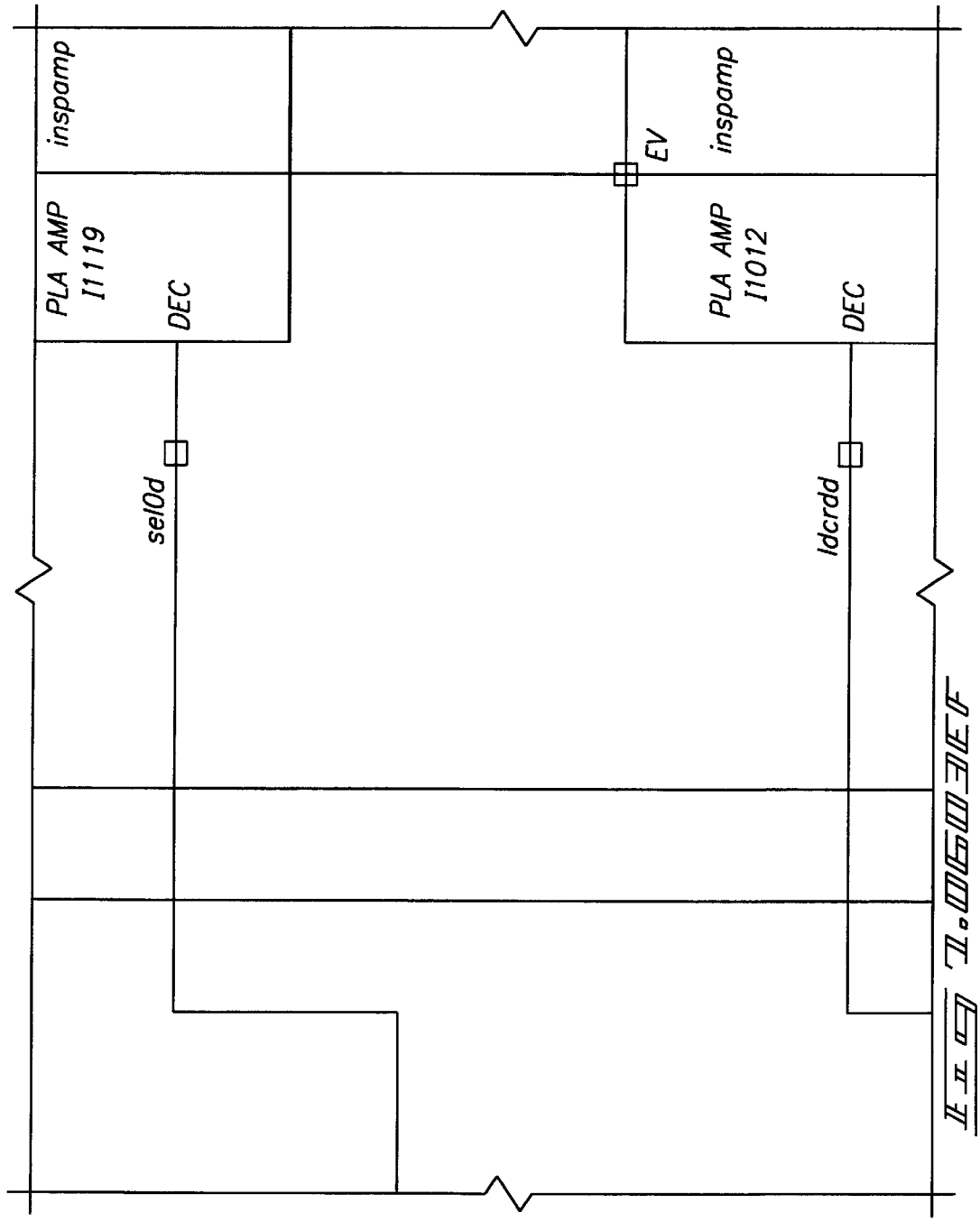


FIG. 659E


S3
net190193
ldr:1u
wdr=8u
S4
sel0d
8u/1u
net190160
ldr:1u
M1422
"nch"
C1
net190202
8u/1u
M1829
"nch"
net190193
8u/1u
M1831
"nch"
net190160
8u/1u
wdr=8u
net190536
ldr:1u
wdr=8u
C1
net190528
ldr:1u
wdr=8u
C1
net190524
ldr:1u


M1423
"nch"
wdr=8u
S2
net190202
ldr:1u
wdr=8u
sel0d
8u/1u
M1830
"nch"
sel0d
8u/1u
M1832
"nch"
FIG. 5


inspamp
PLA AMP
I1119
DEC
sel0d
EV
inspamp
PLA AMP
I1012
DEC
ldcrdd
FIG. 685.0L

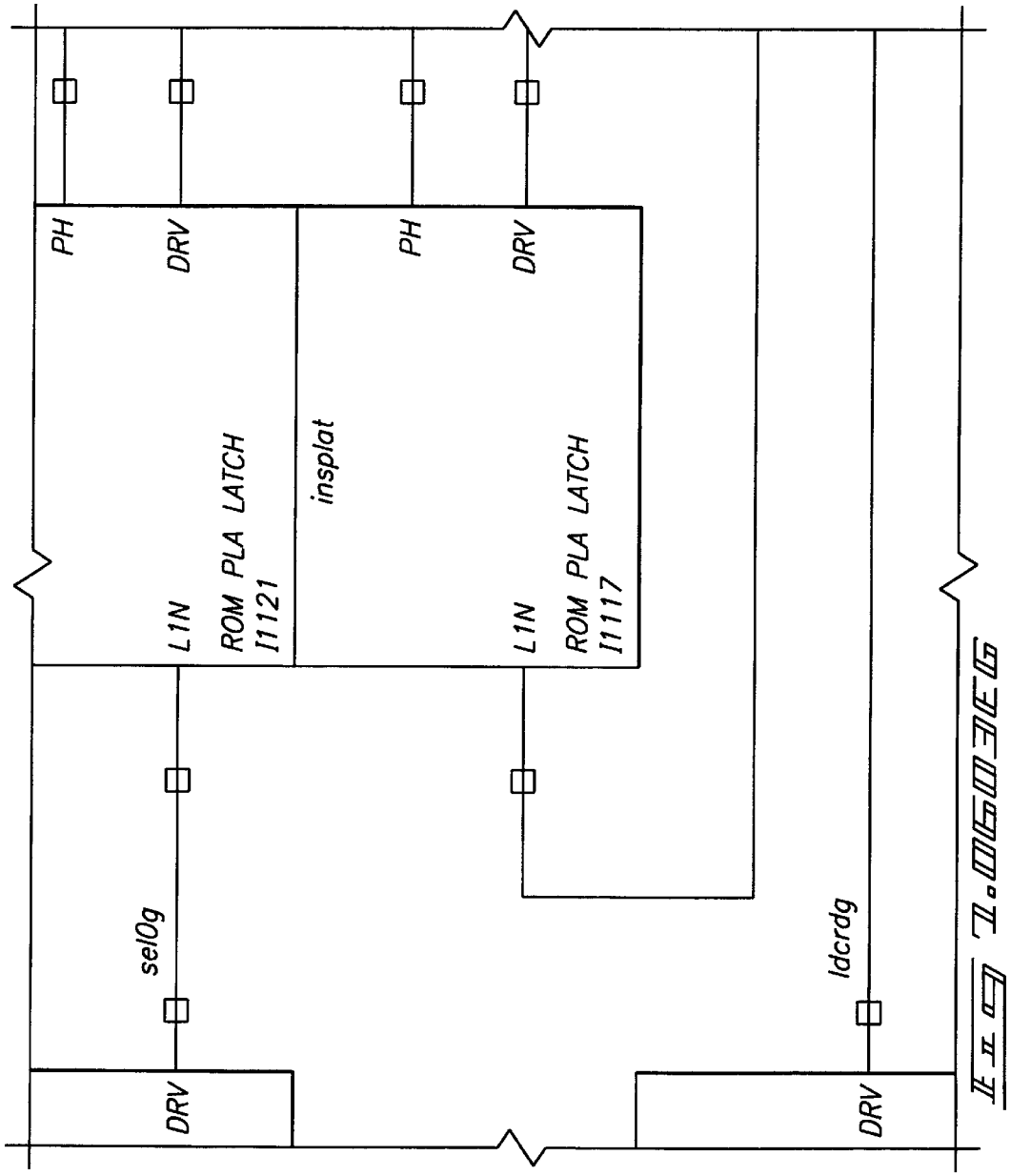
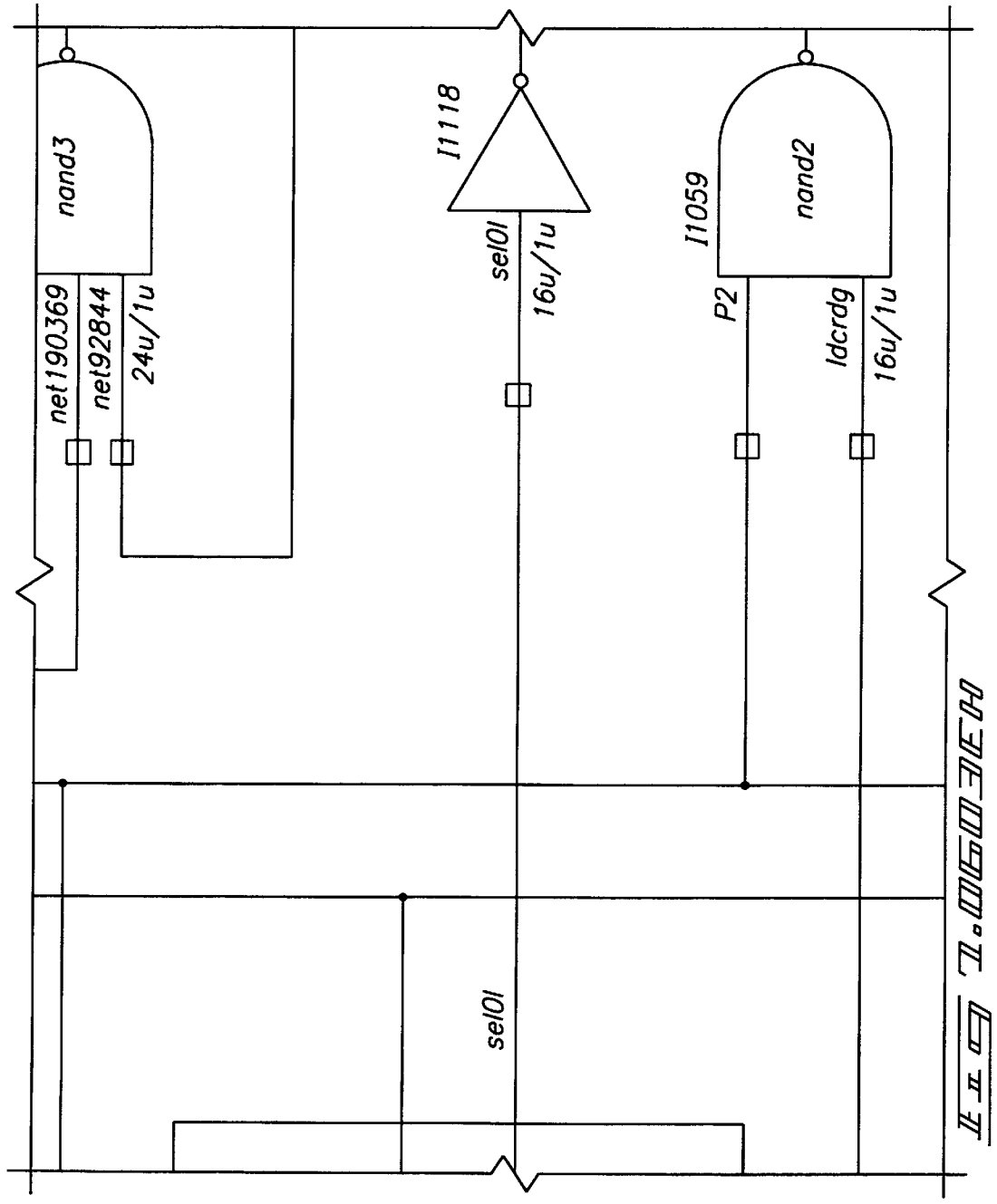
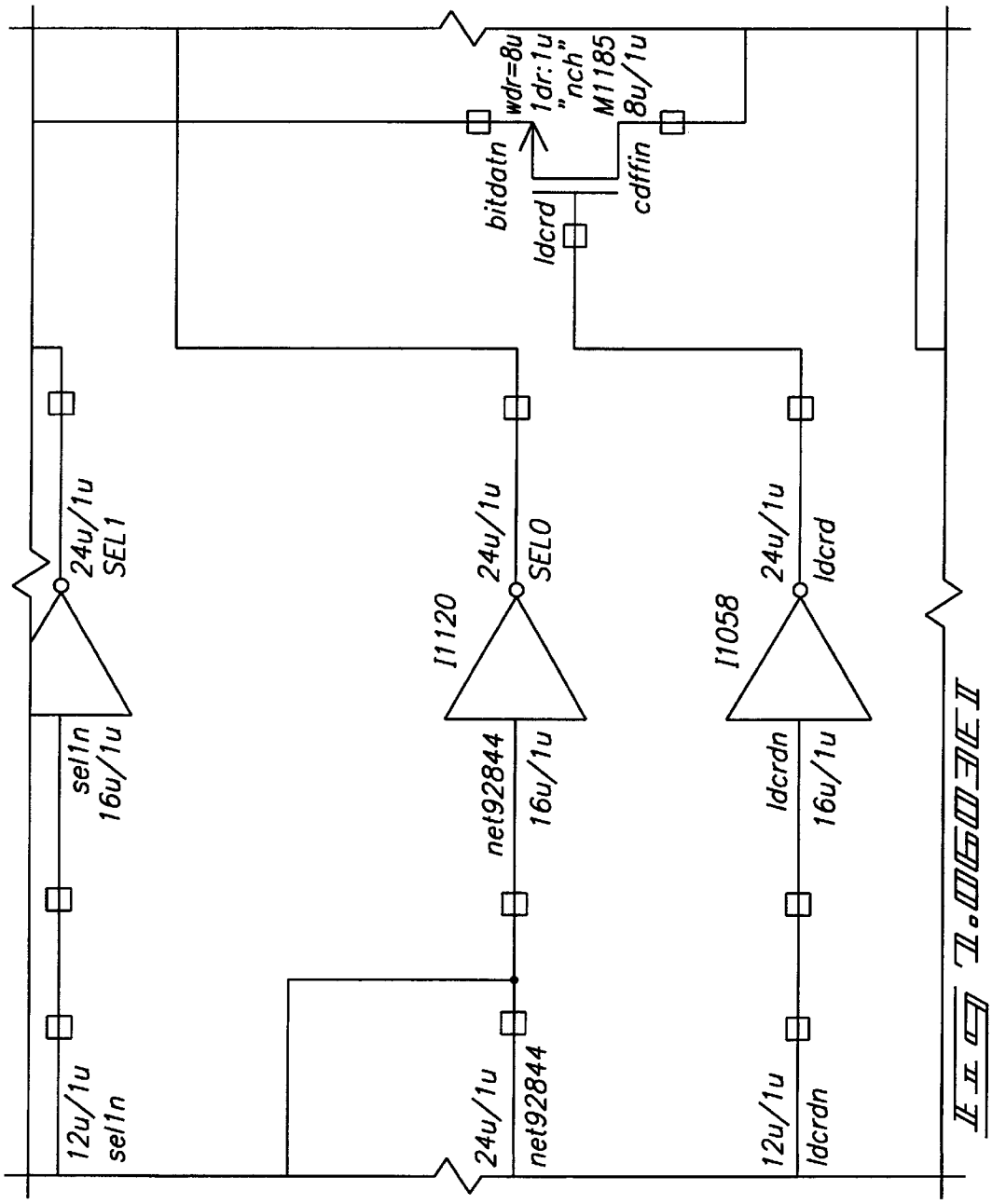
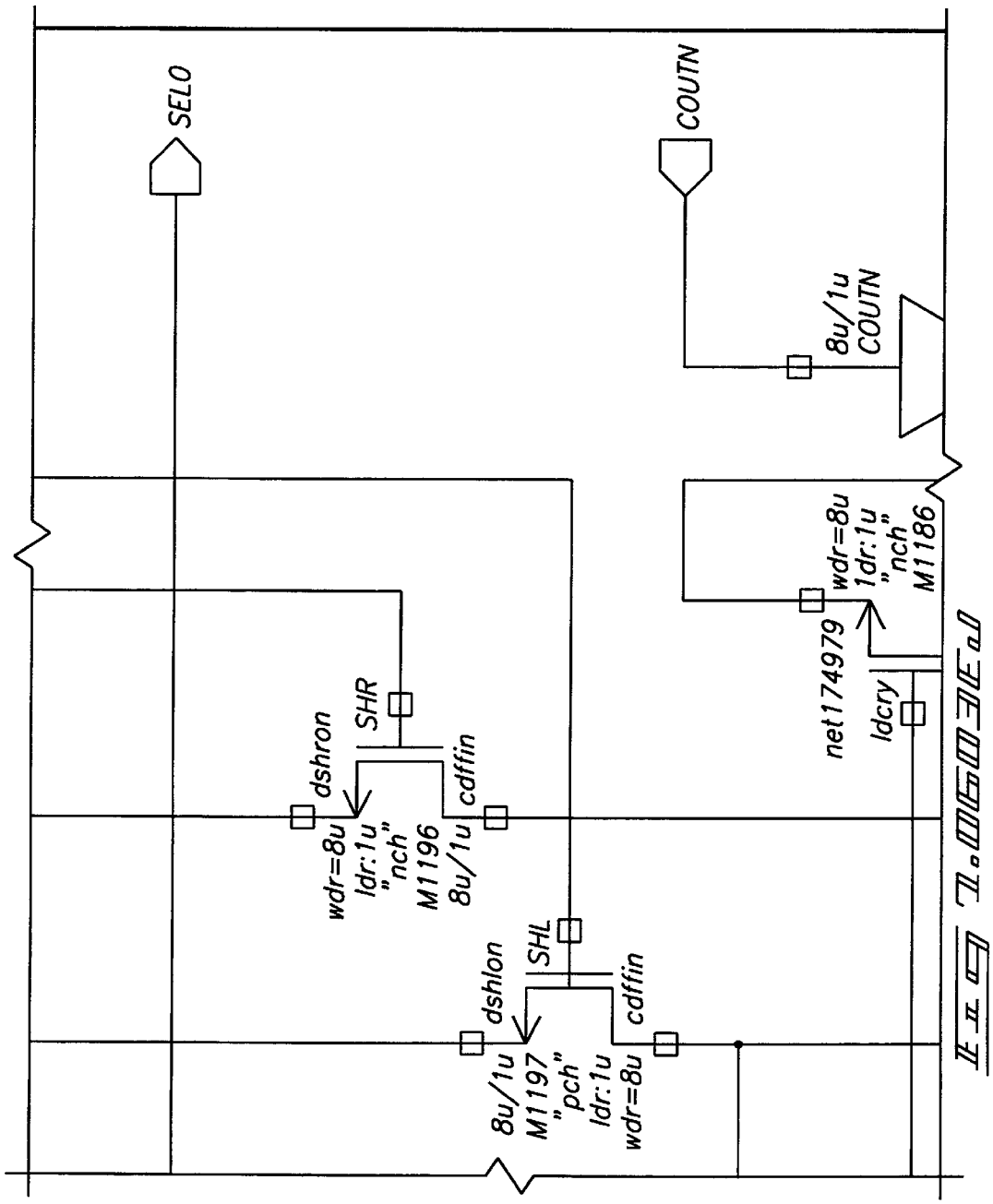

PH
DRV
PH
DRV
L1N
ROM PLA LATCH
I1121
insplat
L1N
ROM PLA LATCH
I1117
sel0g
ldcrdg
DRV
DRV

FIG. 1L


nand3
net190369
net92844
24u/1u
I1118
sel0l
16u/1u
I1059
nand2
P2
ldcrdg
16u/1u
sel0l


wdr=8u
1dr:1u
"nch"
M1185
8u/1u
bitdatn
cdffin
ldcrd
24u/1u
SEL1
24u/1u
SEL0
24u/1u
ldcrd
I1120
I1058
sel1n
16u/1u
net92844
16u/1u
ldcrdn
16u/1u
12u/1u
sel1n
24u/1u
net92844
12u/1u
ldcrdn
FIG 3E


SEL0
COUTN
8u/1u
COUTN
wdr=8u
ldr:1u
"nch"
M1186
net174979
ldcry
SHR
dshron
cdffin
wdr=8u
ldr:1u
"nch"
M1196
8u/1u
SHL
dshlon
cdffin
8u/1u
M1197
"pch"
ldr:1u
wdr=8u

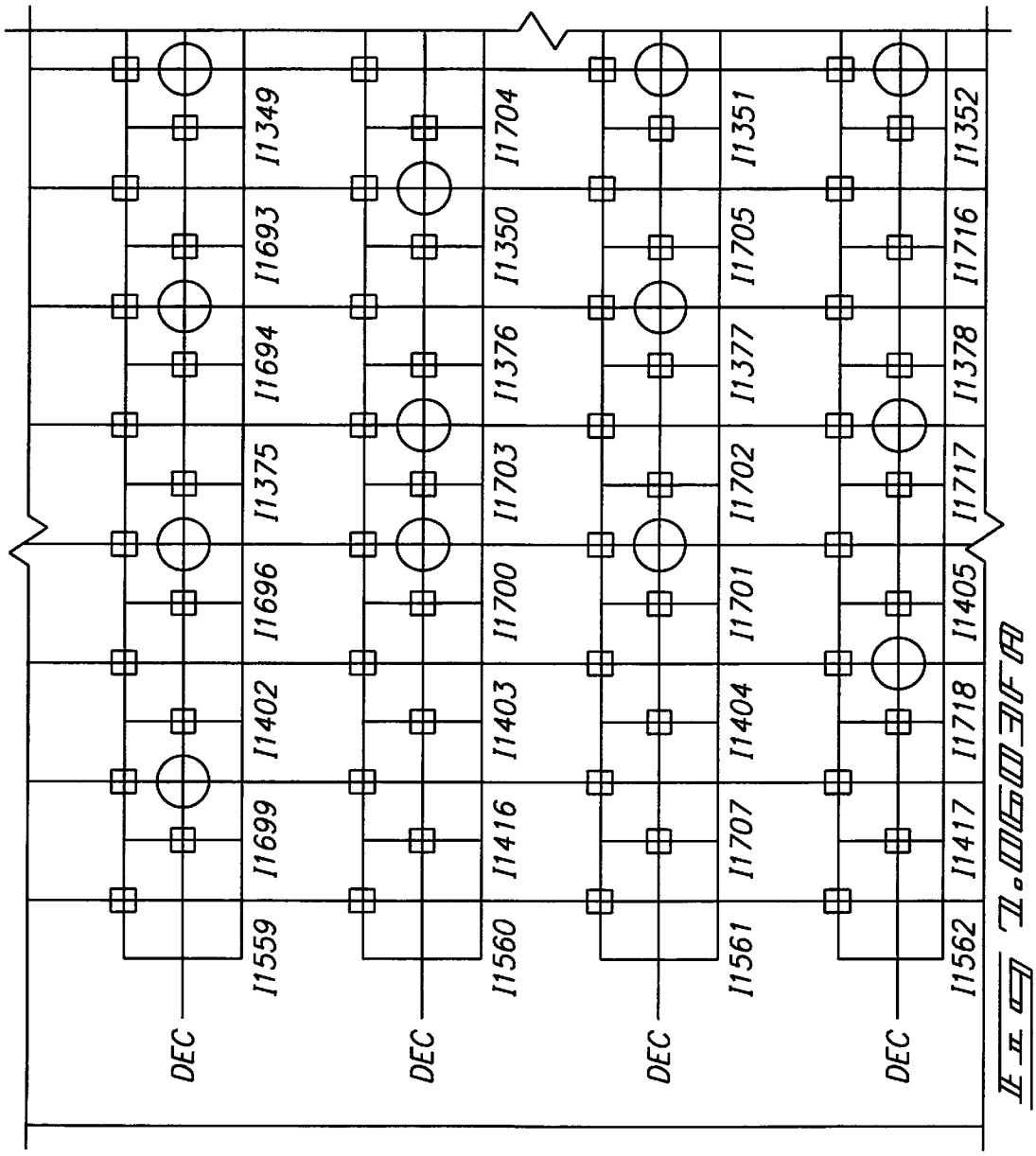
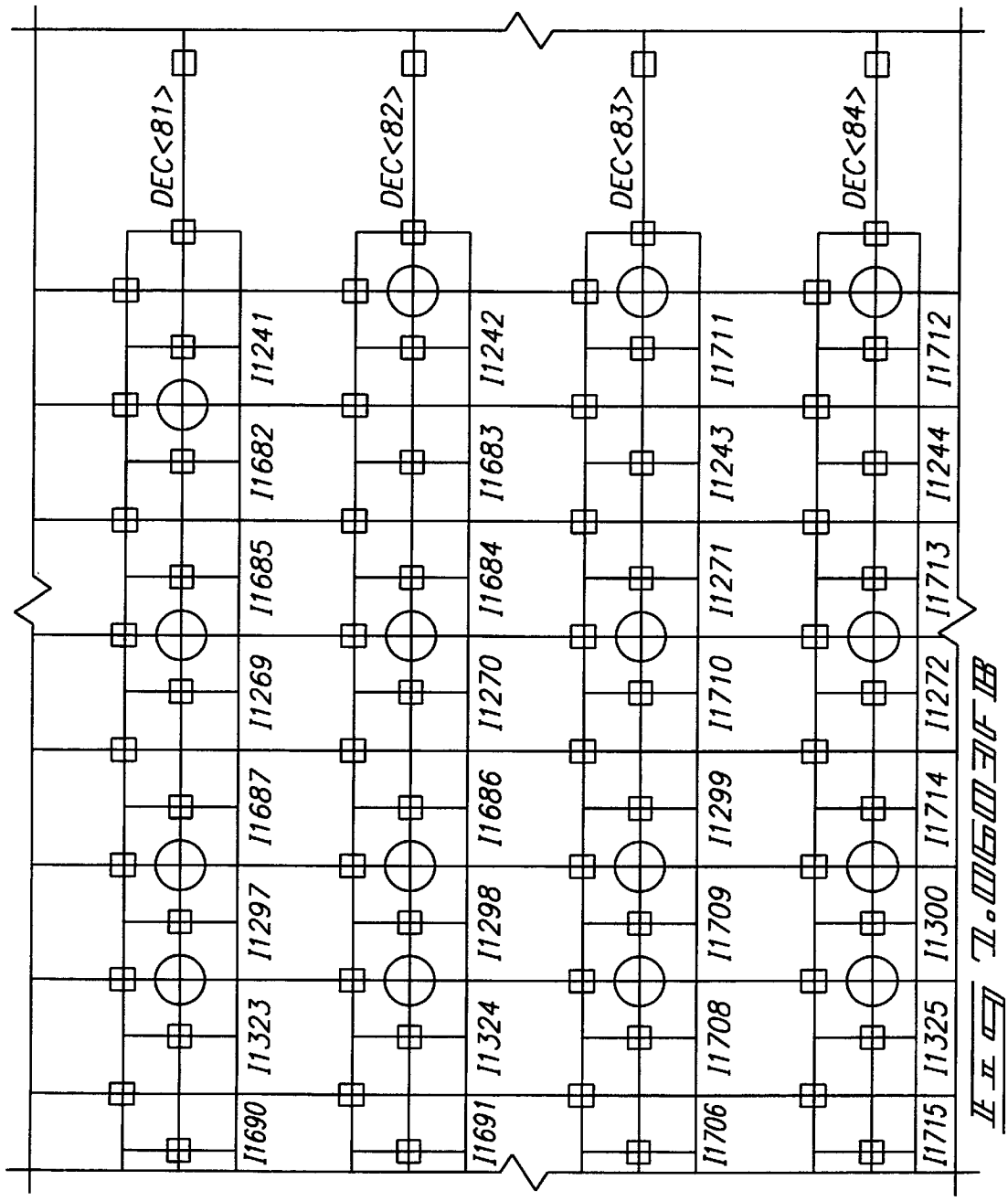

DEC
DEC
DEC
DEC
I1559
I1699
I1402
I1696
I1375
I1694
I1693
I1349
I1560
I1416
I1403
I1700
I1703
I1376
I1350
I1704
I1561
I1707
I1404
I1701
I1702
I1377
I1705
I1351
I1562
I1417
I1718
I1405
I1717
I1378
I1716
I1352

FIG. 691


DEC<81>
DEC<82>
DEC<83>
DEC<84>
I1241
I1682
I1685
I1269
I1687
I1297
I1323
I1690
I1242
I1683
I1684
I1270
I1686
I1298
I1324
I1691
I1711
I1243
I1271
I1710
I1299
I1709
I1708
I1706
I1712
I1244
I1713
I1272
I1714
I1300
I1325
I1715

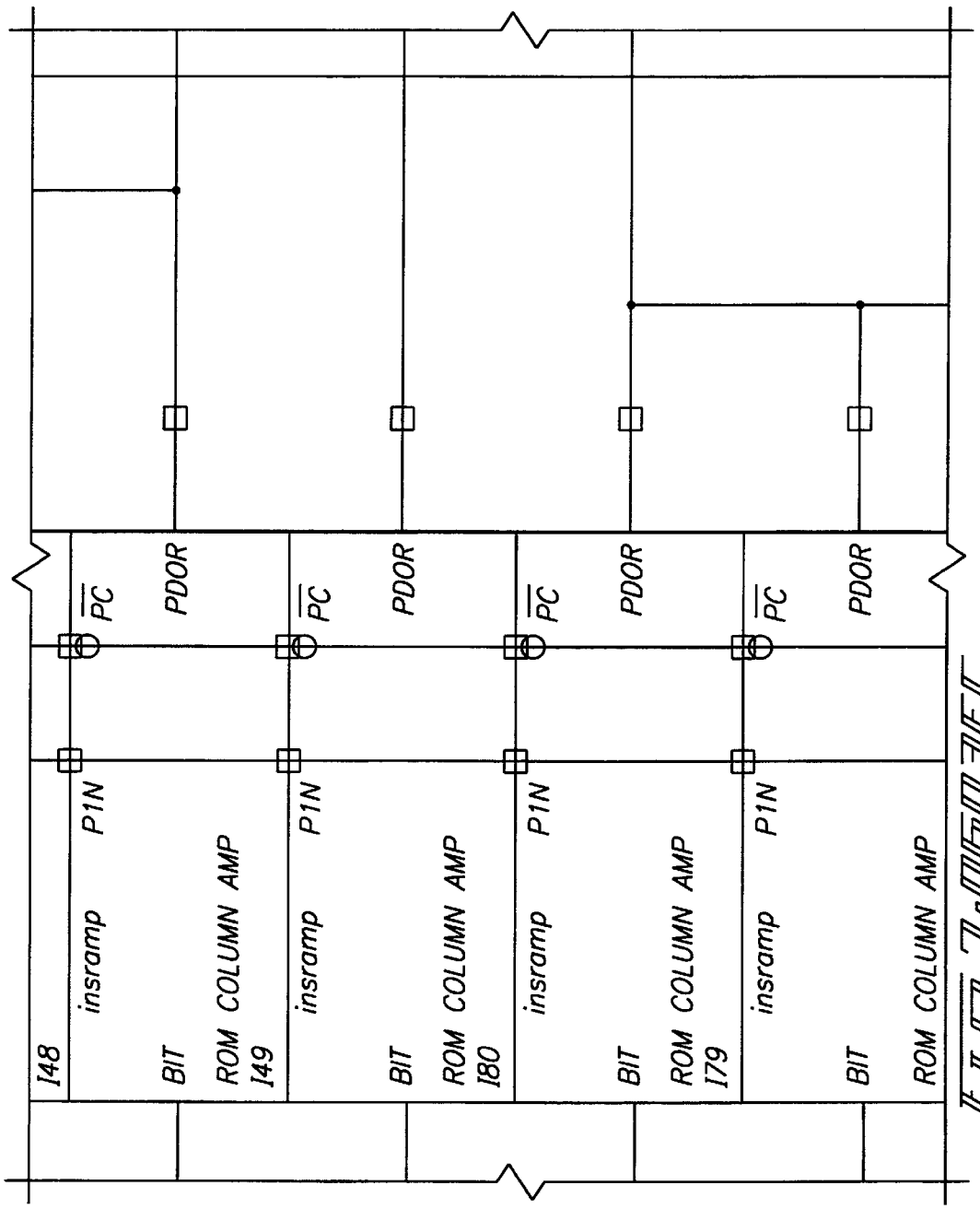


FIG. 169E

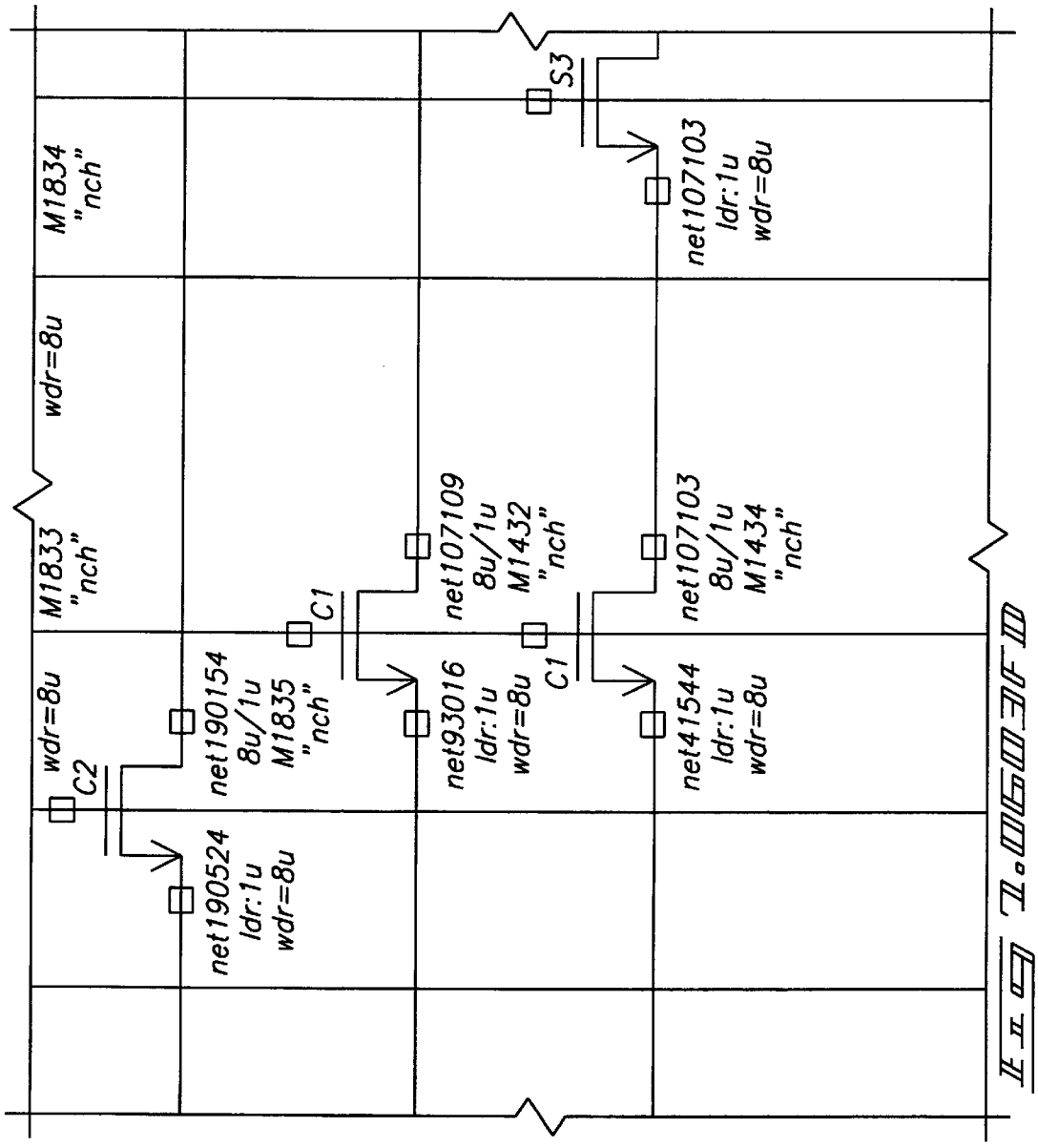

M1834
"nch"
wdr=8u
M1833
"nch"
wdr=8u
C2
net190524
ldr:1u
wdr=8u
net190154
8u/1u
M1835
"nch"
C1
net93016
ldr:1u
wdr=8u
net107109
8u/1u
M1432
"nch"
C1
net41544
ldr:1u
wdr=8u
S3
net107103
ldr:1u
wdr=8u
net107103
8u/1u
M1434
"nch"

FIG. 1L

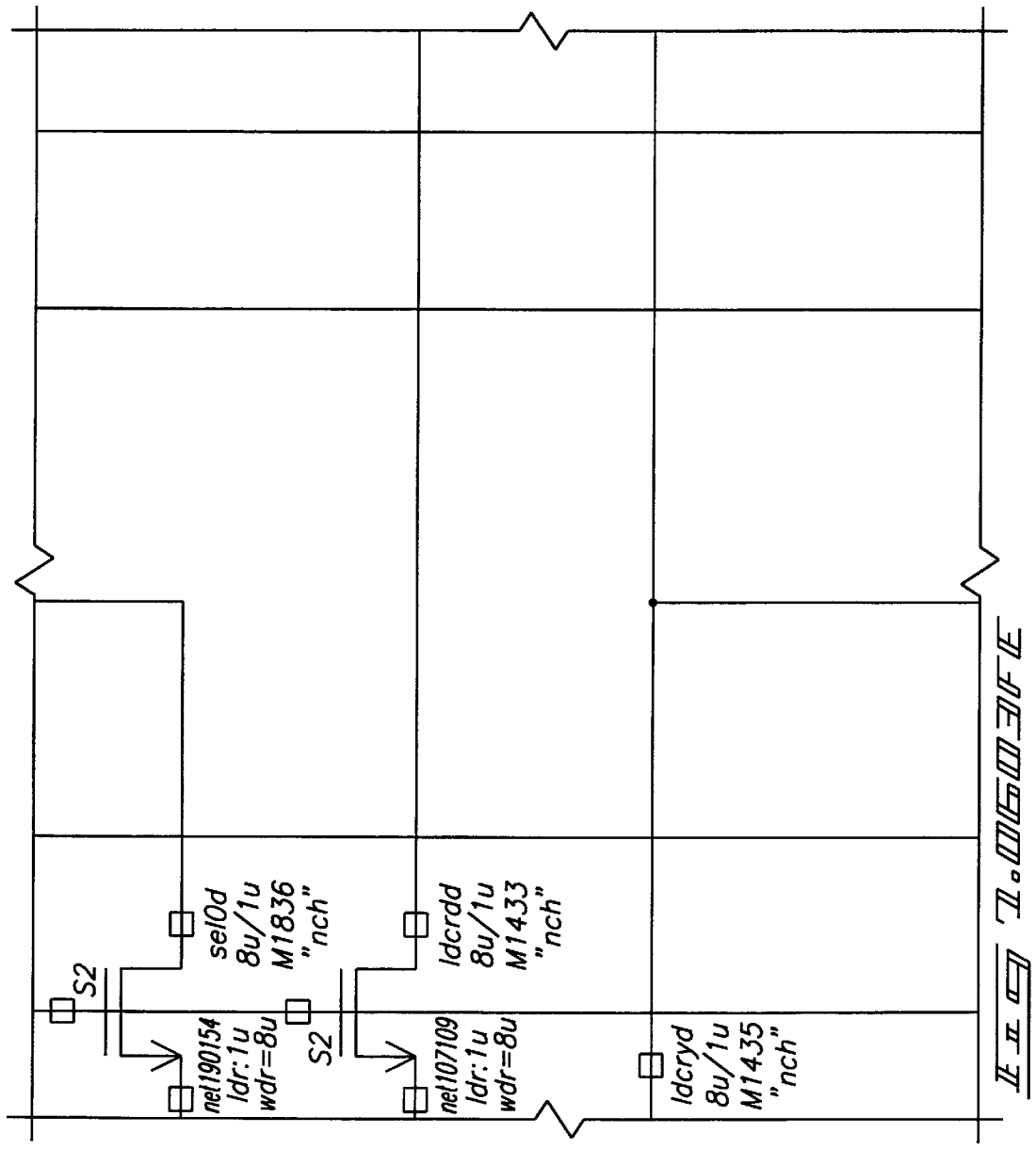
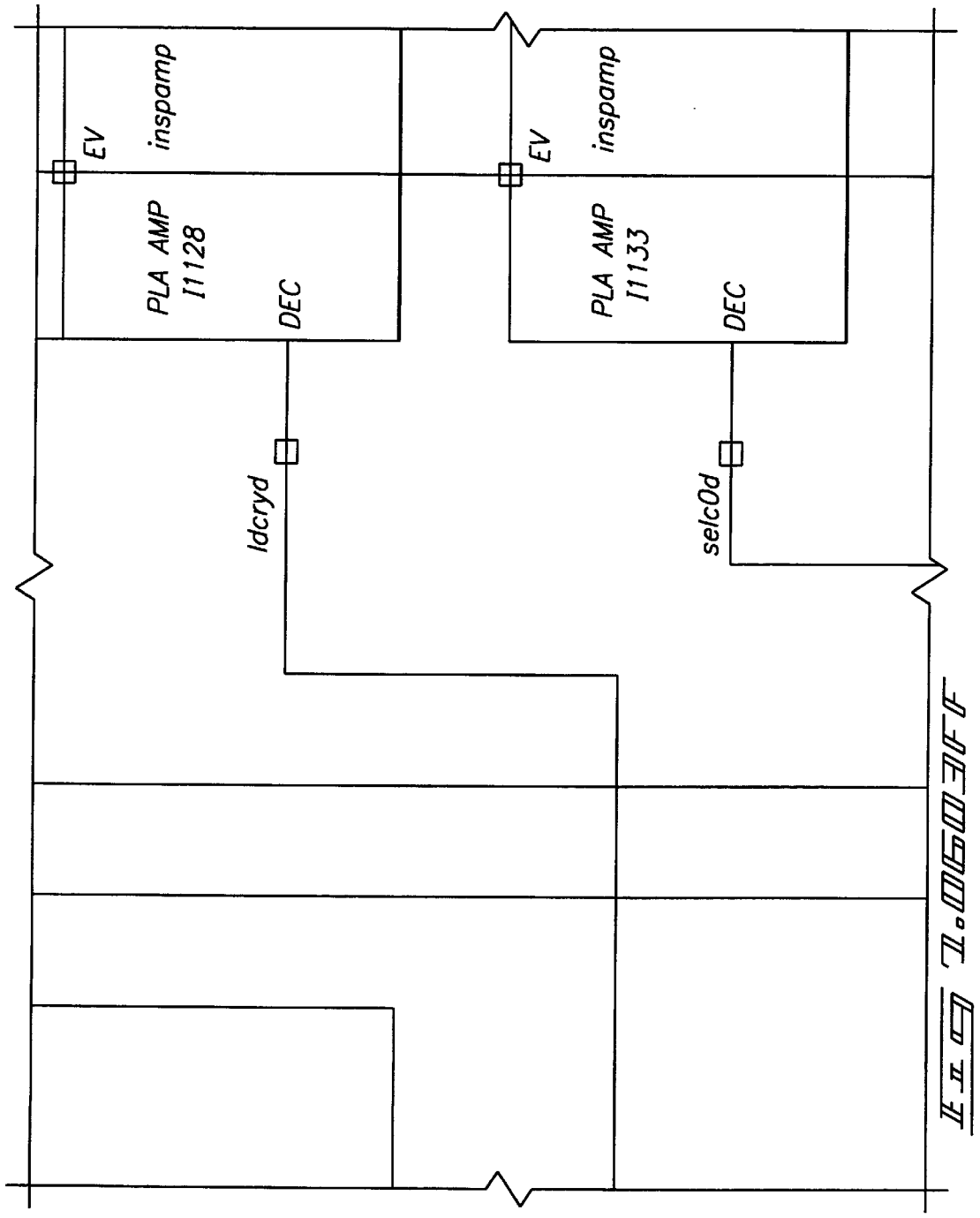
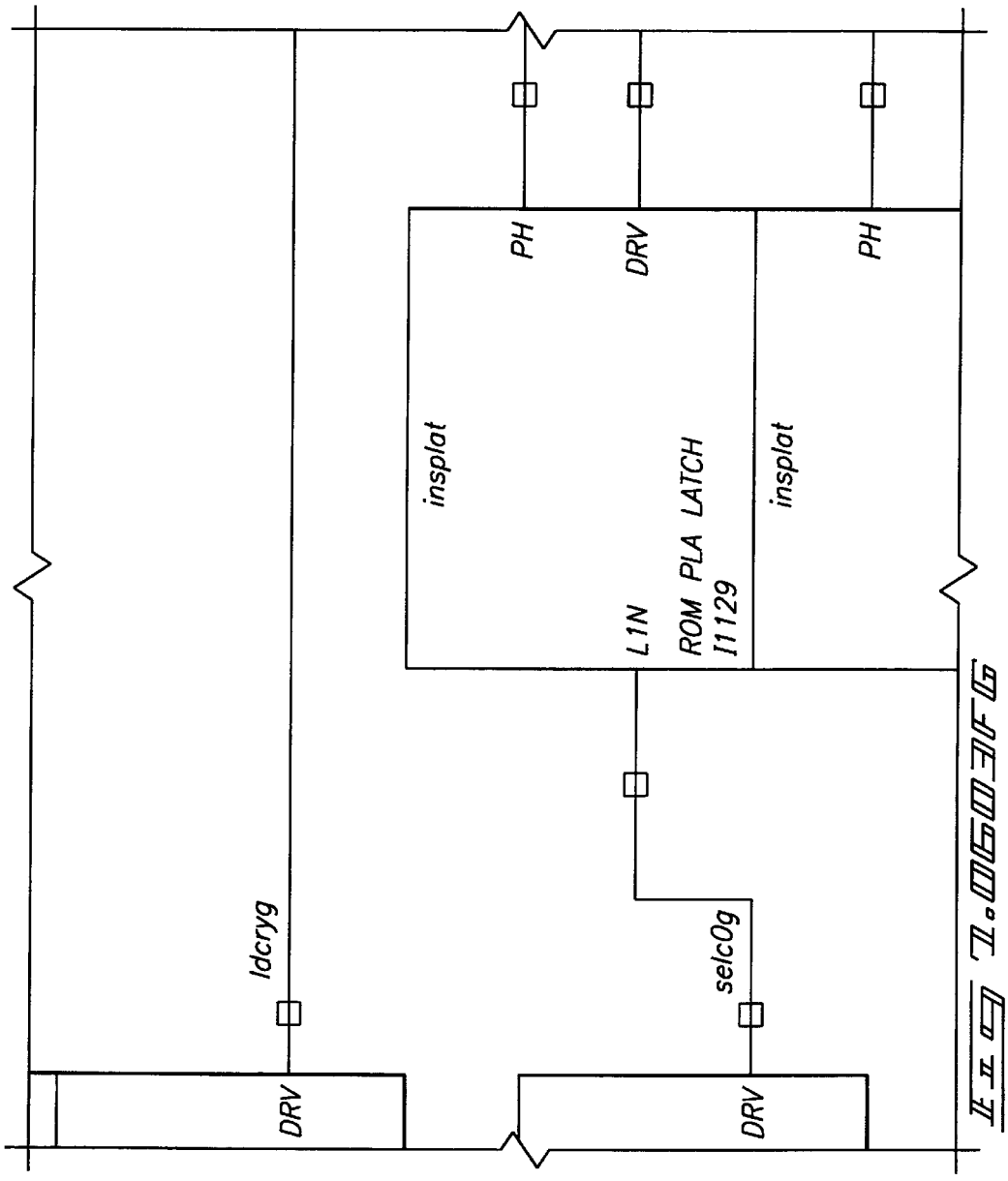
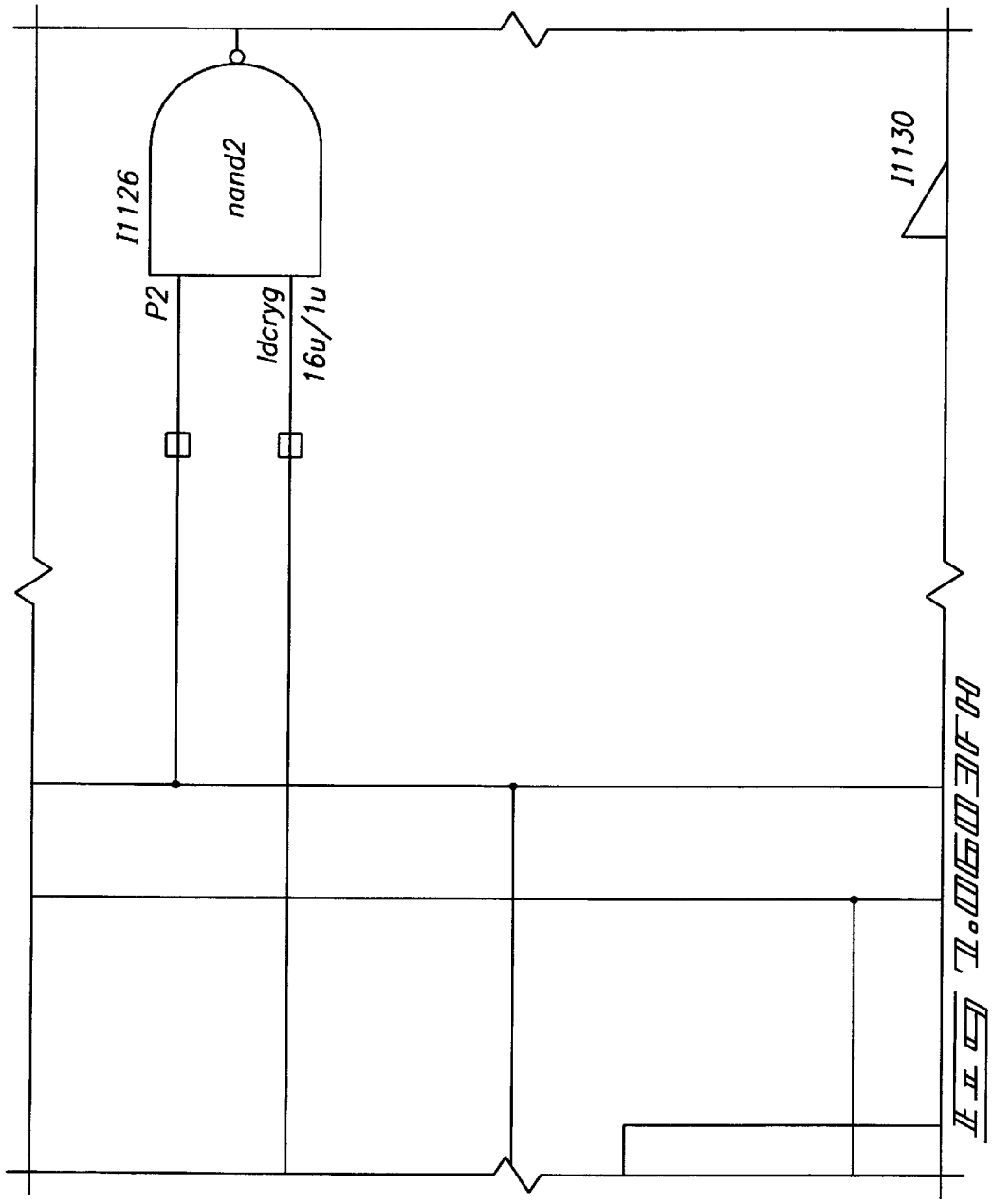
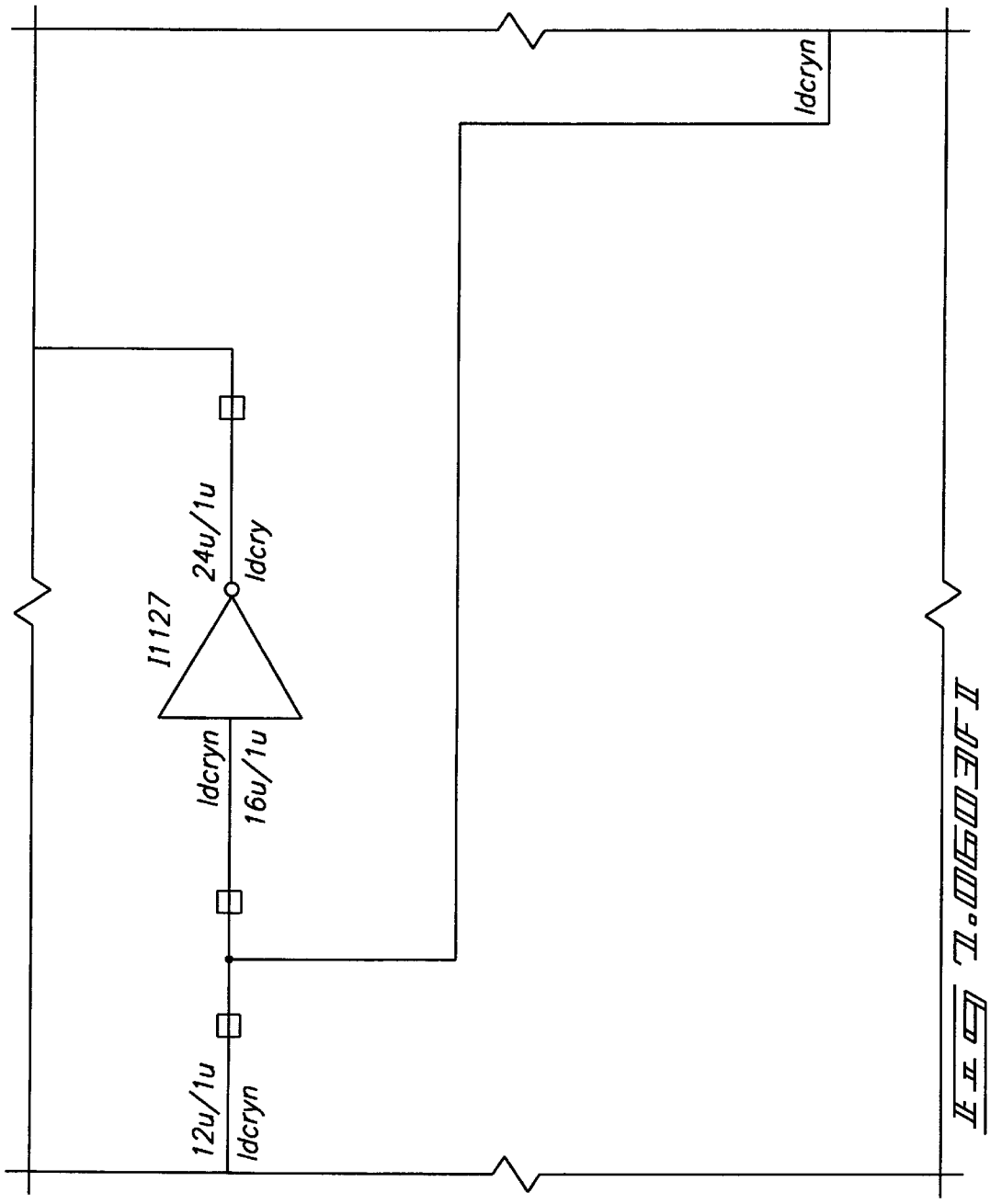


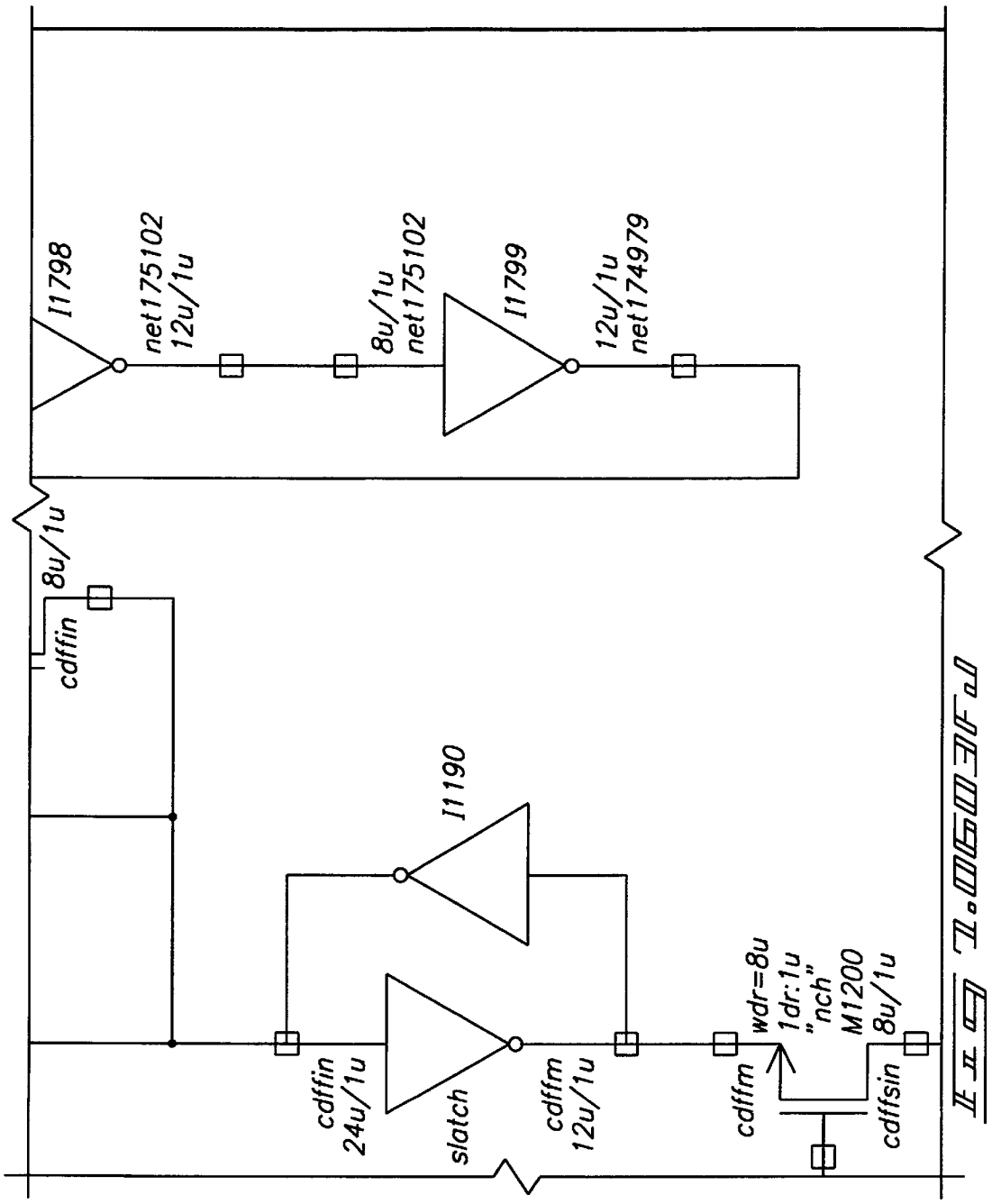
FIG. 695E
S2
sel0d
8u/1u
M1836
"nch"
S2
ldcrdd
8u/1u
M1433
"nch"
net190154
ldr:1u
wdr=8u
net107109
ldr:1u
wdr=8u
ldcryd
8u/1u
M1435
"nch"

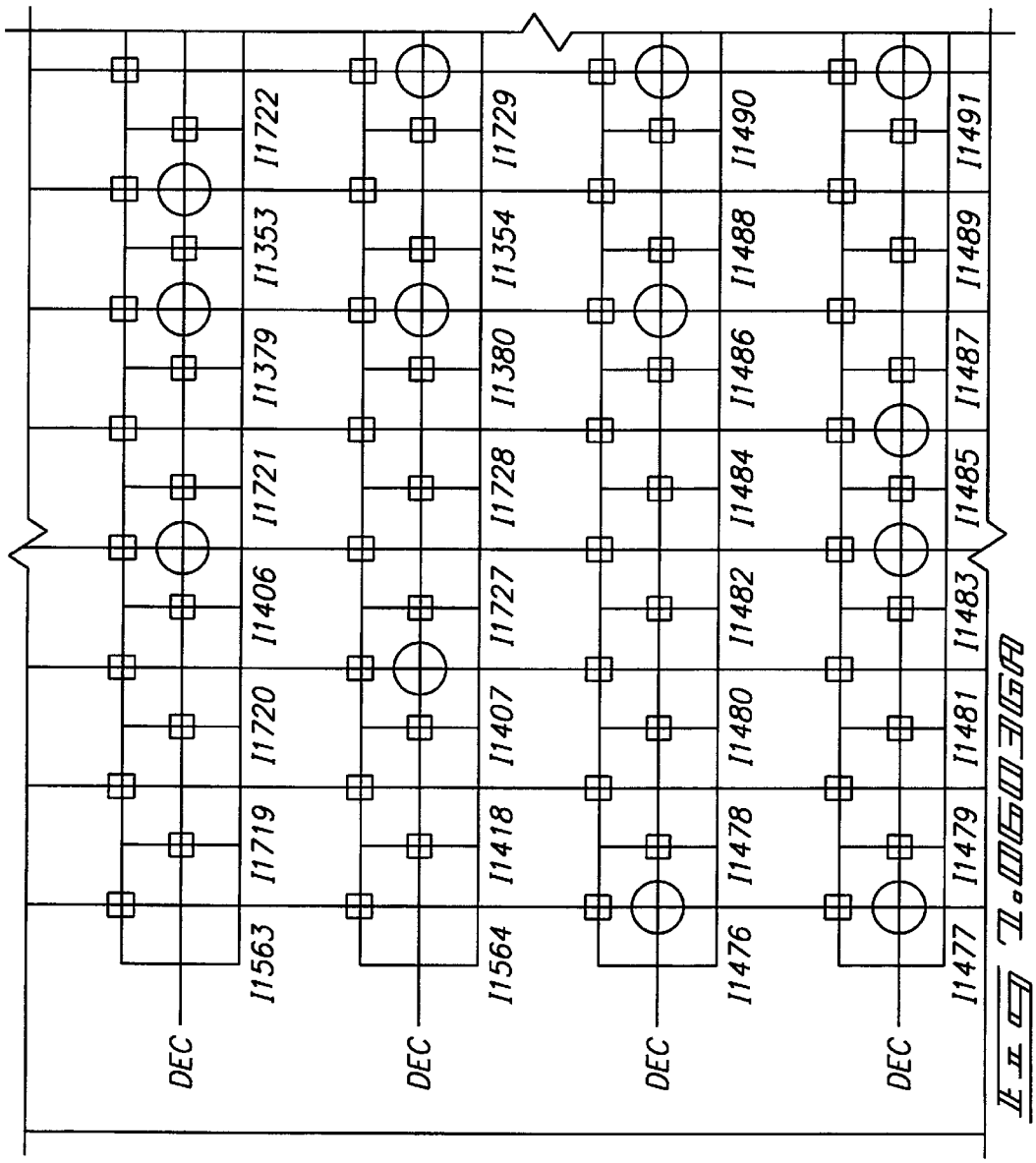

EV
inspamp
PLA AMP
I1128
DEC
EV
inspamp
PLA AMP
I1133
DEC
ldcryd
selc0d
FIG. 5900.1E

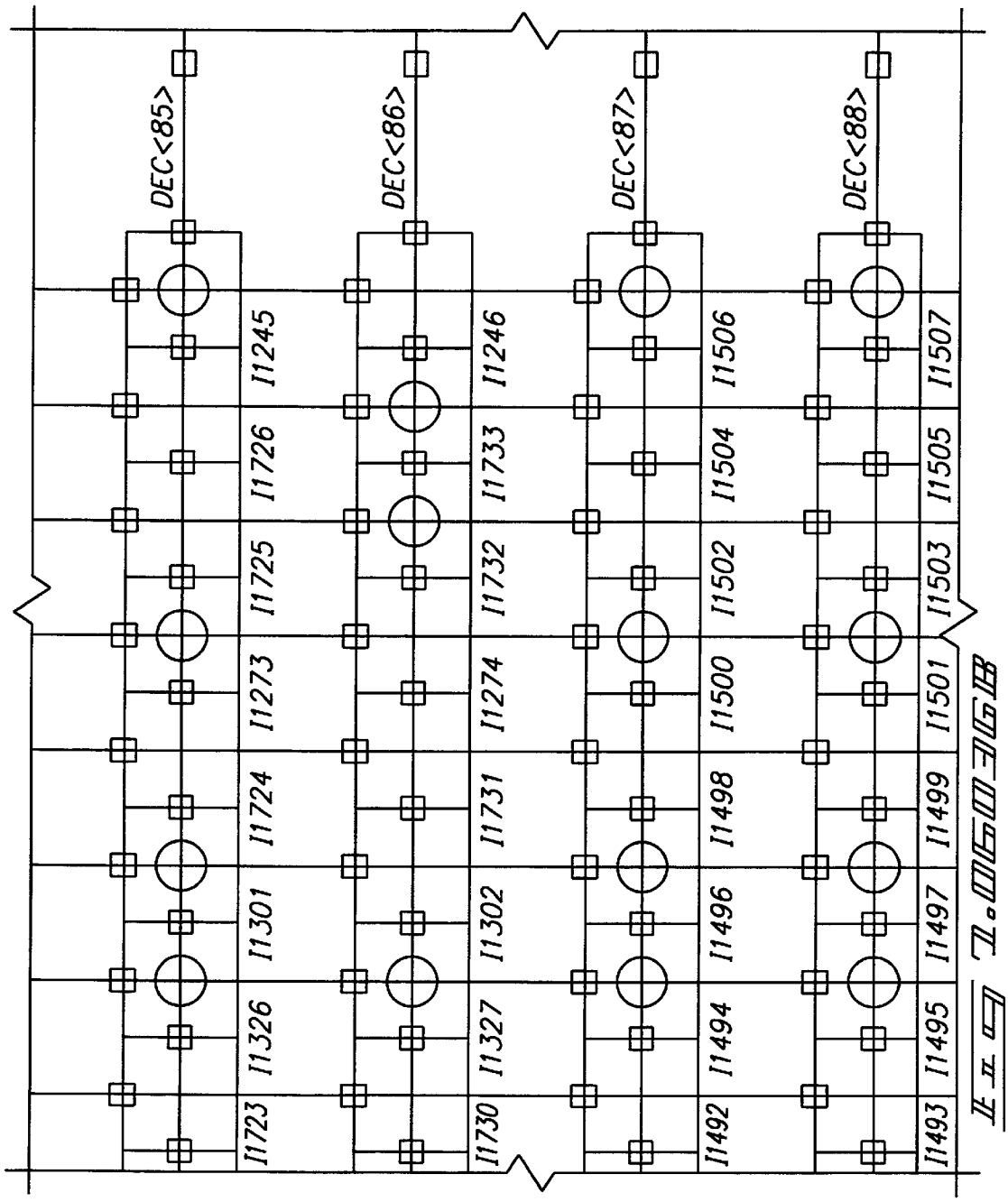

PH
DRV
PH
insplat
L1N
ROM PLA LATCH
I1129
insplat
ldcryg
selc0g
DRV
DRV
FIG. 1L


I1126
nand2
I1130
P2
ldcryg
16u/1u


ldcryn
24u/1u
ldcry
I1127
ldcryn
16u/1u
12u/1u
ldcryn
FIG. 699


I1798
net175102
12u/1u
8u/1u
net175102
I1799
12u/1u
net174979
8u/1u
cdffin
I1190
cdffin
24u/1u
slatch
cdffm
12u/1u
cdffm
wdr=8u
1dr:1u
"nch"
M1200
8u/1u
cdffsin


DEC
DEC
DEC
DEC
I1563
I1719
I1720
I1406
I1721
I1379
I1353
I1722
I1564
I1418
I1407
I1727
I1728
I1380
I1354
I1729
I1476
I1478
I1480
I1482
I1484
I1486
I1488
I1490
I1477
I1479
I1481
I1483
I1485
I1487
I1489
I1491
FIG. 1050.701


DEC<85>
DEC<86>
DEC<87>
DEC<88>
I1245
I1726
I1725
I1273
I1724
I1301
I1326
I1723
I1246
I1733
I1732
I1274
I1731
I1302
I1327
I1730
I1506
I1504
I1502
I1500
I1498
I1496
I1494
I1492
I1507
I1505
I1503
I1501
I1499
I1497
I1495
I1493

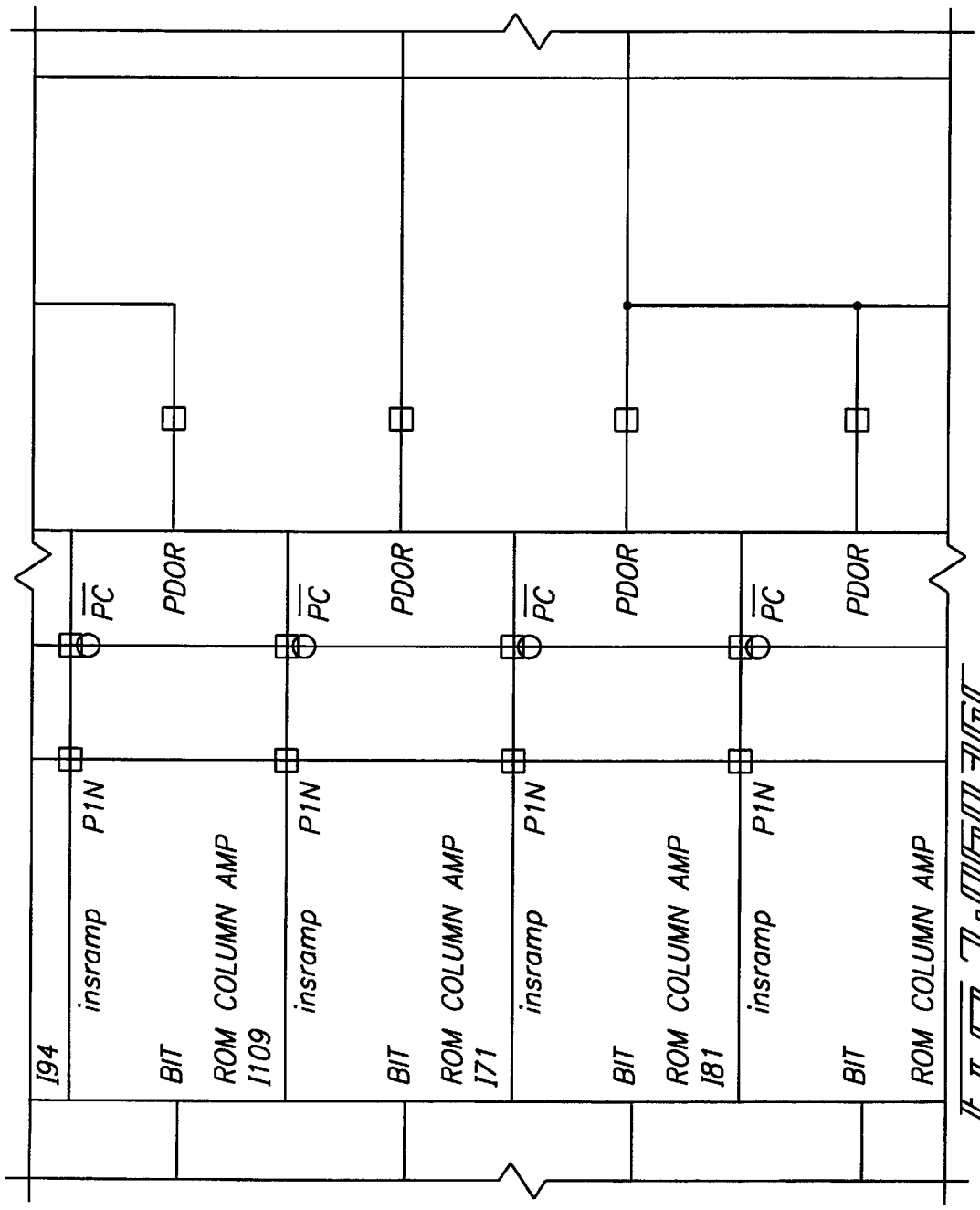
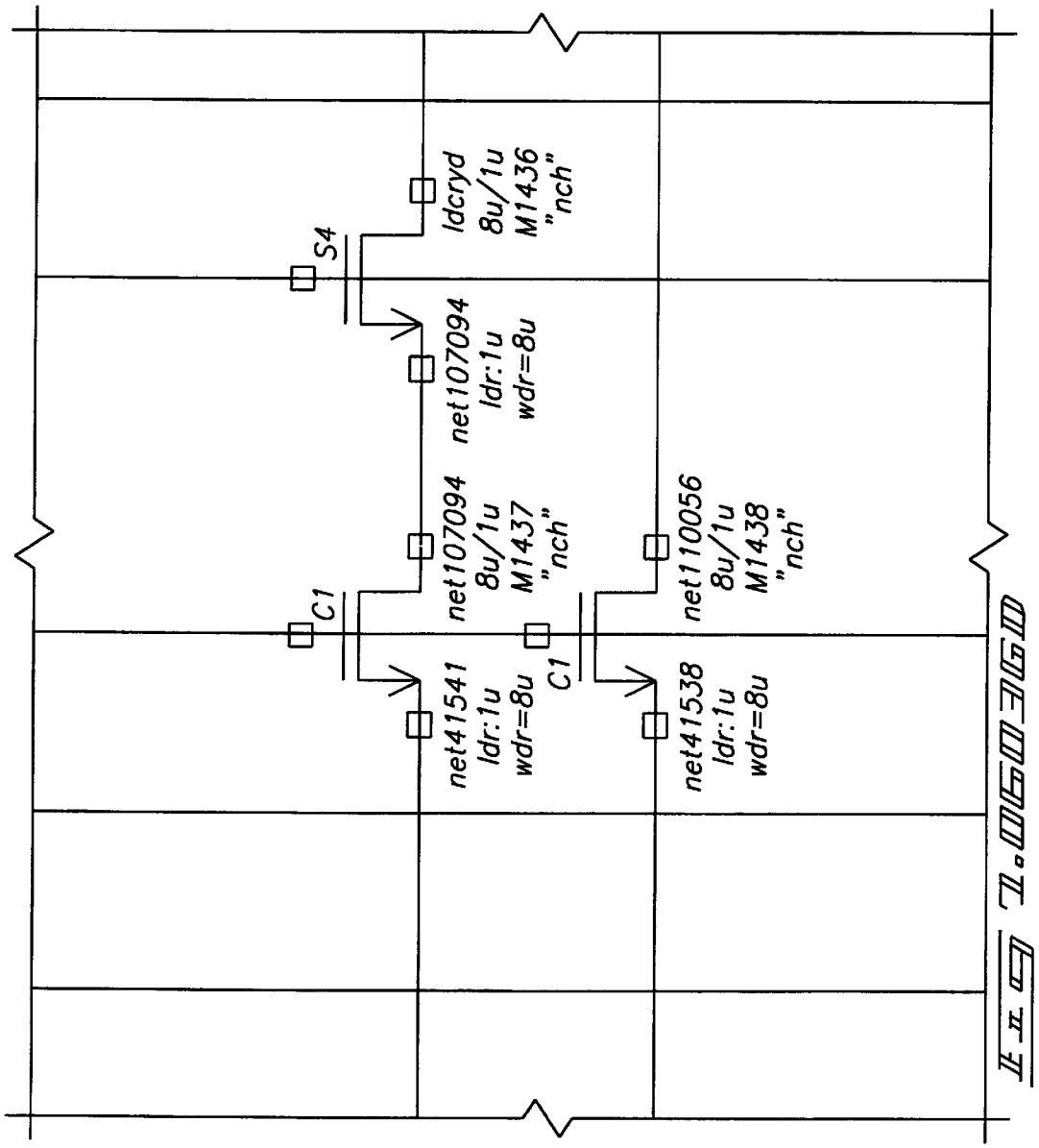
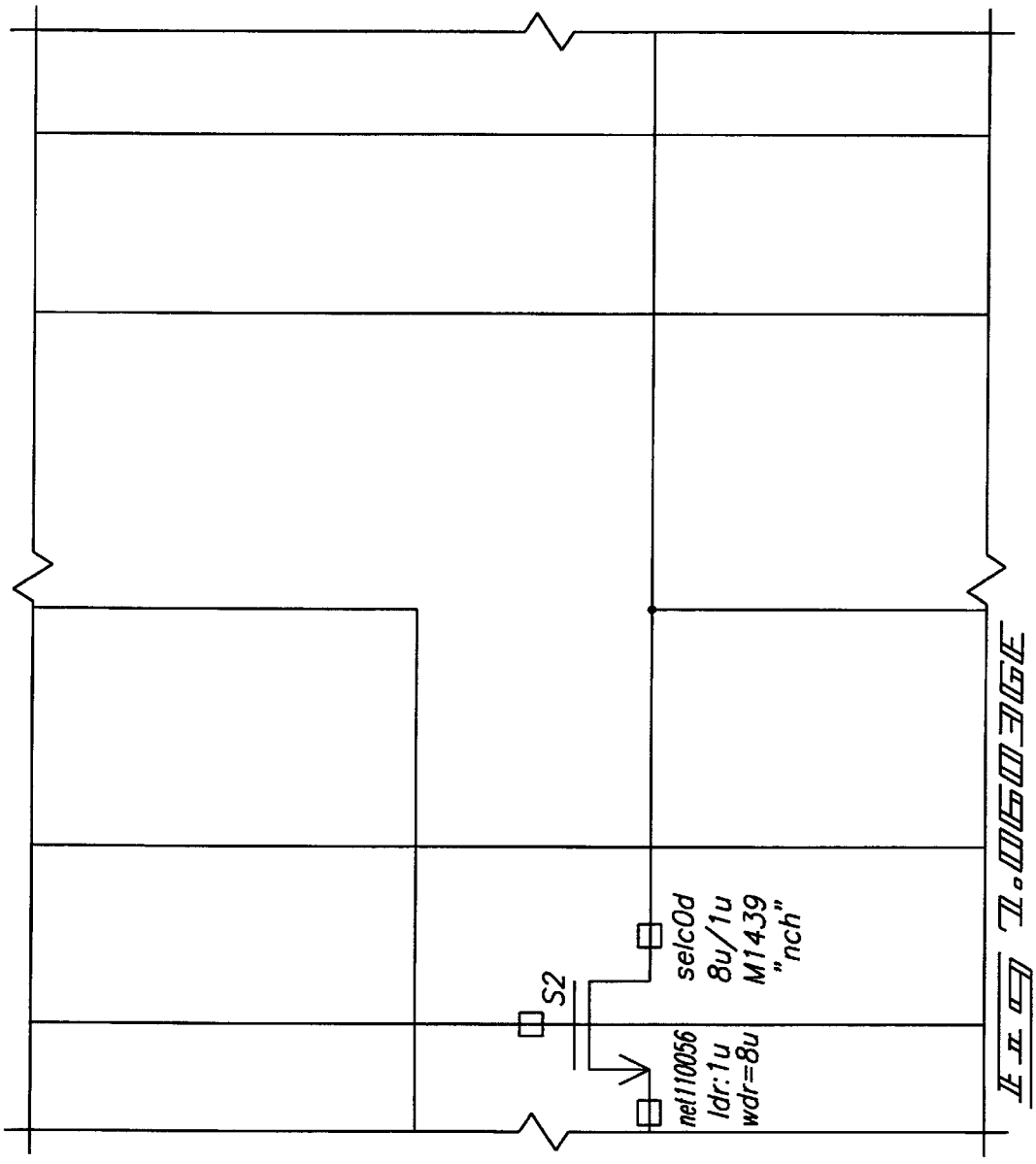
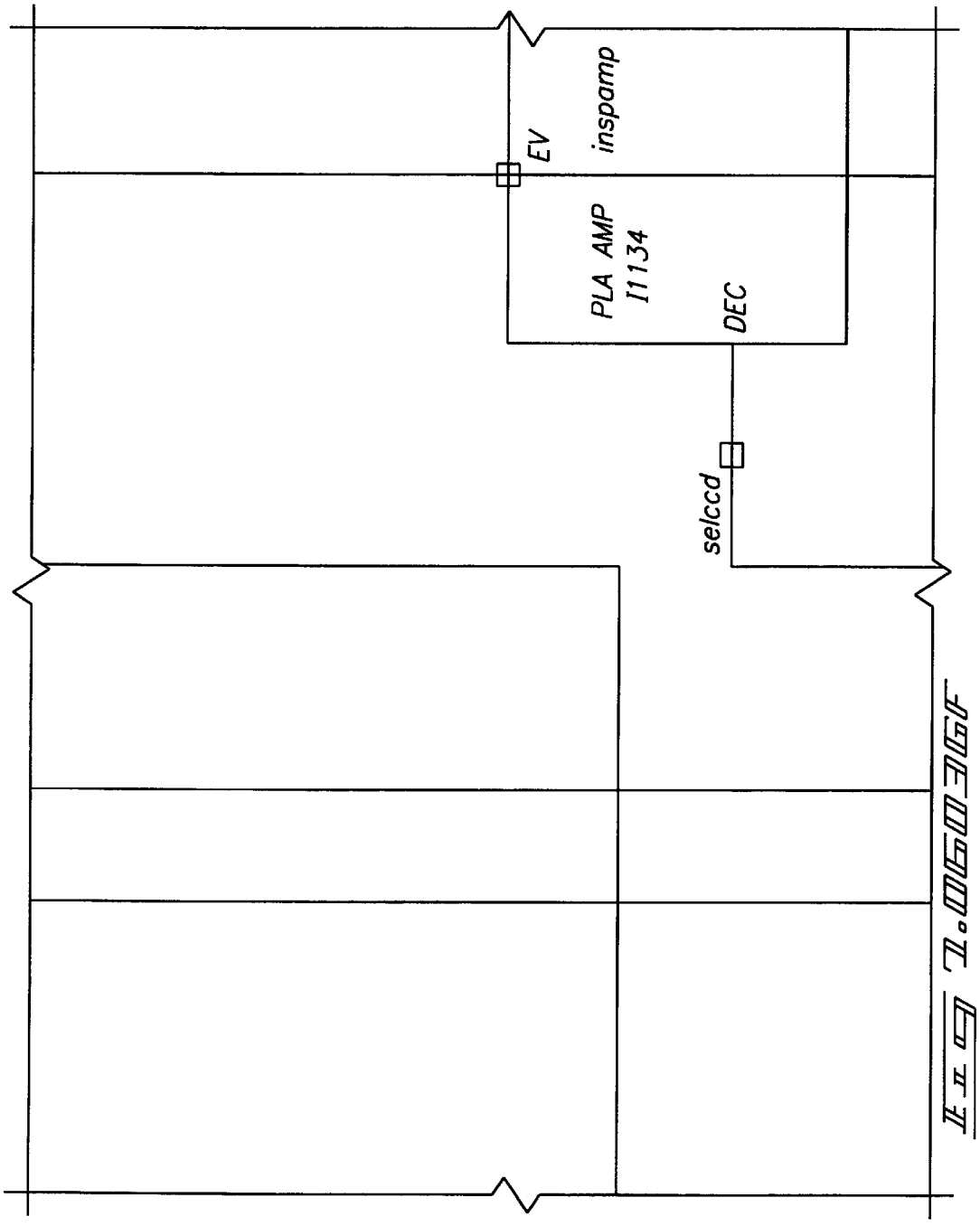
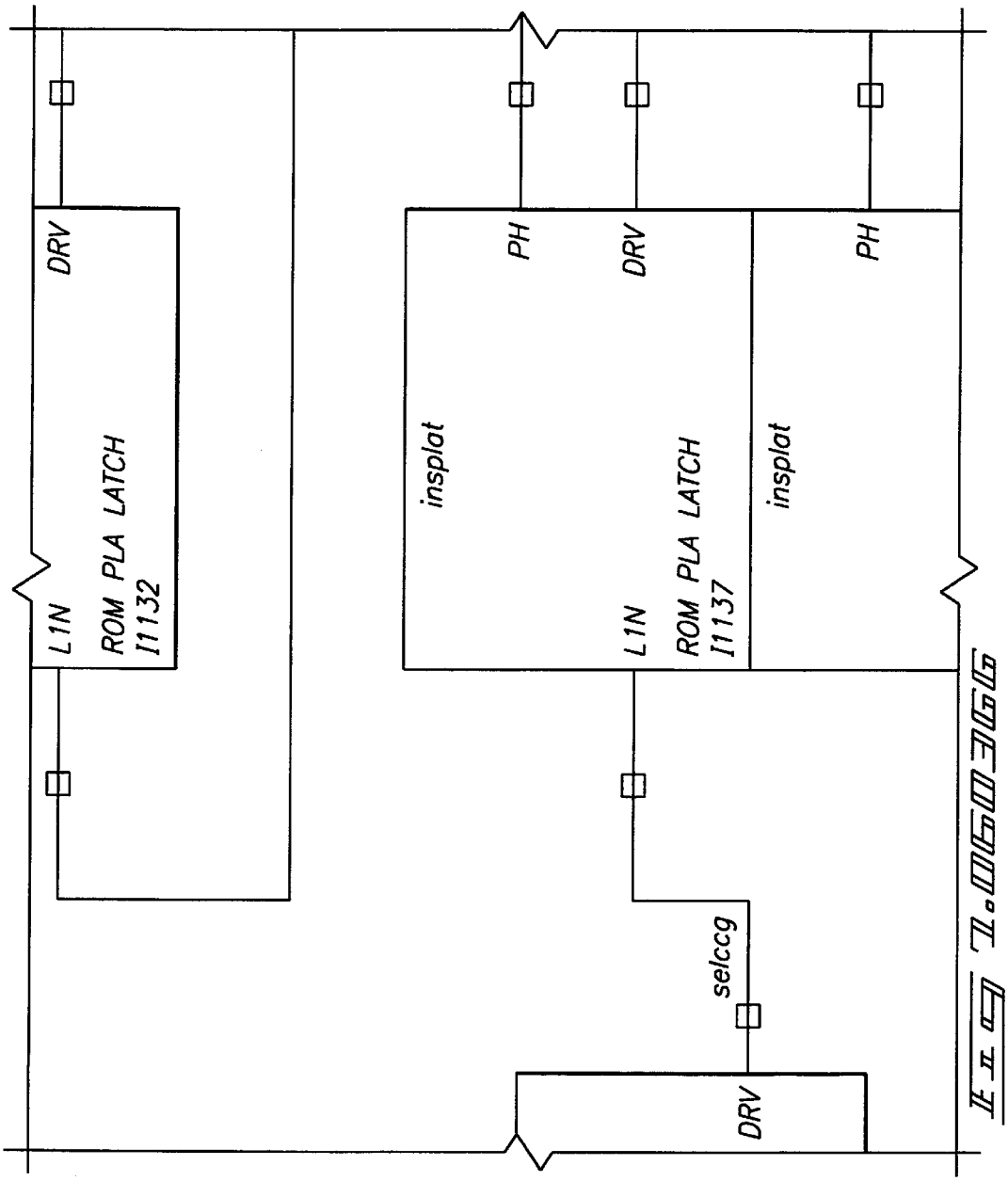


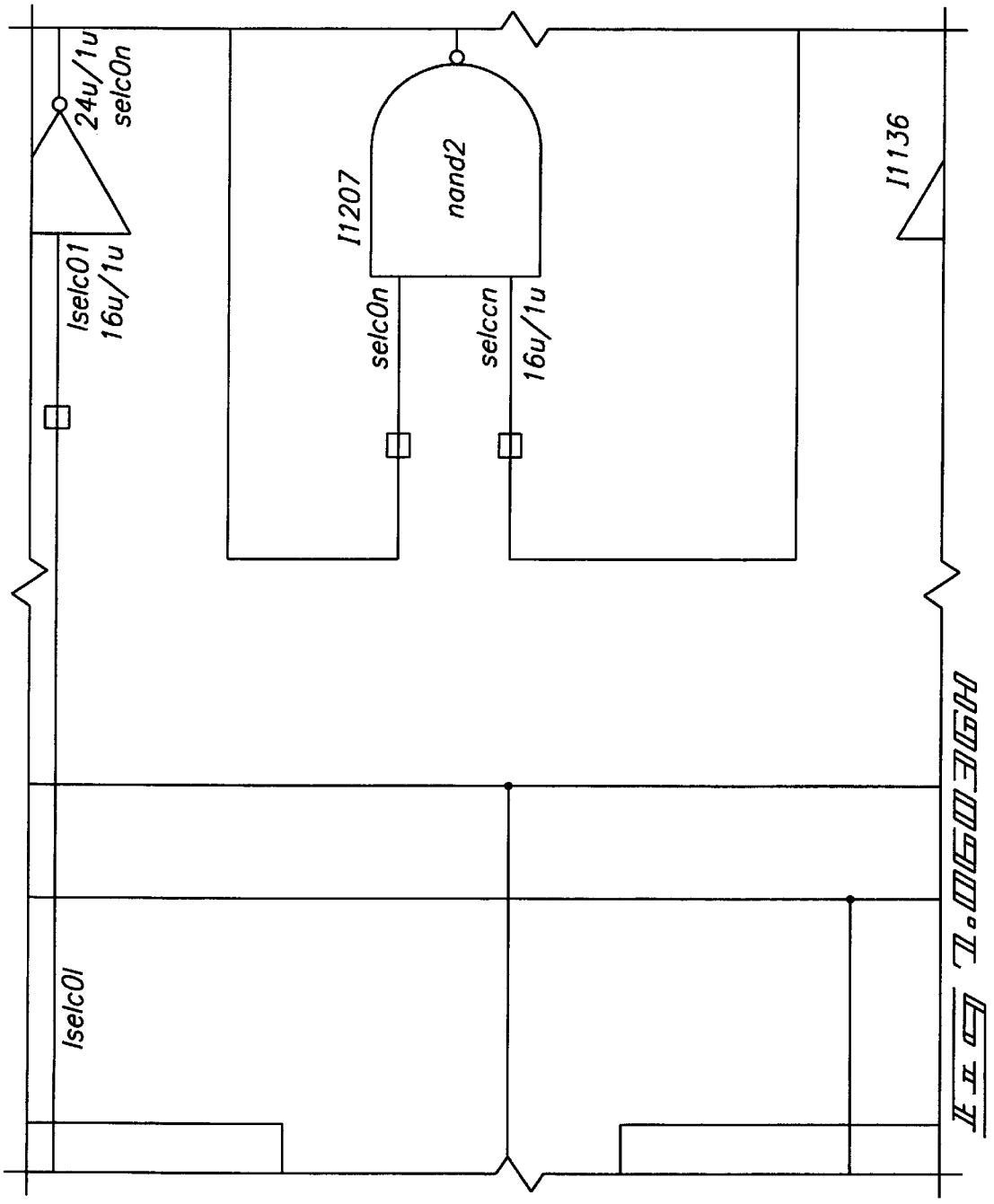
FIG. 703E

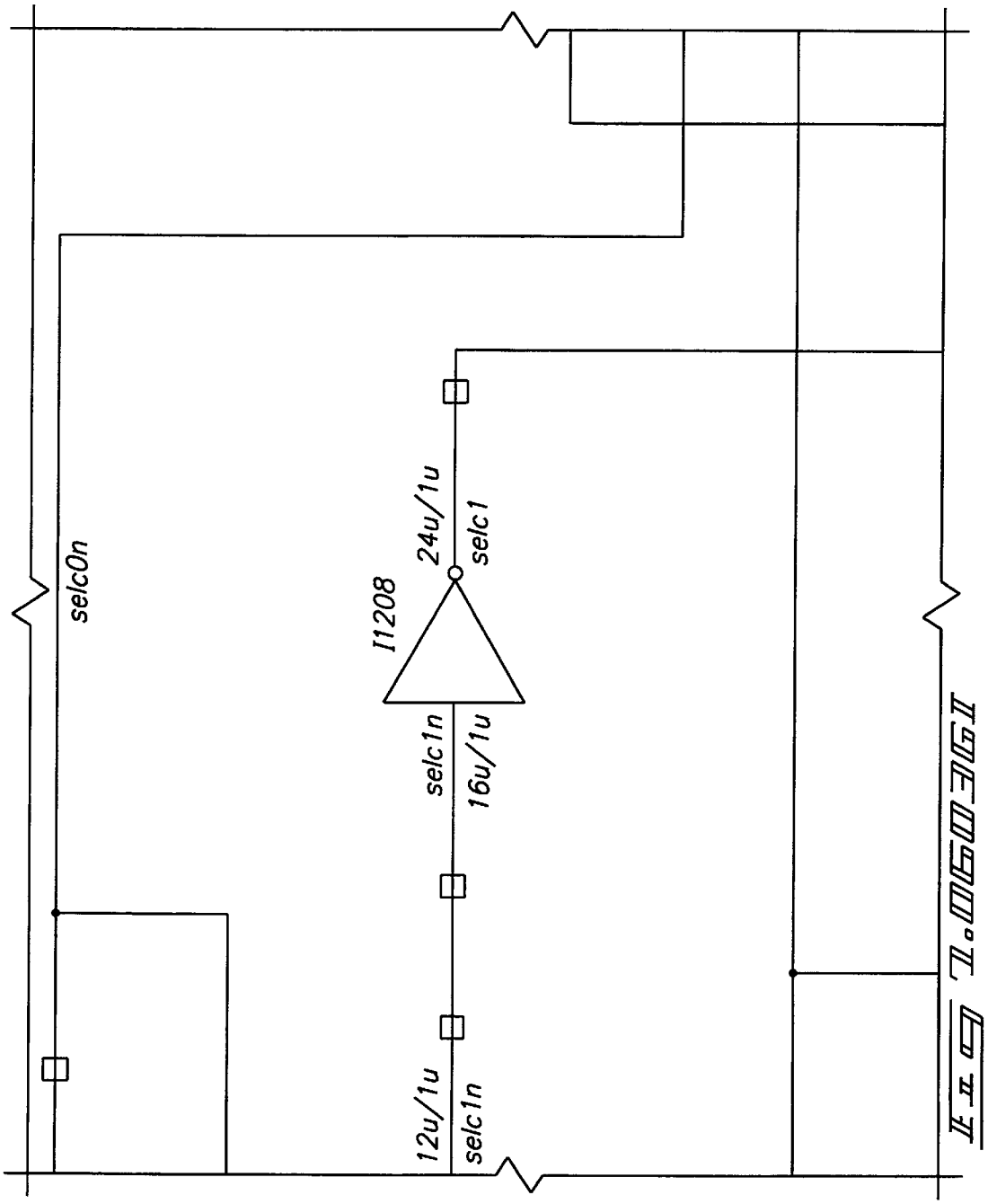

S4
ldcryd
8u/1u
M1436
"nch"
net107094
ldr:1u
wdr=8u
C1
net107094
8u/1u
M1437
"nch"
net110056
8u/1u
M1438
"nch"
C1
net41541
ldr:1u
wdr=8u
net41538
ldr:1u
wdr=8u
FIG. 704


selcOd
8u/1u
M1439
"nch"
S2
net110056
ldr:1u
wdr=8u
FIG. 705


EV
inspamp
PLA AMP
I1134
DEC
selccd
FIG 706.1


DRV
L1N
ROM PLA LATCH
I1132
PH
DRV
PH
insplat
L1N
ROM PLA LATCH
I1137
insplat
selccg
DRV
FIG. 1130E


24u/1u
selc0n
I1207
nand2
I1136
Iselc01
16u/1u
selc0n
selccn
16u/1u
Iselc0l
HSDE050U.L 5.7T


selcOn
I1208
24u/1u
selc1
selc1n
16u/1u
12u/1u
selc1n
VSS
VDD

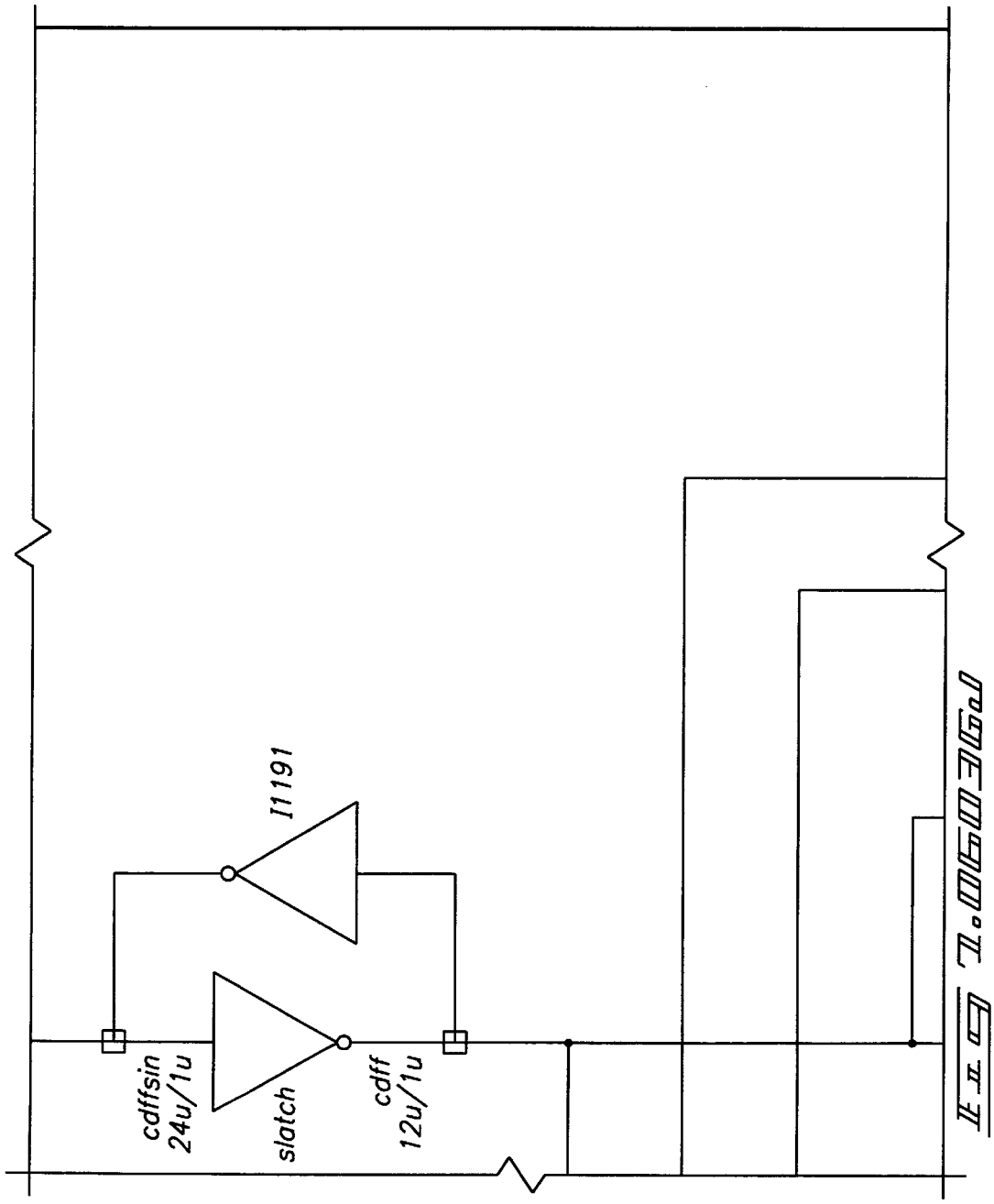


FIG. 709

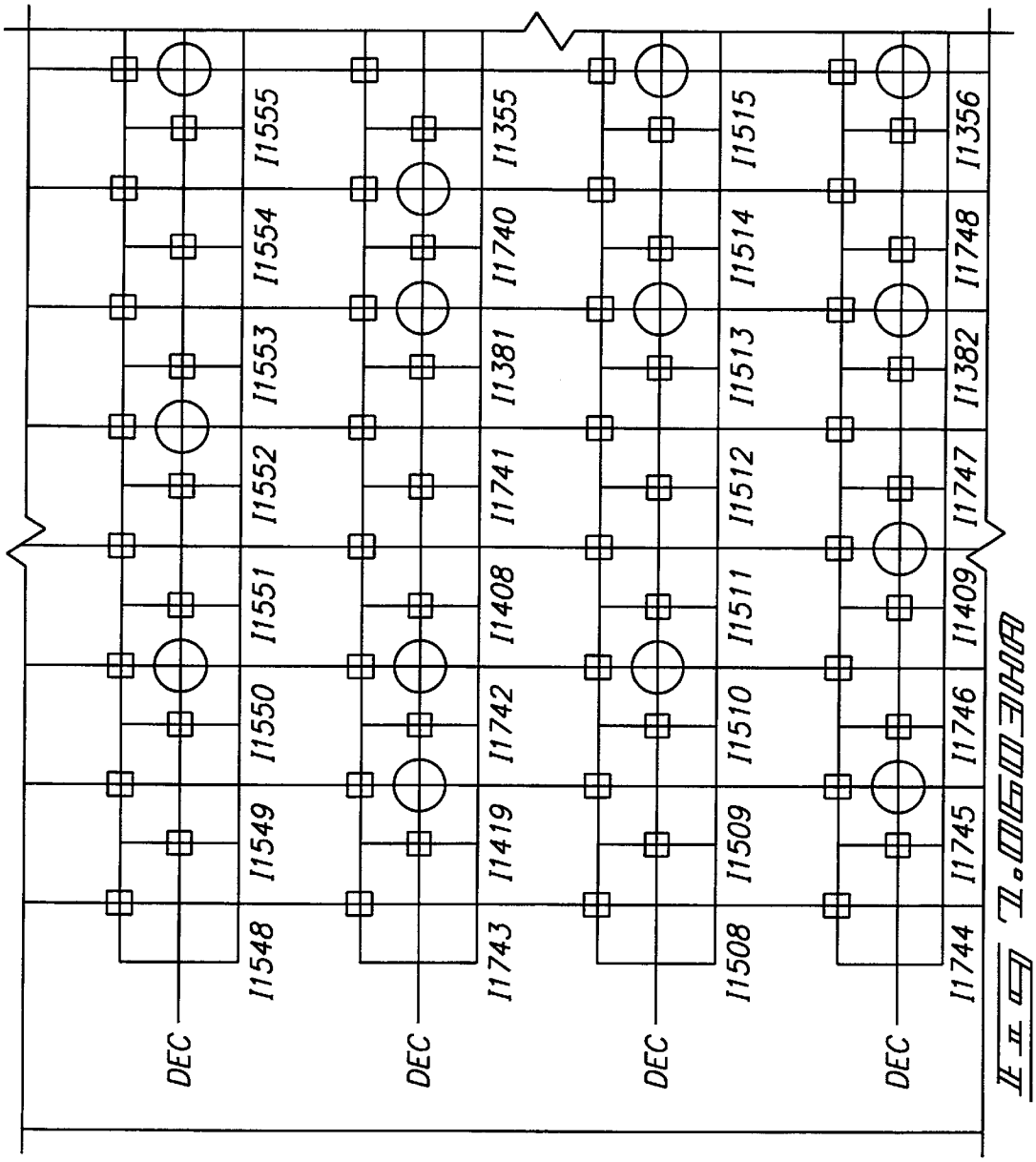
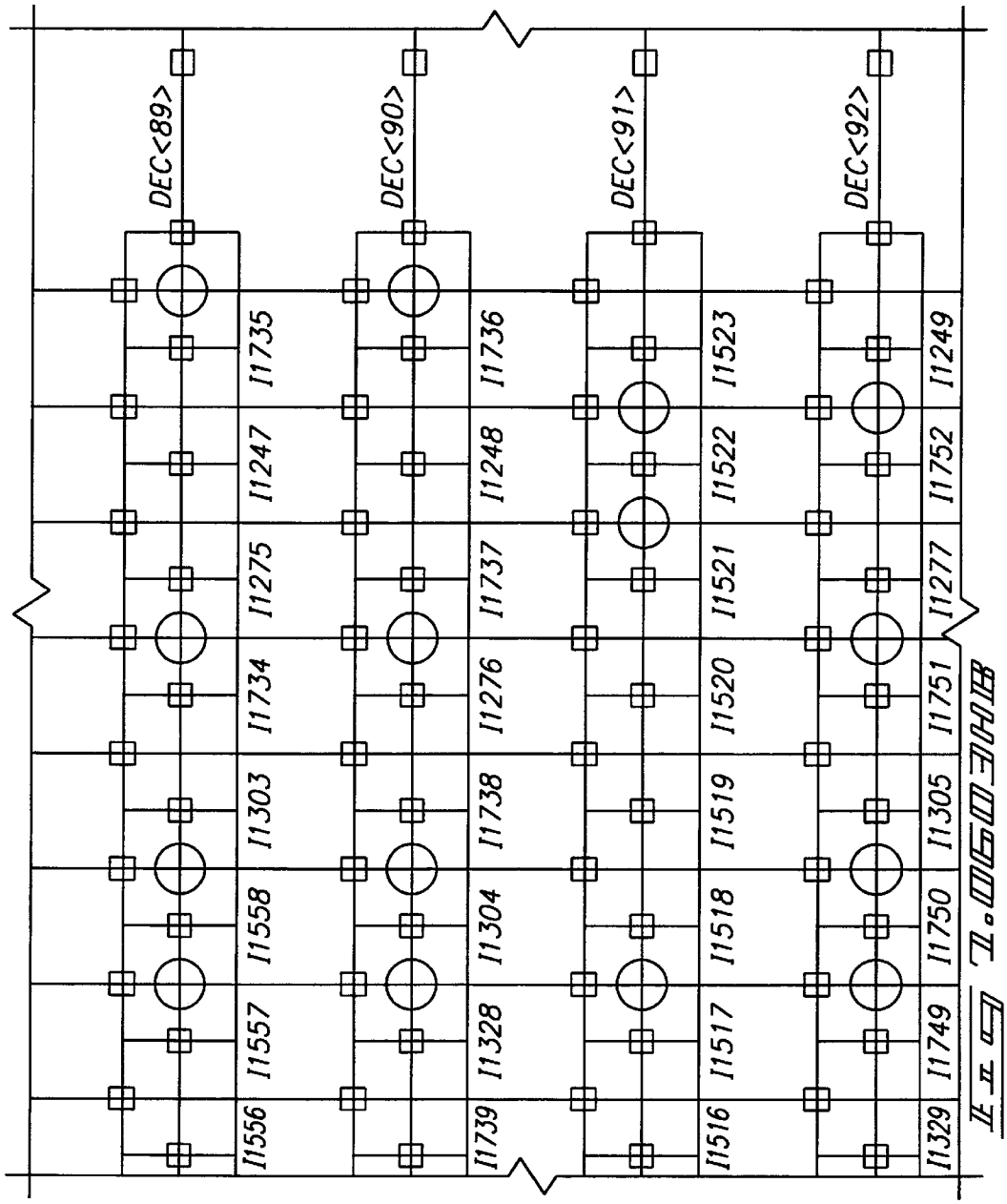

DEC
I1548
I1549
I1550
I1551
I1552
I1553
I1554
I1555
I1743
I1419
I1742
I1408
I1741
I1381
I1740
I1355
I1508
I1509
I1510
I1511
I1512
I1513
I1514
I1515
I1744
I1745
I1746
I1409
I1747
I1382
I1748
I1356

FIG. 711


DEC<89>
DEC<90>
DEC<91>
DEC<92>
I1735
I1247
I1275
I1734
I1303
I1558
I1557
I1556
I1736
I1248
I1737
I1276
I1738
I1304
I1328
I1739
I1523
I1522
I1521
I1520
I1519
I1518
I1517
I1516
I1249
I1752
I1277
I1751
I1305
I1750
I1749
I1329

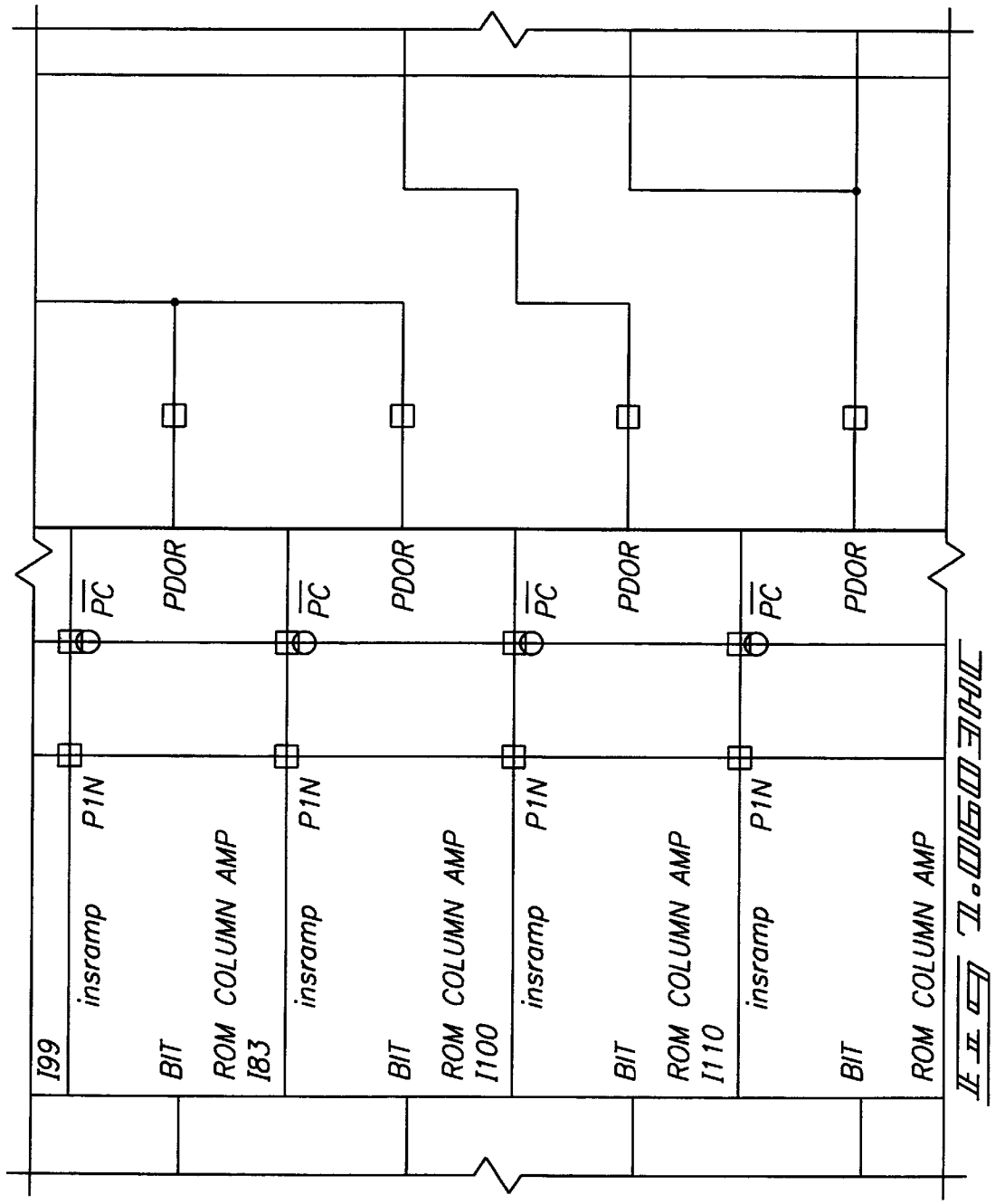
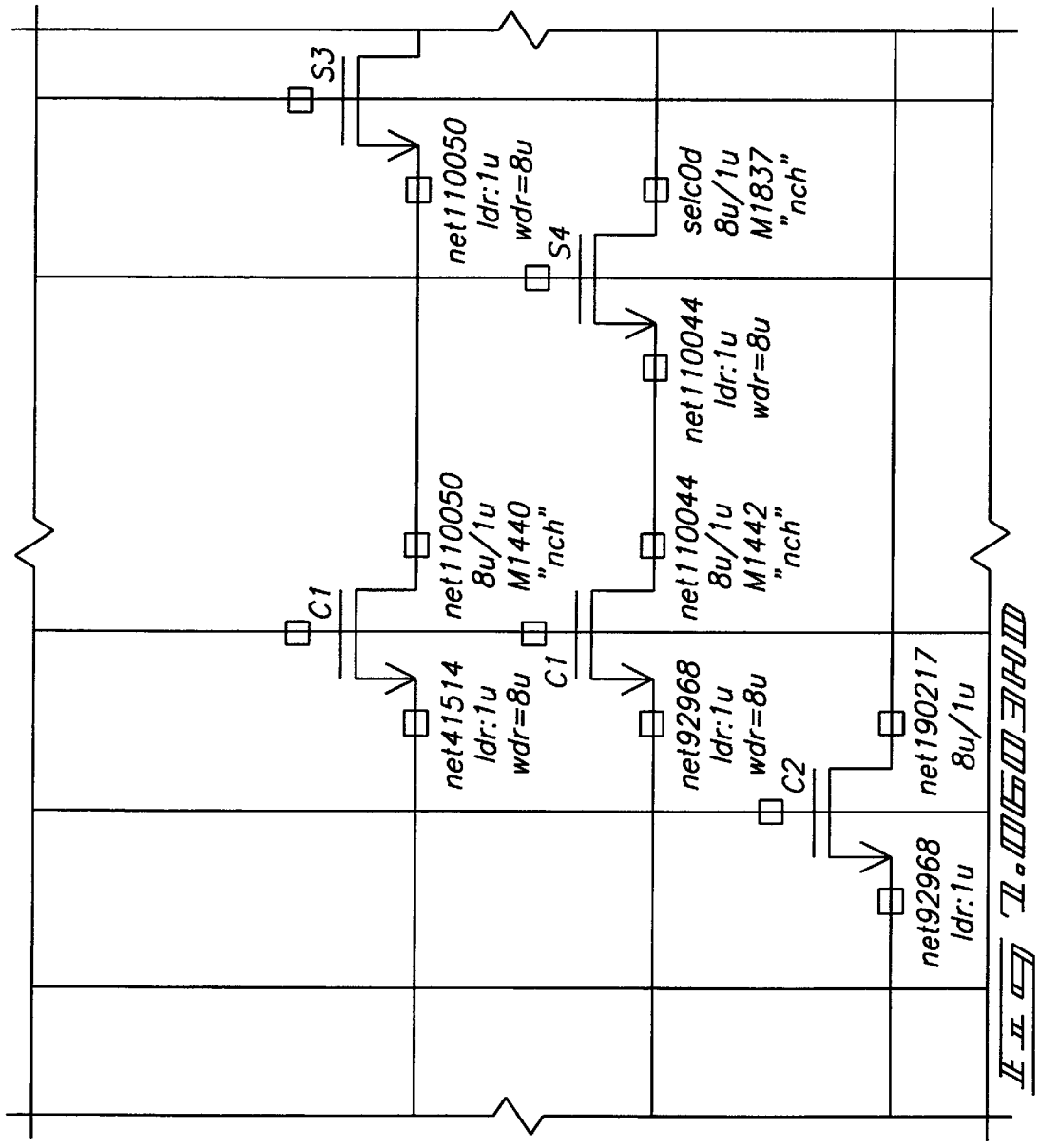
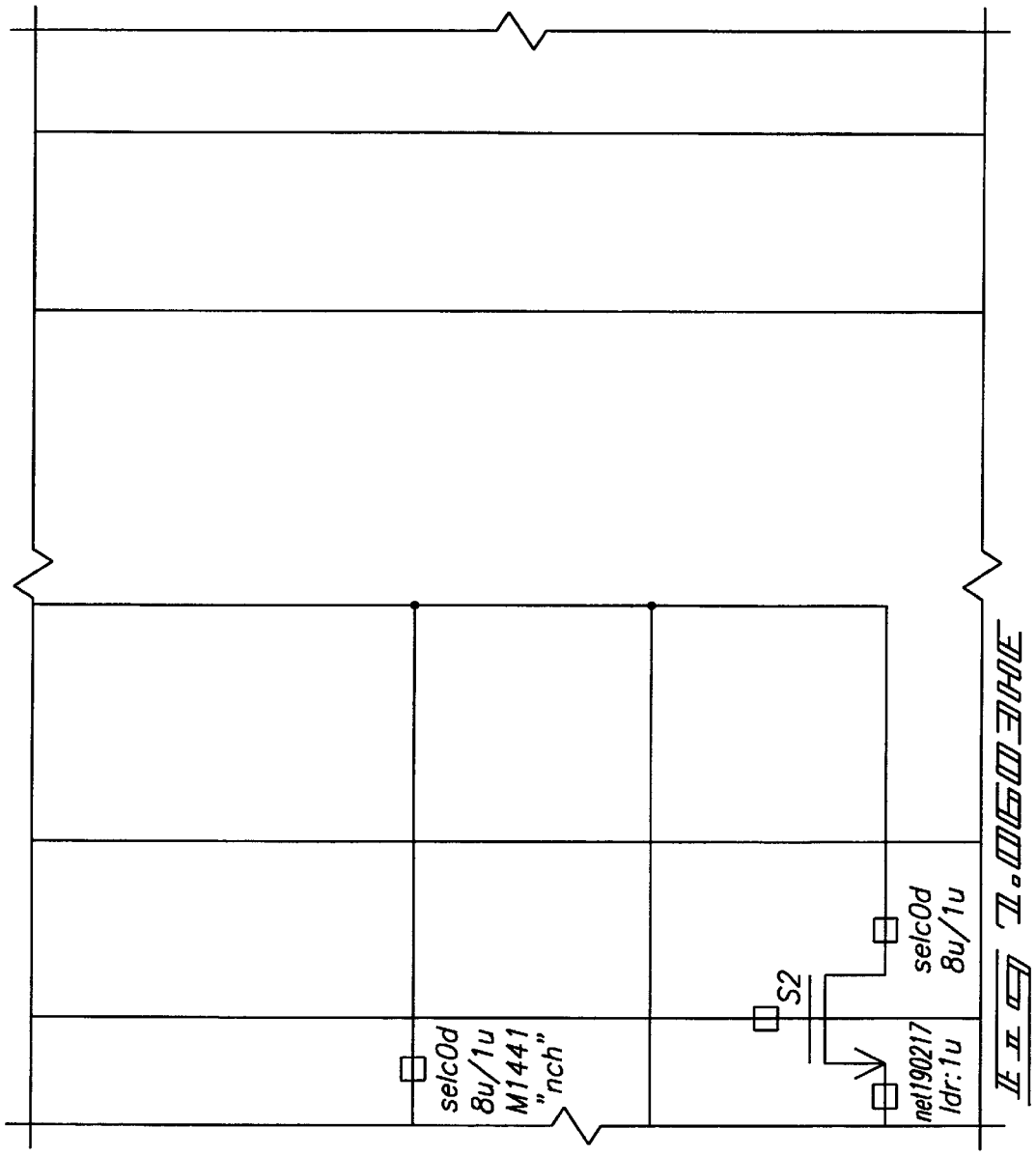
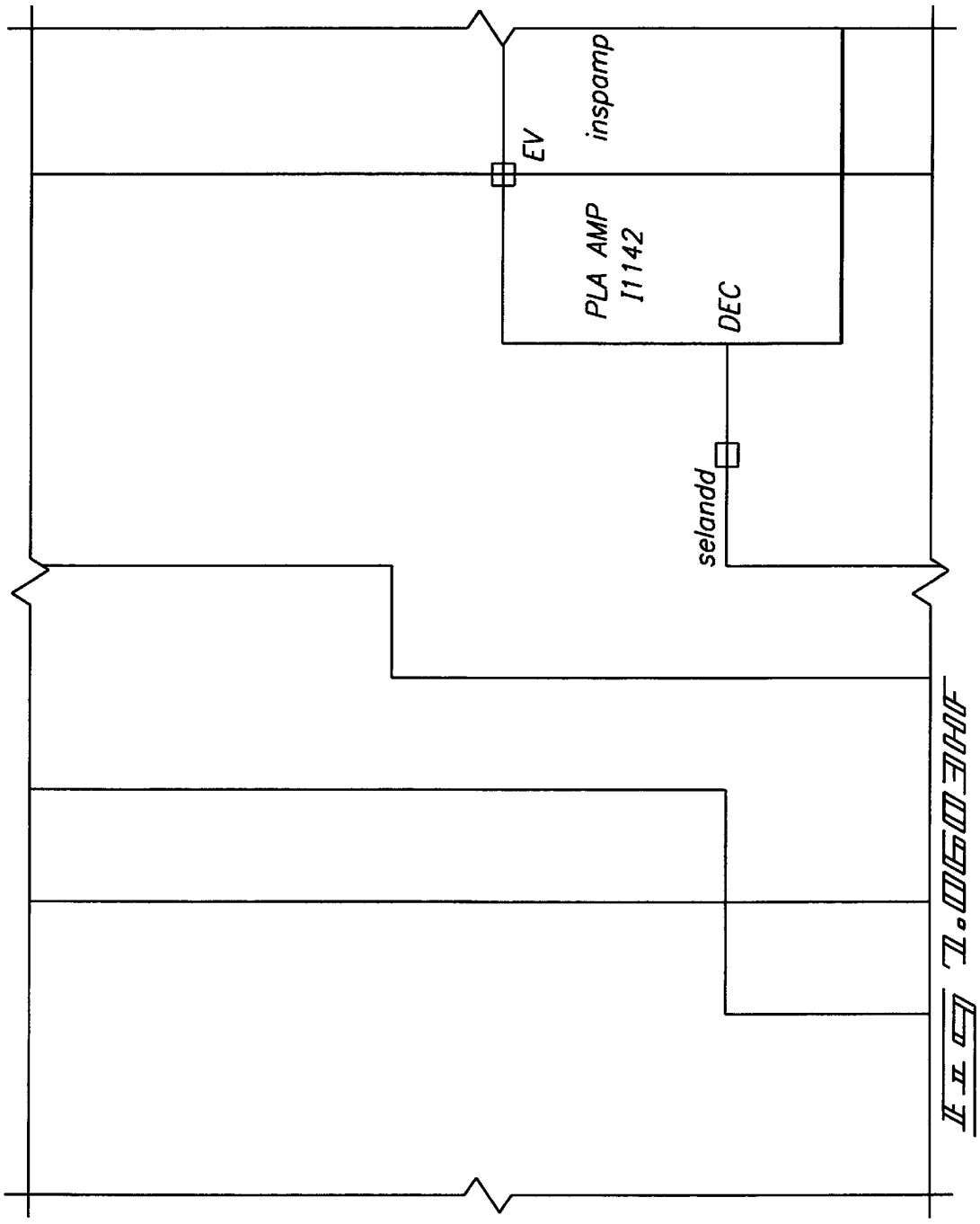
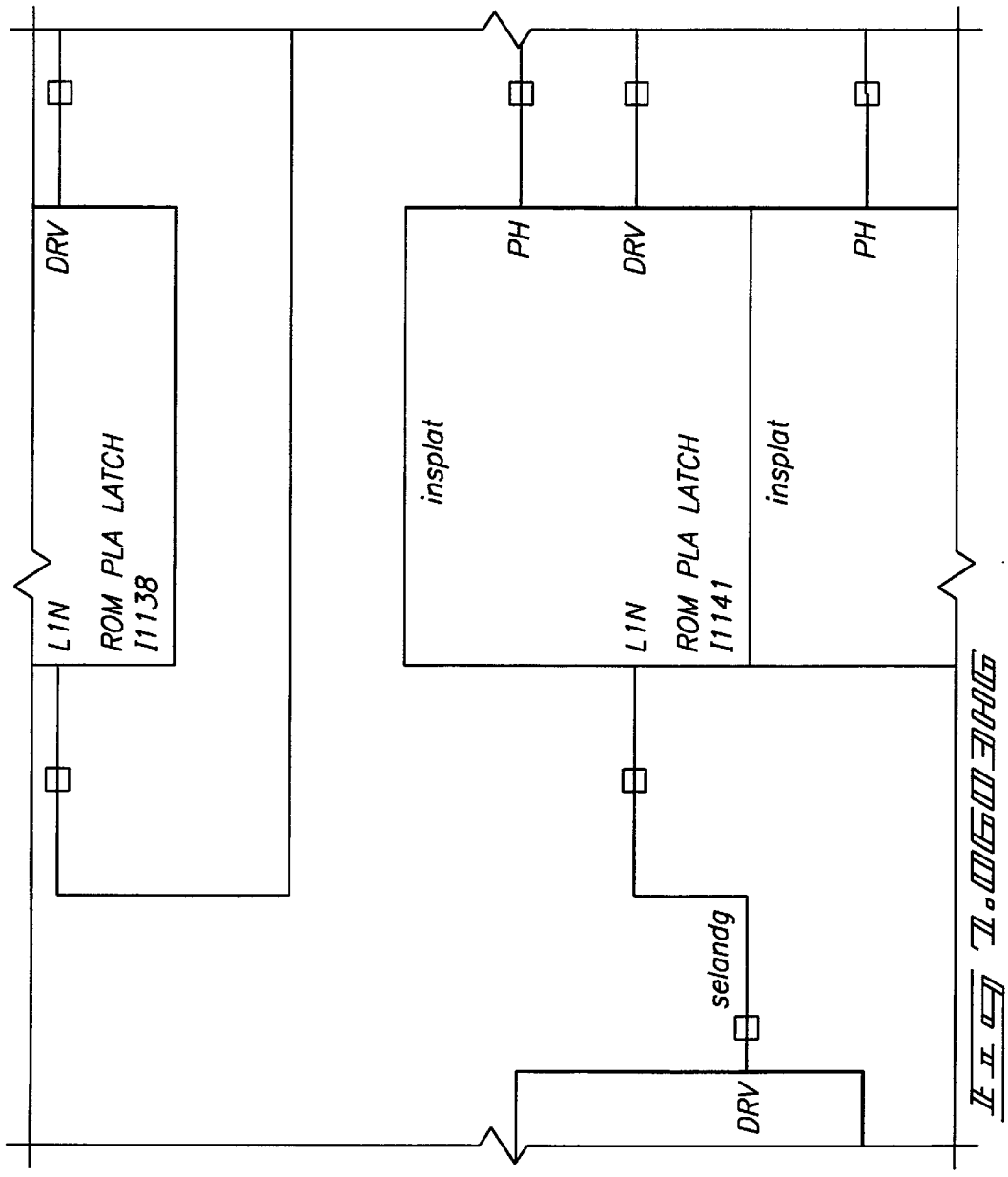


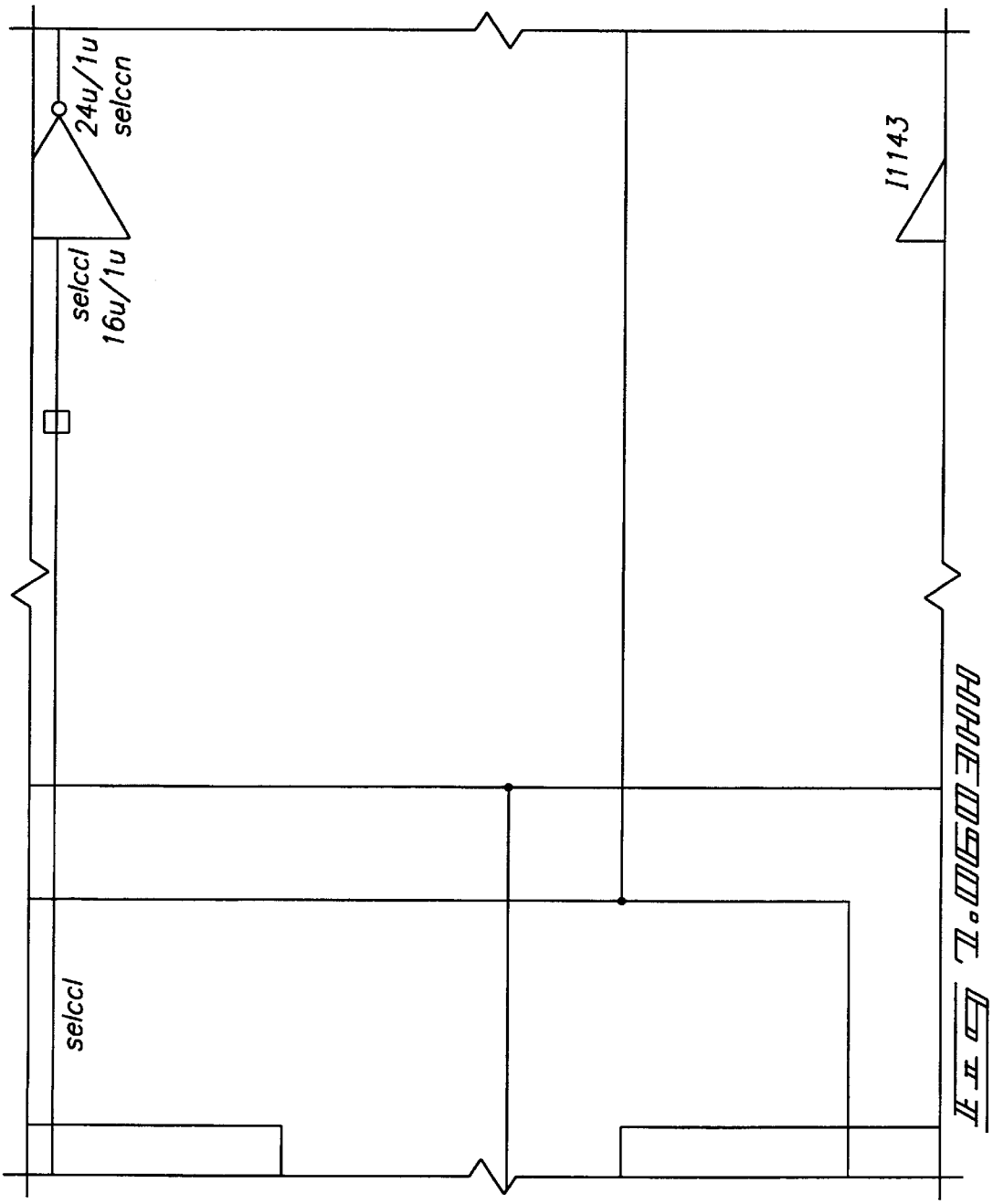
FIG. 713

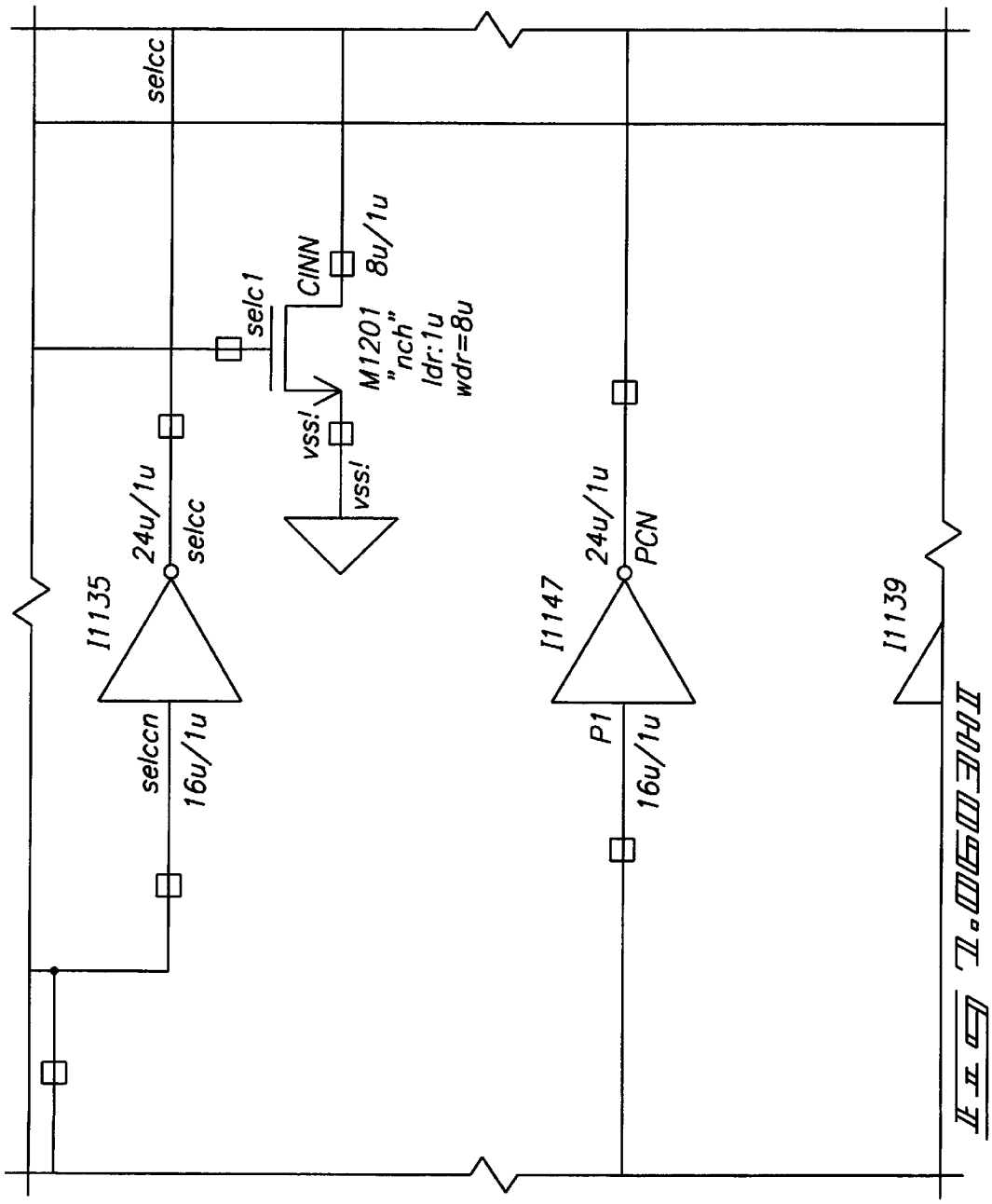

S3
net110050
ldr:1u
wdr=8u
S4
selc0d
8u/1u
M1837
"nch"
net110044
ldr:1u
wdr=8u
net110050
8u/1u
M1440
"nch"
net110044
8u/1u
M1442
"nch"
C1
C1
net41514
ldr:1u
wdr=8u
net92968
ldr:1u
wdr=8u
C2
net190217
8u/1u
net92968
ldr:1u
FIG. 59

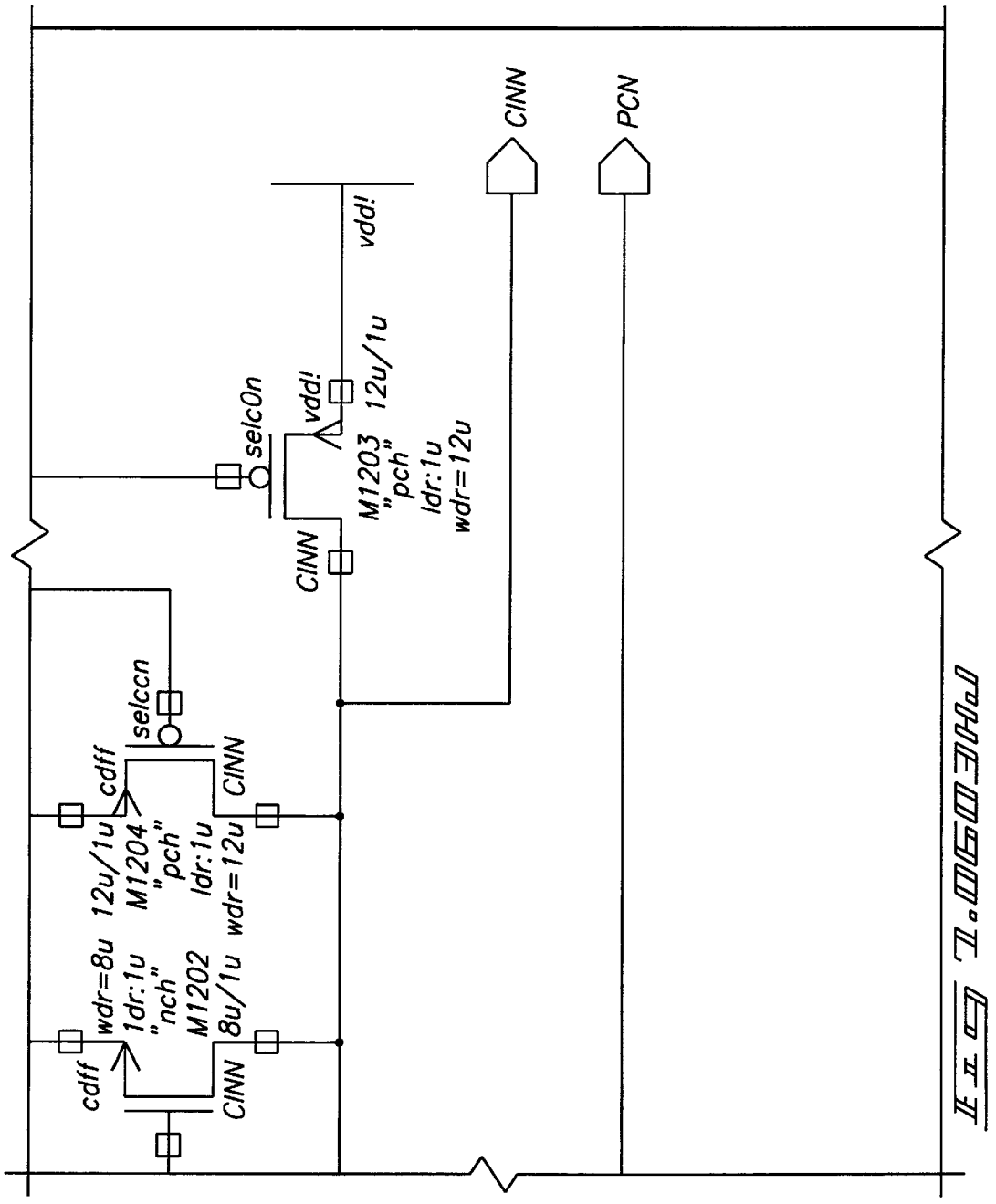

selc0d
8u/1u
M1441
"nch"
S2
selc0d
8u/1u
net190217
ldr:1u


inspamp
EV
PLA AMP
I1142
DEC
selandd
FIG. 5000.71


DRV
L1N
ROM PLA LATCH
I1138
PH
DRV
PH
insplat
L1N
ROM PLA LATCH
I1141
insplat
selandg
DRV
FIG 59.1


24u/1u
selccn
selccl
16u/1u
selccl
I1143
FIG. 718


selcc
selc1
CINN
8u/1u
M1201
"nch"
ldr:1u
wdr=8u
vss!
vss!
24u/1u
selcc
I1135
selccn
16u/1u
24u/1u
PCN
I1147
P1
16u/1u
I1139
THE DOOR'L


CINN
PCN
vdd!
selc0n
vdd!
12u/1u
M1203
"pch"
ldr:1u
wdr=12u
CINN
selccn
cdff
12u/1u
M1204
"pch"
ldr:1u
wdr=12u
CINN
cdff
wdr=8u
1dr:1u
"nch"
M1202
8u/1u
CINN

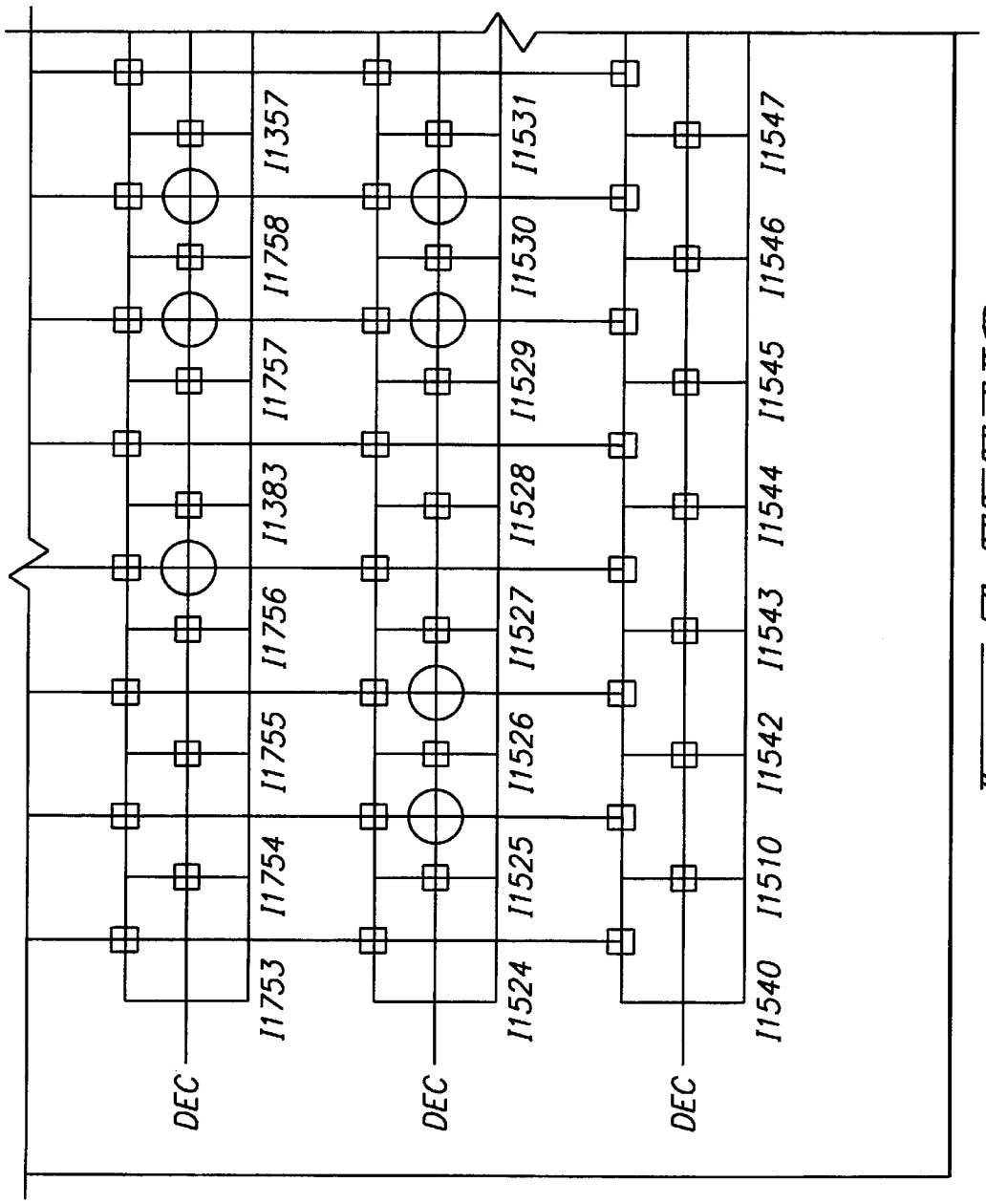

DEC
DEC
DEC
I1753
I1754
I1755
I1756
I1383
I1757
I1758
I1357
I1524
I1525
I1526
I1527
I1528
I1529
I1530
I1531
I1540
I1510
I1542
I1543
I1544
I1545
I1546
I1547

FIG. 1130.0

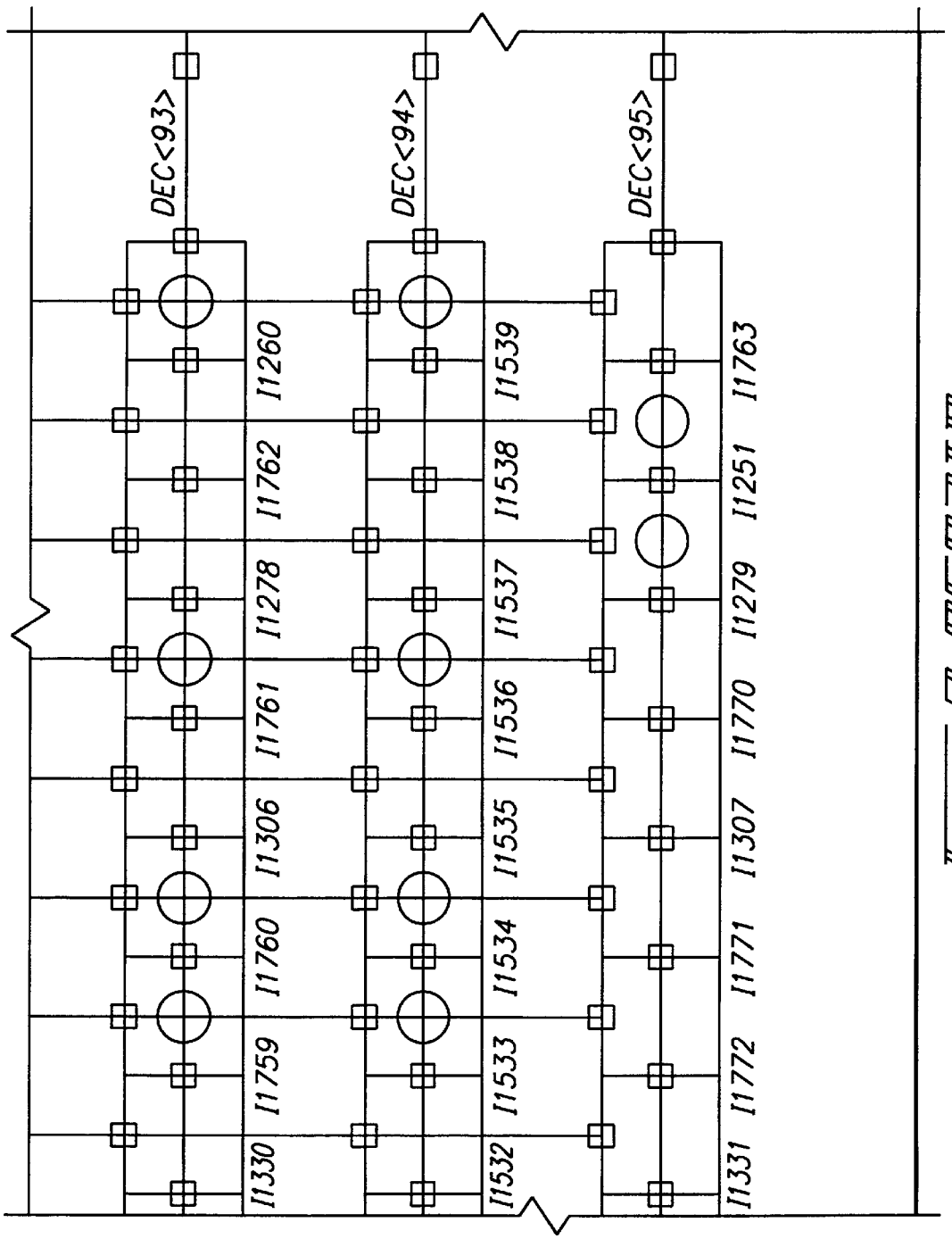

DEC<93>
DEC<94>
DEC<95>
I1260
I1762
I1278
I1761
I1306
I1760
I1759
I1330
I1539
I1538
I1537
I1536
I1535
I1534
I1533
I1532
I1763
I1251
I1279
I1770
I1307
I1771
I1772
I1331

FIG 90.1E

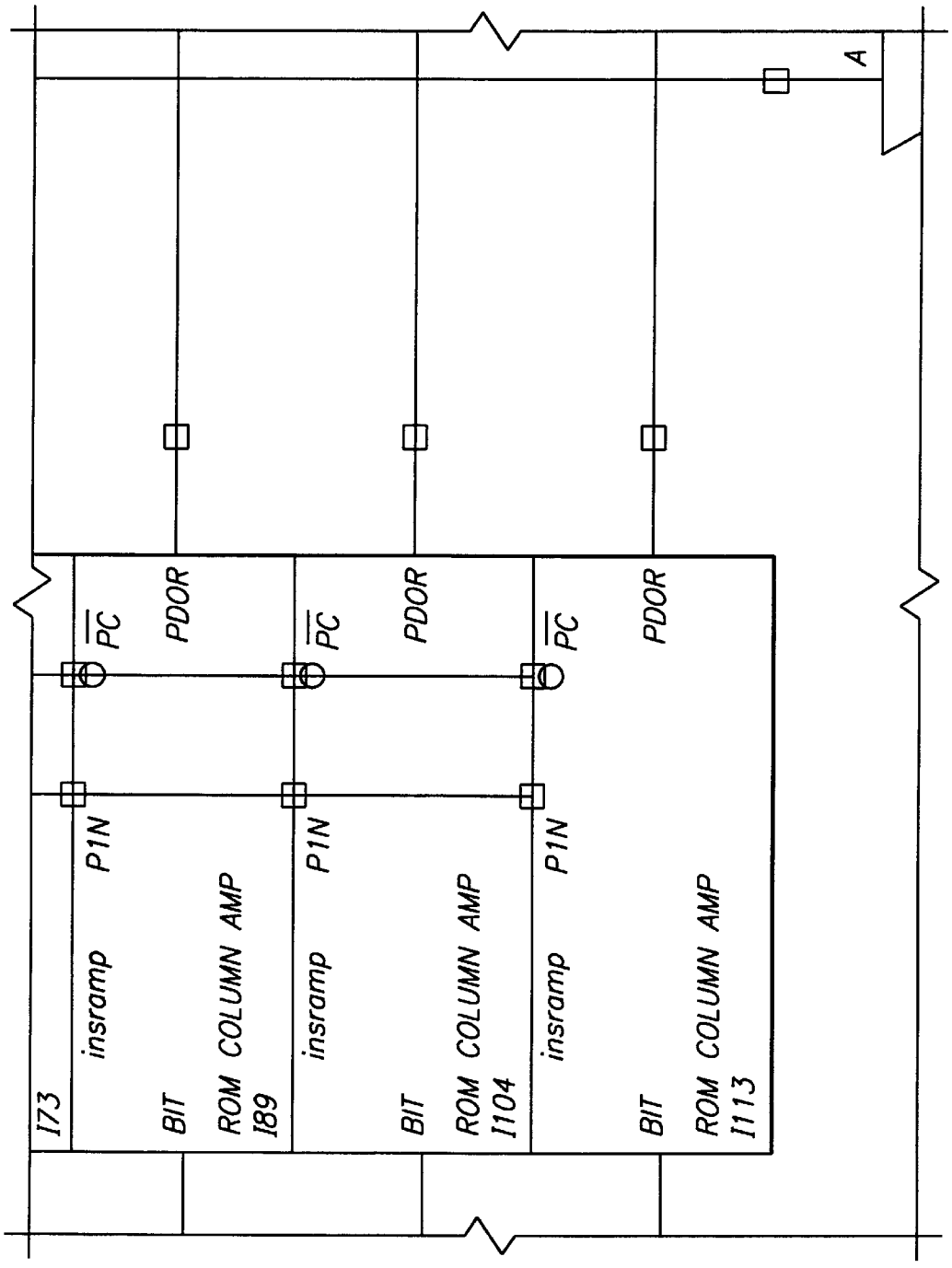


FIG. 69E

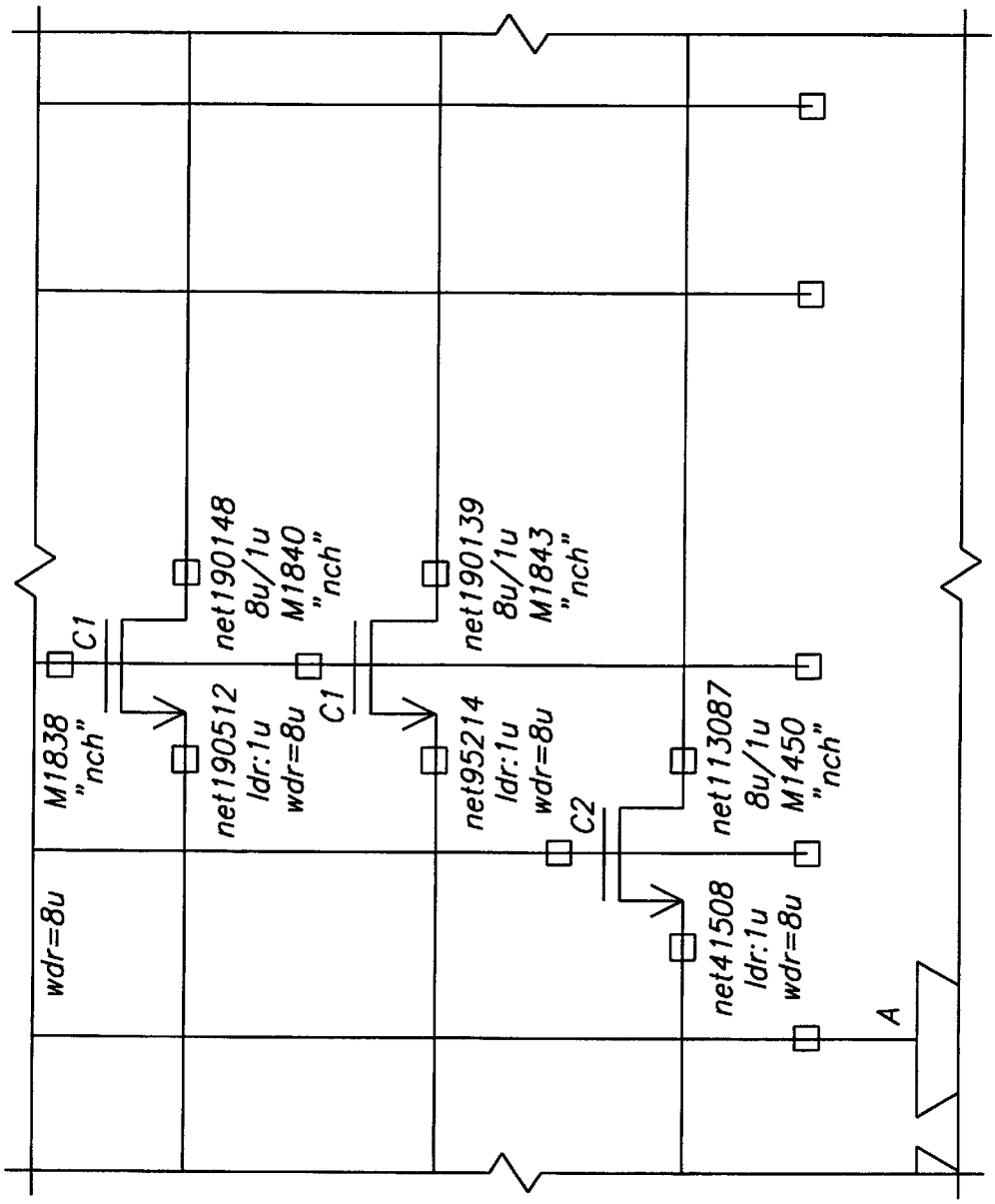
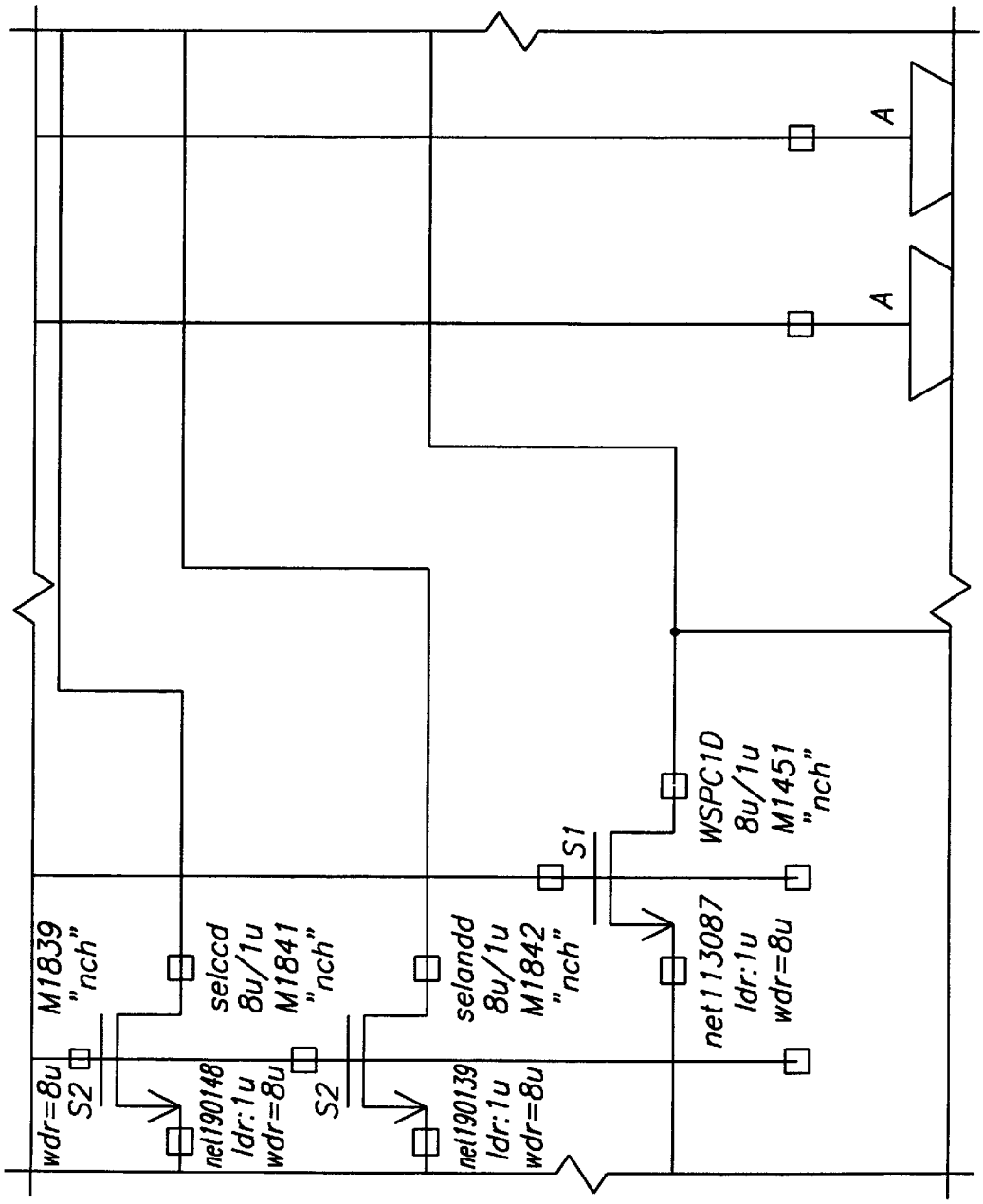


FIG. 709.7L
M1838 "nch"
wdr=8u
C1
net190512 ldr:1u wdr=8u
net190148 8u/1u M1840 "nch"
C1
net95214 ldr:1u wdr=8u
net190139 8u/1u M1843 "nch"
C2
net41508 ldr:1u wdr=8u
net113087 8u/1u M1450 "nch"
A


A
A
WSPC1D
8u/1u
M1451
"nch"
S1
M1839
"nch"
selccd
8u/1u
M1841
"nch"
selandd
8u/1u
M1842
"nch"
net113087
ldr:1u
wdr=8u
wdr=8u
S2
net190148
ldr:1u
wdr=8u
S2
net190139
ldr:1u
wdr=8u

ФИГ. 1,609,811

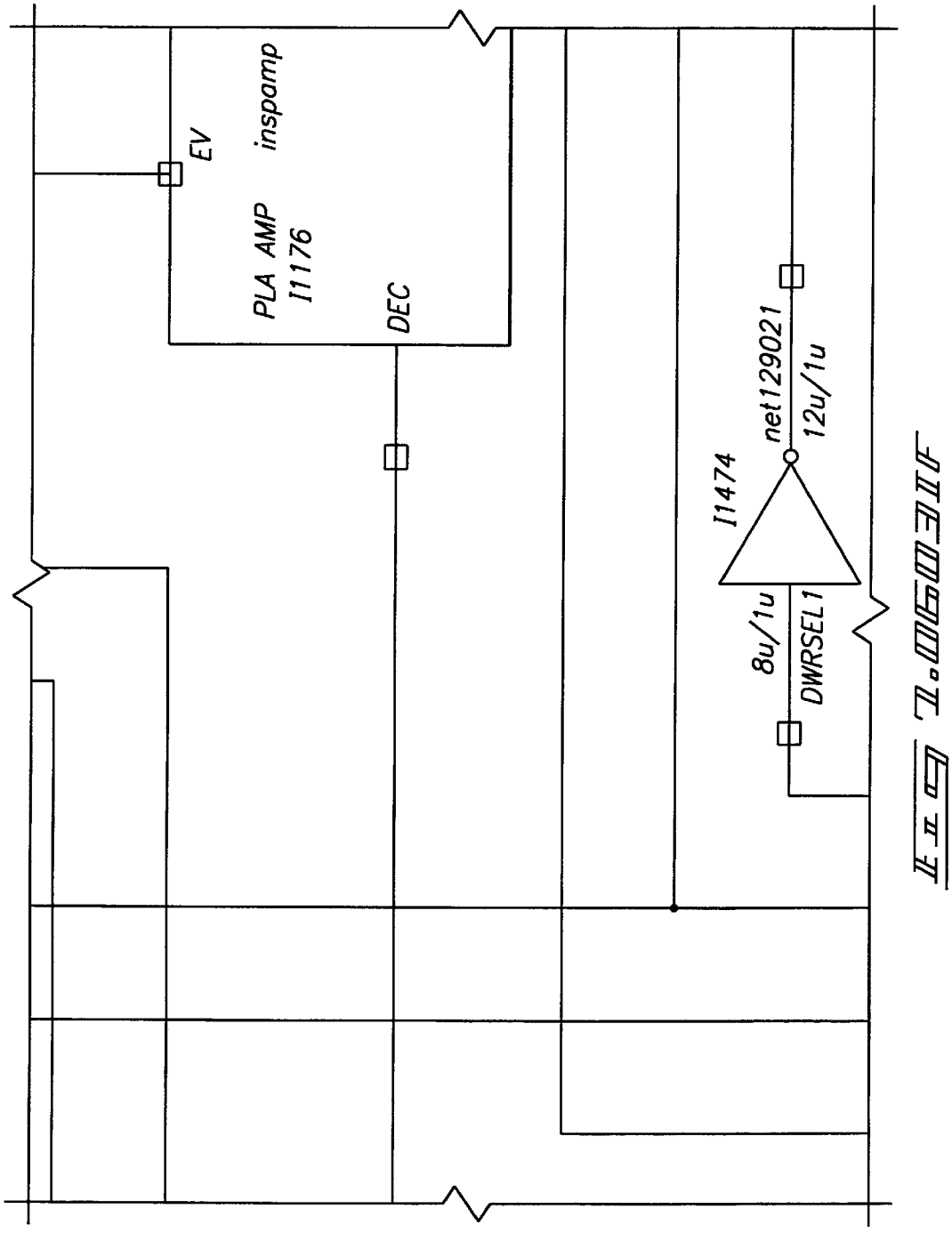

EV
inspamp
PLA AMP
I1176
DEC
I1474
net129021
12u/1u
8u/1u
DWRSEL1

FIG. 6,009,251

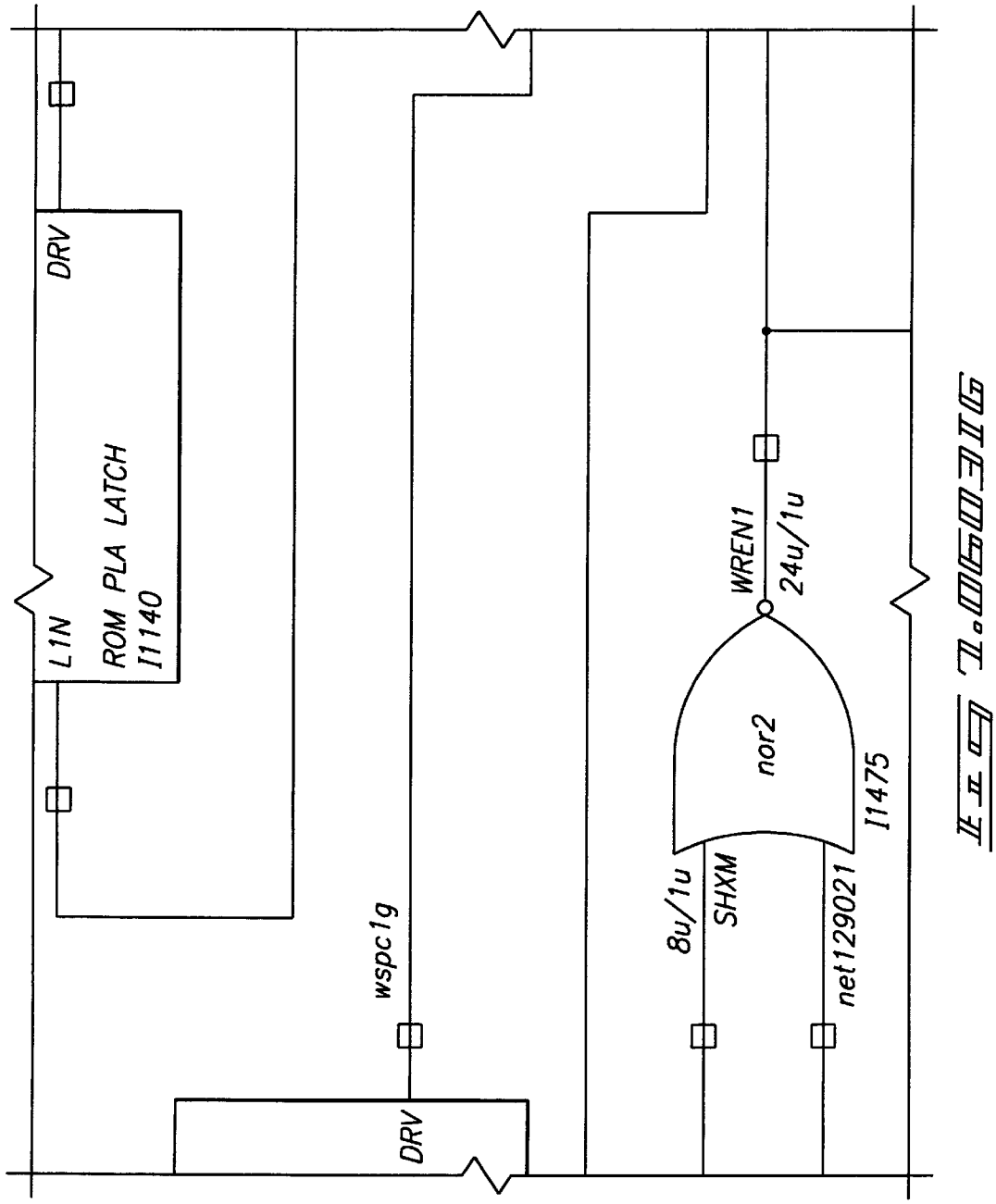

DRV
L1N
ROM PLA LATCH
I1140
wspc1g
DRV
WREN1
24u/1u
nor2
I1475
8u/1u
SHXM
net129021

FIG 731

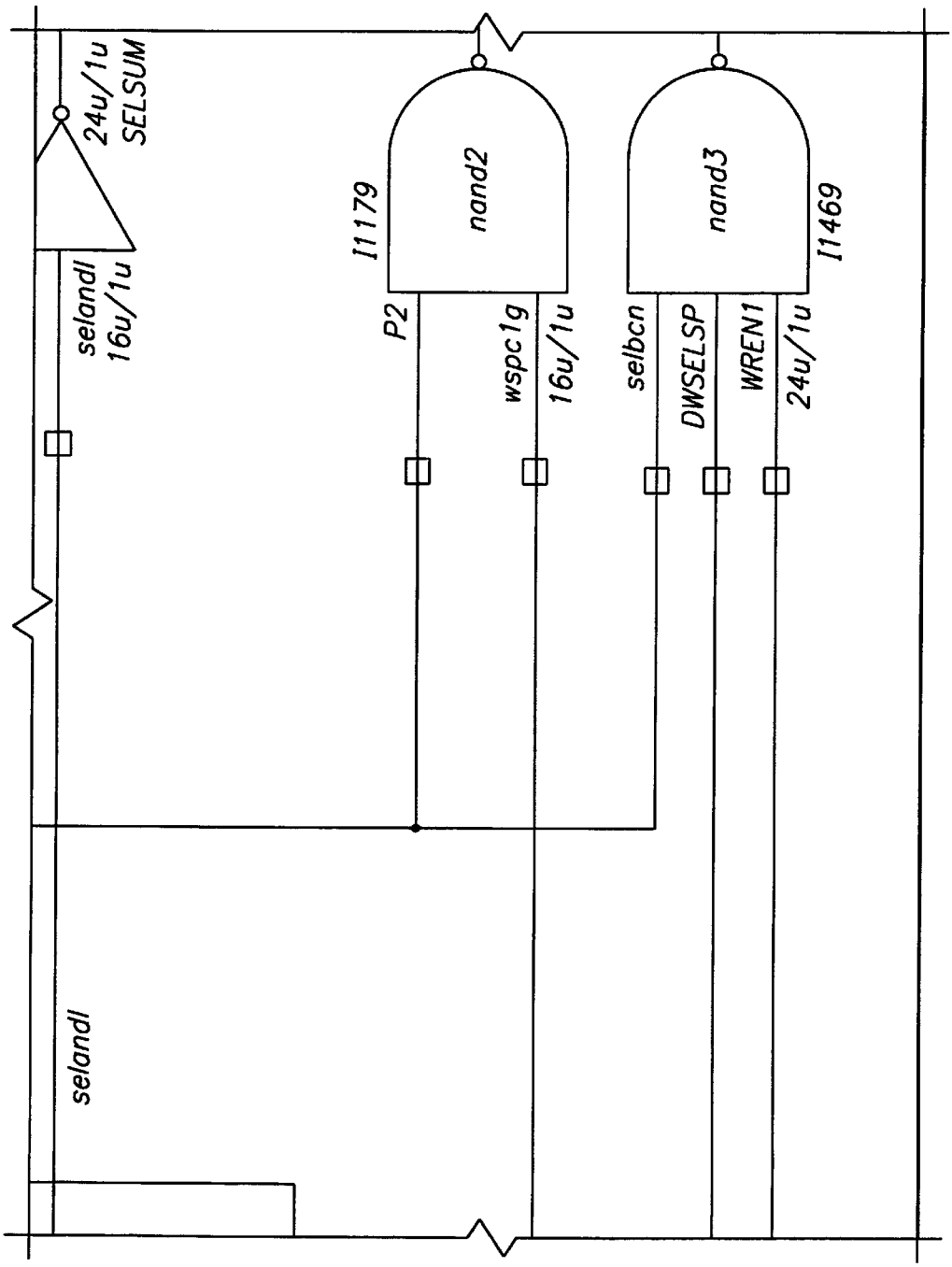

24u/1u
SELSUM
selandl
16u/1u
I1179
nand2
P2
wspc1g
16u/1u
nand3
I1469
selbcn
DWSELSP
WREN1
24u/1u
selandl

FIG 728.1

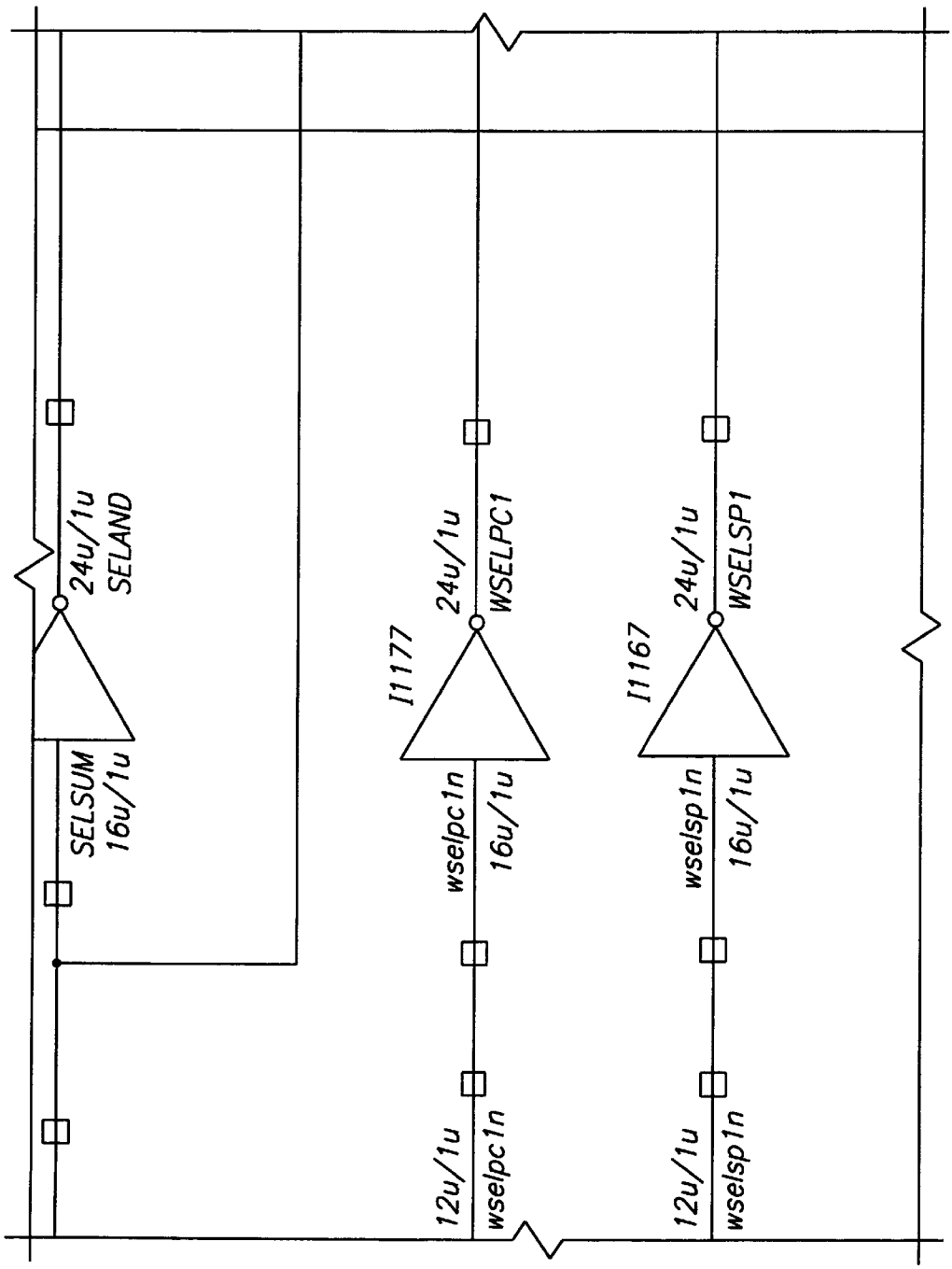
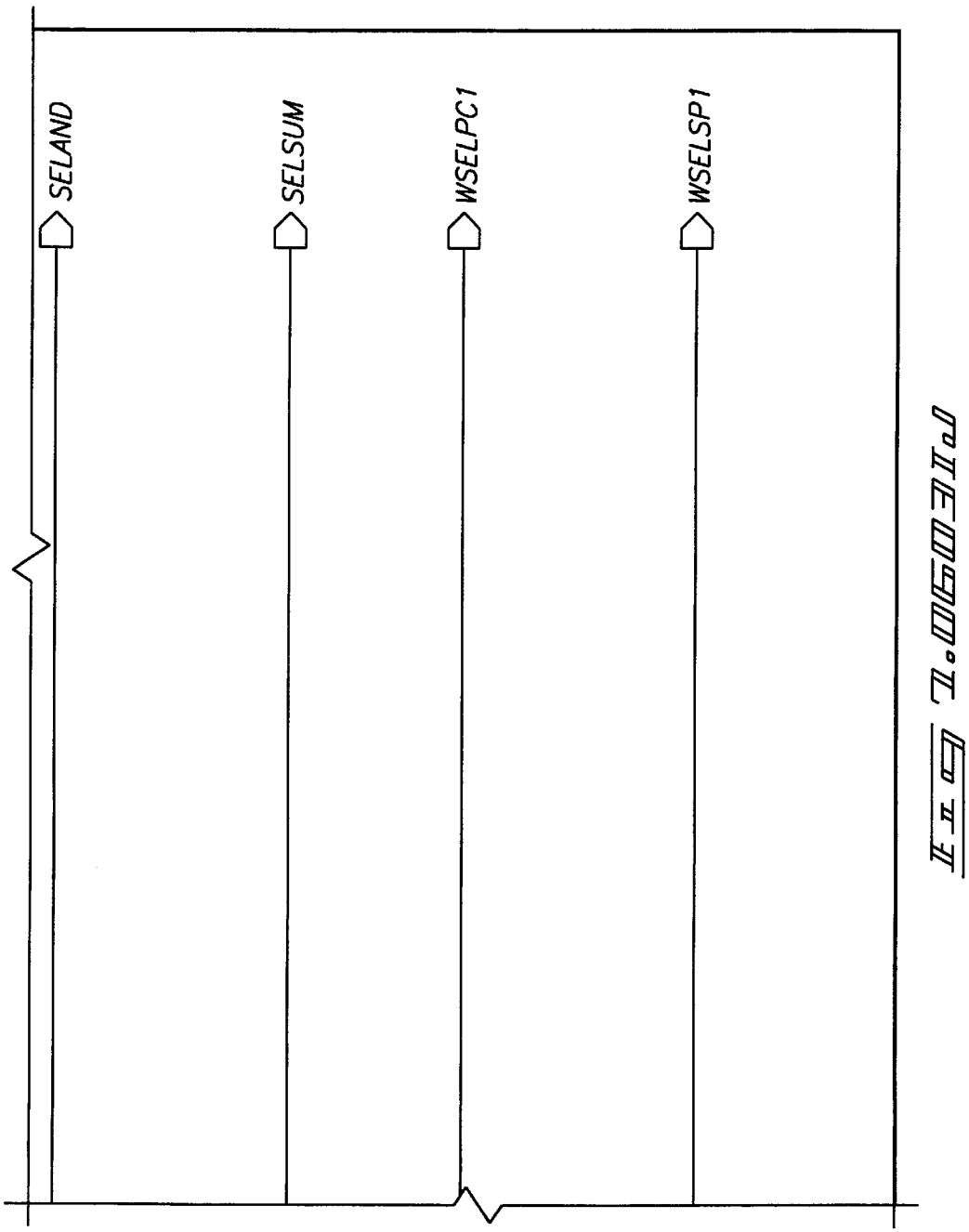
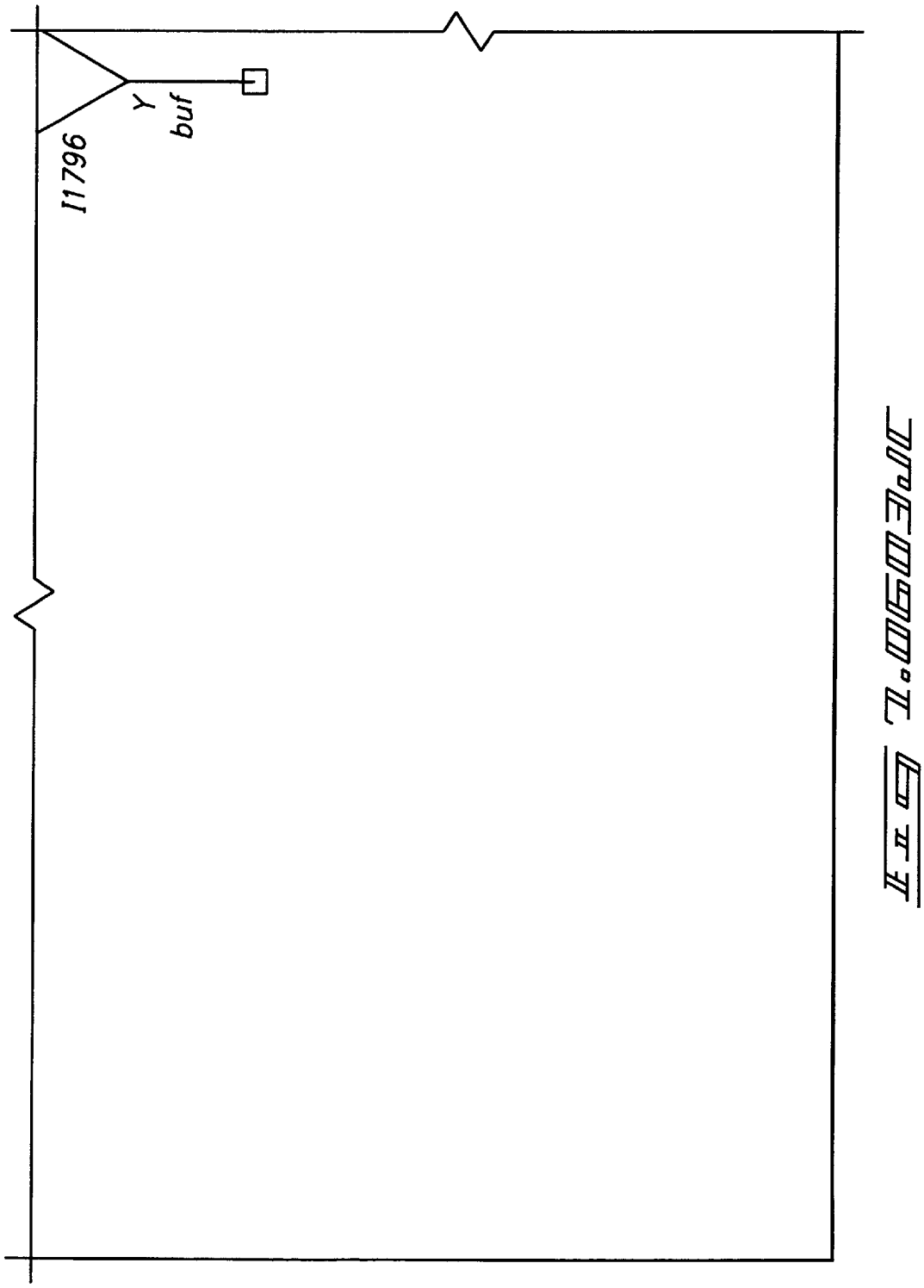

24u/1u
SELAND
SELSUM
16u/1u
I1177
24u/1u
WSELPC1
wselpc1n
16u/1u
12u/1u
wselpc1n
I1167
24u/1u
WSELSP1
wselsp1n
16u/1u
12u/1u
wselsp1n

FIG. 6,130,602


SELAND
SELSUM
WSELPC1
WSELSP1
FIG. 730.1


I1796
Y
buf
FIG. 1796

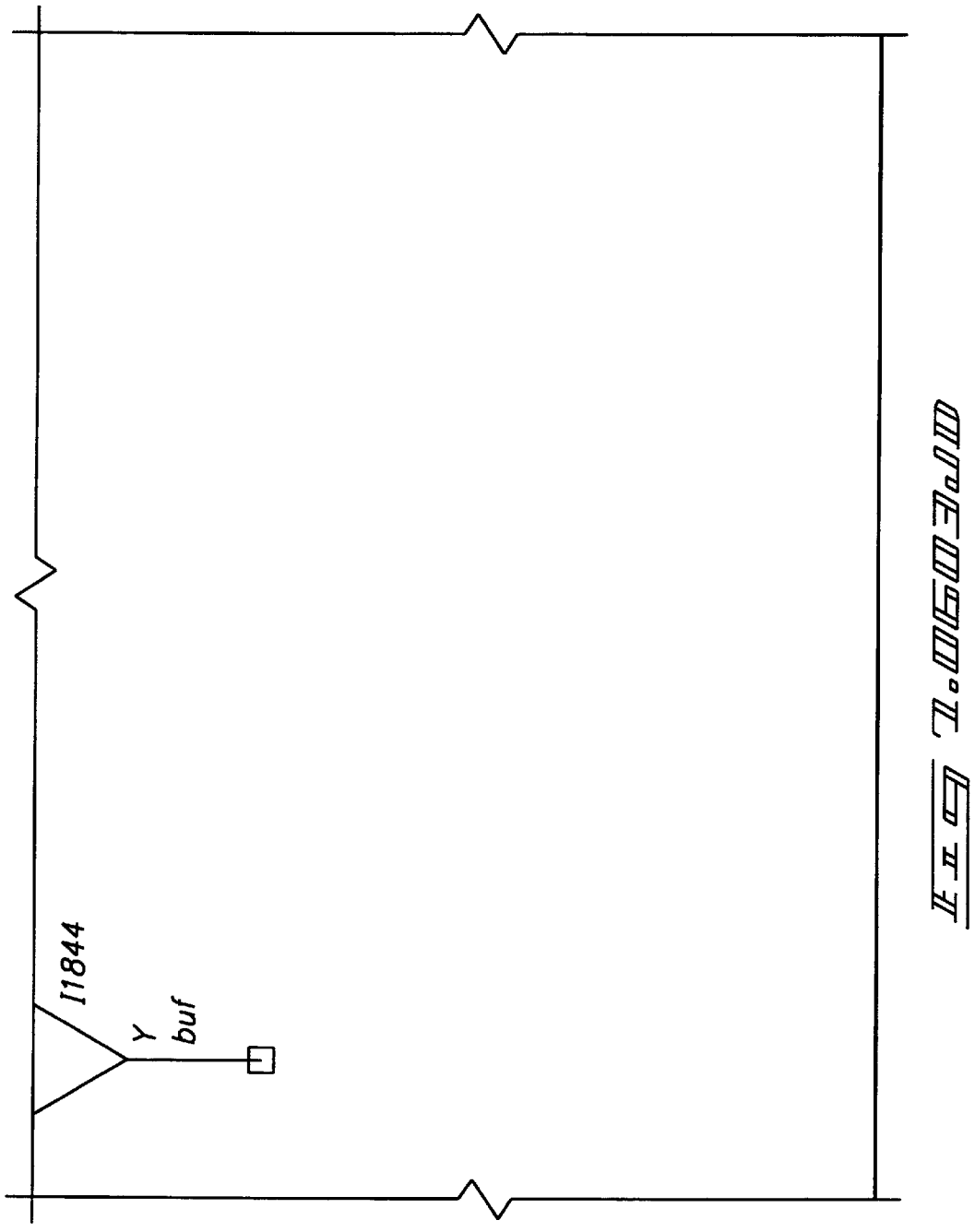
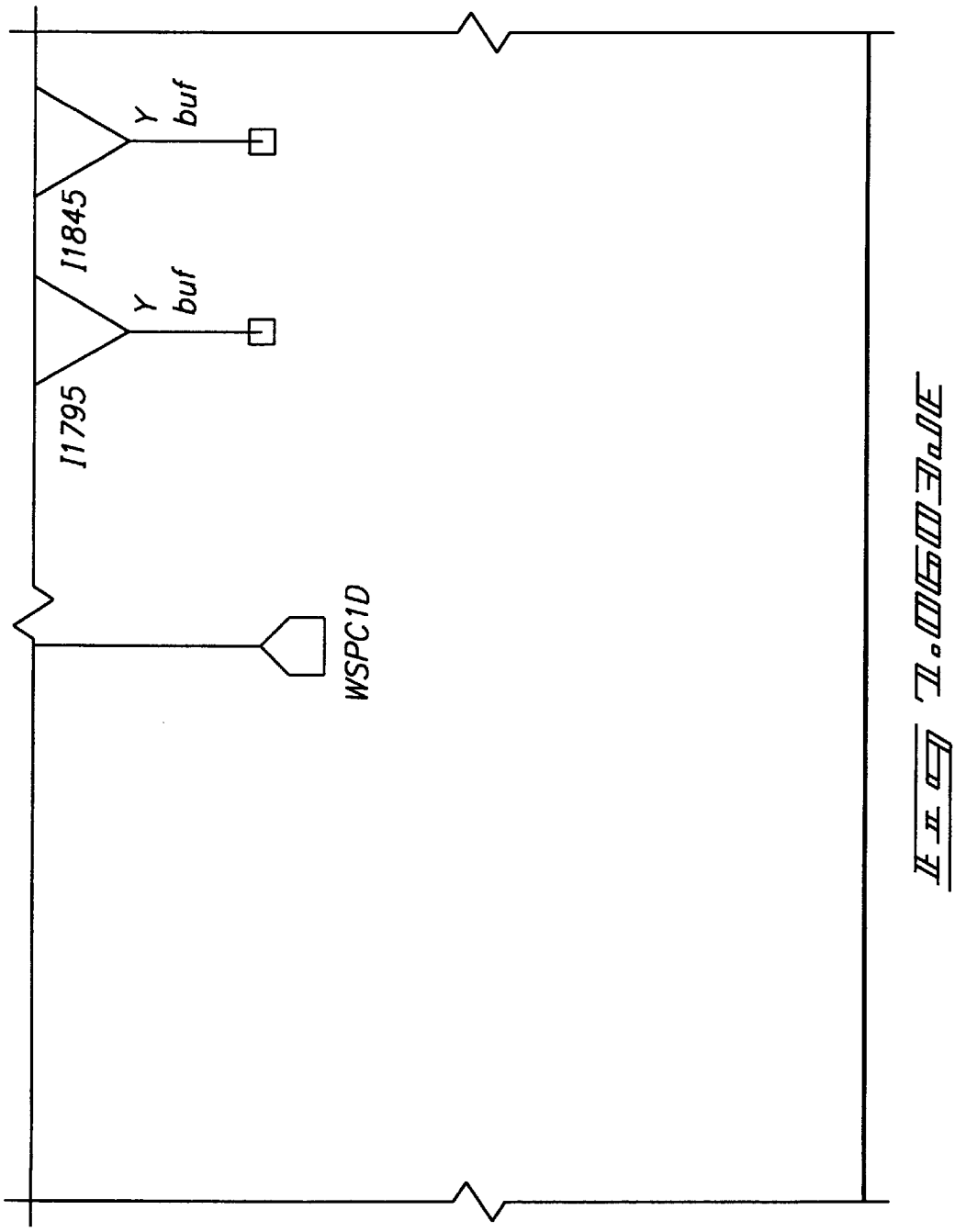
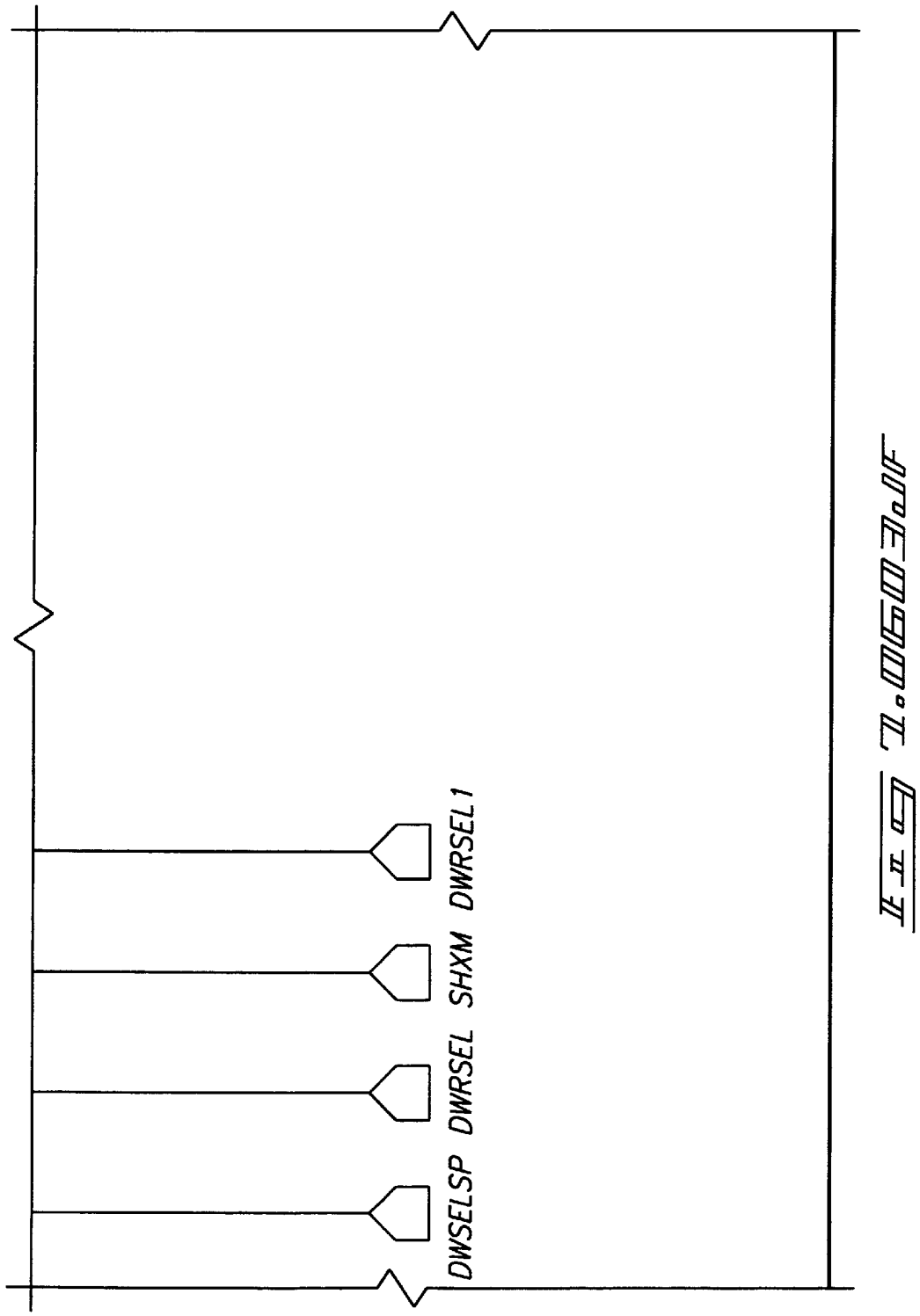
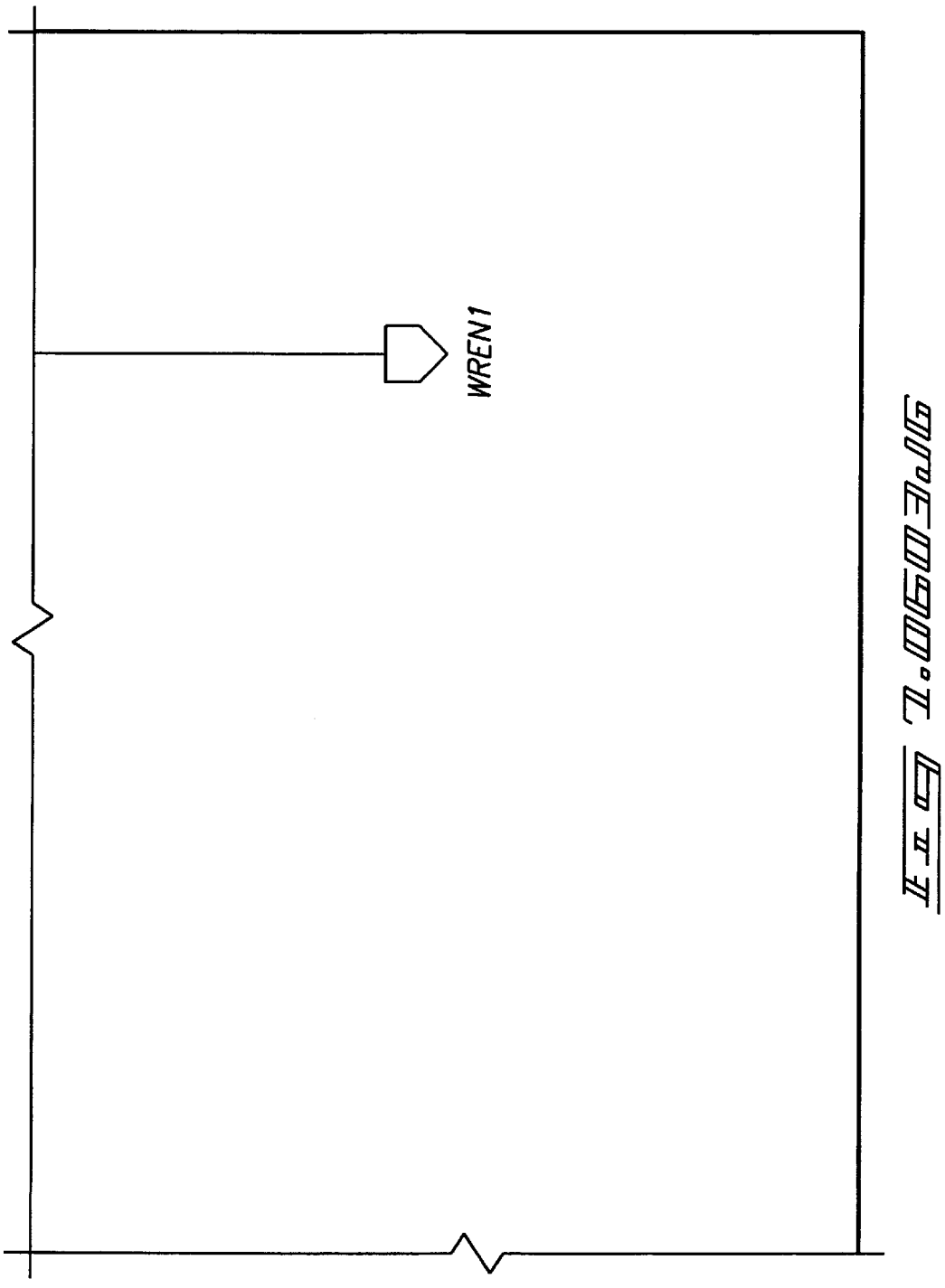


FIG 11,050
I1844
Y
buf


Y
buf
I1845
Y
buf
I1795
WSPC1D
FIG. 733


DWSELSP
DWRSEL
SHXM
DWRSEL1
FIG 6.0900.1L


WREN1
SHEET 0500 OF

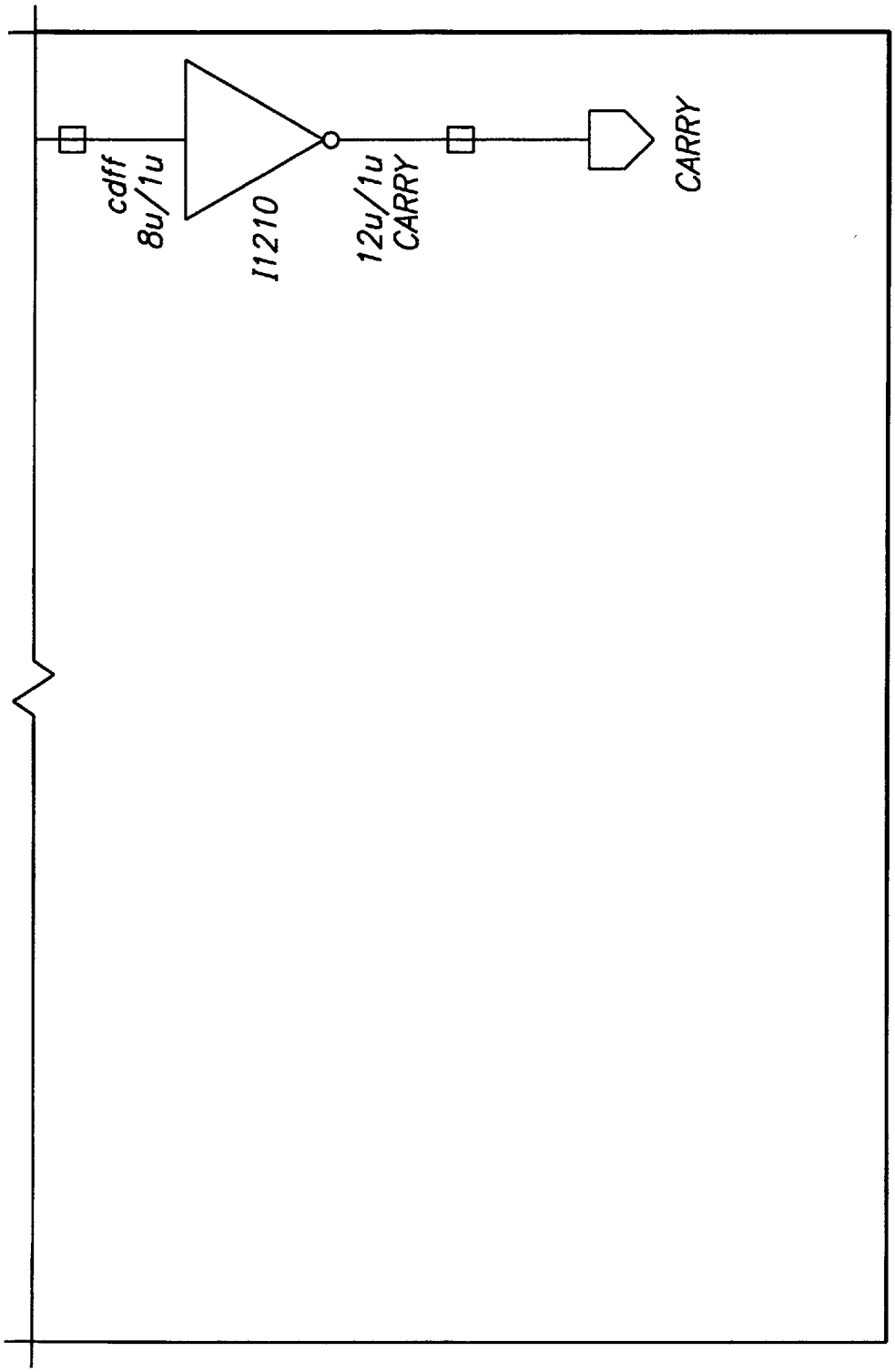


FIG. 1050.736

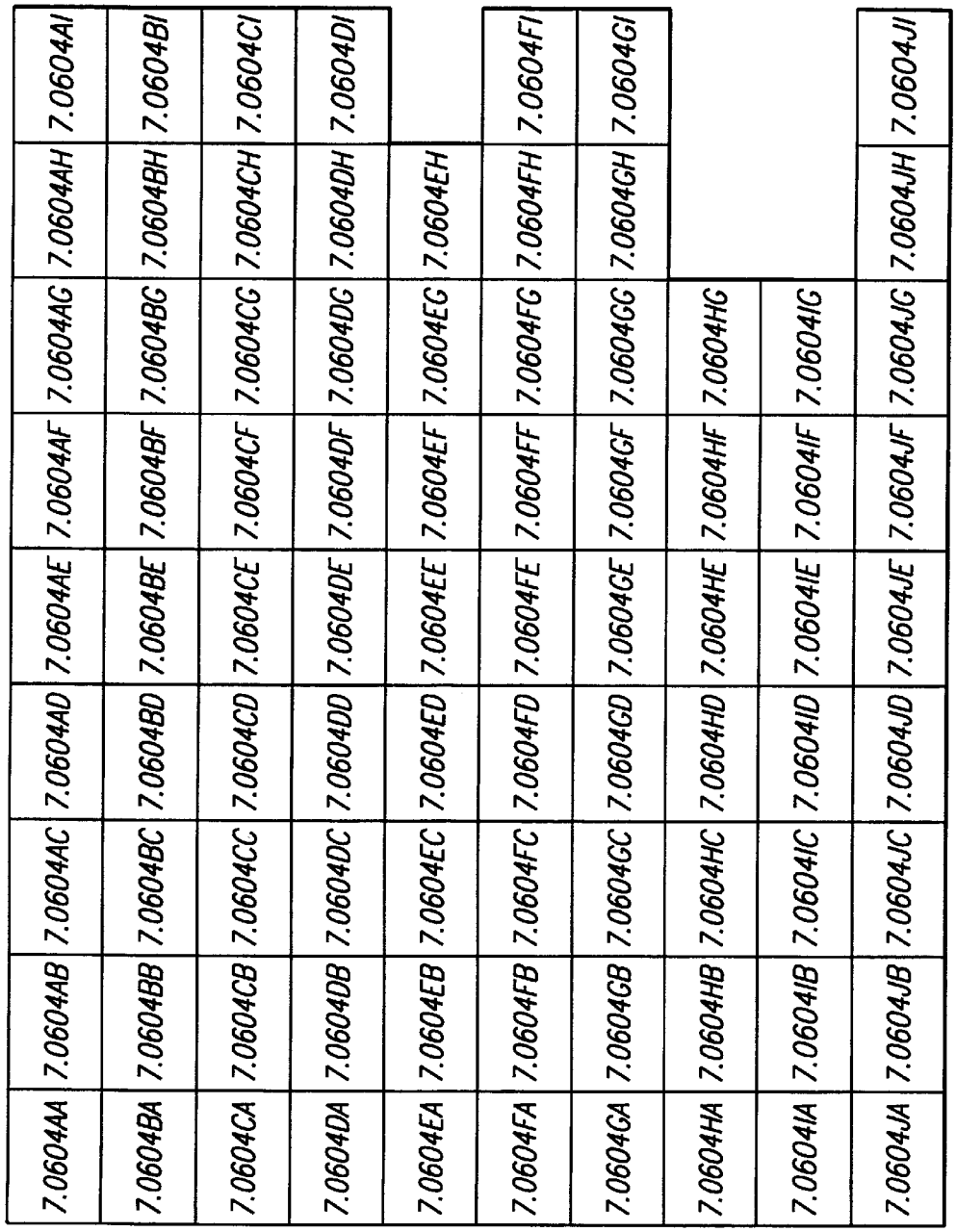

7.0604AA 7.0604AB 7.0604AC 7.0604AD 7.0604AE 7.0604AF 7.0604AG 7.0604AH 7.0604AI
7.0604BA 7.0604BB 7.0604BC 7.0604BD 7.0604BE 7.0604BF 7.0604BG 7.0604BH 7.0604BI
7.0604CA 7.0604CB 7.0604CC 7.0604CD 7.0604CE 7.0604CF 7.0604CG 7.0604CH 7.0604CI
7.0604DA 7.0604DB 7.0604DC 7.0604DD 7.0604DE 7.0604DF 7.0604DG 7.0604DH 7.0604DI
7.0604EA 7.0604EB 7.0604EC 7.0604ED 7.0604EE 7.0604EF 7.0604EG 7.0604EH
7.0604FA 7.0604FB 7.0604FC 7.0604FD 7.0604FE 7.0604FF 7.0604FG 7.0604FH 7.0604FI
7.0604GA 7.0604GB 7.0604GC 7.0604GD 7.0604GE 7.0604GF 7.0604GG 7.0604GH 7.0604GI
7.0604HA 7.0604HB 7.0604HC 7.0604HD 7.0604HE 7.0604HF 7.0604HG
7.0604IA 7.0604IB 7.0604IC 7.0604ID 7.0604IE 7.0604IF 7.0604IG
7.0604JA 7.0604JB 7.0604JC 7.0604JD 7.0604JE 7.0604JF 7.0604JG 7.0604JH 7.0604JI

FIG 7.0604.IL

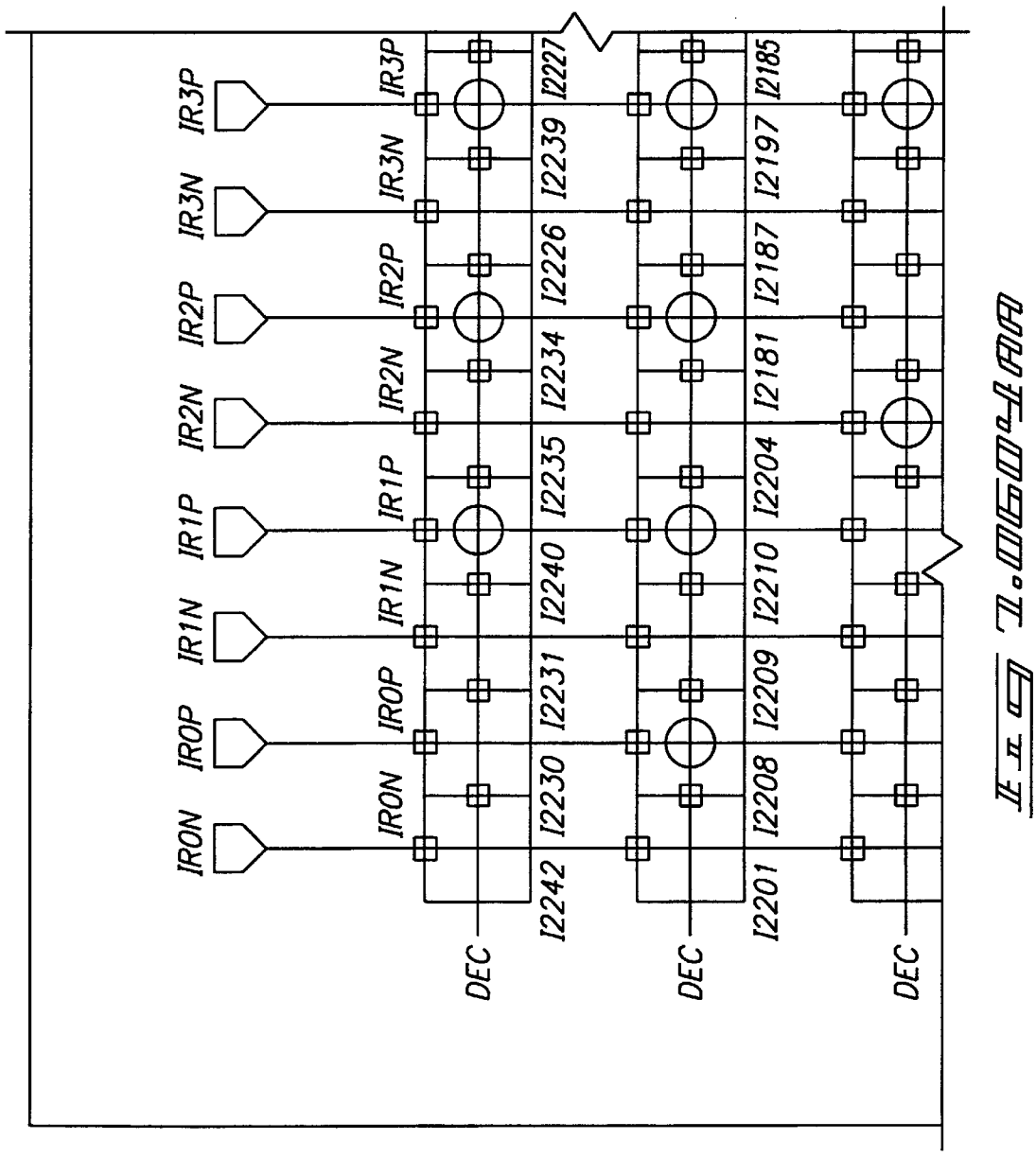

IR3P
IR3N
IR2P
IR2N
IR1P
IR1N
IR0P
IR0N
I2227
I2239
I2226
I2234
I2235
I2240
I2231
I2230
I2242
I2185
I2197
I2187
I2181
I2204
I2210
I2209
I2208
I2201
DEC
DEC
DEC

FIG 738

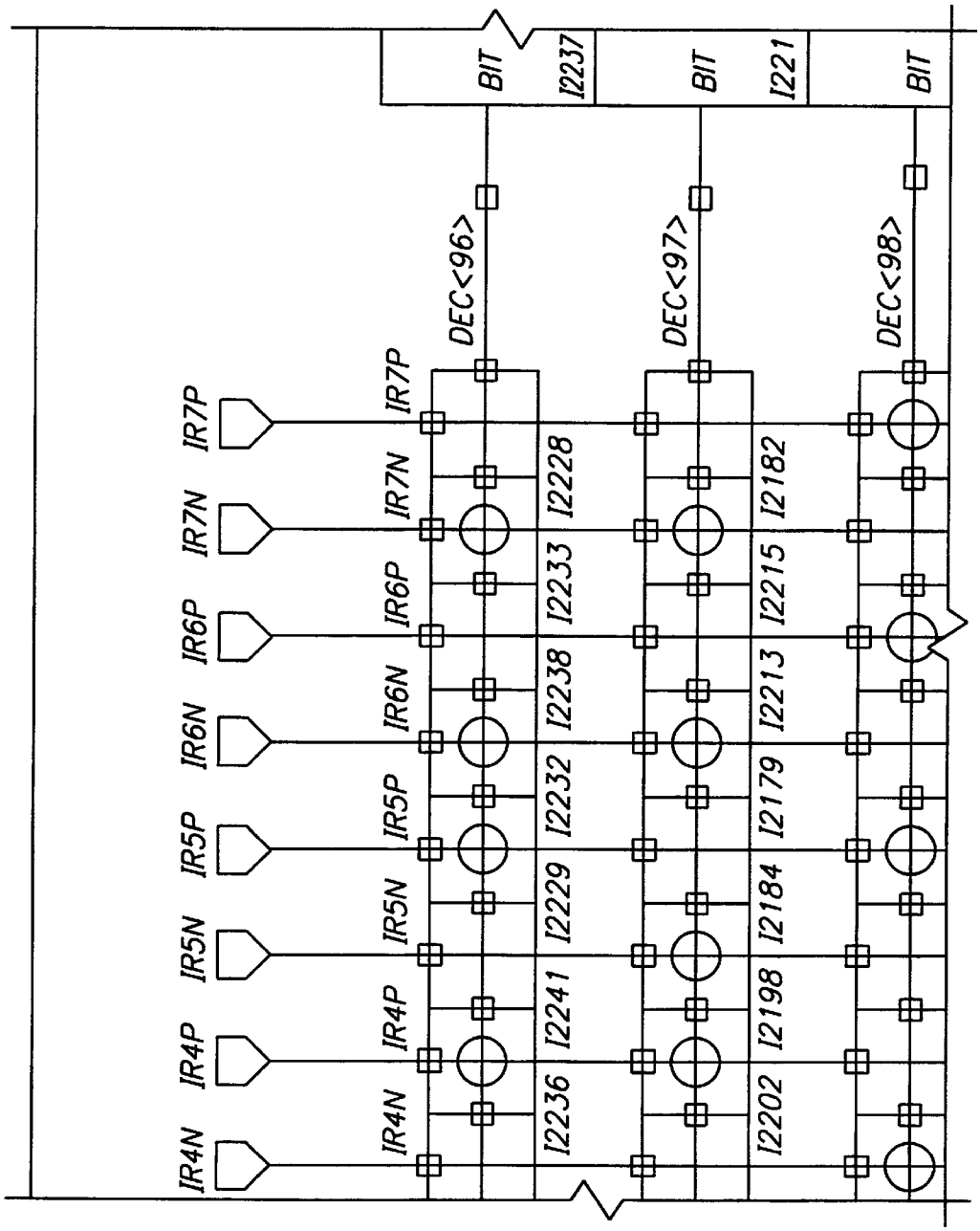

BIT
I2237
I221
DEC<96>
DEC<97>
DEC<98>
IR7P
IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
IR4N
I2228
I2182
I2233
I2215
I2238
I2213
I2232
I2179
I2229
I2184
I2241
I2198
I2236
I2202

Fig. 1.0604AB

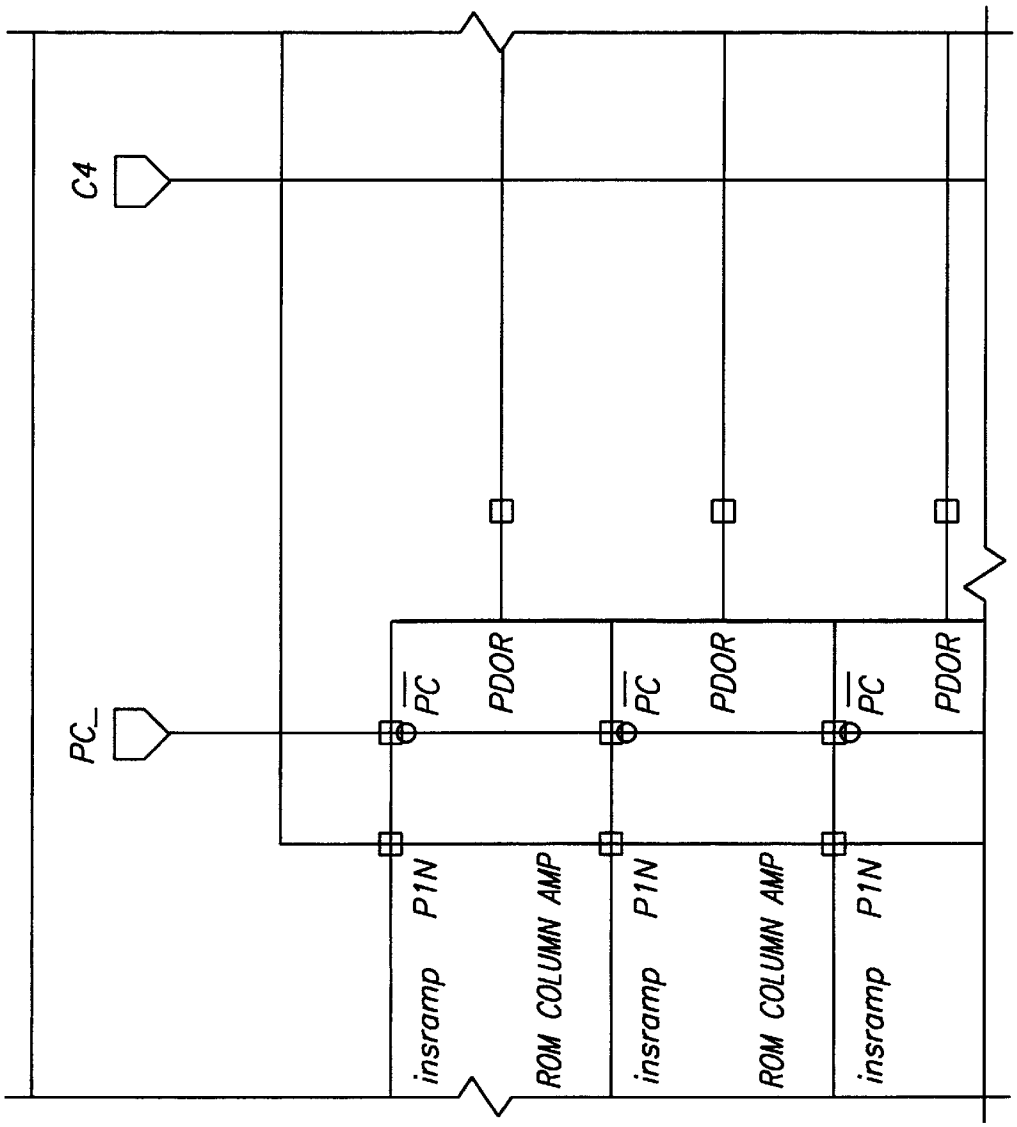


FIG 740

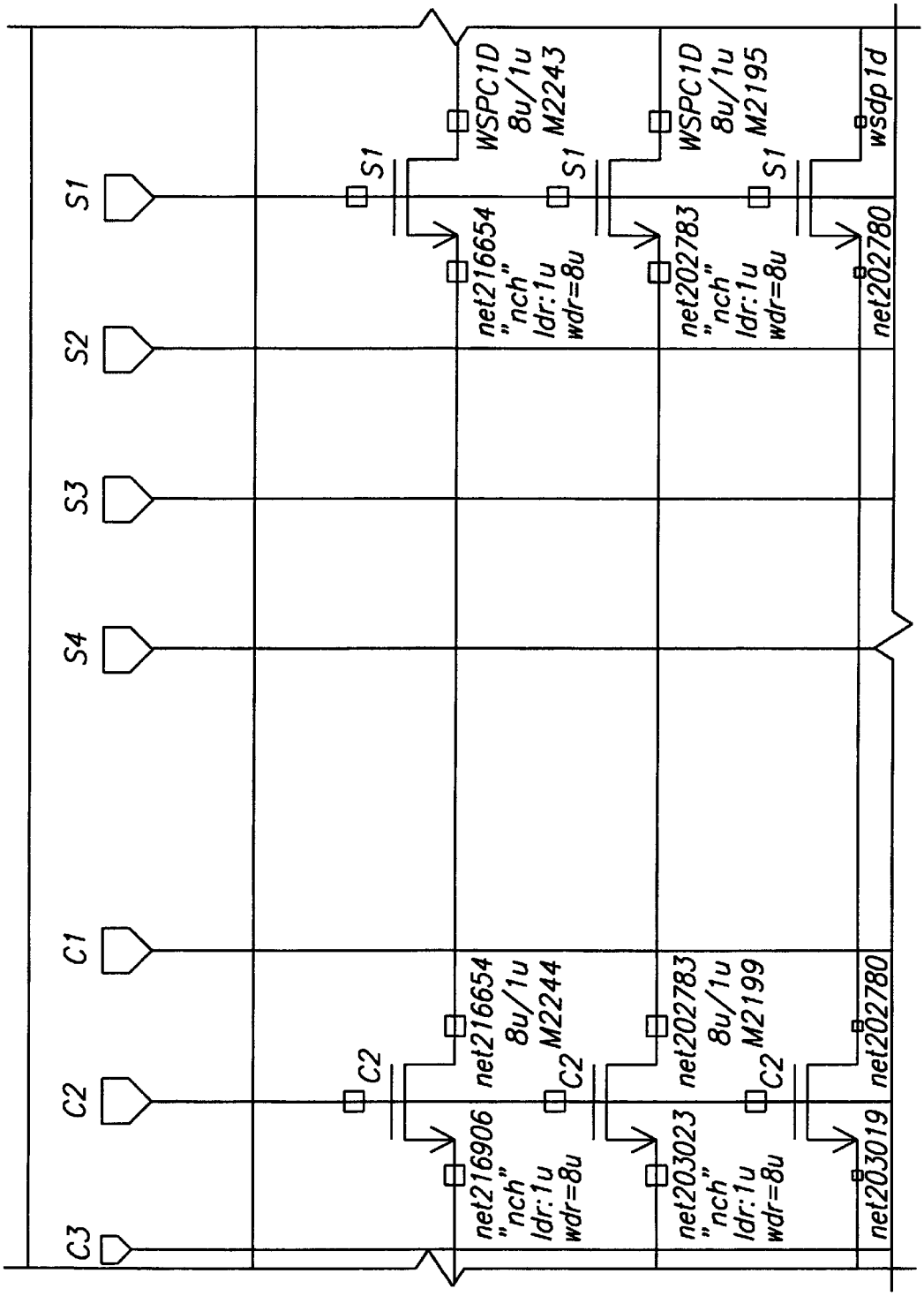

S1
S2
S3
S4
C1
C2
C3
WSPC1D 8u/1u M2243
WSPC1D 8u/1u M2195
wsdp1d
net216654 "nch" ldr:1u wdr=8u
net202783 "nch" ldr:1u wdr=8u
net202780
net216654 8u/1u M2244
net202783 8u/1u M2199
net216906 "nch" ldr:1u wdr=8u
net203023 "nch" ldr:1u wdr=8u
net203019

Fig 741

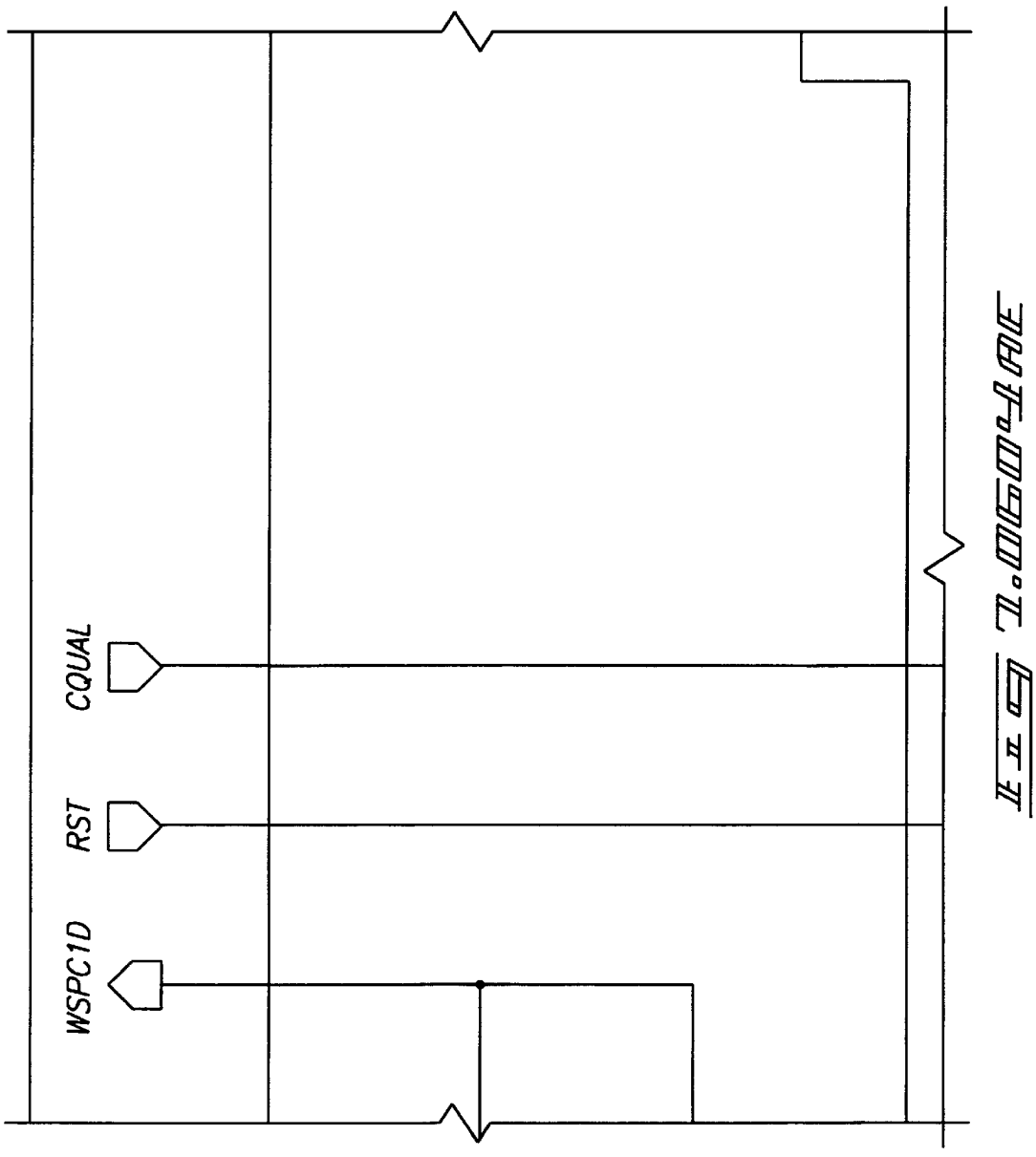


FIG. 1,060,746AE
COUAL
RST
WSPC1D

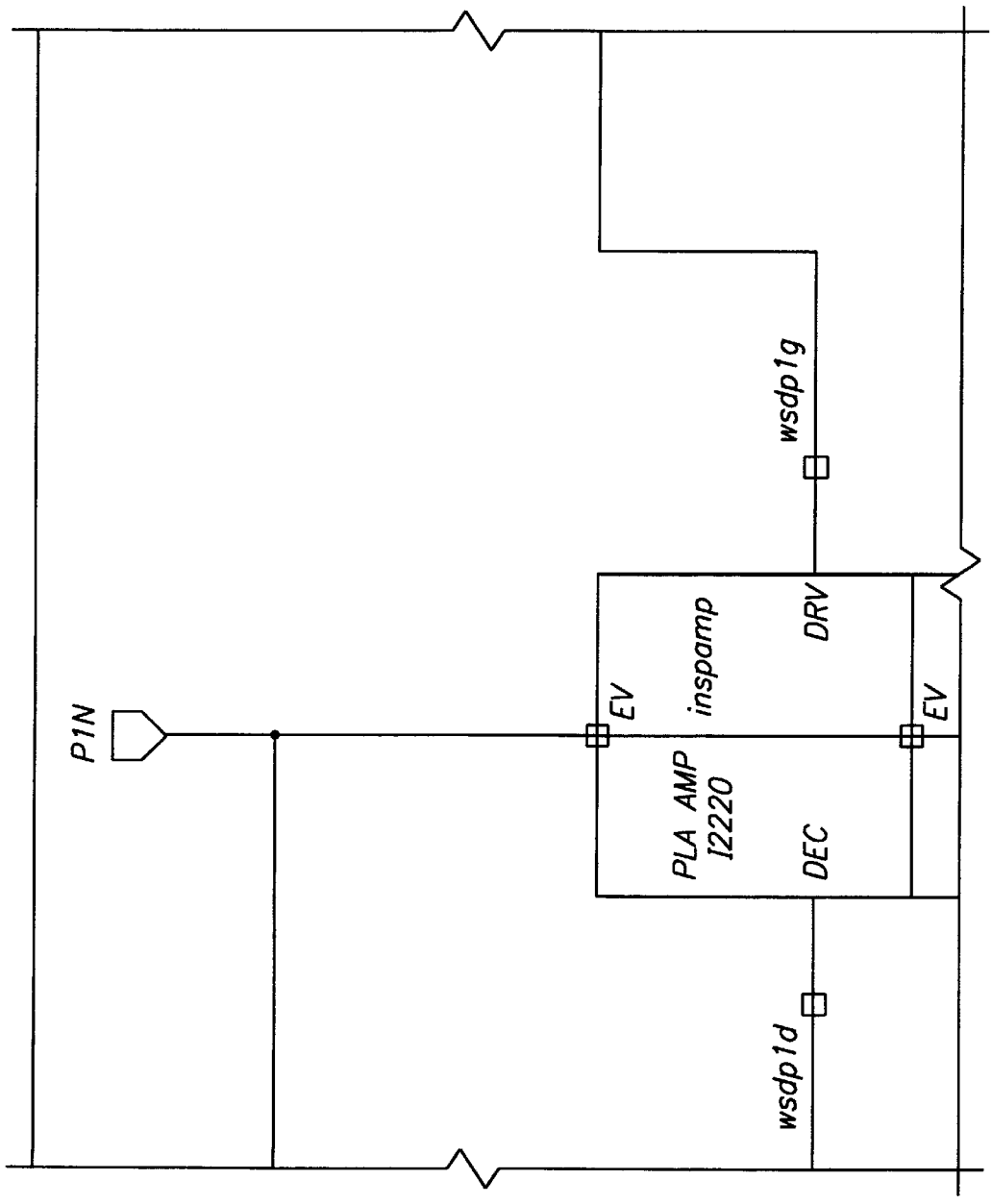


FIG 11.0604AF

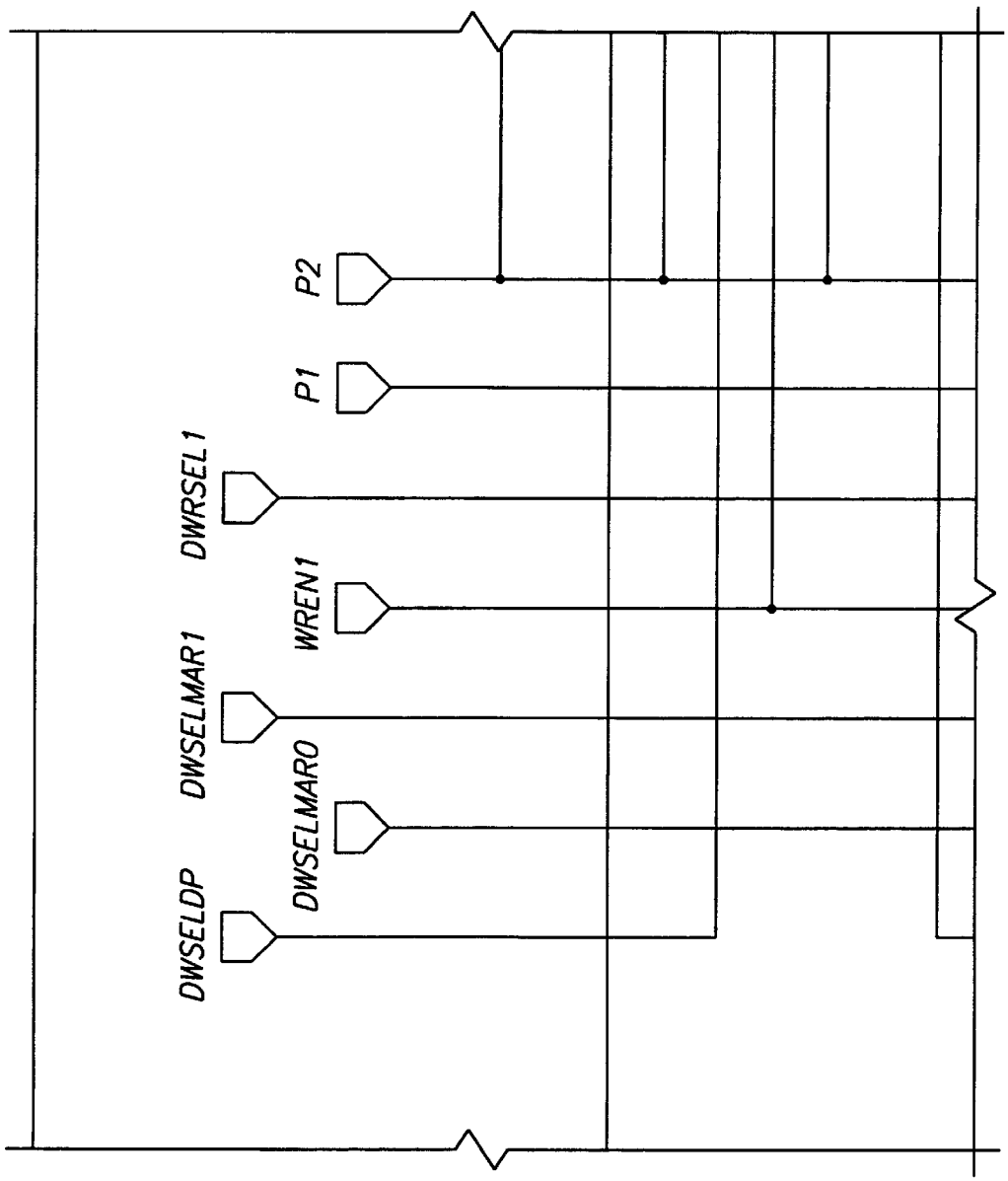


FIG 1,060,146

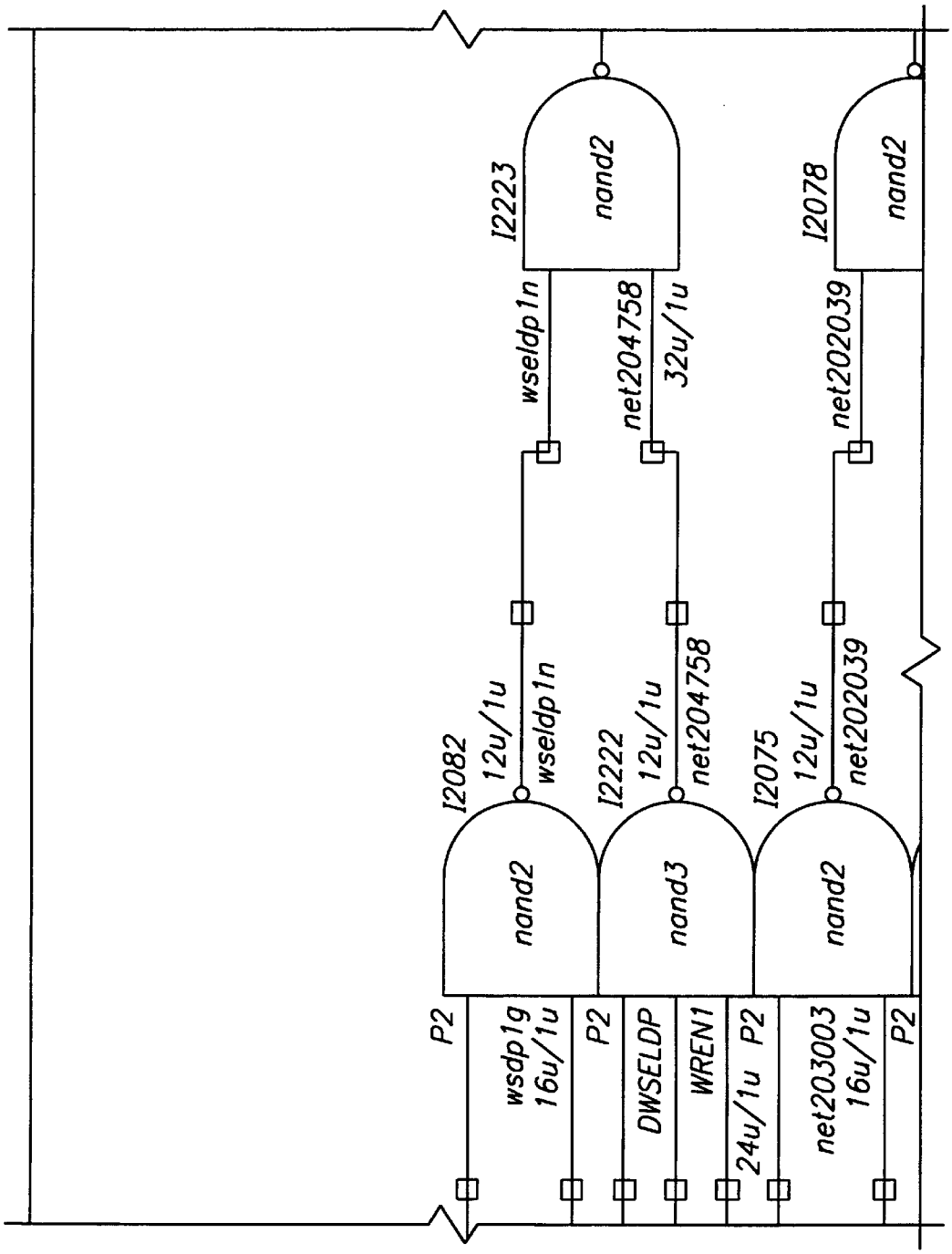

I2223
nand2
I2078
nand2
wseldp1n
net204758
32u/1u
net202039
I2082
12u/1u
wseldp1n
I2222
12u/1u
net204758
I2075
12u/1u
net202039
nand2
nand3
nand2
P2
wsdp1g
16u/1u
P2
DWSELDP
WREN1
24u/1u
P2
net203003
16u/1u
P2

FIG 1,050,744

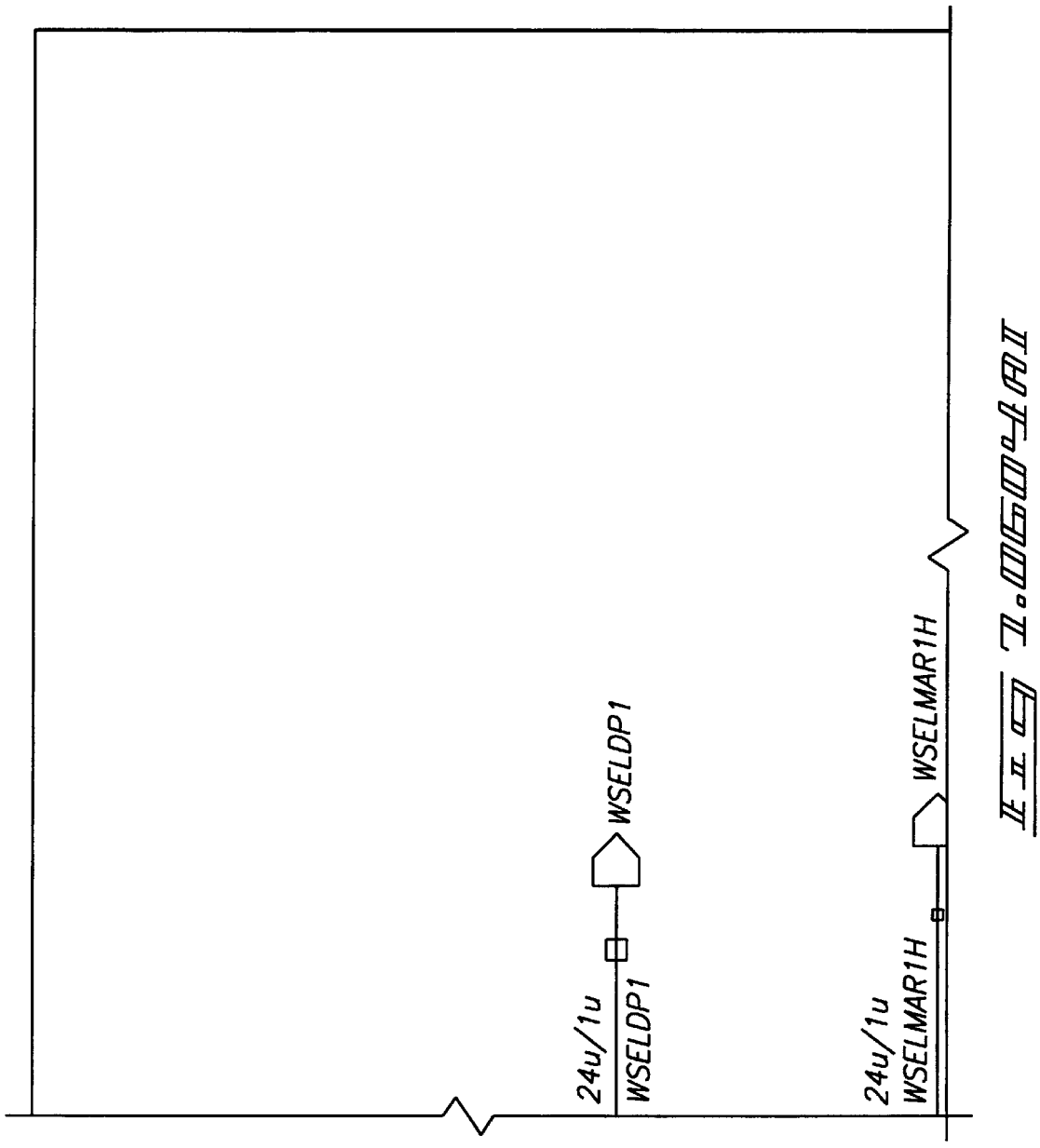
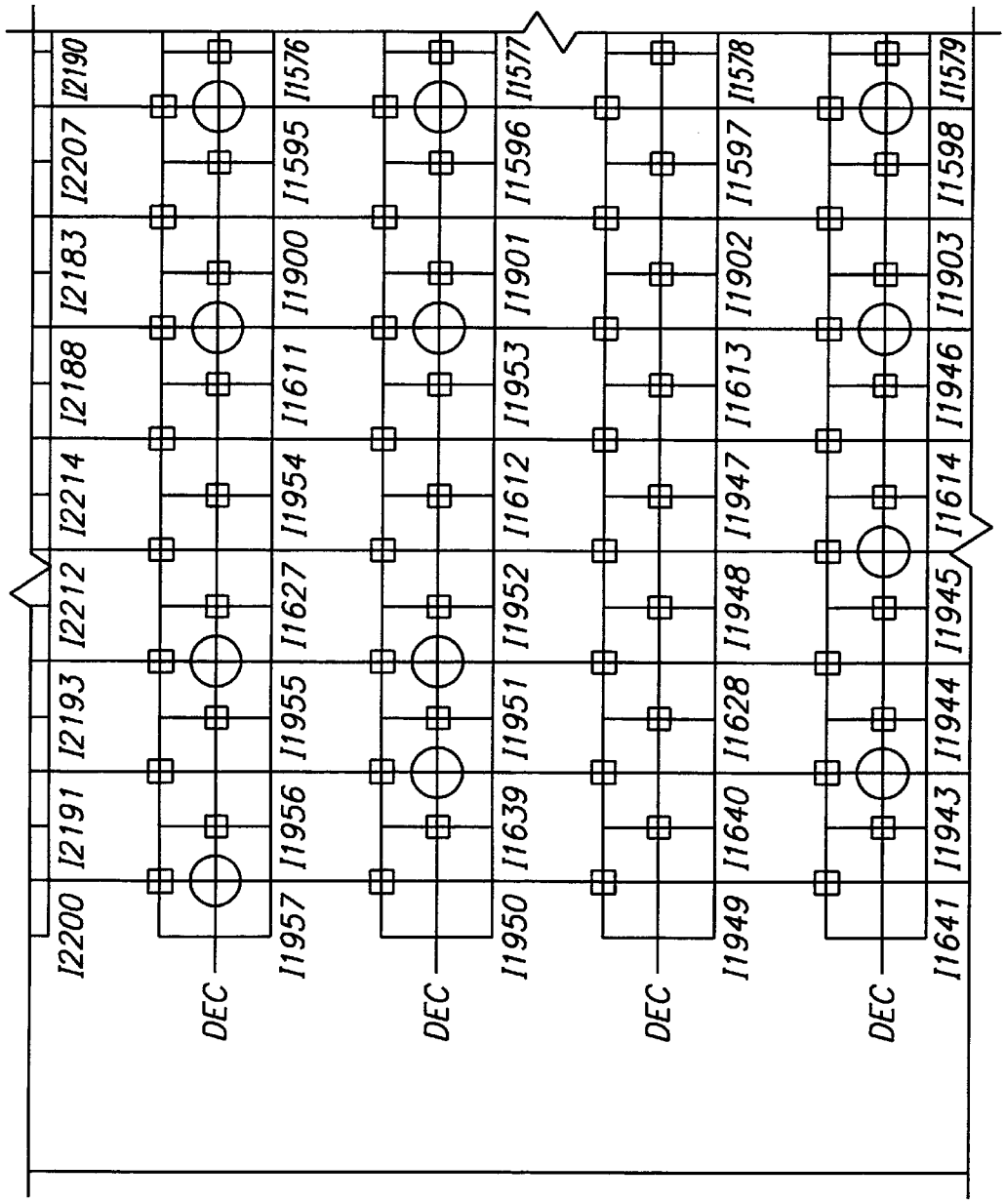
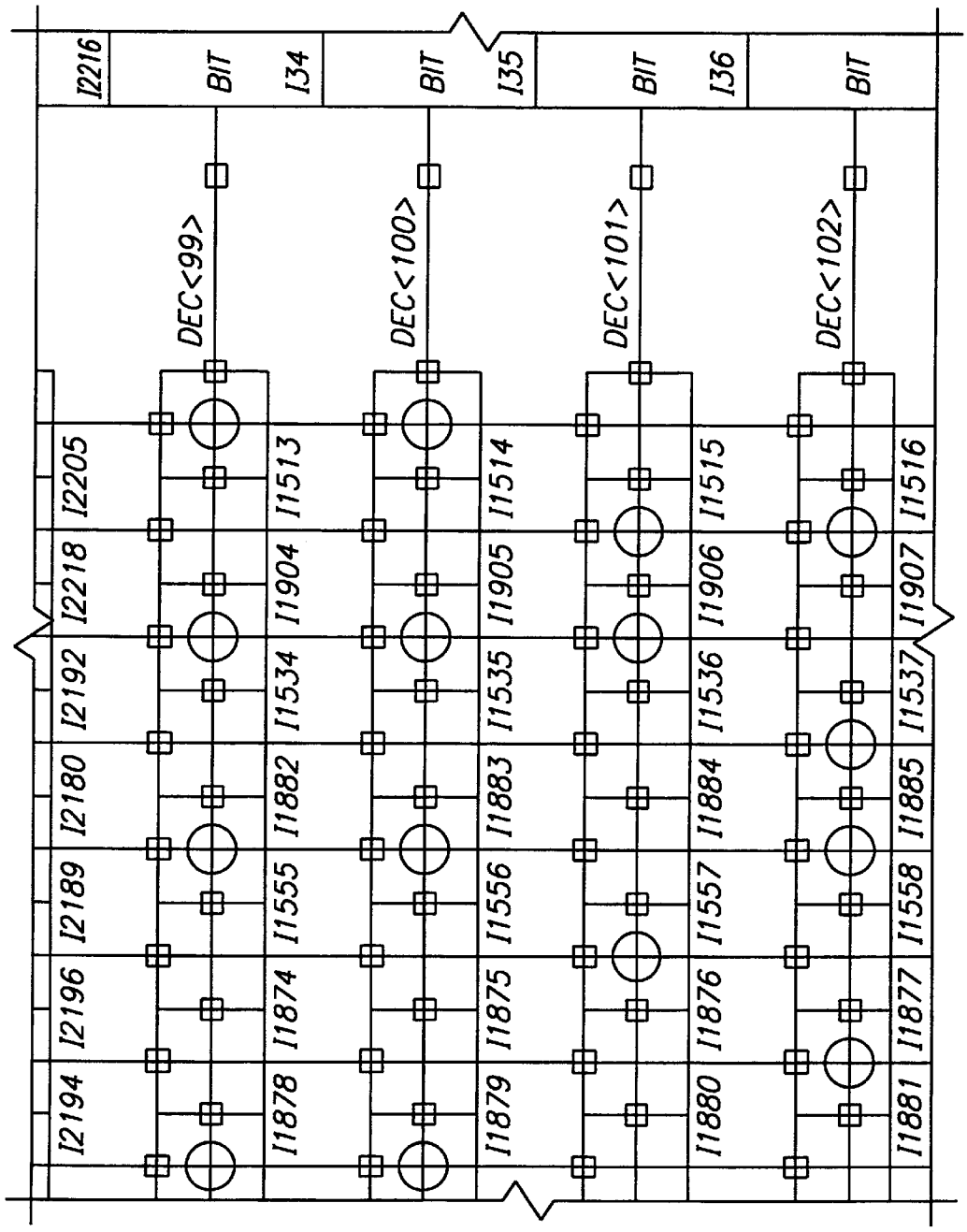


FIG. 1,090


I2200
I2191
I2193
I2212
I2214
I2188
I2183
I2207
I2190
I1957
I1956
I1955
I1627
I1954
I1611
I1900
I1595
I1576
I1950
I1639
I1951
I1952
I1612
I1953
I1901
I1596
I1577
I1949
I1640
I1628
I1948
I1947
I1613
I1902
I1597
I1578
I1641
I1943
I1944
I1945
I1614
I1946
I1903
I1598
I1579
DEC
DEC
DEC
DEC

ВЫХОДЫ ДШ


I2216
BIT
I34
BIT
I35
BIT
I36
BIT
DEC<99>
DEC<100>
DEC<101>
DEC<102>
I2205
I2218
I2192
I2180
I2189
I2196
I2194
I1513
I1904
I1534
I1882
I1555
I1874
I1878
I1514
I1905
I1535
I1883
I1556
I1875
I1879
I1515
I1906
I1536
I1884
I1557
I1876
I1880
I1516
I1907
I1537
I1885
I1558
I1877
I1881

ФИГ. 1,605,044

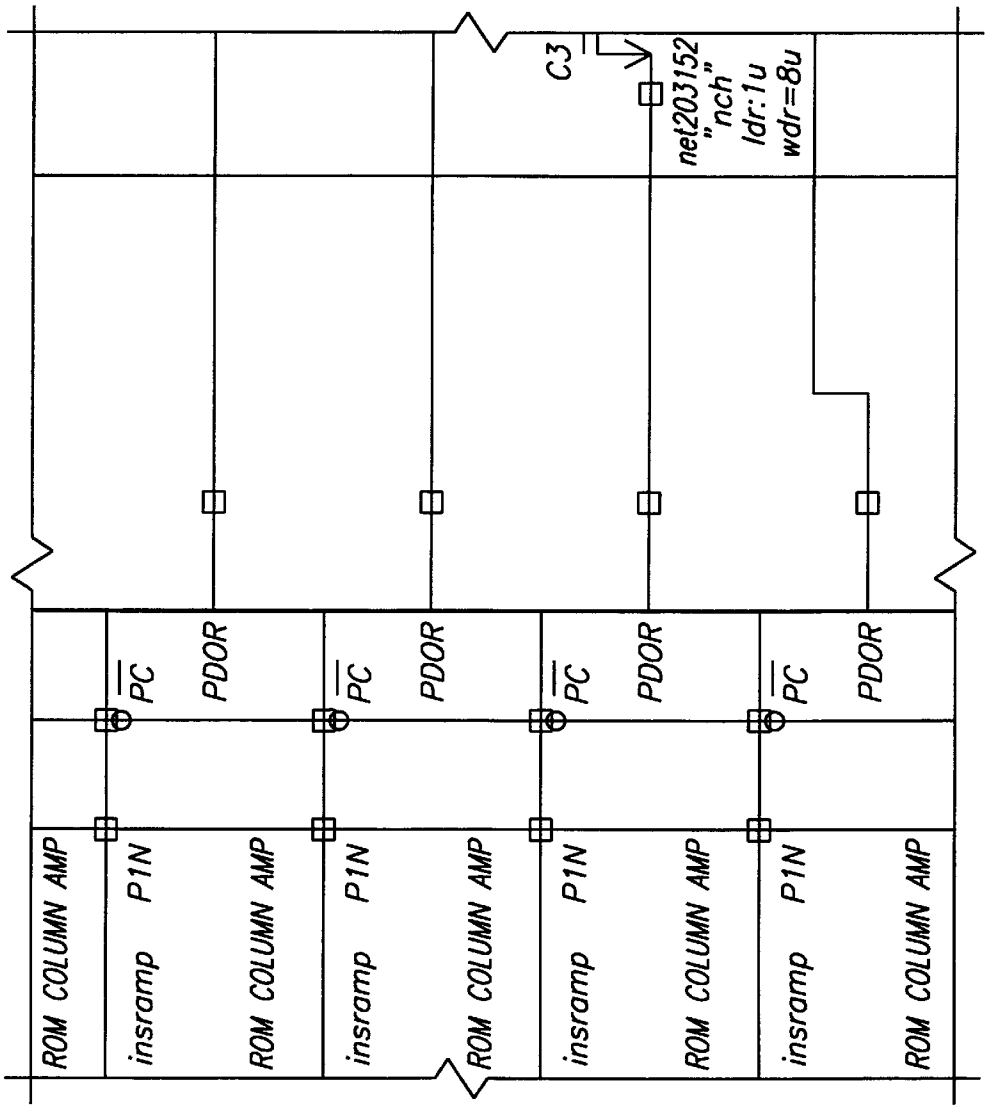

C3
net203152
"nch"
ldr:1u
wdr=8u
PC
PDOR
ROM COLUMN AMP
insramp
P1N

FIG. 7409.1

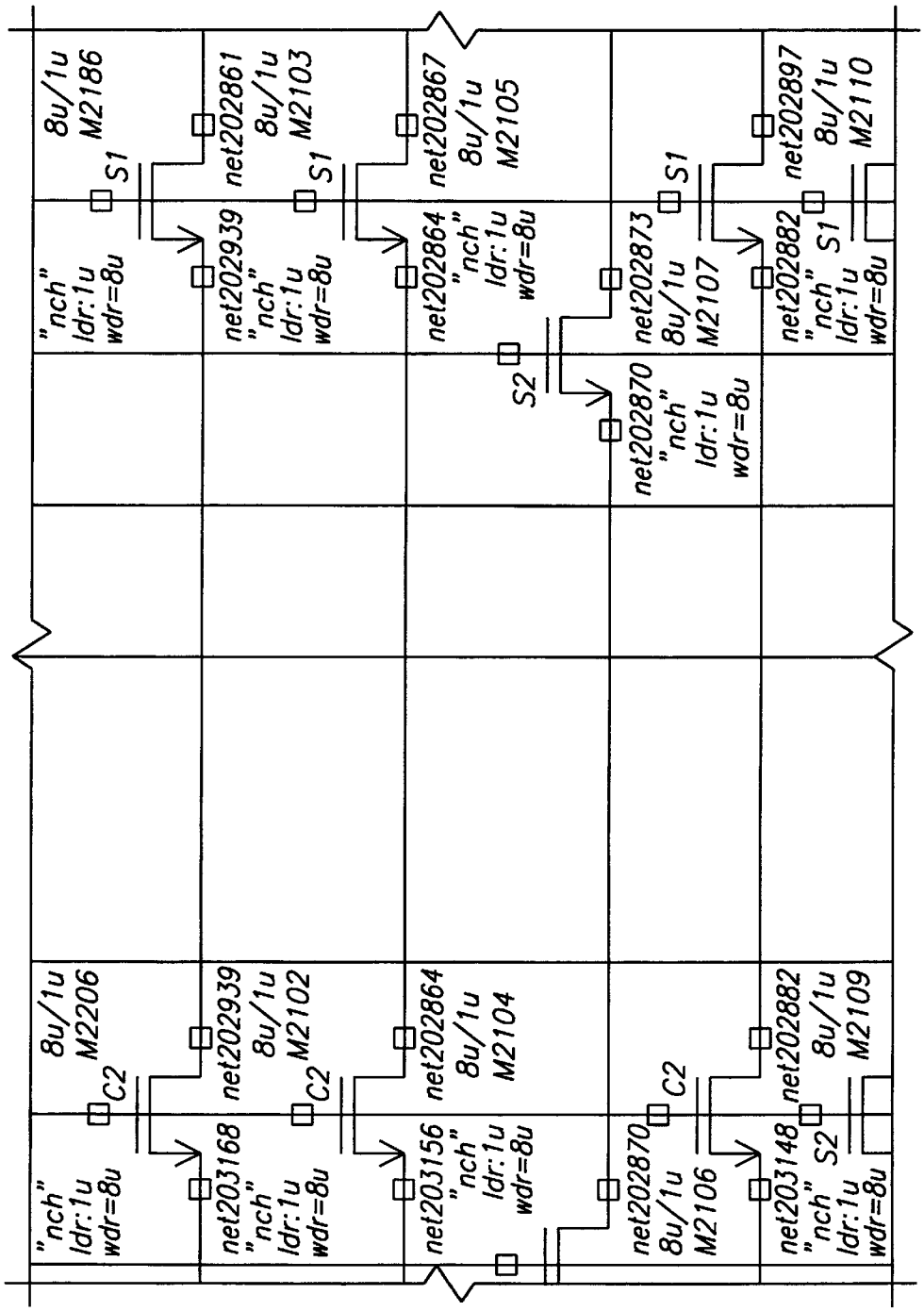

"nch" ldr:1u wdr=8u
8u/1u M2206
C2
net203168
net202939
8u/1u M2102
net203156
net202864
8u/1u M2104
net202870
8u/1u M2106
net203148
net202882
8u/1u M2109
net202939
8u/1u M2186
S1
net202861
8u/1u M2103
net202867
8u/1u M2105
S2
net202870
net202873
8u/1u M2107
net202882
net202897
8u/1u M2110

FIG. 1,050,448

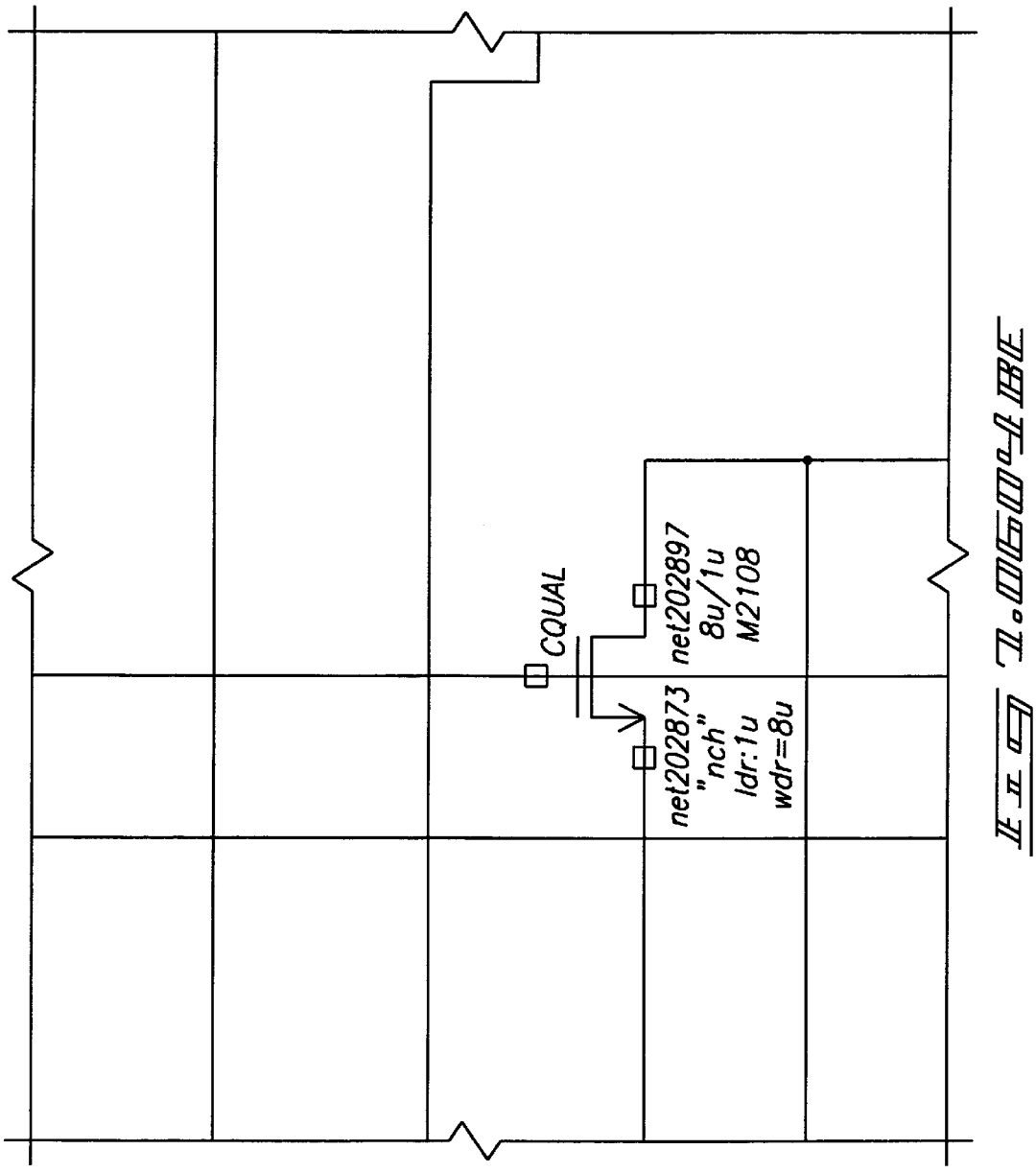


FIG. 1,003,751
CQUAL
net202897
8u/1u
M2108
net202873
"nch"
ldr:1u
wdr=8u

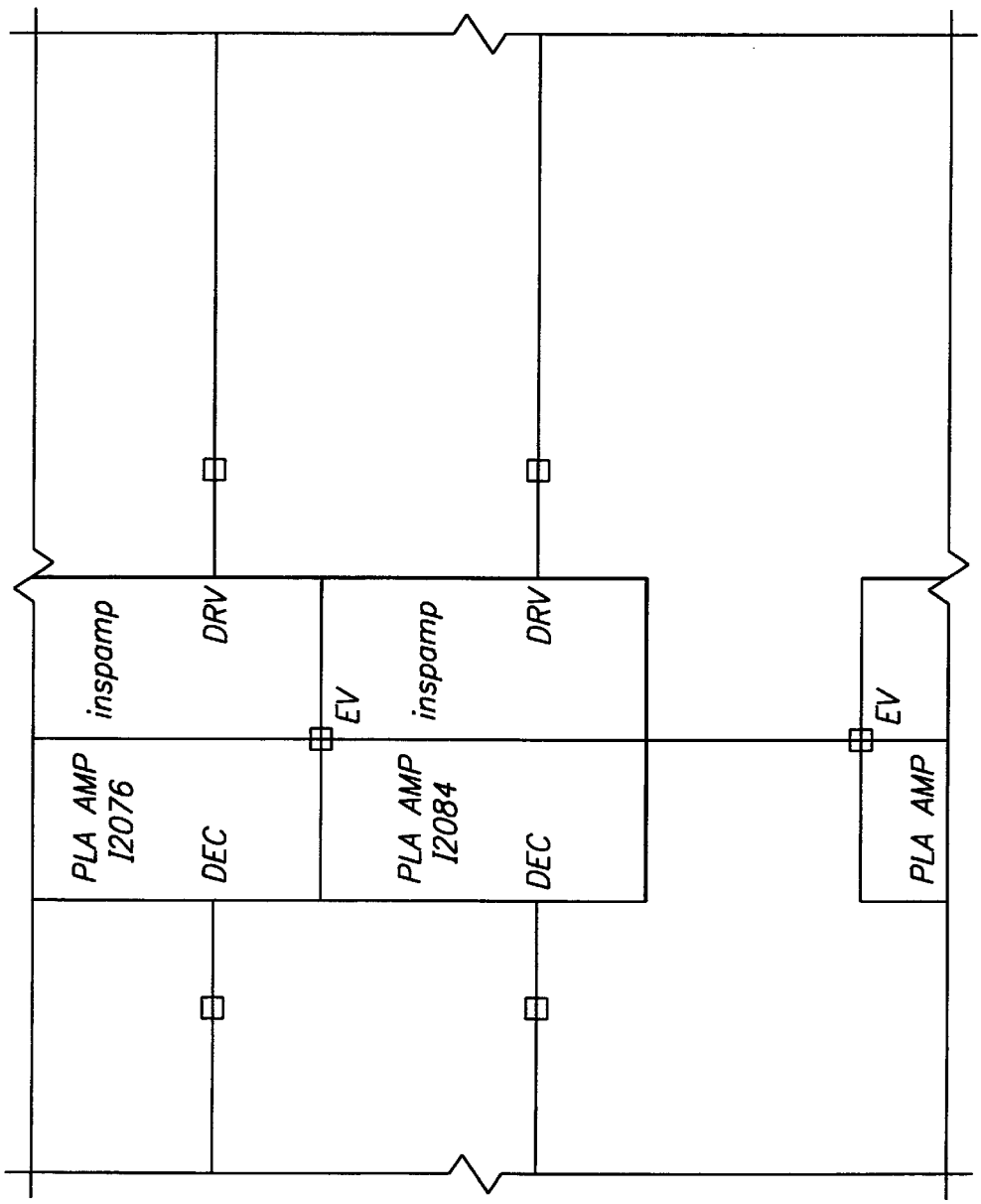
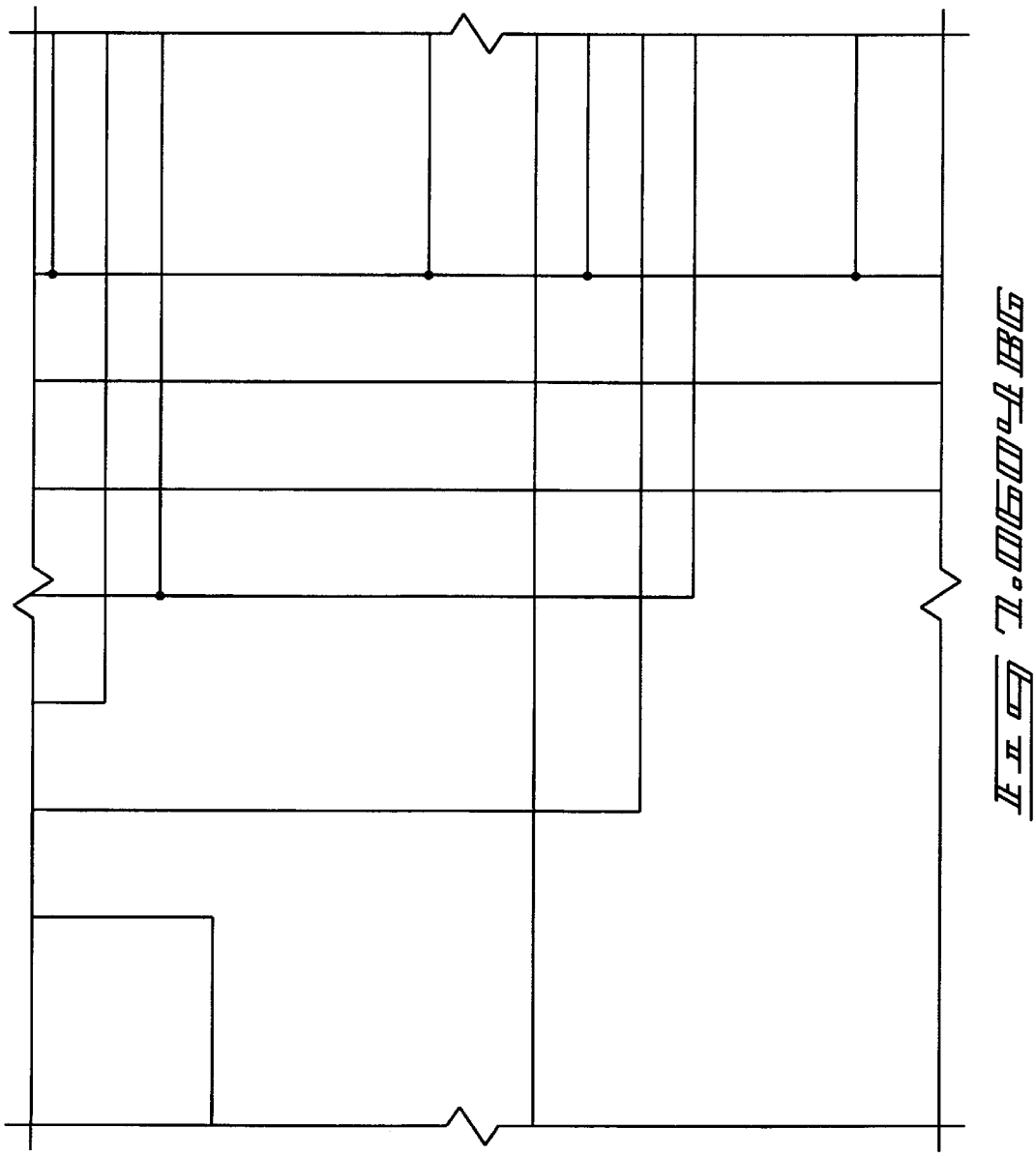

inspamp
DRV
EV
inspamp
DRV
EV
PLA AMP I2076
DEC
PLA AMP I2084
DEC
PLA AMP

FIG 750.1L



SEQ ID NO: 5,047,500

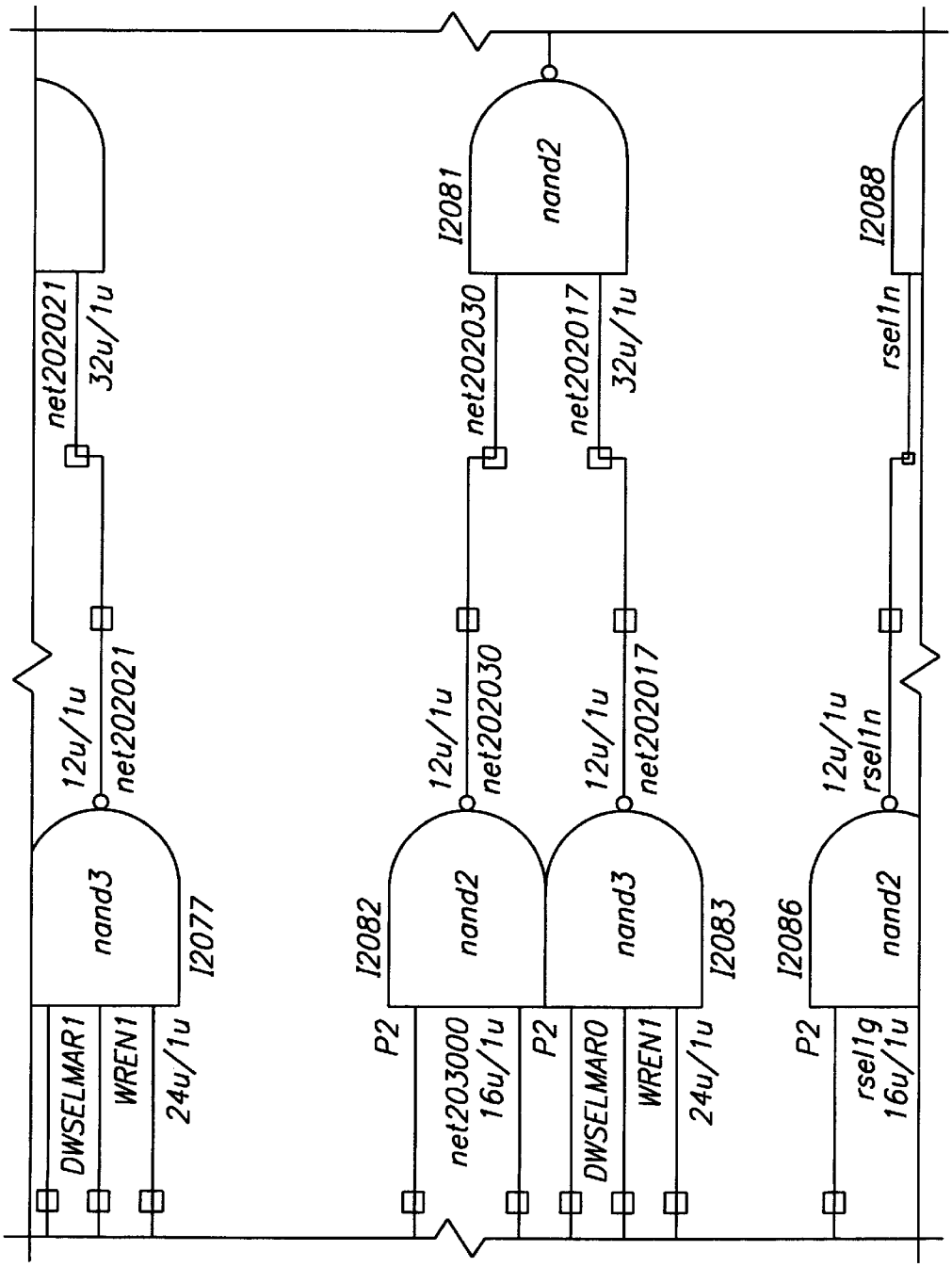
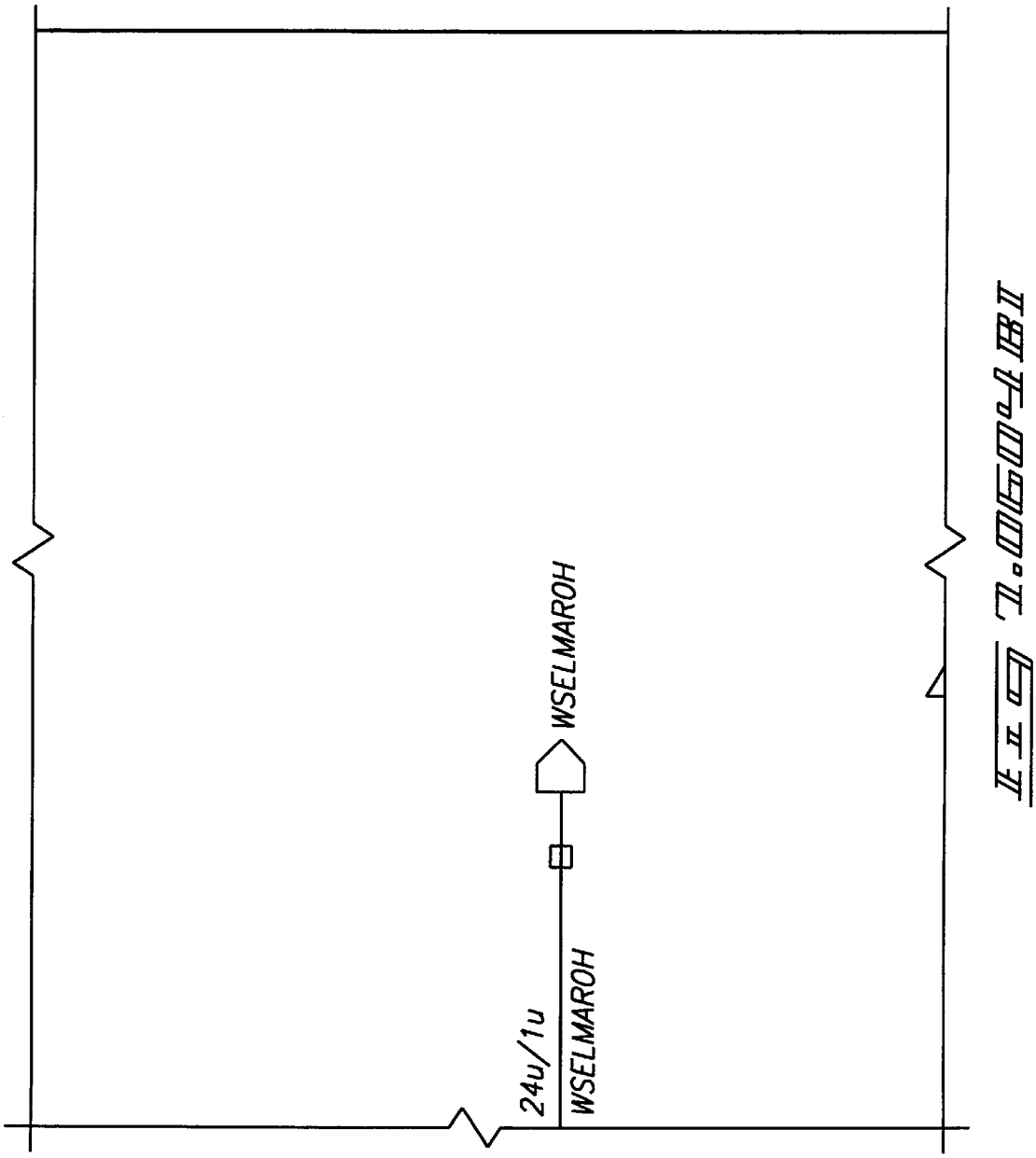

I2077
nand3
DWSELMAR1
WREN1
24u/1u
12u/1u
net202021
net202021
32u/1u
I2081
nand2
net202030
net202017
32u/1u
I2082
nand2
P2
net203000
16u/1u
12u/1u
net202030
I2083
nand3
P2
DWSELMAR0
WREN1
24u/1u
12u/1u
net202017
I2086
nand2
P2
rsel1g
16u/1u
12u/1u
rsel1n
I2088
rsel1n

FIG. 605.754


WSELMAROH
24u/1u
WSELMAROH

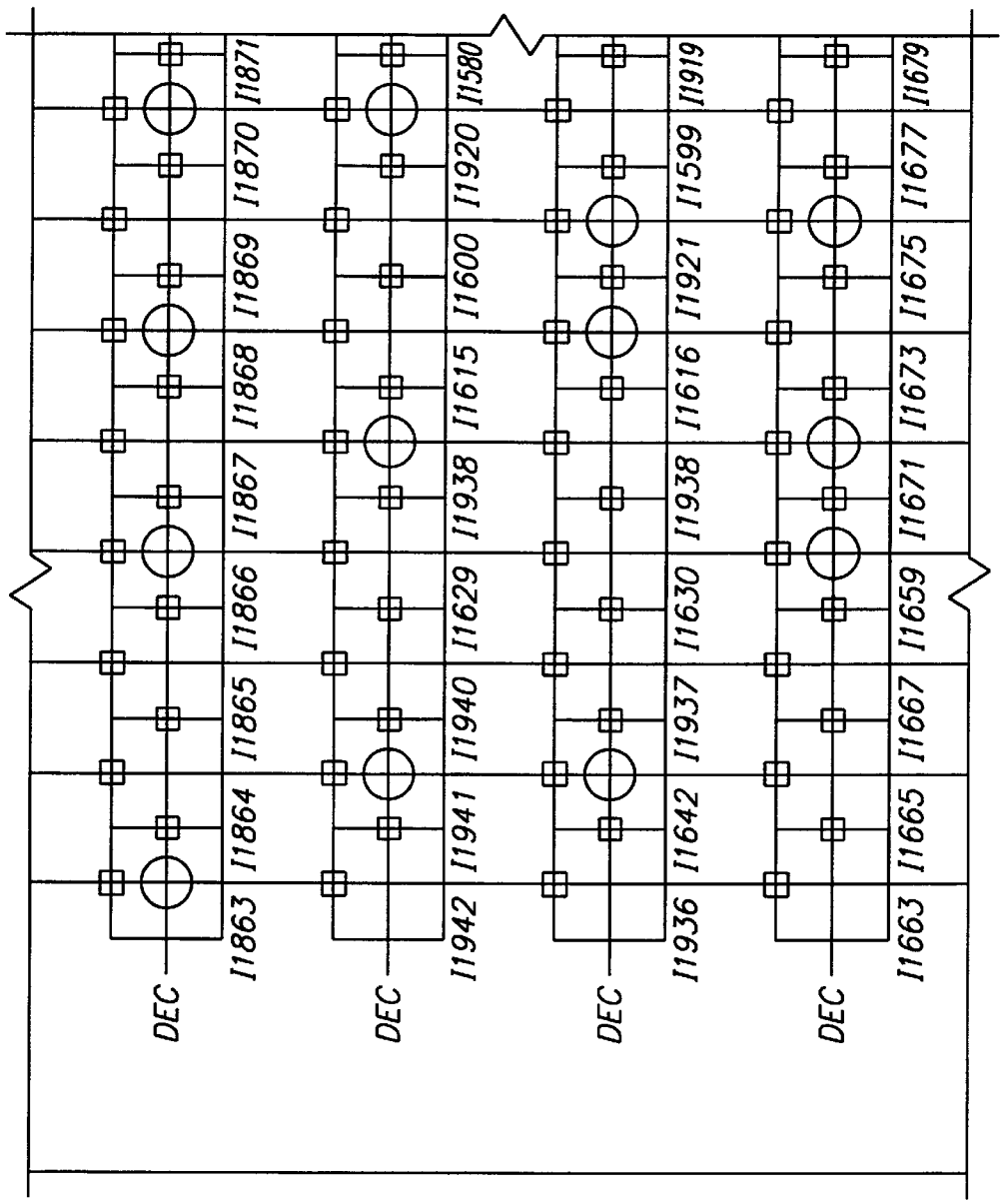

DEC
I1863
I1864
I1865
I1866
I1867
I1868
I1869
I1870
I1871
I1942
I1941
I1940
I1629
I1938
I1615
I1600
I1920
I1580
I1936
I1642
I1937
I1630
I1938
I1616
I1921
I1599
I1919
I1663
I1665
I1667
I1659
I1671
I1673
I1675
I1677
I1679

FIG 756.

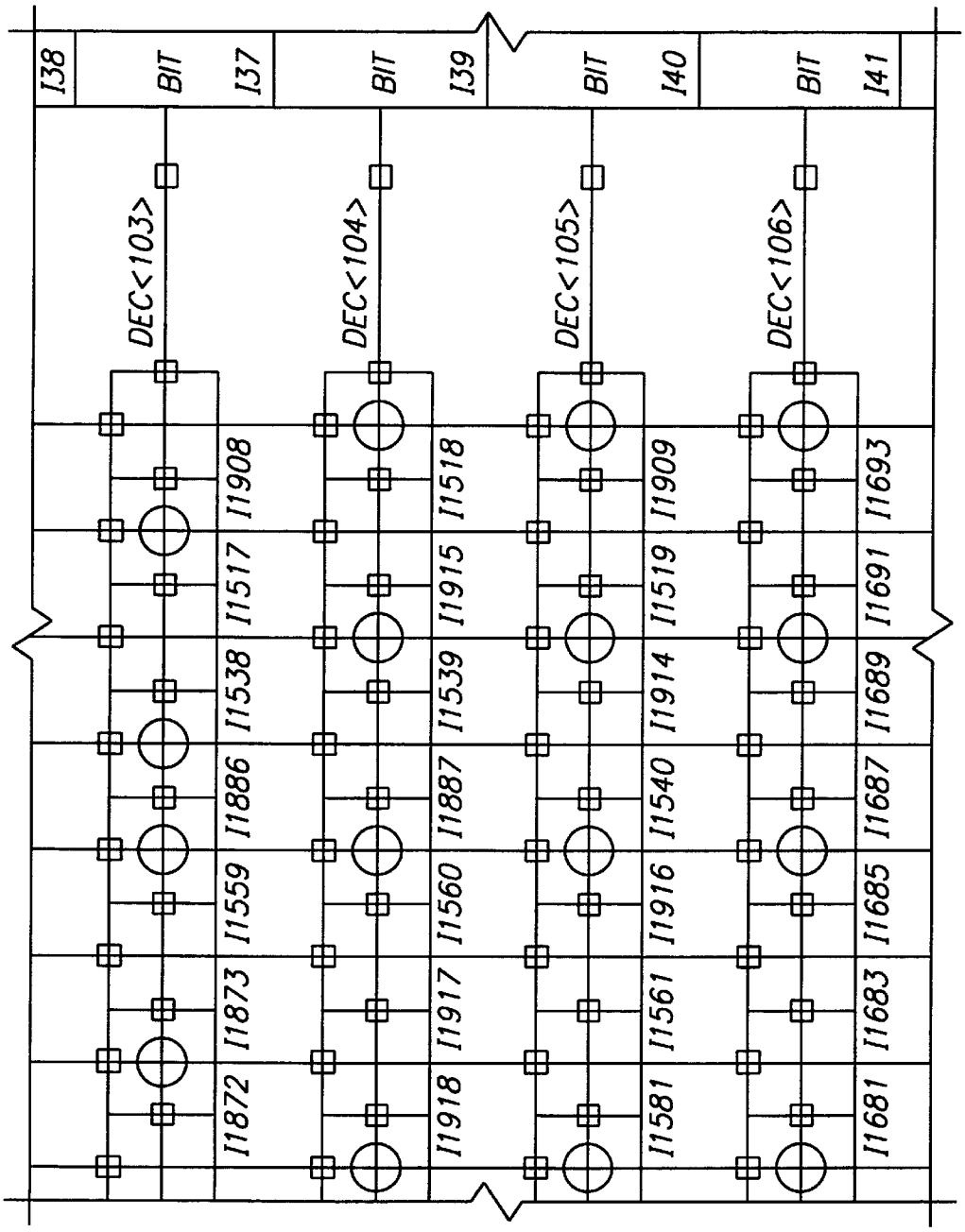

I38
BIT
I37
BIT
I39
BIT
I40
BIT
I41
DEC<103>
DEC<104>
DEC<105>
DEC<106>
I1908
I1517
I1538
I1886
I1559
I1873
I1872
I1518
I1915
I1539
I1887
I1560
I1917
I1918
I1909
I1519
I1914
I1540
I1916
I1561
I1581
I1693
I1691
I1689
I1687
I1685
I1683
I1681

Fig. 1,605,048

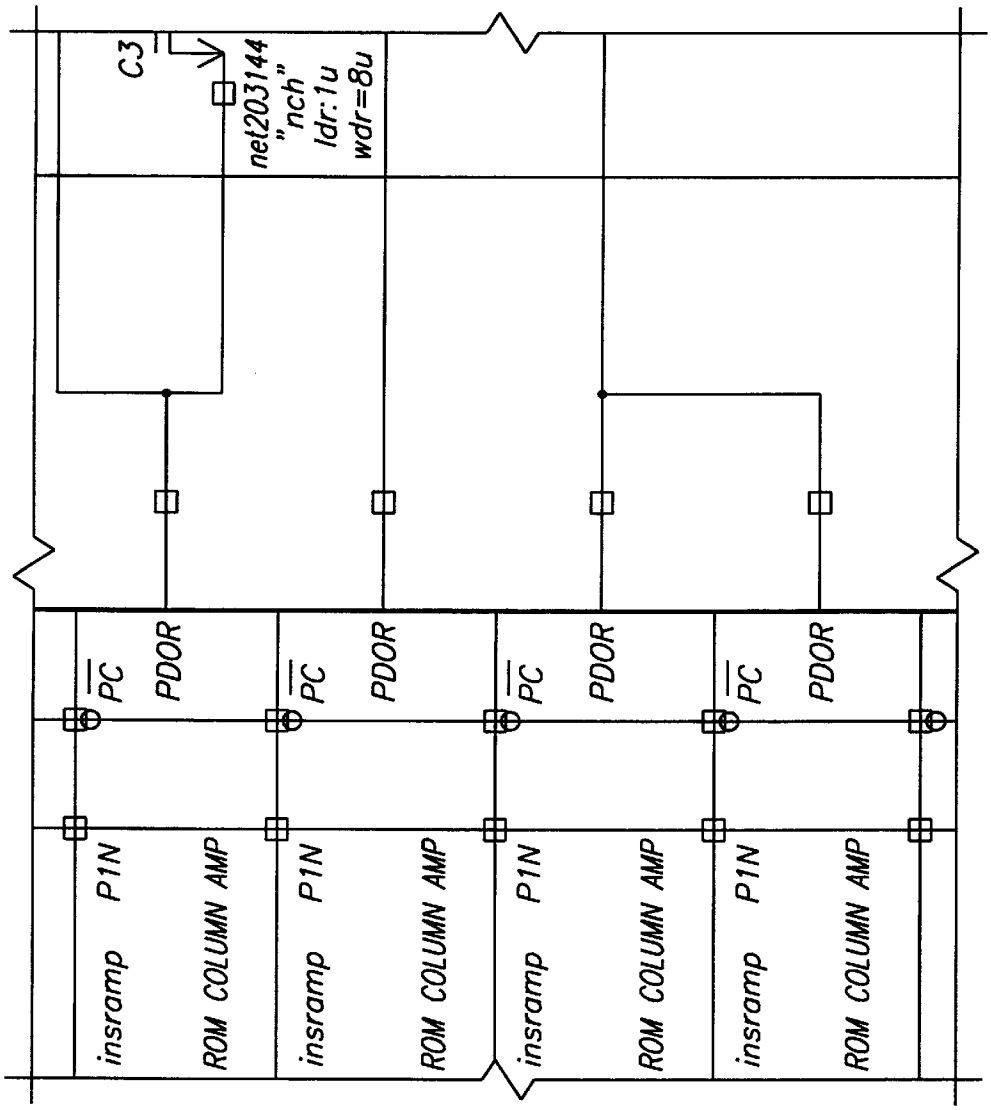

C3
net203144
"nch"
ldr:1u
wdr=8u
PC
PDOR
insramp P1N
ROM COLUMN AMP

FIG. 609.1

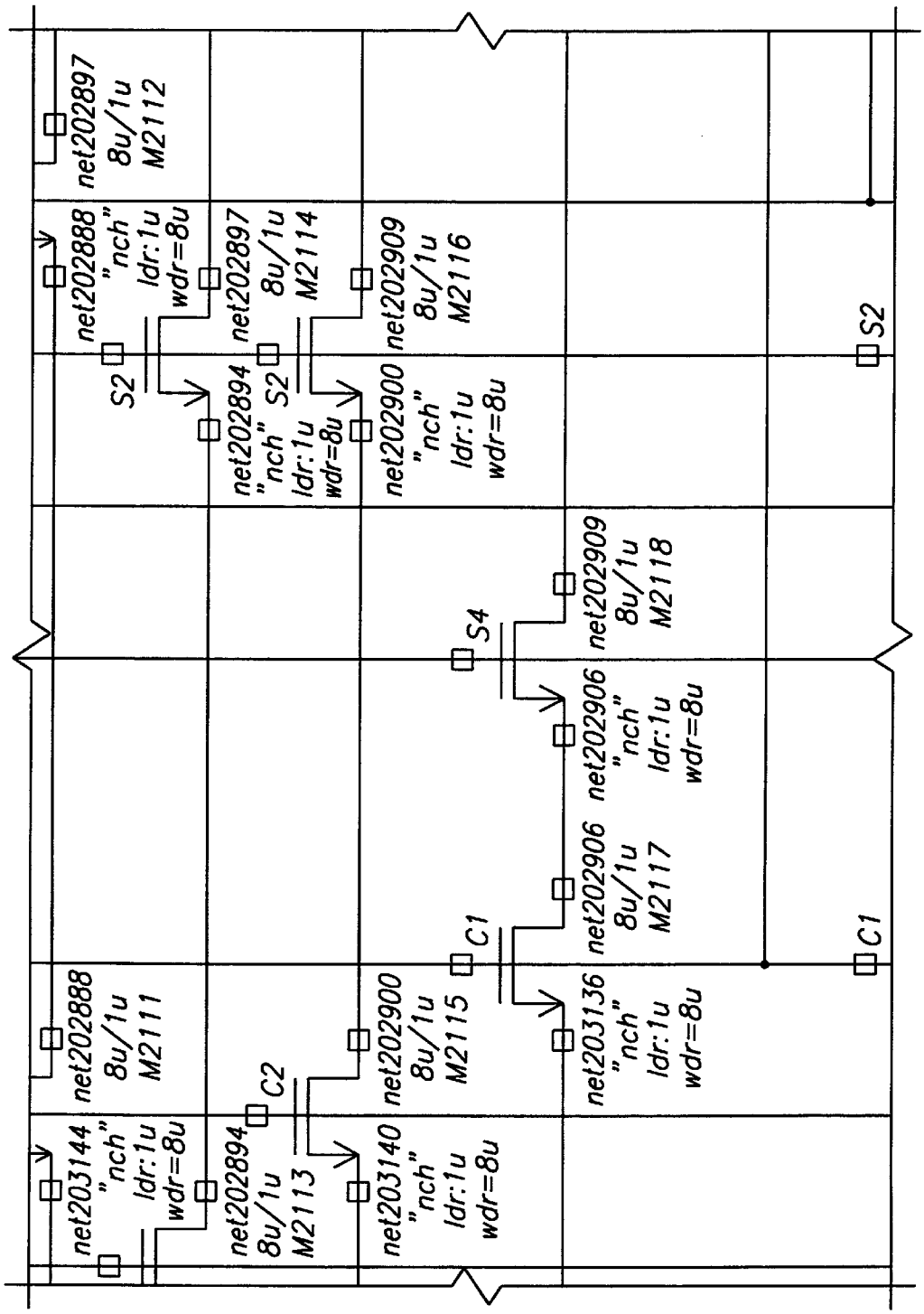

net202897
8u/1u
M2112
net202888
"nch"
ldr:1u
wdr=8u
net202897
8u/1u
M2114
net202909
8u/1u
M2116
S2
net202894
"nch"
ldr:1u
wdr=8u
net202900
"nch"
ldr:1u
wdr=8u
S2
S4
net202909
8u/1u
M2118
net202906
"nch"
ldr:1u
wdr=8u
net202906
8u/1u
M2117
C1
net203136
"nch"
ldr:1u
wdr=8u
net202888
8u/1u
M2111
net202900
8u/1u
M2115
C2
net203144
"nch"
ldr:1u
wdr=8u
net202894
8u/1u
M2113
net203140
"nch"
ldr:1u
wdr=8u

FIG. 6,130,602

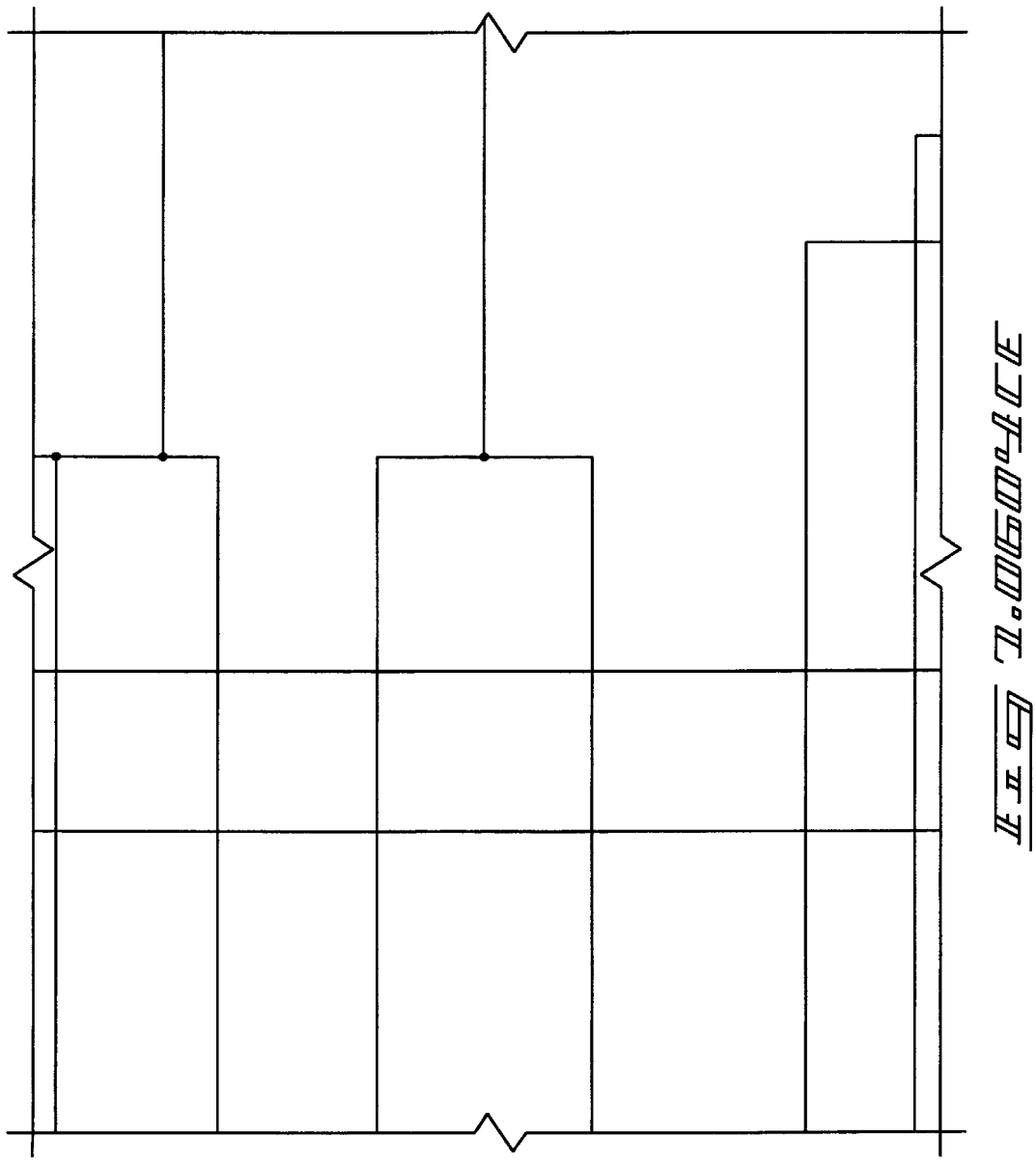


FIG. 1,005,00

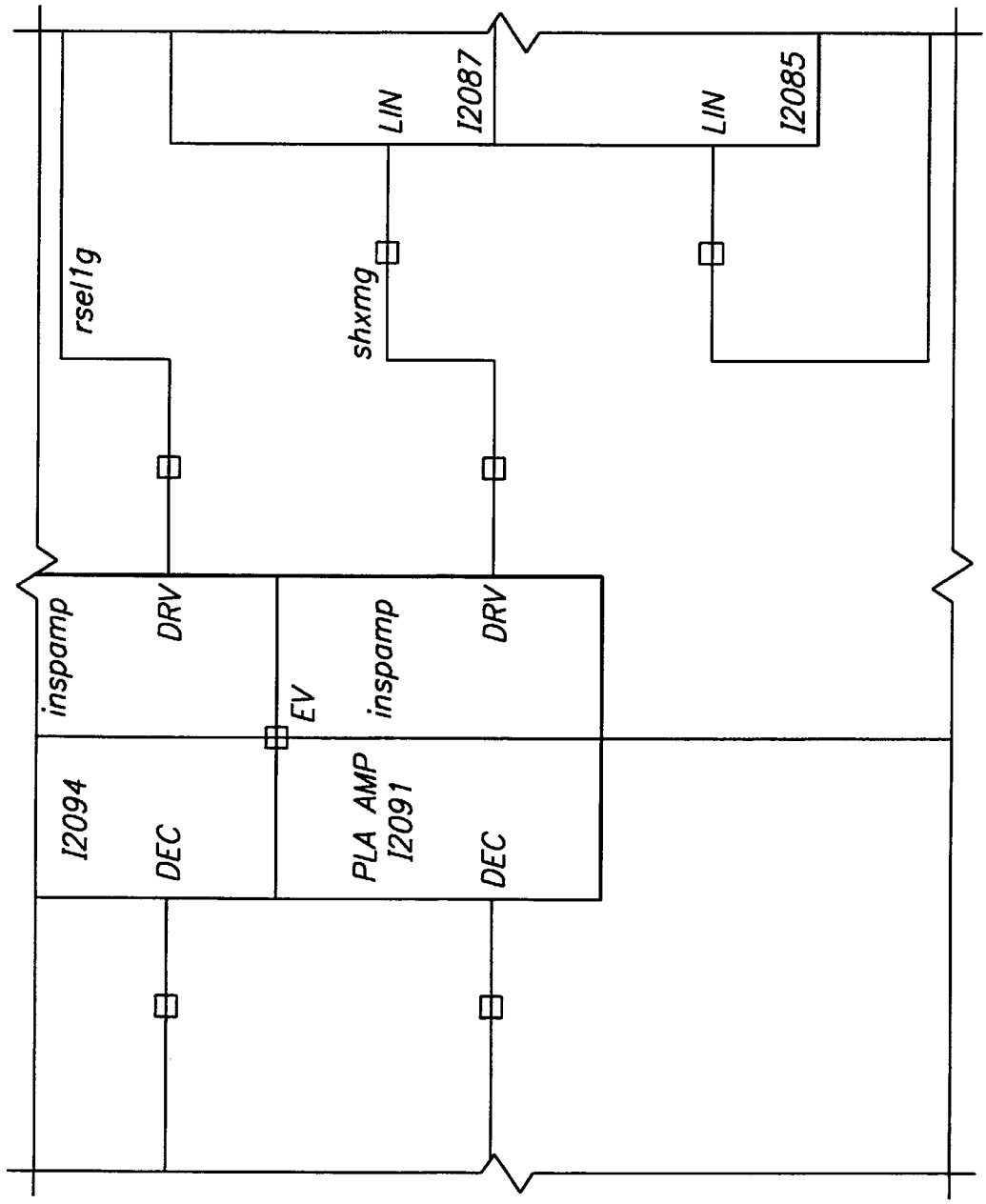

LIN
I2087
LIN
I2085
rsel1g
shxmg
inspamp
DRV
EV
inspamp
DRV
I2094
DEC
PLA AMP
I2091
DEC

FIG. 1.0059.L

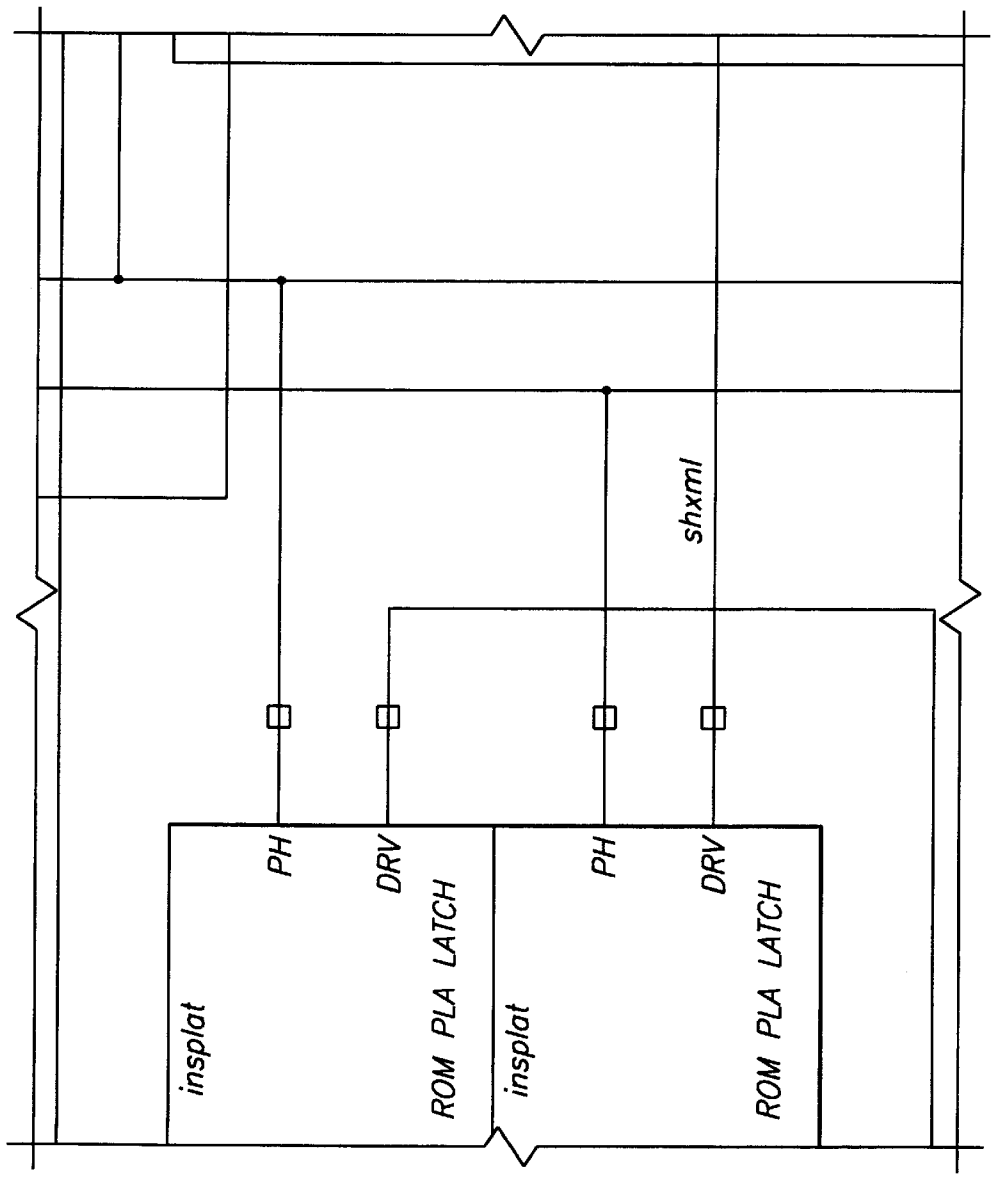


FIG 7L.0059.0473

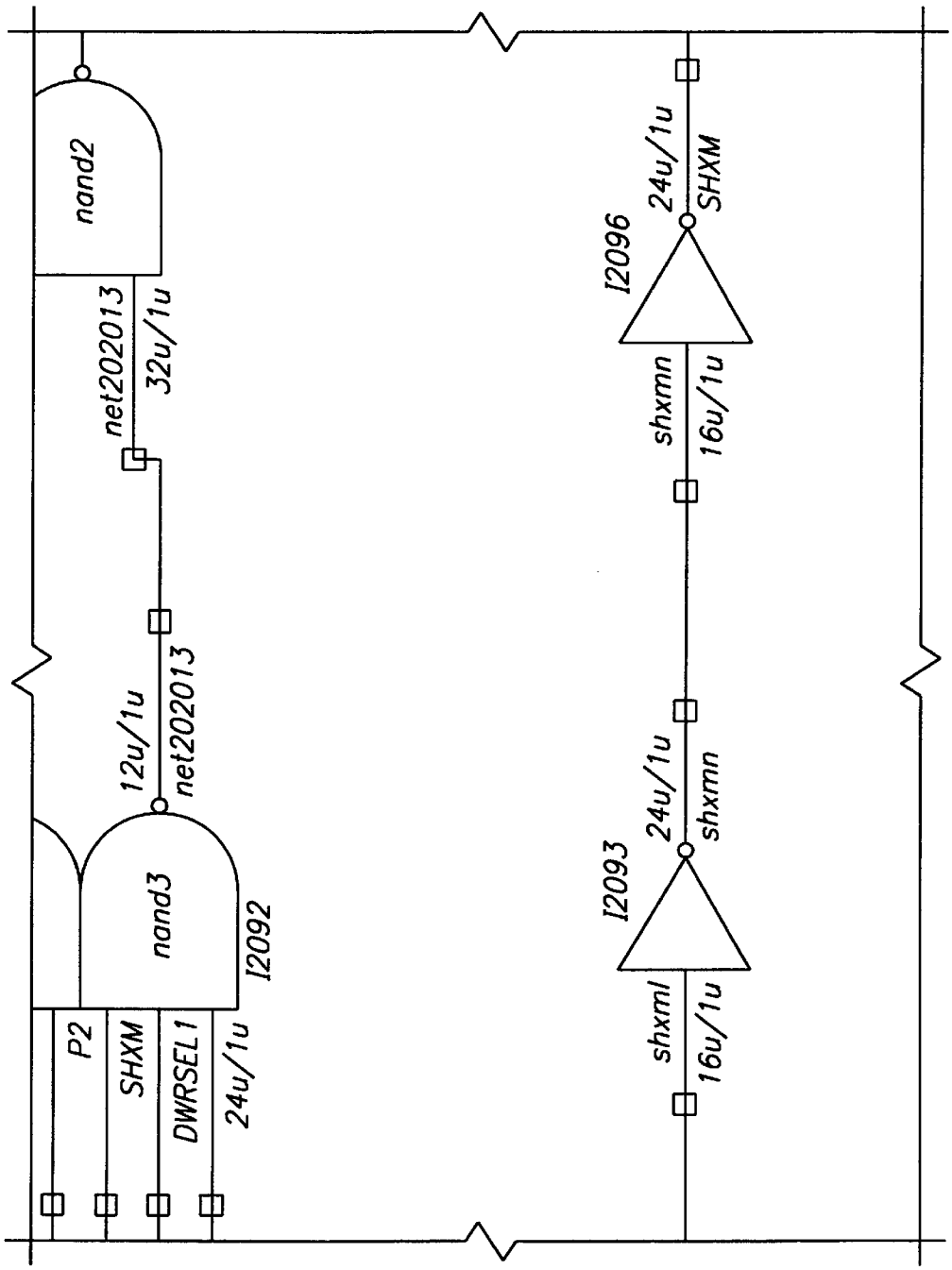

nand2
net202013
32u/1u
12u/1u
net202013
nand3
I2092
P2
SHXM
DWRSEL1
24u/1u
I2096
24u/1u
SHXM
shxmn
16u/1u
I2093
24u/1u
shxmn
shxml
16u/1u

FIG. 1,050,774

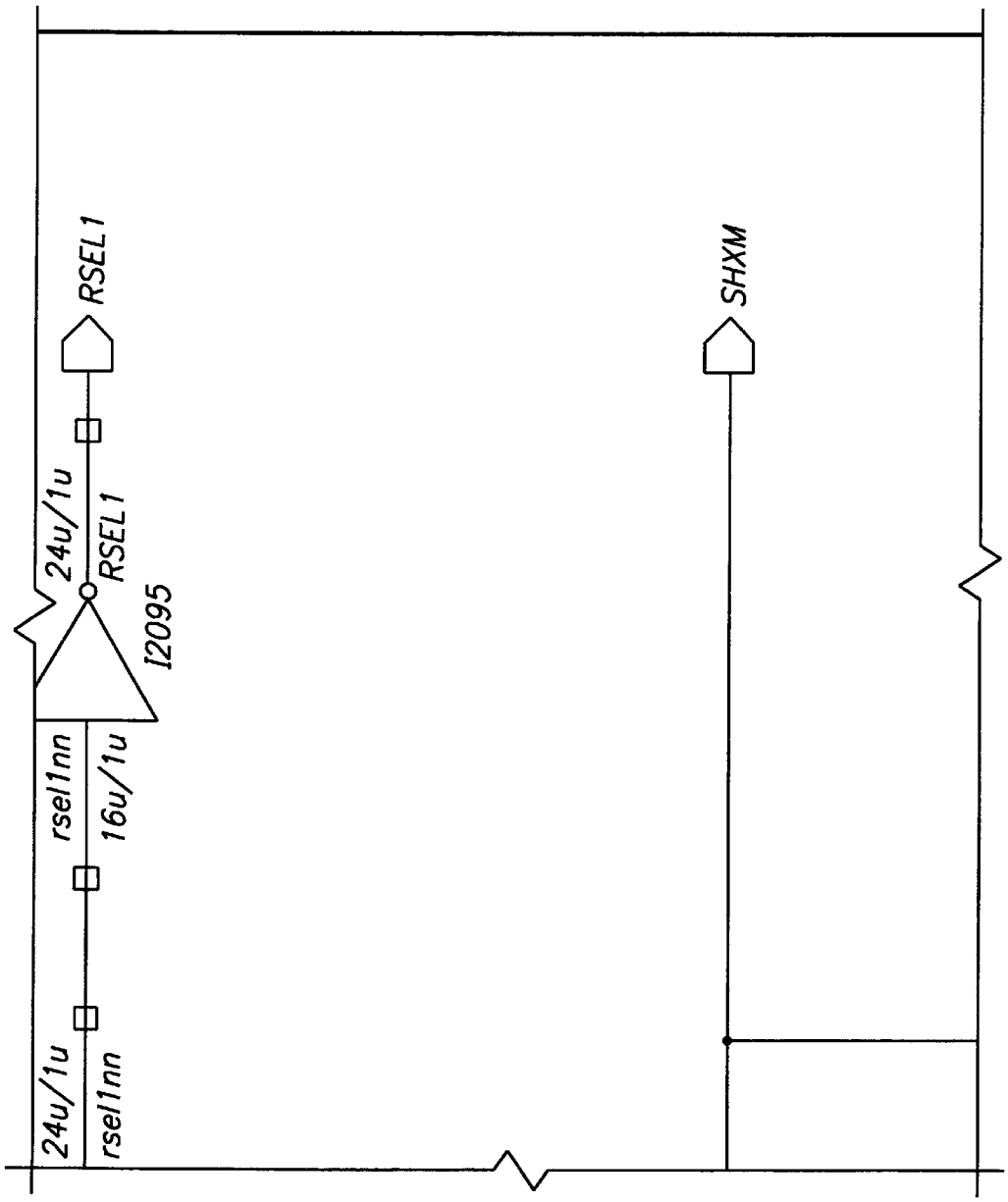


FIG 1.0604CII

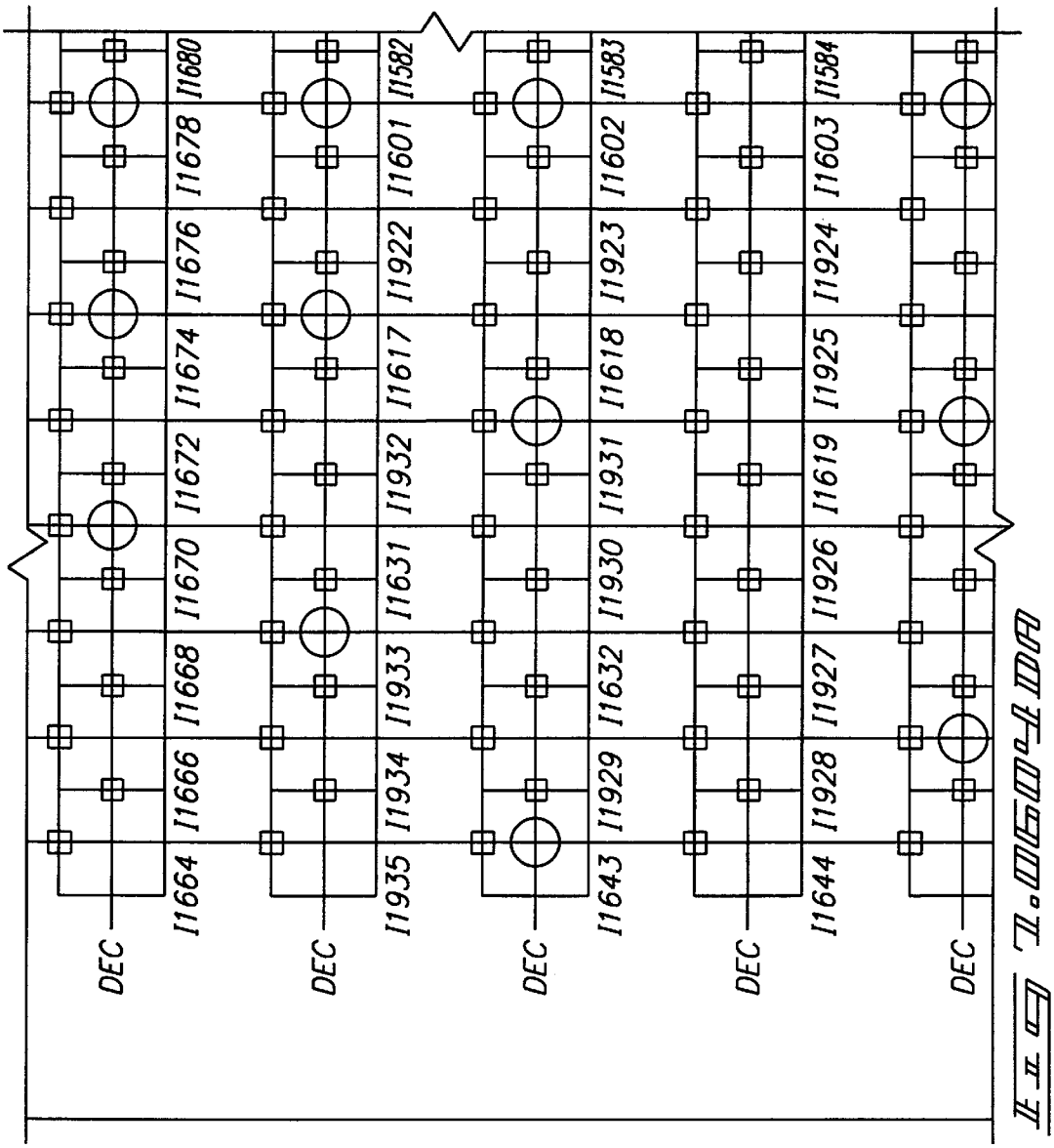


FIG 1.0590-1.0604

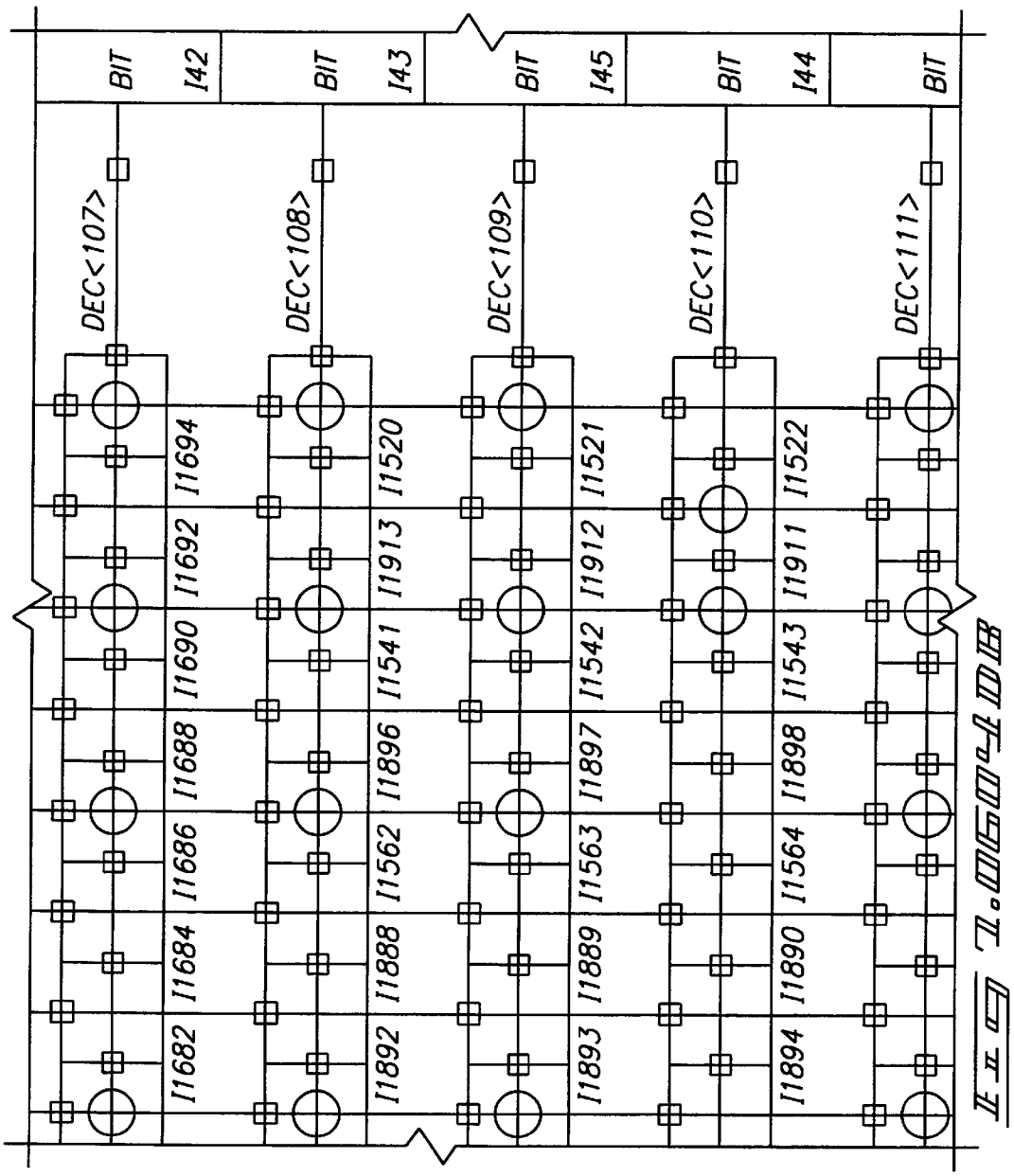
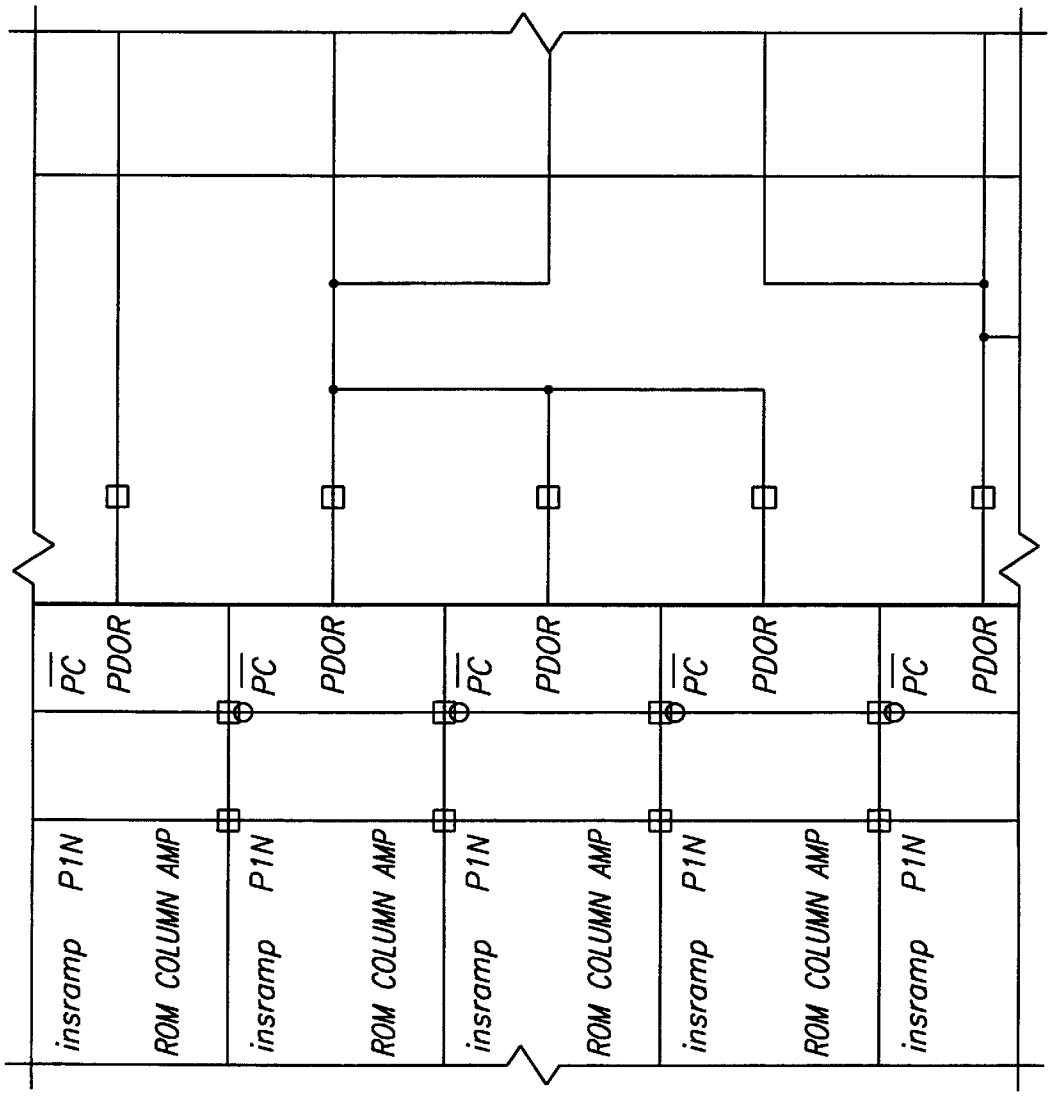

BIT I42
BIT I43
BIT I45
BIT I44
BIT
DEC<107>
DEC<108>
DEC<109>
DEC<110>
DEC<111>
I1682 I1684 I1686 I1688 I1690 I1692 I1694
I1892 I1888 I1562 I1896 I1541 I1913 I1520
I1893 I1889 I1563 I1897 I1542 I1912 I1521
I1894 I1890 I1564 I1898 I1543 I1911 I1522

FIG 1,005,00'L



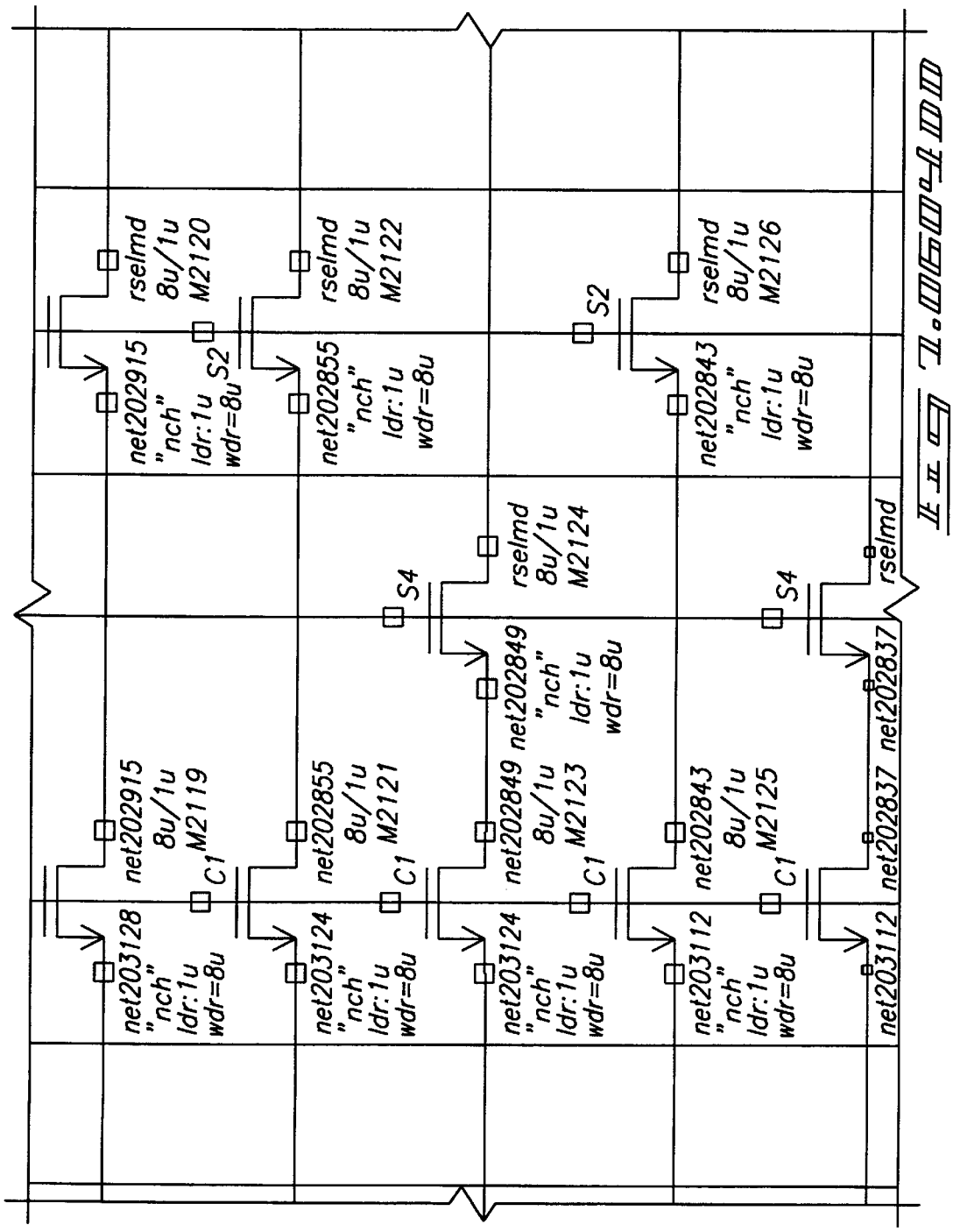
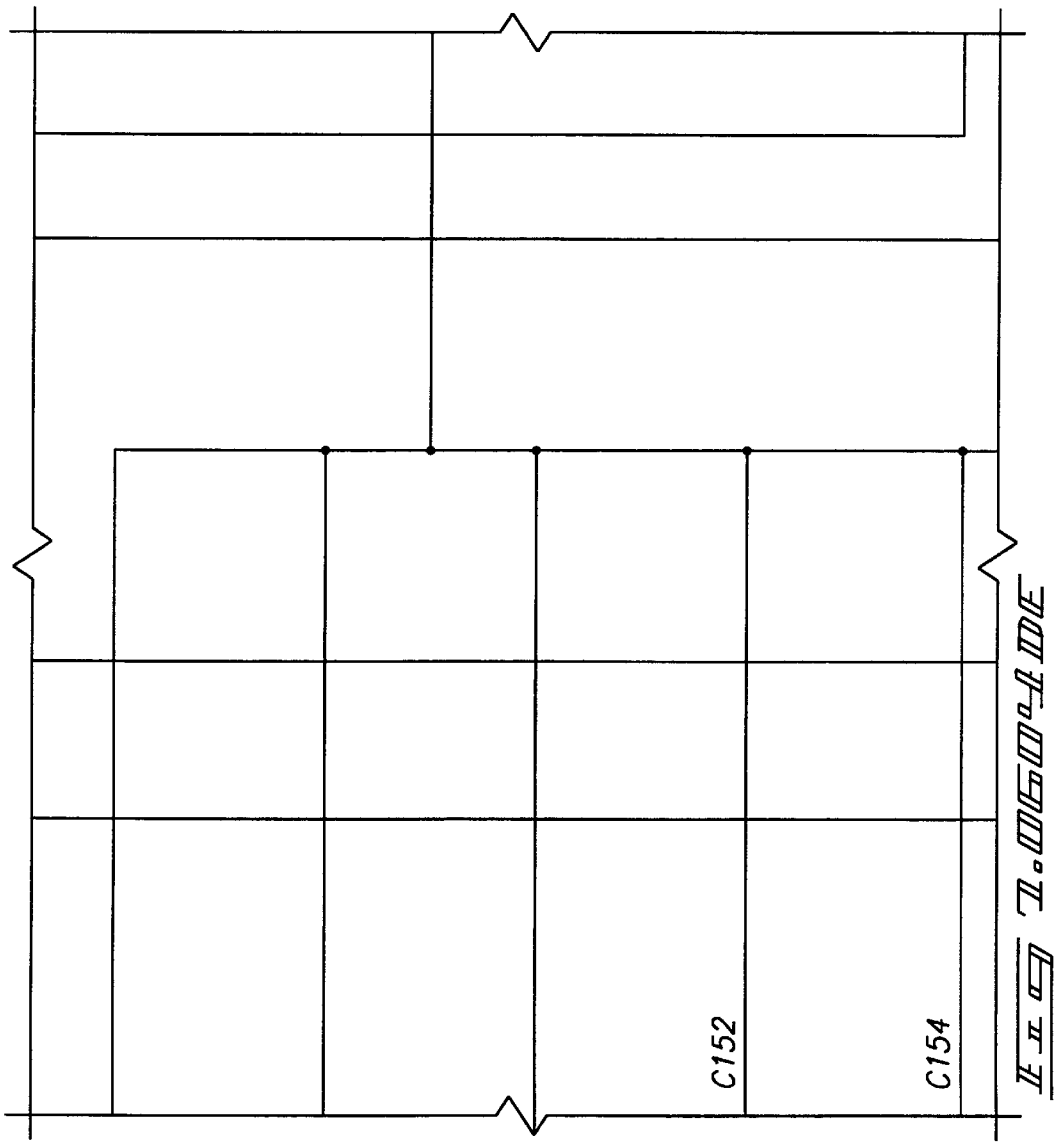
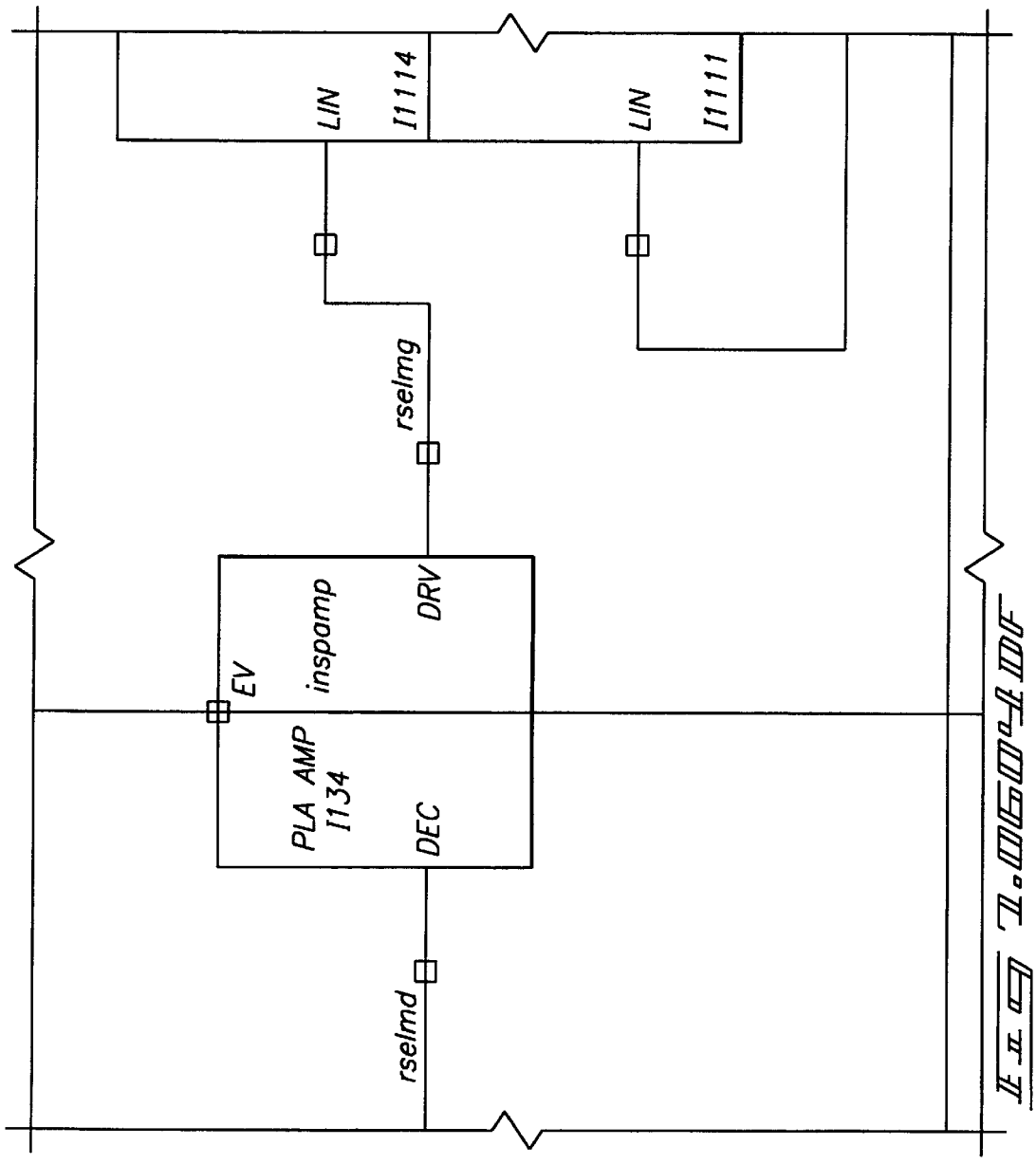

net202915 "nch" ldr:1u wdr=8u
rselmd 8u/1u M2120
S2
net202855 "nch" ldr:1u wdr=8u
rselmd 8u/1u M2122
S2
net202843 "nch" ldr:1u wdr=8u
rselmd 8u/1u M2126
S4
rselmd 8u/1u M2124
S4
rselmd
net202915 8u/1u M2119
C1
net202855 8u/1u M2121
C1
net202849 8u/1u M2123
C1
net202843 8u/1u M2125
C1
net202837
net203128 "nch" ldr:1u wdr=8u
net203124 "nch" ldr:1u wdr=8u
net203124 "nch" ldr:1u wdr=8u
net203112 "nch" ldr:1u wdr=8u
net202837
net203112

Fig. 1,605,401


C152
C154


LIN
I1114
LIN
I1111
rselmg
DRV
inspamp
EV
PLA AMP
I134
DEC
rselmd
FIG 770.0500.L

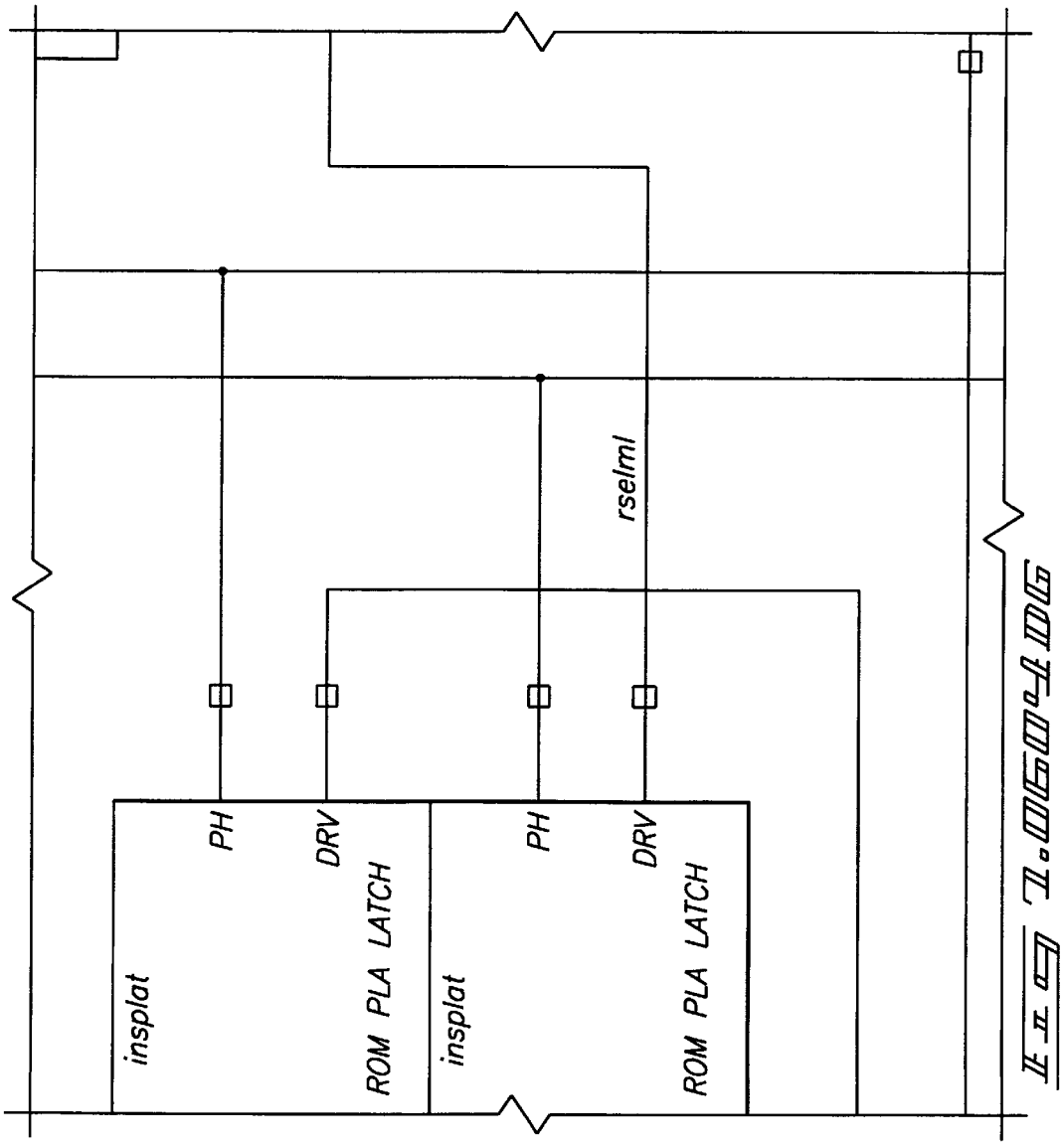
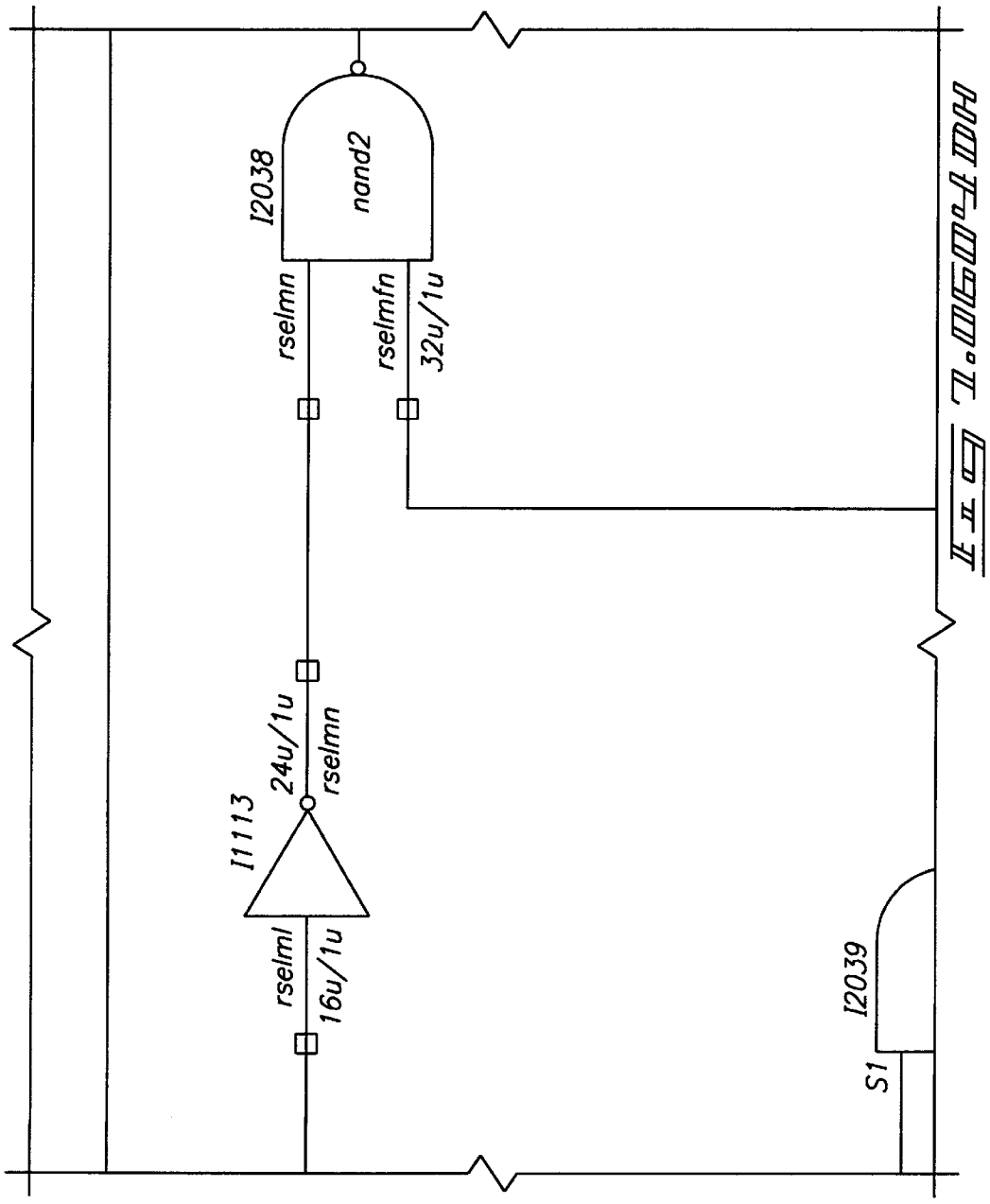

rselml
PH
DRV
ROM PLA LATCH
insplat
PH
DRV
ROM PLA LATCH
insplat

FIG 1,060,405


I2038
nand2
rselmn
rselmfn
32u/1u
24u/1u
rselmn
I1113
rselml
16u/1u
I2039
S1

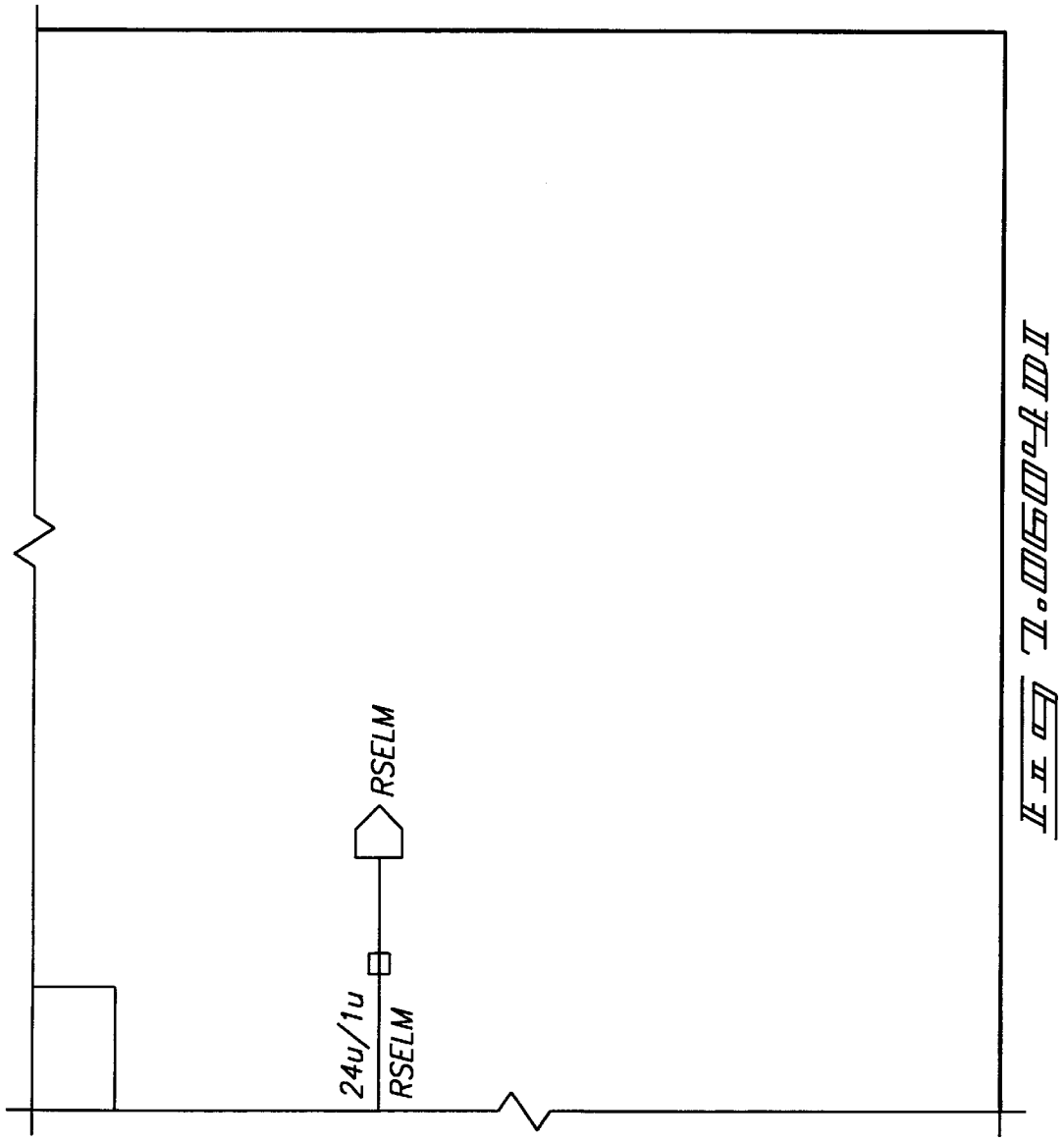


FIG. 773
RSELM
24u/1u
RSELM

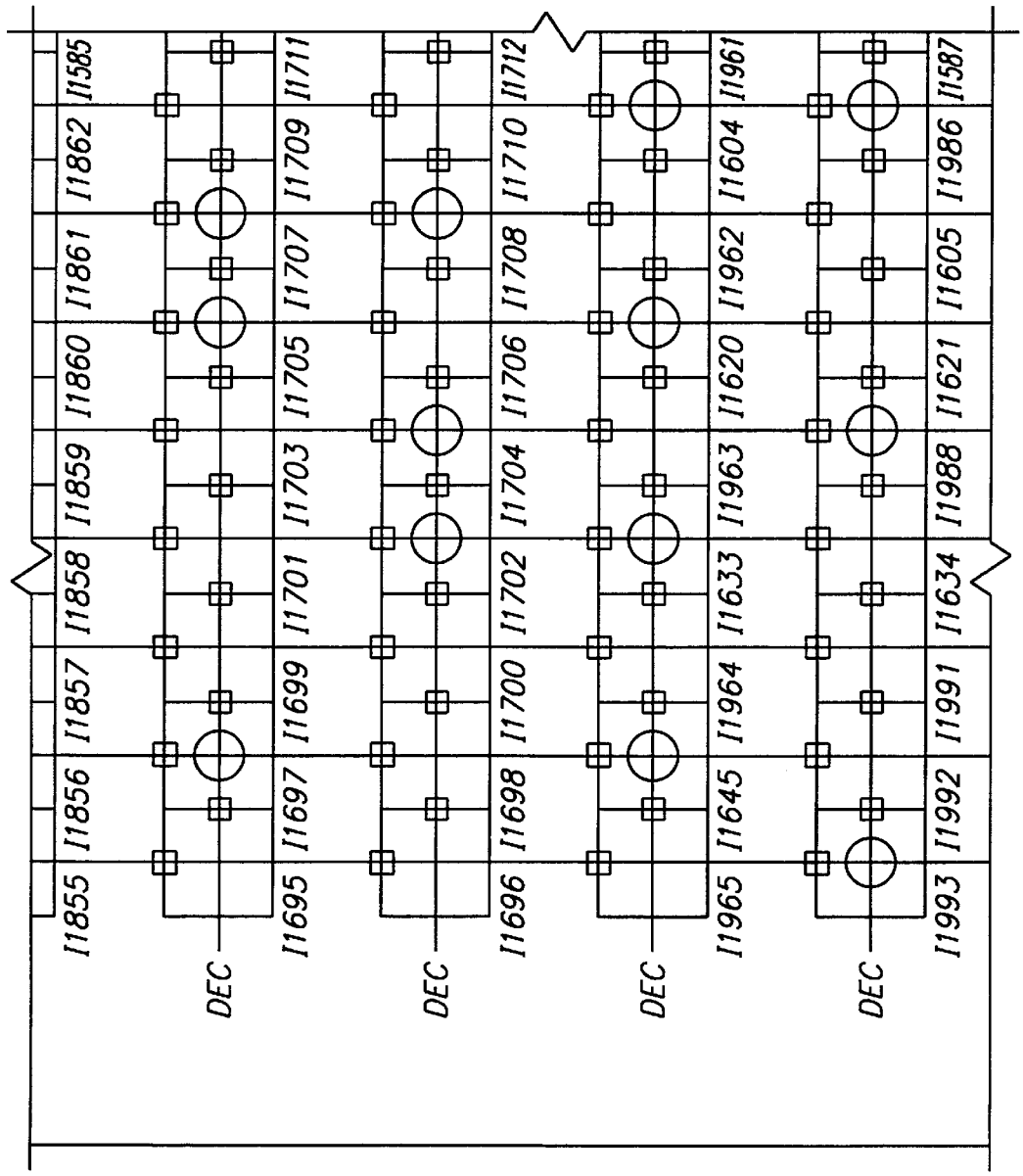

I1855
I1856
I1857
I1858
I1859
I1860
I1861
I1862
I1585
I1695
I1697
I1699
I1701
I1703
I1705
I1707
I1709
I1711
I1696
I1698
I1700
I1702
I1704
I1706
I1708
I1710
I1712
I1965
I1645
I1964
I1633
I1963
I1620
I1962
I1604
I1961
I1993
I1992
I1991
I1634
I1988
I1621
I1605
I1986
I1587
DEC
DEC
DEC
DEC

FIG. 1150

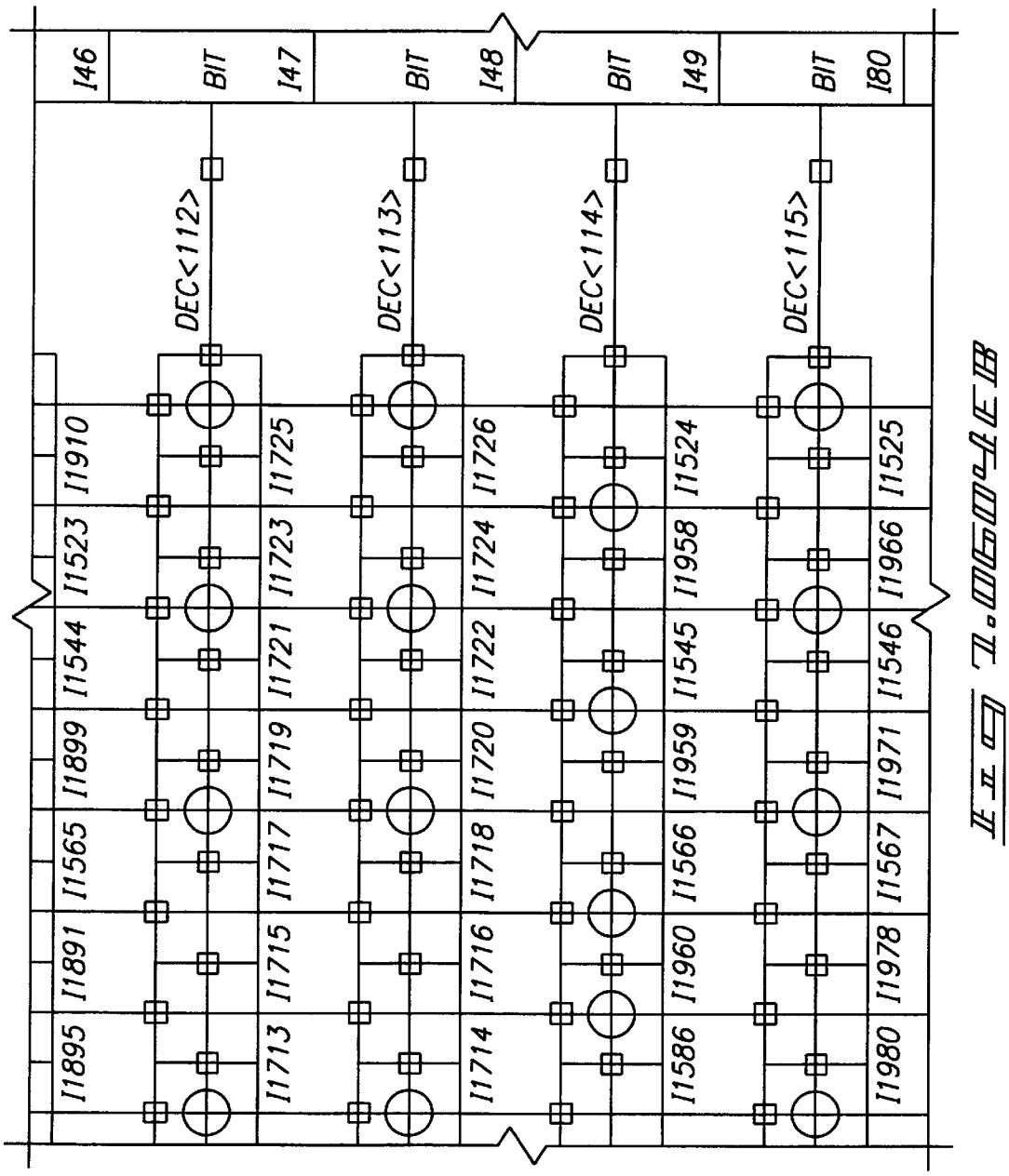

I46
BIT
I47
I48
I49
I80
DEC<112>
DEC<113>
DEC<114>
DEC<115>
I1910
I1523
I1544
I1899
I1565
I1891
I1895
I1725
I1723
I1721
I1719
I1717
I1715
I1713
I1726
I1724
I1722
I1720
I1718
I1716
I1714
I1524
I1958
I1545
I1959
I1566
I1960
I1586
I1525
I1966
I1546
I1971
I1567
I1978
I1980

Fig. 1,005,944

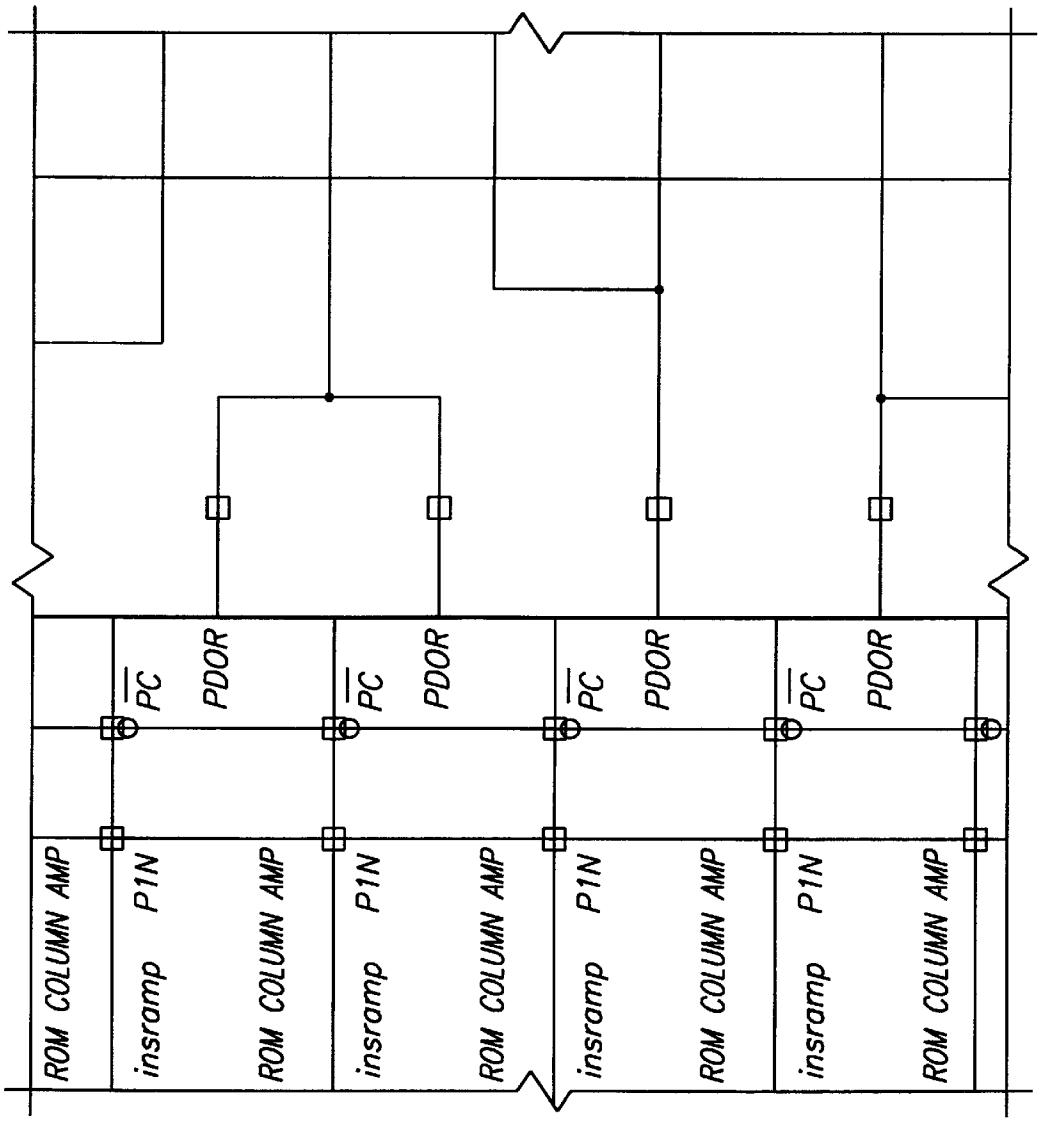

ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
PC
PDOR
PC
PDOR
PC
PDOR
PC
PDOR

FIG. 776

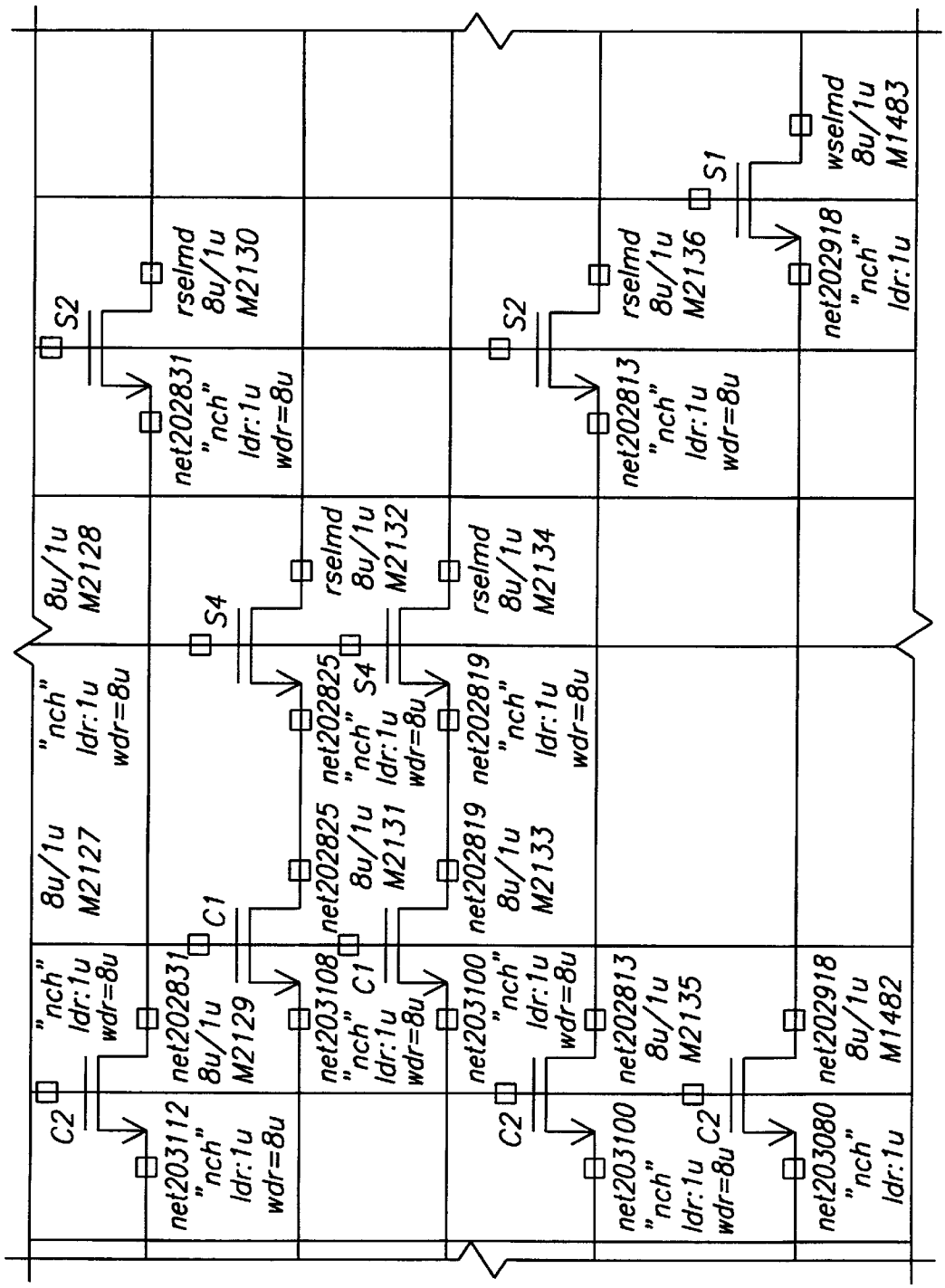
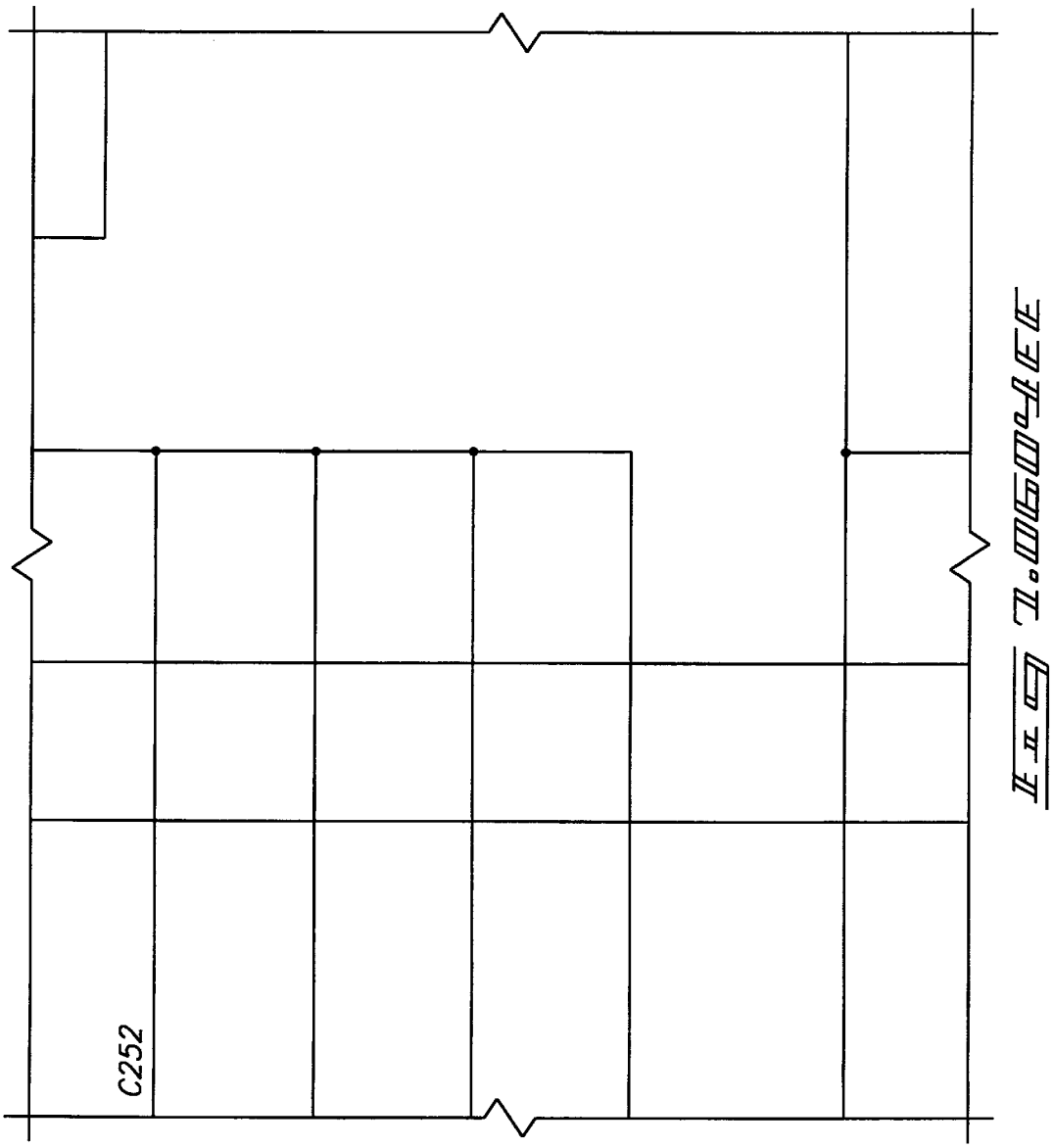


FIG. 1,063,464E


C252
3.0590'' E
E3

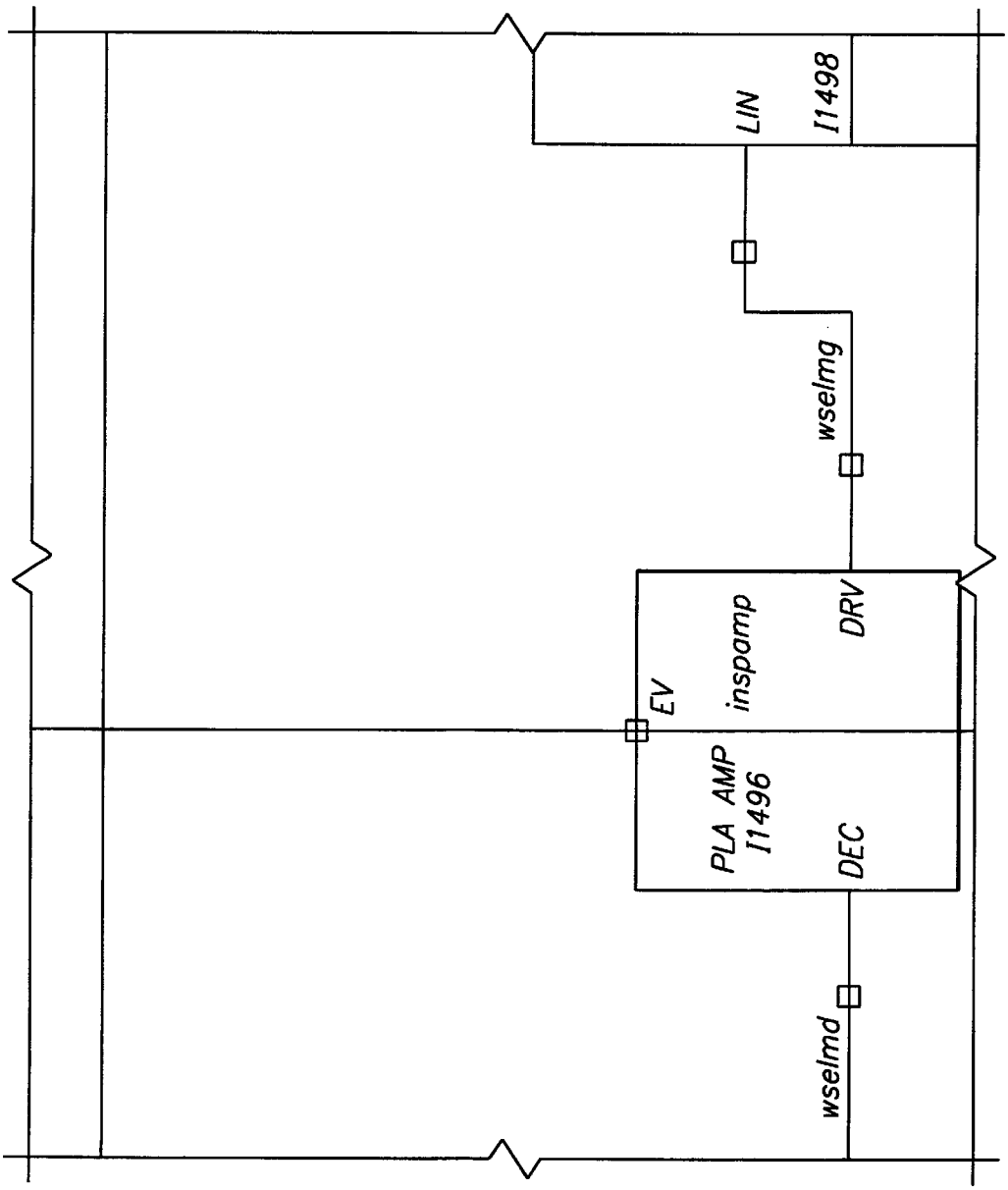


FIG. 1,060,415

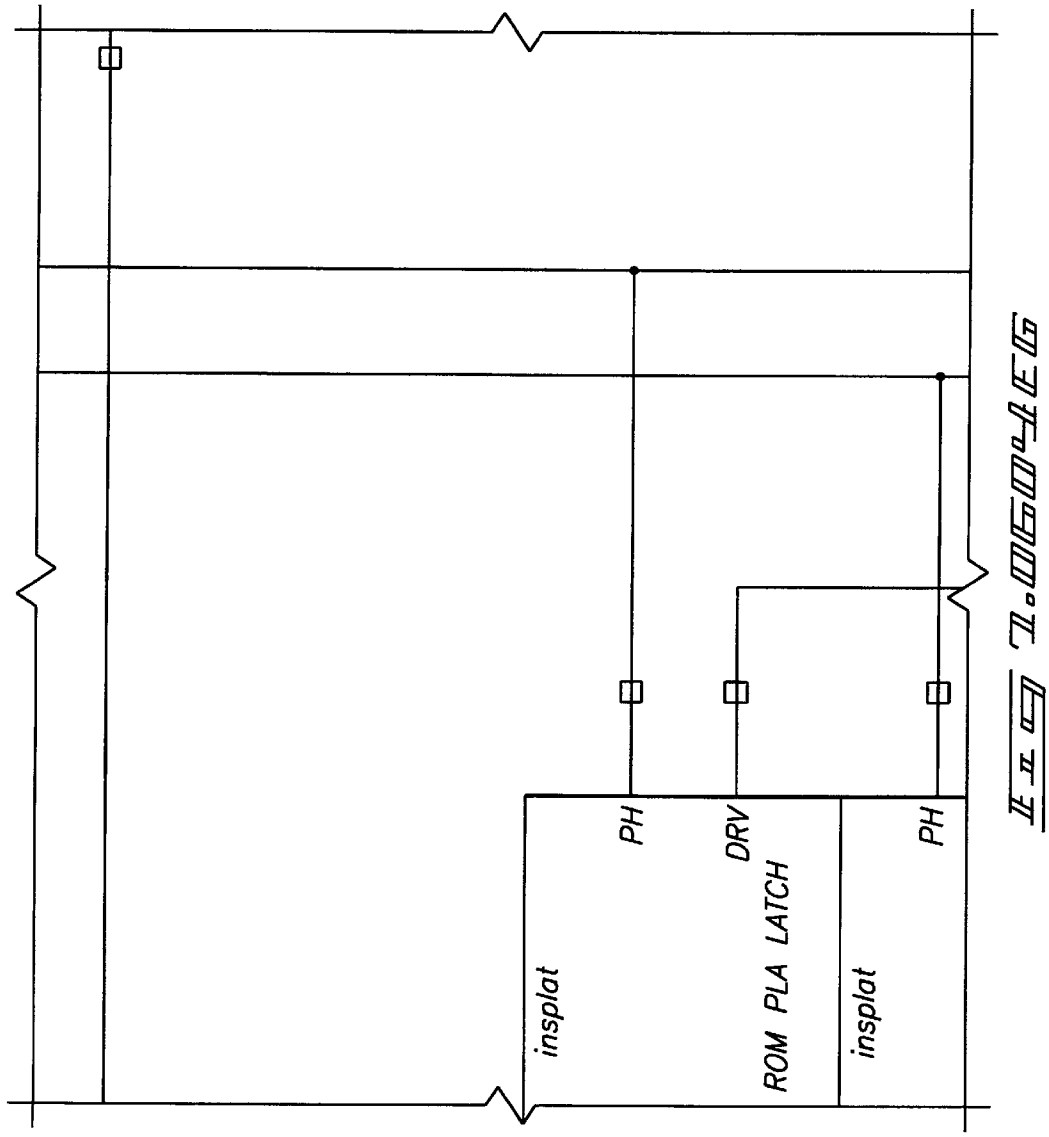


FIG 1.0604E
PH
DRV
PH
ROM PLA LATCH
insplat
insplat

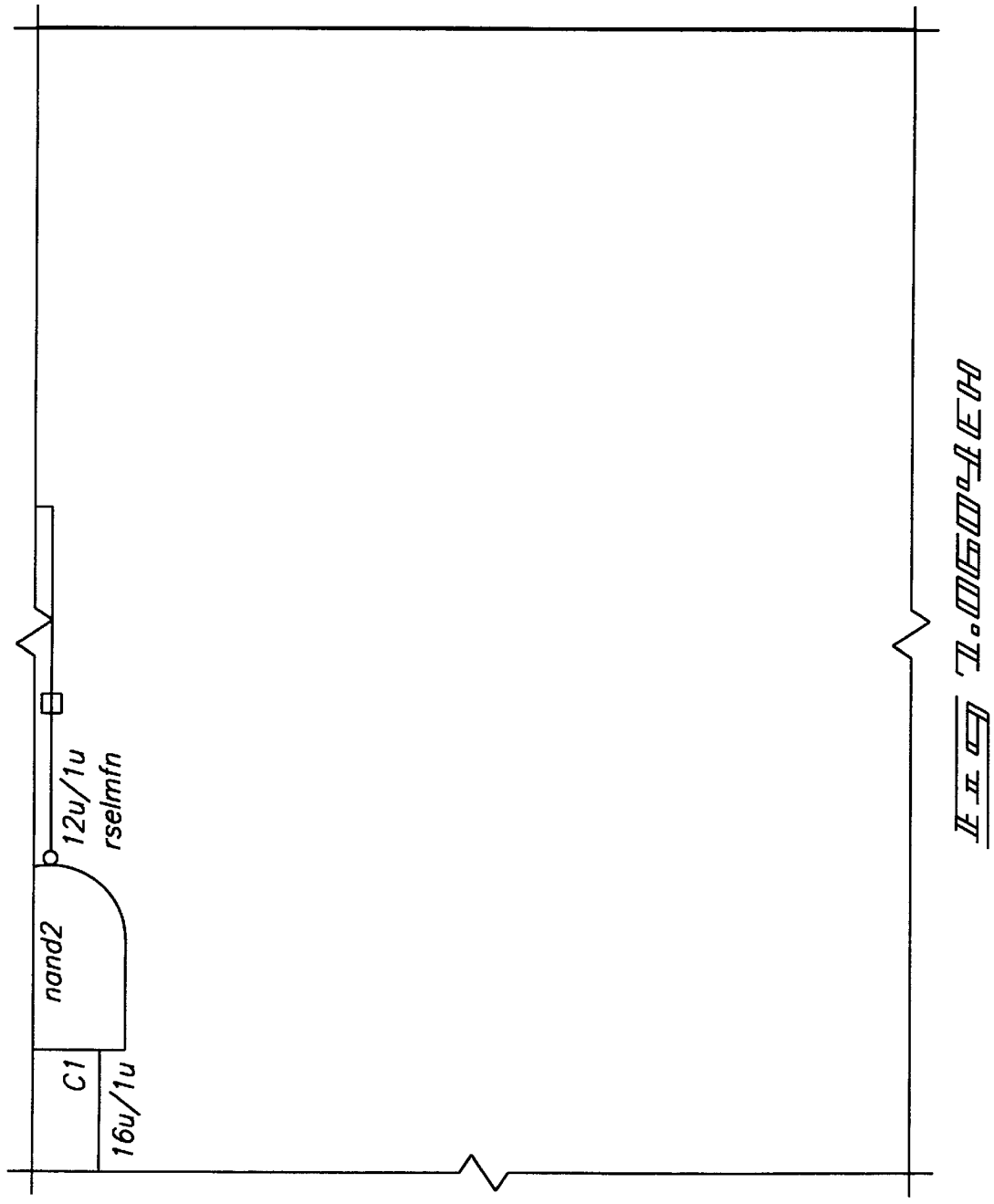


FIG. 780
12u/1u
rselmfn
nand2
C1
16u/1u

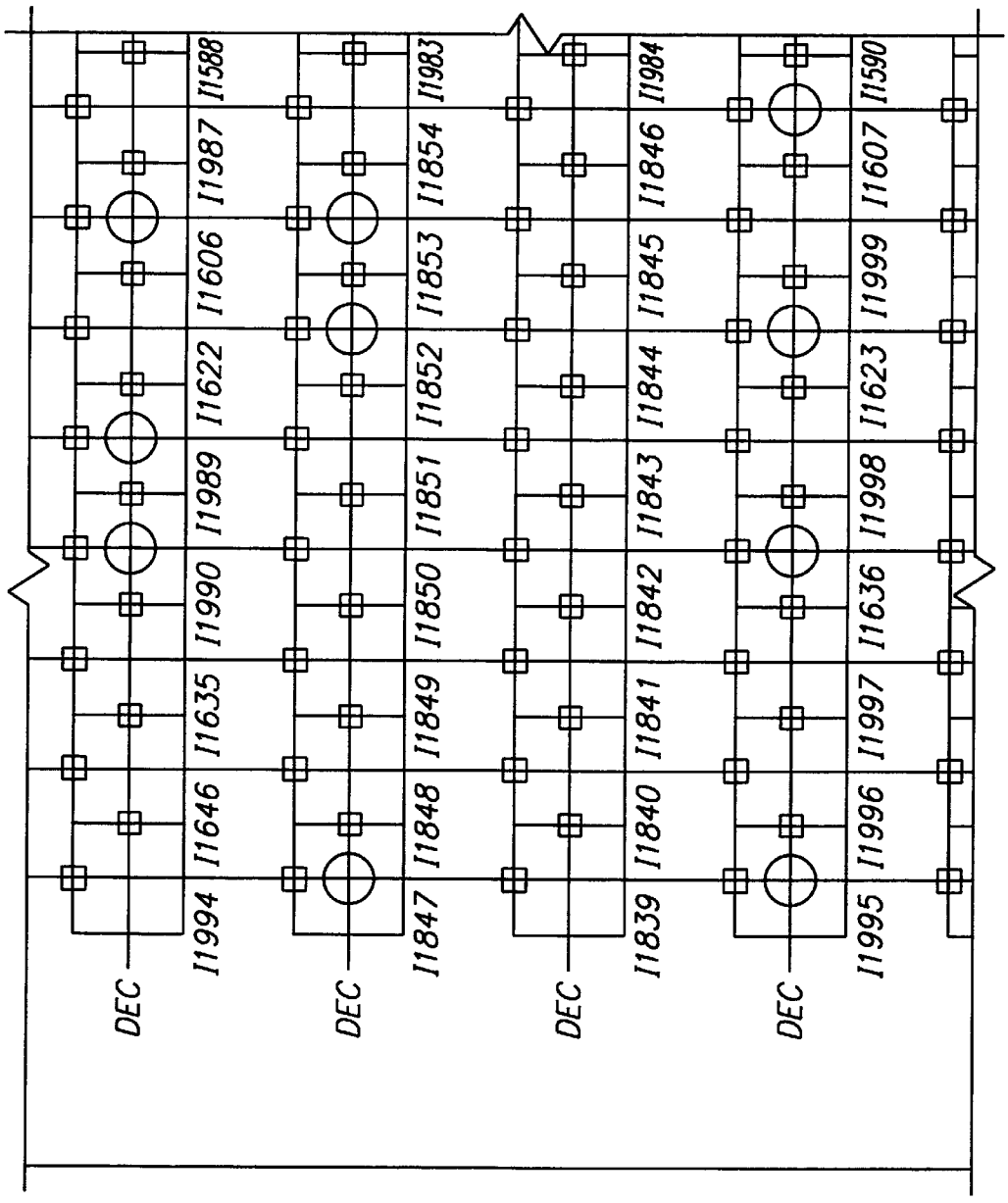

DEC
DEC
DEC
DEC
I1994
I1646
I1635
I1990
I1989
I1622
I1606
I1987
I1588
I1847
I1848
I1849
I1850
I1851
I1852
I1853
I1854
I1983
I1839
I1840
I1841
I1842
I1843
I1844
I1845
I1846
I1984
I1995
I1996
I1997
I1636
I1998
I1623
I1999
I1607
I1590

FIG 1600A

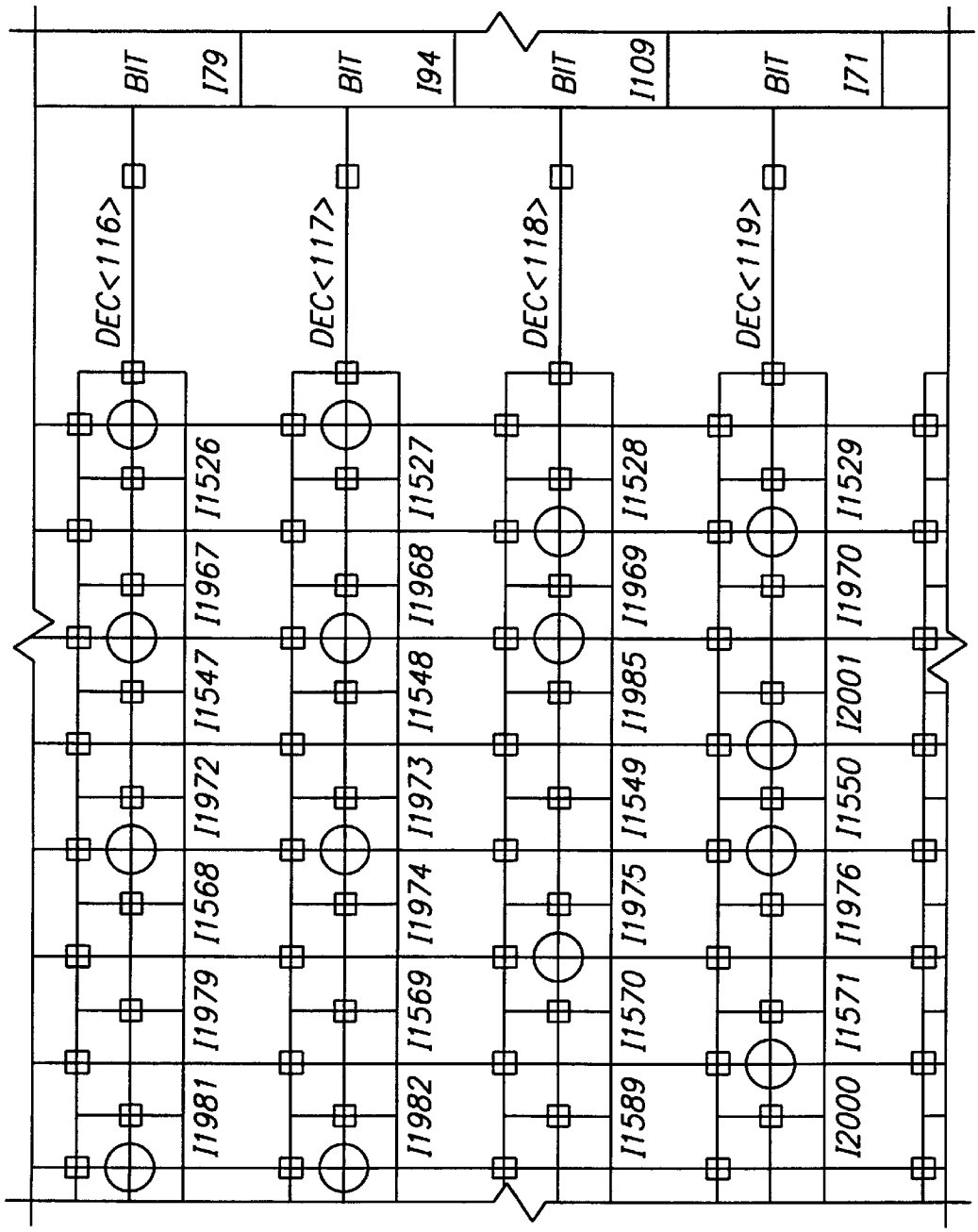


FIG. 1,605,047B

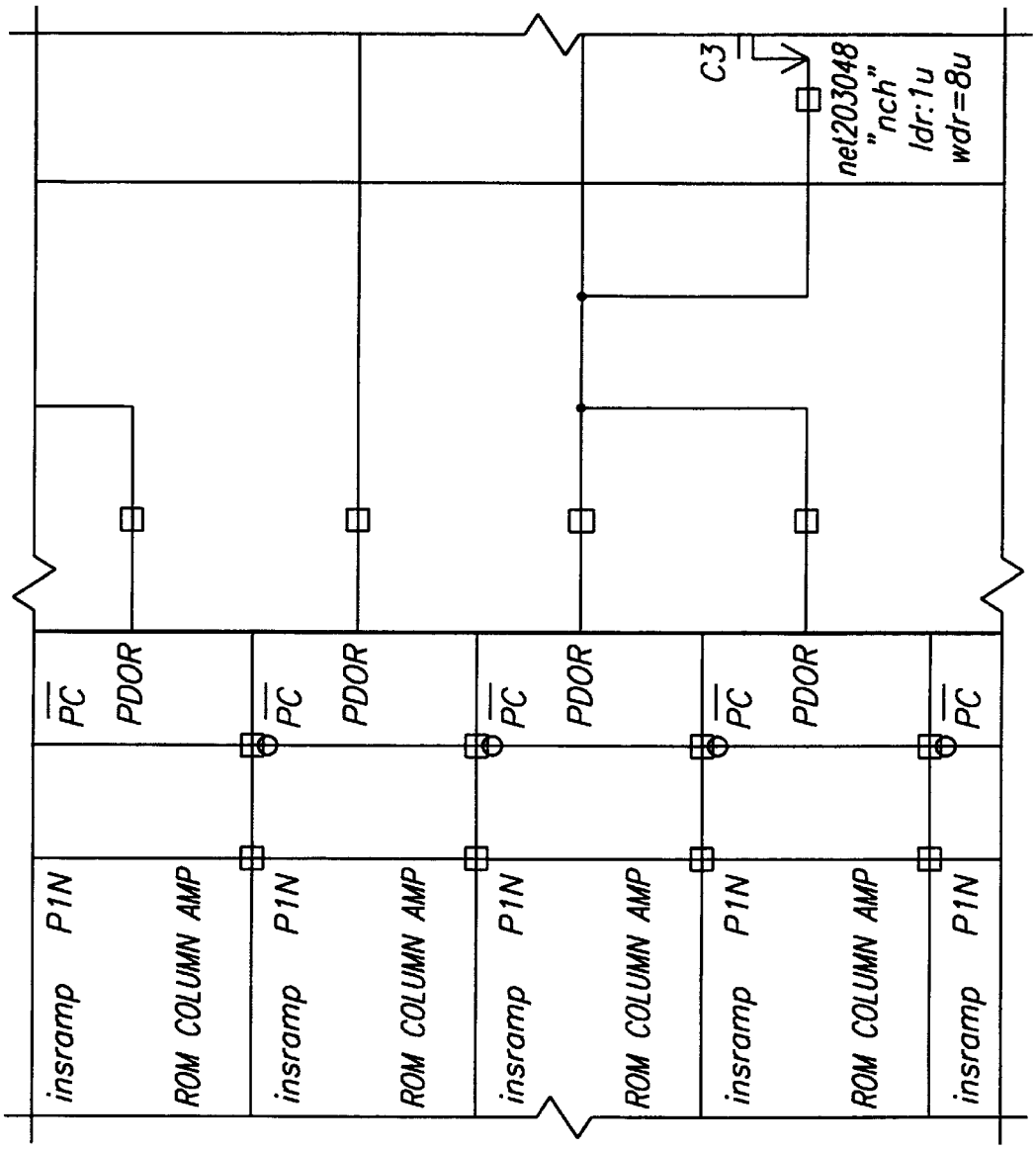

C3
net203048
"nch"
ldr:1u
wdr=8u
PC
PDOR
insramp
P1N
ROM COLUMN AMP

FIG. 6,130,602

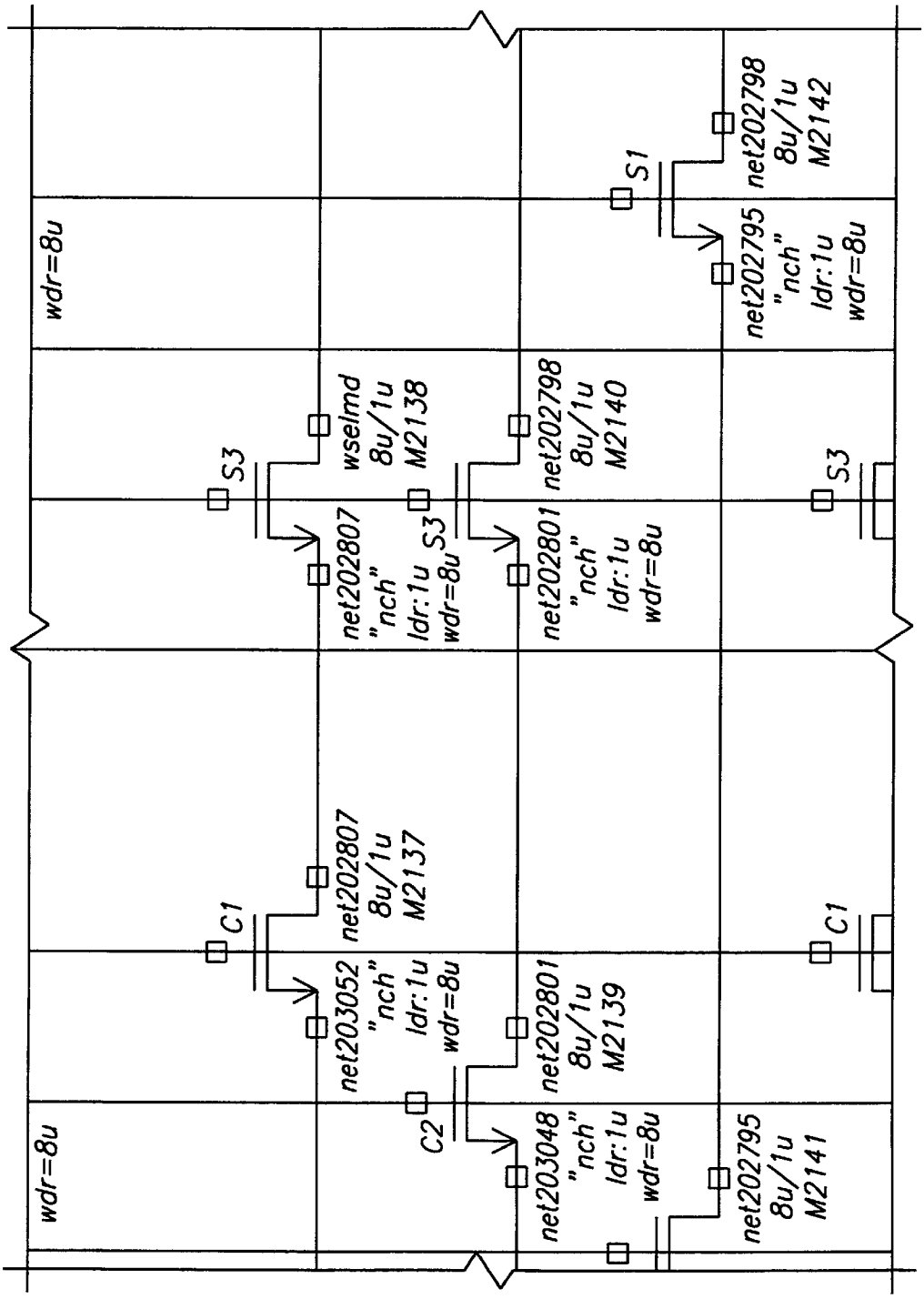


FIG 1.0604FIG

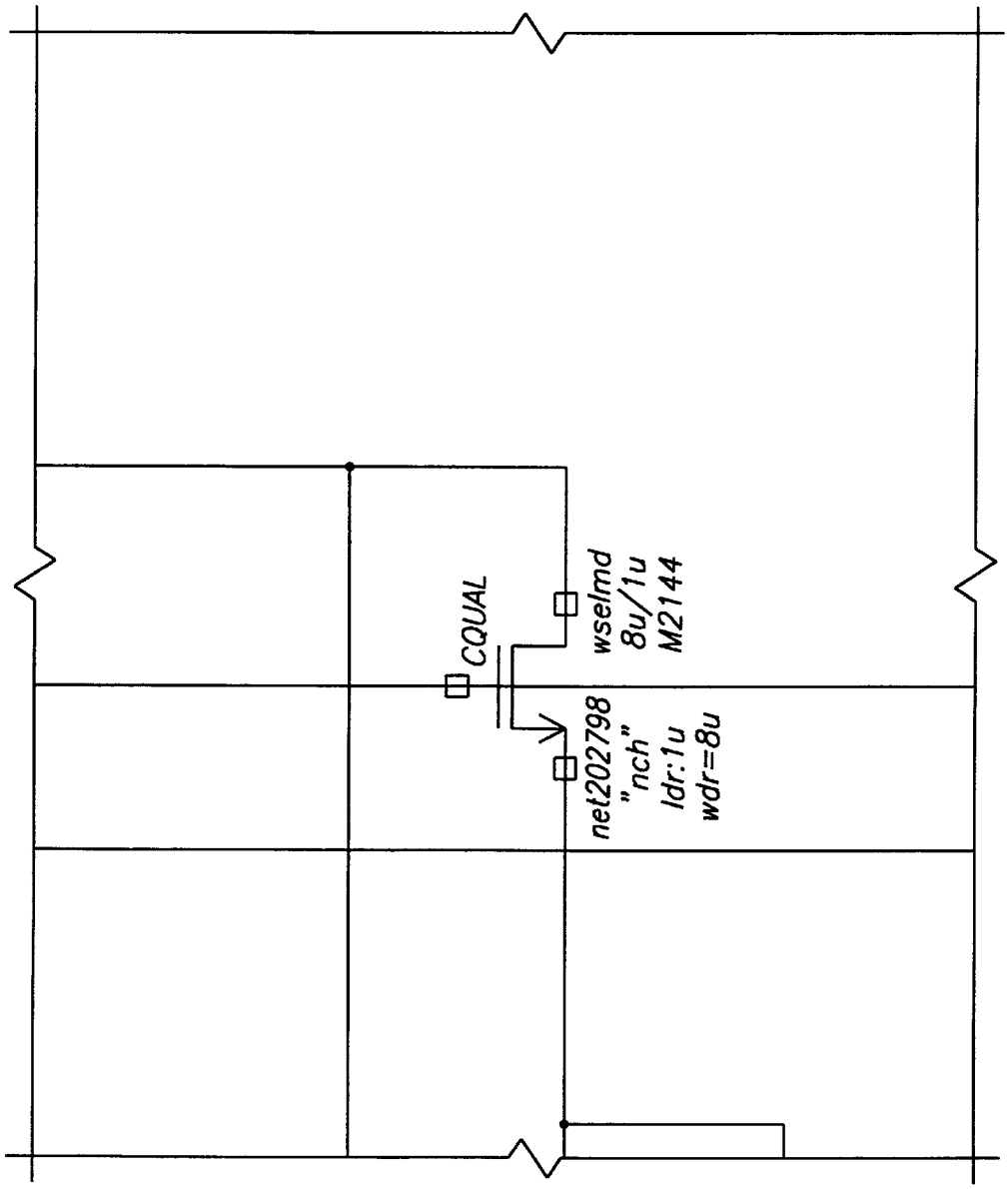


FIG 1,060,4FE

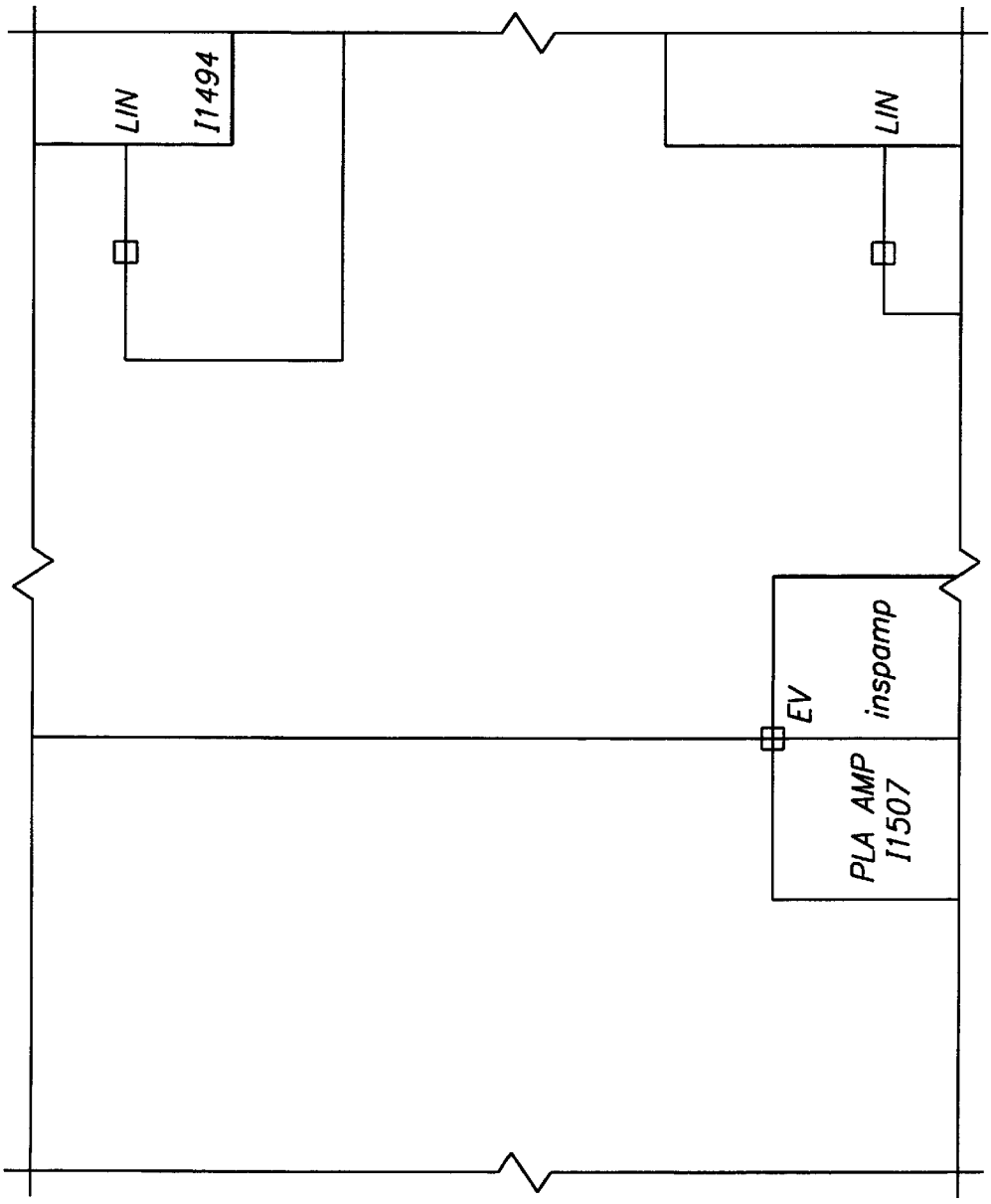


FIG 7.0604FF

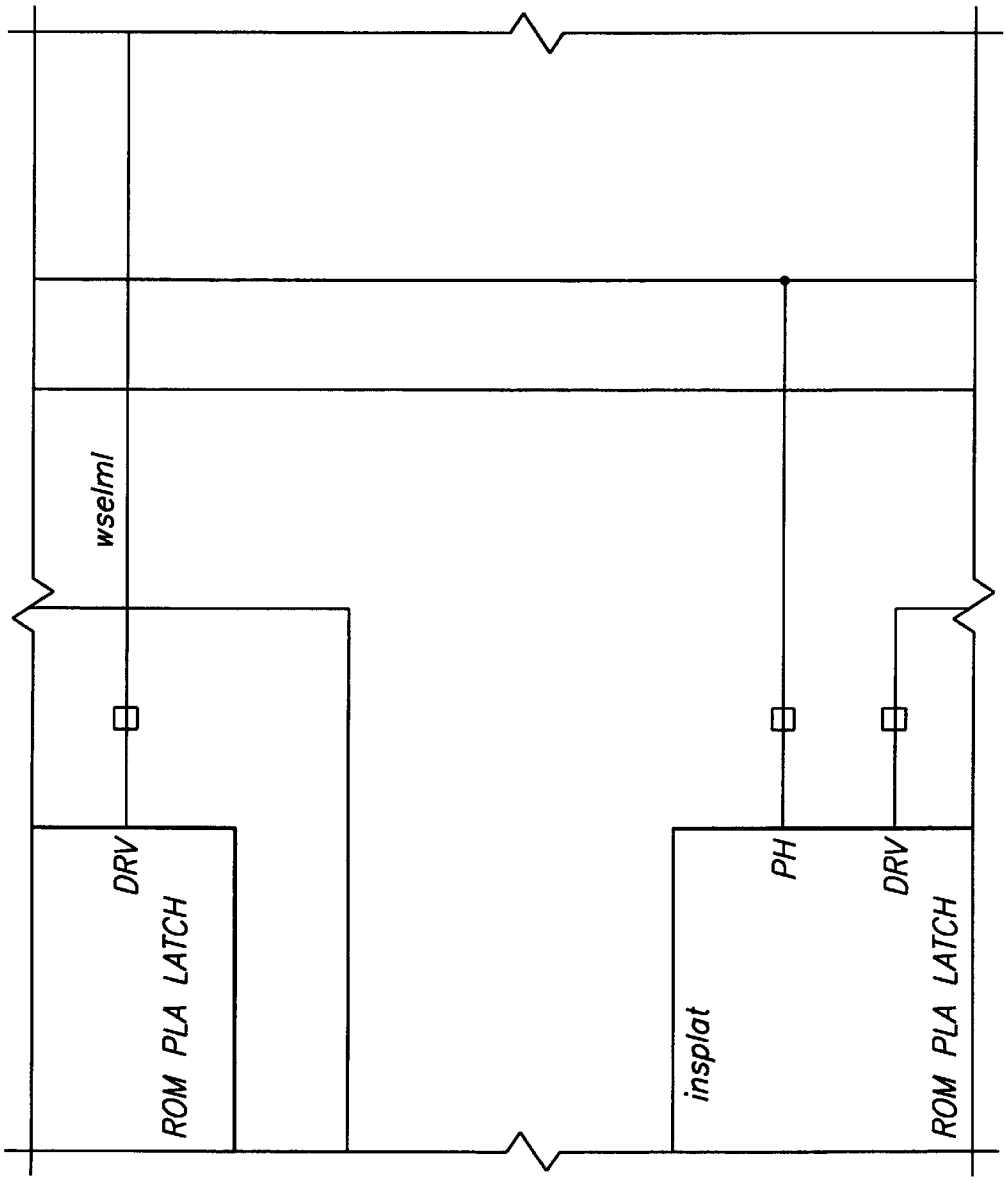


FIG 1,050,F5

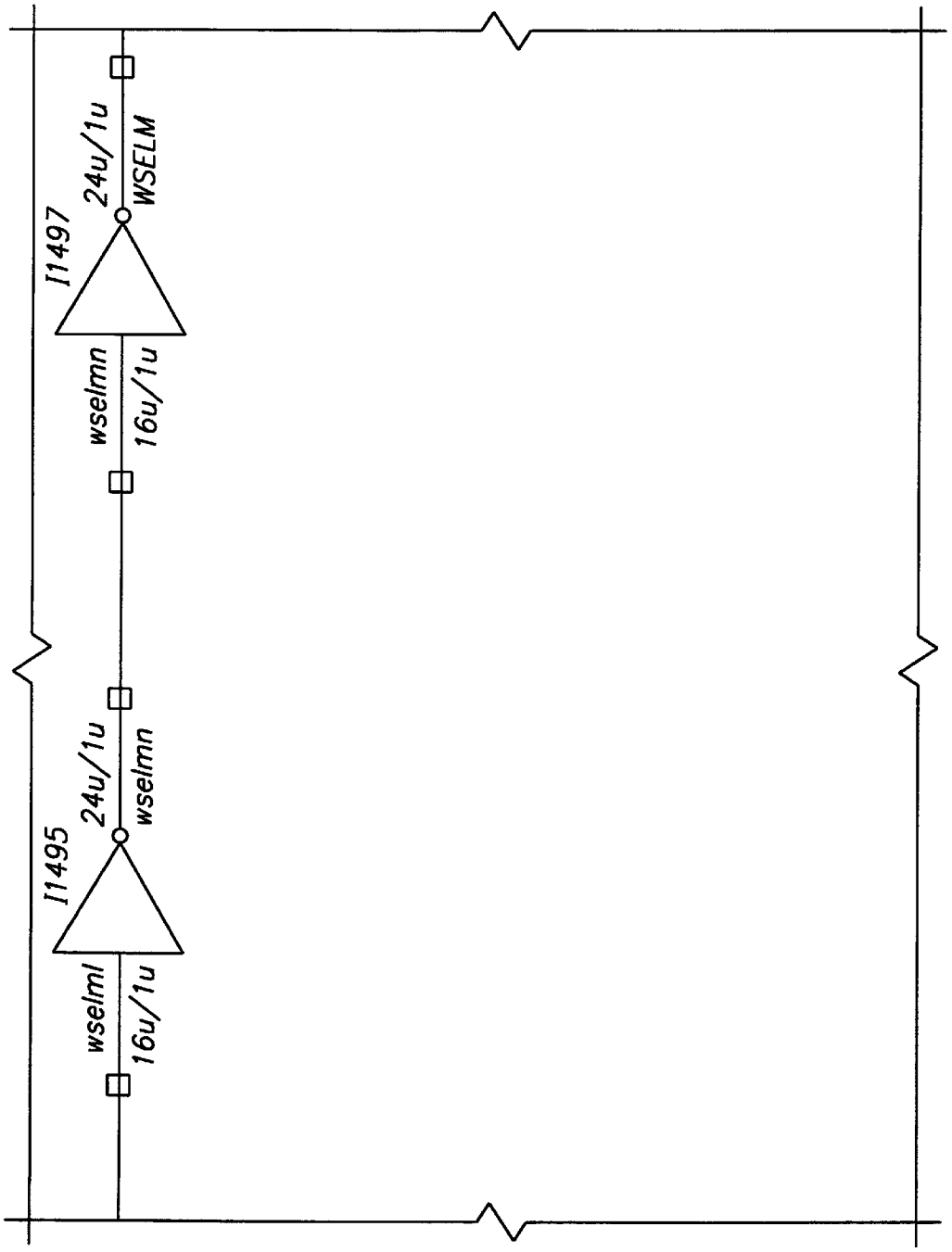
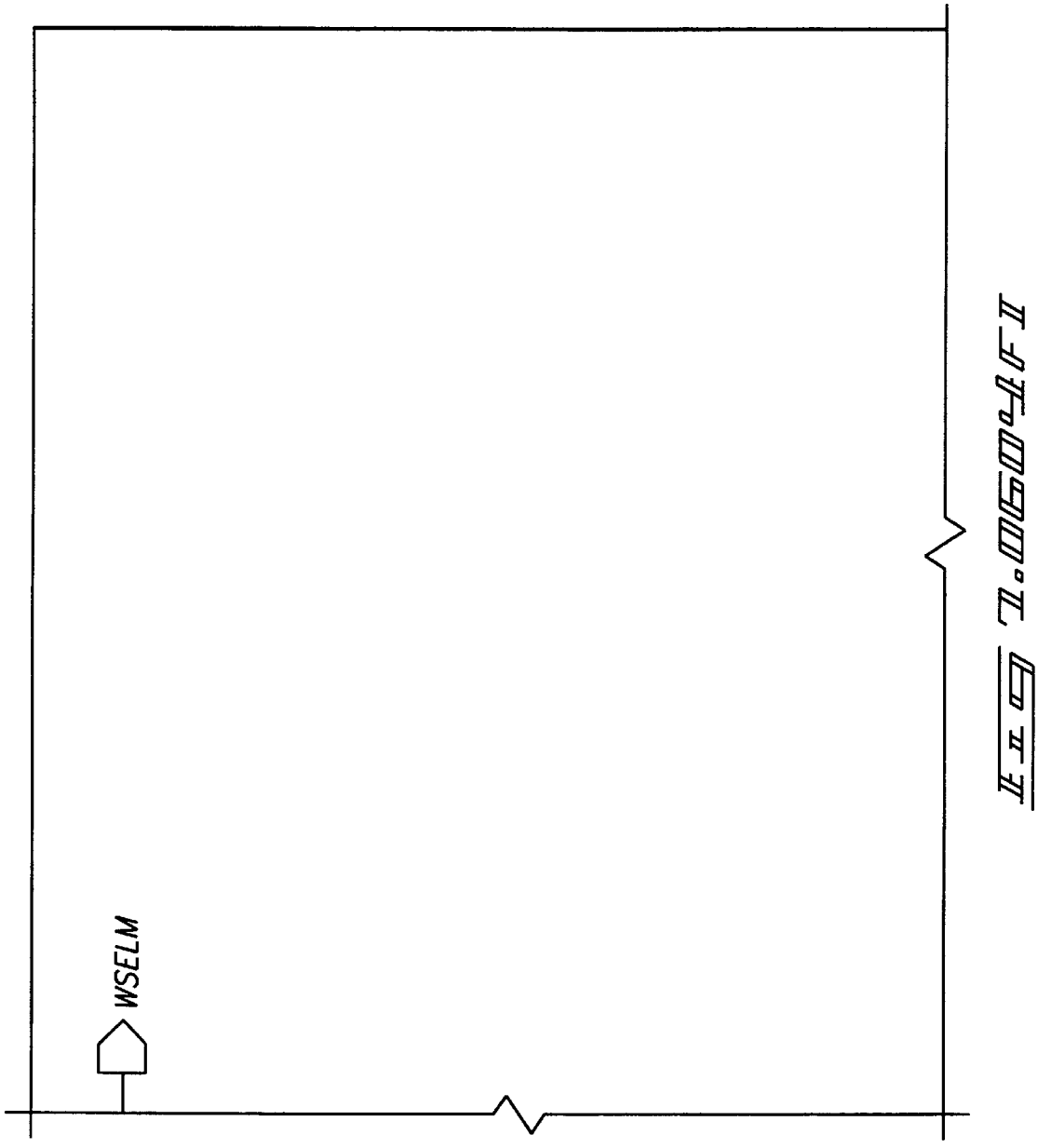


FIG. 1L 6,130,602


WSELM
FIG. 1,050,474

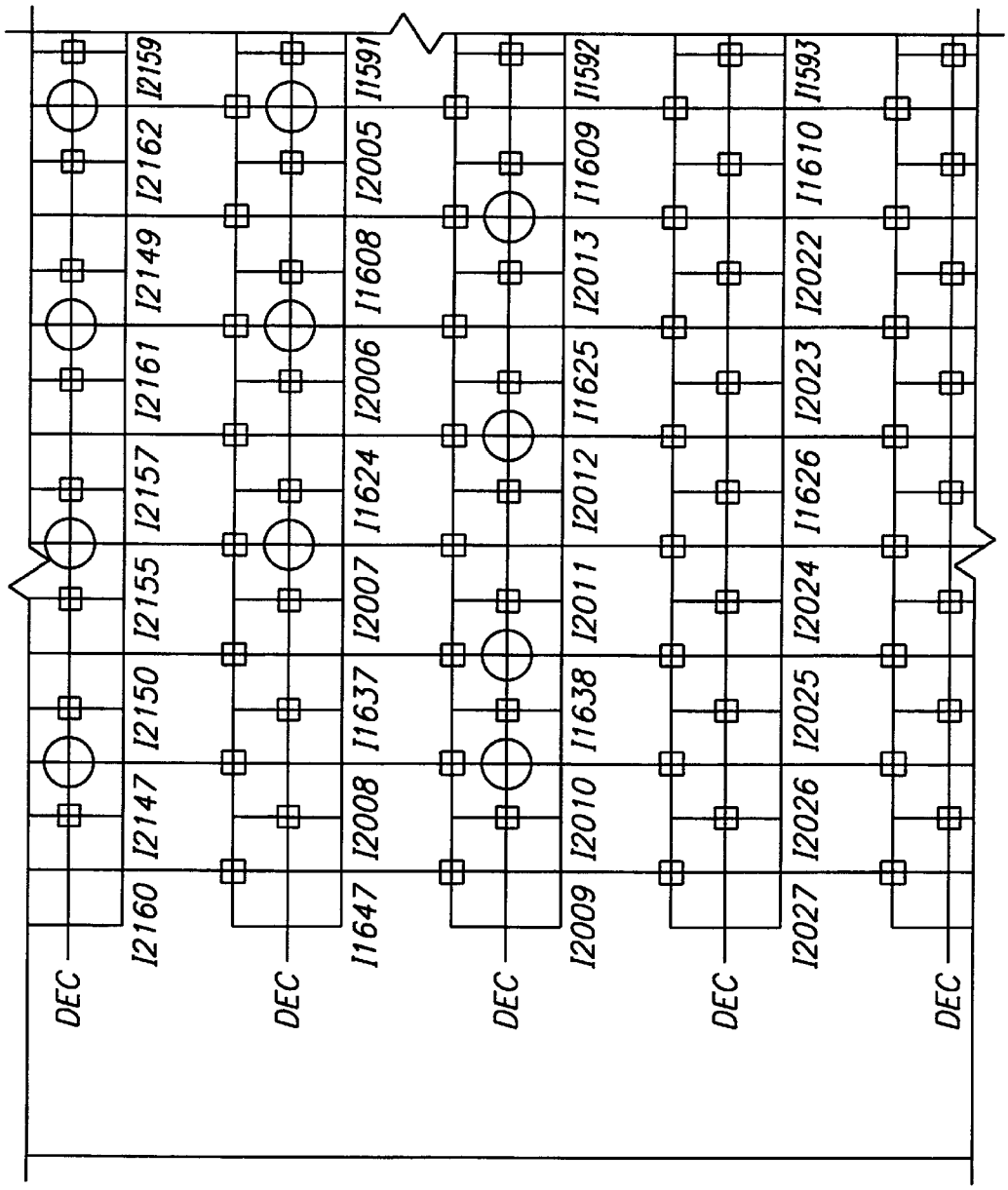

DEC
I2160
I2147
I2150
I2155
I2157
I2161
I2149
I2162
I2159
DEC
I1647
I2008
I1637
I2007
I1624
I2006
I1608
I2005
I1591
DEC
I2009
I2010
I1638
I2011
I2012
I1625
I2013
I1609
I1592
DEC
I2027
I2026
I2025
I2024
I1626
I2023
I2022
I1610
I1593
DEC

FIG 1.06047A

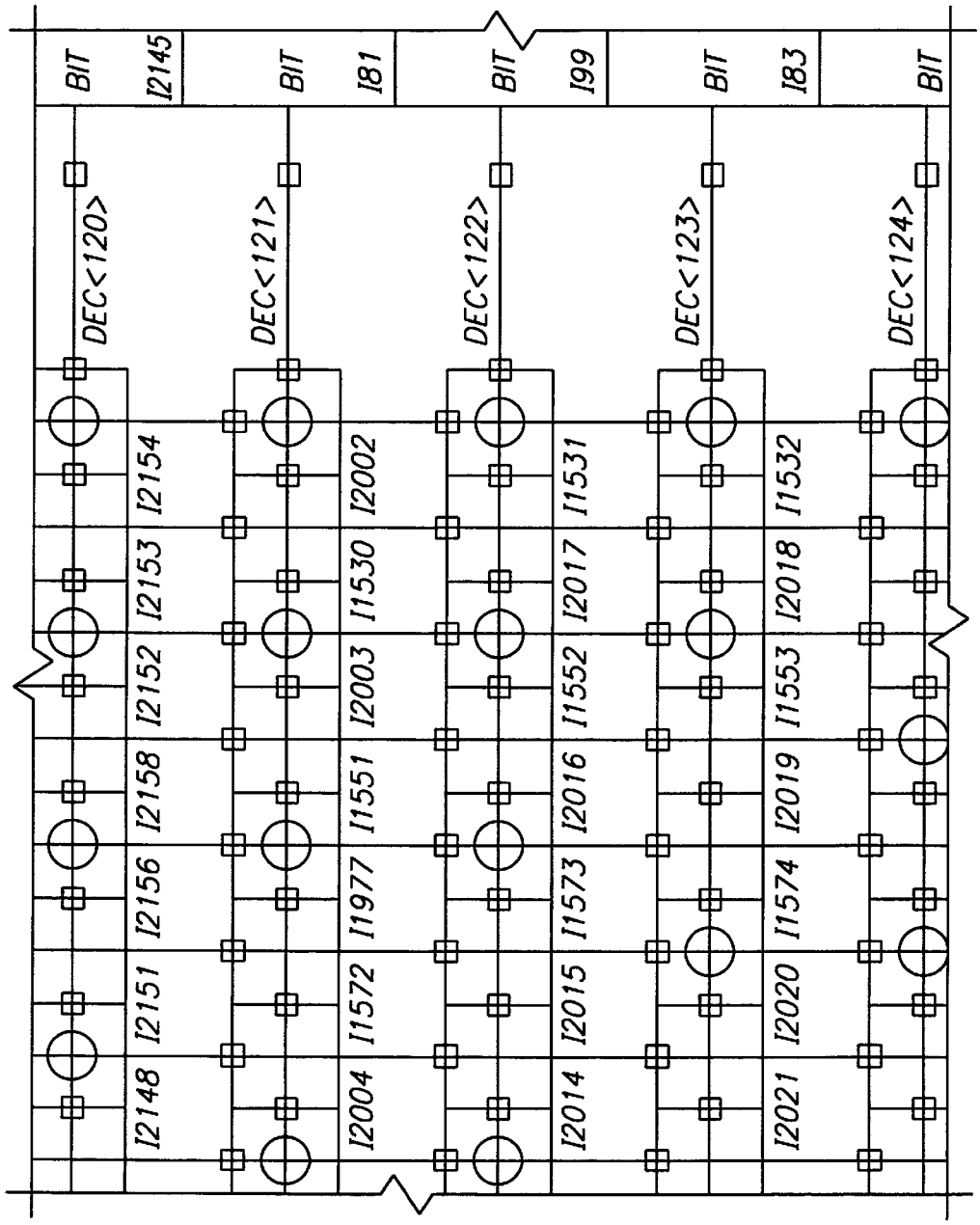

BIT
I2145
BIT
I81
BIT
I99
BIT
I83
BIT
DEC<120>
DEC<121>
DEC<122>
DEC<123>
DEC<124>
I2148
I2151
I2156
I2158
I2152
I2153
I2154
I2004
I1572
I1977
I1551
I2003
I1530
I2002
I2014
I2015
I1573
I2016
I1552
I2017
I1531
I2021
I2020
I1574
I2019
I1553
I2018
I1532

Fig. 1,605,744

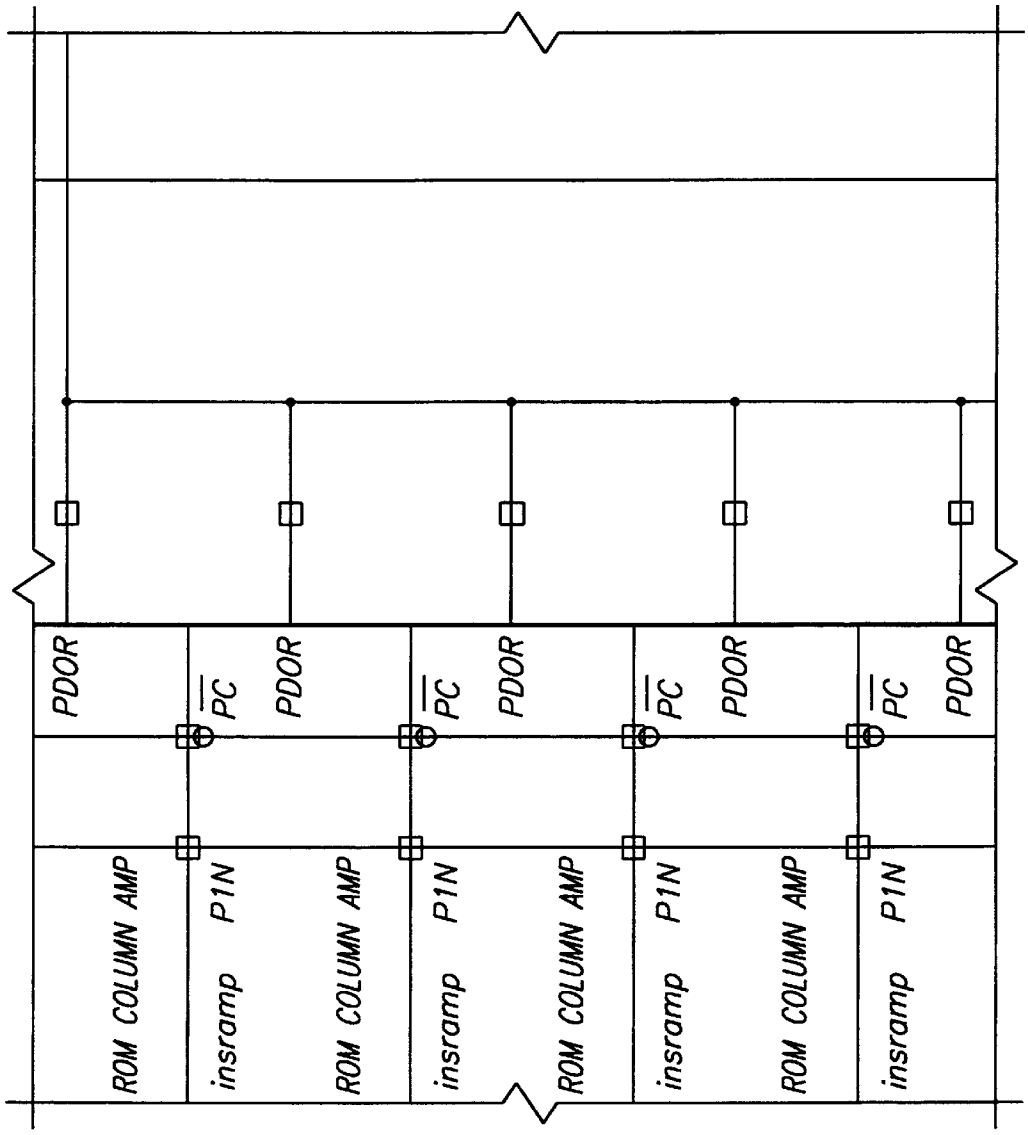

PDOR
PC
PDOR
PC
PDOR
PC
PDOR
PC
PDOR
ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
insramp P1N

FIG. 793

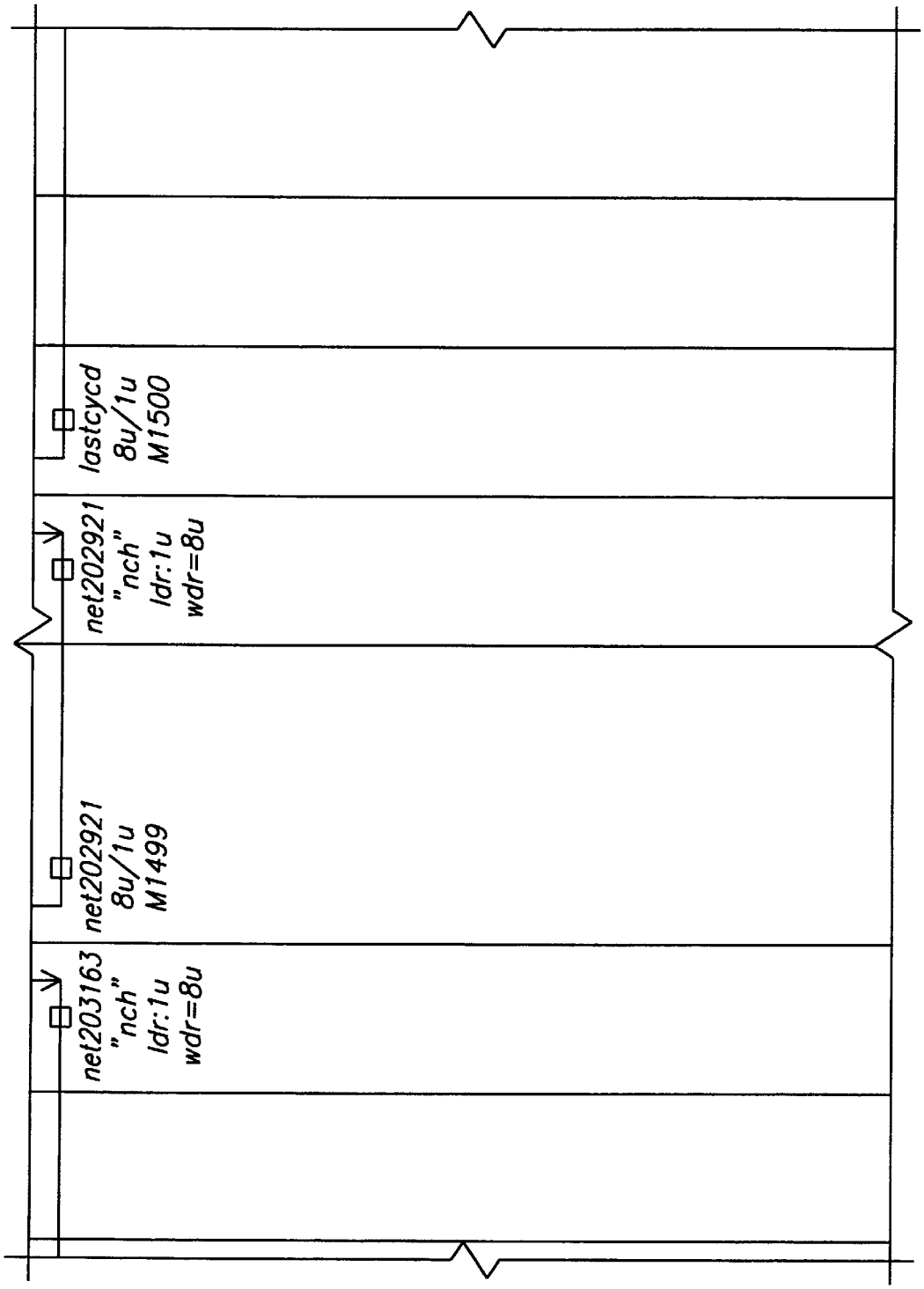

net203163
"nch"
ldr:1u
wdr=8u
net202921
8u/1u
M1499
net202921
"nch"
ldr:1u
wdr=8u
lastcycd
8u/1u
M1500

FIG 1,059,459

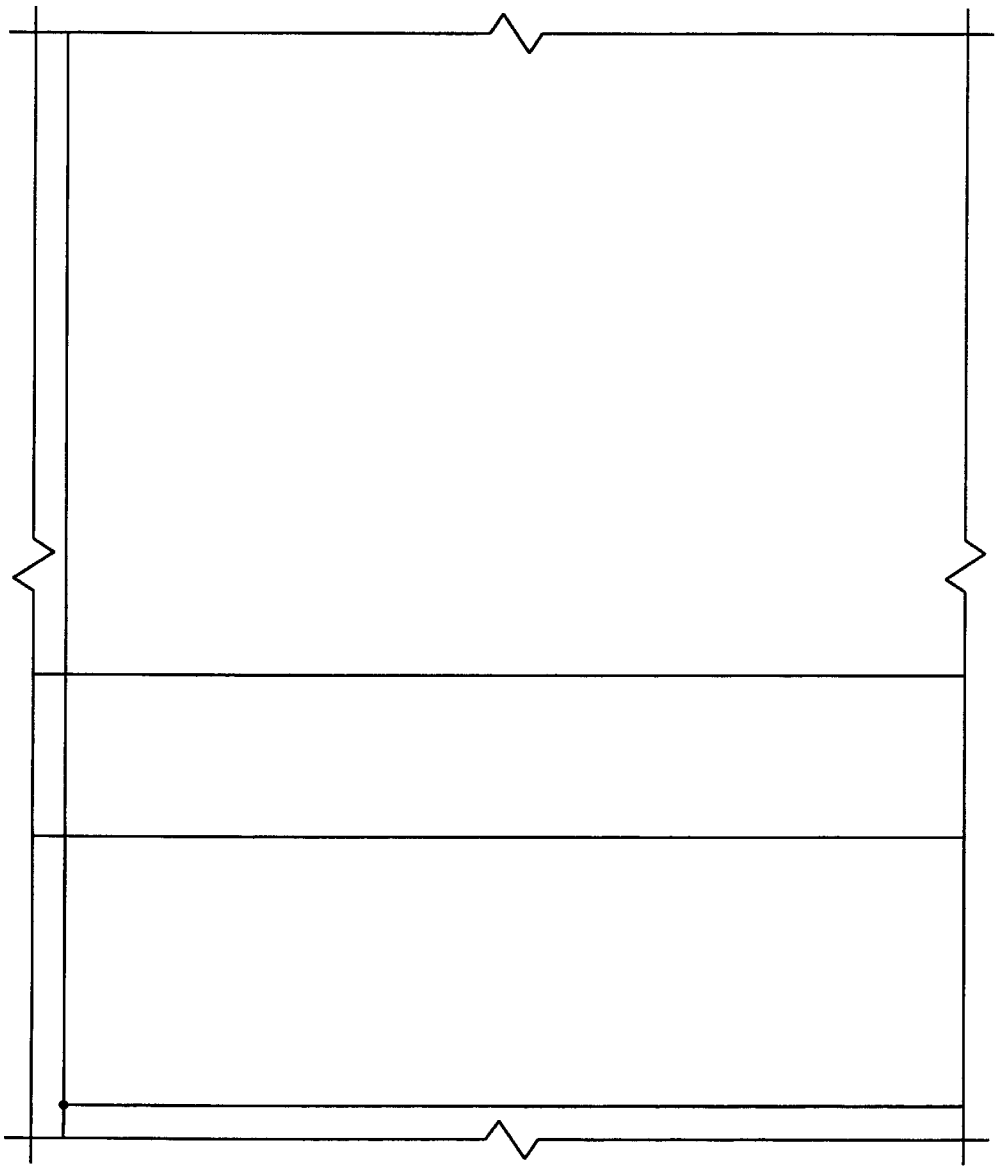


FIG. 795A

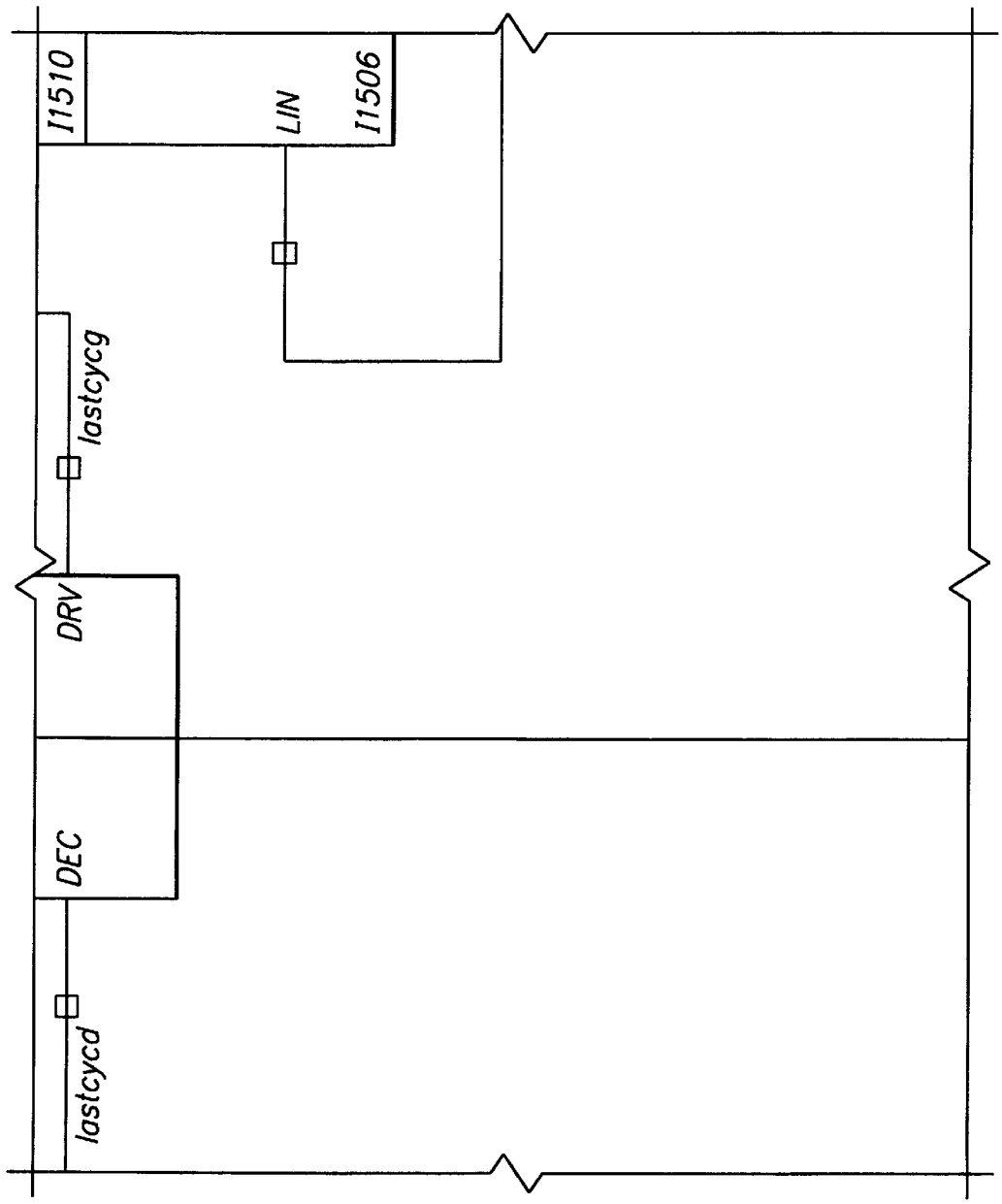


FIG. 1L,1M,1N,1O,1P

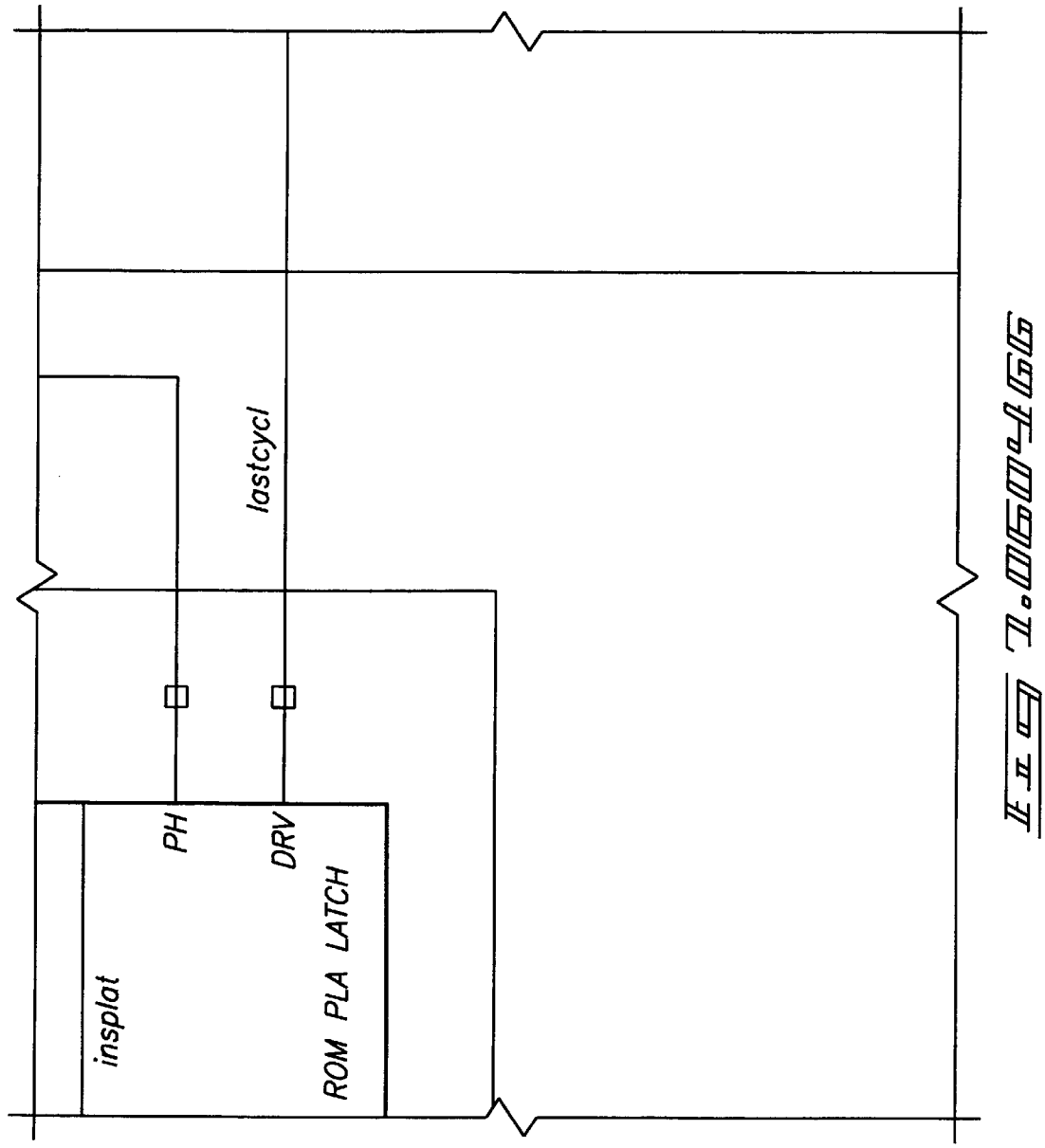


FIG 59F

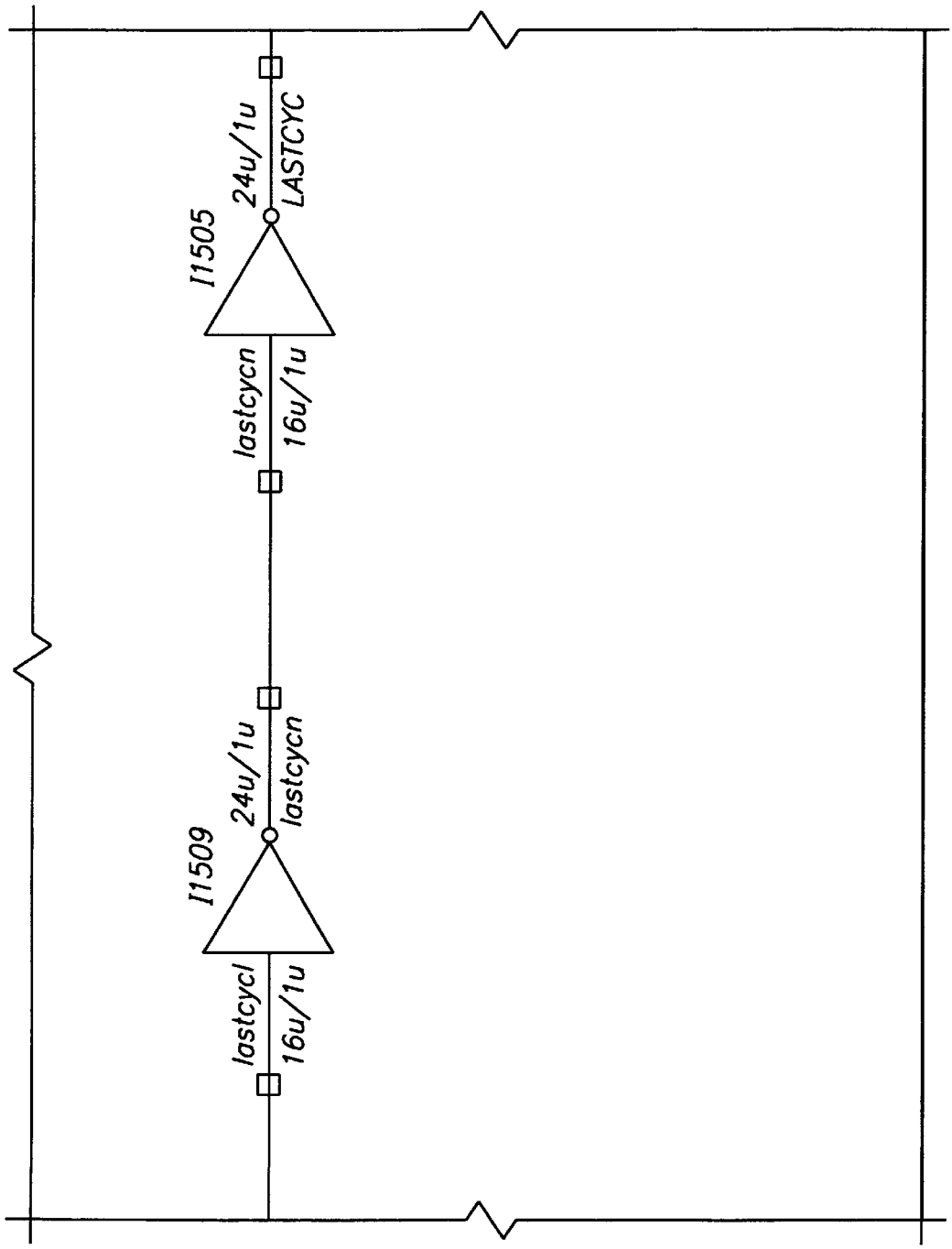


FIG 798 of 3273

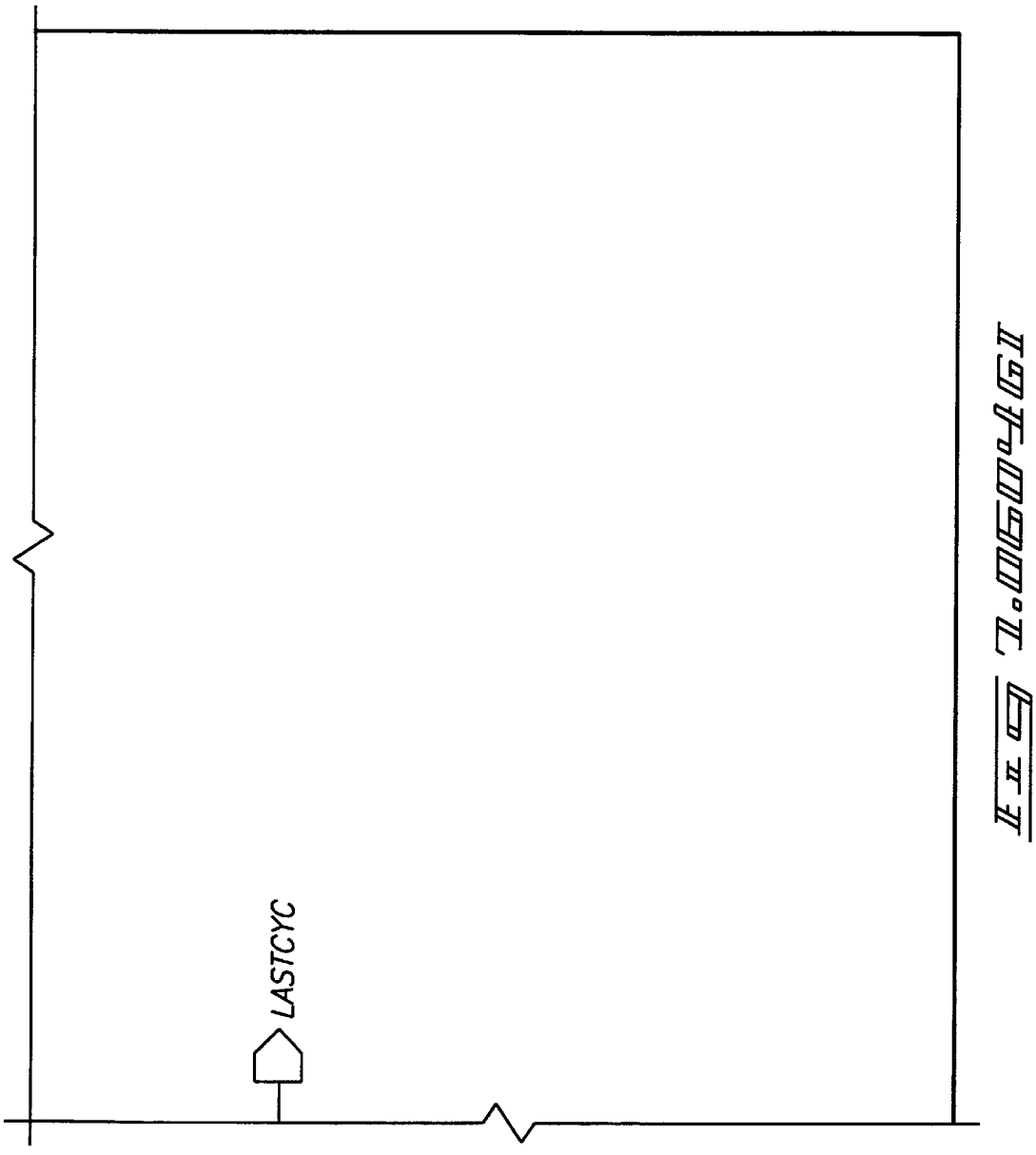


FIG. 11,059
LASTCYC

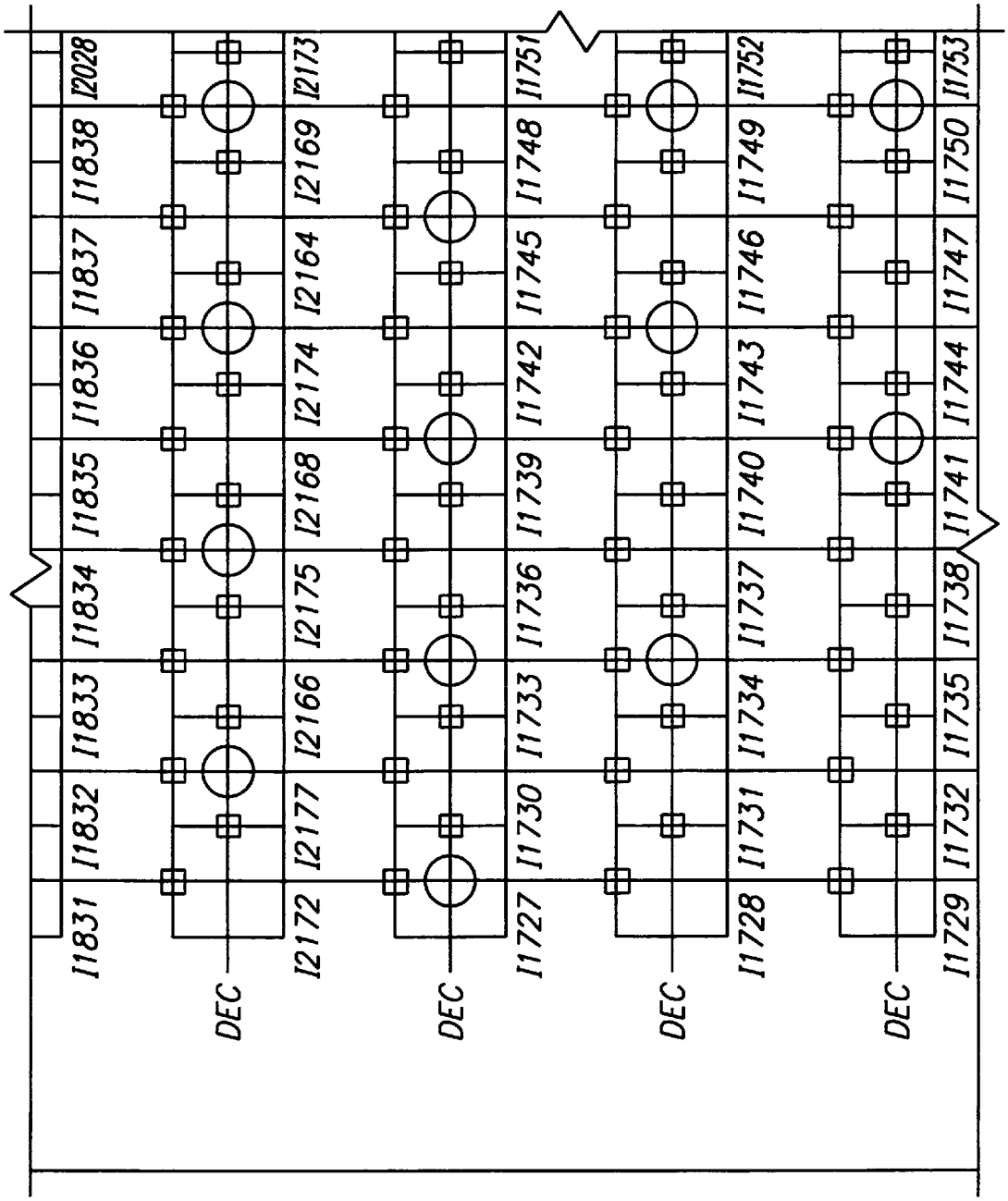
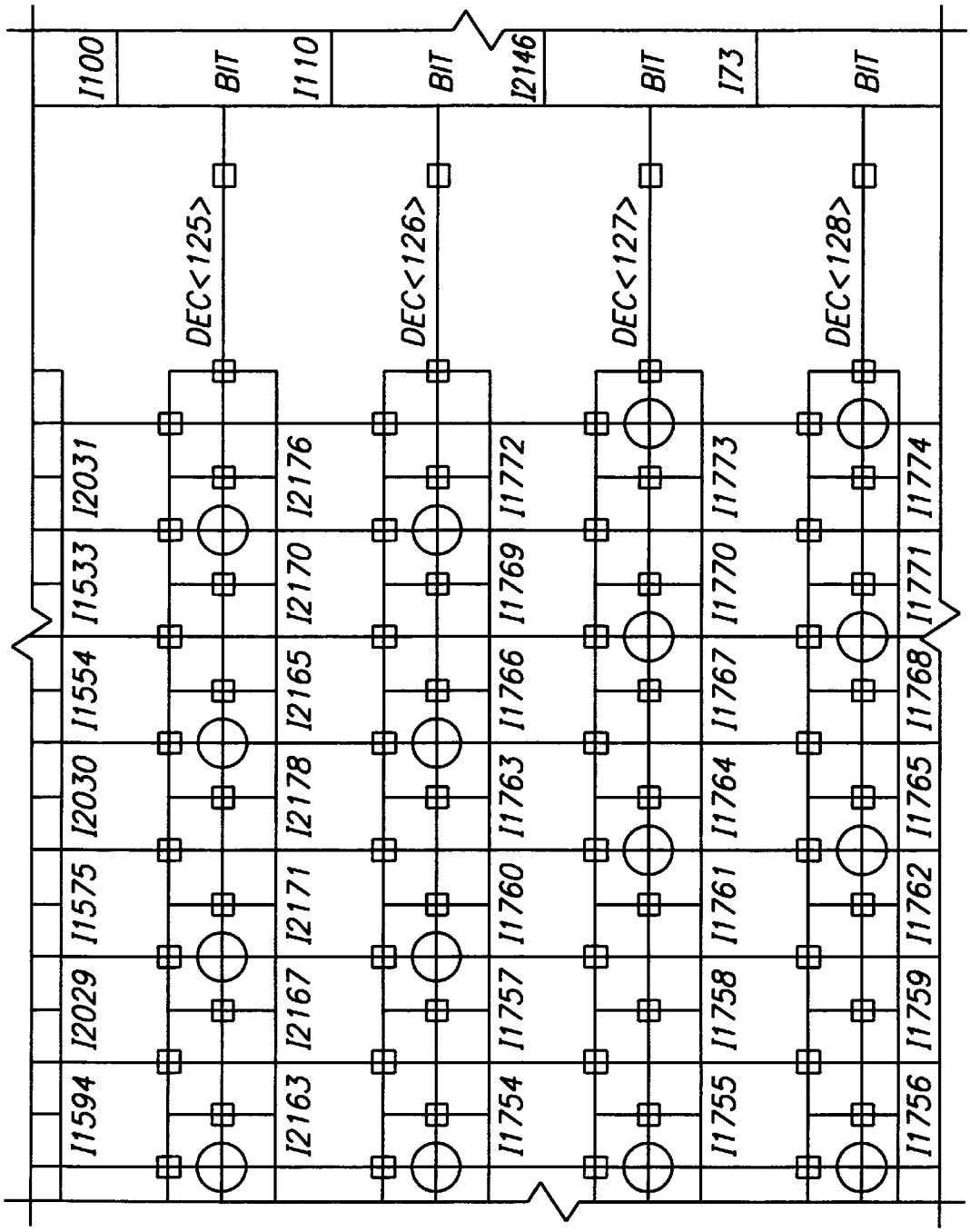

I1831
I1832
I1833
I1834
I1835
I1836
I1837
I1838
I2028
I2172
I2177
I2166
I2175
I2168
I2174
I2164
I2169
I2173
I1727
I1730
I1733
I1736
I1739
I1742
I1745
I1748
I1751
I1728
I1731
I1734
I1737
I1740
I1743
I1746
I1749
I1752
I1729
I1732
I1735
I1738
I1741
I1744
I1747
I1750
I1753
DEC
DEC
DEC
DEC

FIG. 1100


I1100
BIT
I1110
BIT
I2146
BIT
I73
BIT
DEC<125>
DEC<126>
DEC<127>
DEC<128>
I2031
I1533
I1554
I2030
I1575
I2029
I1594
I2176
I2170
I2165
I2178
I2171
I2167
I2163
I1772
I1769
I1766
I1763
I1760
I1757
I1754
I1773
I1770
I1767
I1764
I1761
I1758
I1755
I1774
I1771
I1768
I1765
I1762
I1759
I1756

ФИГ. 1100

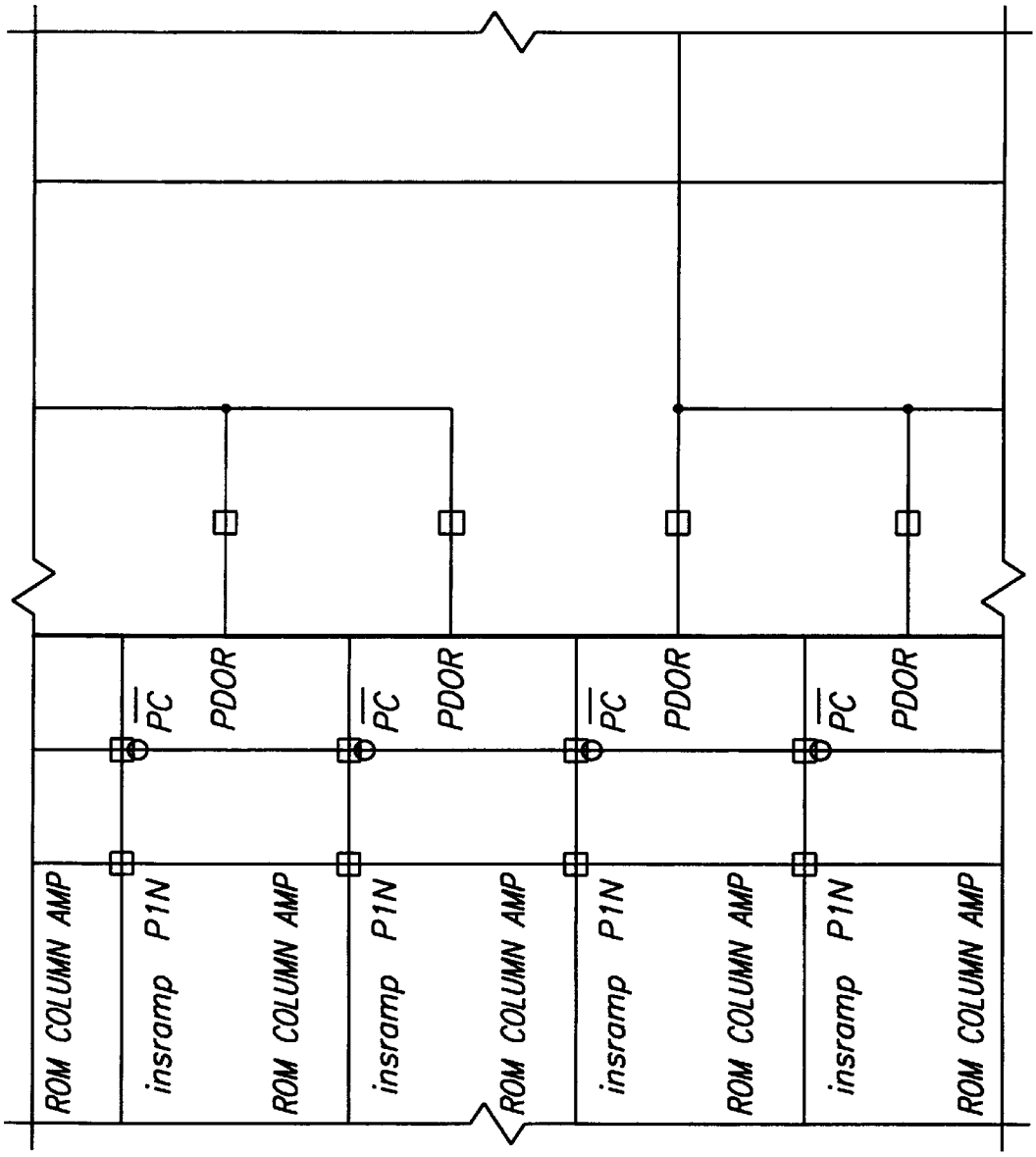

ROM COLUMN AMP
insramp P1N
ROM COLUMN AMP
PDOR
PC
PDOR
PC
PDOR
PC
PDOR
PC

FIG. 802

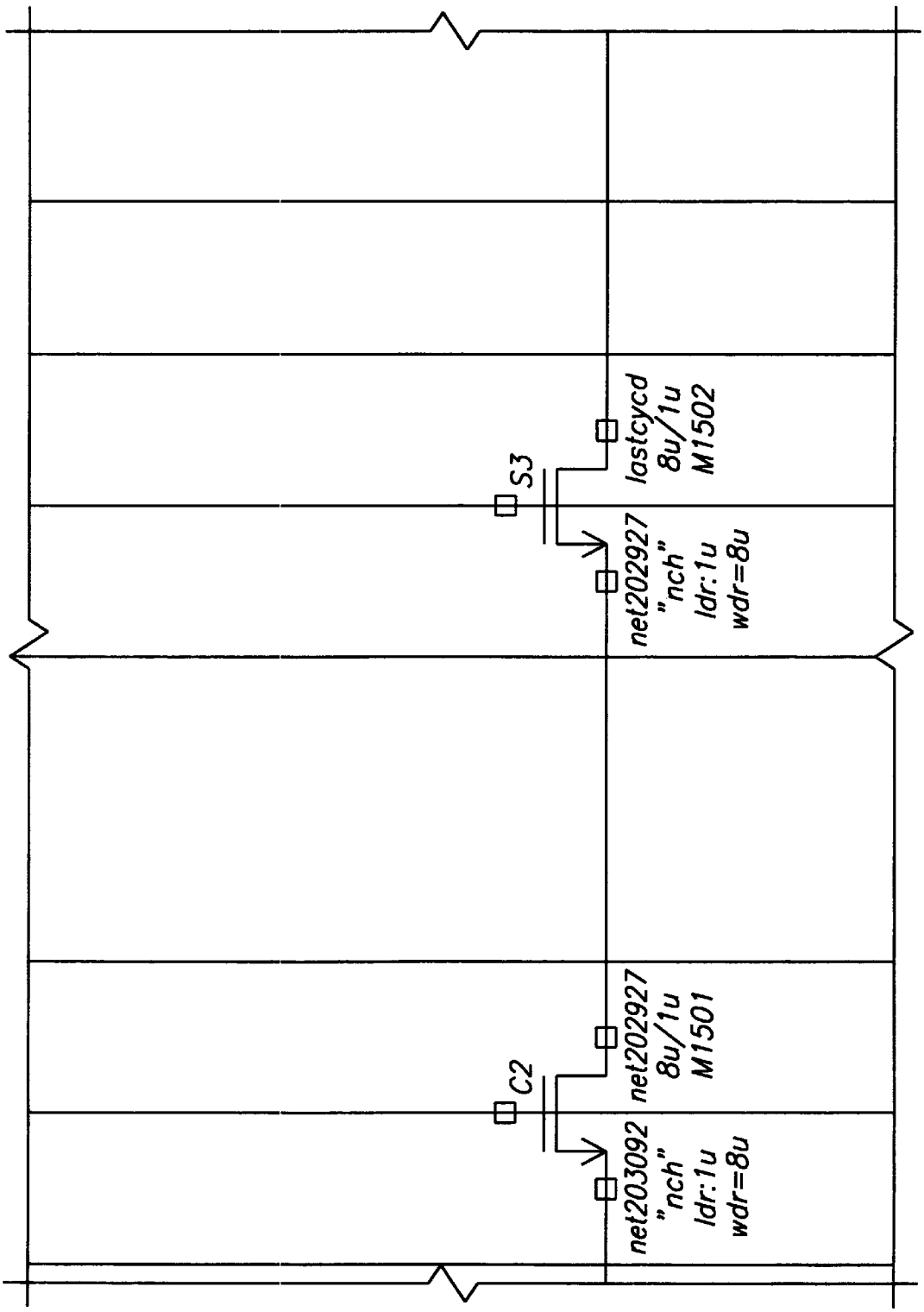

lastcycd
8u/1u
M1502
S3
net202927
"nch"
ldr:1u
wdr=8u
net202927
8u/1u
M1501
C2
net203092
"nch"
ldr:1u
wdr=8u

FIG 1.0500.1

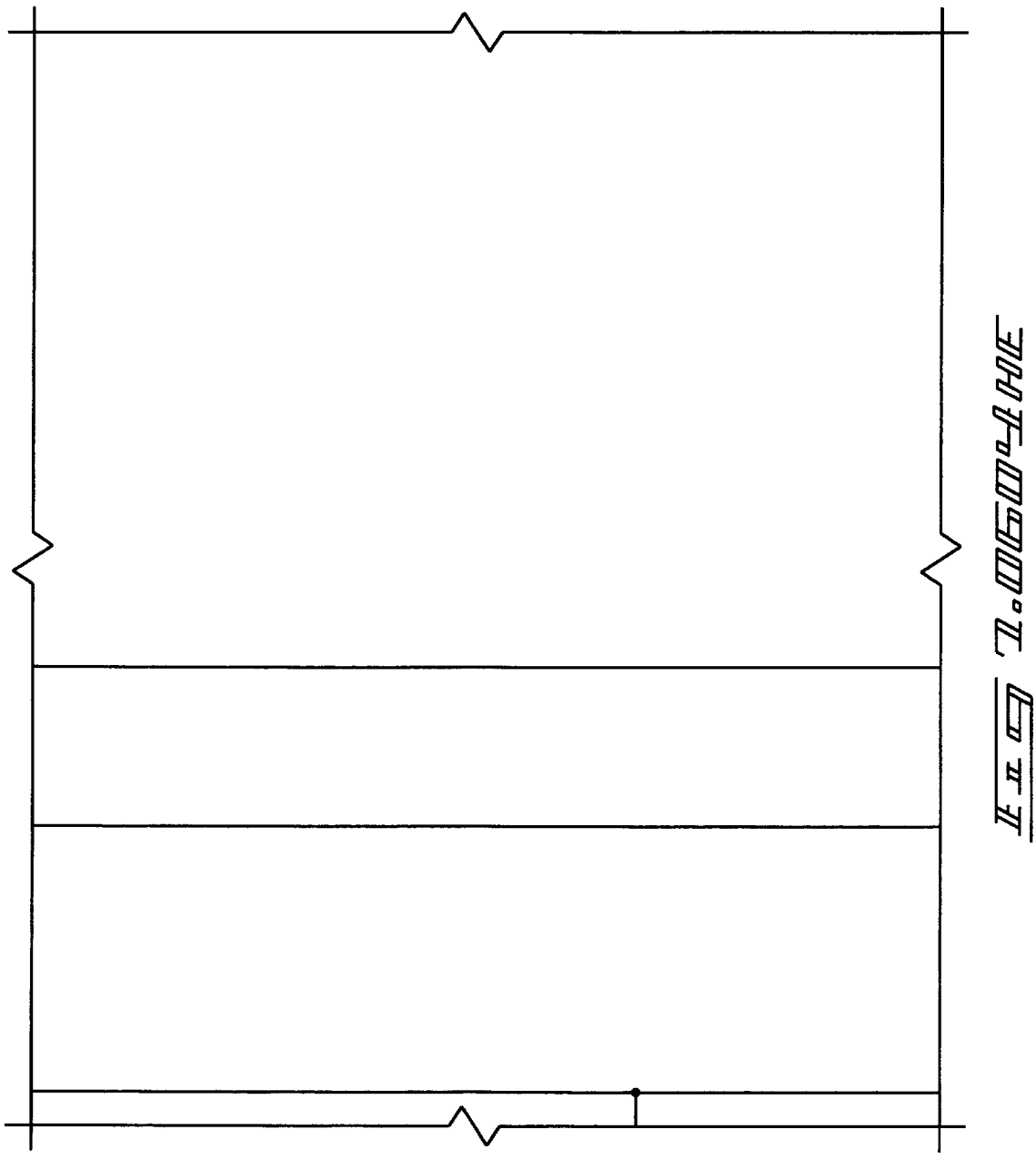


FIG. 1,050A

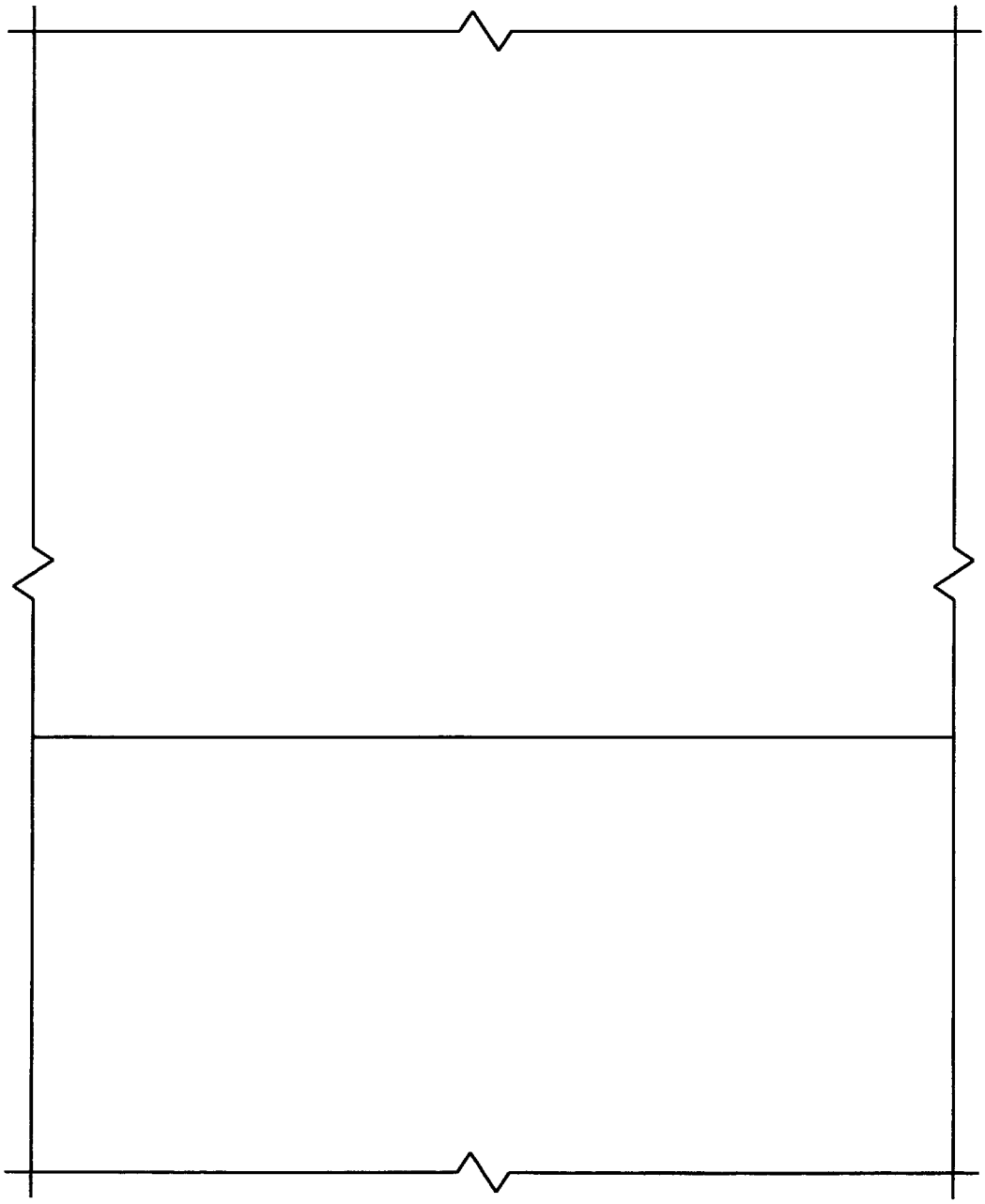
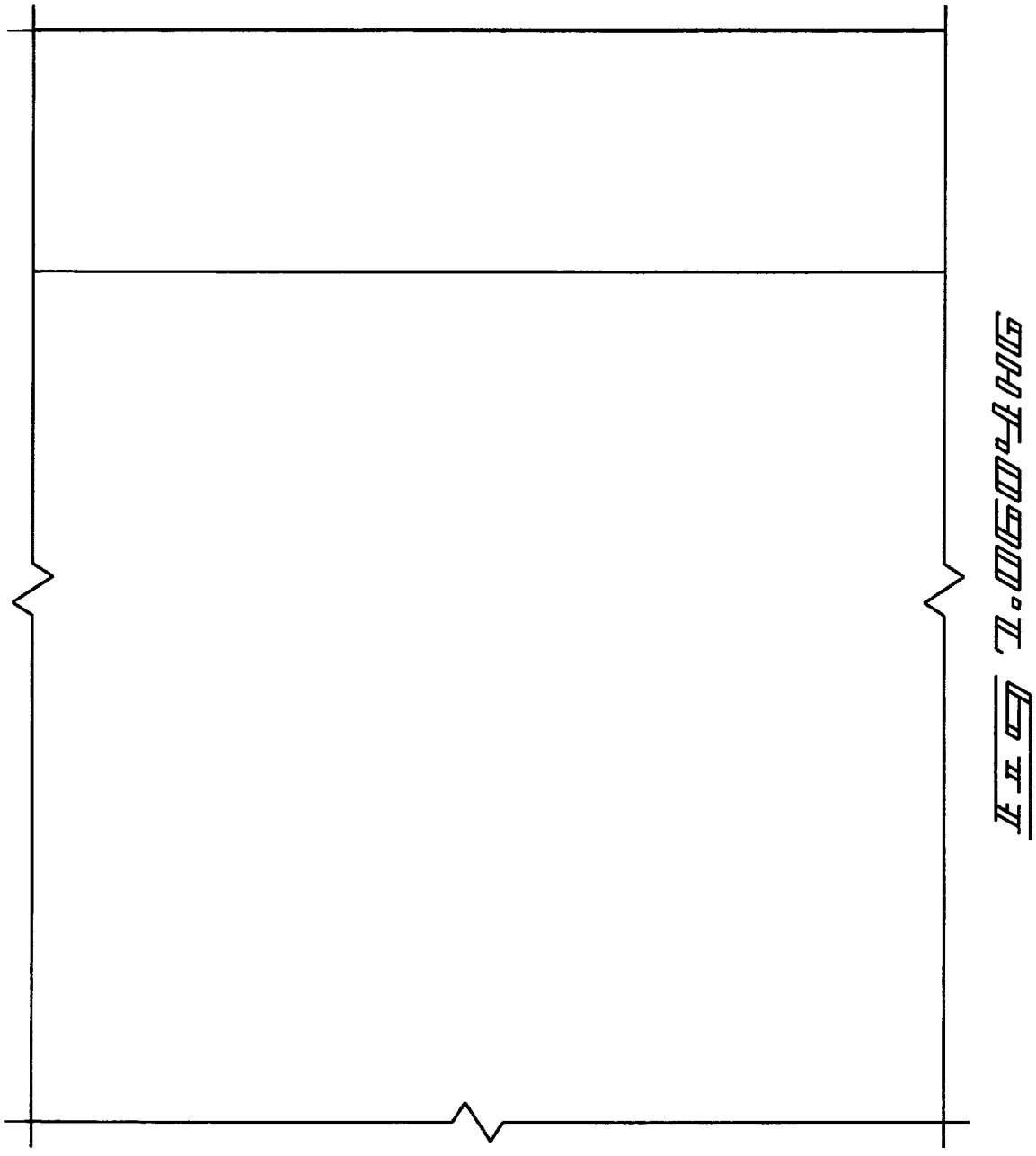


FIG. 1,090,478



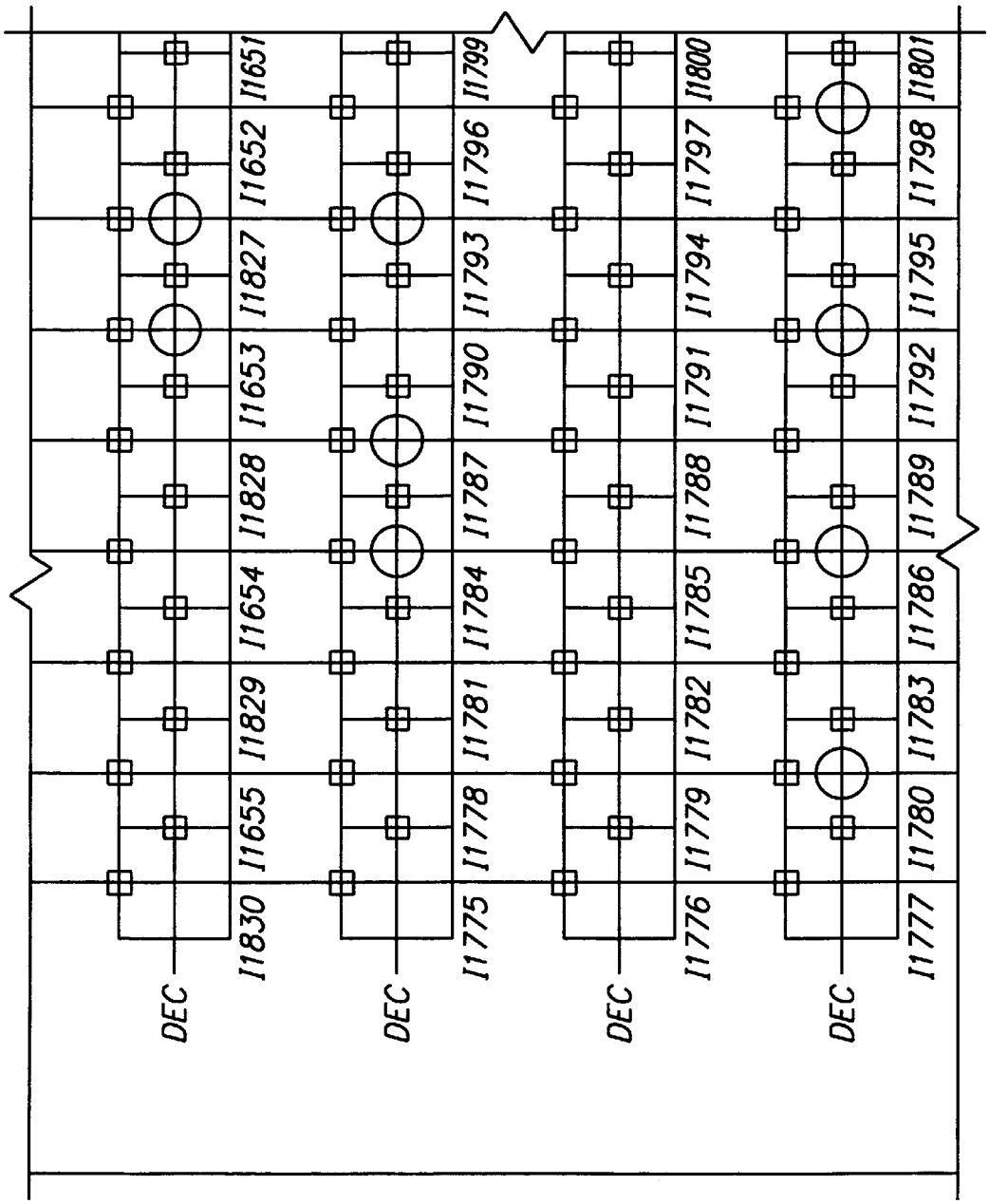

I1651
I1652
I1827
I1653
I1828
I1654
I1829
I1655
I1830
I1799
I1796
I1793
I1790
I1787
I1784
I1781
I1778
I1775
I1800
I1797
I1794
I1791
I1788
I1785
I1782
I1779
I1776
I1801
I1798
I1795
I1792
I1789
I1786
I1783
I1780
I1777
DEC
DEC
DEC
DEC

FIG. 11

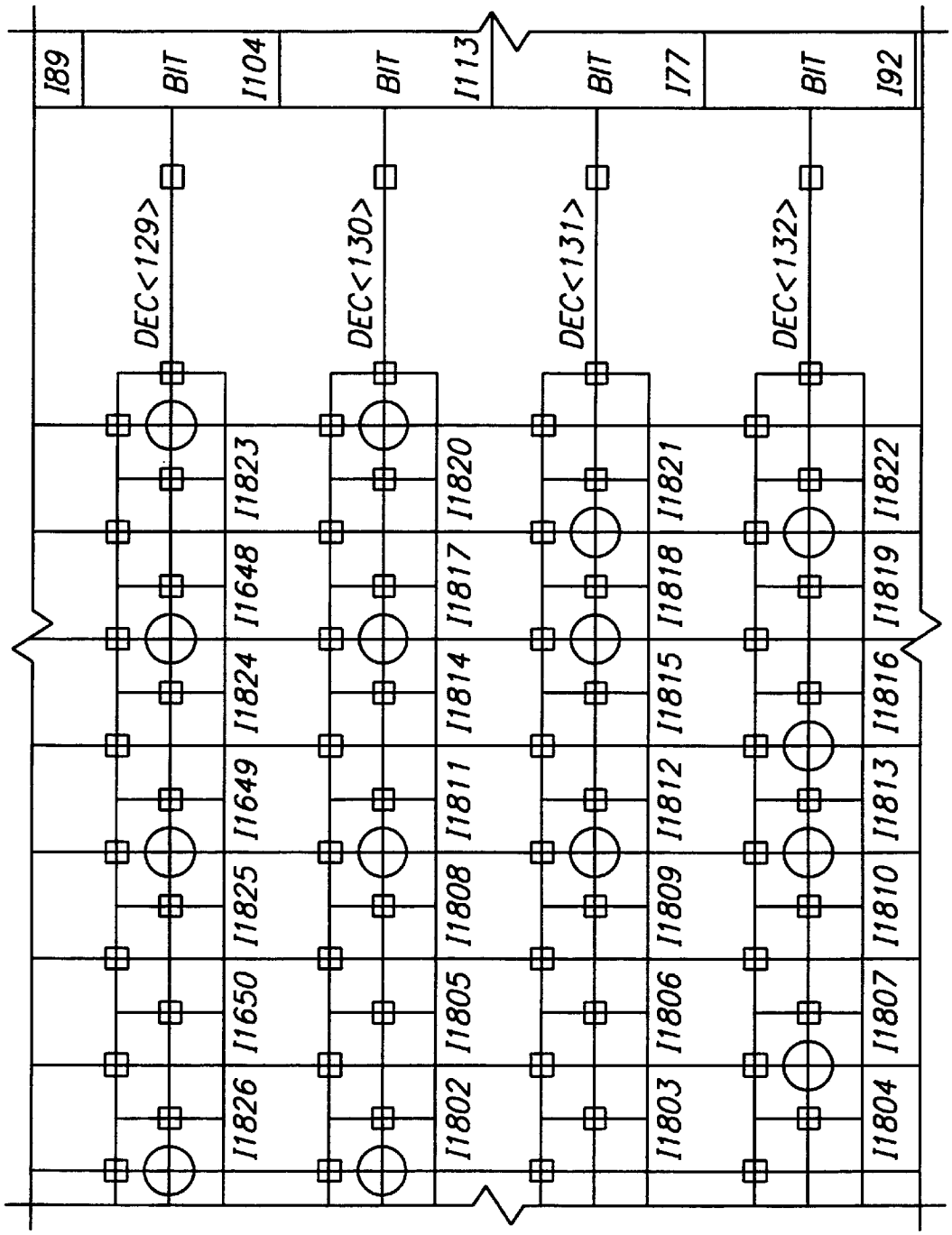

I89
BIT
I104
I113
I77
I92
DEC<129>
DEC<130>
DEC<131>
DEC<132>
I1823
I1648
I1824
I1649
I1825
I1650
I1826
I1820
I1817
I1814
I1811
I1808
I1805
I1802
I1821
I1818
I1815
I1812
I1809
I1806
I1803
I1822
I1819
I1816
I1813
I1810
I1807
I1804

FIG 6,050A

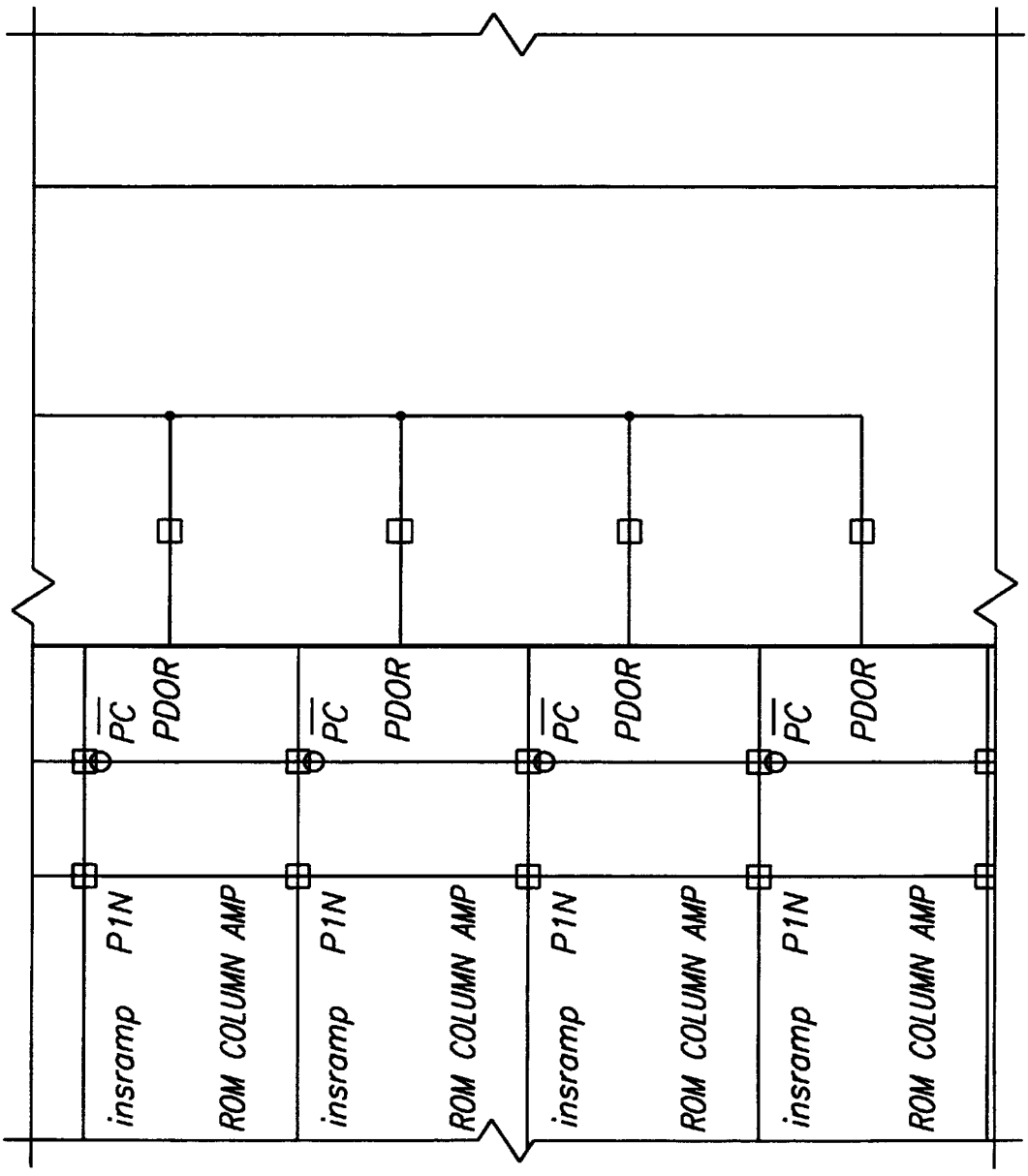


FIG 850.11

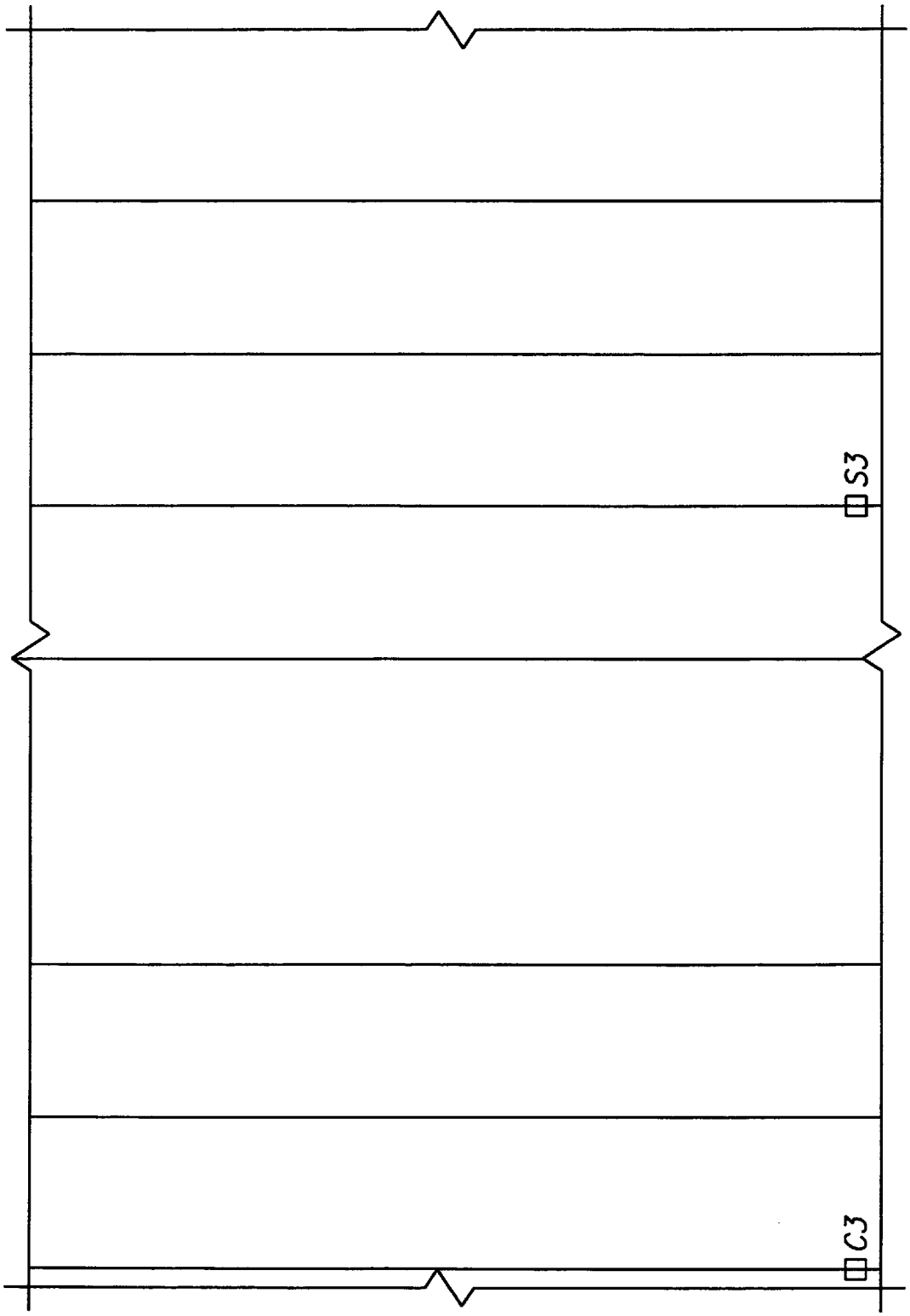


FIG 1.0504.11

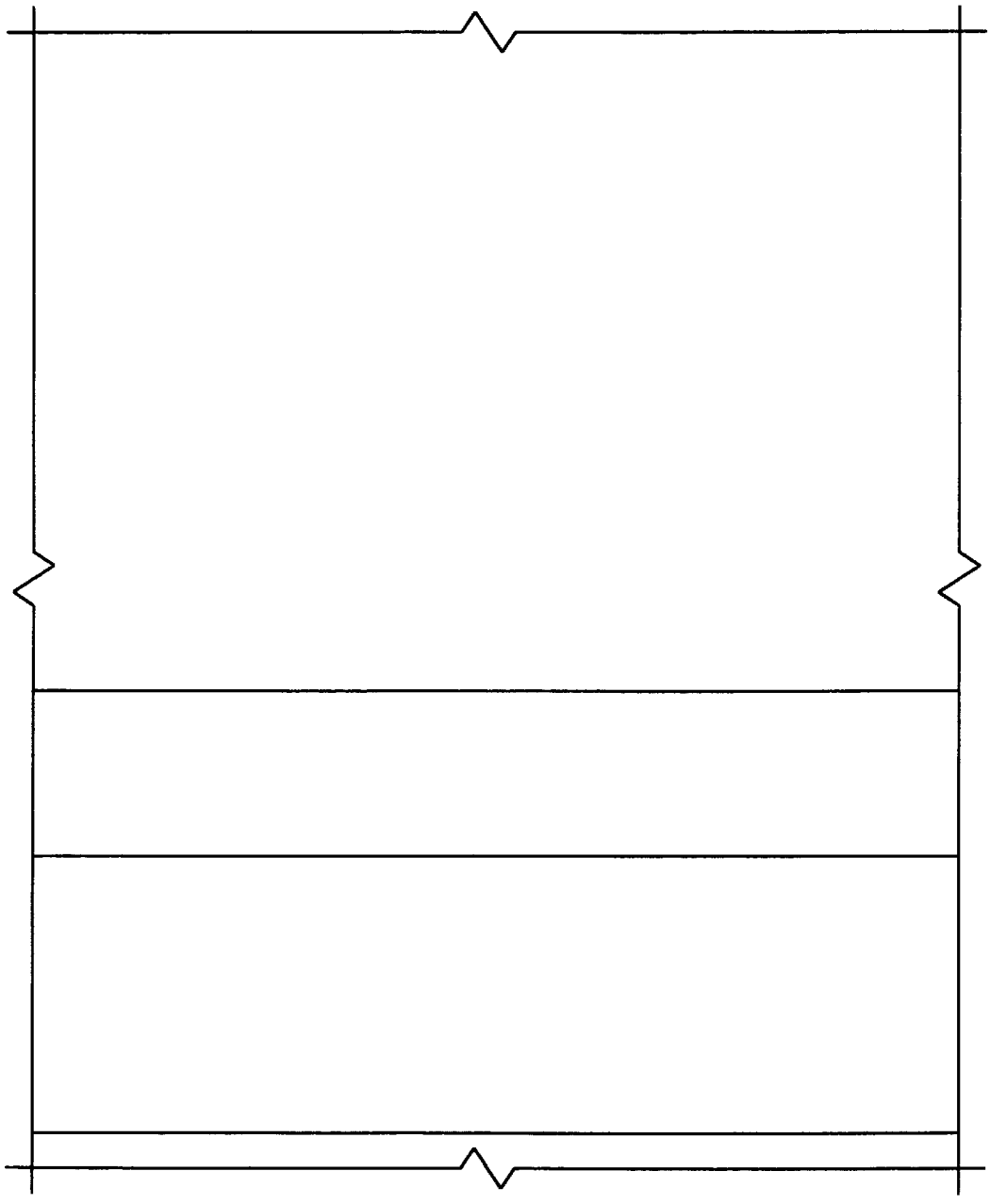


FIG. 700L

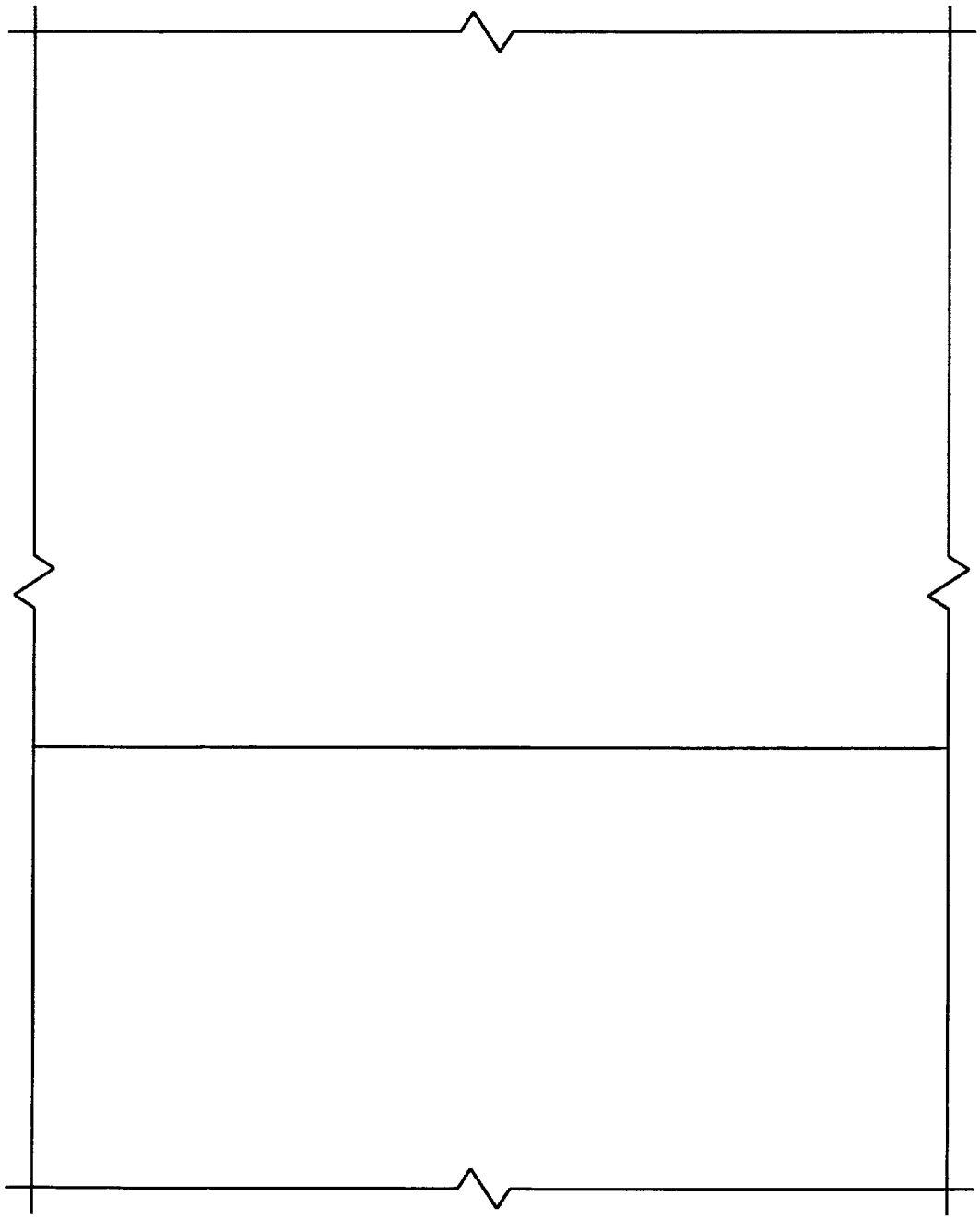
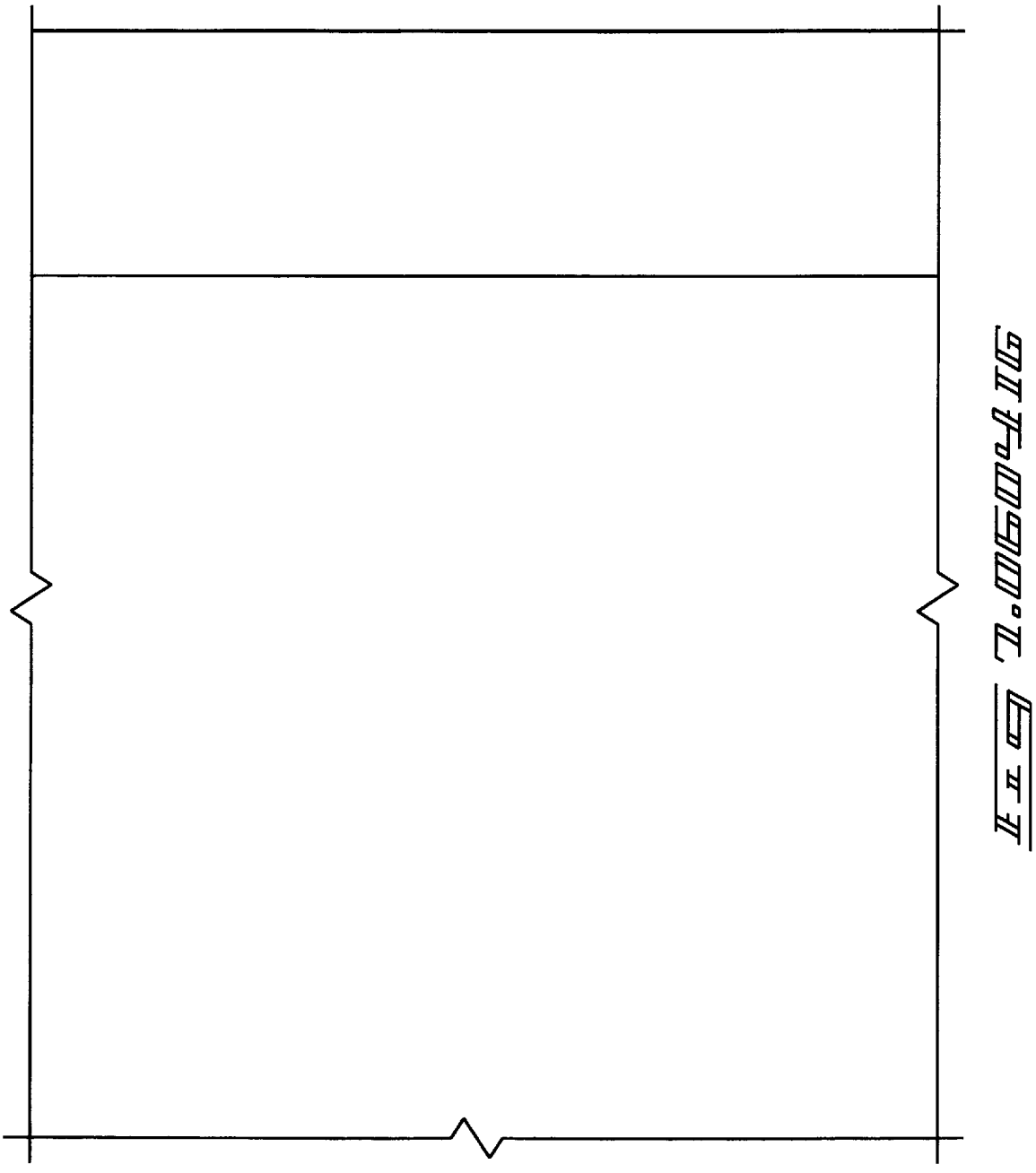


FIG. 71.0590


SIF0900.TIF

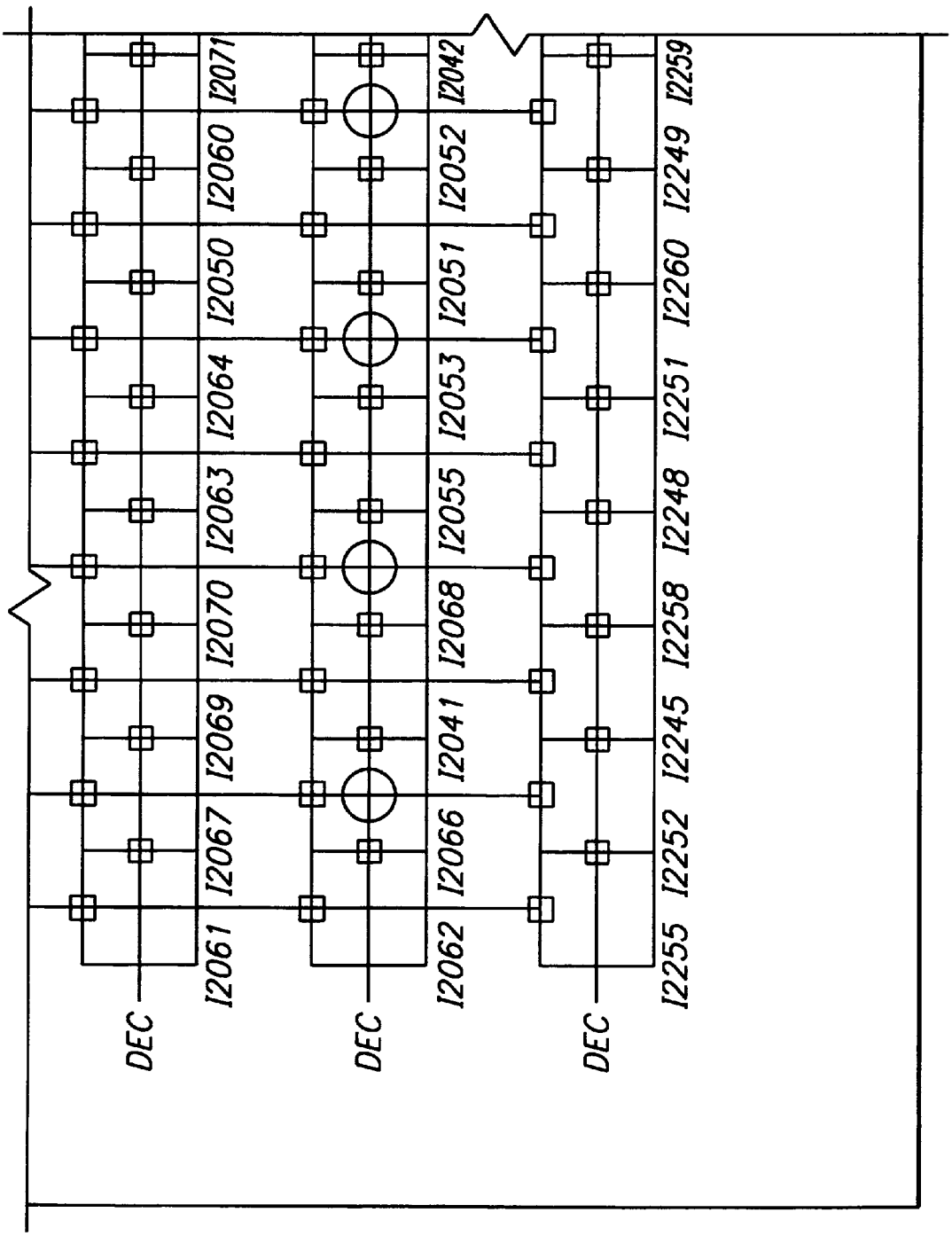

DEC
DEC
DEC
I2061
I2067
I2069
I2070
I2063
I2064
I2050
I2060
I2071
I2062
I2066
I2041
I2068
I2055
I2053
I2051
I2052
I2042
I2255
I2252
I2245
I2258
I2248
I2251
I2260
I2249
I2259

FIG. 6,090,611

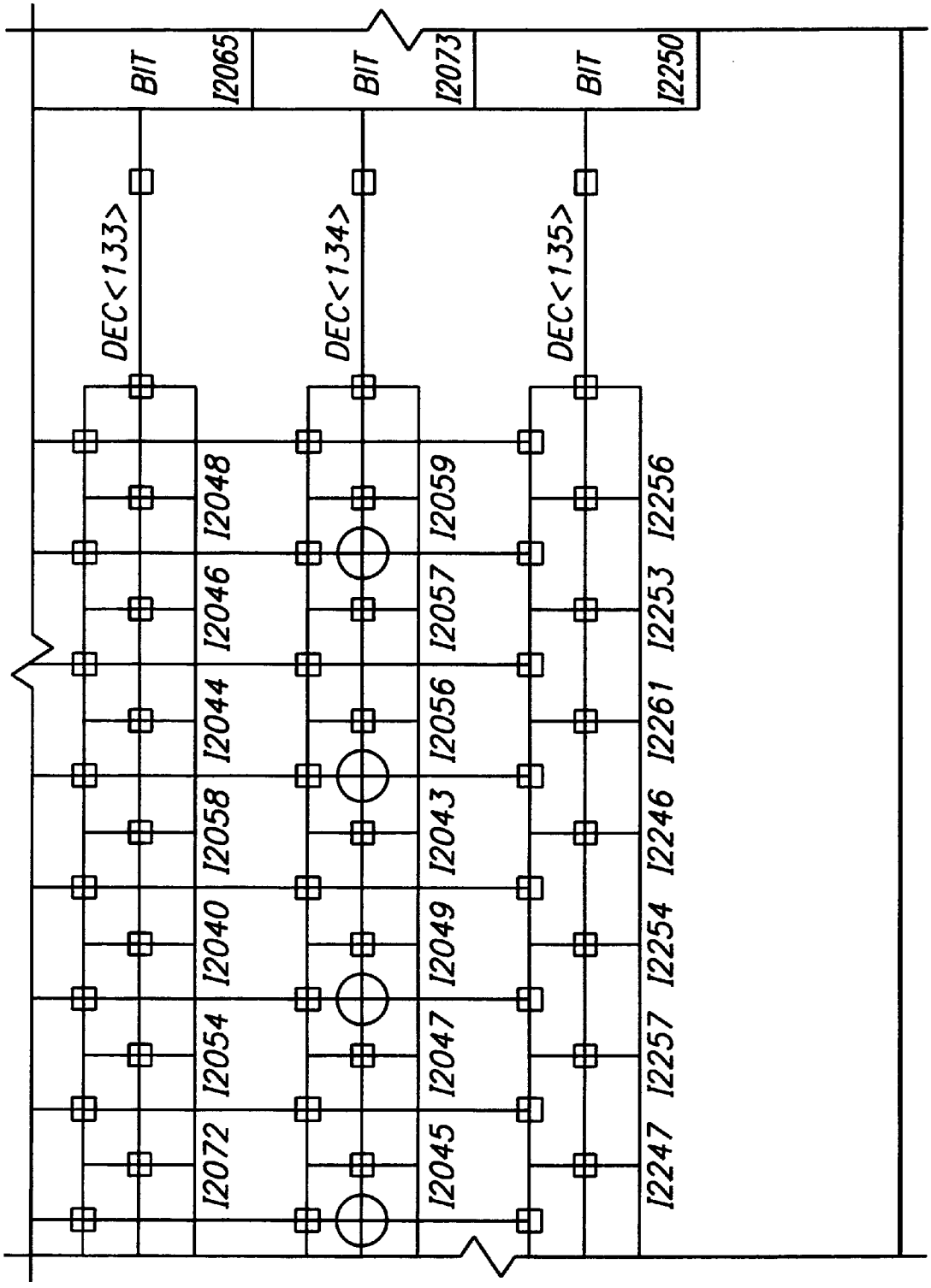

BIT
I2065
BIT
I2073
BIT
I2250
DEC<133>
DEC<134>
DEC<135>
I2048
I2046
I2044
I2058
I2040
I2054
I2072
I2059
I2057
I2056
I2043
I2049
I2047
I2045
I2256
I2253
I2261
I2246
I2254
I2257
I2247

FIG 7,050,711

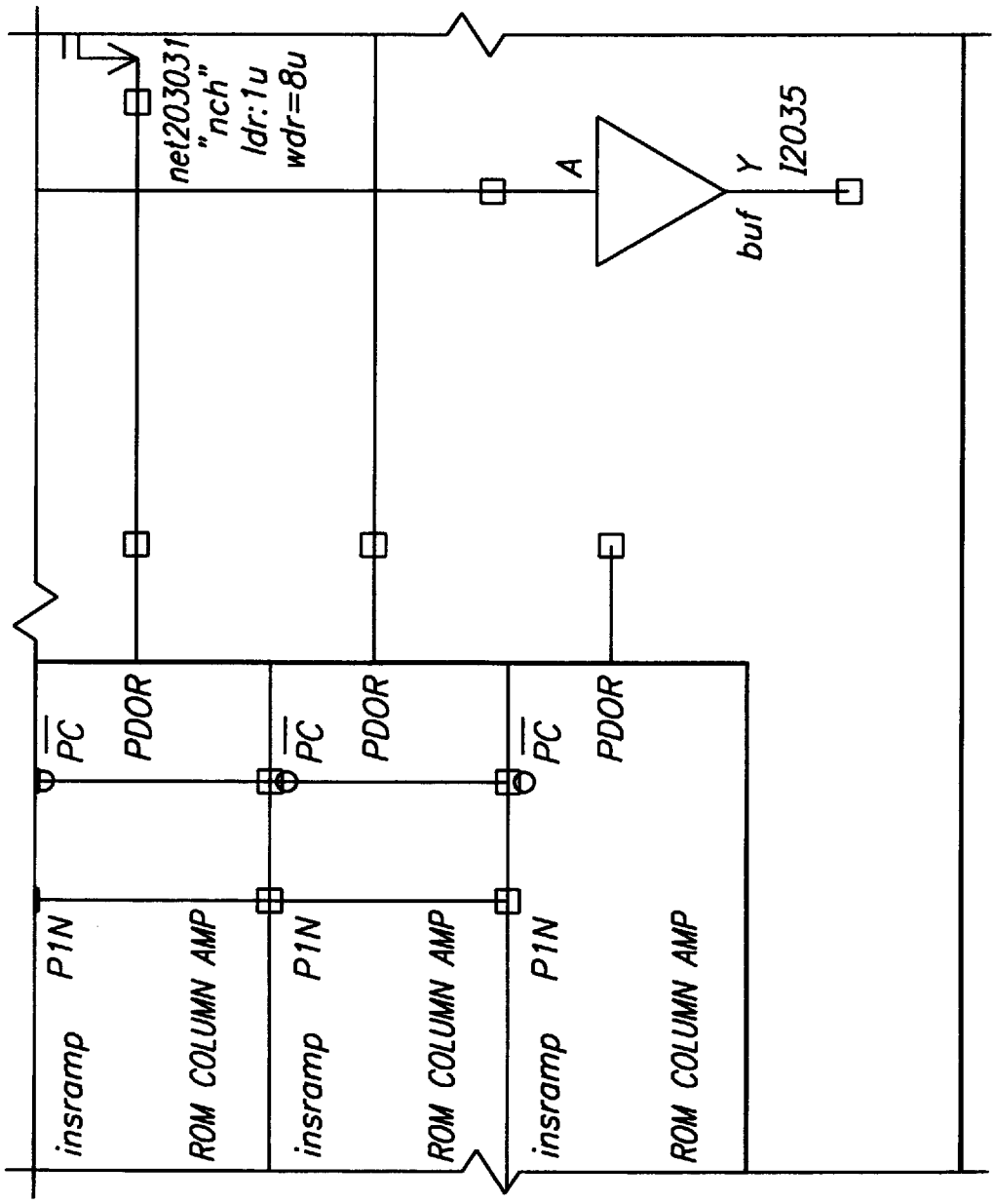

net203031
"nch"
ldr:1u
wdr=8u
A
Y
I2035
buf
PDOR
PC
P1N
insramp
ROM COLUMN AMP

FIG. 1L

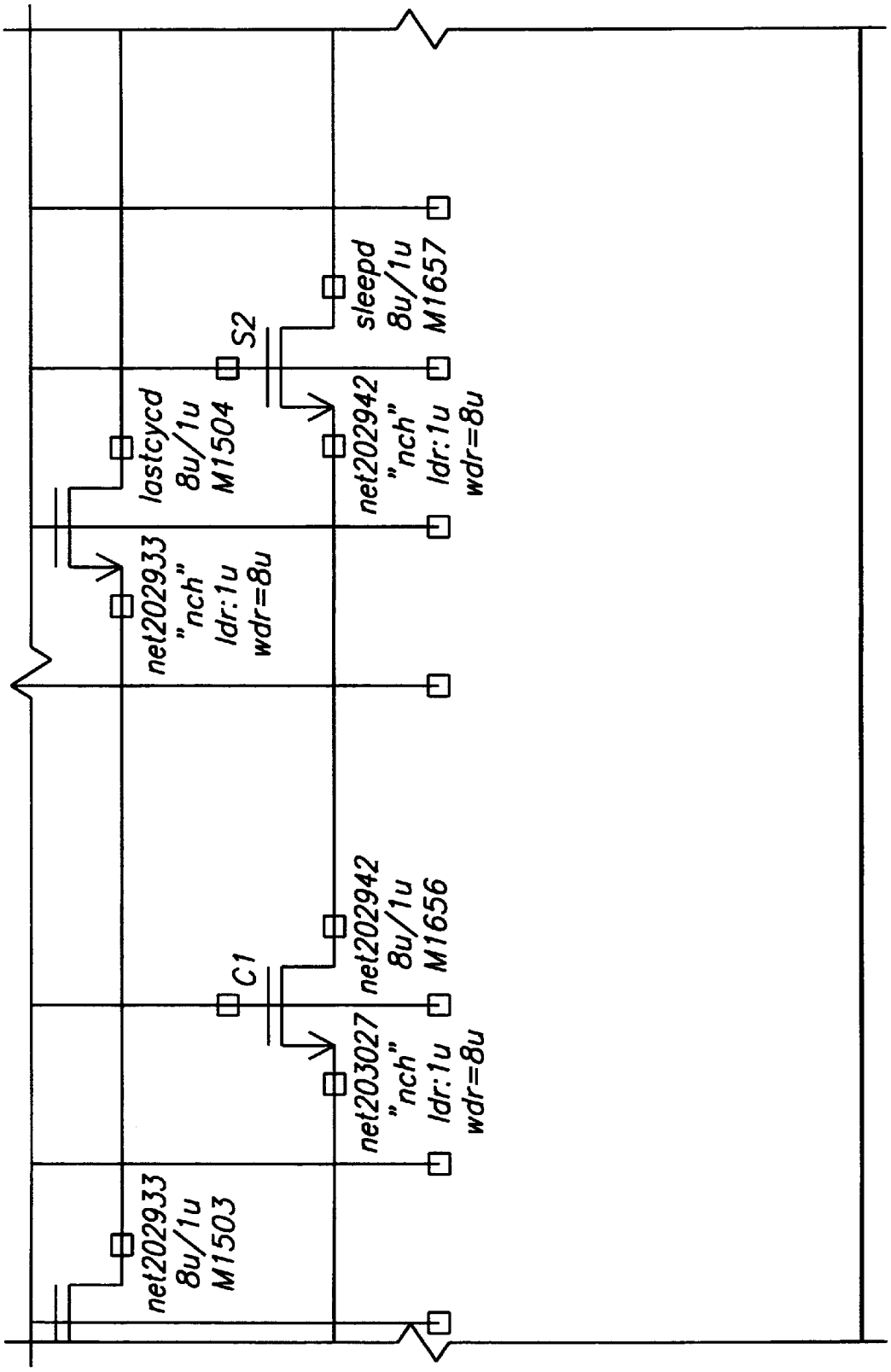

net202933
8u/1u
M1503
net203027
"nch"
ldr:1u
wdr=8u
C1
net202942
8u/1u
M1656
net202933
"nch"
ldr:1u
wdr=8u
lastcycd
8u/1u
M1504
S2
net202942
"nch"
ldr:1u
wdr=8u
sleepd
8u/1u
M1657

FIG. 1,060,811

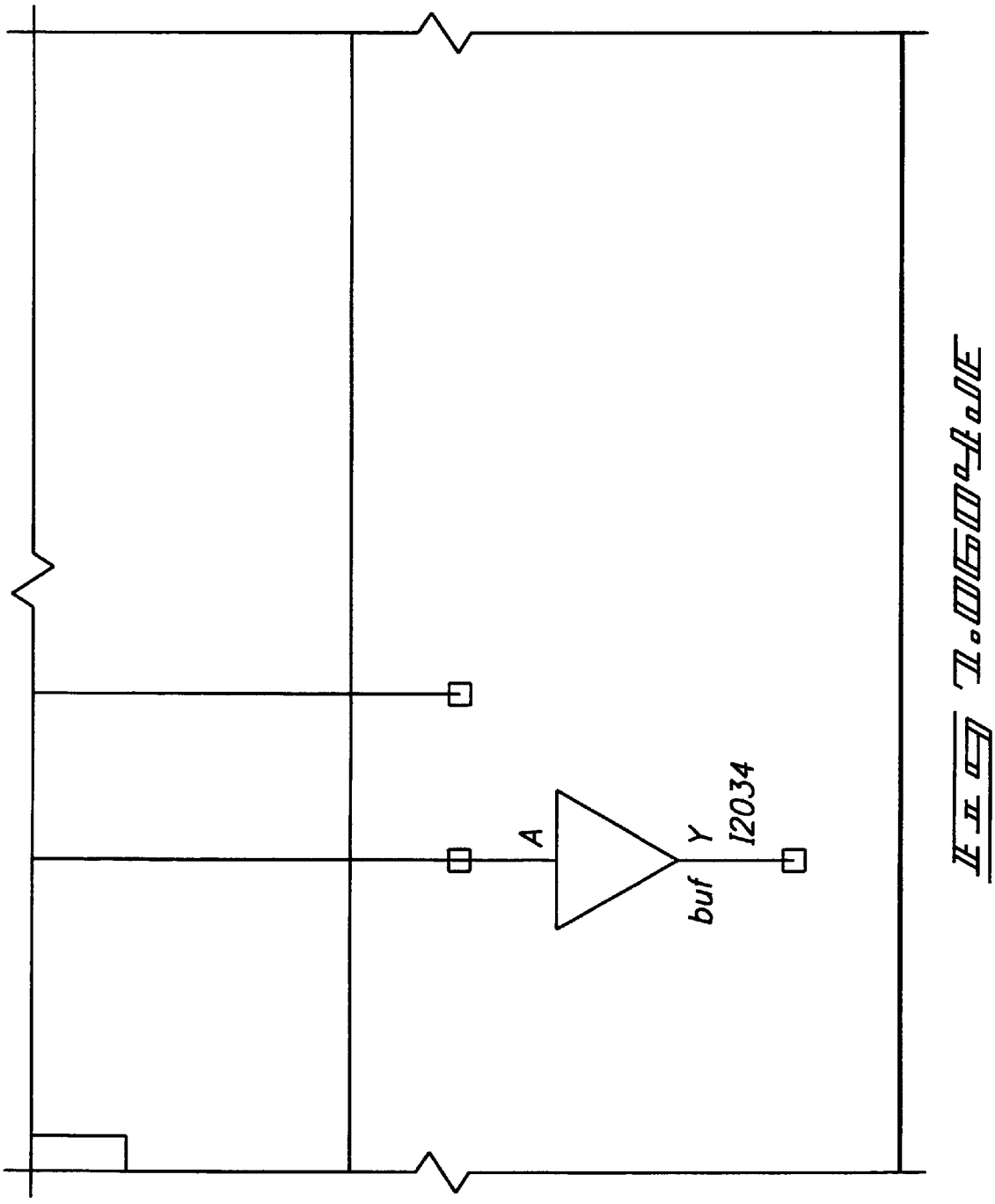


FIG 1,050,048

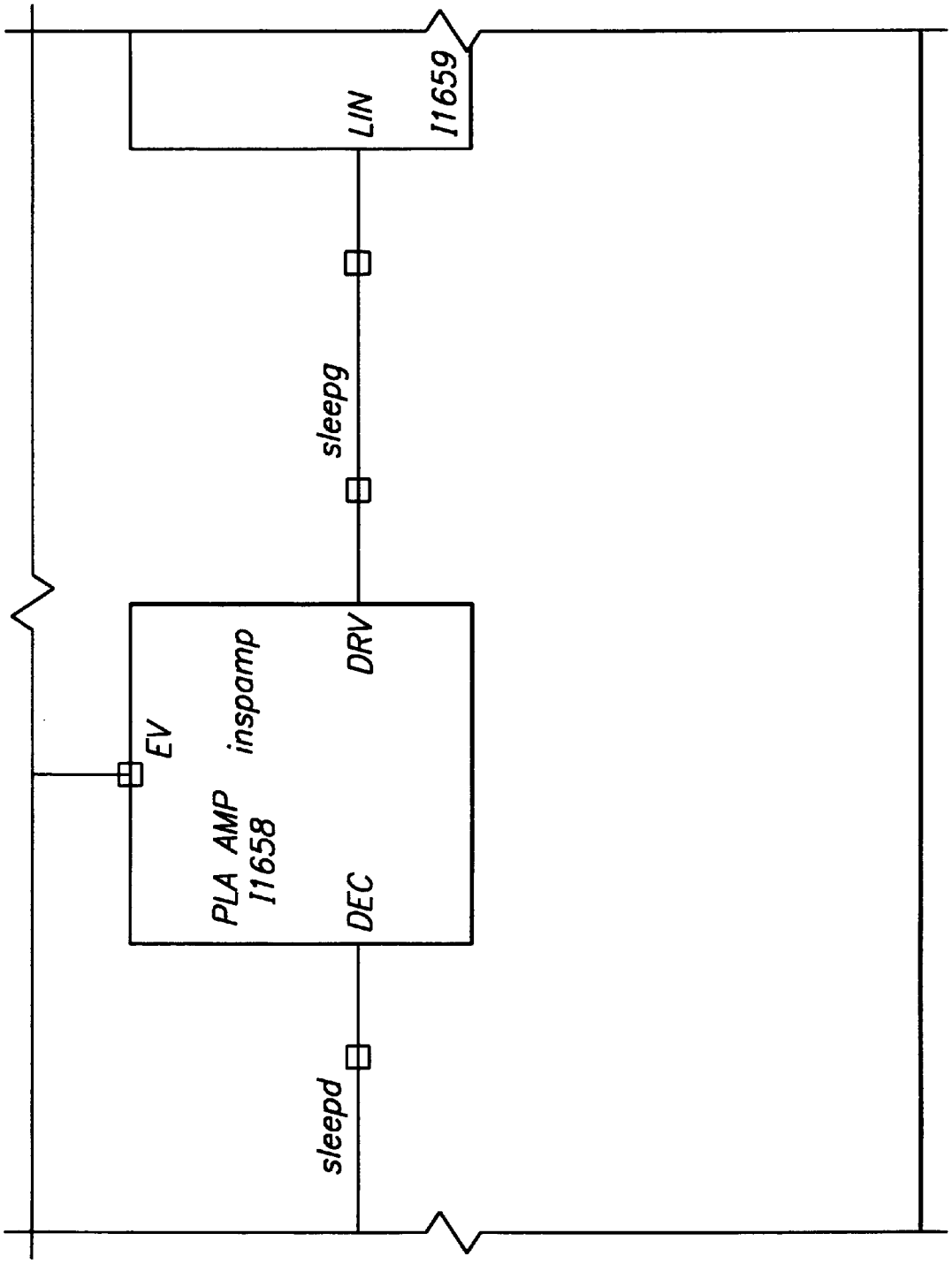


FIG 819

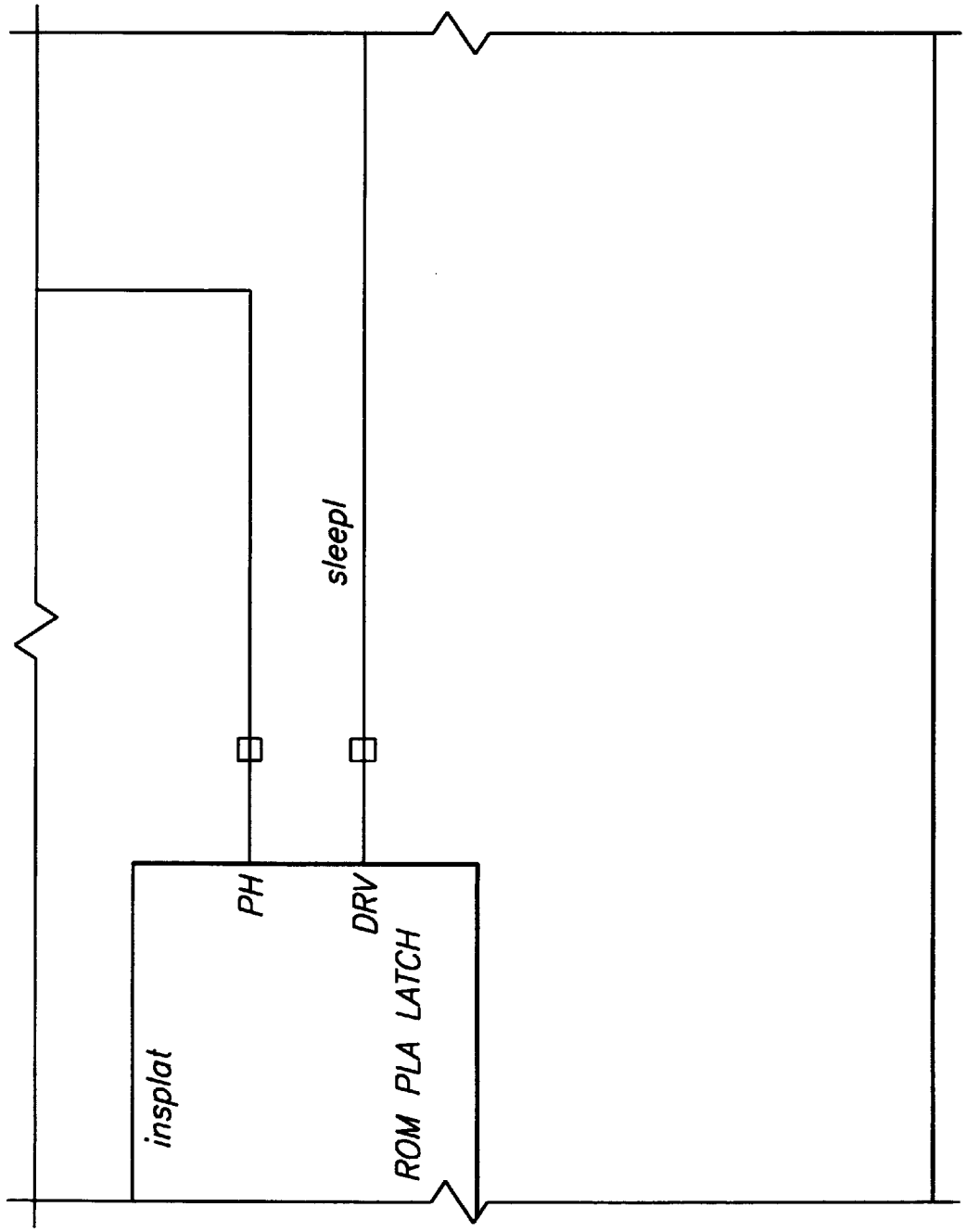


FIG 11,005'L

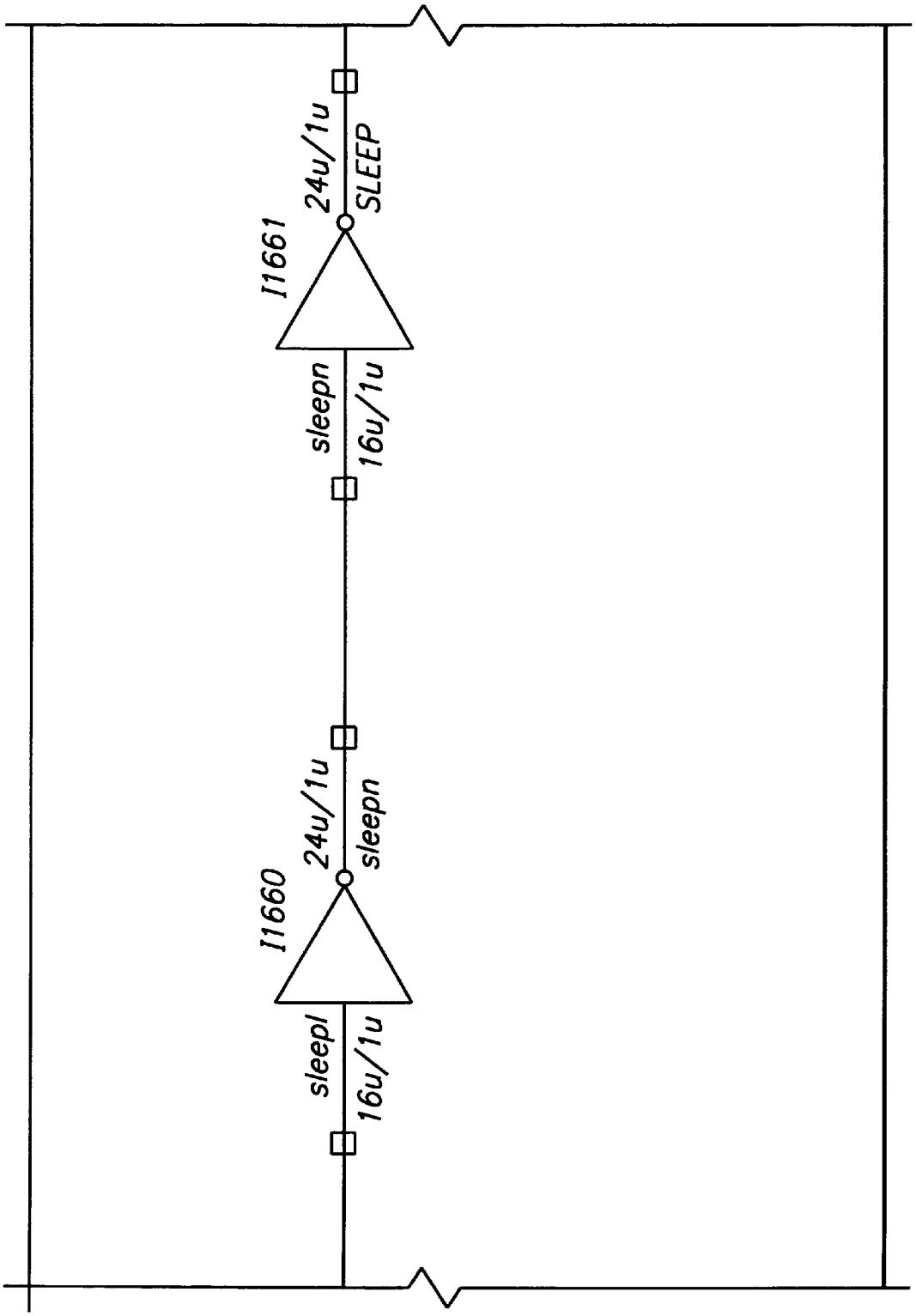
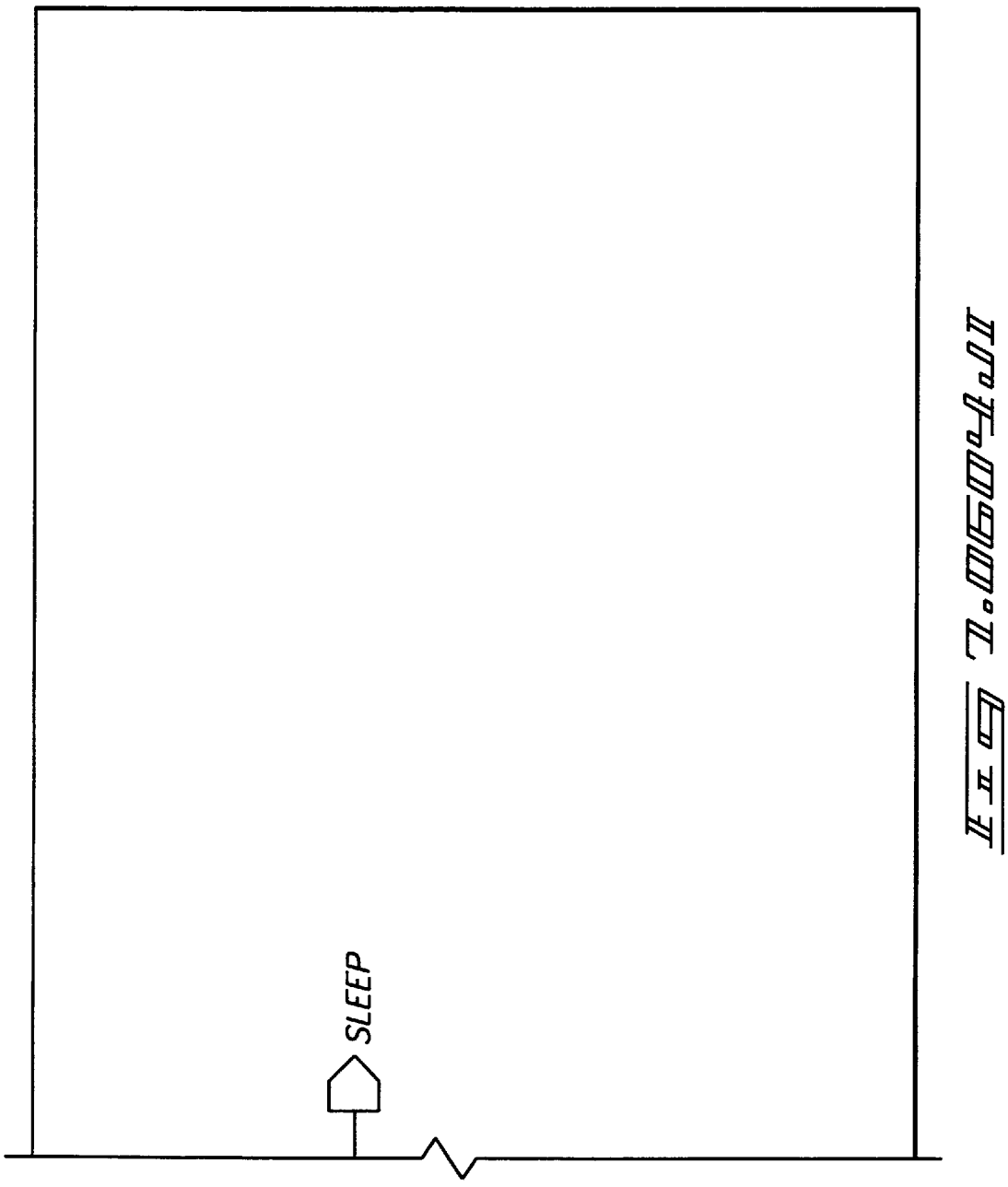

I1661
24u/1u
SLEEP
sleepn
16u/1u
I1660
24u/1u
sleepn
sleepl
16u/1u

FIG. 821


SLEEP
FIG. 700L

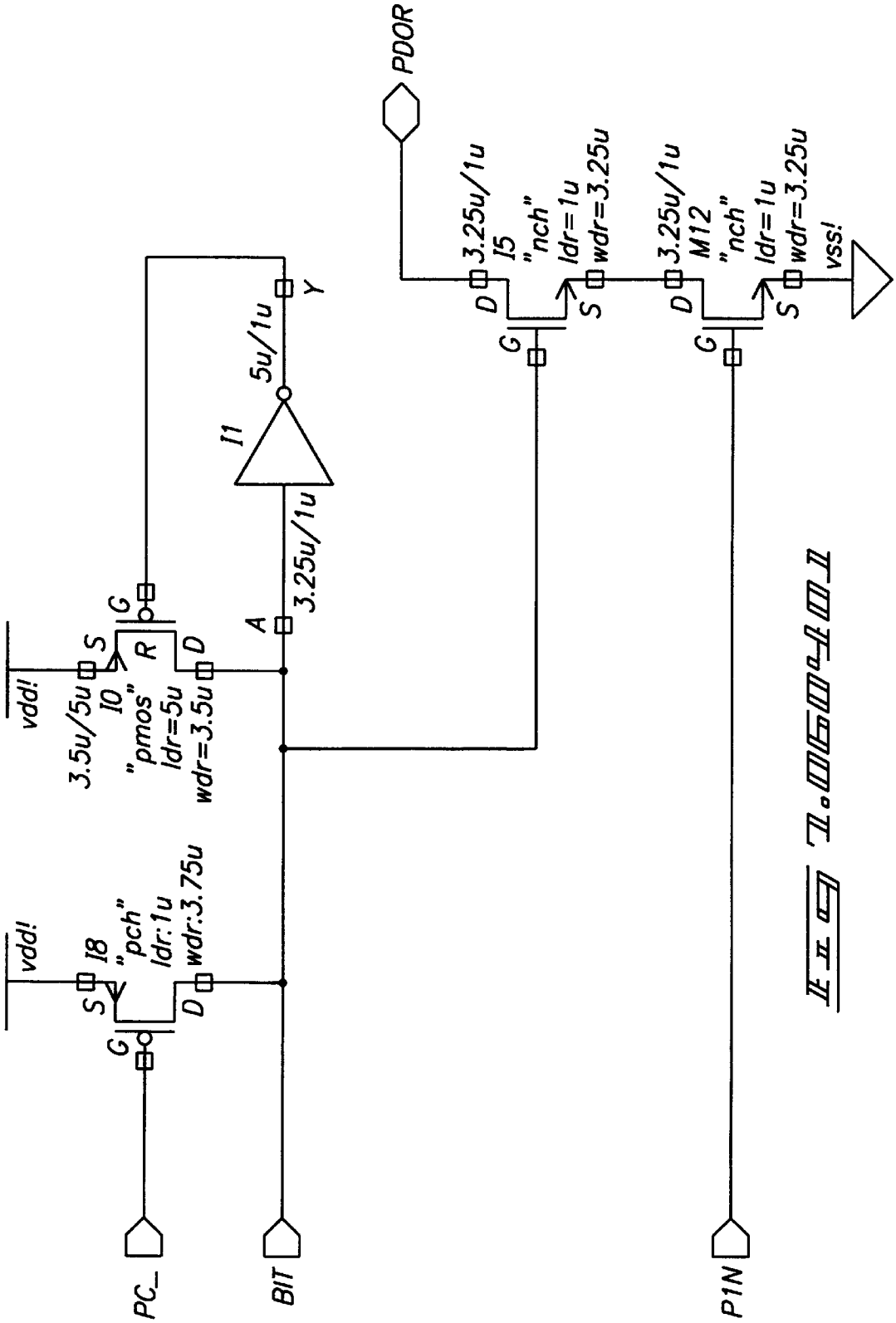

PDOR
3.25u/1u
I5
"nch"
ldr=1u
wdr=3.25u
3.25u/1u
M12
"nch"
ldr=1u
wdr=3.25u
vss!
Y
5u/1u
I1
3.25u/1u
A
G
S
R
D
vdd!
3.5u/5u
I0
"pmos"
ldr=5u
wdr=3.5u
vdd!
I8
"pch"
ldr:1u
wdr:3.75u
PC_
BIT
P1N

FIG 1.0604.II

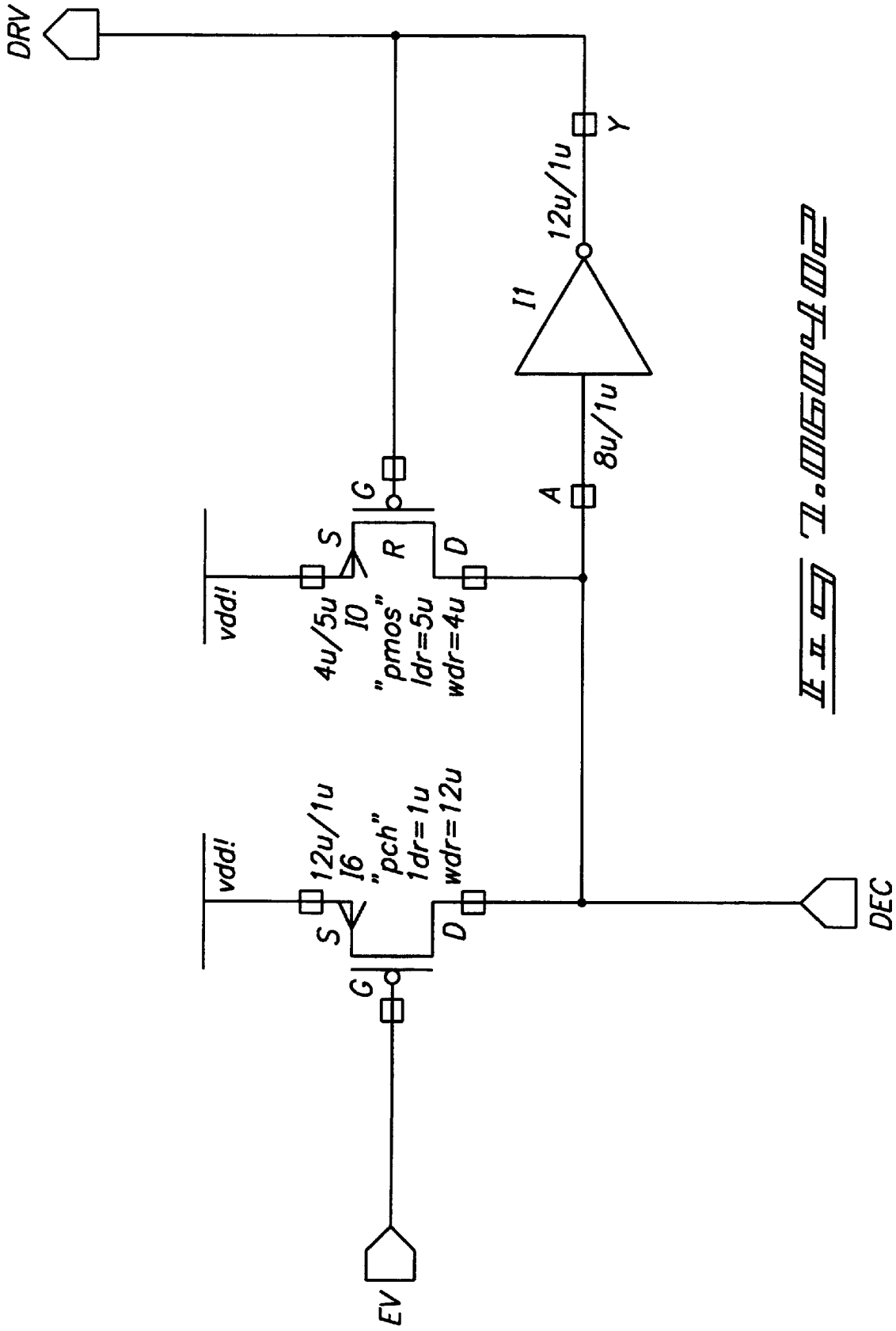
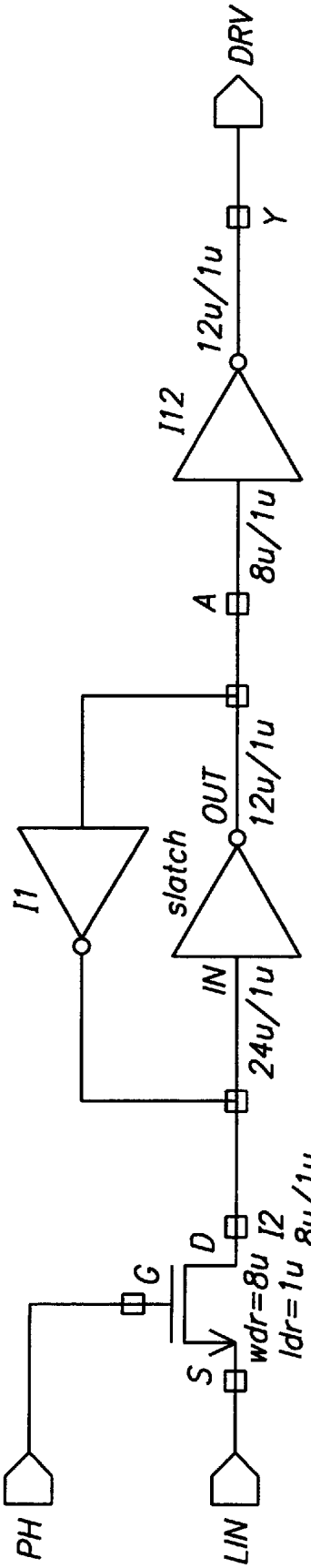

DRV
Y
12u/1u
I1
8u/1u
A
G
S
R
D
vdd!
4u/5u
I0
"pmos"
ldr=5u
wdr=4u
vdd!
12u/1u
I6
"pch"
ldr=1u
wdr=12u
S
D
G
DEC
EV

Fig 6


DRV
Y
12u/1u
I12
8u/1u
A
OUT
12u/1u
I1
slatch
IN
24u/1u
D
I2
8u/1u
G
wdr=8u
ldr=1u
"nch"
S
PH
LIN

Фиг. 825

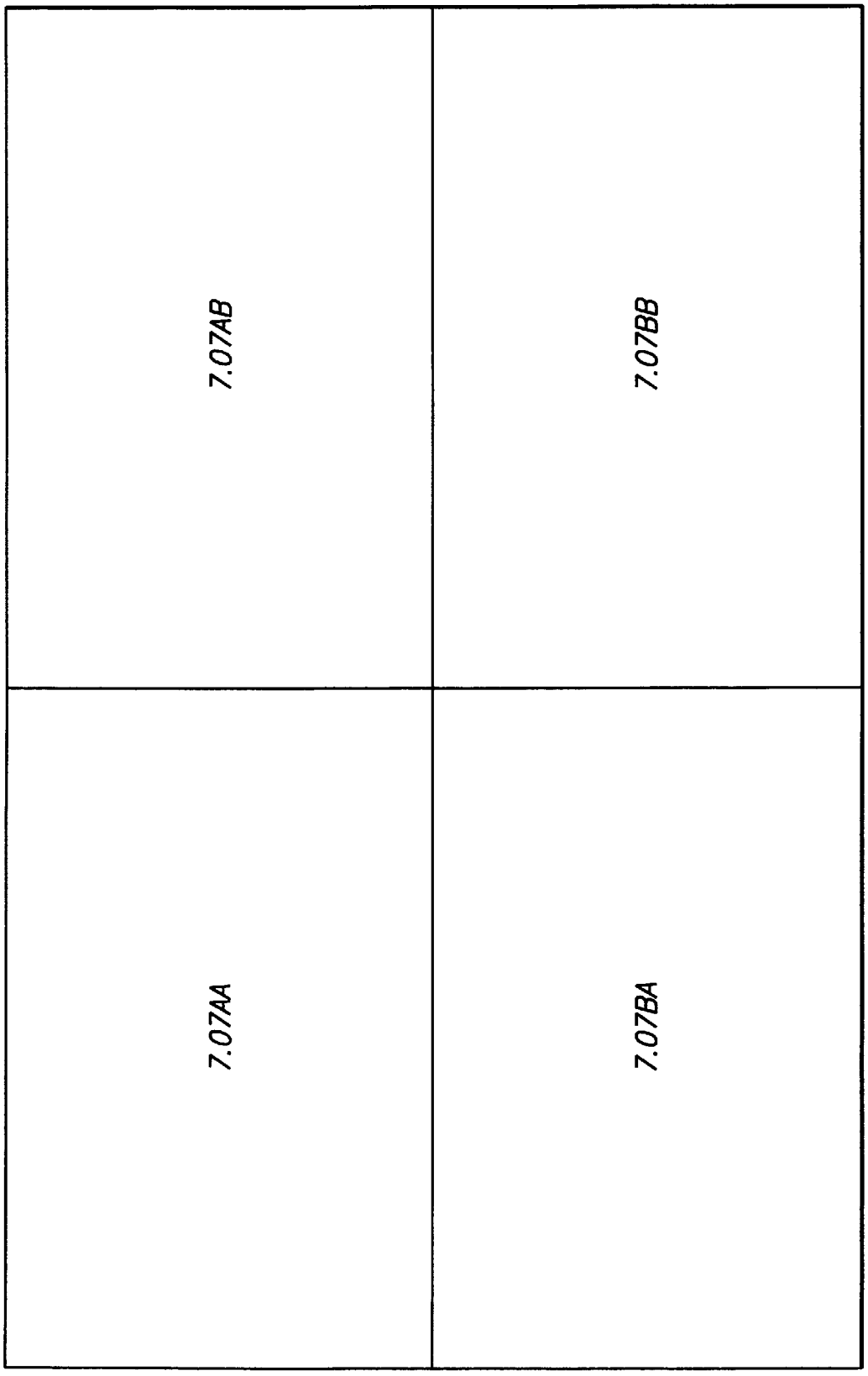
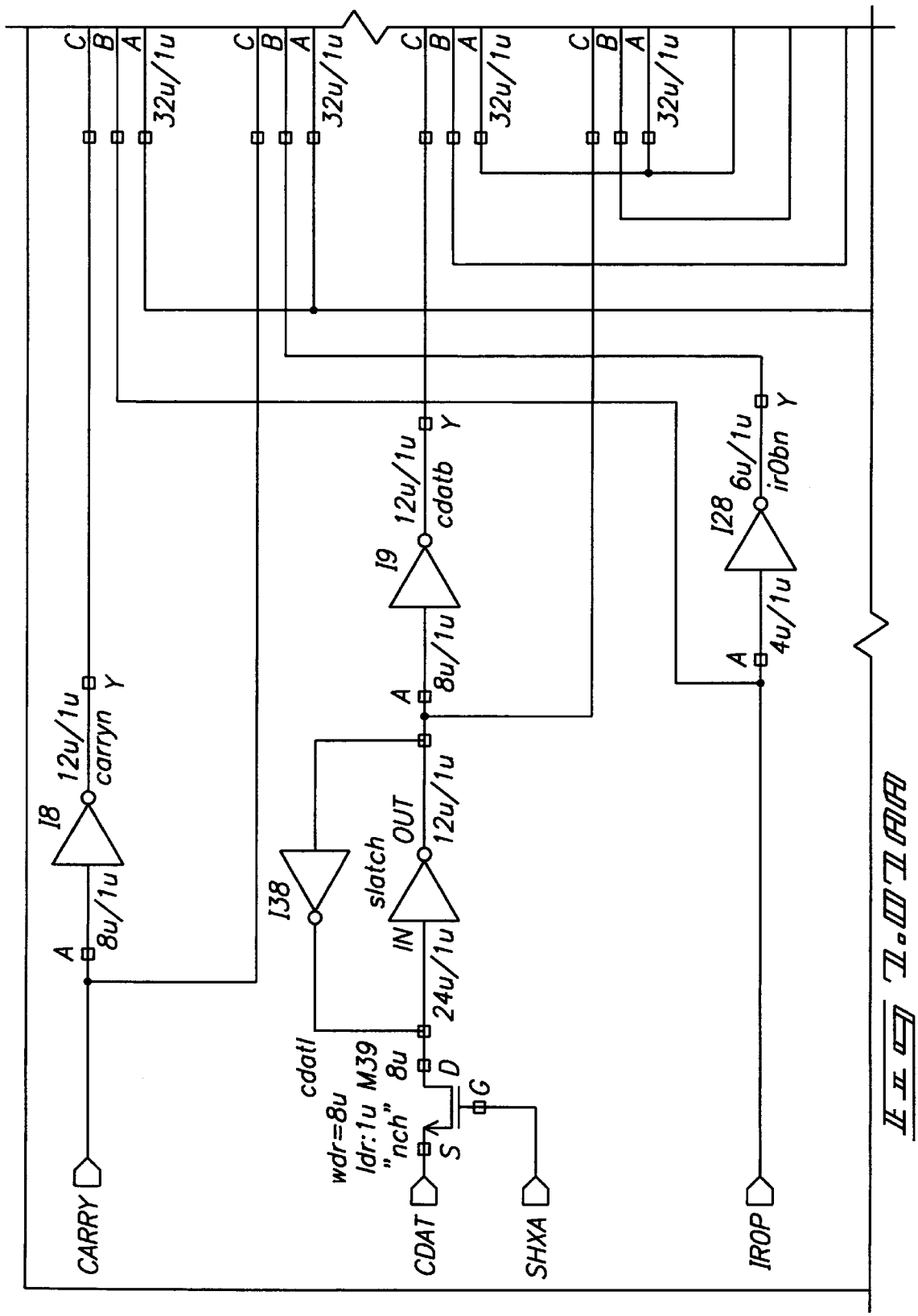
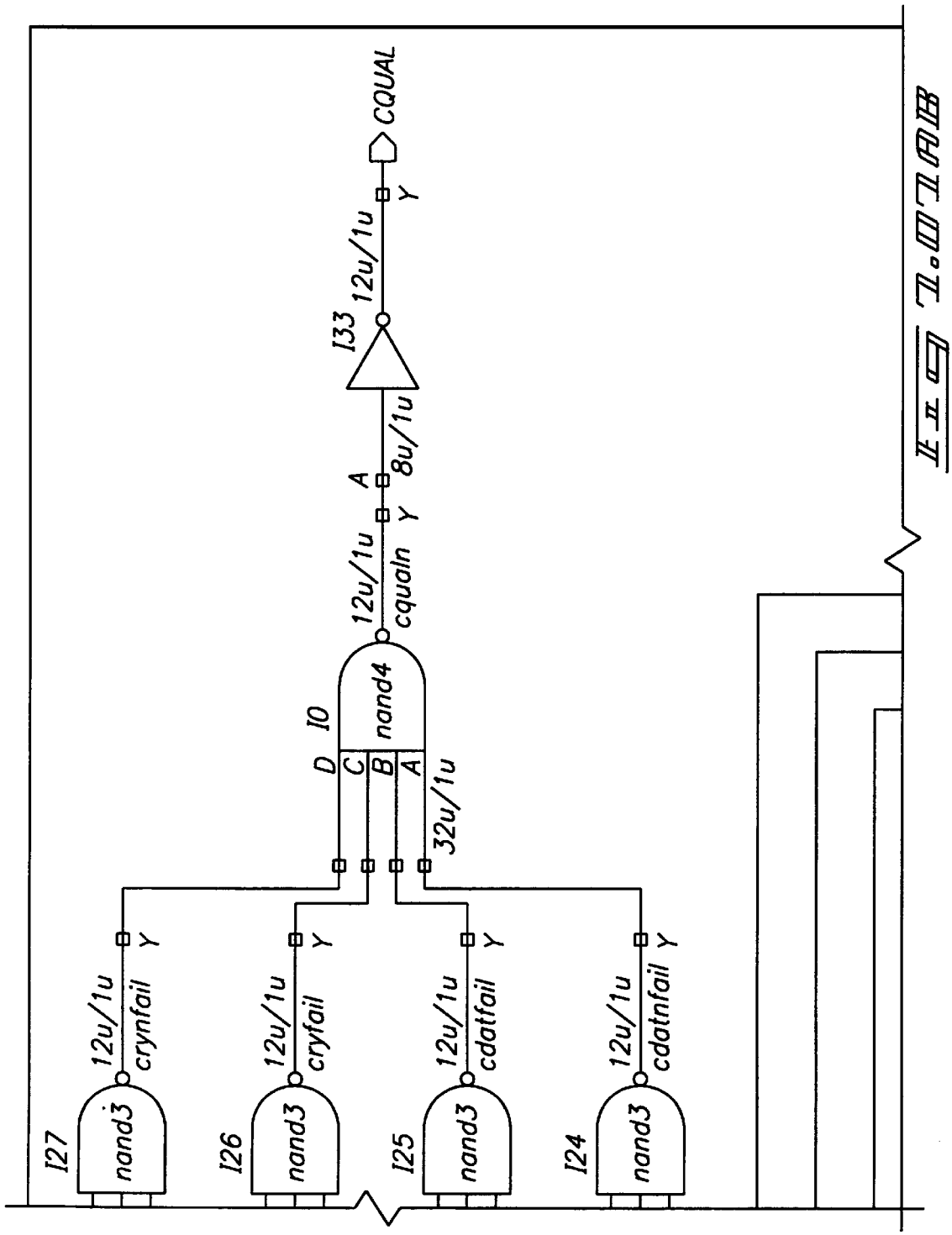


FIG. 7.07L


32u/1u
12u/1u
carryn
I8
8u/1u
12u/1u
cdatb
I9
8u/1u
6u/1u
irObn
I28
4u/1u
I38
slatch
OUT
IN
12u/1u
24u/1u
cdatl
wdr=8u
ldr:1u M39
"nch" 8u
CARRY
CDAT
SHXA
IROP


I27
nand3
12u/1u
crymfail
Y
I26
nand3
12u/1u
cryfail
Y
I25
nand3
12u/1u
cdatfail
Y
I24
nand3
12u/1u
cdatnfail
Y
I0
nand4
D
C
B
A
32u/1u
12u/1u
cqualn
Y
A
8u/1u
I33
12u/1u
Y
CQUAL

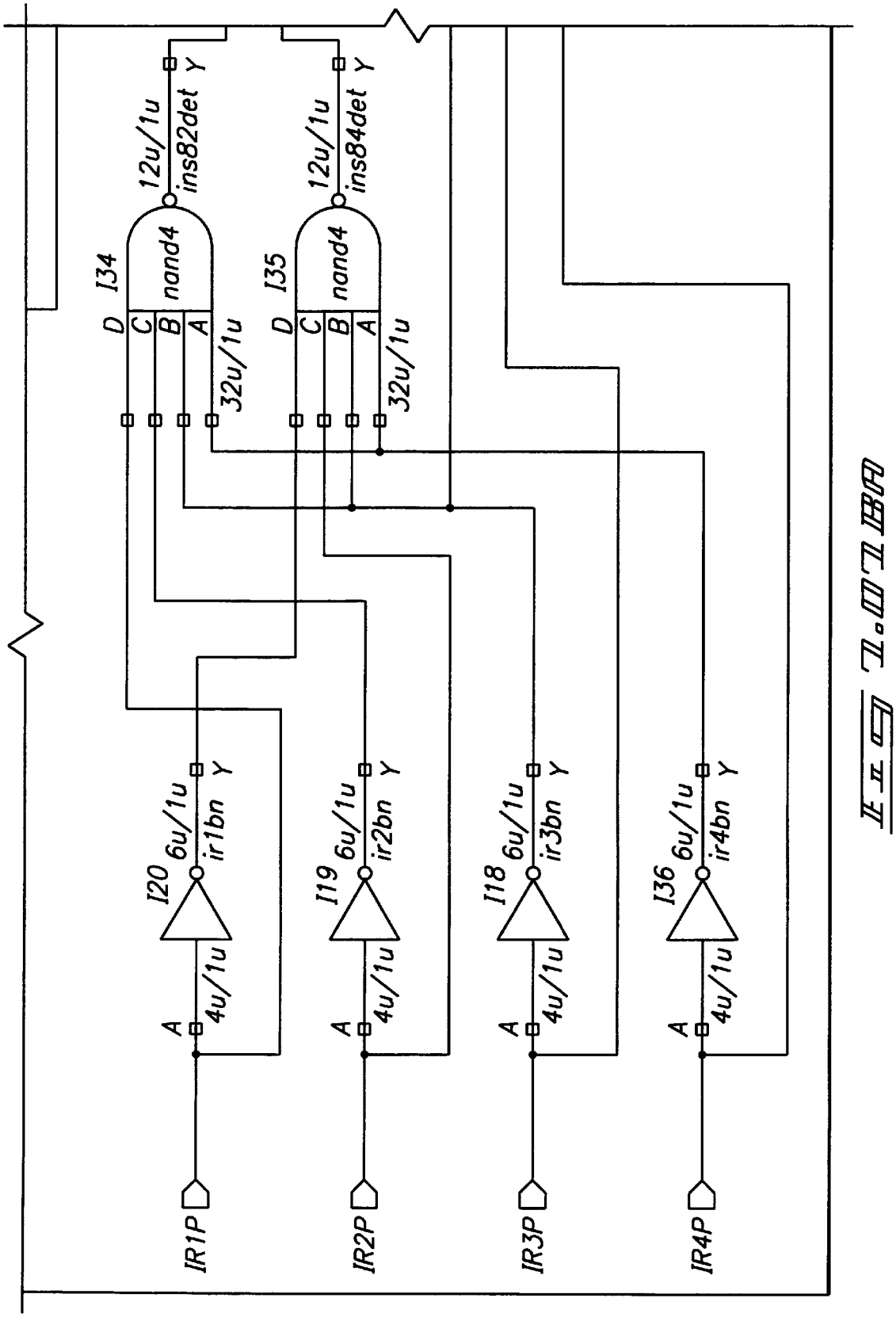

I34
nand4
12u/1u
ins82det
Y
D
C
B
A
32u/1u
I35
nand4
12u/1u
ins84det
Y
D
C
B
A
32u/1u
I20
6u/1u
ir1bn
Y
A
4u/1u
I19
6u/1u
ir2bn
Y
A
4u/1u
I18
6u/1u
ir3bn
Y
A
4u/1u
I36
6u/1u
ir4bn
Y
A
4u/1u
IR1P
IR2P
IR3P
IR4P

FIG 1.00 IBM

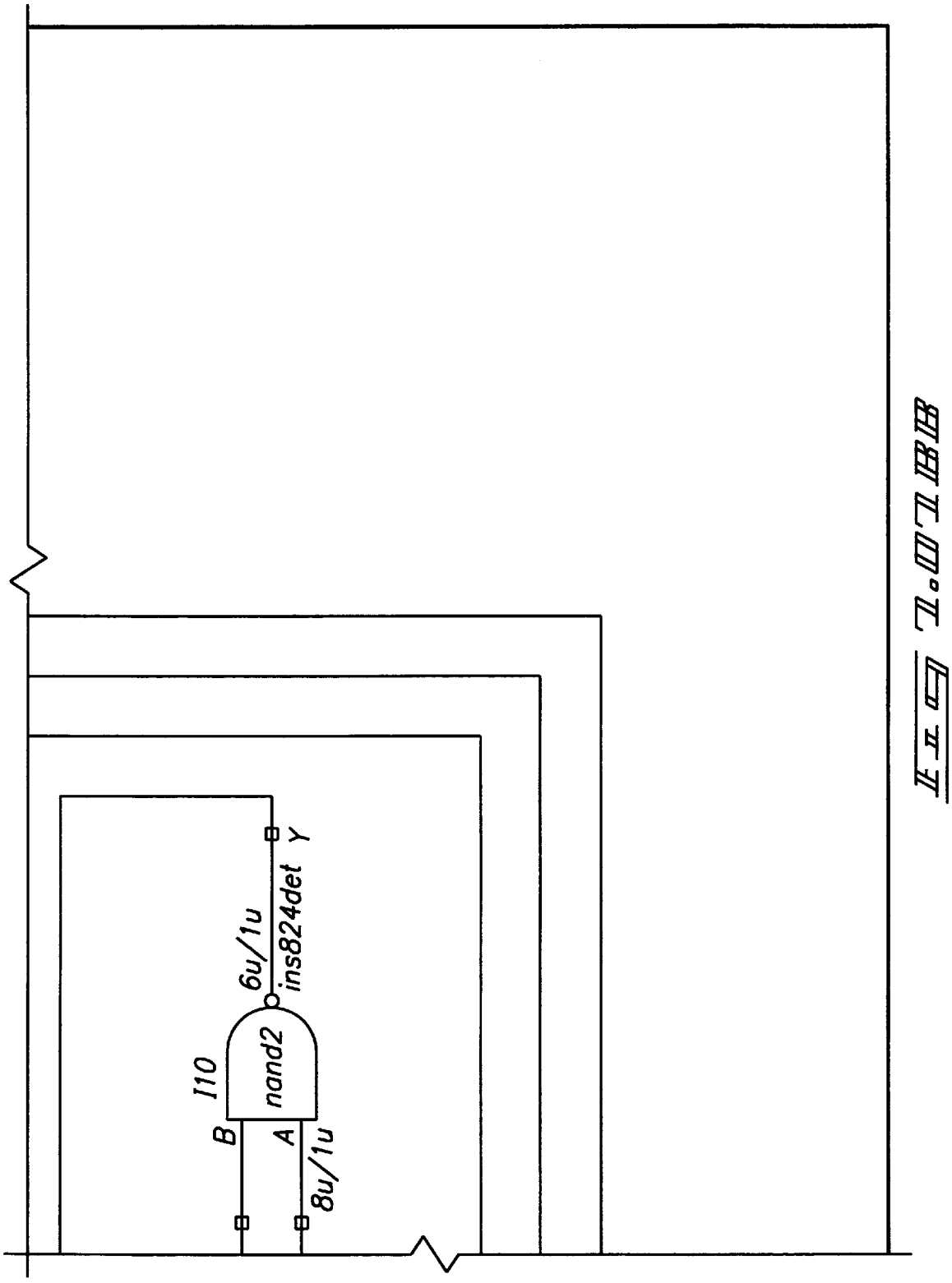


FIG. 1,001
6u/1u
ins824det
Y
110
nand2
B
A
8u/1u

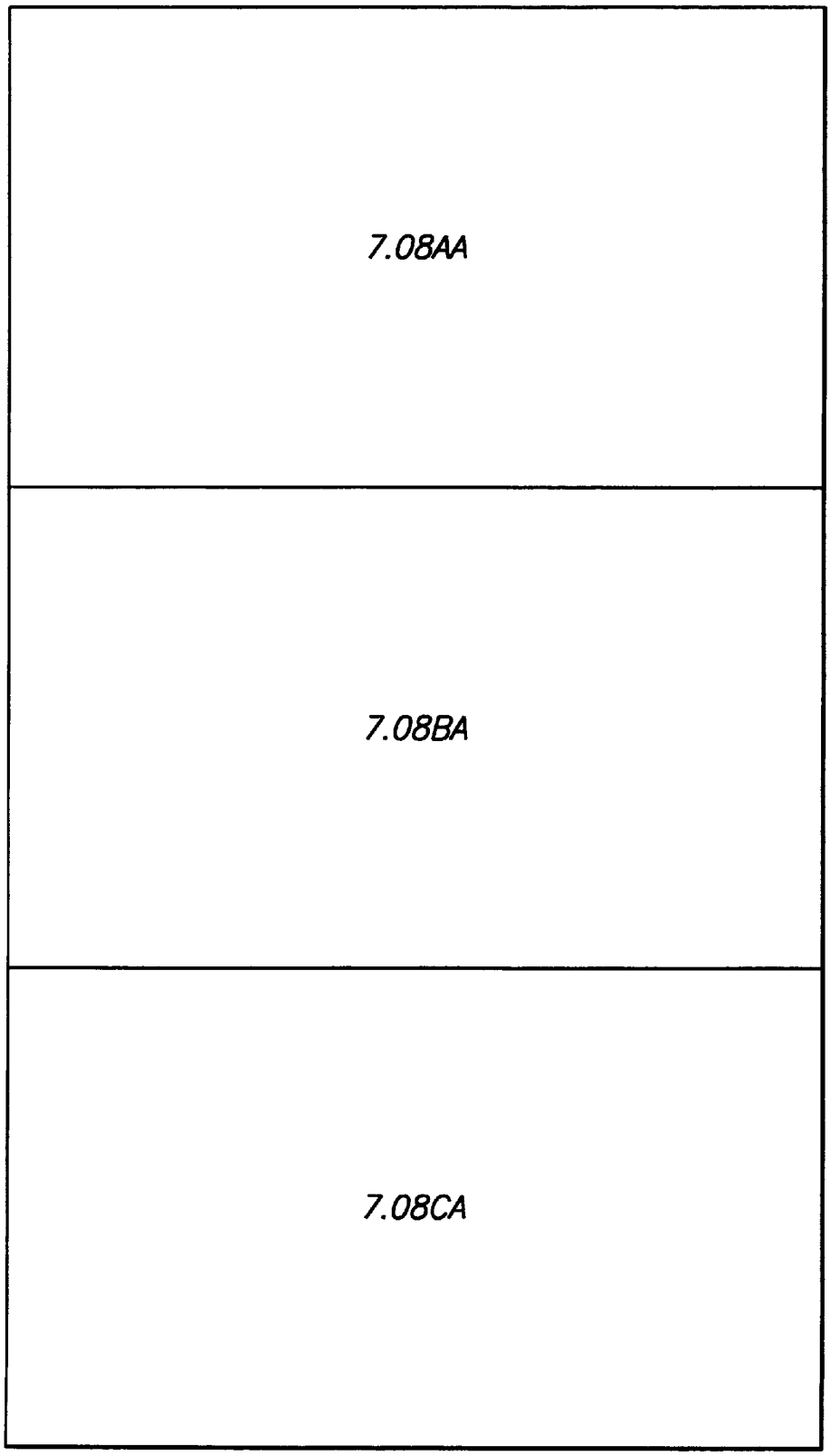


Fig 7.08B

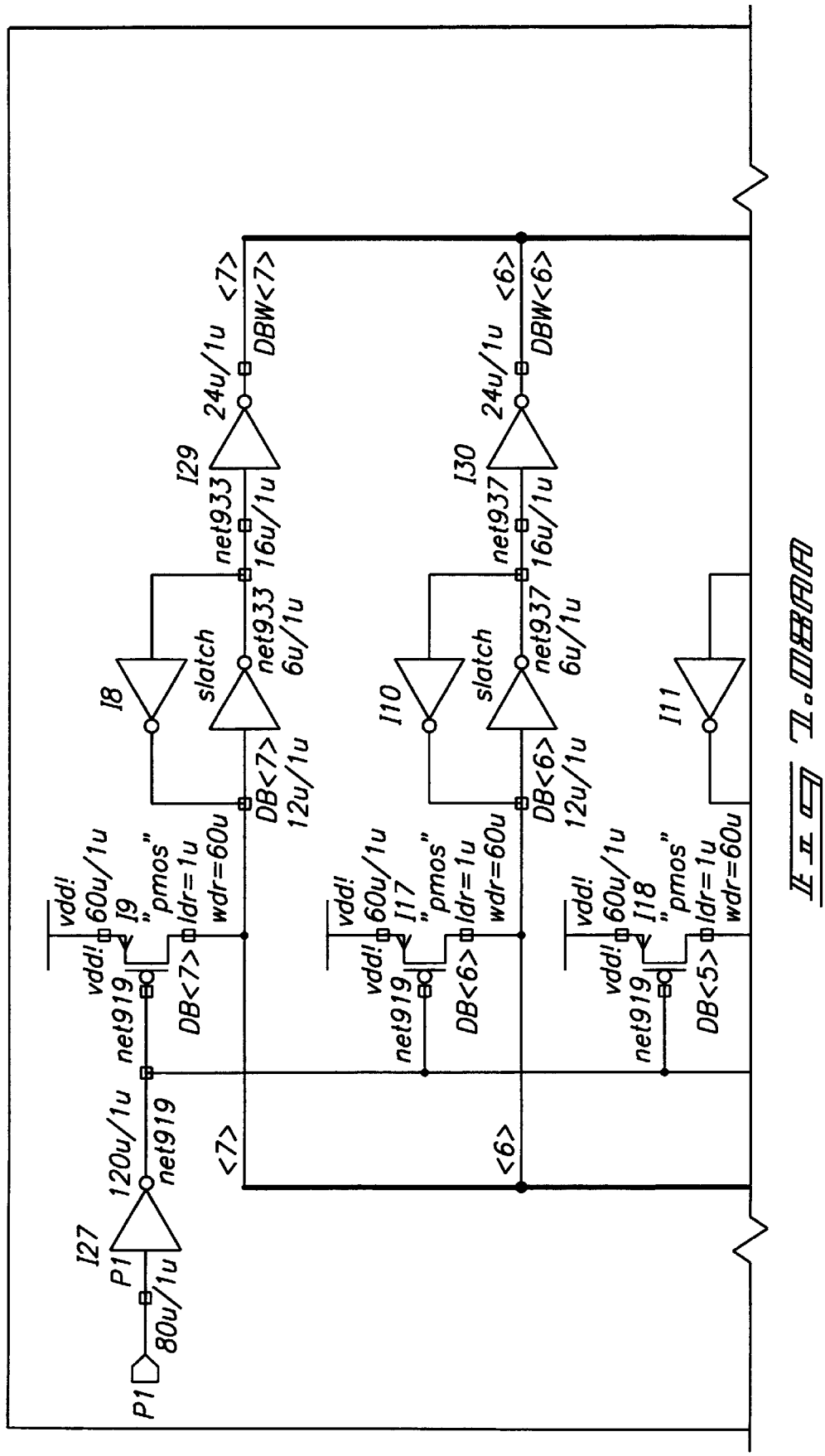


FIG. 11.0BBAAA

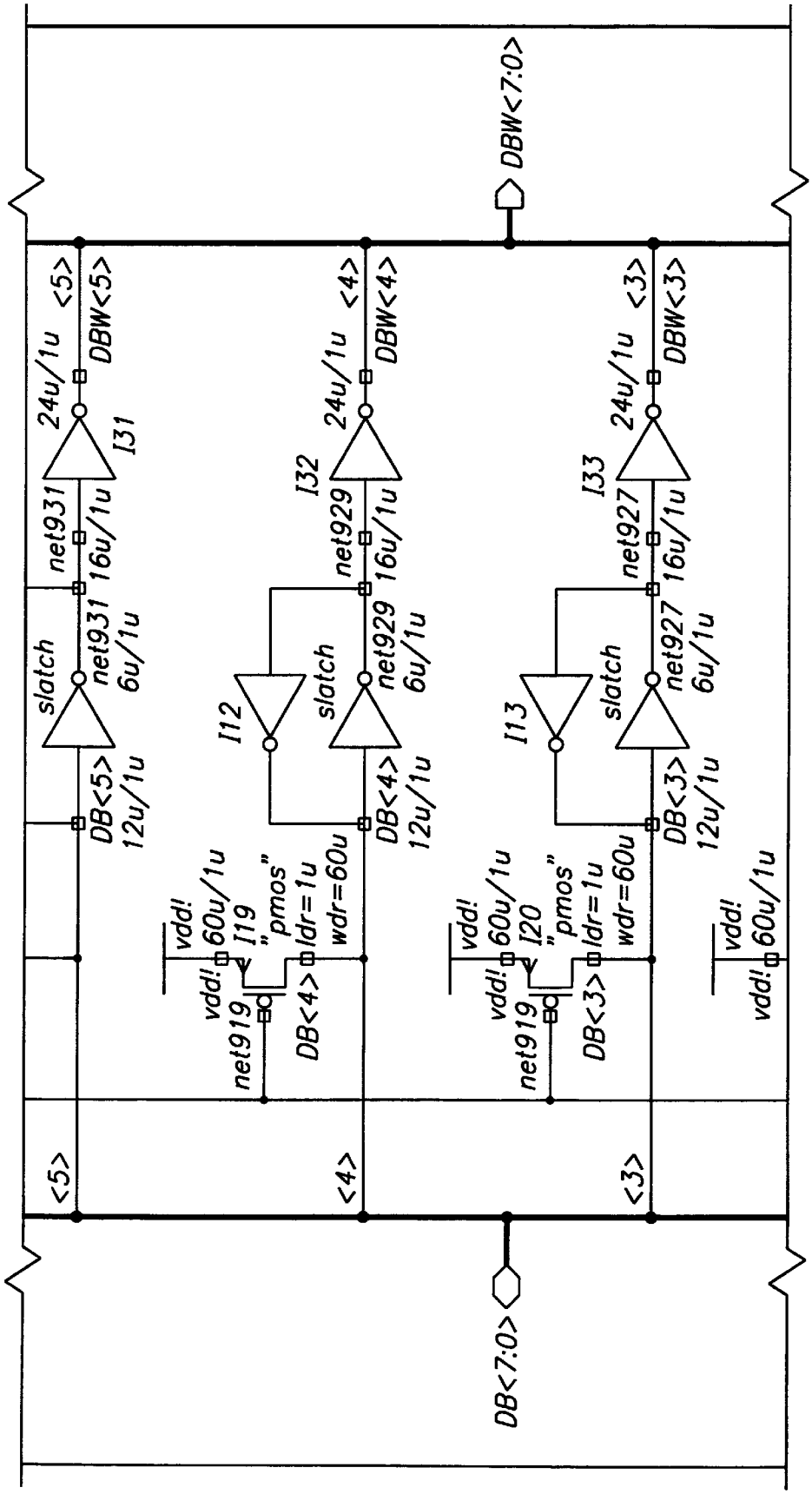

DBW<7:0>
DB<7:0>
<5>
<4>
<3>
24u/1u
DBW<5>
DBW<4>
DBW<3>
I31
I32
I33
net931
net929
net927
16u/1u
6u/1u
slatch
I12
I13
DB<5>
DB<4>
DB<3>
12u/1u
vdd!
60u/1u
I19
I20
"pmos"
ldr=1u
wdr=60u
net919

FIG. 833A

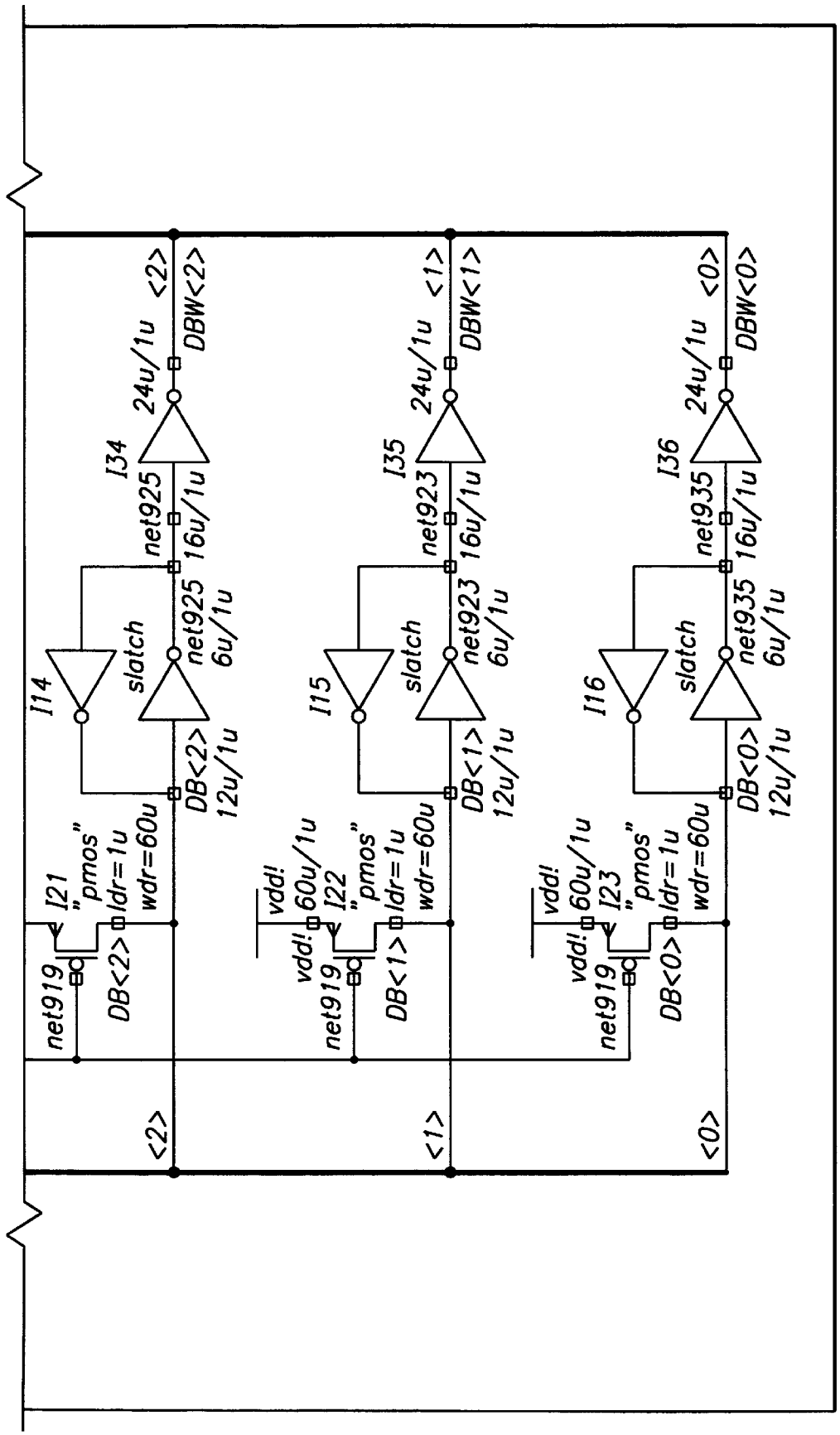

I34
24u/1u
<2>
DBW<2>
net925
16u/1u
net925
6u/1u
slatch
I14
DB<2>
12u/1u
I21
"pmos"
ldr=1u
wdr=60u
vdd!
60u/1u
net919
DB<2>
<2>
I35
24u/1u
<1>
DBW<1>
net923
16u/1u
net923
6u/1u
slatch
I15
DB<1>
12u/1u
I22
"pmos"
ldr=1u
wdr=60u
vdd!
60u/1u
net919
DB<1>
<1>
I36
24u/1u
<0>
DBW<0>
net935
16u/1u
net935
6u/1u
slatch
I16
DB<0>
12u/1u
I23
"pmos"
ldr=1u
wdr=60u
vdd!
60u/1u
net919
DB<0>
<0>

FIG. 834

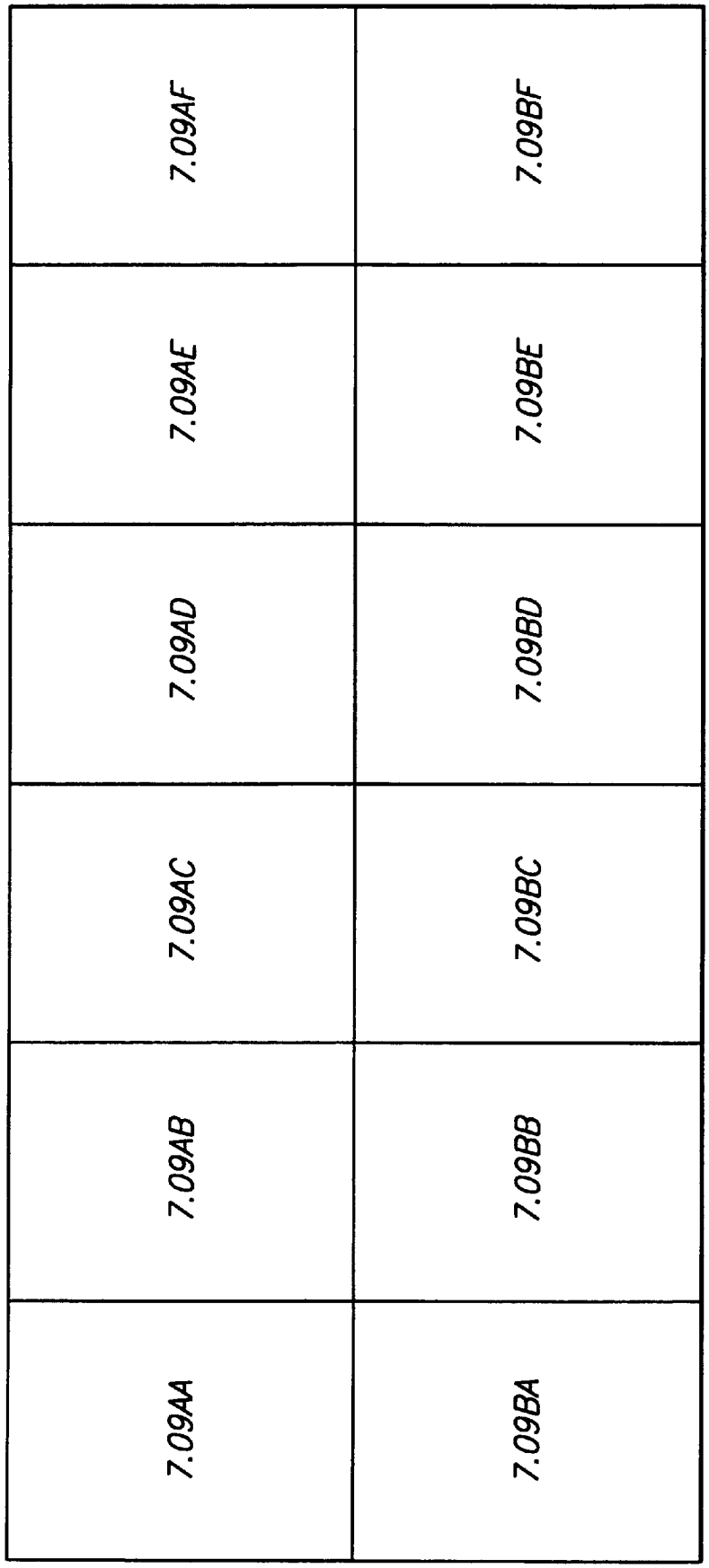
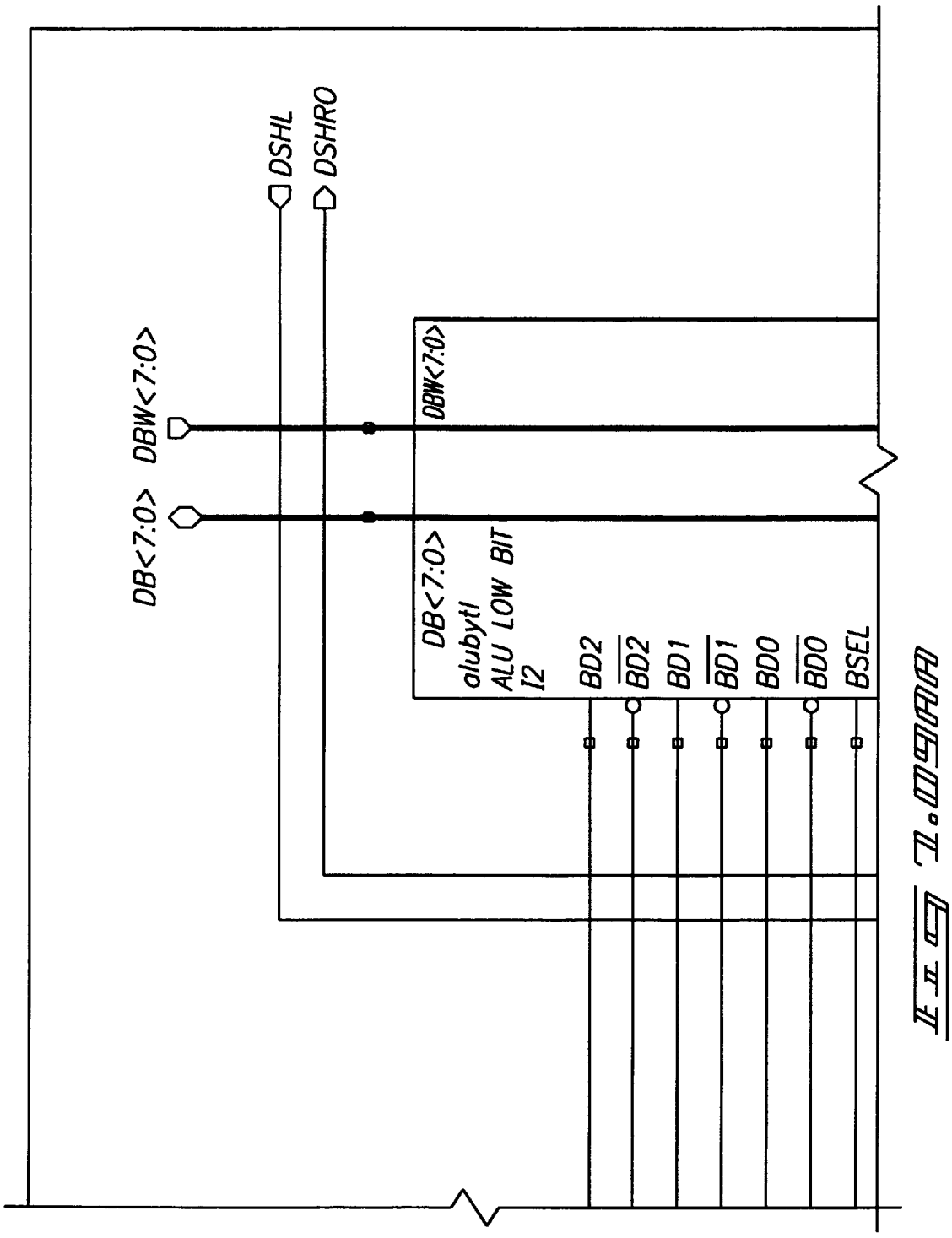

7.09AF
7.09BF
7.09AE
7.09BE
7.09AD
7.09BD
7.09AC
7.09BC
7.09AB
7.09BB
7.09AA
7.09BA

FIG. 7.09


DSHL
DSHRO
DBW<7:0>
DB<7:0>
DBW<7:0>
DB<7:0>
alubyt1
ALU LOW BIT
I2
BD2
BD2
BD1
BD1
BD0
BD0
BSEL

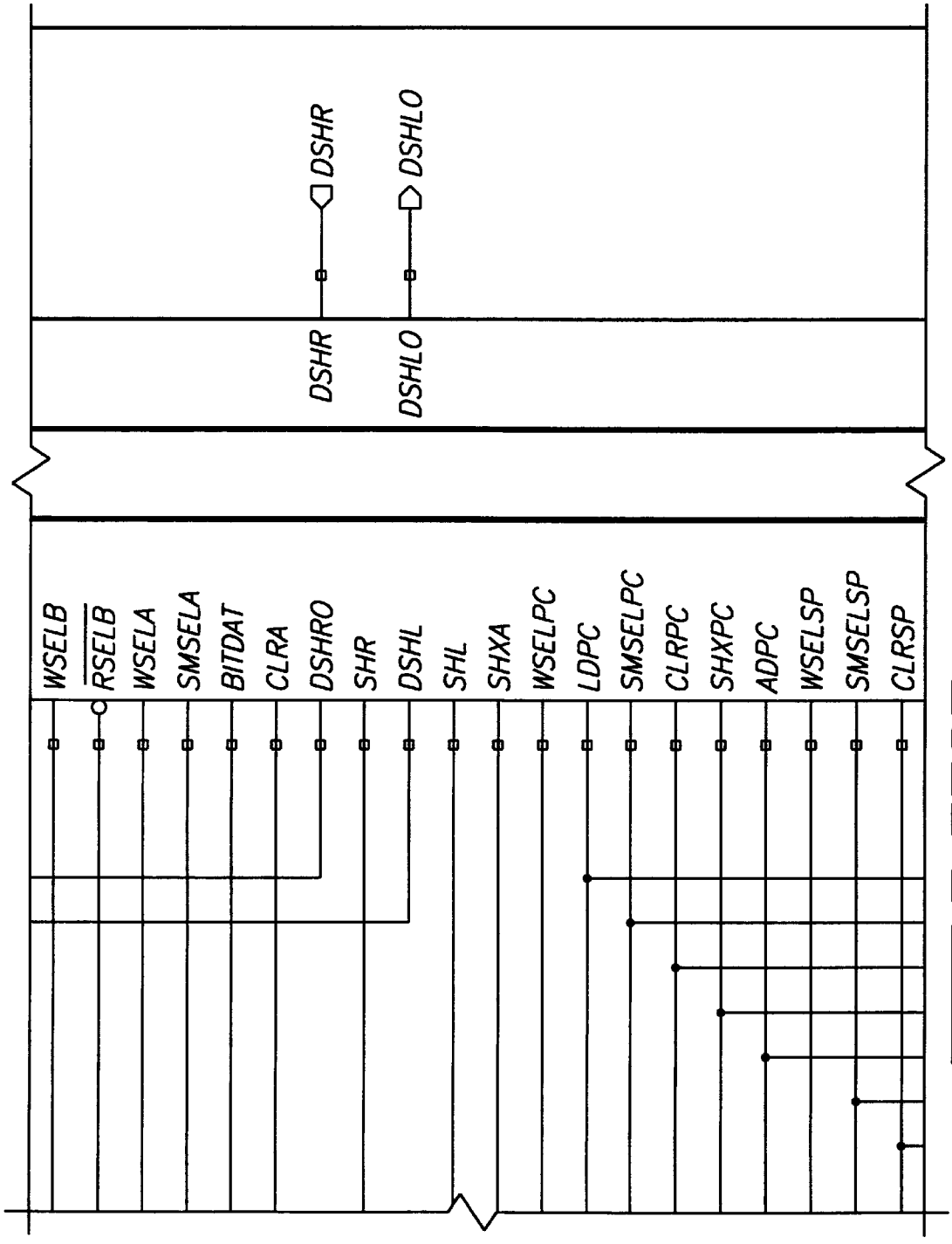

DSHR
DSHLO
DSHR
DSHLO
WSELB
RSELB
WSELA
SMSELA
BITDAT
CLRA
DSHRO
SHR
DSHL
SHL
SHXA
WSELPC
LDPC
SMSELPC
CLRPC
SHXPC
ADPC
WSELSP
SMSELSP
CLRSP

FIG. 837

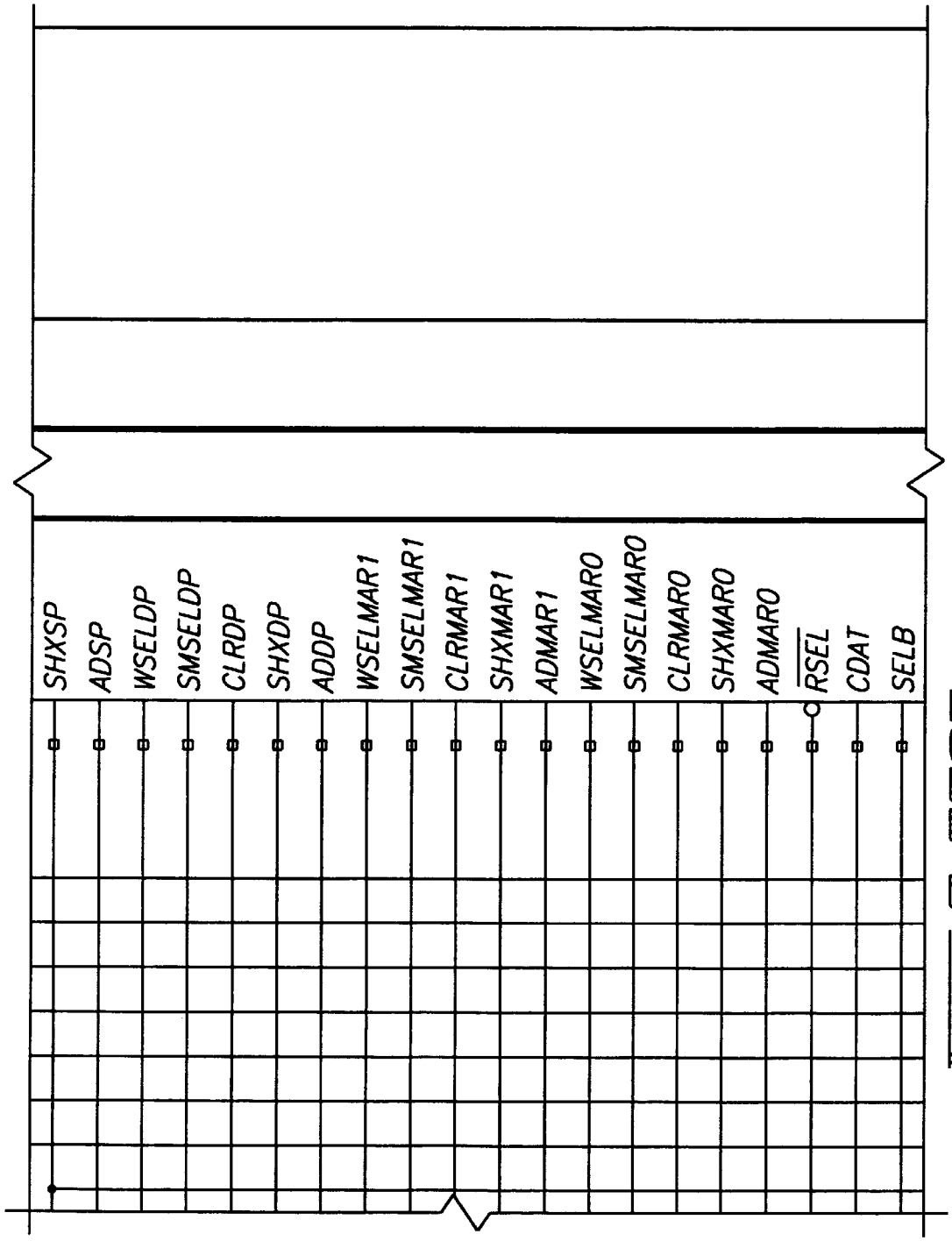

SHXSP
ADSP
WSELDP
SMSELDP
CLRDP
SHXDP
ADDP
WSELMAR1
SMSELMAR1
CLRMAR1
SHXMAR1
ADMAR1
WSELMAR0
SMSELMAR0
CLRMAR0
SHXMAR0
ADMAR0
RSEL
CDAT
SELB

FIG. 6.0AL

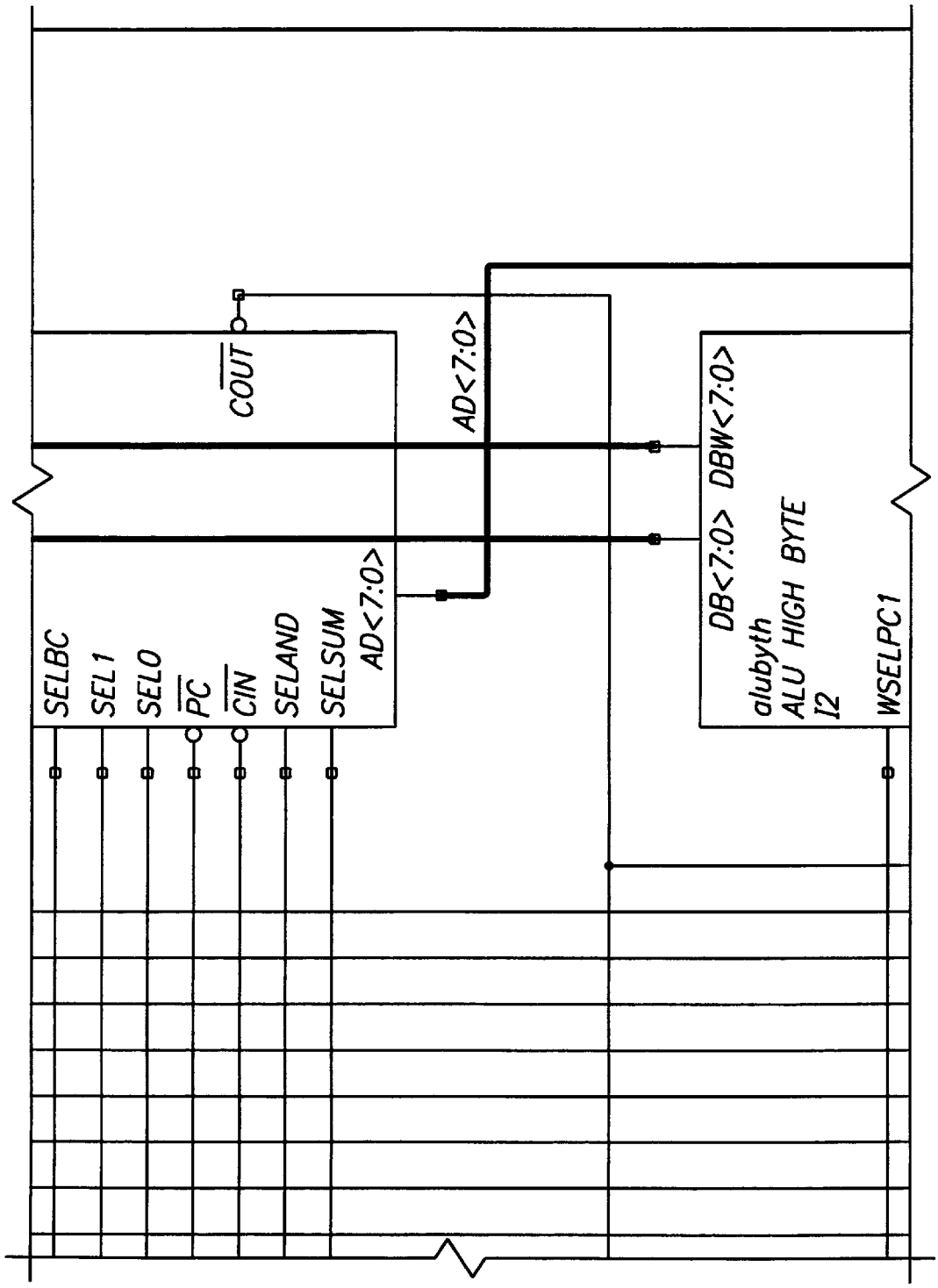

COUT
AD<7:0>
DB<7:0> DBW<7:0>
alubyth
ALU HIGH BYTE
I2
WSELPC1
SELBC
SEL1
SEL0
PC
CIN
SELAND
SELSUM
AD<7:0>

FIG. 7.0540

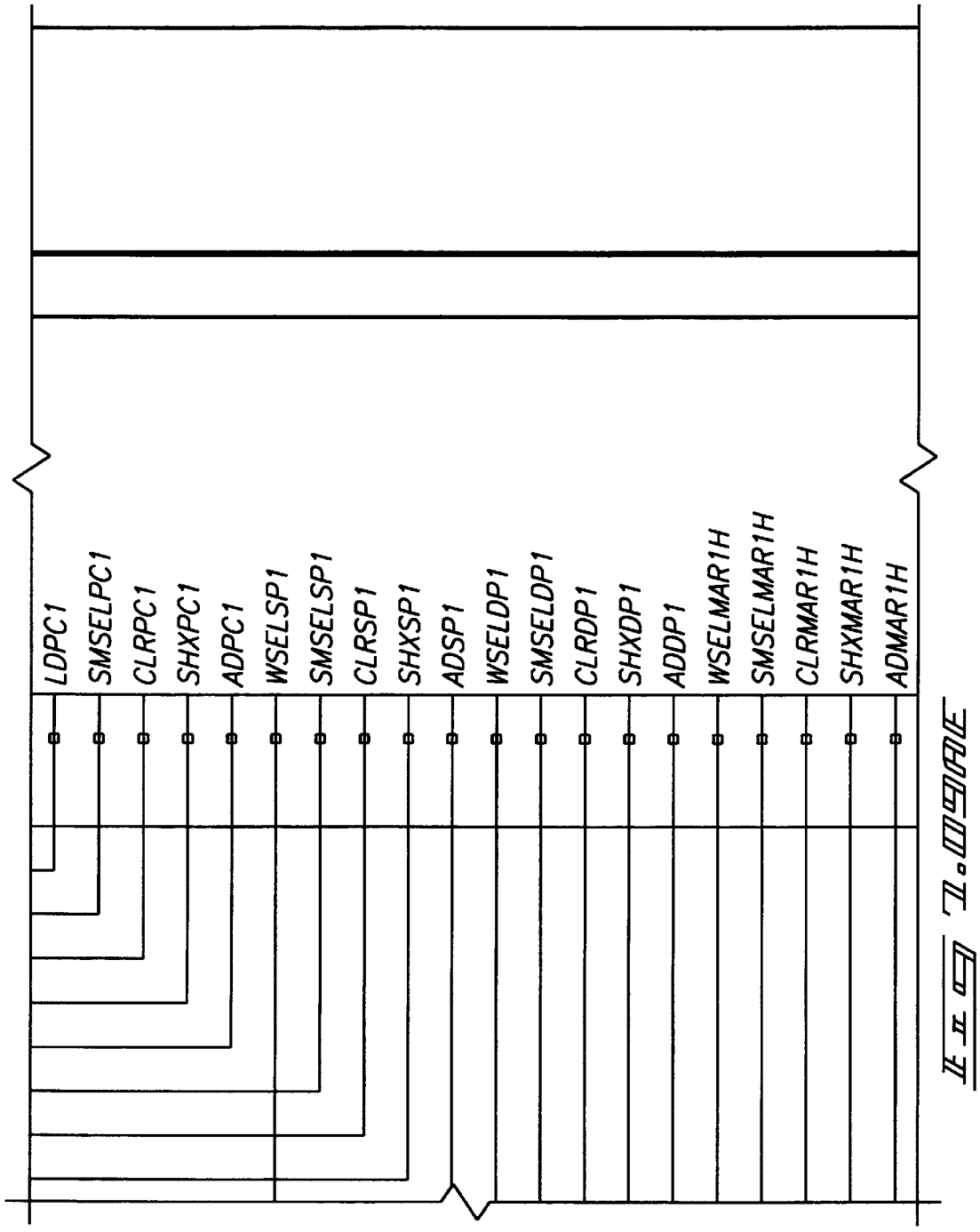

LDPC1
SMSELPC1
CLRPC1
SHXPC1
ADPC1
WSELSP1
SMSELSP1
CLRSP1
SHXSP1
ADSP1
WSELDP1
SMSELDP1
CLRDP1
SHXDP1
ADDP1
WSELMAR1H
SMSELMAR1H
CLRMAR1H
SHXMAR1H
ADMAR1H

FIG. 1,089AE

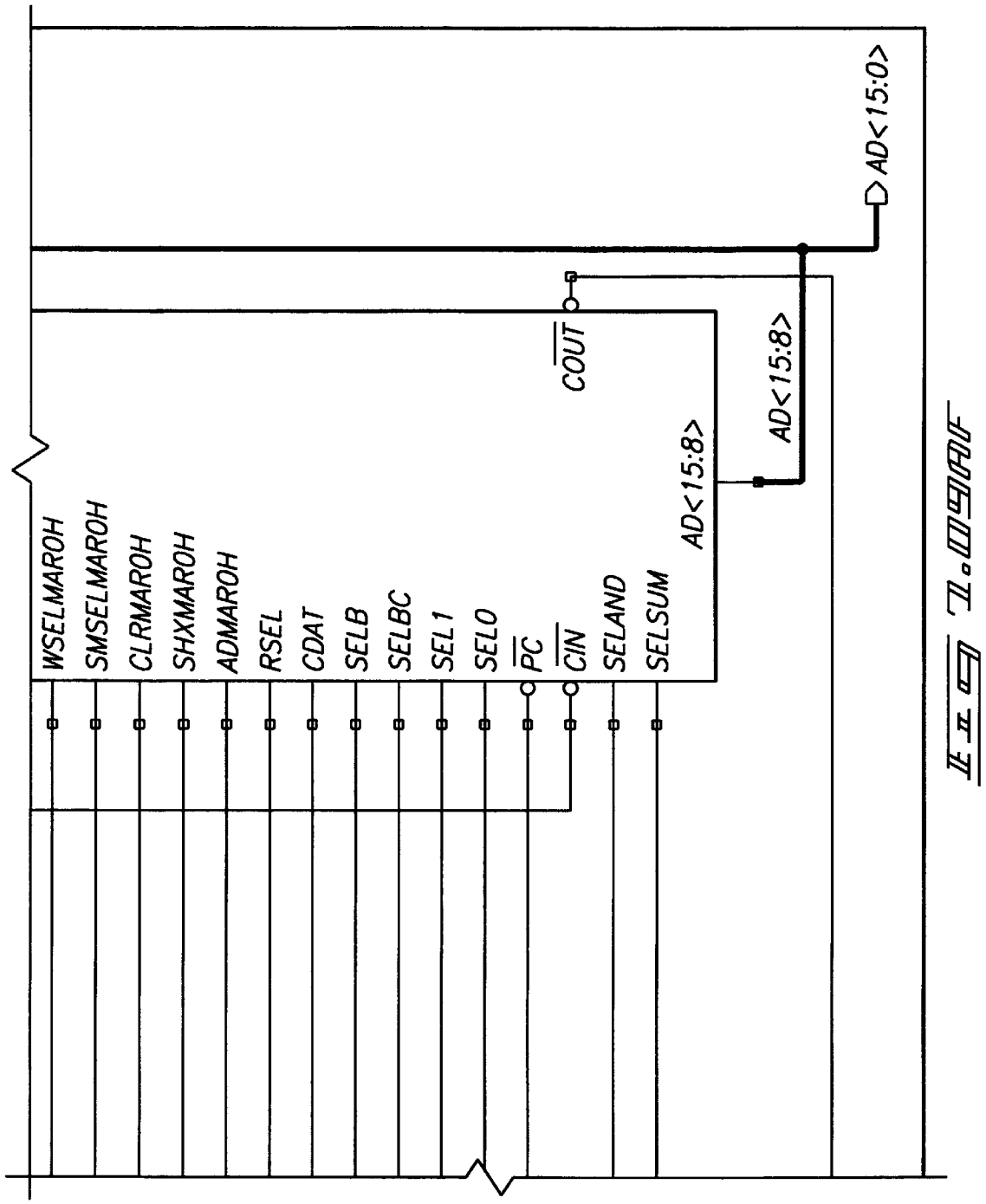

AD<15:0>
COUT
AD<15:8>
AD<15:8>
WSELMAROH
SMSELMAROH
CLRMAROH
SHXMAROH
ADMAROH
RSEL
CDAT
SELB
SELBC
SEL1
SEL0
PC
CIN
SELAND
SELSUM

FIG. 841

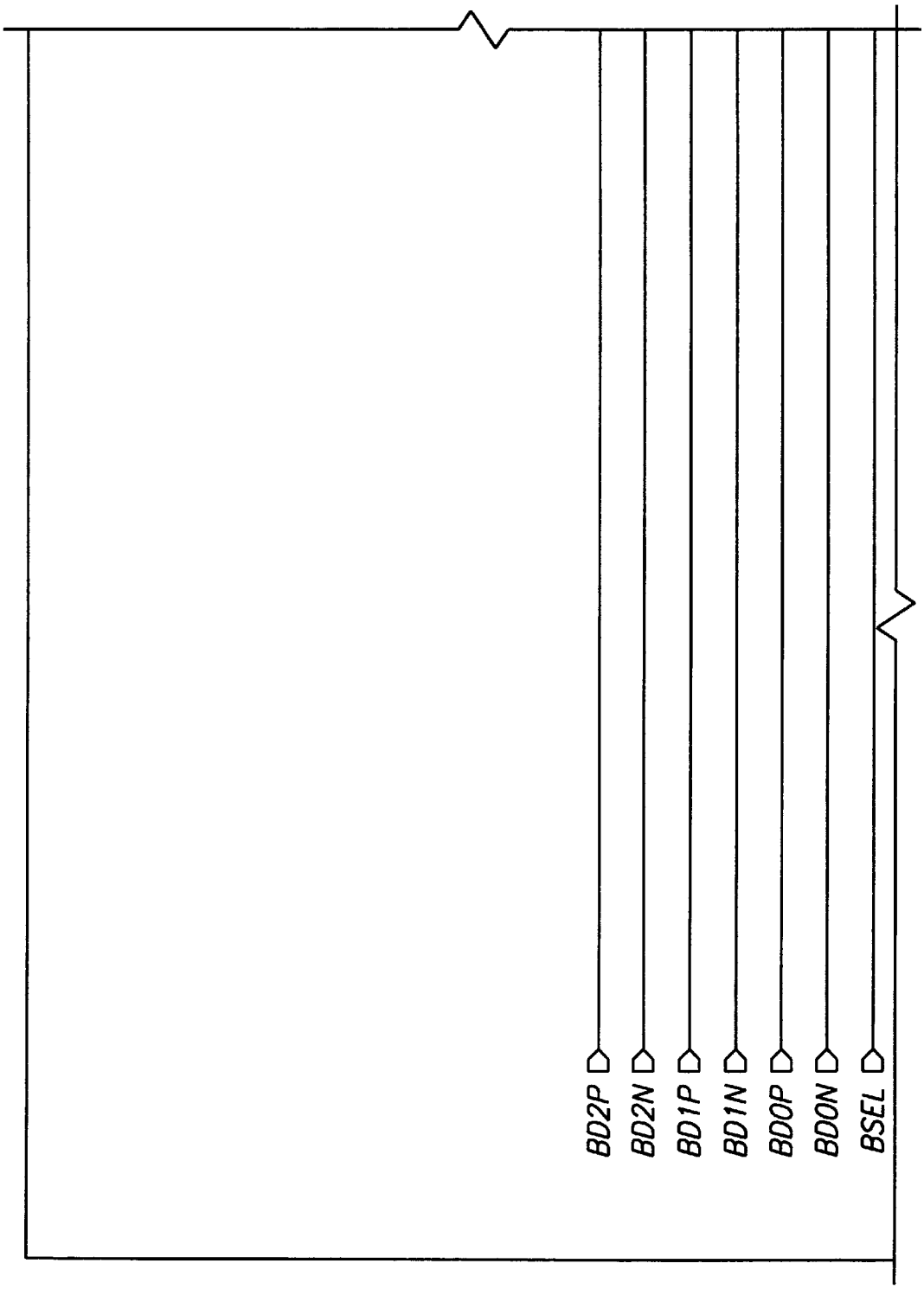


FIG. 6.0568A

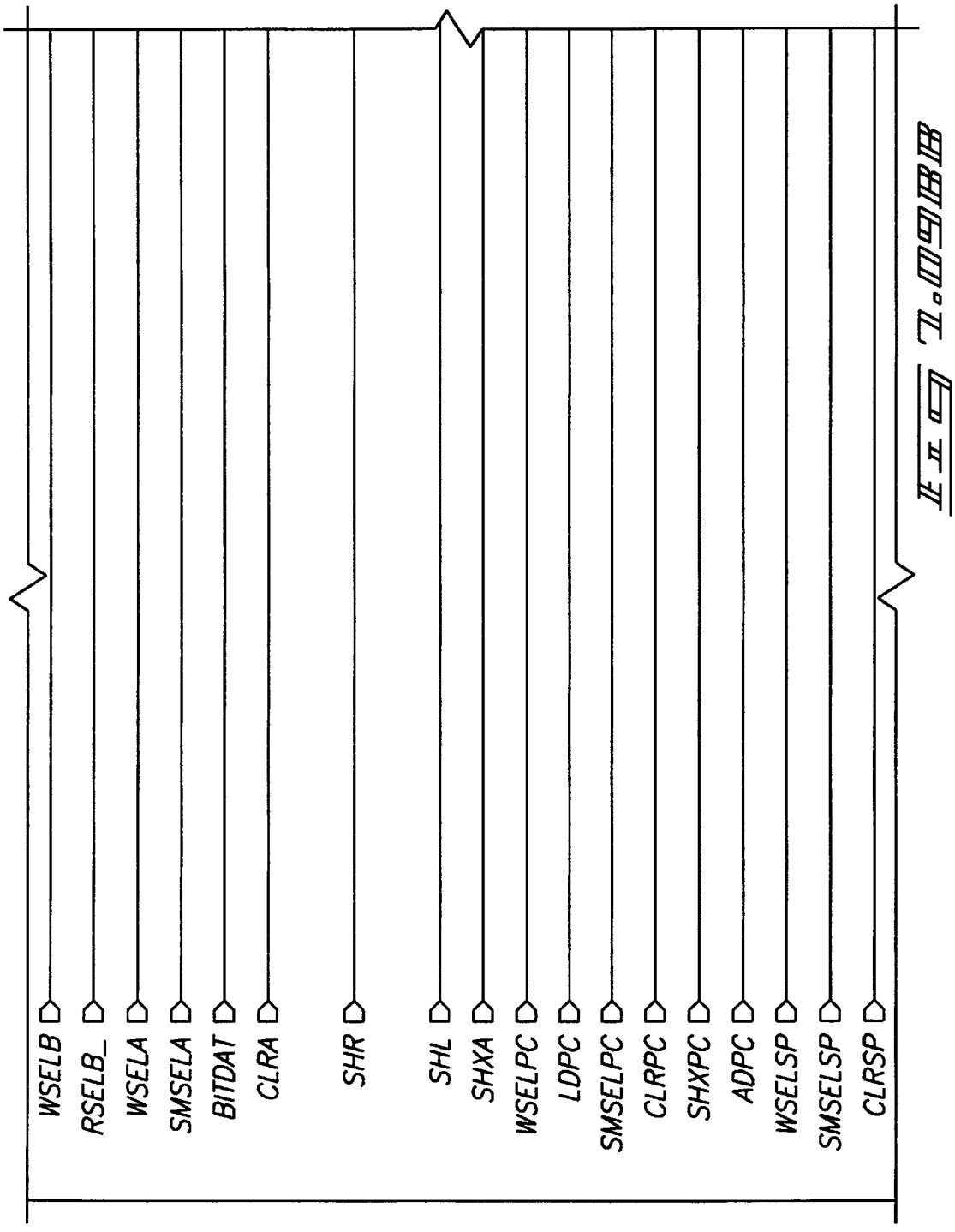

WSELB
RSELB_
WSELA
SMSELA
BITDAT
CLRA
SHR
SHL
SHXA
WSELPC
LDPC
SMSELPC
CLRPC
SHXPC
ADPC
WSELSP
SMSELSP
CLRSP

FIG. 6,130,602

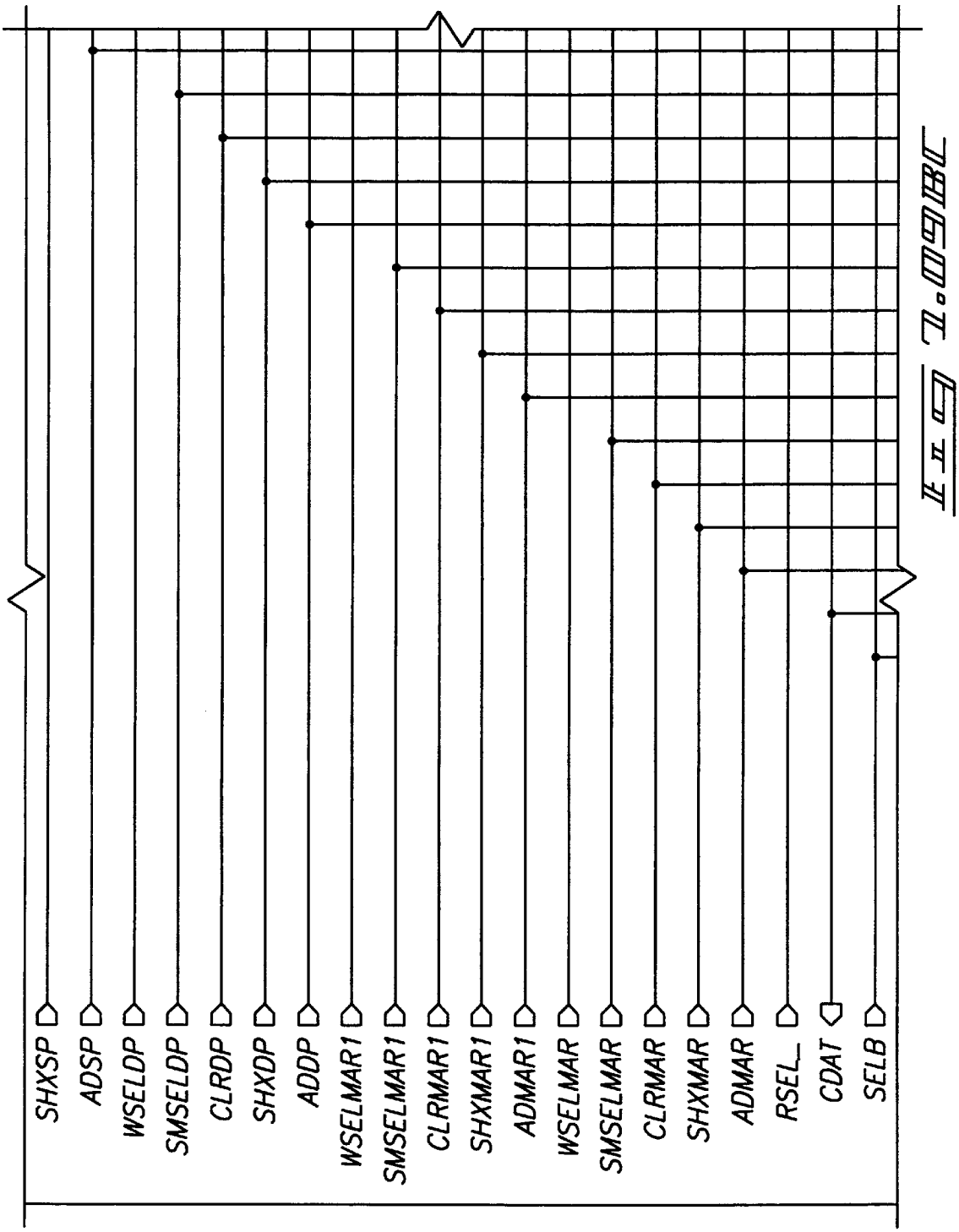

SHXSP
ADSP
WSELDP
SMSELDP
CLRDP
SHXDP
ADDP
WSELMAR1
SMSELMAR1
CLRMAR1
SHXMAR1
ADMAR1
WSELMAR
SMSELMAR
CLRMAR
SHXMAR
ADMAR
RSEL_
CDAT
SELB

FIG. 844.

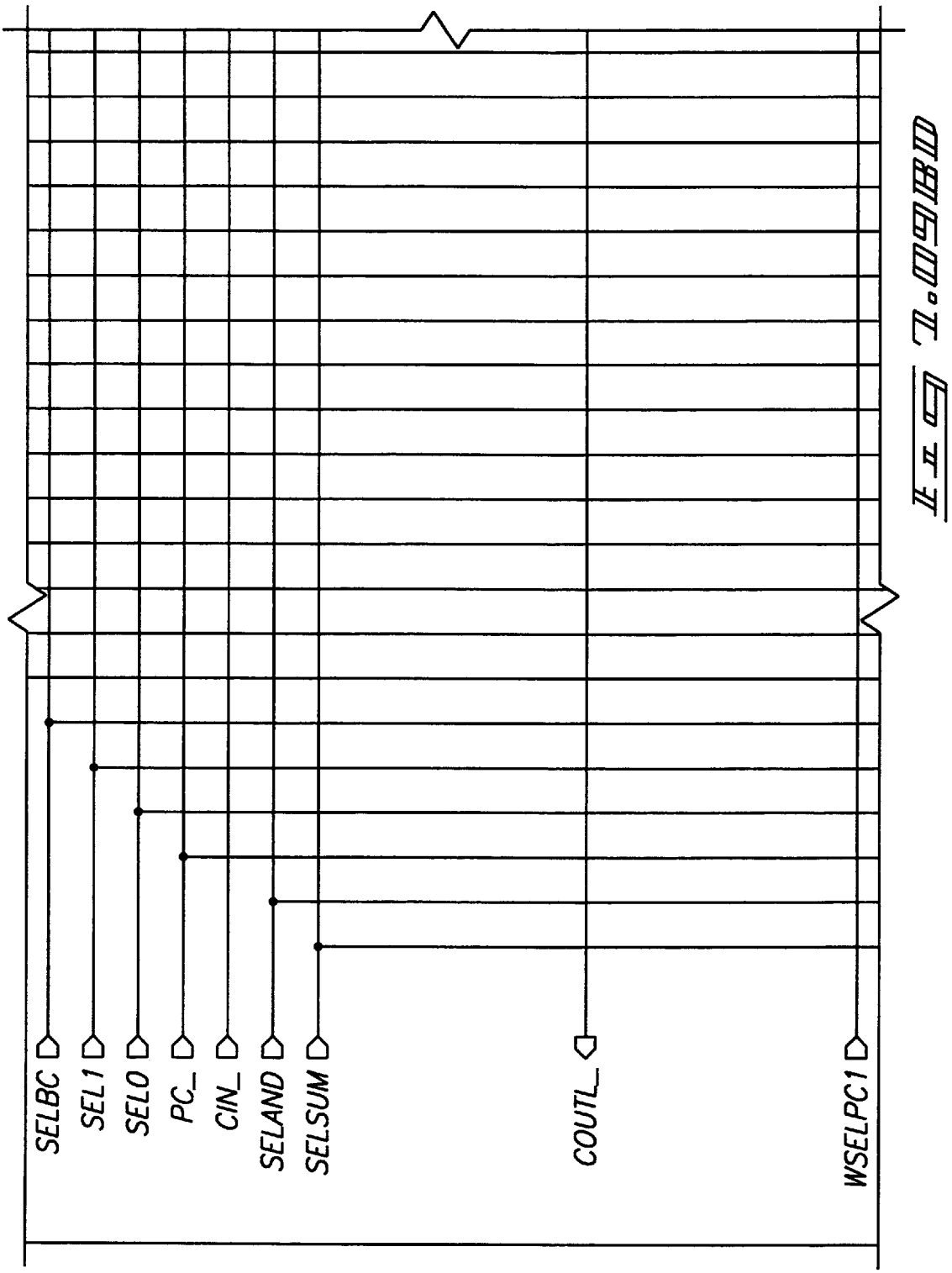


FIG. 845

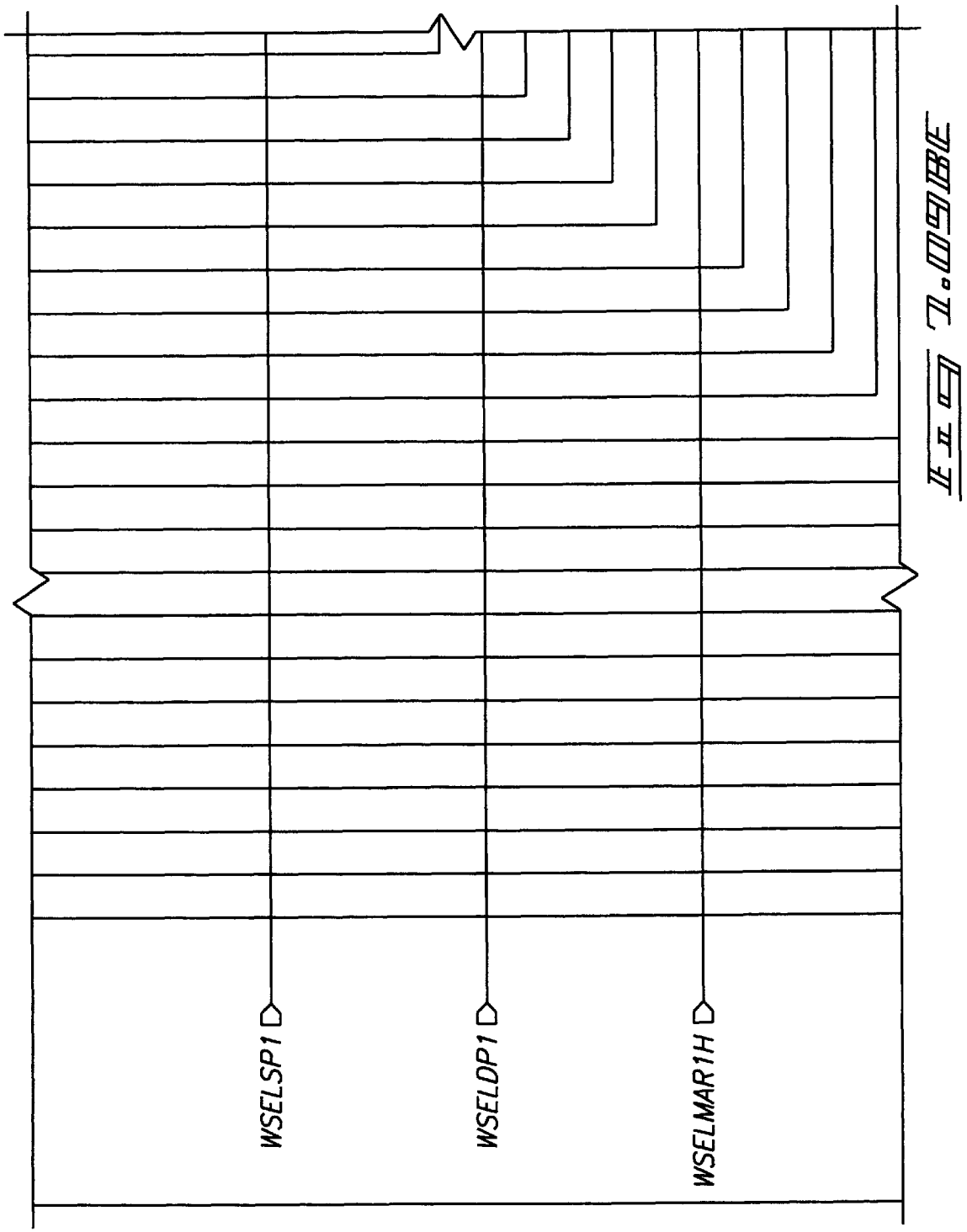
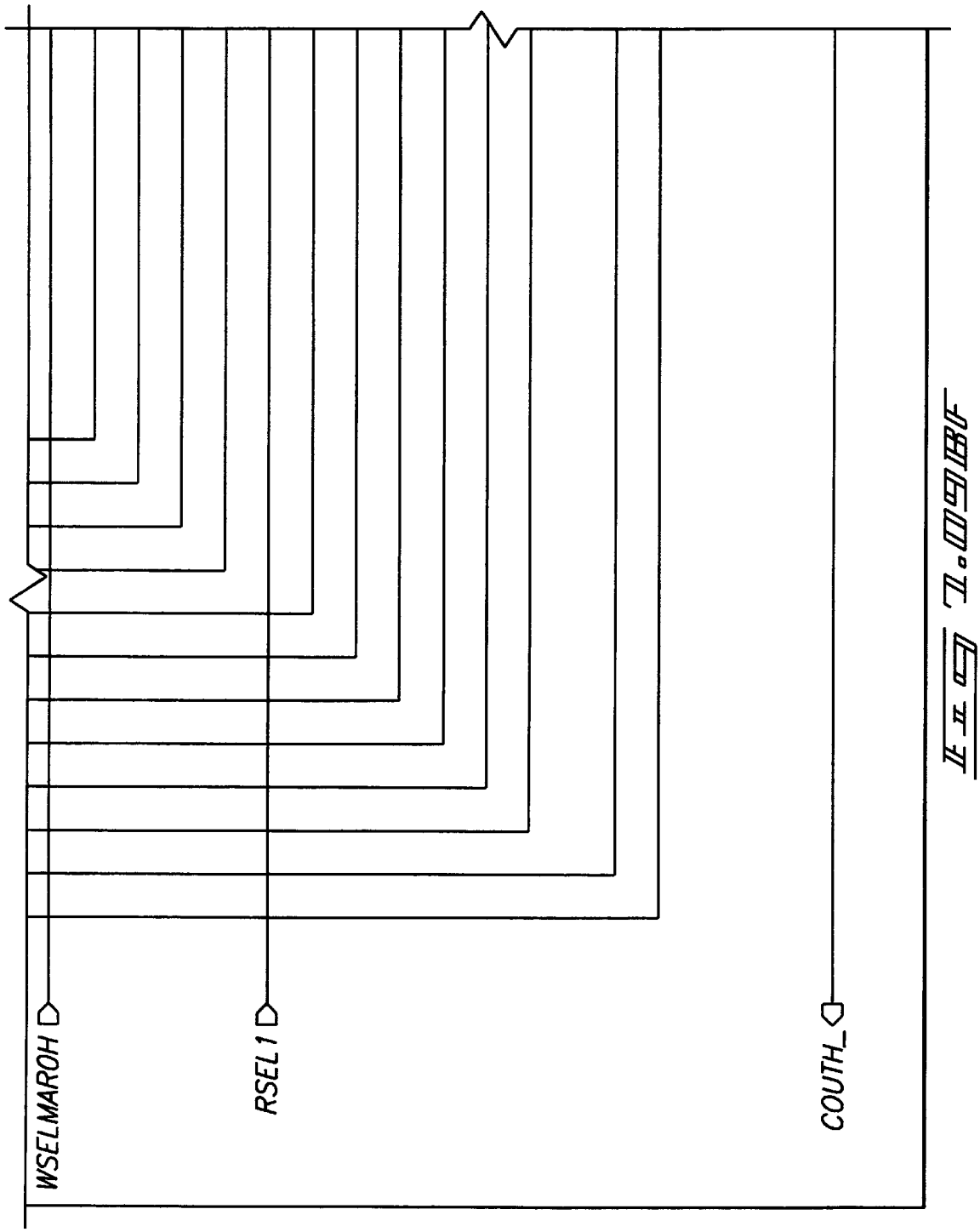


FIG 1.0918E
WSELSP1
WSELOP1
WSELMAR1H


WSELMAROH
RSEL1
COUTH_
FIG 11.0918F

7.0901AE	7.0901BE	7.0901CE
7.0901AD	7.0901BD	7.0901CD
7.0901AC	7.0901BC	7.0901CC
7.0901AB	7.0901BB	7.0901CB
7.0901AA	7.0901BA	7.0901CA

FIG. 7.0901

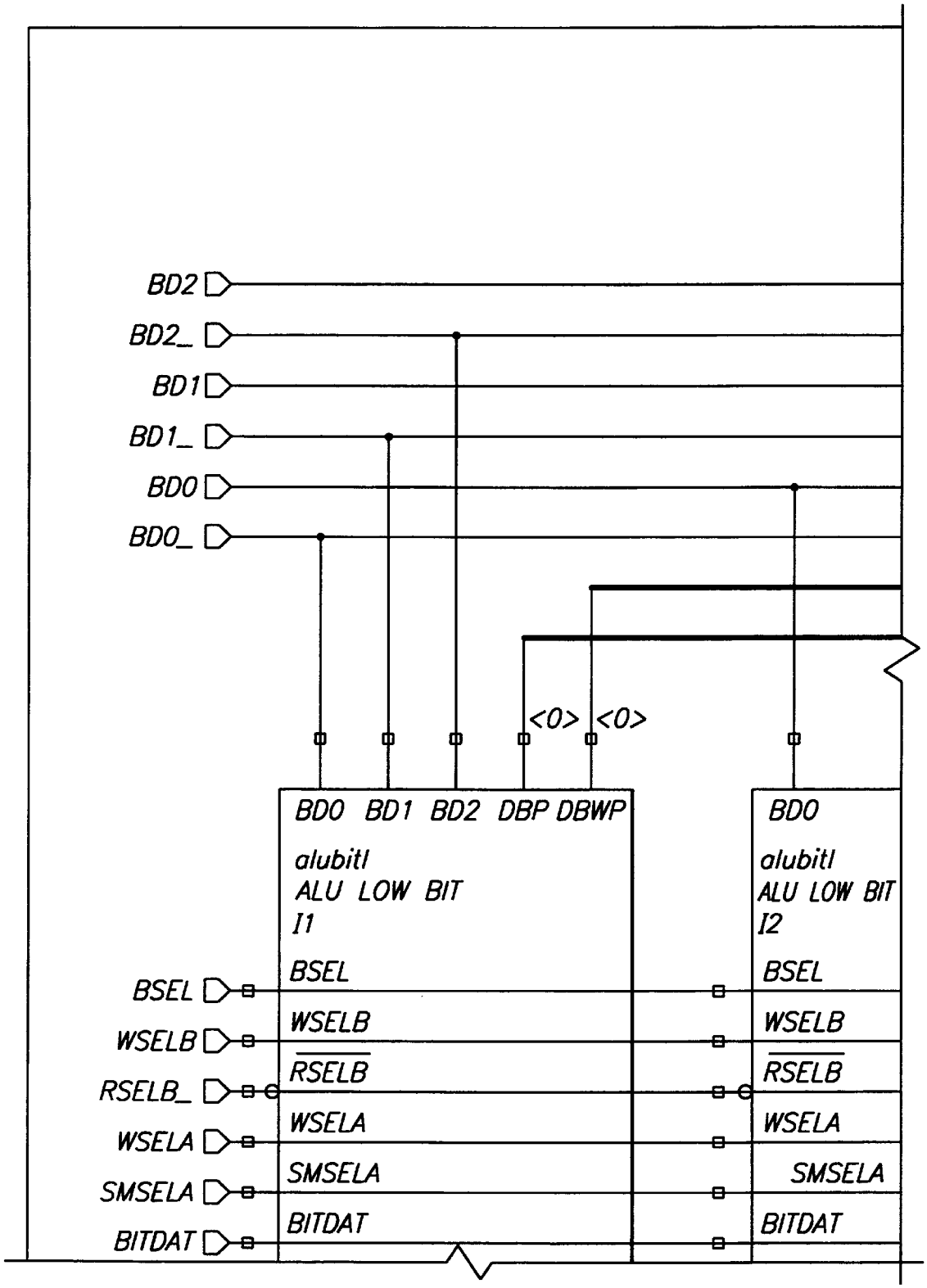

BD2
BD2_
BD1
BD1_
BD0
BD0_
<0>
<0>
BD0 BD1 BD2 DBP DBWP
alubitl
ALU LOW BIT
I1
BD0
alubitl
ALU LOW BIT
I2
BSEL
WSELB
RSELB_
WSELA
SMSELA
BITDAT
BSEL
WSELB
RSELB
WSELA
SMSELA
BITDAT
BSEL
WSELB
RSELB
WSELA
SMSELA
BITDAT

Fig 1.090.1AA

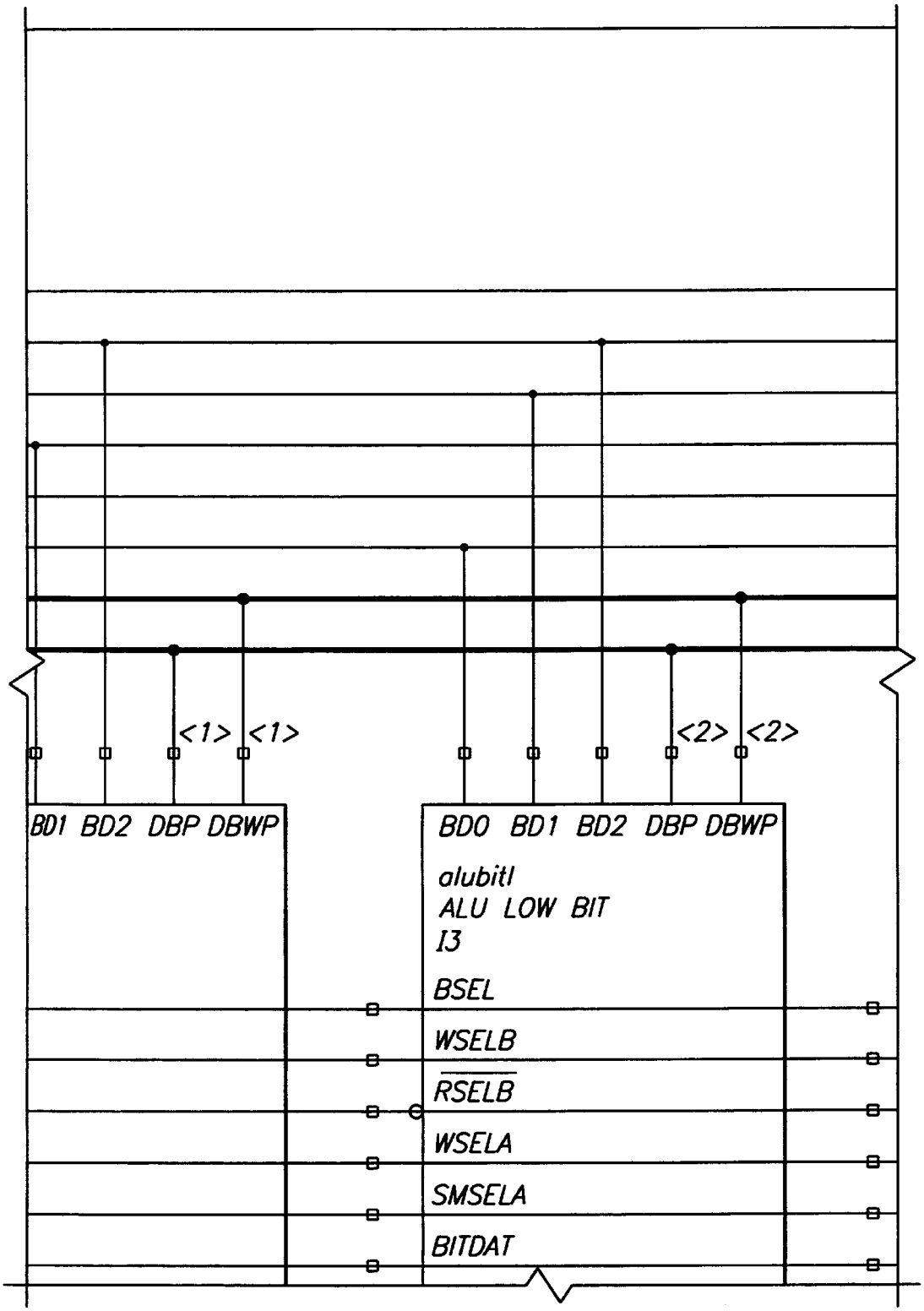


Fig 7.09010AB

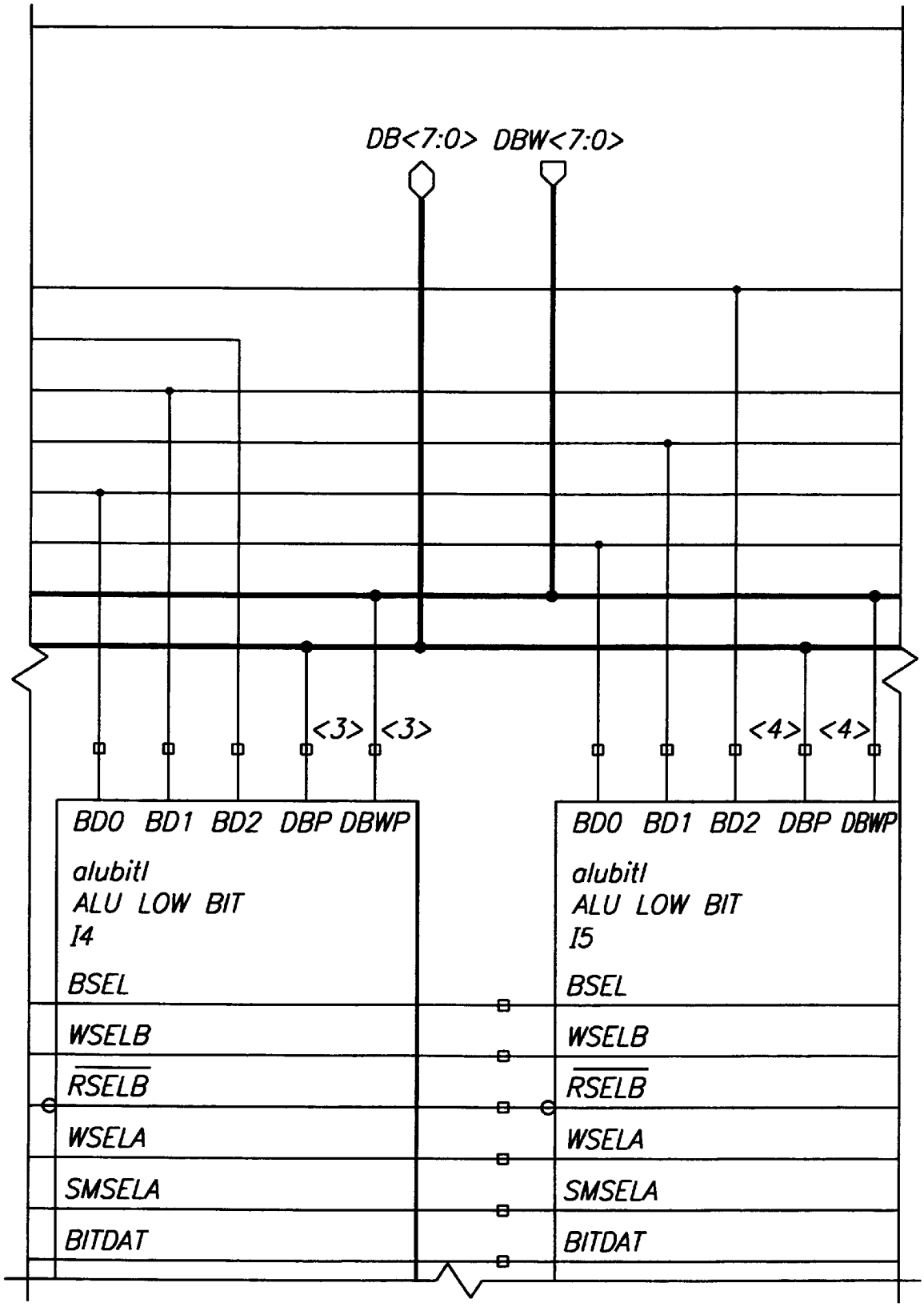

DB<7:0> DBW<7:0>
<3> <3>
<4> <4>
BD0 BD1 BD2 DBP DBWP
alubitl
ALU LOW BIT
I4
BSEL
WSELB
RSELB
WSELA
SMSELA
BITDAT
BD0 BD1 BD2 DBP DBWP
alubitl
ALU LOW BIT
I5
BSEL
WSELB
RSELB
WSELA
SMSELA
BITDAT

Fig 1.0901AC

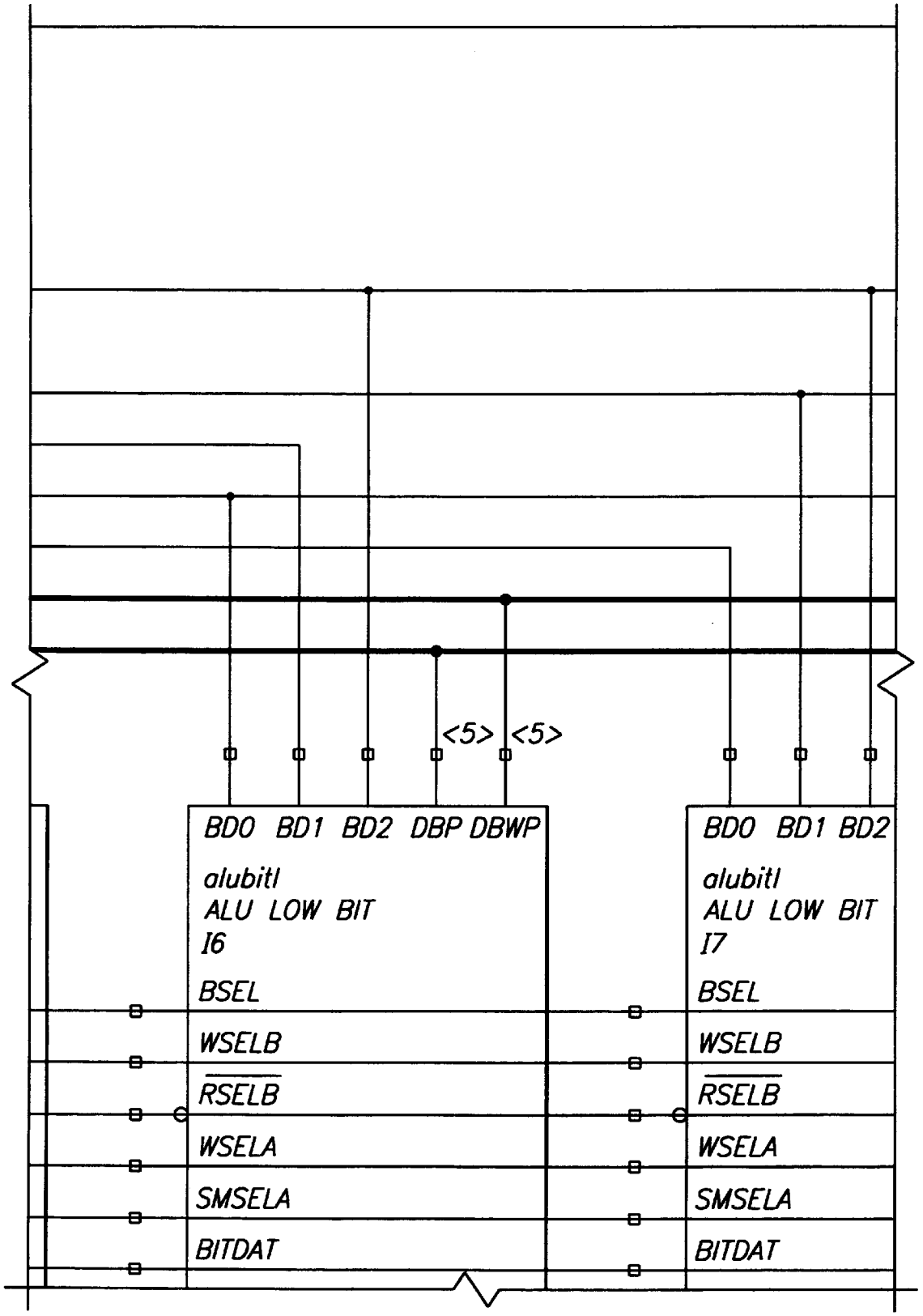


Fig 1.09010AD

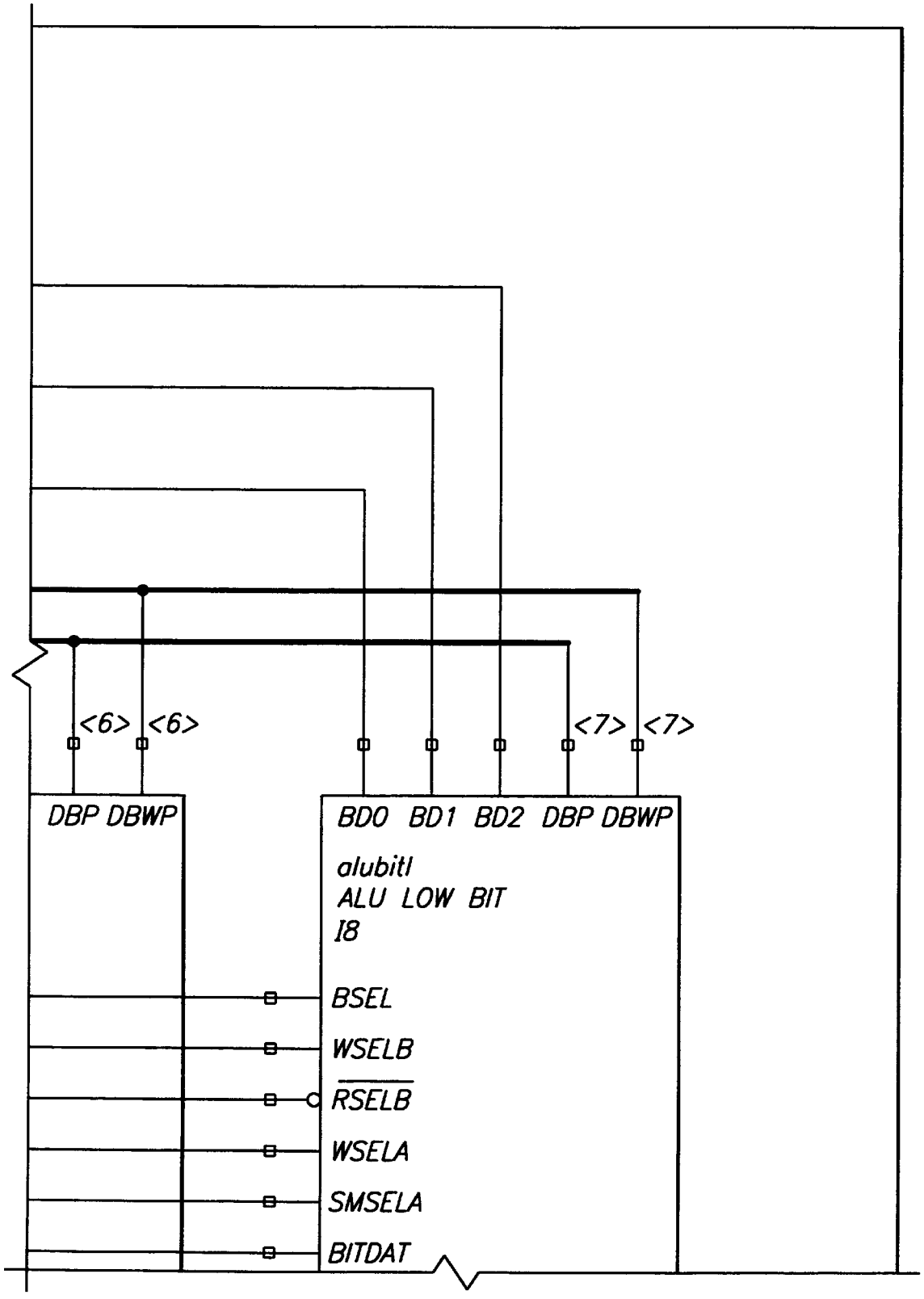

<6>
<6>
<7>
<7>
DBP DBWP
BD0 BD1 BD2 DBP DBWP
alubitl
ALU LOW BIT
I8
BSEL
WSELB
RSELB
WSELA
SMSELA
BITDAT

Fig 1.0901AE

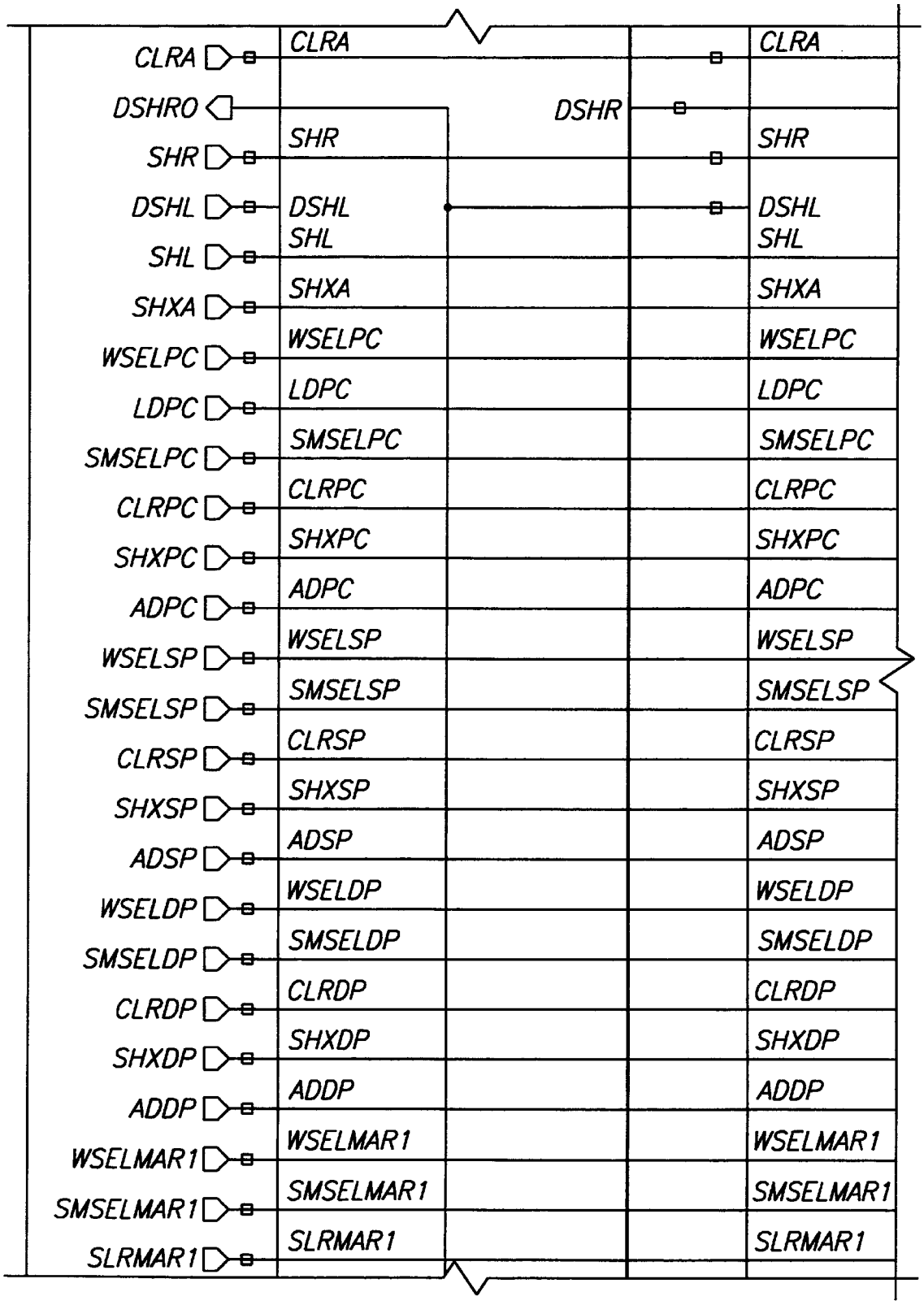

CLRA
DSHRO
SHR
DSHL
SHL
SHXA
WSELPC
LDPC
SMSELPC
CLRPC
SHXPC
ADPC
WSELSP
SMSELSP
CLRSP
SHXSP
ADSP
WSELDP
SMSELDP
CLRDP
SHXDP
ADDP
WSELMAR1
SMSELMAR1
SLRMAR1
DSHR

Fig 1.0901BA

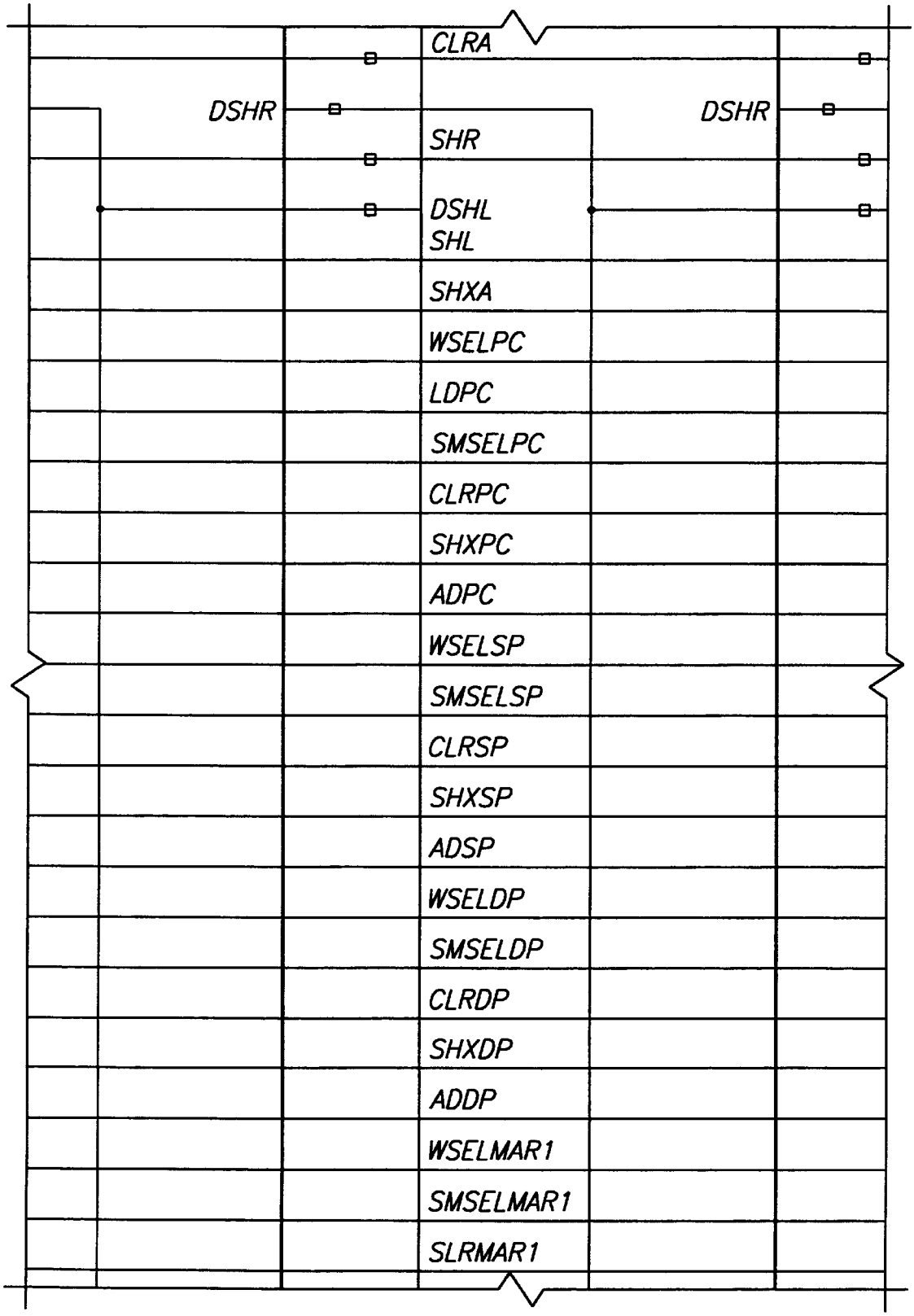


Fig 1.0900188

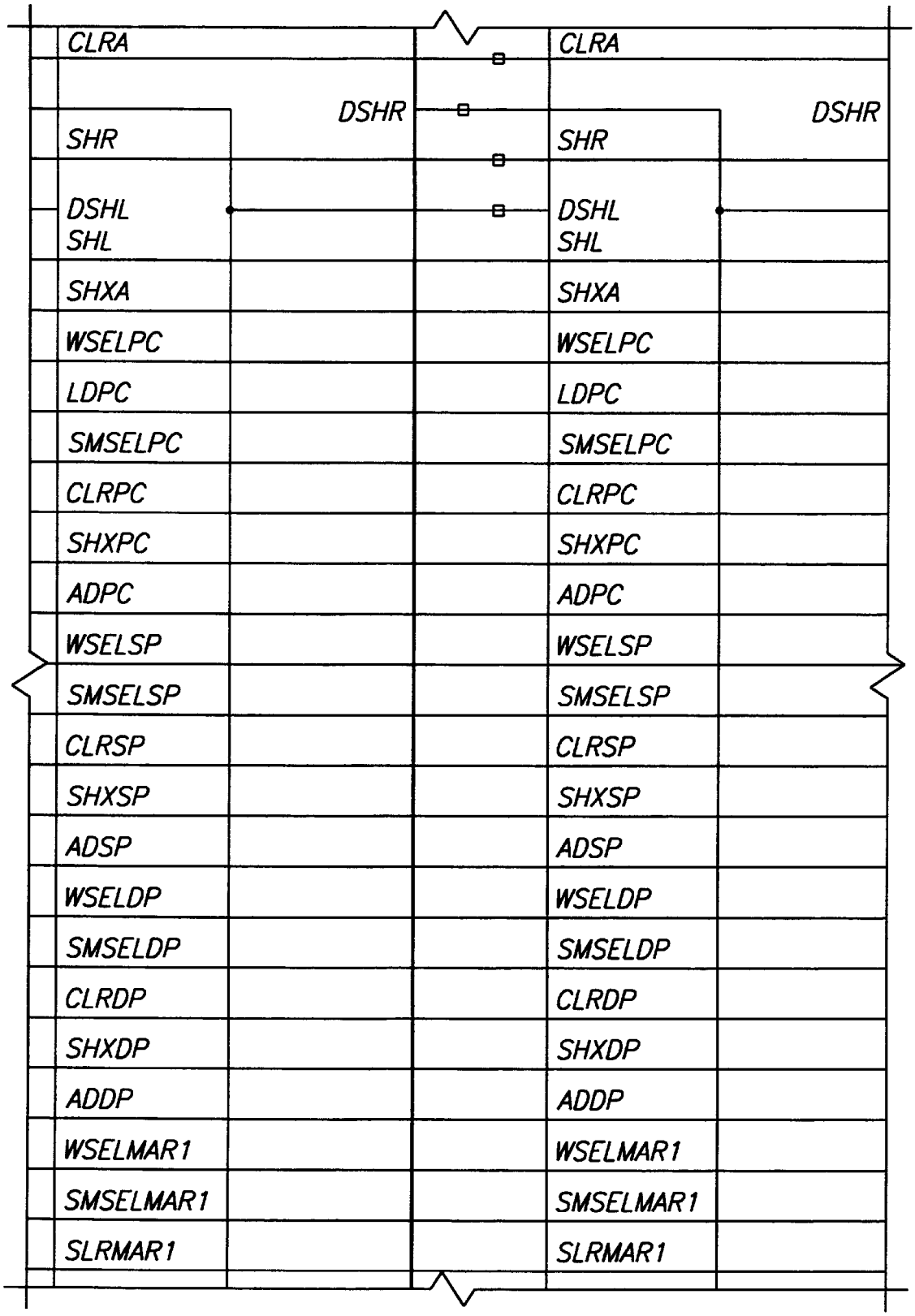


Fig 1.09001BC

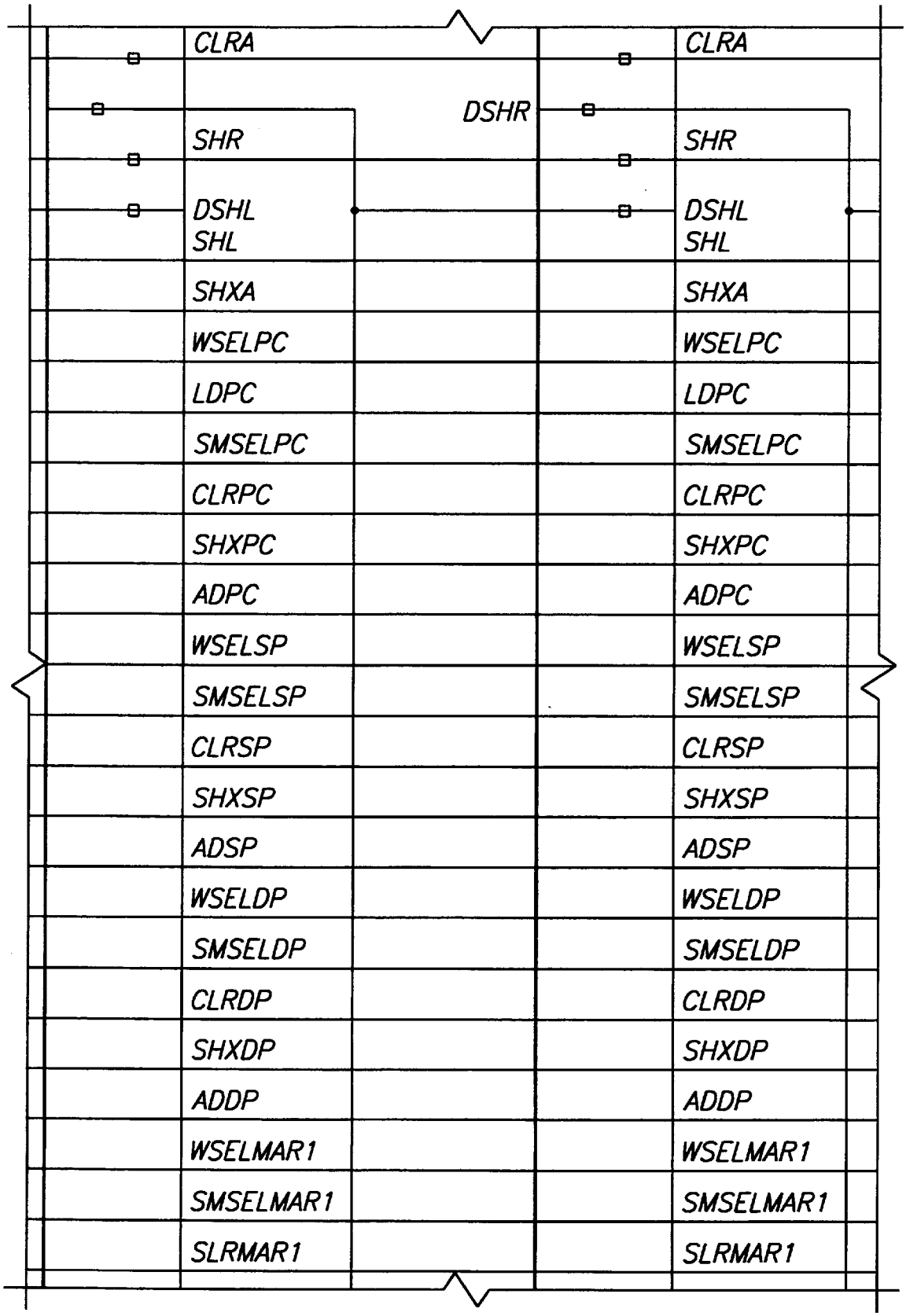

CLRA
DSHR
SHR
DSHL
SHL
SHXA
WSELPC
LDPC
SMSELPC
CLRPC
SHXPC
ADPC
WSELSP
SMSELSP
CLRSP
SHXSP
ADSP
WSELDP
SMSELDP
CLRDP
SHXDP
ADDP
WSELMAR1
SMSELMAR1
SLRMAR1
CLRA
SHR
DSHL
SHL
SHXA
WSELPC
LDPC
SMSELPC
CLRPC
SHXPC
ADPC
WSELSP
SMSELSP
CLRSP
SHXSP
ADSP
WSELDP
SMSELDP
CLRDP
SHXDP
ADDP
WSELMAR1
SMSELMAR1
SLRMAR1

Fig 1.0901BD

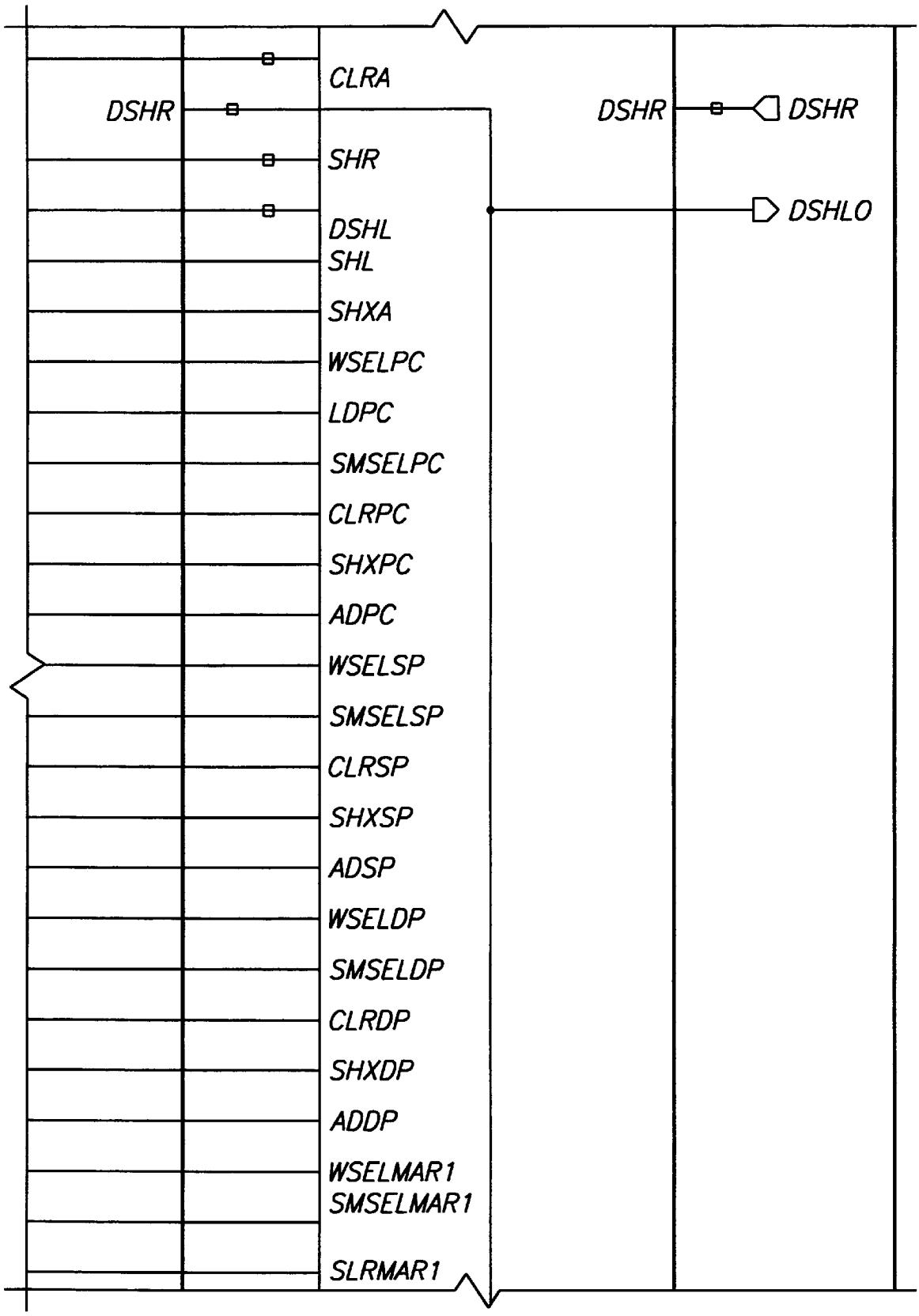

CLRA
DSHR
DSHR
DSHR
SHR
DSHLO
DSHL
SHL
SHXA
WSELPC
LDPC
SMSELPC
CLRPC
SHXPC
ADPC
WSELSP
SMSELSP
CLRSP
SHXSP
ADSP
WSELDP
SMSELDP
CLRDP
SHXDP
ADDP
WSELMAR1
SMSELMAR1
SLRMAR1

Fig 1.09018E

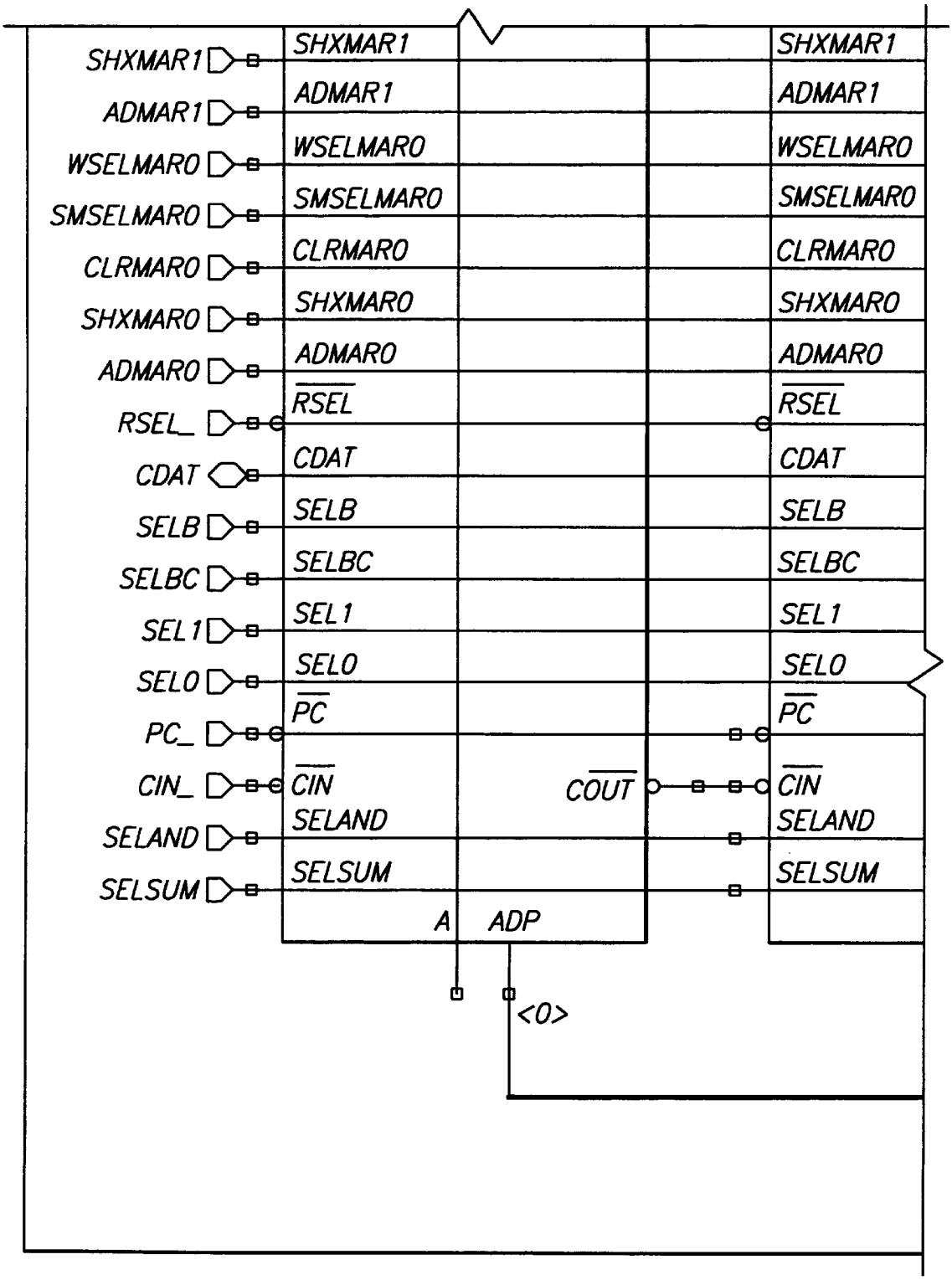

SHXMAR1
ADMAR1
WSELMARO
SMSELMARO
CLRMARO
SHXMARO
ADMARO
RSEL_
CDAT
SELB
SELBC
SEL1
SELO
PC_
CIN_
SELAND
SELSUM
SHXMAR1
ADMAR1
WSELMARO
SMSELMARO
CLRMARO
SHXMARO
ADMARO
RSEL
CDAT
SELB
SELBC
SEL1
SELO
PC
CIN
SELAND
SELSUM
A
ADP
COUT
<0>
SHXMAR1
ADMAR1
WSELMARO
SMSELMARO
CLRMARO
SHXMARO
ADMARO
RSEL
CDAT
SELB
SELBC
SEL1
SELO
PC
CIN
SELAND
SELSUM

Fig 1.090ICA

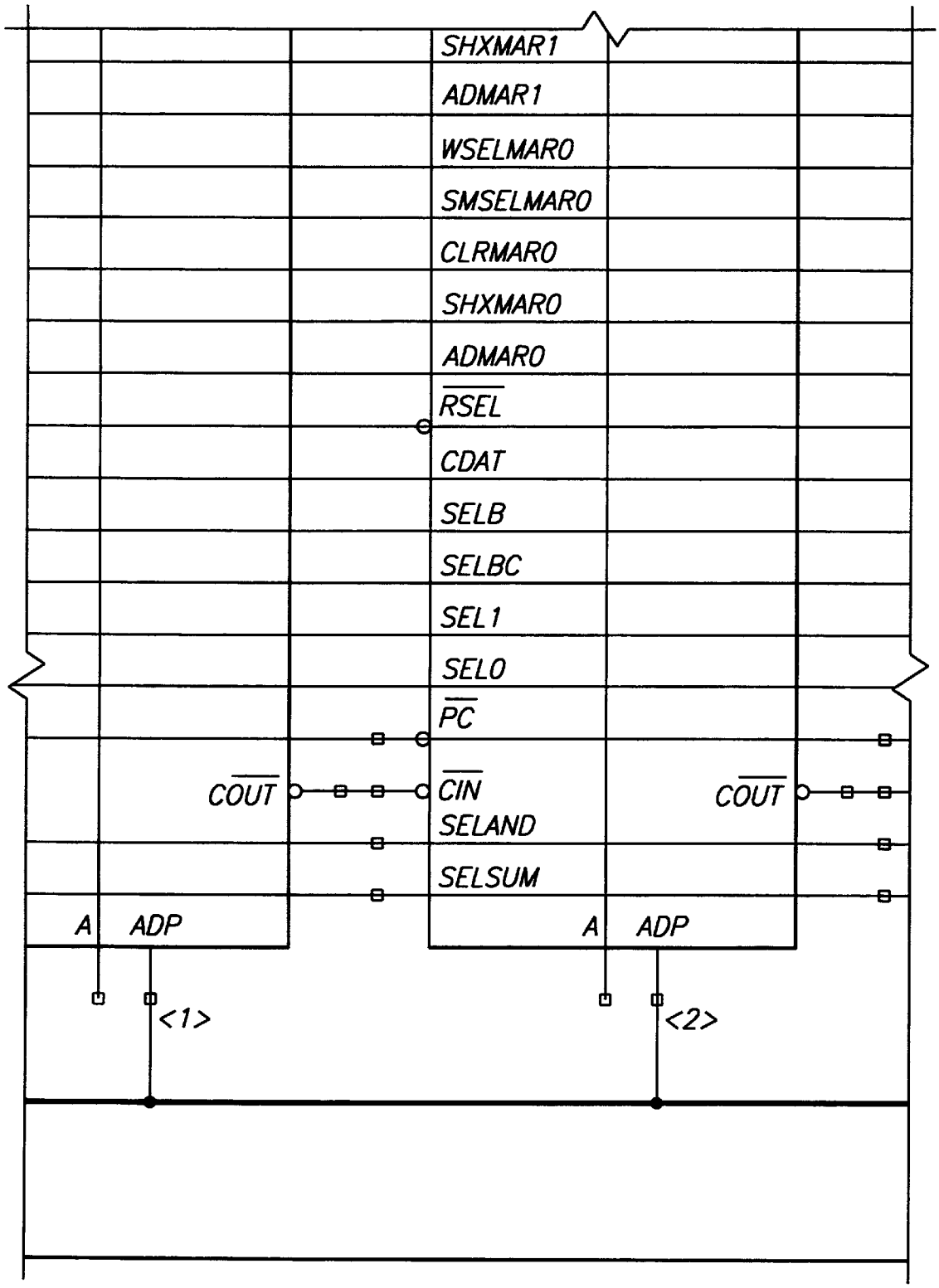

SHXMAR1
ADMAR1
WSELMAR0
SMSELMAR0
CLRMAR0
SHXMAR0
ADMAR0
RSEL
CDAT
SELB
SELBC
SEL1
SEL0
PC
COUT
CIN
SELAND
SELSUM
A
ADP
<1>
A
ADP
<2>
COUT

Fig 1.090ICB

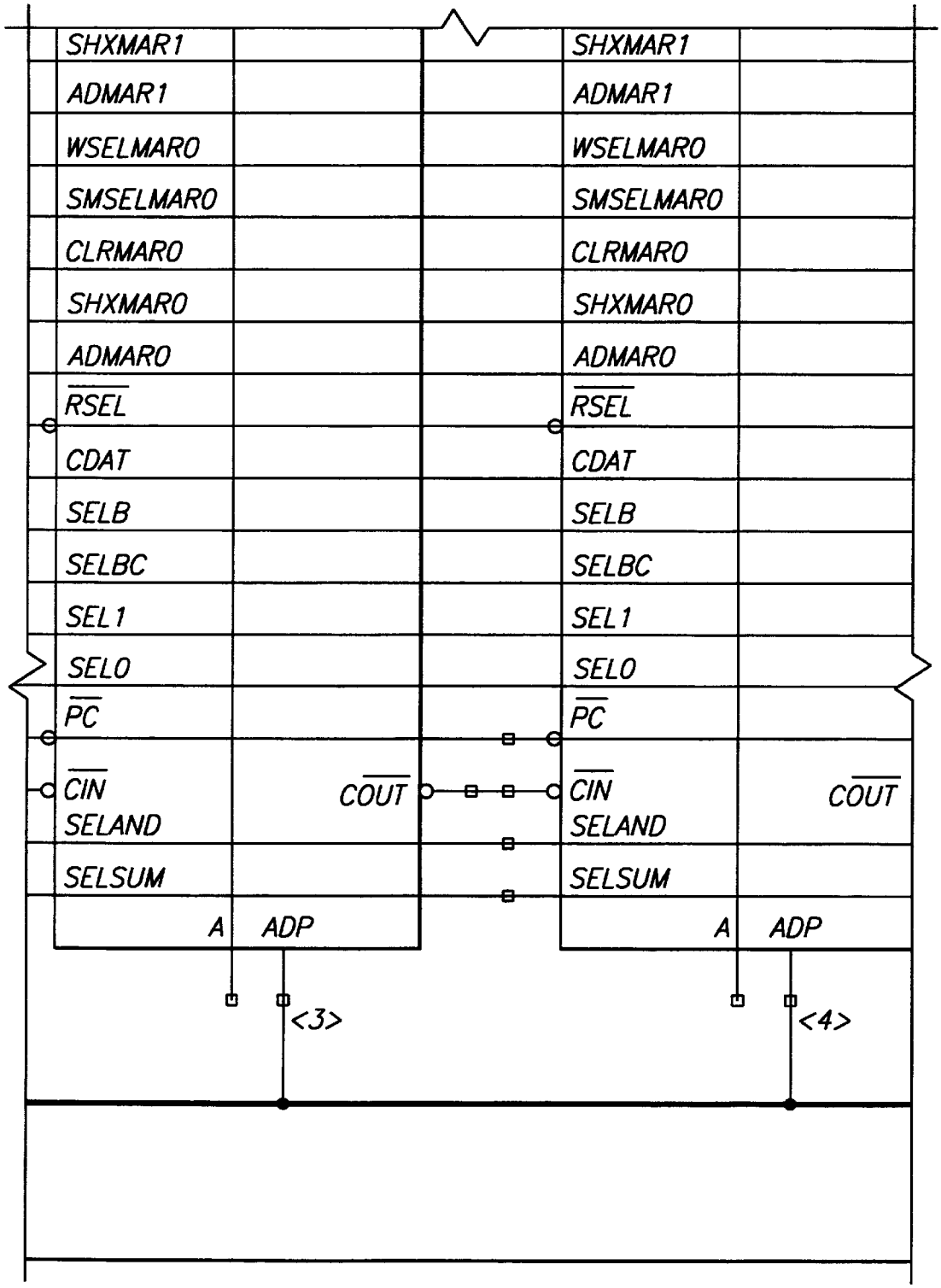

SHXMAR1
ADMAR1
WSELMARO
SMSELMARO
CLRMARO
SHXMARO
ADMARO
RSEL
CDAT
SELB
SELBC
SEL1
SELO
PC
CIN
SELAND
COUT
SELSUM
A
ADP
<3>
SHXMAR1
ADMAR1
WSELMARO
SMSELMARO
CLRMARO
SHXMARO
ADMARO
RSEL
CDAT
SELB
SELBC
SEL1
SELO
PC
CIN
SELAND
COUT
SELSUM
A
ADP
<4>

Fig 1.090116

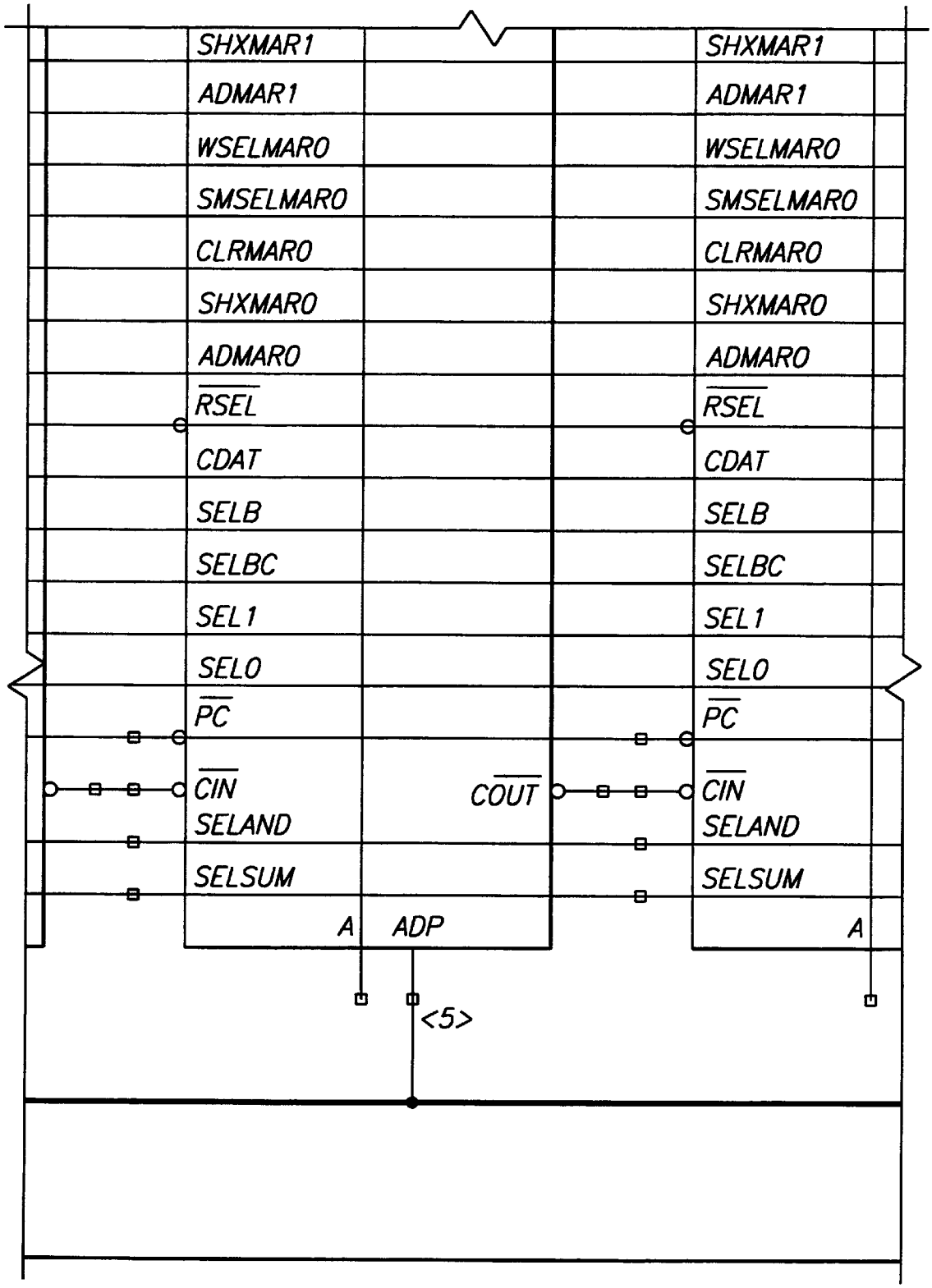

SHXMAR1
ADMAR1
WSELMARO
SMSELMARO
CLRMARO
SHXMARO
ADMARO
RSEL
CDAT
SELB
SELBC
SEL1
SELO
PC
CIN
SELAND
SELSUM
A
ADP
COUT
<5>
SHXMAR1
ADMAR1
WSELMARO
SMSELMARO
CLRMARO
SHXMARO
ADMARO
RSEL
CDAT
SELB
SELBC
SEL1
SELO
PC
CIN
SELAND
SELSUM
A

Fig 1.090ICD

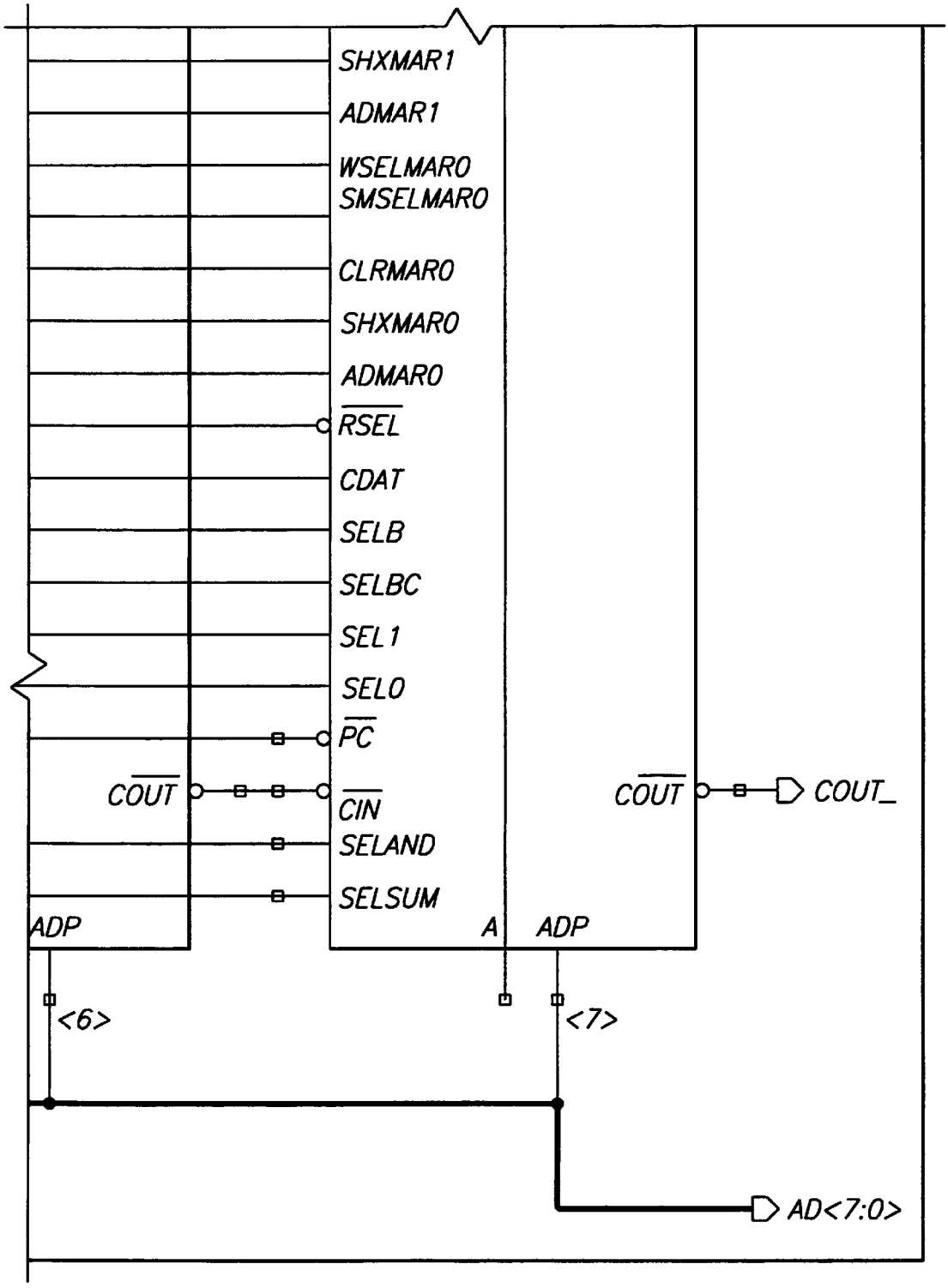

SHXMAR1
ADMAR1
WSELMAR0
SMSELMAR0
CLRMAR0
SHXMAR0
ADMAR0
RSEL
CDAT
SELB
SELBC
SEL1
SEL0
PC
COUT
CIN
SELAND
SELSUM
ADP
A
ADP
COUT
COUT_
<6>
<7>
AD<7:0>

Fig 1.09011E

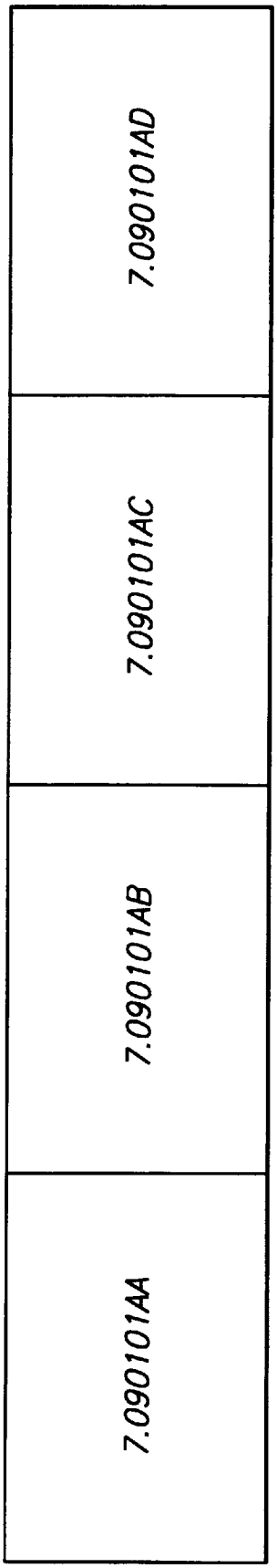


FIG. 7.090101

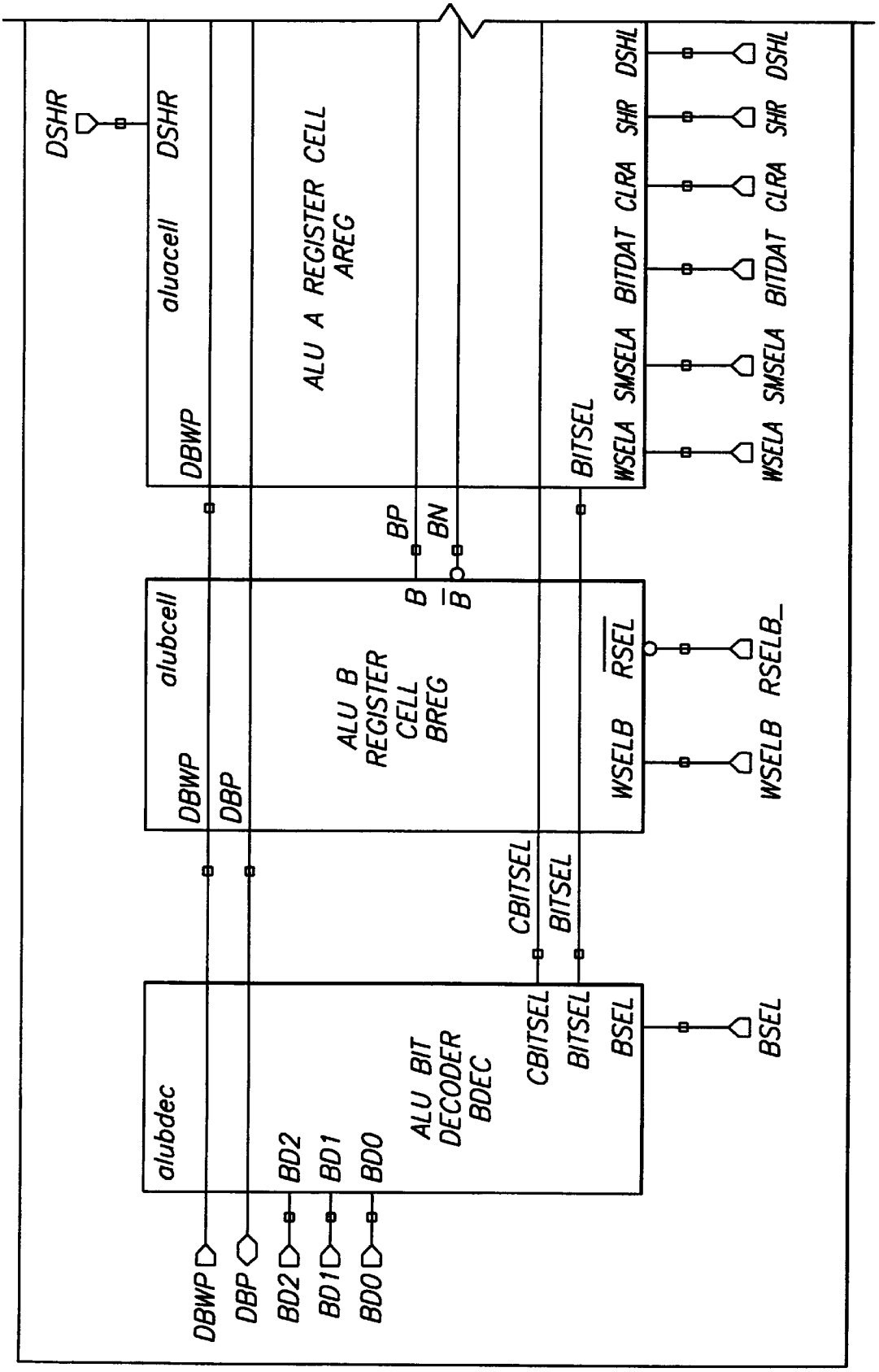
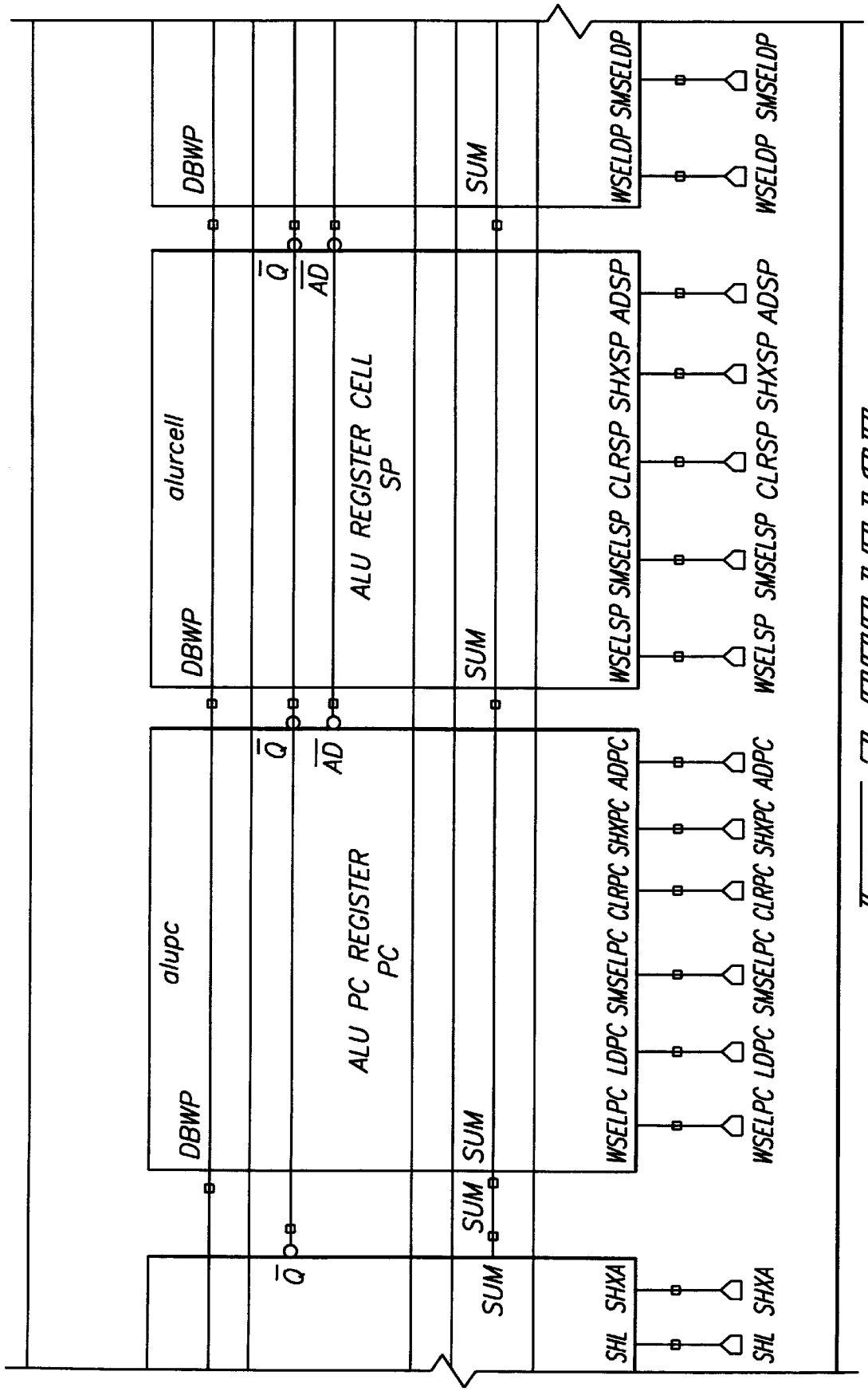


FIG 7.09011AA


DBWP
alupc
ALU PC REGISTER
PC
SUM
WSELPC LDPC SMSELPC CLRPC SHXPC ADPC
SHL SHXA
alurcell
ALU REGISTER CELL
SP
WSELSP SMSELSP CLRSP SHXSP ADSP
WSELDP SMSELDP

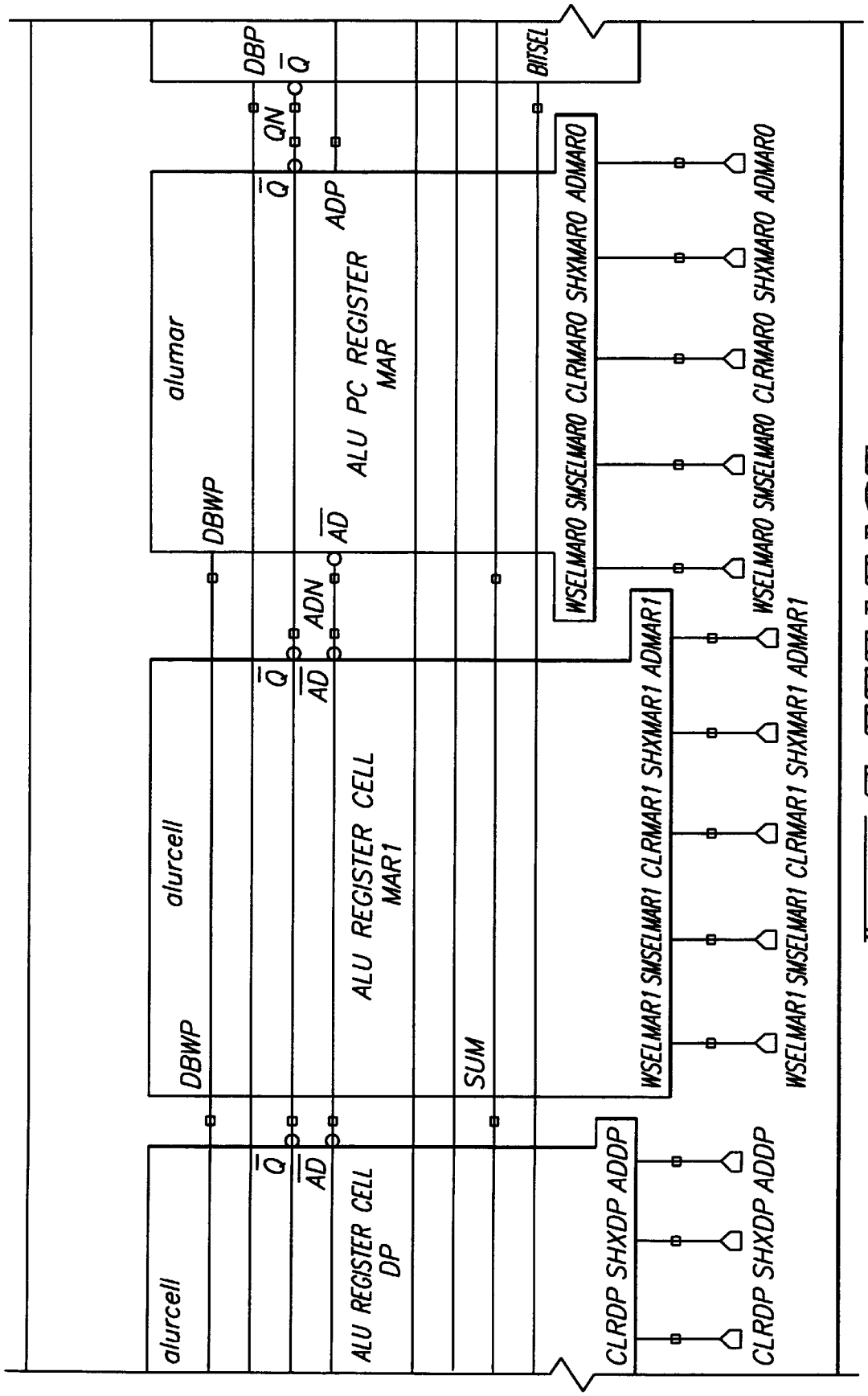


FIG. 6.0001.AAC

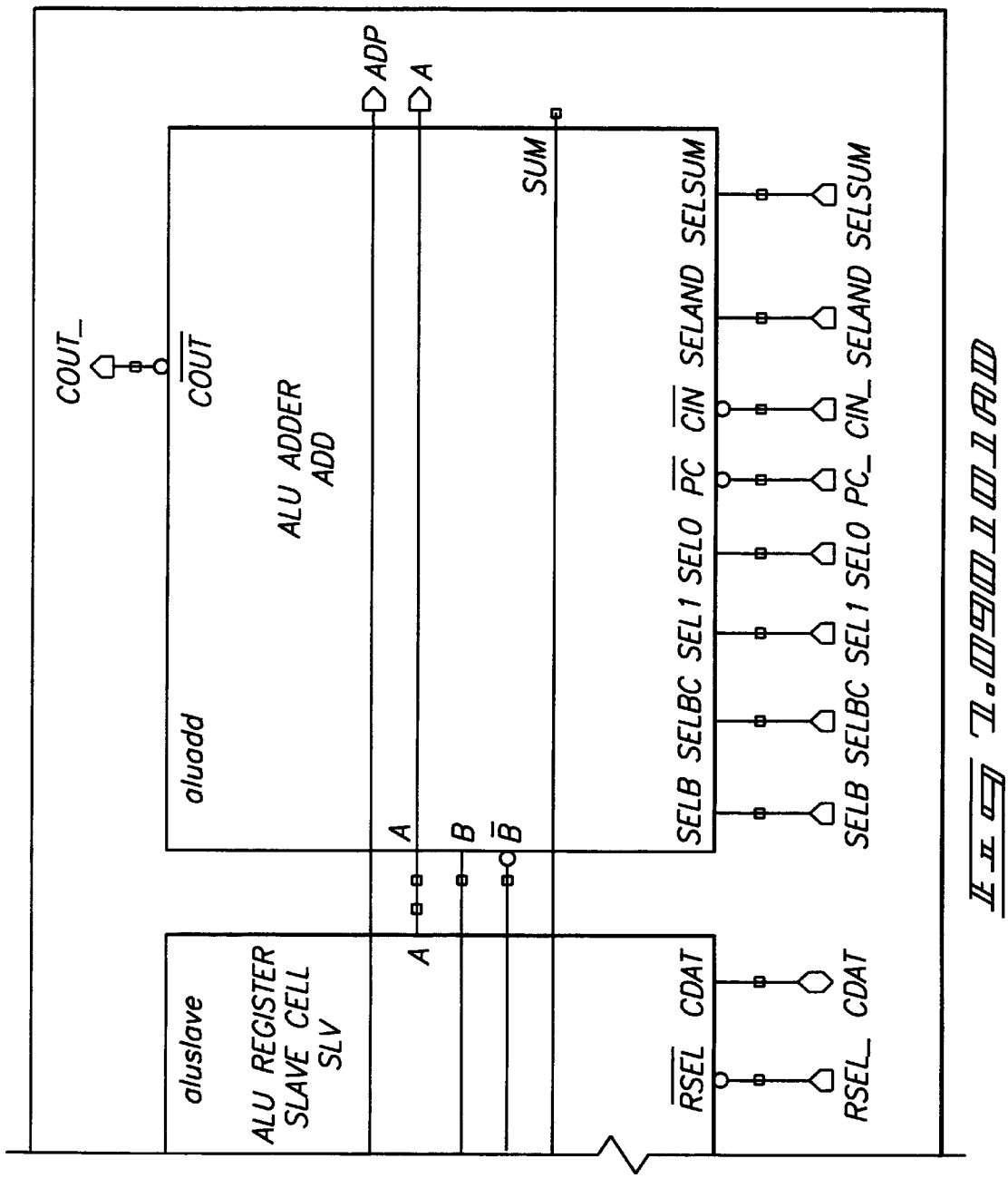


FIG. 11.0901AM

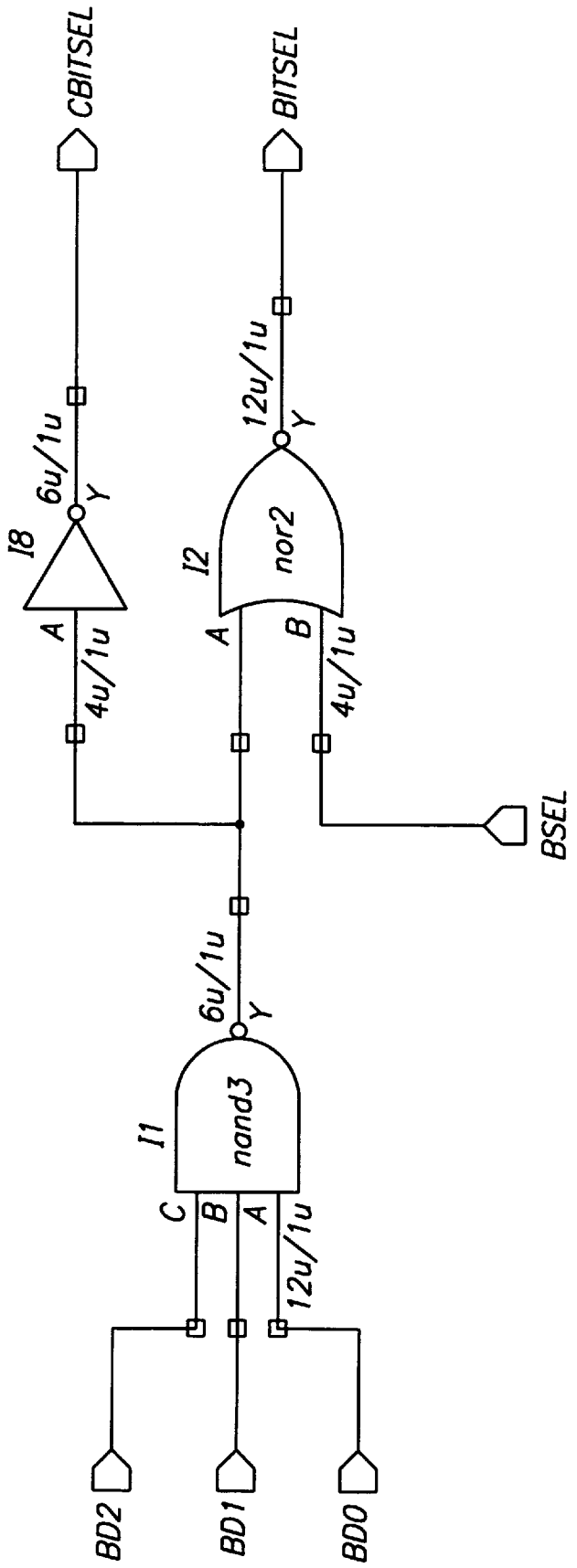

CBITSEL
BITSEL
6u/1u
Y
I8
A
4u/1u
12u/1u
Y
I2
nor2
A
B
4u/1u
BSEL
6u/1u
Y
I1
nand3
C
B
A
12u/1u
BD2
BD1
BD0

FIG. 7L

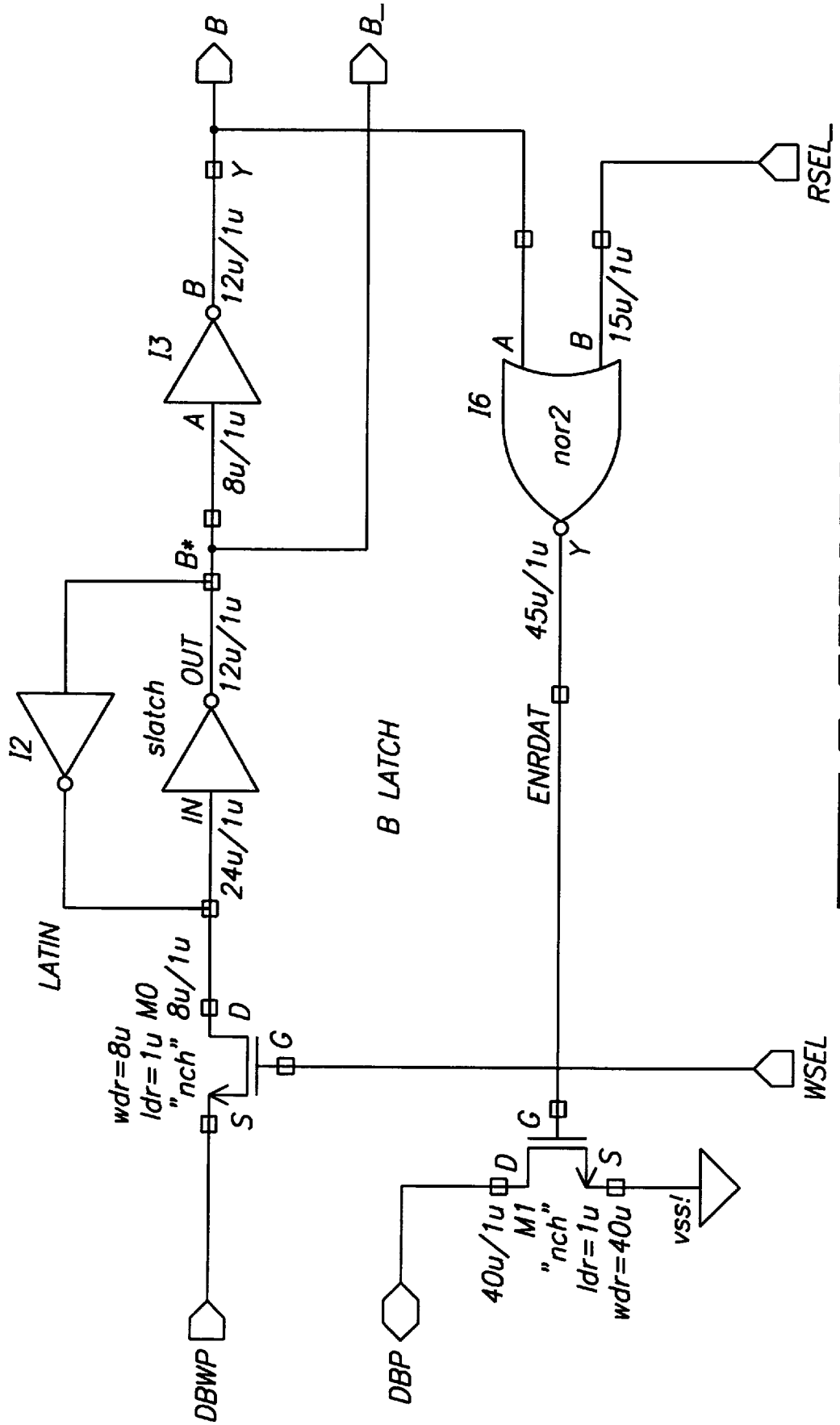
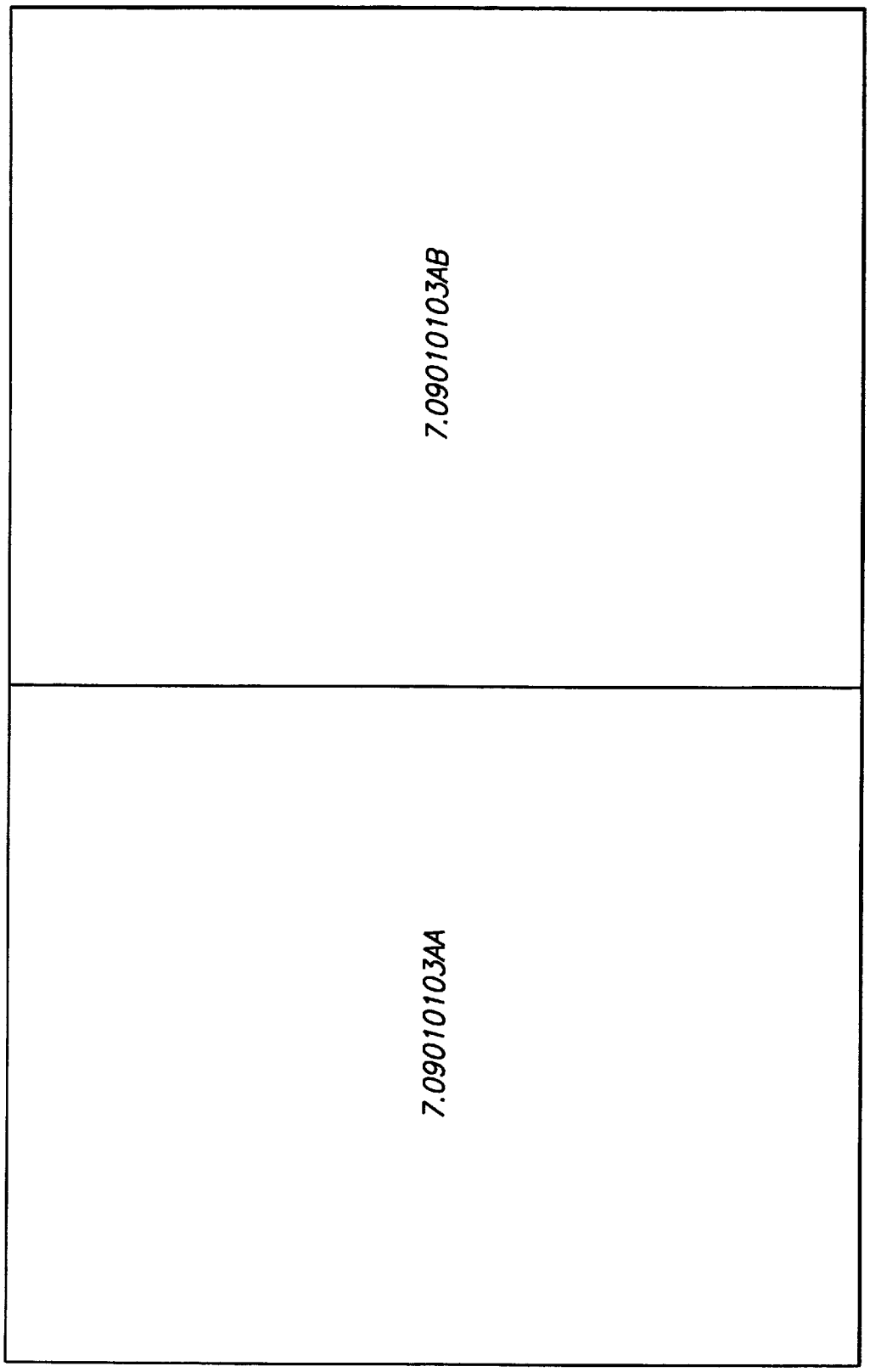

B
B_
Y
12u/1u
B
I3
A
8u/1u
B*
OUT
12u/1u
slatch
IN
24u/1u
I2
LATIN
wdr=8u
ldr=1u
M0
"nch"
8u/1u
D
G
S
DBWP
B LATCH
RSEL
15u/1u
A
B
I6
nor2
Y
45u/1u
ENRDAT
WSEL
G
D
S
40u/1u
M1
"nch"
ldr=1u
wdr=40u
vss!
DBP

FIG 870


7.09010103AB
7.09010103AA
FIG. 7.09010103

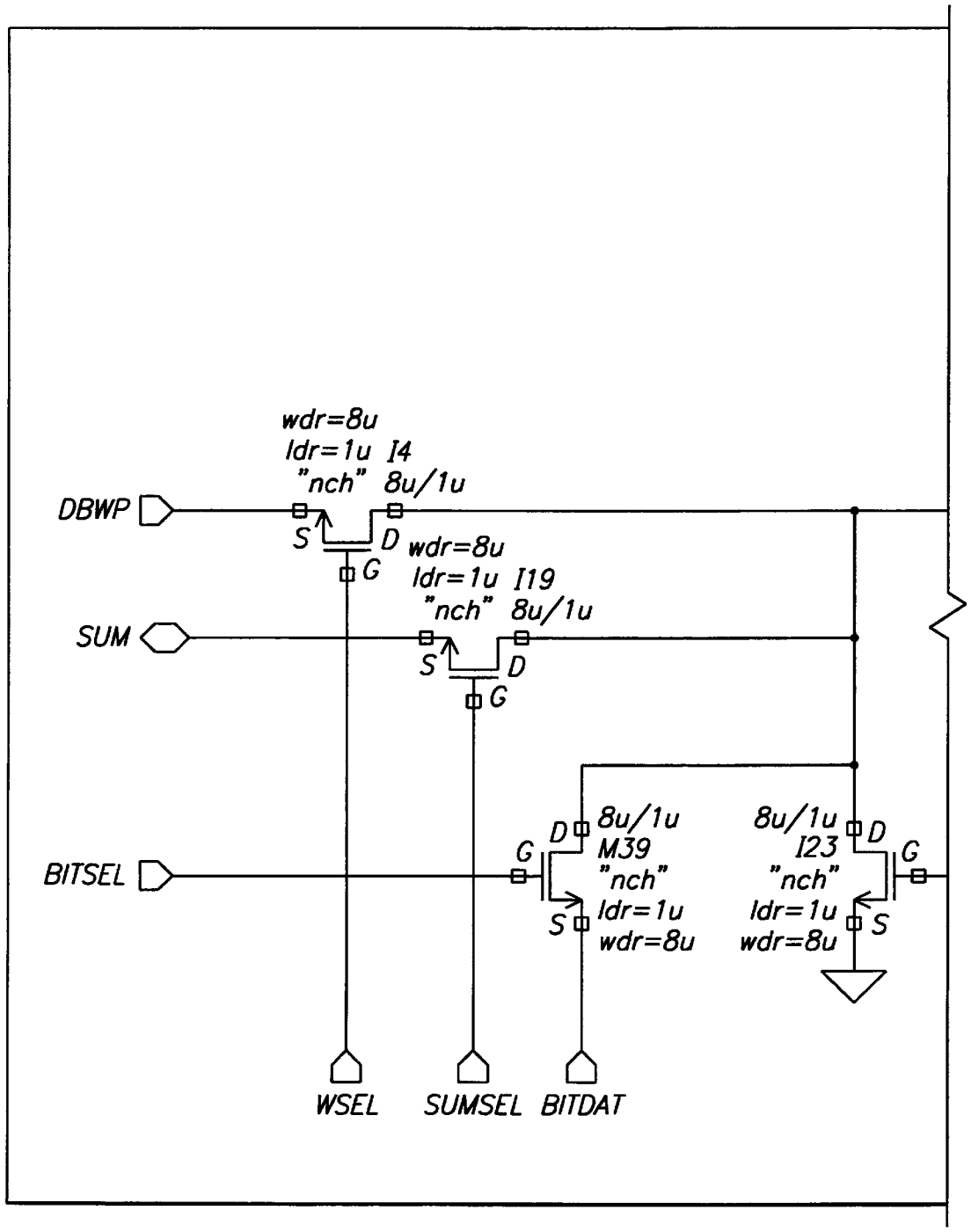


Fig 1.090101103AA

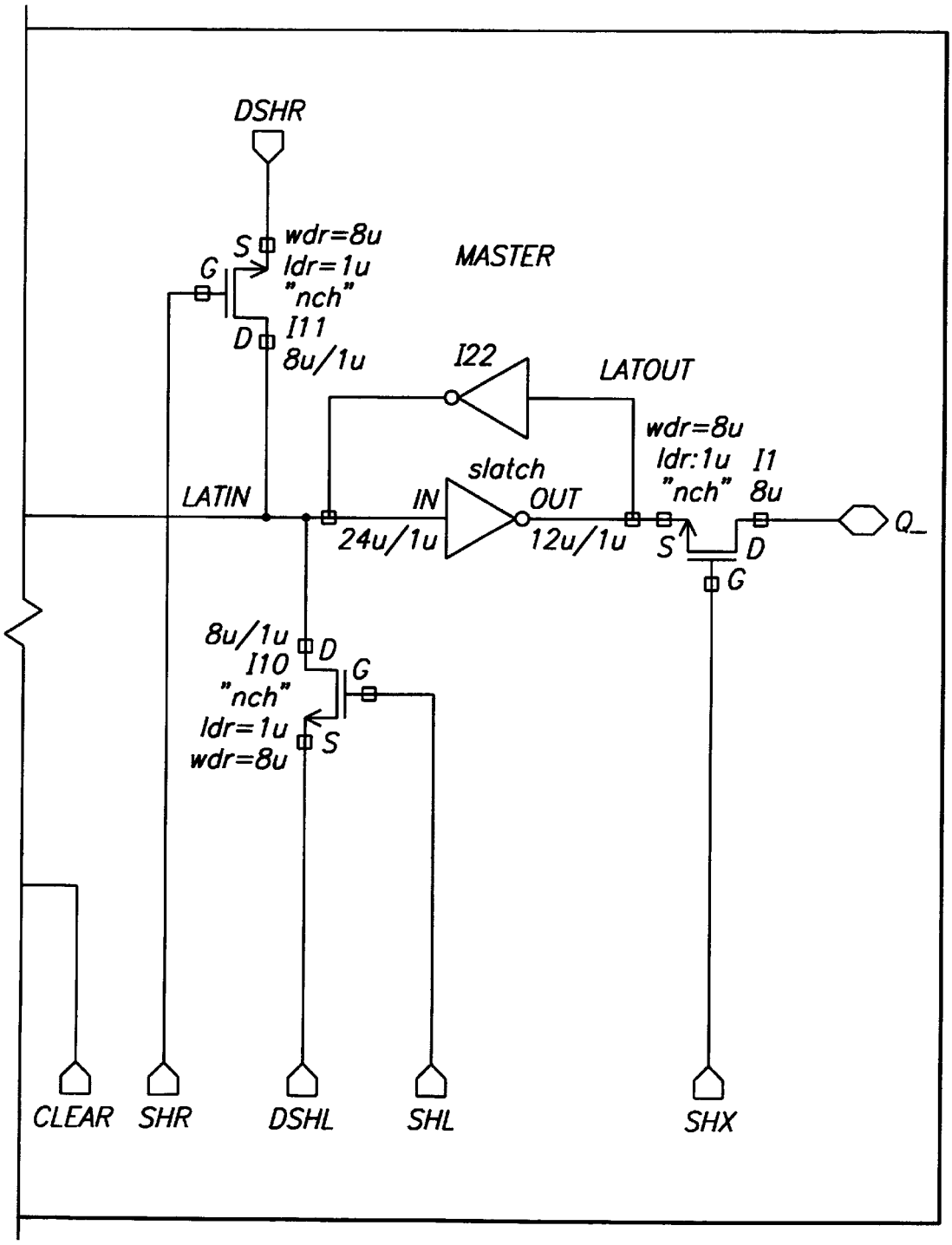


Fig 1.090101030AB

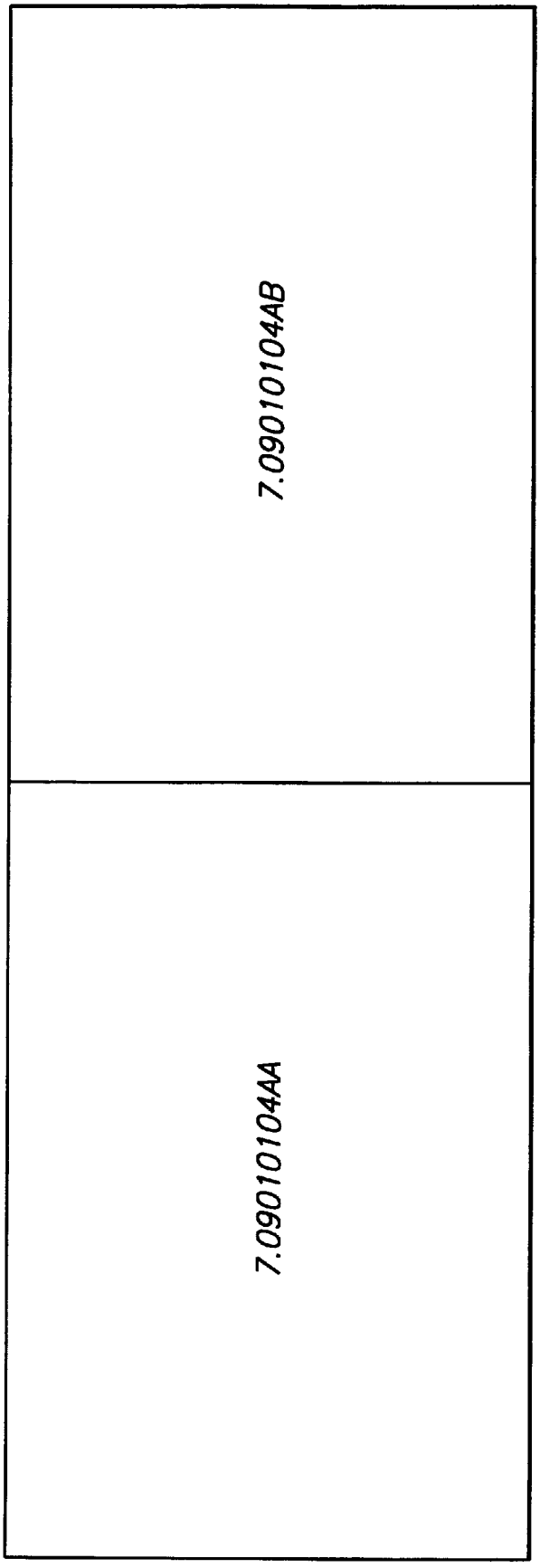


FIG 7.09010104

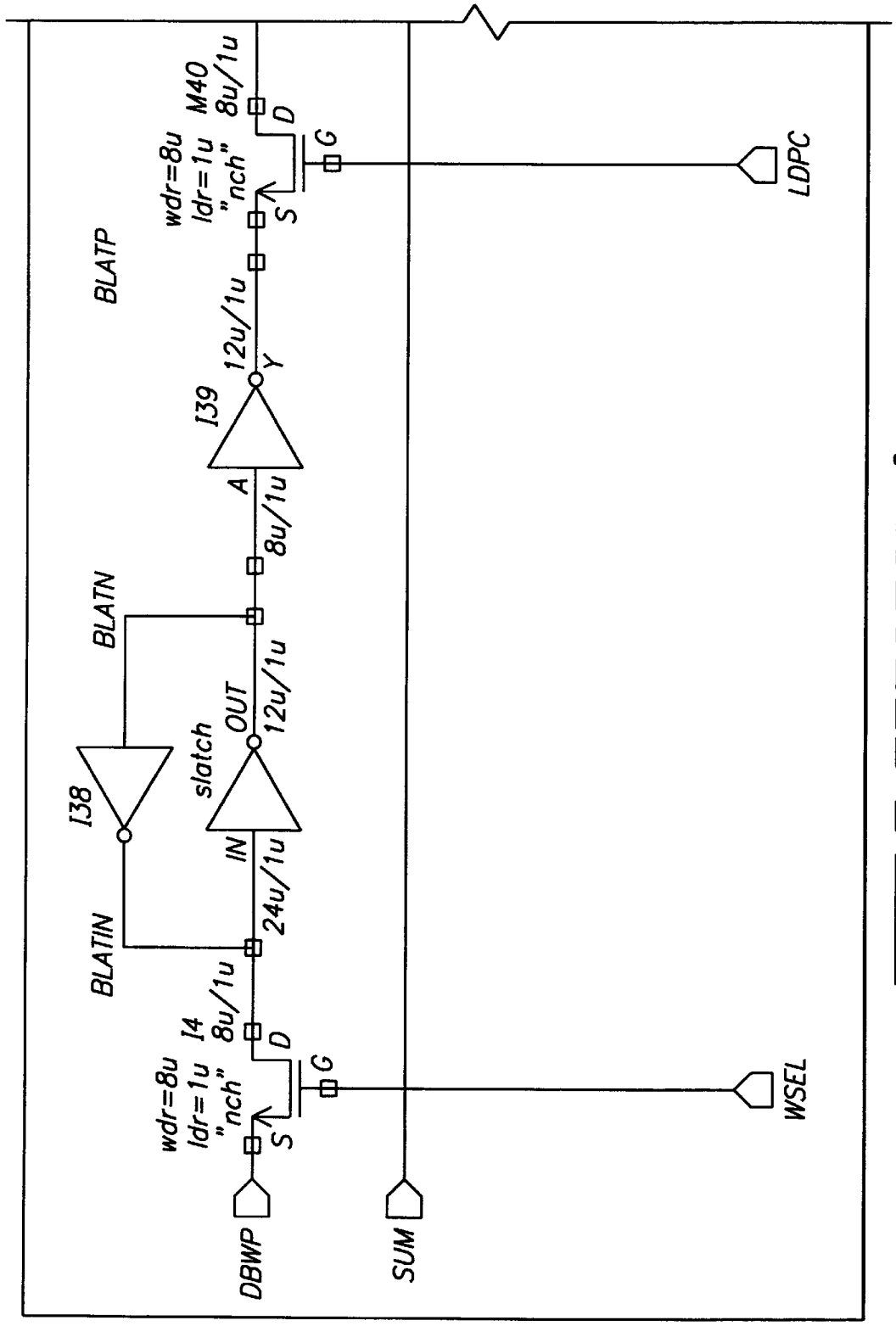

M40
8u/1u
wdr=8u
ldr=1u
"nch"
D
G
S
LDPC
BLATP
12u/1u
Y
I39
A
8u/1u
BLATN
OUT
12u/1u
slatch
I38
IN
24u/1u
BLATIN
I4
8u/1u
wdr=8u
ldr=1u
"nch"
D
G
S
WSEL
DBWP
SUM

FIG 1.0.0.0

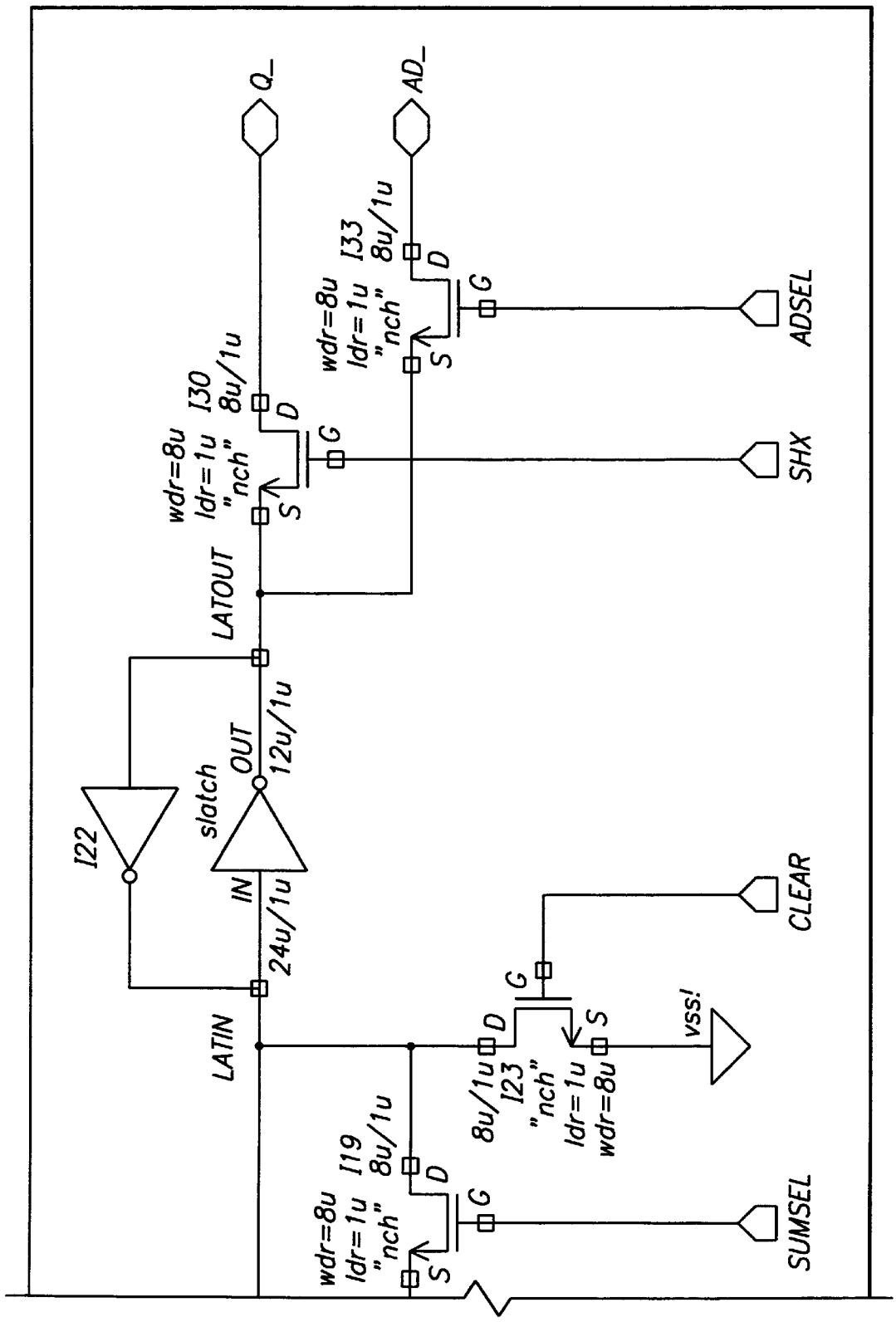

Q_
AD_
I33
8u/1u
wdr=8u
ldr=1u
"nch"
D
G
S
ADSEL
I30
8u/1u
wdr=8u
ldr=1u
"nch"
SHX
LATOUT
I22
slatch
OUT
12u/1u
IN
24u/1u
CLEAR
LATIN
8u/1u
I23
"nch"
ldr=1u
wdr=8u
vss!
I19
8u/1u
wdr=8u
ldr=1u
"nch"
SUMSEL

FIG. 876

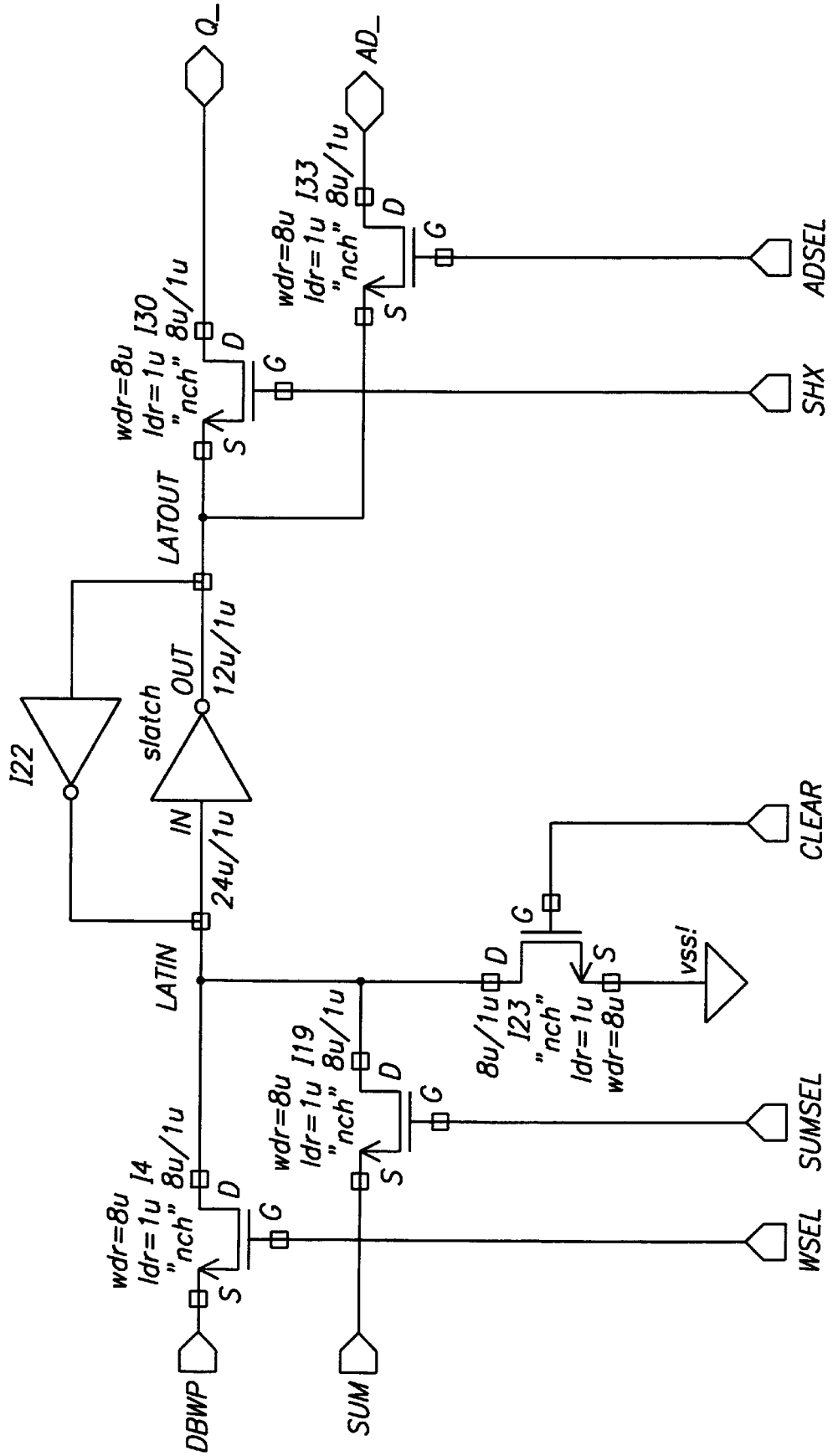
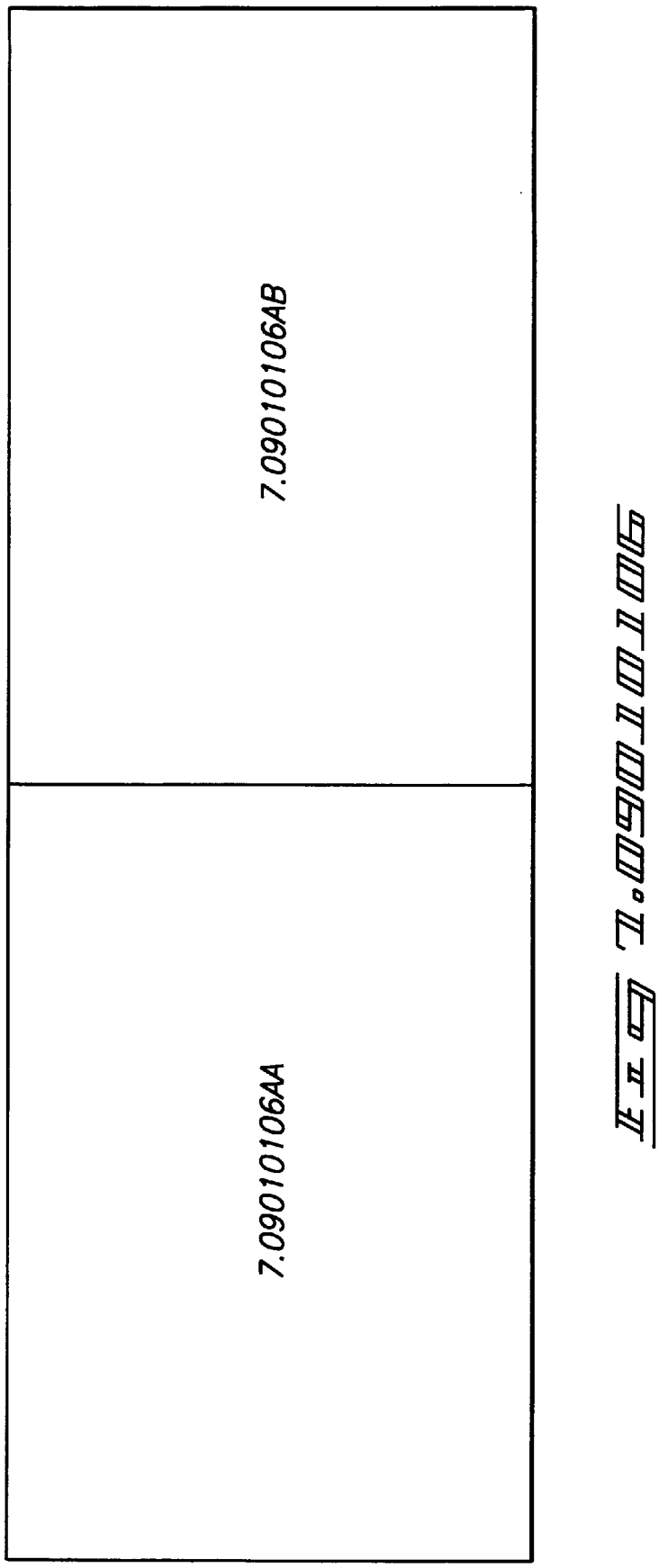

Q_
AD_
I33
wdr=8u
ldr=1u
"nch"
8u/1u
D
G
S
ADSEL
I30
wdr=8u
ldr=1u
"nch"
8u/1u
SHX
LATOUT
I22
slatch
OUT
12u/1u
IN
24u/1u
LATIN
CLEAR
I23
"nch"
ldr=1u
wdr=8u
8u/1u
vss!
I19
wdr=8u
ldr=1u
"nch"
8u/1u
SUMSEL
I4
wdr=8u
ldr=1u
"nch"
8u/1u
WSEL
DBWP
SUM

FIG. 7.0600.1


7.09010106AB
7.09010106AA
FIG. 7.09010106

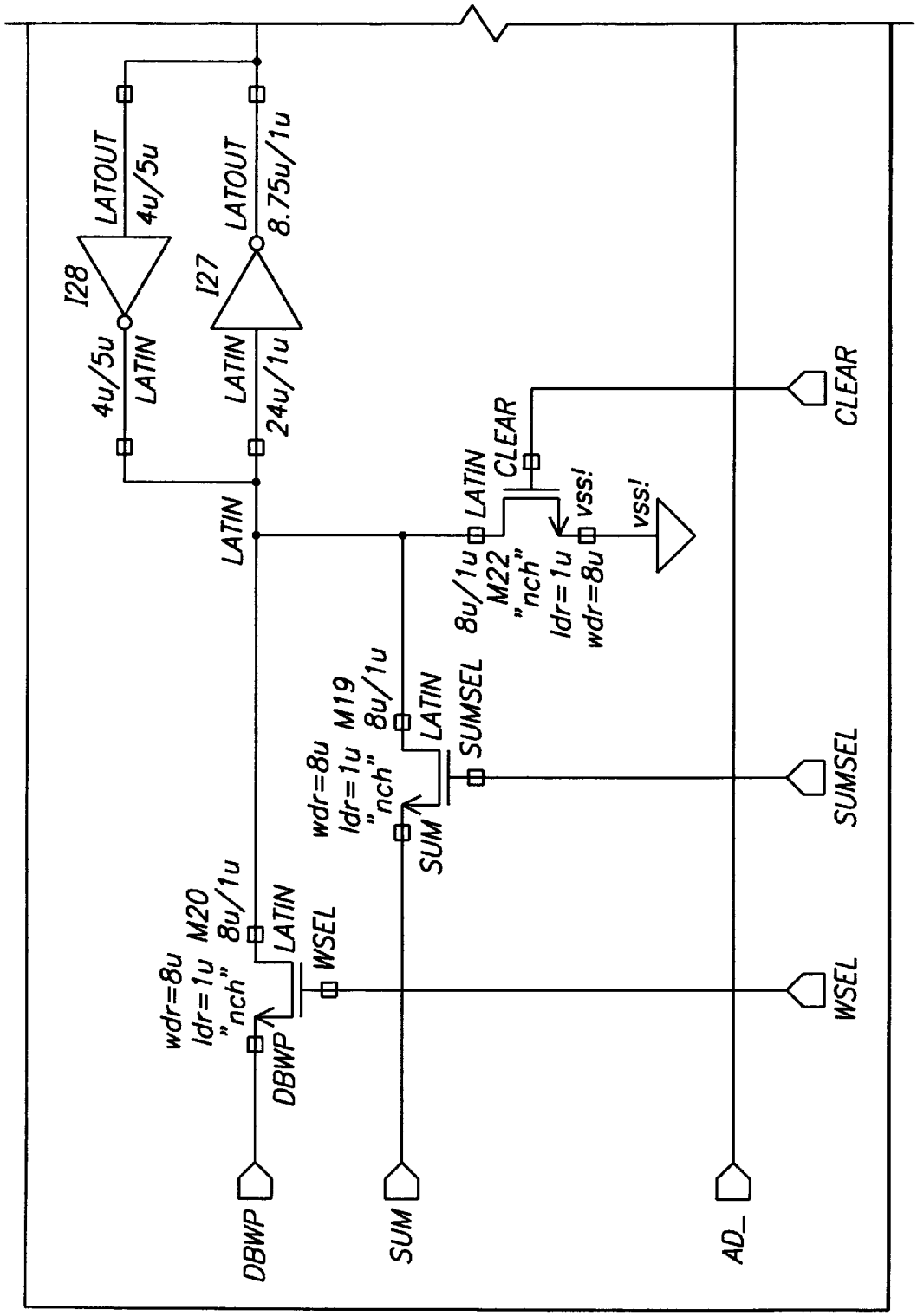

I28
LATOUT
4u/5u
4u/5u
LATIN
I27
LATOUT
8.75u/1u
LATIN
24u/1u
LATIN
CLEAR
LATIN
8u/1u
M22
"nch"
ldr=1u
wdr=8u
vss!
vss!
CLEAR
wdr=8u
ldr=1u
"nch"
M19
8u/1u
LATIN
SUMSEL
SUM
SUMSEL
wdr=8u
ldr=1u
"nch"
M20
8u/1u
LATIN
WSEL
DBWP
WSEL
DBWP
SUM
AD_

FIG. 69.1

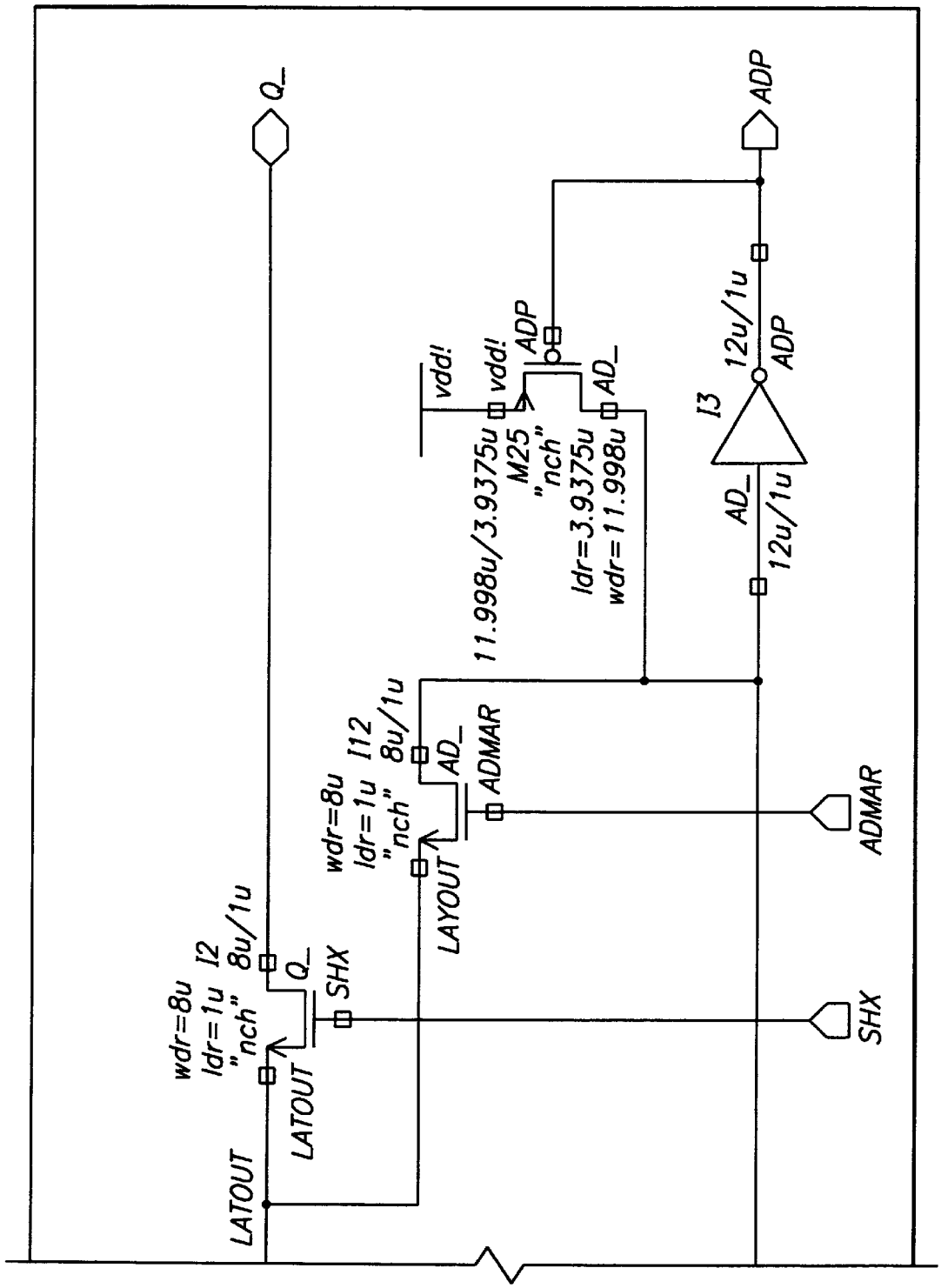

Q_
ADP
vdd!
vdd!
ADP
M25
"nch"
ldr=3.9375u
wdr=11.998u
AD_
11.998u/3.9375u
I3
12u/1u
ADP
AD_
12u/1u
I12
8u/1u
AD_
ADMAR
wdr=8u
ldr=1u
"nch"
LAYOUT
ADMAR
I2
8u/1u
Q_
SHX
wdr=8u
ldr=1u
"nch"
LATOUT
LATOUT
SHX

FIG. 1.0901 L

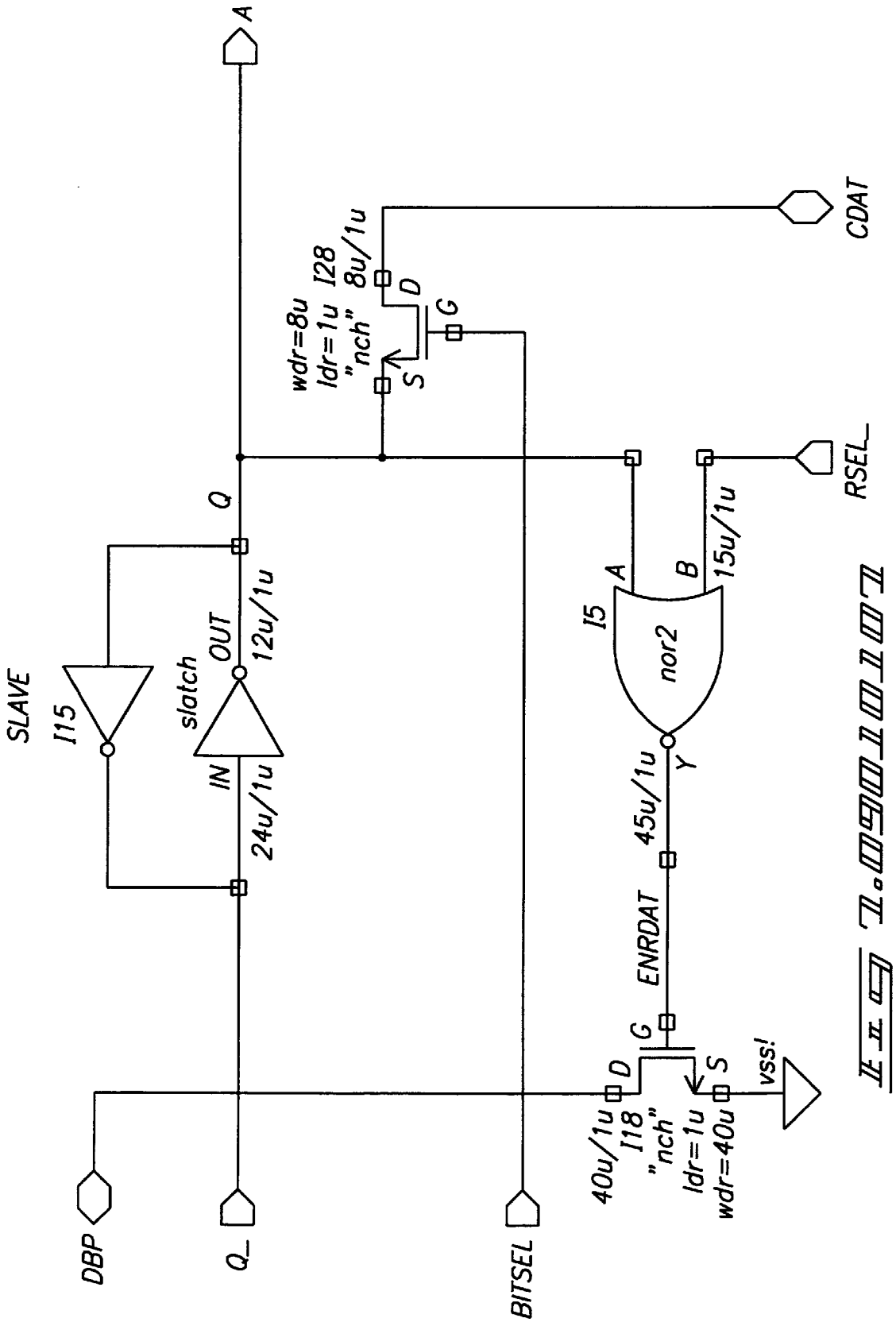

A
CDAT
wdr=8u
ldr=1u
"nch"
I28
8u/1u
D
G
S
RSEL_
Q
SLAVE
I15
slatch
OUT
12u/1u
I5
A
B
15u/1u
nor2
IN
24u/1u
Y
45u/1u
ENRDAT
G
D
S
vss!
40u/1u
I18
"nch"
ldr=1u
wdr=40u
DBP
Q_
BITSEL

FIG. 1.0950

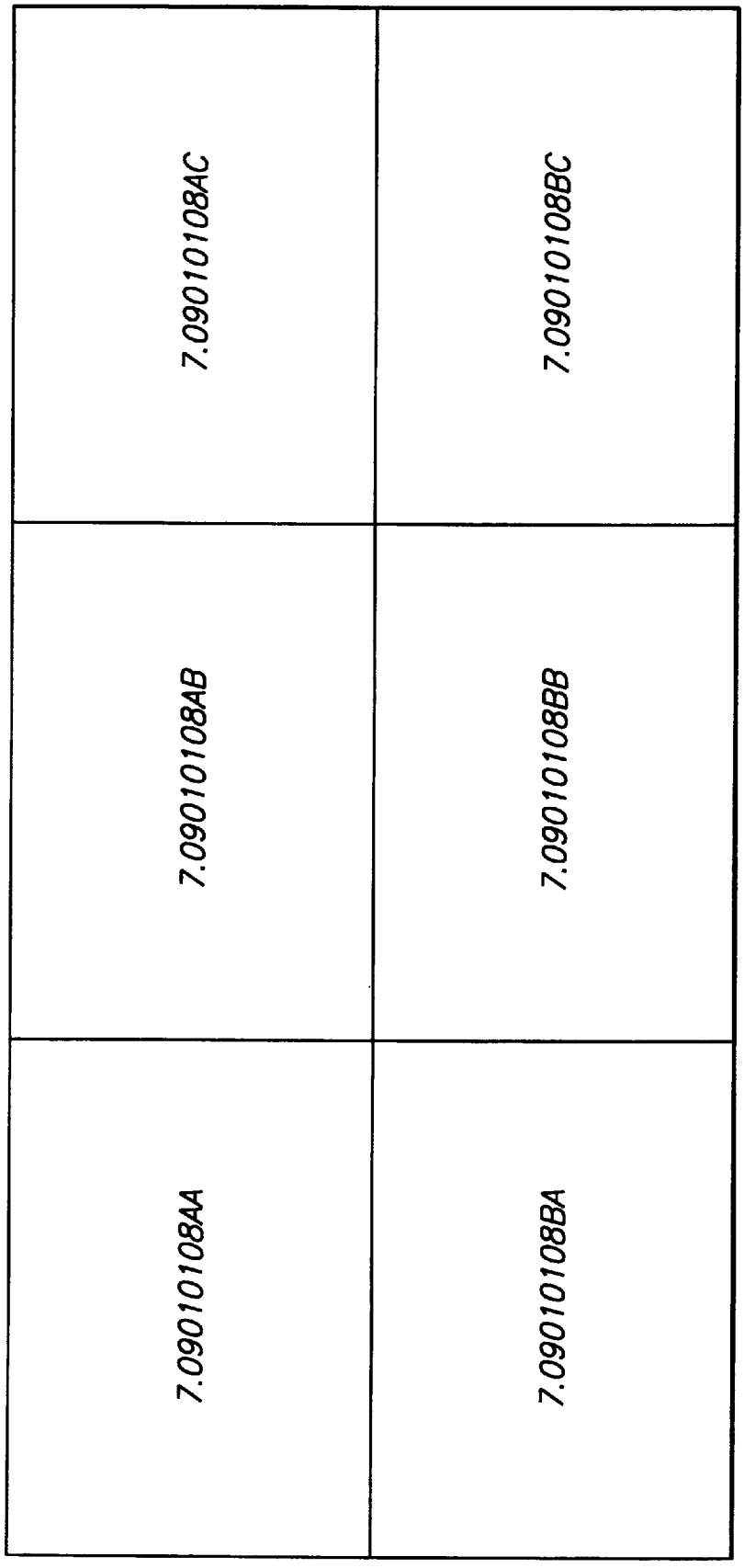
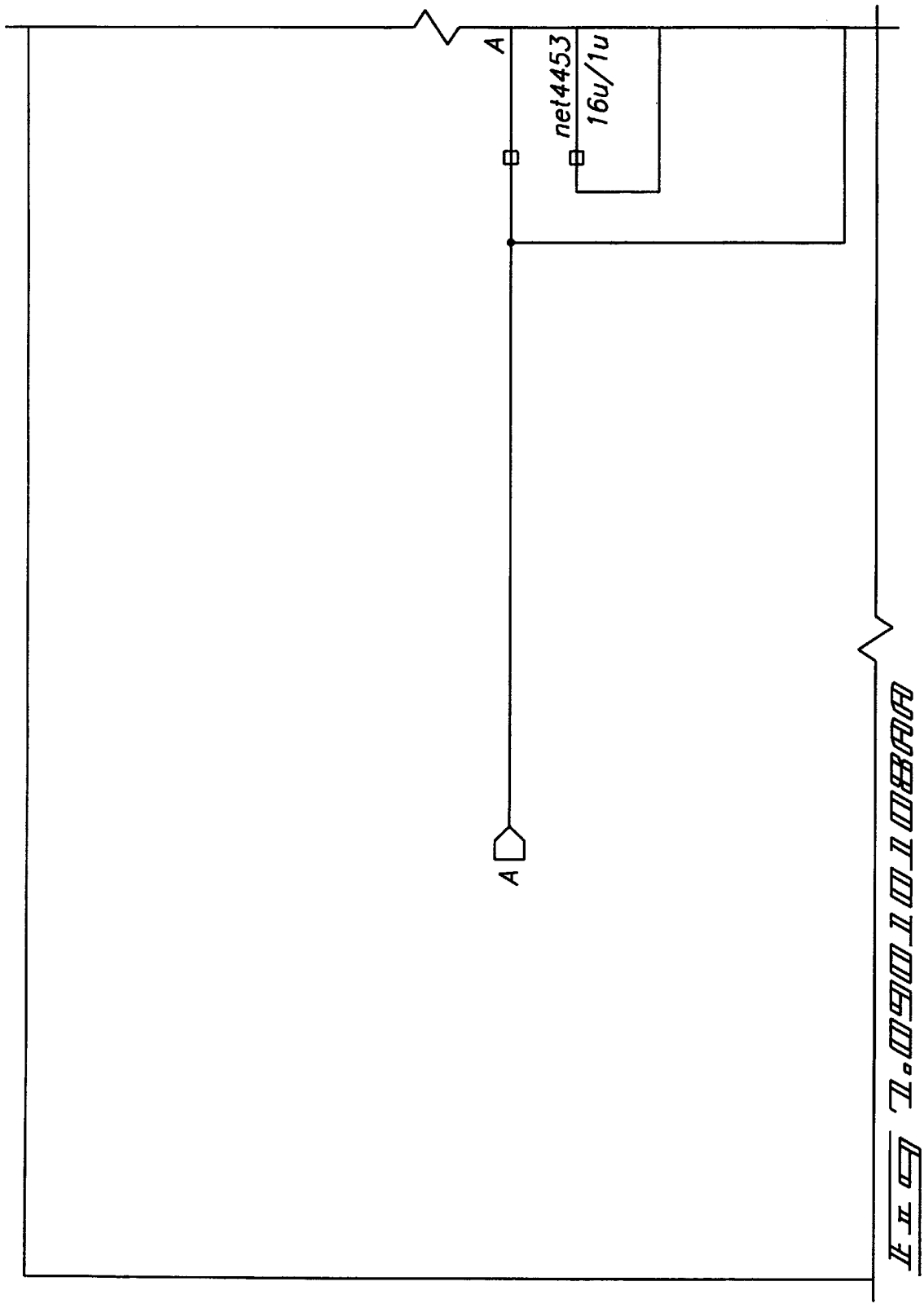
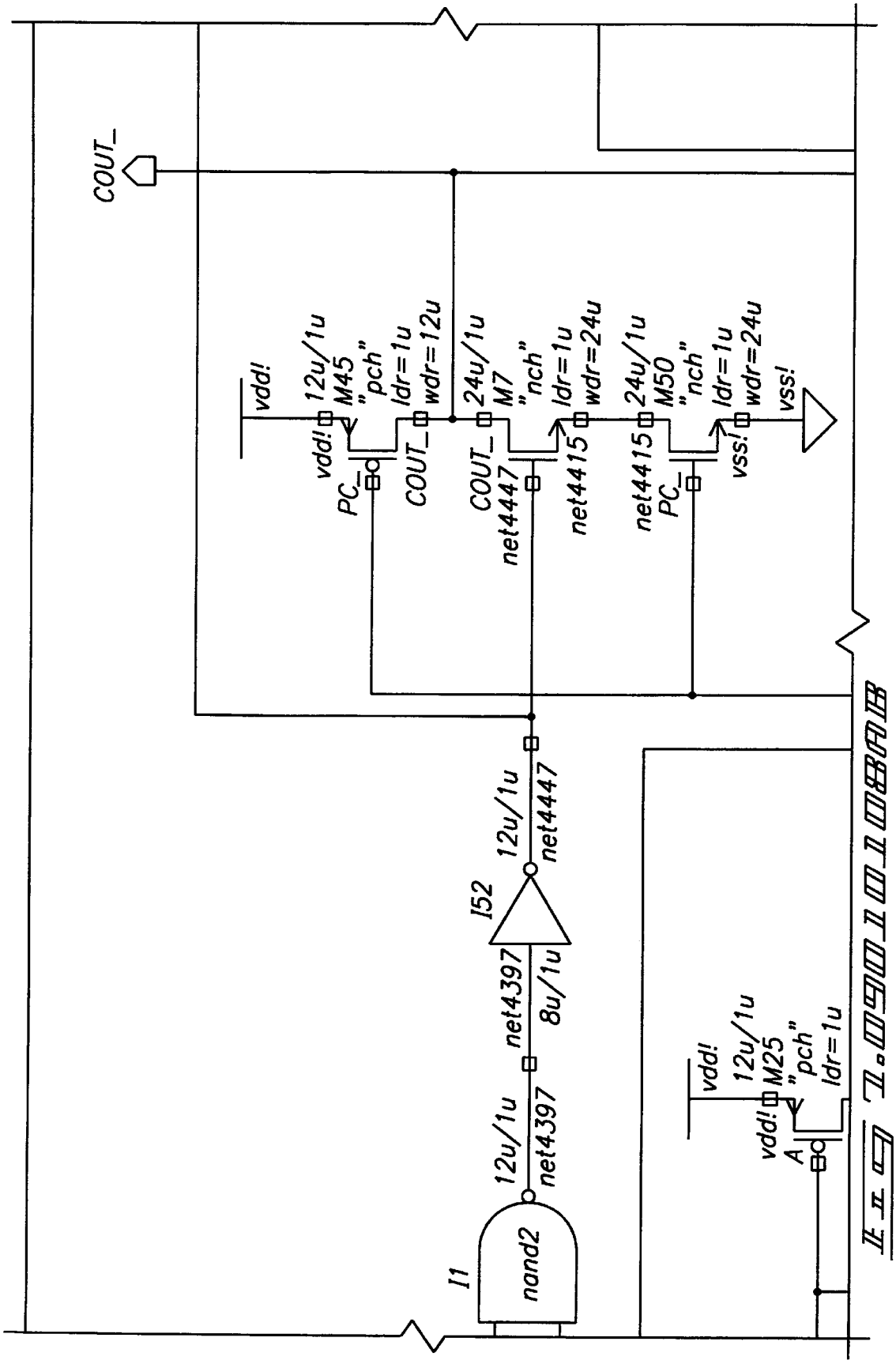
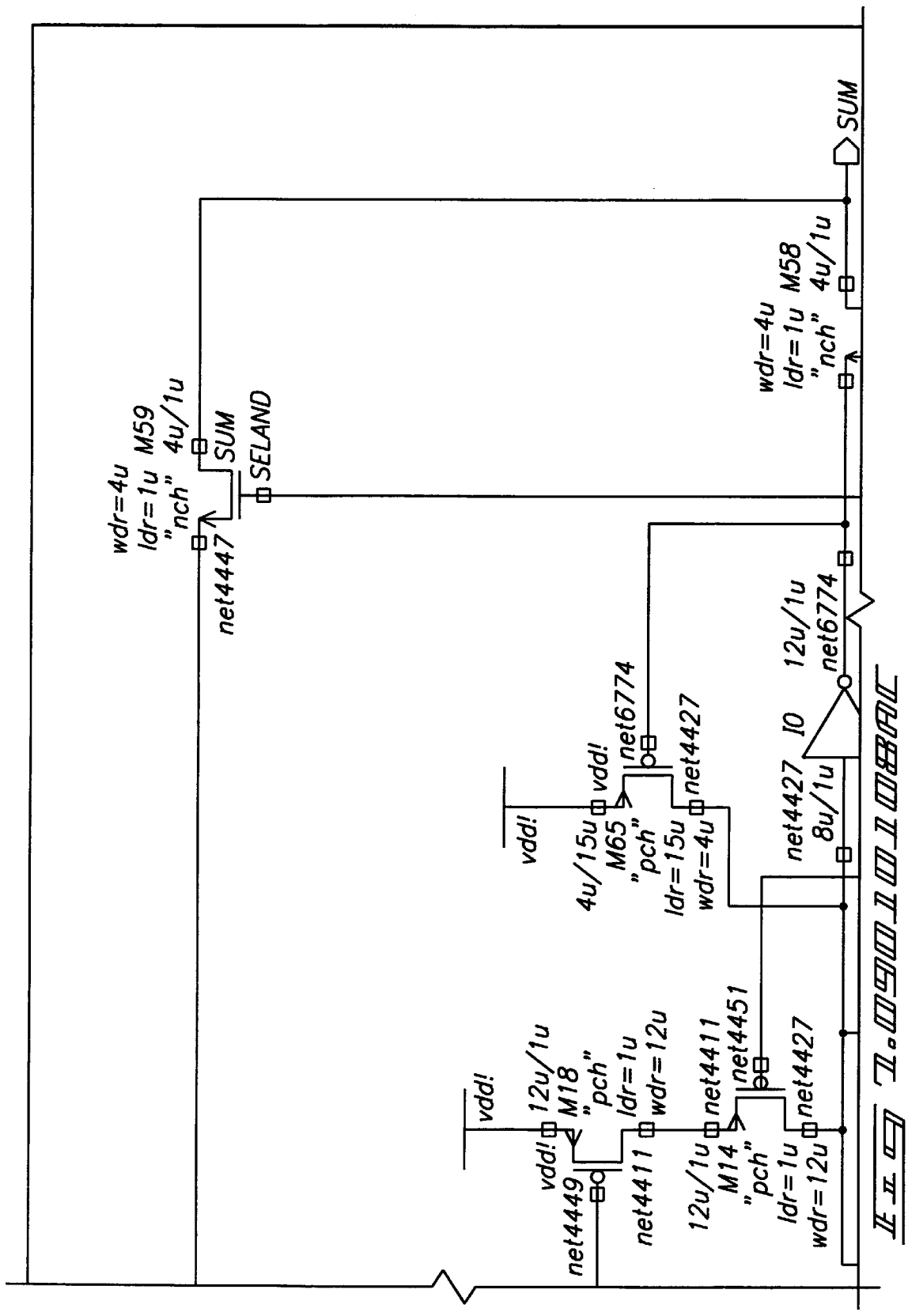


FIG. 7.09010108


A
net4453
16u/1u
A
VSS


COUT_
vdd!
12u/1u
M45
"pch"
ldr=1u
wdr=12u
24u/1u
M7
"nch"
ldr=1u
wdr=24u
24u/1u
M50
"nch"
ldr=1u
wdr=24u
vss!
PC_
COUT_
net4447
net4415
12u/1u
net4447
I52
net4397
8u/1u
12u/1u
net4397
I1
nand2
A
M25
"pch"
ldr=1u


SUM
wdr=4u
ldr=1u M58
"nch" 4u/1u
wdr=4u
ldr=1u M59
"nch" 4u/1u
SUM
SELAND
net4447
net6774
12u/1u
I0
net4427
8u/1u
vdd!
4u/15u
M65
"pch"
ldr=15u
wdr=4u
net6774
net4427
vdd!
12u/1u
M18
"pch"
ldr=1u
wdr=12u
net4411
net4449
vdd!
12u/1u
M14
"pch"
ldr=1u
wdr=12u
net4411
net4451
net4427

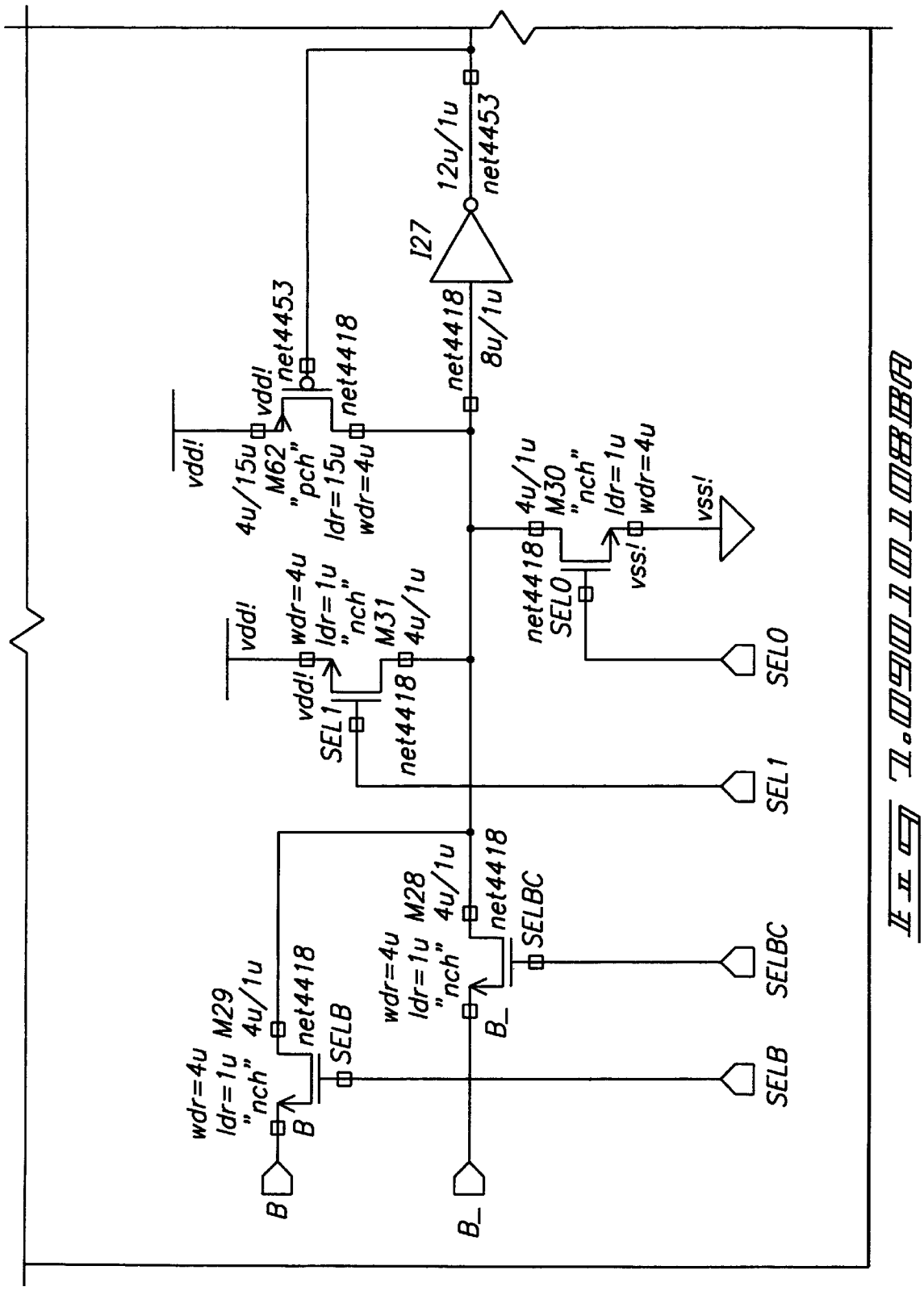

I27
12u/1u
net4453
net4418
8u/1u
vdd!
4u/15u
M62
"pch"
ldr=15u
wdr=4u
net4453
net4418
vdd!
wdr=4u
ldr=1u
"nch"
M31
4u/1u
SEL1
net4418
vdd!
4u/1u
M30
"nch"
ldr=1u
wdr=4u
vss!
net4418
SEL0
vss!
SEL0
SEL1
wdr=4u
ldr=1u
"nch"
M29
4u/1u
net4418
SELB
B
B
wdr=4u
ldr=1u
"nch"
M28
4u/1u
net4418
SELBC
B_
B_
SELBC
SELB

FIG. 5

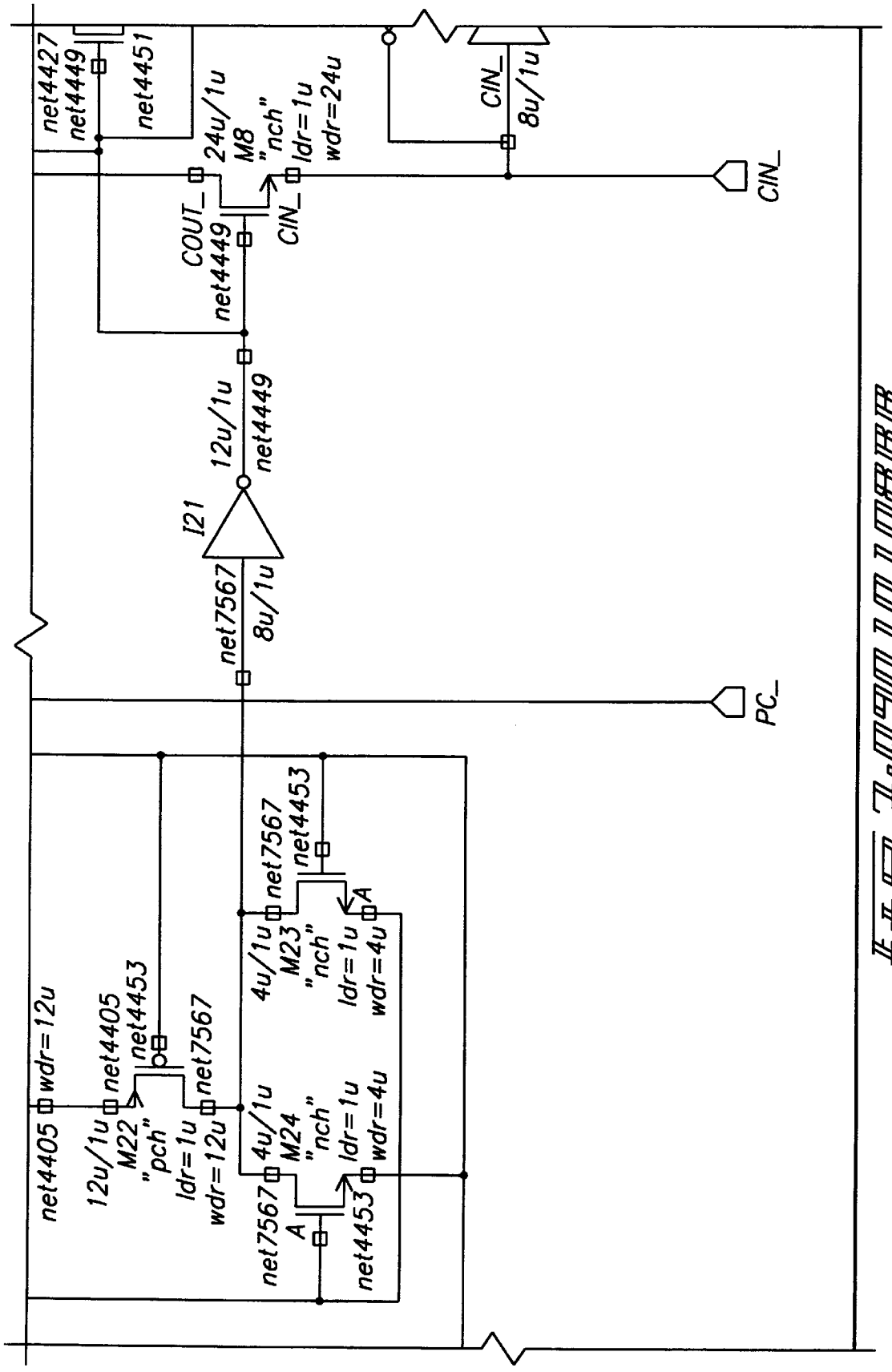
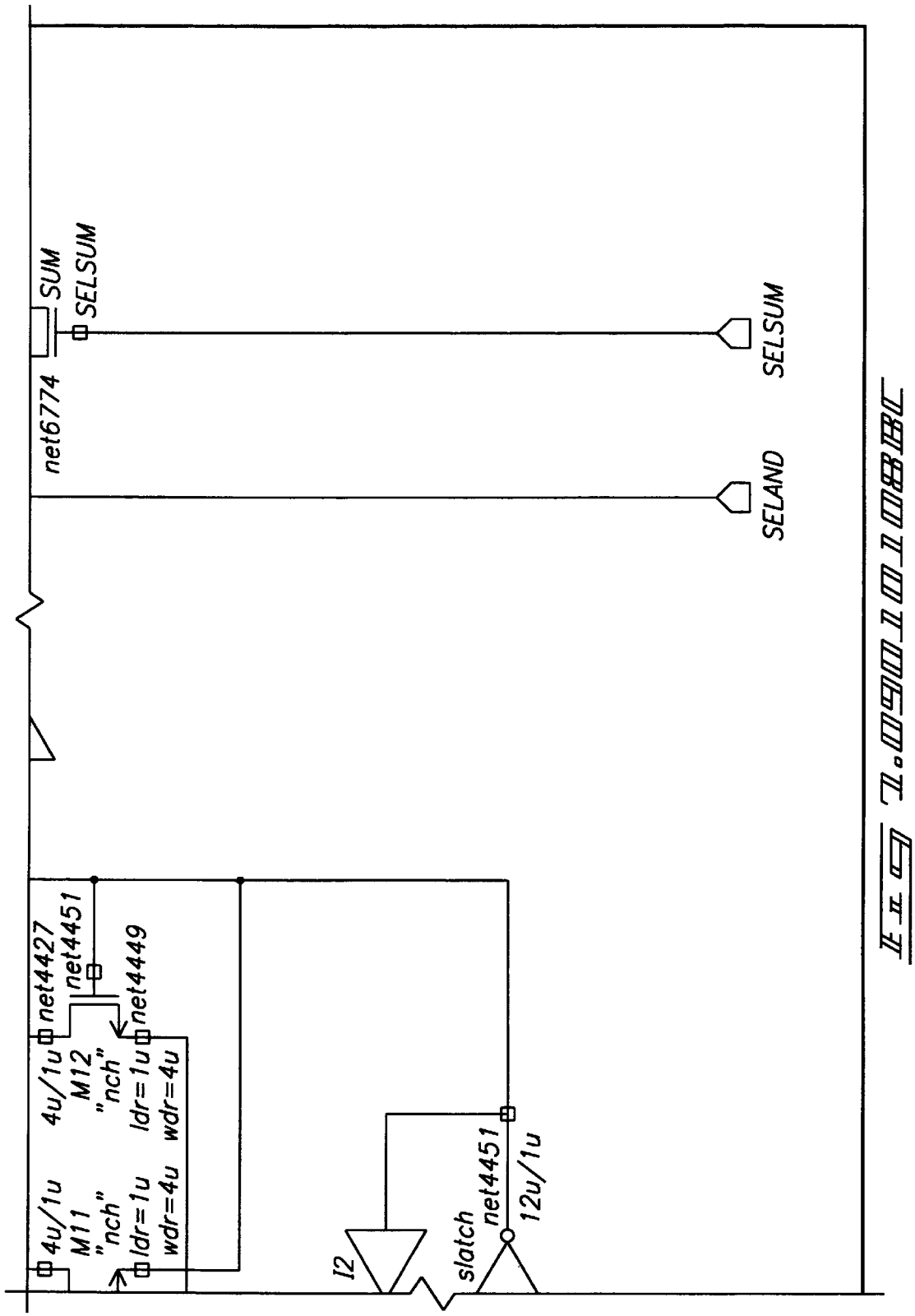

net4427
net4449
net4451
24u/1u
M8
"nch"
ldr=1u
wdr=24u
CIN_
8u/1u
CIN_
COUT_
net4449
CIN_
12u/1u
net4449
I21
net7567
8u/1u
PC_
net4405
wdr=12u
12u/1u
M22
"pch"
ldr=1u
wdr=12u
net4405
net4453
net7567
4u/1u
M24
"nch"
ldr=1u
wdr=4u
net7567
A
net4453
4u/1u
M23
"nch"
ldr=1u
wdr=4u
net7567
net4453
A

FIG. 6.050.11


SUM
SELSUM
net6774
SELSUM
SELAND
net4427
net4451
net4449
4u/1u
M12
"nch"
ldr=1u
wdr=4u
4u/1u
M11
"nch"
ldr=1u
wdr=4u
I2
slatch
net4451
12u/1u

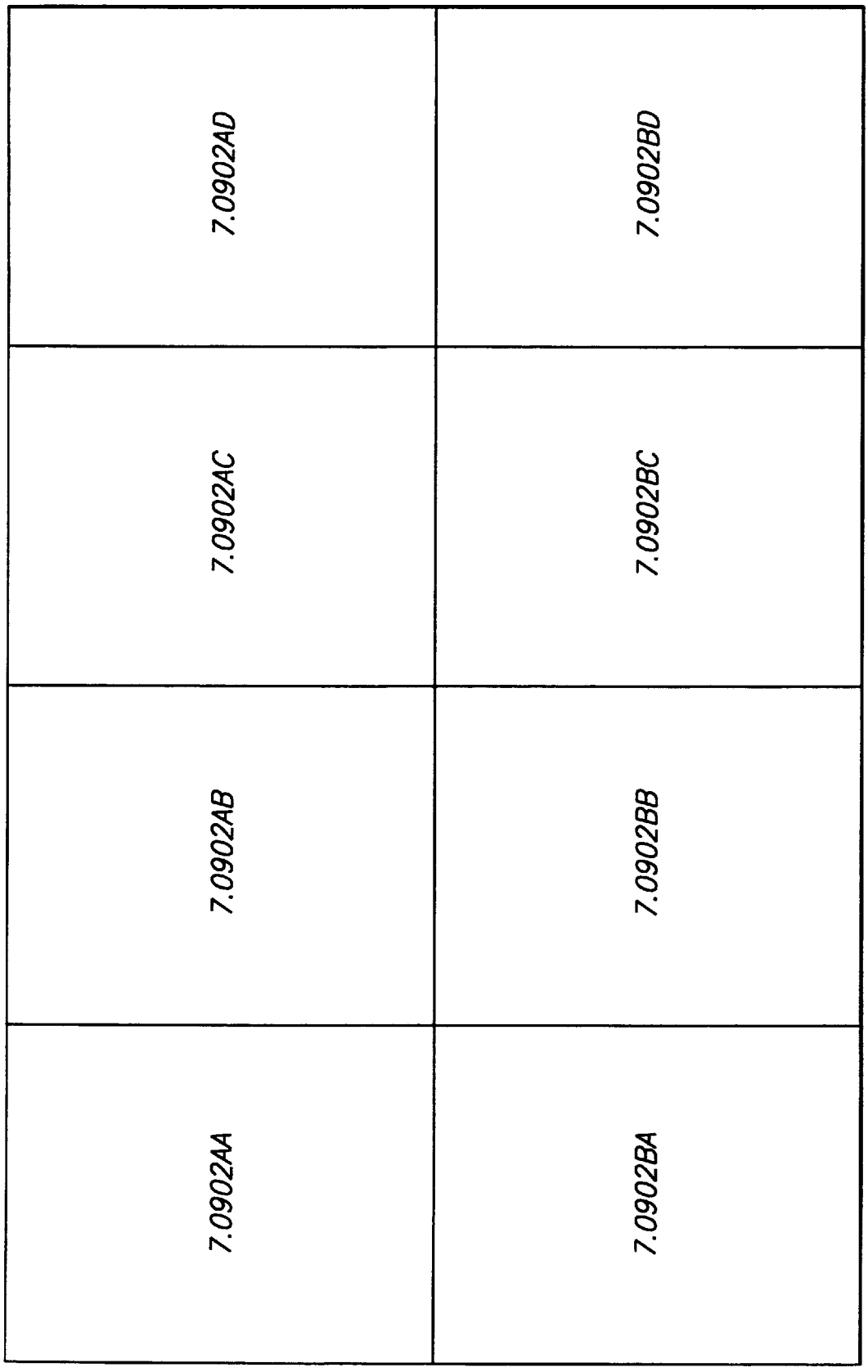

7.0902AD
7.0902BD
7.0902AC
7.0902BC
7.0902AB
7.0902BB
7.0902AA
7.0902BA

FIG. 7.0902

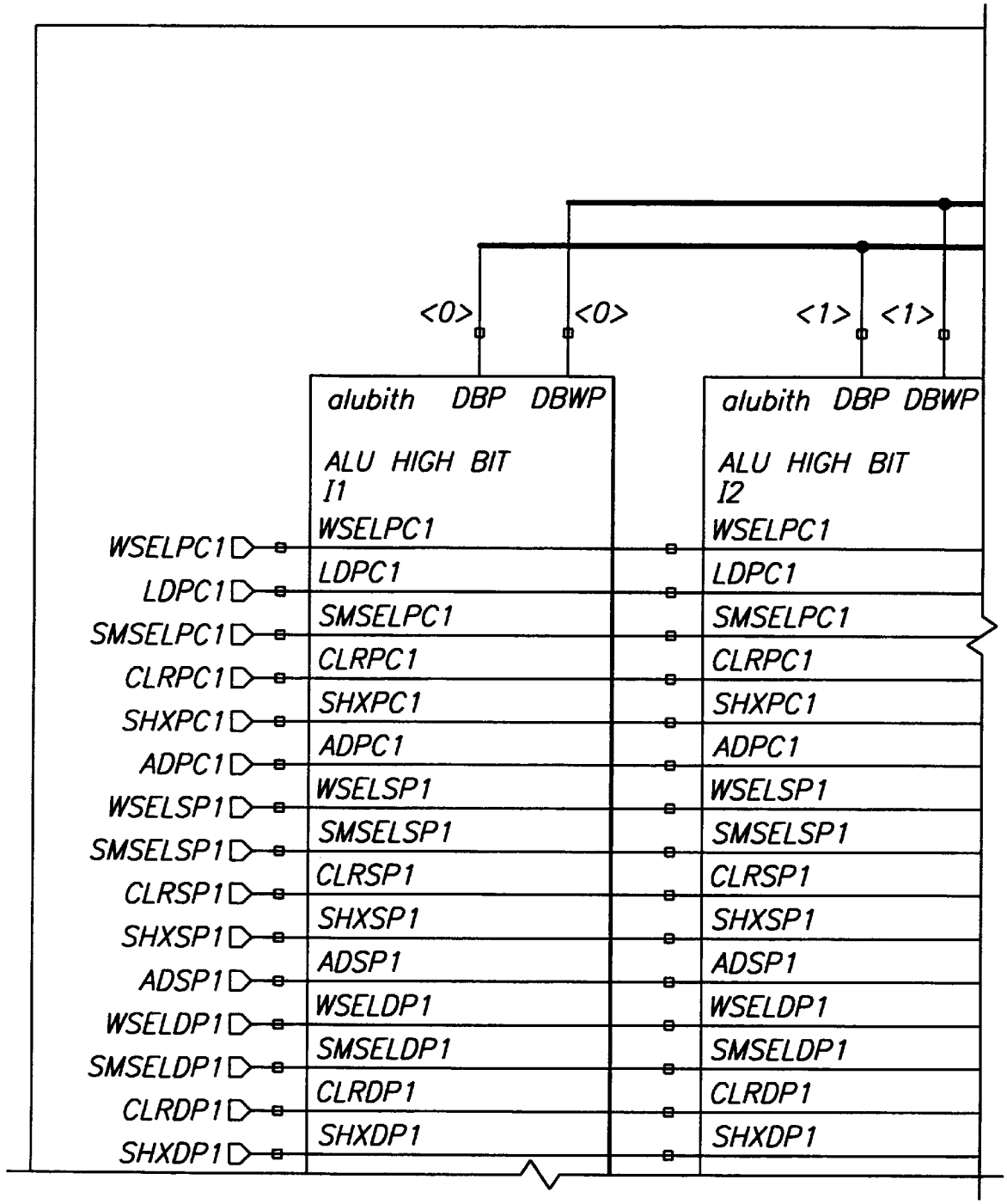

<0>
<0>
<1>
<1>
alubith DBP DBWP
ALU HIGH BIT
I1
alubith DBP DBWP
ALU HIGH BIT
I2
WSELPC1
LDPC1
SMSELPC1
CLRPC1
SHXPC1
ADPC1
WSELSP1
SMSELSP1
CLRSP1
SHXSP1
ADSP1
WSELDP1
SMSELDP1
CLRDP1
SHXDP1

Fig 1.090zAA

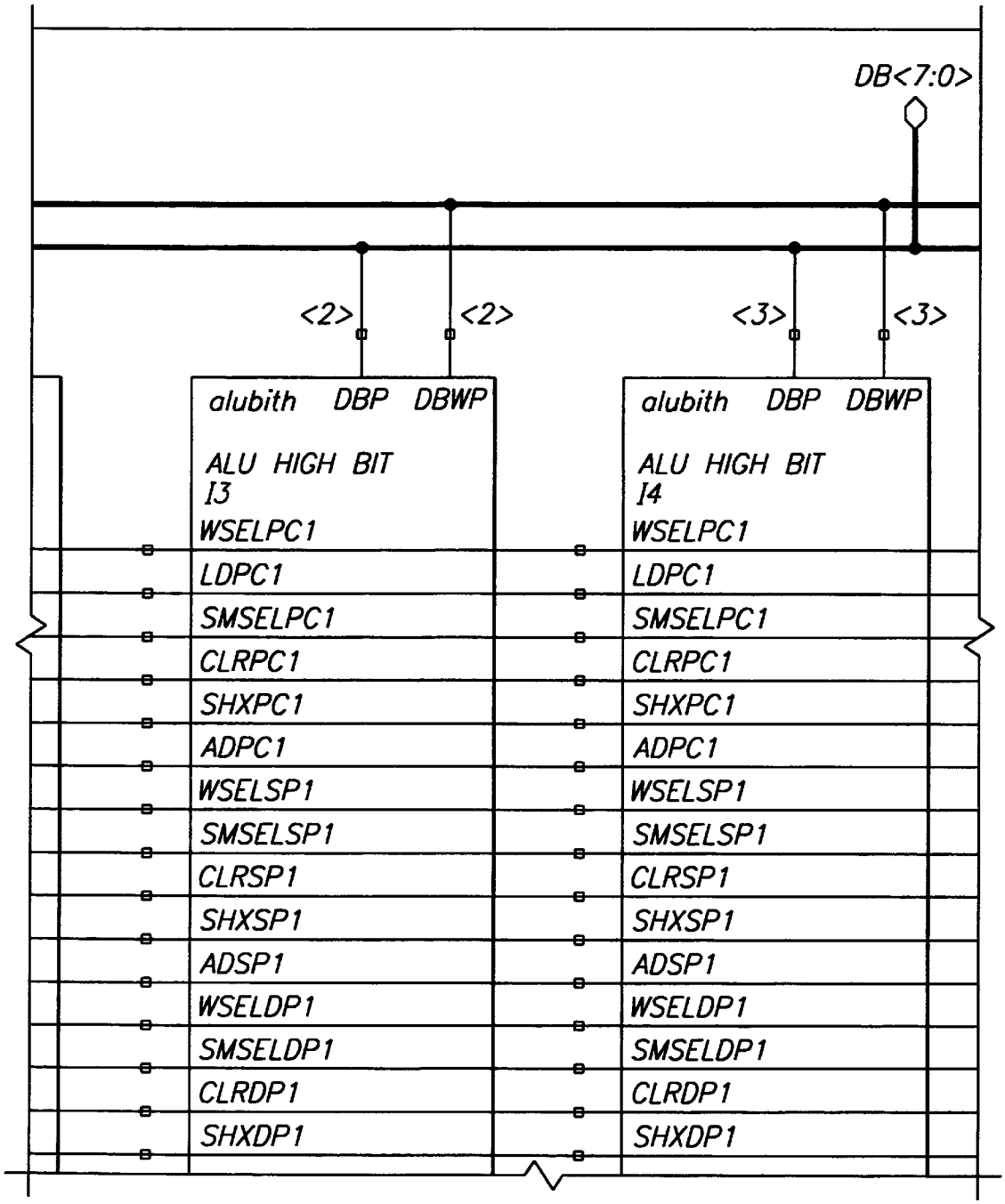

DB<7:0>
<2>
<2>
<3>
<3>
alubith DBP DBWP
ALU HIGH BIT
I3
WSELPC1
LDPC1
SMSELPC1
CLRPC1
SHXPC1
ADPC1
WSELSP1
SMSELSP1
CLRSP1
SHXSP1
ADSP1
WSELDP1
SMSELDP1
CLRDP1
SHXDP1
alubith DBP DBWP
ALU HIGH BIT
I4
WSELPC1
LDPC1
SMSELPC1
CLRPC1
SHXPC1
ADPC1
WSELSP1
SMSELSP1
CLRSP1
SHXSP1
ADSP1
WSELDP1
SMSELDP1
CLRDP1
SHXDP1

Fig 1.090208

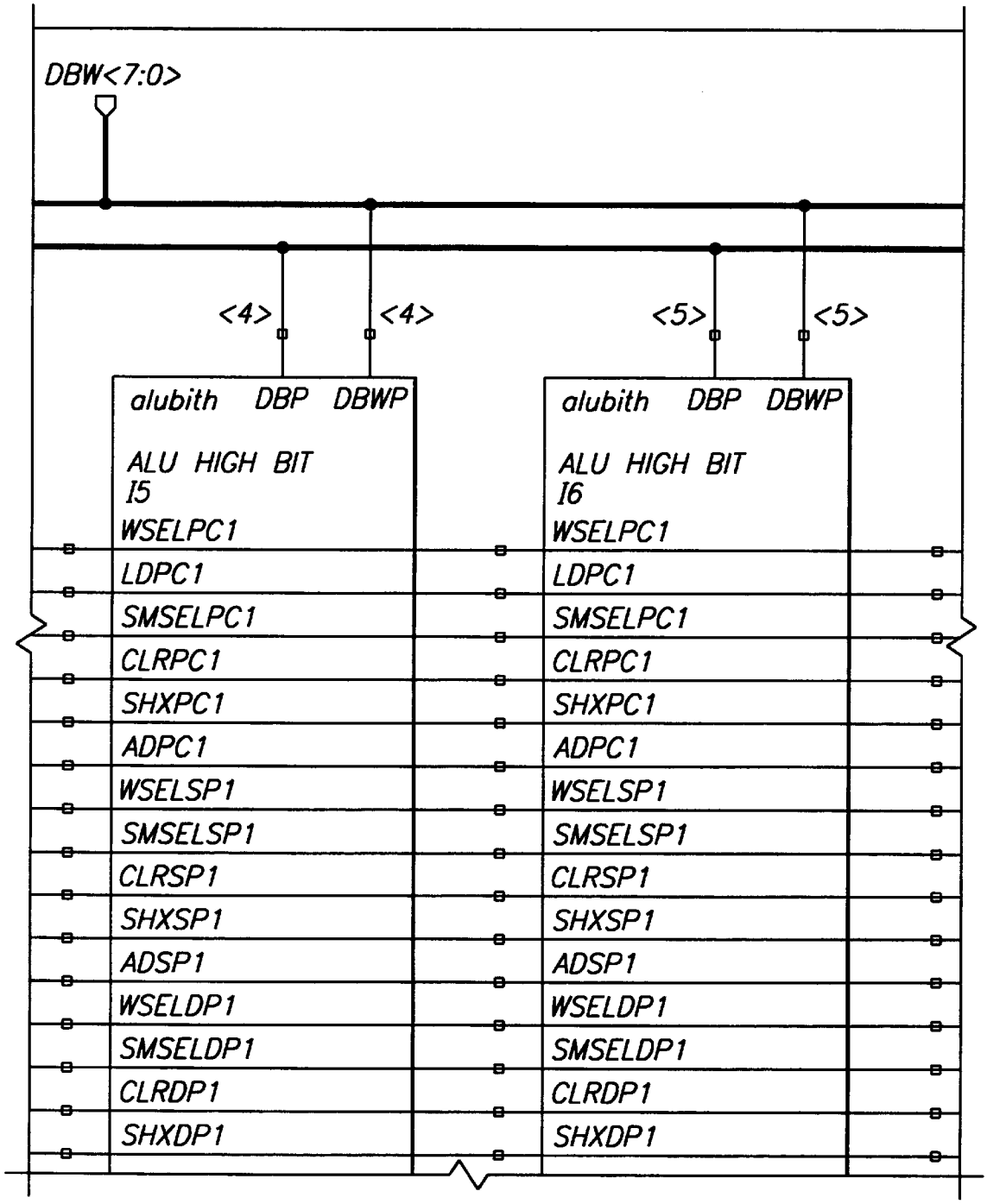

DBW<7:0>
<4>
<4>
<5>
<5>
alubith DBP DBWP
ALU HIGH BIT
I5
alubith DBP DBWP
ALU HIGH BIT
I6
WSELPC1
LDPC1
SMSELPC1
CLRPC1
SHXPC1
ADPC1
WSELSP1
SMSELSP1
CLRSP1
SHXSP1
ADSP1
WSELDP1
SMSELDP1
CLRDP1
SHXDP1

Fig 1.090AC

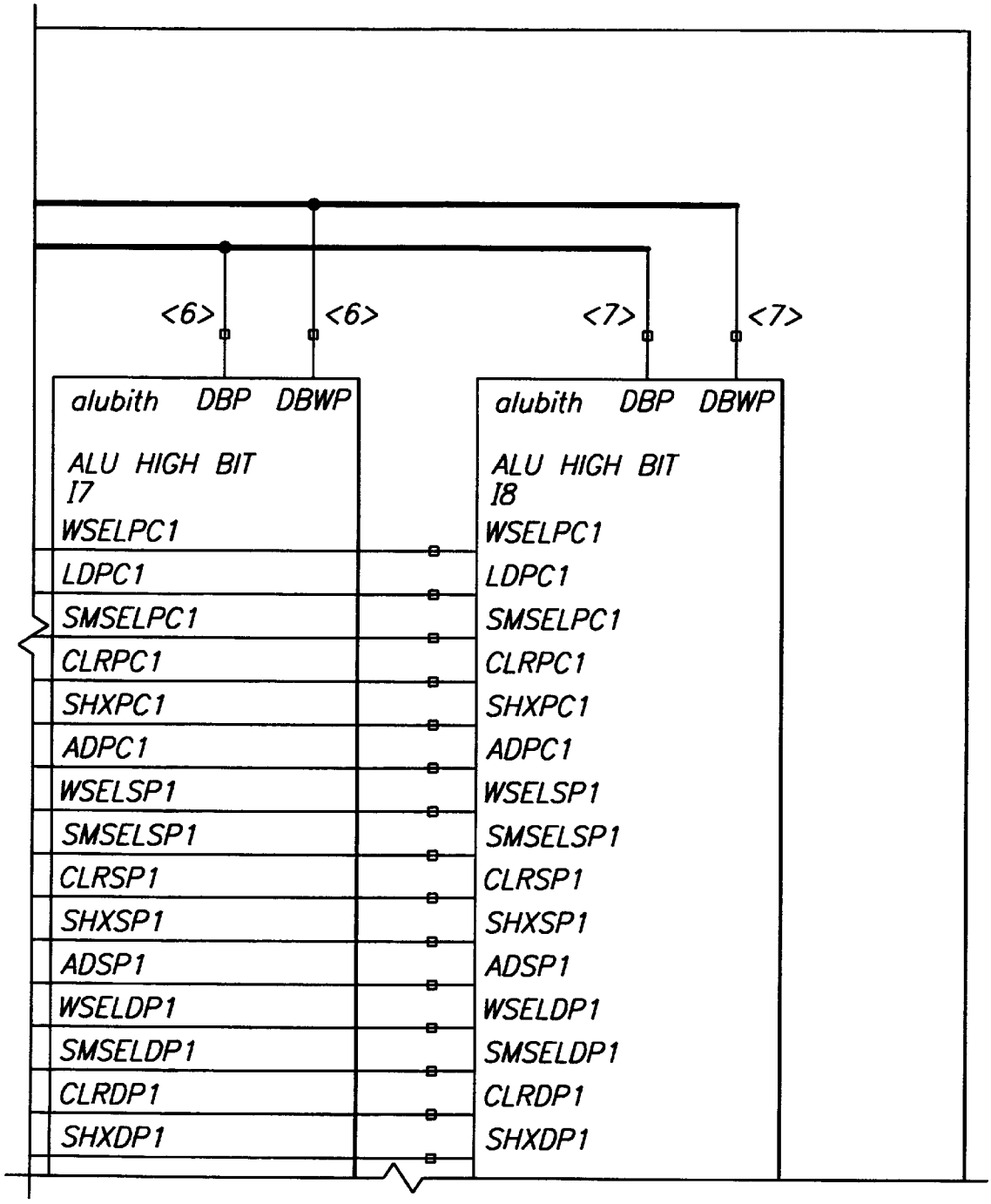

<6>
<6>
<7>
<7>
alubith DBP DBWP
ALU HIGH BIT
I7
WSELPC1
LDPC1
SMSELPC1
CLRPC1
SHXPC1
ADPC1
WSELSP1
SMSELSP1
CLRSP1
SHXSP1
ADSP1
WSELDP1
SMSELDP1
CLRDP1
SHXDP1
alubith DBP DBWP
ALU HIGH BIT
I8
WSELPC1
LDPC1
SMSELPC1
CLRPC1
SHXPC1
ADPC1
WSELSP1
SMSELSP1
CLRSP1
SHXSP1
ADSP1
WSELDP1
SMSELDP1
CLRDP1
SHXDP1

Fig 1.090200

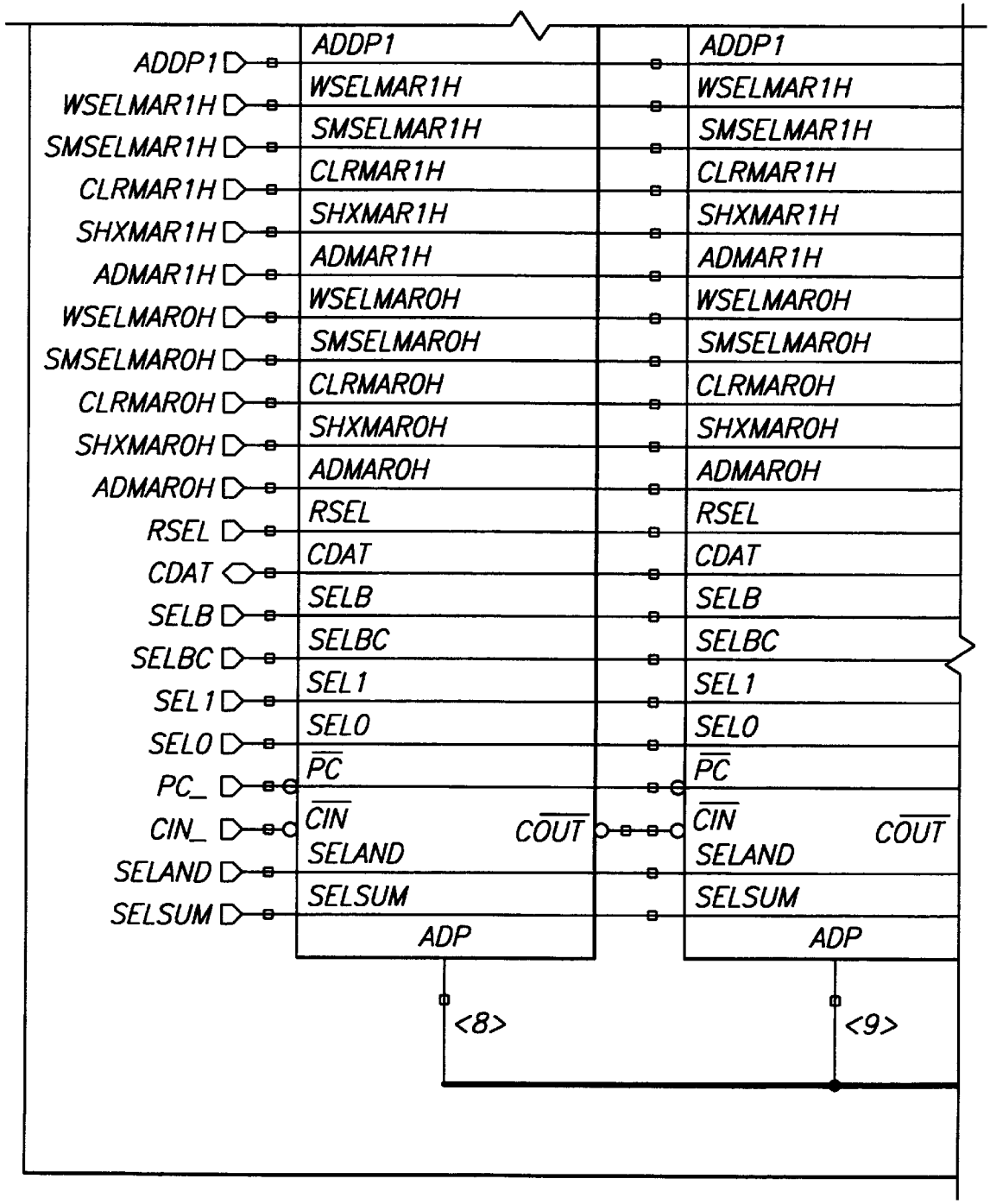


Fig 1.090208A

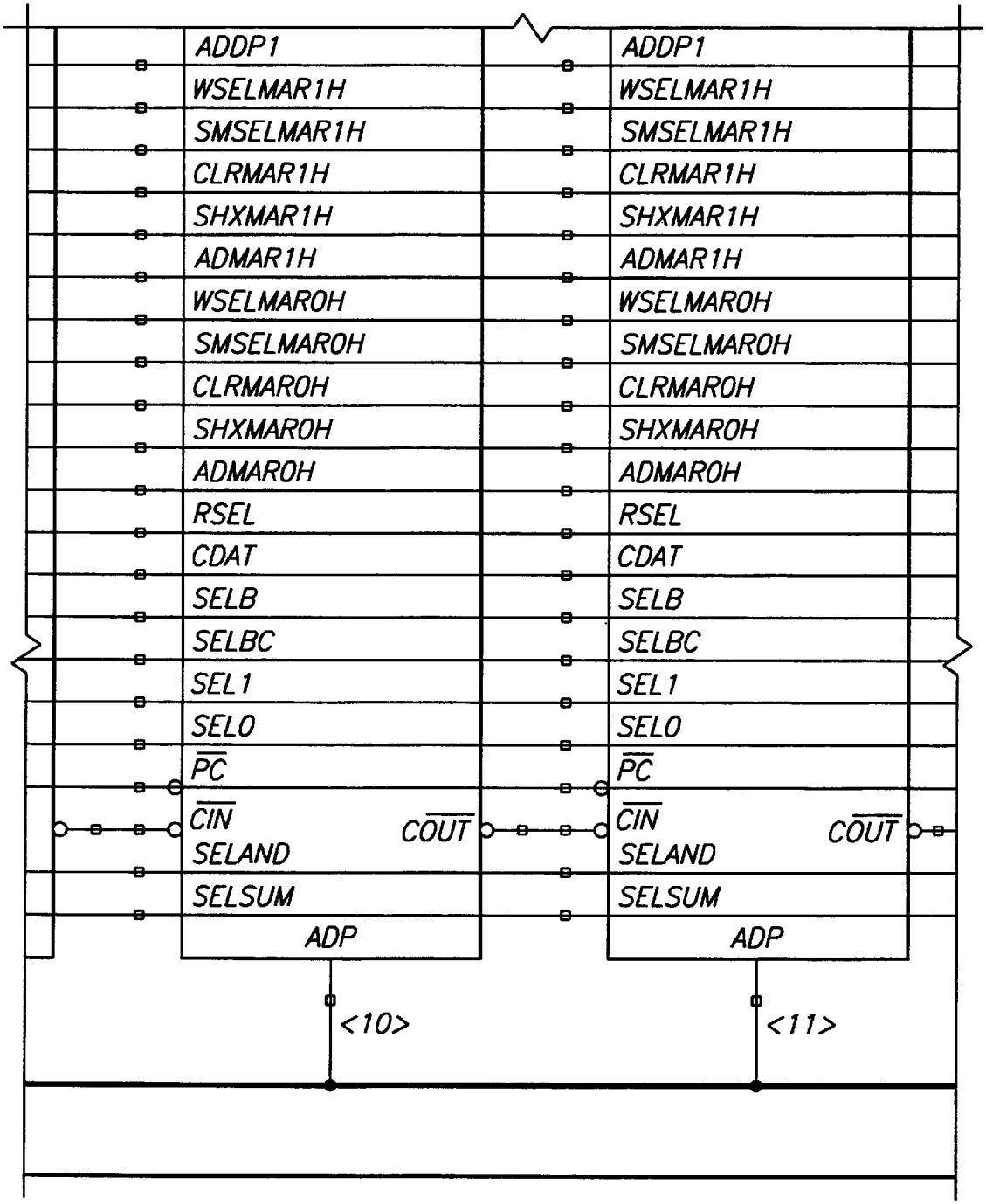

ADDP1
WSELMAR1H
SMSELMAR1H
CLRMAR1H
SHXMAR1H
ADMAR1H
WSELMAROH
SMSELMAROH
CLRMAROH
SHXMAROH
ADMAROH
RSEL
CDAT
SELB
SELBC
SEL1
SEL0
PC
CIN
COUT
SELAND
SELSUM
ADP
<10>
<11>

Fig 1.090288

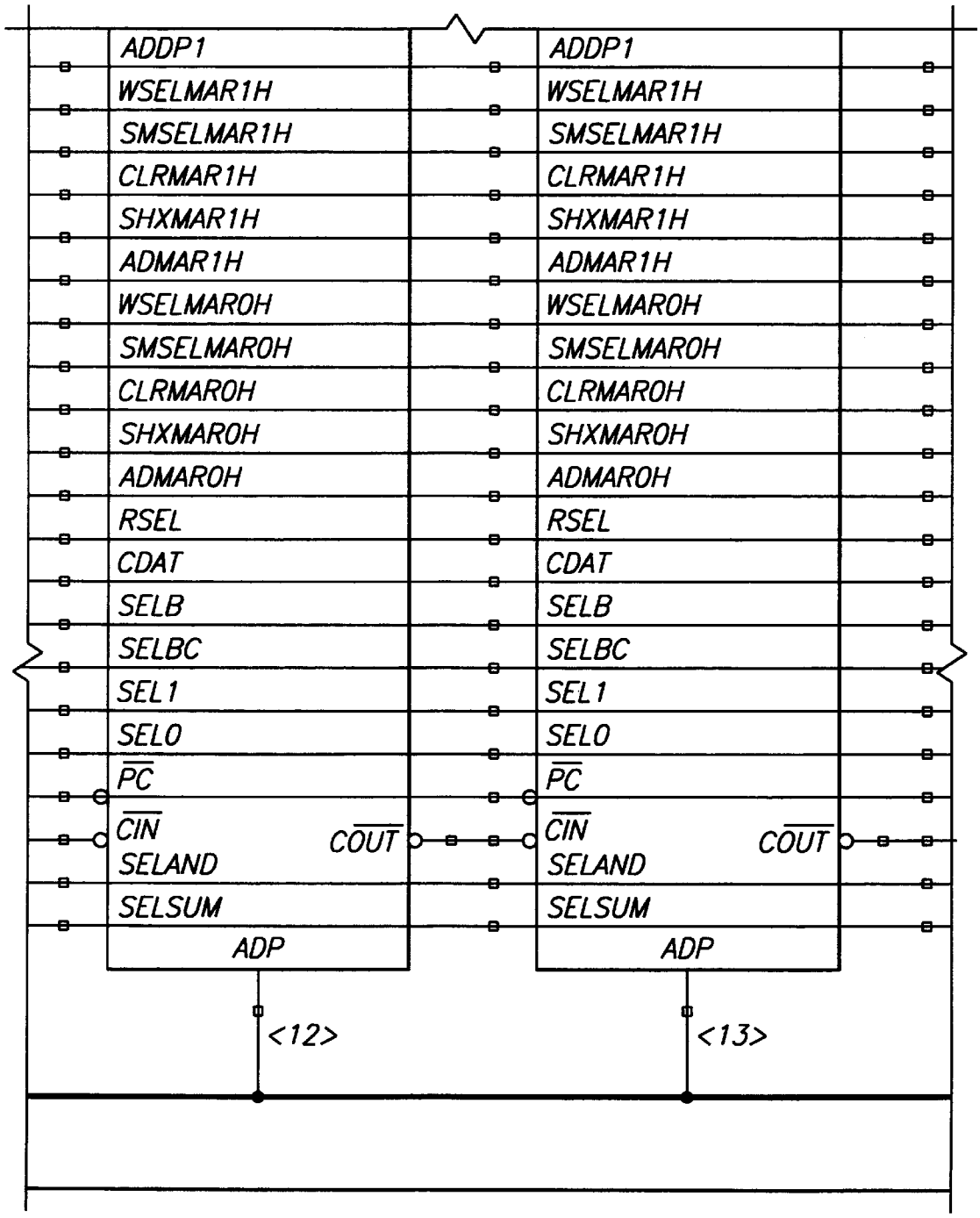


Fig 1.090286C

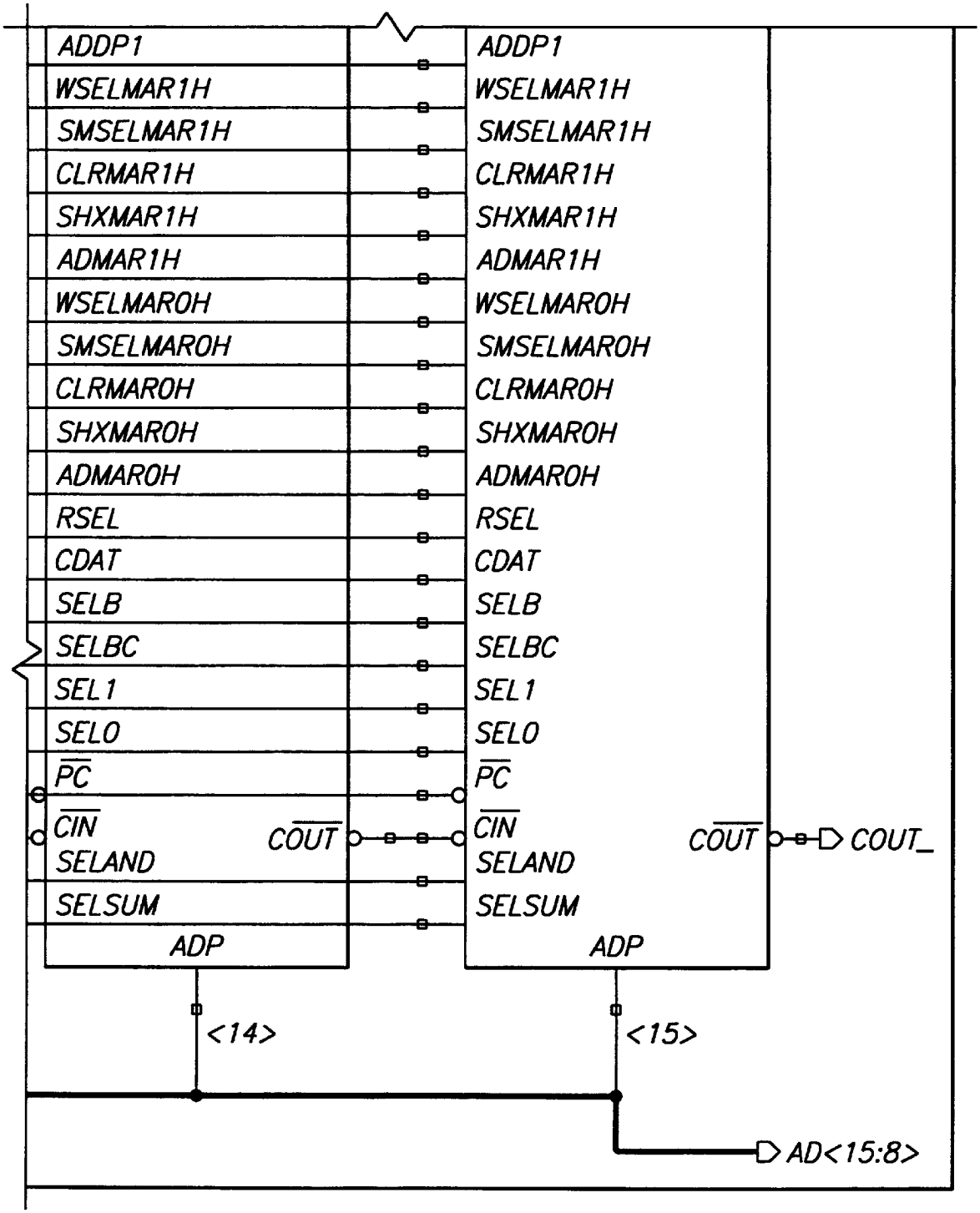

ADDP1
WSELMAR1H
SMSELMAR1H
CLRMAR1H
SHXMAR1H
ADMAR1H
WSELMAROH
SMSELMAROH
CLRMAROH
SHXMAROH
ADMAROH
RSEL
CDAT
SELB
SELBC
SEL1
SELO
PC
CIN
SELAND
COUT
SELSUM
ADP
<14>
<15>
COUT_
AD<15:8>

Fig 1.090280

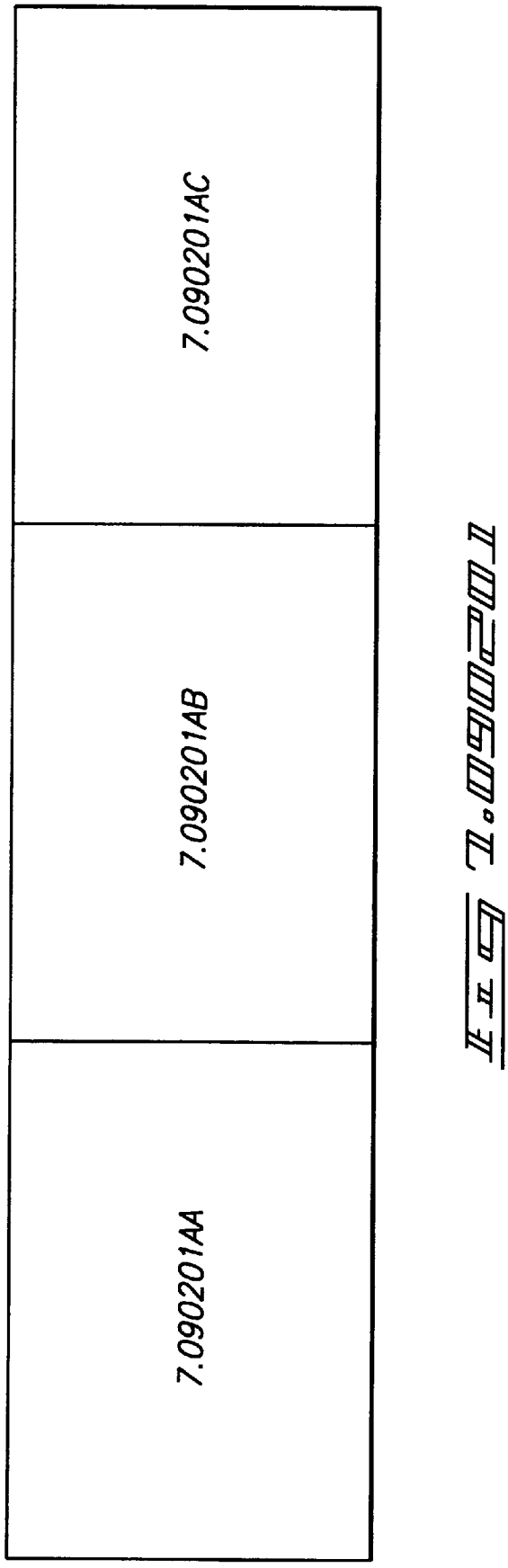


FIG. 7.090201

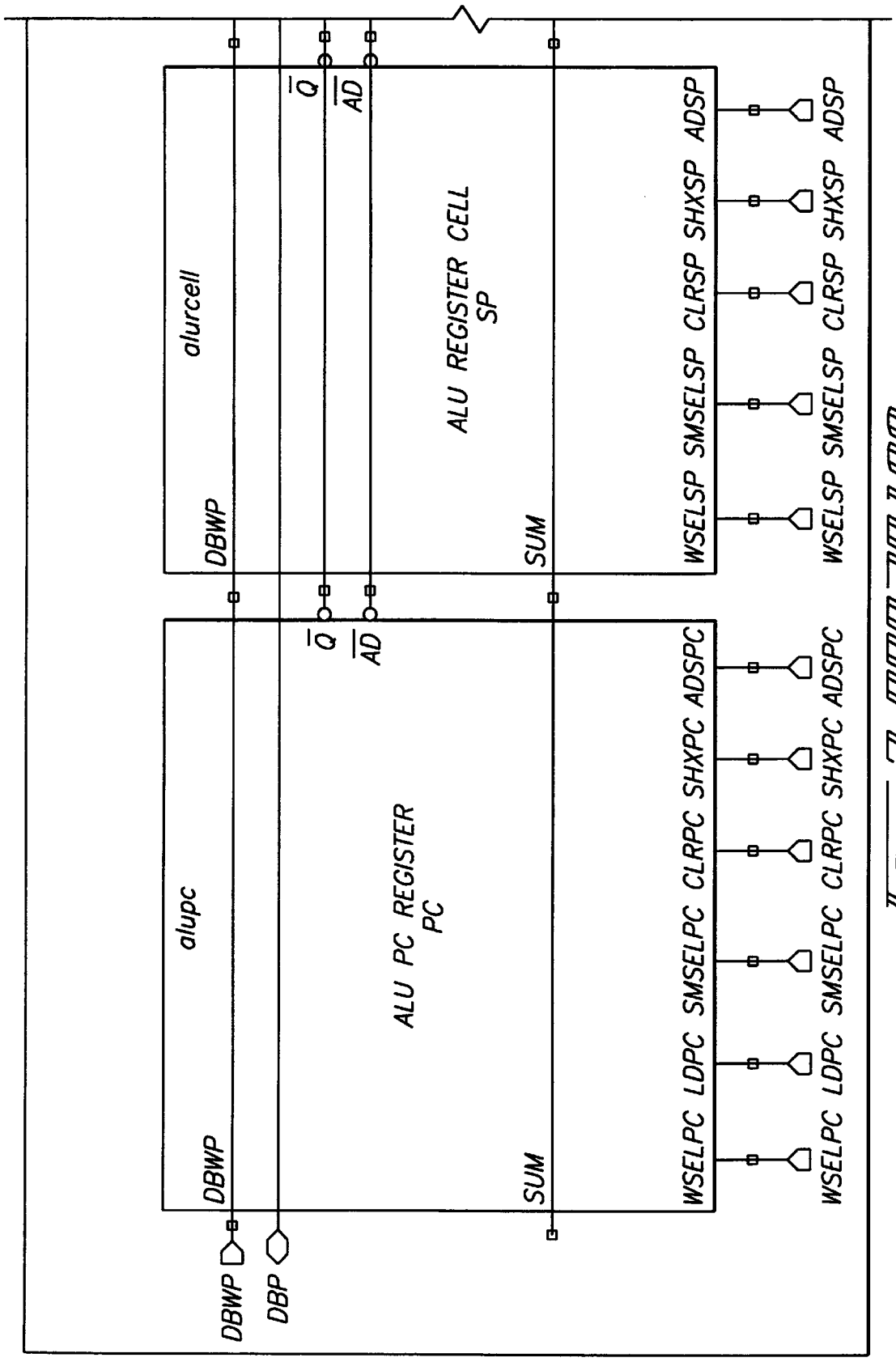
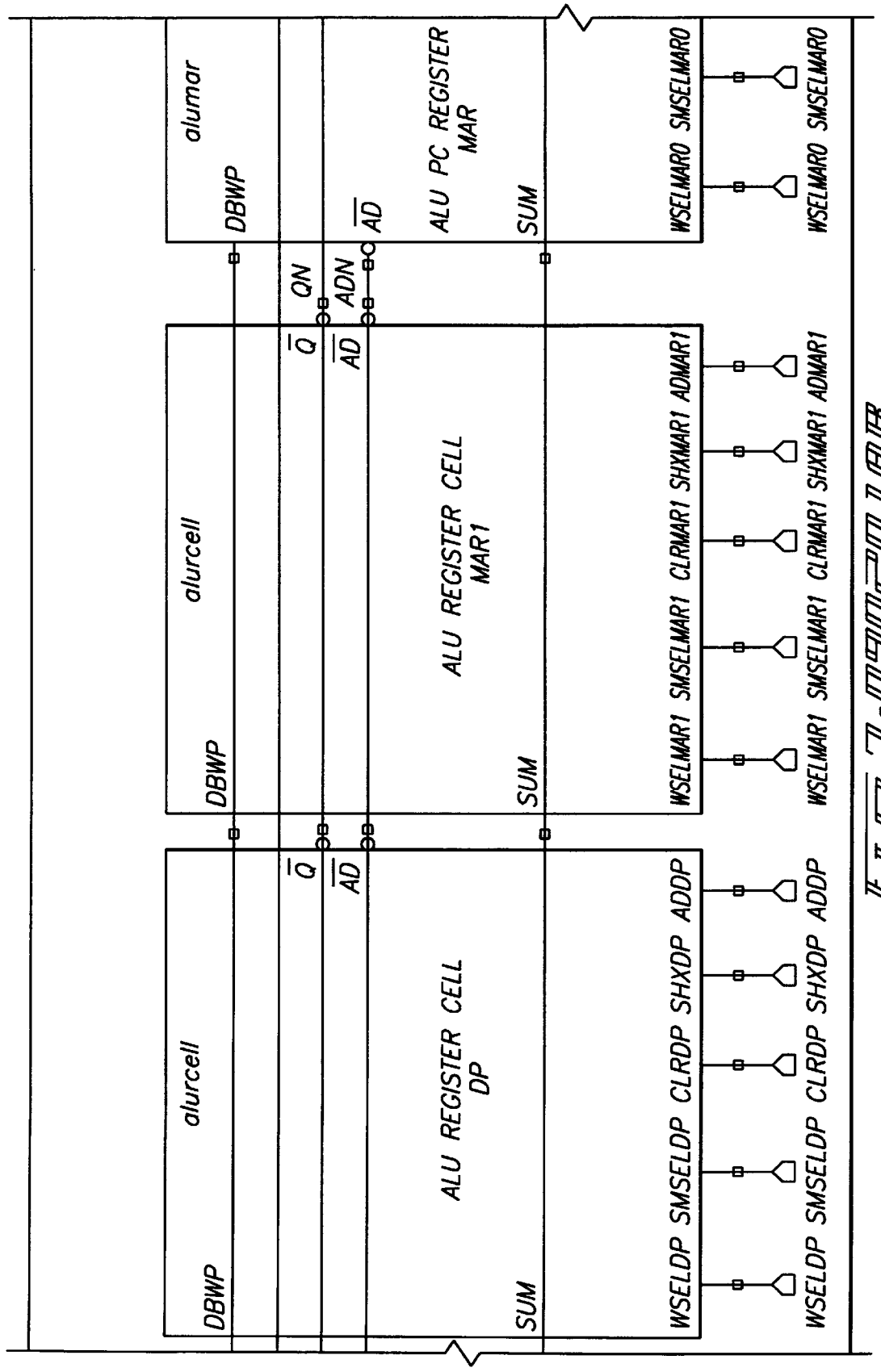

alurcell
DBWP
ALU REGISTER CELL
SP
SUM
Q
AD
WSELSP SMSELSP CLRSP SHXSP ADSP
alupc
DBWP
ALU PC REGISTER
PC
SUM
Q
AD
WSELPC LDPC SMSELPC CLRPC SHXPC ADSPC
DBWP
DBP

FIG. 11A


alumar
DBWP
ALU PC REGISTER MAR
SUM
WSELMAR0 SMSELMAR0
QN
ADN
AD
alurcell
ALU REGISTER CELL MAR1
WSELMAR1 SMSELMAR1 CLRMAR1 SHXMAR1 ADMAR1
alurcell
ALU REGISTER CELL DP
WSELDP SMSELDP CLRDP SHXDP ADDP

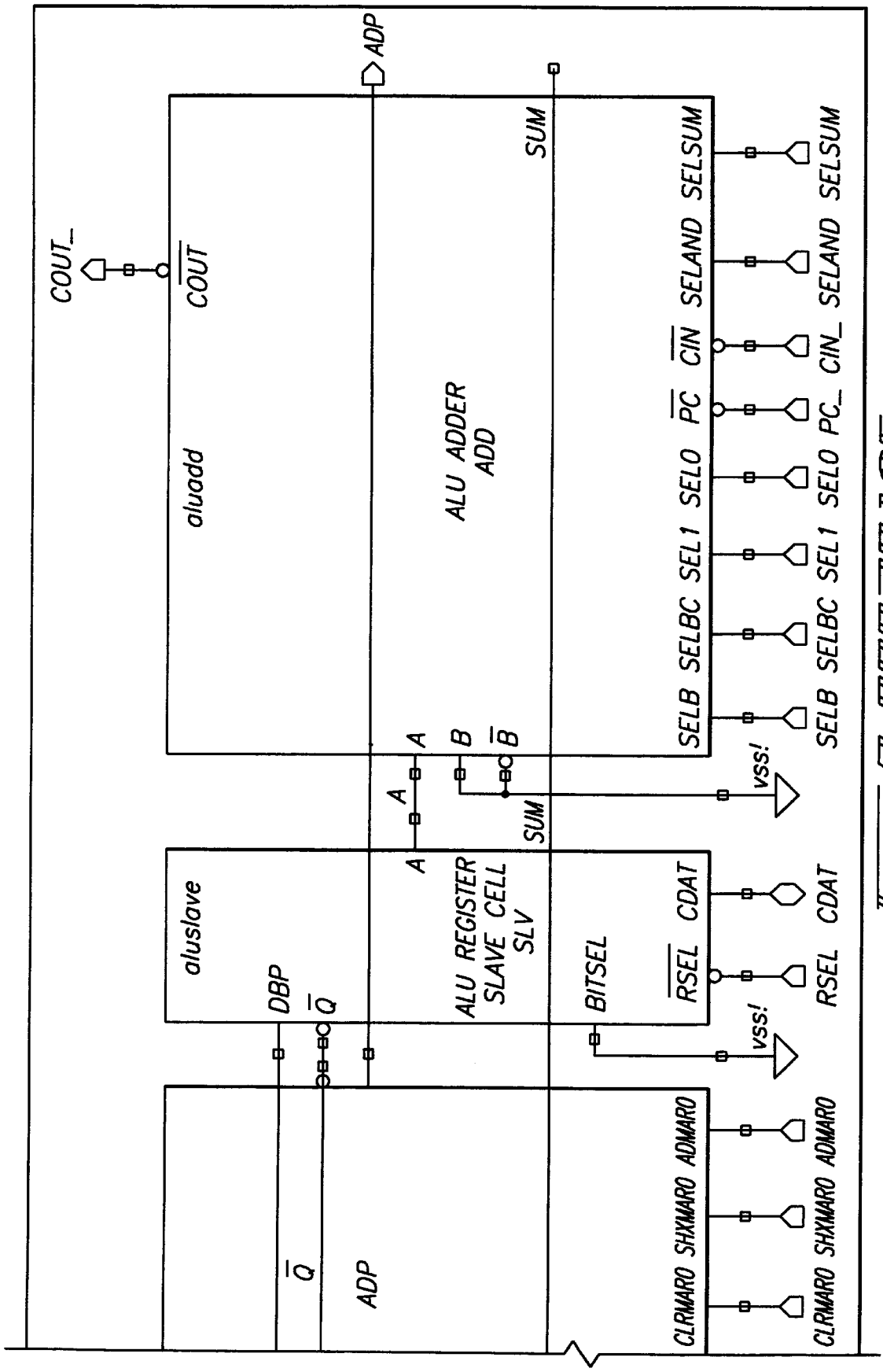

ADP
SUM
COUT_
COUT
aluadd
ALU ADDER
ADD
SELB SELBC SEL1 SELO PC CIN SELAND SELSUM
SELB SELBC SEL1 SELO PC_ CIN_ SELAND SELSUM
A
B
B
vss!
aluslave
DBP
Q
ALU REGISTER
SLAVE CELL
SLV
BITSEL
RSEL CDAT
RSEL CDAT
vss!
Q
ADP
CLRMARO SHXMARO ADMARO
CLRMARO SHXMARO ADMARO

FIG. 901

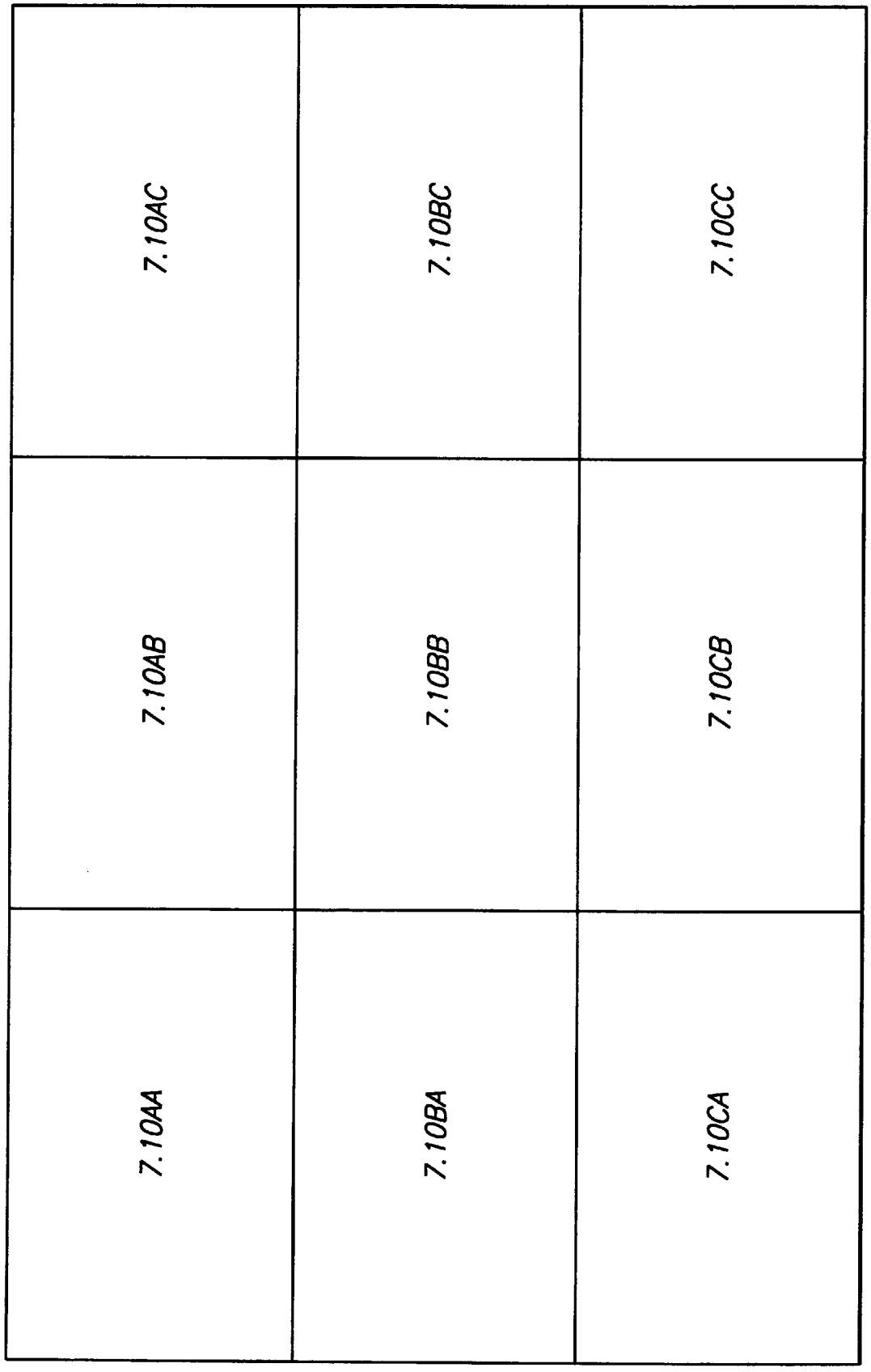


FIG. 7.100

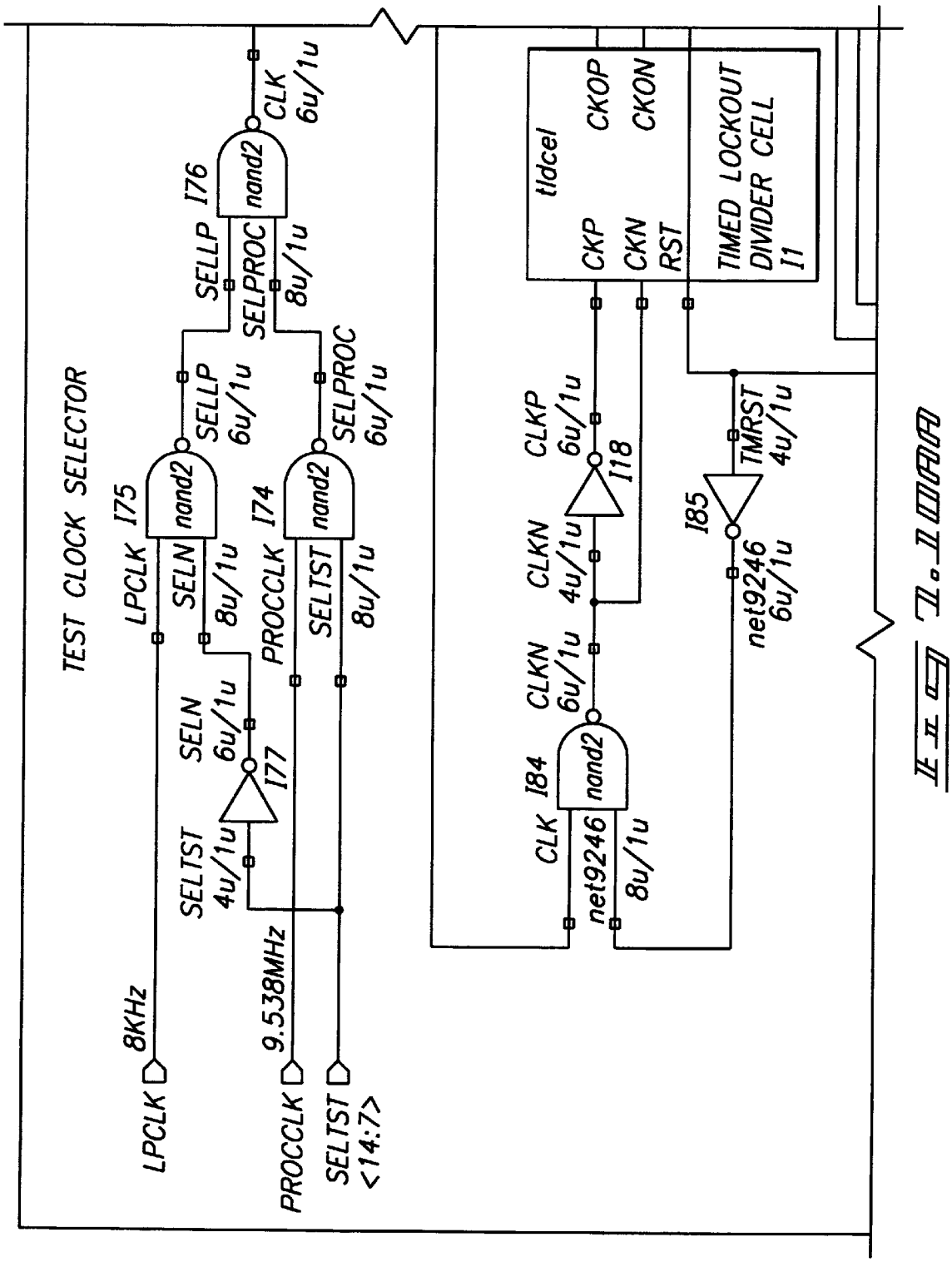

TEST CLOCK SELECTOR
LPCLK
8KHz
PROCCLK
9.538MHz
SELTST<14:7>
I75
I74
I76
I77
I84
I85
I18
nand2
SELN
SELLP
SELPROC
SELTST
LPCLK
PROCCLK
CLK
CLKN
CLKP
TMRST
net9246
4u/1u
6u/1u
8u/1u
tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I1

FIG. 11.00AA

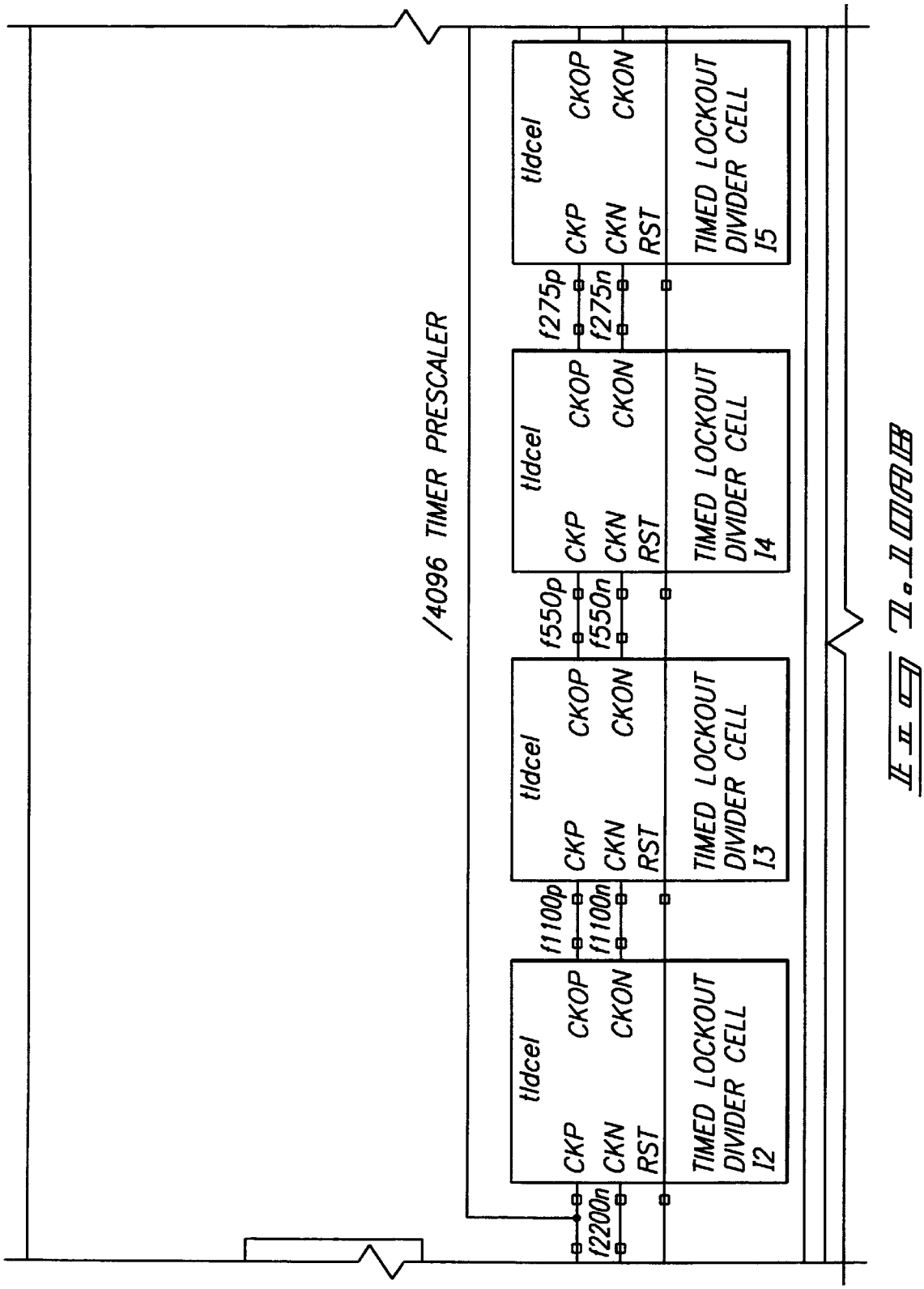

/4096 TIMER PRESCALER
tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I5
I4
I3
I2
f2200n
f1100p
f1100n
f550p
f550n
f275p
f275n

FIG. 11.0048

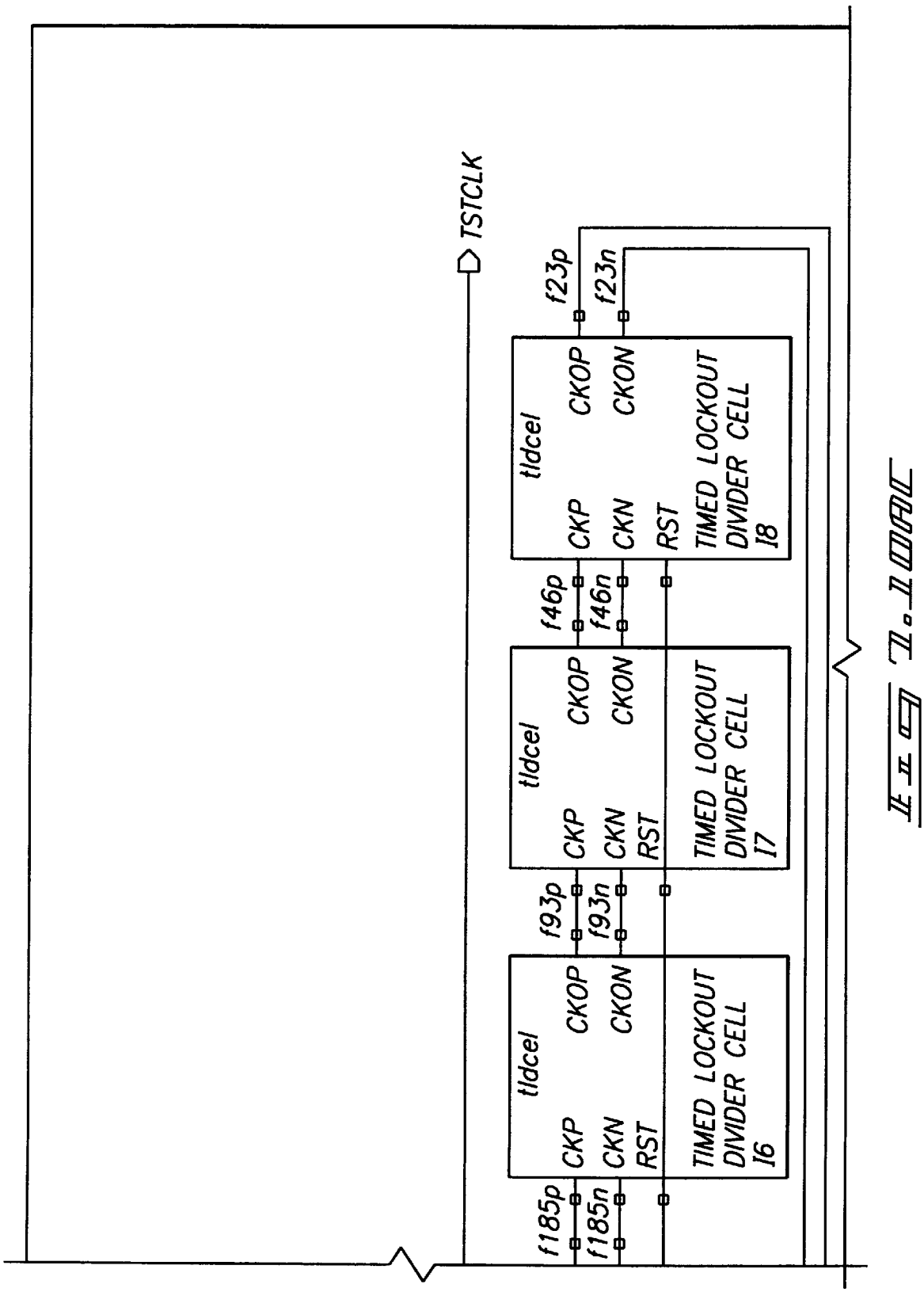

TSTCLK
tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL I6
TIMED LOCKOUT DIVIDER CELL I7
TIMED LOCKOUT DIVIDER CELL I8
f185p
f185n
f93p
f93n
f46p
f46n
f23p
f23n

FIG. 11.00AC

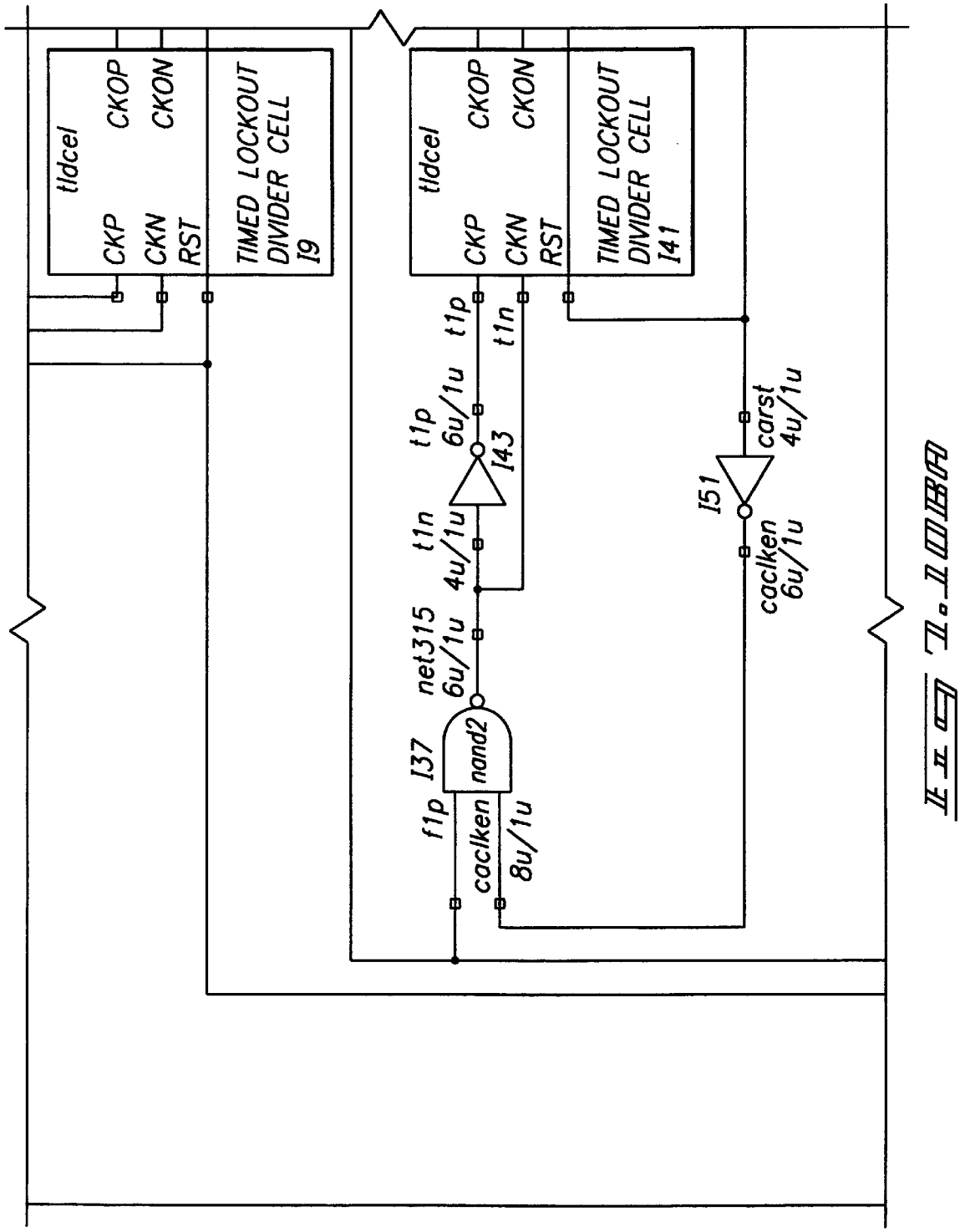

tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL
I9
tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL
I41
t1p
t1n
t1p
6u/1u
I43
t1n
4u/1u
net315
6u/1u
I37
nand2
f1p
caclken
8u/1u
I51
carst
4u/1u
caclken
6u/1u

FIG. 11

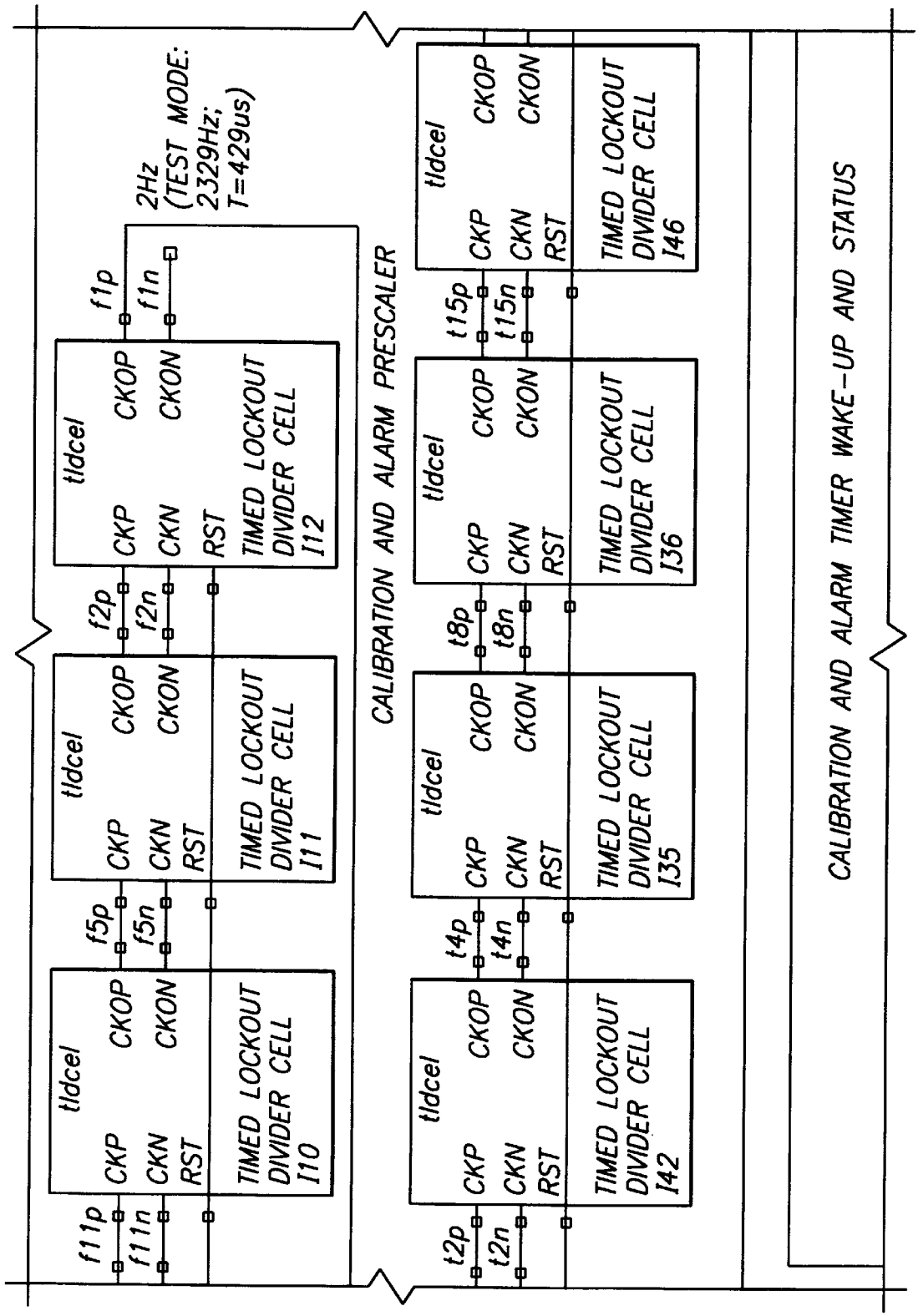

tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL I10
TIMED LOCKOUT DIVIDER CELL I11
TIMED LOCKOUT DIVIDER CELL I12
TIMED LOCKOUT DIVIDER CELL I42
TIMED LOCKOUT DIVIDER CELL I35
TIMED LOCKOUT DIVIDER CELL I36
TIMED LOCKOUT DIVIDER CELL I46
f11p
f11n
f5p
f5n
f2p
f2n
f1p
f1n
t4p
t4n
t8p
t8n
t15p
t15n
t2p
t2n
2Hz (TEST MODE: 2329Hz; T=429us)
CALIBRATION AND ALARM PRESCALER
CALIBRATION AND ALARM TIMER WAKE-UP AND STATUS

FIG. 11

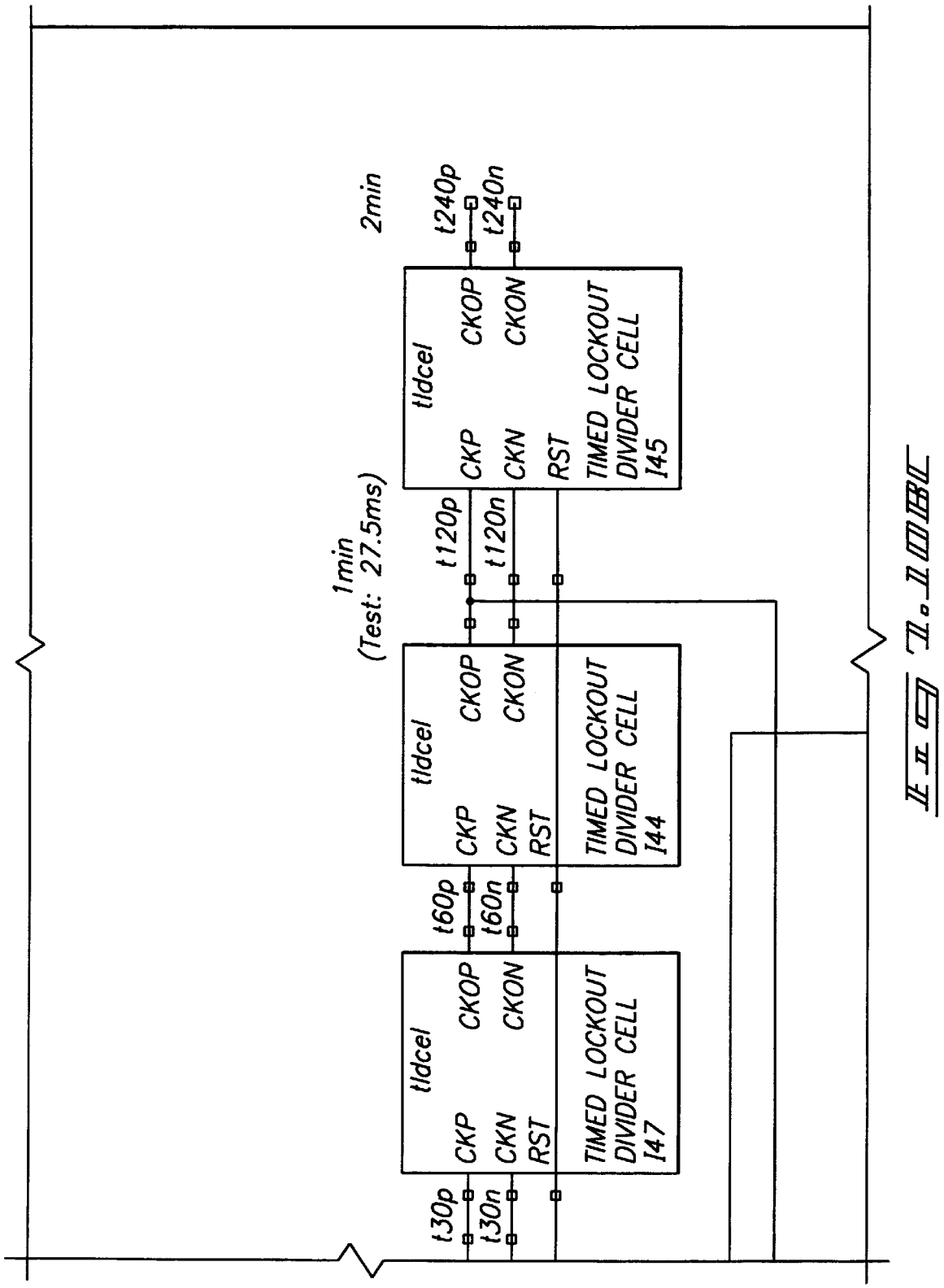
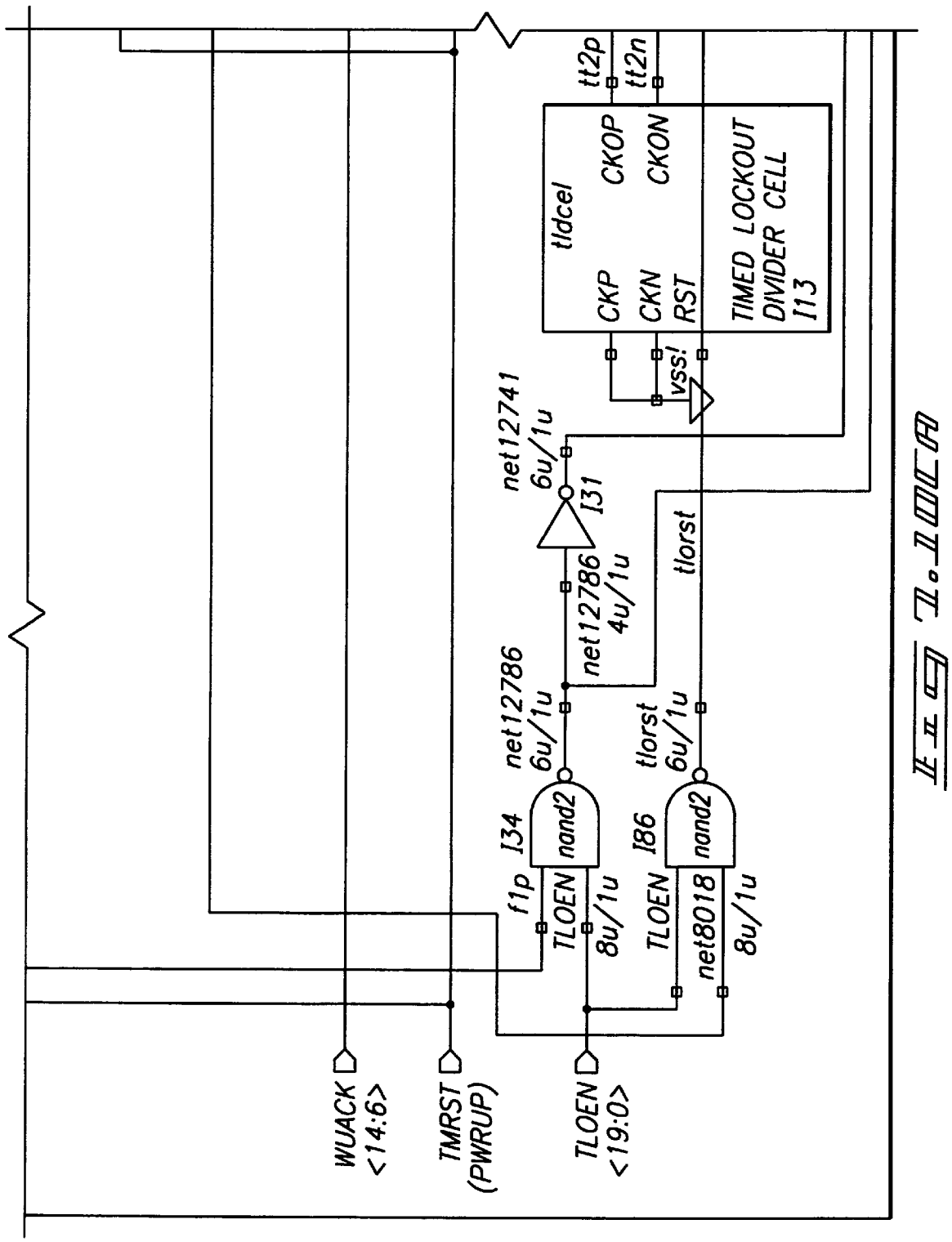

2min
t240p
t240n
tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL 145
1min (Test: 27.5ms)
t120p
t120n
TIMED LOCKOUT DIVIDER CELL 144
t60p
t60n
TIMED LOCKOUT DIVIDER CELL 147
t30p
t30n

FIG. 11.1


tt2p
tt2n
tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL
I13
vss!
net12741
6u/1u
I31
net12786
4u/1u
tlorst
net12786
6u/1u
I34
nand2
f1p
TLOEN
8u/1u
tlorst
6u/1u
I86
nand2
TLOEN
net8018
8u/1u
WUACK <14:6>
TMRST (PWRUP)
TLOEN <19:0>
FIG. 1L

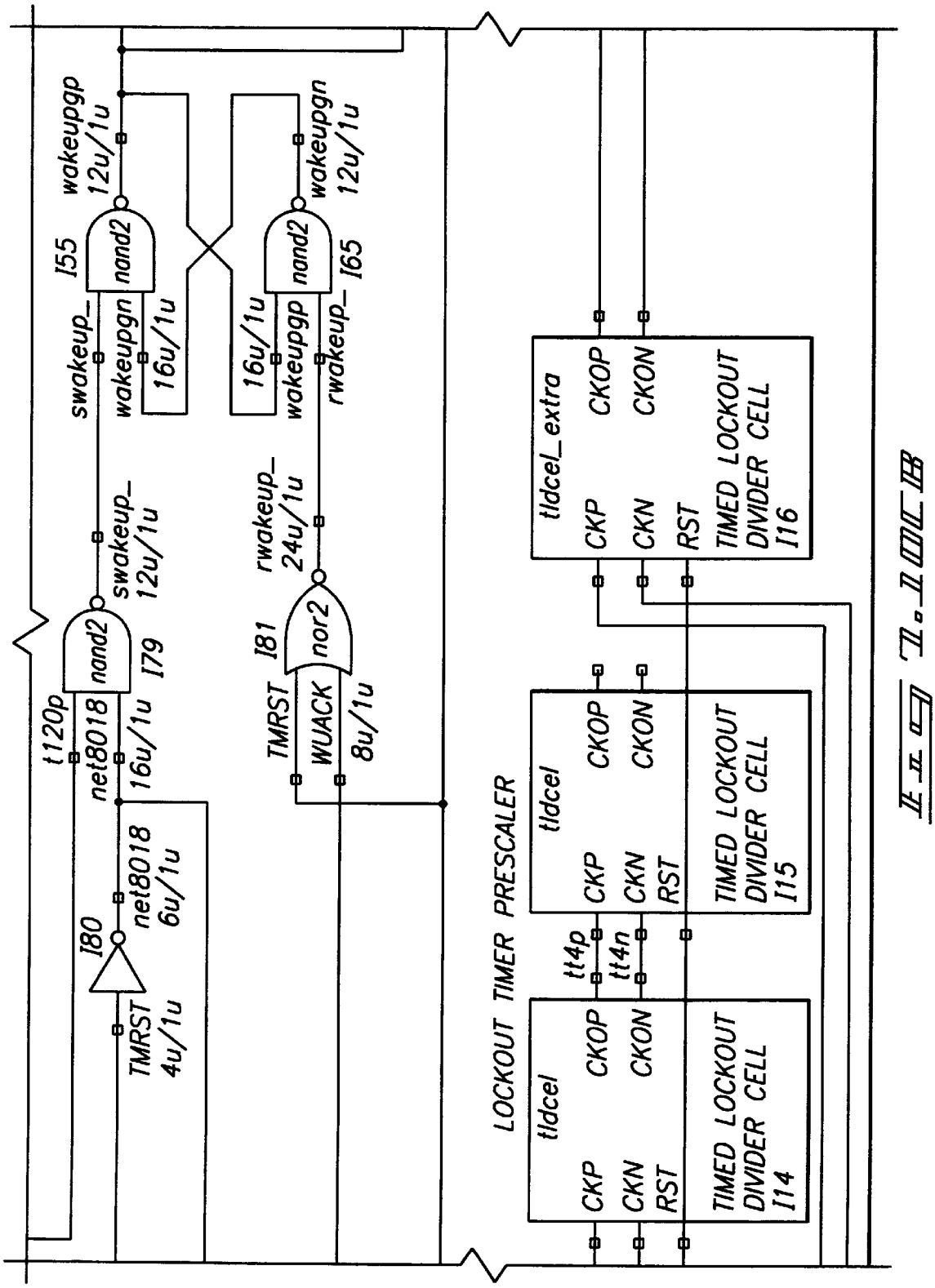

LOCKOUT TIMER PRESCALER
t120p
net8018
16u/1u
I79
nand2
swakeup_
12u/1u
I80
net8018
6u/1u
TMRST
4u/1u
I55
nand2
wakeupgp
12u/1u
swakeup_
wakeupgn
16u/1u
I65
nand2
wakeupgn
12u/1u
16u/1u
wakeupgp
rwakeup_
I81
nor2
rwakeup_
24u/1u
TMRST
WUACK
8u/1u
tt4p
tt4n
tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I14
I15
tldcel_extra
I16

FIG. 1100B

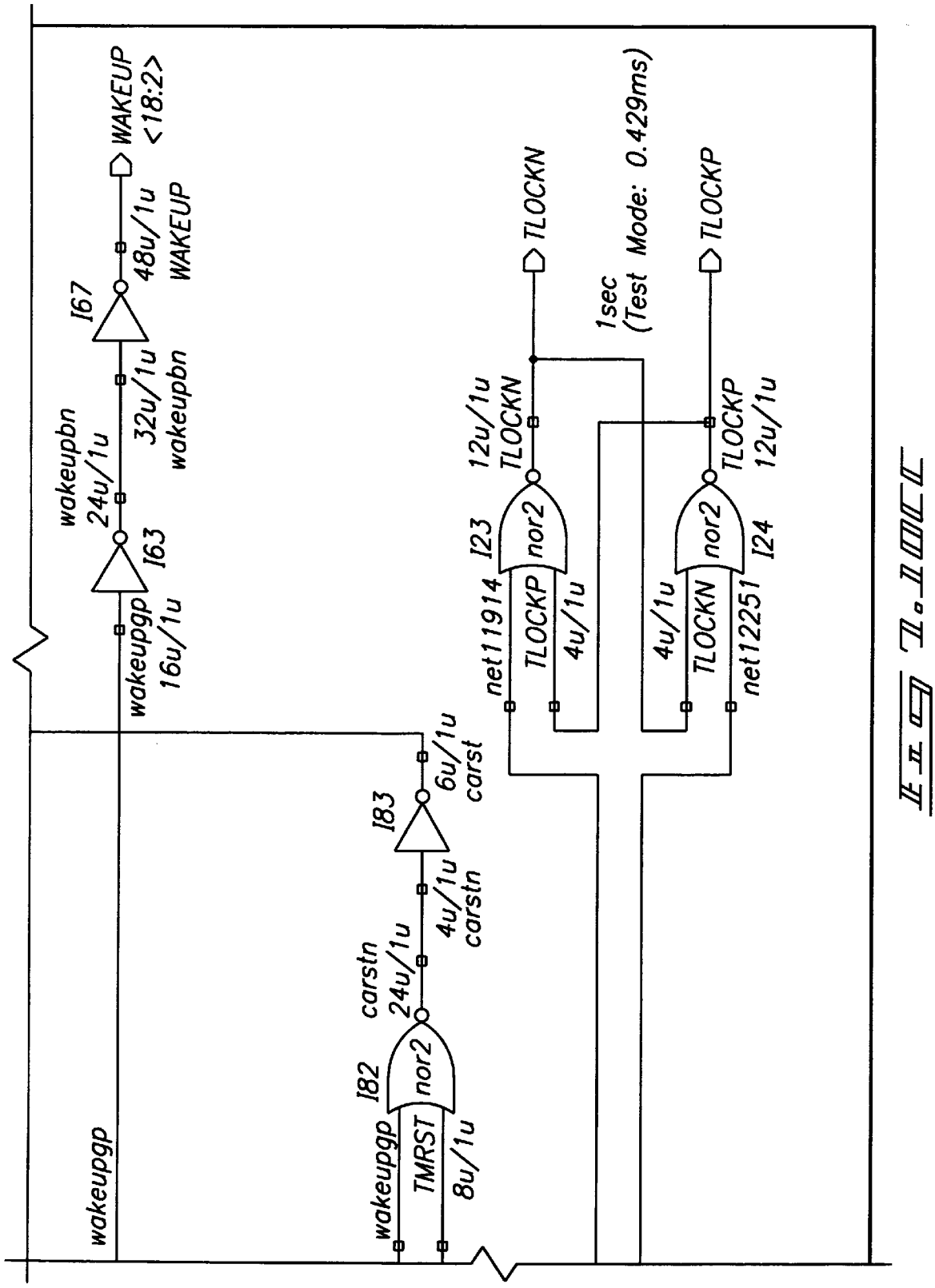

WAKEUP <18:2>
48u/1u
WAKEUP
I67
32u/1u
wakeupbn
wakeupbn
24u/1u
I63
wakeupgp
16u/1u
wakeupgp
TLOCKN
1sec (Test Mode: 0.429ms)
TLOCKP
12u/1u
TLOCKN
I23
nor2
net11914
TLOCKP
4u/1u
4u/1u
TLOCKN
nor2
I24
net12251
TLOCKP
12u/1u
6u/1u
carst
I83
4u/1u
carstn
carstn
24u/1u
I82
nor2
wakeupgp
TMRST
8u/1u

FIG. 11,001E

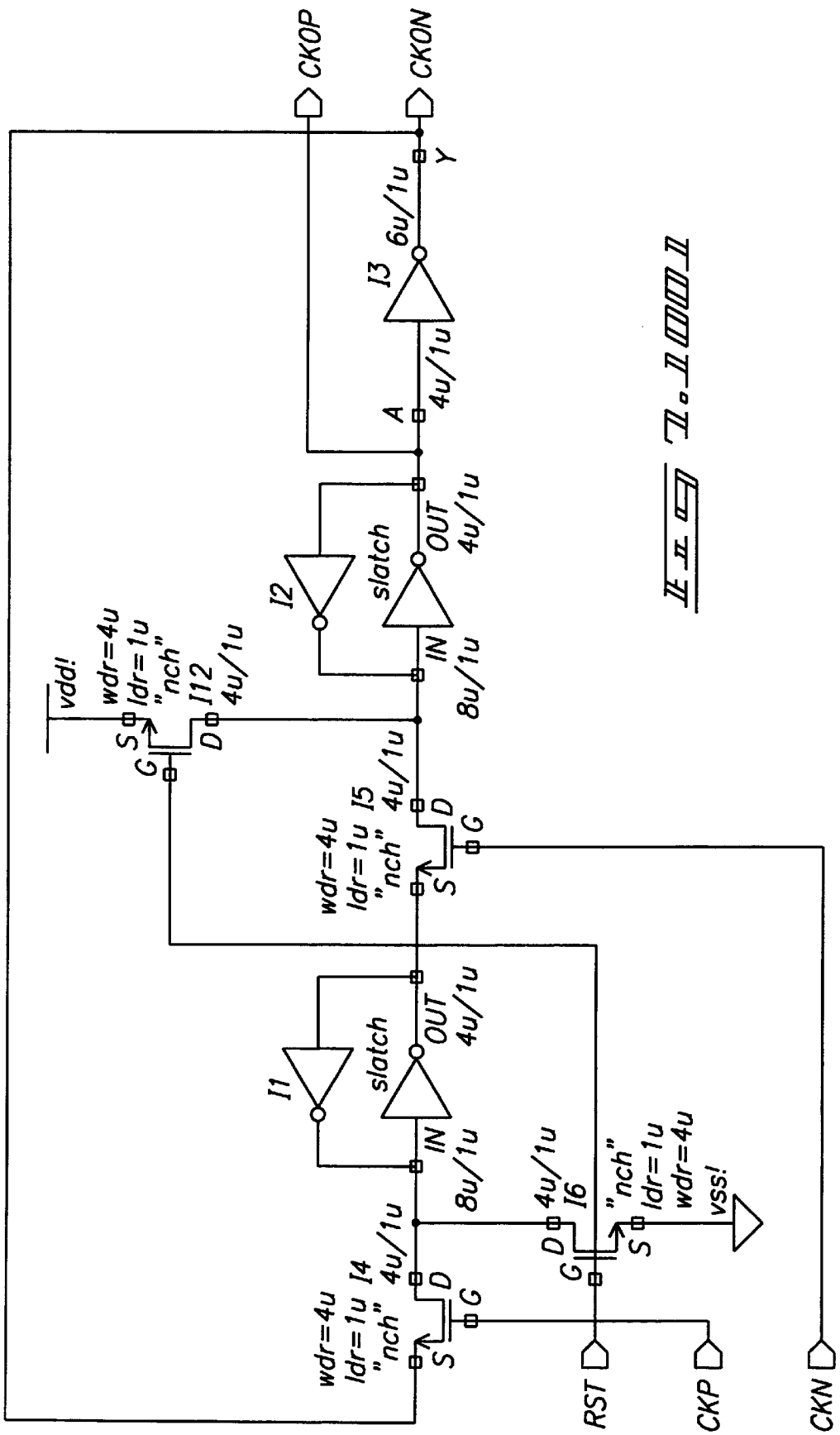

CK0P
CK0N
Y
I3 6u/1u
A
4u/1u
I2
slatch
OUT
4u/1u
IN
8u/1u
vdd!
wdr=4u
ldr=1u
"nch"
I12
4u/1u
S
D
G
I5
4u/1u
wdr=4u
ldr=1u
"nch"
I1
slatch
OUT
4u/1u
IN
8u/1u
4u/1u
I6
"nch"
ldr=1u
wdr=4u
vss!
I4
4u/1u
wdr=4u
ldr=1u
"nch"
RST
CKP
CKN

FIG. 11.0011

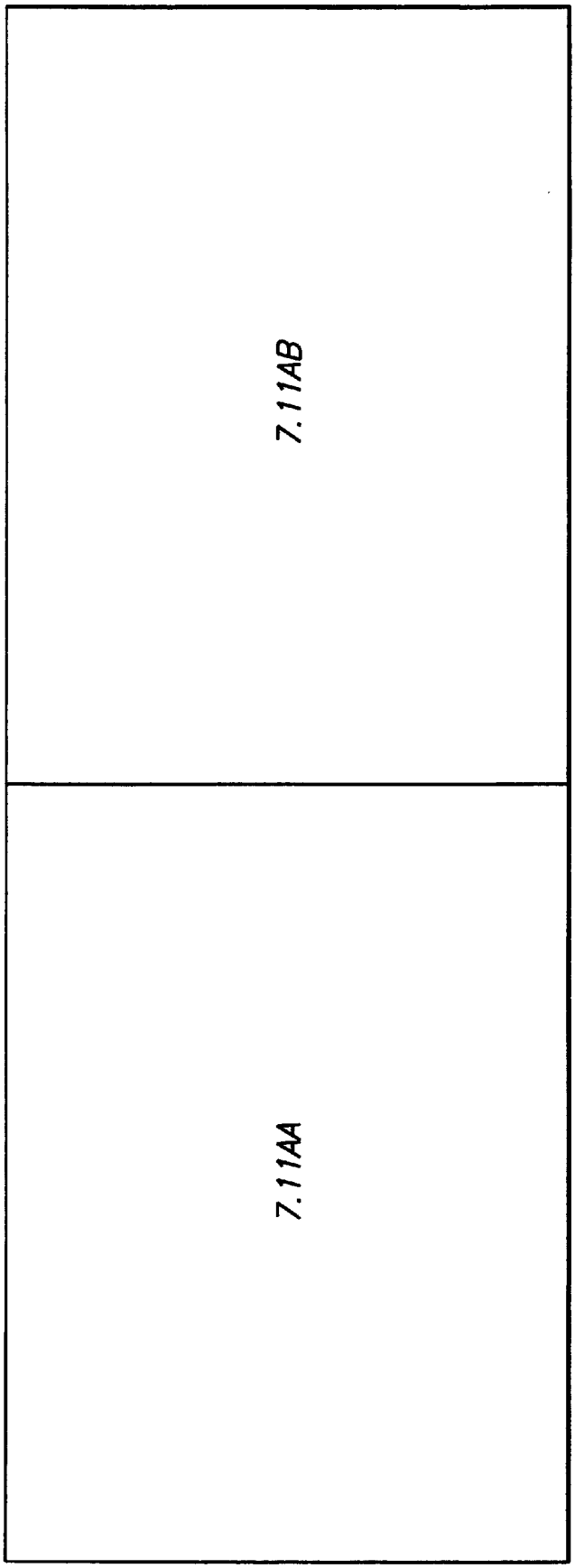


FIG. 711

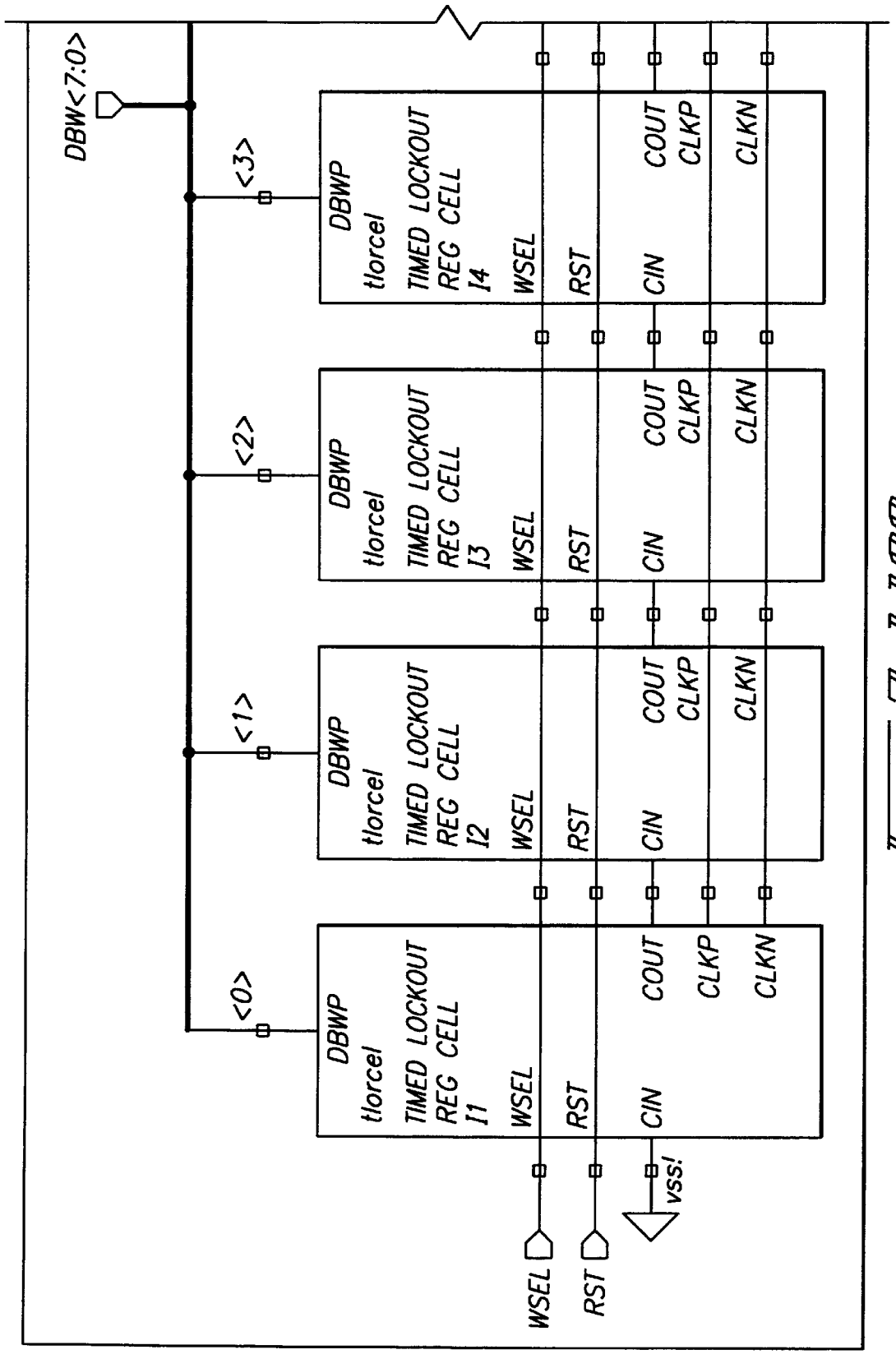

DBW<7:0>
<3>
<2>
<1>
<0>
DBWP
tlorcel
TIMED LOCKOUT
REG CELL
I4
I3
I2
I1
WSEL
RST
CIN
COUT
CLKP
CLKN
vss!

FIG. 11.11A

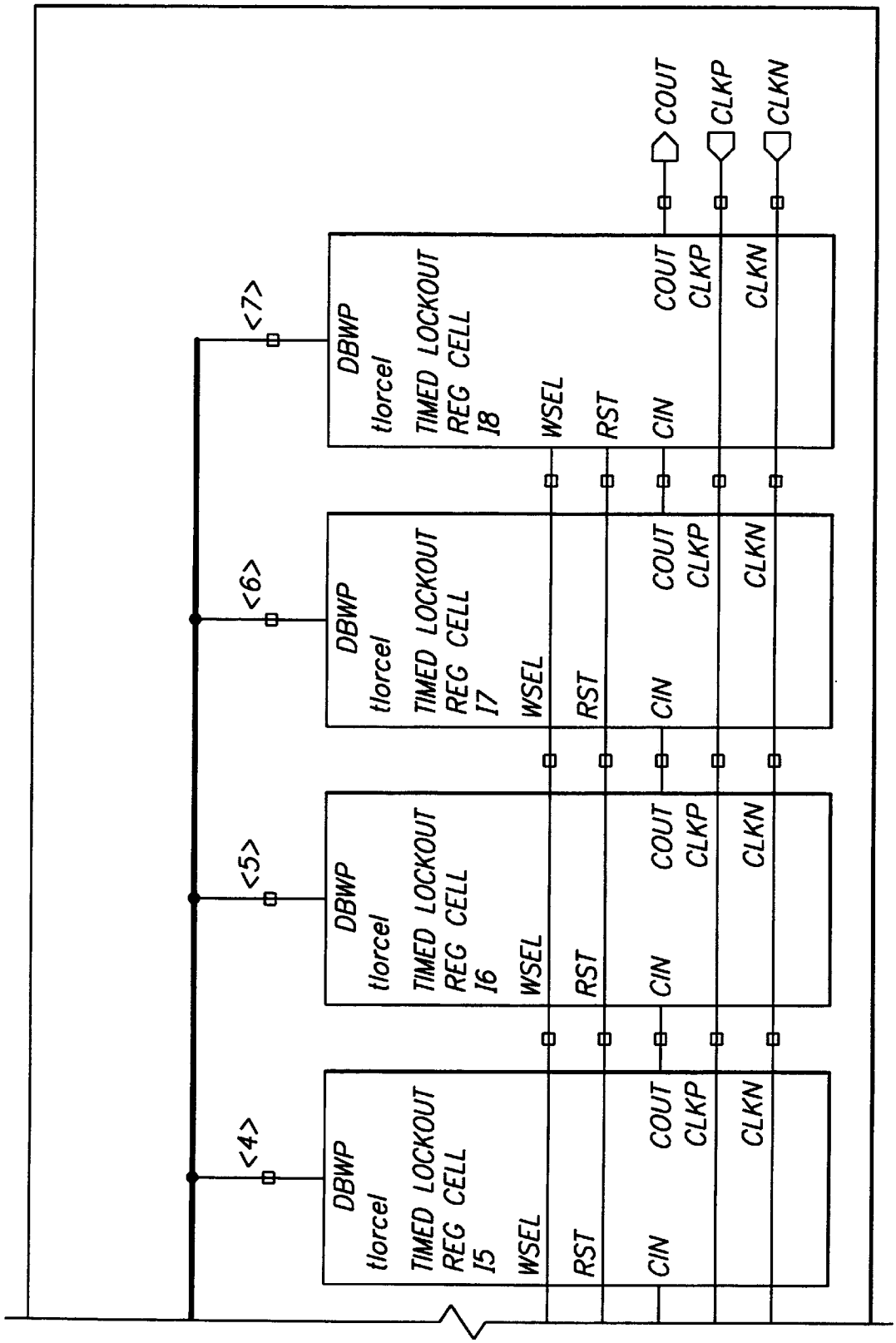

<4>
<5>
<6>
<7>
DBWP
tlorcel
TIMED LOCKOUT
REG CELL
I5
I6
I7
I8
WSEL
RST
CIN
COUT
CLKP
CLKN

FIG. 11A

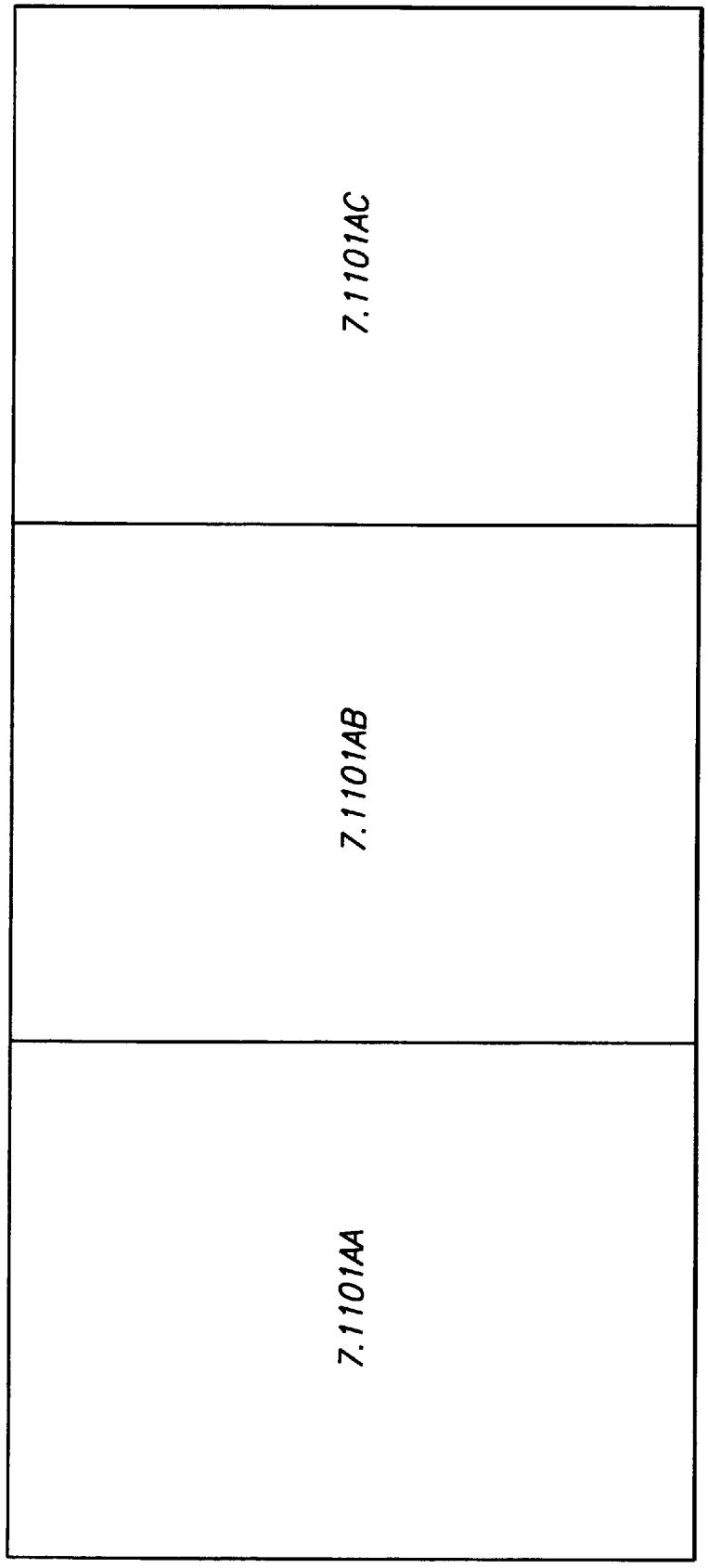


FIG 7.1101

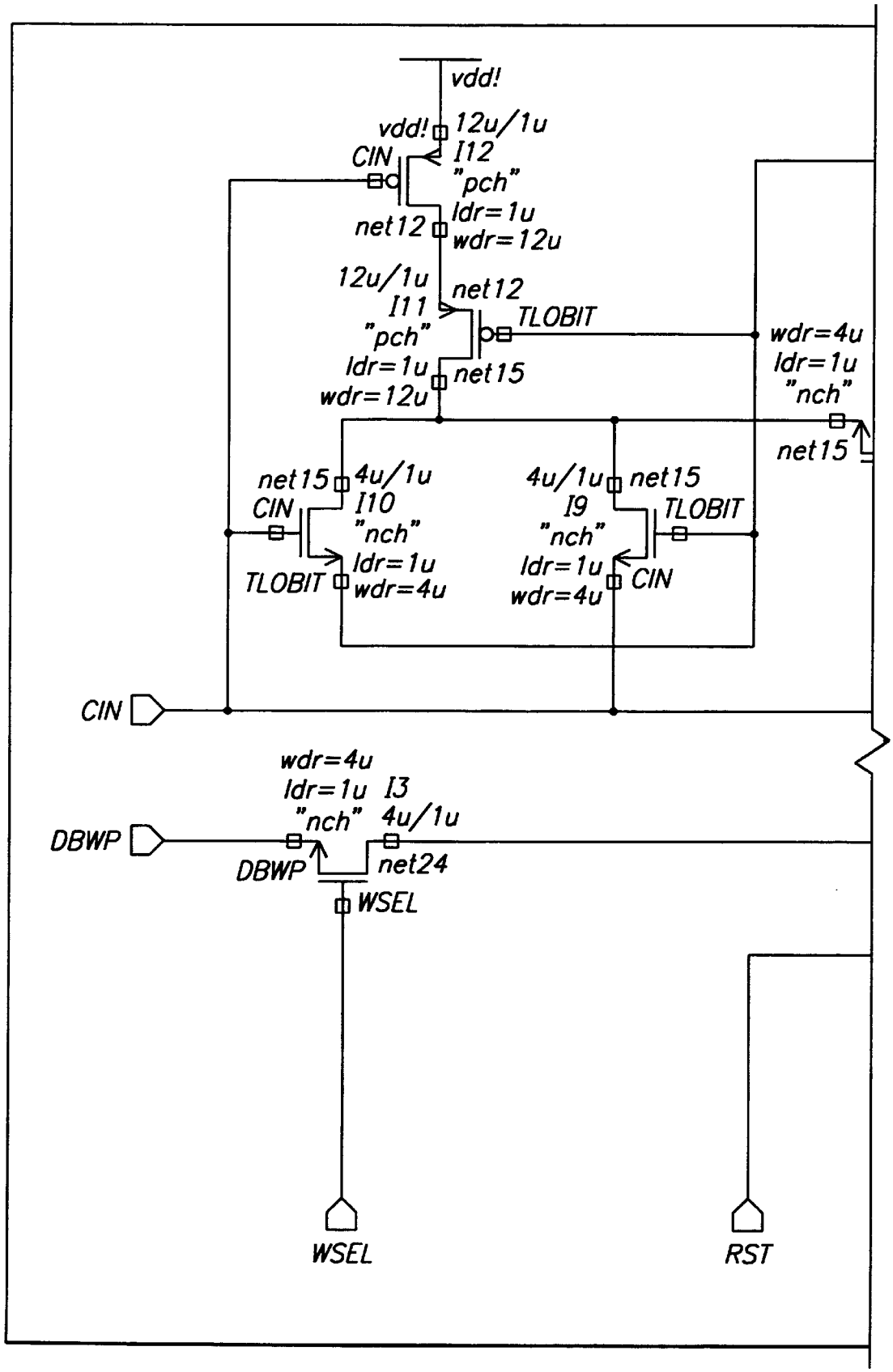

vdd!
vdd!
12u/1u
I12
"pch"
ldr=1u
wdr=12u
CIN
net12
12u/1u
I11
"pch"
ldr=1u
wdr=12u
net12
TLOBIT
net15
wdr=4u
ldr=1u
"nch"
net15
net15
4u/1u
I10
"nch"
ldr=1u
wdr=4u
CIN
TLOBIT
4u/1u
I9
"nch"
ldr=1u
wdr=4u
net15
TLOBIT
CIN
CIN
wdr=4u
ldr=1u
"nch"
I3
4u/1u
DBWP
DBWP
net24
WSEL
WSEL
RST

Fig 7.1101AA

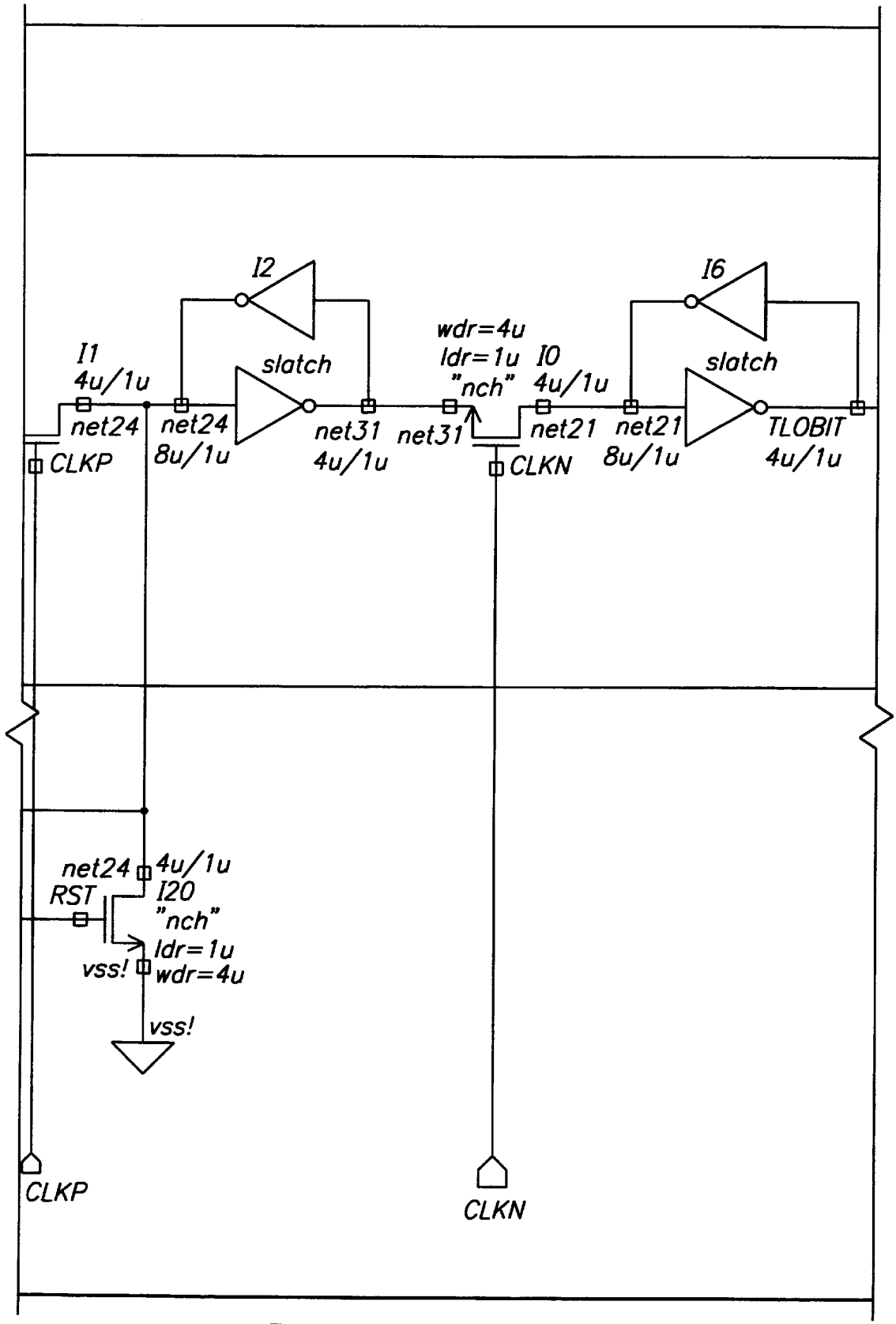

I2
I6
wdr=4u
ldr=1u
"nch"
I0
4u/1u
I1
4u/1u
slatch
slatch
net24
net24
8u/1u
net31
4u/1u
net31
net21
net21
8u/1u
TLOBIT
4u/1u
CLKP
CLKN
net24
4u/1u
RST
I20
"nch"
ldr=1u
vss!
wdr=4u
vss!
CLKP
CLKN

Fig 7.1118B

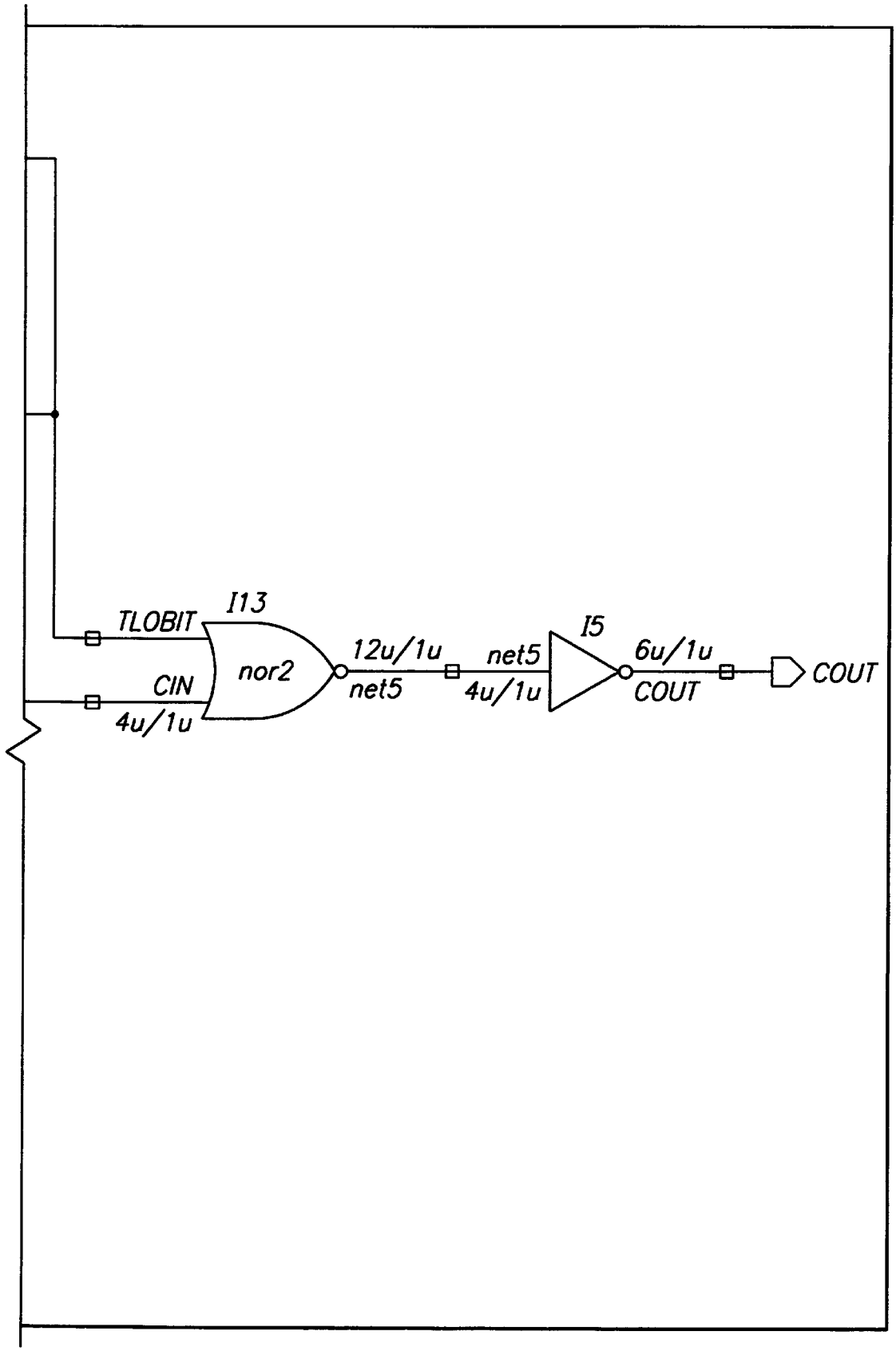

TLOBIT
CIN
4u/1u
I13
nor2
12u/1u
net5
net5
4u/1u
I5
6u/1u
COUT
COUT

Fig 7.1101AC

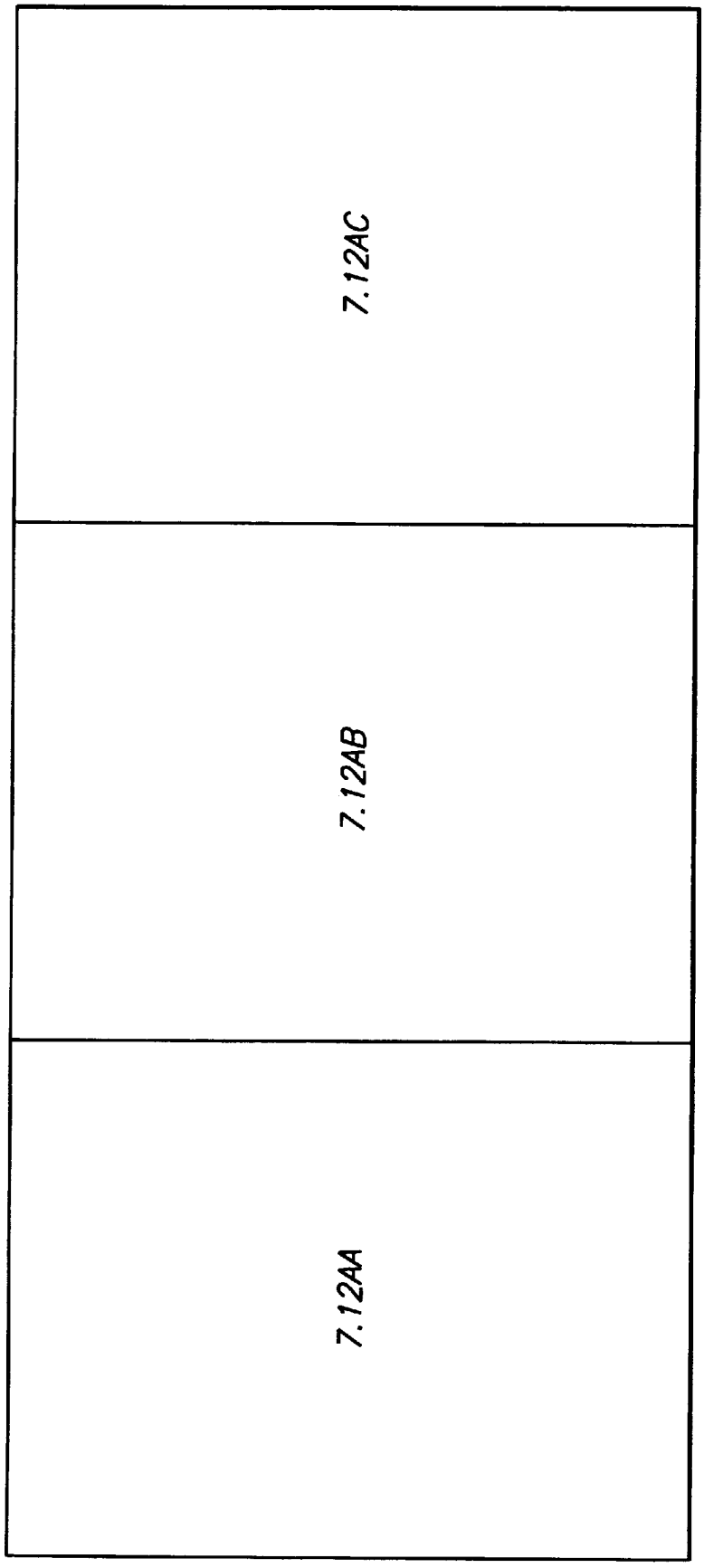


FIG. 7.12

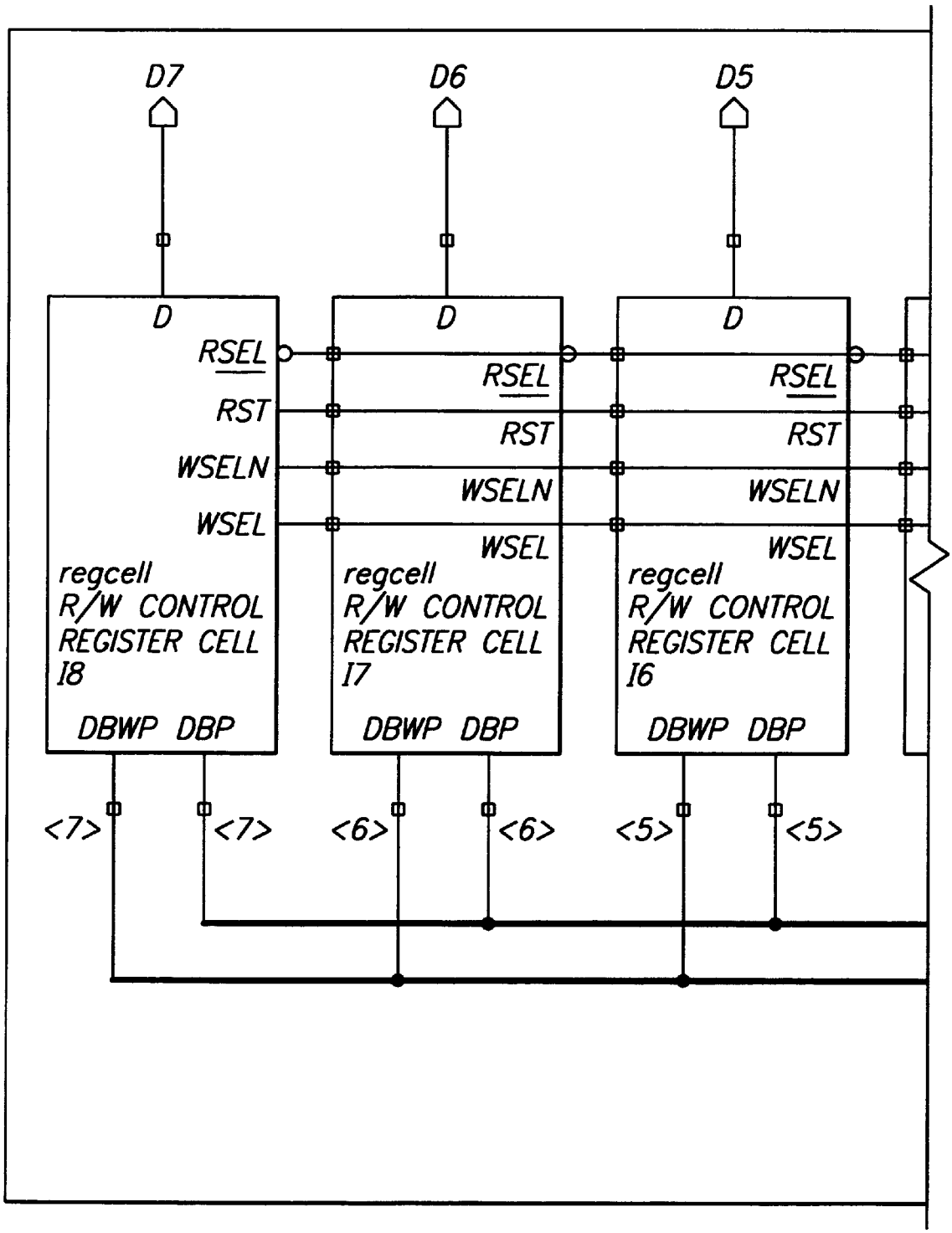

D7
D6
D5
D
D
D
RSEL
RST
WSELN
WSEL
RSEL
RST
WSELN
WSEL
RSEL
RST
WSELN
WSEL
regcell
R/W CONTROL
REGISTER CELL
I8
DBWP DBP
regcell
R/W CONTROL
REGISTER CELL
I7
DBWP DBP
regcell
R/W CONTROL
REGISTER CELL
I6
DBWP DBP
<7>
<7>
<6>
<6>
<5>
<5>

Fig 1.12AA

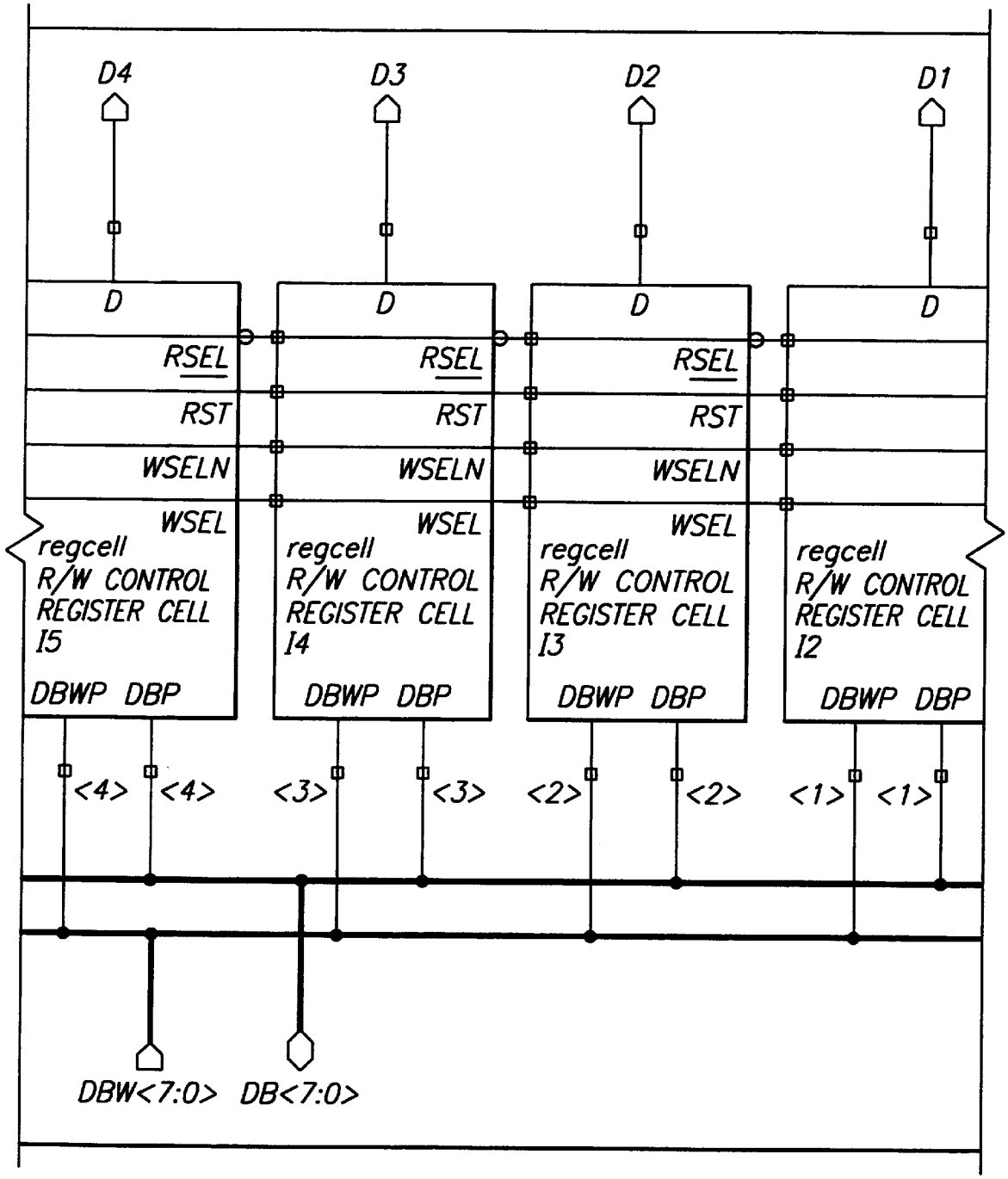

D4
D3
D2
D1
D
RSEL
RST
WSELN
WSEL
regcell
R/W CONTROL
REGISTER CELL
I5
I4
I3
I2
DBWP DBP
<4>
<3>
<2>
<1>
DBW<7:0>
DB<7:0>

Fig 1.12AB

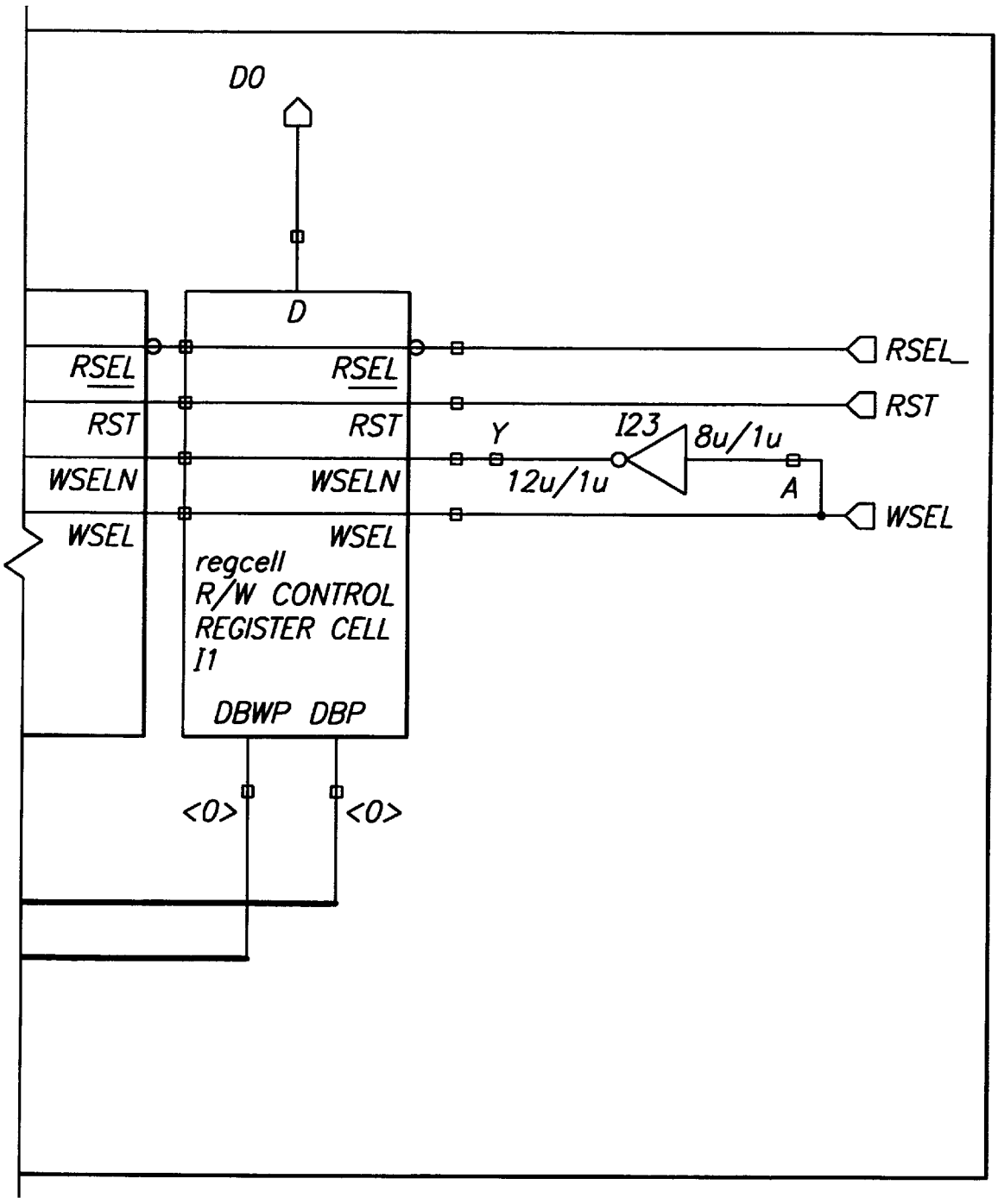

DO
D
RSEL
RSEL
RST
RST
WSELN
WSELN
WSEL
WSEL
regcell
R/W CONTROL
REGISTER CELL
I1
DBWP DBP
<0>
<0>
Y
I23
8u/1u
12u/1u
A
RSEL_
RST
WSEL

Fig 1.12AC

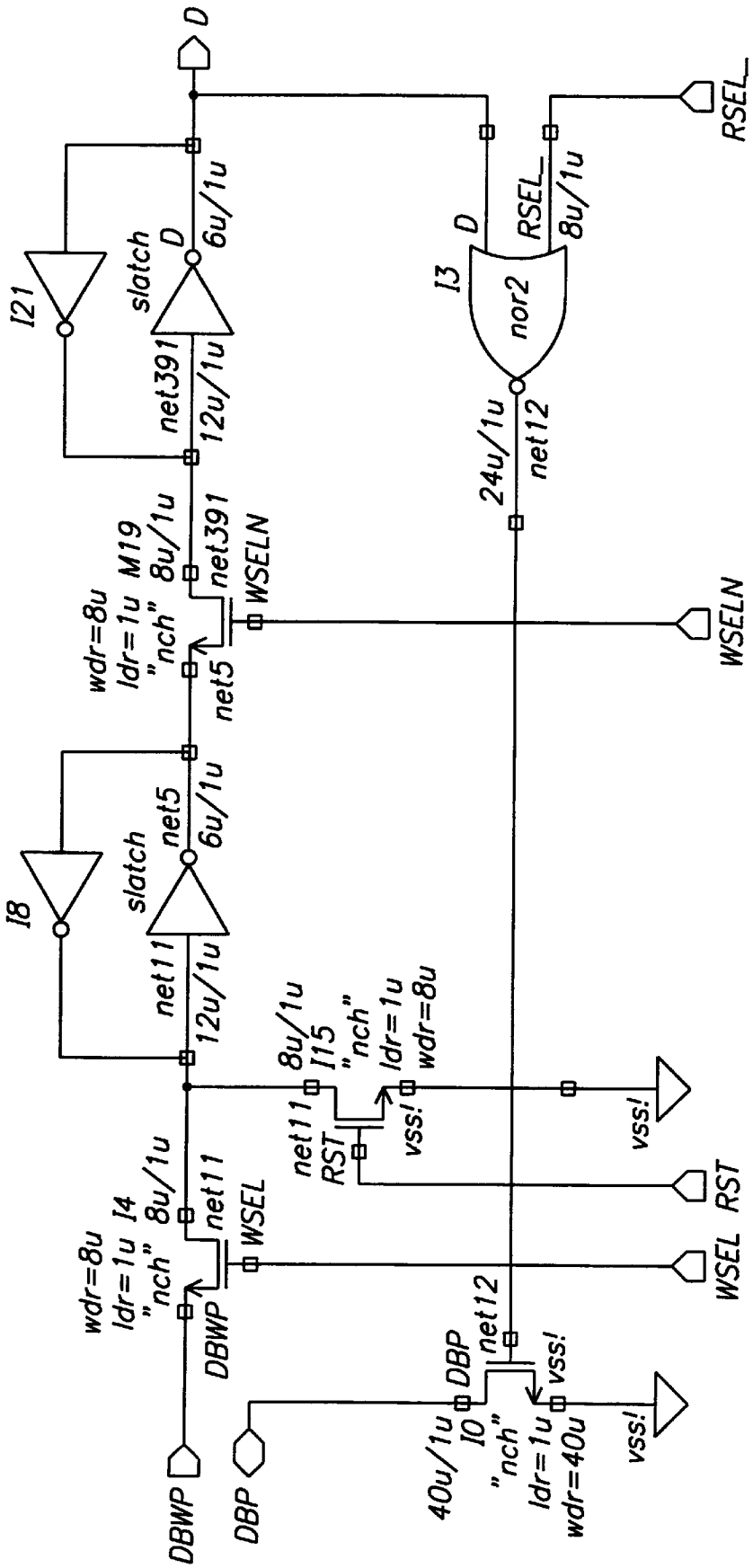

D
RSEL
I21
slatch
D
6u/1u
net391
12u/1u
I3
nor2
RSEL
8u/1u
24u/1u
net12
wdr=8u
ldr=1u
"nch"
M19
8u/1u
net391
WSELN
net5
WSELN
I8
slatch
net5
6u/1u
net11
12u/1u
8u/1u
I15
"nch"
ldr=1u
wdr=8u
net11
RST
vss!
vss!
WSEL RST
I4
8u/1u
net11
WSEL
wdr=8u
ldr=1u
"nch"
DBWP
WSEL
DBP
net12
40u/1u
I0
"nch"
ldr=1u
wdr=40u
vss!
vss!
DBWP
DBP

FIG. 11.2

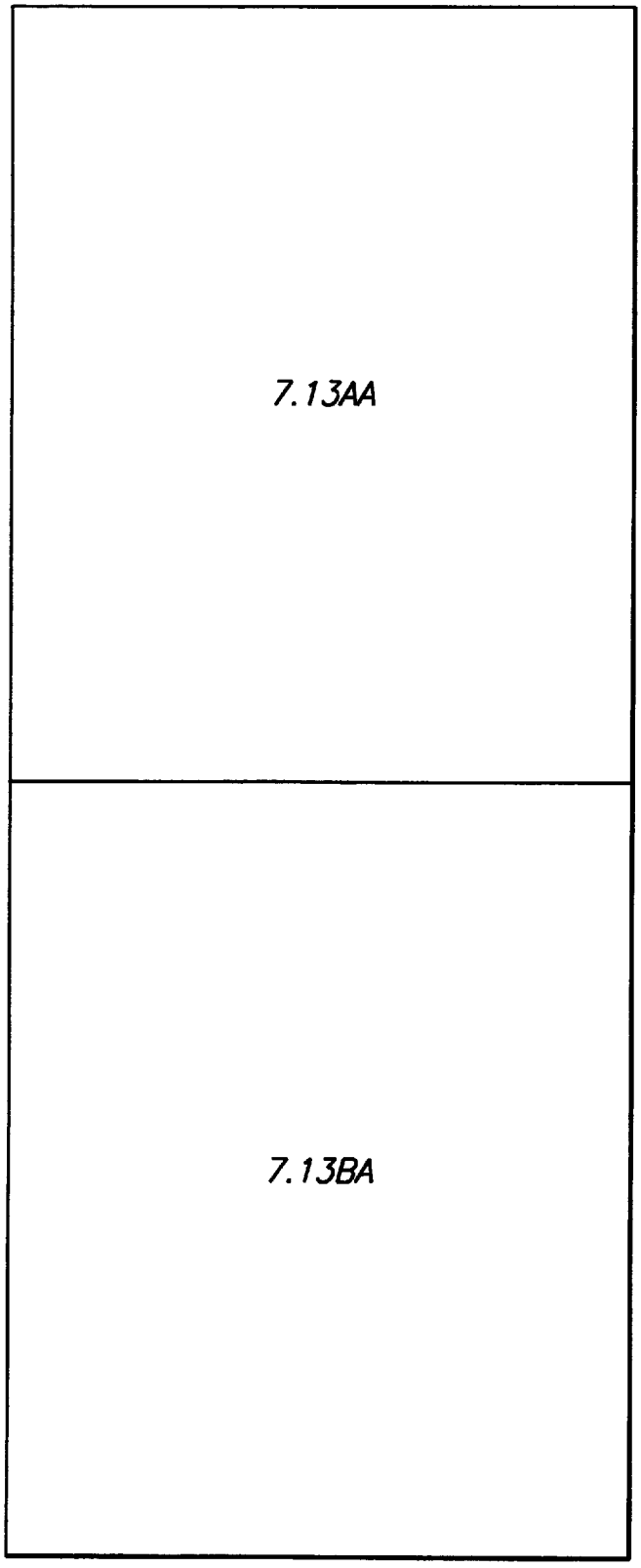


Fig 7.13

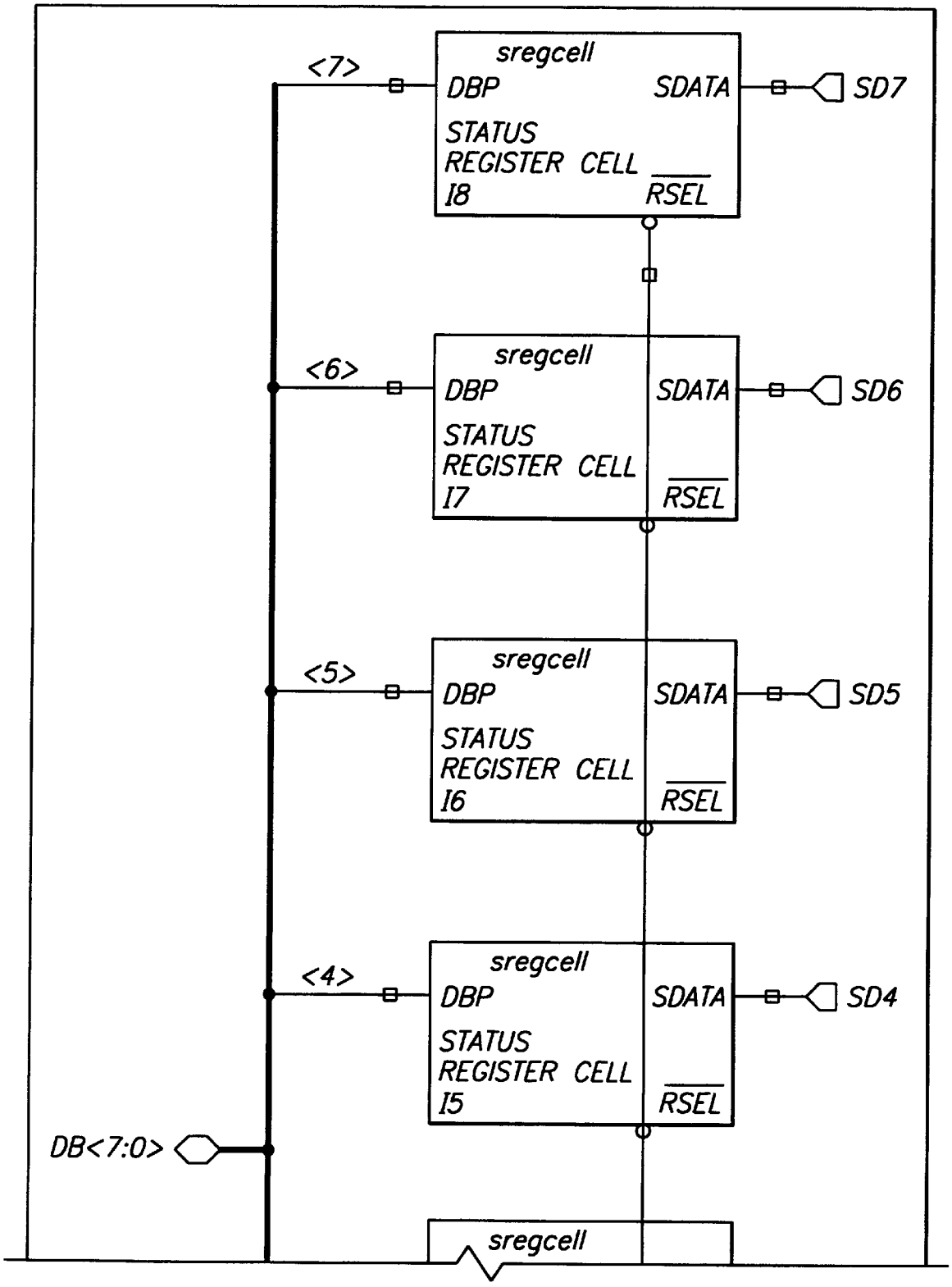

<7>
sregcell
DBP
SDATA
SD7
STATUS
REGISTER CELL
I8
RSEL
<6>
sregcell
DBP
SDATA
SD6
STATUS
REGISTER CELL
I7
RSEL
<5>
sregcell
DBP
SDATA
SD5
STATUS
REGISTER CELL
I6
RSEL
<4>
sregcell
DBP
SDATA
SD4
STATUS
REGISTER CELL
I5
RSEL
DB<7:0>
sregcell

Fig 11.13AA

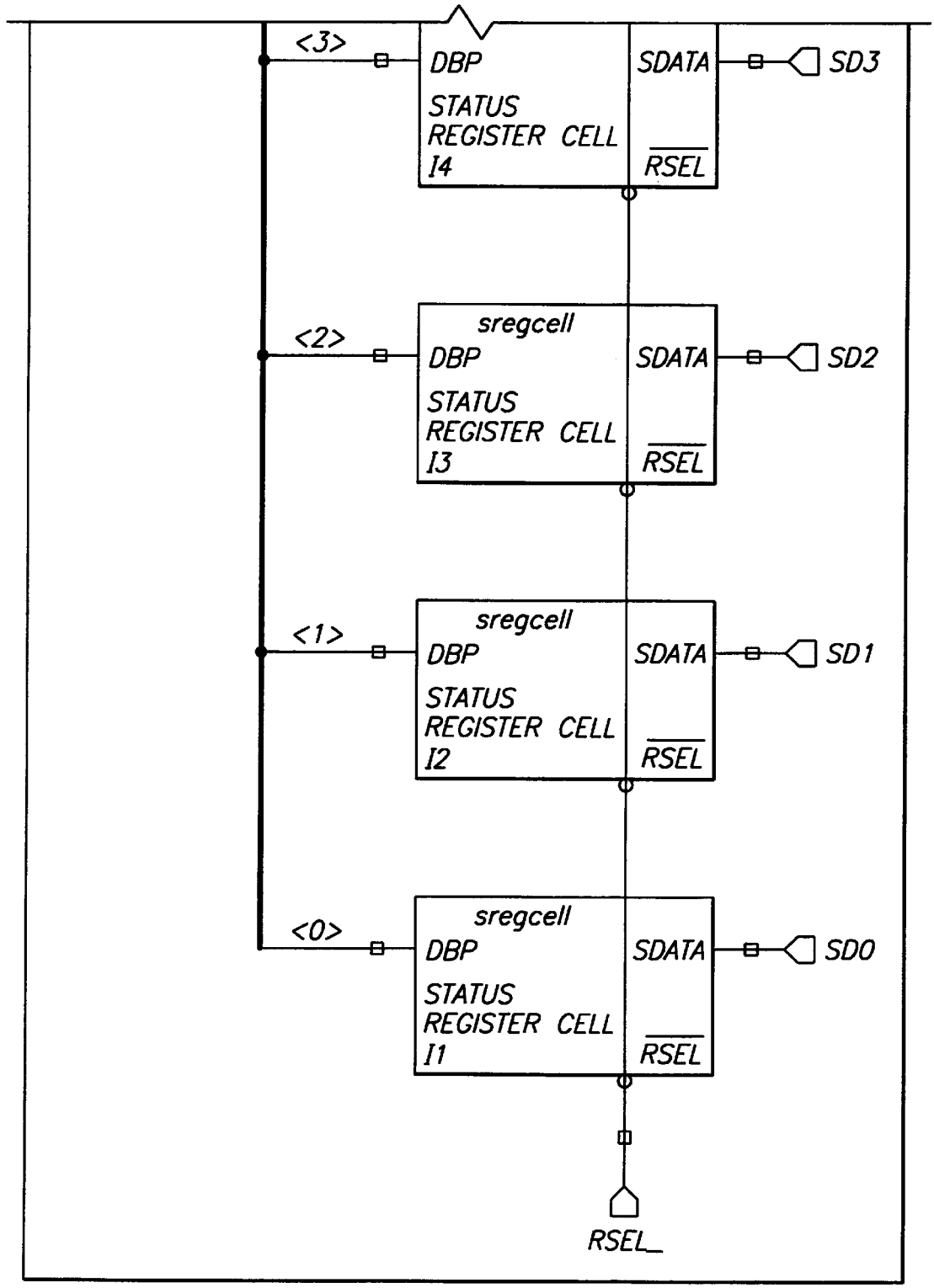

<3>
DBP
STATUS
REGISTER CELL
I4
SDATA
SD3
RSEL
sregcell
<2>
DBP
STATUS
REGISTER CELL
I3
SDATA
SD2
RSEL
sregcell
<1>
DBP
STATUS
REGISTER CELL
I2
SDATA
SD1
RSEL
sregcell
<0>
DBP
STATUS
REGISTER CELL
I1
SDATA
SD0
RSEL
RSEL_

Fig 2.13BA

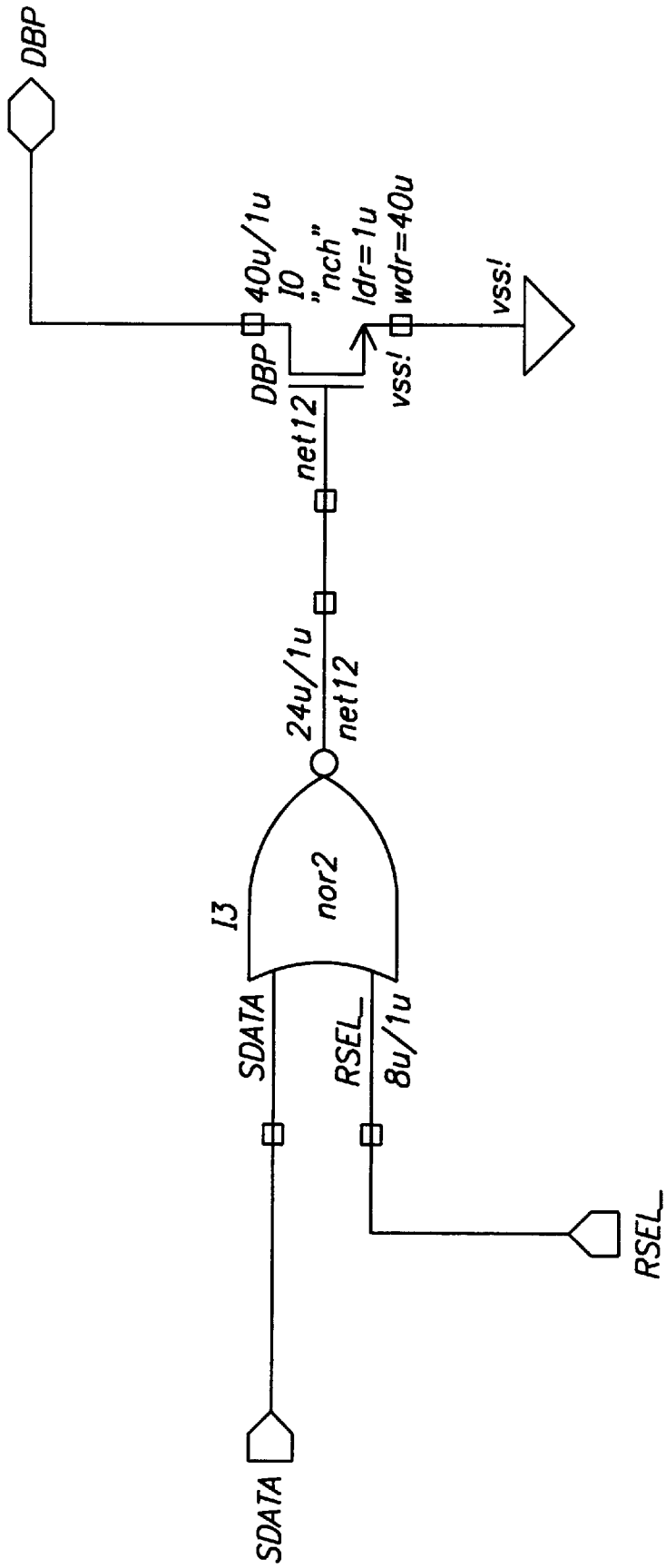

DBP
40u/1u
I0
"nch"
ldr=1u
wdr=40u
vss!
DBP
net12
vss!
24u/1u
net12
I3
nor2
SDATA
RSEL
8u/1u
SDATA
RSEL

FIG. 11.0E

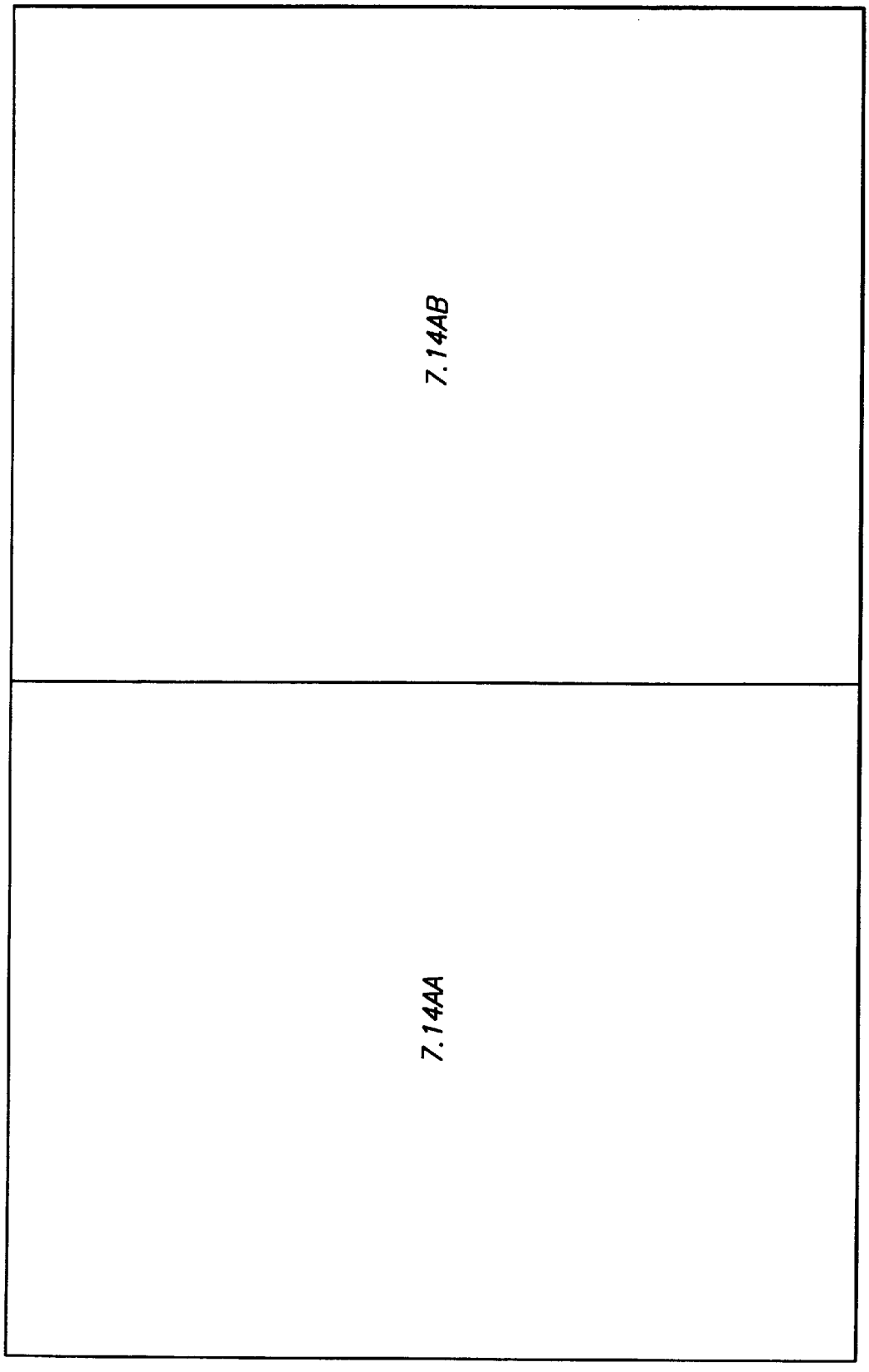


FIG. 7.14

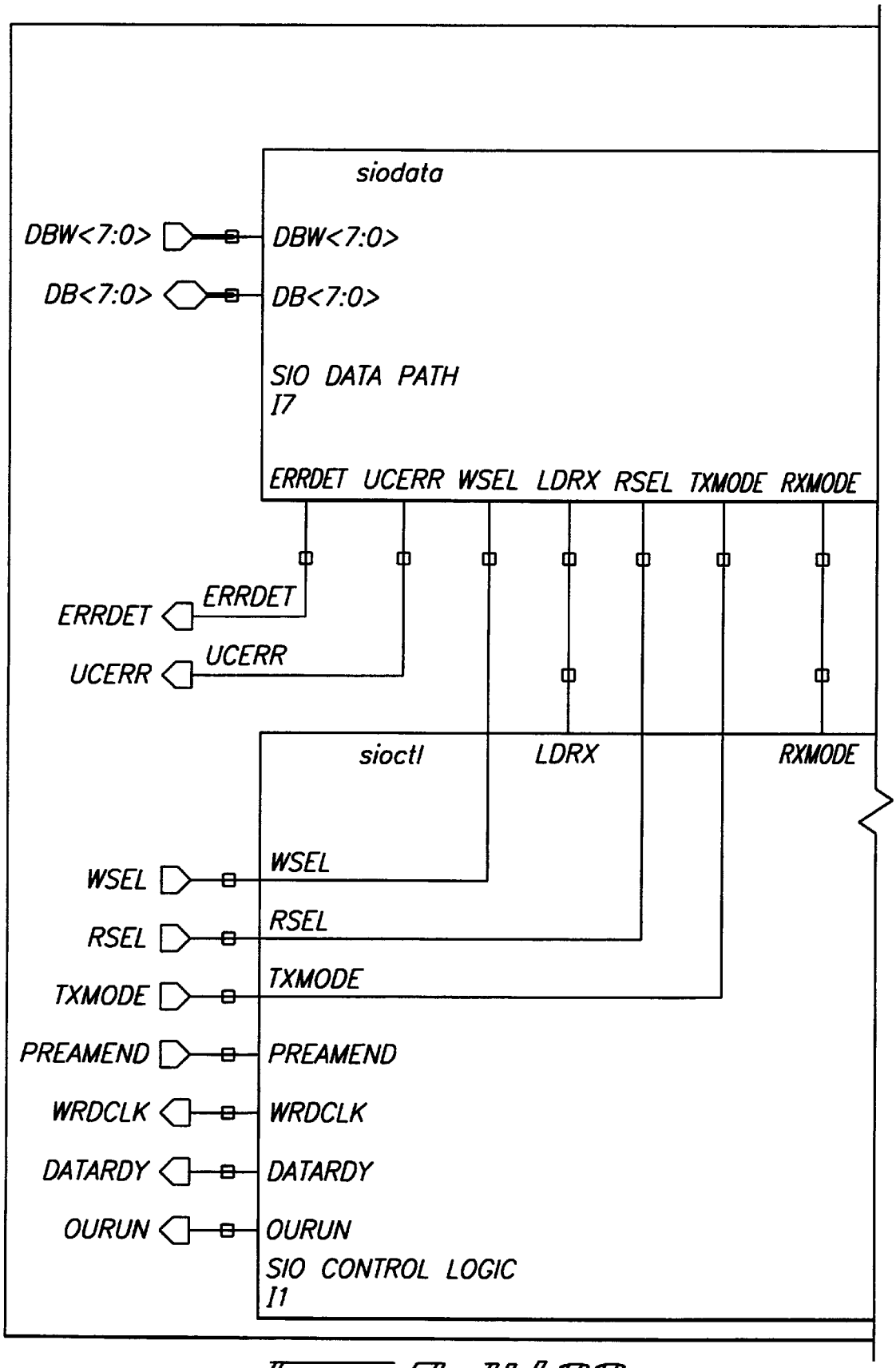

siodata
DBW<7:0>
DBW<7:0>
DB<7:0>
DB<7:0>
SIO DATA PATH
I7
ERRDET UCERR WSEL LDRX RSEL TXMODE RXMODE
ERRDET
ERRDET
UCERR
UCERR
sioctl
LDRX
RXMODE
WSEL
WSEL
RSEL
RSEL
TXMODE
TXMODE
PREAMEND
PREAMEND
WRDCLK
WRDCLK
DATARDY
DATARDY
OURUN
OURUN
SIO CONTROL LOGIC
I1

Fig 1.14AA

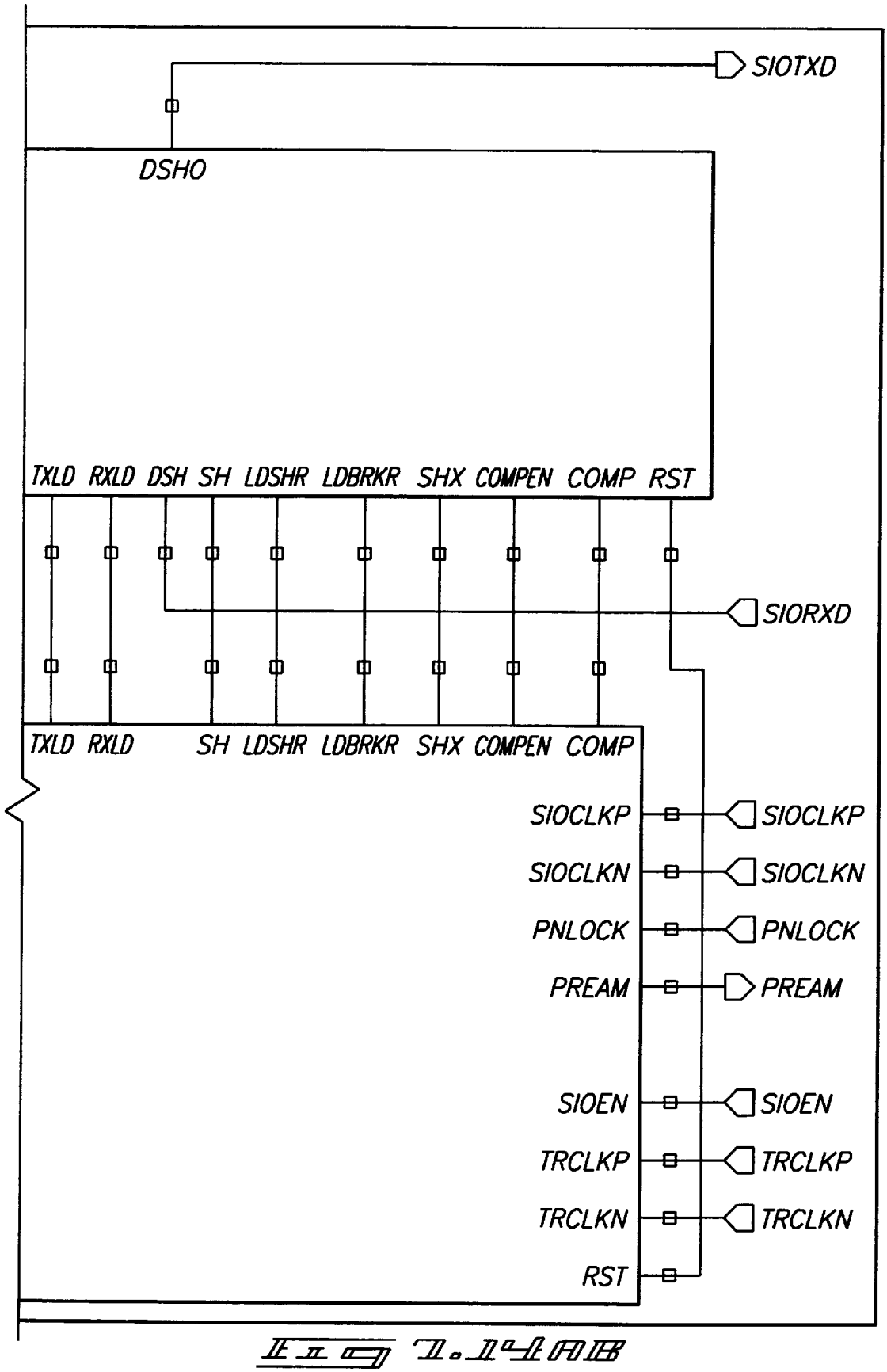

SIOTXD
DSHO
TXLD RXLD DSH SH LDSHR LDBRKR SHX COMPEN COMP RST
SIORXD
TXLD RXLD SH LDSHR LDBRKR SHX COMPEN COMP
SIOCLKP
SIOCLKN
PNLOCK
PREAM
SIOEN
TRCLKP
TRCLKN
RST
SIOCLKP
SIOCLKN
PNLOCK
PREAM
SIOEN
TRCLKP
TRCLKN

FIG. 11AB

7.1401AA	7.1401AB	7.1401AC	7.1401AD	7.1401AE	7.1401AF
7.1401BA	7.1401BB	7.1401BC	7.1401BD	7.1401BE	7.1401BF
7.1401CA	7.1401CB	7.1401CC	7.1401CD	7.1401CE	7.1401CF
7.1401DA	7.1401DB	7.1401DC	7.1401DD	7.1401DE	7.1401DF
7.1401EA	7.1401EB	7.1401EC	7.1401ED	7.1401EE	7.1401EF
7.1401FA	7.1401FB	7.1401FC	7.1401FD	7.1401FE	7.1401FF
7.1401GA	7.1401GB	7.1401GC	7.1401GD	7.1401GE	7.1401GF

FIG. 7.1401

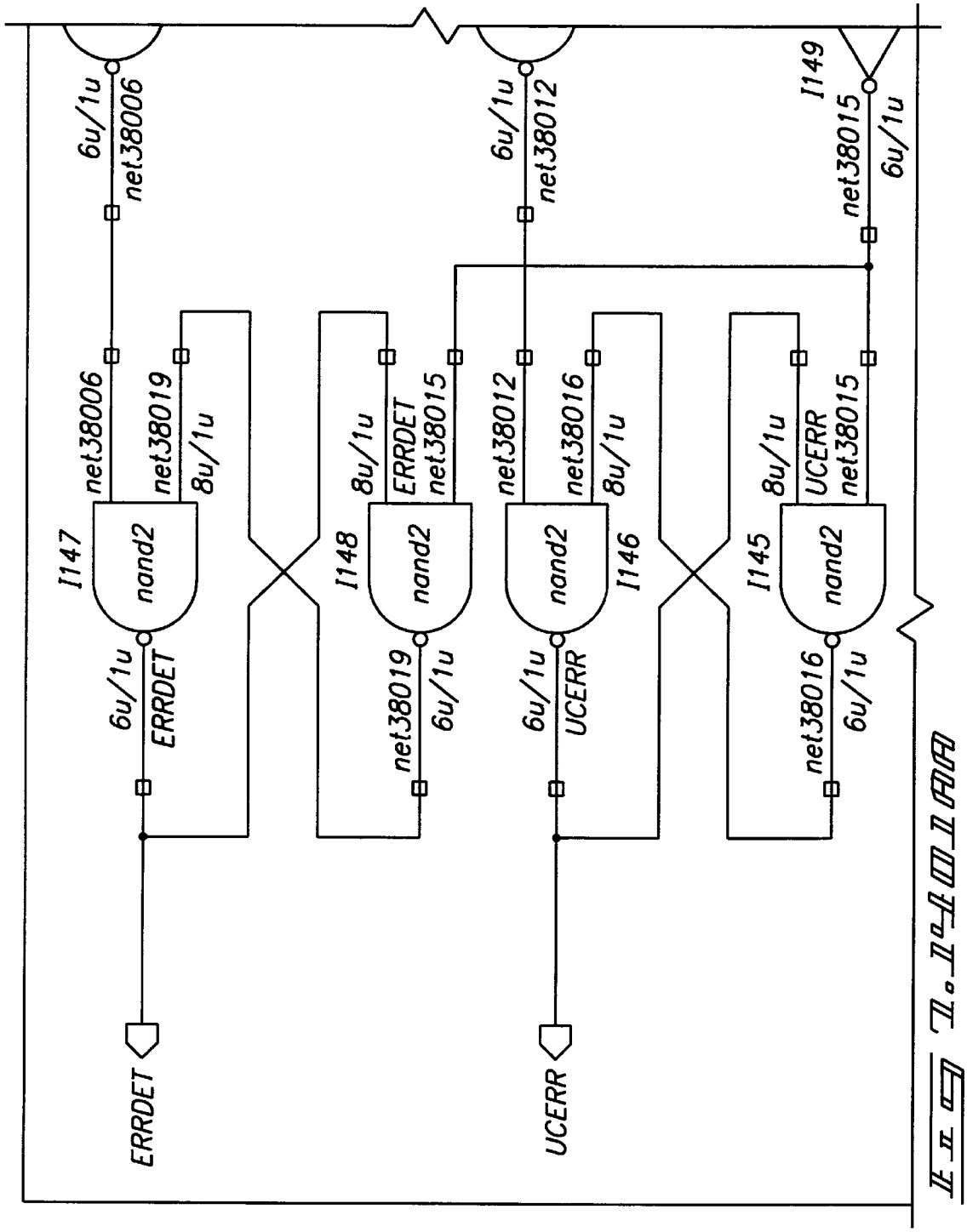
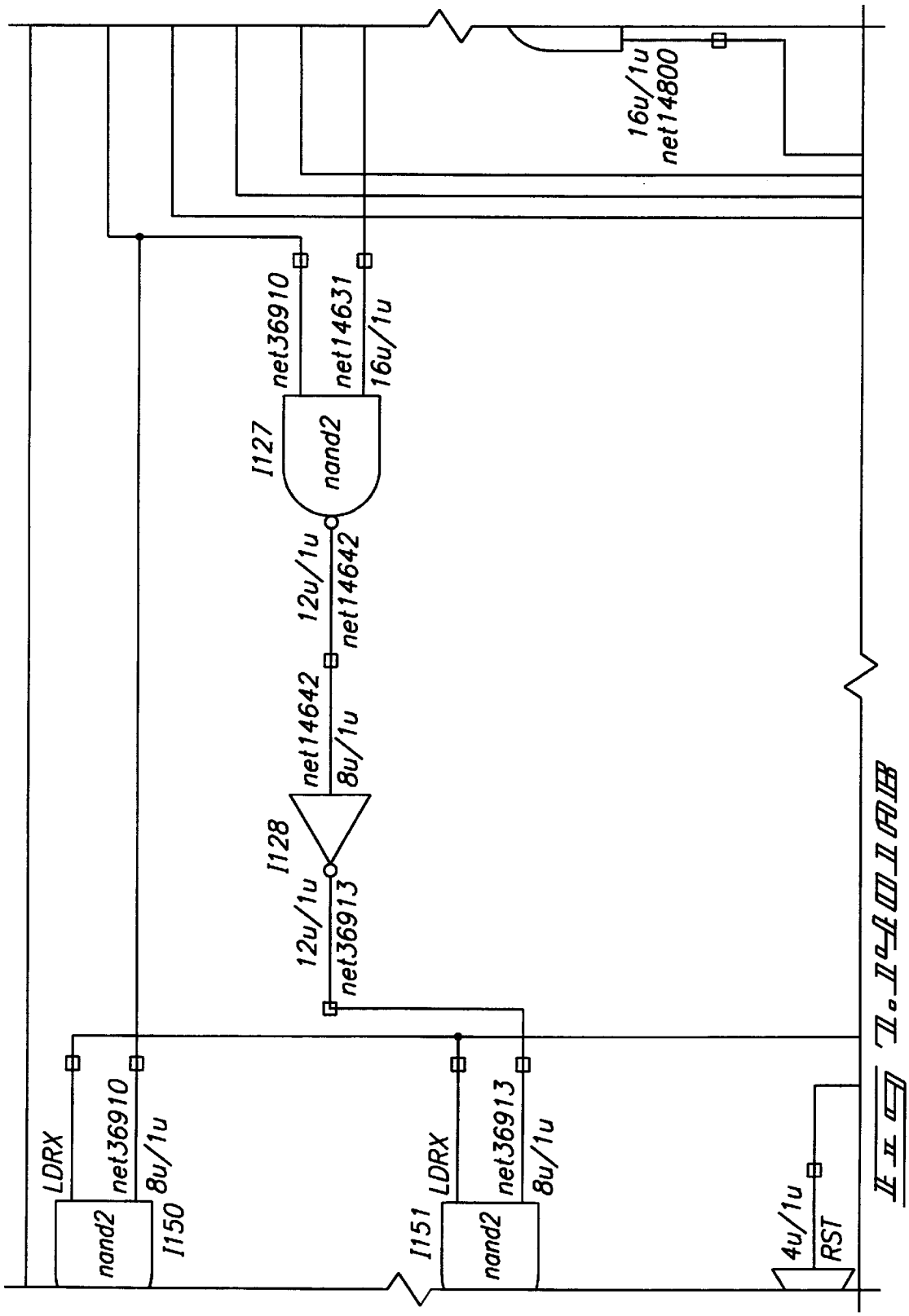
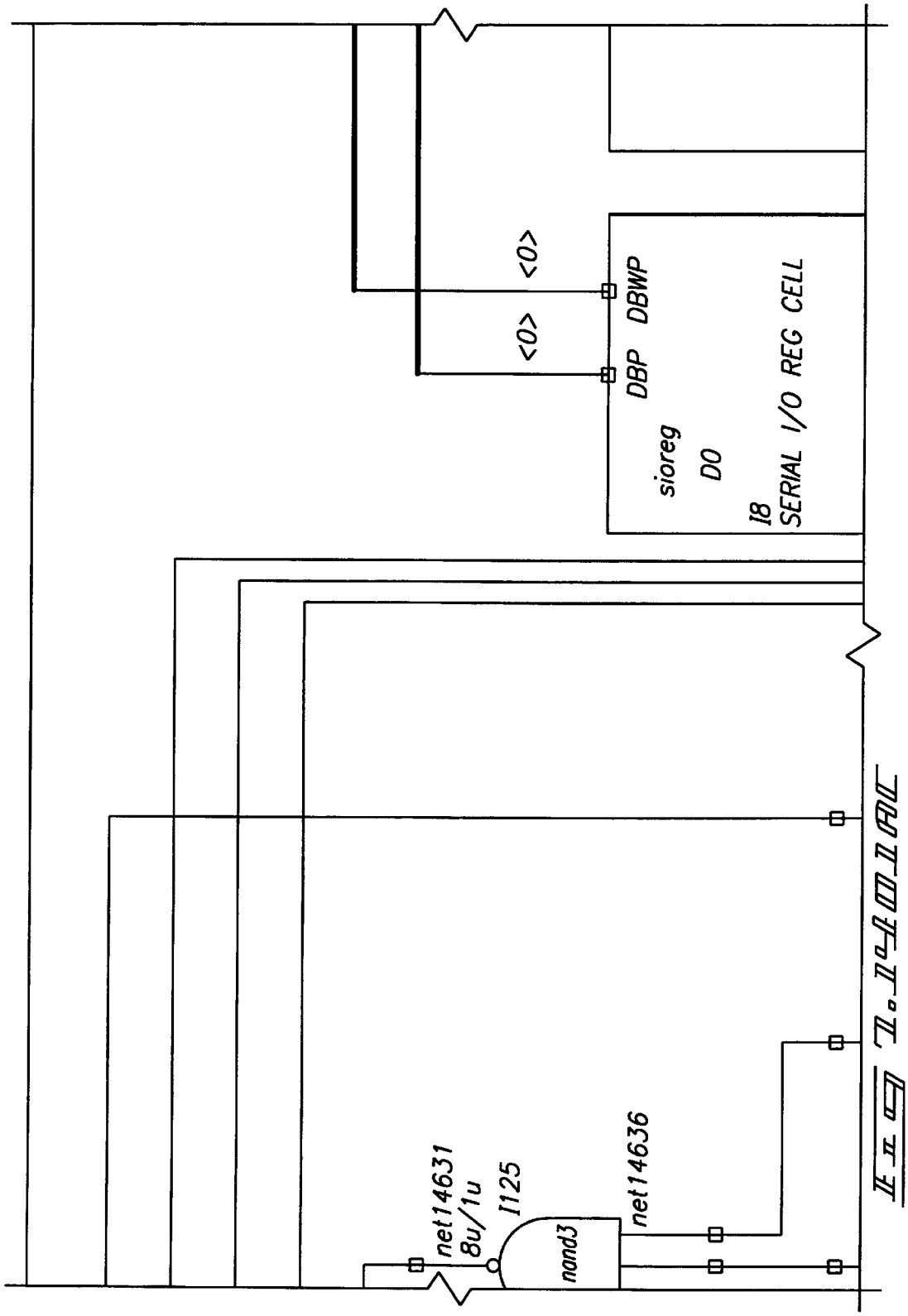

6u/1u
net38006
6u/1u
net38012
I149
net38015
6u/1u
net38006
net38019
8u/1u
8u/1u
ERRDET
net38015
net38012
net38016
8u/1u
8u/1u
UCERR
net38015
I147
nand2
I148
nand2
nand2
I146
I145
nand2
6u/1u
ERRDET
net38019
6u/1u
6u/1u
UCERR
net38016
6u/1u
ERRDET
UCERR

FIG 931


16u/1u
net14800
net36910
net14631
16u/1u
I127
nand2
12u/1u
net14642
net14642
8u/1u
I128
12u/1u
net36913
LDRX
net36910
8u/1u
nand2
I150
I151
LDRX
net36913
8u/1u
nand2
4u/1u
RST


<0>
<0>
DBP DBWP
sioreg
DO
I8
SERIAL I/O REG CELL
net14631
8u/1u
I125
nand3
net14636

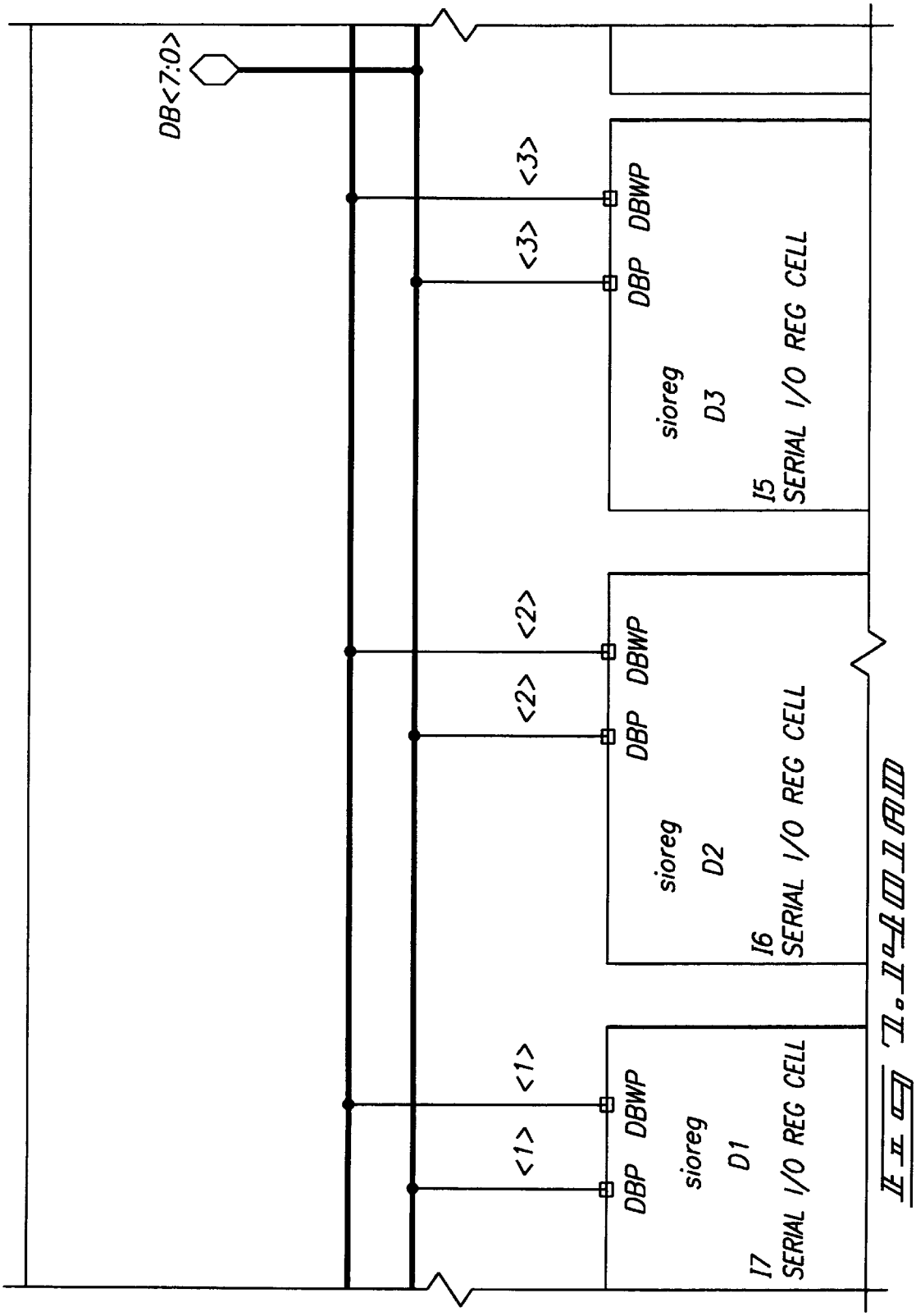

DB<7:0>
<3>
<3>
DBP DBWP
sioreg
D3
I5
SERIAL I/O REG CELL
<2>
<2>
DBP DBWP
sioreg
D2
I6
SERIAL I/O REG CELL
<1>
<1>
DBP DBWP
sioreg
D1
I7
SERIAL I/O REG CELL

FIG. 6L

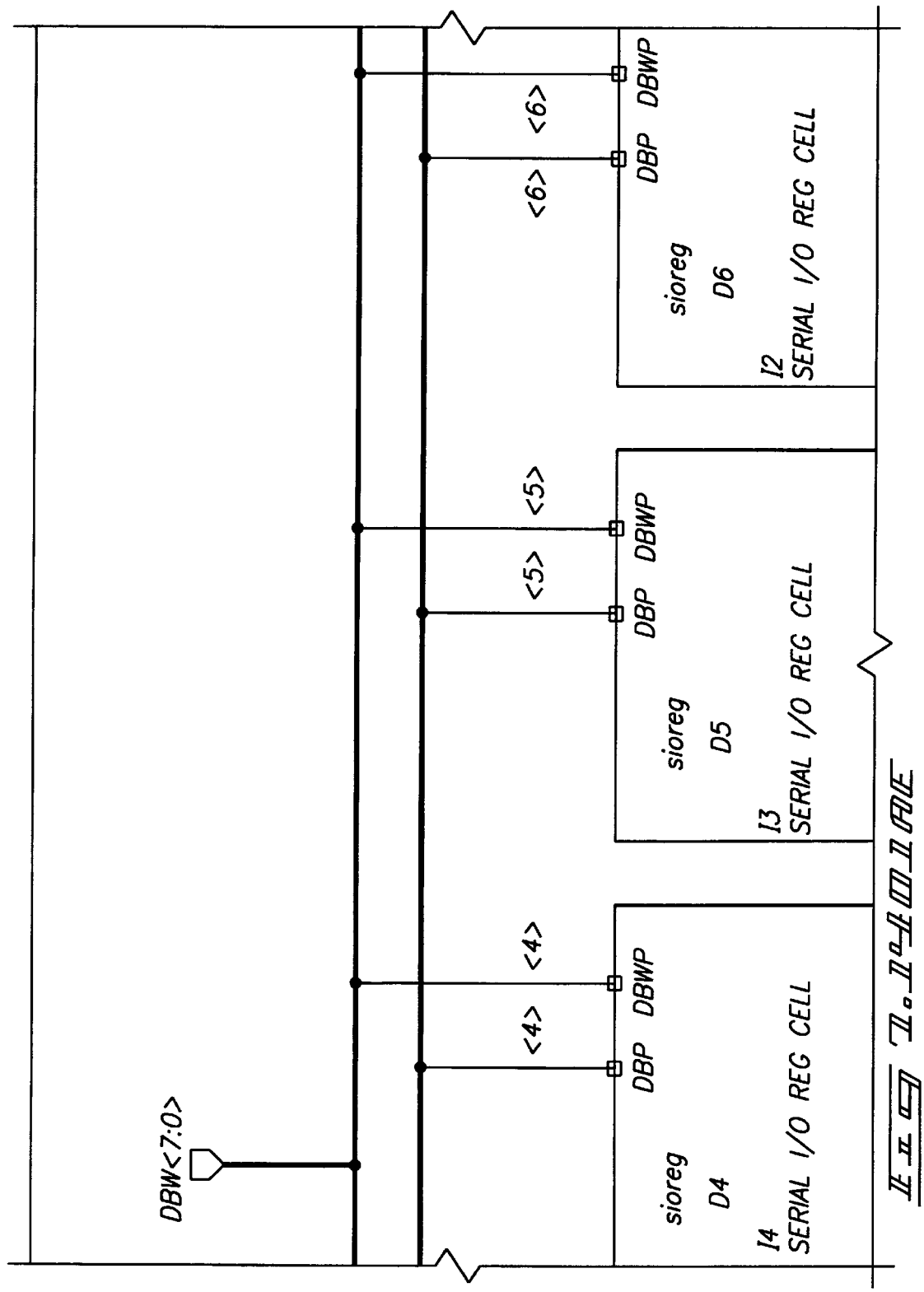


FIG 11.14001AE

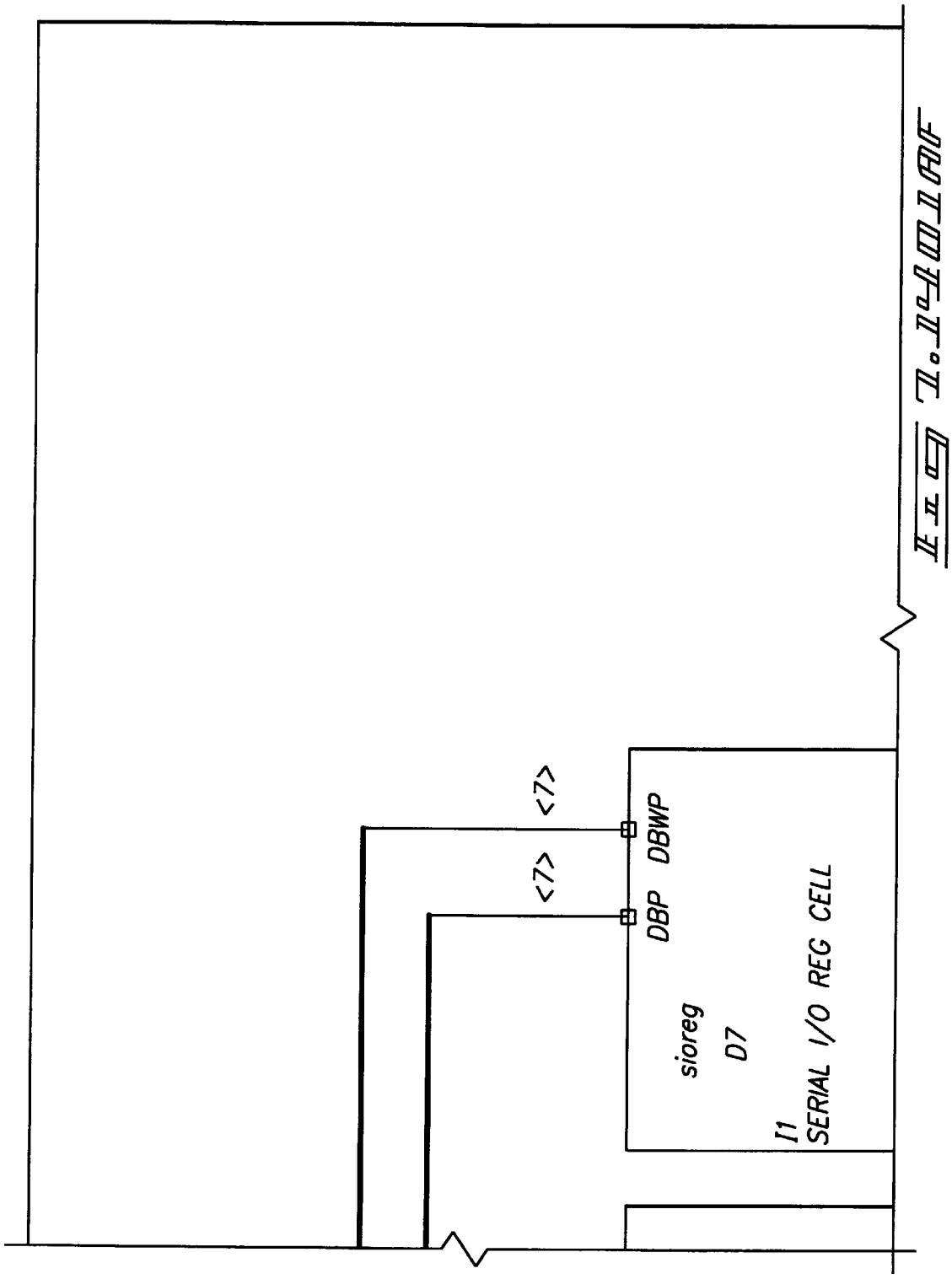
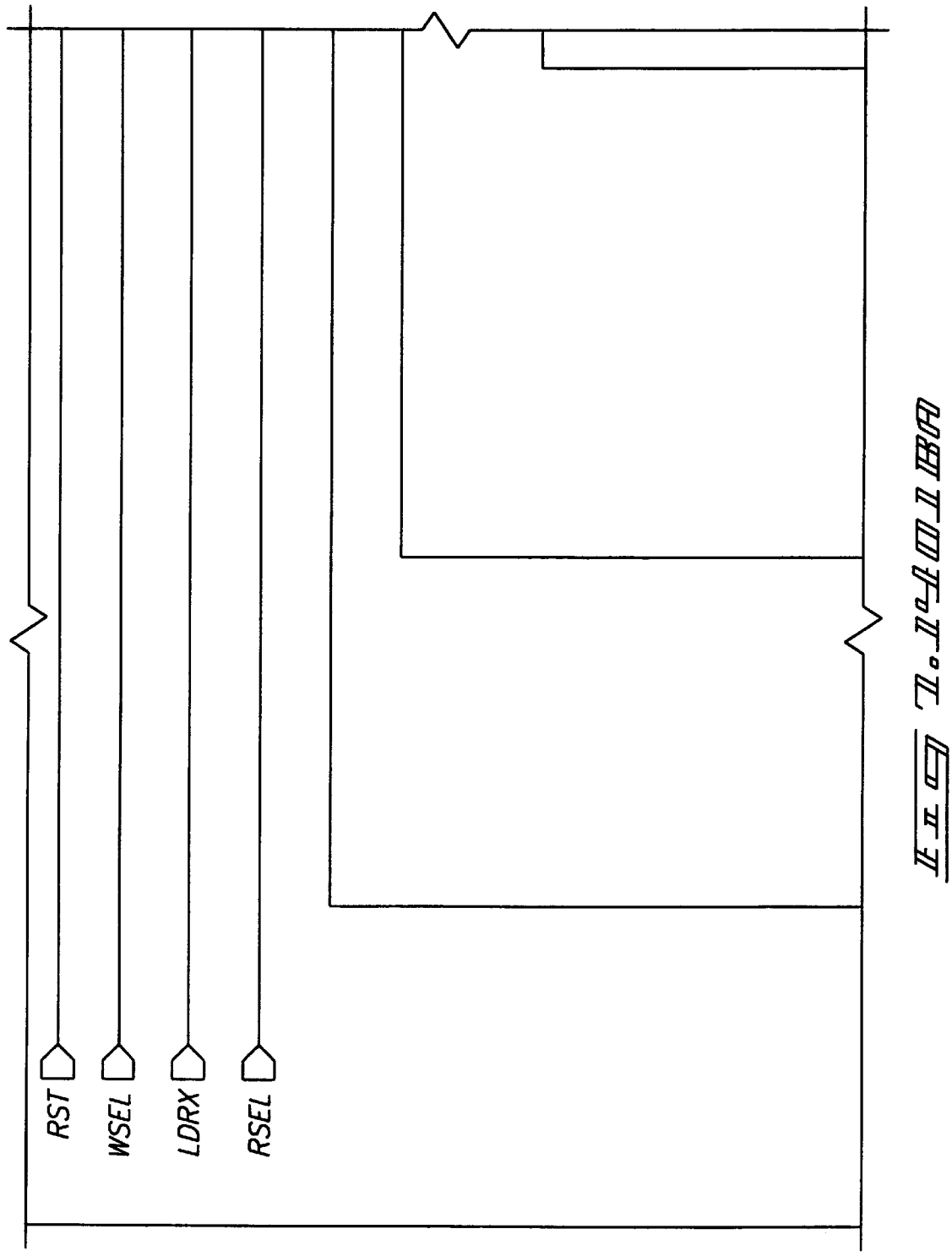
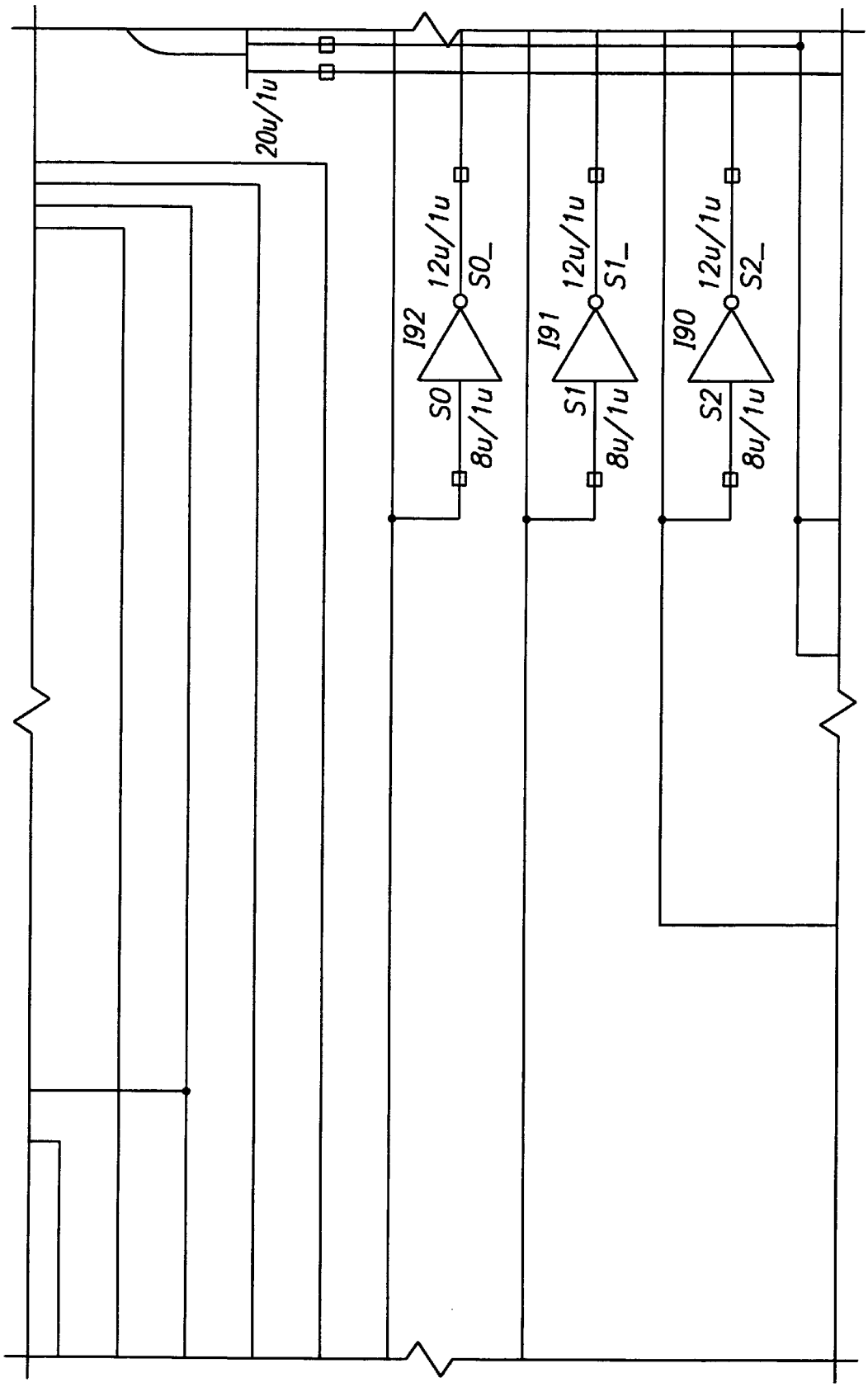


FIG. 7AAAL
<7>
<7>
DBWP
DBP
sioreg
D7
I1
SERIAL I/O REG CELL


RST
WSEL
LDRX
RSEL
SUBSTRATE


20u/1u
I92
12u/1u
S0_
S0
8u/1u
I91
12u/1u
S1_
S1
8u/1u
I90
12u/1u
S2_
S2
8u/1u

ФИГ. 1.

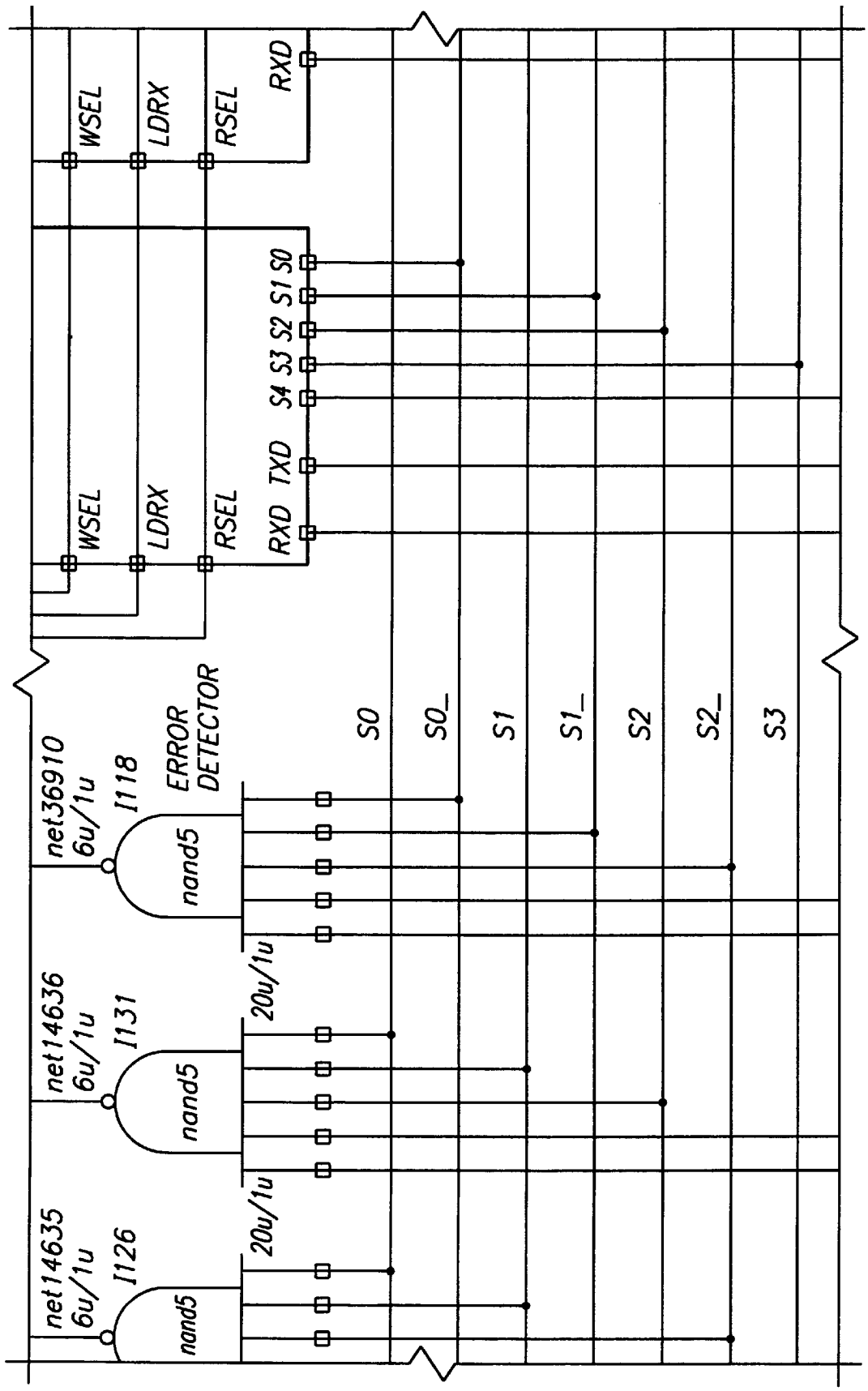
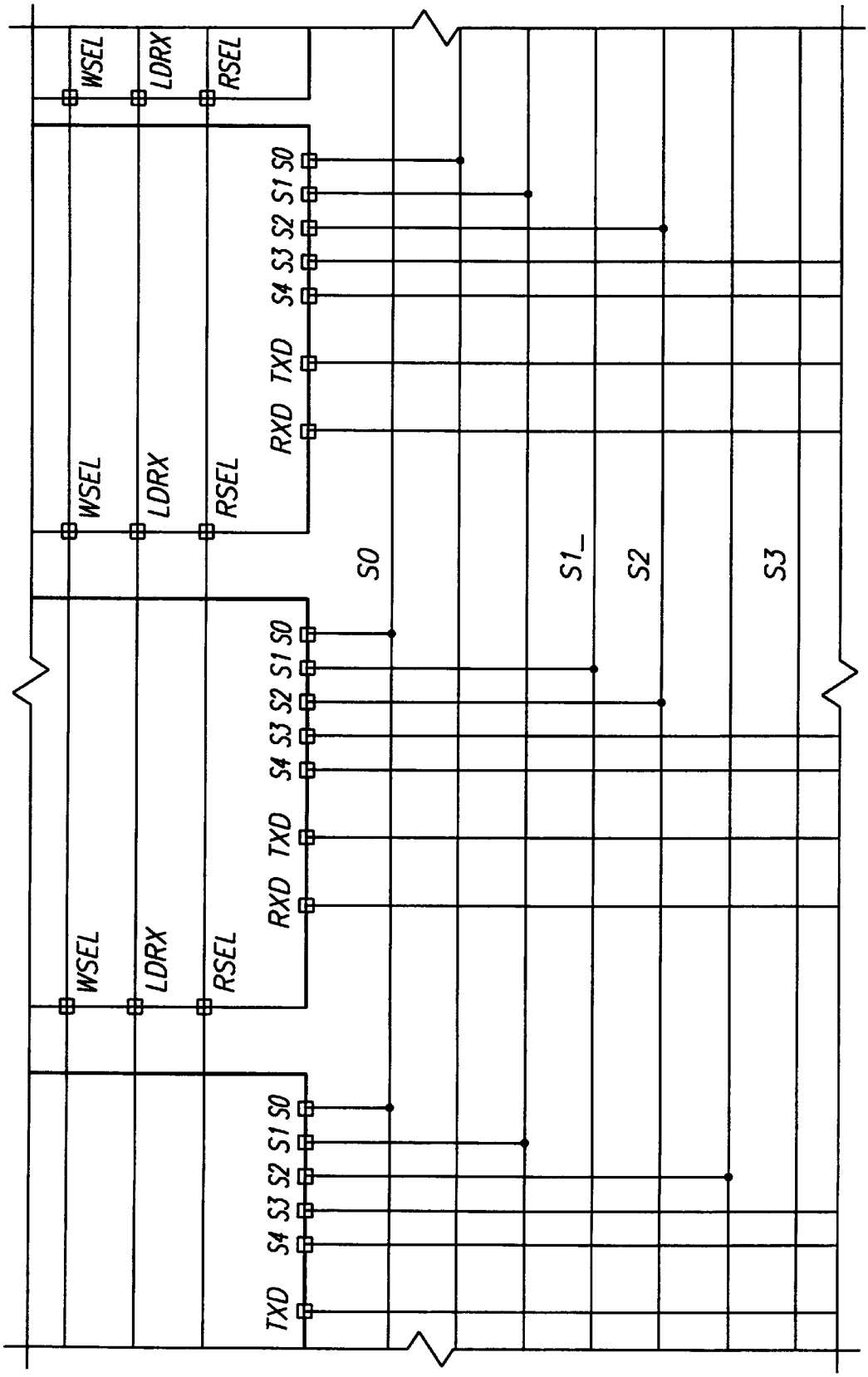

RXD
RSEL
LDRX
WSEL
S0
S1
S2
S3
S4
TXD
RXD
RSEL
LDRX
WSEL
S0
S0_
S1
S1_
S2
S2_
S3
ERROR DETECTOR
I118
net36910
6u/1u
nand5
20u/1u
I131
net14636
6u/1u
nand5
20u/1u
I126
net14635
6u/1u
nand5

FIG. 604E



Фиг. 11

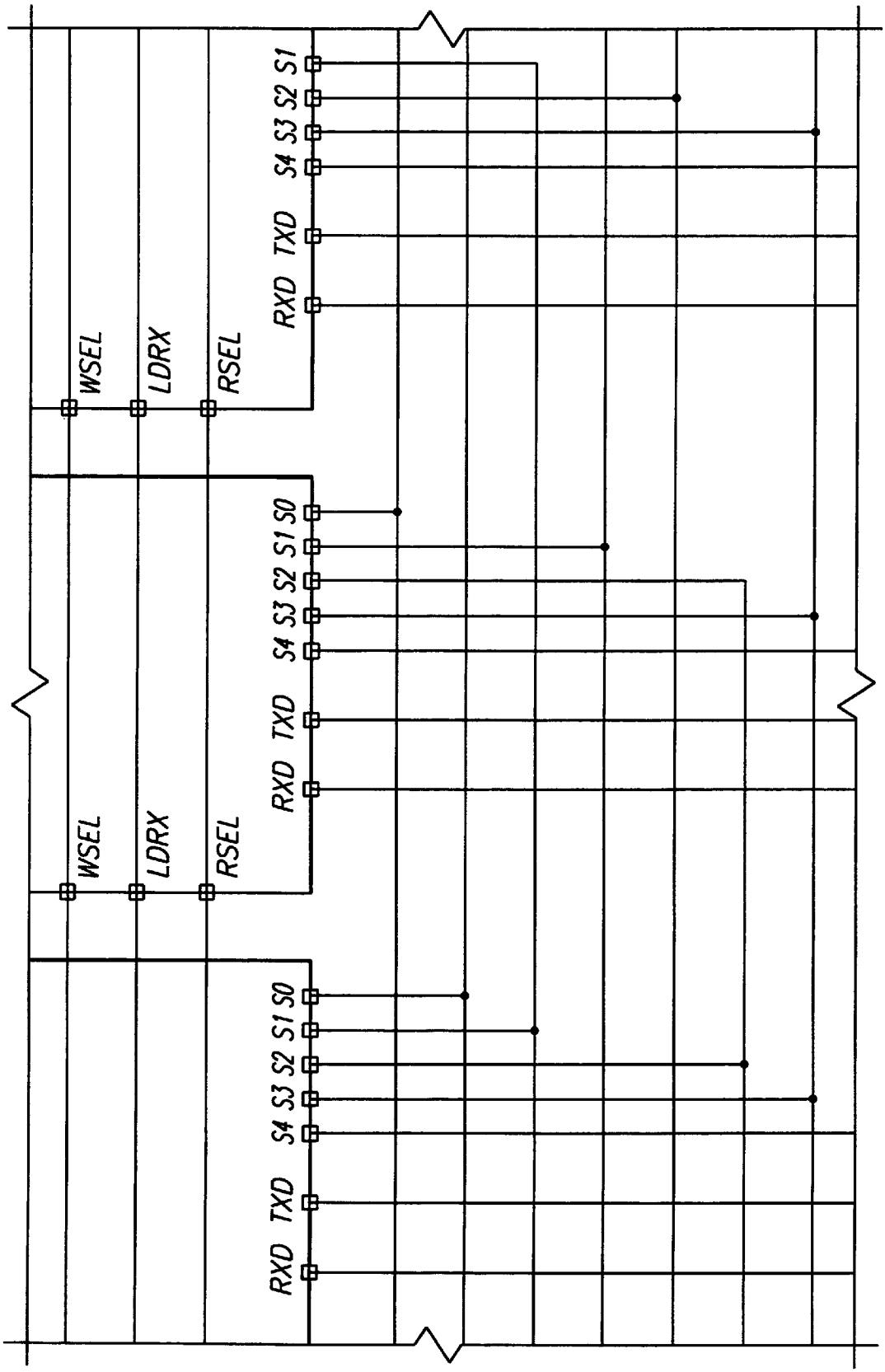

WSEL
LDRX
RSEL
RXD TXD S4 S3 S2 S1
WSEL
LDRX
RSEL
RXD TXD S4 S3 S2 S1 S0
WSEL
LDRX
RSEL
RXD TXD S4 S3 S2 S1 S0

FIG. 943

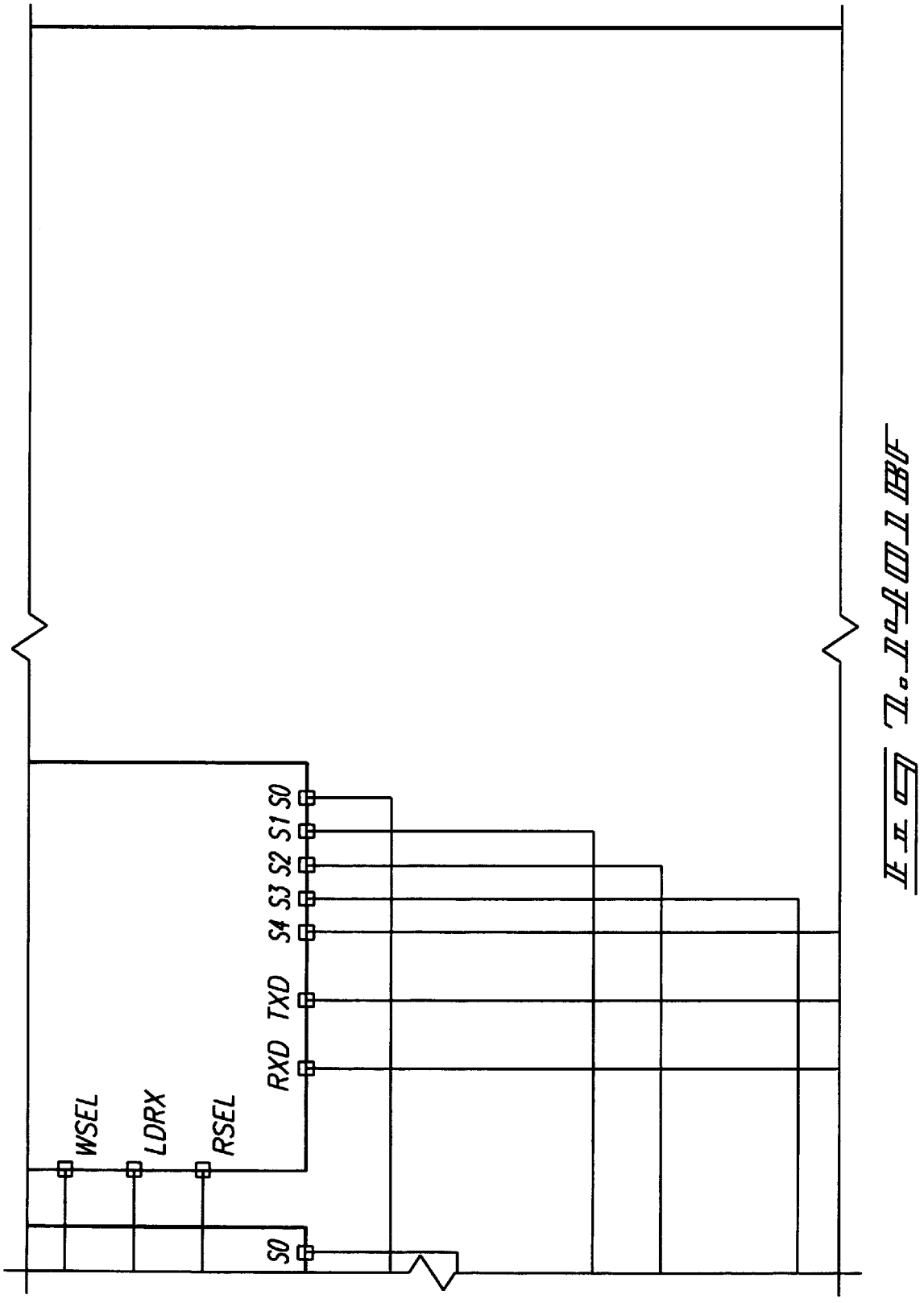
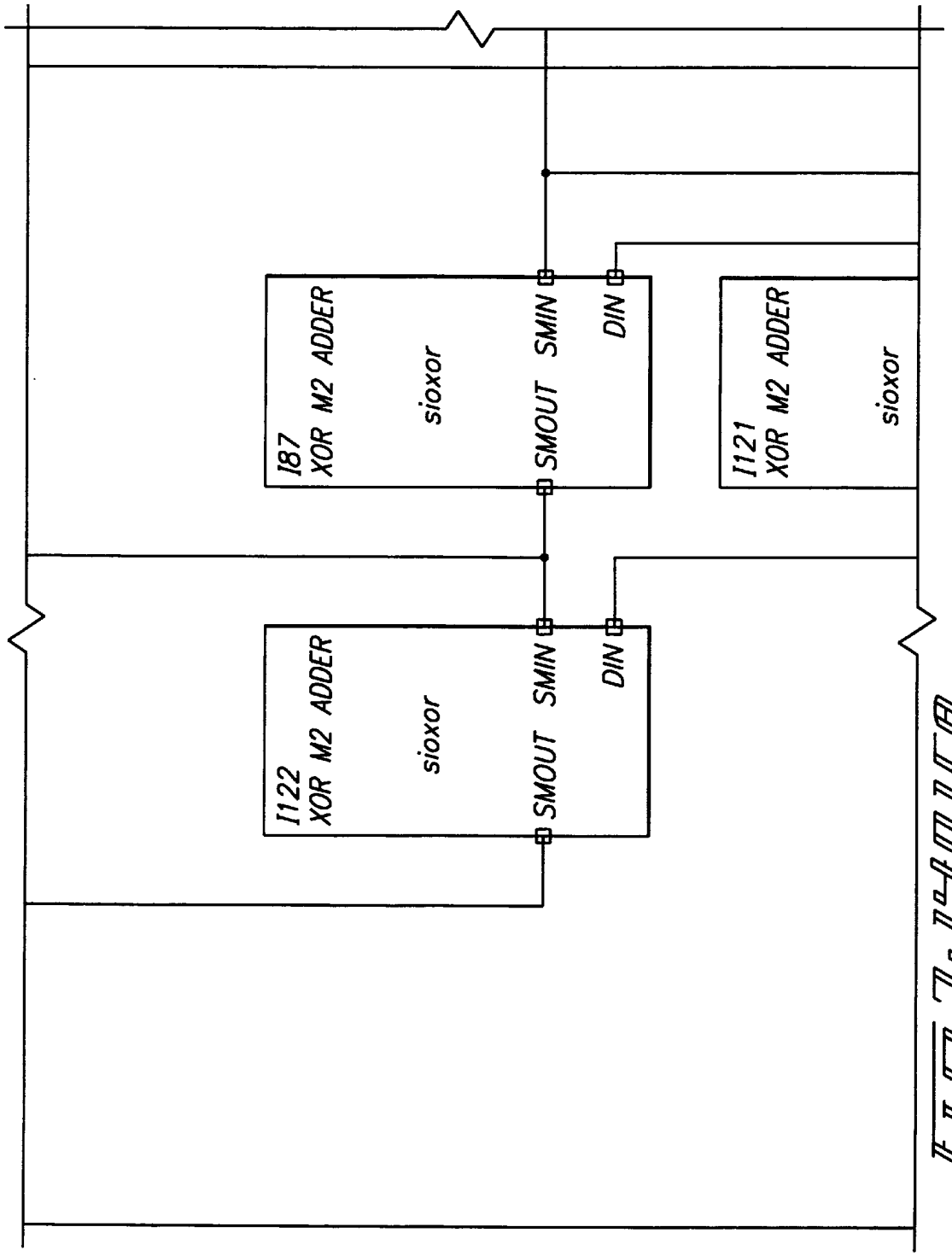
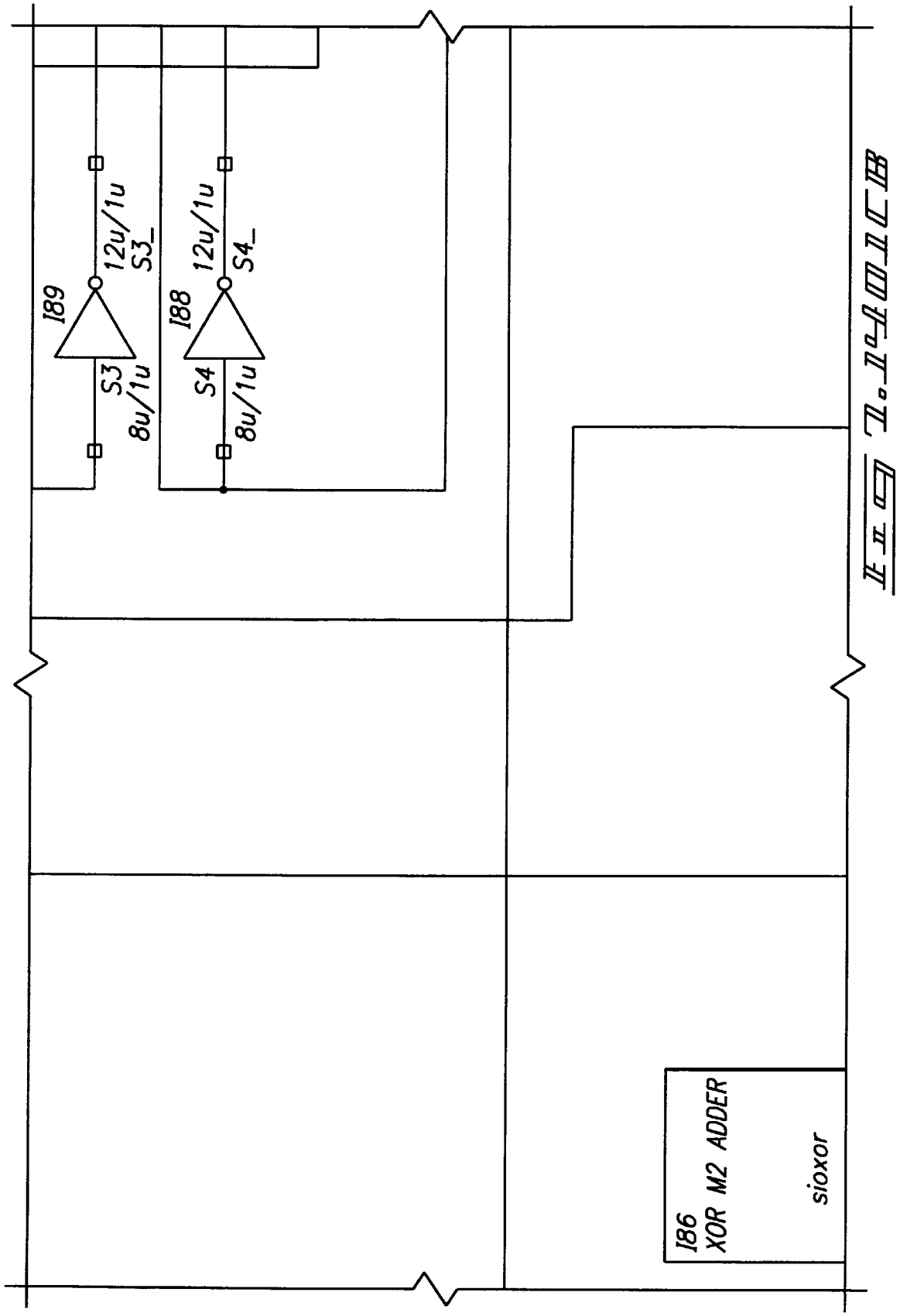
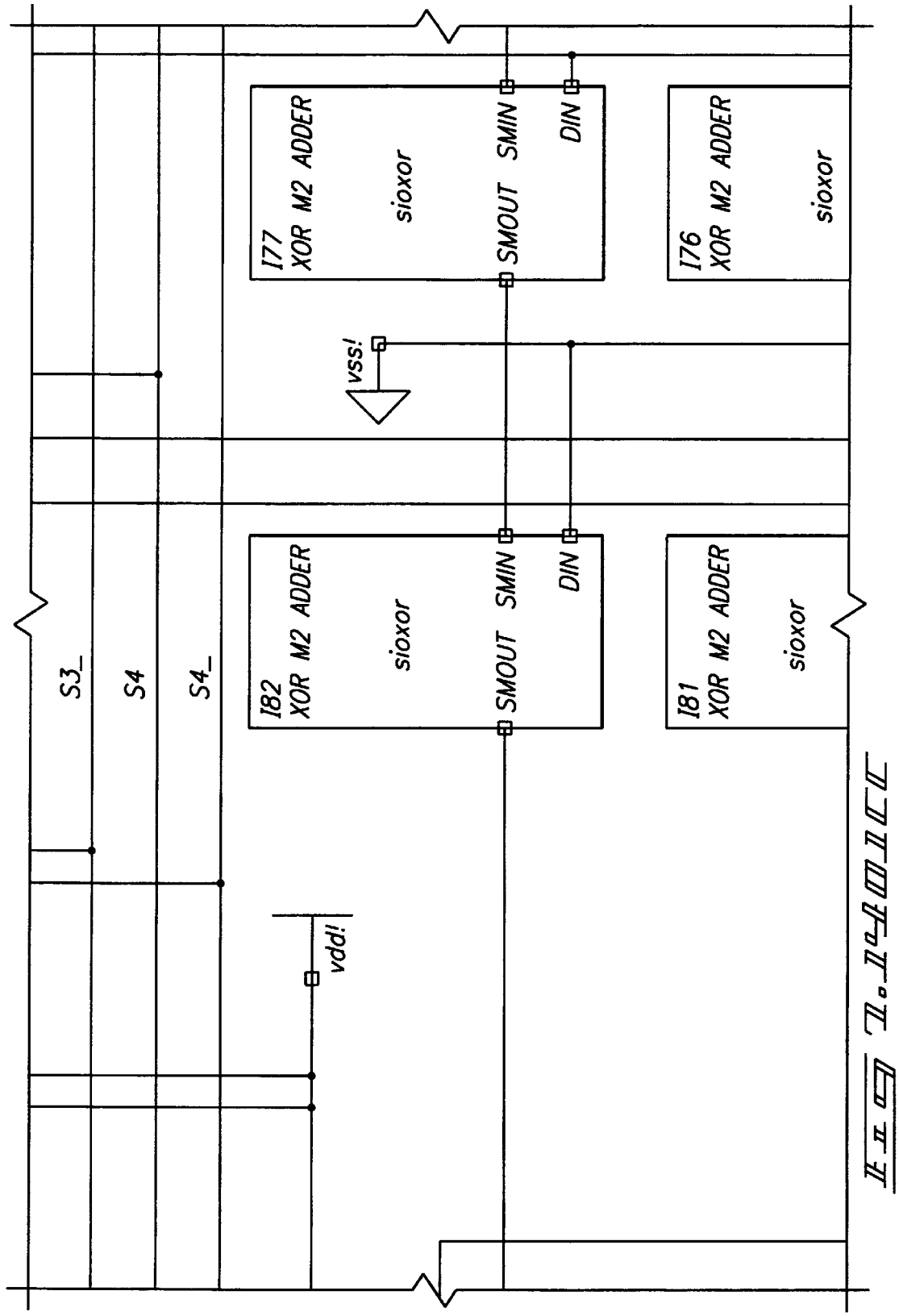


FIG 1064 of 5411

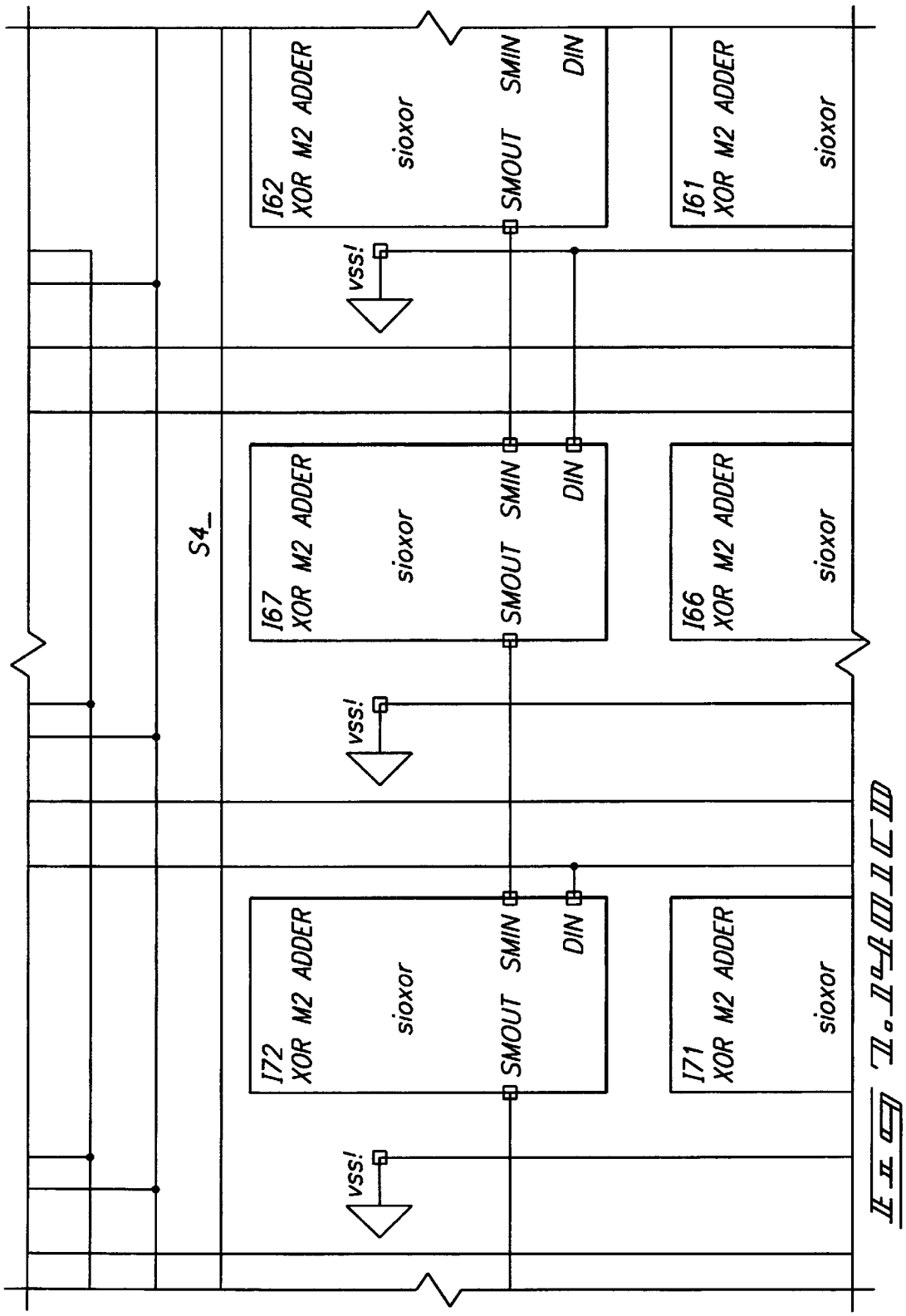

I87
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I121
XOR M2 ADDER
sioxor
I122
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN

ФИГ. 1.947


I89
12u/1u
S3_
S3
8u/1u
I88
12u/1u
S4_
S4
8u/1u
I86
XOR M2 ADDER
sioxor


I77
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I76
XOR M2 ADDER
sioxor
vss!
I82
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I81
XOR M2 ADDER
sioxor
S3_
S4
S4_
vdd!

Фиг. 6.11


I62
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I61
XOR M2 ADDER
sioxor
vss!
S4_
I67
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I66
XOR M2 ADDER
sioxor
vss!
I72
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I71
XOR M2 ADDER
sioxor
vss!

Фиг. 1

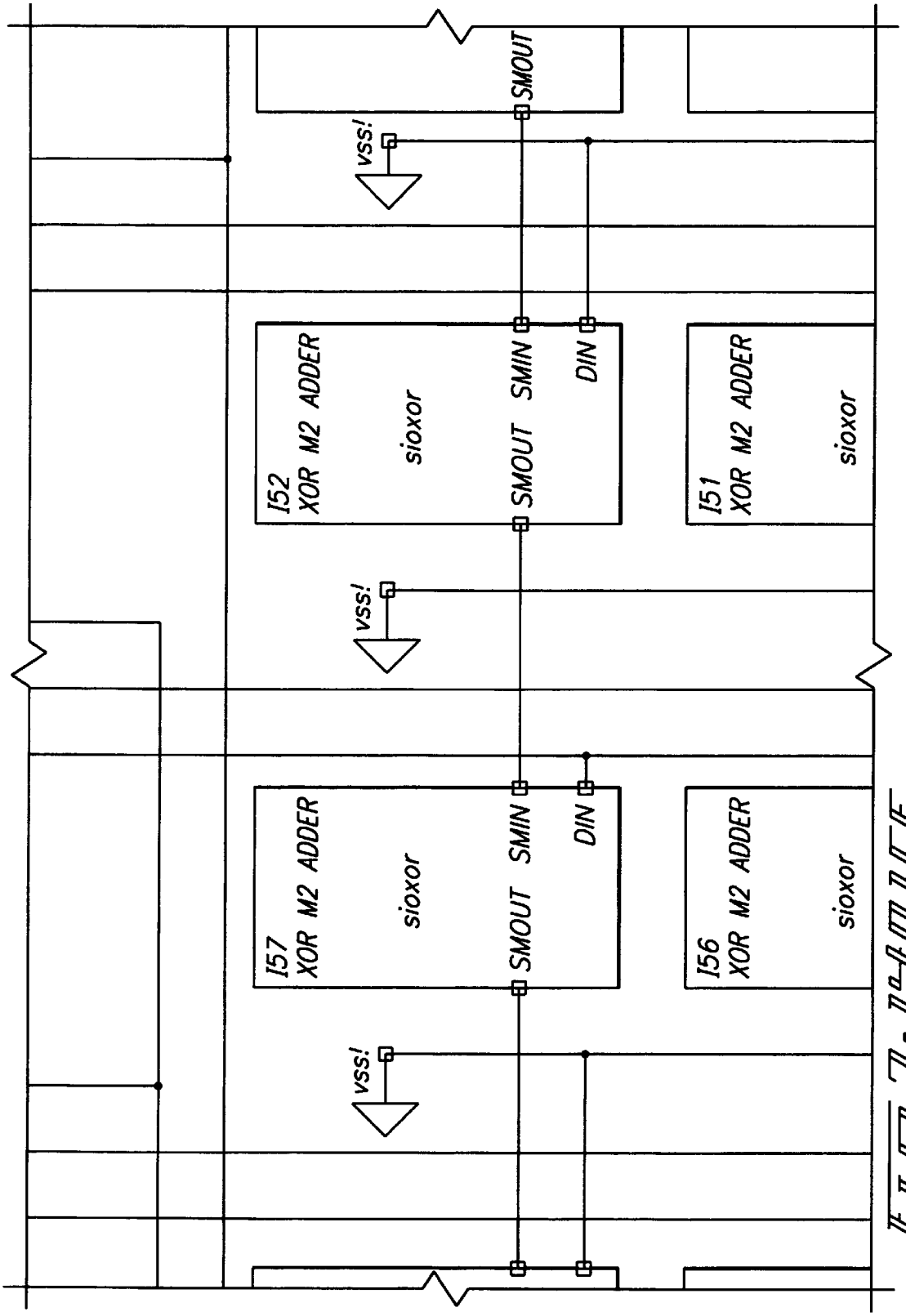

SMOUT
vss!
I52
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I51
XOR M2 ADDER
sioxor
vss!
I57
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
I56
XOR M2 ADDER
sioxor
vss!

Fig. 1101E

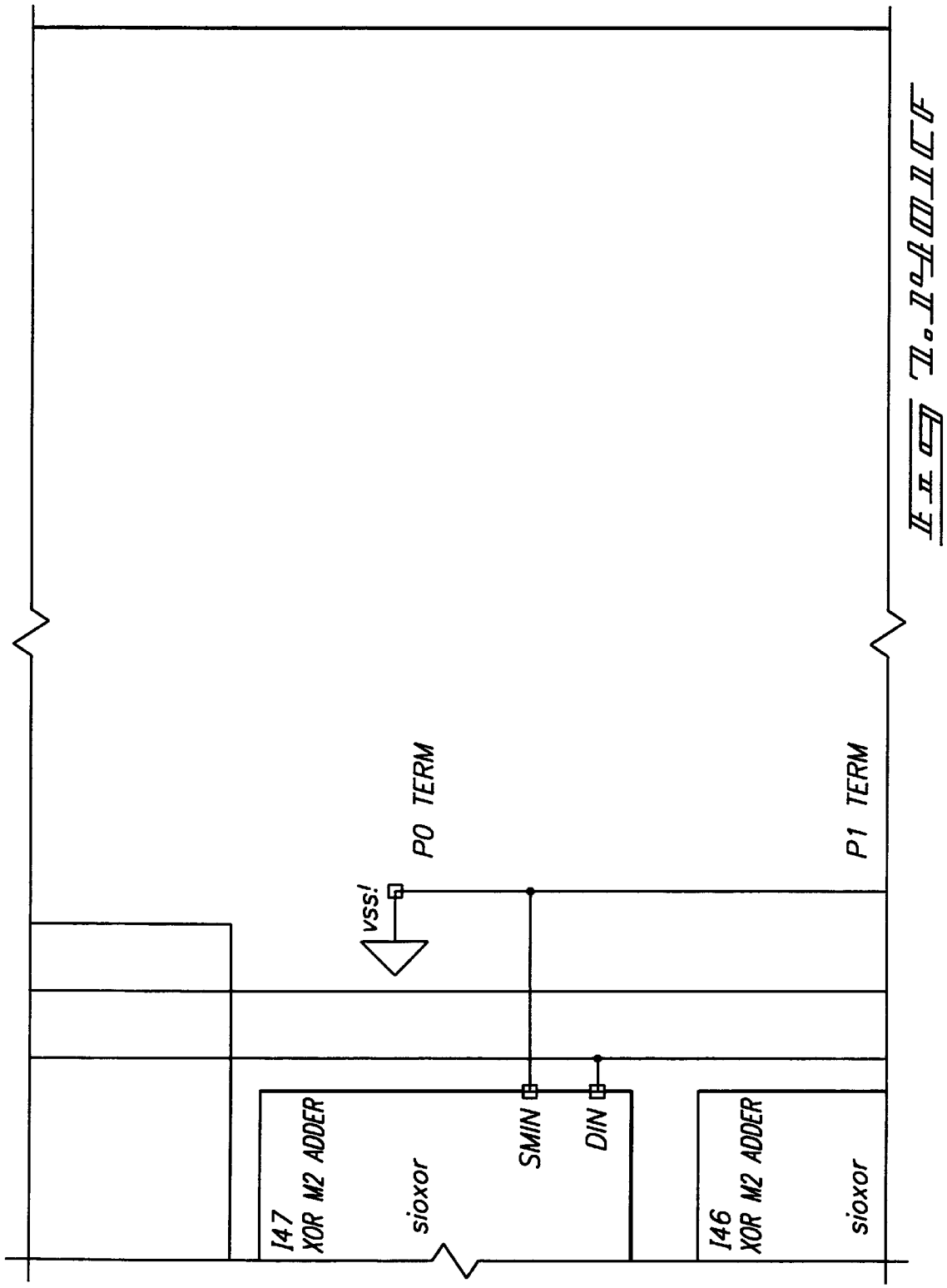


FIG. 11.0478
P0 TERM
P1 TERM
vss!
SMIN
DIN
147
XOR M2 ADDER
sioxor
146
XOR M2 ADDER
sioxor

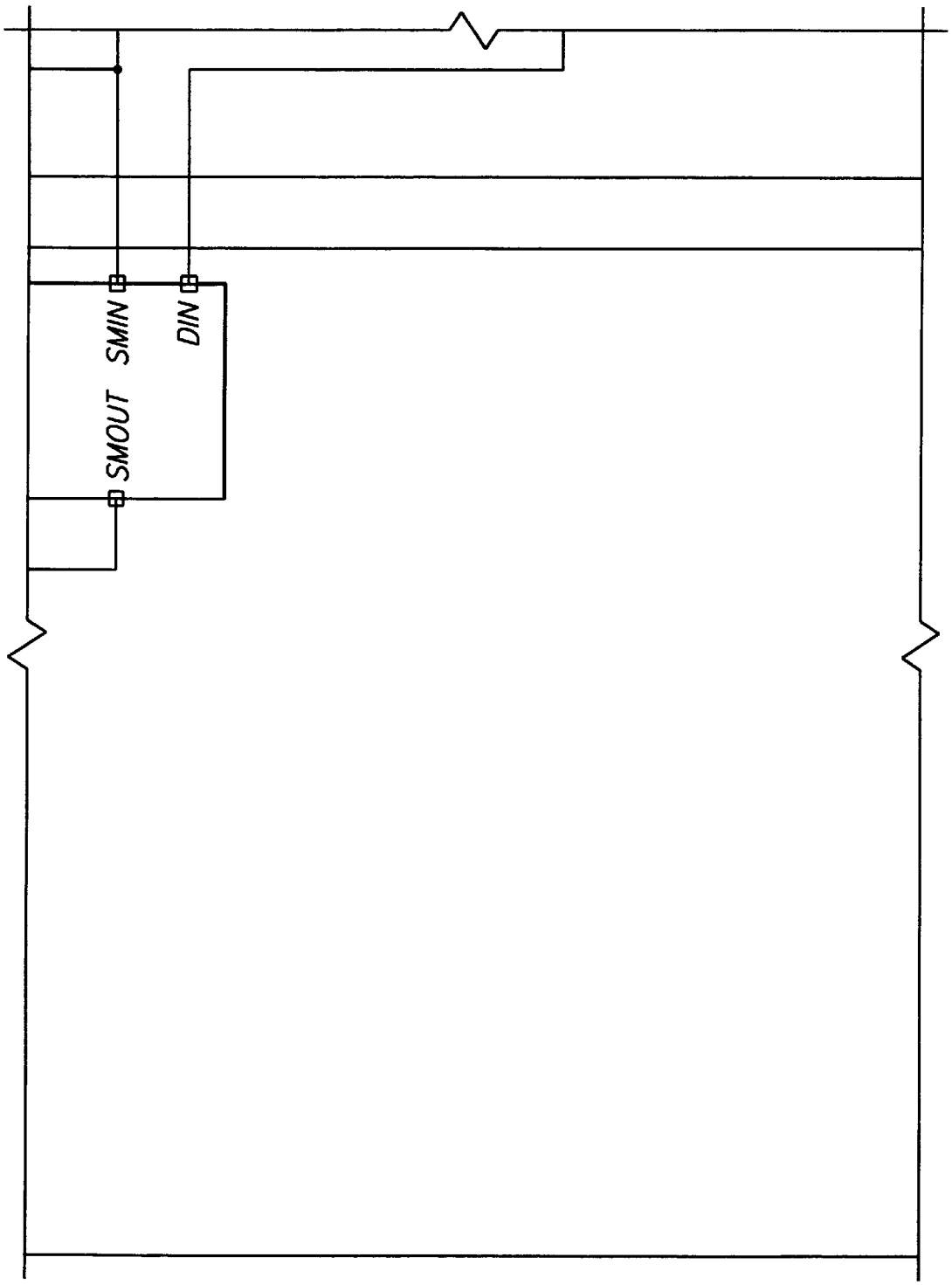


FIG 7.14MDA

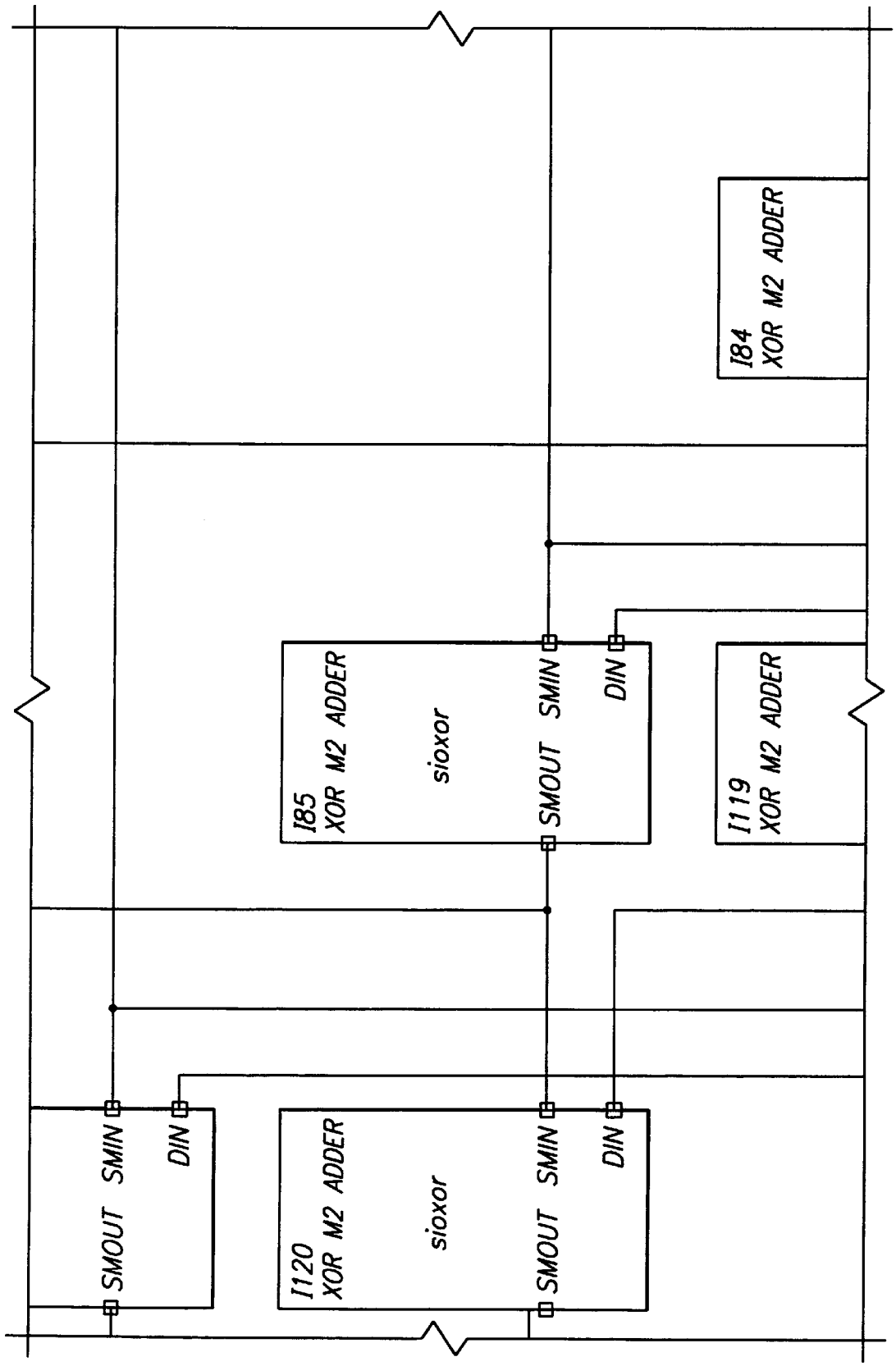

I84
XOR M2 ADDER
I85
XOR M2 ADDER
sioxor
SMOUT SMIN
DIN
I119
XOR M2 ADDER
I120
XOR M2 ADDER
sioxor
SMOUT SMIN
DIN

FIG. 1120

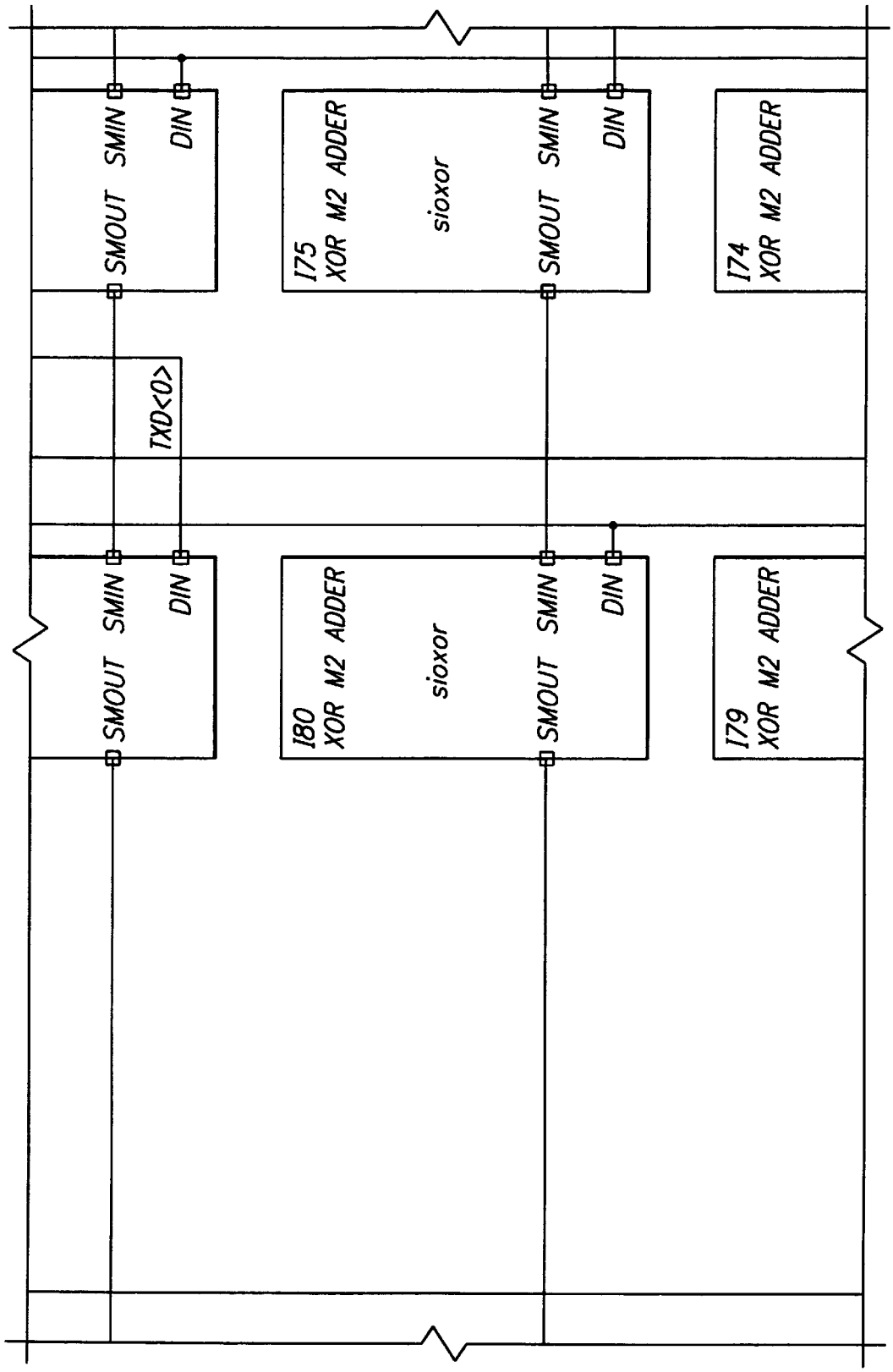


FIG. 11.0-11.1

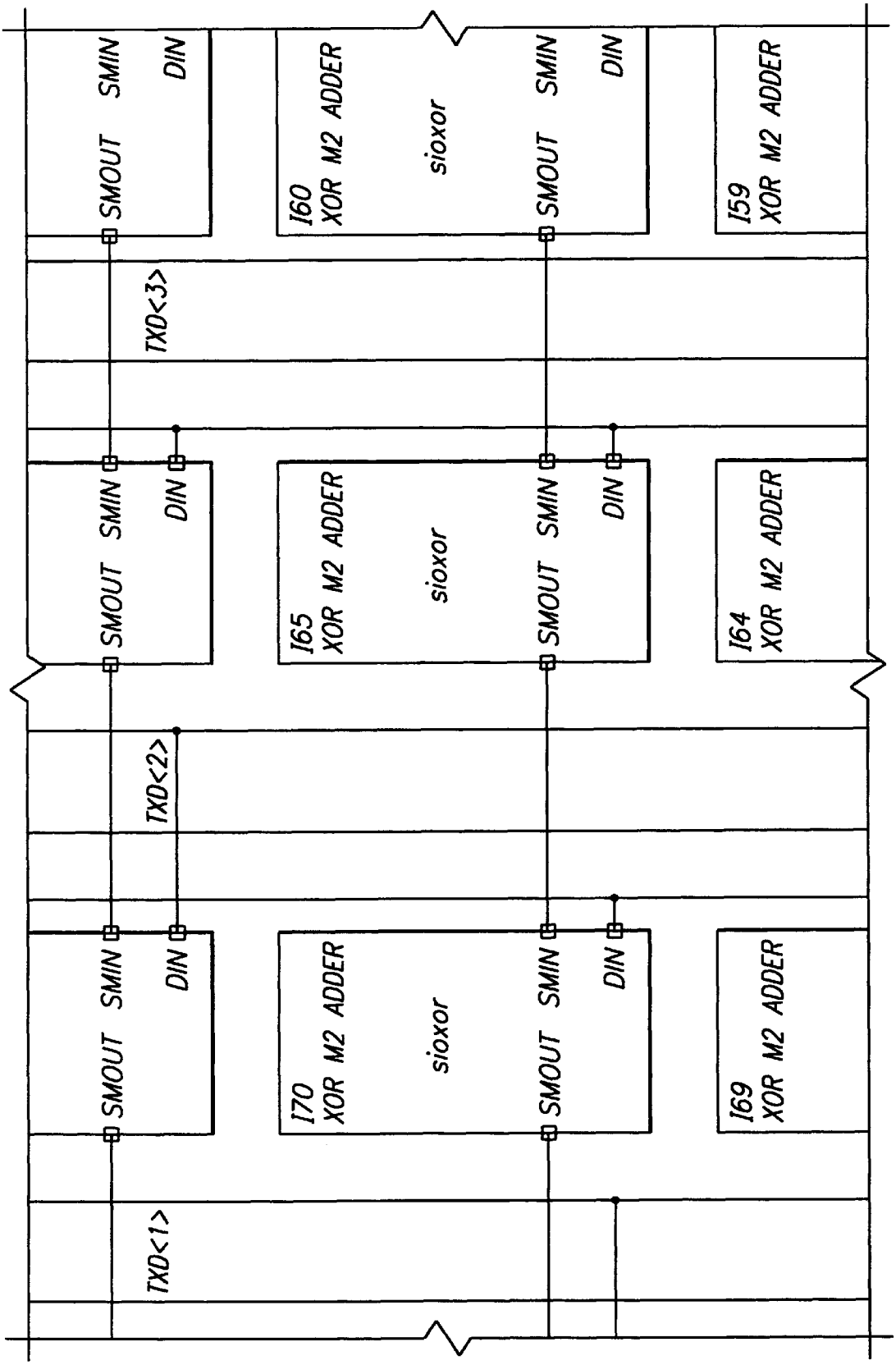
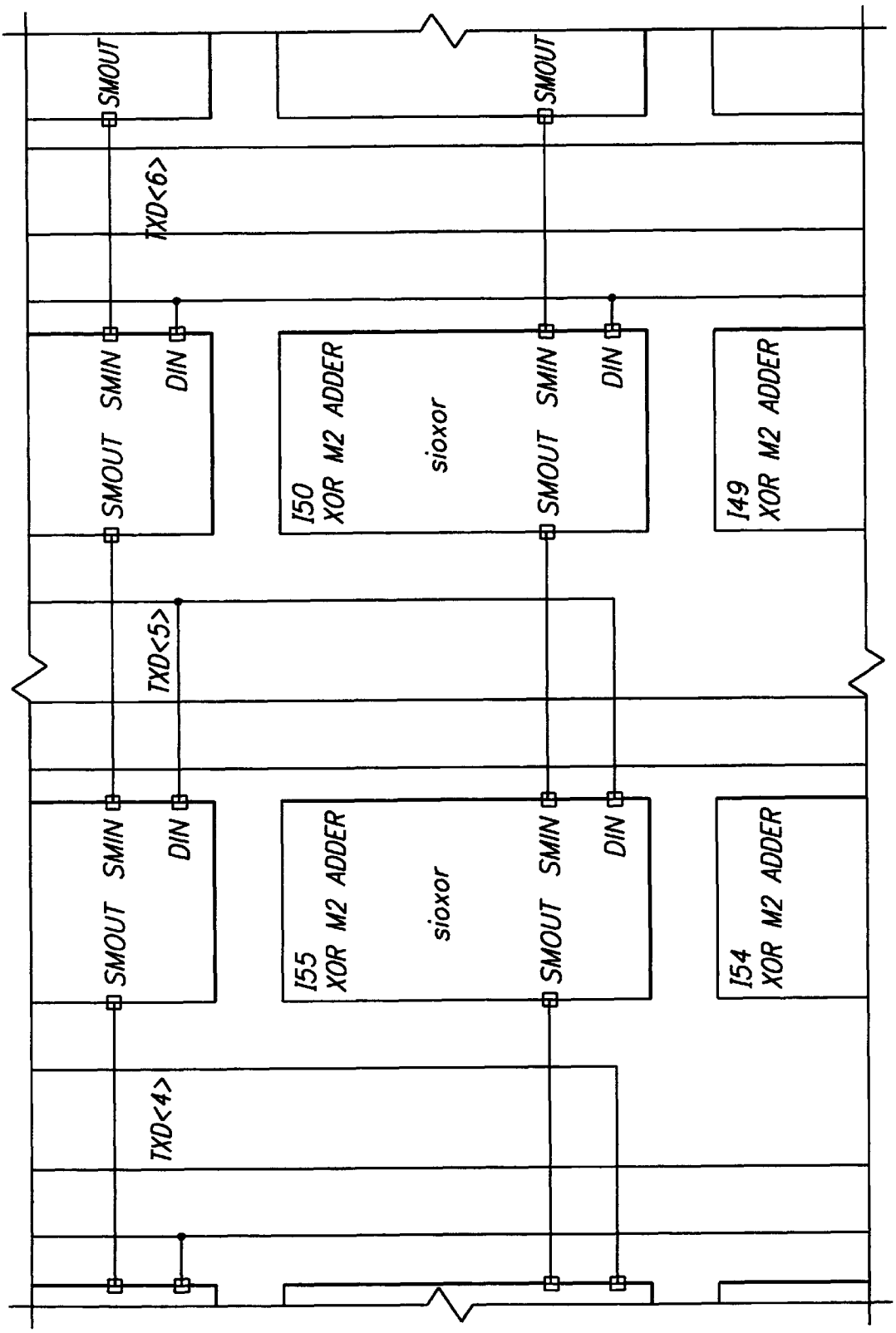

I70
XOR M2 ADDER
sioxor
SMOUT SMIN DIN
I69
XOR M2 ADDER
TXD<1>
I65
XOR M2 ADDER
I64
XOR M2 ADDER
TXD<2>
I60
XOR M2 ADDER
I59
XOR M2 ADDER
TXD<3>

FIG. 11


SMOUT
SMOUT
IXD<6>
SMOUT SMIN
DIN
I50
XOR M2 ADDER
sioxor
SMOUT SMIN
DIN
I49
XOR M2 ADDER
IXD<5>
SMOUT SMIN
DIN
I55
XOR M2 ADDER
sioxor
SMOUT SMIN
DIN
I54
XOR M2 ADDER
IXD<4>

ФИГ. 1145

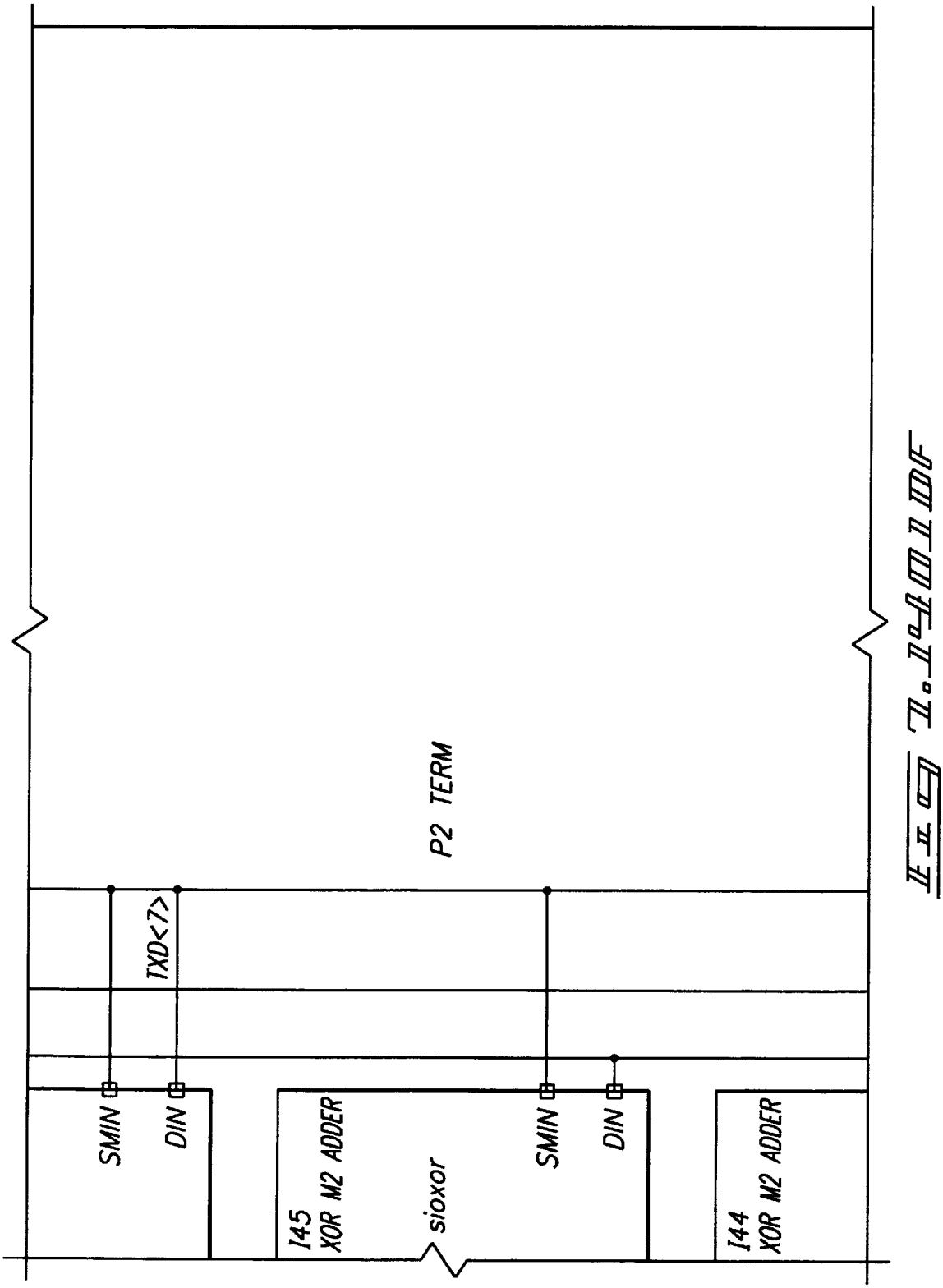


FIG. 11.0F.11.DF

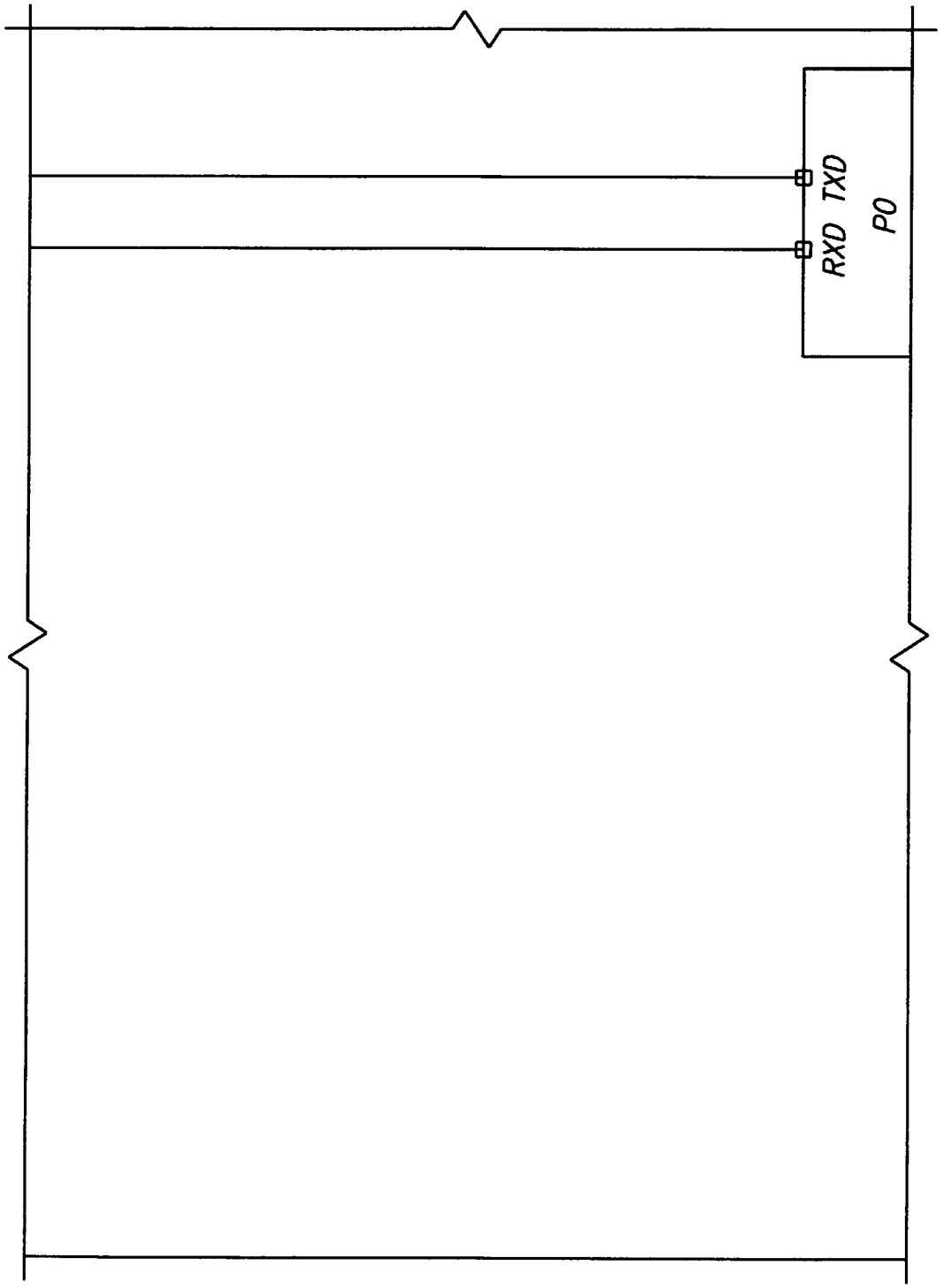
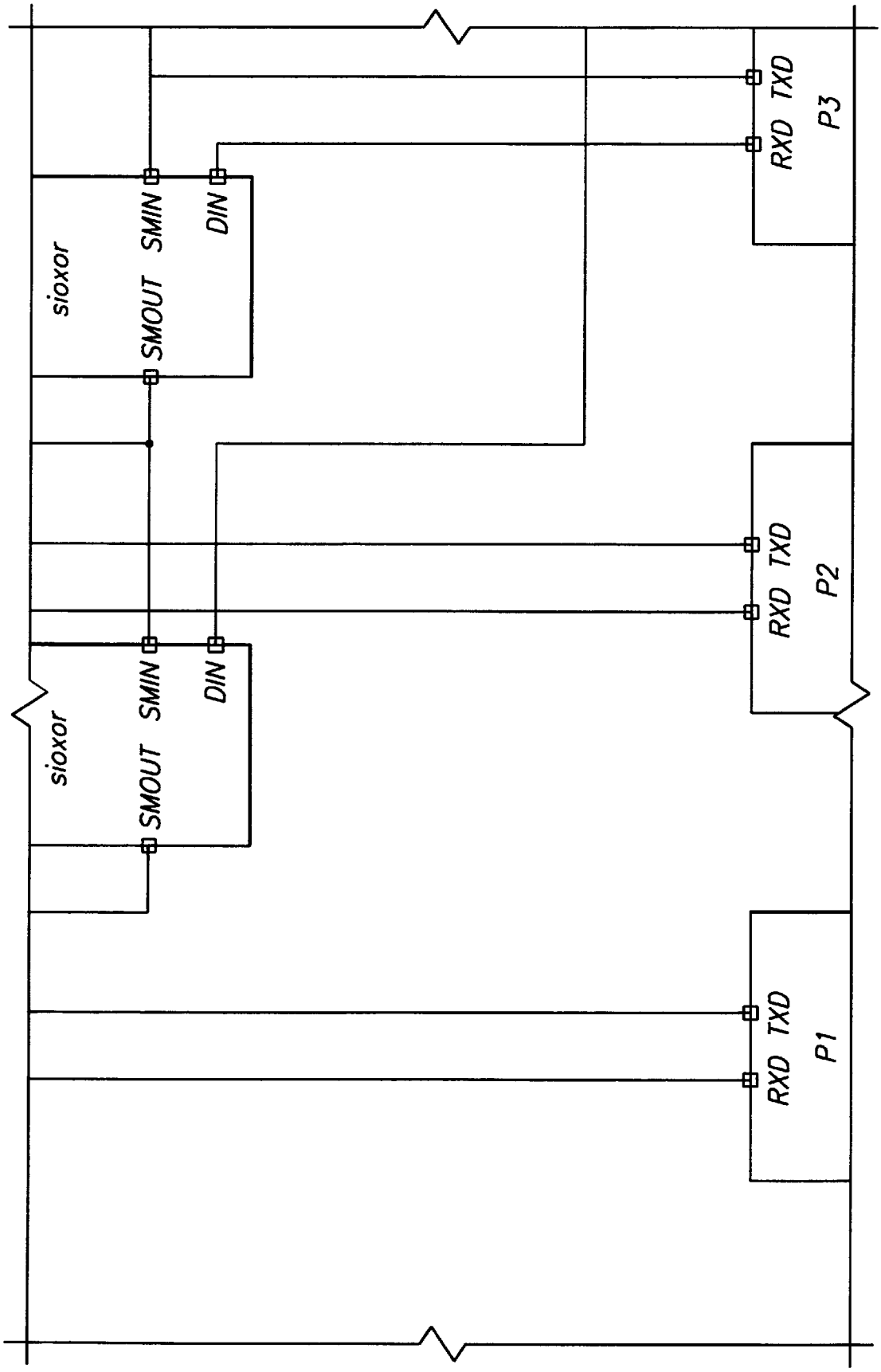
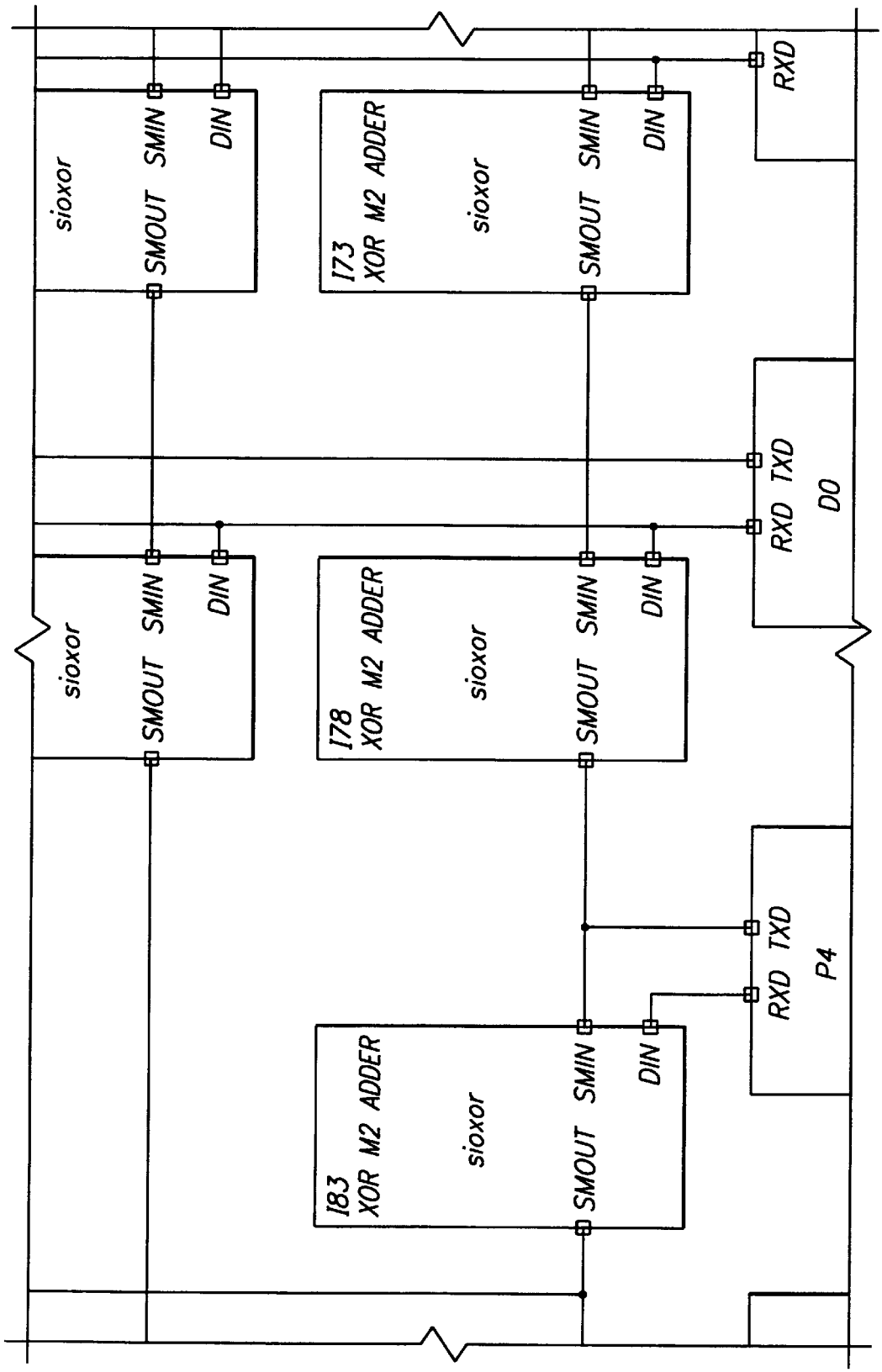


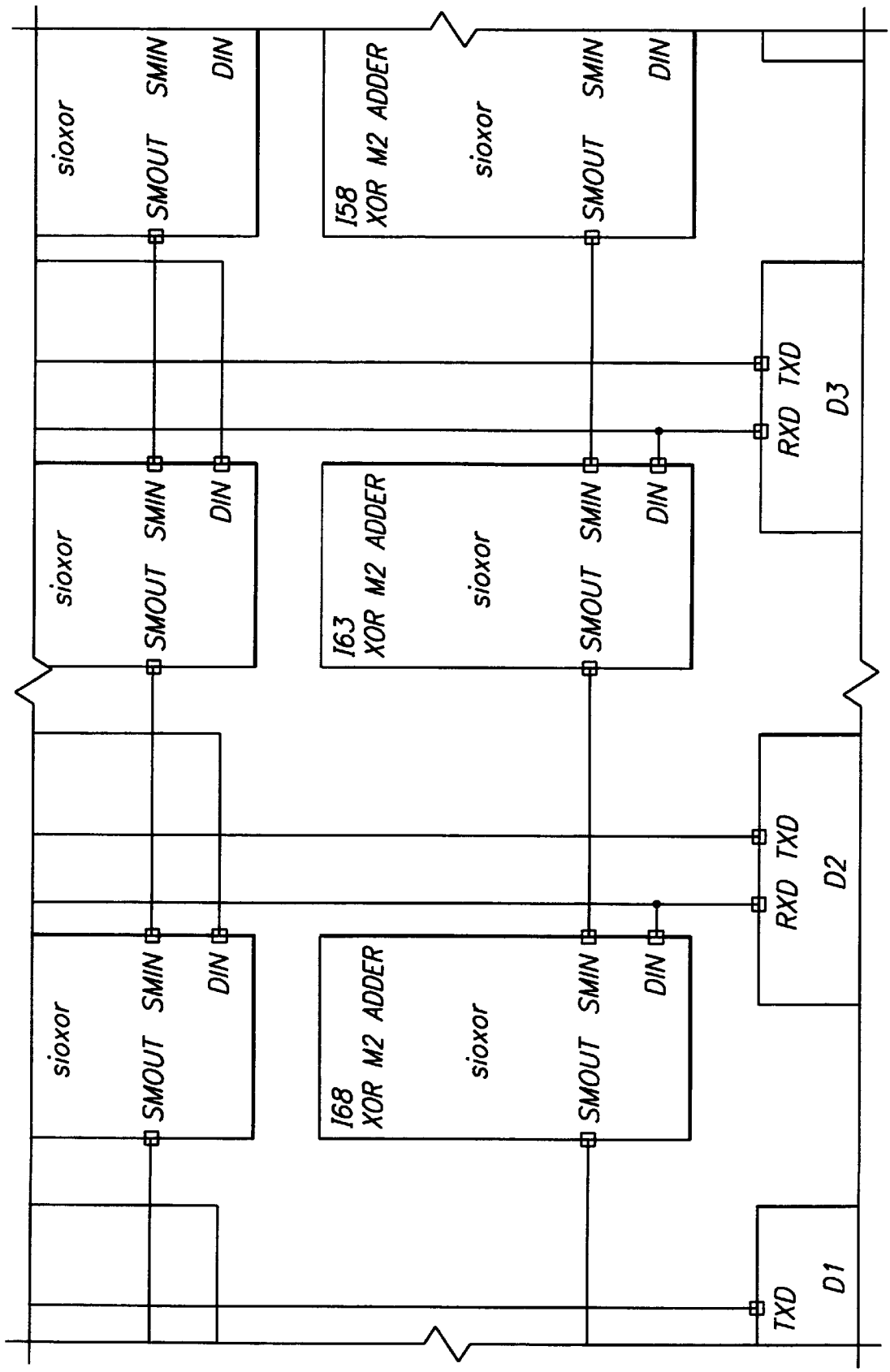
FIG. 11.4



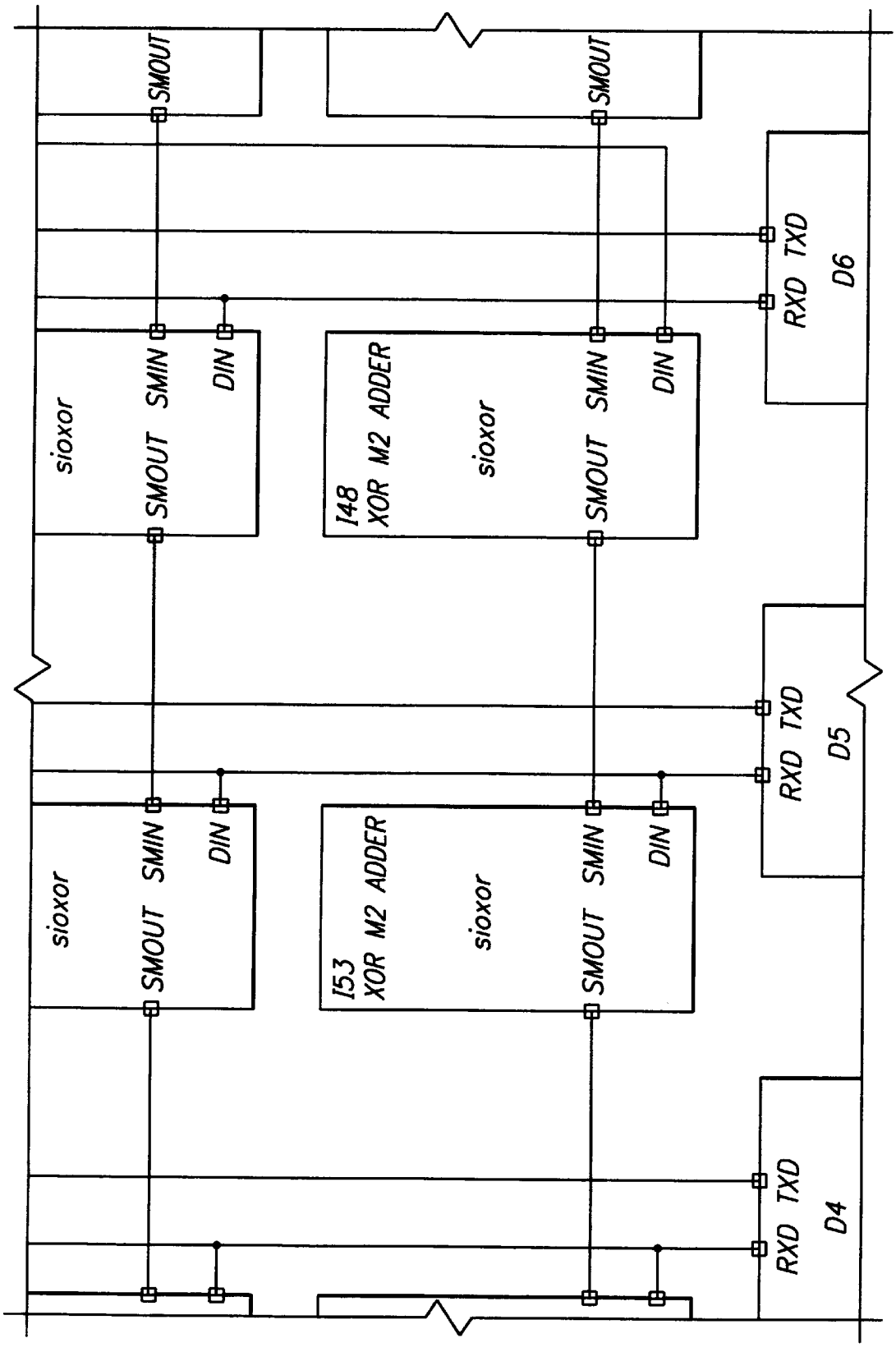
Фиг. 1.4.1.1.1


RXD
I73
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
RXD TXD
DO
I78
P4
I83

ФИГ. 11.


sioxor
SMIN
SMOUT
DIN
I58
XOR M2 ADDER
I63
I68
RXD TXD
D3
D2
D1
TXD

Фиг. 114


SMOUT
SMOUT
RXD TXD
D6
sioxor
SMIN
SMOUT
DIN
148
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
RXD TXD
D5
sioxor
SMIN
SMOUT
DIN
153
XOR M2 ADDER
sioxor
SMIN
SMOUT
DIN
RXD TXD
D4

Фиг. 149

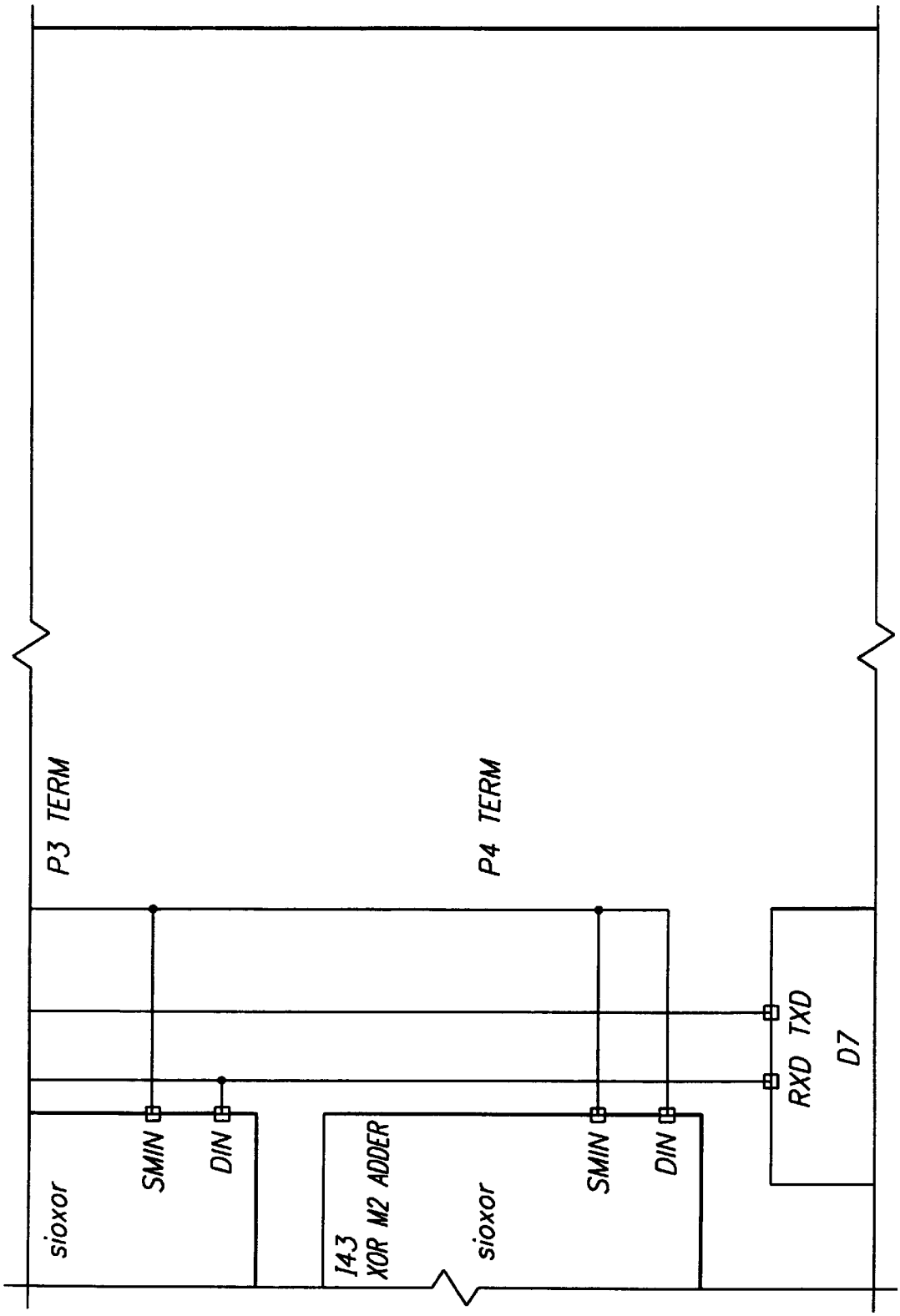

P3 TERM
P4 TERM
RXD TXD
D7
SMIN
DIN
sioxor
143
XOR M2 ADDER
SMIN
DIN
sioxor

FIG 9L

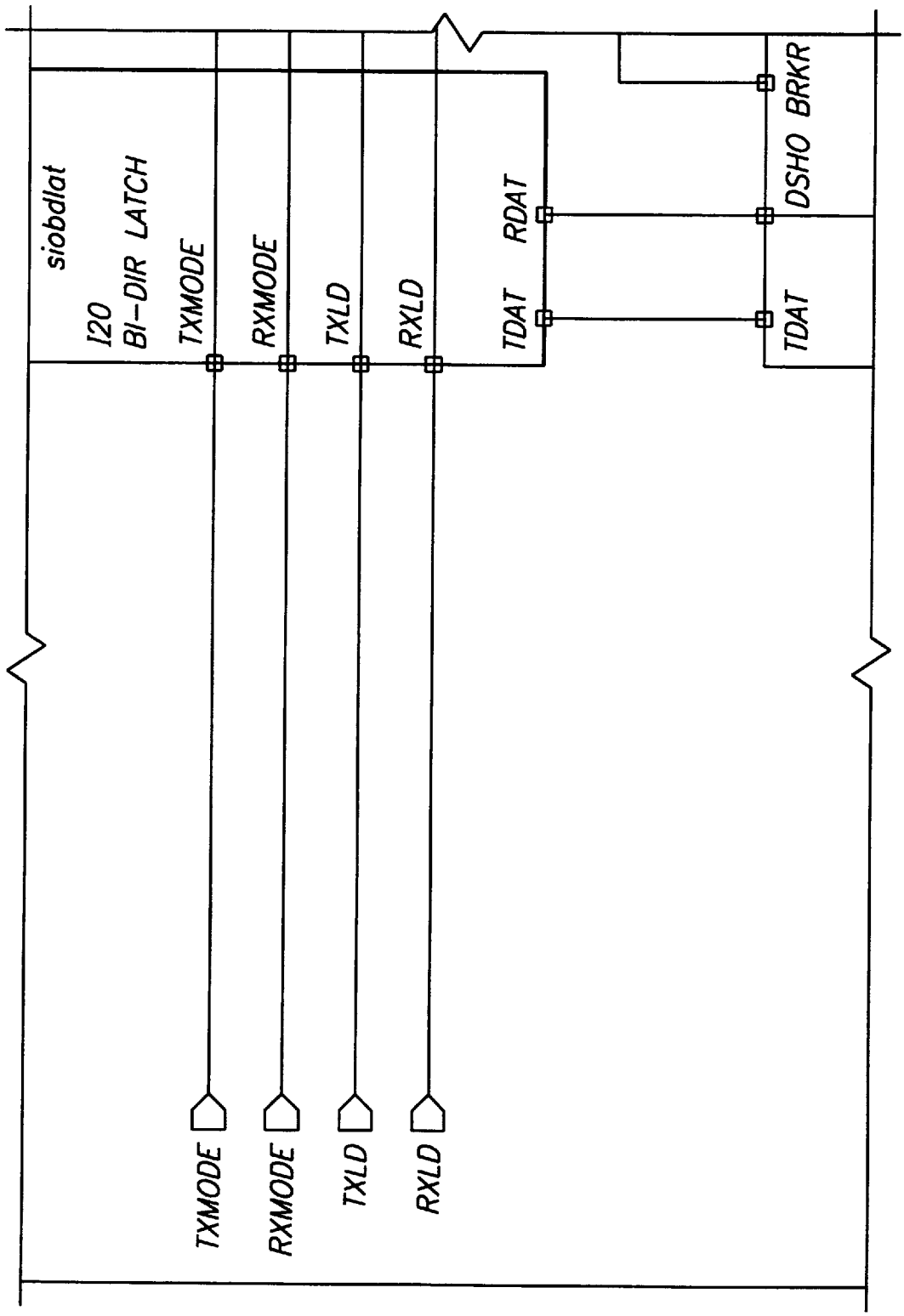


FIG. 11.14.00.11FA

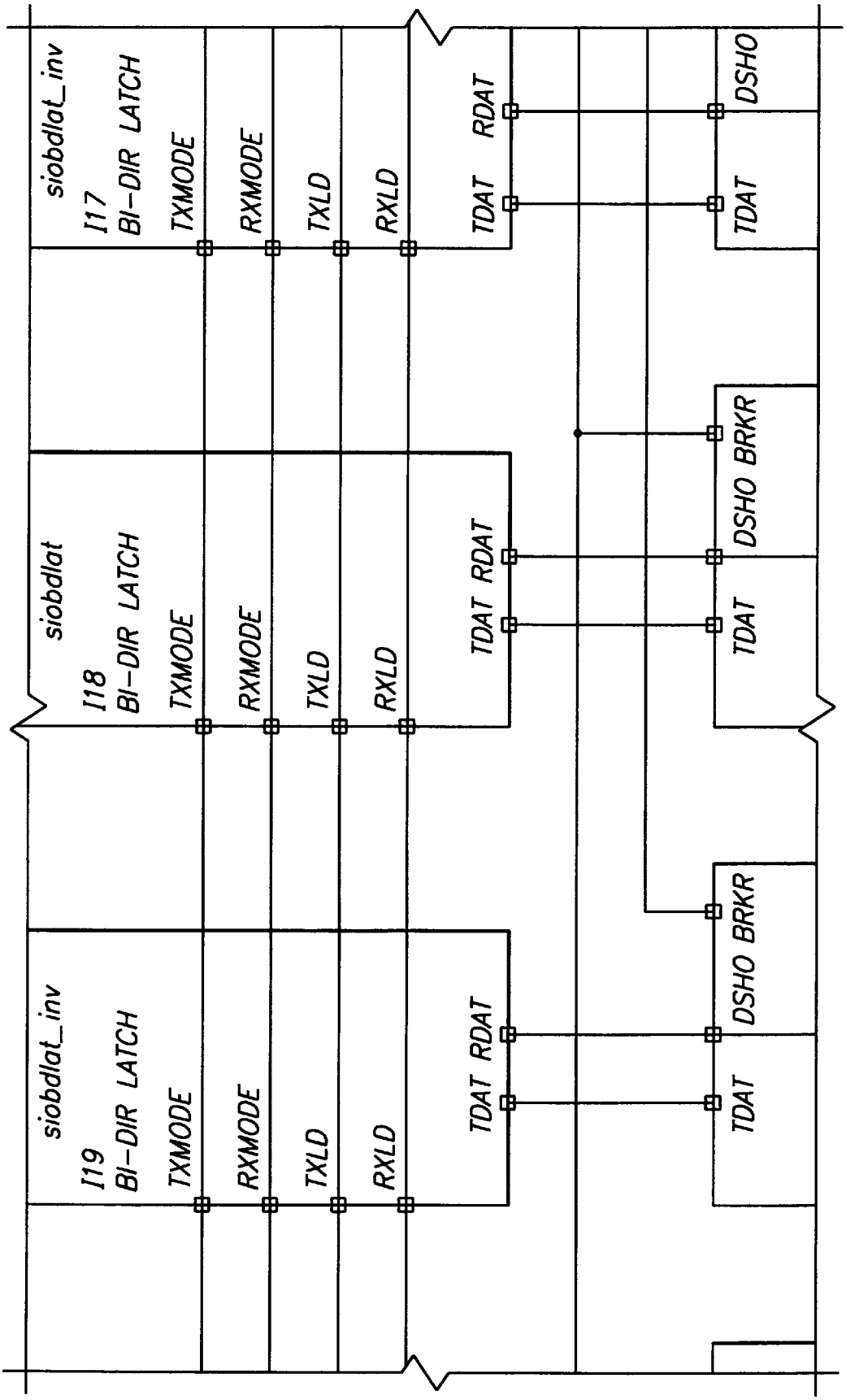

siobdlat_inv
I17
BI-DIR LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT RDAT
DSHO
TDAT
siobdlat
I18
BI-DIR LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT RDAT
DSHO BRKR
TDAT
siobdlat_inv
I19
BI-DIR LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT RDAT
DSHO BRKR
TDAT

FIG. 11.

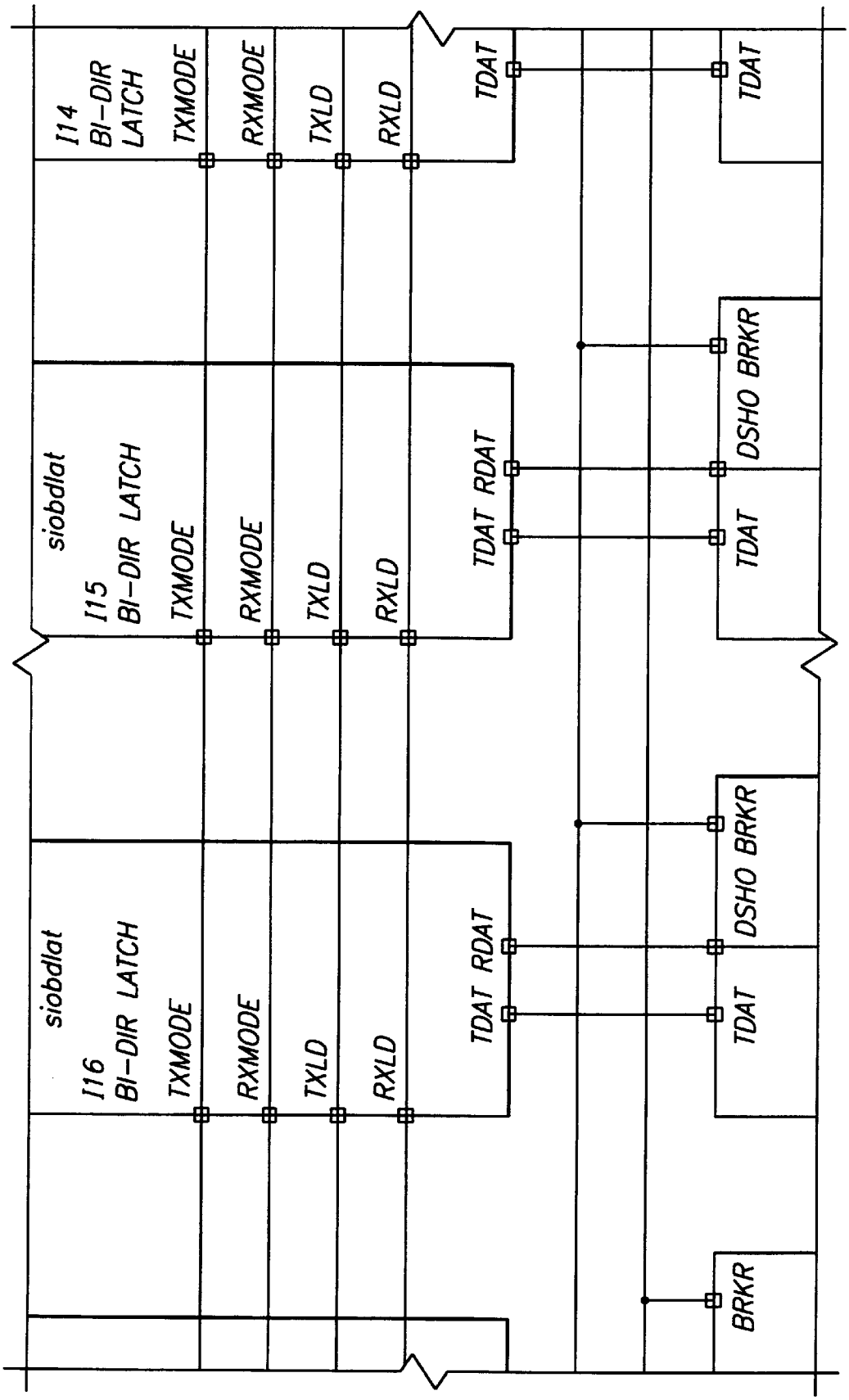

I14
BI-DIR
LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT
TDAT
siobdlat
I15
BI-DIR LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT RDAT
DSHO BRKR
TDAT
siobdlat
I16
BI-DIR LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT RDAT
DSHO BRKR
TDAT
BRKR

FIG. 11.

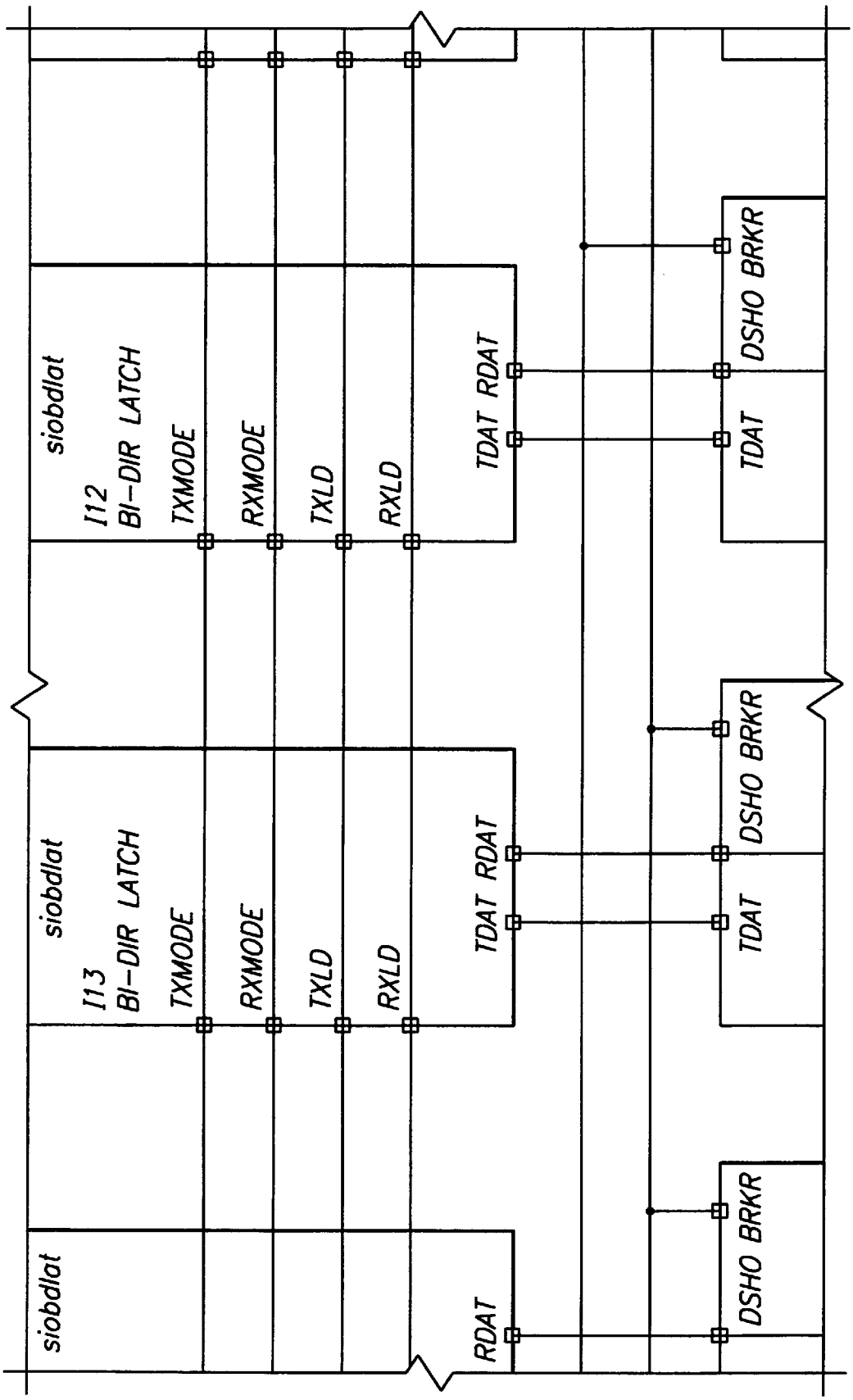

siobdlat
I12
BI-DIR LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT RDAT
DSHO BRKR
TDAT
siobdlat
I13
BI-DIR LATCH
TXMODE
RXMODE
TXLD
RXLD
TDAT RDAT
DSHO BRKR
TDAT
siobdlat
RDAT
DSHO BRKR

FIG. 114

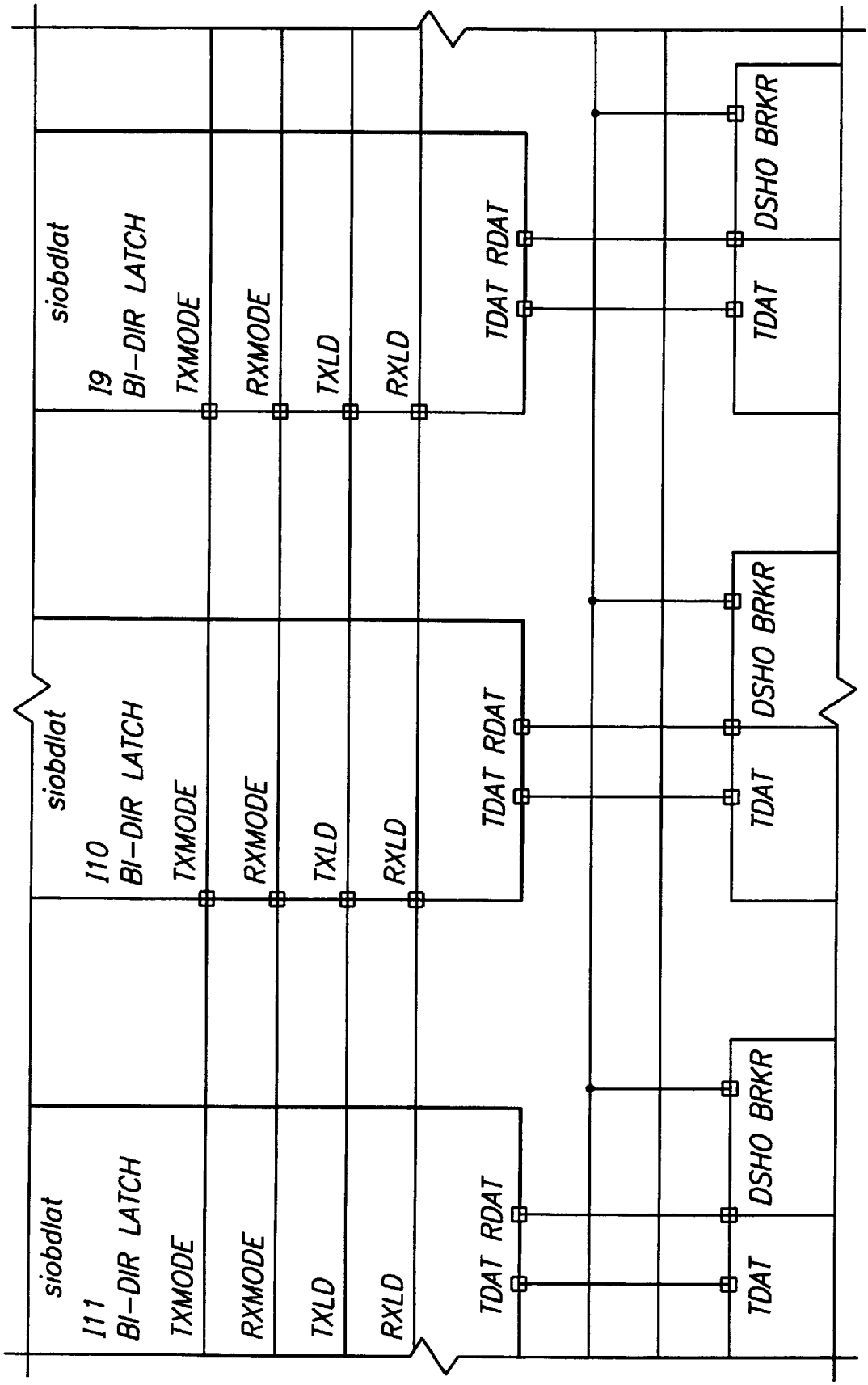


FIG. 114-00011F

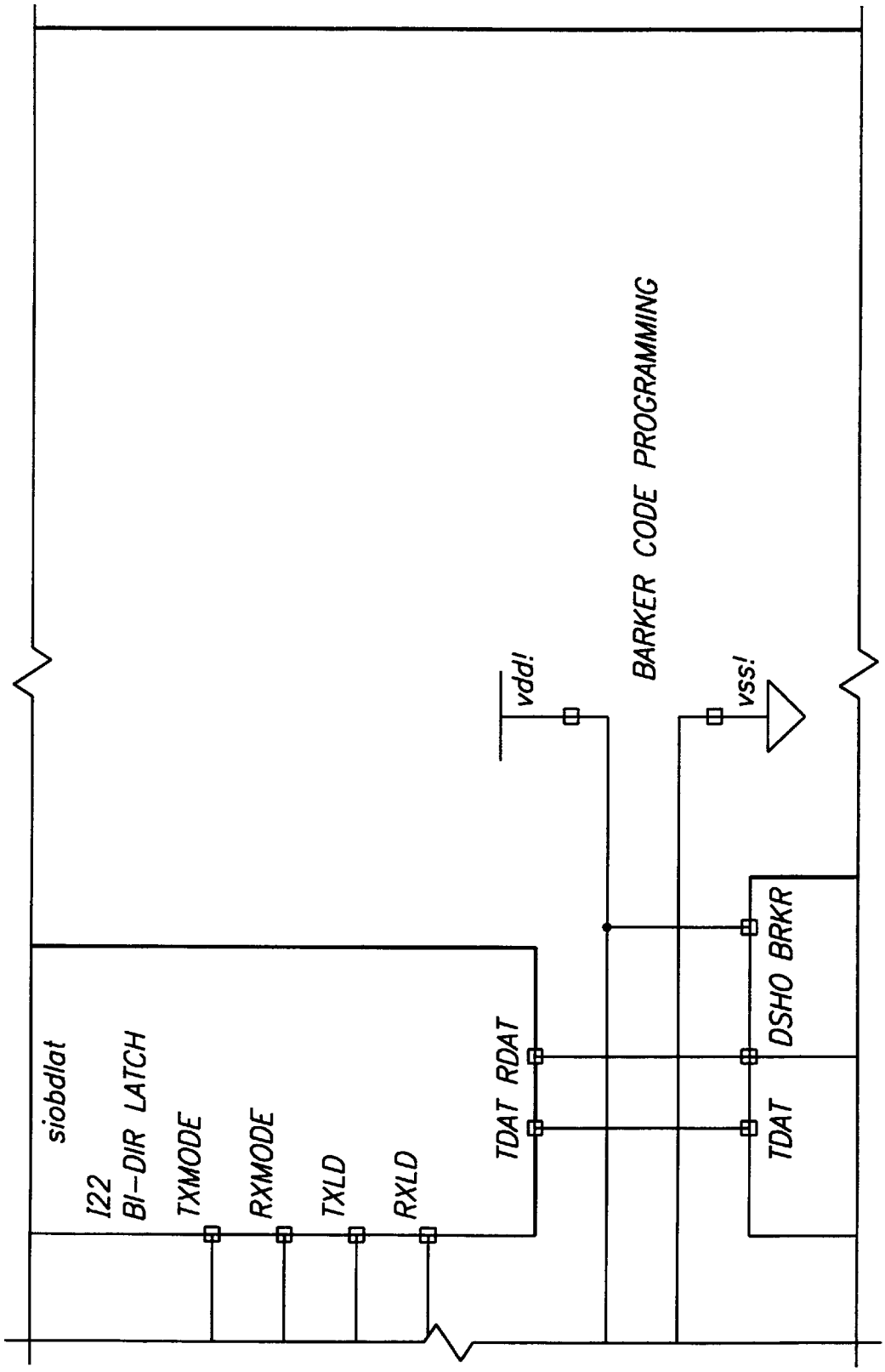


FIG. 11.14.11FF

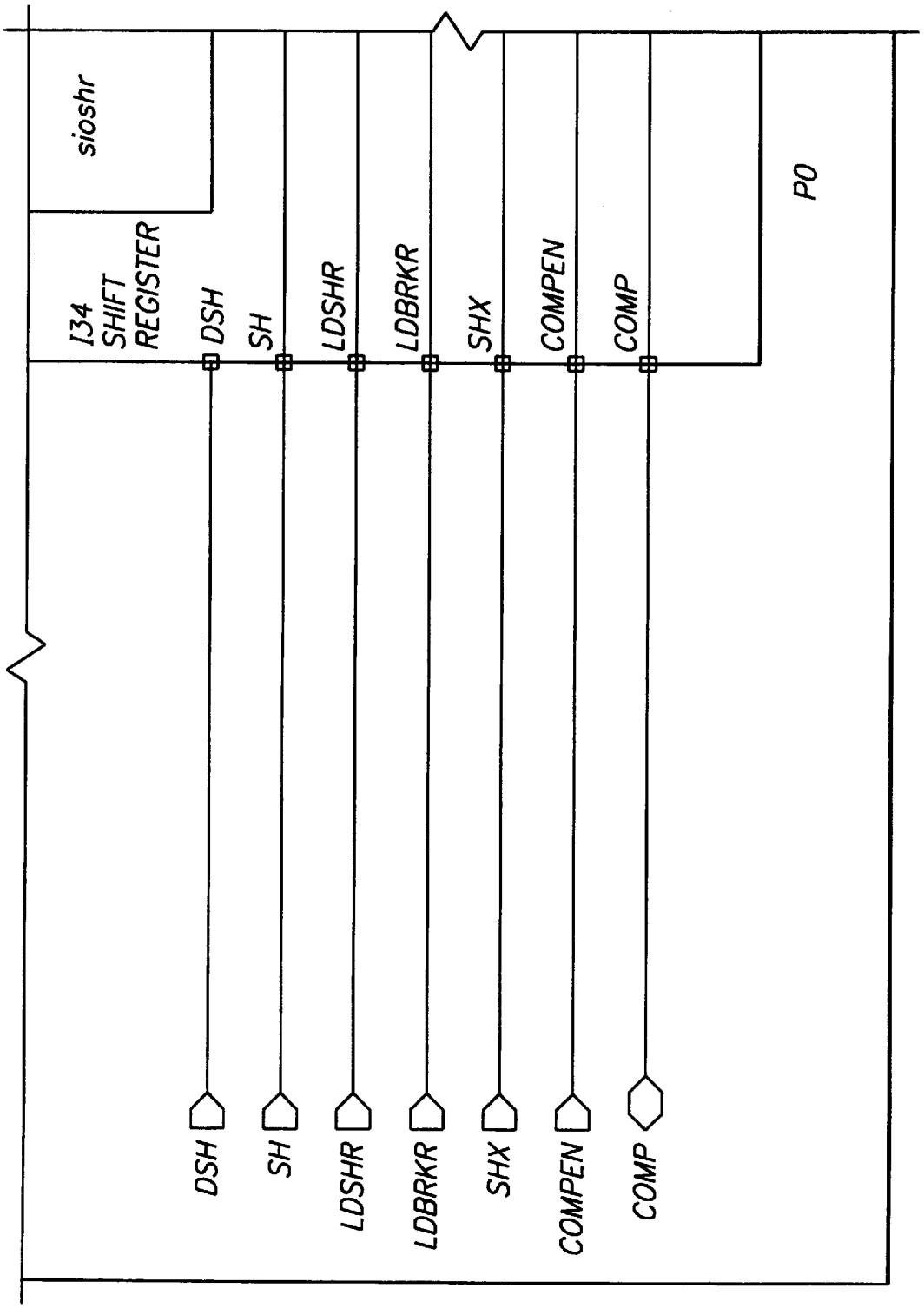

sioshr
I34
SHIFT
REGISTER
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
PO
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP

FIG 1170

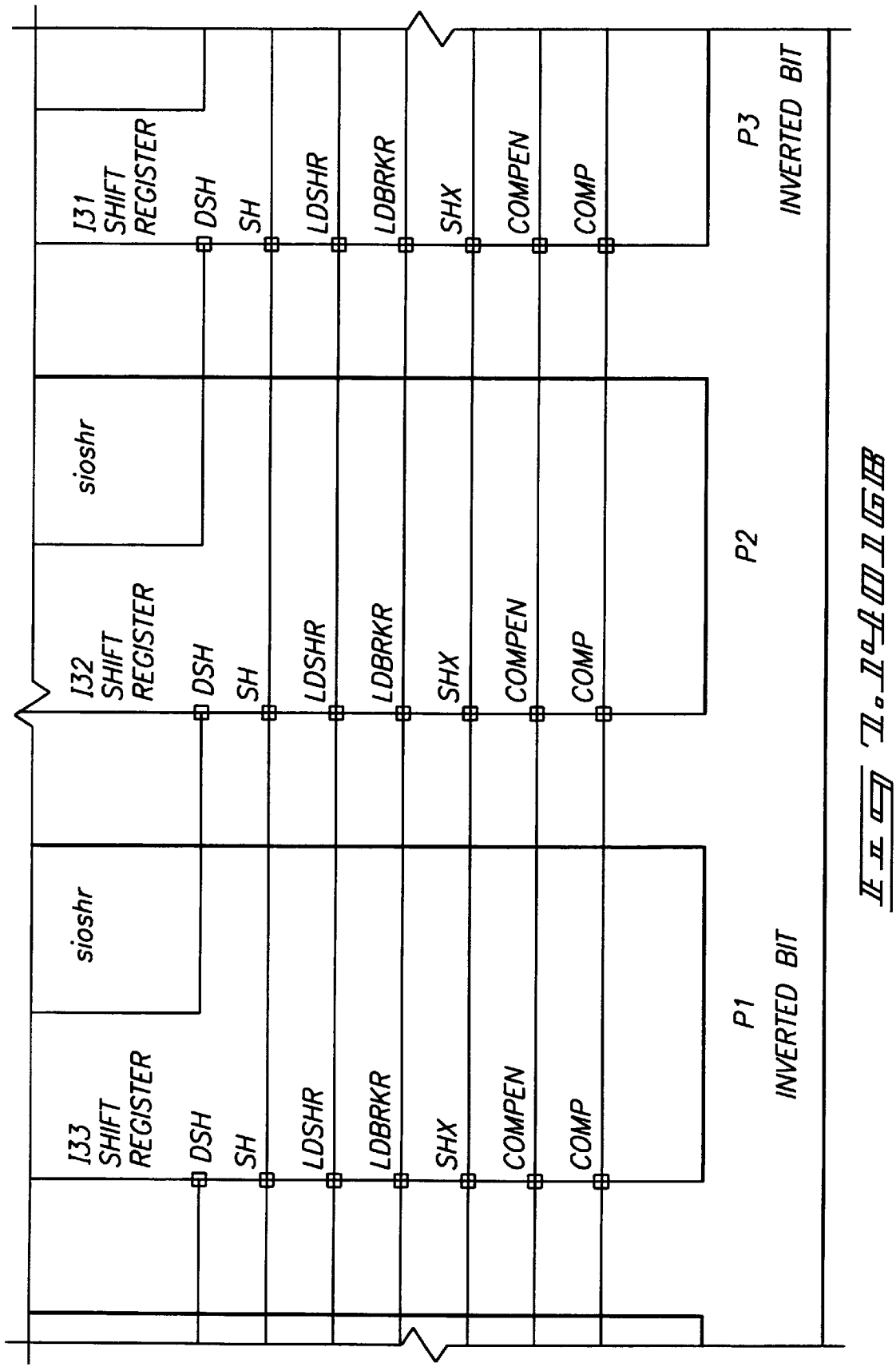

I31 SHIFT REGISTER
I32 SHIFT REGISTER
I33 SHIFT REGISTER
sioshr
sioshr
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
P3 INVERTED BIT
P2
P1 INVERTED BIT

Fig. 11a-11b

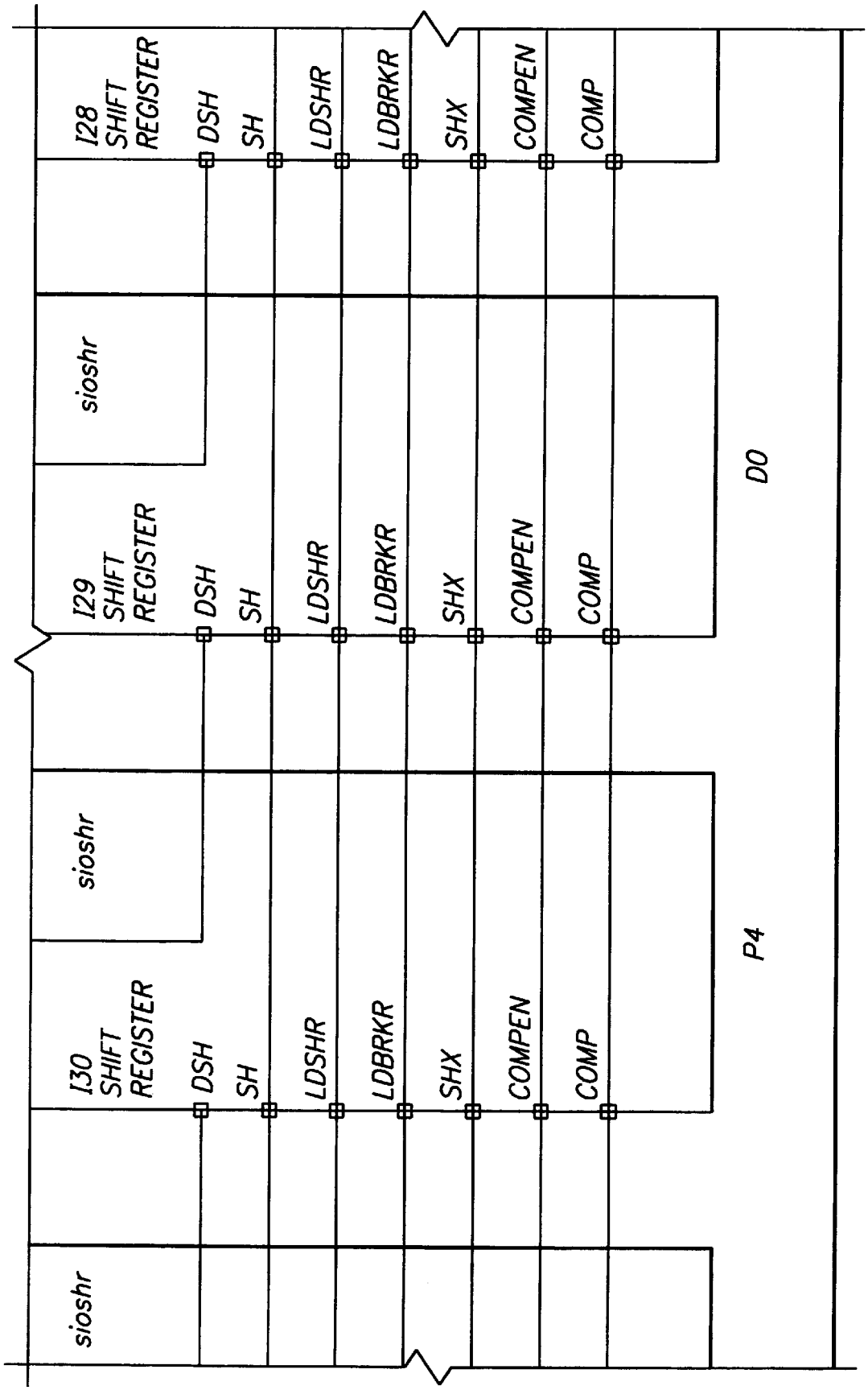

I28 SHIFT REGISTER
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
sioshr
I29 SHIFT REGISTER
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
sioshr
I30 SHIFT REGISTER
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
sioshr
D0
P4

FIG. 971

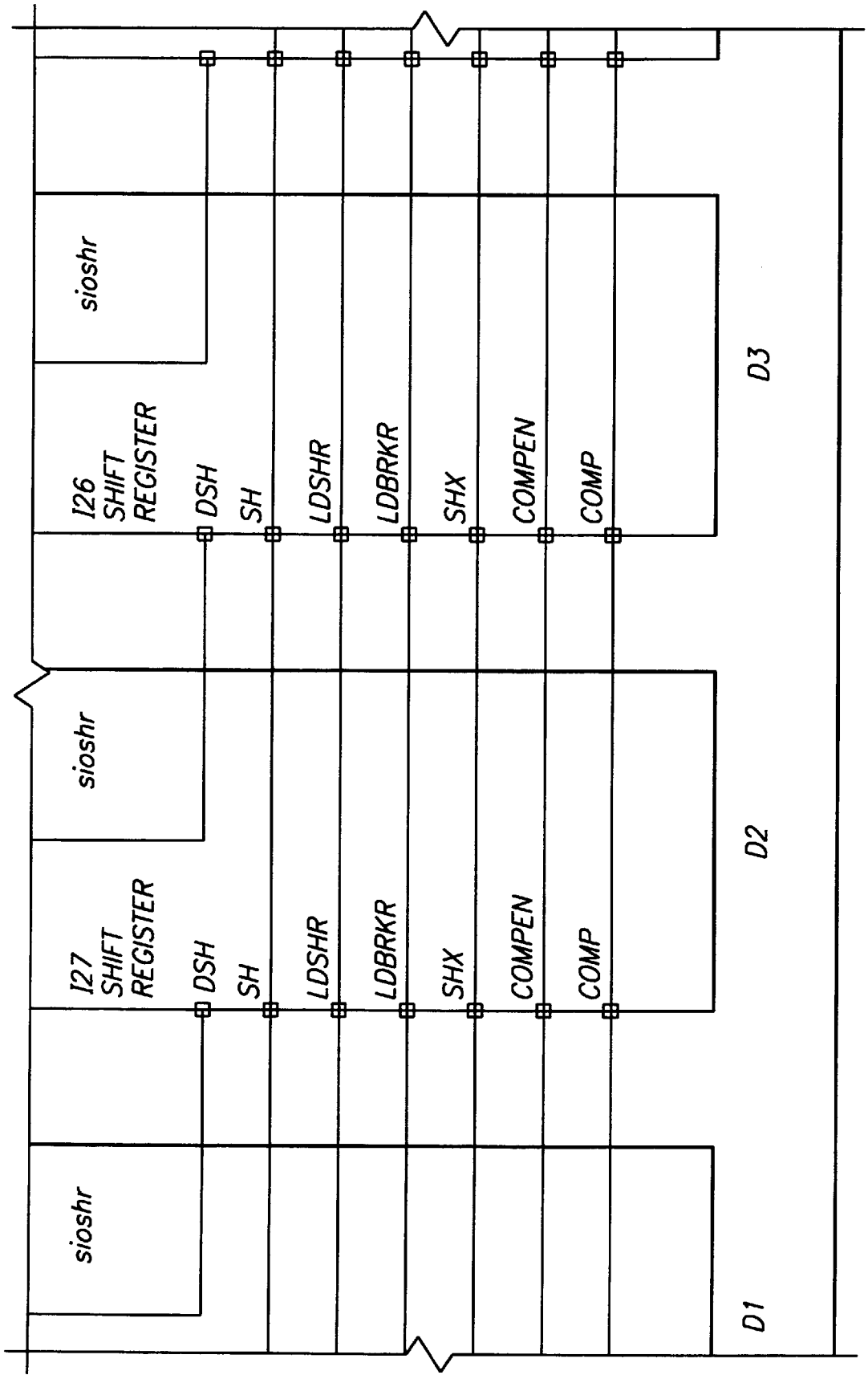


FIG. 114 (SHEET 972 OF 3273)

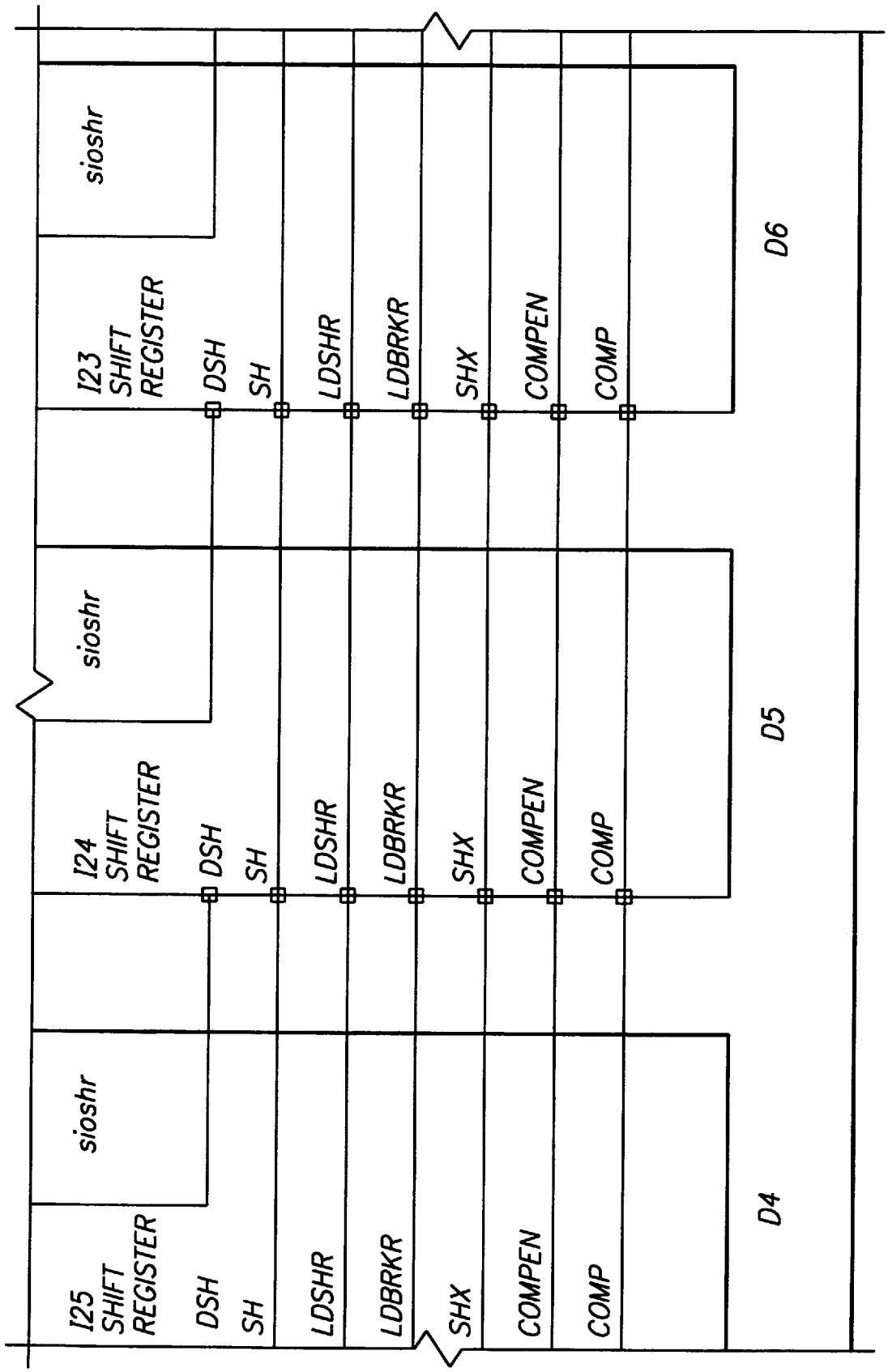

I25 SHIFT REGISTER
sioshr
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
D4
I24 SHIFT REGISTER
sioshr
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
D5
I23 SHIFT REGISTER
sioshr
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
D6

FIG. 11.405

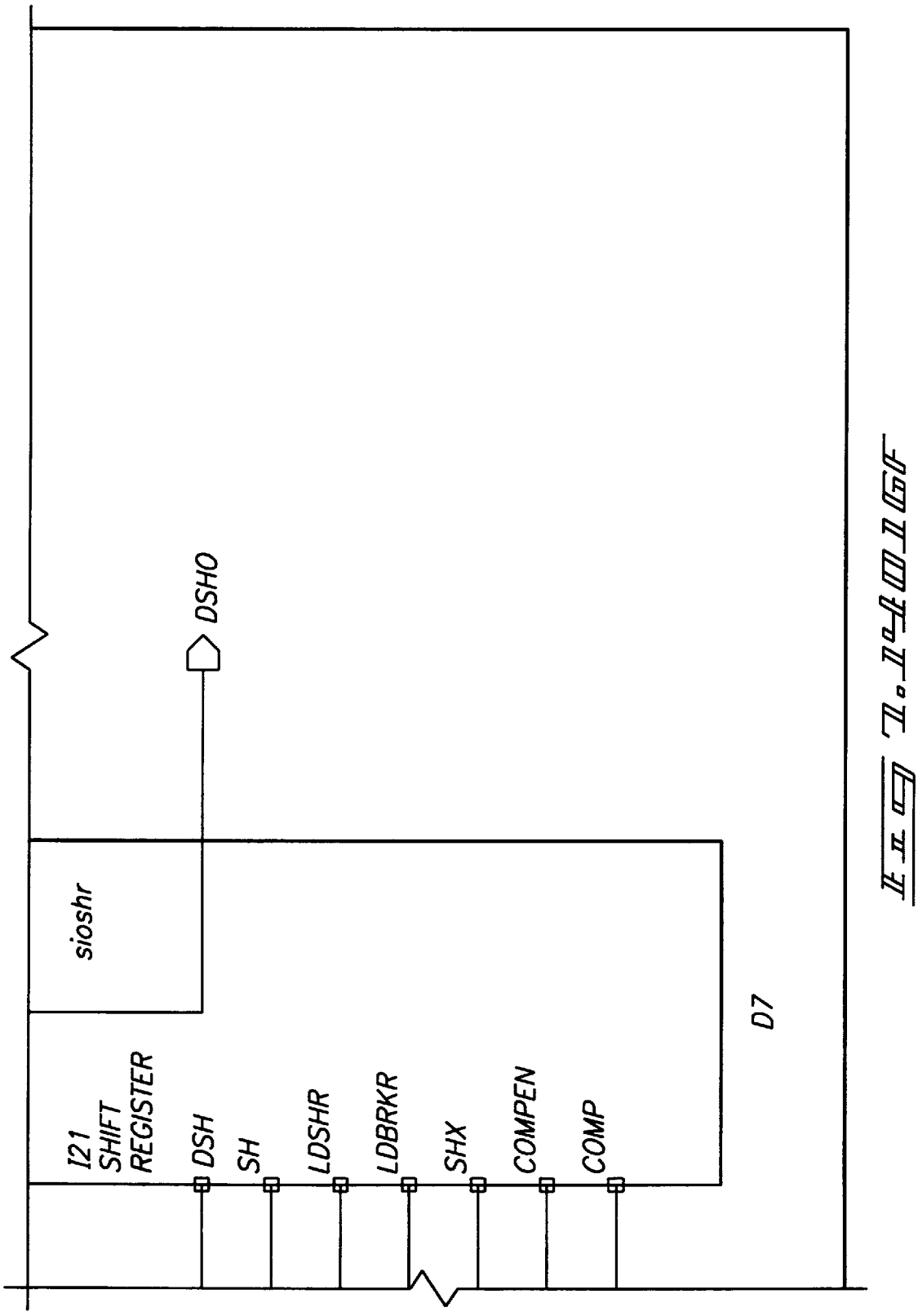

DSHO
sioshr
I21
SHIFT
REGISTER
DSH
SH
LDSHR
LDBRKR
SHX
COMPEN
COMP
D7

FIG. 11.1405F

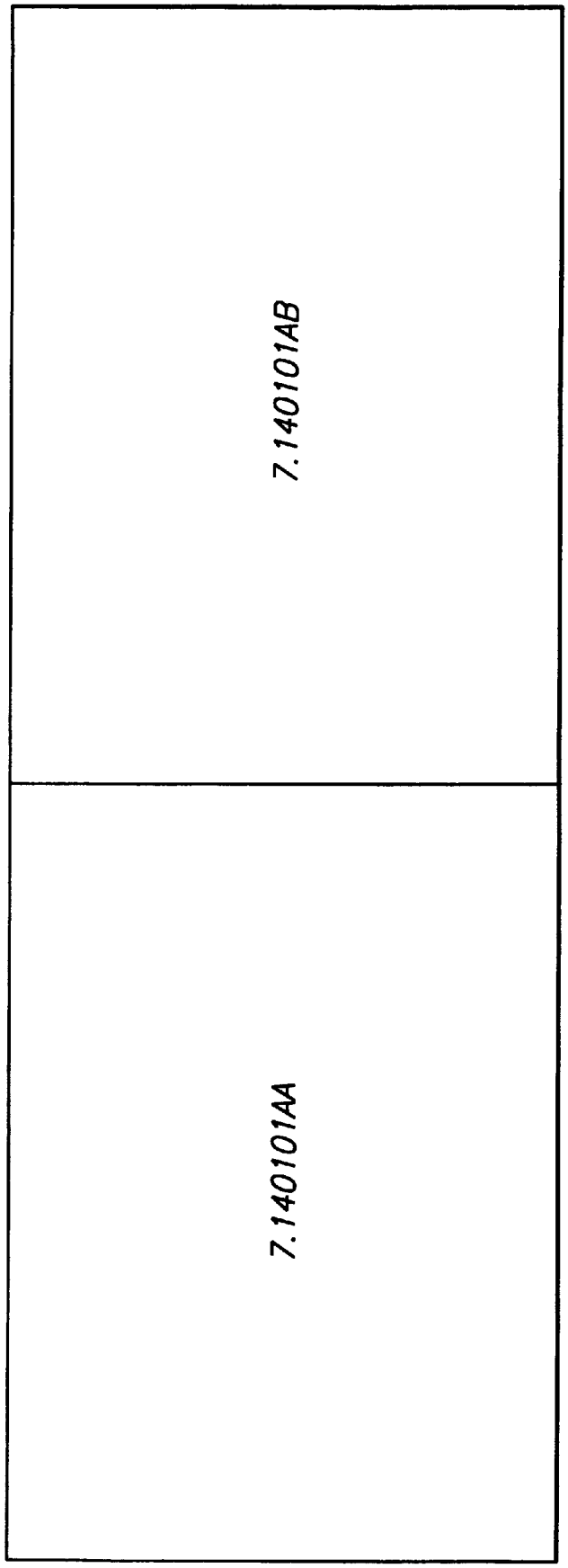


FIG. 7.140101

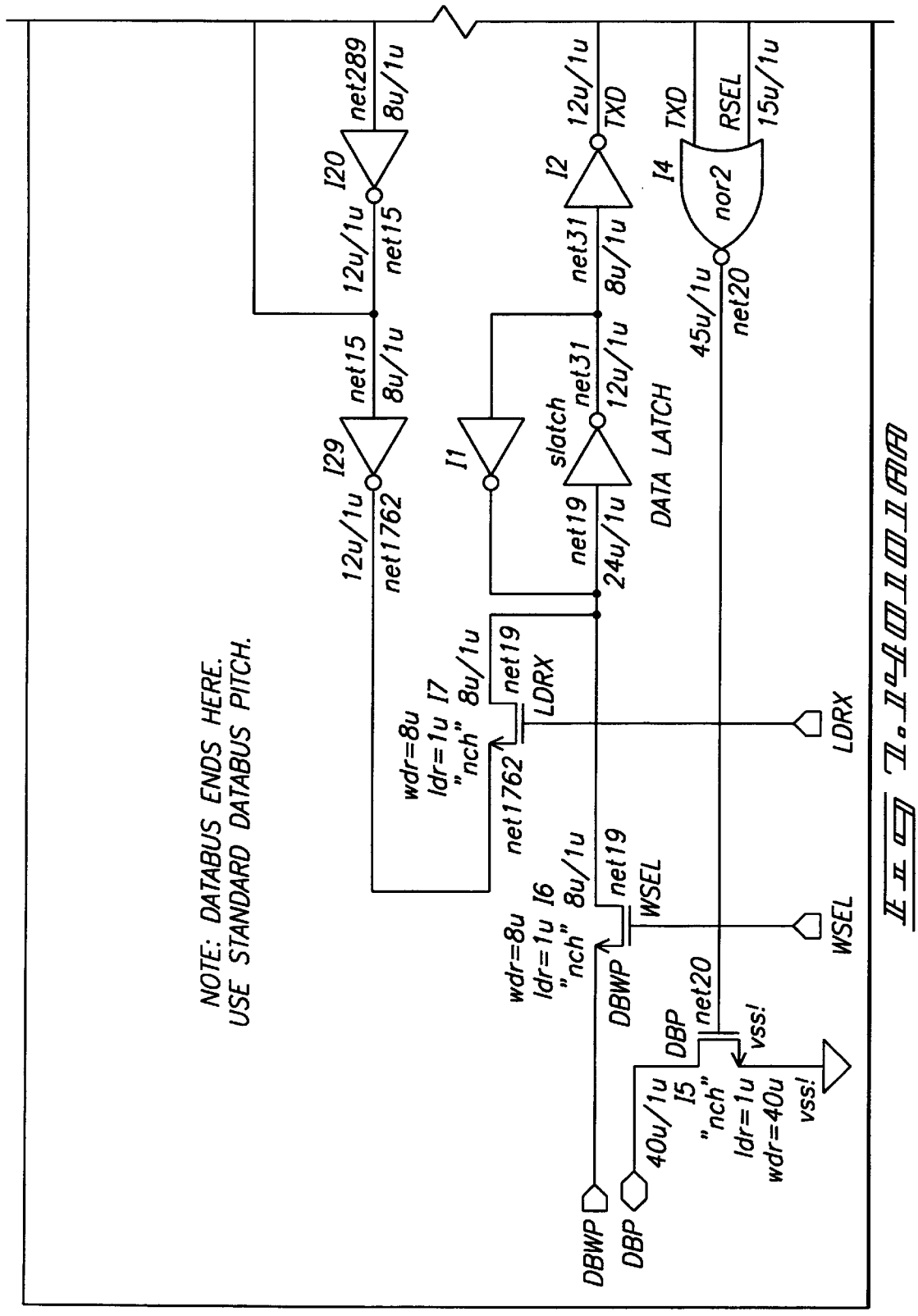


FIG. 11.0.11.00.11.AAA

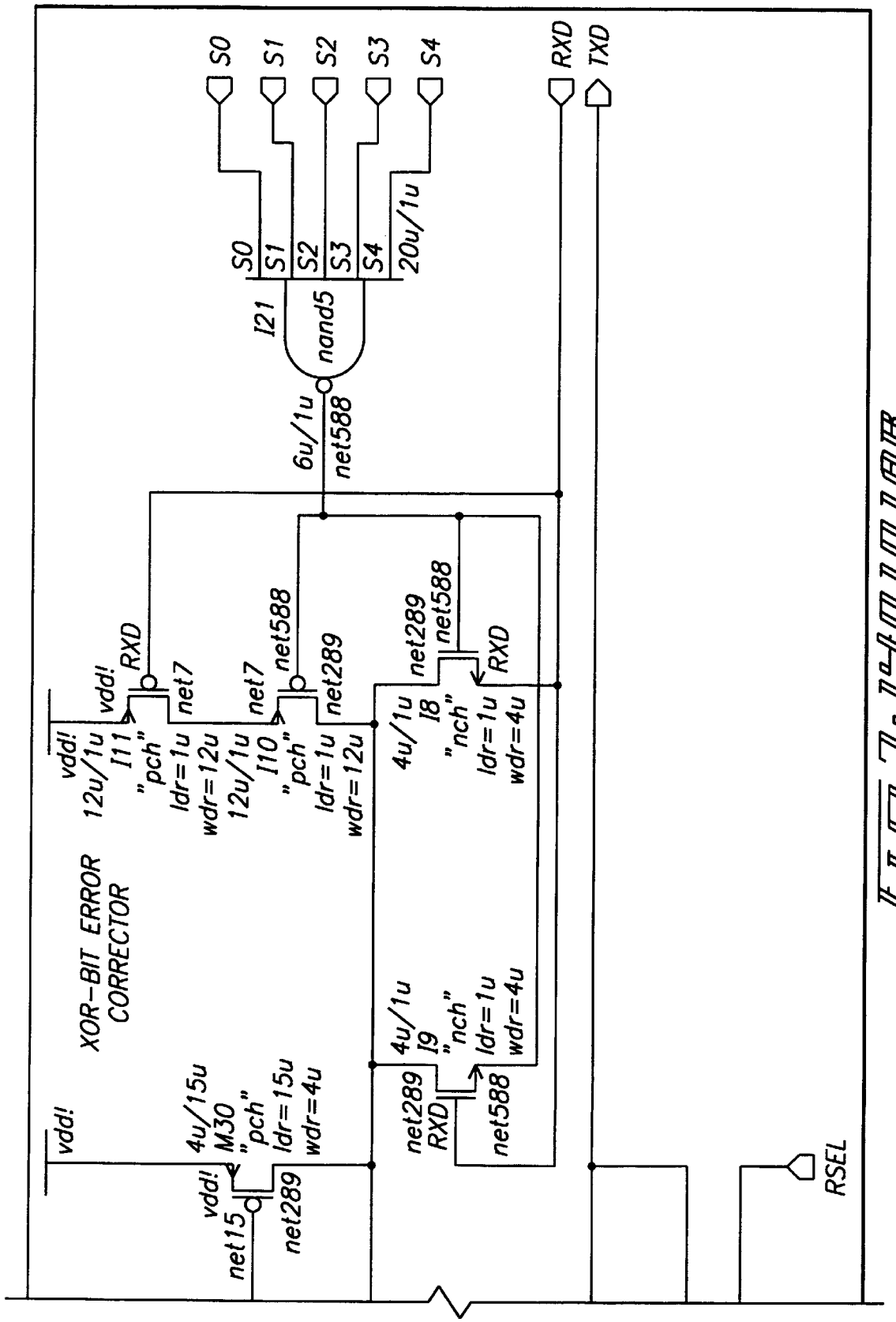

S0
S1
S2
S3
S4
RXD
TXD
S0
S1
S2
S3
S4
20u/1u
I21
nand5
6u/1u
net588
XOR-BIT ERROR CORRECTOR
vdd!
12u/1u
I11
"pch"
ldr=1u
wdr=12u
RXD
net7
12u/1u
I10
"pch"
ldr=1u
wdr=12u
net588
net289
4u/1u
I8
"nch"
ldr=1u
wdr=4u
net289
net588
RXD
4u/15u
M30
"pch"
ldr=15u
wdr=4u
vdd!
net15
net289
4u/1u
I9
"nch"
ldr=1u
wdr=4u
net289
RXD
net588
RSEL

Fig. 1,477,188

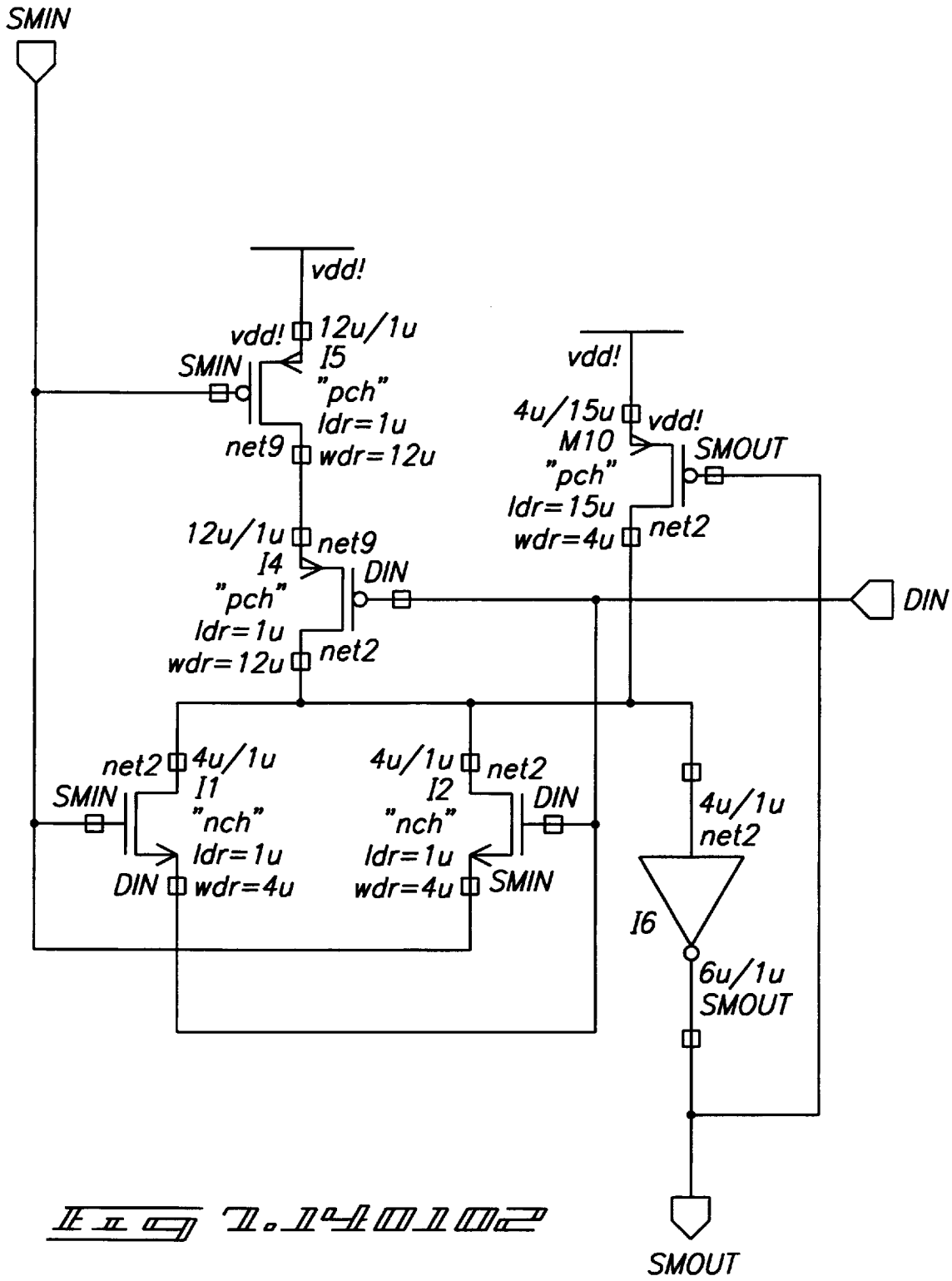
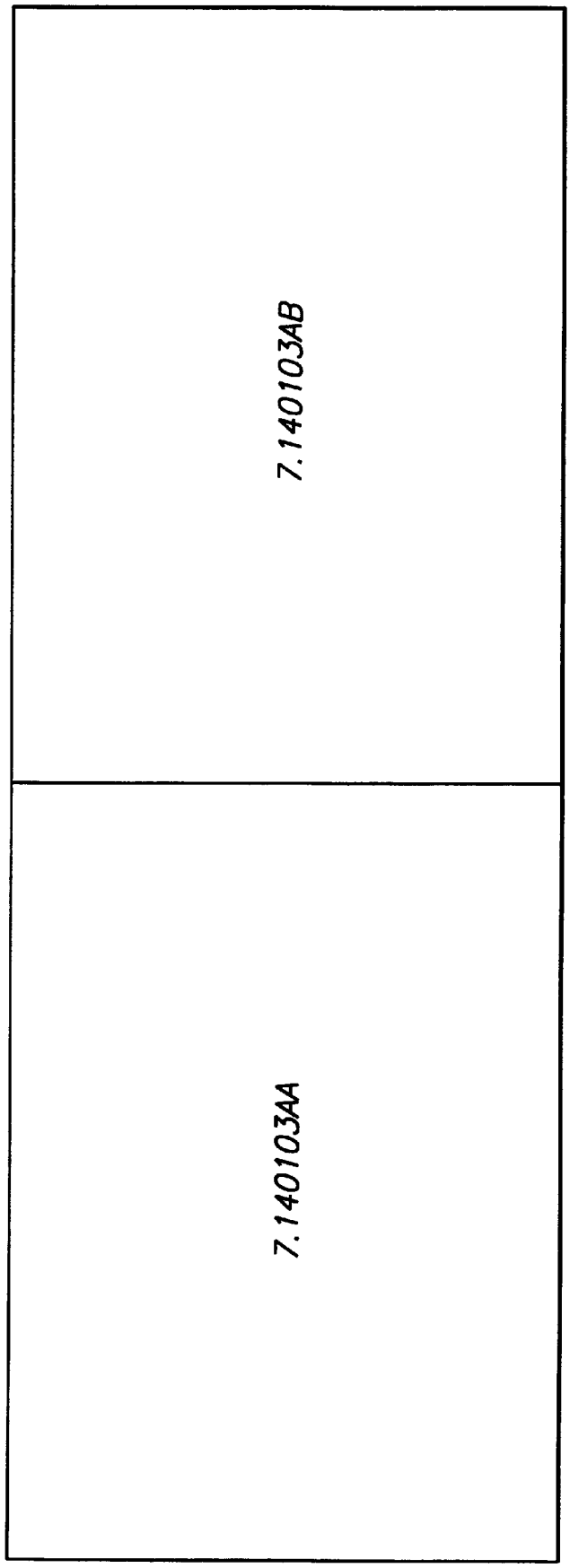

SMIN
vdd!
vdd!
12u/1u
I5
"pch"
ldr=1u
wdr=12u
SMIN
net9
vdd!
4u/15u
M10
"pch"
ldr=15u
wdr=4u
vdd!
SMOUT
net2
12u/1u
net9
I4
"pch"
ldr=1u
wdr=12u
DIN
net2
DIN
net2
4u/1u
I1
"nch"
ldr=1u
wdr=4u
SMIN
DIN
4u/1u
net2
I2
"nch"
ldr=1u
wdr=4u
DIN
SMIN
4u/1u
net2
I6
6u/1u
SMOUT
SMOUT

Fig 1.140102


7.140103AB
7.140103AA
FIG. 7.140103

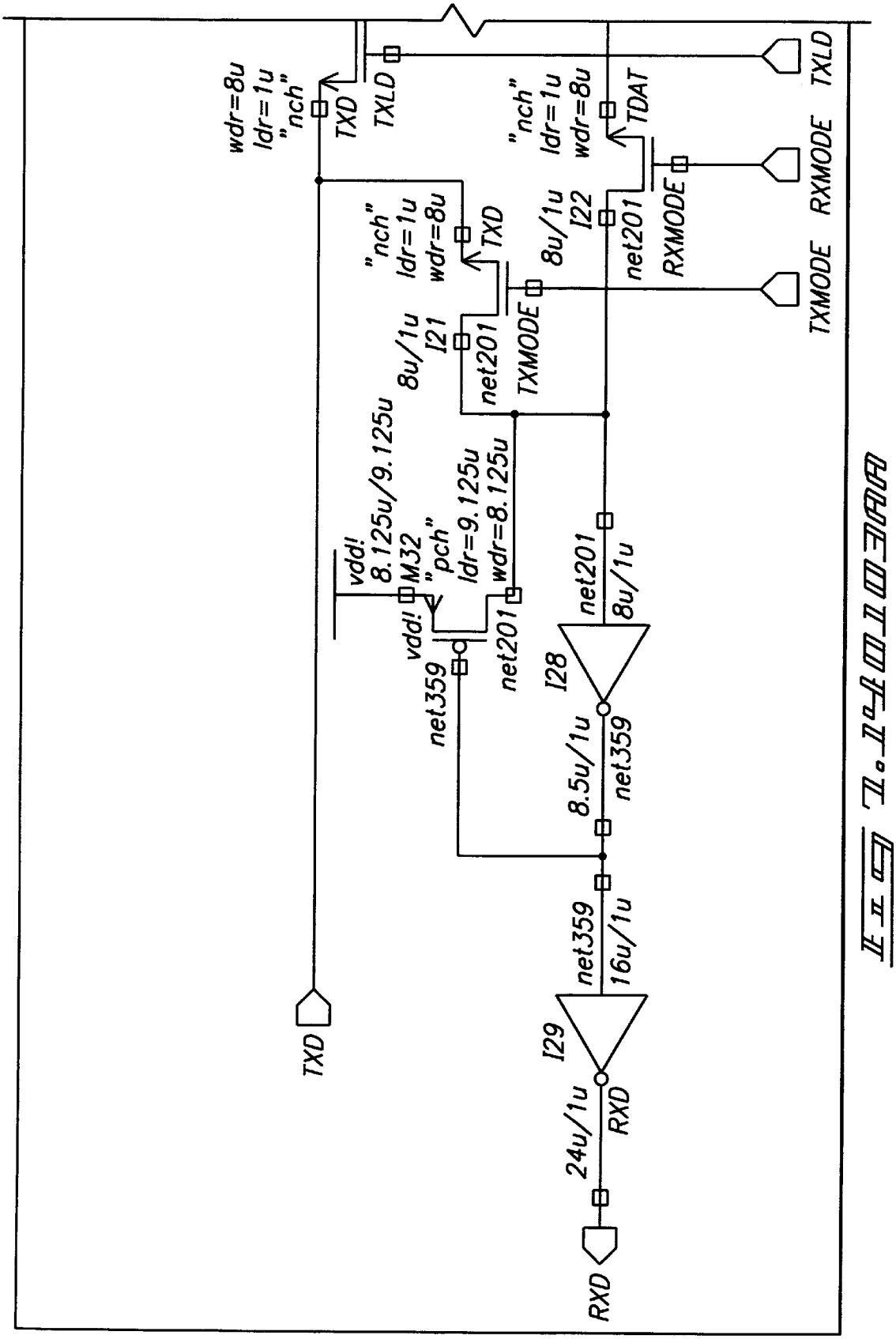

wdr=8u
ldr=1u
"nch"
TXD
TXLD
"nch"
ldr=1u
wdr=8u
TDAT
TXLD
RXMODE
TXMODE
net201
I22
8u/1u
"nch"
ldr=1u
wdr=8u
TXD
I21
8u/1u
net201
TXMODE
8.125u/9.125u
vdd!
M32
"pch"
ldr=9.125u
wdr=8.125u
net201
8u/1u
I28
net359
8.5u/1u
net359
net359
16u/1u
I29
24u/1u
RXD
TXD
RXD

FIG. 980

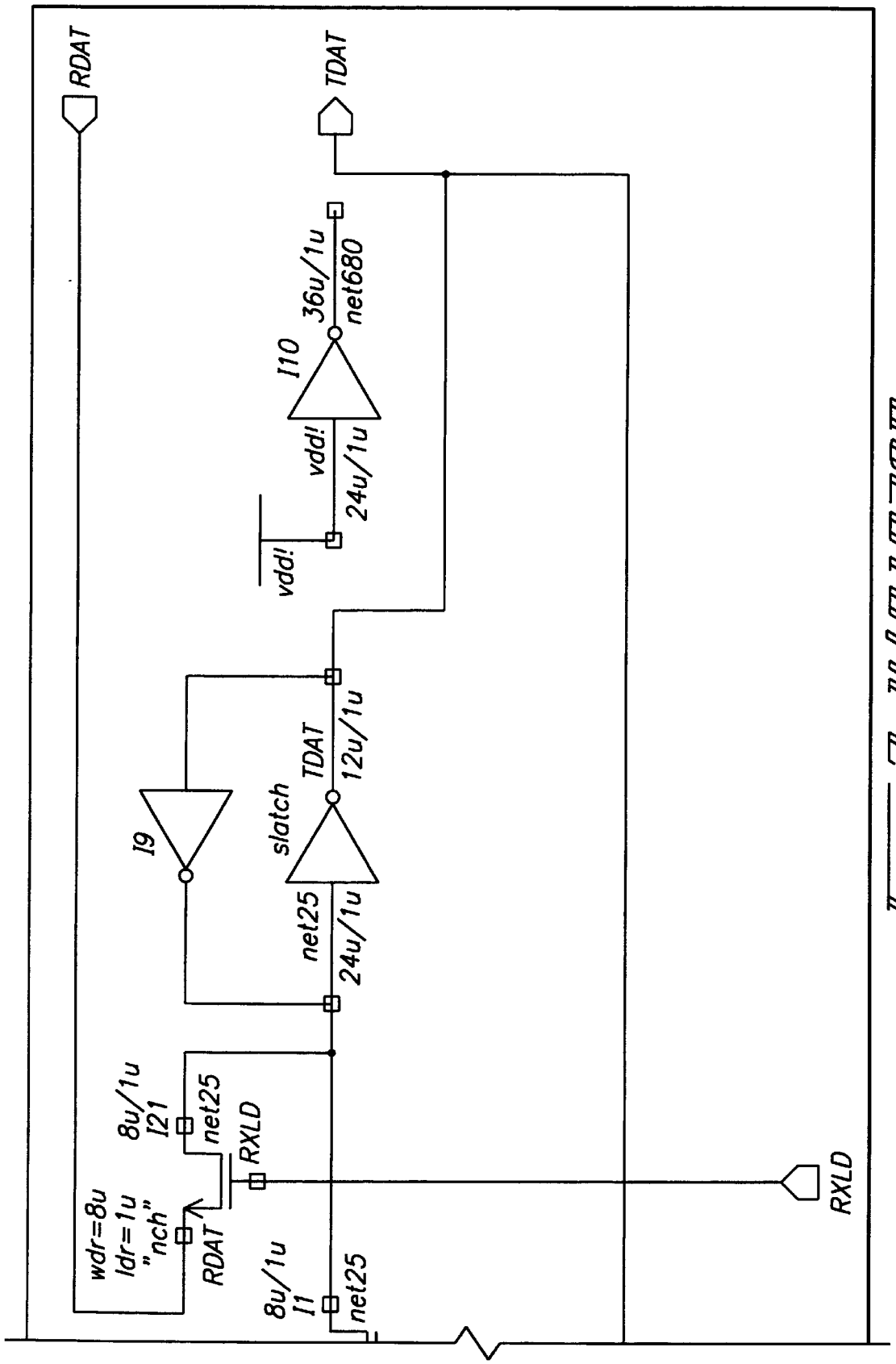

RDAT
TDAT
I10
36u/1u
net680
vdd!
24u/1u
vdd!
I9
slatch
TDAT
12u/1u
net25
24u/1u
8u/1u
I21
net25
RXLD
wdr=8u
ldr=1u
"nch"
RDAT
8u/1u
I1
net25
RXLD

FIG. 11

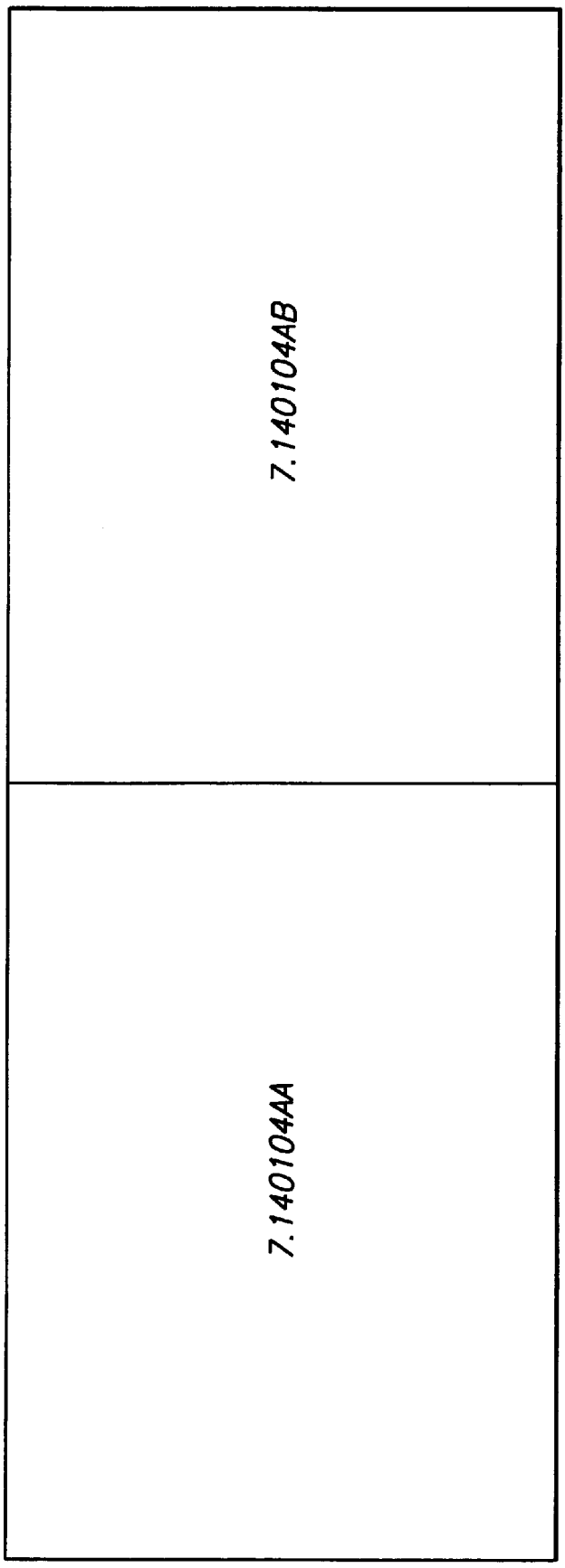


FIG. 7.140104

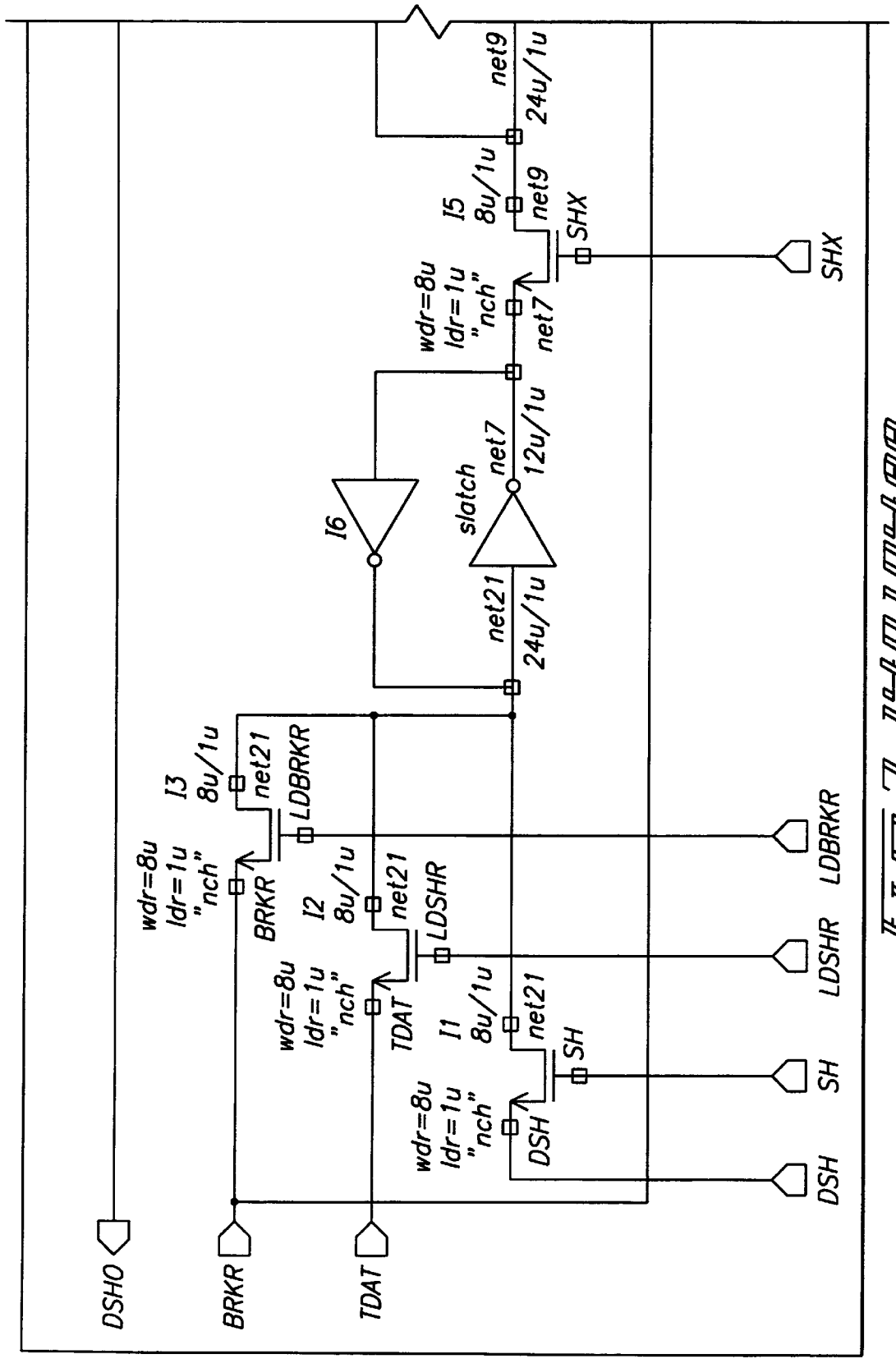

DSHO
BRKR
TDAT
DSH
SH
LDSHR
LDBRKR
SHX
net9
24u/1u
I5
8u/1u
net9
SHX
wdr=8u
ldr=1u
"nch"
net7
I6
slatch
net7
12u/1u
net21
24u/1u
I3
8u/1u
net21
LDBRKR
wdr=8u
ldr=1u
"nch"
BRKR
I2
8u/1u
net21
LDSHR
wdr=8u
ldr=1u
"nch"
TDAT
I1
8u/1u
net21
SH
wdr=8u
ldr=1u
"nch"
DSH

FIG. 1.983

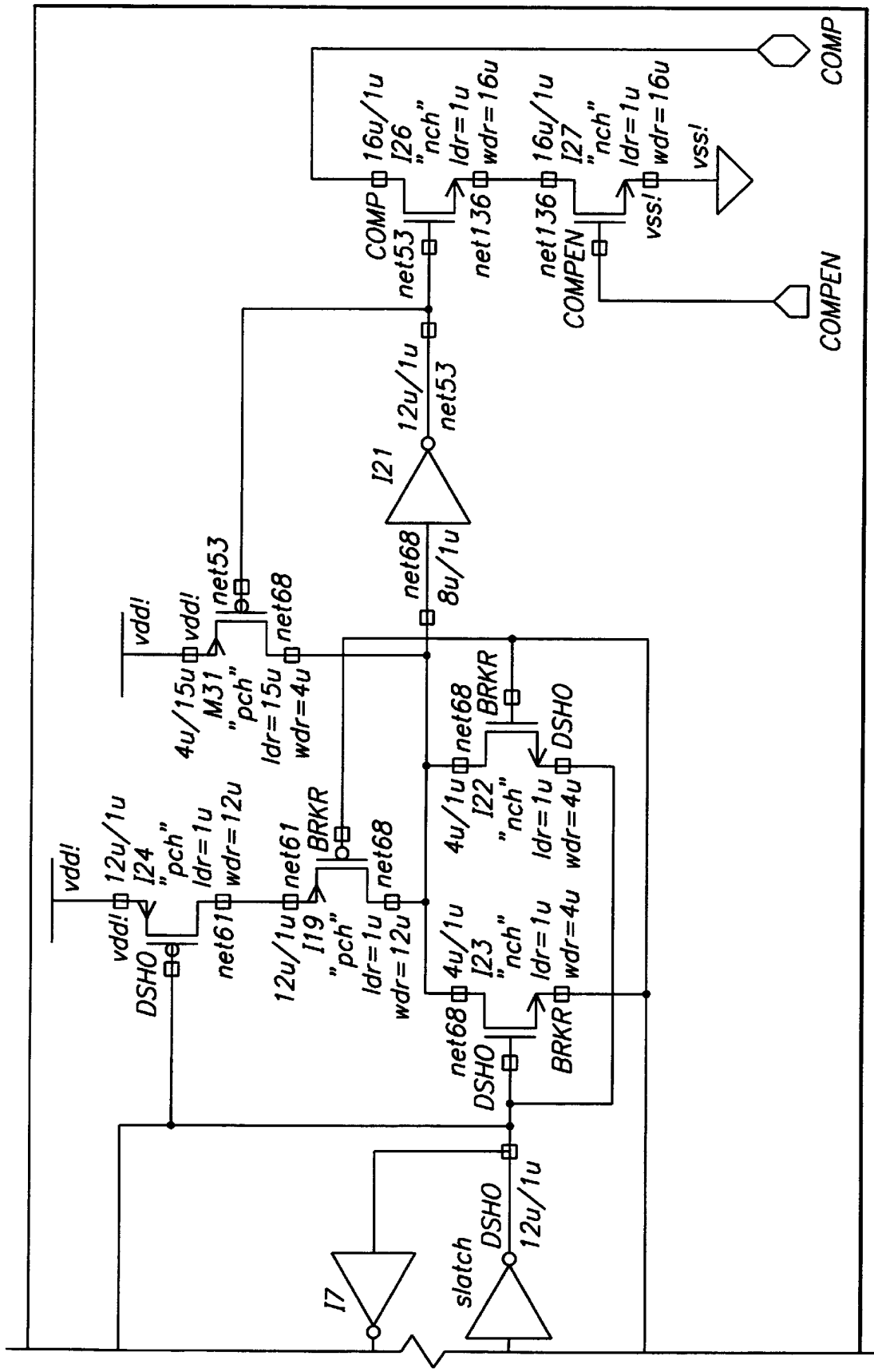

COMP
COMPEN
vss!
vdd!
DSHO
BRKR
net53
net68
net61
net136
net1136
I7
I19
I21
I22
I23
I24
I26
I27
M31
slatch
16u/1u
12u/1u
8u/1u
4u/1u
4u/15u
"pch"
"nch"
ldr=1u
ldr=15u
wdr=4u
wdr=12u
wdr=16u

FIG. 984

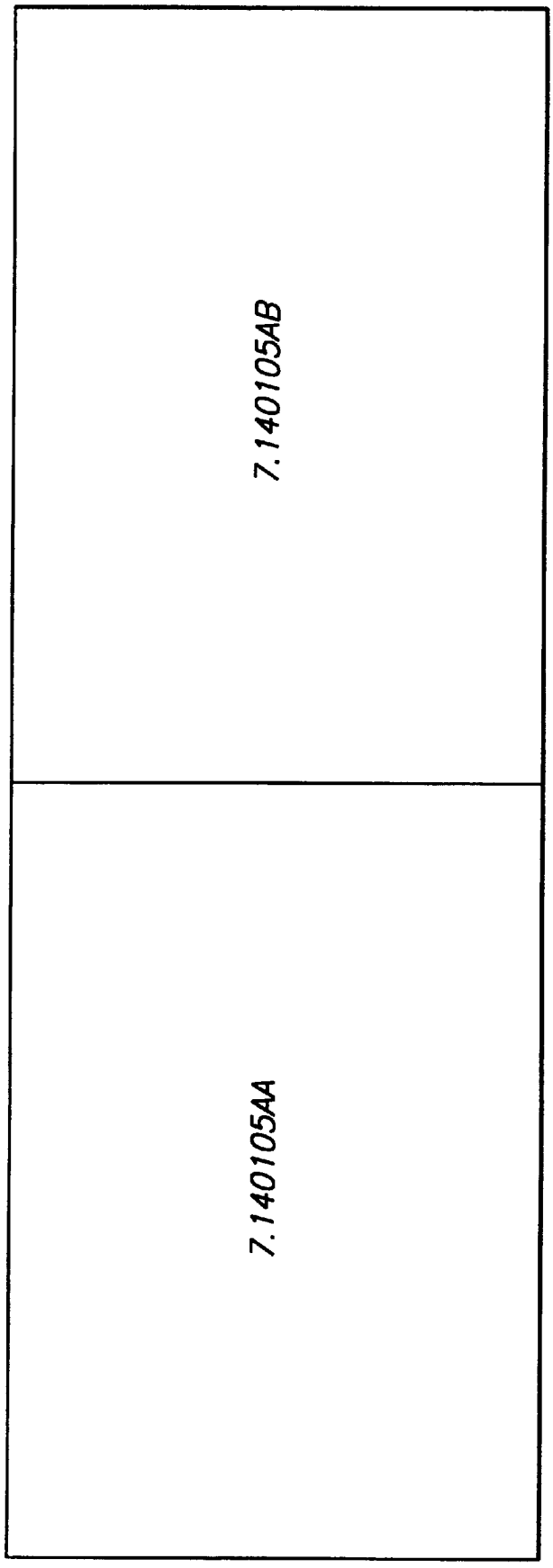


FIG. 7.140105

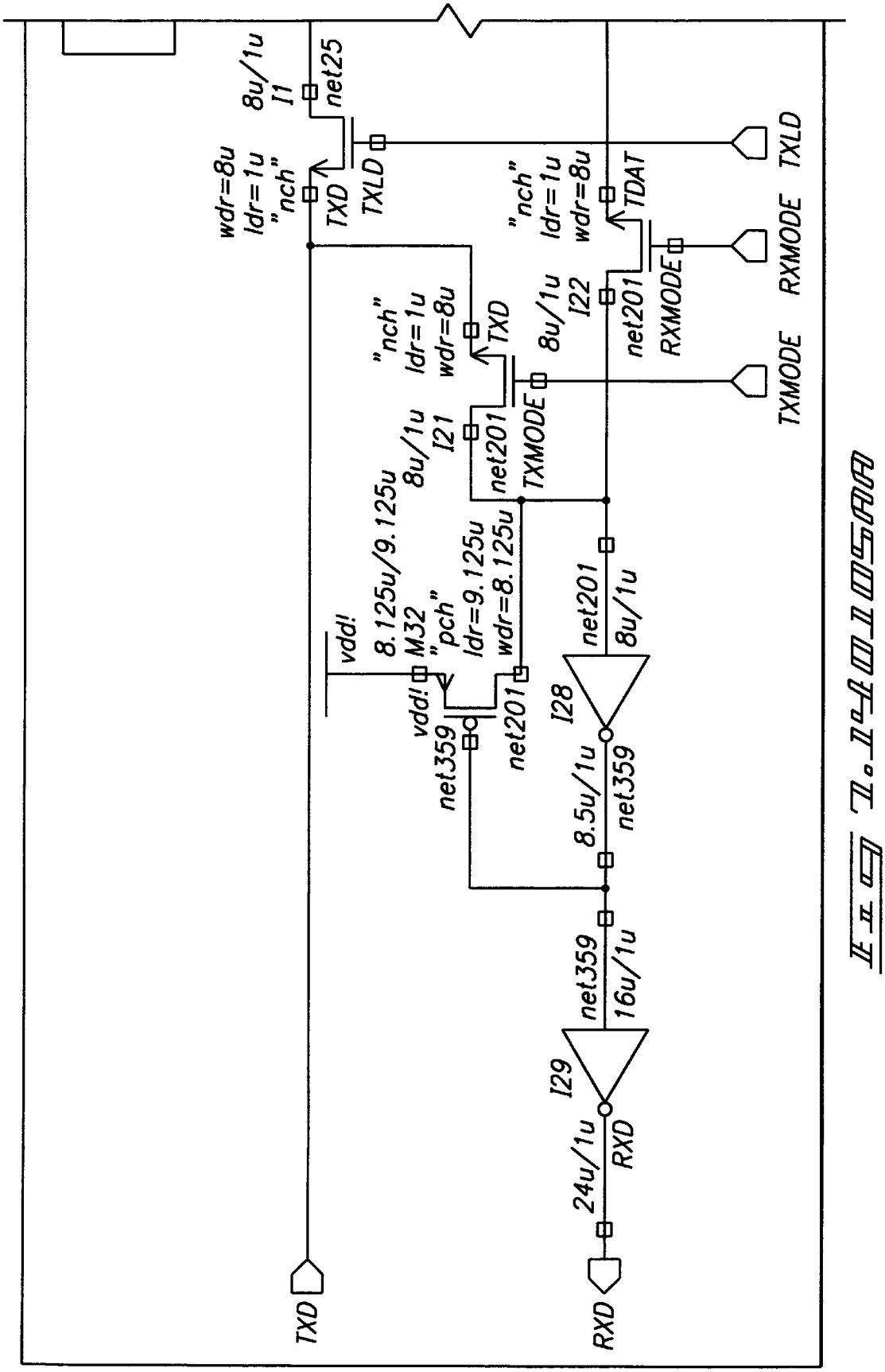

8u/1u
I1
net25
wdr=8u
ldr=1u
"nch"
TXD
TXLD
TXLD
"nch"
ldr=1u
wdr=8u
TDAT
RXMODE
TXD
"nch"
ldr=1u
wdr=8u
8u/1u
I22
net201
RXMODE
TXMODE
8u/1u
I21
net201
TXMODE
8.125u/9.125u
M32
"pch"
ldr=9.125u
wdr=8.125u
vdd!
vdd!
net359
net201
net201
8u/1u
I28
8.5u/1u
net359
net359
16u/1u
I29
24u/1u
RXD
TXD
RXD

FIG. 1,604,602

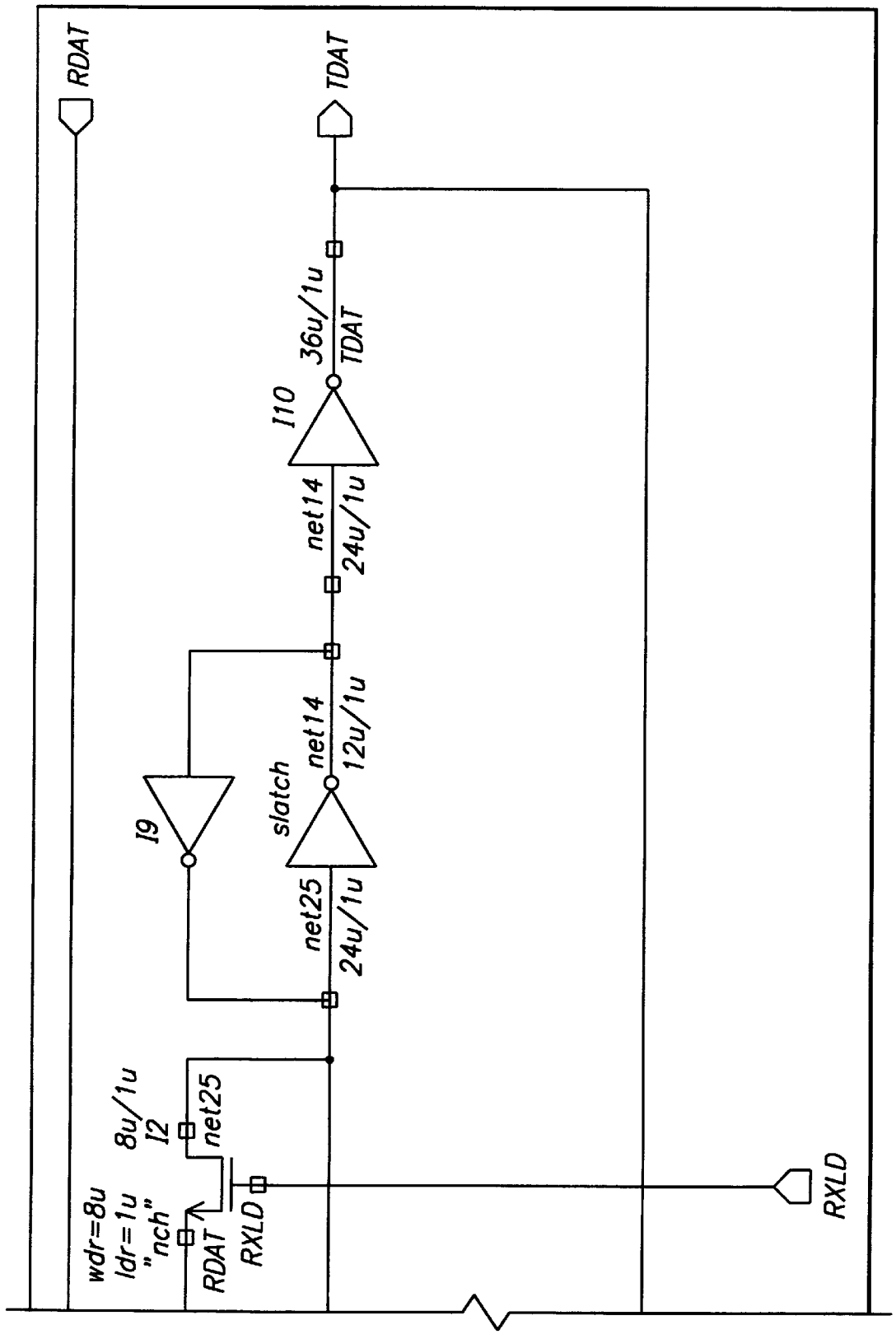

RDAT
TDAT
36u/1u
TDAT
I10
net14
24u/1u
net14
12u/1u
slatch
I9
net25
24u/1u
8u/1u
I2
net25
wdr=8u
ldr=1u
"nch"
RDAT
RXLD
RXLD

FIG. 11.

7.1402AC	7.1402AD	7.1402AE	7.1402AF	7.1402AG	7.1402AH	7.1402AI		
7.1402BA	7.1402BB	7.1402BC	7.1402BD	7.1402BE	7.1402BF	7.1402BG	7.1402BH	7.1402BI
7.1402CA	7.1402CB	7.1402CC	7.1402CD	7.1402CE	7.1402CF	7.1402CG	7.1402CH	7.1402CI
7.1402DA	7.1402DB	7.1402DC	7.1402DD	7.1402DE	7.1402DF	7.1402DG	7.1402DH	7.1402DI
7.1402EA	7.1402EB	7.1402EC	7.1402ED	7.1402EE	7.1402EF	7.1402EG	7.1402EH	7.1402EI

FIG. 7.1402

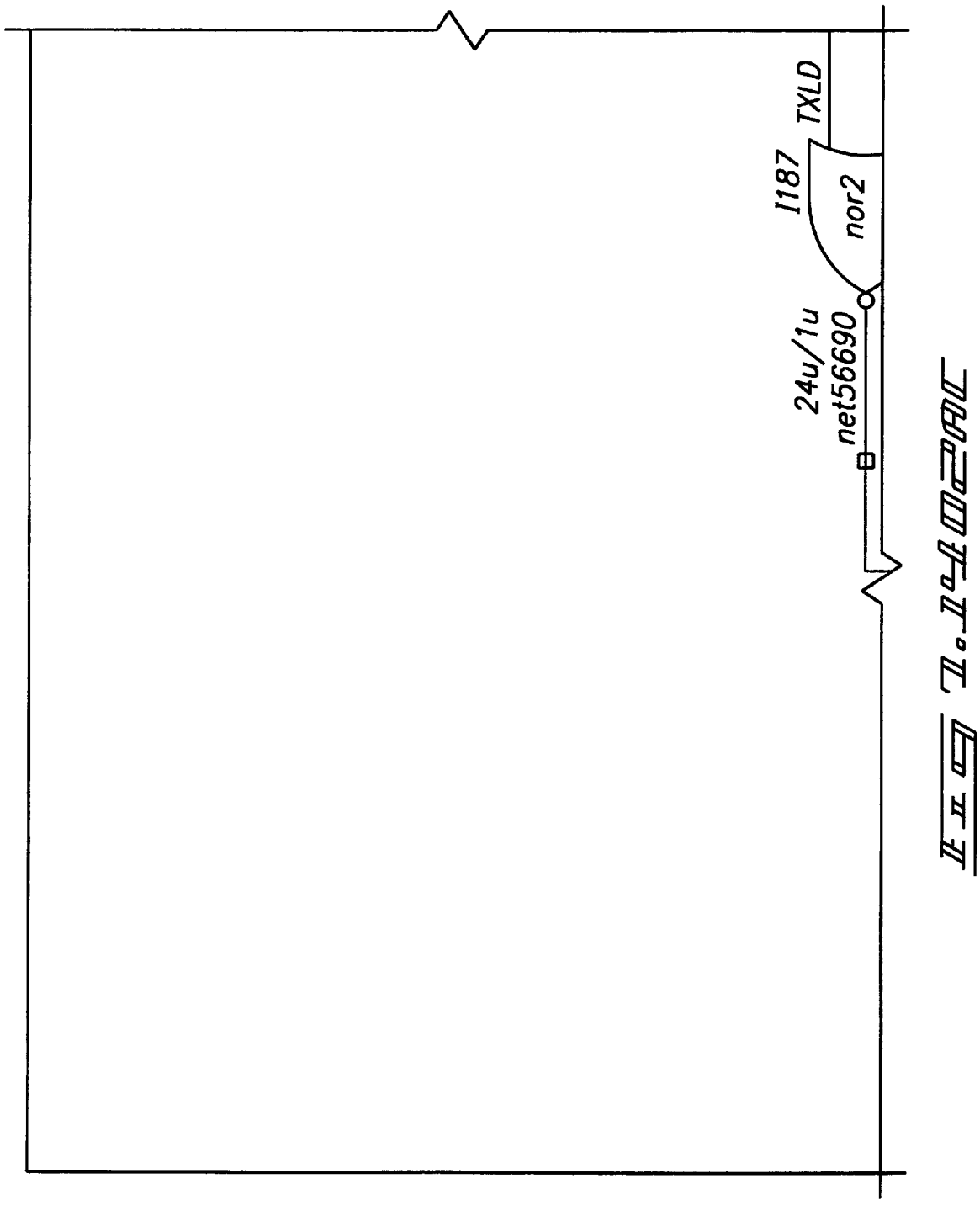
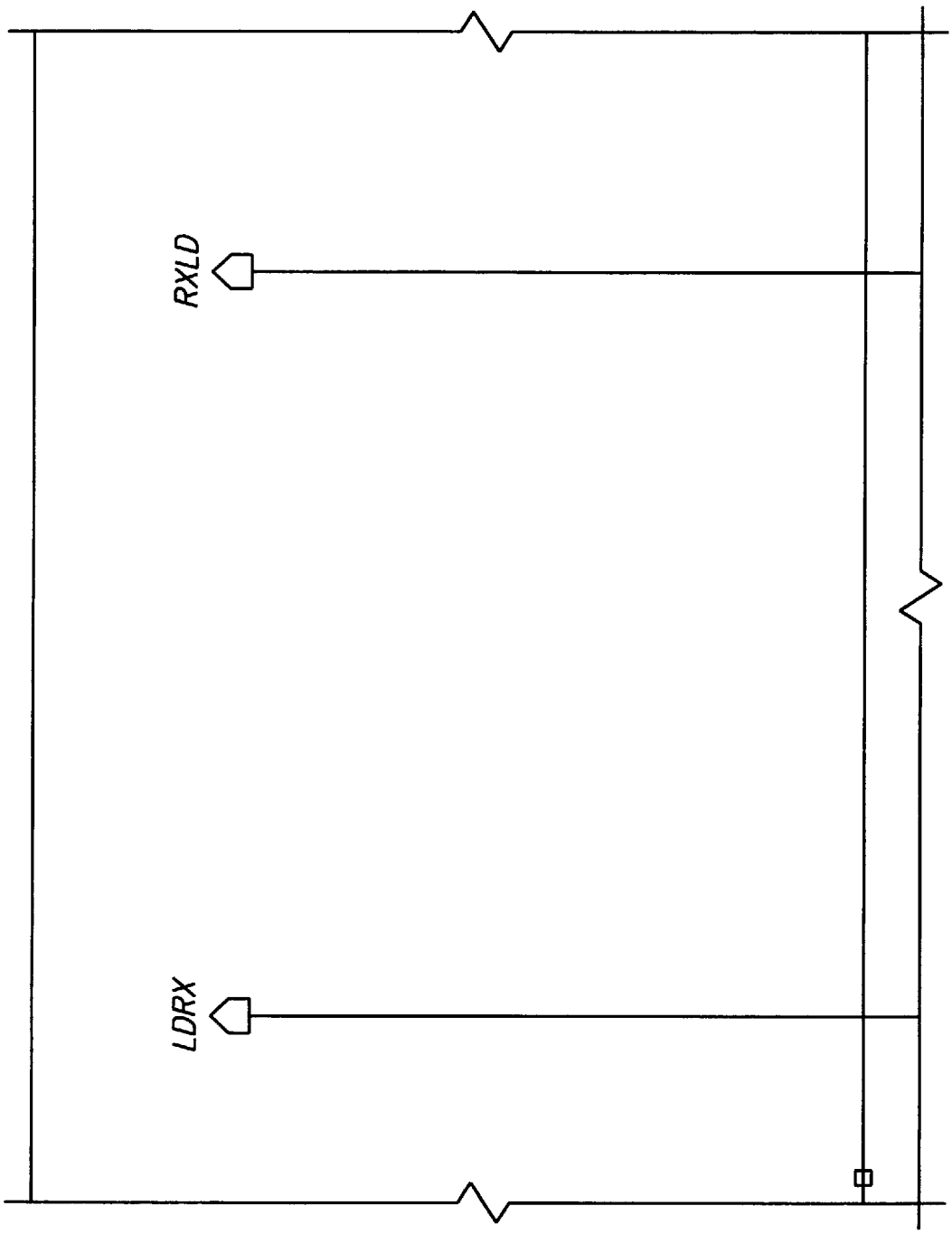


FIG. 1,605,744


RXLD
LDRX
FIG. 6AT.L

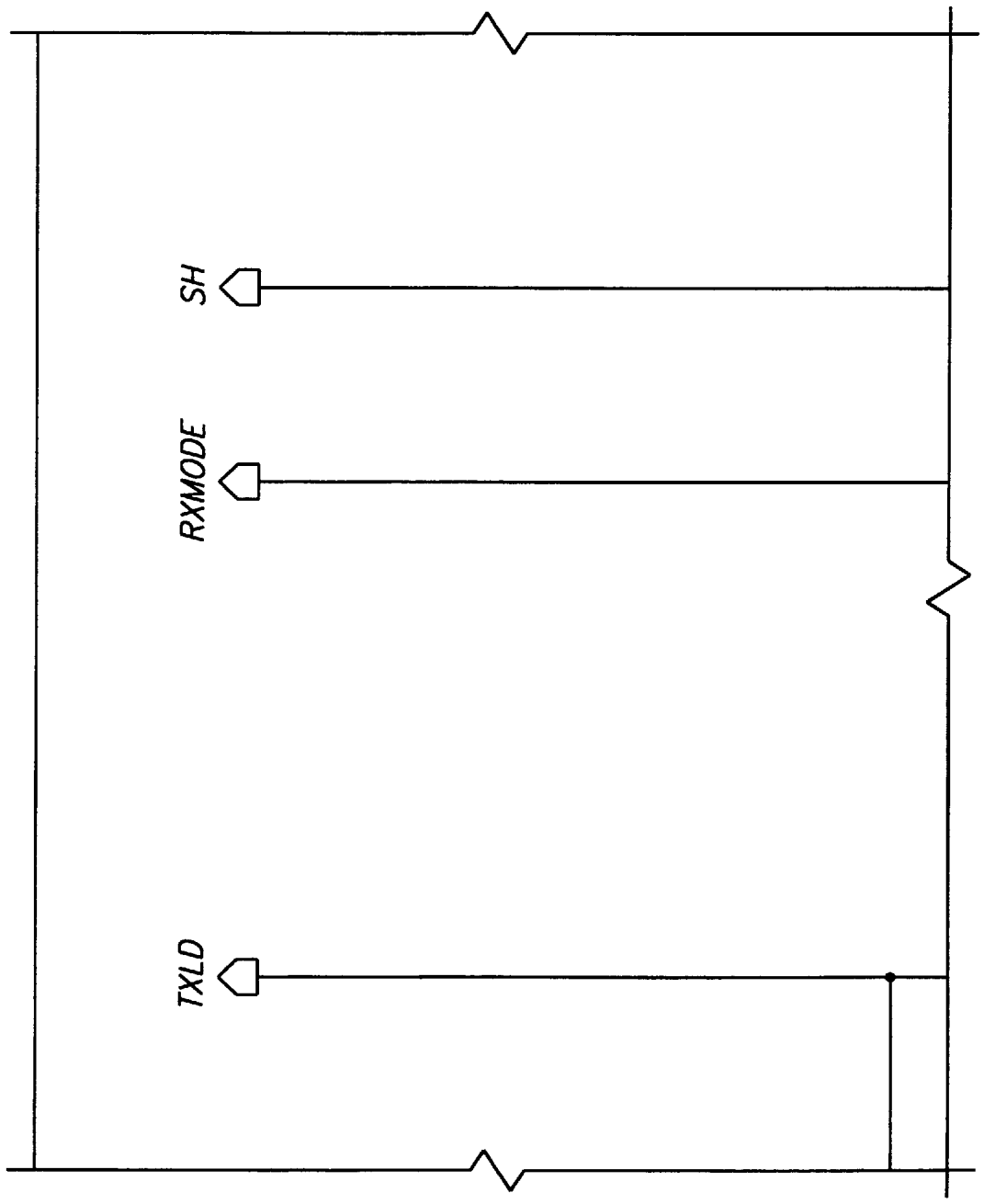


FIG 11.14D2AE

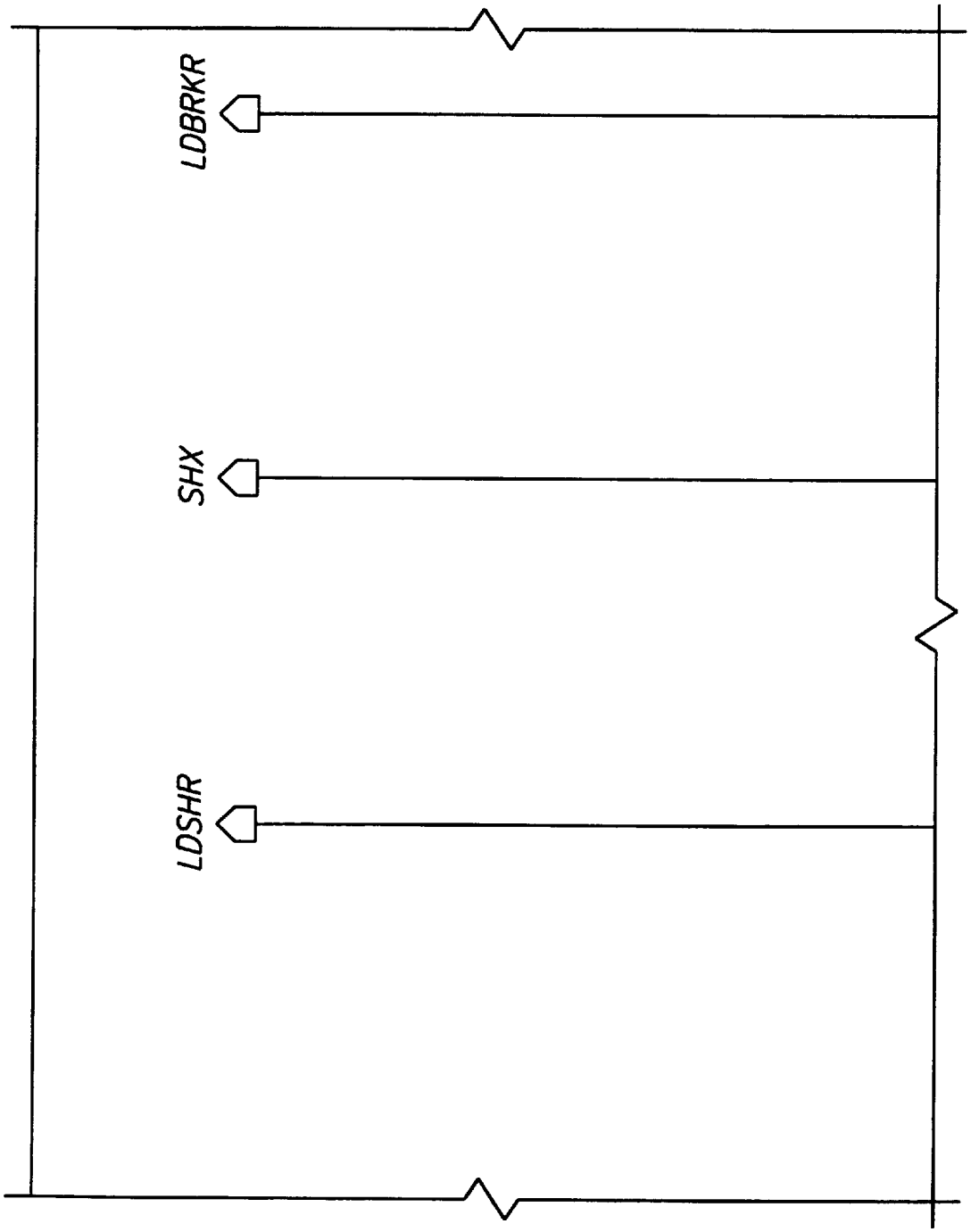


FIG 7.1407AF

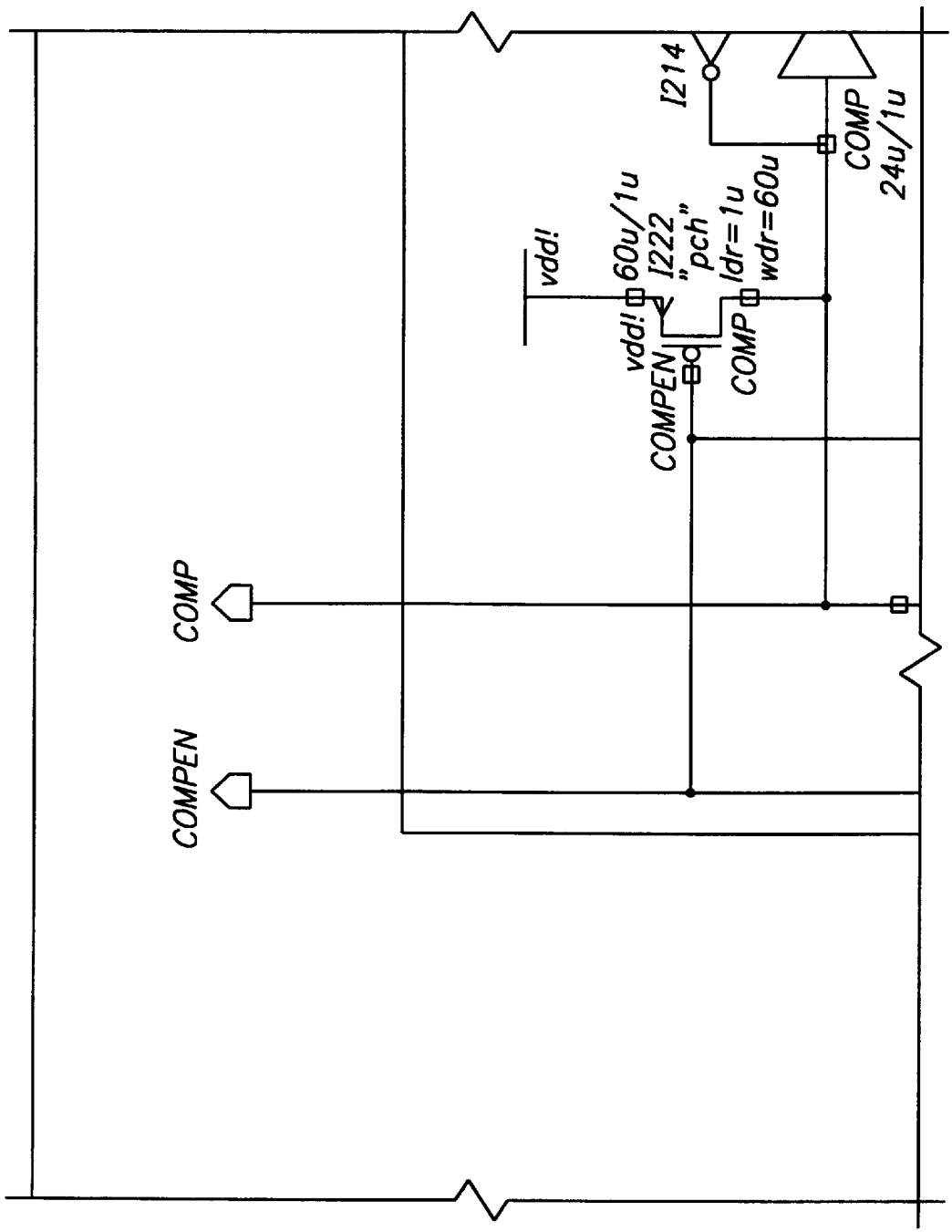

I214
COMP
24u/1u
vdd!
60u/1u
I222
"pch"
ldr=1u
wdr=60u
vdd!
COMPEN
COMP
COMP
COMPEN

FIG. 114

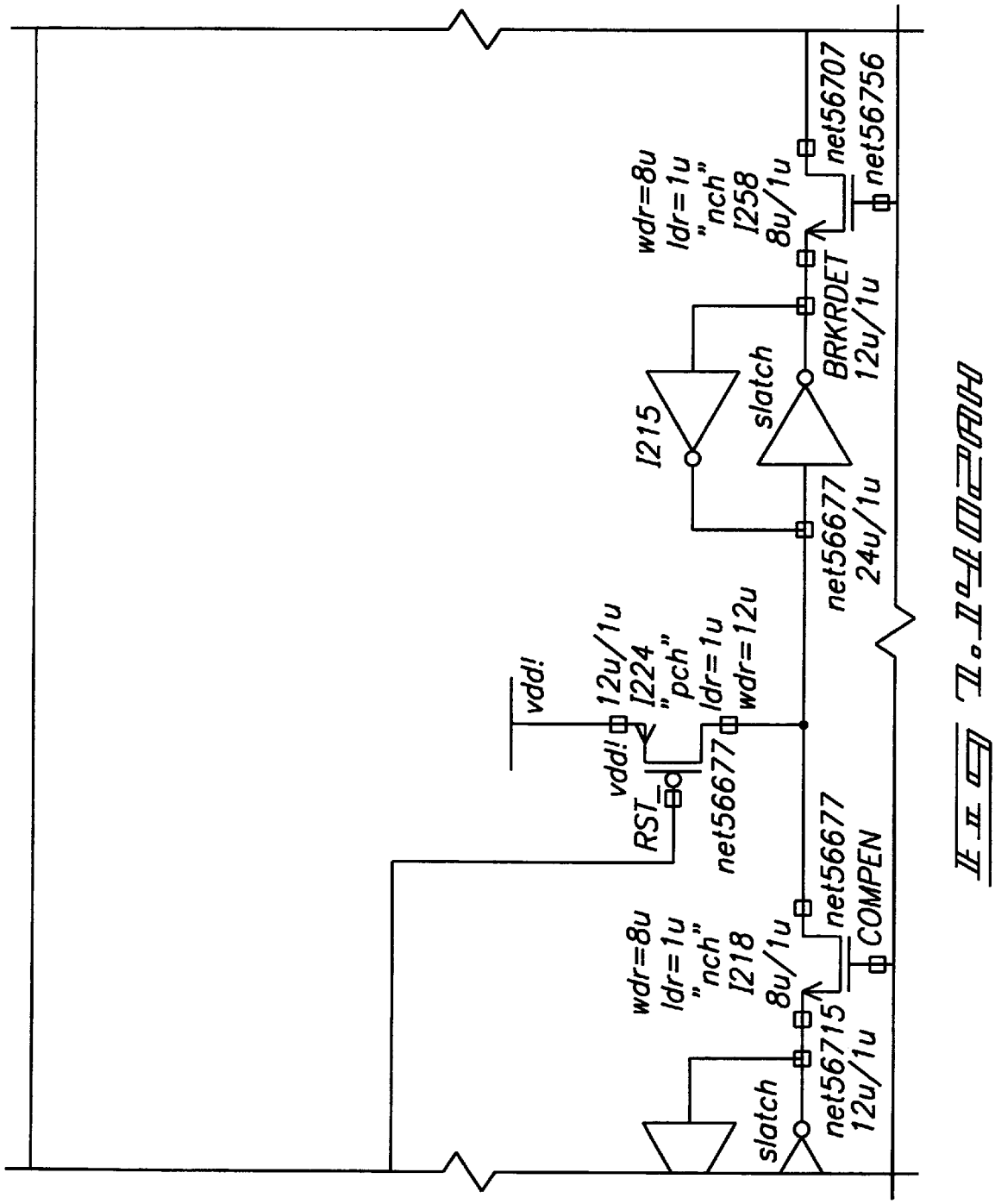

net56707
net56756
wdr=8u
ldr=1u
"nch"
I258
8u/1u
BRKRDET
12u/1u
slatch
I215
net56677
24u/1u
vdd!
12u/1u
I224
"pch"
ldr=1u
wdr=12u
vdd!
RST
net56677
net56677
COMPEN
wdr=8u
ldr=1u
"nch"
I218
8u/1u
net56715
12u/1u
slatch

FIG. 994

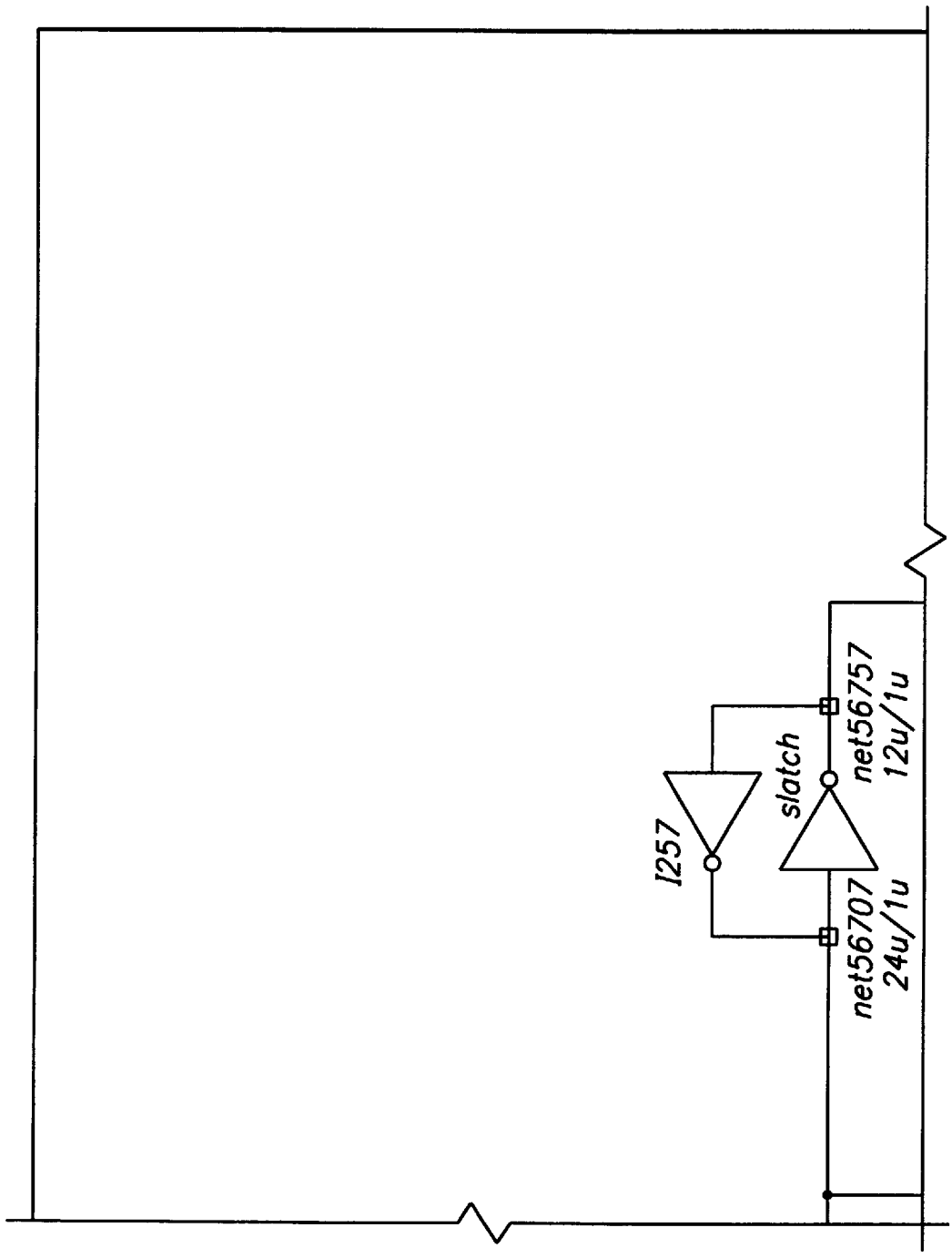
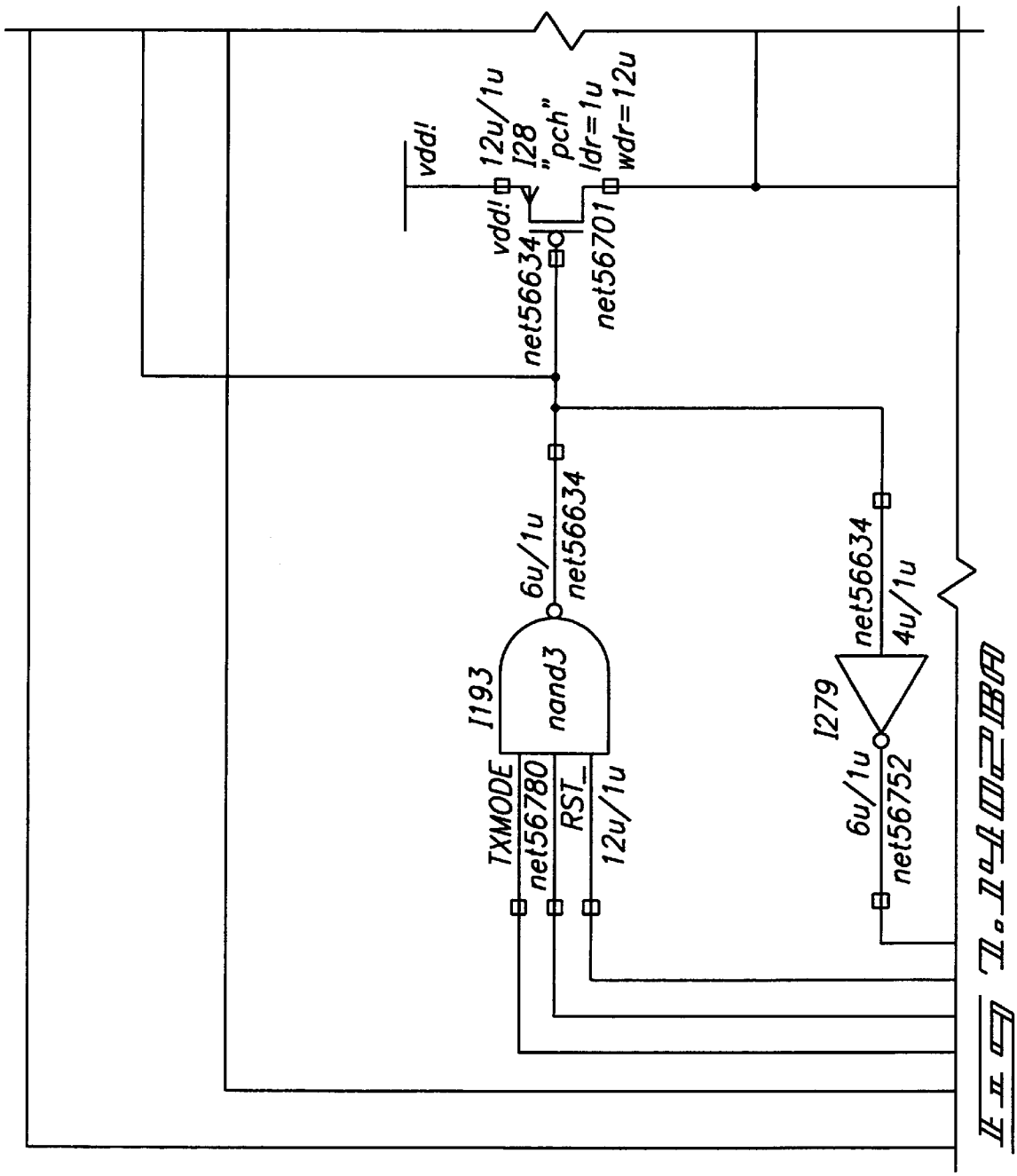
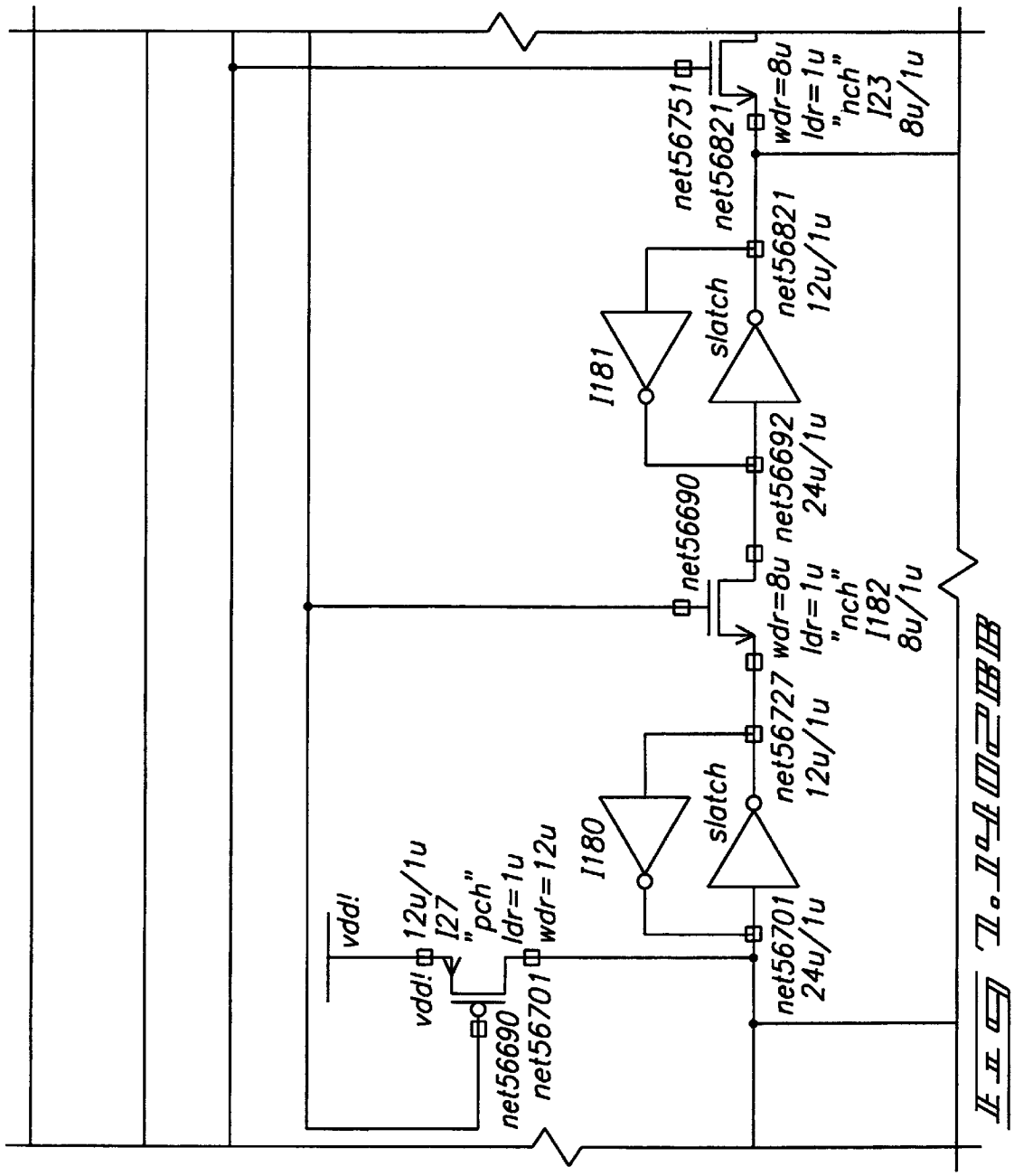


FIG. 1,004,011


vdd!
12u/1u
I28
"pch"
ldr=1u
wdr=12u
vdd!
net56634
net56701
6u/1u
net56634
I193
nand3
TXMODE
net56780
RST_
12u/1u
net56634
4u/1u
I279
6u/1u
net56752


net56751
net56821
wdr=8u
ldr=1u
"nch"
I23
8u/1u
net56821
12u/1u
slatch
I181
net56692
24u/1u
net56690
wdr=8u
ldr=1u
"nch"
I182
8u/1u
net56727
12u/1u
slatch
I180
net56701
24u/1u
vdd!
12u/1u
I27
"pch"
ldr=1u
wdr=12u
vdd!
net56690
net56701

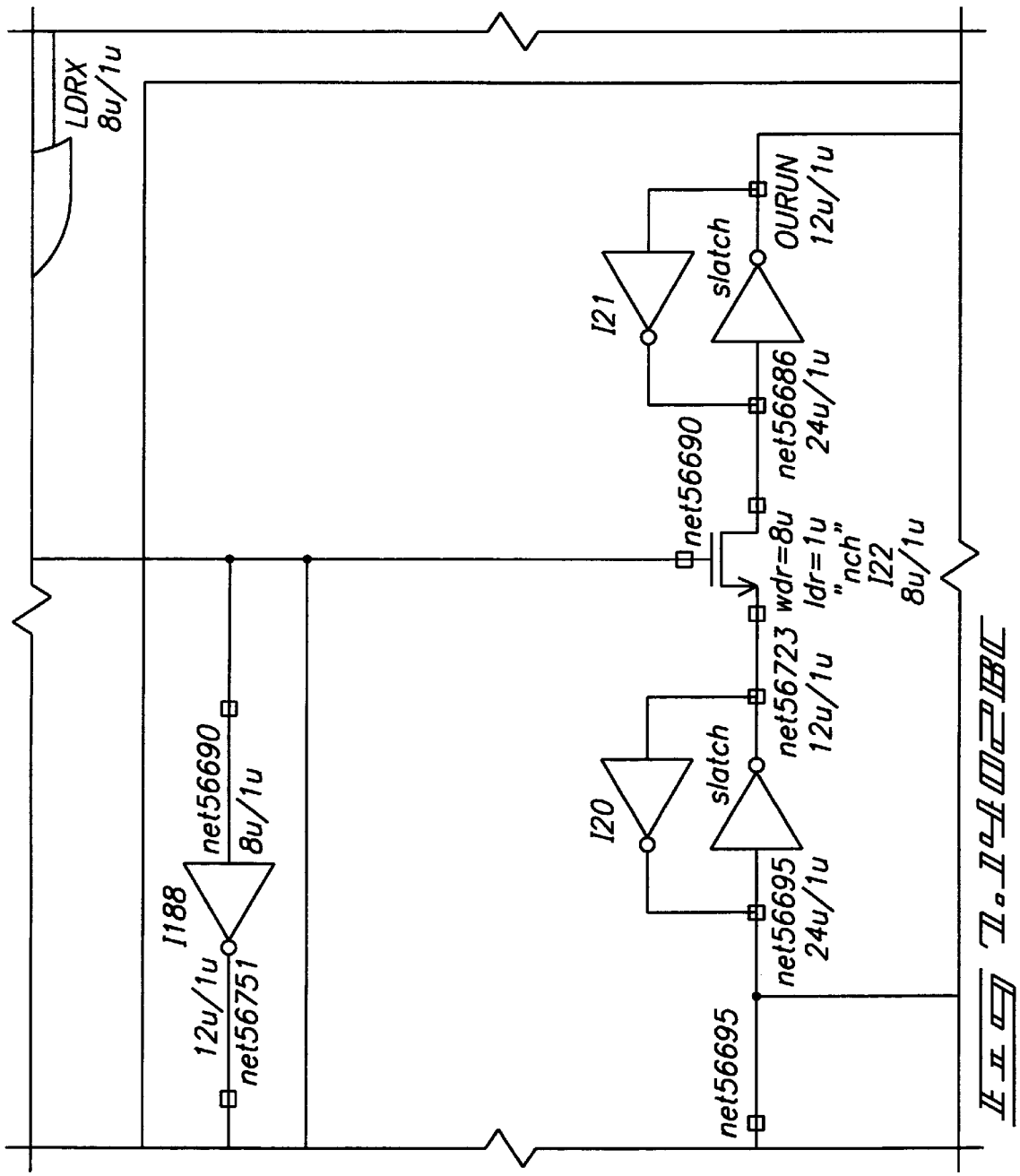

LDRX
8u/1u
I21
slatch
OURUN
12u/1u
net56686
24u/1u
net56690
wdr=8u
ldr=1u
"nch"
I22
8u/1u
net56723
12u/1u
I20
slatch
net56695
24u/1u
net56695
net56690
8u/1u
I188
12u/1u
net56751

FIG. 114

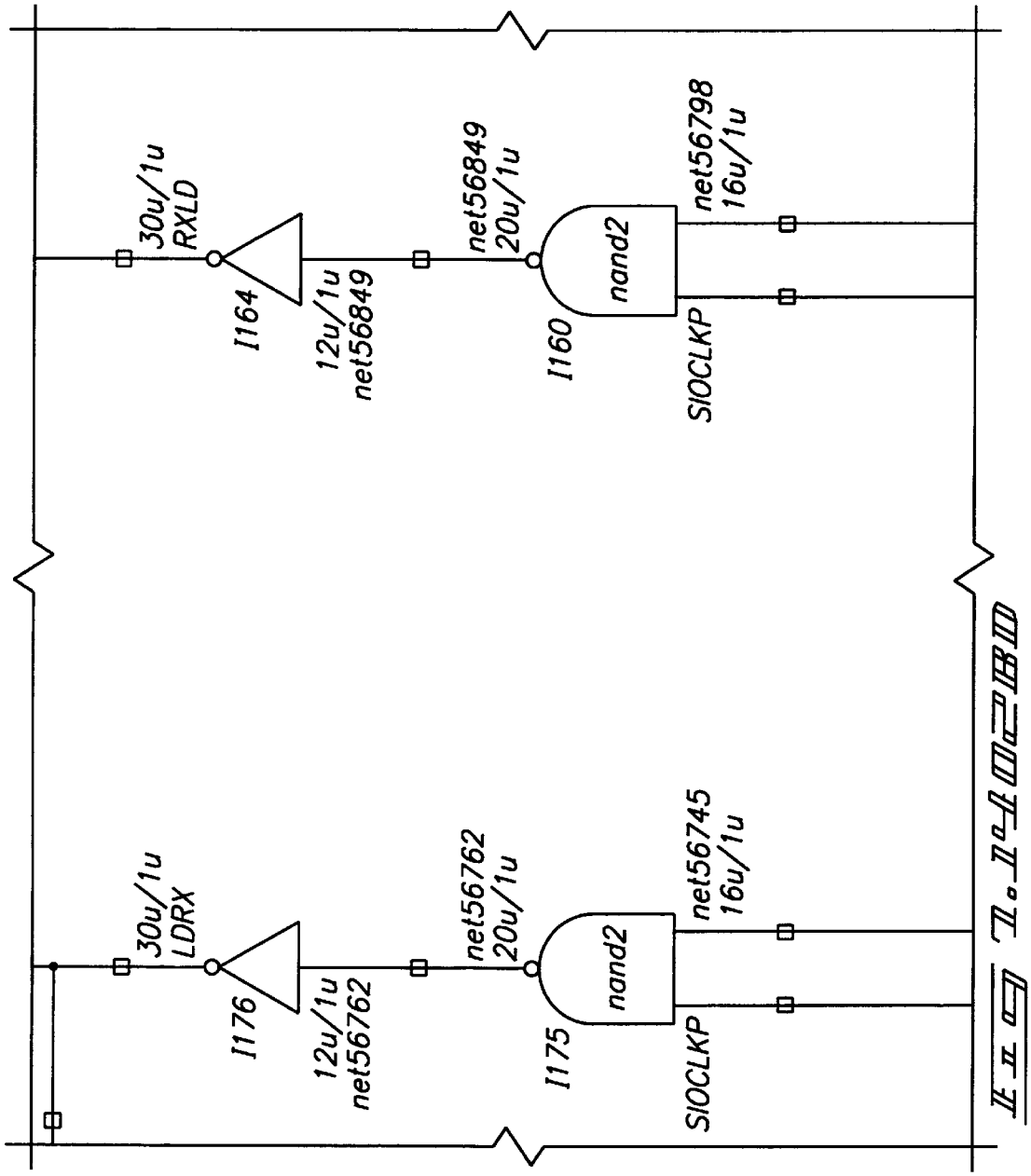

30u/1u
RXLD
I164
12u/1u
net56849
net56849
20u/1u
I160
nand2
net56798
16u/1u
SIOCLKP
30u/1u
LDRX
I176
12u/1u
net56762
net56762
20u/1u
I175
nand2
net56745
16u/1u
SIOCLKP

FIG. 1.4780

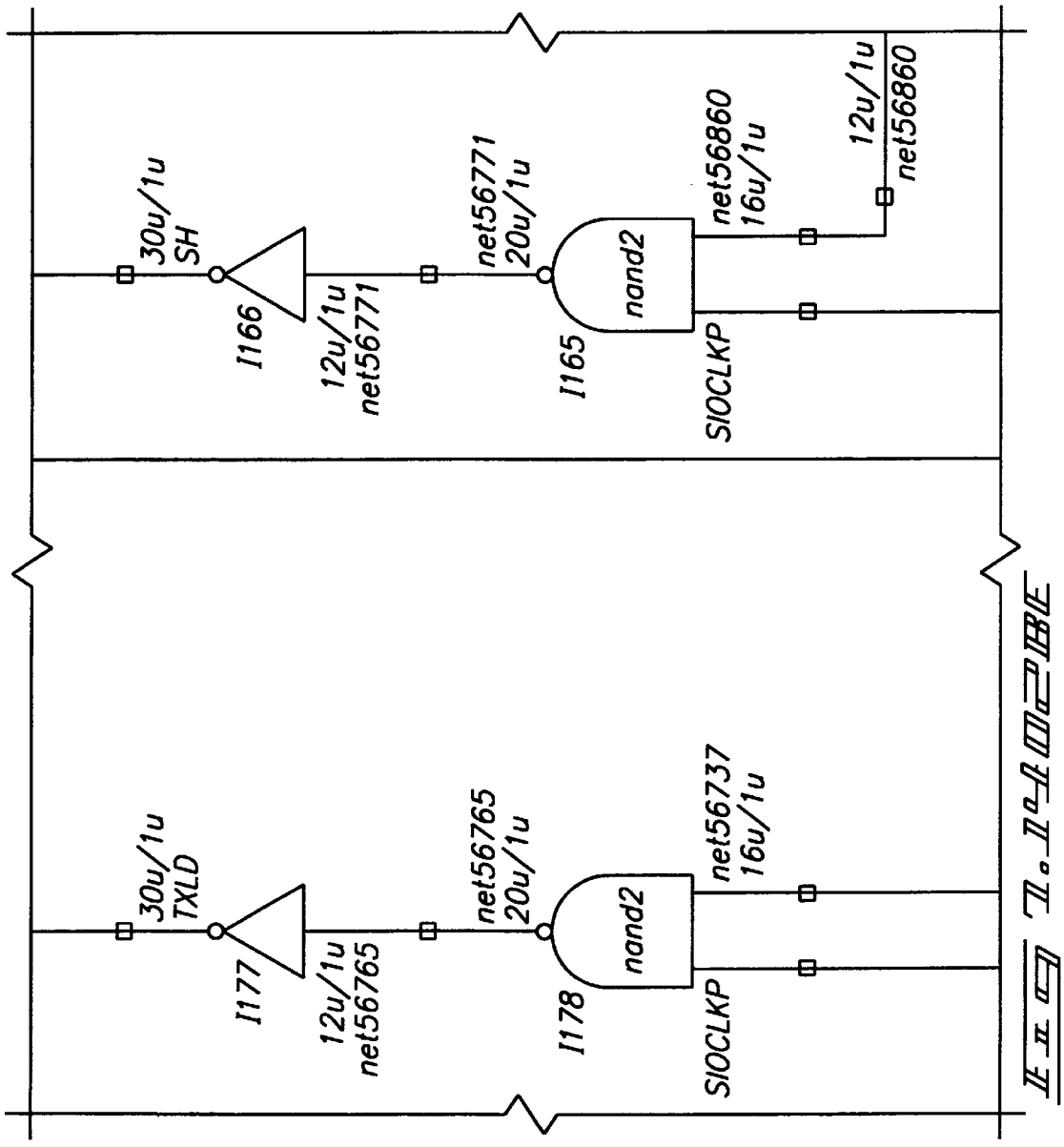
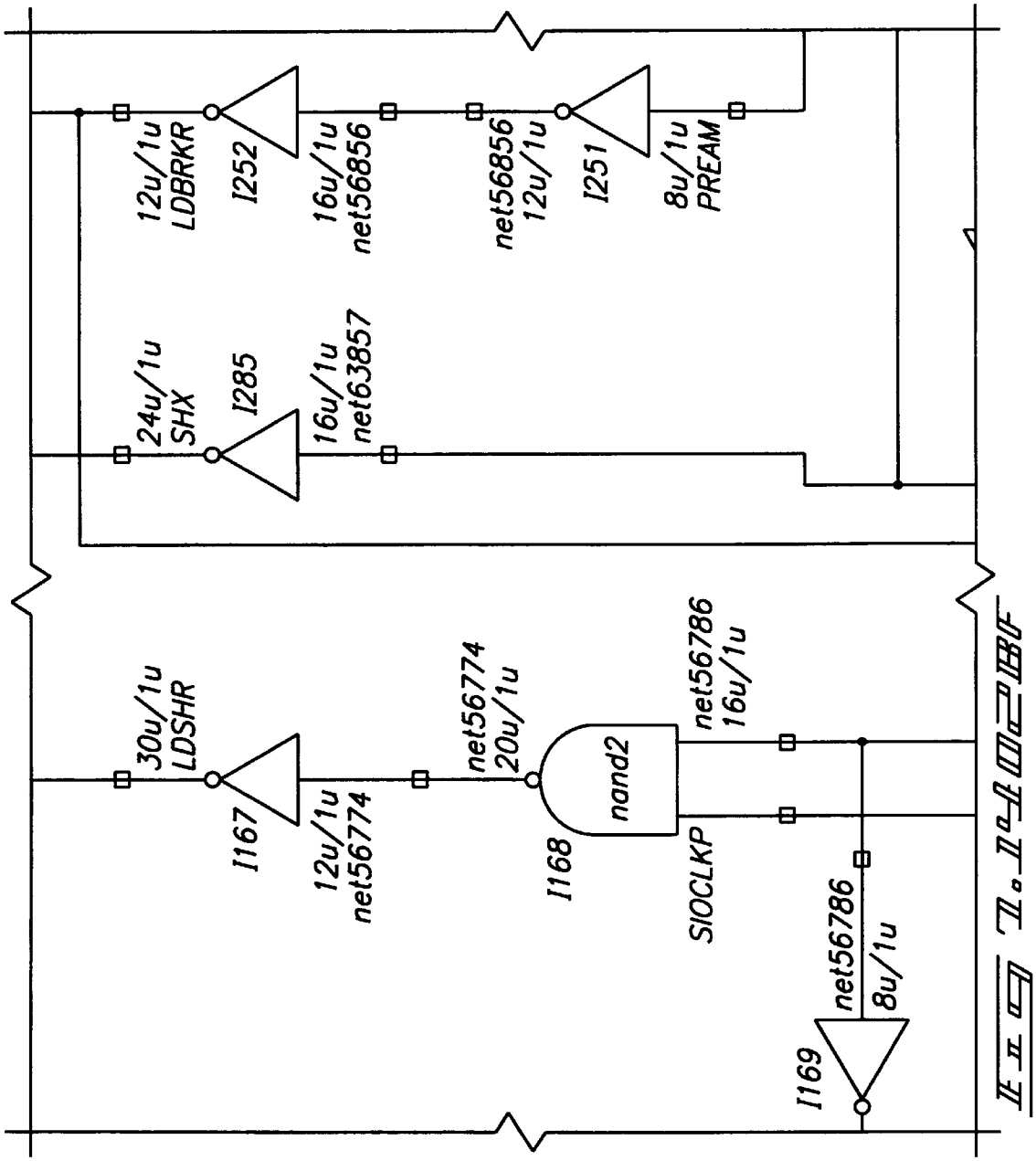

30u/1u
SH
I166
12u/1u
net56771
net56771
20u/1u
I165
nand2
net56860
16u/1u
12u/1u
net56860
SIOCLKP
30u/1u
TXLD
I177
12u/1u
net56765
net56765
20u/1u
I178
nand2
net56737
16u/1u
SIOCLKP

FIG. 114


12u/1u
LDBRKR
I252
16u/1u
net56856
net56856
12u/1u
I251
8u/1u
PREAM
24u/1u
SHX
I285
16u/1u
net63857
30u/1u
LDSHR
I167
12u/1u
net56774
net56774
20u/1u
nand2
I168
net56786
16u/1u
SIOCLKP
net56786
8u/1u
I169

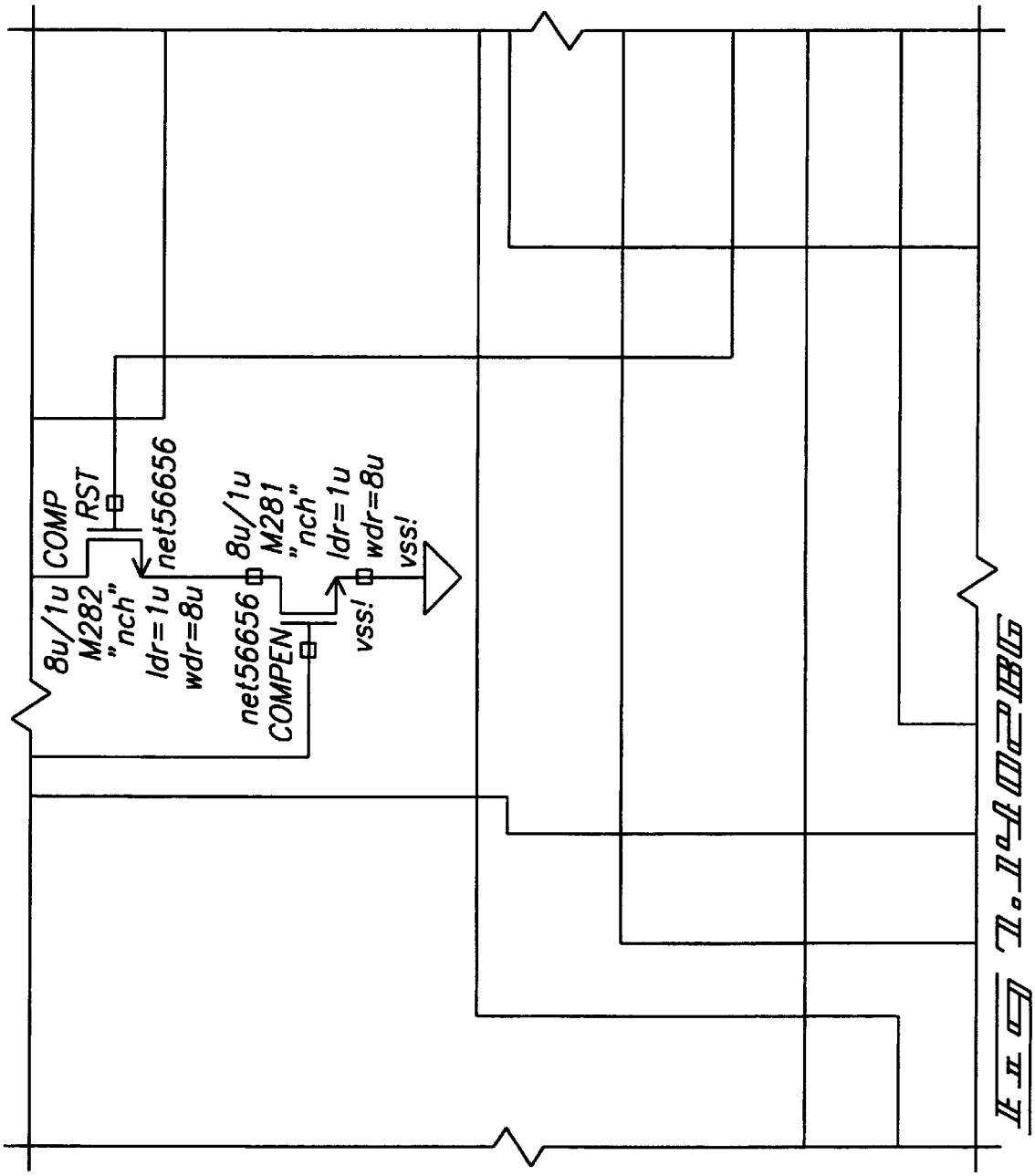

8u/1u
M282
"nch"
ldr=1u
wdr=8u
COMP
RST
net56656
net56656
COMPEN
8u/1u
M281
"nch"
ldr=1u
wdr=8u
vss!
vss!

FIG. 1.1402B

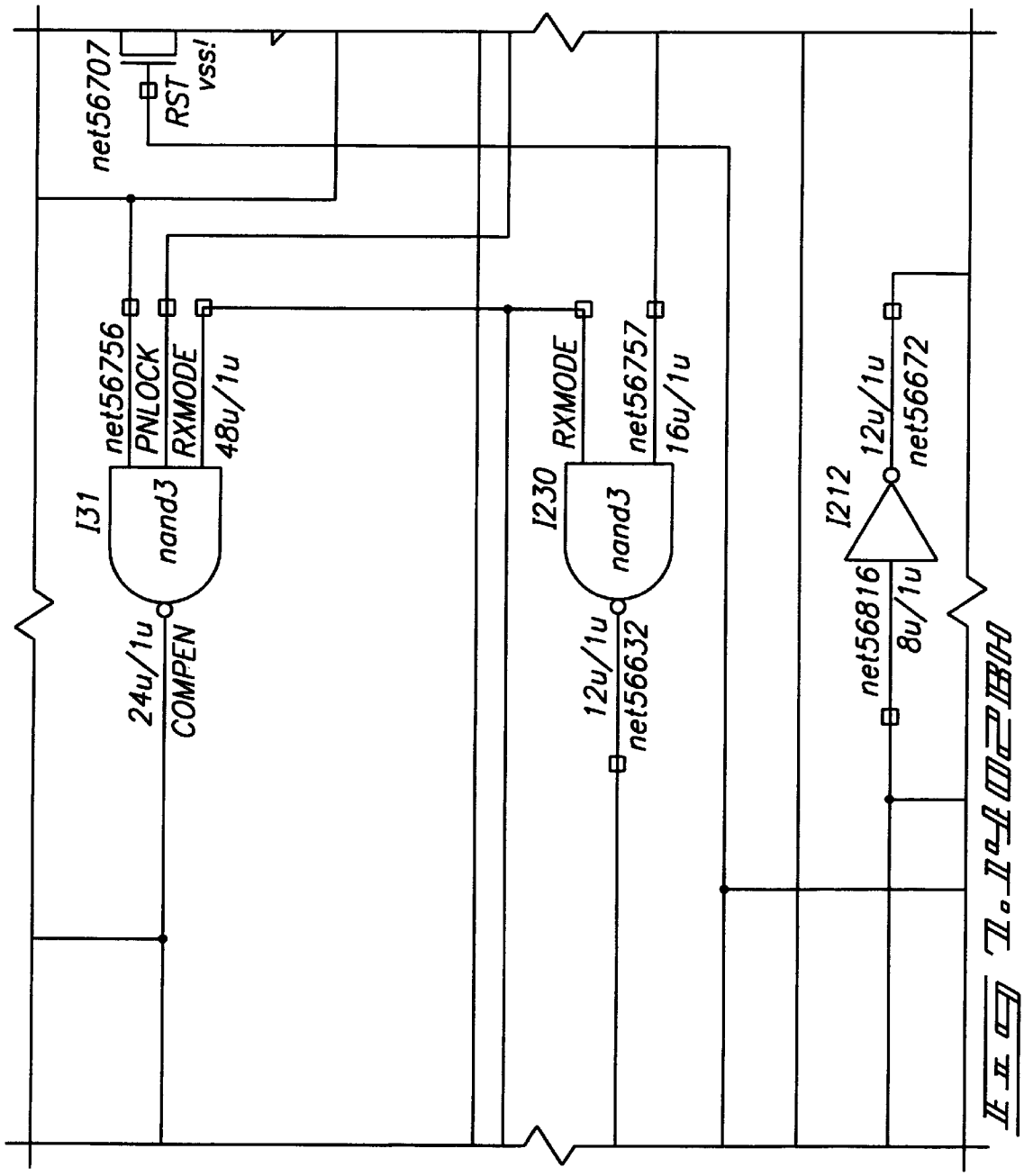
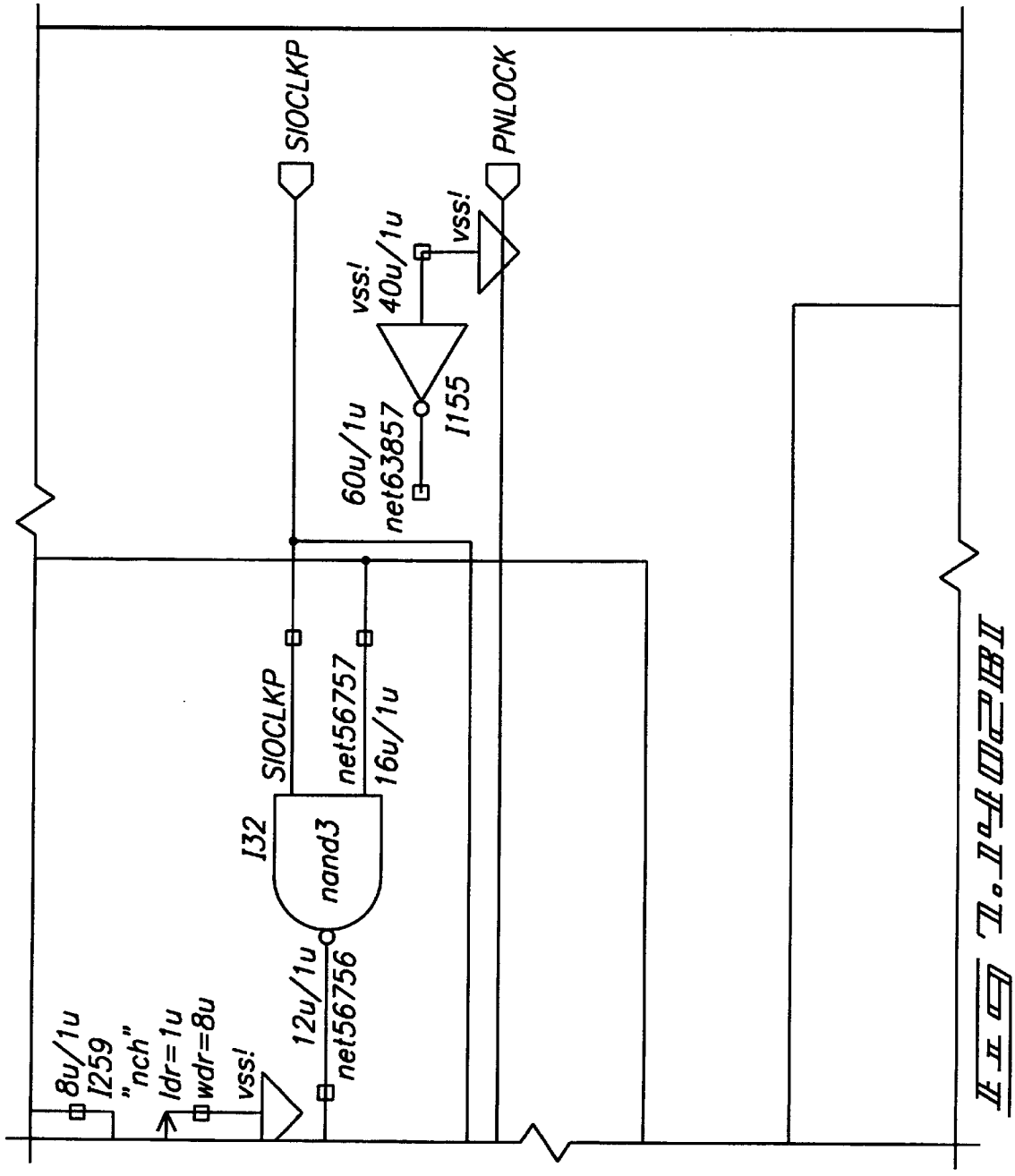

net56707
RST
vss!
net56756
PNLOCK
RXMODE
48u/1u
I31
nand3
24u/1u
COMPEN
RXMODE
net56757
16u/1u
I230
nand3
12u/1u
net56632
12u/1u
net56672
I212
net56816
8u/1u

FIG. 1130


SIOCLKP
PNLOCK
vss!
40u/1u
vss!
I155
60u/1u
net63857
SIOCLKP
net56757
16u/1u
I32
nand3
12u/1u
net56756
8u/1u
I259
"nch"
ldr=1u
wdr=8u
vss!

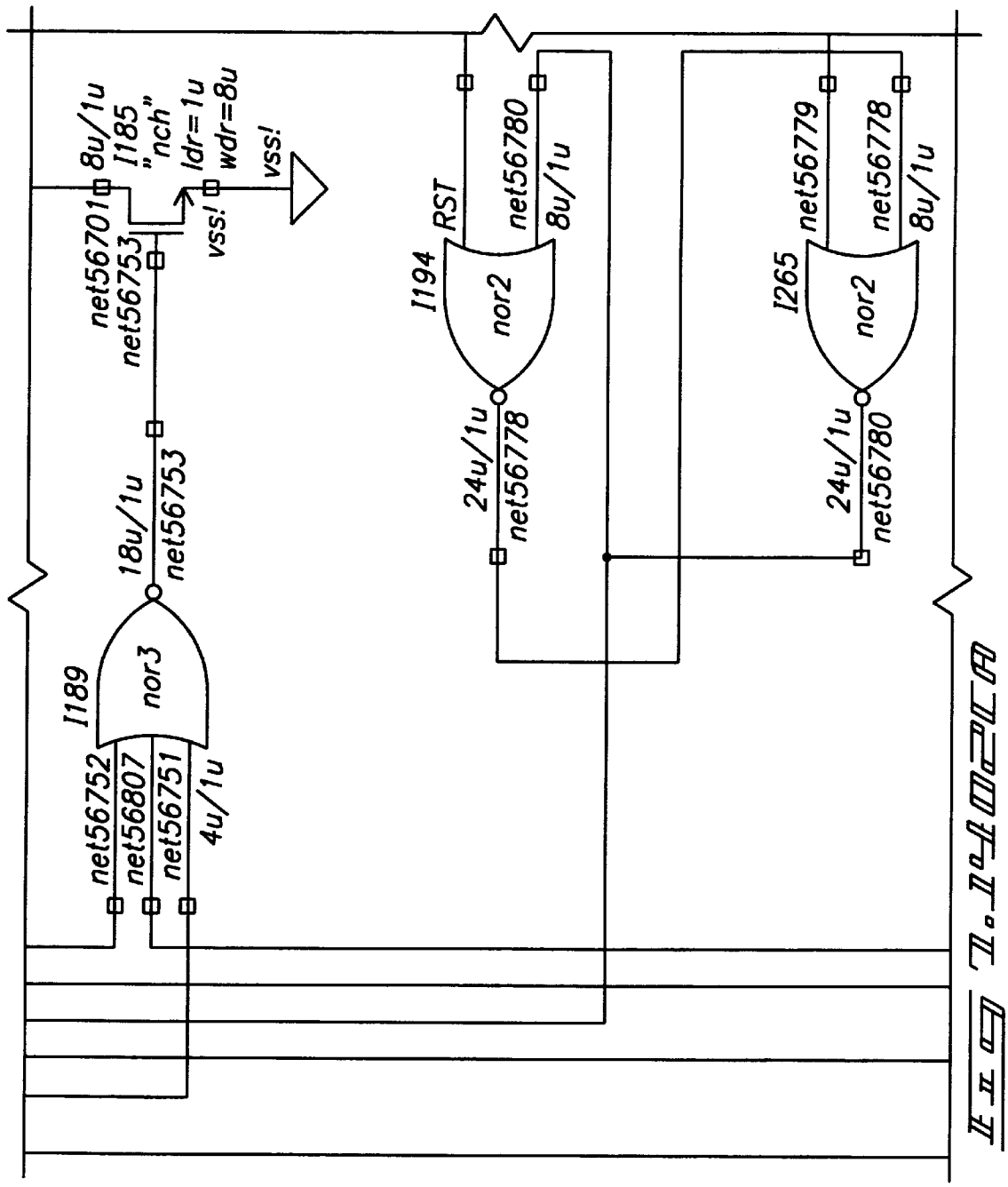
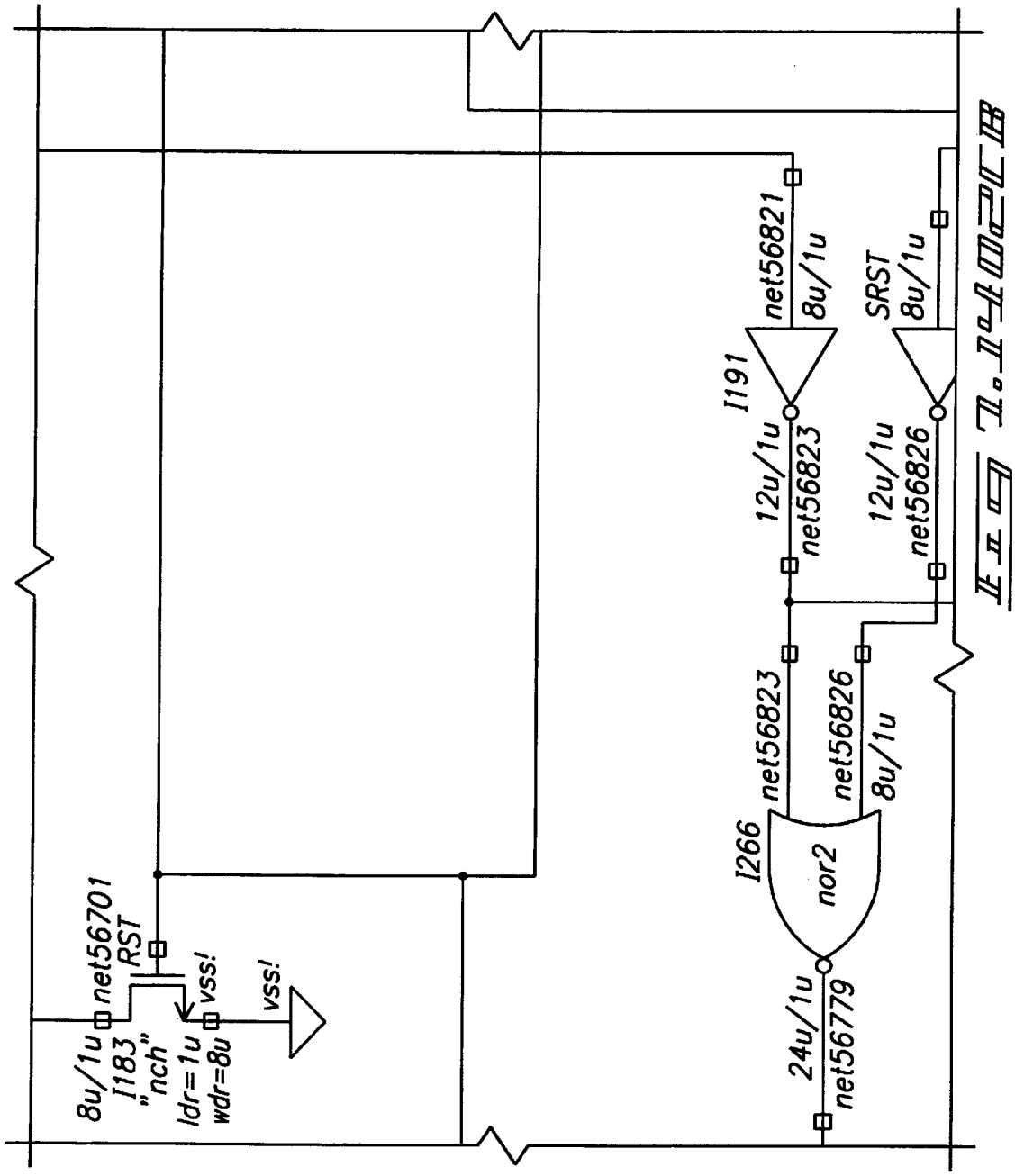

8u/1u
I185
"nch"
ldr=1u
wdr=8u
vss!
net56701
net56753
vss!
18u/1u
net56753
I189
nor3
net56752
net56807
net56751
4u/1u
I194
RST
net56780
8u/1u
nor2
24u/1u
net56778
I265
net56779
net56778
8u/1u
nor2
24u/1u
net56780

FIG. 1.1.1


net56701
RST
8u/1u
I183
"nch"
ldr=1u
wdr=8u
vss!
vss!
net56821
8u/1u
I191
12u/1u
net56823
SRST
8u/1u
12u/1u
net56826
net56823
net56826
8u/1u
I266
nor2
24u/1u
net56779

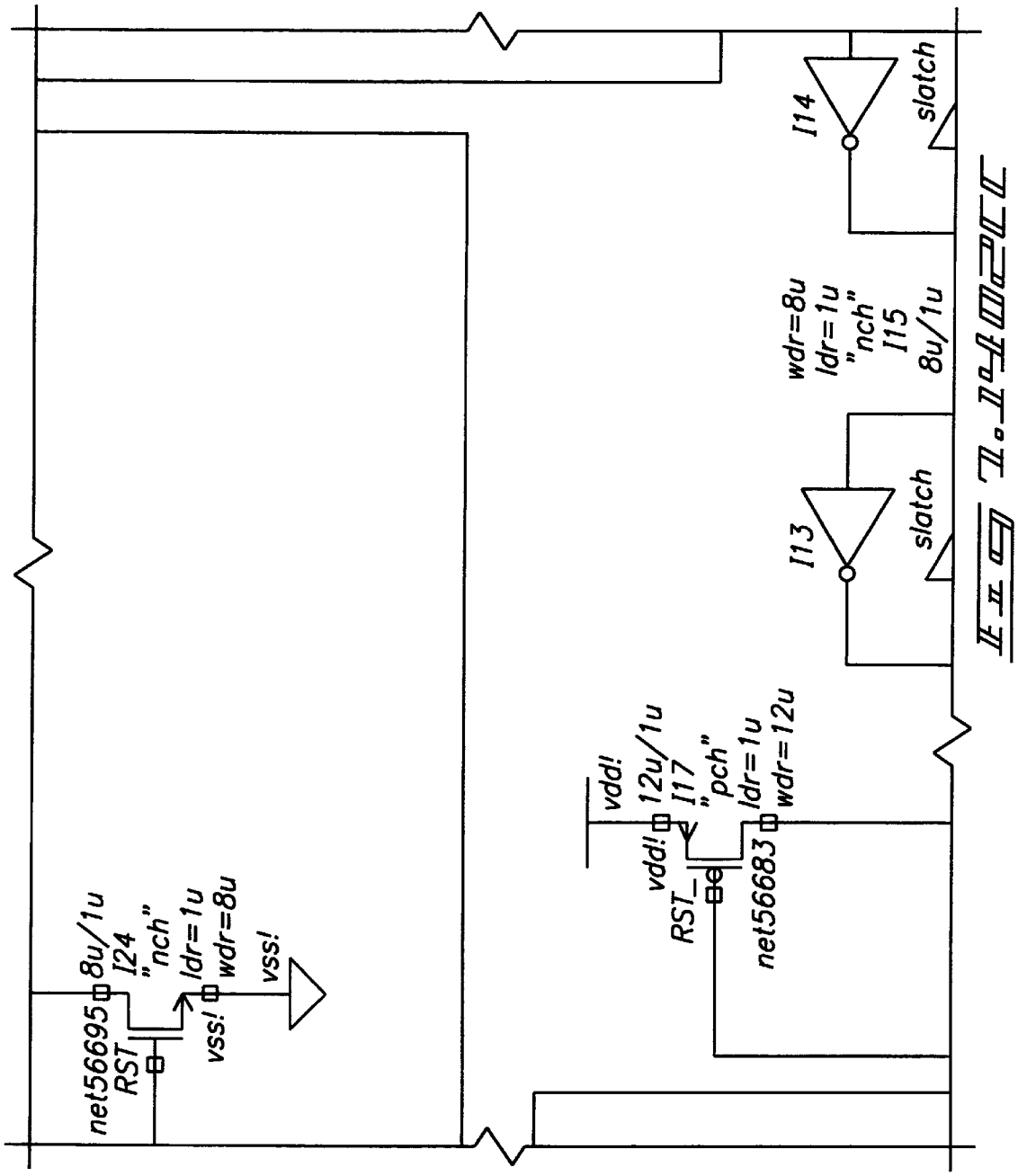

I14
slatch
wdr=8u
ldr=1u
"nch"
I15
8u/1u
I13
slatch
vdd!
12u/1u
I17
"pch"
ldr=1u
wdr=12u
vdd!
RST_
net56683
8u/1u
I24
"nch"
ldr=1u
wdr=8u
vss!
net56695
RST
vss!

FIG. 1L

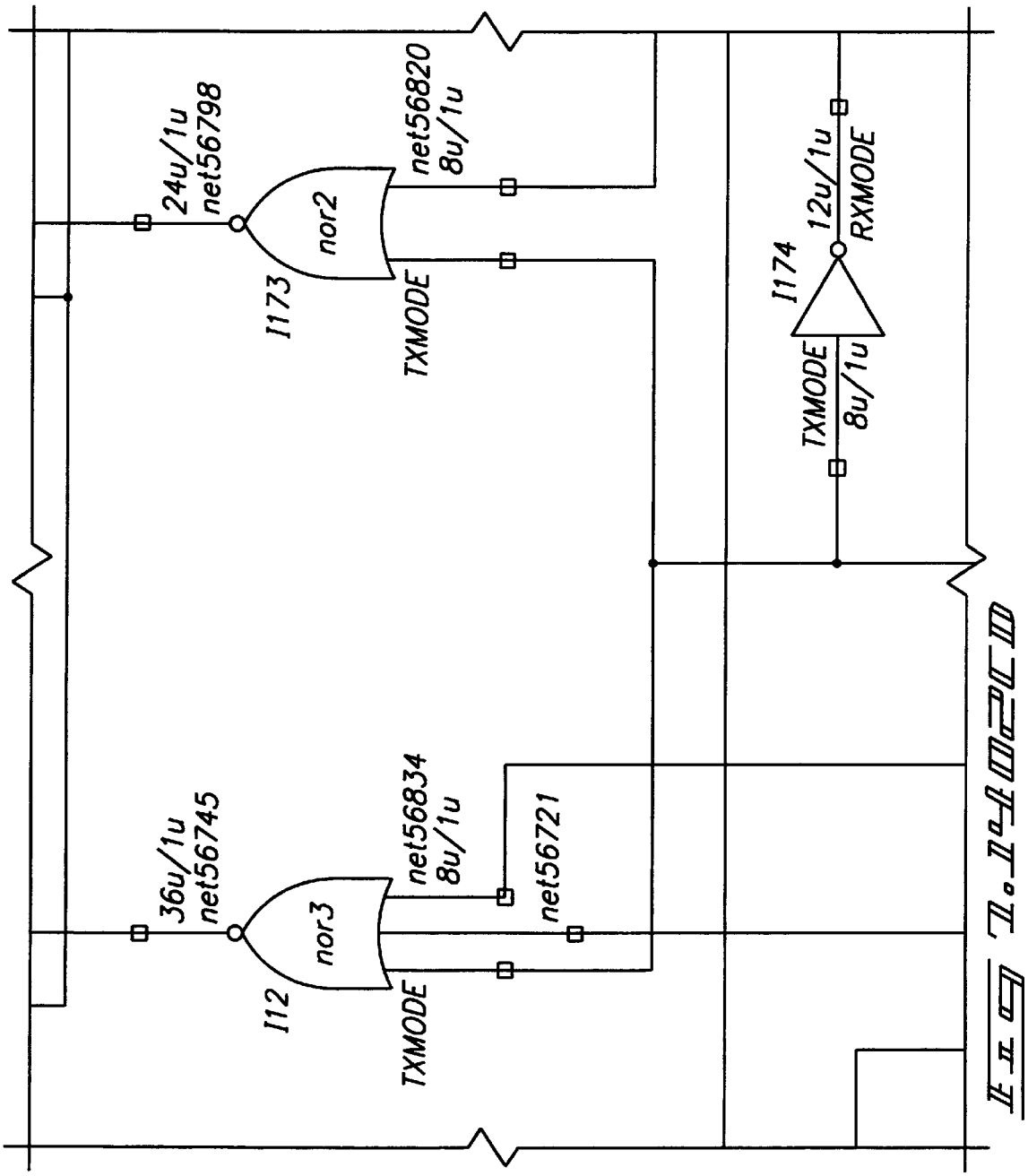

24u/1u
net56798
net56820
8u/1u
nor2
I173
TXMODE
I174
12u/1u
RXMODE
TXMODE
8u/1u
36u/1u
net56745
net56834
8u/1u
net56721
nor3
I12
TXMODE

FIG. 1204L

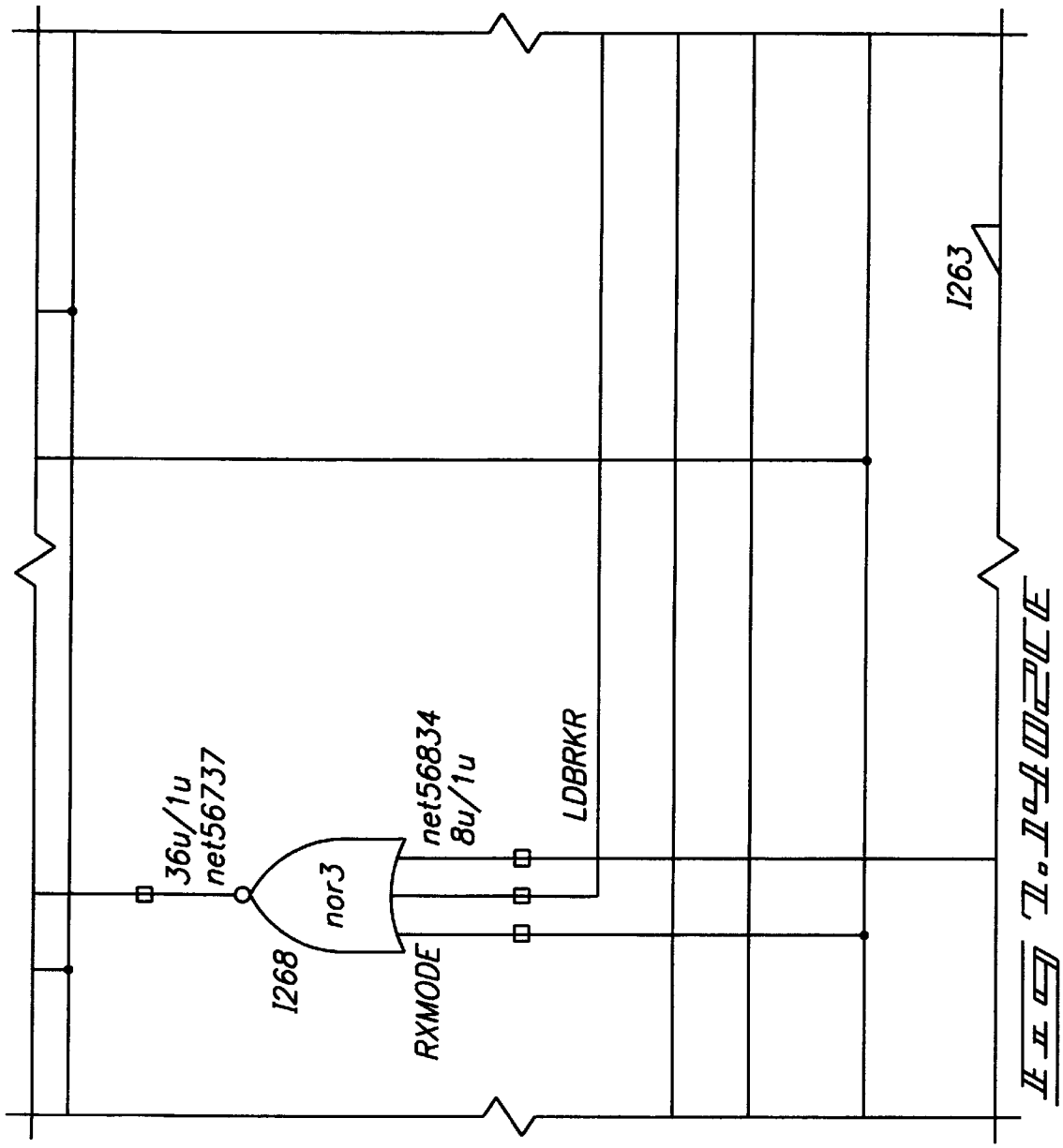
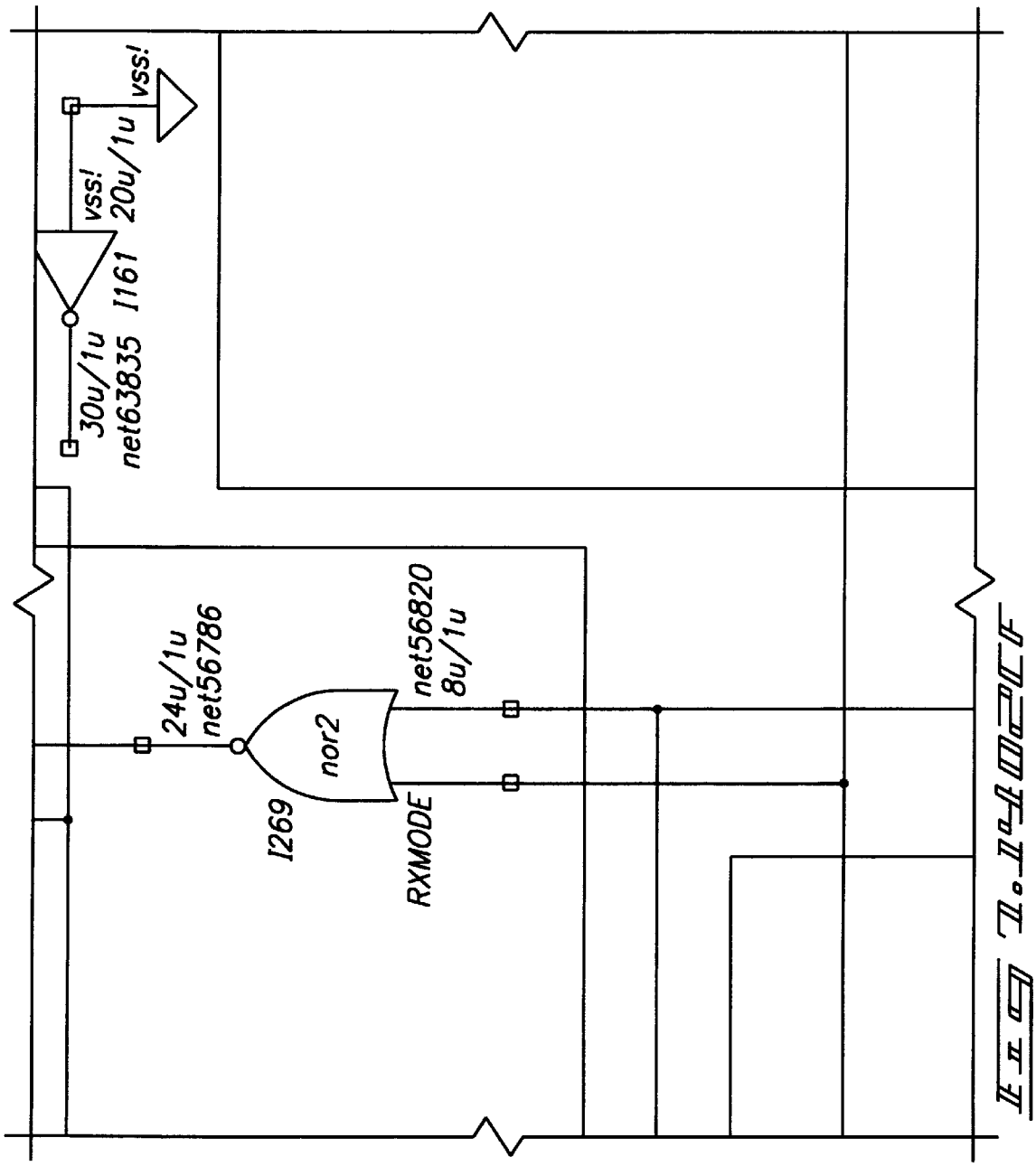
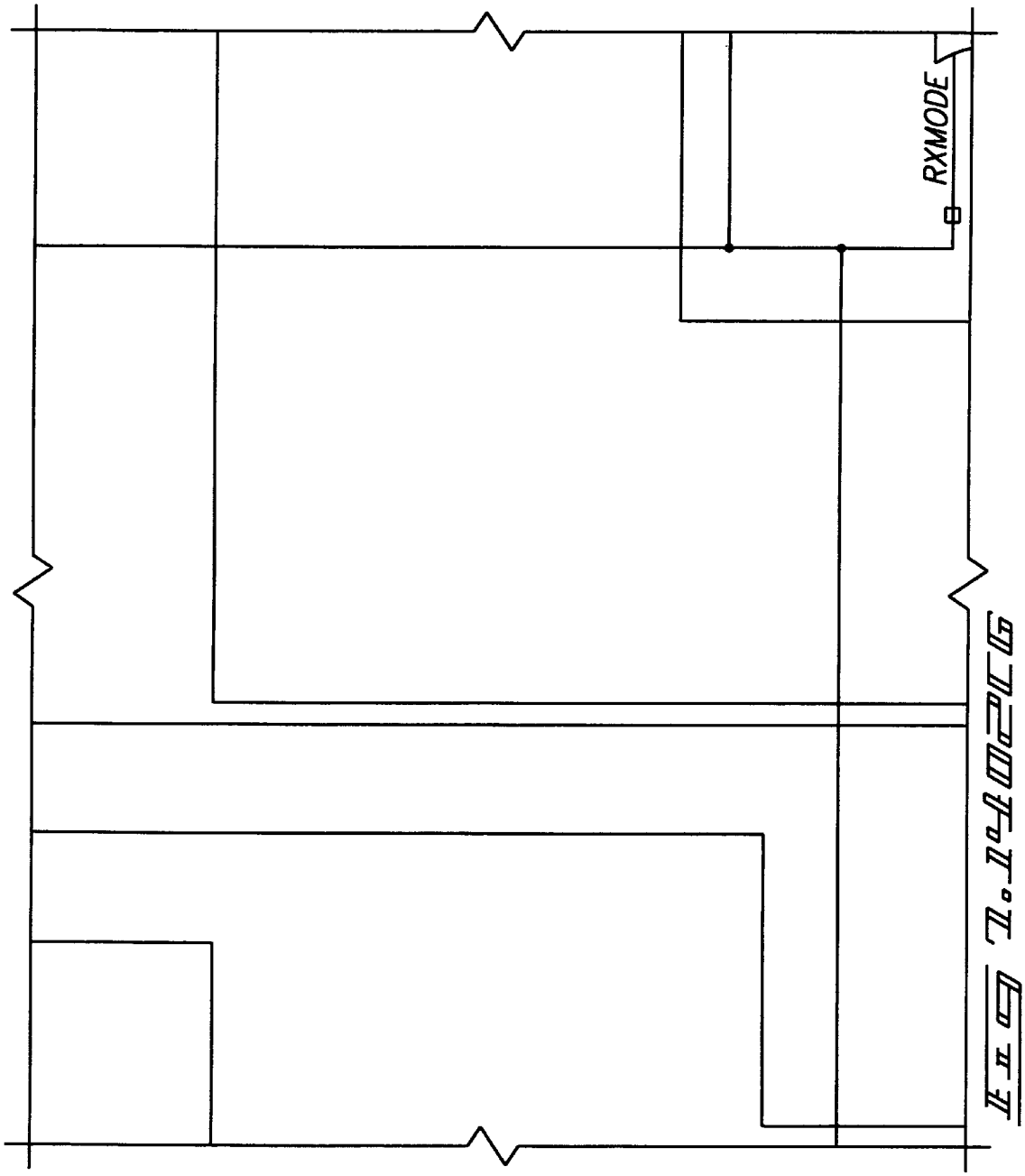


FIG. 1.1463E


vss!
vss!
20u/1u
I161
30u/1u
net63835
24u/1u
net56786
nor2
net56820
8u/1u
I269
RXMODE


RXMODE
FIG. 1011

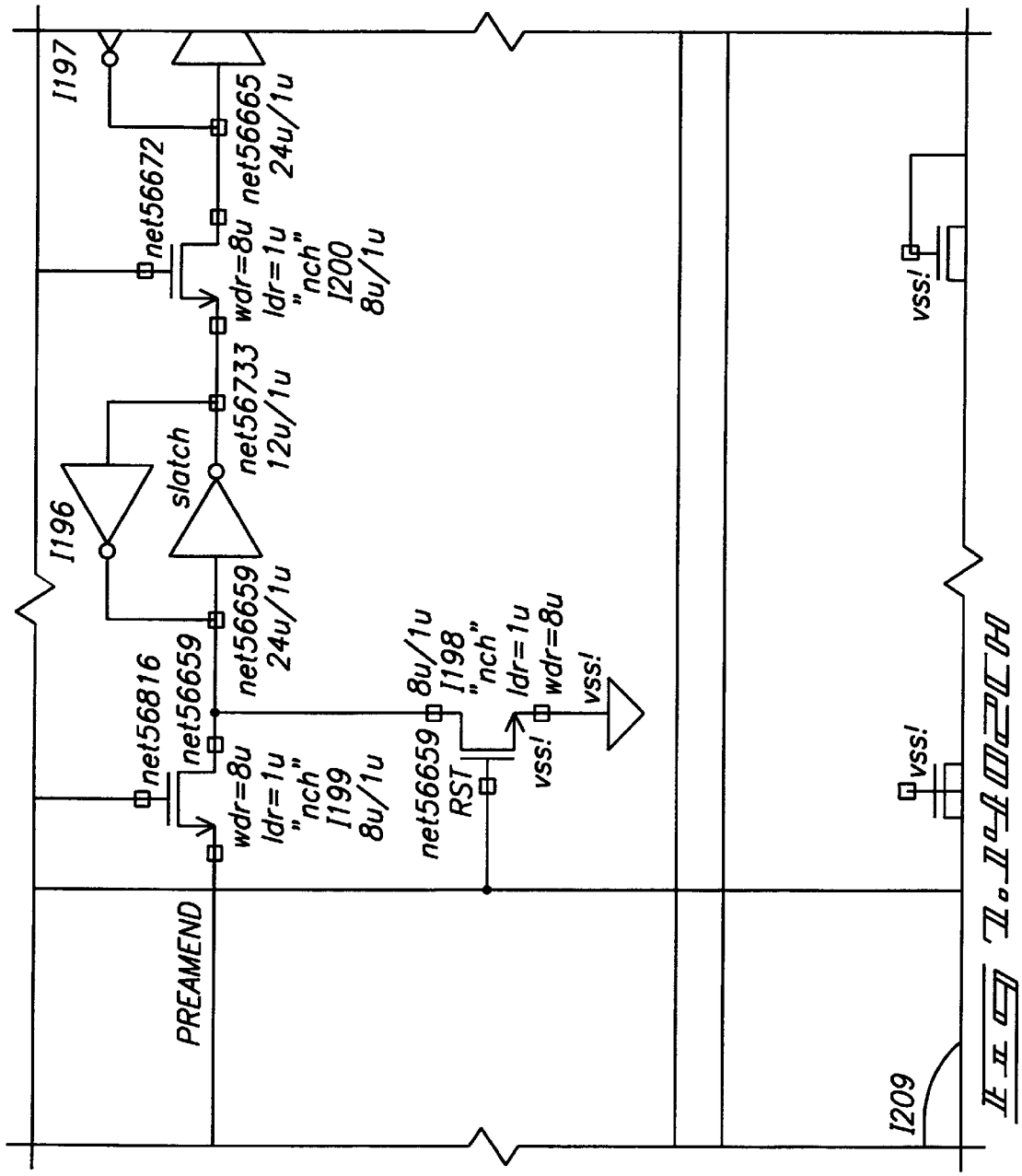

I197
net56672
net56665
24u/1u
wdr=8u
ldr=1u
"nch"
I200
8u/1u
net56733
12u/1u
slatch
I196
net56659
24u/1u
net56816
net56659
wdr=8u
ldr=1u
"nch"
I199
8u/1u
PREAMEND
net56659
RST
8u/1u
I198
"nch"
ldr=1u
wdr=8u
vss!
vss!
vss!
vss!
I209

FIG 6L

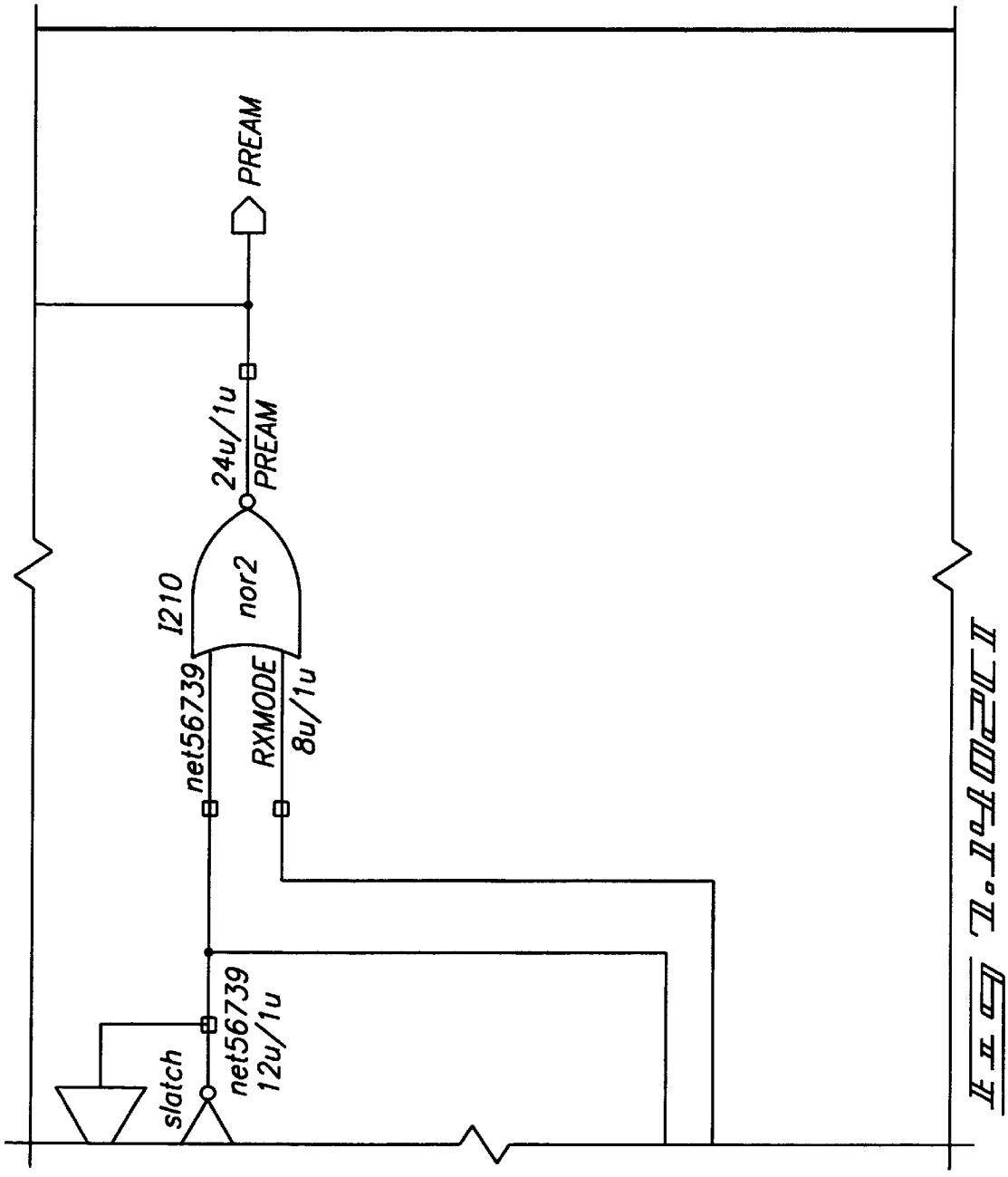

PREAM
24u/1u
PREAM
I210
nor2
net56739
RXMODE
8u/1u
net56739
12u/1u
slatch

FIG. 1207

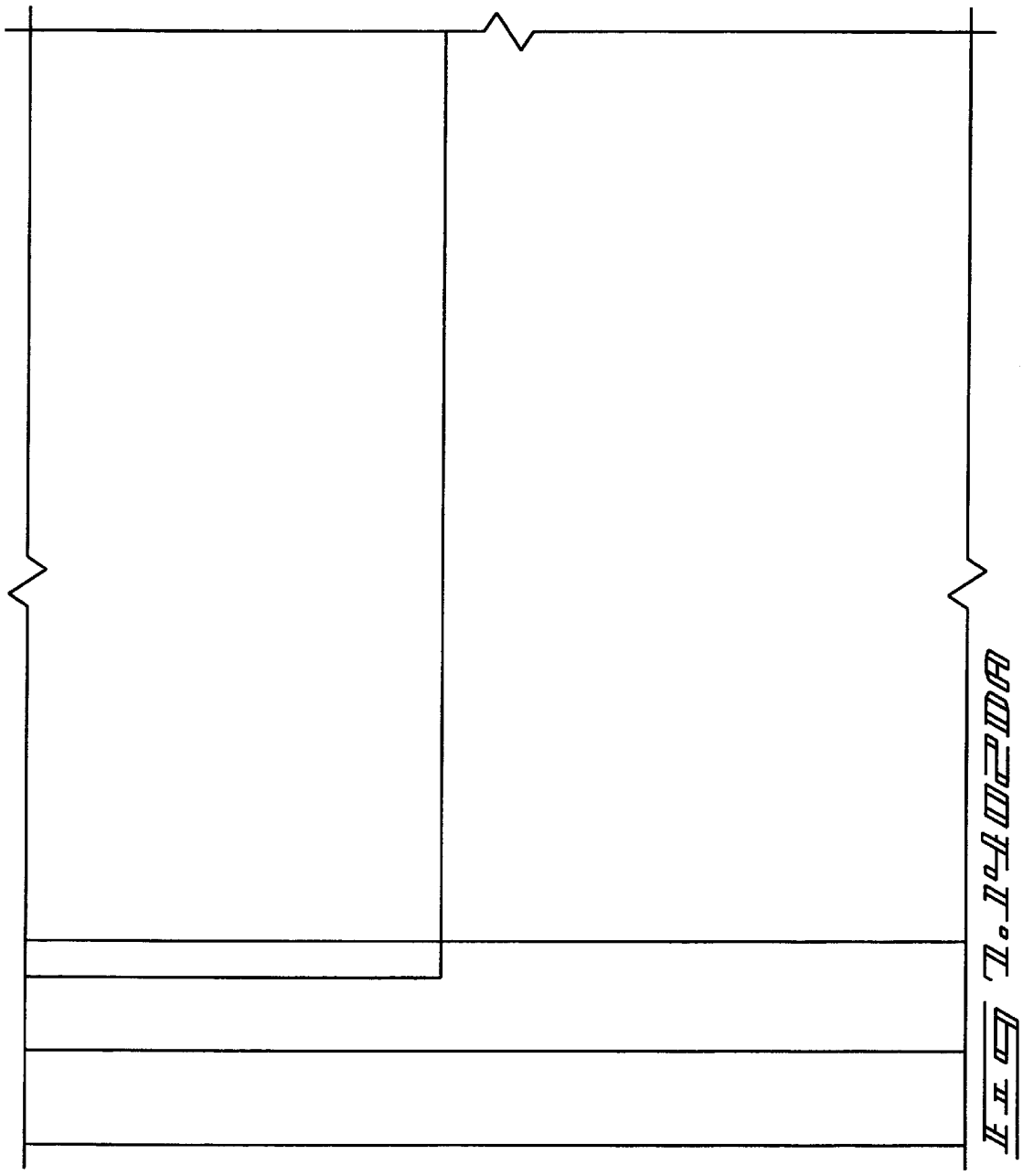
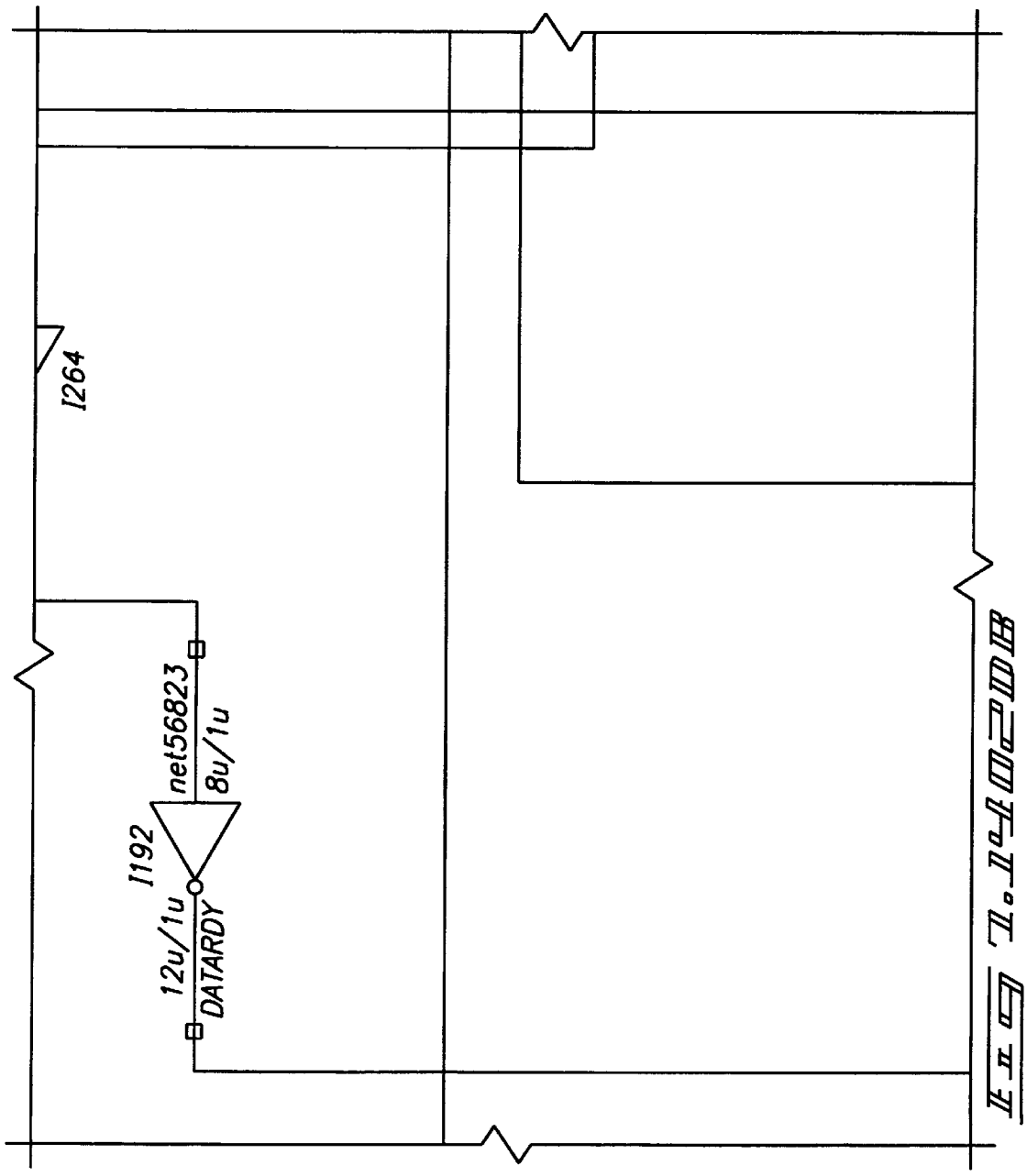


FIG. 1,402A


I264
net56823
8u/1u
I192
12u/1u
DATARDY
FIG. 1015

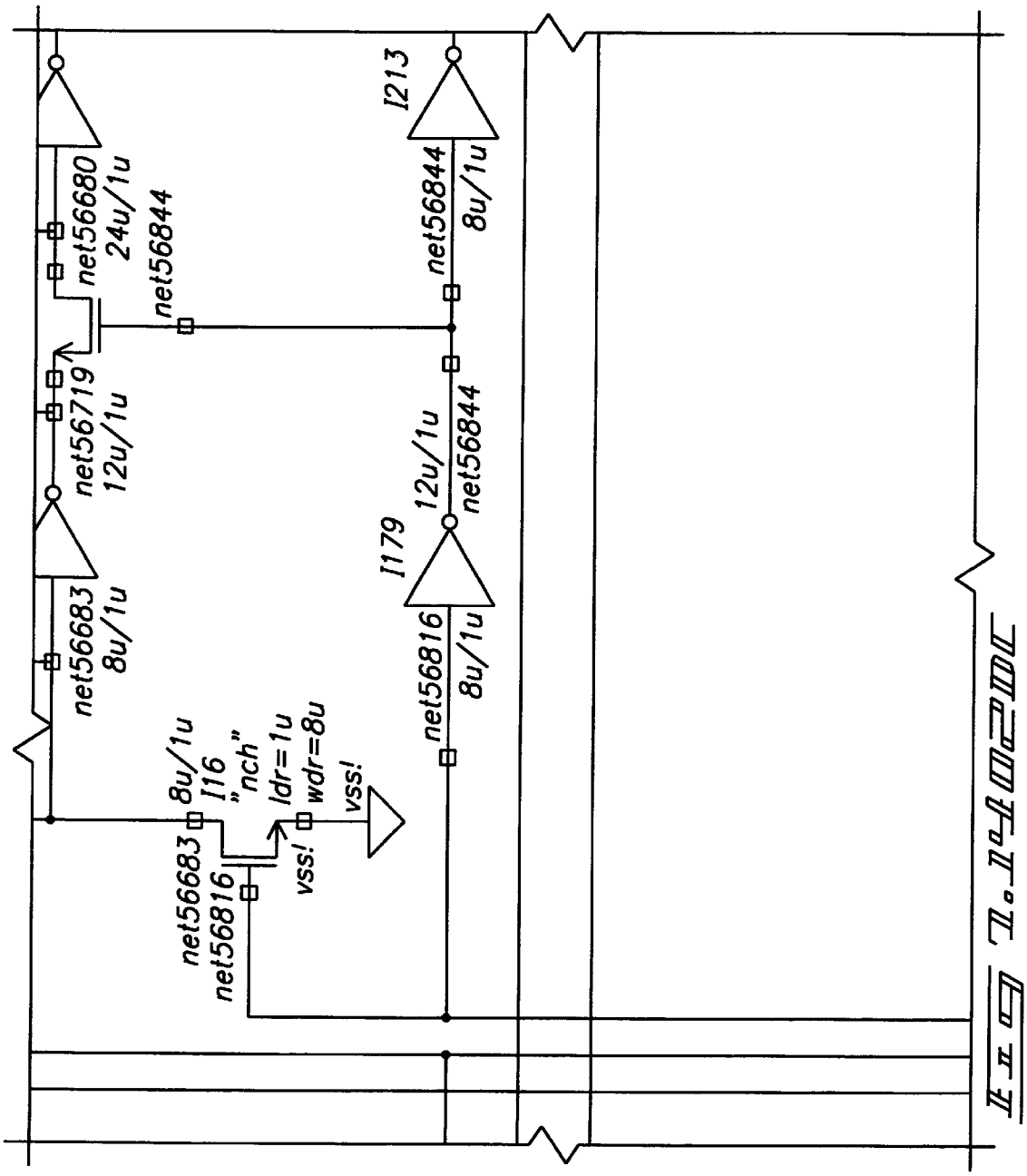
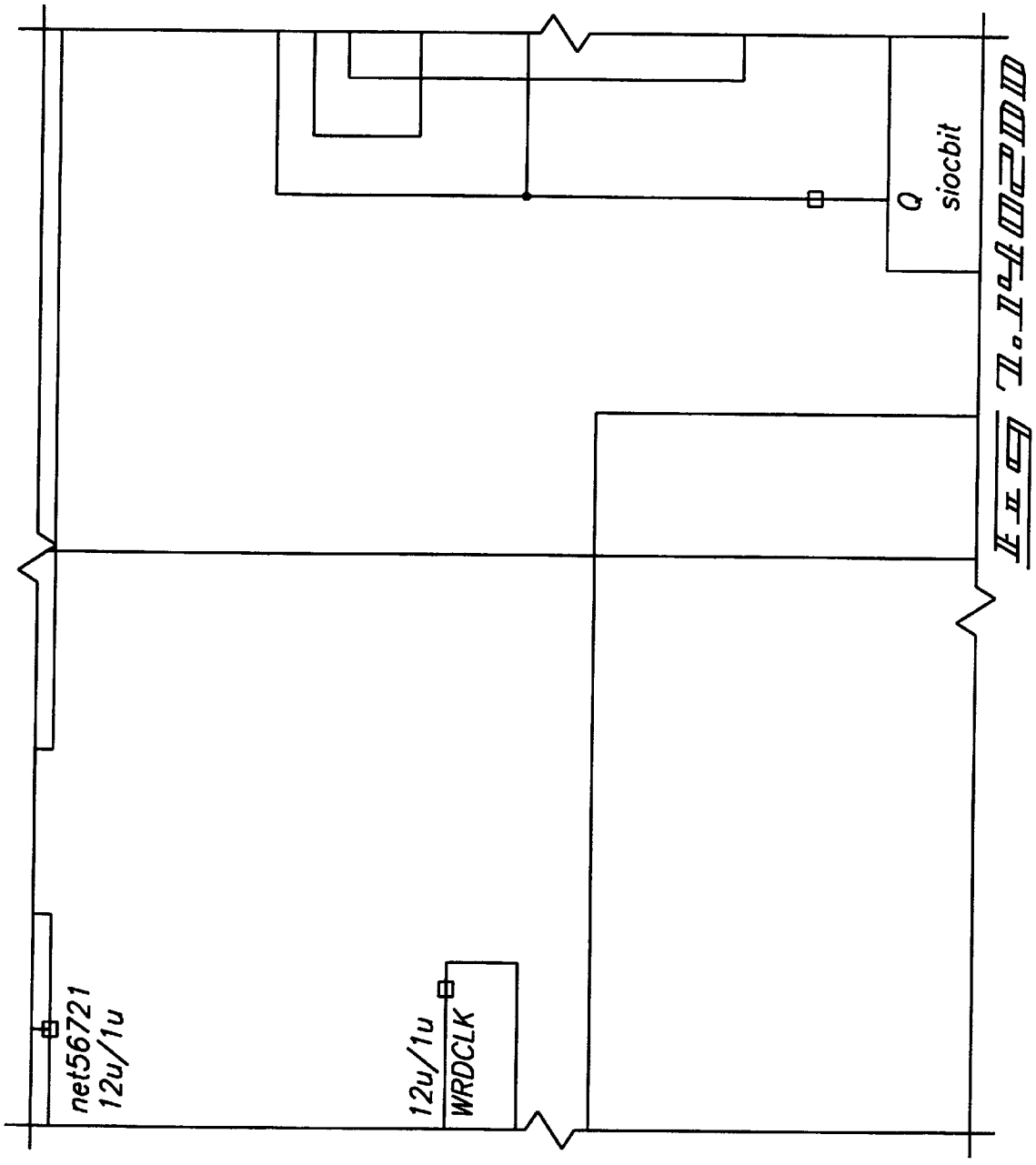
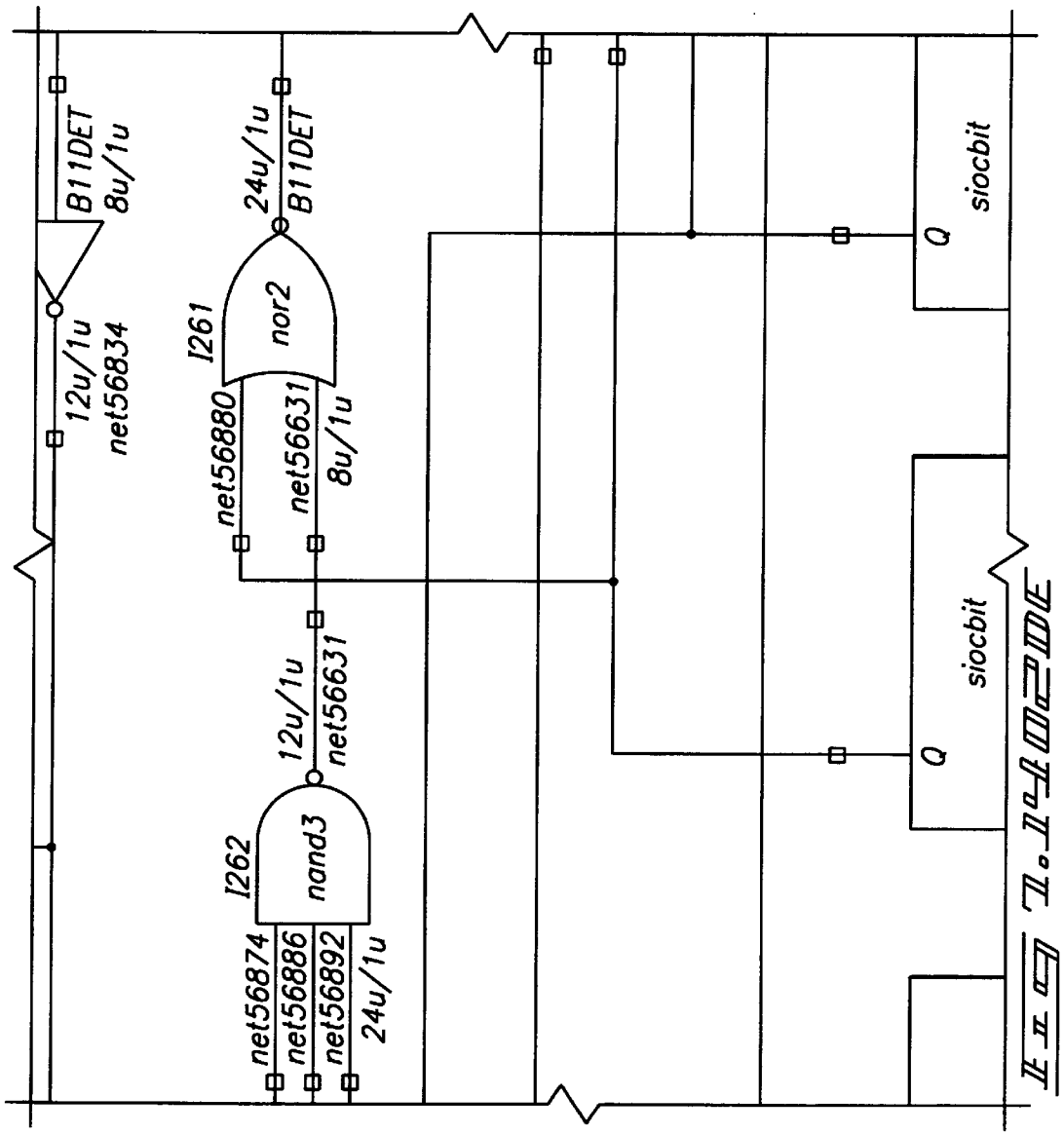
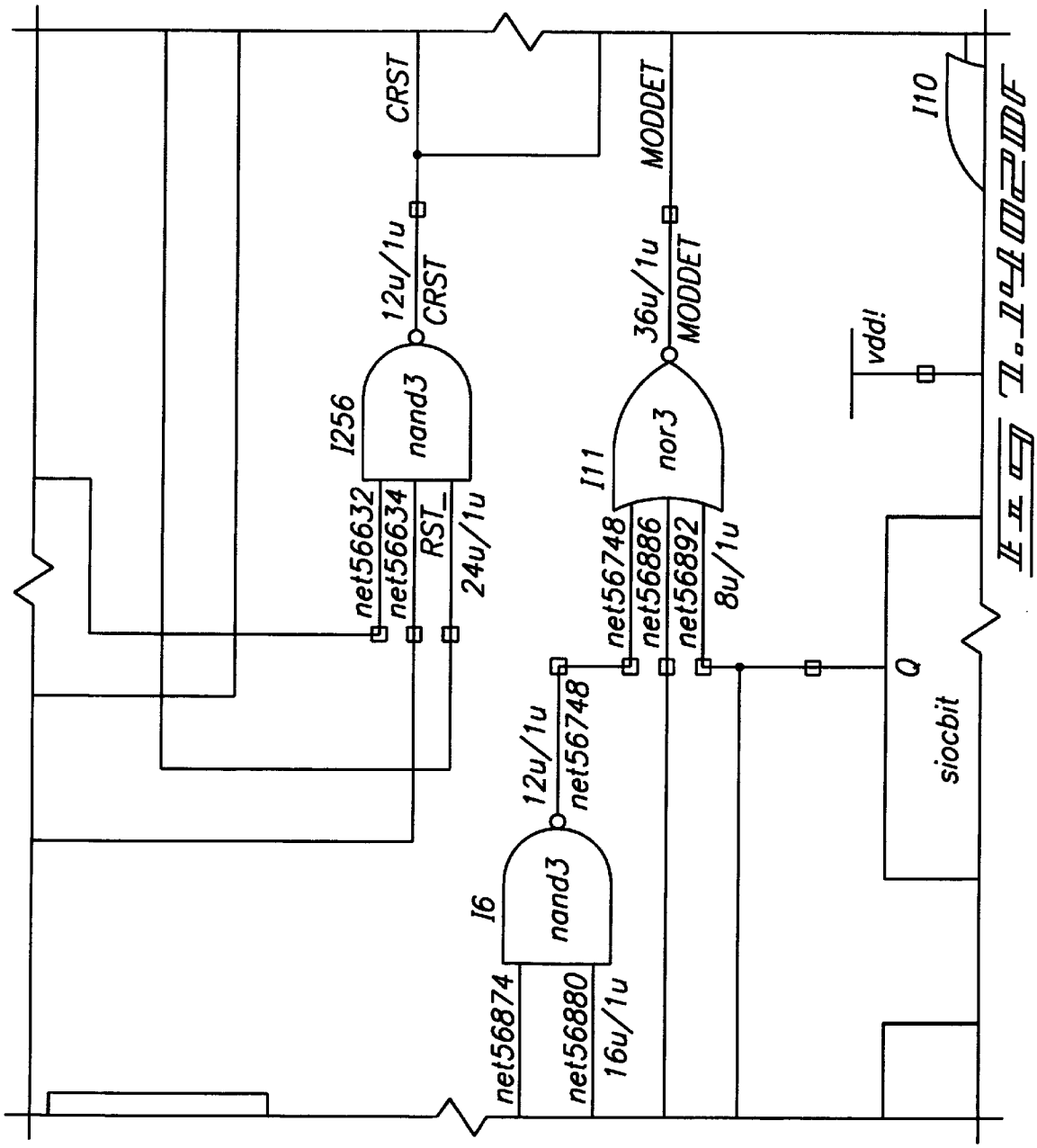

I213
net56844
8u/1u
net56680
24u/1u
net56844
net56719
12u/1u
net56683
8u/1u
I179
12u/1u
net56844
net56816
8u/1u
8u/1u
I16
„nch"
ldr=1u
wdr=8u
vss!
net56683
net56816
vss!

FIG 31


Q
siocbit
net56721
12u/1u
12u/1u
WRDCLK


B11DET
8u/1u
12u/1u
net56834
24u/1u
B11DET
I261
nor2
net56880
net56631
8u/1u
12u/1u
net56631
I262
nand3
net56874
net56886
net56892
24u/1u
Q
siocbit
Q
siocbit


CRST
MODDET
I10
12u/1u
CRST
36u/1u
MODDET
vdd!
I256
nand3
I11
nor3
net56632
net56634
RST_
24u/1u
net56748
net56886
net56892
8u/1u
Q
siocbit
12u/1u
net56748
I6
nand3
net56874
net56880
16u/1u

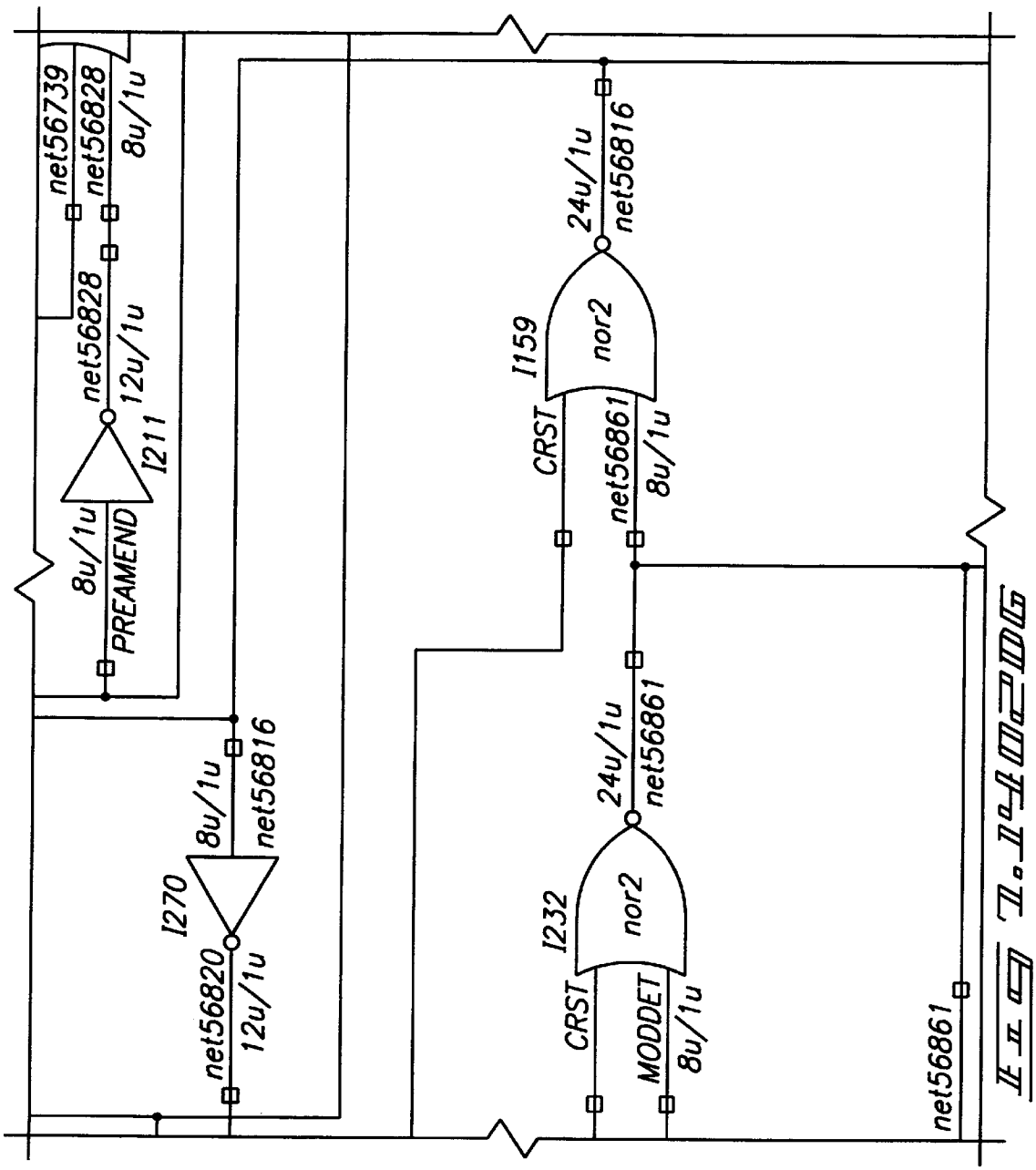
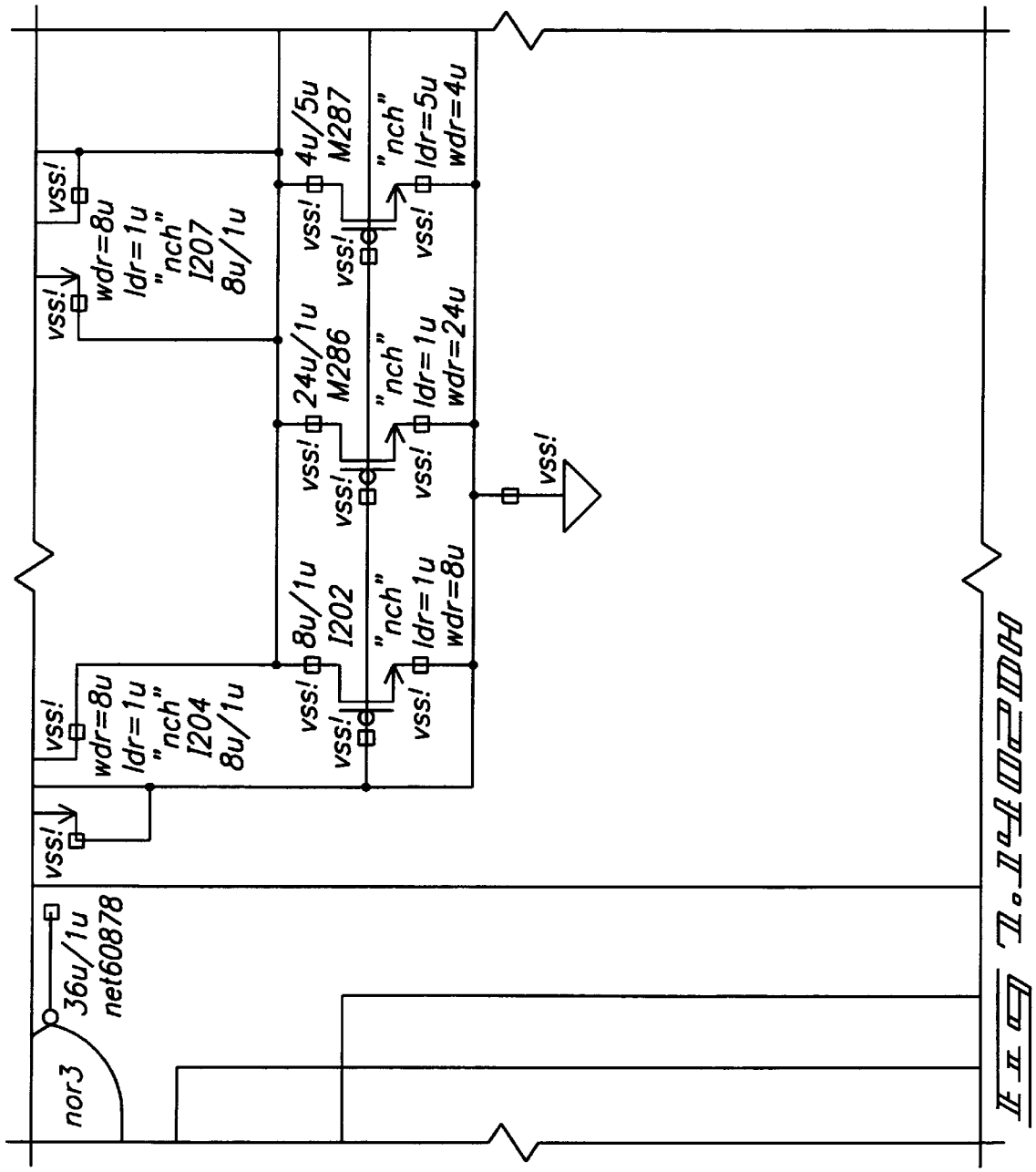
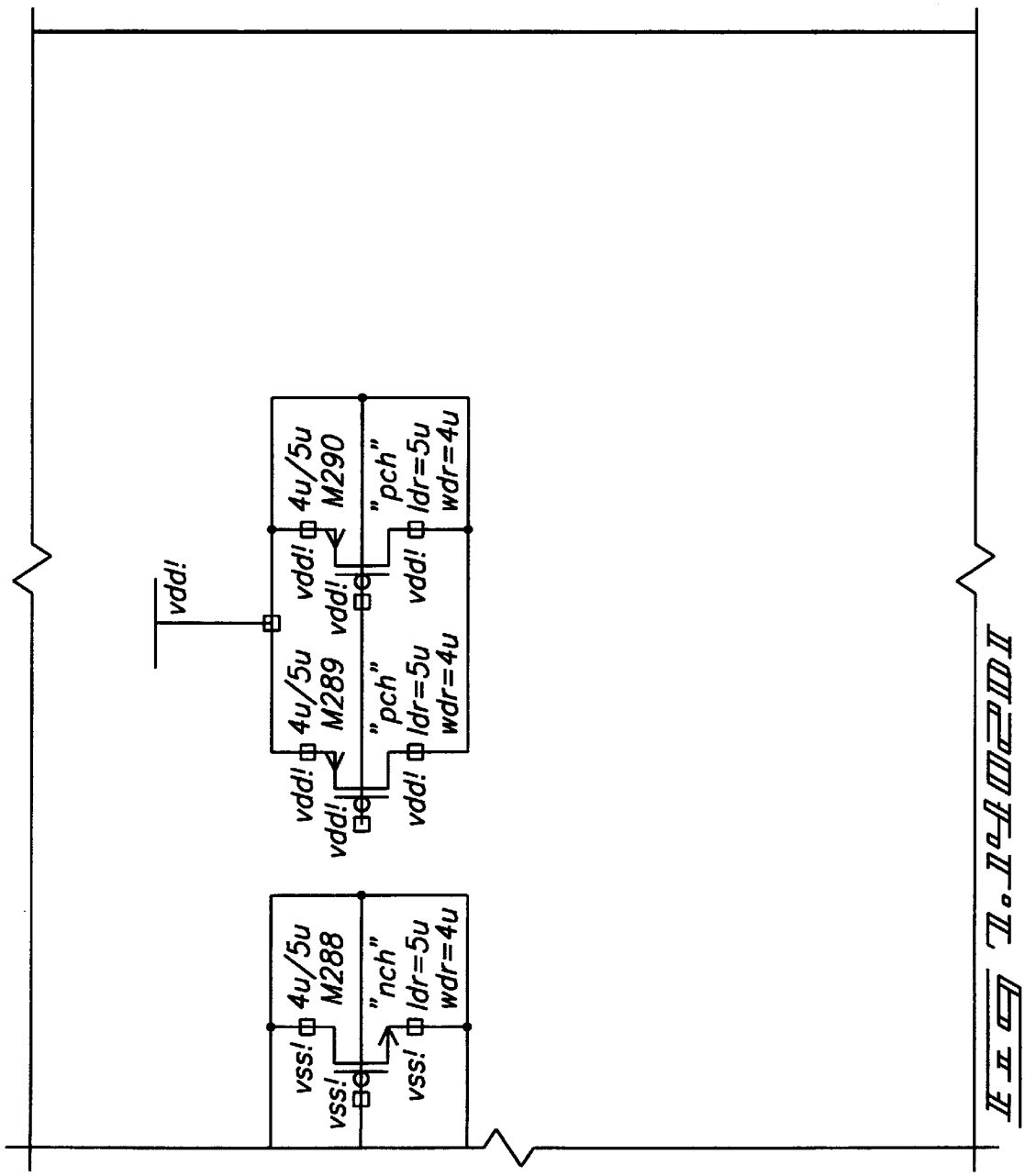

net56739
net56828
8u/1u
net56828
12u/1u
I211
8u/1u
PREAMEND
8u/1u
net56816
I270
net56820
12u/1u
24u/1u
net56816
I159
nor2
CRST
net56861
8u/1u
24u/1u
net56861
I232
nor2
CRST
MODDET
8u/1u
net56861

FIG. 1020


net60878
36u/1u
nor3
vss!
wdr=8u
ldr=1u
"nch"
I204
8u/1u
I202
8u/1u
M286
24u/1u
M287
4u/5u
I207
8u/1u
ldr=1u
ldr=5u
wdr=24u
wdr=4u


vdd!
4u/5u M290
"pch" ldr=5u wdr=4u
4u/5u M289
"pch" ldr=5u wdr=4u
4u/5u M288
"nch" ldr=5u wdr=4u
vss!
vdd!

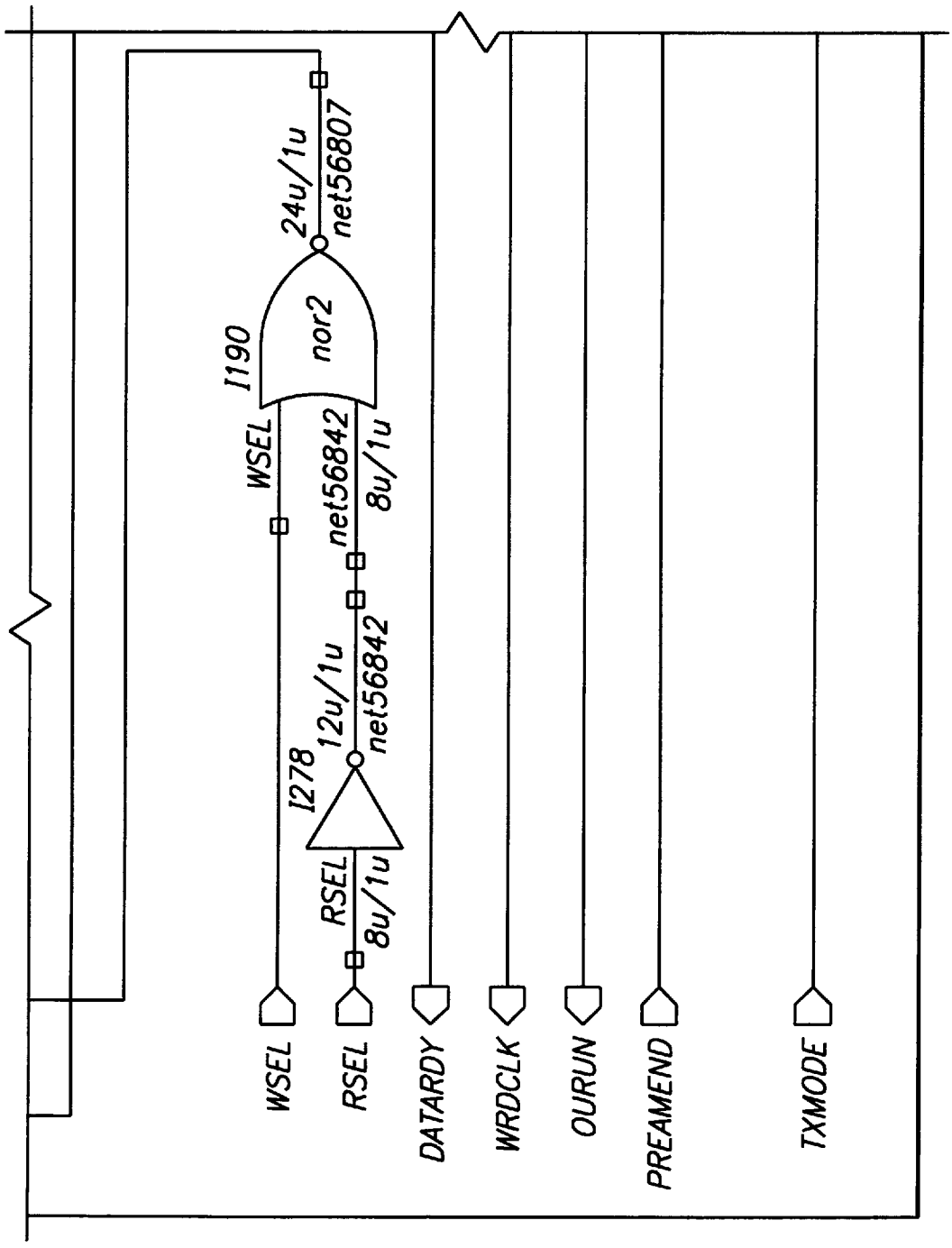

I190
nor2
24u/1u
net56807
WSEL
net56842
8u/1u
I278
12u/1u
net56842
RSEL
8u/1u
WSEL
RSEL
DATARDY
WRDCLK
OURUN
PREAMEND
TXMODE

FIG. 1023

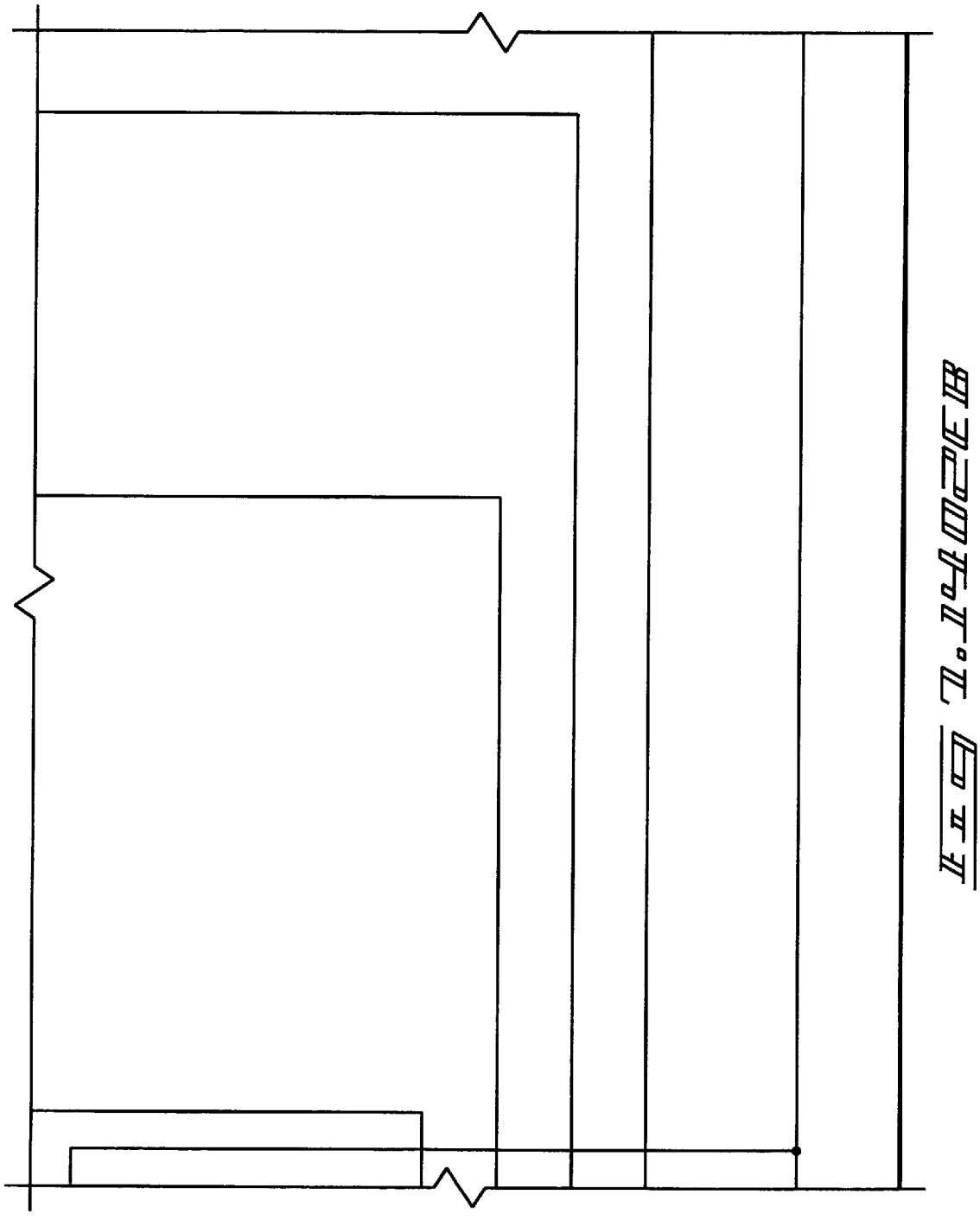


FIG. 1024

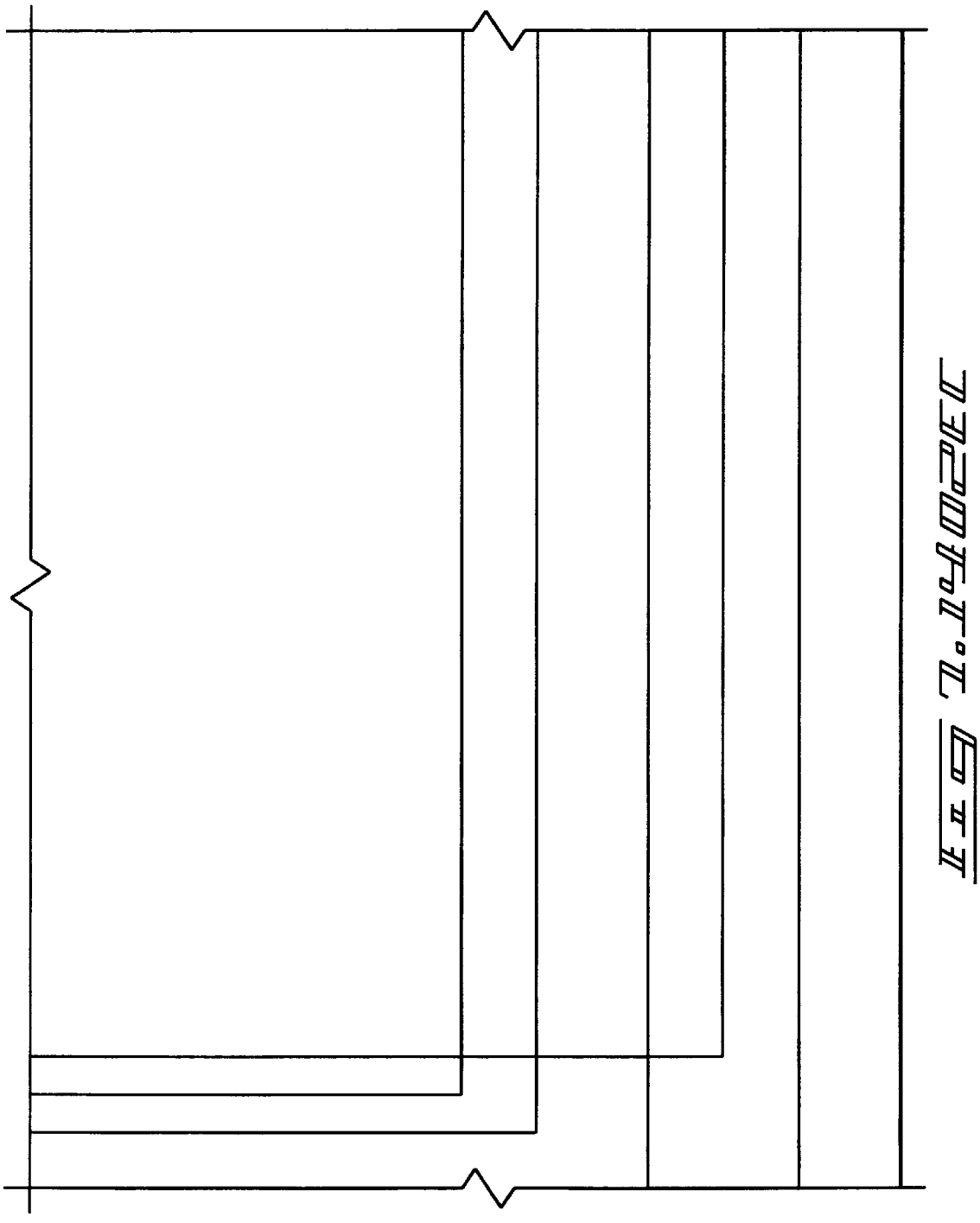


FIG. 1025

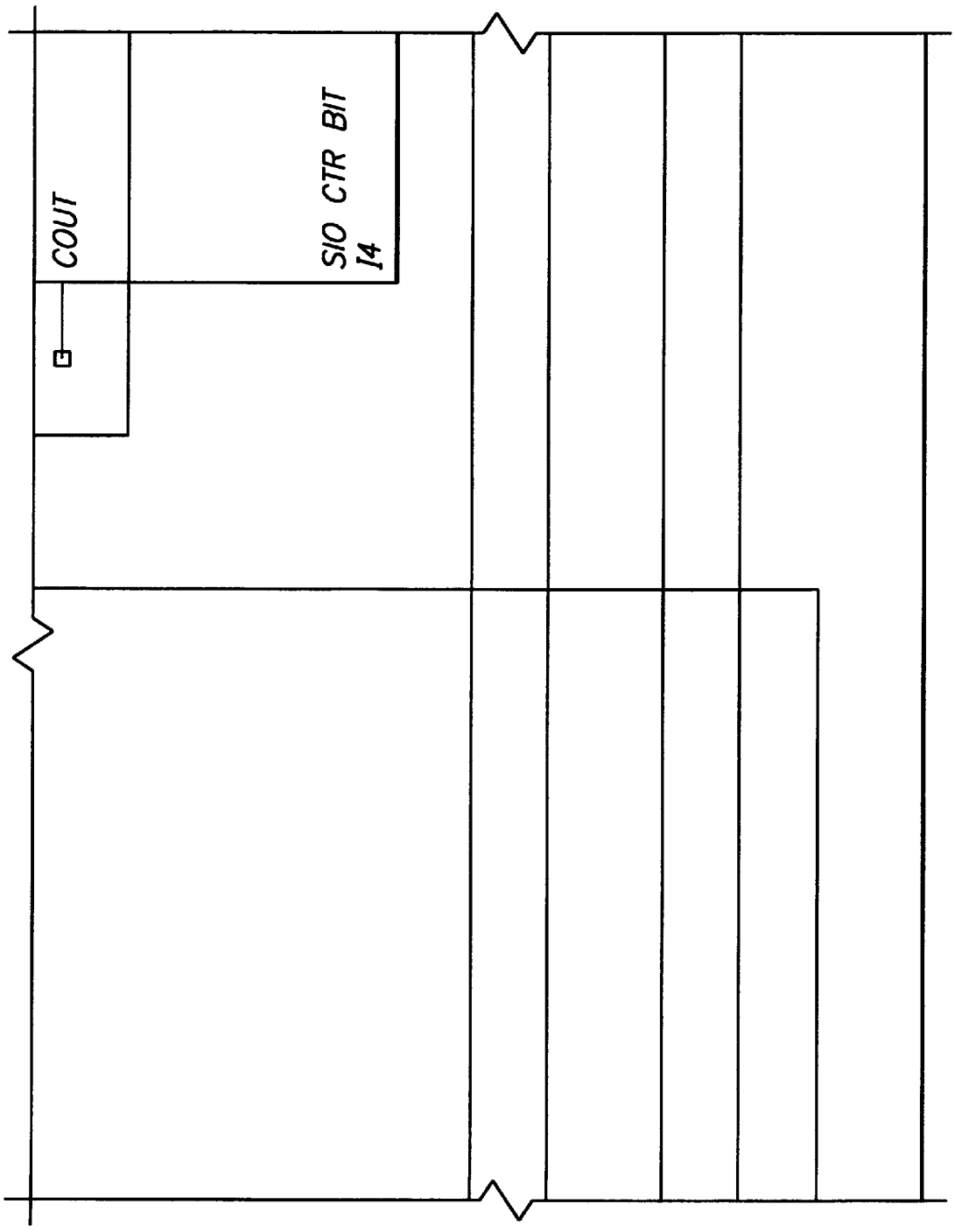


FIG 1L

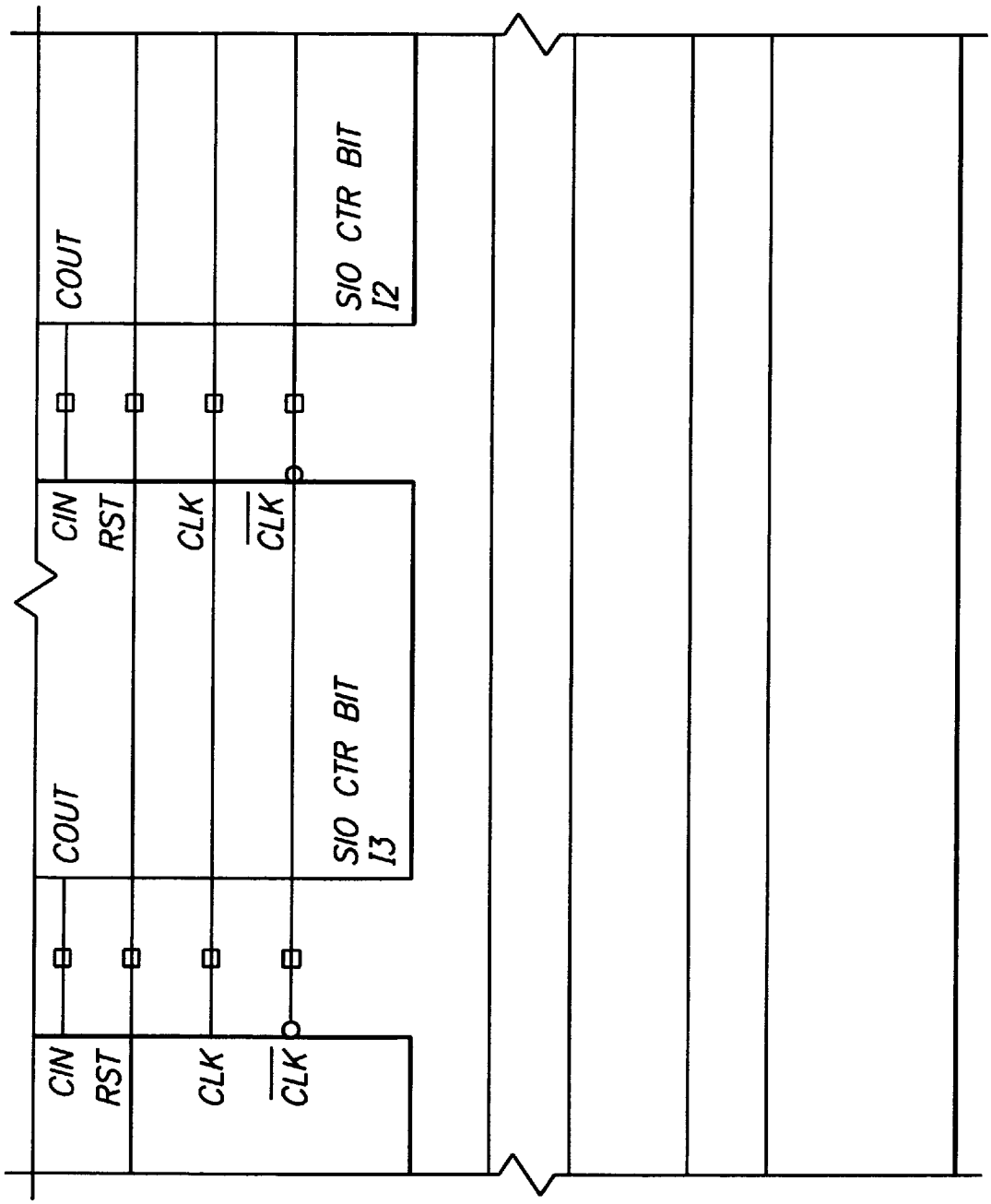

SIO CTR BIT I2
COUT
CIN
RST
CLK
$\overline{CLK}$
SIO CTR BIT I3
COUT
CIN
RST
CLK
$\overline{CLK}$

FIG. 14

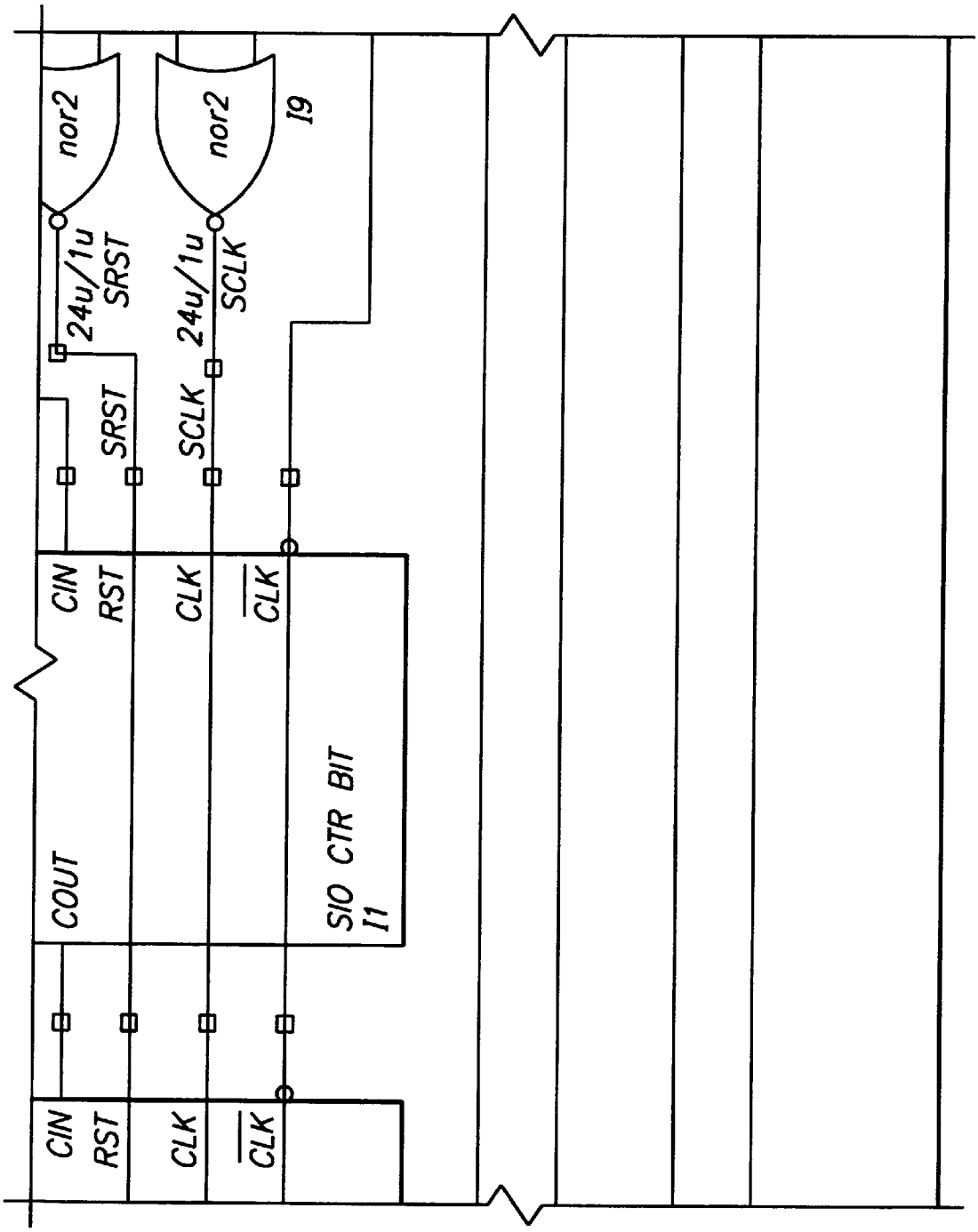

nor2
nor2
19
24u/1u
SRST
24u/1u
SCLK
SRST
SCLK
CIN
RST
CLK
CLK
COUT
SIO CTR BIT
11
CIN
RST
CLK
CLK

FIG. 11.

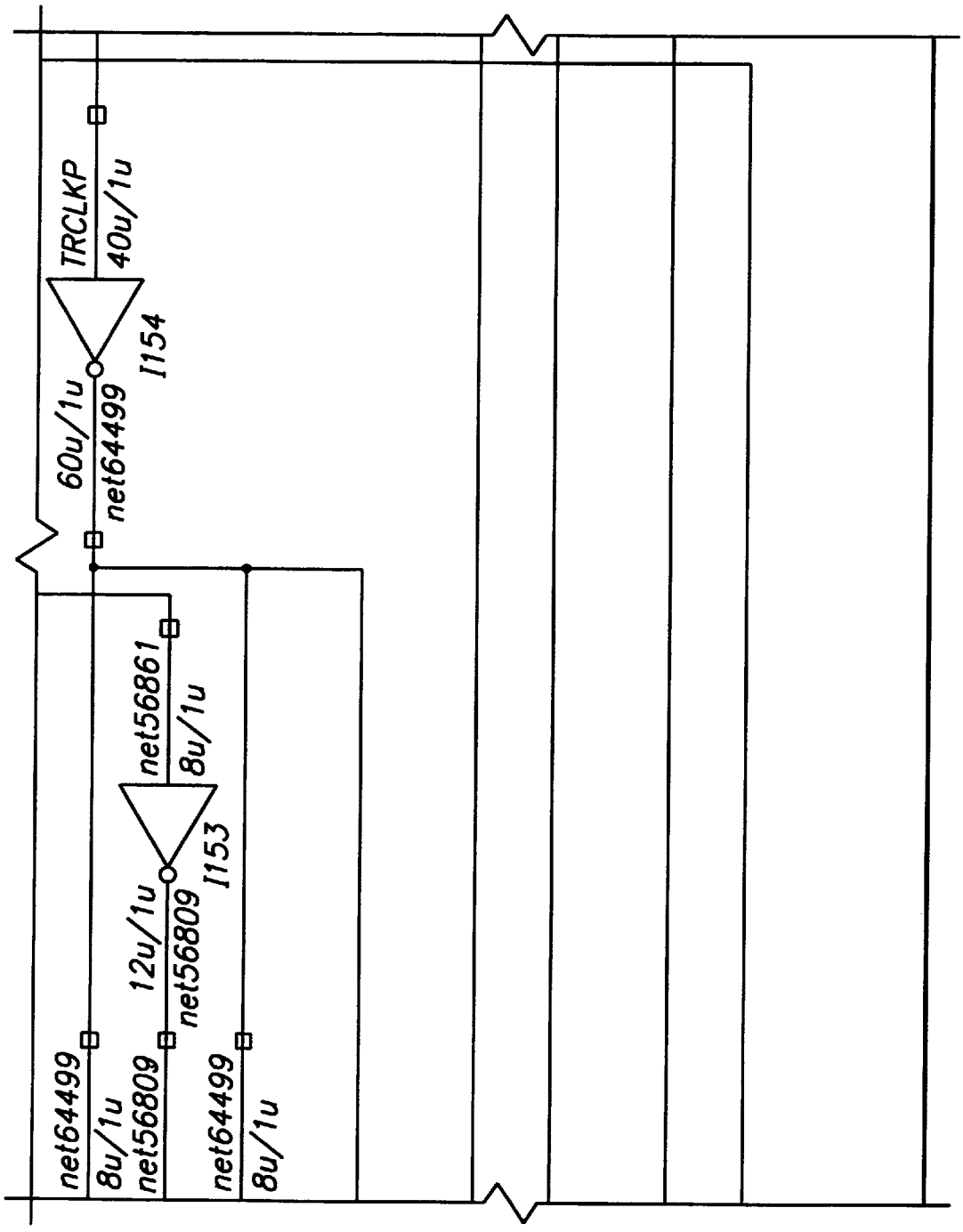

TRCLKP
40u/1u
I154
60u/1u
net64499
net56861
8u/1u
I153
12u/1u
net56809
net64499
8u/1u
net56809
8u/1u
net64499
8u/1u

FIG. 1029

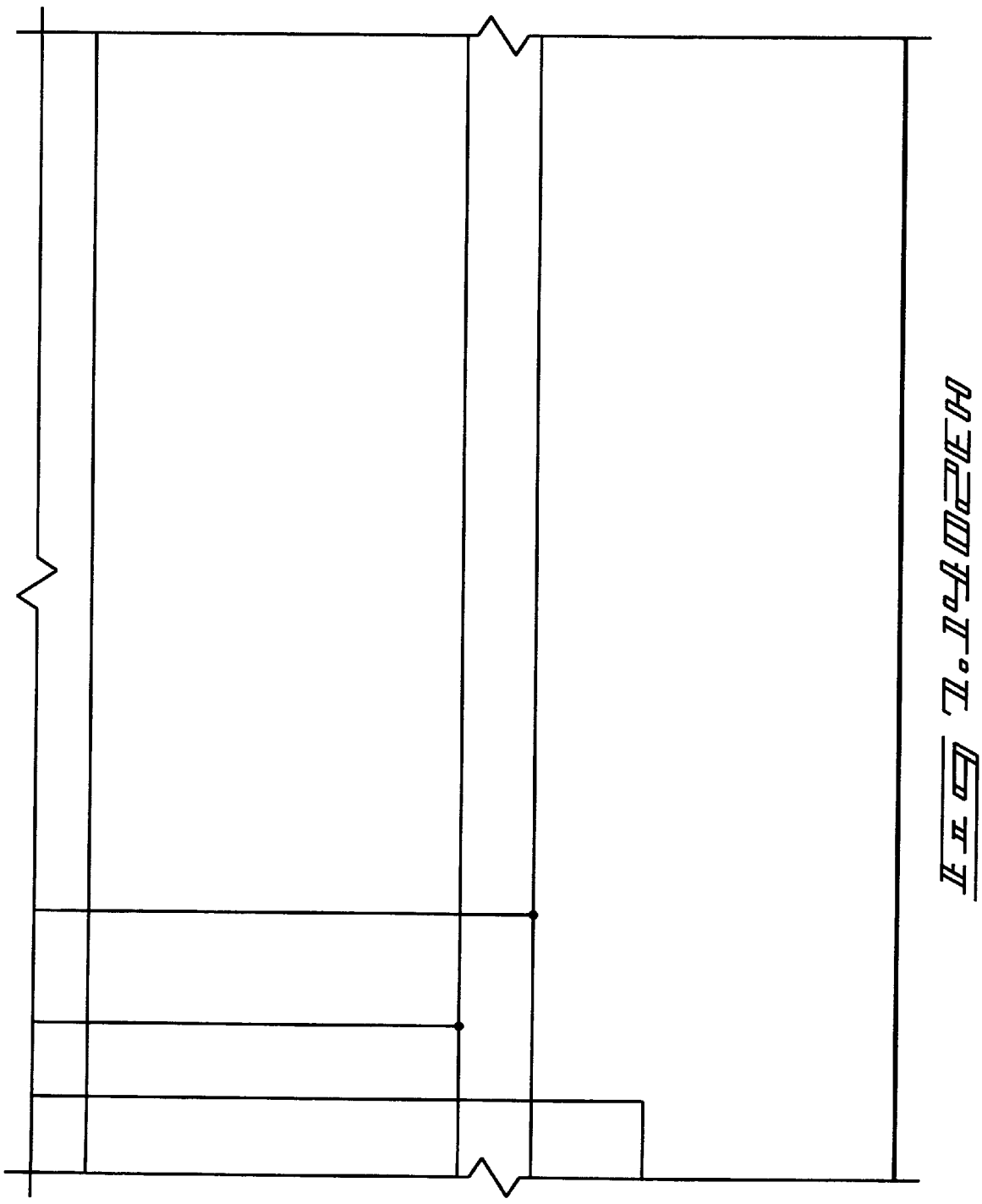


FIG. 1030

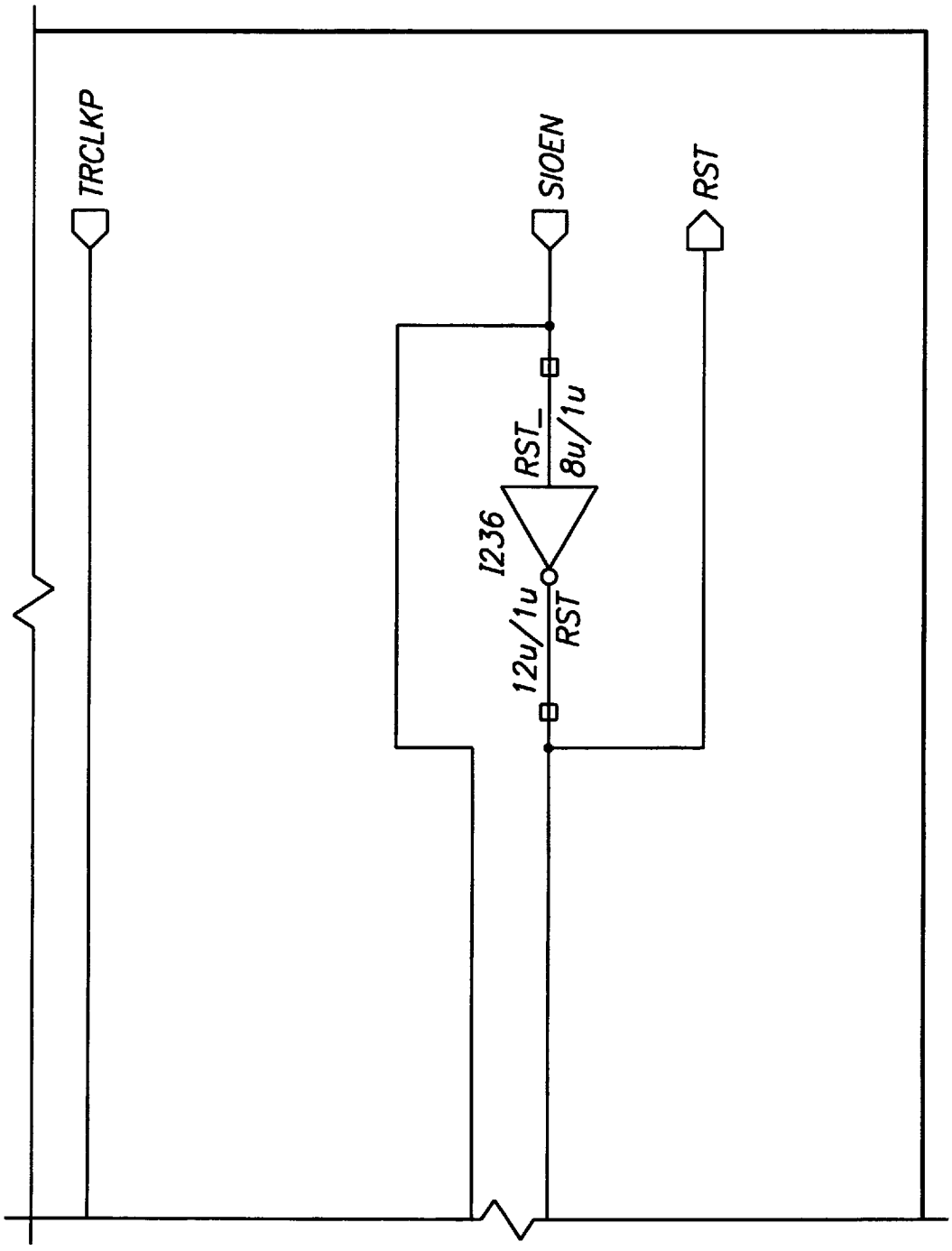


FIG 11.1400E

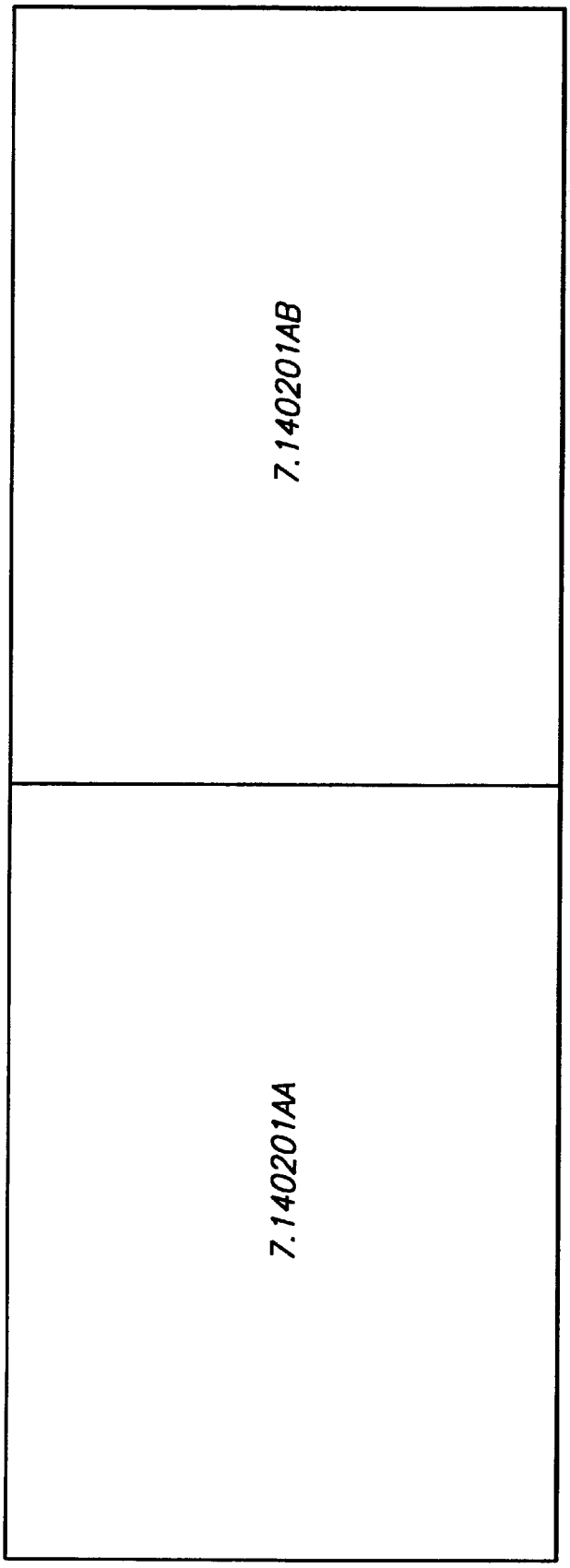


FIG. 7.140201

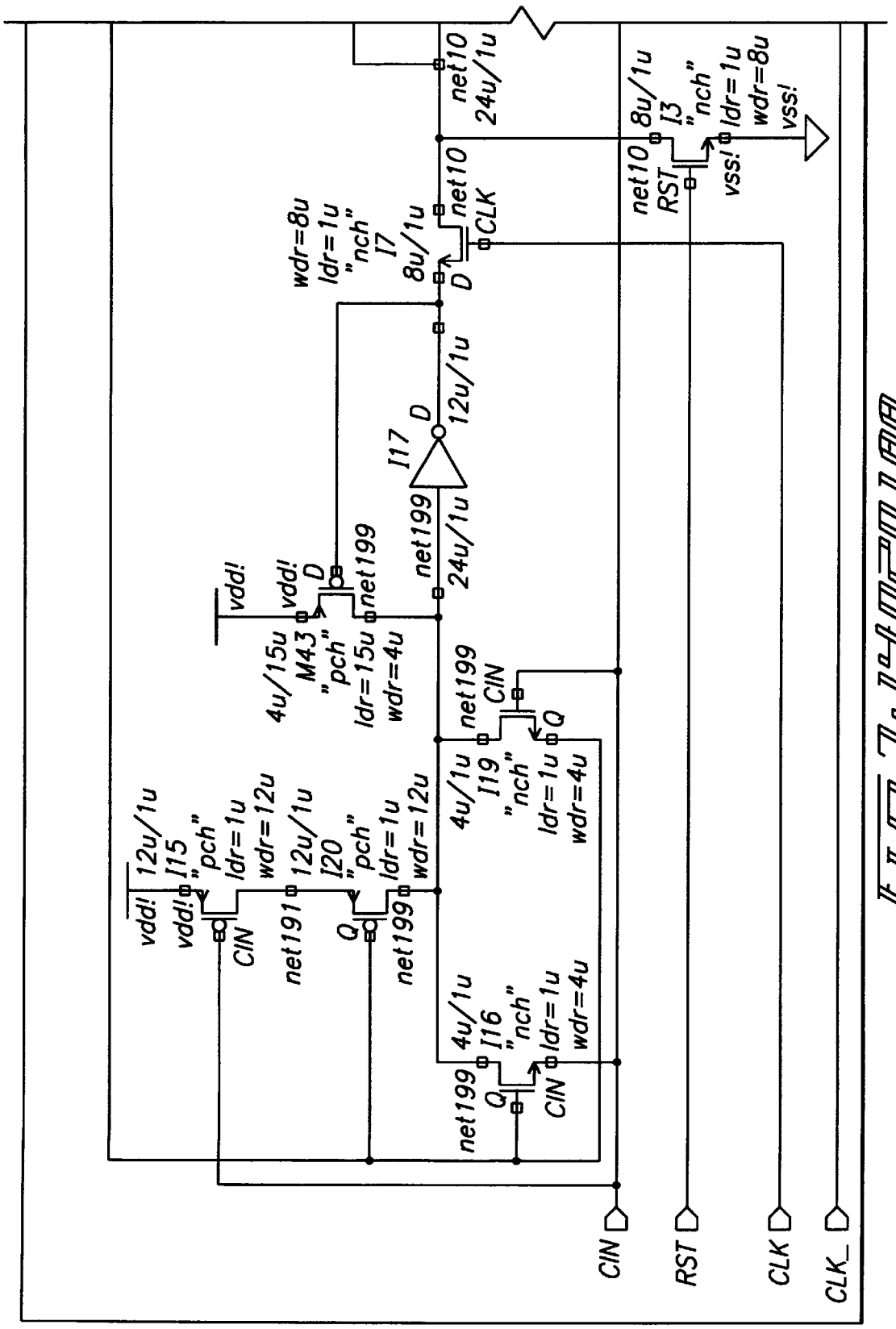

net10
24u/1u
8u/1u
I3
"nch"
ldr=1u
wdr=8u
vss!
RST
CLK
wdr=8u
ldr=1u
"nch"
I7
D
12u/1u
I17
net199
24u/1u
vdd!
M43
"pch"
4u/15u
ldr=15u
wdr=4u
CIN
Q
I19
4u/1u
I15
12u/1u
I20
I16
net191
CLK_

FIG. 1033

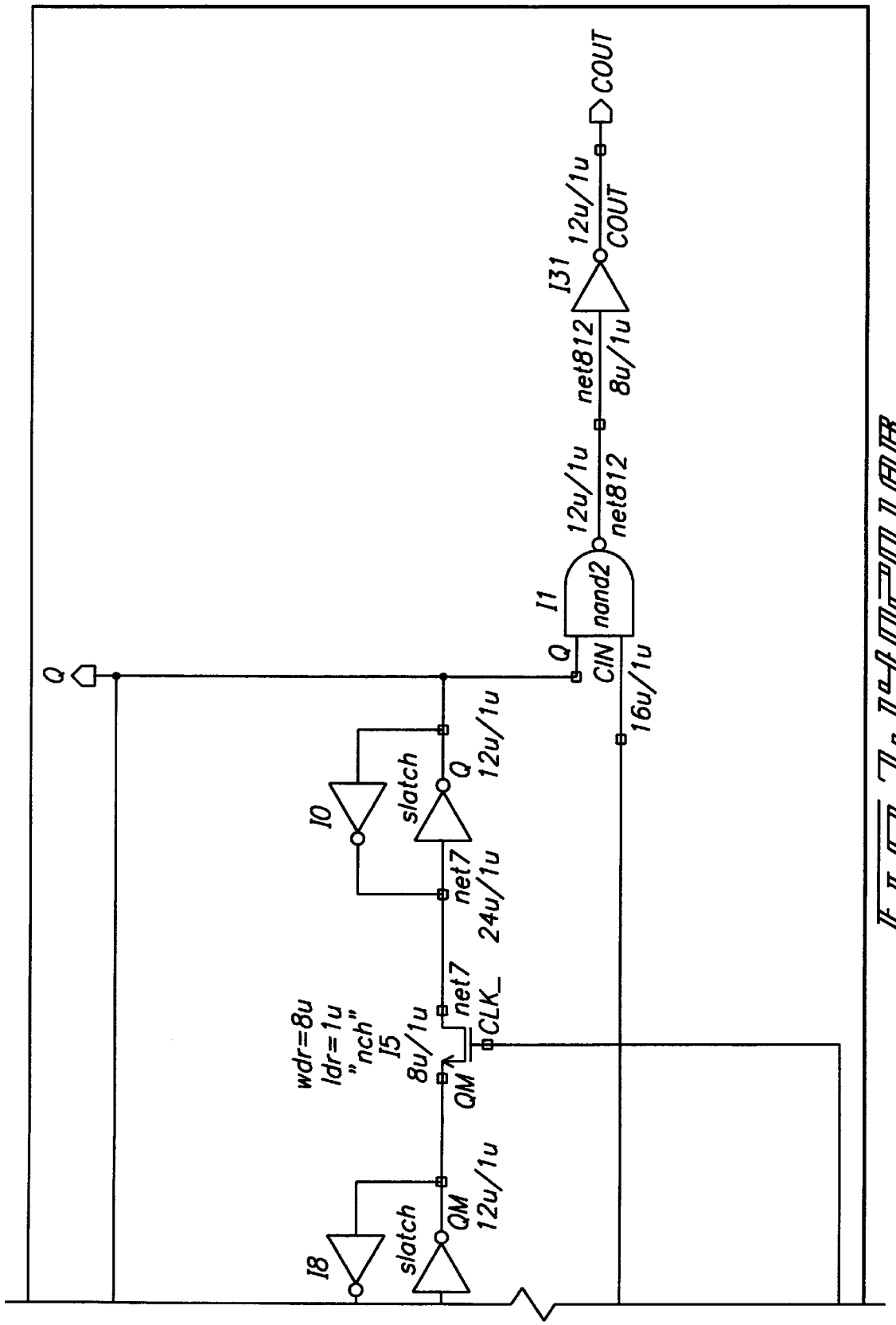


FIG. 1.1420011A1B

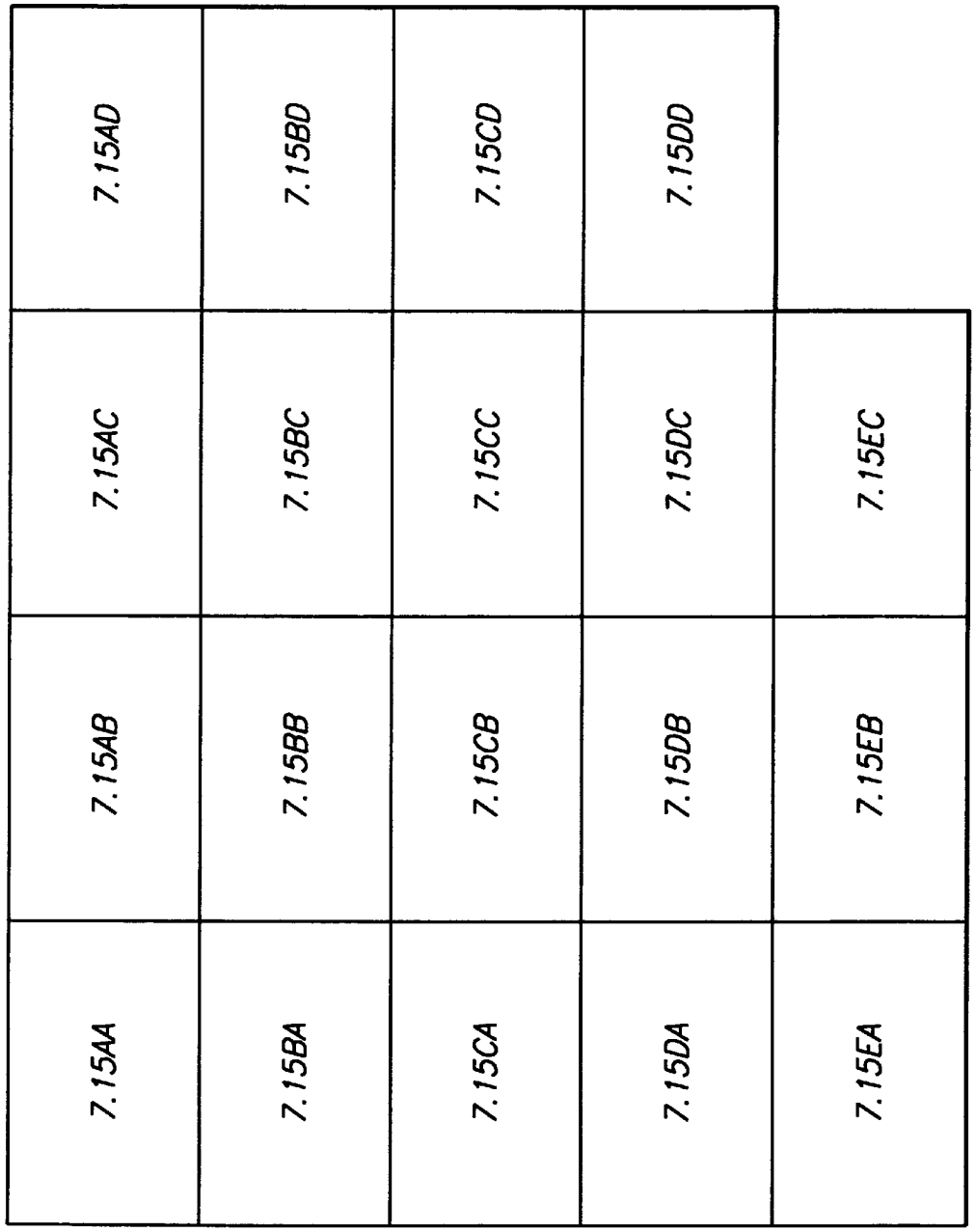
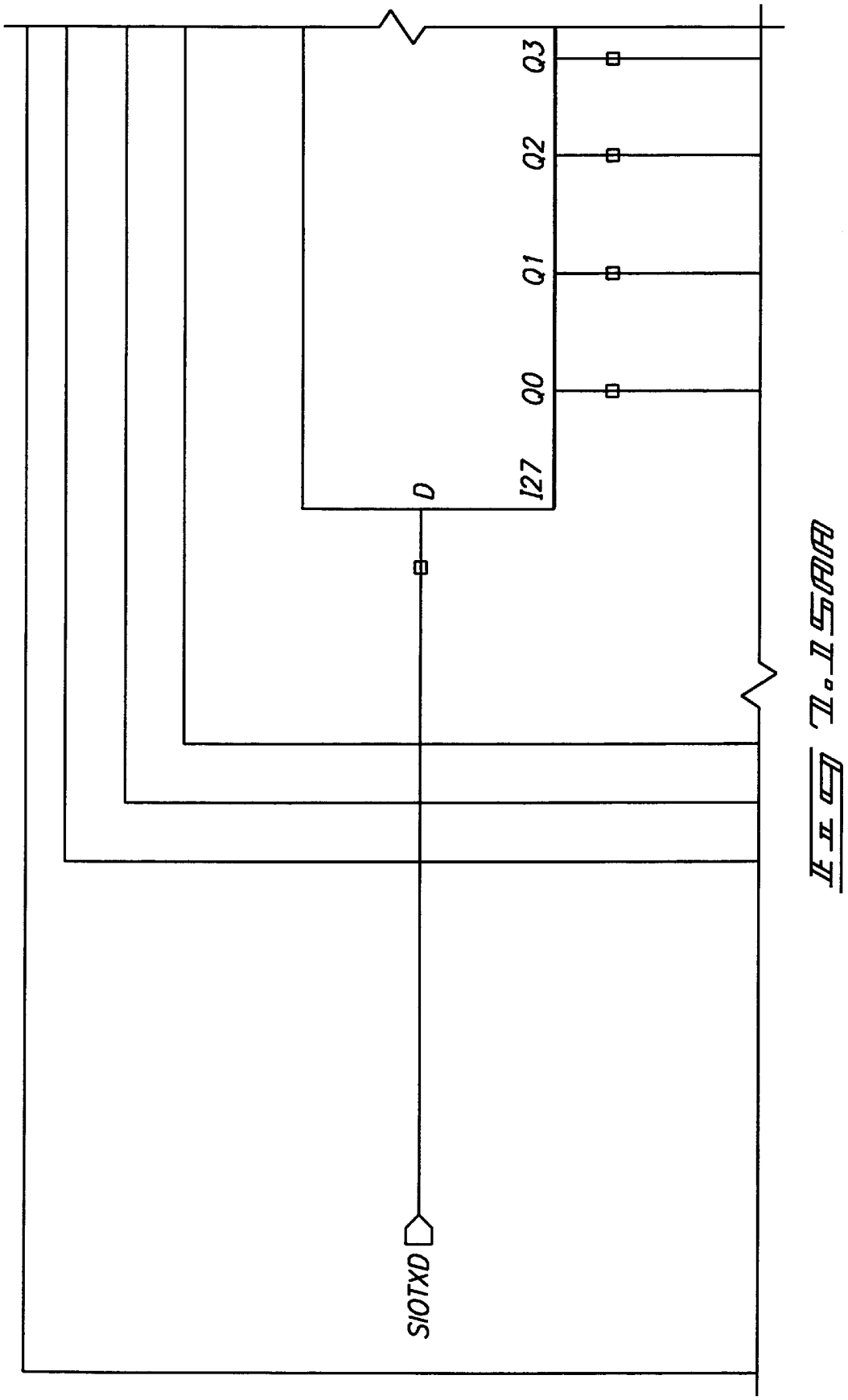
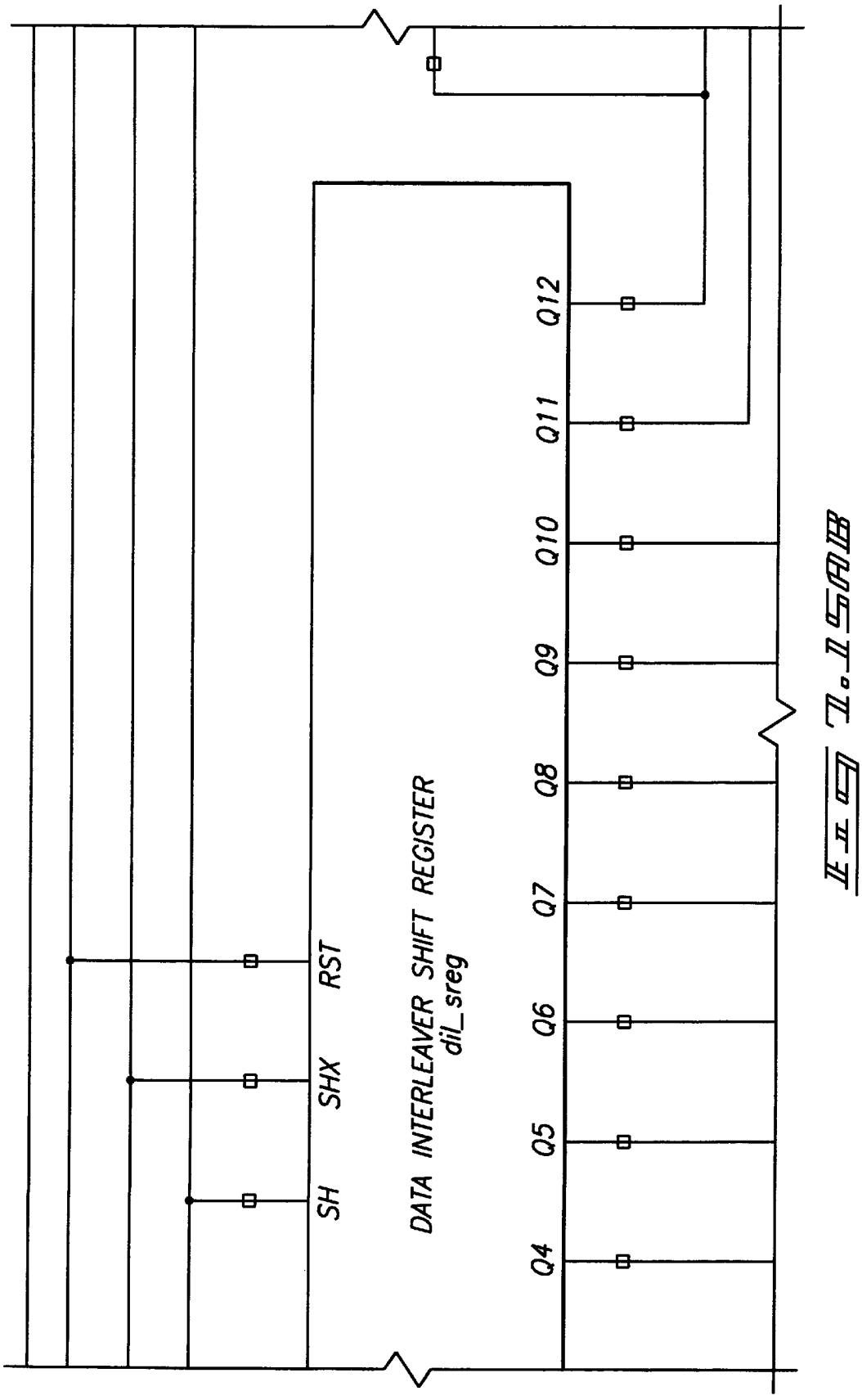

7.15AD
7.15BD
7.15CD
7.15DD
7.15AC
7.15BC
7.15CC
7.15DC
7.15EC
7.15AB
7.15BB
7.15CB
7.15DB
7.15EB
7.15AA
7.15BA
7.15CA
7.15DA
7.15EA

FIG. 7.15


Q3
Q2
Q1
Q0
I27
D
SIOTXD


RST
SHX
SH
DATA INTERLEAVER SHIFT REGISTER
dil_sreg
Q12
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4

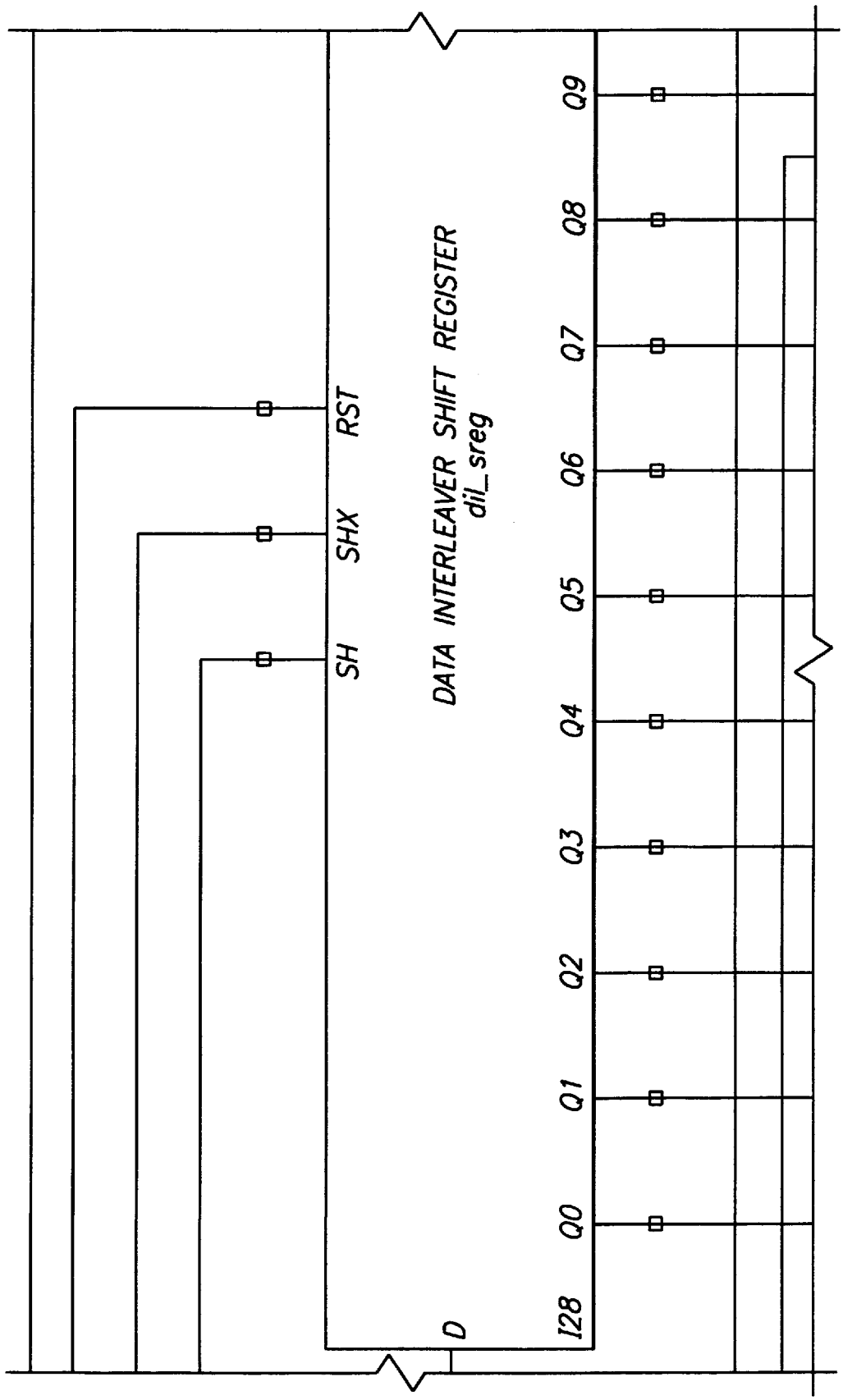
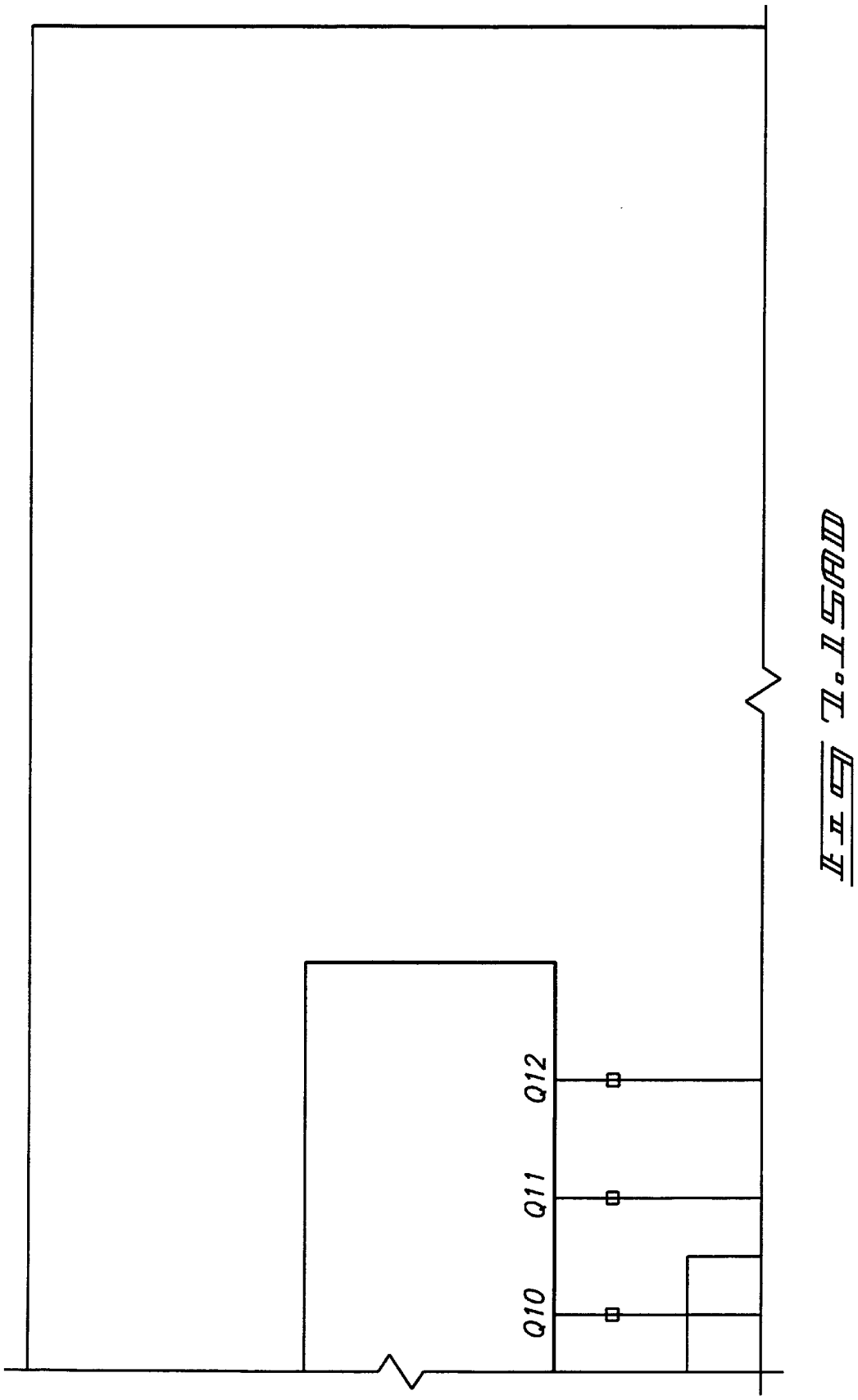

DATA INTERLEAVER SHIFT REGISTER
dil_sreg
RST
SHX
SH
D
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
128

FIG. 1151


Q12
Q11
Q10
FIG 11.1SAD

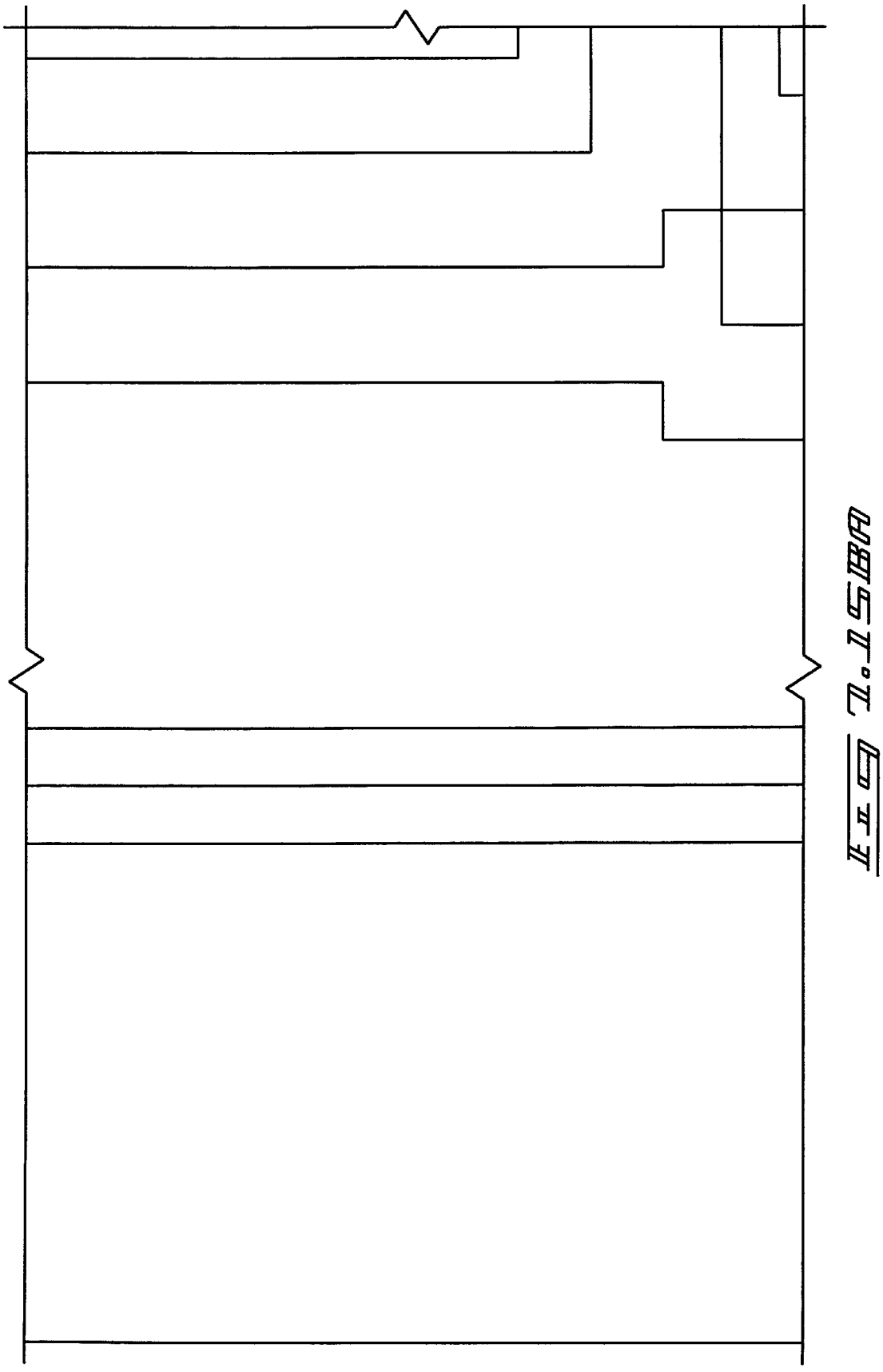


FIG. 11.5BA

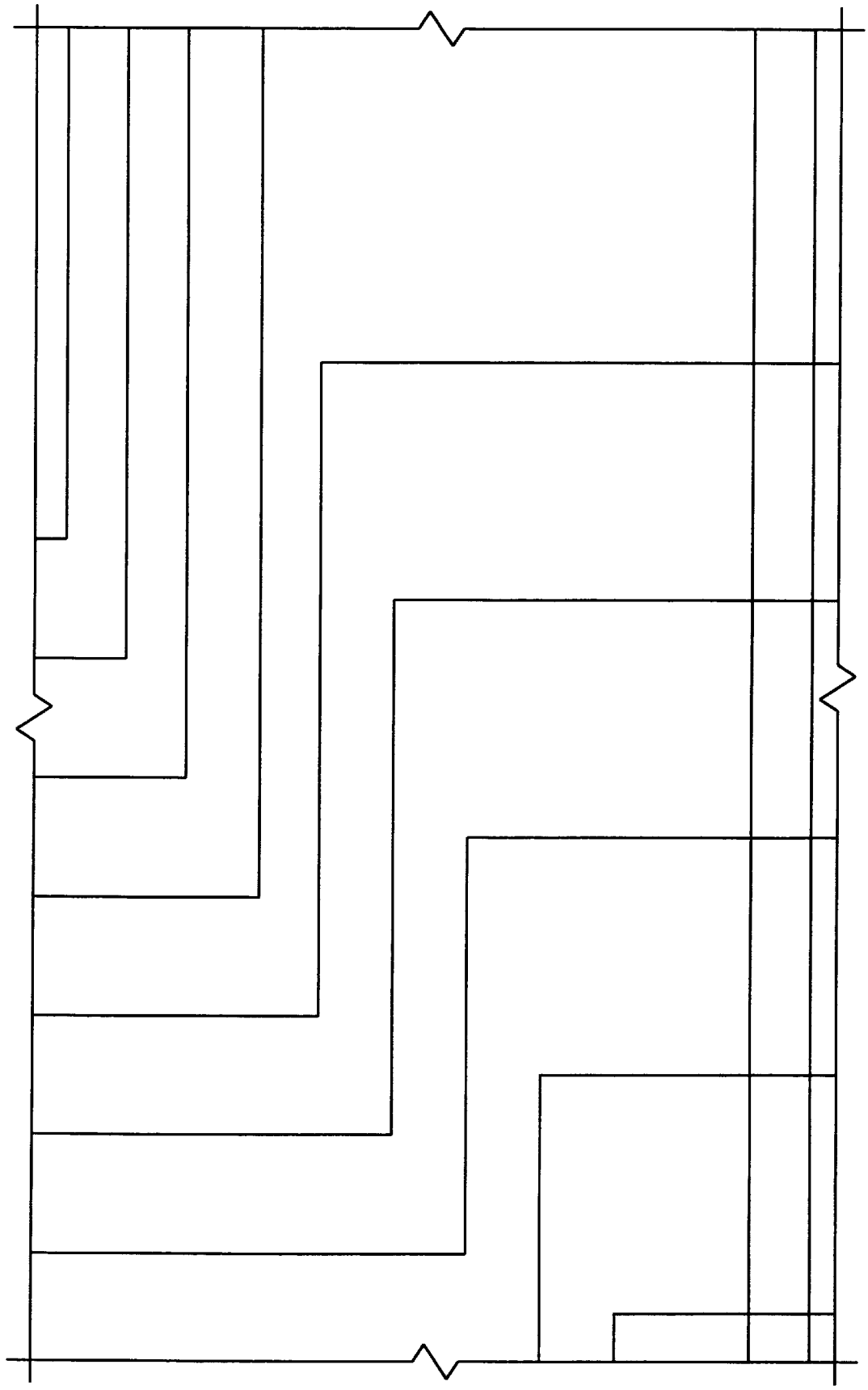


FIG. 1041

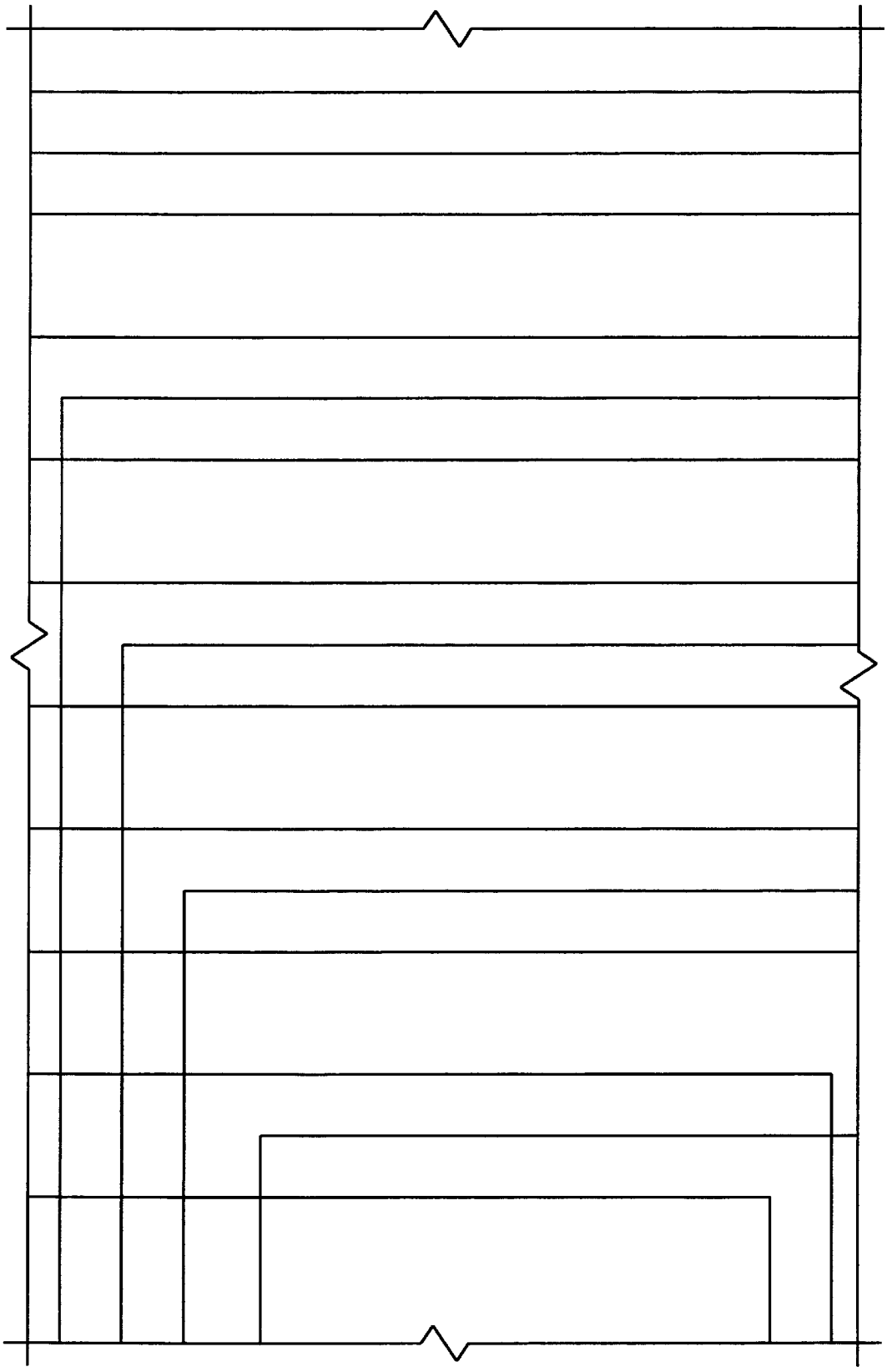


FIG. 1042

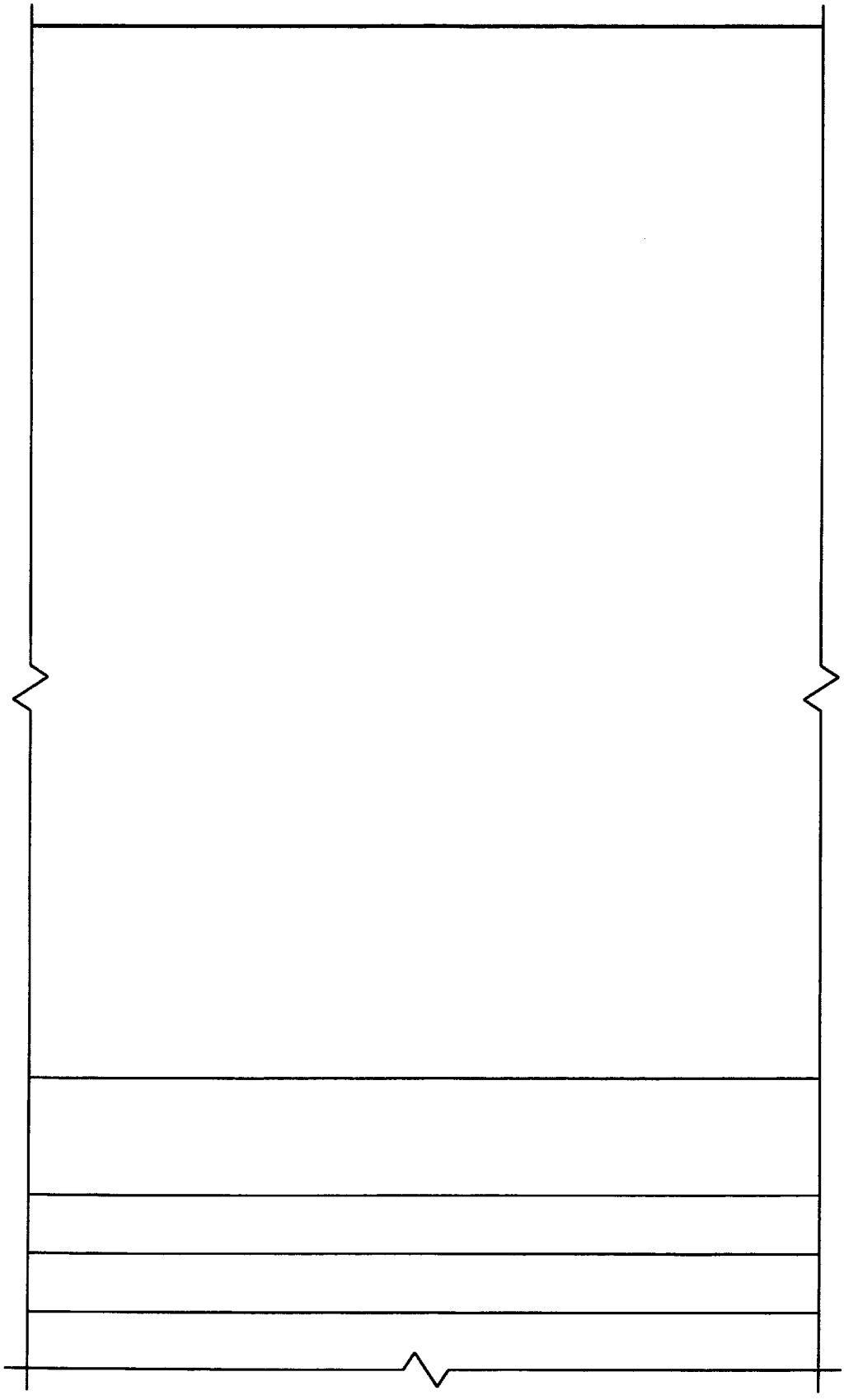


FIG. 1,580

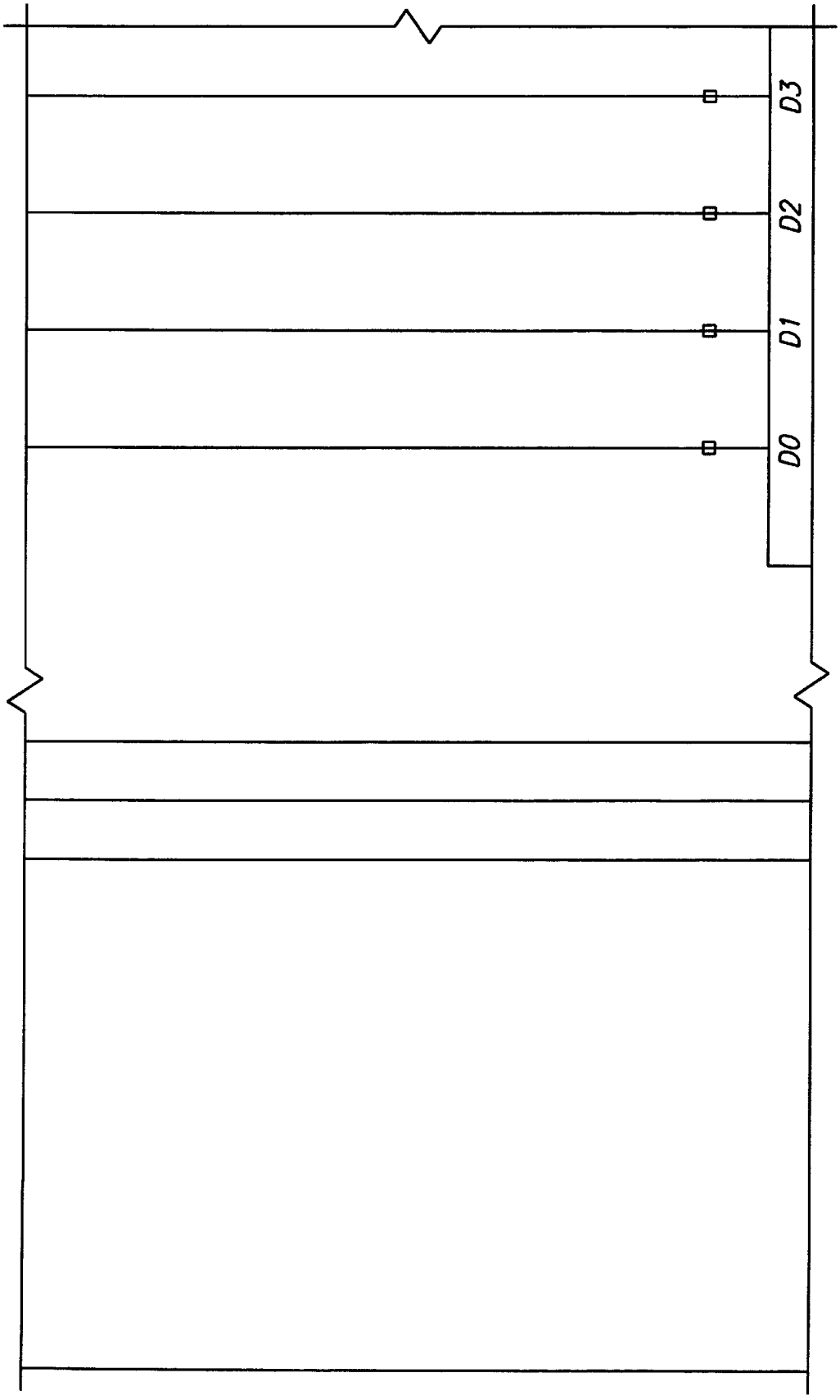
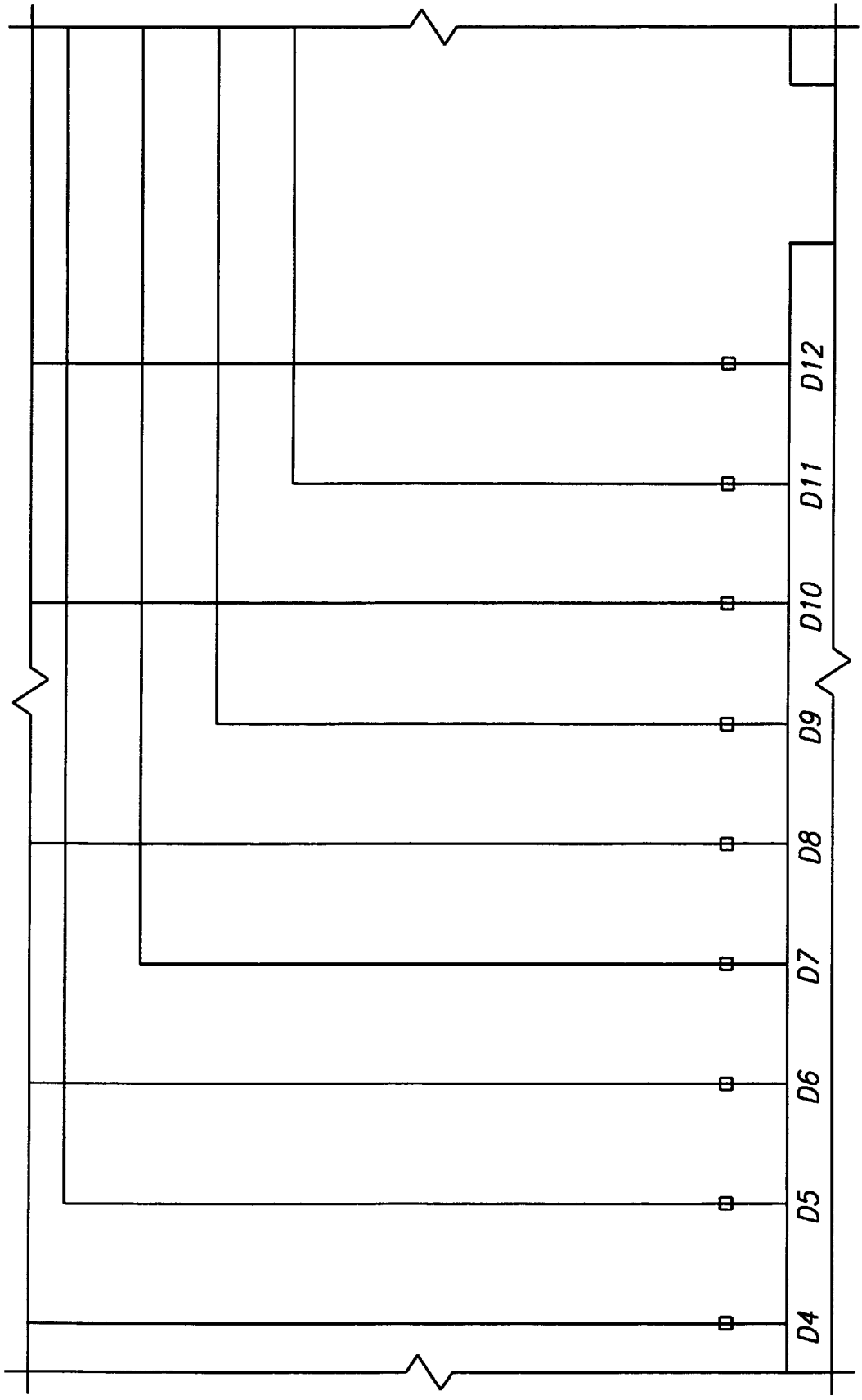
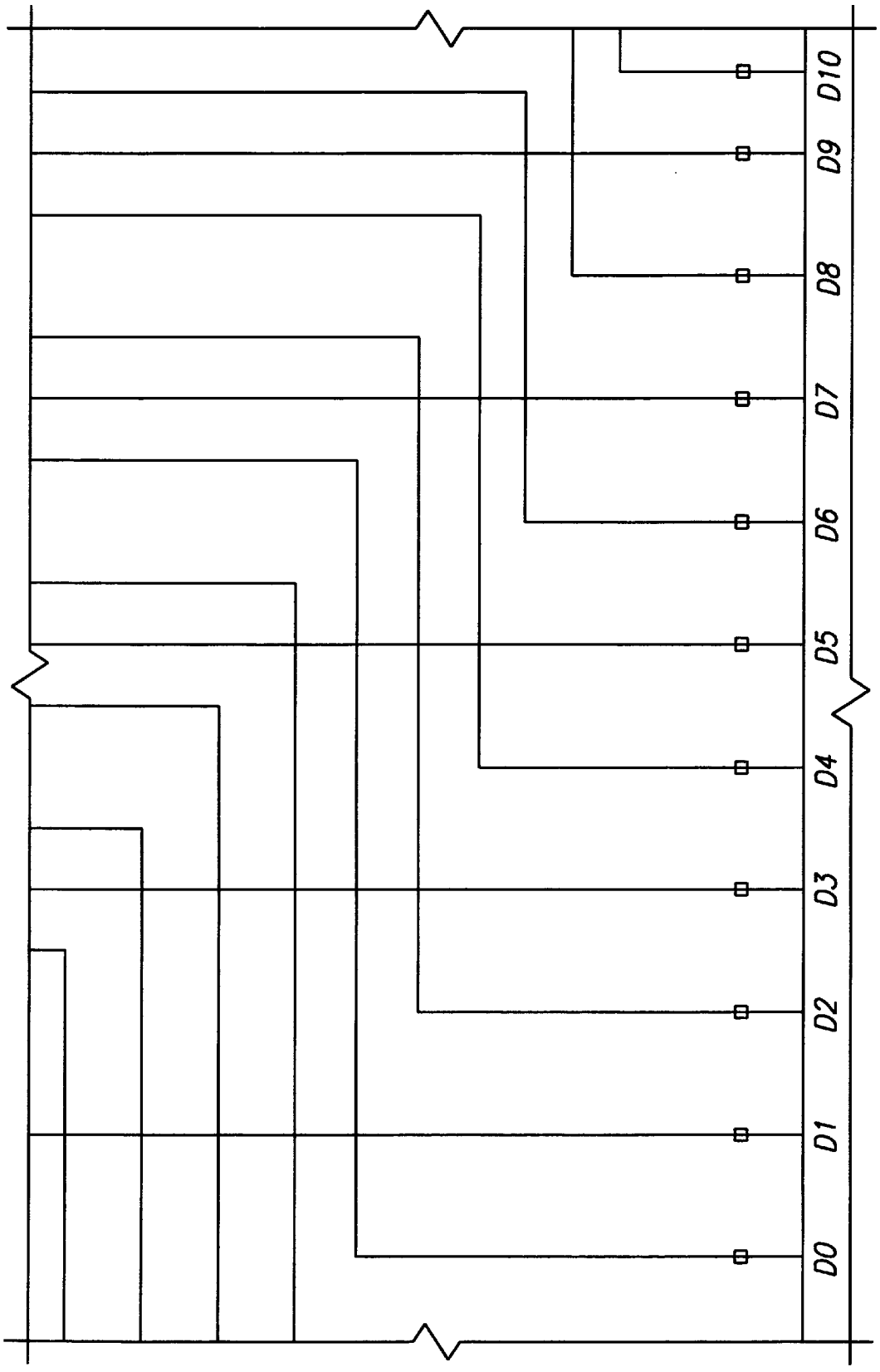


FIG. 1044



ФИГ. 1045



ФИГ. 1045

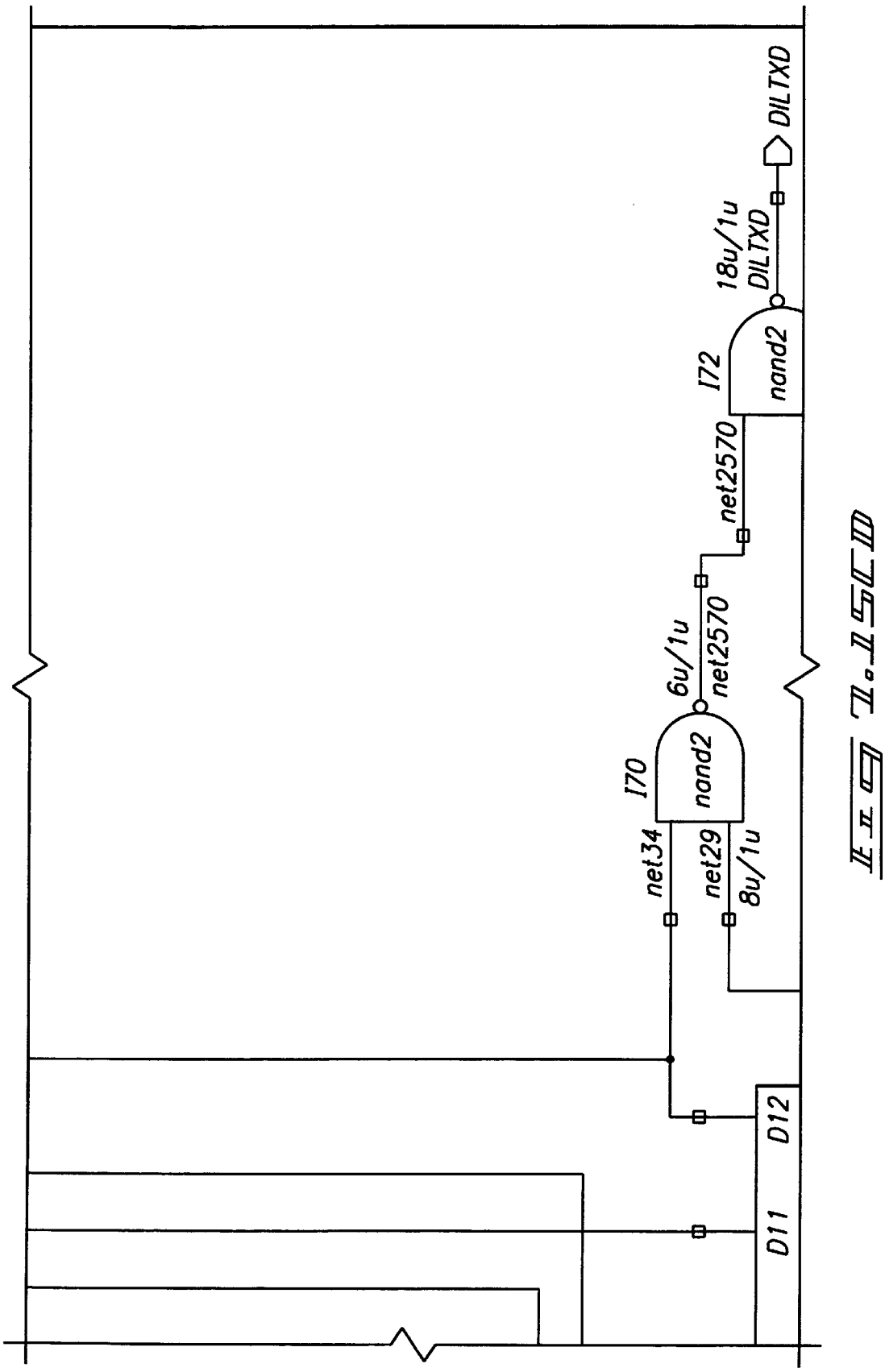

DILTXD
18u/1u
DILTXD
I72
nand2
net2570
net2570
6u/1u
I70
nand2
net34
net29
8u/1u
D12
D11

FIG. 1057

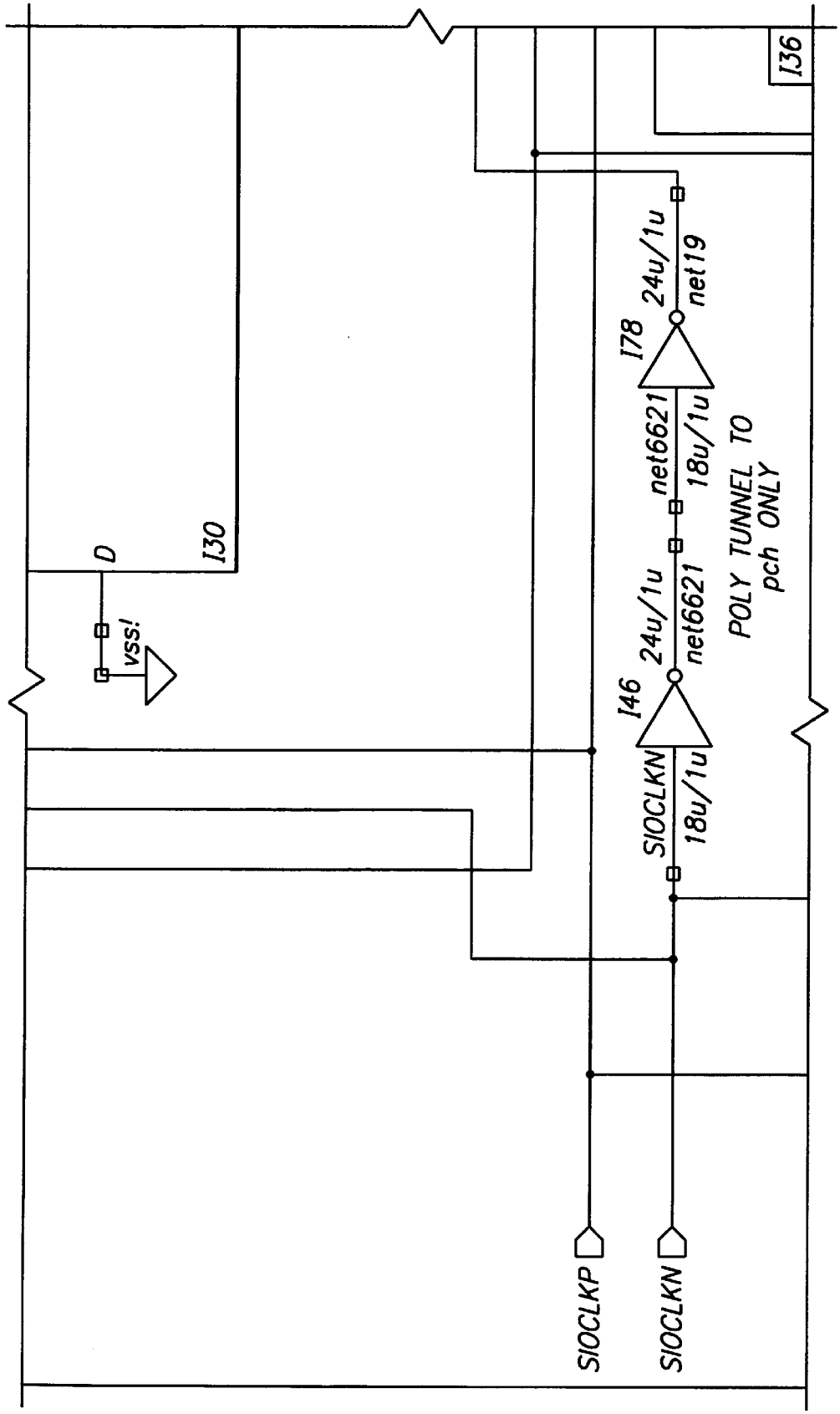

I36
I78
24u/1u
net19
net6621
18u/1u
POLY TUNNEL TO
pch ONLY
I46
24u/1u
net6621
SIOCLKN
18u/1u
I30
D
vss!
SIOCLKP
SIOCLKN

FIG. 11.5DDA

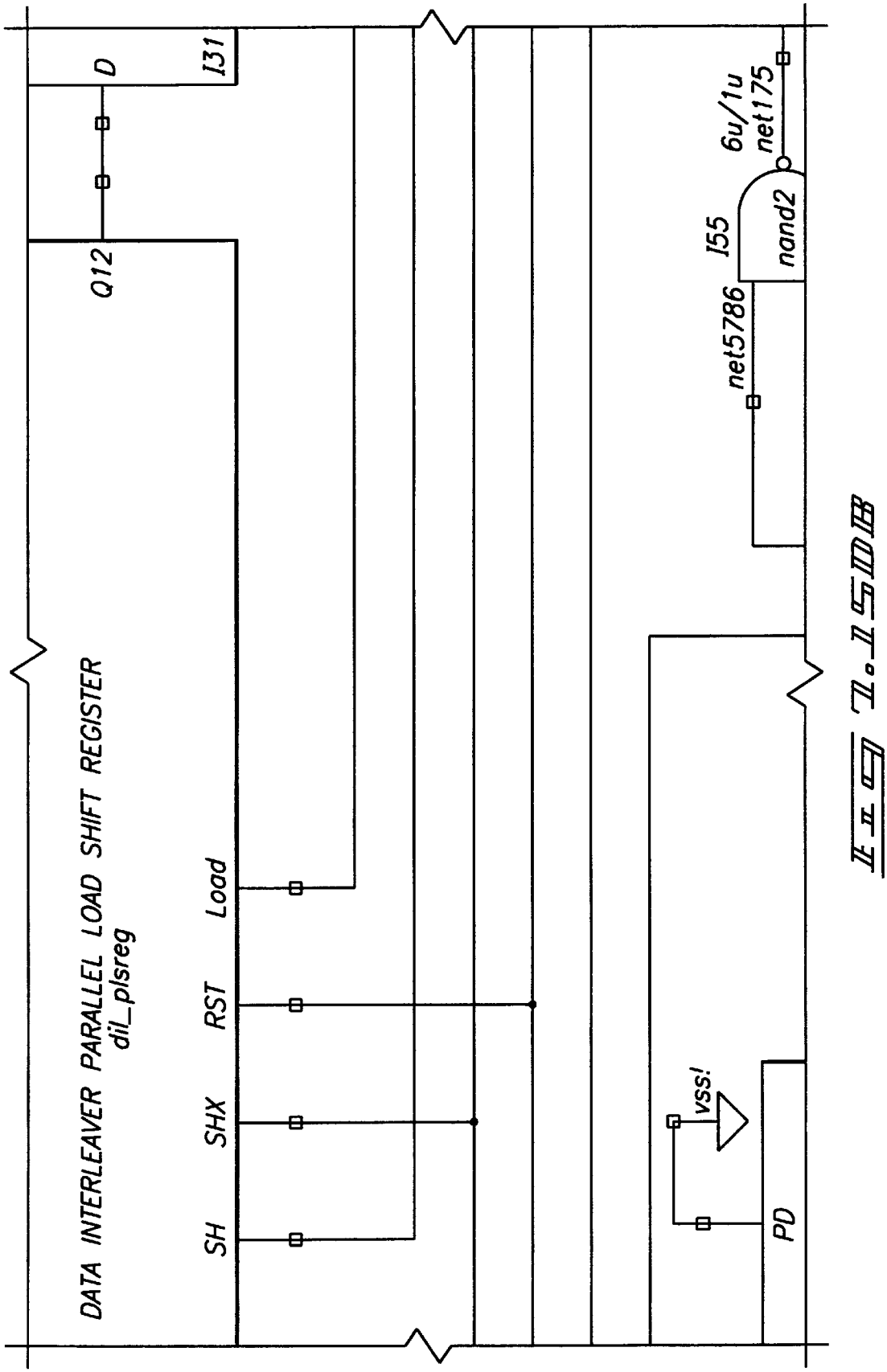

DATA INTERLEAVER PARALLEL LOAD SHIFT REGISTER
dil_plsreg
SH
SHX
RST
Load
Q12
D
I31
I55
nand2
net5786
6u/1u
net175
vss!
PD

FIG. 1150

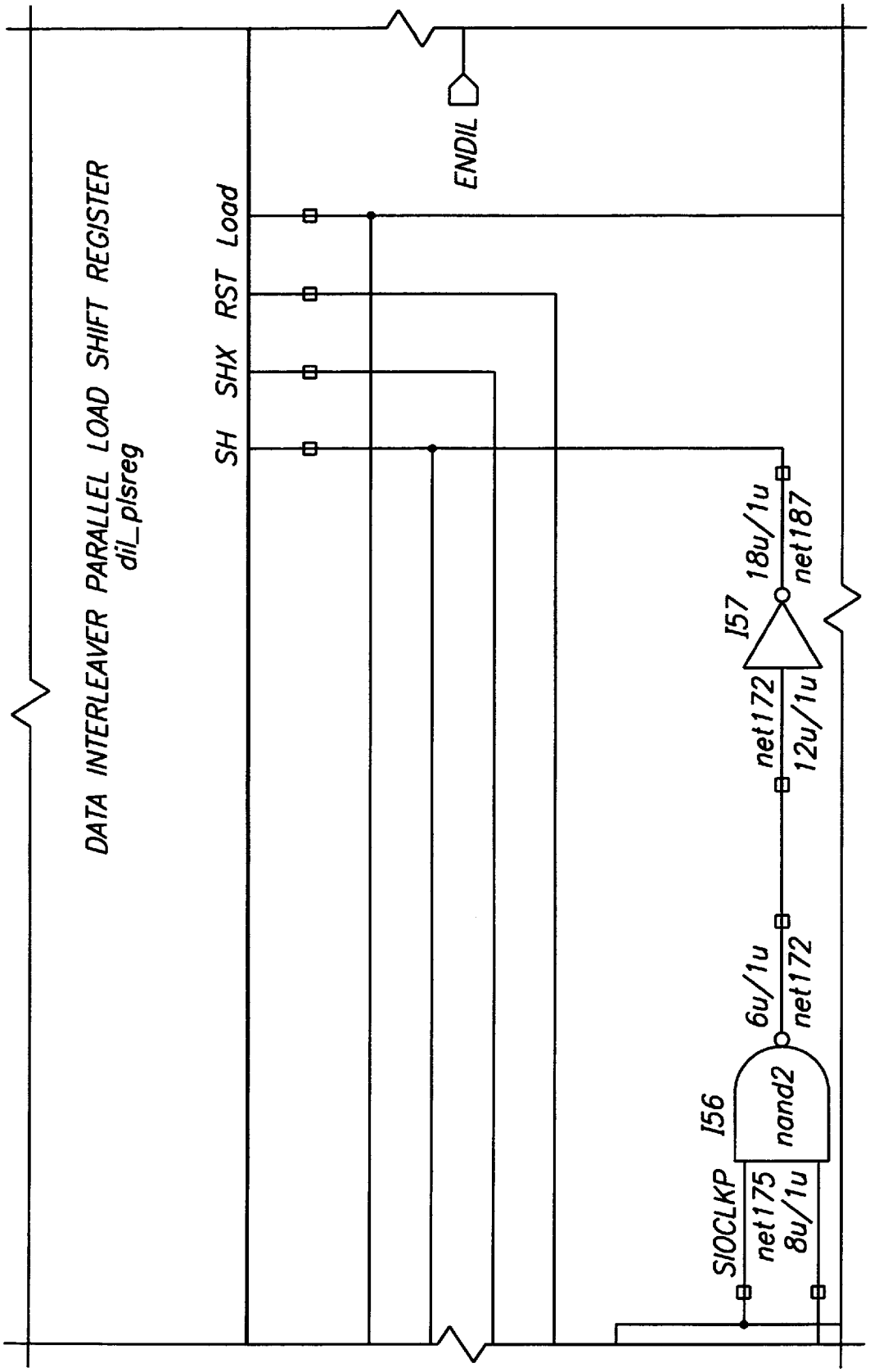

DATA INTERLEAVER PARALLEL LOAD SHIFT REGISTER
dil_plsreg
SH SHX RST Load
ENDIL
I57
18u/1u
net187
net172
12u/1u
6u/1u
net172
I56
nand2
SIOCLKP
net175
8u/1u

FIG. 1150

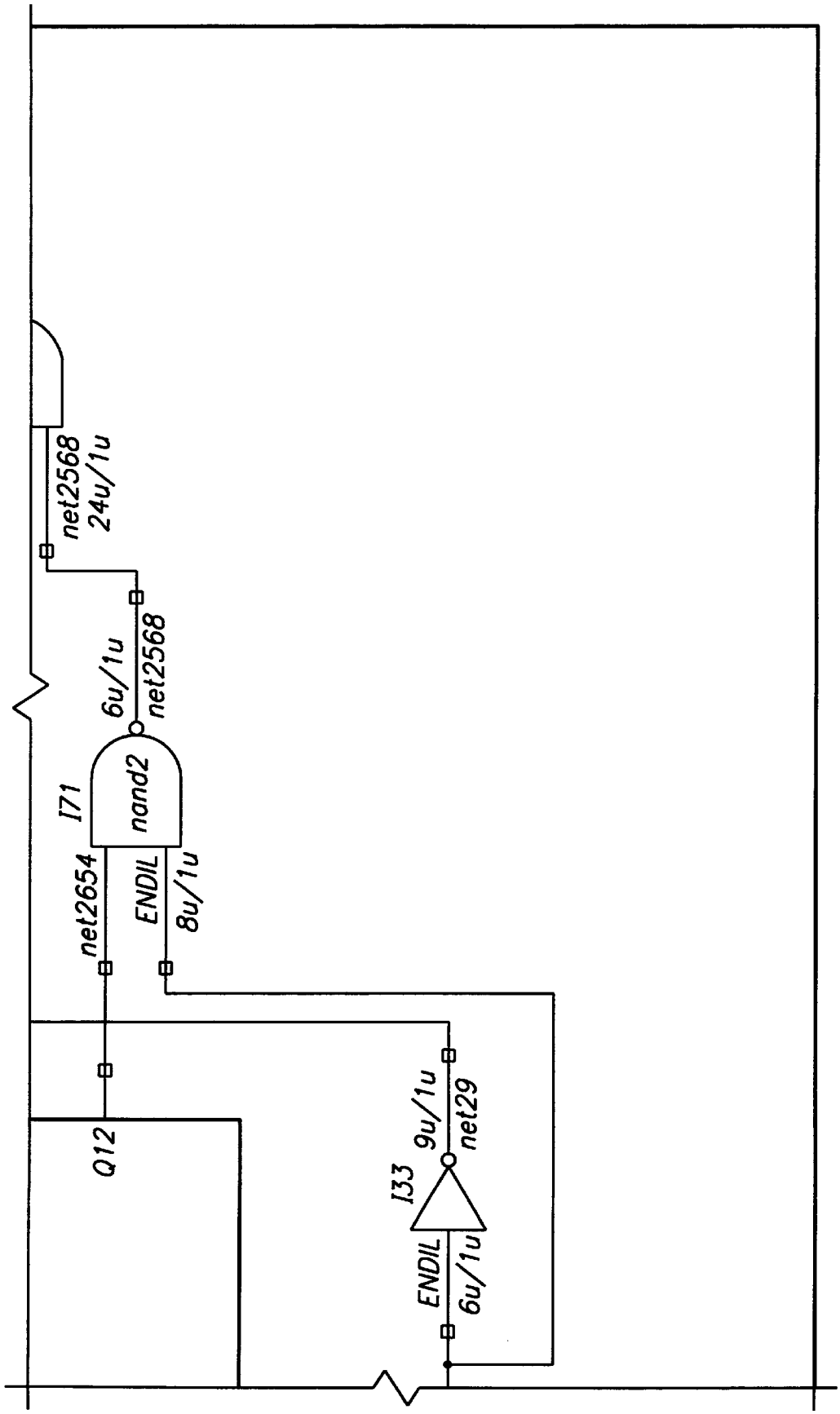

net2568
24u/1u
6u/1u
net2568
I71
nand2
net2654
ENDIL
8u/1u
Q12
I33
9u/1u
net29
ENDIL
6u/1u

FIG. 1151

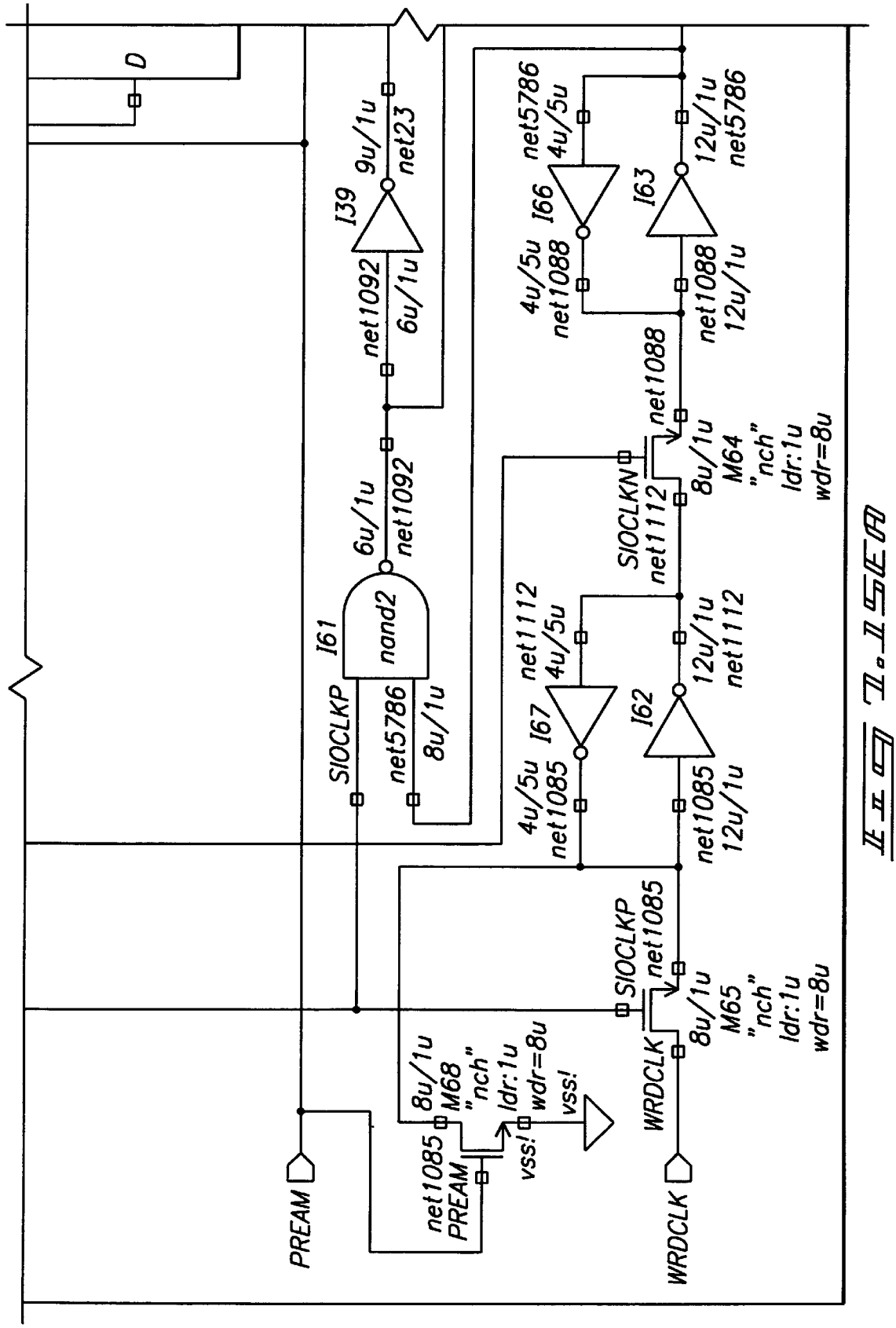

D
I39
9u/1u
net23
net1092
6u/1u
I61
nand2
6u/1u
net1092
SIOCLKP
net5786
8u/1u
I66
net5786
4u/5u
4u/5u
net1088
I63
12u/1u
net5786
net1088
12u/1u
net1088
SIOCLKN
net1112
8u/1u
M64
"nch"
ldr:1u
wdr=8u
I67
net1112
4u/5u
4u/5u
net1085
I62
12u/1u
net1112
net1085
12u/1u
SIOCLKP
net1085
8u/1u
M65
"nch"
ldr:1u
wdr=8u
WRDCLK
PREAM
8u/1u
M68
"nch"
ldr:1u
wdr=8u
vss!
net1085
PREAM
vss!
WRDCLK

FIG. 1.1564

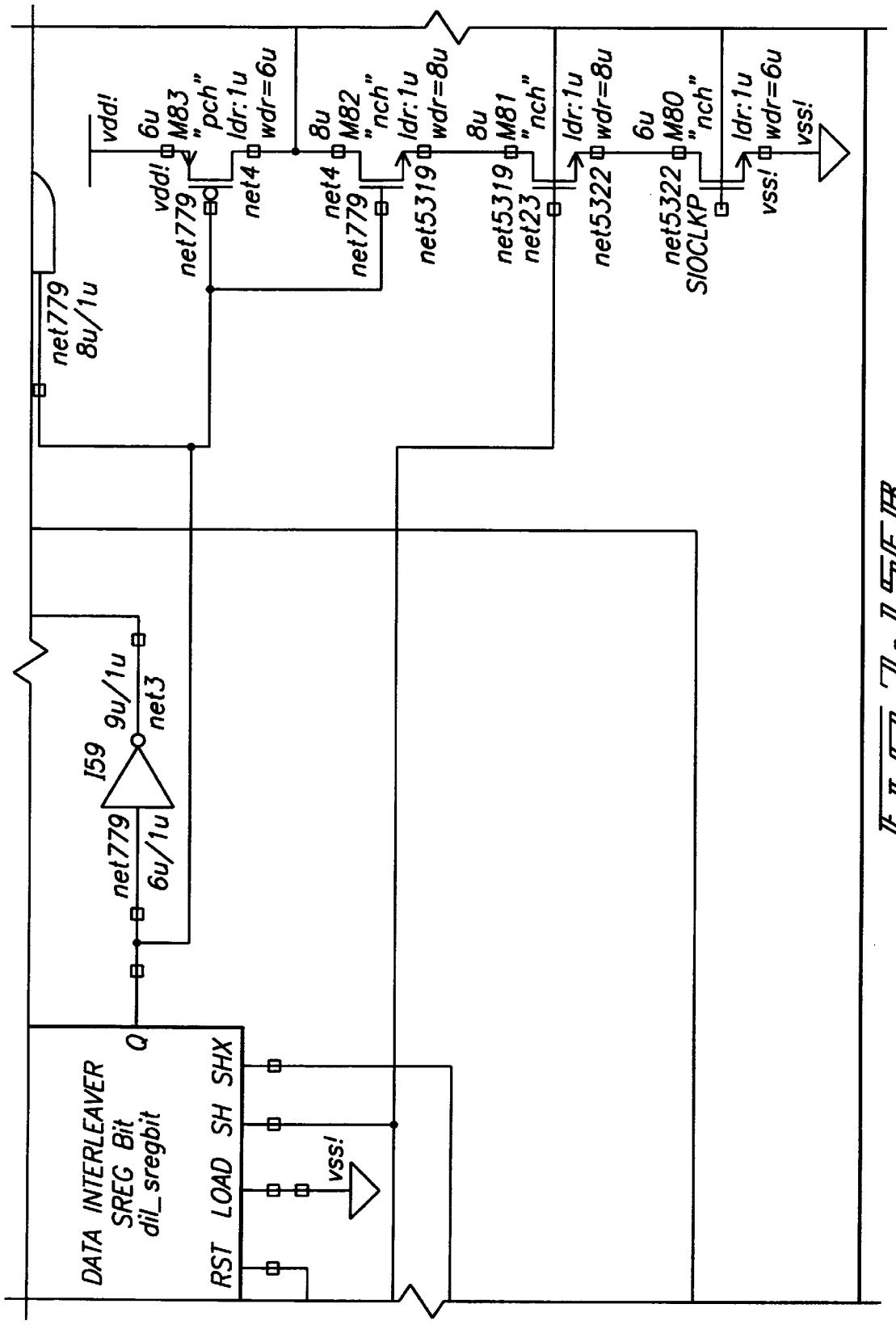

vdd!
6u
M83
"pch"
ldr:1u
wdr=6u
net4
net779
8u
M82
"nch"
ldr:1u
wdr=8u
net5319
net23
M81
net5322
M80
SIOCLKP
vss!
net779
8u/1u
I59
9u/1u
net3
6u/1u
DATA INTERLEAVER
SREG Bit
dil_sregbit
Q
RST
LOAD
SH
SHX

FIG. 11.1558

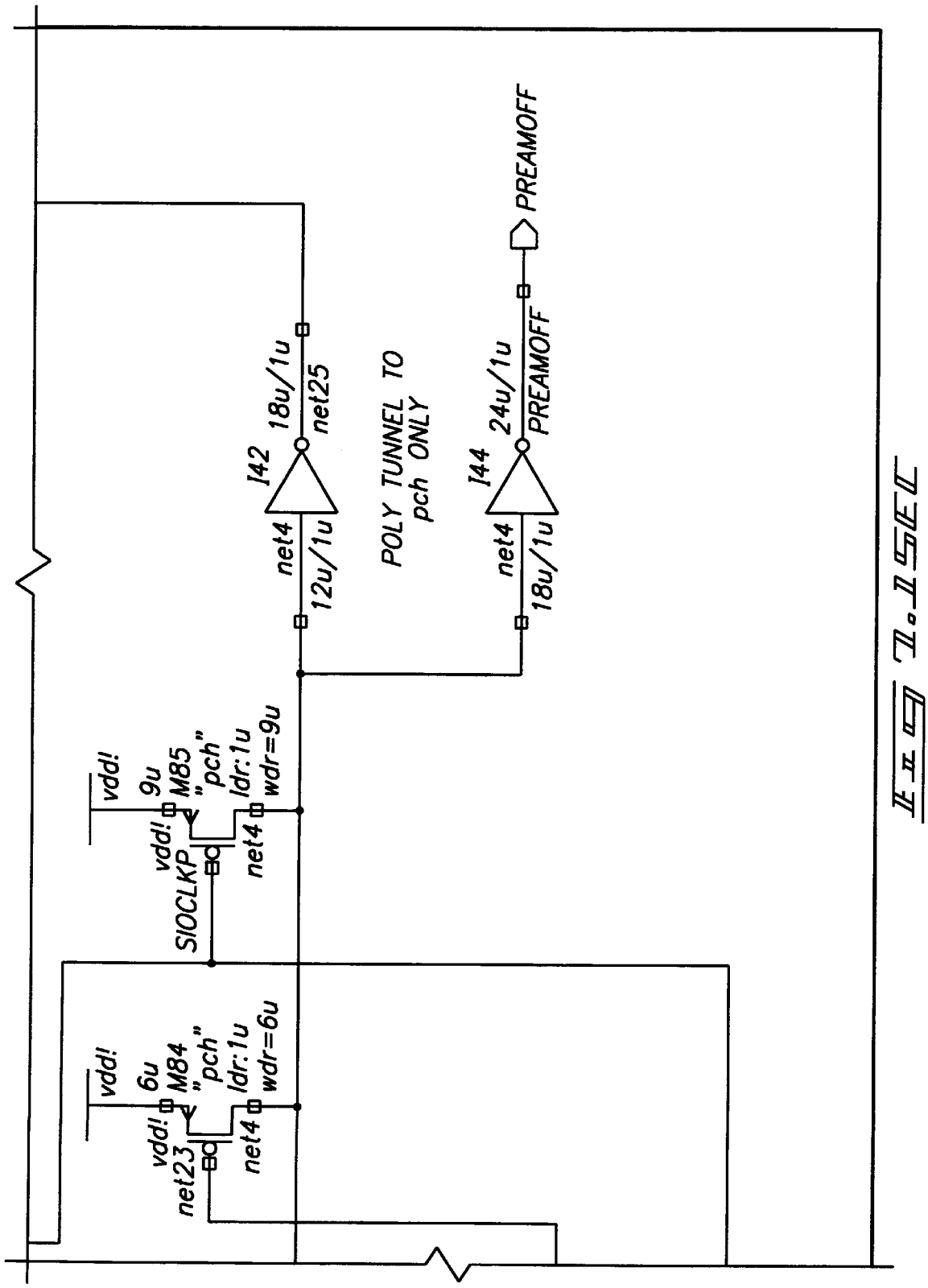


FIG. 11.1351
PREAMOFF
I44 24u/1u
PREAMOFF
net4
18u/1u
POLY TUNNEL TO
pch ONLY
I42 18u/1u
net25
net4
12u/1u
vdd!
9u
M85
"pch"
ldr:1u
wdr=9u
vdd!
SIOCLKP
net4
vdd!
6u
M84
"pch"
ldr:1u
wdr=6u
vdd!
net23
net4

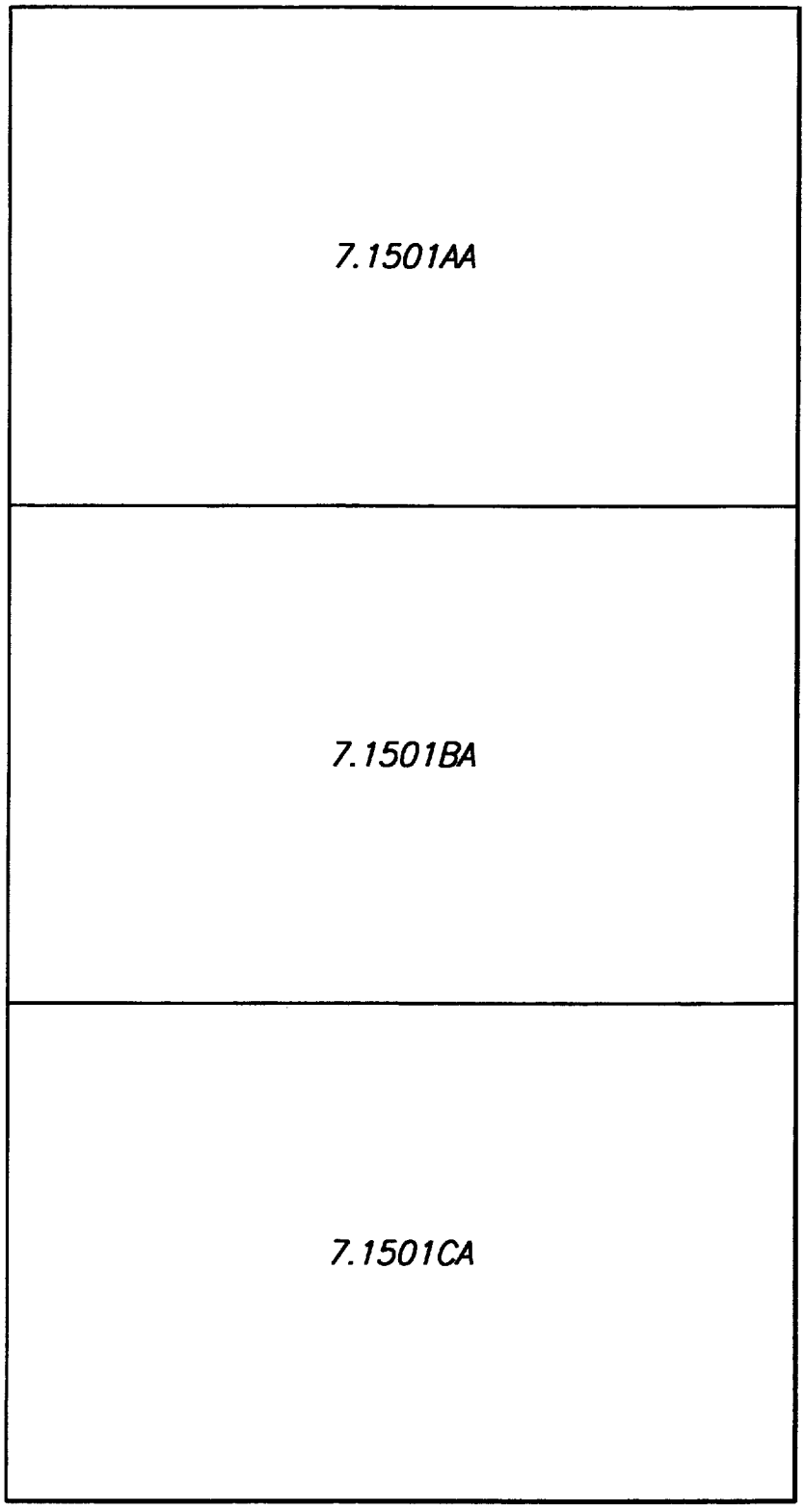


Fig 7.1501

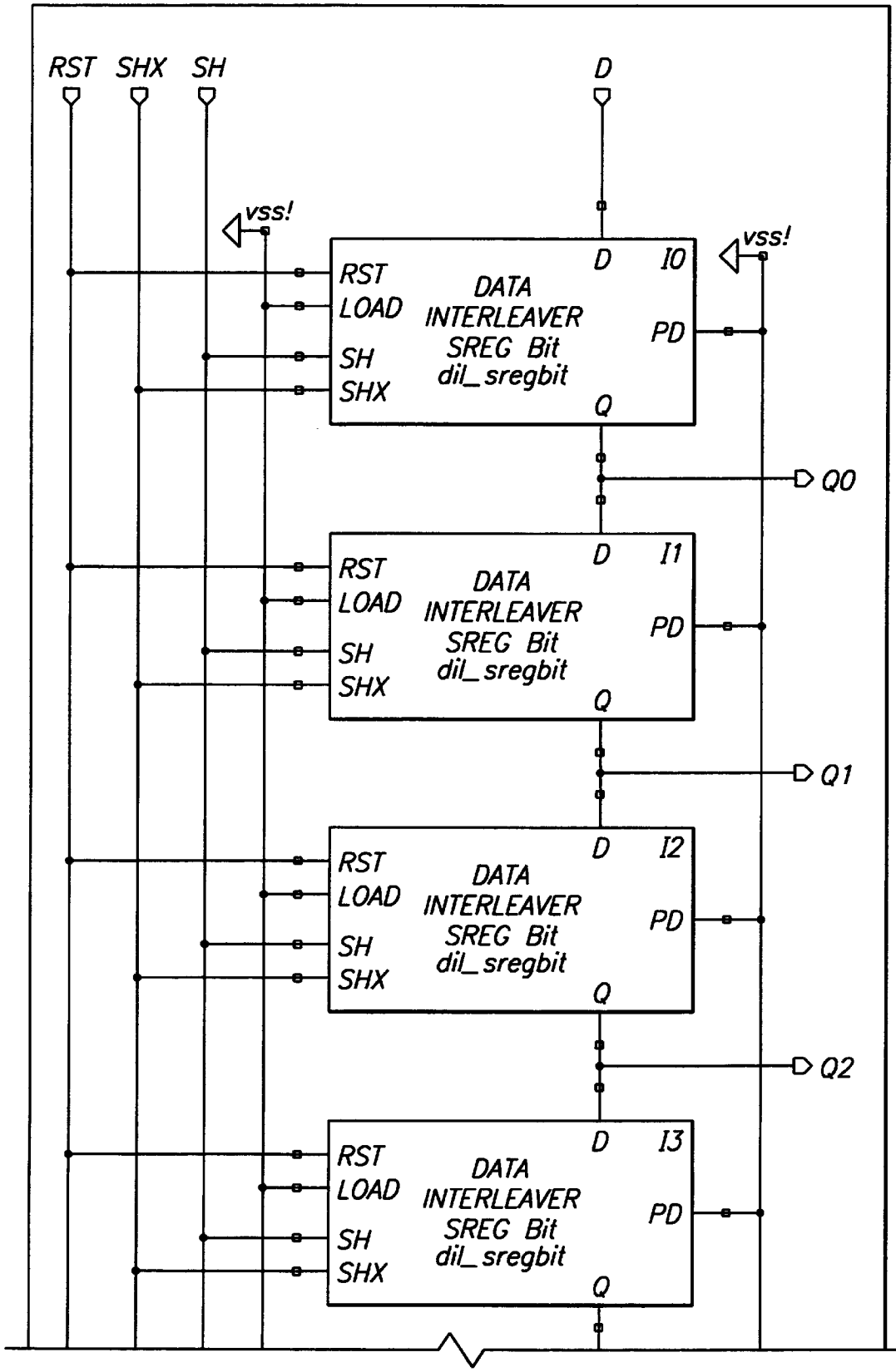

RST
SHX
SH
D
vss!
vss!
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
D
I0
PD
Q
Q0
I1
Q1
I2
Q2
I3

Fig 1.150AA

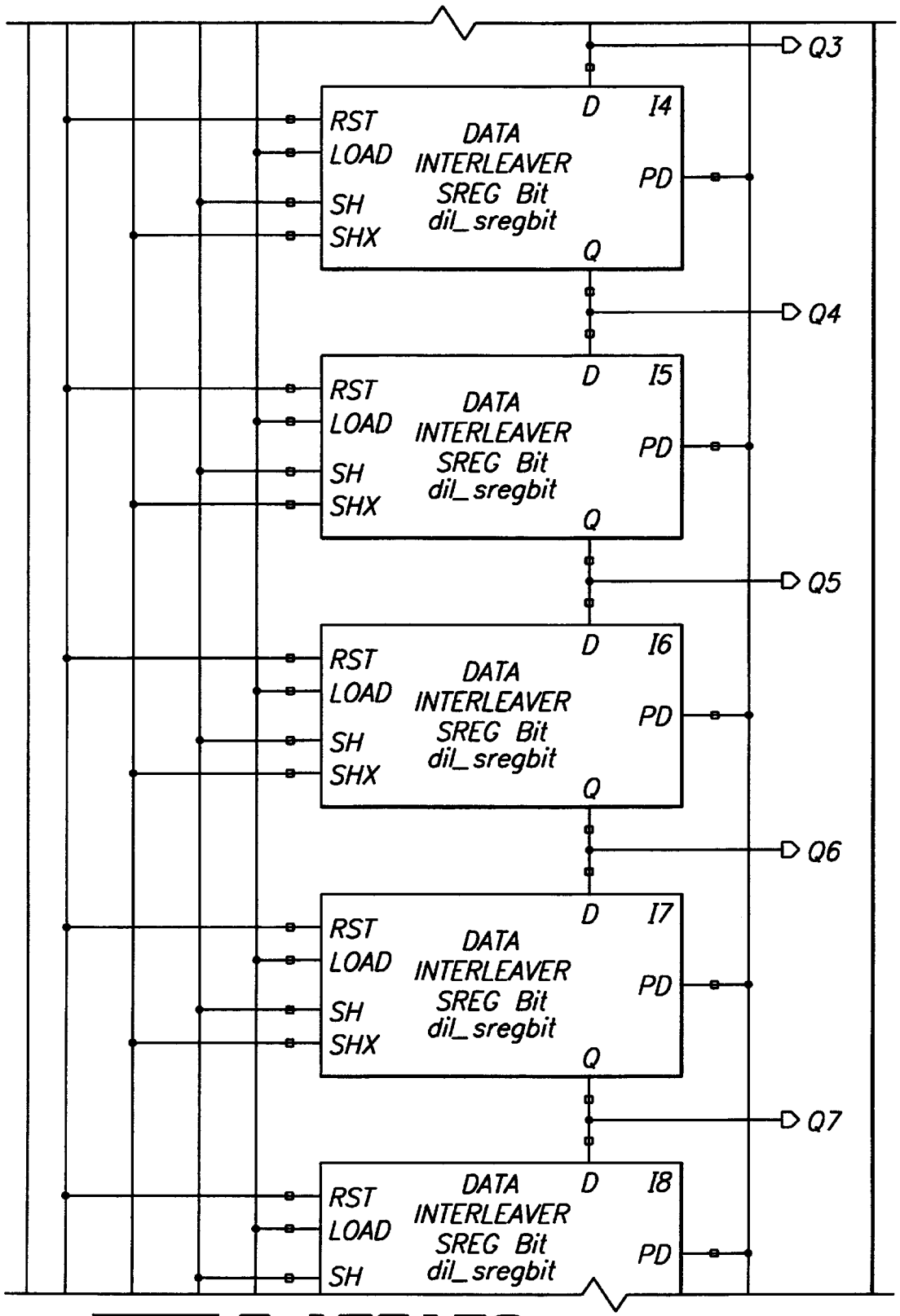


Fig 1.150118A

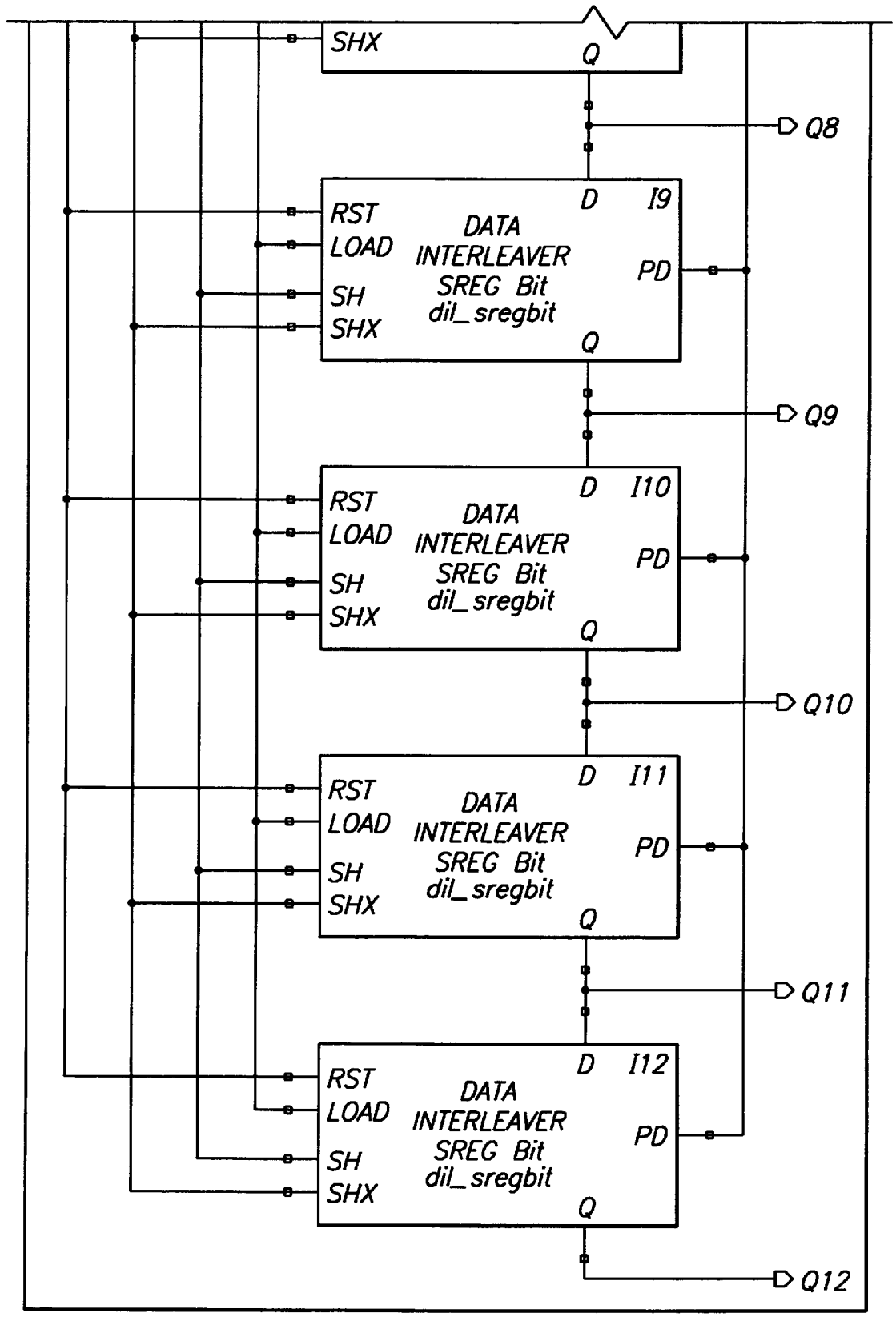

SHX
Q
Q8
D
I9
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
Q
Q9
D
I10
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
Q
Q10
D
I11
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
Q
Q11
D
I12
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
Q
Q12

Fig 1.1501CA

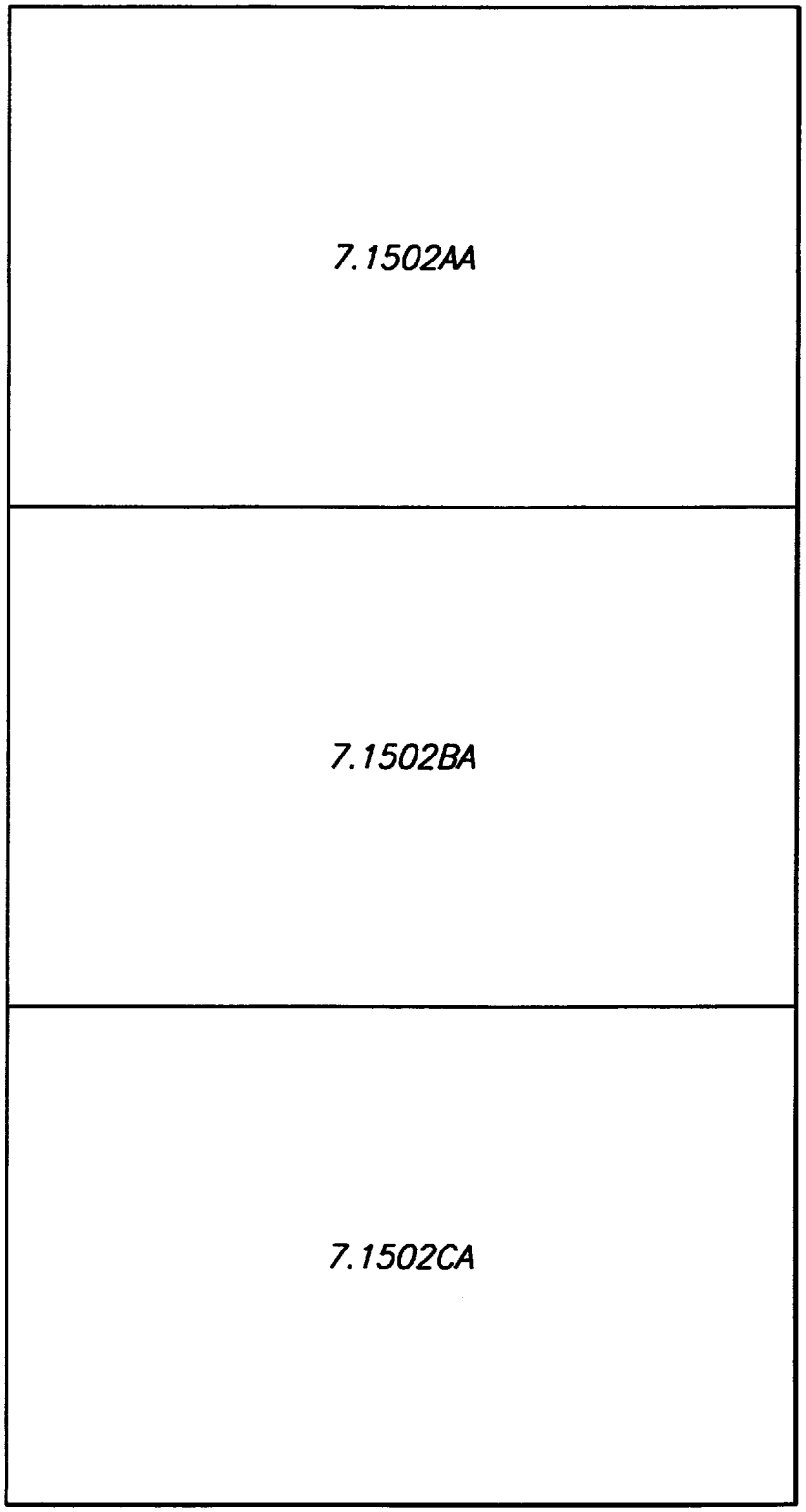


Fig 7.1502

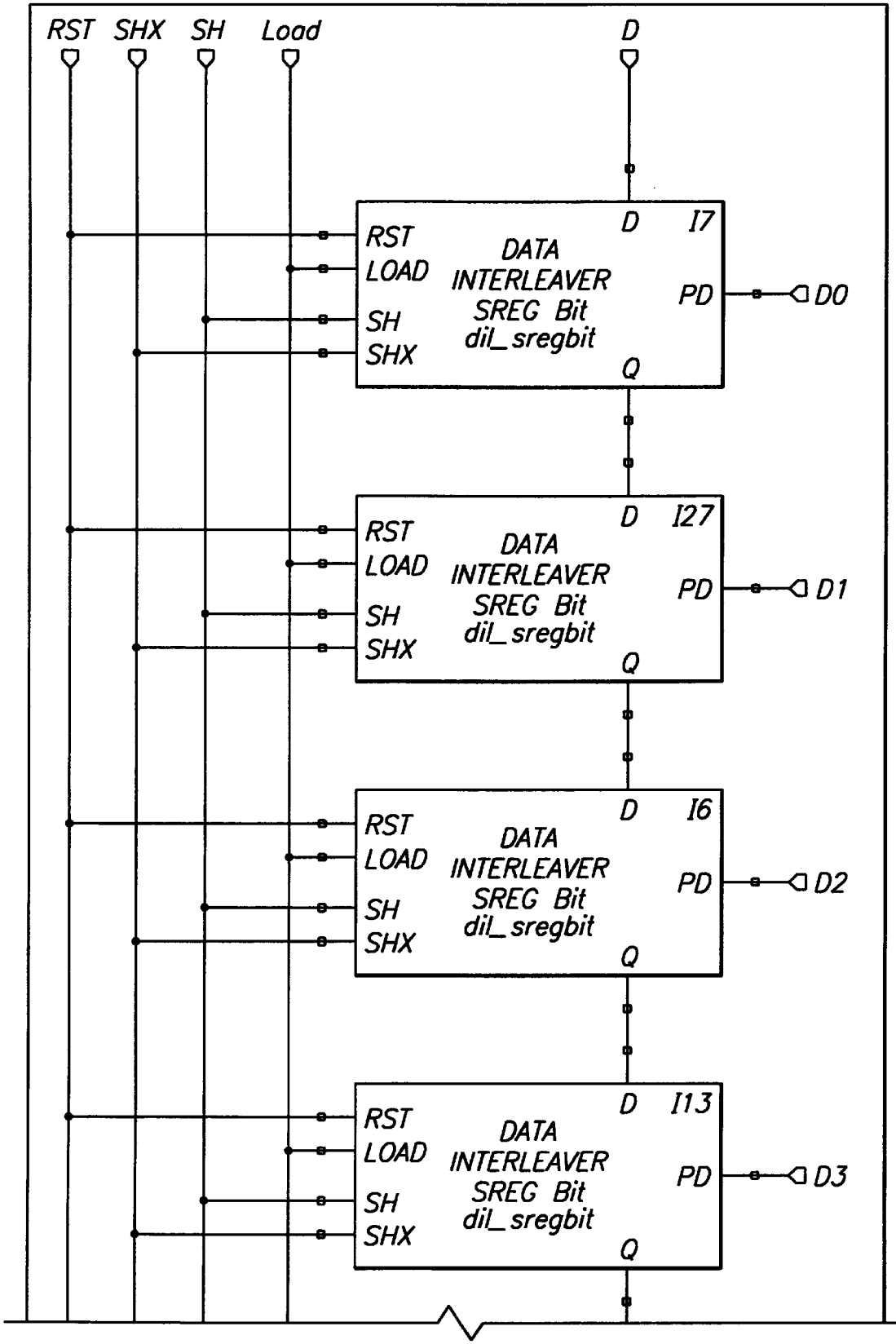

RST
SHX
SH
Load
D
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
D
I7
PD
D0
Q
D
I27
PD
D1
D
I6
PD
D2
D
I13
PD
D3

Fig 1.1502AA

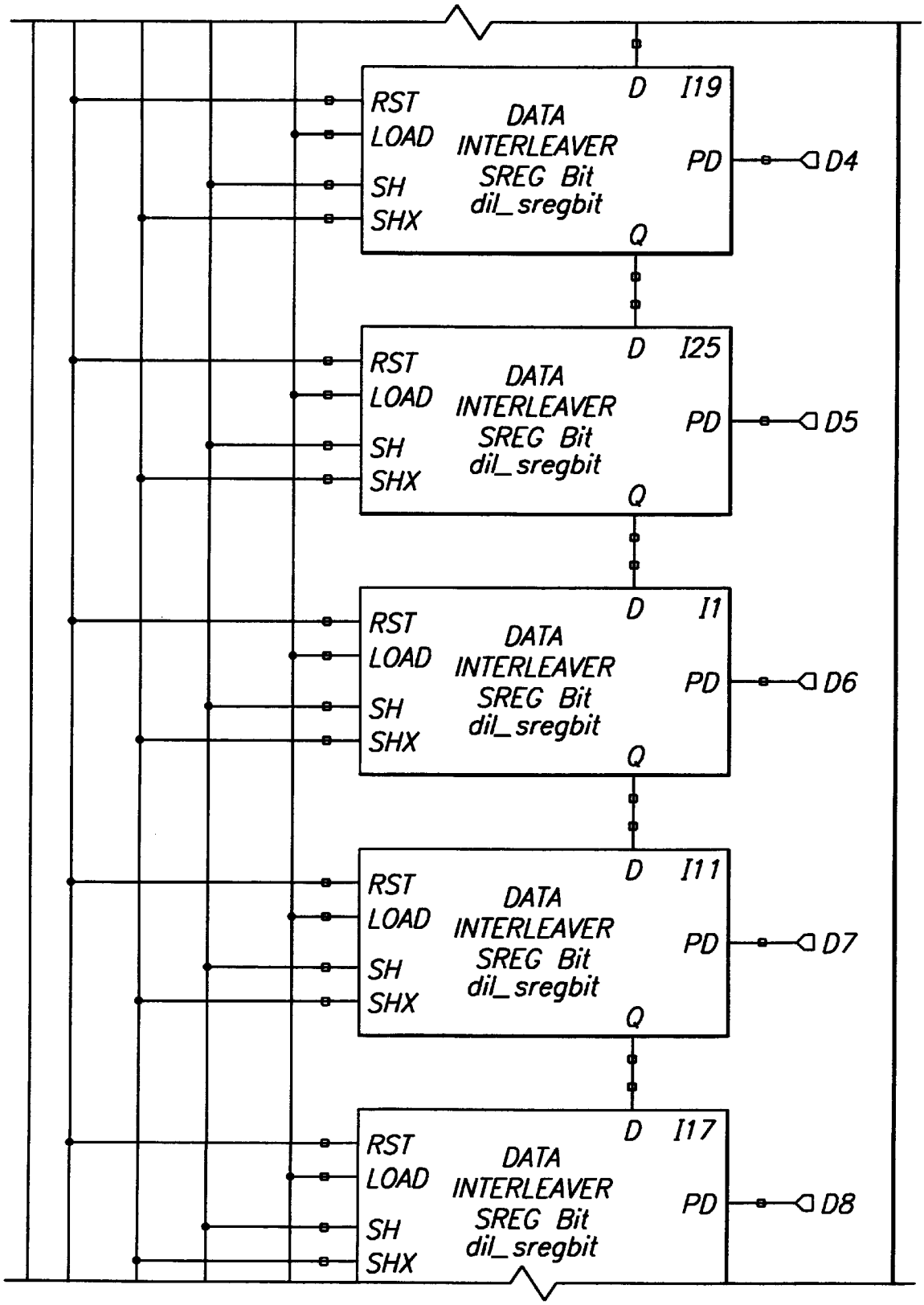


Fig 1.150288A

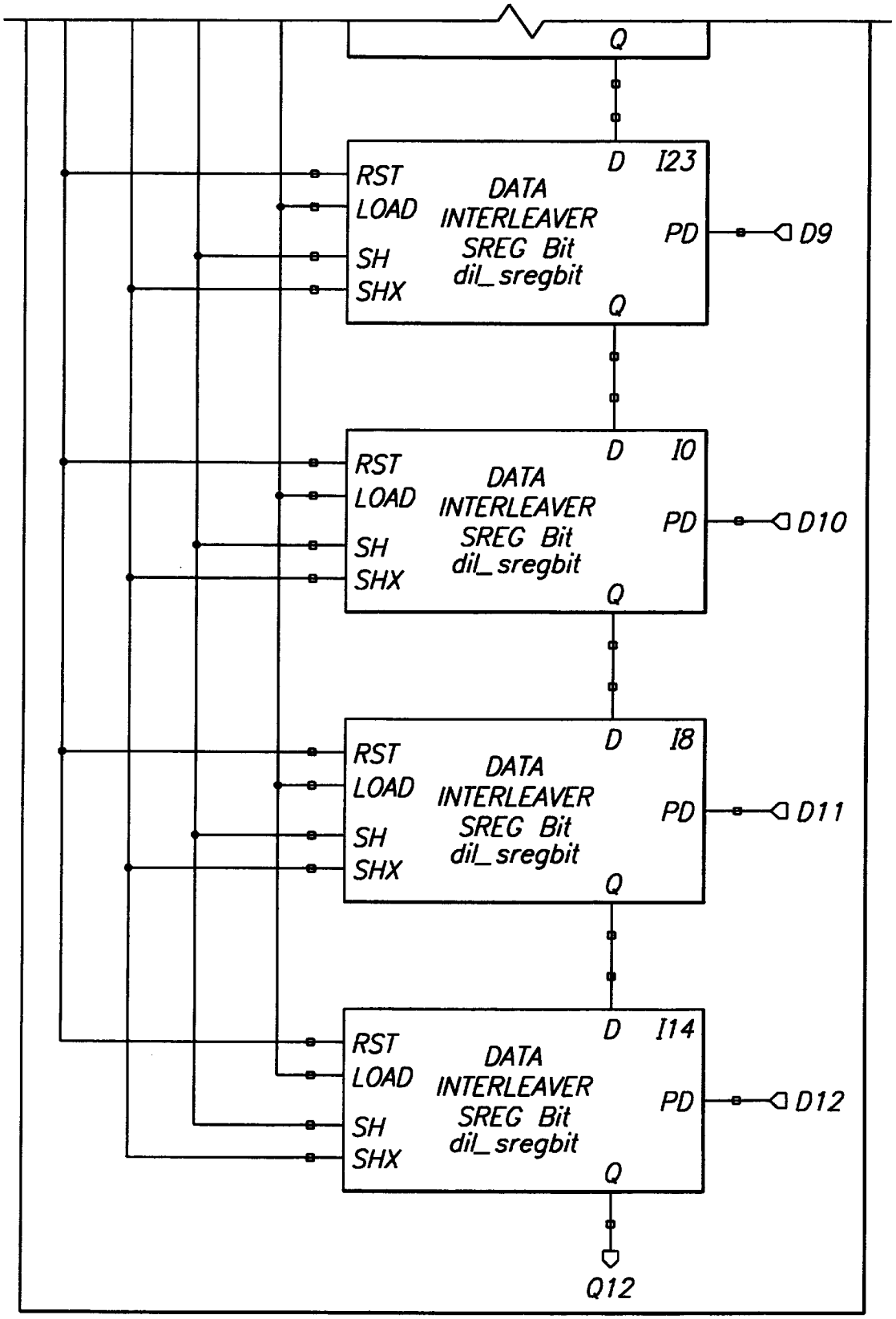

Q
D
I23
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
D9
Q
D
I0
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
D10
Q
D
I8
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
D11
Q
D
I14
RST
LOAD
SH
SHX
DATA
INTERLEAVER
SREG Bit
dil_sregbit
PD
D12
Q
Q12

Fig 1.1502CA

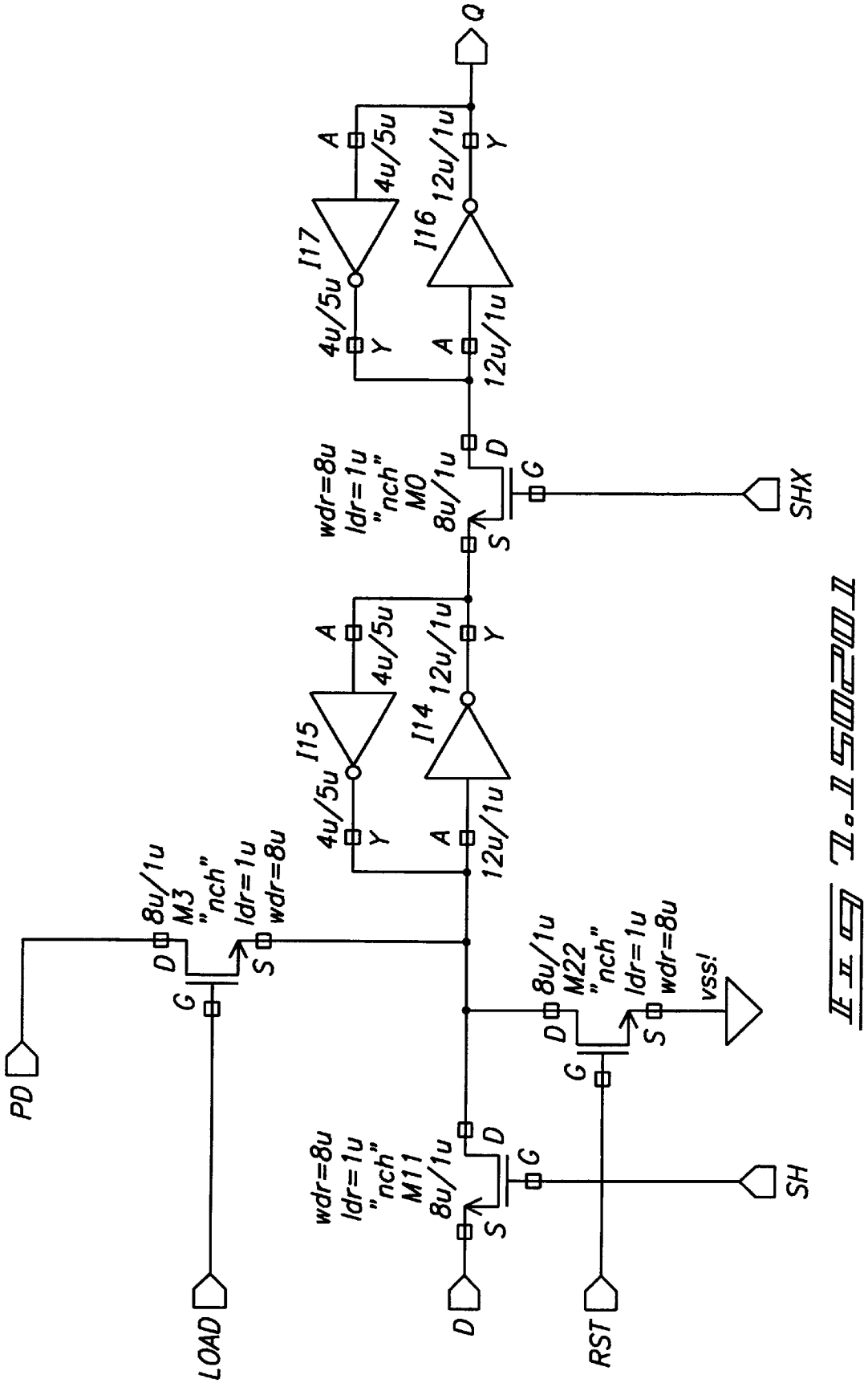

Q
A
4u/5u
Y
12u/1u
I17
I16
4u/5u
Y
A
12u/1u
wdr=8u
ldr=1u
"nch"
M0
8u/1u
D
G
S
SHX
I15
I14
PD
M3
M22
M11
LOAD
RST
SH
vss!

FIG. 11,605

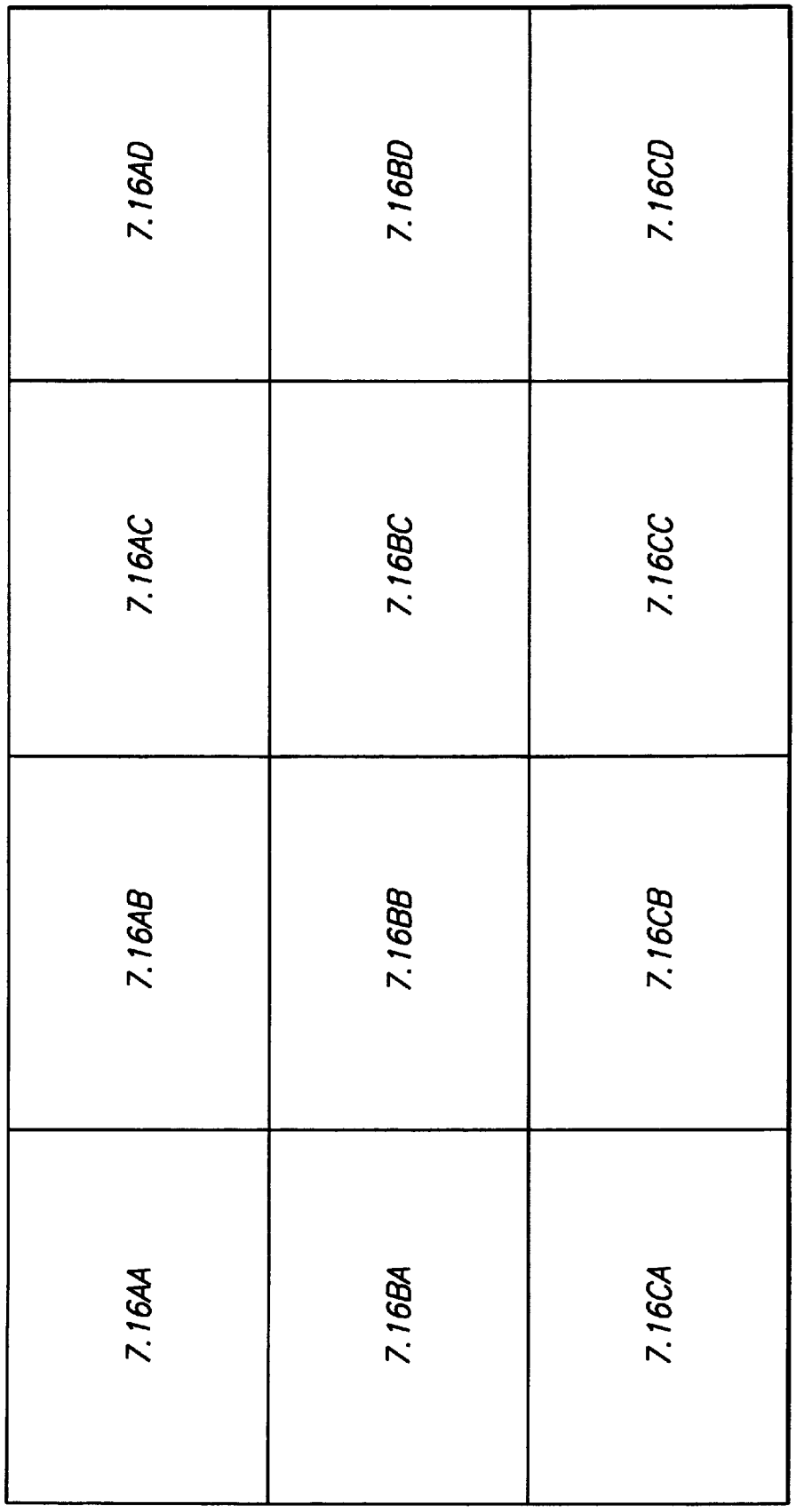

7.16AD
7.16BD
7.16CD
7.16AC
7.16BC
7.16CC
7.16AB
7.16BB
7.16CB
7.16AA
7.16BA
7.16CA

FIG. 7.16

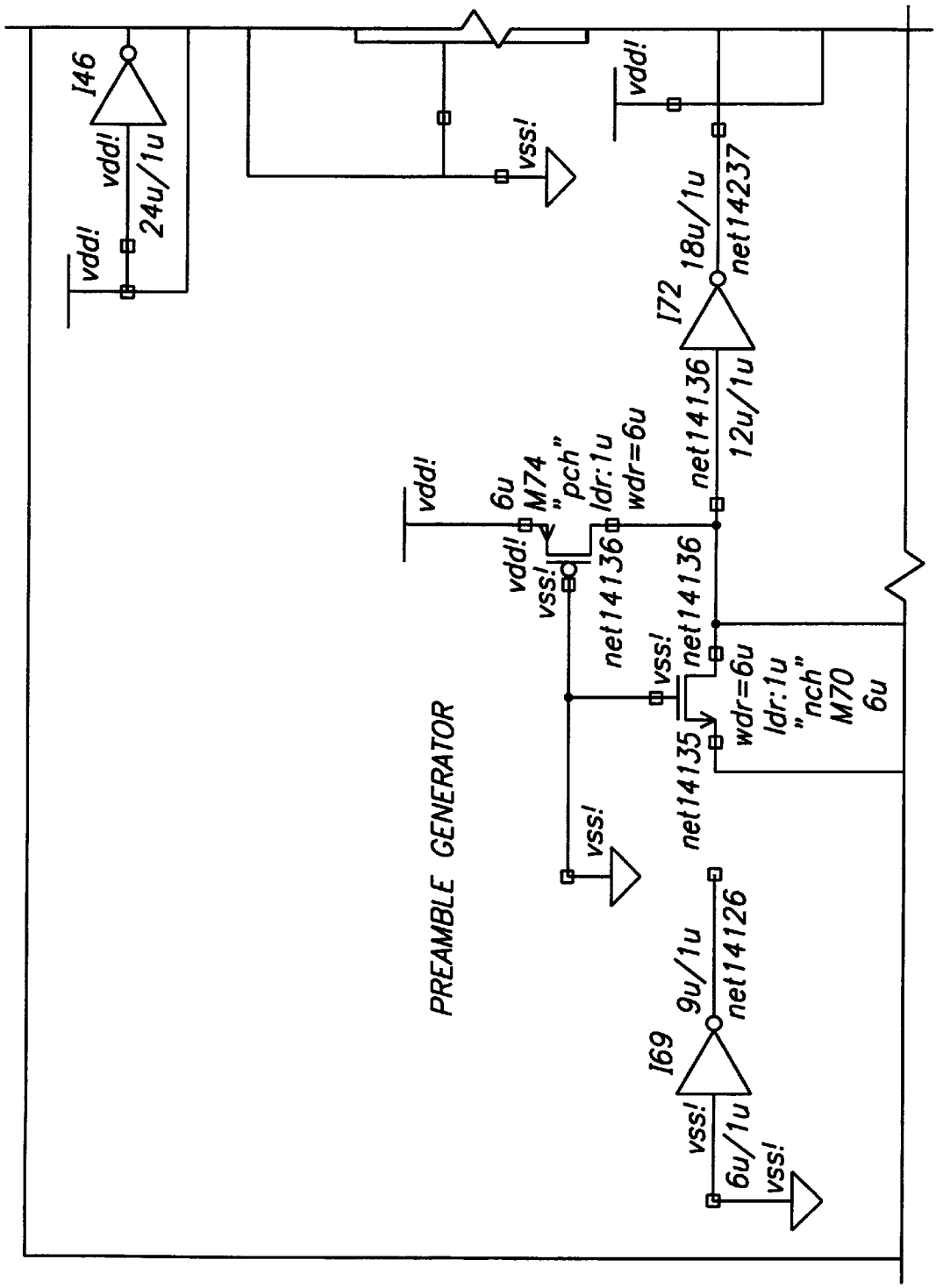

I46
vdd!
24u/1u
vdd!
vss!
vdd!
I72
18u/1u
net14237
net14136
12u/1u
vdd!
6u
M74
"pch"
ldr:1u
wdr=6u
vdd!
vss!
net14136
net14136
vss!
net14136
wdr=6u
ldr:1u
"nch"
M70
6u
net14135
vss!
PREAMBLE GENERATOR
I69
9u/1u
net14126
vss!
6u/1u
vss!

FIG. 11.15A

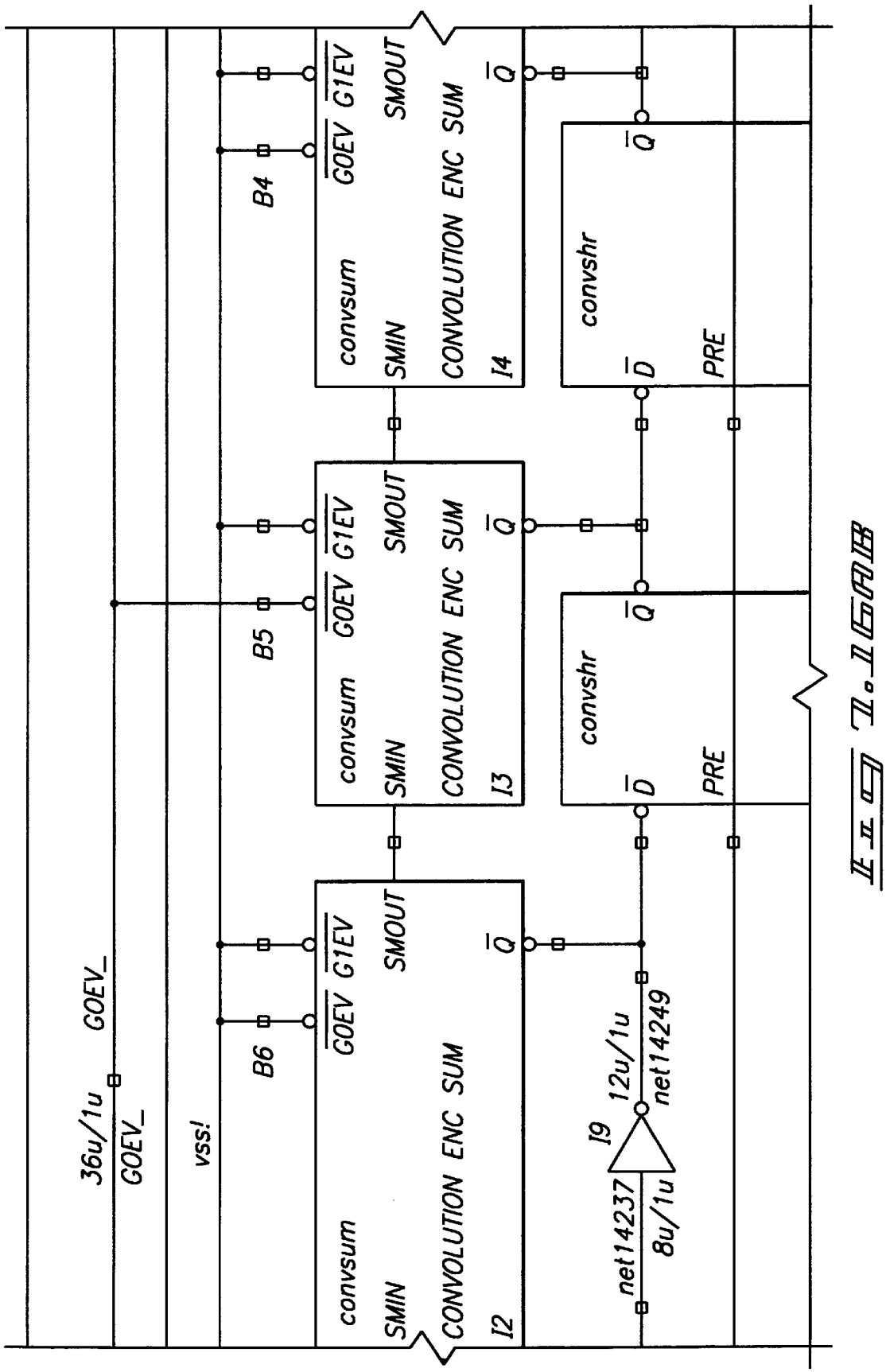

36u/1u
GOEV_
GOEV_
vss!
B6
B5
B4
GOEV
G1EV
convsum
SMIN
SMOUT
CONVOLUTION ENC SUM
I2
I3
I4
Q
D
convshr
PRE
I9
12u/1u
net14249
net14237
8u/1u

FIG 11.16AB

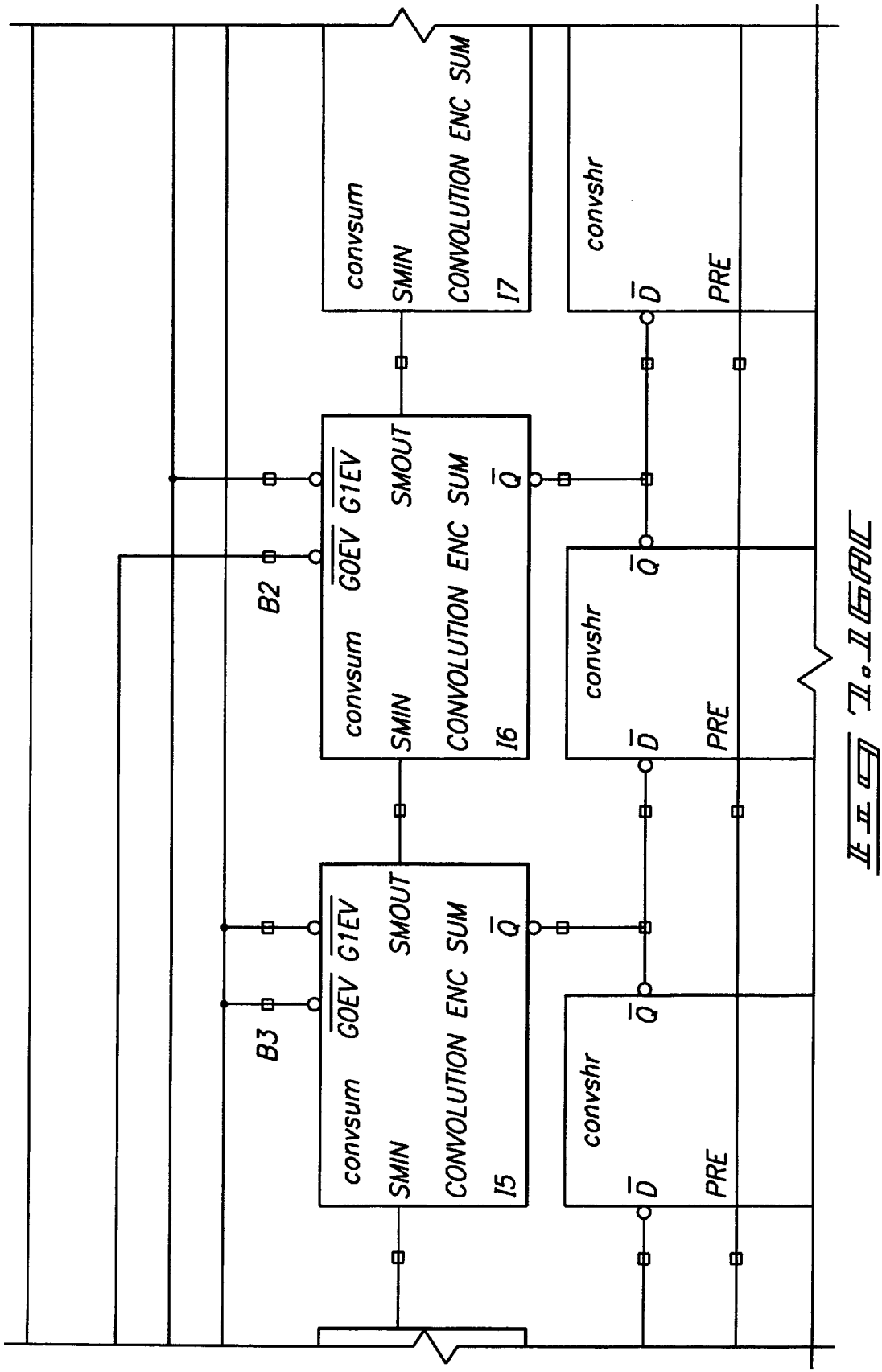

convsum
SMIN
CONVOLUTION ENC SUM
I7
convshr
D
PRE
B2
GOEV G1EV
SMOUT
Q
I6
B3
I5

FIG. 1167

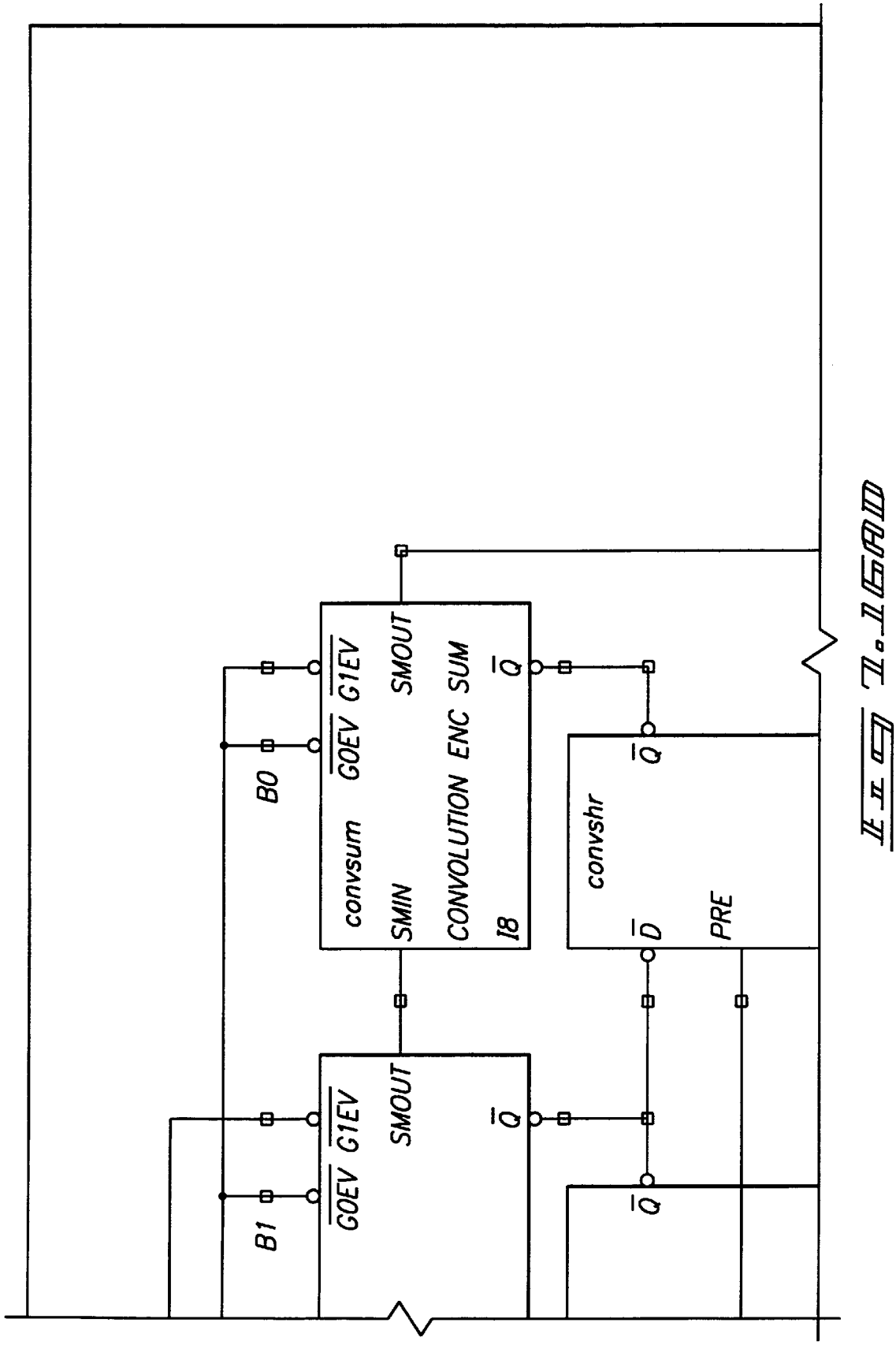

convsum
CONVOLUTION ENC SUM
SMIN
SMOUT
I8
B0
B1
G0EV
G1EV
Q
convshr
D
PRE

FIG. 11.1548

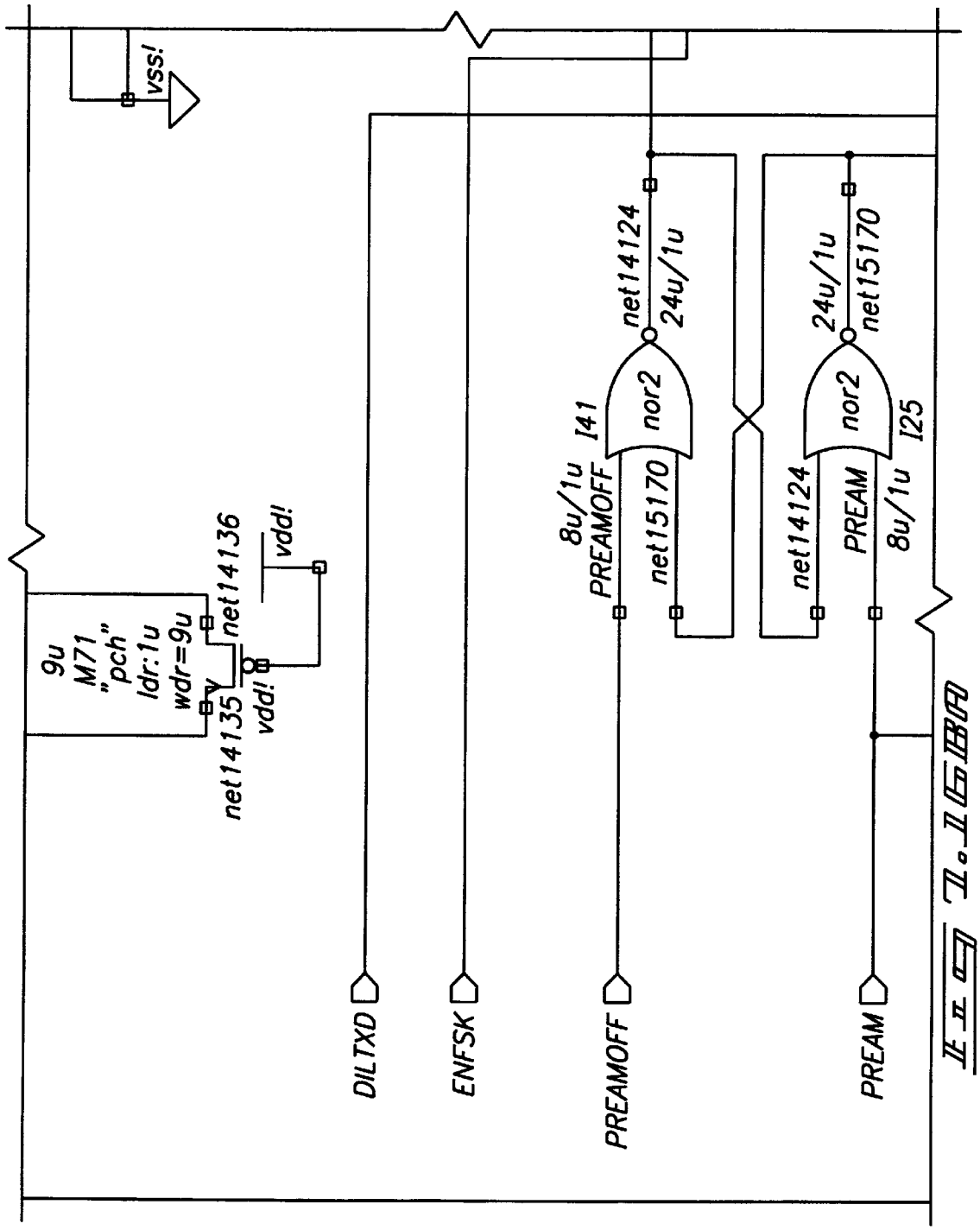
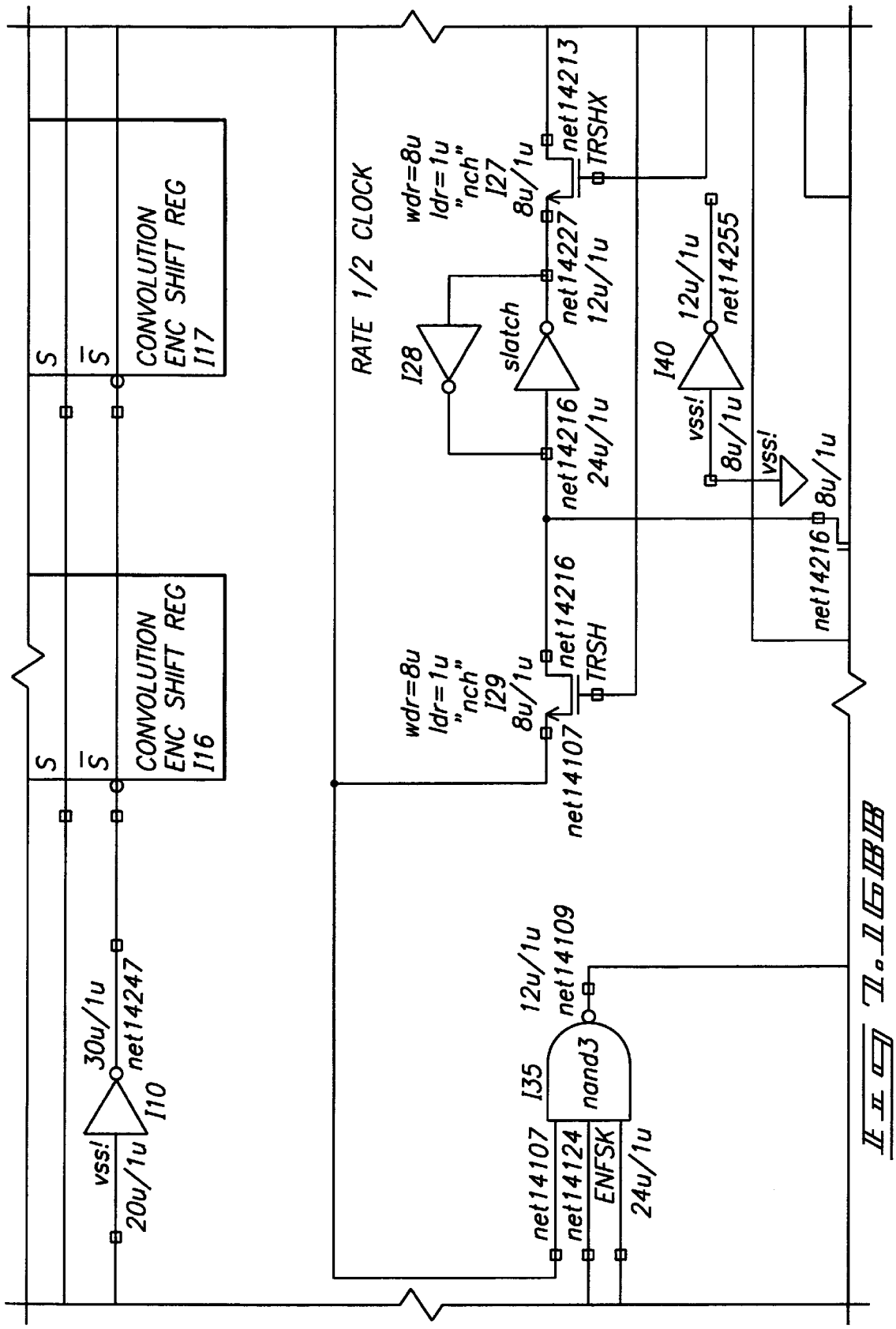

vss!
9u
M71
"pch"
ldr:1u
wdr=9u
net14135
net14136
vdd!
vdd!
DILTXD
ENFSK
PREAMOFF
PREAM
8u/1u
PREAMOFF
I41
nor2
net14124
24u/1u
net15170
net14124
PREAM
8u/1u
I25
nor2
24u/1u
net15170

FIG. 1163A


CONVOLUTION ENC SHIFT REG I17
CONVOLUTION ENC SHIFT REG I16
RATE 1/2 CLOCK
I10
I27
I28
I29
I35
I40
nand3
slatch
TRSHX
TRSH
ENFSK
vss!
net14247
net14213
net14227
net14255
net14216
net14107
net14124
net14109
30u/1u
20u/1u
wdr=8u
ldr=1u
"nch"
8u/1u
12u/1u
24u/1u

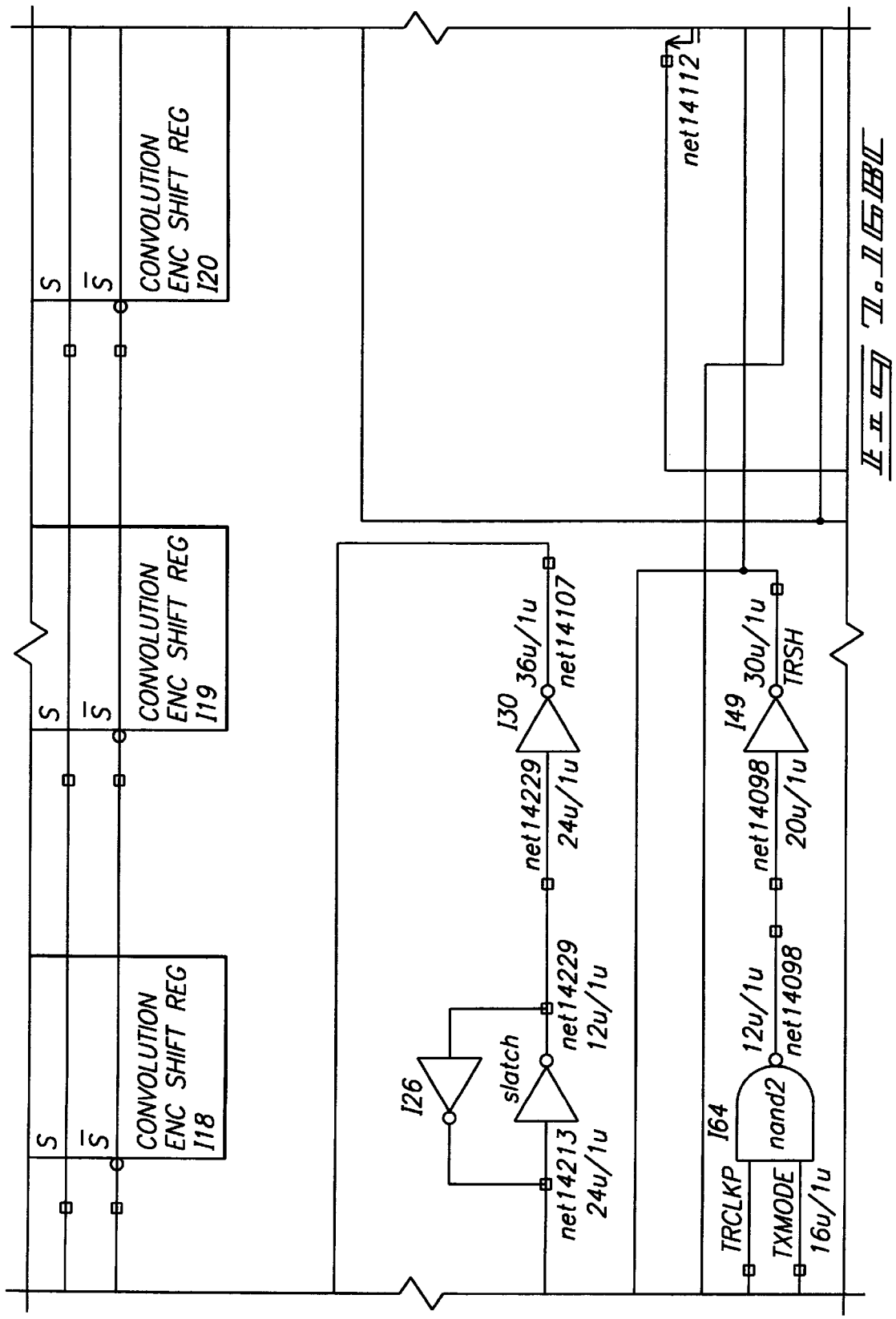

CONVOLUTION ENC SHIFT REG I20
CONVOLUTION ENC SHIFT REG I19
CONVOLUTION ENC SHIFT REG I18
S
S̄
net14112
I30 36u/1u net14107
net14229 24u/1u
I26
slatch
net14229 12u/1u
net14213 24u/1u
I49 30u/1u TRSH
net14098 20u/1u
12u/1u net14098
I64 nand2
TRCLKP
TXMODE
16u/1u

FIG. 1163

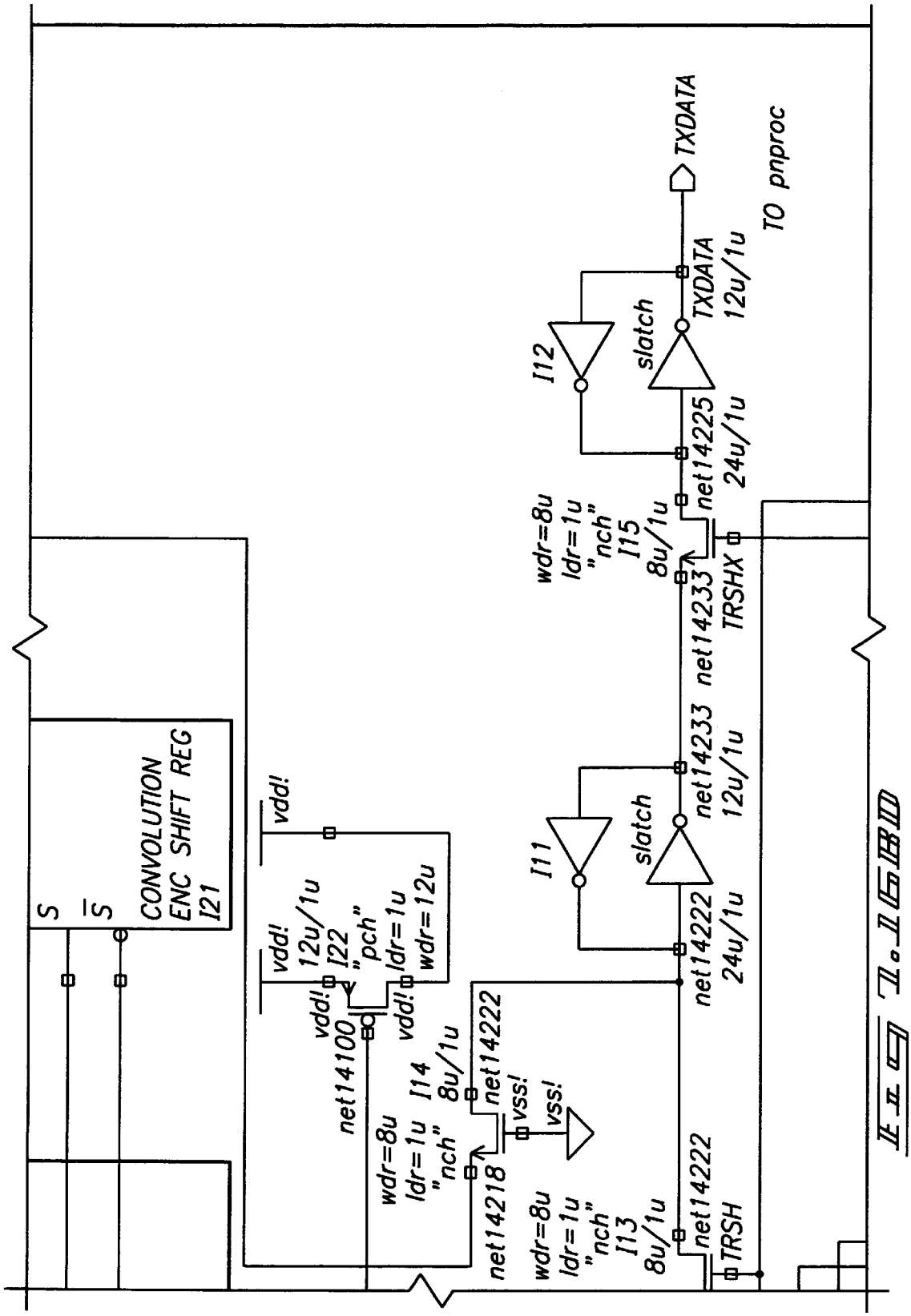

CONVOLUTION ENC SHIFT REG I21
S
S
vdd!
I22
"pch"
12u/1u
ldr=1u
wdr=12u
net14100
I14
"nch"
8u/1u
wdr=8u
ldr=1u
net14218
net14222
vss!
I13
I11
slatch
net14233
net14222
I12
slatch
TXDATA
net14225
I15
net14233
TRSHX
net14222
TRSH
TO pnproc

FIG. 1161B

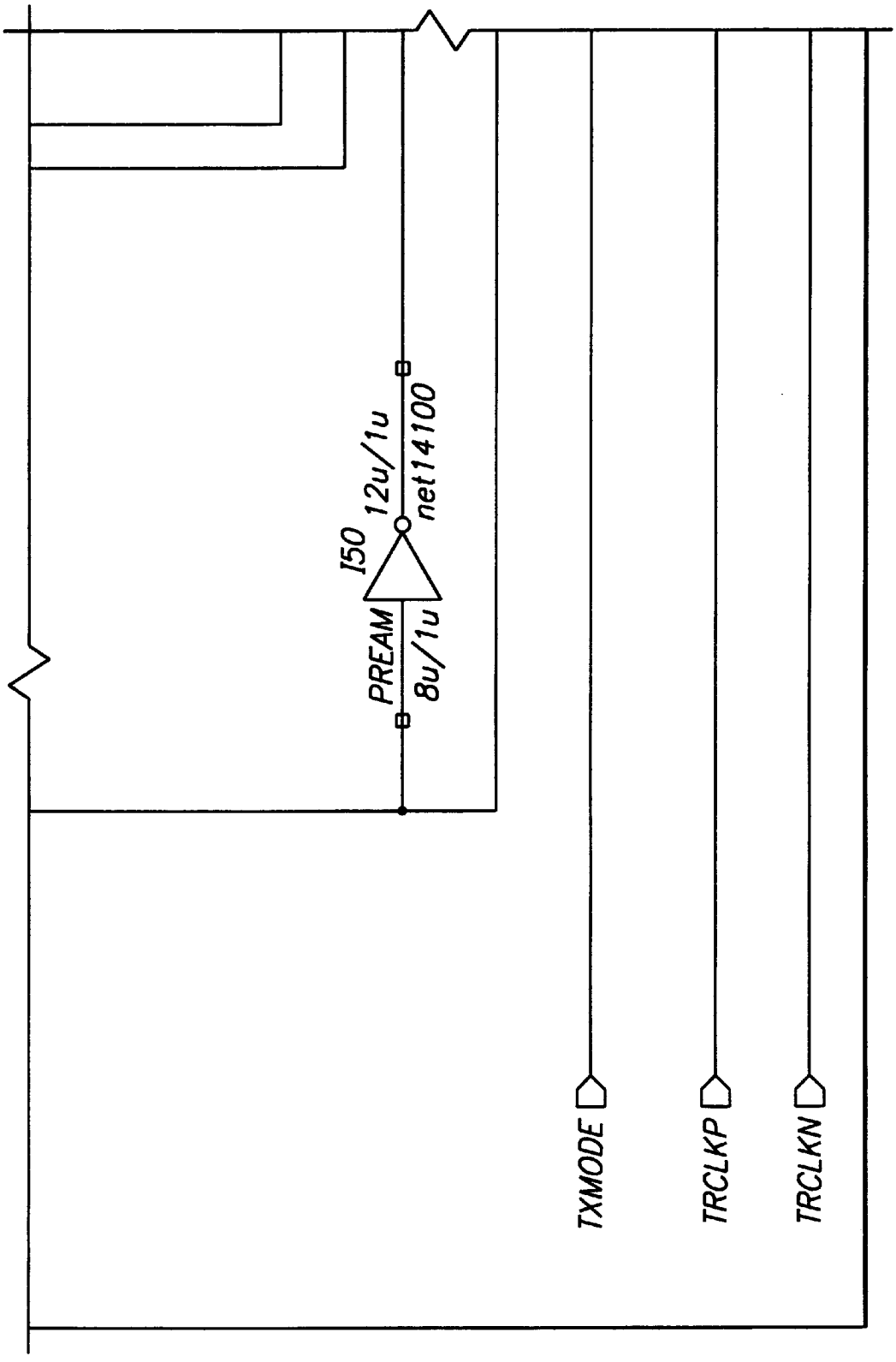


FIG. 11.1GA

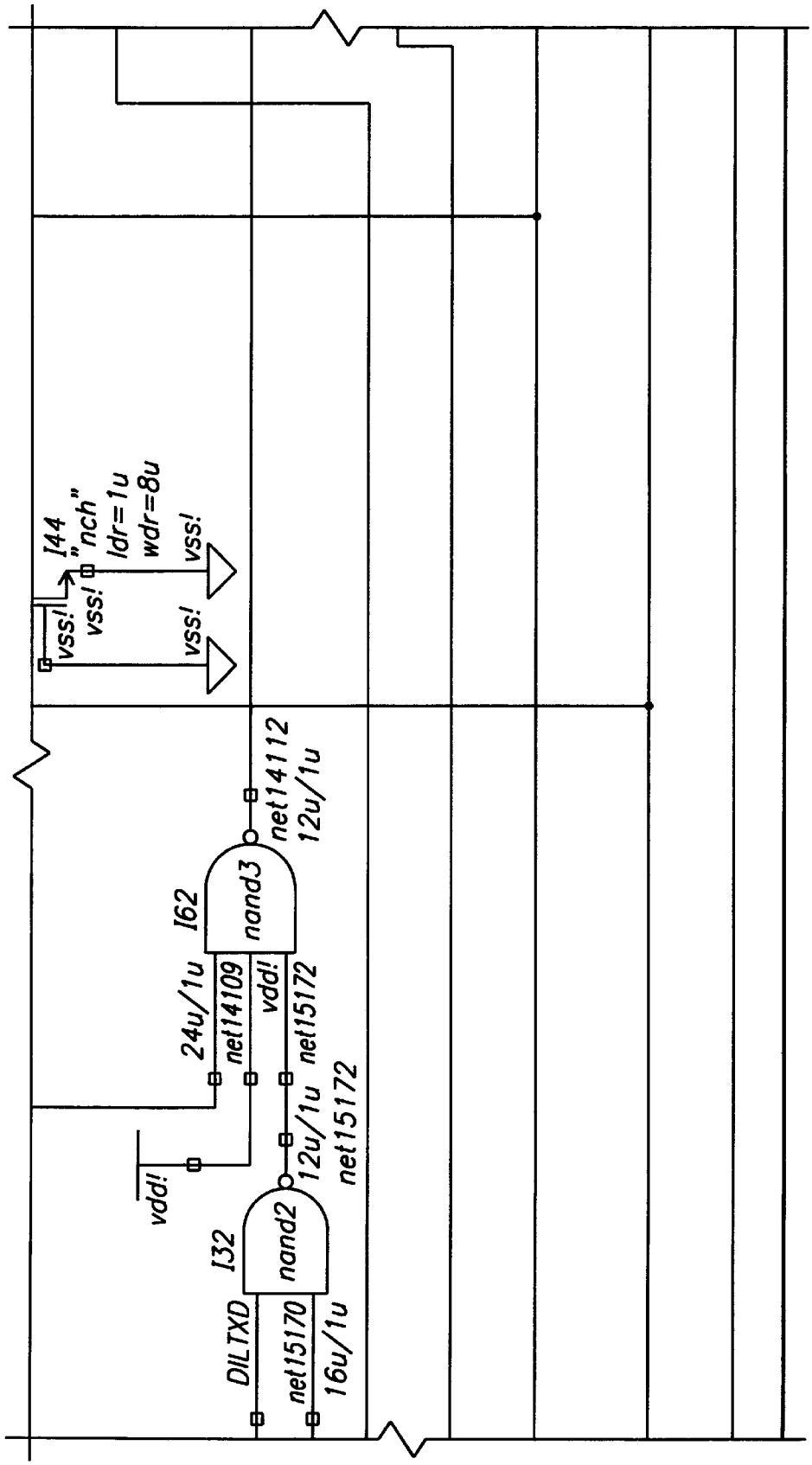

I44
"nch"
ldr=1u
wdr=8u
vss!
vss!
vss!
vss!
I62
nand3
net14112
12u/1u
24u/1u
net14109
vdd!
net15172
vdd!
I32
nand2
12u/1u
net15172
DILTXD
net15170
16u/1u

FIG. 1074

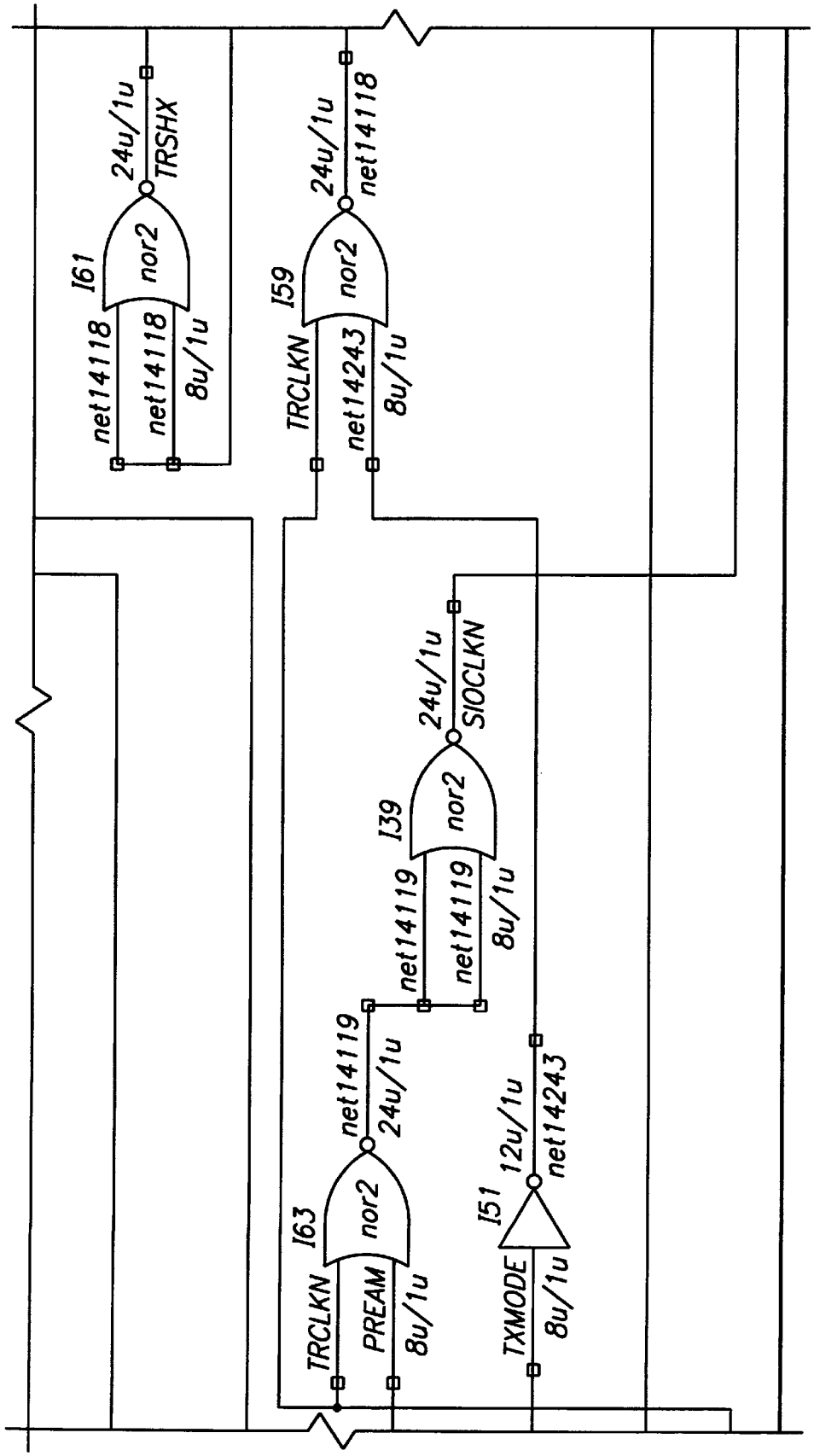

I61
nor2
24u/1u
TRSHX
net14118
net14118
8u/1u
I59
nor2
24u/1u
net14118
TRCLKN
net14243
8u/1u
I39
nor2
24u/1u
SIOCLKN
net14119
net14119
8u/1u
I63
nor2
net14119
24u/1u
TRCLKN
PREAM
8u/1u
I51
12u/1u
net14243
TXMODE
8u/1u

FIG. 1.1551

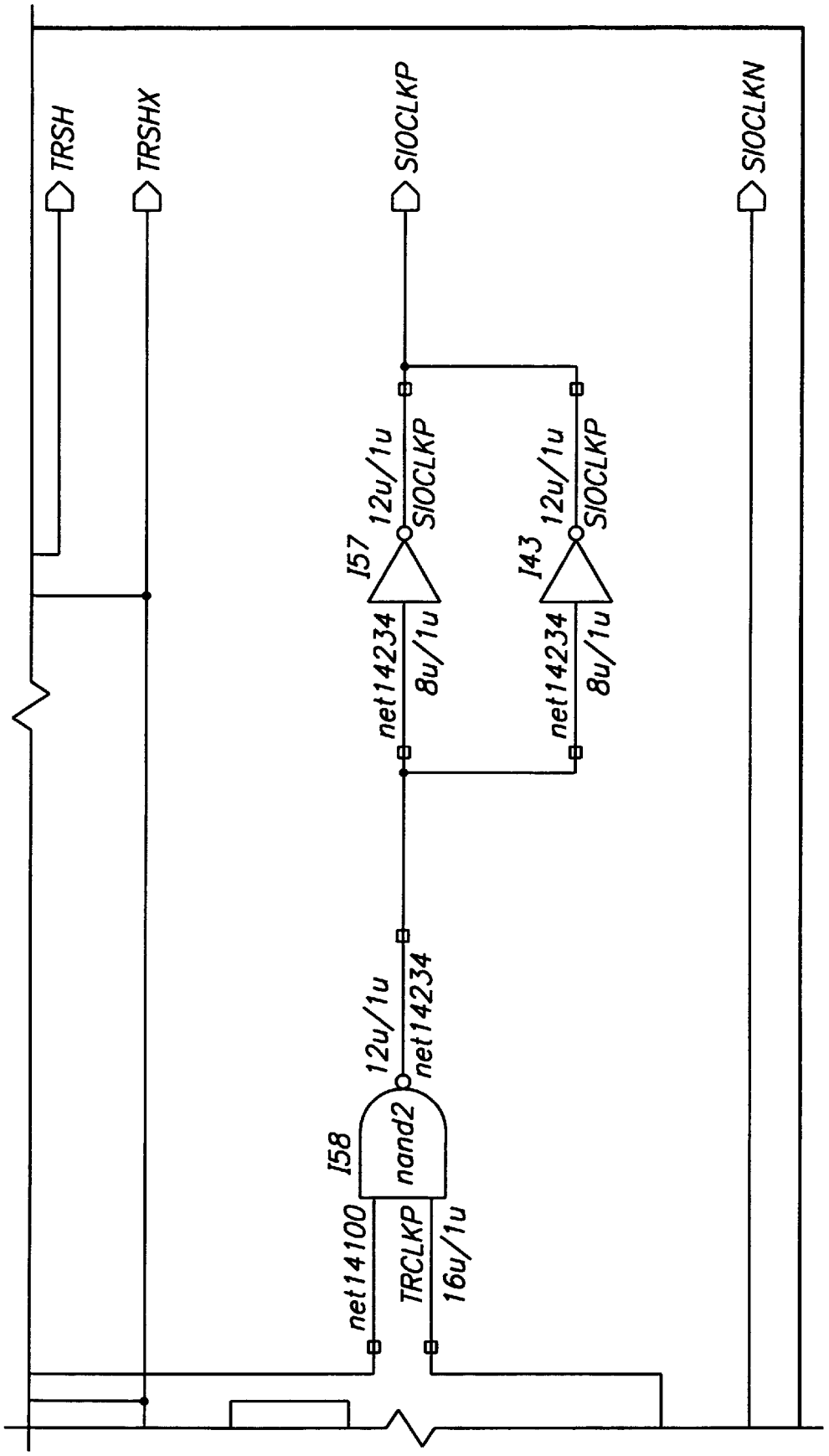

TRSH
TRSHX
SIOCLKP
SIOCLKN
I57
12u/1u
SIOCLKP
net14234
8u/1u
I43
12u/1u
SIOCLKP
net14234
8u/1u
12u/1u
net14234
I58
nand2
net14100
TRCLKP
16u/1u

FIG. 11E

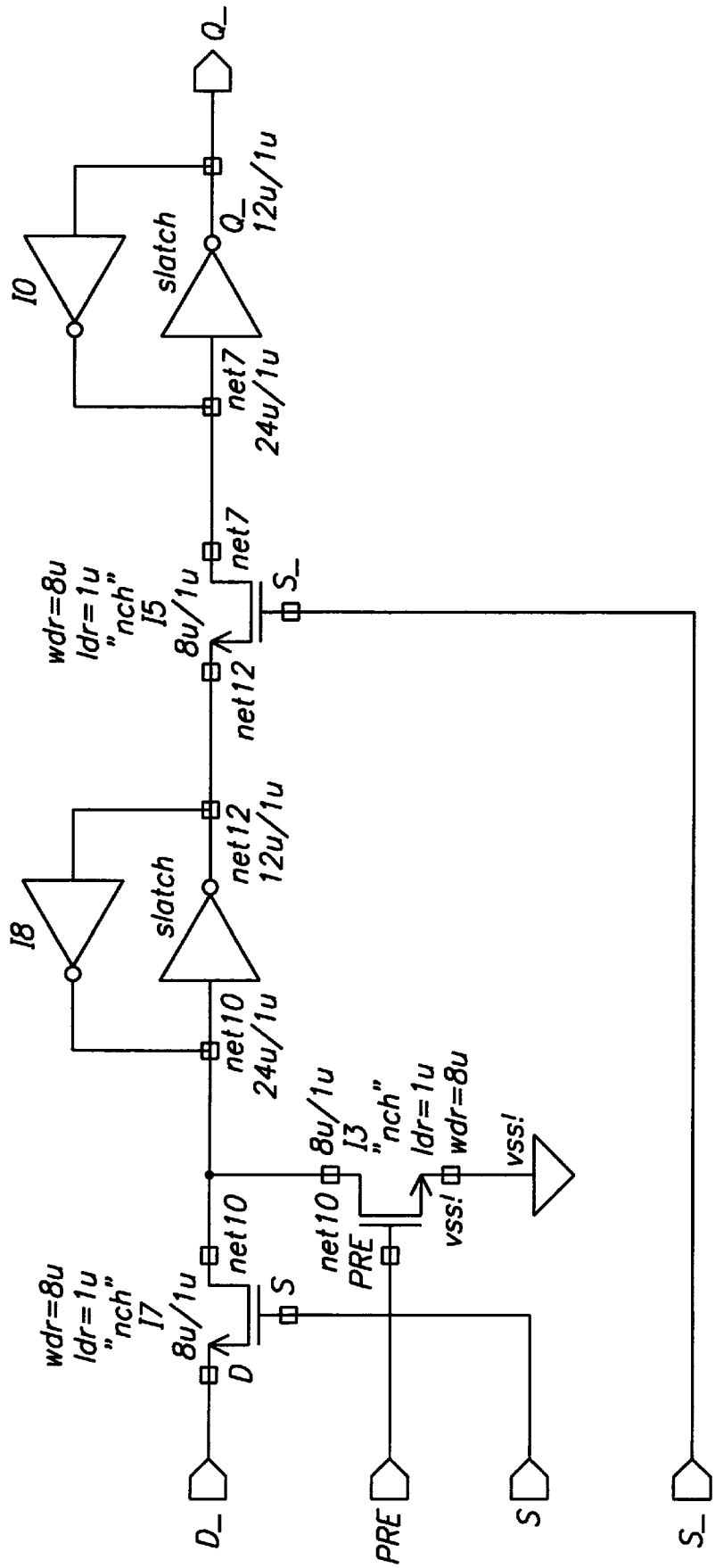

Q_
I0
slatch
Q_
12u/1u
net7
24u/1u
wdr=8u
ldr=1u
"nch"
I5
8u/1u
net7
S_
net12
I8
slatch
net12
12u/1u
net10
24u/1u
8u/1u
I3
"nch"
ldr=1u
wdr=8u
vss!
net10
PRE
vss!
wdr=8u
ldr=1u
"nch"
I7
8u/1u
net10
S
D
D_
PRE
S
S_

FIG. 1L

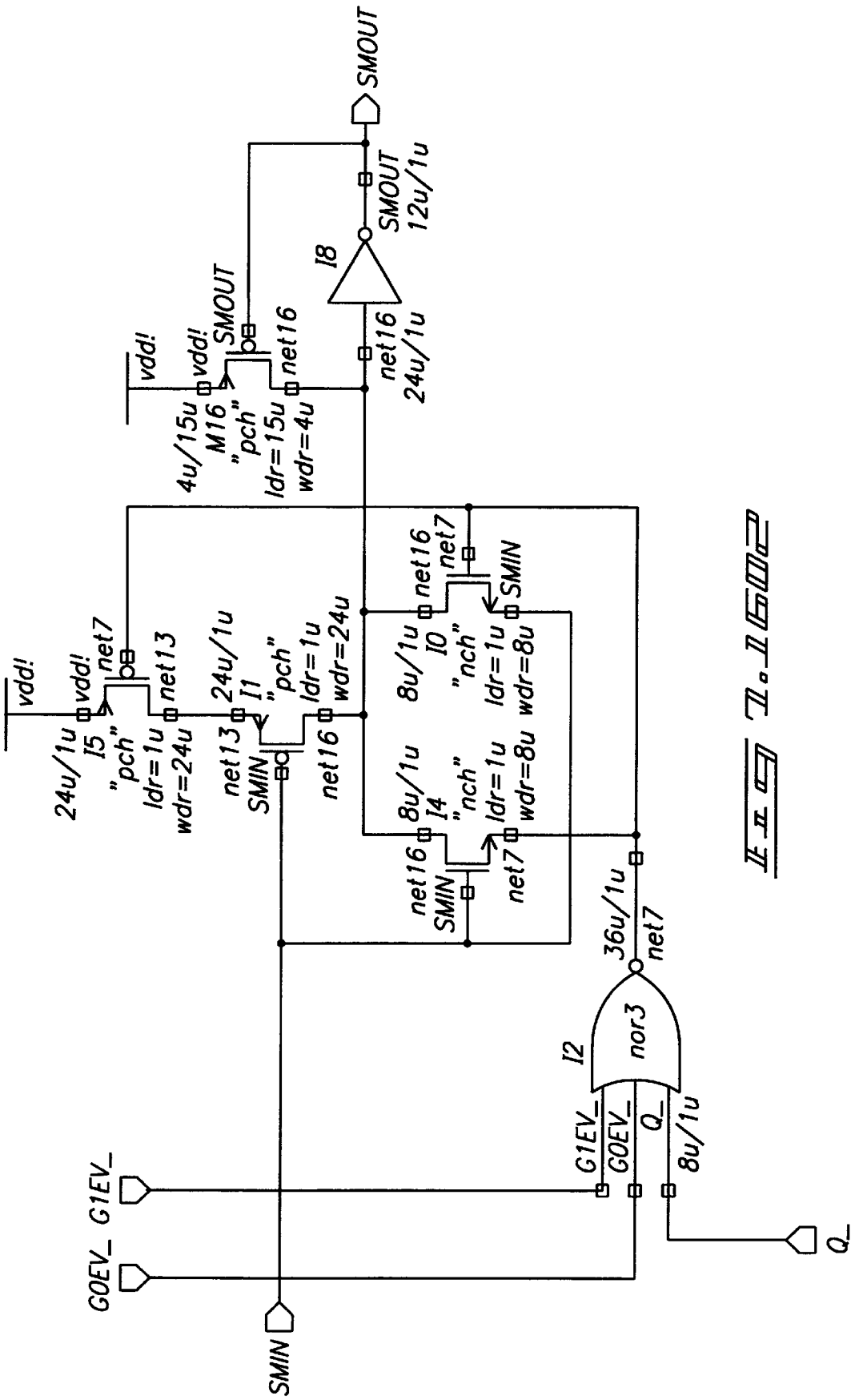

SMOUT
SMOUT
12u/1u
I8
net16
24u/1u
vdd!
vdd!
SMOUT
4u/15u
M16
"pch"
ldr=15u
wdr=4u
net16
vdd!
vdd!
net7
24u/1u
I5
"pch"
ldr=1u
wdr=24u
net13
net13
24u/1u
I1
"pch"
ldr=1u
wdr=24u
SMIN
net16
net16
net7
8u/1u
I0
"nch"
ldr=1u
wdr=8u
SMIN
net16
8u/1u
I4
"nch"
ldr=1u
wdr=8u
SMIN
net7
36u/1u
net7
I2
nor3
G1EV_
G0EV_
Q_
8u/1u
G1EV_
G0EV_
SMIN
Q_

FIG. 1,600

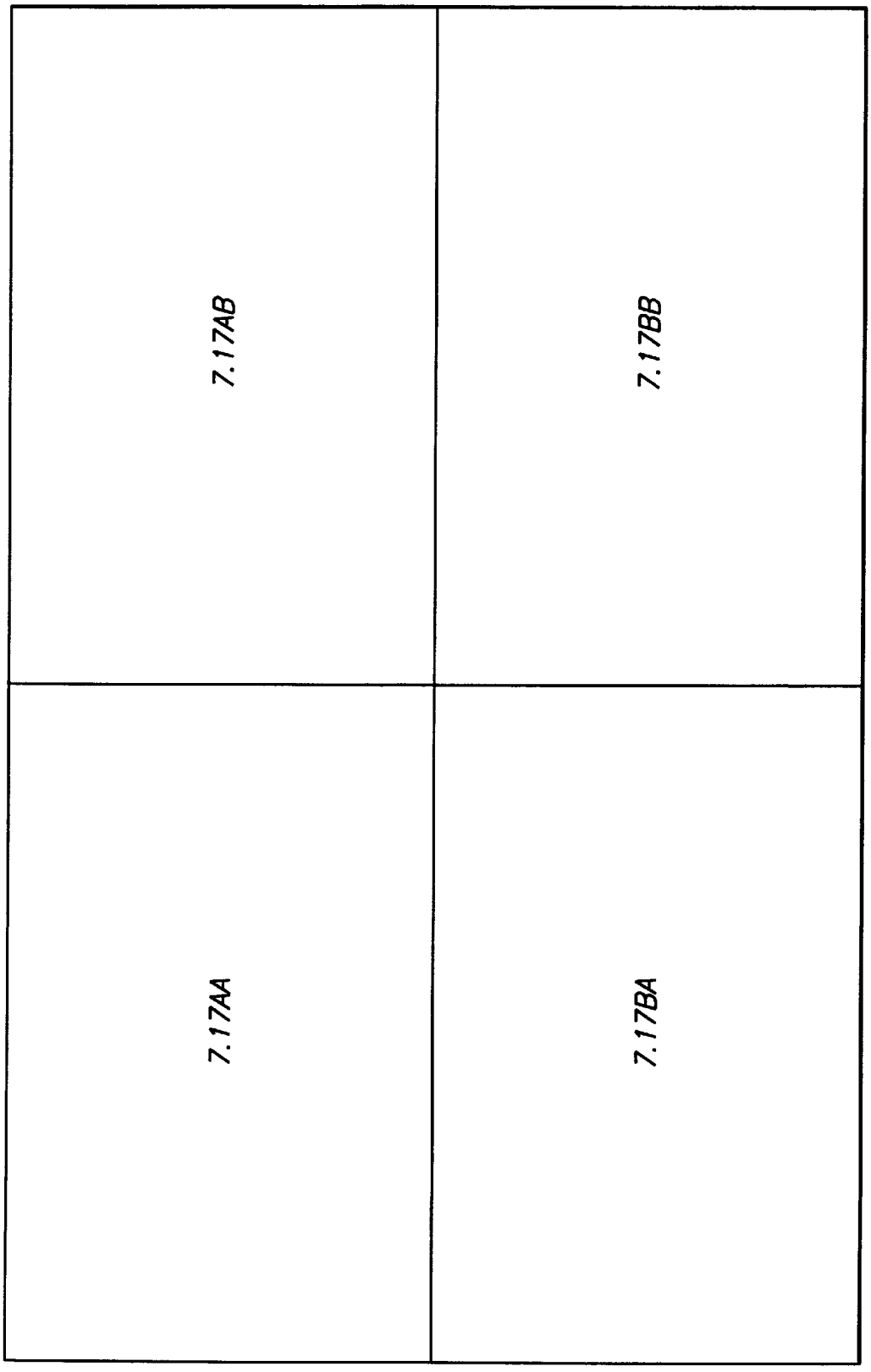


FIG. 7.17

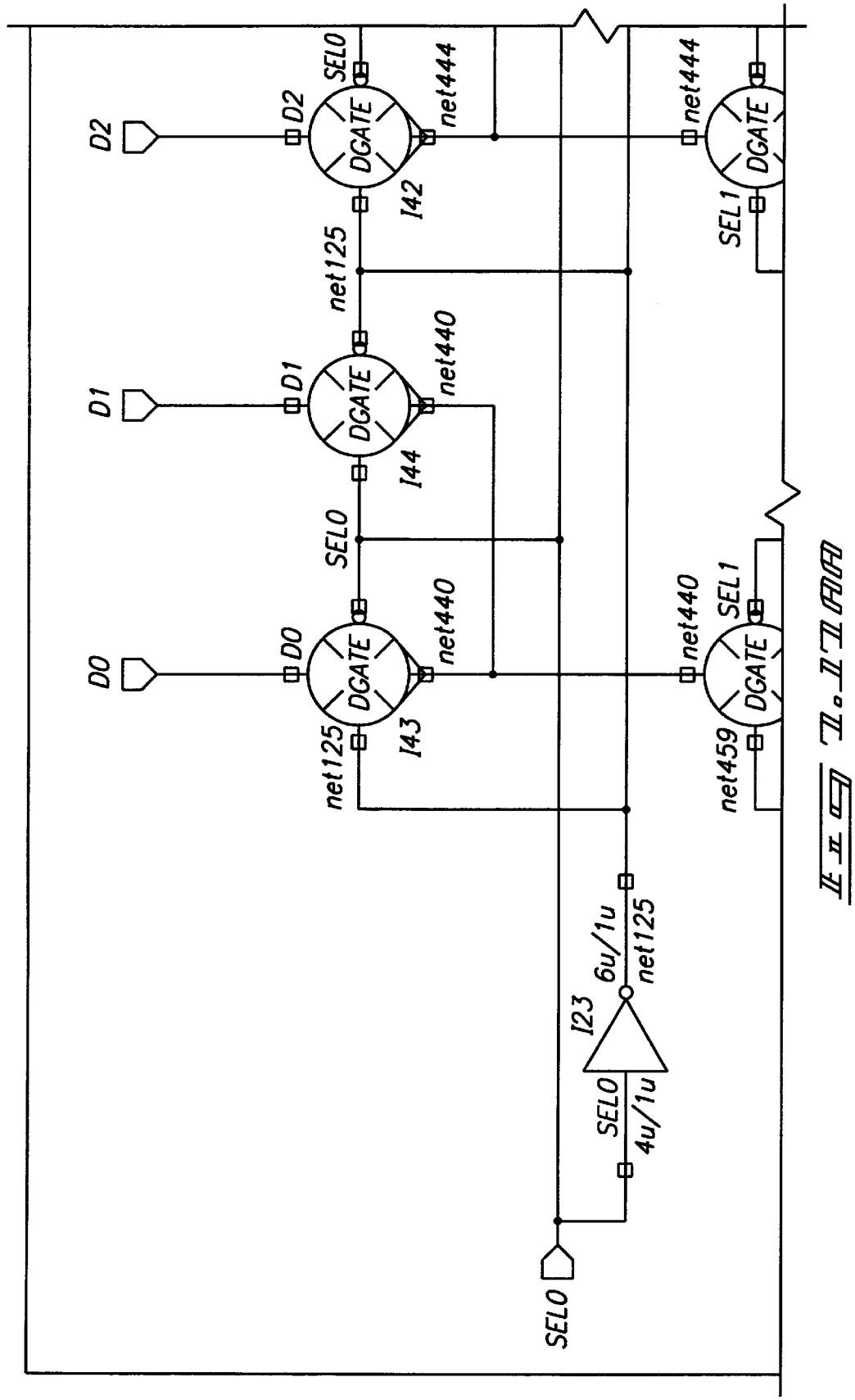

D2
D1
D0
SEL0
SEL1
DGATE
I42
I44
I43
I23
net444
net125
net440
net459
6u/1u
4u/1u

FIG. 11AAA

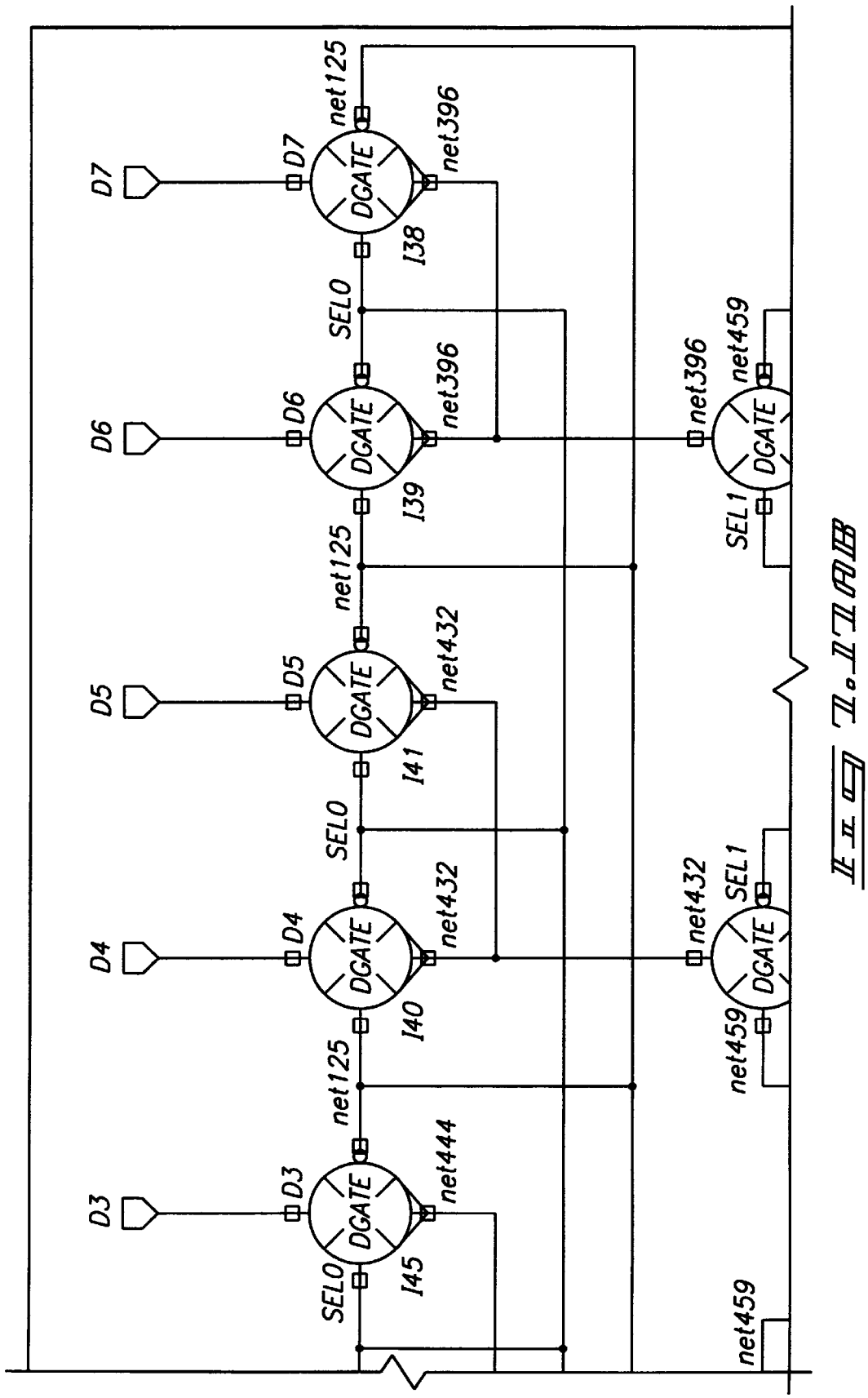

D7
D6
D5
D4
D3
D7
DGATE
D6
DGATE
D5
DGATE
D4
DGATE
D3
DGATE
net125
net396
I38
SEL0
net396
net459
I39
net125
net432
I41
SEL0
net432
SEL1
I40
net125
net444
I45
SEL0
net459
net459
SEL1
net396
net459
net432
net459

FIG. 1171

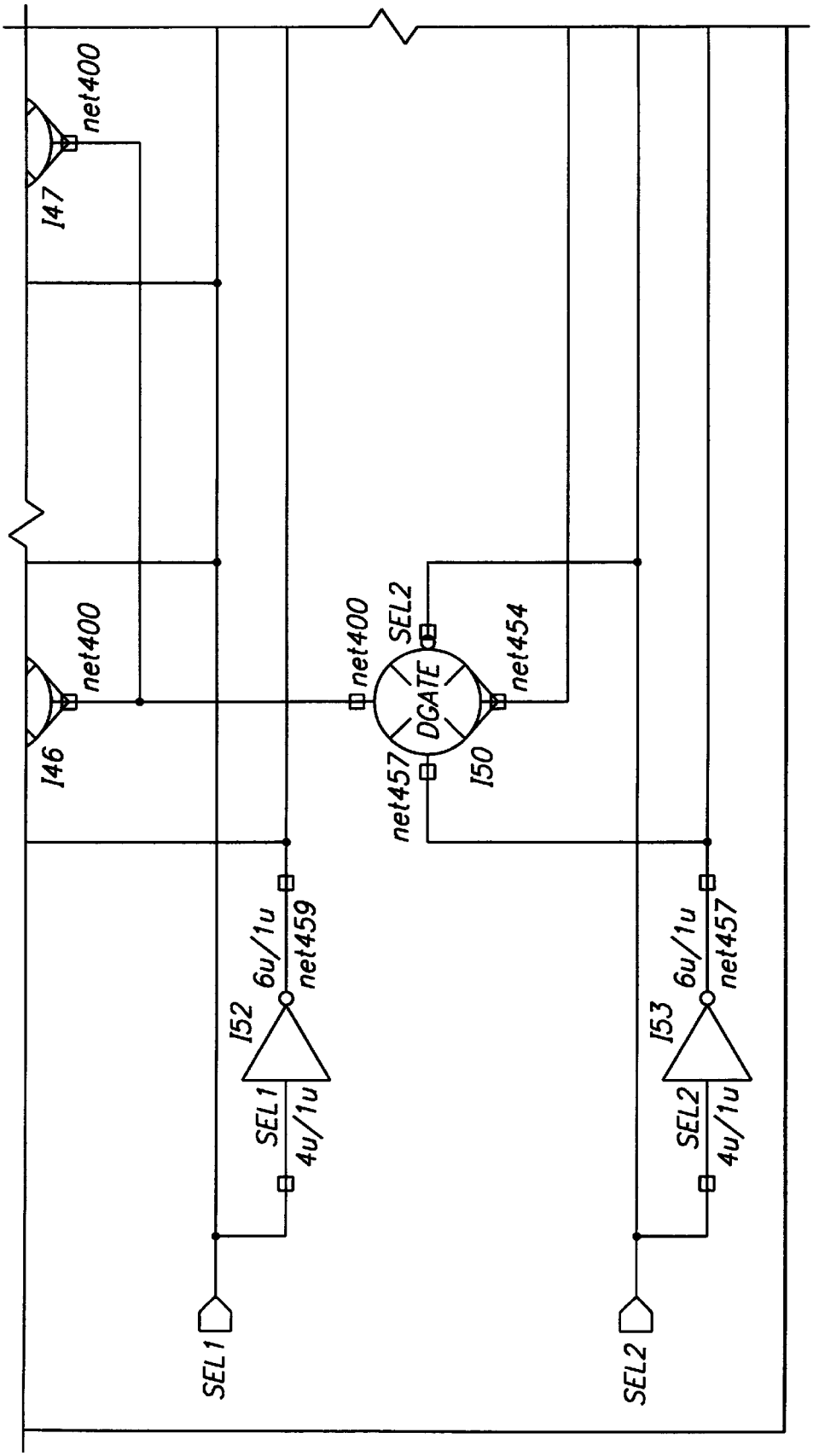

net400
I47
net400
I46
net400
SEL2
DGATE
net454
net457
I50
6u/1u
net459
I52
SEL1
4u/1u
SEL1
6u/1u
net457
I53
SEL2
4u/1u
SEL2

FIG. 1182

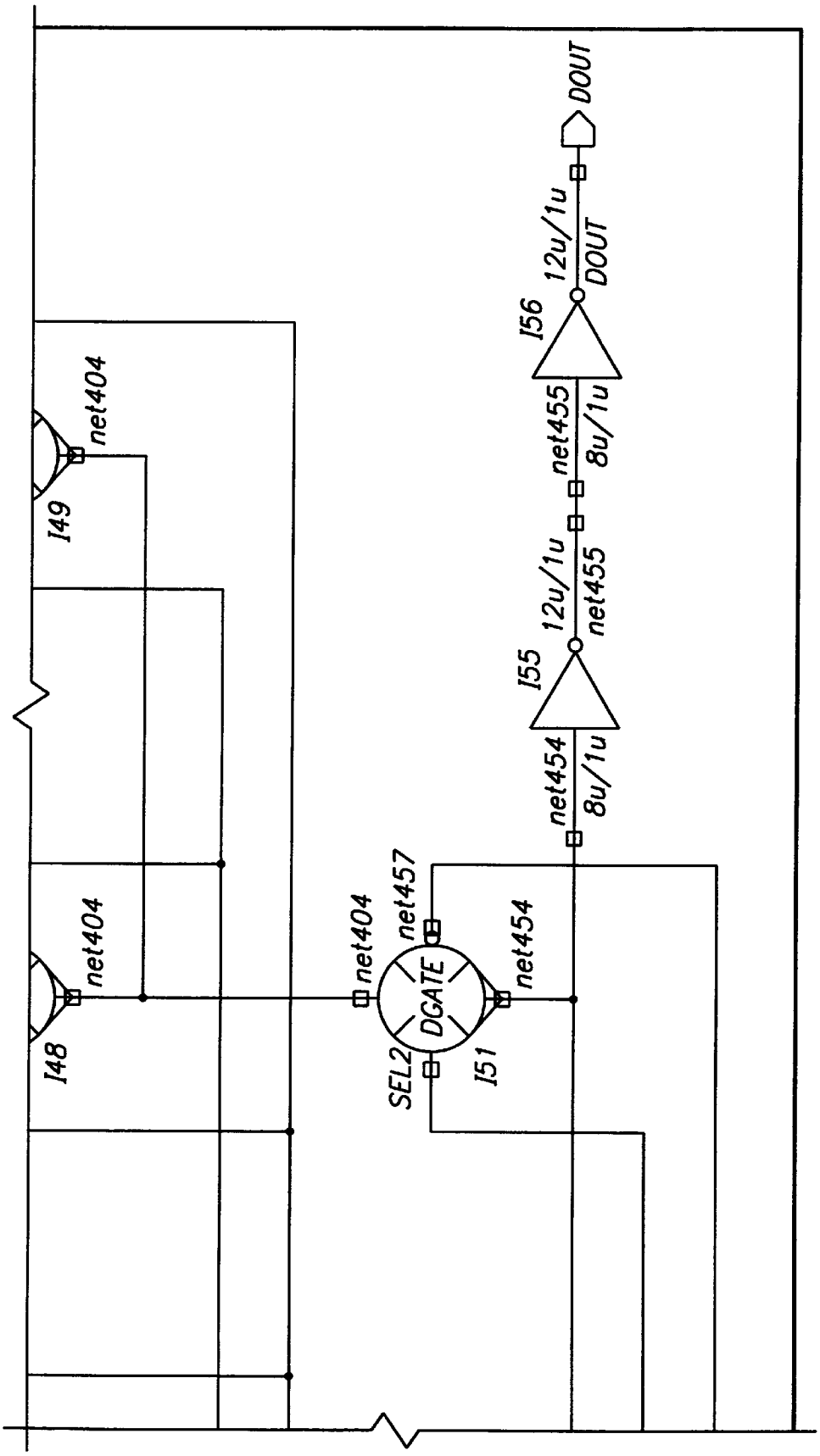

DOUT
I56
12u/1u
DOUT
net455
8u/1u
I55
12u/1u
net455
net454
8u/1u
net404
I49
net404
I48
net404
net457
DGATE
SEL2
I51
net454

FIG. 1183

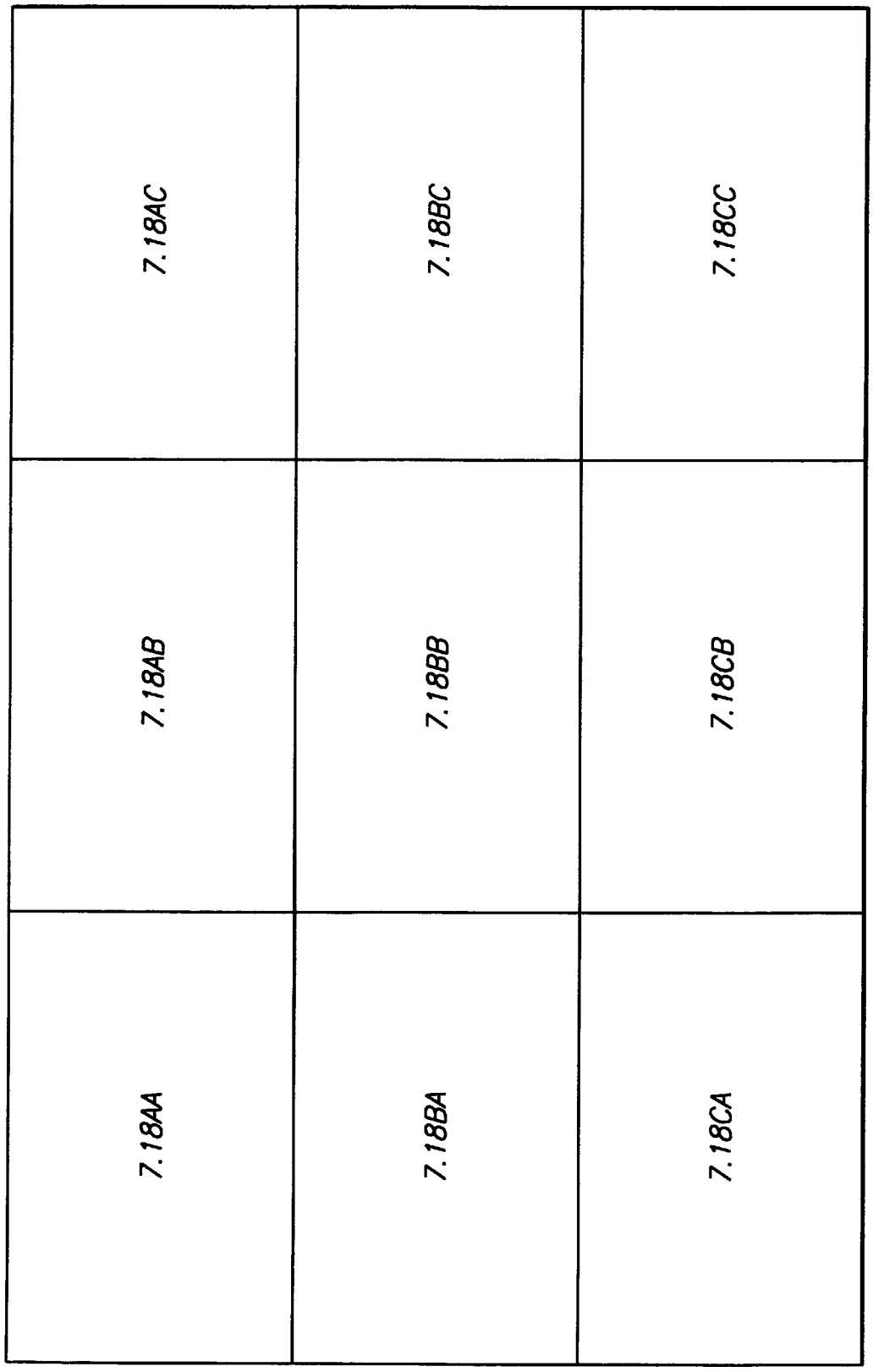
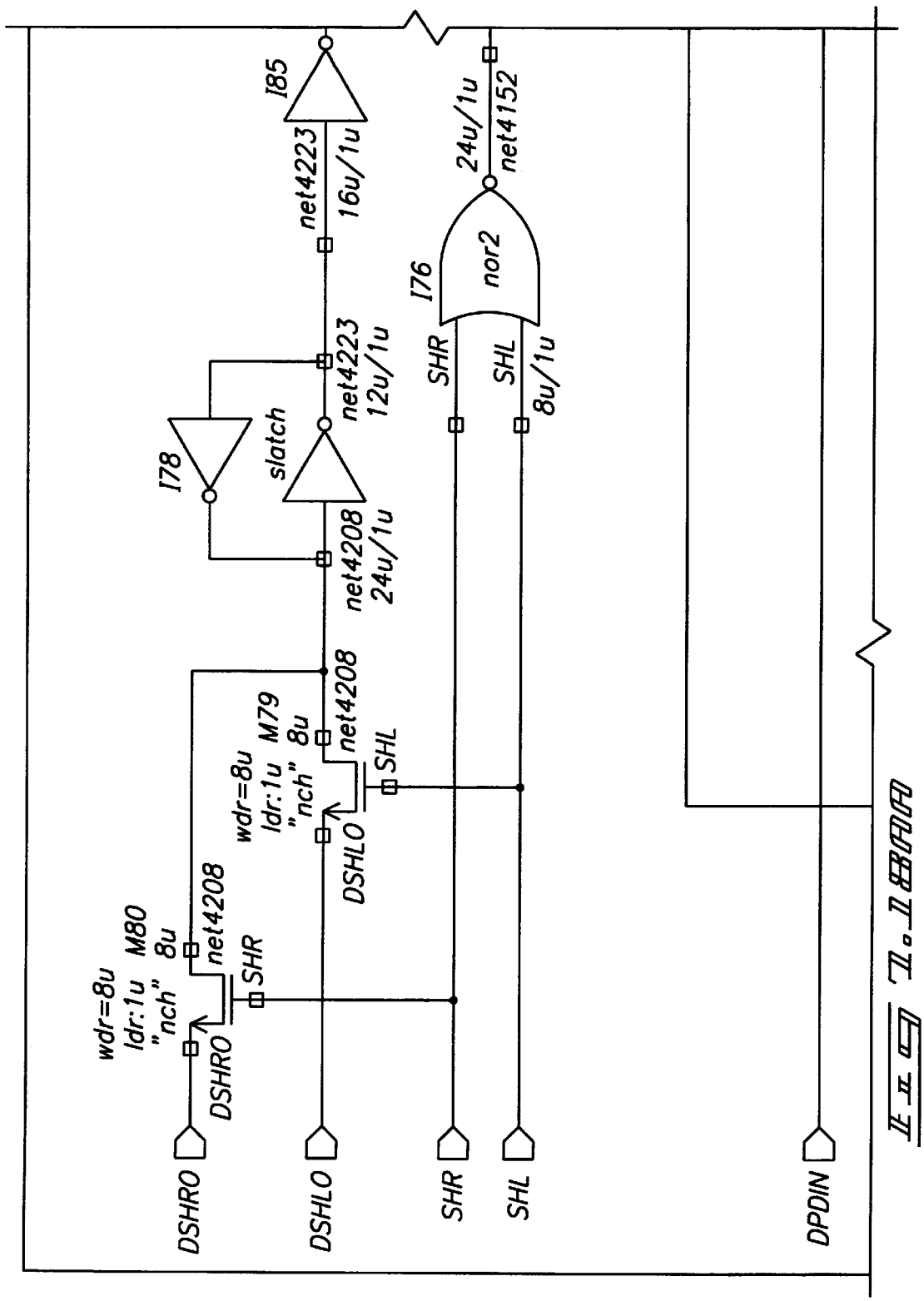
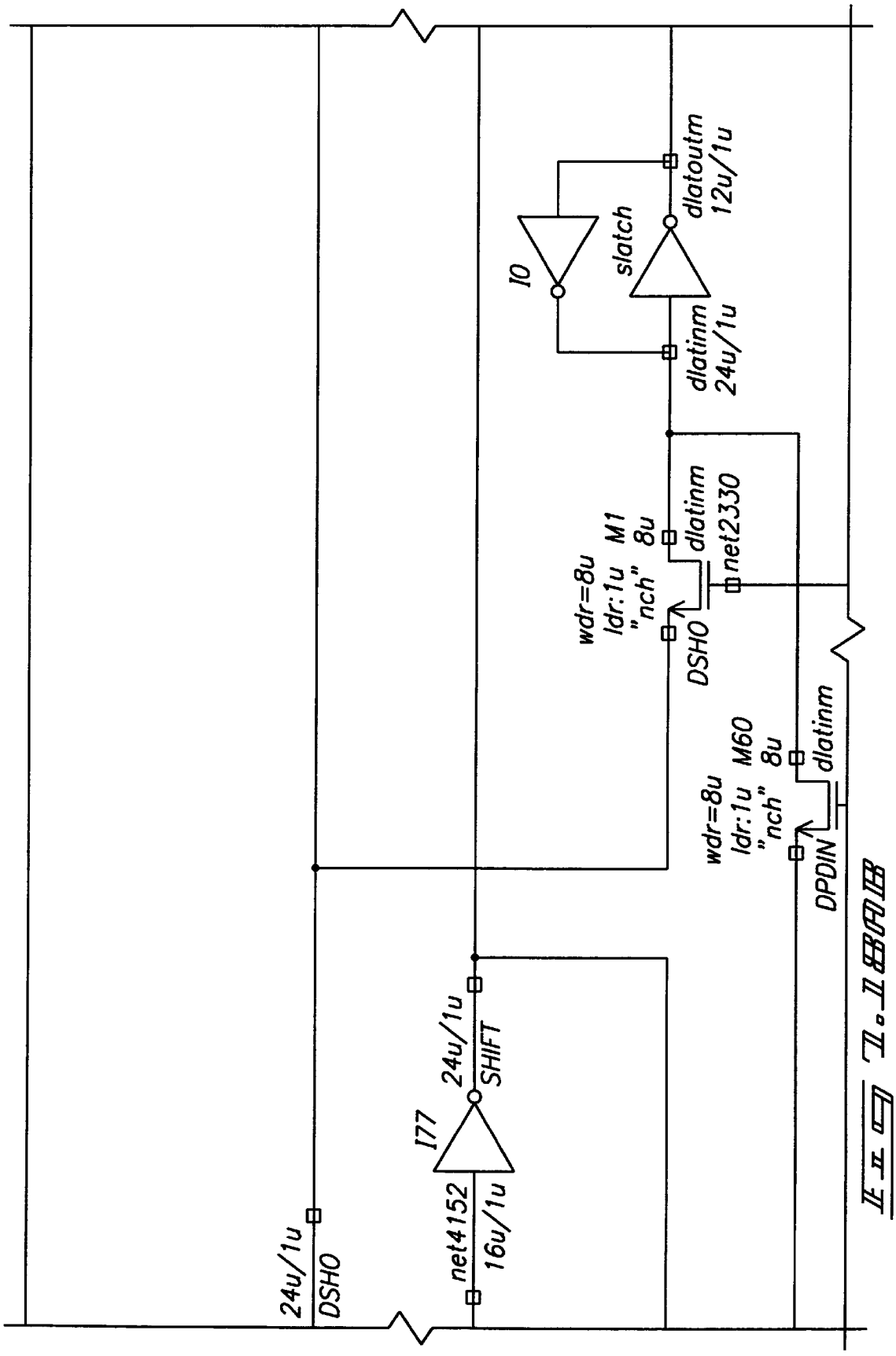
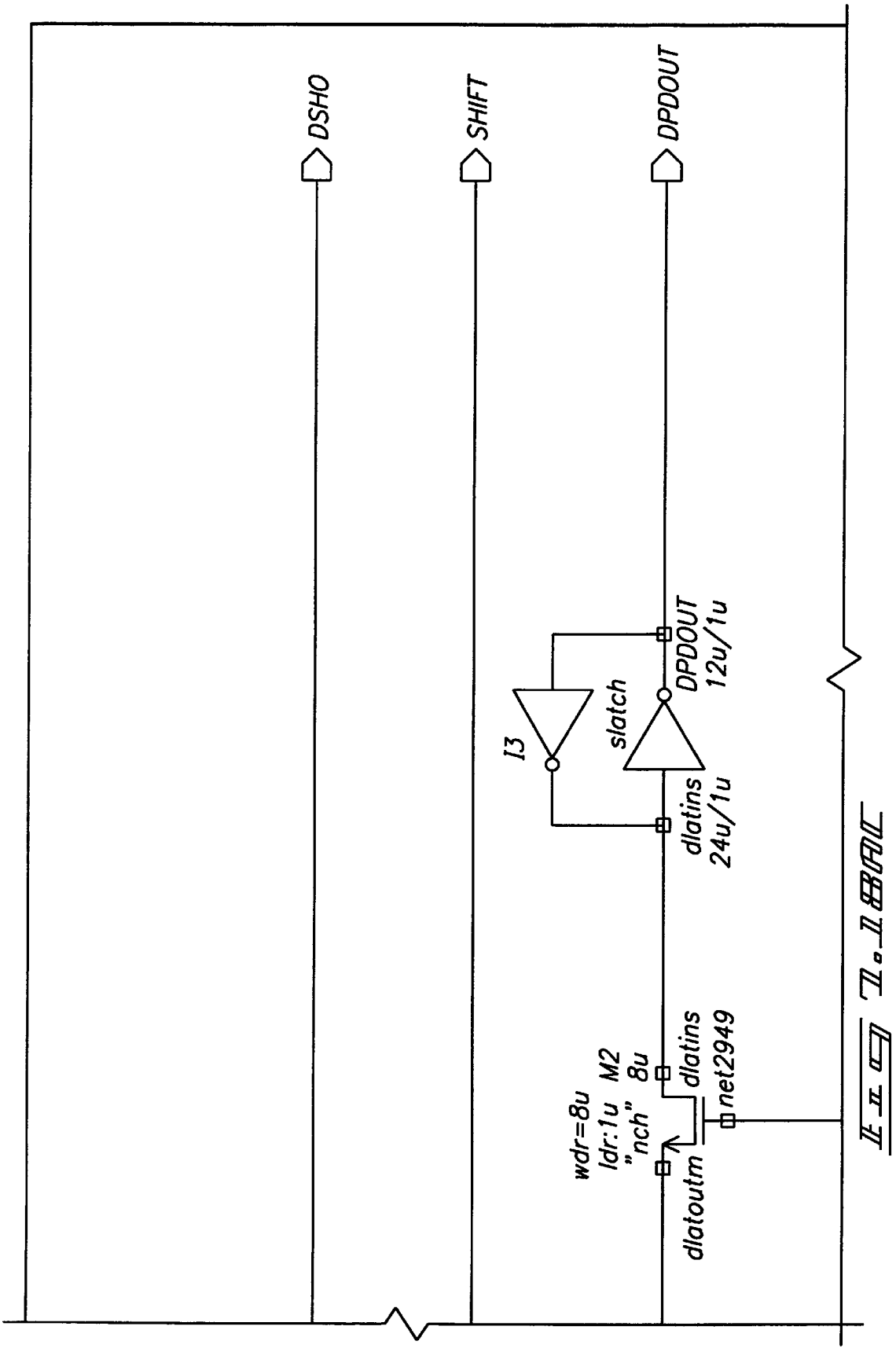


FIG. 718


I85
net4223
16u/1u
24u/1u
net4152
I76
nor2
SHR
SHL
8u/1u
net4223
12u/1u
I78
slatch
net4208
24u/1u
net4208
M79
8u
wdr=8u
ldr:1u
"nch"
SHL
DSHLO
net4208
M80
8u
wdr=8u
ldr:1u
"nch"
SHR
DSHRO
DSHRO
DSHLO
SHR
SHL
DPDIN

Фиг. 11.1085


I0
slatch
dlatoutm
12u/1u
dlatinm
24u/1u
wdr=8u
ldr:1u
"nch"
M1
8u
dlatinm
net2330
DSHO
wdr=8u
ldr:1u
"nch"
M60
8u
dlatinm
DPDIN
I77
24u/1u
SHIFT
net4152
16u/1u
24u/1u
DSHO


DSHO
SHIFT
DPDOUT
DPDOUT
12u/1u
slatch
I3
dlatins
24u/1u
dlatins
net2949
M2
8u
wdr=8u
ldr:1u
"nch"
dlatoutm

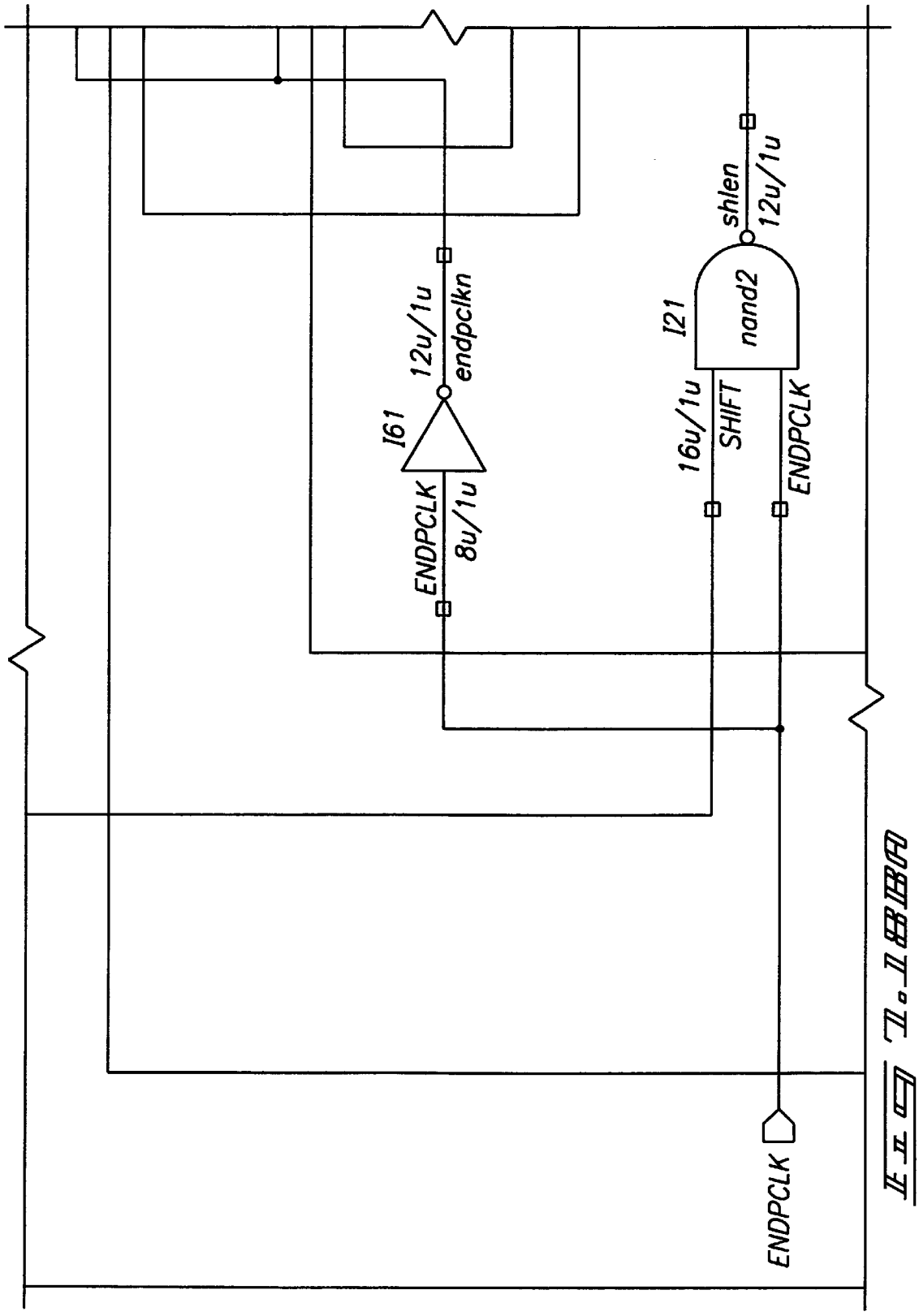

I61
12u/1u
endpclkn
ENDPCLK
8u/1u
I21
nand2
shlen
12u/1u
16u/1u
SHIFT
ENDPCLK
ENDPCLK

FIG. 1088

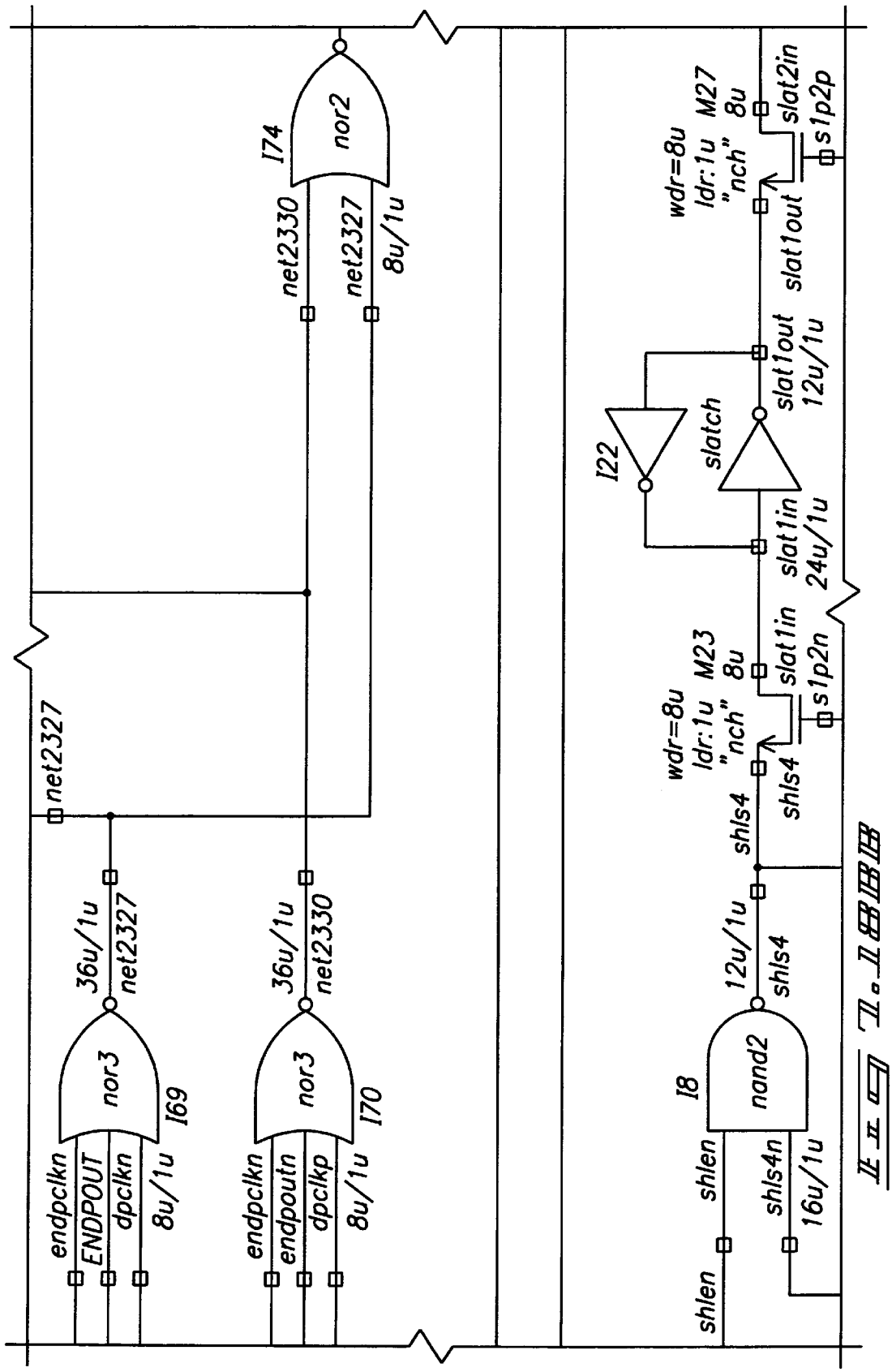

I74
nor2
net2330
net2327
8u/1u
net2327
36u/1u
net2327
nor3
I69
endpclkn
ENDPOUT
dpclkn
8u/1u
36u/1u
net2330
nor3
I70
endpclkn
endpoutn
dpclkp
8u/1u
wdr=8u
ldr:1u
"nch"
M27
8u
slat2in
s1p2p
slat1out
I22
slatch
slat1out
12u/1u
slat1in
24u/1u
wdr=8u
ldr:1u
"nch"
M23
8u
slat1in
s1p2n
shls4
shls4
12u/1u
shls4
I8
nand2
shlen
shlen
shls4n
16u/1u

FIG. 1130

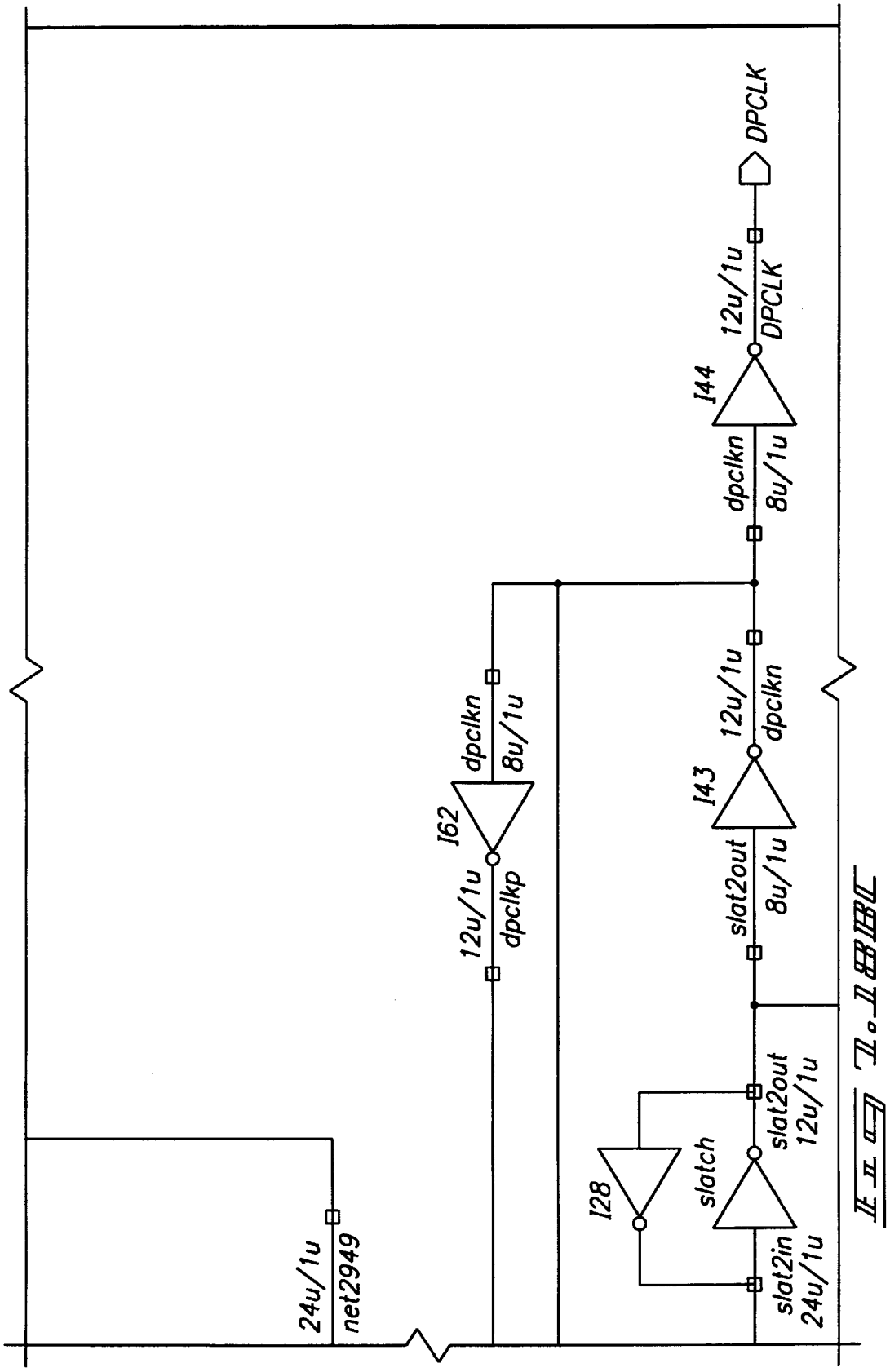

DPCLK
12u/1u
DPCLK
I44
dpclkn
8u/1u
12u/1u
dpclkn
I43
slat2out
8u/1u
dpclkn
8u/1u
I62
12u/1u
dpclkp
slat2out
12u/1u
I28
slatch
slat2in
24u/1u
24u/1u
net2949

FIG. 1102

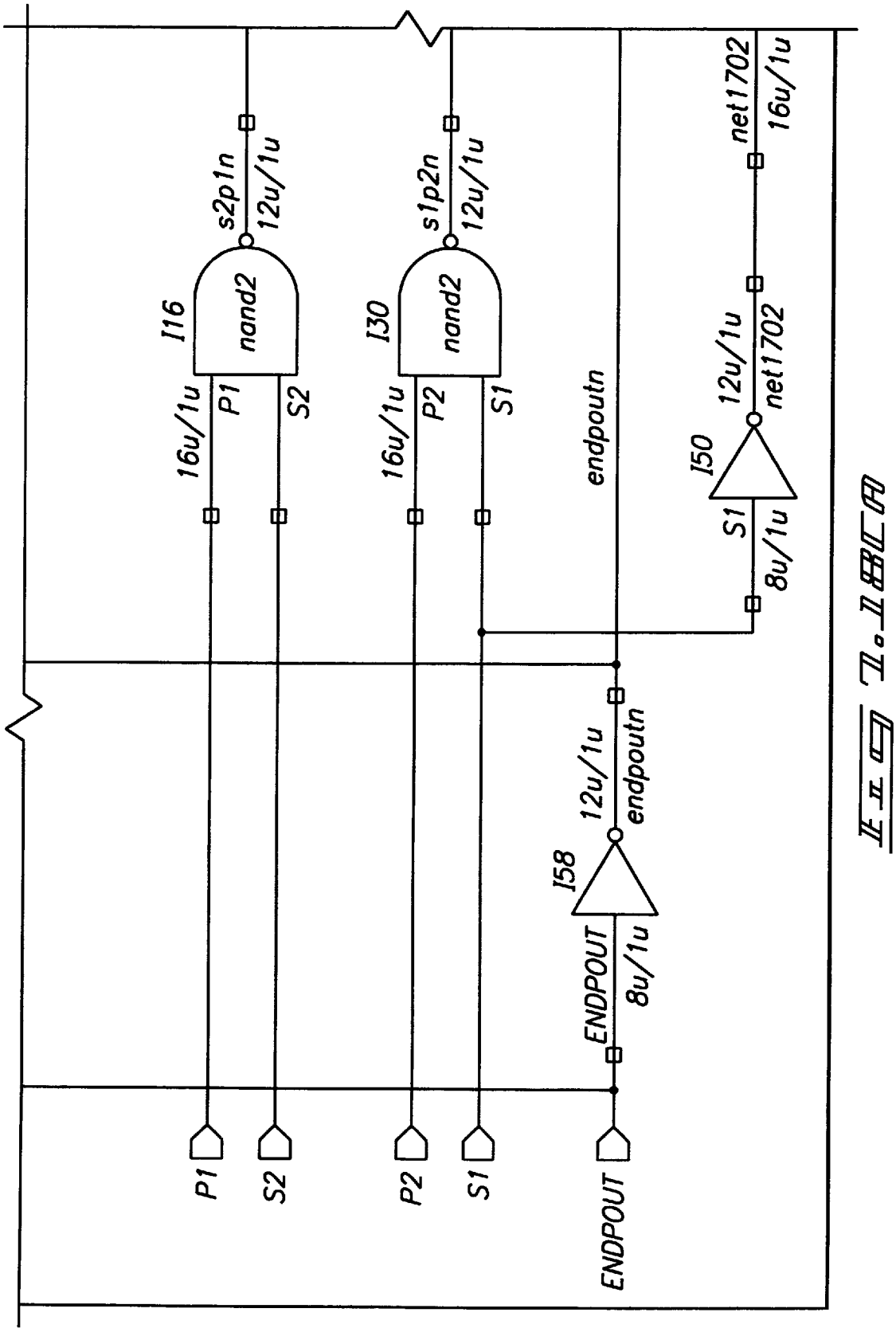

I16
nand2
s2p1n
12u/1u
16u/1u
P1
S2
I30
nand2
s1p2n
12u/1u
16u/1u
P2
S1
endpoutn
net1702
16u/1u
I50
12u/1u
net1702
S1
8u/1u
I58
12u/1u
endpoutn
ENDPOUT
8u/1u
P1
S2
P2
S1
ENDPOUT

FIG. 1091

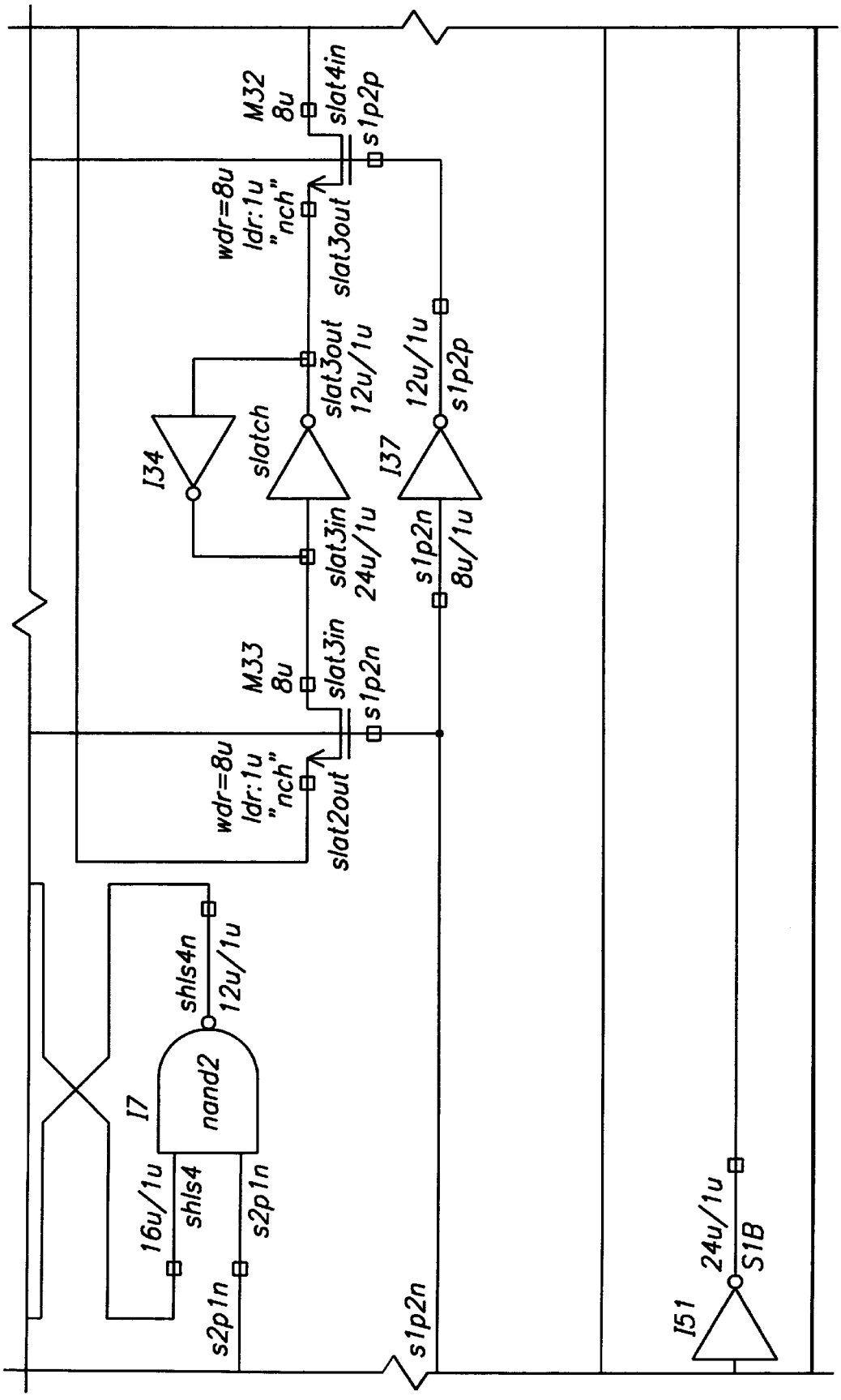

M32
8u
slat4in
s1p2p
wdr=8u
ldr:1u
"nch"
slat3out
slat3out
12u/1u
12u/1u
s1p2p
slatch
I34
I37
slat3in
24u/1u
s1p2n
8u/1u
M33
8u
slat3in
s1p2n
wdr=8u
ldr:1u
"nch"
slat2out
shls4n
12u/1u
I7
nand2
16u/1u
shls4
s2p1n
s2p1n
s1p2n
I51
24u/1u
S1B

FIG. 1130

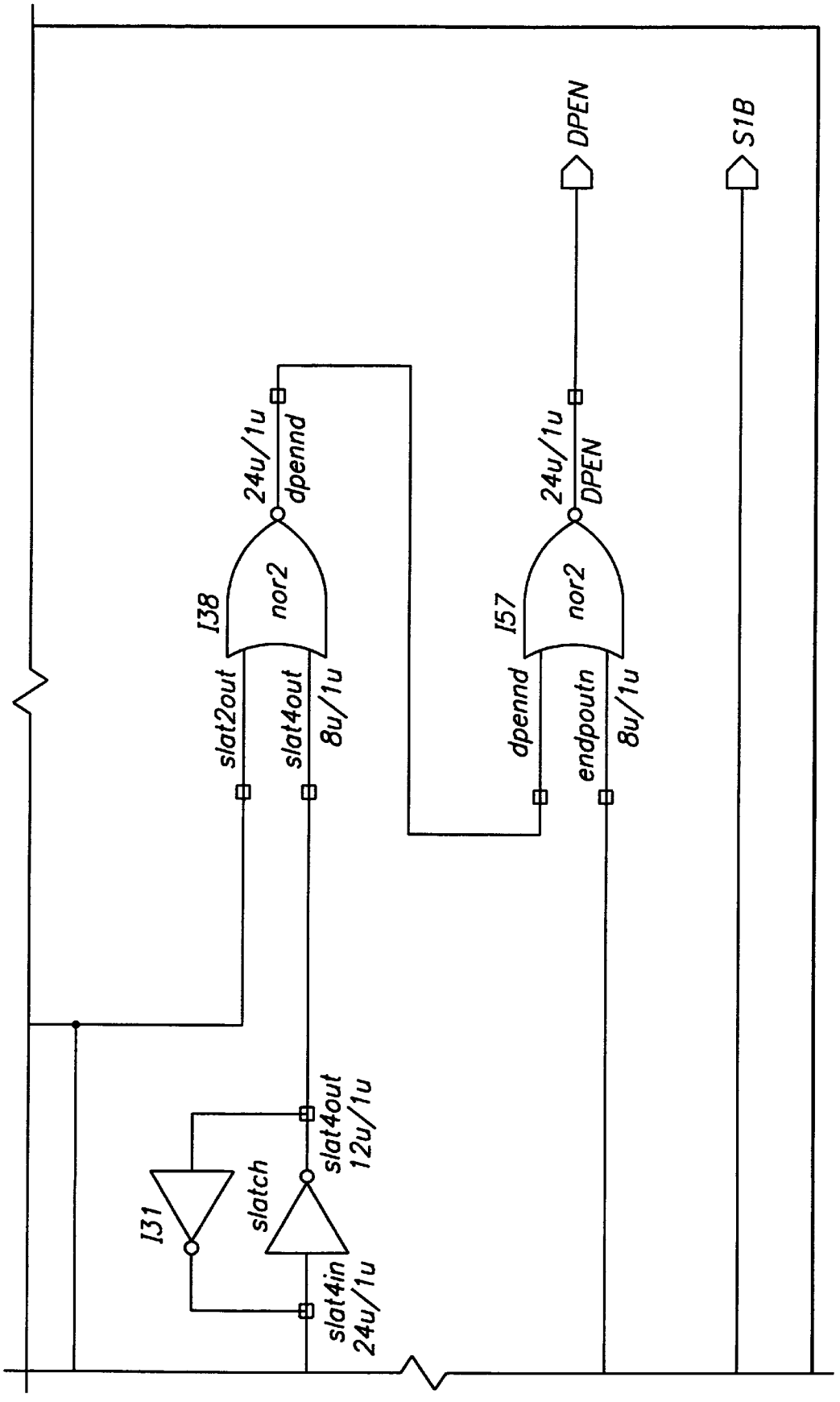

DPEN
S1B
24u/1u
dpennd
I38
nor2
slat2out
slat4out
8u/1u
24u/1u
DPEN
I57
nor2
dpennd
endpoutn
8u/1u
slat4out
12u/1u
I31
slatch
slat4in
24u/1u

FIG. 1131

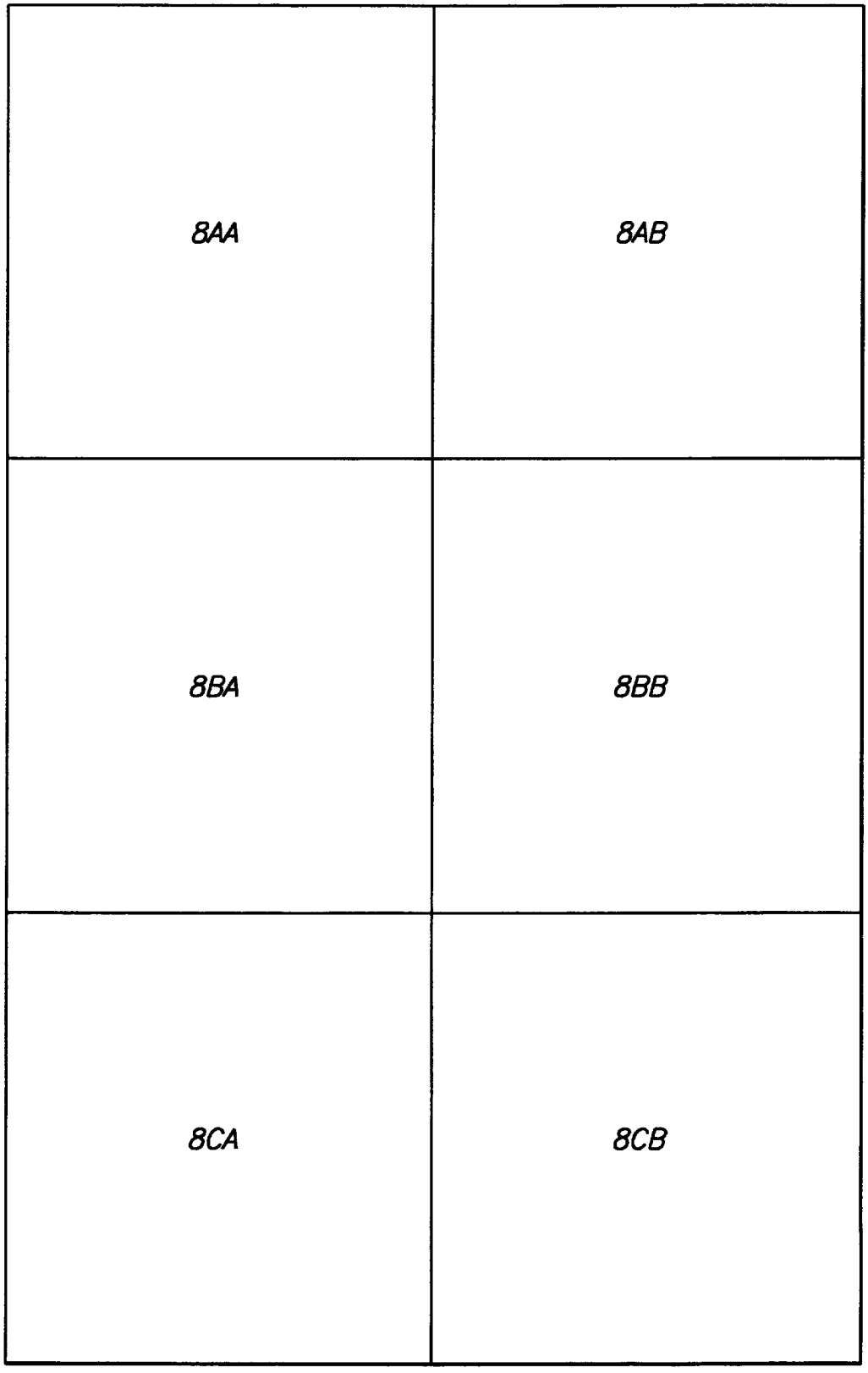
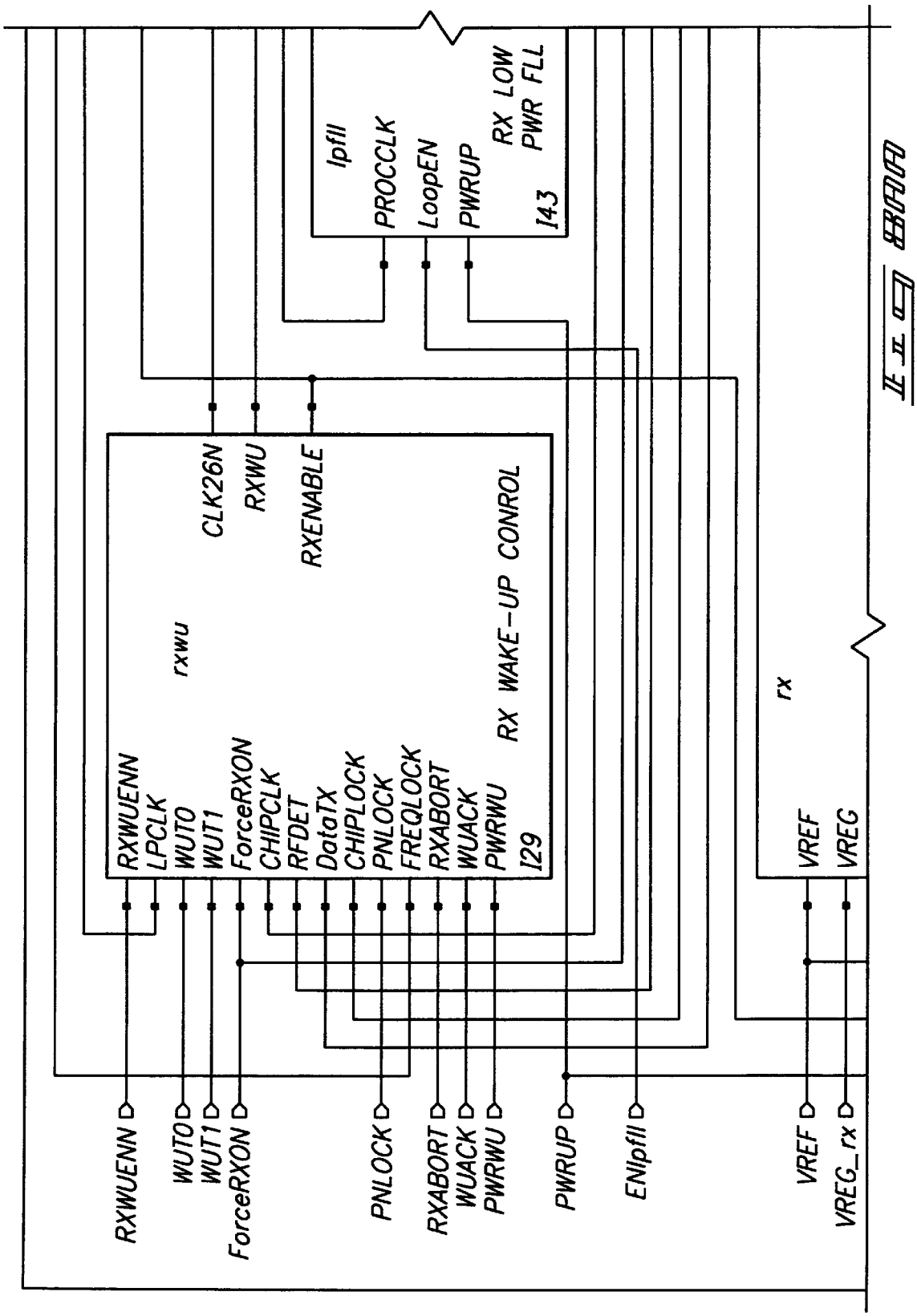
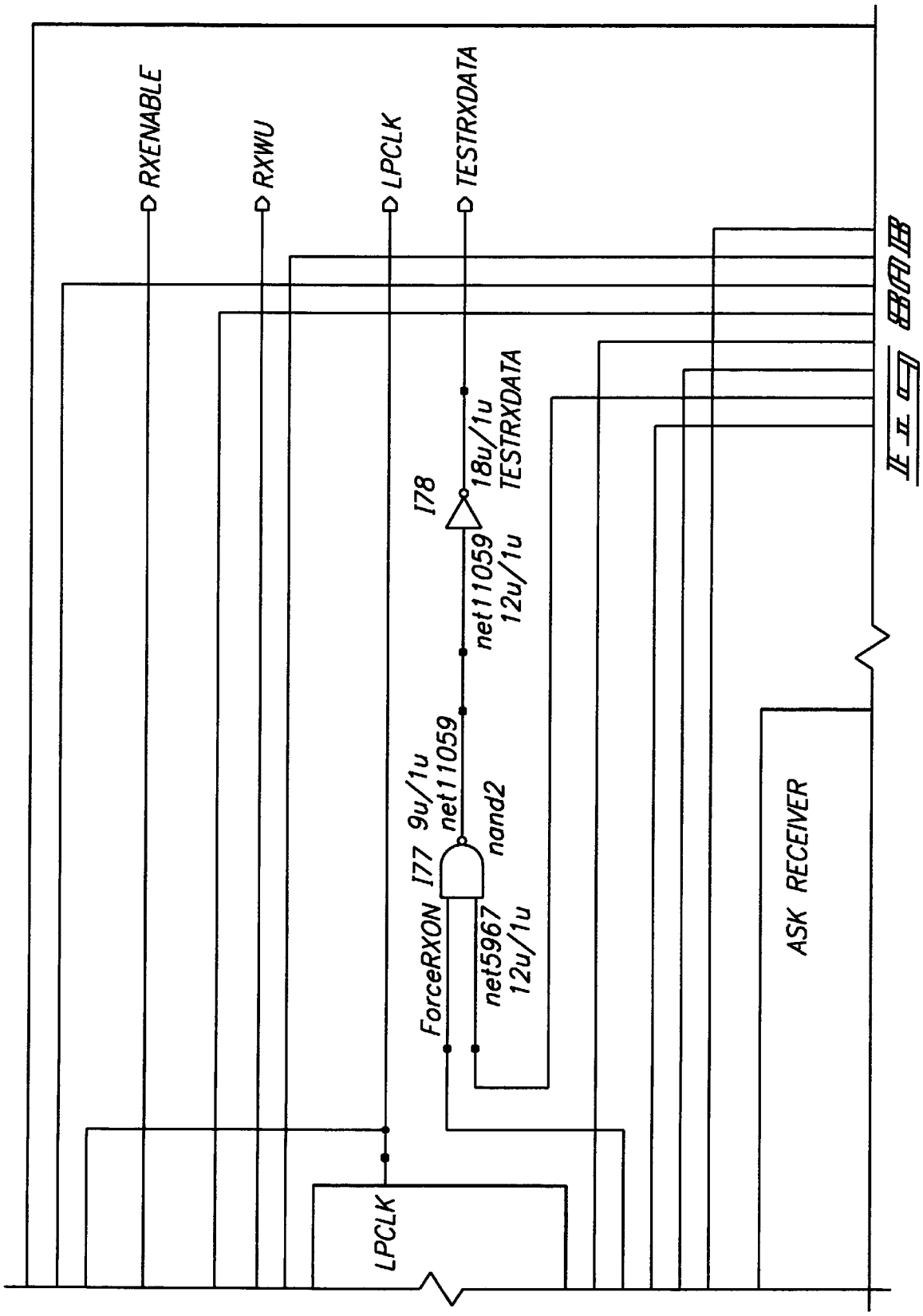
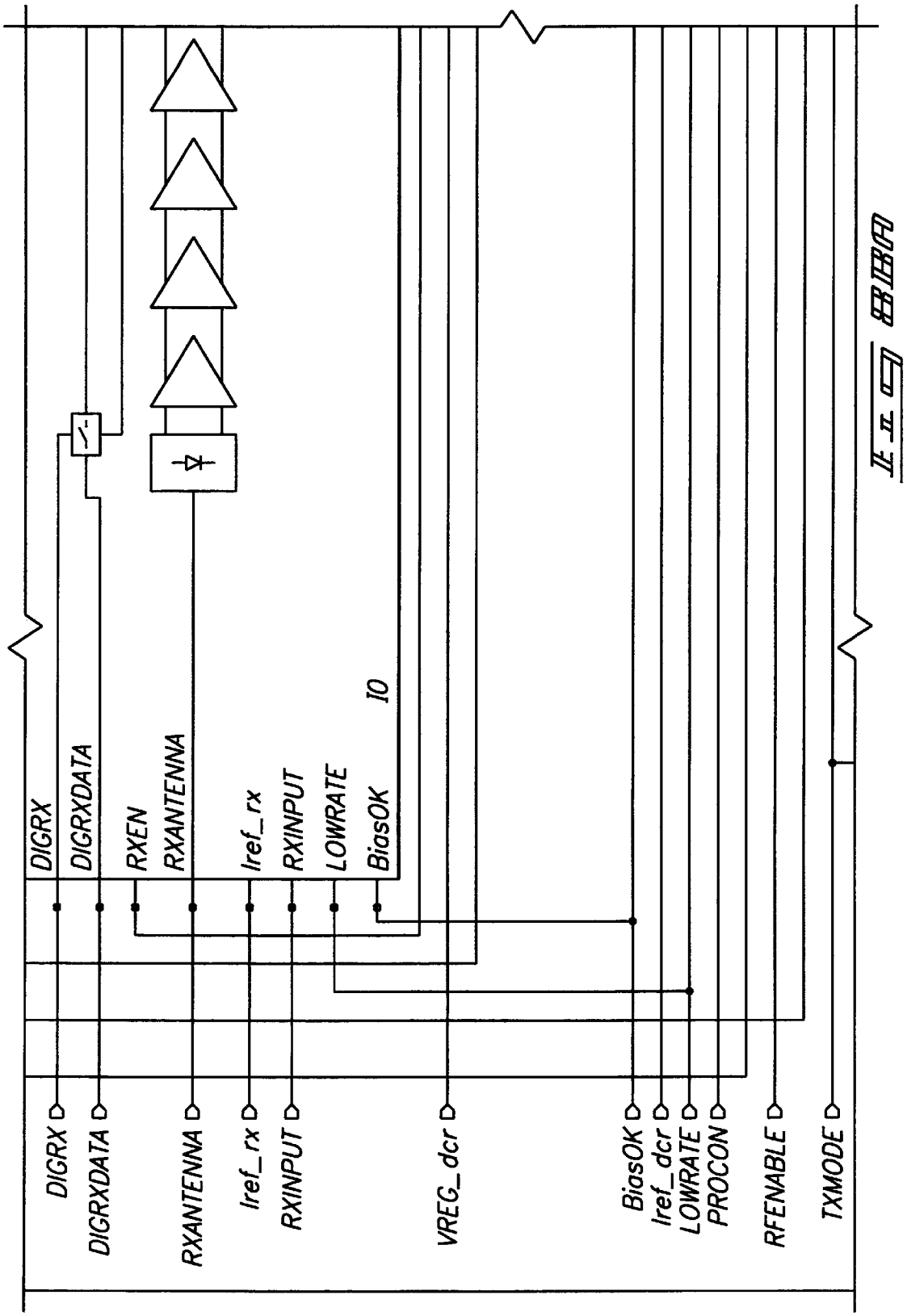
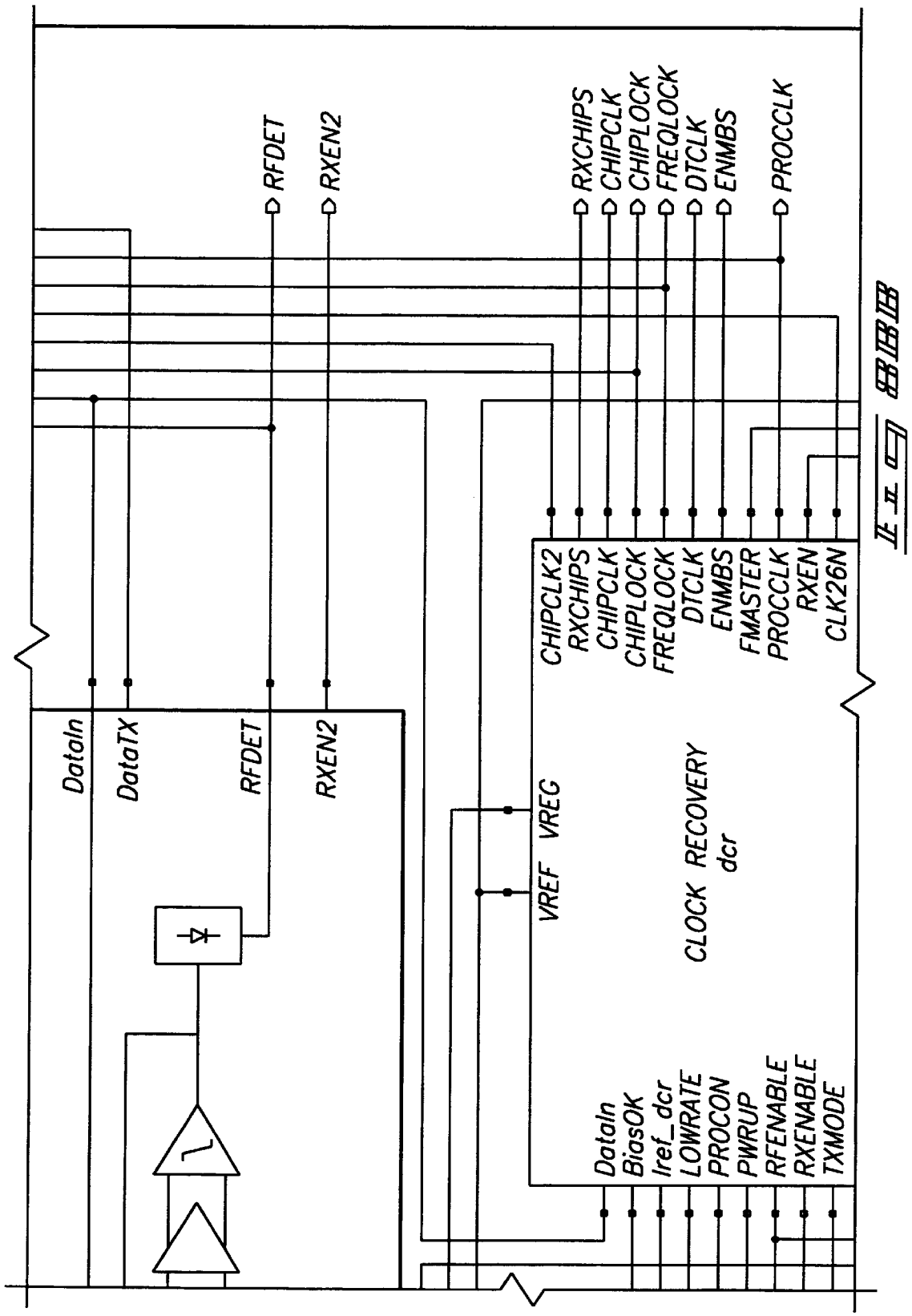


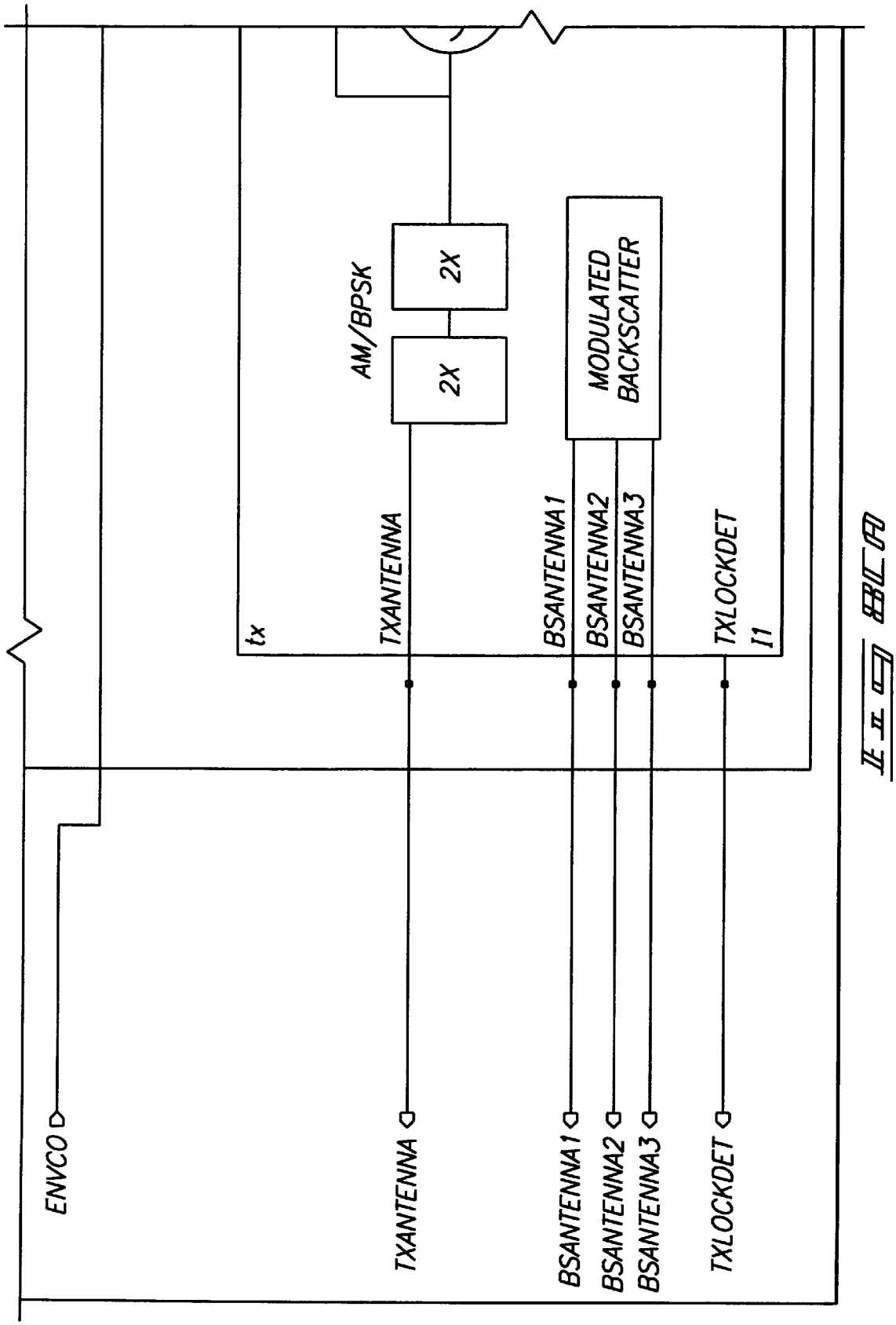
Fig 88


RXWUENN
WUT0
WUT1
ForceRXON
PNLOCK
RXABORT
WUACK
PWRWU
PWRUP
ENIpfll
VREF
VREG_rx
RXWUENN
LPCLK
WUT0
WUT1
ForceRXON
CHIPCLK
RFDET
DataTX
CHIPLOCK
PNLOCK
FREQLOCK
RXABORT
WUACK
PWRWU
I29
rxwu
RX WAKE-UP CONROL
CLK26N
RXWU
RXENABLE
VREF
VREG
rx
Ipfll
PROCCLK
LoopEN
PWRUP
I43
RX LOW PWR FLL


RXENABLE
RXWU
LPCLK
TESTRXDATA
I78
18u/1u
TESTRXDATA
net11059
12u/1u
I77
9u/1u
net11059
nand2
ForceRXON
net5967
12u/1u
LPCLK
ASK RECEIVER


DIGRX
DIGRXDATA
RXEN
RXANTENNA
Iref_rx
RXINPUT
LOWRATE
BiasOK
IO
DIGRX
DIGRXDATA
RXANTENNA
Iref_rx
RXINPUT
VREG_dcr
BiasOK
Iref_dcr
LOWRATE
PROCON
RFENABLE
TXMODE


RFDET
RXEN2
RXCHIPS
CHIPCLK
CHIPLOCK
FREQLOCK
DTCLK
ENMBS
PROCCLK
CHIPCLK2
RXCHIPS
CHIPCLK
CHIPLOCK
FREQLOCK
DTCLK
ENMBS
FMASTER
PROCCLK
RXEN
CLK26N
DataIn
DataTX
RFDET
RXEN2
VREF VREG
CLOCK RECOVERY
dcr
DataIn
BiasOK
Iref_dcr
LOWRATE
PROCON
PWRUP
RFENABLE
RXENABLE
TXMODE


ENVCO
TXANTENNA
BSANTENNA1
BSANTENNA2
BSANTENNA3
TXLOCKDET
tx
TXANTENNA
BSANTENNA1
BSANTENNA2
BSANTENNA3
I1
TXLOCKDET
AM/BPSK
2X
2X
MODULATED
BACKSCATTER

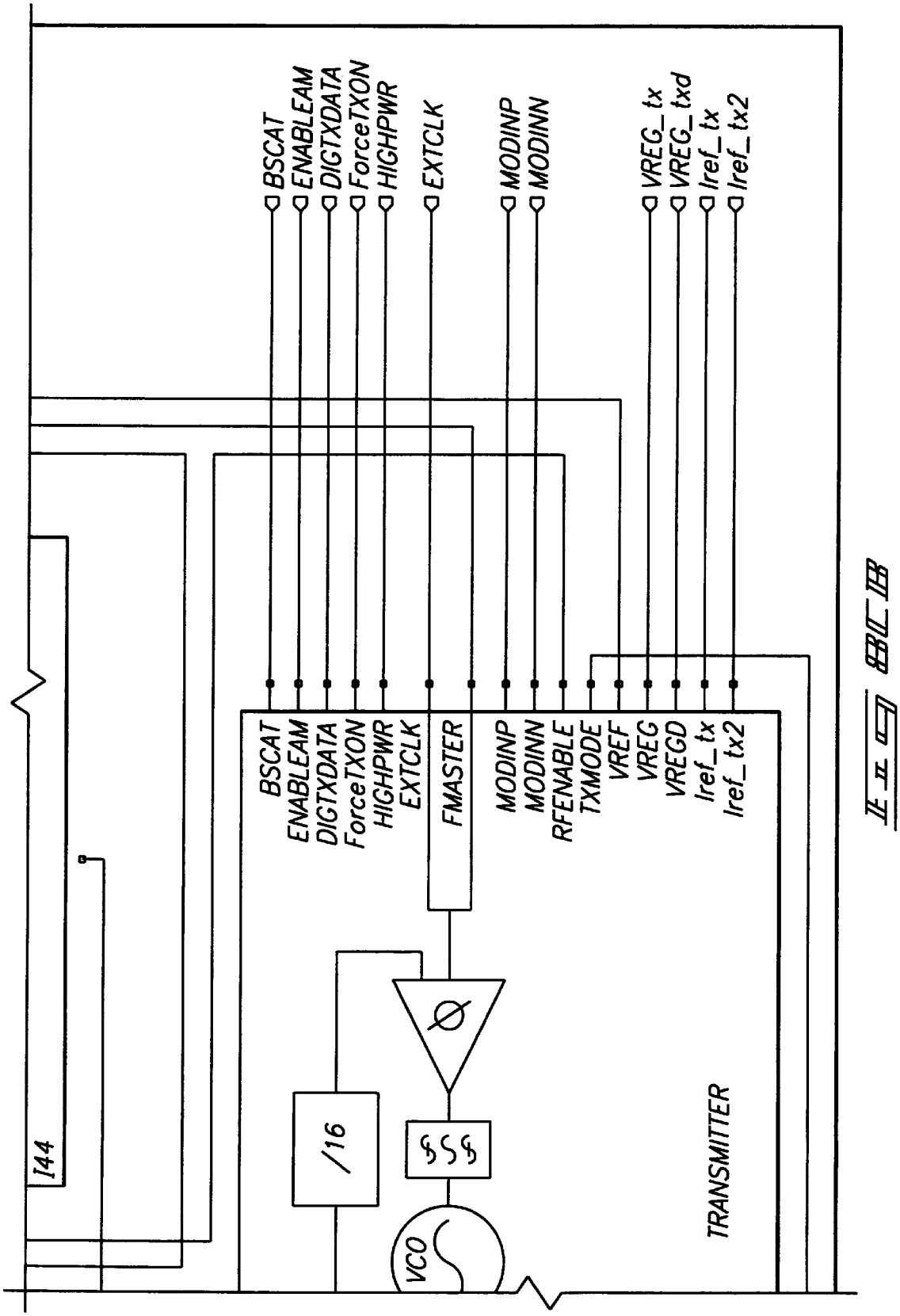

BSCAT
ENABLEAM
DIGTXDATA
ForceTXON
HIGHPWR
EXTCLK
MODINP
MODINN
VREG_tx
VREG_txd
Iref_tx
Iref_tx2
BSCAT
ENABLEAM
DIGTXDATA
ForceTXON
HIGHPWR
EXTCLK
FMASTER
MODINP
MODINN
RFENABLE
TXMODE
VREF
VREG
VREGD
Iref_tx
Iref_tx2
144
/16
VCO
TRANSMITTER

FIG. 88C

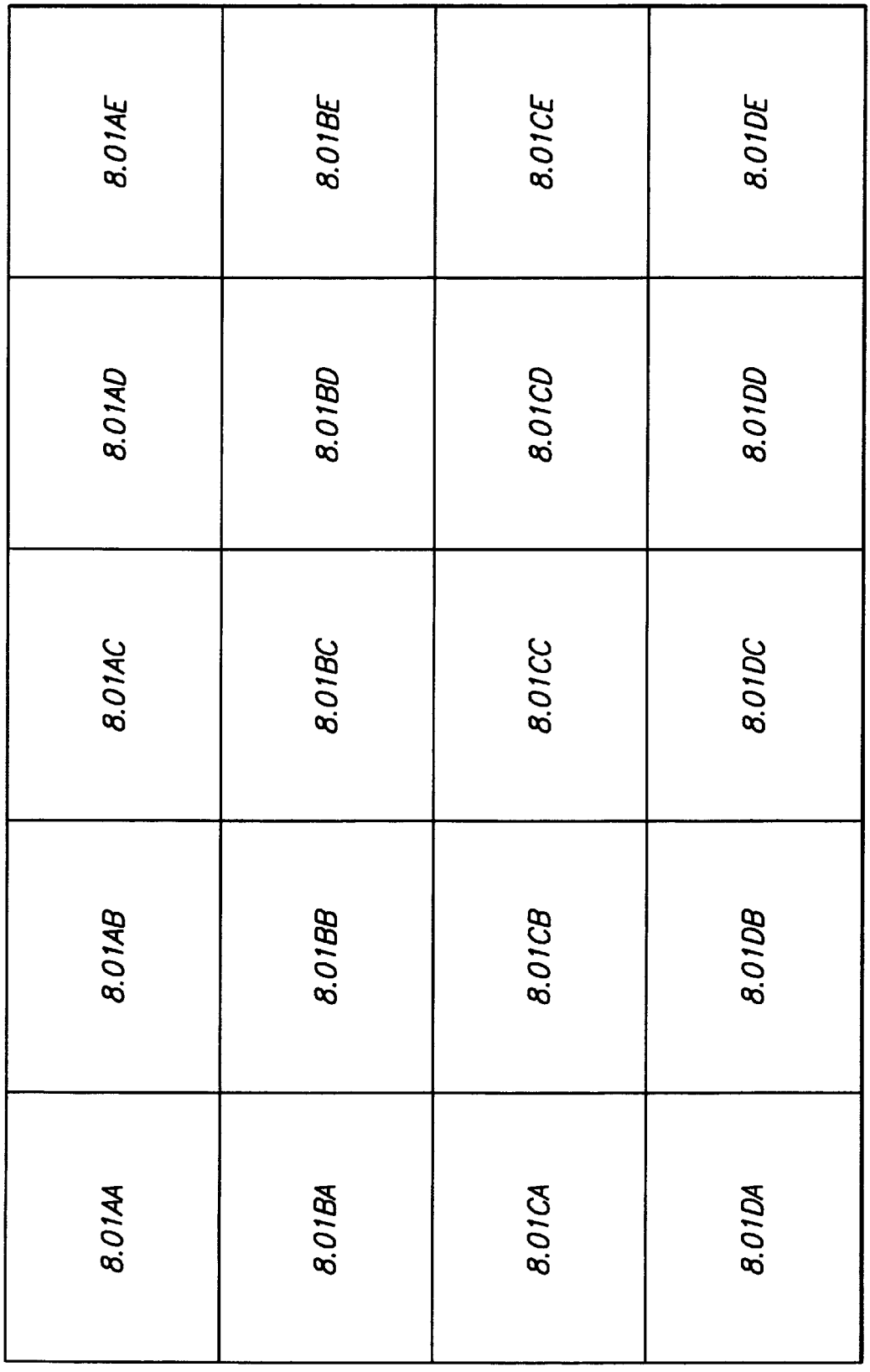

8.01AE
8.01BE
8.01CE
8.01DE
8.01AD
8.01BD
8.01CD
8.01DD
8.01AC
8.01BC
8.01CC
8.01DC
8.01AB
8.01BB
8.01CB
8.01DB
8.01AA
8.01BA
8.01CA
8.01DA

FIG. 8.01

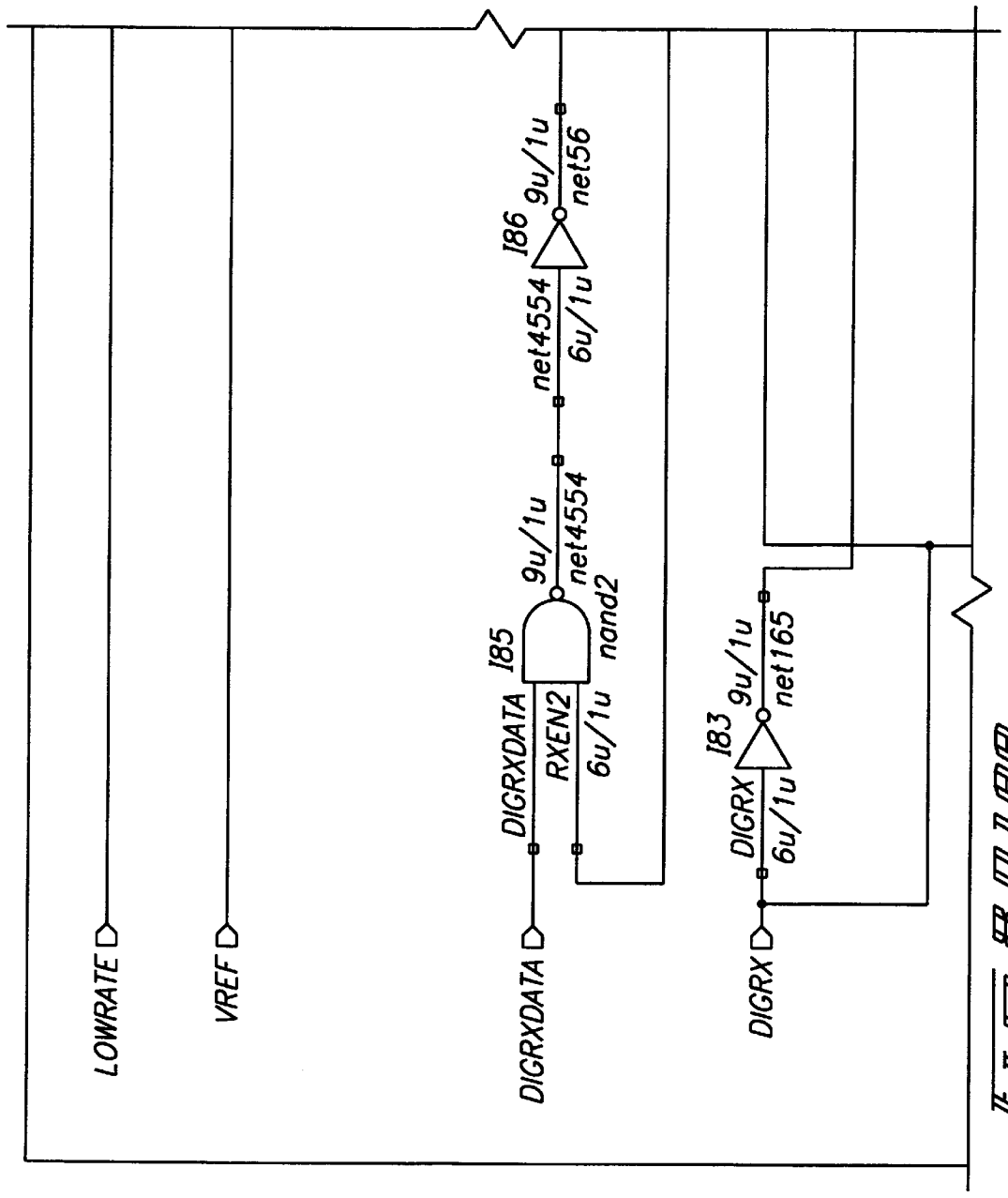
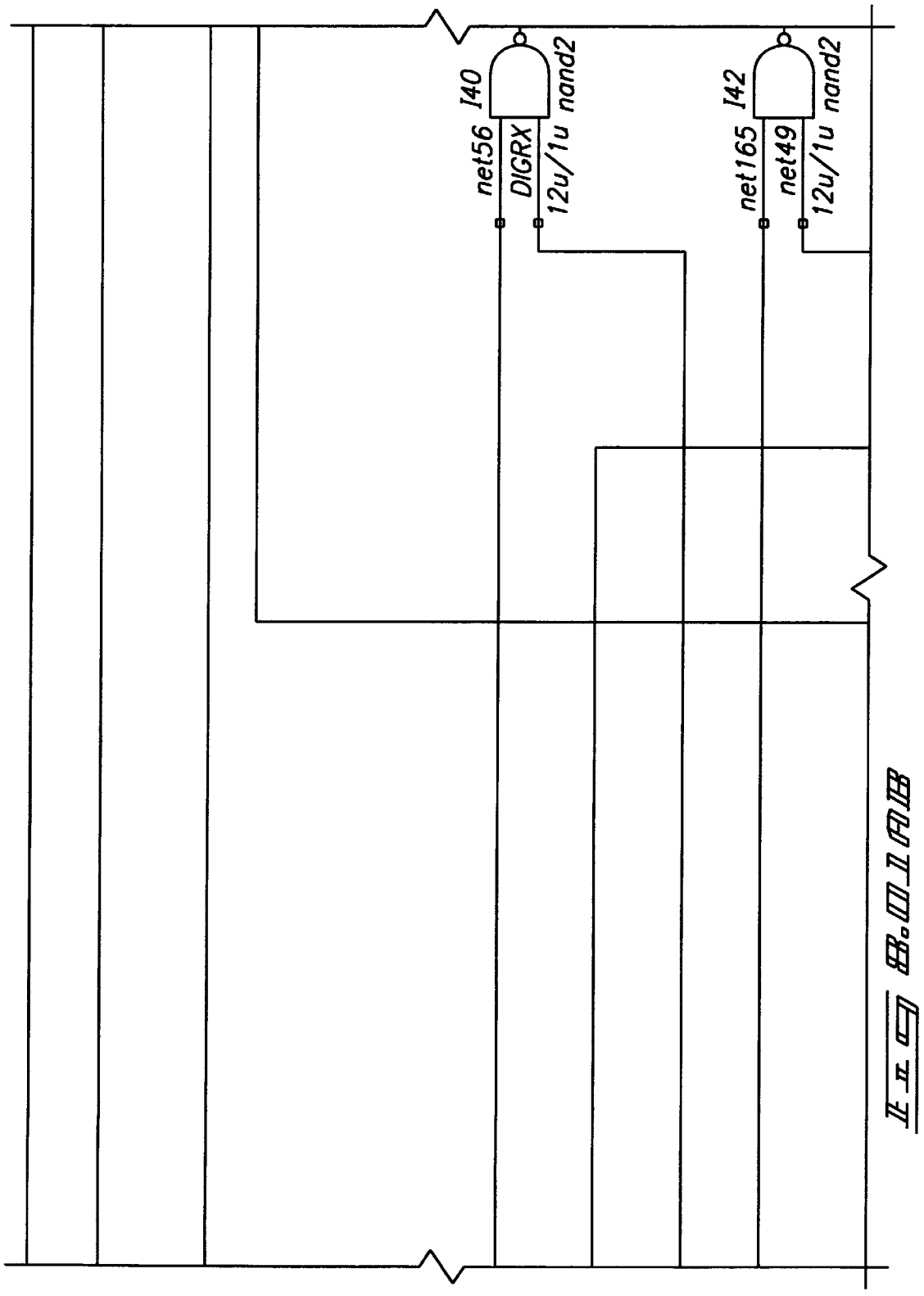
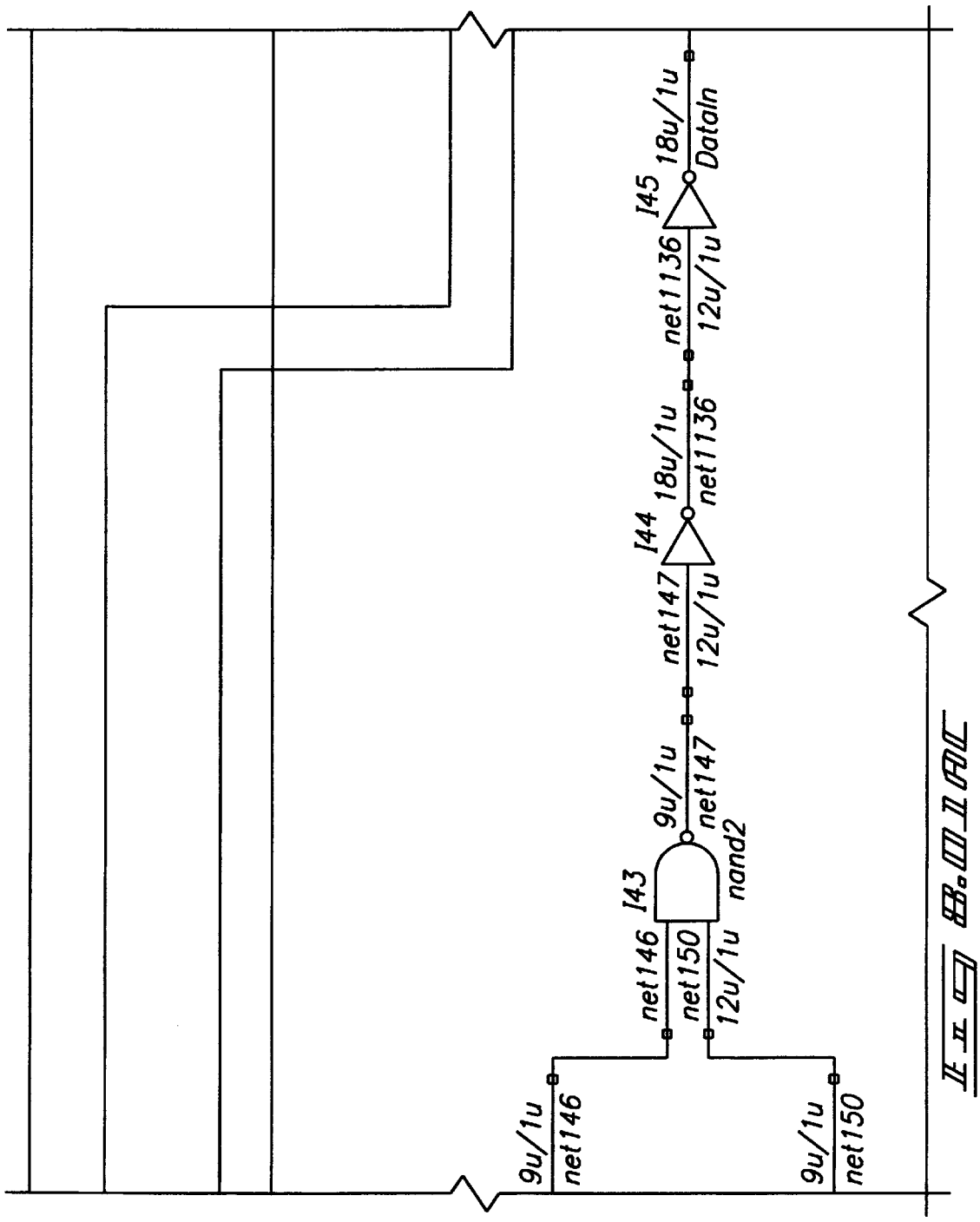

LOWRATE
VREF
DIGRXDATA
DIGRX
I85
nand2
9u/1u
net4554
RXEN2
6u/1u
I86
net56
net4554
I83
net165
DIGRX

FIG. 1102


I40
nand2
net56
DIGRX
12u/1u
I42
nand2
net165
net49
12u/1u


I45
18u/1u
DataIn
net1136
12u/1u
I44
18u/1u
net1136
net147
12u/1u
I43
9u/1u
net147
nand2
net146
net150
12u/1u
9u/1u
net146
9u/1u
net150

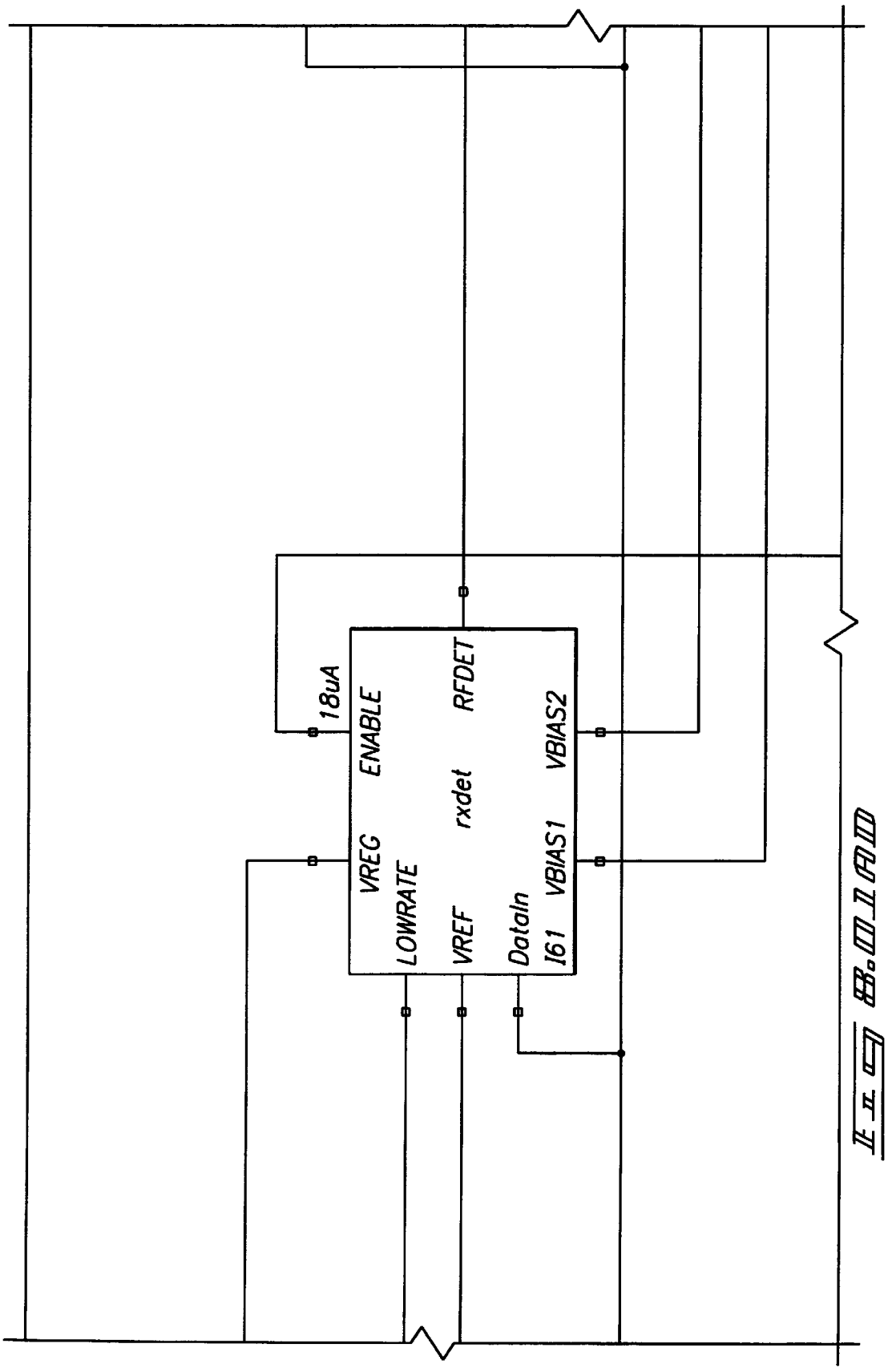
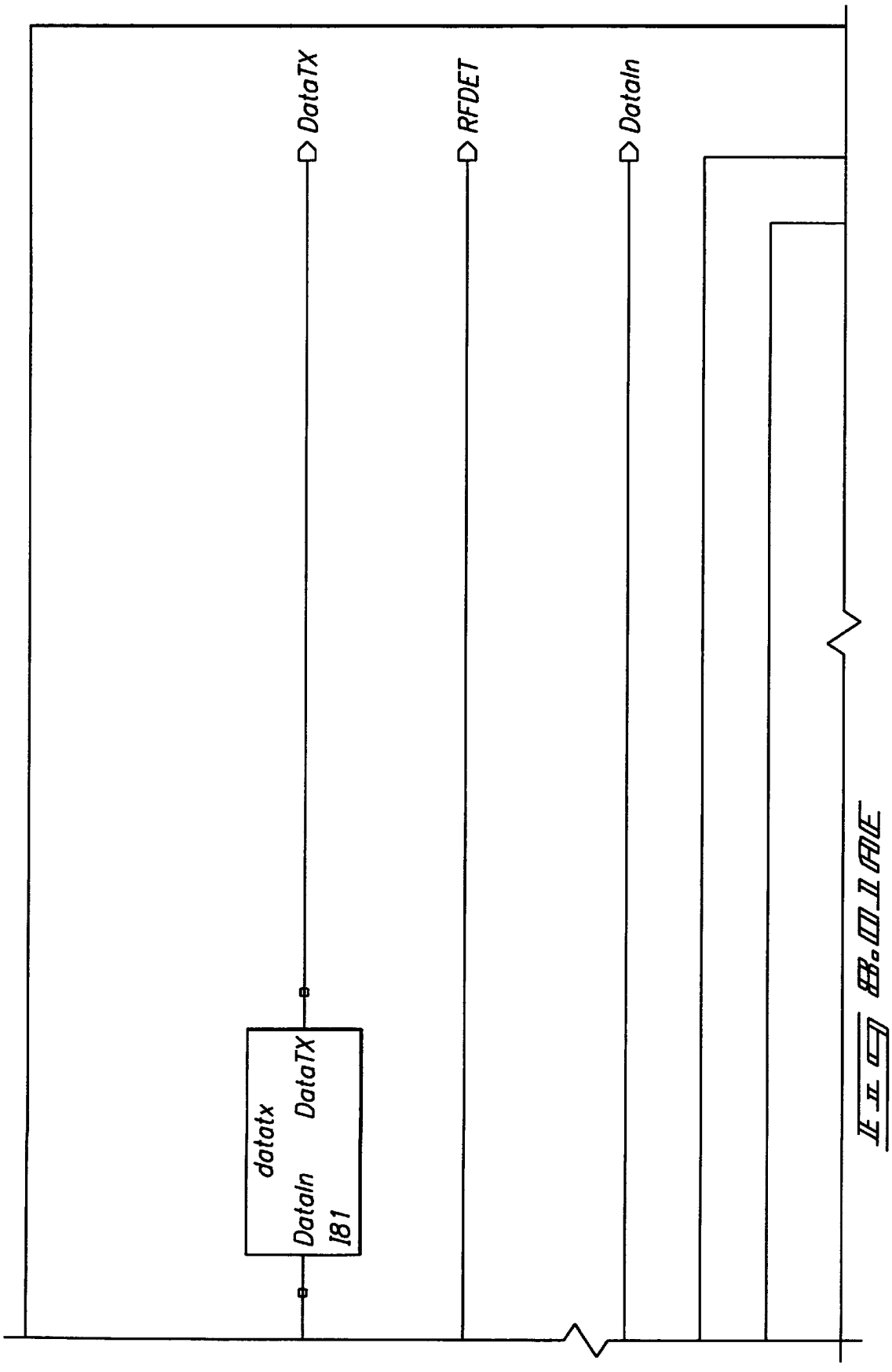

18uA
ENABLE
RFDET
VREG
rxdet
VBIAS2
LOWRATE
VREF
DataIn
I61
VBIAS1

FIG. 88.011A


DataTX
RFDET
DataIn
datatx
DataTX
DataIn
181

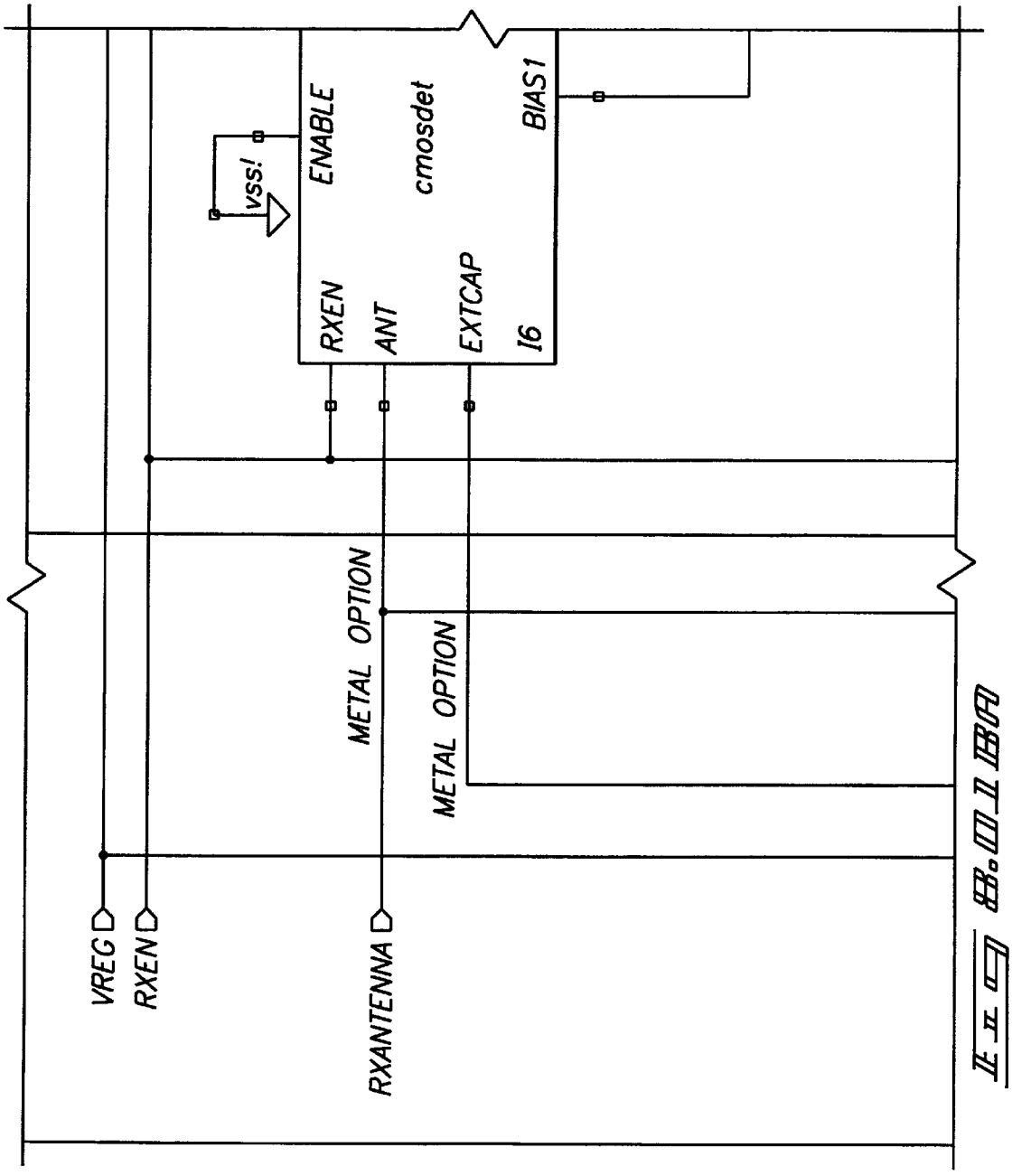

ENABLE
cmosdet
BIAS1
vss!
RXEN
ANT
EXTCAP
I6
METAL OPTION
METAL OPTION
VREG
RXEN
RXANTENNA

FIG. 88.011BA

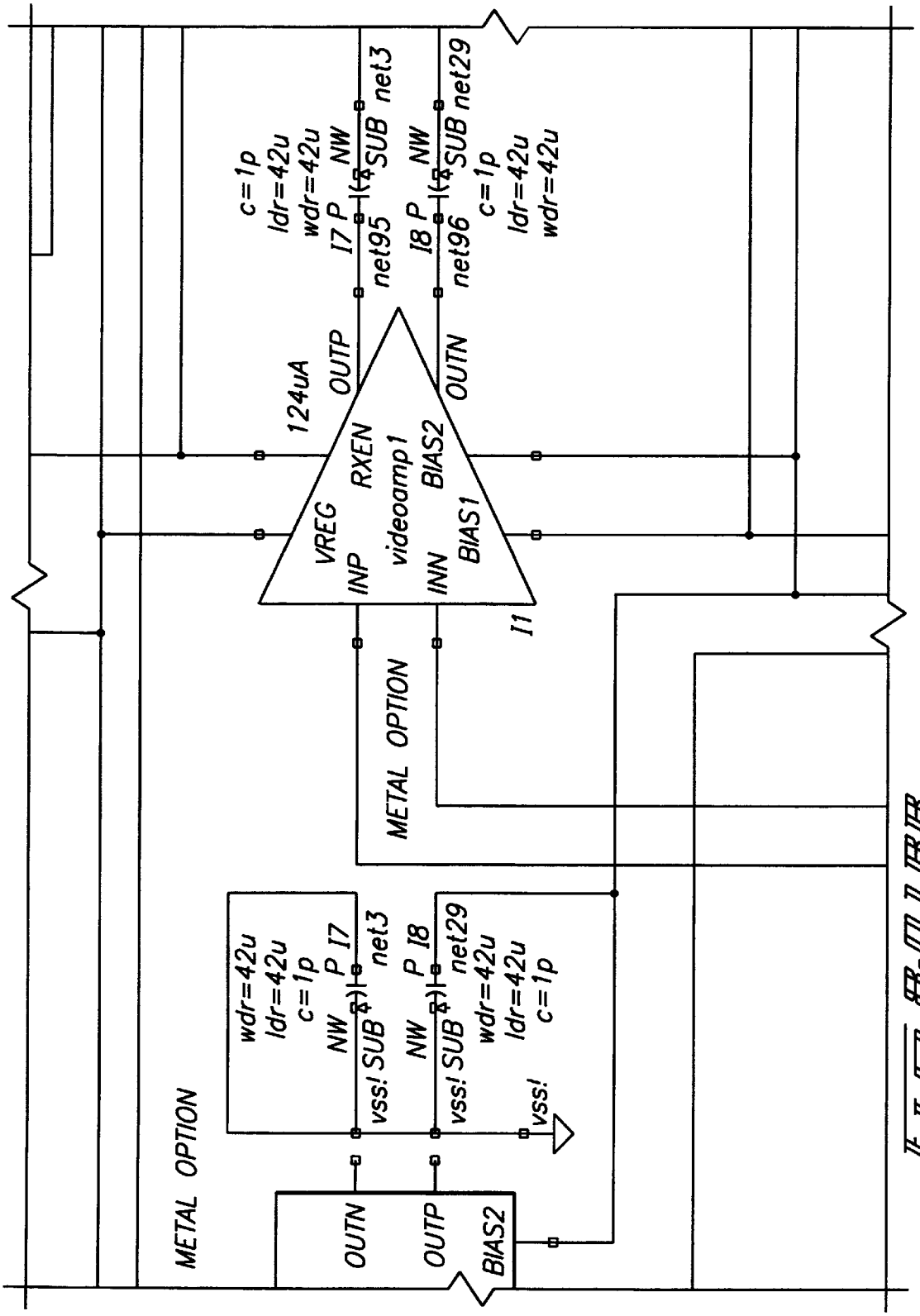

c=1p
ldr=42u
wdr=42u
NW
I7 P
SUB net3
net95
I8 P
NW
SUB net29
net96
c=1p
ldr=42u
wdr=42u
124uA
OUTP
OUTN
VREG
RXEN
videoamp1
BIAS2
INP
INN
BIAS1
I1
METAL OPTION
wdr=42u
ldr=42u
c=1p
NW
P I7
vss! SUB
net3
NW
P I8
vss! SUB
net29
wdr=42u
ldr=42u
c=1p
vss!
METAL OPTION
OUTN
OUTP
BIAS2

FIG 89.011

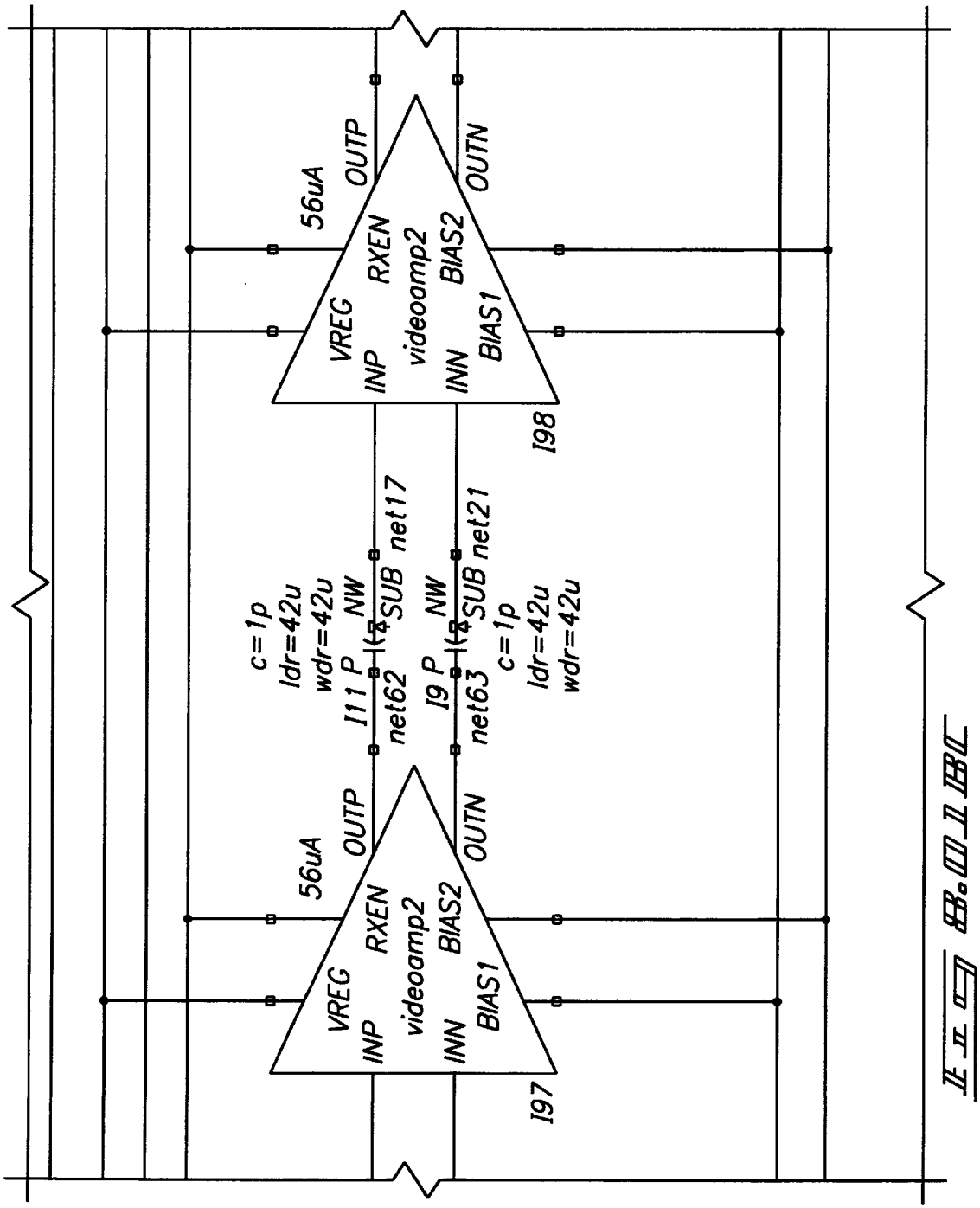

56uA
OUTP
OUTN
RXEN
BIAS2
VREG
videoamp2
INP
INN
BIAS1
I98
c=1p
ldr=42u
wdr=42u
NW
SUB
net17
net21
I11 P
I9 P
net62
net63
I97

FIG. 1109

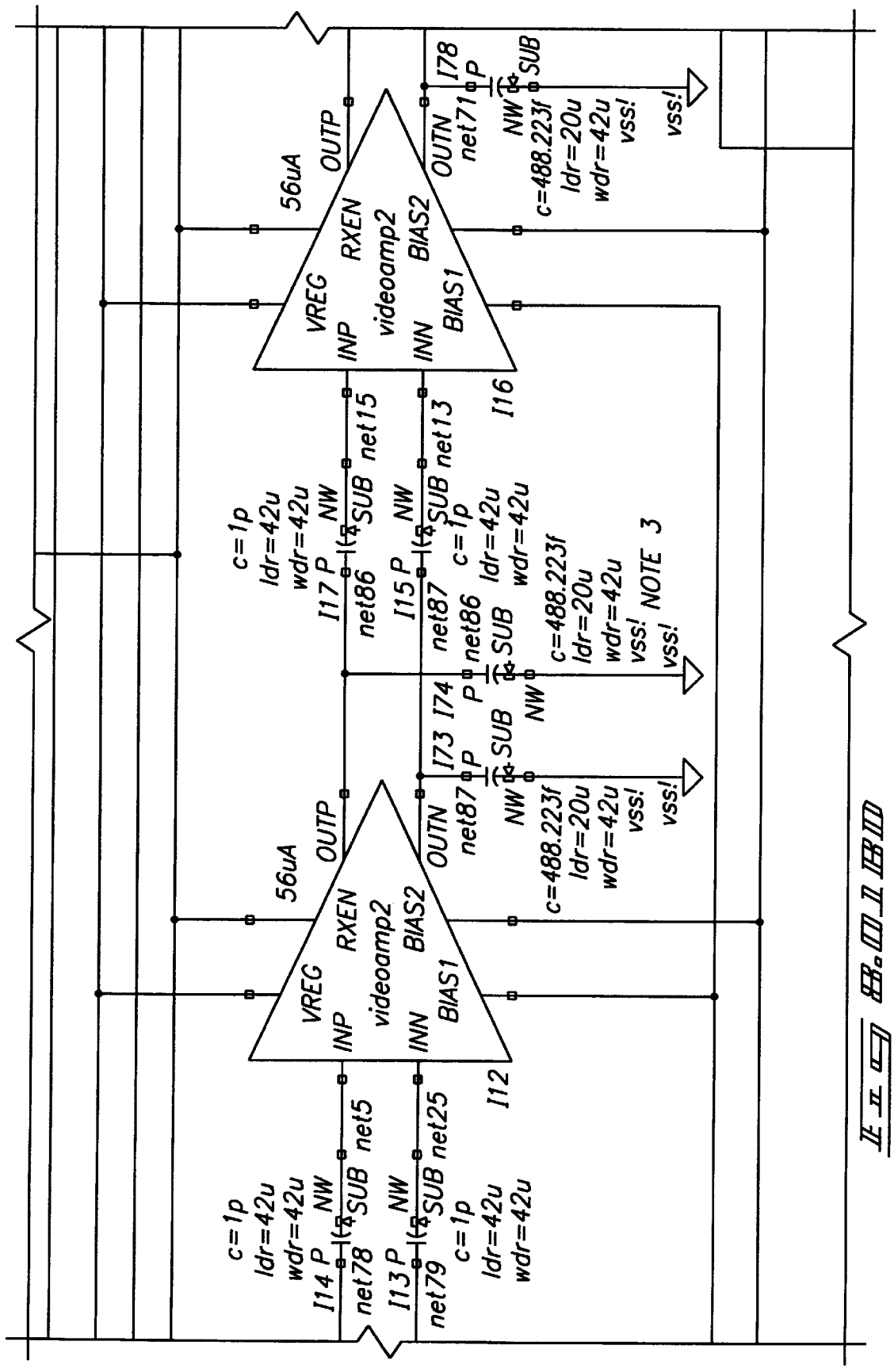
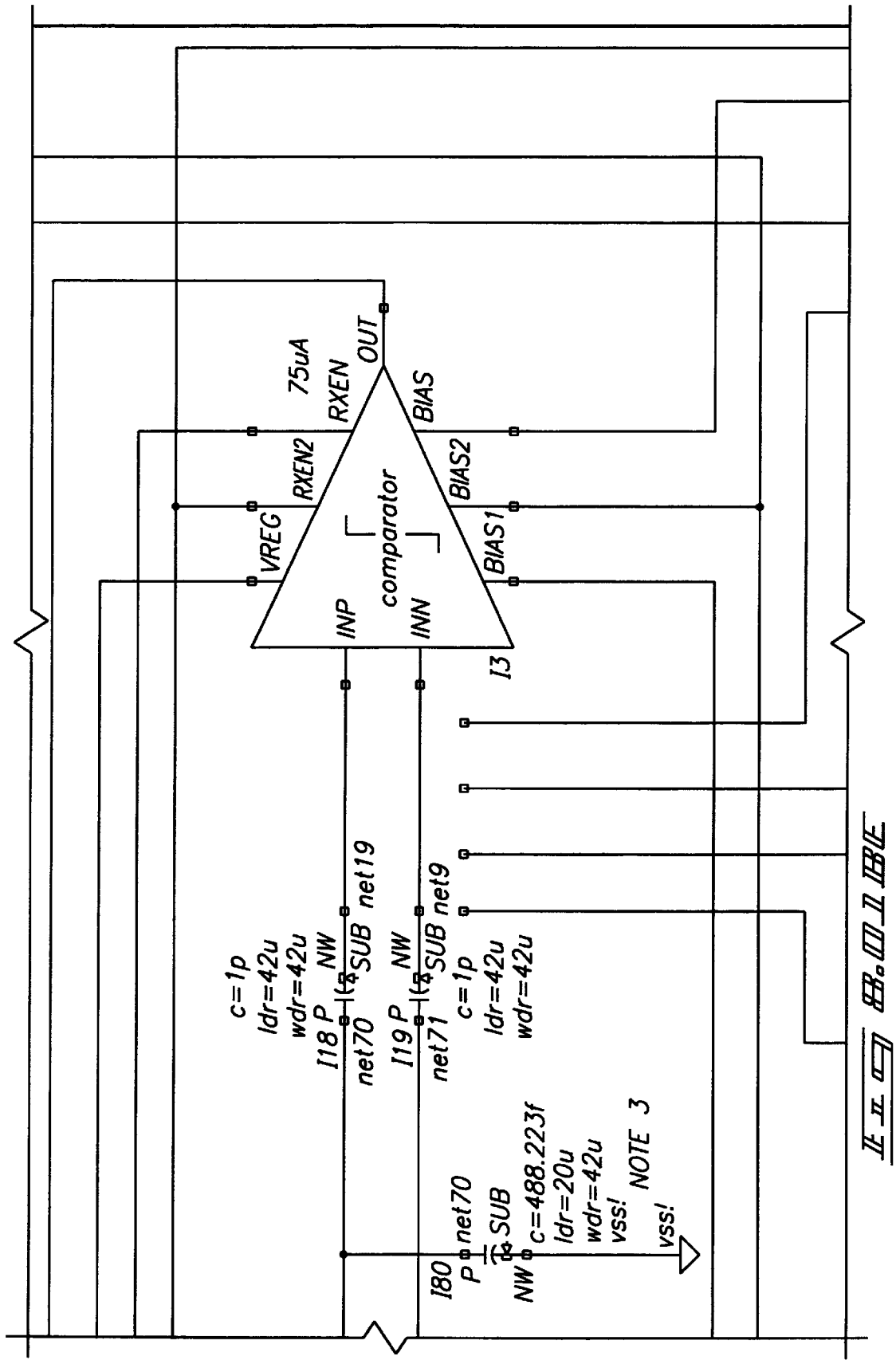

videoamp2
VREG
INP
INN
RXEN
BIAS2
BIAS1
OUTP
OUTN
56uA
I16
I12
I78
I74
I73
I17 P
I15 P
I14 P
I13 P
net71
net87
net86
net15
net13
net5
net25
net78
net79
NW
SUB
P
c=1p
ldr=42u
wdr=42u
c=488.223f
ldr=20u
vss!
NOTE 3

FIG. 1110


75uA
RXEN
OUT
BIAS
RXEN2
BIAS2
VREG
comparator
BIAS1
INP
INN
I3
c=1p
ldr=42u
wdr=42u
I18 P
NW
SUB
net19
net70
I19 P
net71
net9
I80
net70
SUB
c=488.223f
ldr=20u
wdr=42u
vss!
NOTE 3
vss!

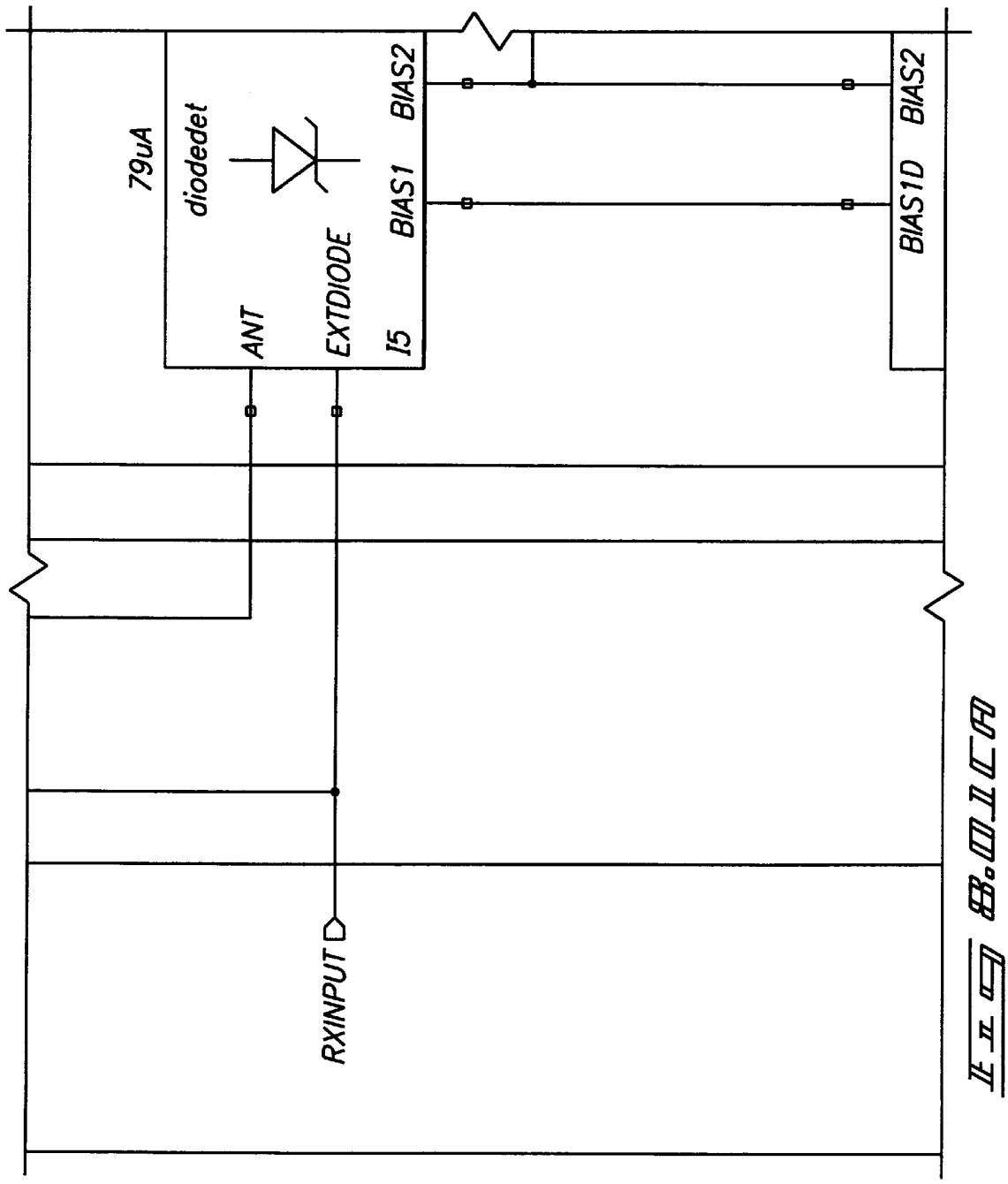


FIG. 88.00116A

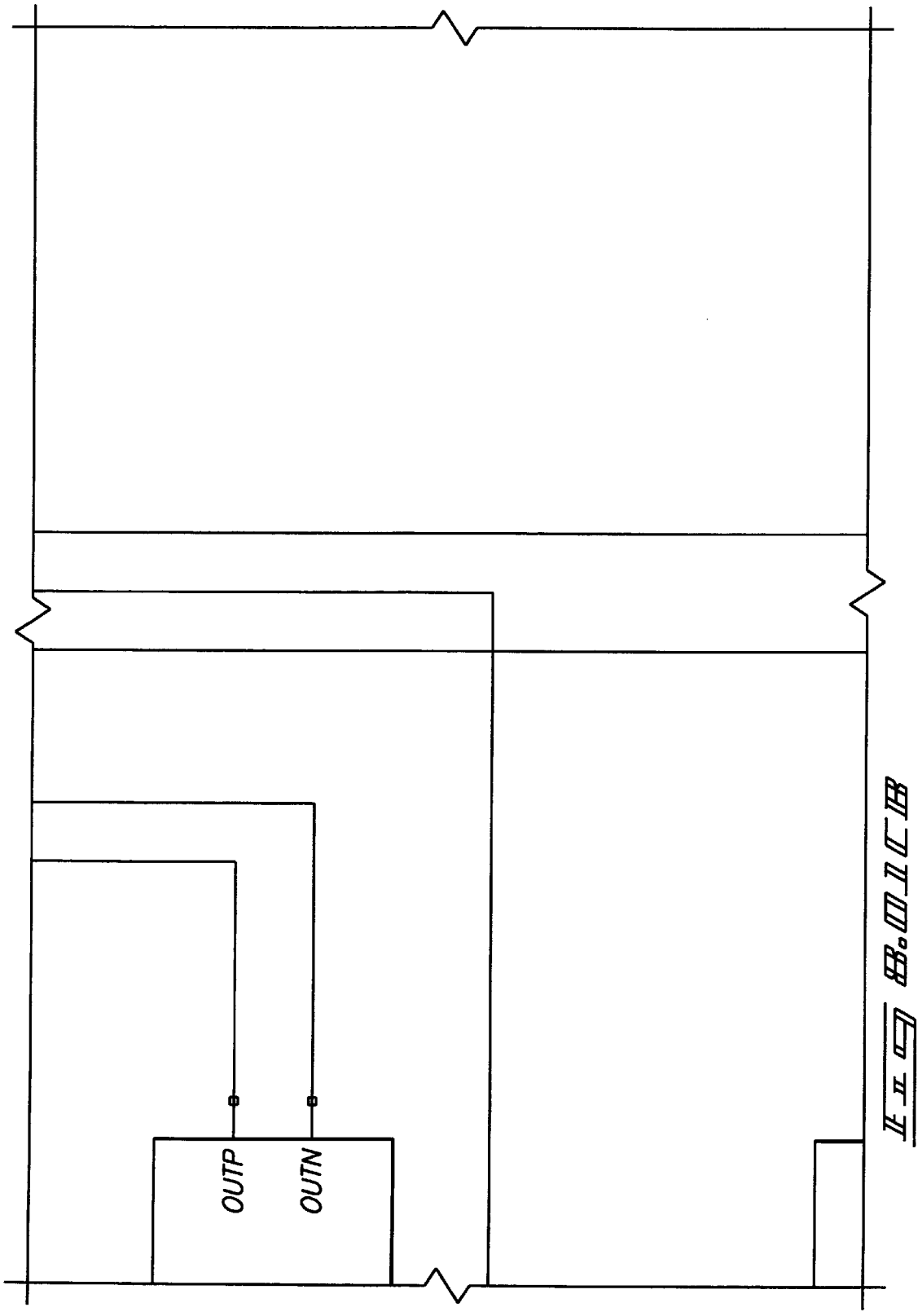


FIG. 8.0112

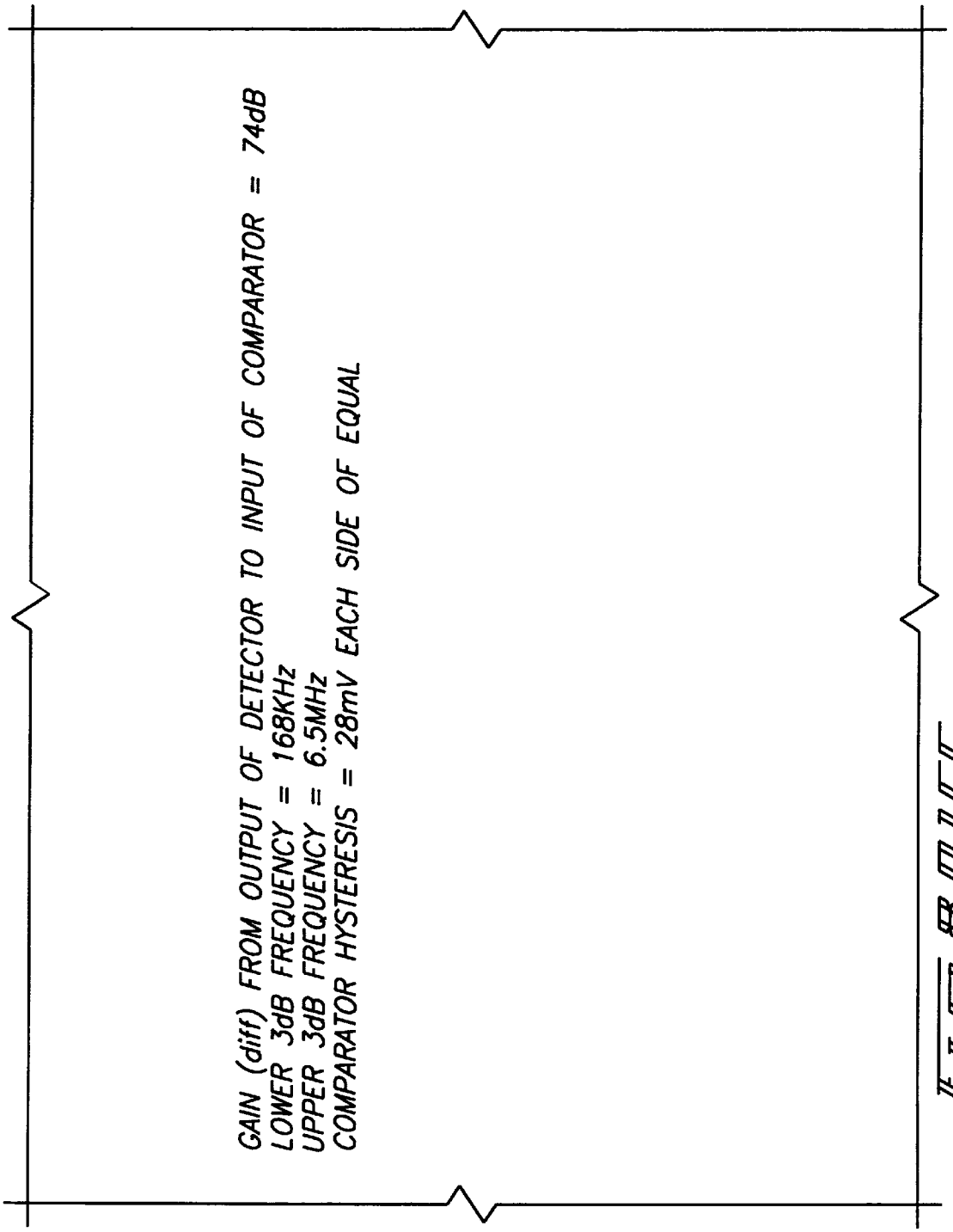

GAIN (diff) FROM OUTPUT OF DETECTOR TO INPUT OF COMPARATOR = 74dB
LOWER 3dB FREQUENCY = 168KHz
UPPER 3dB FREQUENCY = 6.5MHz
COMPARATOR HYSTERESIS = 28mV EACH SIDE OF EQUAL

FIG. 88.111C

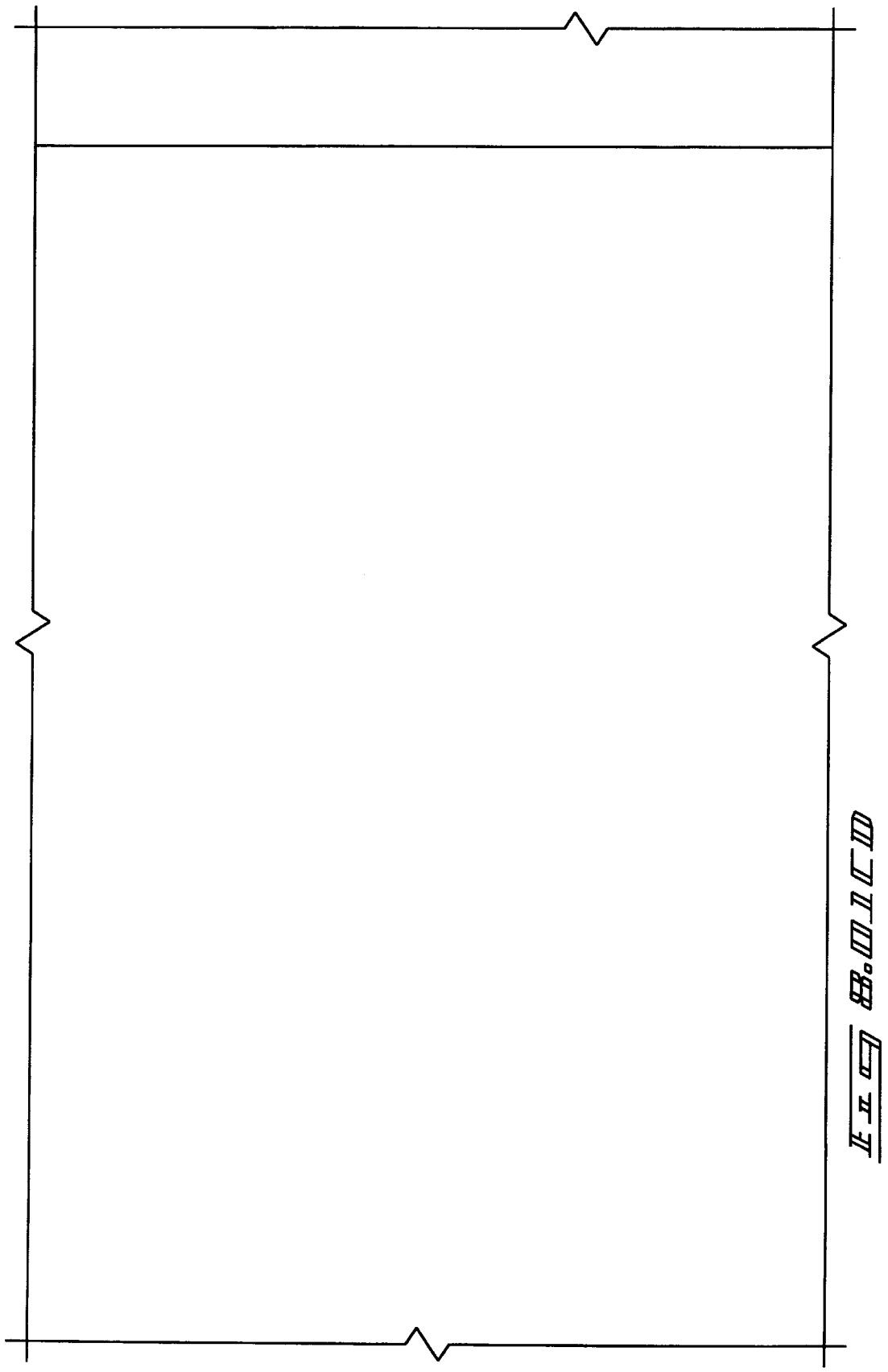


FIG 88.0110

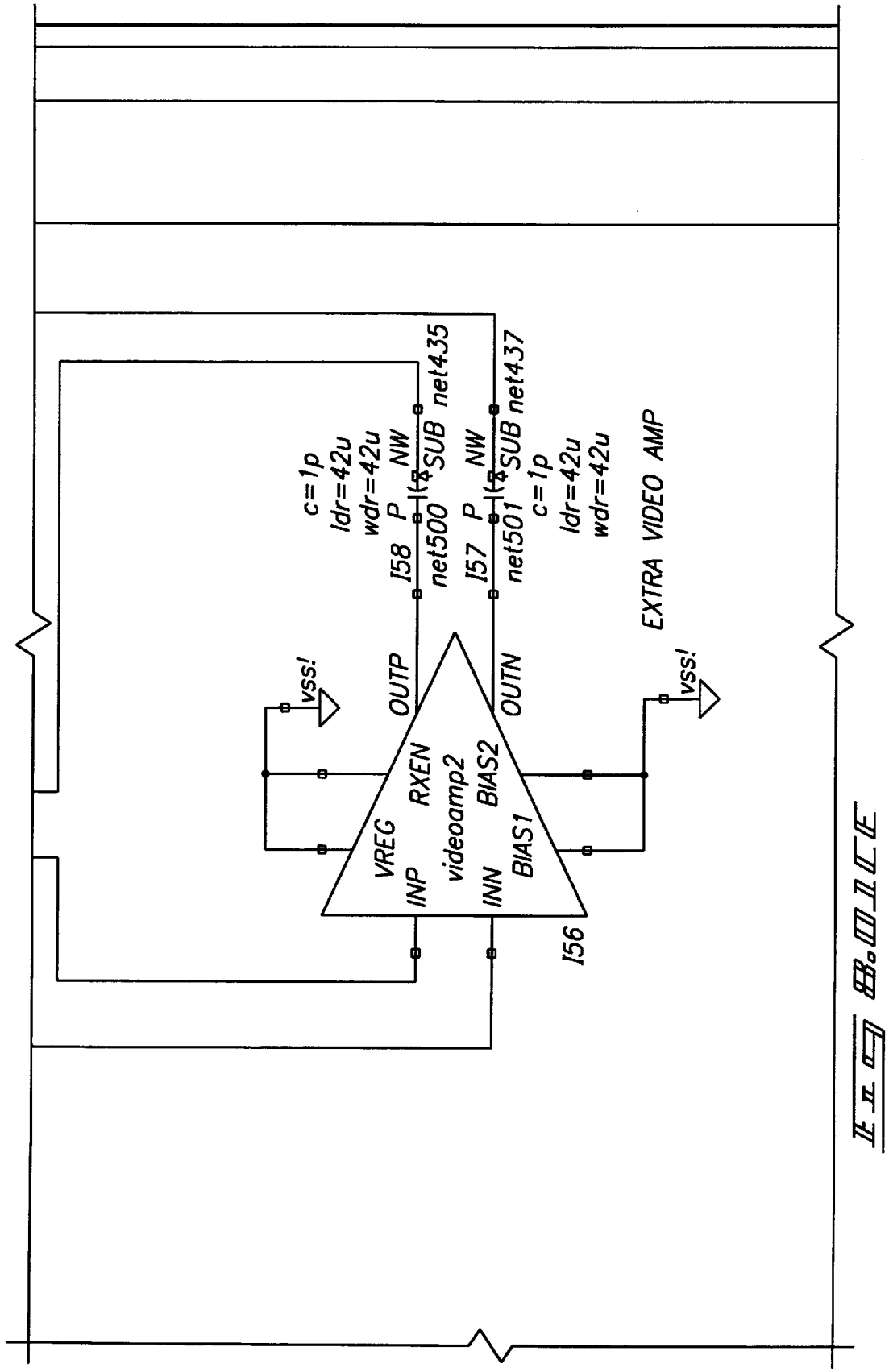

c=1p
ldr=42u
wdr=42u
NW
SUB
net435
P
I58
net500
OUTP
vss!
VREG
INP
RXEN
videoamp2
BIAS2
BIAS1
INN
I56
OUTN
net501
I57
net437
EXTRA VIDEO AMP

FIG. 88.111E

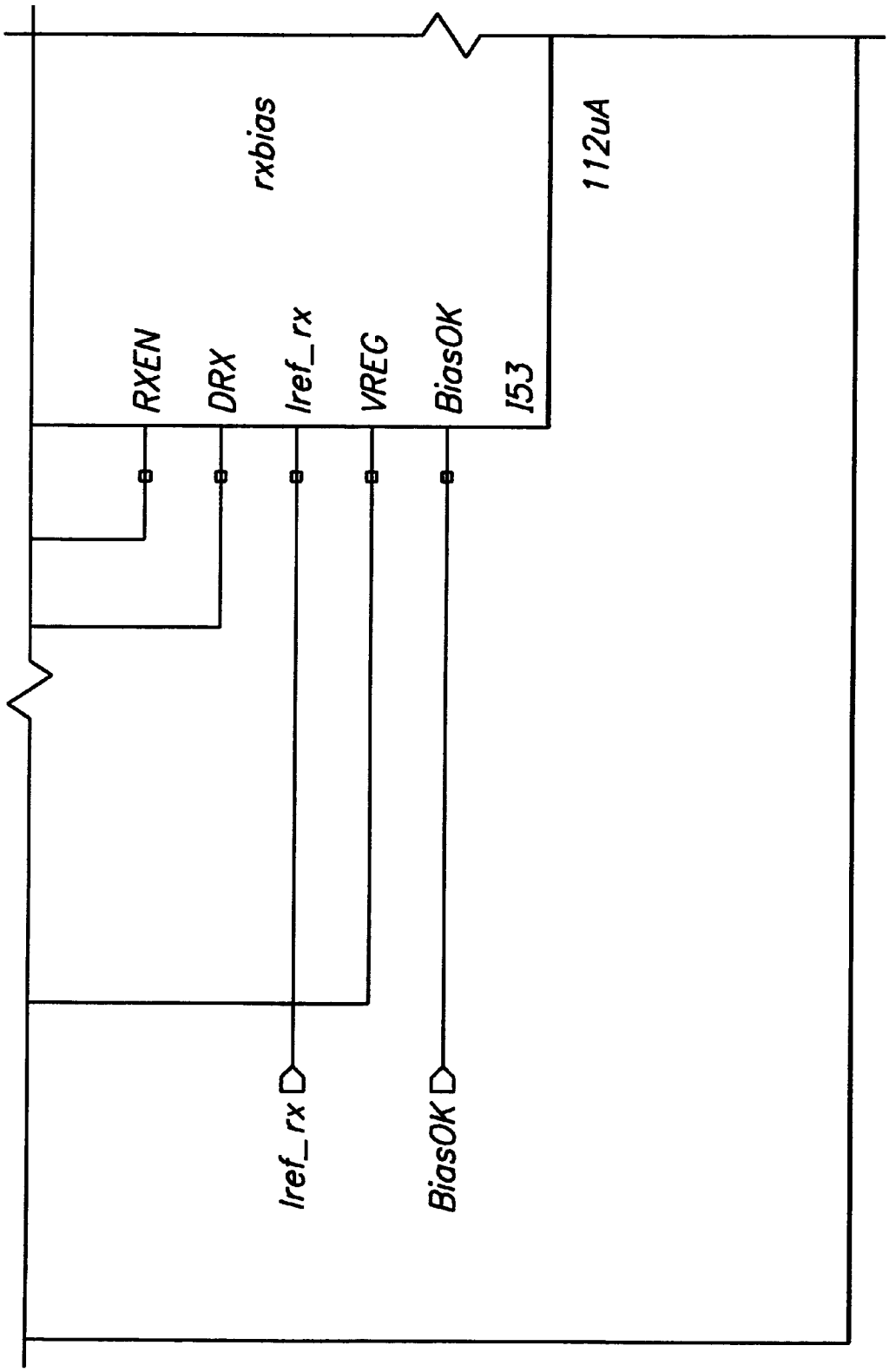


FIG 8.011DA

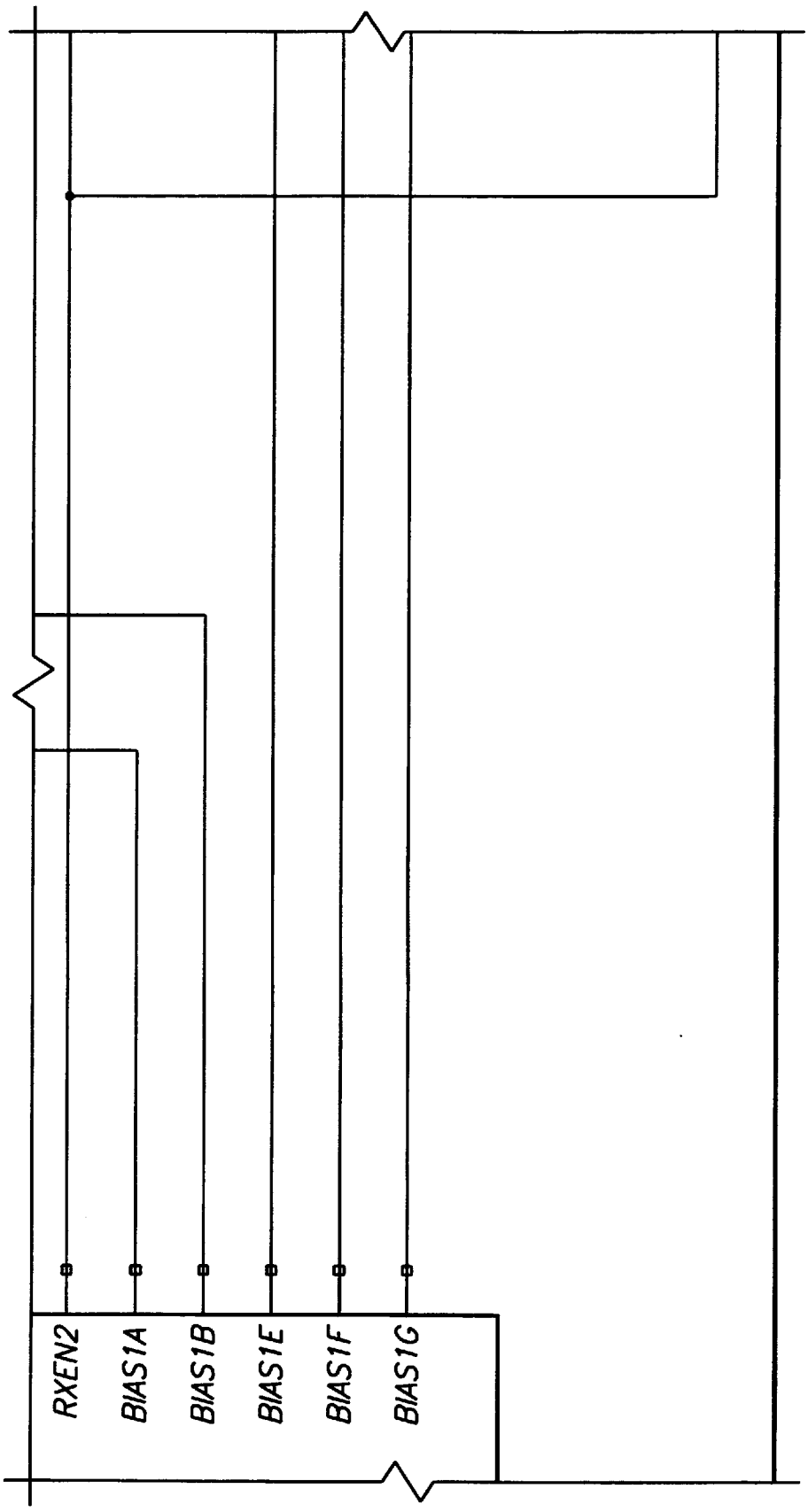


FIG. 88.00_11.00IB

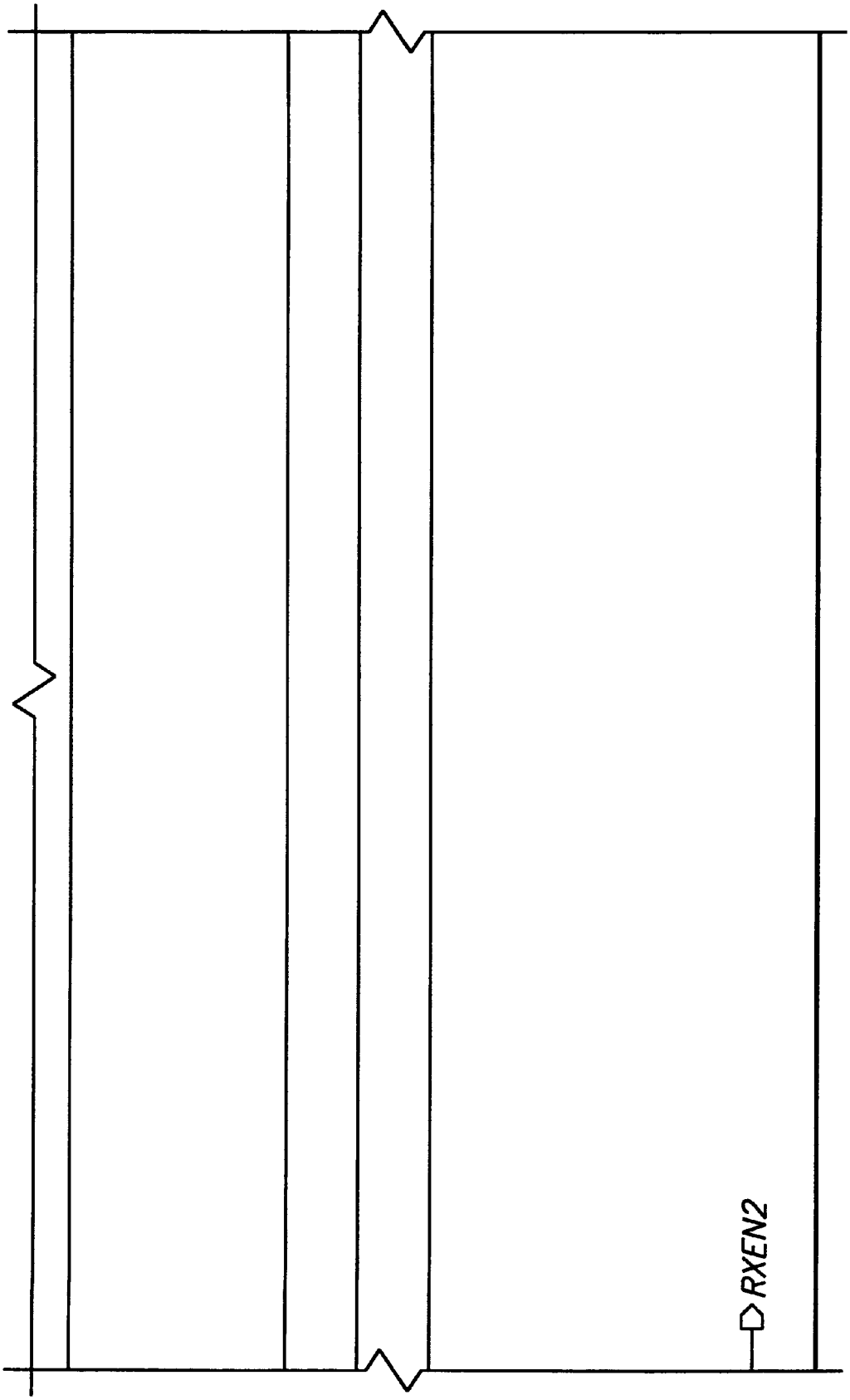


FIG. 88.0011DC

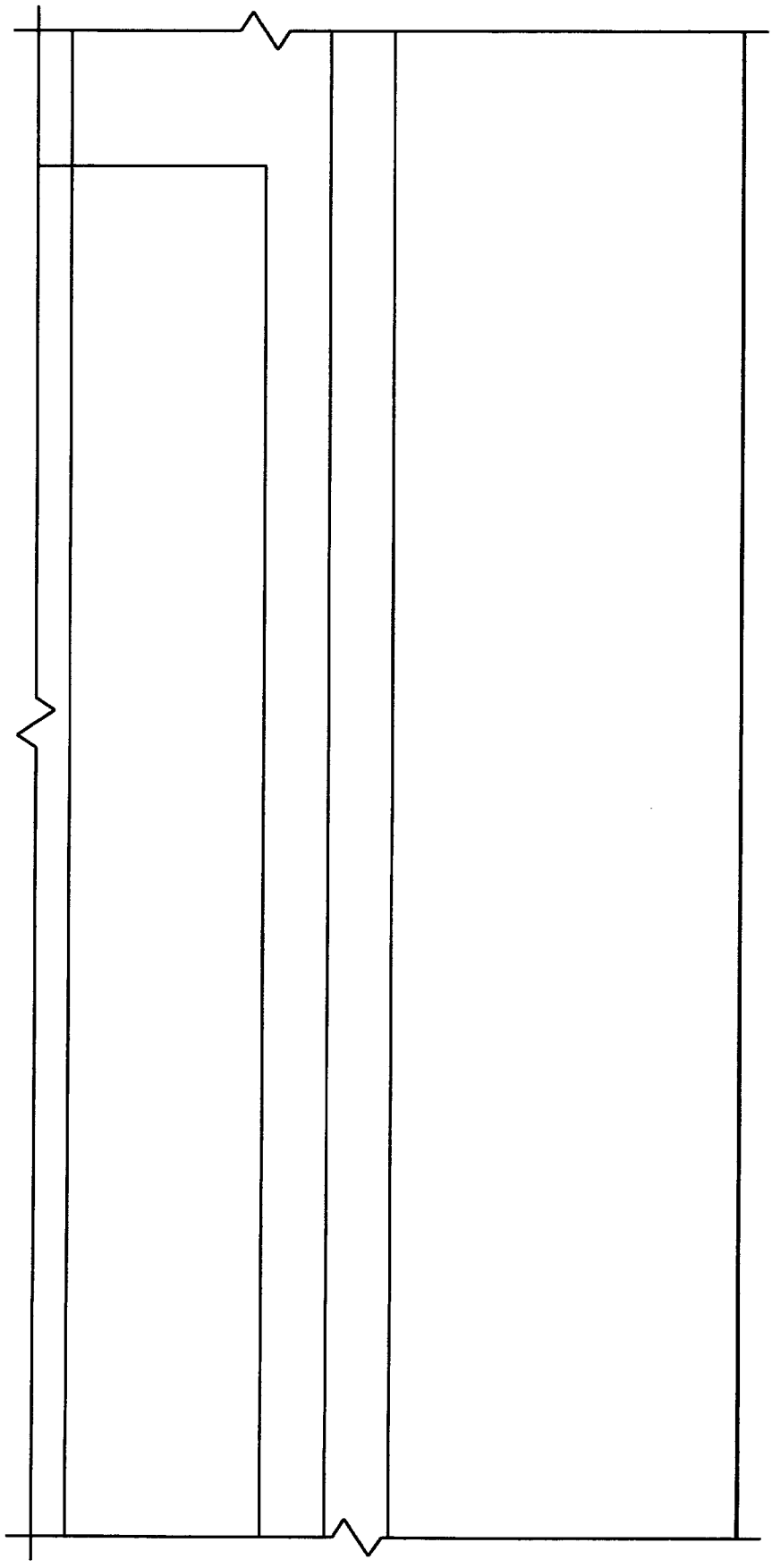


Fig. 8.1110

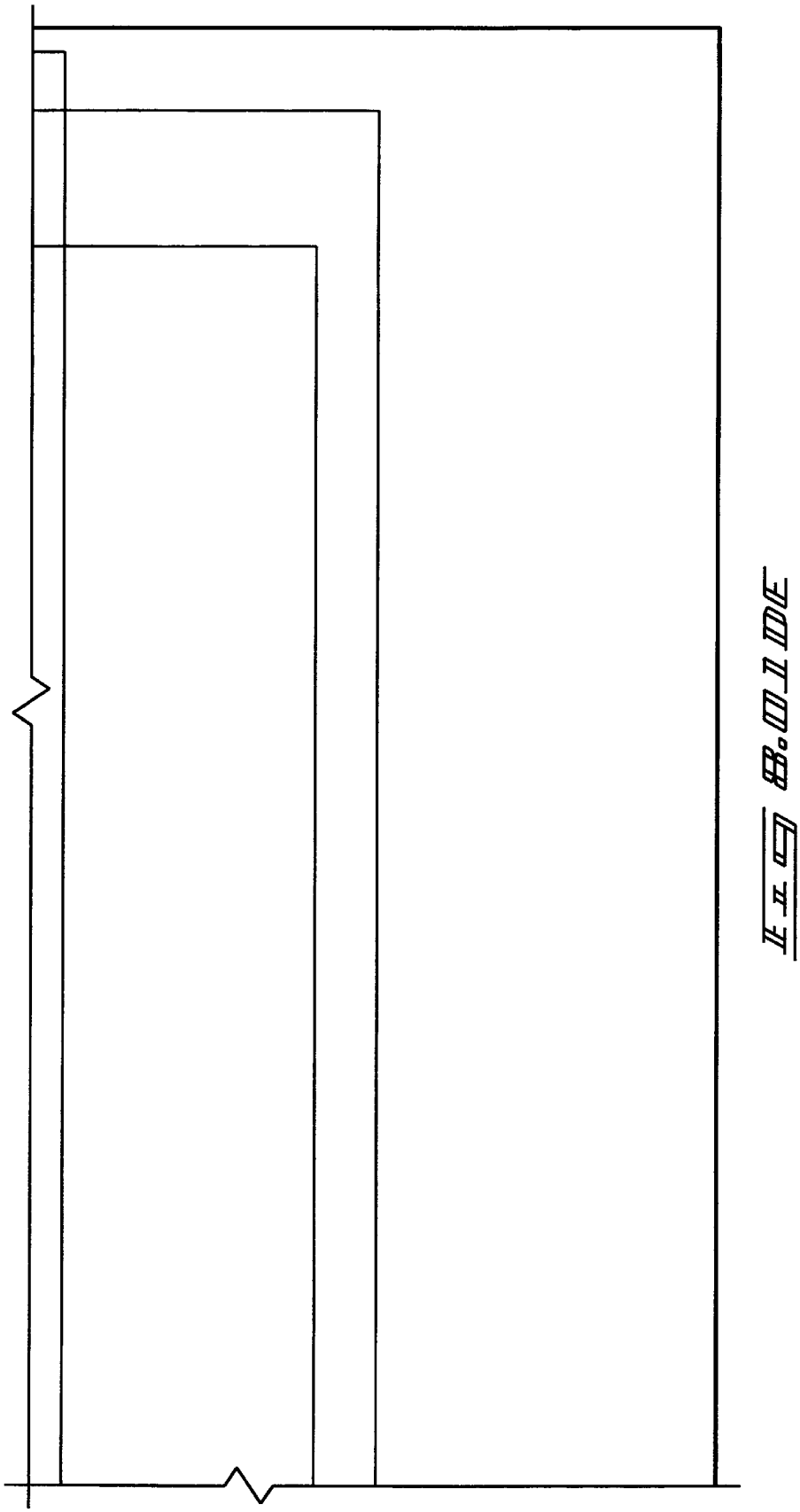


FIG 88.01DE

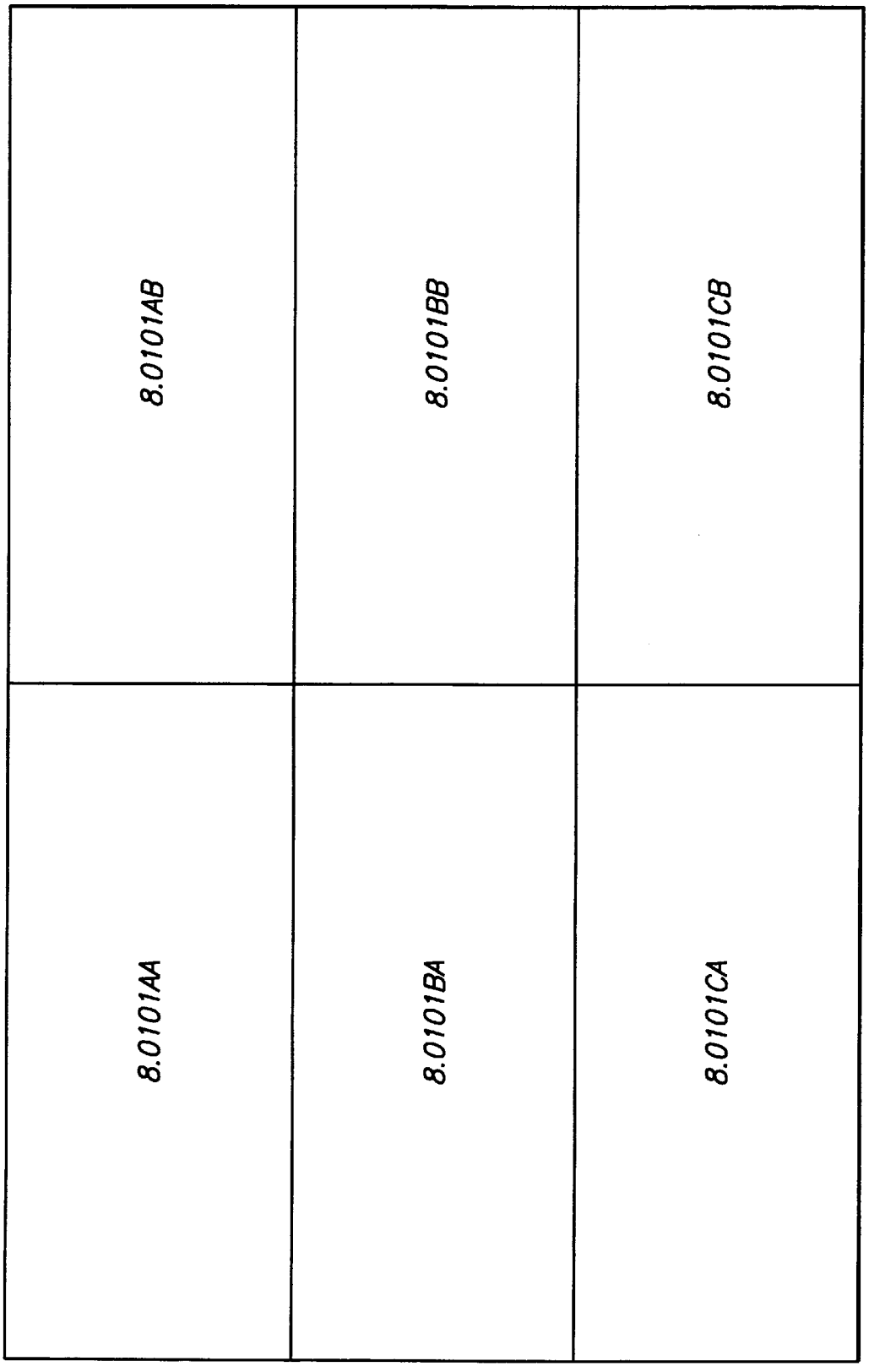


FIG 8.0101

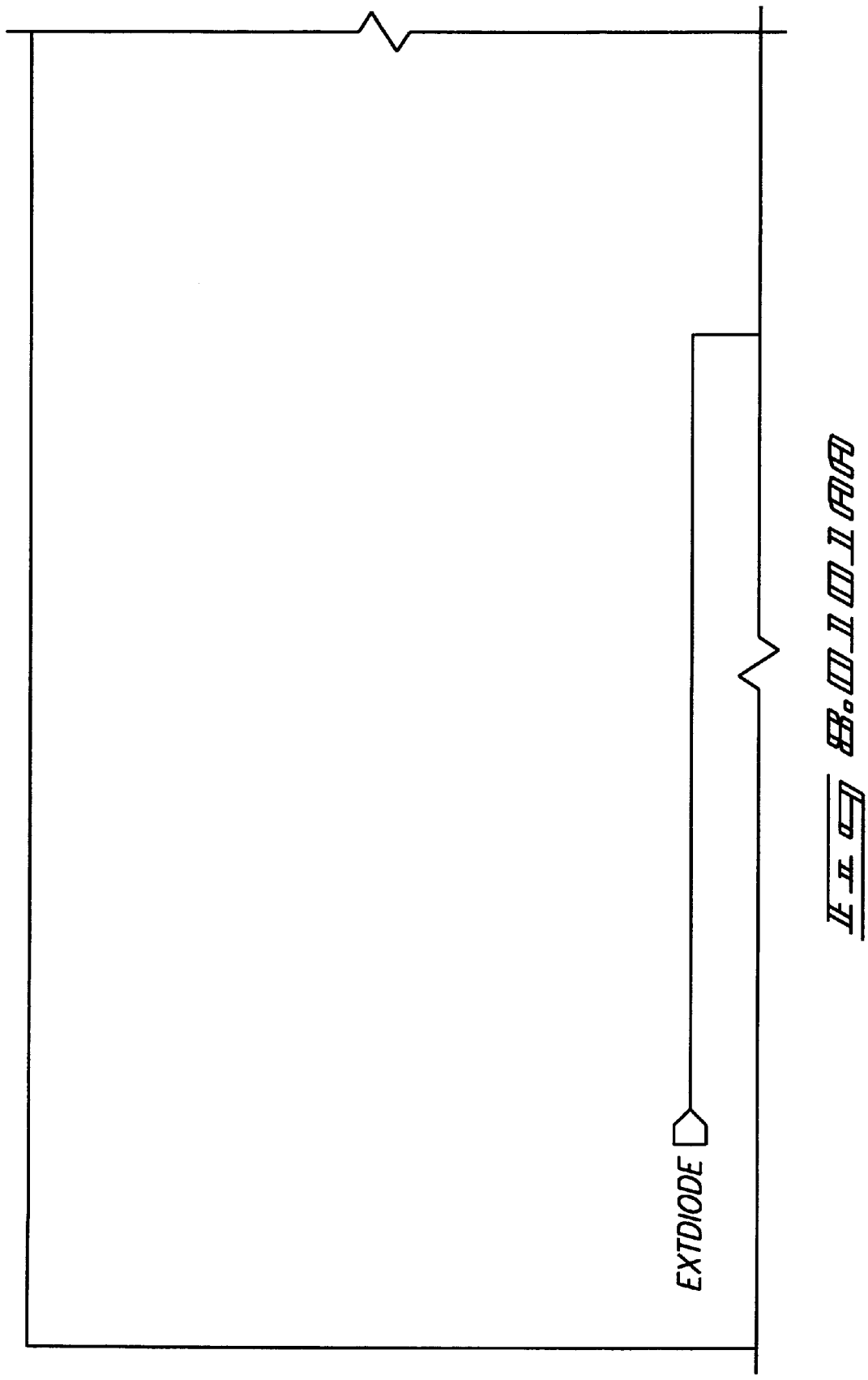


FIG. 88,011AA

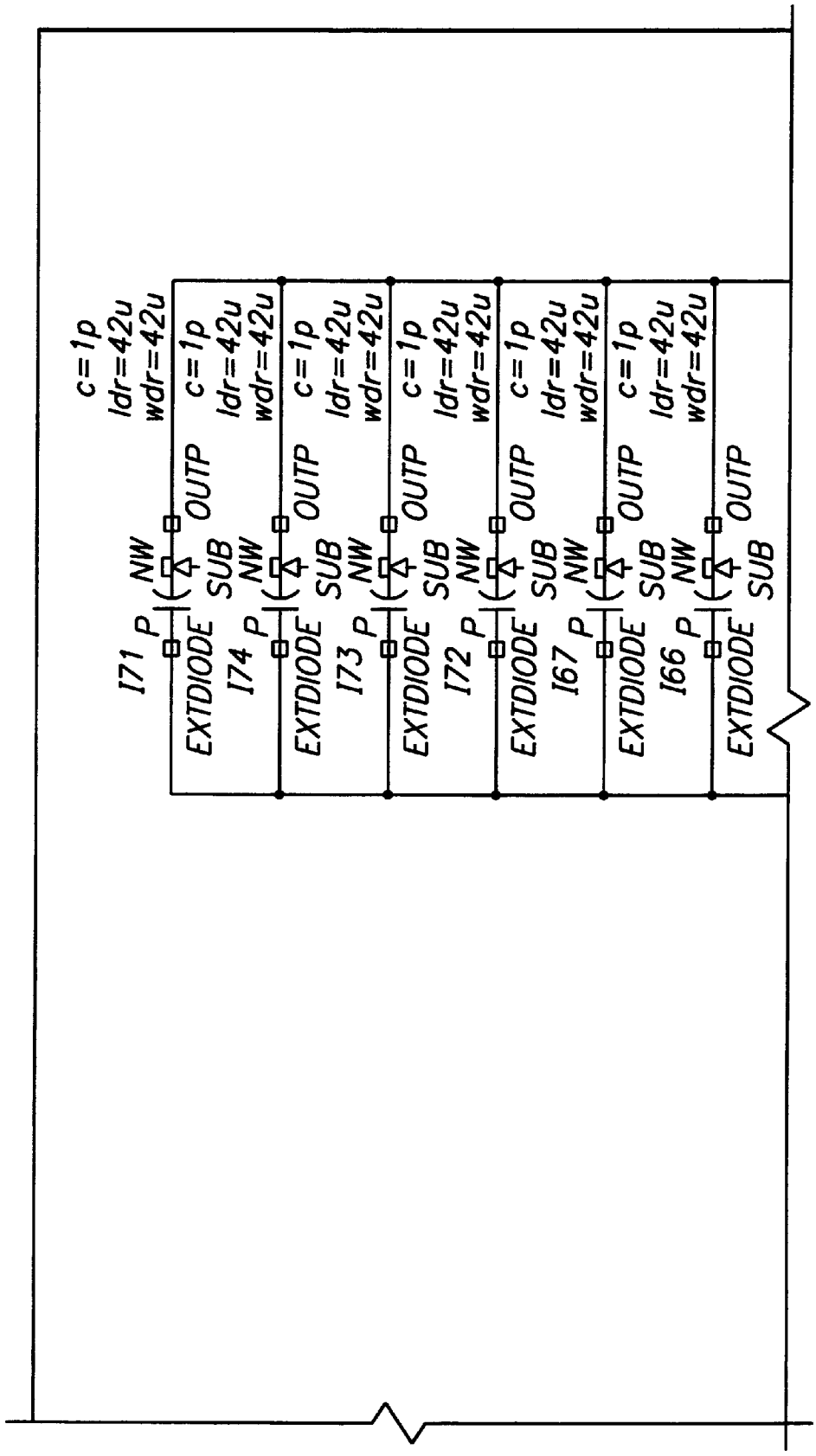

c=1p
ldr=42u
wdr=42u
OUTP
NW
SUB
P
EXTDIODE
I71
I74
I73
I72
I67
I66

FIG. 88.011

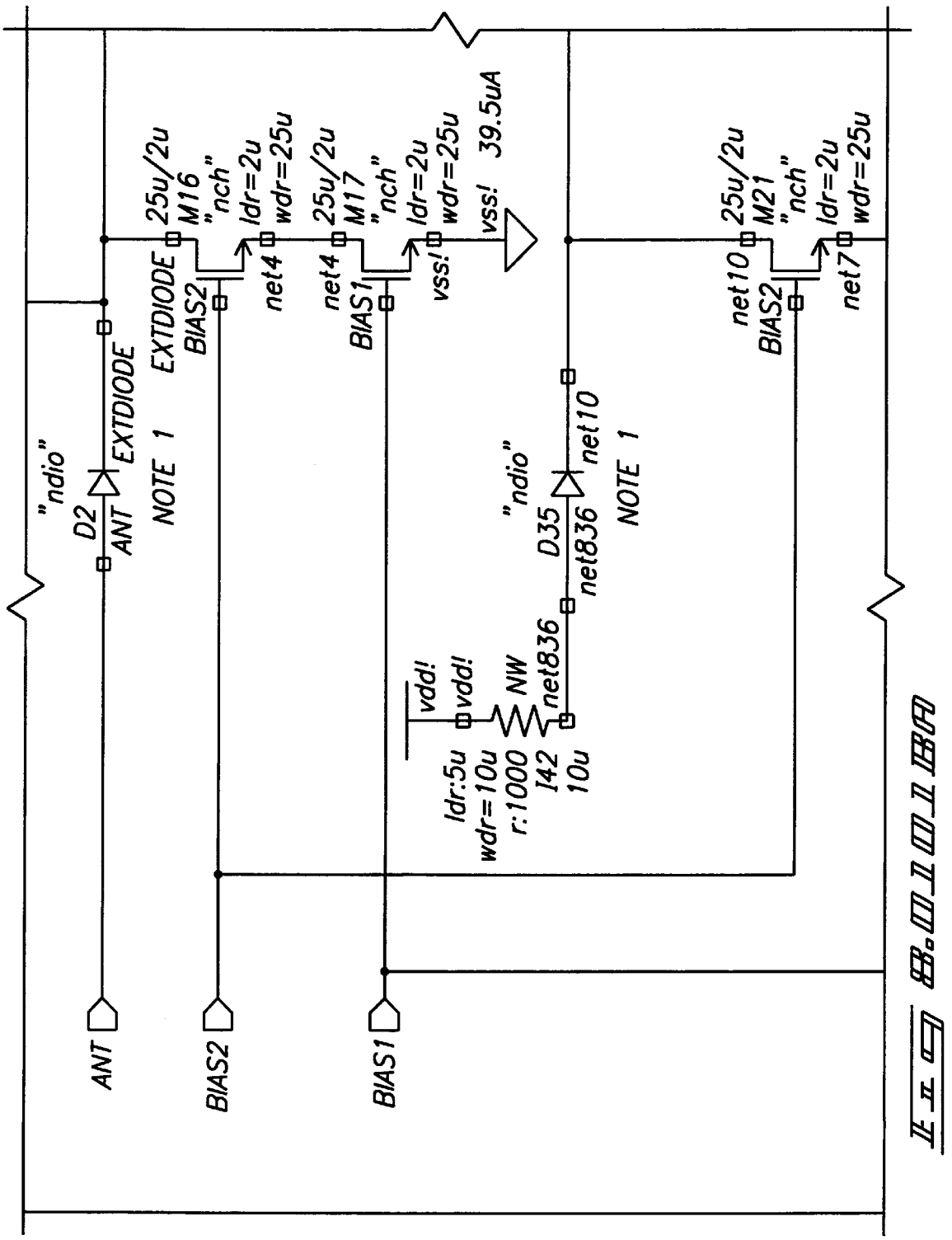
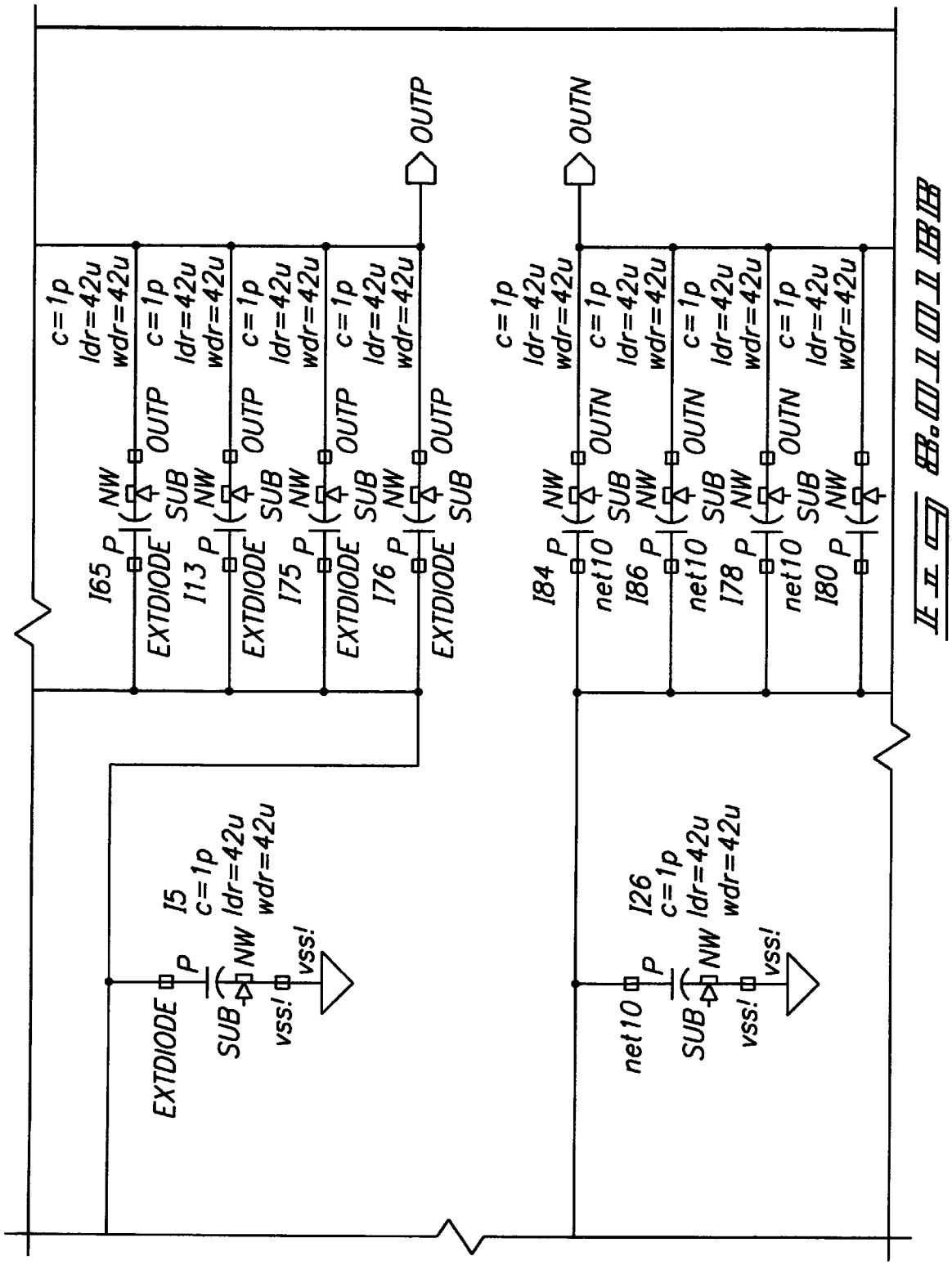


FIG 88.00110BA


OUTP
OUTN
I65 P
I13 P
I75 P
I76 P
I84 P
I86 P
I78 P
I80 P
net10
EXTDIODE
NW
SUB
c=1p
ldr=42u
wdr=42u
I5
I26
vss!

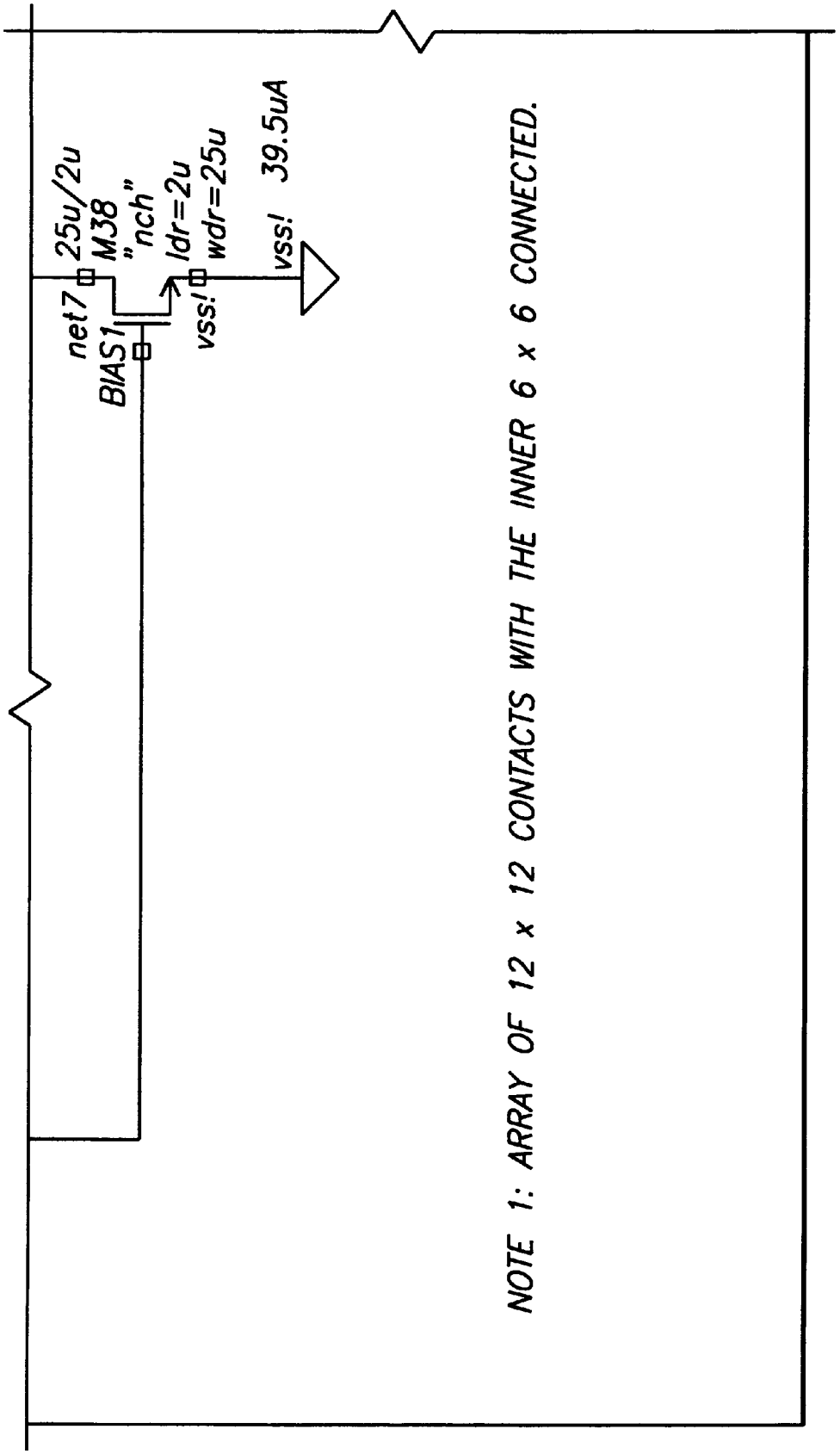


FIG 88.00110CA

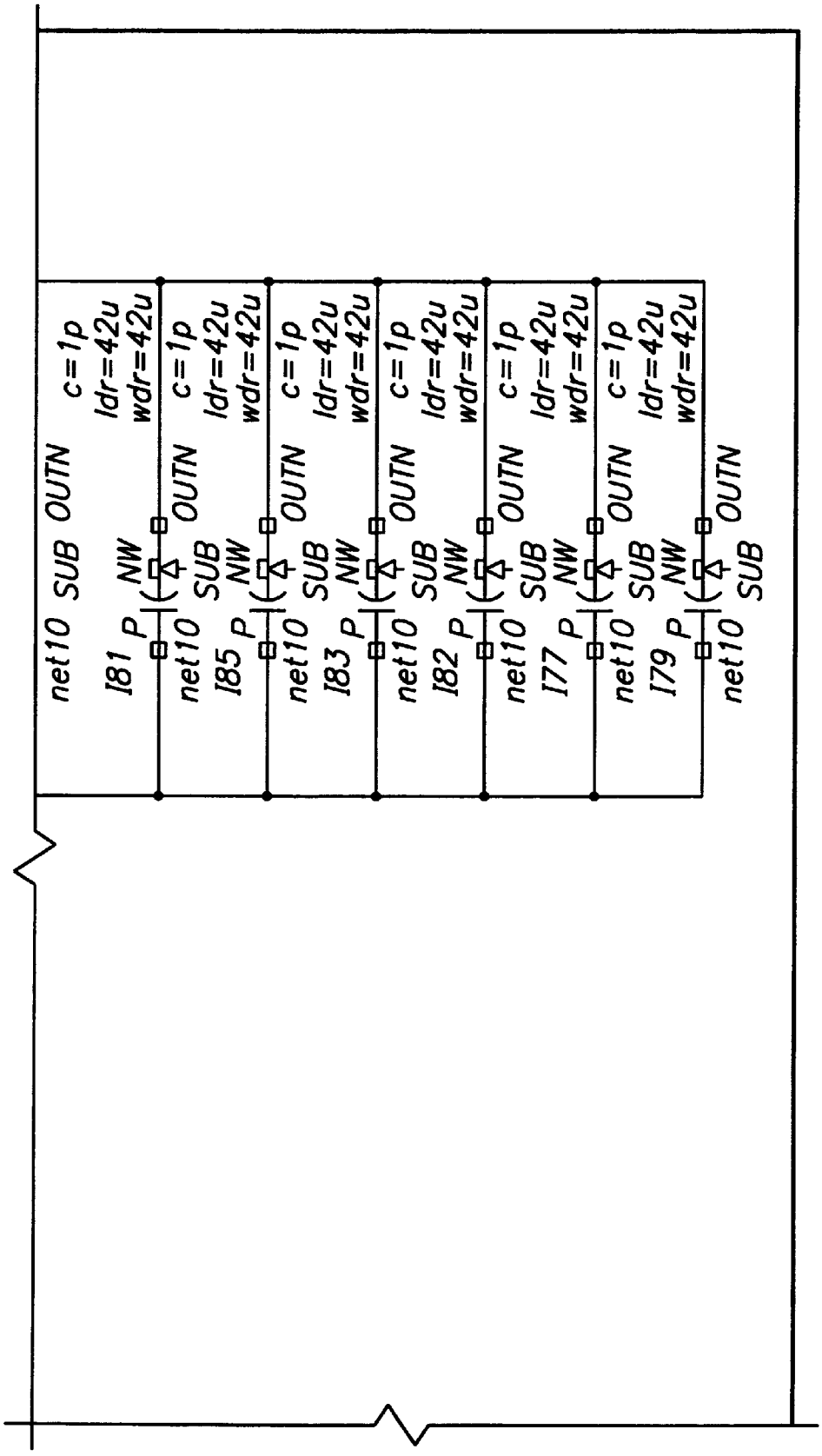

net10 SUB OUTN c=1p ldr=42u wdr=42u
I81 P NW SUB OUTN c=1p ldr=42u wdr=42u
net10 SUB OUTN c=1p ldr=42u wdr=42u
I85 P NW SUB OUTN c=1p ldr=42u wdr=42u
net10 SUB OUTN c=1p ldr=42u wdr=42u
I83 P NW SUB OUTN c=1p ldr=42u wdr=42u
net10 SUB OUTN c=1p ldr=42u wdr=42u
I82 P NW SUB OUTN c=1p ldr=42u wdr=42u
net10 SUB OUTN c=1p ldr=42u wdr=42u
I77 P NW SUB OUTN c=1p ldr=42u wdr=42u
net10 SUB OUTN c=1p ldr=42u wdr=42u
I79 P NW SUB OUTN
net10 SUB

FIG. 88,011

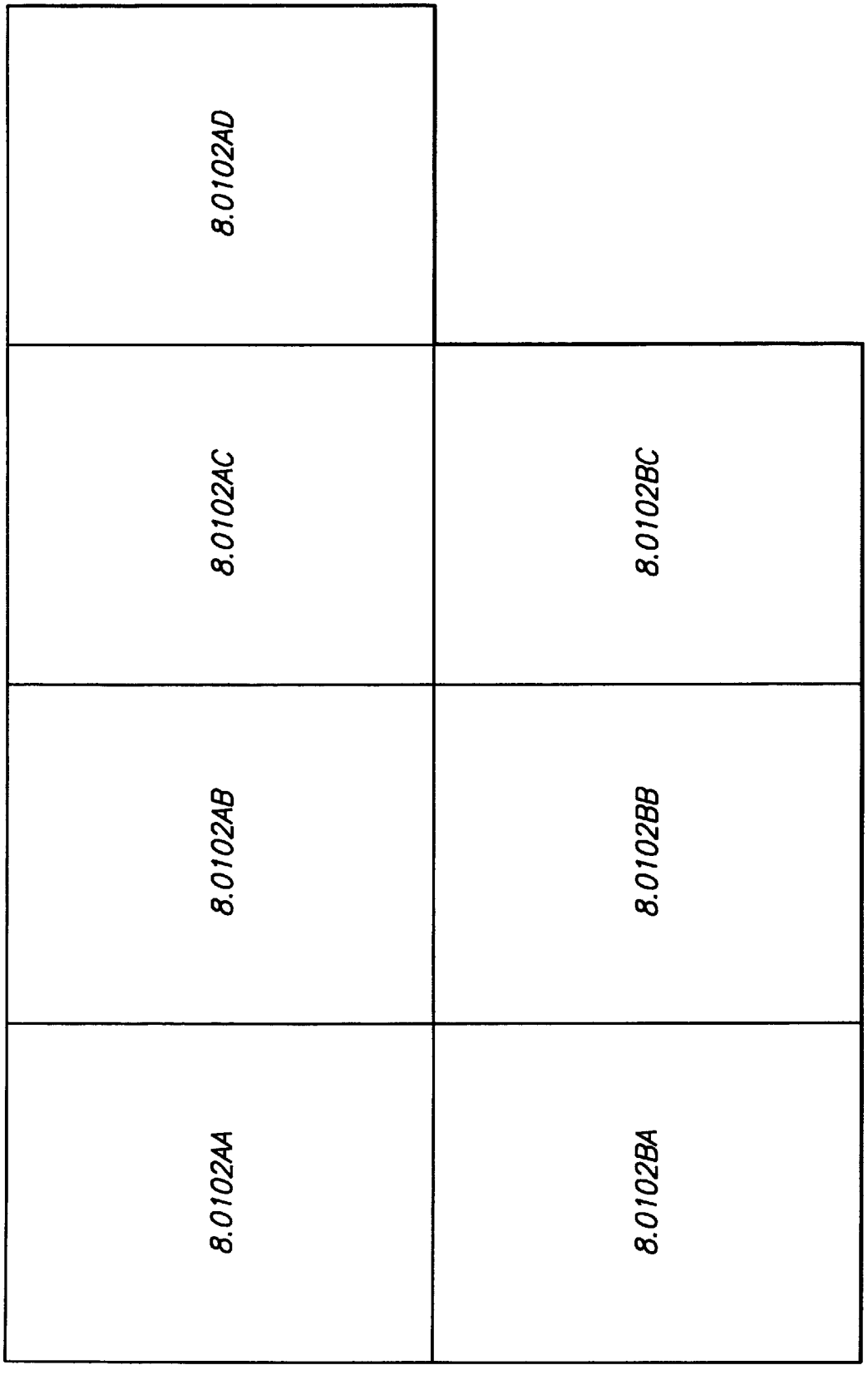
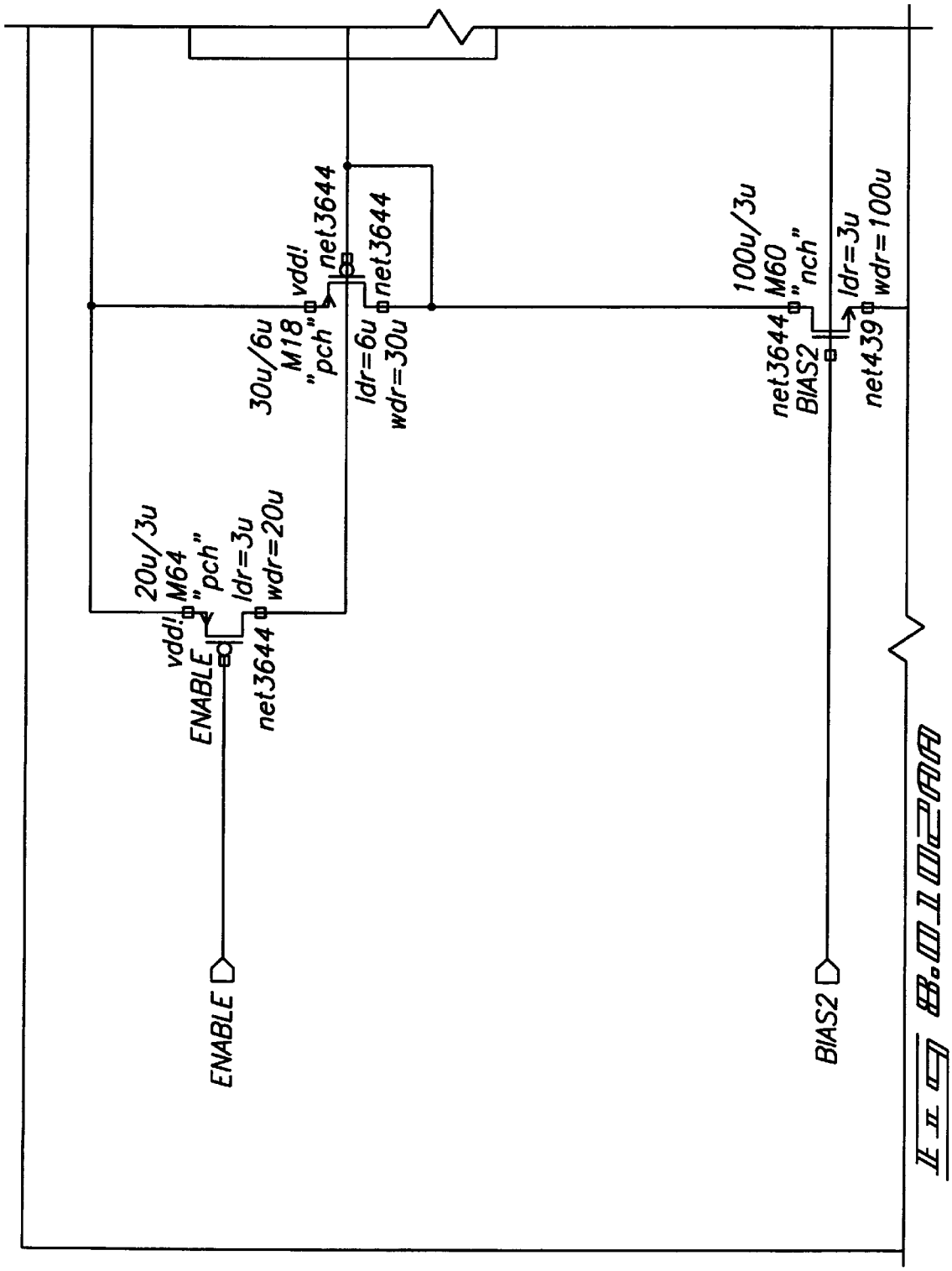
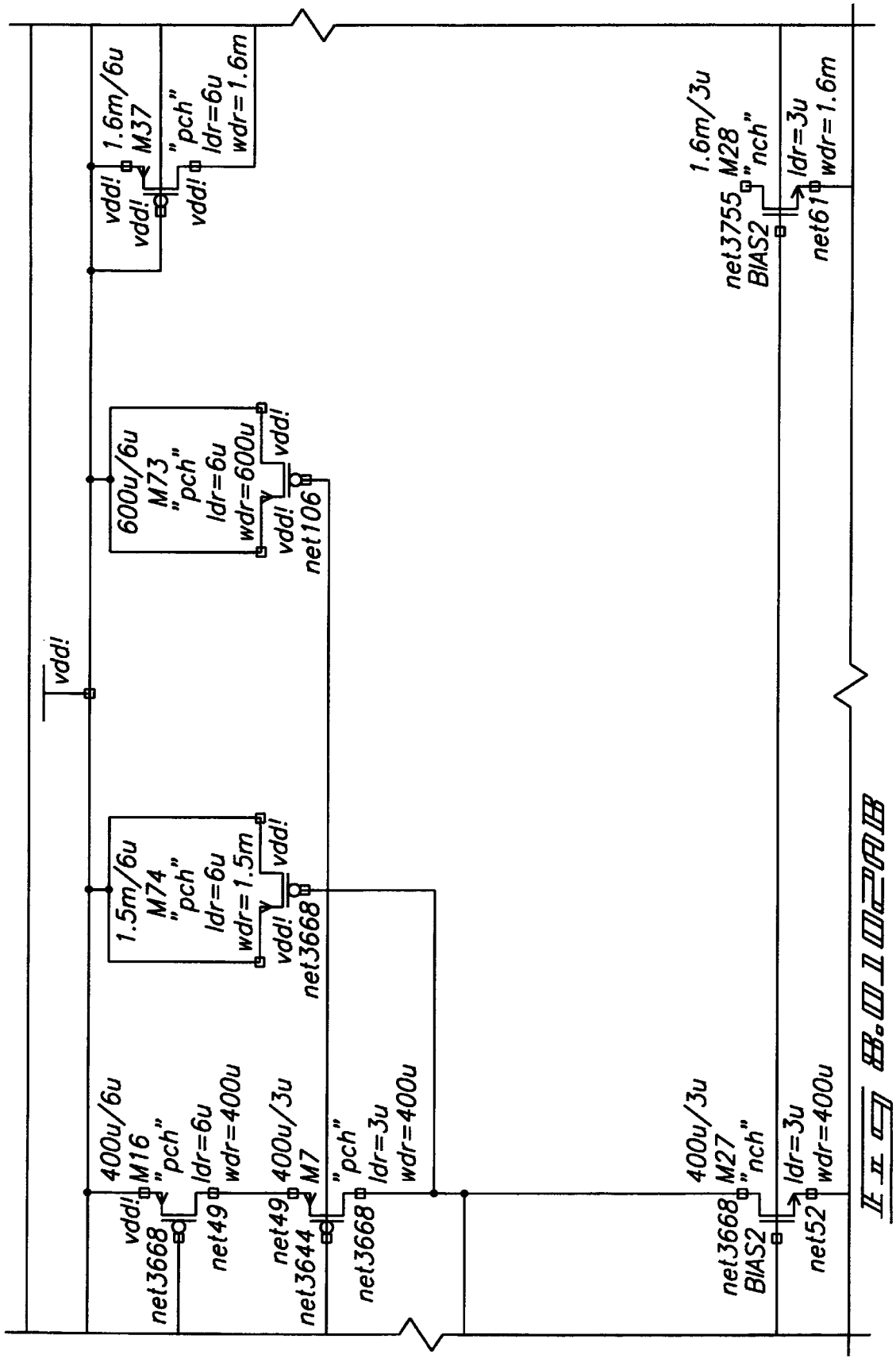
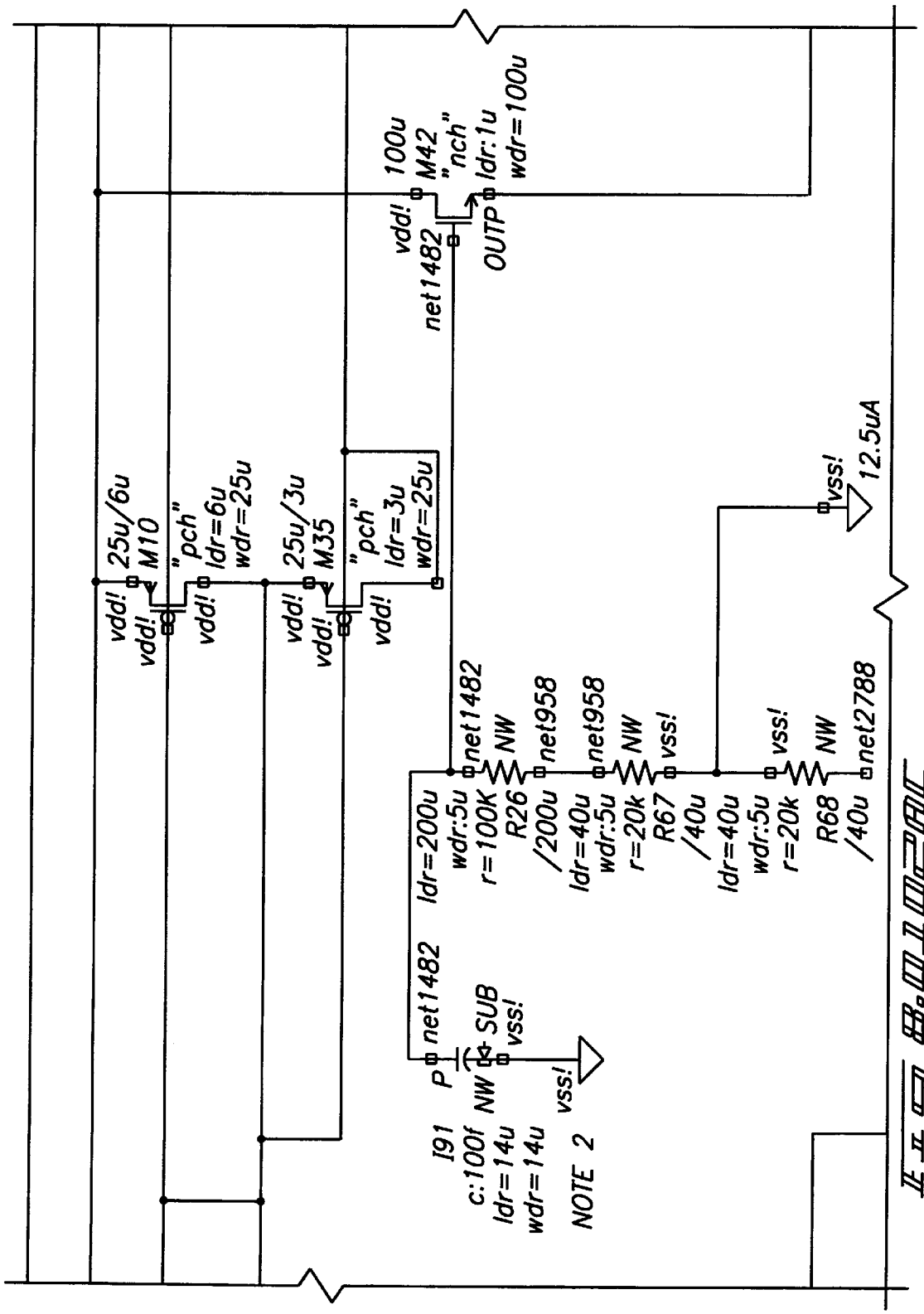
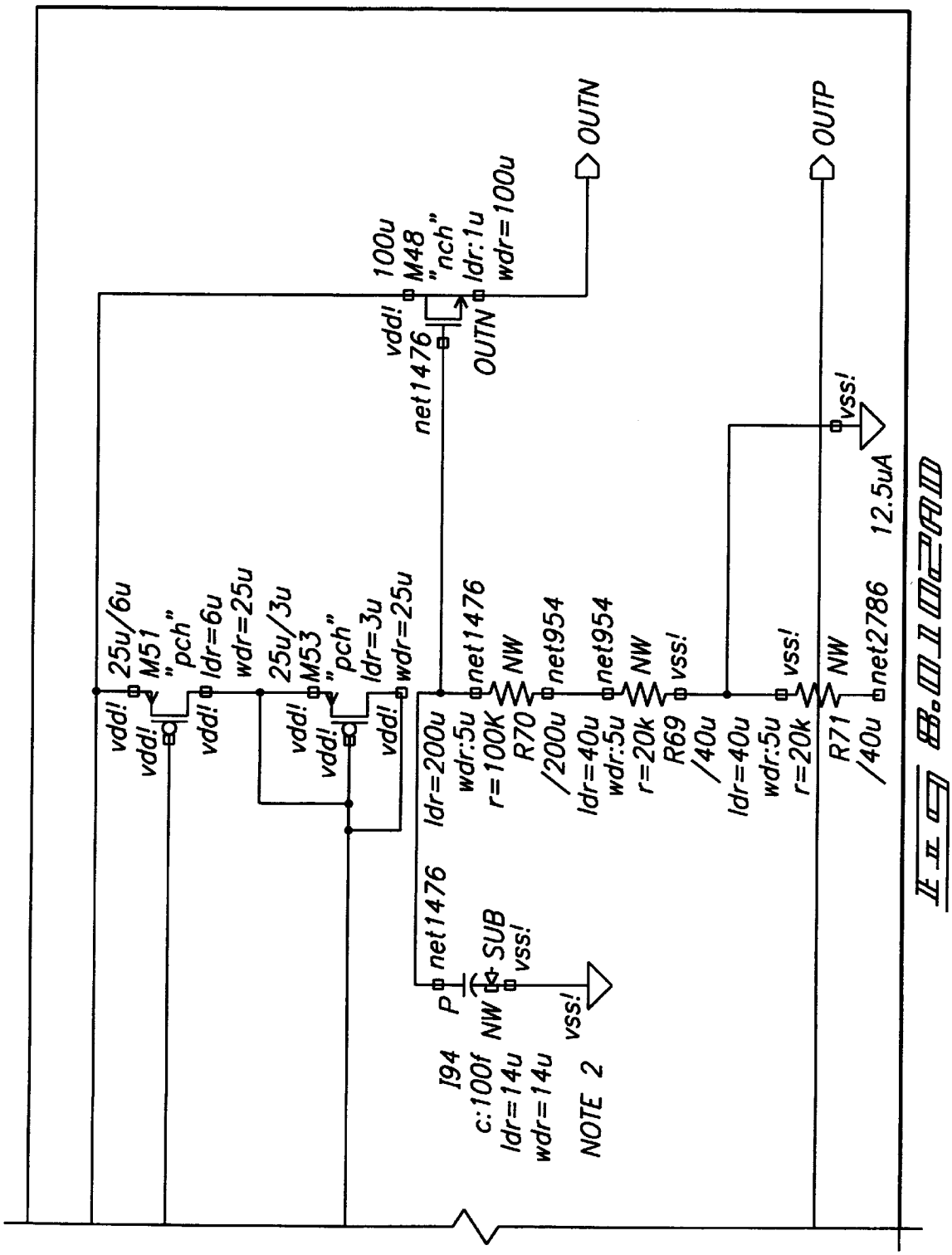


FIG 8.0102


20u/3u
M64
"pch"
ldr=3u
wdr=20u
vdd!
ENABLE
net3644
30u/6u
M18
"pch"
ldr=6u
wdr=30u
vdd!
net3644
net3644
100u/3u
M60
"nch"
ldr=3u
wdr=100u
net3644
BIAS2
net439
ENABLE
BIAS2


vdd!
1.6m/6u
M37
"pch"
ldr=6u
wdr=1.6m
600u/6u
M73
"pch"
ldr=6u
wdr=600u
net106
1.5m/6u
M74
"pch"
ldr=6u
wdr=1.5m
net3668
400u/6u
M16
"pch"
ldr=6u
wdr=400u
net3668
net49
400u/3u
M7
"pch"
ldr=3u
wdr=400u
net3644
net3668
1.6m/3u
M28
"nch"
ldr=3u
wdr=1.6m
net3755
BIAS2
net61
400u/3u
M27
"nch"
ldr=3u
wdr=400u
net3668
BIAS2
net52


100u
M42
"nch"
ldr:1u
wdr=100u
vdd!
net1482
OUTP
25u/6u
M10
"pch"
ldr=6u
wdr=25u
25u/3u
M35
"pch"
ldr=3u
wdr=25u
vdd!
vss!
12.5uA
net1482
NW
net958
net958
NW
vss!
vss!
NW
net2788
ldr=200u
wdr:5u
r=100K
R26
/200u
ldr=40u
wdr:5u
r=20k
R67
/40u
ldr=40u
wdr:5u
r=20k
R68
/40u
net1482
P
SUB
NW
vss!
vss!
I91
c:100f
ldr=14u
wdr=14u
NOTE 2


25u/6u
M51
"pch"
ldr=6u
wdr=25u
25u/3u
M53
"pch"
ldr=3u
wdr=25u
100u
M48
"nch"
ldr:1u
wdr=100u
OUTN
OUTP
vdd!
net1476
net954
net2786
ldr=200u
wdr:5u
r=100K
R70
/200u
ldr=40u
wdr:5u
r=20k
R69
/40u
R71
/40u
NW
vss!
12.5uA
I94
c:100f
ldr=14u
wdr=14u
P
SUB
NOTE 2

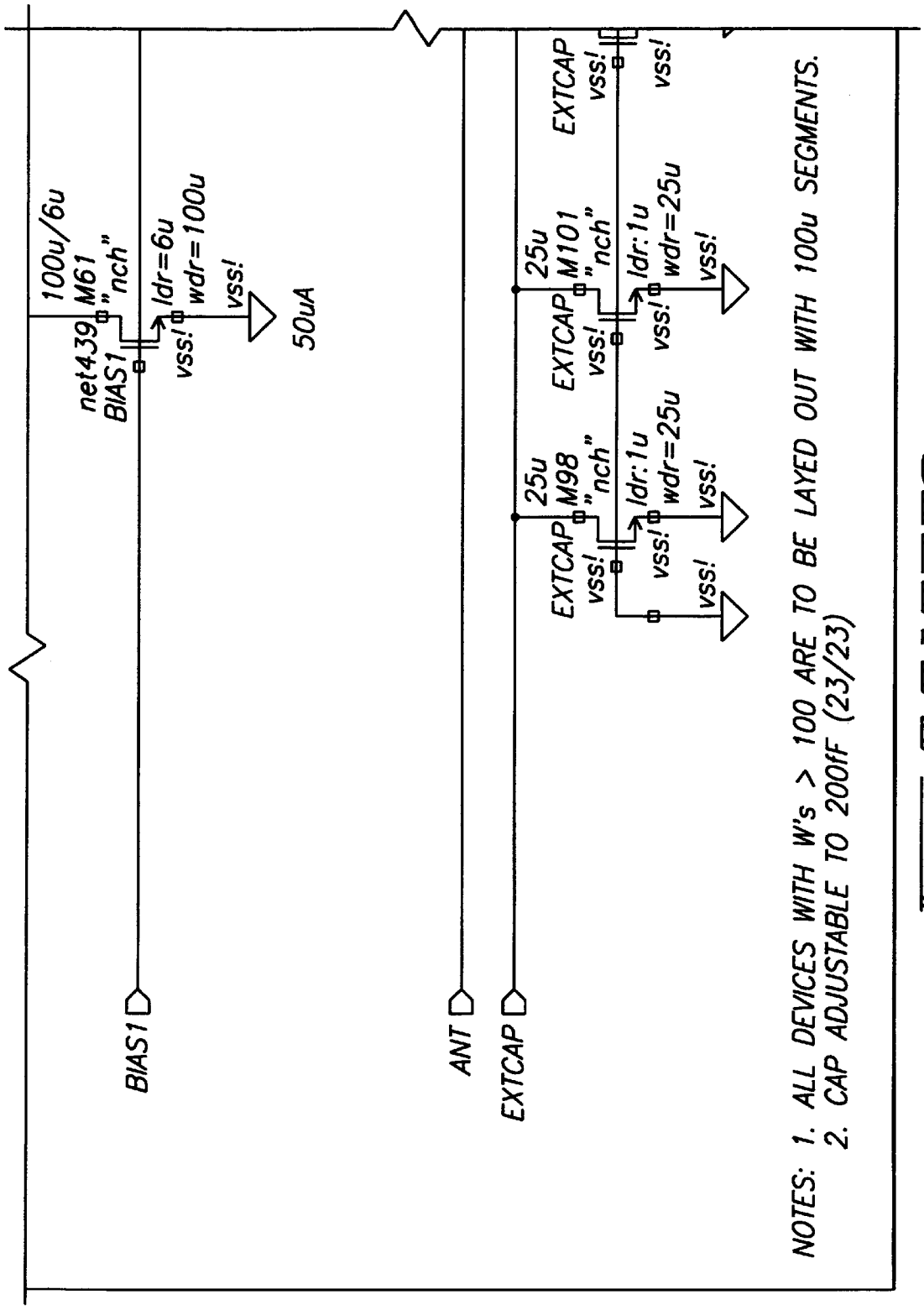

100u/6u
M61
"nch"
net439
BIAS1
ldr=6u
wdr=100u
vss!
50uA
BIAS1
ANT
EXTCAP
25u
M98
"nch"
EXTCAP
vss!
ldr:1u
wdr=25u
25u
M101
"nch"
EXTCAP
NOTES: 1. ALL DEVICES WITH W's > 100 ARE TO BE LAYED OUT WITH 100u SEGMENTS.
2. CAP ADJUSTABLE TO 200fF (23/23)

FIG. 88.111

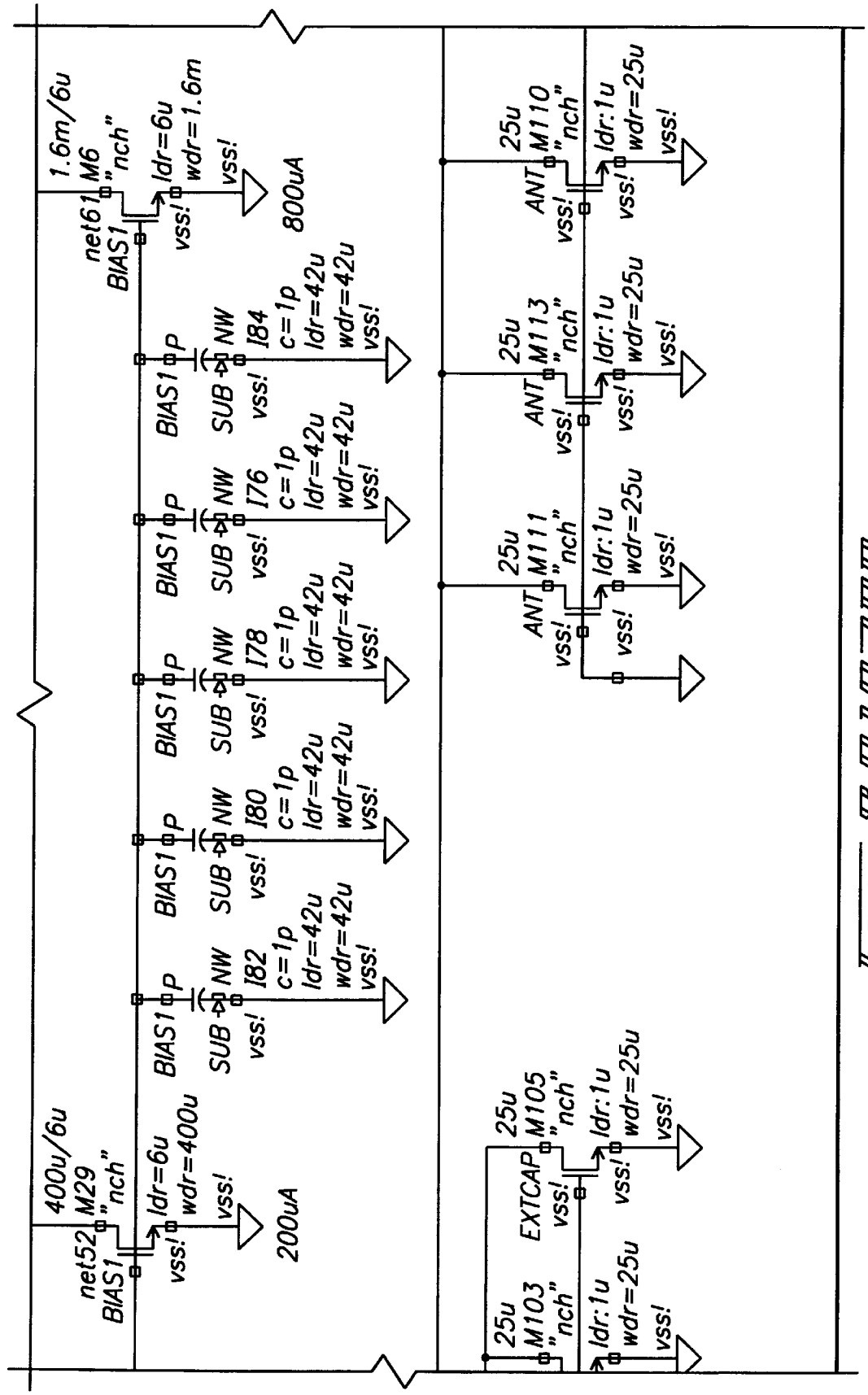

1.6m/6u
M6
"nch"
net61
BIAS1
ldr=6u
wdr=1.6m
vss!
800uA
BIAS1
P
NW
SUB
I84
c=1p
ldr=42u
wdr=42u
I76
I78
I80
I82
400u/6u
M29
net52
ldr=6u
wdr=400u
200uA
25u
M110
ANT
ldr:1u
wdr=25u
M113
M111
M105
EXTCAP
M103

FIG. 111

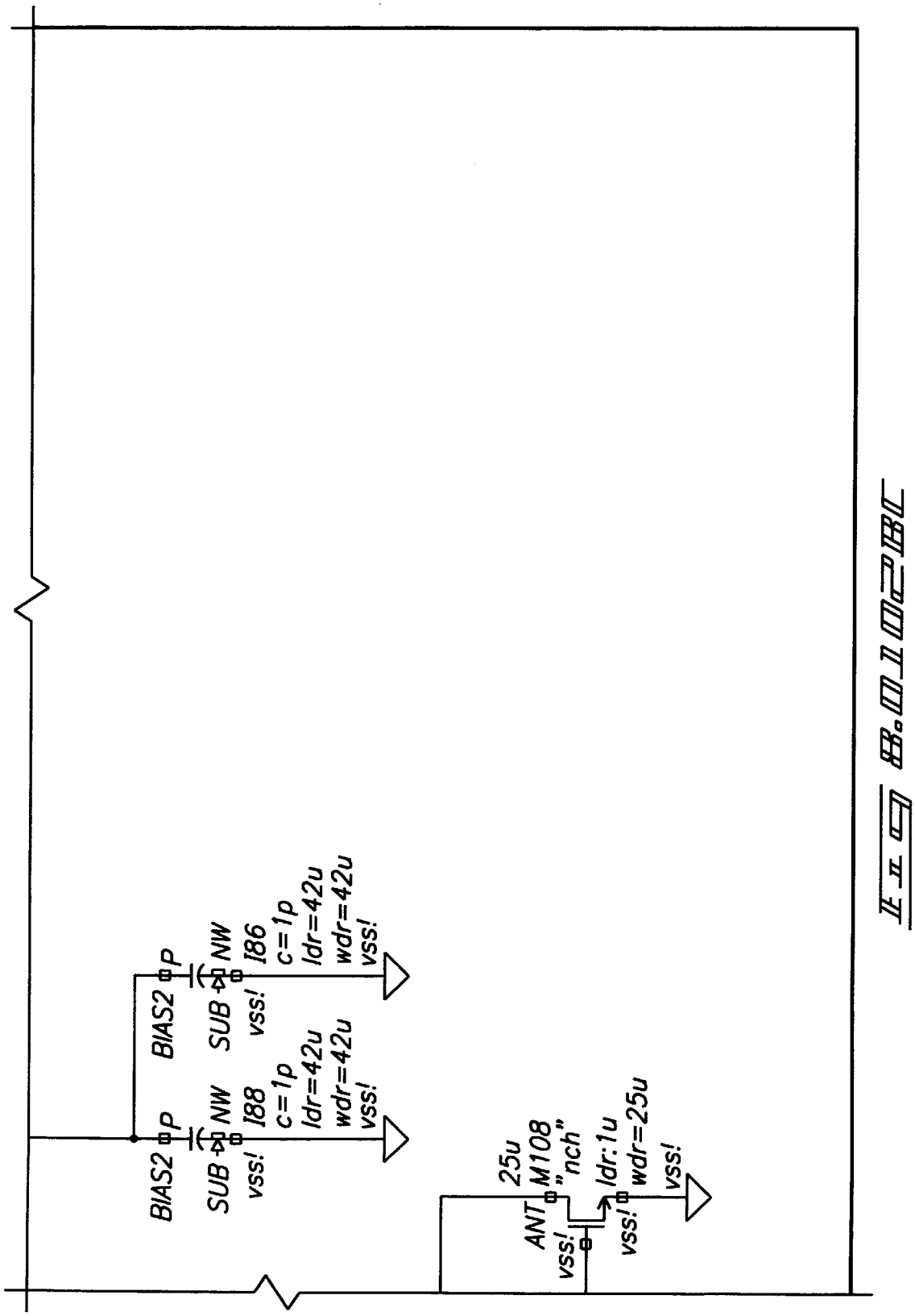


FIG 8.01102BIC

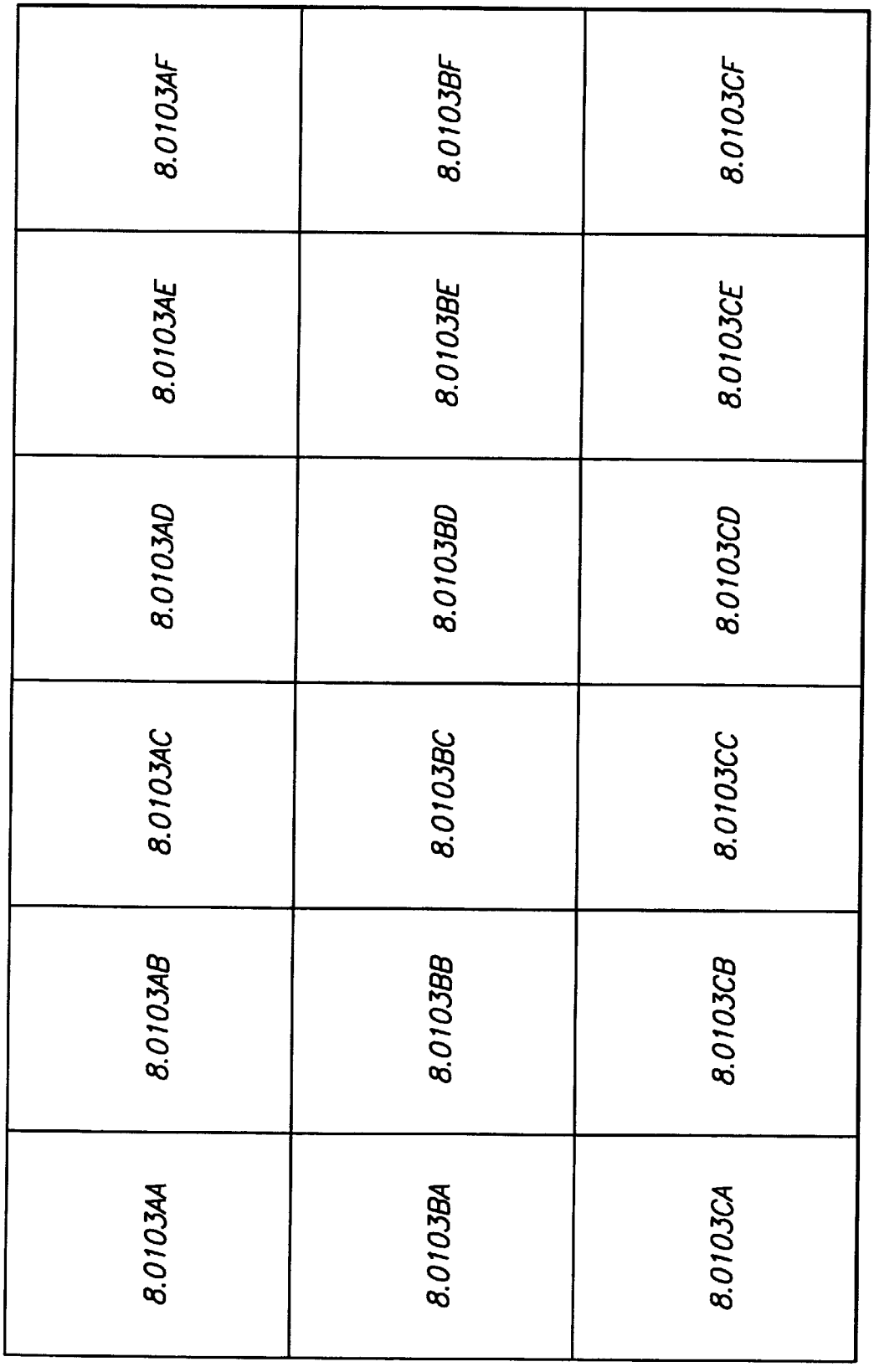

8.0103AA
8.0103AB
8.0103AC
8.0103AD
8.0103AE
8.0103AF
8.0103BA
8.0103BB
8.0103BC
8.0103BD
8.0103BE
8.0103BF
8.0103CA
8.0103CB
8.0103CC
8.0103CD
8.0103CE
8.0103CF

FIG. 8.0103

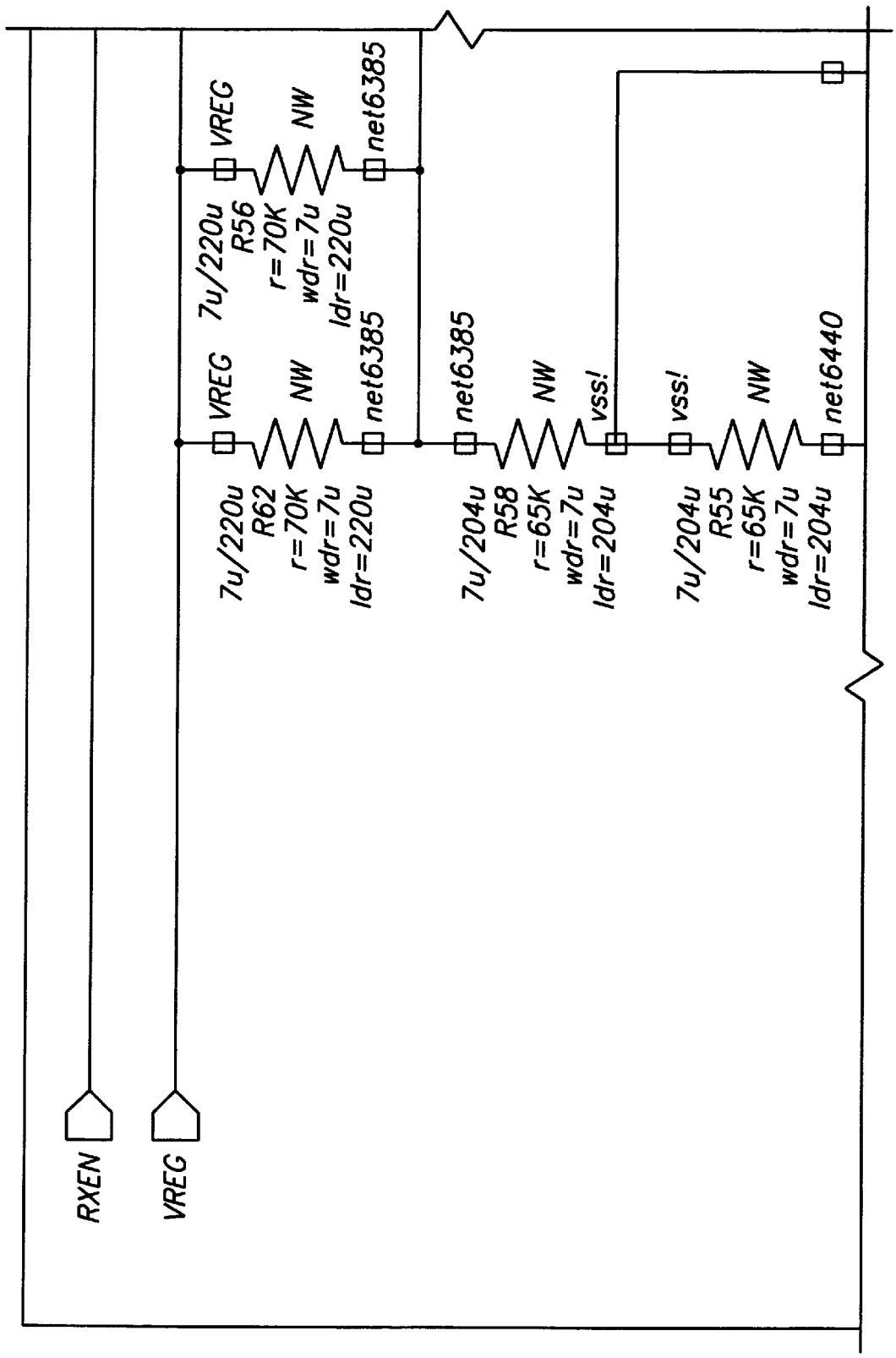

RXEN
VREG
7u/220u
R62
r=70K
wdr=7u
ldr=220u
VREG
NW
net6385
7u/220u
R56
r=70K
wdr=7u
ldr=220u
VREG
NW
net6385
7u/204u
R58
r=65K
wdr=7u
ldr=204u
net6385
NW
vss!
7u/204u
R55
r=65K
wdr=7u
ldr=204u
vss!
NW
net6440

FIG. 88.00

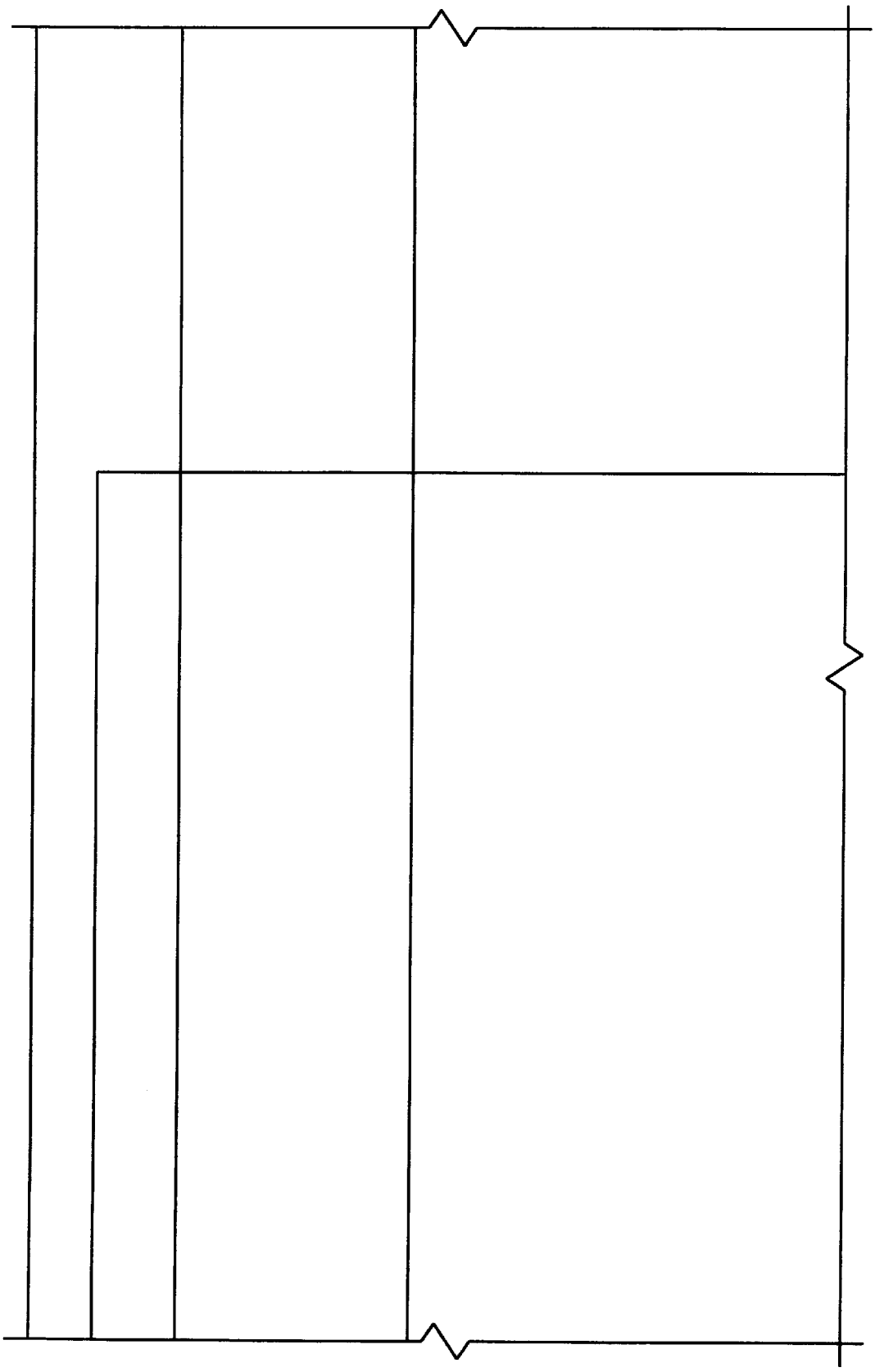


FIG 88,708

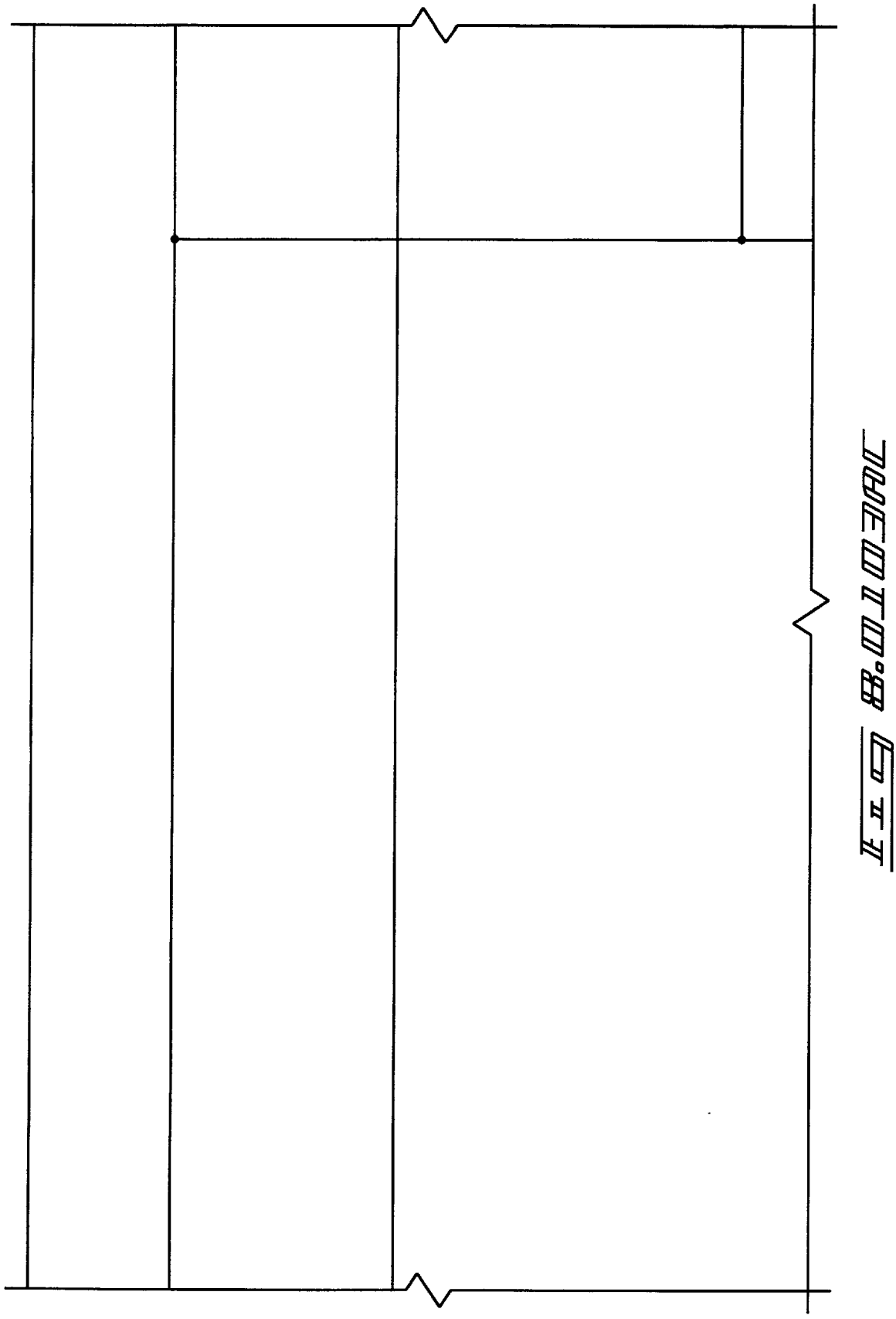


FIG. 68

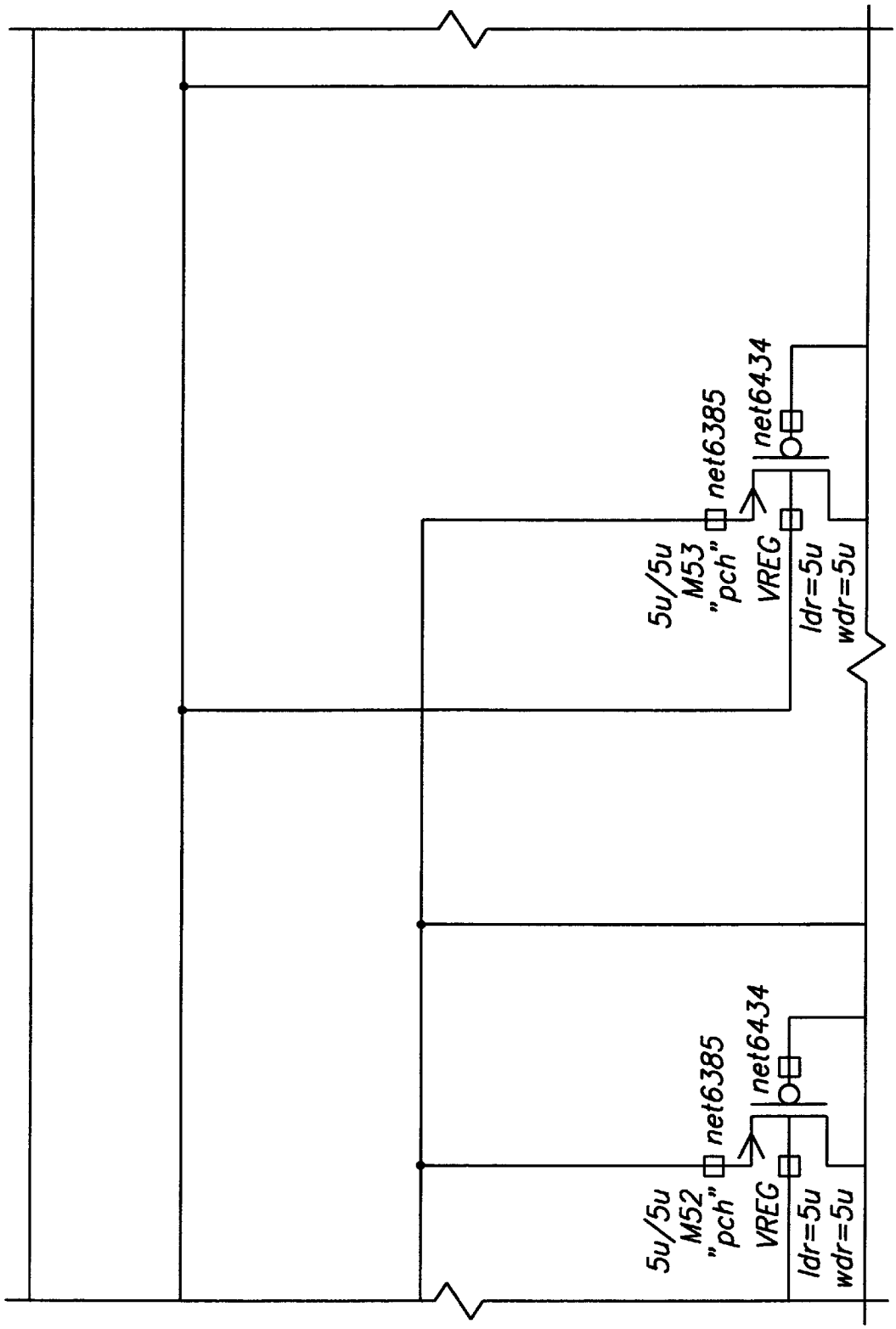

net6434
net6385
5u/5u
M53
"pch"
VREG
ldr=5u
wdr=5u
net6434
net6385
5u/5u
M52
"pch"
VREG
ldr=5u
wdr=5u

FIG. 1141

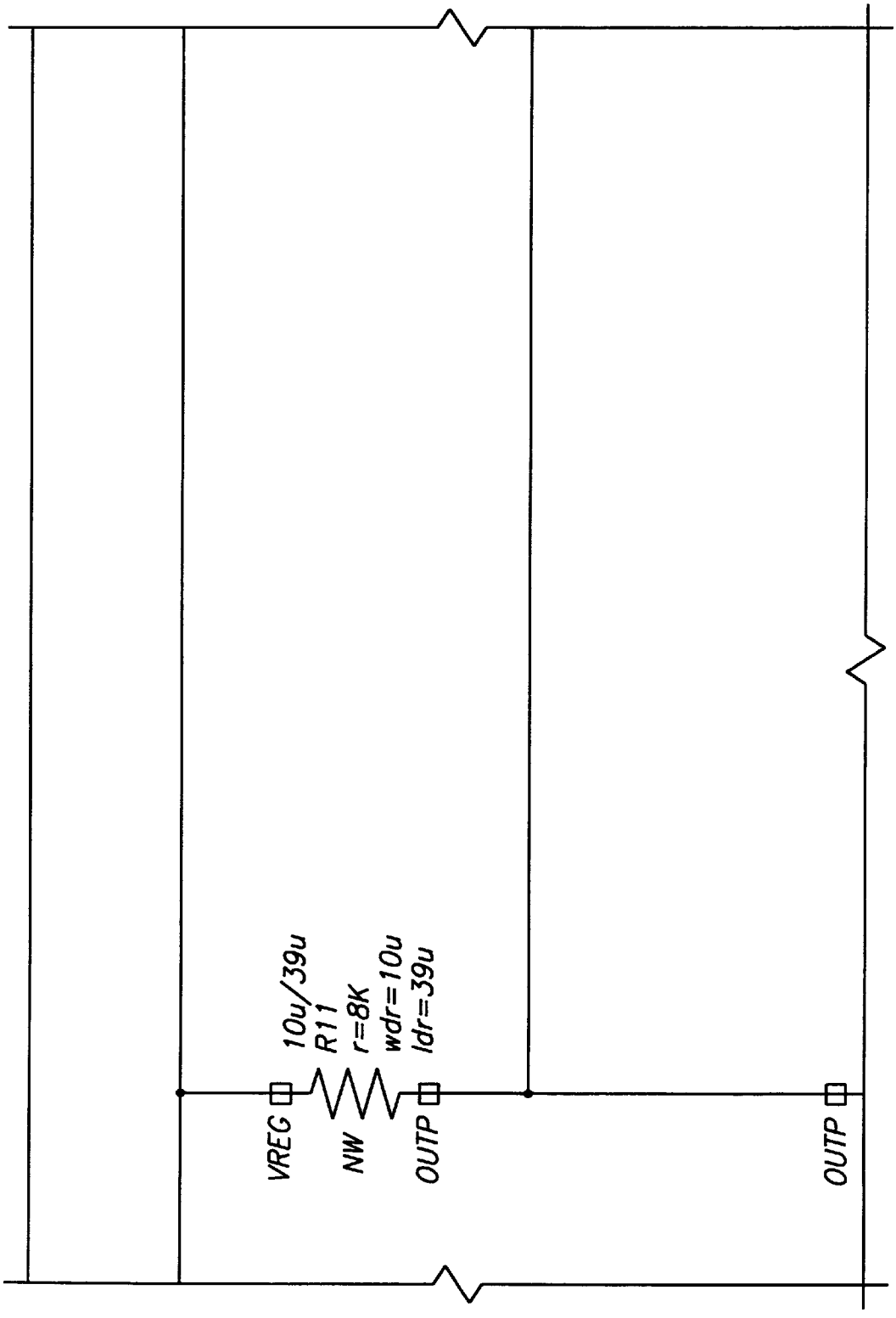


FIG 88.0110

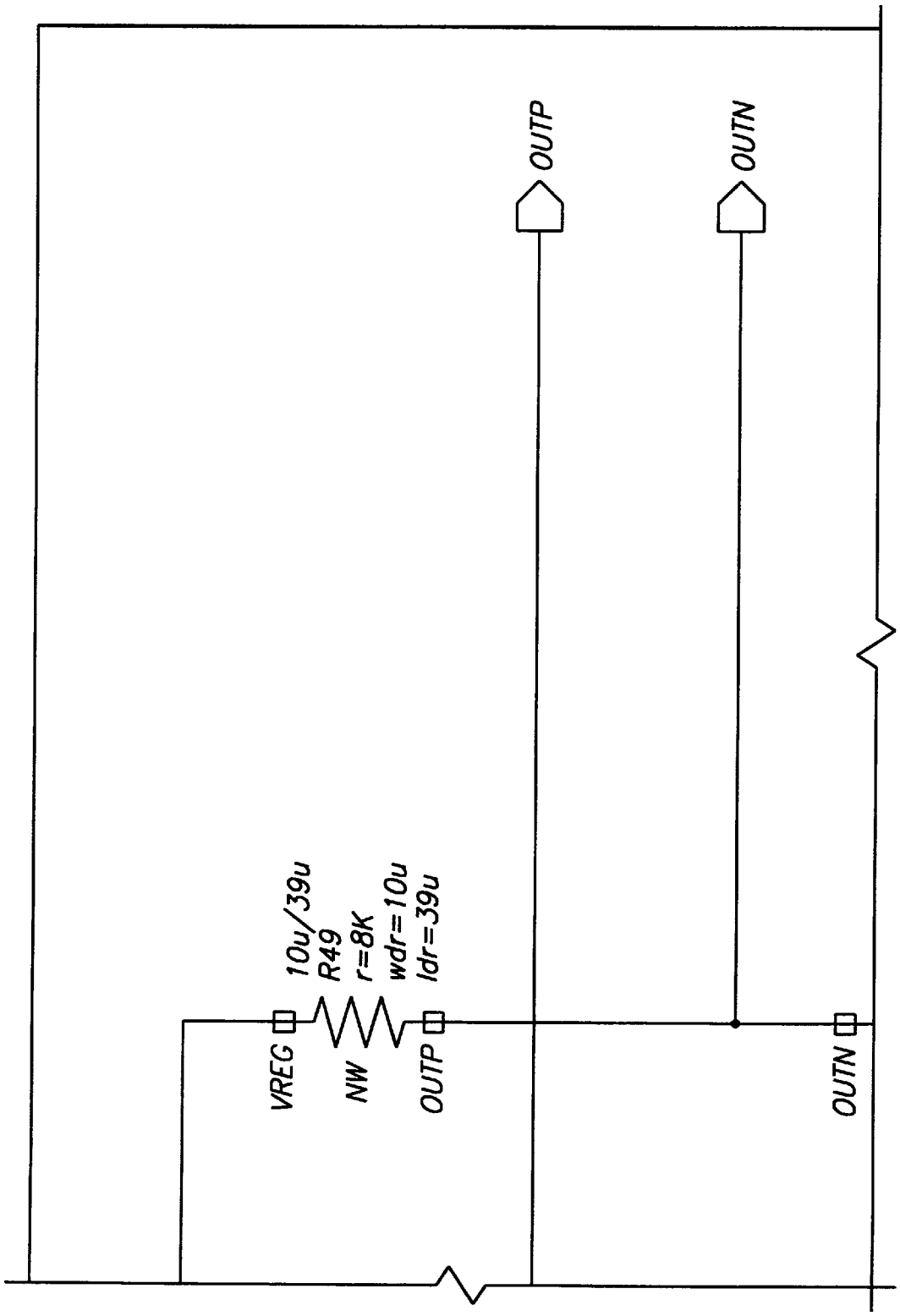


FIG. 88.00 (PRIOR ART)

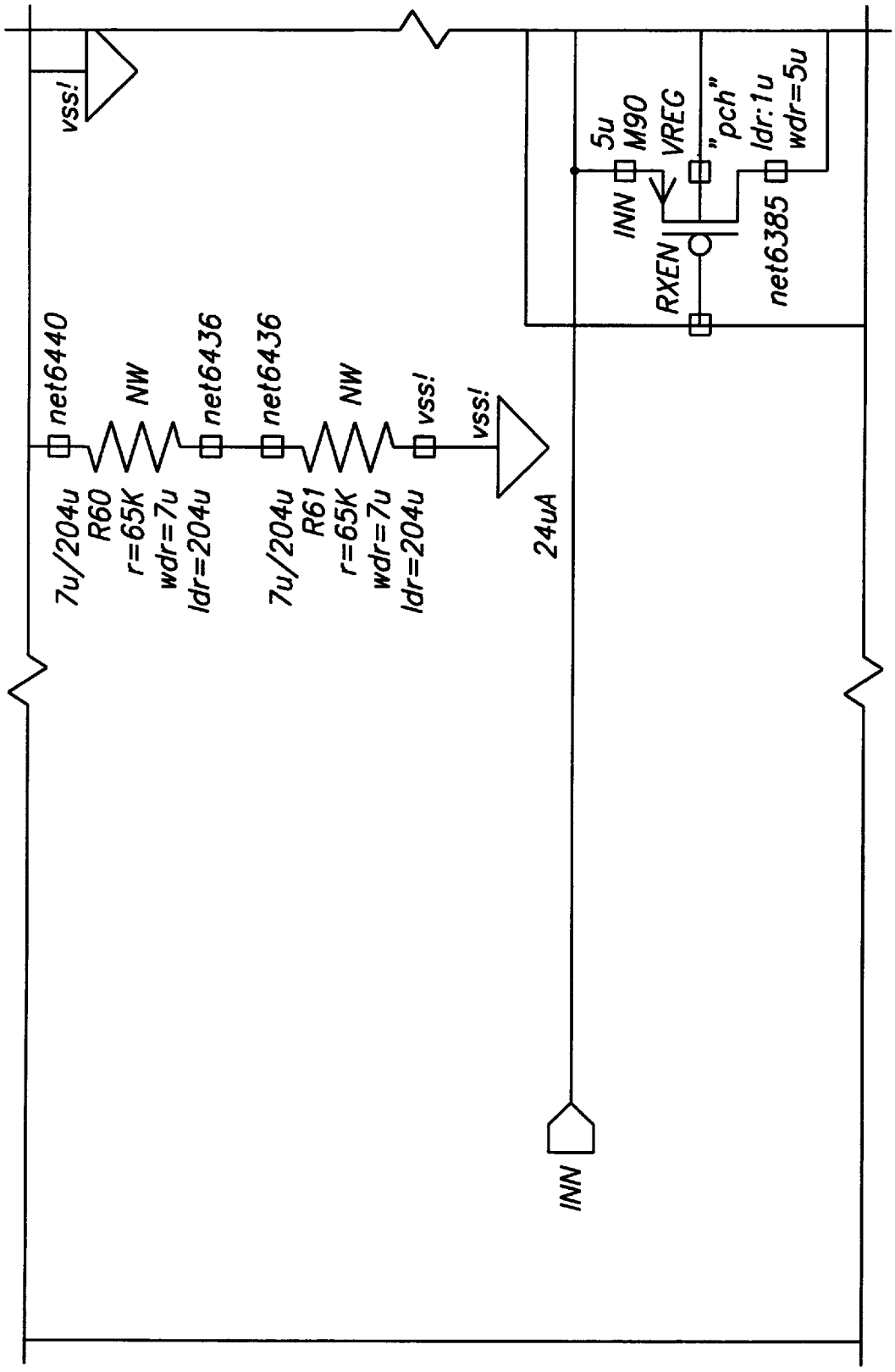
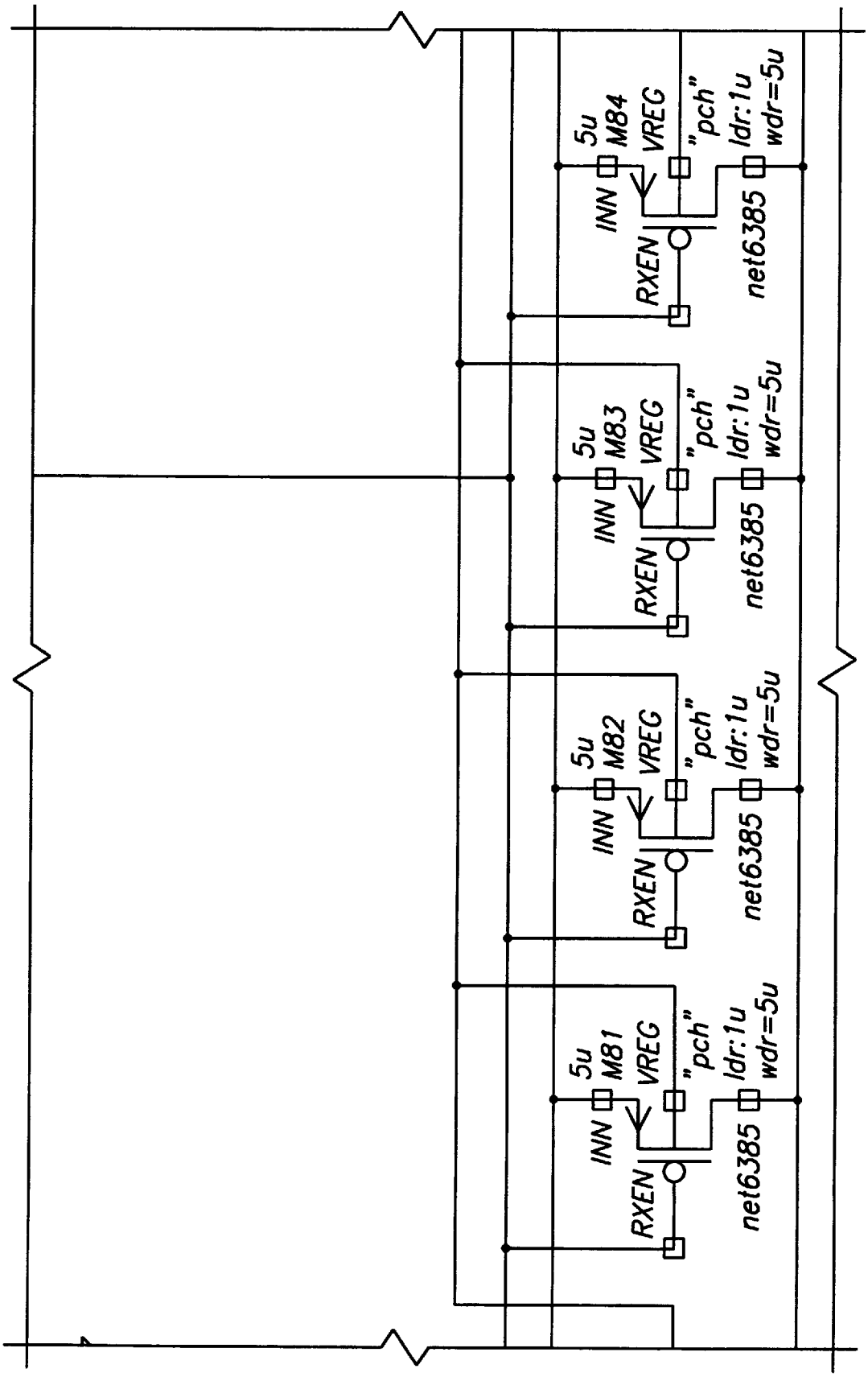

vss!
net6440
7u/204u
R60
r=65K
wdr=7u
ldr=204u
NW
net6436
net6436
7u/204u
R61
r=65K
wdr=7u
ldr=204u
NW
vss!
vss!
24uA
INN
5u
M90
INN
VREG
RXEN
"pch"
ldr:1u
wdr=5u
net6385

FIG. 8.0100


5u M84 VREG "pch" ldr:1u wdr=5u
INN
RXEN
net6385
5u M83 VREG "pch" ldr:1u wdr=5u
INN
RXEN
net6385
5u M82 VREG "pch" ldr:1u wdr=5u
INN
RXEN
net6385
5u M81 VREG "pch" ldr:1u wdr=5u
INN
RXEN
net6385

Фиг 8.00108

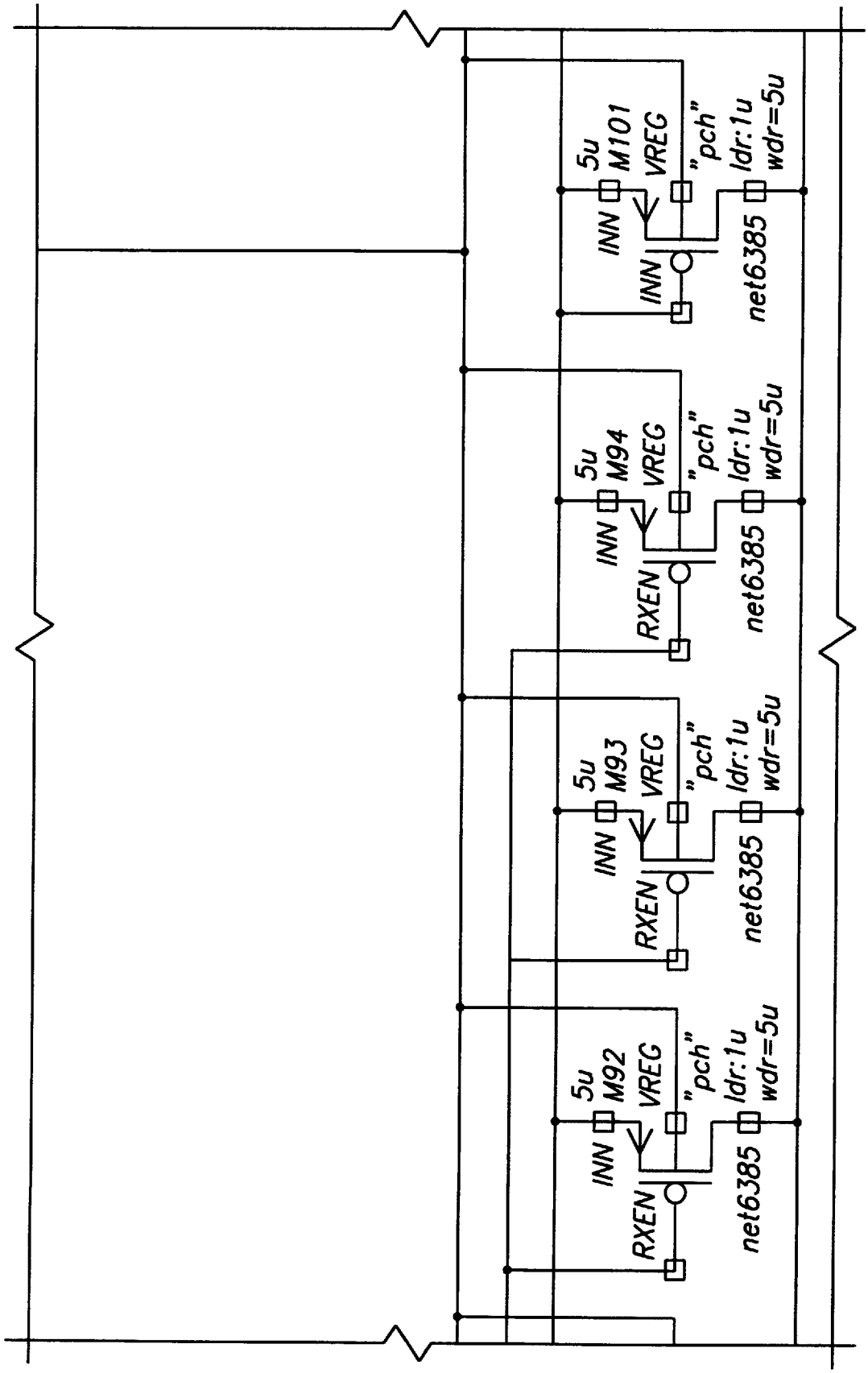

5u M101 VREG "pch" ldr:1u wdr=5u
INN
INN
net6385
5u M94 VREG "pch" ldr:1u wdr=5u
INN
RXEN
net6385
5u M93 VREG "pch" ldr:1u wdr=5u
INN
RXEN
net6385
5u M92 VREG "pch" ldr:1u wdr=5u
INN
RXEN
net6385

FIG. 88.00

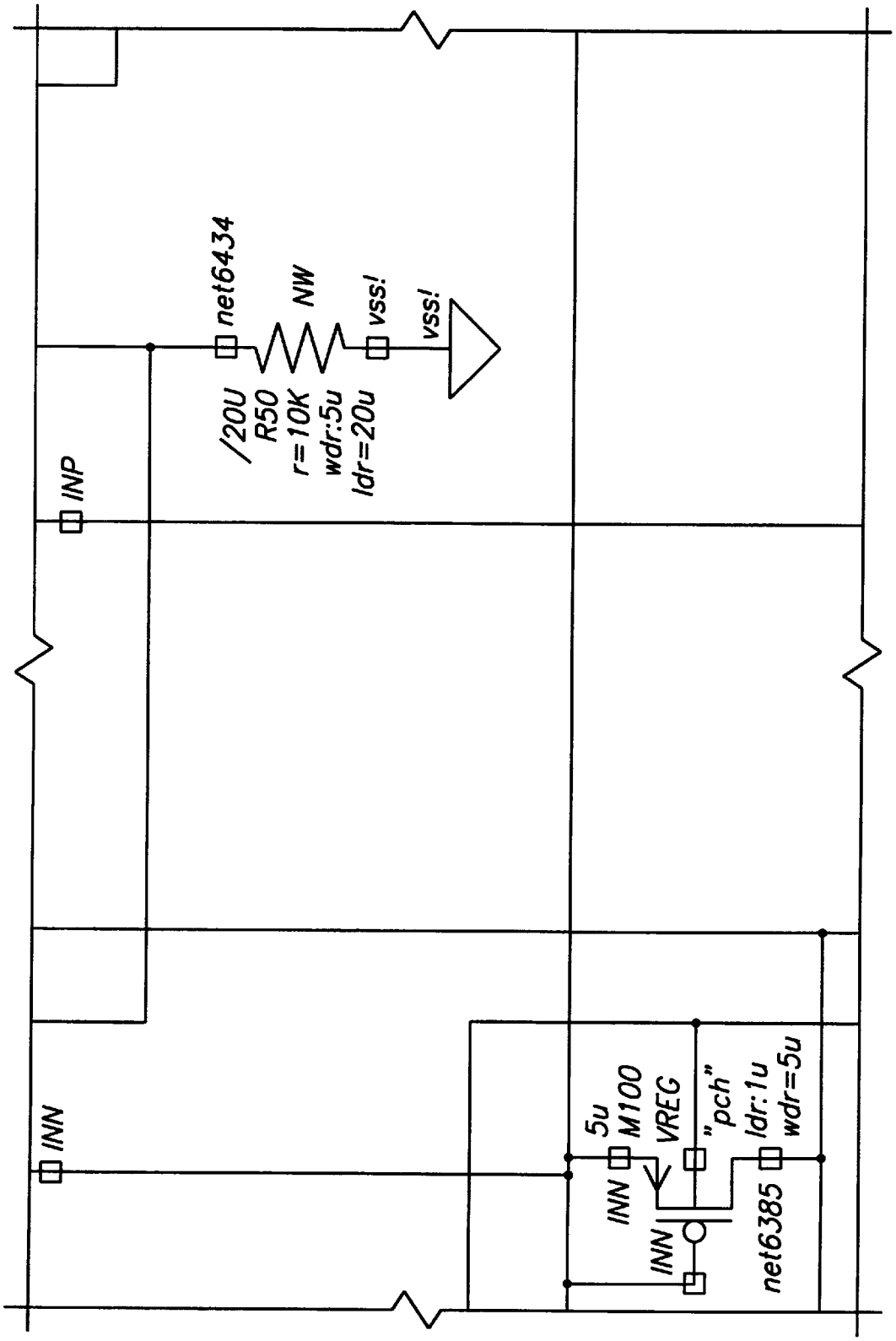

net6434
NW
vss!
vss!
/20U
R50
r=10K
wdr:5u
ldr=20u
INP
INN
5u
M100
VREG
"pch"
ldr:1u
wdr=5u
INN
INN
net6385

FIG 88.00188

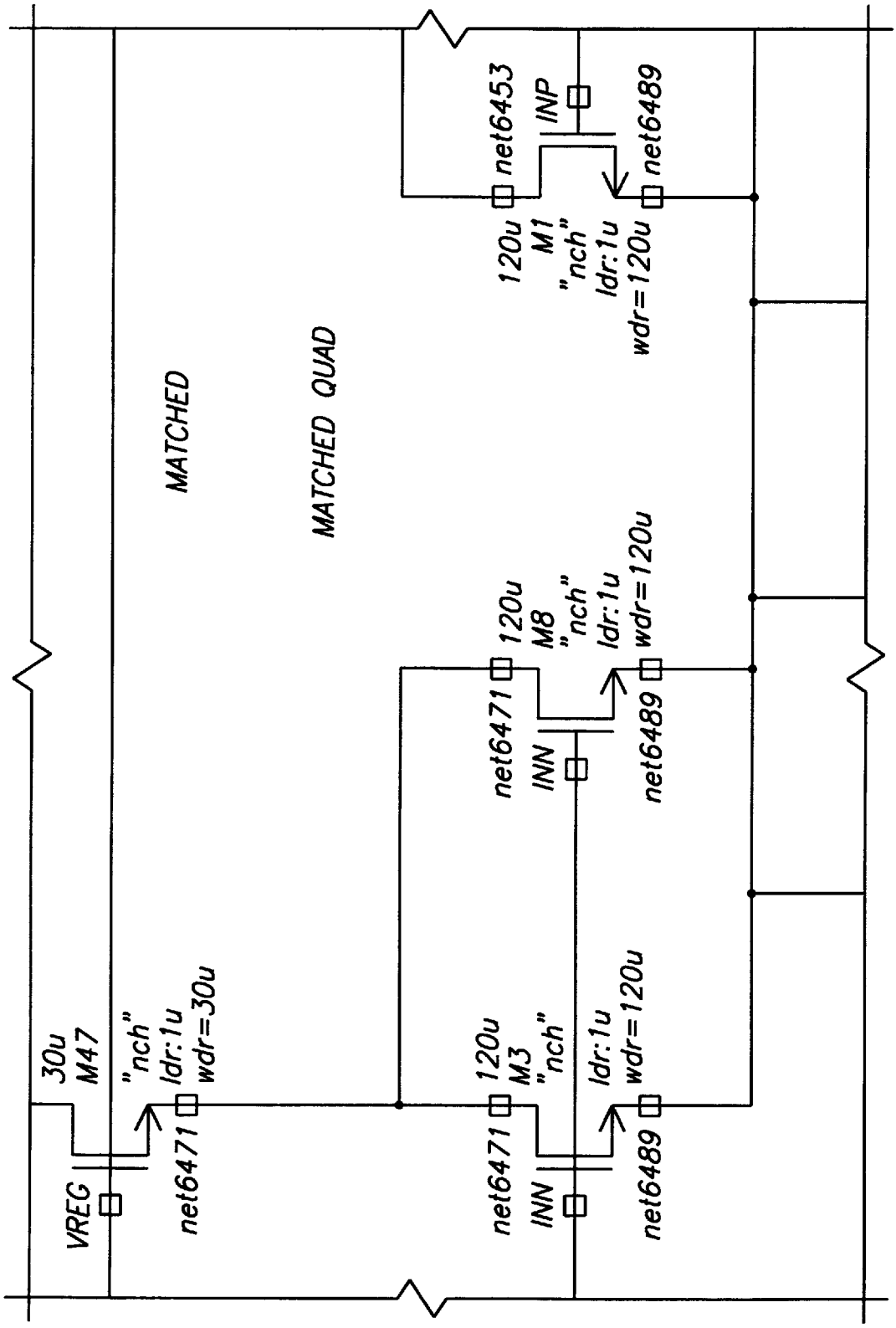

MATCHED
MATCHED QUAD
net6453
INP
net6489
120u
M1
"nch"
ldr:1u
wdr=120u
net6471
INN
net6489
120u
M8
"nch"
ldr:1u
wdr=120u
VREG
net6471
30u
M47
"nch"
ldr:1u
wdr=30u
net6471
INN
net6489
120u
M3
"nch"
ldr:1u
wdr=120u

FIG 1108

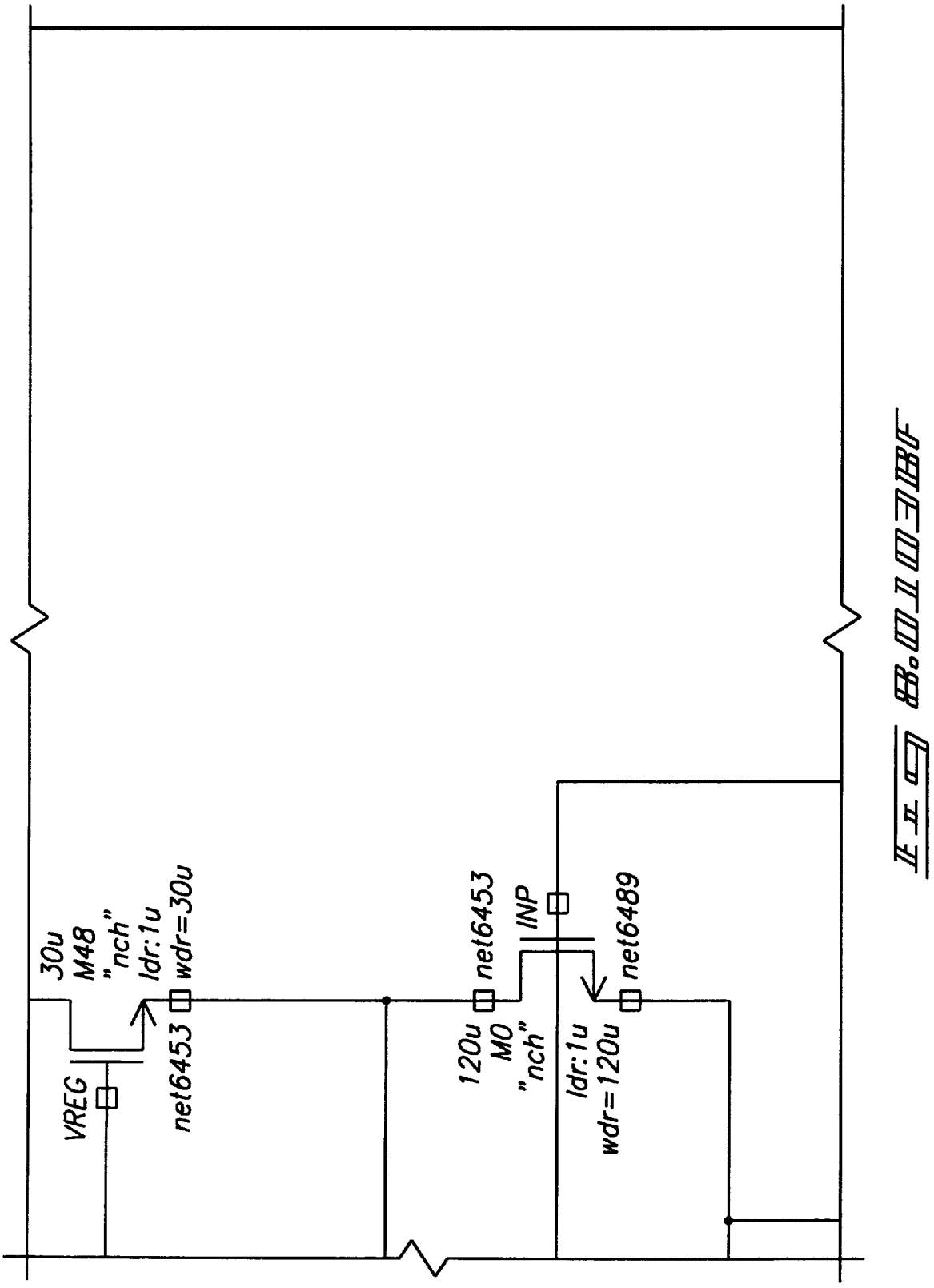


FIG. 88.00 II 00 3 1 8 F

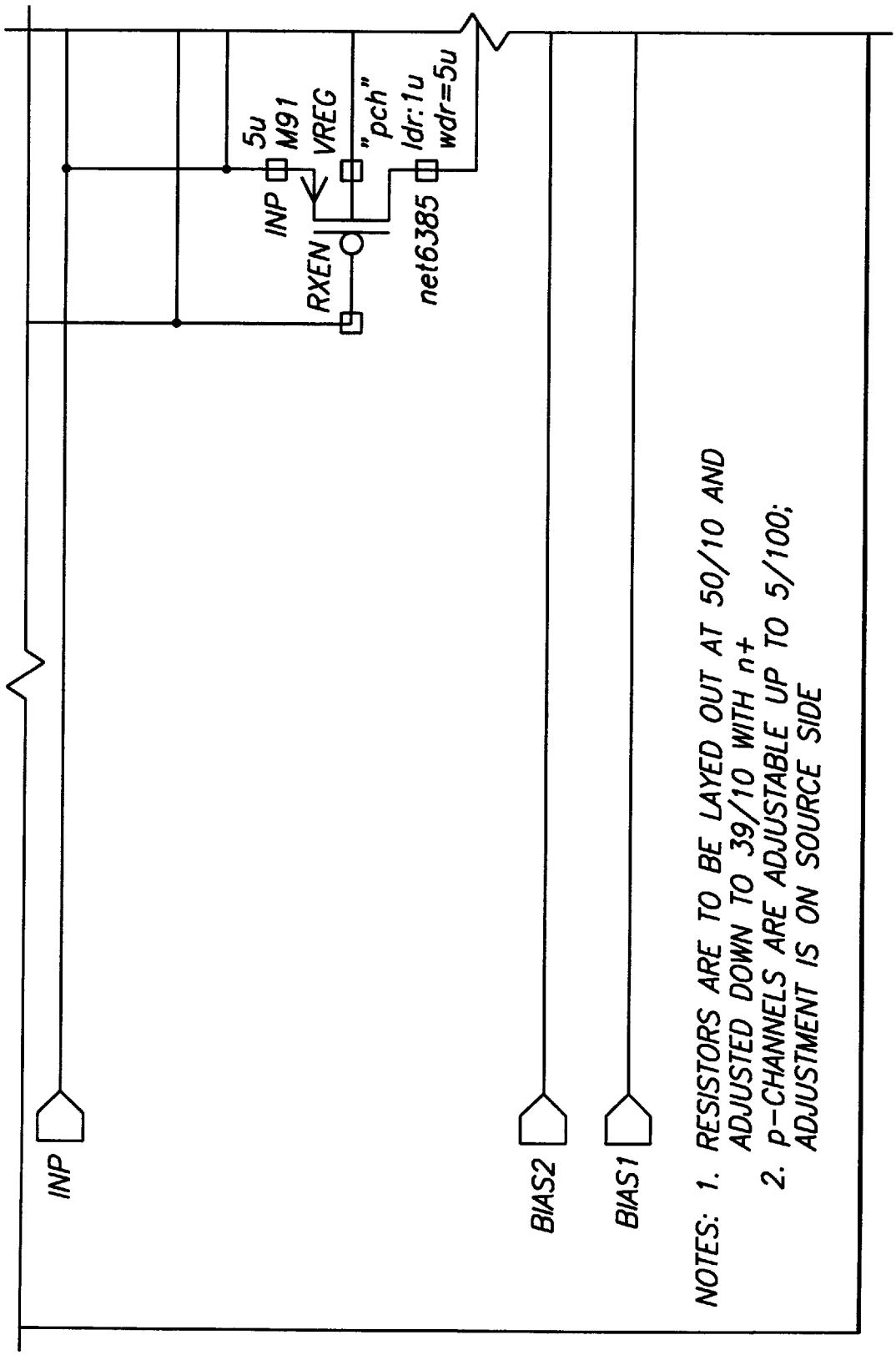


FIG. 88.00 (PRIOR ART)

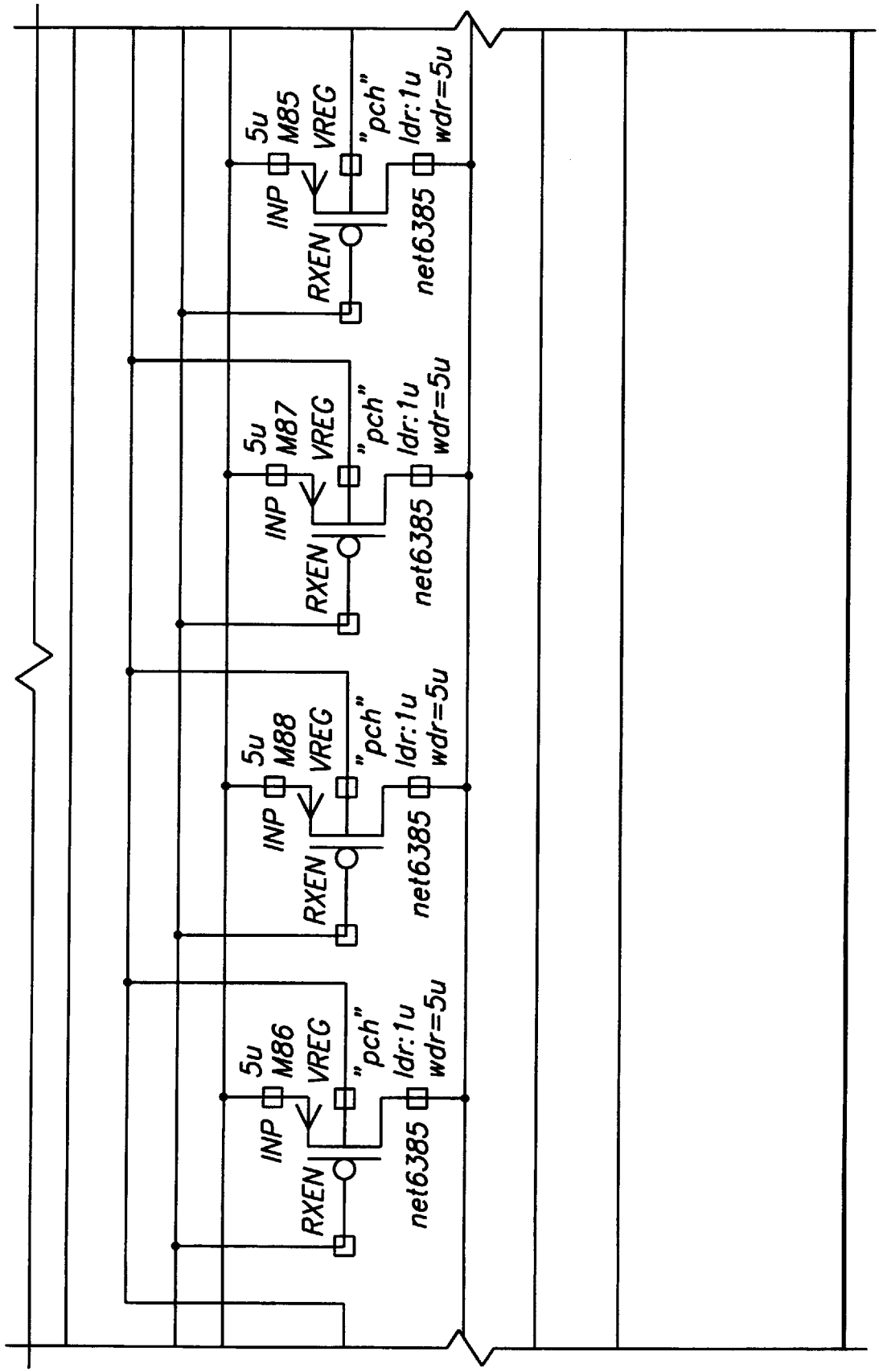

5u M85 VREG "pch" ldr:1u wdr=5u
INP
RXEN
net6385
5u M87 VREG "pch" ldr:1u wdr=5u
INP
RXEN
net6385
5u M88 VREG "pch" ldr:1u wdr=5u
INP
RXEN
net6385
5u M86 VREG "pch" ldr:1u wdr=5u
INP
RXEN
net6385

FIG. 88,001

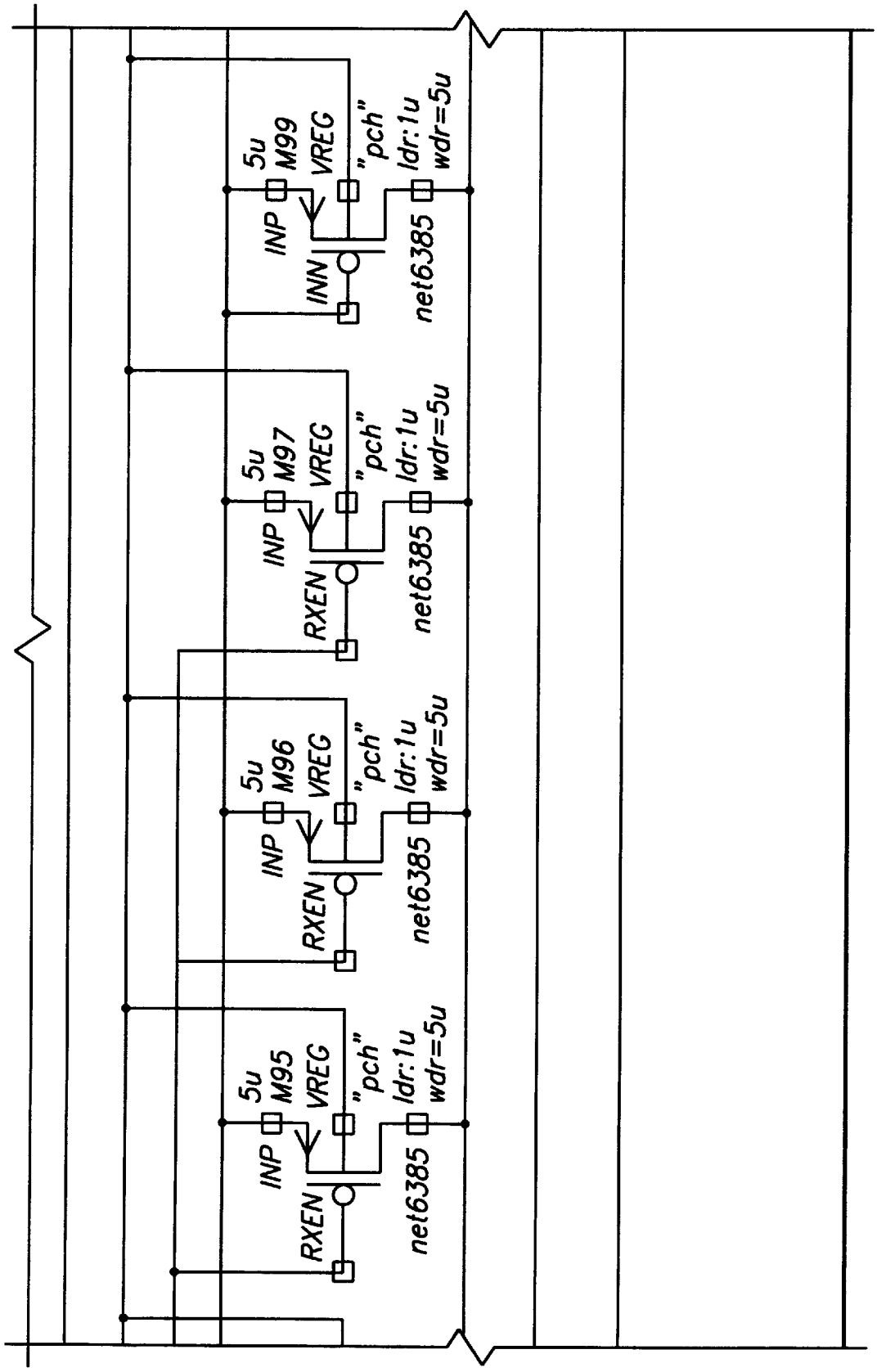

5u M99 VREG "pch" ldr:1u wdr=5u
INP
INN
net6385
5u M97 VREG "pch" ldr:1u wdr=5u
INP
RXEN
net6385
5u M96 VREG "pch" ldr:1u wdr=5u
INP
RXEN
net6385
5u M95 VREG "pch" ldr:1u wdr=5u
INP
RXEN
net6385

FIG. 88.00IE

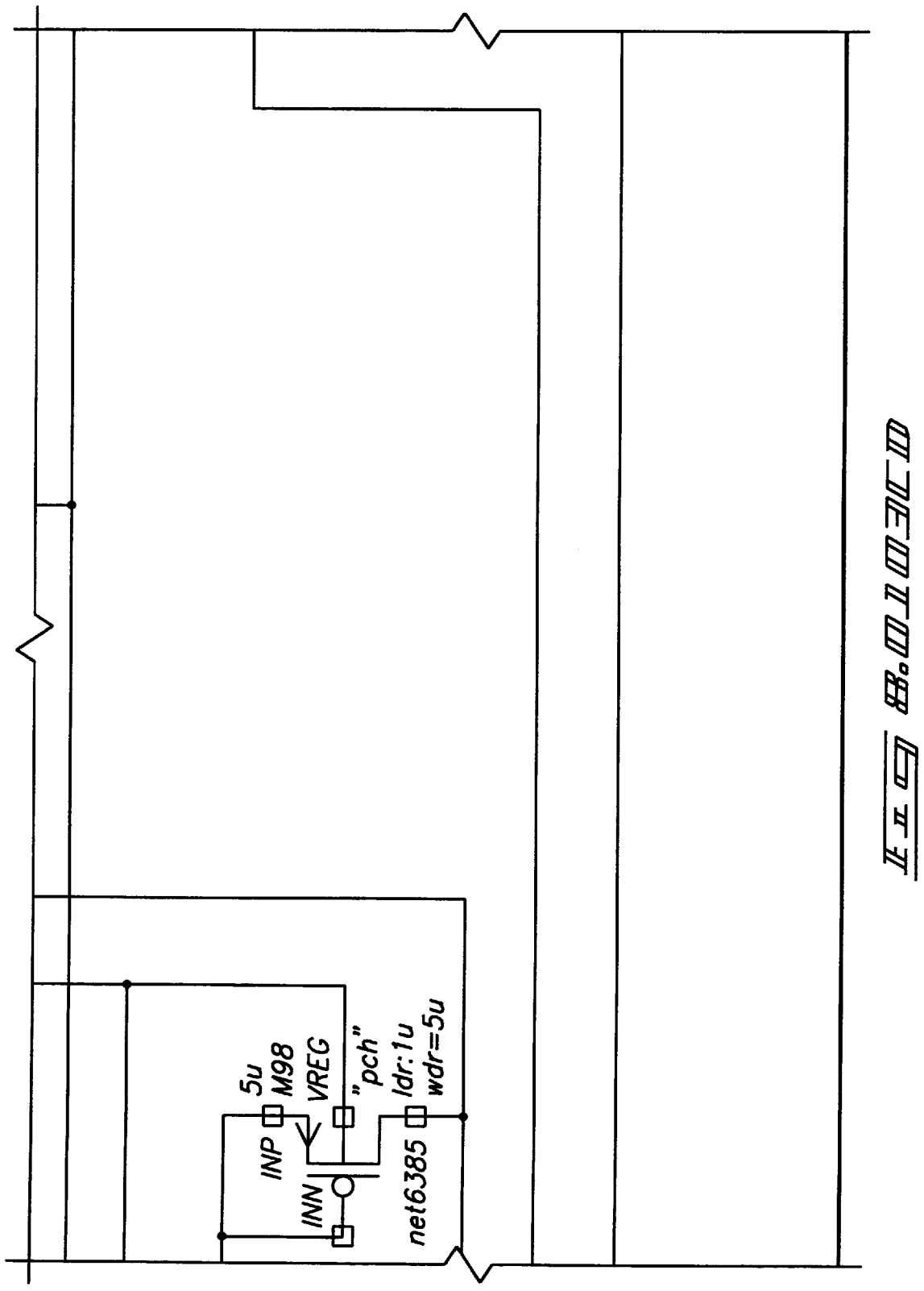


FIG. 88,010

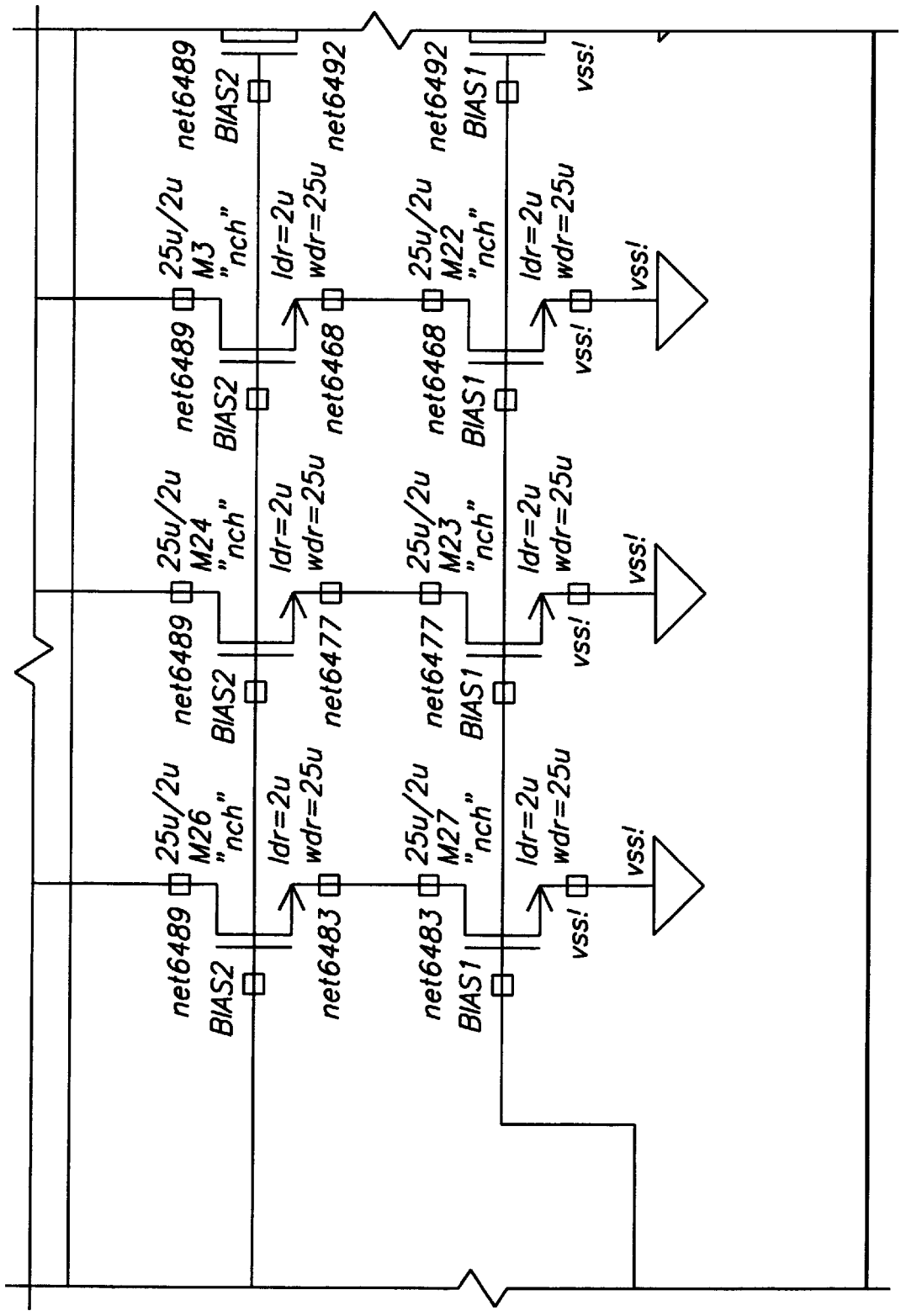

net6489
BIAS2
net6492
BIAS1
vss!
25u/2u
M3
"nch"
ldr=2u
wdr=25u
M22
M24
M23
M26
M27
net6468
net6477
net6483

FIG. 88.00136

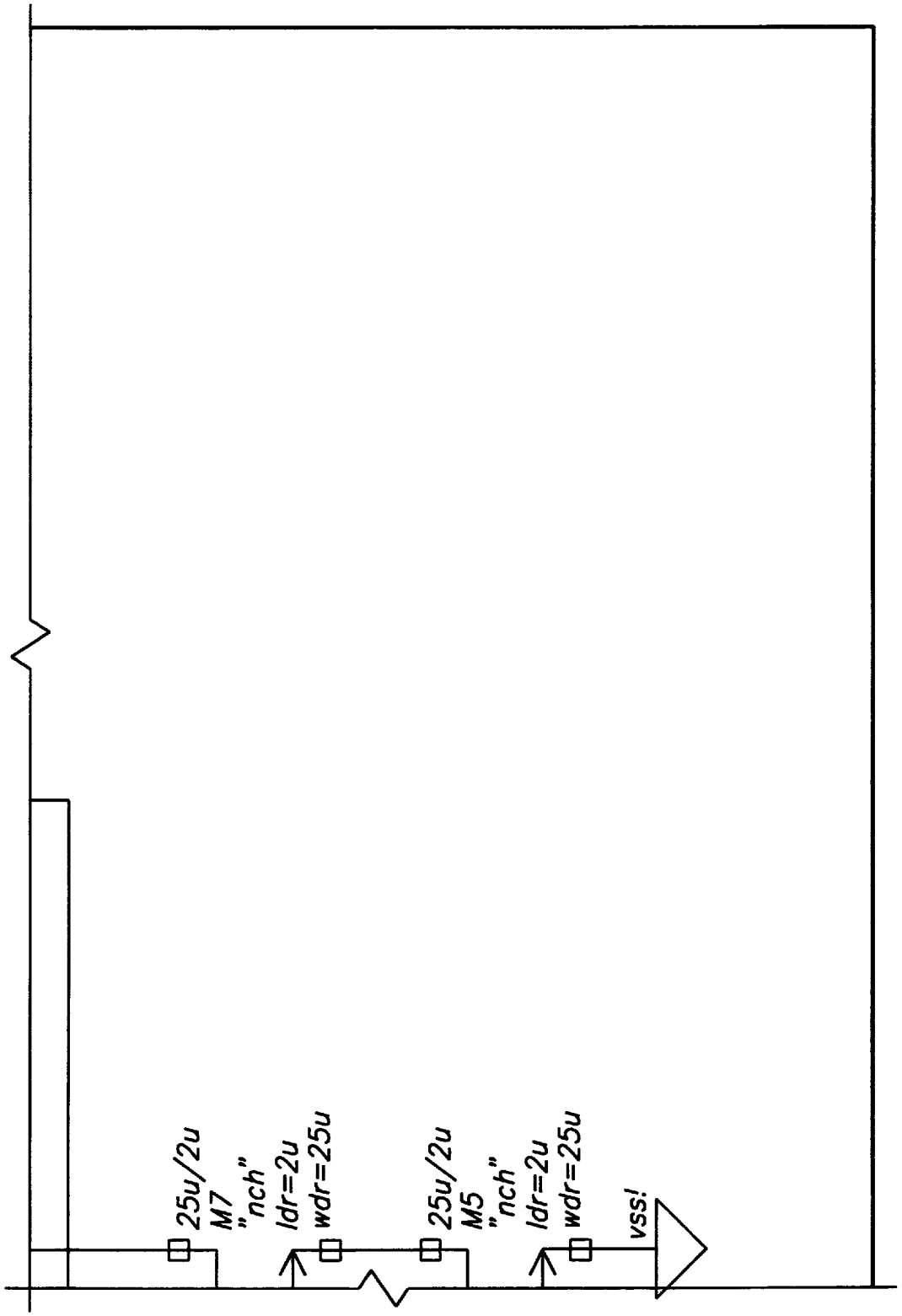


FIG 88

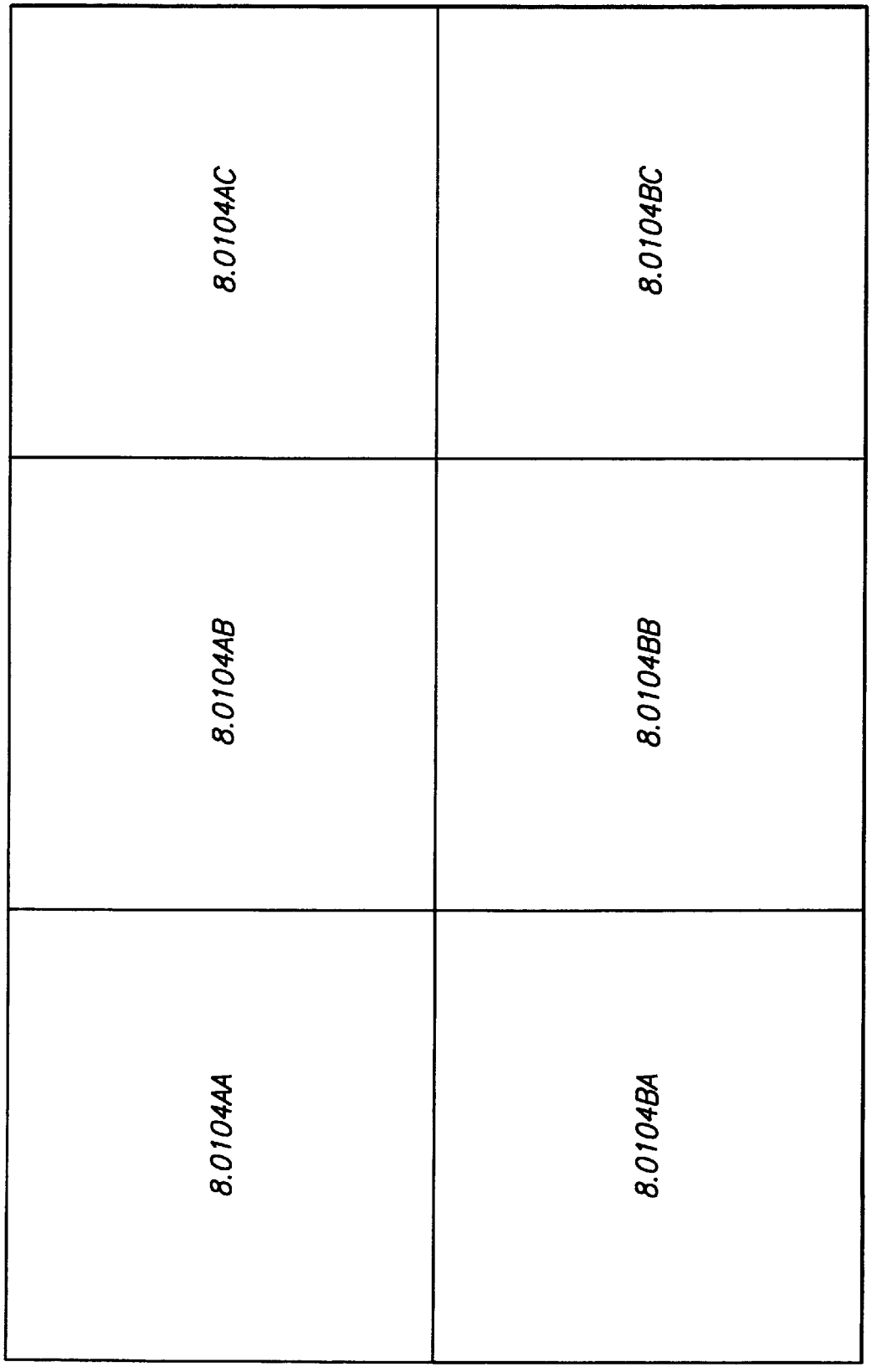


FIG 8.0104

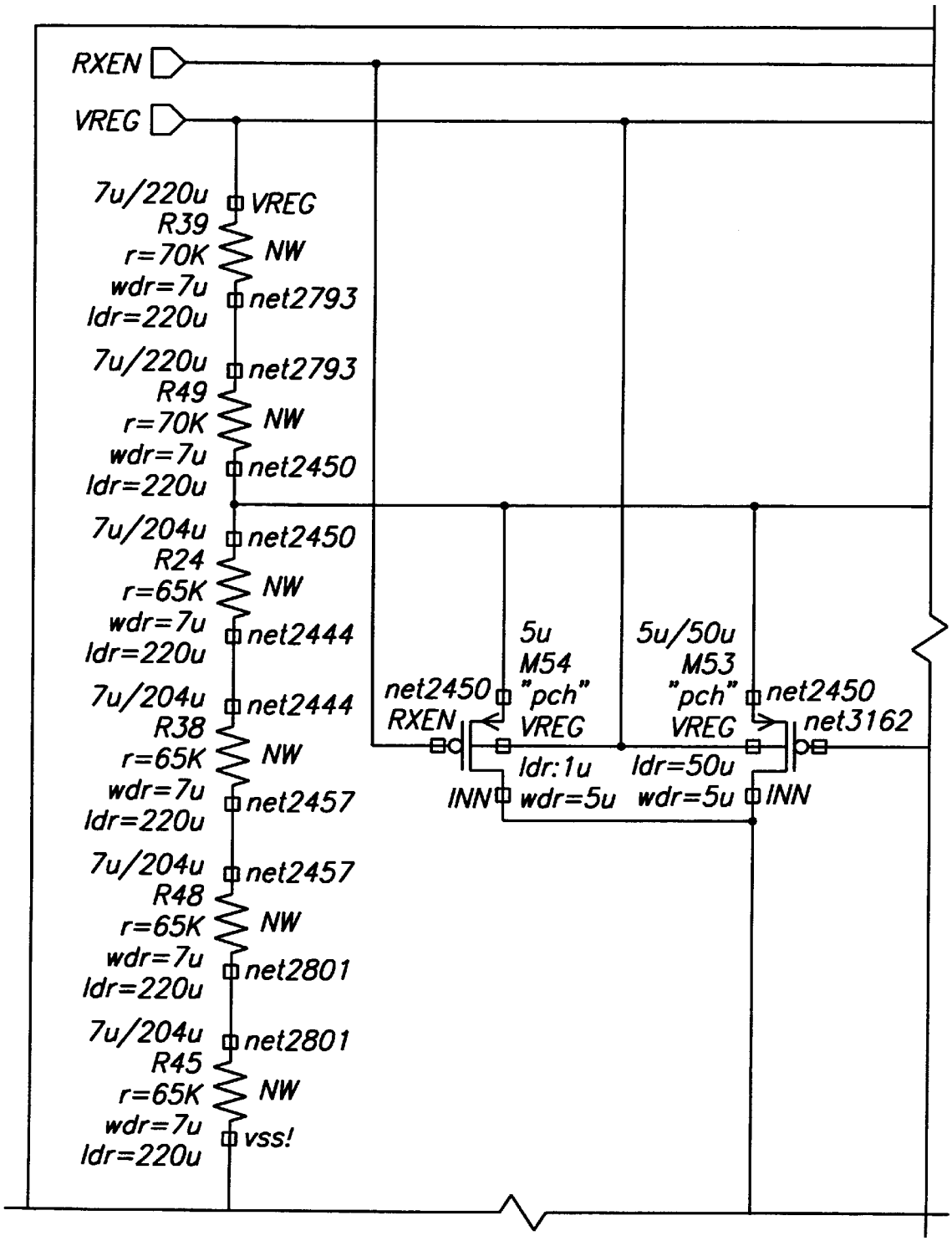


Fig 8.01074AA

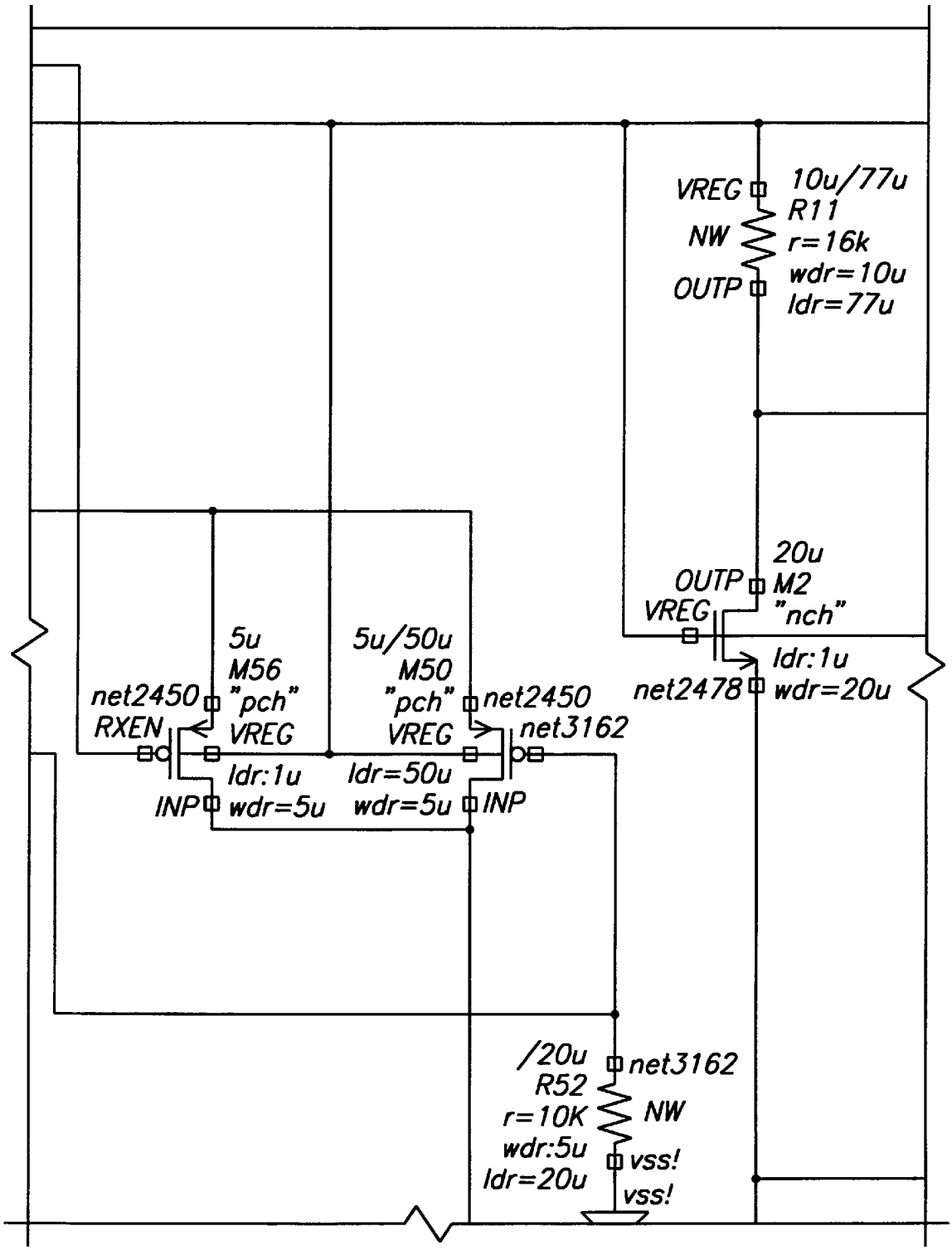


Fig 8.0110-AAB

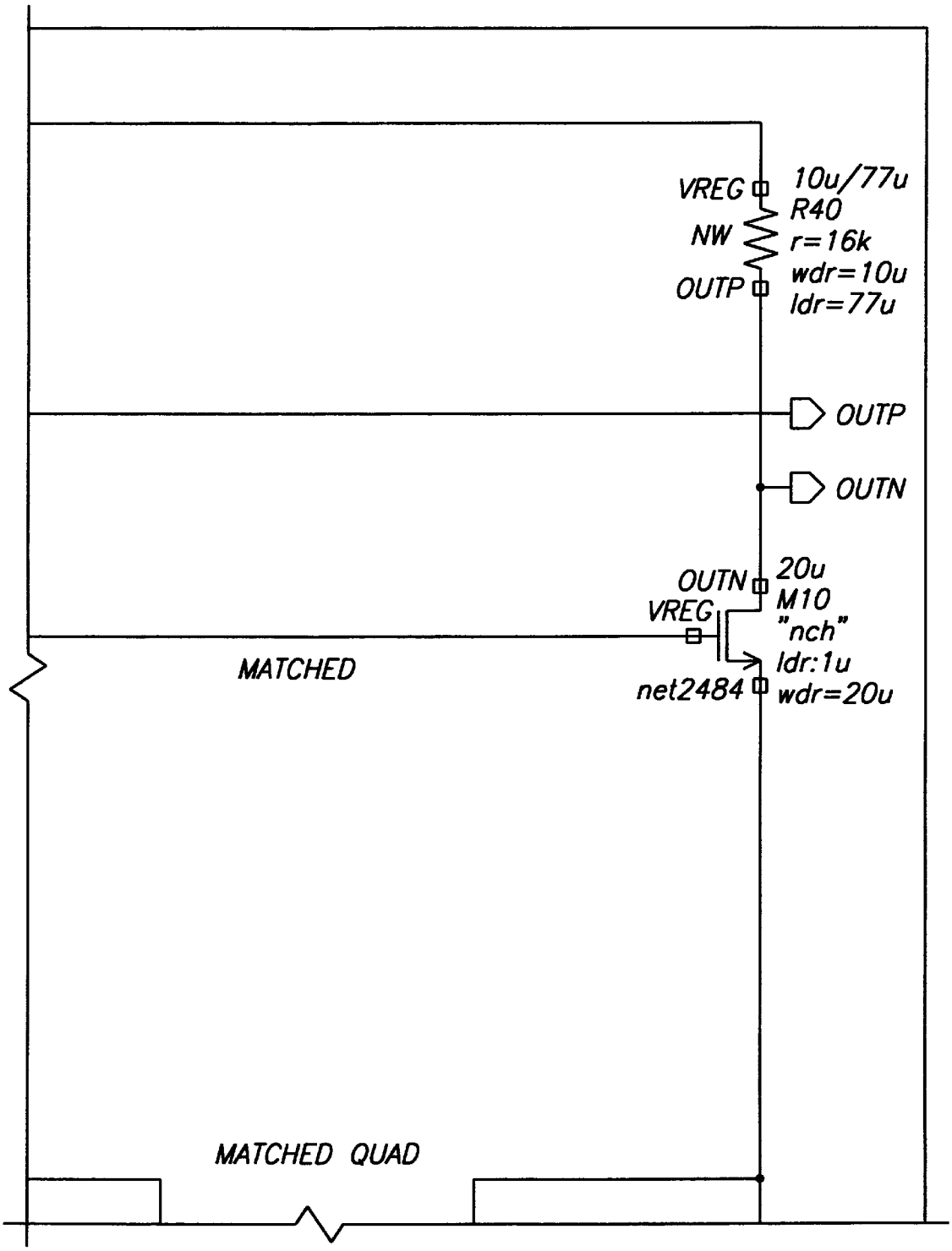

VREG
10u/77u
R40
NW
r=16k
wdr=10u
OUTP
ldr=77u
OUTP
OUTN
OUTN
20u
M10
VREG
"nch"
ldr:1u
MATCHED
net2484
wdr=20u
MATCHED QUAD

Fig 8.0104AC

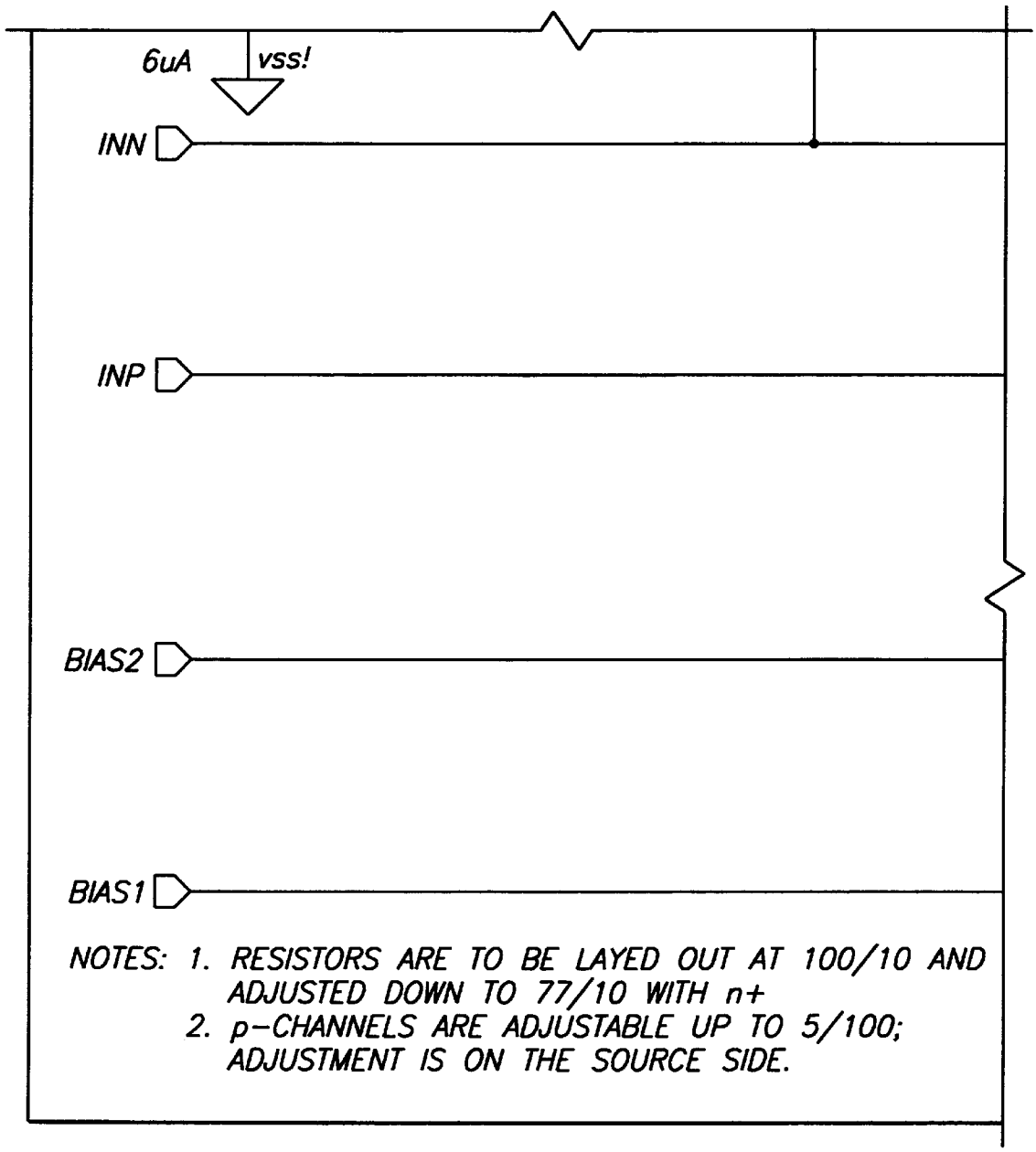


Fig 8.0110-1BA

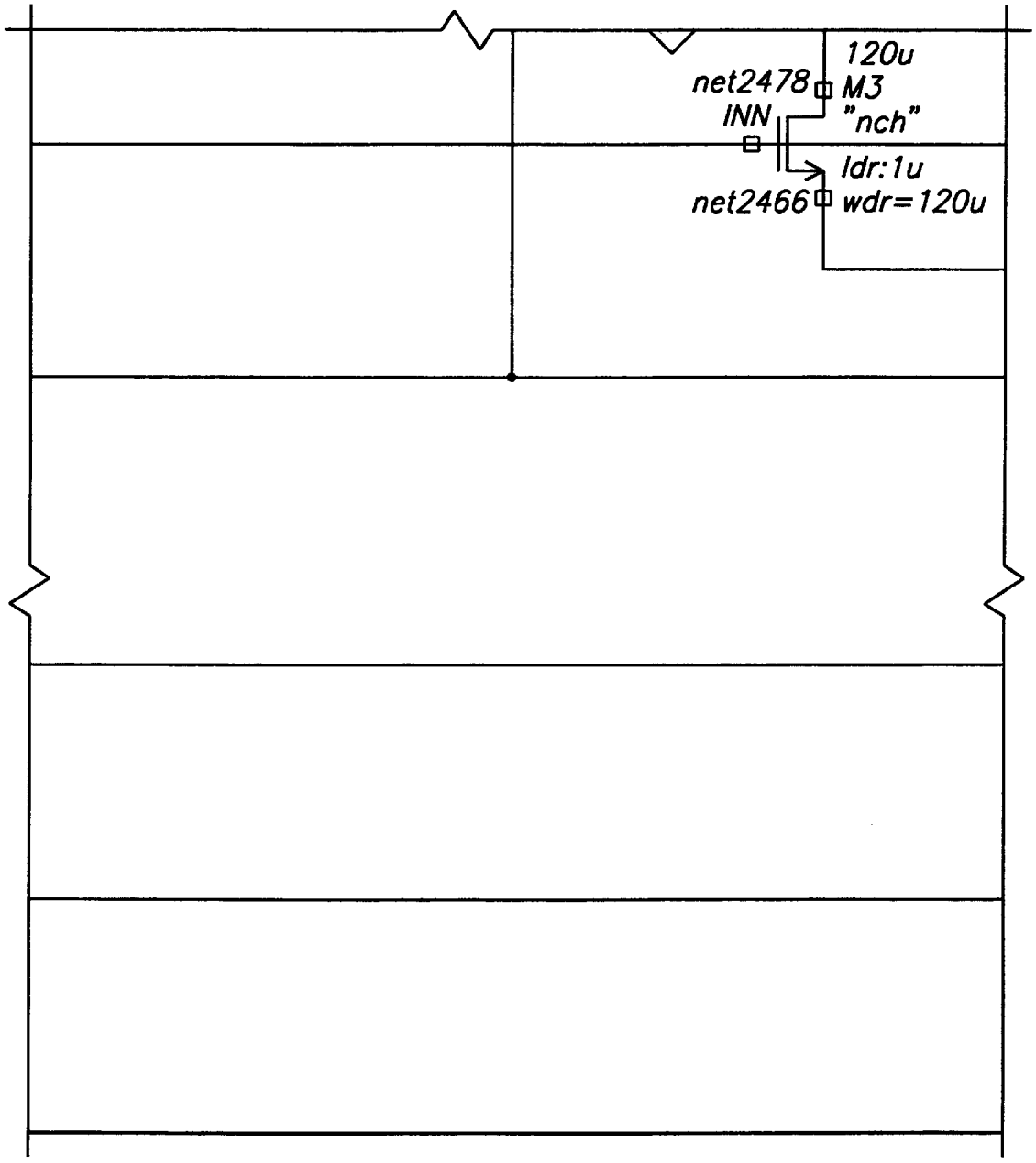


FIG 88.0110-1888

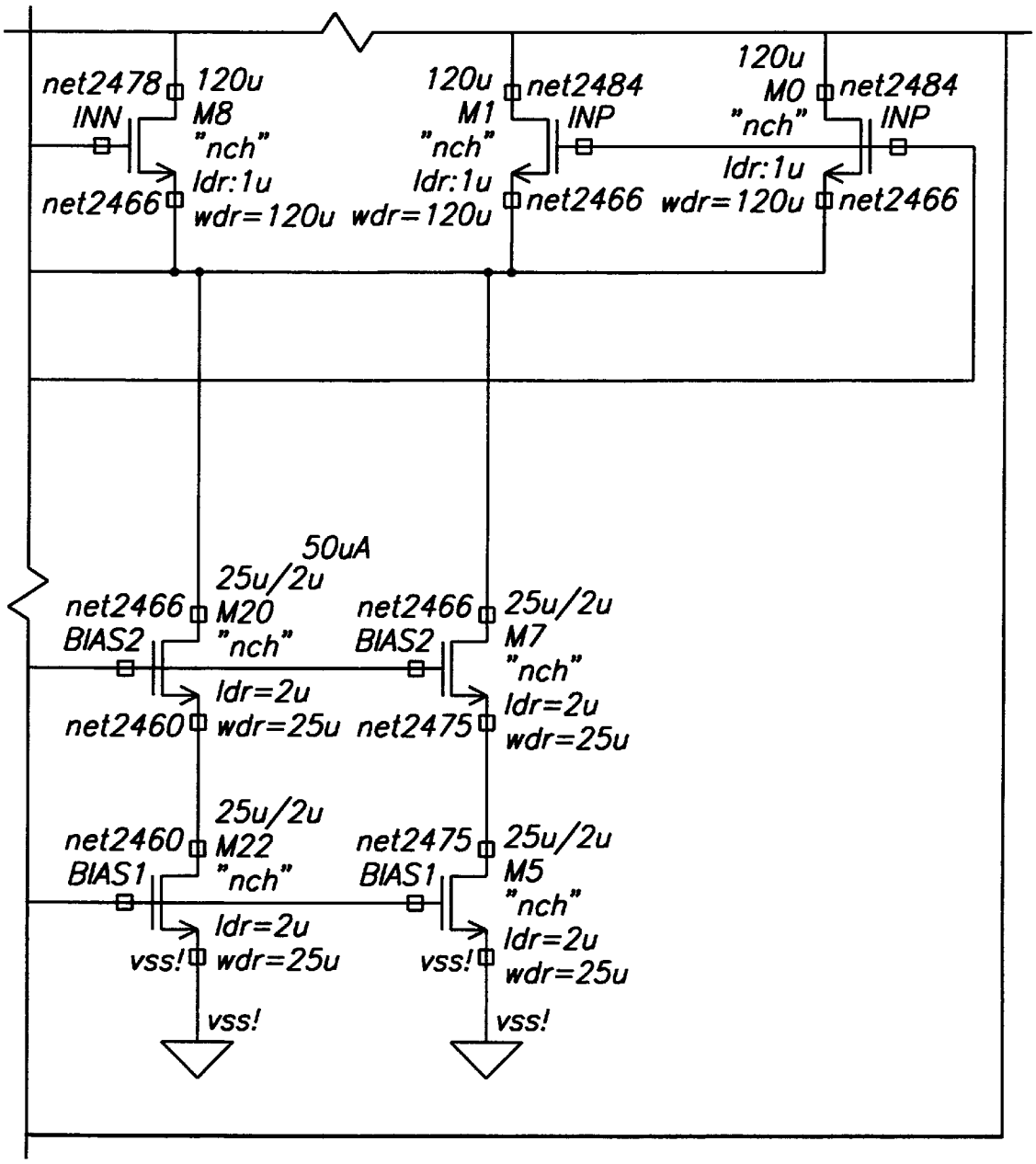


FIG. 80.1180-1180

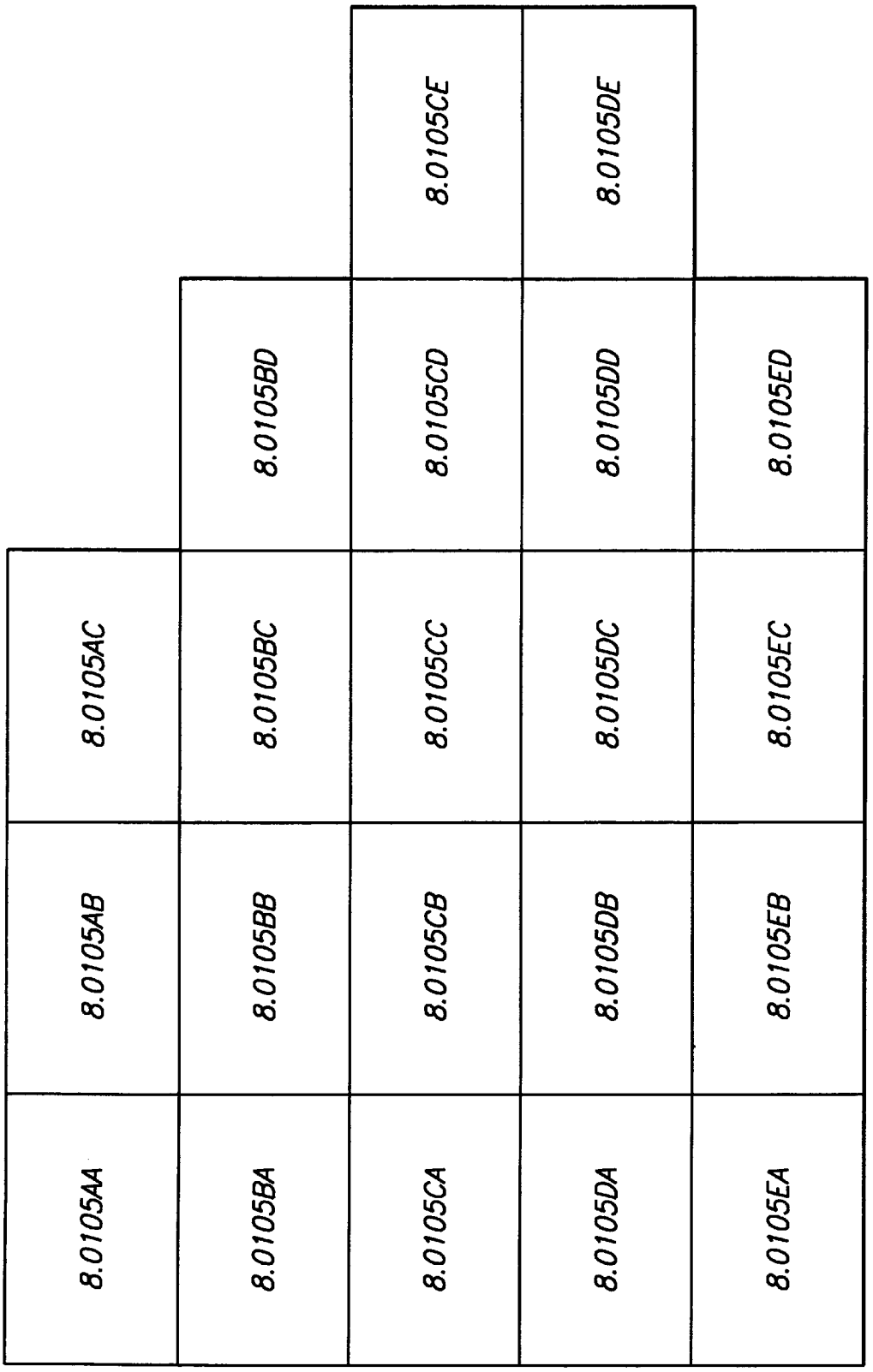

8.0105AA
8.0105AB
8.0105AC
8.0105BA
8.0105BB
8.0105BC
8.0105BD
8.0105CA
8.0105CB
8.0105CC
8.0105CD
8.0105CE
8.0105DA
8.0105DB
8.0105DC
8.0105DD
8.0105DE
8.0105EA
8.0105EB
8.0105EC
8.0105ED

FIG. 8.0105

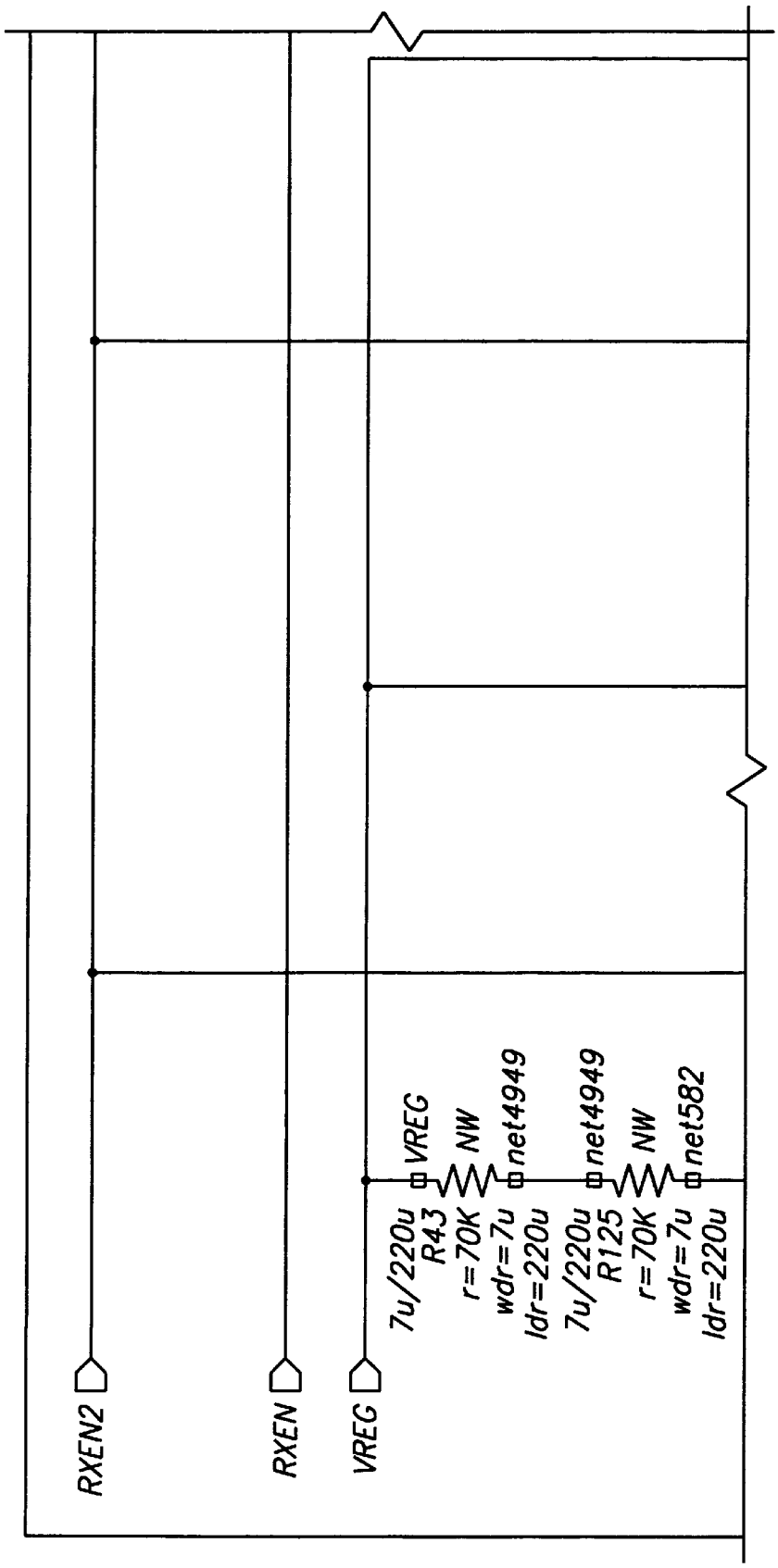

RXEN2
RXEN
VREG
7u/220u
R43
r=70K
wdr=7u
ldr=220u
VREG
NW
net4949
7u/220u
R125
r=70K
wdr=7u
ldr=220u
net4949
NW
net582

FIG 8.01OSAA

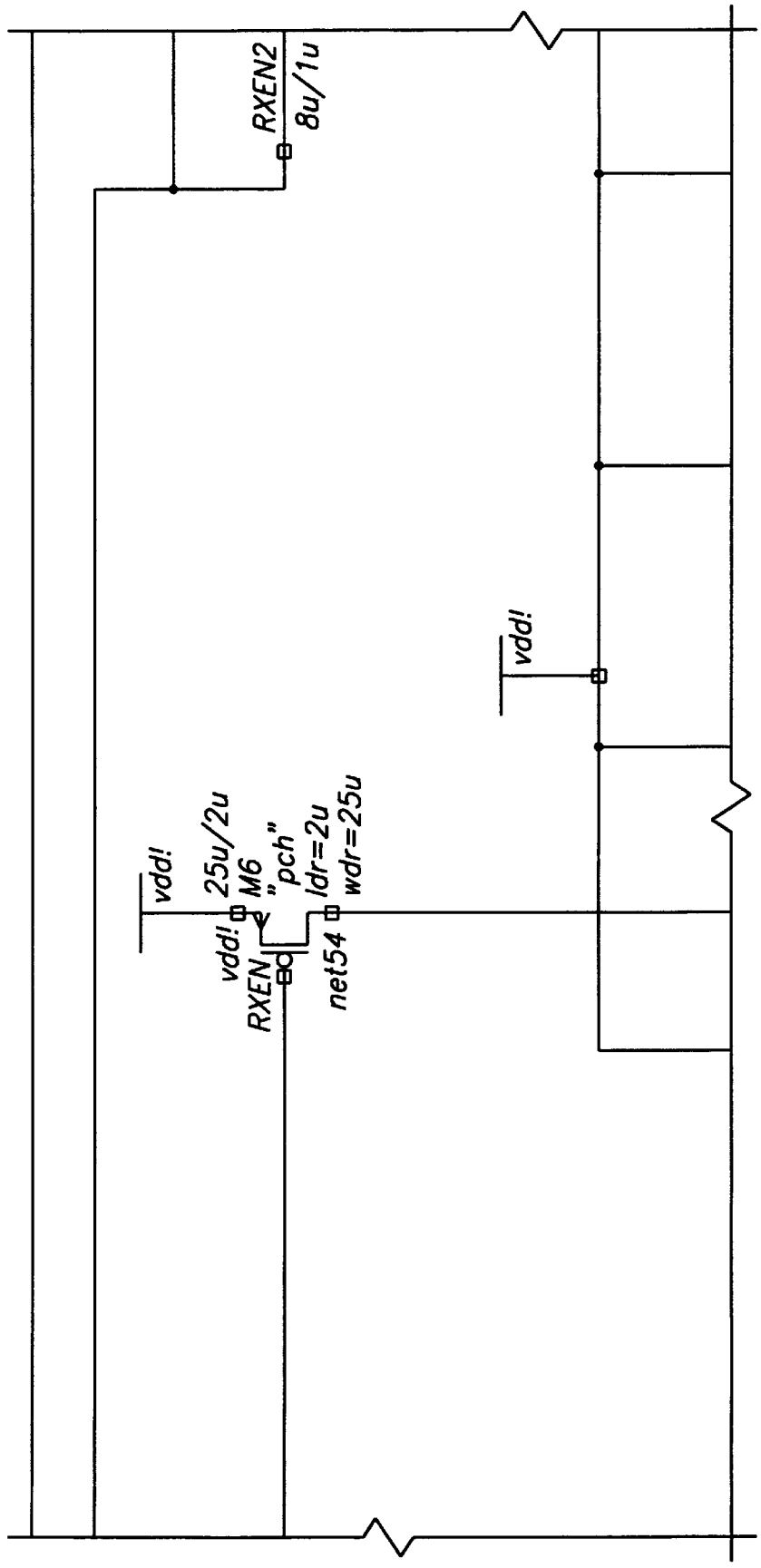
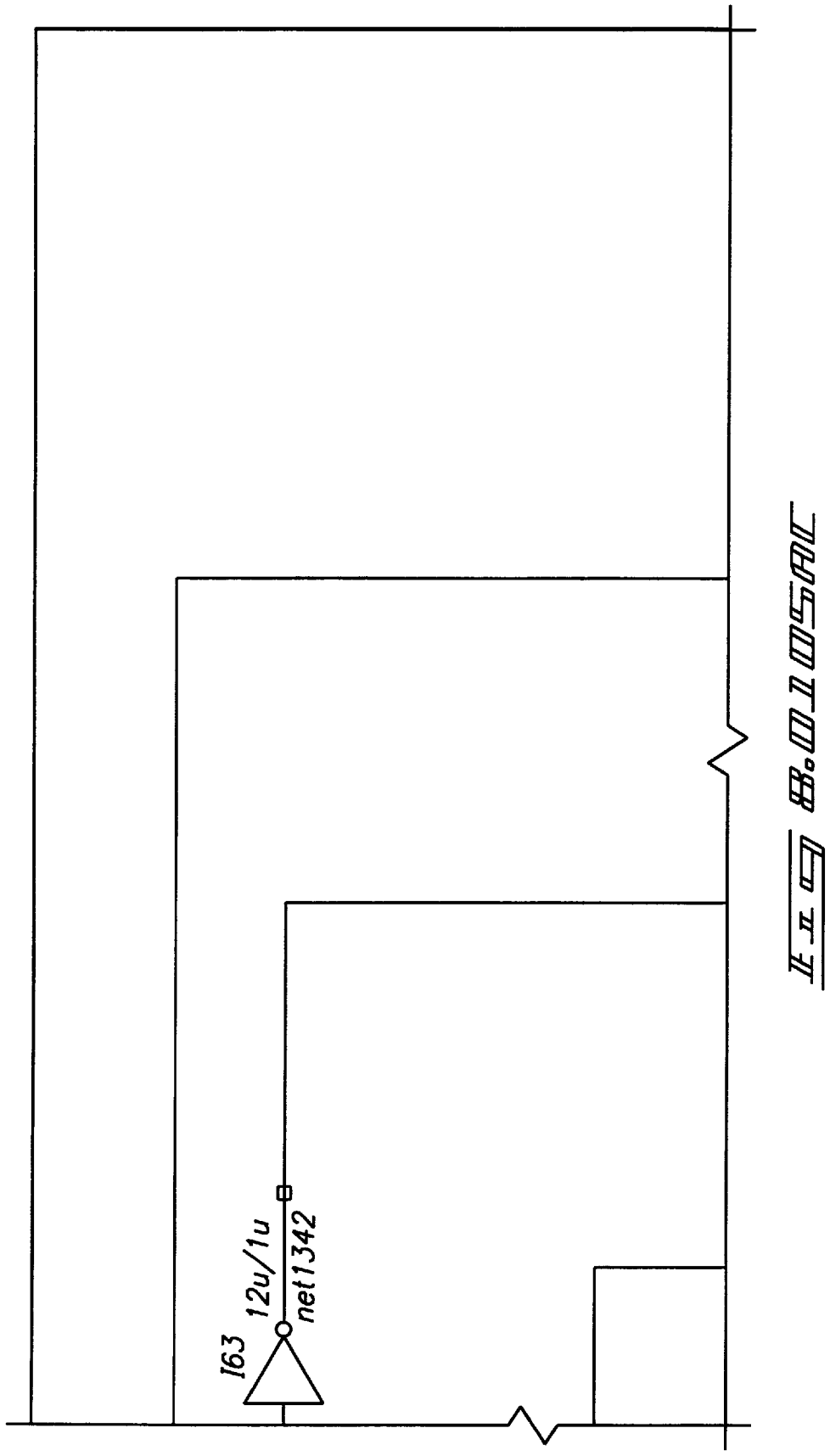
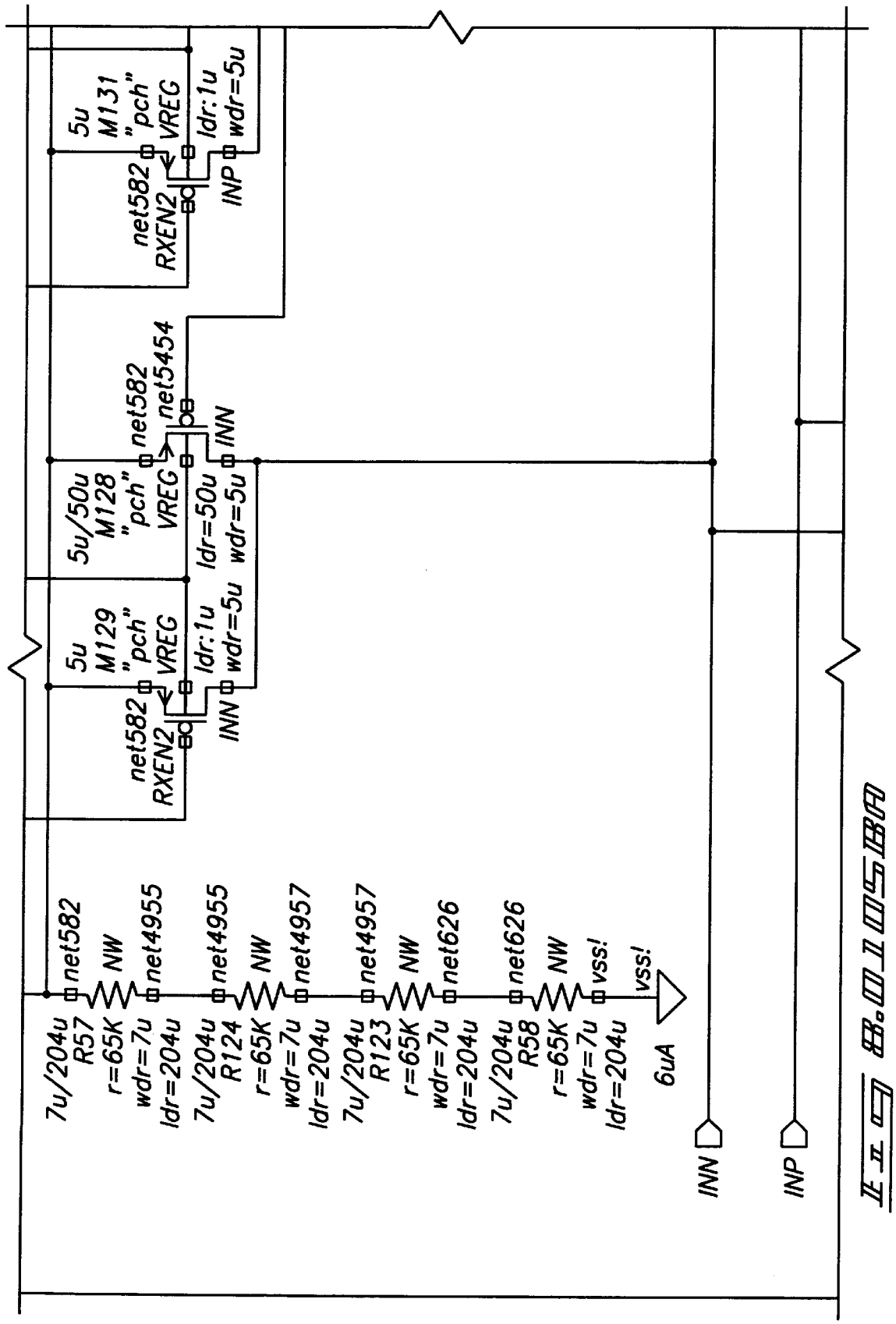


FIG 88.00110SAB


I63
12u/1u
net1342
VSS
8.0110


5u
M131
"pch"
VREG
net582
RXEN2
ldr:1u
wdr=5u
INP
5u/50u
M128
"pch"
VREG
net582
net5454
ldr=50u
wdr=5u
INN
5u
M129
"pch"
VREG
net582
RXEN2
ldr:1u
wdr=5u
INN
7u/204u
R57
r=65K
wdr=7u
ldr=204u
net582
NW
net4955
7u/204u
R124
r=65K
wdr=7u
ldr=204u
net4955
NW
net4957
7u/204u
R123
r=65K
wdr=7u
ldr=204u
net4957
NW
net626
7u/204u
R58
r=65K
wdr=7u
ldr=204u
net626
NW
vss!
vss!
6uA
INN
INP

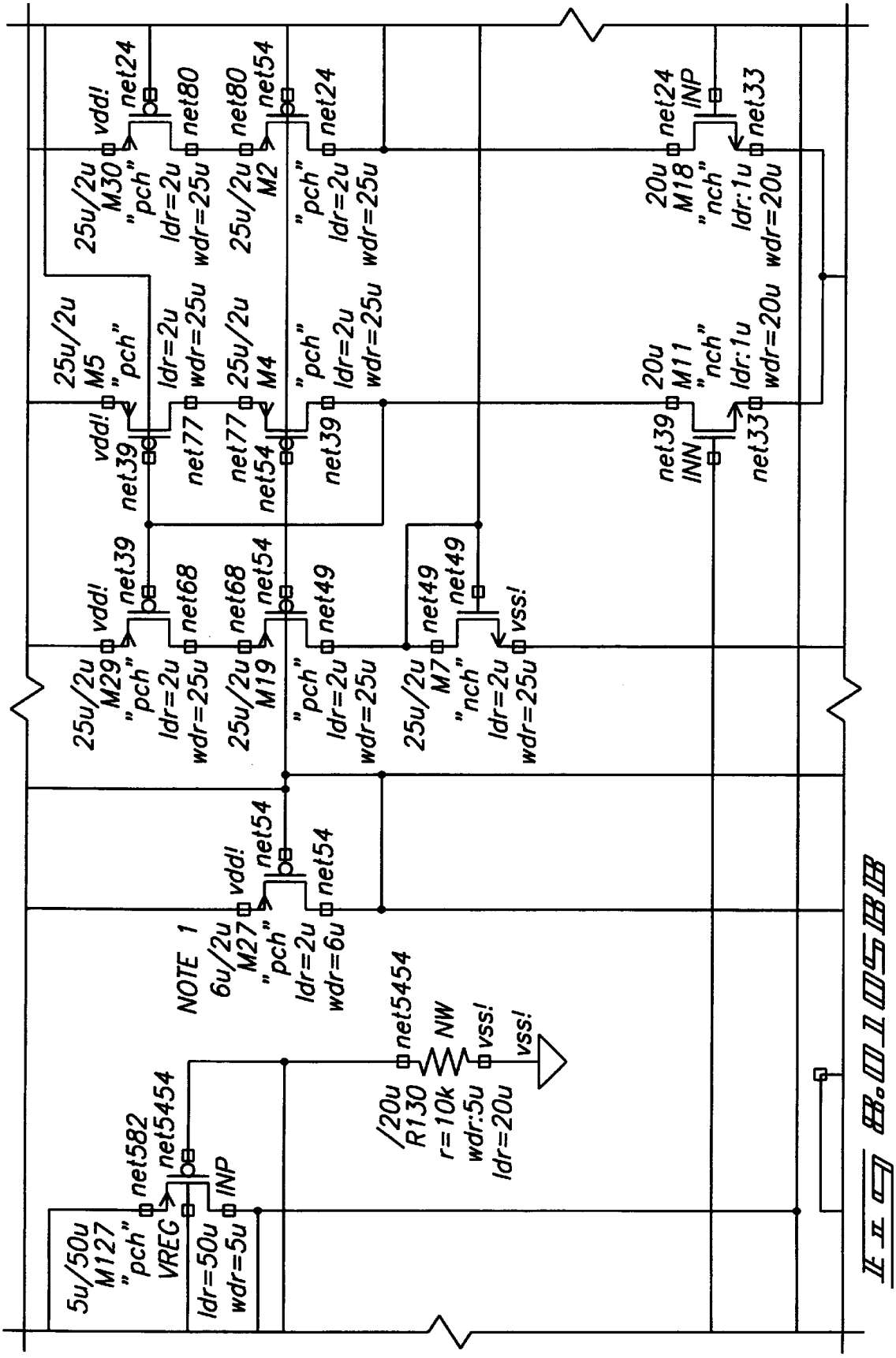

25u/2u M30 "pch" ldr=2u wdr=25u
vdd! net24 net80
25u/2u M2 "pch" ldr=2u wdr=25u
net80 net54 net24
20u M18 "nch" ldr:1u wdr=20u
net24 INP net33
25u/2u M5 "pch" ldr=2u wdr=25u
vdd! net39 net77
25u/2u M4 "pch" ldr=2u wdr=25u
net77 net54 net39
20u M11 "nch" ldr:1u wdr=20u
net39 INN net33
25u/2u M29 "pch" ldr=2u wdr=25u
vdd! net39 net68
25u/2u M19 "pch" ldr=2u wdr=25u
net68 net54 net49
25u/2u M7 "nch" ldr=2u wdr=25u
net49 net49 vss!
6u/2u M27 "pch" ldr=2u wdr=6u
vdd! net54 net54
NOTE 1
/20u R130 r=10k wdr:5u ldr=20u
net5454 NW vss! vss!
5u/50u M127 "pch" VREG ldr=50u wdr=5u
net582 net5454 INP

FIG. 1168

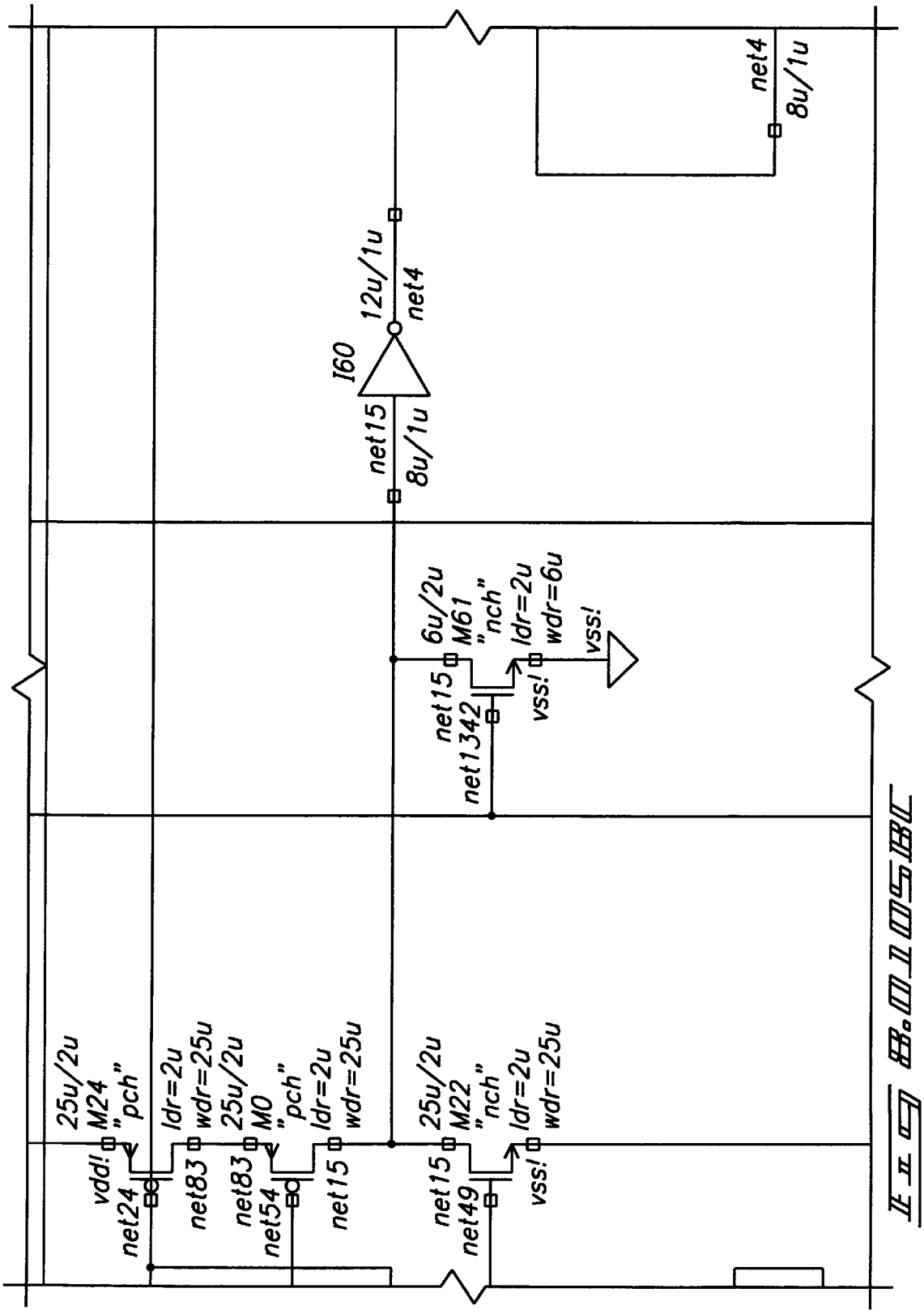

net4
8u/1u
I60
12u/1u
net4
net15
8u/1u
6u/2u
M61
"nch"
ldr=2u
wdr=6u
vss!
net15
net1342
vss!
25u/2u
M24
"pch"
ldr=2u
wdr=25u
25u/2u
M0
"pch"
ldr=2u
wdr=25u
25u/2u
M22
"nch"
ldr=2u
wdr=25u
vdd!
net24
net83
net83
net54
net15
net15
net49
vss!

FIG. 88.0.1.0.0.0

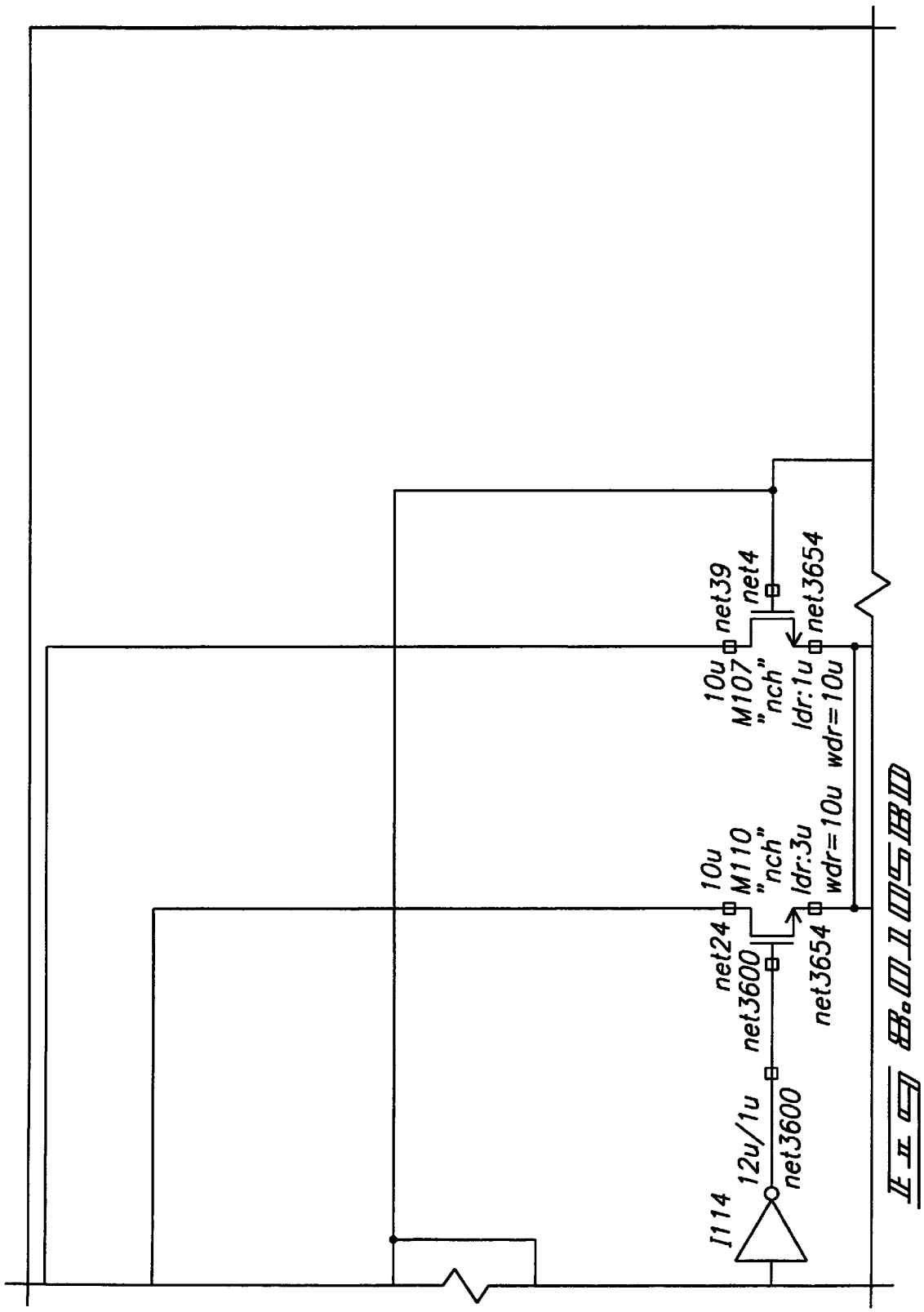
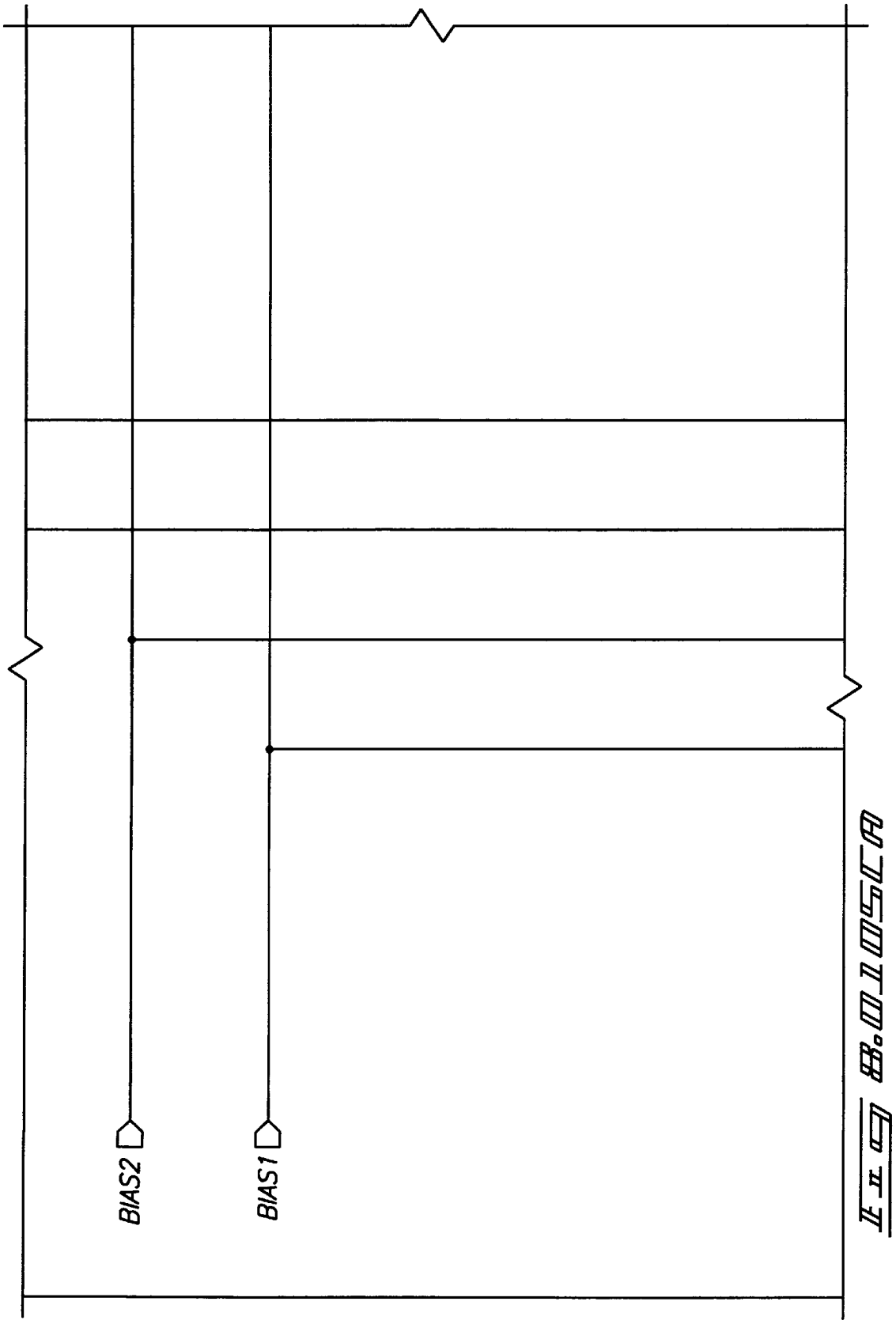

net39
net4
net3654
10u
M107
"nch"
ldr:1u
wdr=10u
10u
M110
"nch"
ldr:3u
wdr=10u
net24
net3600
net3654
12u/1u
net3600
I114

FIG. 1130


BIAS2
BIAS1
VSS
8.0100 FIG

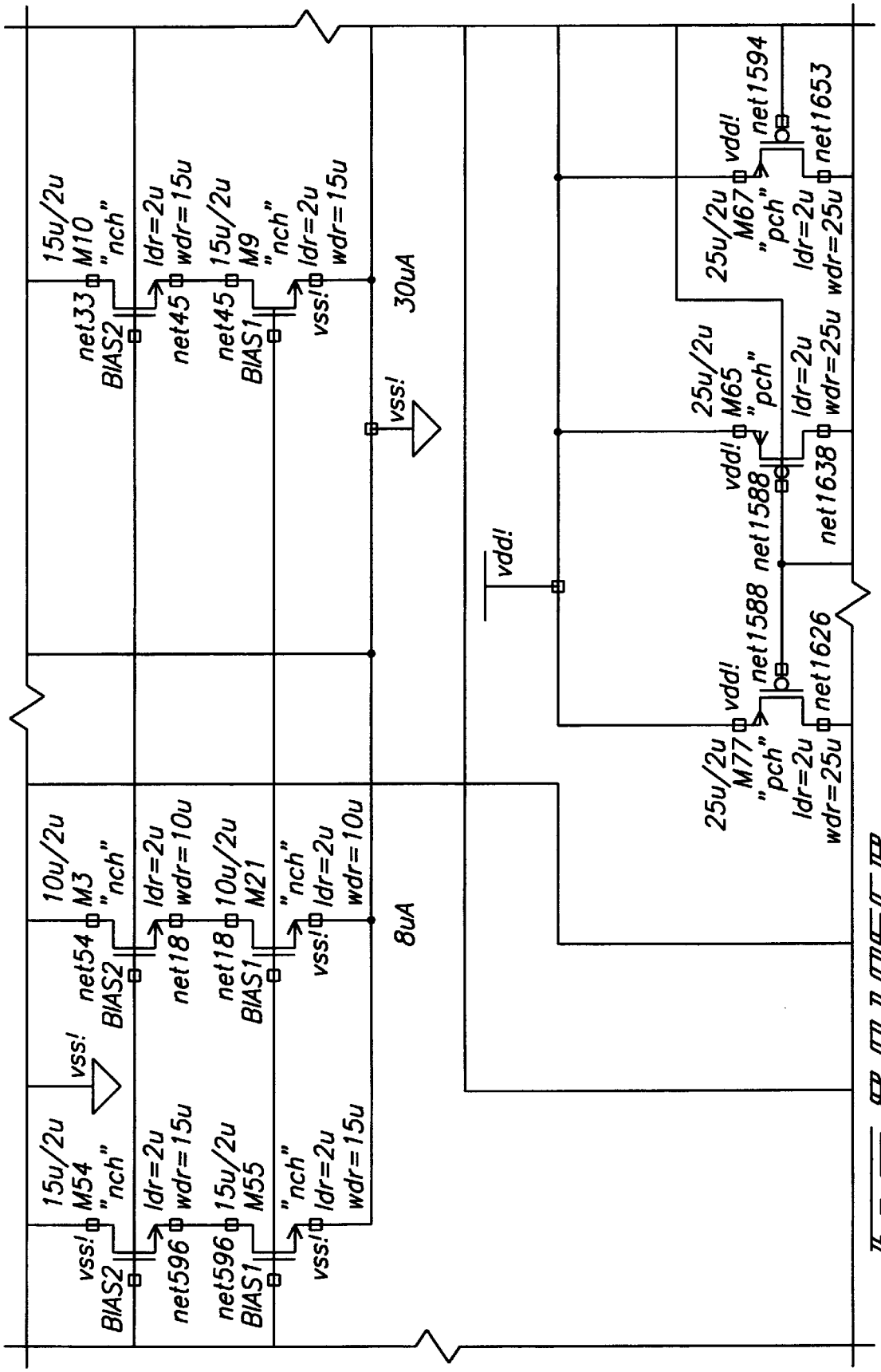

15u/2u
M10
"nch"
ldr=2u
wdr=15u
net33
BIAS2
net45
15u/2u
M9
"nch"
ldr=2u
wdr=15u
net45
BIAS1
vss!
30uA
vss!
vdd!
25u/2u
M67
"pch"
ldr=2u
wdr=25u
vdd!
net1594
net1653
25u/2u
M65
"pch"
ldr=2u
wdr=25u
vdd!
net1588
net1638
25u/2u
M77
"pch"
ldr=2u
wdr=25u
vdd!
net1588
net1626
10u/2u
M3
"nch"
ldr=2u
wdr=10u
net54
BIAS2
net18
10u/2u
M21
"nch"
ldr=2u
wdr=10u
net18
BIAS1
vss!
8uA
15u/2u
M54
"nch"
ldr=2u
wdr=15u
vss!
BIAS2
net596
15u/2u
M55
"nch"
ldr=2u
wdr=15u
net596
BIAS1
vss!

FIG. 1130

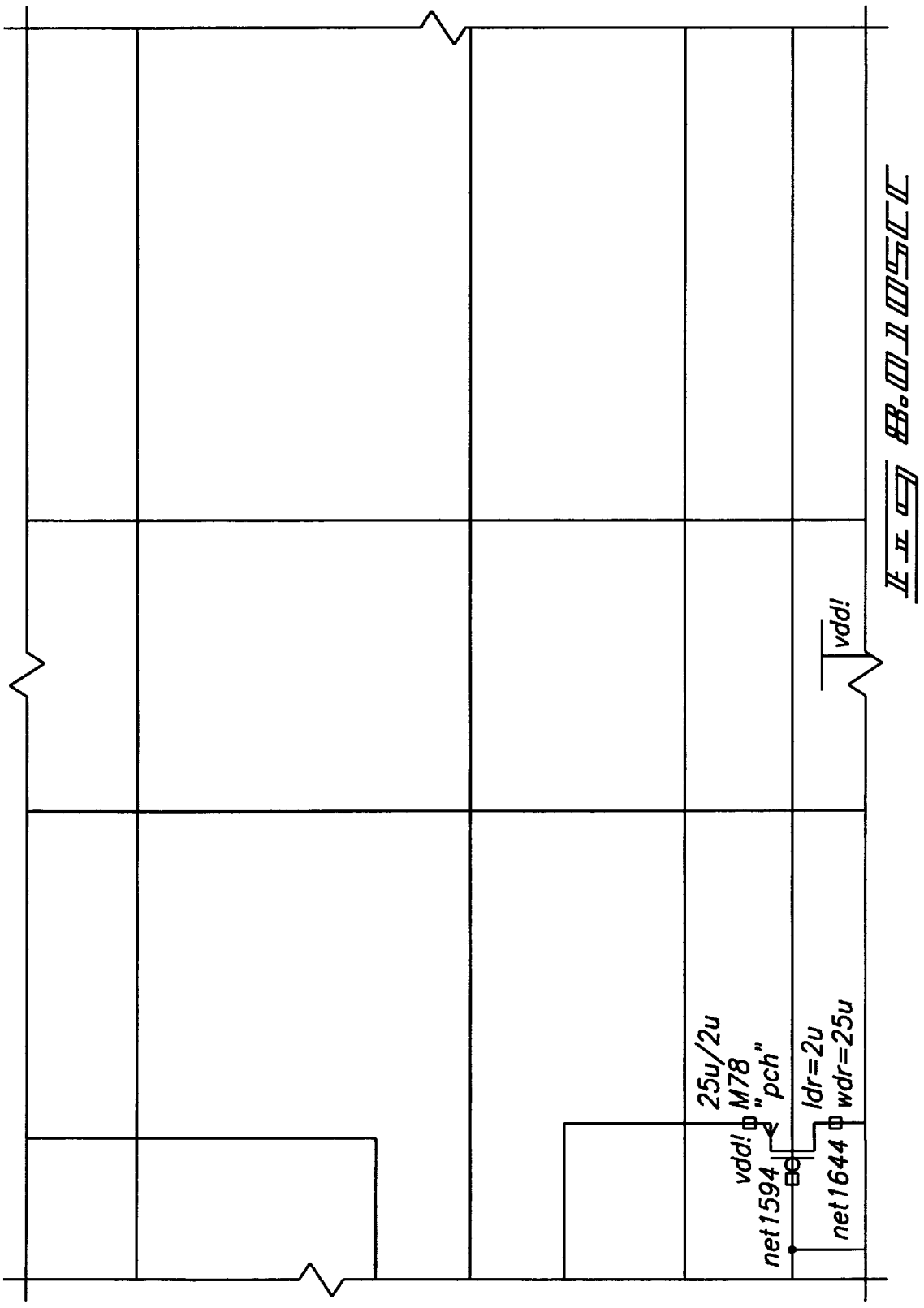


FIG 88.00 (PRIOR ART)
vdd!
25u/2u
M78
"pch"
ldr=2u
wdr=25u
vdd!
net1594
net1644

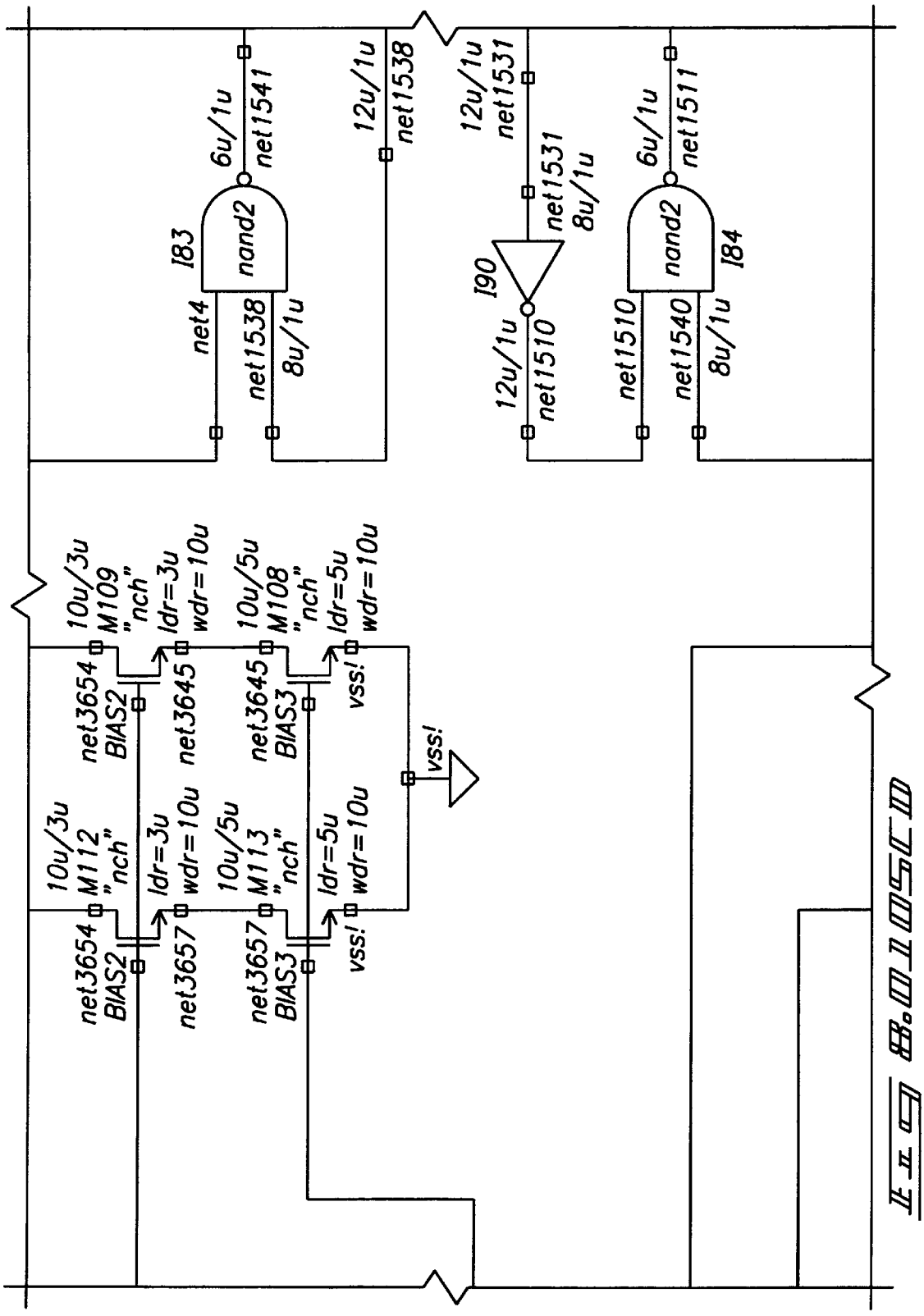
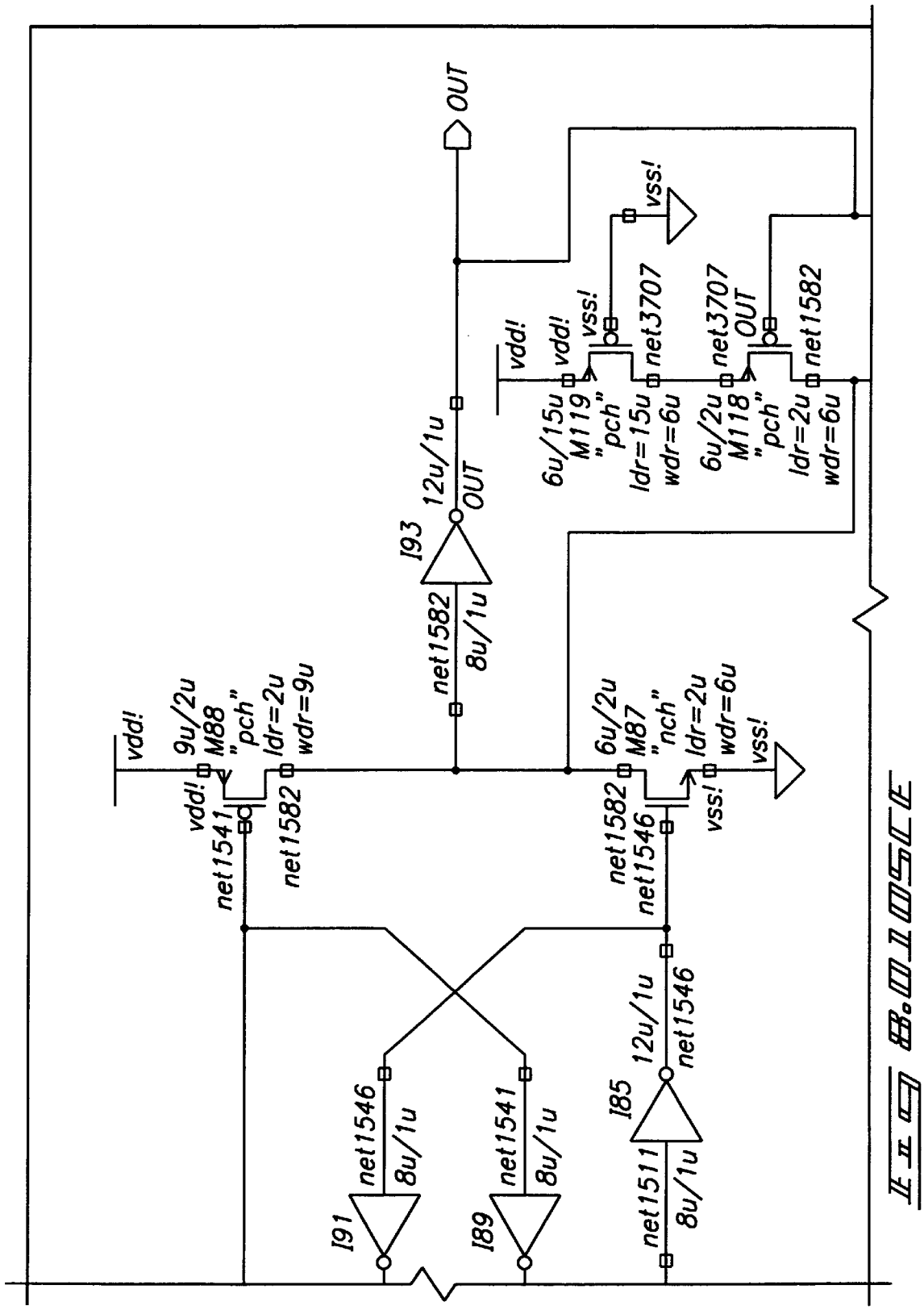

I83
nand2
6u/1u
net1541
net4
net1538
8u/1u
12u/1u
net1538
I90
12u/1u
net1531
net1531
8u/1u
12u/1u
net1510
net1510
I84
nand2
6u/1u
net1511
net1540
8u/1u
net1510
10u/3u
M109
"nch"
ldr=3u
wdr=10u
net3654
BIAS2
net3645
10u/5u
M108
"nch"
ldr=5u
wdr=10u
net3645
BIAS3
vss!
vss!
10u/3u
M112
"nch"
ldr=3u
wdr=10u
net3654
BIAS2
net3657
10u/5u
M113
"nch"
ldr=5u
wdr=10u
net3657
BIAS3
vss!

FIG. 88.0110


OUT
vss!
vdd!
vdd!
vss!
net3707
net3707
OUT
net1582
6u/15u
M119
"pch"
ldr=15u
wdr=6u
6u/2u
M118
"pch"
ldr=2u
wdr=6u
I93
12u/1u
OUT
net1582
8u/1u
vdd!
9u/2u
M88
"pch"
ldr=2u
wdr=9u
6u/2u
M87
"nch"
ldr=2u
wdr=6u
vss!
vdd!
net1541
net1582
net1582
net1546
vss!
net1546
8u/1u
net1541
8u/1u
I91
I89
I85
12u/1u
net1546
net1511
8u/1u

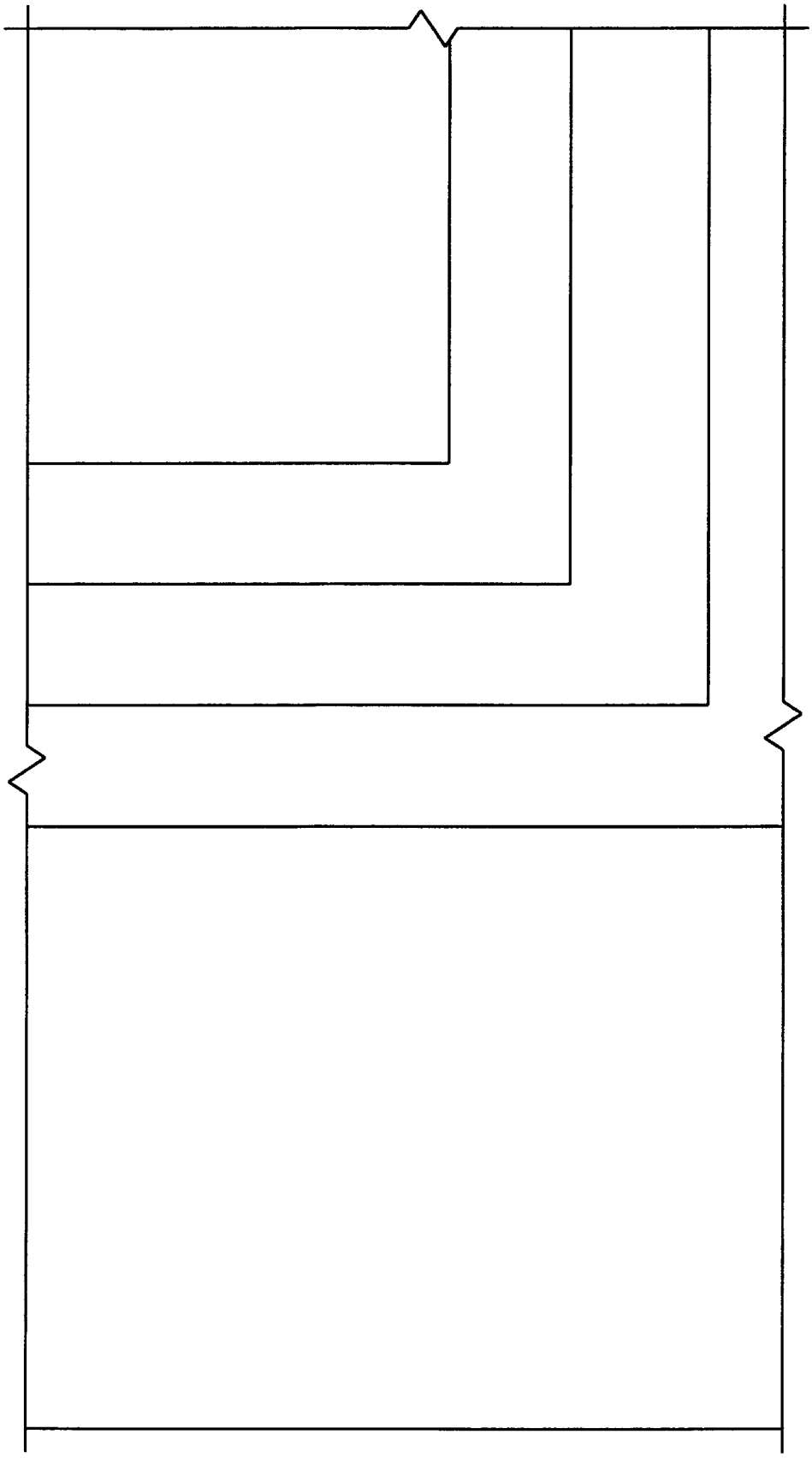


FIG 88.0110SDA

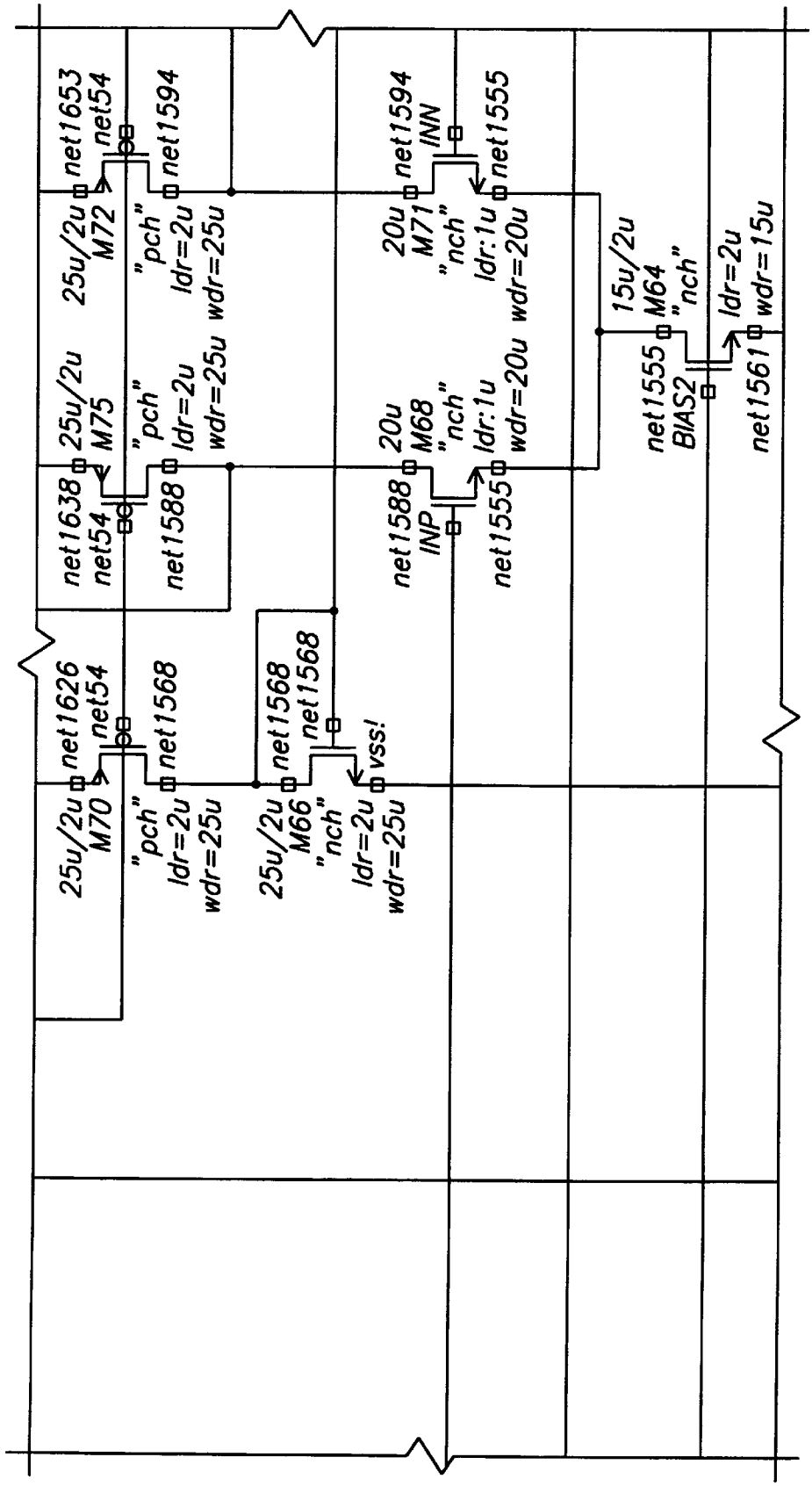


FIG. 88.00150B

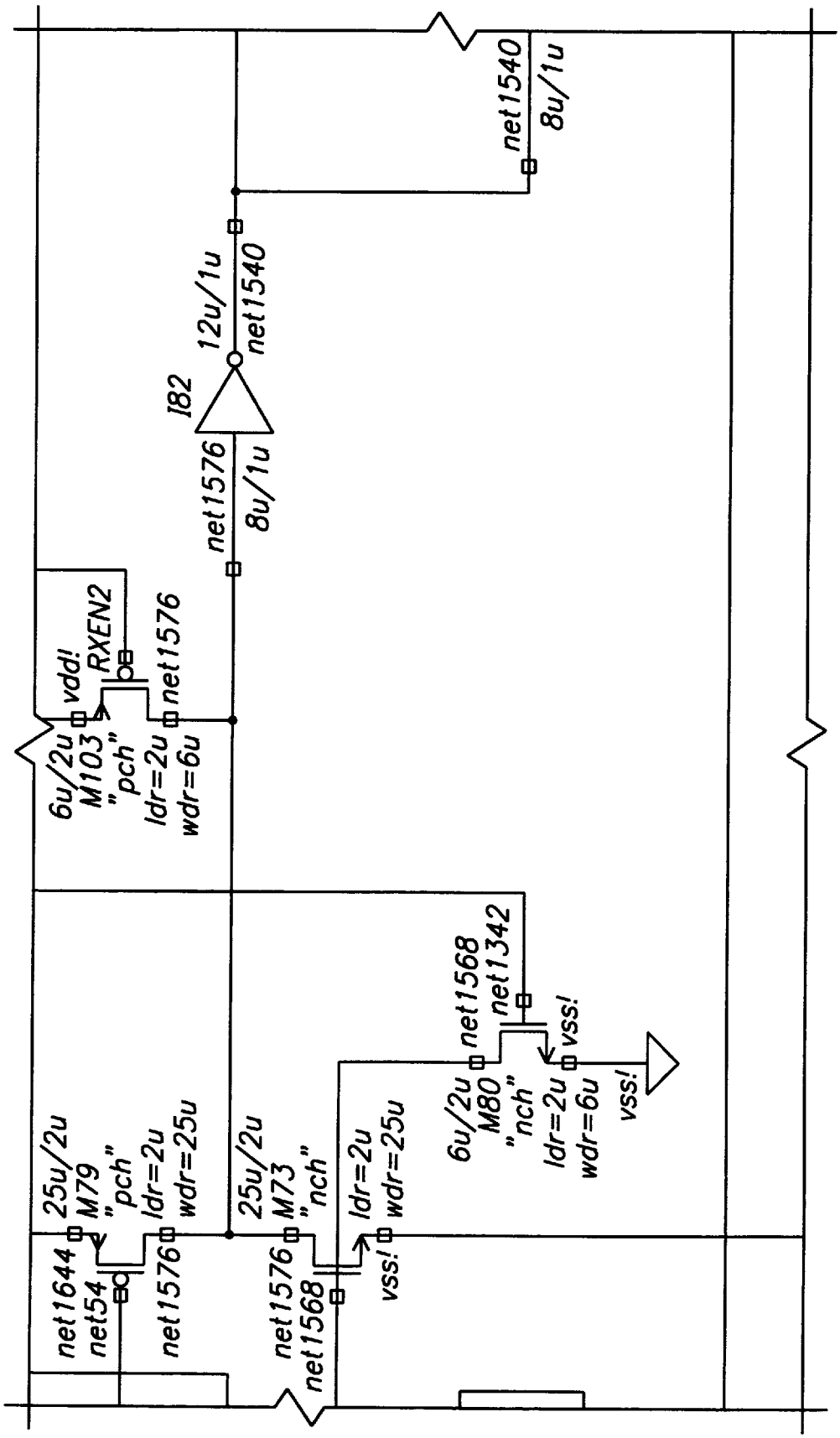

net1540
8u/1u
12u/1u
net1540
I82
net1576
8u/1u
6u/2u
M103
"pch"
ldr=2u
wdr=6u
vdd!
RXEN2
net1576
25u/2u
M79
"pch"
ldr=2u
wdr=25u
net1644
net54
net1576
25u/2u
M73
"nch"
ldr=2u
wdr=25u
net1576
net1568
vss!
6u/2u
M80
"nch"
ldr=2u
wdr=6u
net1568
net1342
vss!
vss!

FIG 8.0115DC

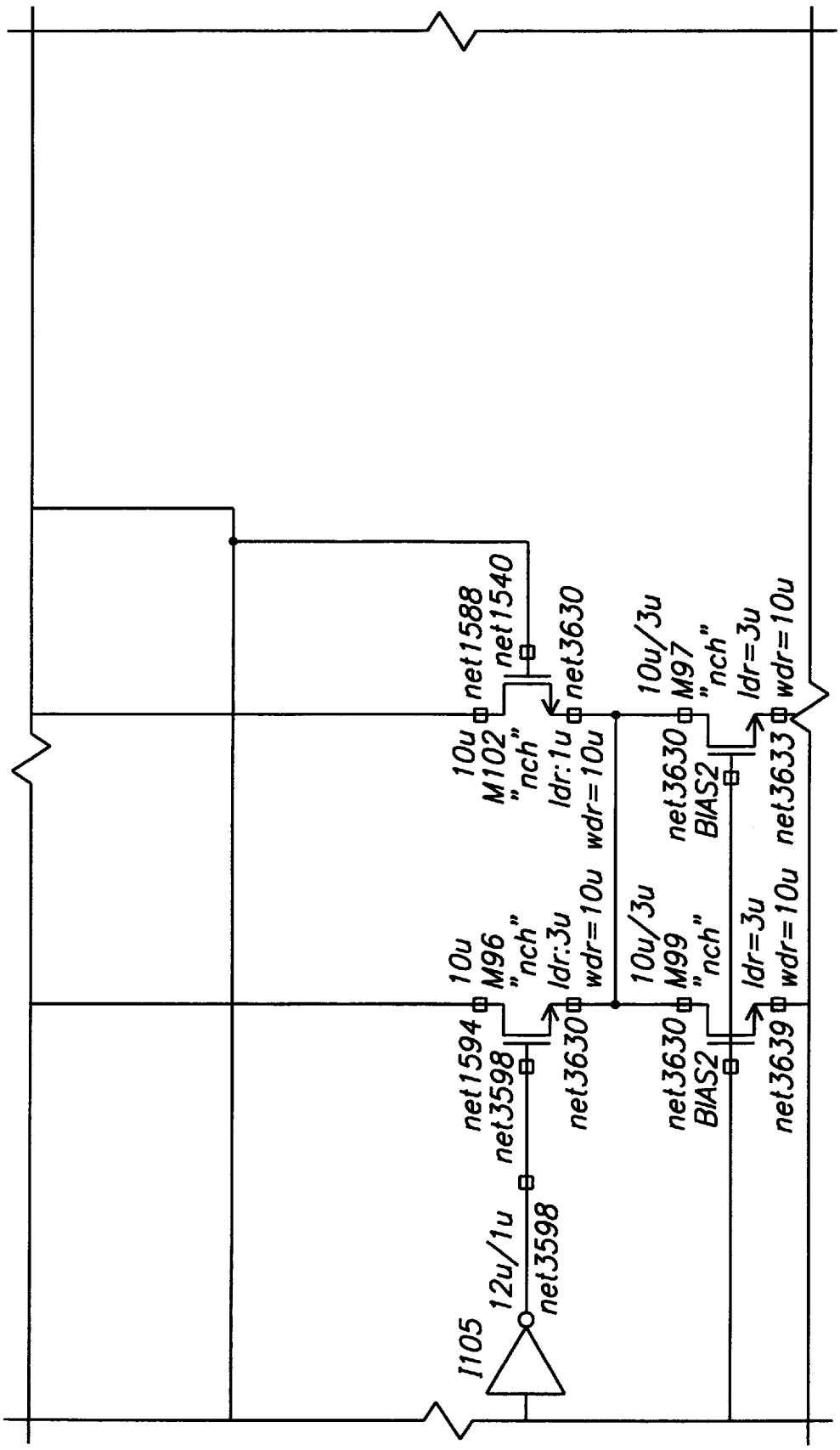

I105
12u/1u
net3598
net1594
net3598
10u
M96
"nch"
ldr:3u
wdr=10u
net3630
10u
M102
"nch"
ldr:1u
wdr=10u
net1588
net1540
net3630
10u/3u
M99
"nch"
ldr=3u
wdr=10u
net3630
BIAS2
net3639
10u/3u
M97
"nch"
ldr=3u
wdr=10u
net3630
BIAS2
net3633

FIG. 88.111

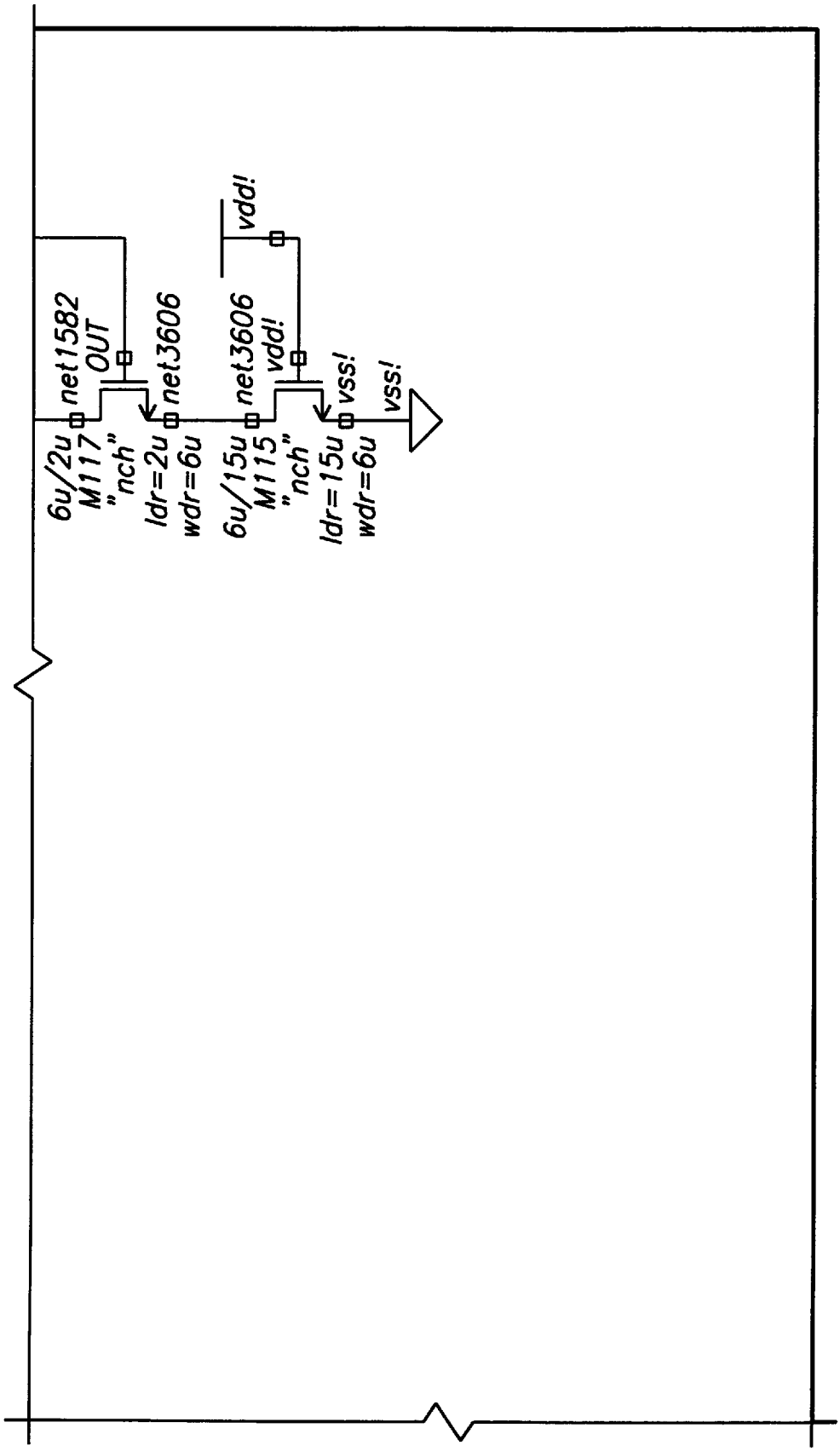


FIG 8.01WSIDE

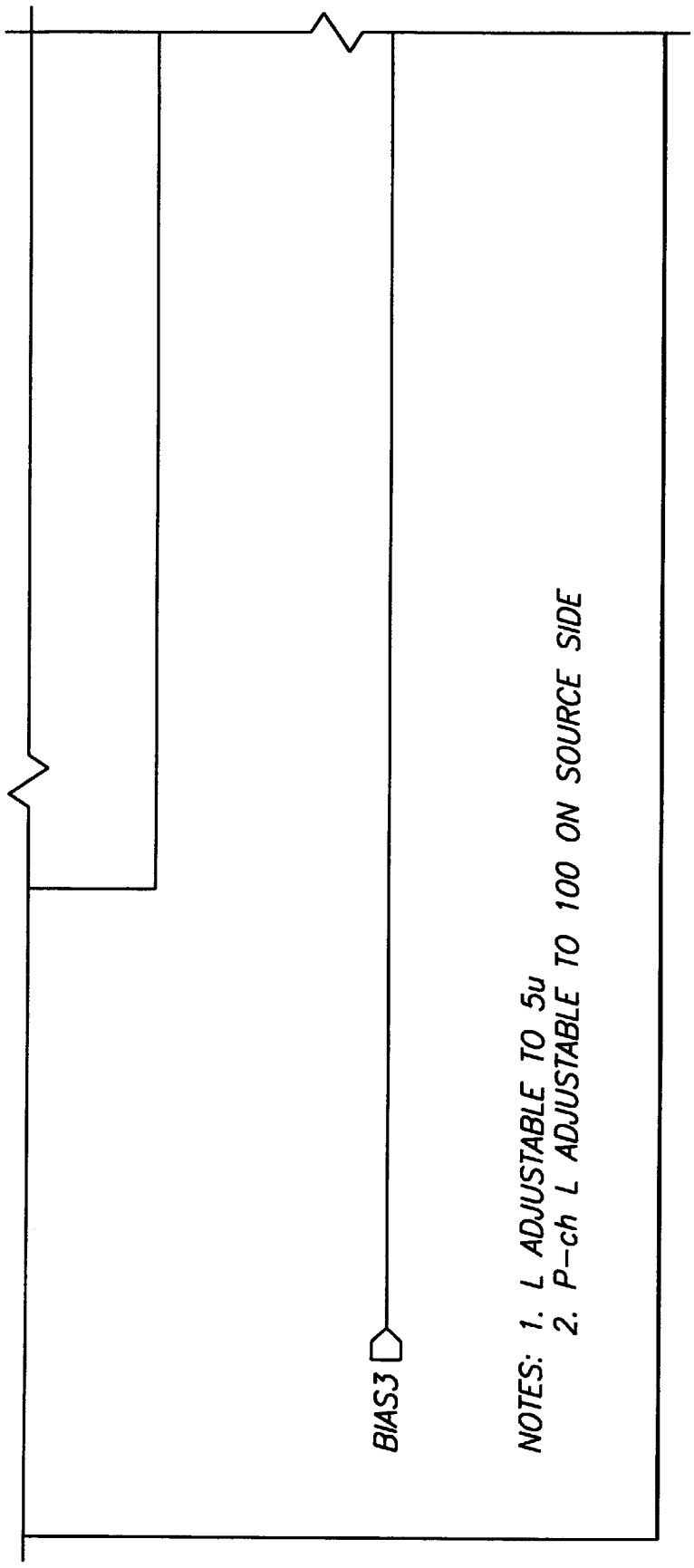


FIG 88.0110SEA

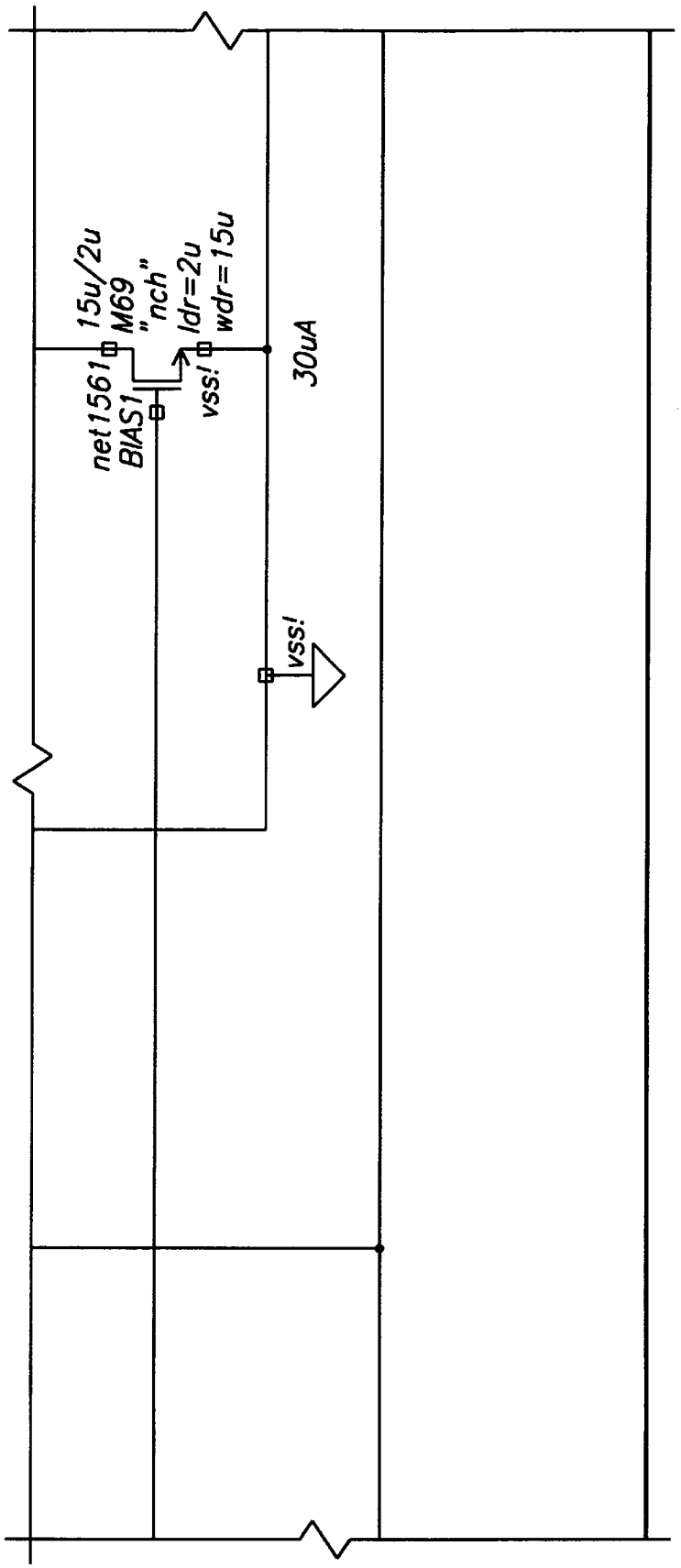


FIG 88.0110SE1B

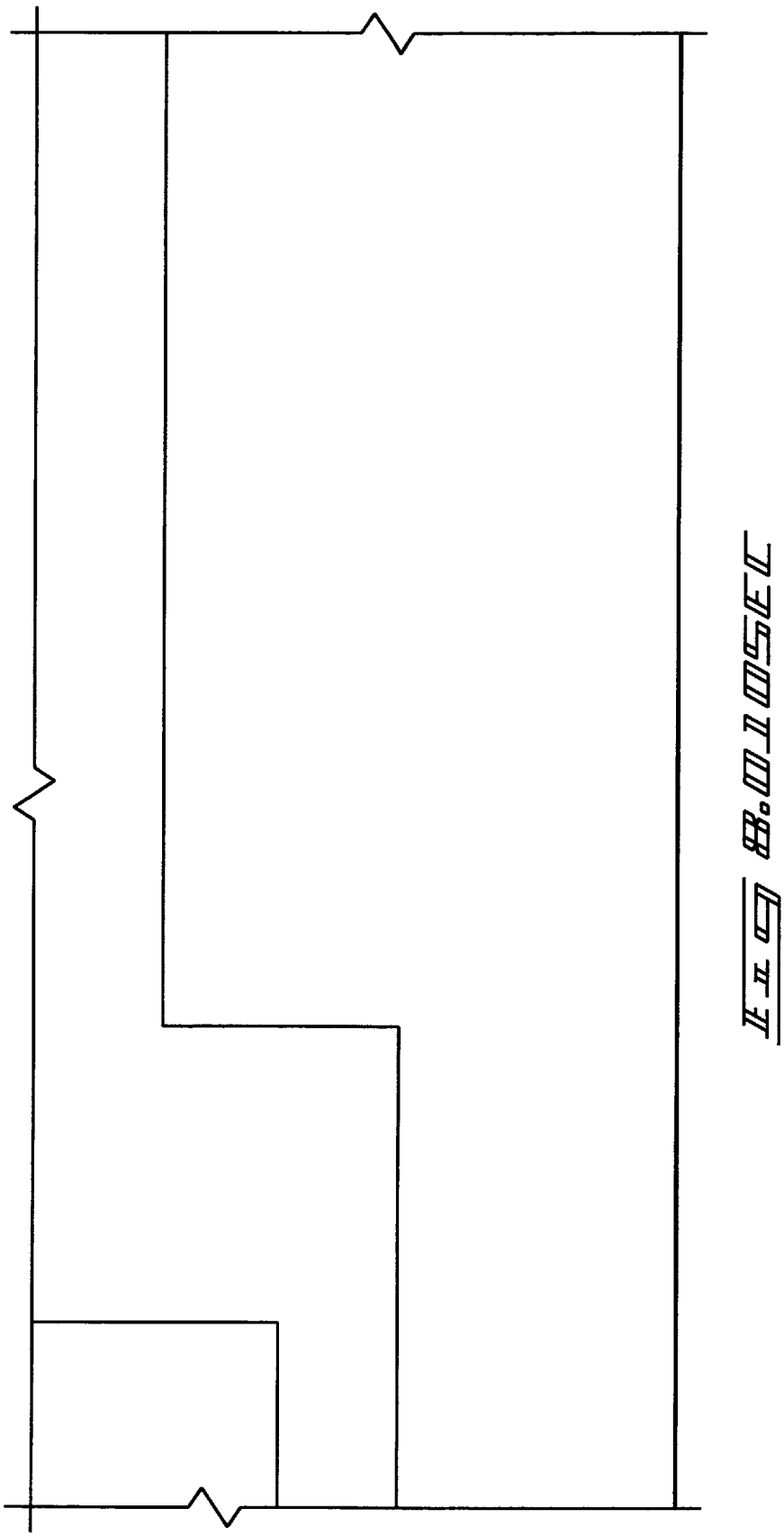


FIG 88.01056

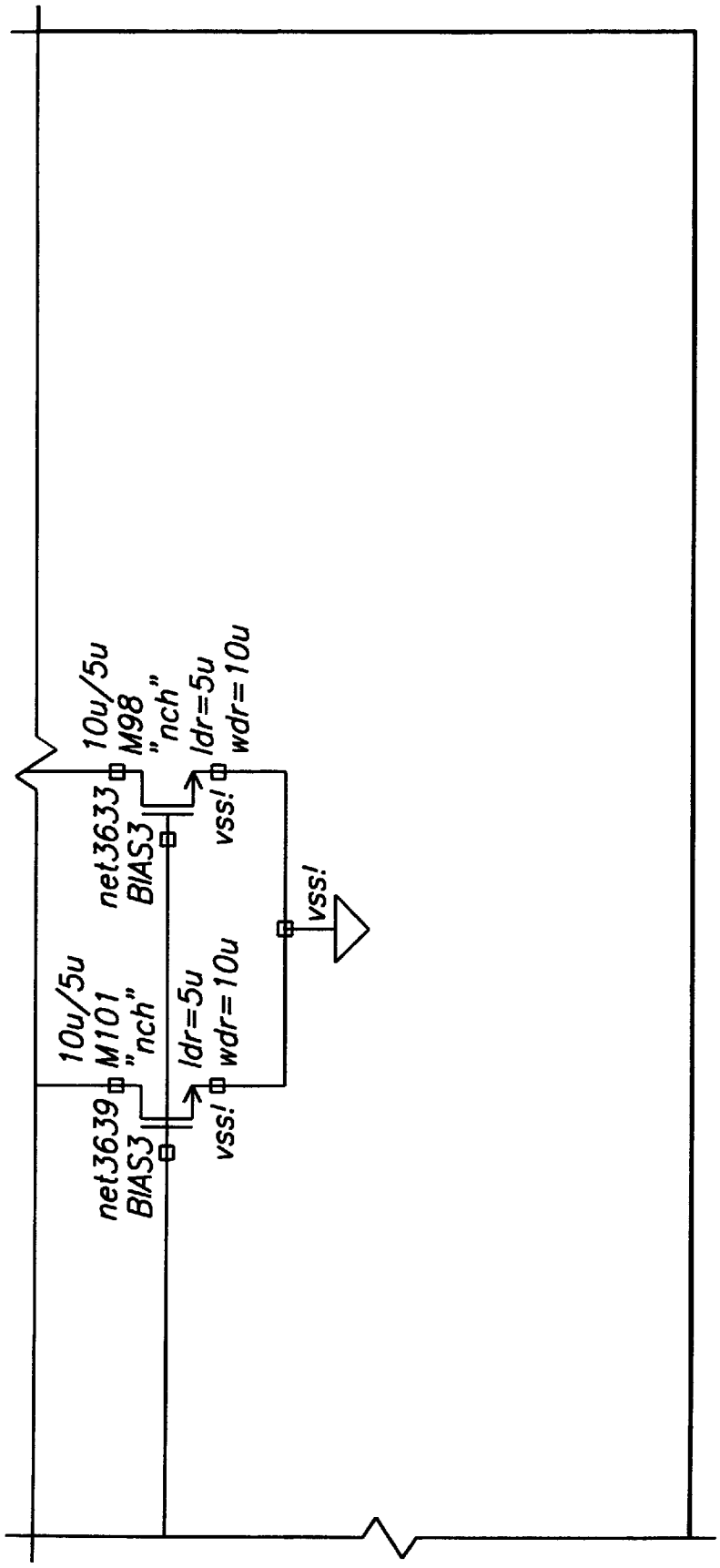


FIG. 88.0115EM

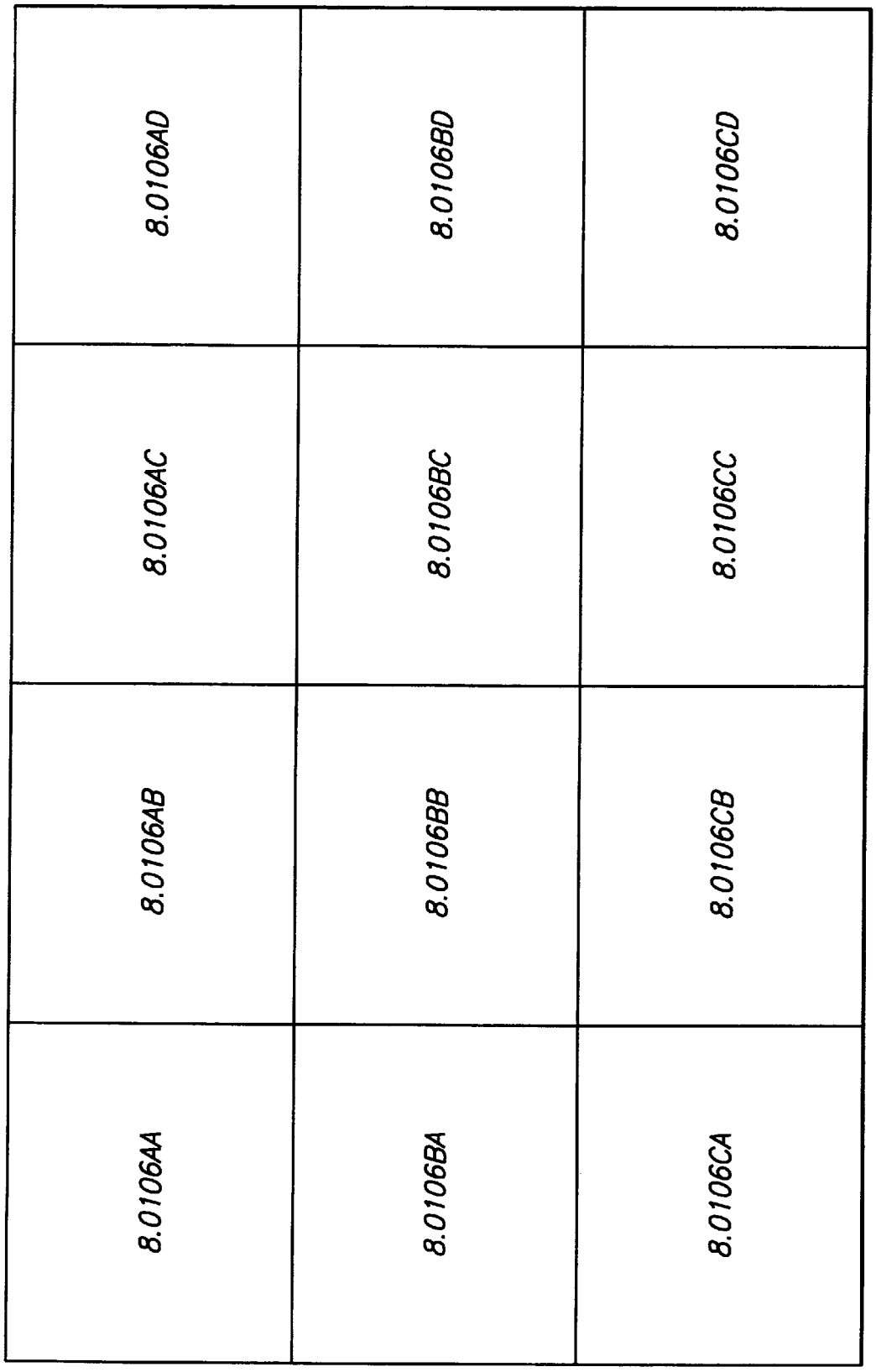

8.0106AD
8.0106BD
8.0106CD
8.0106AC
8.0106BC
8.0106CC
8.0106AB
8.0106BB
8.0106CB
8.0106AA
8.0106BA
8.0106CA

FIG. 8.0106

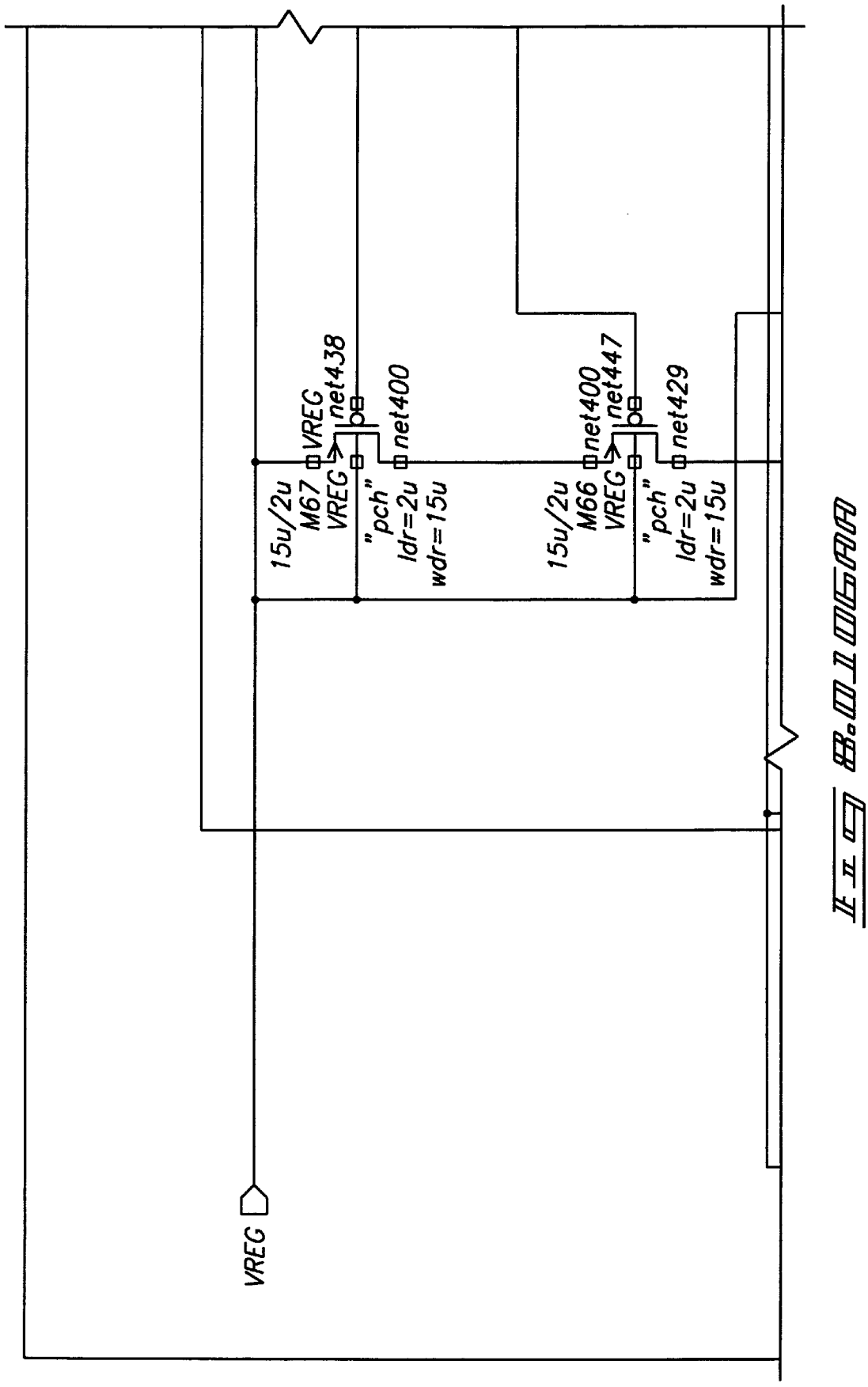

VREG
net438
net400
15u/2u
M67
VREG
"pch"
ldr=2u
wdr=15u
net400
net447
net429
15u/2u
M66
VREG
"pch"
ldr=2u
wdr=15u
VREG

FIG 8.01GAA

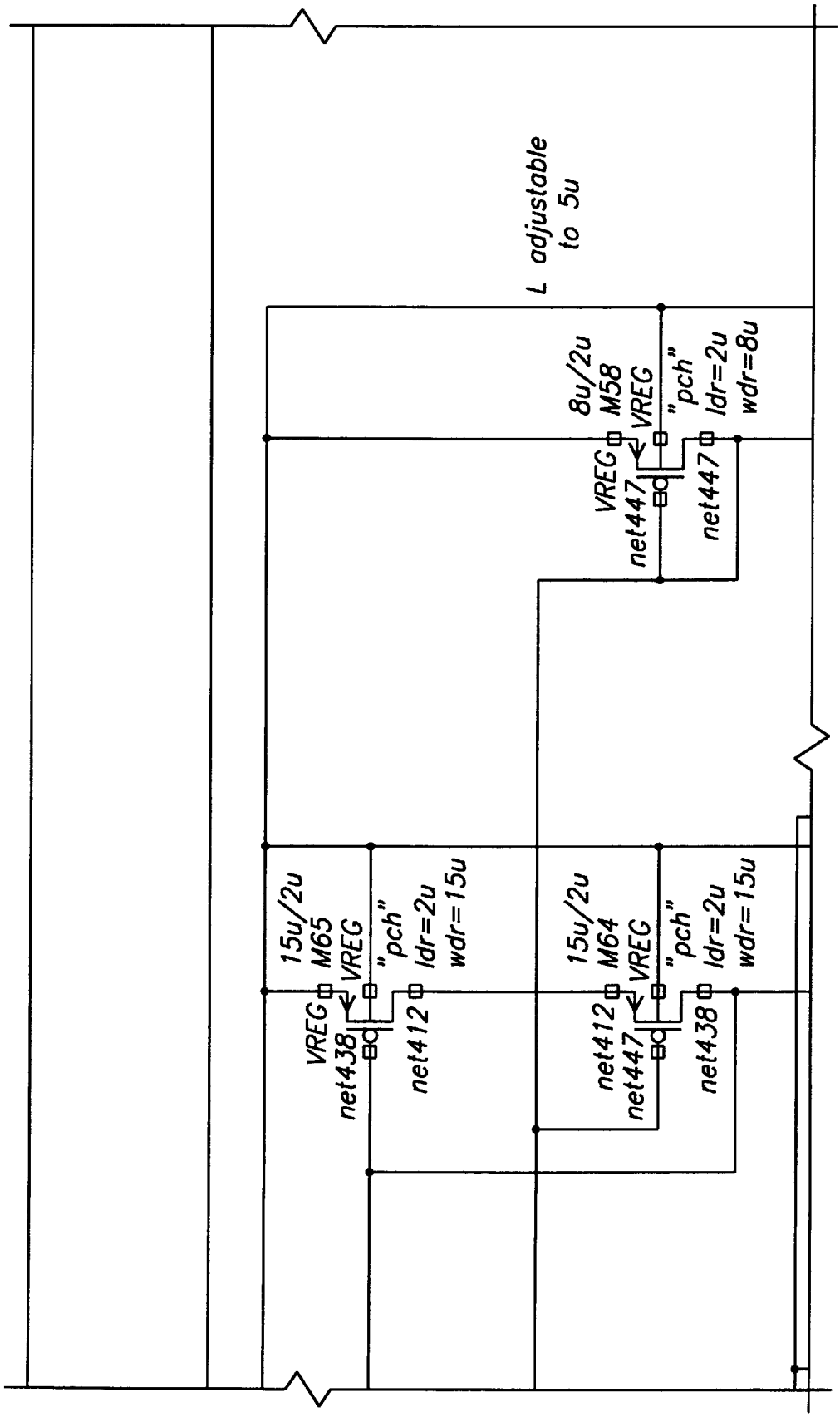


FIG. 88.00 (PRIOR ART)

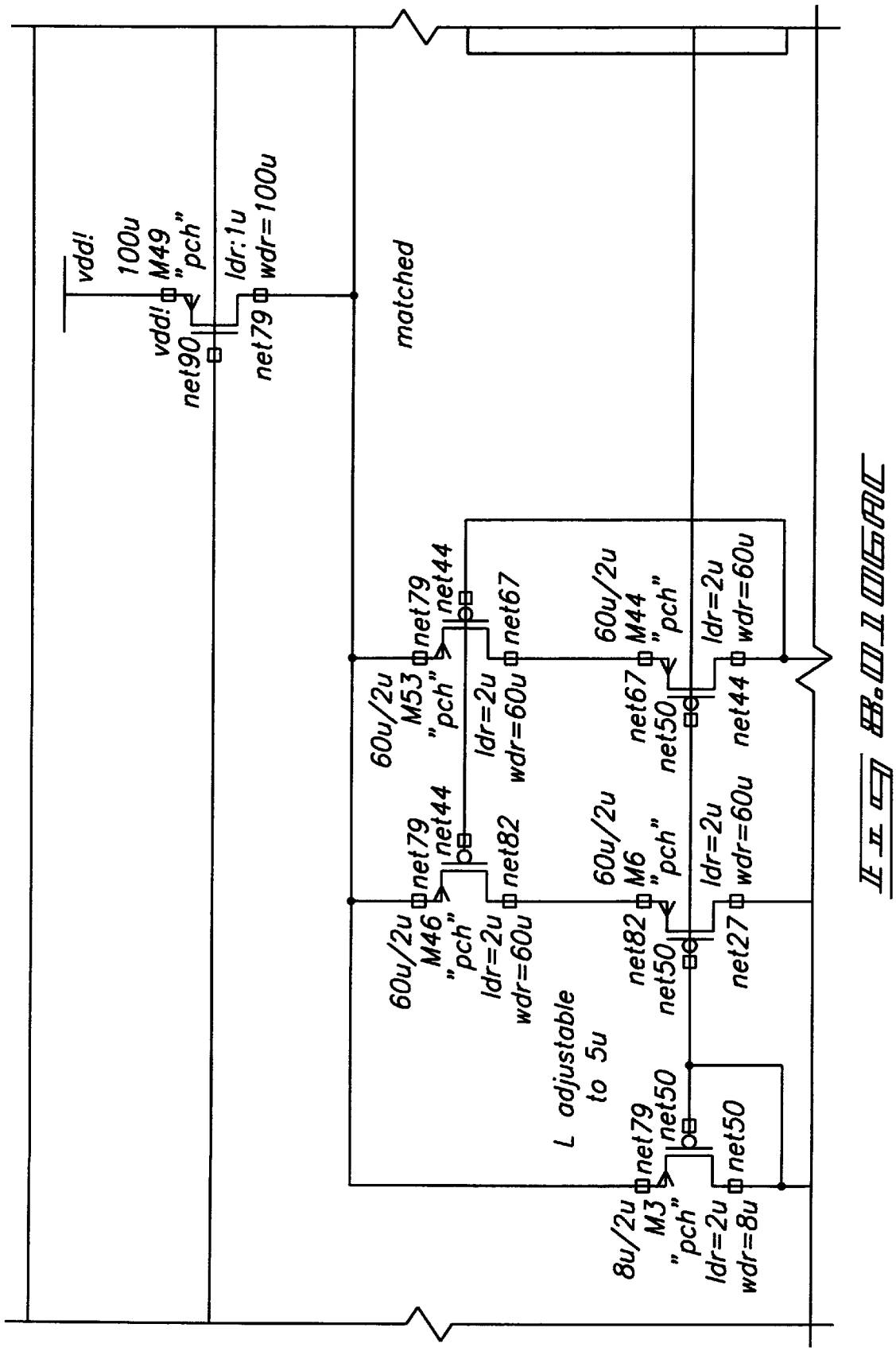


FIG 88.00 II (PRIOR ART)

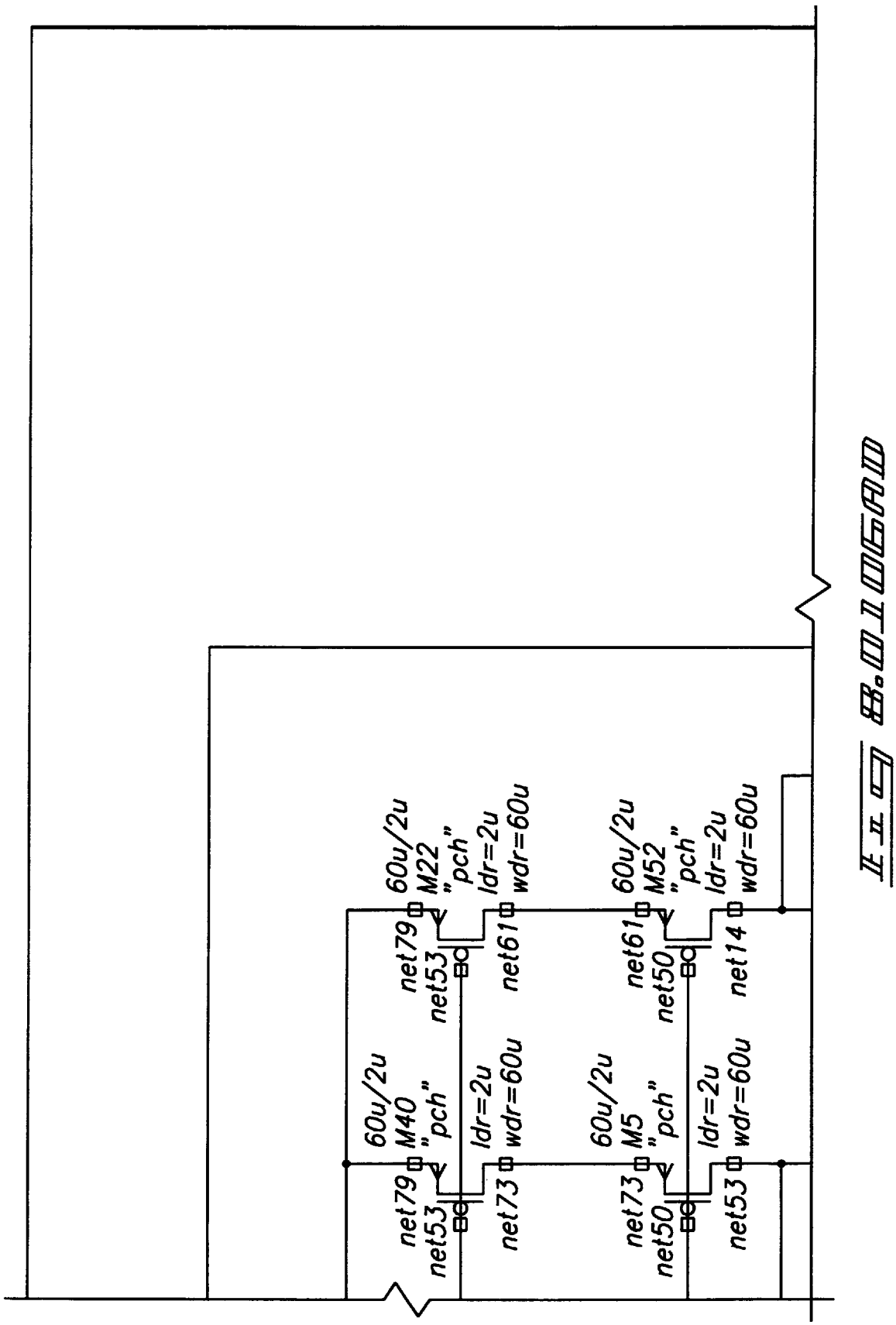


FIG 88.01USAD

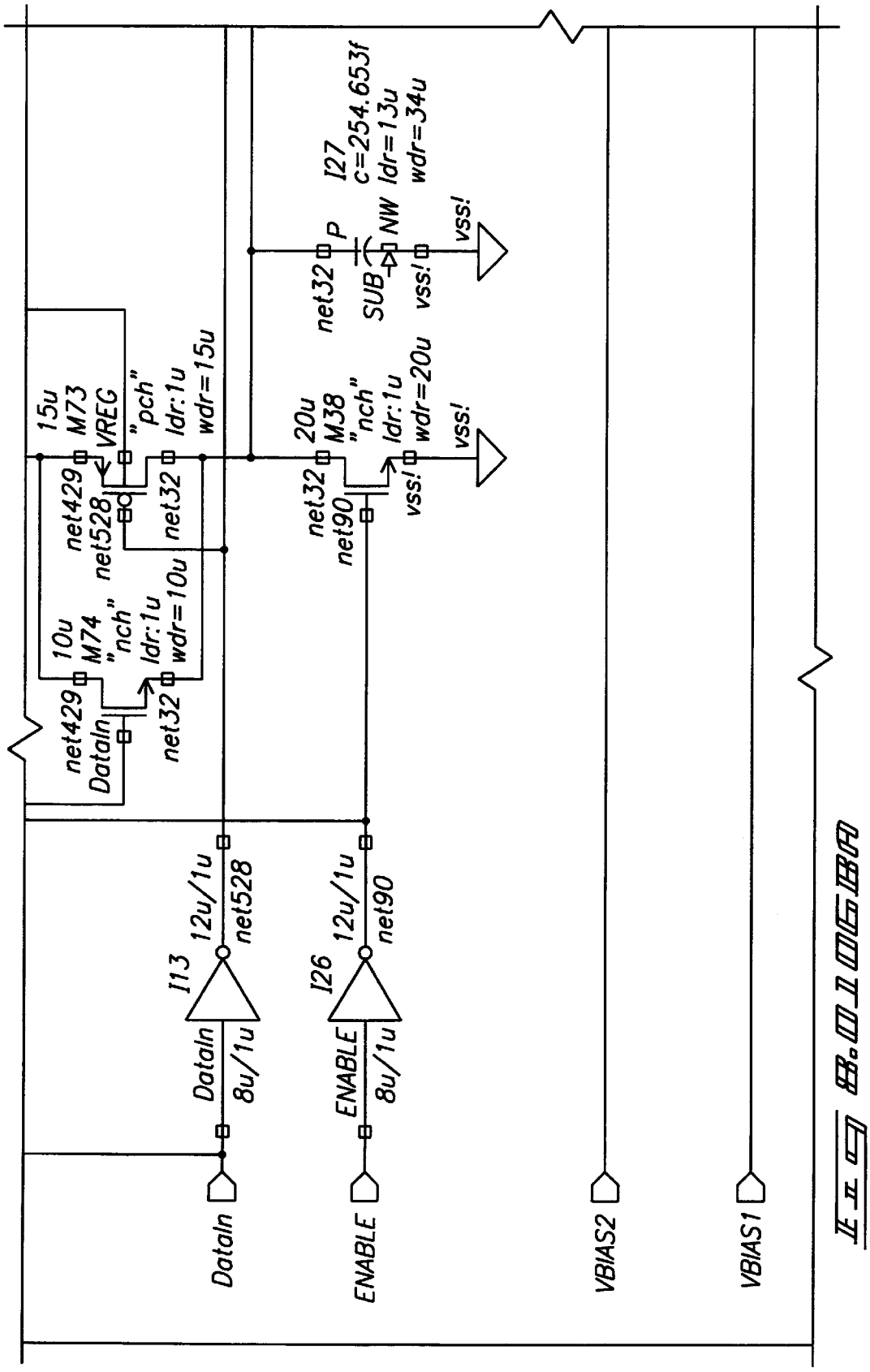

I27
c=254.653f
ldr=1.3u
wdr=34u
net32
P
SUB
NW
vss!
vss!
15u
M73
VREG
"pch"
ldr:1u
wdr=15u
net429
net528
net32
20u
M38
"nch"
ldr:1u
wdr=20u
net32
net90
vss!
vss!
10u
M74
"nch"
ldr:1u
wdr=10u
net429
DataIn
net32
I13
12u/1u
net528
DataIn
8u/1u
I26
12u/1u
net90
ENABLE
8u/1u
DataIn
ENABLE
VBIAS2
VBIAS1

FIG. 88.0100

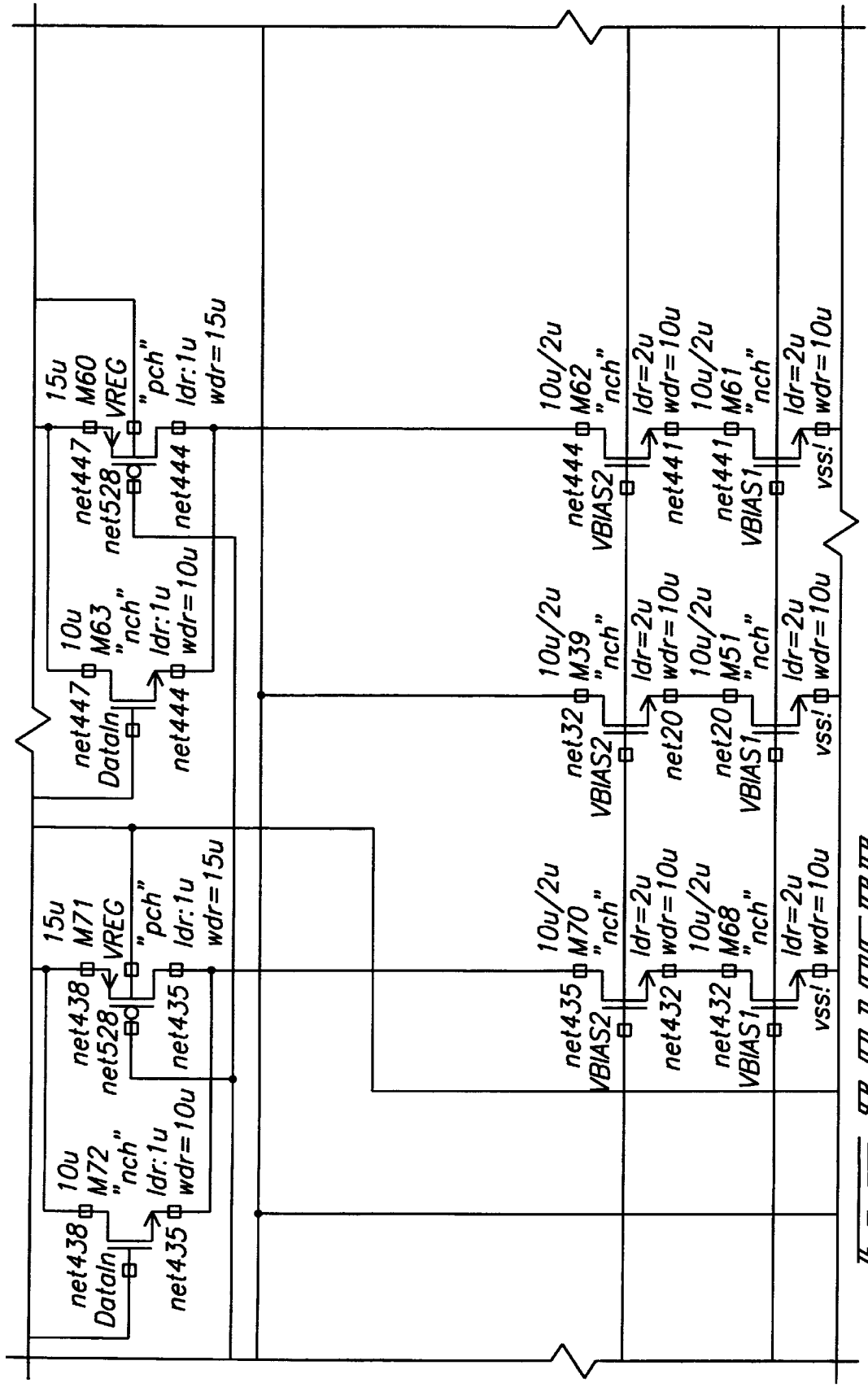

15u M60 VREG "pch" ldr:1u wdr=15u
net447 net528 net444
10u M63 "nch" ldr:1u wdr=10u
net447 DataIn net444
15u M71 VREG "pch" ldr:1u wdr=15u
net438 net528 net435
10u M72 "nch" ldr:1u wdr=10u
net438 DataIn net435
10u/2u M62 "nch" ldr=2u wdr=10u
net444 VBIAS2 net441
10u/2u M61 "nch" ldr=2u wdr=10u
net441 VBIAS1 vss!
10u/2u M39 "nch" ldr=2u wdr=10u
net32 VBIAS2 net20
10u/2u M51 "nch" ldr=2u wdr=10u
net20 VBIAS1 vss!
10u/2u M70 "nch" ldr=2u wdr=10u
net435 VBIAS2 net432
10u/2u M68 "nch" ldr=2u wdr=10u
net432 VBIAS1 vss!

FIG. 1188

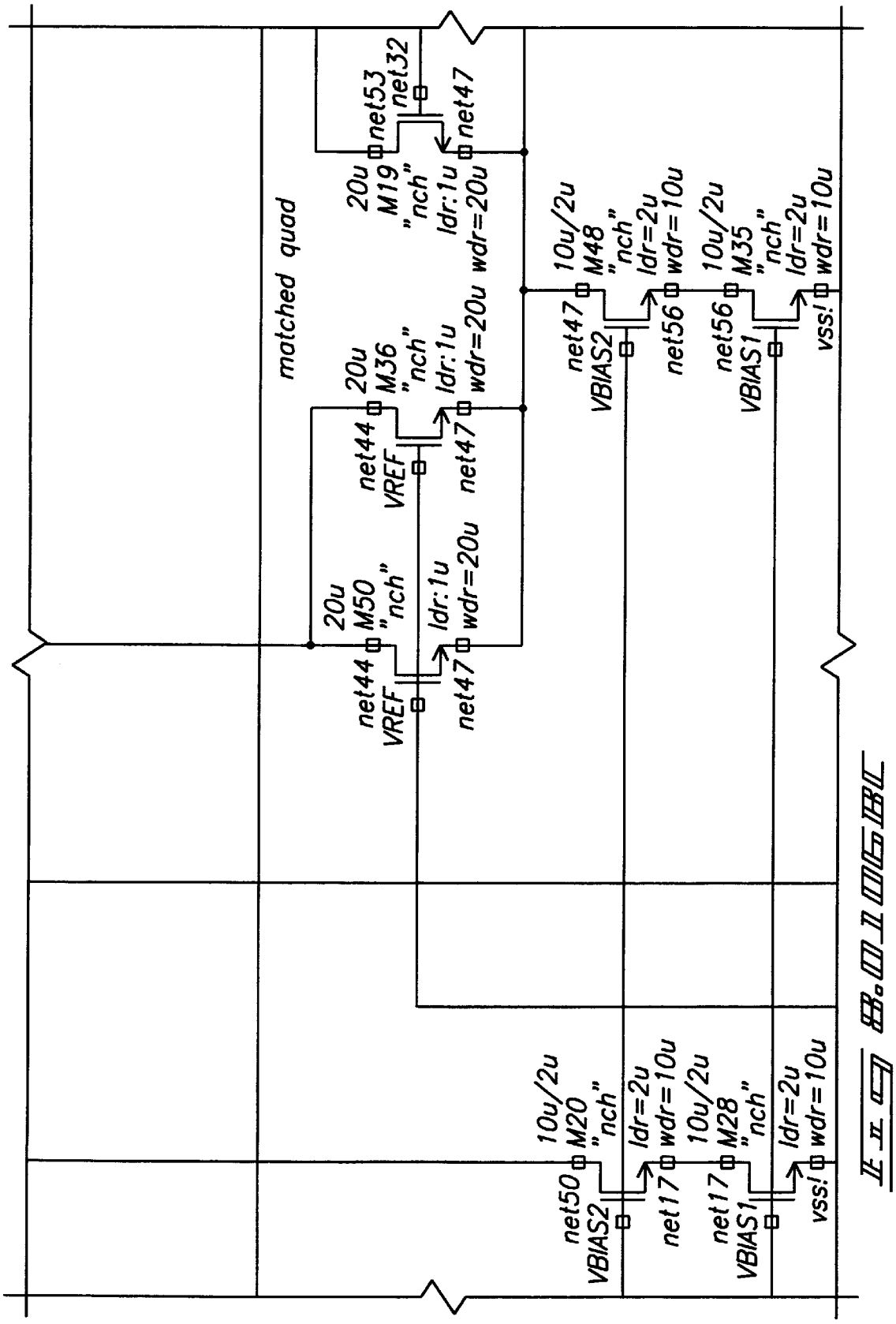

matched quad
net53
net32
20u
M19
"nch"
ldr:1u
wdr=20u
net47
10u/2u
M48
"nch"
ldr=2u
wdr=10u
net47
VBIAS2
net56
10u/2u
M35
"nch"
ldr=2u
wdr=10u
net56
VBIAS1
vss!
20u
M36
"nch"
ldr:1u
wdr=20u
net44
VREF
net47
20u
M50
"nch"
ldr:1u
wdr=20u
net44
VREF
net47
10u/2u
M20
"nch"
ldr=2u
wdr=10u
net50
VBIAS2
net17
10u/2u
M28
"nch"
ldr=2u
wdr=10u
net17
VBIAS1
vss!

FIG. 88.011

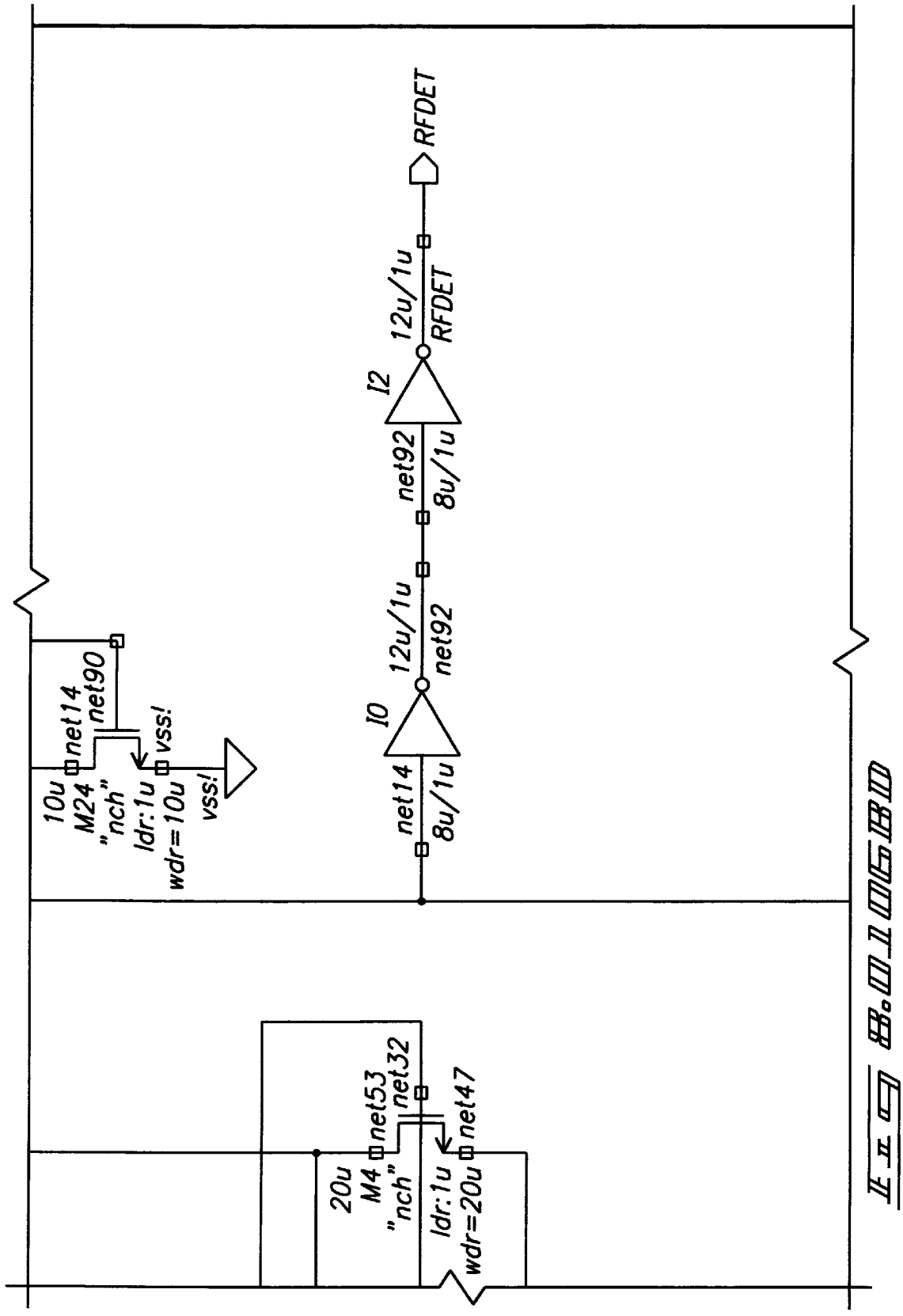


FIG 88.01105810

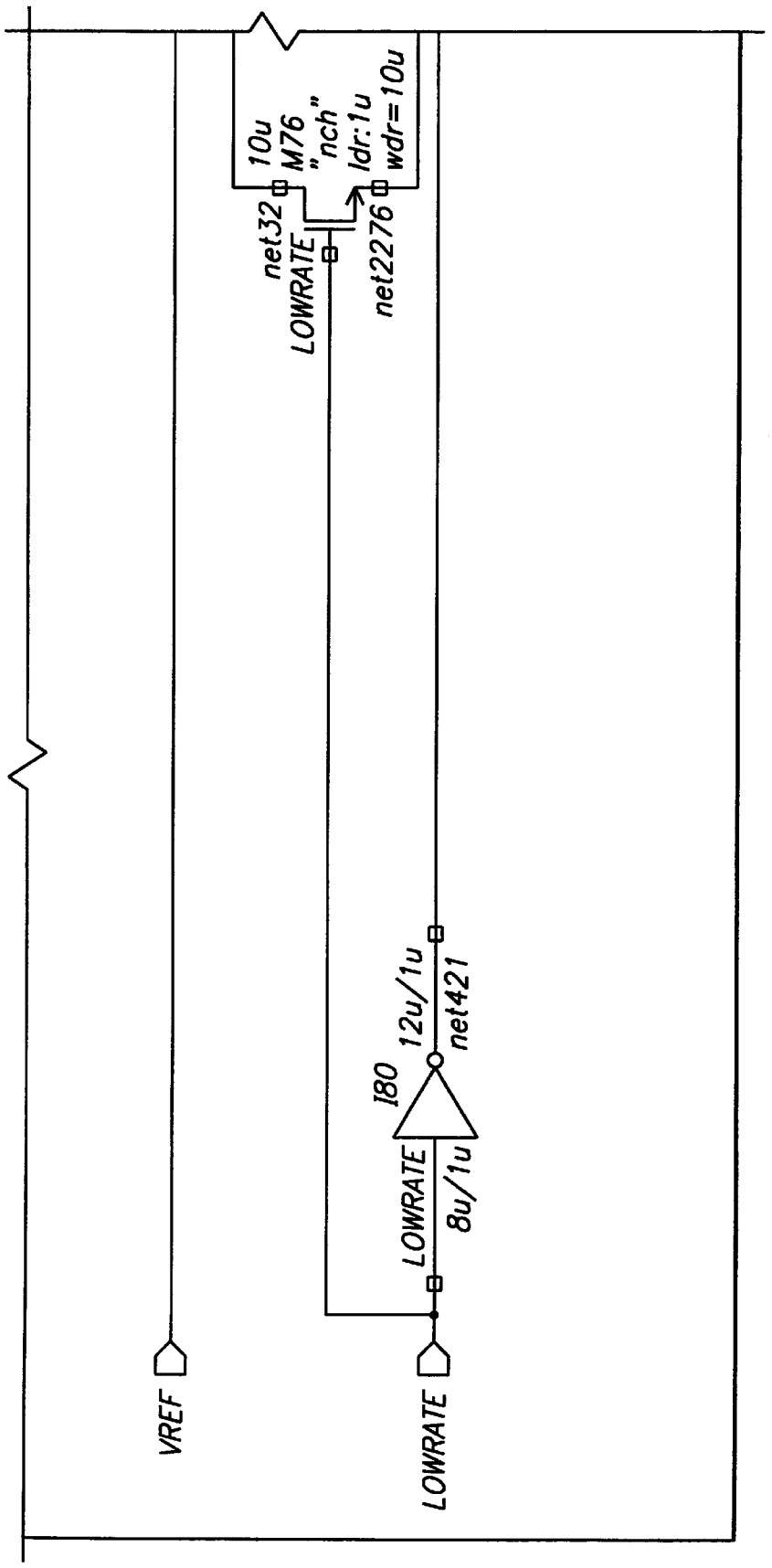

10u
M76
"nch"
ldr:1u
wdr=10u
net32
LOWRATE
net2276
I80
12u/1u
net421
LOWRATE
8u/1u
VREF
LOWRATE

FIG 8.00116A

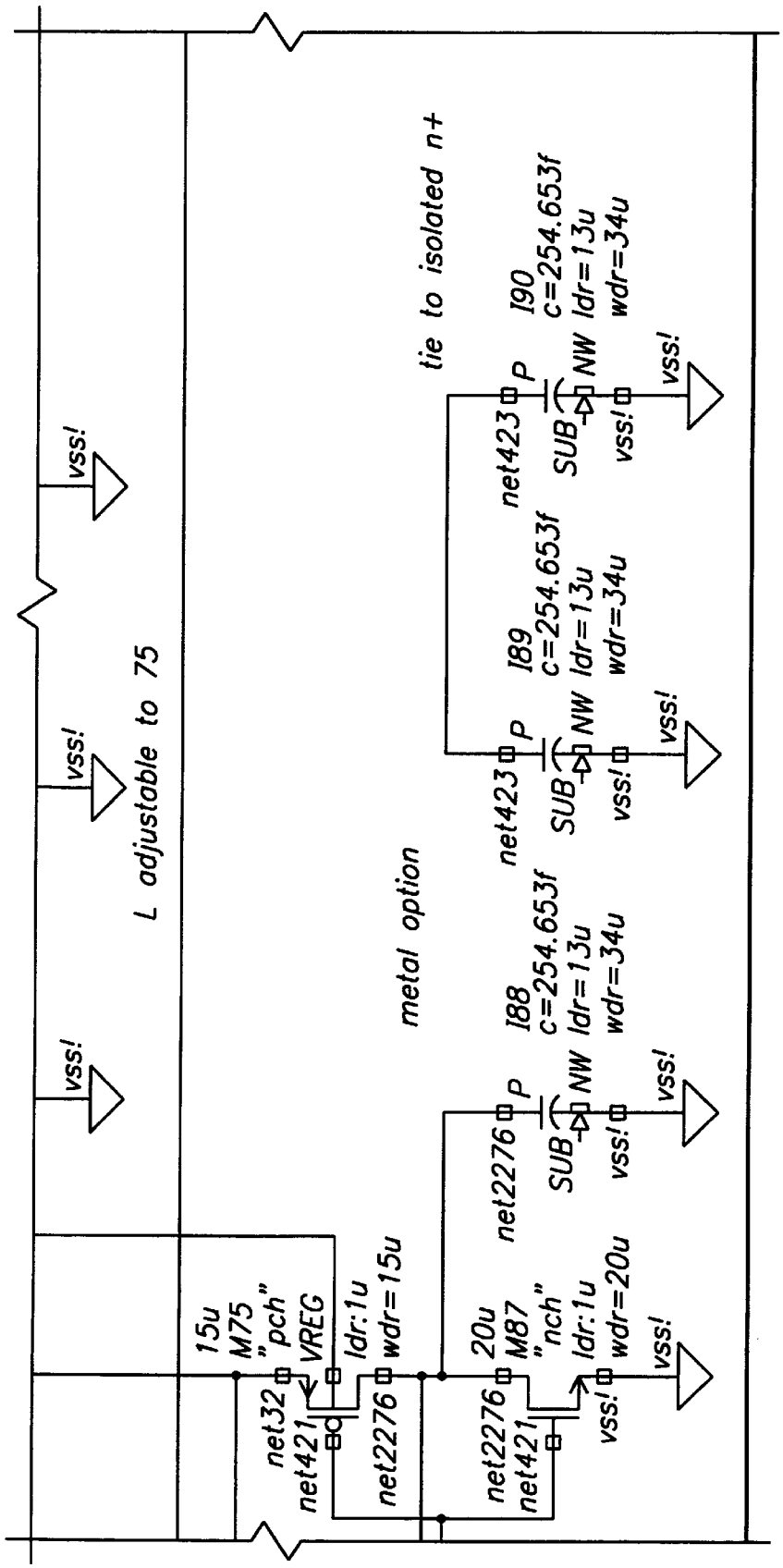

vss!
vss!
vss!
vss!
L adjustable to 75
metal option
tie to isolated n+
15u
M75
"pch"
VREG
ldr:1u
wdr=15u
net32
net421
net2276
20u
M87
"nch"
ldr:1u
wdr=20u
net2276
net421
net2276
P
SUB
NW
I88
c=254.653f
ldr=13u
wdr=34u
net423
I89
c=254.653f
ldr=13u
wdr=34u
net423
I90
c=254.653f
ldr=13u
wdr=34u

FIG. 88.011

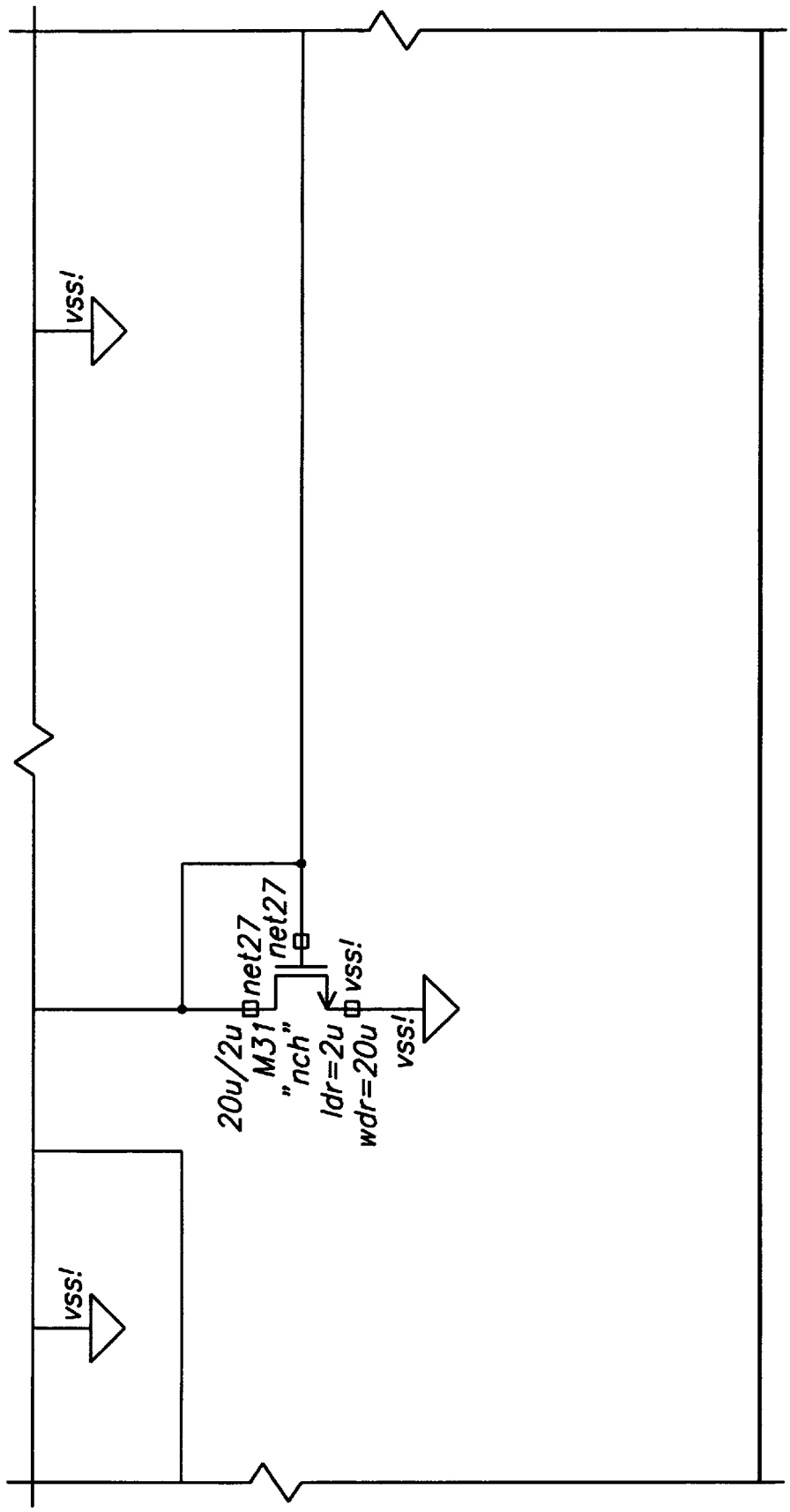


FIG 88.01105C

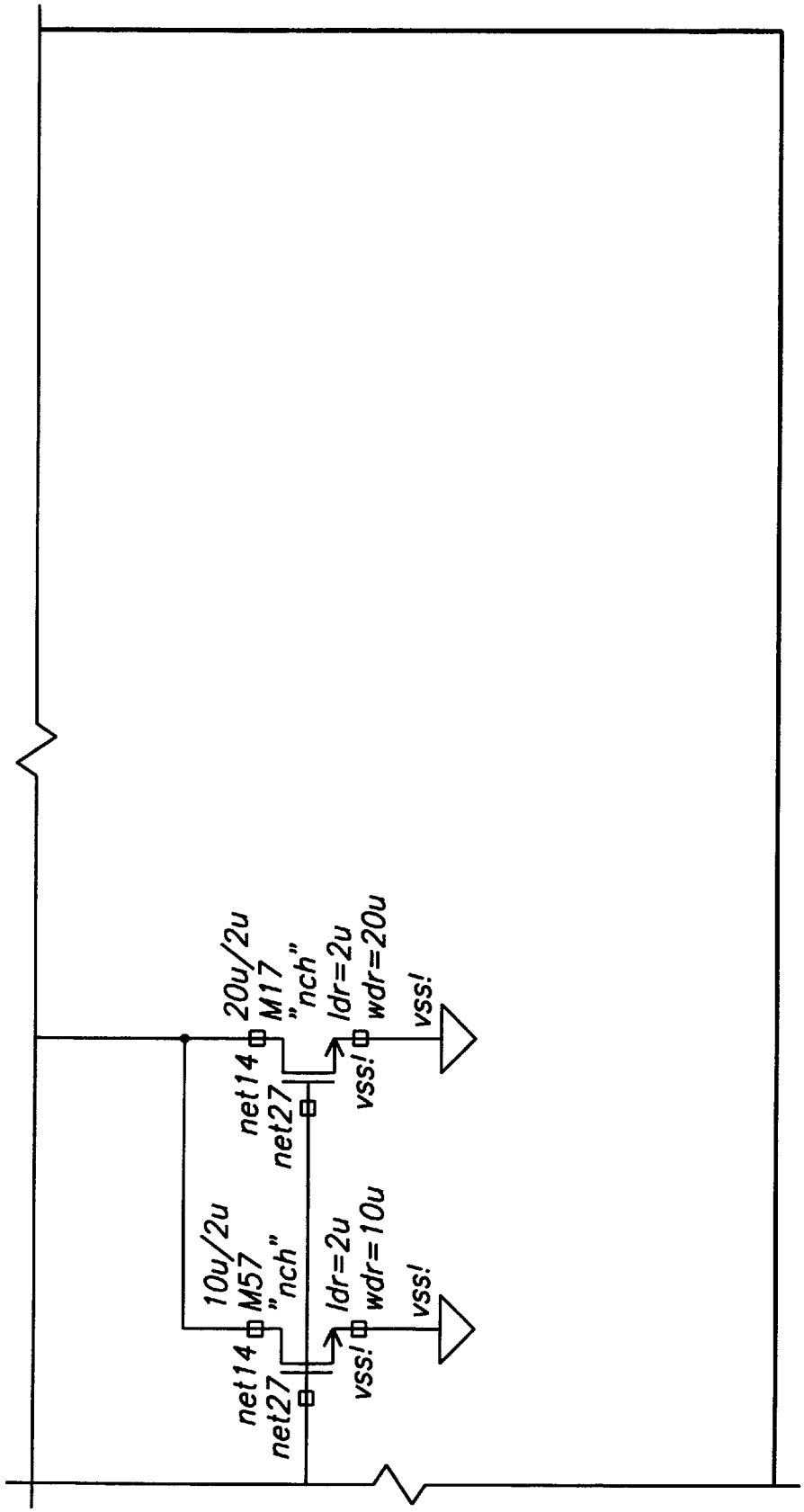

20u/2u
M17
"nch"
ldr=2u
wdr=20u
vss!
net14
net27
vss!
10u/2u
M57
"nch"
ldr=2u
wdr=10u
vss!
net14
net27
vss!

FIG 8.0115C

8.0107AA	8.0107AB	8.0107AC	8.0107AD	8.0107AE	8.0107AF	8.0107AG	8.0107AH	8.0107AI	8.0107AJ	8.0107AK	8.0107AL	8.0107AM
8.0107BA	8.0107BB	8.0107BC	8.0107BD	8.0107BE	8.0107BF	8.0107BG	8.0107BH	8.0107BI	8.0107BJ	8.0701BK	8.0107BL	8.0107BM
8.0107CA	8.0107CB	8.0107CC	8.0107CD	8.0107CE	8.0107CF	8.0107CG	8.0107CH	8.0107CI	8.0107CJ	8.0107CK	8.0107CL	8.0107CM
8.0107DA	8.0107DB	8.0107DC	8.0107DD	8.0107DE	8.0107DF	8.0107DG	8.0107DH	8.0107DI	8.0107DJ	8.0107DK	8.0107DL	8.0107DM
8.0107EA	8.0107EB	8.0107EC	8.0107ED	8.0107EE	8.0107EF	8.0107EG	8.0107EH	8.0107EI	8.0107EJ	8.0107EK	8.0107EL	8.0107EM
8.0107FA	8.0107FB	8.0107FC	8.0107FD	8.0107FE	8.0107FF	8.0107FG	8.0107FH	8.0107FI	8.0107FJ	8.0107FK	8.0107FL	8.0107FM
8.0107GA	8.0107GB	8.0107GC	8.0107GD	8.0107GE	8.0107GF	8.0107GG	8.0107GH	8.0107GI	8.0107GJ	8.0107GK	8.0107GL	8.0107GM

8.0107CN	8.0107EN
8.0107DN	8.0107FN
8.0107EN	8.0107GN
8.0107FN	
8.0107GN	

FIG. 8.0107

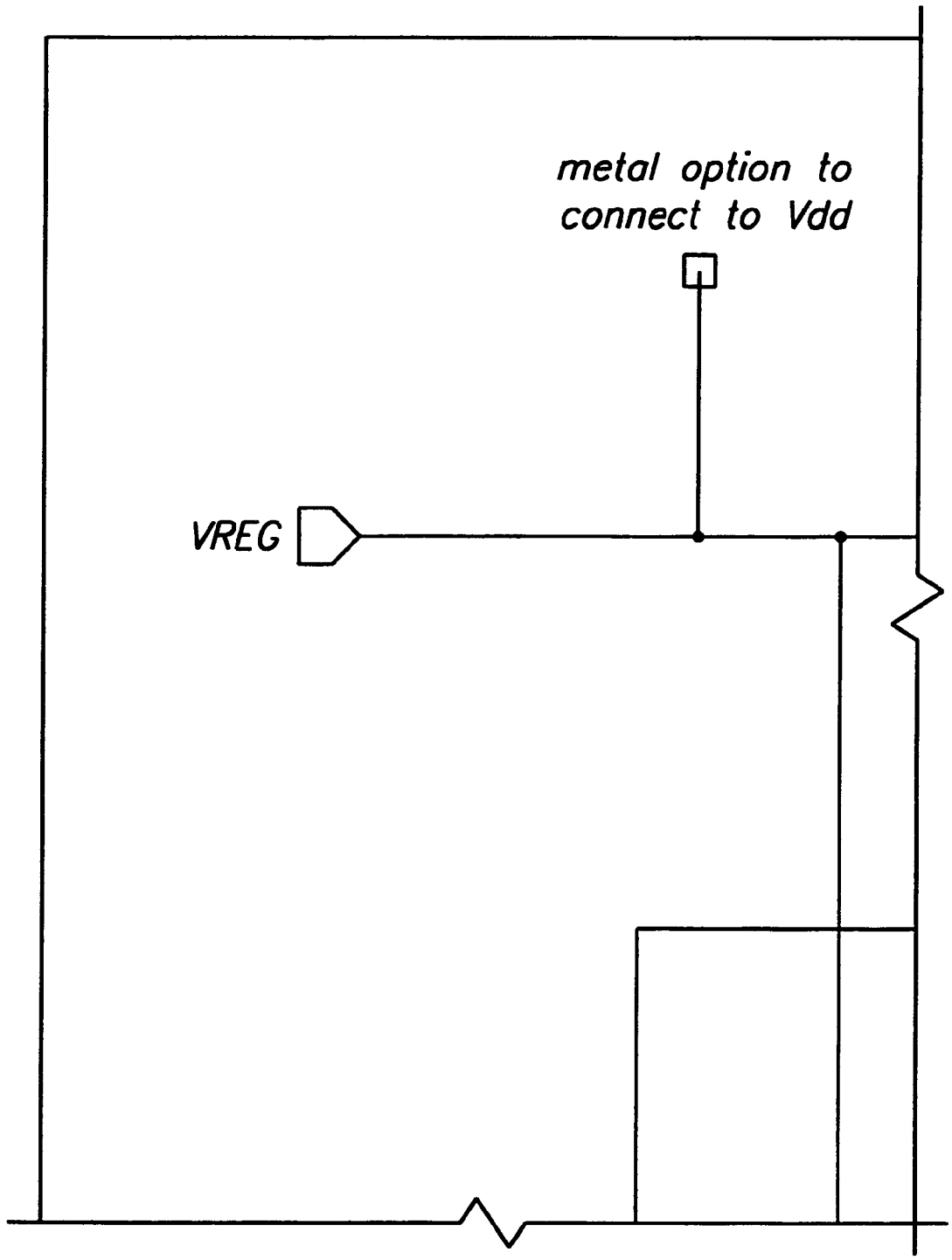


Fig 88.0107AA

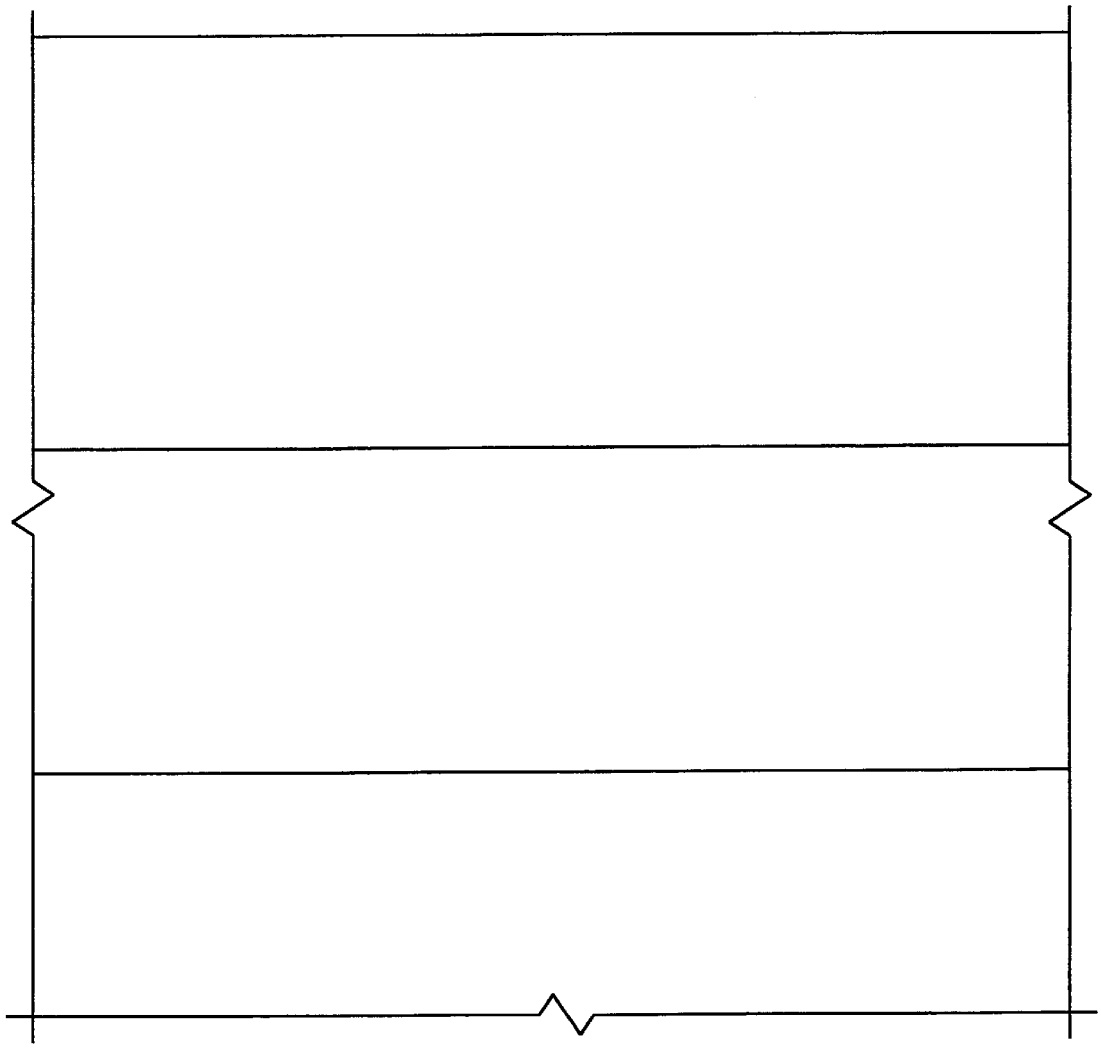


Fig 8.0107AB

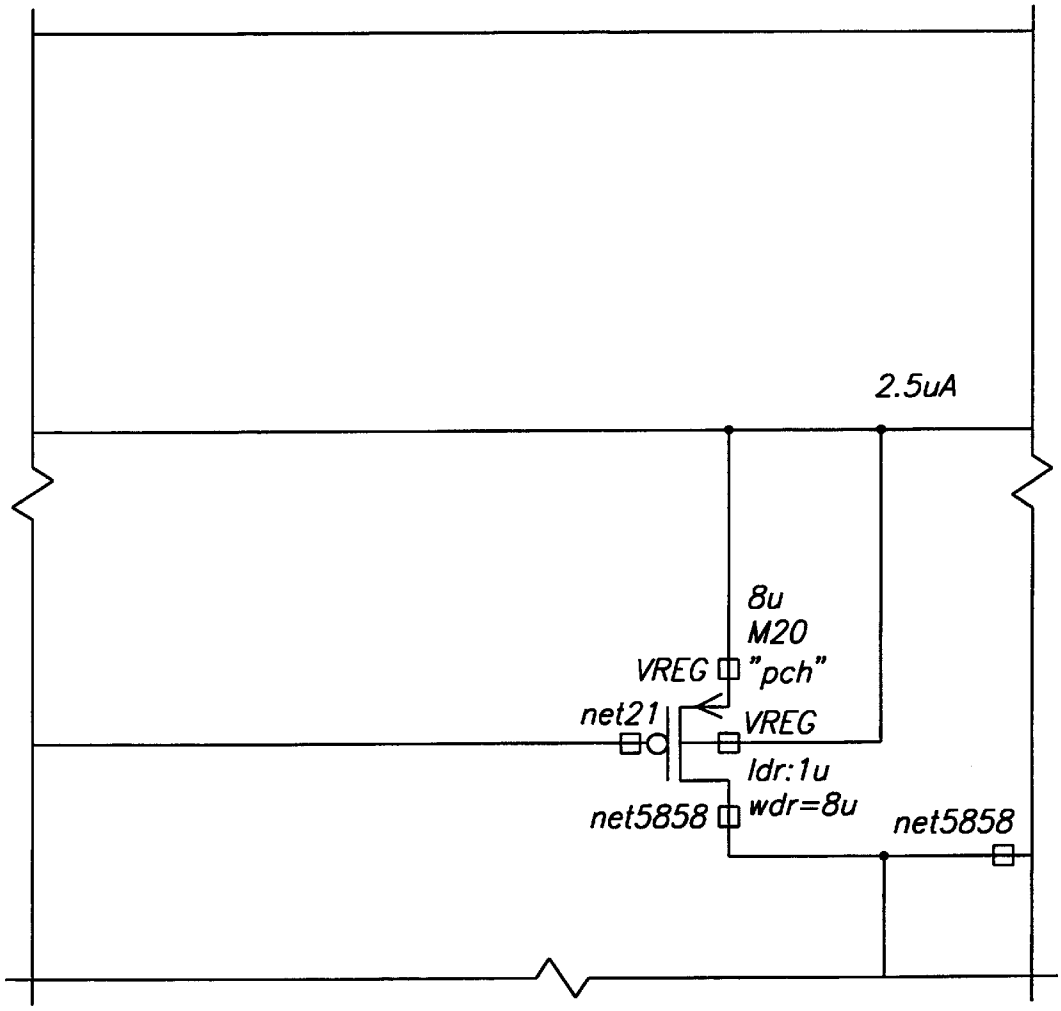


FIG 8.0107AC

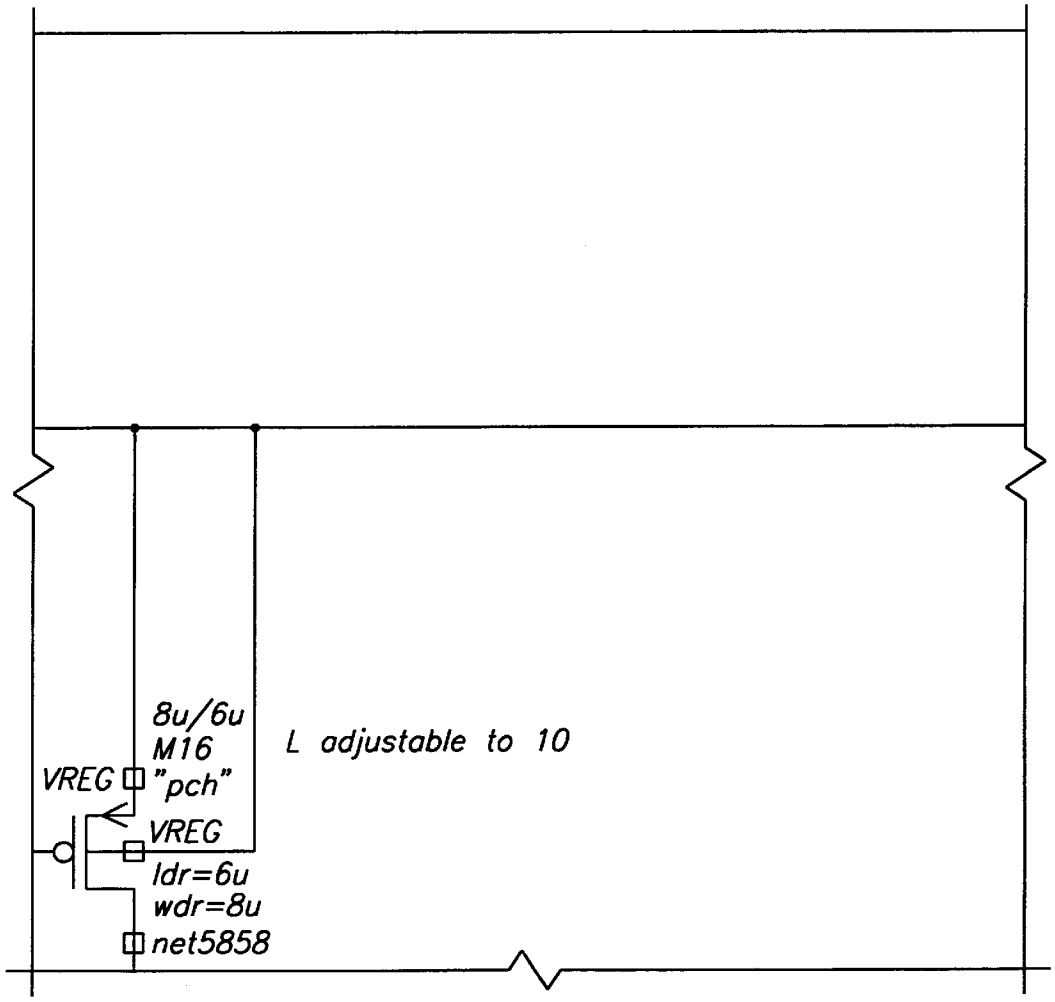

8u/6u
M16
"pch"
VREG
VREG
ldr=6u
wdr=8u
net5858
L adjustable to 10

FIG 8010AD

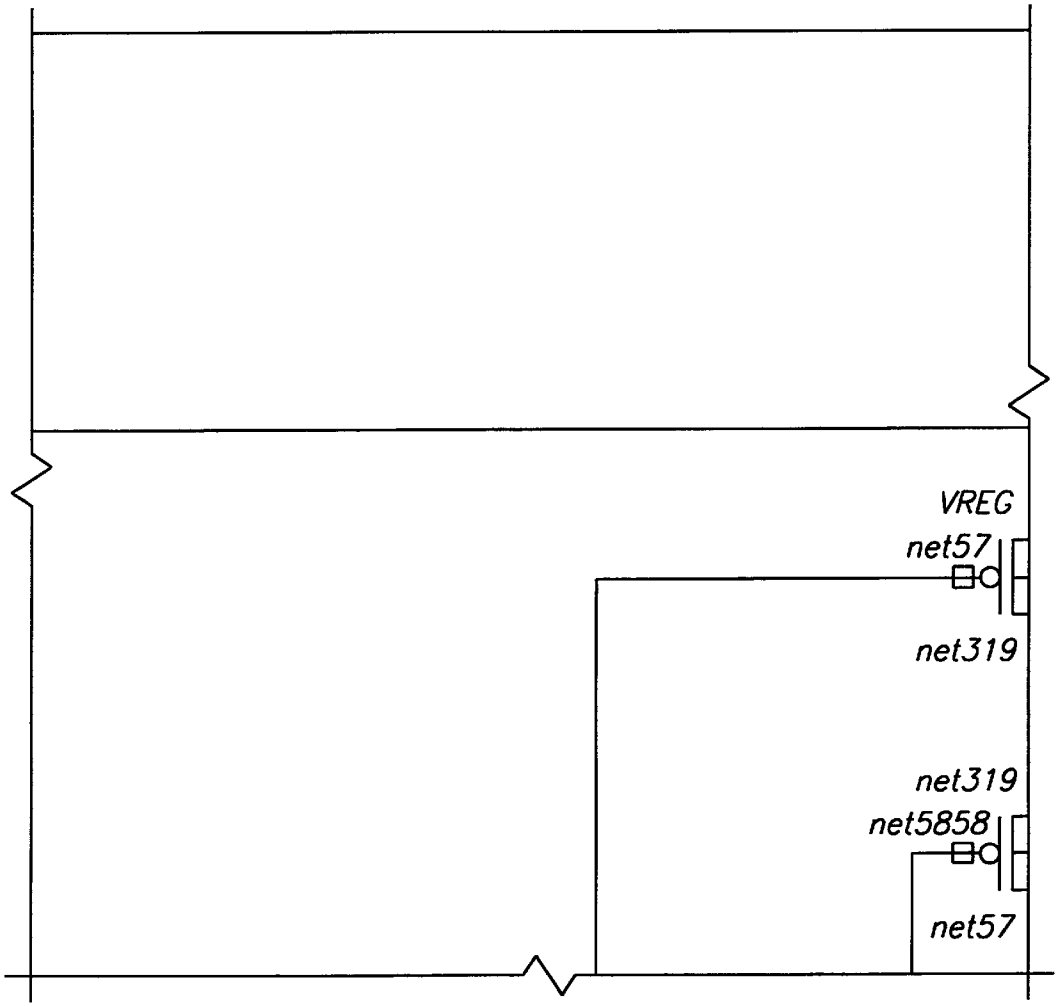


Fig 8.0107AE

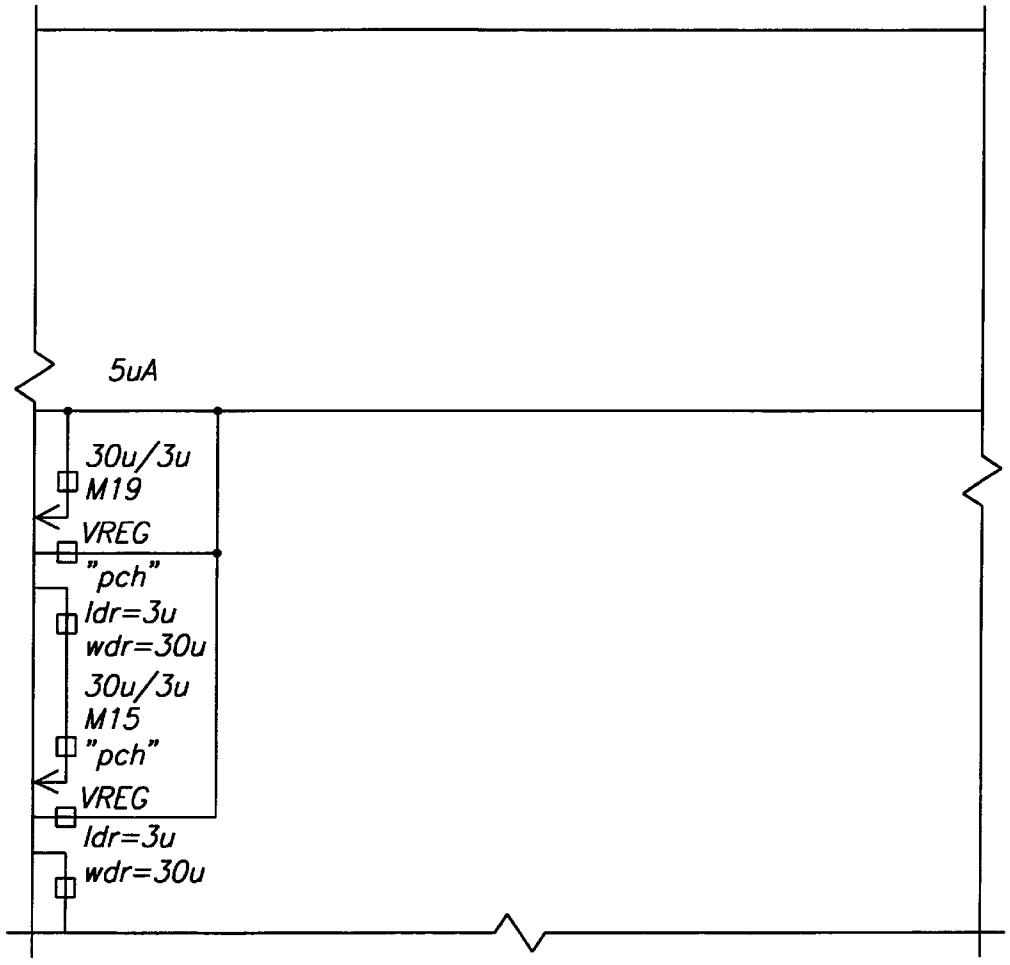

5uA
30u/3u
M19
VREG
"pch"
ldr=3u
wdr=30u
30u/3u
M15
"pch"
VREG
ldr=3u
wdr=30u

Fig 8.0107AF

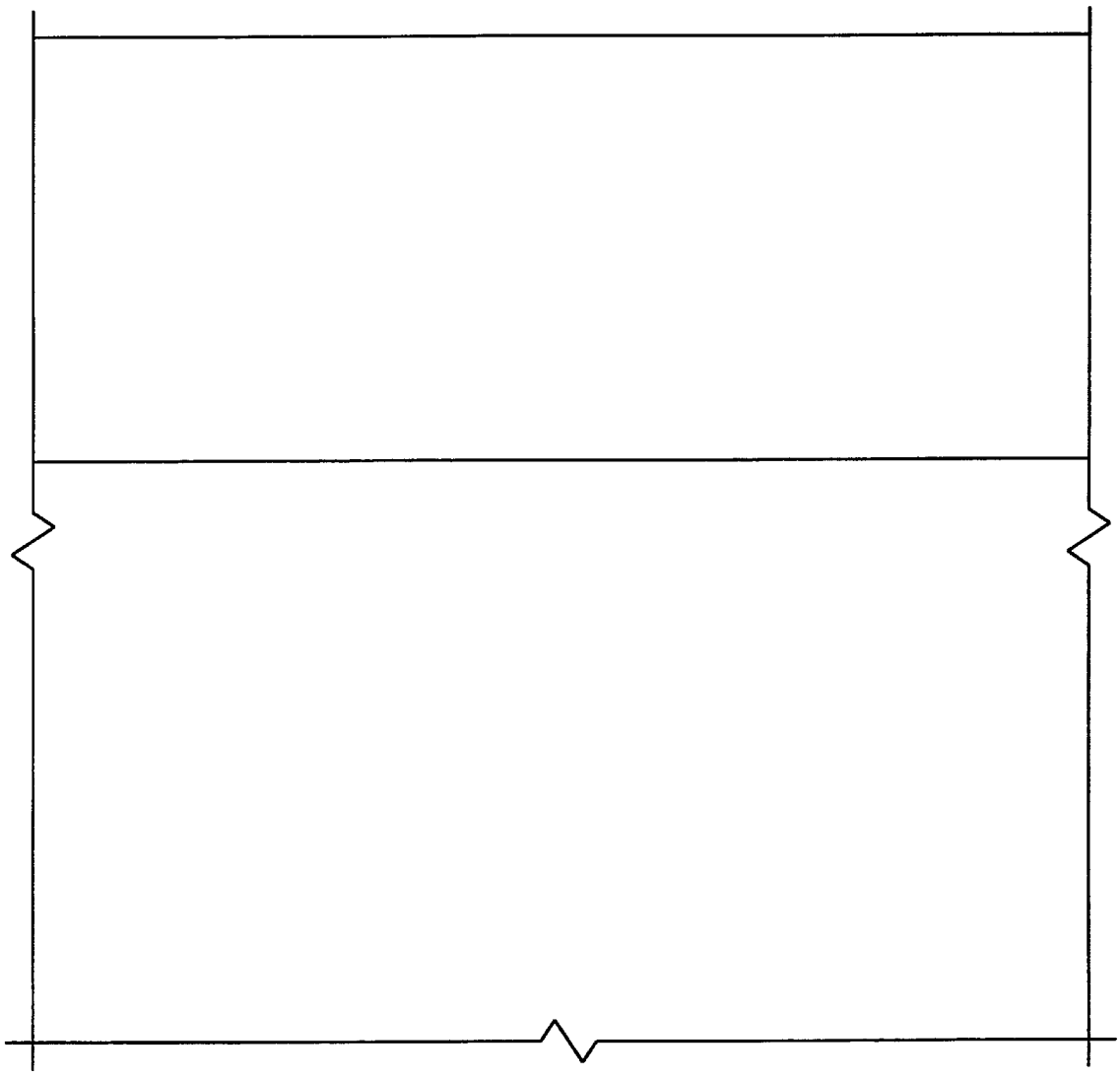


Fig 8.0107AG

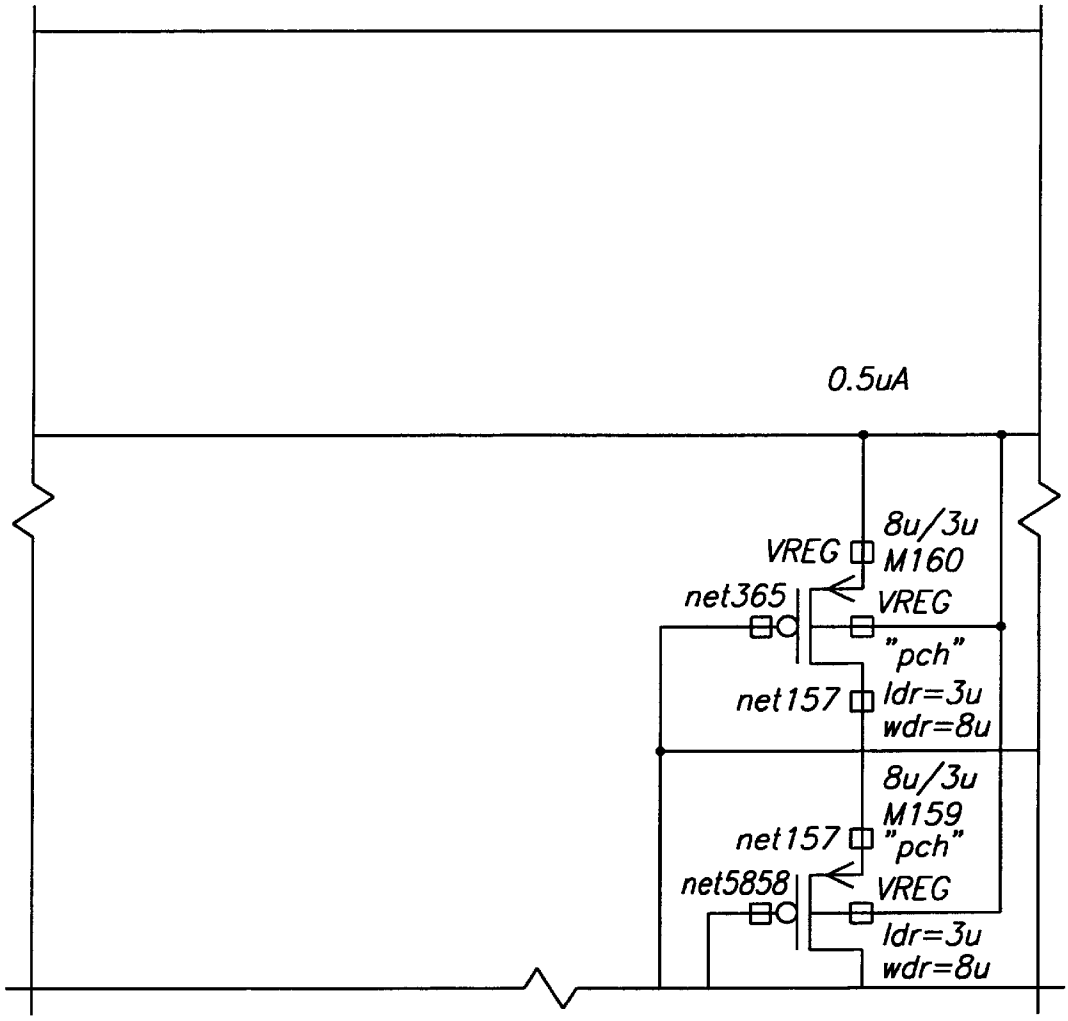

0.5uA
8u/3u
M160
VREG
net365
VREG
"pch"
net157
ldr=3u
wdr=8u
8u/3u
M159
net157
"pch"
net5858
VREG
ldr=3u
wdr=8u

FIG 8.0107AH

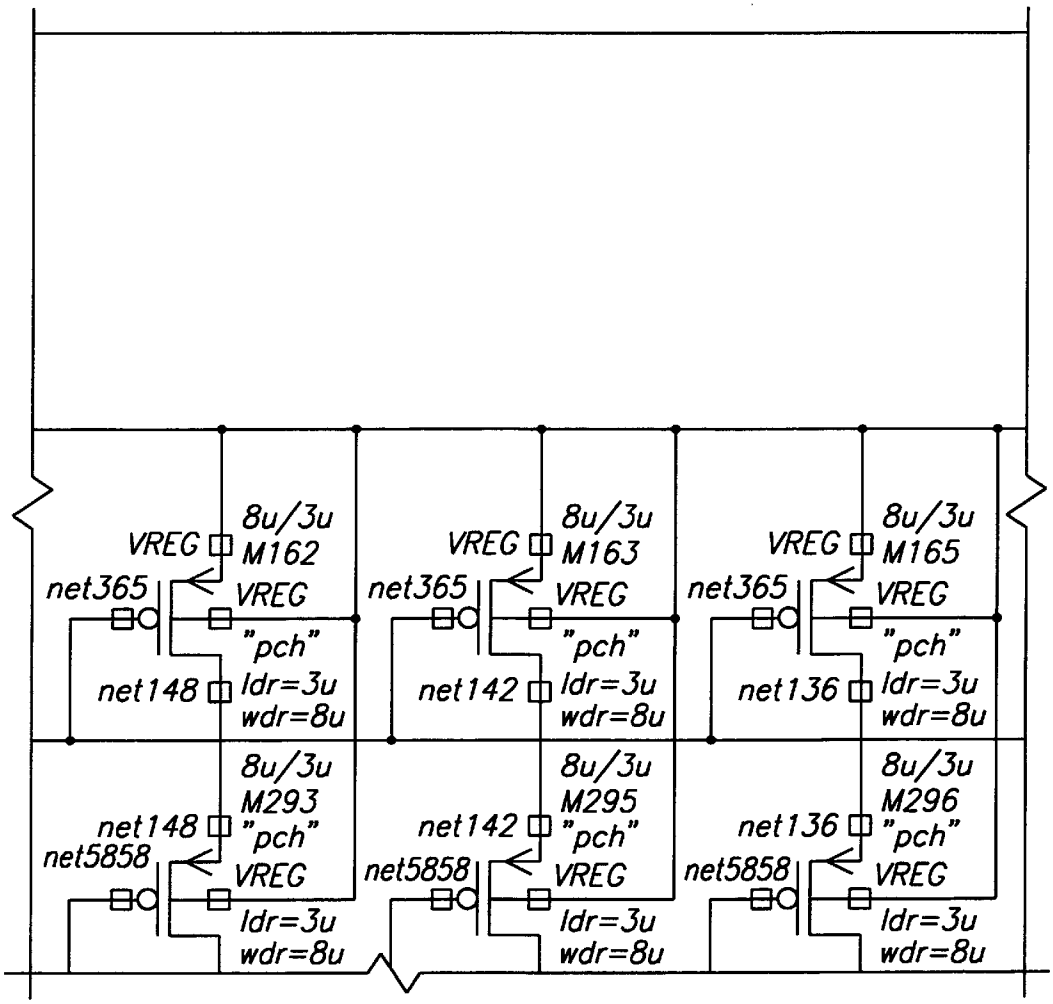


Fig 8.0110AII

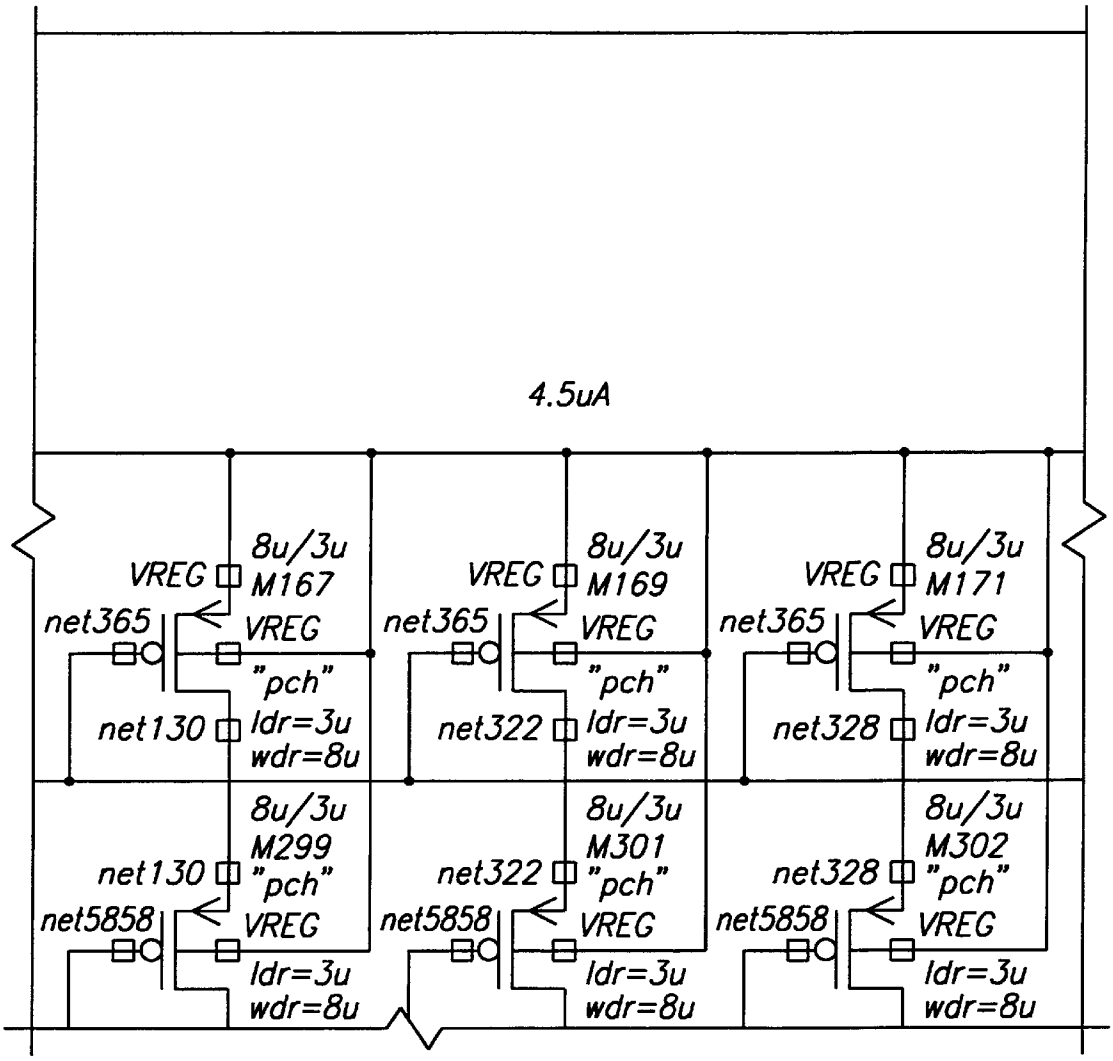

4.5uA
8u/3u
M167
VREG
net365
VREG
"pch"
net130
ldr=3u
wdr=8u
8u/3u
M169
VREG
net365
VREG
"pch"
net322
ldr=3u
wdr=8u
8u/3u
M171
VREG
net365
VREG
"pch"
net328
ldr=3u
wdr=8u
8u/3u
M299
net130
"pch"
net5858
VREG
ldr=3u
wdr=8u
8u/3u
M301
net322
"pch"
net5858
VREG
ldr=3u
wdr=8u
8u/3u
M302
net328
"pch"
net5858
VREG
ldr=3u
wdr=8u

Fig 8.0110Aa

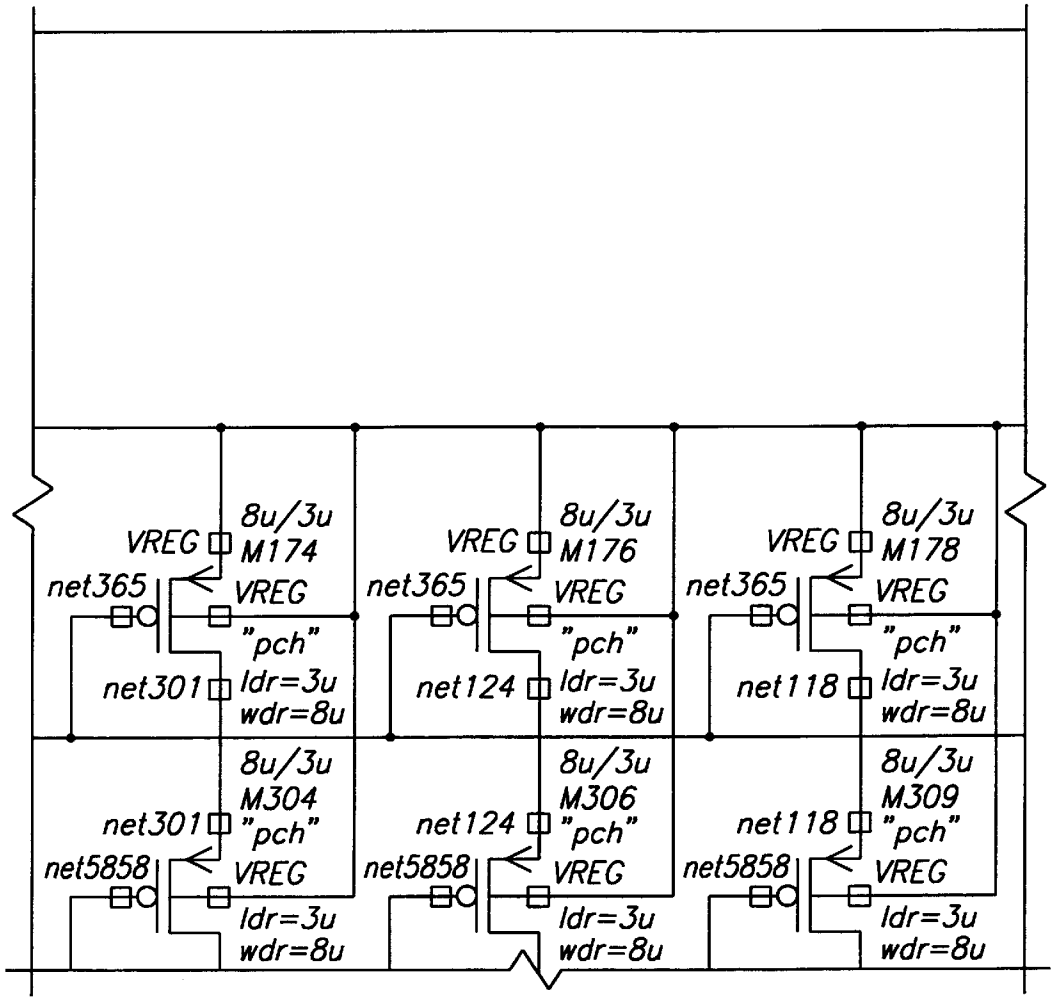

8u/3u
M174
VREG
net365
VREG
"pch"
net301
ldr=3u
wdr=8u
8u/3u
M176
VREG
net365
VREG
"pch"
net124
ldr=3u
wdr=8u
8u/3u
M178
VREG
net365
VREG
"pch"
net118
ldr=3u
wdr=8u
8u/3u
M304
net301
"pch"
net5858
VREG
ldr=3u
wdr=8u
8u/3u
M306
net124
"pch"
net5858
VREG
ldr=3u
wdr=8u
8u/3u
M309
net118
"pch"
net5858
VREG
ldr=3u
wdr=8u

Fig 8.0110AK

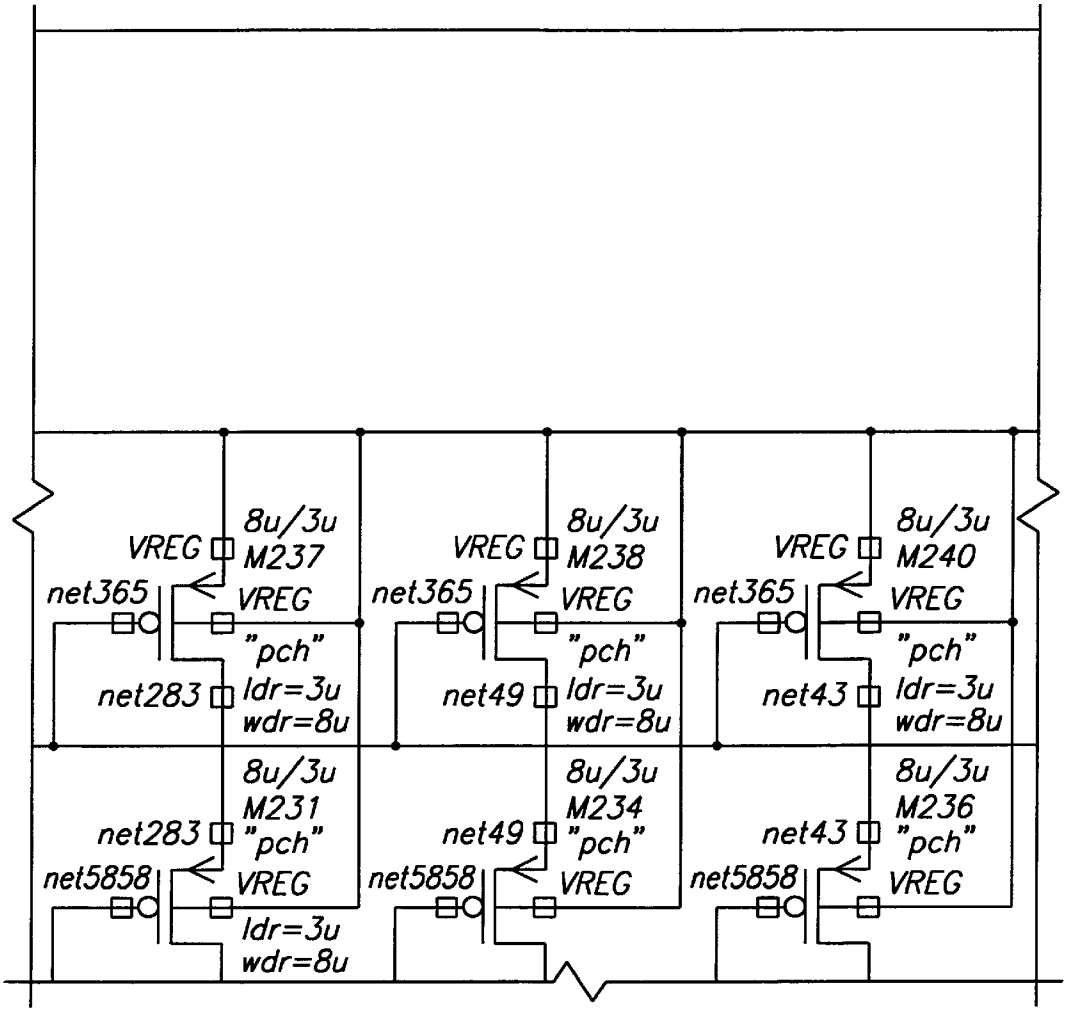


FIG 8B.0131AL

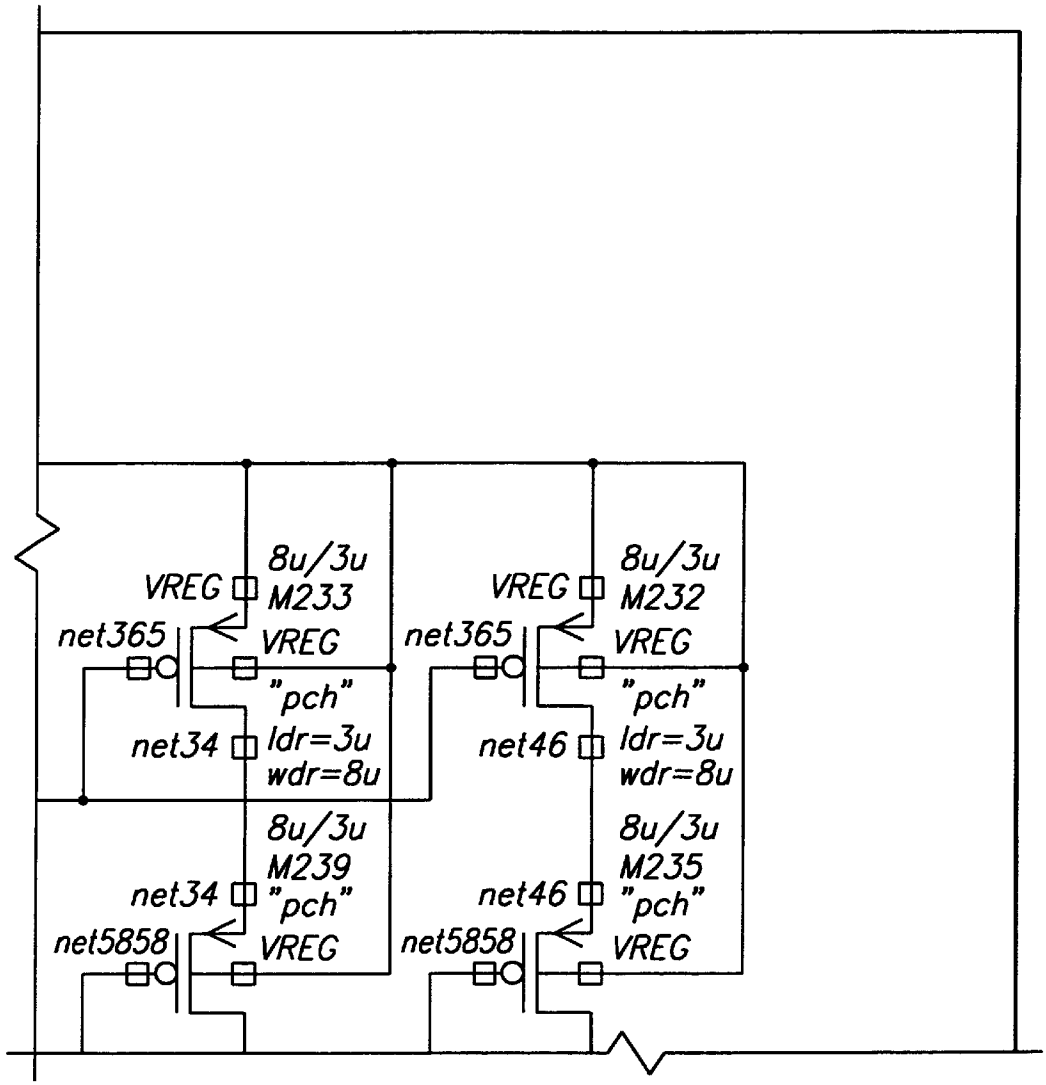

8u/3u
M233
VREG
net365
VREG
"pch"
net34
ldr=3u
wdr=8u
8u/3u
M232
VREG
net365
VREG
"pch"
net46
ldr=3u
wdr=8u
8u/3u
M239
net34
"pch"
net5858
VREG
8u/3u
M235
net46
"pch"
net5858
VREG

Fig 8.0107AM

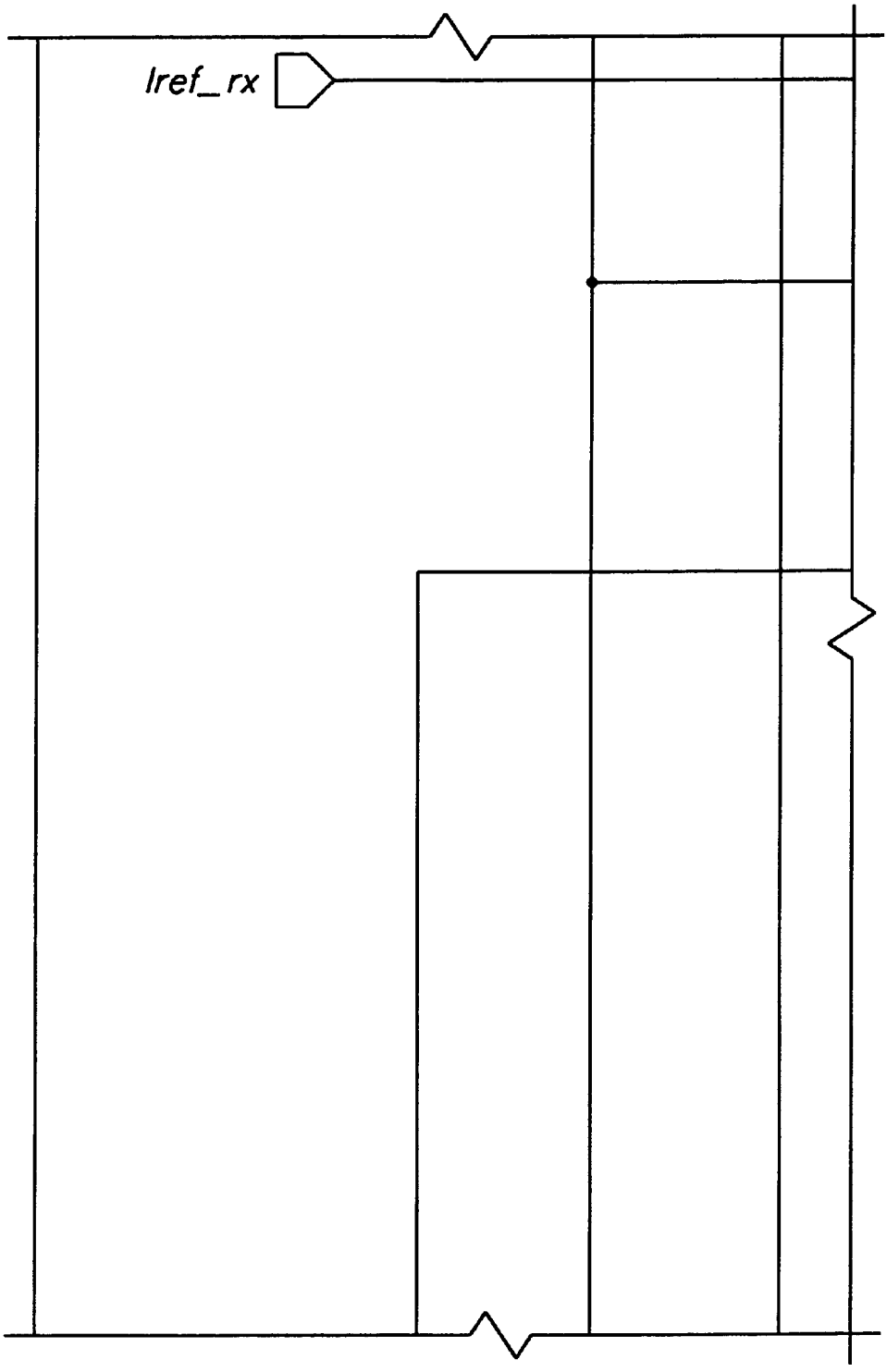


Fig. 8.0108A

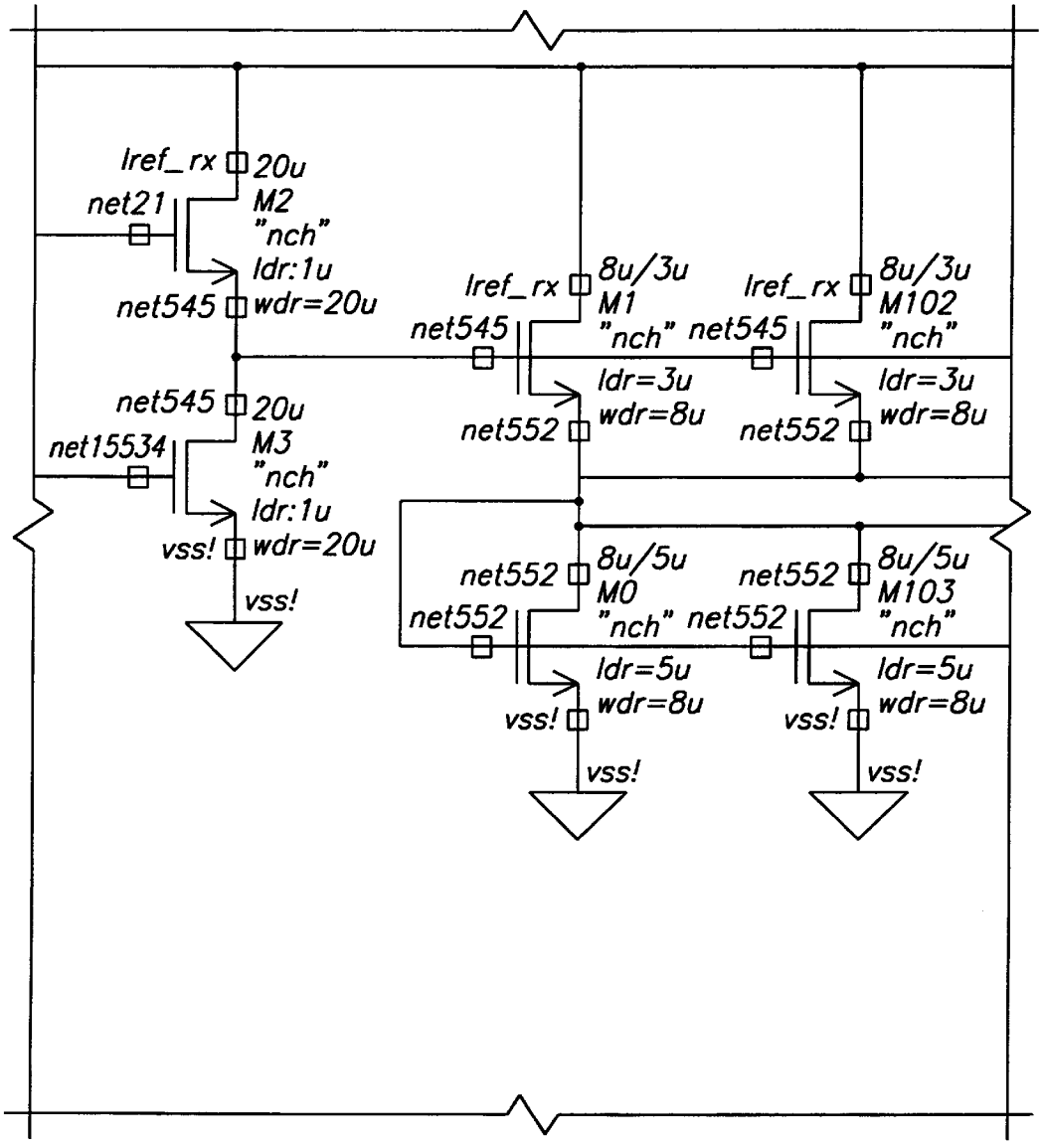

Iref_rx
20u
M2
"nch"
net21
ldr:1u
net545
wdr=20u
Iref_rx
8u/3u
M1
"nch"
net545
ldr=3u
net552
wdr=8u
Iref_rx
8u/3u
M102
"nch"
net545
ldr=3u
net552
wdr=8u
net545
20u
M3
"nch"
net15534
ldr:1u
vss!
wdr=20u
vss!
net552
8u/5u
M0
"nch"
net552
ldr=5u
vss!
wdr=8u
vss!
net552
8u/5u
M103
"nch"
net552
ldr=5u
vss!
wdr=8u
vss!

FIG 8.0102B

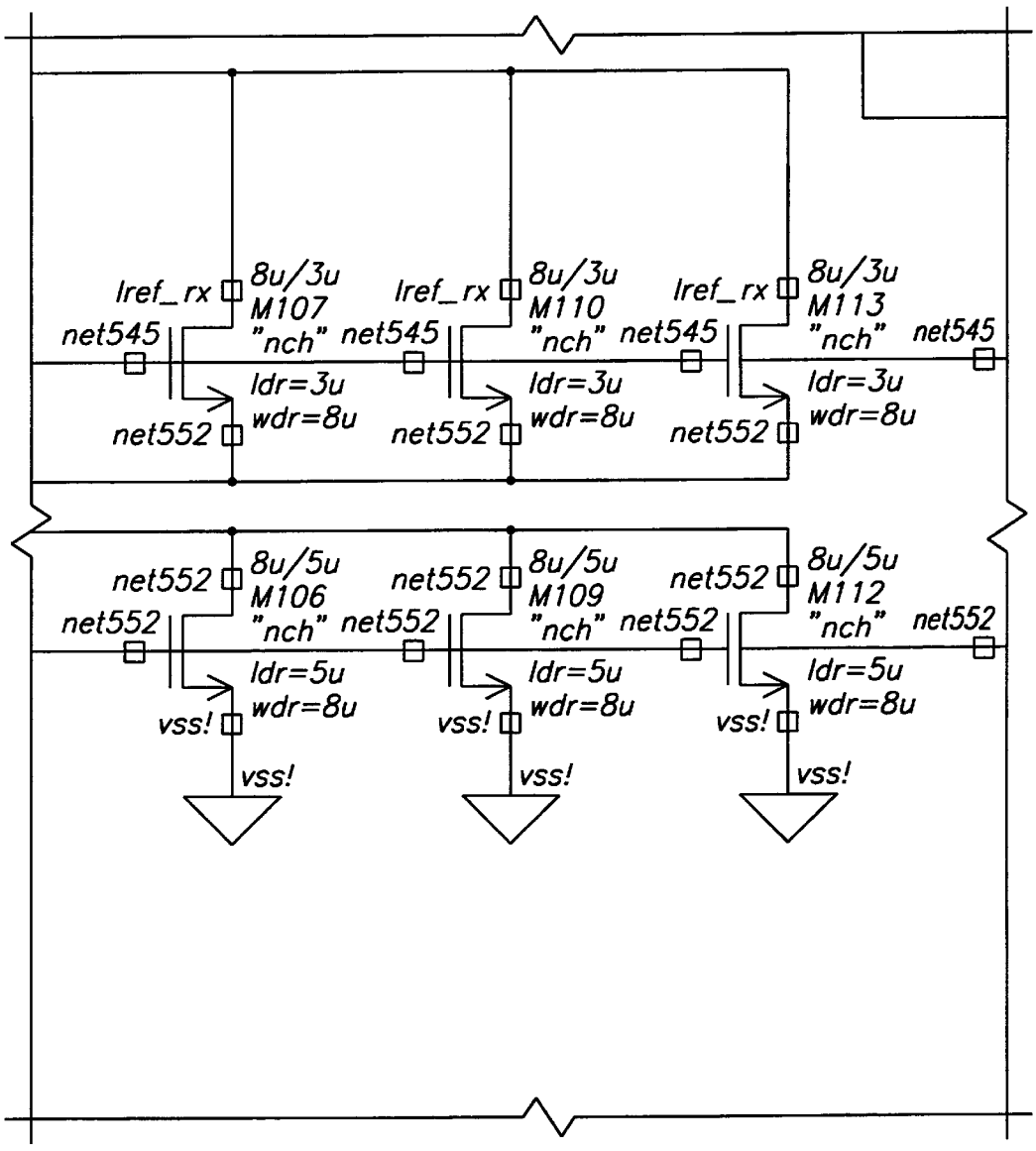

Iref_rx
8u/3u
M107
"nch"
net545
ldr=3u
wdr=8u
net552
Iref_rx
8u/3u
M110
"nch"
net545
ldr=3u
wdr=8u
net552
Iref_rx
8u/3u
M113
"nch"
net545
ldr=3u
wdr=8u
net552
net552
8u/5u
M106
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!
net552
8u/5u
M109
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!
net552
8u/5u
M112
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!

Fig 8.0110BC

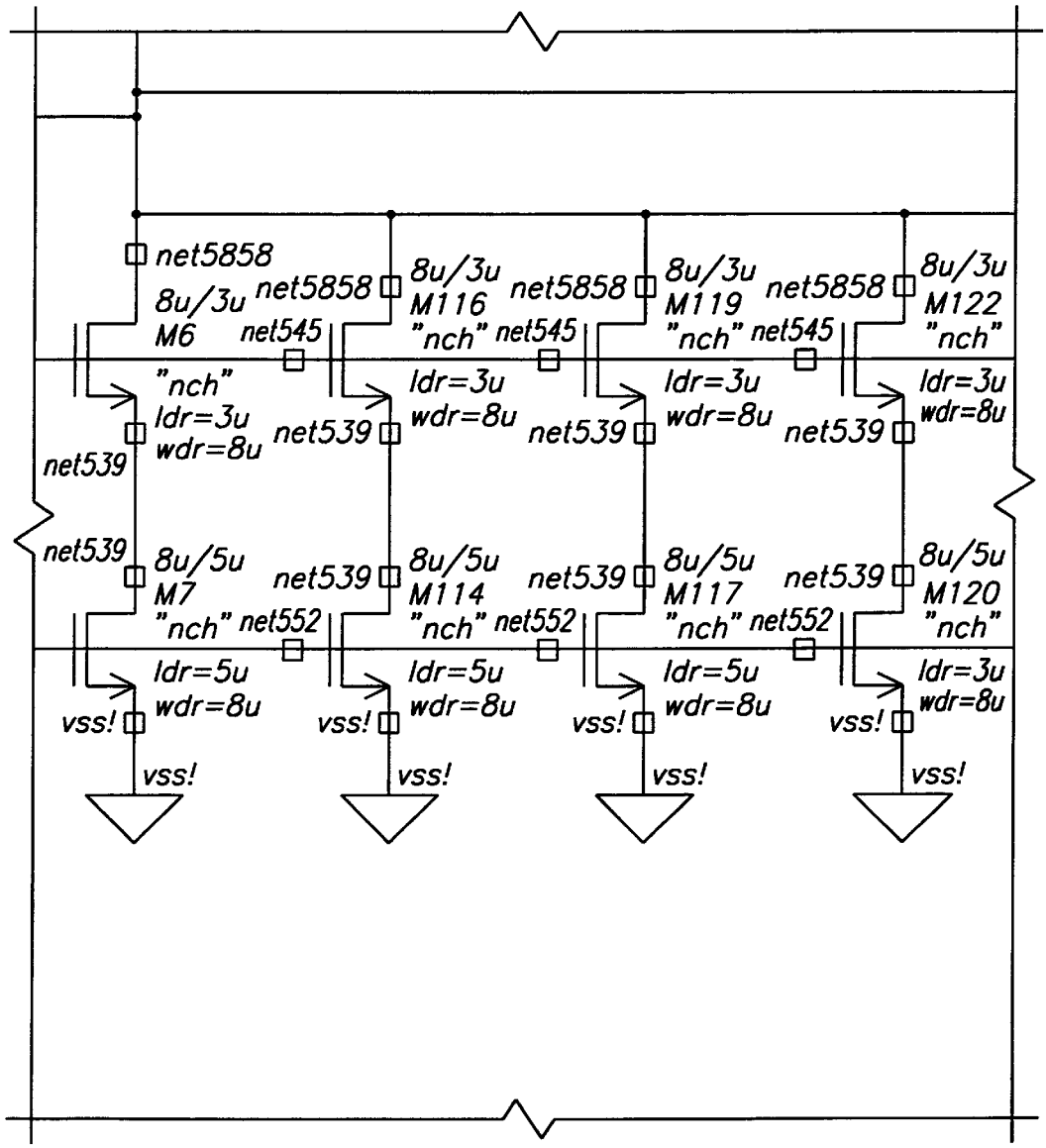

net5858
8u/3u
M6
"nch"
ldr=3u
wdr=8u
net539
8u/5u
M7
"nch"
ldr=5u
wdr=8u
vss!
net545
net552
net5858
8u/3u
M116
"nch"
ldr=3u
wdr=8u
net539
8u/5u
M114
"nch"
ldr=5u
wdr=8u
vss!
net5858
8u/3u
M119
"nch"
ldr=3u
wdr=8u
net539
8u/5u
M117
"nch"
ldr=5u
wdr=8u
vss!
net5858
8u/3u
M122
"nch"
ldr=3u
wdr=8u
net539
8u/5u
M120
"nch"
ldr=3u
wdr=8u
vss!

Fig 8.0107BD

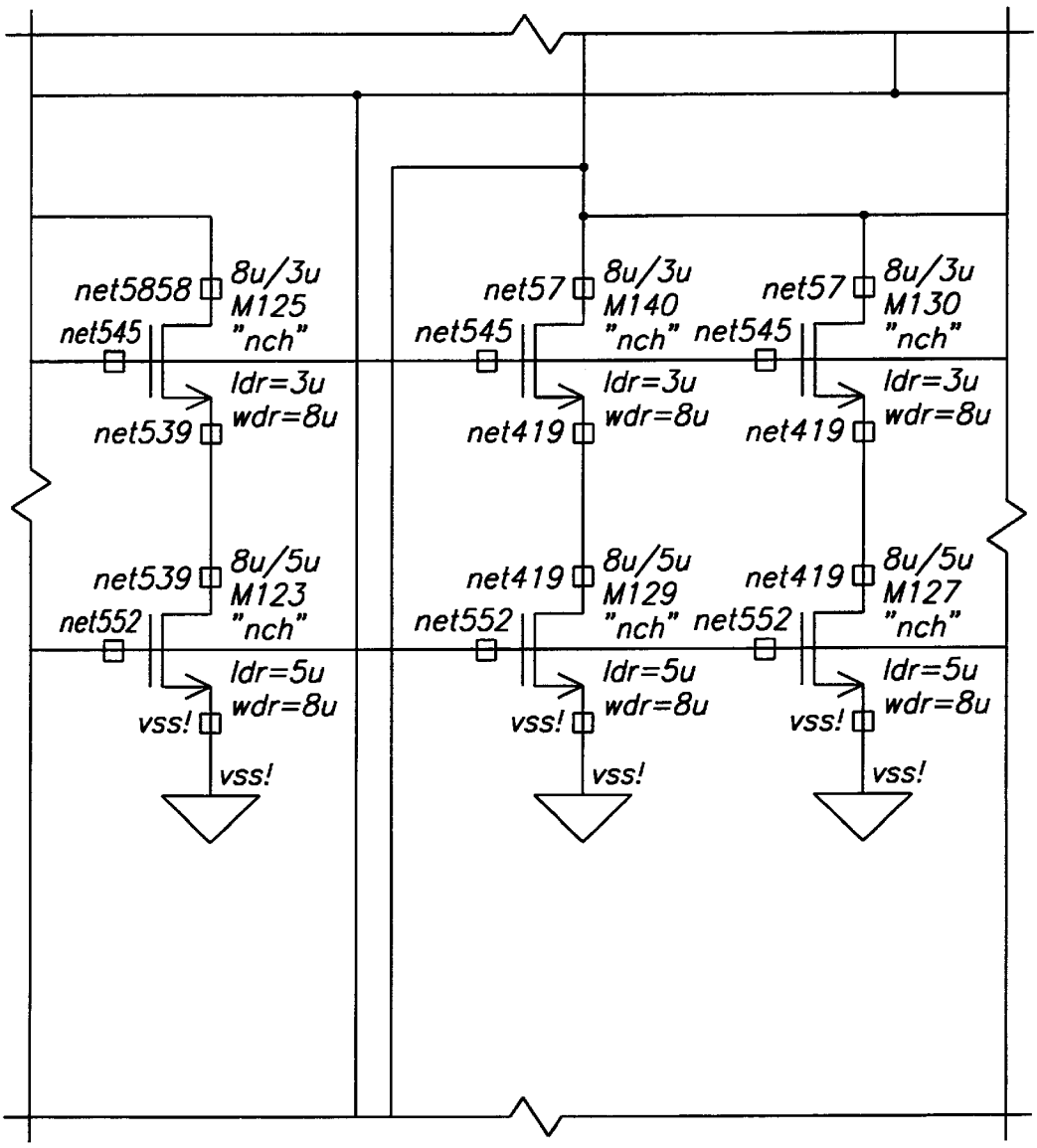

net5858
8u/3u
M125
"nch"
net545
ldr=3u
wdr=8u
net539
net539
8u/5u
M123
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!
net57
8u/3u
M140
"nch"
net545
ldr=3u
wdr=8u
net419
net419
8u/5u
M129
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!
net57
8u/3u
M130
"nch"
net545
ldr=3u
wdr=8u
net419
net419
8u/5u
M127
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!

Fig 8.0107BE

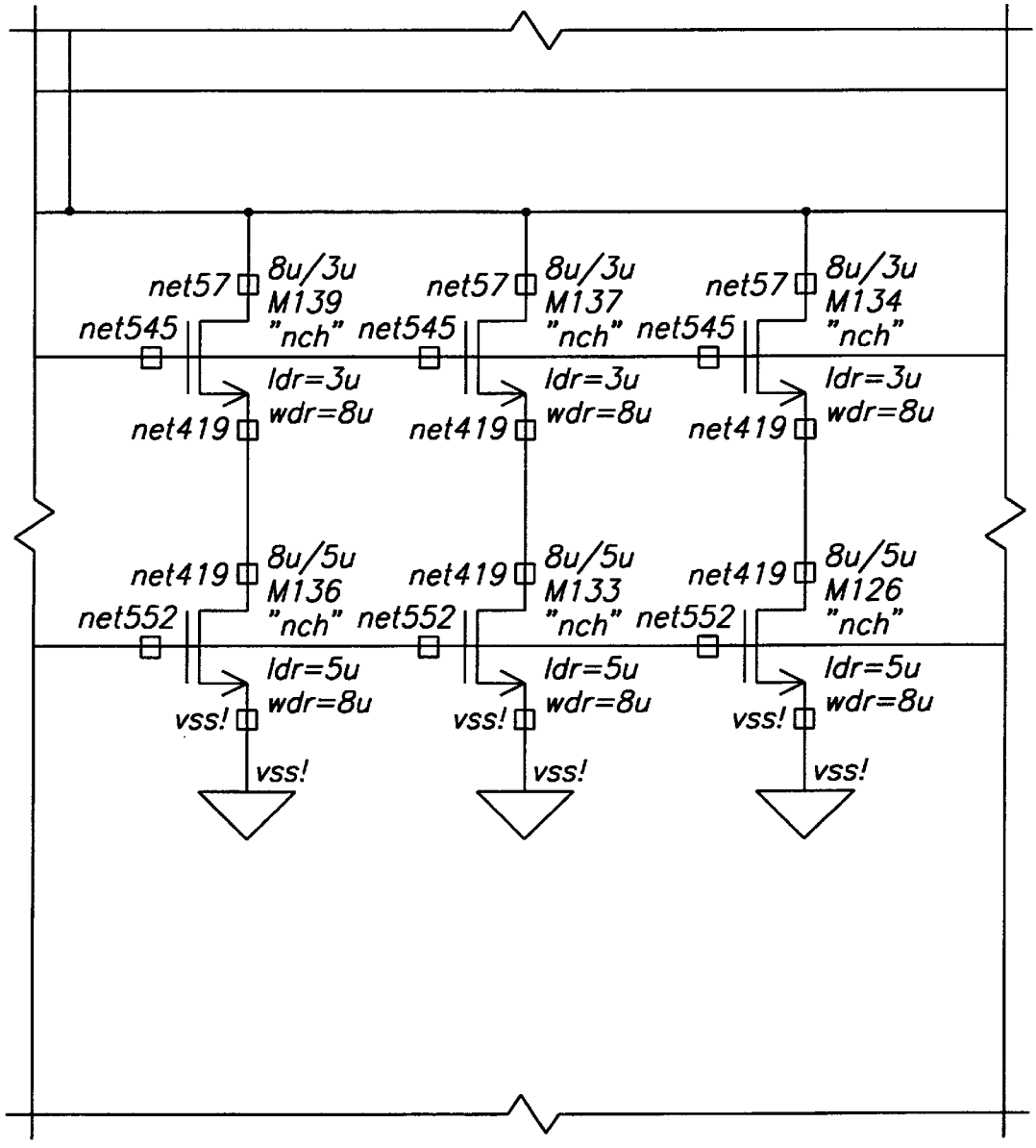


Fig 8.0110.1BF

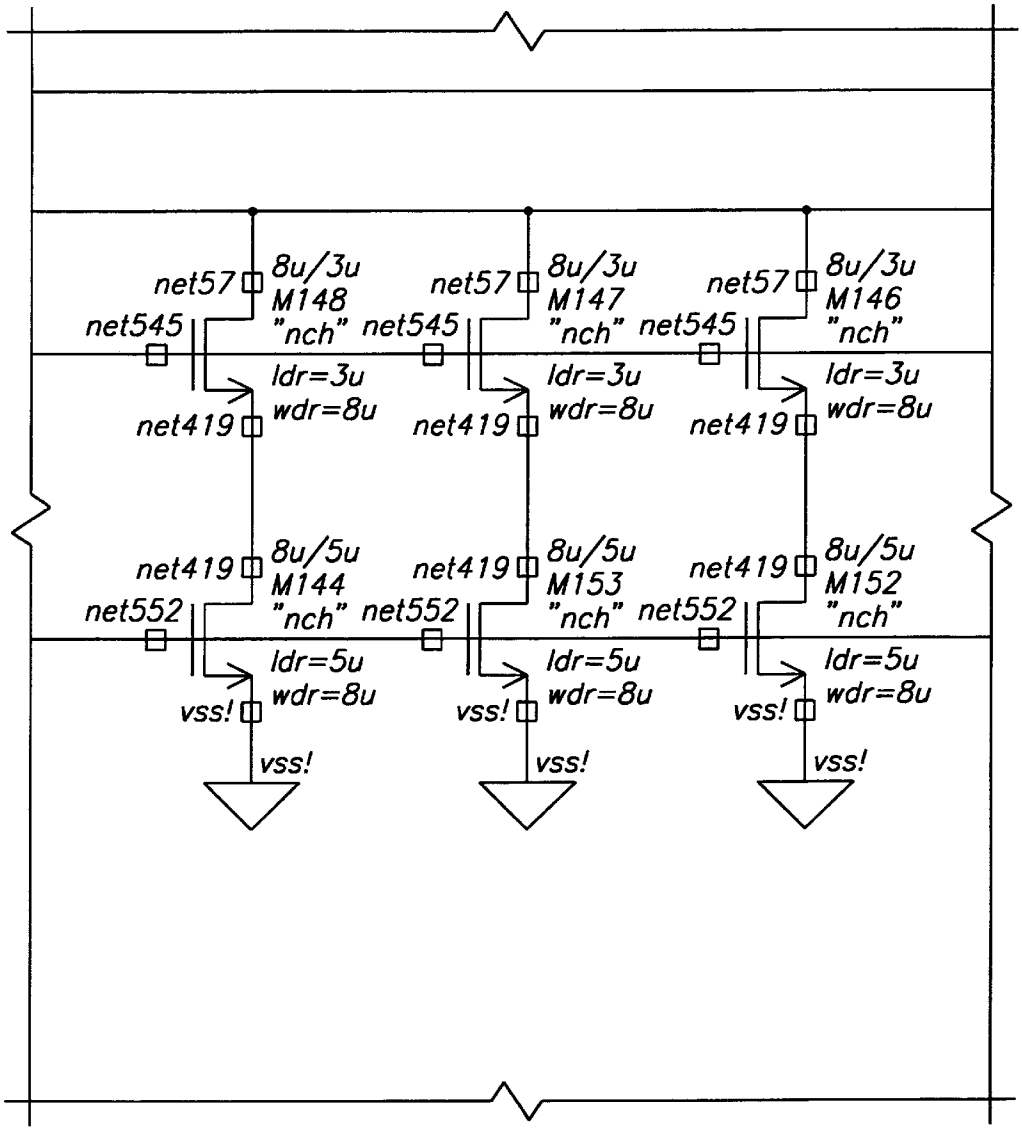
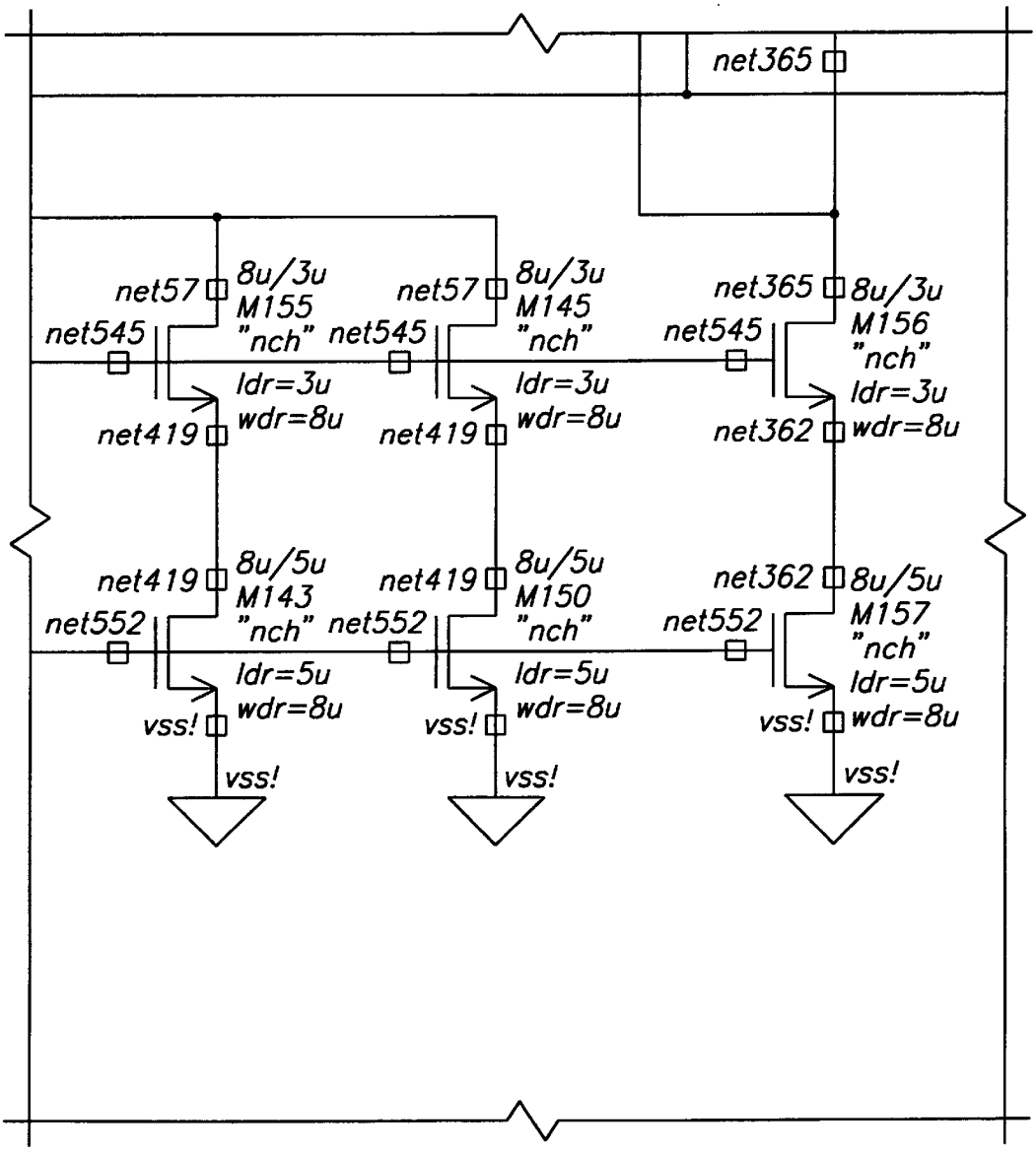

net57
8u/3u
M148
"nch"
net545
ldr=3u
wdr=8u
net419
net57
8u/3u
M147
"nch"
net545
ldr=3u
wdr=8u
net419
net57
8u/3u
M146
"nch"
net545
ldr=3u
wdr=8u
net419
net419
8u/5u
M144
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!
net419
8u/5u
M153
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!
net419
8u/5u
M152
"nch"
net552
ldr=5u
wdr=8u
vss!
vss!

Fig 8.0110B6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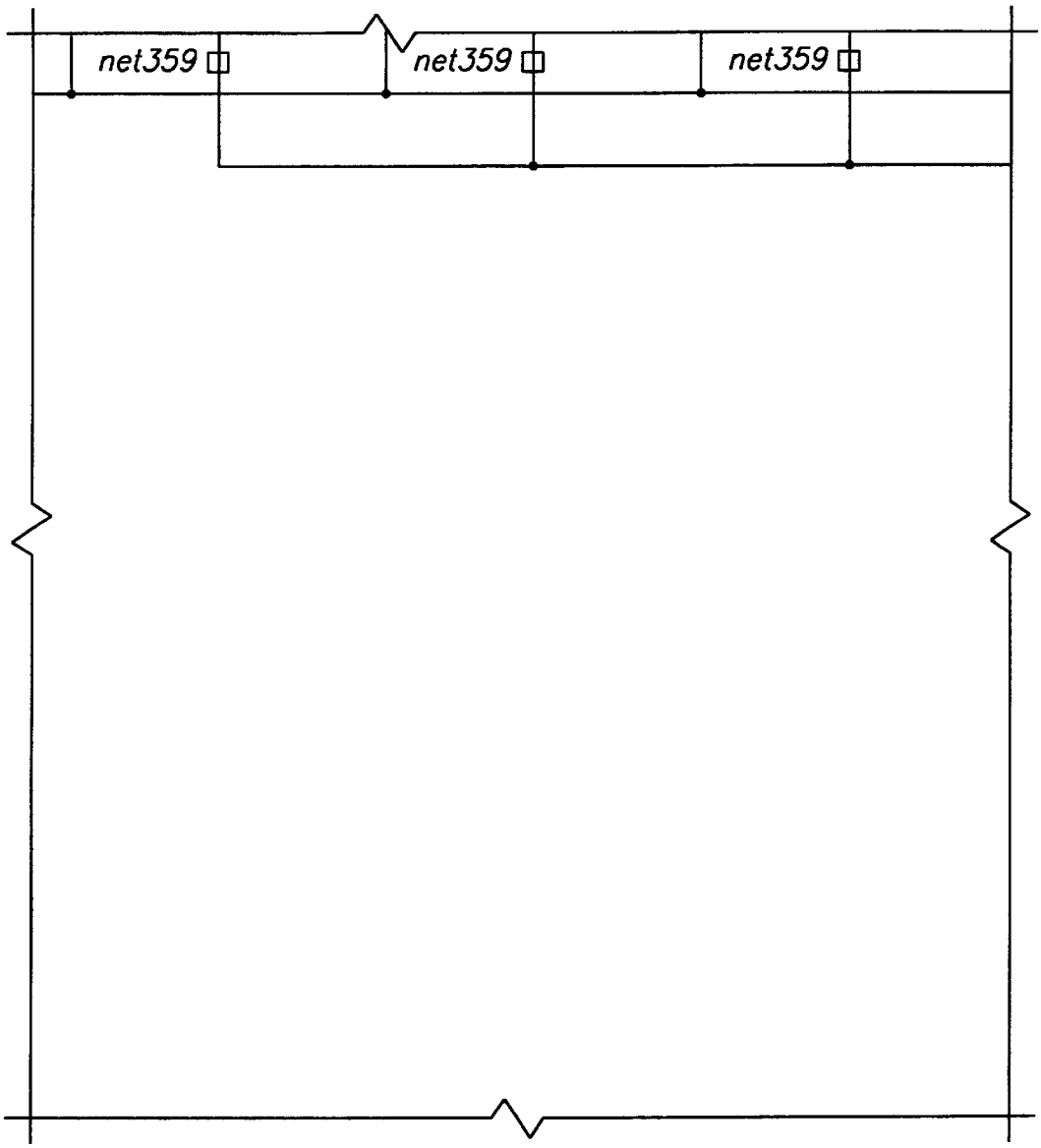
net57
8u/3u
M155
"nch"
ldr=3u
wdr=8u
net545
net419
net57
8u/3u
M145
"nch"
ldr=3u
wdr=8u
net545
net419
net365
8u/3u
M156
"nch"
ldr=3u
wdr=8u
net545
net362
net419
8u/5u
M143
"nch"
ldr=5u
wdr=8u
net552
vss!
net419
8u/5u
M150
"nch"
ldr=5u
wdr=8u
net552
vss!
net362
8u/5u
M157
"nch"
ldr=5u
wdr=8u
net552
vss!
vss!
vss!
vss!

Fig 8.0107BH


net359
net359
net359

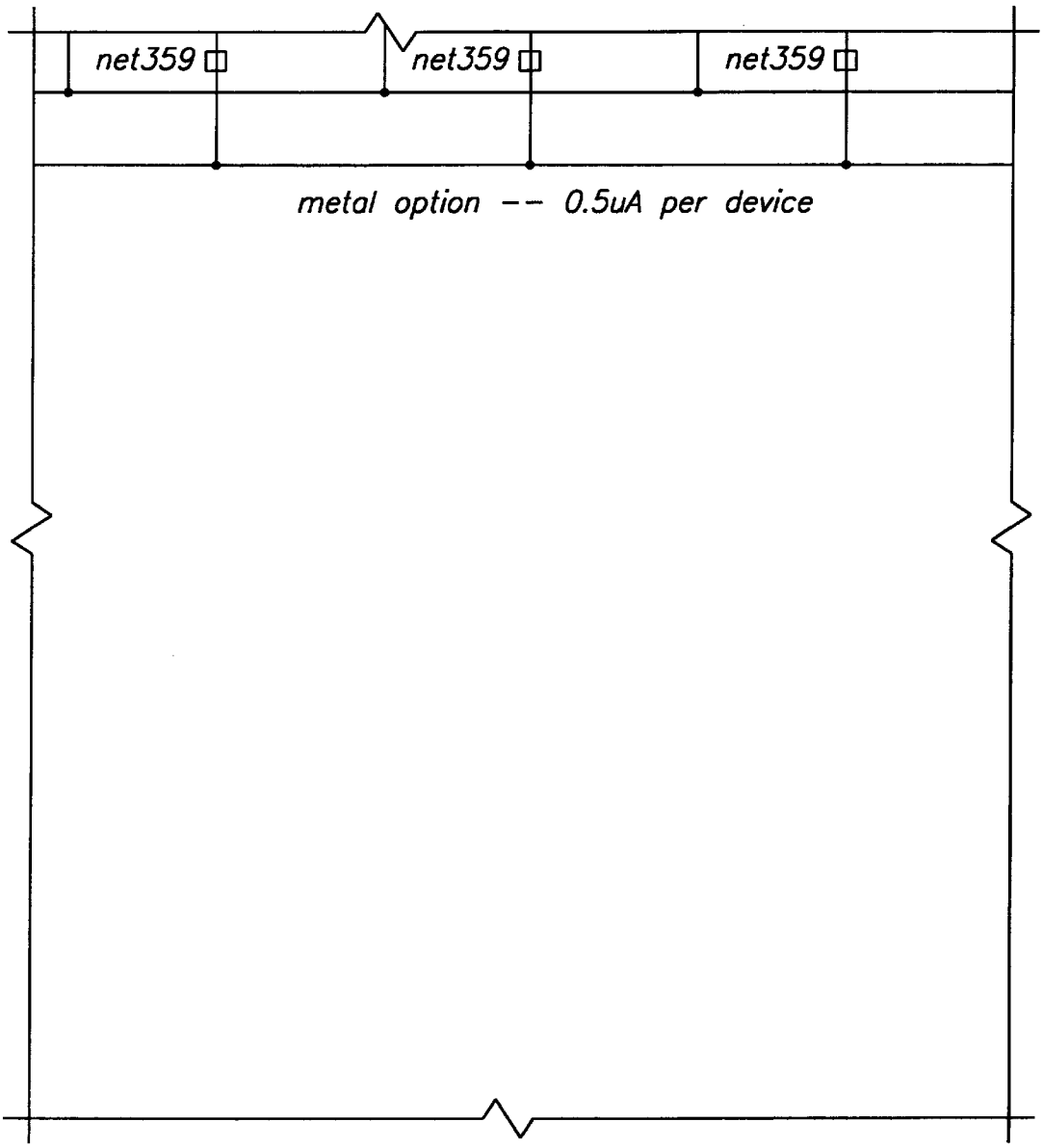


Fig 8,0107Bal

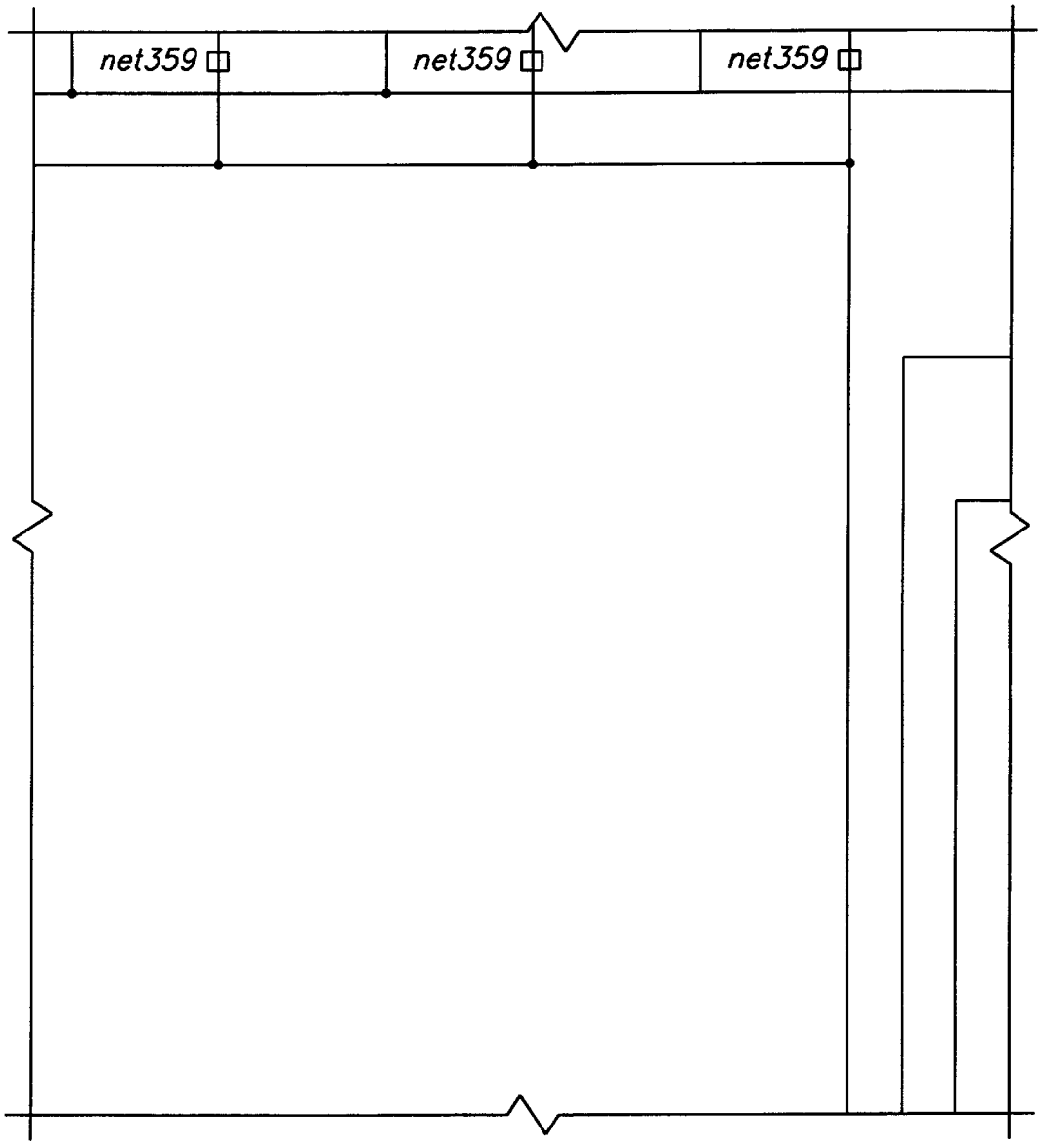


Fig 8.0107BK

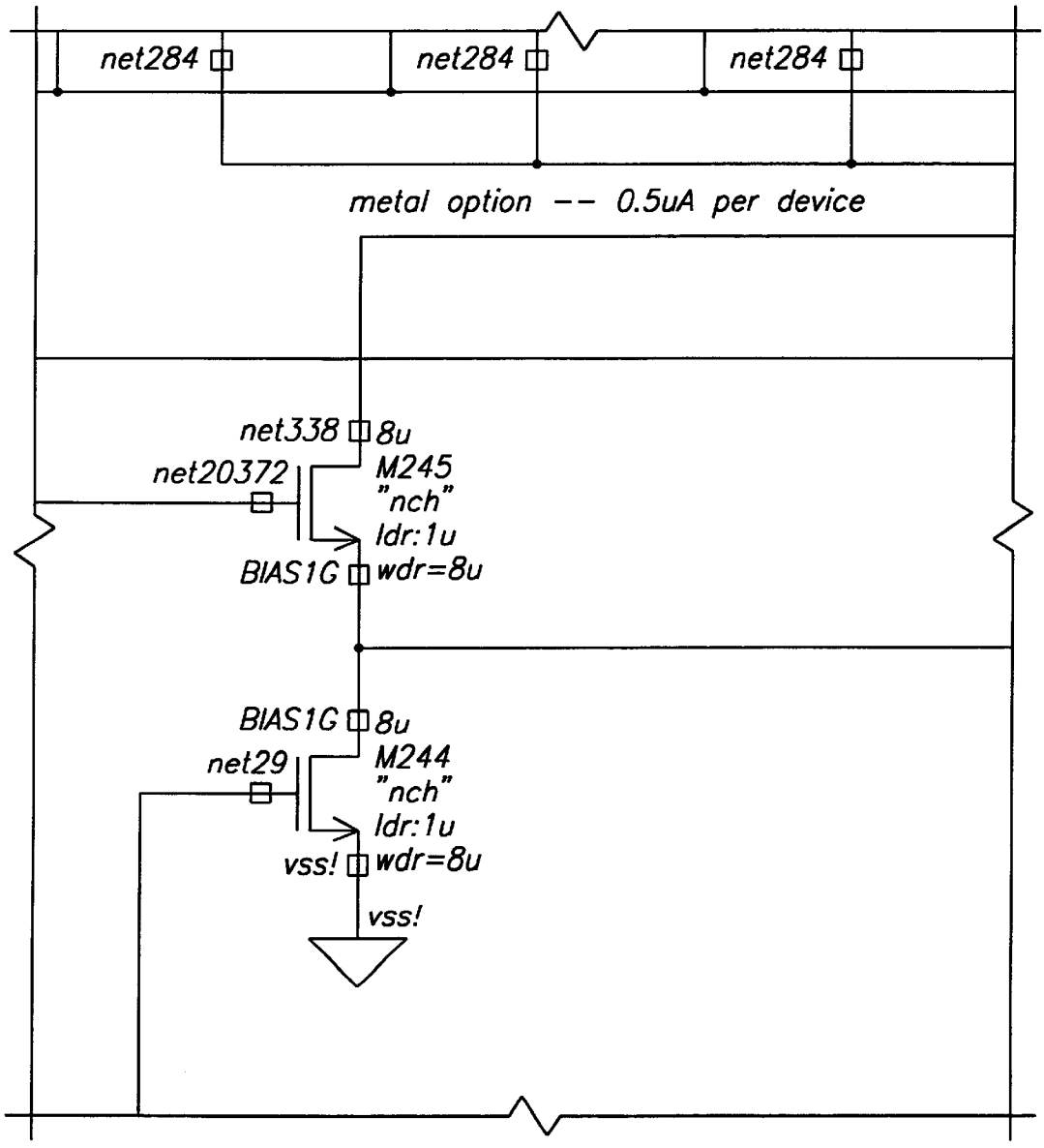

net284
net284
net284
metal option -- 0.5uA per device
net338
8u
net20372
M245
"nch"
ldr:1u
BIAS1G
wdr=8u
BIAS1G
8u
net29
M244
"nch"
ldr:1u
vss!
wdr=8u
vss!

Fig 8.0107BL

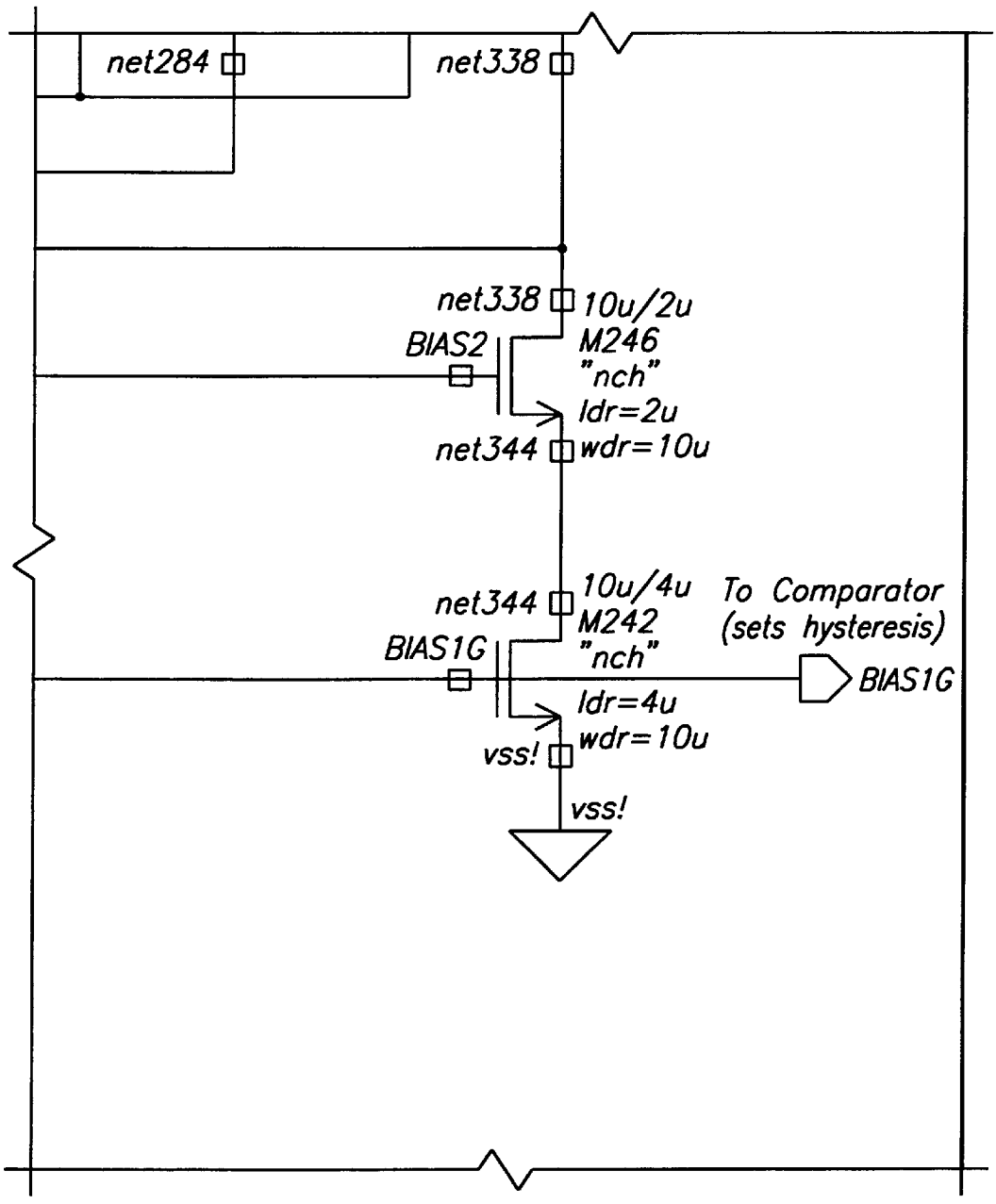

net284
net338
net338
10u/2u
BIAS2
M246
"nch"
ldr=2u
net344
wdr=10u
net344
10u/4u
M242
"nch"
To Comparator
(sets hysteresis)
BIAS1G
BIAS1G
ldr=4u
wdr=10u
vss!
vss!

Fig 8.0107BM

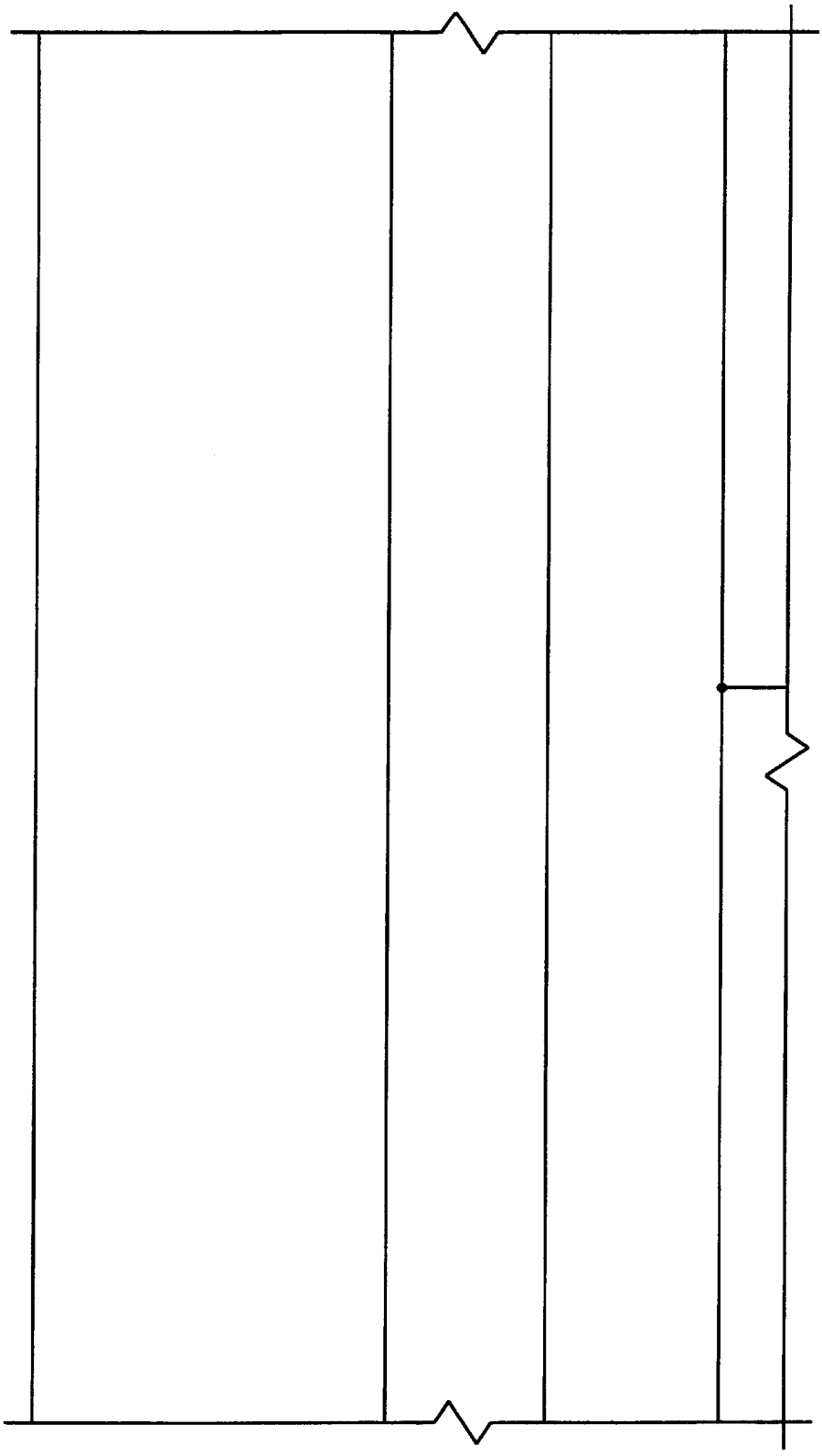


Fig 8.0110A

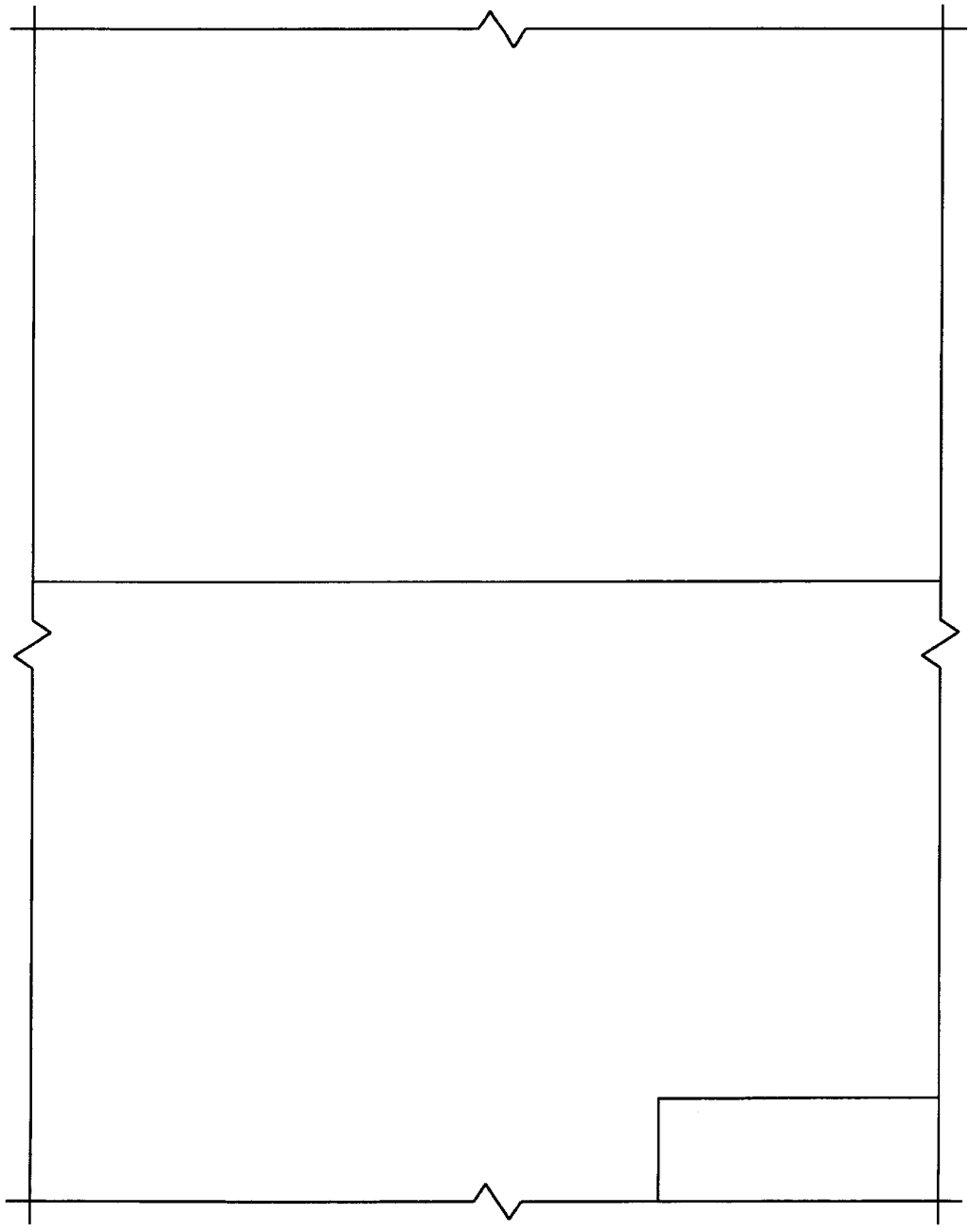


Fig 8.01076B

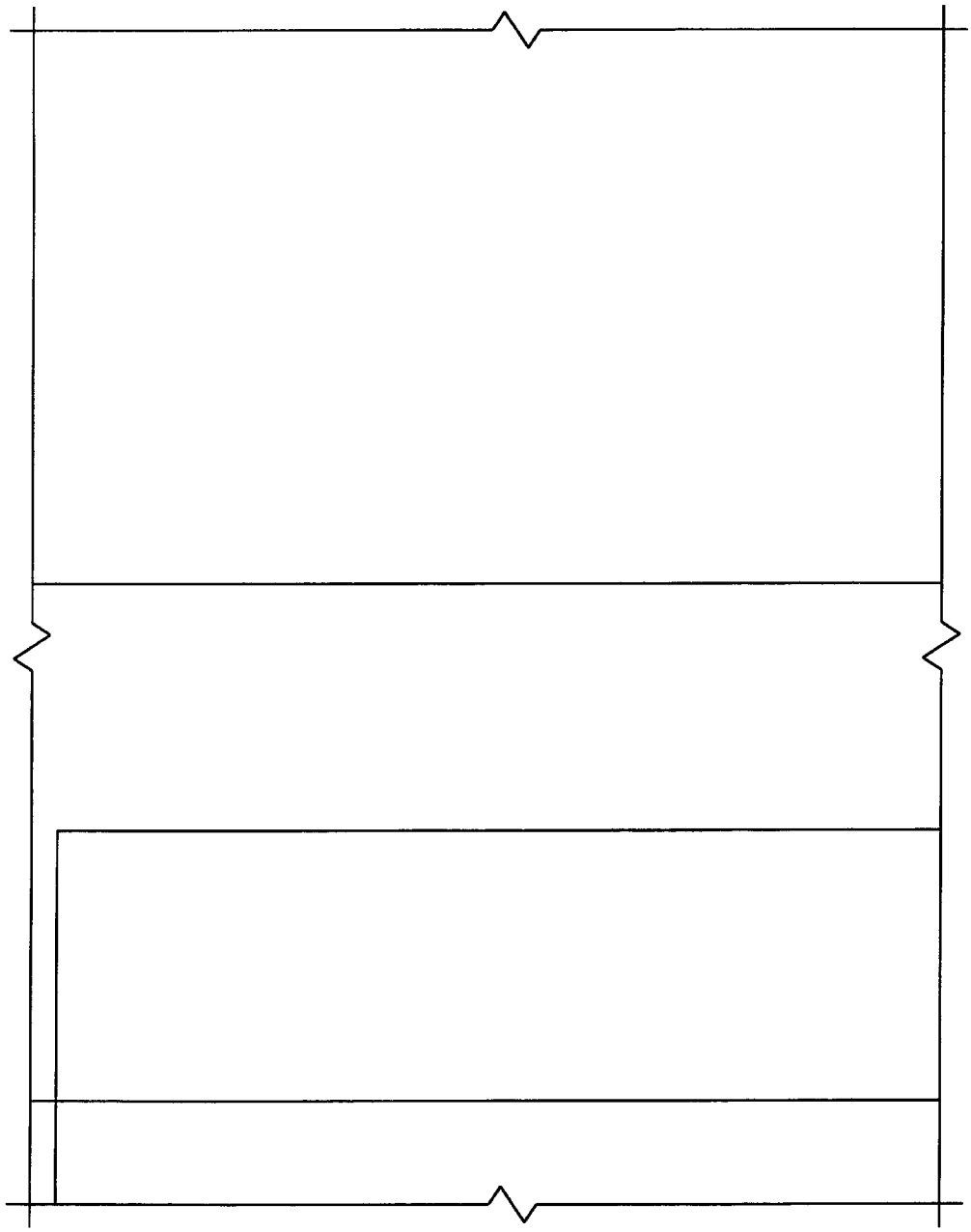


Fig 8.01071CC

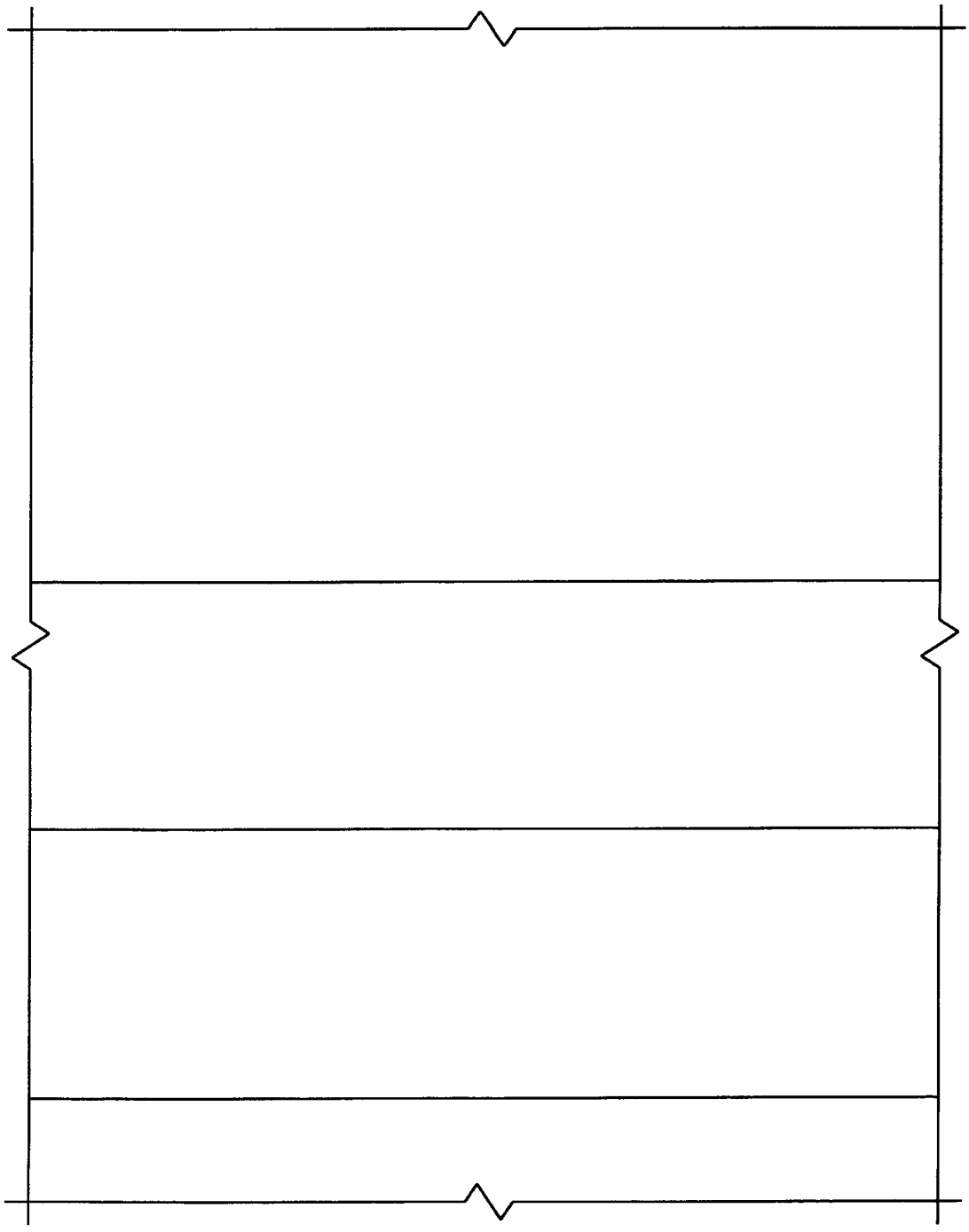


Fig 80107CD

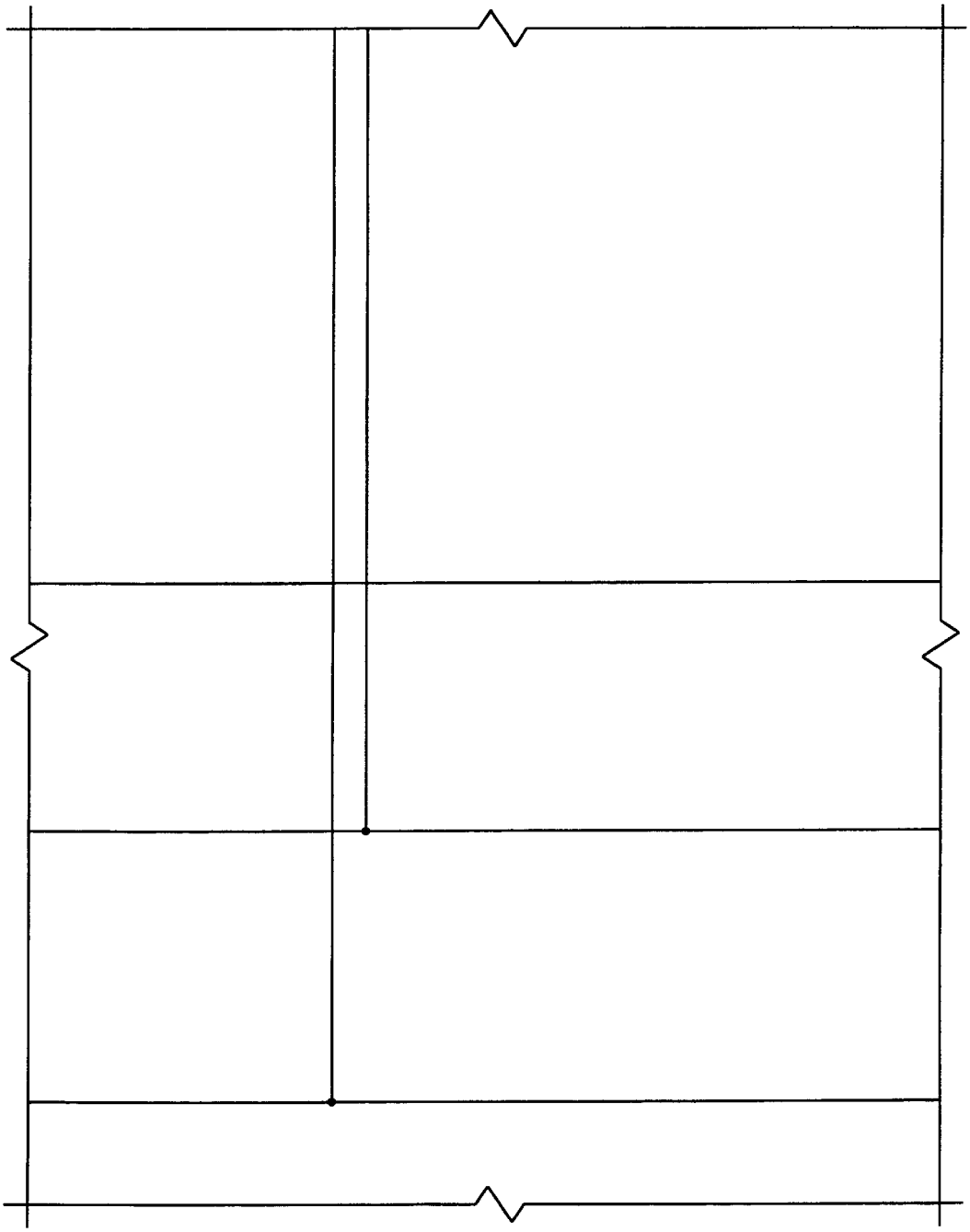


Fig 8.01071CE

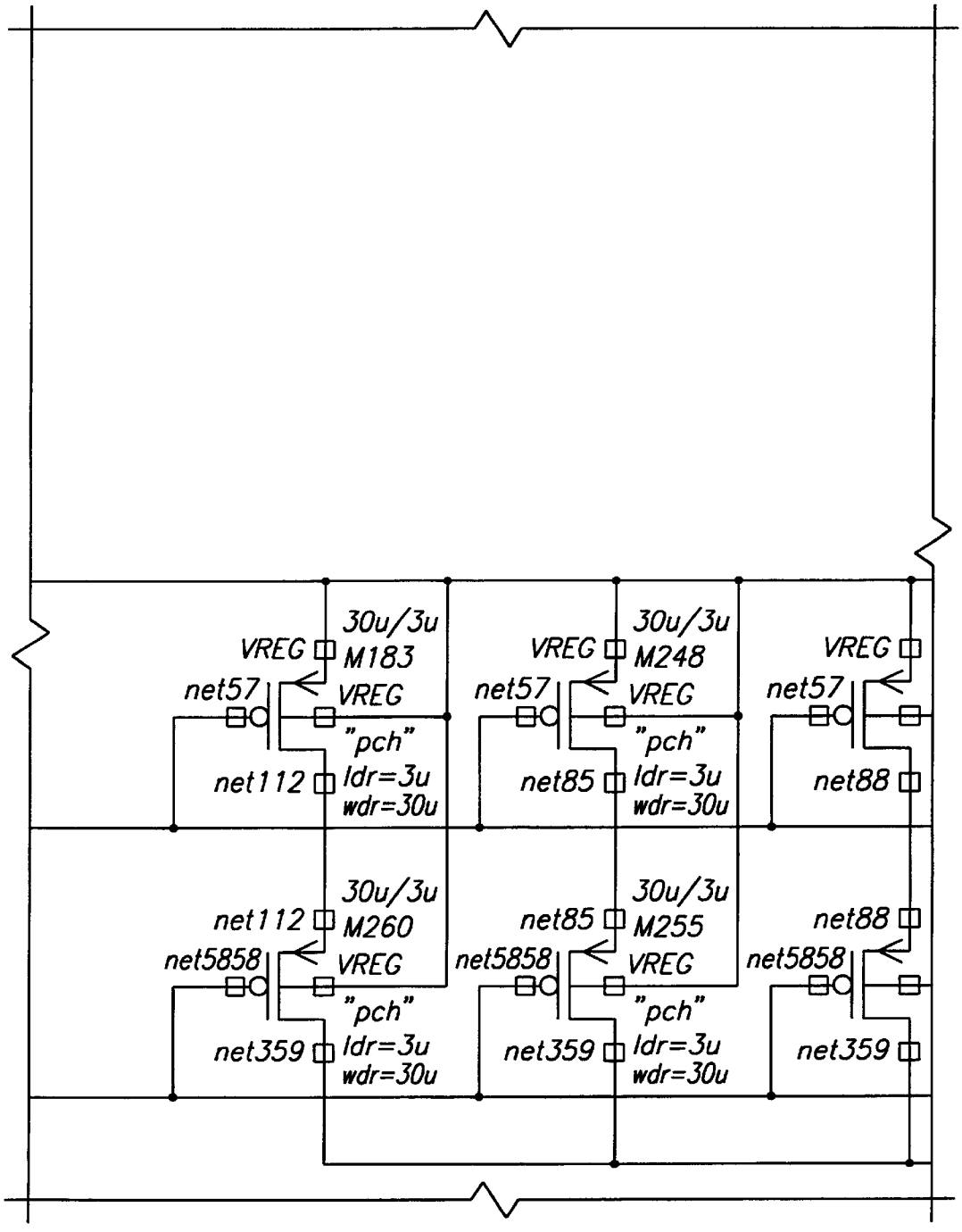


FIG 8B.0110CF

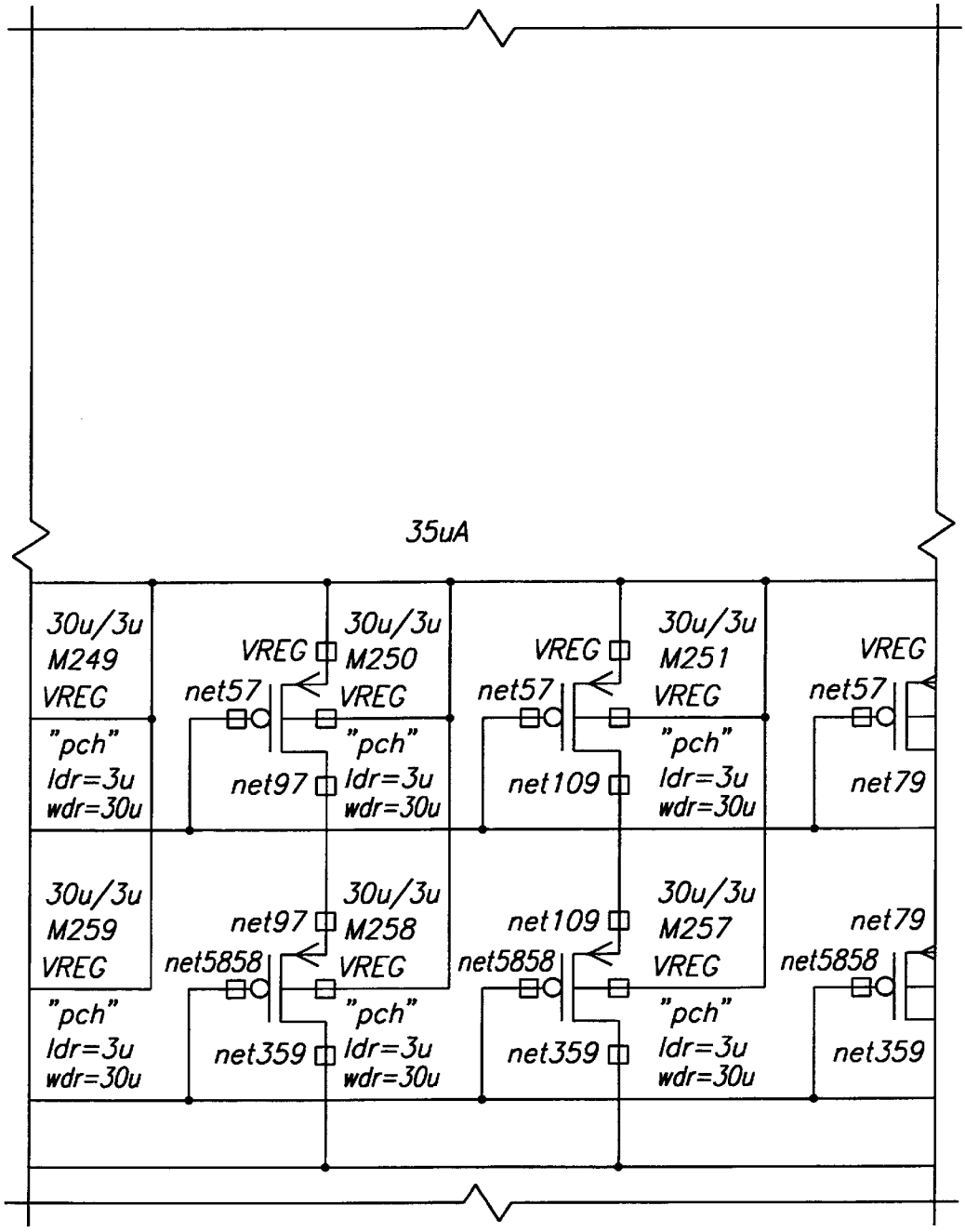


Fig 8.0110116

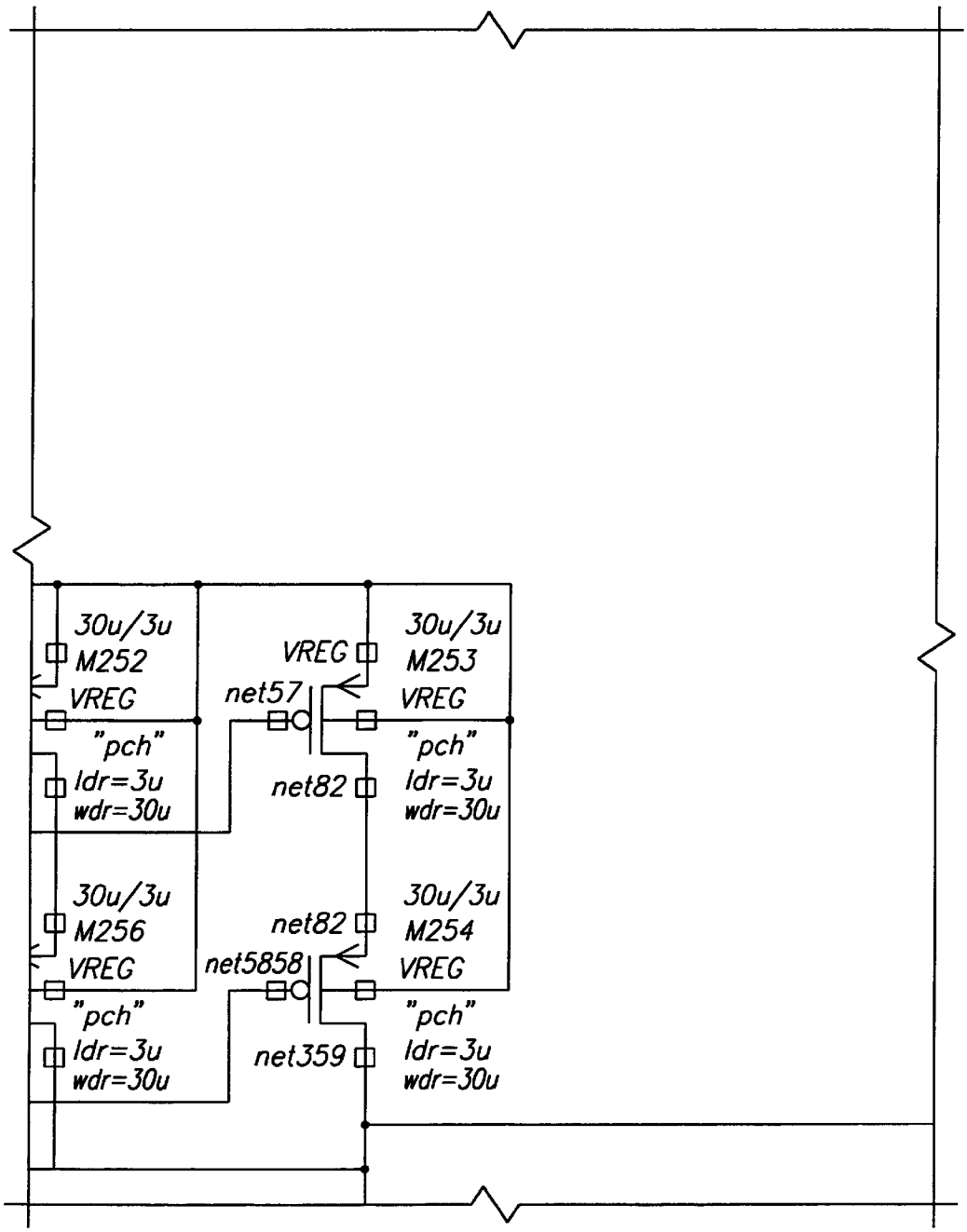


Fig 88.0110CH

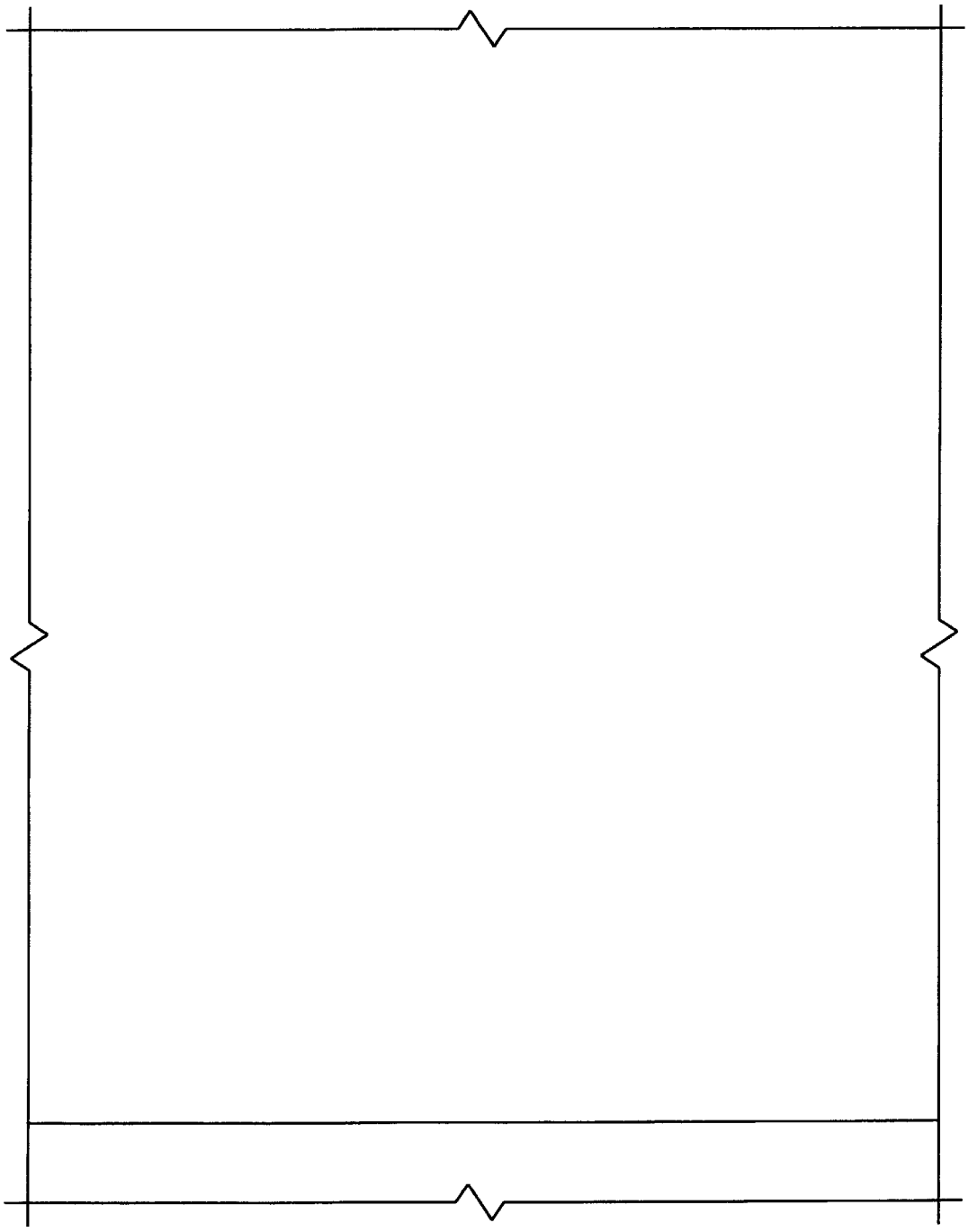


Fig 8.01071

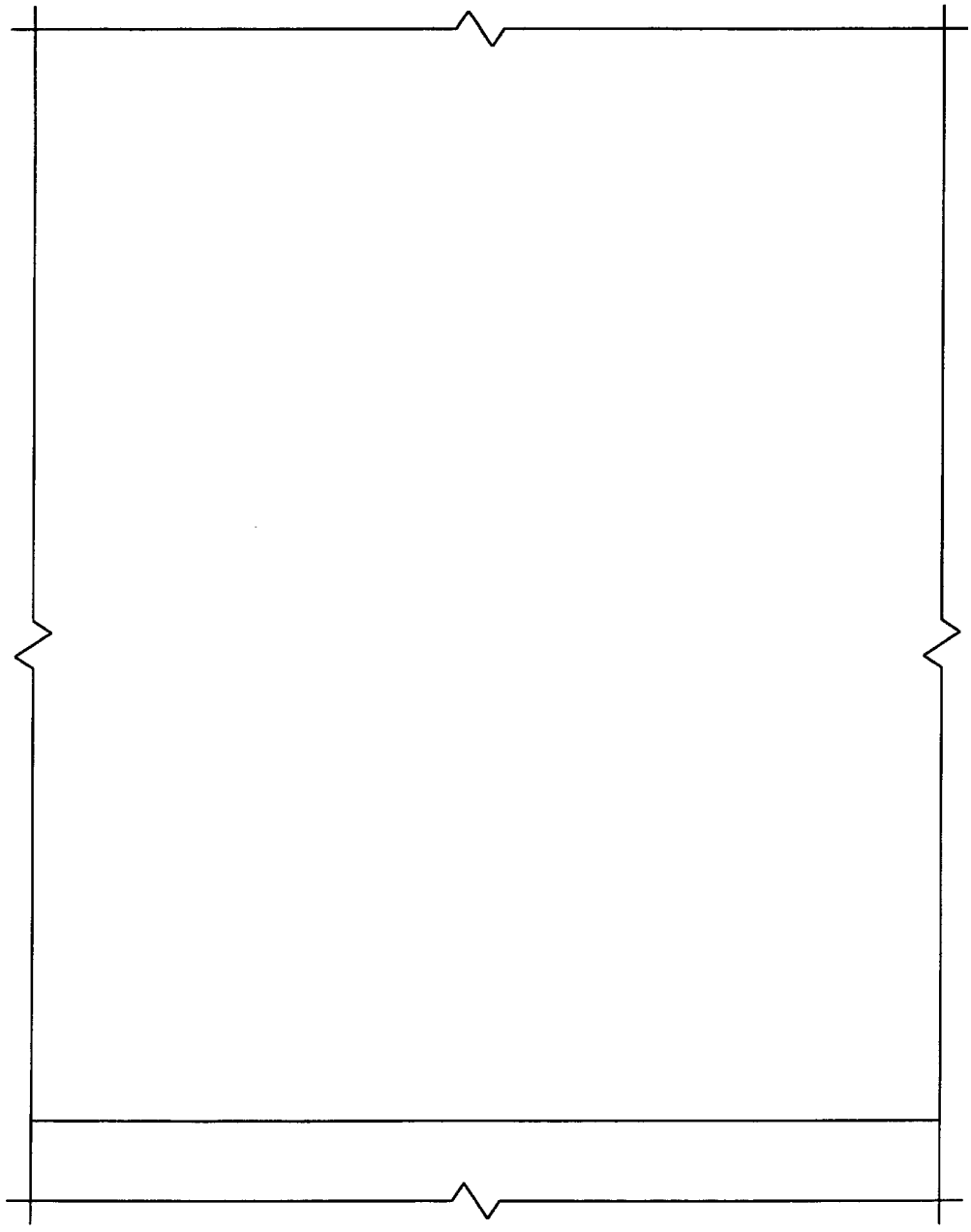


Fig. 8,010,710

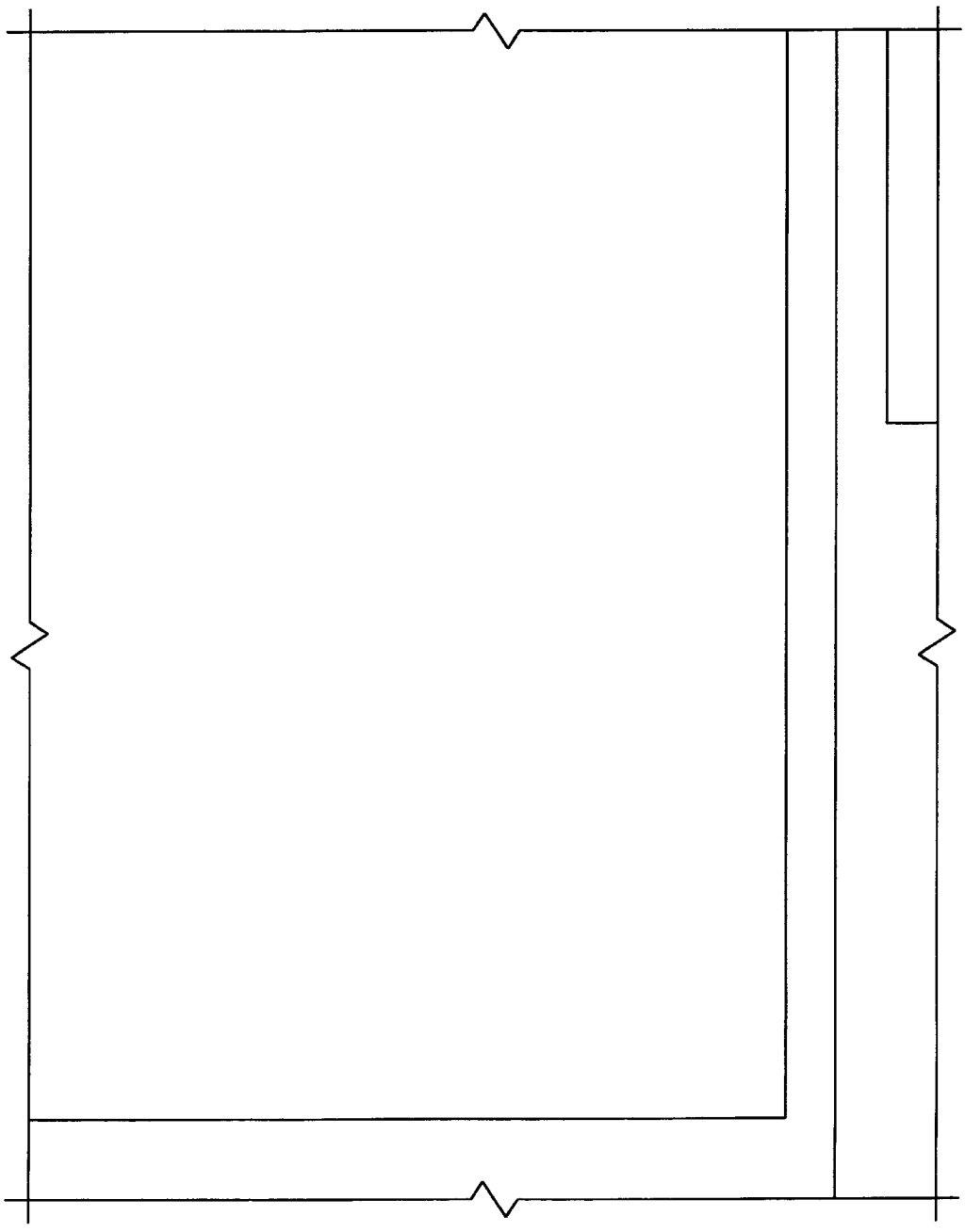


Fig 8.01076

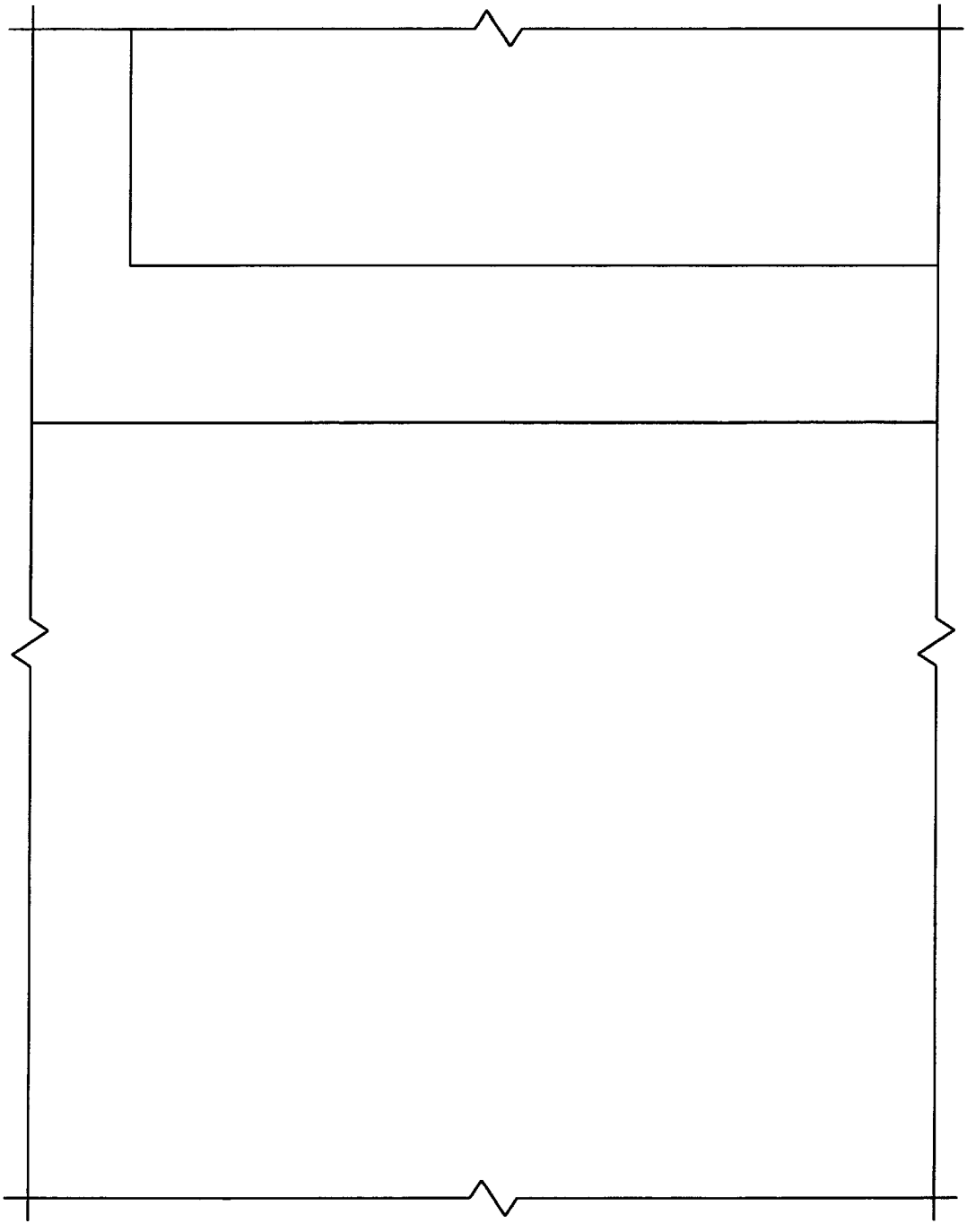


Fig 8.0107CL

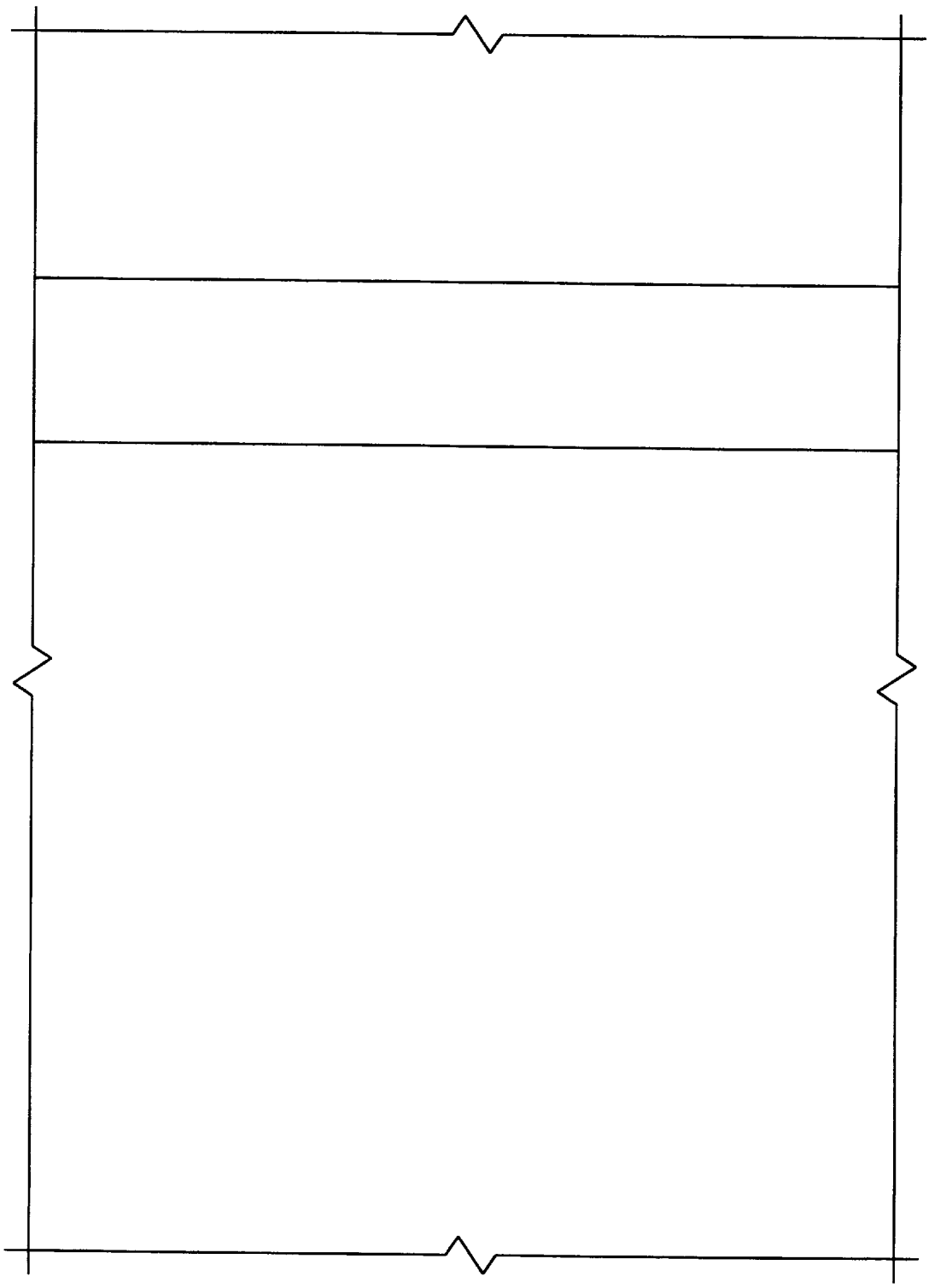


Fig 8.0107CM

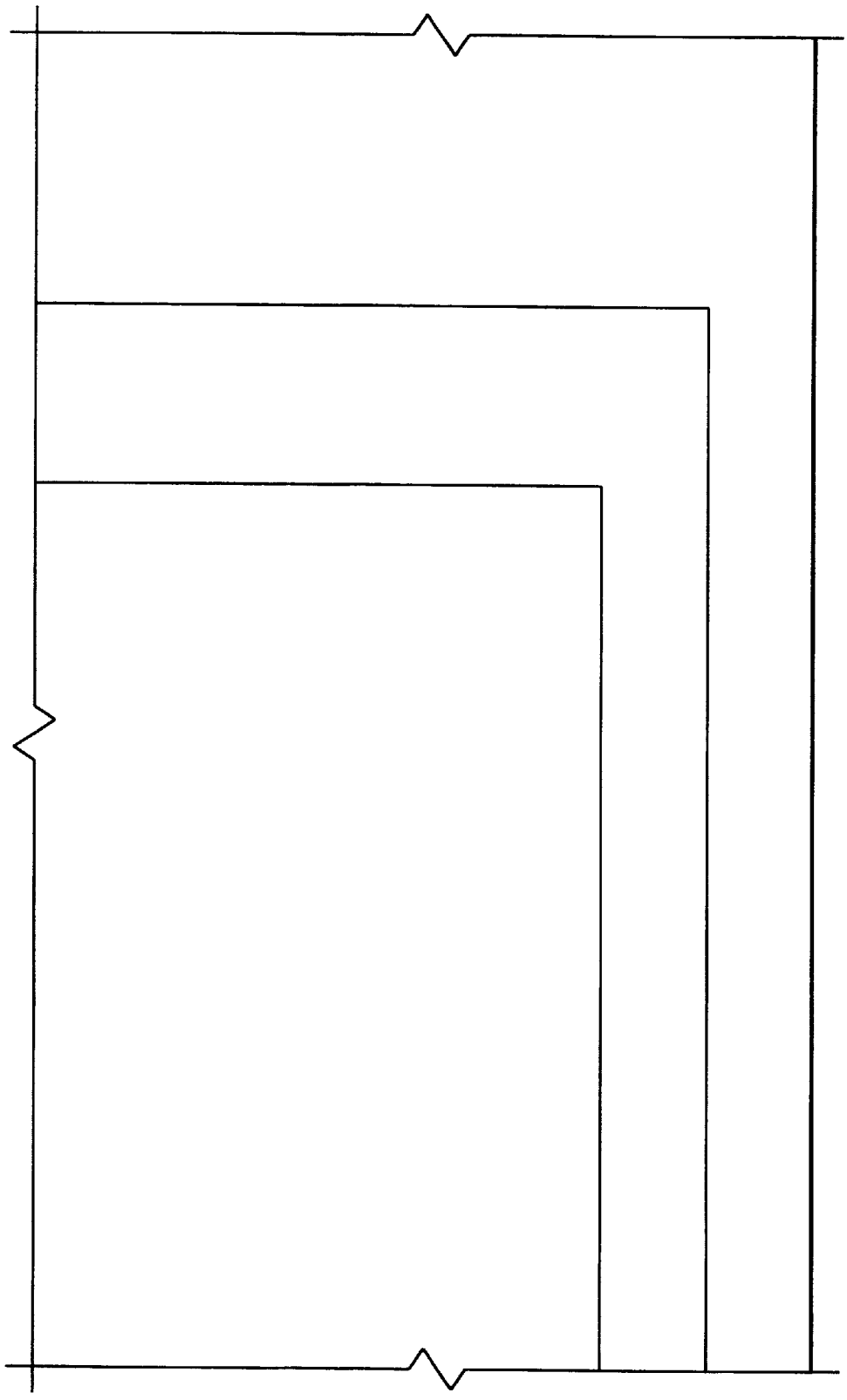


Fig 8.0107CN

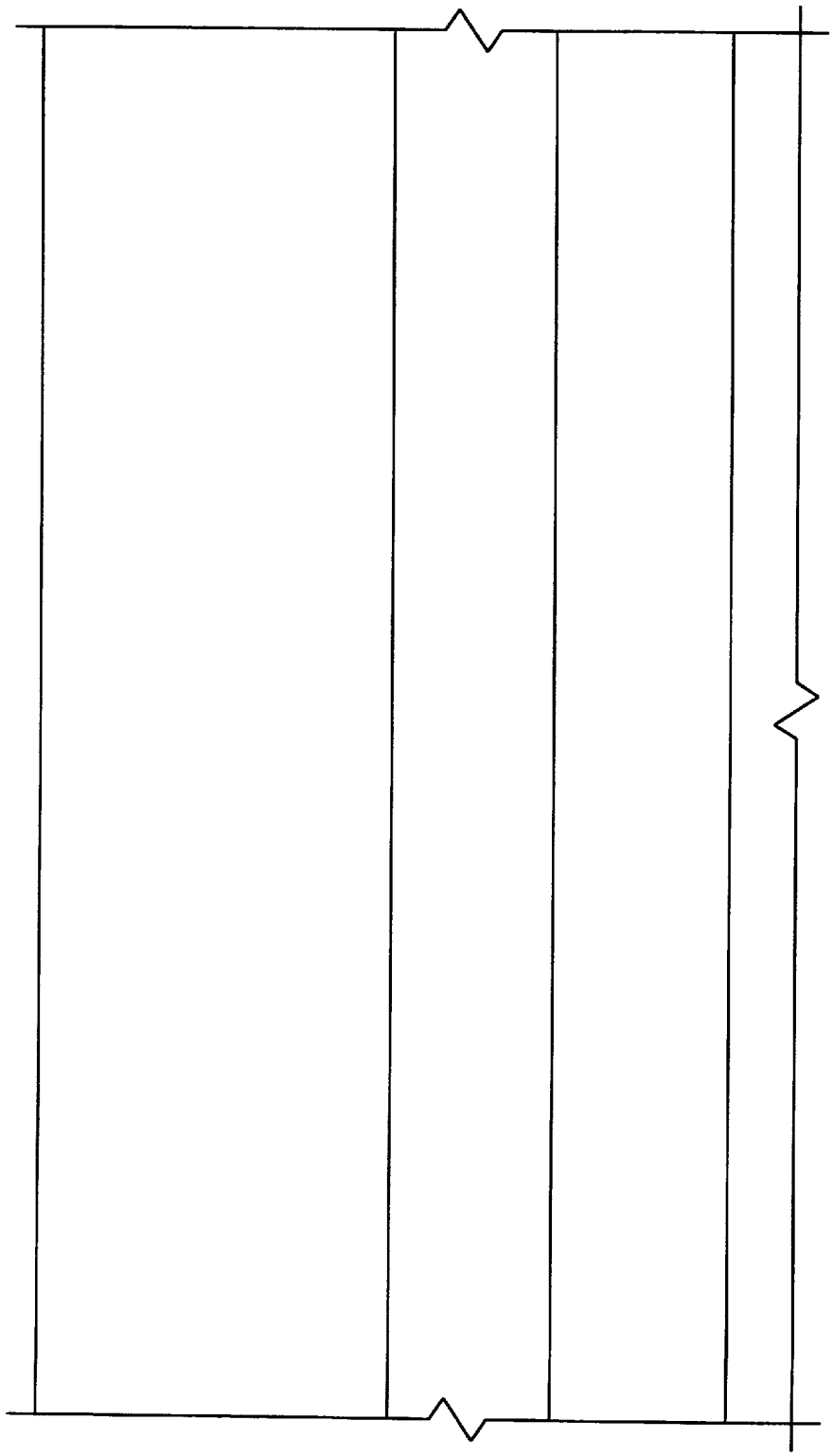


Fig 8.0107DA

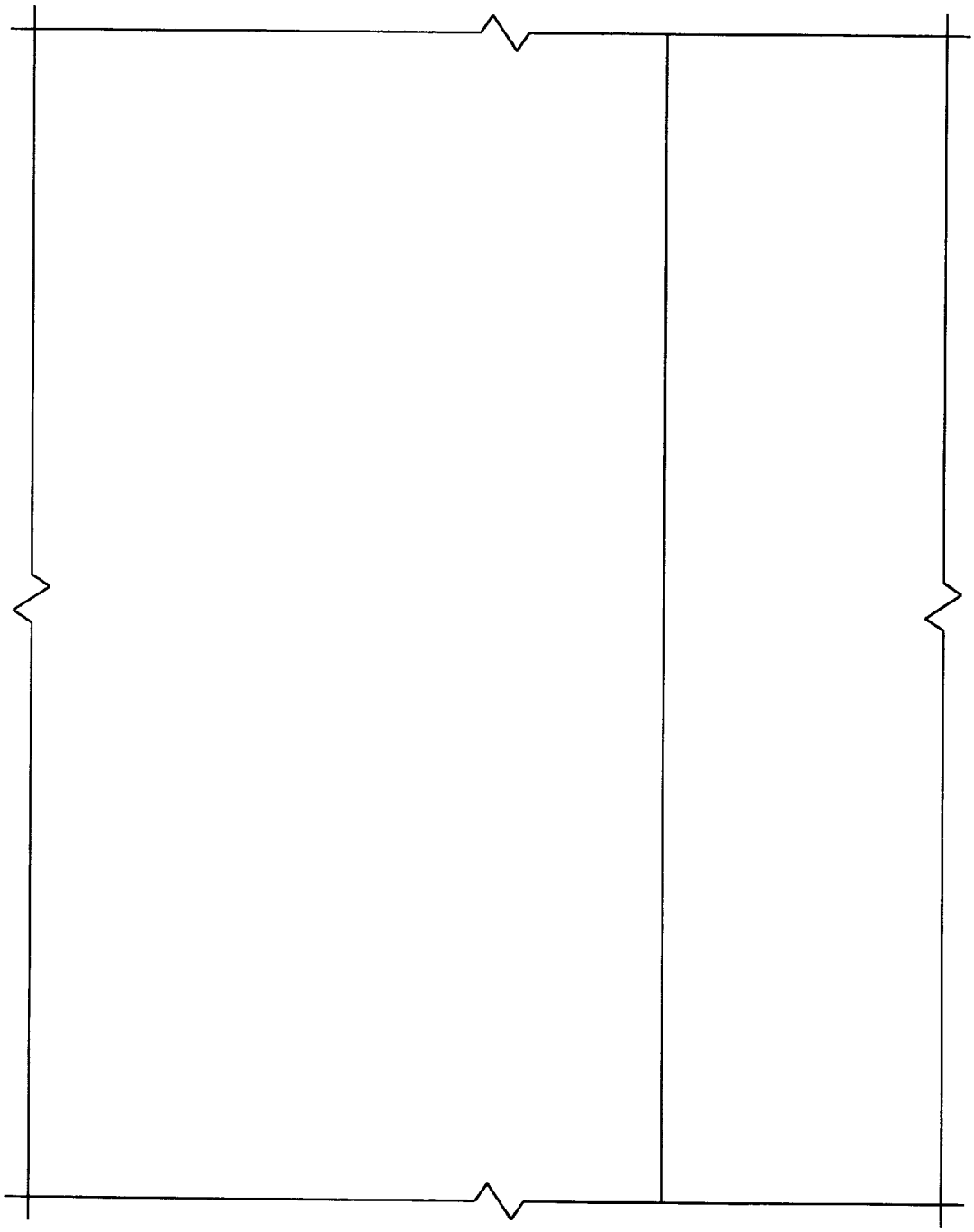


FIG 8.01078

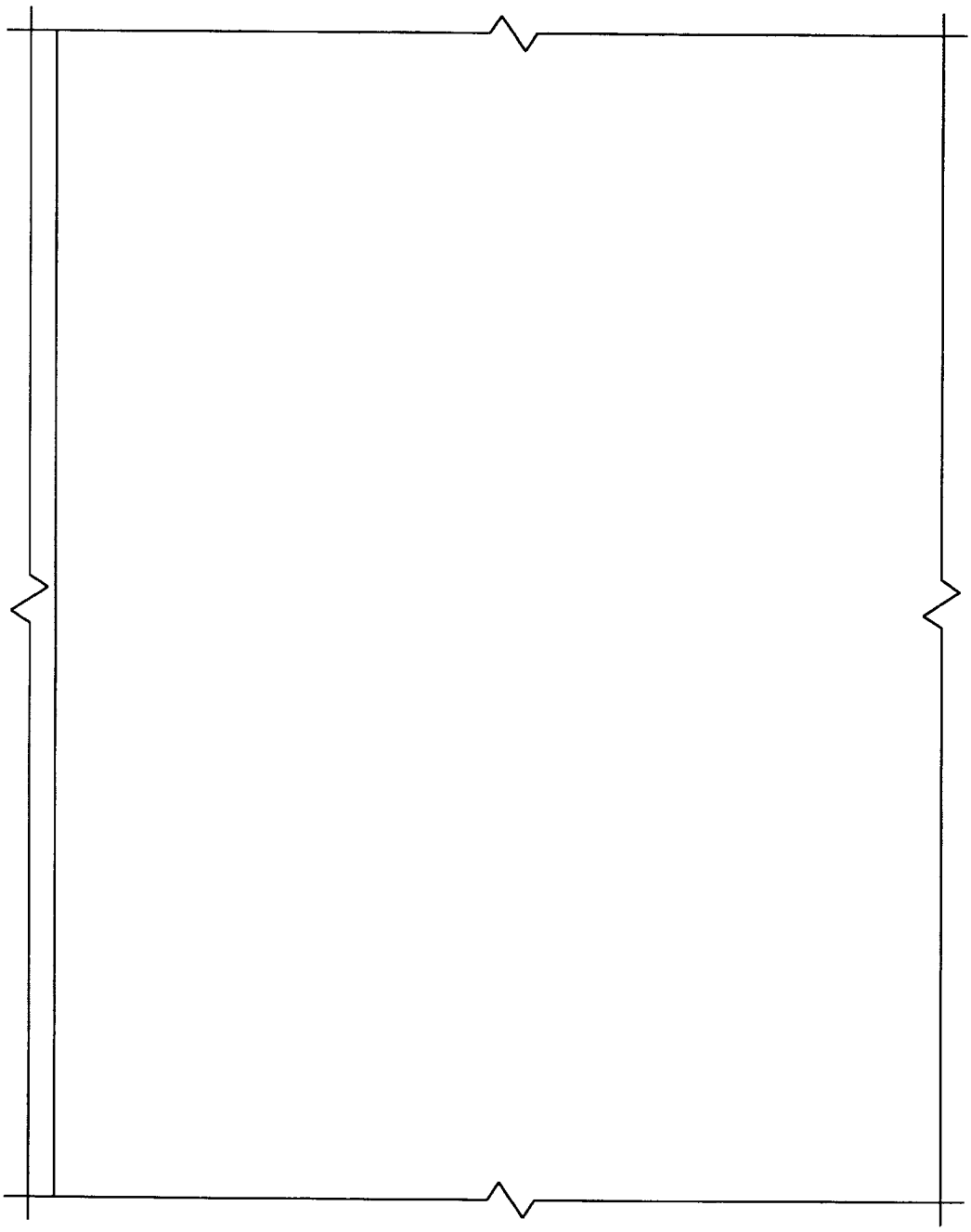


Fig 8.01070C

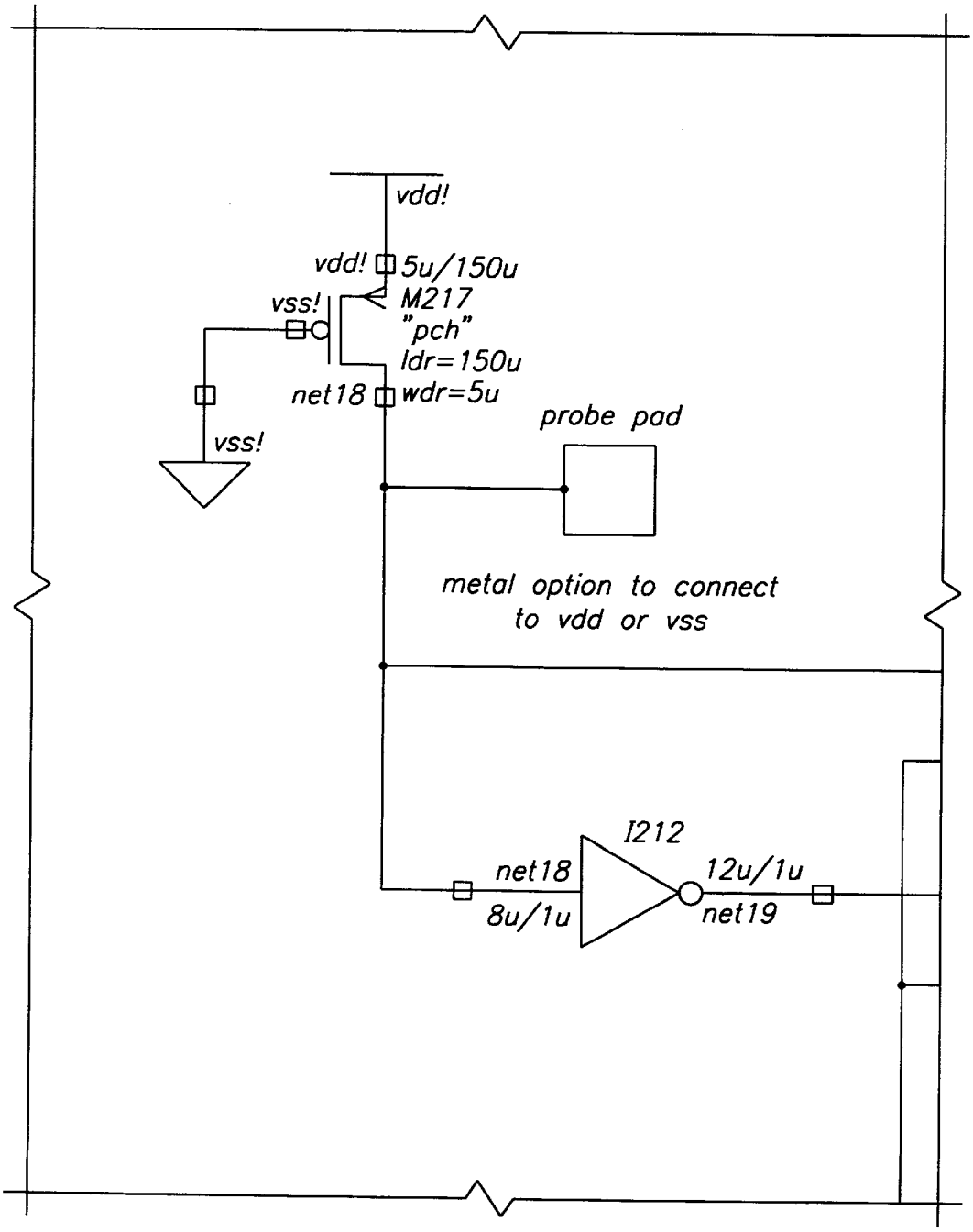

vdd!
vdd!
5u/150u
M217
"pch"
ldr=150u
wdr=5u
vss!
net18
vss!
probe pad
metal option to connect
to vdd or vss
I212
net18
8u/1u
12u/1u
net19

Fig 8,010,100

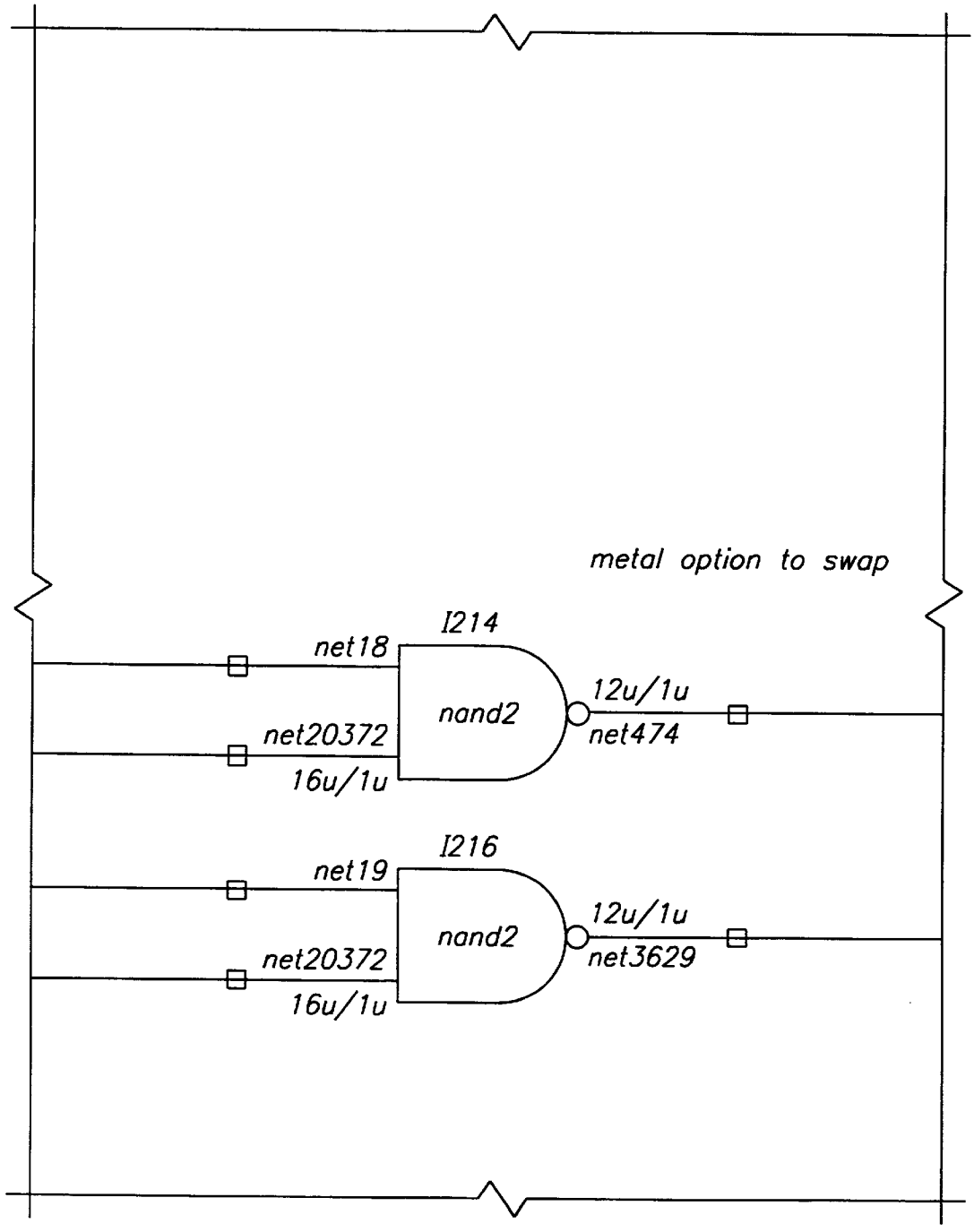

metal option to swap
I214
net18
net20372
16u/1u
nand2
12u/1u
net474
I216
net19
net20372
16u/1u
nand2
12u/1u
net3629

Fig 80108DE

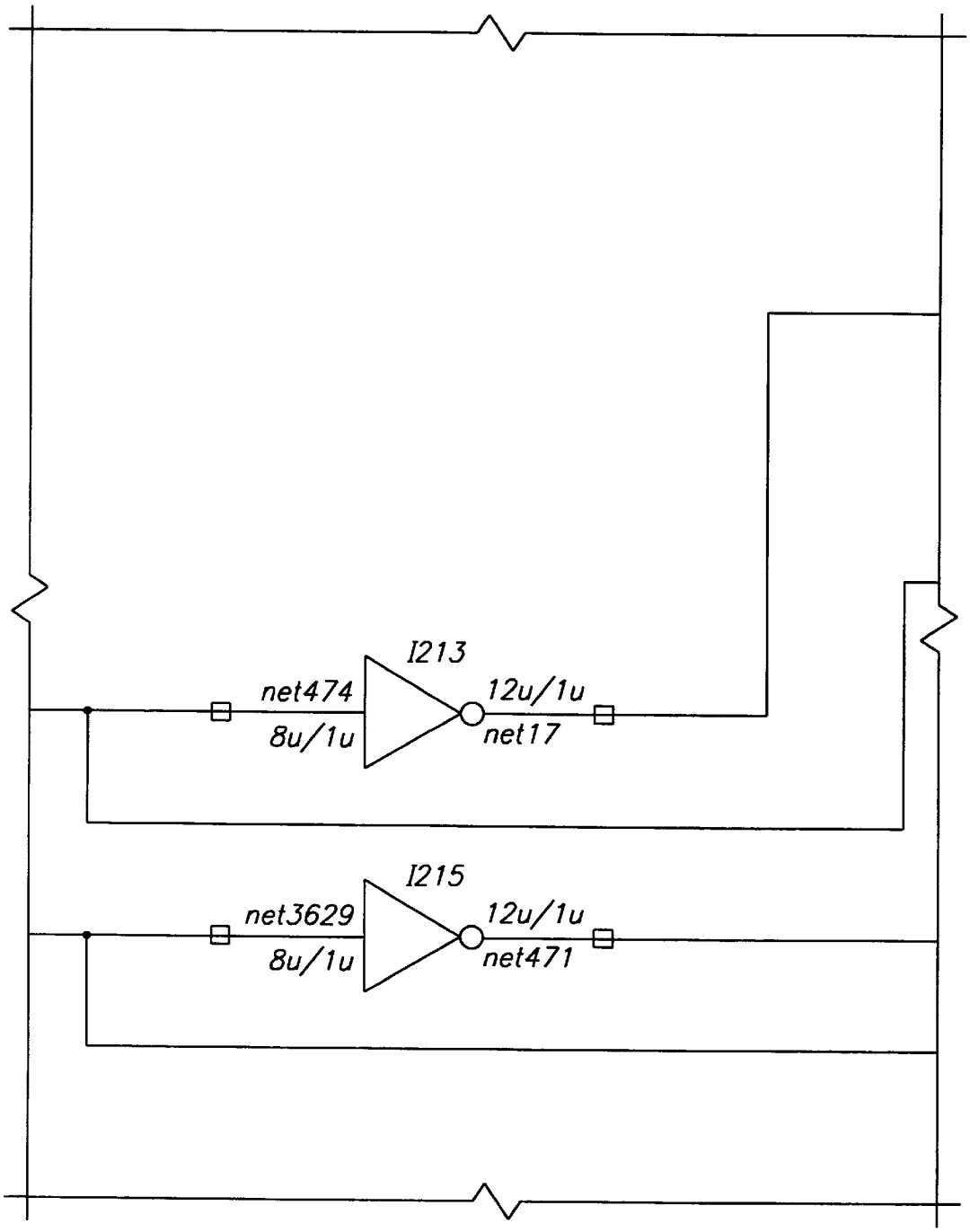


Fig 8B1071DF

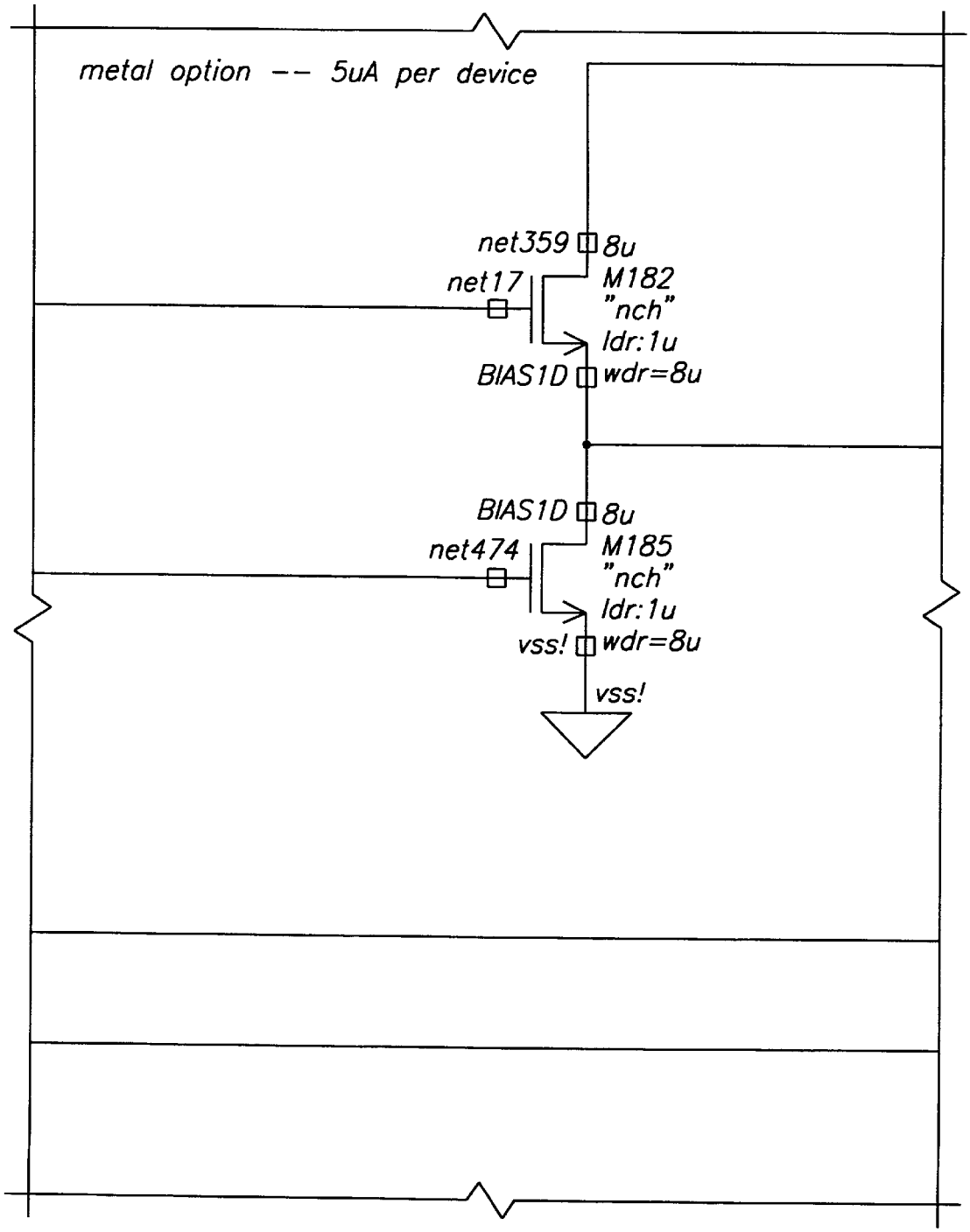
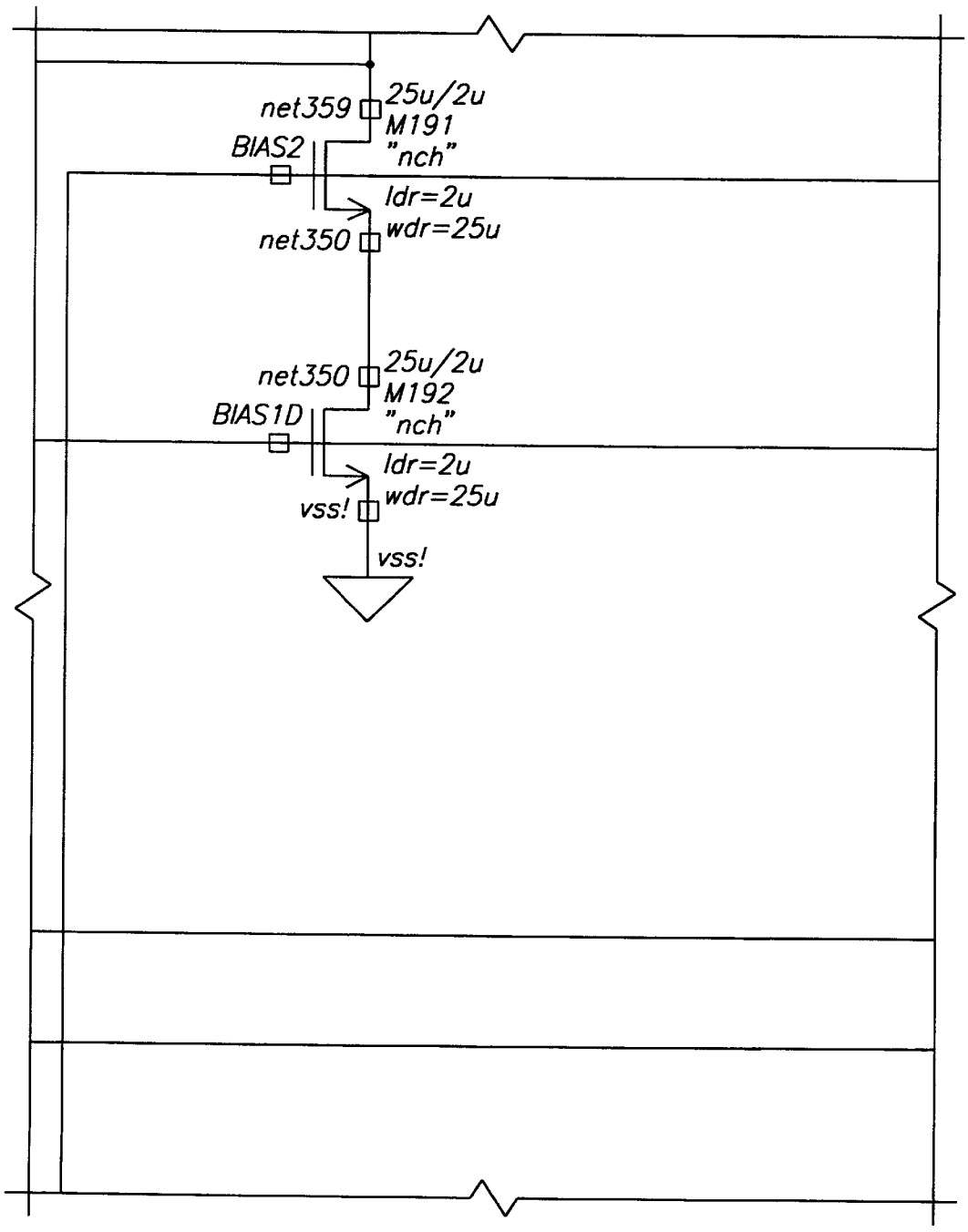


Fig 80107106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M191
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BIAS2
ldr=2u
wdr=25u
net350
net350
25u/2u
M192
"nch"
BIAS1D
ldr=2u
wdr=25u
vss!
vss!

Fig 8.0107DH

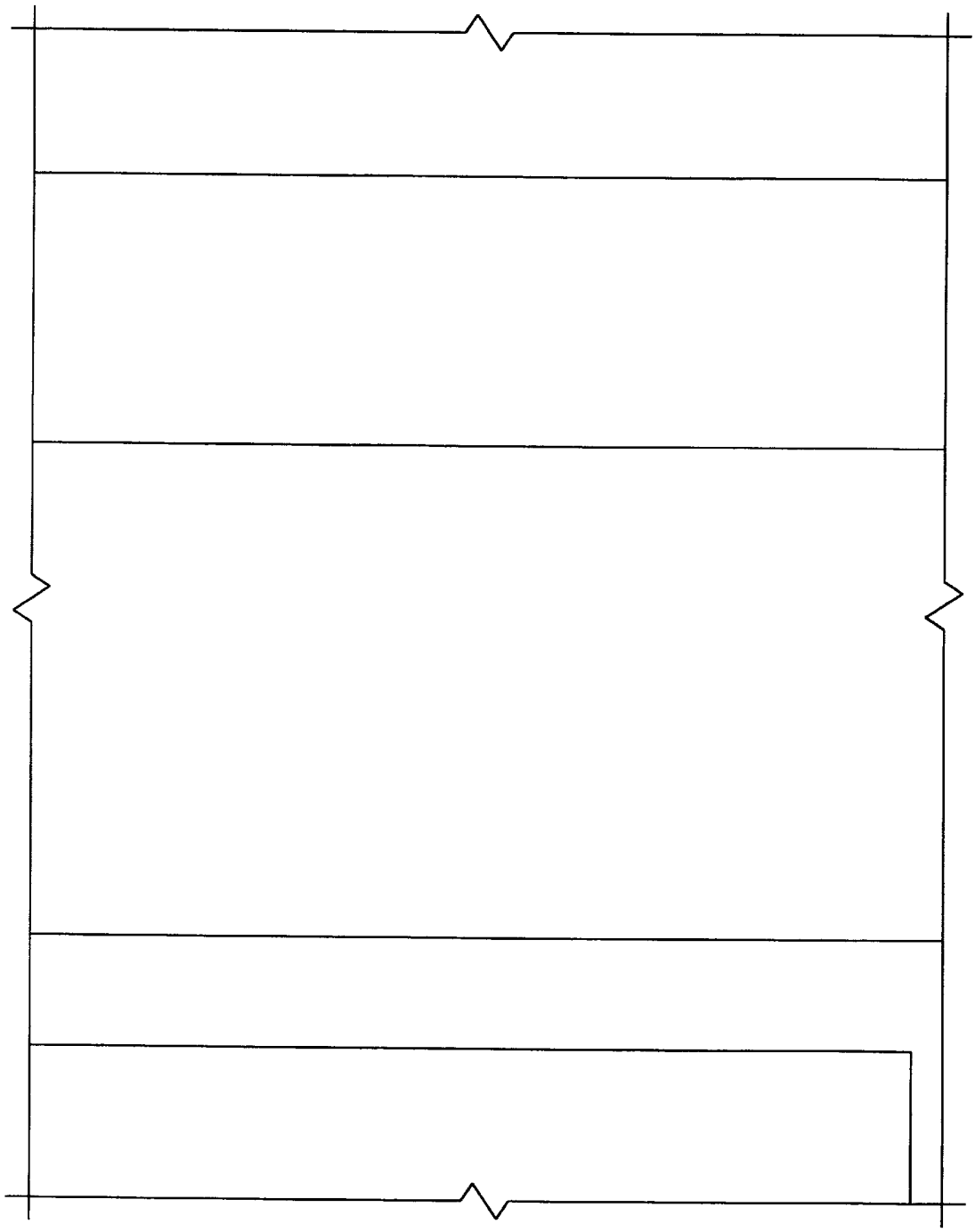


Fig 8.0110101

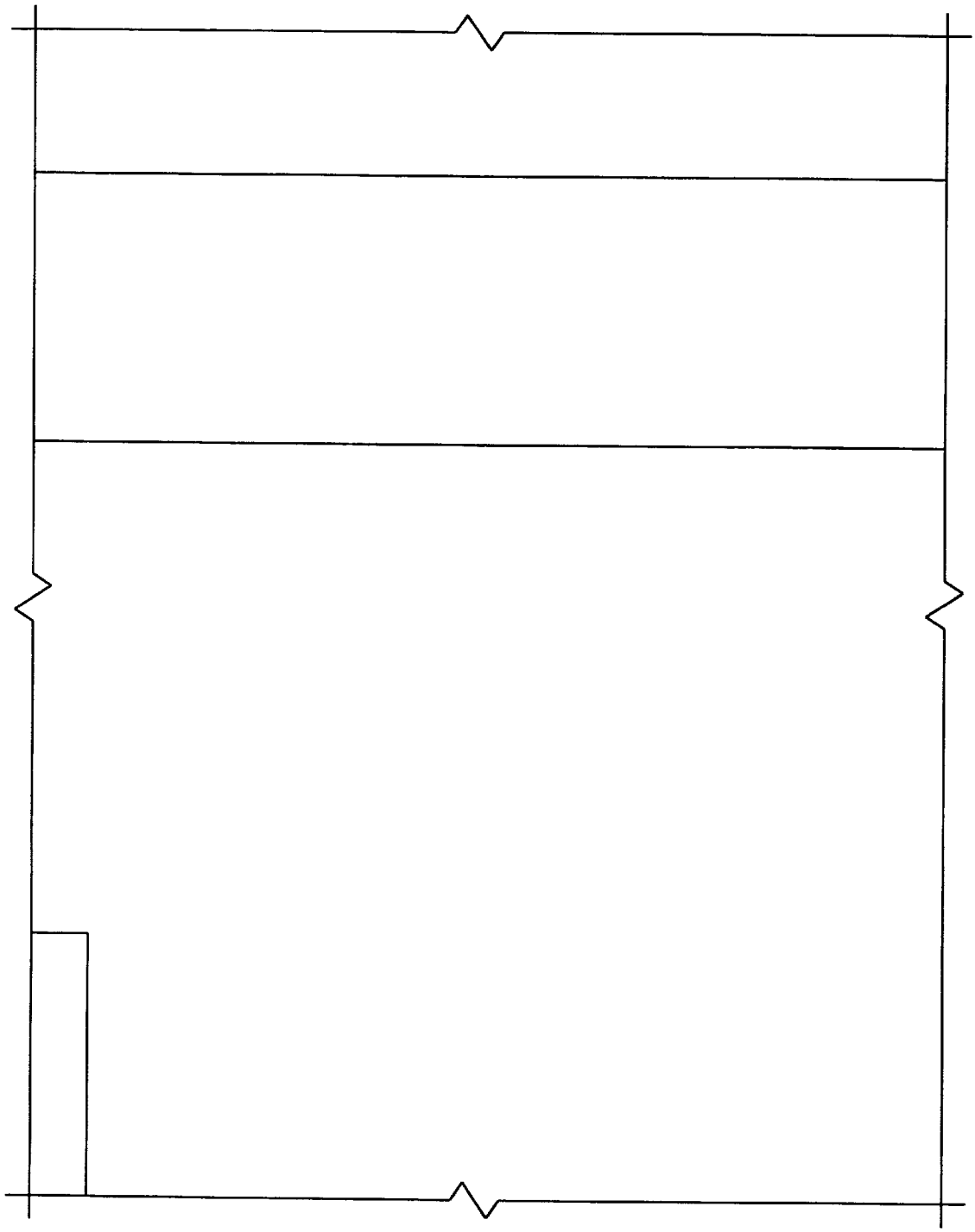


Fig 8.01071.01

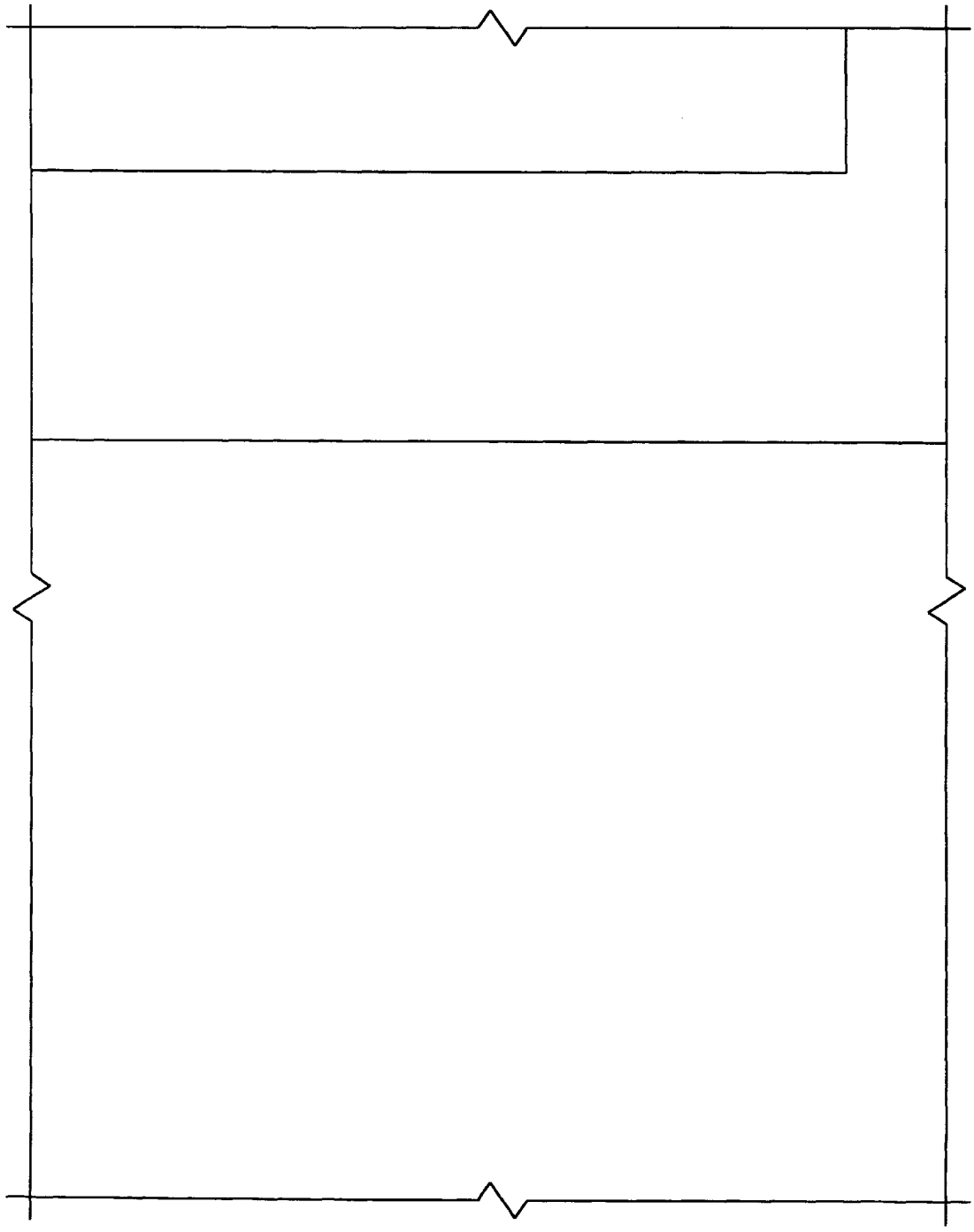


Fig 8.0107DK

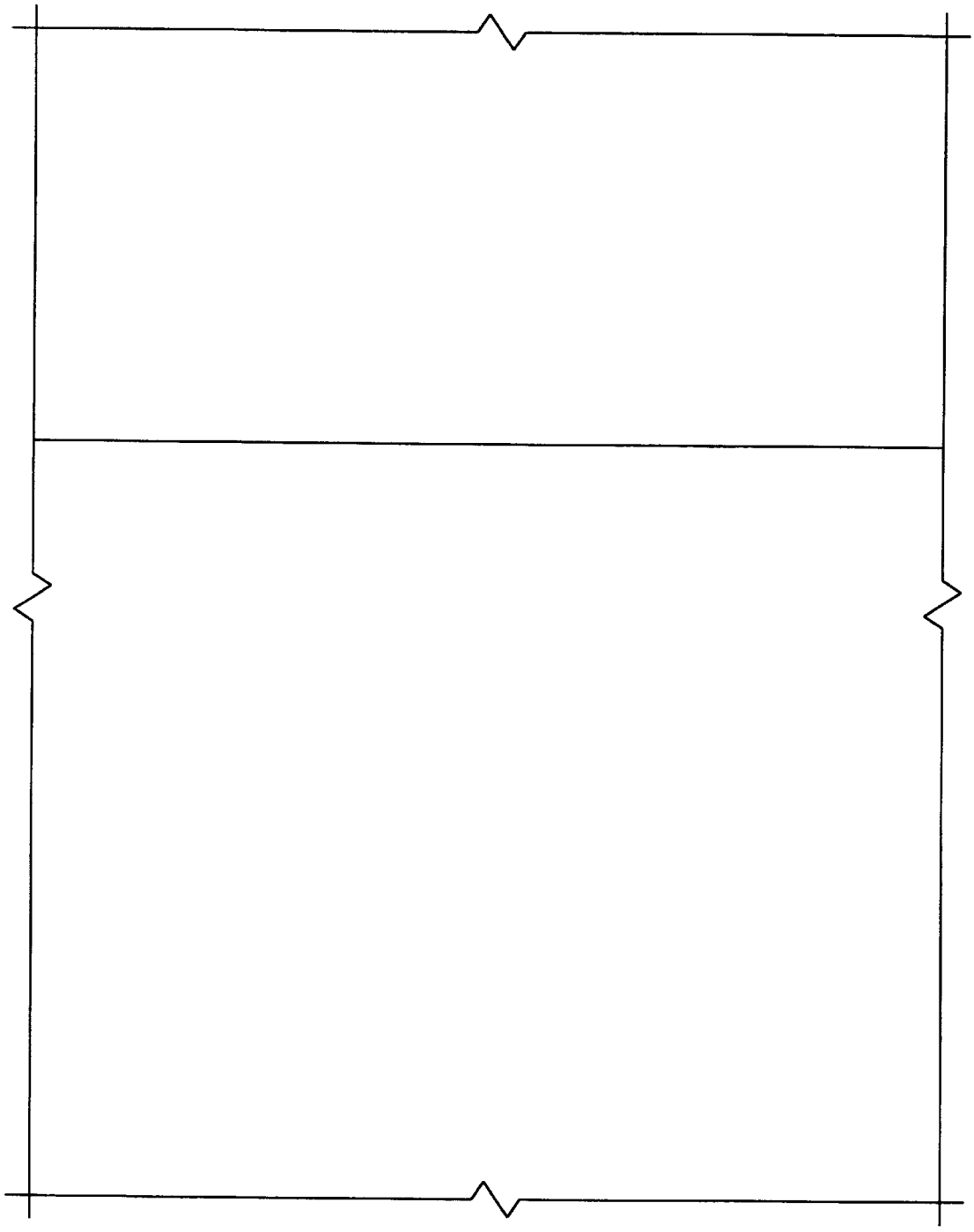


Fig 8.0107101

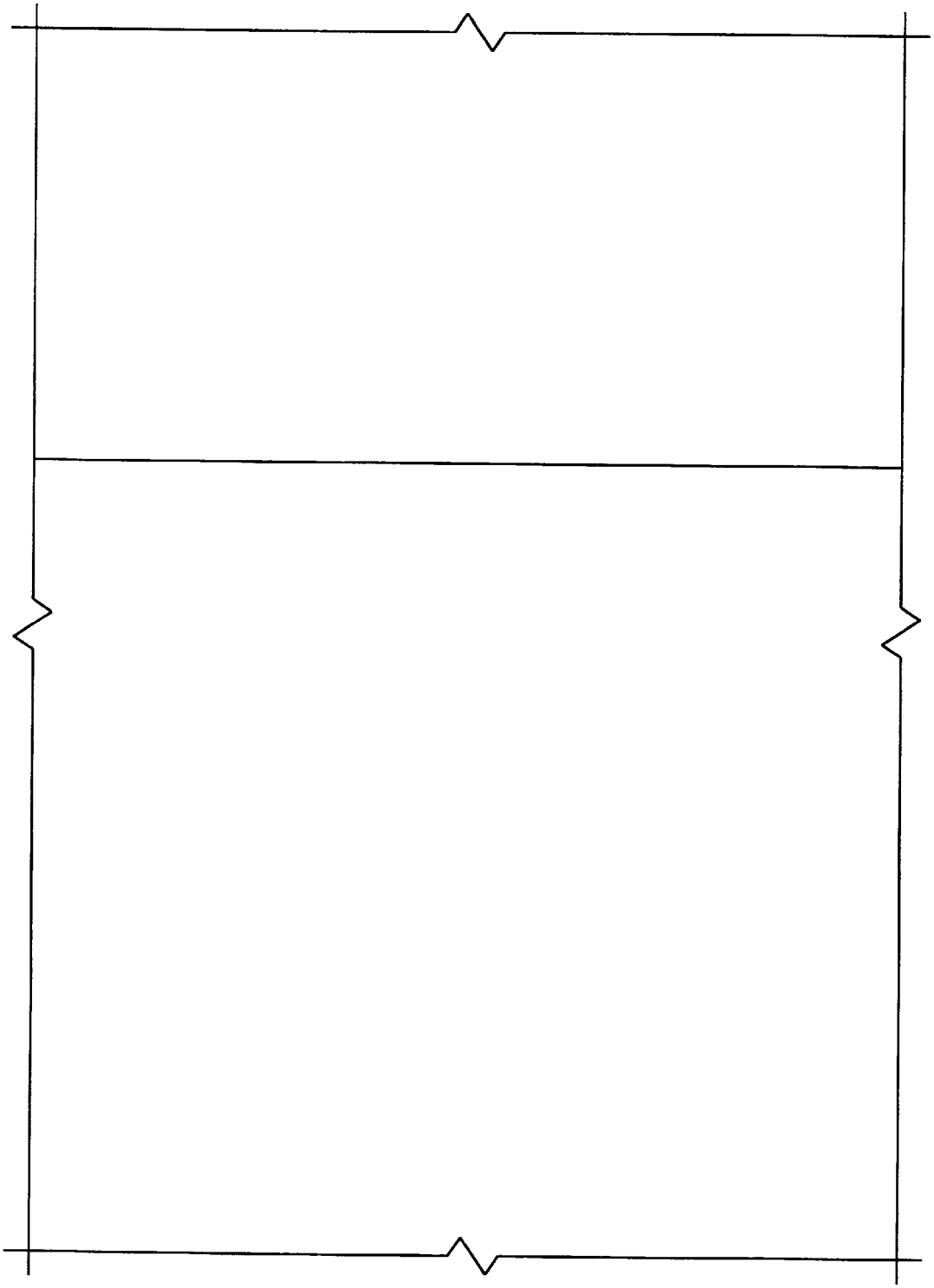


Fig 8.0107DM

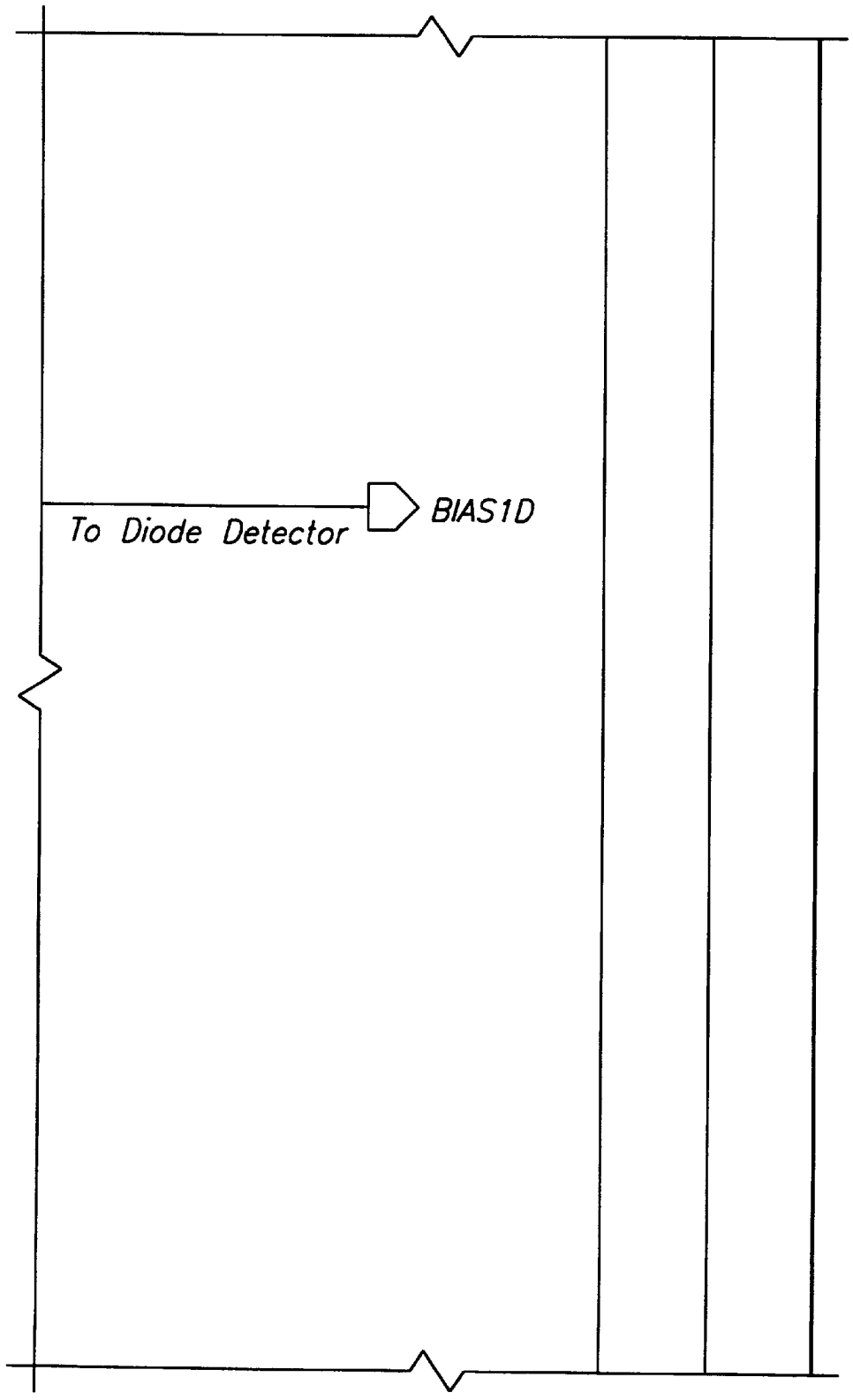


Fig 8.0107DN

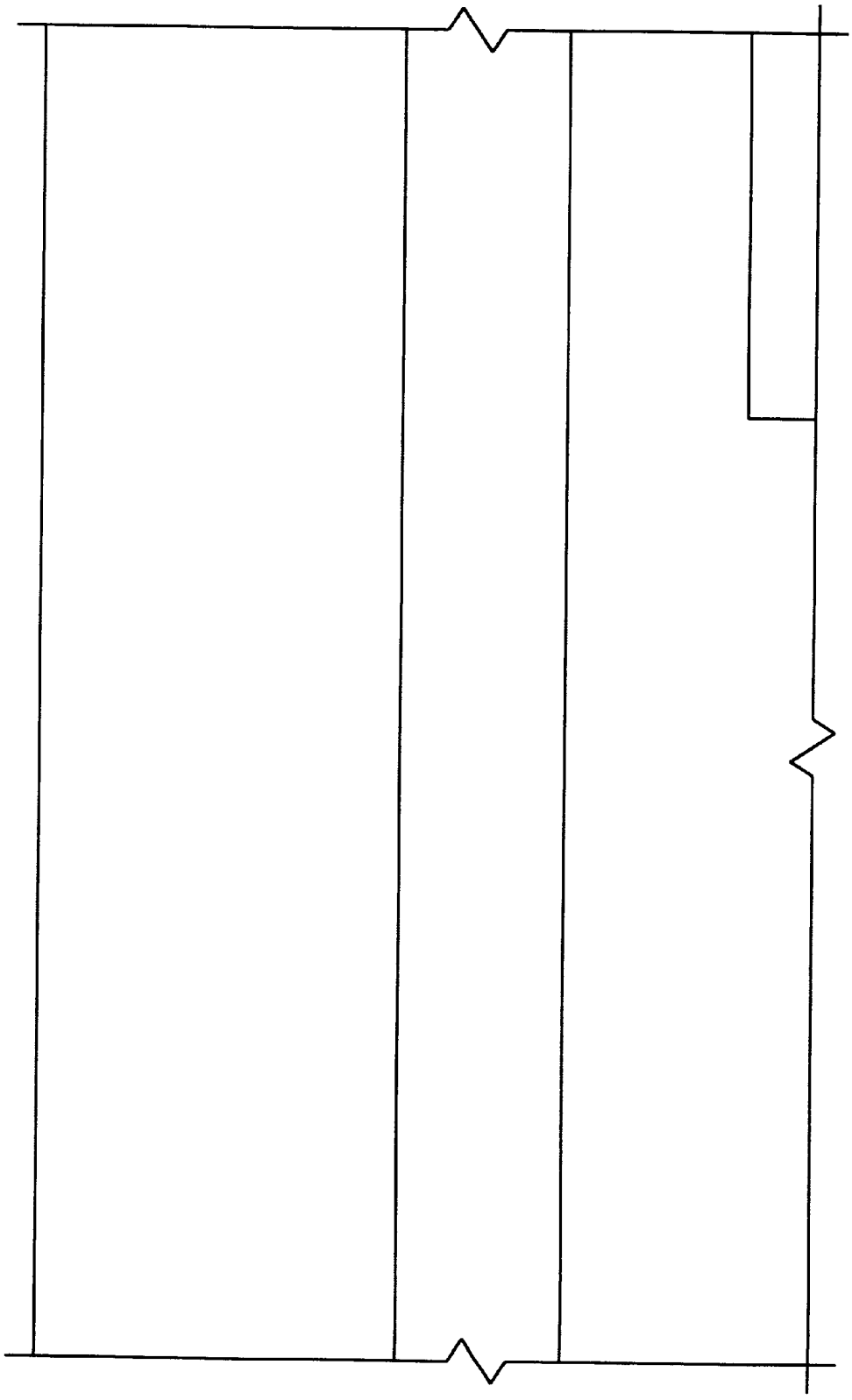


Fig 8.0107EA

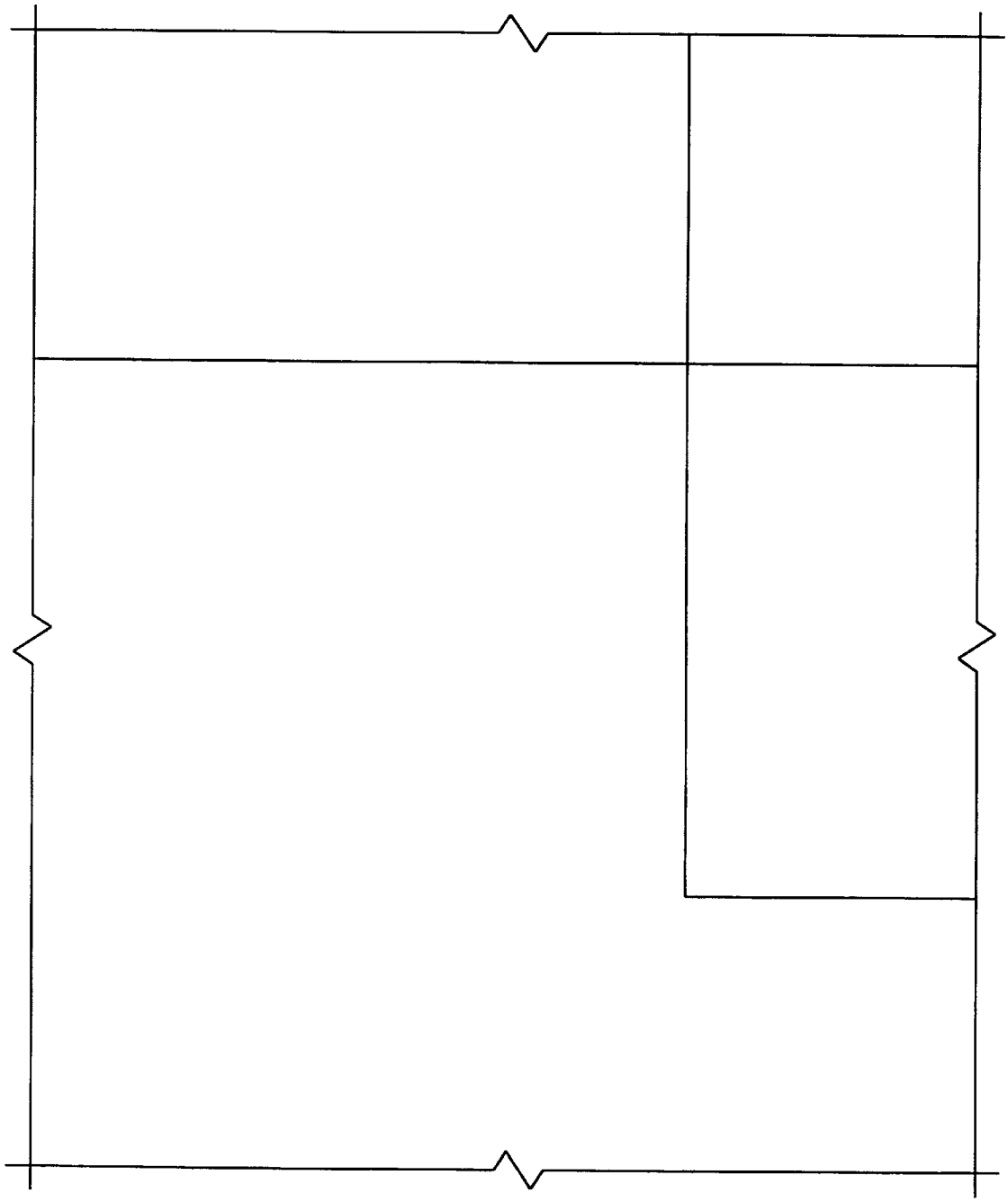
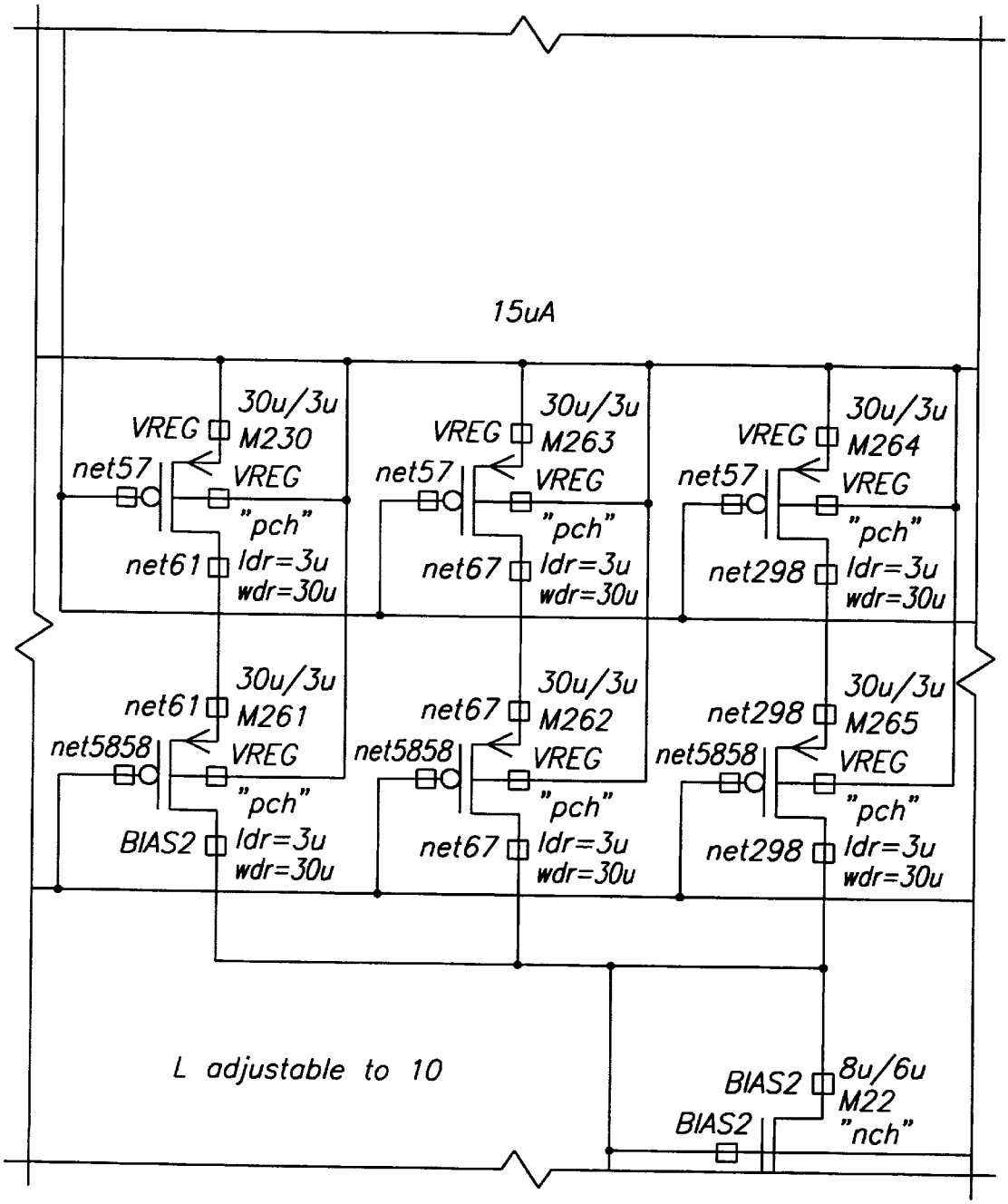


Fig. 8.0107EB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VREG
30u/3u
M230
net57
VREG
"pch"
net61
ldr=3u
wdr=30u
VREG
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M263
net57
VREG
"pch"
net67
ldr=3u
wdr=30u
VREG
30u/3u
M264
net57
VREG
"pch"
net298
ldr=3u
wdr=30u
net61
30u/3u
M261
net5858
VREG
"pch"
BIAS2
ldr=3u
wdr=30u
net67
30u/3u
M262
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VREG
"pch"
net67
ldr=3u
wdr=30u
net298
30u/3u
M265
net5858
VREG
"pch"
net298
ldr=3u
wdr=30u
L adjustable to 10
BIAS2
8u/6u
M22
"nch"
BIAS2

Fig 80110EC

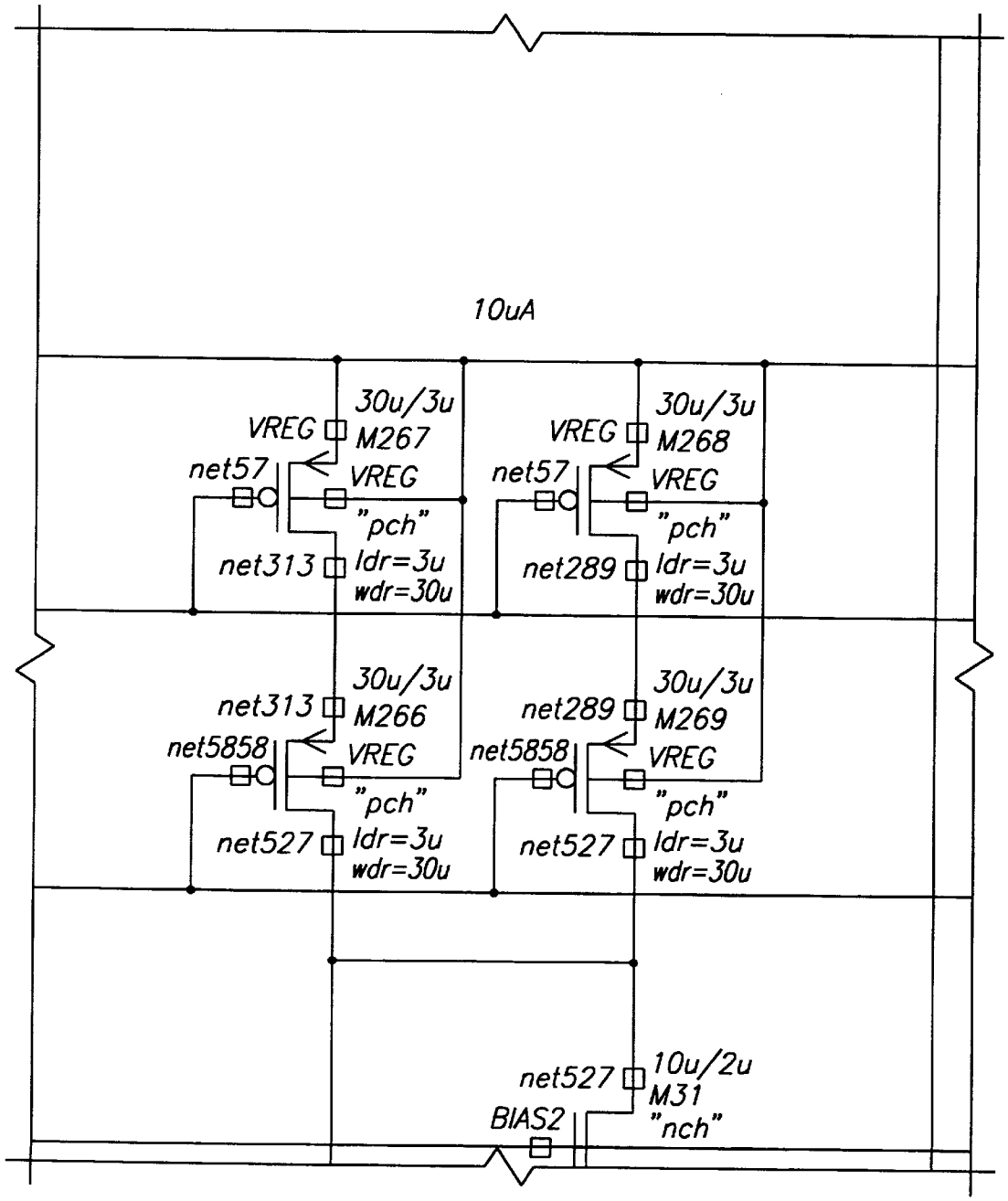


FIG 88.01007ED

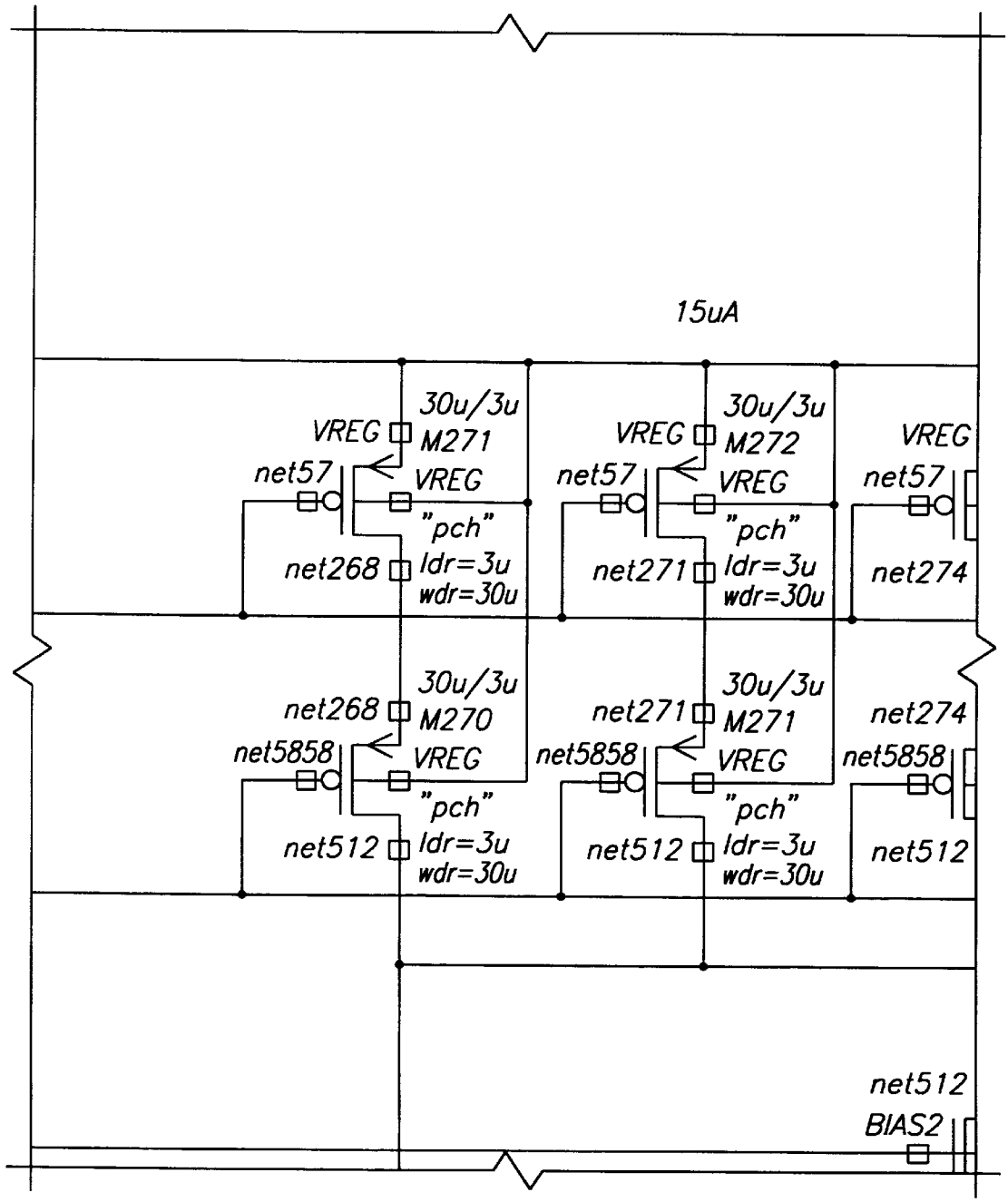
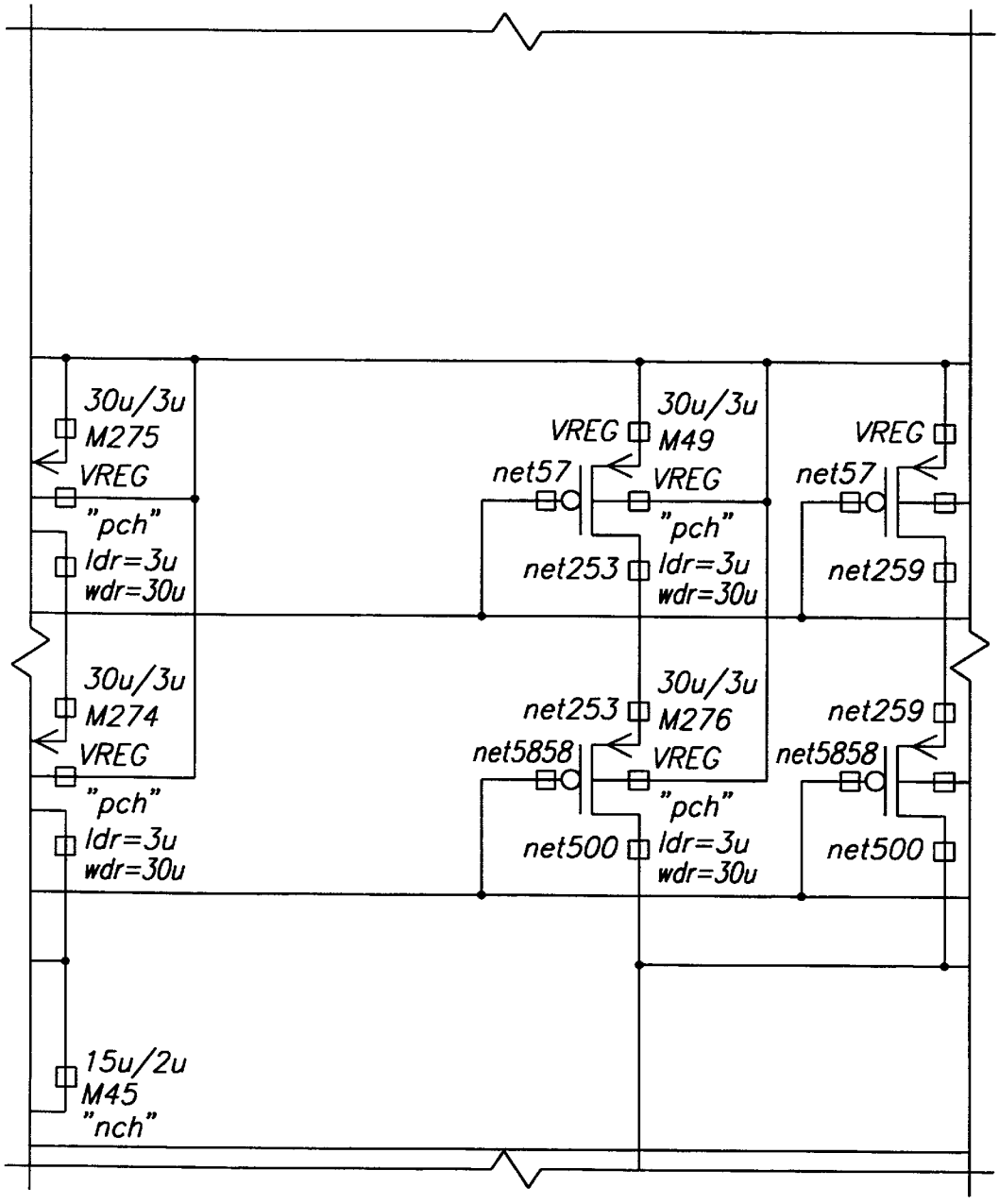


Fig 88.0110EE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VREG
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wdr=30u
30u/3u
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VREG
net57
VREG
"pch"
net253
ldr=3u
wdr=30u
VREG
net57
net259
30u/3u
M274
VREG
"pch"
ldr=3u
wdr=30u
net253
30u/3u
M276
net5858
VREG
"pch"
net500
ldr=3u
wdr=30u
net259
net5858
net500
15u/2u
M45
"nch"

Fig 8.0107EF

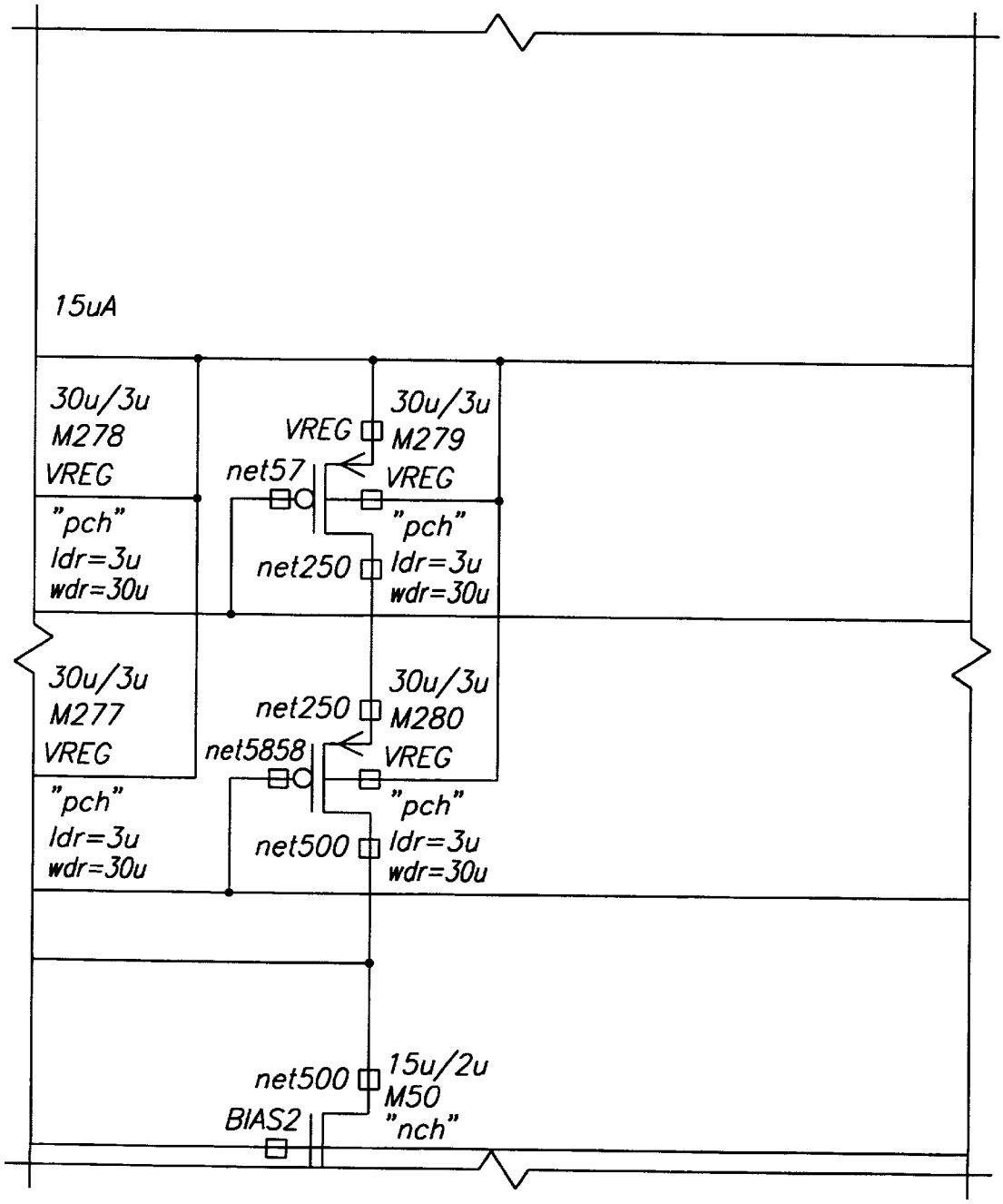
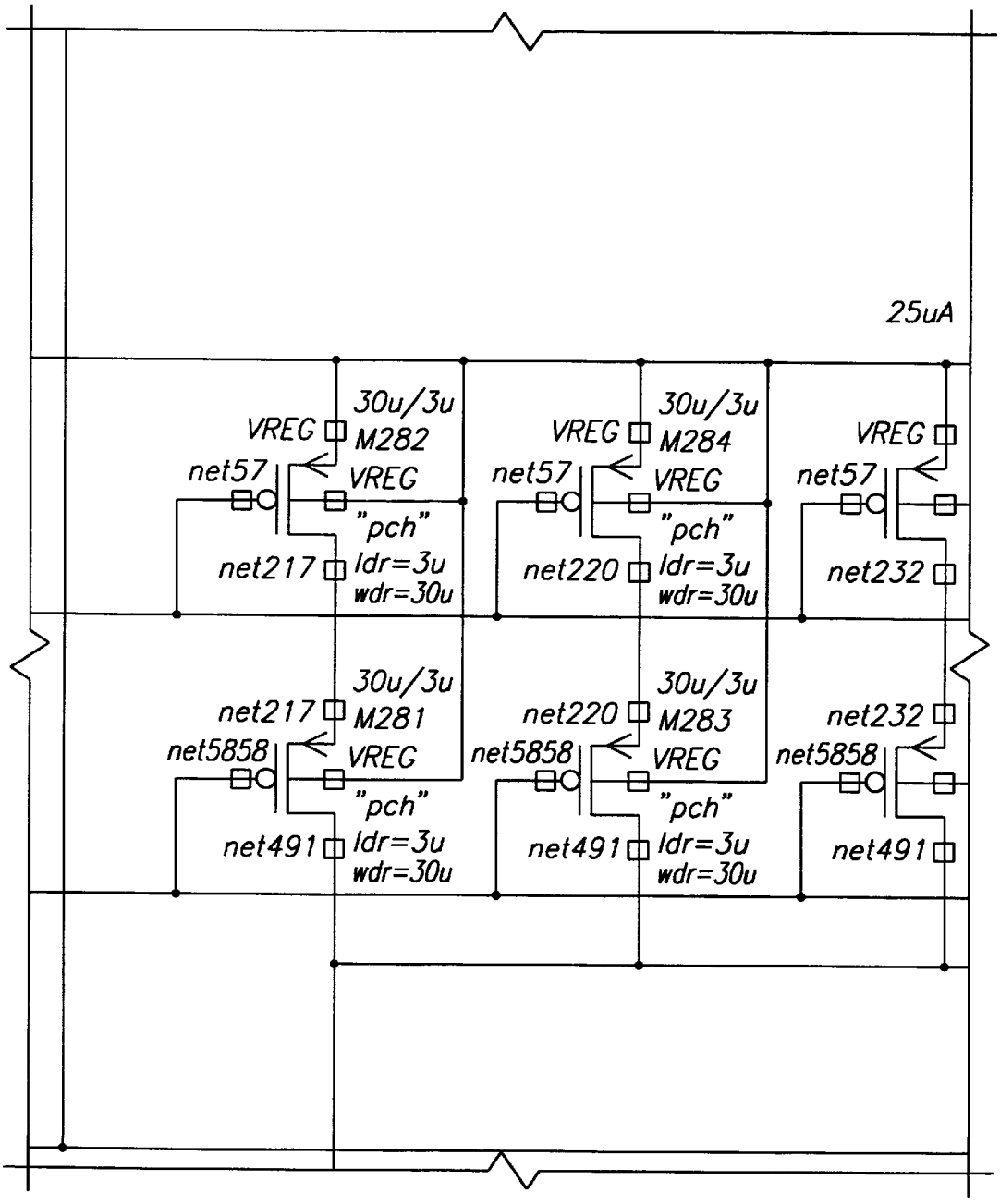

15uA
30u/3u
M278
VREG
"pch"
ldr=3u
wdr=30u
VREG
net57
net250
30u/3u
M279
VREG
"pch"
ldr=3u
wdr=30u
30u/3u
M277
VREG
"pch"
ldr=3u
wdr=30u
net250
net5858
net500
30u/3u
M280
VREG
"pch"
ldr=3u
wdr=30u
net500
BIAS2
15u/2u
M50
"nch"

FIG 8.0107E6


25uA
30u/3u
VREG
M282
net57
VREG
"pch"
net217
ldr=3u
wdr=30u
30u/3u
VREG
M284
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VREG
"pch"
net220
ldr=3u
wdr=30u
VREG
net57
net232
30u/3u
net217
M281
net5858
VREG
"pch"
net491
ldr=3u
wdr=30u
30u/3u
net220
M283
net5858
VREG
"pch"
net491
ldr=3u
wdr=30u
net232
net5858
net491

Fig 8010TEH

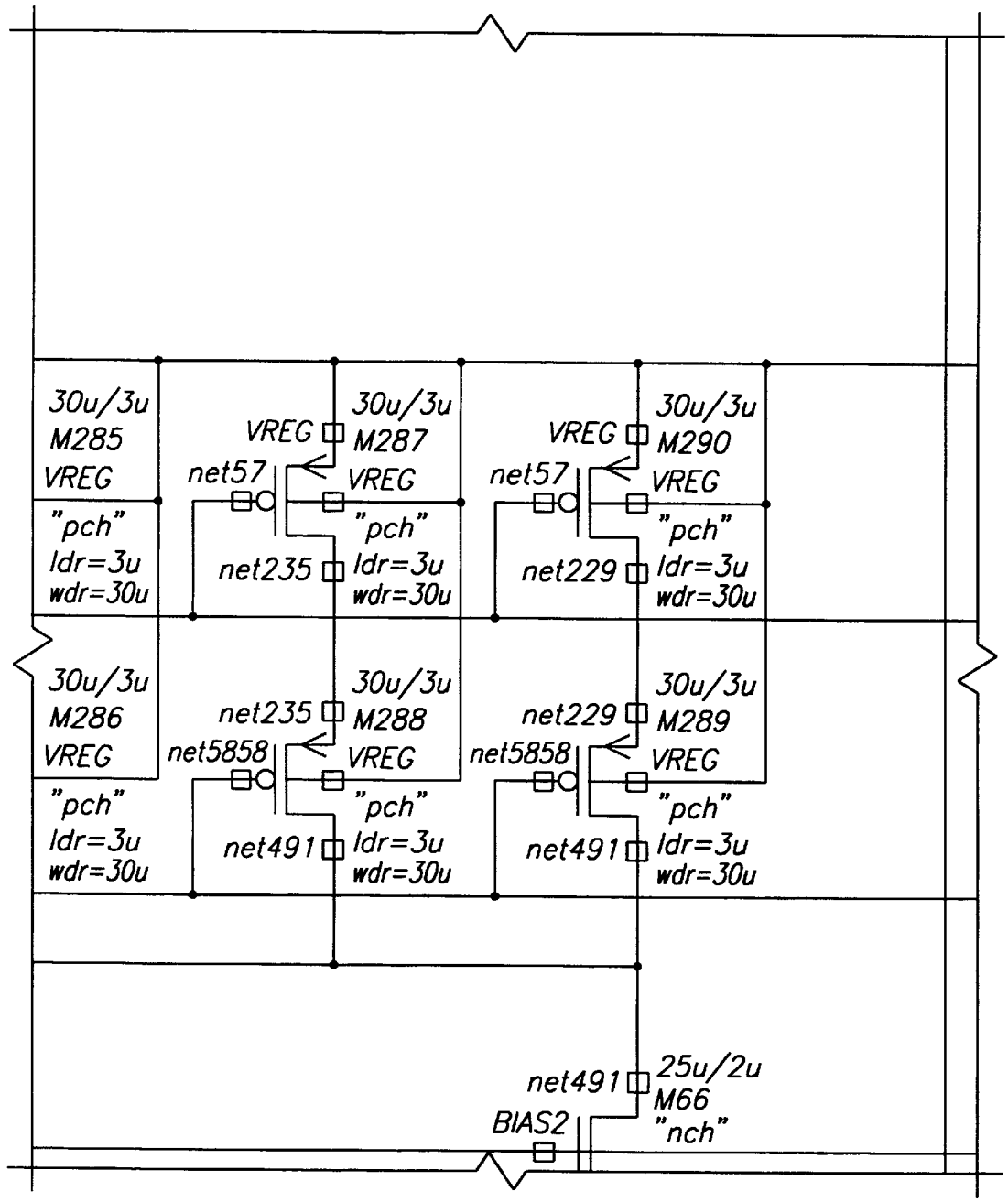
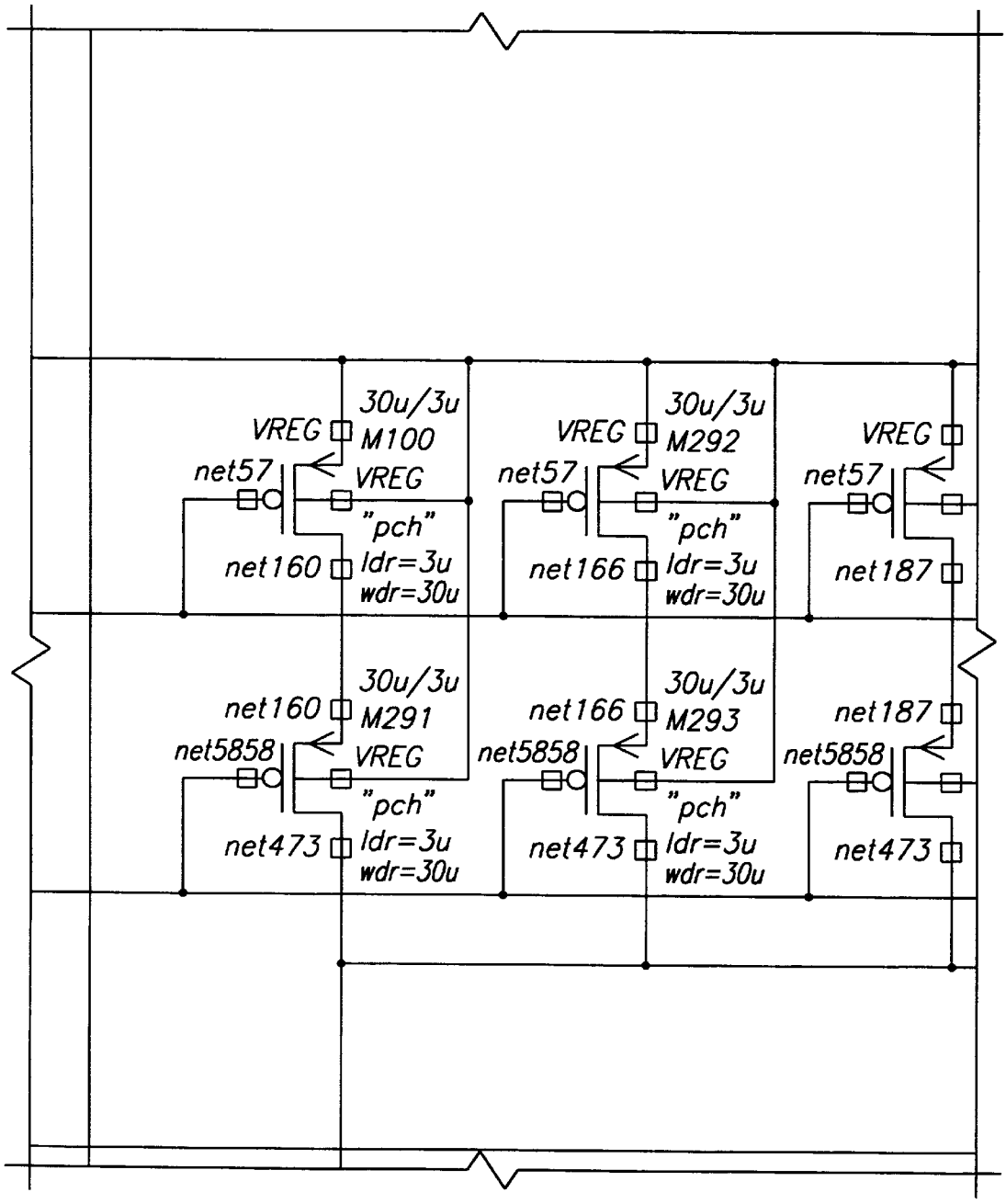


FIG. 8.0100'1E11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VREG
M100
net57
VREG
"pch"
net160
ldr=3u
wdr=30u
30u/3u
VREG
M292
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VREG
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ldr=3u
wdr=30u
VREG
net57
net187
30u/3u
net160
M291
net5858
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"pch"
net473
ldr=3u
wdr=30u
30u/3u
net166
M293
net5858
VREG
"pch"
net473
ldr=3u
wdr=30u
net187
net5858
net473

Fig 8.0110Ed

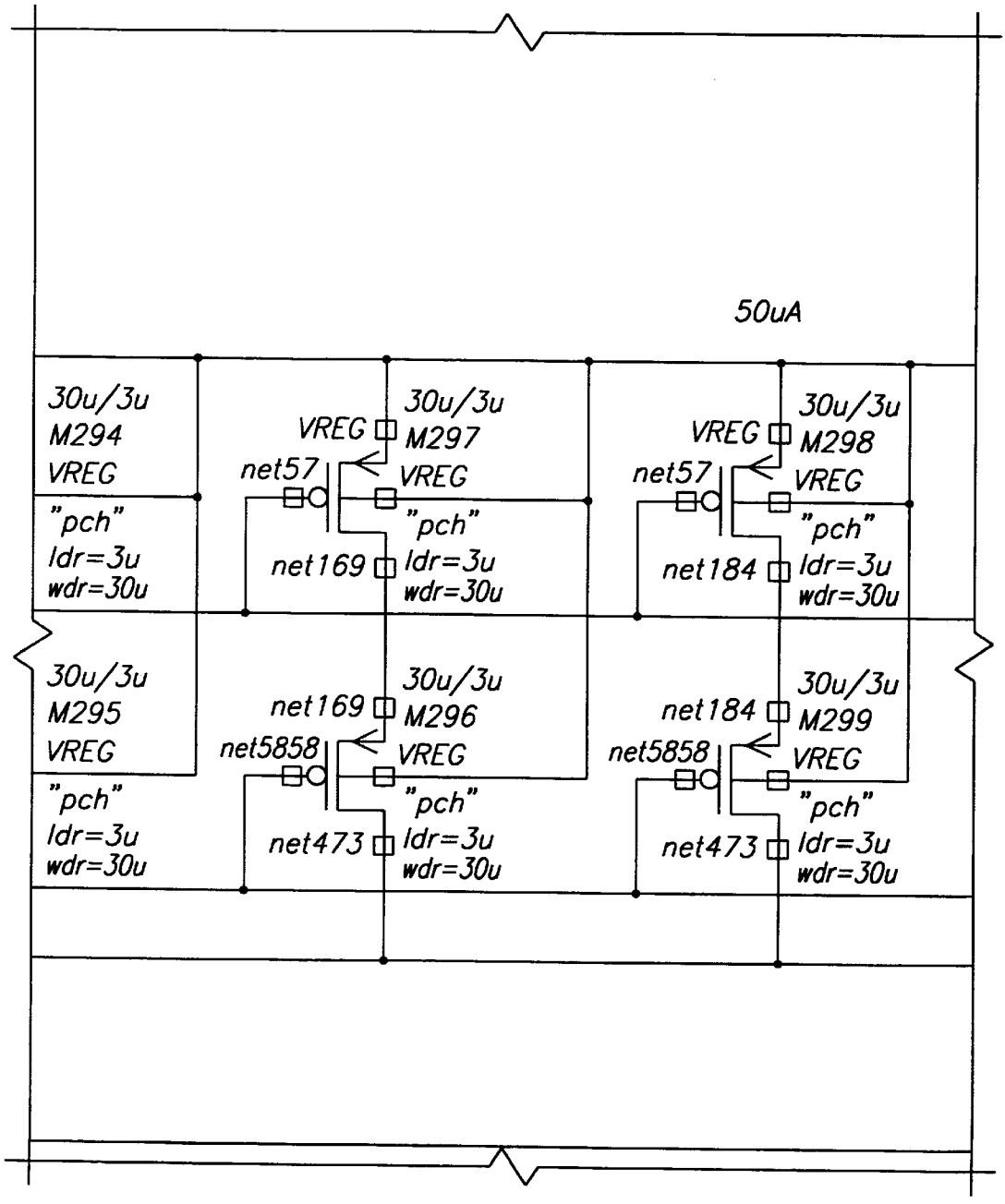
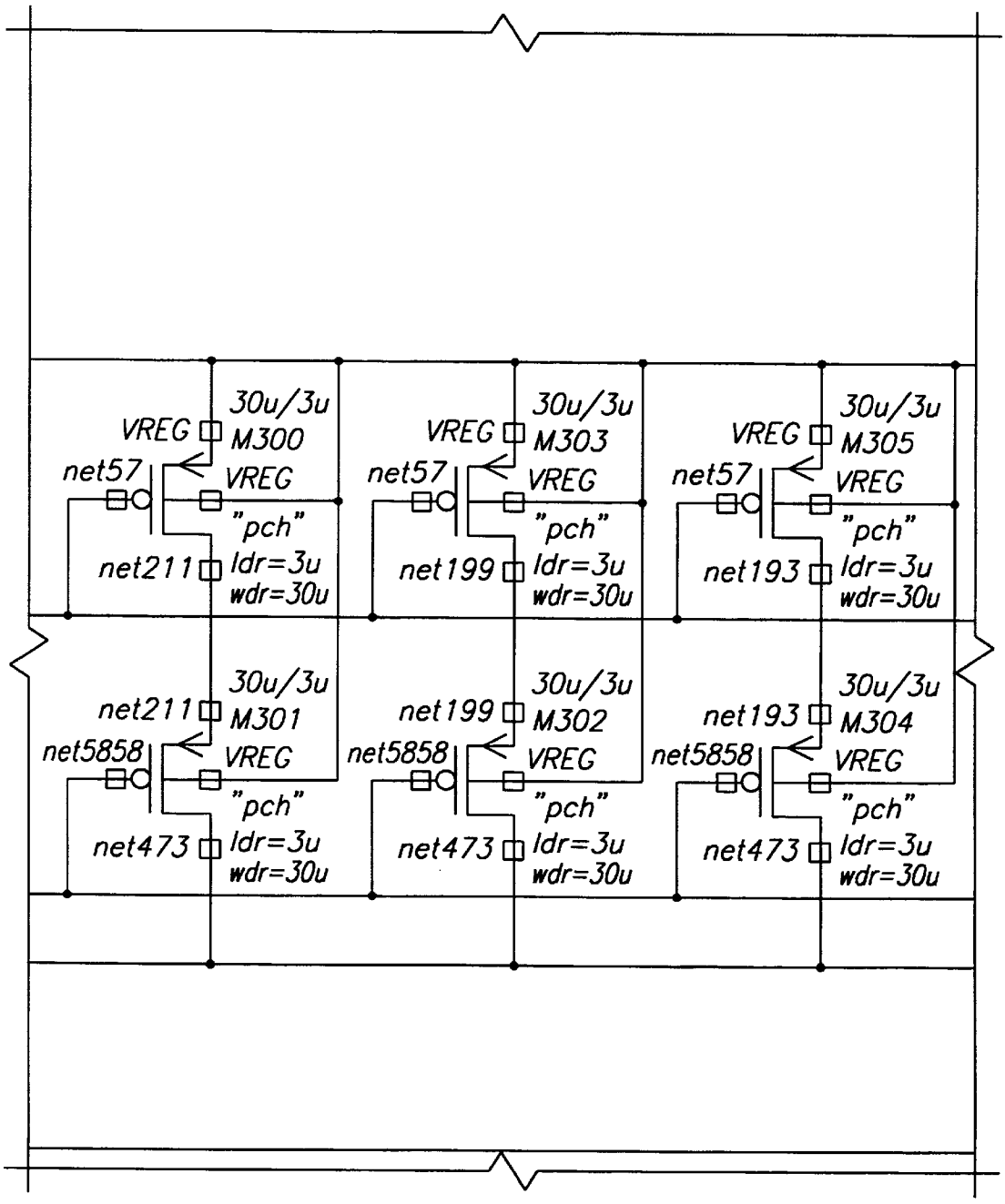

50uA
30u/3u
M294
VREG
"pch"
ldr=3u
wdr=30u
30u/3u
VREG
M297
net57
VREG
"pch"
net169
ldr=3u
wdr=30u
30u/3u
VREG
M298
net57
VREG
"pch"
net184
ldr=3u
wdr=30u
30u/3u
M295
VREG
"pch"
ldr=3u
wdr=30u
30u/3u
net169
M296
net5858
VREG
"pch"
net473
ldr=3u
wdr=30u
30u/3u
net184
M299
net5858
VREG
"pch"
net473
ldr=3u
wdr=30u

Fig 8.0110E


30u/3u
VREG
M300
net57
VREG
"pch"
net211
ldr=3u
wdr=30u
30u/3u
VREG
M303
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VREG
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net199
ldr=3u
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30u/3u
VREG
M305
net57
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wdr=30u
30u/3u
net211
M301
net5858
VREG
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wdr=30u
30u/3u
net199
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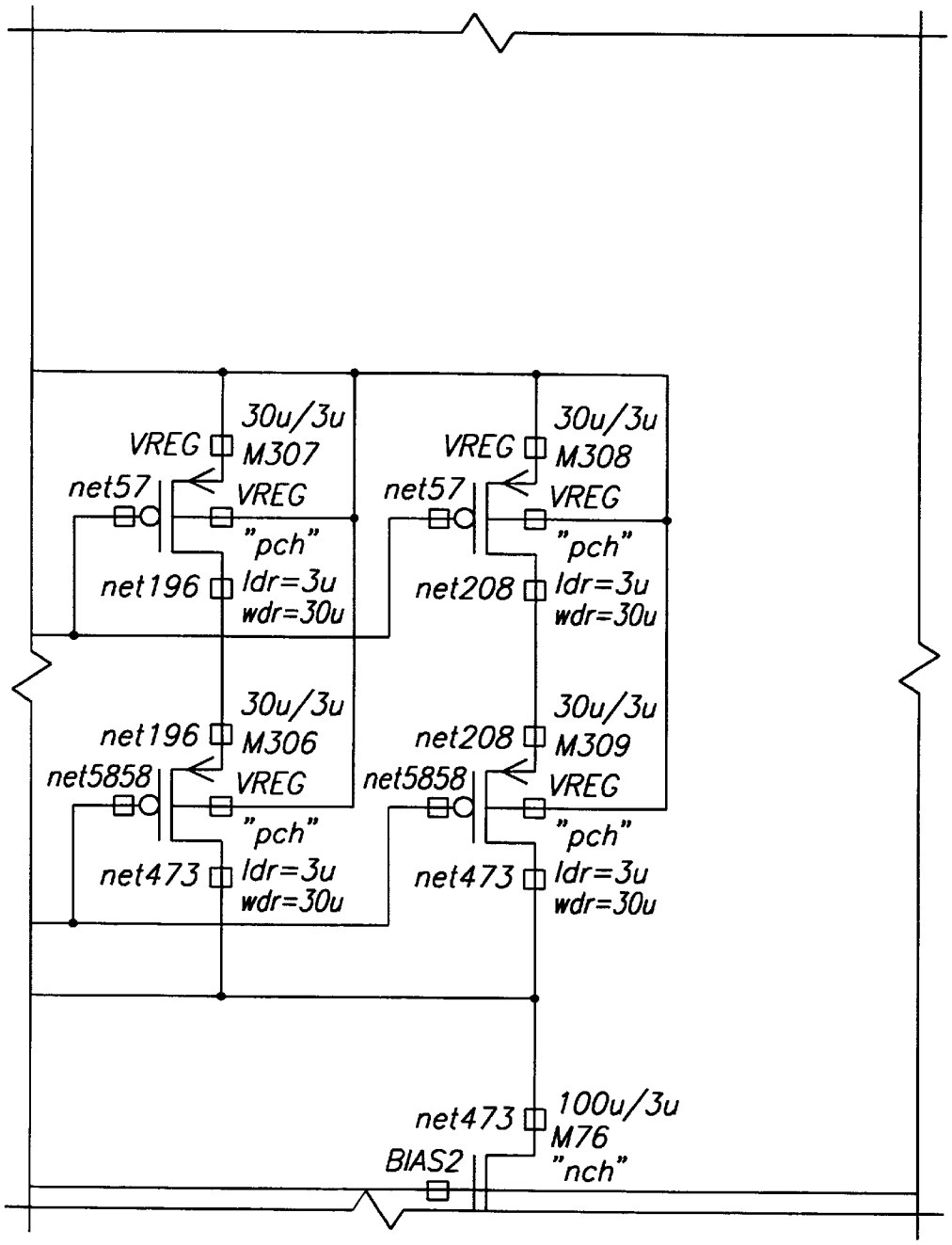
"pch"
net473
ldr=3u
wdr=30u
30u/3u
net193
M304
net5858
VREG
"pch"
net473
ldr=3u
wdr=30u

FIG 8.0110E


30u/3u
VREG
M307
net57
VREG
"pch"
net196
ldr=3u
wdr=30u
30u/3u
VREG
M308
net57
VREG
"pch"
net208
ldr=3u
wdr=30u
30u/3u
net196
M306
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VREG
"pch"
net473
ldr=3u
wdr=30u
30u/3u
net208
M309
net5858
VREG
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net473
ldr=3u
wdr=30u
100u/3u
net473
M76
BIAS2
"nch"

FIG 8.0107EM

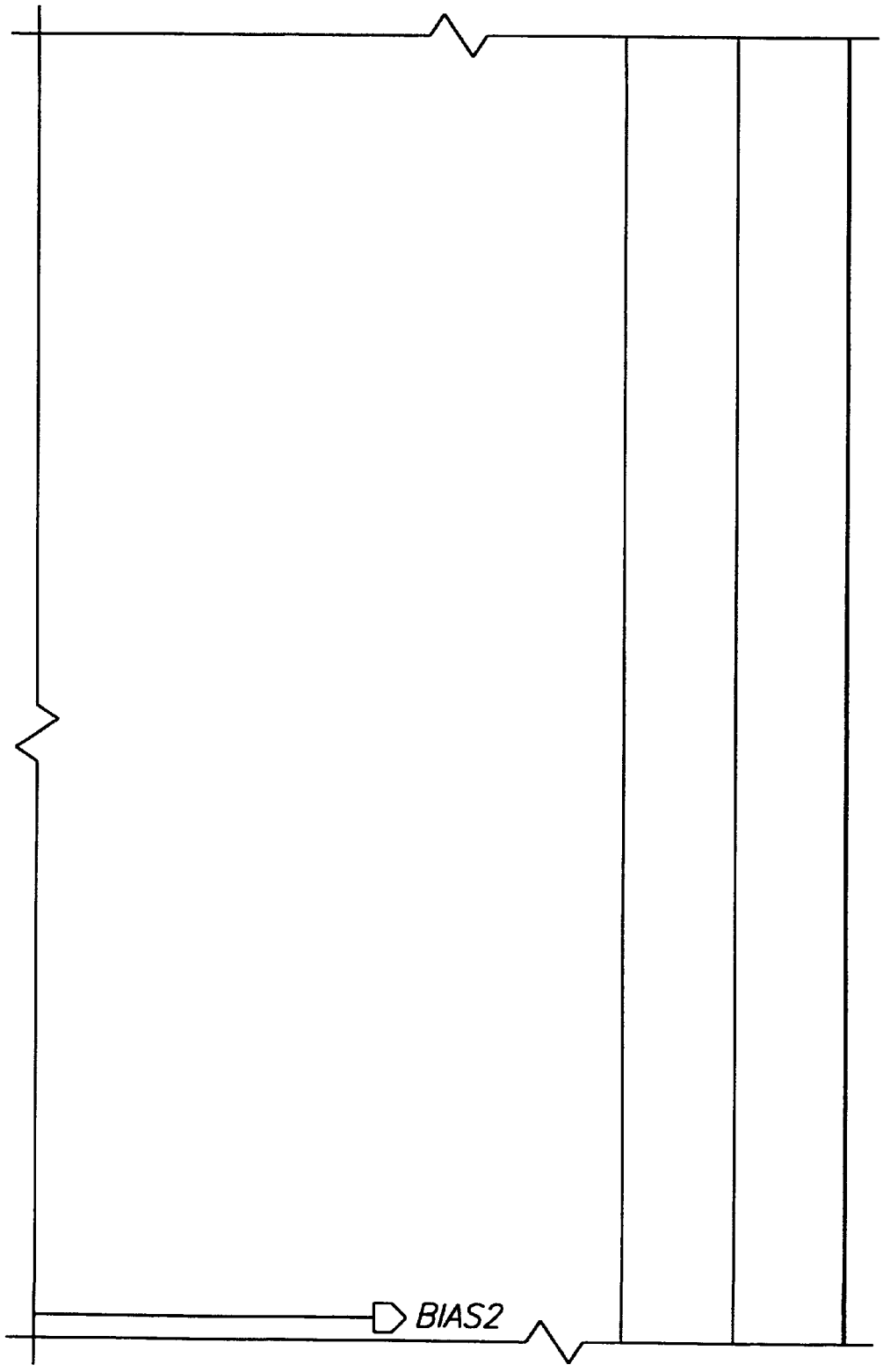


Fig 88.00107EN

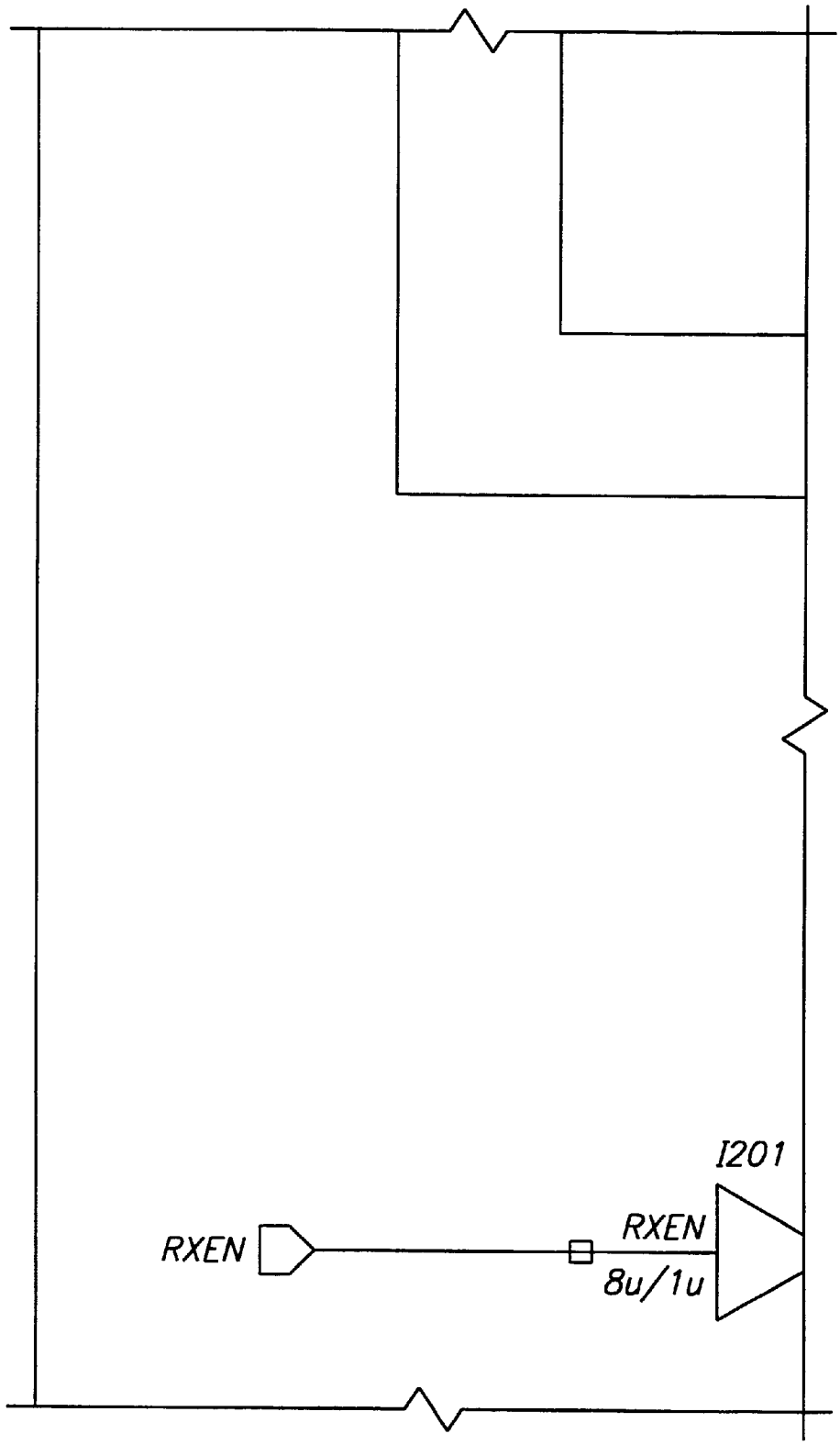


Fig 8010FA

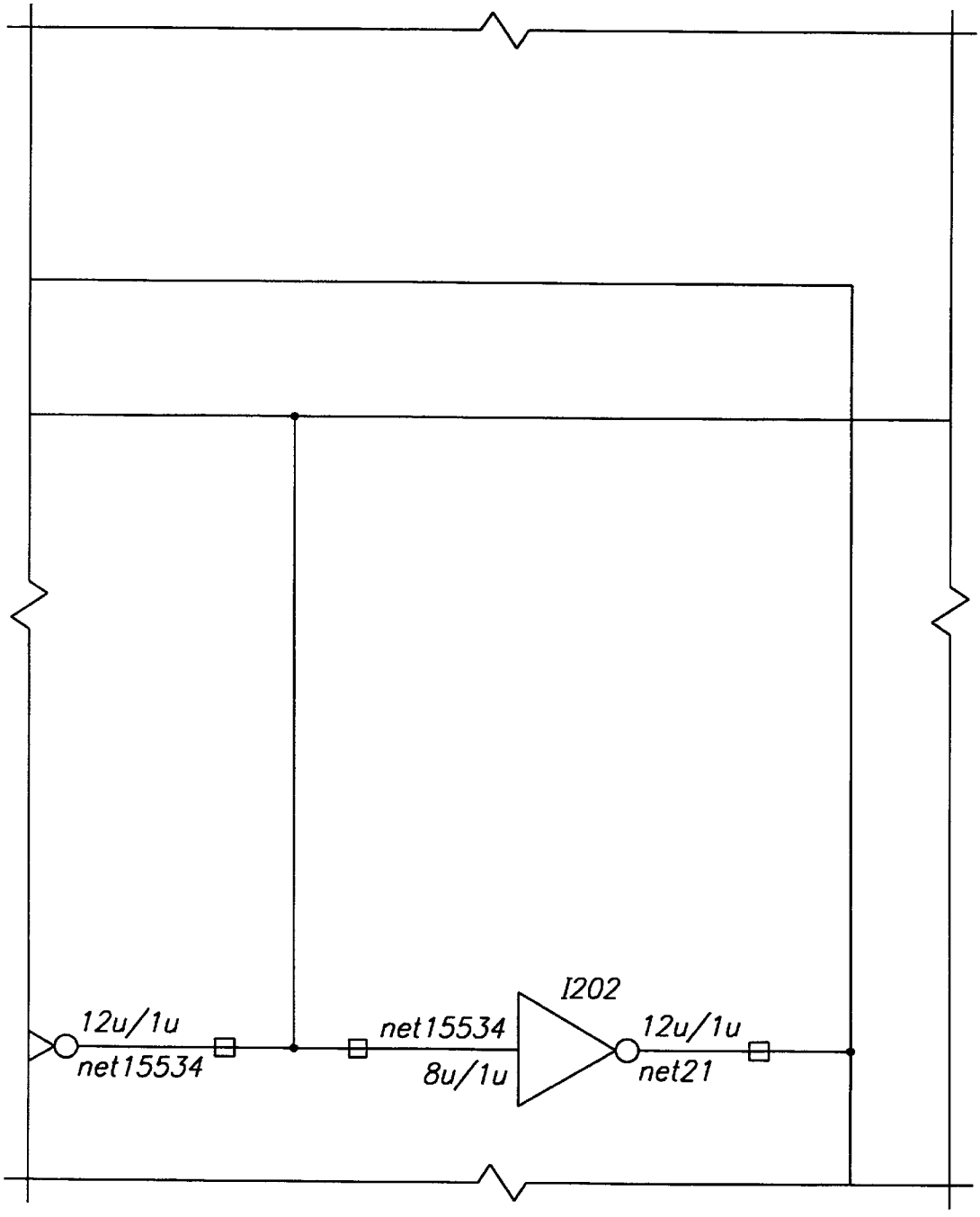


FIG 88.0110FB

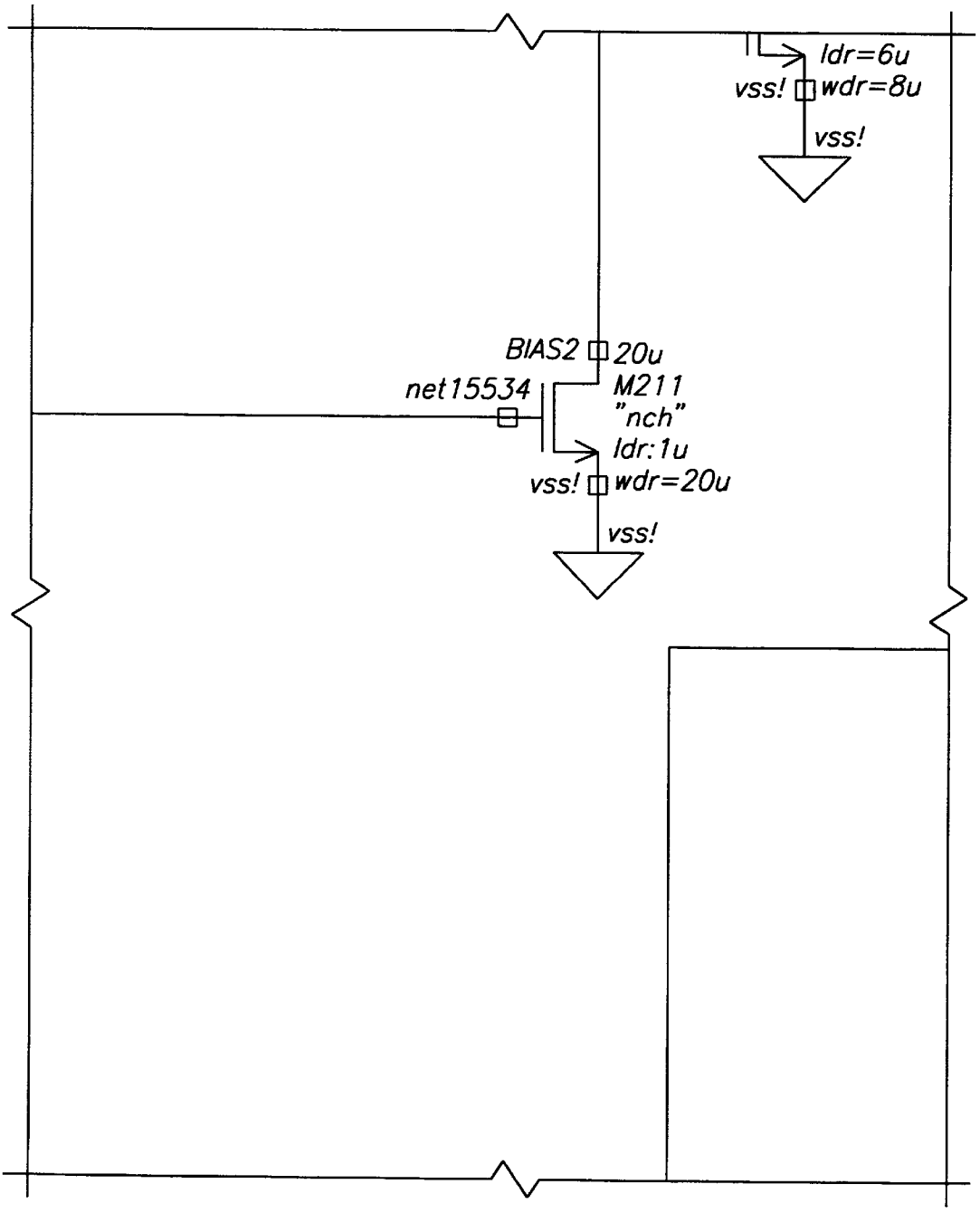
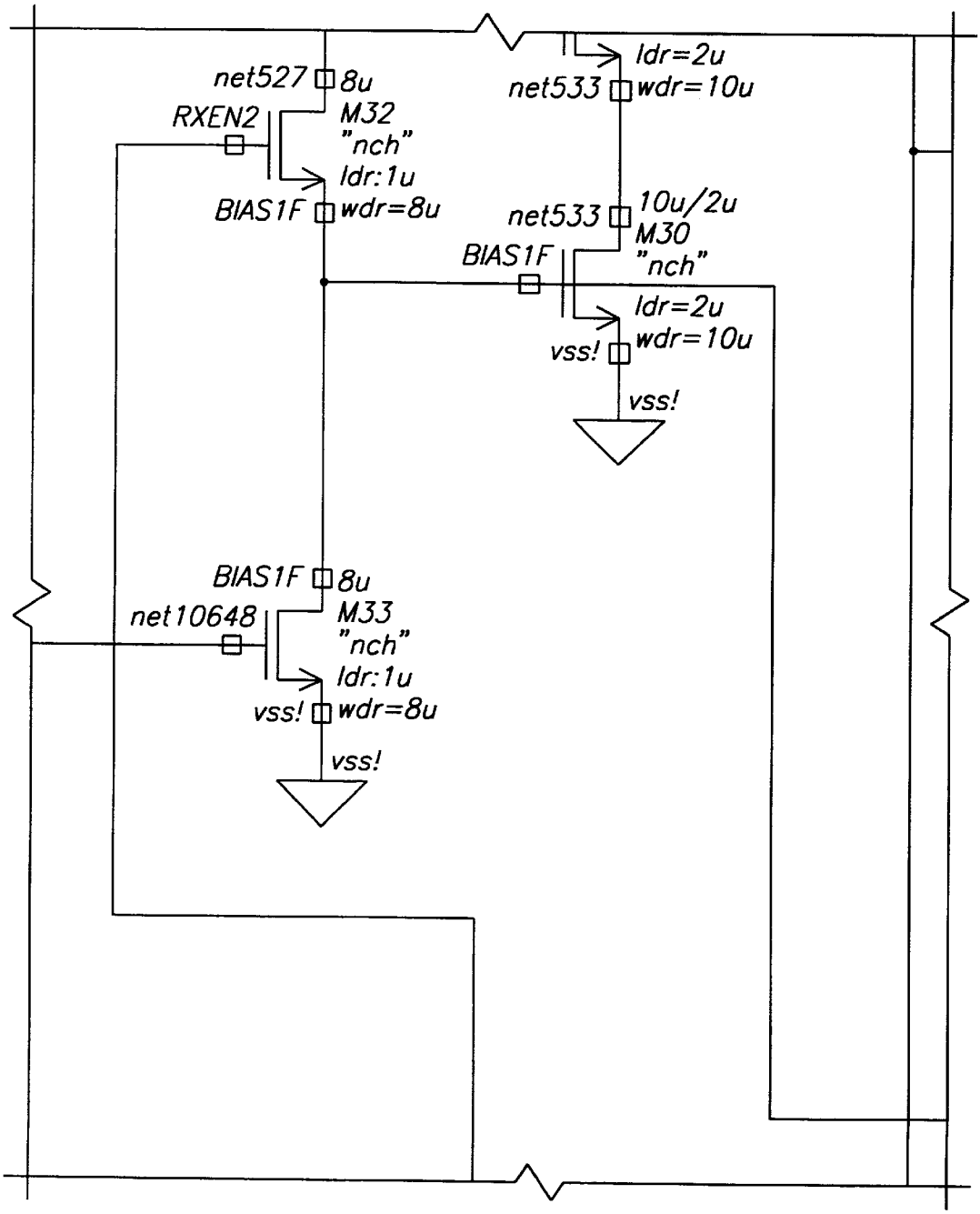

ldr=6u
vss!
wdr=8u
vss!
BIAS2
20u
net15534
M211
"nch"
ldr:1u
vss!
wdr=20u
vss!

Fig 8.0107fc


net527
8u
RXEN2
M32
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BIAS1F
wdr=8u
ldr=2u
net533
wdr=10u
net533
10u/2u
M30
"nch"
BIAS1F
ldr=2u
vss!
wdr=10u
vss!
BIAS1F
8u
net10648
M33
"nch"
ldr:1u
vss!
wdr=8u
vss!

Fig 8.0107F

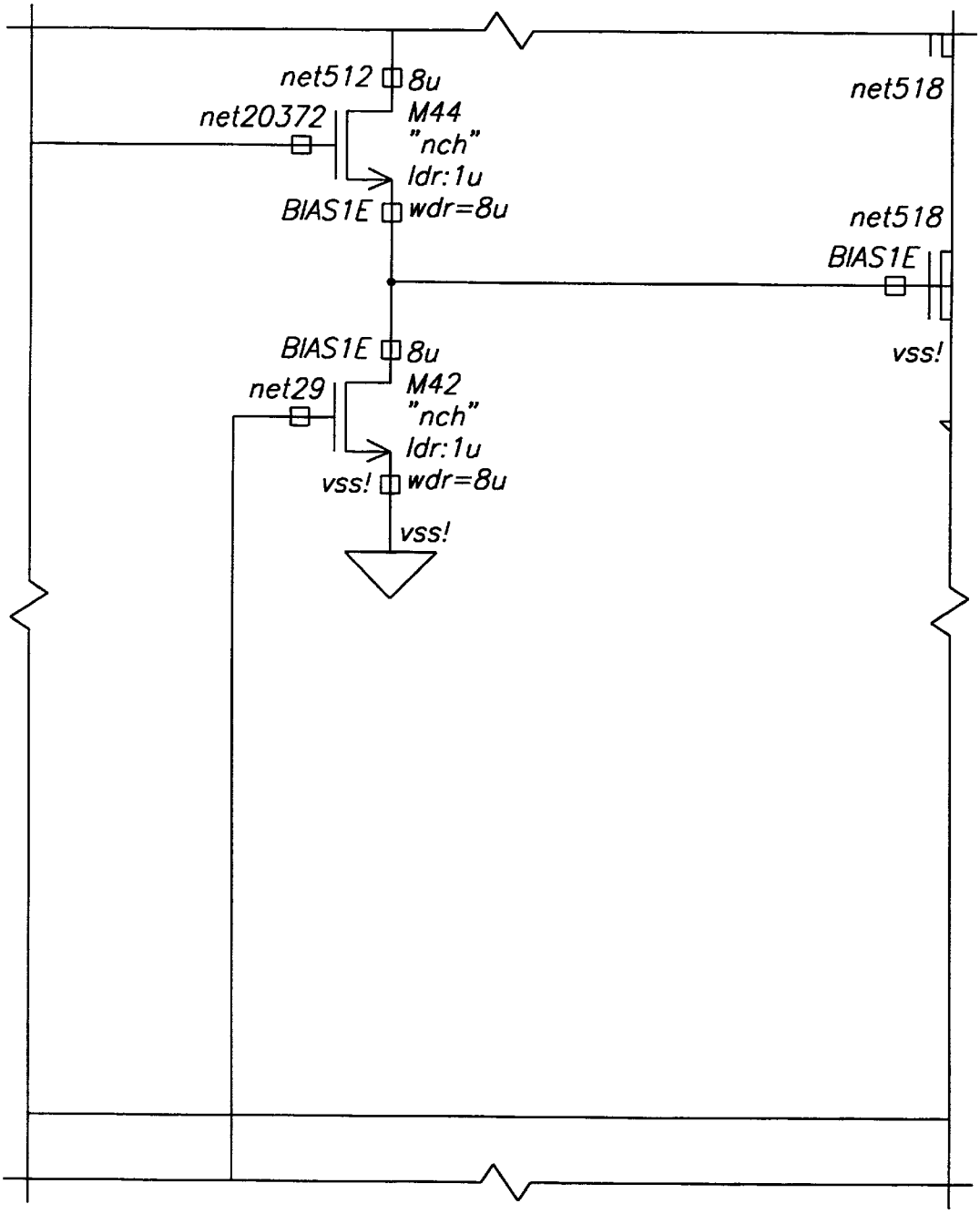

net512
8u
M44
"nch"
ldr:1u
wdr=8u
net20372
BIAS1E
net518
net518
BIAS1E
vss!
BIAS1E
8u
M42
"nch"
ldr:1u
wdr=8u
net29
vss!
vss!

Fig 8.0107E

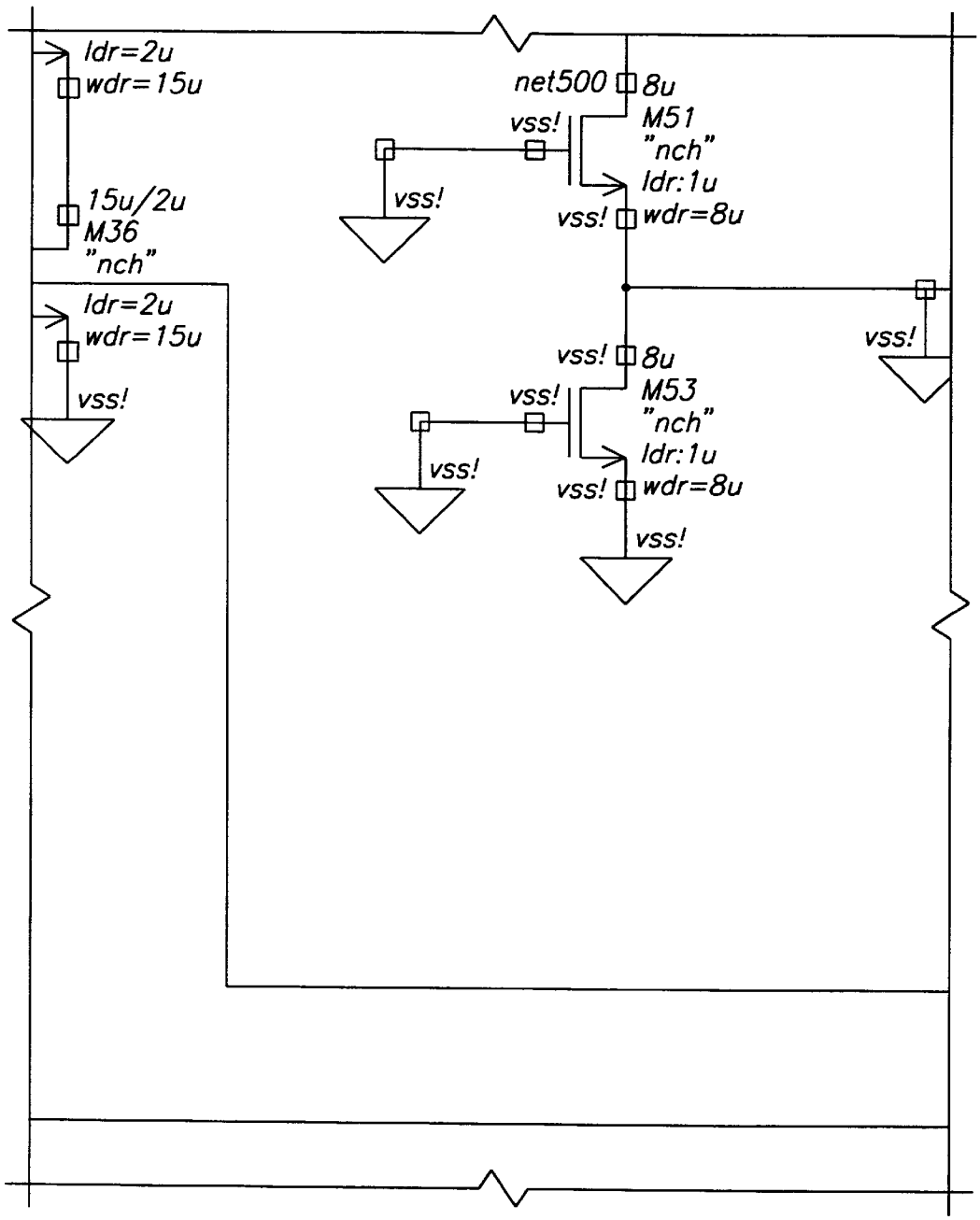
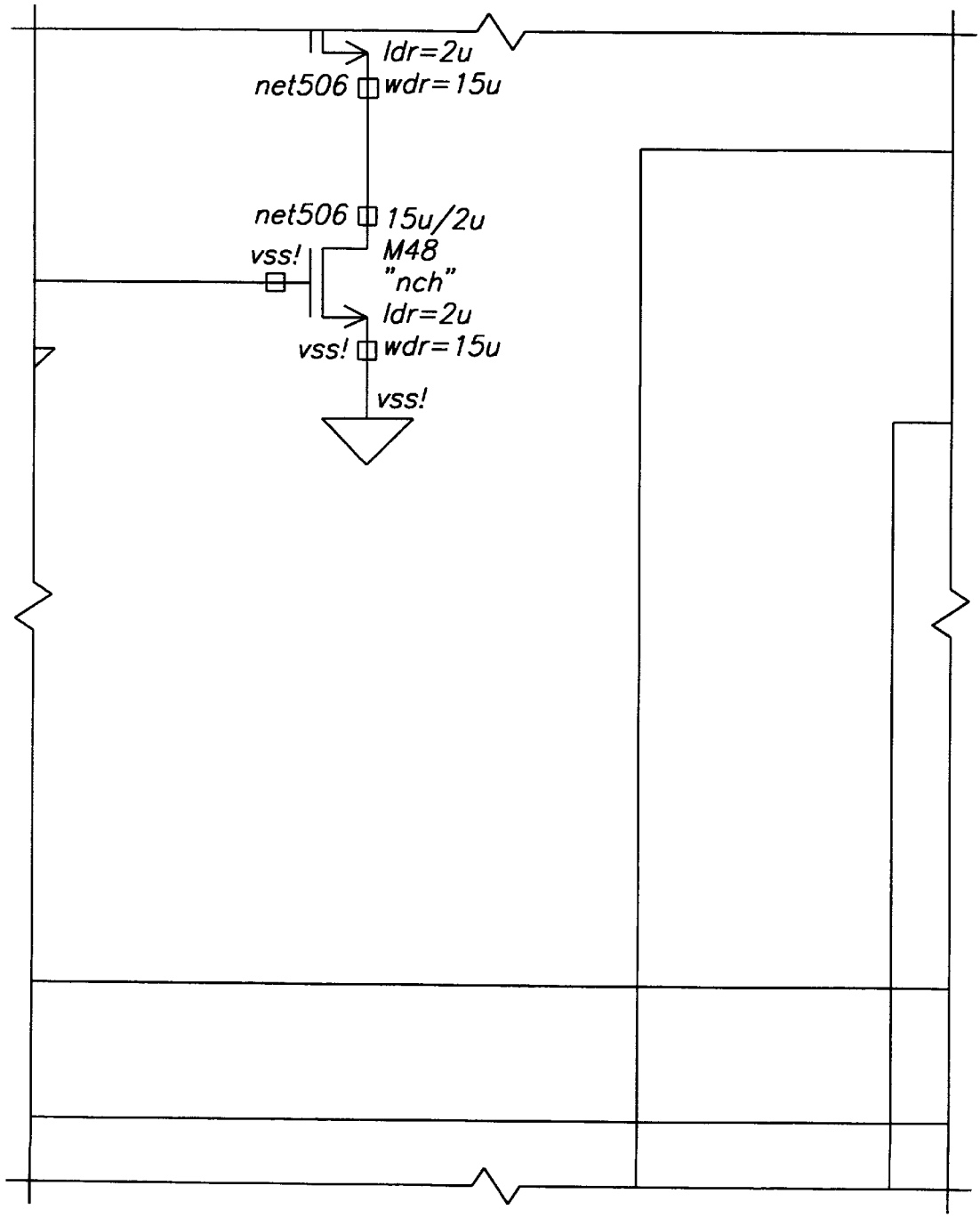

ldr=2u
wdr=15u
15u/2u
M36
"nch"
ldr=2u
wdr=15u
vss!
vss!
net500
8u
vss!
M51
"nch"
ldr:1u
vss!
wdr=8u
vss!
vss!
vss!
8u
vss!
M53
"nch"
ldr:1u
vss!
wdr=8u
vss!
vss!

Fig 8.0107F


ldr=2u
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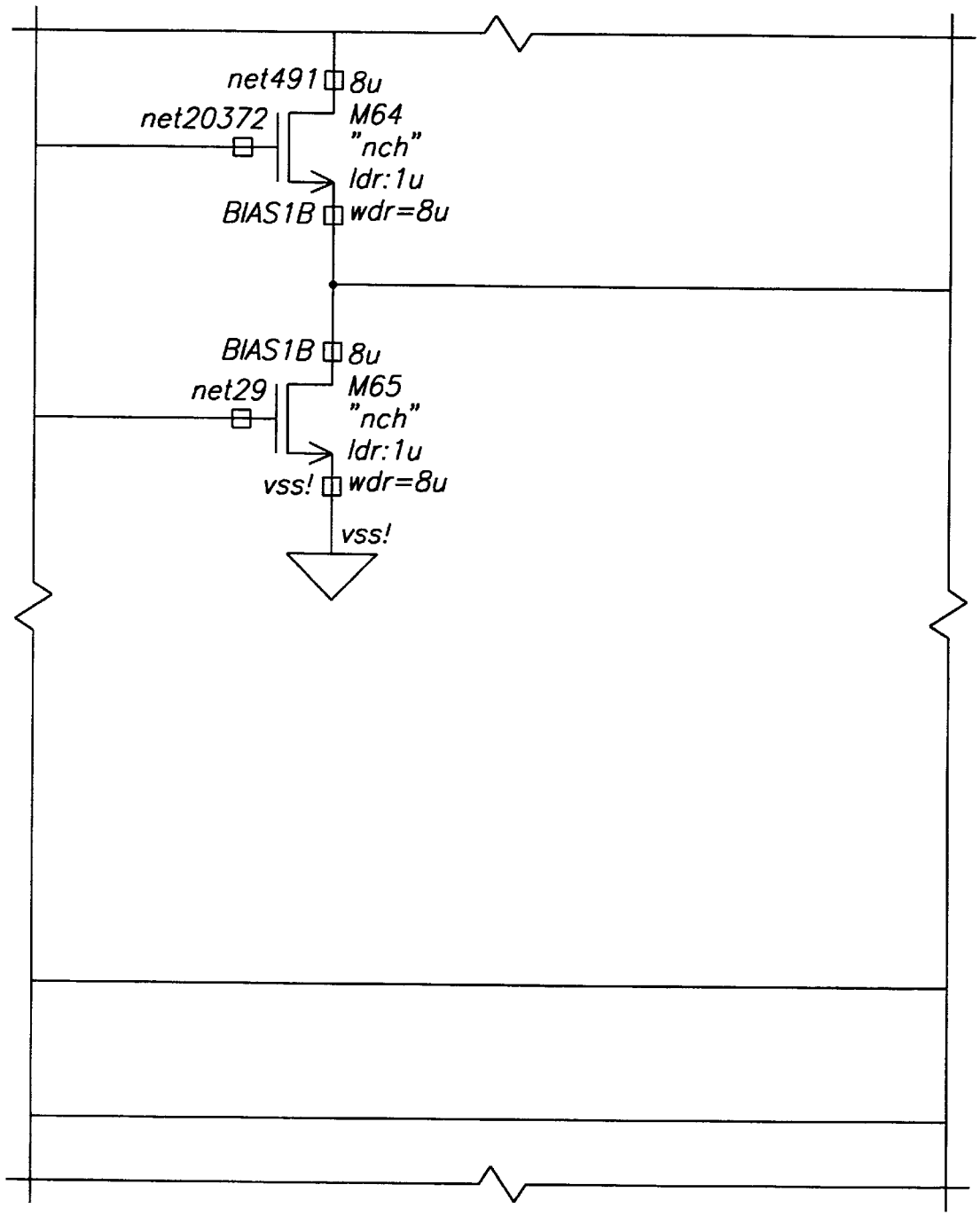
wdr=15u
net506
15u/2u
M48
"nch"
vss!
ldr=2u
vss!
wdr=15u
vss!

Fig 8.0107F6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8u
net20372
M64
"nch"
ldr:1u
BIAS1B
wdr=8u
BIAS1B
8u
net29
M65
"nch"
ldr:1u
vss!
wdr=8u
vss!

Fig 8.0107H

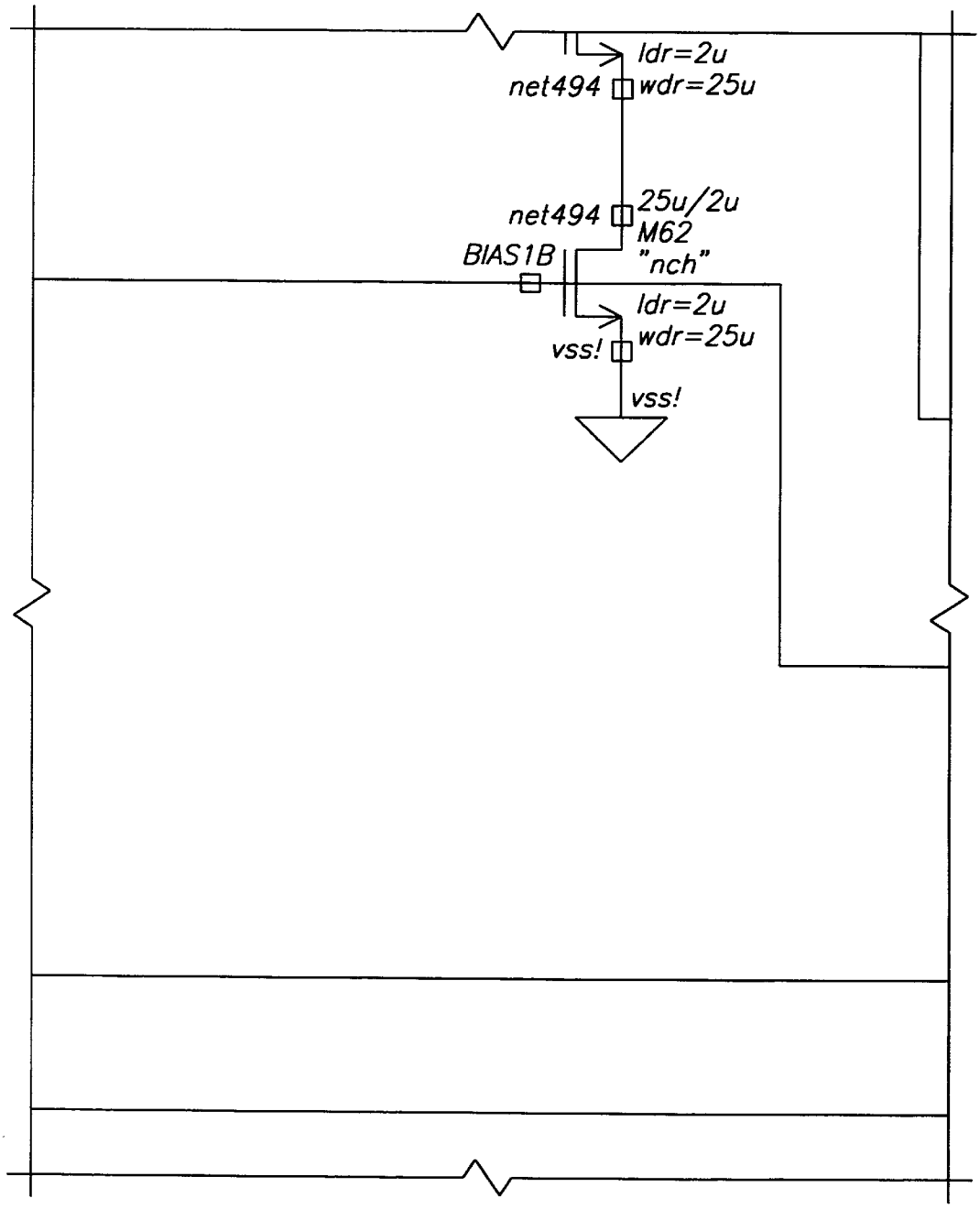
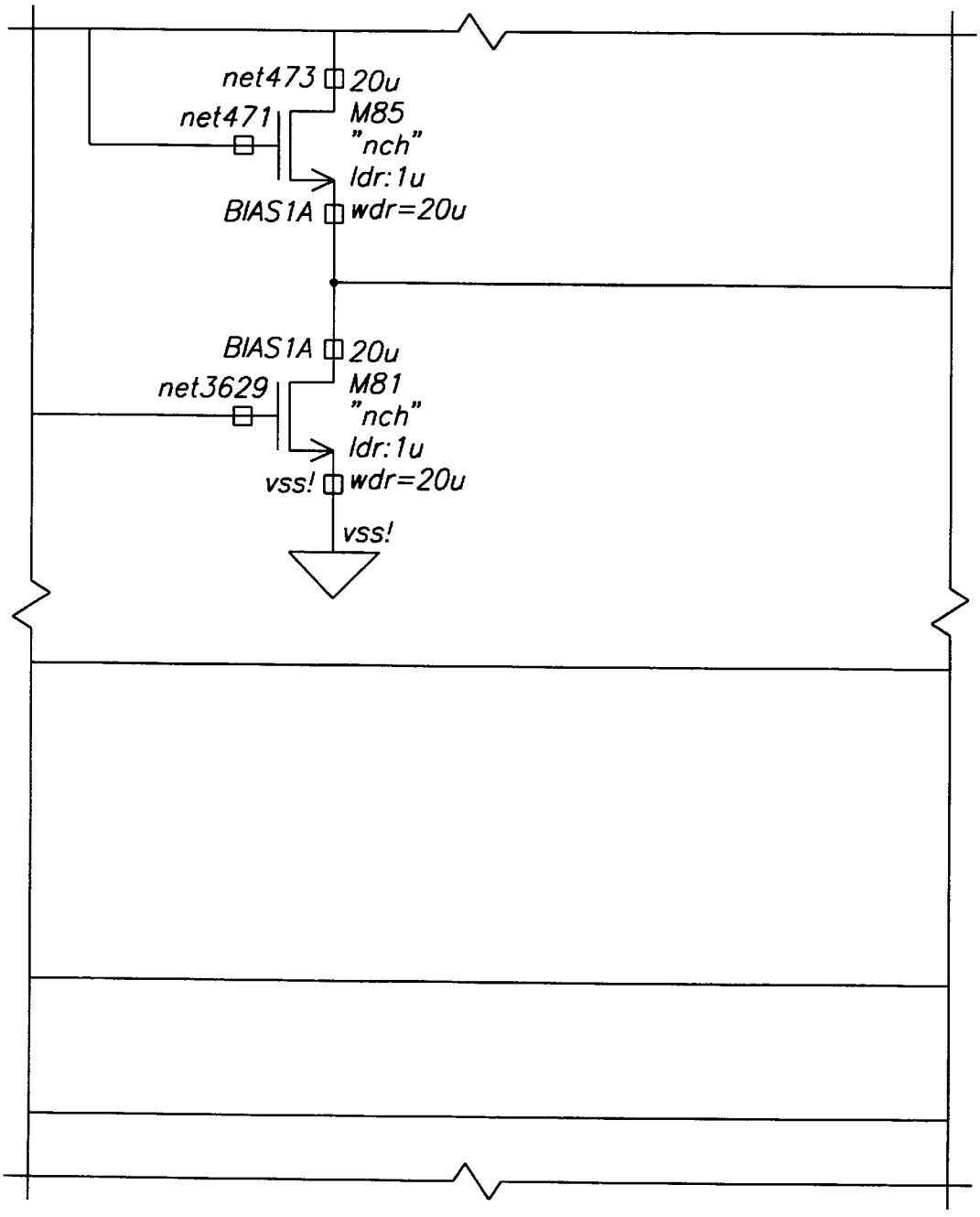


Fig 8.0110FII


net473
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net471
M85
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ldr:1u
BIAS1A
wdr=20u
BIAS1A
20u
net3629
M81
"nch"
ldr:1u
vss!
wdr=20u
vss!

Fig 8.0107Fa

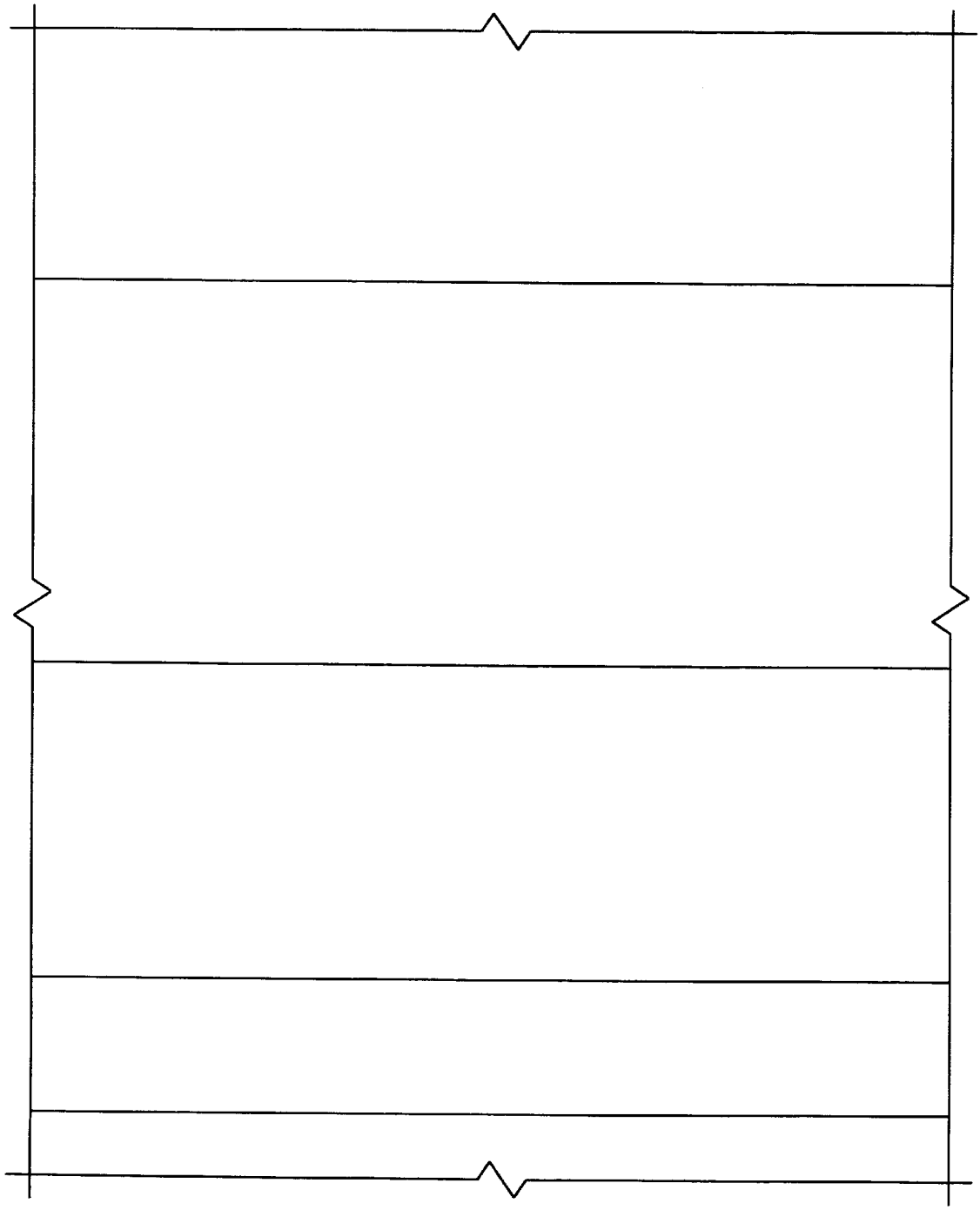


Fig 8.0107FK

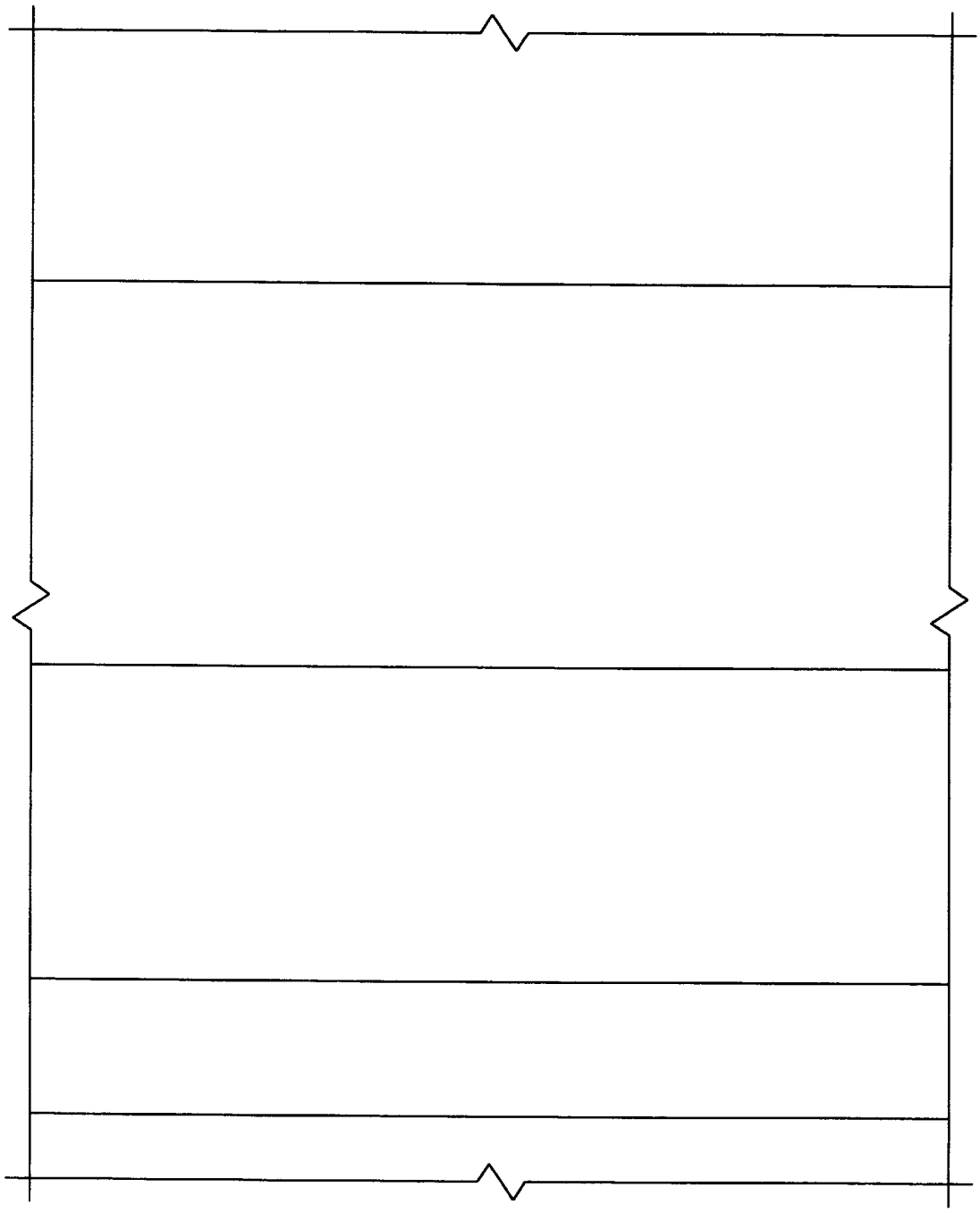
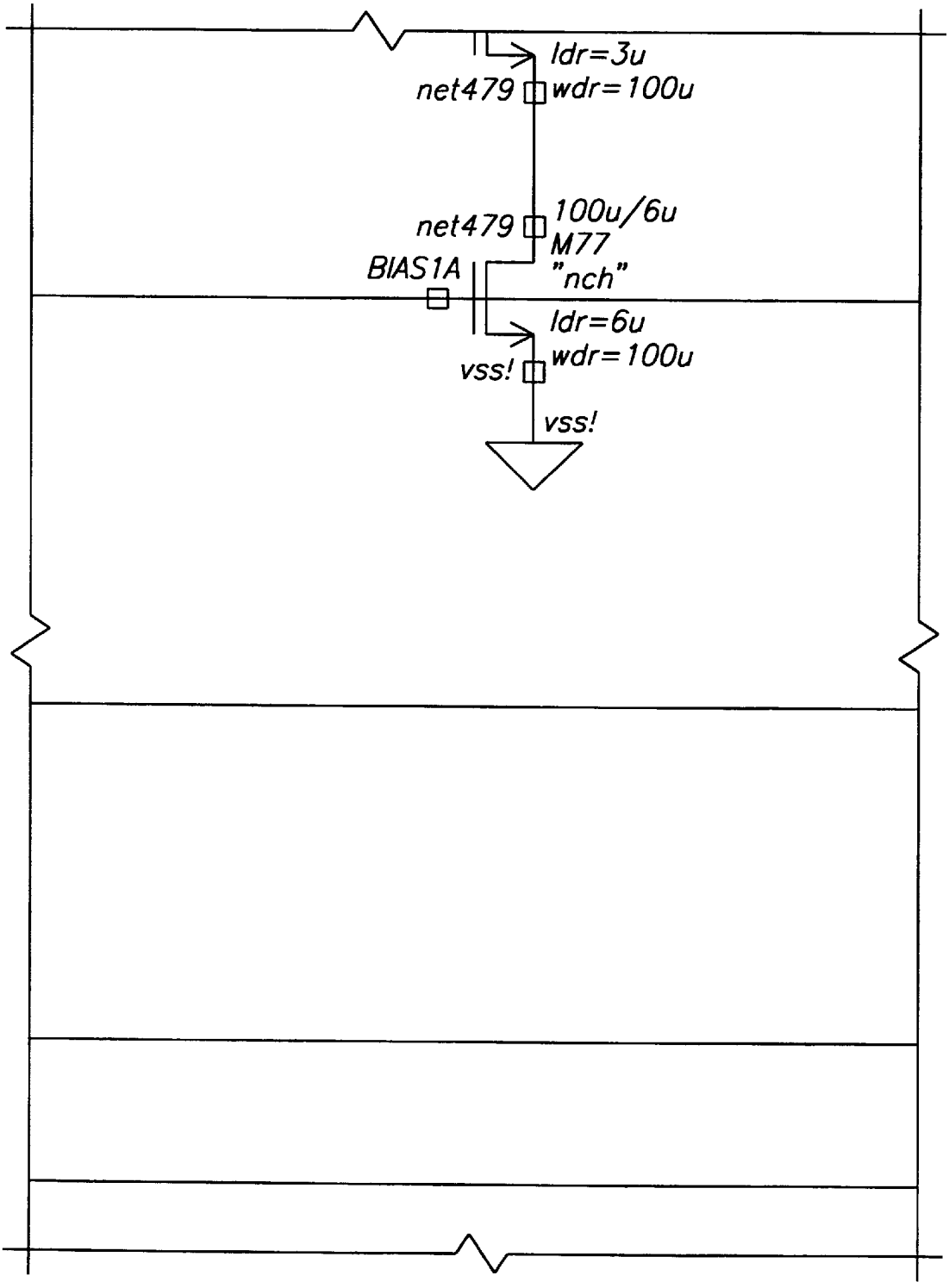


Fig 8.0107fL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wdr=100u
net479
100u/6u
M77
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ldr=6u
wdr=100u
vss!
vss!

Fig 8.0107FM

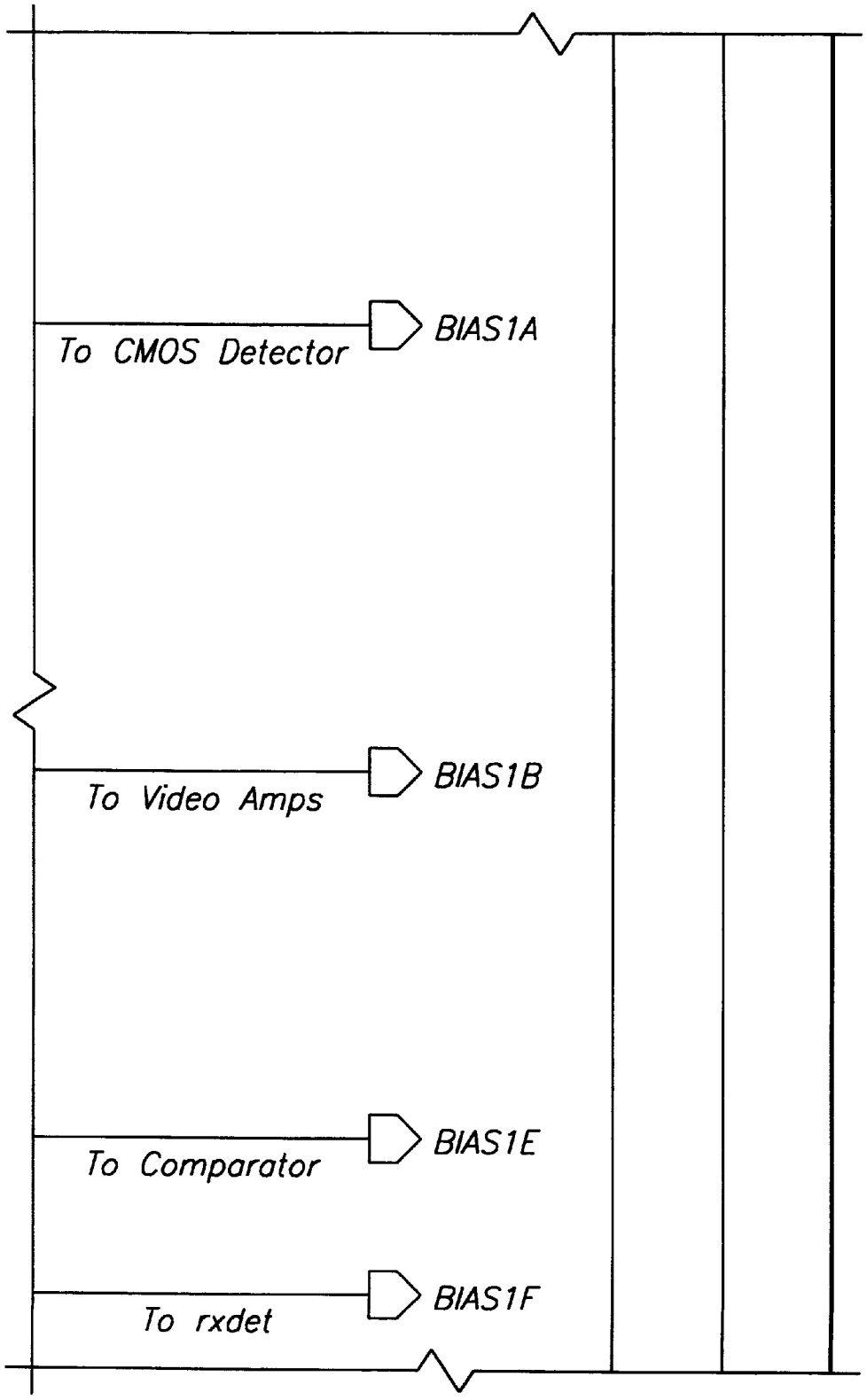


FIG 88.01017FN

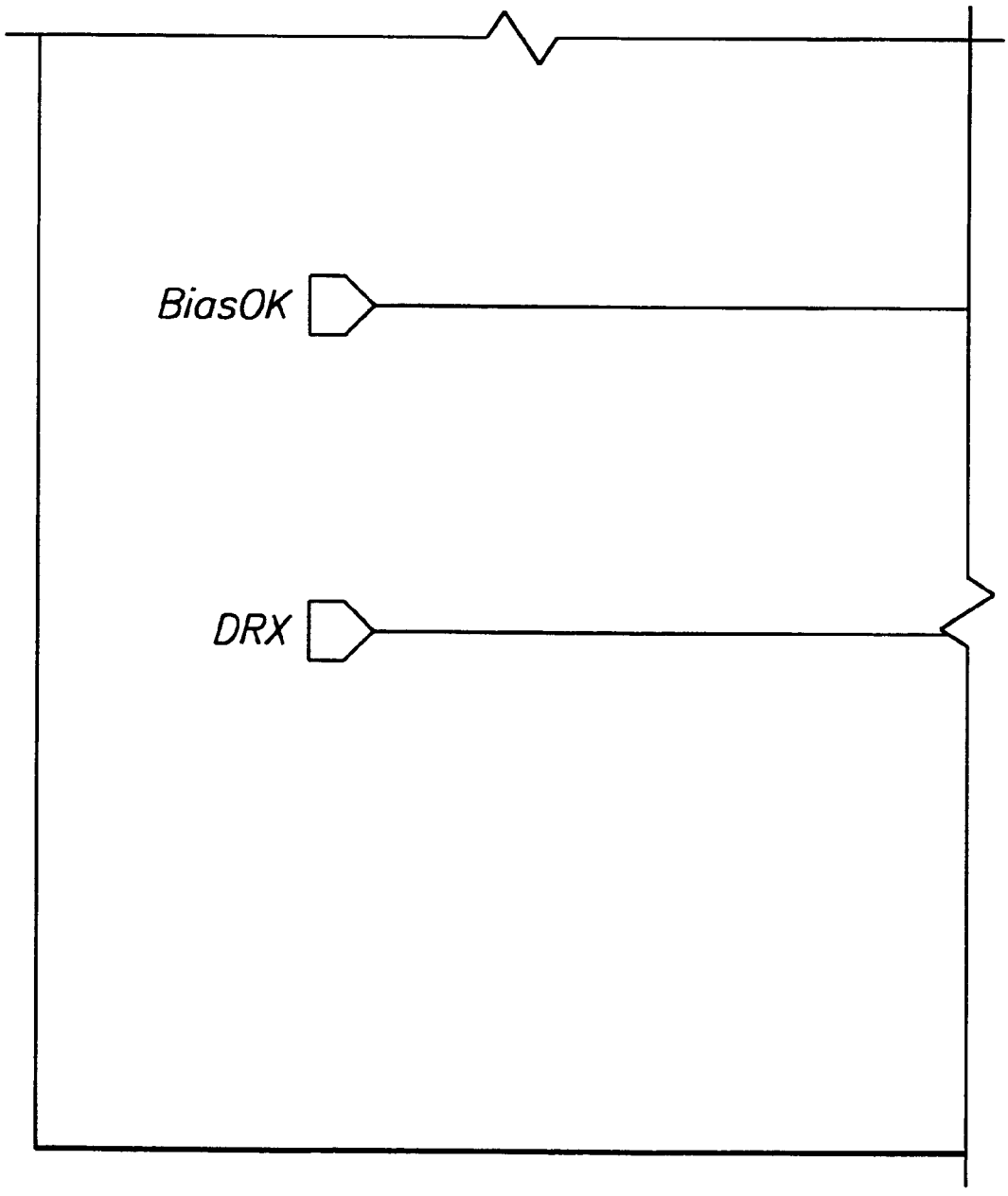


Fig 8.0107GA

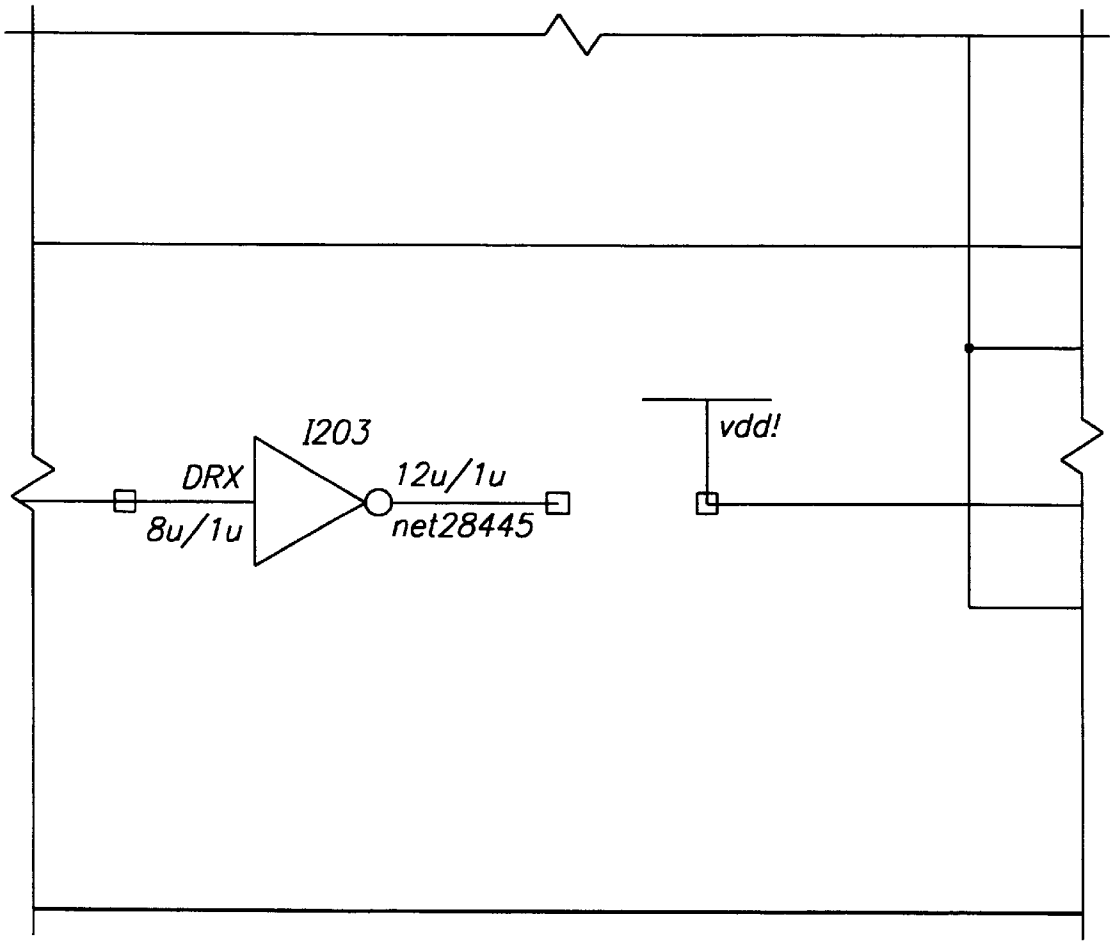


Fig 88.0107GB

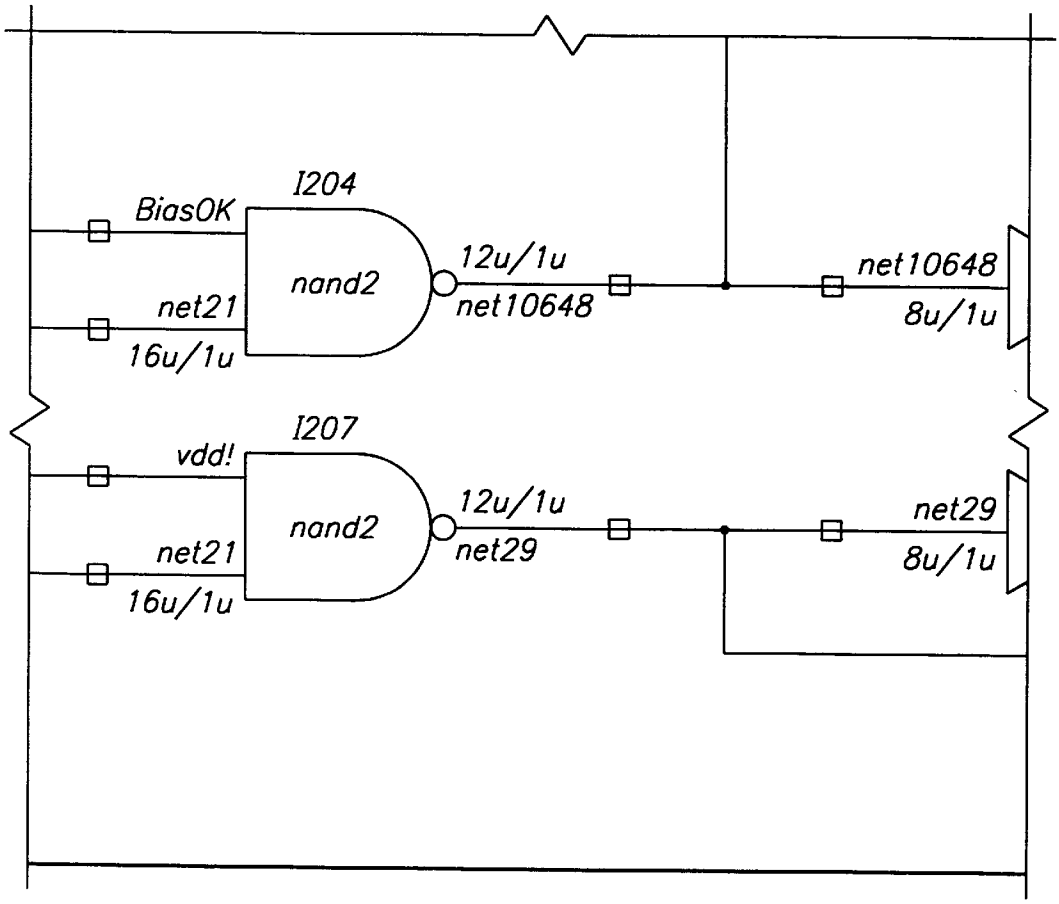

I204
BiasOK
net21
16u/1u
nand2
12u/1u
net10648
net10648
8u/1u
I207
vdd!
net21
16u/1u
nand2
12u/1u
net29
net29
8u/1u

Fig 8.0110

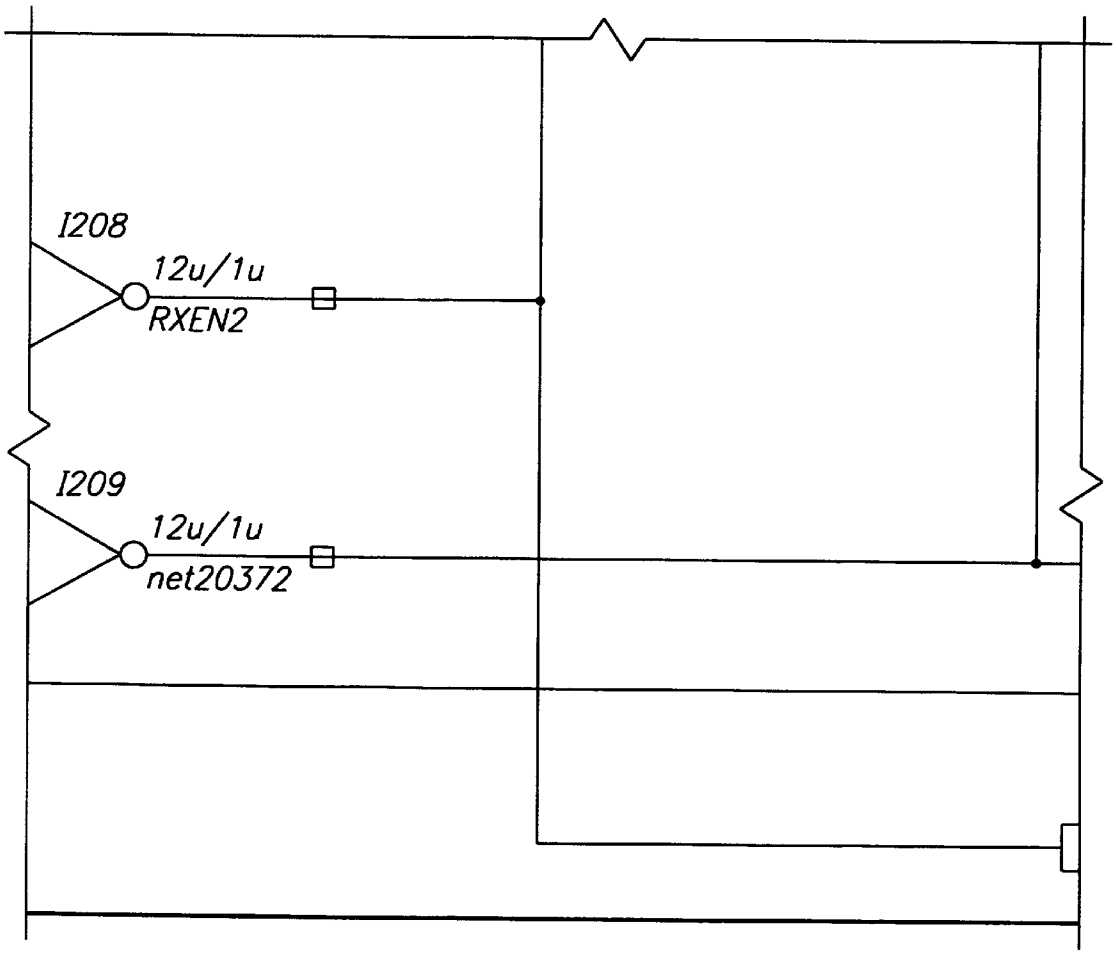


FIG. 8.0100

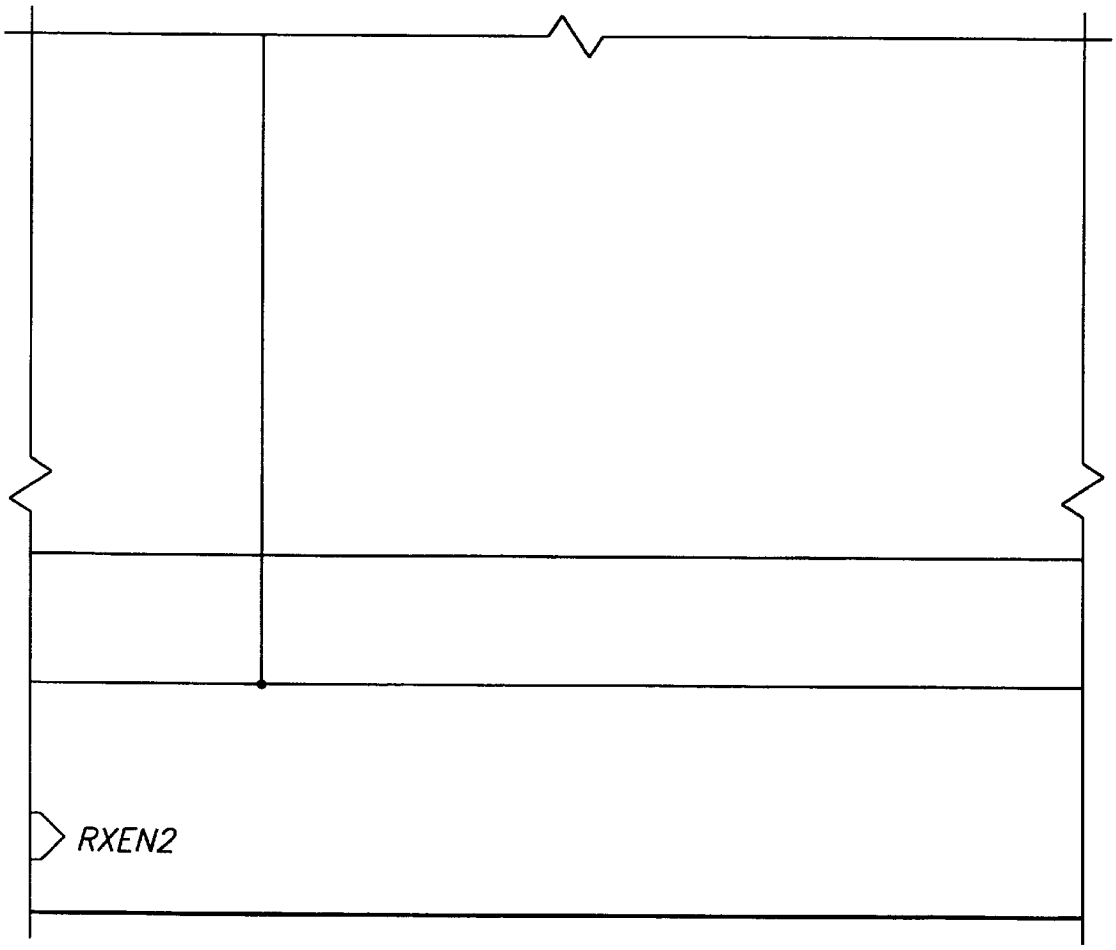


Fig 80106E

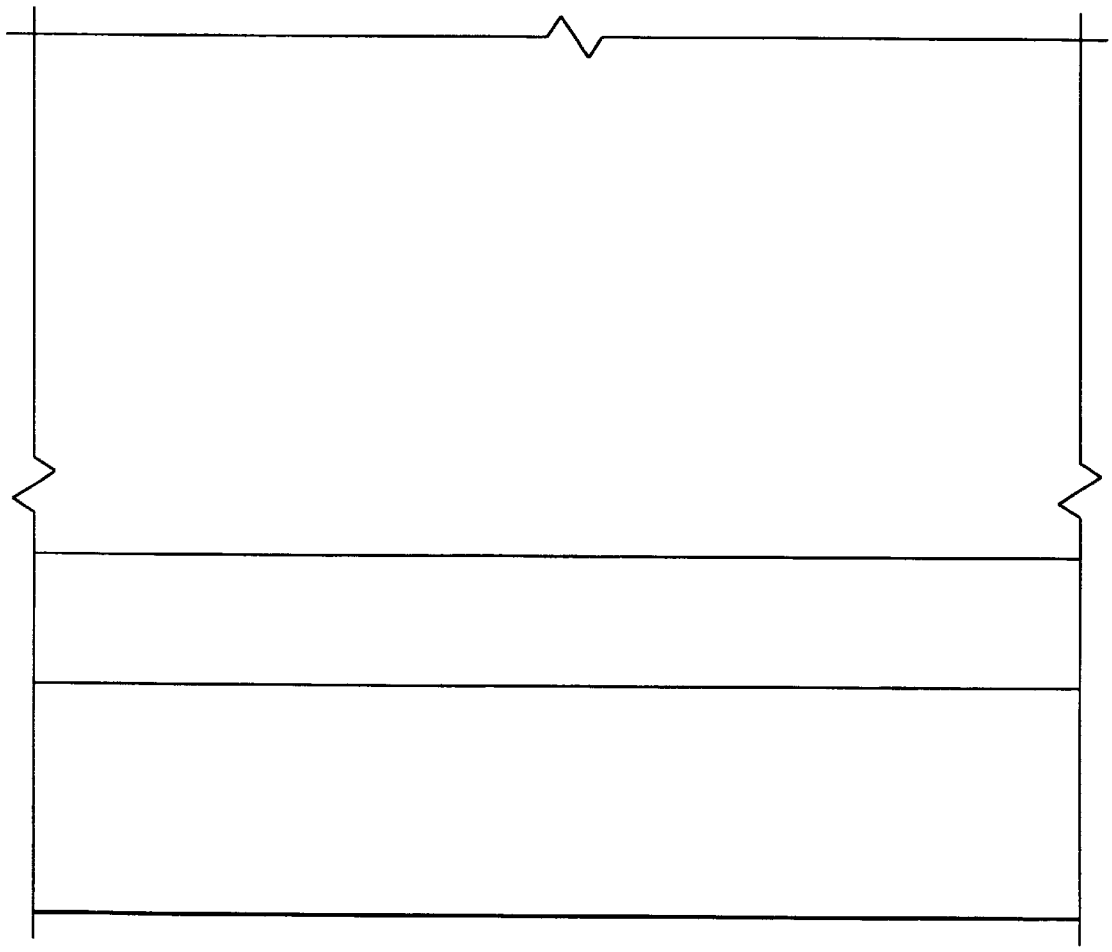


Fig 88.00107GF

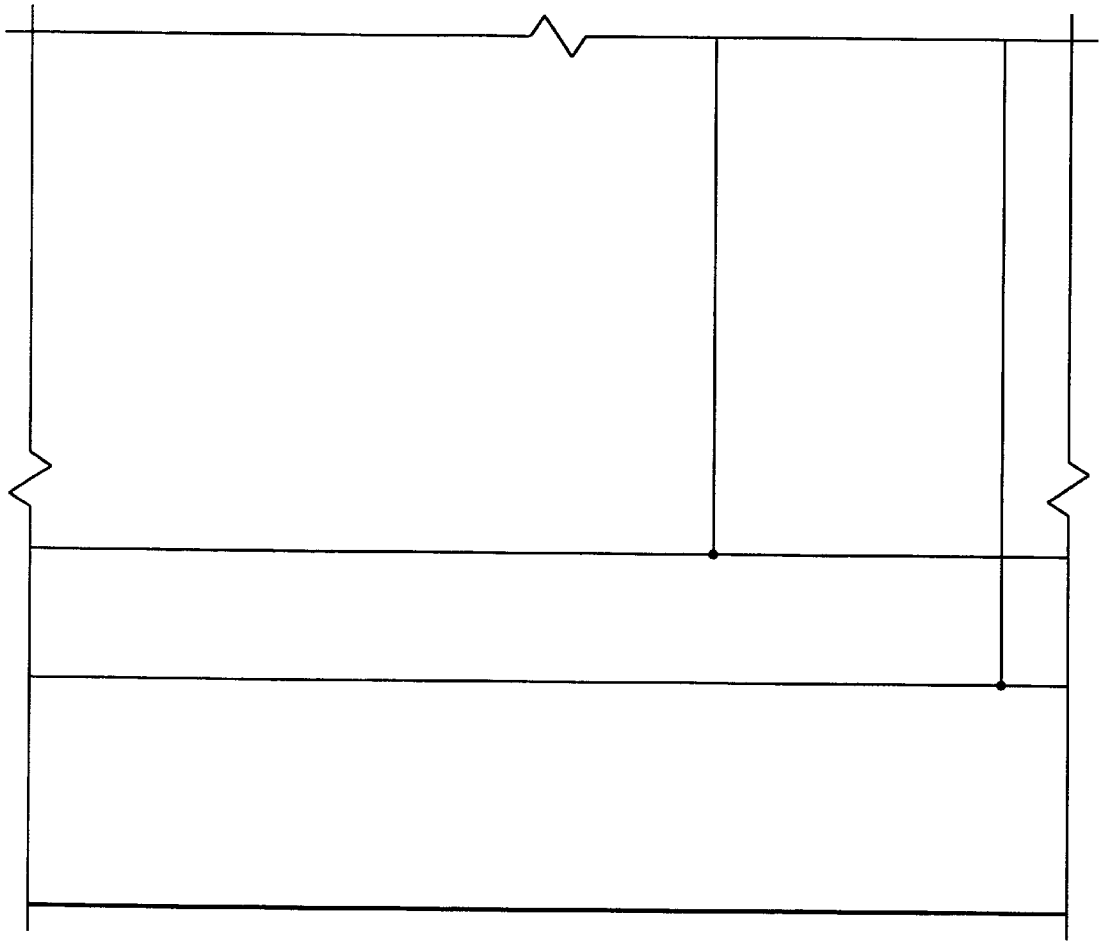


Fig 80107166

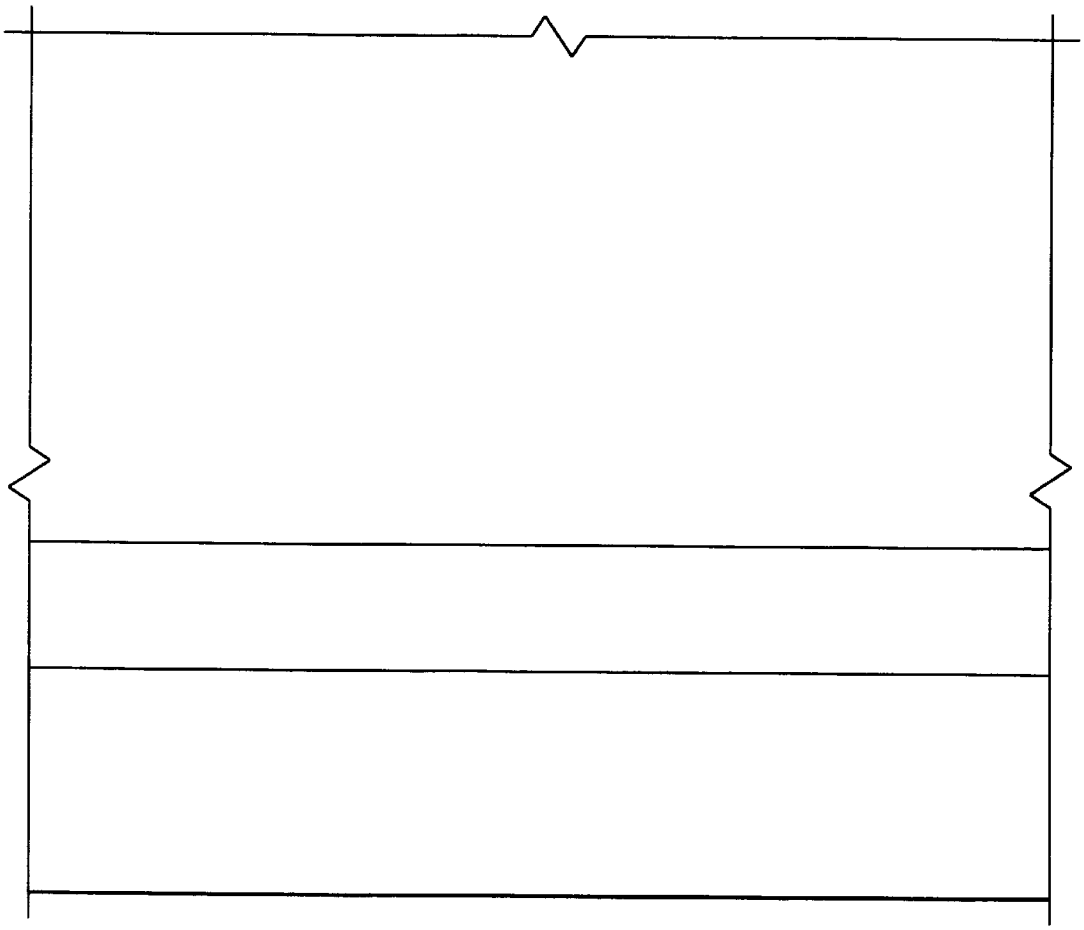


Fig 88.01016H

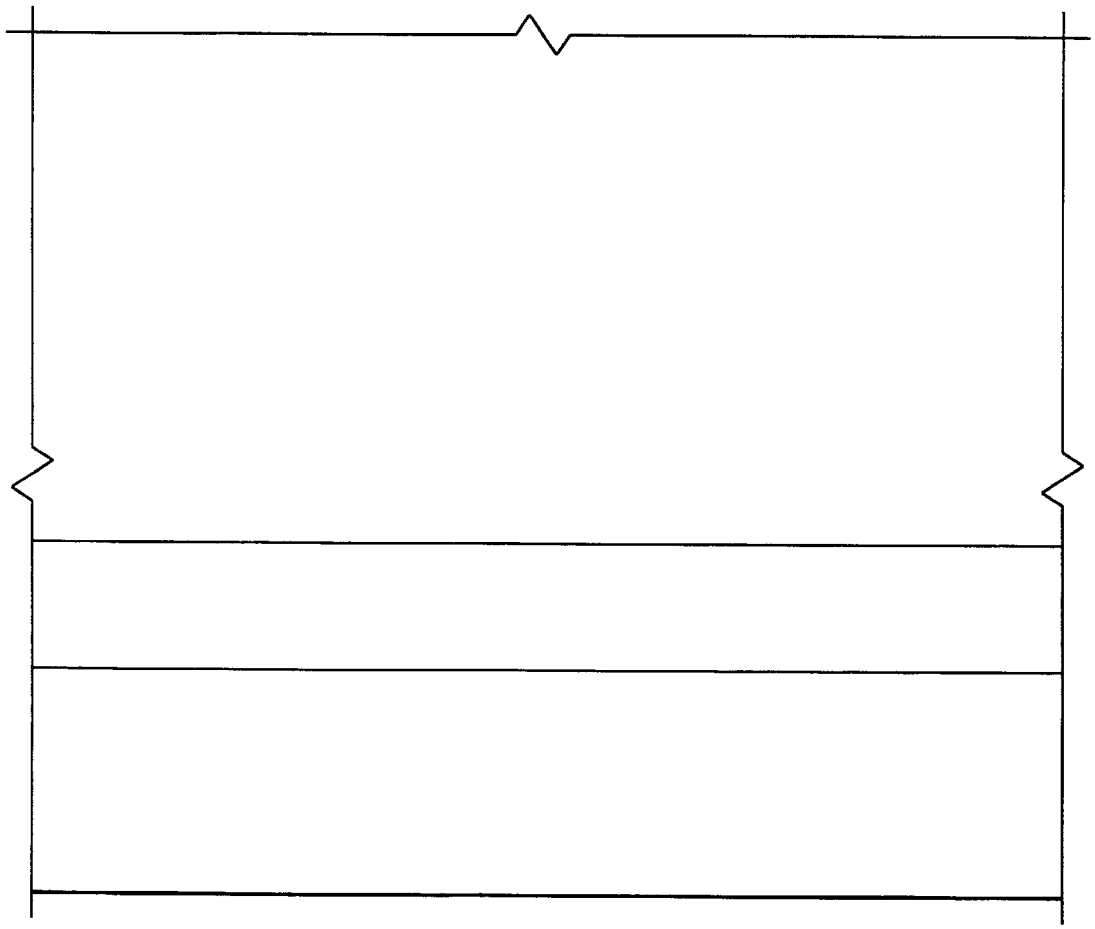


Fig 8.0100761

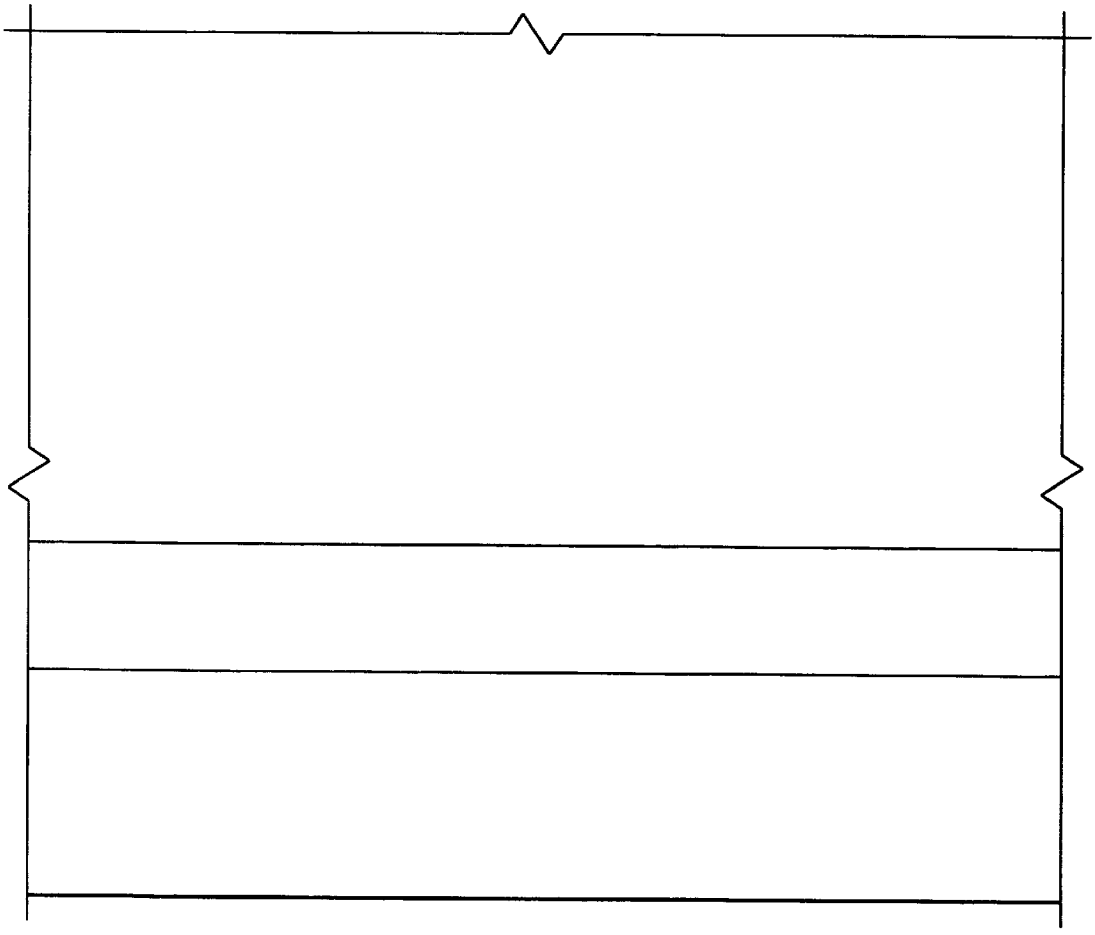


Fig 80107Gal

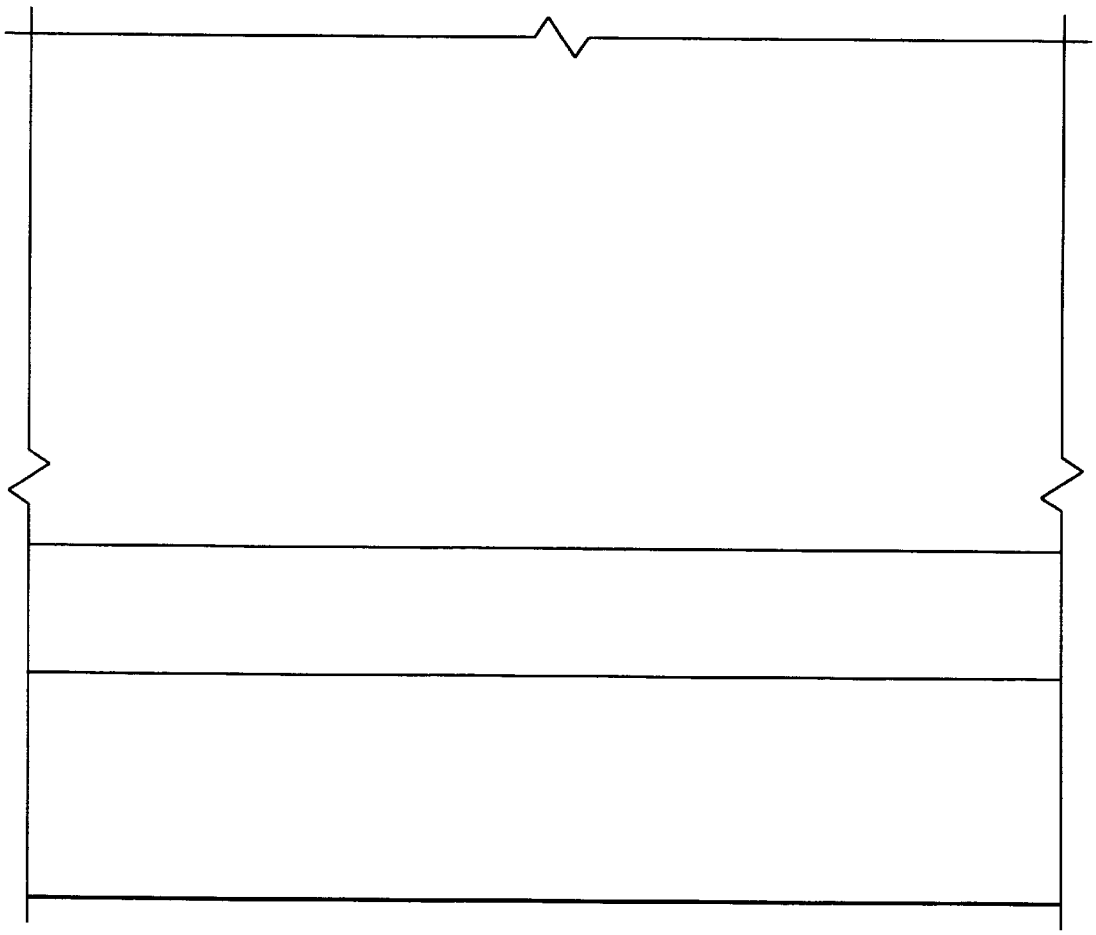


Fig 8.01076K

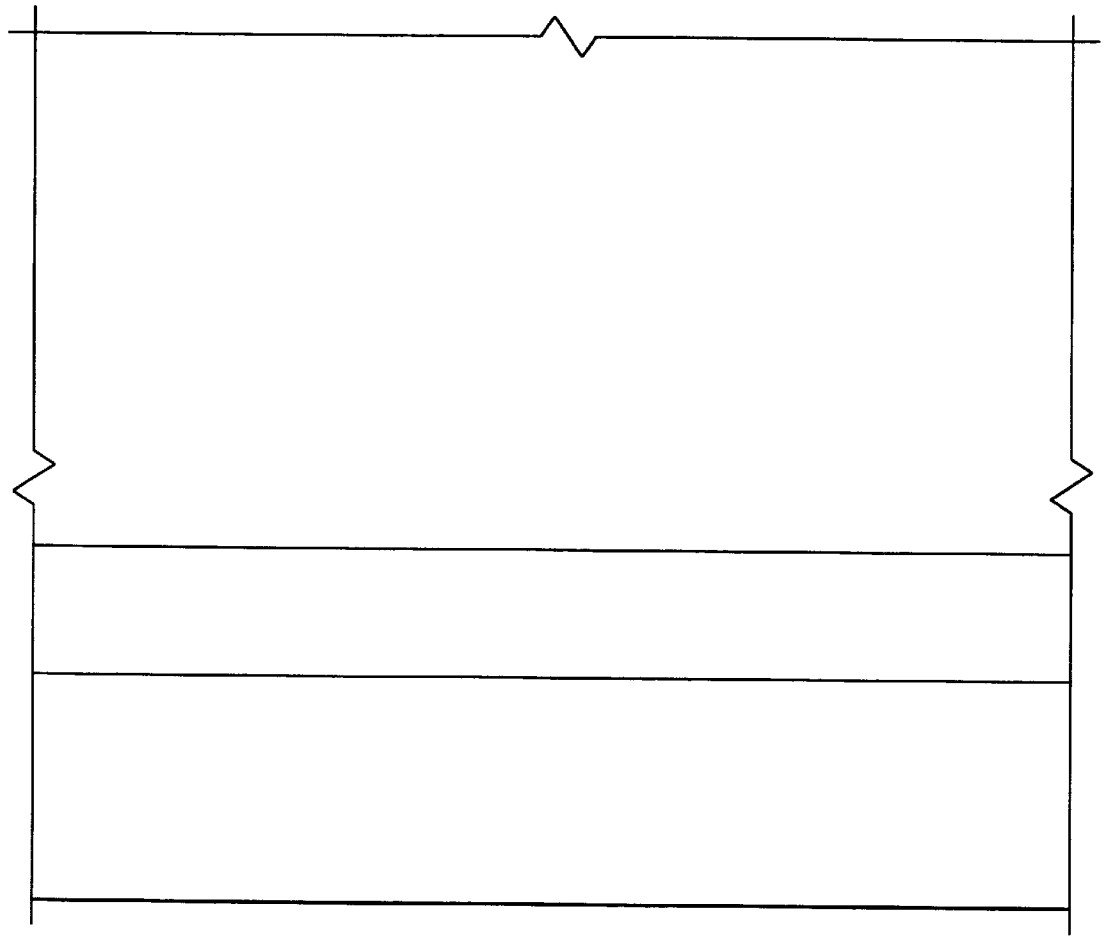


Fig 88.01007161

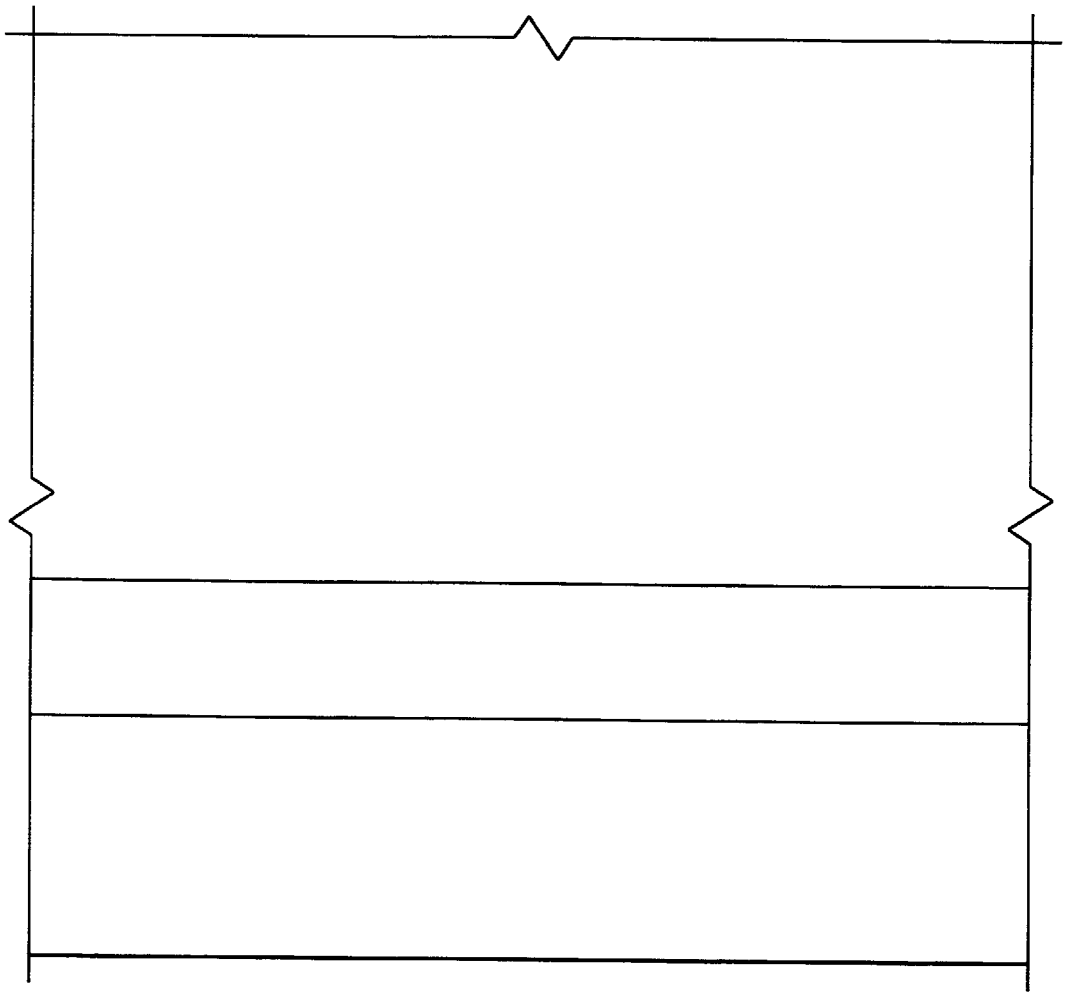


Fig 8.0107GM

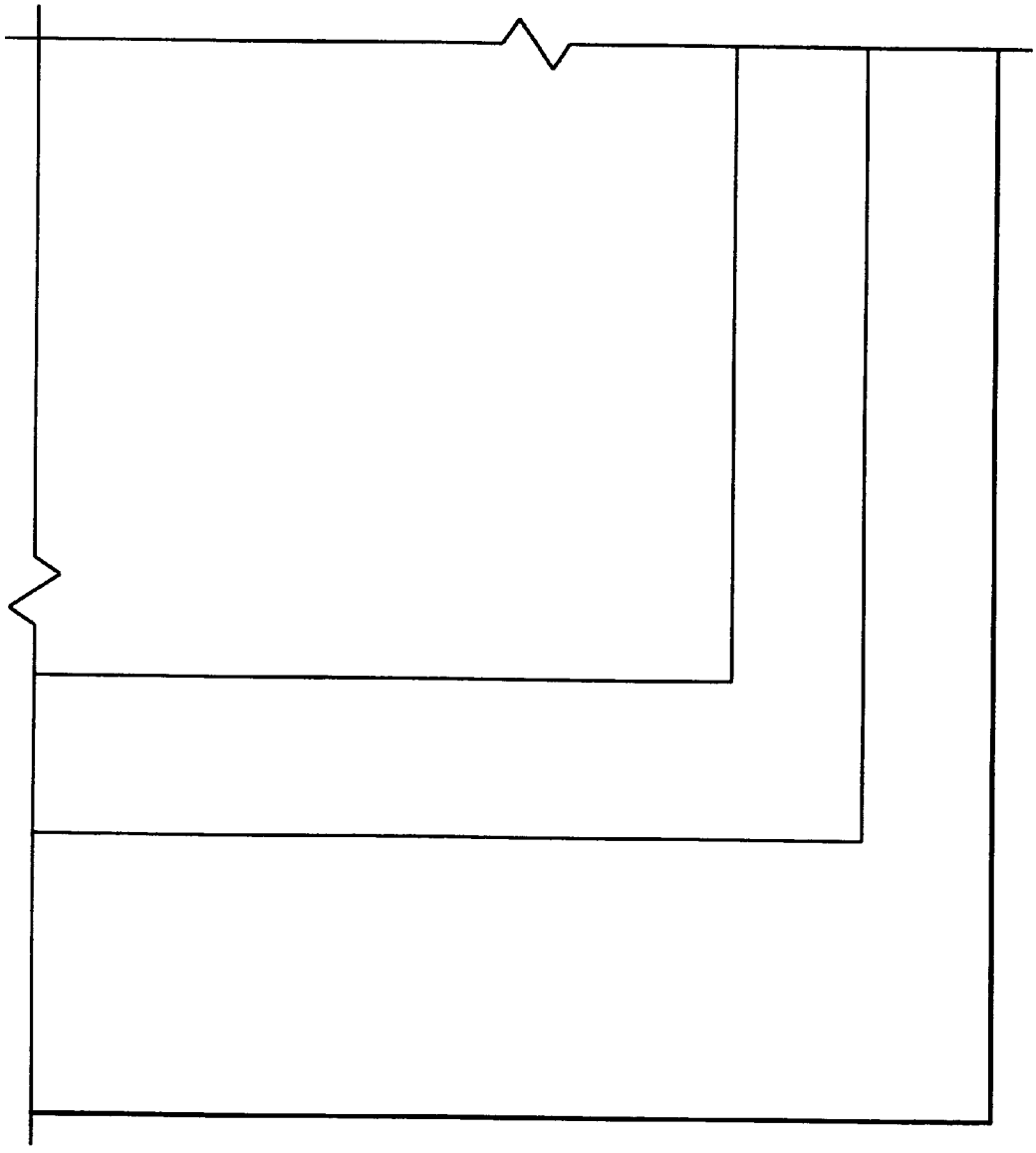


Fig 8.0107GN

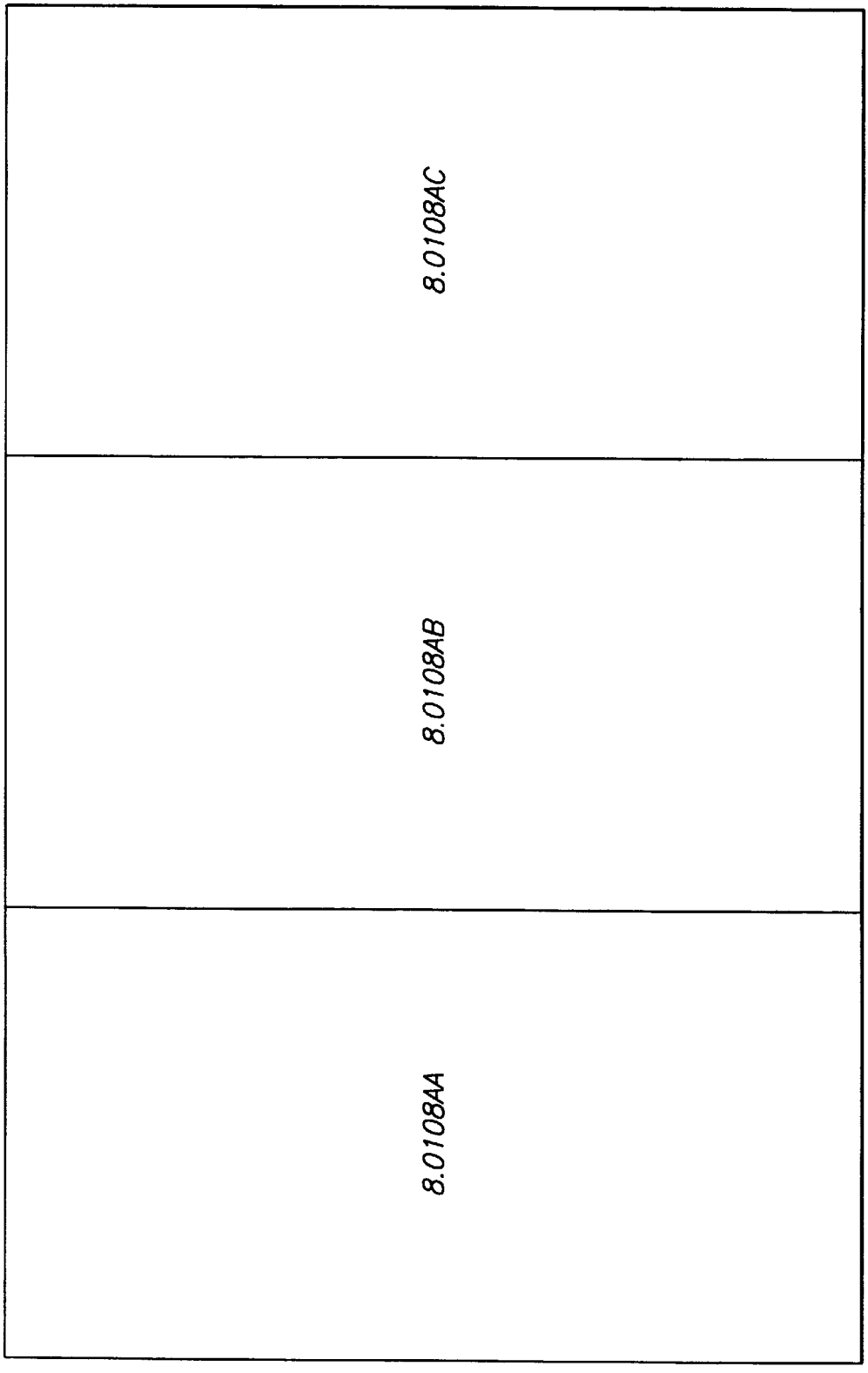


FIG 8.0108B

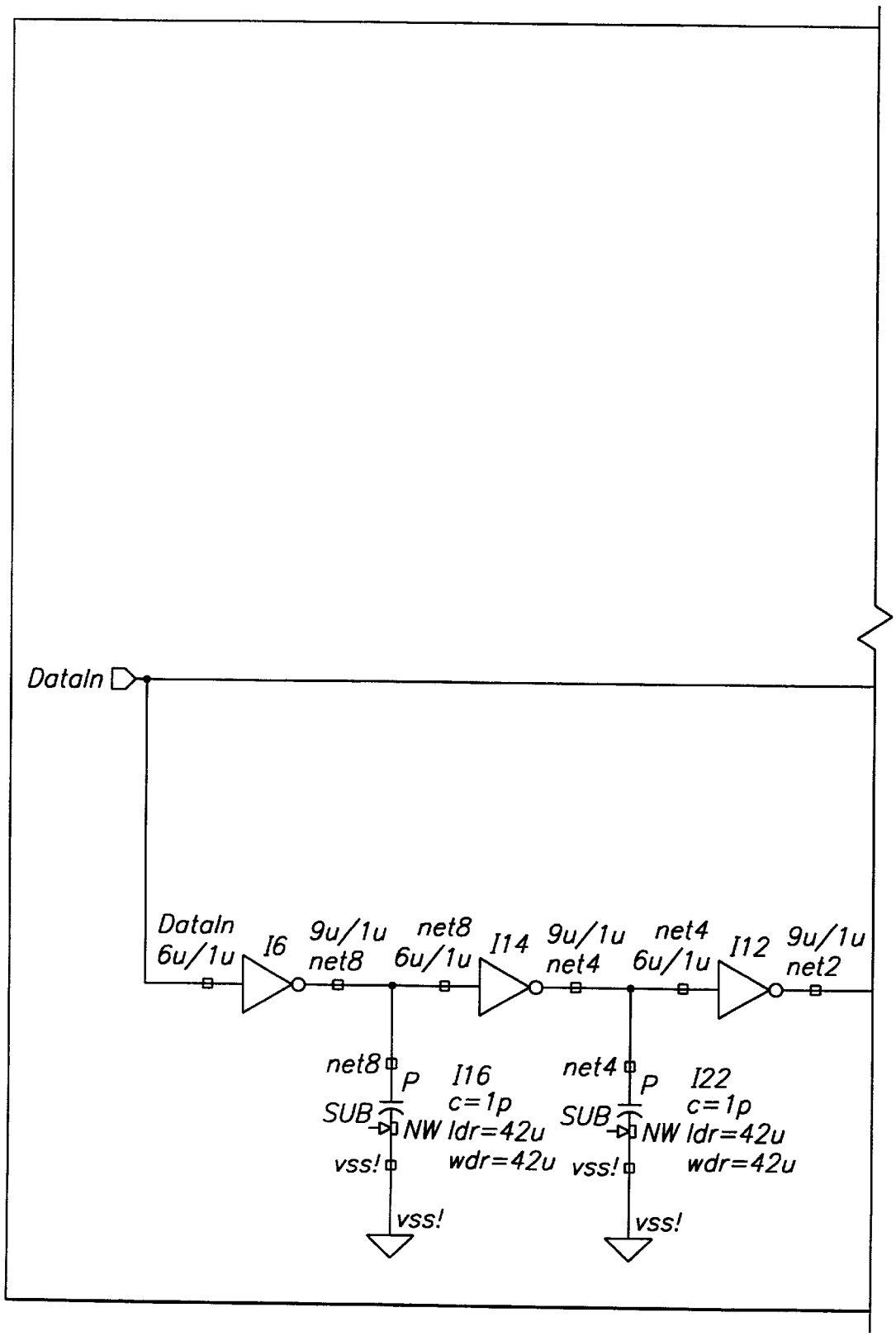

DataIn
DataIn
6u/1u
I6
9u/1u
net8
net8
6u/1u
I14
9u/1u
net4
net4
6u/1u
I12
9u/1u
net2
net8
P
SUB
NW
vss!
I16
c=1p
ldr=42u
wdr=42u
vss!
net4
P
SUB
NW
vss!
I22
c=1p
ldr=42u
wdr=42u
vss!

Fig 8.0108AA

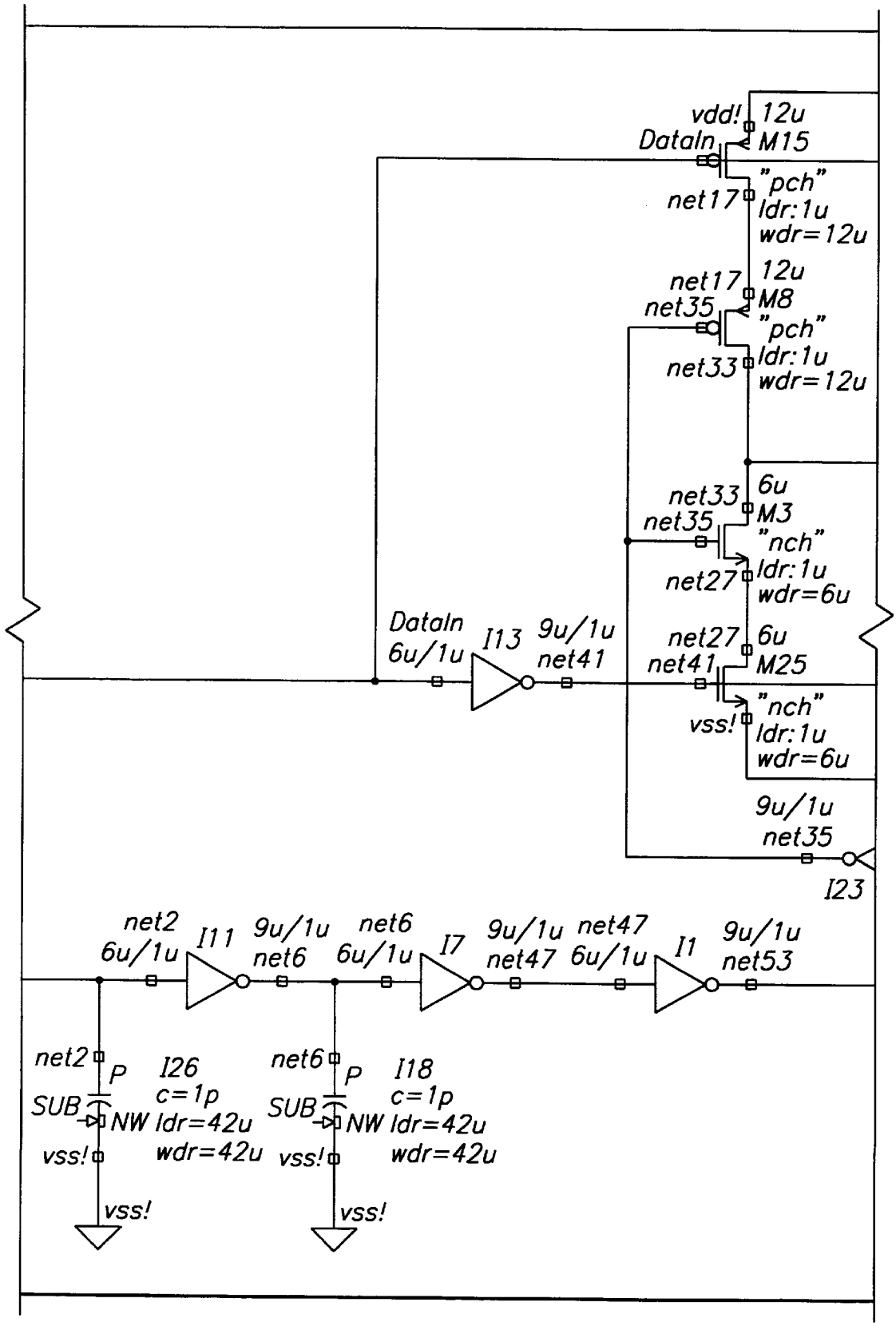


Fig 8.01080AB

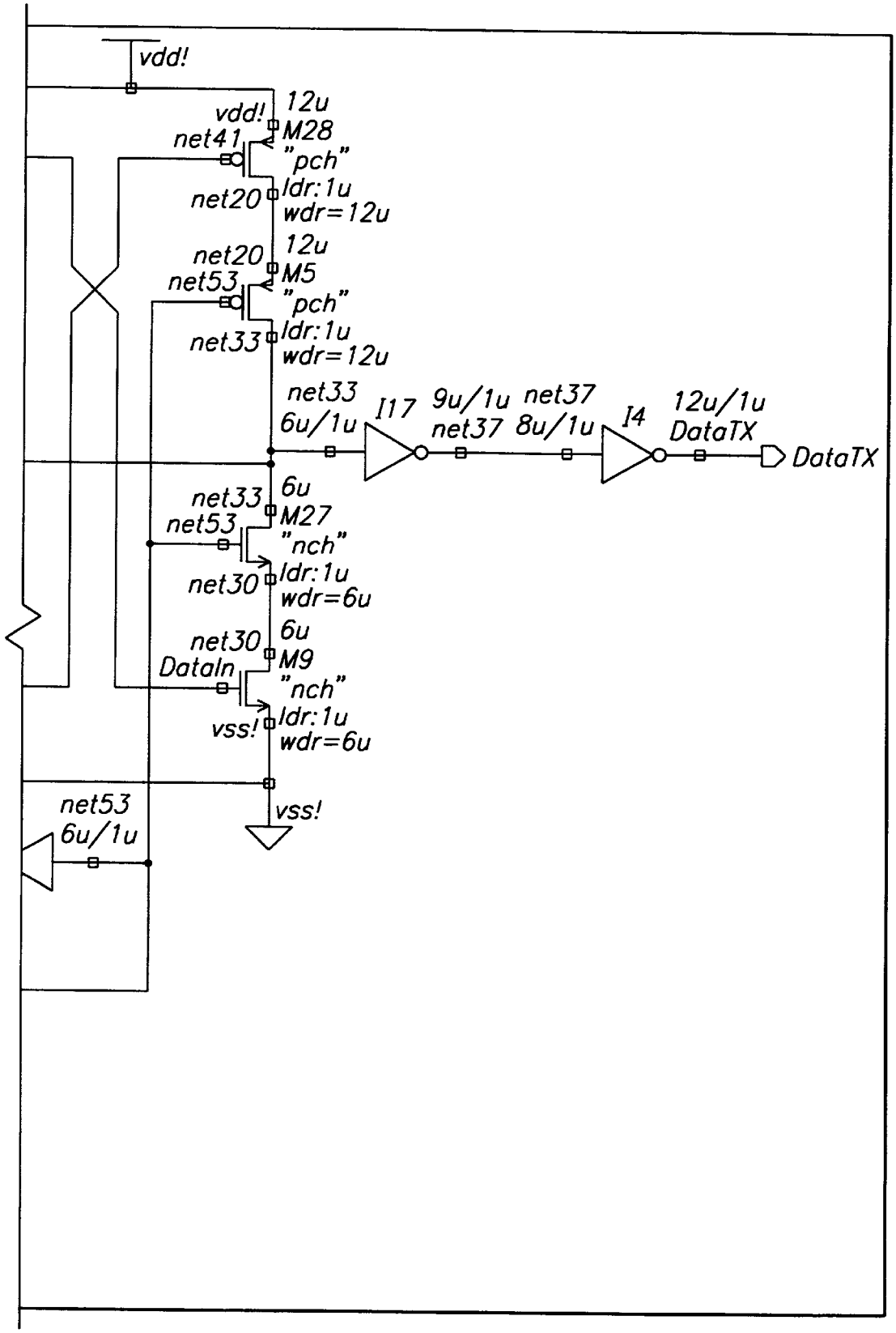
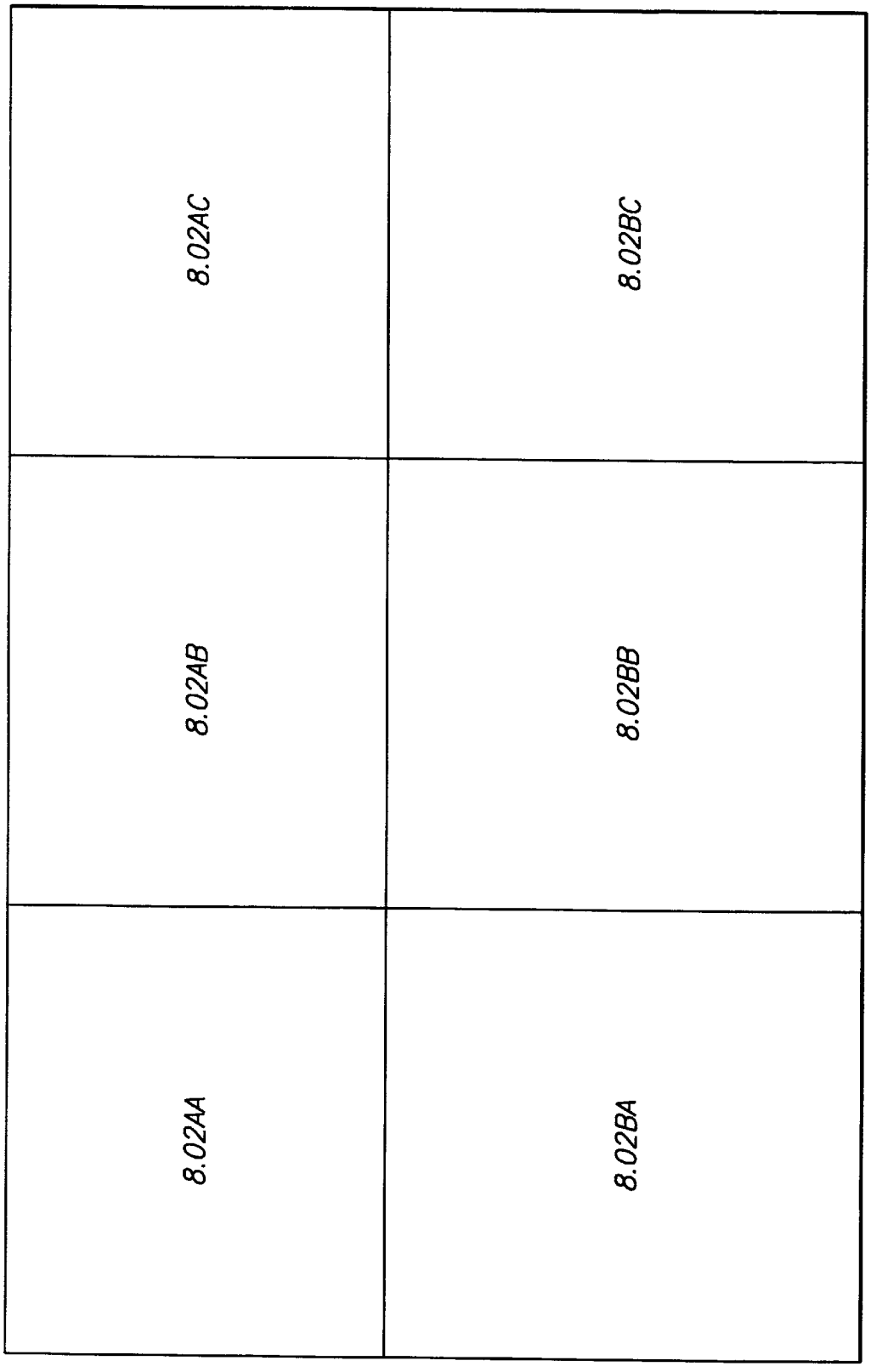
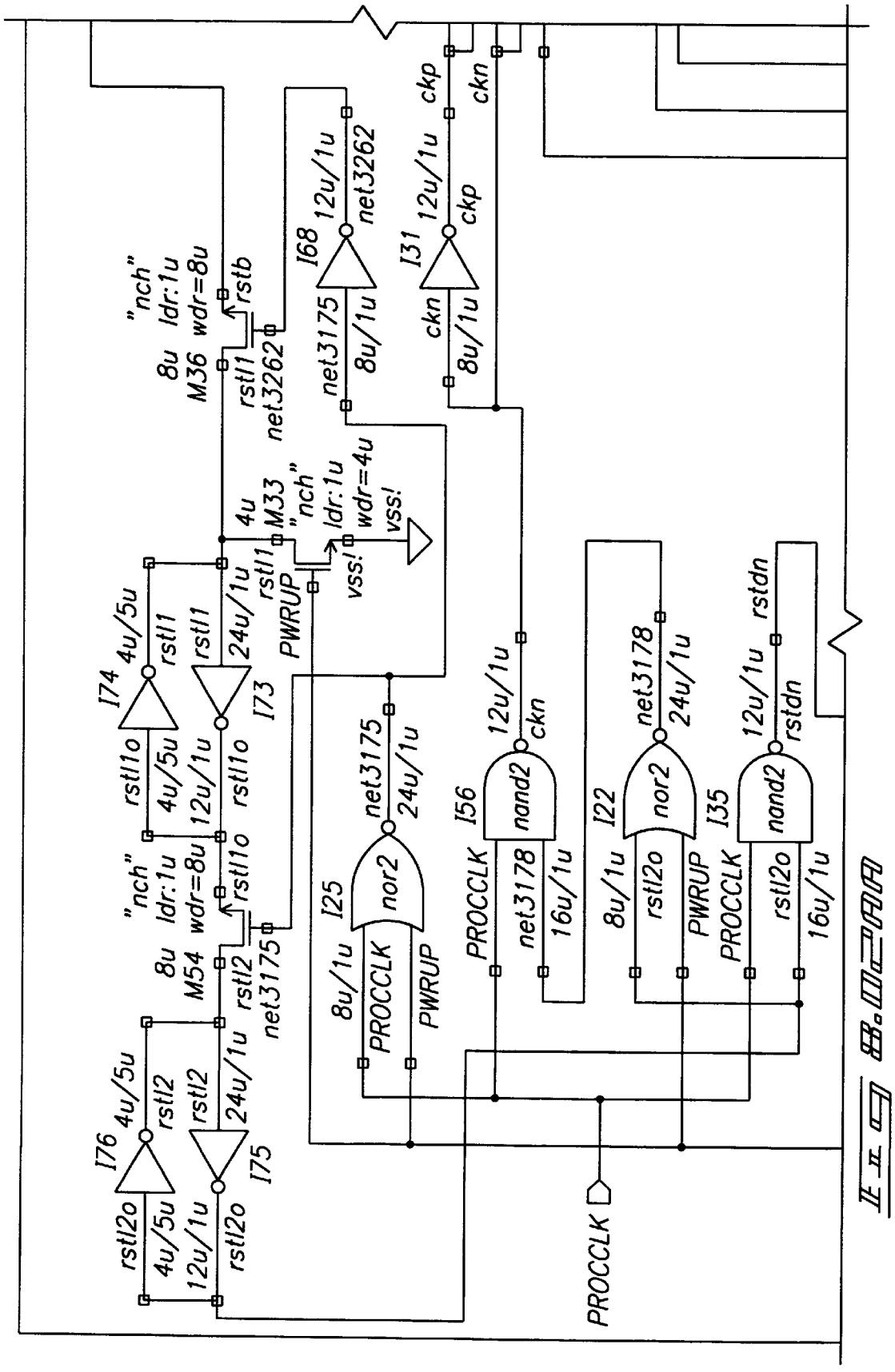


Fig 8.01088AC


8.02AC
8.02BC
8.02AB
8.02BB
8.02AA
8.02BA
FIG. 8.02


"nch"
ldr:1u
wdr=8u
8u
M36
rstb
rstl1
net3262
I68
12u/1u
net3262
net3175
8u/1u
I31
12u/1u
ckp
ckn
ckn
8u/1u
ckp
ckn
4u
M33
"nch"
ldr:1u
wdr=4u
vss!
vss!
PWRUP
rstl1
24u/1u
I73
I74
4u/5u
rstl1
rstl1
4u/5u
rstl1o
"nch"
ldr:1u
wdr=8u
8u
M54
rstl1o
rstl2
net3175
12u/1u
rstl1o
4u/5u
rstl1o
I25
nor2
net3175
24u/1u
8u/1u
PROCCLK
PWRUP
I56
nand2
12u/1u
ckn
PROCCLK
net3178
16u/1u
I22
nor2
net3178
24u/1u
8u/1u
rstl2o
PWRUP
PROCCLK
I35
nand2
12u/1u
rstdn
rstdn
rstl2o
16u/1u
I76
4u/5u
rstl2
rstl2
24u/1u
I75
rstl2o
4u/5u
12u/1u
rstl2o
PROCCLK

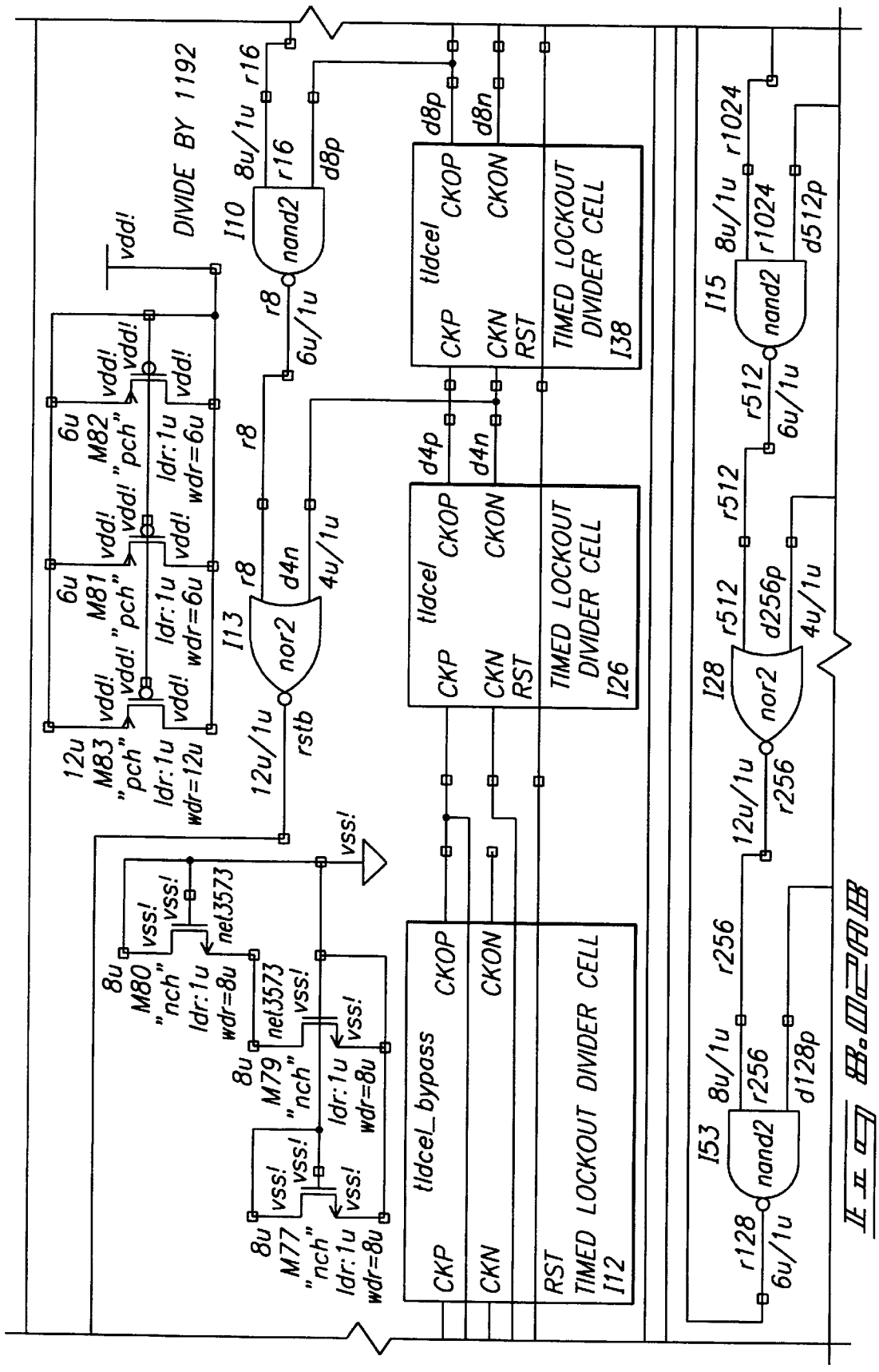

DIVIDE BY 1192
vdd!
vss!
I10 8u/1u r16 nand2 r16 d8p
r8 6u/1u
I13 r8 d4n 4u/1u nor2
12u/1u rstb
12u M83 "pch" ldr:1u wdr=12u
6u M81 "pch" ldr:1u wdr=6u
6u M82 "pch" ldr:1u wdr=6u
8u M80 "nch" ldr:1u wdr=8u net3573
8u M79 "nch" ldr:1u wdr=8u net3573
8u M77 "nch" ldr:1u wdr=8u
tldceI CKP CKN RST CKOP CKON TIMED LOCKOUT DIVIDER CELL I38
tldceI CKP CKN RST CKOP CKON TIMED LOCKOUT DIVIDER CELL I26
tldceI_bypass CKP CKN CKOP CKON RST TIMED LOCKOUT DIVIDER CELL I12
d8p d8n d4p d4n
I15 8u/1u r1024 nand2 r1024 d512p
r512 6u/1u
I28 r512 d256p 4u/1u nor2
12u/1u r256
I53 8u/1u r256 nand2 r256 d128p
r128 6u/1u

FIG. 1301

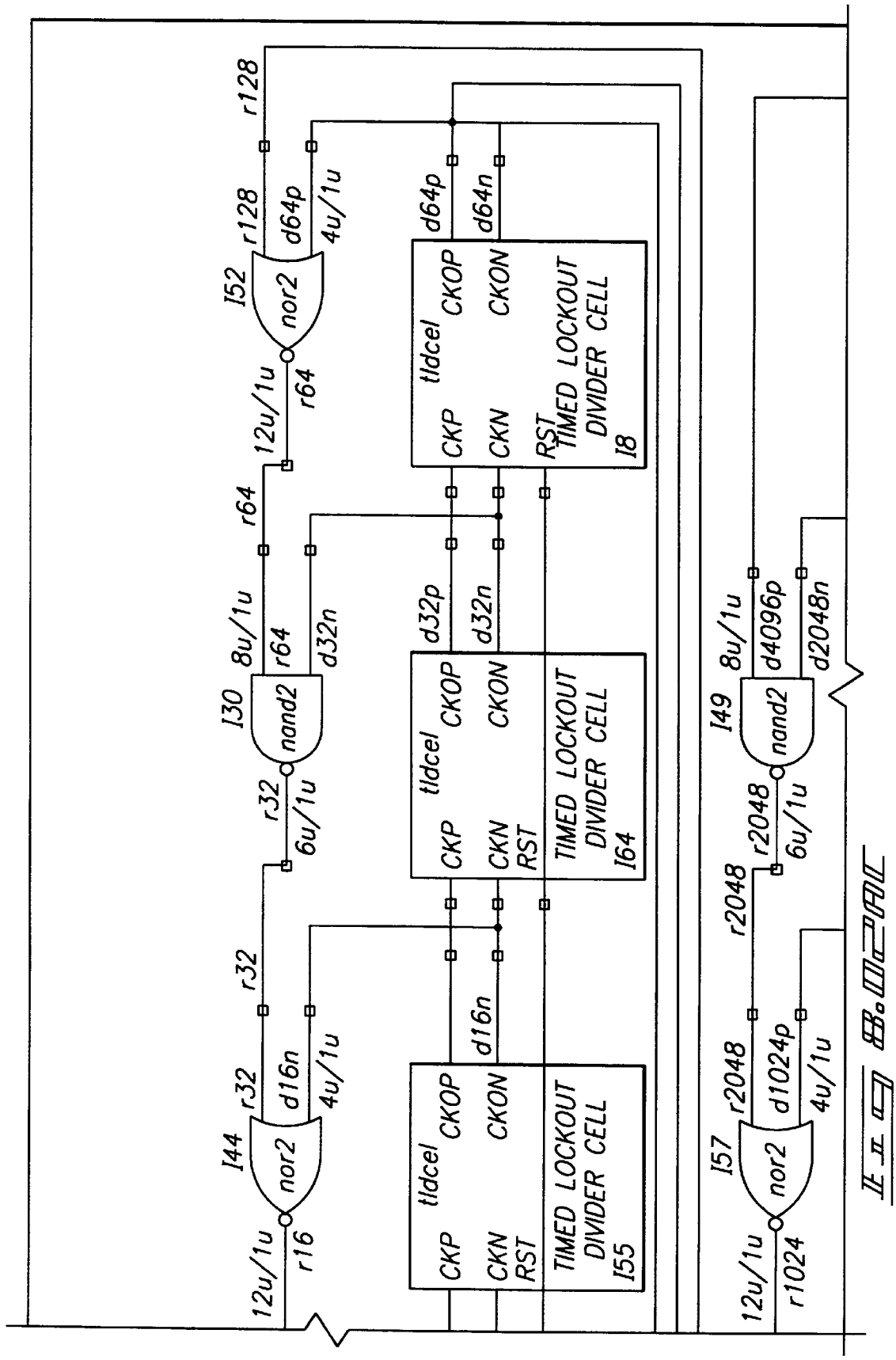

r128
I52
nor2
r128
d64p
4u/1u
12u/1u
r64
r64
I30
nand2
8u/1u
r64
d32n
r32
6u/1u
r32
I44
nor2
r32
d16n
4u/1u
12u/1u
r16
tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I55
d16n
tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I64
d32p
d32n
tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I8
d64p
d64n
I49
nand2
8u/1u
d4096p
d2048n
r2048
6u/1u
r2048
I57
nor2
r2048
d1024p
4u/1u
12u/1u
r1024

FIG. 88.00PAC

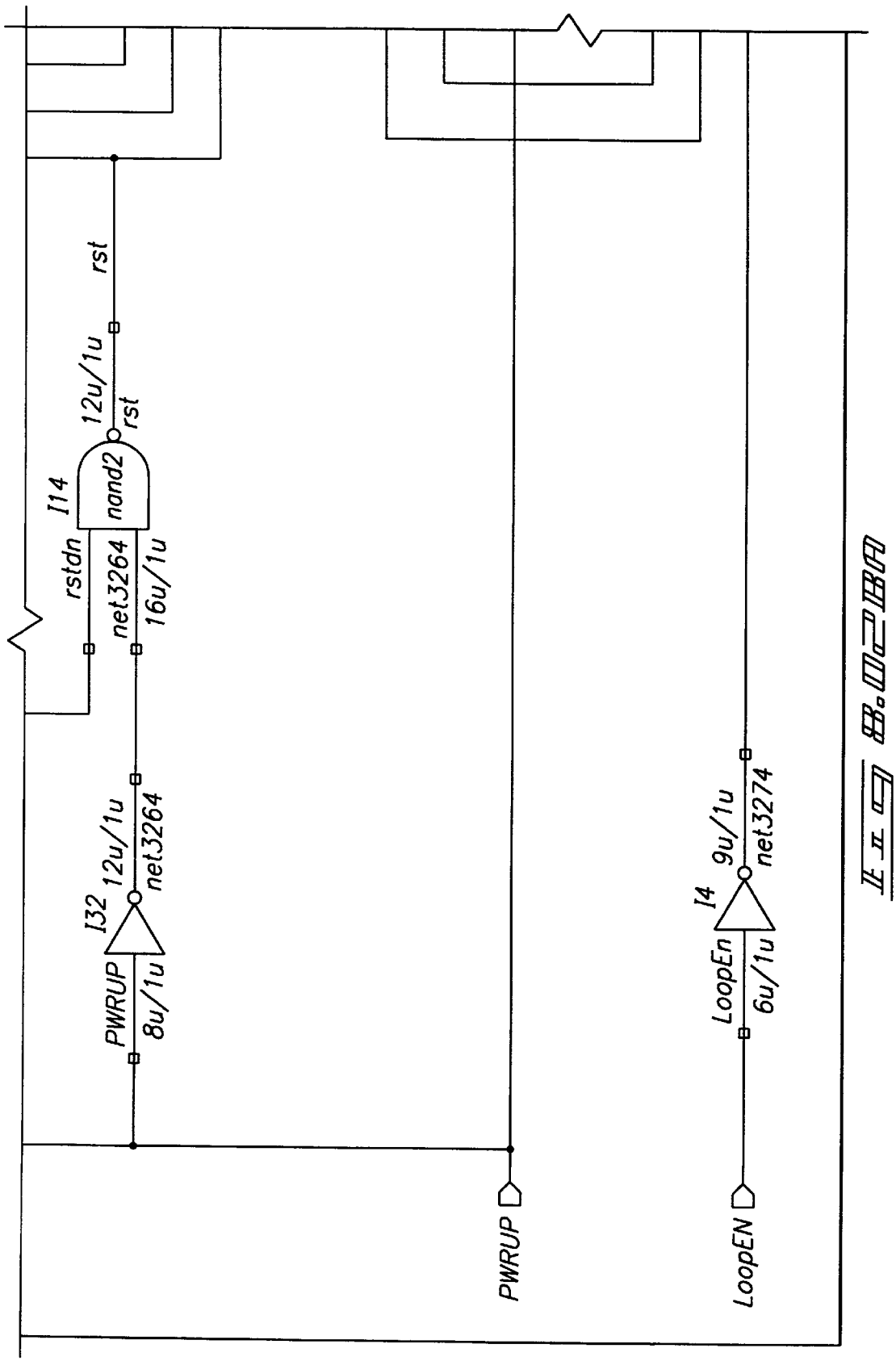

rst
12u/1u
rst
I14
nand2
rstdn
net3264
16u/1u
I32
12u/1u
net3264
PWRUP
8u/1u
PWRUP
I4
9u/1u
net3274
LoopEn
6u/1u
LoopEN

FIG 8.0284A

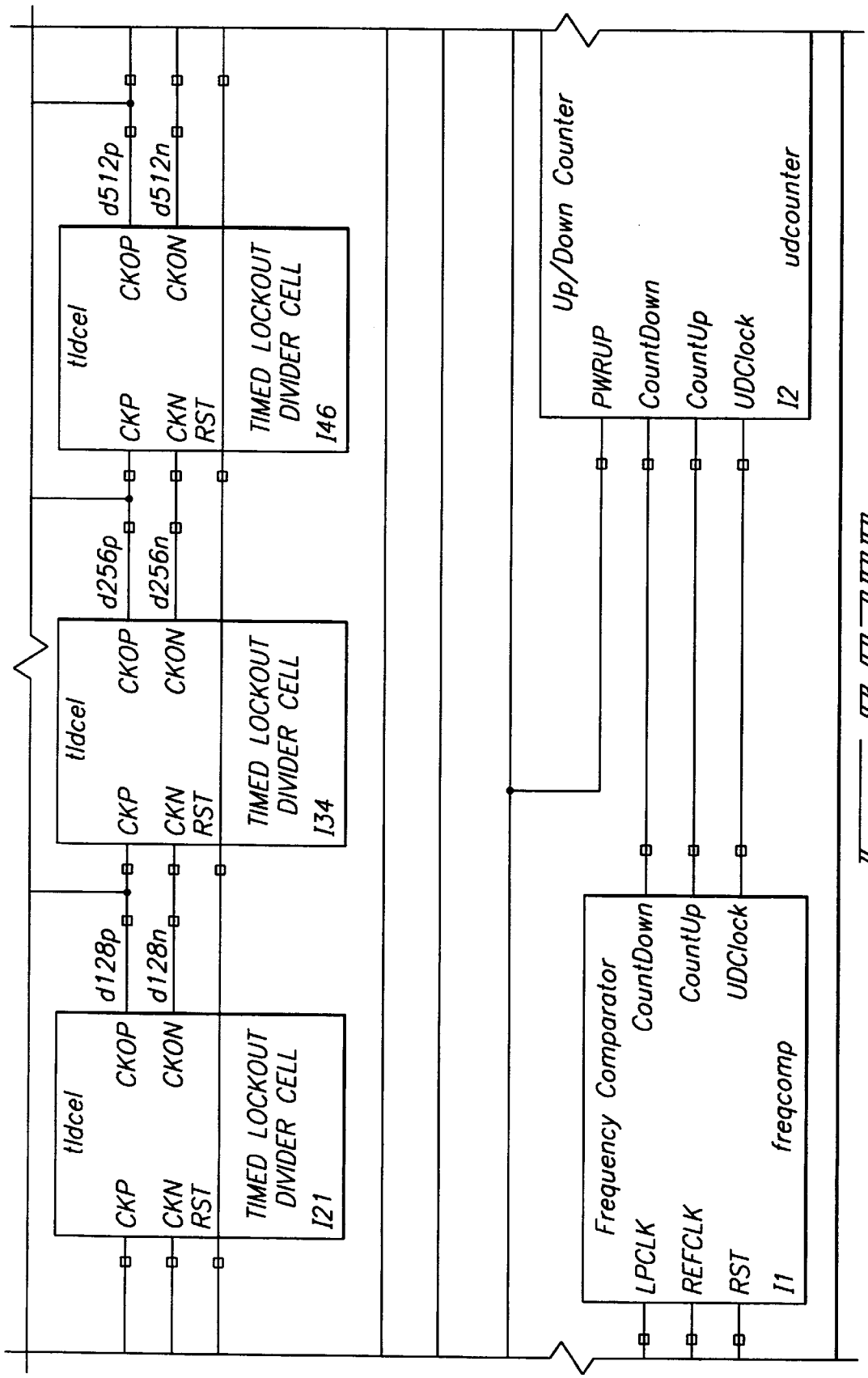

tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I21
d128p
d128n
I34
d256p
d256n
I46
d512p
d512n
Up/Down Counter
PWRUP
CountDown
CountUp
UDClock
I2
udcounter
Frequency Comparator
LPCLK
REFCLK
RST
I1
freqcomp

FIG. 1304

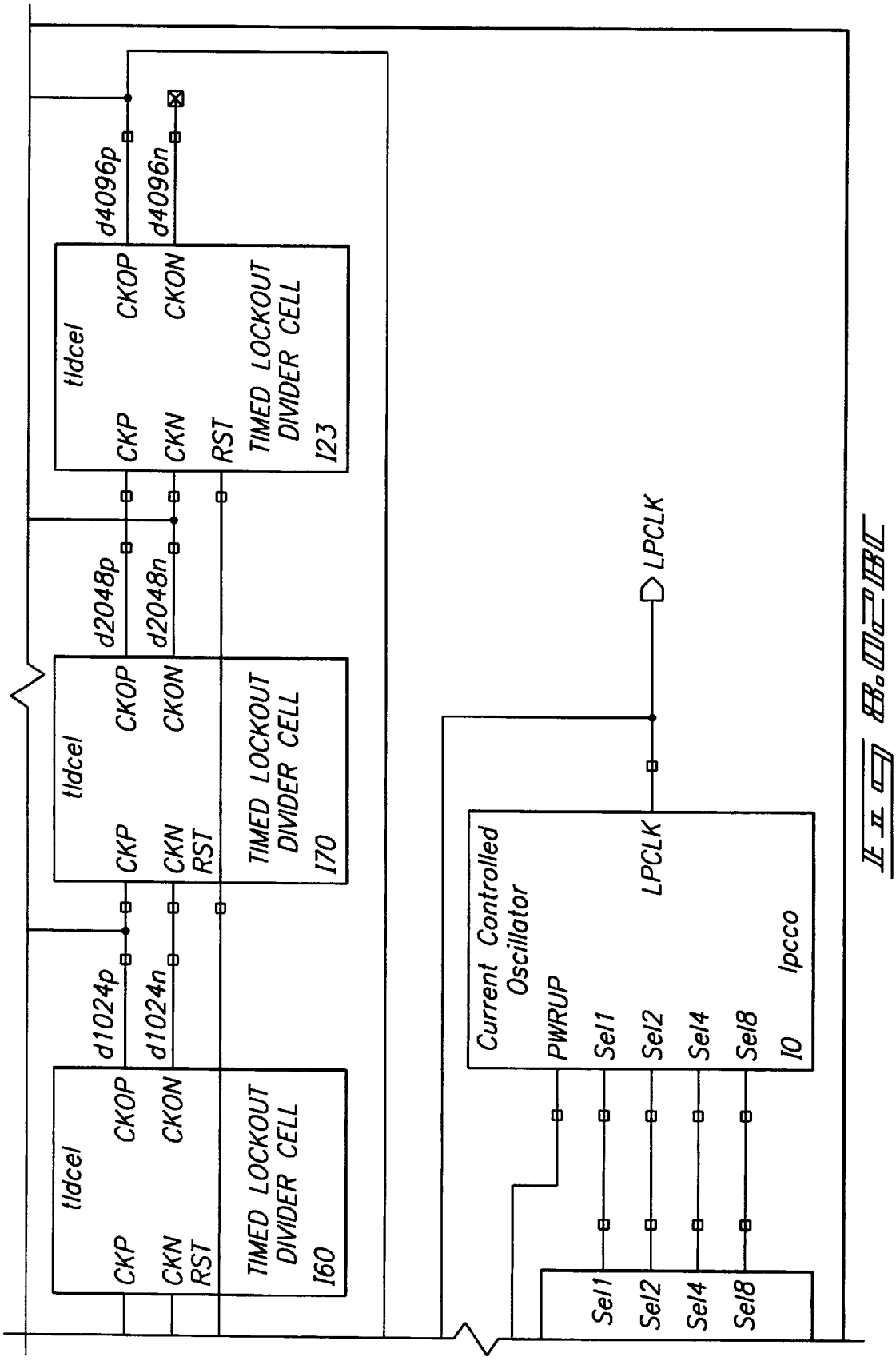

tldcel
CKP
CKN
RST
CKOP
CKON
TIMED LOCKOUT DIVIDER CELL
I60
d1024p
d1024n
I70
d2048p
d2048n
I23
d4096p
d4096n
LPCLK
Current Controlled Oscillator
PWRUP
Sel1
Sel2
Sel4
Sel8
I0
lpcco

FIG. 1308

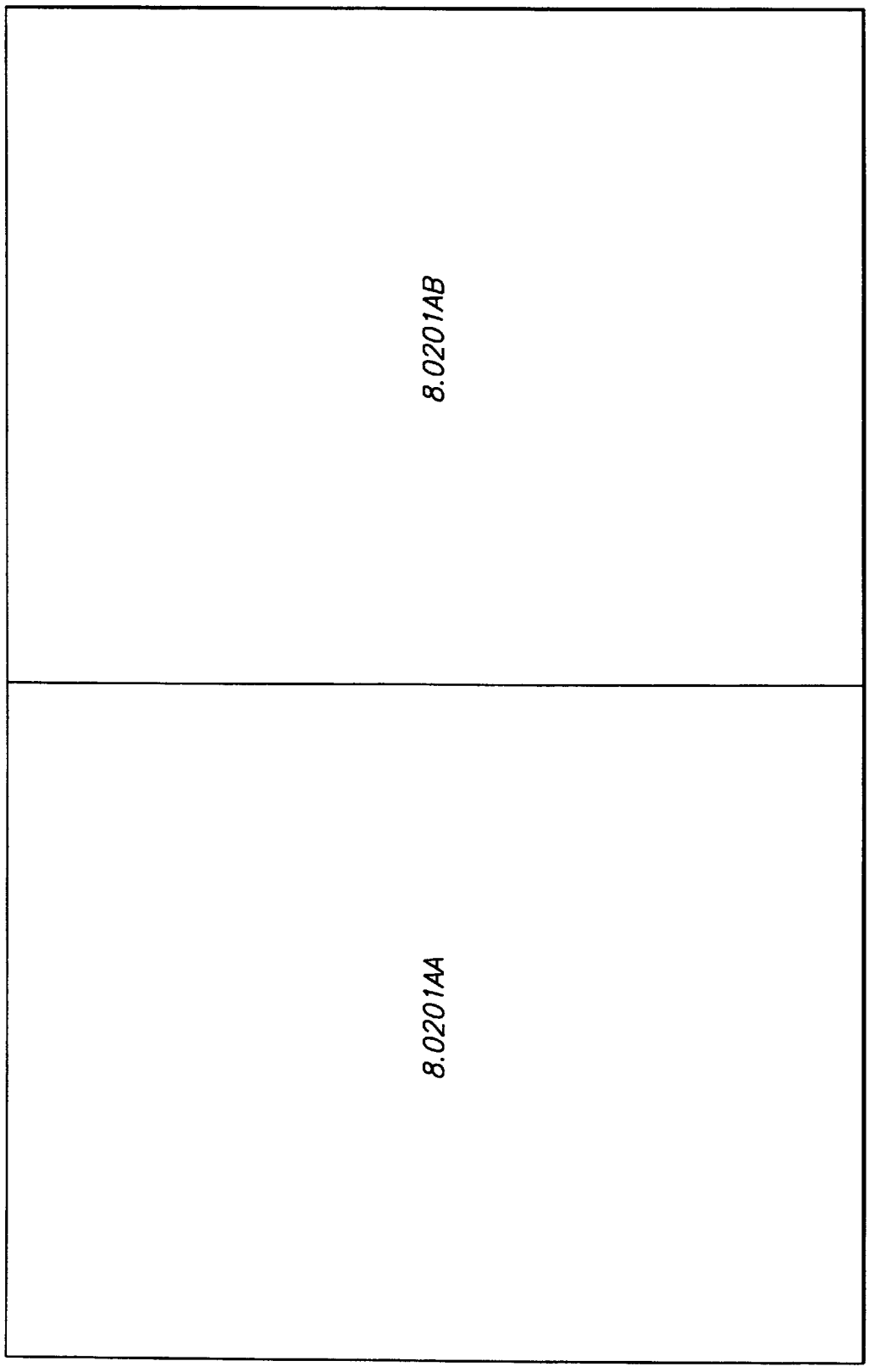


FIG 8.0201

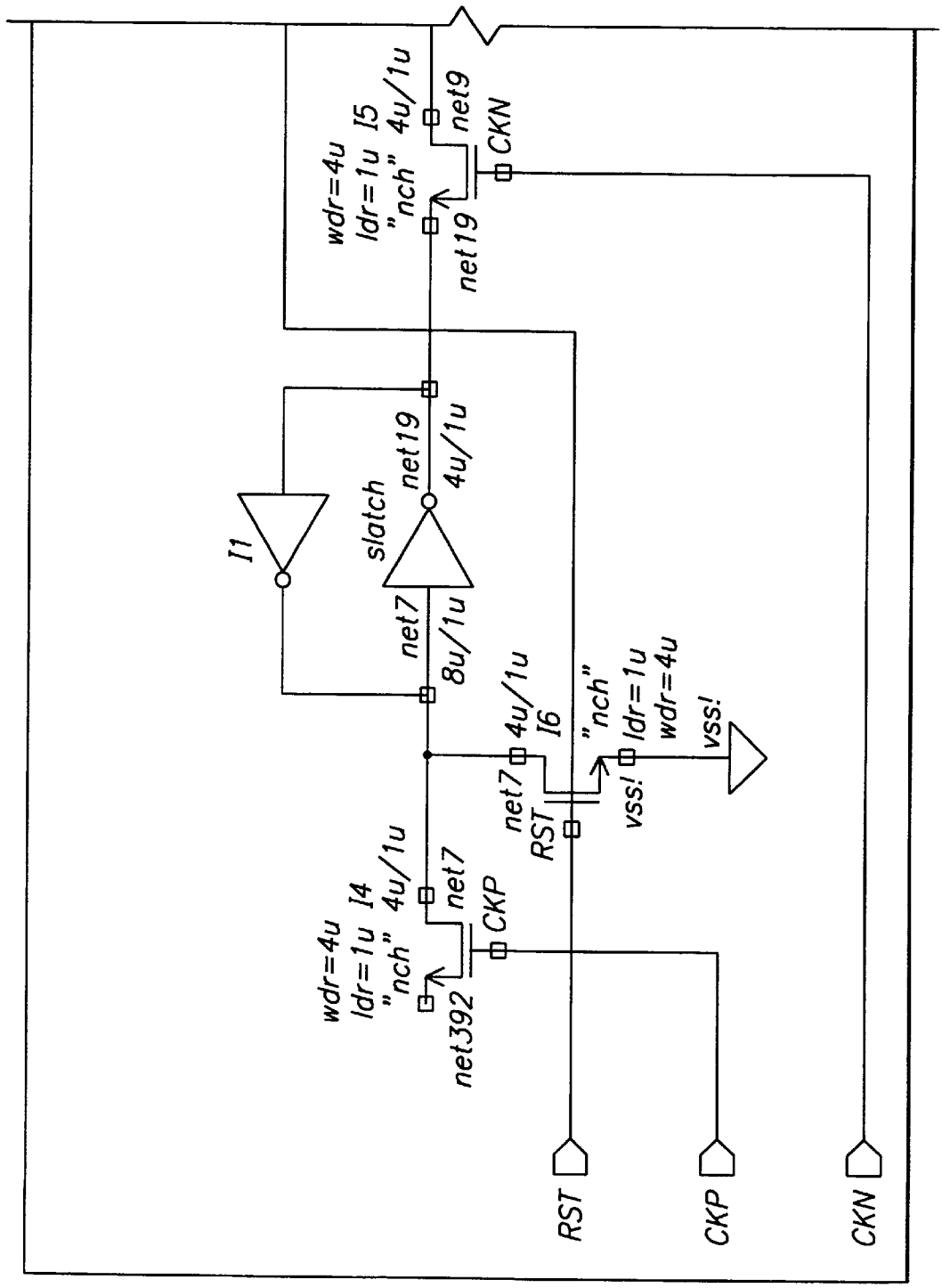


FIG 88.00211AA

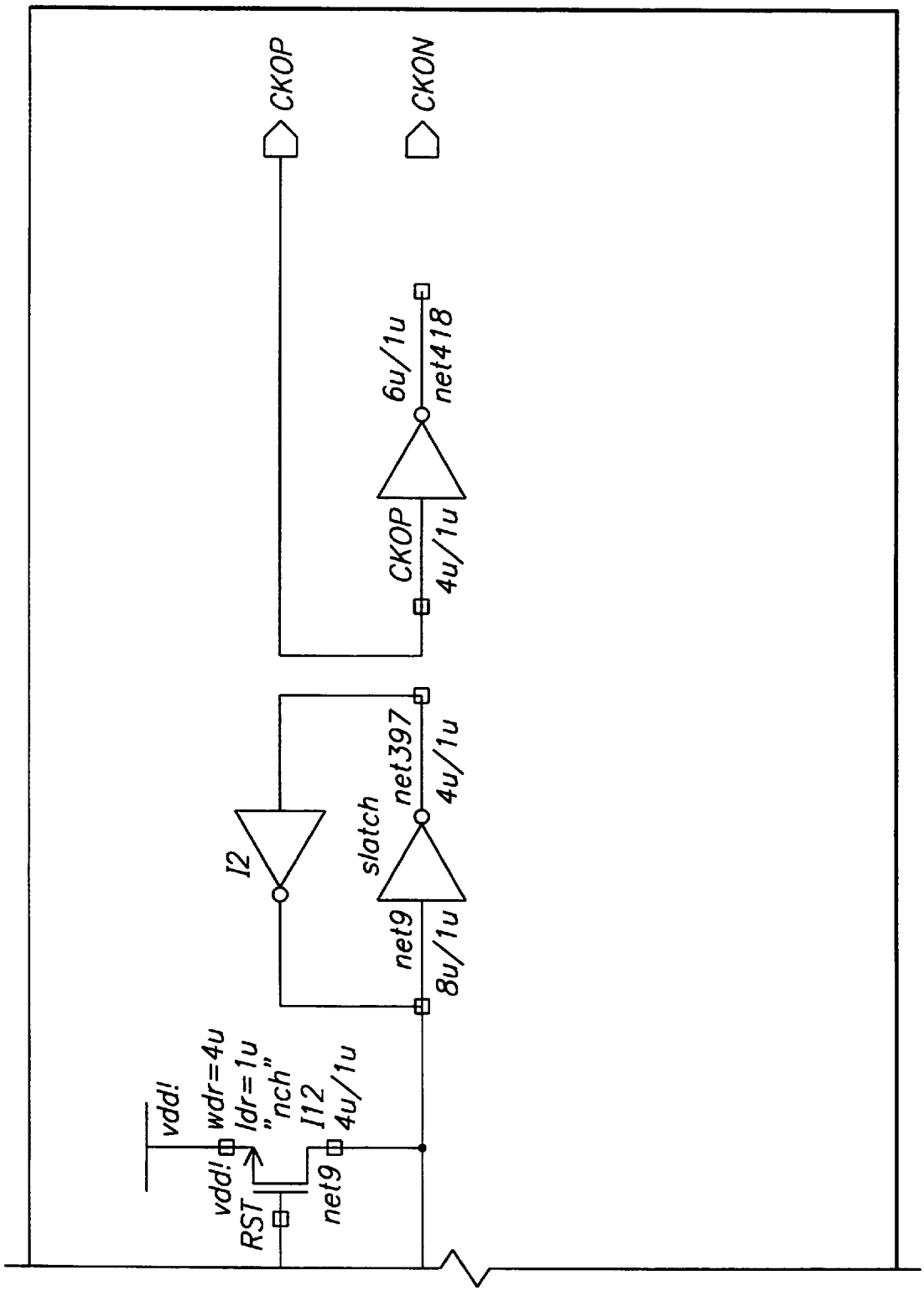

CKOP
CKON
6u/1u
net418
CKOP
4u/1u
I2
slatch
net397
4u/1u
net9
8u/1u
vdd!
wdr=4u
ldr=1u
"nch"
I12
4u/1u
vdd!
RST
net9

FIG 8.0211AB

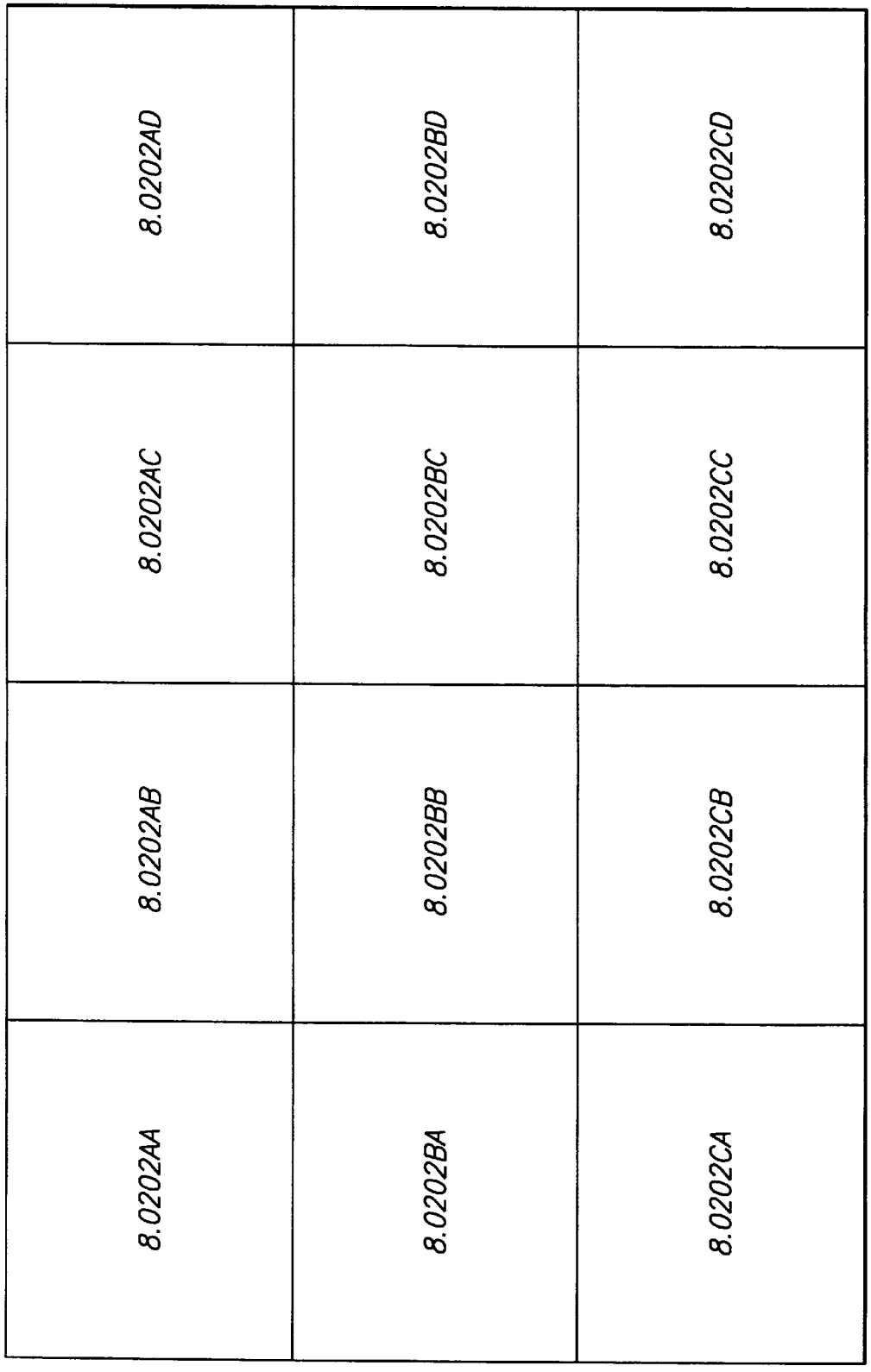

8.0202AD
8.0202BD
8.0202CD
8.0202AC
8.0202BC
8.0202CC
8.0202AB
8.0202BB
8.0202CB
8.0202AA
8.0202BA
8.0202CA

FIG. 8.0202

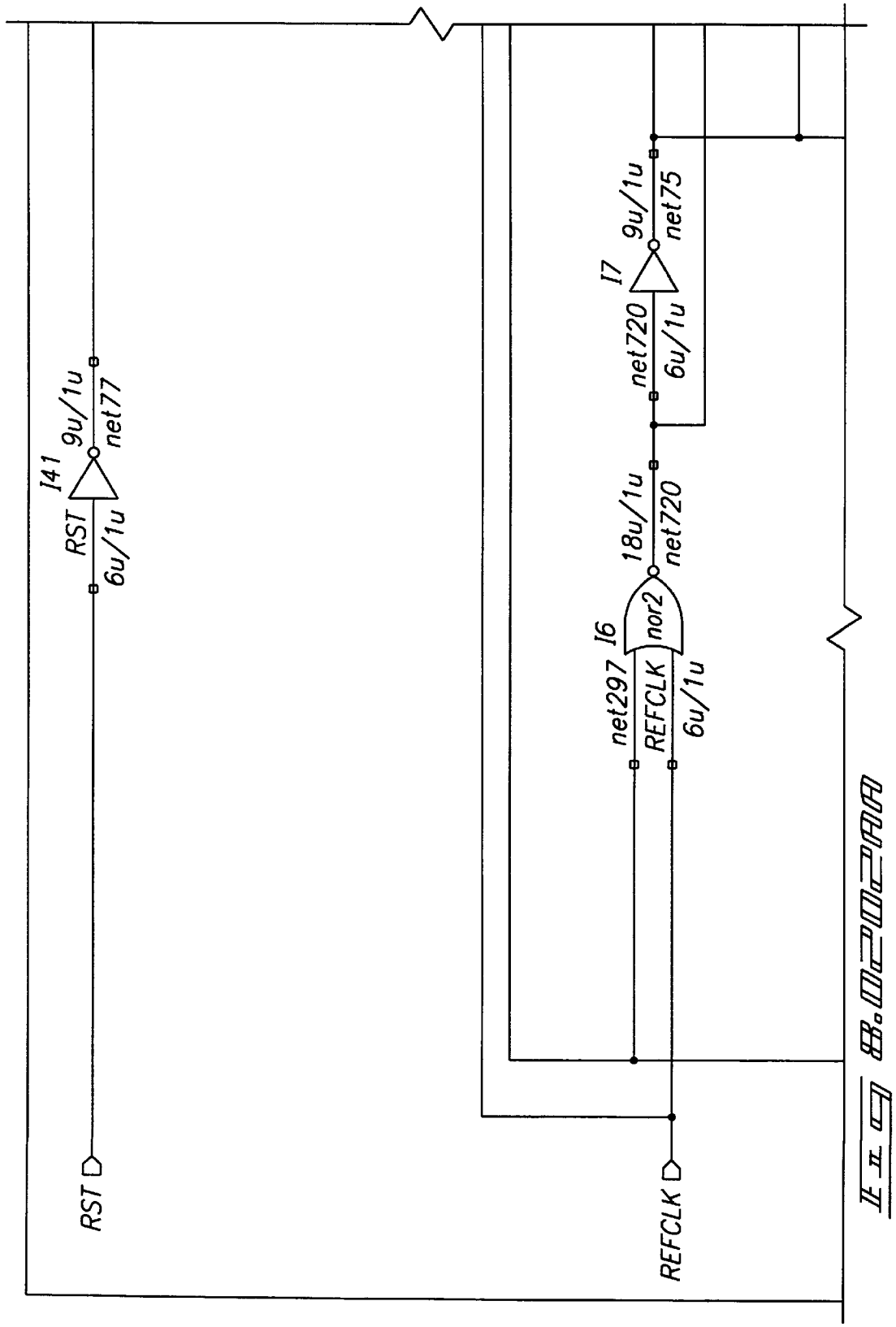

I41
9u/1u
net77
RST
6u/1u
I7
9u/1u
net75
net720
6u/1u
18u/1u
net720
I6
nor2
net297
REFCLK
6u/1u
RST
REFCLK

FIG. 1300

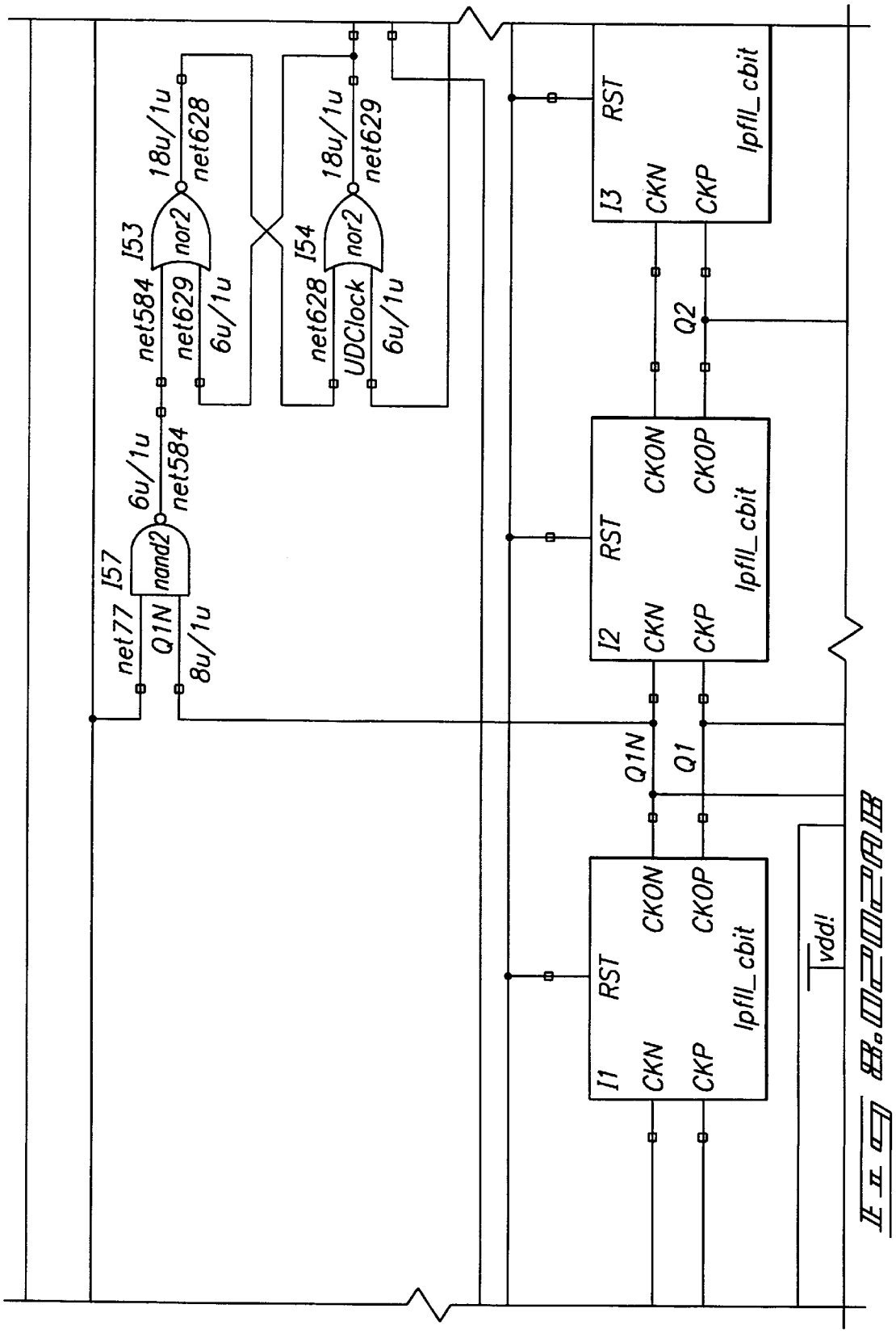

I53
nor2
18u/1u
net628
net584
net629
6u/1u
I54
nor2
18u/1u
net629
net628
UDClock
6u/1u
I57
nand2
6u/1u
net584
net77
Q1N
8u/1u
I3
RST
CKN
CKP
lpfll_cbit
Q2
I2
RST
CKON
CKOP
lpfll_cbit
CKN
CKP
Q1N
Q1
I1
RST
CKON
CKOP
lpfll_cbit
CKN
CKP
vdd!

Fig. 8,002,048

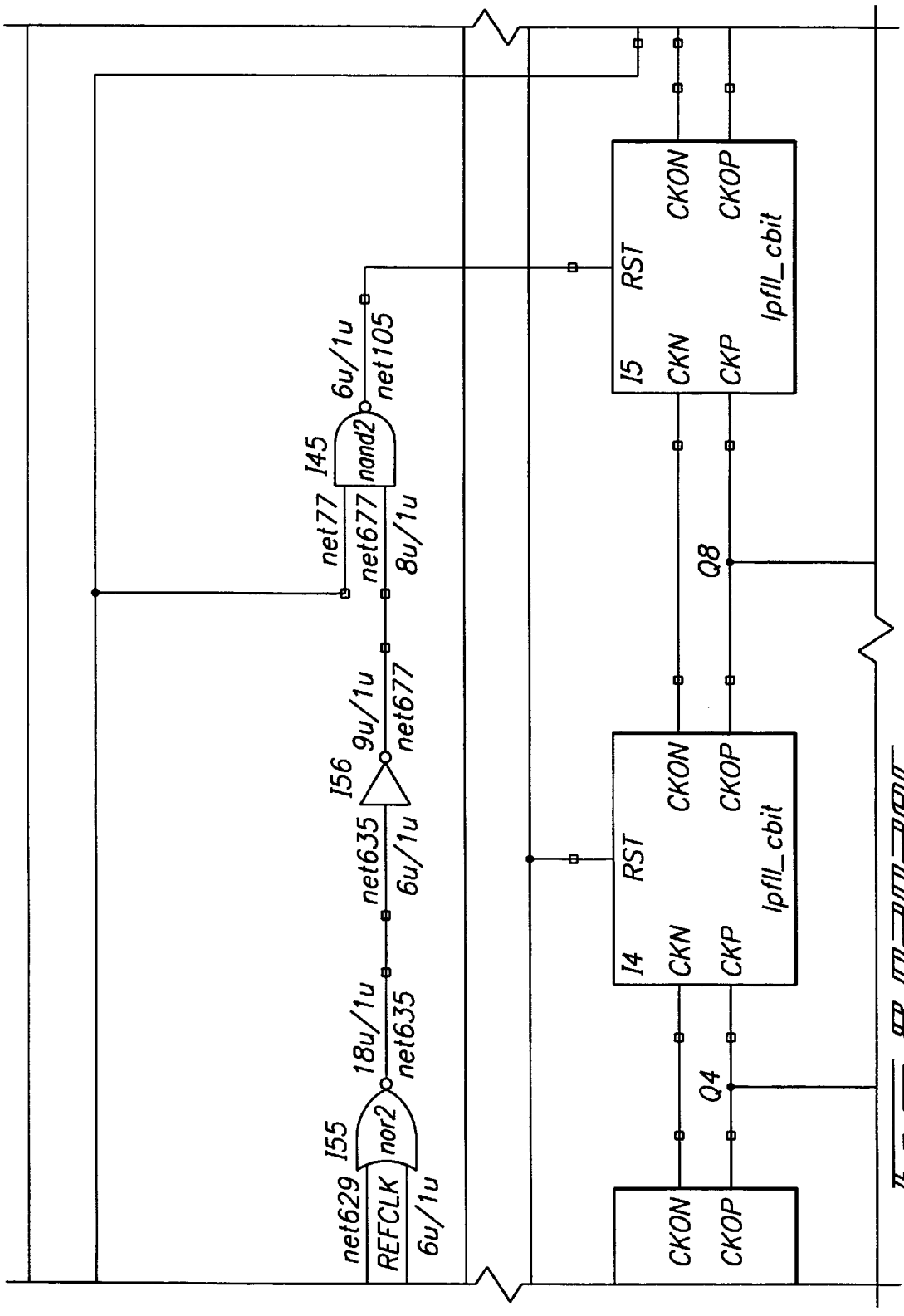
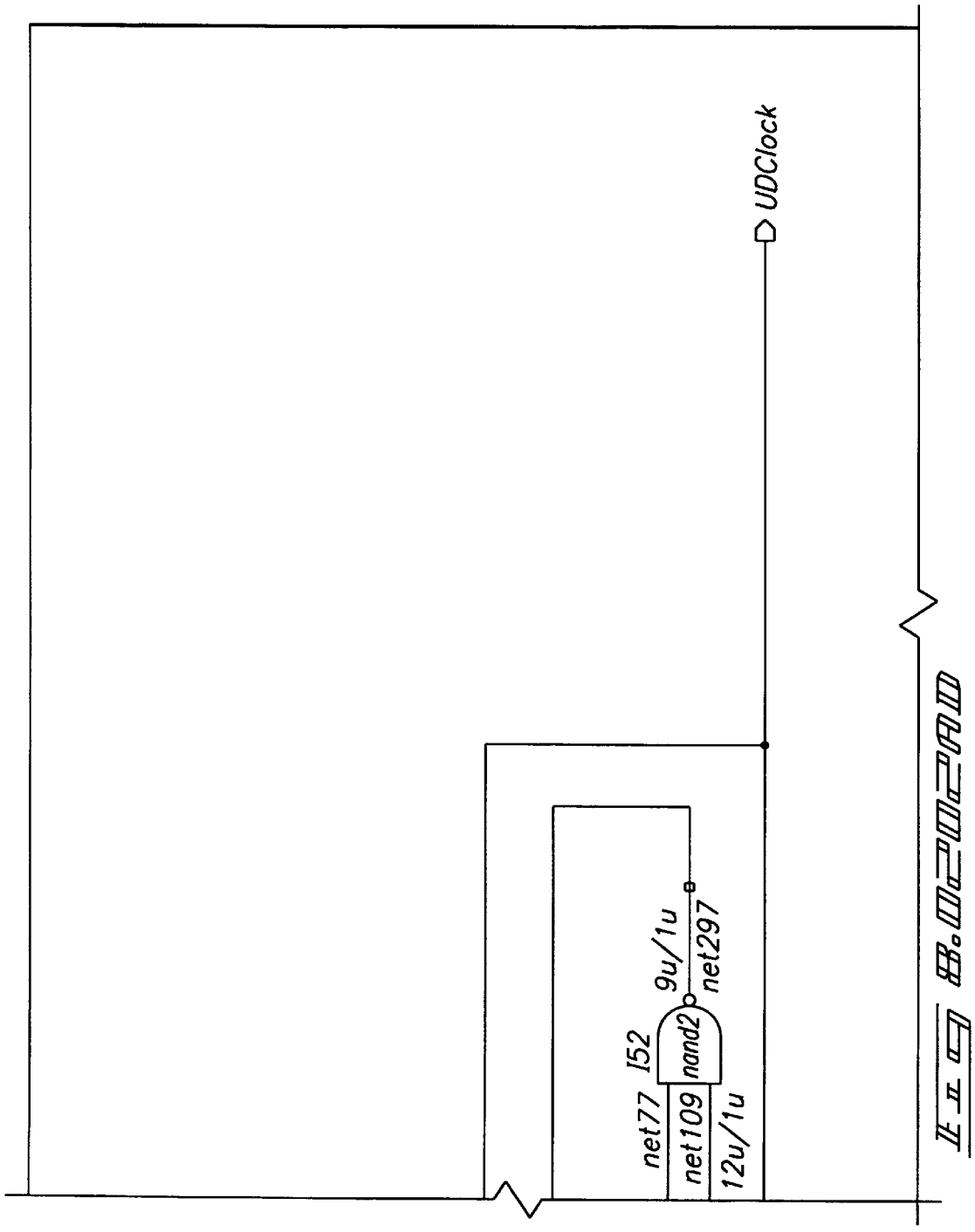

REFCLK
net629
6u/1u
I55
nor2
18u/1u
net635
6u/1u
I56
9u/1u
net677
8u/1u
I45
nand2
6u/1u
net105
net77
net677
net635
I5
I4
RST
CKN
CKP
CKON
CKOP
lpfll_cbit
Q8
Q4

FIG 88.02AAL


UDClock
9u/1u
net297
I52
nand2
net77
net109
12u/1u

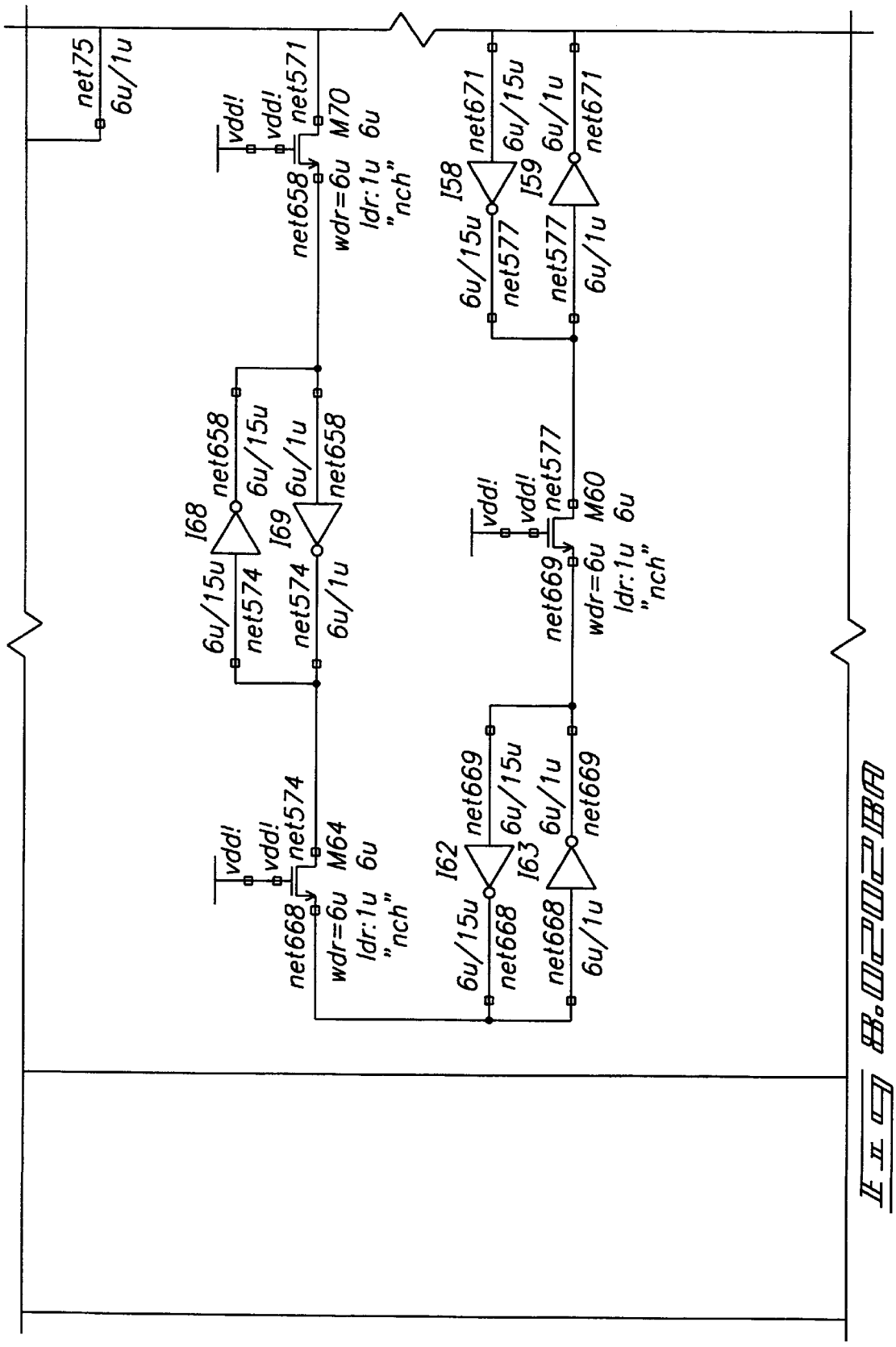

net75
6u/1u
vdd!
net571
M70
6u
wdr=6u
ldr:1u
"nch"
net658
I58
I59
net671
6u/15u
6u/1u
net577
I68
I69
net574
I62
I63
net669
net668
M64
M60

FIG. 1314

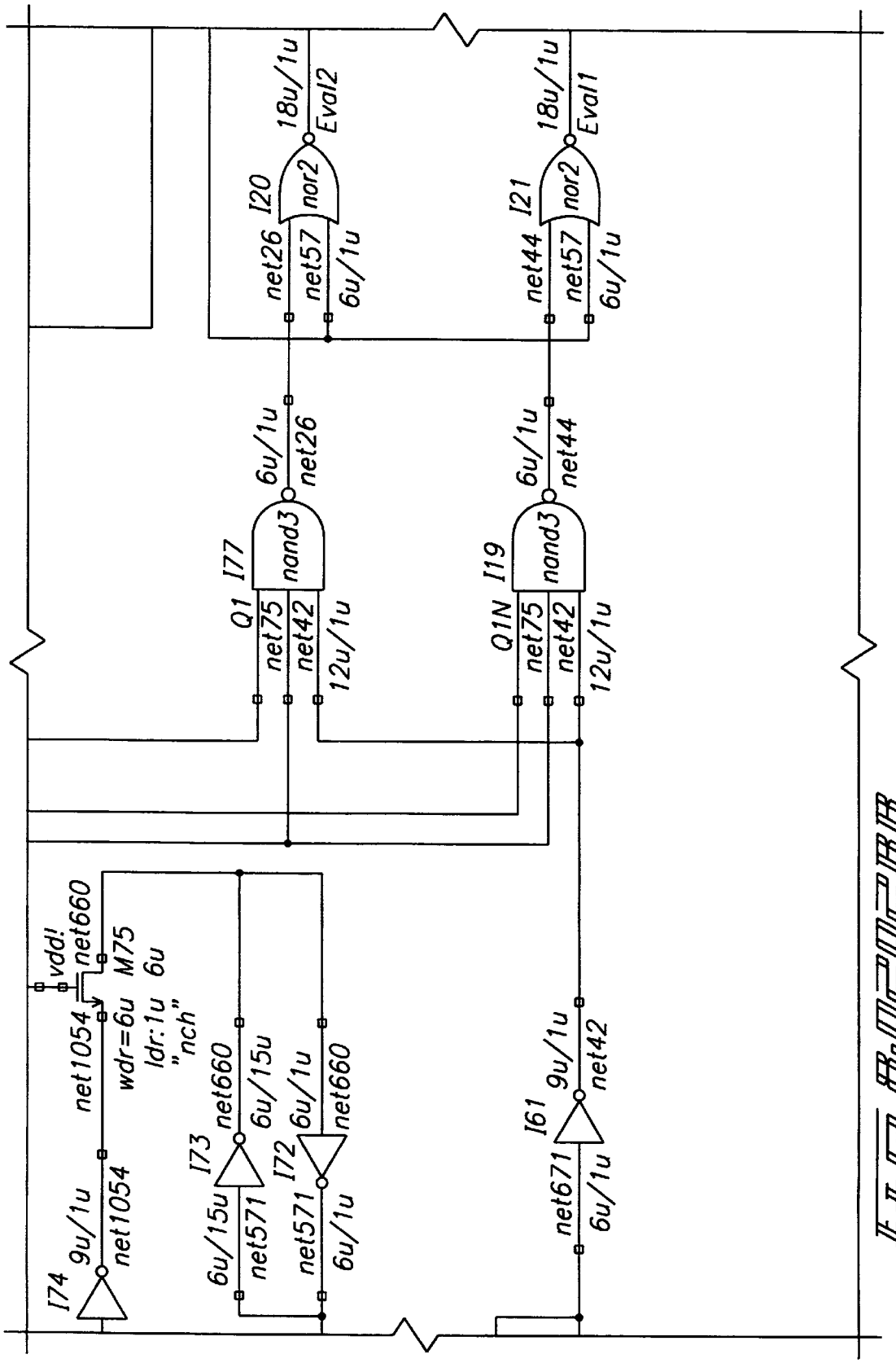


FIG 88.00200B

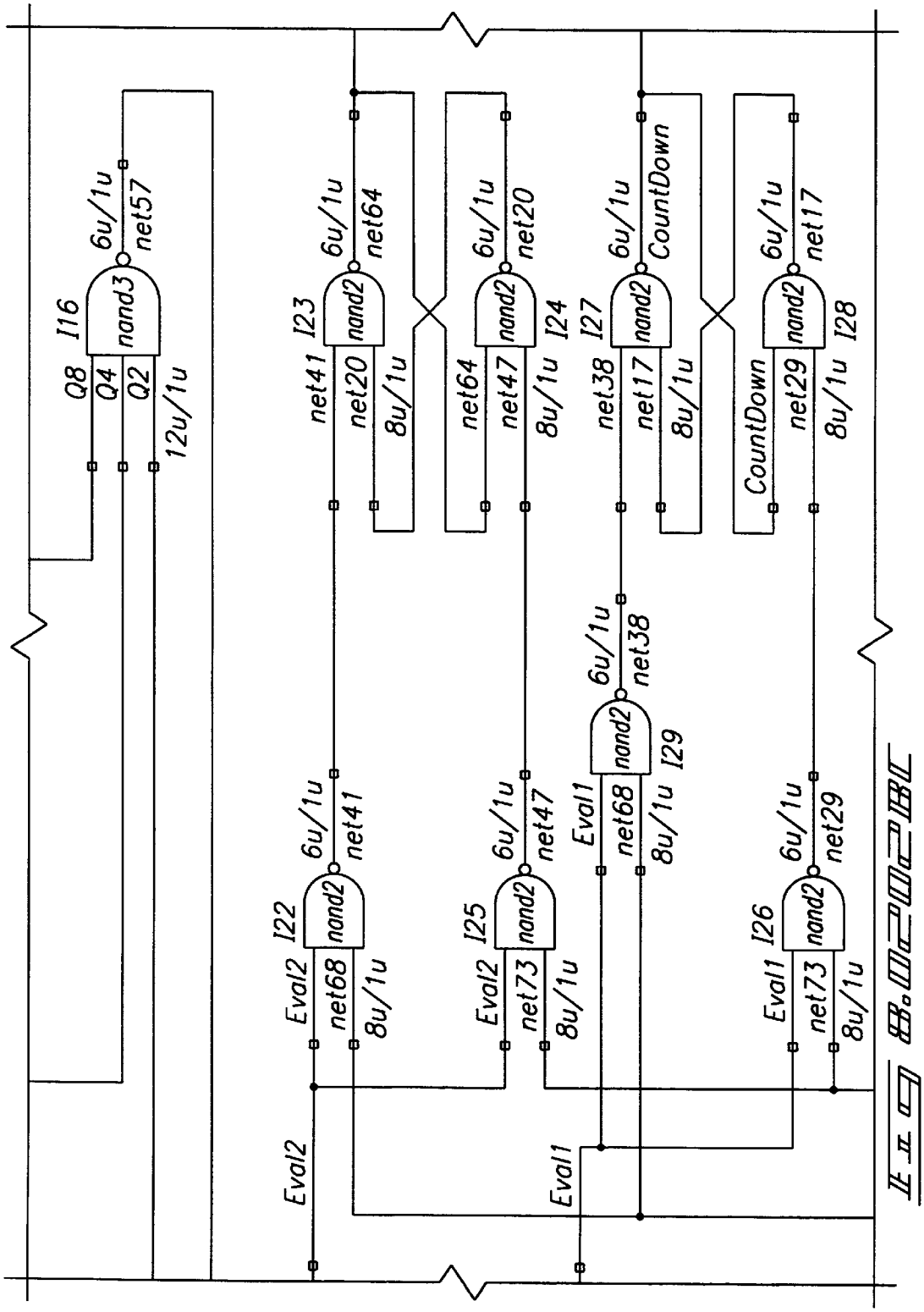
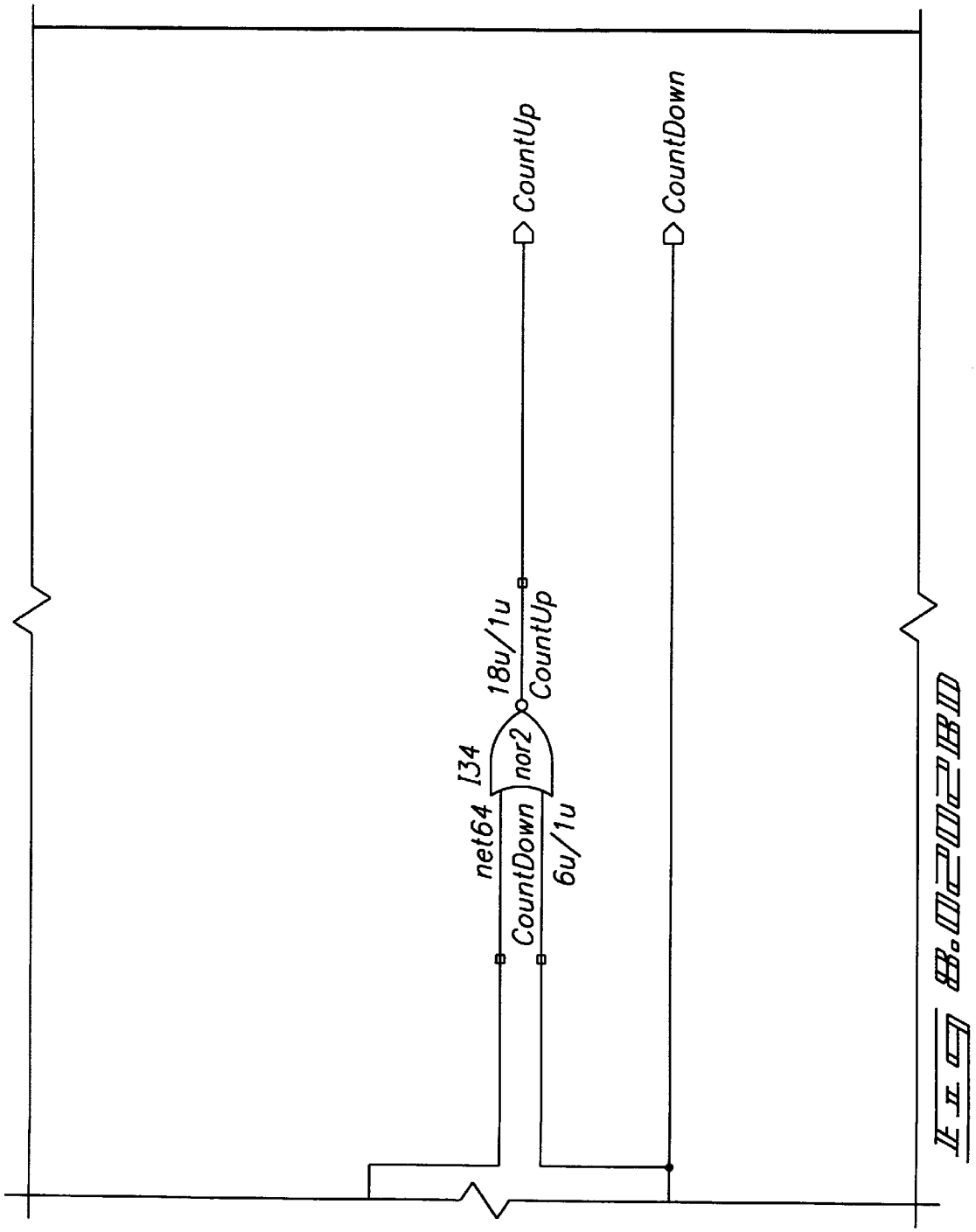

I16
nand3
6u/1u
net57
Q8
Q4
Q2
12u/1u
I23
nand2
6u/1u
net64
net41
net20
8u/1u
I24
nand2
6u/1u
net20
net64
net47
8u/1u
I27
nand2
6u/1u
CountDown
net38
net17
8u/1u
I28
nand2
6u/1u
net17
CountDown
net29
8u/1u
I22
nand2
6u/1u
net41
Eval2
net68
8u/1u
I25
nand2
6u/1u
net47
Eval2
net73
8u/1u
I29
nand2
6u/1u
net38
Eval1
net68
8u/1u
I26
nand2
6u/1u
net29
Eval1
net73
8u/1u
Eval2
Eval1

FIG. 1316


CountUp
CountDown
18u/1u
CountUp
I34
nor2
net64
CountDown
6u/1u
FIG. 88.02200

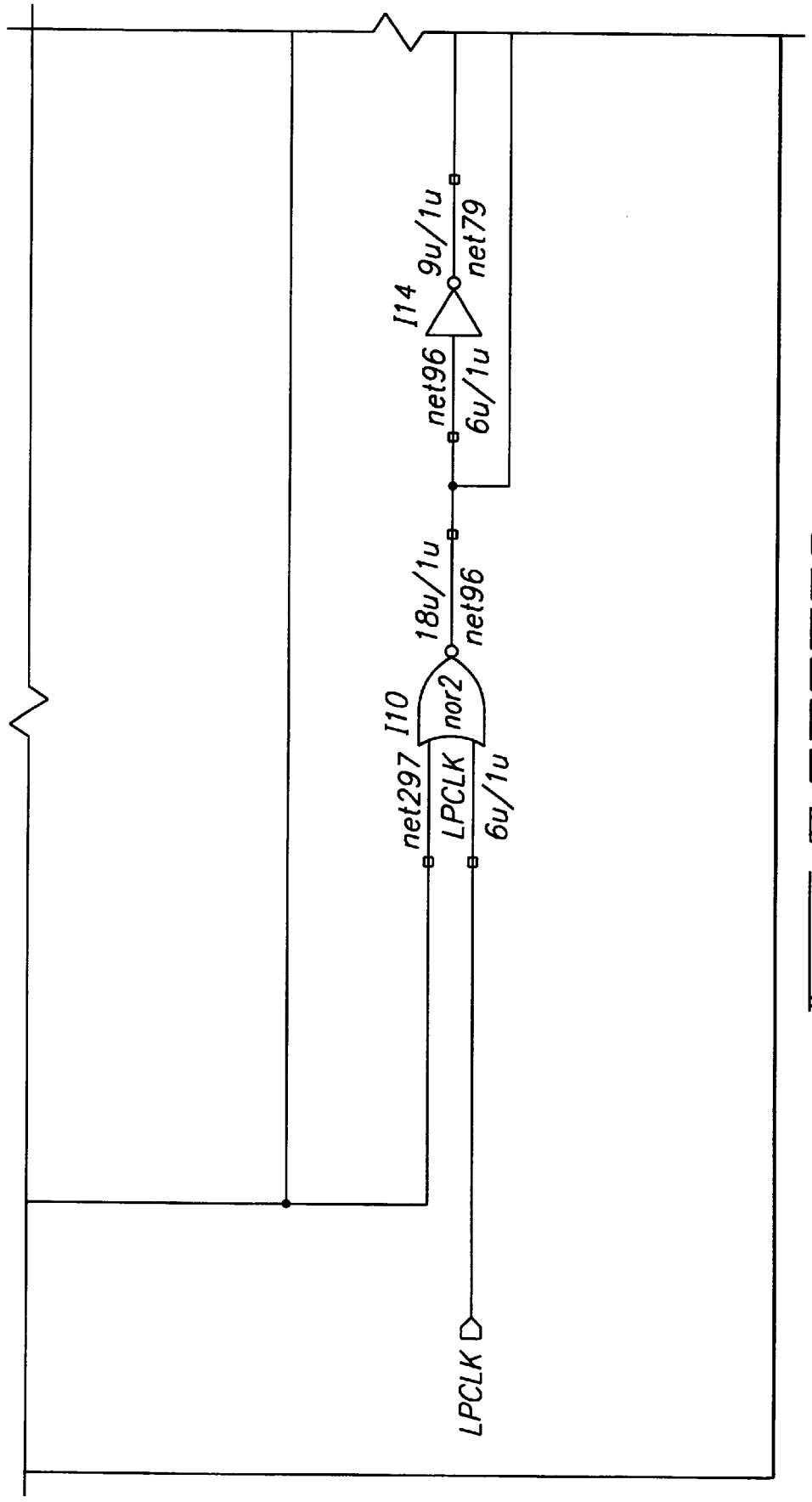

I14
9u/1u
net79
net96
6u/1u
18u/1u
net96
I10
nor2
net297
LPCLK
6u/1u
LPCLK

FIG 88.02A

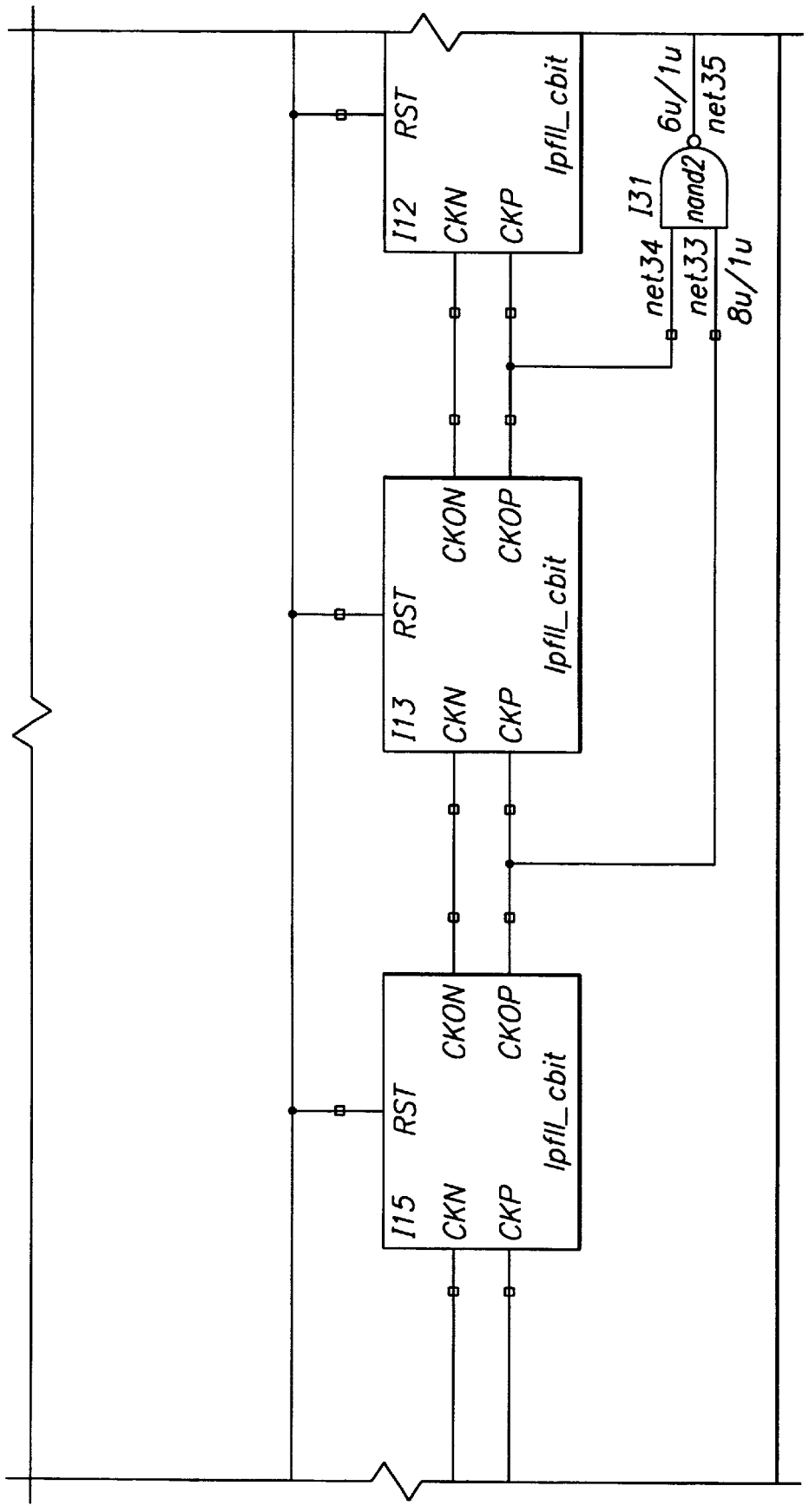

I12
RST
CKN
CKP
lpfll_cbit
I13
RST
CKN
CKP
CKON
CKOP
lpfll_cbit
I15
RST
CKN
CKP
CKON
CKOP
lpfll_cbit
I31
nand2
6u/1u
net35
net34
net33
8u/1u

FIG 8.0202B

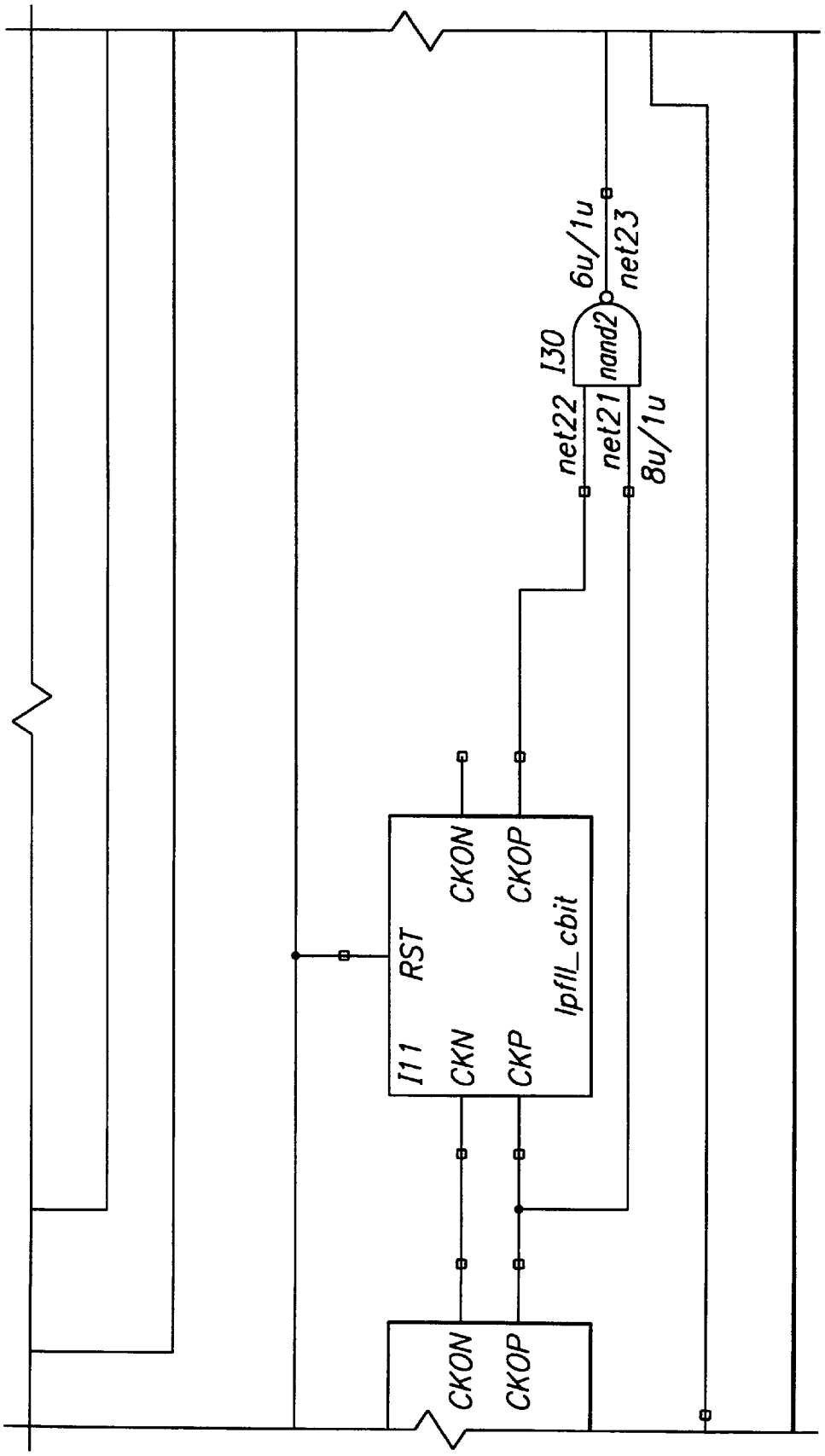


FIG. 88.00200C

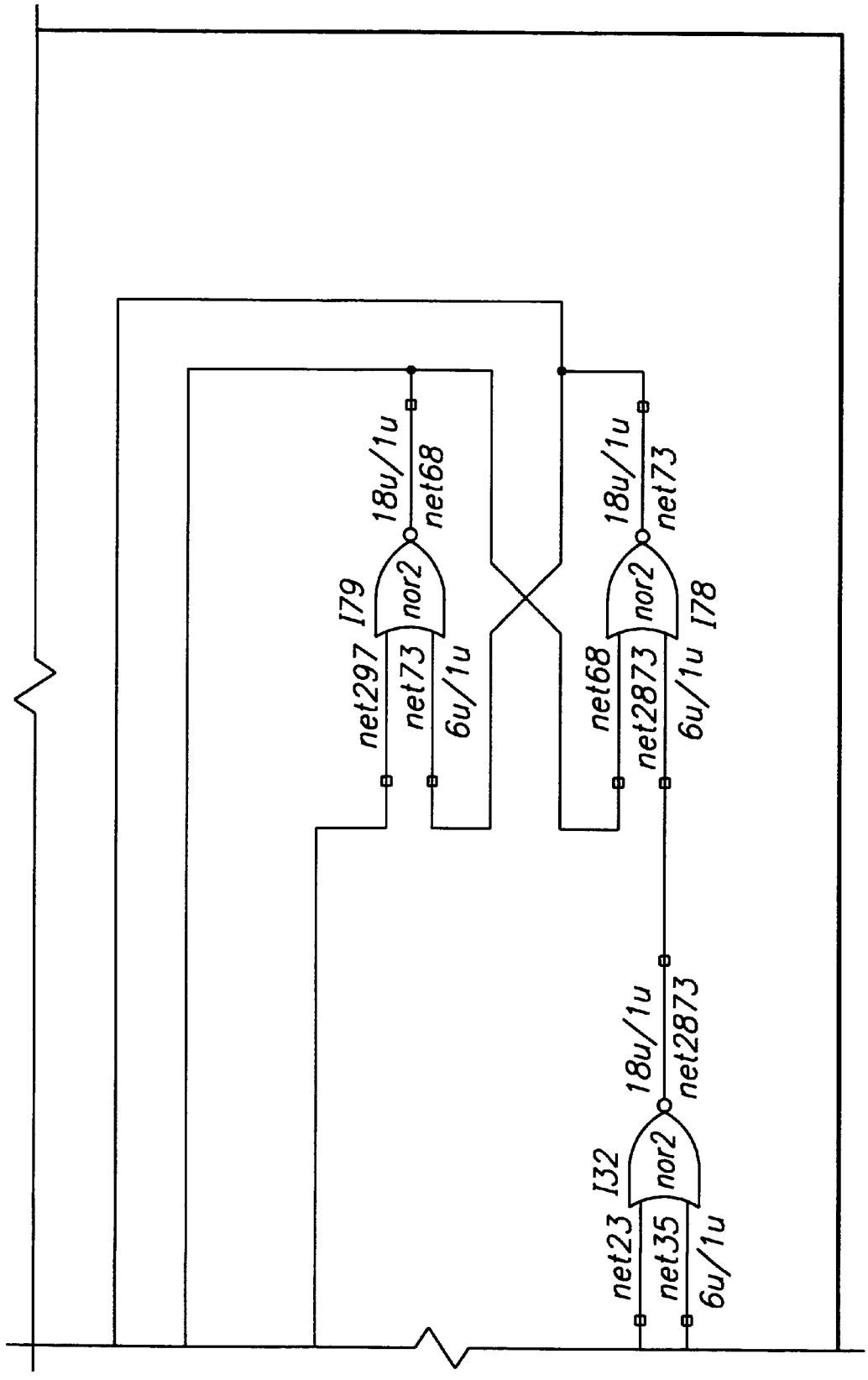
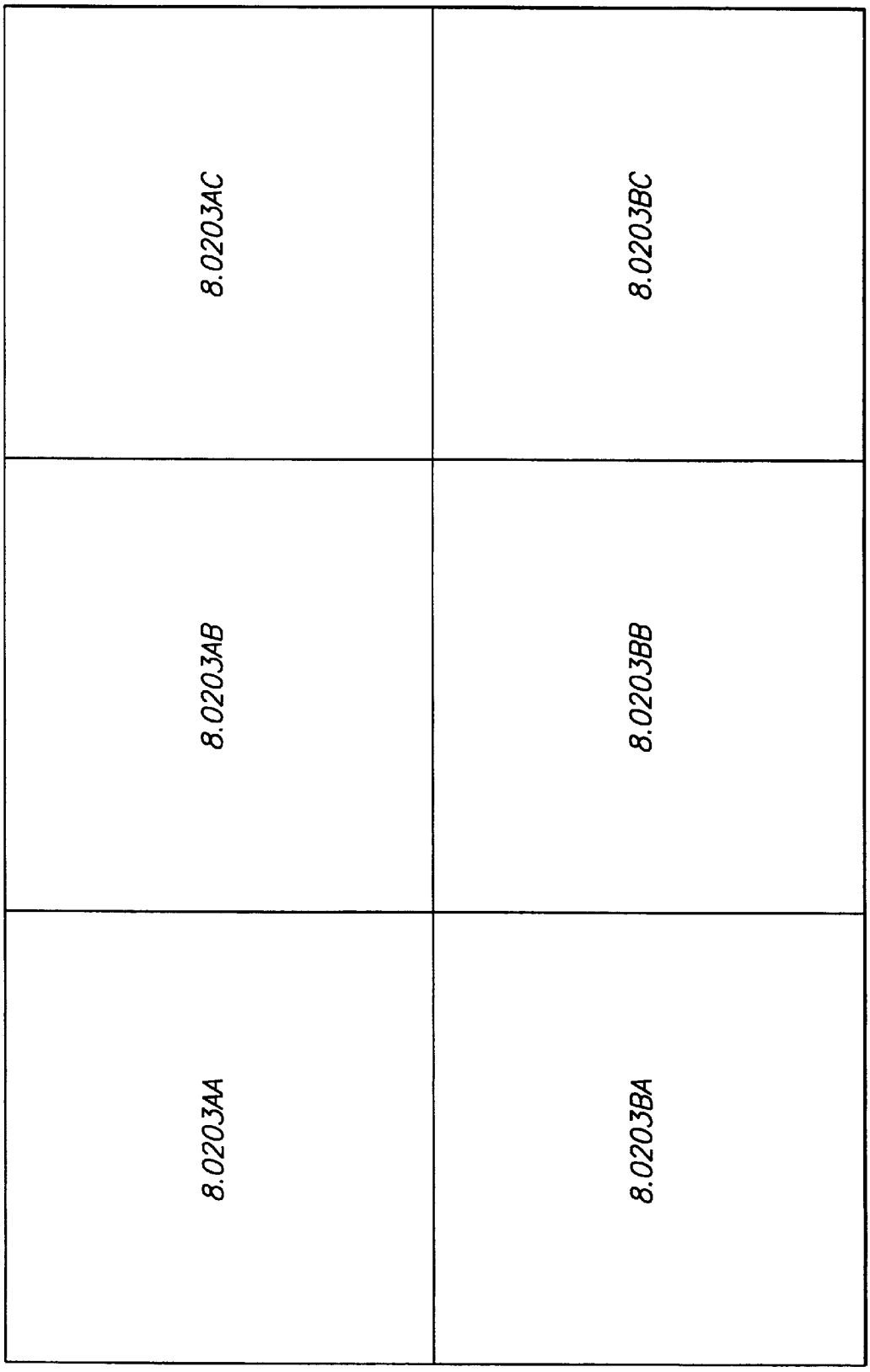


FIG 88.00200210


8.0203AC
8.0203BC
8.0203AB
8.0203BB
8.0203AA
8.0203BA
FIG. 8.0203

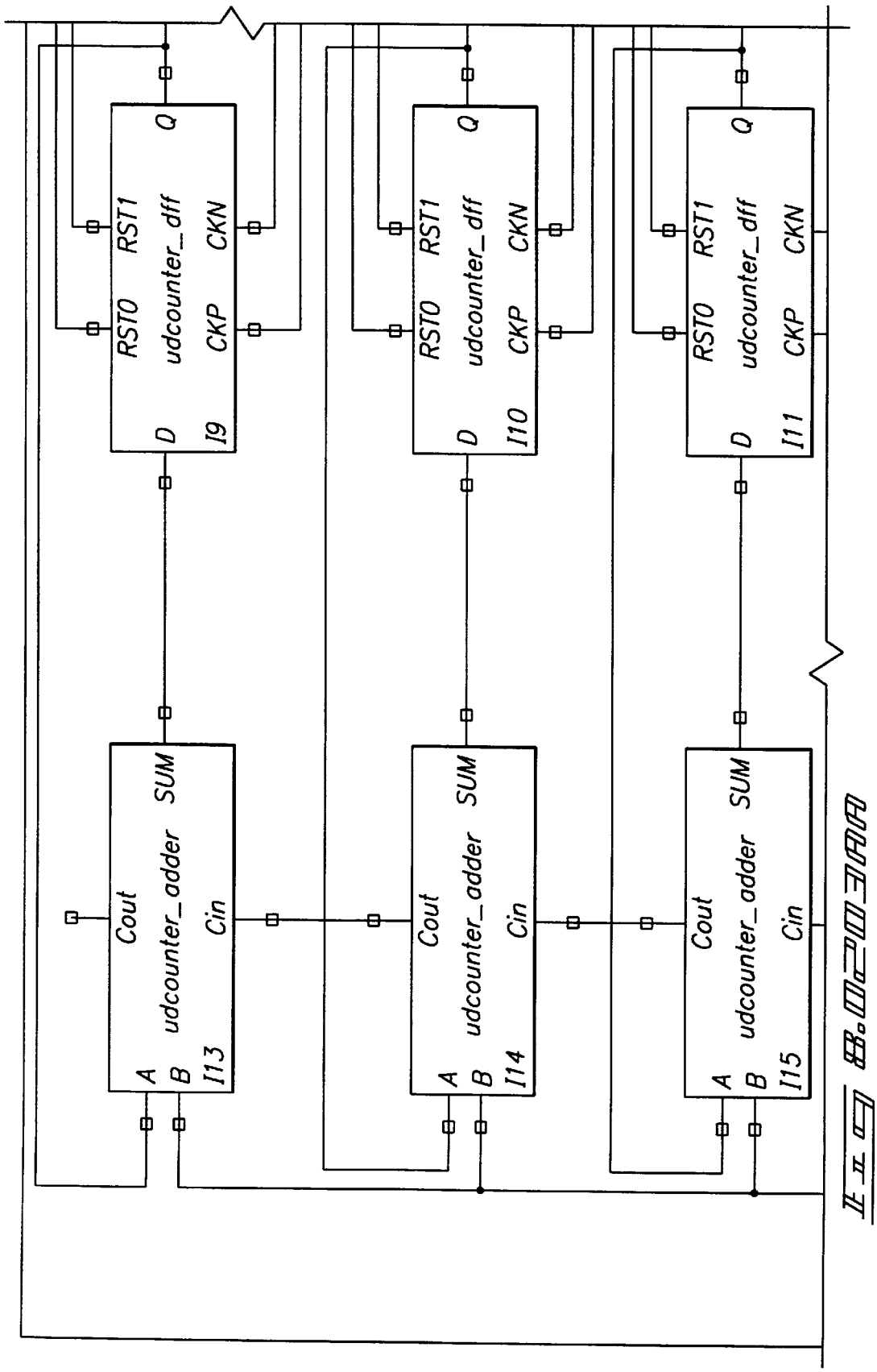

udcounter_dff
RST0
RST1
CKP
CKN
D
Q
I9
I10
I11
udcounter_adder
A
B
Cout
Cin
SUM
I13
I14
I15

FIG. 8.00EAA

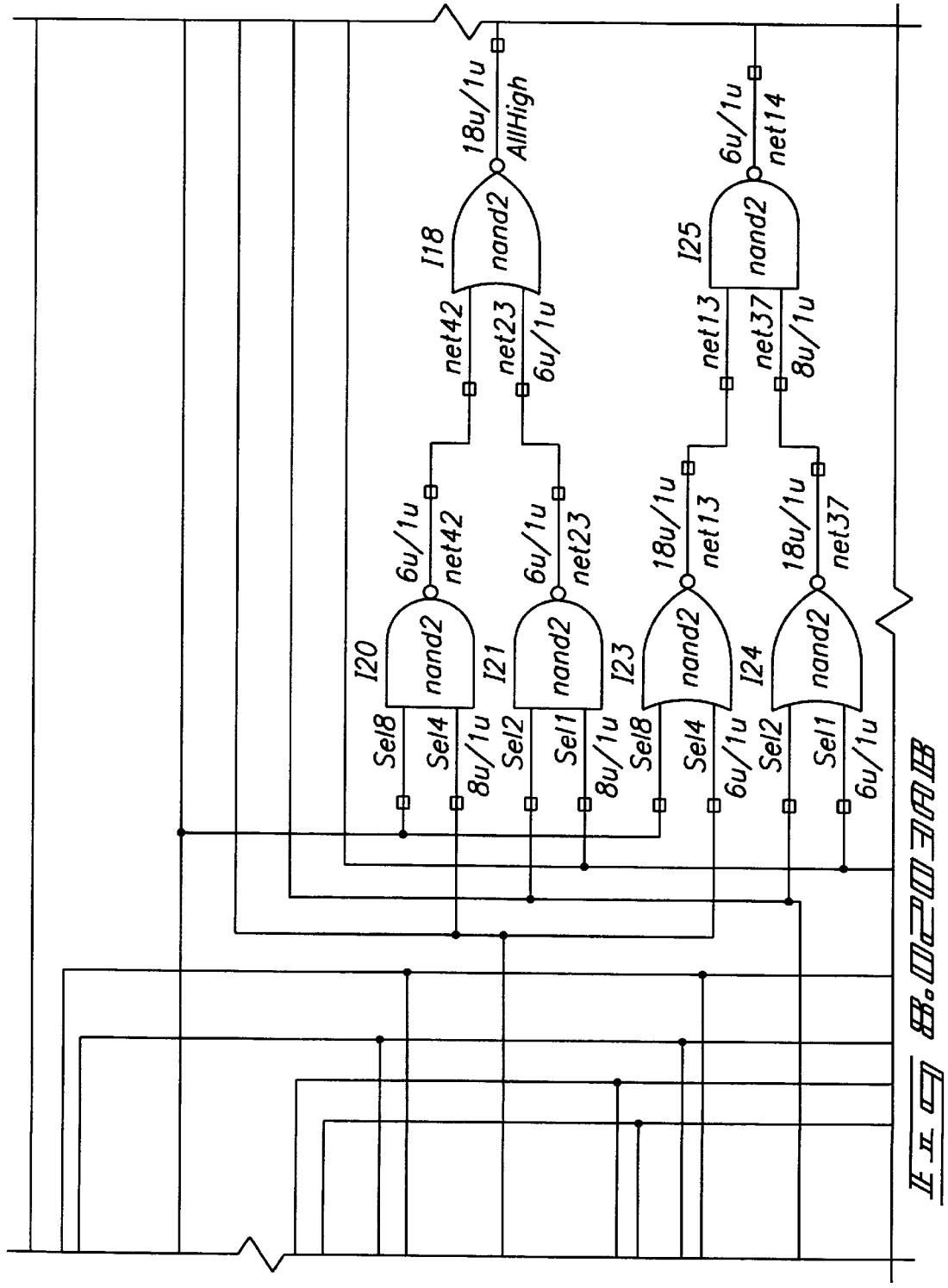

I18
nand2
18u/1u
AllHigh
I25
nand2
6u/1u
net14
net42
net23
6u/1u
net13
net37
8u/1u
I20
nand2
6u/1u
net42
I21
nand2
6u/1u
net23
I23
nand2
18u/1u
net13
I24
nand2
18u/1u
net37
Sel8
Sel4
8u/1u
Sel2
Sel1
8u/1u
Sel8
Sel4
6u/1u
Sel2
Sel1
6u/1u

FIG. 800A

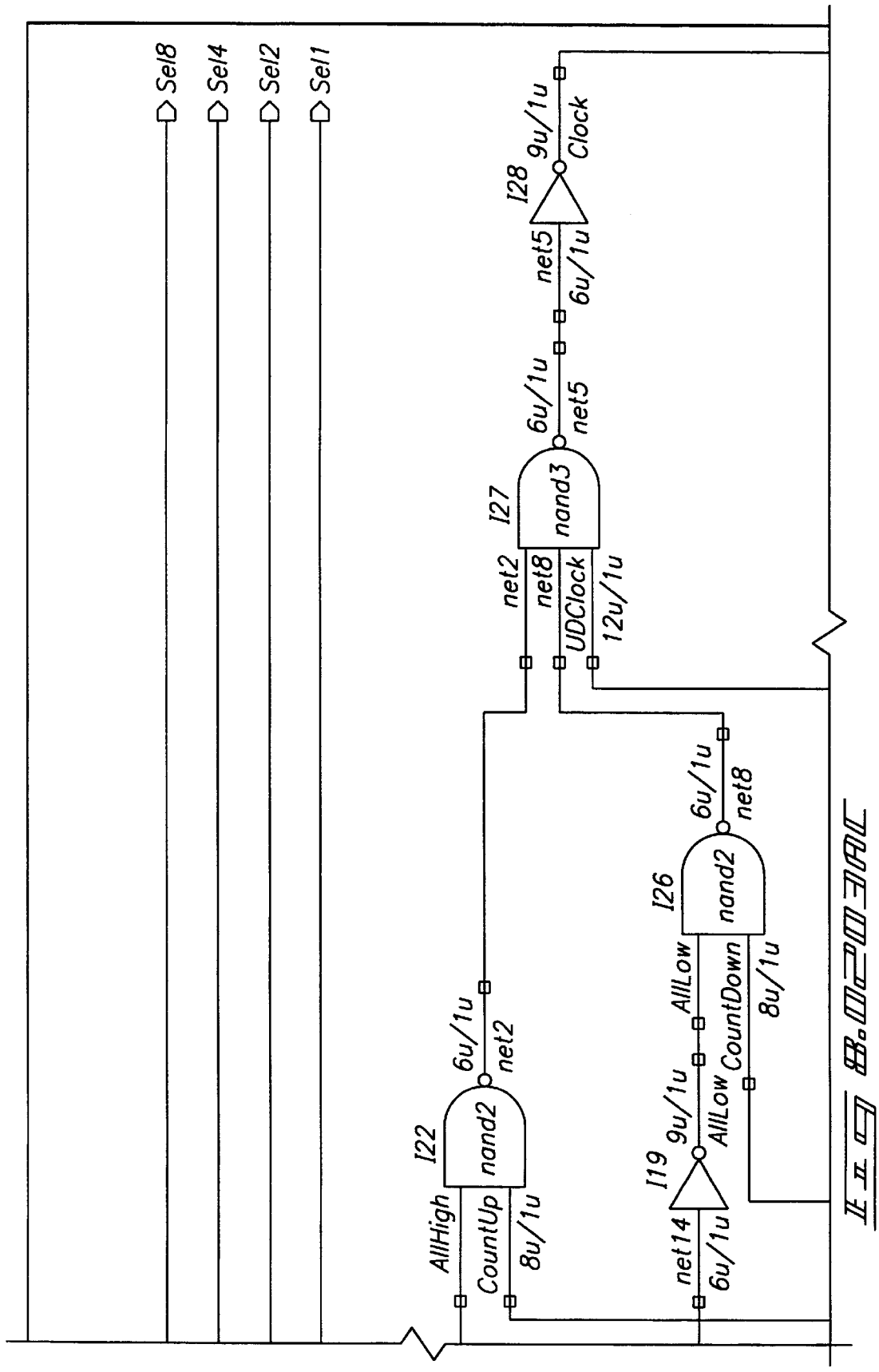

Sel8
Sel4
Sel2
Sel1
I28
9u/1u
Clock
net5
6u/1u
6u/1u
net5
I27
nand3
net2
net8
UDClock
12u/1u
6u/1u
net8
I26
nand2
AllLow
CountDown
8u/1u
6u/1u
net2
I22
nand2
AllHigh
CountUp
8u/1u
9u/1u
AllLow
I19
net14
6u/1u

FIG 8.00AE

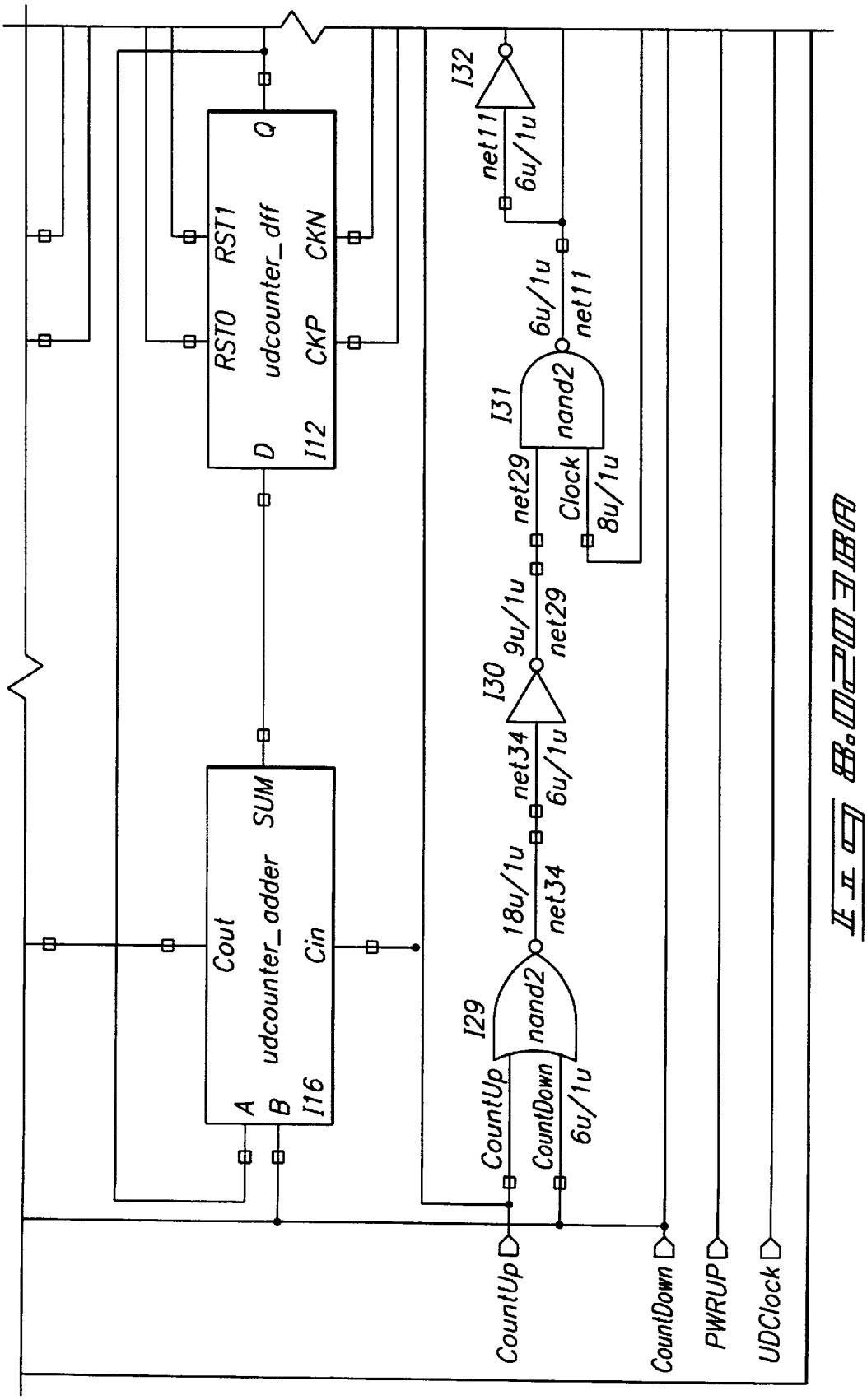

I32
net11
6u/1u
RST0
RST1
udcounter_dff
Q
D
I12
CKP
CKN
6u/1u
net11
I31
nand2
net29
Clock
8u/1u
9u/1u
net29
I30
net34
6u/1u
Cout
udcounter_adder
SUM
Cin
A
B
I16
18u/1u
net34
I29
nand2
CountUp
CountDown
6u/1u
CountUp
CountDown
PWRUP
UDClock

FIG 8.00EBA

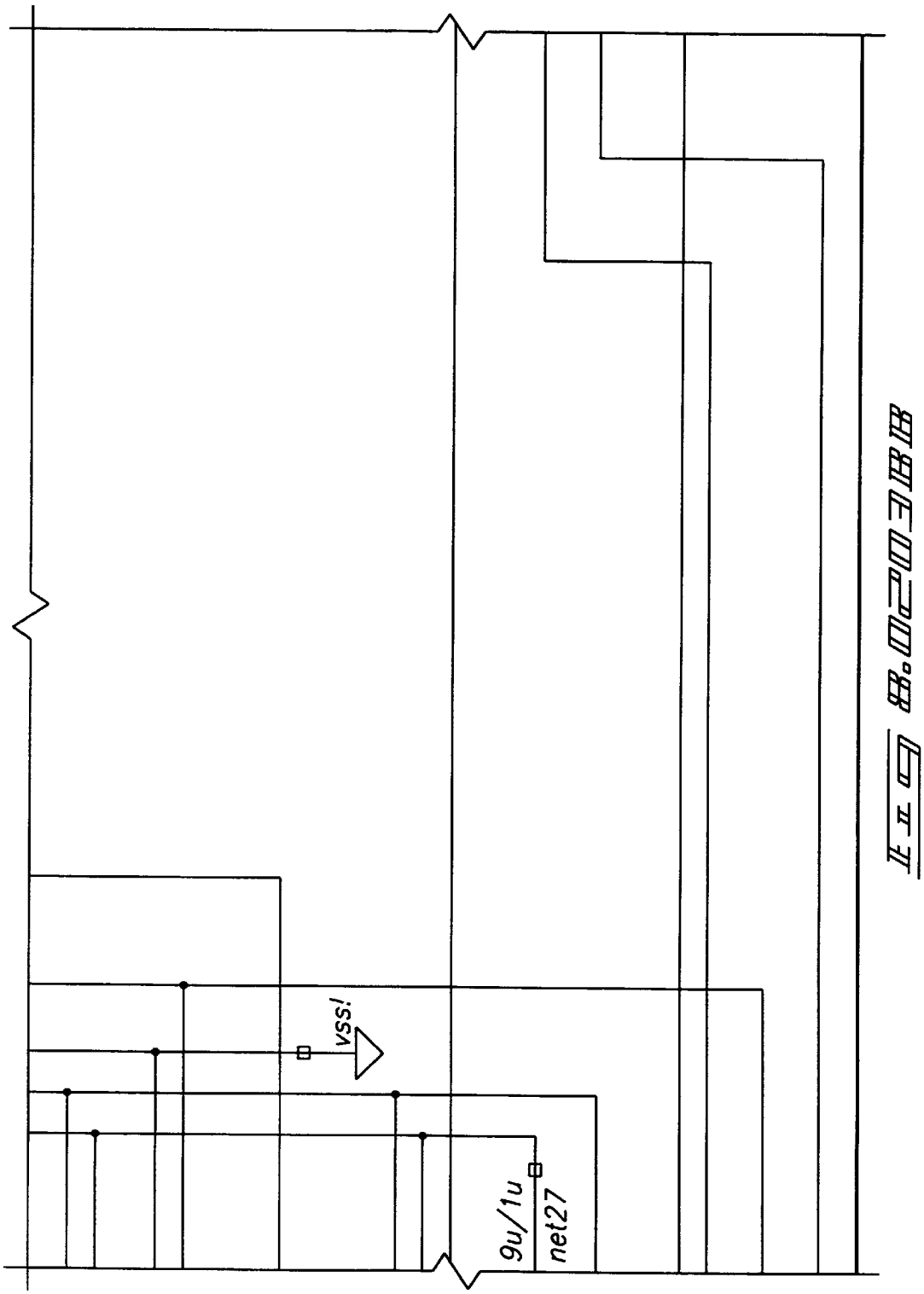
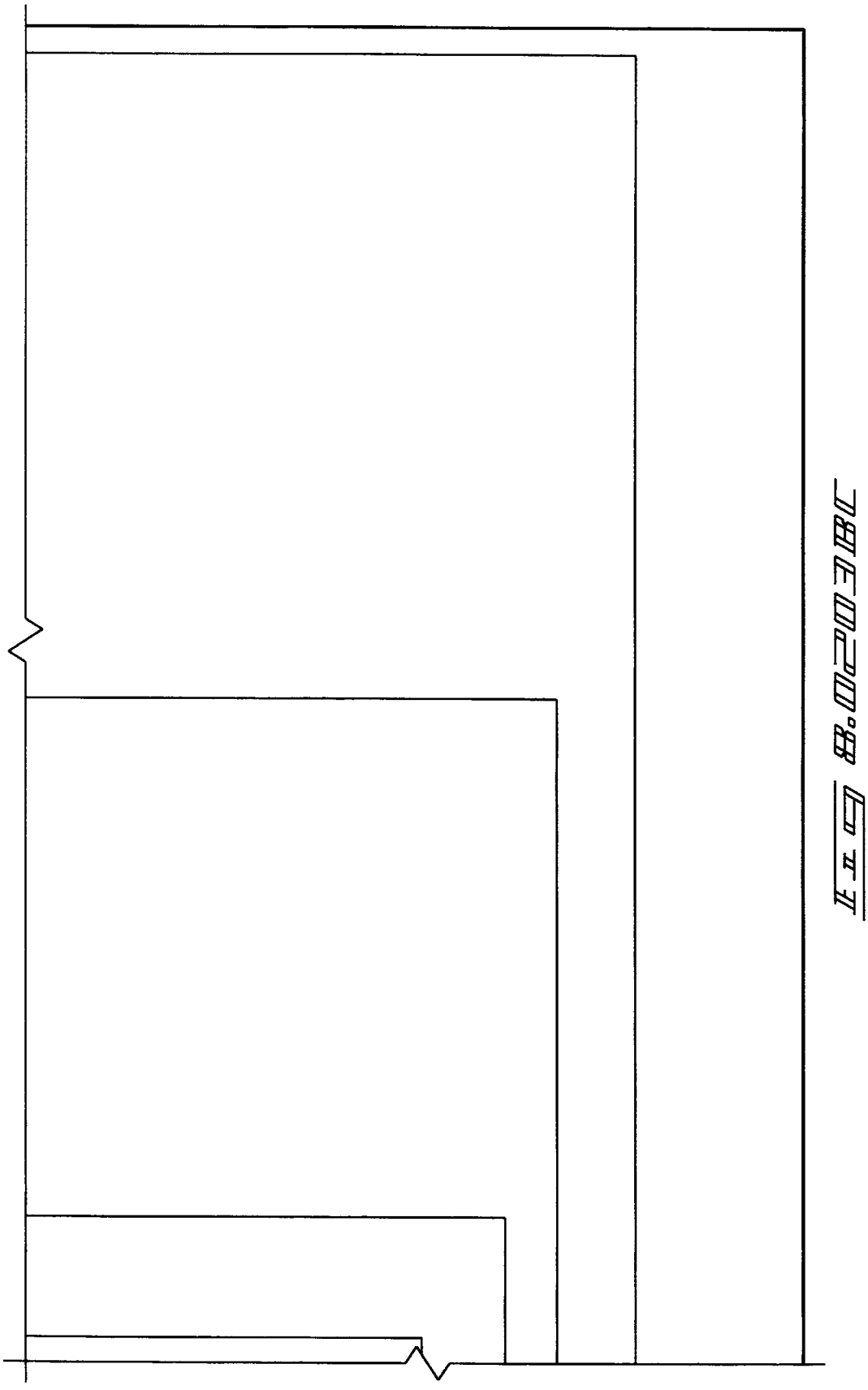


FIG 800.88
vss!
9u/1u
net27



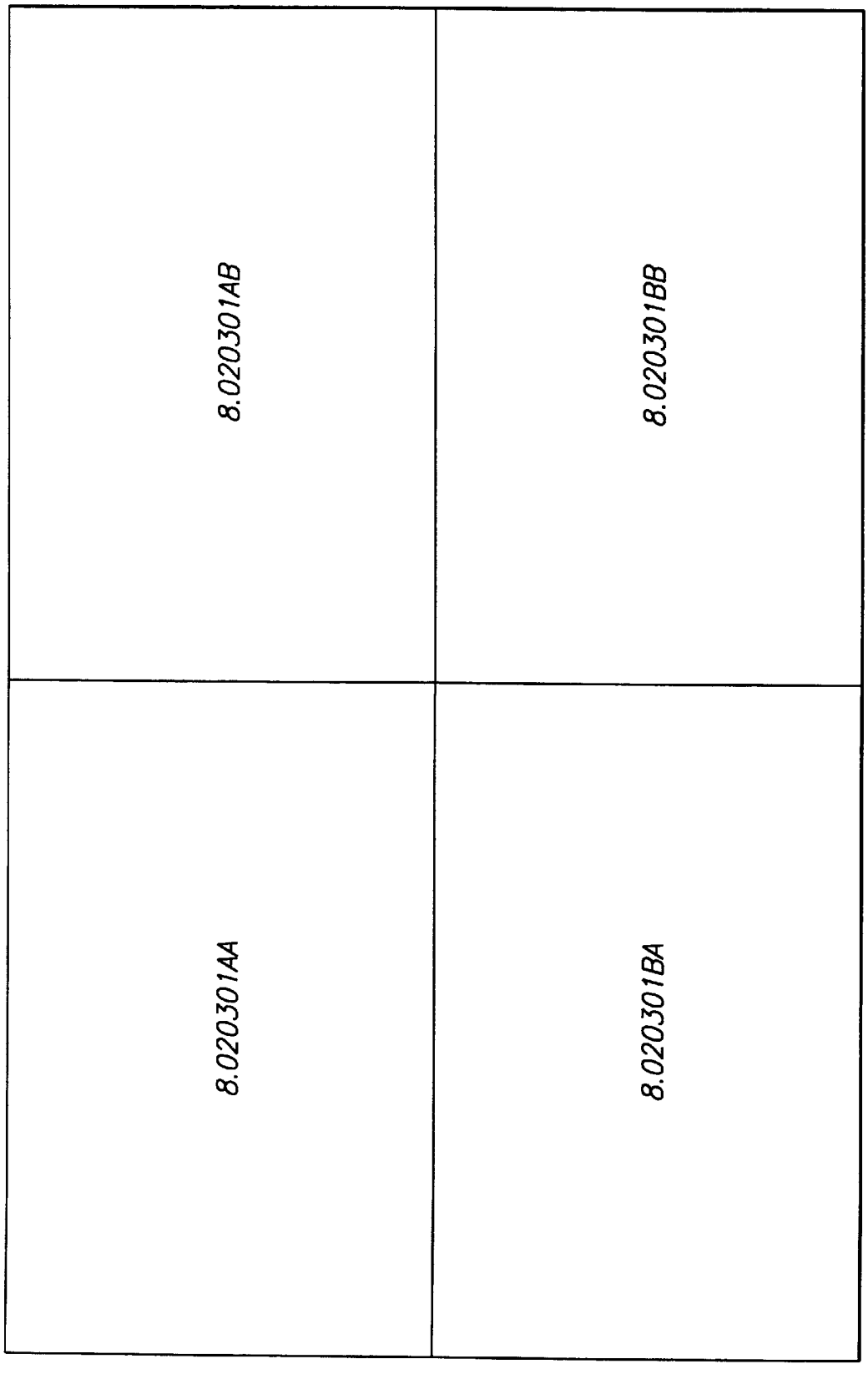


FIG 8.020301

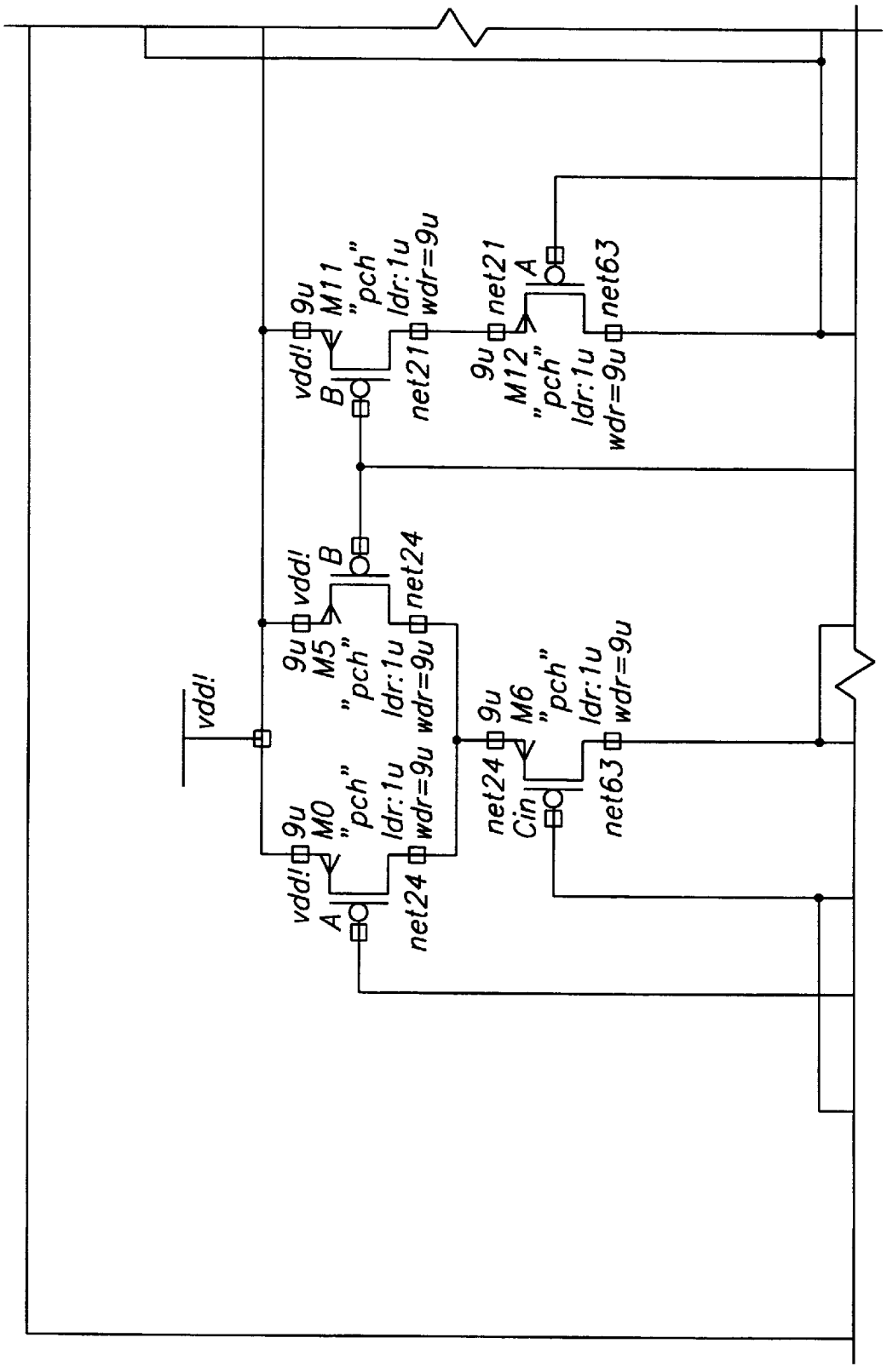


FIG 88.00E300_11AA

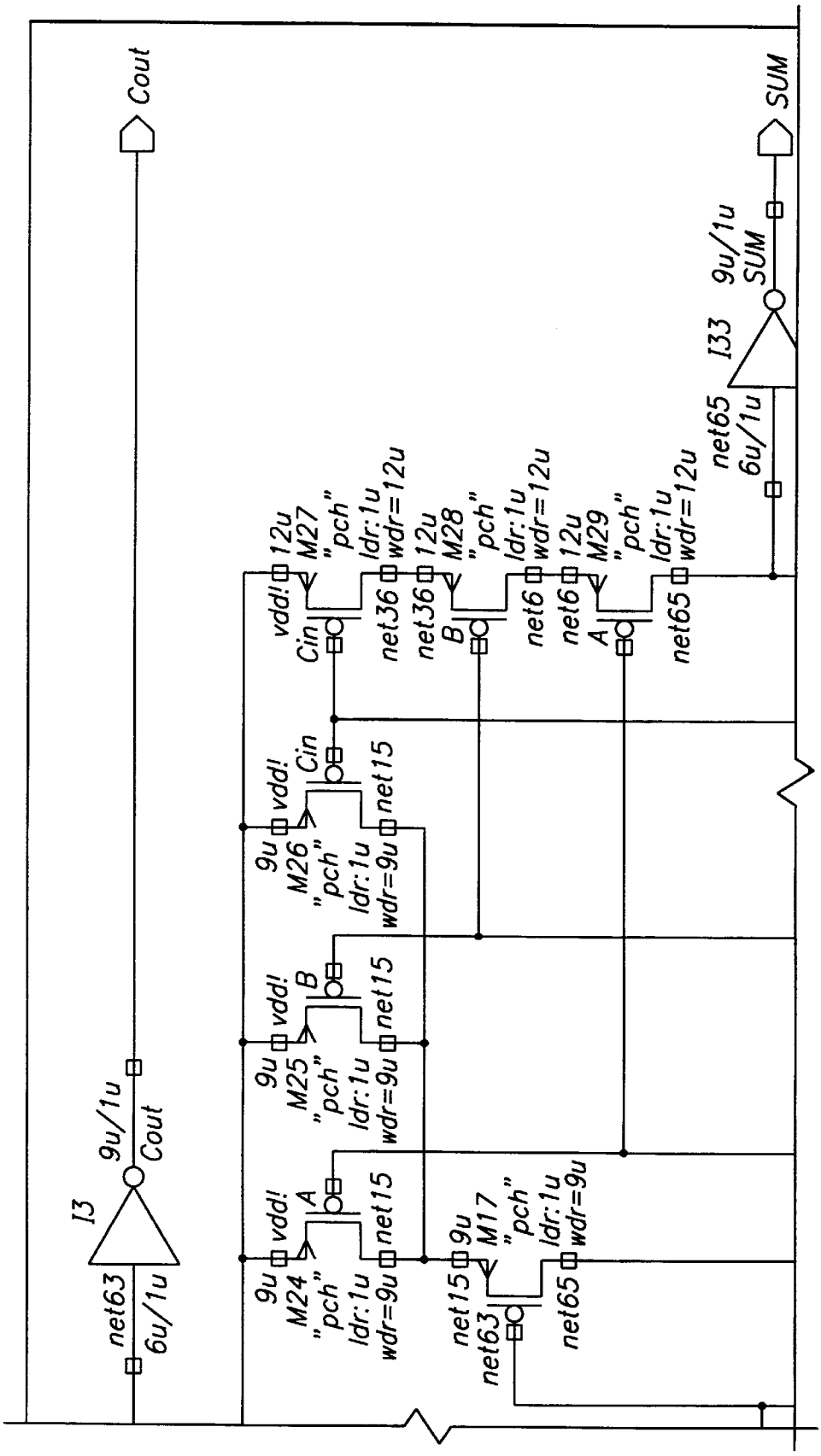


FIG. 88.00E00E00 IA/IB

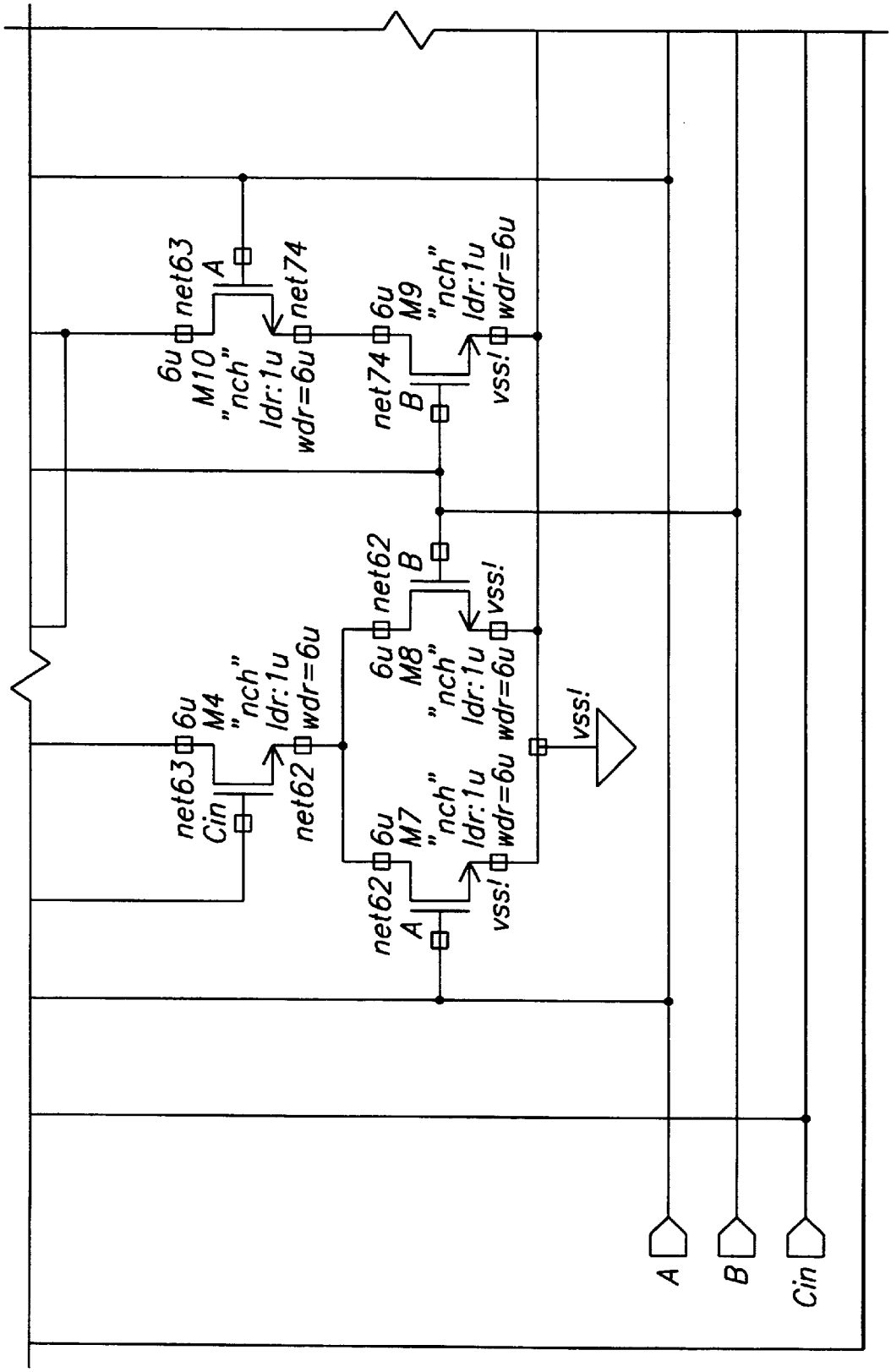
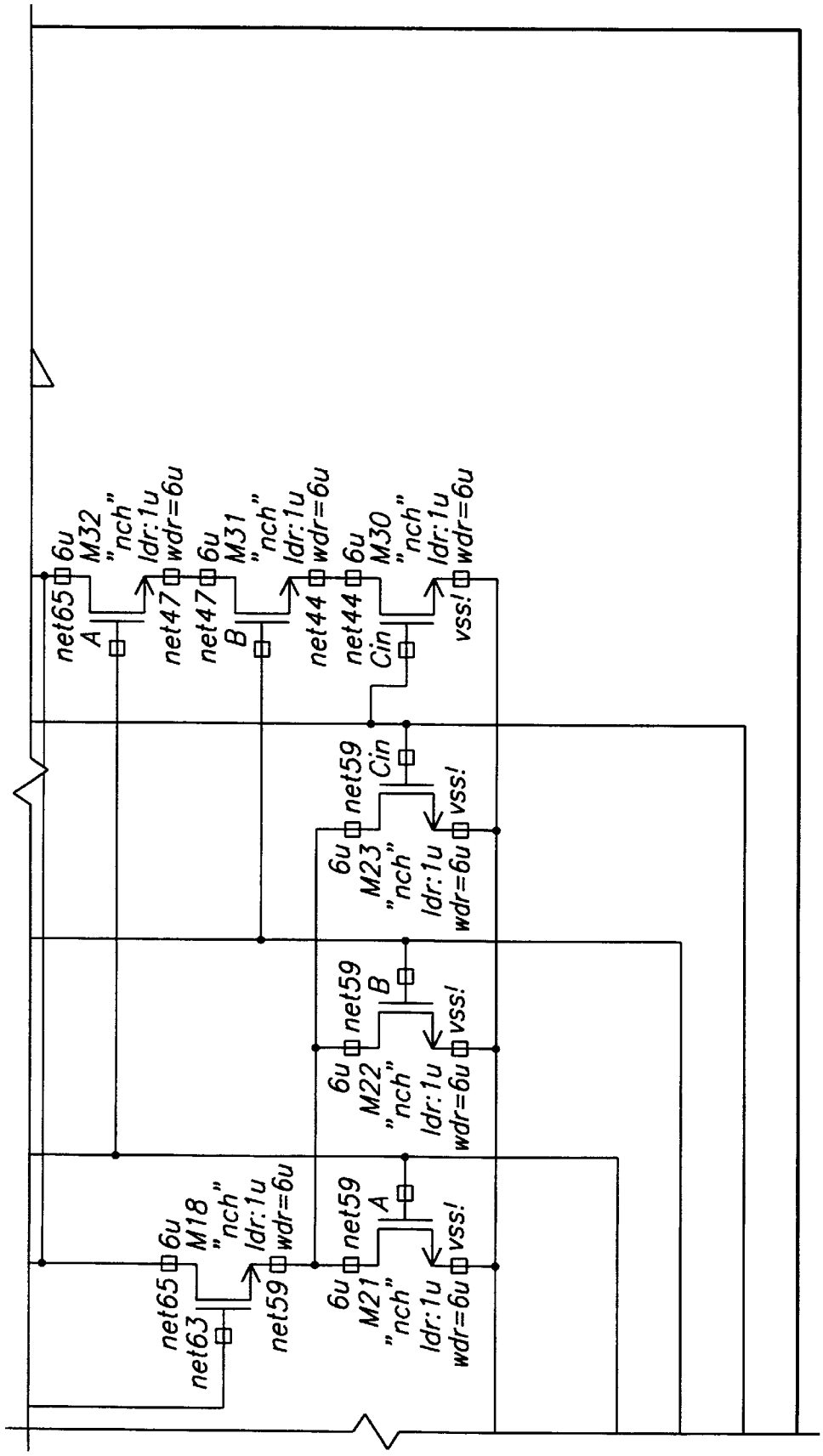

6u M10 "nch" ldr:1u wdr=6u net63 A net74
6u M9 "nch" ldr:1u wdr=6u net74 B vss!
6u M8 "nch" ldr:1u wdr=6u net62 B vss!
6u M4 "nch" ldr:1u wdr=6u net63 Cin net62
6u M7 "nch" ldr:1u wdr=6u net62 A vss!
vss!
A
B
Cin

FIG 8,008,008


net65
6u
M32
"nch"
ldr:1u
wdr=6u
A
net47
net47
6u
M31
"nch"
ldr:1u
wdr=6u
B
net44
net44
6u
M30
"nch"
ldr:1u
wdr=6u
Cin
vss!
net59
Cin
6u
M23
"nch"
ldr:1u
wdr=6u
vss!
net59
B
6u
M22
"nch"
ldr:1u
wdr=6u
vss!
net59
A
6u
M21
"nch"
ldr:1u
wdr=6u
vss!
net65
6u
M18
"nch"
ldr:1u
wdr=6u
net63
net59

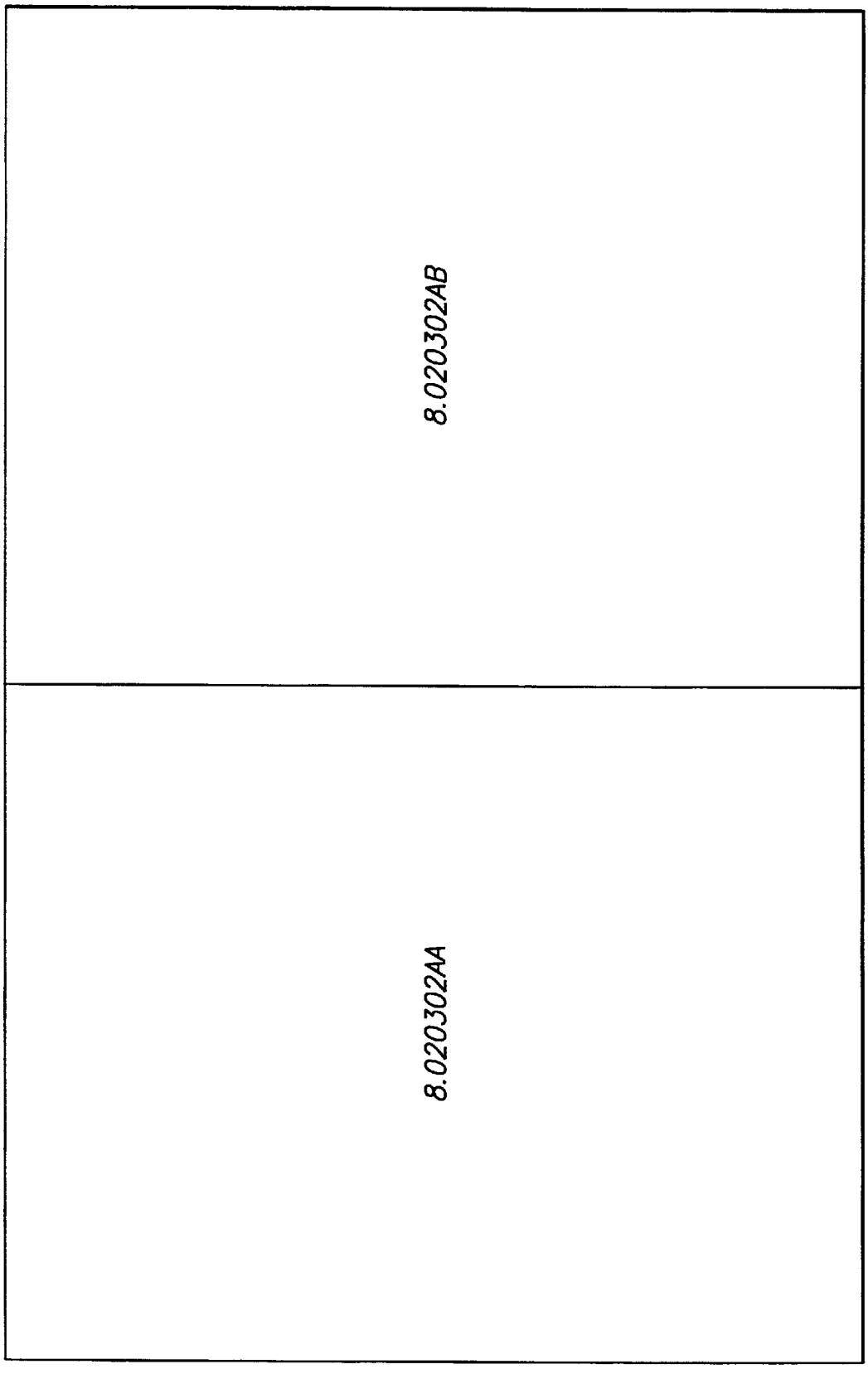


FIG 8.020302

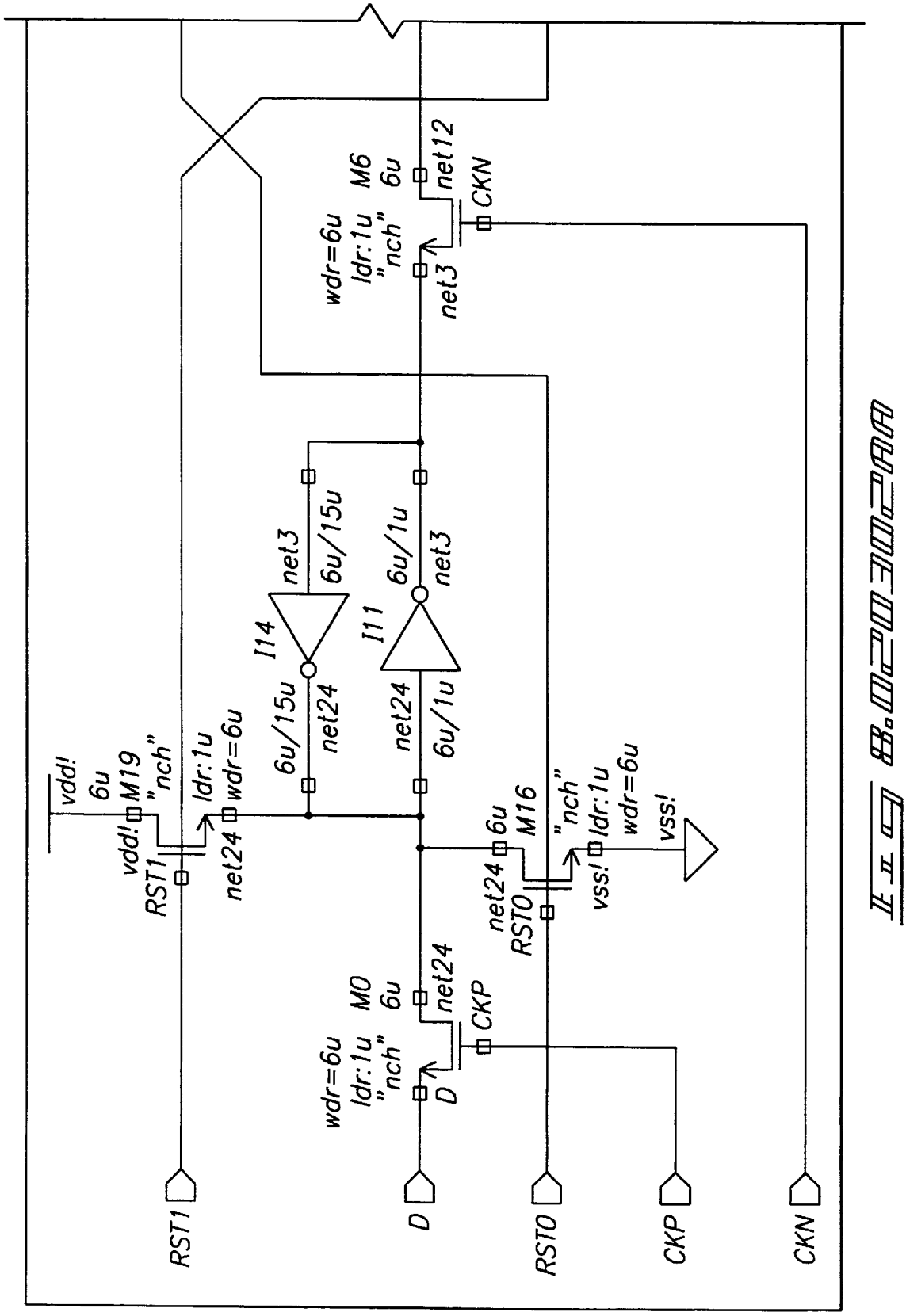


FIG 88.00200E00300AA

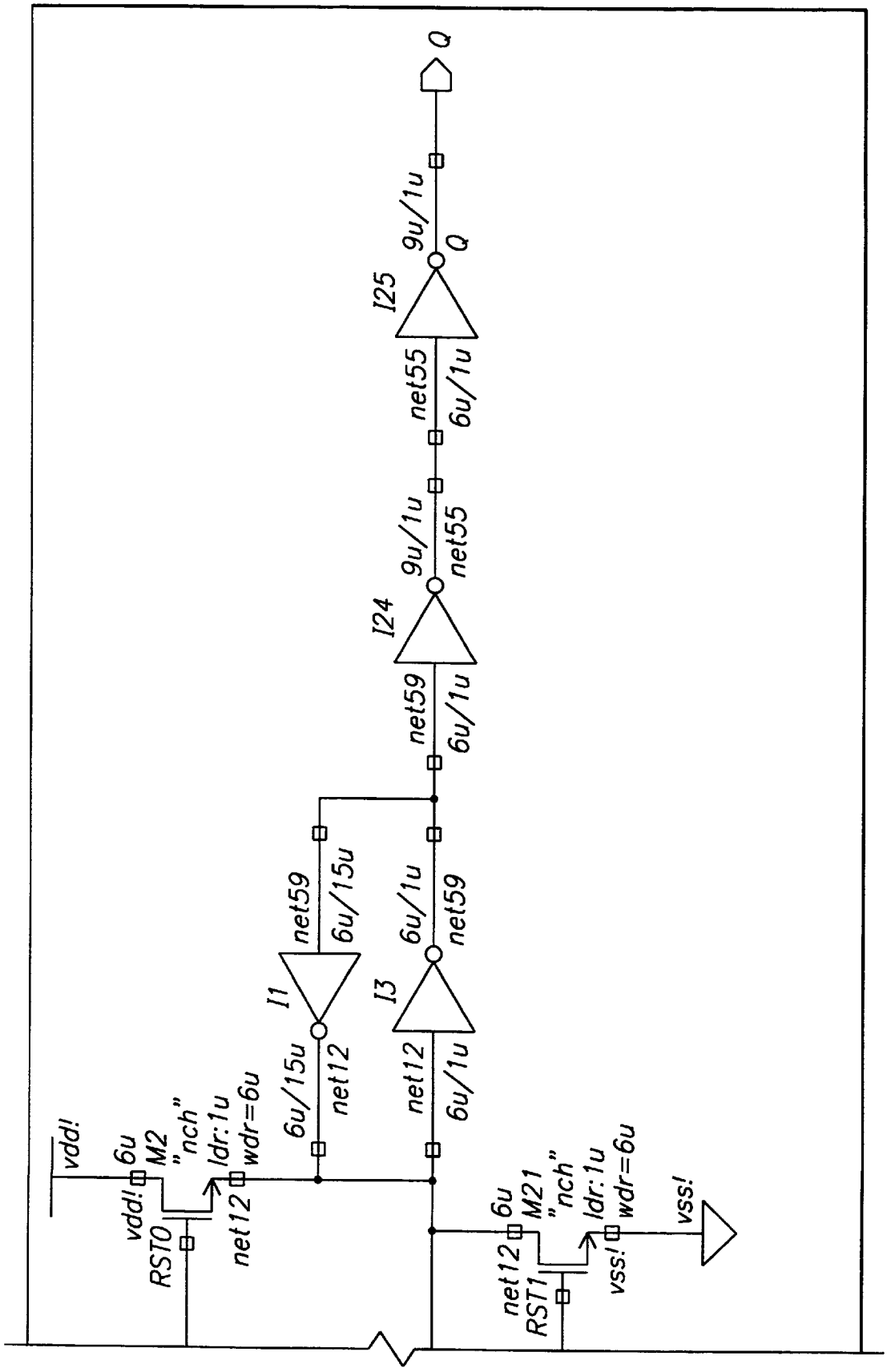

Q
I25
9u/1u
Q
net55
6u/1u
I24
9u/1u
net55
net59
6u/1u
I1
net59
6u/15u
I3
6u/1u
net59
6u/15u
net12
6u/1u
net12
vdd!
6u
M2
"nch"
ldr:1u
wdr=6u
vdd!
RST0
net12
6u
M21
"nch"
ldr:1u
wdr=6u
vss!
net12
RST1
vss!

FIG. 8.0E2AB

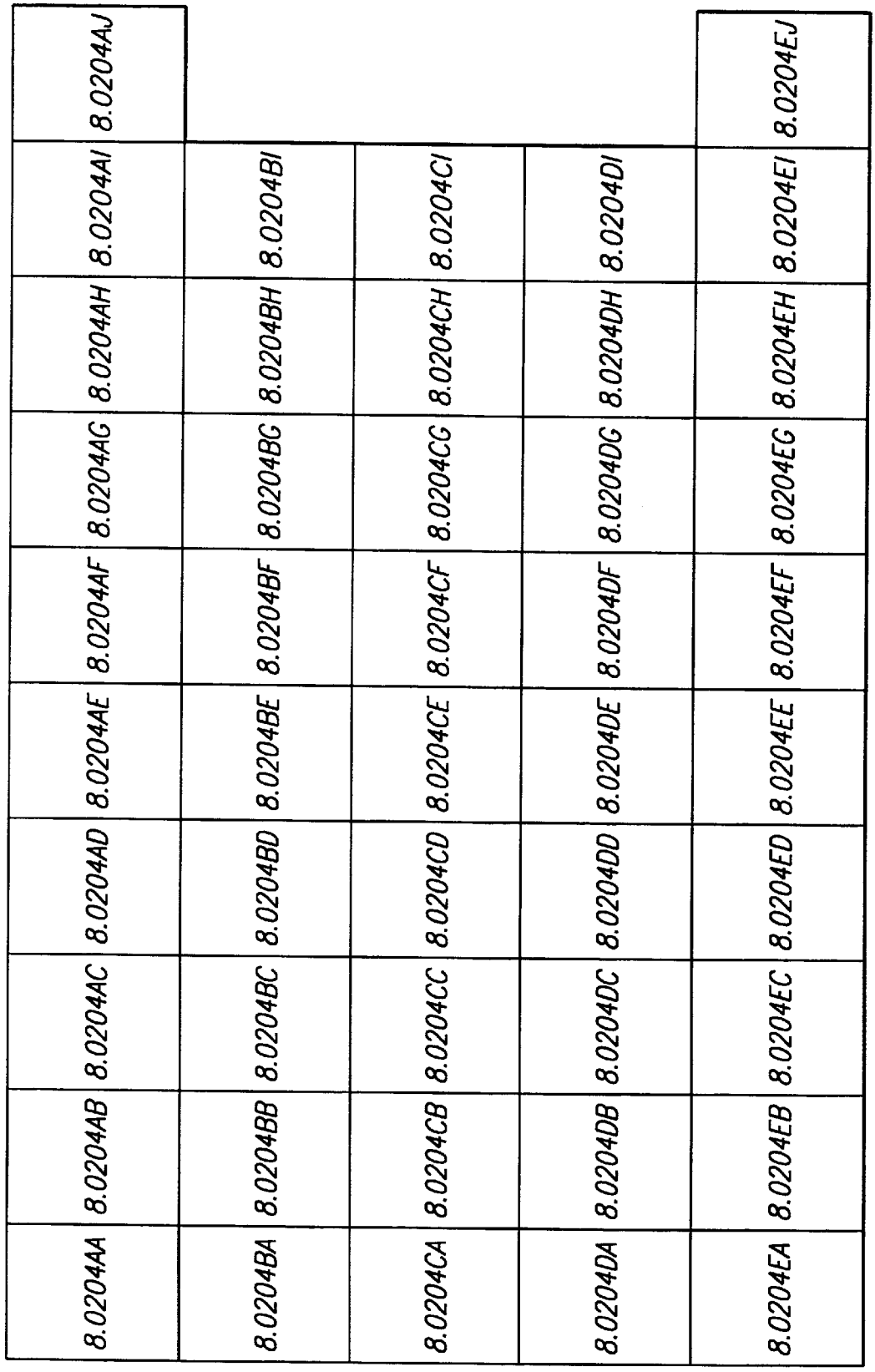

8.0204AA
8.0204AB
8.0204AC
8.0204AD
8.0204AE
8.0204AF
8.0204AG
8.0204AH
8.0204AI
8.0204AJ
8.0204BA
8.0204BB
8.0204BC
8.0204BD
8.0204BE
8.0204BF
8.0204BG
8.0204BH
8.0204BI
8.0204CA
8.0204CB
8.0204CC
8.0204CD
8.0204CE
8.0204CF
8.0204CG
8.0204CH
8.0204CI
8.0204DA
8.0204DB
8.0204DC
8.0204DD
8.0204DE
8.0204DF
8.0204DG
8.0204DH
8.0204DI
8.0204EA
8.0204EB
8.0204EC
8.0204ED
8.0204EE
8.0204EF
8.0204EG
8.0204EH
8.0204EI
8.0204EJ

FIG. 8.00204

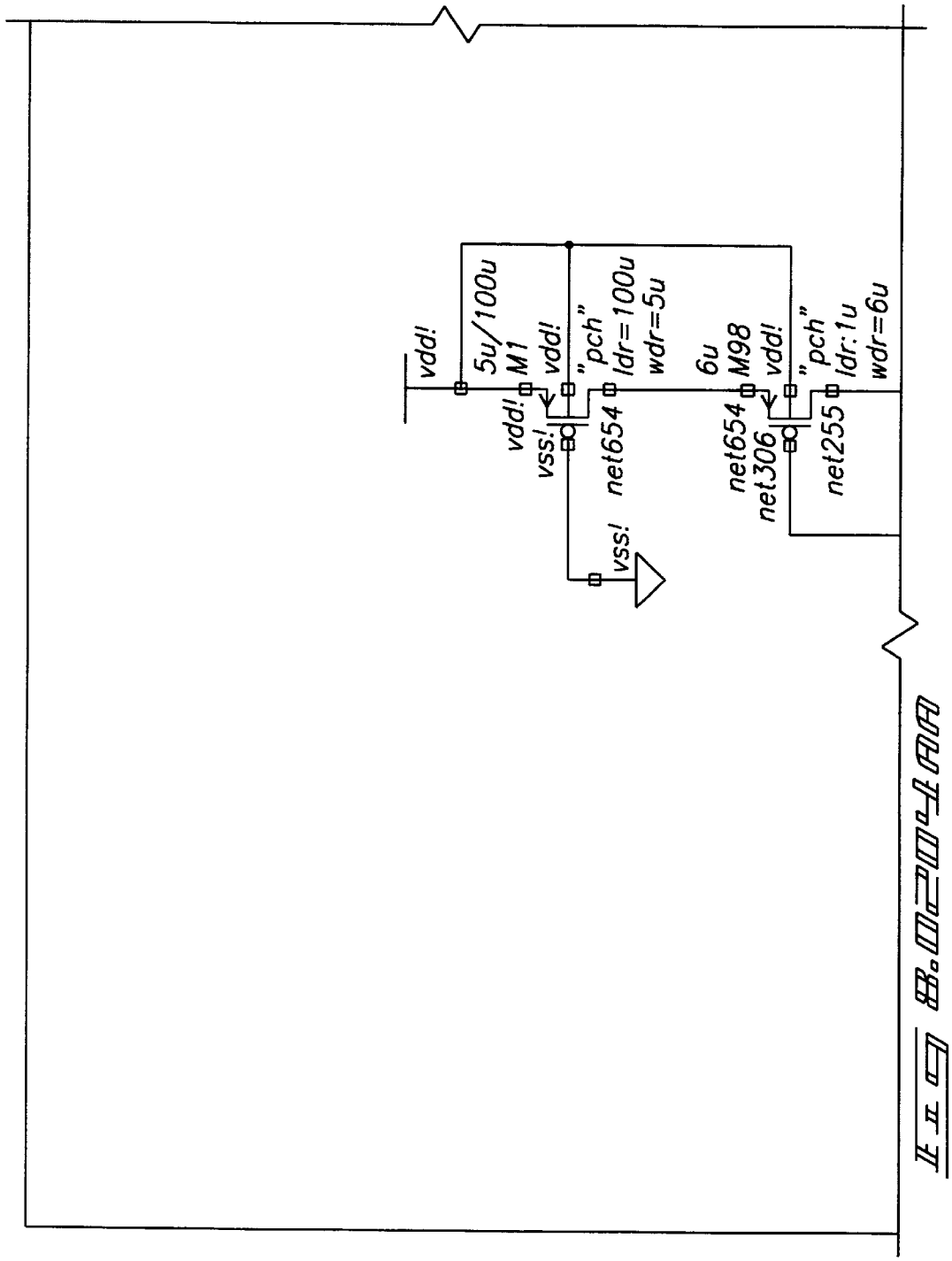

vdd!
5u/100u
M1
vdd!
"pch"
ldr=100u
wdr=5u
6u
M98
vdd!
"pch"
ldr:1u
wdr=6u
vdd!
vss!
net654
net654
net306
net255
vss!

FIG 1328

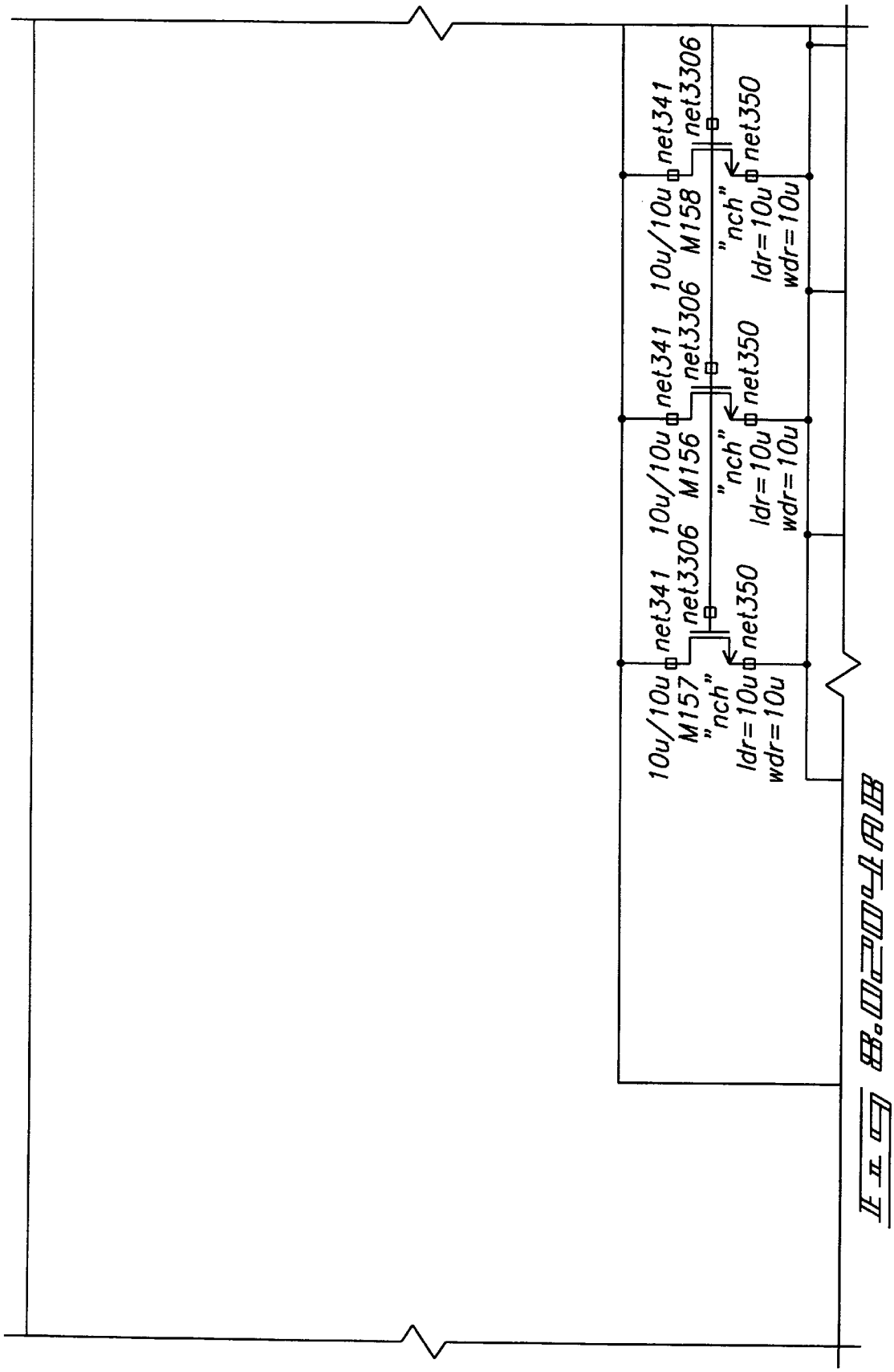

10u/10u
M157
"nch"
ldr=10u
wdr=10u
net341
net3306
net350
10u/10u
M156
"nch"
ldr=10u
wdr=10u
net341
net3306
net350
10u/10u
M158
"nch"
ldr=10u
wdr=10u
net341
net3306
net350

FIG. 8,004AB

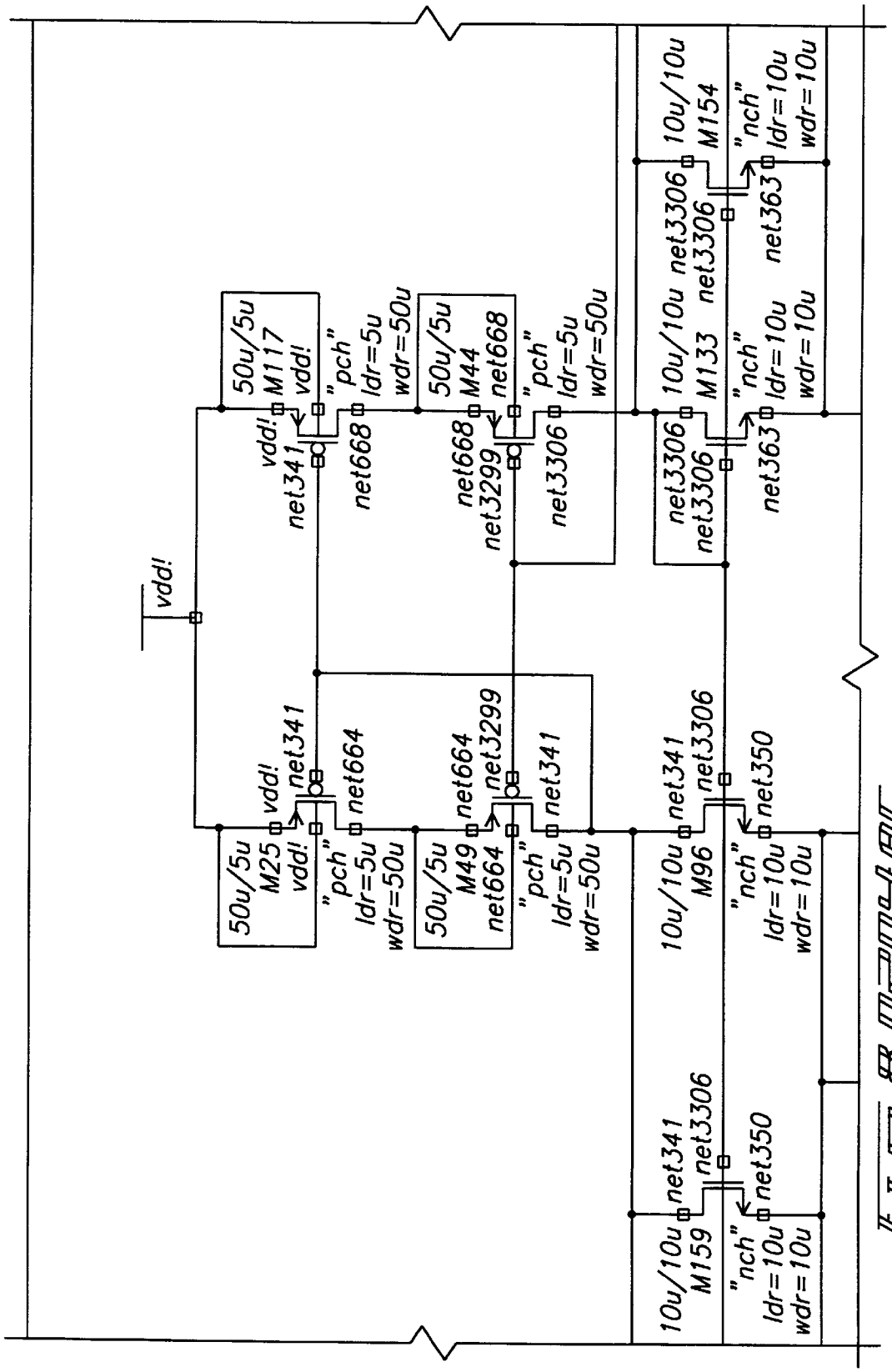

vdd!
50u/5u
M117
vdd!
net341
"pch"
ldr=5u
wdr=50u
net668
50u/5u
M44
net668
net3299
"pch"
ldr=5u
wdr=50u
net3306
10u/10u
M133
net3306
net3306
"nch"
ldr=10u
wdr=10u
net363
10u/10u
M154
net3306
"nch"
ldr=10u
wdr=10u
net363
50u/5u
M25
vdd!
net341
"pch"
ldr=5u
wdr=50u
net664
50u/5u
M49
net664
net3299
"pch"
ldr=5u
wdr=50u
net341
10u/10u
M96
net341
net3306
"nch"
ldr=10u
wdr=10u
net350
10u/10u
M159
net341
net3306
"nch"
ldr=10u
wdr=10u
net350

FIG. 88,004A

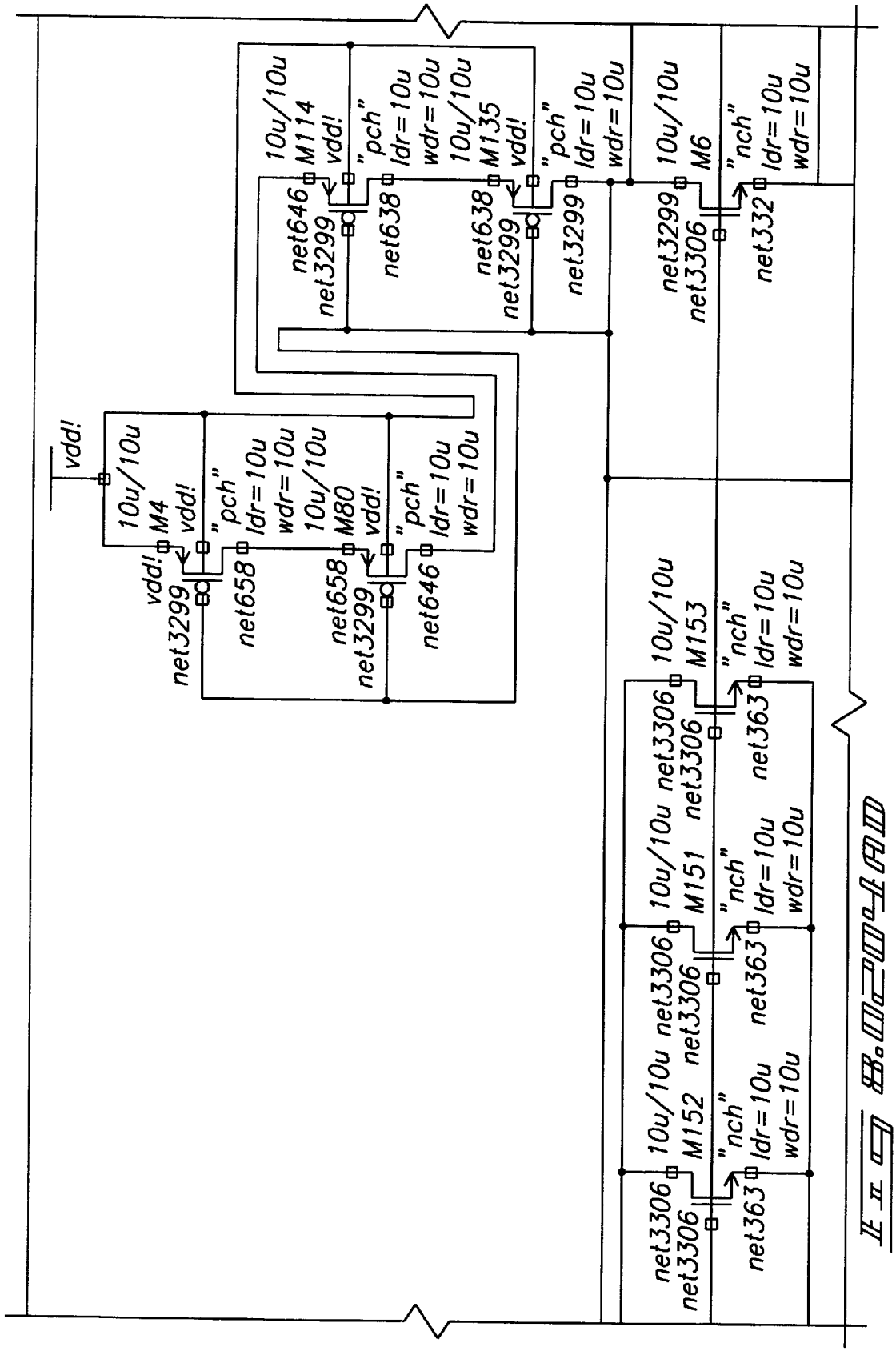

vdd!
10u/10u
M4
vdd!
"pch"
ldr=10u
wdr=10u
net658
net3299
vdd!
10u/10u
M80
vdd!
"pch"
ldr=10u
wdr=10u
net658
net3299
net646
10u/10u
M114
vdd!
"pch"
ldr=10u
wdr=10u
net646
net3299
net638
10u/10u
M135
vdd!
"pch"
ldr=10u
wdr=10u
net638
net3299
net3299
10u/10u
M6
"nch"
ldr=10u
wdr=10u
net3299
net3306
net332
10u/10u
M153
"nch"
ldr=10u
wdr=10u
net3306
net3306
net363
10u/10u
M151
"nch"
ldr=10u
wdr=10u
net3306
net3306
net363
10u/10u
M152
"nch"
ldr=10u
wdr=10u
net3306
net3306
net363

FIG. 8.0204AM

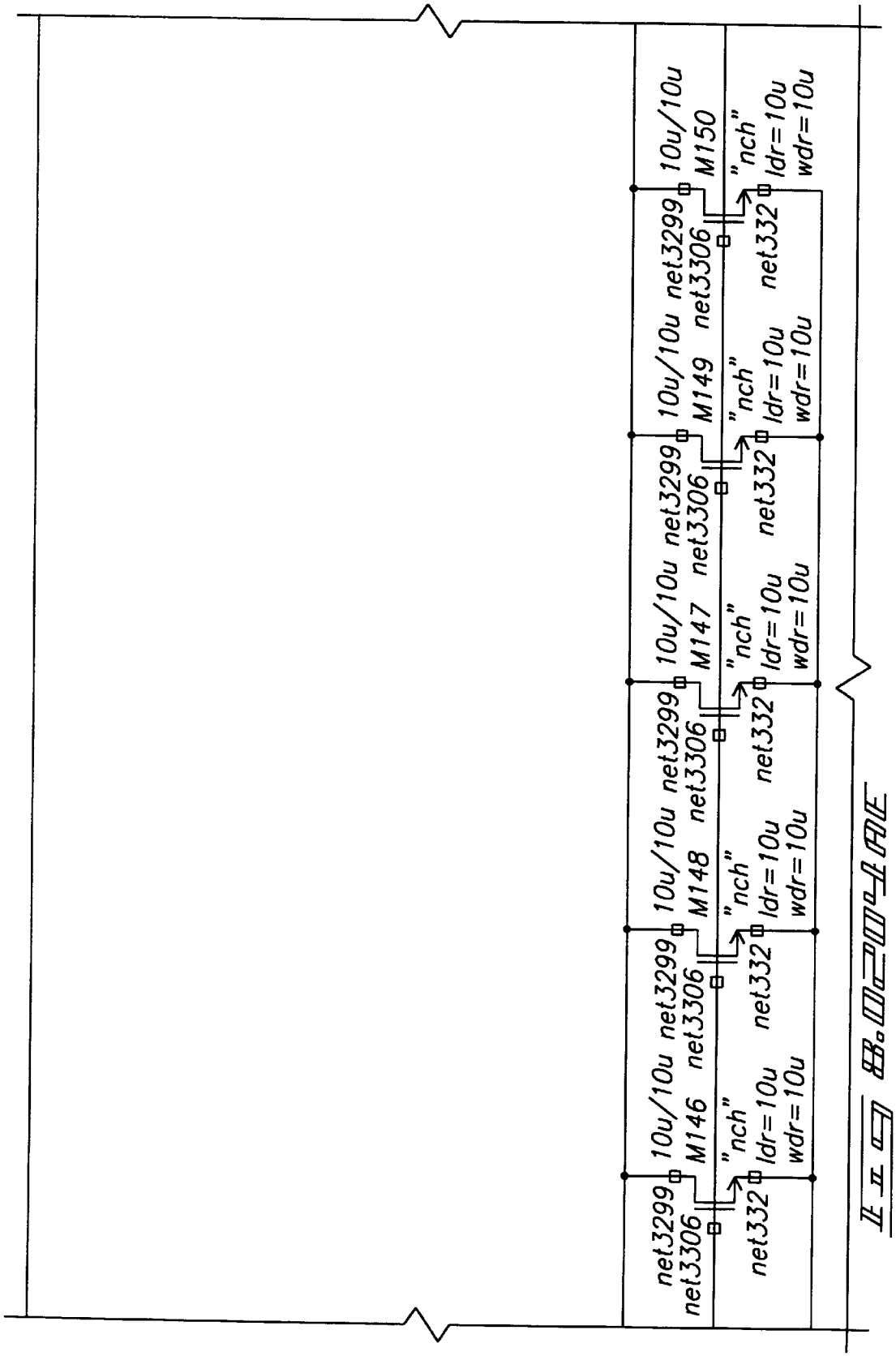

net3299
net3306
10u/10u
M146
"nch"
ldr=10u
wdr=10u
net332
10u/10u
M148
10u/10u
M147
10u/10u
M149
10u/10u
M150

FIG. 1342

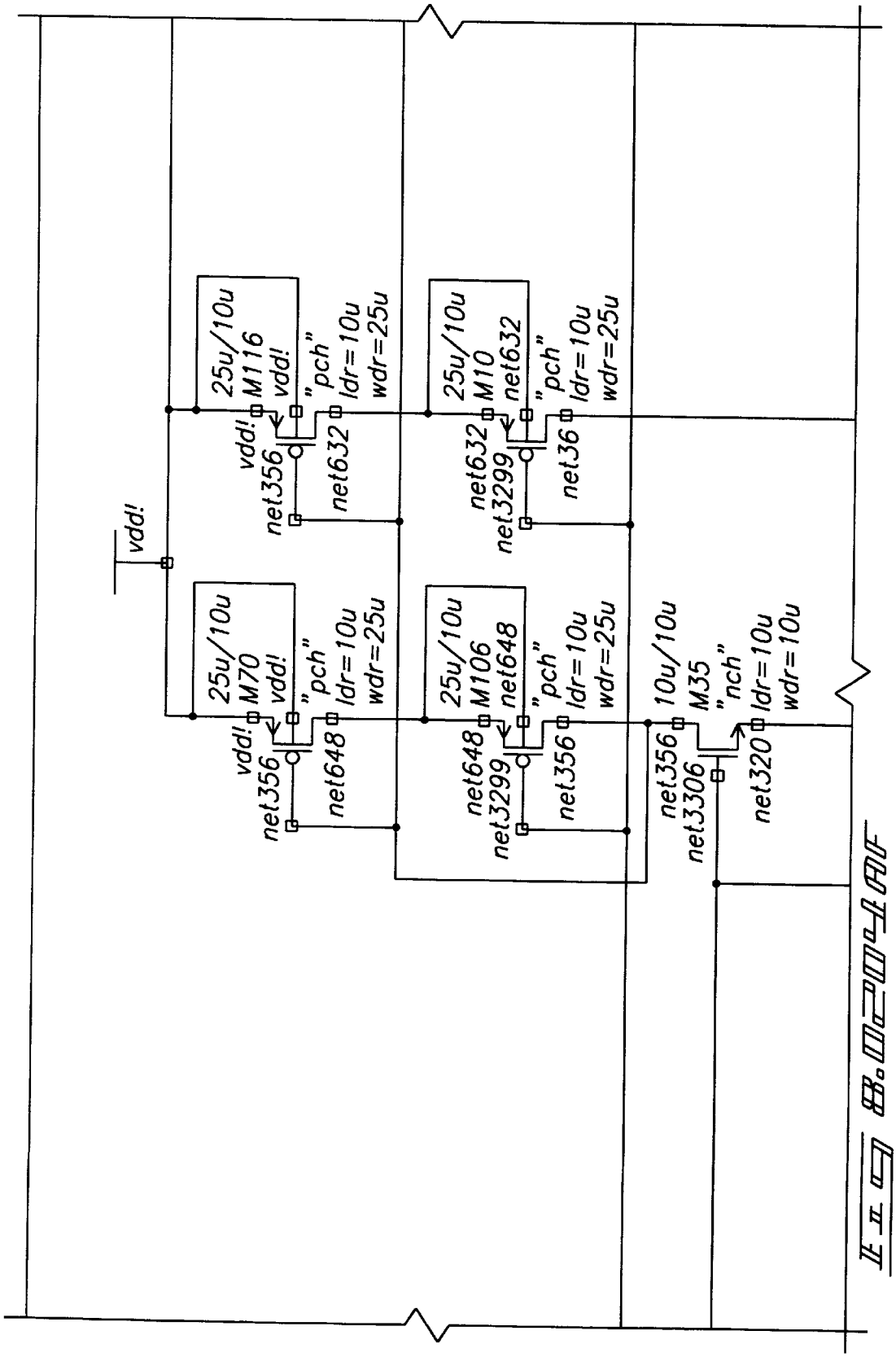

vdd!
25u/10u
M116
vdd!
"pch"
ldr=10u
wdr=25u
net356
net632
25u/10u
M10
net632
"pch"
ldr=10u
wdr=25u
net3299
net36
25u/10u
M70
vdd!
"pch"
ldr=10u
wdr=25u
net356
net648
25u/10u
M106
net648
"pch"
ldr=10u
wdr=25u
net3299
net356
10u/10u
M35
"nch"
ldr=10u
wdr=10u
net3306
net320

FIG 8.00744F

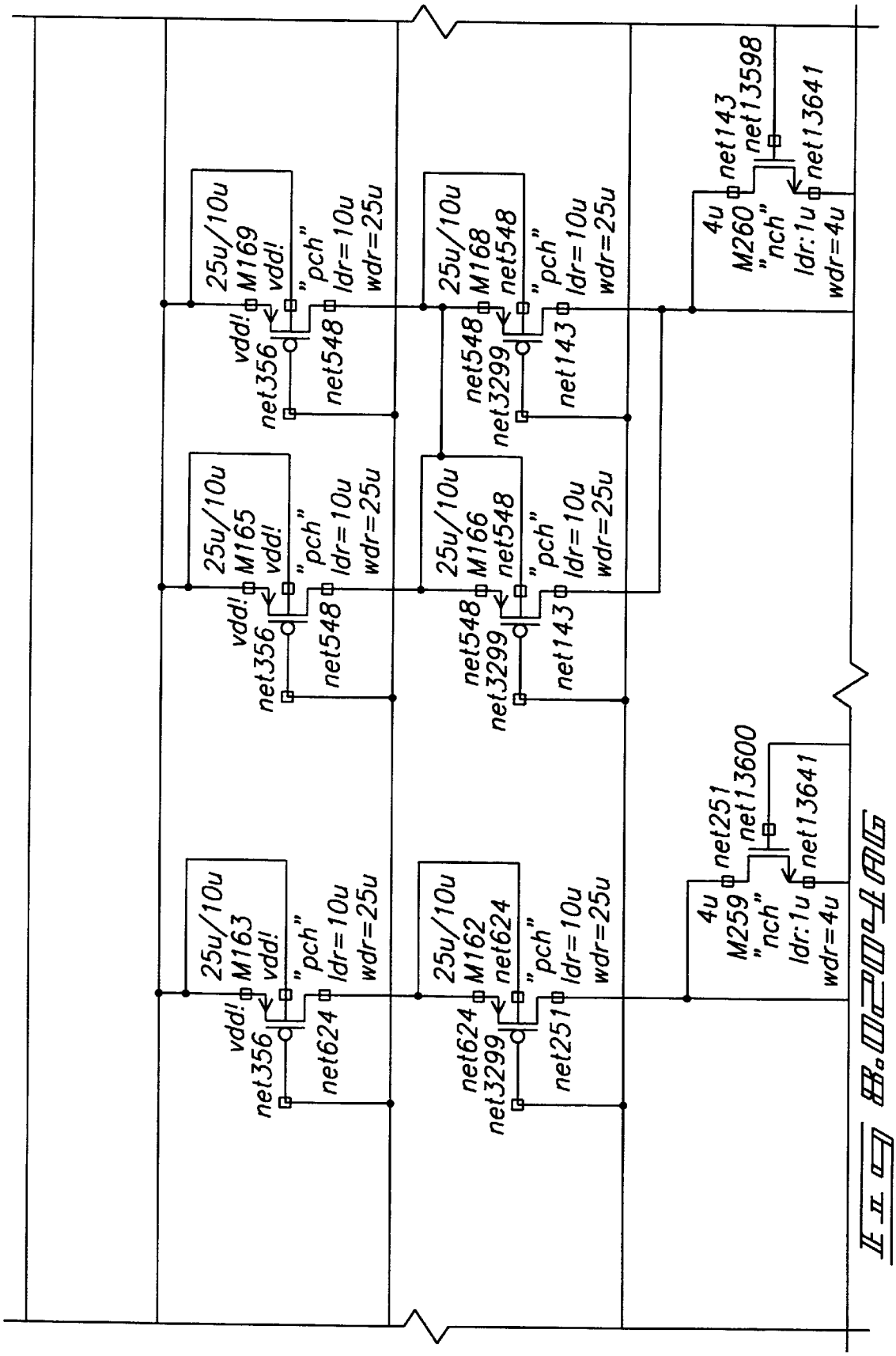

25u/10u
M169
vdd!
"pch"
ldr=10u
wdr=25u
vdd!
net356
net548
25u/10u
M168
net548
"pch"
ldr=10u
wdr=25u
net548
net3299
net143
4u
M260
"nch"
ldr:1u
wdr=4u
net143
net13598
net13641
25u/10u
M165
vdd!
"pch"
ldr=10u
wdr=25u
vdd!
net356
net548
25u/10u
M166
net548
"pch"
ldr=10u
wdr=25u
net548
net3299
net143
25u/10u
M163
vdd!
"pch"
ldr=10u
wdr=25u
vdd!
net356
net624
25u/10u
M162
net624
"pch"
ldr=10u
wdr=25u
net624
net3299
net251
4u
M259
"nch"
ldr:1u
wdr=4u
net251
net13600
net13641

FIG 8,002,AS

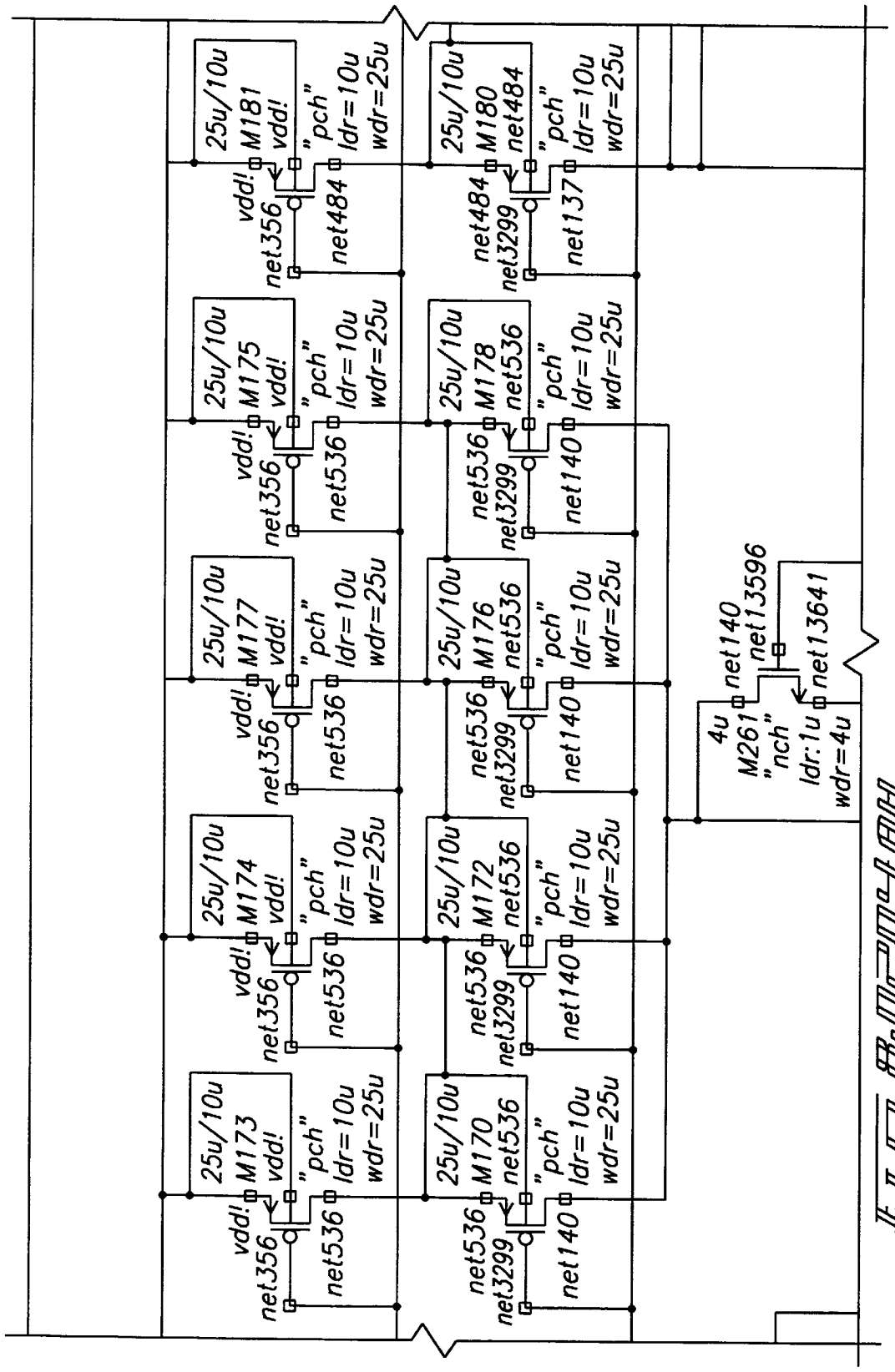


FIG. 88.00204 AHA

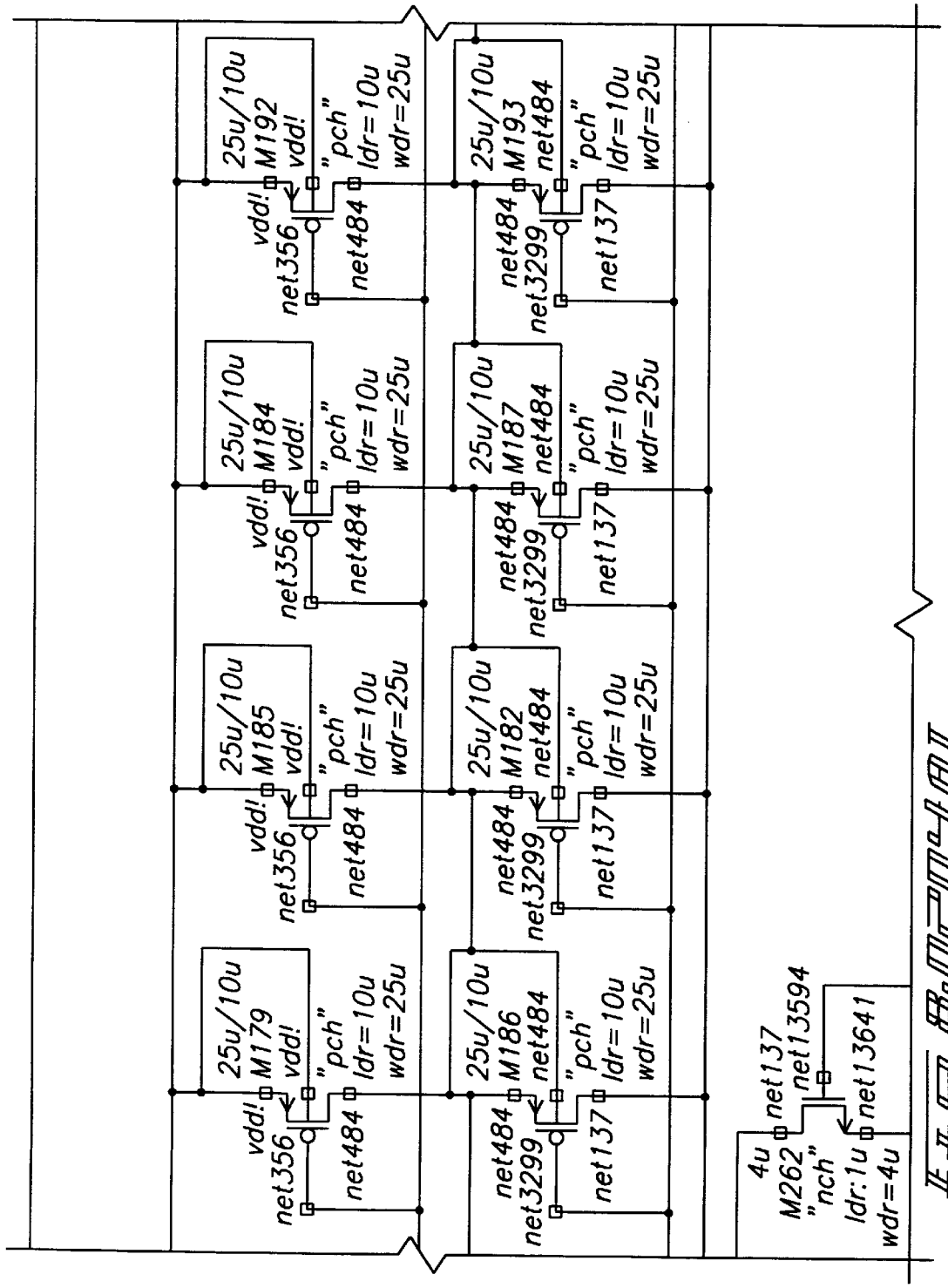


FIG. 88.00794 II

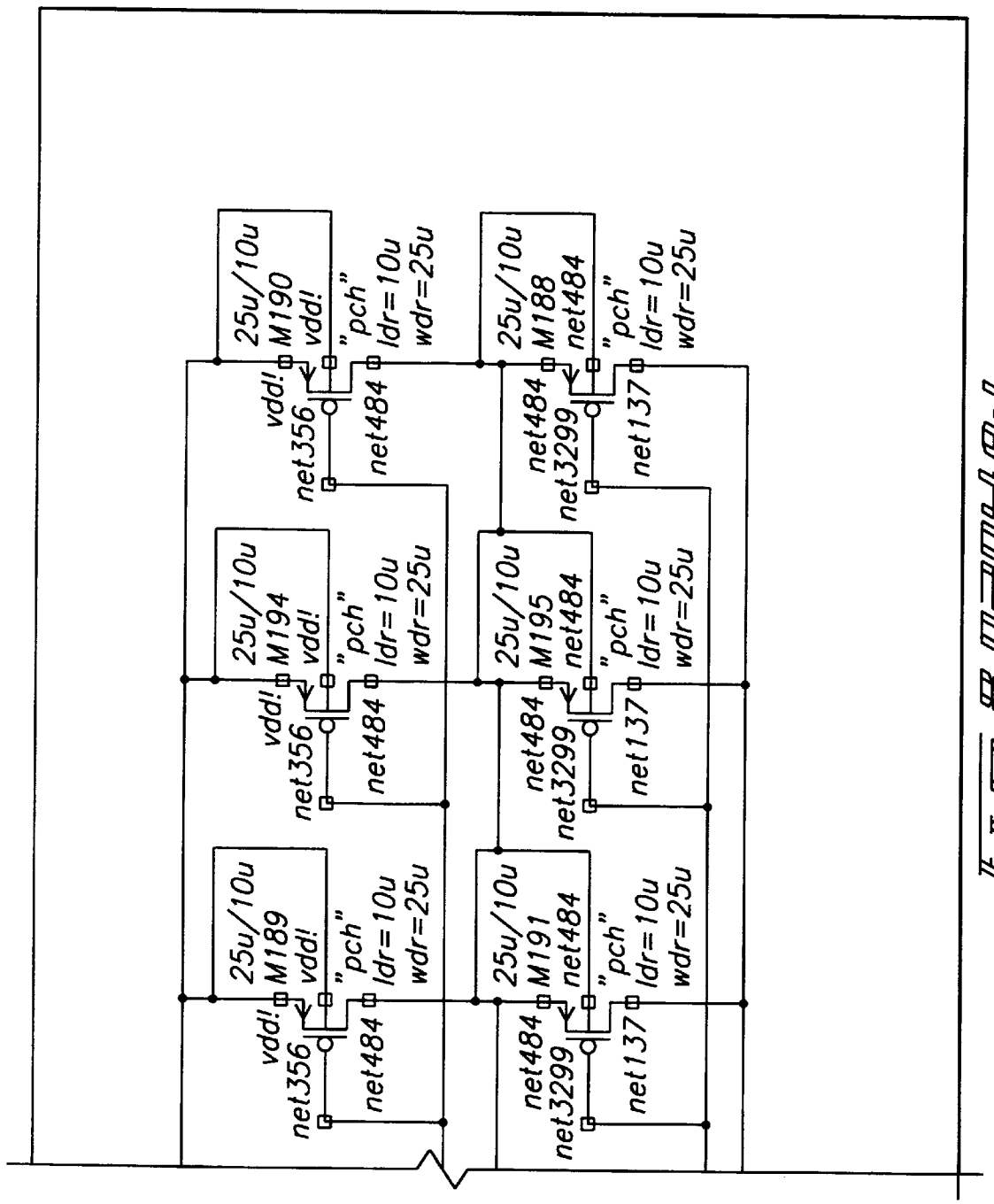

25u/10u
M190
vdd!
"pch"
ldr=10u
wdr=25u
net356
net484
25u/10u
M188
net484
"pch"
ldr=10u
wdr=25u
net3299
net137
25u/10u
M194
vdd!
"pch"
ldr=10u
wdr=25u
net356
net484
25u/10u
M195
net484
"pch"
ldr=10u
wdr=25u
net3299
net137
25u/10u
M189
vdd!
"pch"
ldr=10u
wdr=25u
net356
net484
25u/10u
M191
net484
"pch"
ldr=10u
wdr=25u
net3299
net137

FIG. 8,002

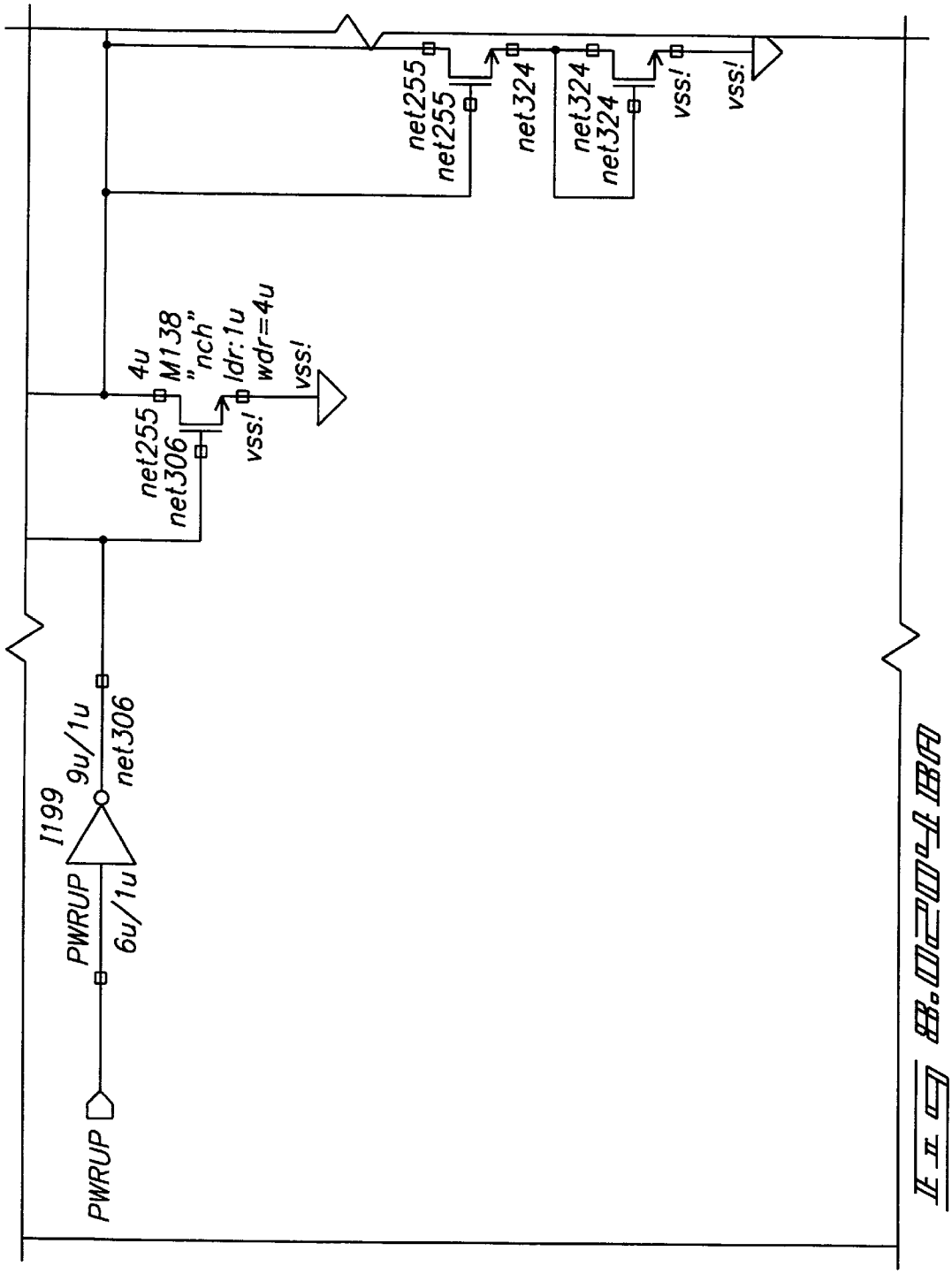

net255
net255
net324
net324
net324
vss!
vss!
4u
M138
"nch"
ldr:1u
wdr=4u
vss!
net255
net306
vss!
I199
9u/1u
net306
PWRUP
6u/1u
PWRUP

FIG 74,002,88

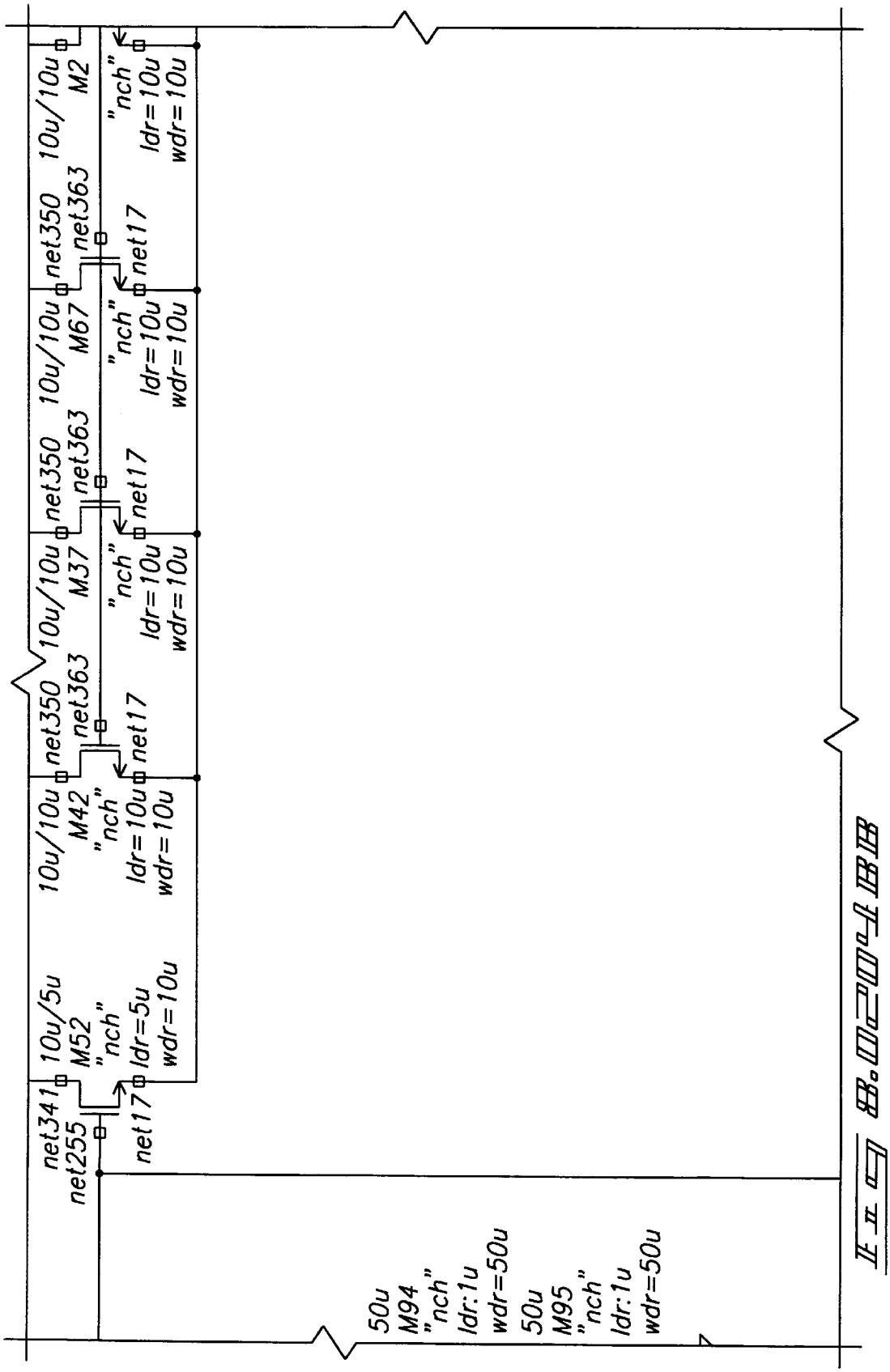
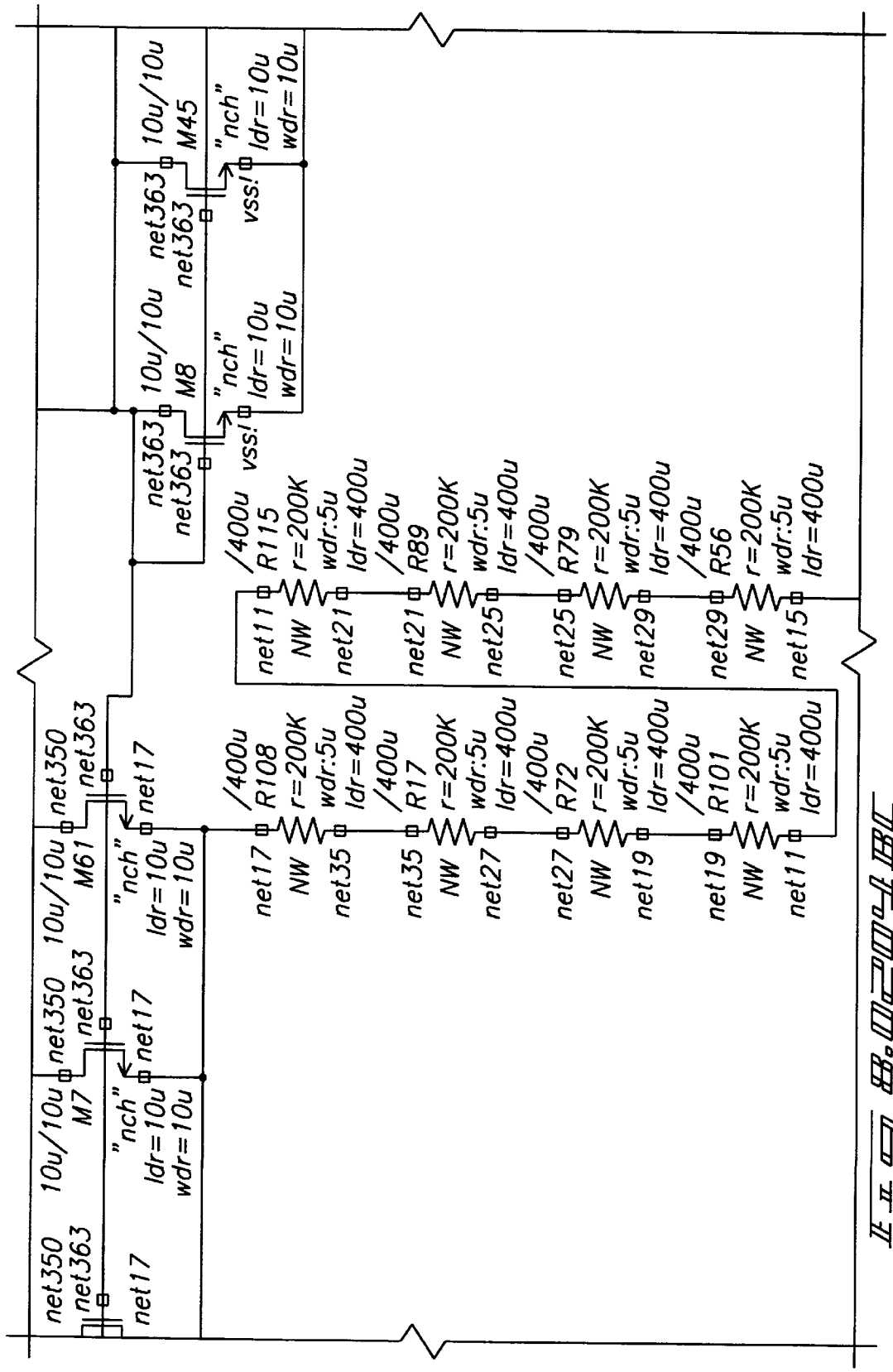

net341
net255
10u/5u
M52
"nch"
ldr=5u
wdr=10u
net17
10u/10u
M42
"nch"
ldr=10u
wdr=10u
net350
net363
net17
10u/10u
M37
"nch"
ldr=10u
wdr=10u
net350
net363
net17
10u/10u
M67
"nch"
ldr=10u
wdr=10u
net350
net363
net17
10u/10u
M2
"nch"
ldr=10u
wdr=10u
50u
M94
"nch"
ldr:1u
wdr=50u
50u
M95
"nch"
ldr:1u
wdr=50u

FIG. 88.00


net350
net363
net17
10u/10u
M7
"nch"
ldr=10u
wdr=10u
net350
net363
net17
10u/10u
M61
"nch"
ldr=10u
wdr=10u
net350
net363
net17
/400u
R108
r=200K
wdr:5u
ldr=400u
net17
NW
net35
/400u
R17
r=200K
wdr:5u
ldr=400u
net35
NW
net27
/400u
R72
r=200K
wdr:5u
ldr=400u
net27
NW
net19
/400u
R101
r=200K
wdr:5u
ldr=400u
net19
NW
net11
net363
net363
10u/10u
M8
"nch"
ldr=10u
wdr=10u
vss!
net363
net363
10u/10u
M45
"nch"
ldr=10u
wdr=10u
vss!
/400u
R115
r=200K
wdr:5u
ldr=400u
net11
NW
net21
/400u
R89
r=200K
wdr:5u
ldr=400u
net21
NW
net25
/400u
R79
r=200K
wdr:5u
ldr=400u
net25
NW
net29
/400u
R56
r=200K
wdr:5u
ldr=400u
net29
NW
net15

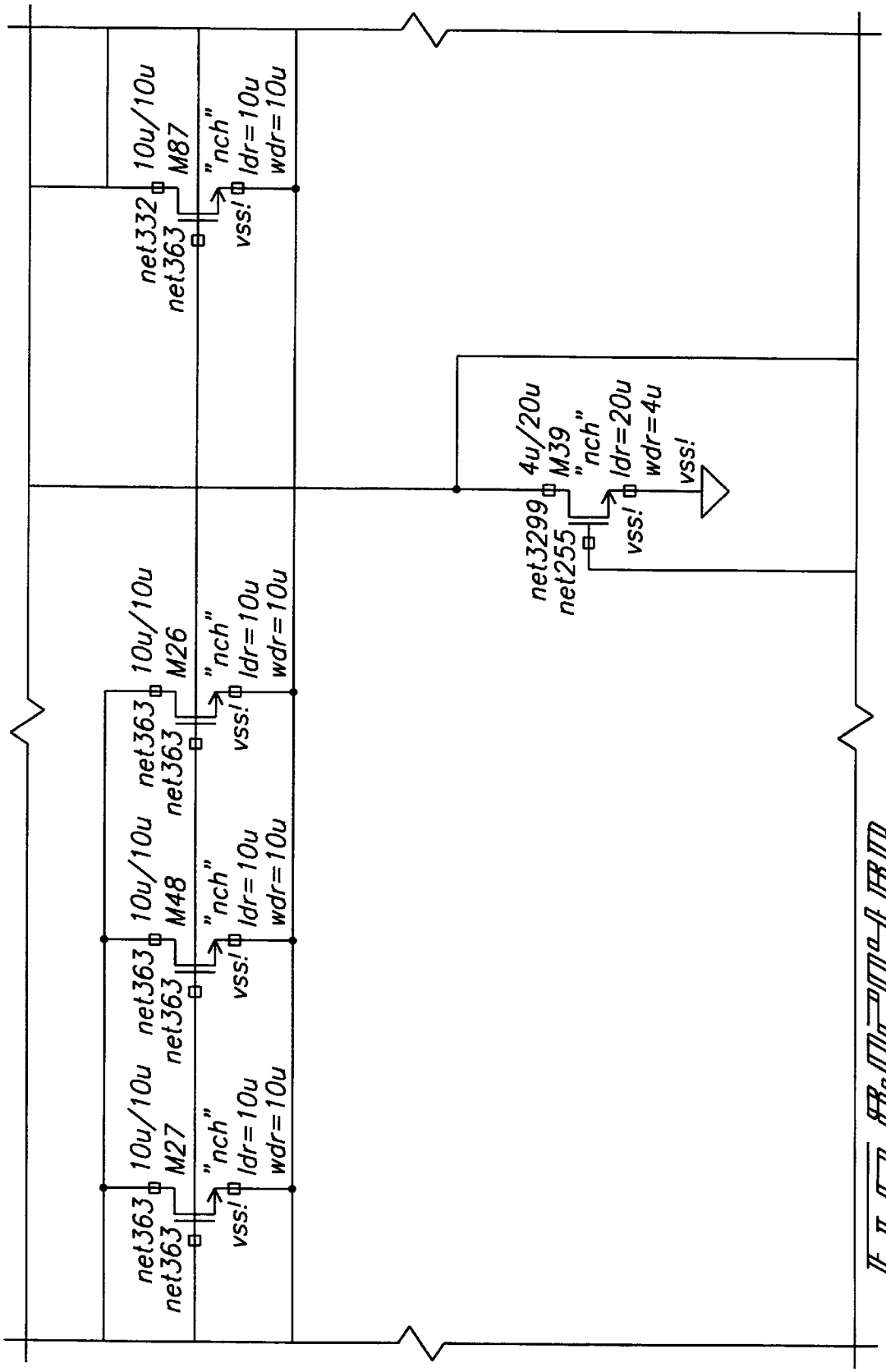

10u/10u
M87
"nch"
ldr=10u
wdr=10u
net332
net363
vss!
4u/20u
M39
"nch"
ldr=20u
wdr=4u
vss!
net3299
net255
vss!
10u/10u
M26
"nch"
ldr=10u
wdr=10u
net363
net363
vss!
10u/10u
M48
"nch"
ldr=10u
wdr=10u
net363
net363
vss!
10u/10u
M27
"nch"
ldr=10u
wdr=10u
net363
net363
vss!

FIG 88.00200

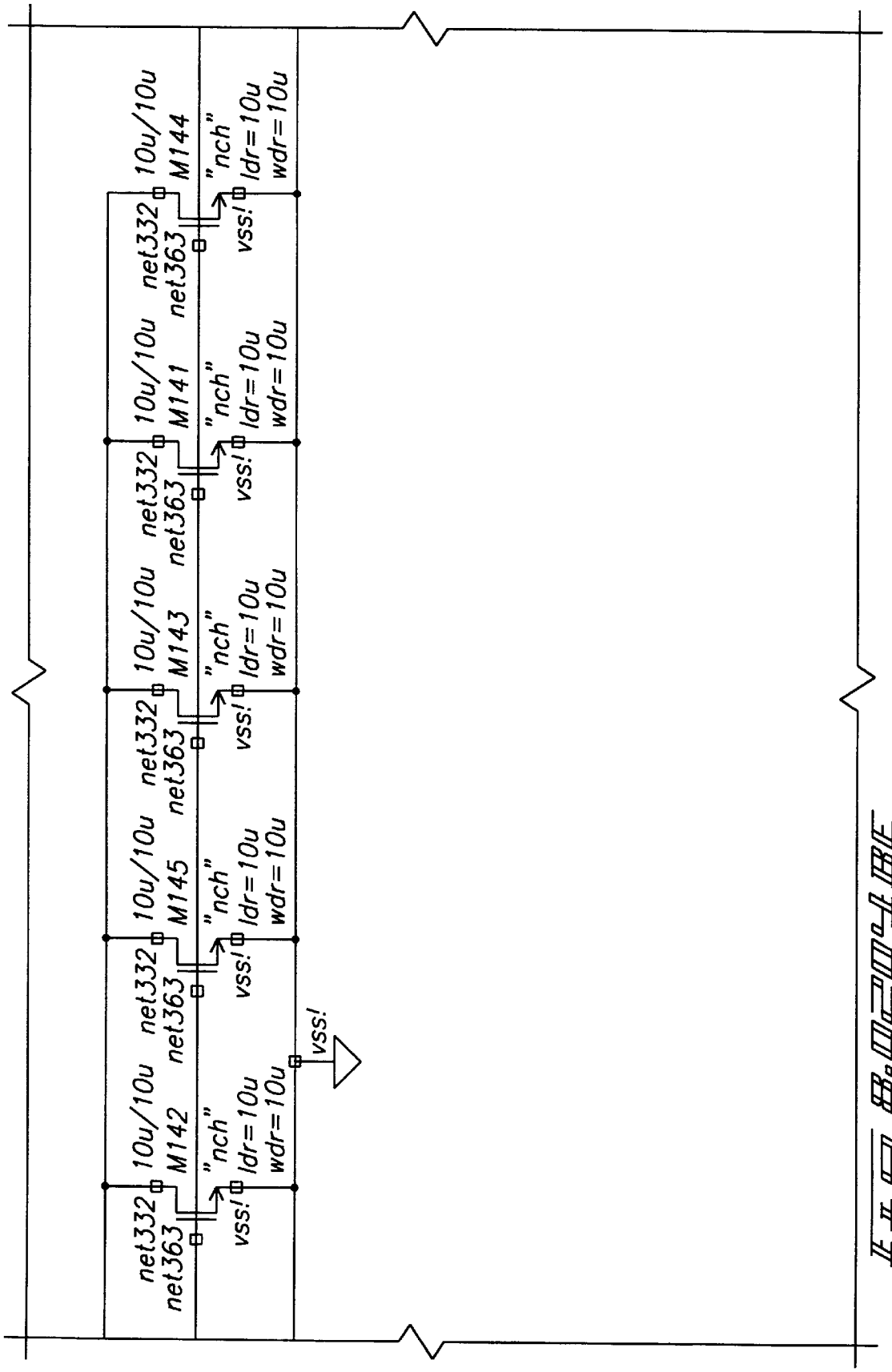


FIG. 88.00204 IBE

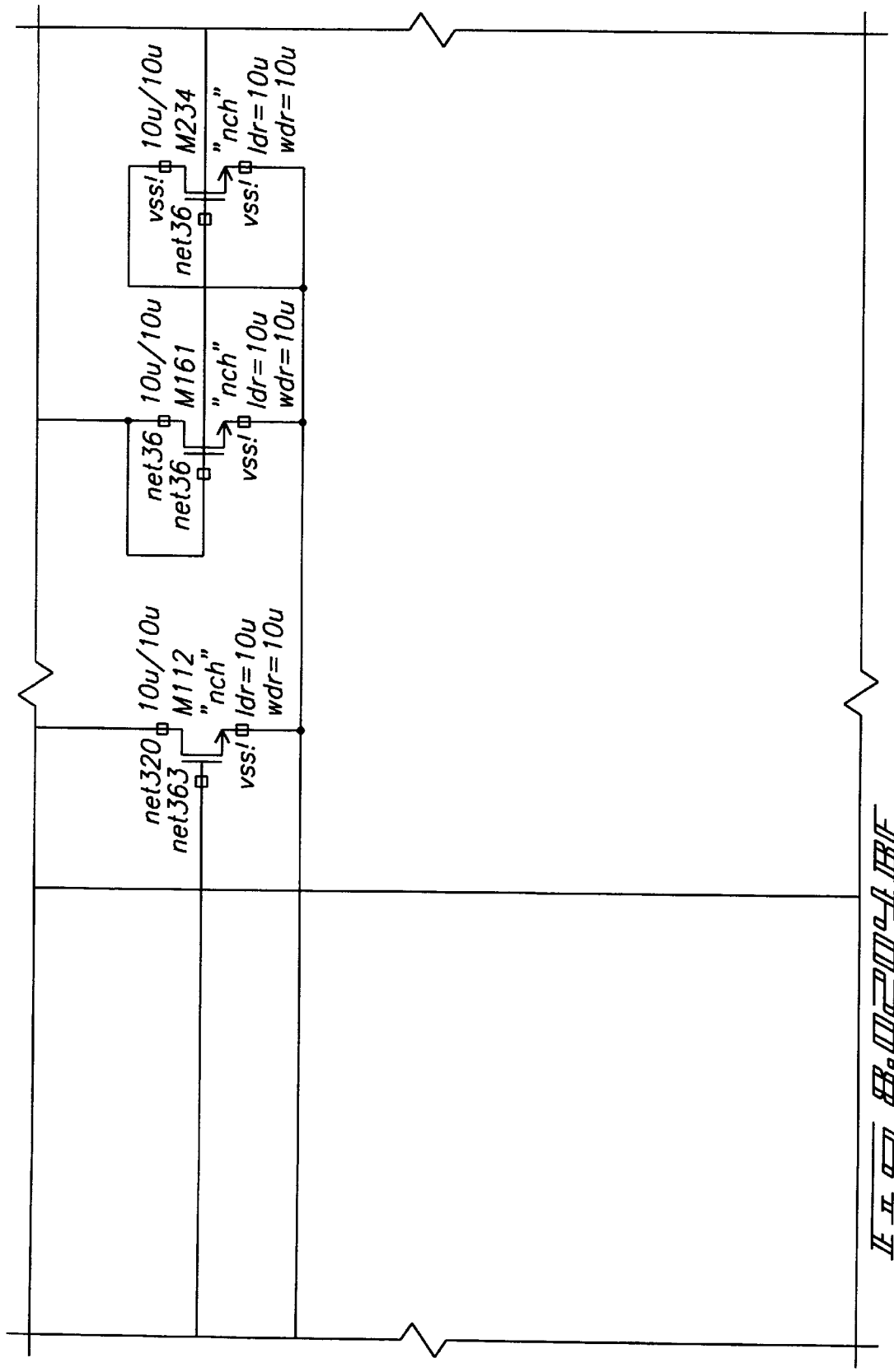

10u/10u
M234
"nch"
ldr=10u
wdr=10u
vss!
net36
vss!
10u/10u
M161
"nch"
ldr=10u
wdr=10u
net36
net36
vss!
10u/10u
M112
"nch"
ldr=10u
wdr=10u
net320
net363
vss!

FIG. 1353

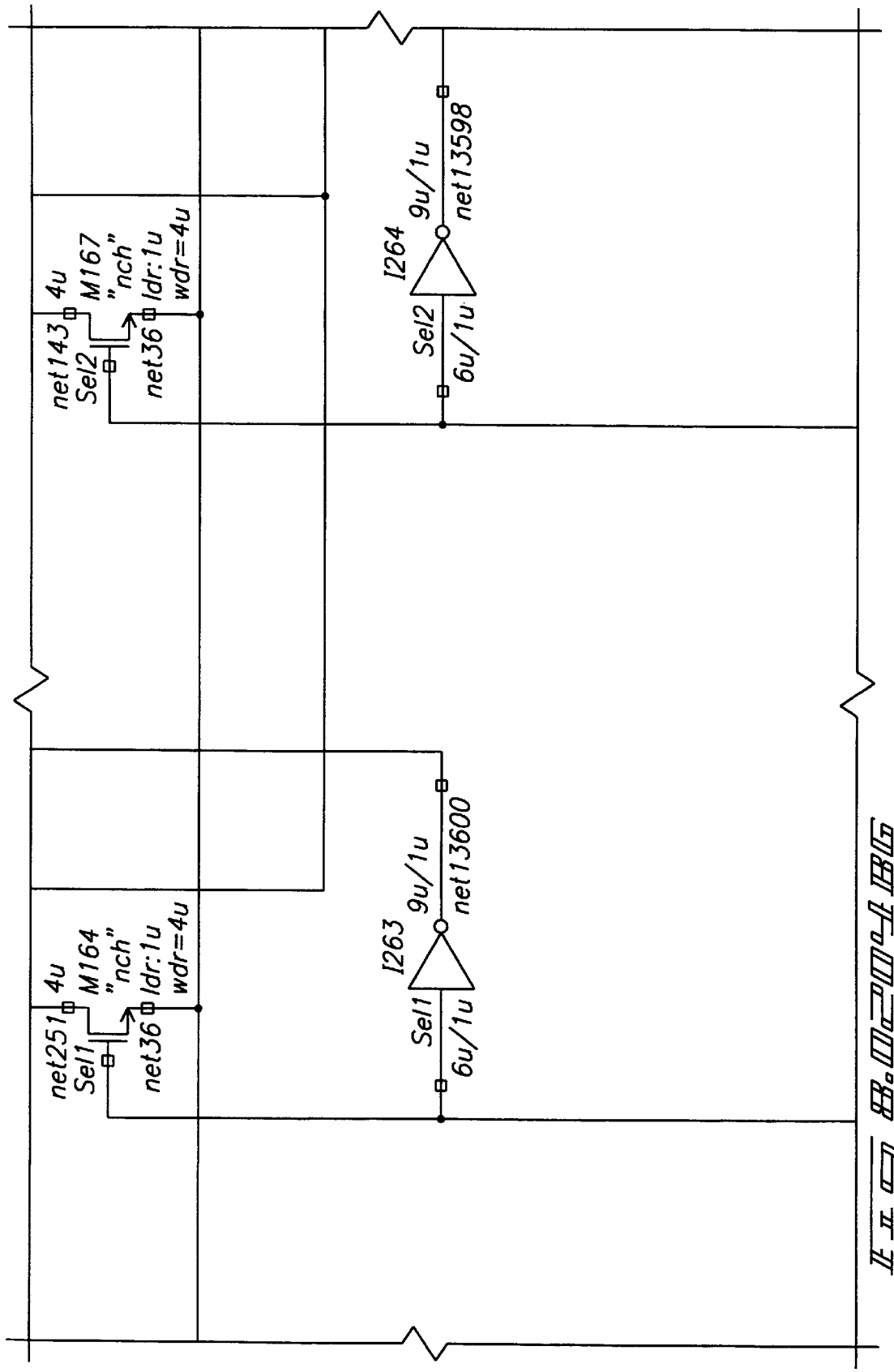

net143
Sel2
4u
M167
"nch"
ldr:1u
wdr=4u
net36
I264
9u/1u
net13598
Sel2
6u/1u
net251
Sel1
4u
M164
"nch"
ldr:1u
wdr=4u
net36
I263
9u/1u
net13600
Sel1
6u/1u

FIG 8,004,185

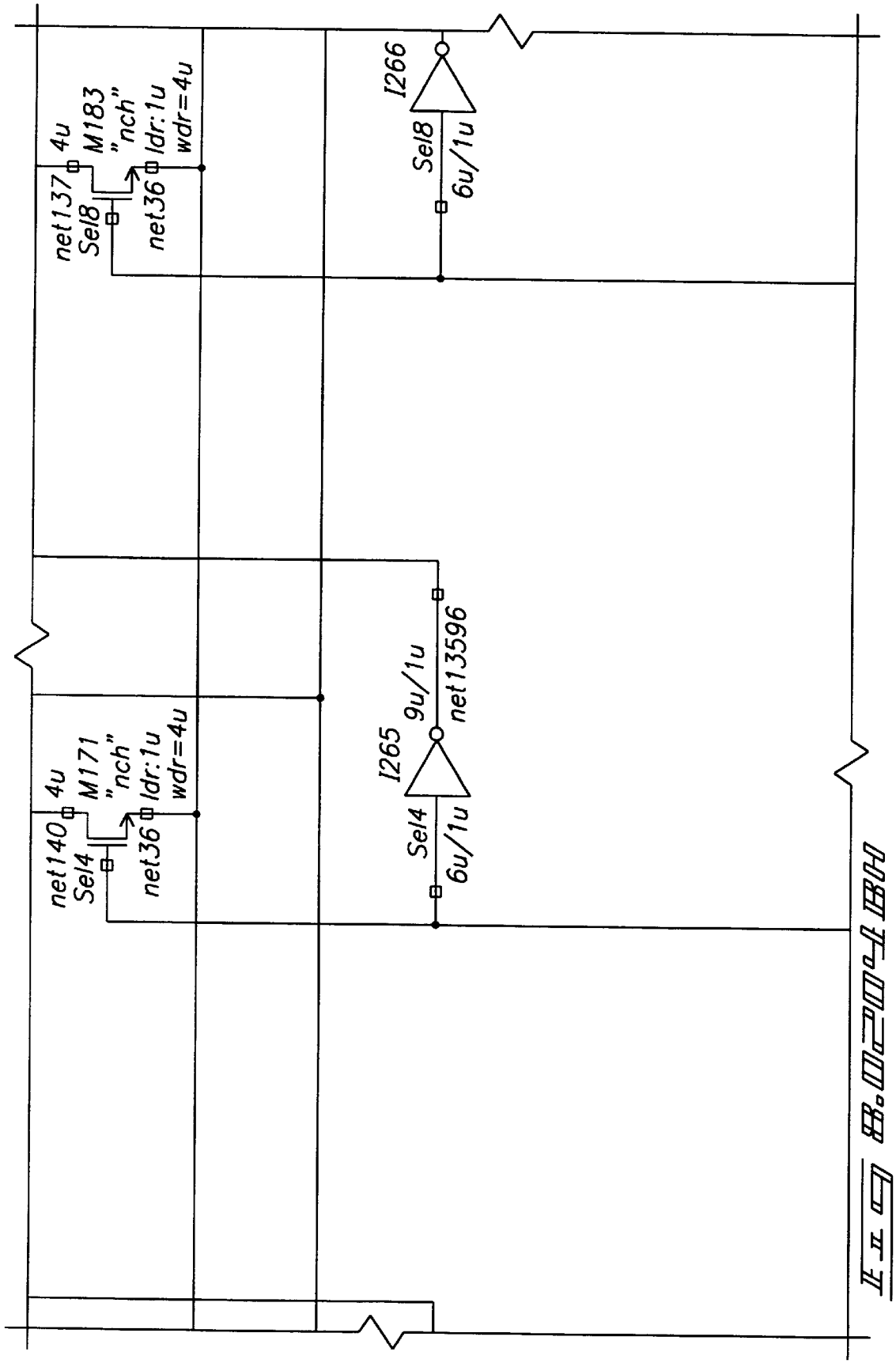

I266
Sel8
6u/1u
net137
Sel8
4u
M183
"nch"
ldr:1u
wdr=4u
net36
I265
9u/1u
net13596
Sel4
6u/1u
net140
Sel4
4u
M171
"nch"
ldr:1u
wdr=4u
net36

FIG. 8,002

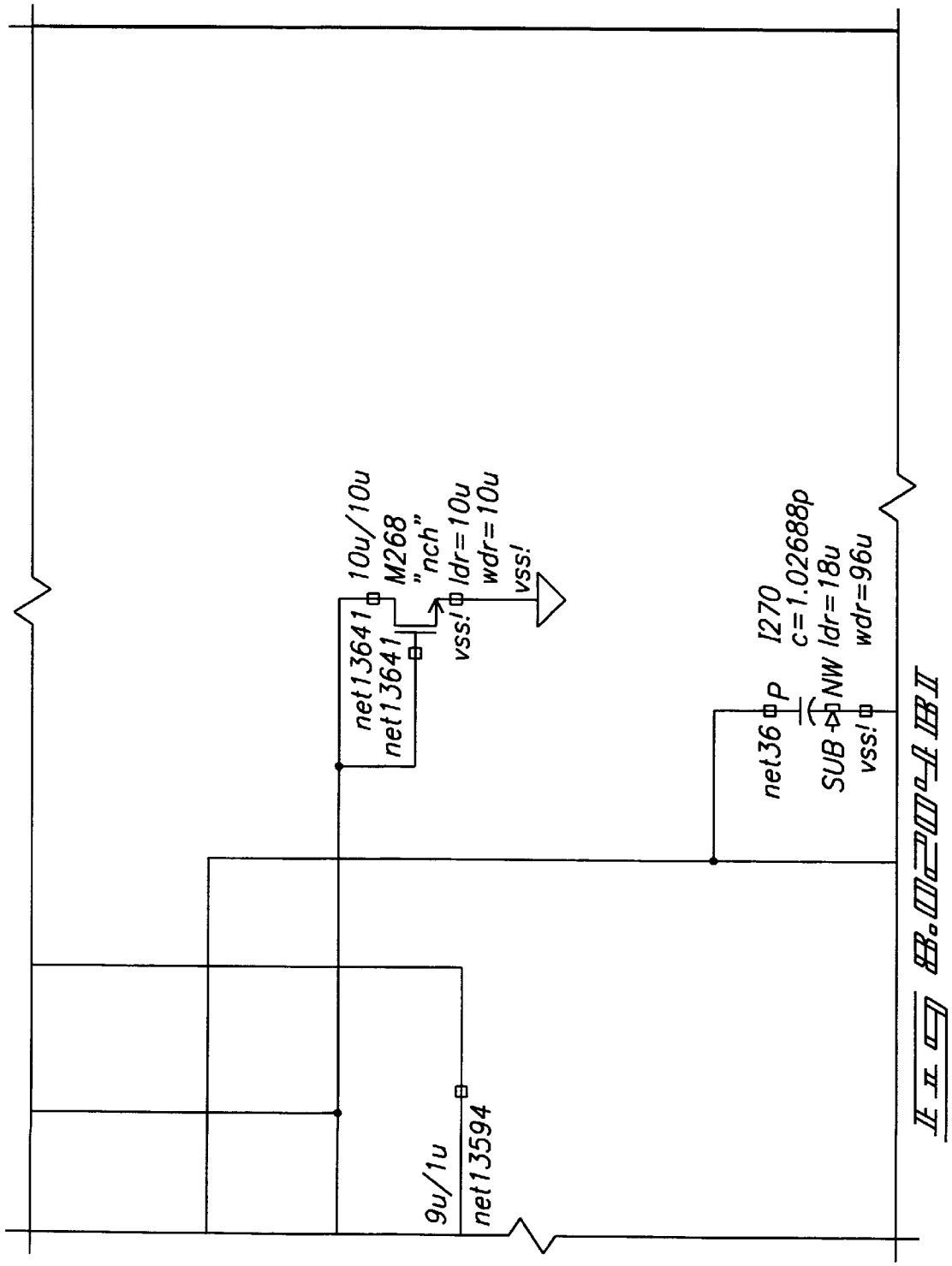
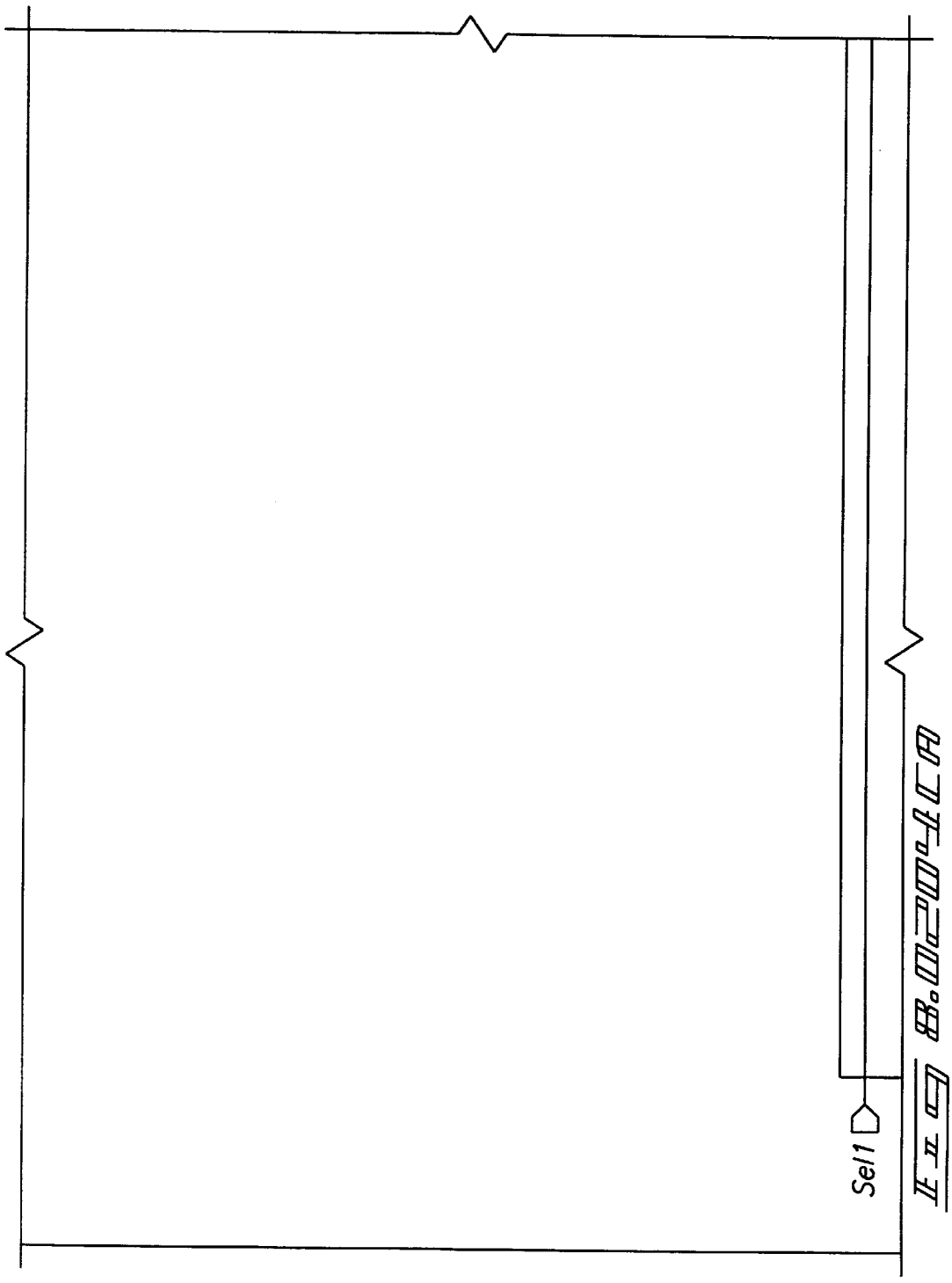
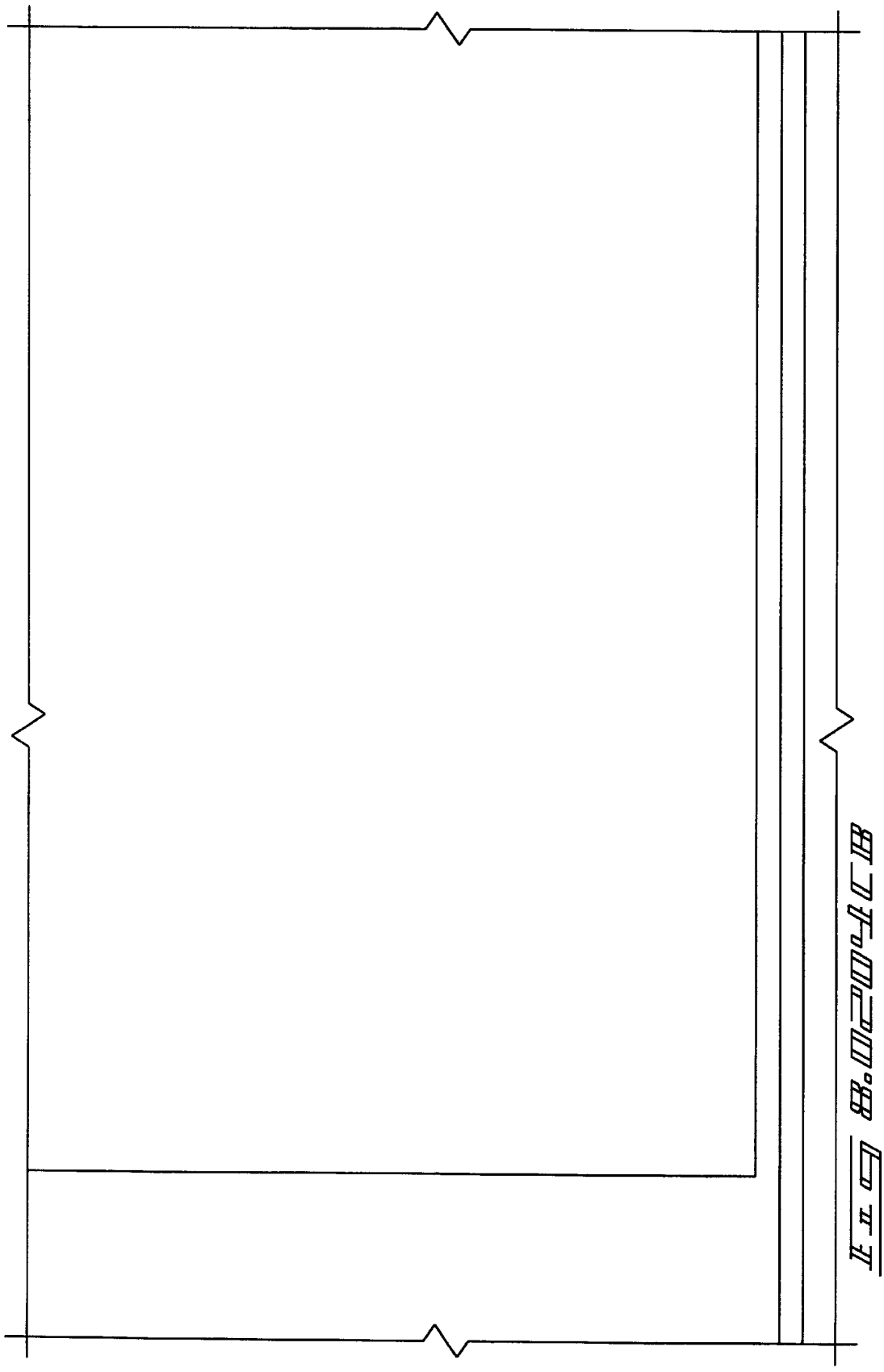


FIG. 8.00200 BII


Sel1
BUFFER



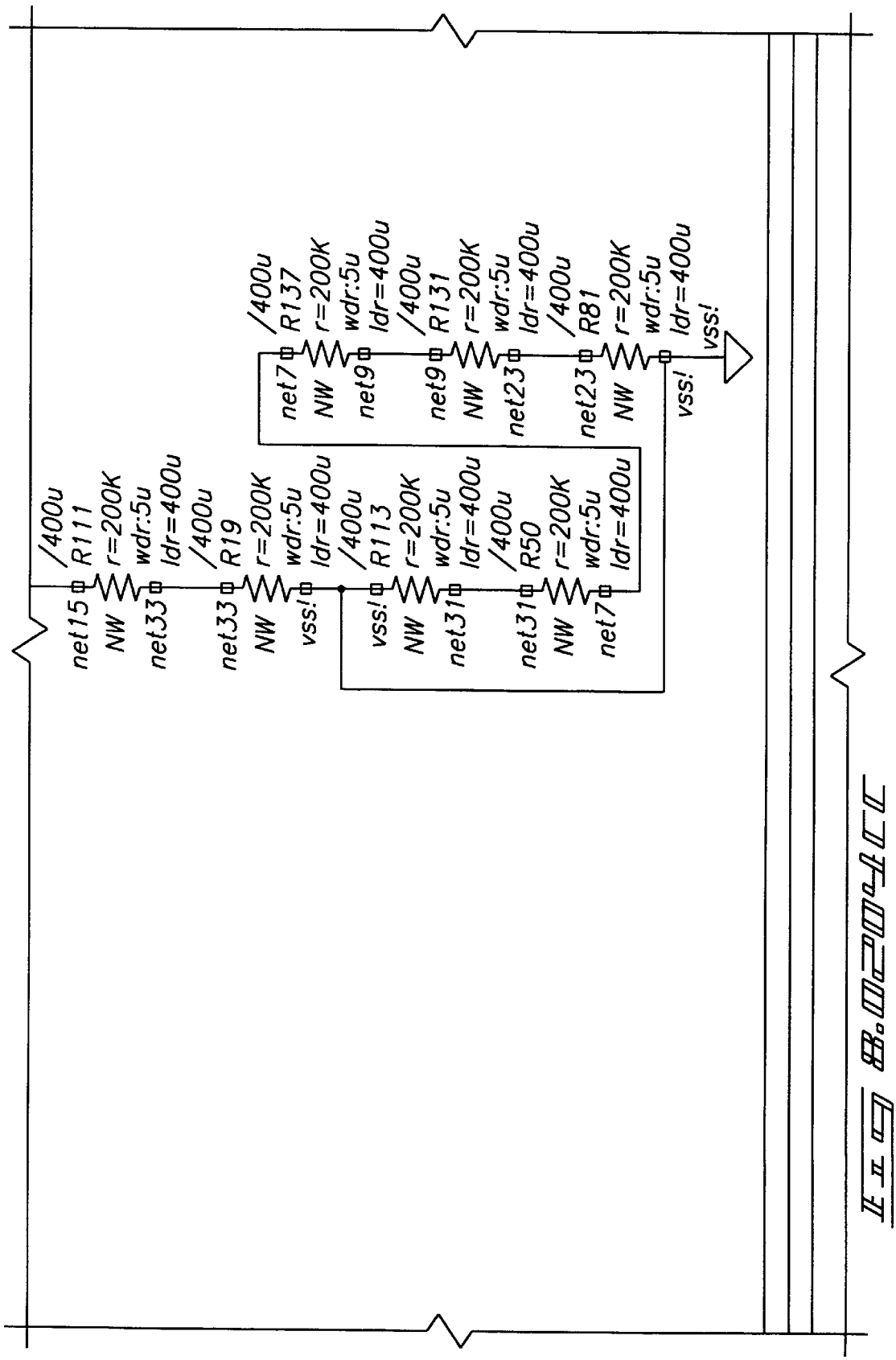
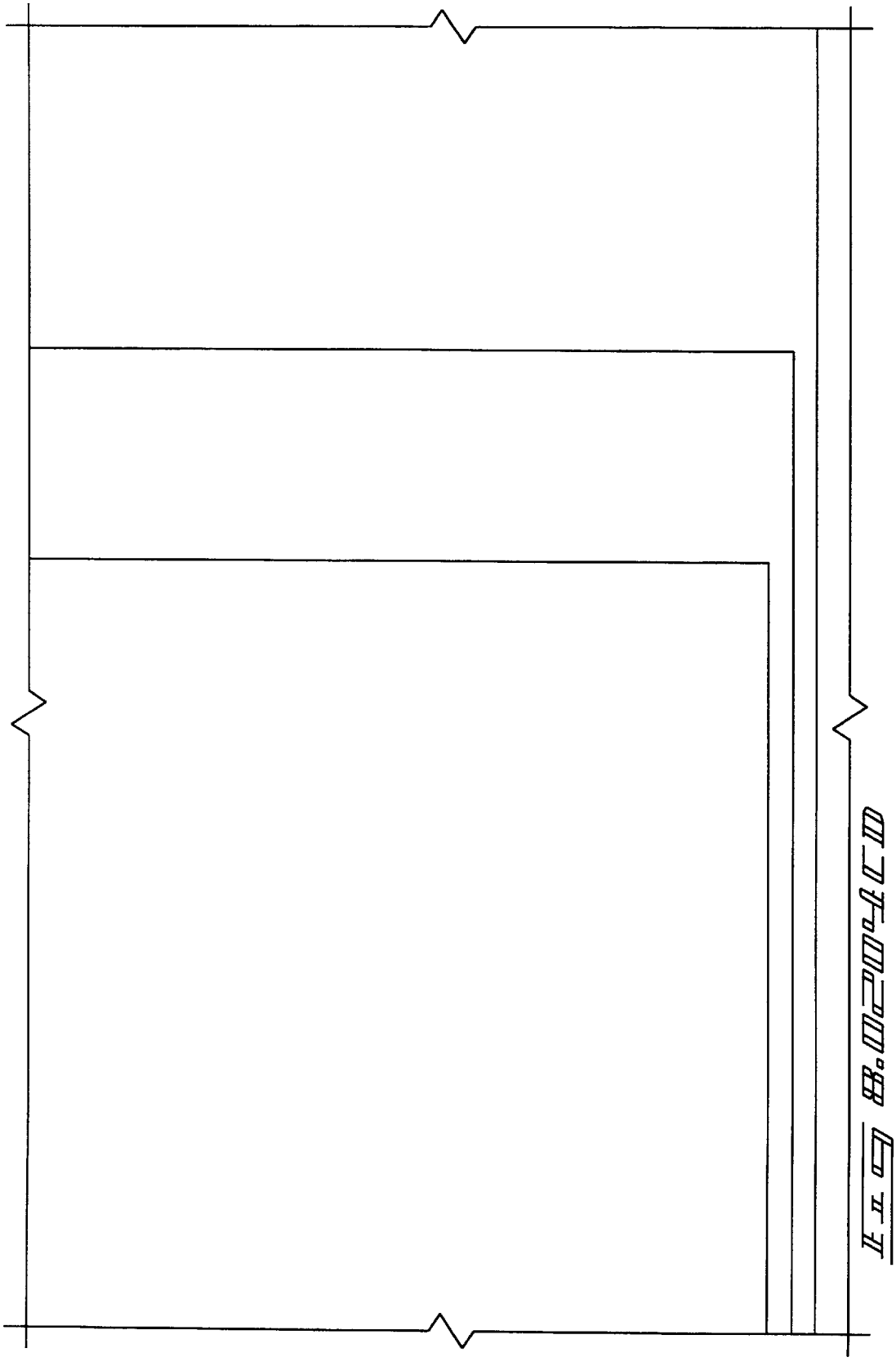
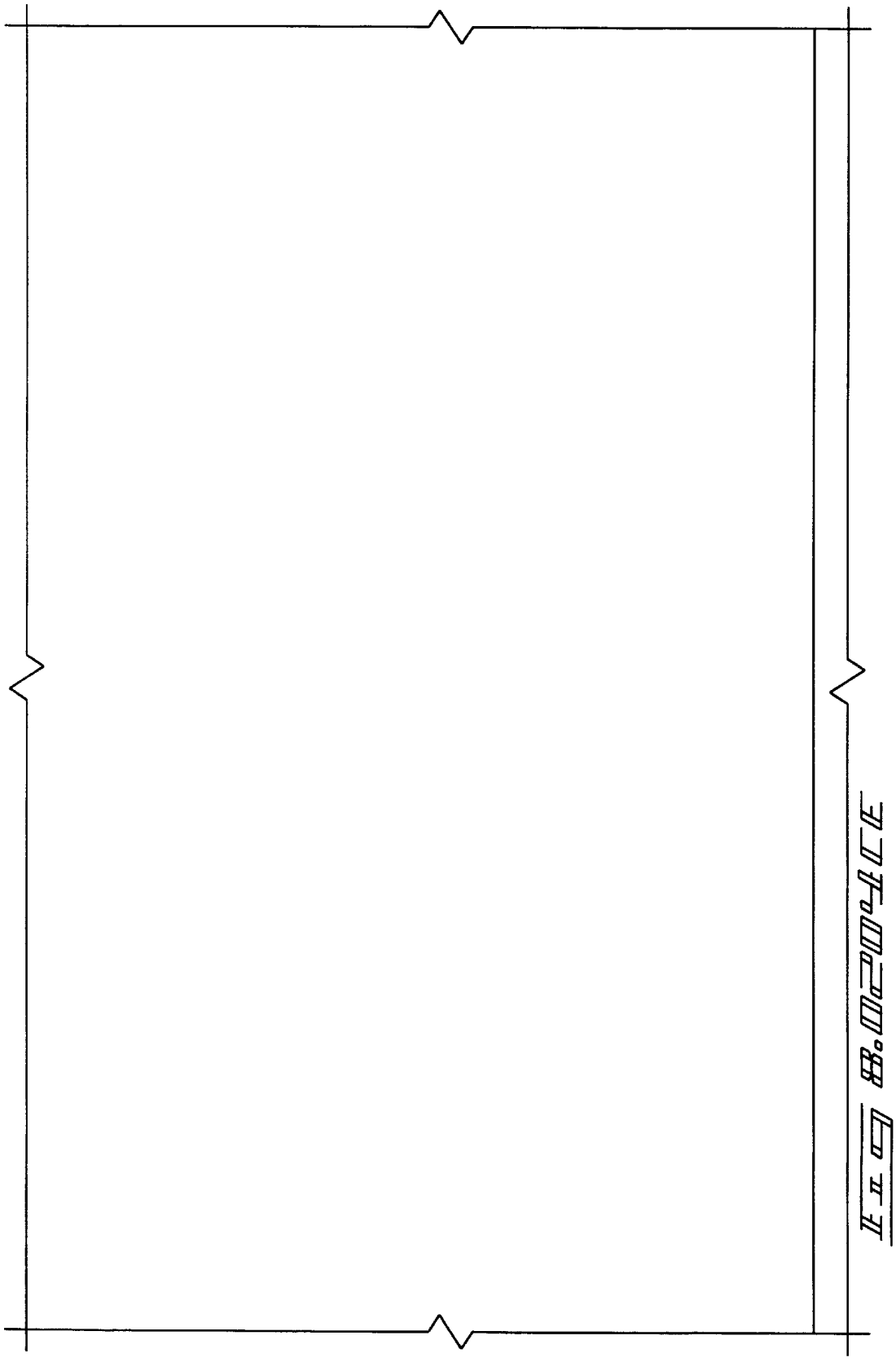


FIG 88,002,048





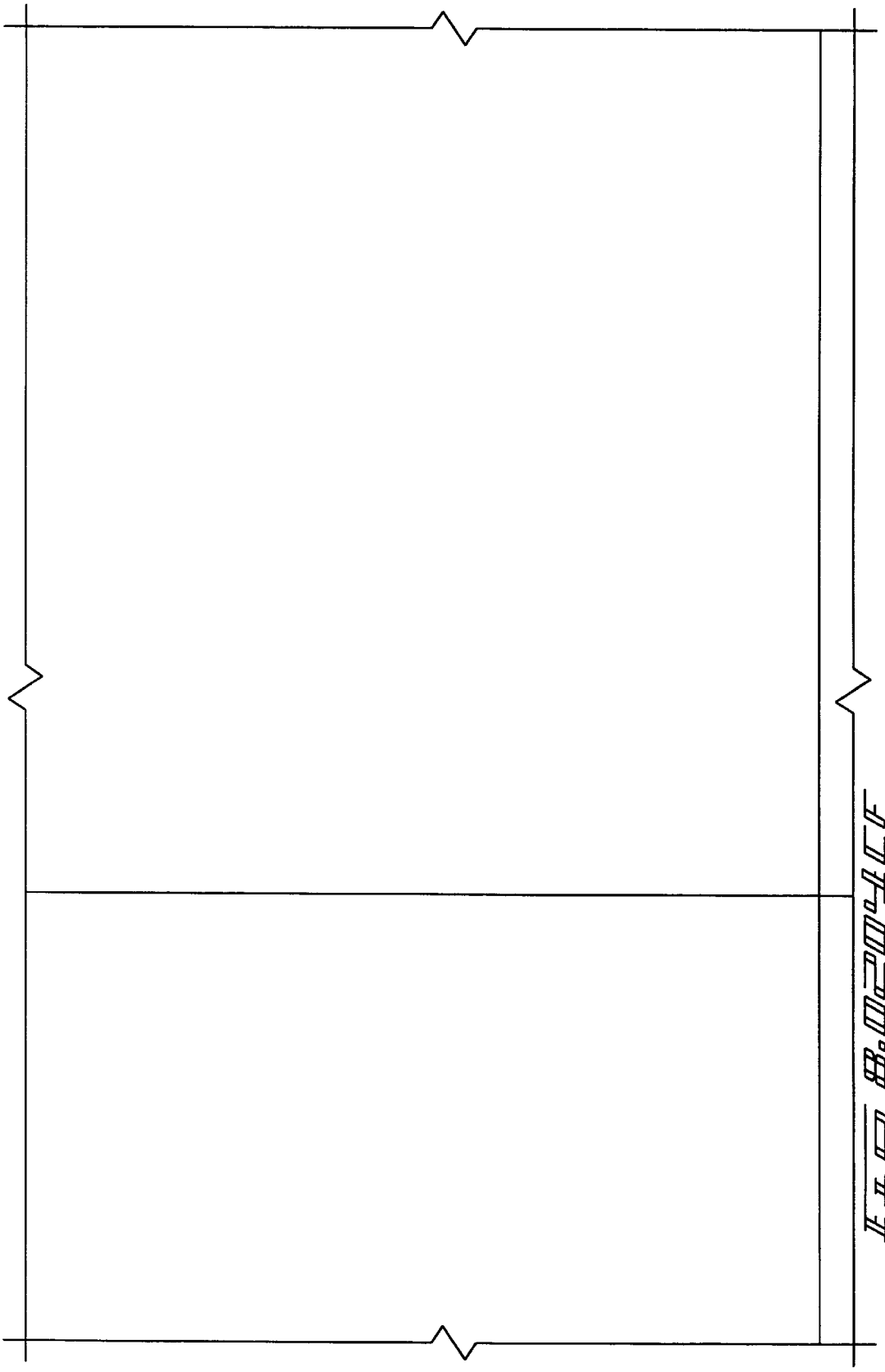
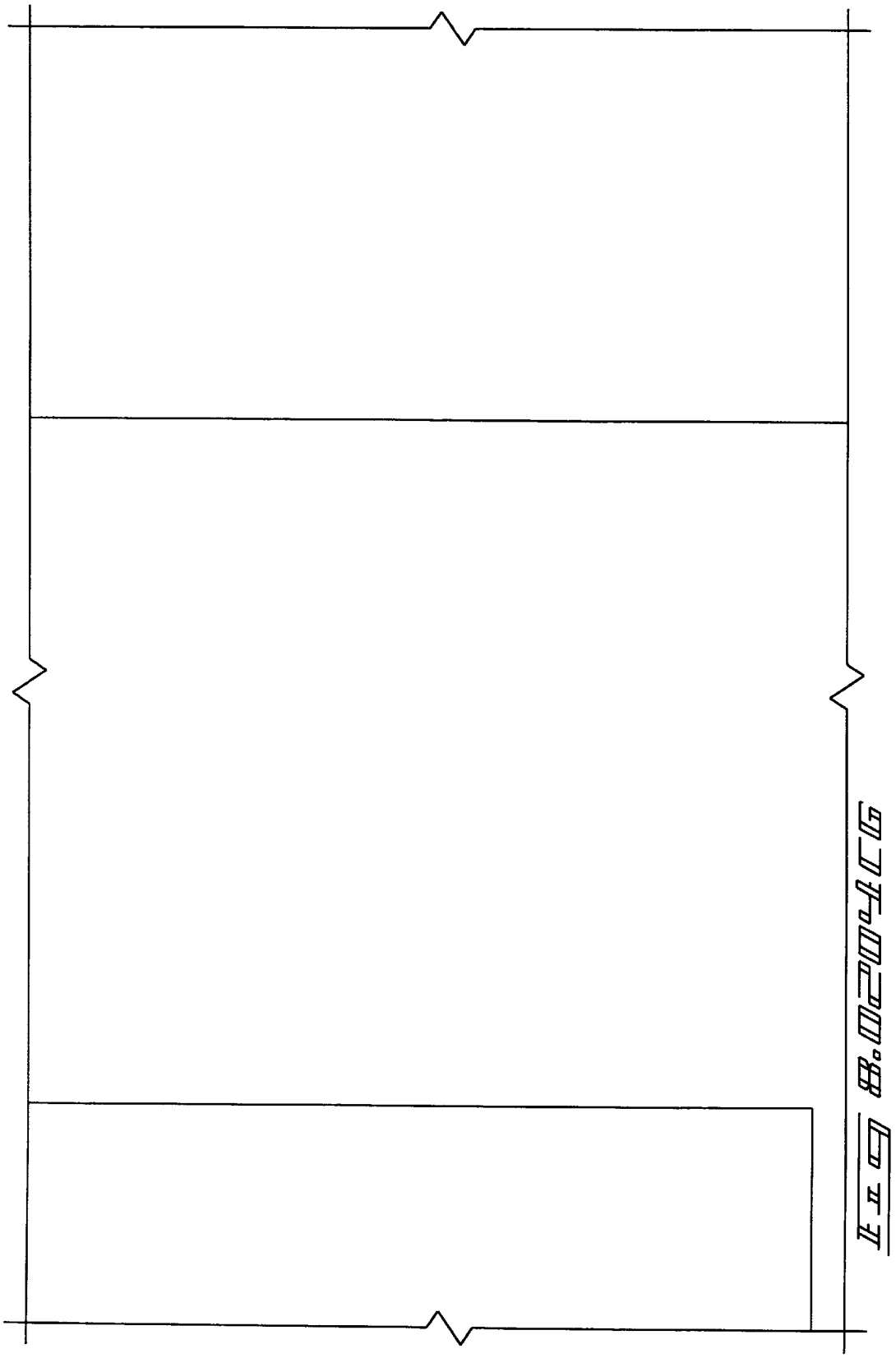


FIG 8,002F


SJ7400-98.00200

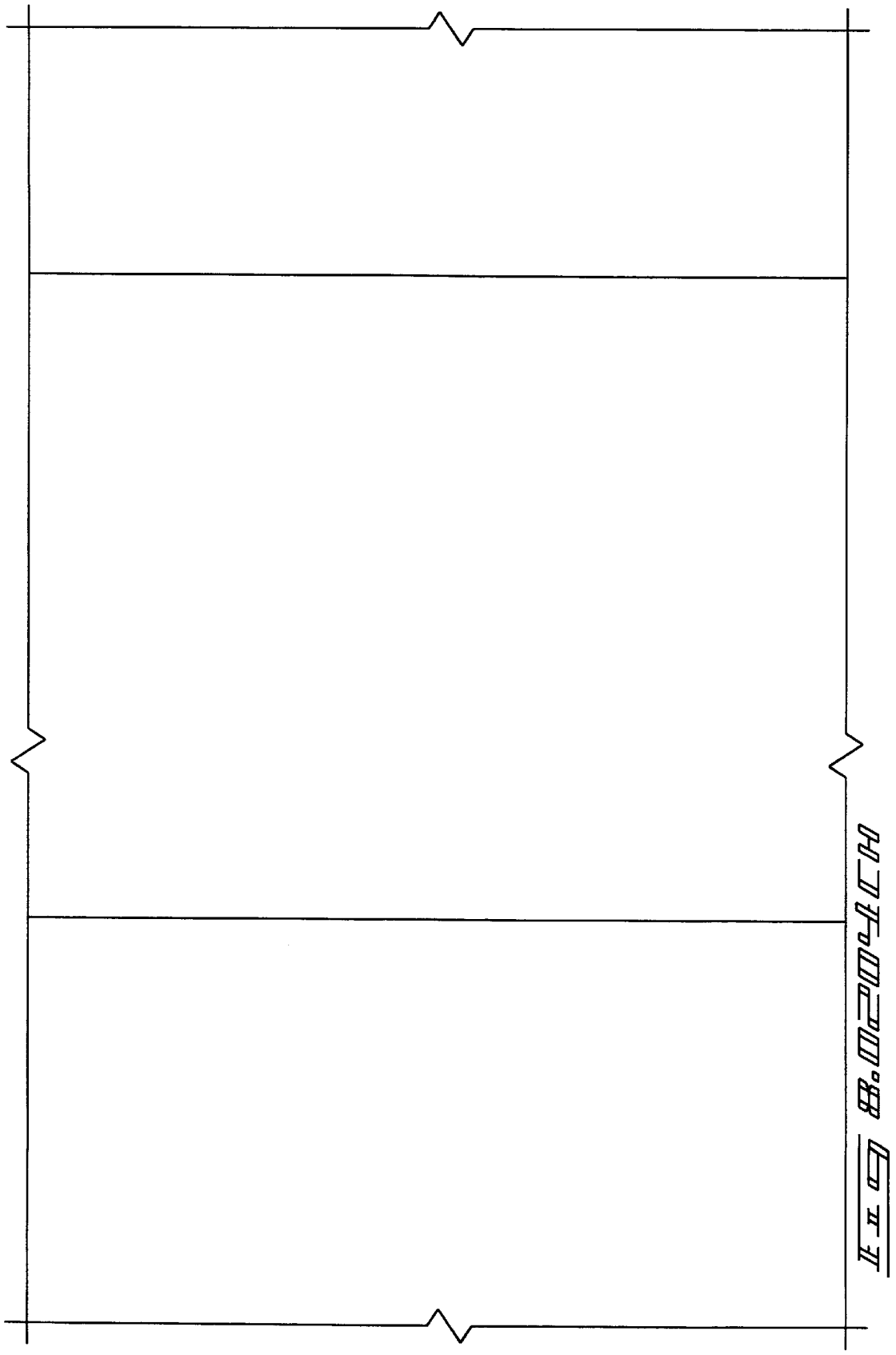
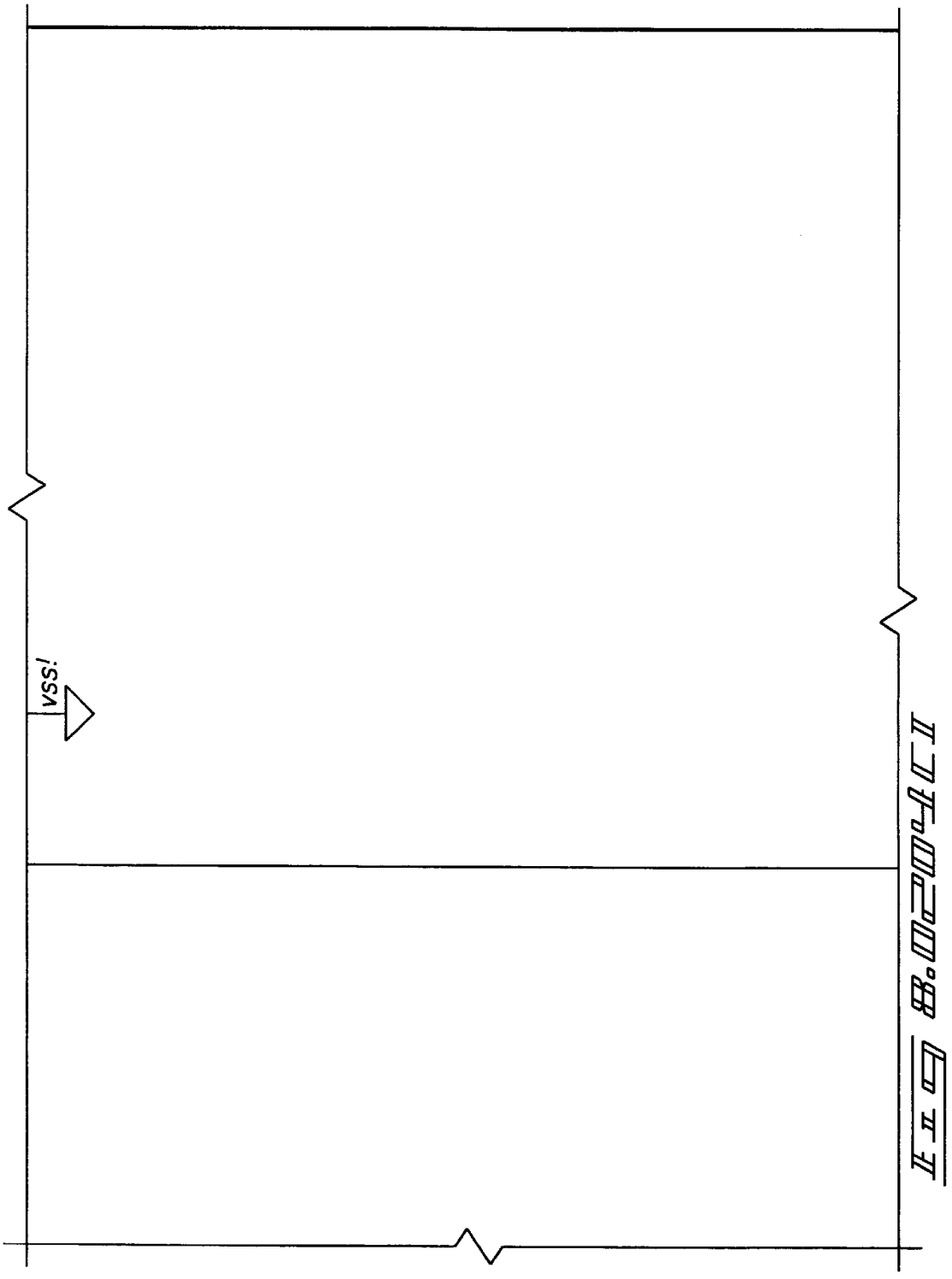


FIG 88.02H4


VSS!
FIG. 8,020,711

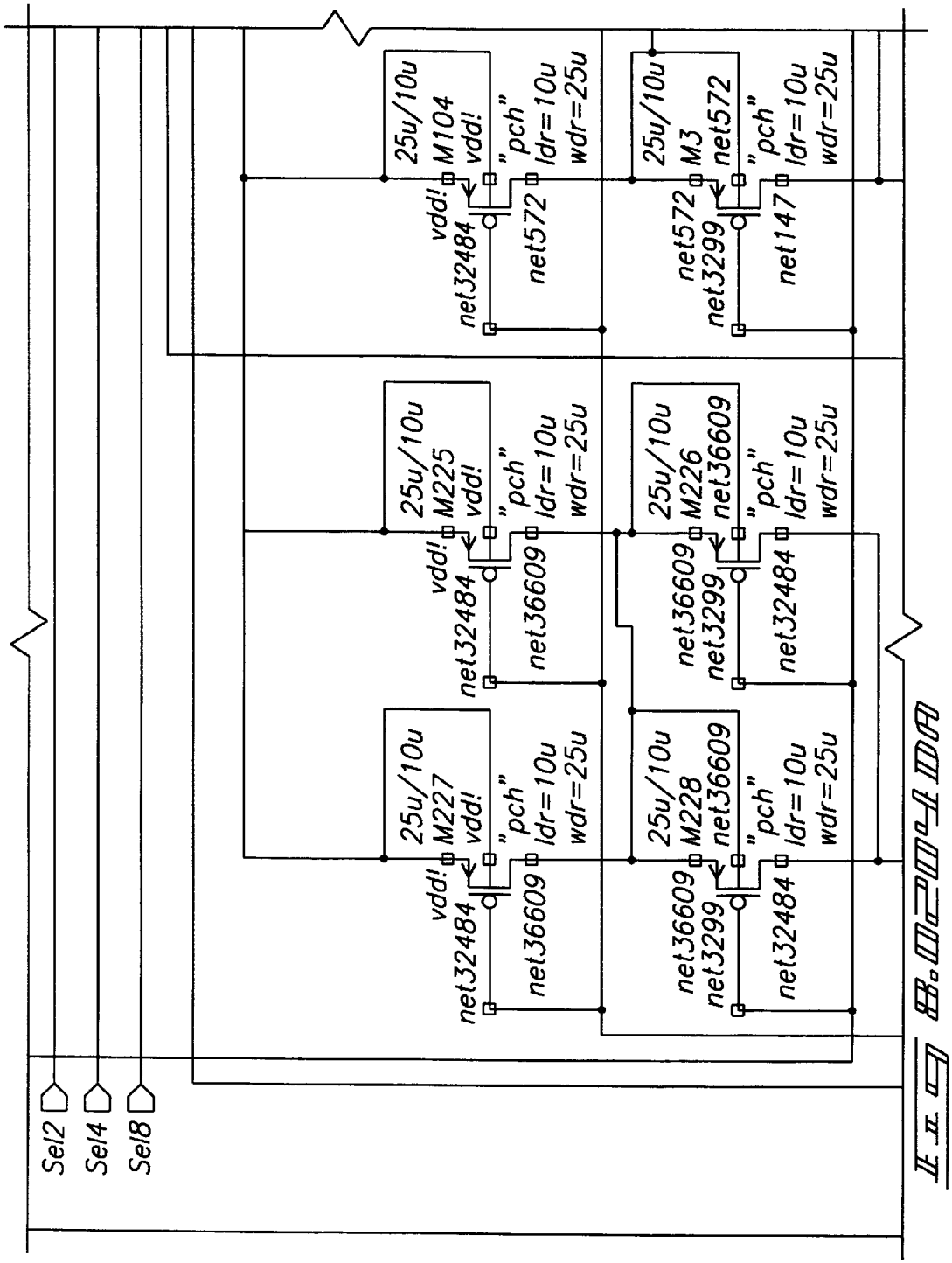
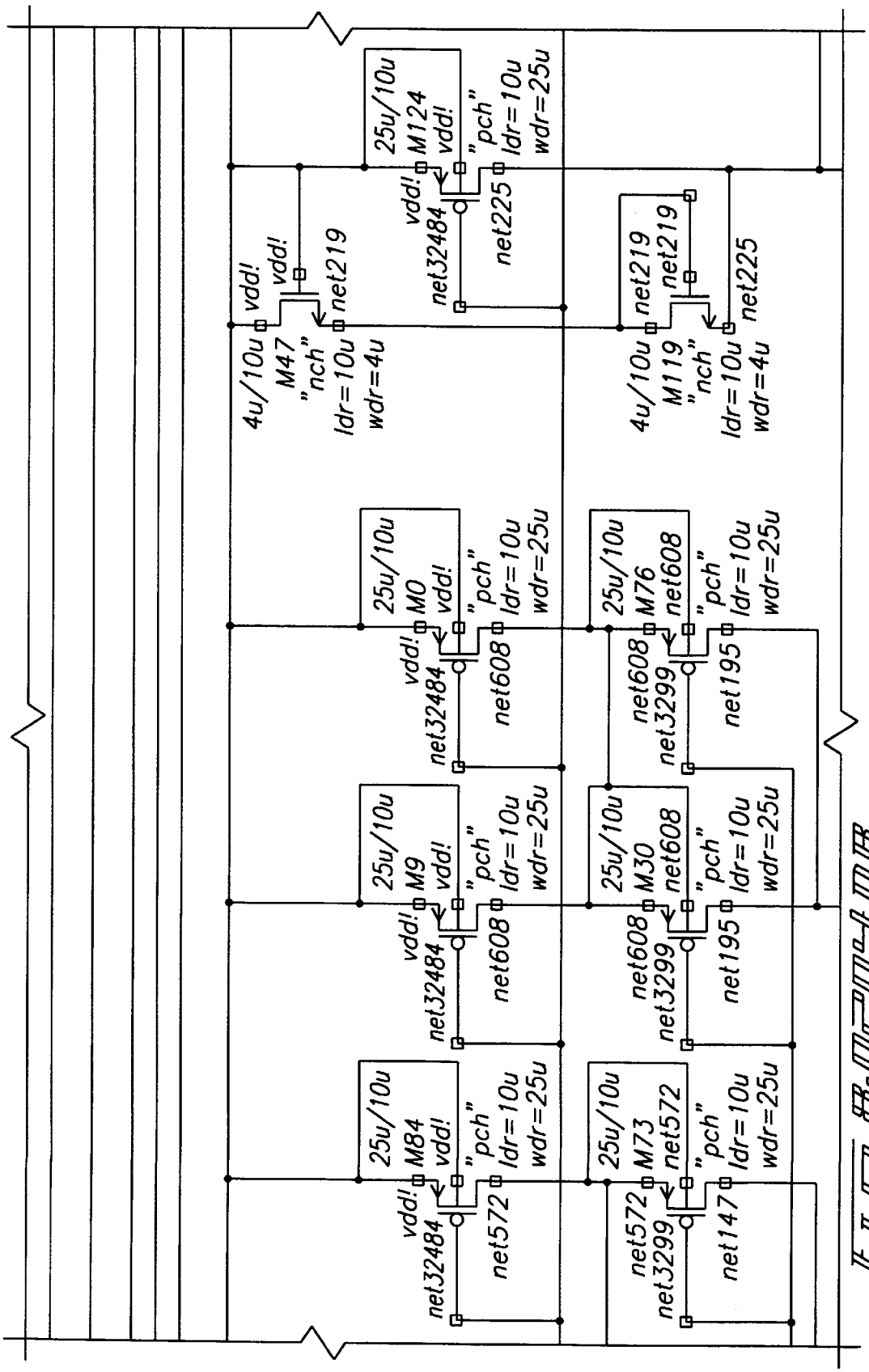


FIG. 8.0C2004A1DA


25u/10u M124 vdd! "pch" ldr=10u wdr=25u
vdd! net32484 net225
4u/10u M47 "nch" ldr=10u wdr=4u
vdd! vdd! net219
4u/10u M119 "nch" ldr=10u wdr=4u
net219 net219 net225
25u/10u M0 vdd! "pch" ldr=10u wdr=25u
vdd! net32484 net608
25u/10u M76 net608 "pch" ldr=10u wdr=25u
net608 net3299 net195
25u/10u M9 vdd! "pch" ldr=10u wdr=25u
vdd! net32484 net608
25u/10u M30 net608 "pch" ldr=10u wdr=25u
net608 net3299 net195
25u/10u M84 vdd! "pch" ldr=10u wdr=25u
vdd! net32484 net572
25u/10u M73 net572 "pch" ldr=10u wdr=25u
net572 net3299 net147

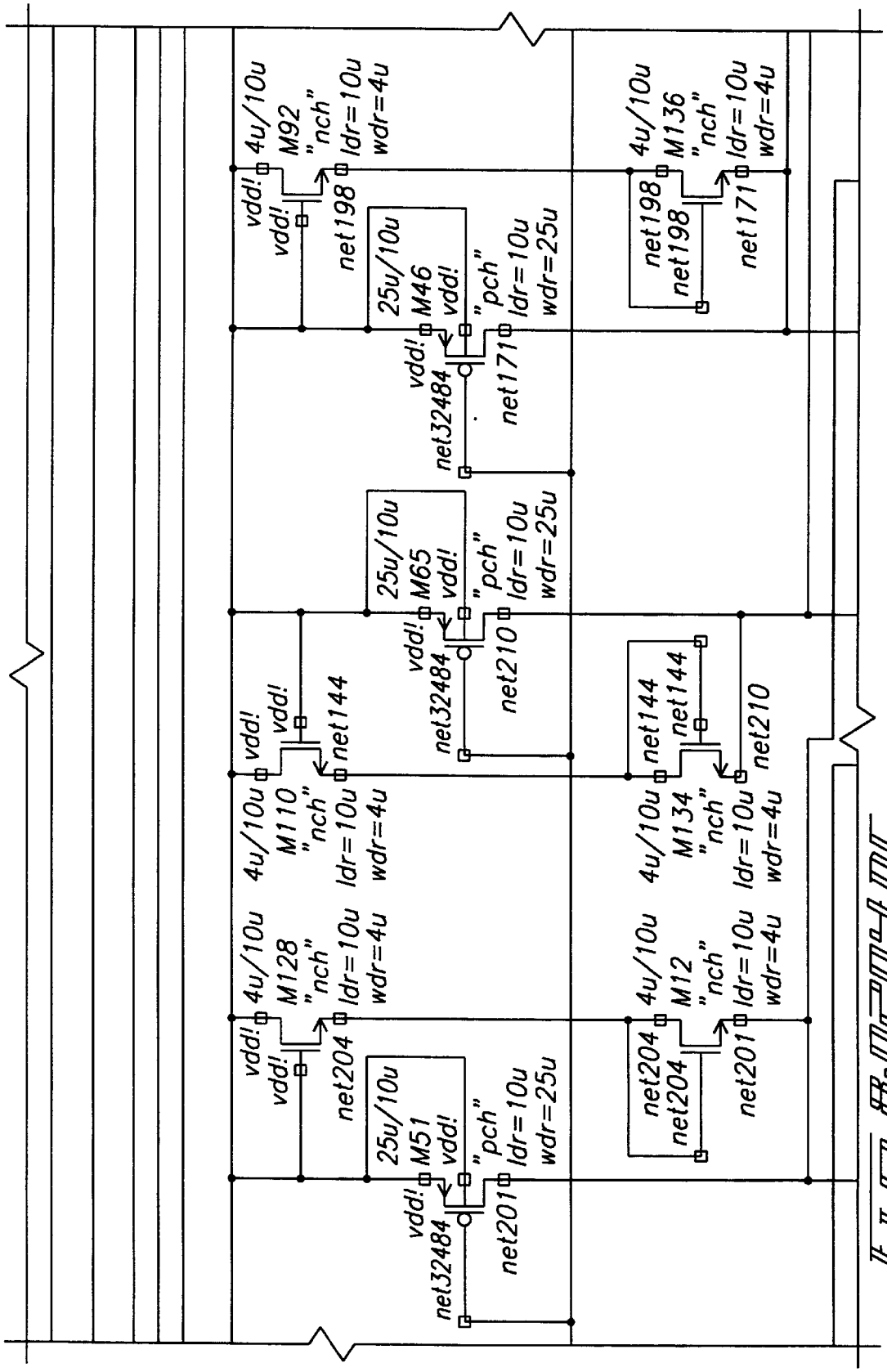
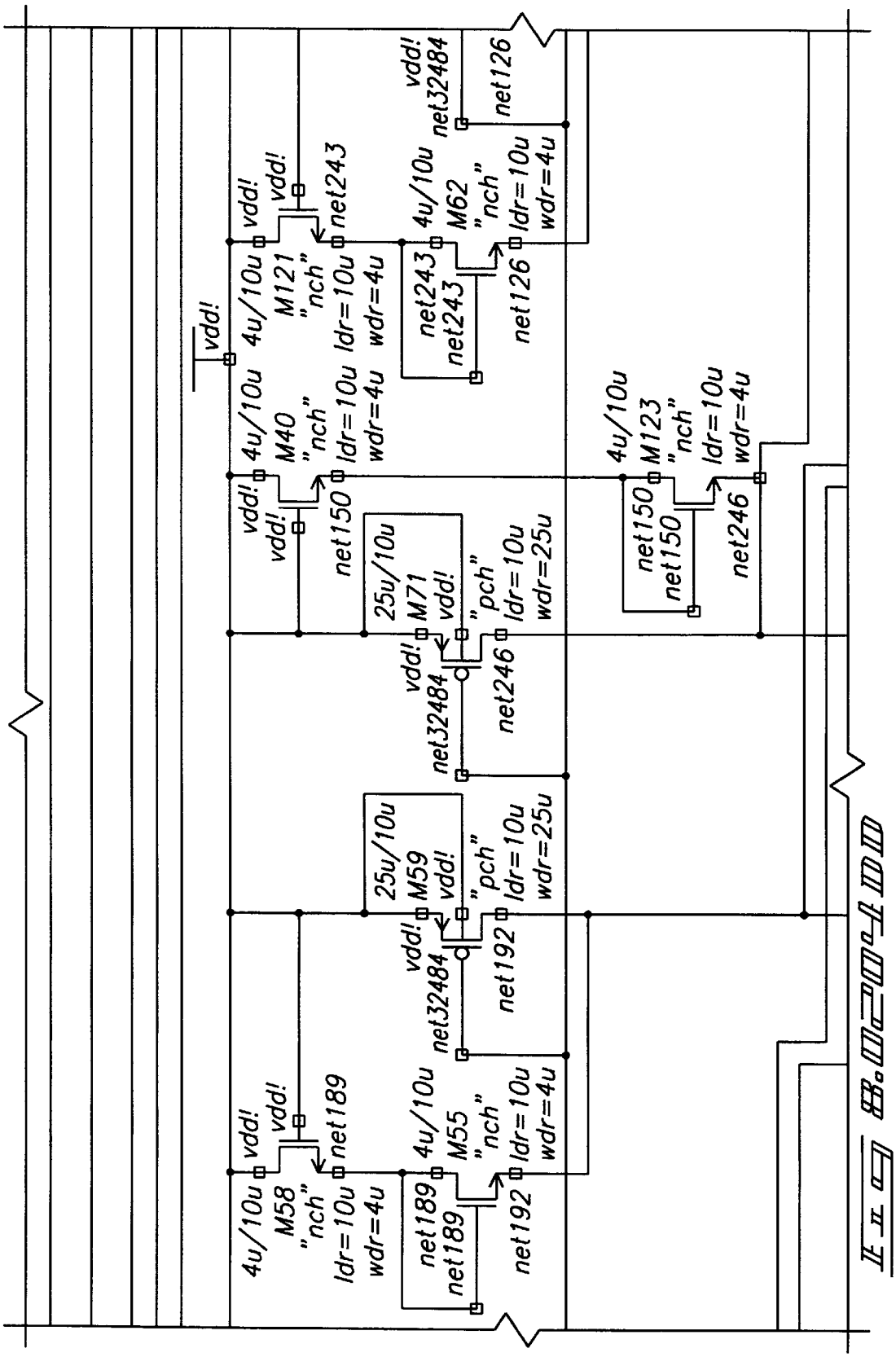

4u/10u M92 "nch" ldr=10u wdr=4u
vdd! vdd! net198
25u/10u M46 vdd! "pch" ldr=10u wdr=25u
vdd! net32484 net171
4u/10u M136 "nch" ldr=10u wdr=4u
net198 net198 net171
25u/10u M65 vdd! "pch" ldr=10u wdr=25u
vdd! net32484 net210
4u/10u M110 "nch" ldr=10u wdr=4u
vdd! vdd! net144
4u/10u M134 "nch" ldr=10u wdr=4u
net144 net144 net210
4u/10u M128 "nch" ldr=10u wdr=4u
vdd! vdd! net204
25u/10u M51 vdd! "pch" ldr=10u wdr=25u
vdd! net32484 net201
4u/10u M12 "nch" ldr=10u wdr=4u
net204 net204 net201

FIG. 1368


vdd!
4u/10u
M58
"nch"
ldr=10u
wdr=4u
net189
net189
net189
4u/10u
M55
"nch"
ldr=10u
wdr=4u
net192
net192
25u/10u
M59
vdd!
"pch"
ldr=10u
wdr=25u
net32484
vdd!
net246
25u/10u
M71
vdd!
"pch"
ldr=10u
wdr=25u
net32484
vdd!
net150
4u/10u
M40
"nch"
ldr=10u
wdr=4u
net150
net150
4u/10u
M123
"nch"
ldr=10u
wdr=4u
net246
4u/10u
M121
"nch"
ldr=10u
wdr=4u
net243
net243
net243
4u/10u
M62
"nch"
ldr=10u
wdr=4u
net126
net126
net32484
vdd!

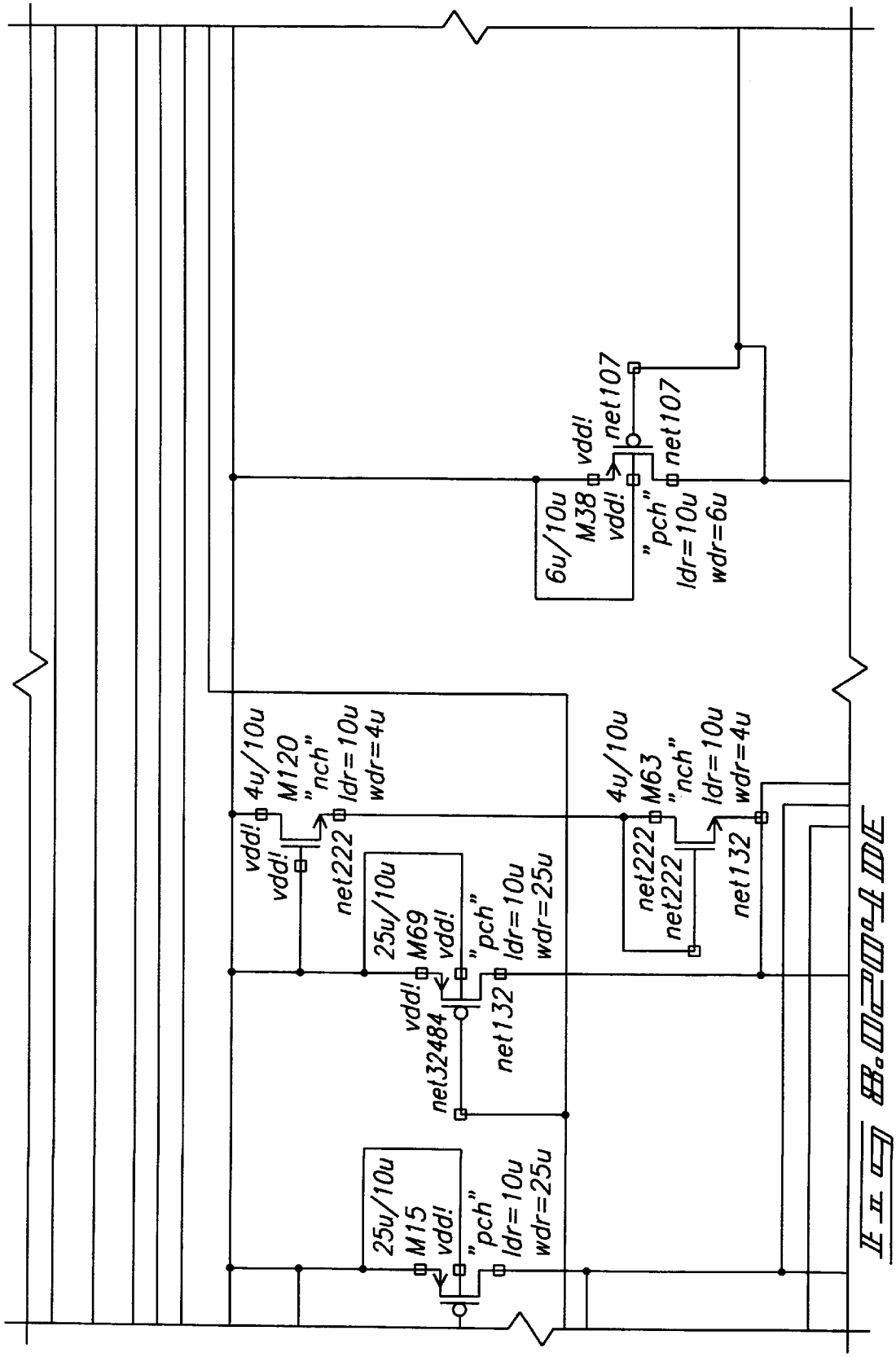
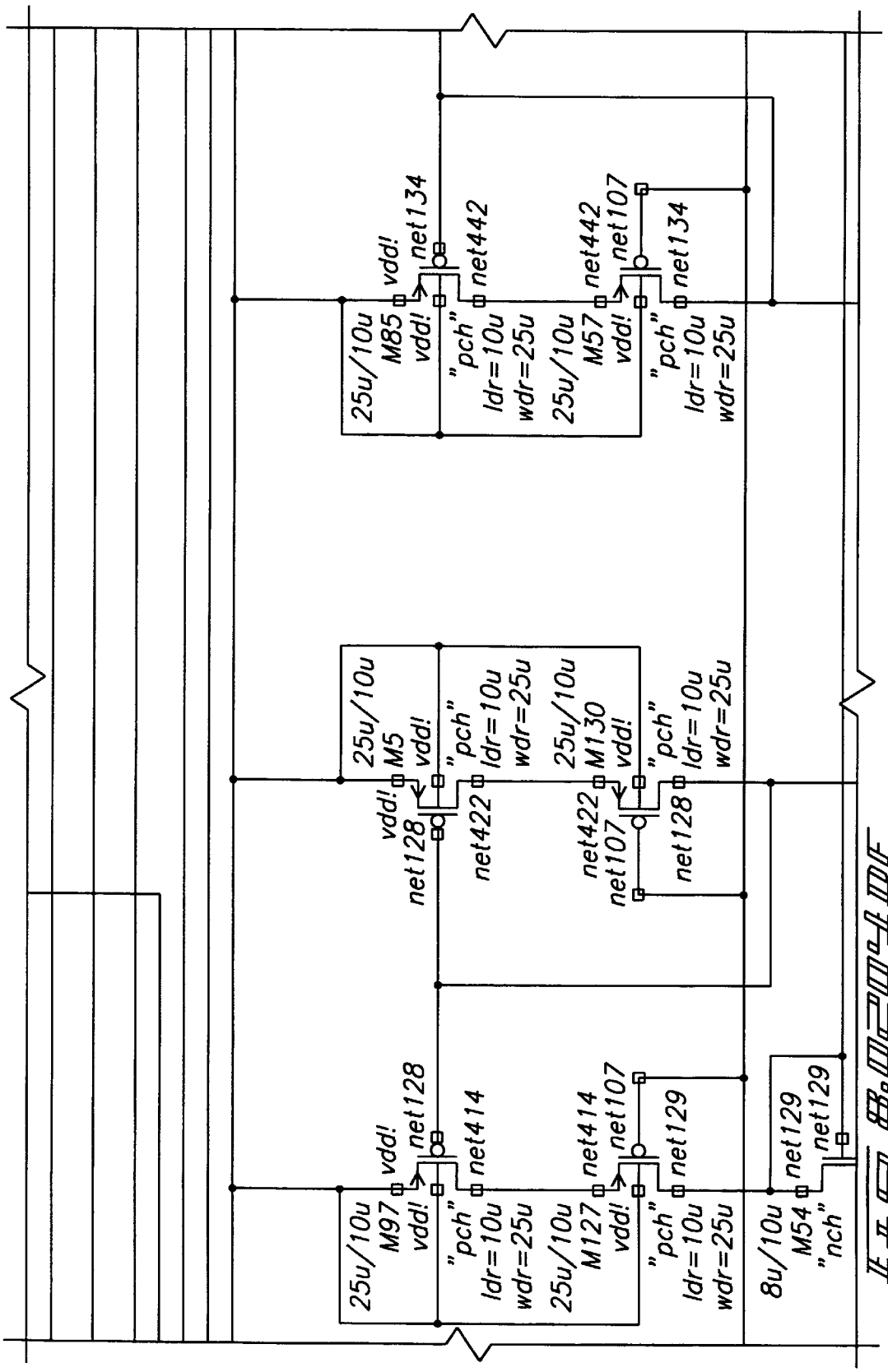

6u/10u
M38
vdd!
"pch"
ldr=10u
wdr=6u
net107
4u/10u
M120
"nch"
ldr=10u
wdr=4u
net222
25u/10u
M69
"pch"
ldr=10u
wdr=25u
net32484
net132
4u/10u
M63
"nch"
ldr=10u
wdr=4u
25u/10u
M15
"pch"
ldr=10u
wdr=25u

FIG 8.00274E


25u/10u
M85
"pch"
ldr=10u
wdr=25u
25u/10u
M57
"pch"
ldr=10u
wdr=25u
25u/10u
M5
"pch"
ldr=10u
wdr=25u
25u/10u
M130
"pch"
ldr=10u
wdr=25u
25u/10u
M97
"pch"
ldr=10u
wdr=25u
25u/10u
M127
"pch"
ldr=10u
wdr=25u
8u/10u
M54
"nch"
vdd!
net134
net442
net107
net128
net422
net414
net129

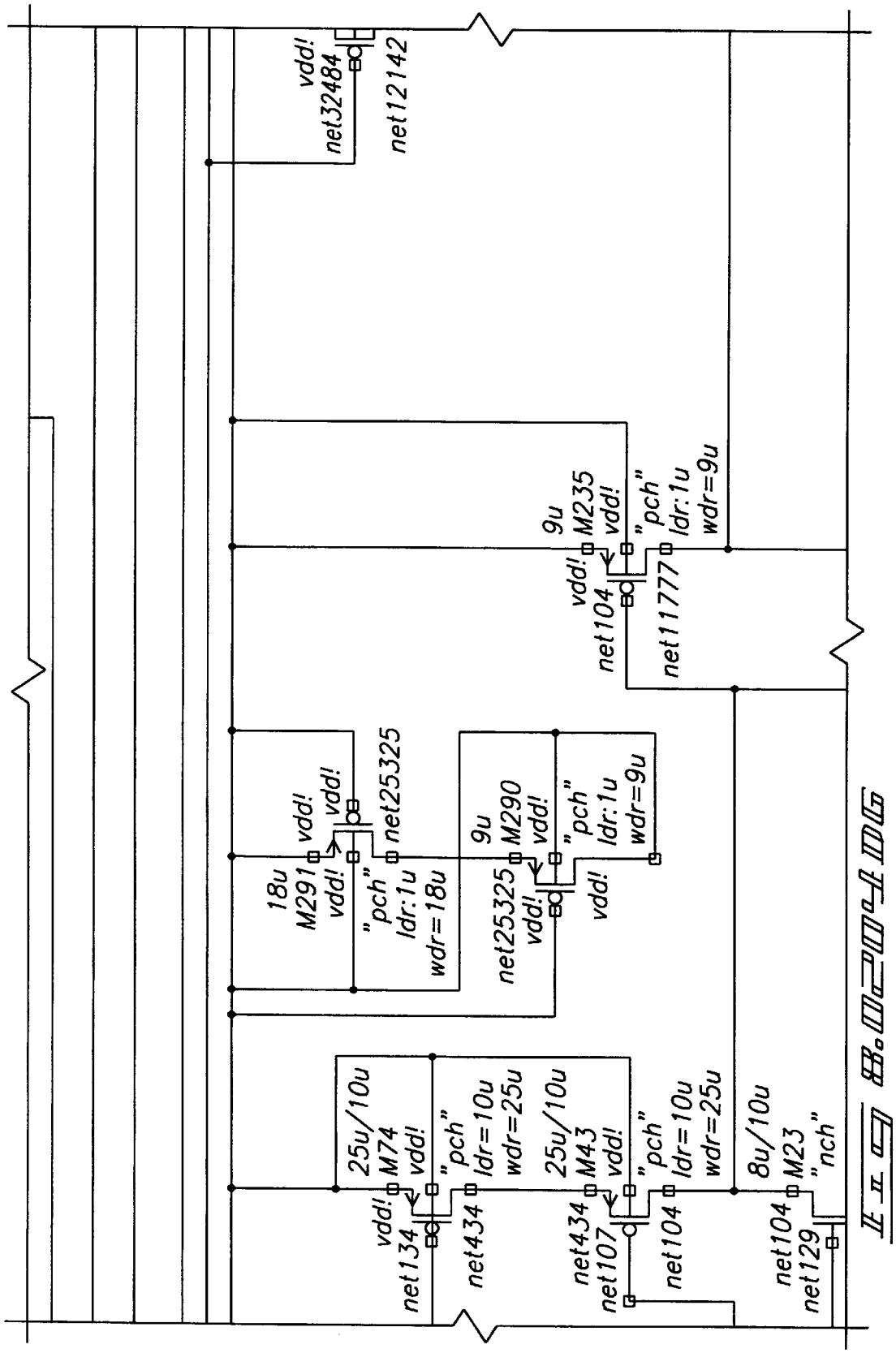

vdd!
net32484
net12142
9u
M235
vdd!
"pch"
ldr:1u
wdr=9u
vdd!
net104
net11777
18u
M291
vdd!
vdd!
"pch"
ldr:1u
wdr=18u
net25325
9u
M290
vdd!
"pch"
ldr:1u
wdr=9u
net25325
vdd!
vdd!
25u/10u
M74
vdd!
"pch"
ldr=10u
wdr=25u
vdd!
net134
net434
25u/10u
M43
vdd!
"pch"
ldr=10u
wdr=25u
net434
net107
net104
8u/10u
M23
"nch"
net104
net129

FIG. 8.0072

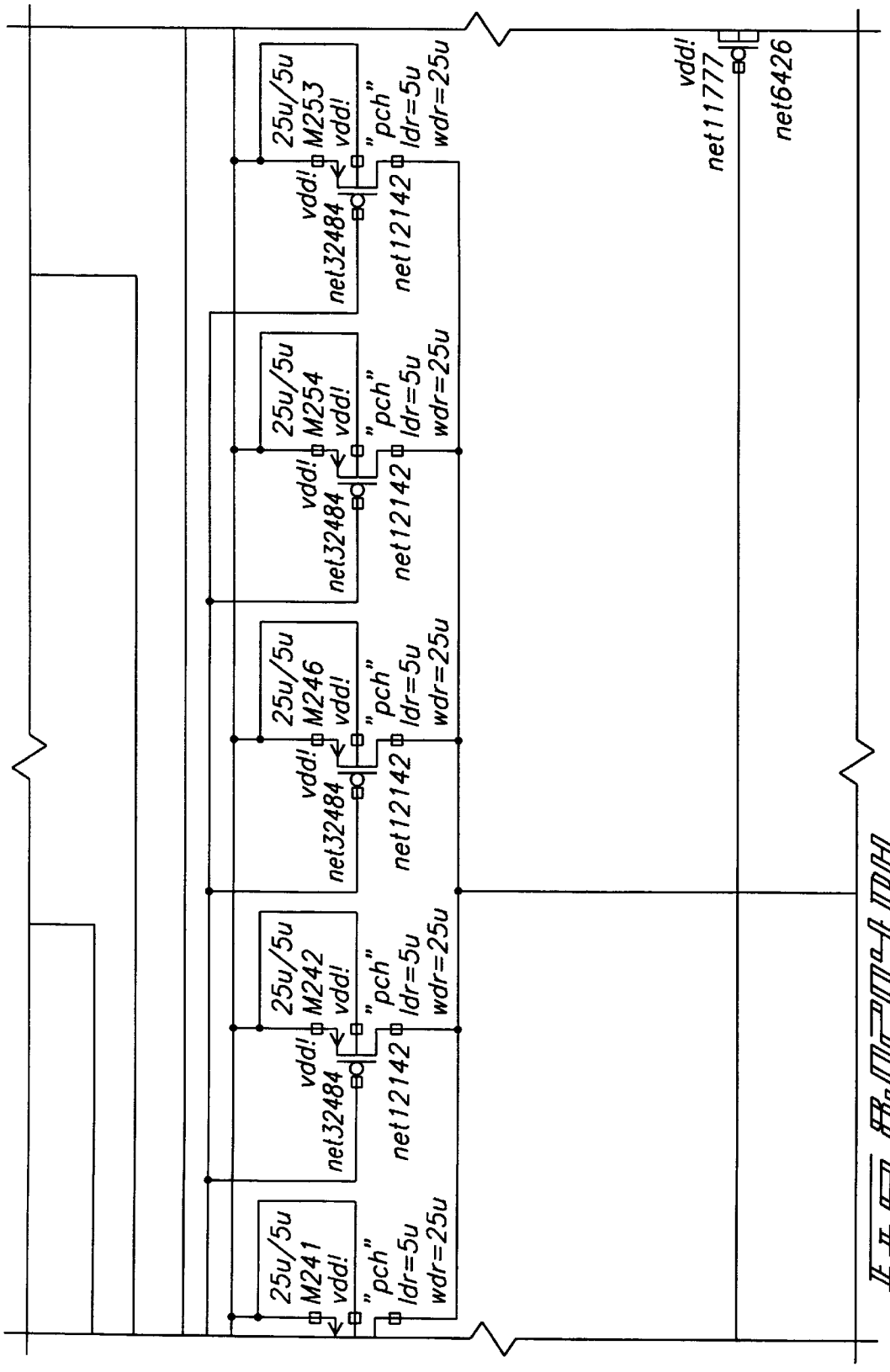

25u/5u
M241
vdd!
"pch"
ldr=5u
wdr=25u
25u/5u
M242
vdd!
"pch"
ldr=5u
wdr=25u
25u/5u
M246
vdd!
"pch"
ldr=5u
wdr=25u
25u/5u
M254
vdd!
"pch"
ldr=5u
wdr=25u
25u/5u
M253
vdd!
"pch"
ldr=5u
wdr=25u
net32484
net12142
vdd!
net11777
net6426

FIG 8,004,602

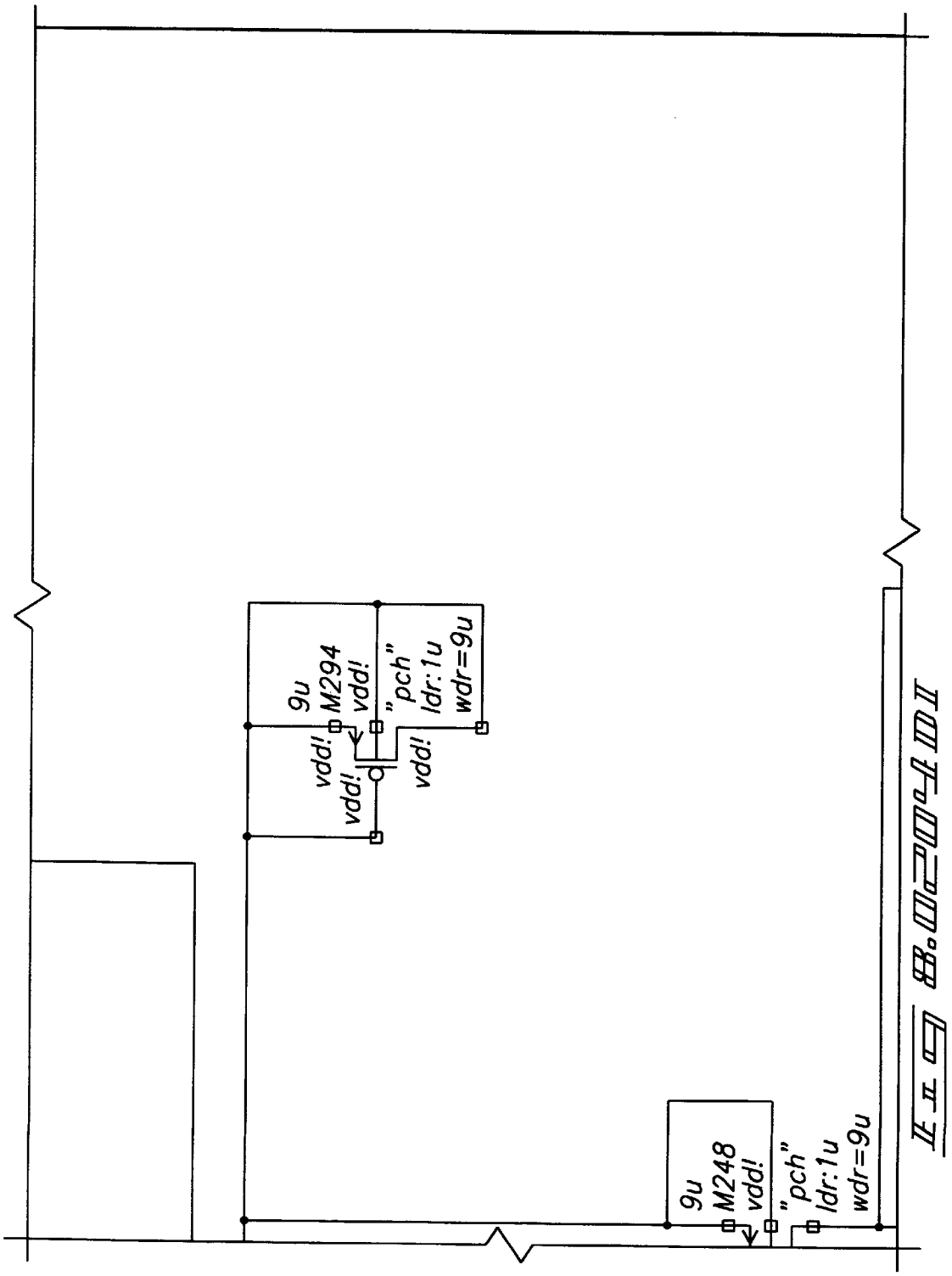

9u
M294
vdd!
"pch"
ldr:1u
wdr=9u
vdd!
vdd!
vdd!
9u
M248
vdd!
"pch"
ldr:1u
wdr=9u

FIG 88.00211

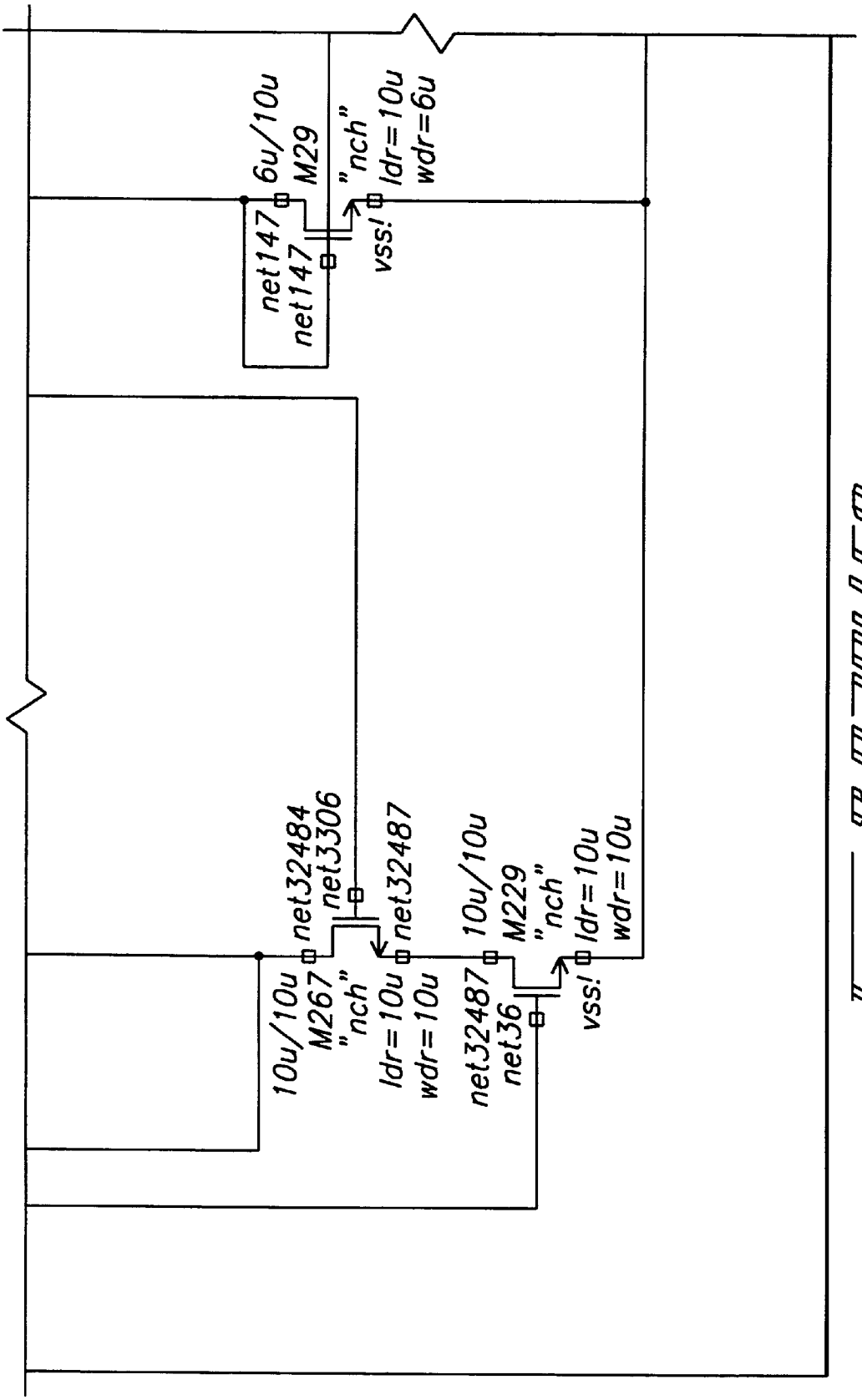


FIG 88.00204EA

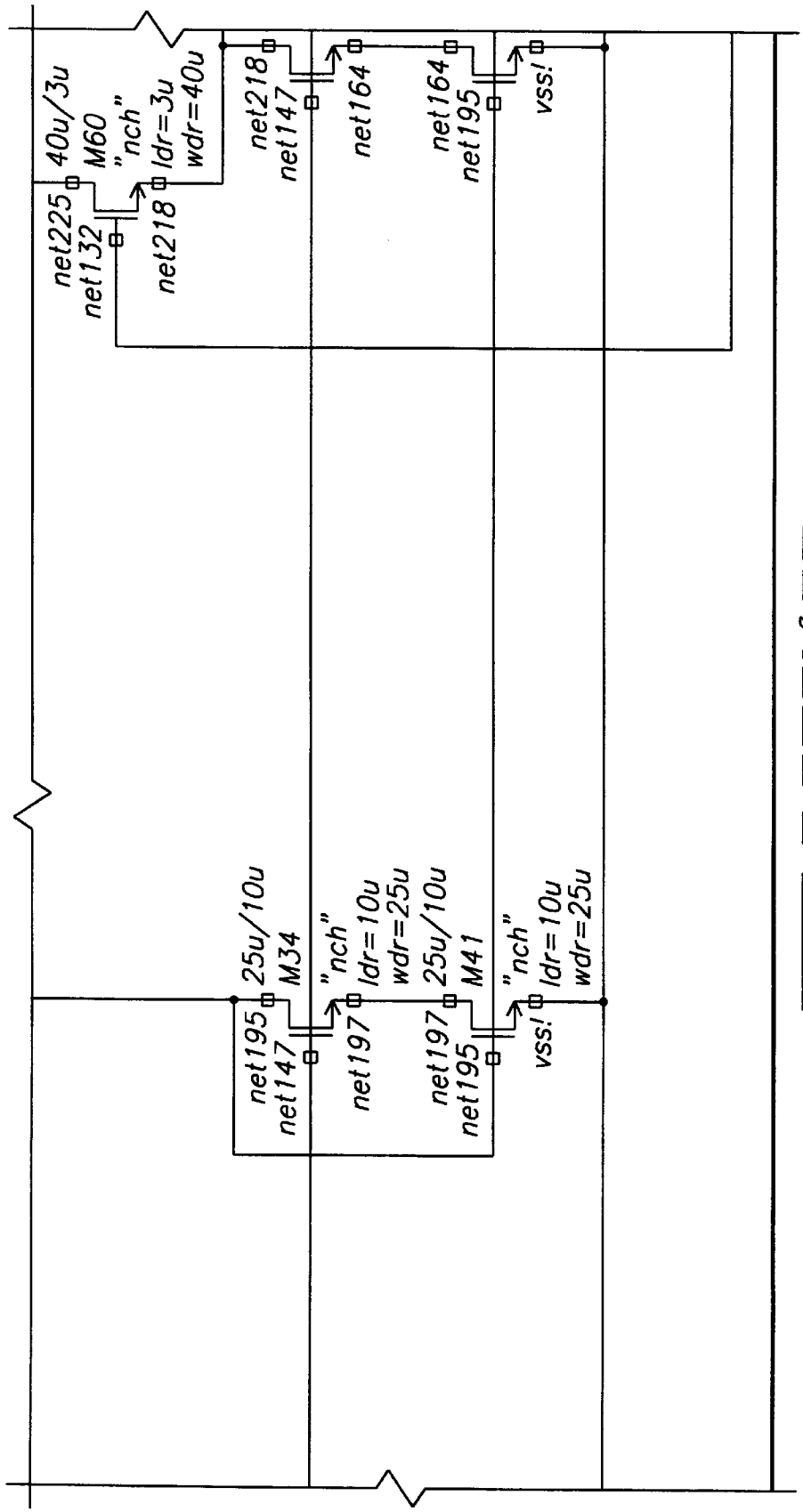

net225
net132
40u/3u
M60
"nch"
ldr=3u
wdr=40u
net218
net218
net147
net164
net164
net195
vss!
net195
net147
25u/10u
M34
"nch"
ldr=10u
wdr=25u
net197
net197
net195
25u/10u
M41
"nch"
ldr=10u
wdr=25u
vss!

FIG. 88,002

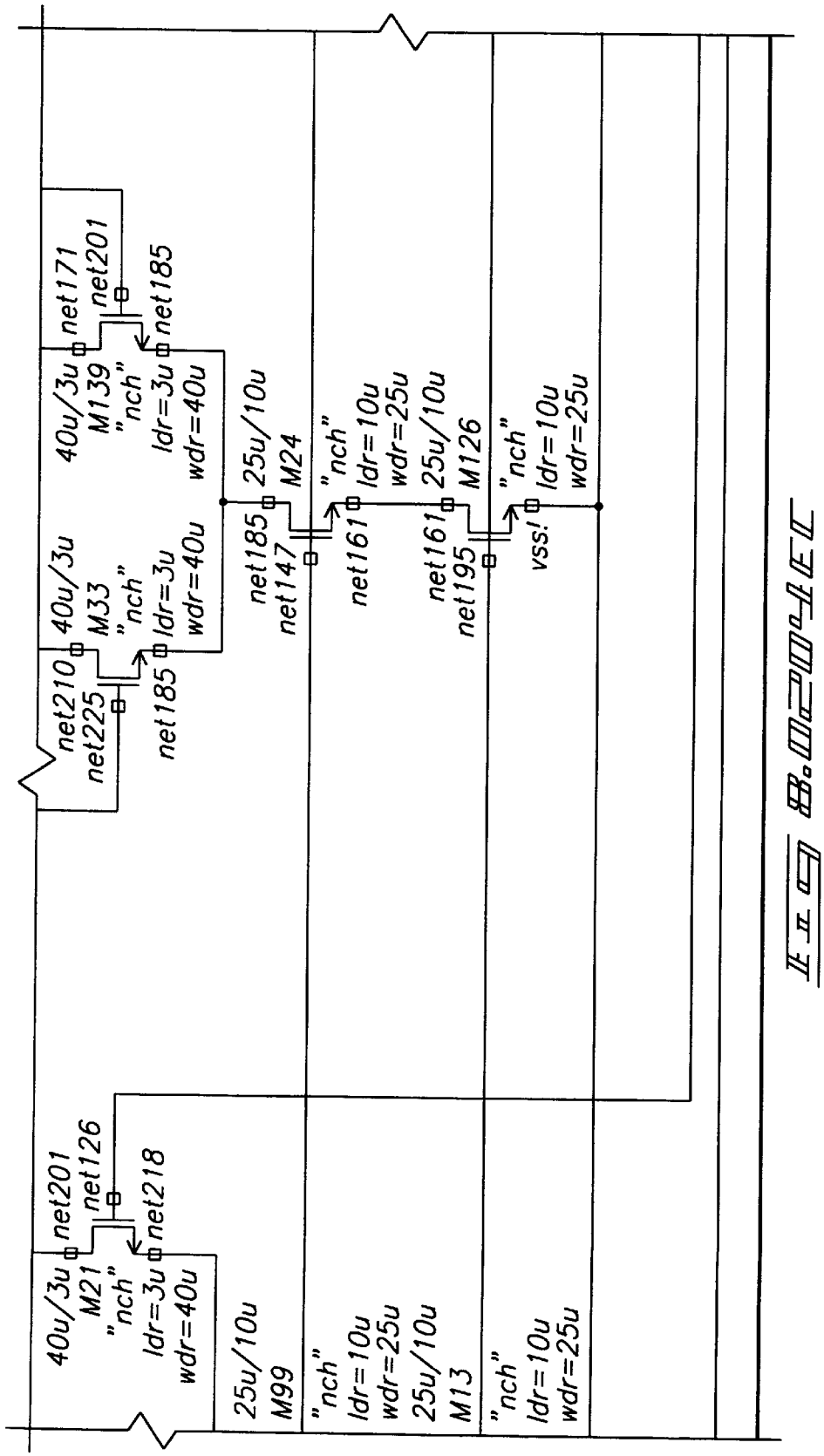

40u/3u
M21
"nch"
ldr=3u
wdr=40u
net201
net126
net218
25u/10u
M99
"nch"
ldr=10u
wdr=25u
25u/10u
M13
"nch"
ldr=10u
wdr=25u
net210
net225
40u/3u
M33
"nch"
ldr=3u
wdr=40u
net185
net185
net147
25u/10u
M24
"nch"
ldr=10u
wdr=25u
net161
net161
net195
25u/10u
M126
"nch"
ldr=10u
wdr=25u
vss!
40u/3u
M139
"nch"
ldr=3u
wdr=40u
net171
net201
net185

FIG. 88,002

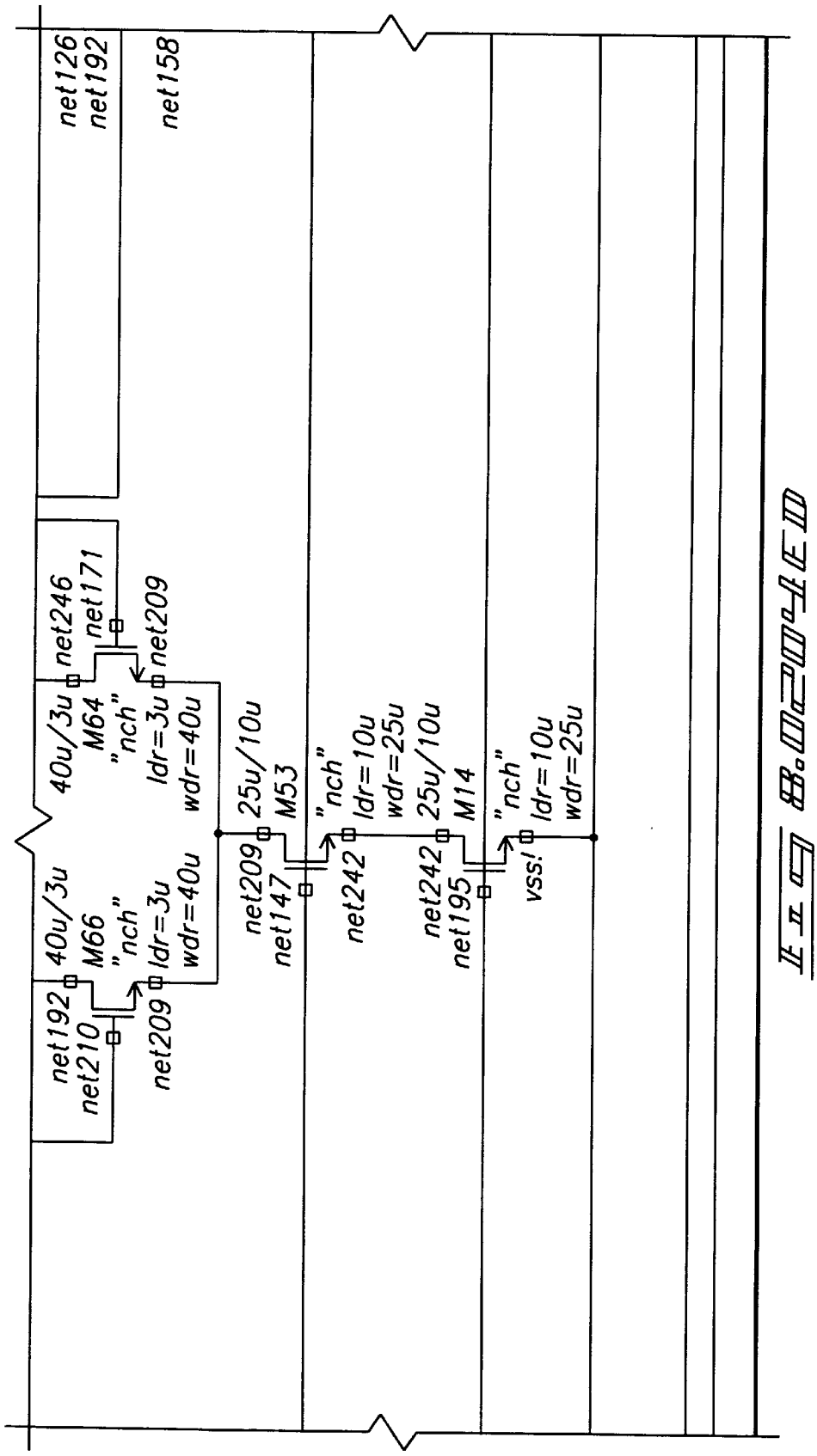

net126
net192
net158
net246
net171
net209
40u/3u
M64
"nch"
ldr=3u
wdr=40u
net192
net210
40u/3u
M66
"nch"
ldr=3u
wdr=40u
net209
25u/10u
M53
net209
net147
"nch"
ldr=10u
wdr=25u
net242
25u/10u
M14
net242
net195
"nch"
ldr=10u
wdr=25u
vss!

FIG. 88.002A

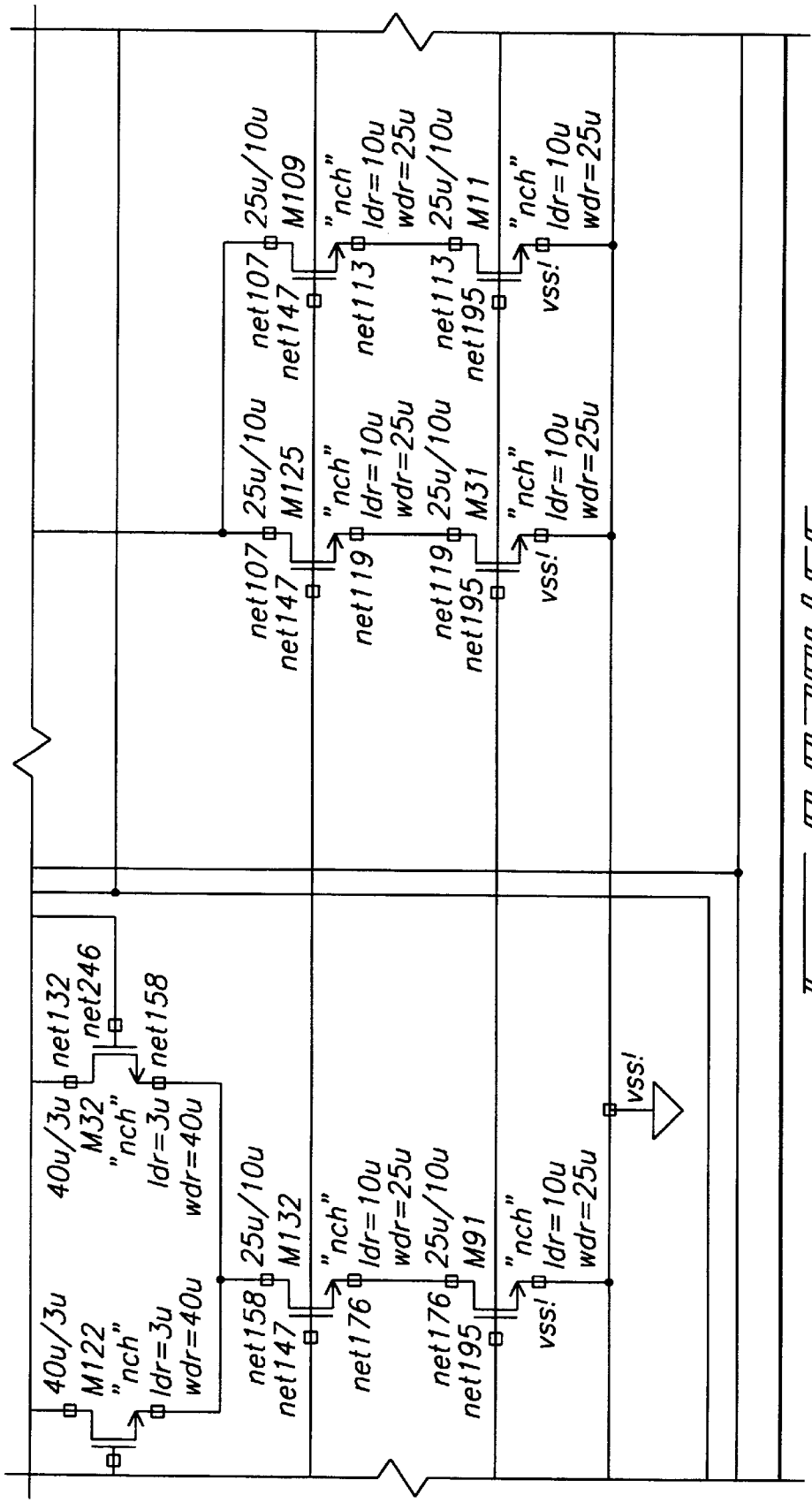

net107
net147
25u/10u
M125
"nch"
ldr=10u
wdr=25u
net119
net107
net147
25u/10u
M109
"nch"
ldr=10u
wdr=25u
net113
net119
net195
25u/10u
M31
"nch"
ldr=10u
wdr=25u
vss!
net113
net195
25u/10u
M11
"nch"
ldr=10u
wdr=25u
vss!
net132
net246
40u/3u
M32
"nch"
ldr=3u
wdr=40u
net158
40u/3u
M122
"nch"
ldr=3u
wdr=40u
net158
net147
25u/10u
M132
"nch"
ldr=10u
wdr=25u
net176
net176
net195
25u/10u
M91
"nch"
ldr=10u
wdr=25u
vss!
vss!

FIG. 88.0004E

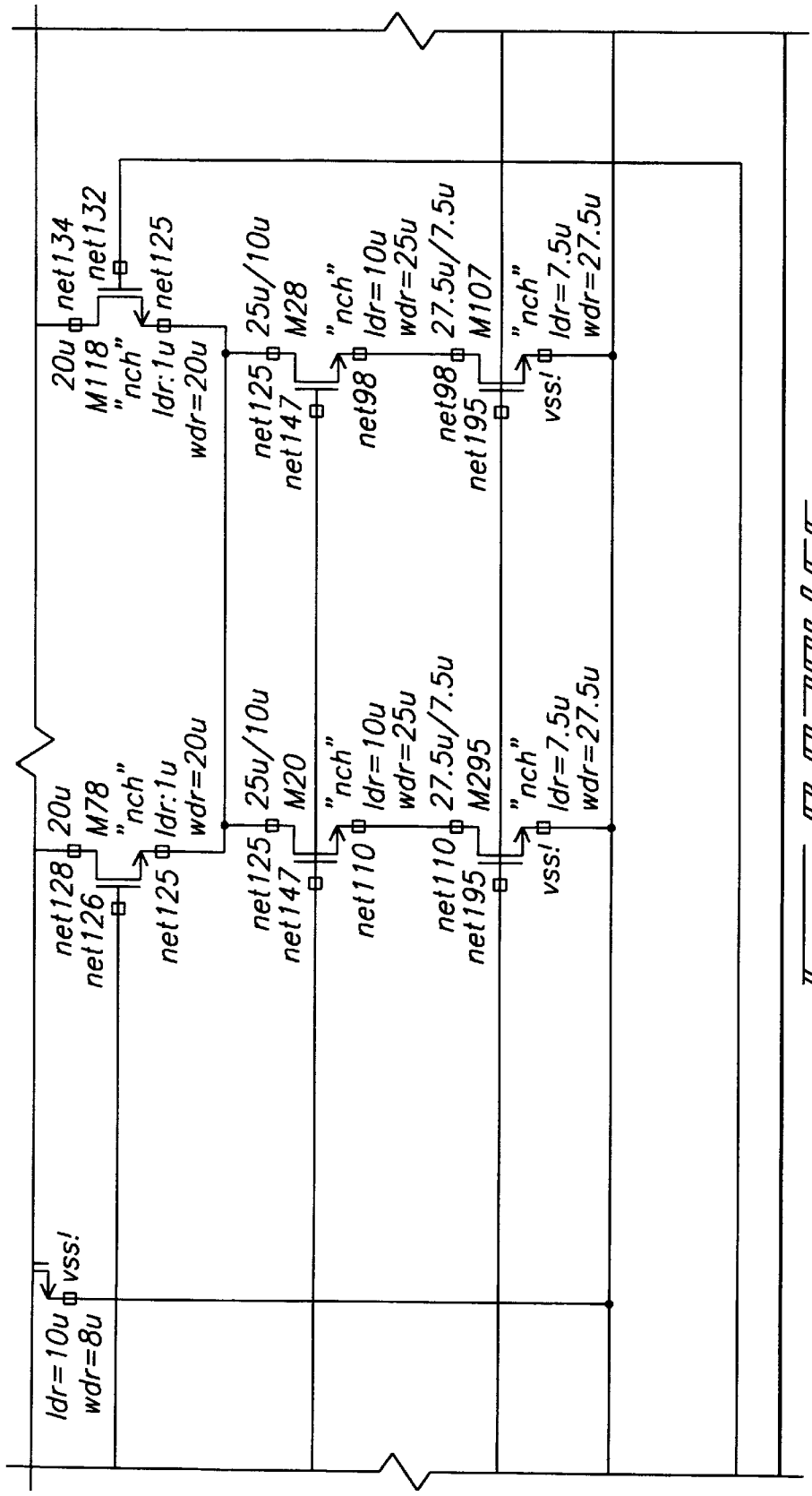


FIG 88.00204E

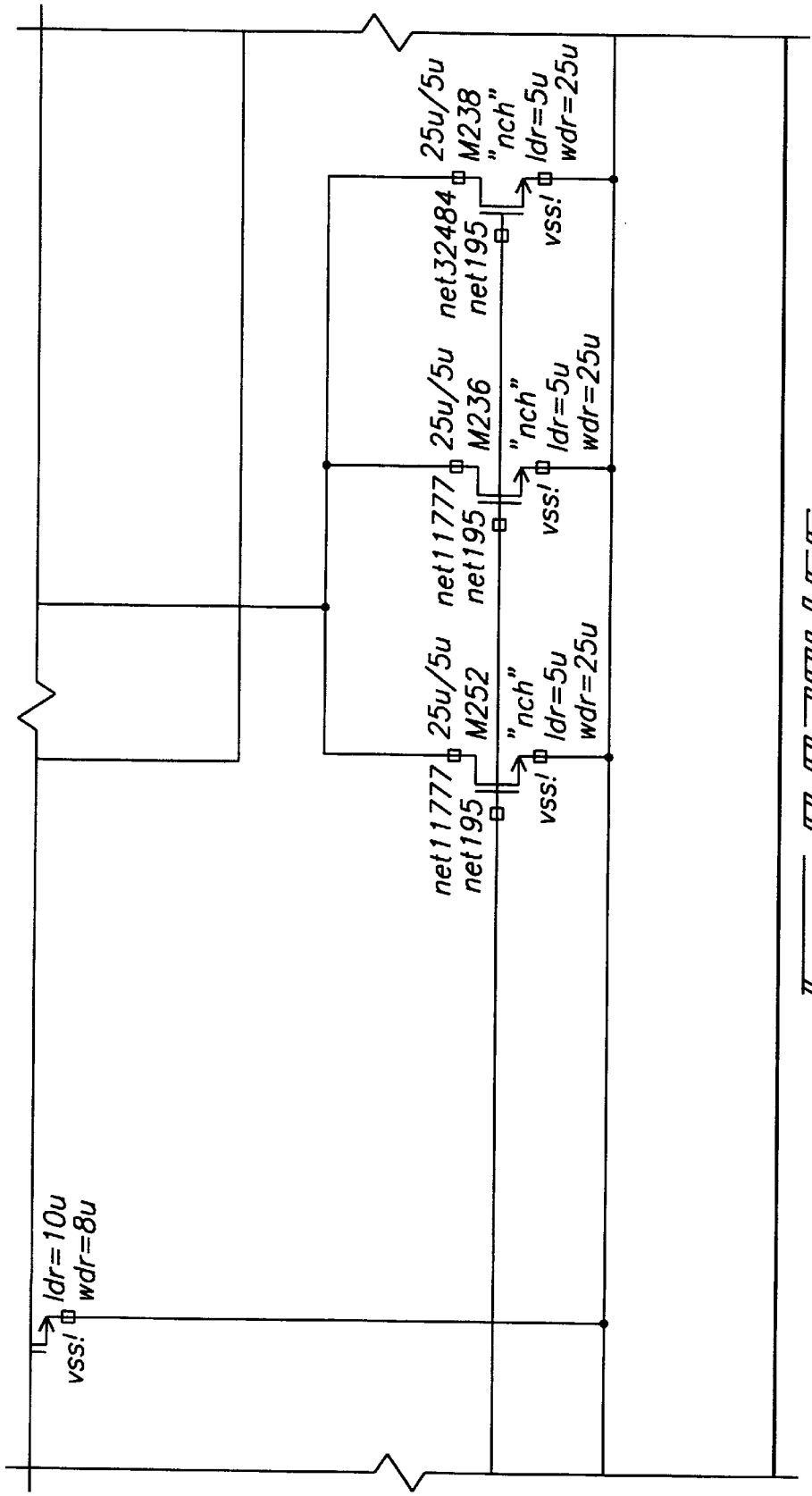


FIG 88.00404E

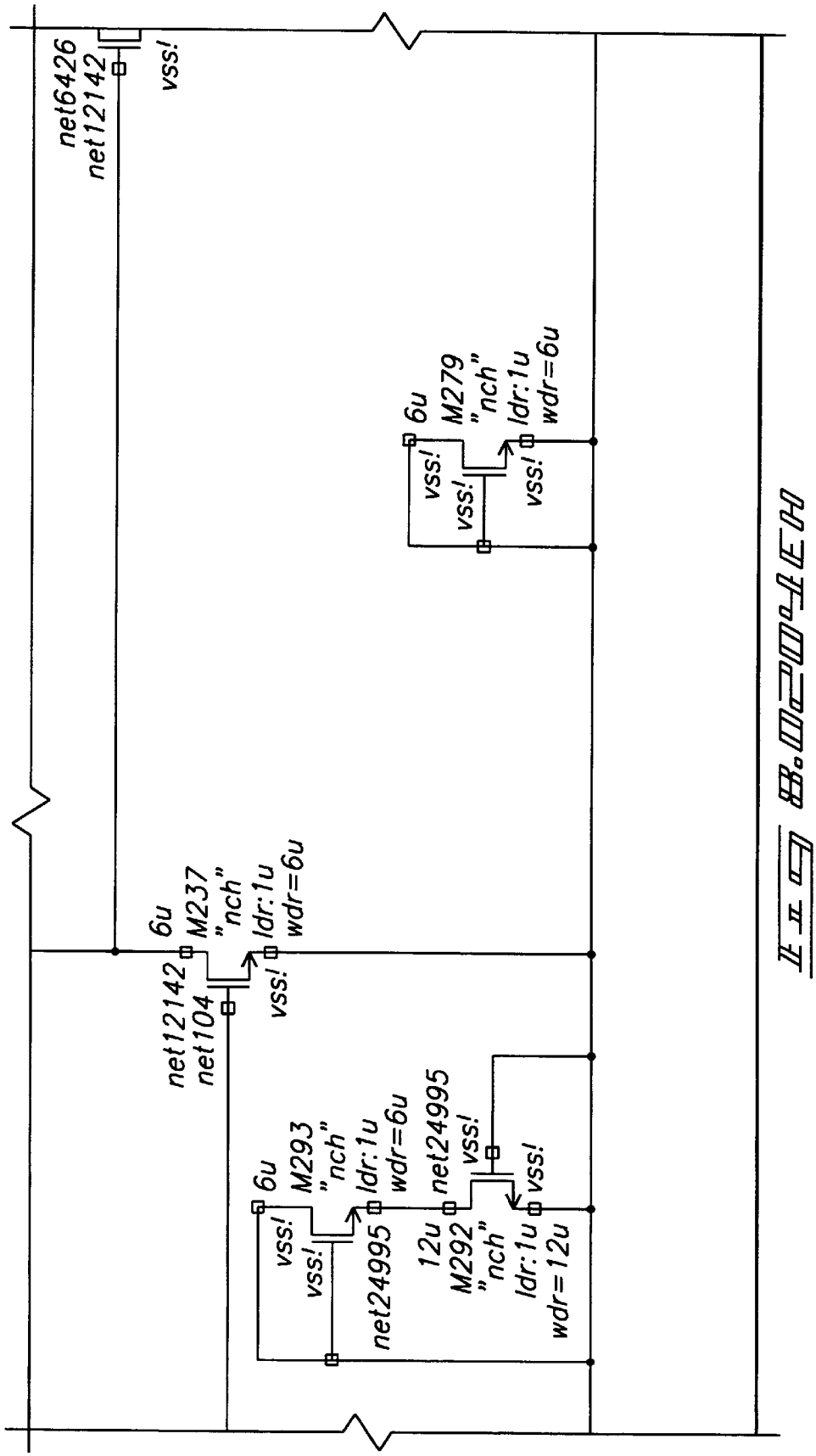
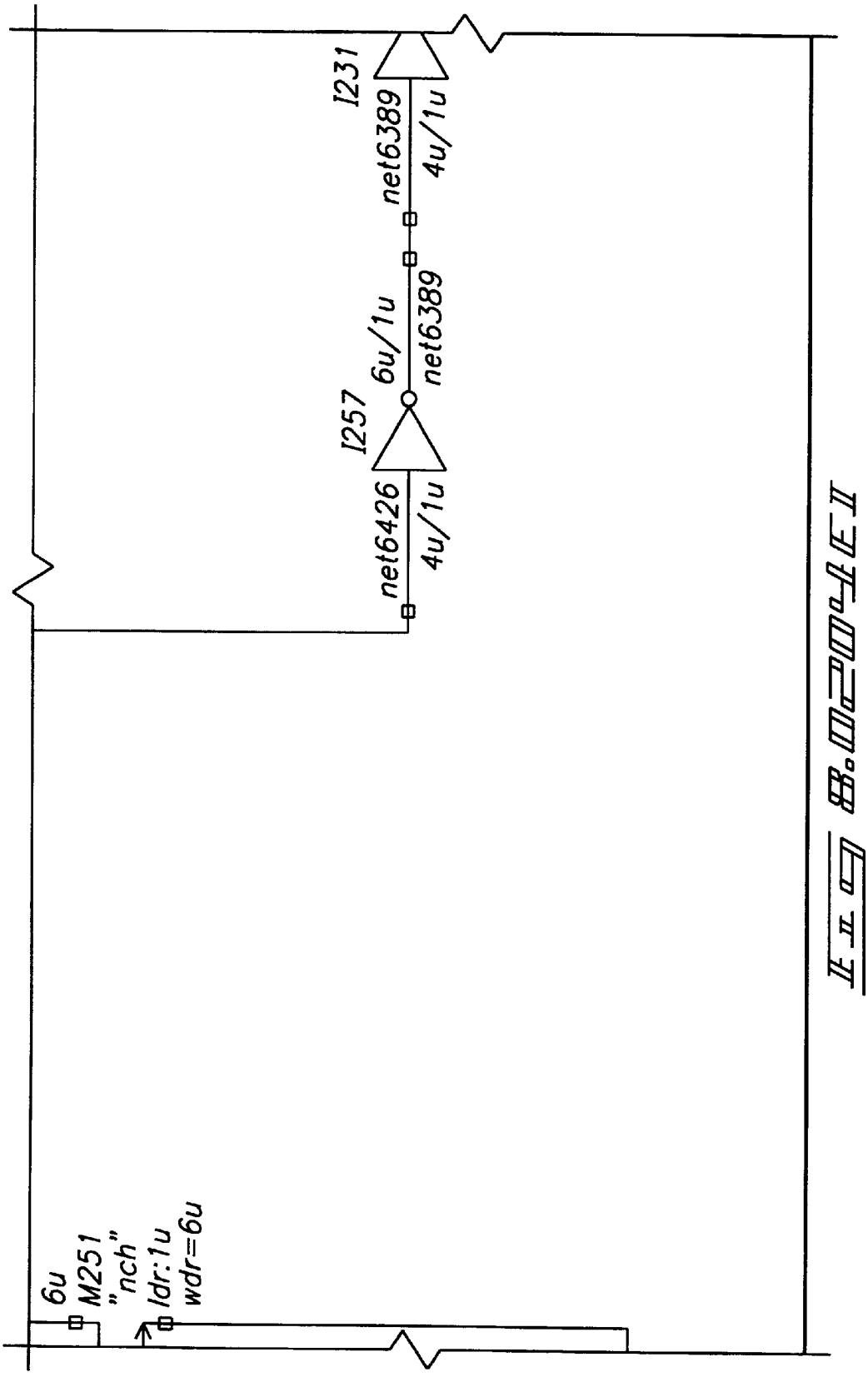

net6426
net12142
vss!
6u
M279
"nch"
ldr:1u
wdr=6u
vss!
vss!
vss!
6u
M237
"nch"
ldr:1u
wdr=6u
net12142
net104
vss!
6u
M293
"nch"
ldr:1u
wdr=6u
net24995
vss!
vss!
net24995
12u
M292
"nch"
ldr:1u
wdr=12u
net24995
vss!
vss!

FIG. 8,002,602


I231
net6389
4u/1u
net6389
6u/1u
I257
net6426
4u/1u
6u
M251
"nch"
ldr:1u
wdr=6u
FIG 88,020A-II

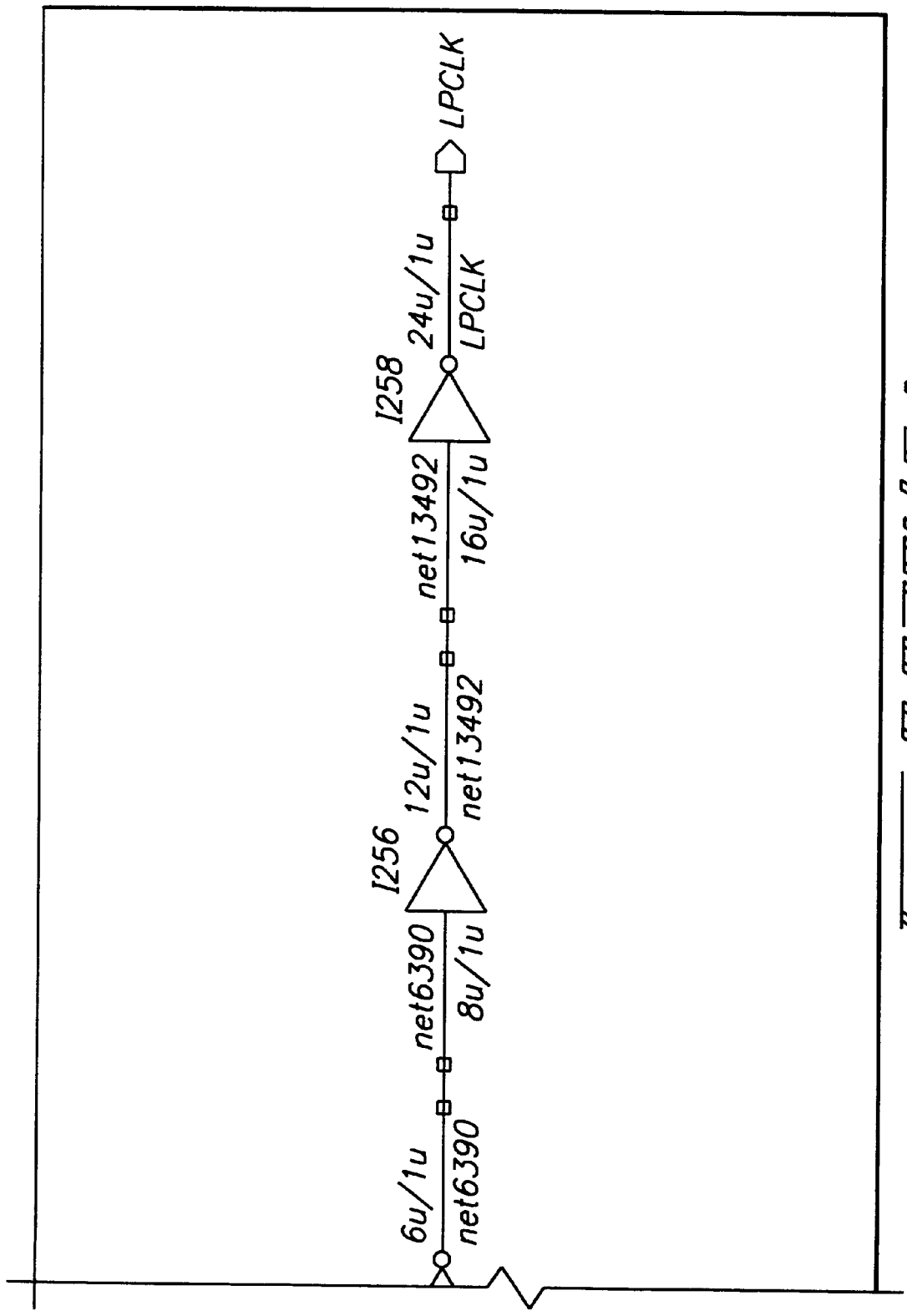


FIG 88.00204E

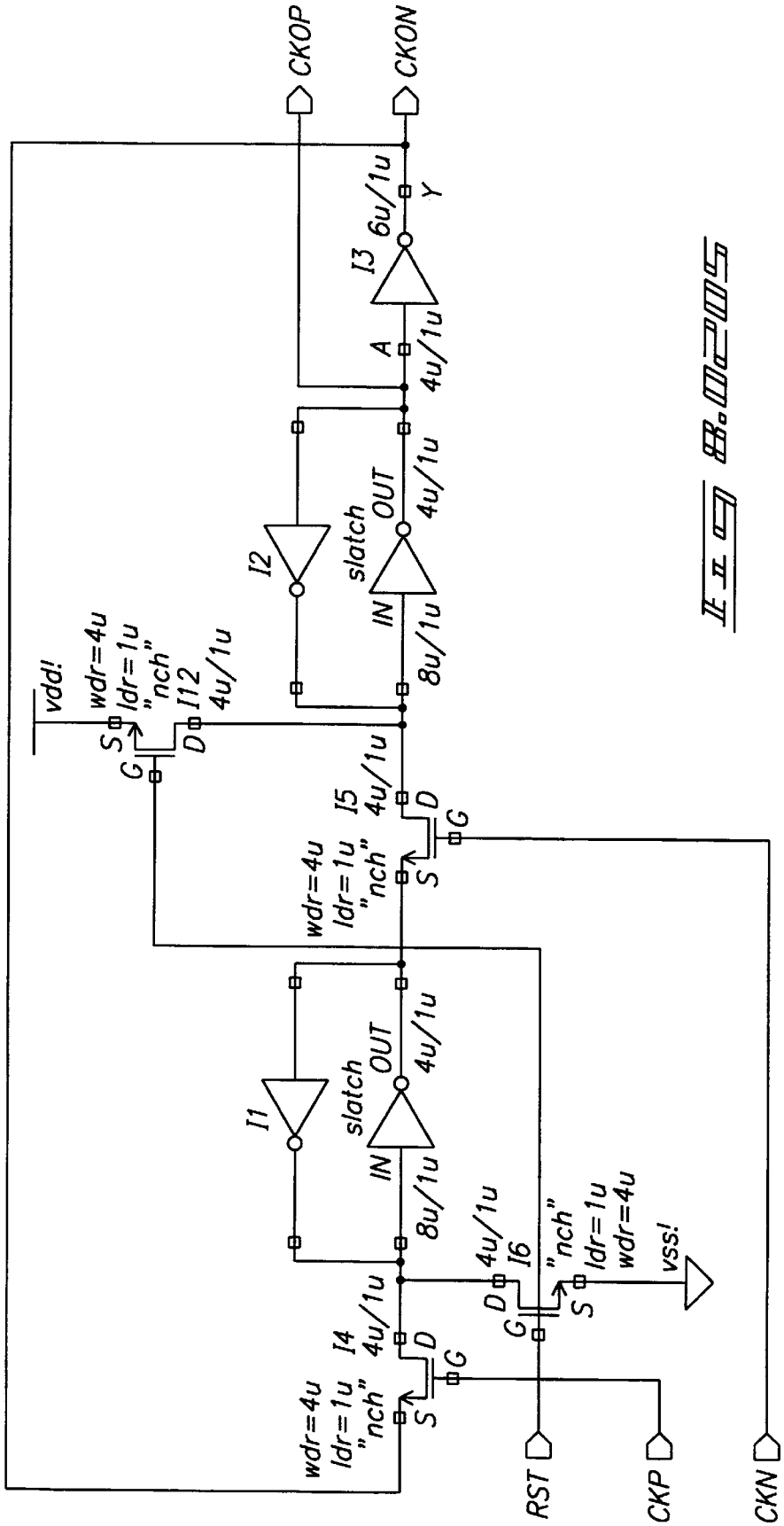
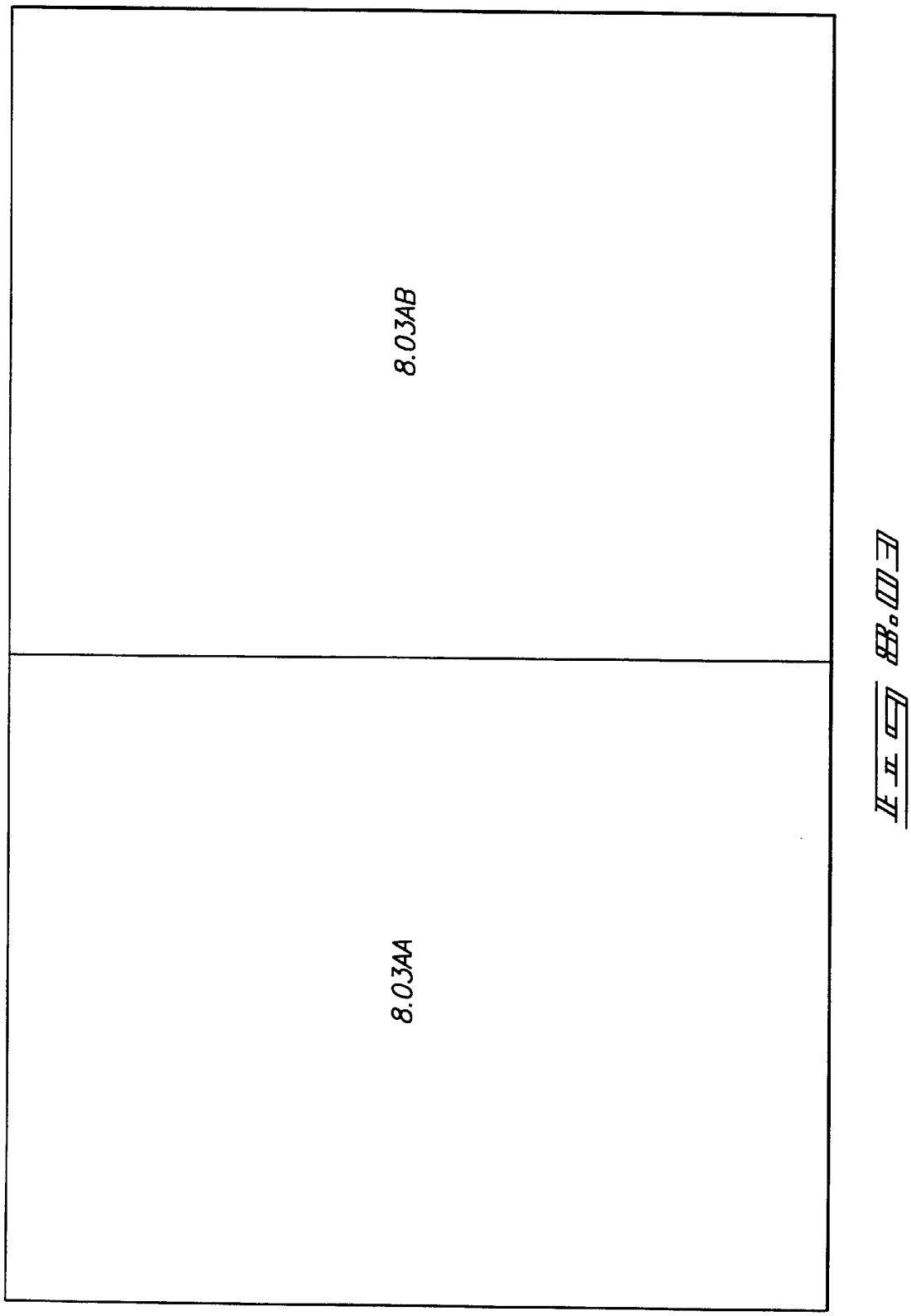

CKOP
CKON
I3
6u/1u
Y
A
4u/1u
I2
slatch
OUT
IN
4u/1u
8u/1u
vdd!
wdr=4u
ldr=1u
"nch"
I12
4u/1u
S
D
G
I5
4u/1u
wdr=4u
ldr=1u
"nch"
I1
slatch
OUT
IN
4u/1u
8u/1u
I6
4u/1u
"nch"
ldr=1u
wdr=4u
vss!
I4
4u/1u
wdr=4u
ldr=1u
"nch"
RST
CKP
CKN

Fig. 1385


8.03AB
8.03AA
E00.88 FT

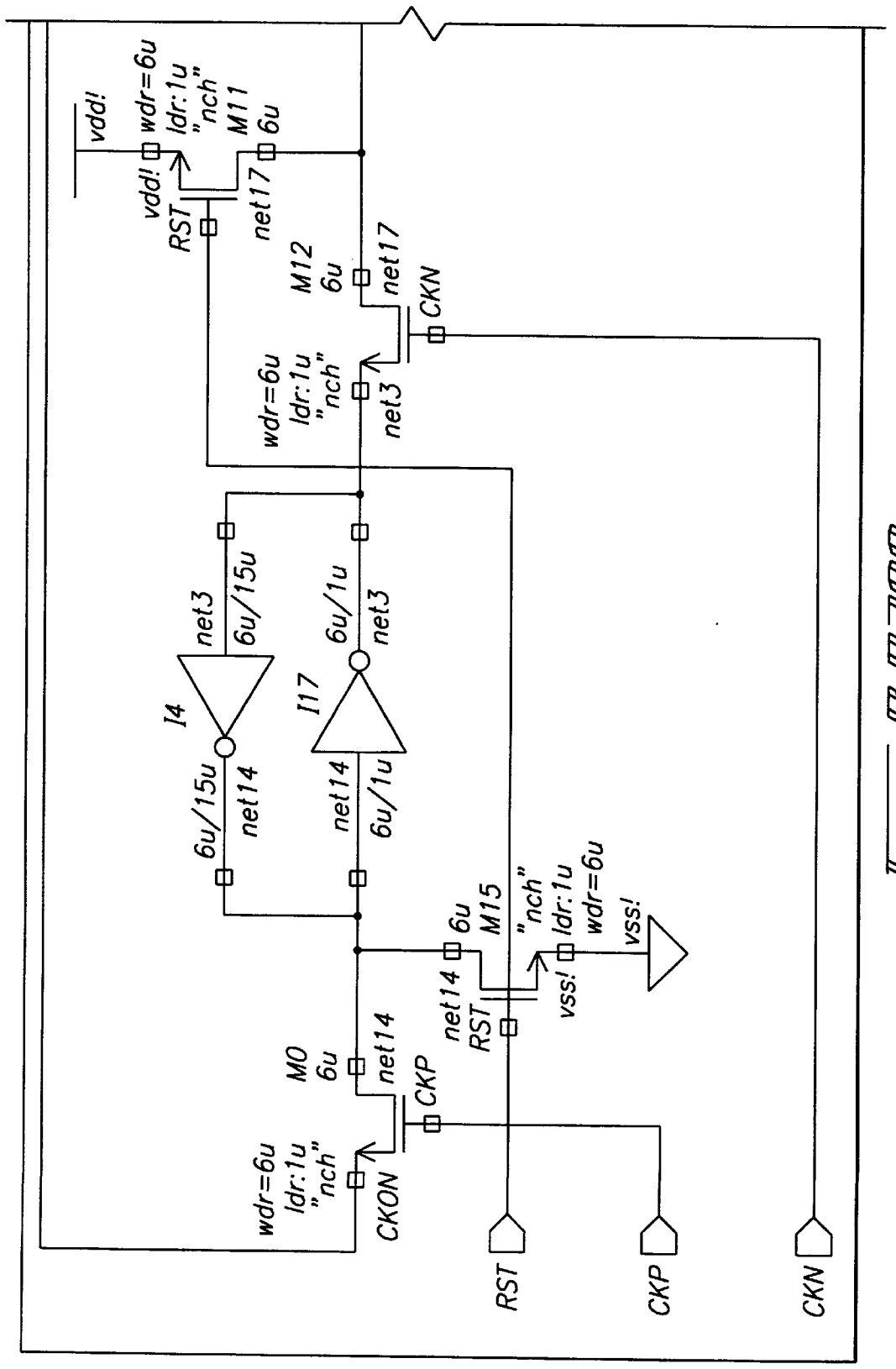

vdd!
wdr=6u
ldr:1u
"nch"
M11
6u
RST
net17
M12
6u
CKN
wdr=6u
ldr:1u
"nch"
net3
net3
6u/15u
I4
6u/15u
net14
6u/1u
net3
I17
net14
6u/1u
6u
M15
"nch"
ldr:1u
wdr=6u
vss!
net14
RST
vss!
M0
6u
net14
CKP
wdr=6u
ldr:1u
"nch"
CKON
RST
CKP
CKN

FIG. 1387

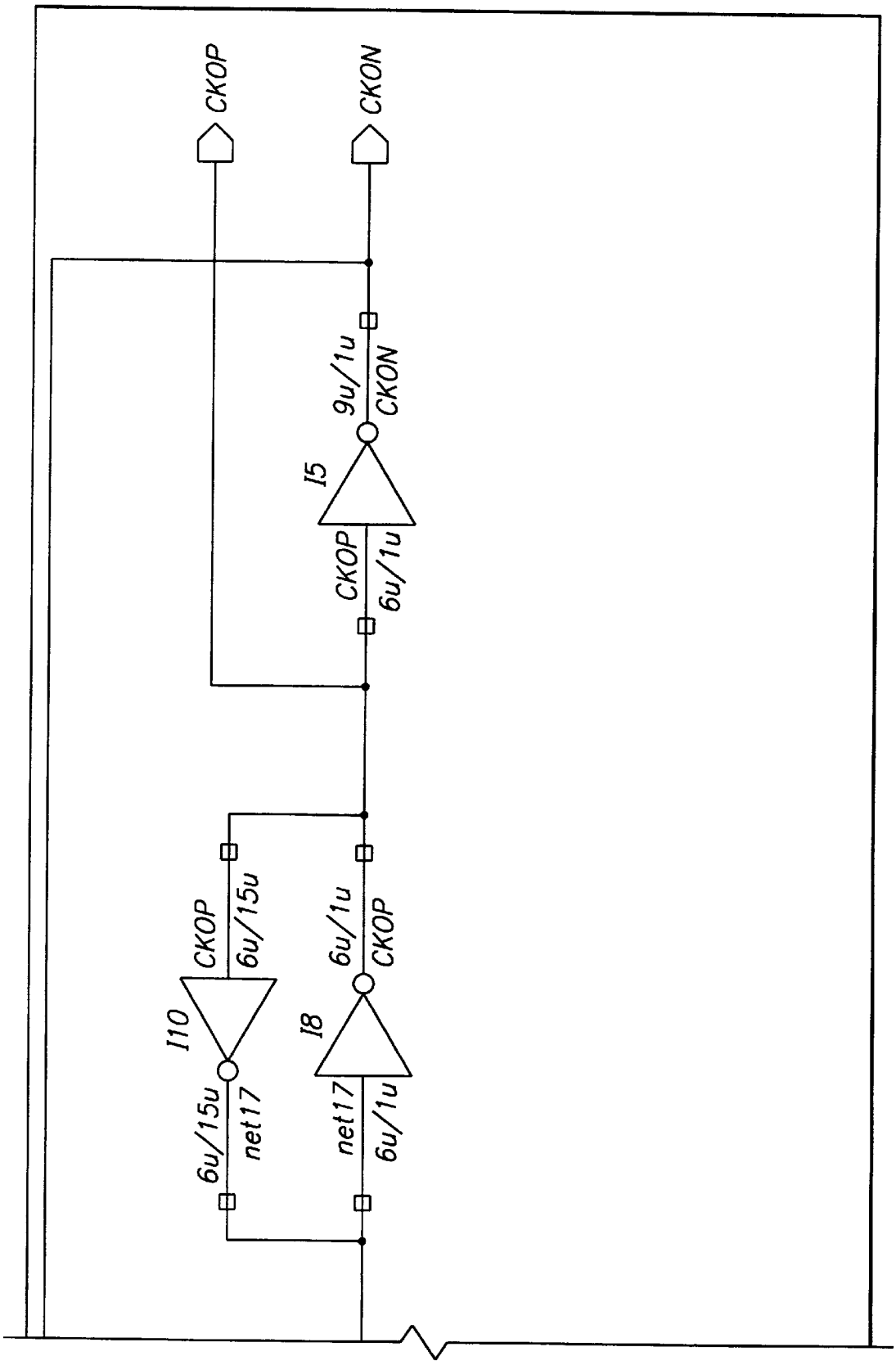

CKOP
CKON
9u/1u
CKON
I5
CKOP
6u/1u
CKOP
6u/15u
6u/1u
CKOP
I10
I8
6u/15u
net17
net17
6u/1u

FIG. 88.00

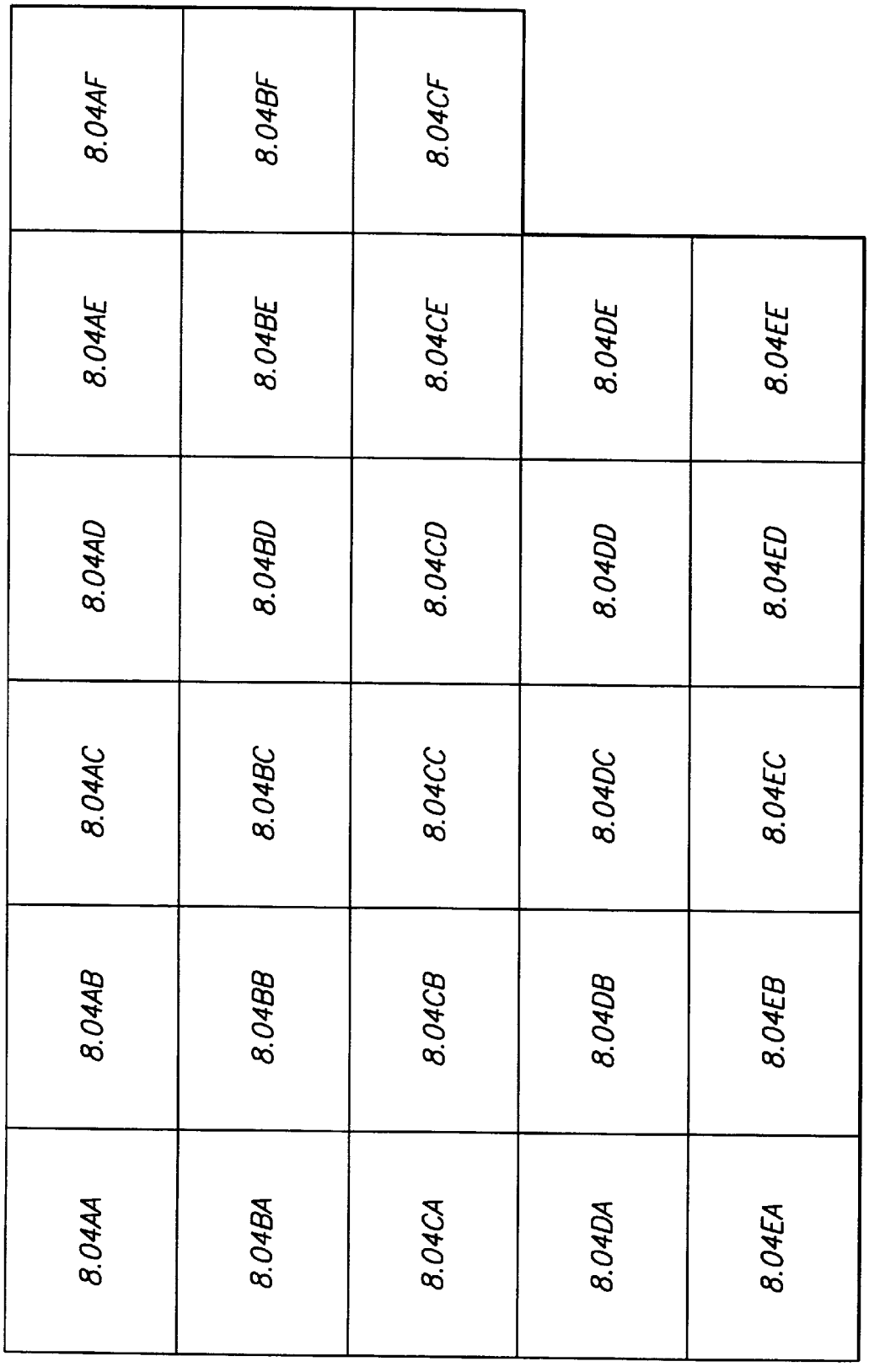

8.04AA
8.04AB
8.04AC
8.04AD
8.04AE
8.04AF
8.04BA
8.04BB
8.04BC
8.04BD
8.04BE
8.04BF
8.04CA
8.04CB
8.04CC
8.04CD
8.04CE
8.04CF
8.04DA
8.04DB
8.04DC
8.04DD
8.04DE
8.04EA
8.04EB
8.04EC
8.04ED
8.04EE

FIG. 8.04

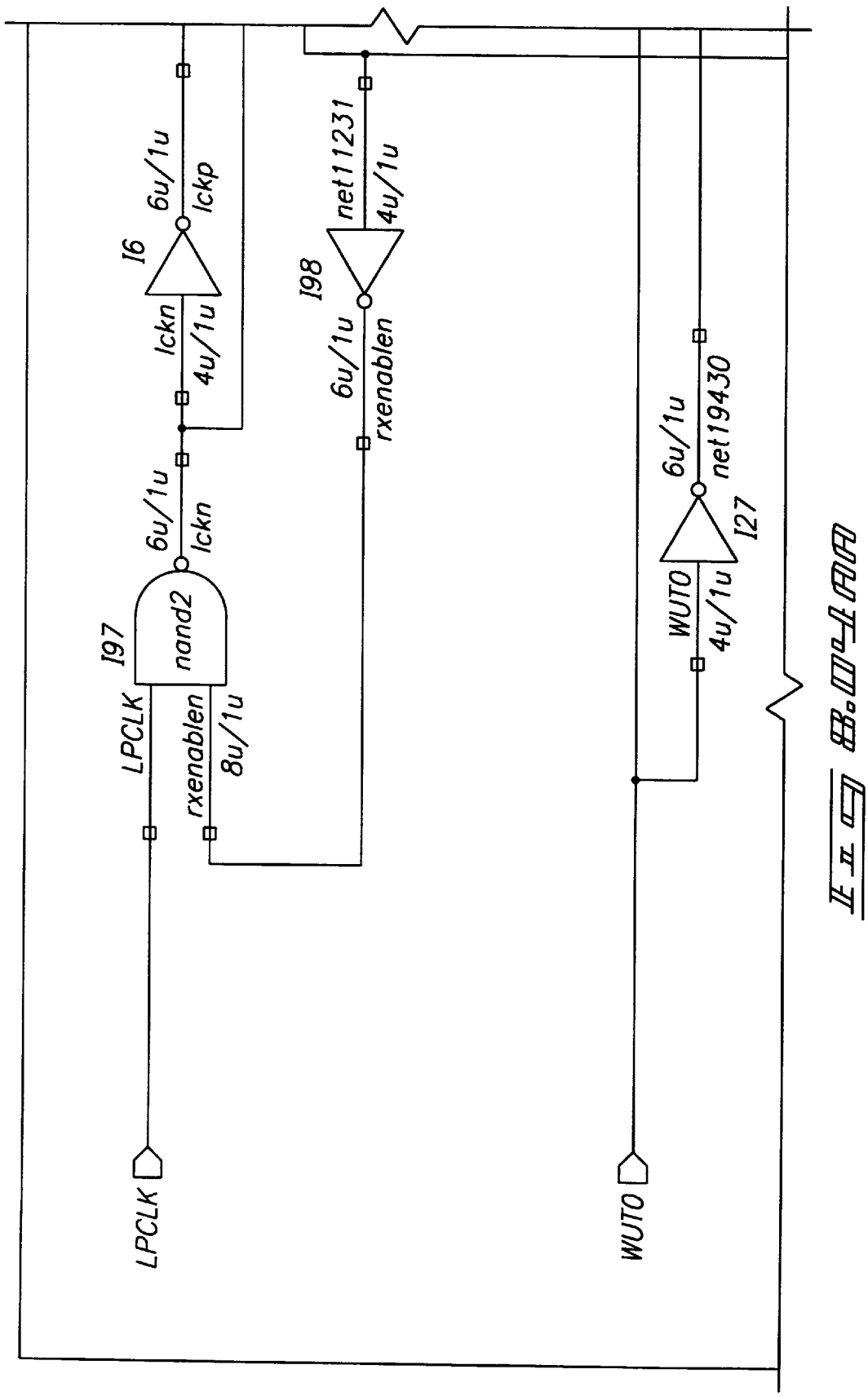

6u/1u
lckp
I6
lckn
4u/1u
6u/1u
lckn
I97
nand2
LPCLK
rxenablen
8u/1u
LPCLK
net11231
4u/1u
I98
6u/1u
rxenablen
6u/1u
net19430
I27
WUTO
4u/1u
WUTO

FIG. 88,004A

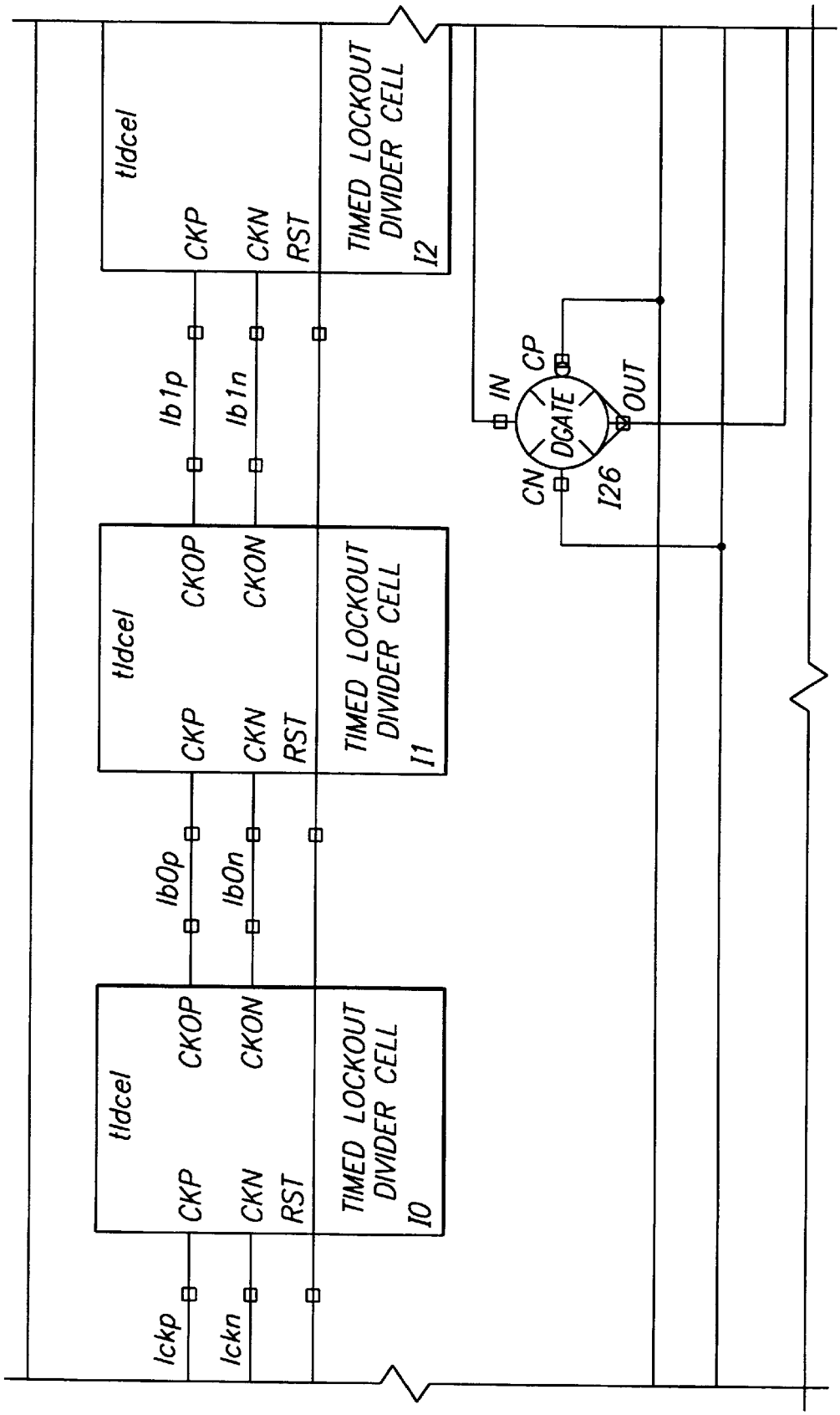

tldcel
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL
I2
lb1p
lb1n
tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL
I1
lb0p
lb0n
tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL
I0
lckp
lckn
IN
CP
DGATE
CN
OUT
I26

FIG 88.00-4AB

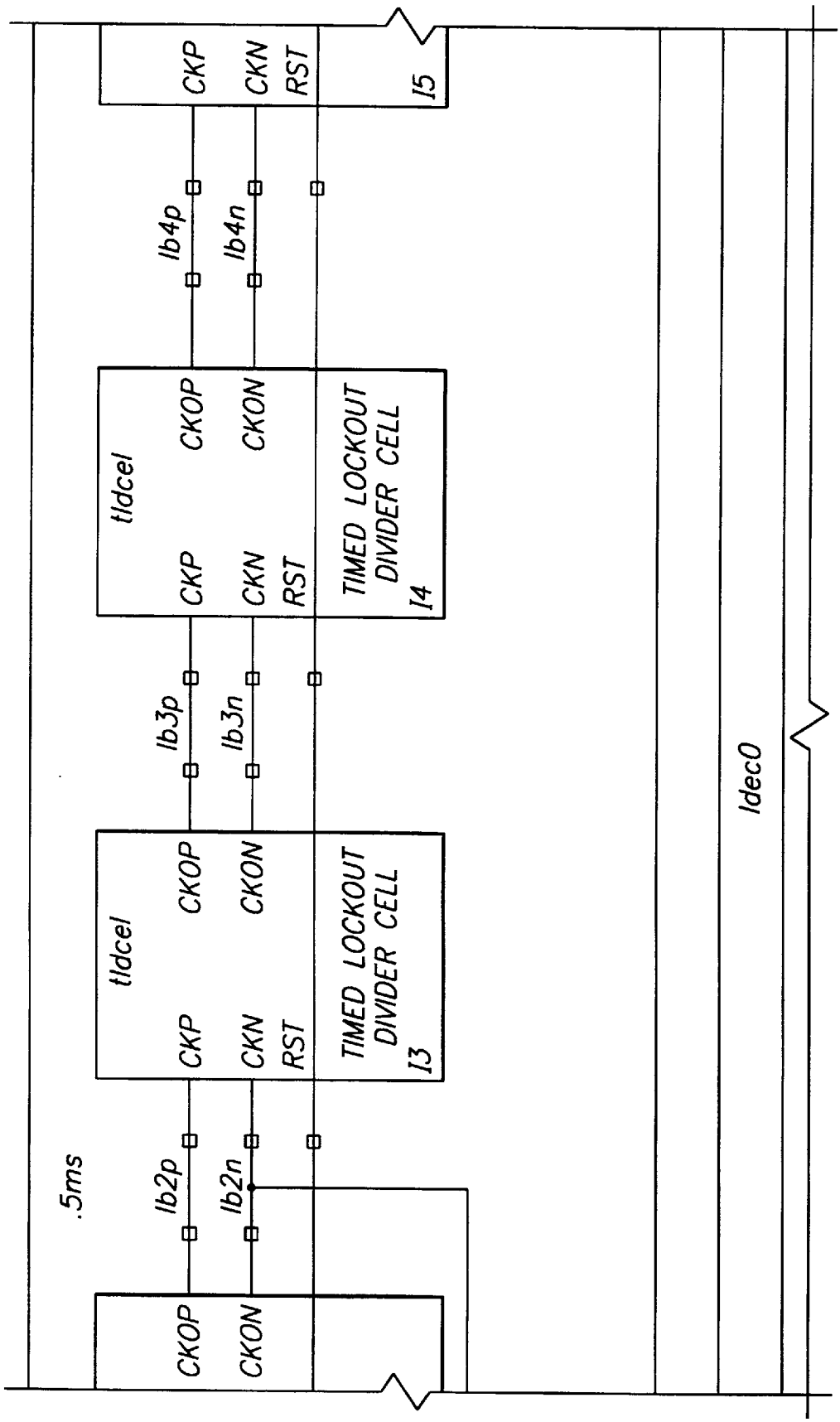


FIG 88.004AAC

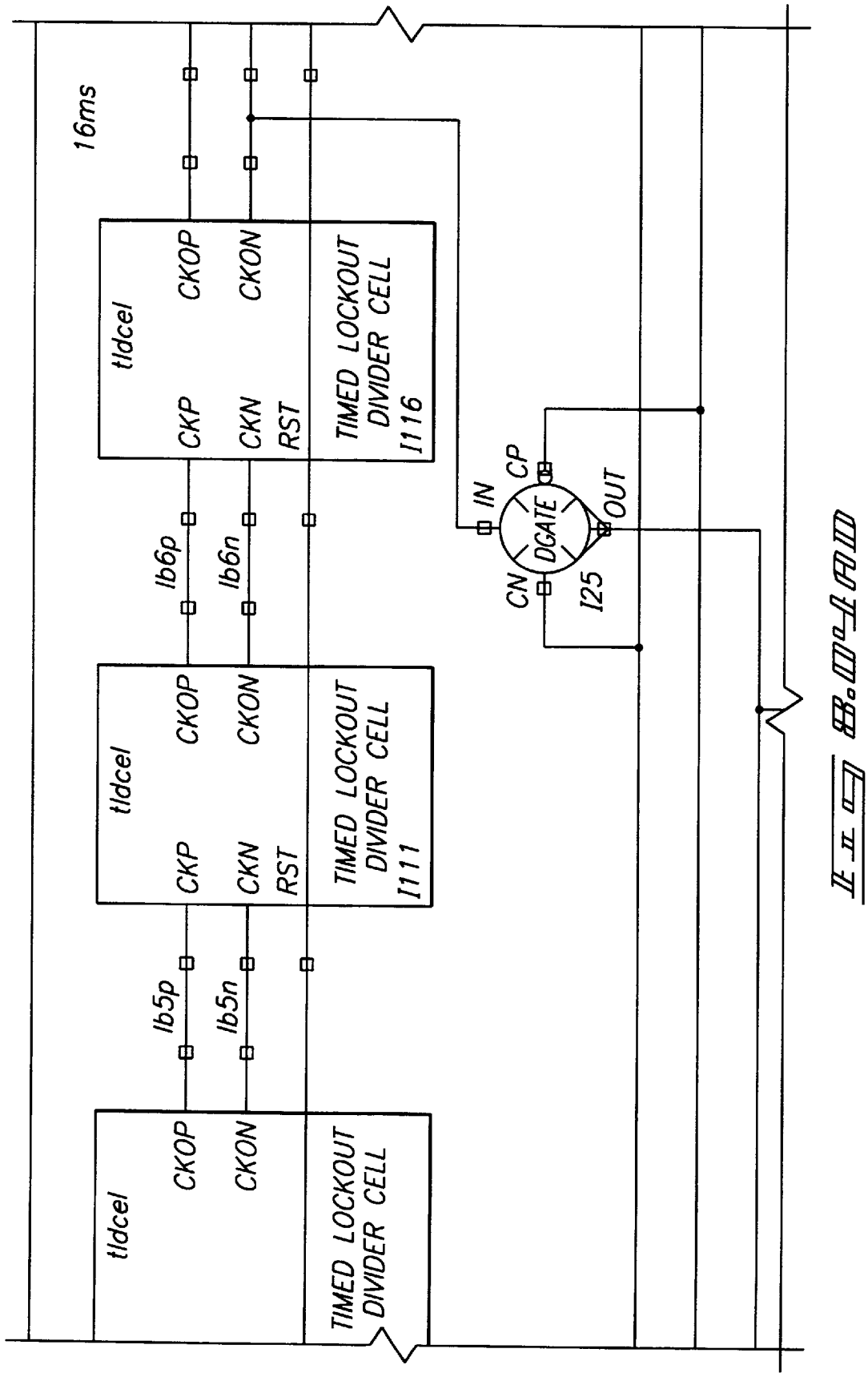

16ms
tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL I116
lb6p
lb6n
TIMED LOCKOUT DIVIDER CELL I111
lb5p
lb5n
TIMED LOCKOUT DIVIDER CELL
IN
CP
DGATE
OUT
CN
I25

FIG. 883A

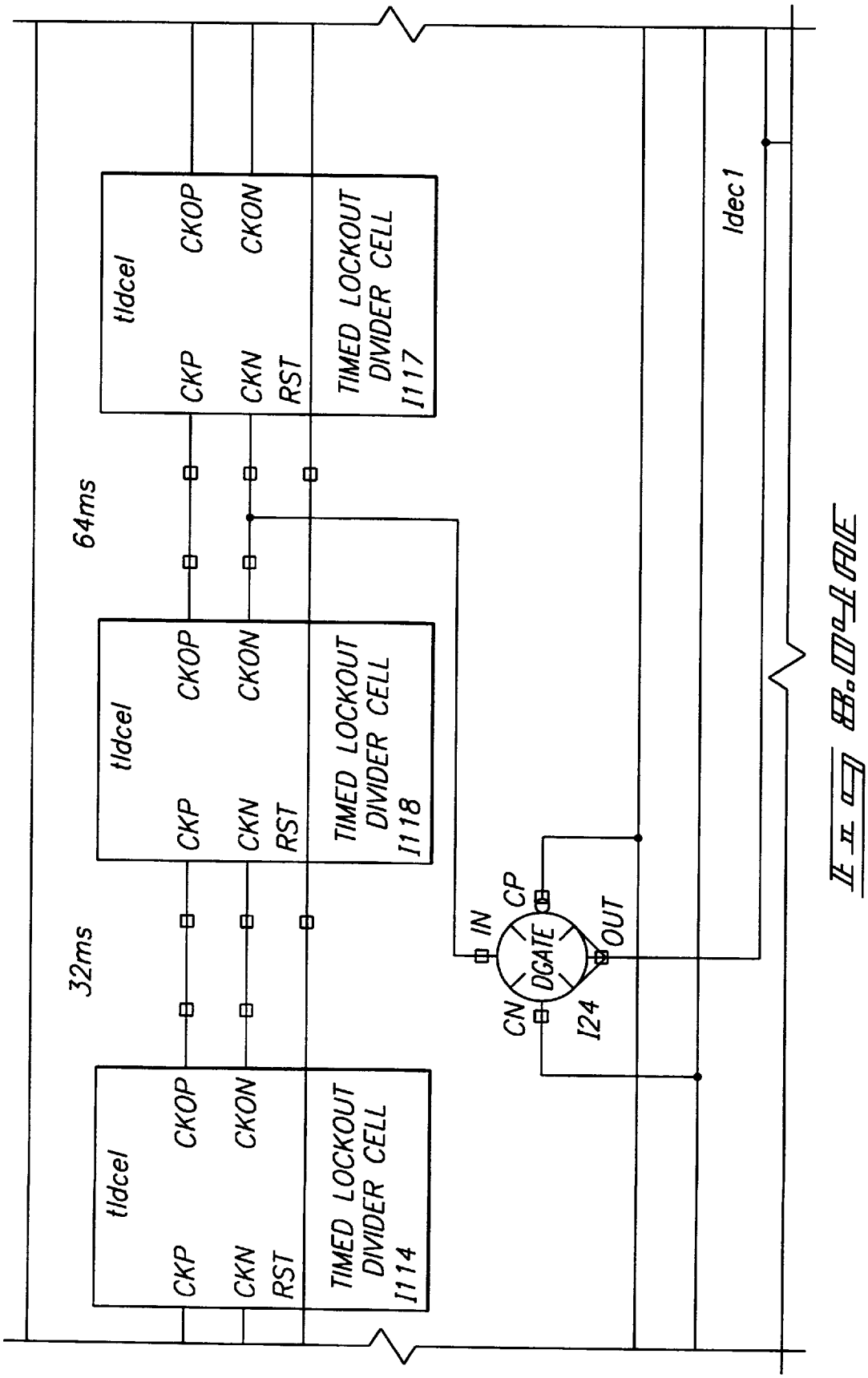

tldcel
CKOP
CKON
CKP
CKN
RST
TIMED LOCKOUT DIVIDER CELL
I117
64ms
I118
32ms
I114
IN
CP
DGATE
CN
OUT
I24
ldec1

FIG. 88.04-1AE

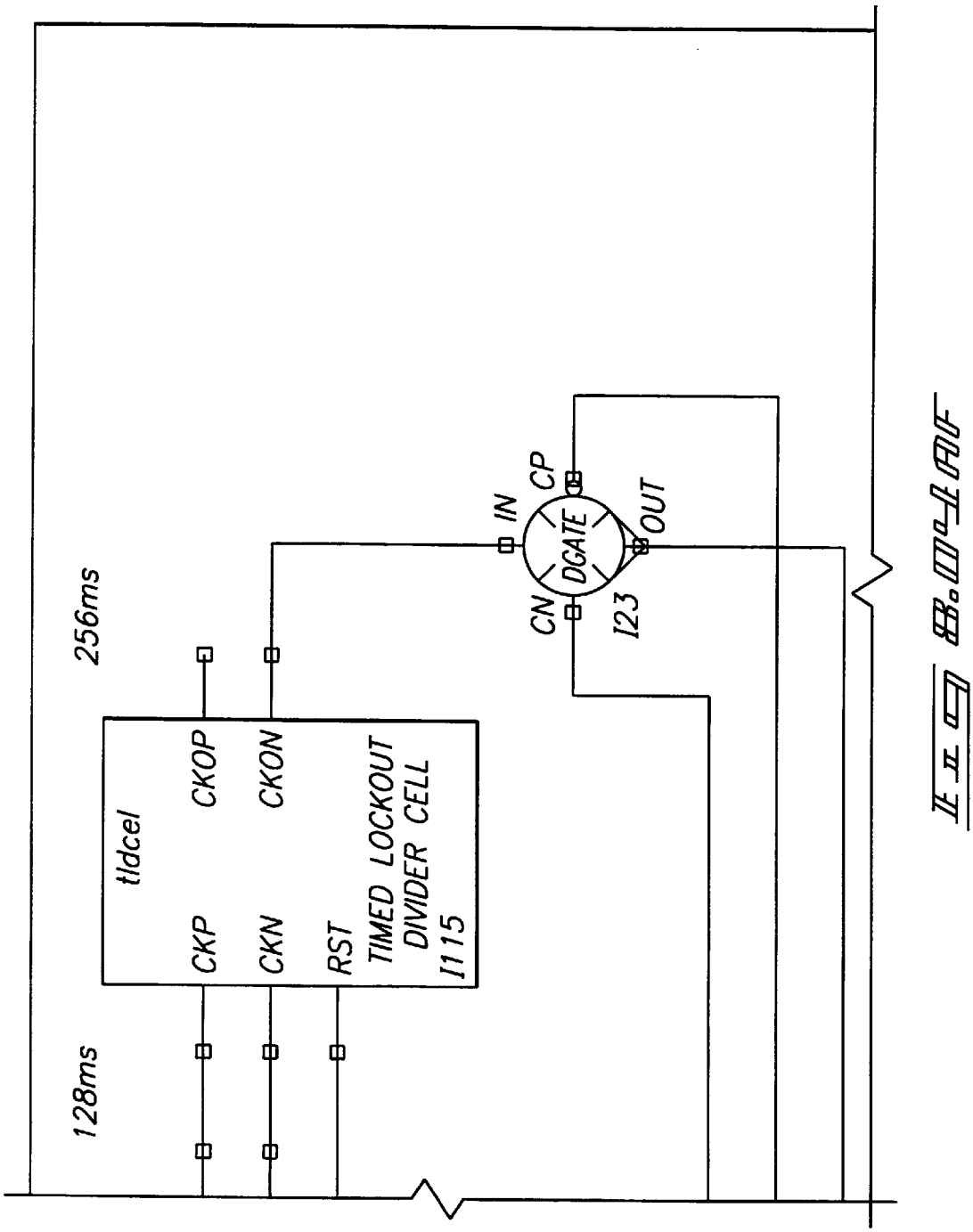


FIG 88.00+1AUF

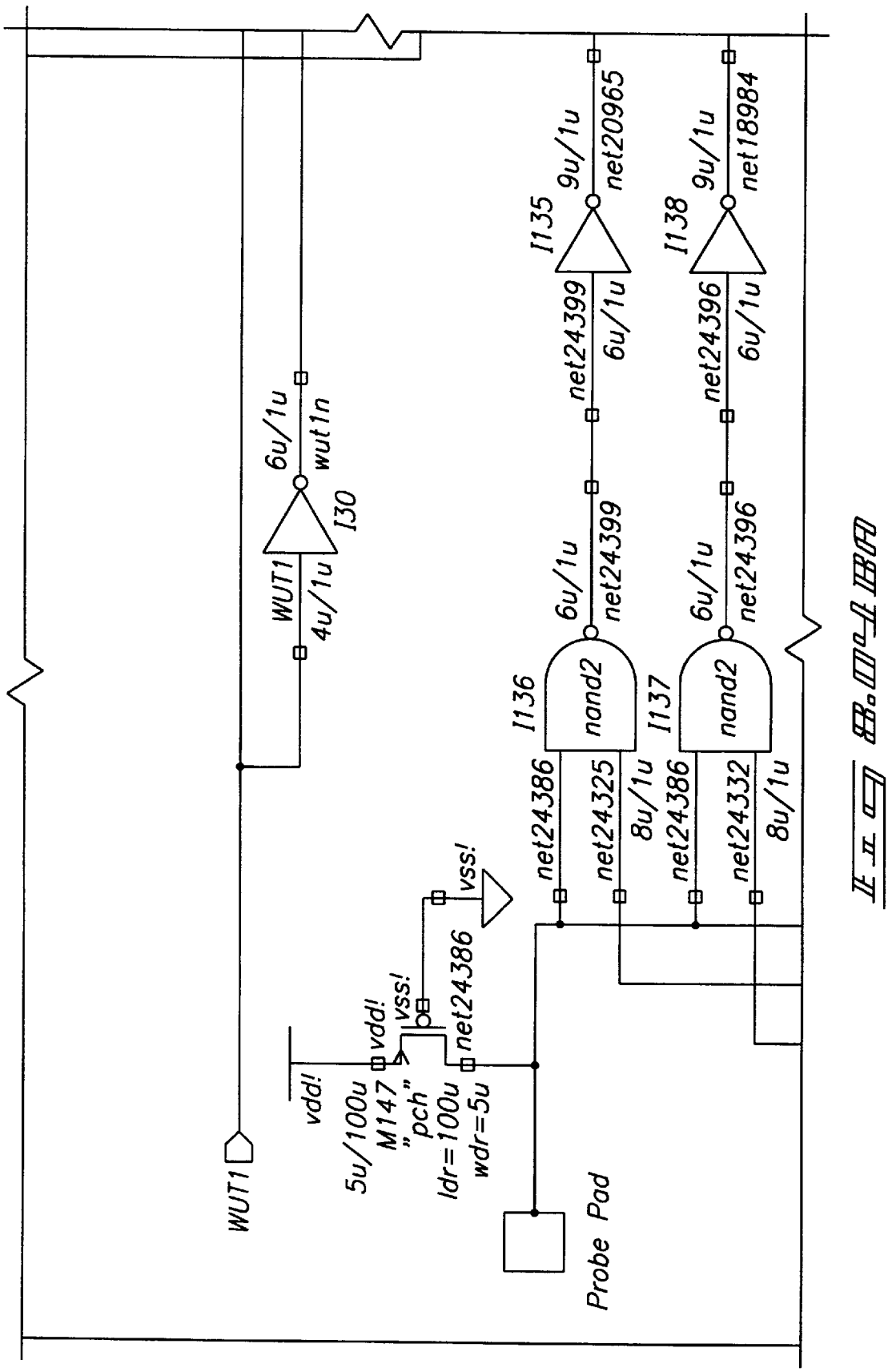

WUT1
5u/100u
M147
"pch"
ldr=100u
wdr=5u
vdd!
vdd!
vss!
net24386
vss!
Probe Pad
I136
nand2
6u/1u
net24386
net24325
8u/1u
I137
nand2
6u/1u
net24386
net24332
8u/1u
I135
9u/1u
net20965
6u/1u
net24399
I138
9u/1u
net18984
6u/1u
net24396
WUT1
4u/1u
I30
6u/1u
wut1n

FIG 8.0011

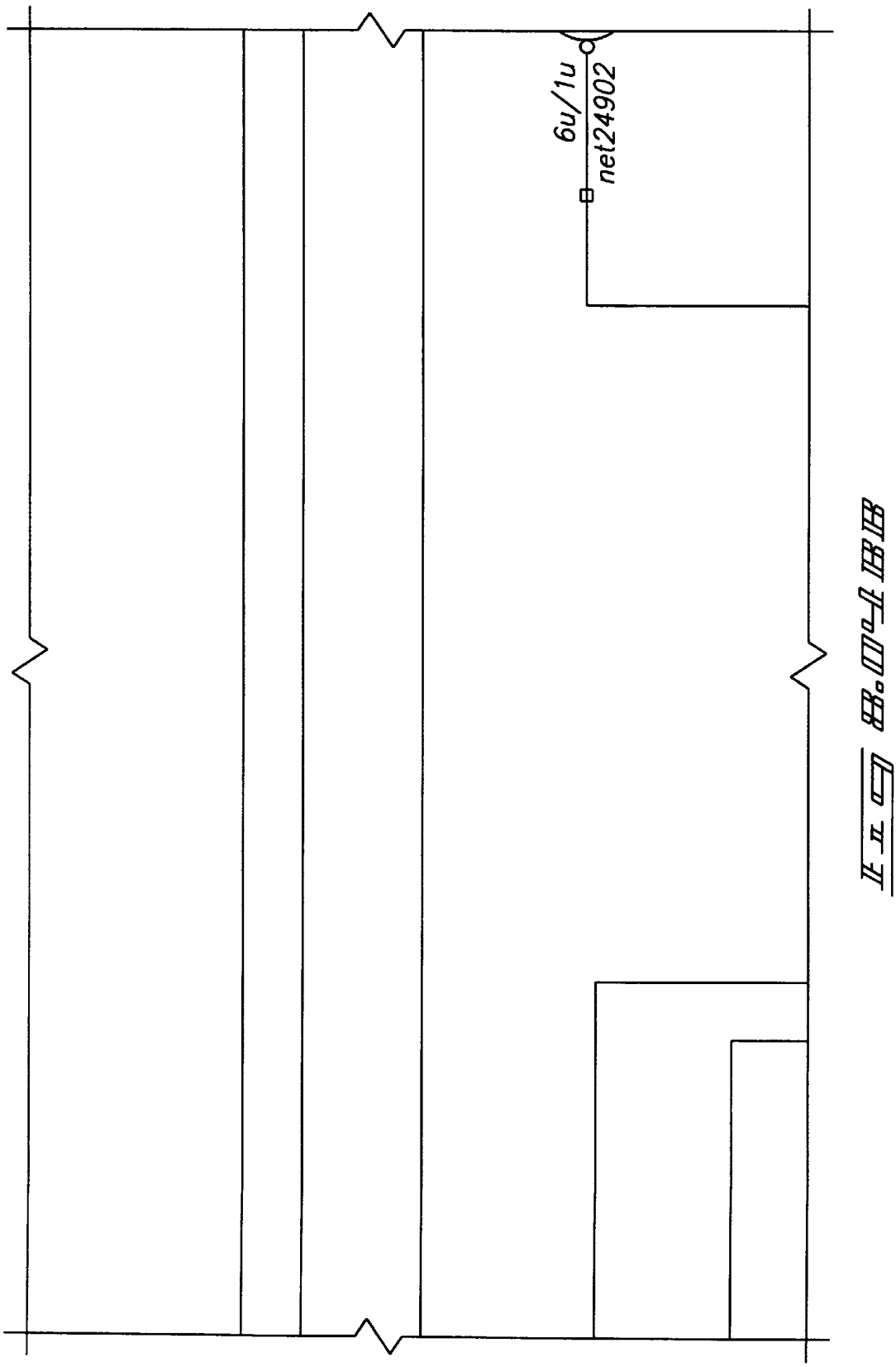


FIG 88.00AAB

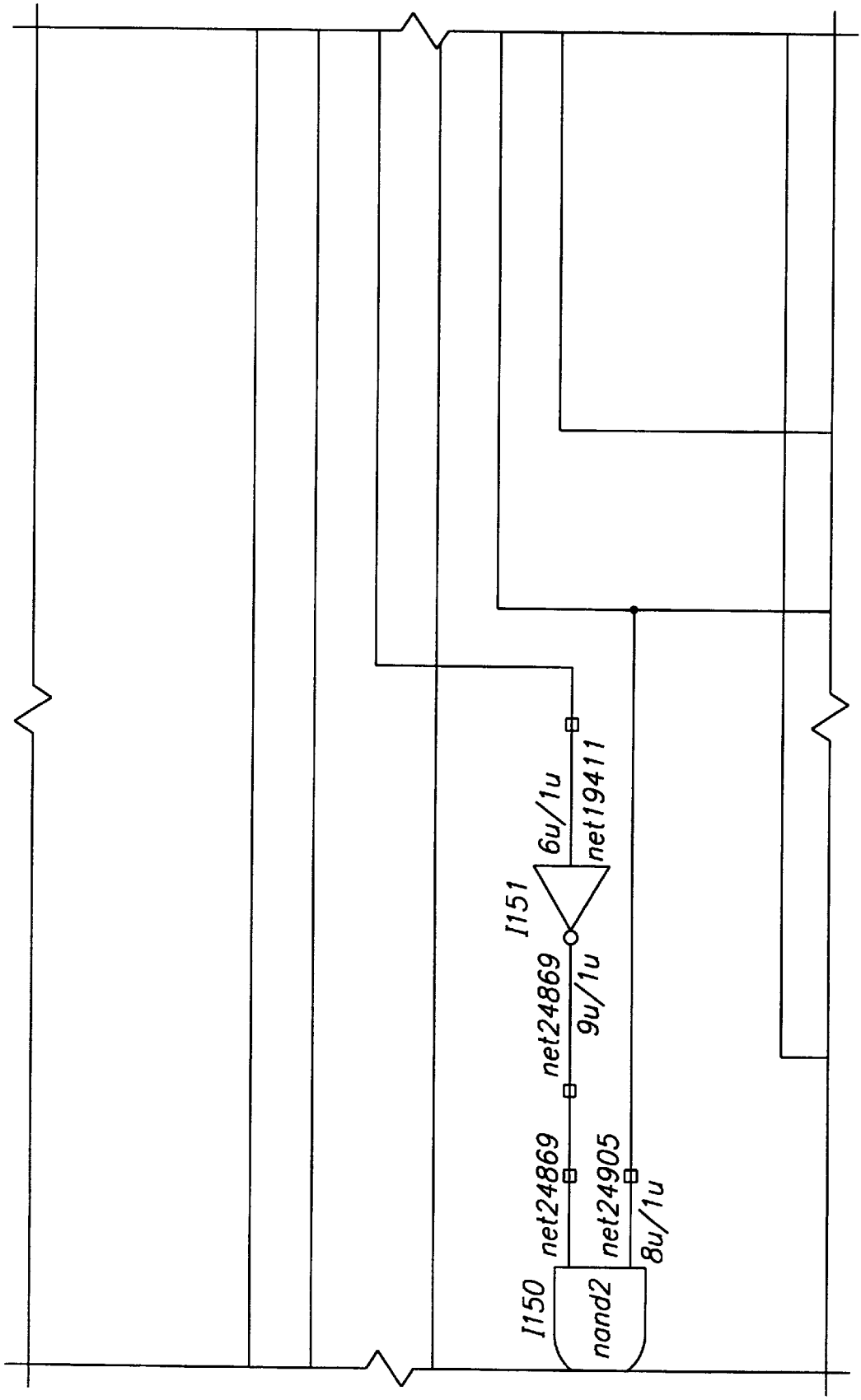

I151
6u/1u
net19411
net24869
9u/1u
net24869
net24905
8u/1u
I150
nond2

FIG 898

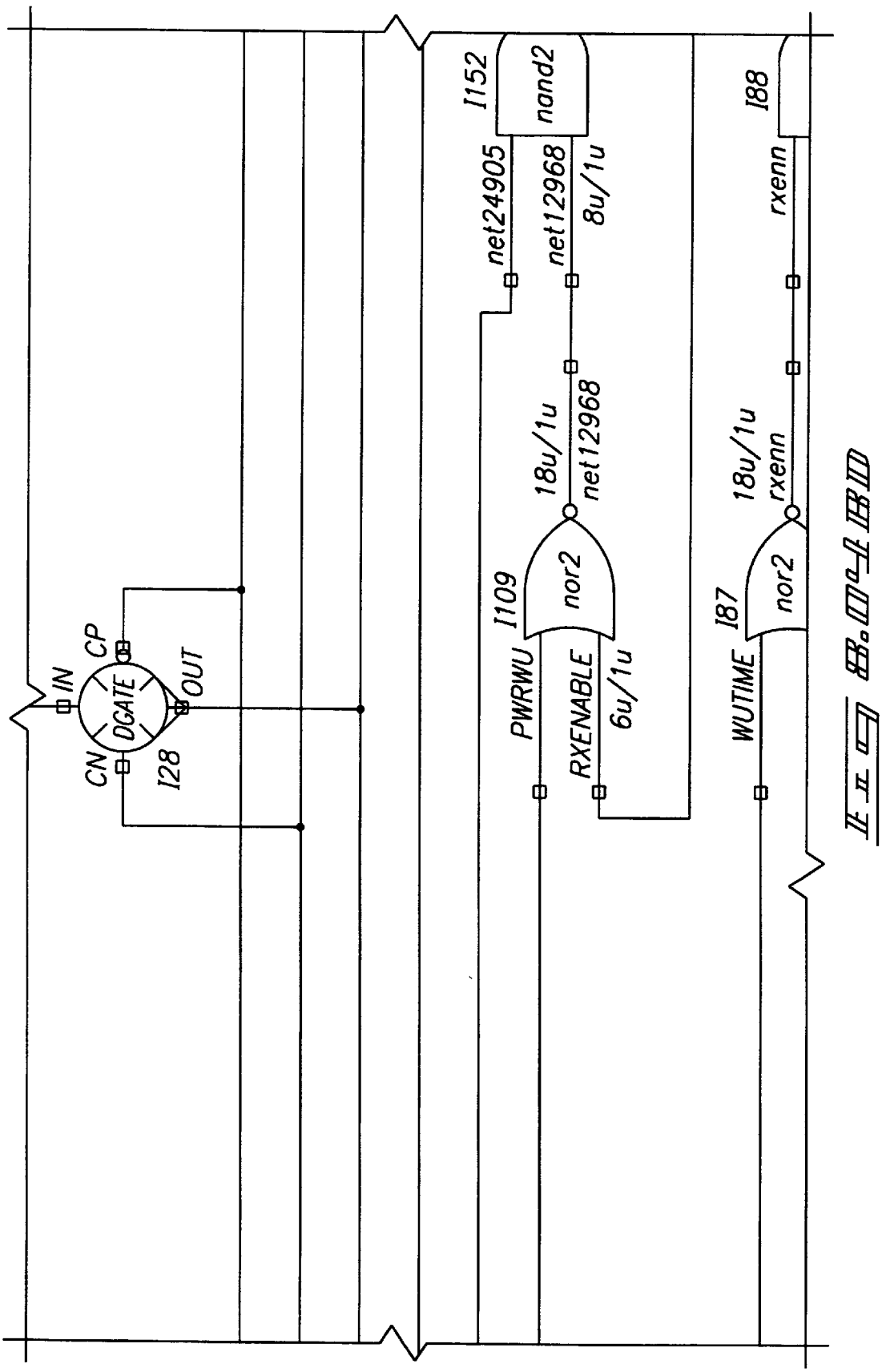

I152
nand2
net24905
net12968
8u/1u
I88
rxenn
18u/1u
net12968
I109
nor2
PWRWU
RXENABLE
6u/1u
18u/1u
rxenn
I87
nor2
WUTIME
IN
CP
DGATE
OUT
CN
I28

FIG. 88.00

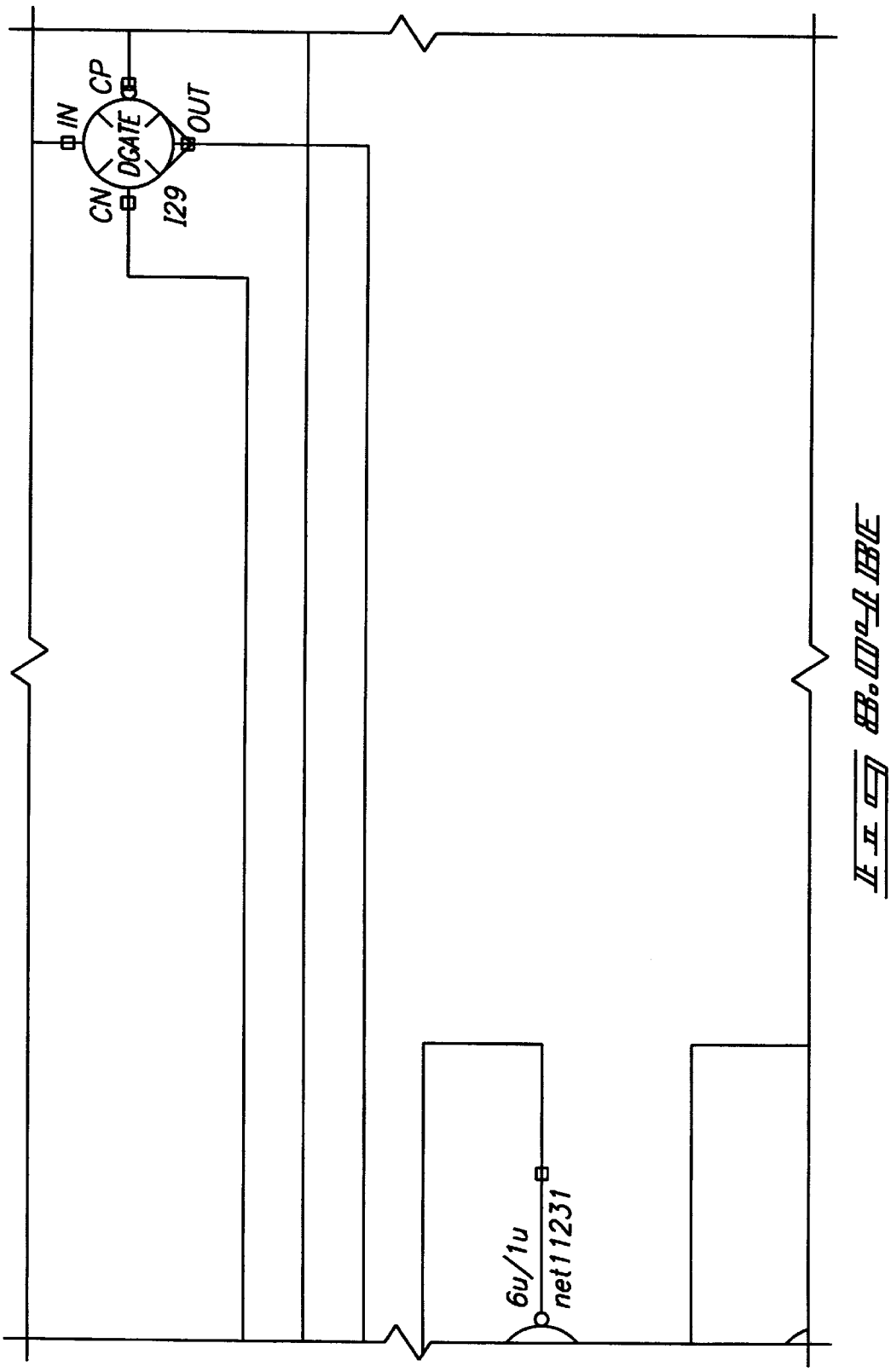


FIG 88A

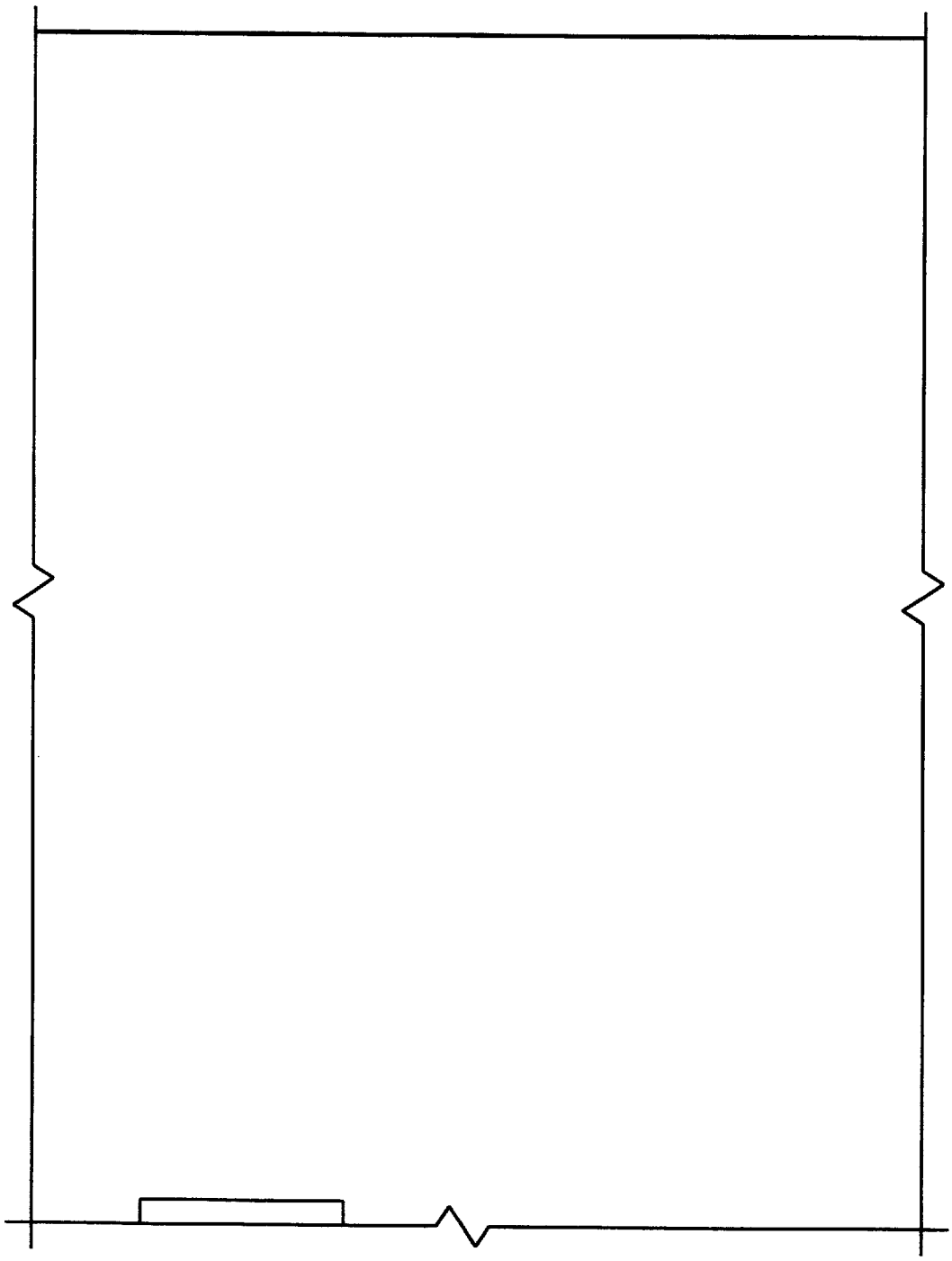


FIG. 88,001A-1B/F

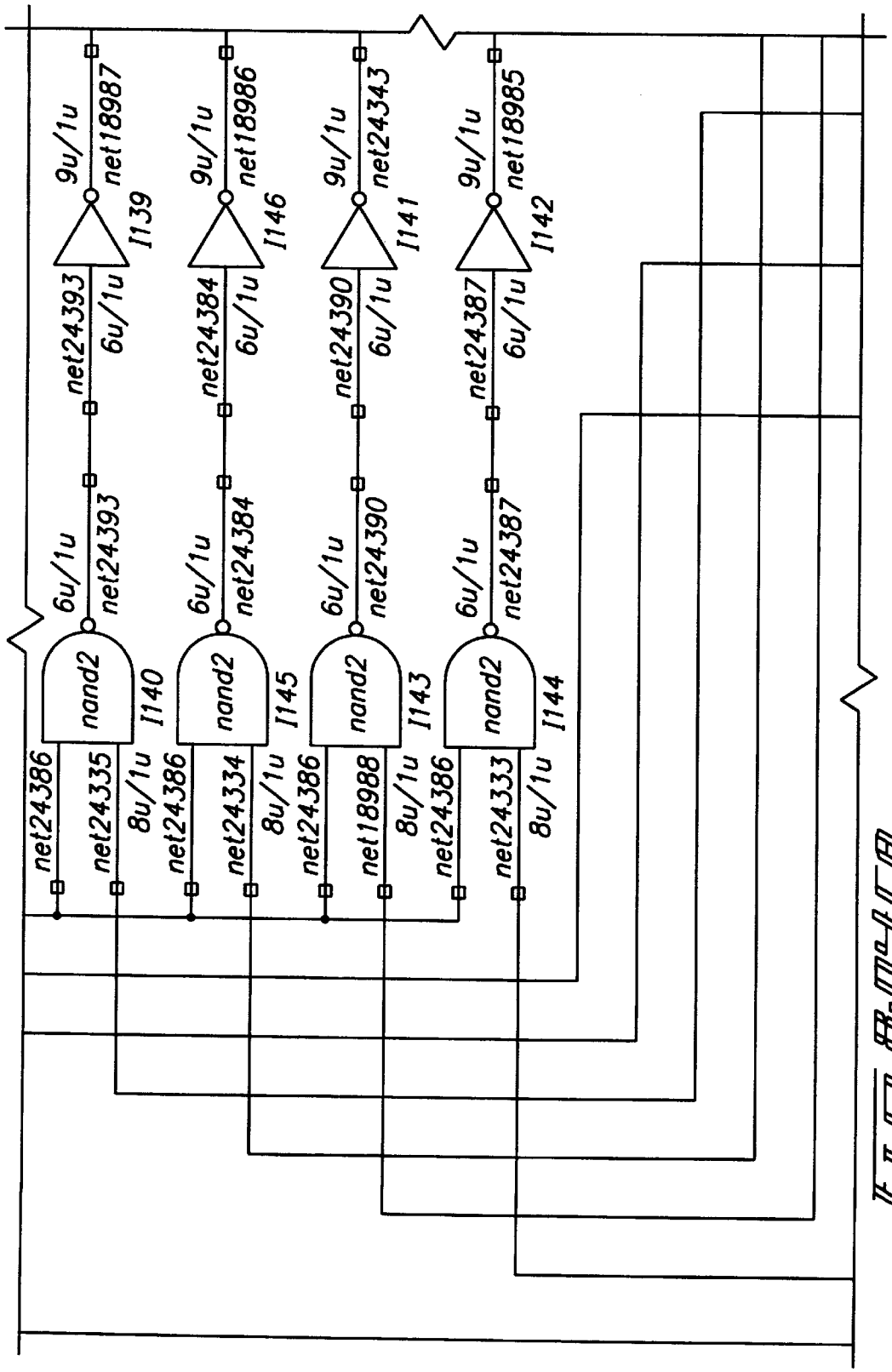
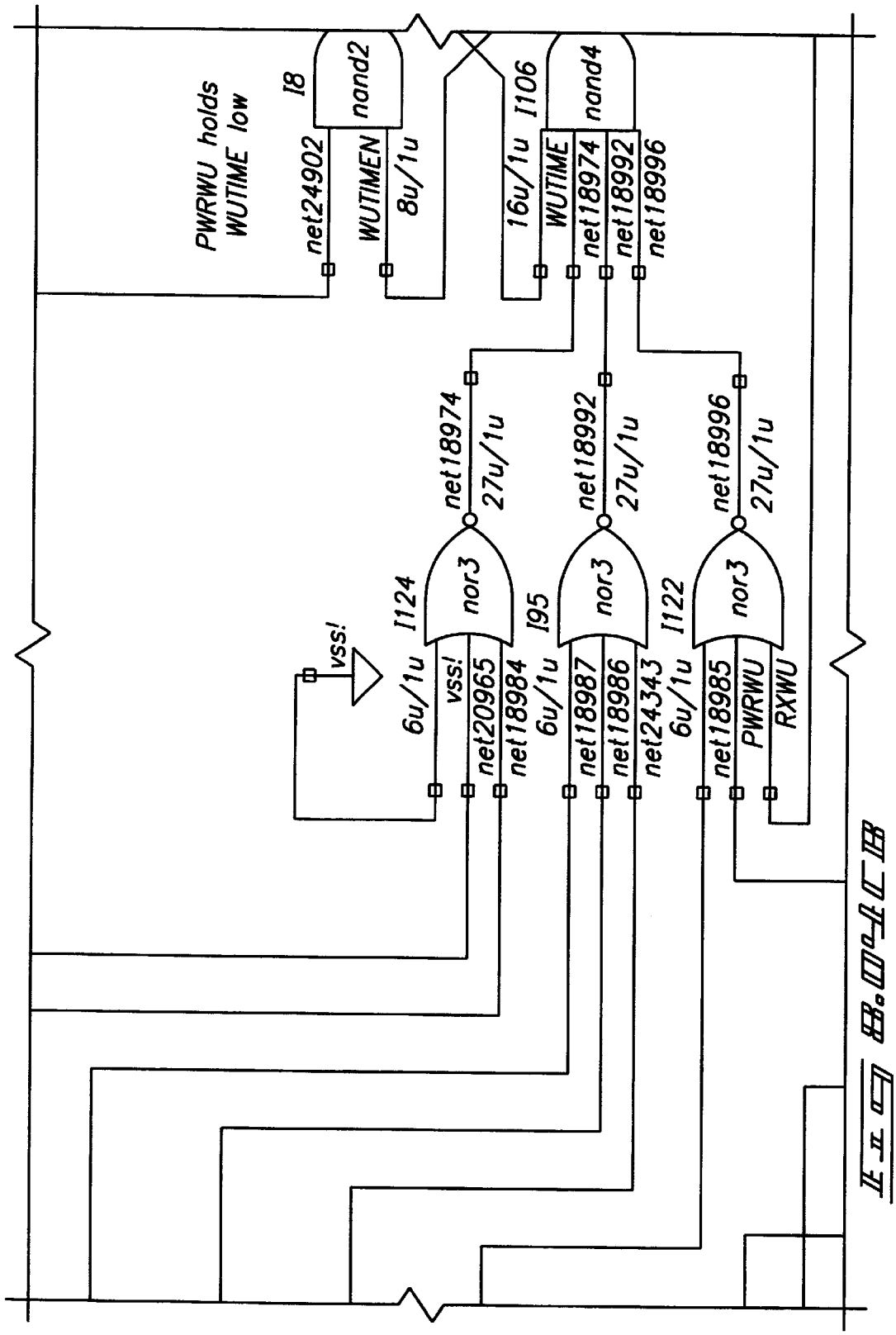

9u/1u
net18987
I139
net24393
6u/1u
6u/1u
net24393
nand2
I140
net24386
net24335
8u/1u
9u/1u
net18986
I146
net24384
6u/1u
6u/1u
net24384
nand2
I145
net24386
net24334
8u/1u
9u/1u
net24343
I141
net24390
6u/1u
6u/1u
net24390
nand2
I143
net24386
net18988
8u/1u
9u/1u
net18985
I142
net24387
6u/1u
6u/1u
net24387
nand2
I144
net24386
net24333
8u/1u

FIG 88.0001A


PWRWU holds
WUTIME low
I8
nand2
net24902
WUTIMEN
8u/1u
I106
nand4
16u/1u
WUTIME
net18974
net18992
net18996
net18974
27u/1u
net18992
27u/1u
net18996
27u/1u
I124
nor3
I95
nor3
I122
nor3
vss!
6u/1u
vss!
net20965
net18984
6u/1u
net18987
net18986
net24343
6u/1u
net18985
PWRWU
RXWU

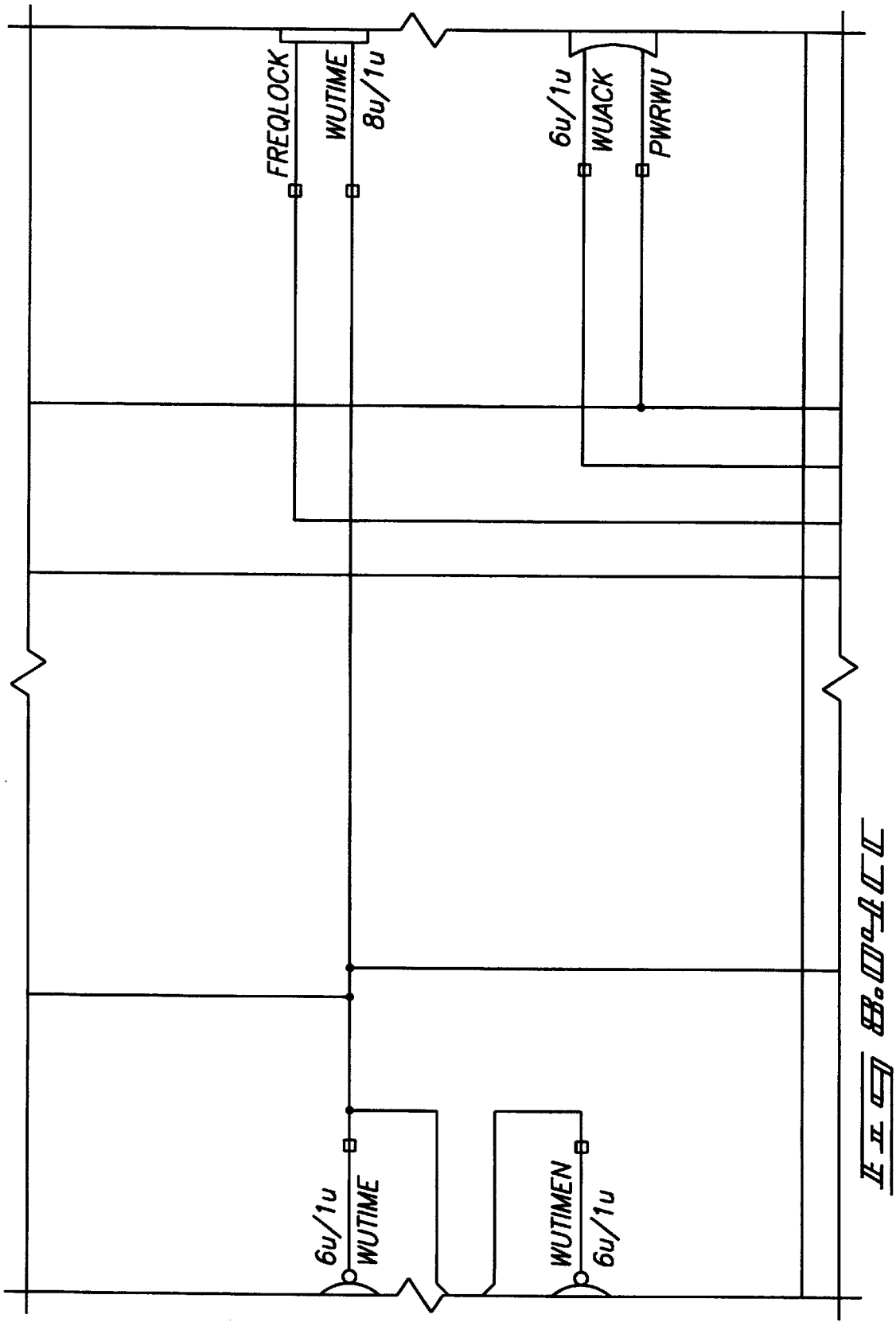
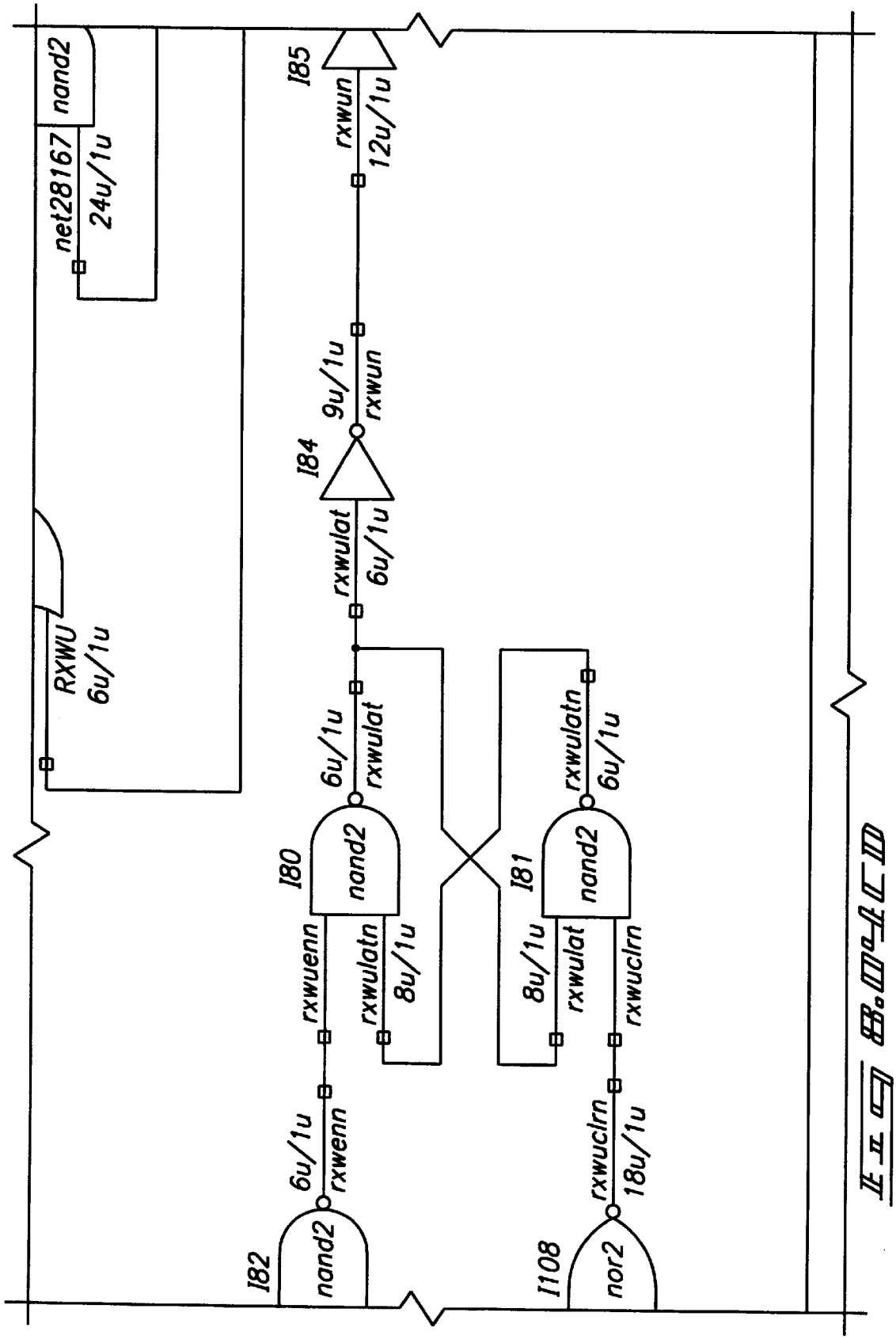
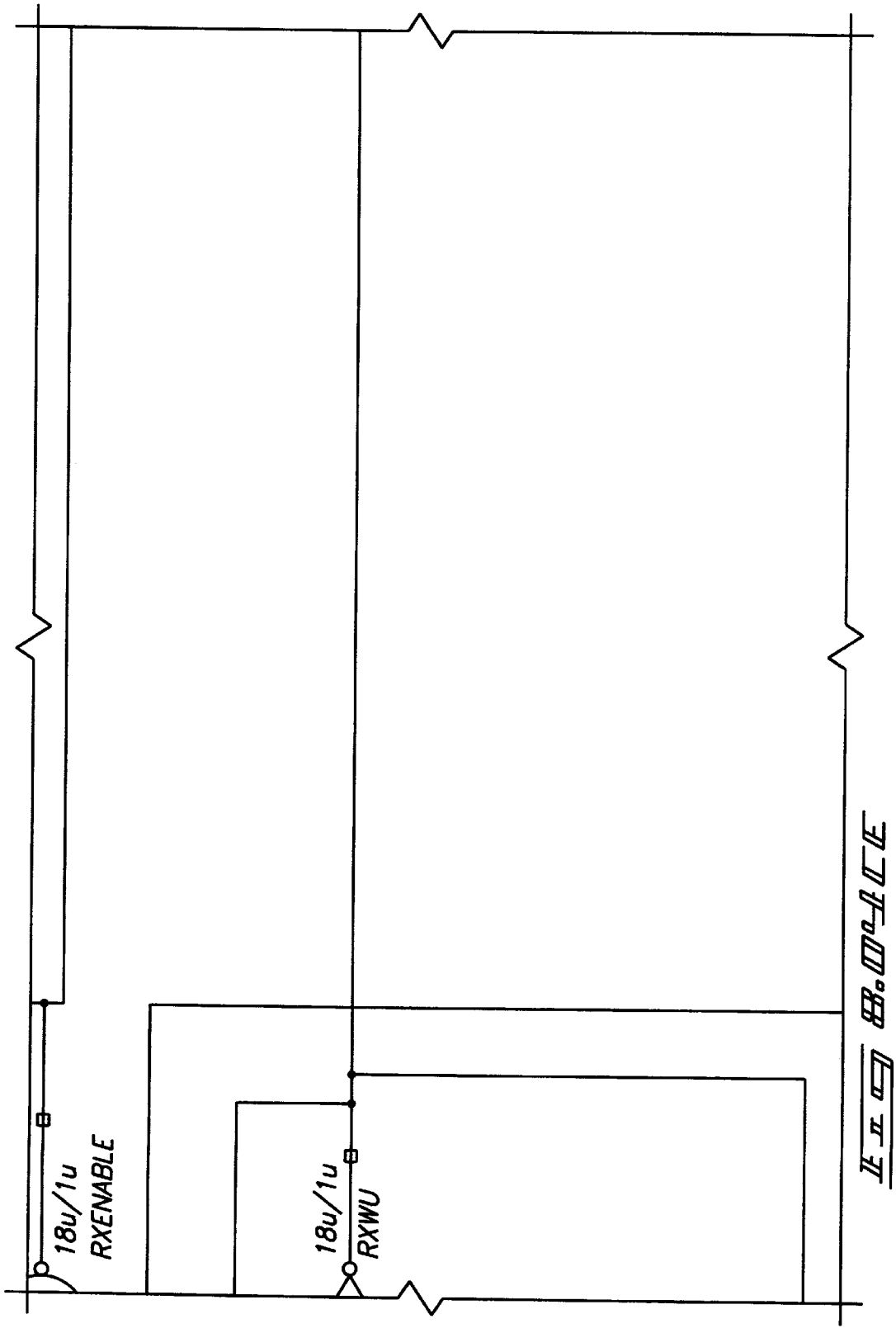

FREQLOCK
WUTIME
8u/1u
6u/1u
WUACK
PWRWU
6u/1u
WUTIME
WUTIMEN
6u/1u

FIG 88.0044


I85
rxwun
12u/1u
nand2
net28167
24u/1u
9u/1u
rxwun
I84
rxwulat
6u/1u
RXWU
6u/1u
6u/1u
rxwulat
6u/1u
rxwulatn
I80
nand2
I81
nand2
rxwuenn
rxwulatn
8u/1u
8u/1u
rxwulat
rxwuclrn
6u/1u
rxwenn
rxwuclrn
18u/1u
I82
nand2
I108
nor2


18u/1u
RXENABLE
18u/1u
RXWU
FIG. 8,047E

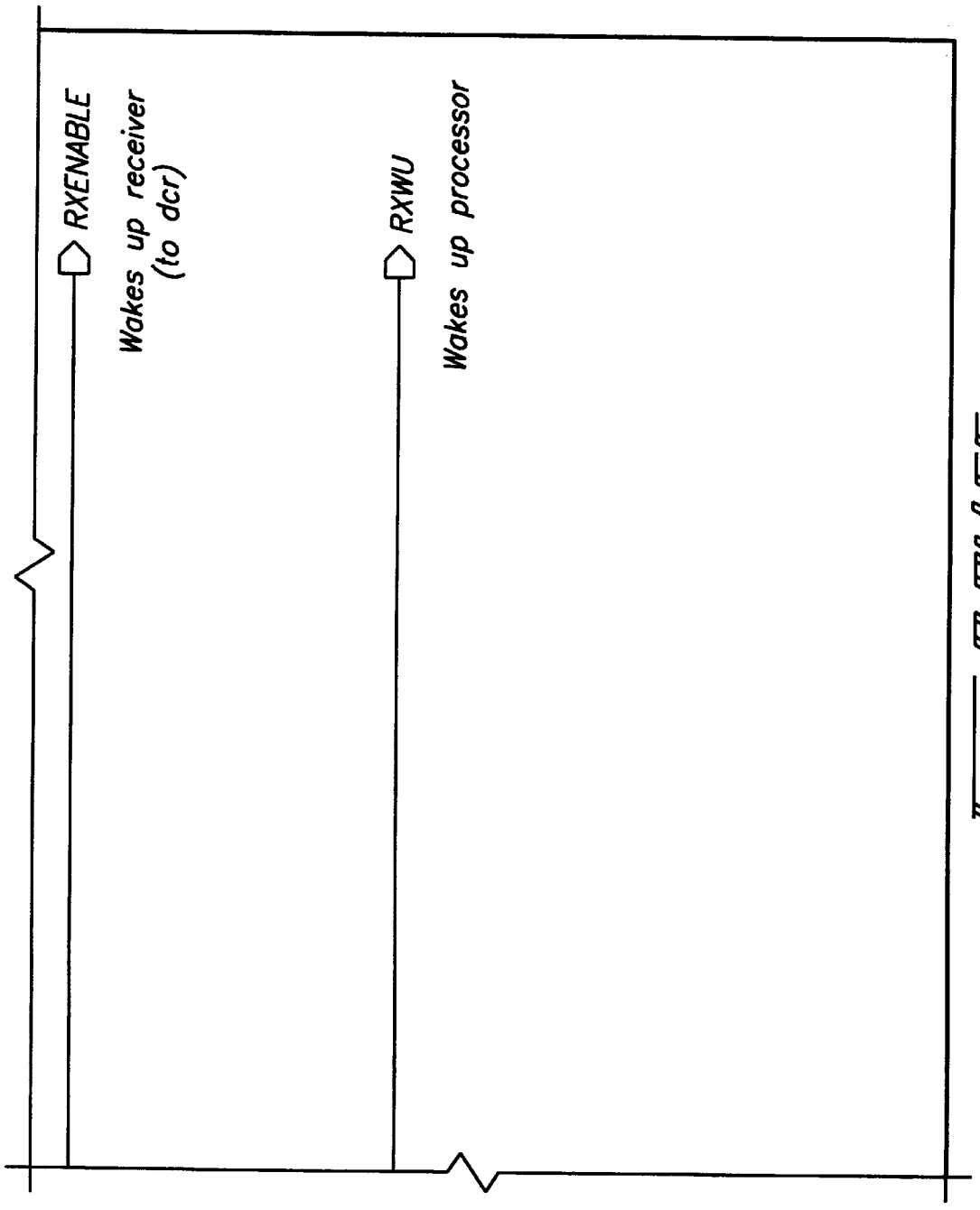
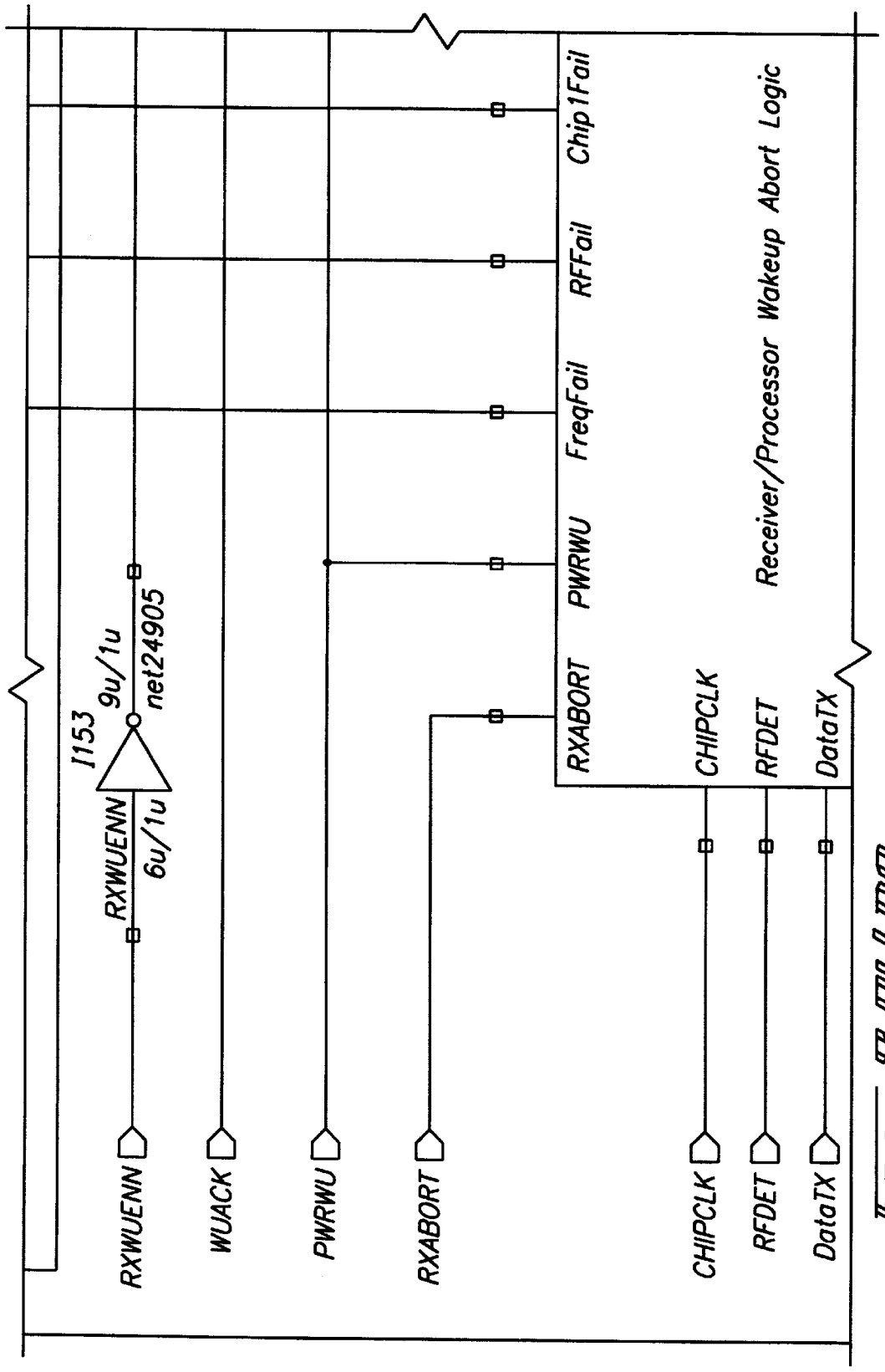


FIG 88.00FF


I153
9u/1u
net24905
RXWUENN
6u/1u
RXWUENN
WUACK
PWRWU
RXABORT
RXABORT
PWRWU
FreqFail
RFFail
Chip1Fail
CHIPCLK
RFDET
DataTX
Receiver/Processor Wakeup Abort Logic
CHIPCLK
RFDET
DataTX

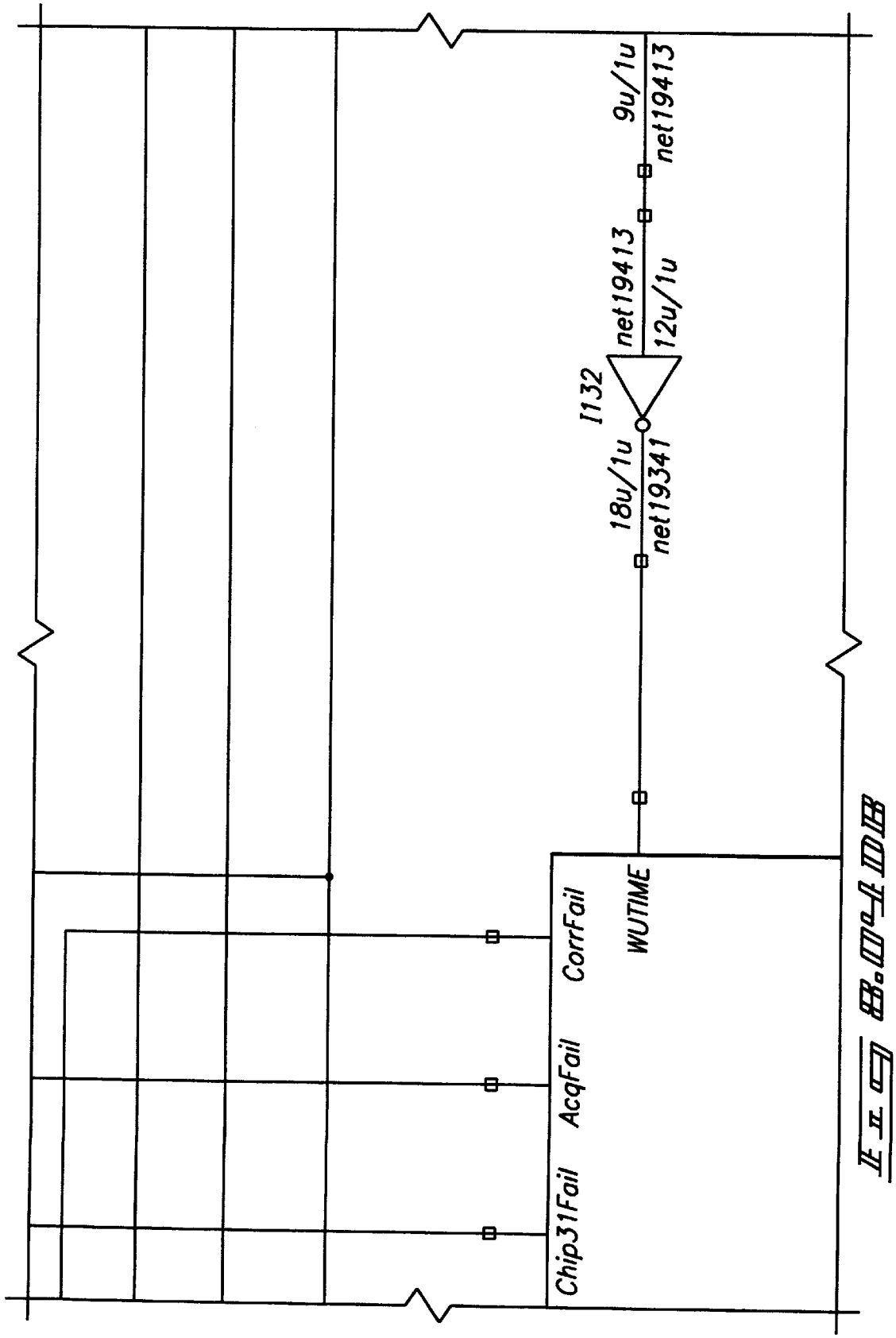
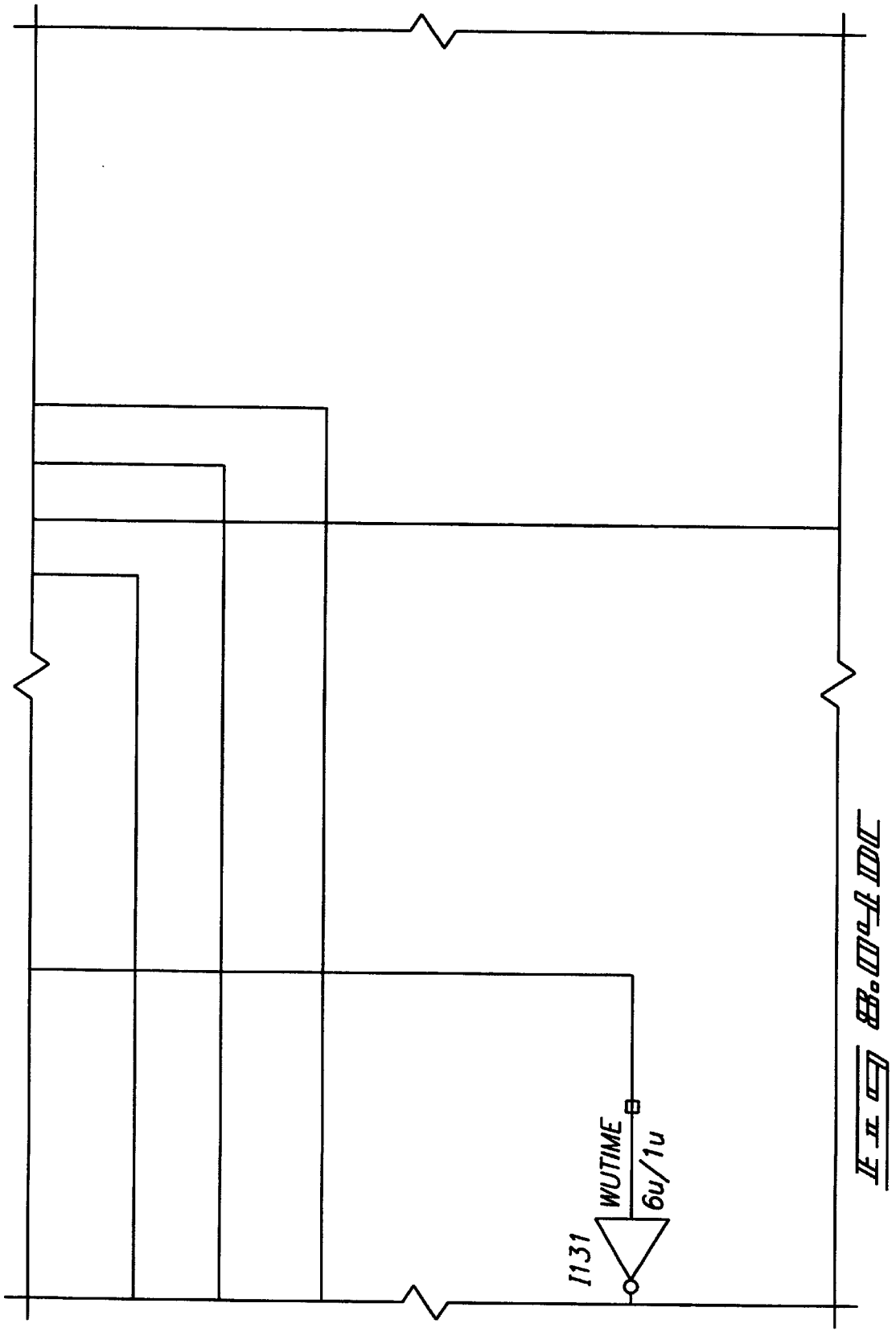

9u/1u
net19413
net19413
12u/1u
I132
18u/1u
net19341
WUTIME
CorrFail
AcqFail
Chip31Fail

FIG. 1409


WUTIME
6u/1u
I131

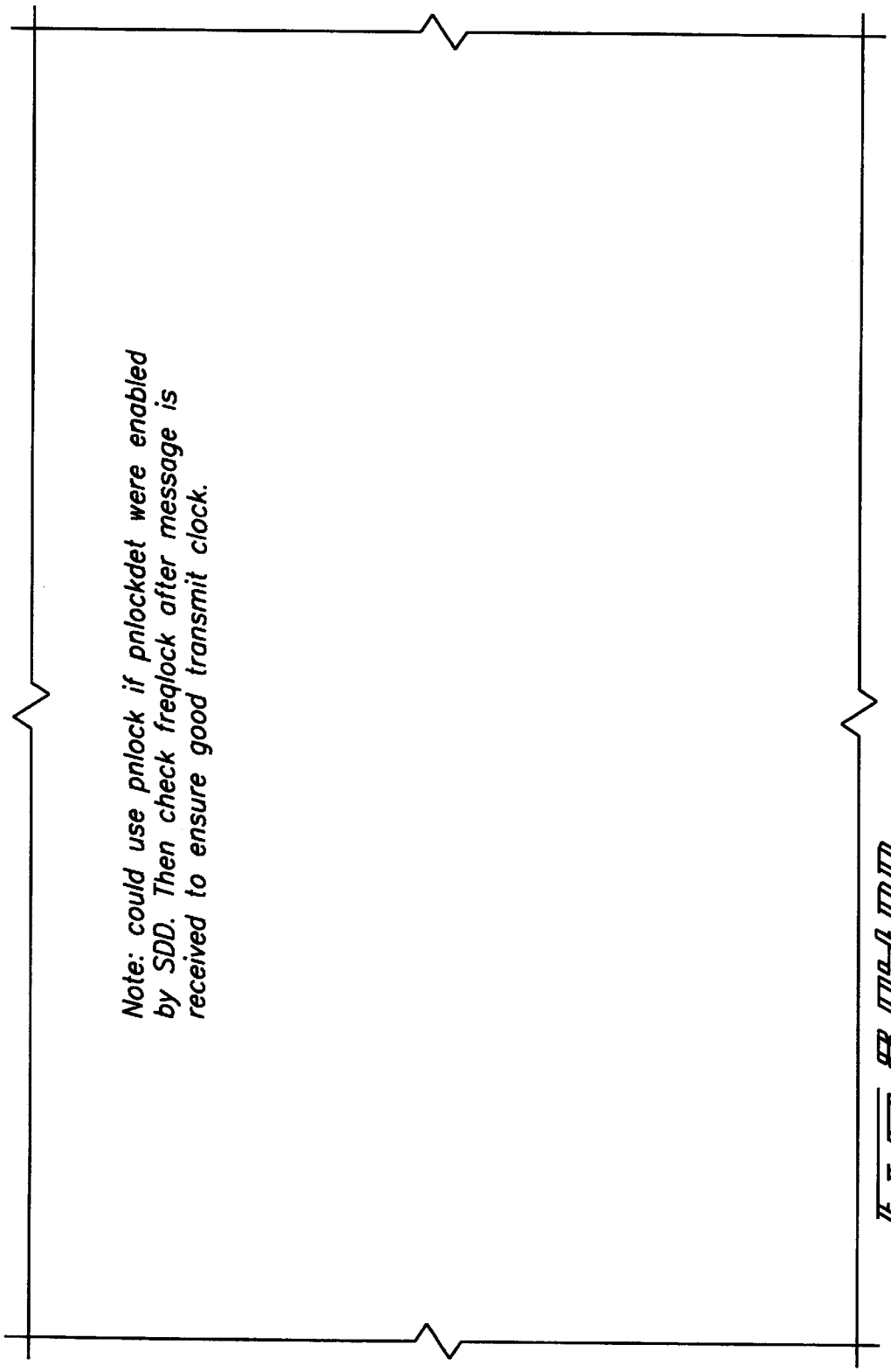


FIG. 88.00-88.00

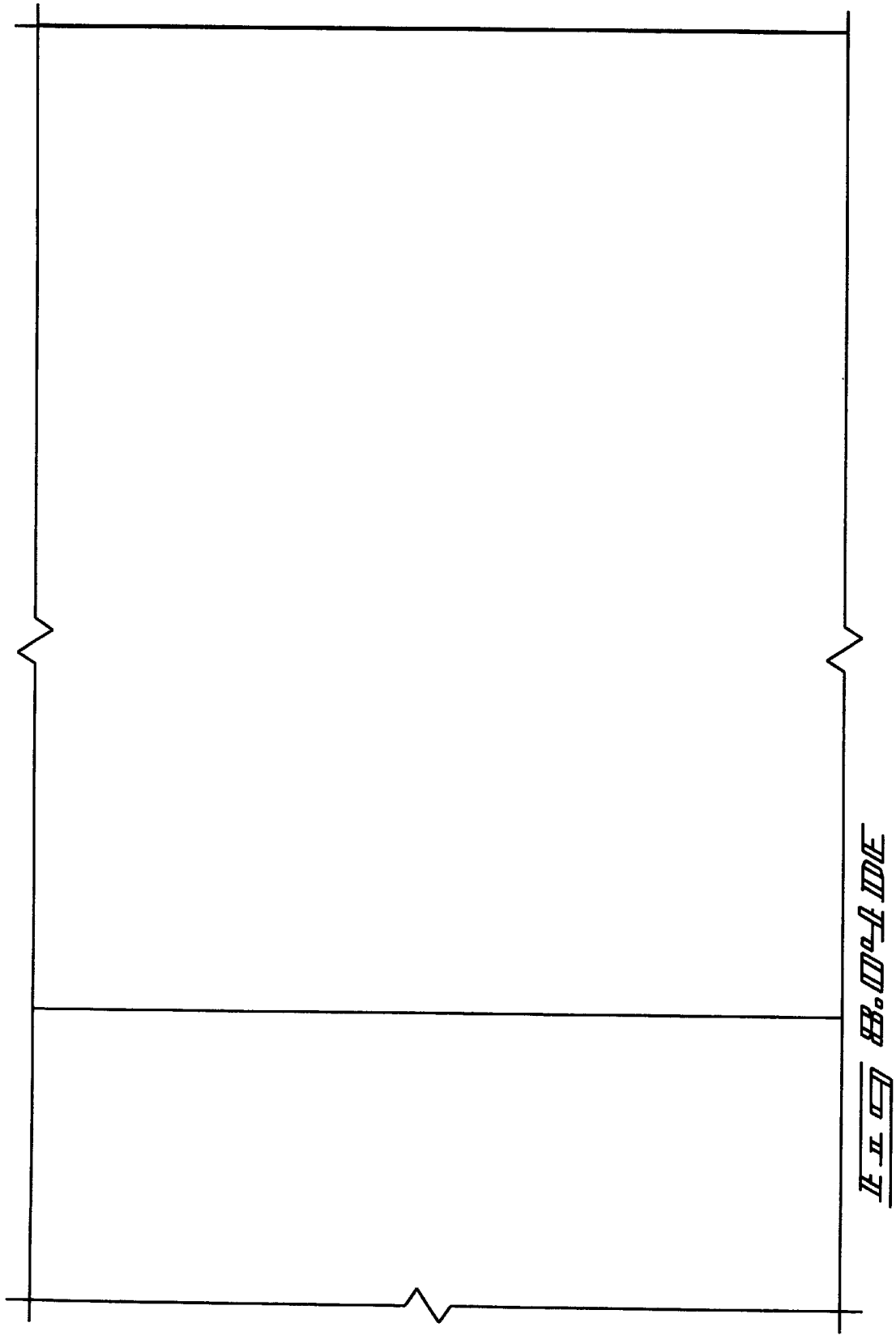


FIG. 84.04E

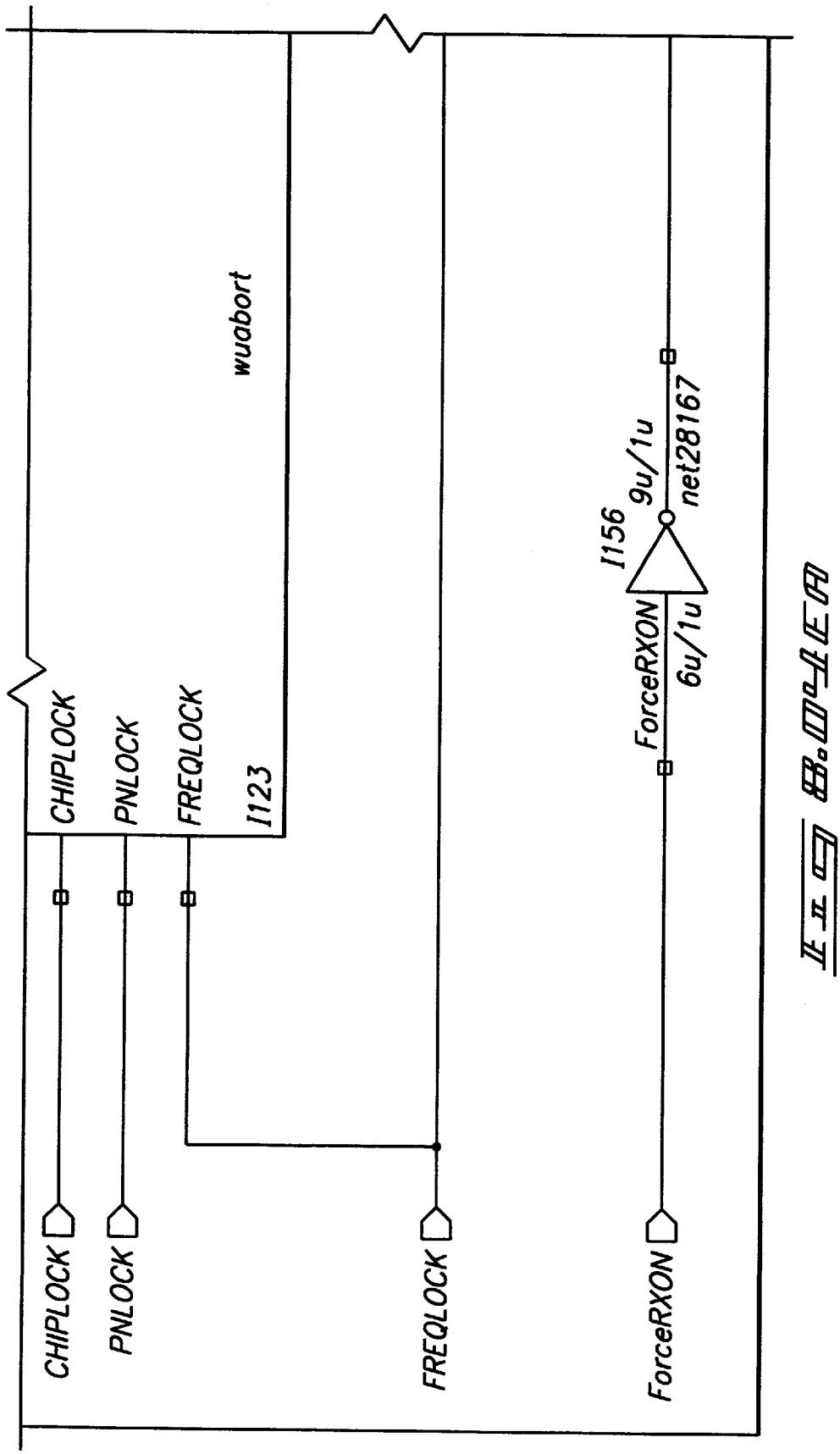
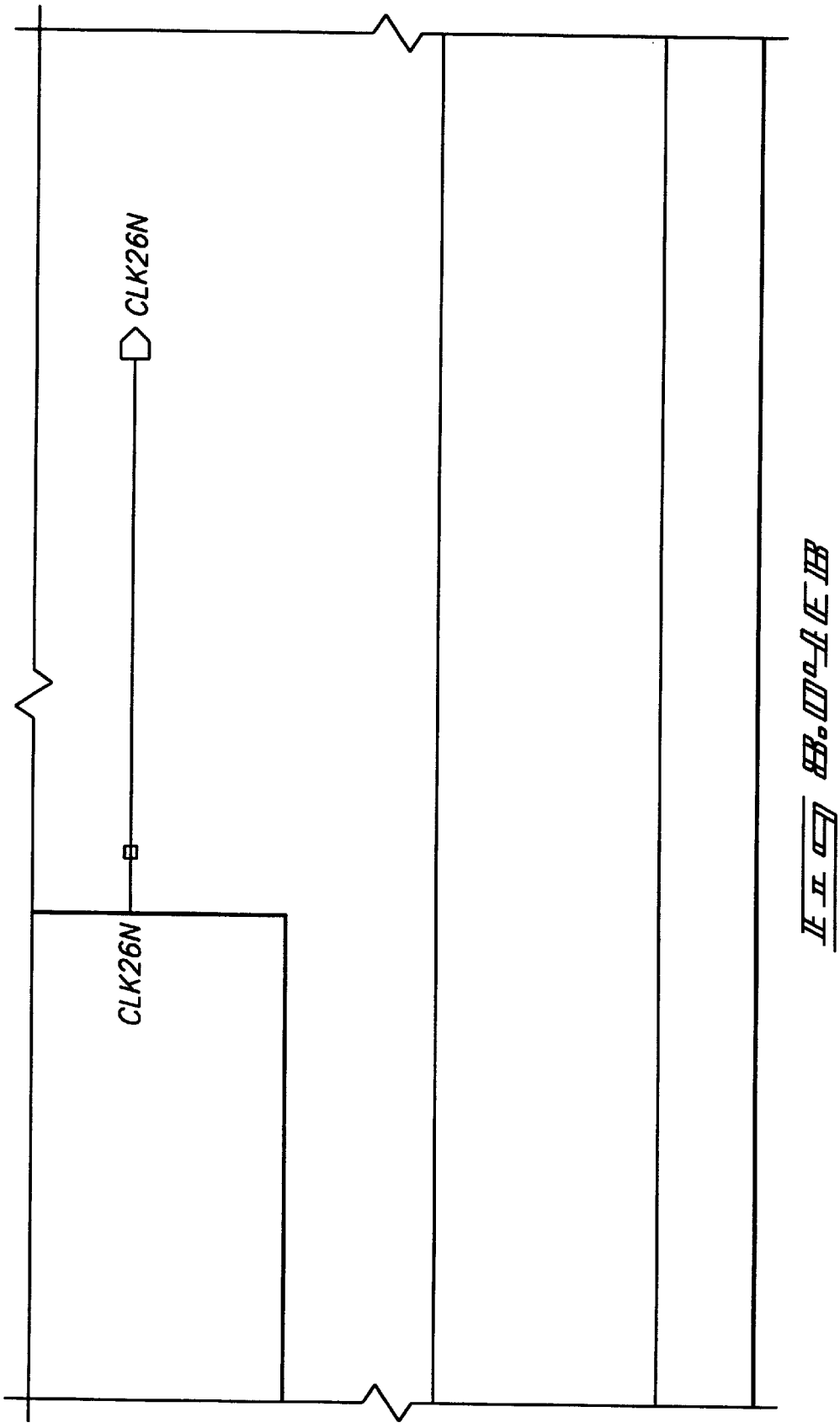

wuabort
CHIPLOCK
PNLOCK
FREQLOCK
I123
I156
9u/1u
net28167
ForceRXON
6u/1u
CHIPLOCK
PNLOCK
FREQLOCK
ForceRXON

FIG. 88.0144


CLK26N
CLK26N
FIG. 88.00

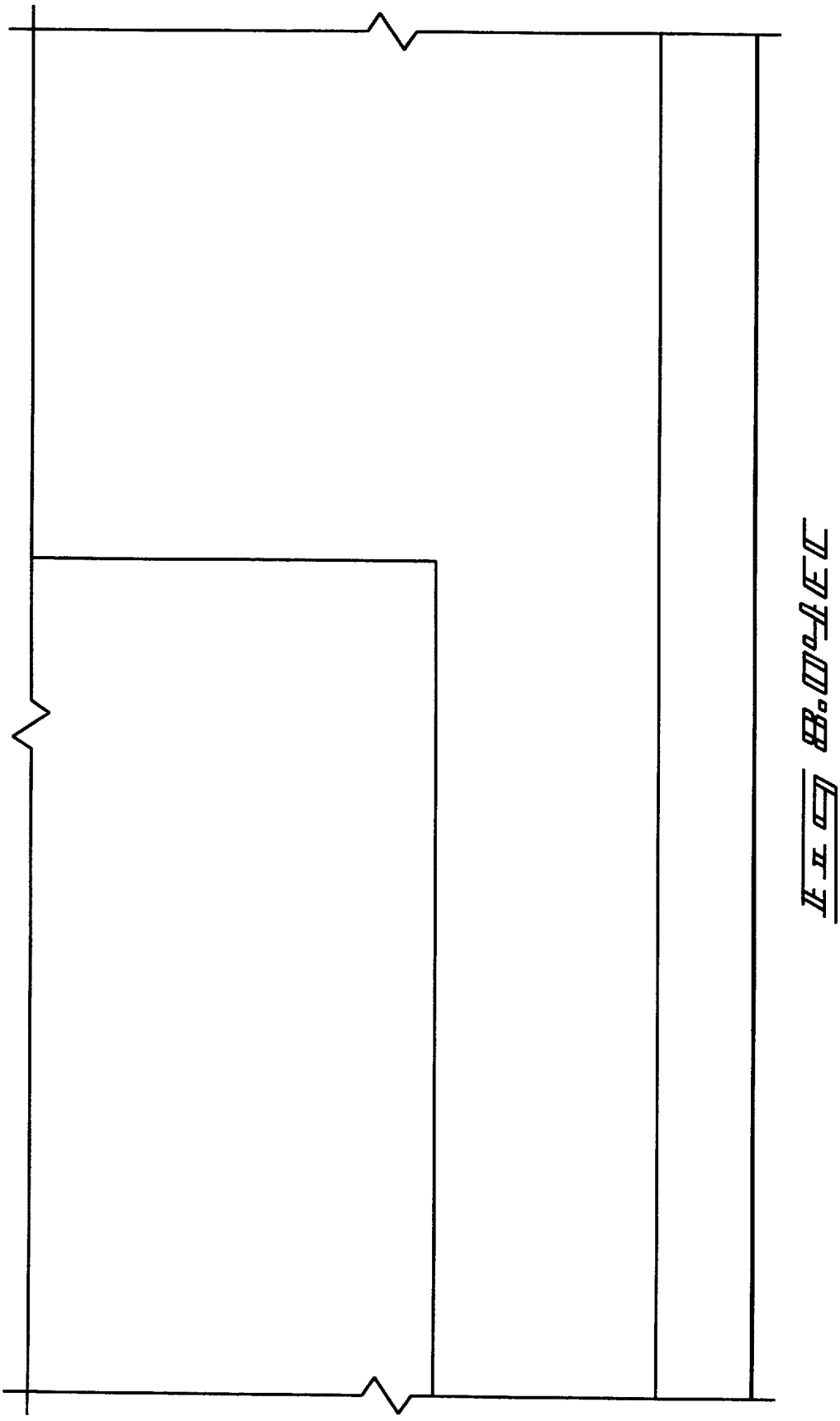


FIG 8.00

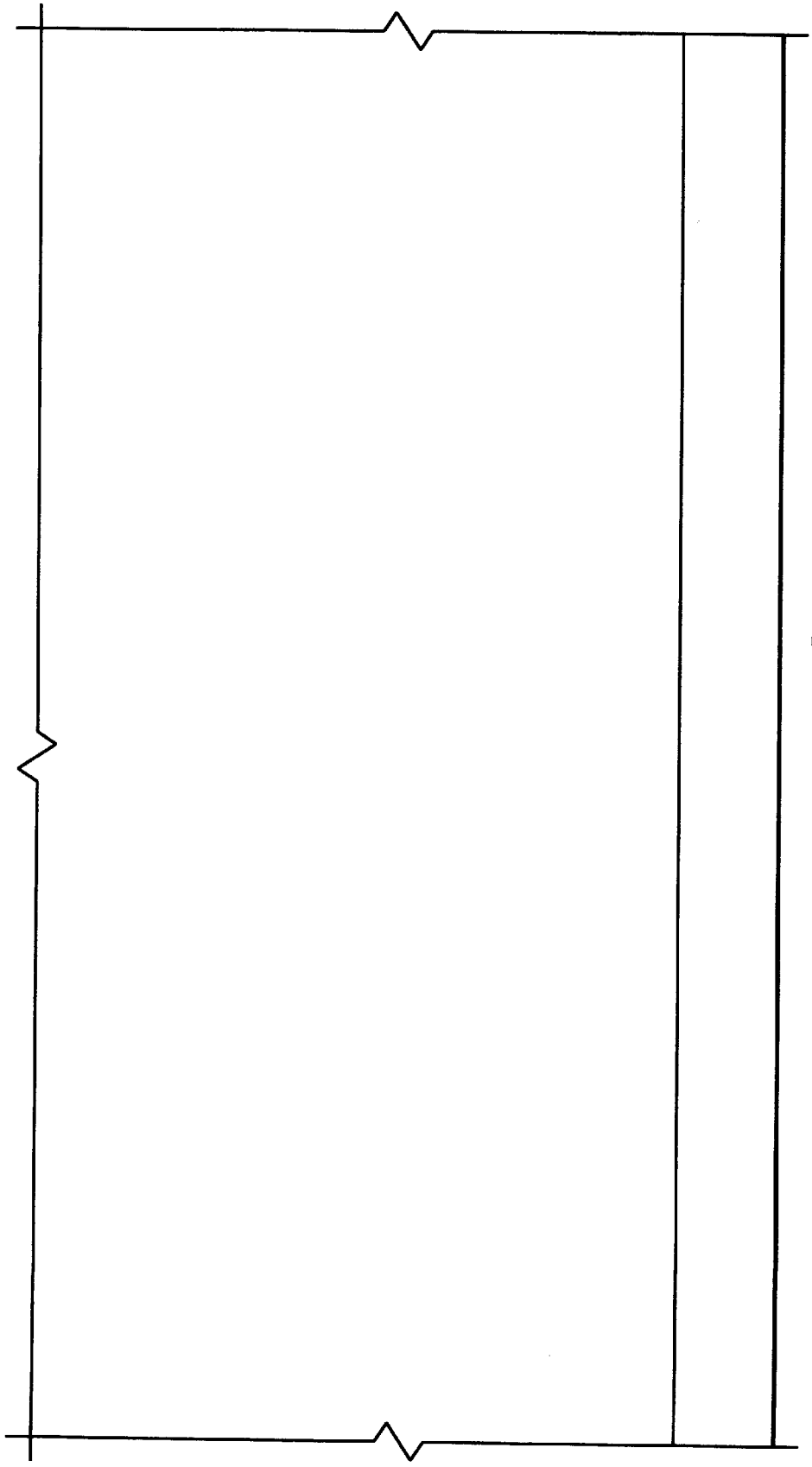


FIG 88.0416

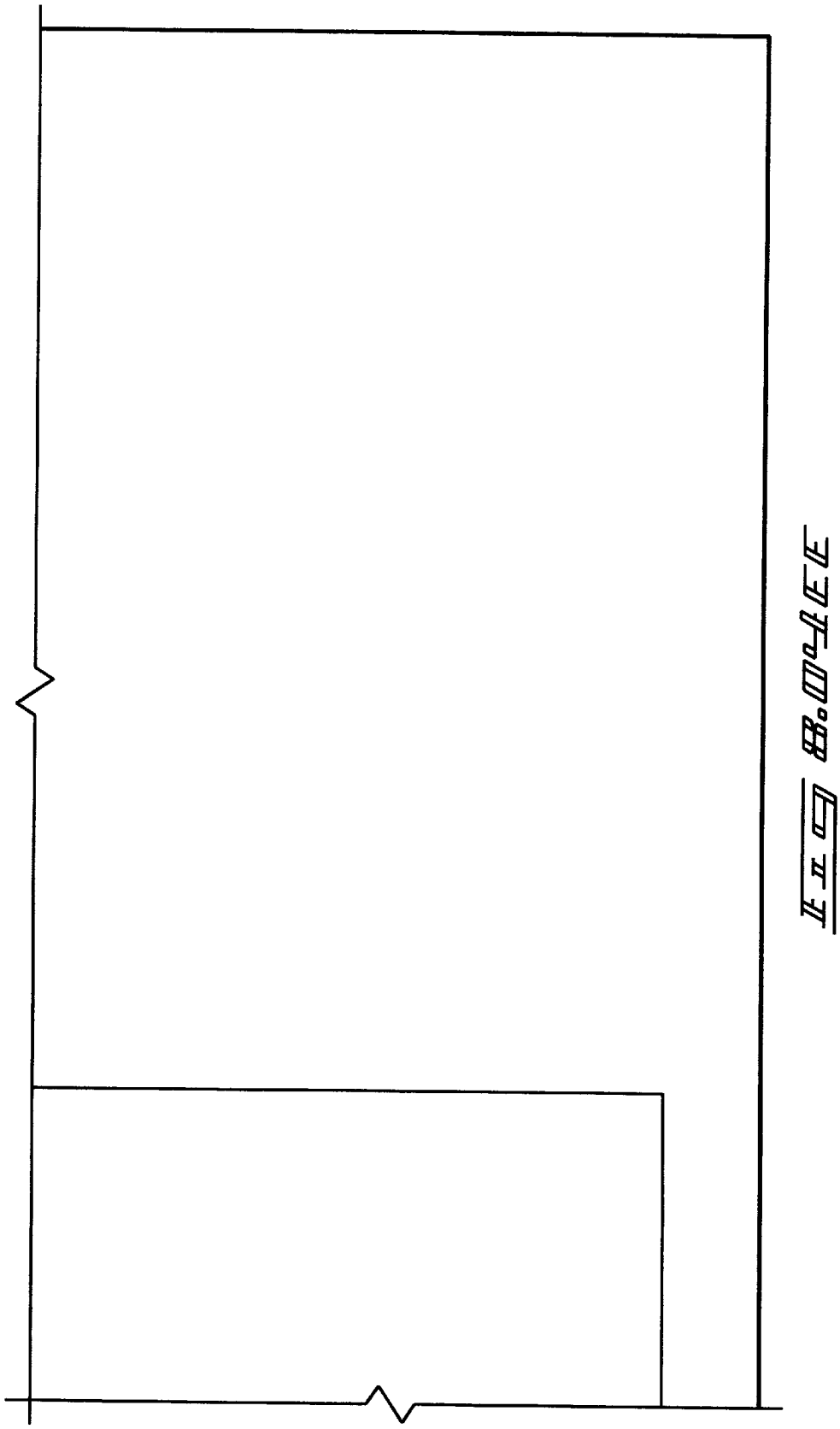


FIG. 88.04E

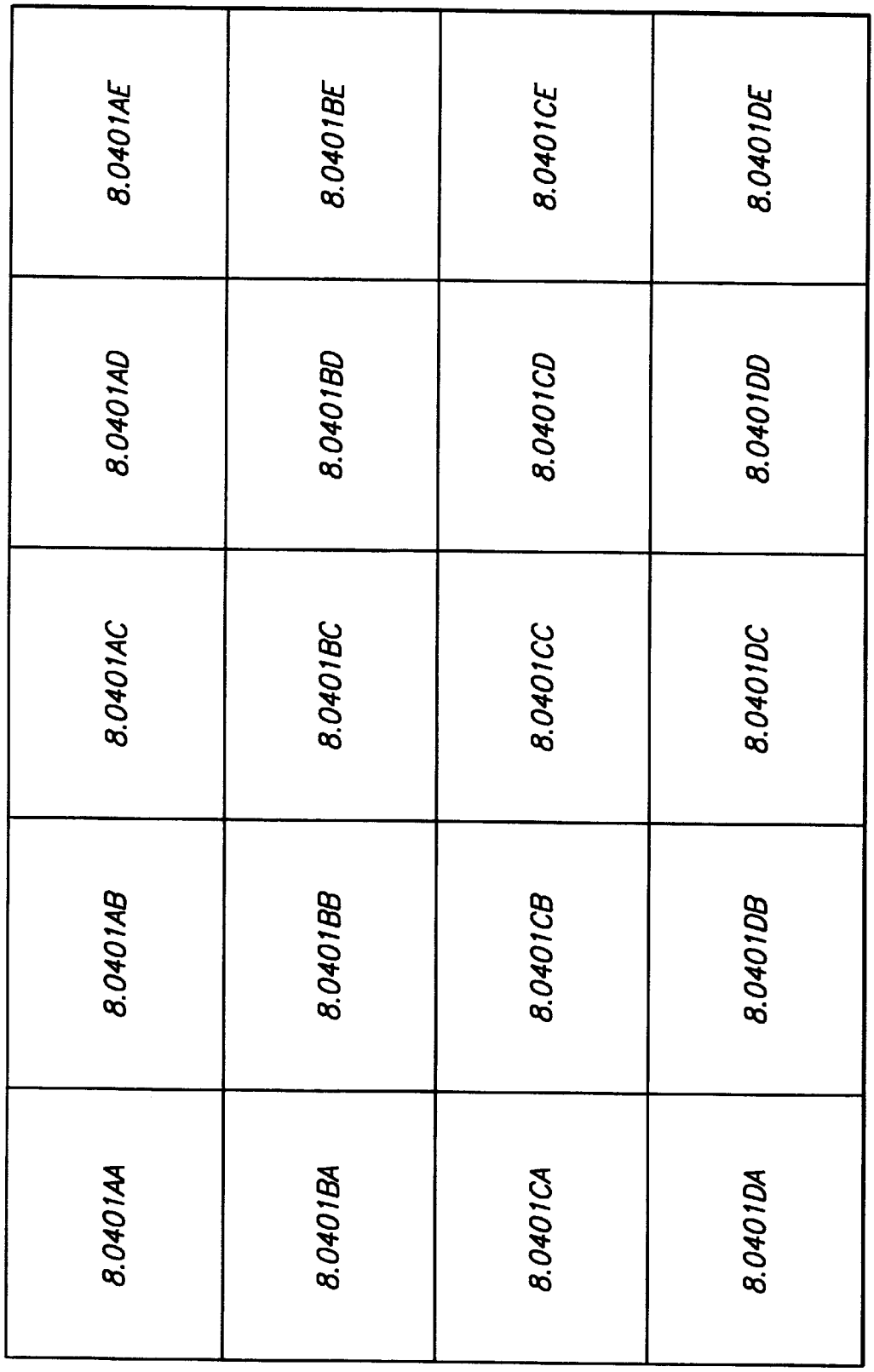
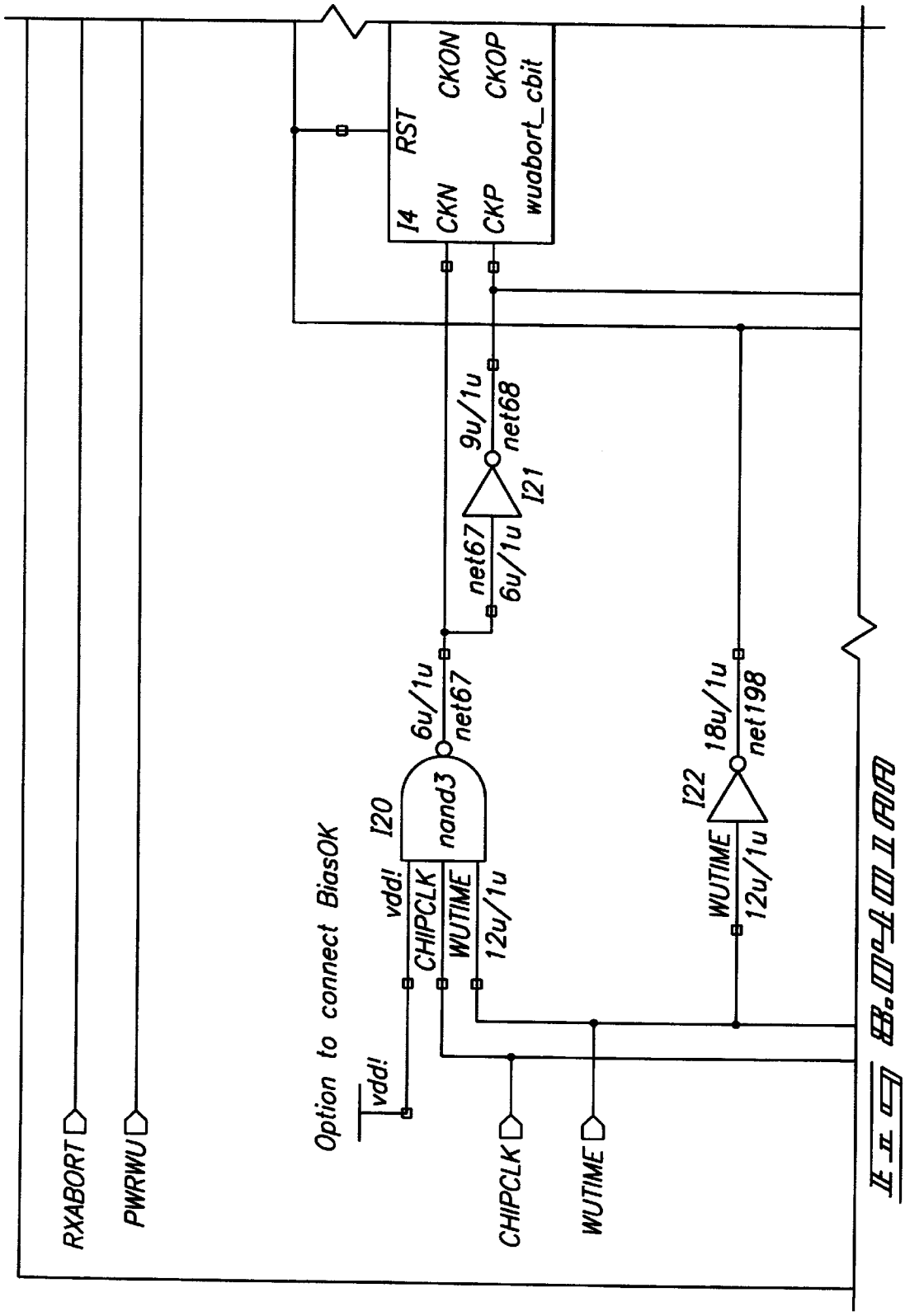
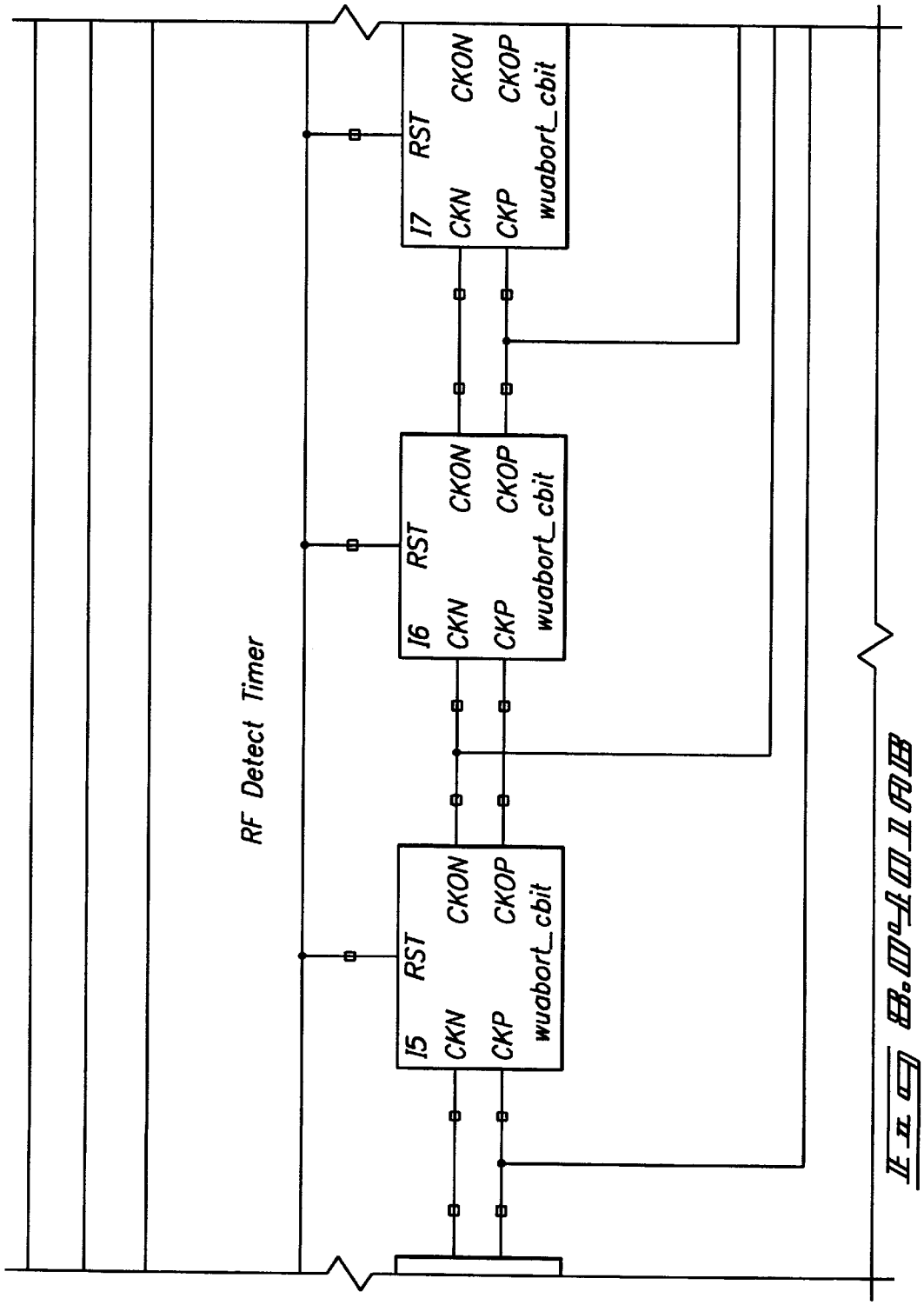
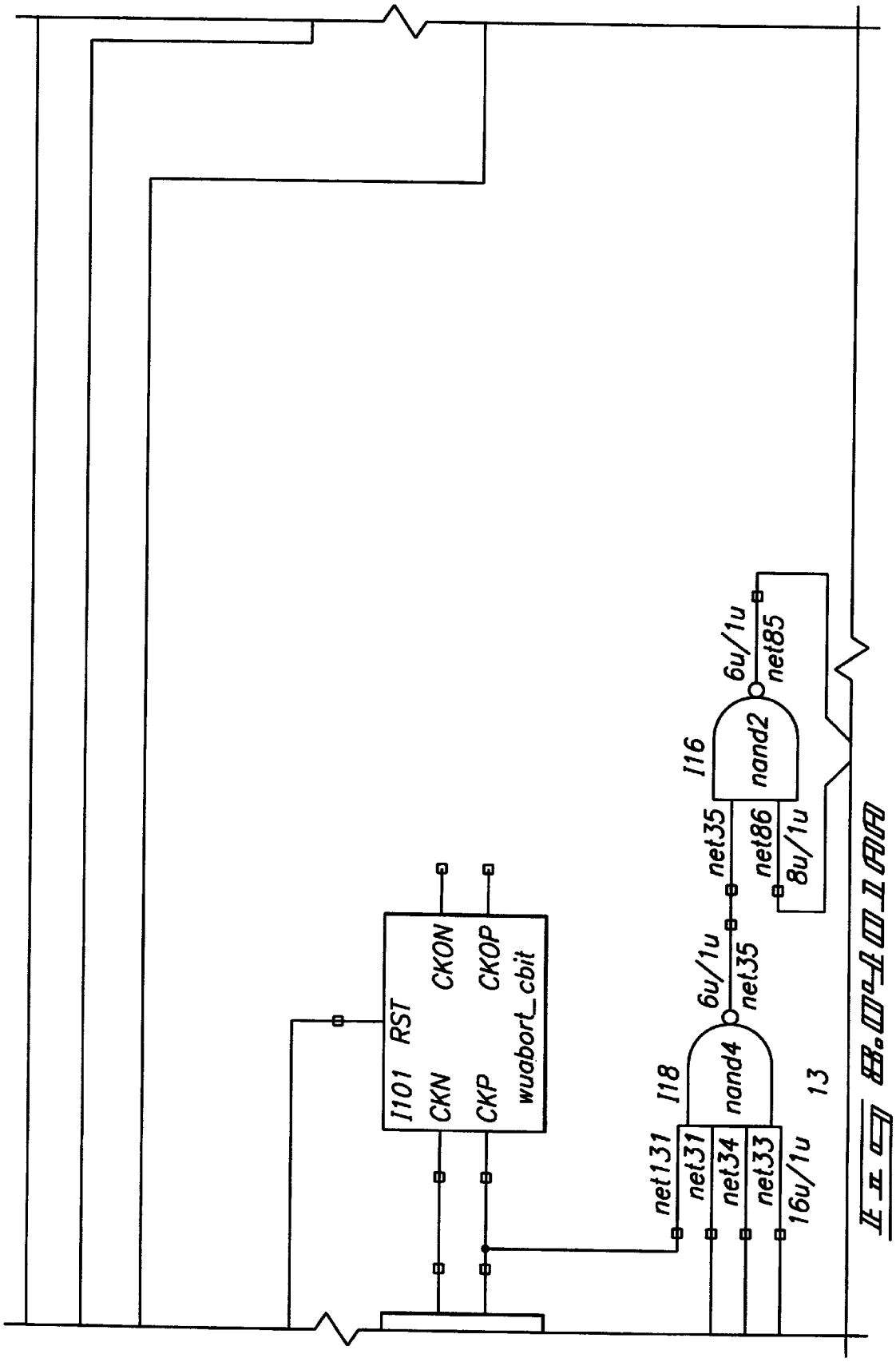

8.0401AA
8.0401AB
8.0401AC
8.0401AD
8.0401AE
8.0401BA
8.0401BB
8.0401BC
8.0401BD
8.0401BE
8.0401CA
8.0401CB
8.0401CC
8.0401CD
8.0401CE
8.0401DA
8.0401DB
8.0401DC
8.0401DD
8.0401DE

FIG. 8.0401


RXABORT
PWRWU
Option to connect BiasOK
vdd!
I20
nand3
vdd!
CHIPCLK
WUTIME
12u/1u
6u/1u
net67
6u/1u
net67
9u/1u
net68
I21
I4
RST
CKN
CKP
CKON
CKOP
wuabort_cbit
I22
18u/1u
net198
WUTIME
12u/1u
CHIPCLK
WUTIME
BIAS_TOP_B


RF Detect Timer
I7
I6
I5
RST
CKN
CKP
CKON
CKOP
wuabort_cbit


I101
RST
CKN
CKP
CKON
CKOP
wuabort_cbit
I116
nand2
6u/1u
net85
net35
net86
8u/1u
I118
nand4
6u/1u
net35
net131
net31
net34
net33
16u/1u
13

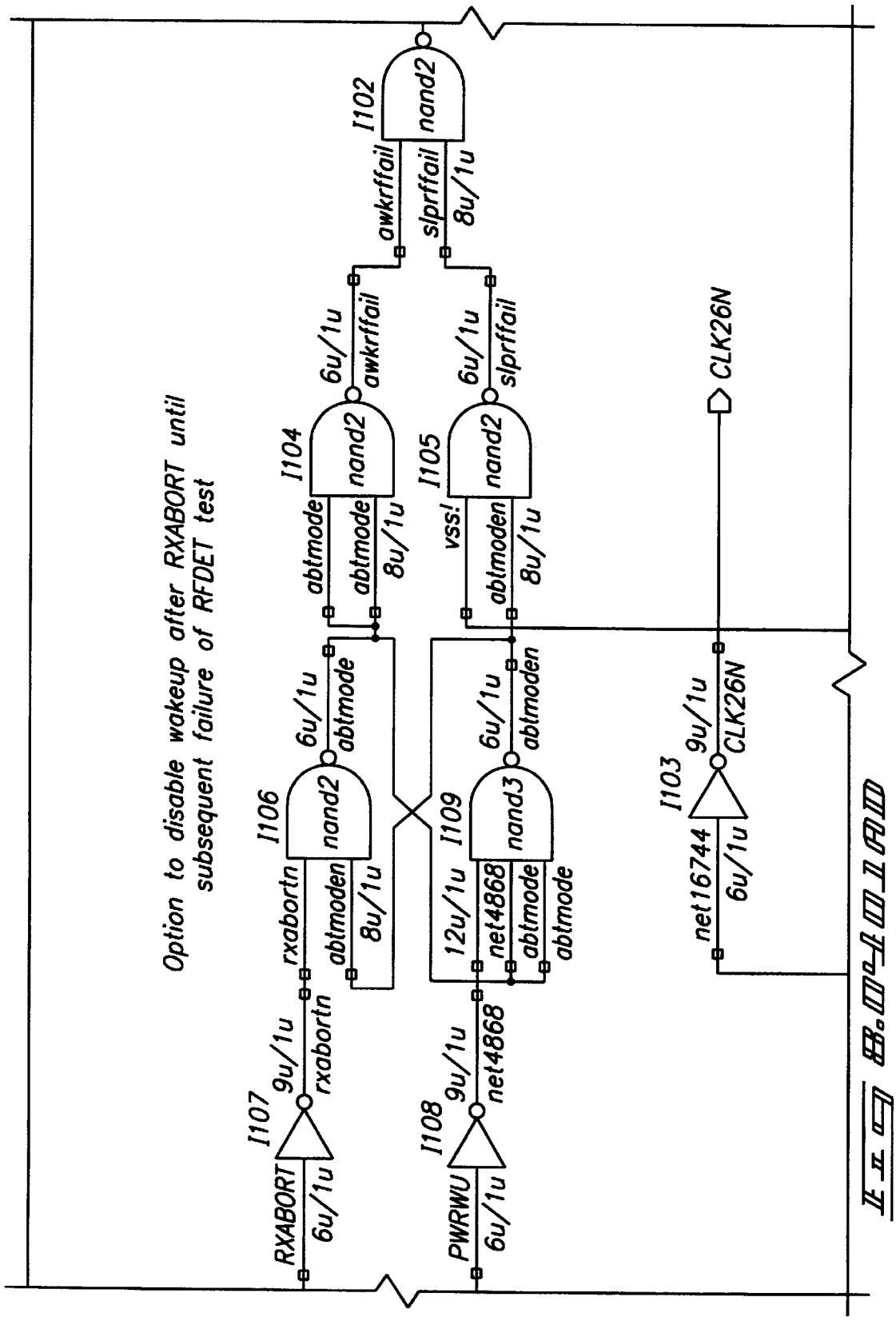


FIG. 88.0FA1AD

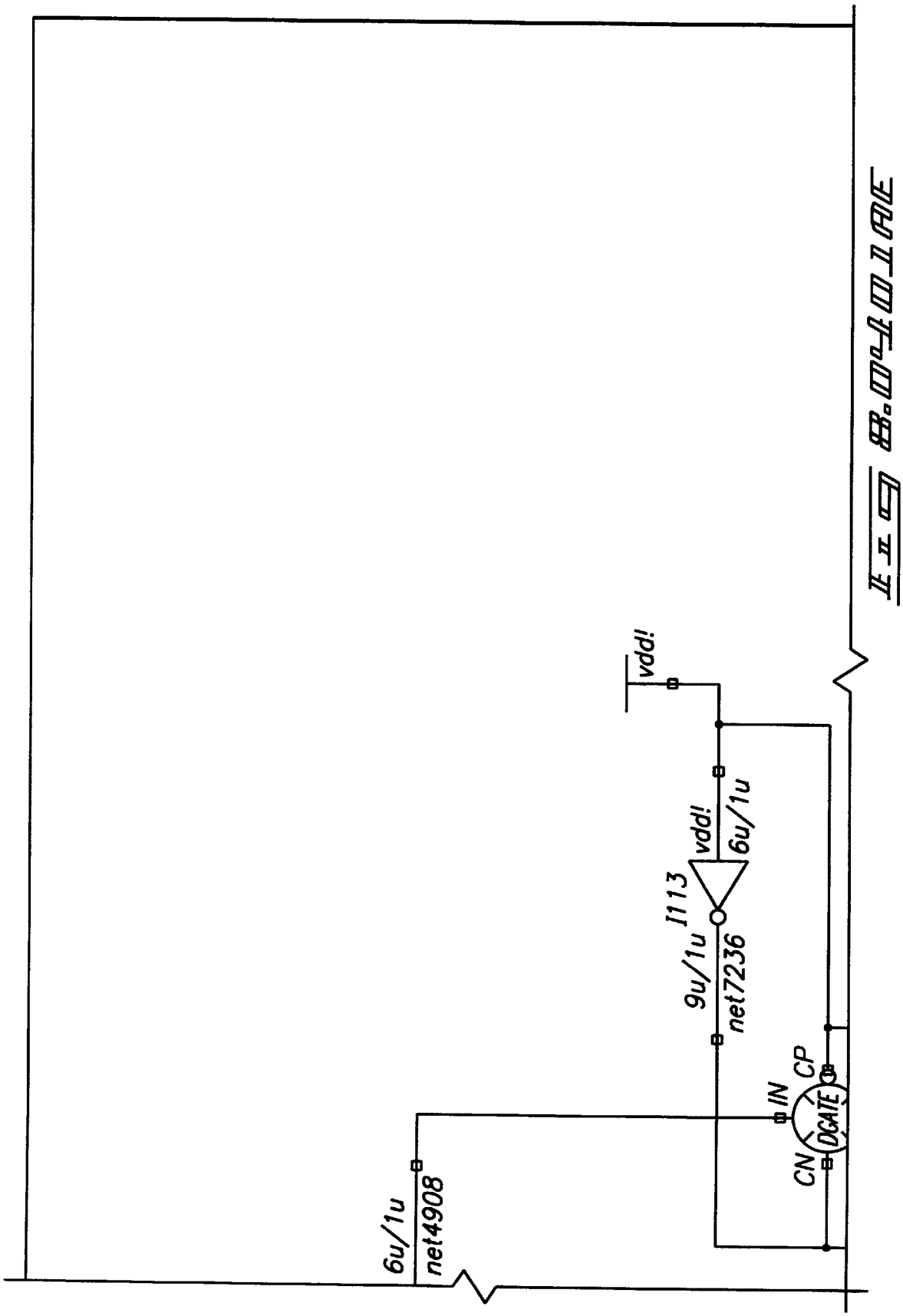


FIG. 88.0-A00_11.AVE

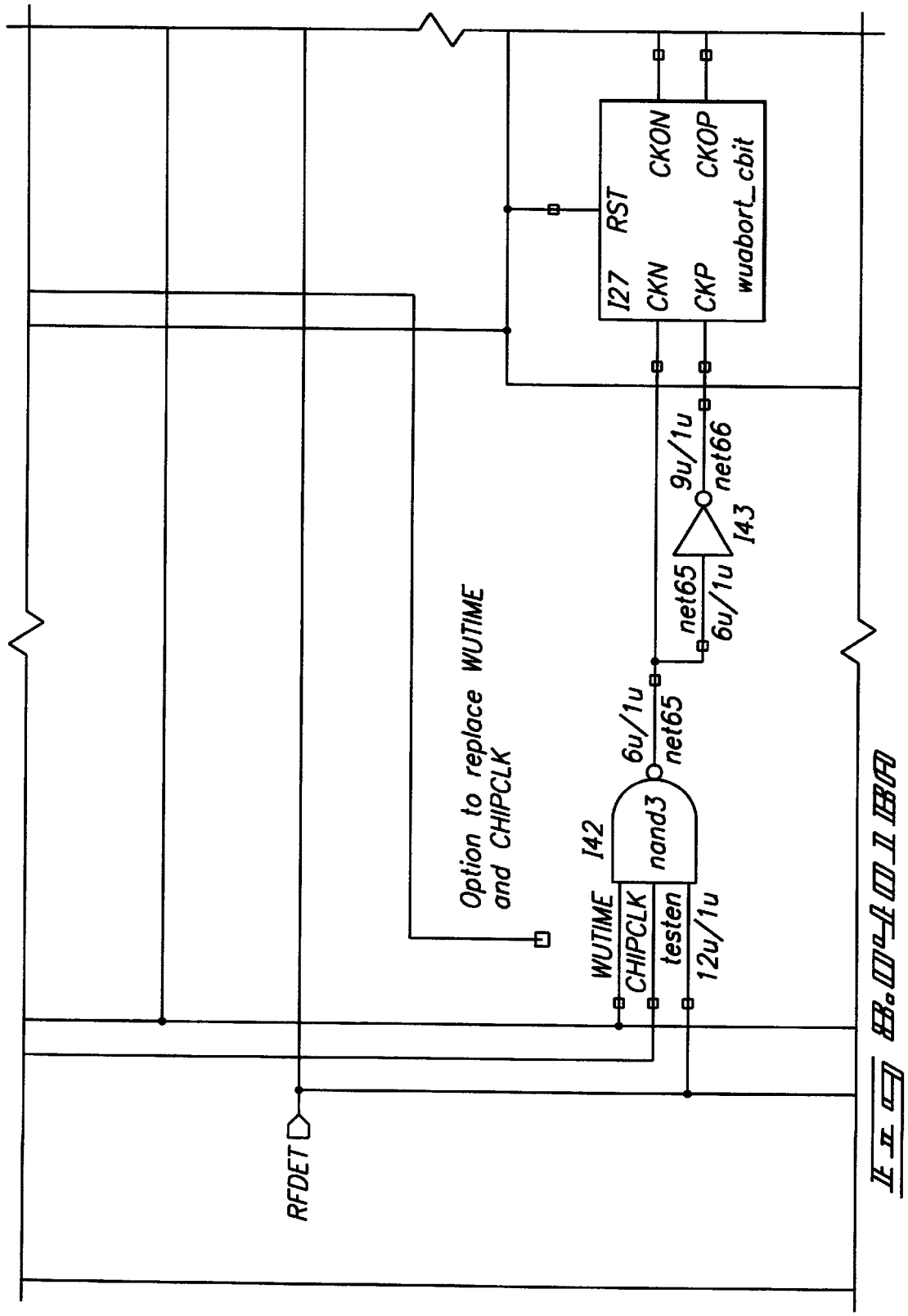


FIG. 88.00-A.00_II.IBIA

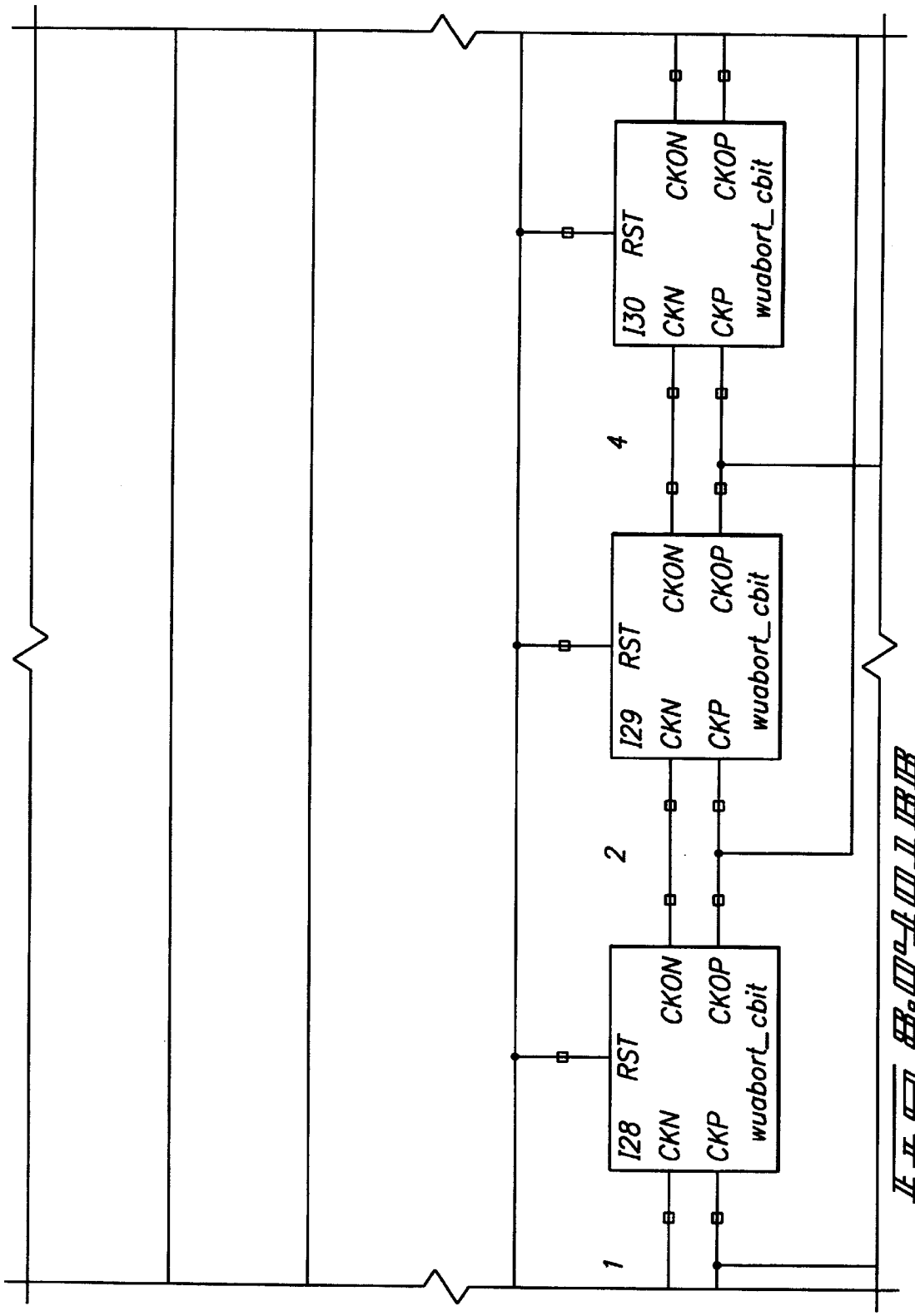
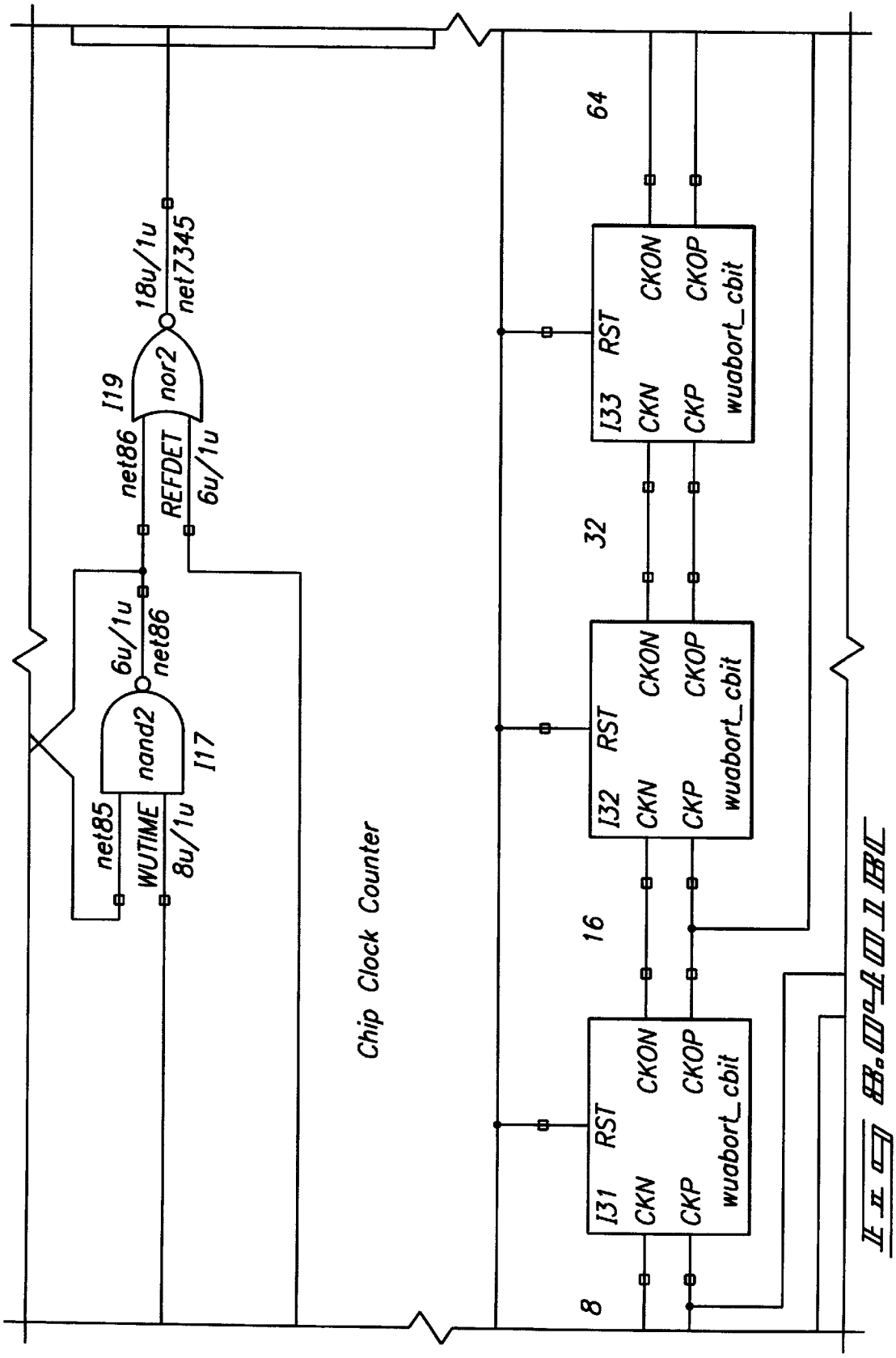
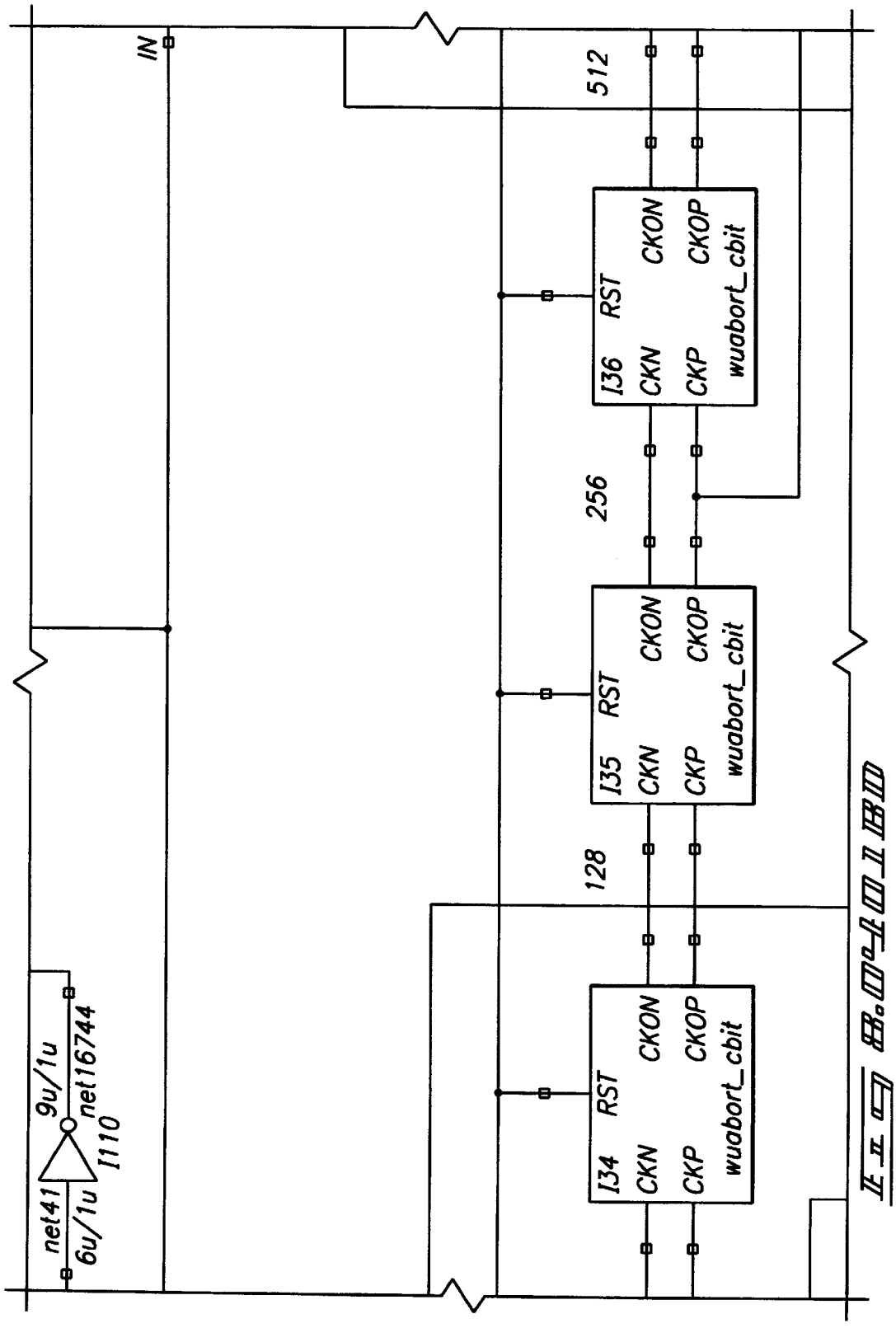


FIG 89.0041 IBM


Chip Clock Counter
I19
nor2
18u/1u
net7345
net86
REFDET
6u/1u
6u/1u
net86
nand2
I17
net85
WUTIME
8u/1u
64
32
16
8
I33
I32
I31
RST
CKON
CKOP
CKN
CKP
wuabort_cbit


IN
512
256
128
I36
I35
I34
RST
CKON
CKOP
CKN
CKP
wuabort_cbit
9u/1u
net16744
I110
net41
6u/1u

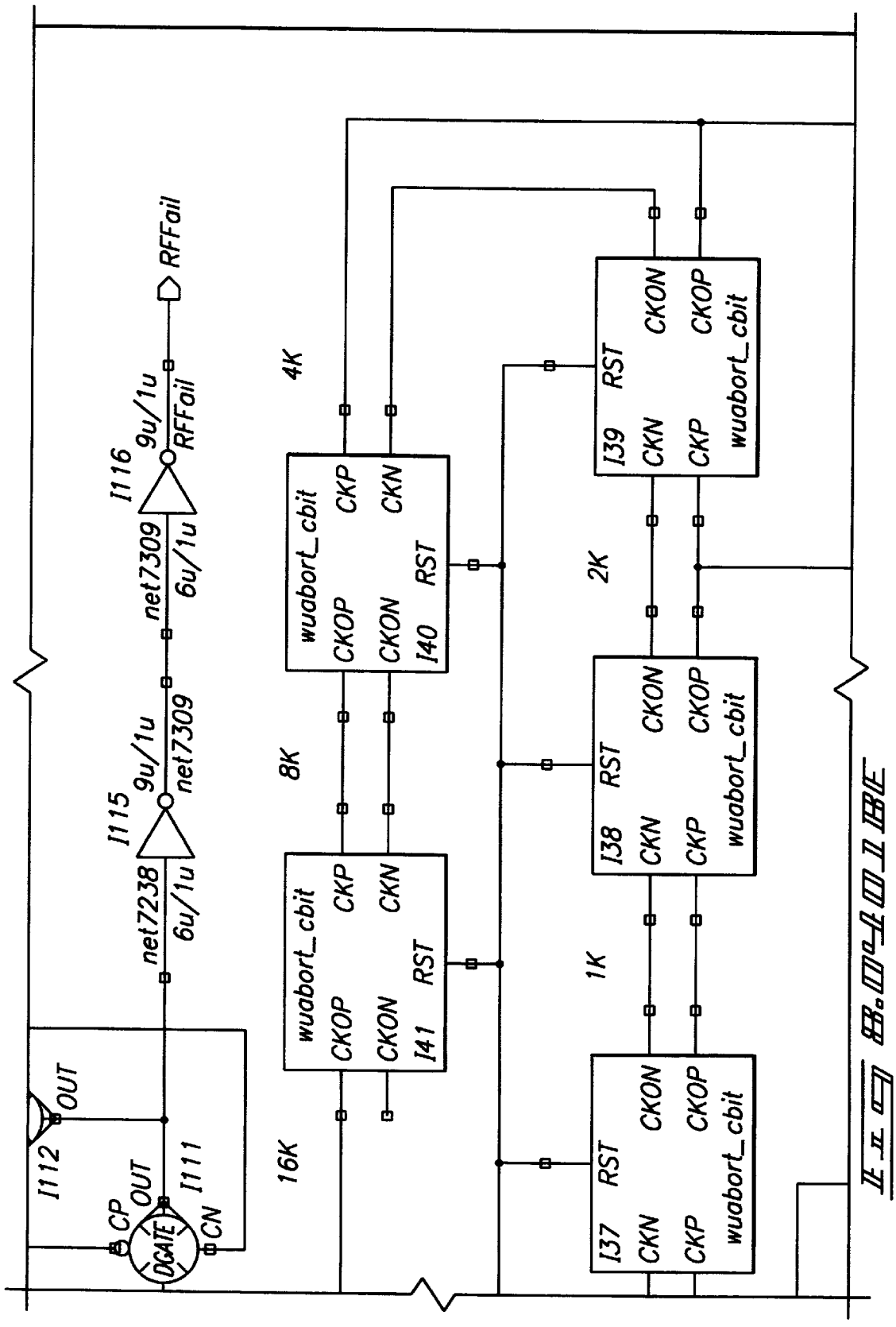

RFFail
I116
9u/1u
RFFail
net7309
6u/1u
I115
9u/1u
net7309
net7238
6u/1u
I112
OUT
CP
OUT
I111
DGATE
CN
4K
8K
16K
2K
1K
wuabort_cbit
CKP
CKN
CKOP
CKON
RST
I40
I41
I39
I38
I37
CKN
CKP

FIG. 1144

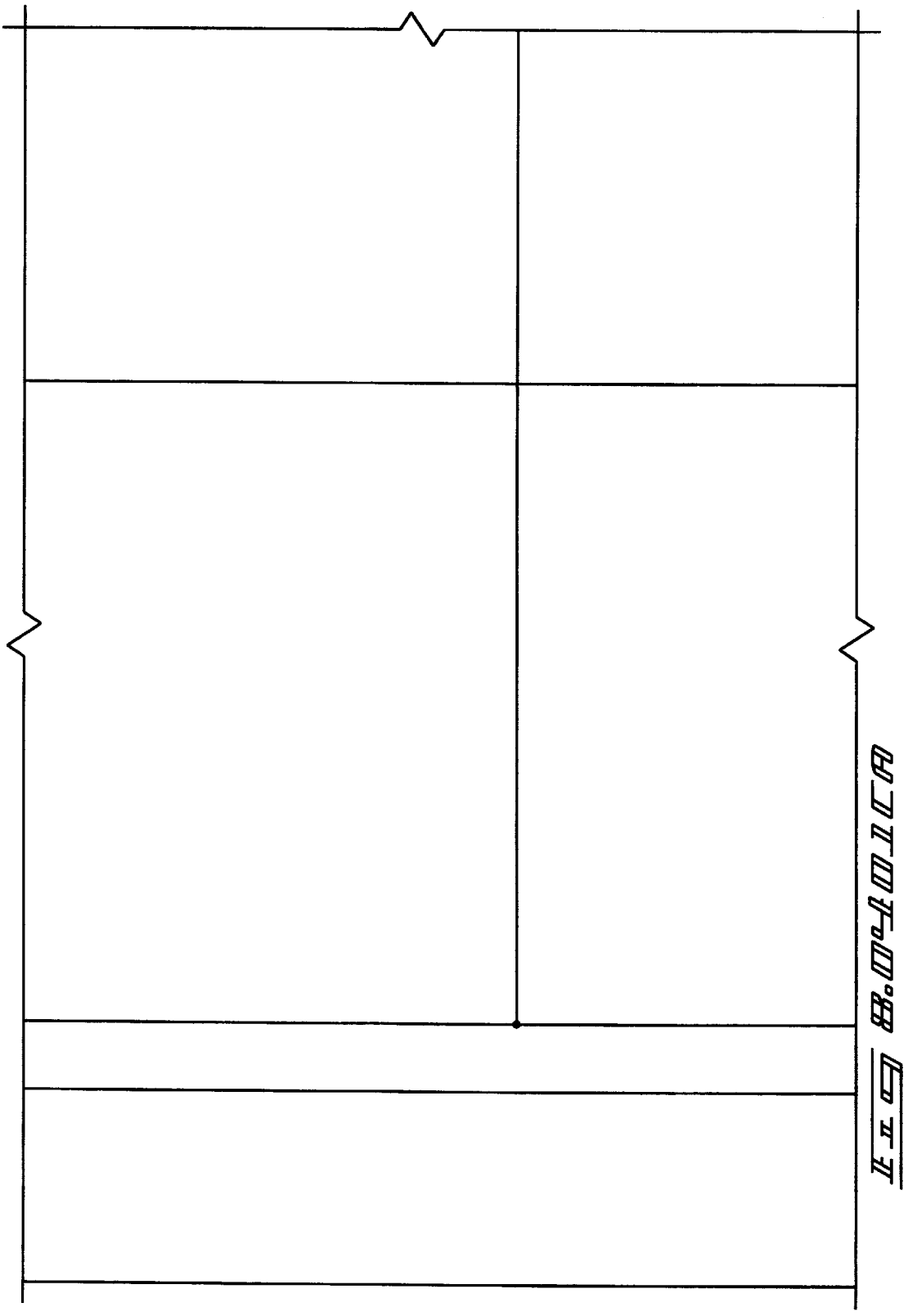
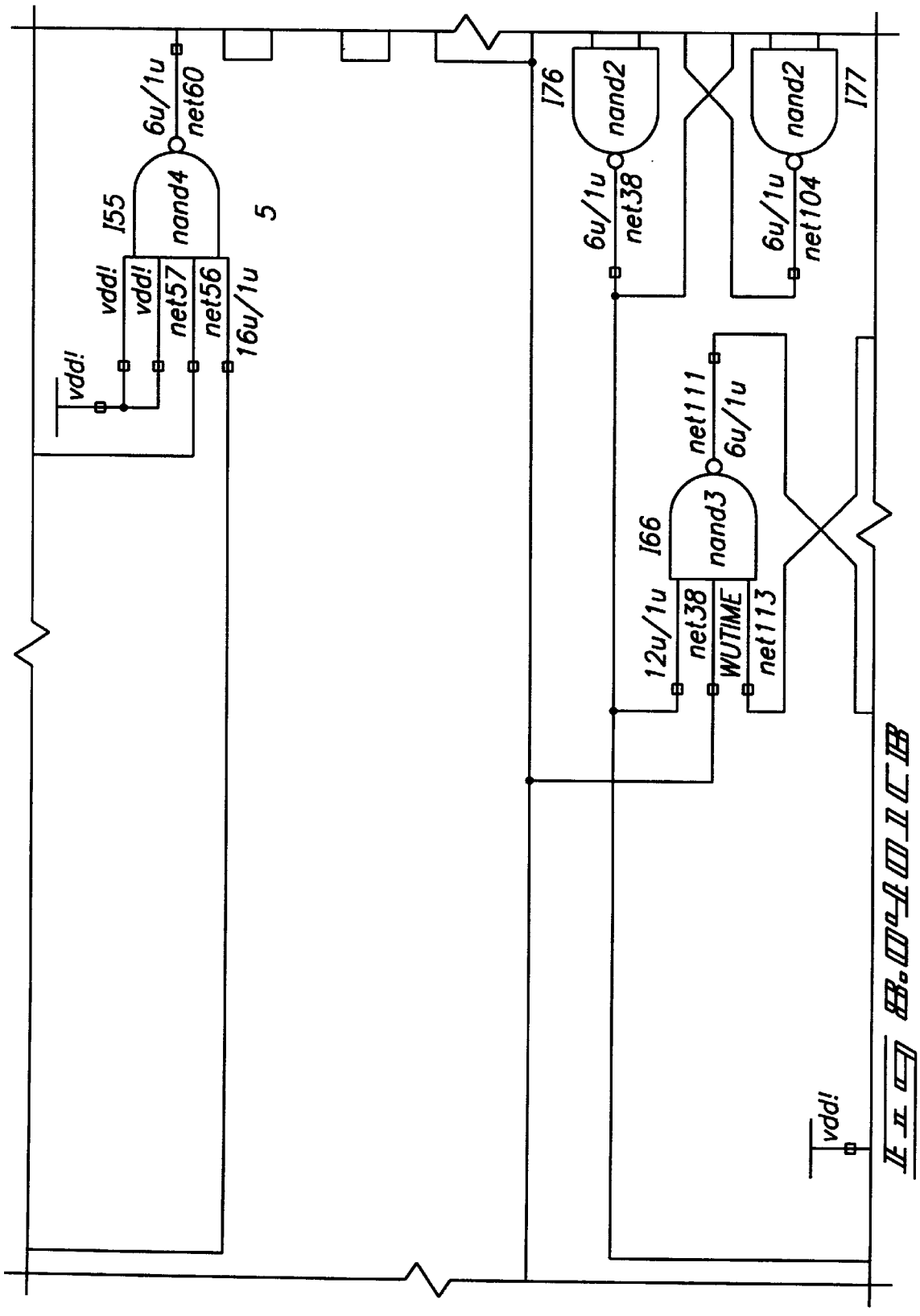


FIG 88.00470


I55
nand4
6u/1u
net60
vdd!
vdd!
net57
net56
16u/1u
vdd!
5
I76
nand2
6u/1u
net38
I77
nand2
6u/1u
net104
net111
6u/1u
I66
nand3
12u/1u
net38
WUTIME
net113
vdd!

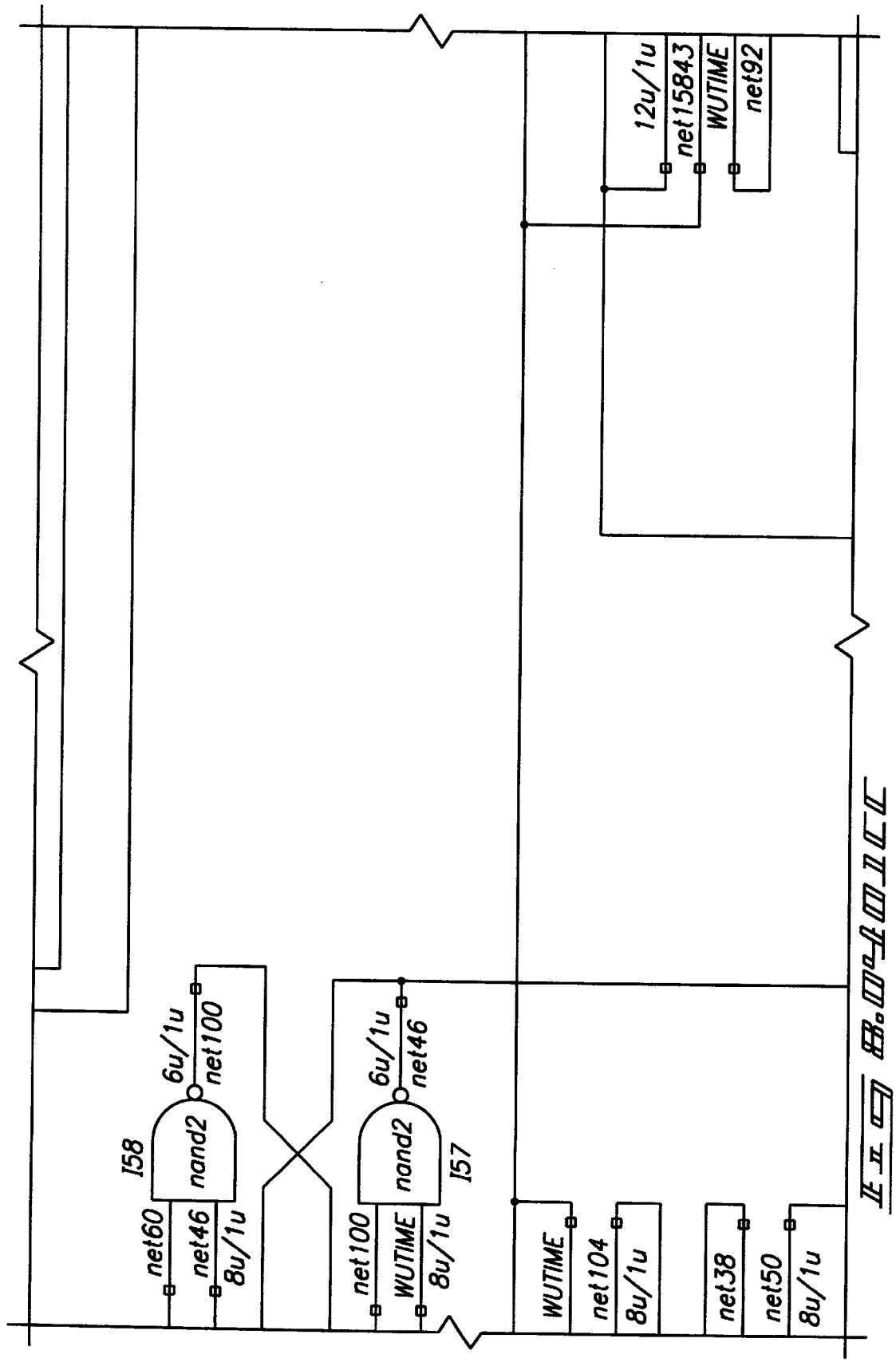
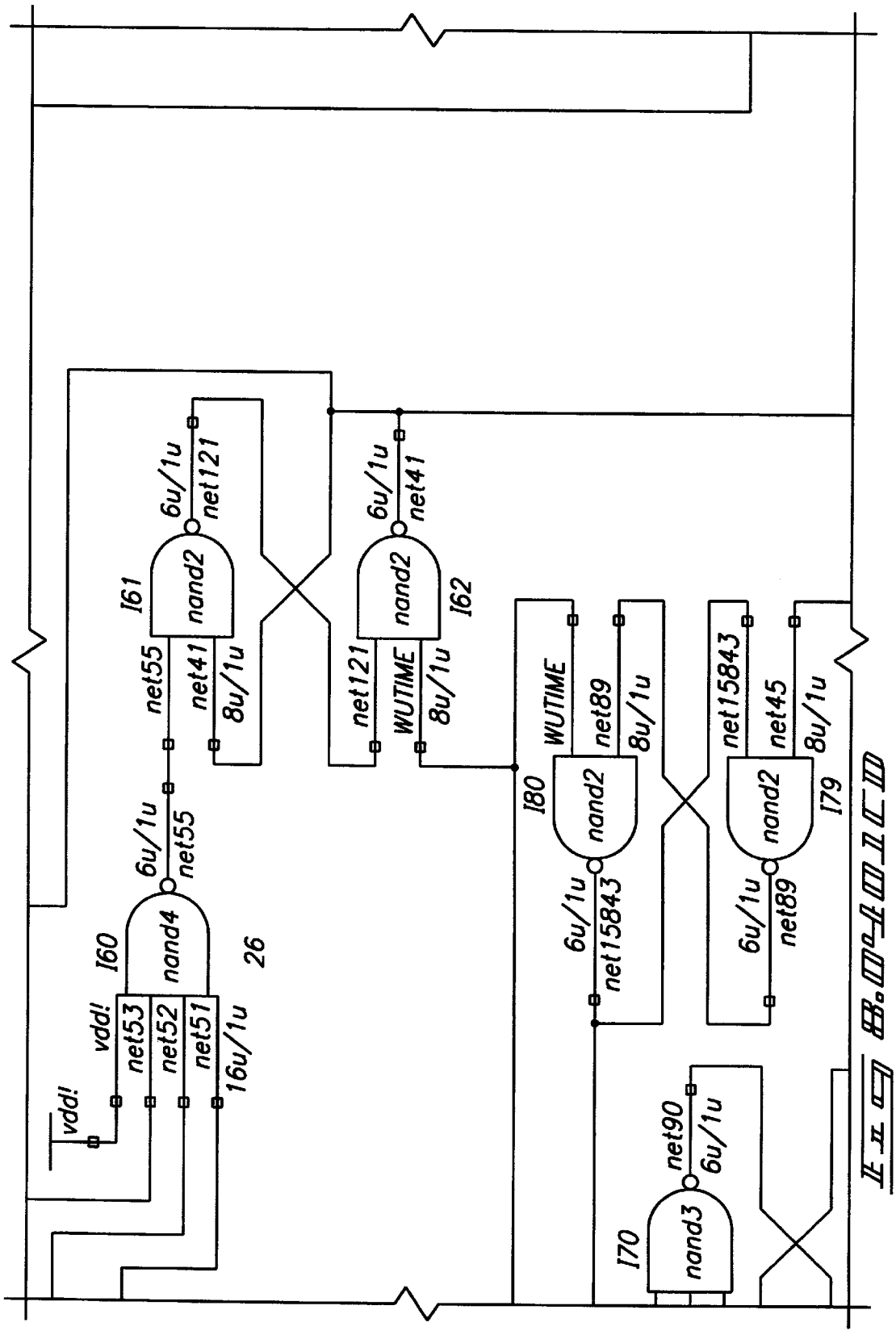
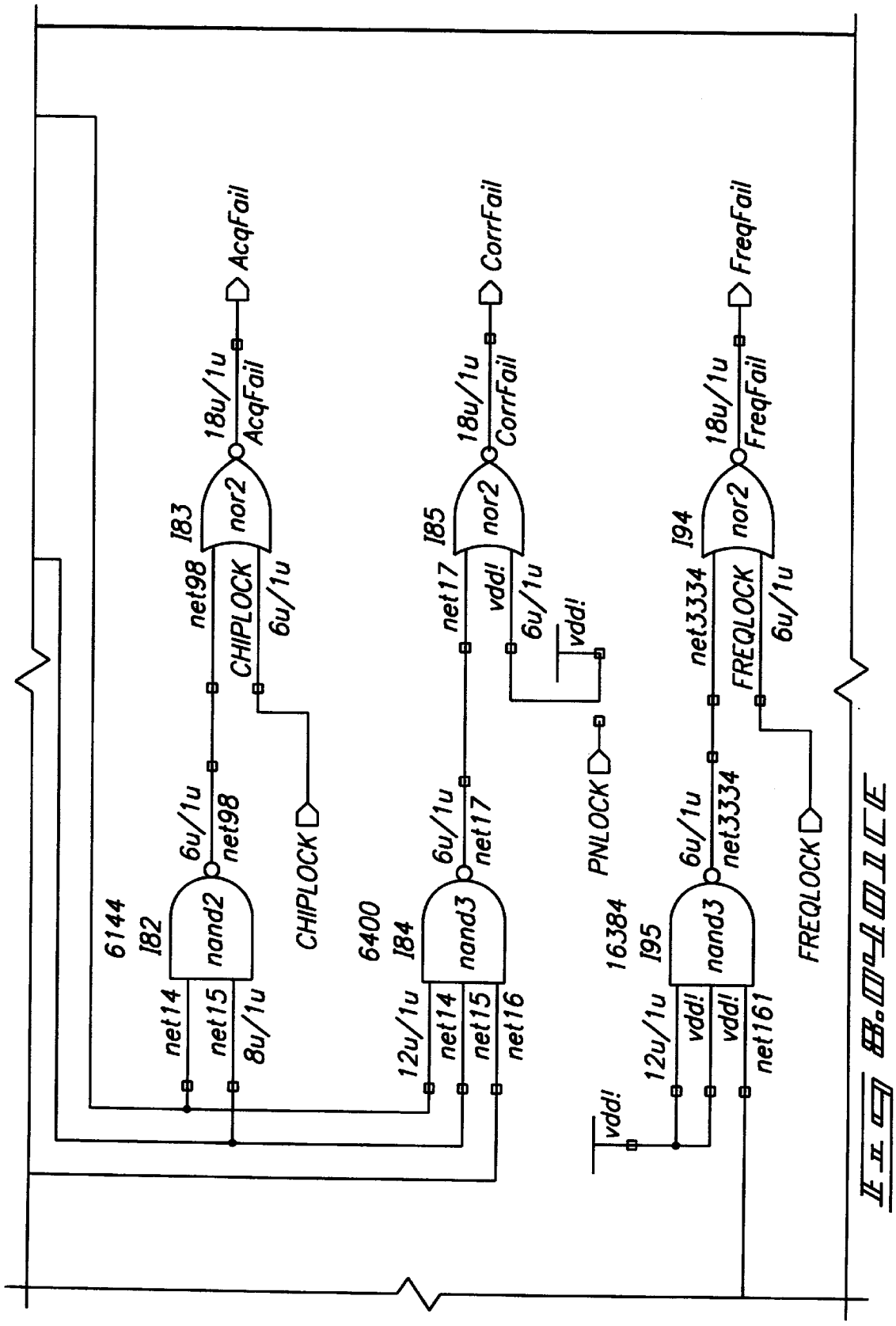

12u/1u
net15843
WUTIME
net92
6u/1u
net100
I58
nand2
net60
net46
8u/1u
6u/1u
net46
nand2
I57
net100
WUTIME
8u/1u
WUTIME
net104
8u/1u
net38
net50
8u/1u

FIG. 8.00FC


I60
nand4
6u/1u
net55
net53
net52
net51
16u/1u
vdd!
I61
nand2
6u/1u
net121
net55
net41
8u/1u
I62
nand2
6u/1u
net41
net121
WUTIME
8u/1u
I80
nand2
WUTIME
net89
8u/1u
6u/1u
net15843
I79
nand2
net15843
net45
8u/1u
6u/1u
net89
I70
nand3
net90
6u/1u
26


6144
I82
nand2
6u/1u
net98
net14
net15
8u/1u
CHIPLOCK
I83
nor2
18u/1u
AcqFail
net98
CHIPLOCK
6u/1u
AcqFail
6400
I84
nand3
6u/1u
net17
12u/1u
net14
net15
net16
I85
nor2
18u/1u
CorrFail
net17
vdd!
6u/1u
CorrFail
vdd!
PNLOCK
16384
I95
nand3
6u/1u
net3334
12u/1u
vdd!
vdd!
net161
I94
nor2
18u/1u
FreqFail
net3334
FREQLOCK
6u/1u
FreqFail
FREQLOCK

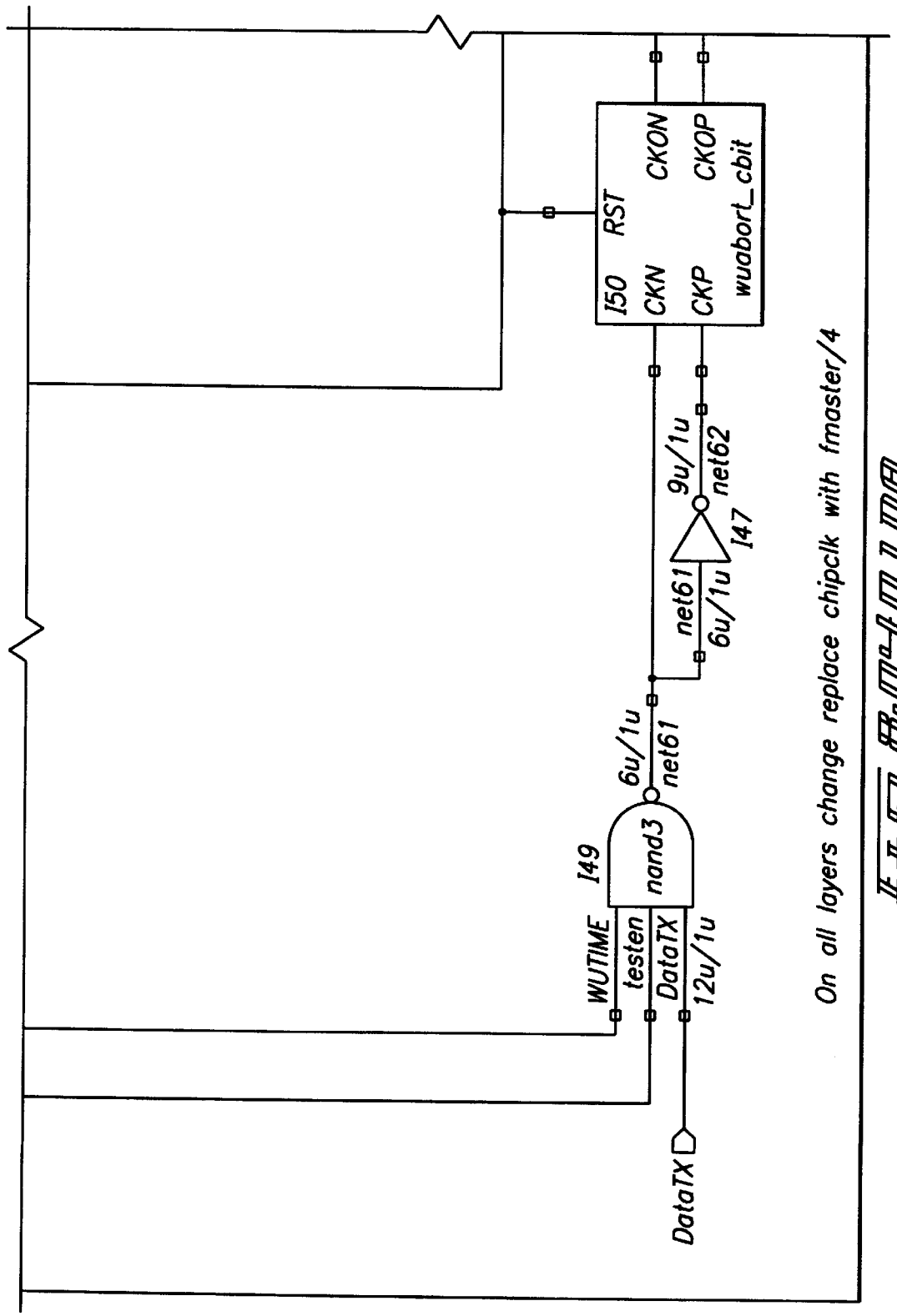
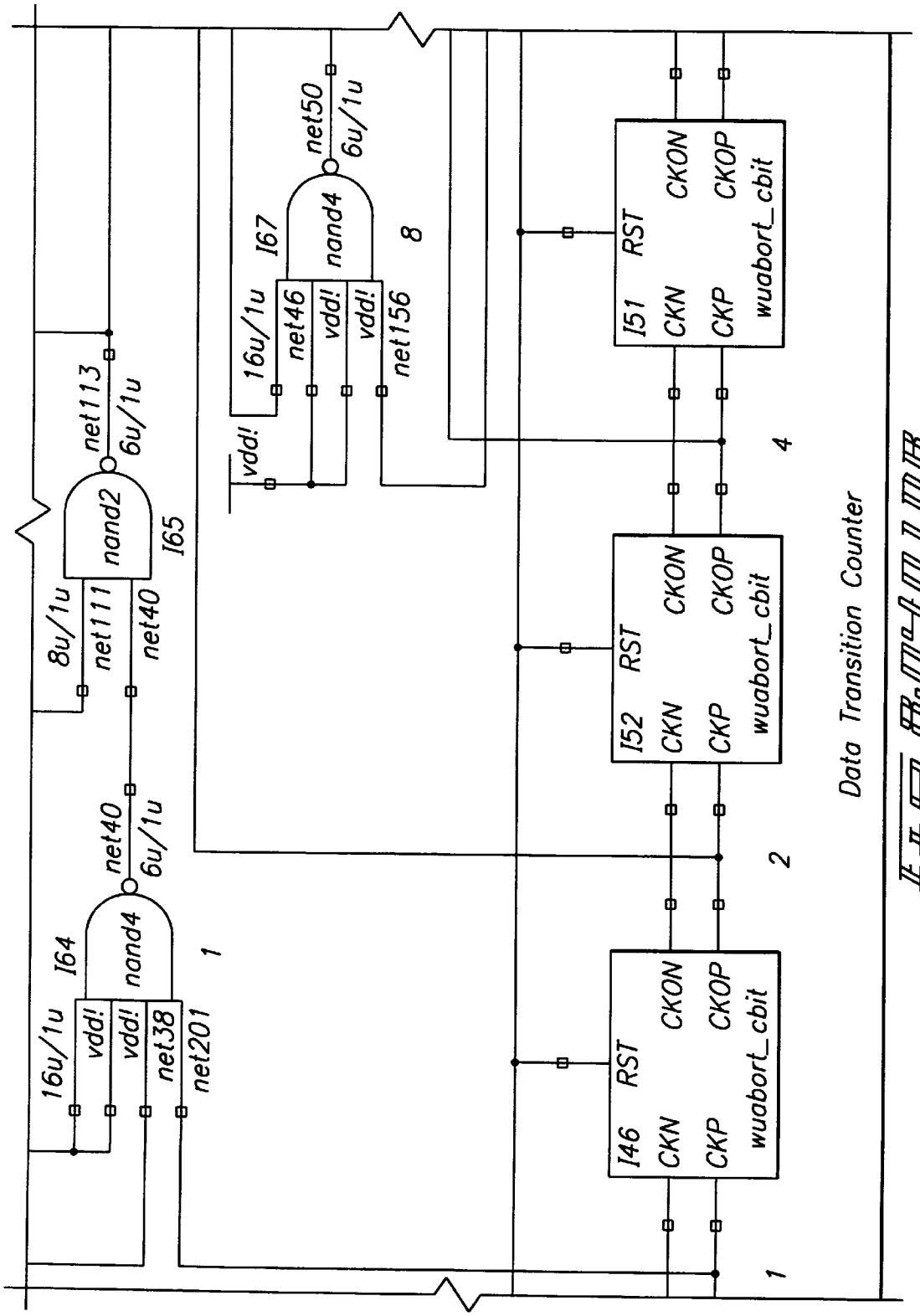
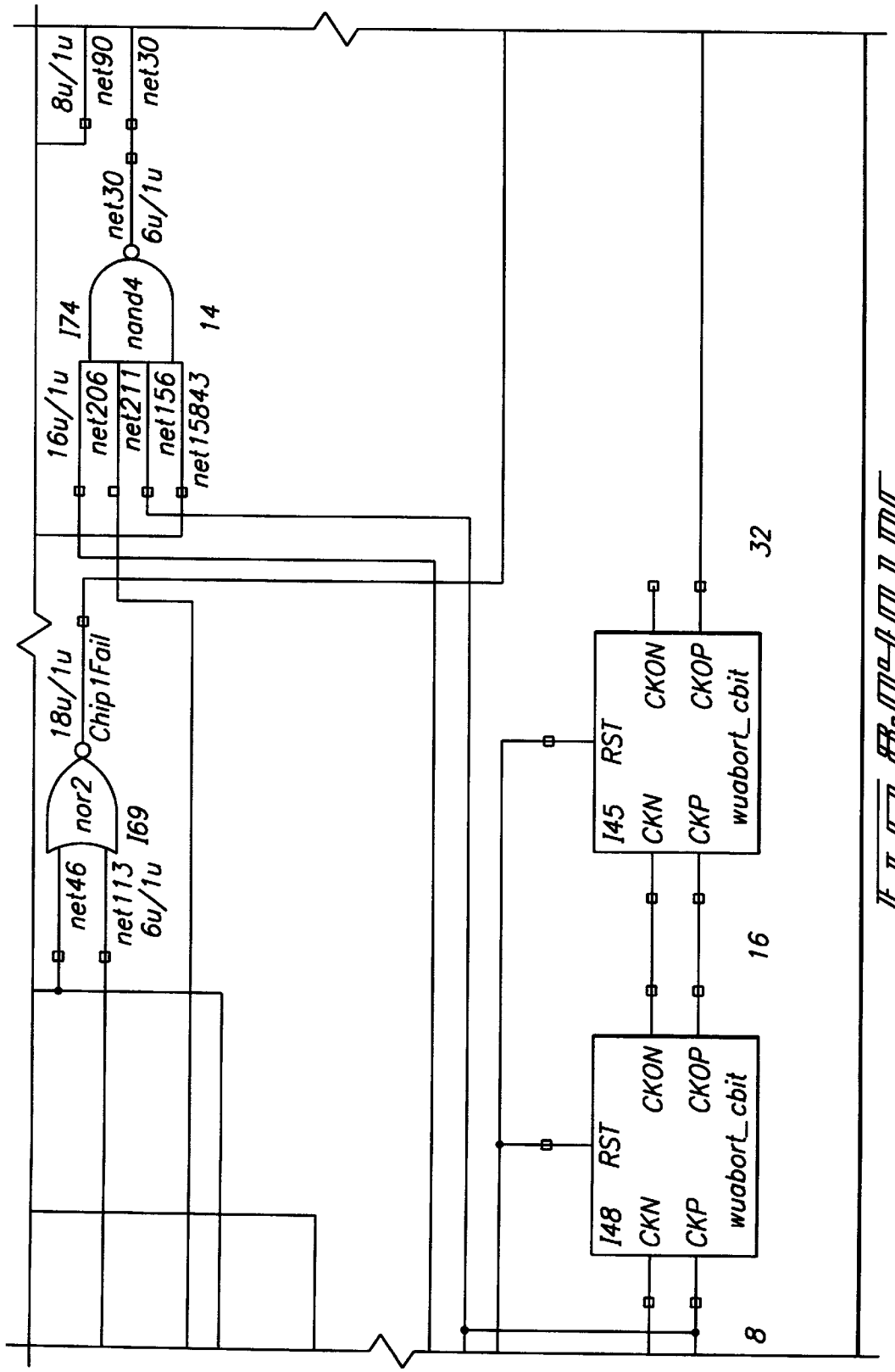


FIG. 88.0041 IDA


Data Transition Counter
I46
I52
I51
wuabort_cbit
RST
CKN
CKP
CKON
CKOP
I64
I65
I67
nand4
nand2
net50
net156
net46
net40
net111
net113
net201
net38
vdd!
16u/1u
6u/1u
8u/1u
8
4
2
1


8u/1u
net90
net30
net30
6u/1u
I74
nand4
14
16u/1u
net206
net211
net156
net15843
18u/1u
Chip1Fail
nor2
I69
net46
net113
6u/1u
I45
RST
CKN
CKP
CKON
CKOP
wuabort_cbit
32
16
I48
RST
CKN
CKP
CKON
CKOP
wuabort_cbit
8

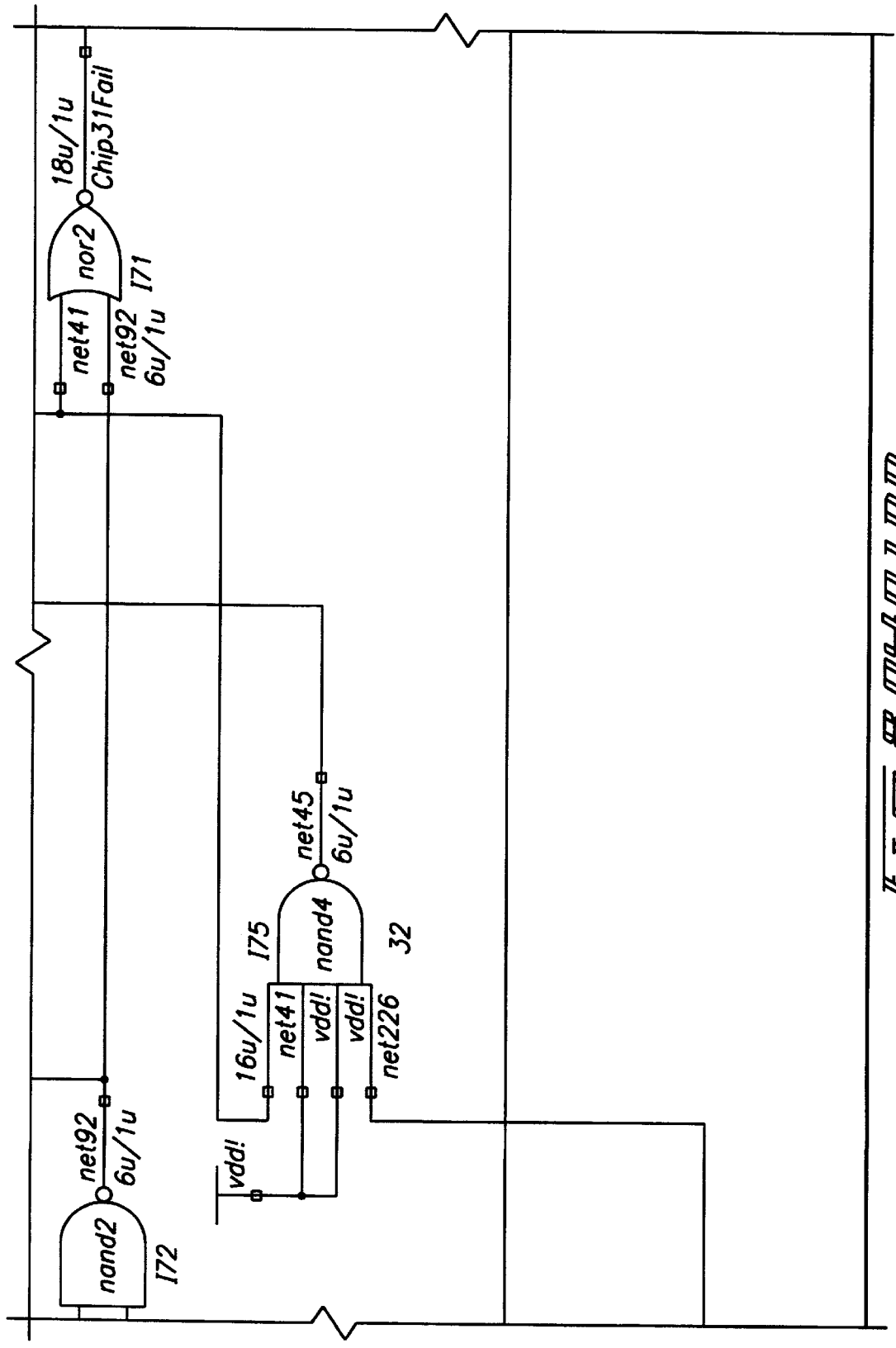
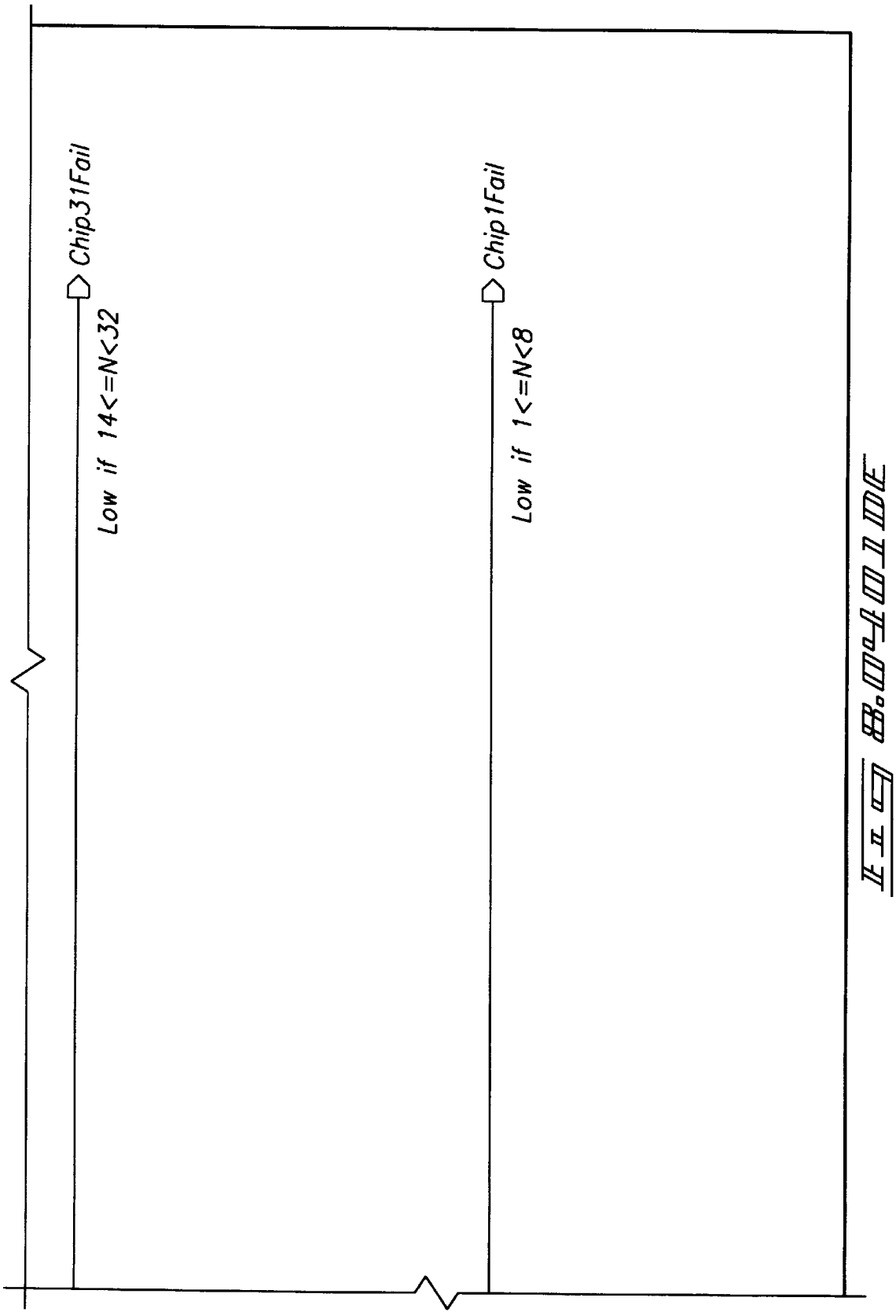

18u/1u
Chip31Fail
nor2
I71
net41
net92
6u/1u
net45
6u/1u
I75
nand4
32
16u/1u
net41
vdd!
vdd!
net226
vdd!
net92
6u/1u
nand2
I72

FIG 8,041,000


Chip31Fail
Low if 14<=N<32
Chip1Fail
Low if 1<=N<8
FIG. 88,004

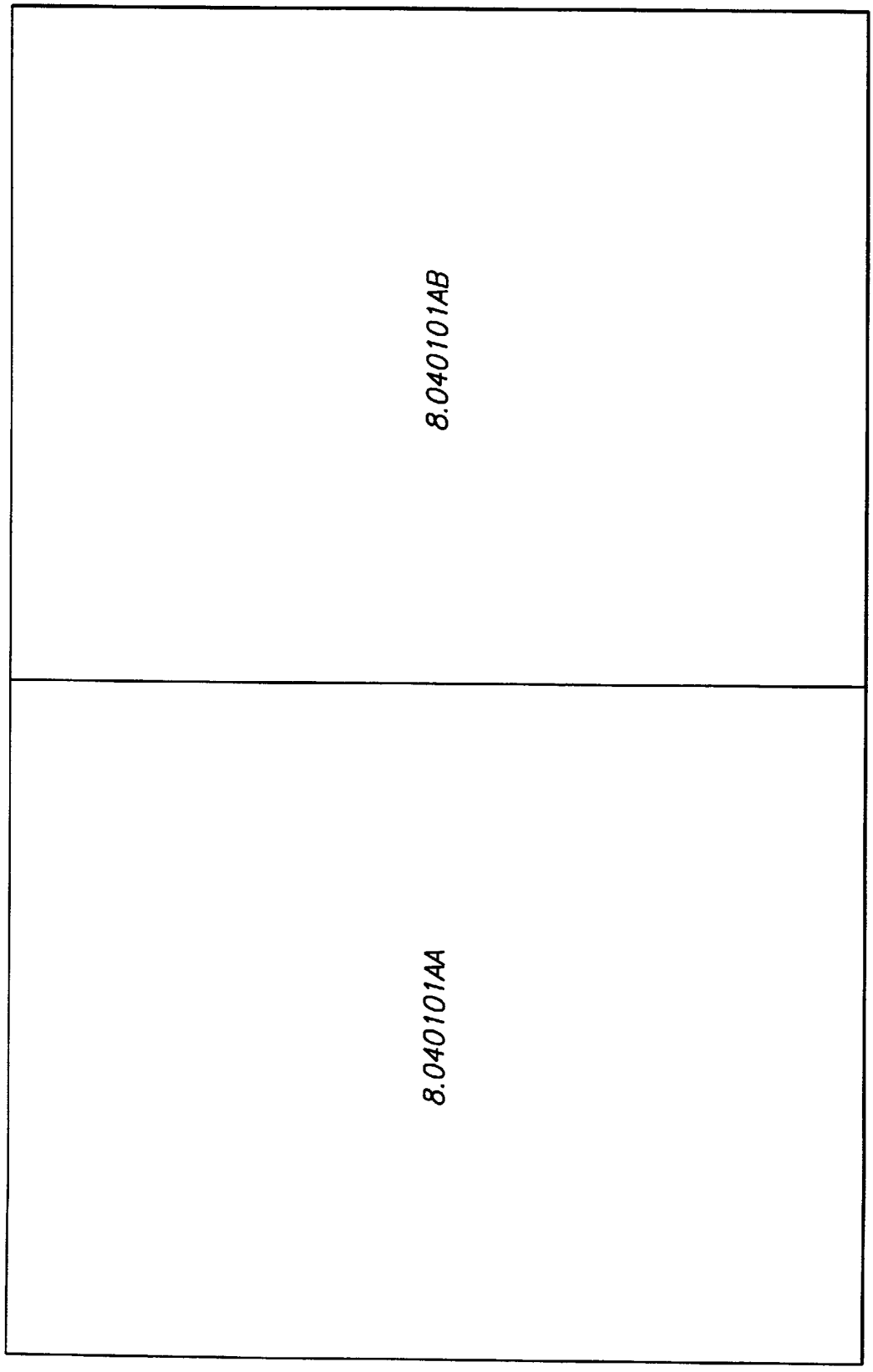


FIG 88.040101

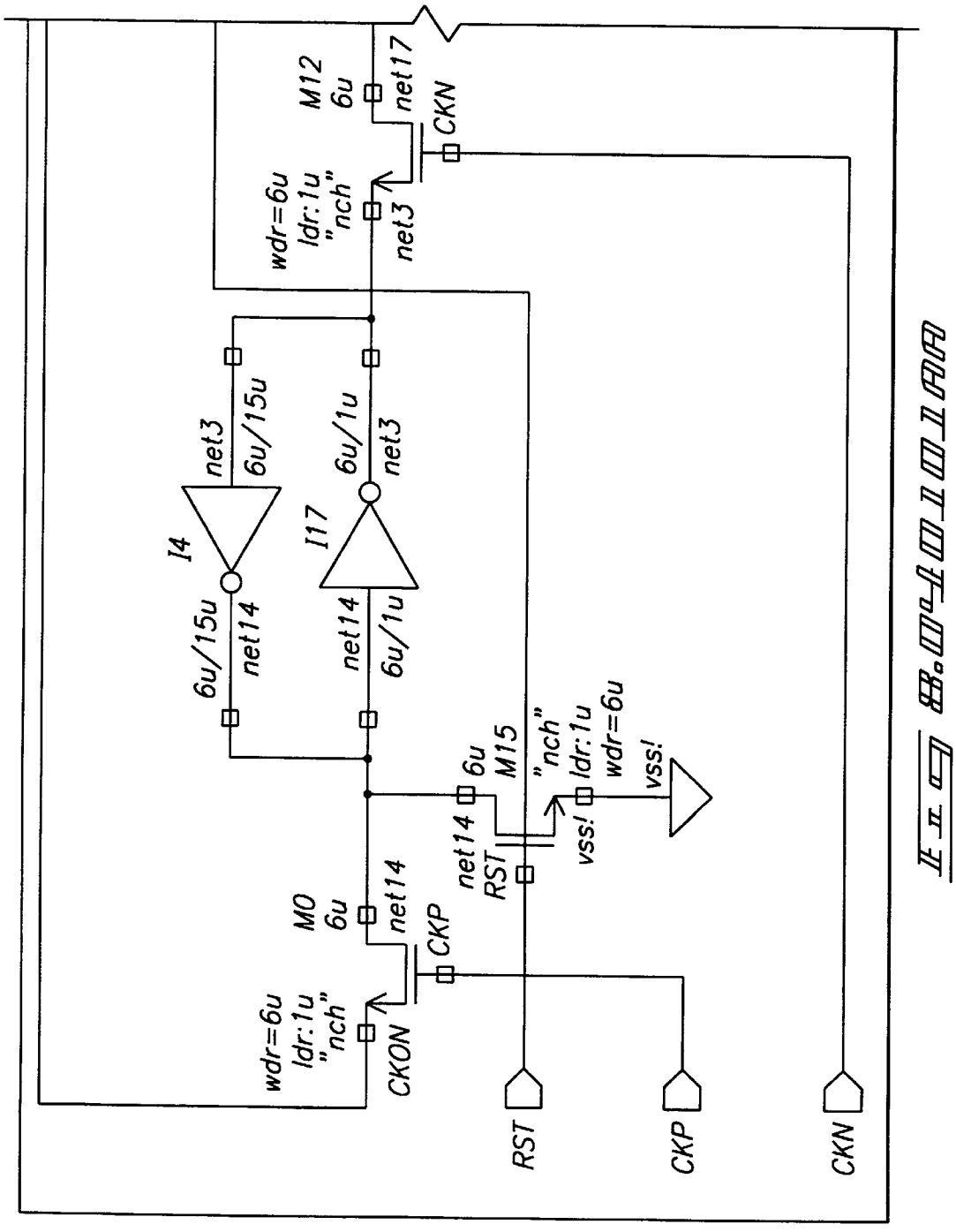


FIG. 88.00fa.00 DUAL LOW POWER

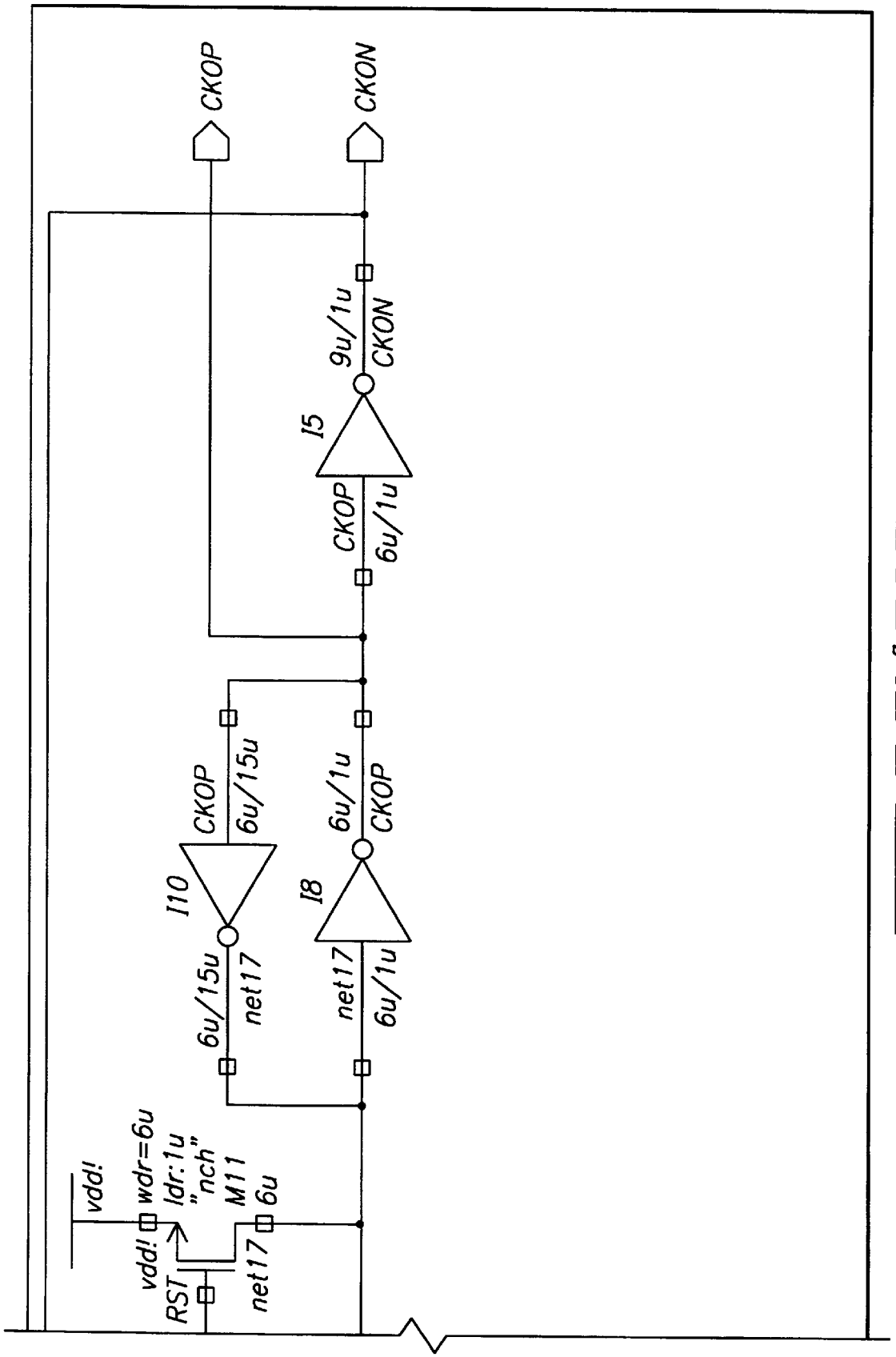
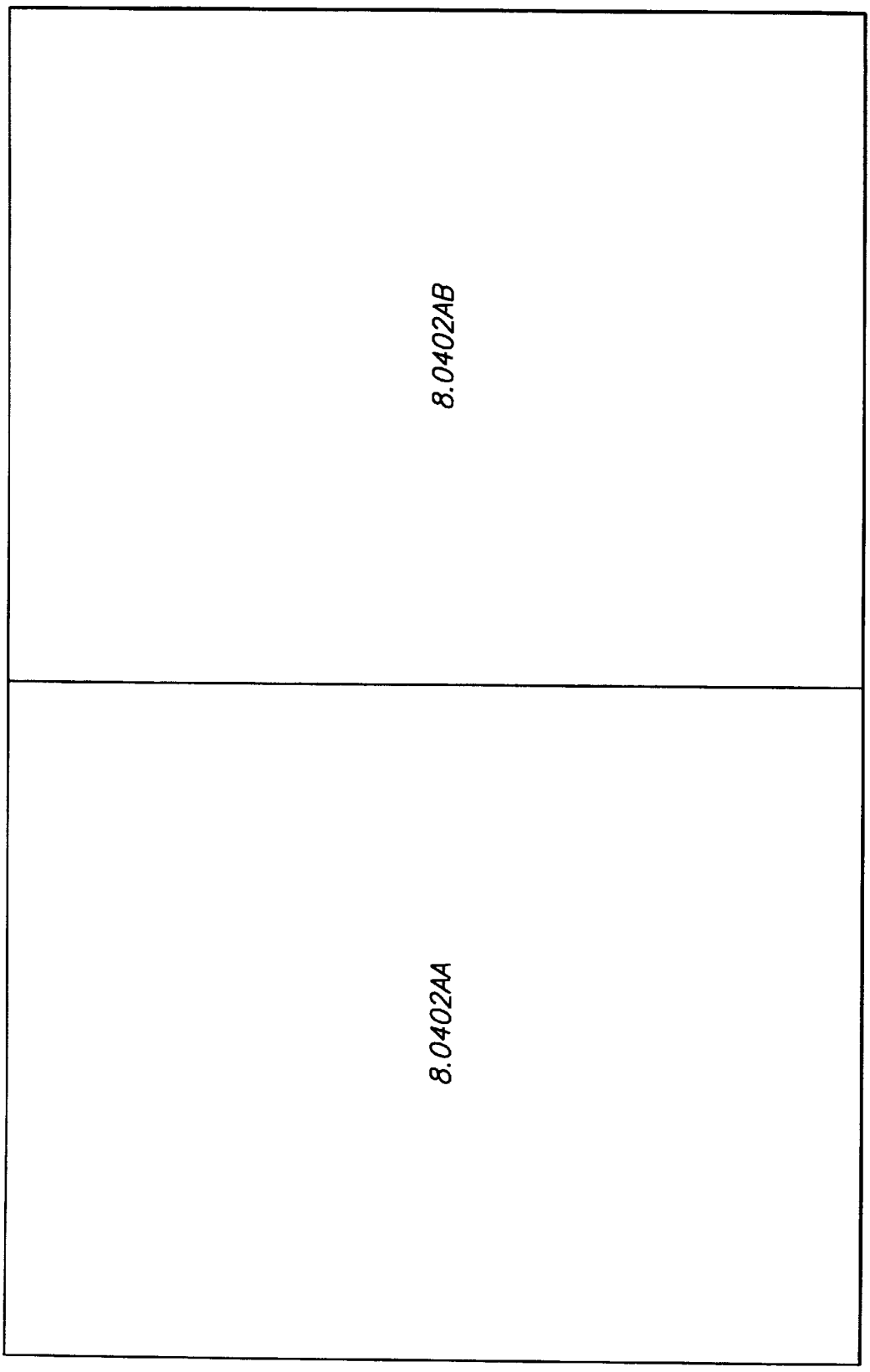

CKOP
CKON
9u/1u
CKON
I5
CKOP
6u/1u
CKOP
6u/15u
6u/1u
CKOP
I10
I8
6u/15u
net17
net17
6u/1u
vdd!
wdr=6u
ldr:1u
"nch"
M11
6u
vdd!
RST
net17

FIG 88.0401A


8.0402AB
8.0402AA
FIG. 8.0402

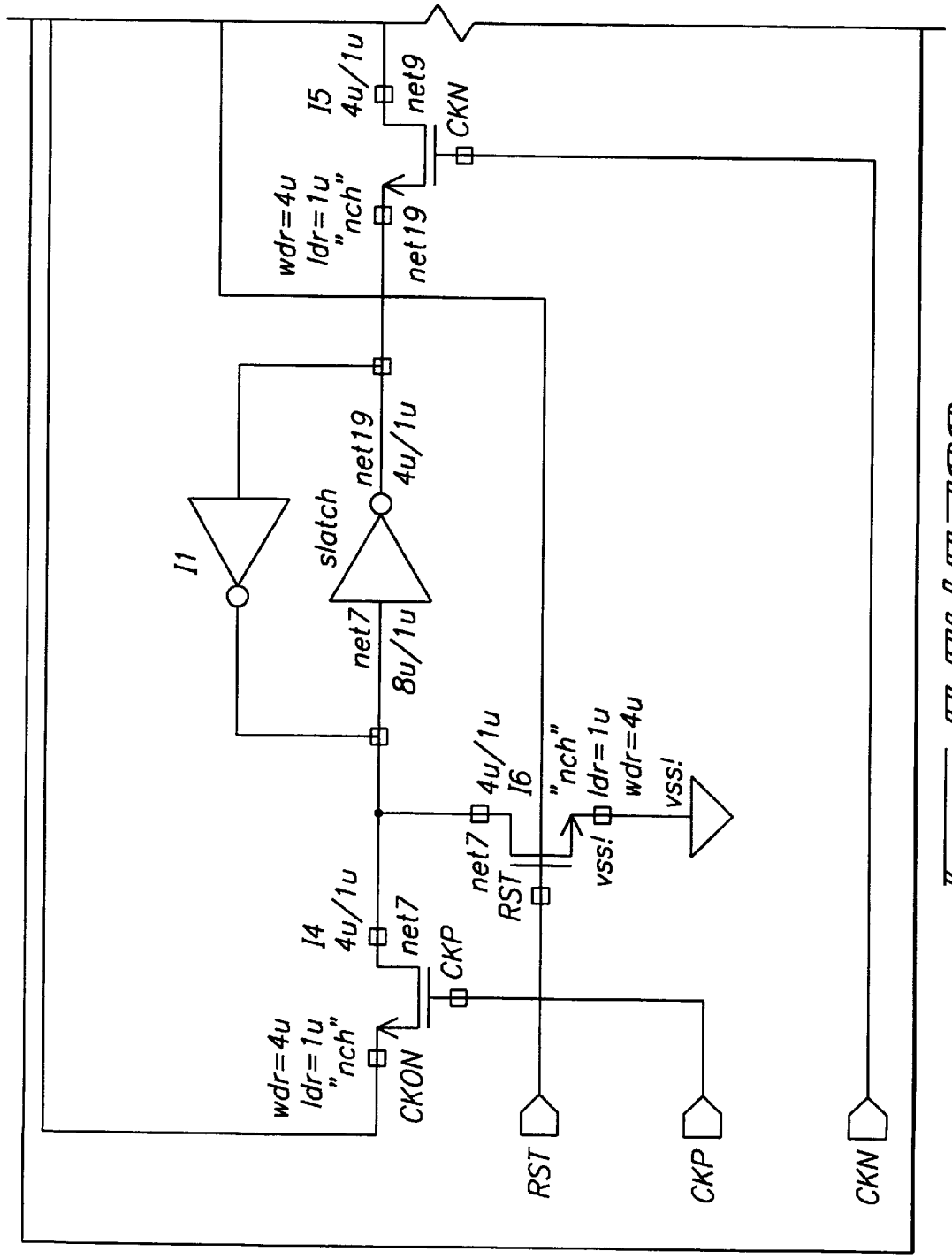

I5
4u/1u
net9
CKN
wdr=4u
ldr=1u
"nch"
net19
I1
slatch
net19
4u/1u
net7
8u/1u
4u/1u
I6
"nch"
ldr=1u
wdr=4u
vss!
net7
RST
vss!
I4
4u/1u
net7
CKP
wdr=4u
ldr=1u
"nch"
CKON
RST
CKP
CKN

FIG 88.00PAA

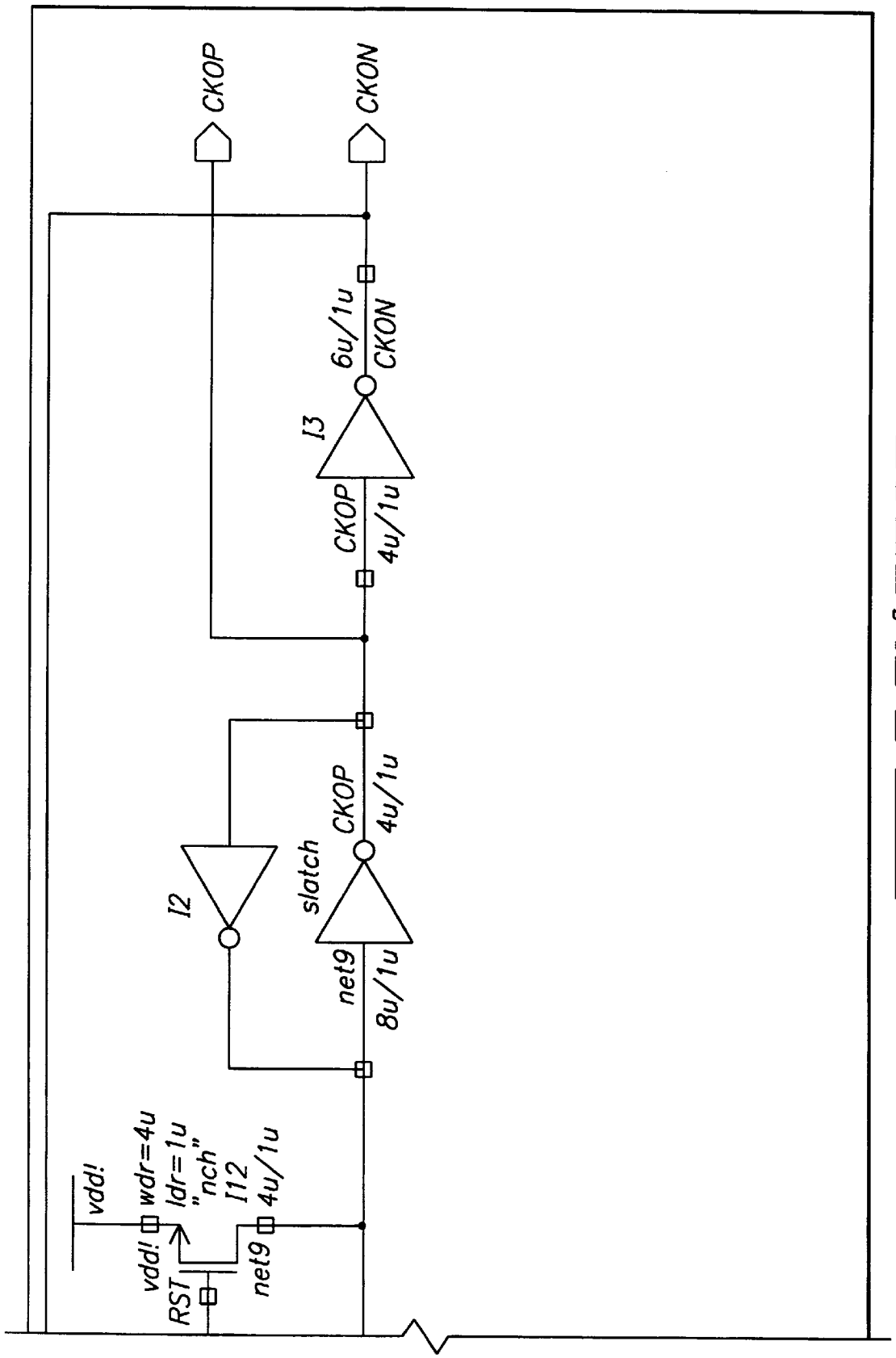

CKOP
CKON
6u/1u
CKON
I3
CKOP
4u/1u
CKOP
4u/1u
slatch
I2
net9
8u/1u
vdd!
wdr=4u
ldr=1u
"nch"
I12
4u/1u
vdd!
RST
net9

FIG 8.004AB

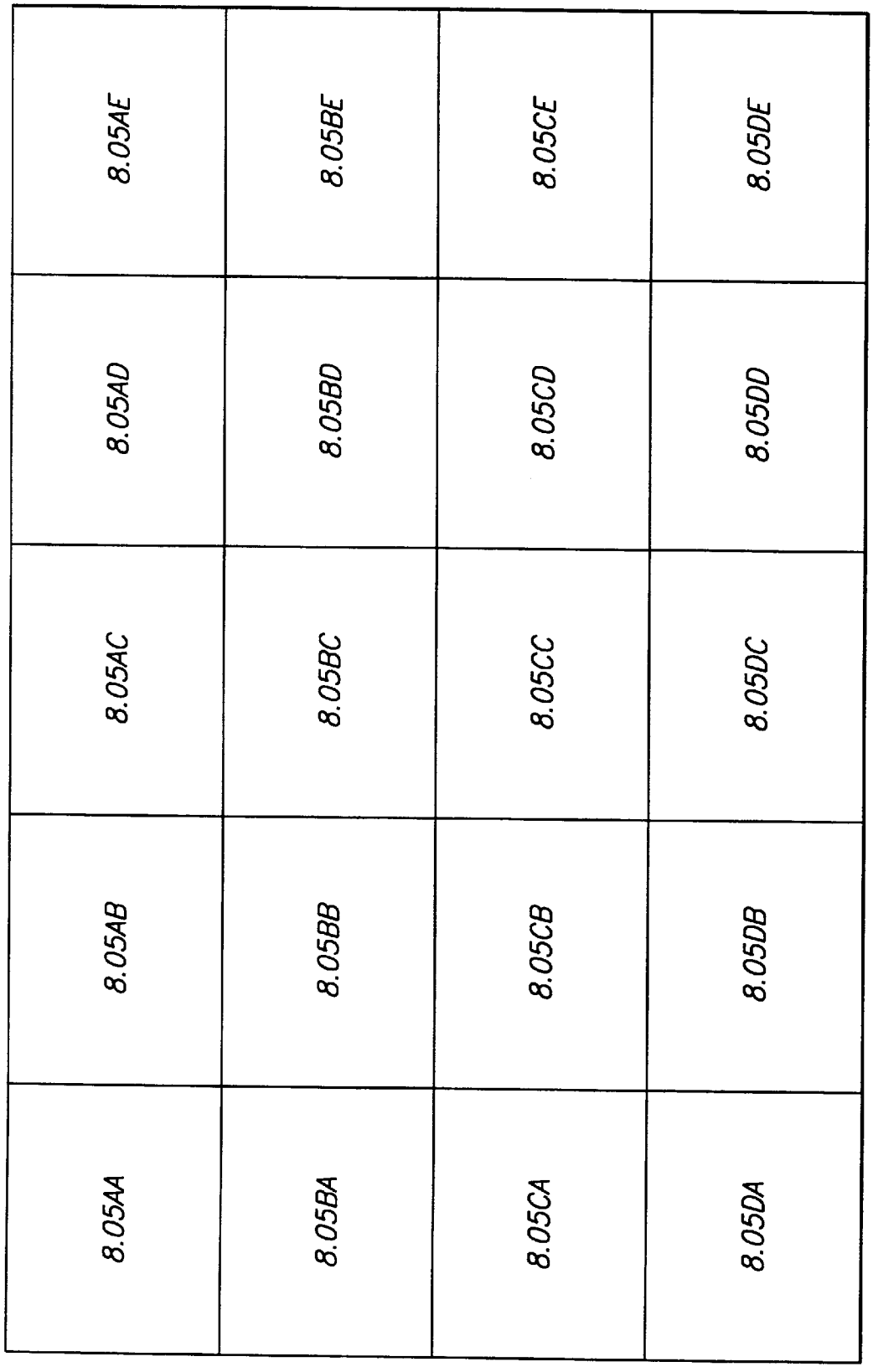

8.05AE
8.05BE
8.05CE
8.05DE
8.05AD
8.05BD
8.05CD
8.05DD
8.05AC
8.05BC
8.05CC
8.05DC
8.05AB
8.05BB
8.05CB
8.05DB
8.05AA
8.05BA
8.05CA
8.05DA

FIG. 8.05

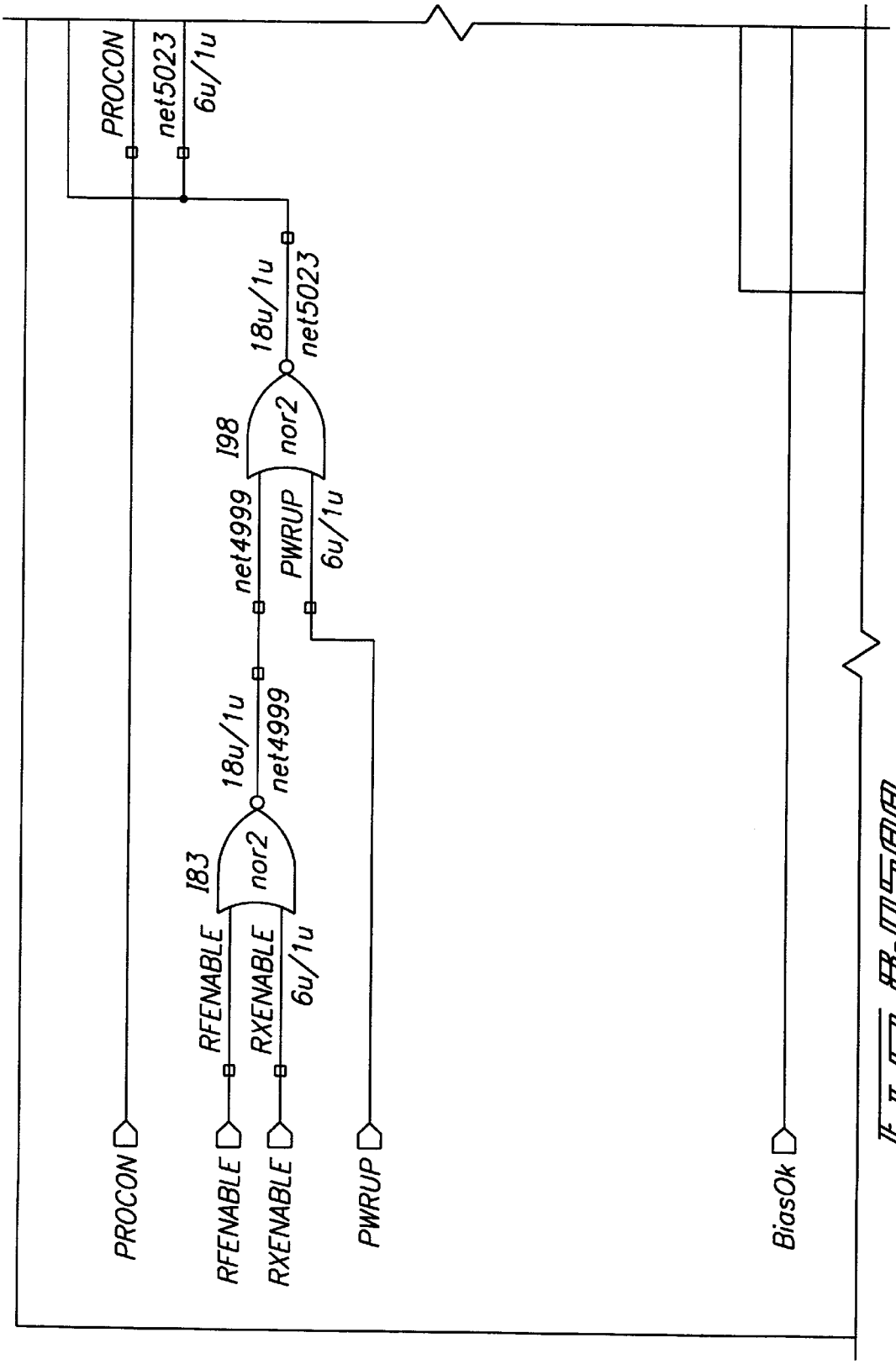
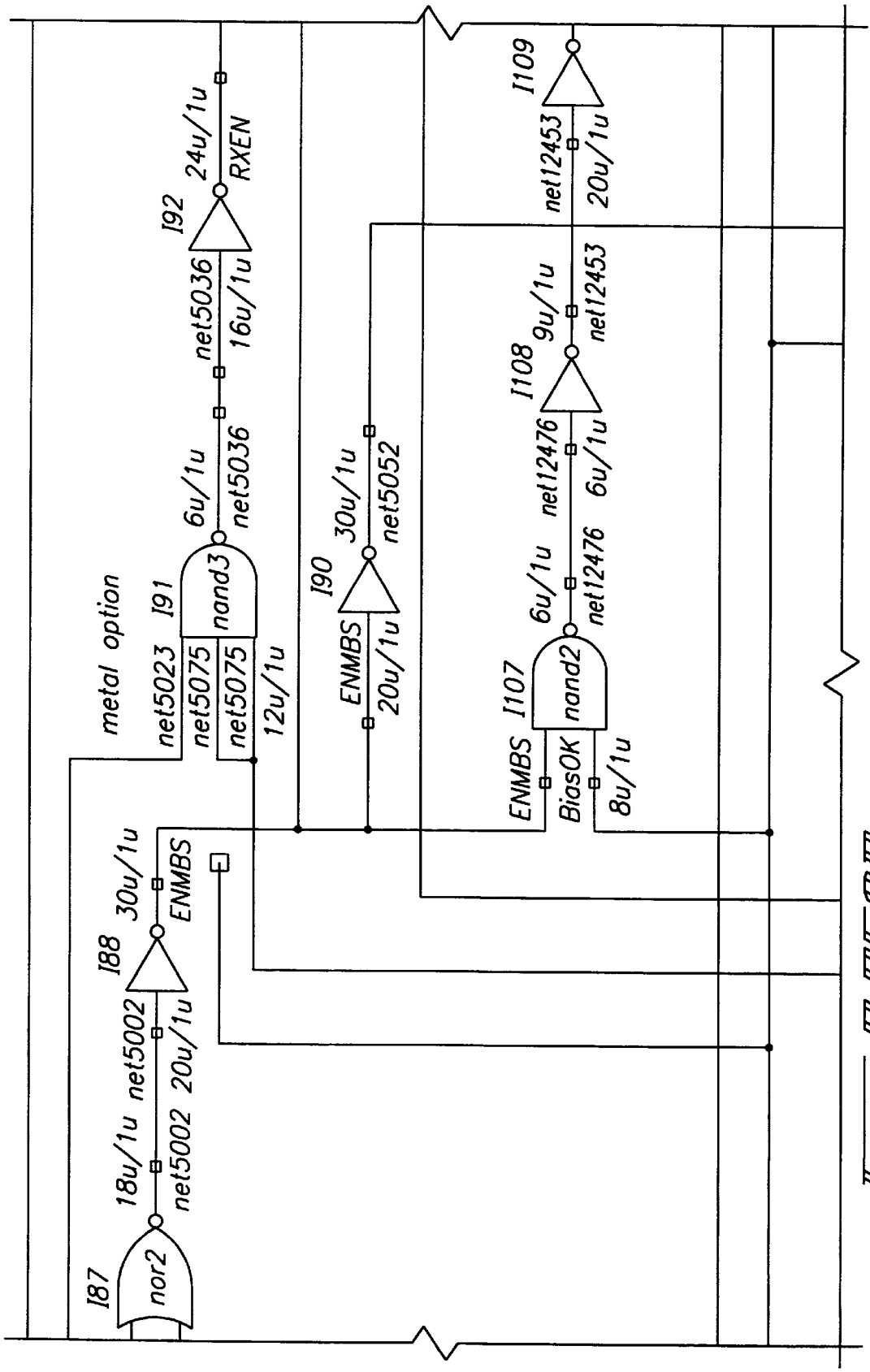
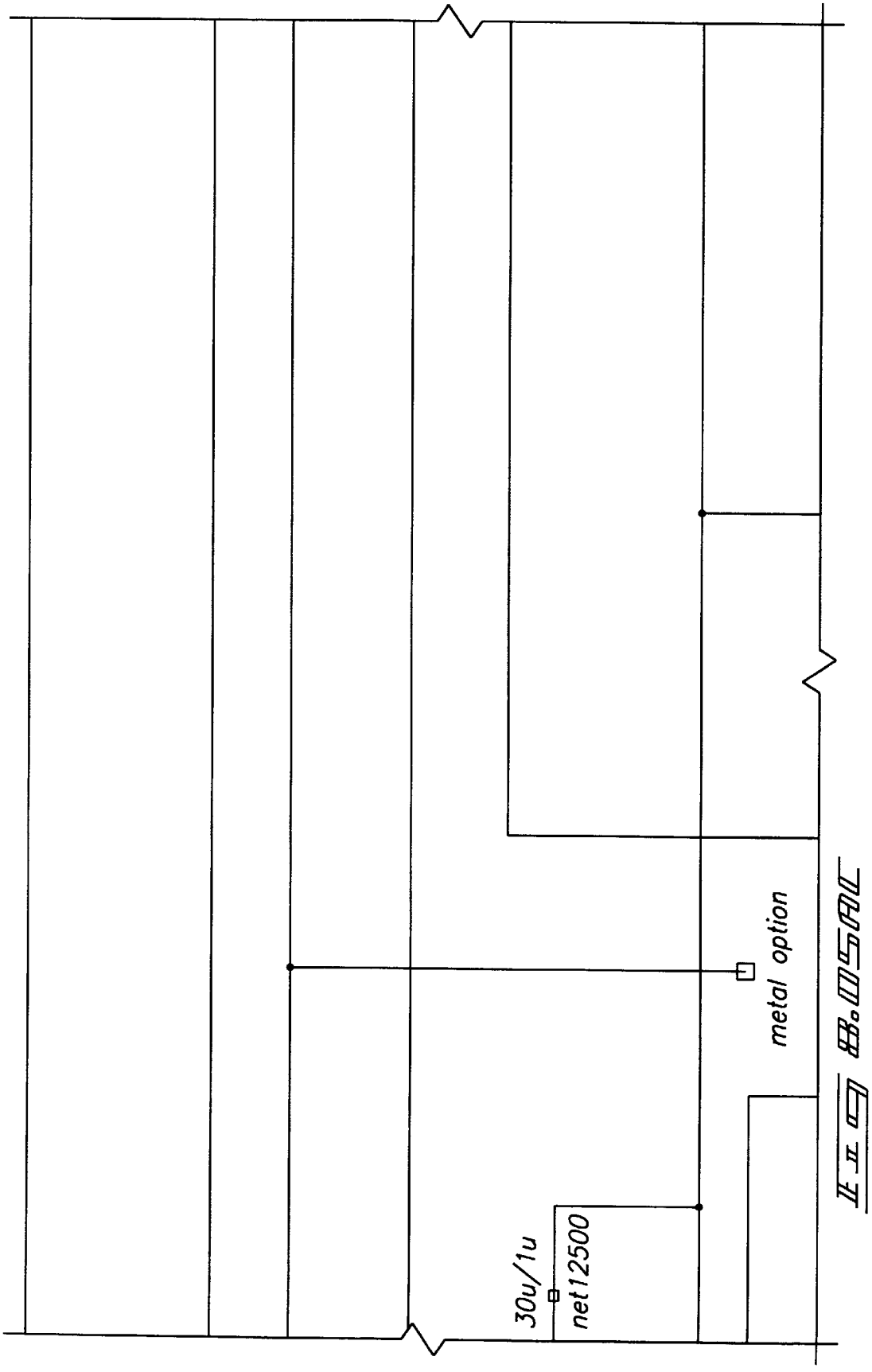

PROCON
net5023
6u/1u
18u/1u
net5023
I98
nor2
net4999
PWRUP
6u/1u
18u/1u
net4999
I83
nor2
RFENABLE
RXENABLE
6u/1u
PROCON
RFENABLE
RXENABLE
PWRUP
BiasOk

FIG. 88.0514A


I87
nor2
18u/1u
net5002
20u/1u
net5002
I88
30u/1u
ENMBS
metal option
I91
nand3
6u/1u
net5036
16u/1u
net5036
I92
24u/1u
RXEN
net5023
net5075
net5075
12u/1u
I90
30u/1u
net5052
ENMBS
20u/1u
I107
nand2
6u/1u
net12476
6u/1u
net12476
I108
9u/1u
net12453
I109
net12453
20u/1u
ENMBS
BiasOK
8u/1u


metal option
30u/1u
net12500

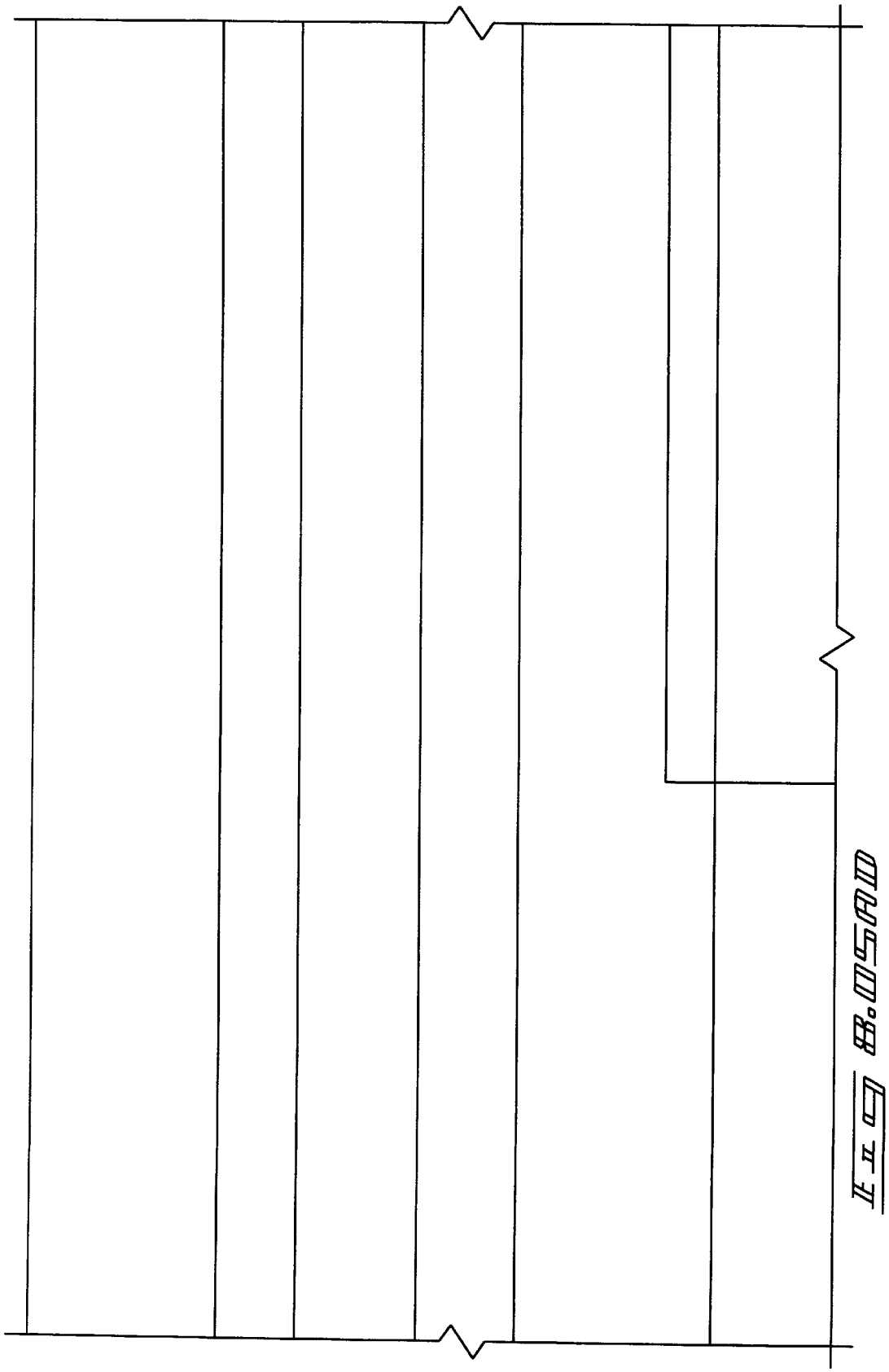


FIG 88.0580

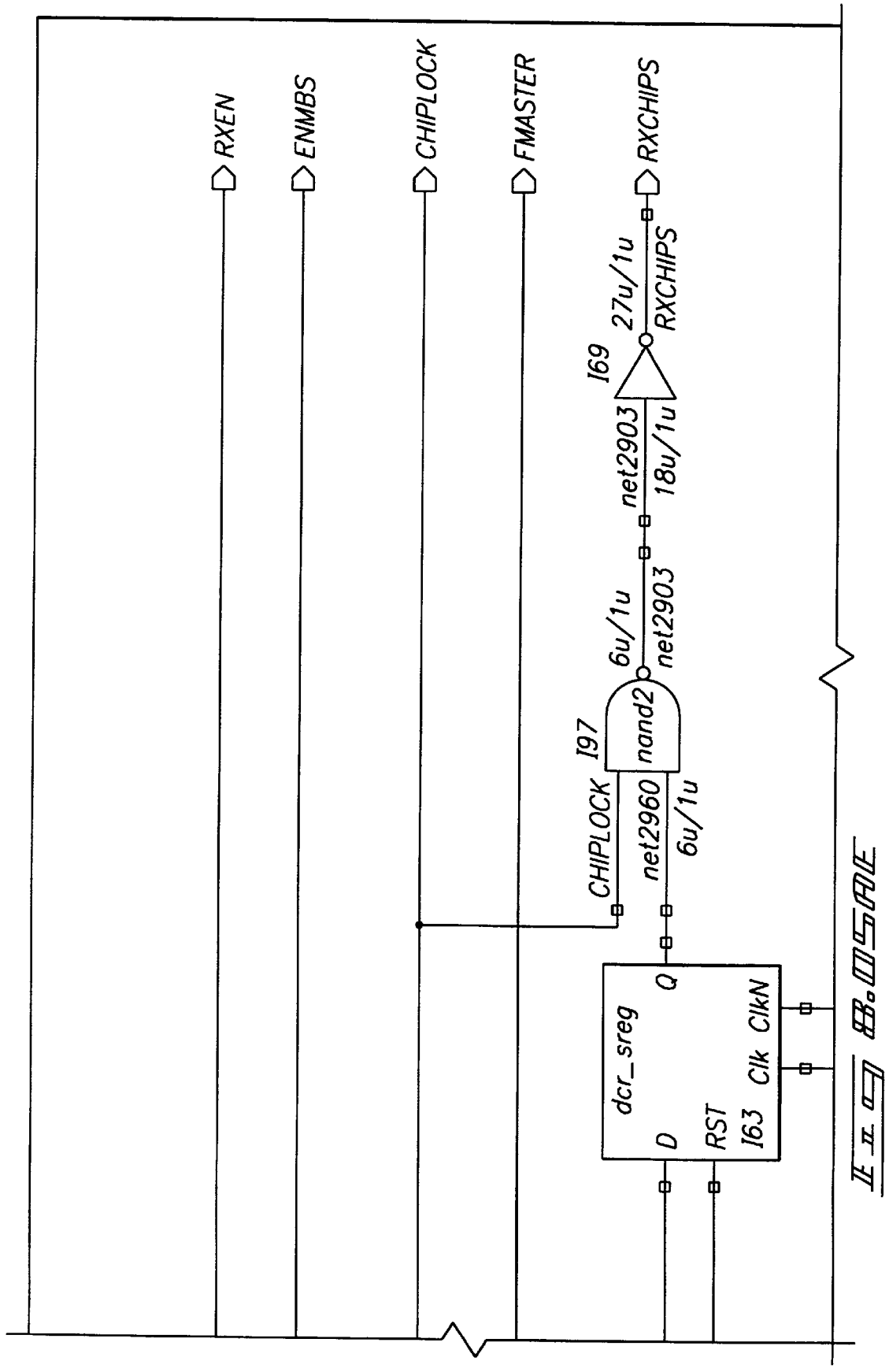
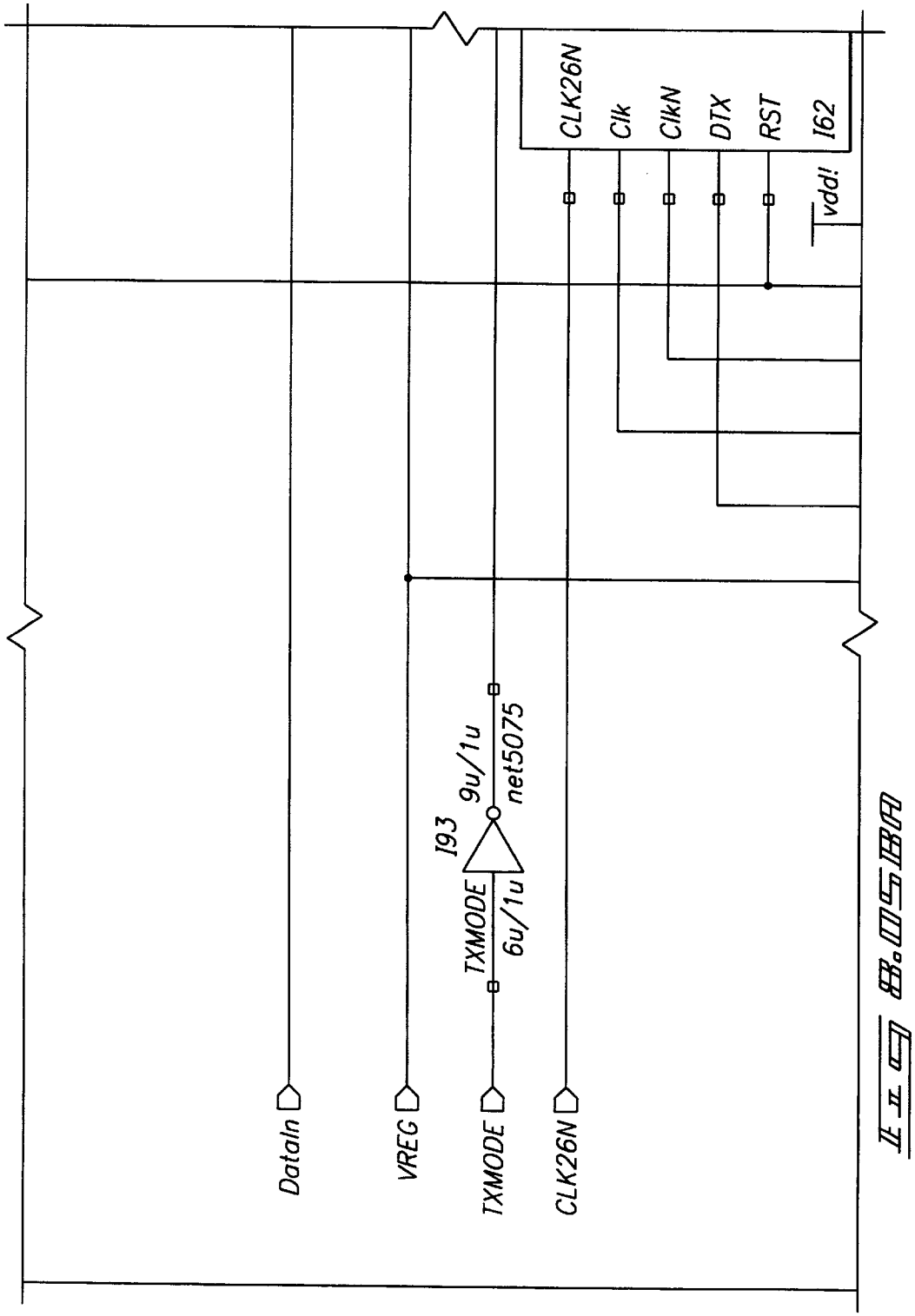
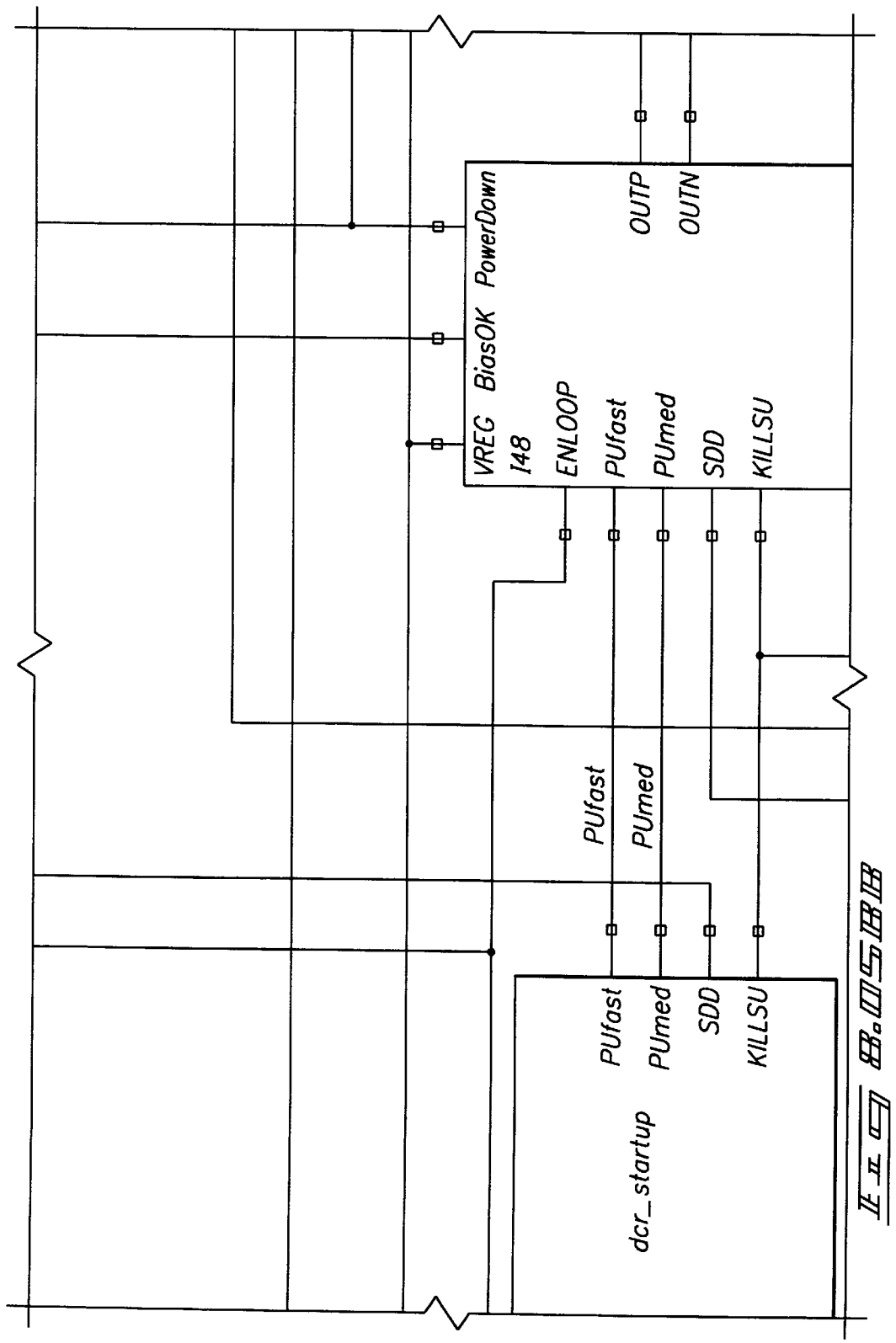

RXEN
ENMBS
CHIPLOCK
FMASTER
RXCHIPS
I69
27u/1u
RXCHIPS
net2903
18u/1u
net2903
6u/1u
I97
nand2
CHIPLOCK
net2960
6u/1u
dcr_sreg
Q
D
RST
I63
Clk
ClkN

FIG. 88.05ADE


CLK26N
Clk
ClkN
DTX
RST
I62
vdd!
I93
9u/1u
net5075
TXMODE
6u/1u
DataIn
VREG
TXMODE
CLK26N


VREG
BiasOK
PowerDown
I48
ENLOOP
PUfast
PUmed
SDD
KILLSU
OUTP
OUTN
PUfast
PUmed
PUfast
PUmed
SDD
KILLSU
dcr_startup

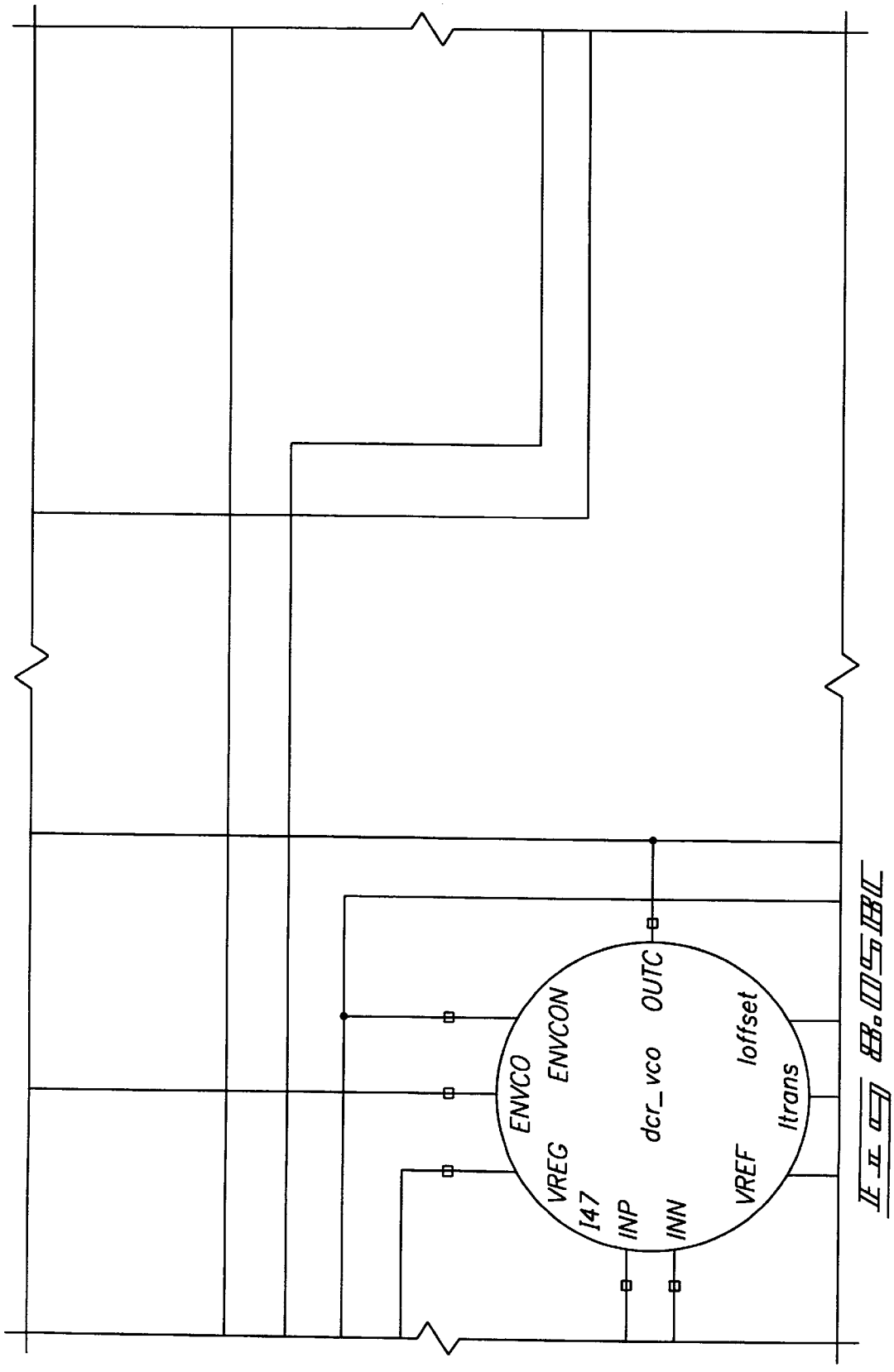

ENVCO
ENVCON
OUTC
loffset
dcr_vco
Itrans
VREG
147
INP
INN
VREF

FIG. 1453

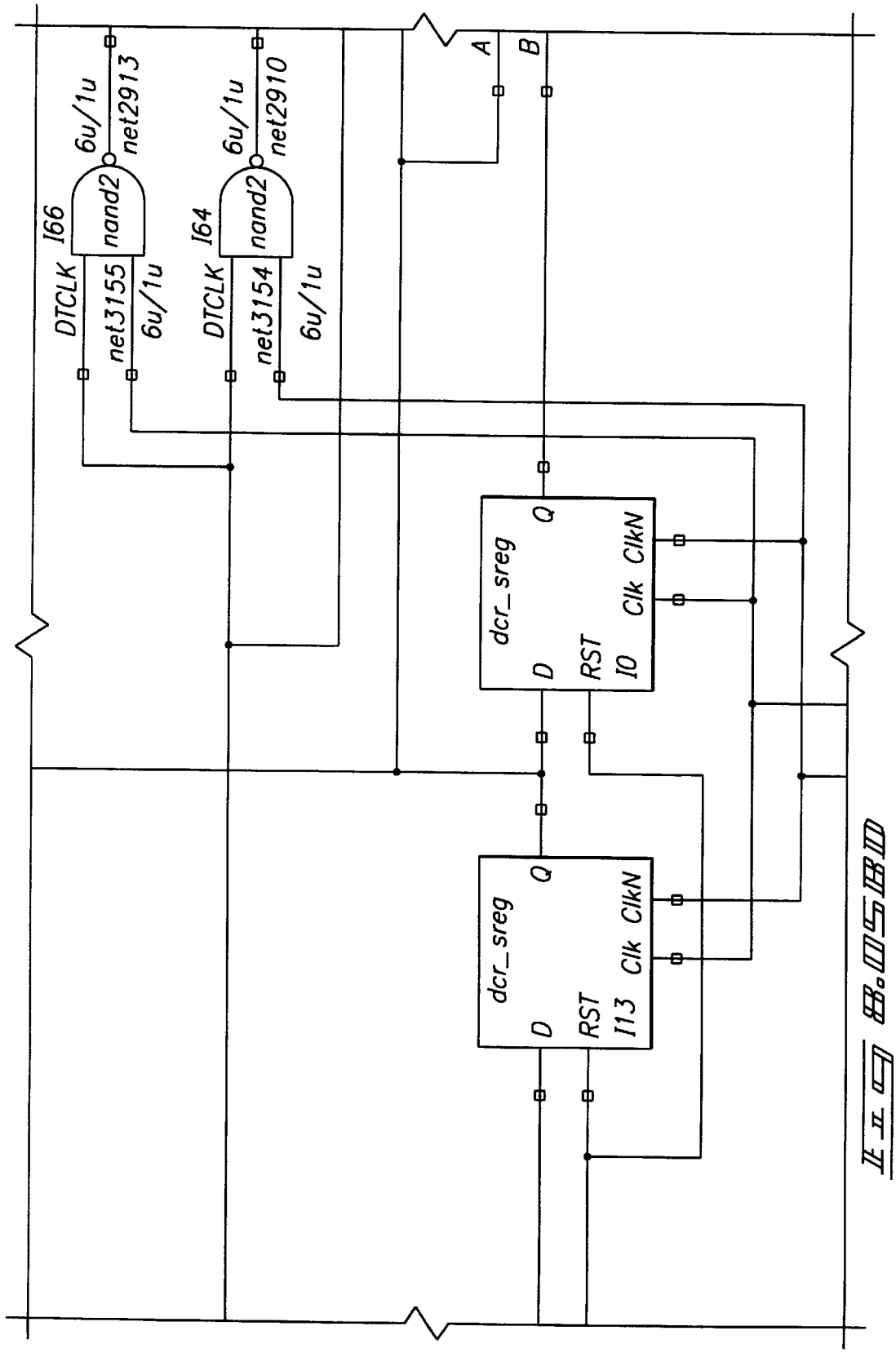
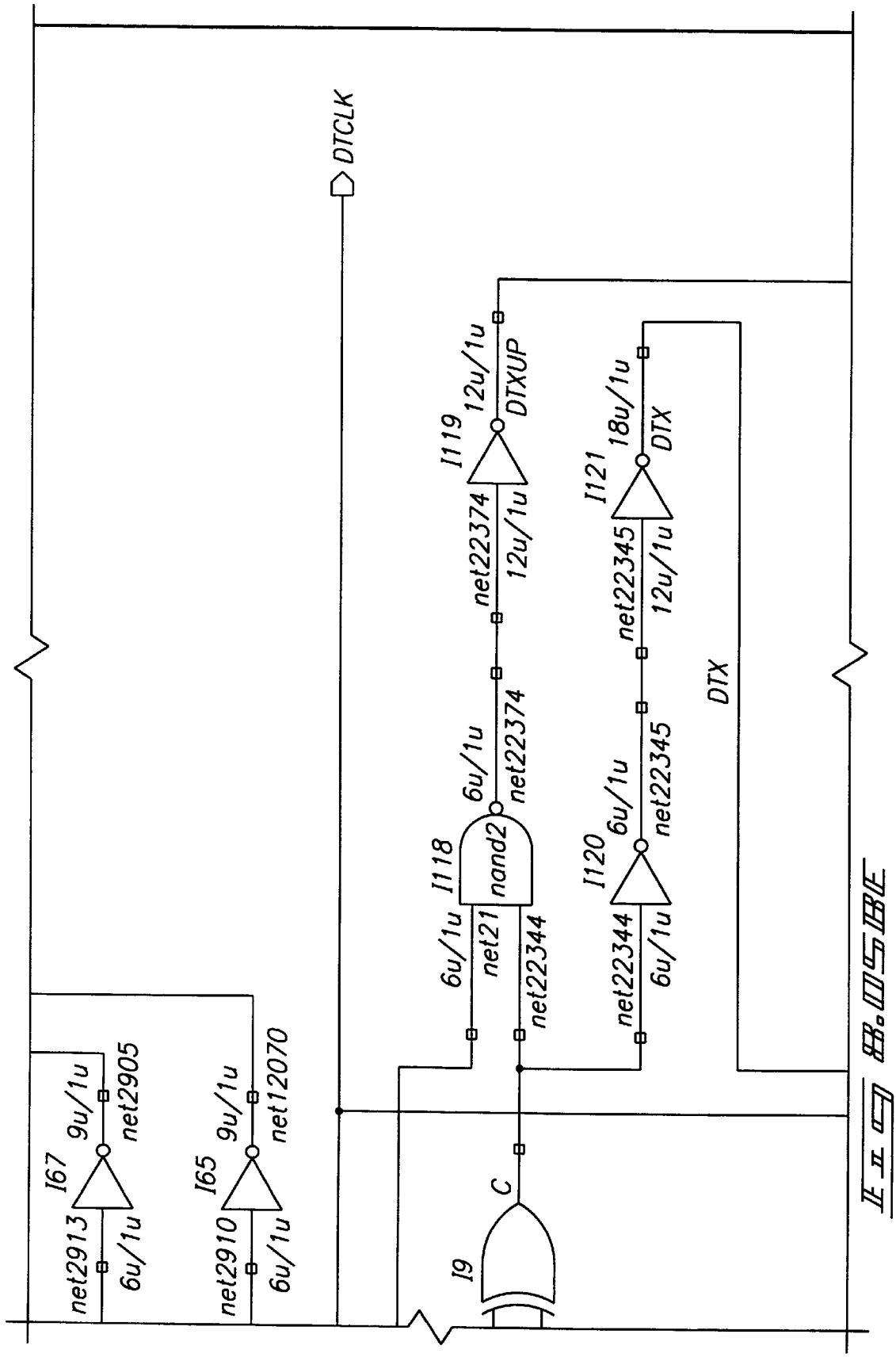

I66
nand2
6u/1u
net2913
DTCLK
net3155
6u/1u
I64
nand2
6u/1u
net2910
DTCLK
net3154
6u/1u
A
B
dcr_sreg
Q
D
RST
I0
Clk
ClkN
dcr_sreg
Q
D
RST
I13
Clk
ClkN

FIG 88.0058


DTCLK
I119
12u/1u
DTXUP
net22374
12u/1u
I121
18u/1u
DTX
net22345
12u/1u
DTX
6u/1u
net22374
I118
nand2
6u/1u
net21
6u/1u
net22344
I120
6u/1u
net22345
net22344
6u/1u
C
I9
I67
9u/1u
net2905
net2913
6u/1u
I65
9u/1u
net12070
net2910
6u/1u

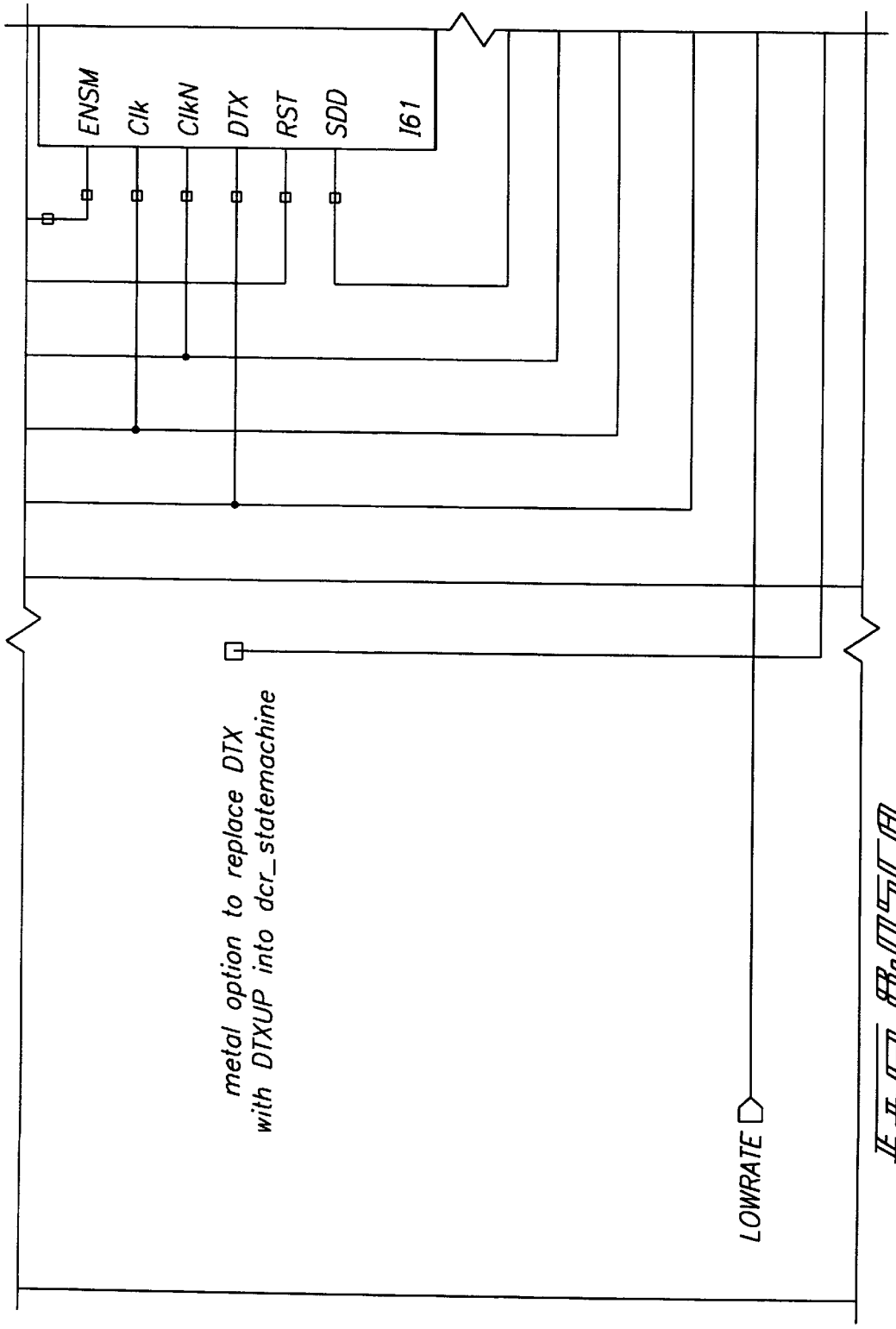

ENSM
Clk
ClkN
DTX
RST
SDD
I61
metal option to replace DTX
with DTXUP into dcr_statemachine
LOWRATE

FIG 88.0570A

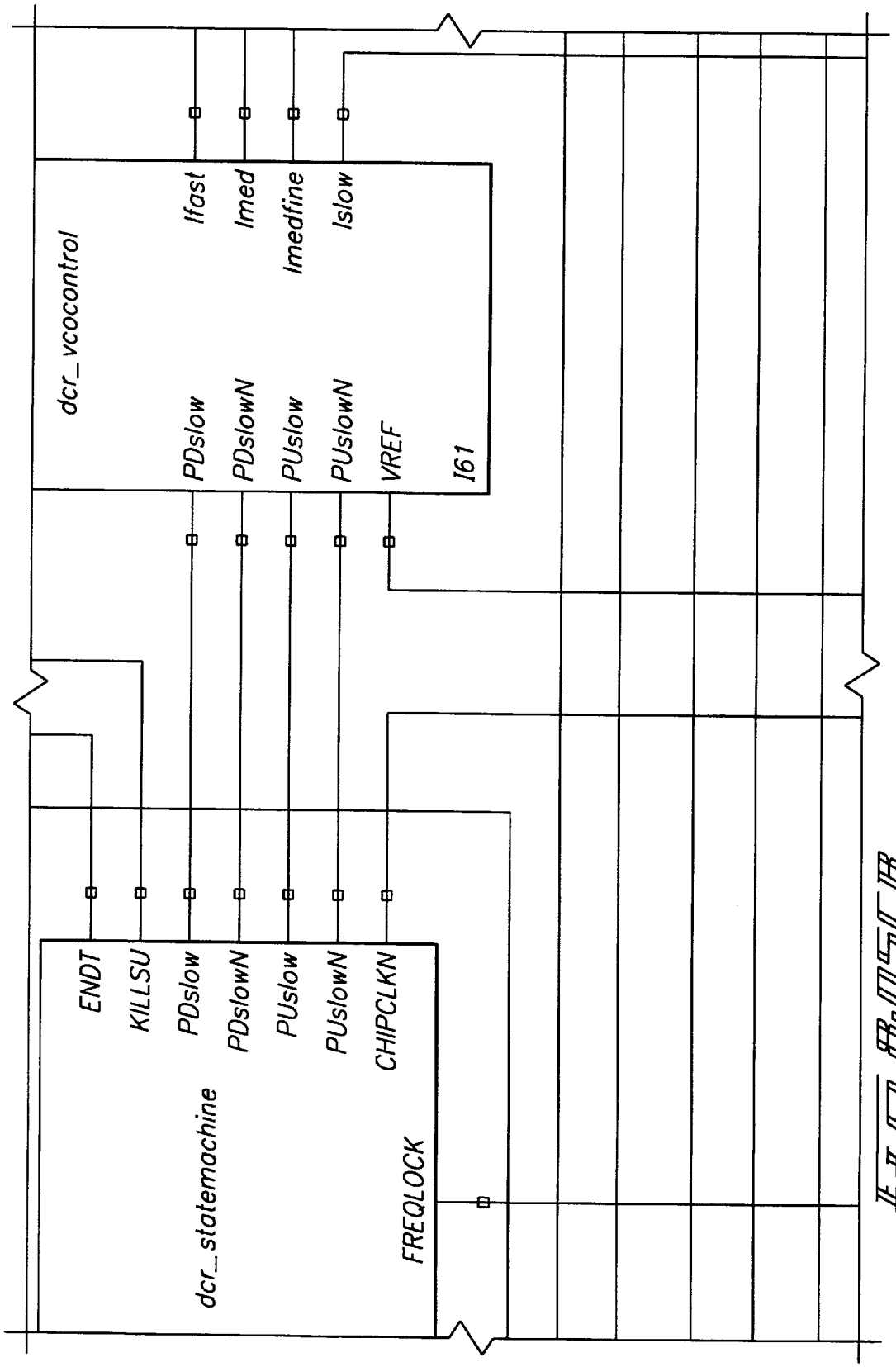

dcr_vcocontrol
Ifast
Imed
Imedfine
Islow
PDslow
PDslowN
PUslow
PUslowN
VREF
I61
dcr_statemachine
ENDT
KILLSU
PDslow
PDslowN
PUslow
PUslowN
CHIPCLKN
FREQLOCK

FIG 88,055

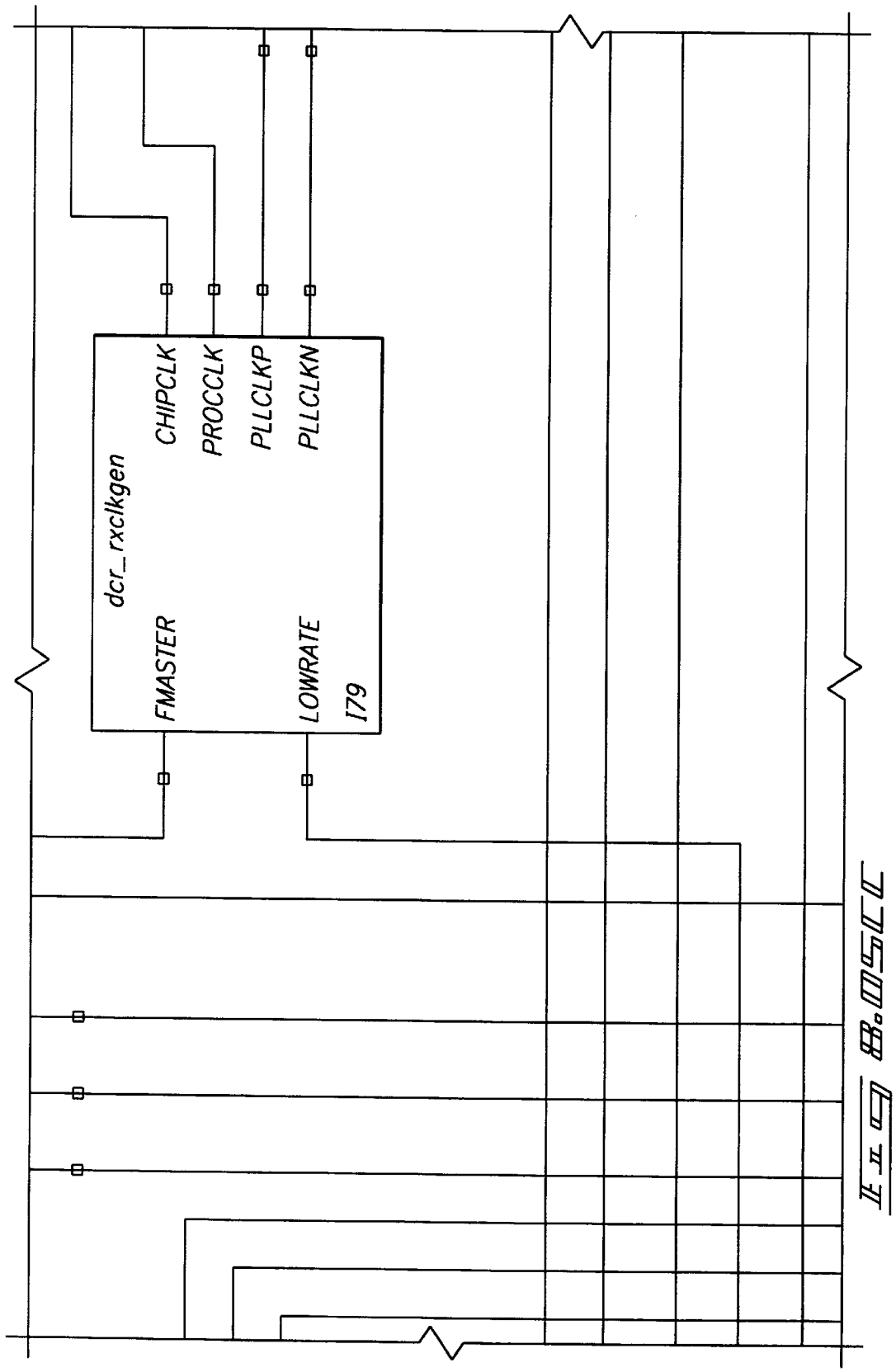
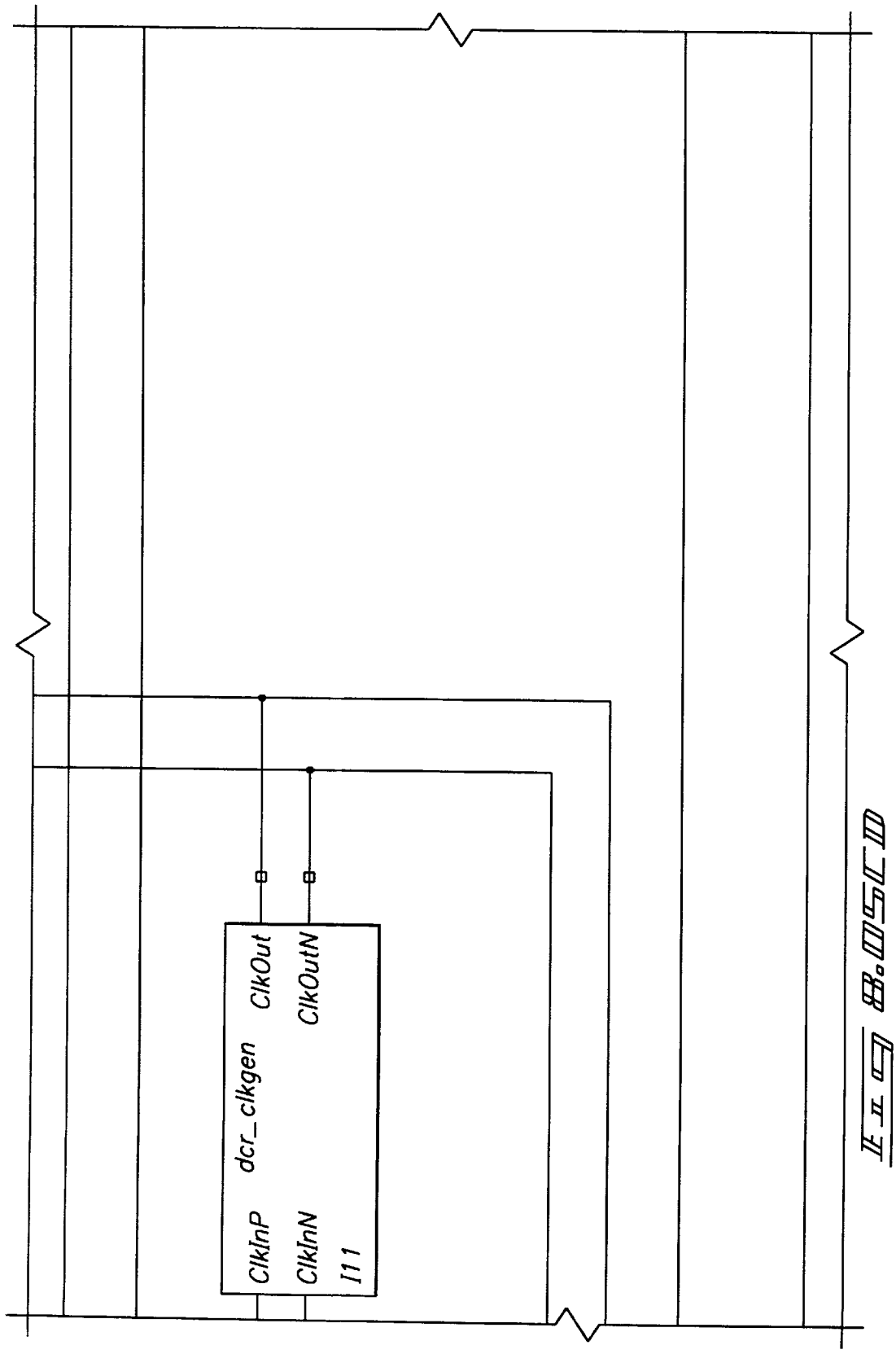
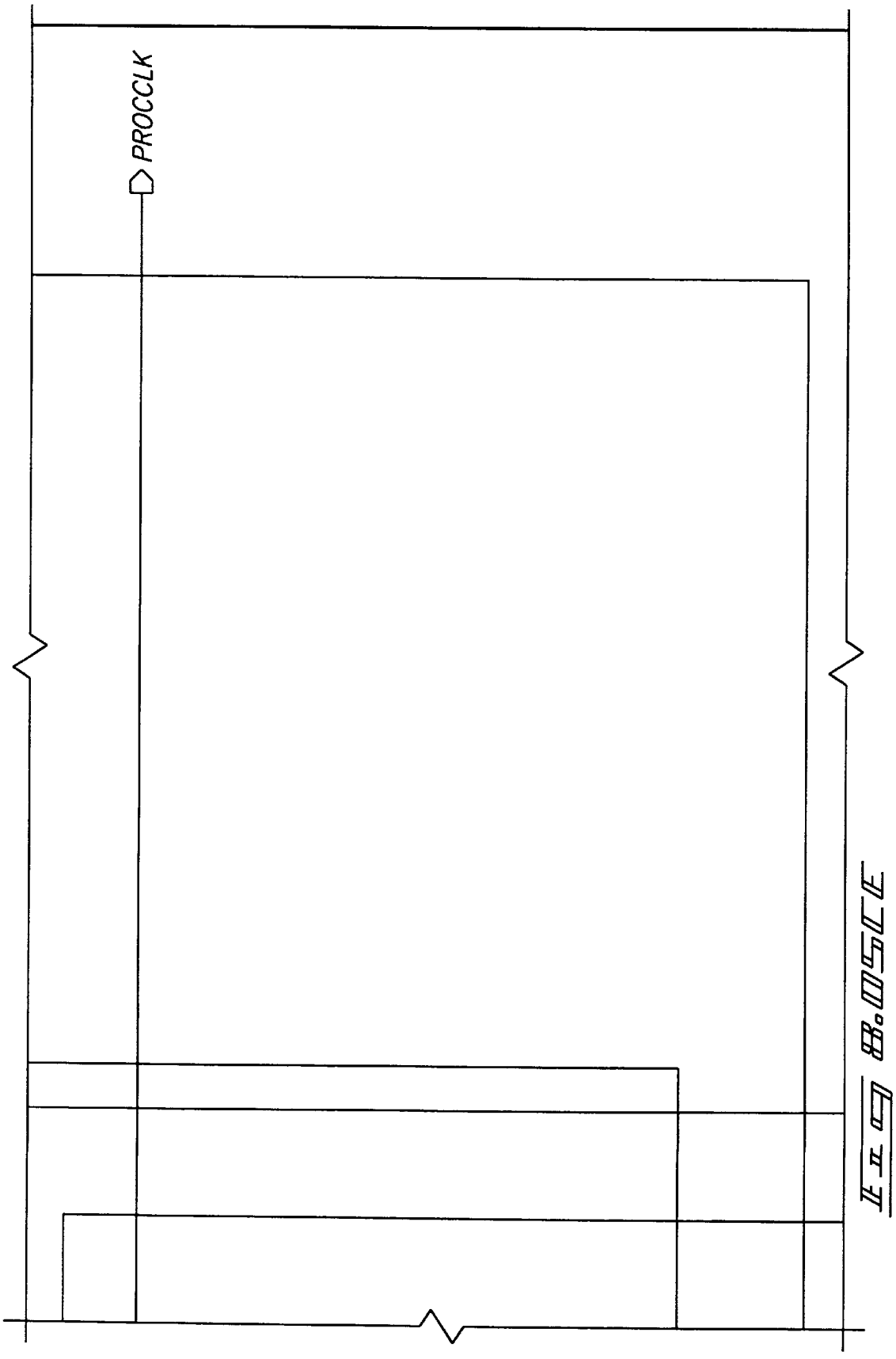
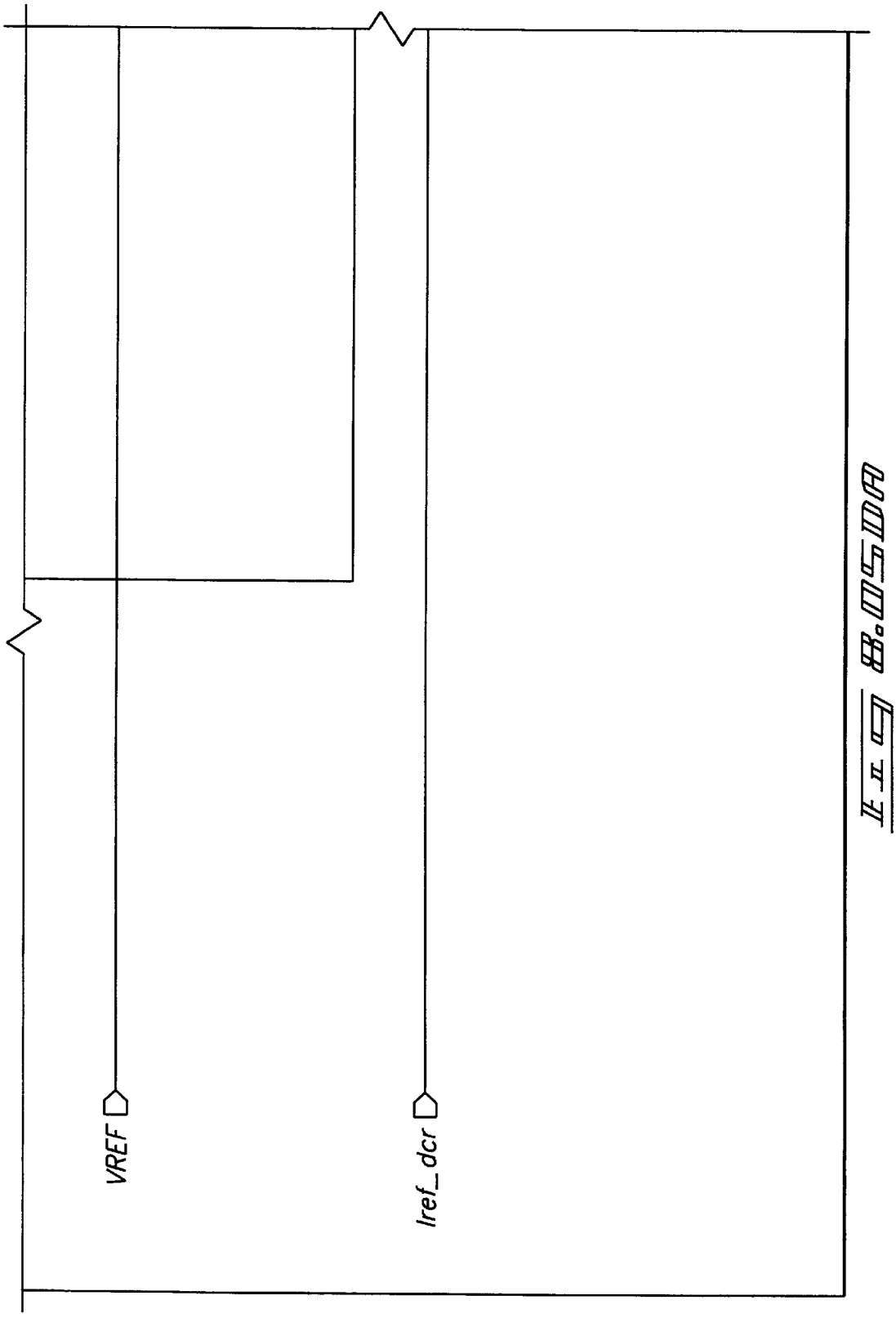

dcr_rxclkgen
CHIPCLK
PROCCLK
PLLCLKP
PLLCLKN
FMASTER
LOWRATE
I79

FIG. 88.0750


dcr_clkgen
ClkOut
ClkOutN
ClkInP
ClkInN
I11
FIG. 1459


PROCCLK
FIG. 98.00578E


VREF
Iref_dcr
FIG 8.0504

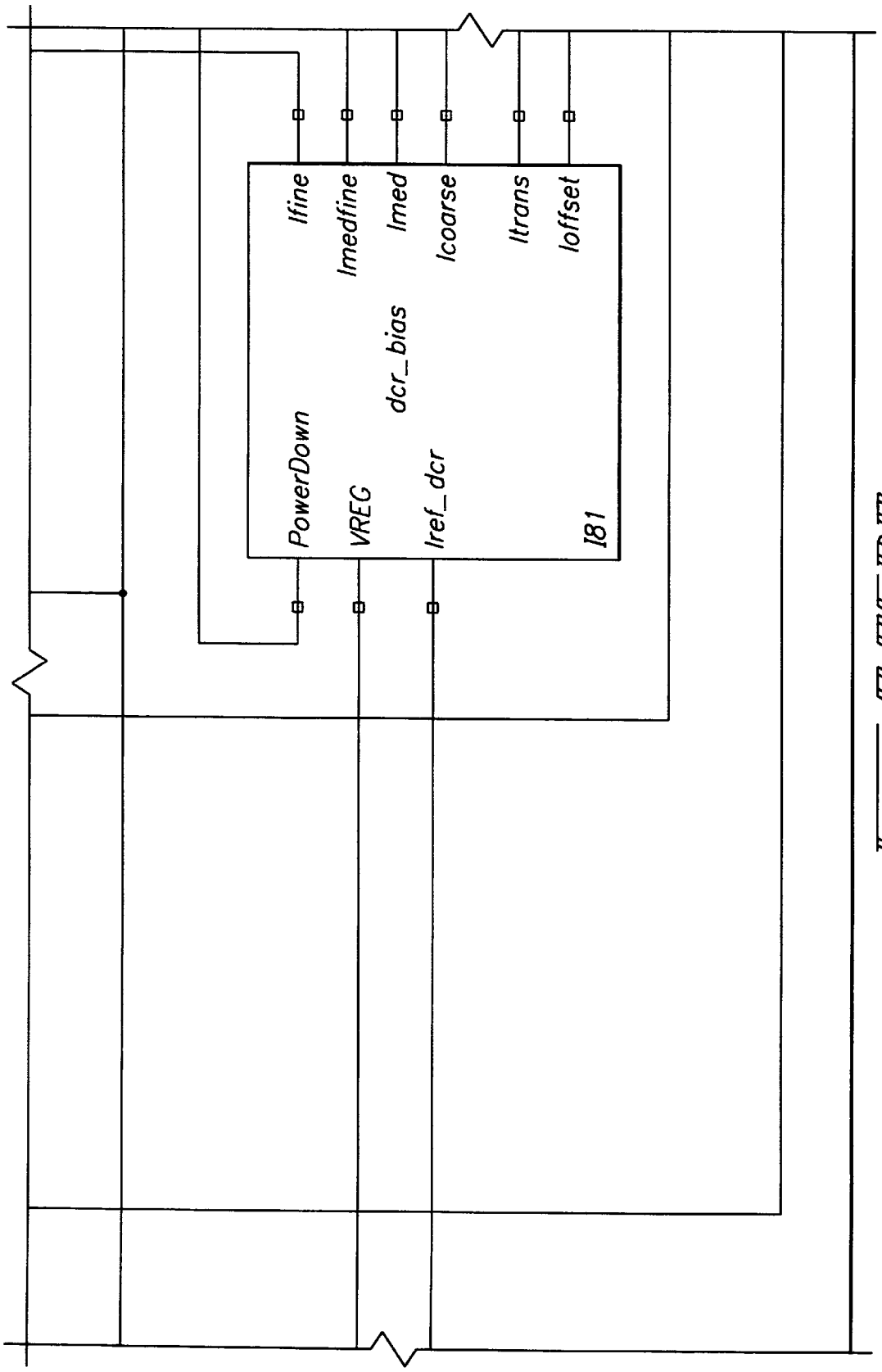


FIG. 88.005.01B

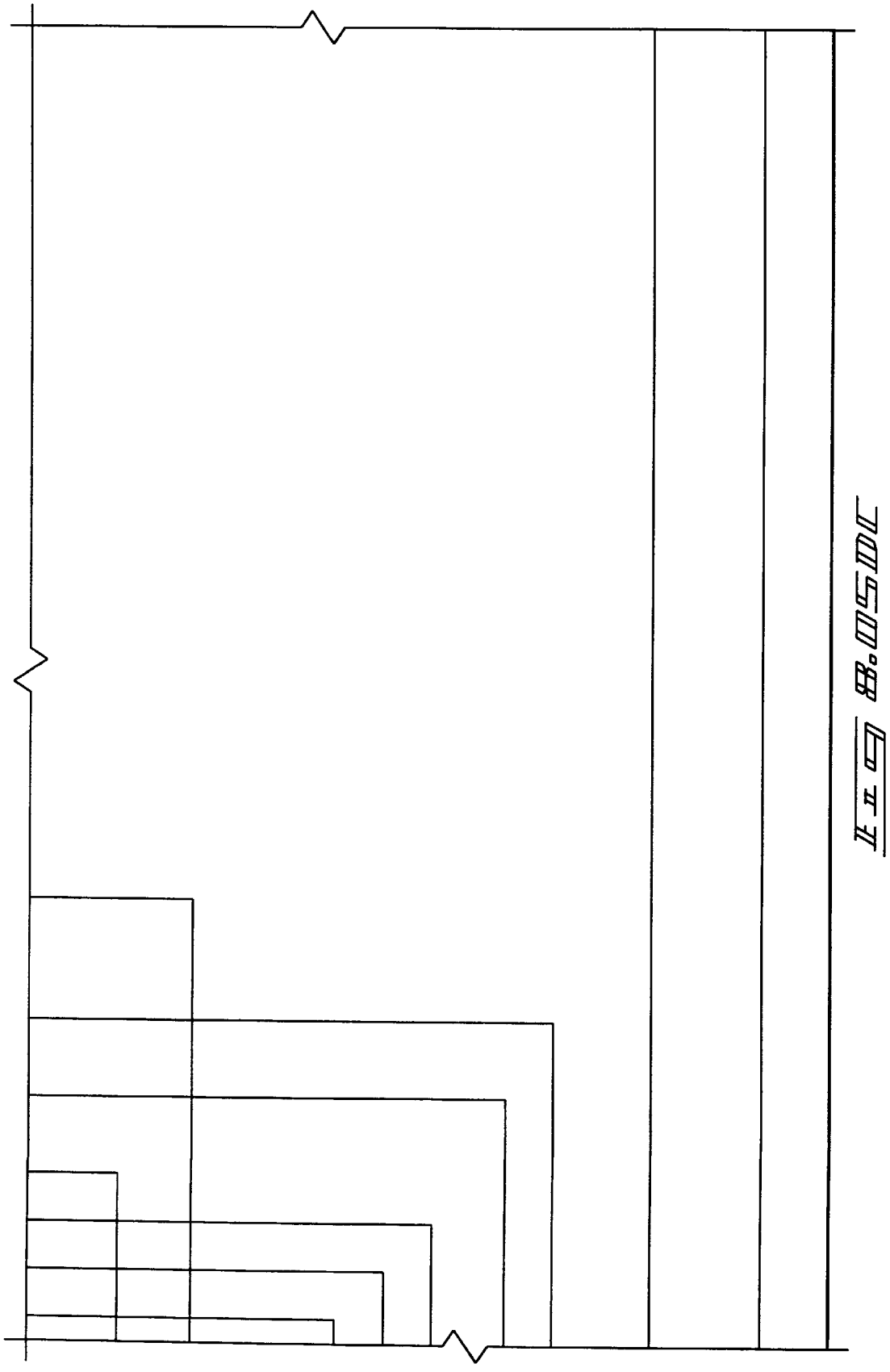


FIG 88.0500

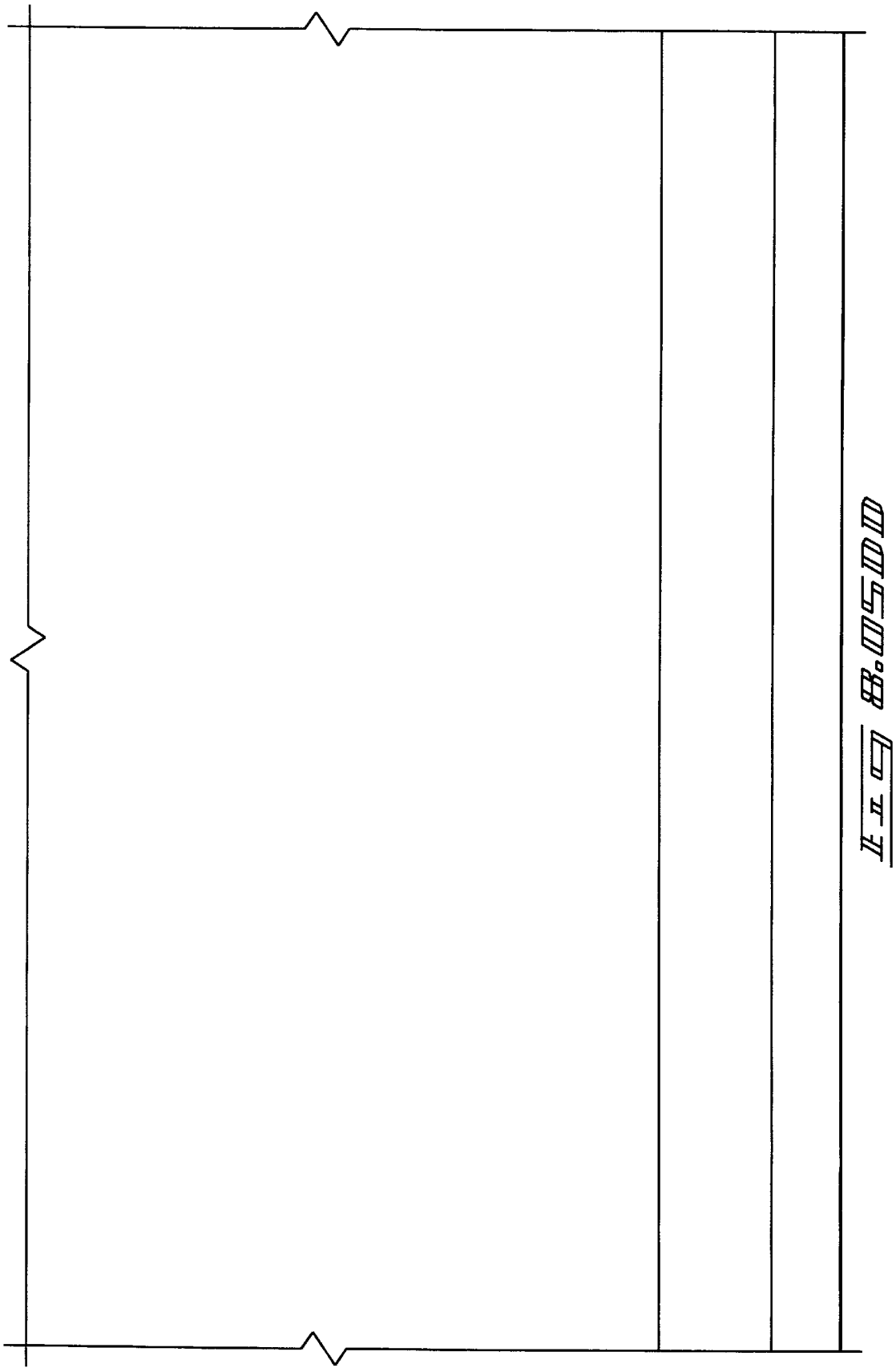


FIG 8,050

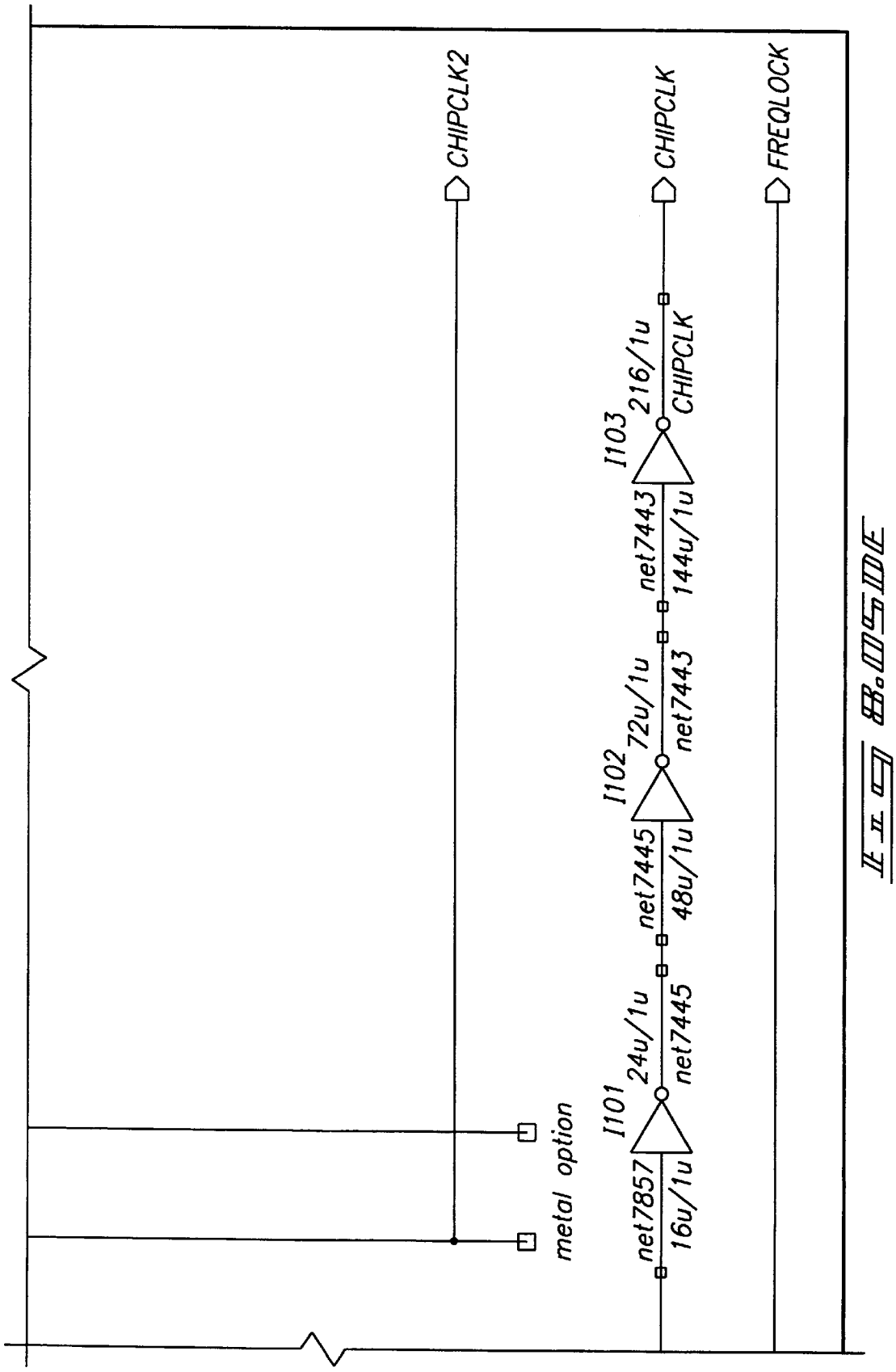


FIG. 88.005IDE

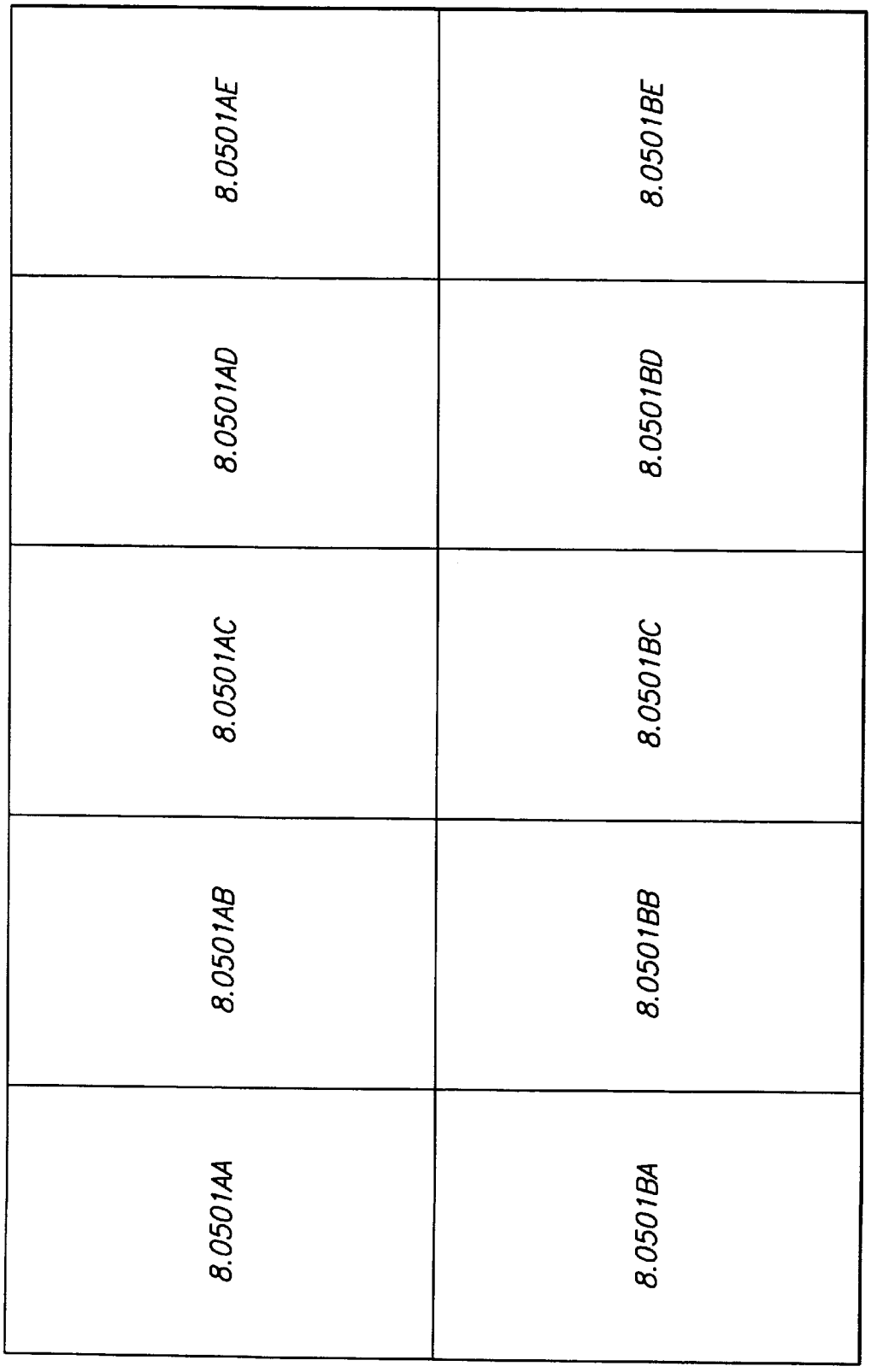
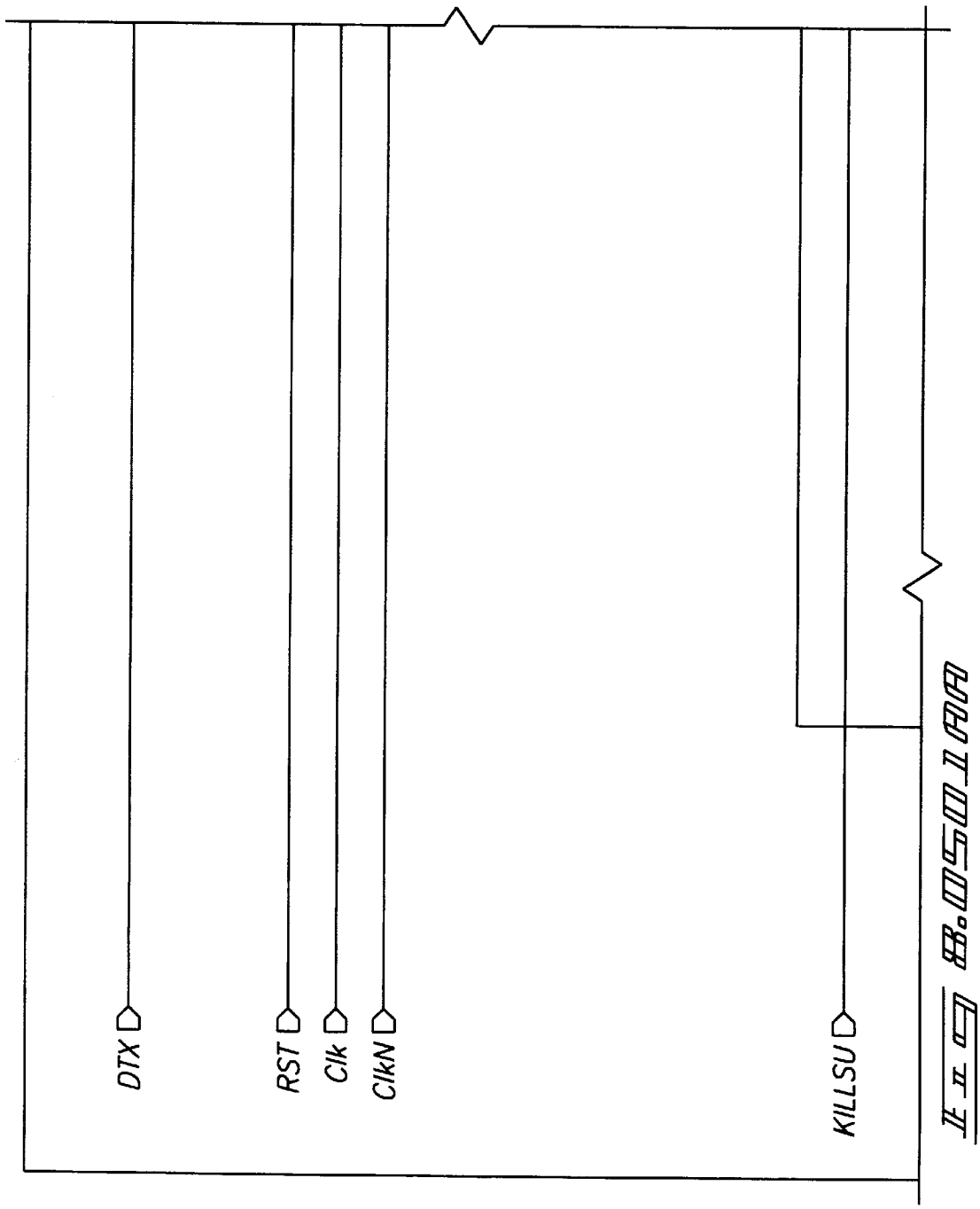
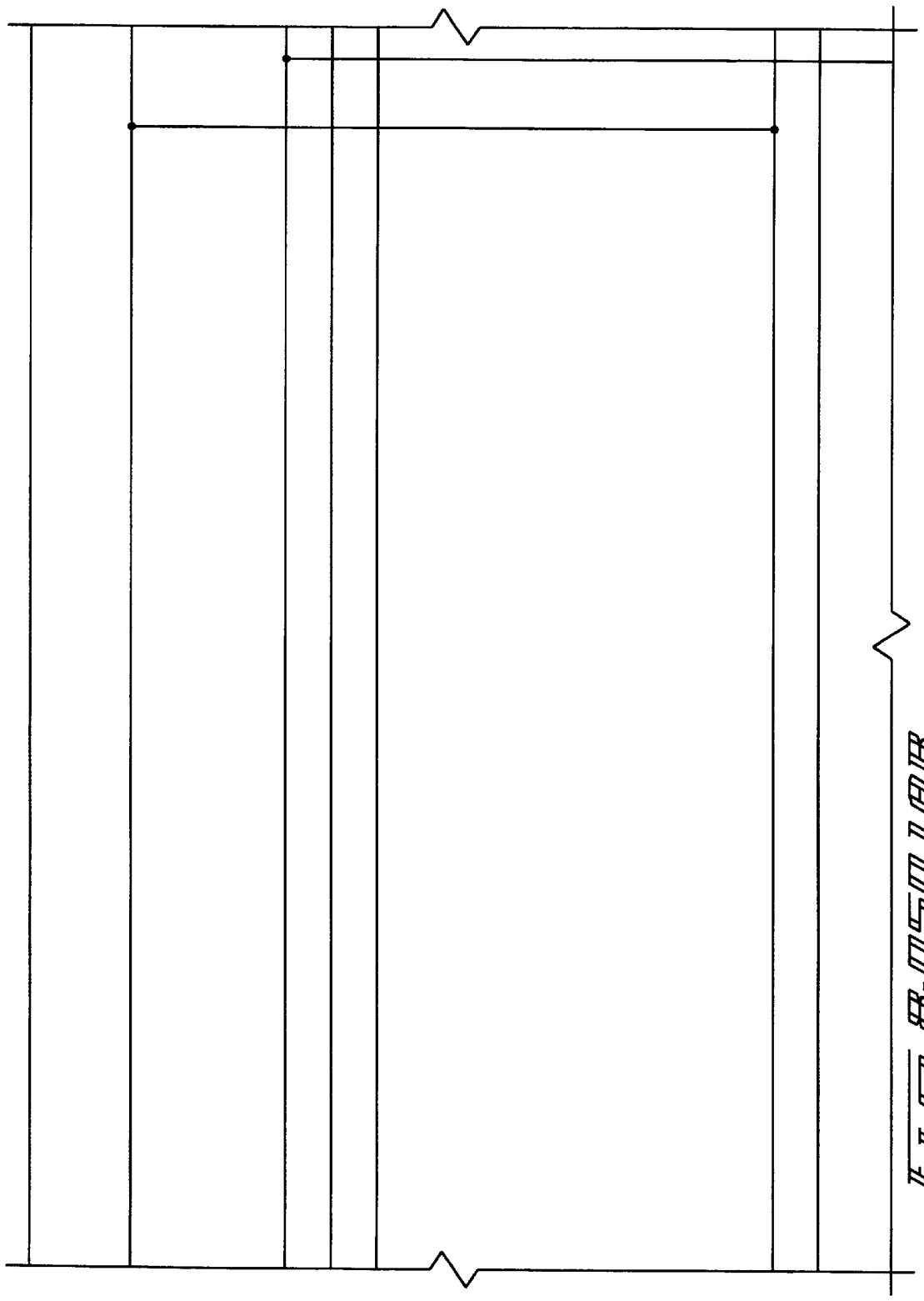
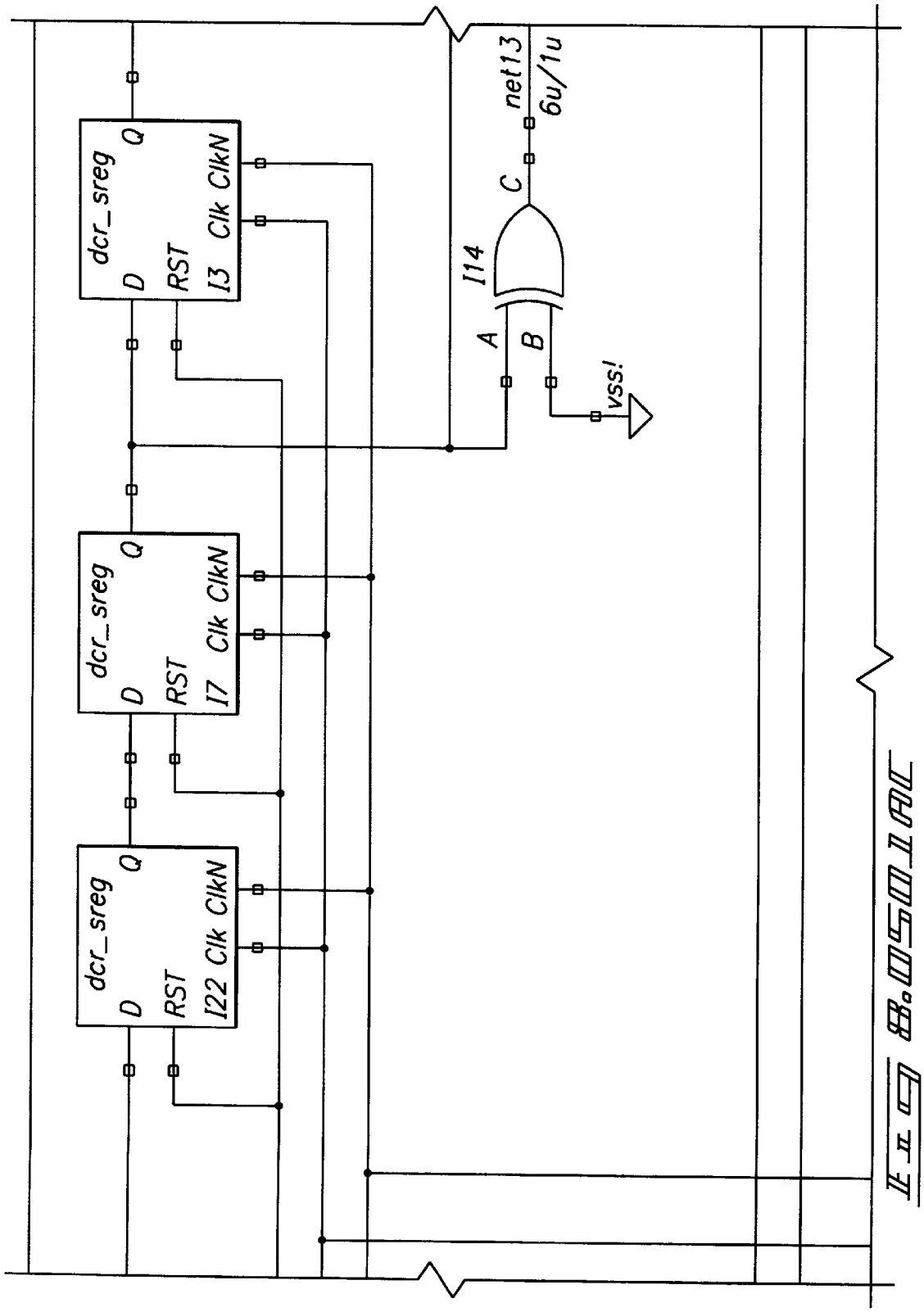

8.0501AE
8.0501BE
8.0501AD
8.0501BD
8.0501AC
8.0501BC
8.0501AB
8.0501BB
8.0501AA
8.0501BA

FIG. 8.0501


DTX
RST
Clk
ClkN
KILLSU
VDD
VSS




dcr_sreg
Q
D
RST
I3 Clk ClkN
dcr_sreg
Q
D
RST
I7 Clk ClkN
dcr_sreg
Q
D
RST
I22 Clk ClkN
I14
A
B
C
net13
6u/1u
vss!
FIG 8.0501AC

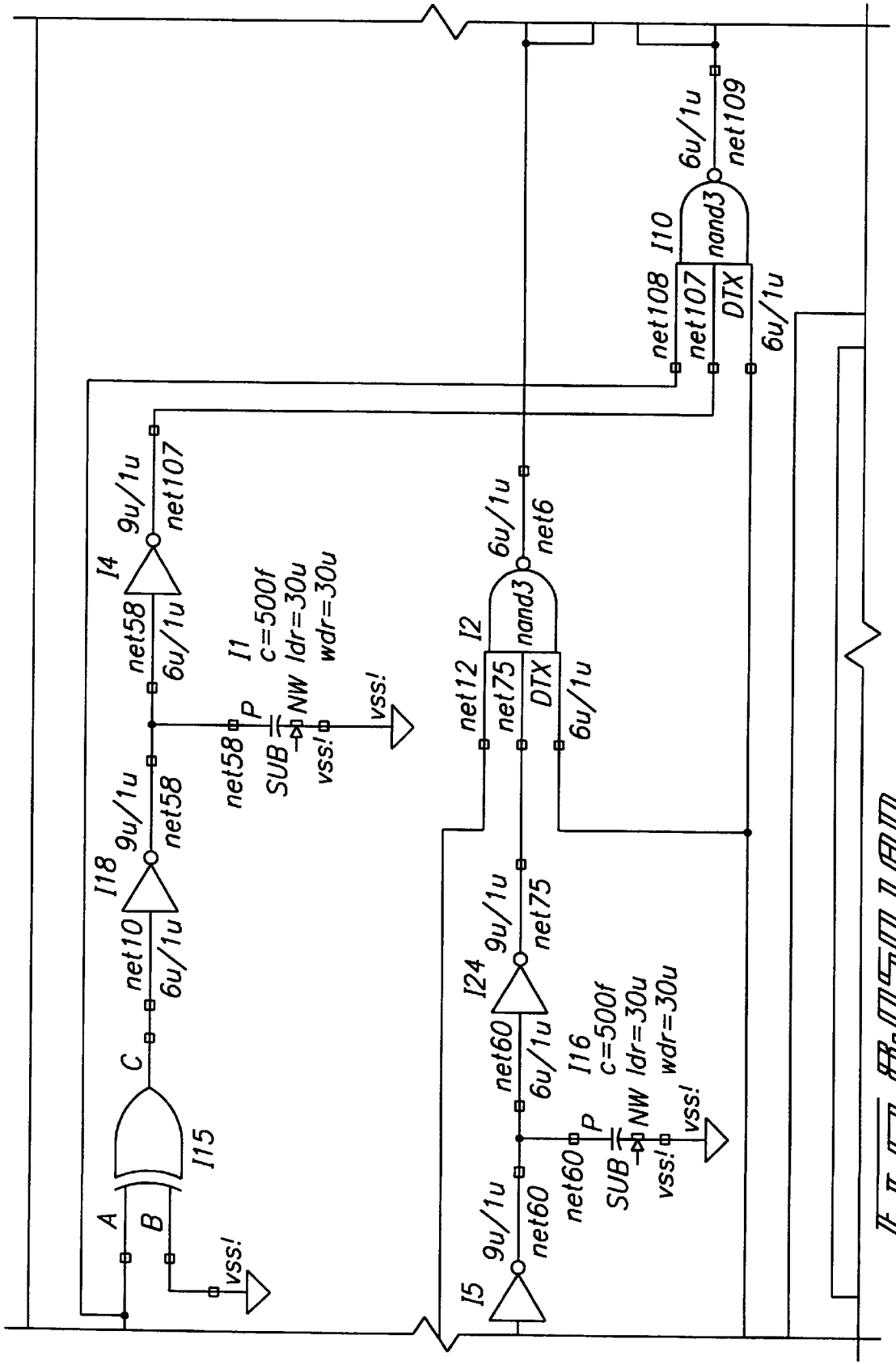
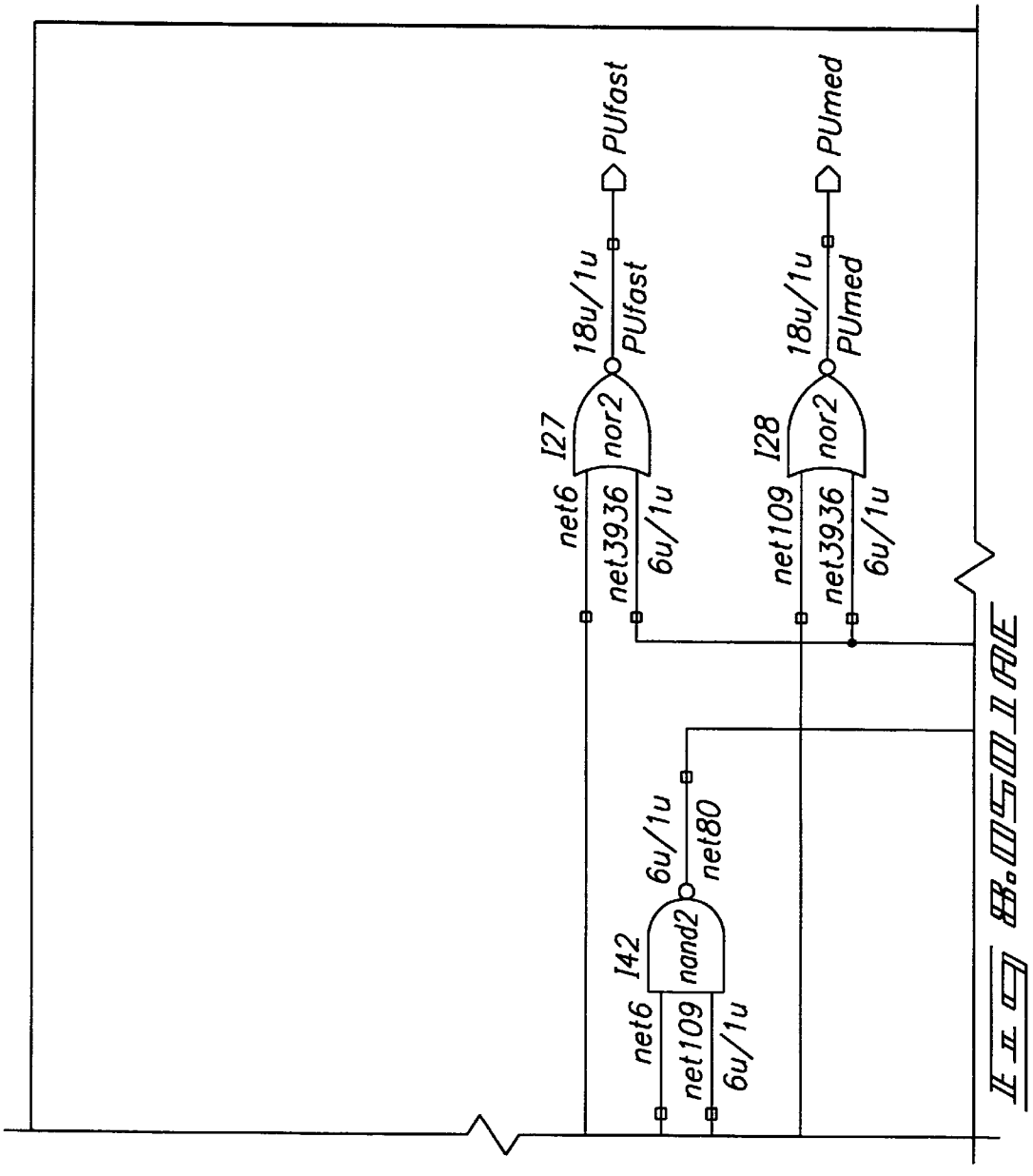


FIG 89. 0SOM ADD


I27
nor2
18u/1u
PUfast
net6
net3936
6u/1u
I28
nor2
18u/1u
PUmed
net109
net3936
6u/1u
I42
nand2
6u/1u
net80
net6
net109
6u/1u

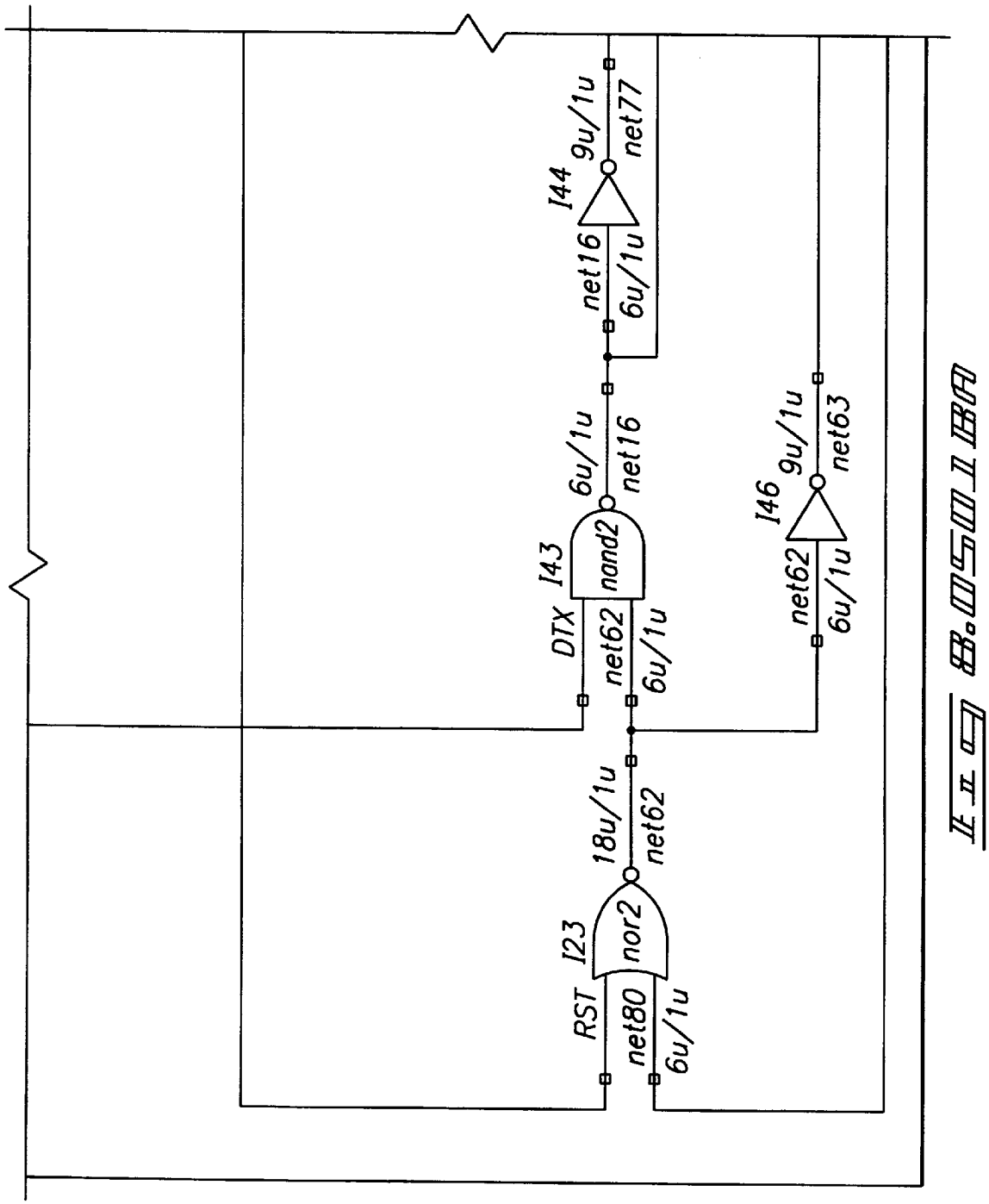

I44
9u/1u
net77
net16
6u/1u
6u/1u
net16
I43
nand2
DTX
net62
6u/1u
I46
9u/1u
net63
net62
6u/1u
18u/1u
net62
I23
nor2
RST
net80
6u/1u

FIG 8.0501 BA

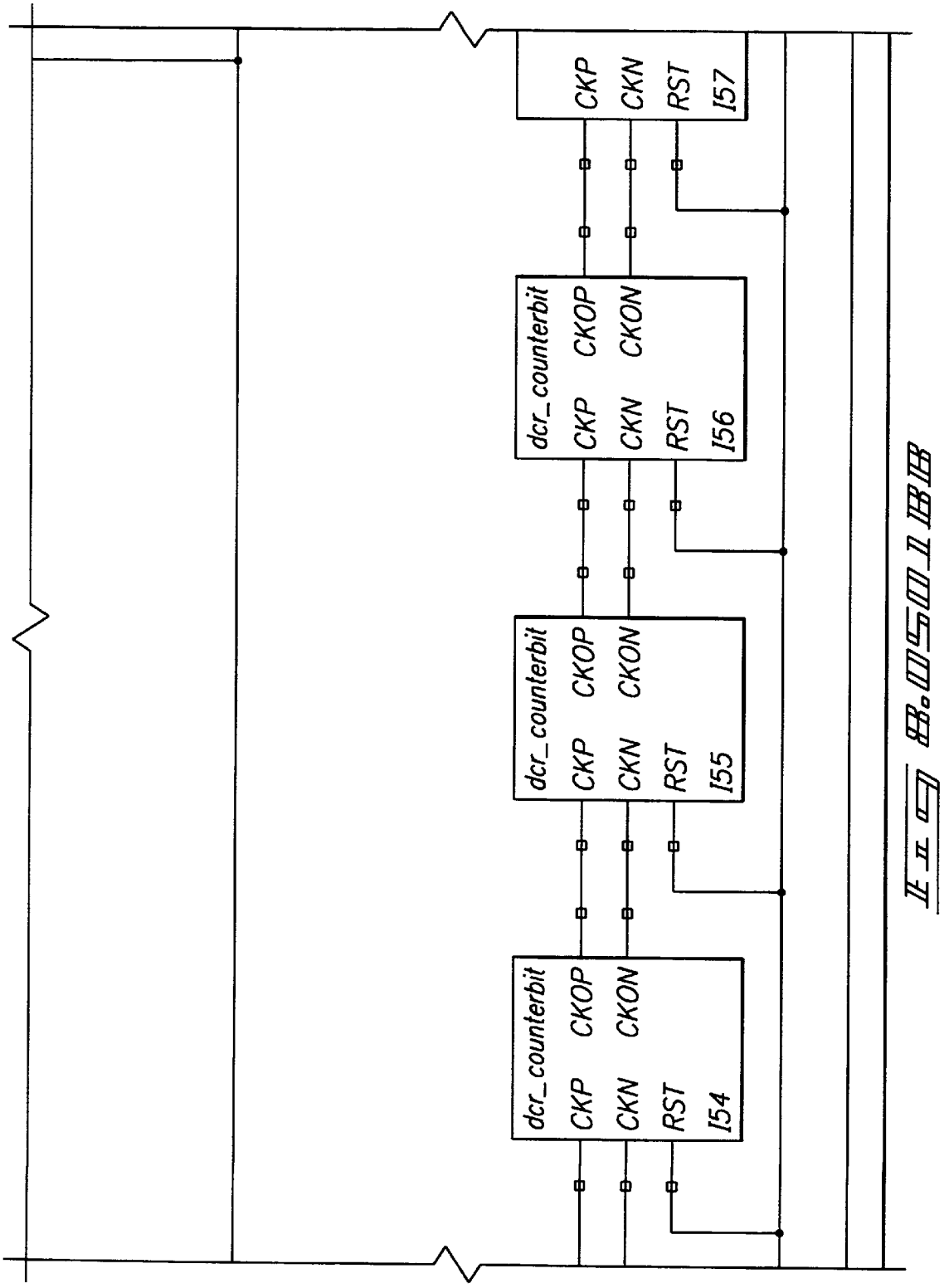


FIG 88.0511B

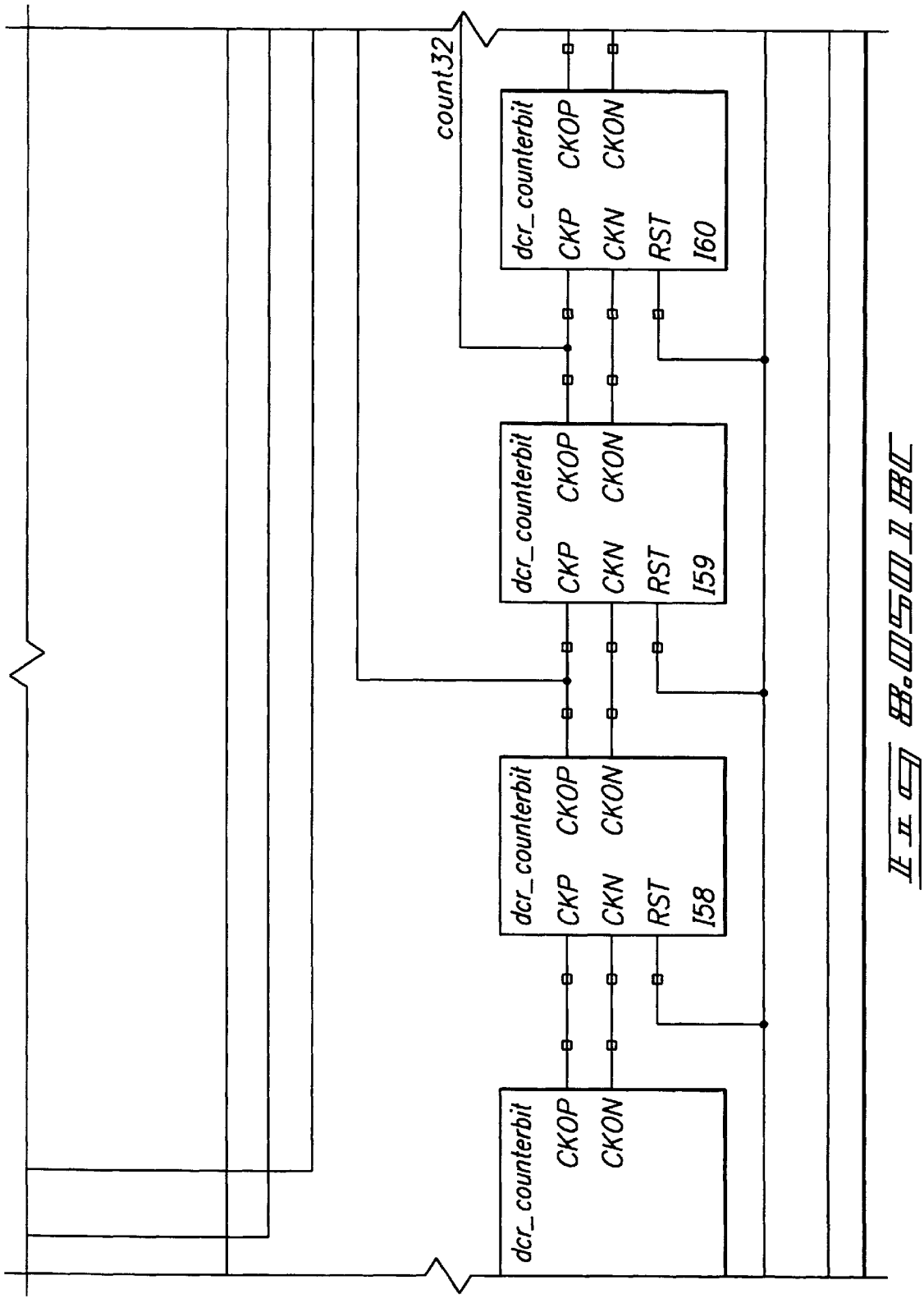


FIG 88.0501 BIT

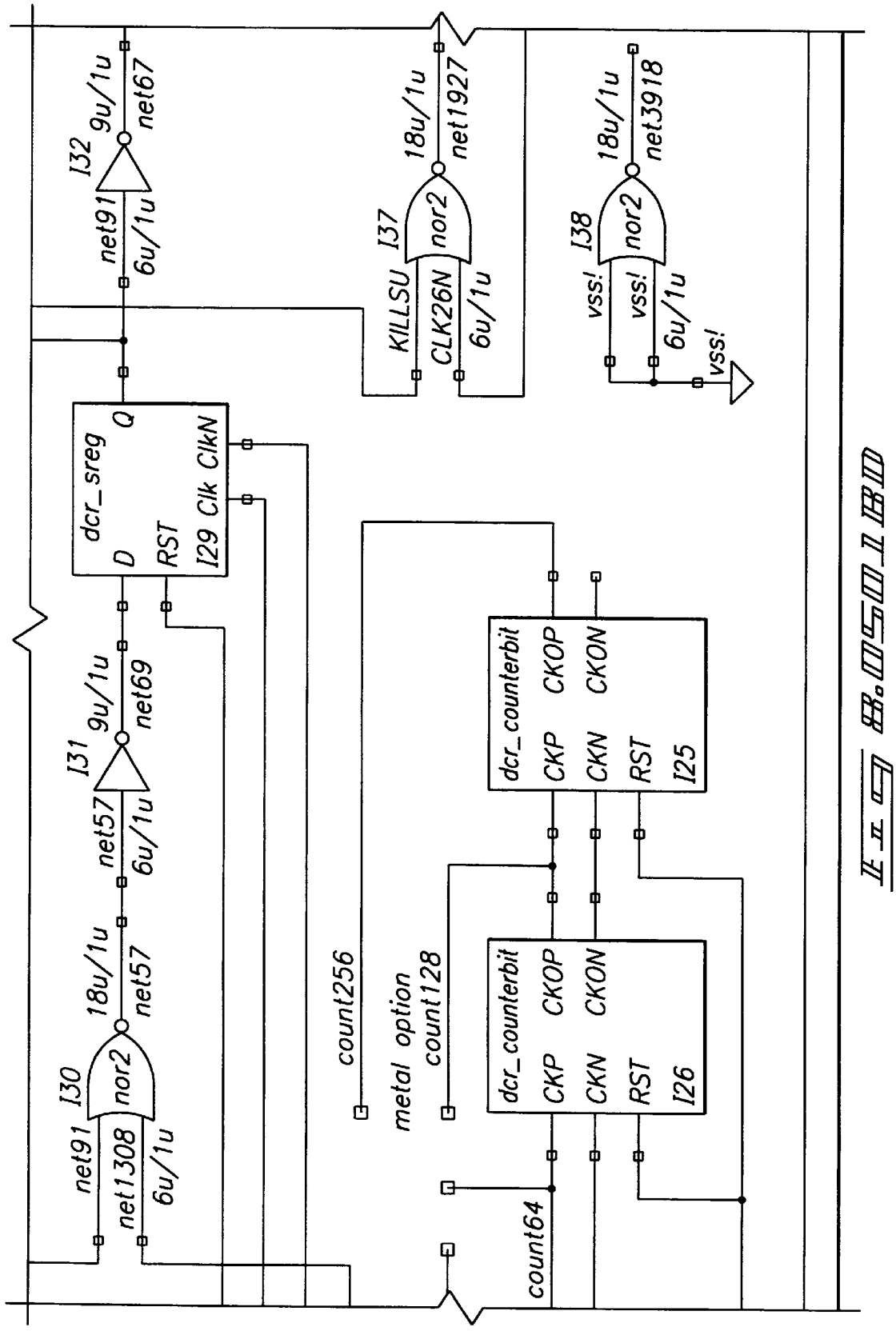


FIG 89.00511 IBM

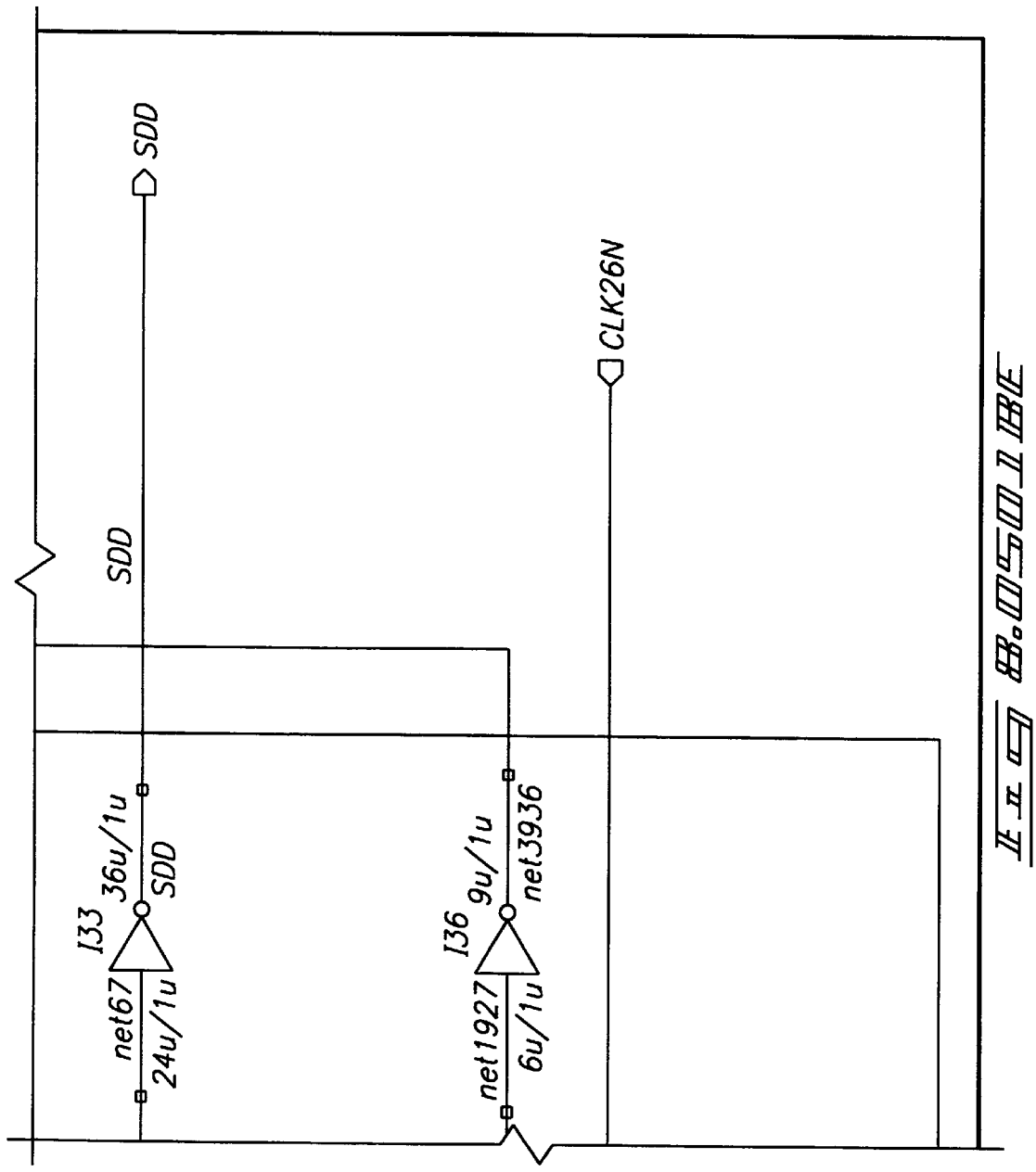
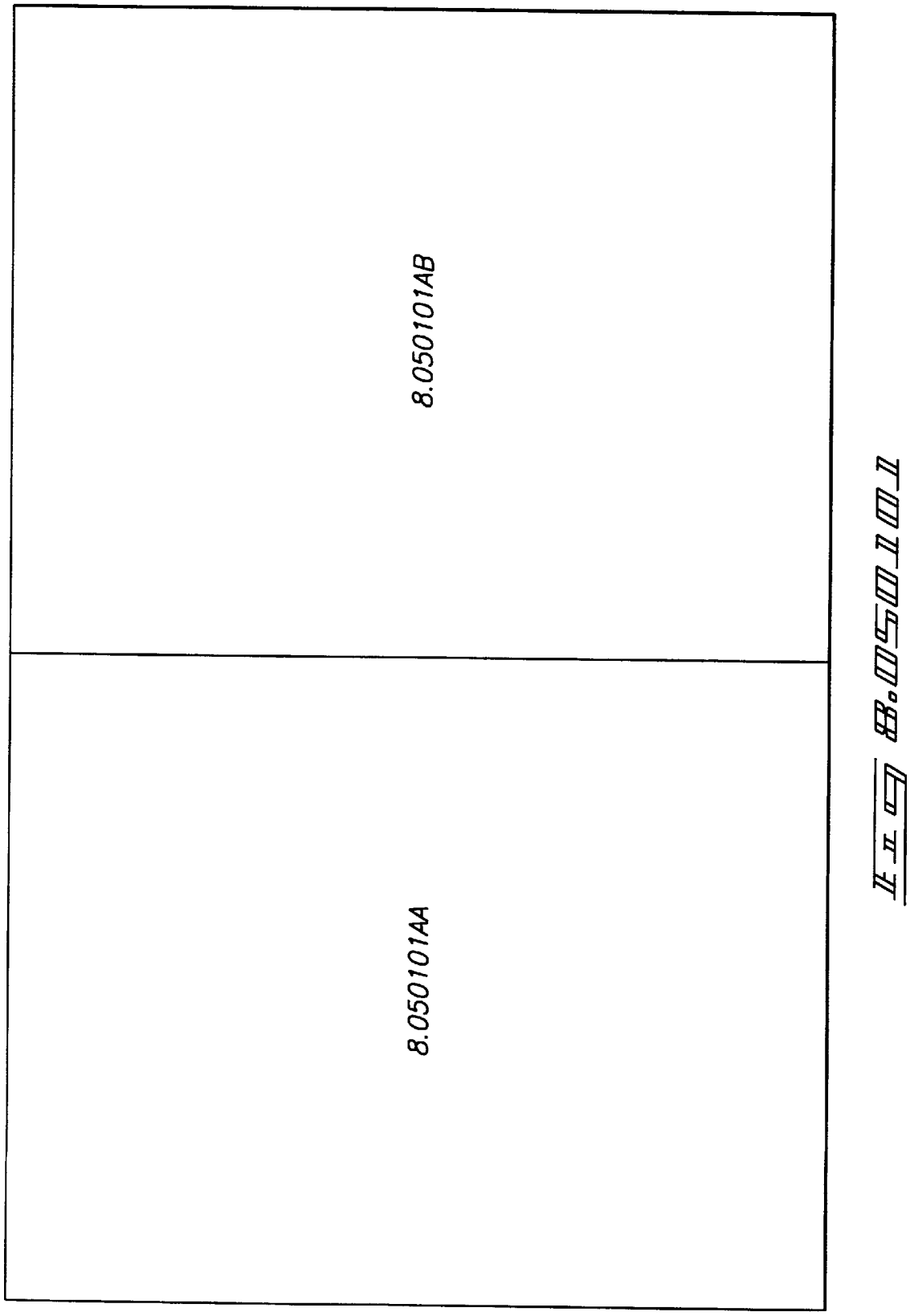


FIG. 88.0501 BE


8.050101AB
8.050101A
FIG 8.050101

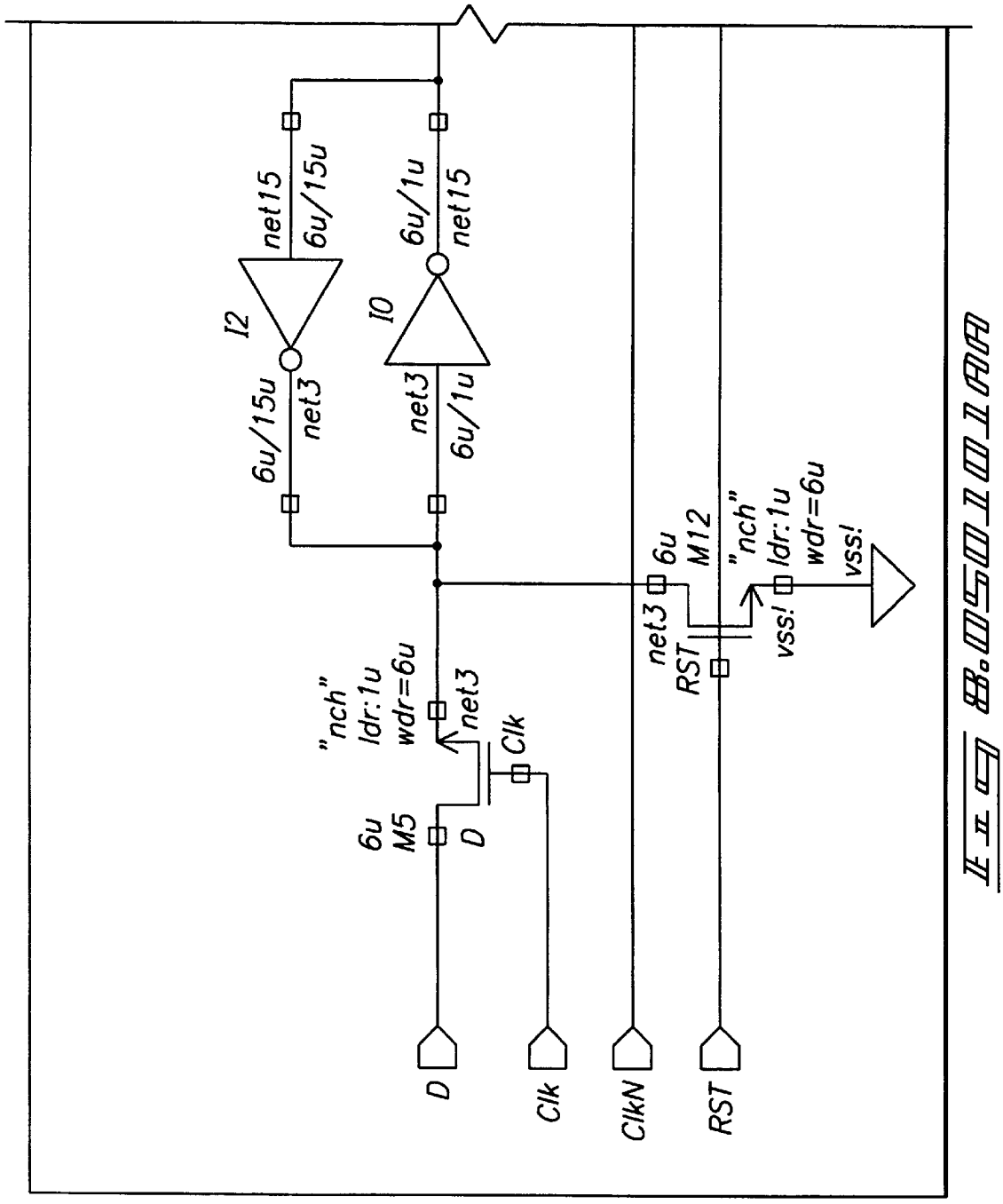


Fig 88.0500111AA

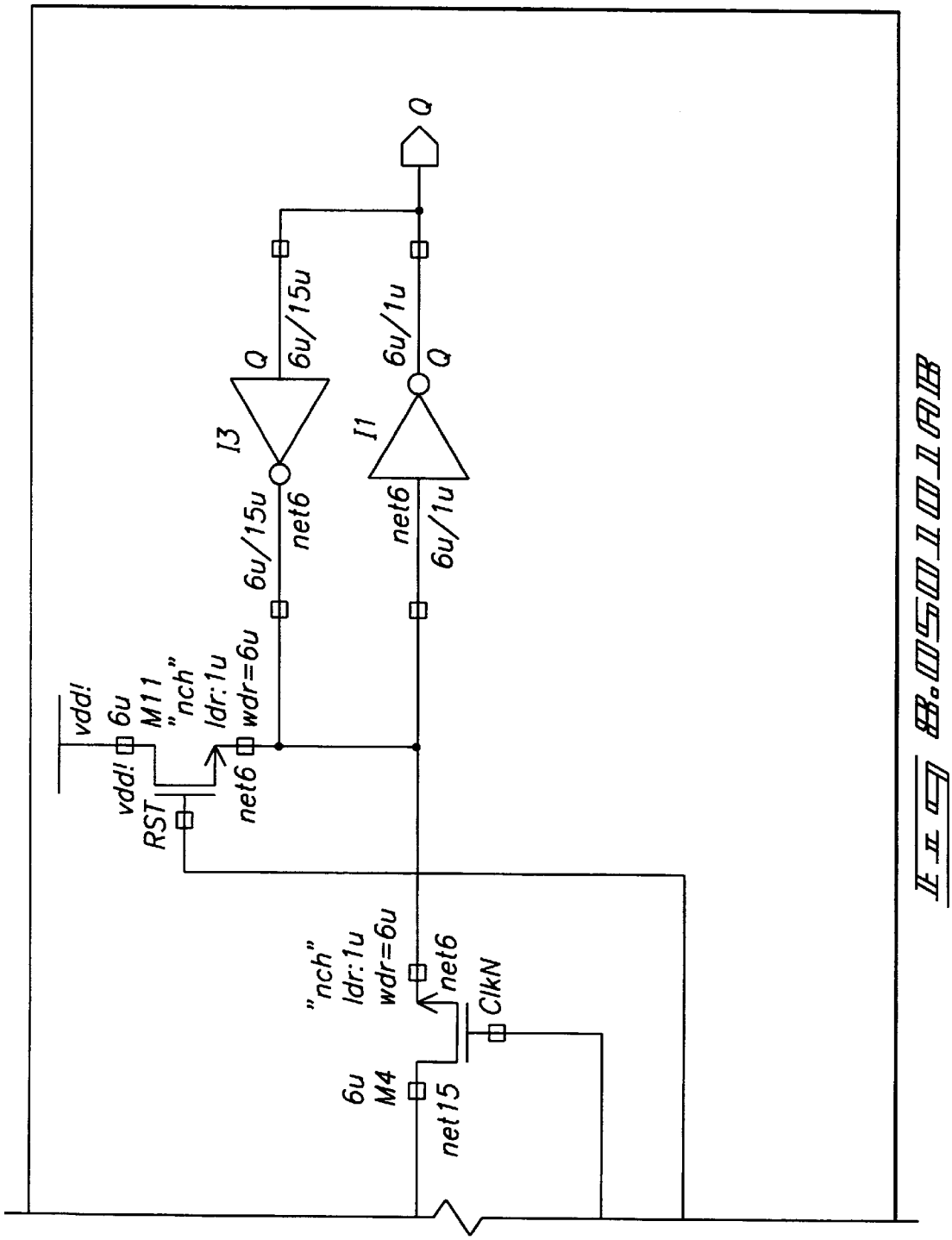
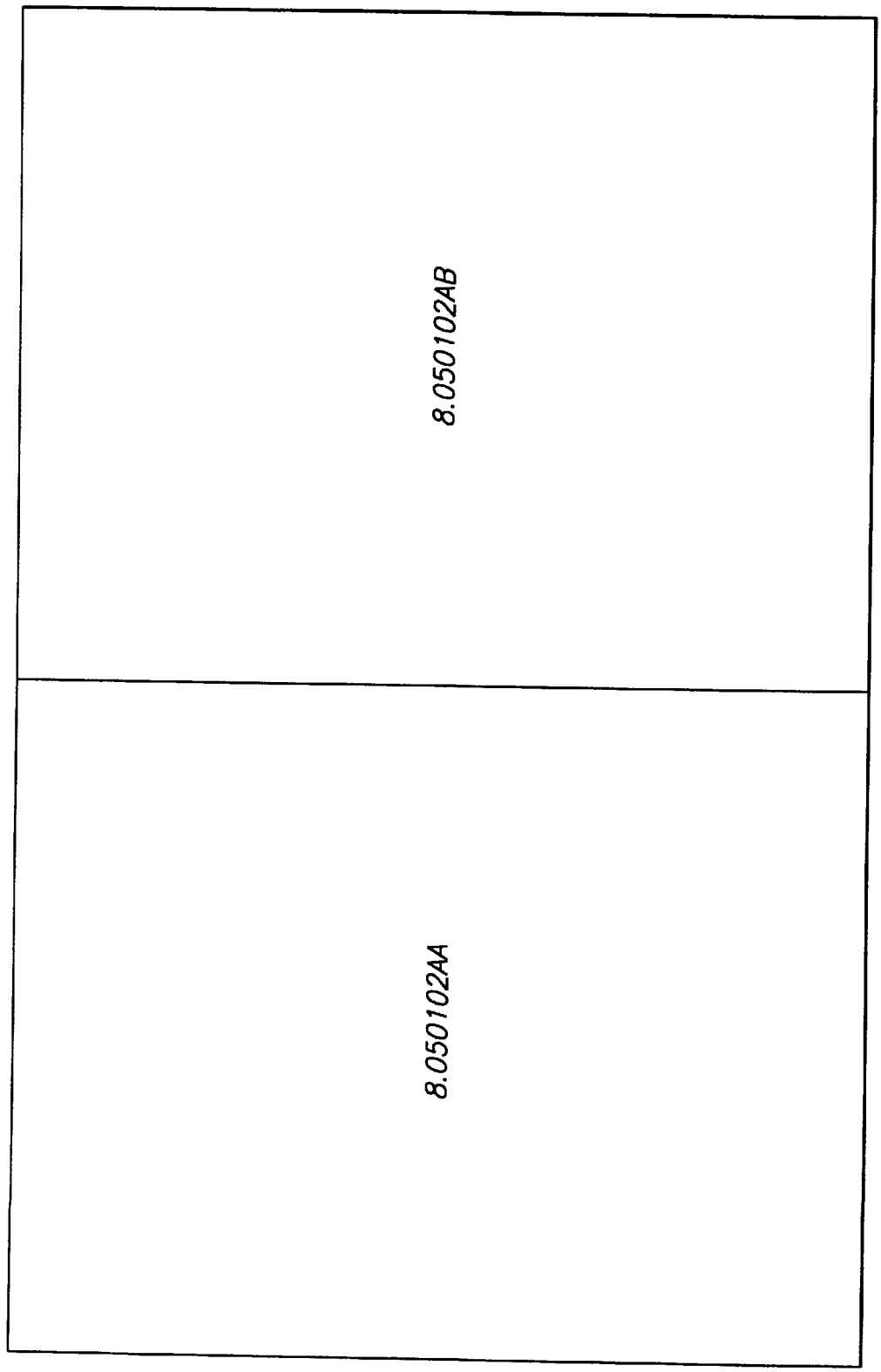

Q
6u/15u
Q
6u/1u
Q
I3
I1
6u/15u
net6
net6
6u/1u
vdd!
6u
M11
"nch"
ldr:1u
wdr=6u
vdd!
RST
net6
"nch"
ldr:1u
wdr=6u
net6
ClkN
6u
M4
net15

FIG 8.0501AB


8.050102AB
8.050102AA
FIG. 8.050102

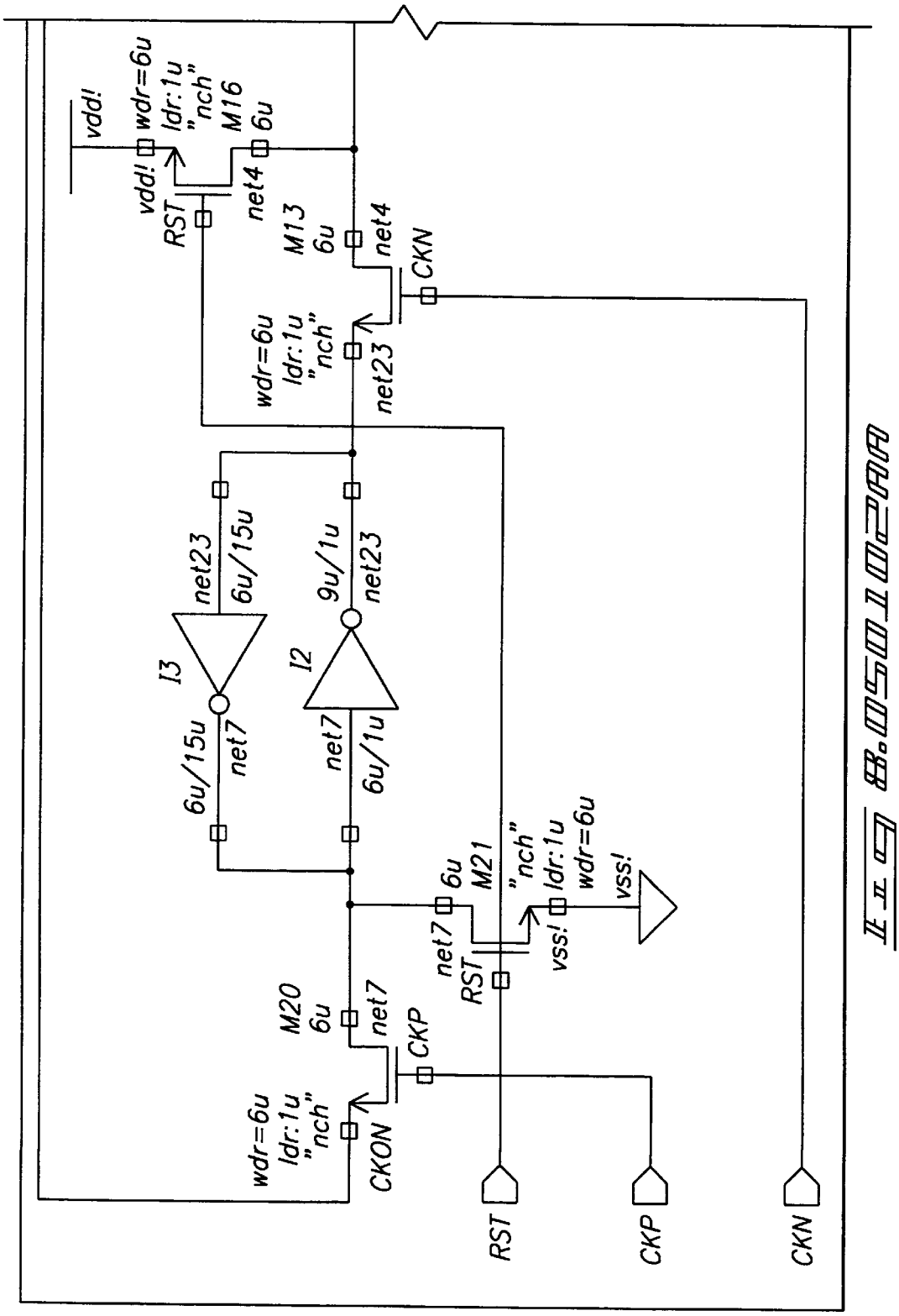

vdd!
wdr=6u
ldr:1u
"nch"
M16
6u
net4
RST
M13
6u
net4
CKN
wdr=6u
ldr:1u
"nch"
net23
net23
6u/15u
9u/1u
net23
I3
I2
6u/15u
net7
net7
6u/1u
6u
M21
"nch"
ldr:1u
wdr=6u
vss!
net7
RST
vss!
M20
6u
net7
CKP
wdr=6u
ldr:1u
"nch"
CKON
RST
CKP
CKN

FIG 8,850,108

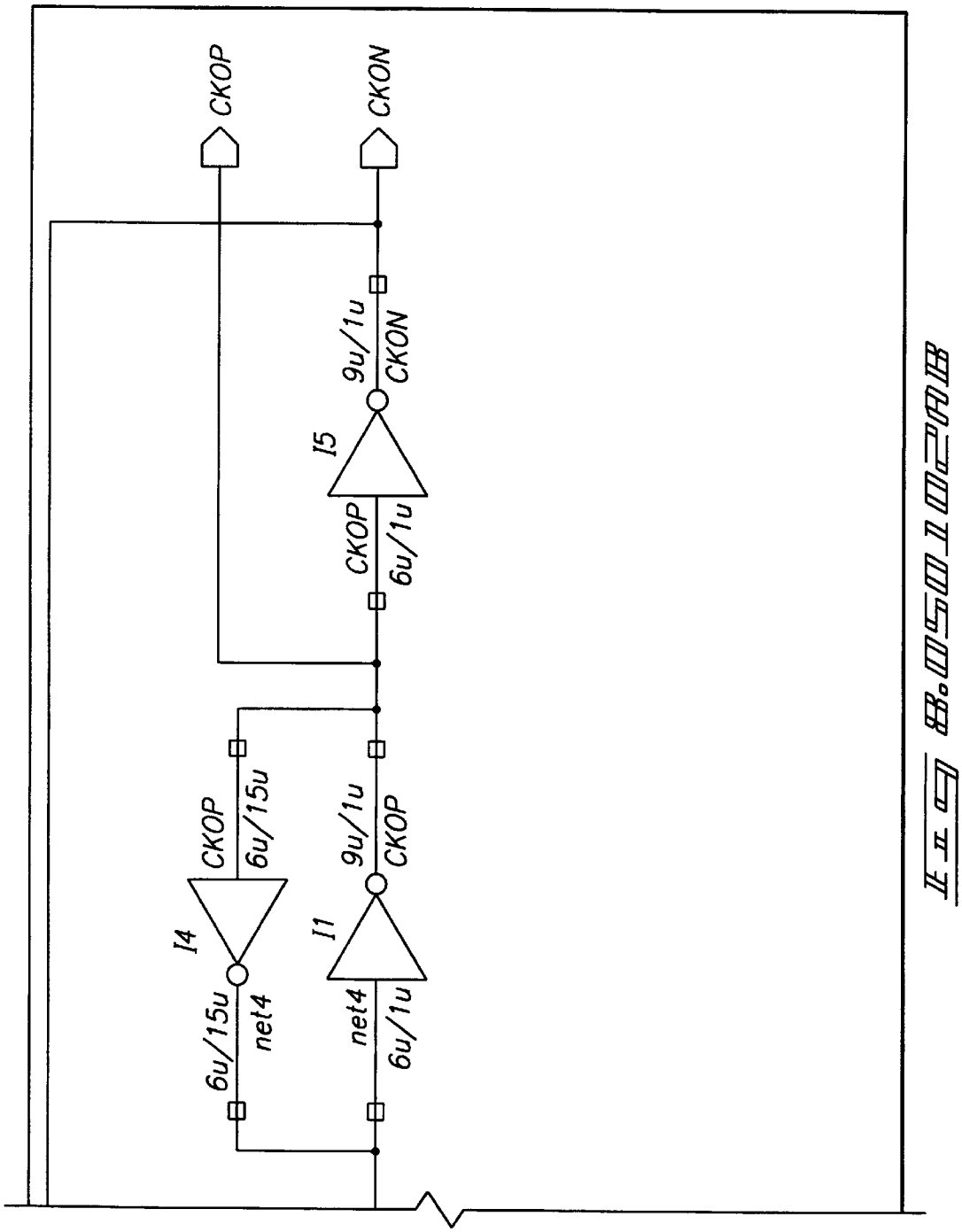

CKOP
CKON
9u/1u
CKON
I5
CKOP
6u/1u
CKOP
6u/15u
9u/1u
CKOP
I4
I1
6u/15u
net4
net4
6u/1u

FIG 88

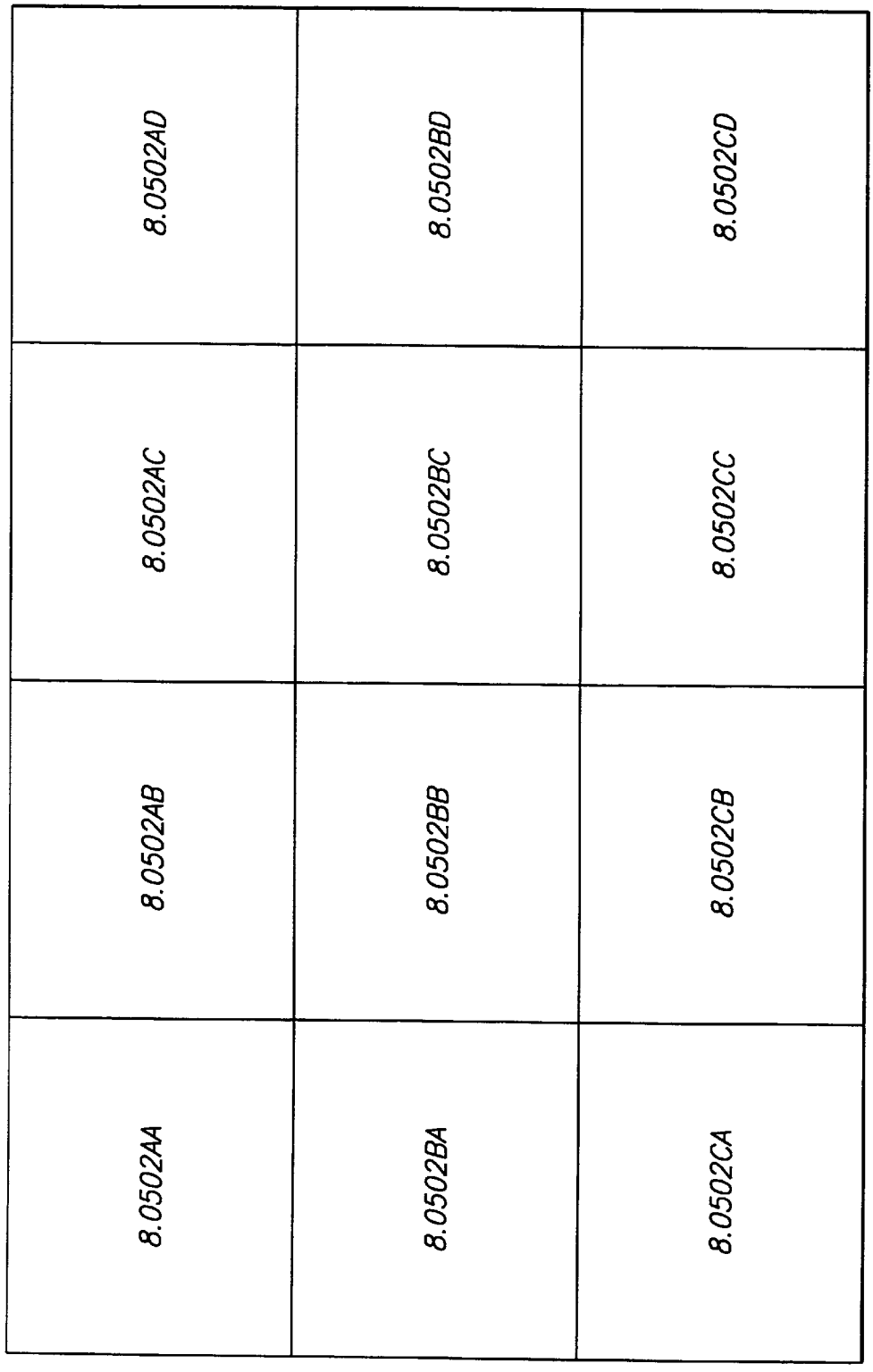

8.0502AD
8.0502BD
8.0502CD
8.0502AC
8.0502BC
8.0502CC
8.0502AB
8.0502BB
8.0502CB
8.0502AA
8.0502BA
8.0502CA

Fig 8.0502

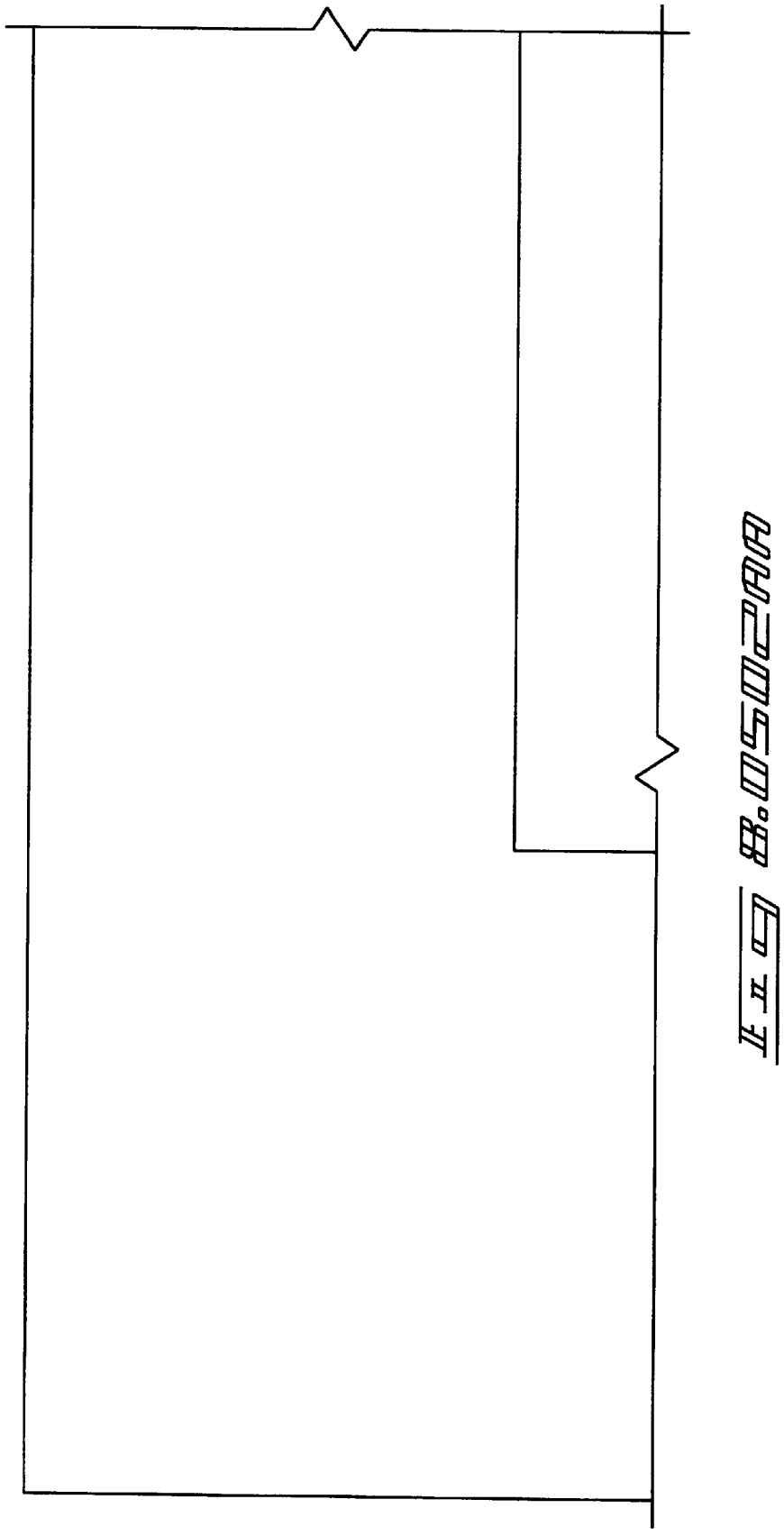


FIG 98.05027AA

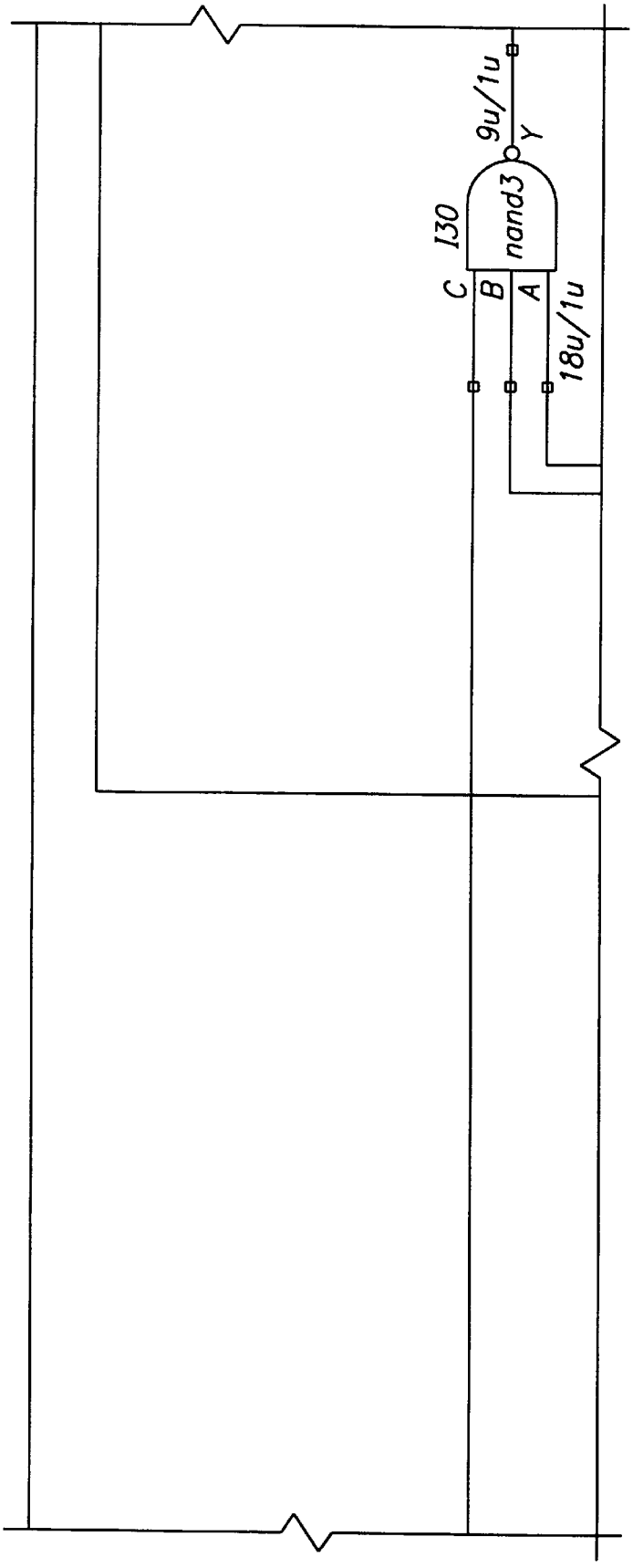


FIG 88.0502AB

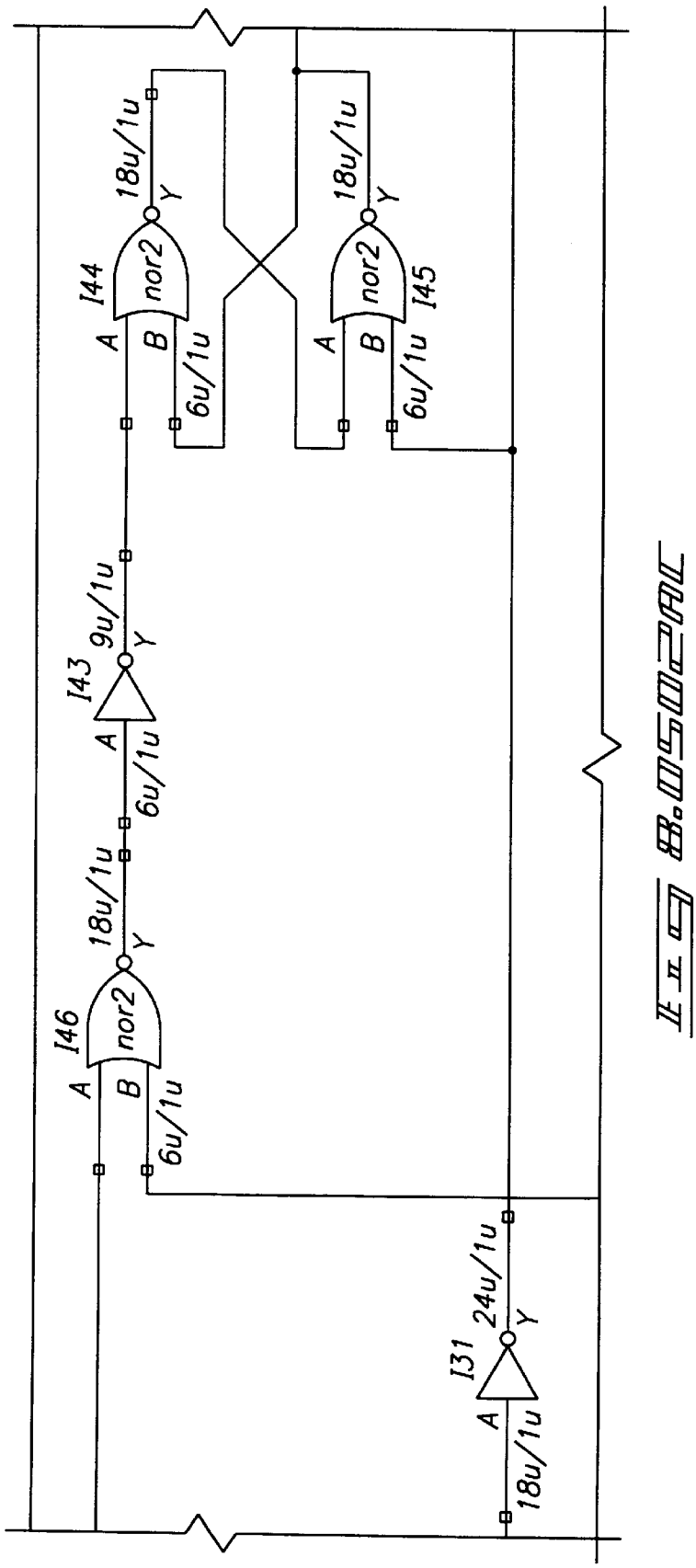


FIG 88.0SDZAC

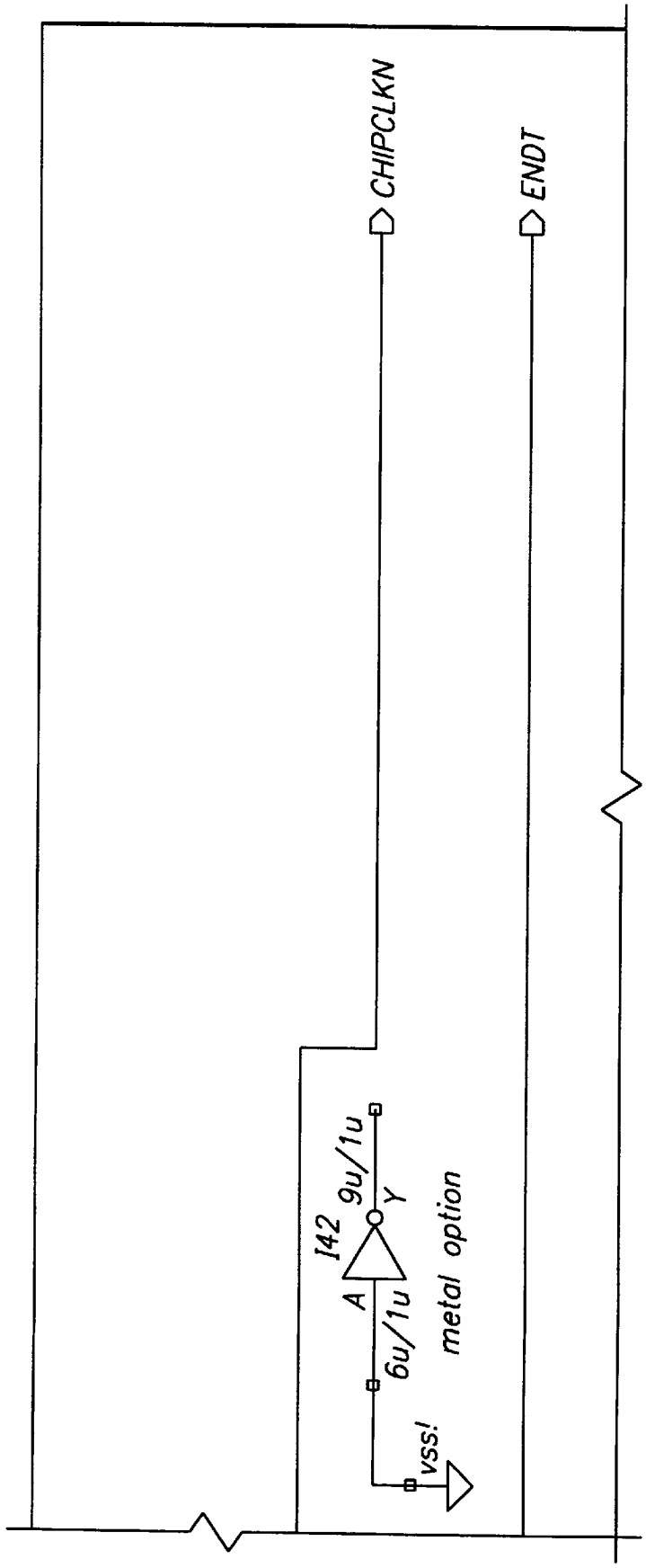


FIG 8.0520AD

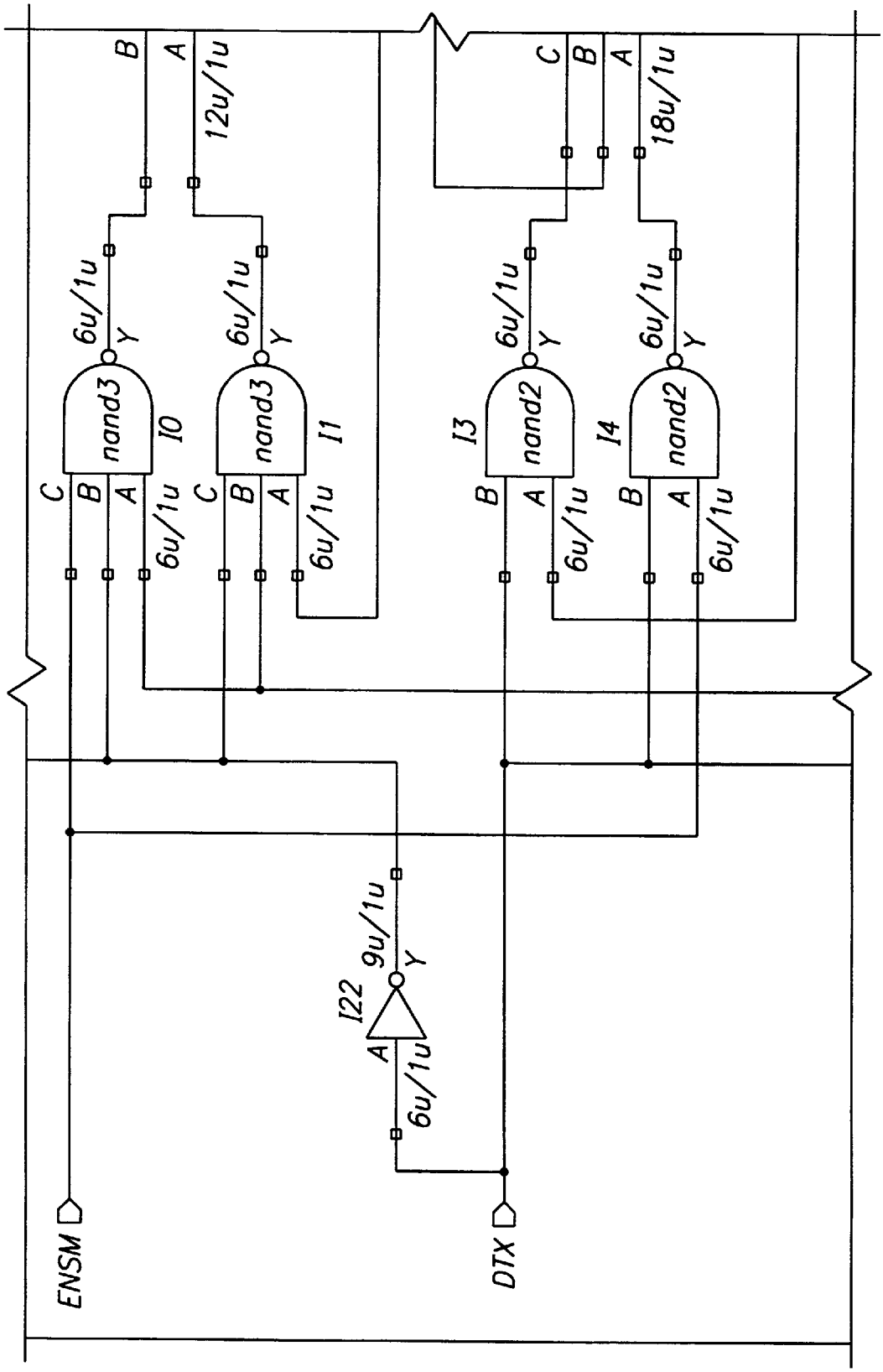


FIG 88.005208A

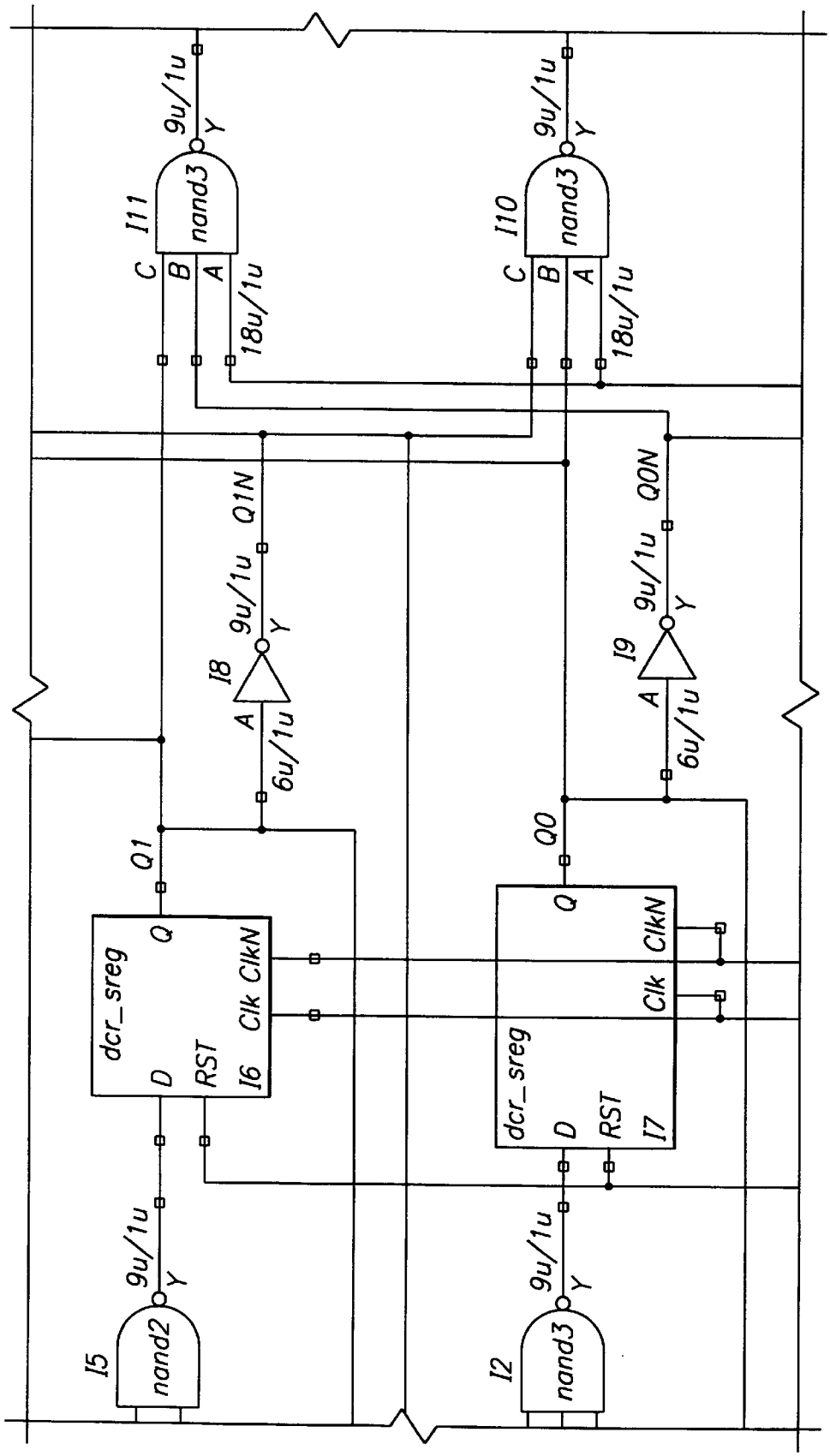


FIG 88,050,288

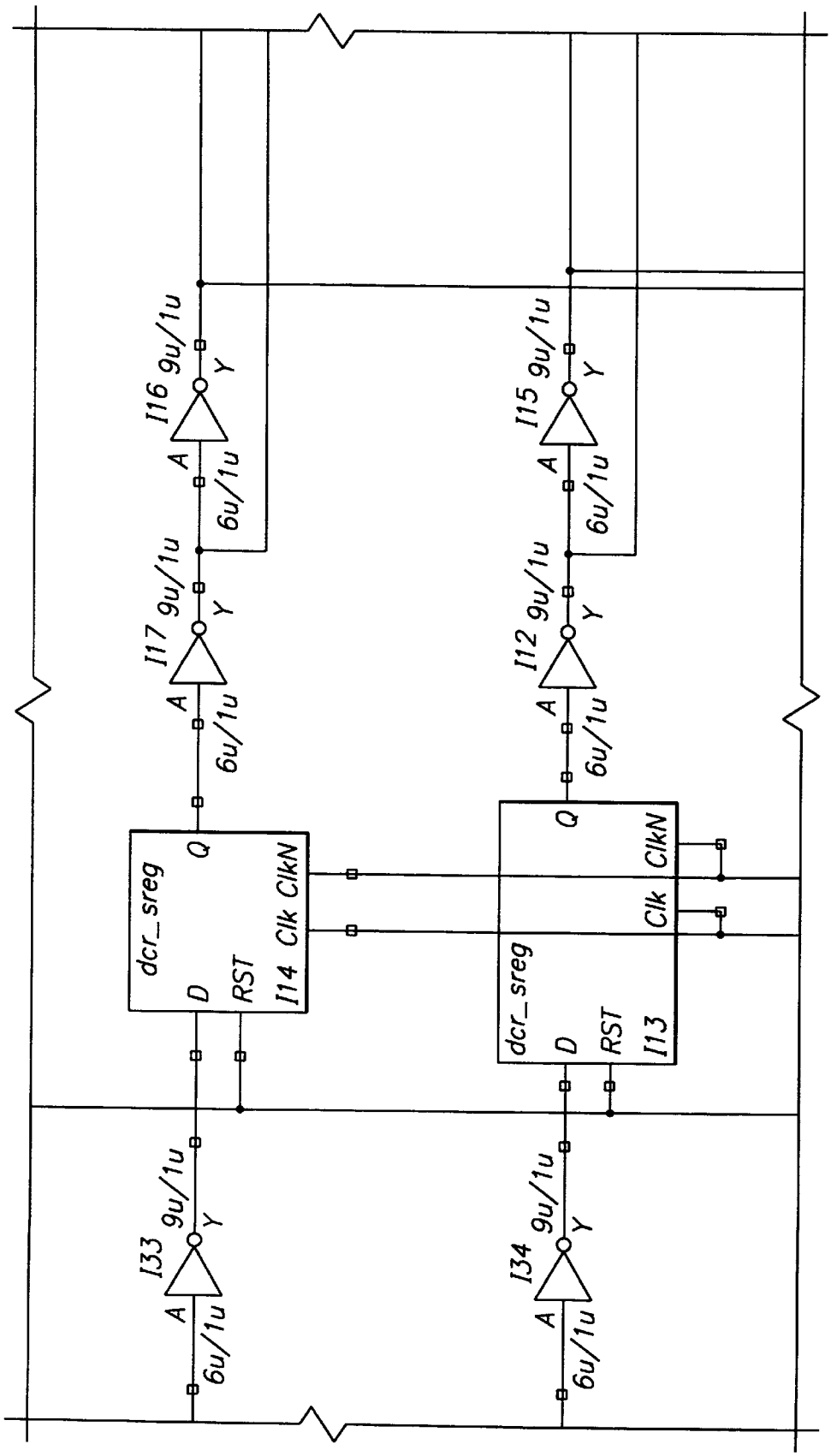


FIG 68.0502BL

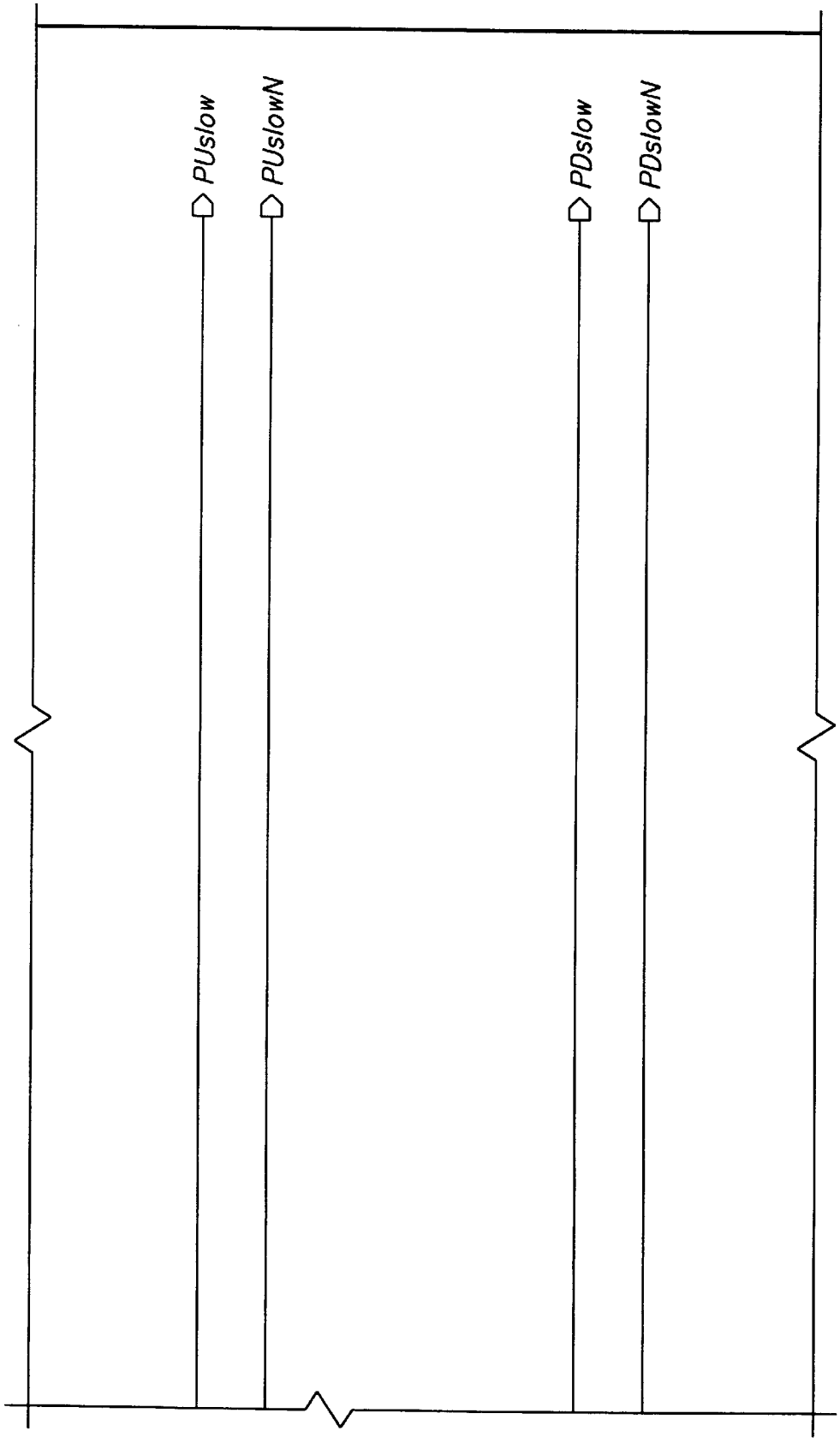


FIG 88,005,2810

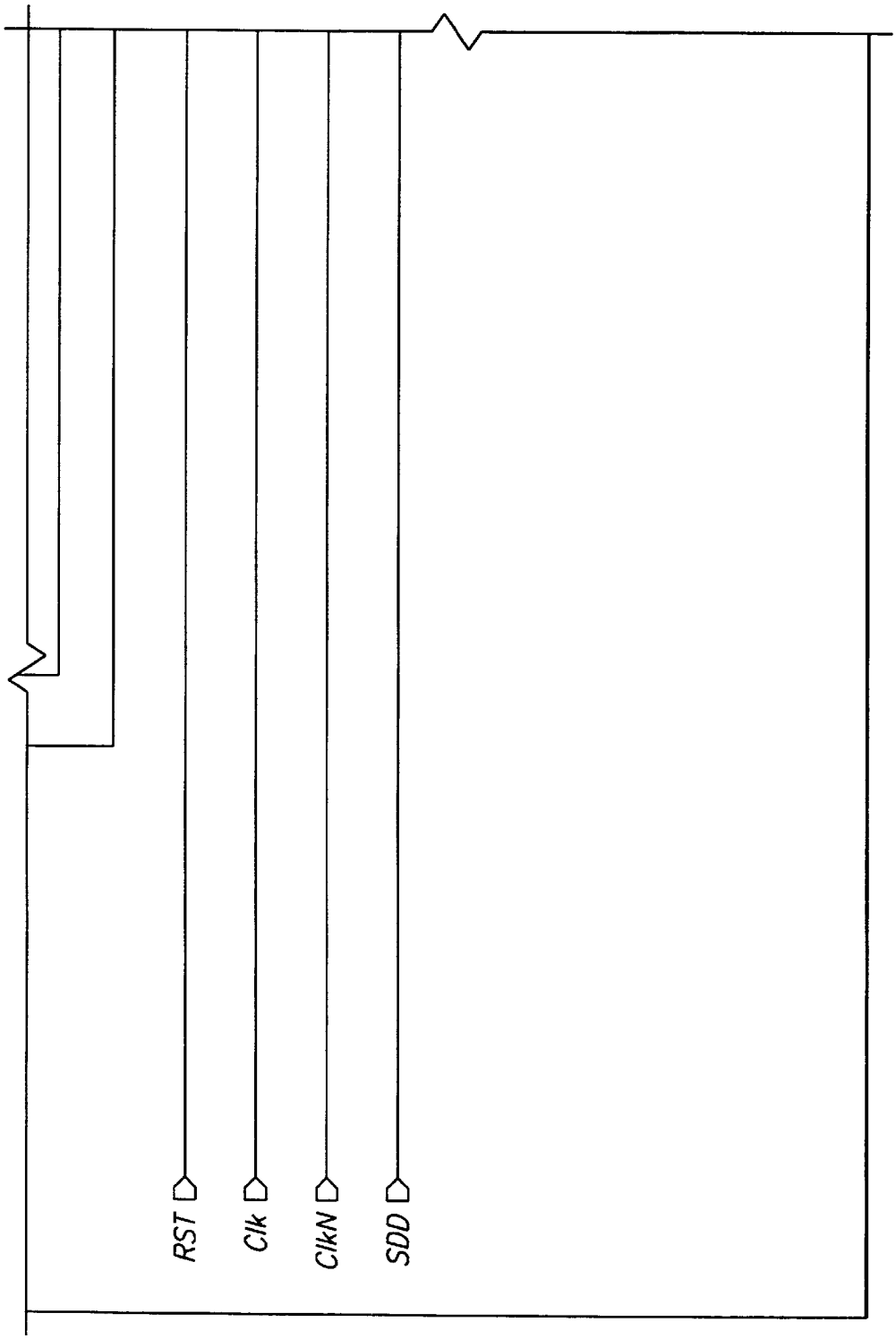


FIG 8,050,A

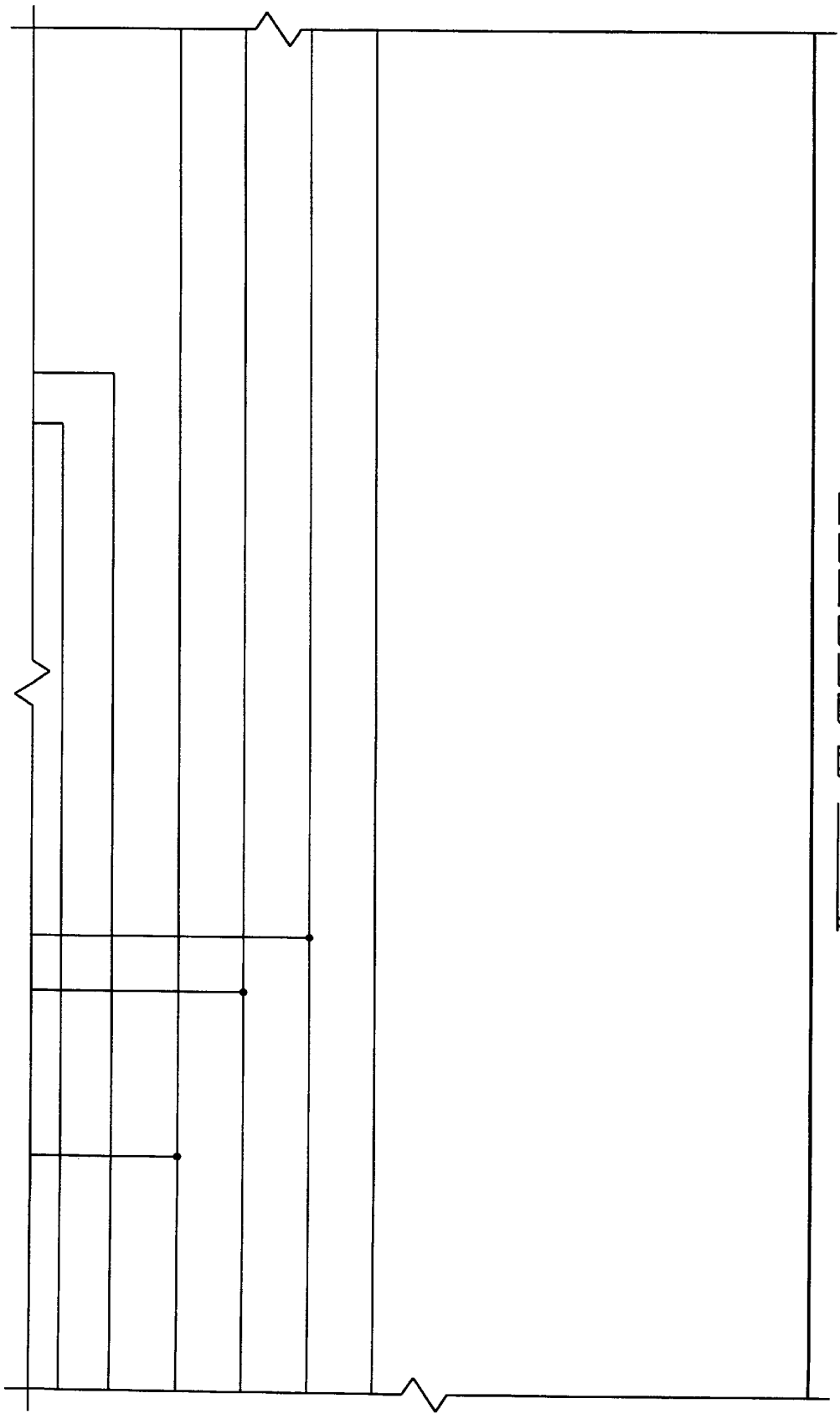


FIG 88.05027B

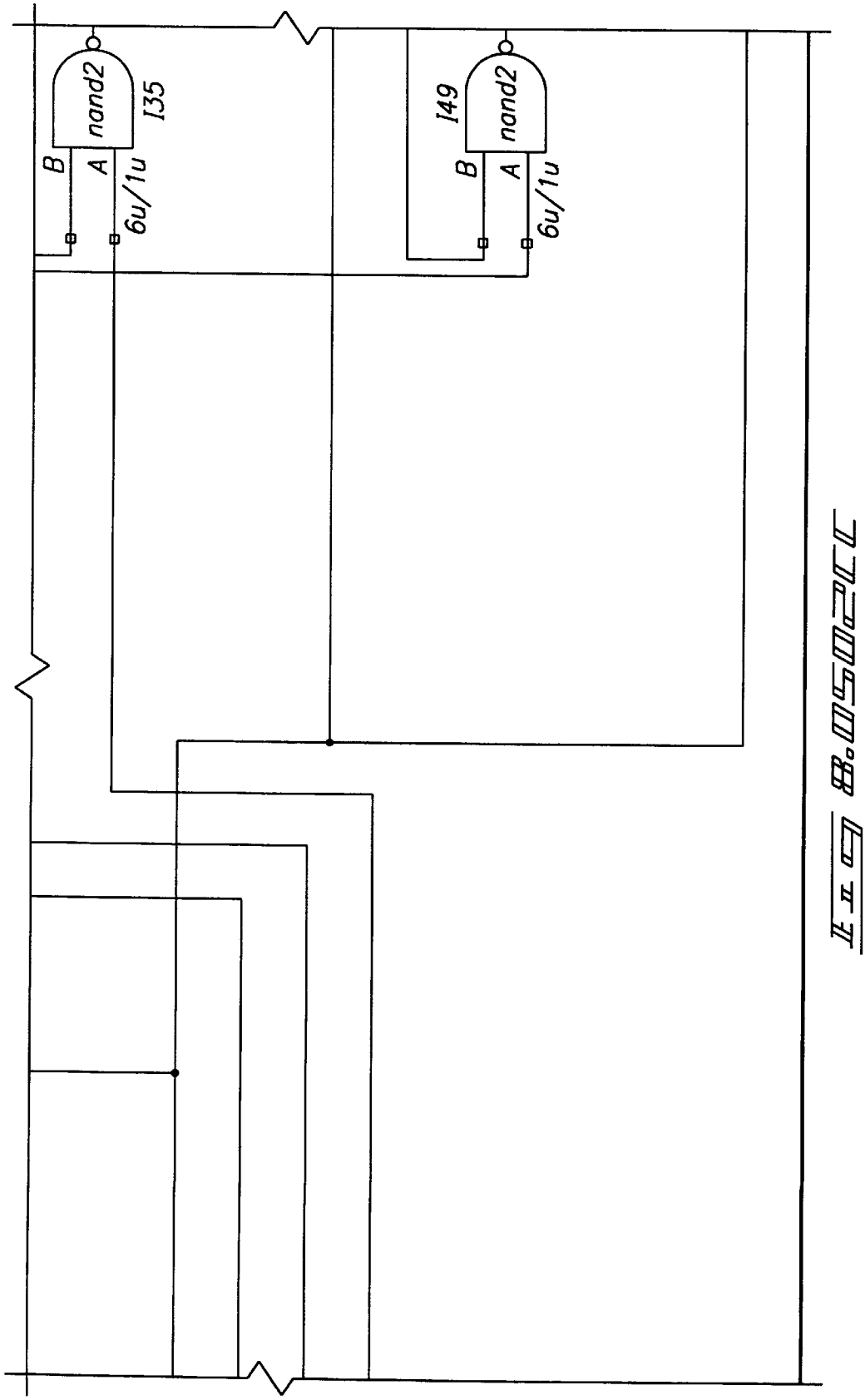


FIG 8,050,778

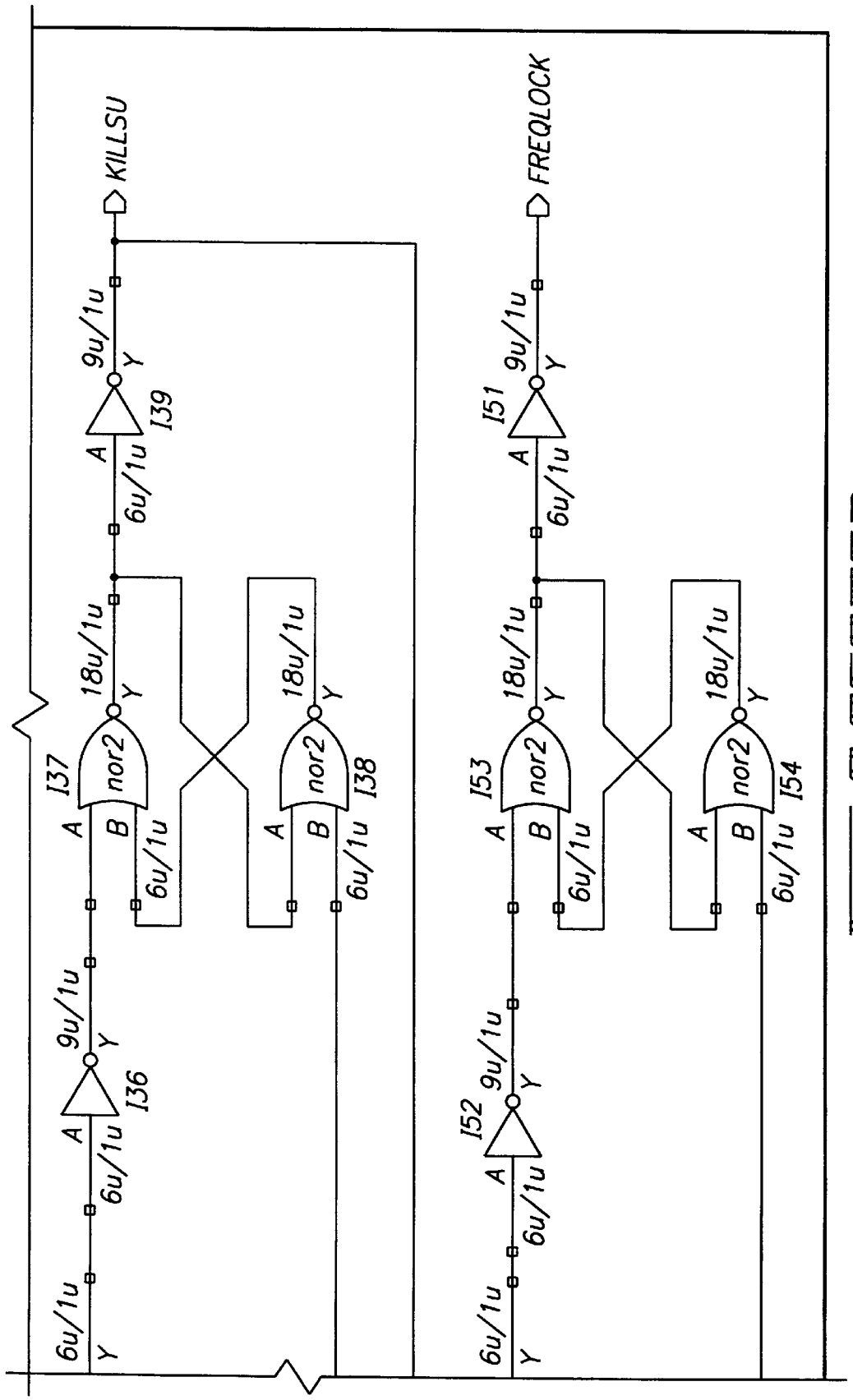

KILLSU
FREQLOCK
9u/1u
6u/1u
18u/1u
nor2
I36
I37
I38
I39
I51
I52
I53
I54
A
B
Y

FIG. 88.00500

8.0503AA	8.0503AB	8.0503AC	8.0503AD	8.0503AE	8.0503AF	8.0503AG	8.0503AH	8.0503AI	8.0503AJ	8.0503AK	8.0503AL	8.0503AM	8.0503AN	8.0503AO	
8.0503BA	8.0503BB	8.0503BC	8.0503BD	8.0503BE	8.0503BF	8.0503BG	8.0503BH	8.0503BI	8.0503BJ	8.0503BK	8.0503BL	8.0503BM	8.0503BN	8.0503BO	
8.0503CA	8.0503CB	8.0503CC	8.0503CD	8.0503CE	8.0503CF	8.0503CG	8.0503CH	8.0503CI	8.0503CJ	8.0503CK	8.0503CL	8.0503CM	8.0503CN	8.0503CO	
8.0503DA	8.0503DB	8.0503DC	8.0503DD	8.0503DE	8.0503DF	8.0503DG	8.0503DH	8.0503DI	8.0503DJ	8.0503DK	8.0503DL	8.0503DM	8.0503DN	8.0503DO	
8.0503EA	8.0503EB	8.0503EC	8.0503ED	8.0503EE	8.0503EF	8.0503EG	8.0503EH	8.0503EI	8.0503EJ	8.0503EK	8.0503EL	8.0503EM	8.0503EN		
8.0503FA	8.0503FB	8.0503FC	8.0503FD	8.0503FE	8.0503FF	8.0503FG	8.0503FH	8.0503FI	8.0503FJ	8.0503FK	8.0503FL	8.0503FM	8.0503FN		

FIG. 8.0503

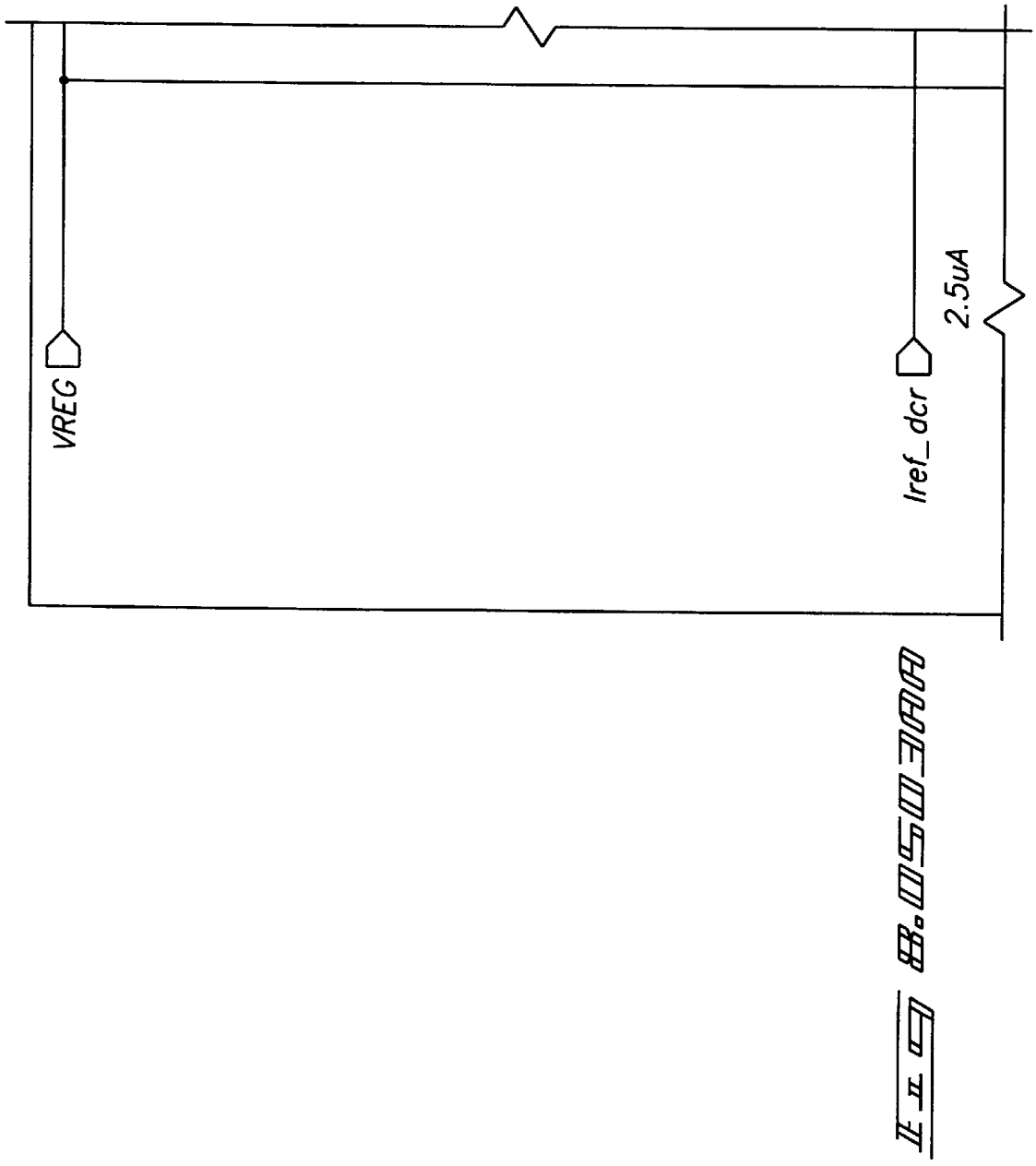


FIG 88.0500AA

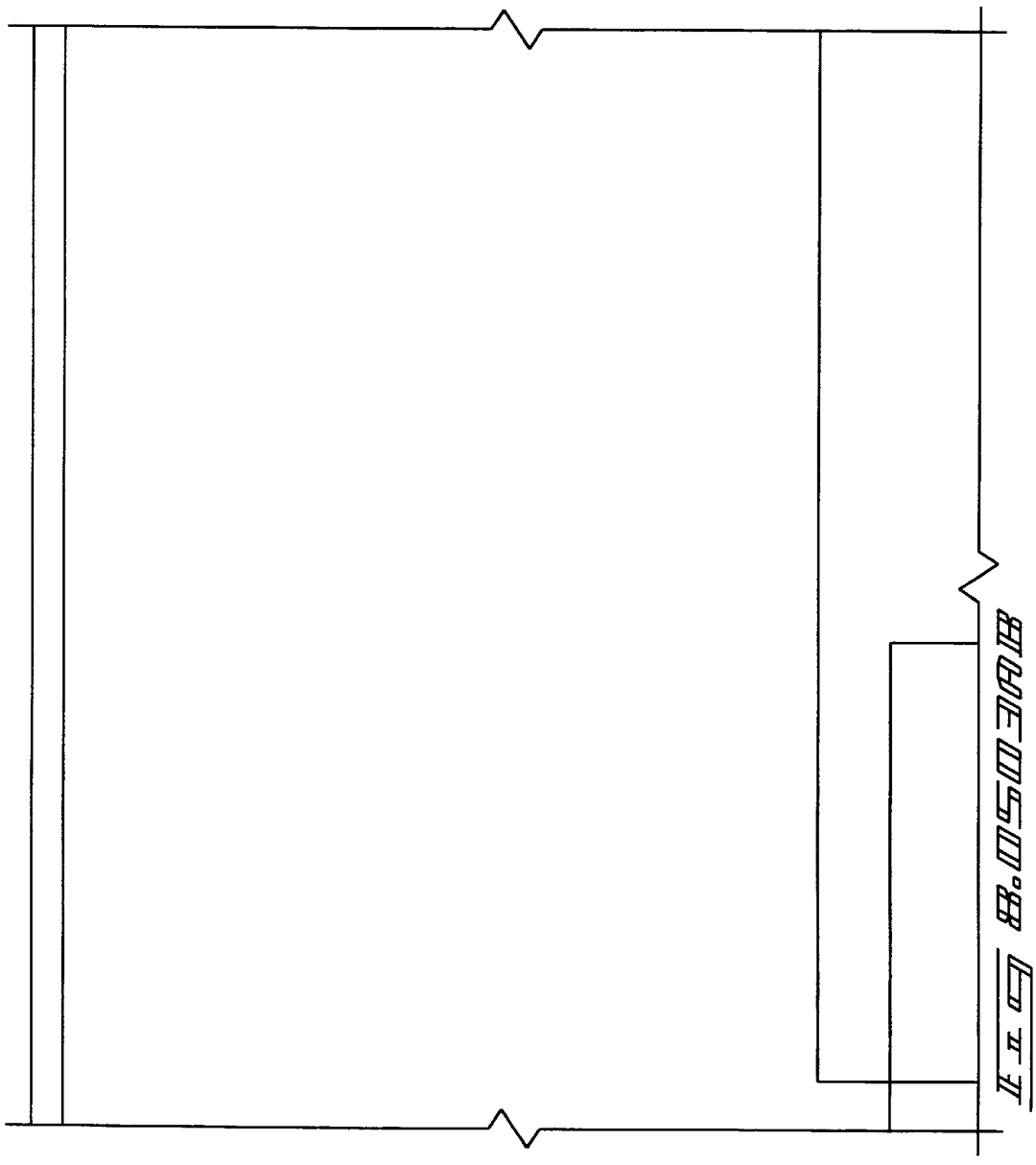


FIG 1498

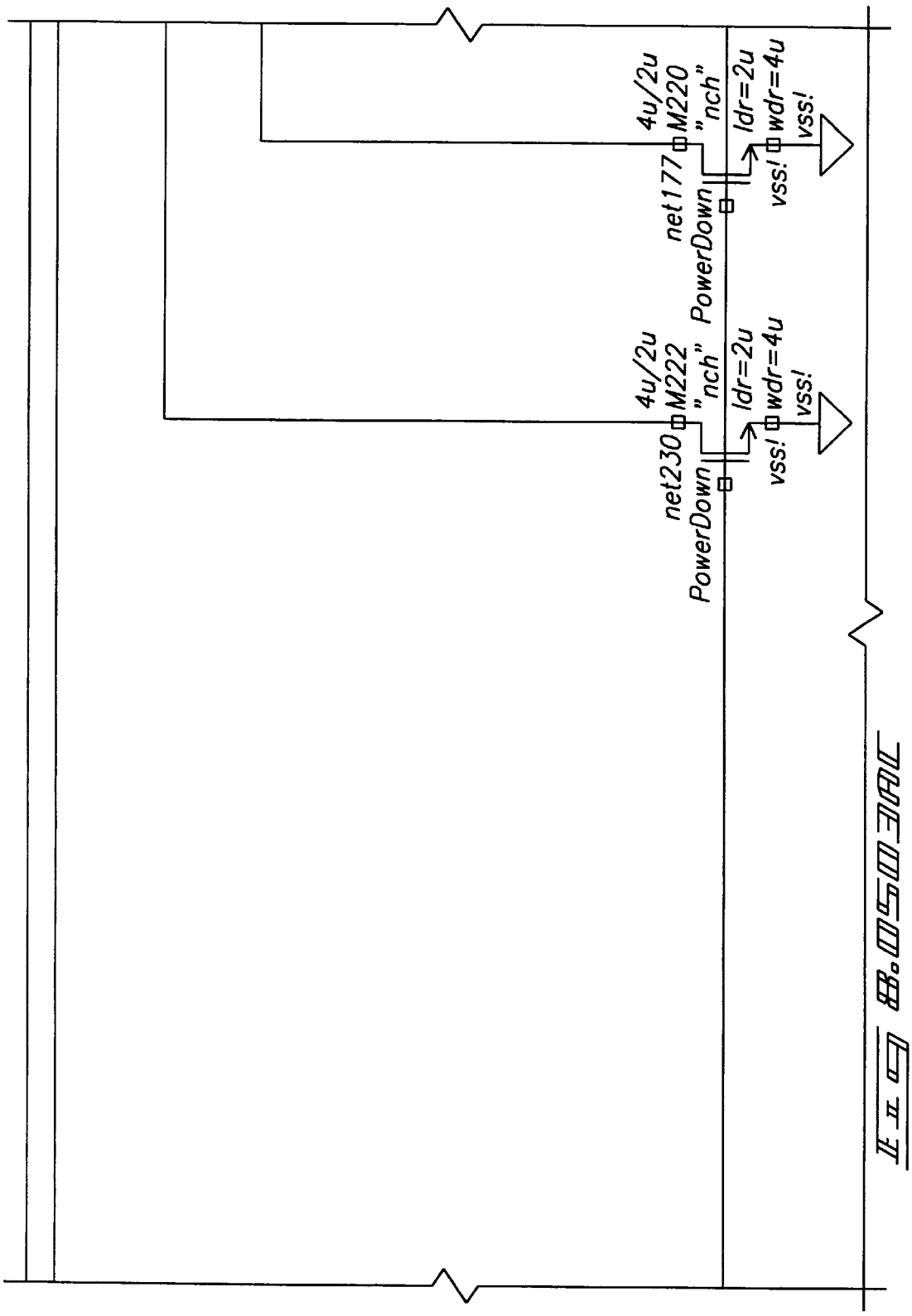
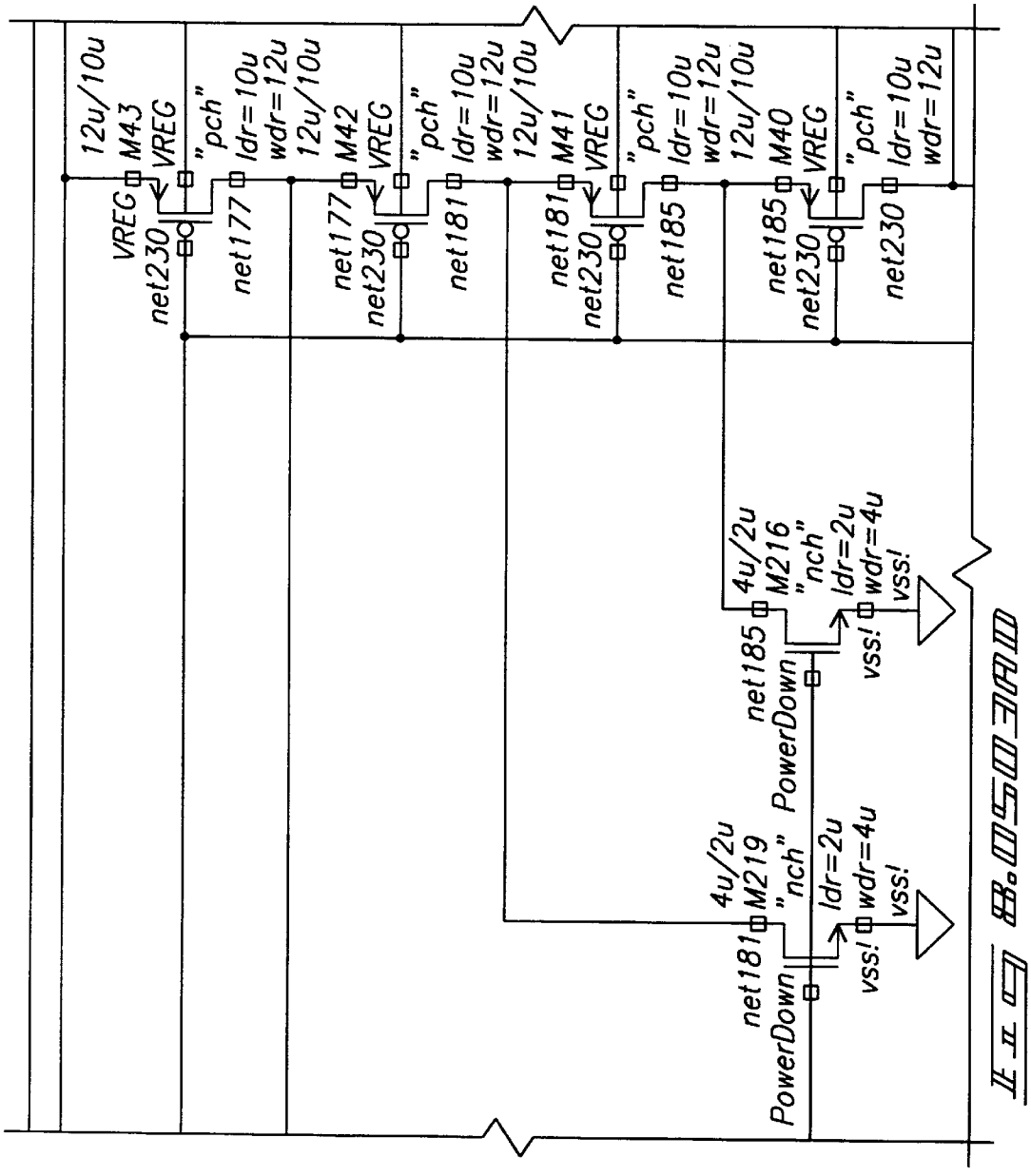

4u/2u
M220
"nch"
ldr=2u
wdr=4u
vss!
net177
PowerDown
vss!
4u/2u
M222
"nch"
ldr=2u
wdr=4u
vss!
net230
PowerDown
vss!

FIG 1499


12u/10u
M43
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
VREG
net230
net177
M42
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
net177
net230
net181
M41
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
net181
net230
net185
M40
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
net185
net230
net230
"pch"
ldr=10u
wdr=12u
4u/2u
M216
"nch"
ldr=2u
wdr=4u
vss!
net185
PowerDown
vss!
4u/2u
M219
"nch"
ldr=2u
wdr=4u
vss!
net181
PowerDown
vss!
VDD 8.000 ft

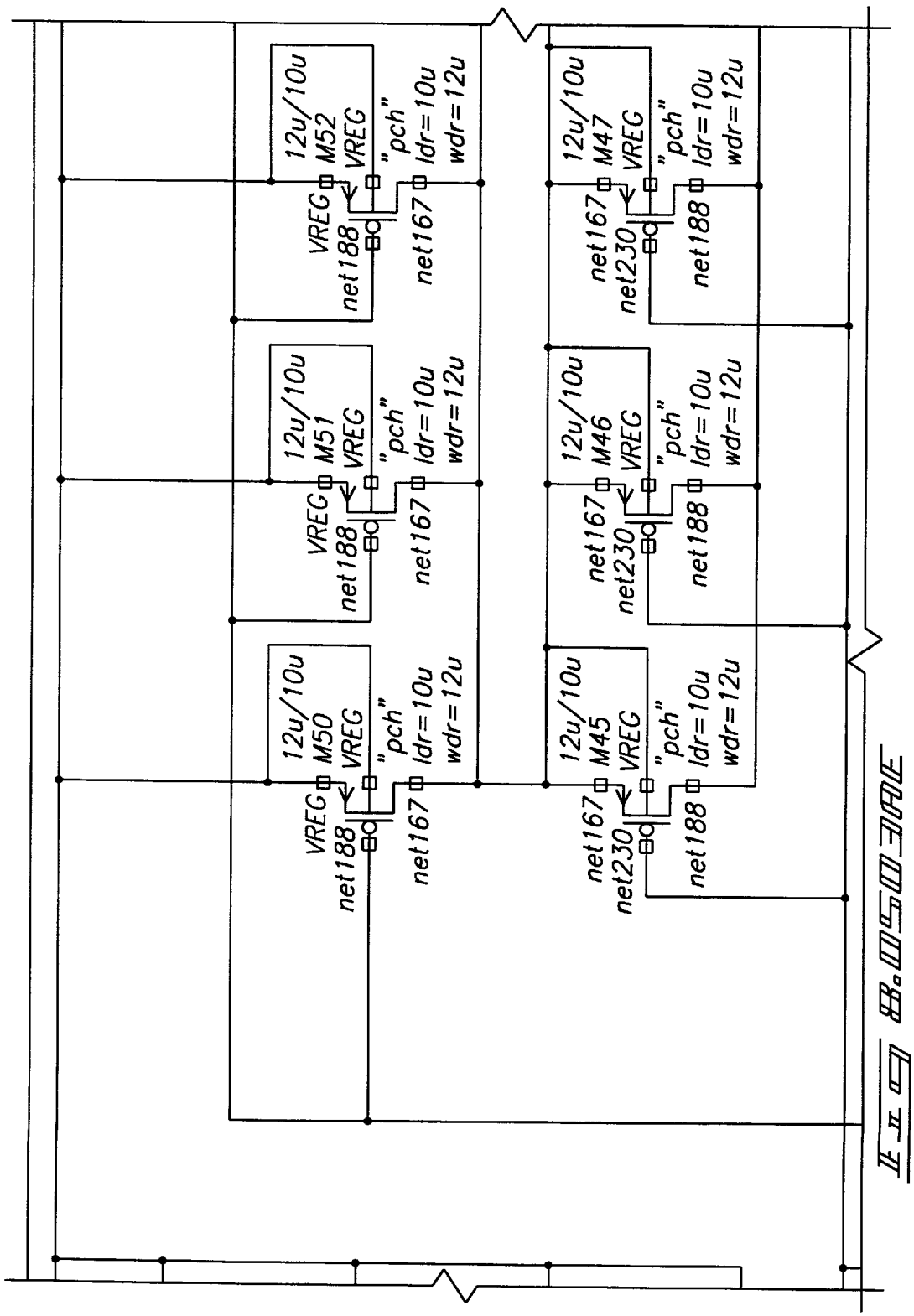

12u/10u
M52
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net167
12u/10u
M51
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net167
12u/10u
M50
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net167
12u/10u
M47
VREG
"pch"
ldr=10u
wdr=12u
net167
net230
net188
12u/10u
M46
VREG
"pch"
ldr=10u
wdr=12u
net167
net230
net188
12u/10u
M45
VREG
"pch"
ldr=10u
wdr=12u
net167
net230
net188

FIG. 88.005

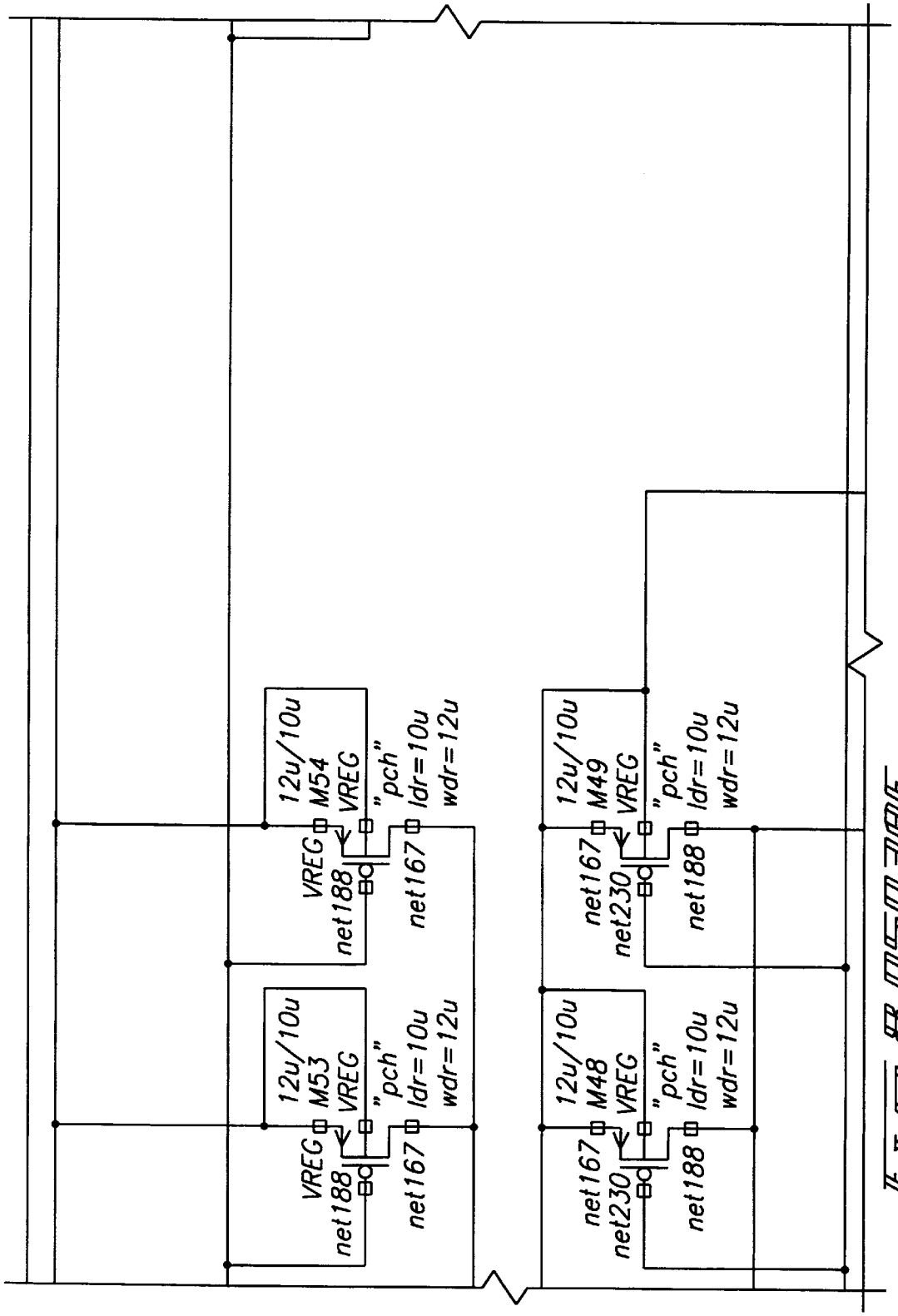


FIG. 888.0SSOM

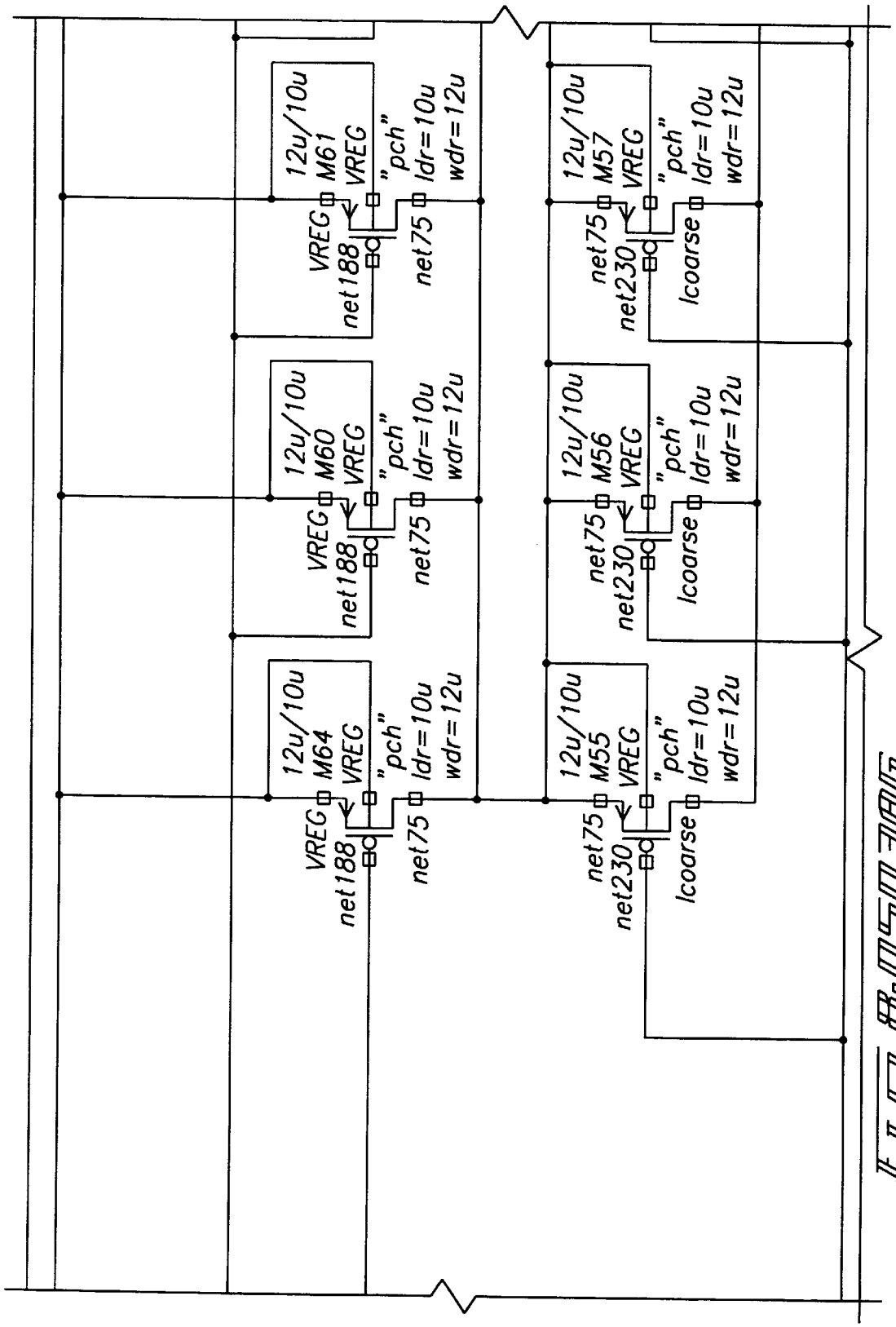

12u/10u
M61
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net75
12u/10u
M60
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net75
12u/10u
M64
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net75
12u/10u
M57
VREG
"pch"
ldr=10u
wdr=12u
net75
net230
lcoarse
12u/10u
M56
VREG
"pch"
ldr=10u
wdr=12u
net75
net230
lcoarse
12u/10u
M55
VREG
"pch"
ldr=10u
wdr=12u
net75
net230
lcoarse

FIG 1503

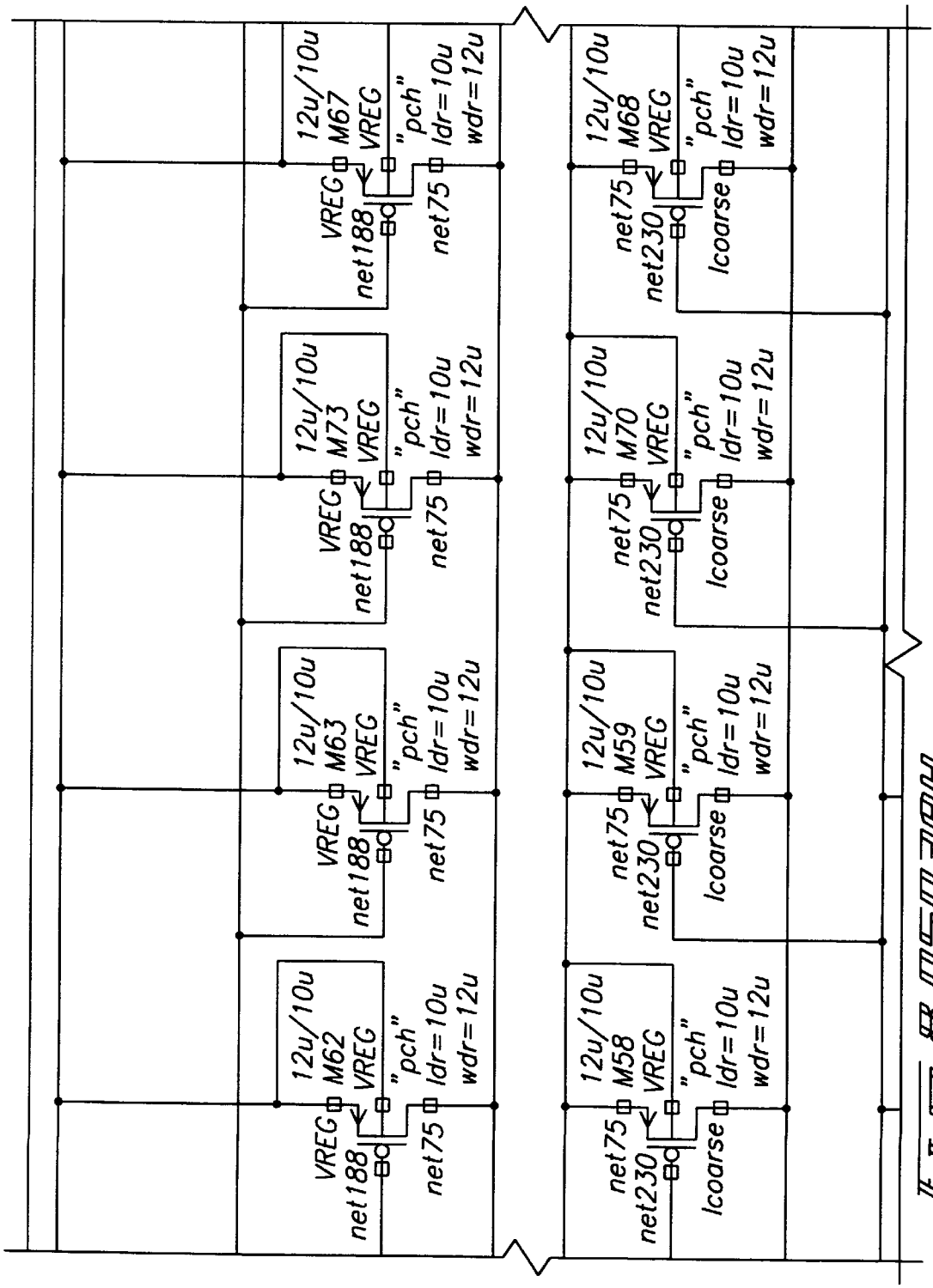

12u/10u
M67
VREG
"pch"
ldr=10u
wdr=12u
net188
net75
12u/10u
M68
net230
lcoarse
12u/10u
M73
12u/10u
M70
12u/10u
M63
12u/10u
M59
12u/10u
M62
12u/10u
M58

FIG 8.0508

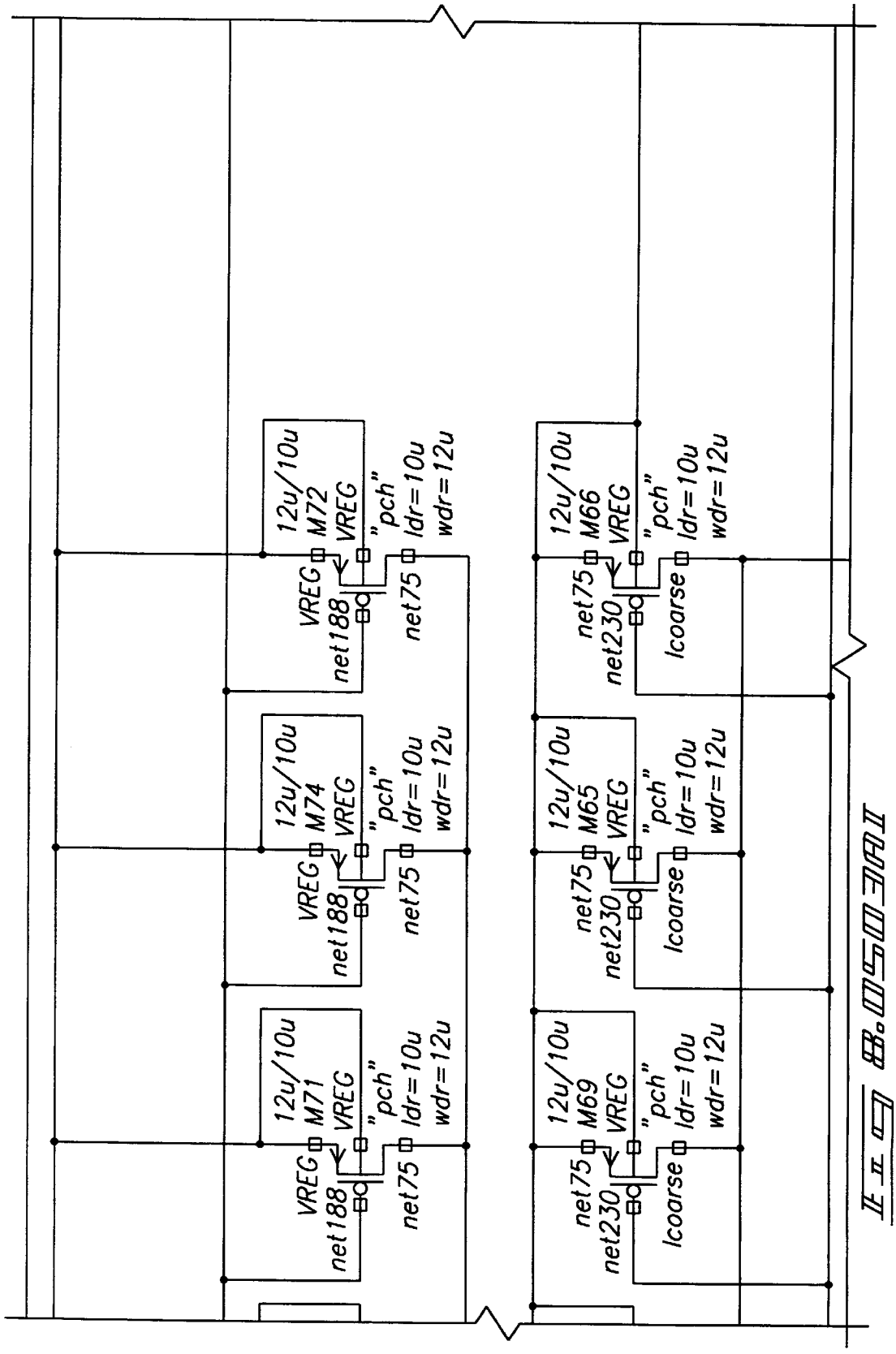

12u/10u
M72
VREG
"pch"
ldr=10u
wdr=12u
net188
net75
12u/10u
M74
12u/10u
M71
12u/10u
M66
net230
lcoarse
12u/10u
M65
12u/10u
M69

FIG 88

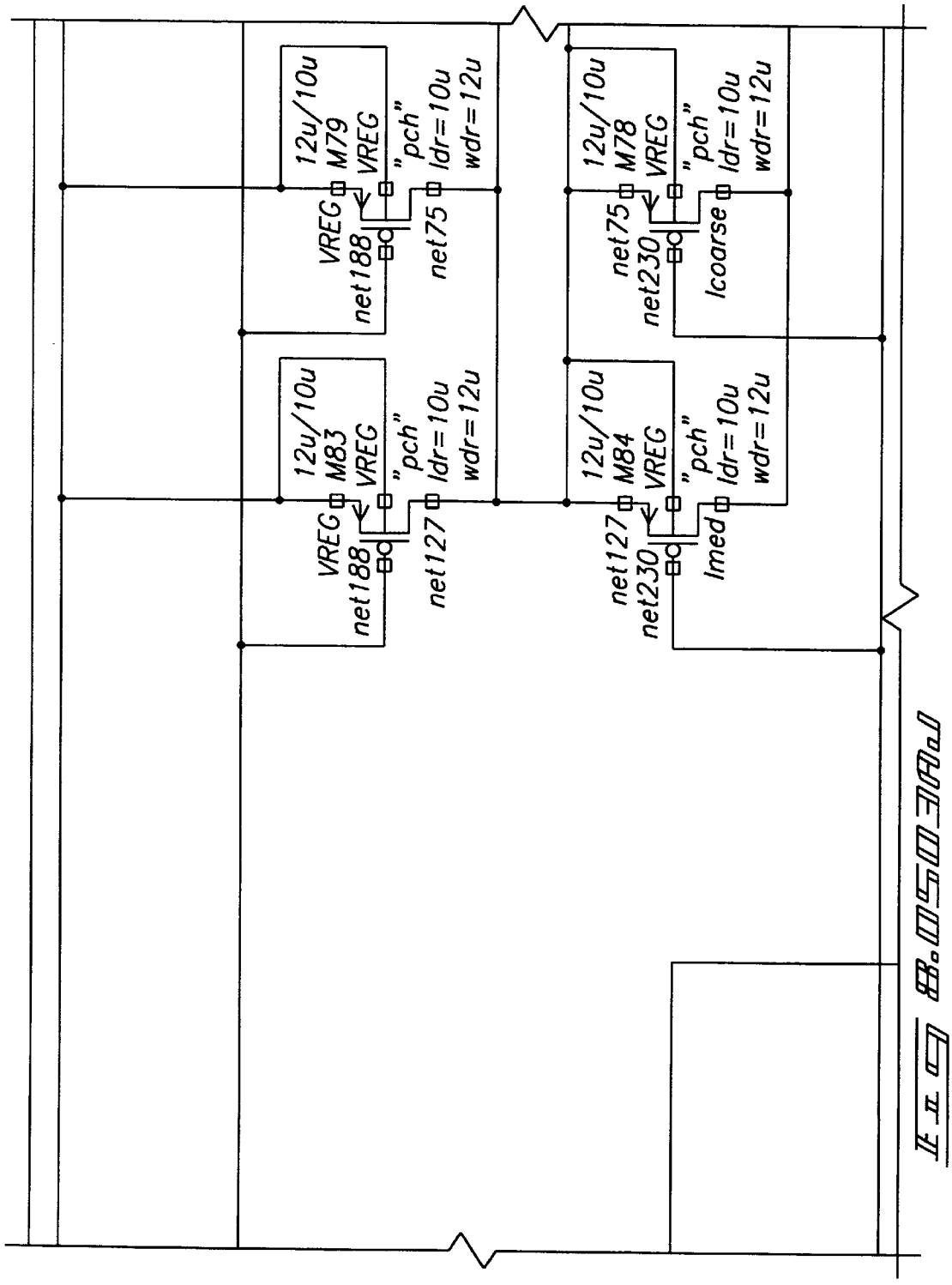

12u/10u
M79
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net75
12u/10u
M78
VREG
"pch"
ldr=10u
wdr=12u
net75
net230
lcoarse
12u/10u
M83
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net127
12u/10u
M84
VREG
"pch"
ldr=10u
wdr=12u
net127
net230
lmed

FIG 8.0500

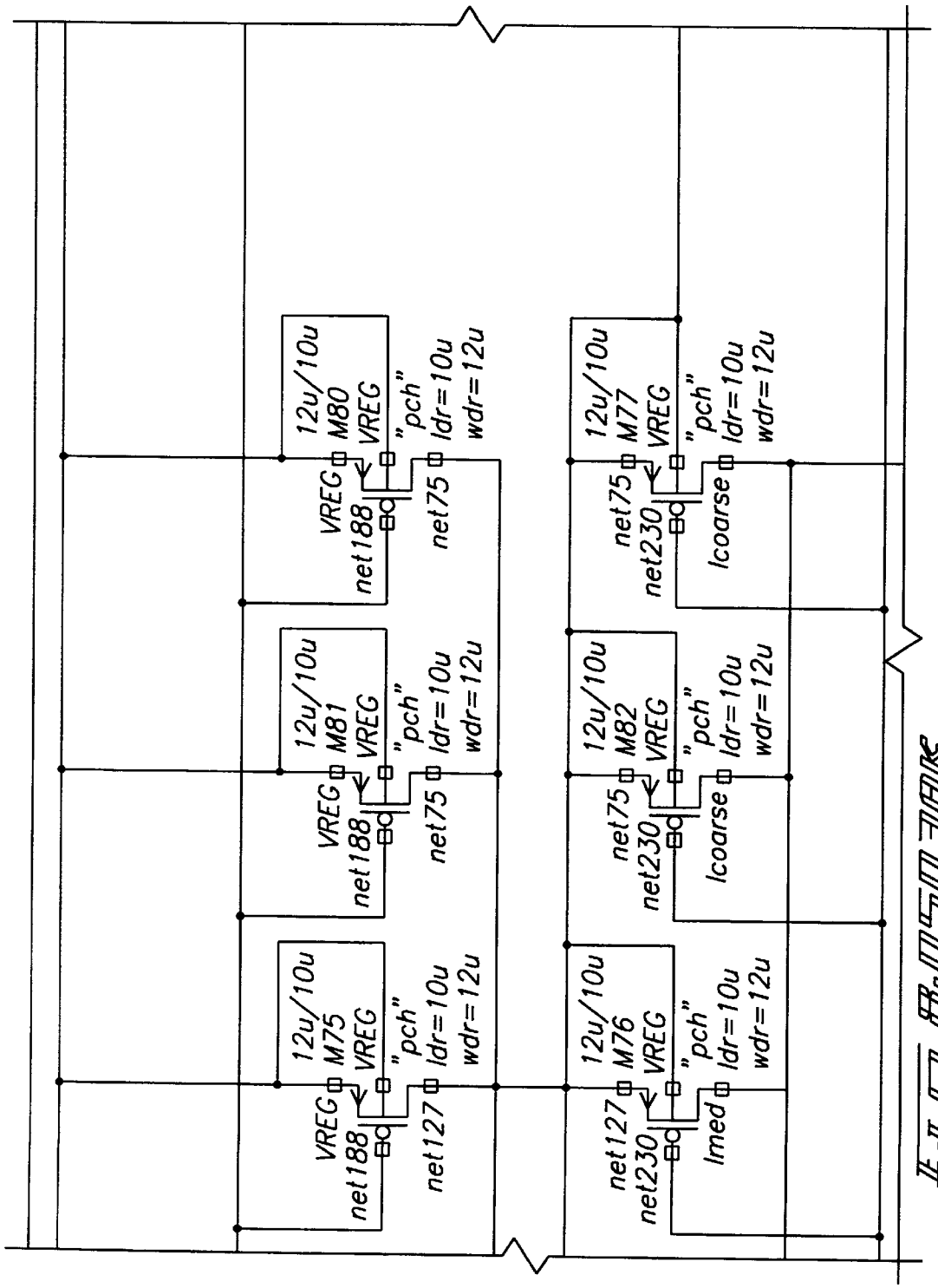


FIG 88.0500 PRIOR ART

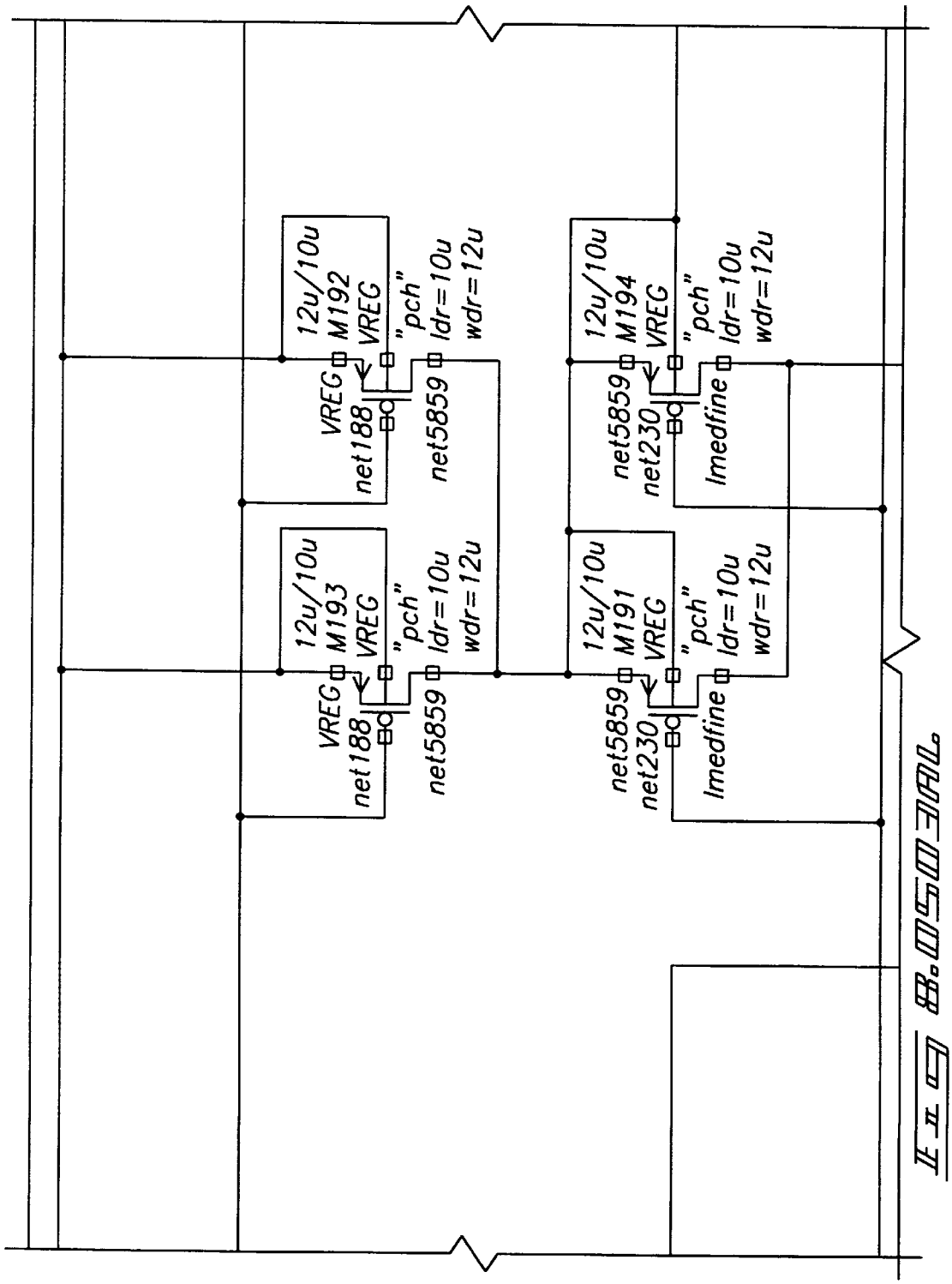
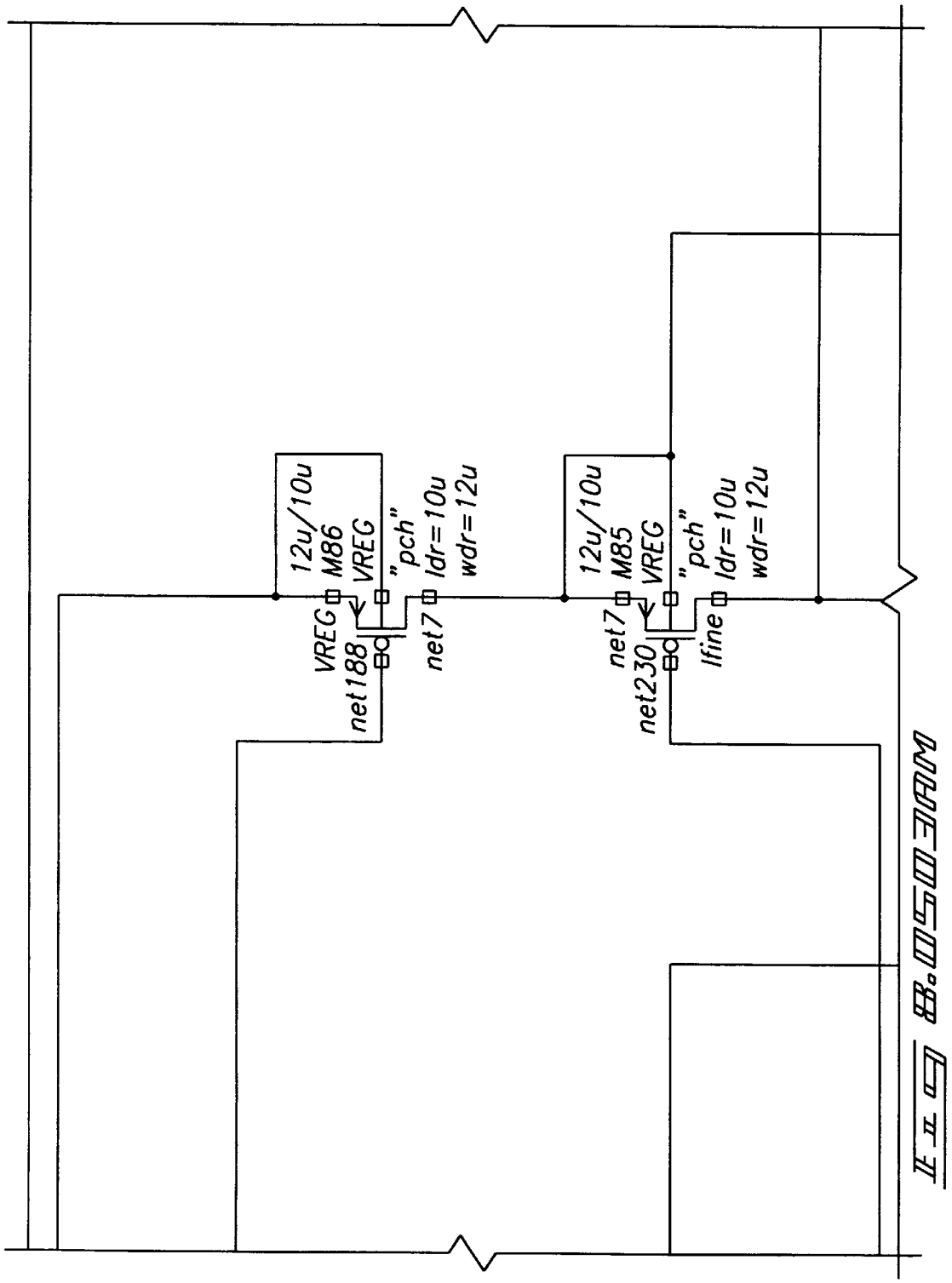

12u/10u
M192
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net5859
12u/10u
M193
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net5859
12u/10u
M194
VREG
"pch"
ldr=10u
wdr=12u
net5859
net230
lmedfine
12u/10u
M191
VREG
"pch"
ldr=10u
wdr=12u
net5859
net230
lmedfine

FIG 8,050


12u/10u
M86
VREG
"pch"
ldr=10u
wdr=12u
VREG
net188
net7
12u/10u
M85
VREG
"pch"
ldr=10u
wdr=12u
net7
net230
lfine
WAVE 0.50 0.88

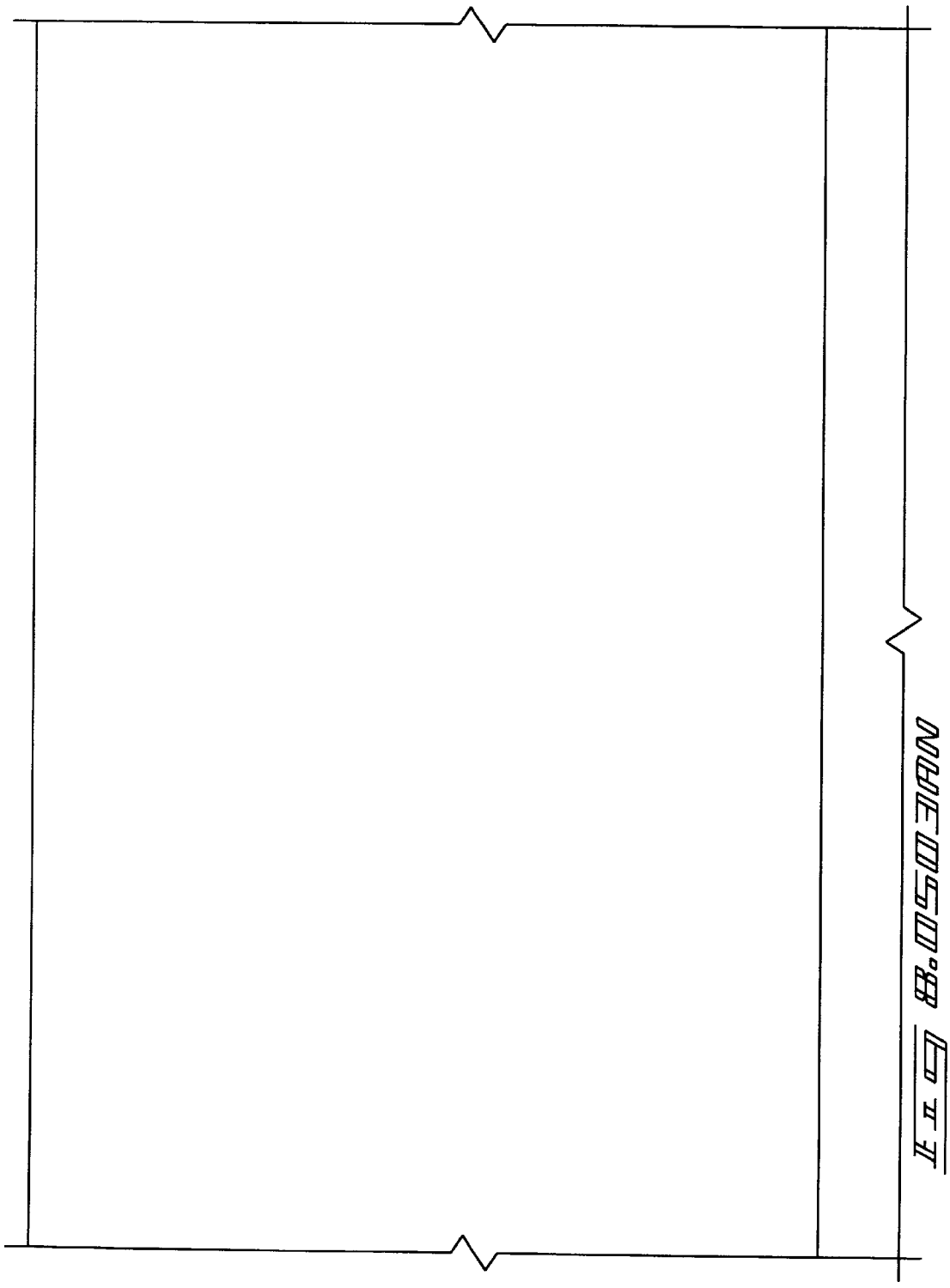
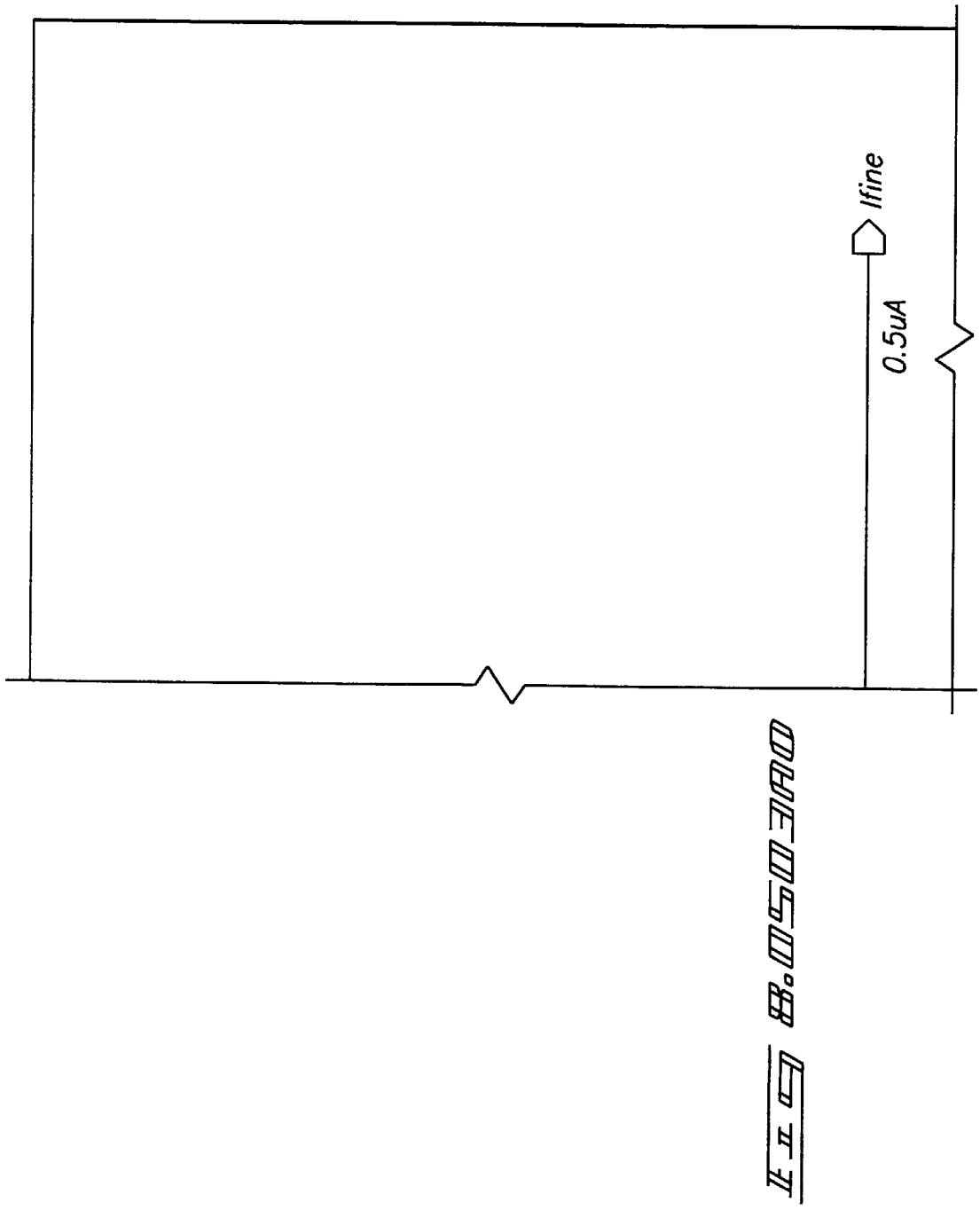


FIG 88,050


Ifine
0.5uA
FIG 8,0500 DAE

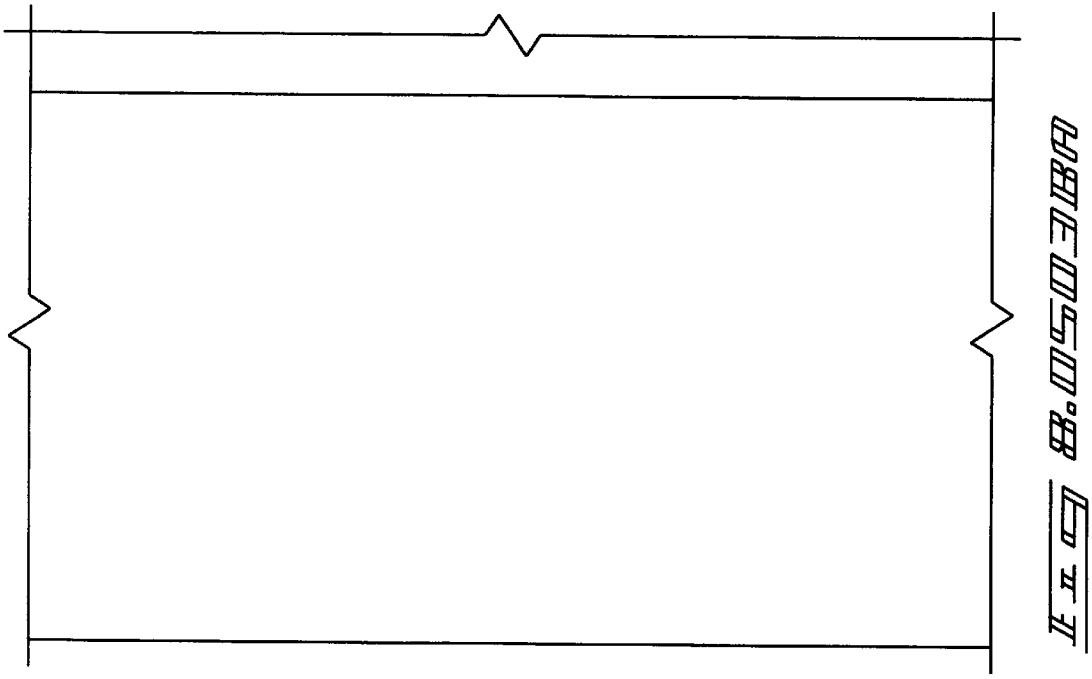


FIG 88.0500 VALUE

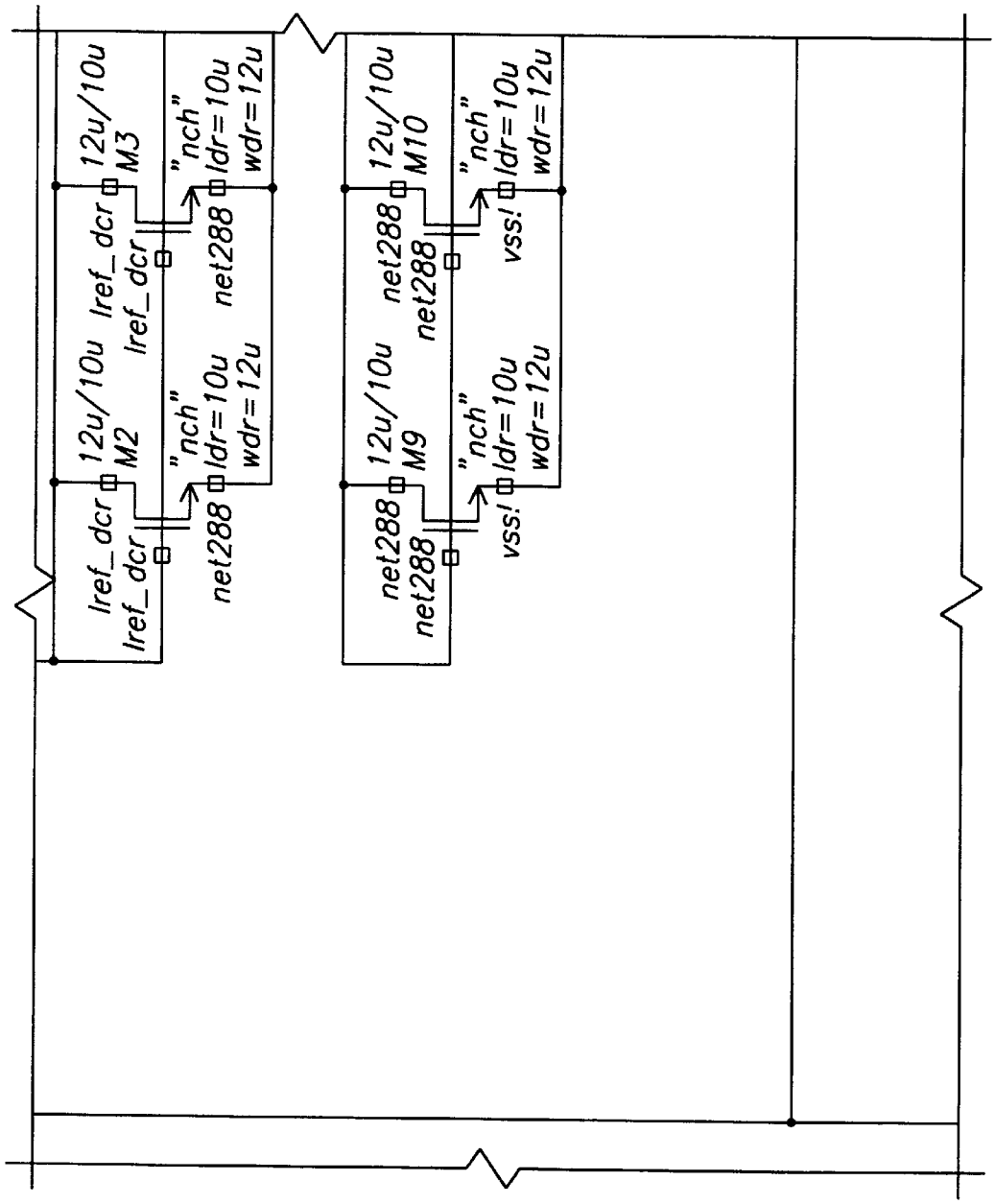

12u/10u
M3
"nch"
ldr=10u
wdr=12u
Iref_dcr
net288
12u/10u
M2
"nch"
ldr=10u
wdr=12u
Iref_dcr
Iref_dcr
net288
12u/10u
M10
"nch"
ldr=10u
wdr=12u
net288
vss!
12u/10u
M9
"nch"
ldr=10u
wdr=12u
net288
vss!
net288

FIG 88,005

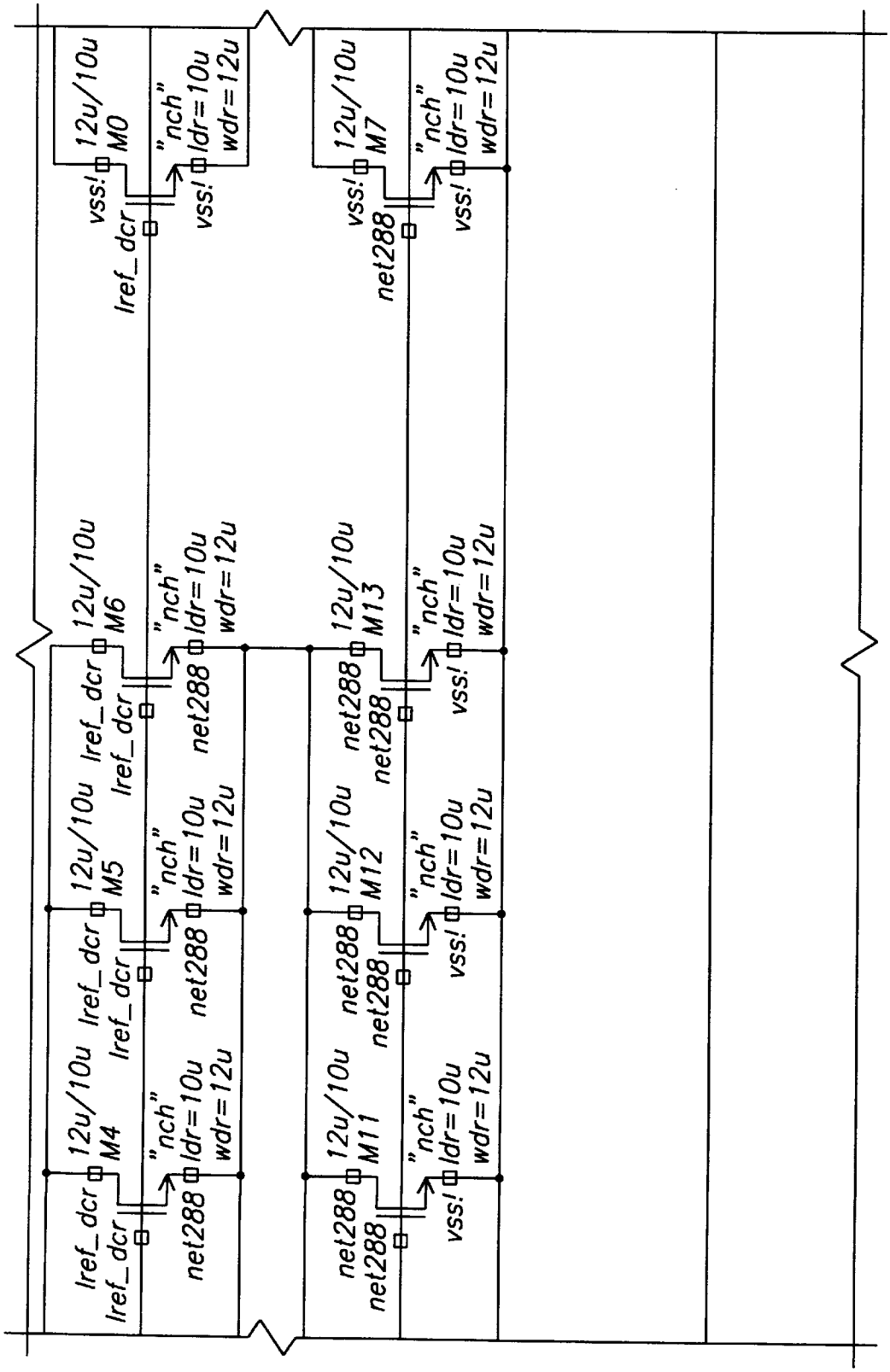

12u/10u
M0
"nch"
ldr=10u
wdr=12u
vss!
lref_dcr
12u/10u
M6
12u/10u
M5
12u/10u
M4
net288
12u/10u
M7
12u/10u
M13
12u/10u
M12
12u/10u
M11

FIG 88.0500

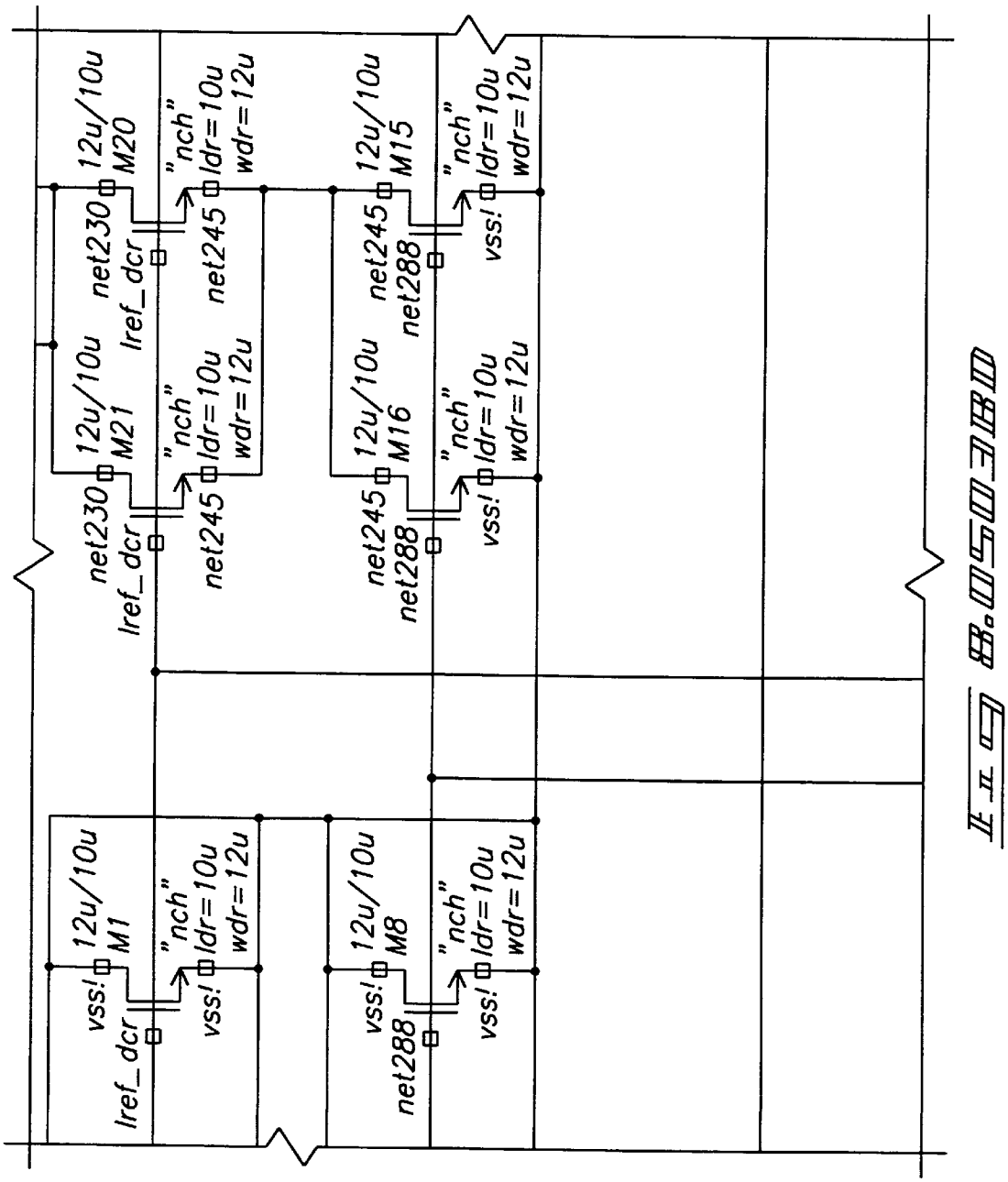

12u/10u
M1
"nch"
ldr=10u
wdr=12u
vss!
lref_dcr
12u/10u
M21
net230
net245
12u/10u
M20
12u/10u
M8
12u/10u
M16
12u/10u
M15
net288

FIG 89.0500

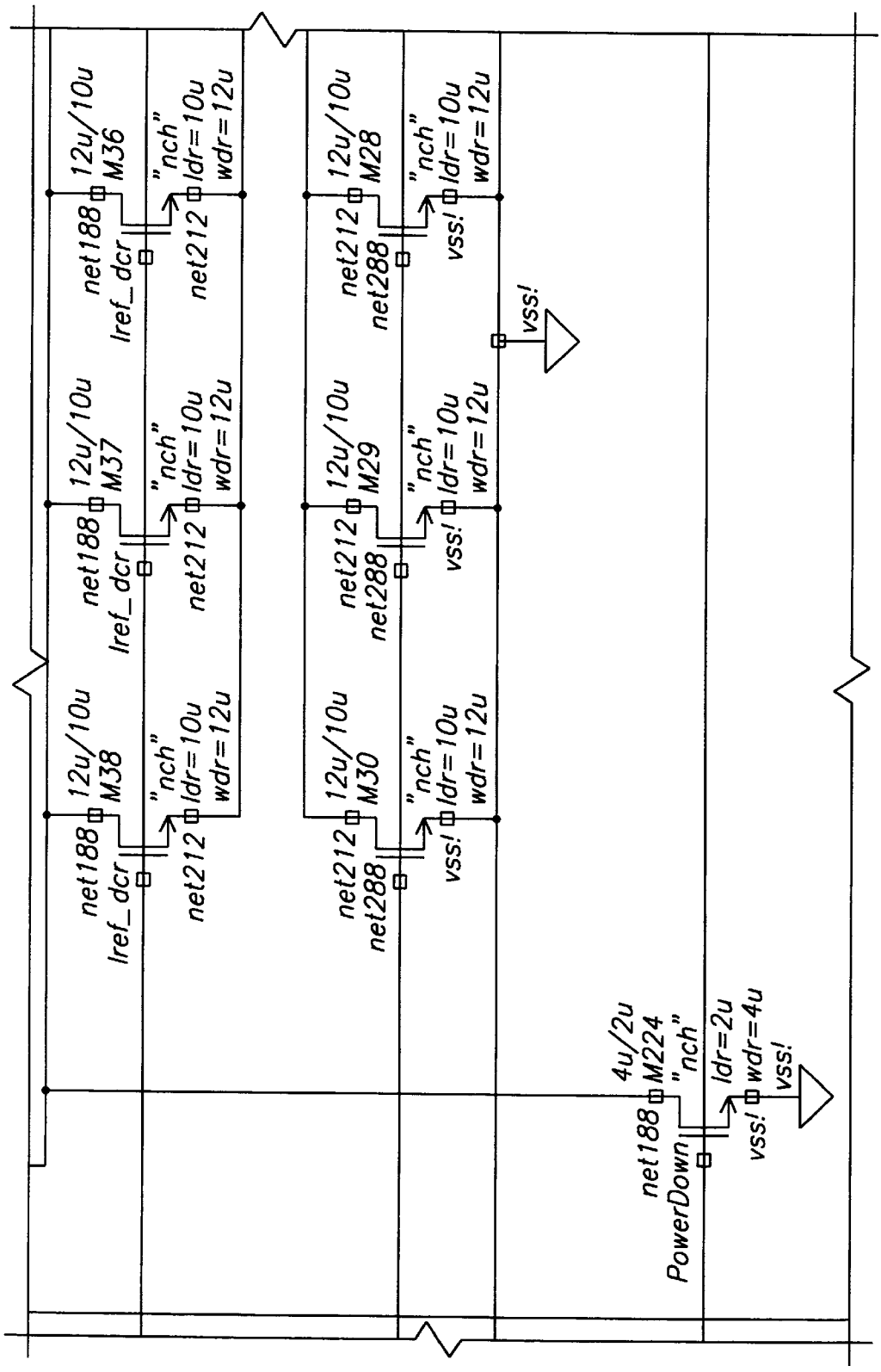

12u/10u
M36
"nch"
ldr=10u
wdr=12u
net188
lref_dcr
net212
12u/10u
M37
"nch"
ldr=10u
wdr=12u
net188
lref_dcr
net212
12u/10u
M38
"nch"
ldr=10u
wdr=12u
net188
lref_dcr
net212
12u/10u
M28
"nch"
ldr=10u
wdr=12u
net212
net288
vss!
12u/10u
M29
"nch"
ldr=10u
wdr=12u
net212
net288
vss!
12u/10u
M30
"nch"
ldr=10u
wdr=12u
net212
net288
vss!
vss!
4u/2u
M224
"nch"
ldr=2u
wdr=4u
net188
PowerDown
vss!
vss!

FIG 88.005E

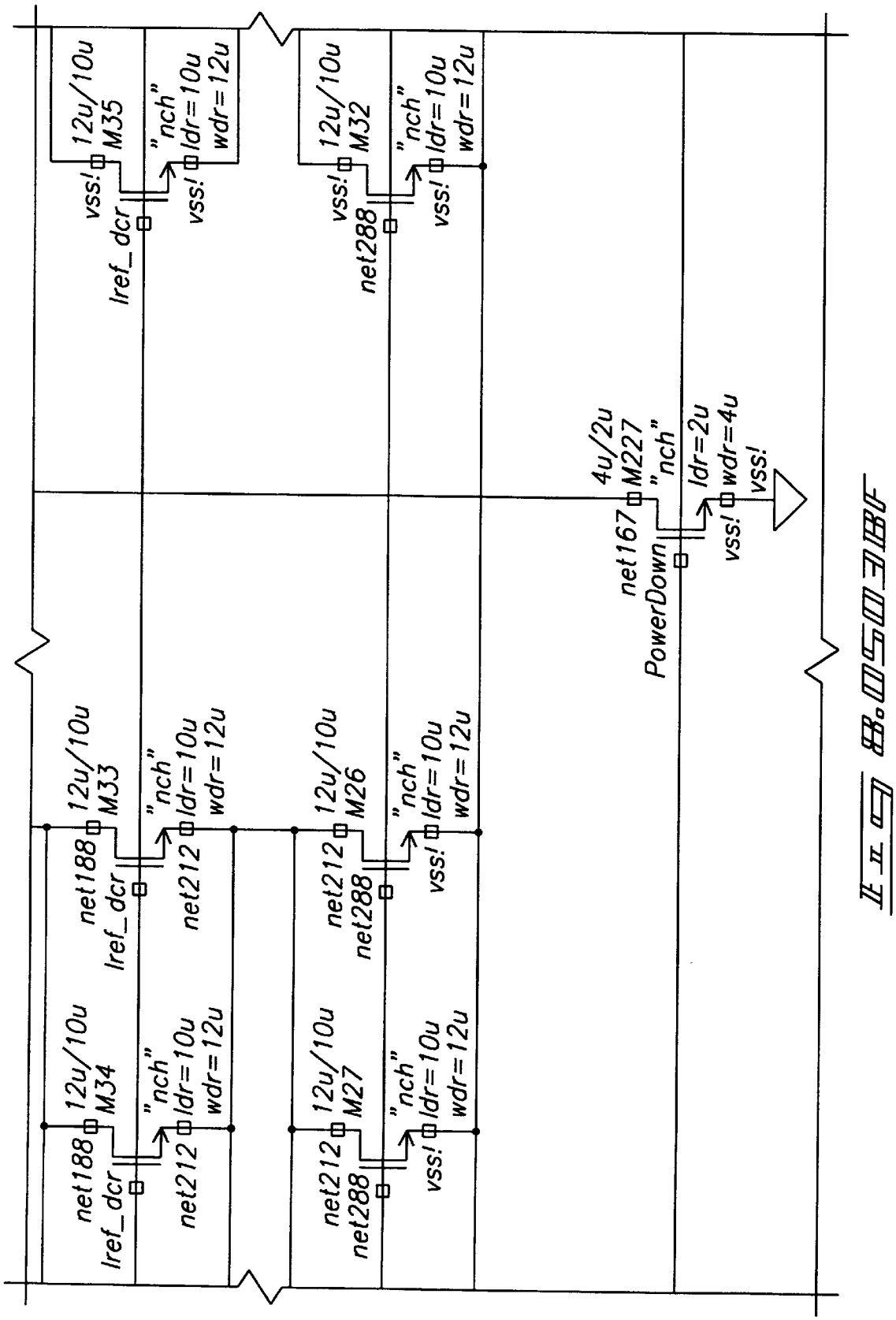

12u/10u
M35
"nch"
ldr=10u
wdr=12u
vss!
lref_dcr
net288
M32
4u/2u
M227
net167
PowerDown
ldr=2u
wdr=4u
net188
M33
net212
M26
M34
M27

FIG. 8.0500E

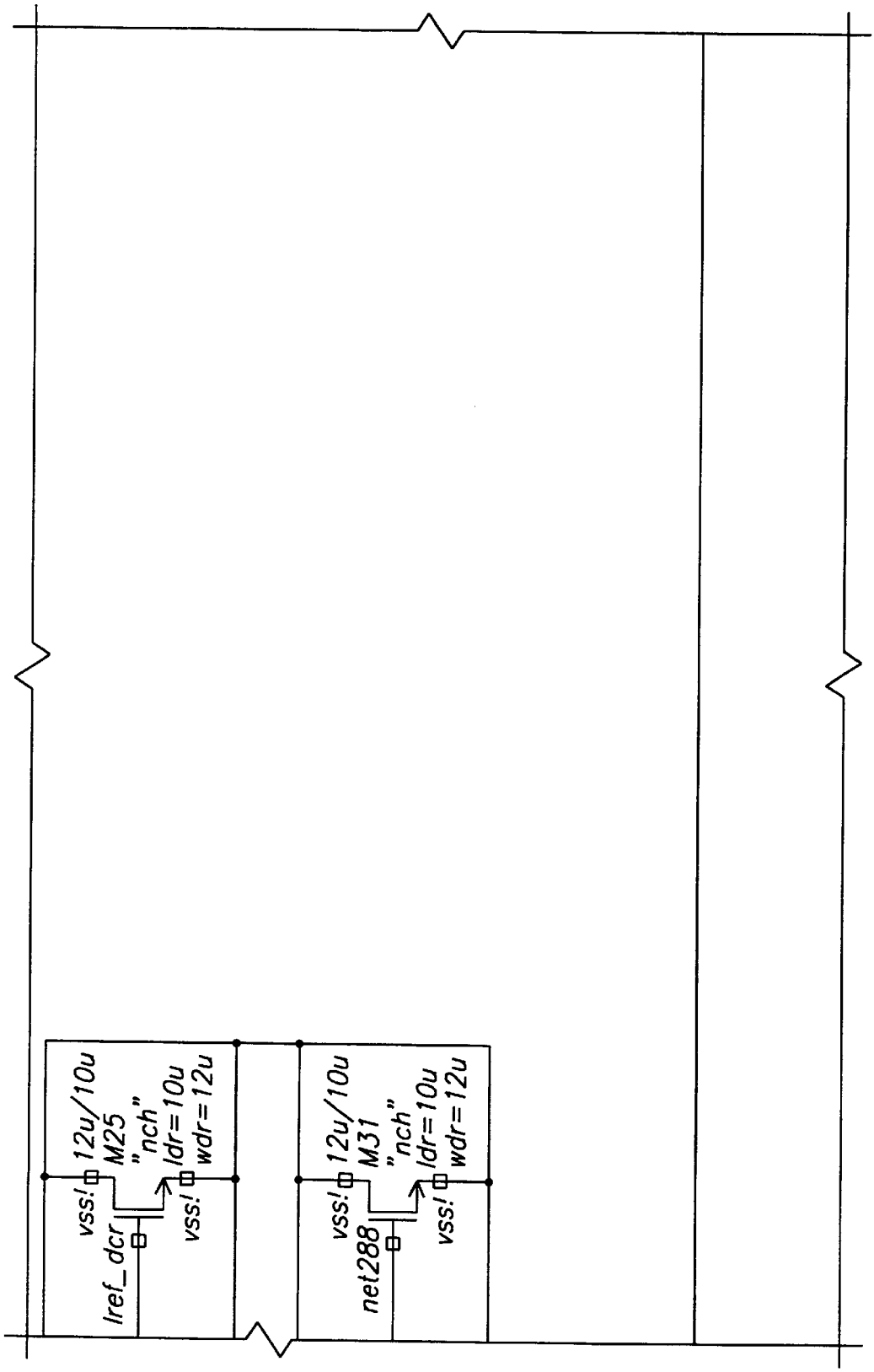

12u/10u
M25
"nch"
ldr=10u
wdr=12u
vss!
lref_dcr
vss!
12u/10u
M31
"nch"
ldr=10u
wdr=12u
vss!
net288
vss!

FIG 88.0500

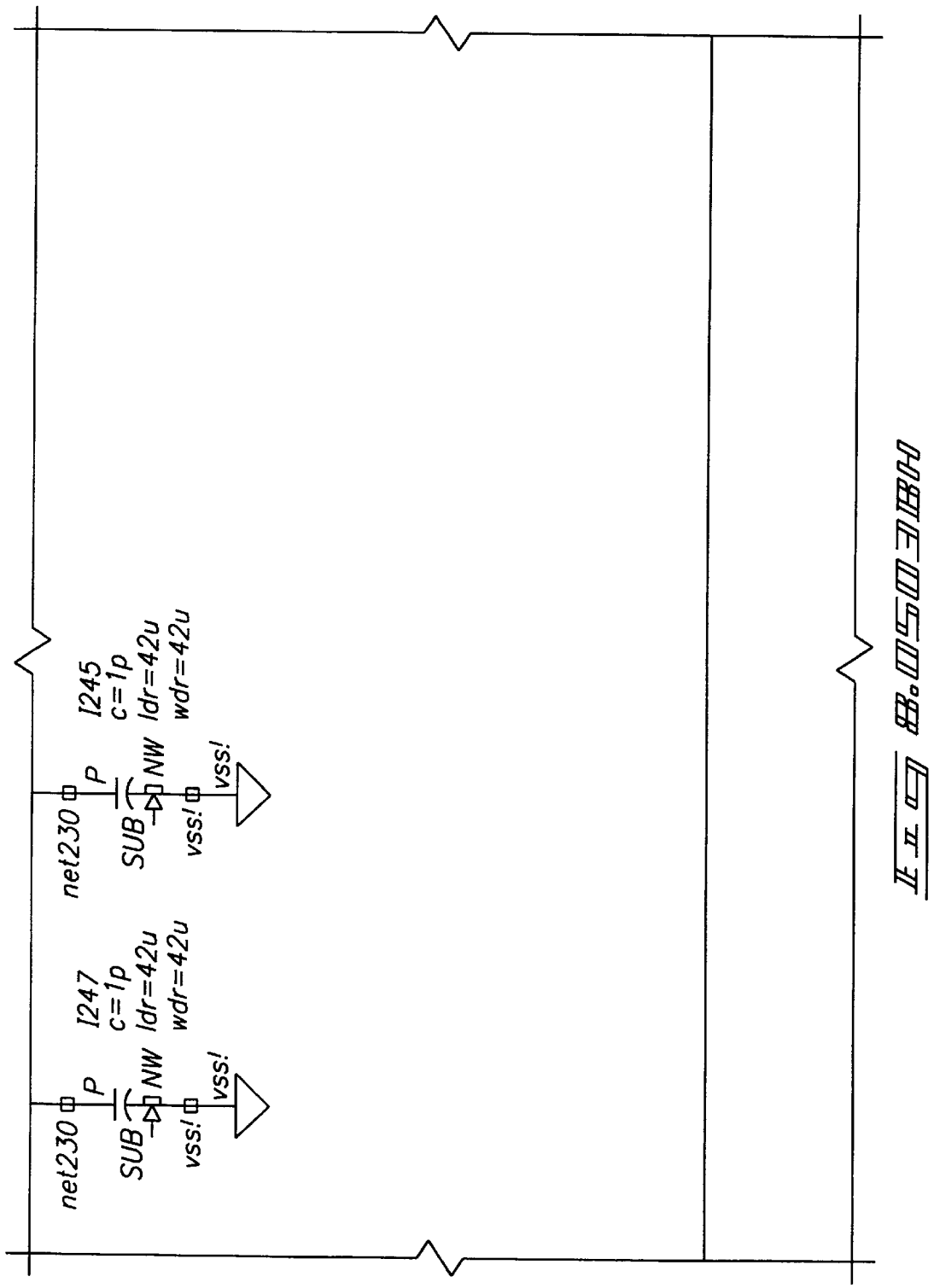

net230
P
SUB
NW
I247
c=1p
ldr=42u
wdr=42u
vss!
vss!
vss!
net230
P
SUB
NW
I245
c=1p
ldr=42u
wdr=42u
vss!
vss!

FIG 1507

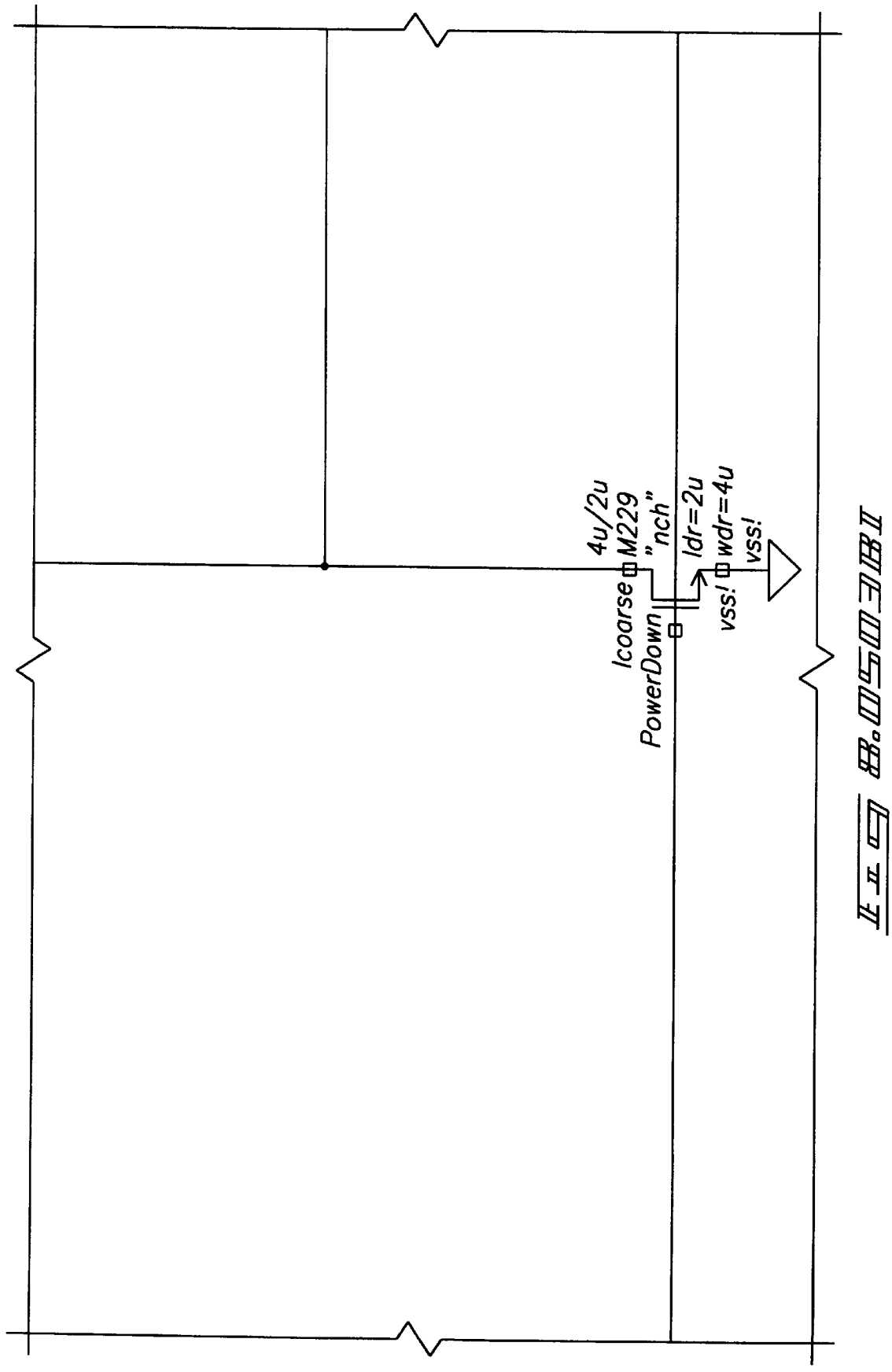


FIG. 88.05

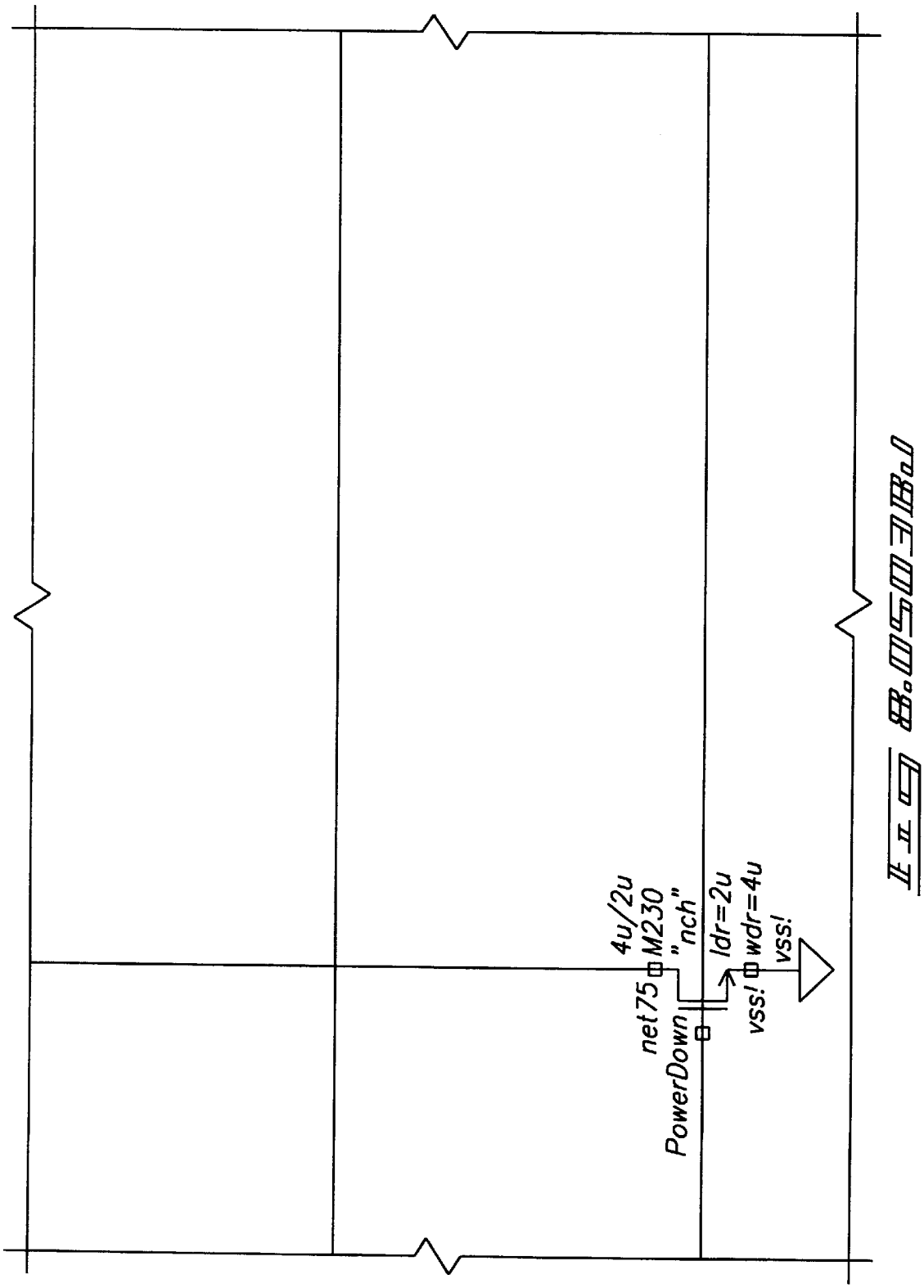


FIG 8,050,811

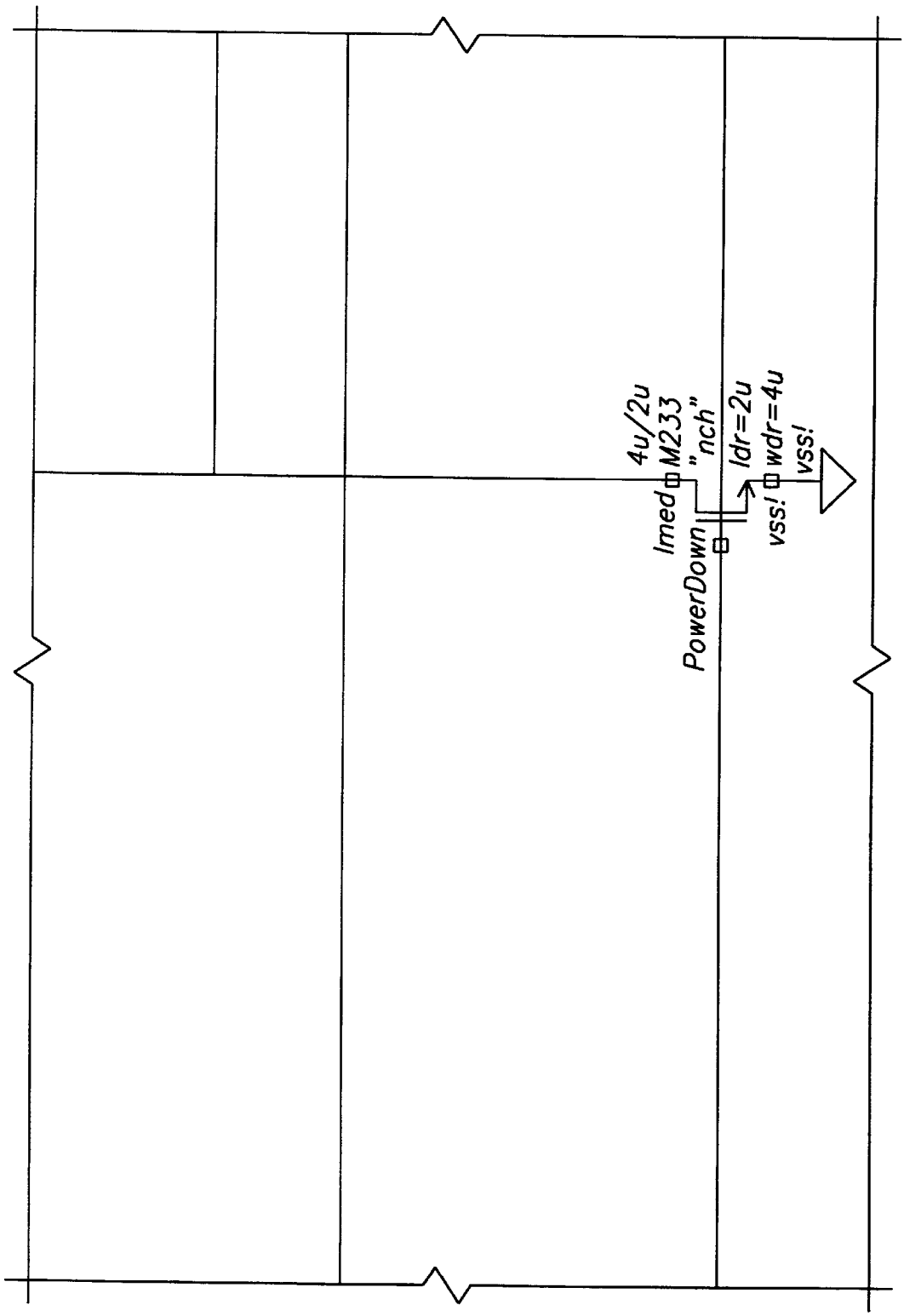


FIG 88.0505E

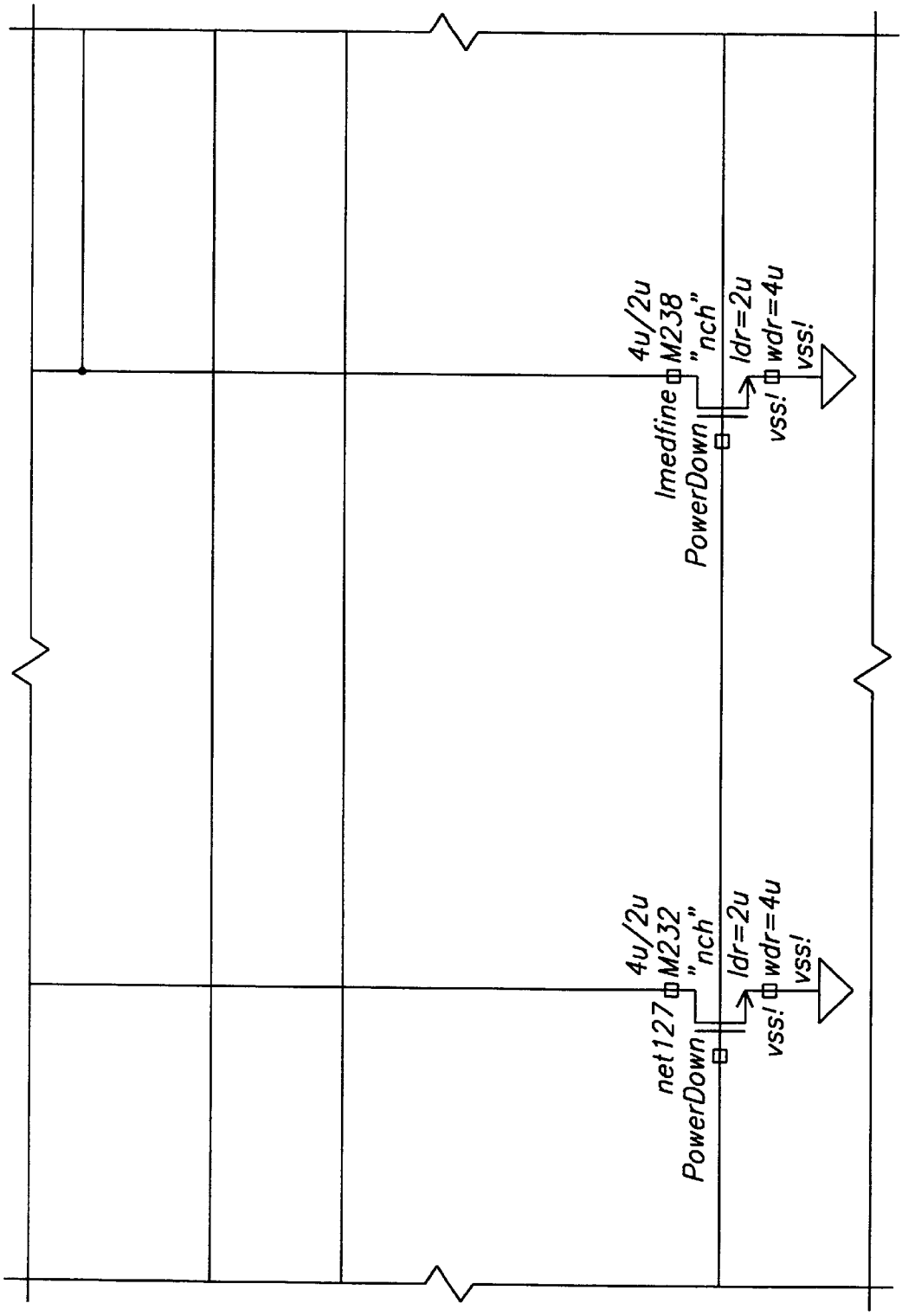

4u/2u
M238
"nch"
ldr=2u
wdr=4u
vss!
Imedfine
PowerDown
vss!
4u/2u
M232
"nch"
ldr=2u
wdr=4u
vss!
net127
PowerDown
vss!

FIG 89.0050

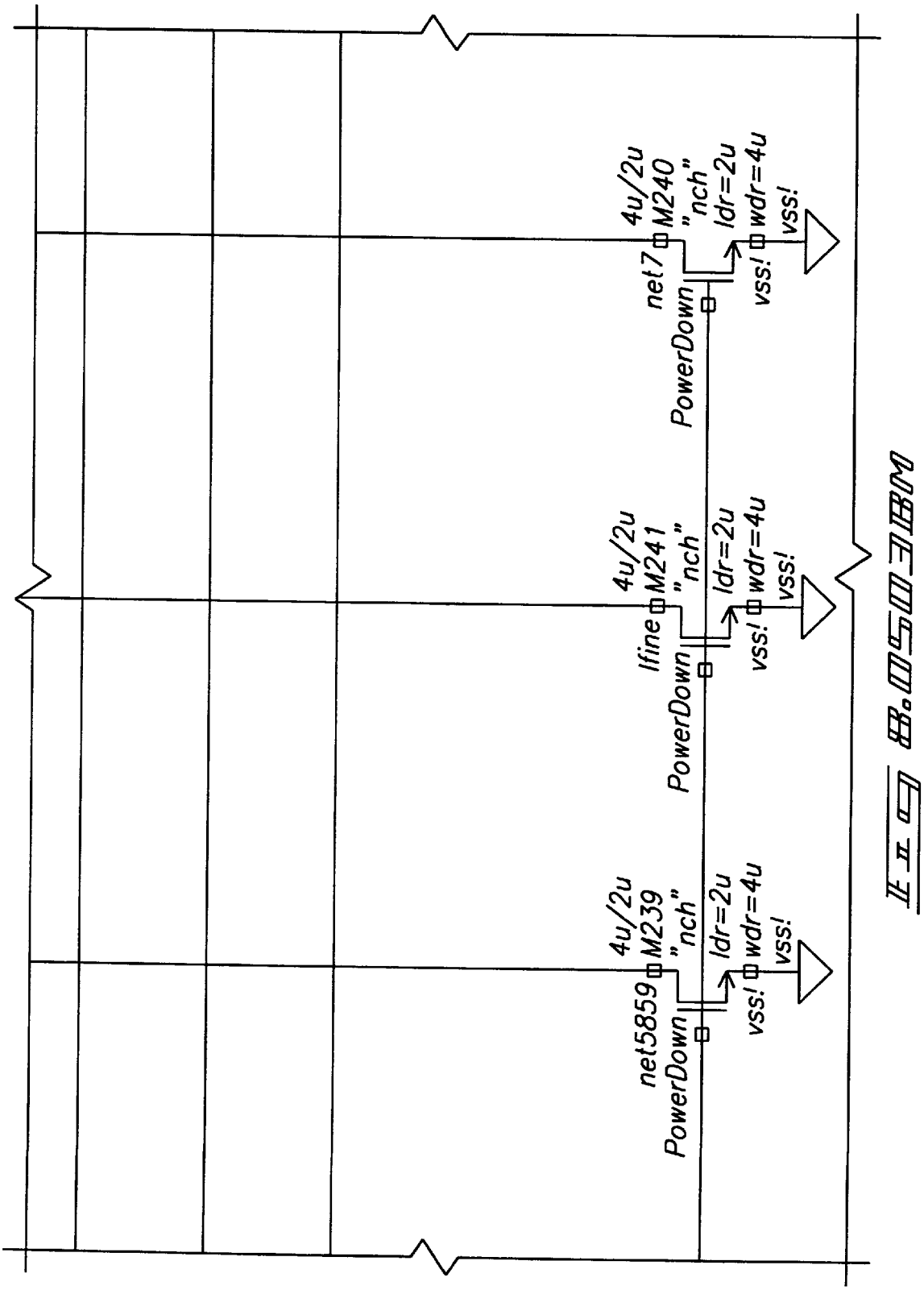


FIG 8.0500 PRIOR ART

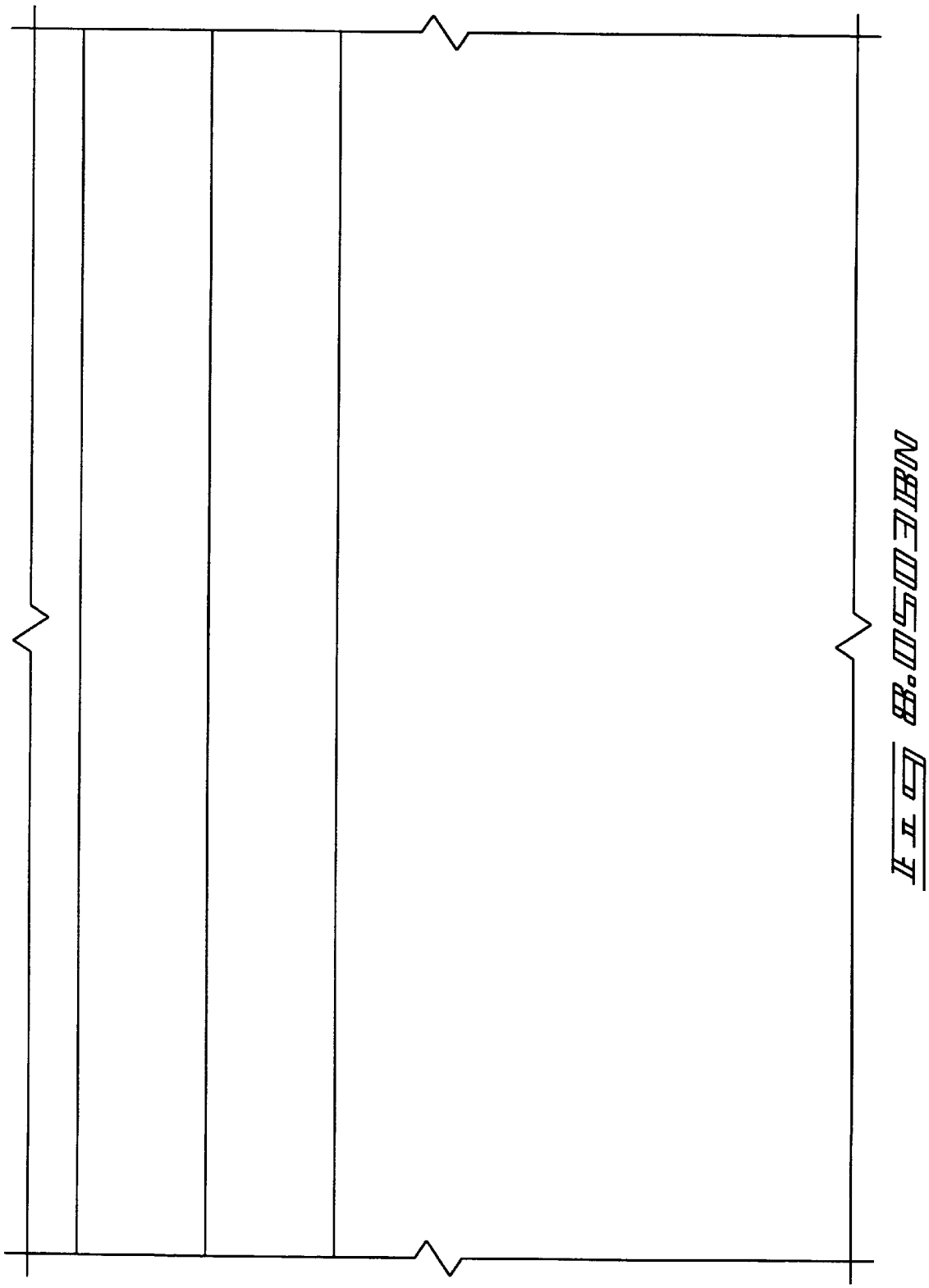


FIG. 88,505

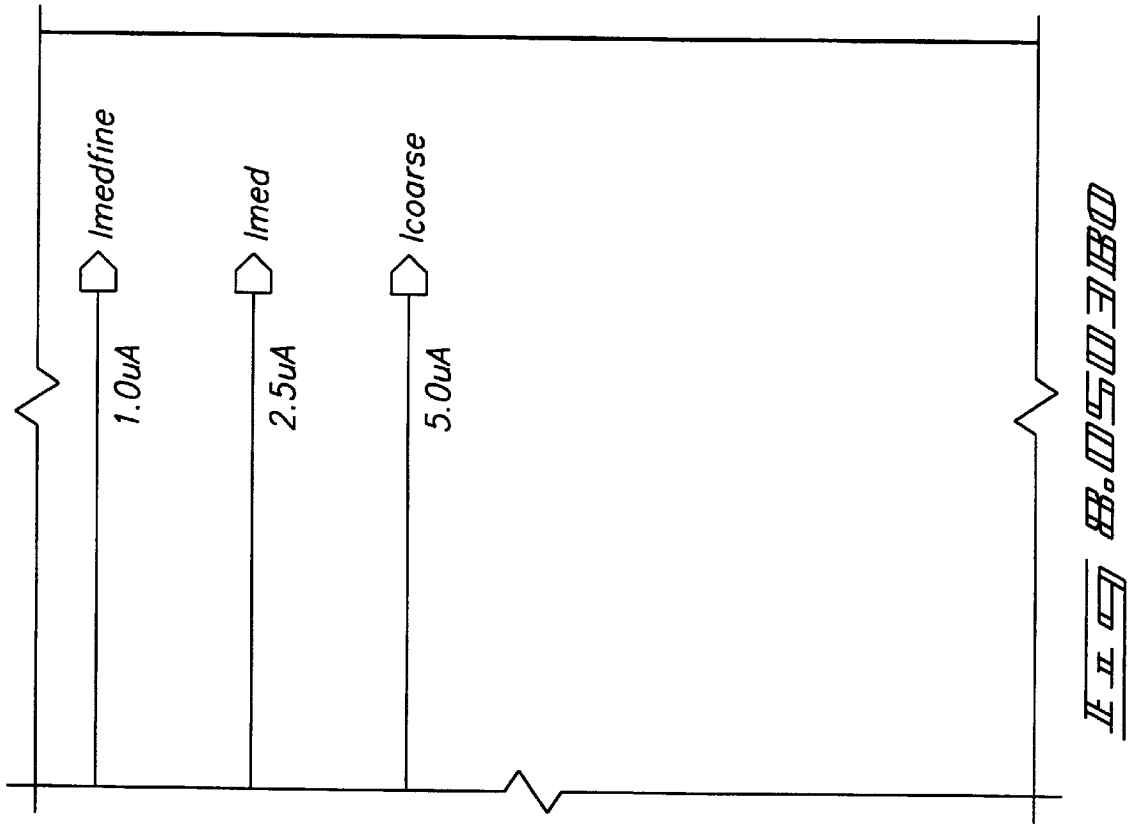


FIG. 805

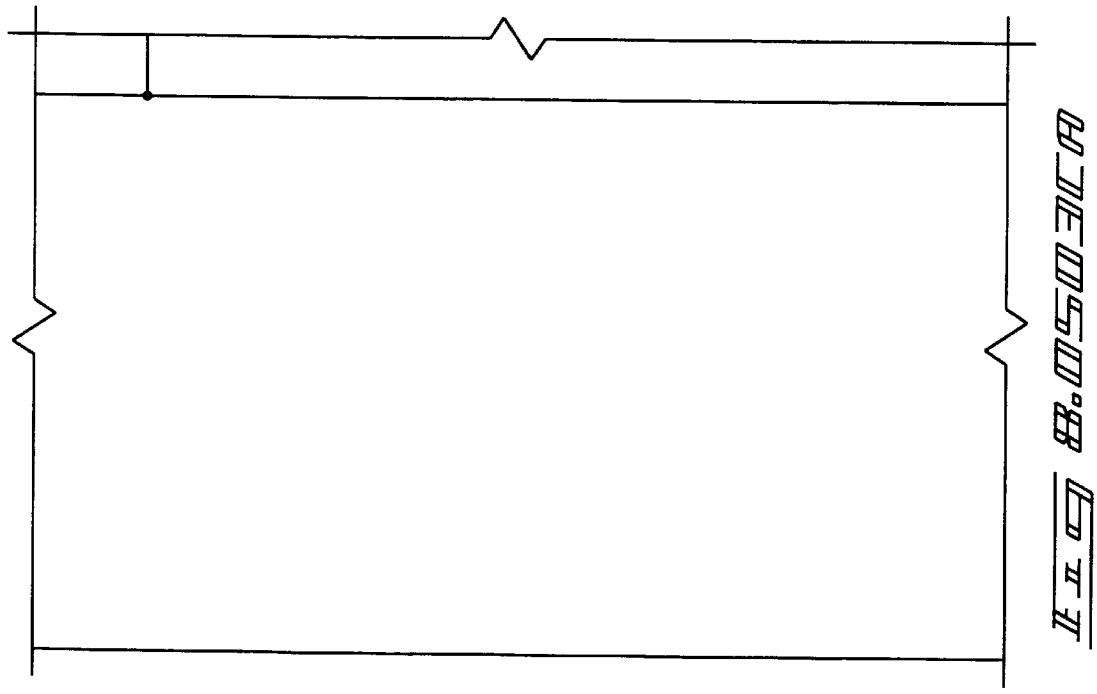


FIG 88,050A

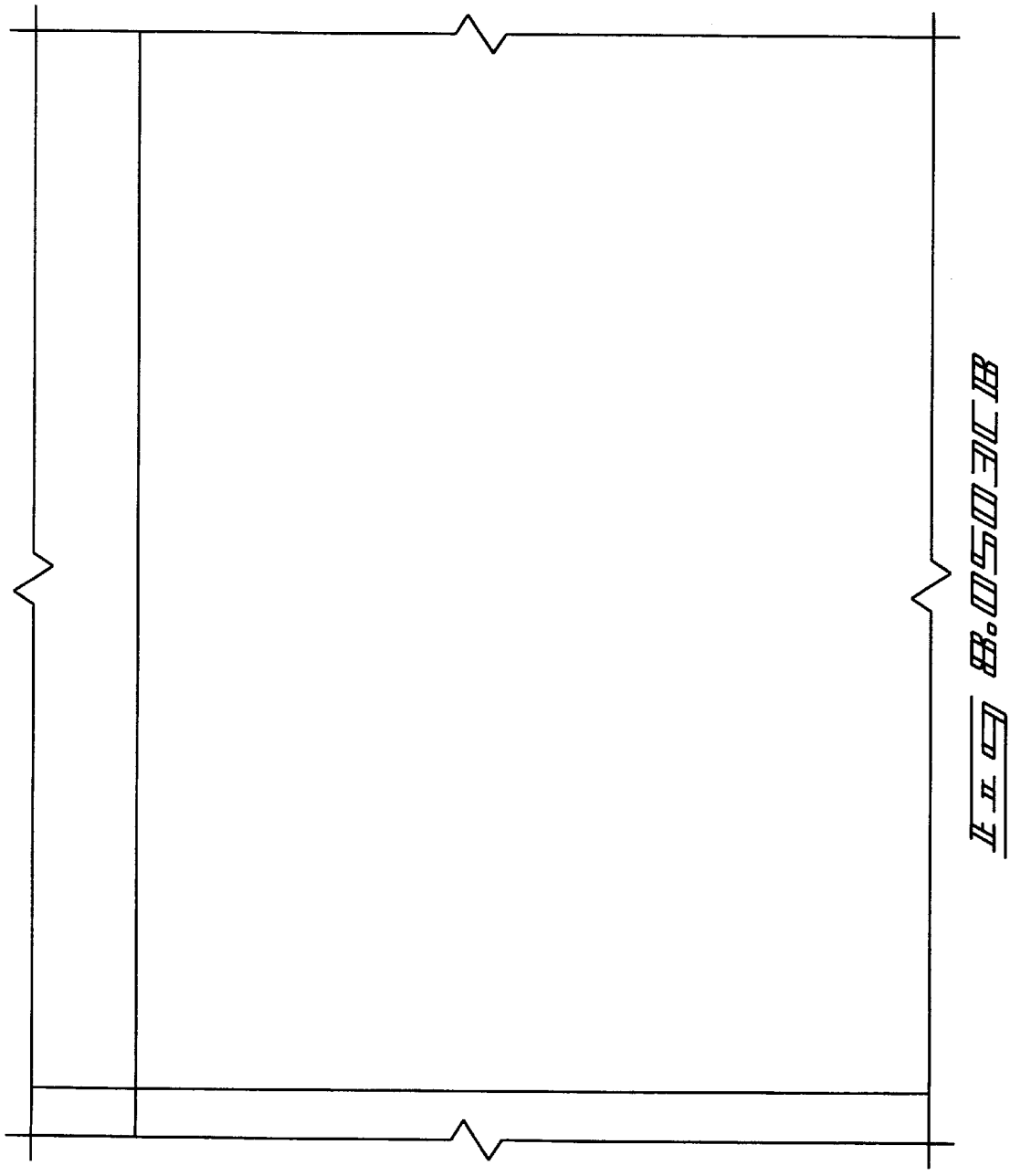


FIG 08 DUPLEX

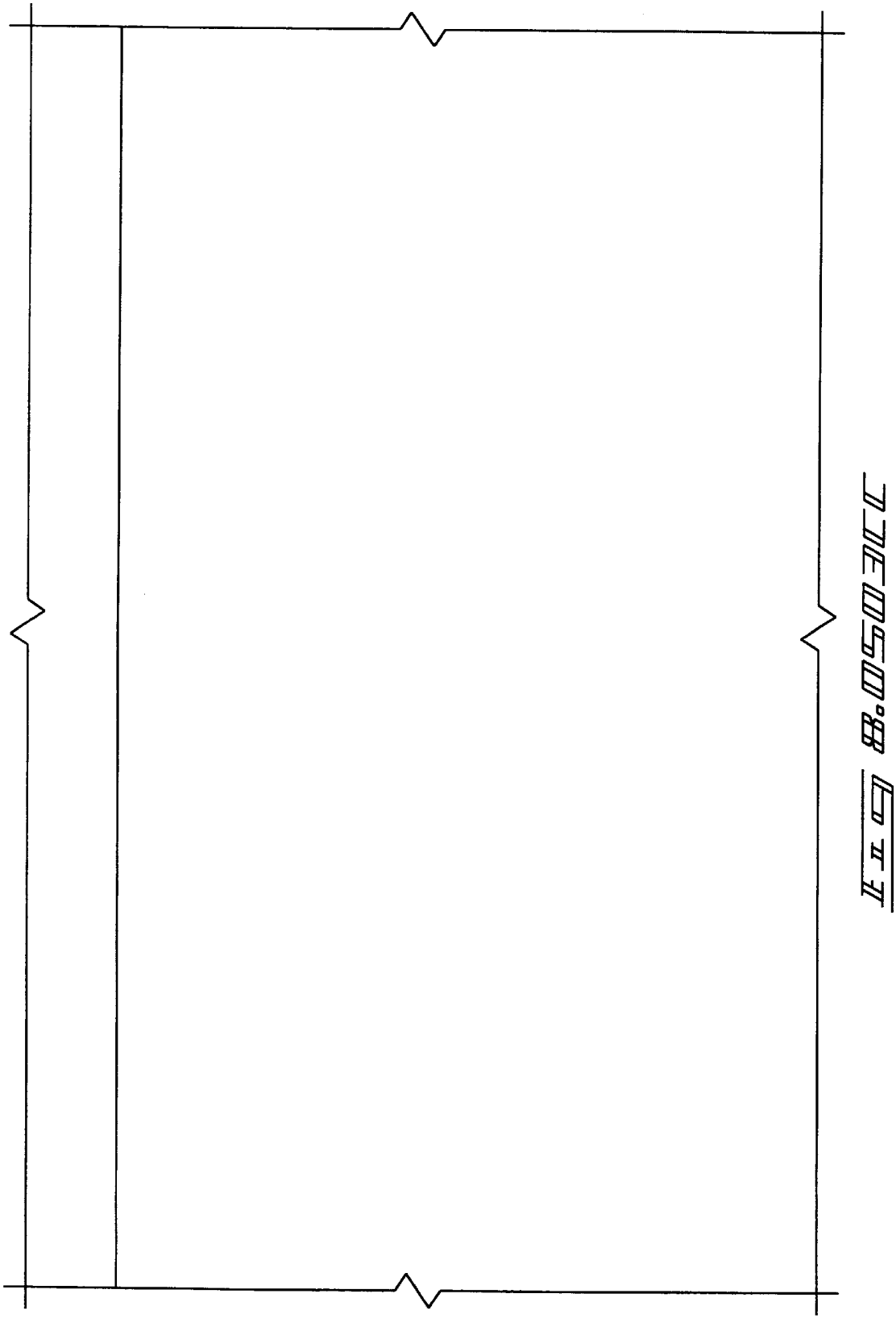


FIG 88,050

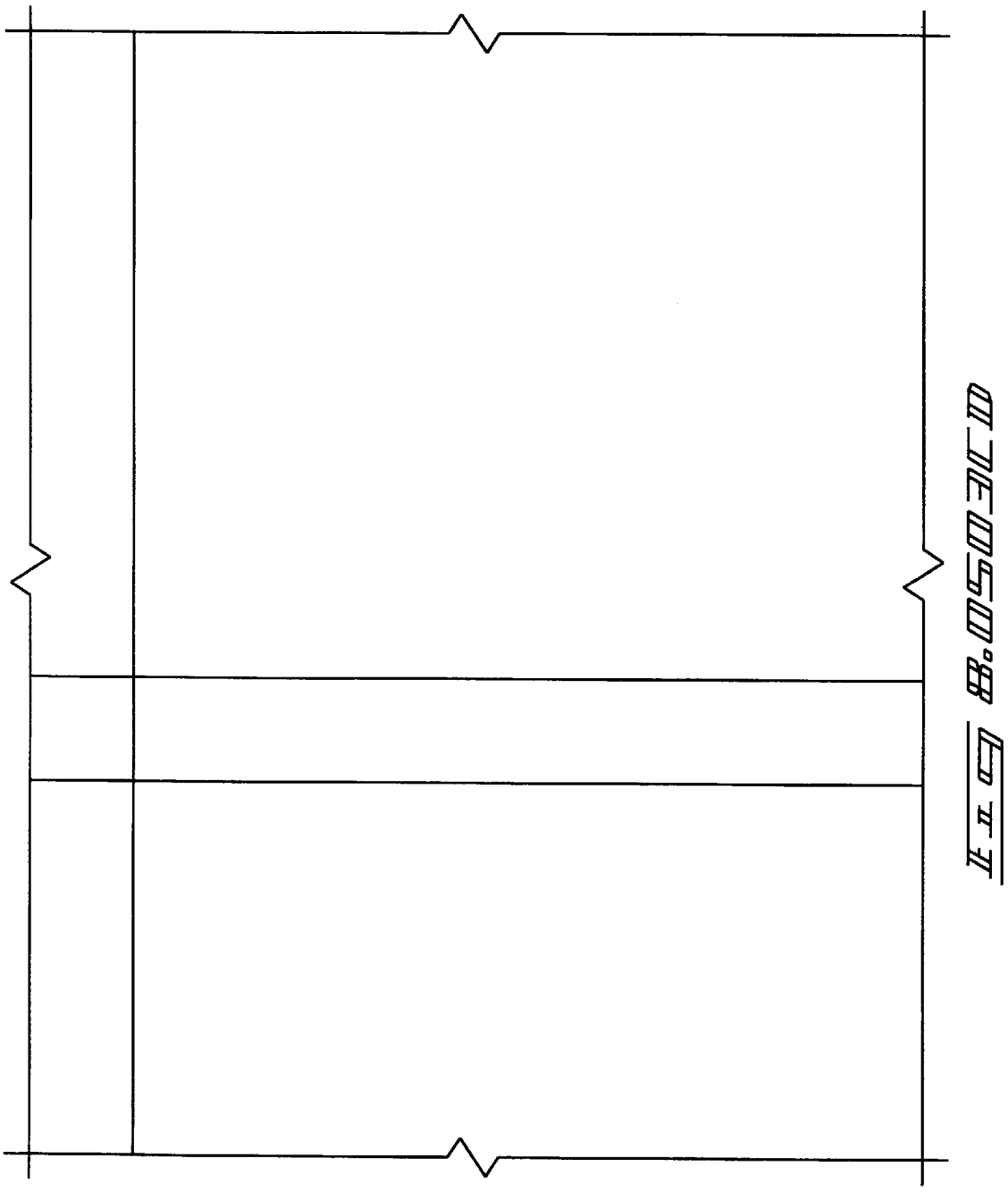


FIG. 31
DE05008.dgn

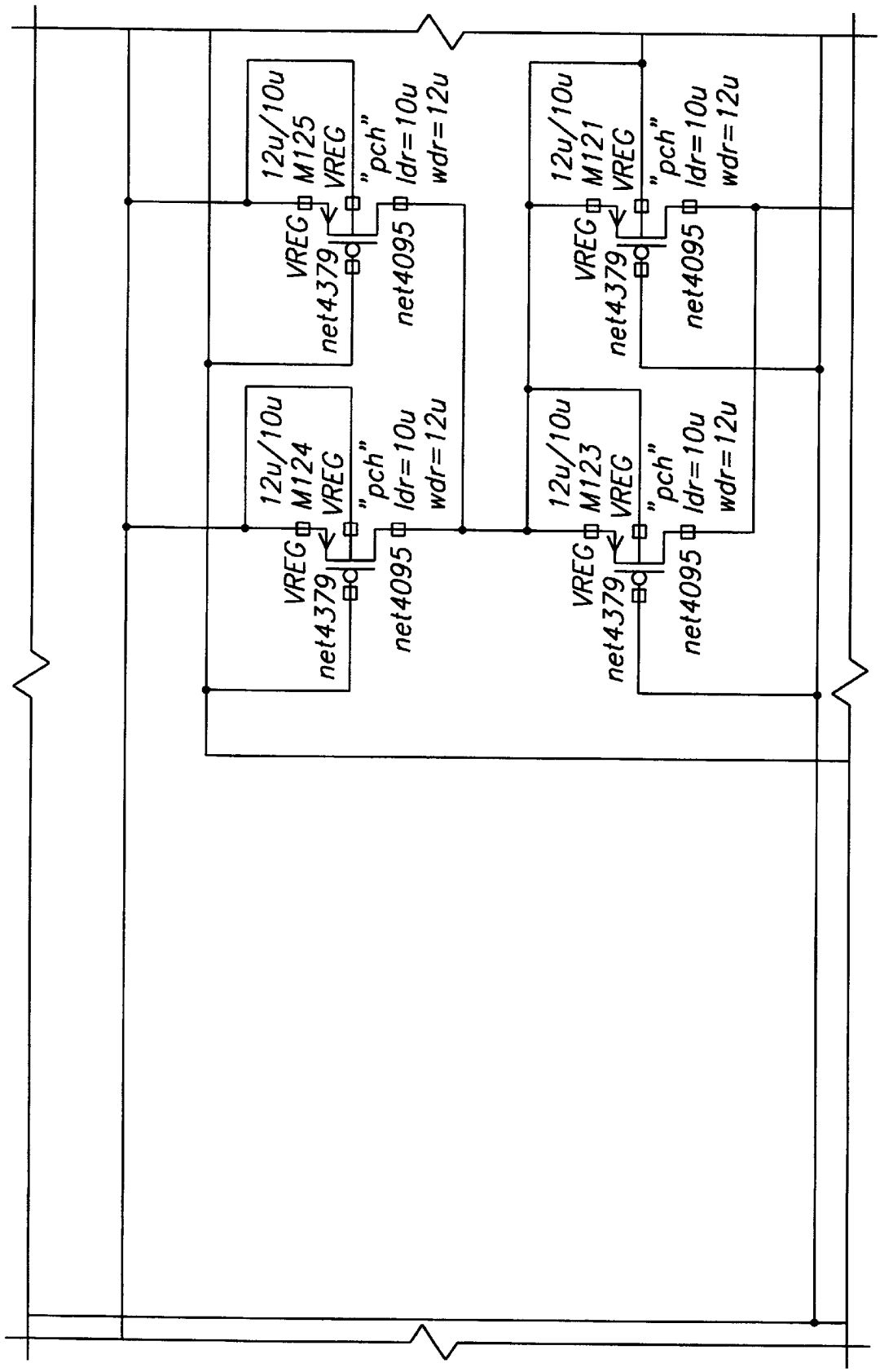

12u/10u
M125
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4095
12u/10u
M121
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4095
12u/10u
M124
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4095
12u/10u
M123
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4095

FIG. 88,005

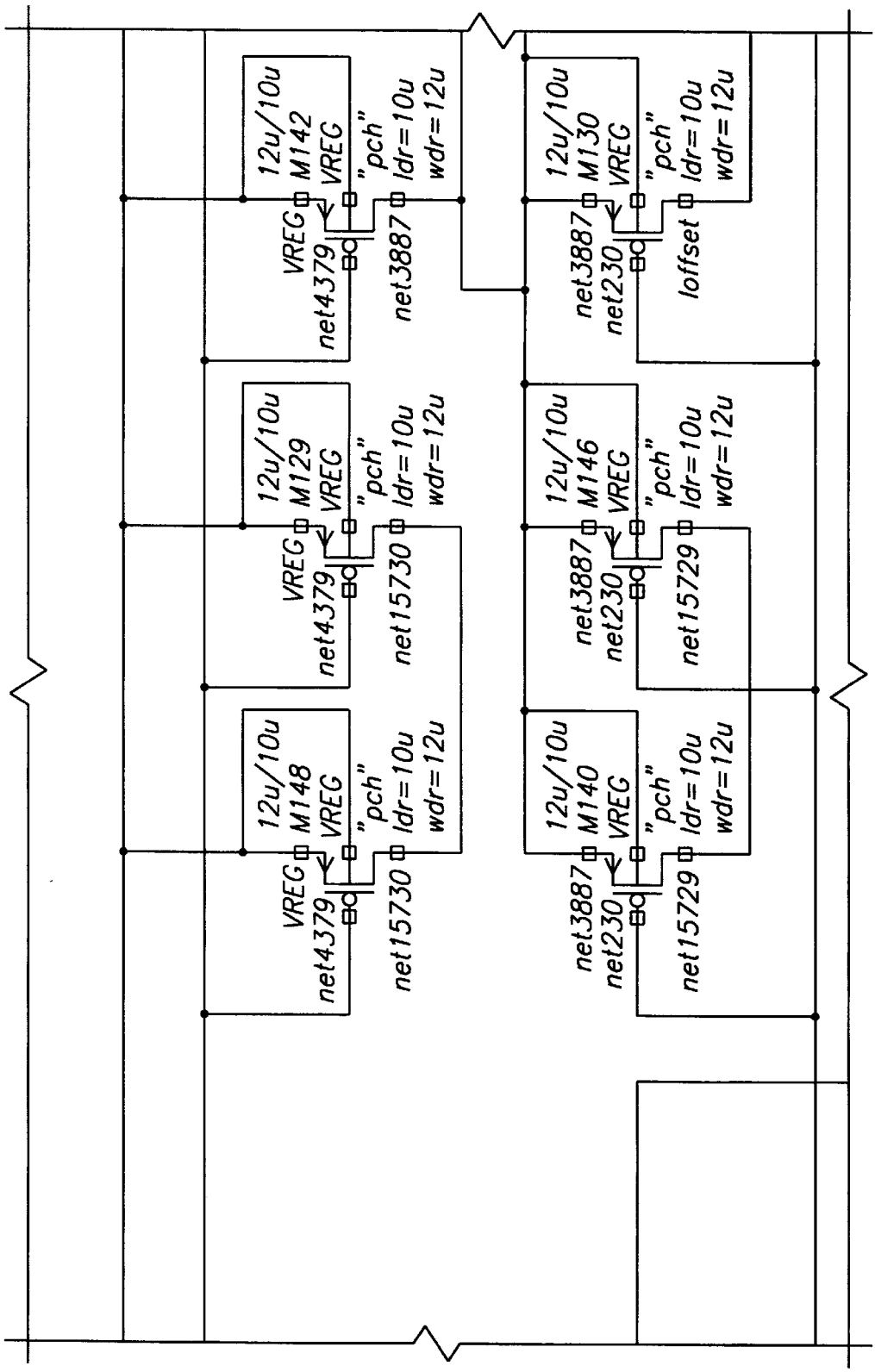

12u/10u
M142
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net3887
12u/10u
M130
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
loffset
12u/10u
M129
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net15730
12u/10u
M146
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
net15729
12u/10u
M148
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net15730
12u/10u
M140
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
net15729

FIG. 8.0505F

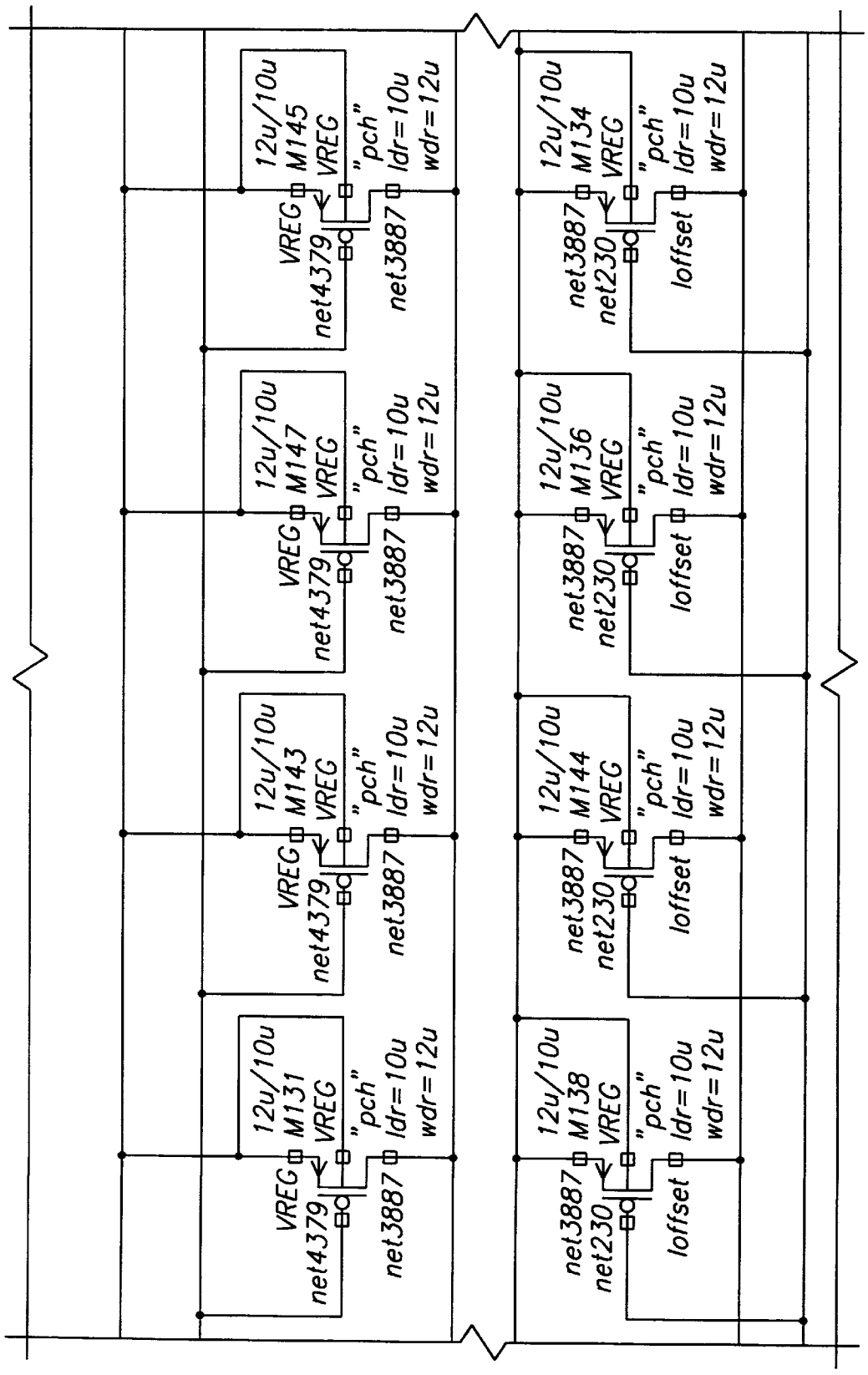

12u/10u
M145
VREG
"pch"
ldr=10u
wdr=12u
net4379
net3887
12u/10u
M147
12u/10u
M143
12u/10u
M131
12u/10u
M134
net230
loffset
12u/10u
M136
12u/10u
M144
12u/10u
M138

FIG 8.0580

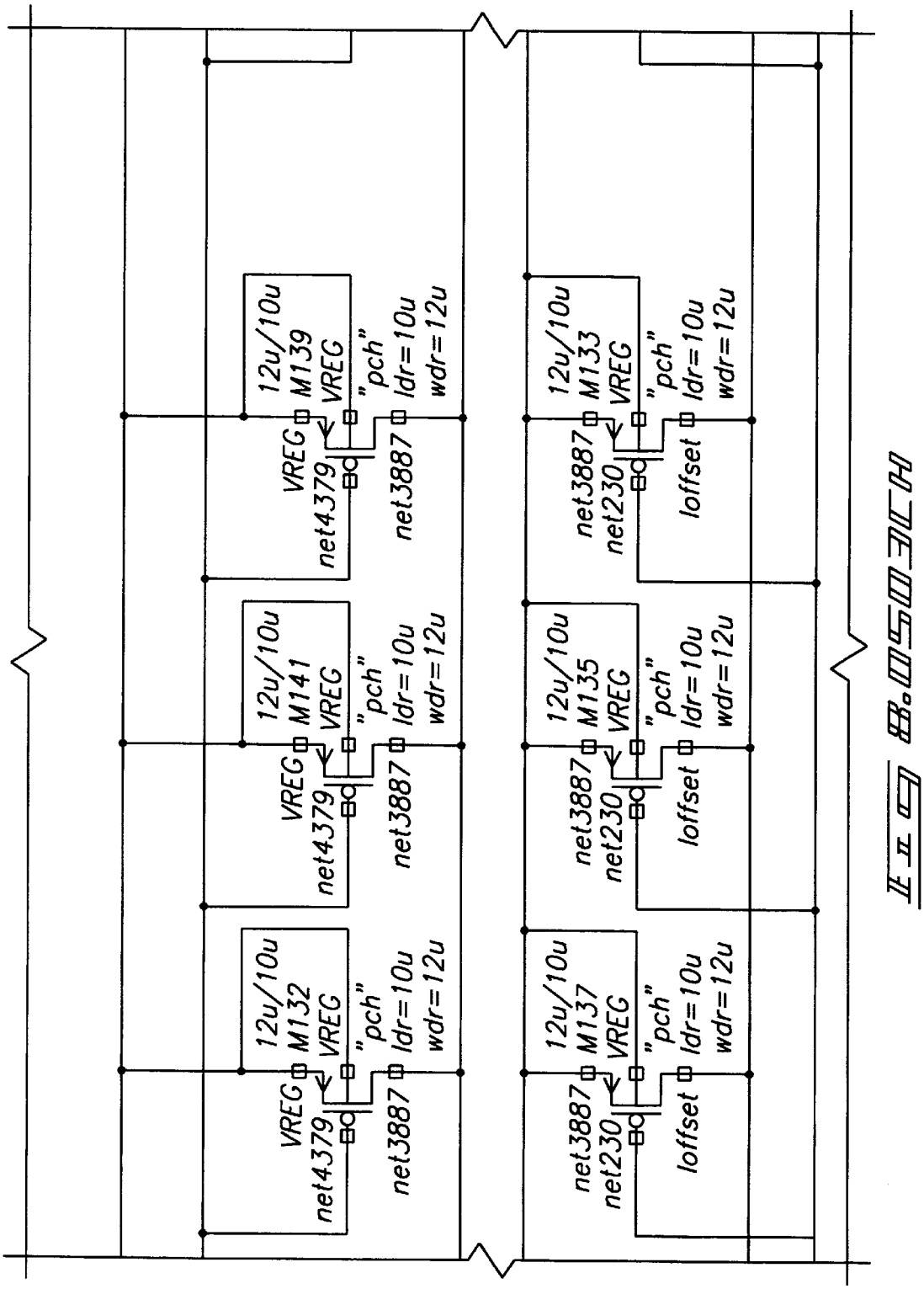

12u/10u
M139
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net3887
12u/10u
M141
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net3887
12u/10u
M132
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net3887
12u/10u
M133
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
loffset
12u/10u
M135
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
loffset
12u/10u
M137
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
loffset

FIG. 8.0050

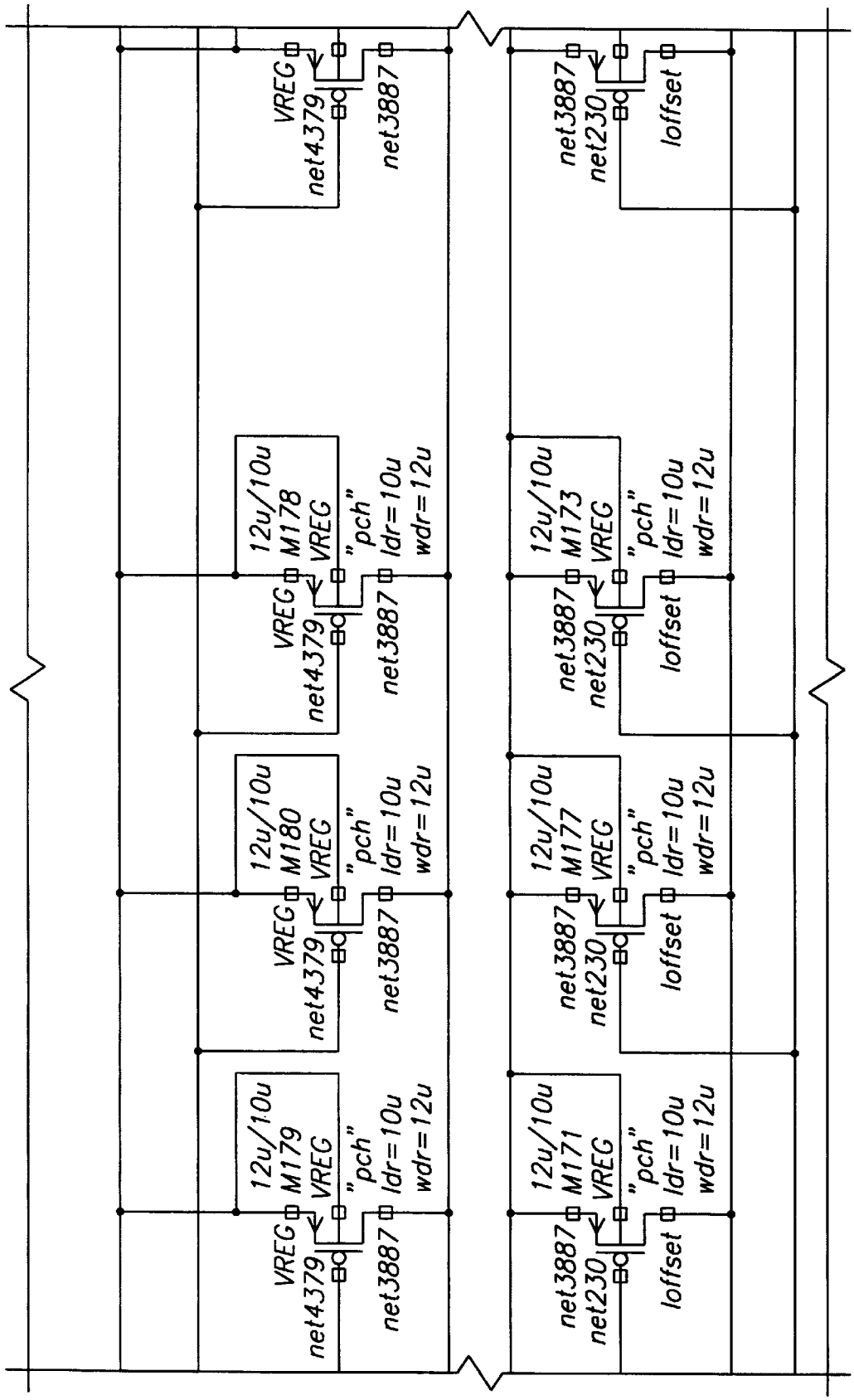

12u/10u
M179
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net3887
12u/10u
M180
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net3887
12u/10u
M178
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net3887
12u/10u
M171
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
loffset
12u/10u
M177
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
loffset
12u/10u
M173
VREG
"pch"
ldr=10u
wdr=12u
net3887
net230
loffset

FIG. 88.0511

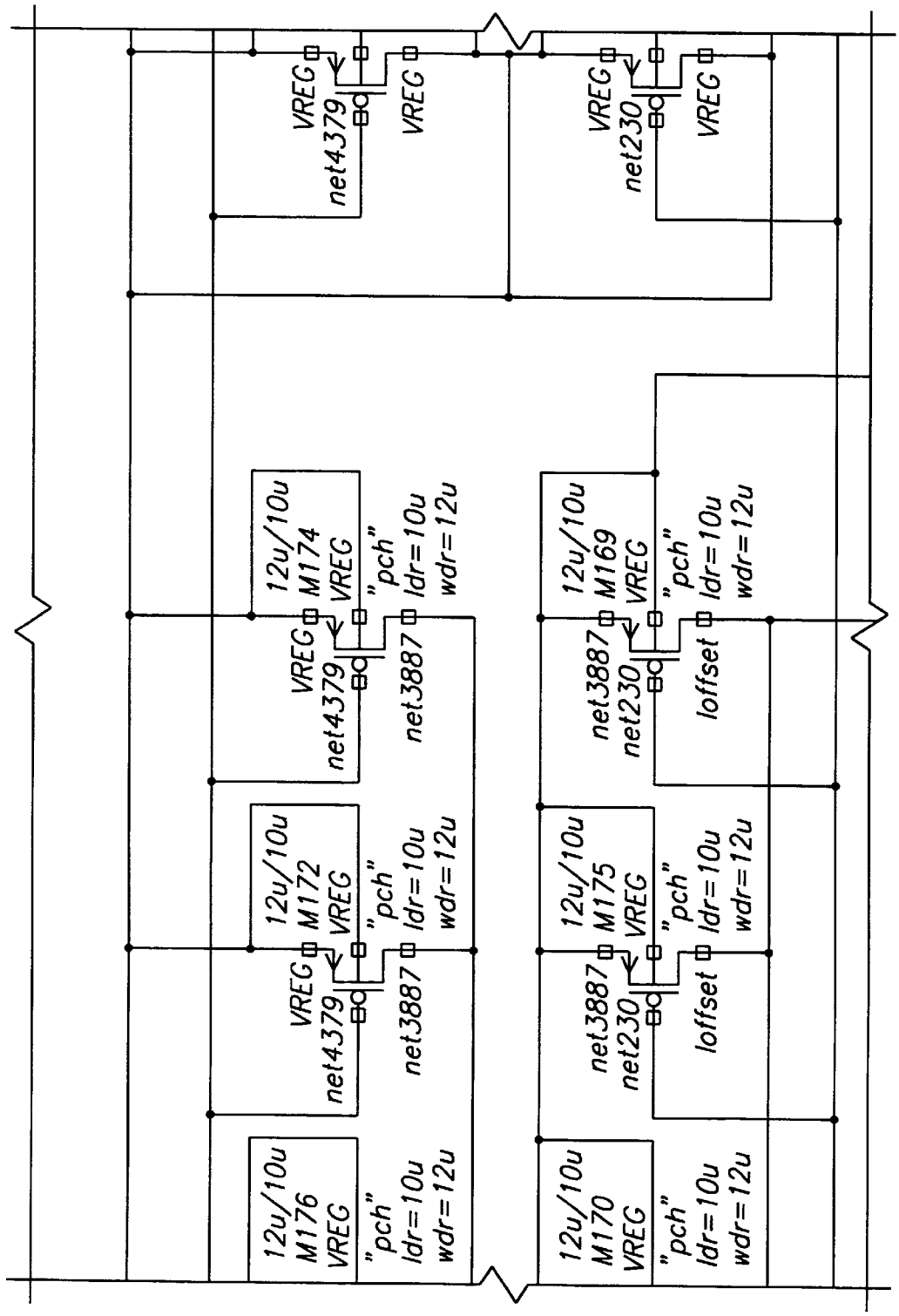

VREG
net4379
VREG
VREG
net230
VREG
12u/10u
M174
VREG
"pch"
ldr=10u
wdr=12u
net3887
12u/10u
M169
VREG
"pch"
ldr=10u
wdr=12u
loffset
12u/10u
M172
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
M175
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
M176
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
M170
VREG
"pch"
ldr=10u
wdr=12u

FIG. 1536

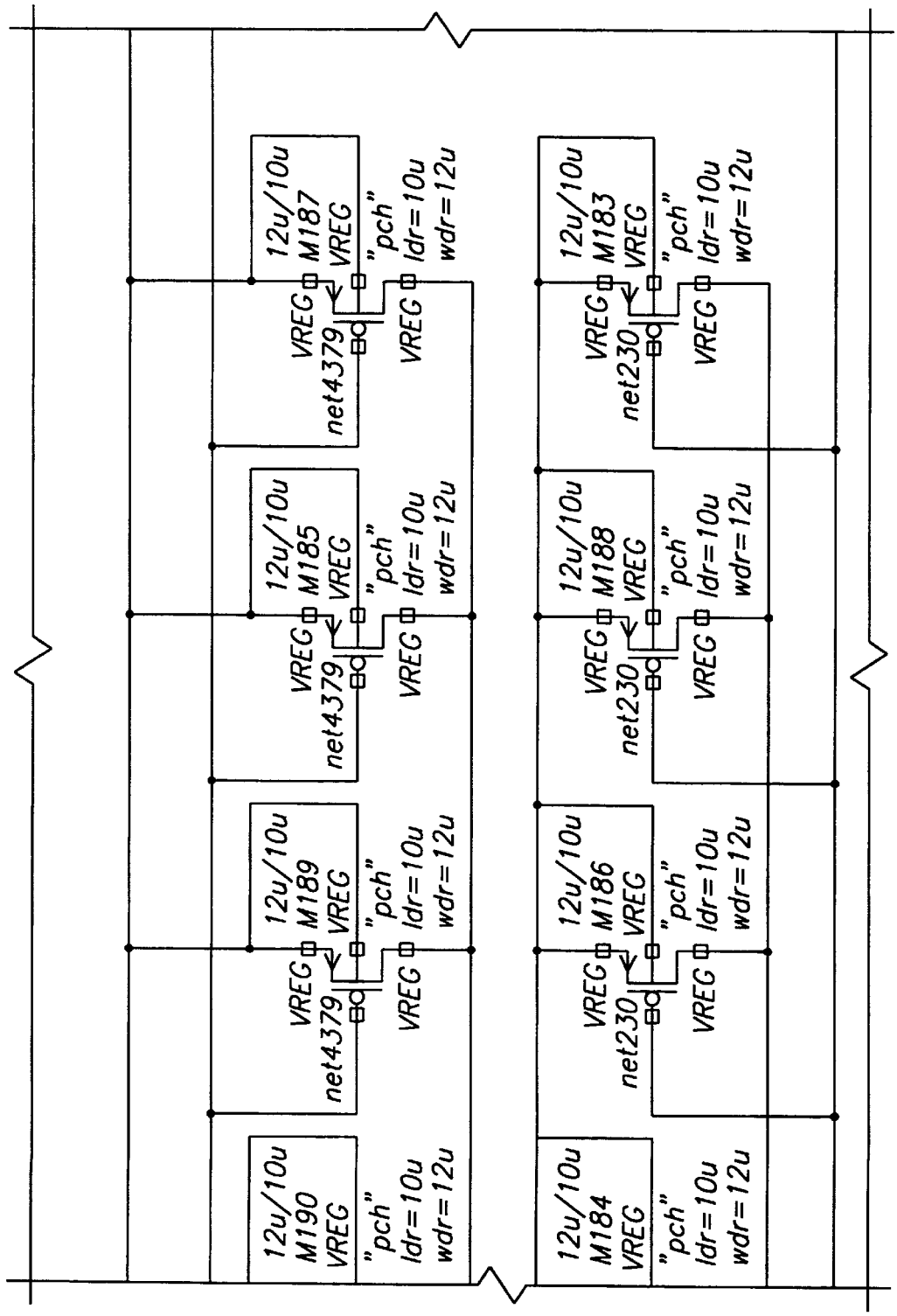

12u/10u
M190
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
M189
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
12u/10u
M185
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
12u/10u
M187
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
12u/10u
M184
VREG
"pch"
ldr=10u
wdr=12u
12u/10u
M186
VREG
"pch"
ldr=10u
wdr=12u
VREG
net230
12u/10u
M188
VREG
"pch"
ldr=10u
wdr=12u
VREG
net230
12u/10u
M183
VREG
"pch"
ldr=10u
wdr=12u
VREG
net230

FIG. 88.0537E

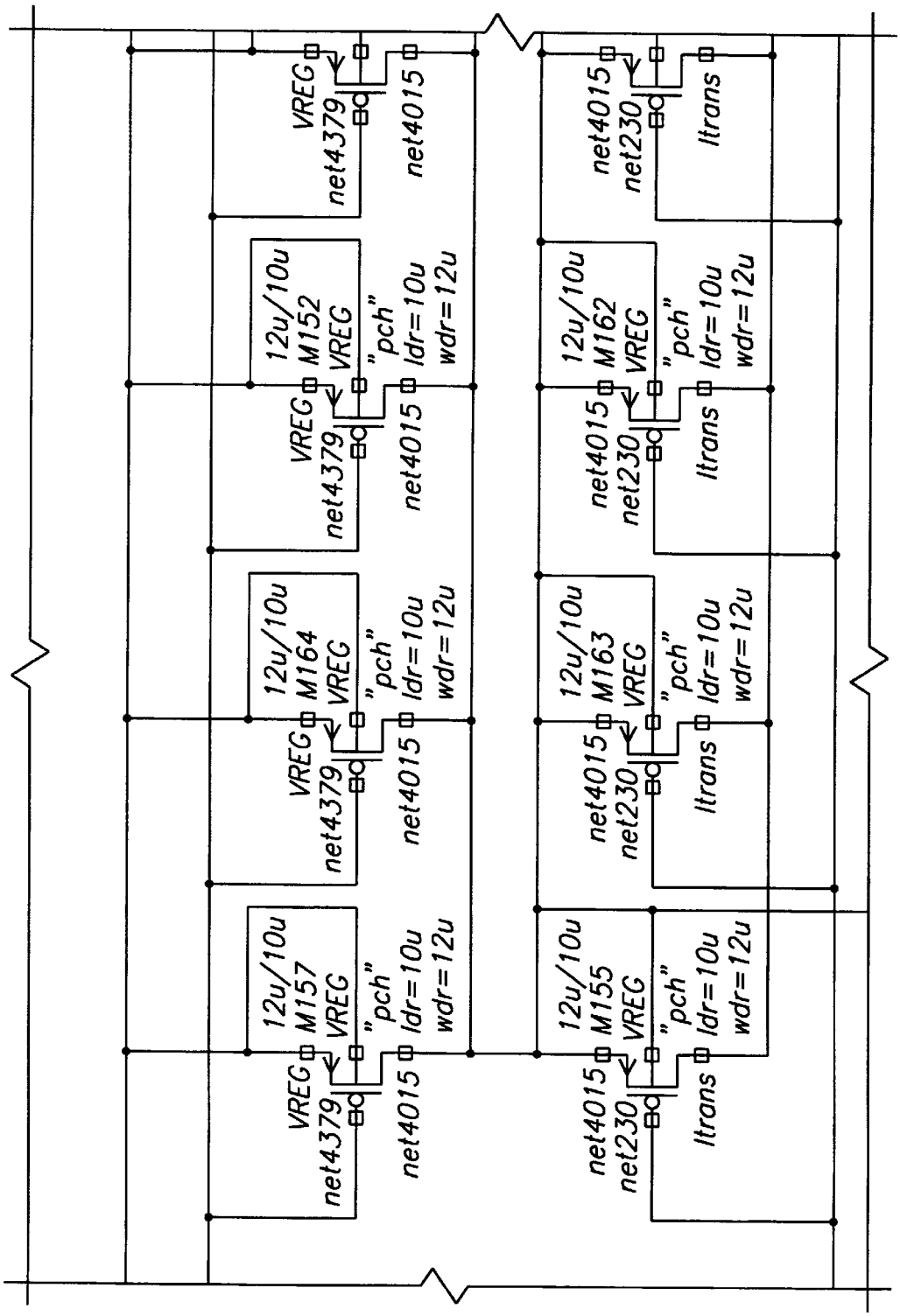

12u/10u
M157
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4015
12u/10u
M164
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4015
12u/10u
M152
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4015
12u/10u
M155
VREG
"pch"
ldr=10u
wdr=12u
net4015
net230
Itrans
12u/10u
M163
VREG
"pch"
ldr=10u
wdr=12u
net4015
net230
Itrans
12u/10u
M162
VREG
"pch"
ldr=10u
wdr=12u
net4015
net230
Itrans
net4015
net230
Itrans

FIG. 8,005

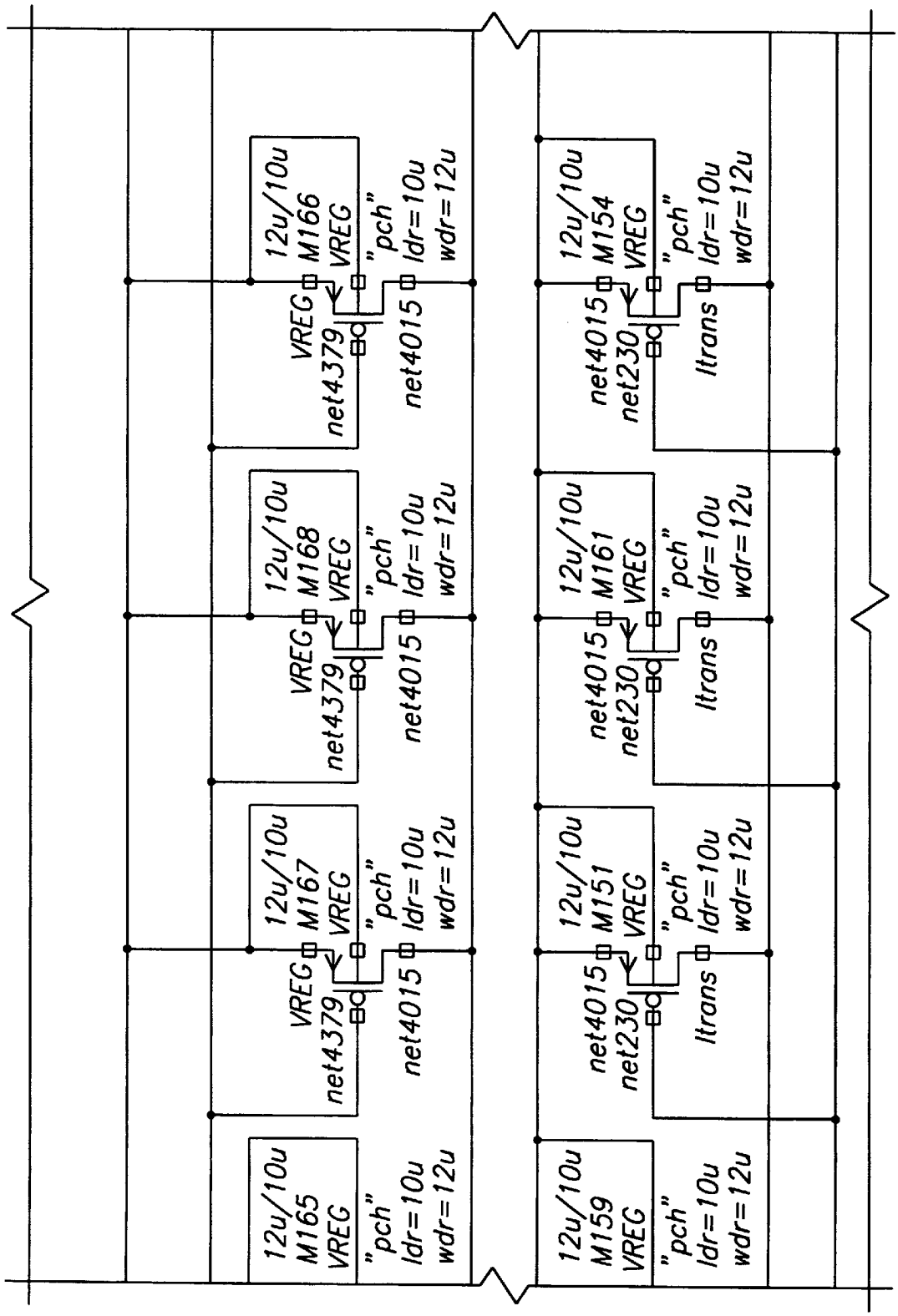

12u/10u
M165
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
12u/10u
M167
VREG
"pch"
ldr=10u
wdr=12u
net4015
12u/10u
M168
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
12u/10u
M166
VREG
"pch"
ldr=10u
wdr=12u
net4015
12u/10u
M159
VREG
"pch"
ldr=10u
wdr=12u
net4015
net230
12u/10u
M151
VREG
"pch"
ldr=10u
wdr=12u
ltrans
net4015
net230
12u/10u
M161
VREG
"pch"
ldr=10u
wdr=12u
ltrans
net4015
net230
12u/10u
M154
VREG
"pch"
ldr=10u
wdr=12u
ltrans

FIG 8,050,008

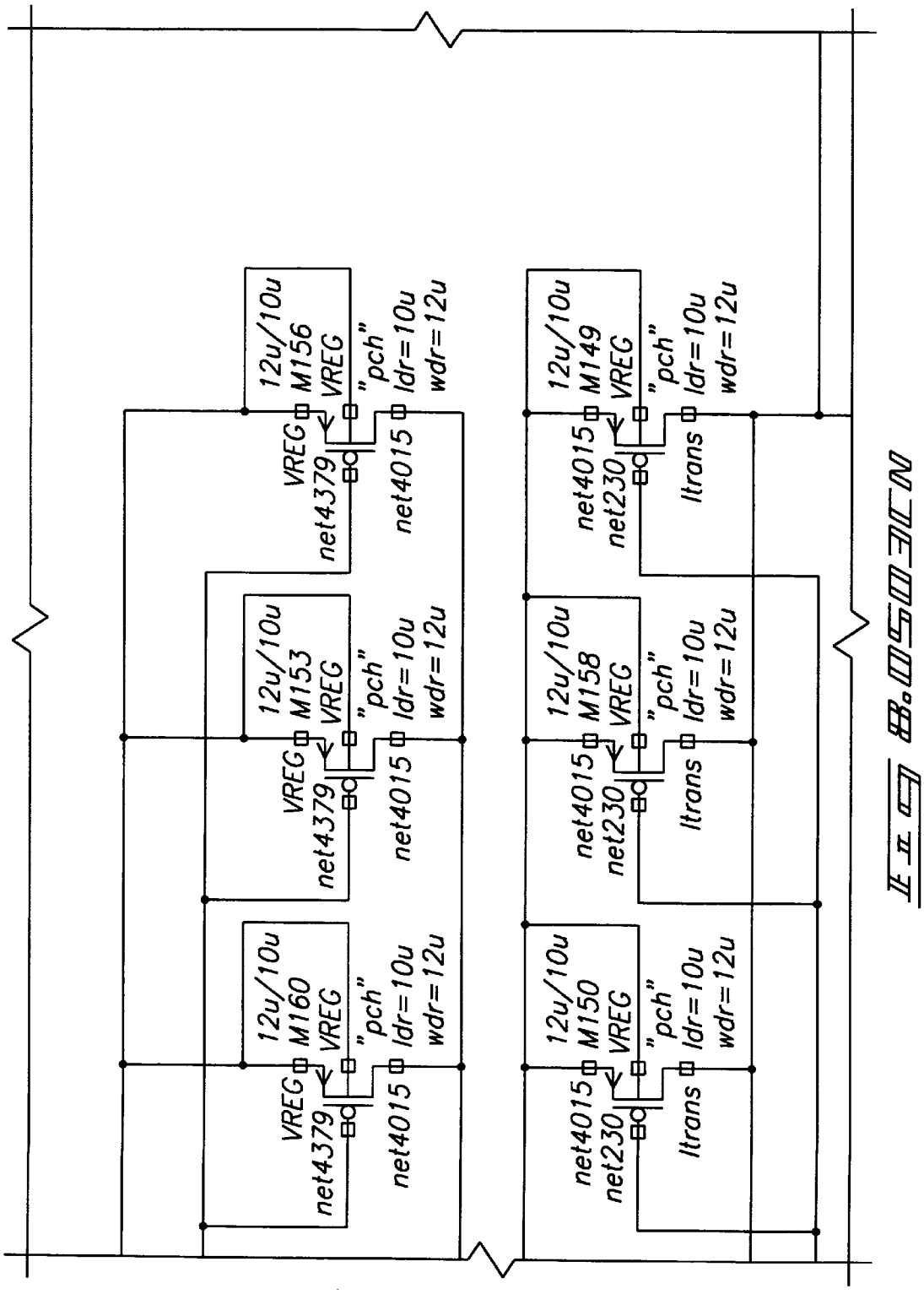
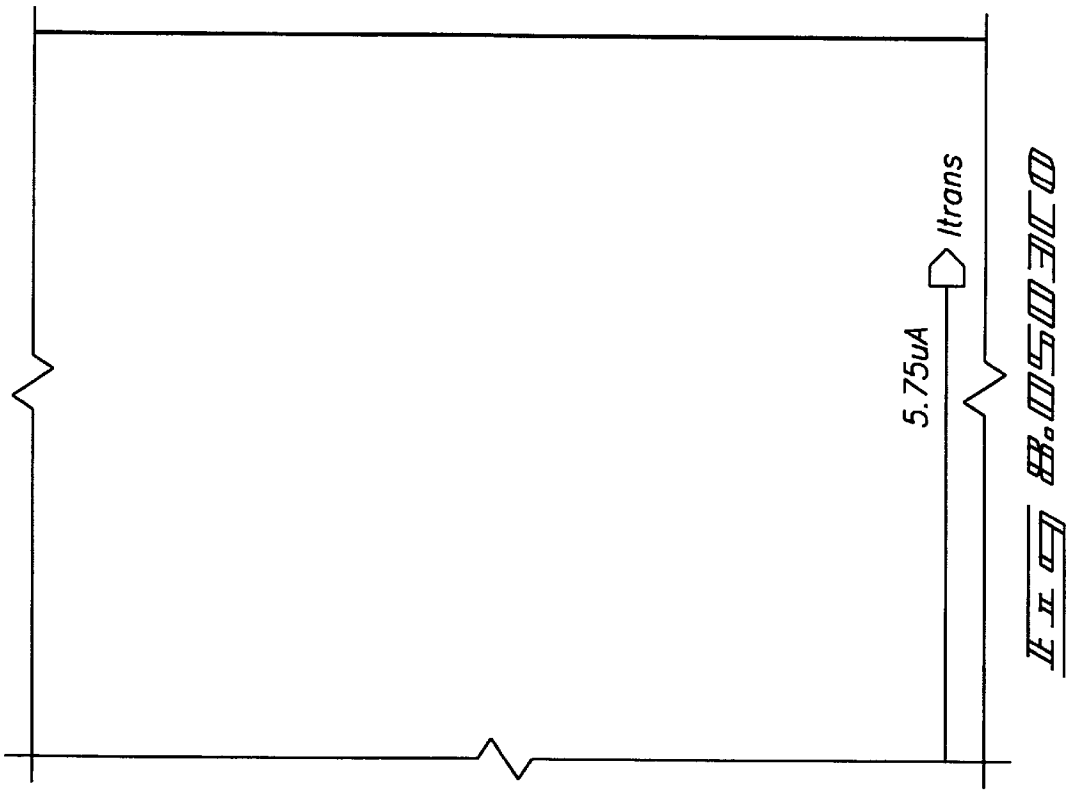
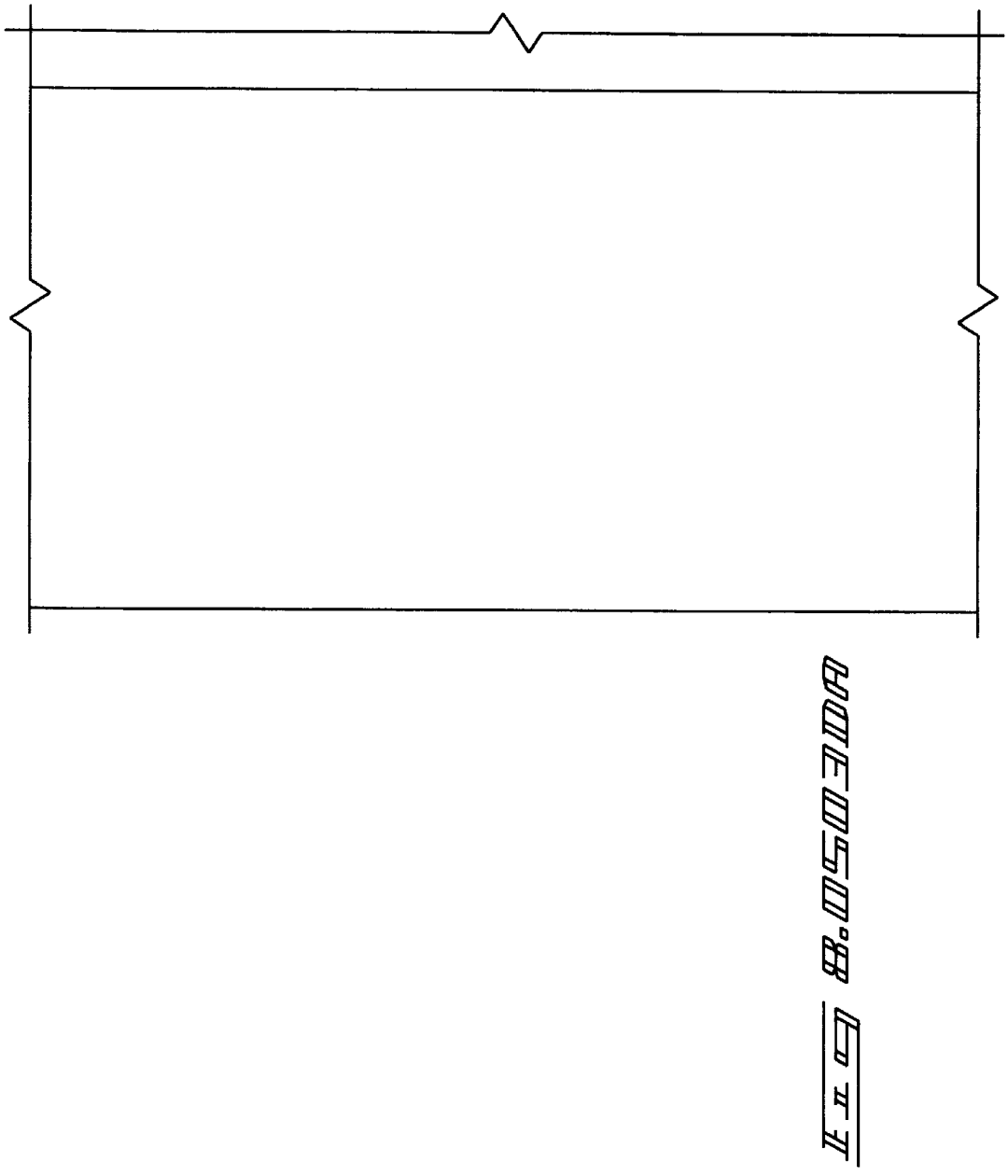

12u/10u
M156
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4015
12u/10u
M153
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4015
12u/10u
M160
VREG
"pch"
ldr=10u
wdr=12u
VREG
net4379
net4015
12u/10u
M149
VREG
"pch"
ldr=10u
wdr=12u
net4015
net230
ltrans
12u/10u
M158
VREG
"pch"
ldr=10u
wdr=12u
net4015
net230
ltrans
12u/10u
M150
VREG
"pch"
ldr=10u
wdr=12u
net4015
net230
ltrans

FIG. 88,005


Itrans
5.75uA
FIG 98.00500E



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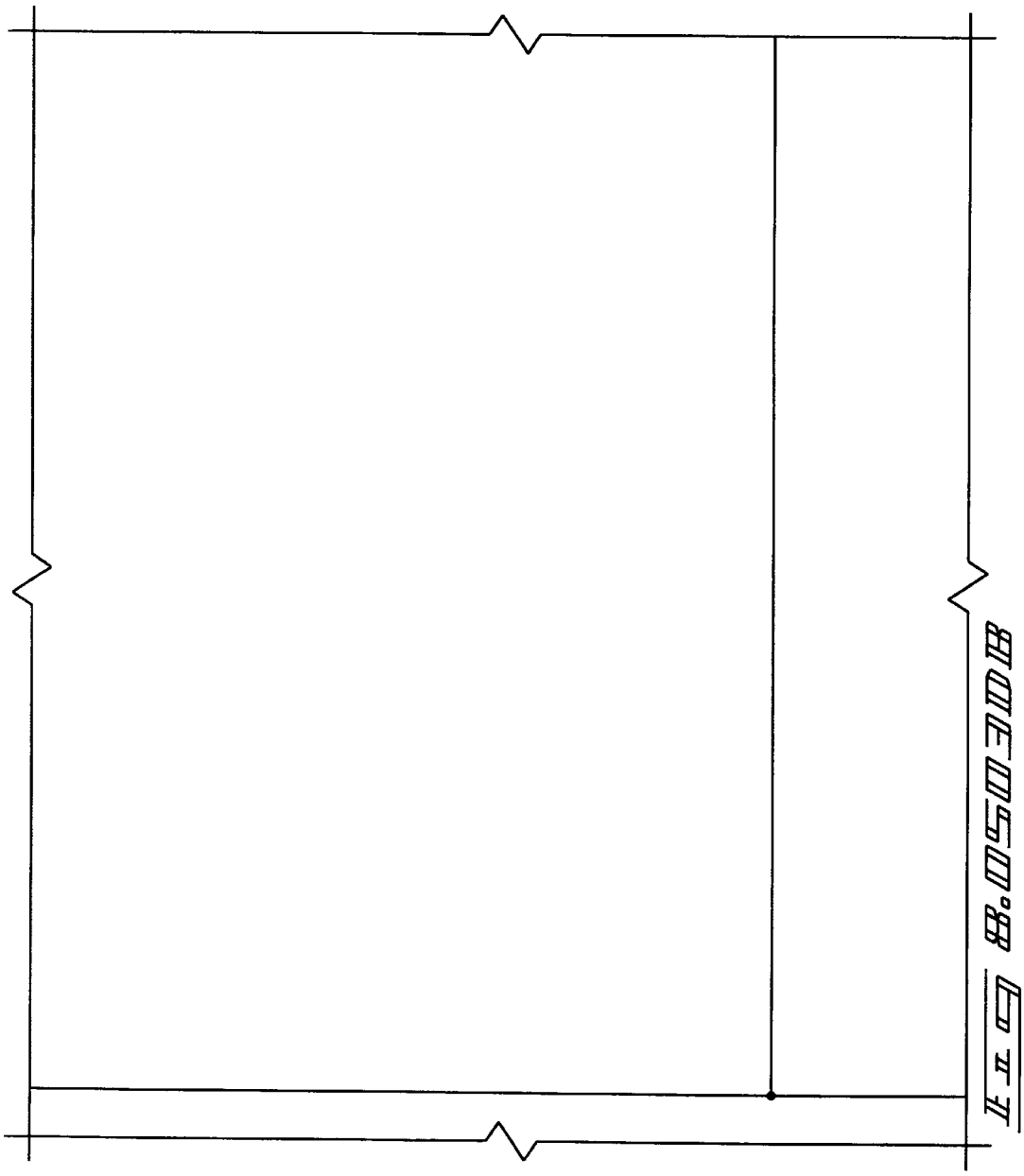


FIG 88.0500E

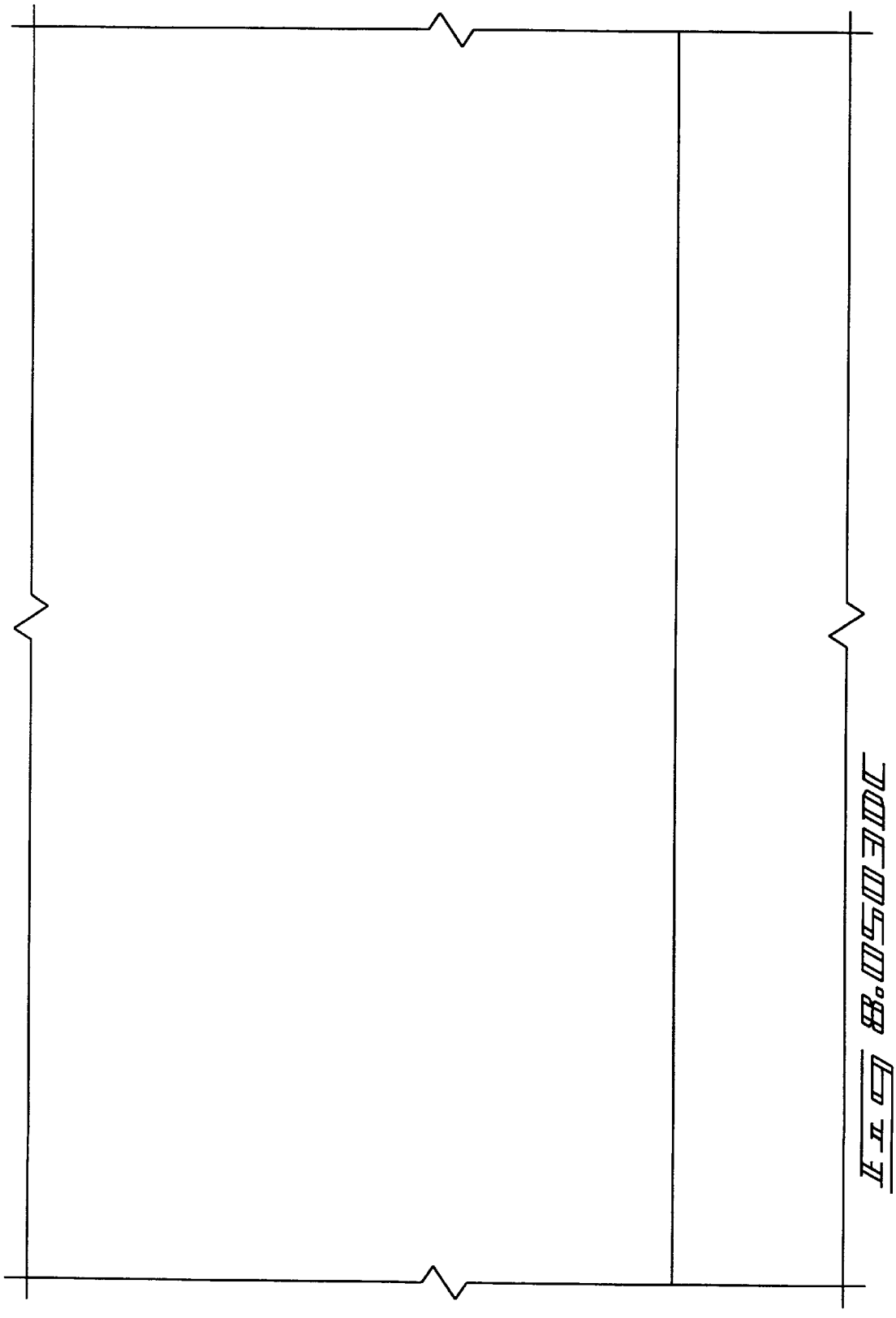


FIG 88,050

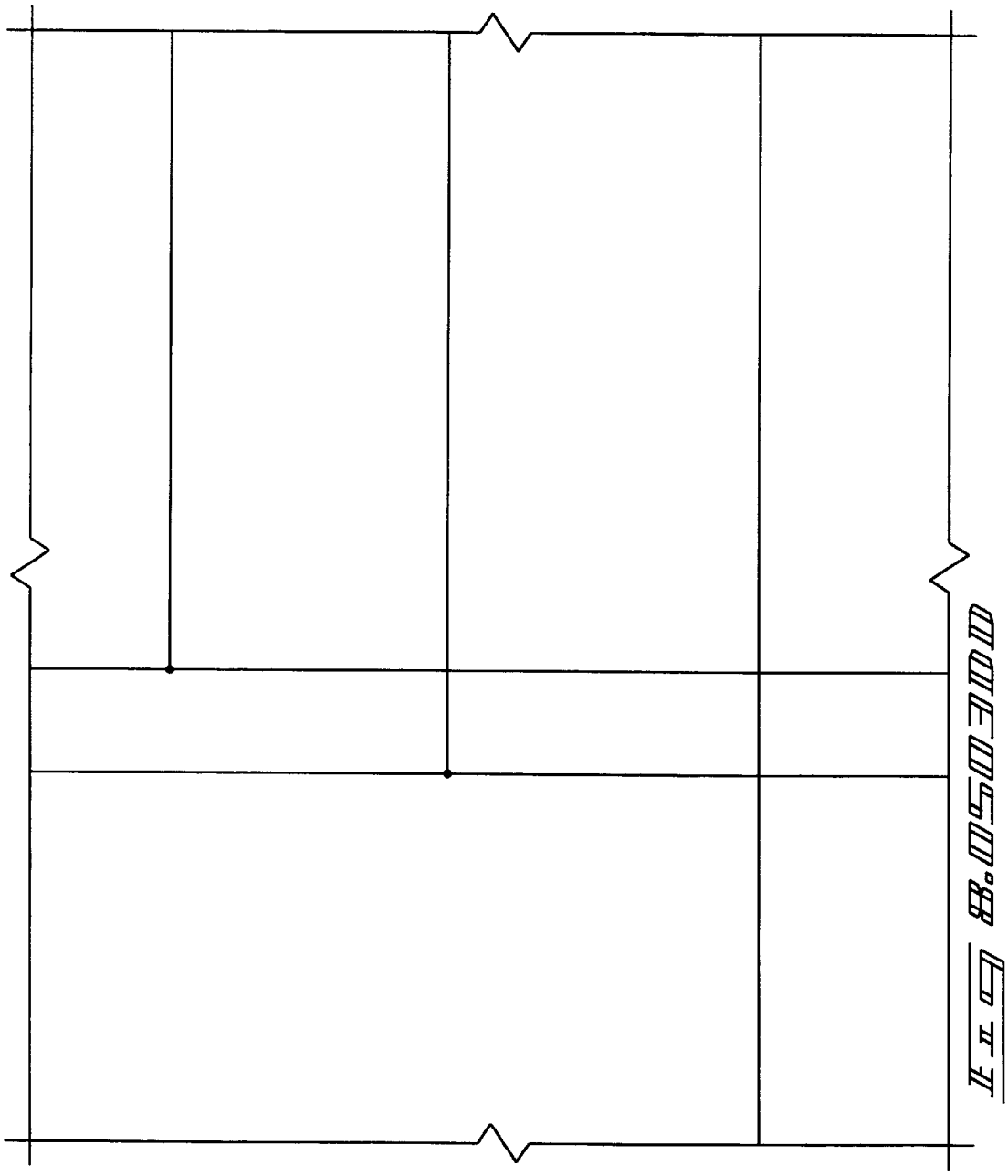
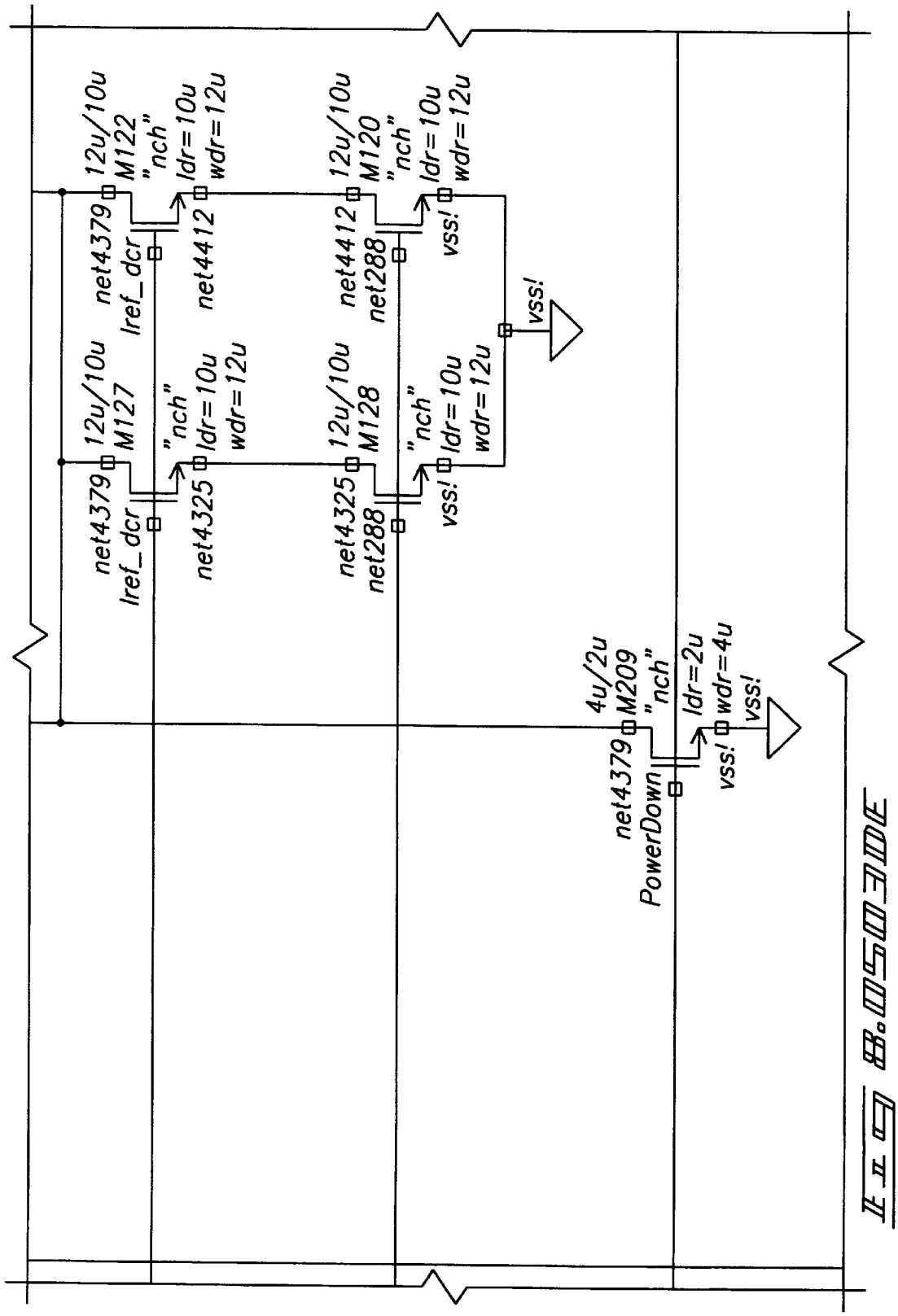


FIG 88


12u/10u
M122
"nch"
ldr=10u
wdr=12u
net4379
lref_dcr
net4412
12u/10u
M120
"nch"
ldr=10u
wdr=12u
net4412
net288
vss!
vss!
12u/10u
M127
"nch"
ldr=10u
wdr=12u
net4379
lref_dcr
net4325
12u/10u
M128
"nch"
ldr=10u
wdr=12u
net4325
net288
vss!
4u/2u
M209
"nch"
ldr=2u
wdr=4u
net4379
PowerDown
vss!
vss!
FIG 88.0SOME

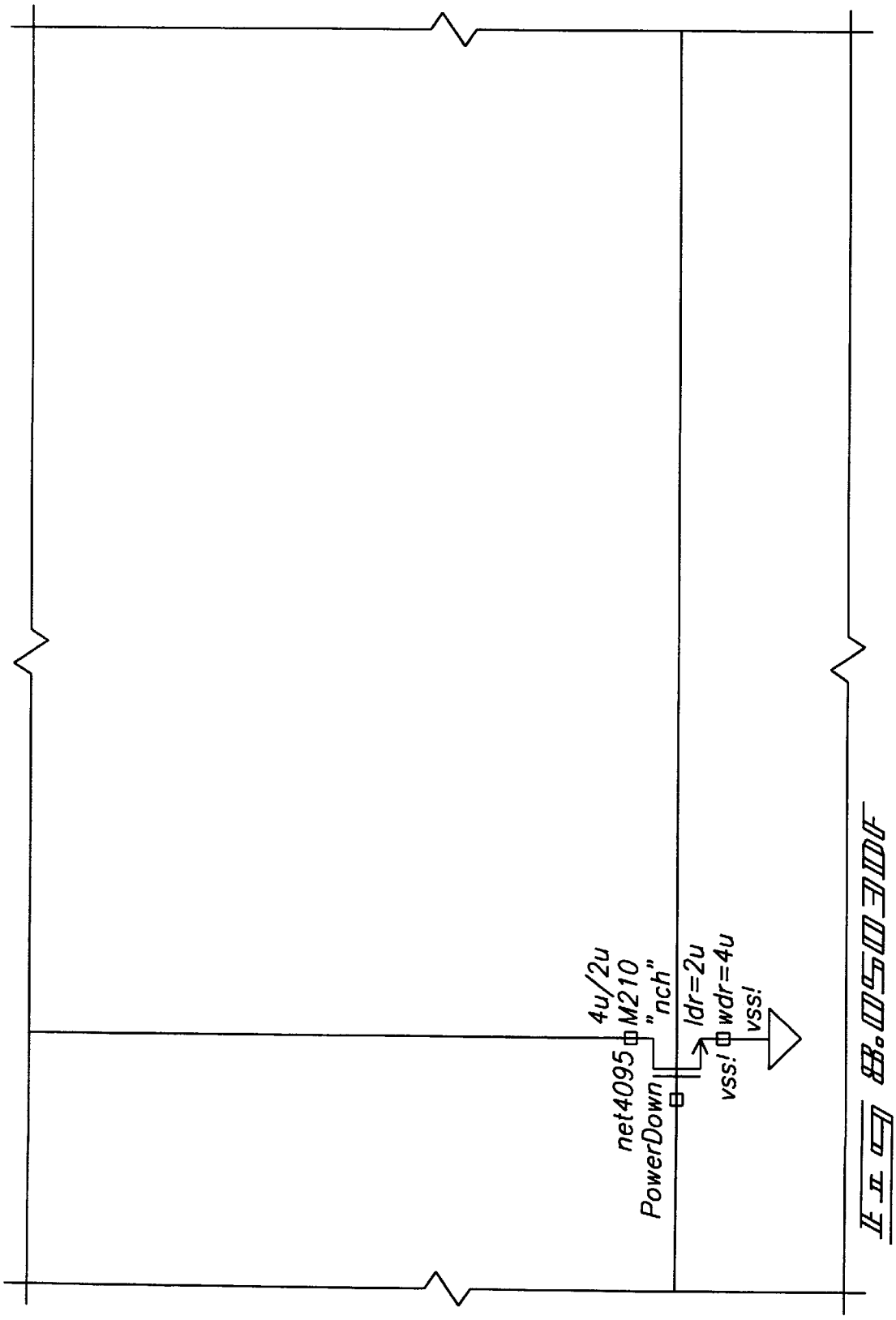


FIG. 8050

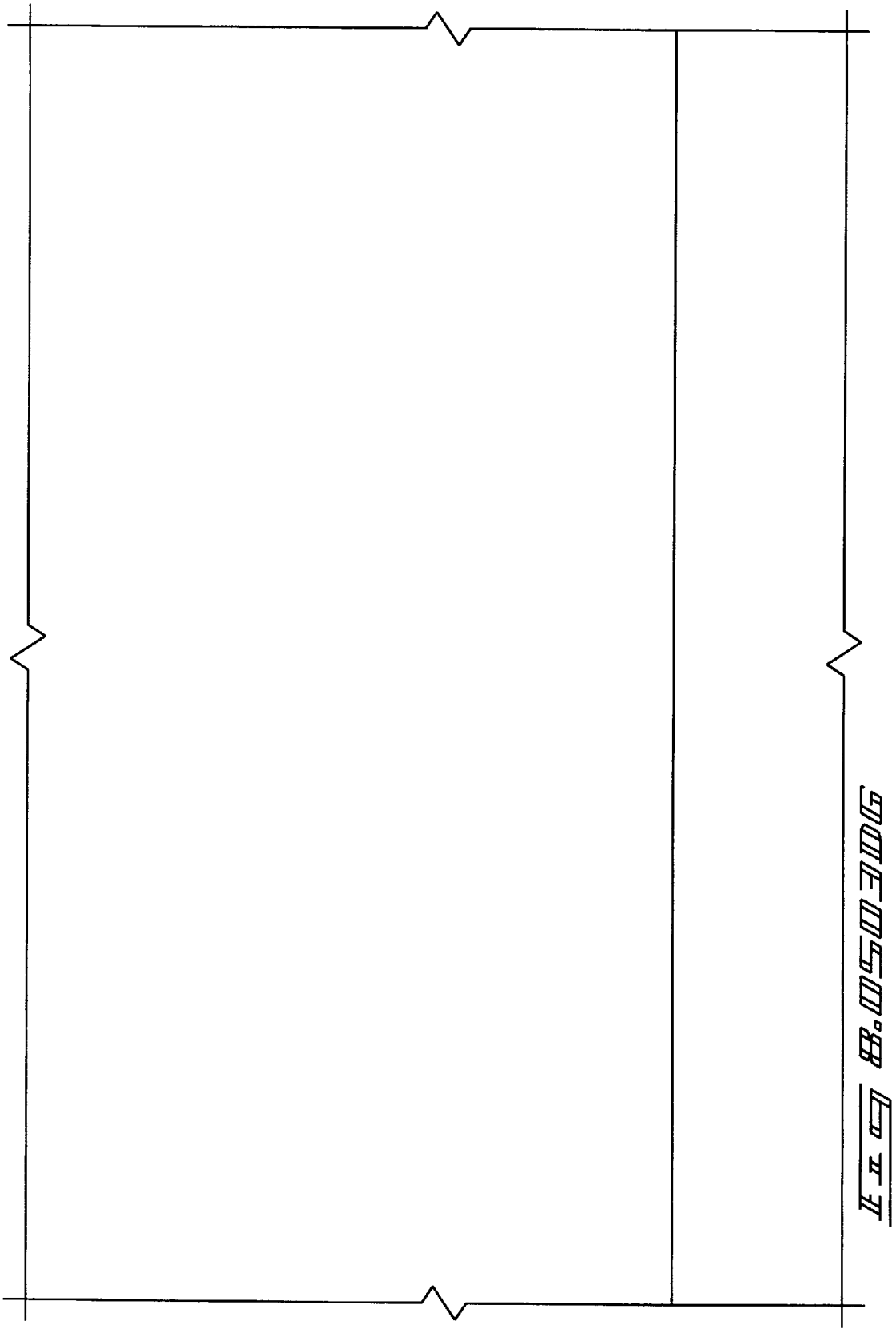
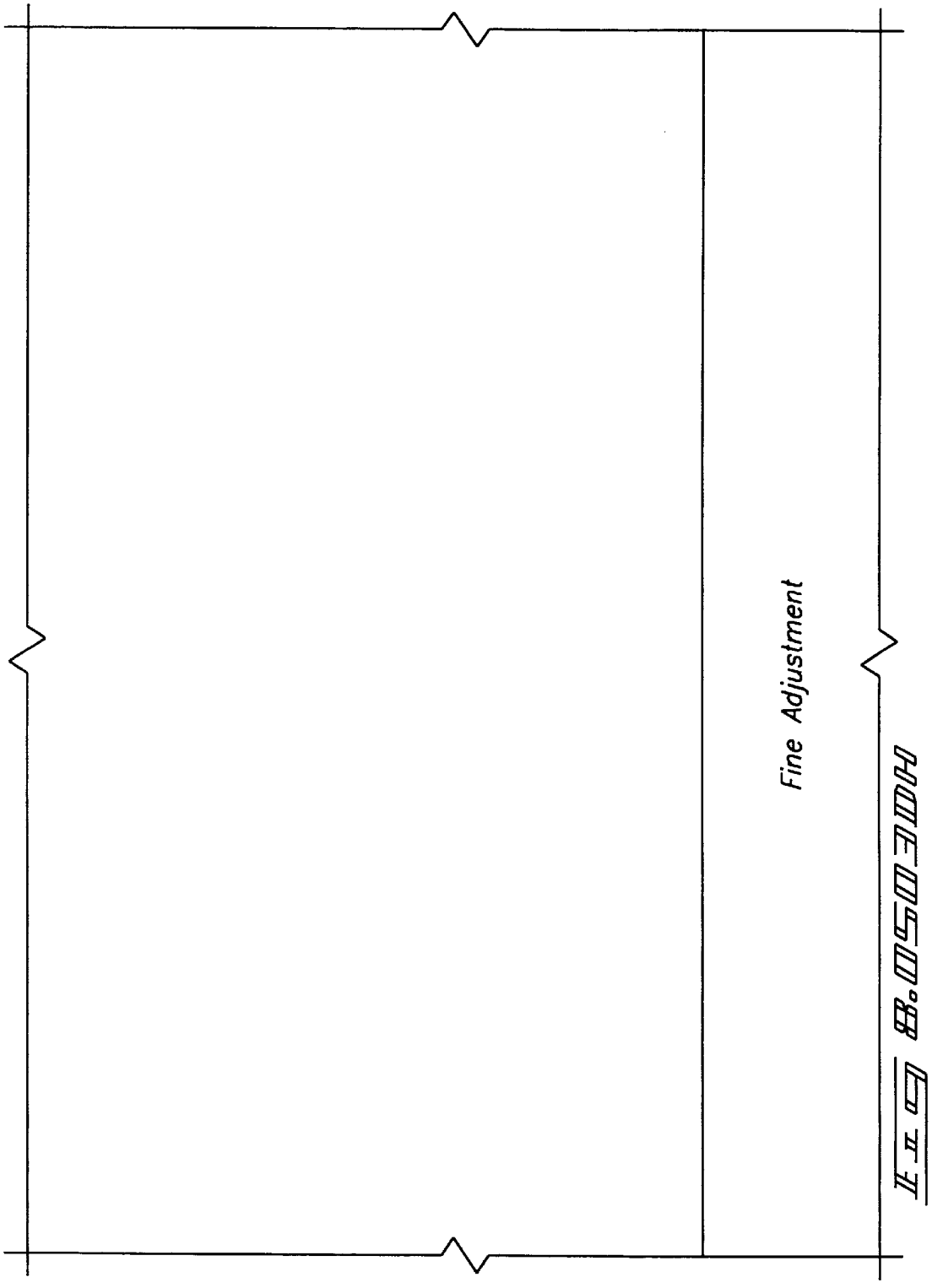


FIG 88.05.05.05


Fine Adjustment
FIG 68.0500
HOME

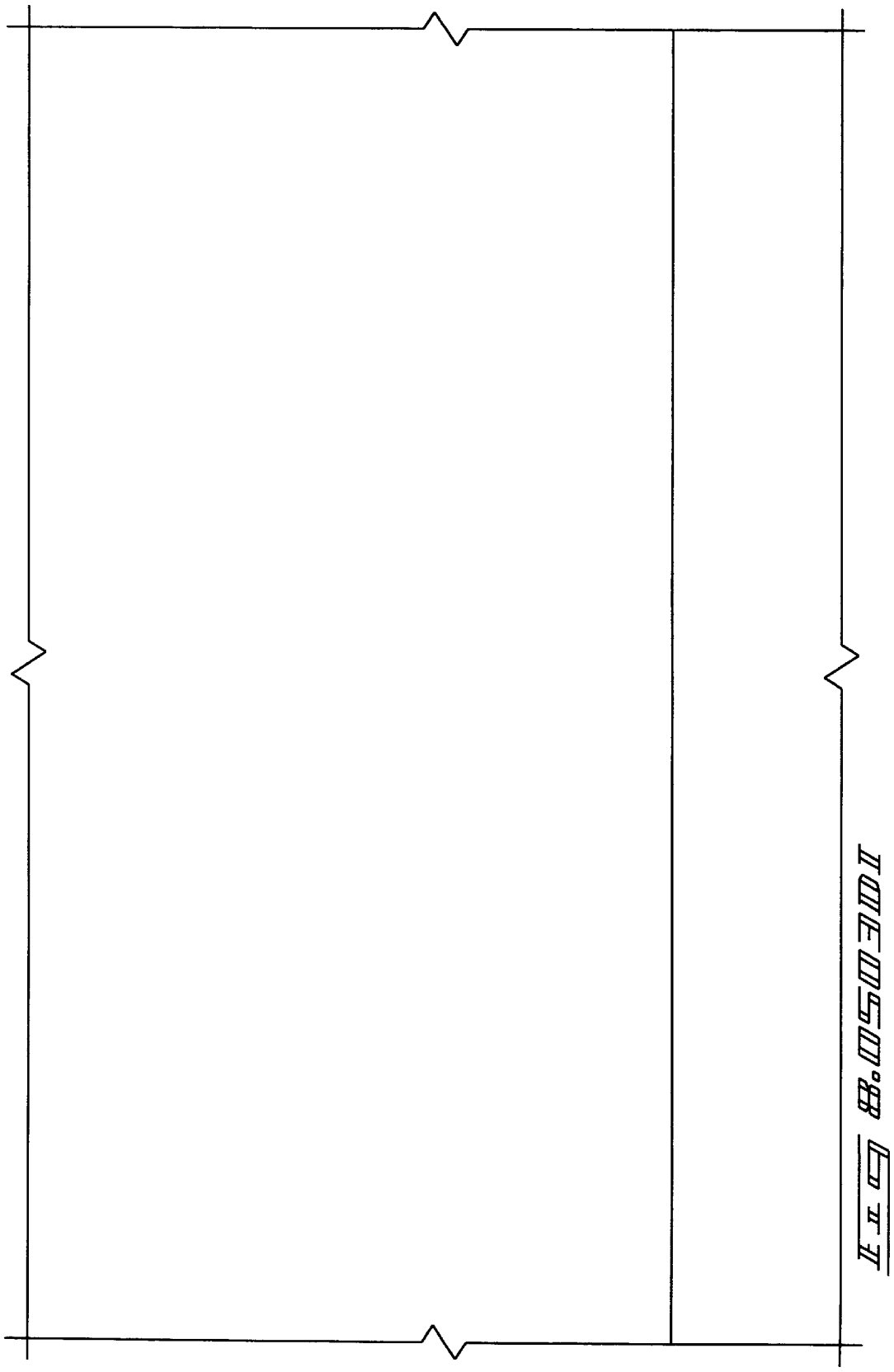


FIG 68,050

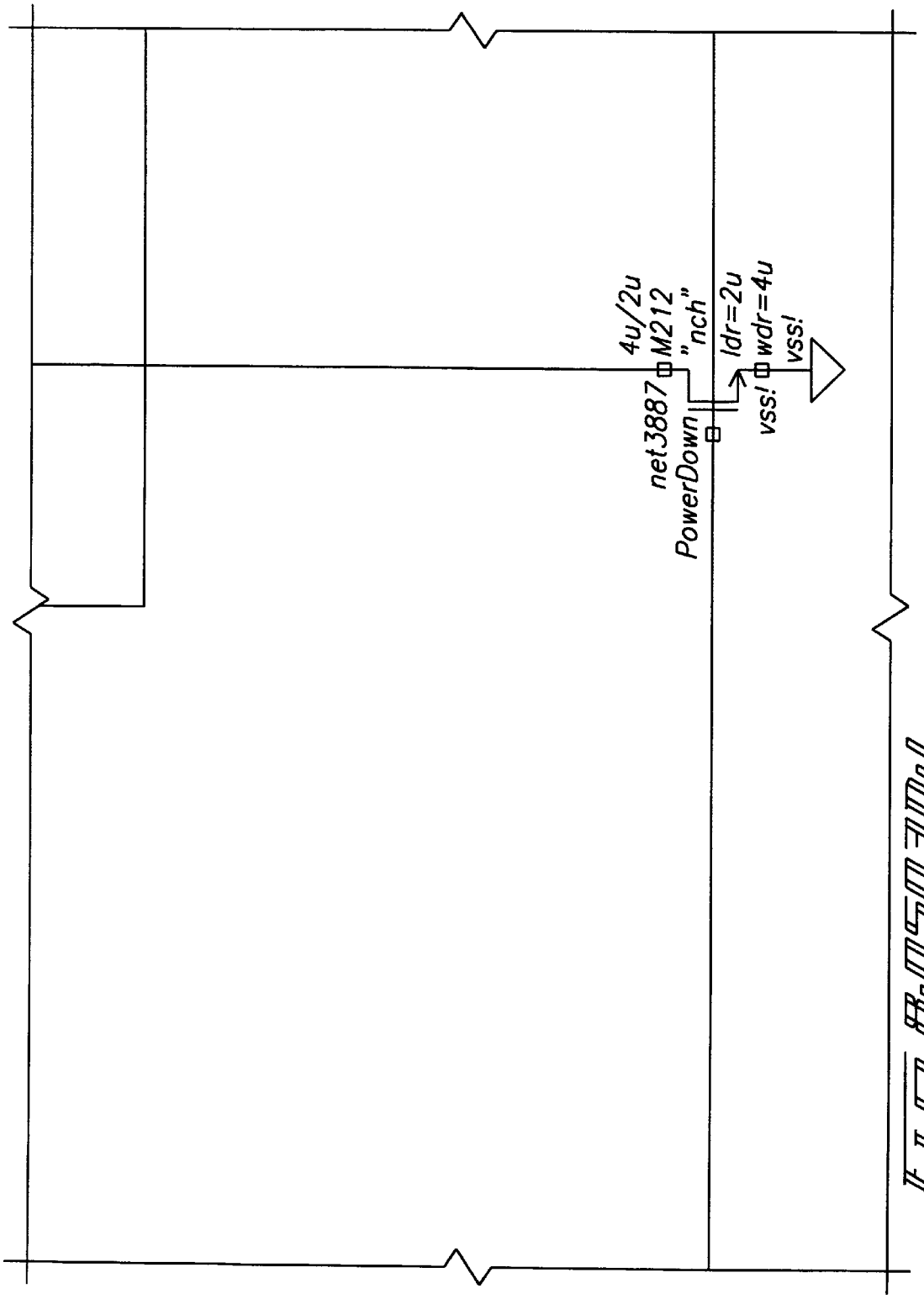
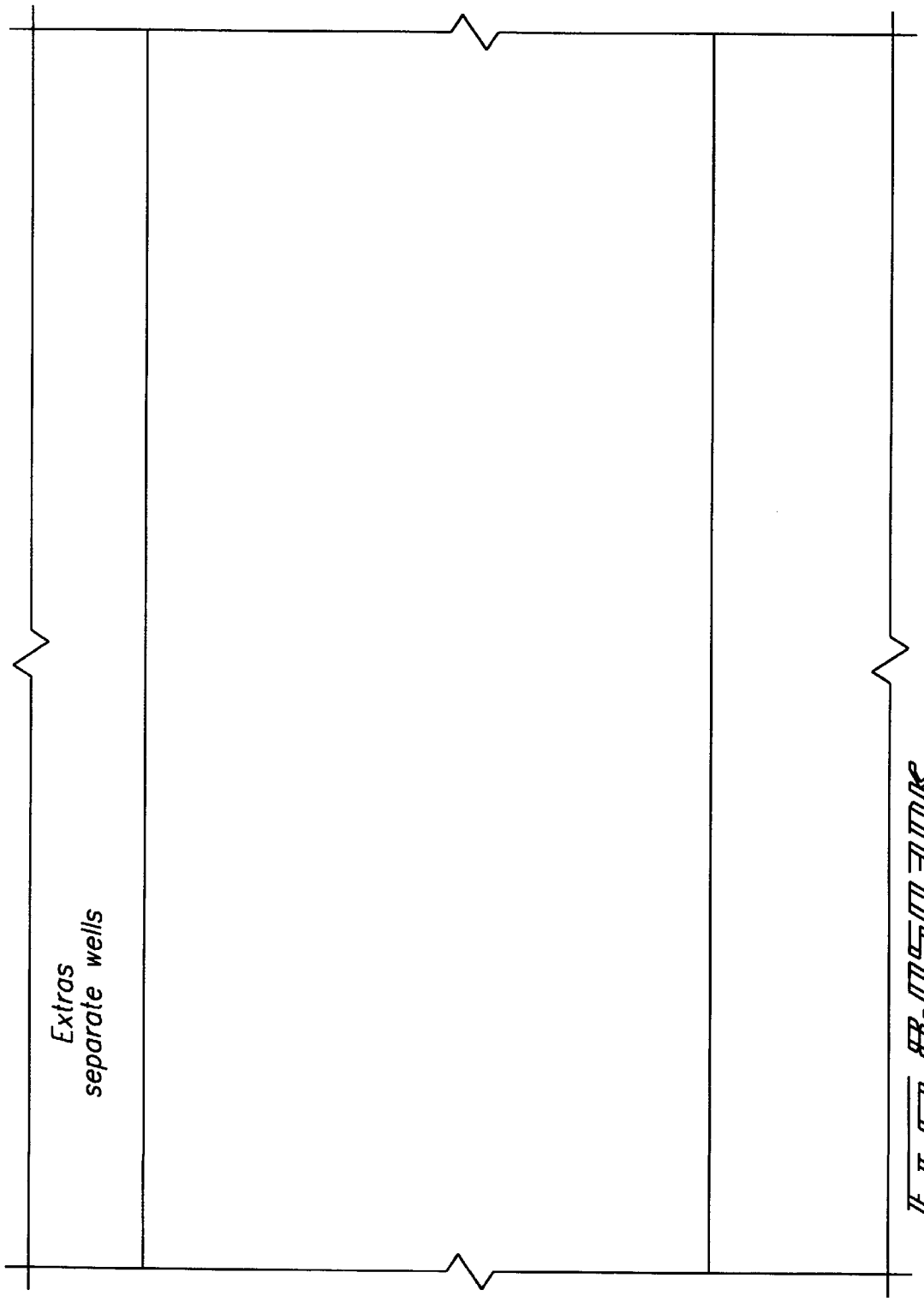


FIG 68,805


Extras
separate wells
FIG 88.0508

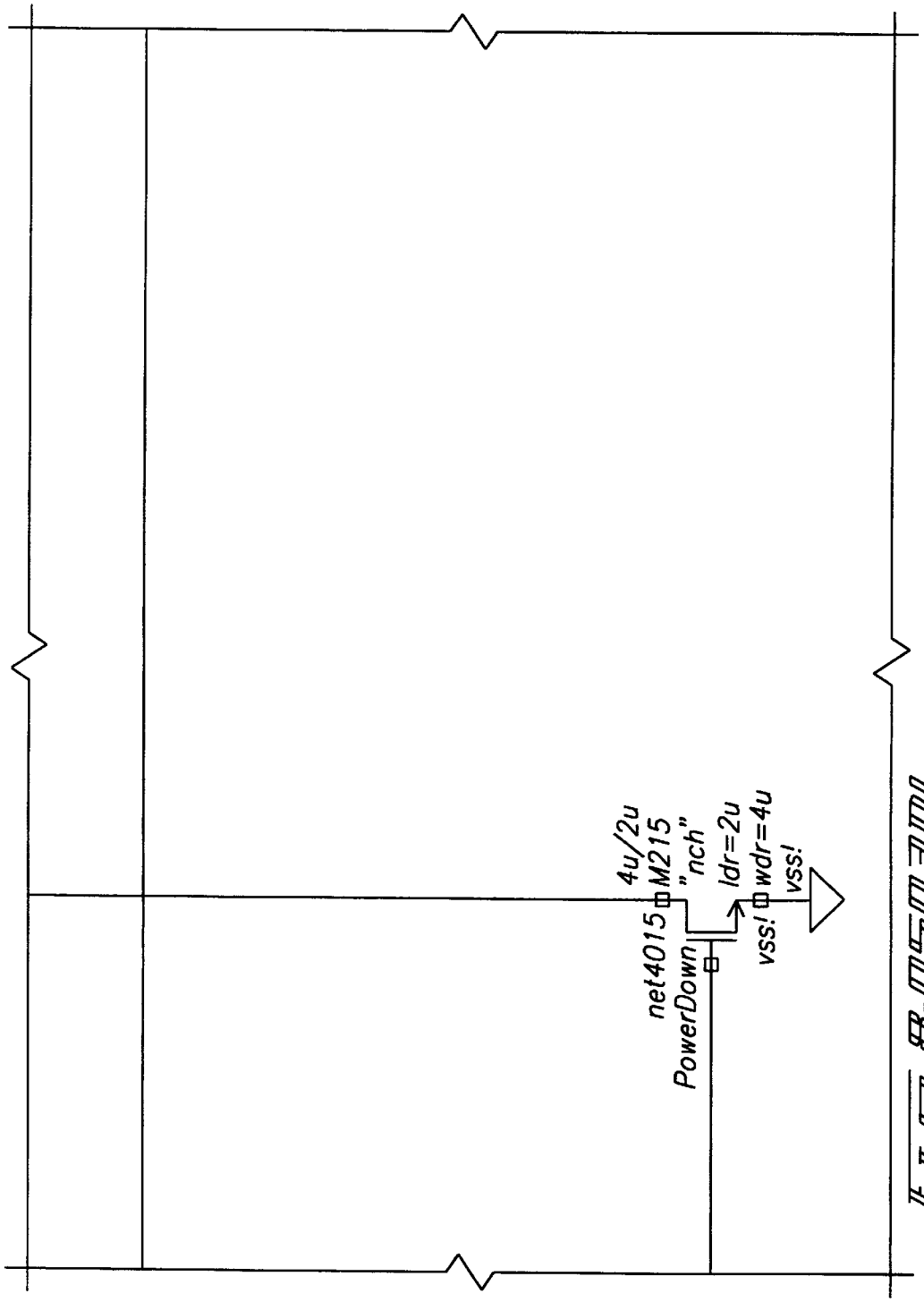


FIG 8.0503E

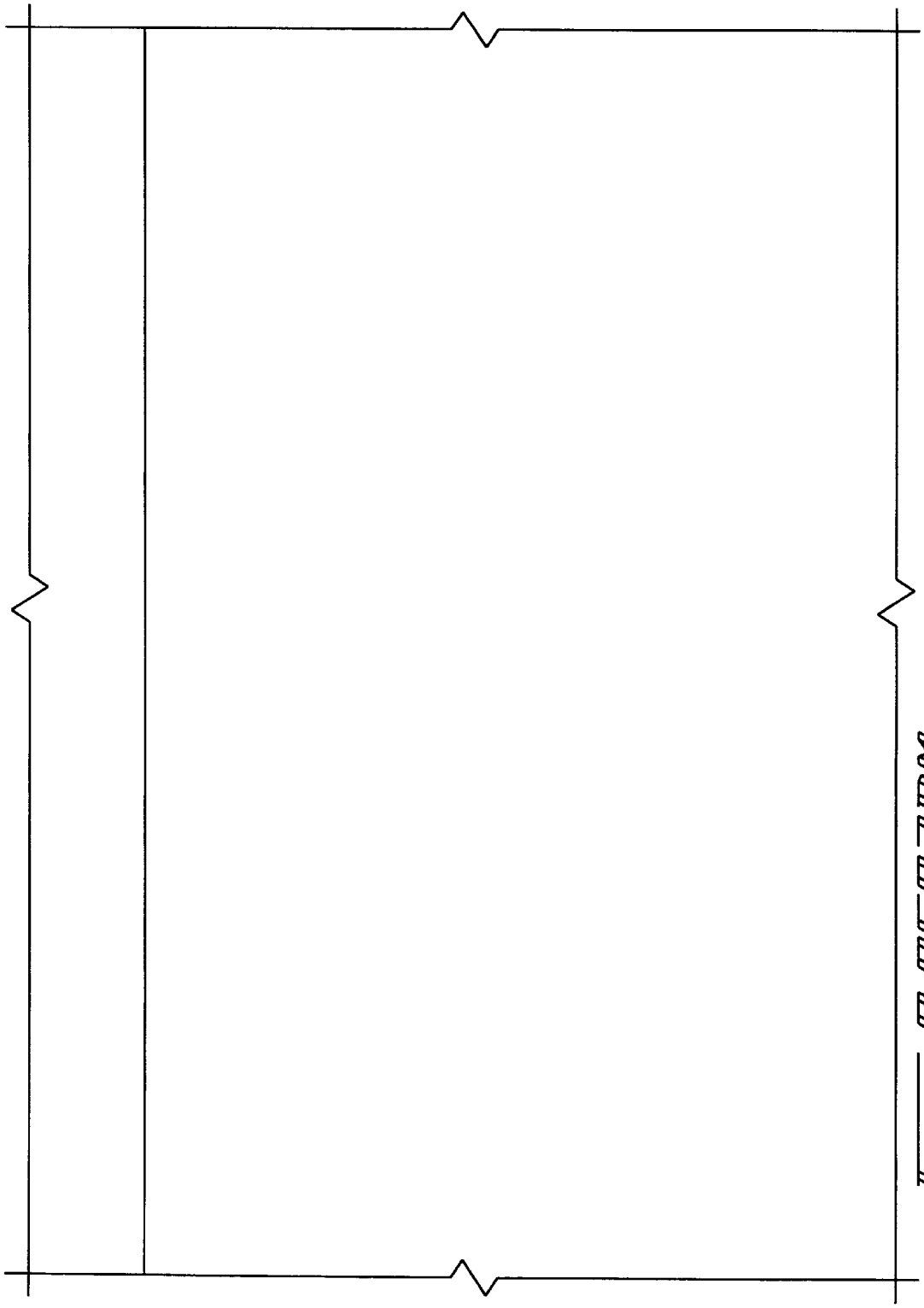
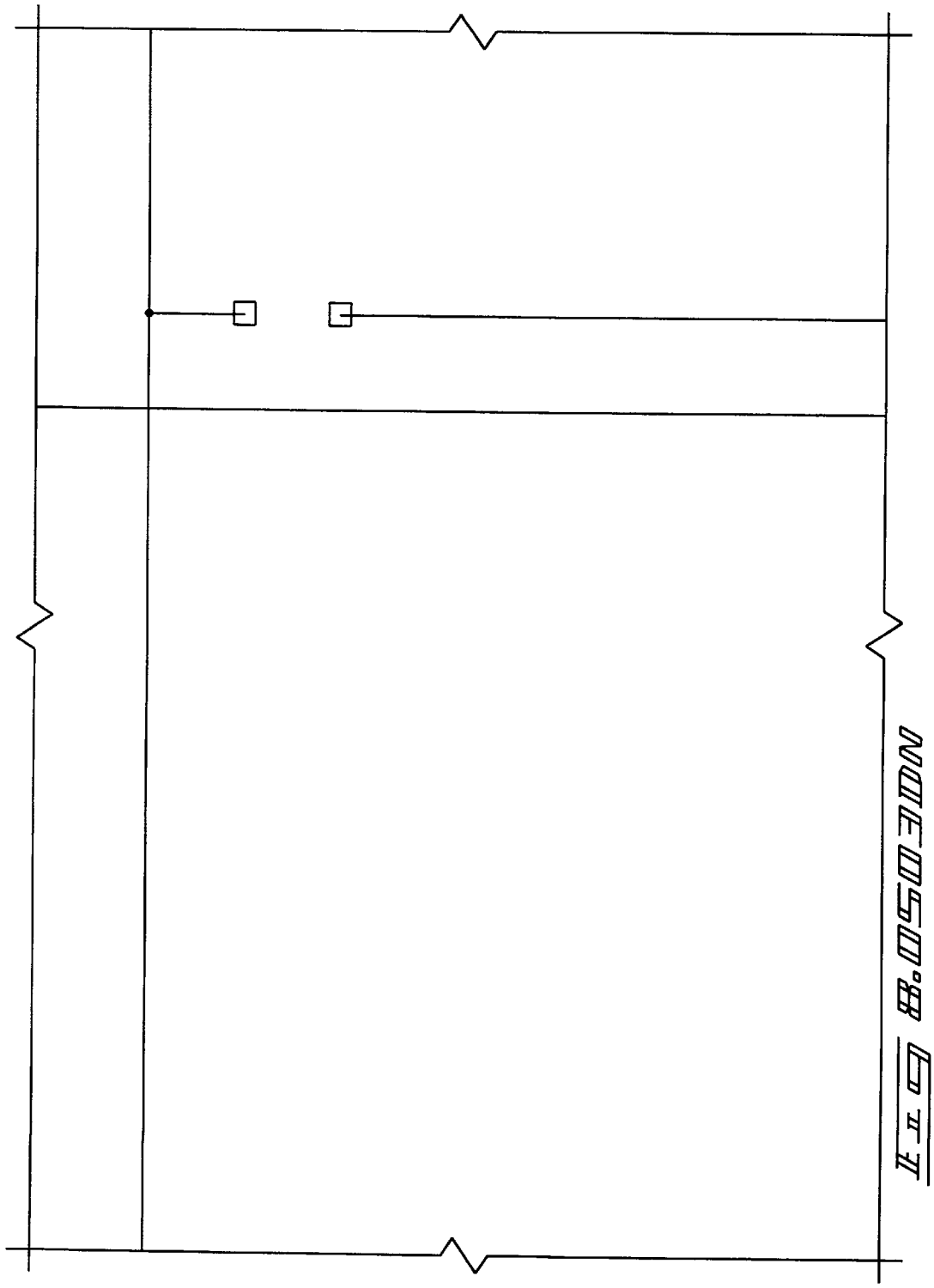
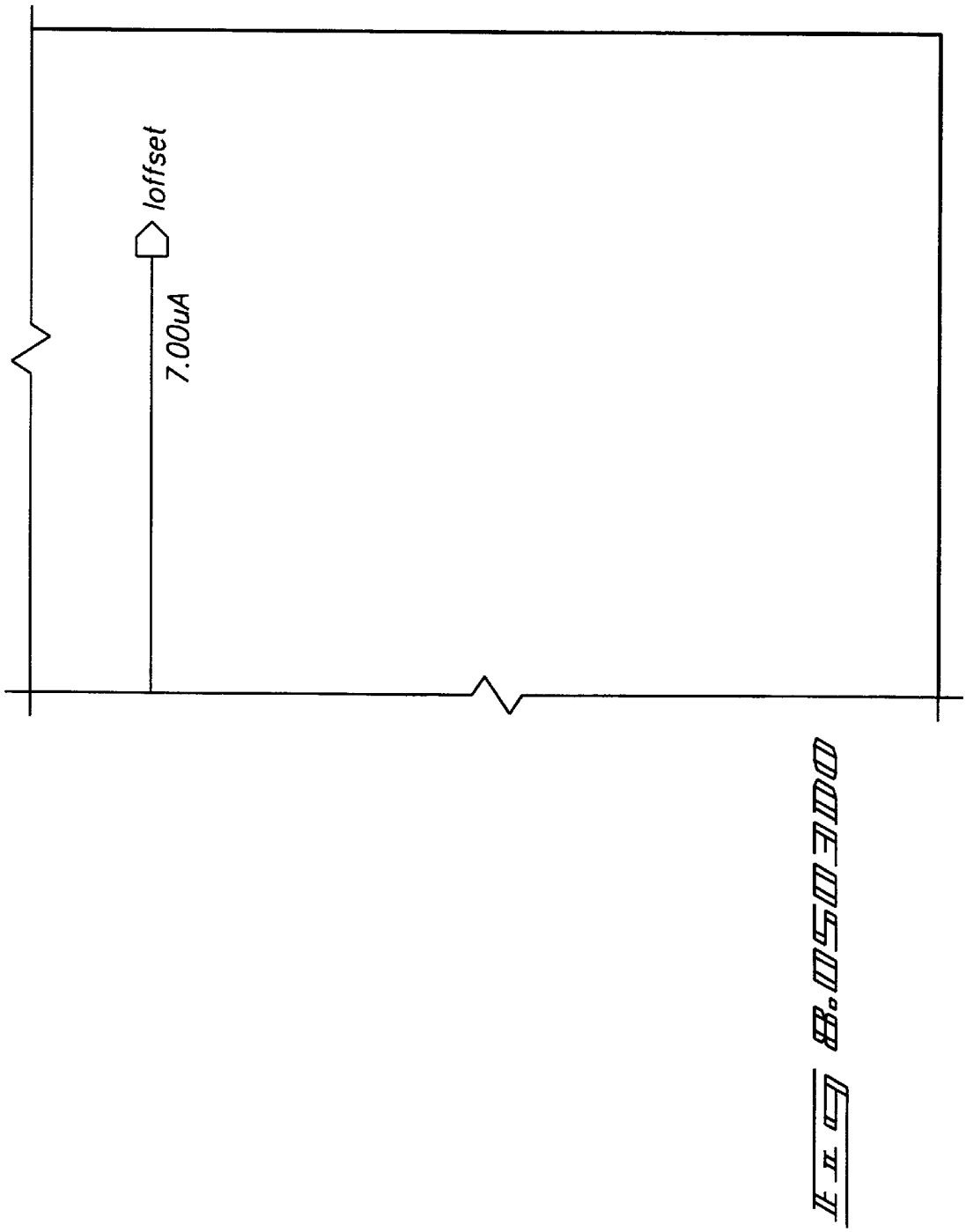


FIG 6,130,602


NODE 5050.88


Ioffset
7.00uA
FIG 88.05000E

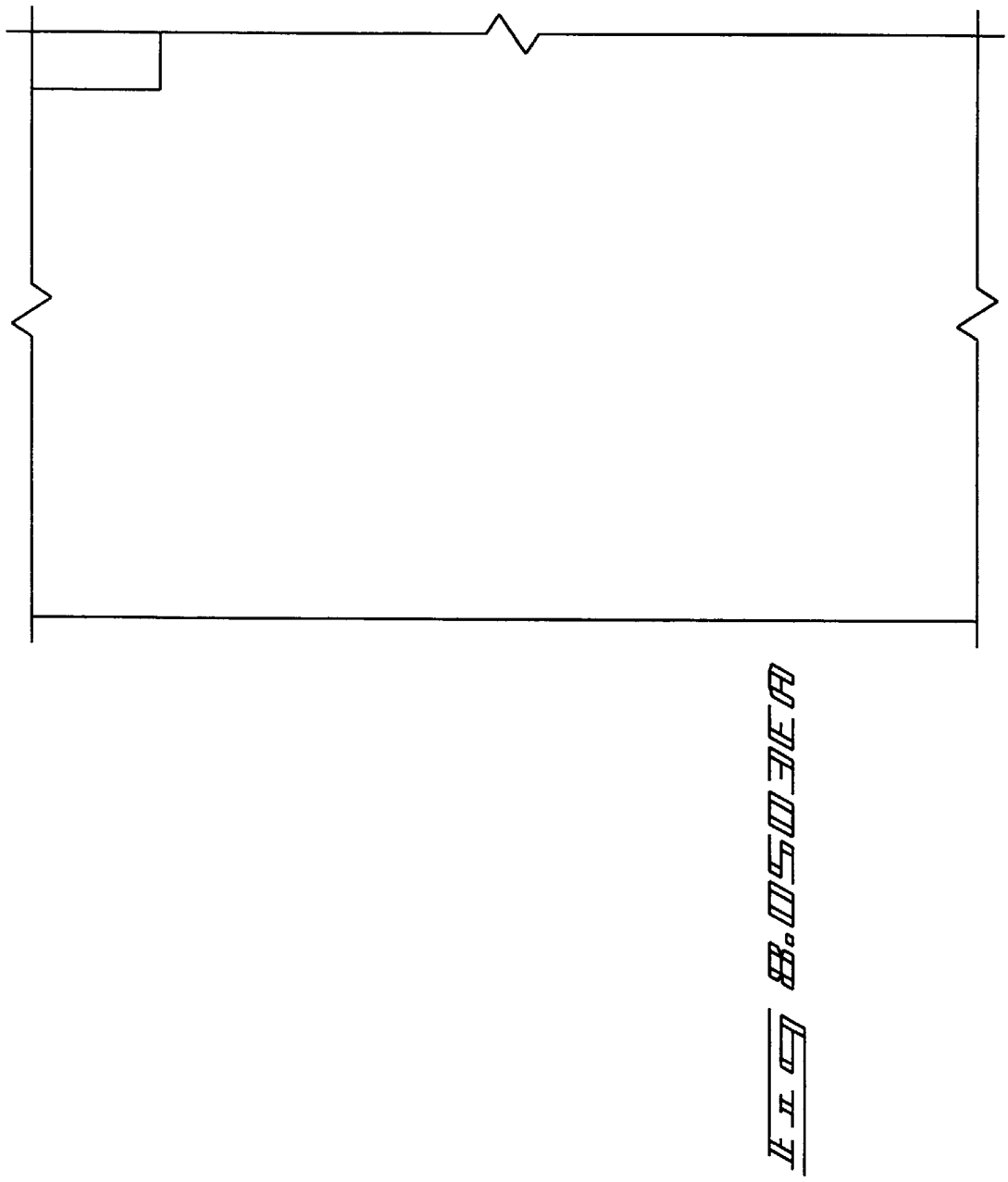


FIG 88.0500EA

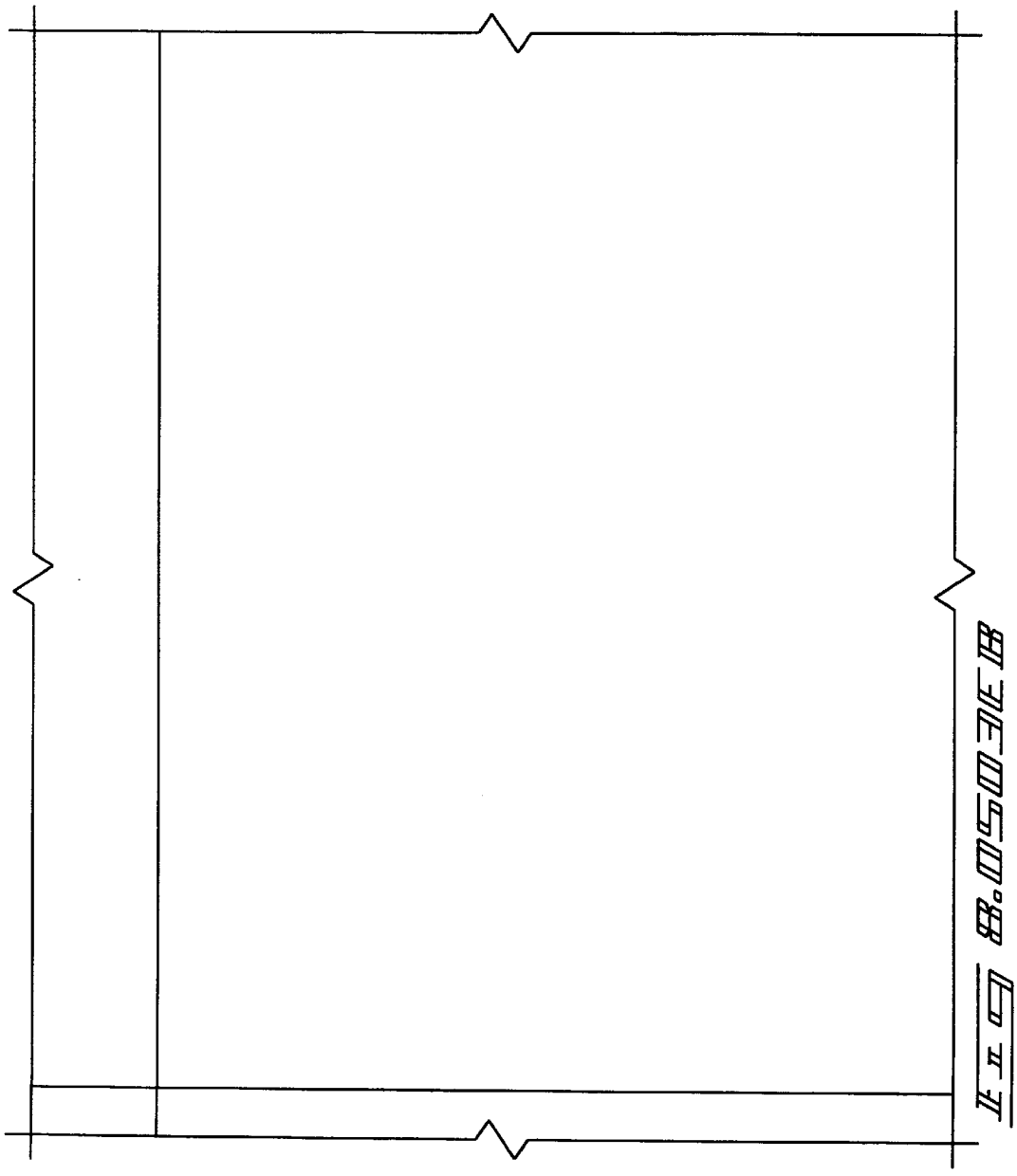


FIG. 88

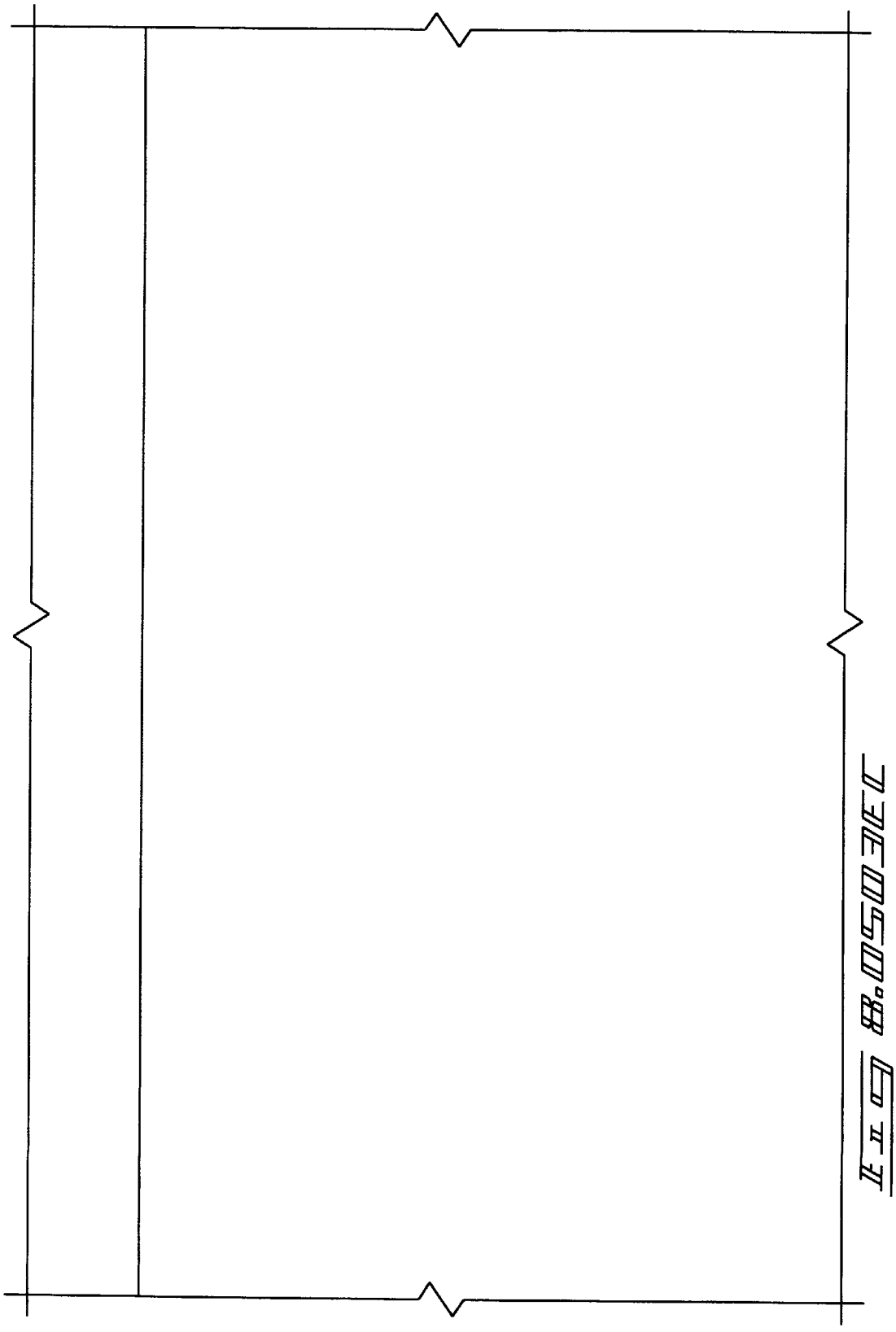


FIG 805.88

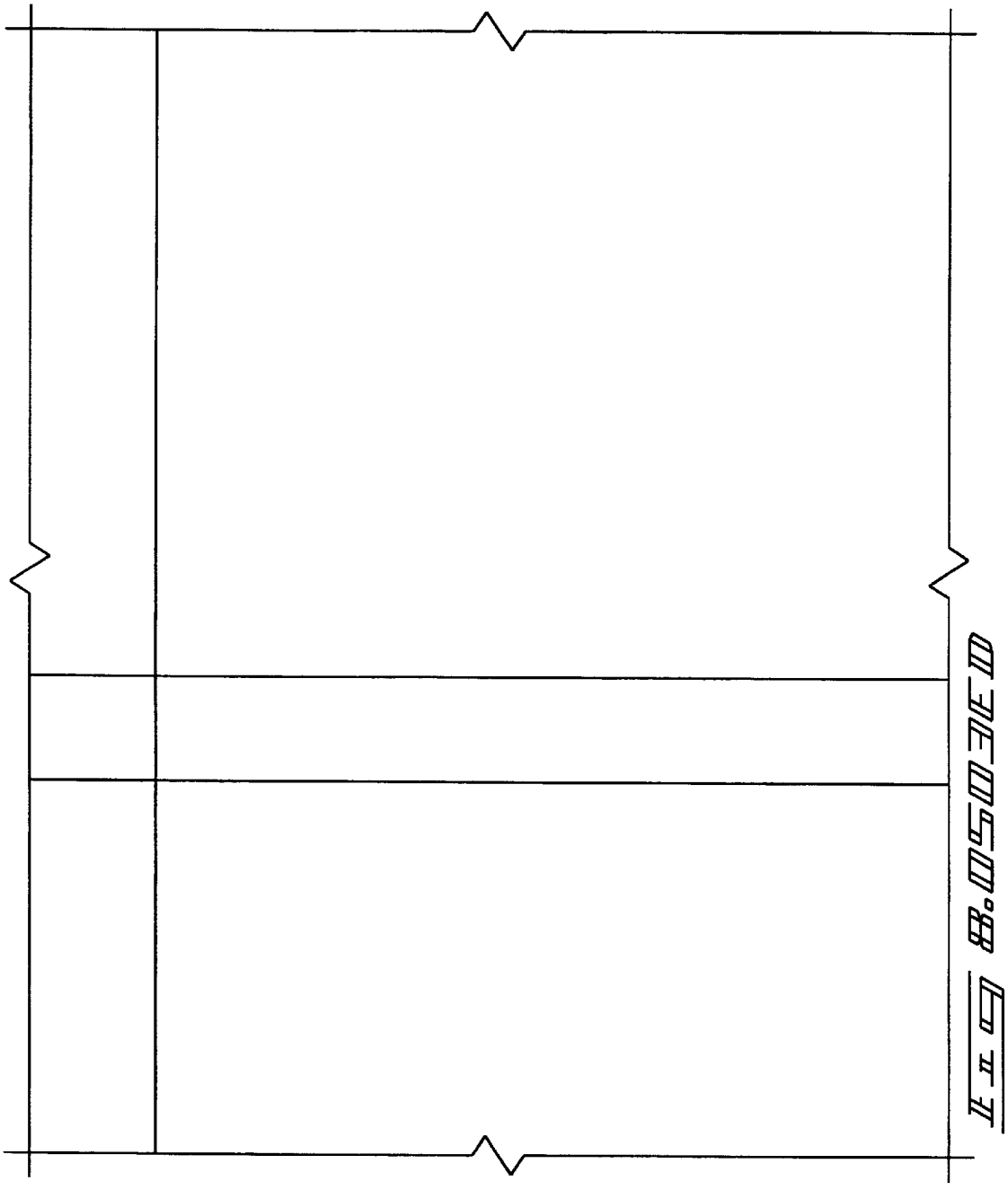


FIG. 850.8E

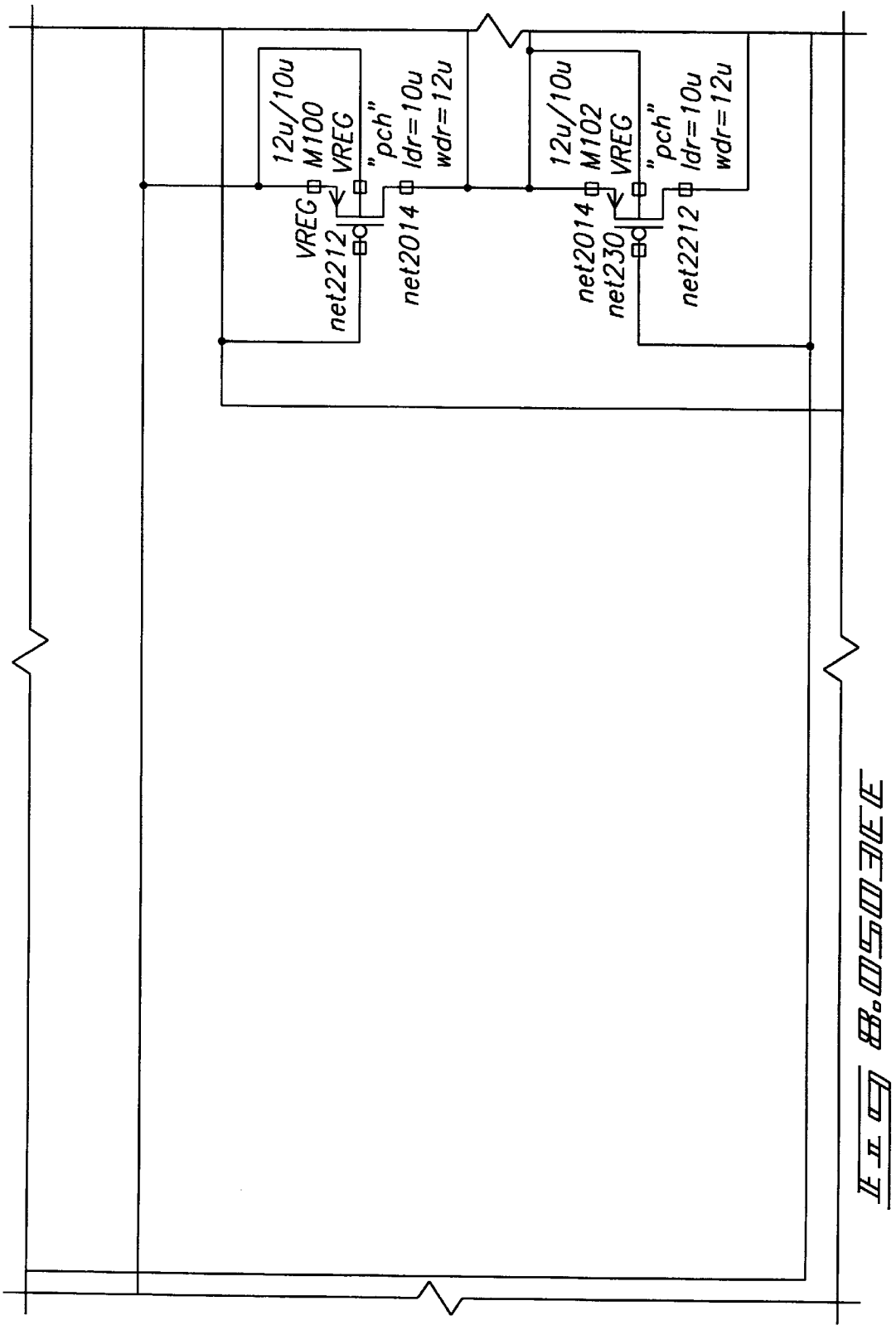

12u/10u
M100
VREG
"pch"
ldr=10u
wdr=12u
VREG
net2212
net2014
12u/10u
M102
VREG
"pch"
ldr=10u
wdr=12u
net2014
net230
net2212

FIG 5058.08

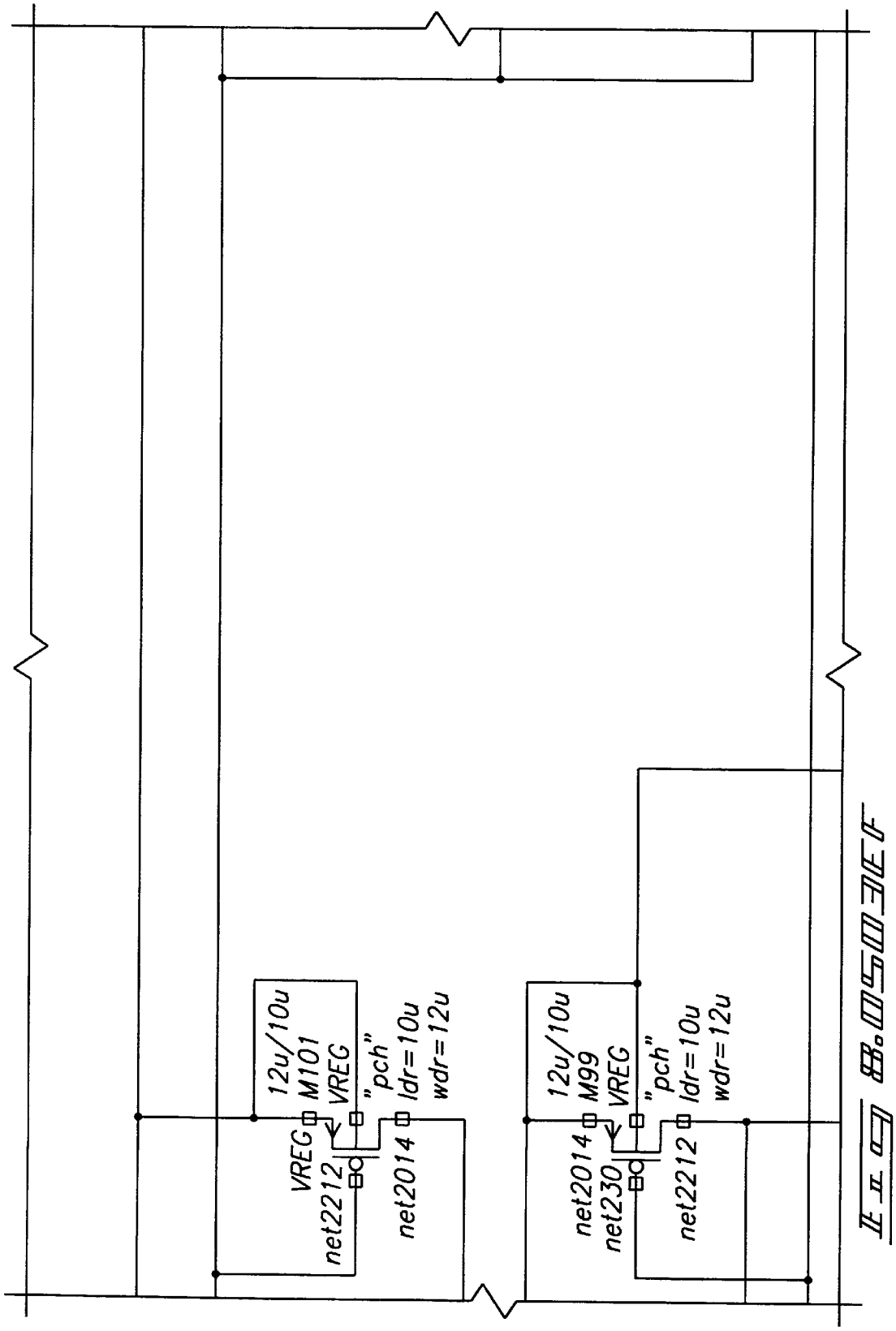

12u/10u
M101
VREG
"pch"
ldr=10u
wdr=12u
VREG
net2212
net2014
12u/10u
M99
VREG
"pch"
ldr=10u
wdr=12u
net2014
net230
net2212

FIG. 1589

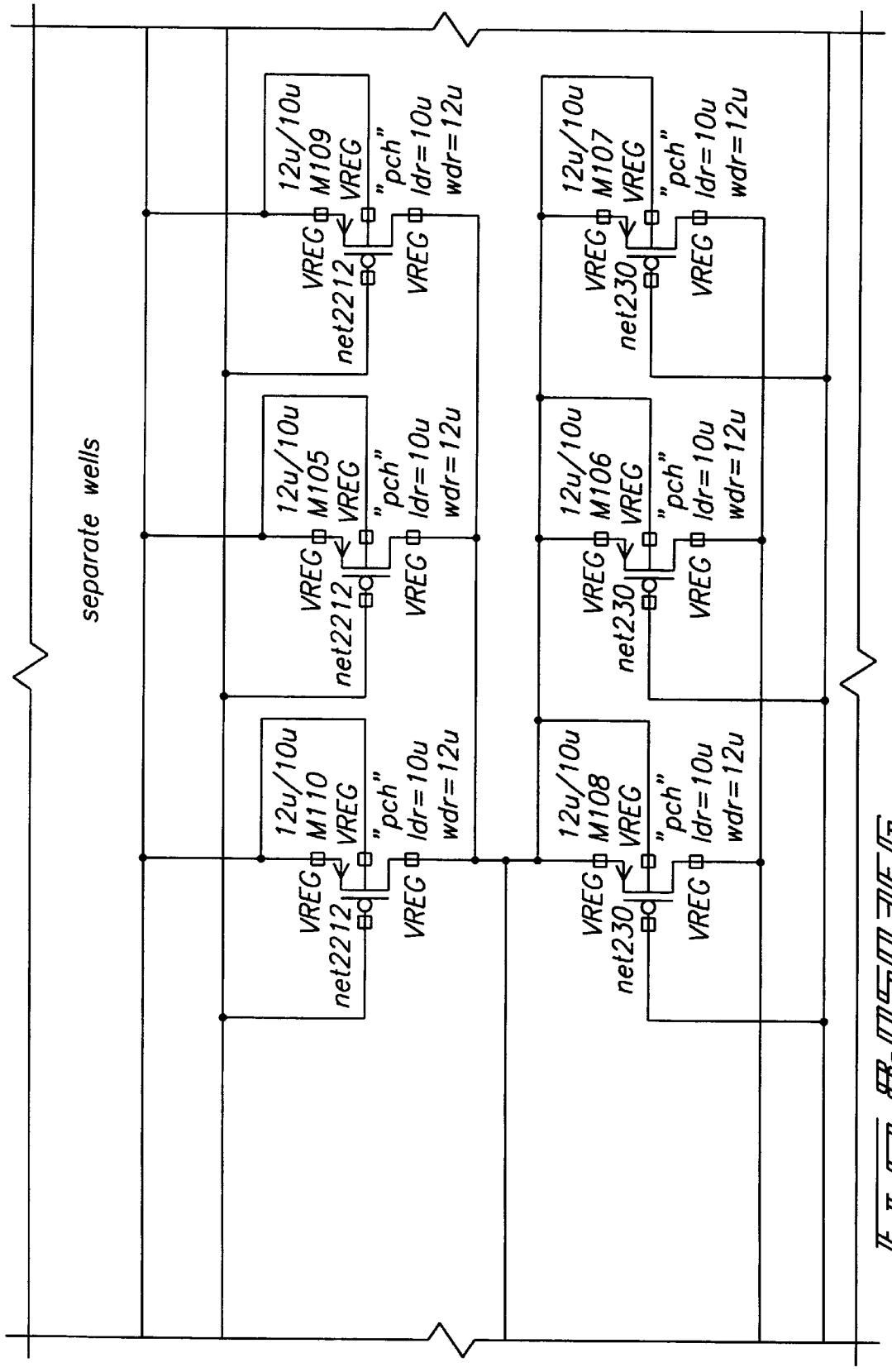
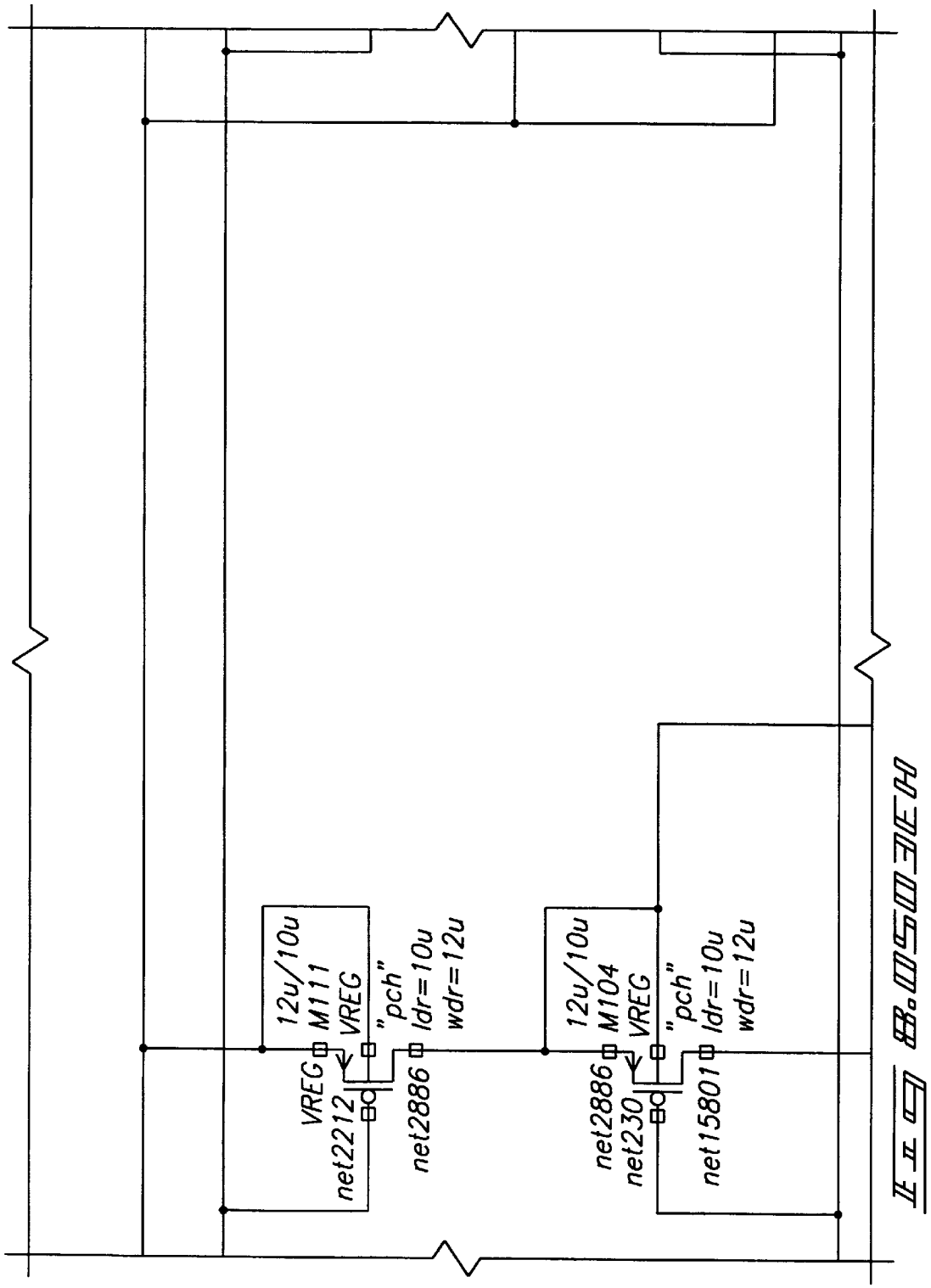

separate wells
12u/10u
M109
VREG
"pch"
ldr=10u
wdr=12u
net2212
12u/10u
M105
12u/10u
M110
12u/10u
M107
12u/10u
M106
12u/10u
M108
net230

FIG. 8,005


12u/10u
M111
VREG
"pch"
ldr=10u
wdr=12u
VREG
net2212
net2886
12u/10u
M104
VREG
"pch"
ldr=10u
wdr=12u
net2886
net230
net15801

Фиг. 1564

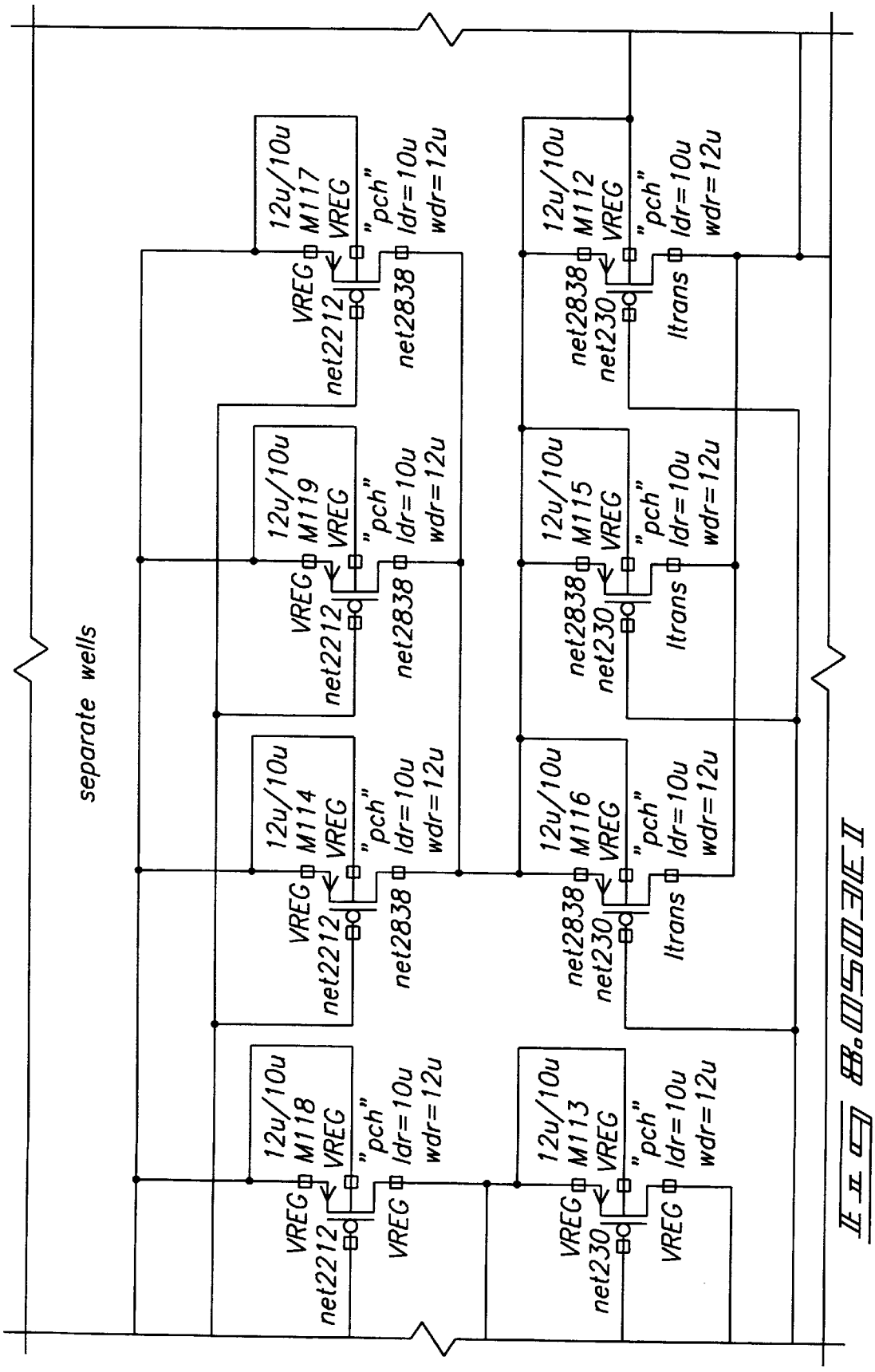

separate wells
12u/10u M117 VREG "pch" ldr=10u wdr=12u
VREG net2212 net2838
12u/10u M119 VREG "pch" ldr=10u wdr=12u
VREG net2212 net2838
12u/10u M114 VREG "pch" ldr=10u wdr=12u
VREG net2212 net2838
12u/10u M118 VREG "pch" ldr=10u wdr=12u
VREG net2212 VREG
12u/10u M112 VREG "pch" ldr=10u wdr=12u
net2838 net230 ltrans
12u/10u M115 VREG "pch" ldr=10u wdr=12u
net2838 net230 ltrans
12u/10u M116 VREG "pch" ldr=10u wdr=12u
net2838 net230 ltrans
12u/10u M113 VREG "pch" ldr=10u wdr=12u
VREG net230 VREG

FIG. 8,005

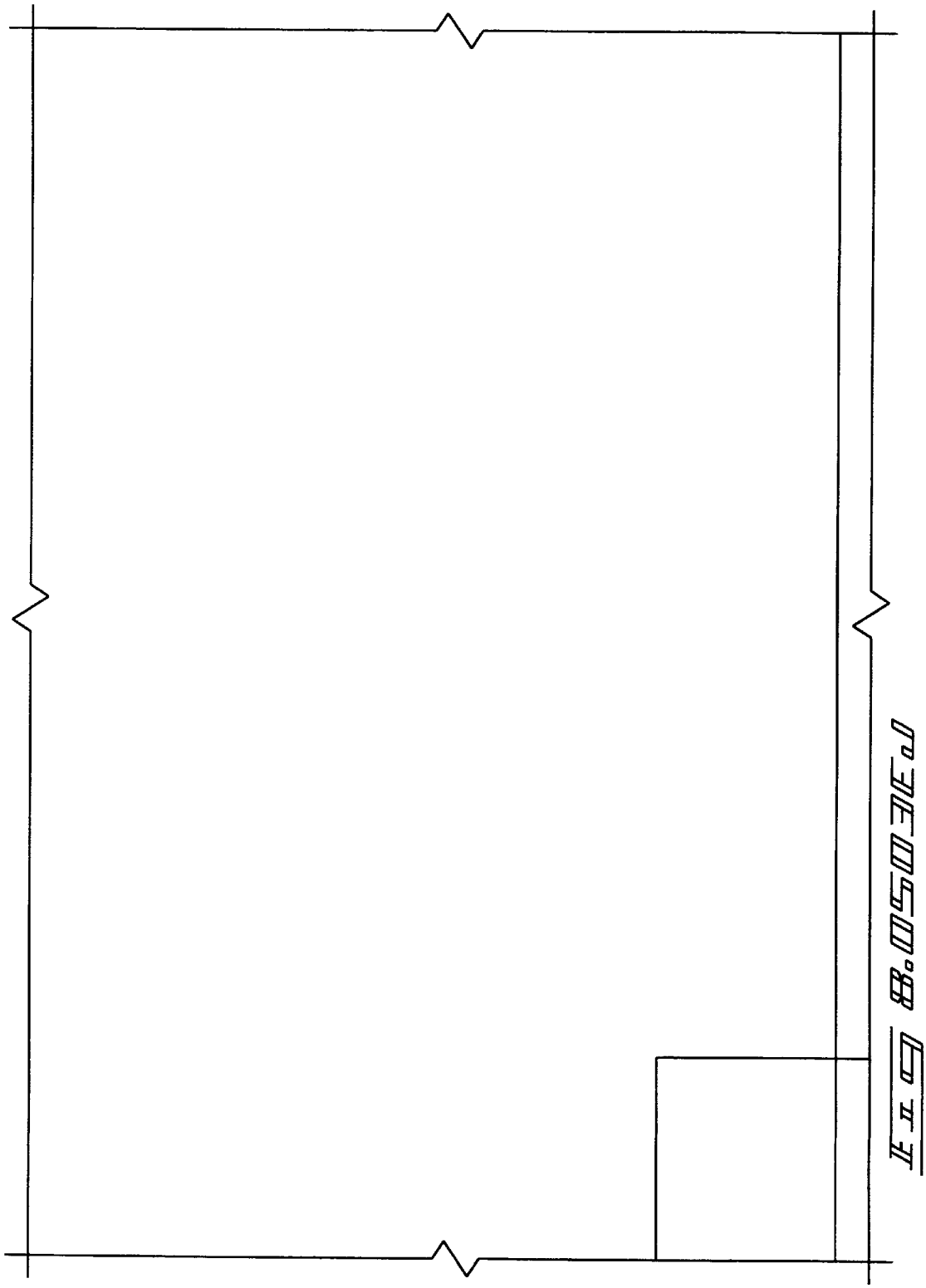


FIG 88.0500

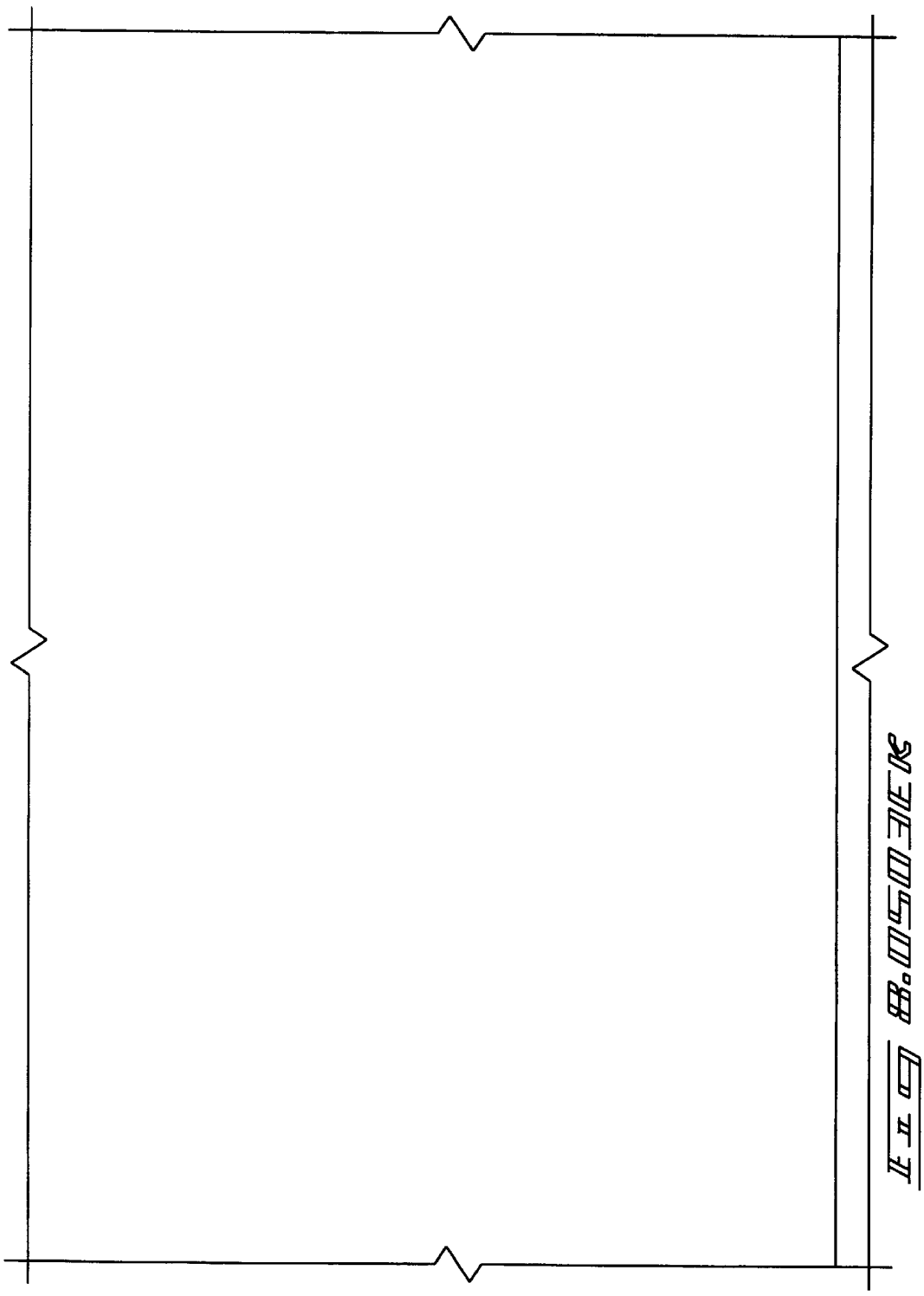


FIG 88.050E3

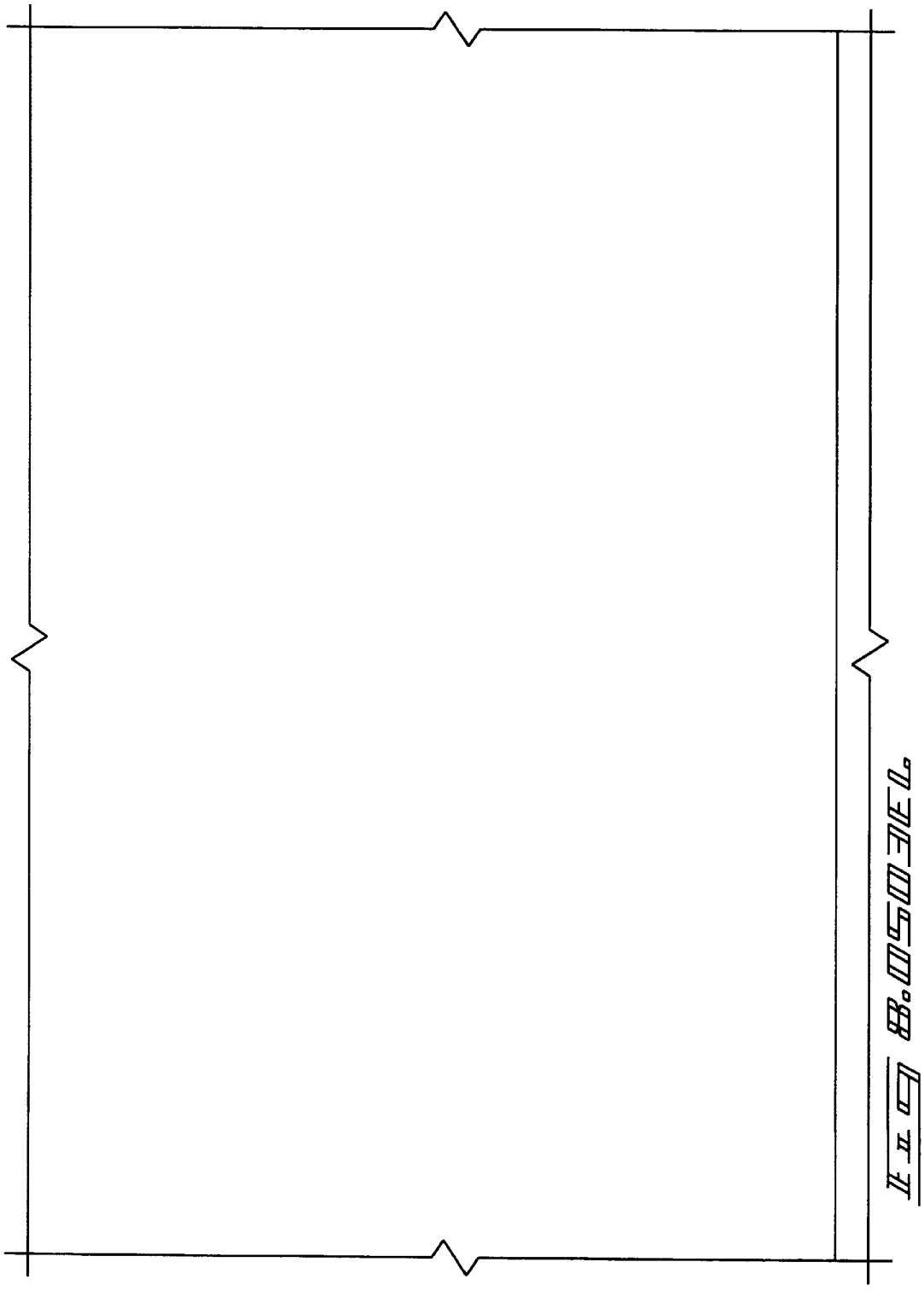
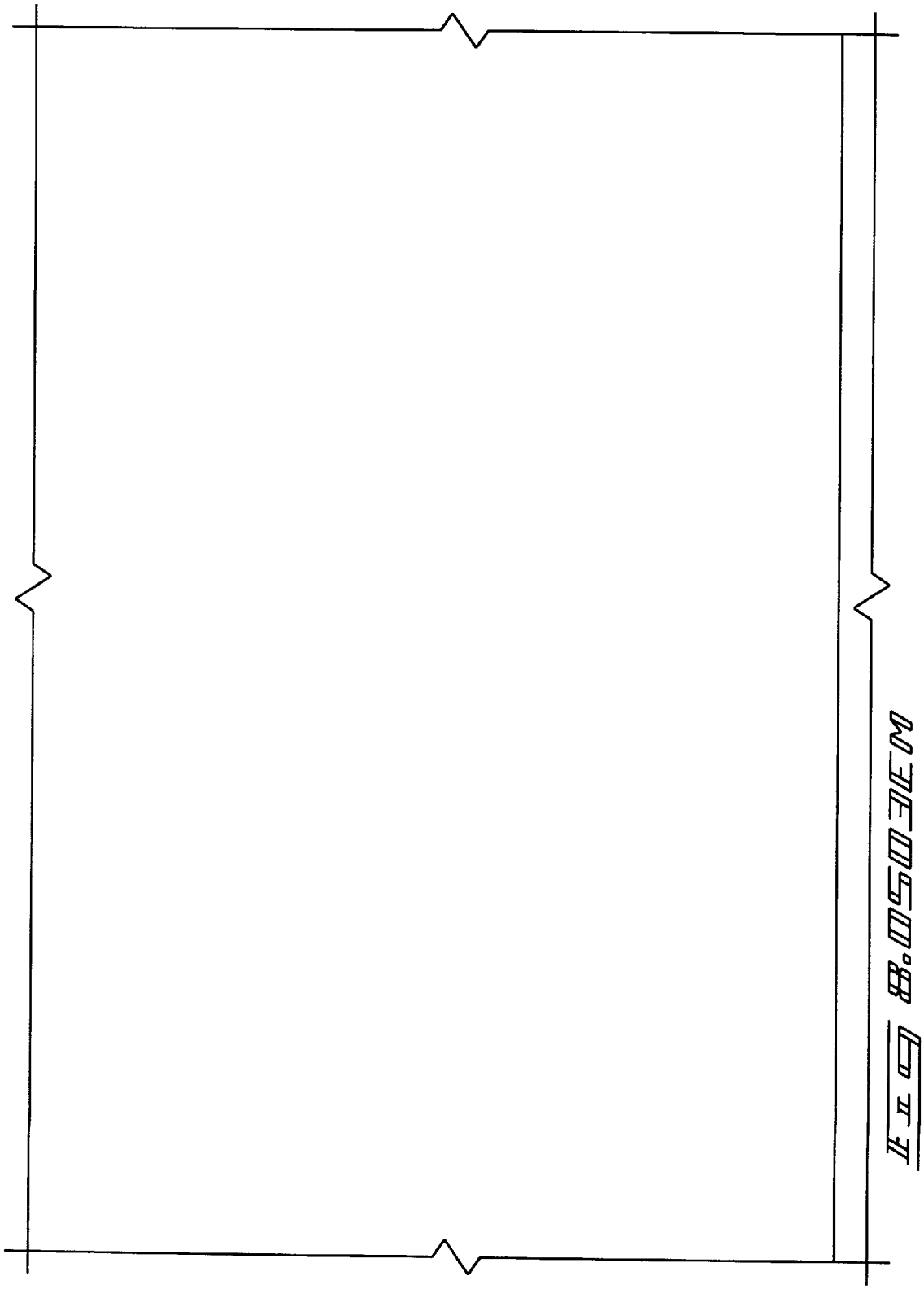


FIG 68,050


WEBSOCKET

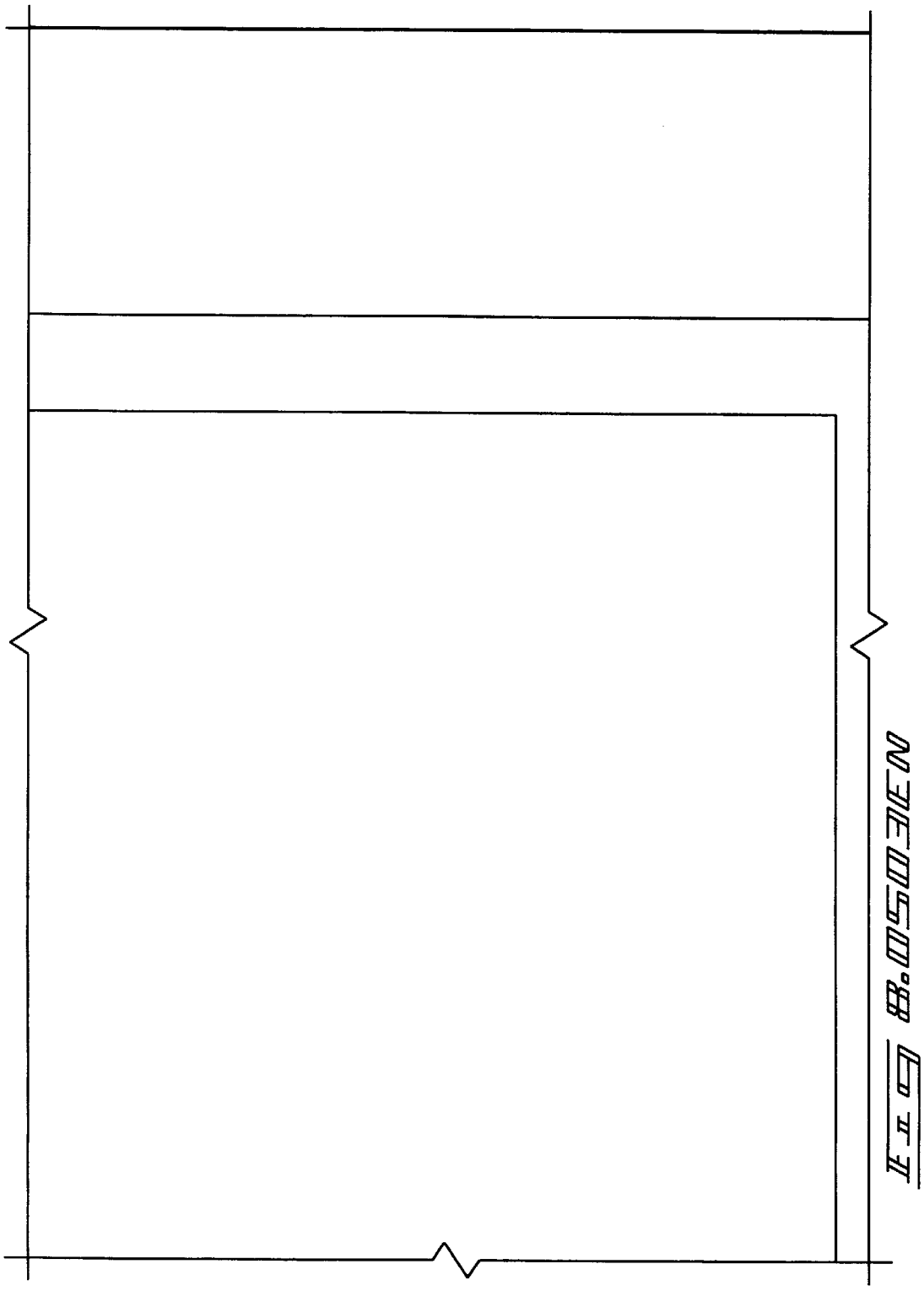


FIG. 8,050,EN

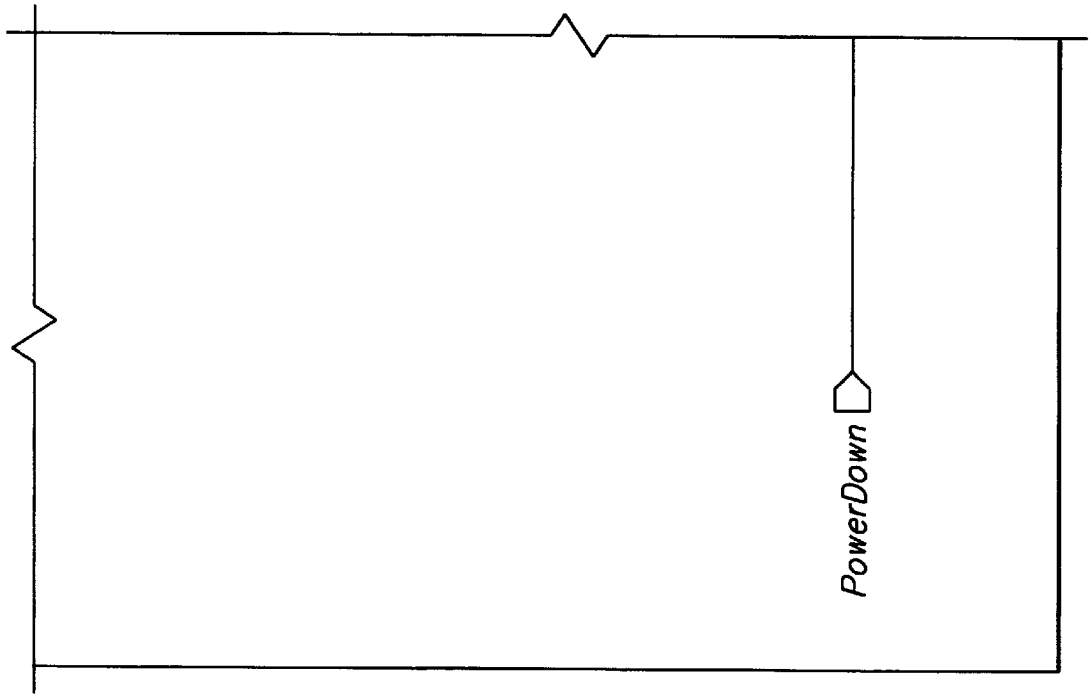


FIG 88.00500E-A

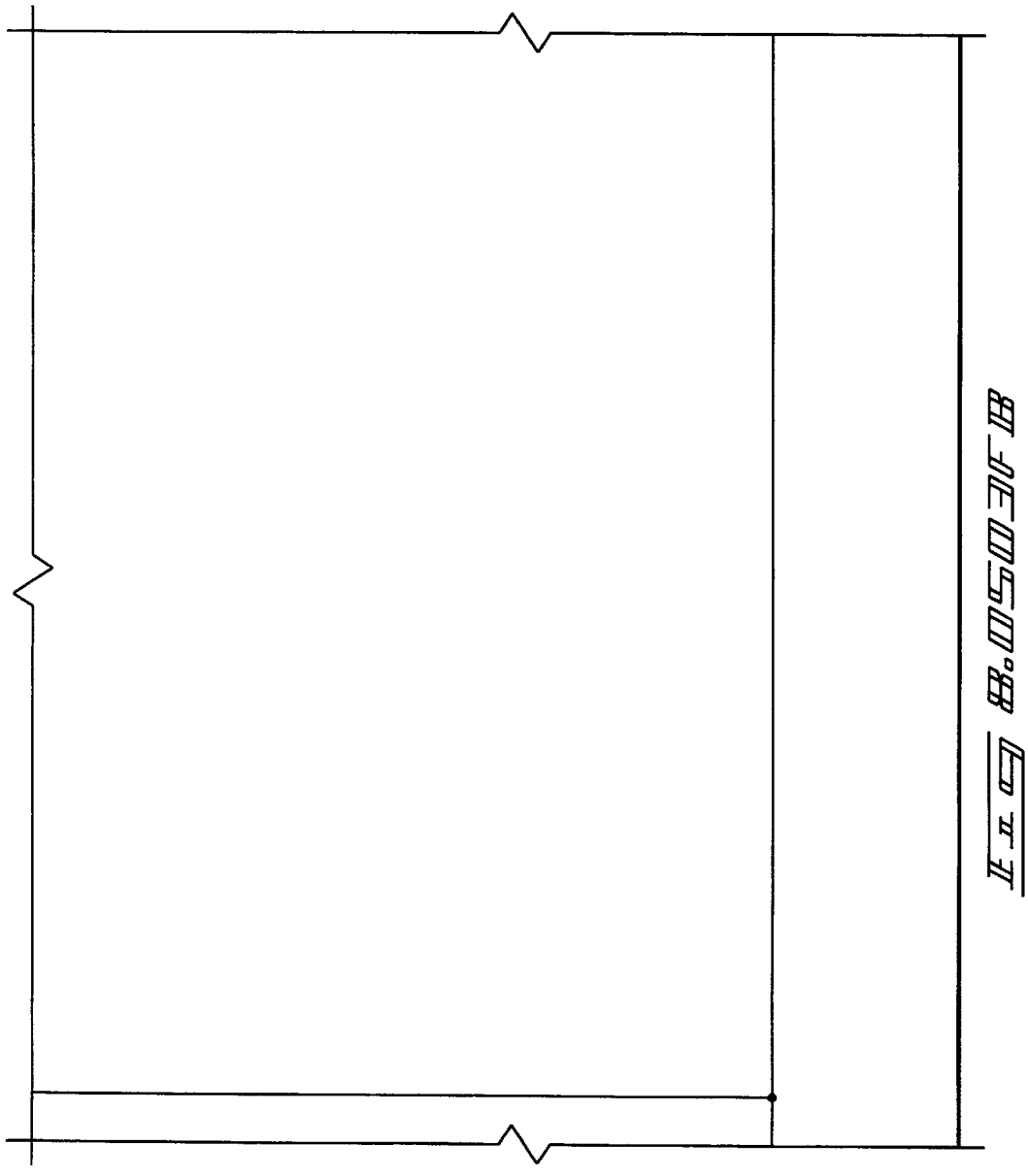


FIG 88,005 JE

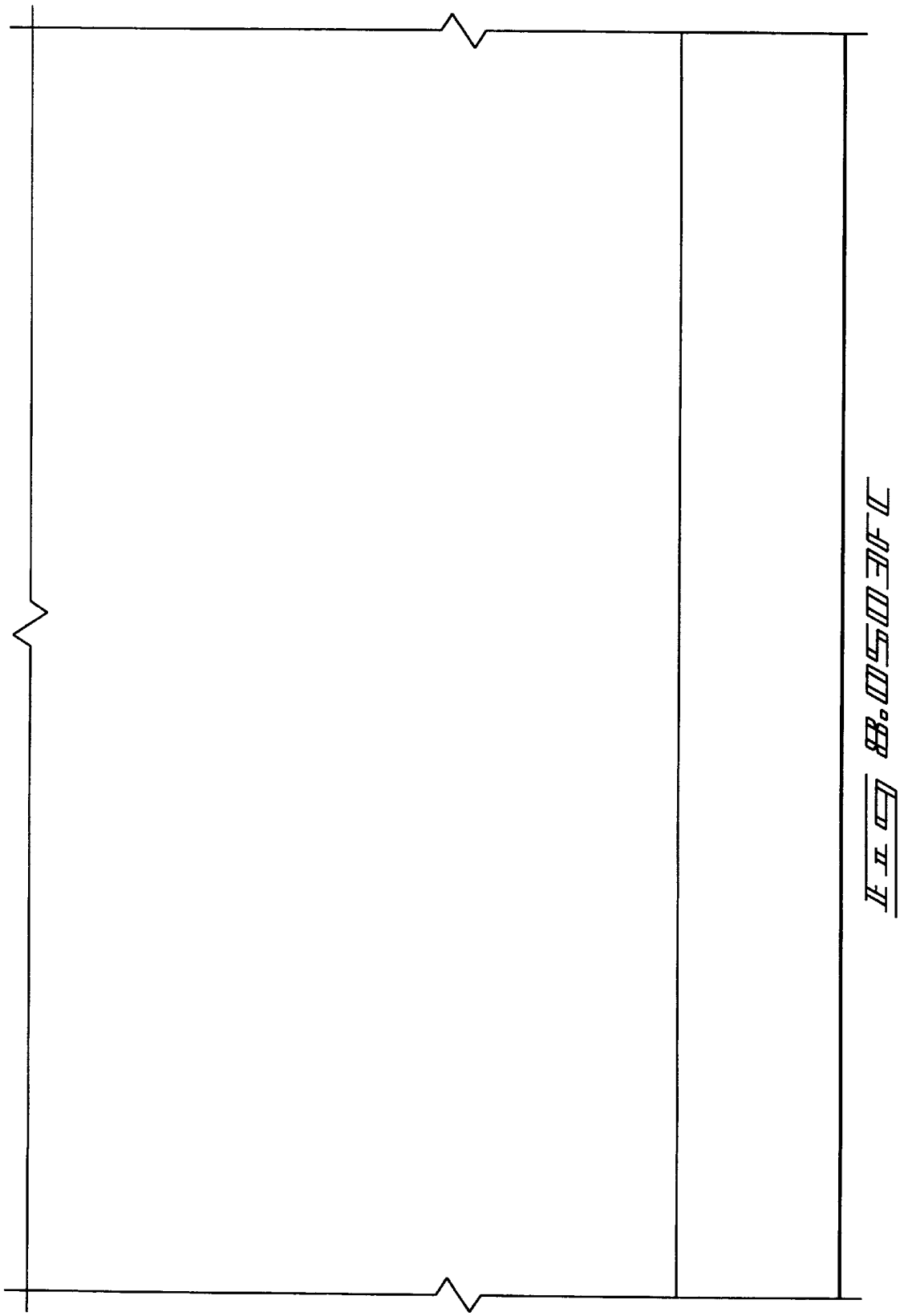


FIG 88,050

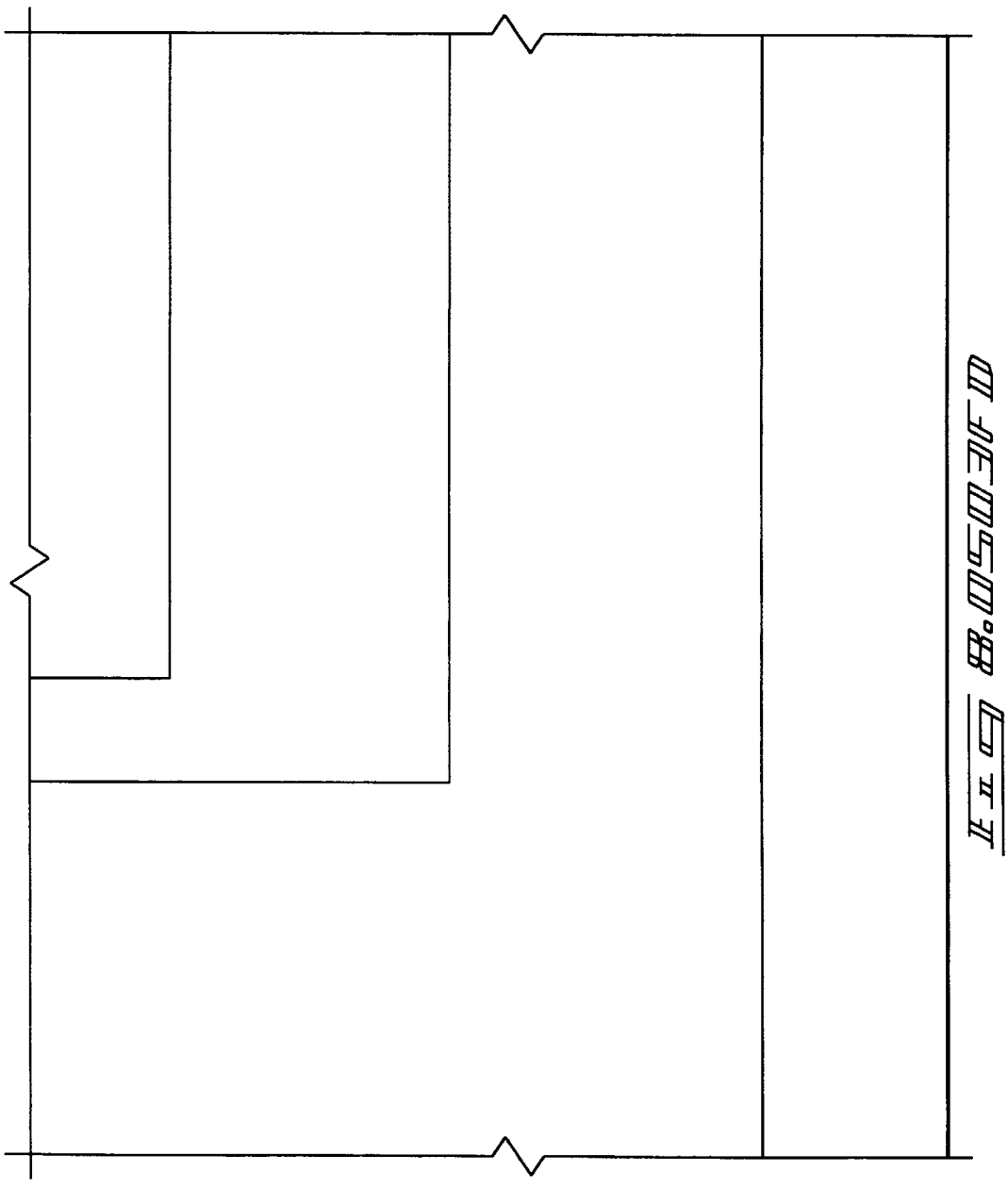


FIG 68,050

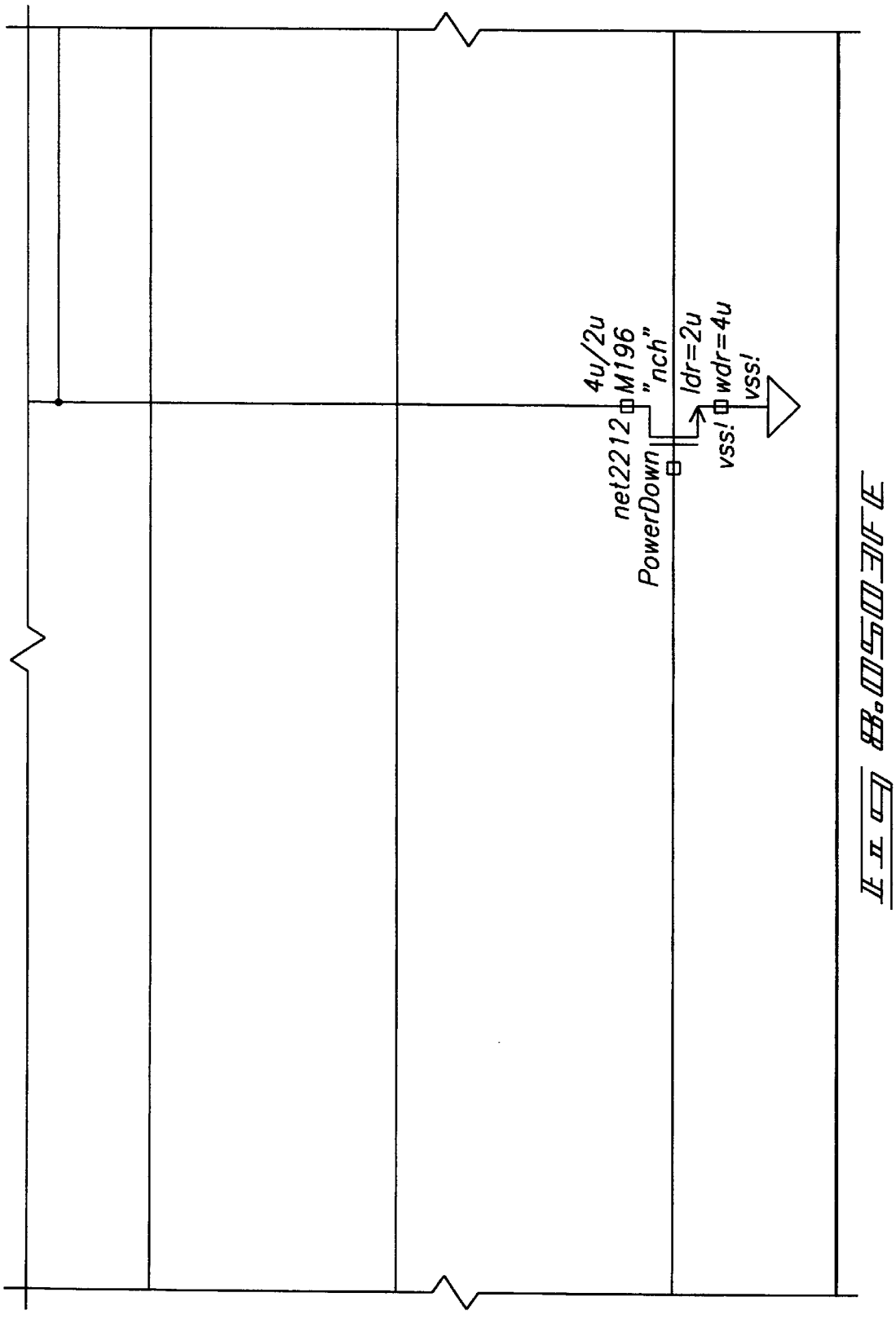


FIG. 88,005

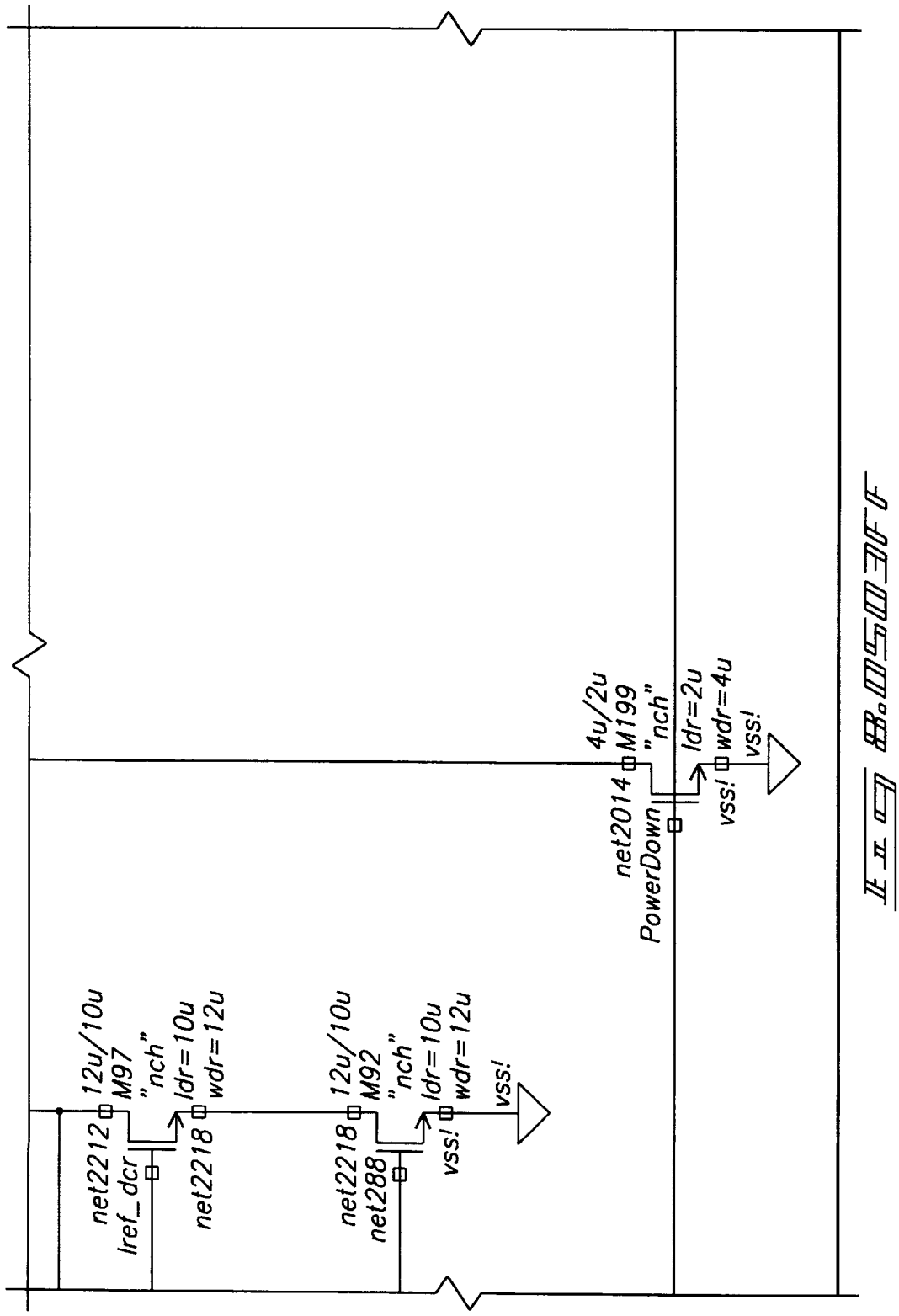
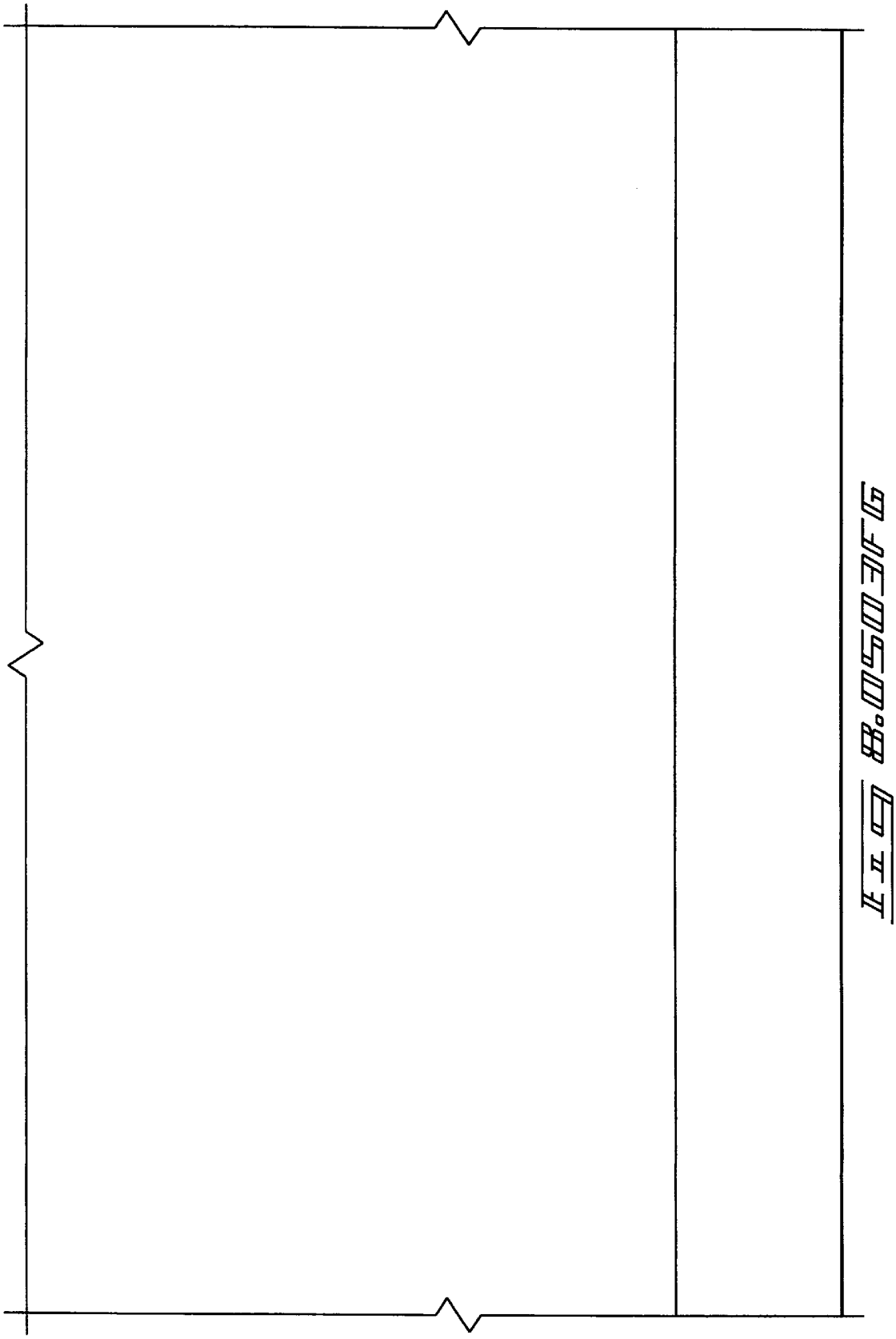

net2212
Iref_dcr
12u/10u
M97
"nch"
ldr=10u
wdr=12u
net2218
net2218
net288
12u/10u
M92
"nch"
ldr=10u
wdr=12u
vss!
vss!
4u/2u
M199
"nch"
ldr=2u
wdr=4u
vss!
net2014
PowerDown
vss!

FIG. 88.0050F


SEQ ID NO 88 (5' to 3')

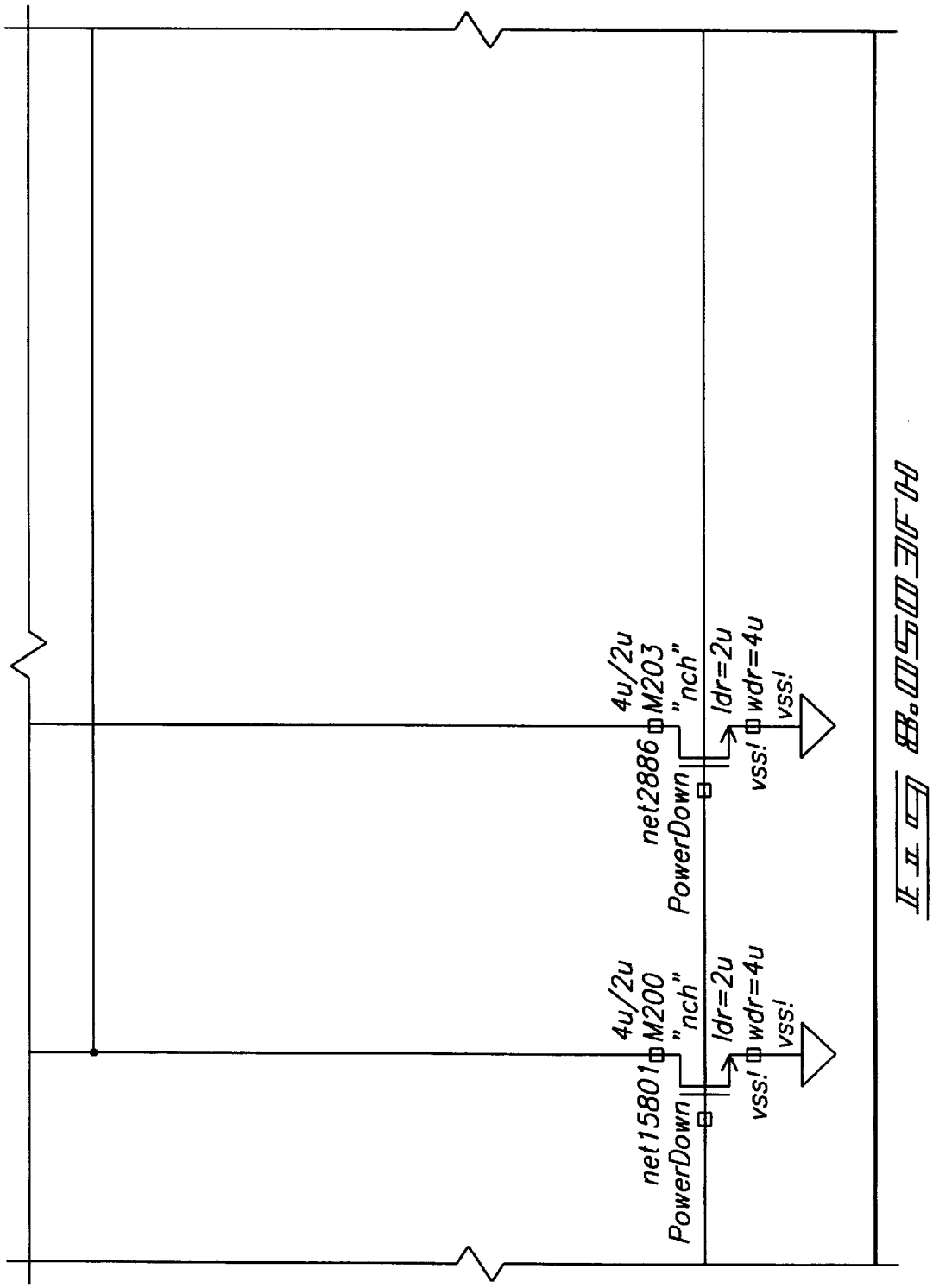

4u/2u
M203
"nch"
ldr=2u
wdr=4u
vss!
net2886
PowerDown
vss!
4u/2u
M200
"nch"
ldr=2u
wdr=4u
vss!
net15801
PowerDown
vss!

FIG. 8,0500

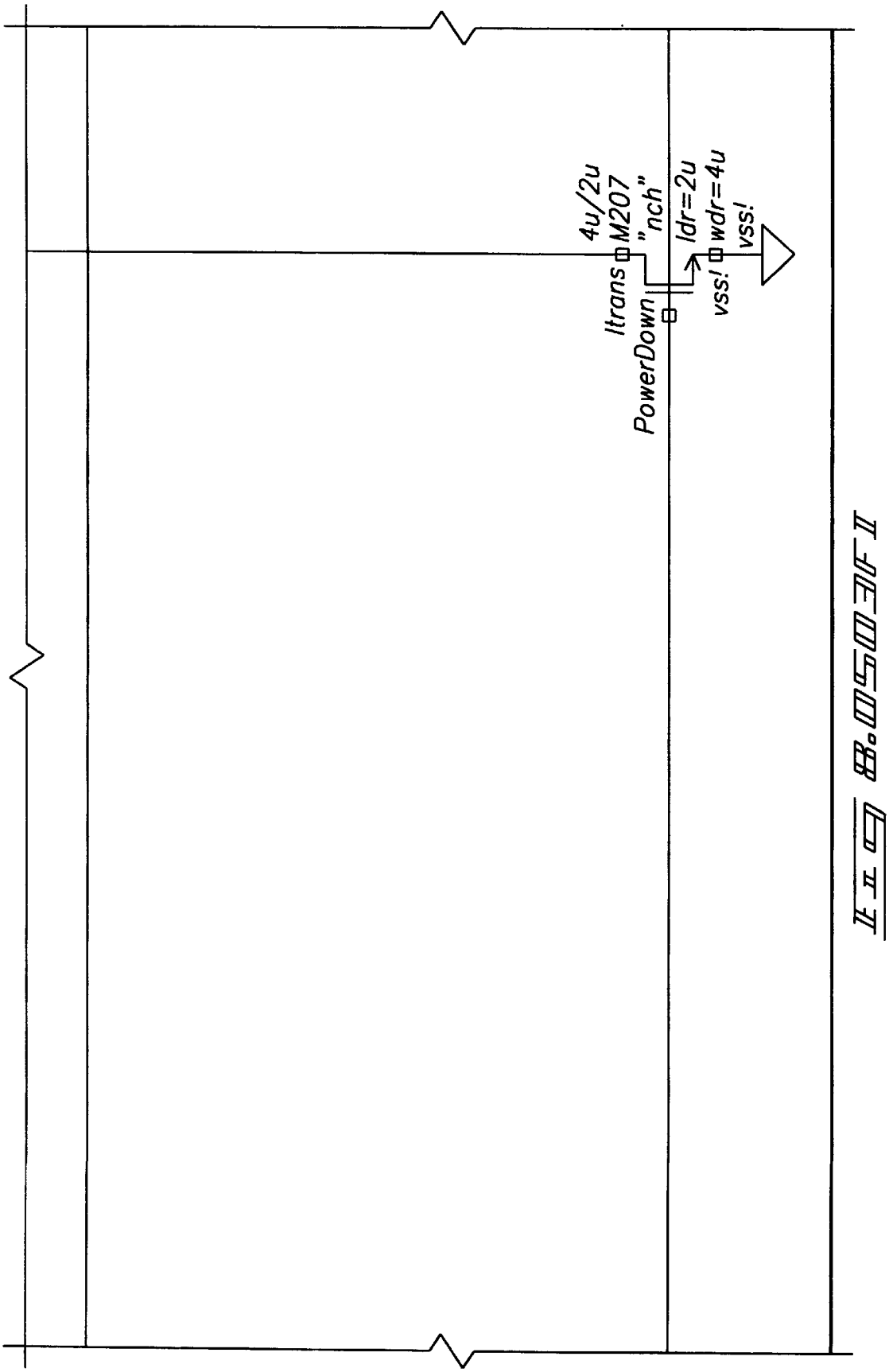


FIG 88,005

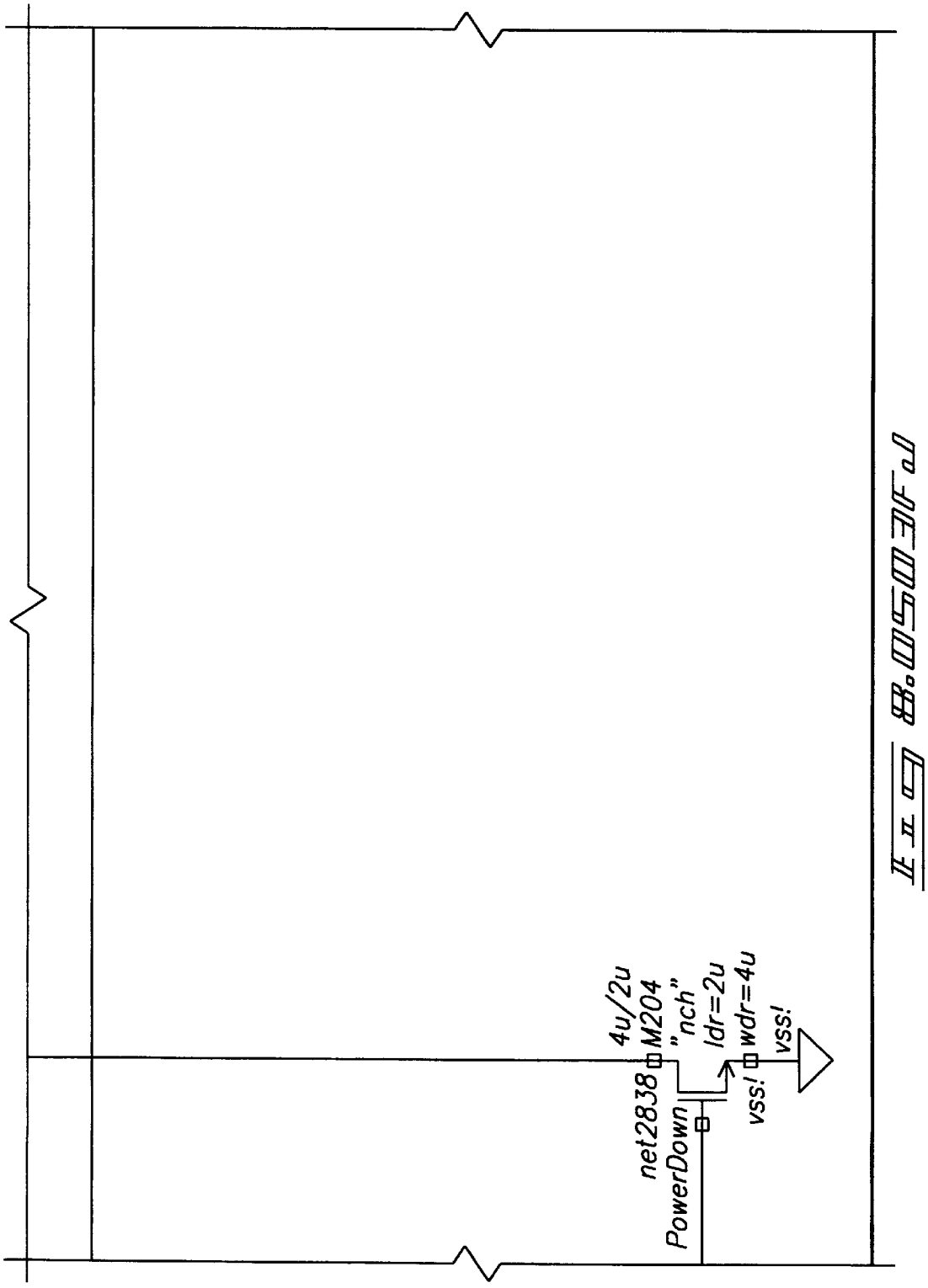


FIG 88.0500F
4u/2u
M204
"nch"
ldr=2u
wdr=4u
vss!
vss!
net2838
PowerDown

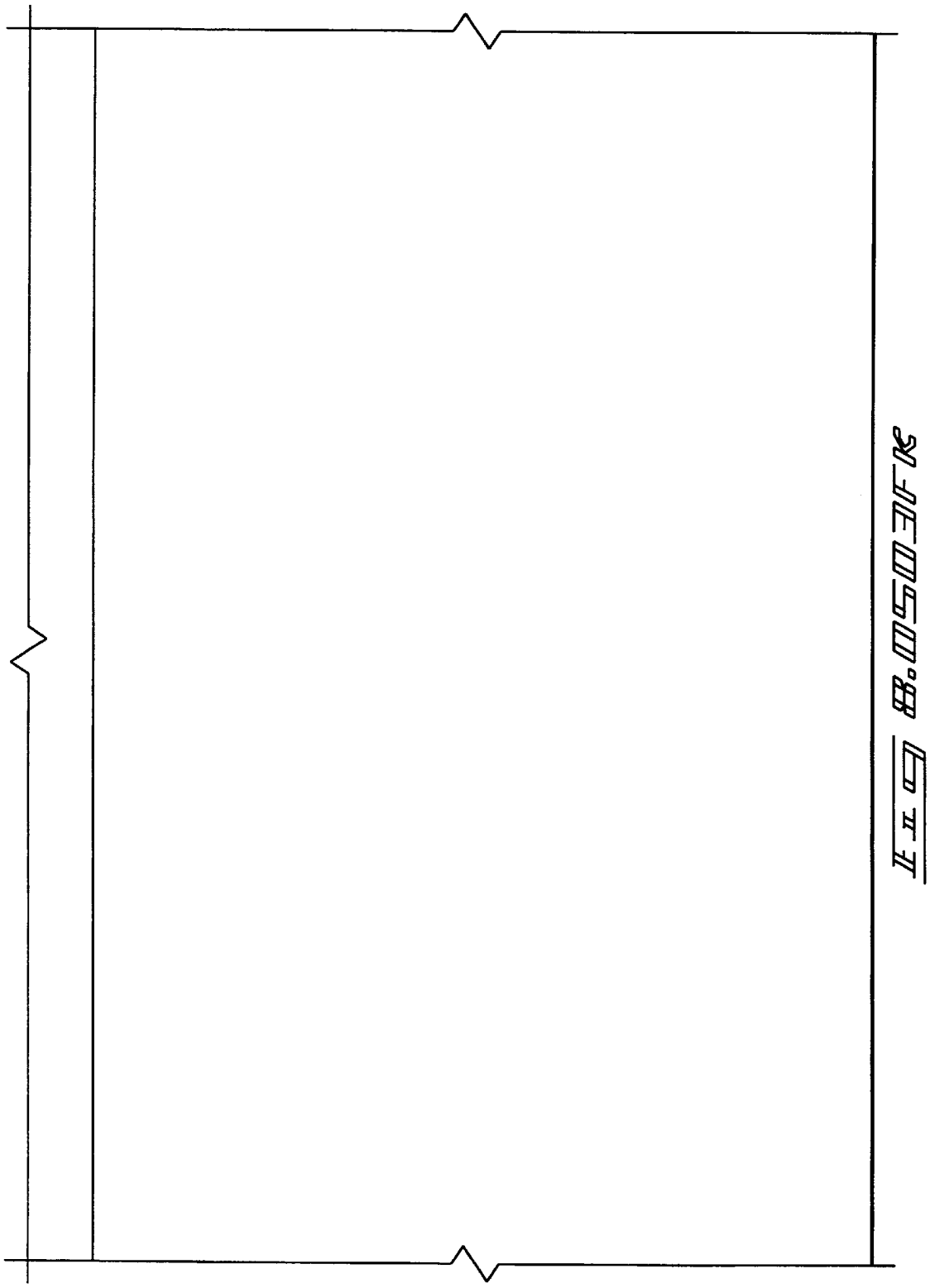


FIG 8,050

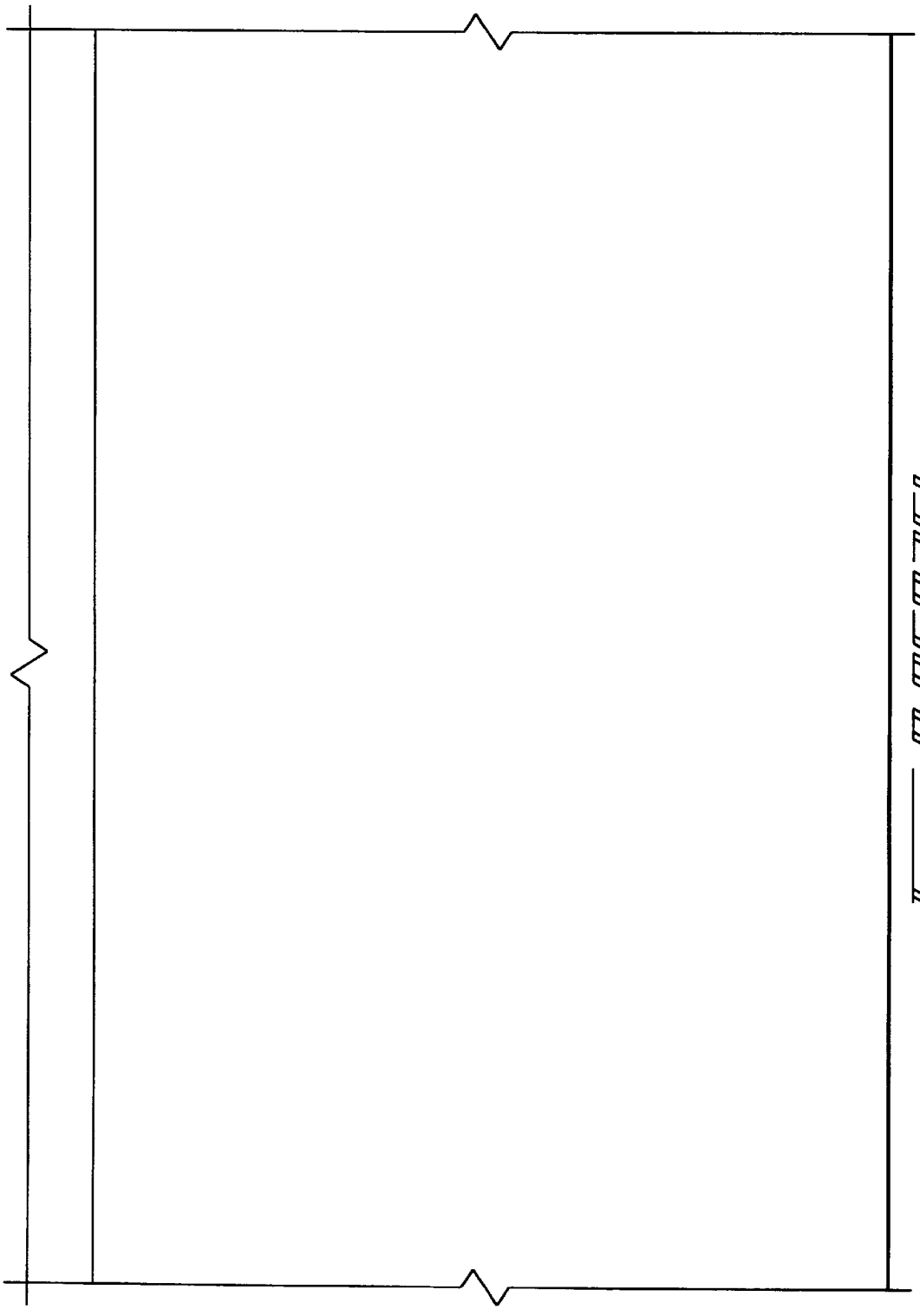


FIG 88

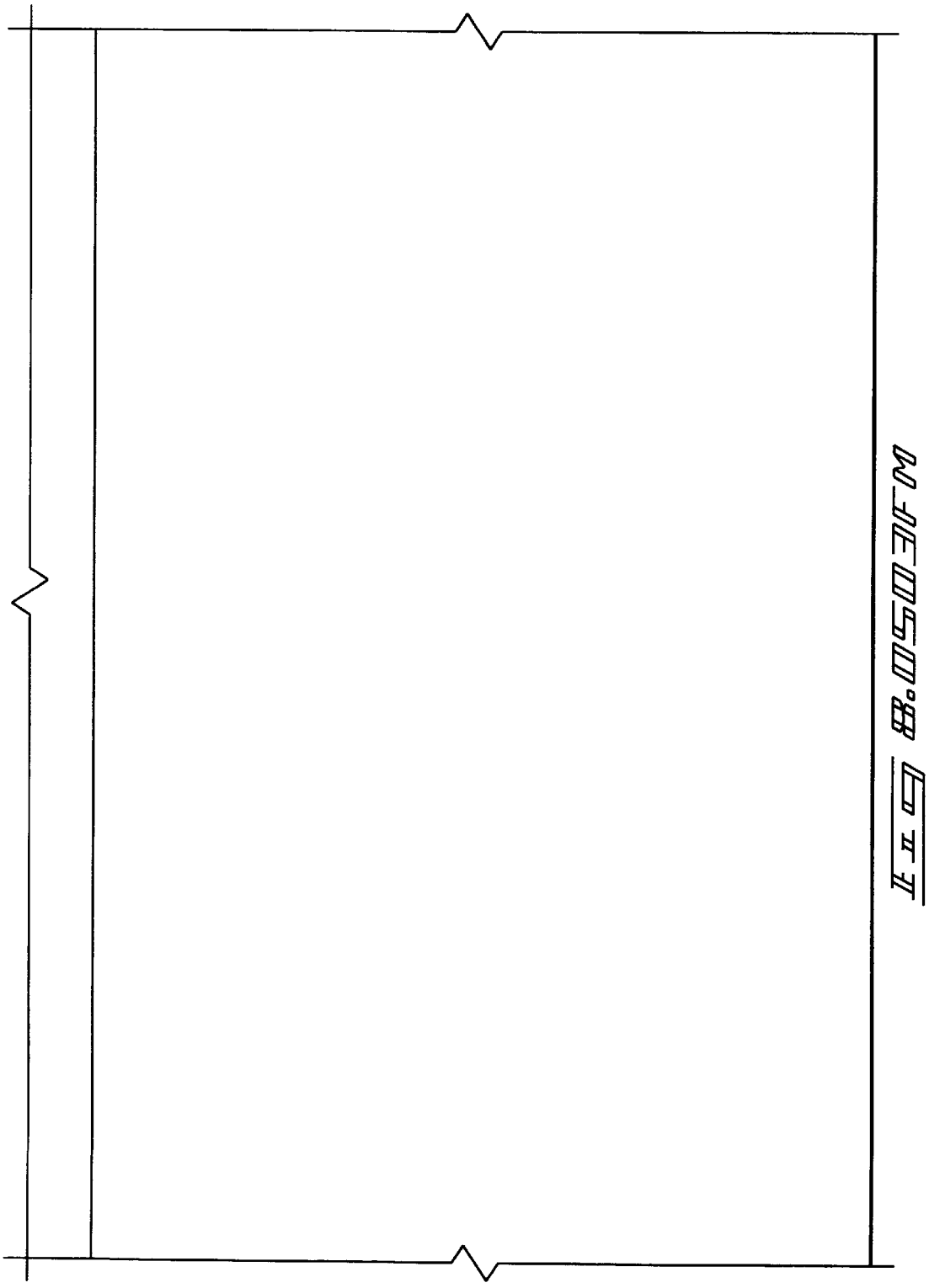


FIG 8050

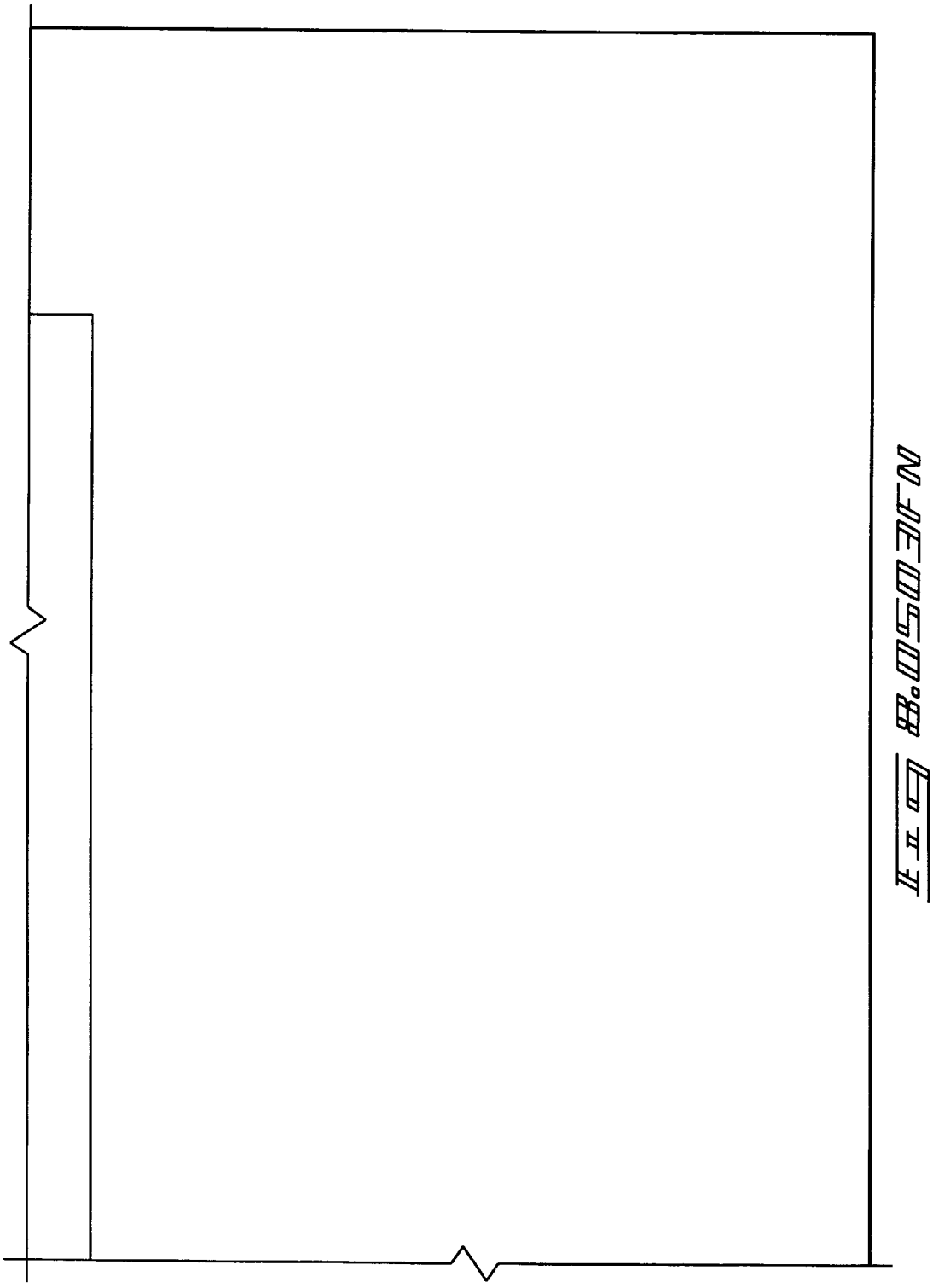


FIG 88,050

8.0504AA	8.0504AB	8.0504AC	8.0504AD	
8.0504BA	8.0504BB	8.0504BC	8.0504BD	8.0504CE
8.0504CA	8.0504CB	8.0504CC	8.0504CD	8.0504DE
8.0504DA	8.0504DB	8.0504DC	8.0504DD	8.0504EE
8.0504EA	8.0504EB	8.0504EC	8.0504ED	

FIG. 8,050,4

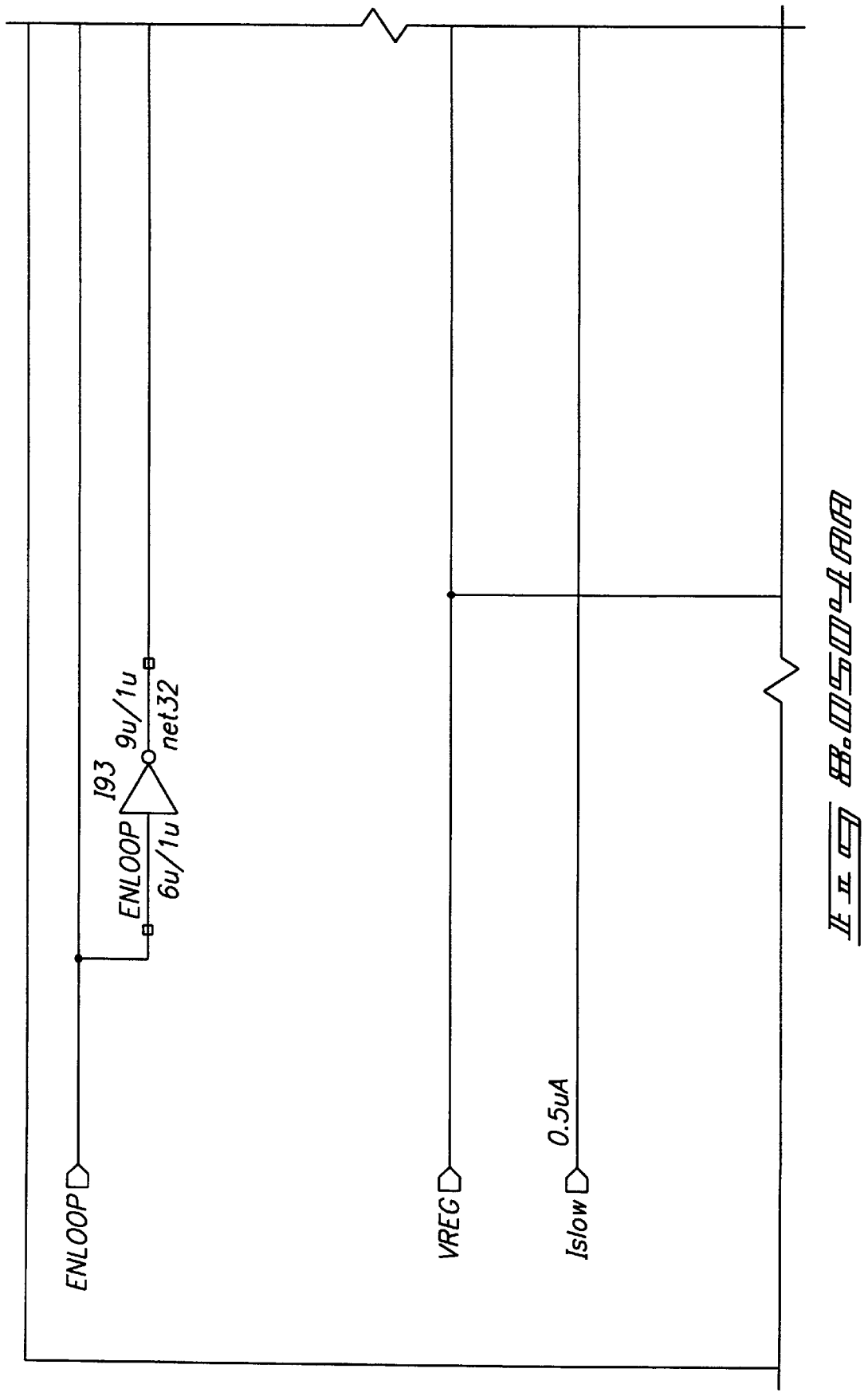


FIG 88.0504AA

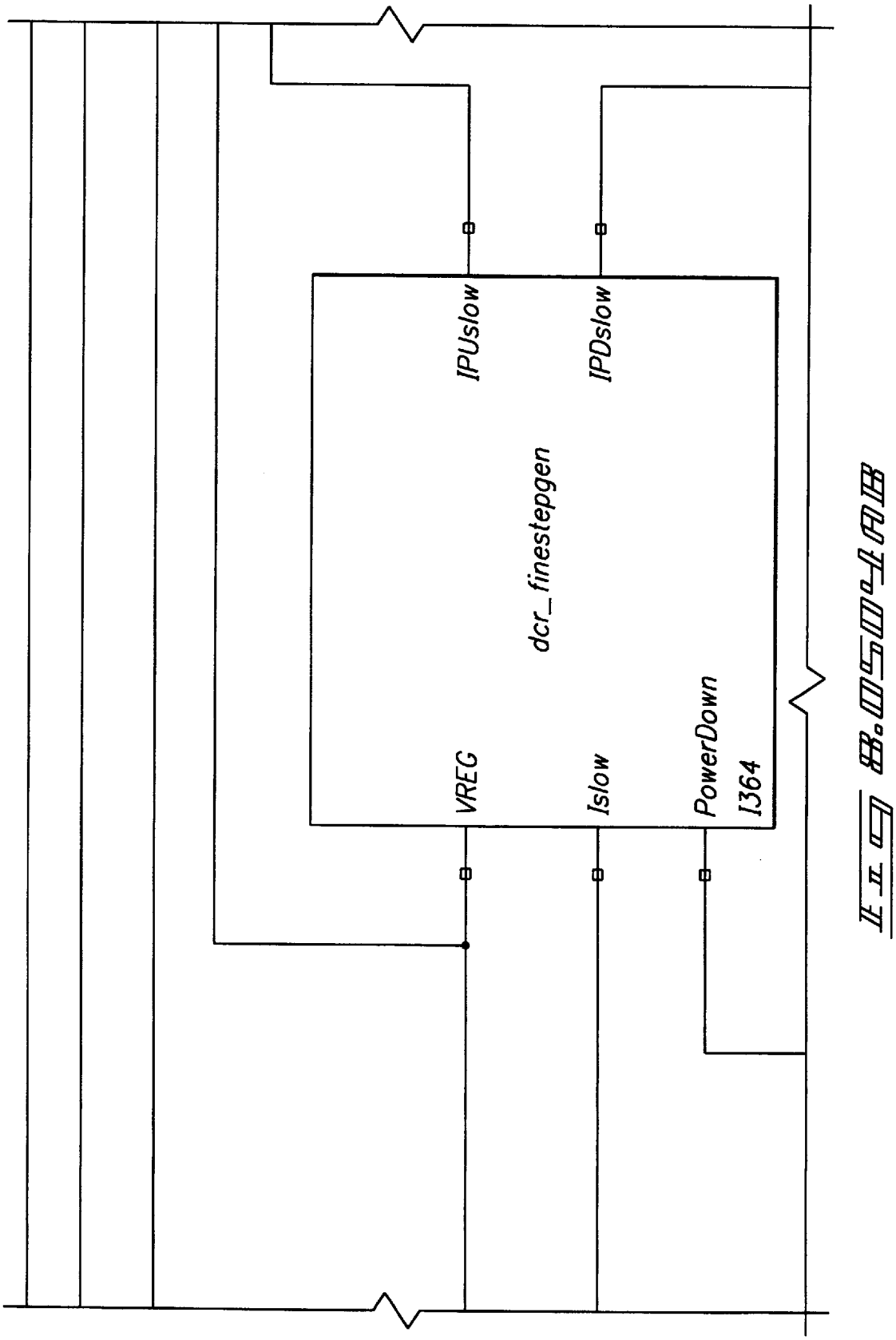

IPUslow
IPDslow
dcr_finestepgen
VREG
Islow
PowerDown
I364

FIG 8,805,048

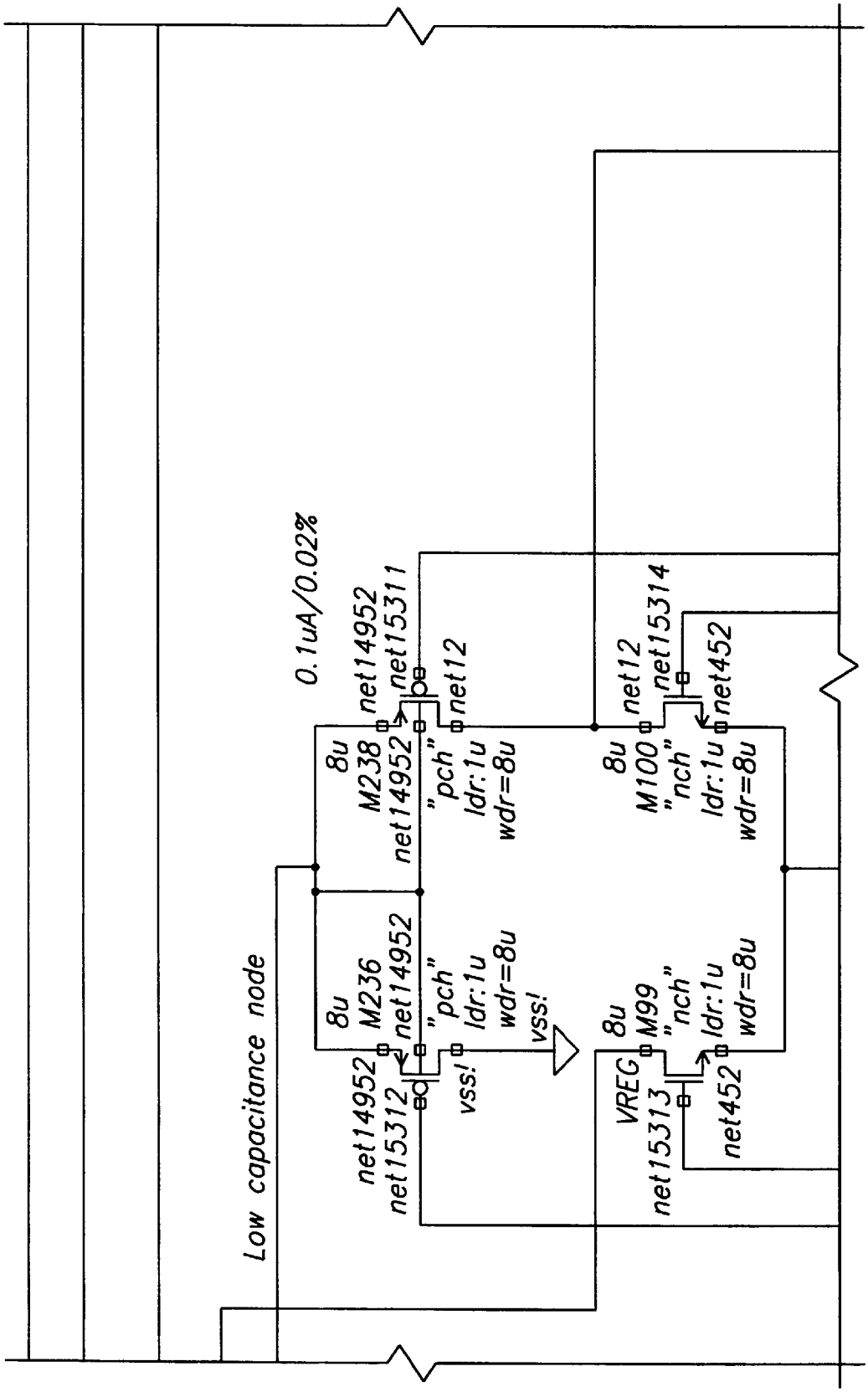

0.1uA/0.02%
Low capacitance node
8u
M238
net14952
"pch"
ldr:1u
wdr=8u
net14952
net15311
net12
8u
M236
net14952
"pch"
ldr:1u
wdr=8u
vss!
net14952
net15312
vss!
8u
M100
"nch"
ldr:1u
wdr=8u
net12
net15314
net452
8u
M99
"nch"
ldr:1u
wdr=8u
VREG
net15313
net452

FIG 8.0504AC

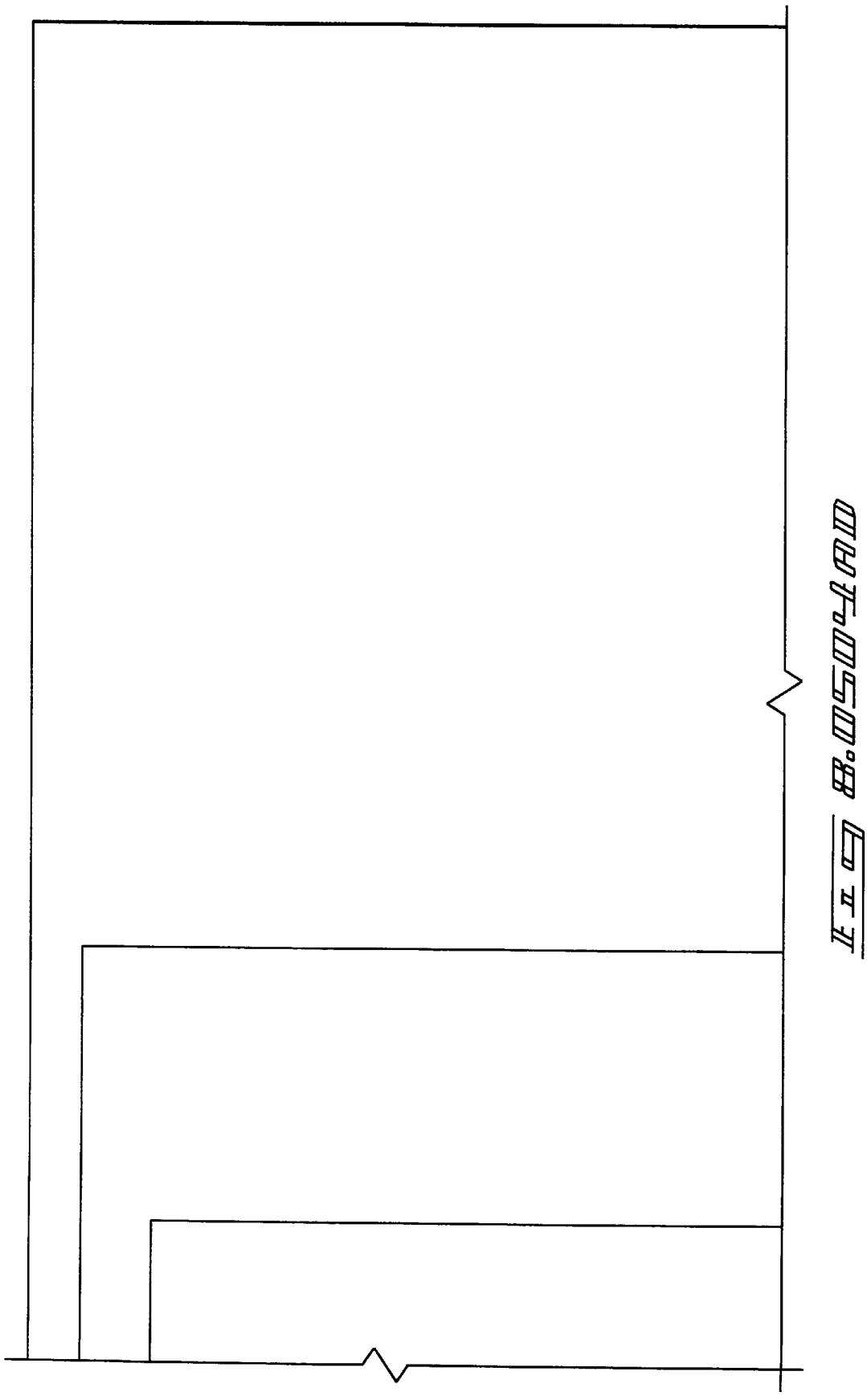


FIG 8,0504AM

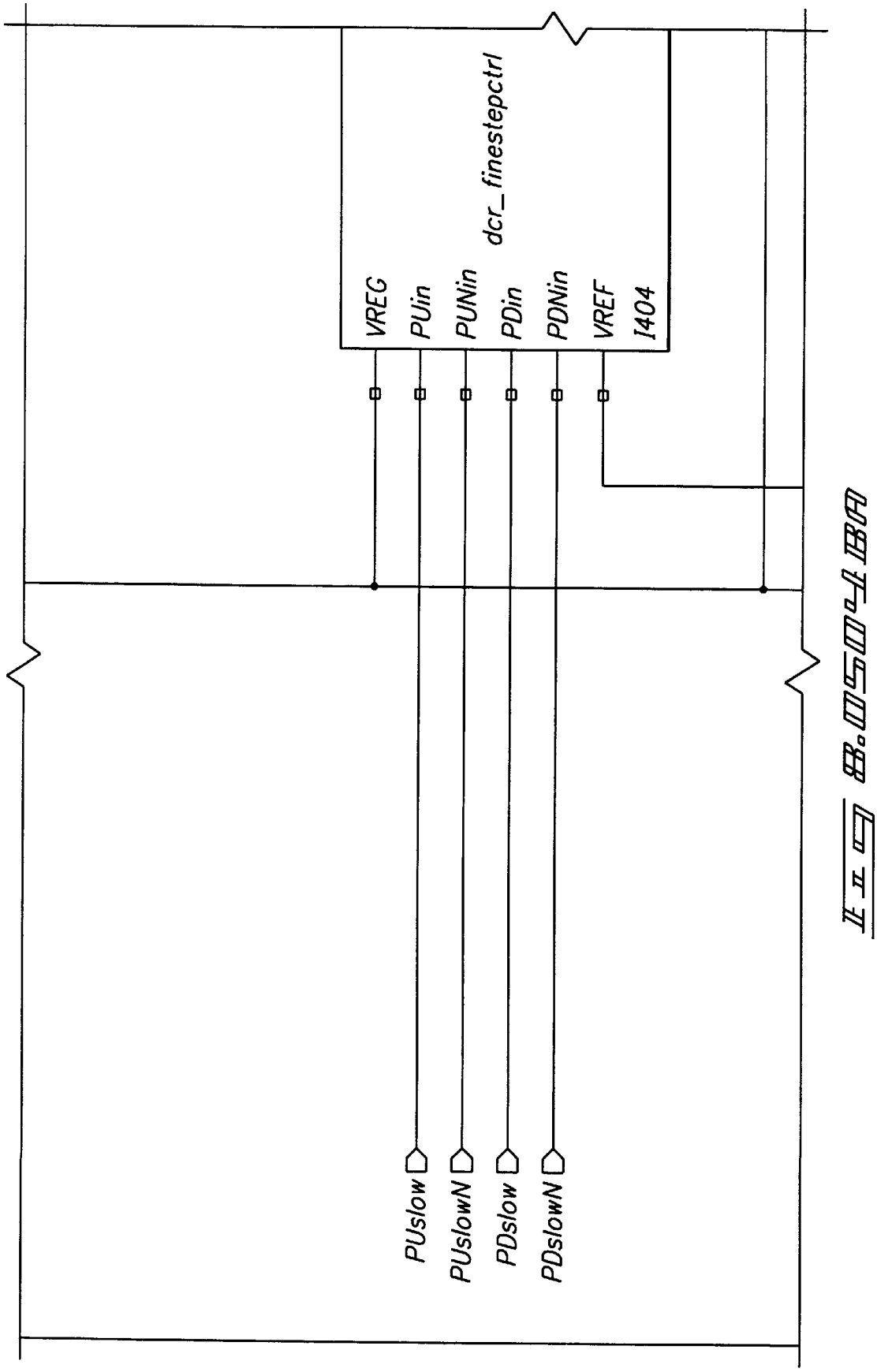


Fig 1404.00.6,130,602

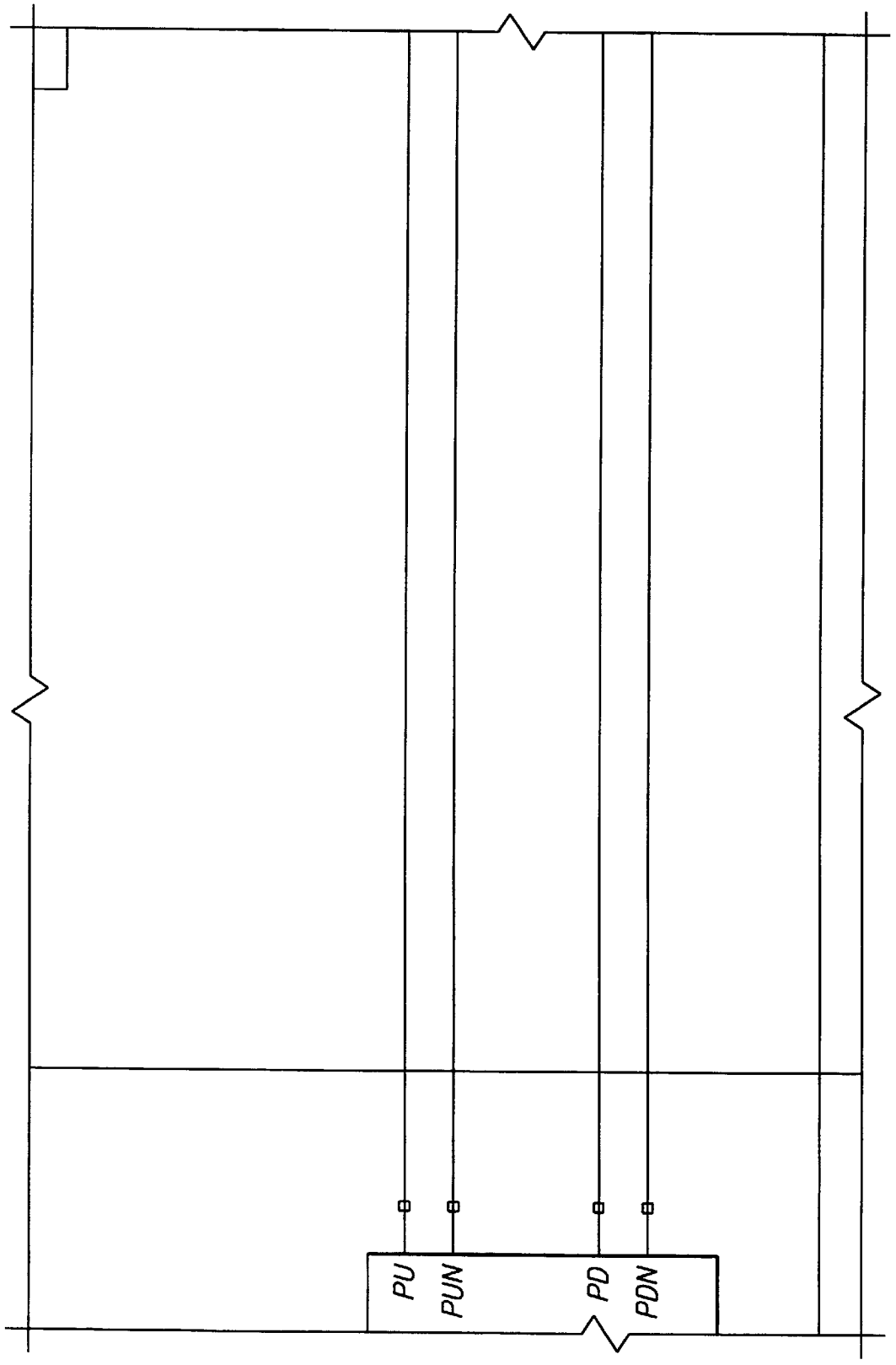
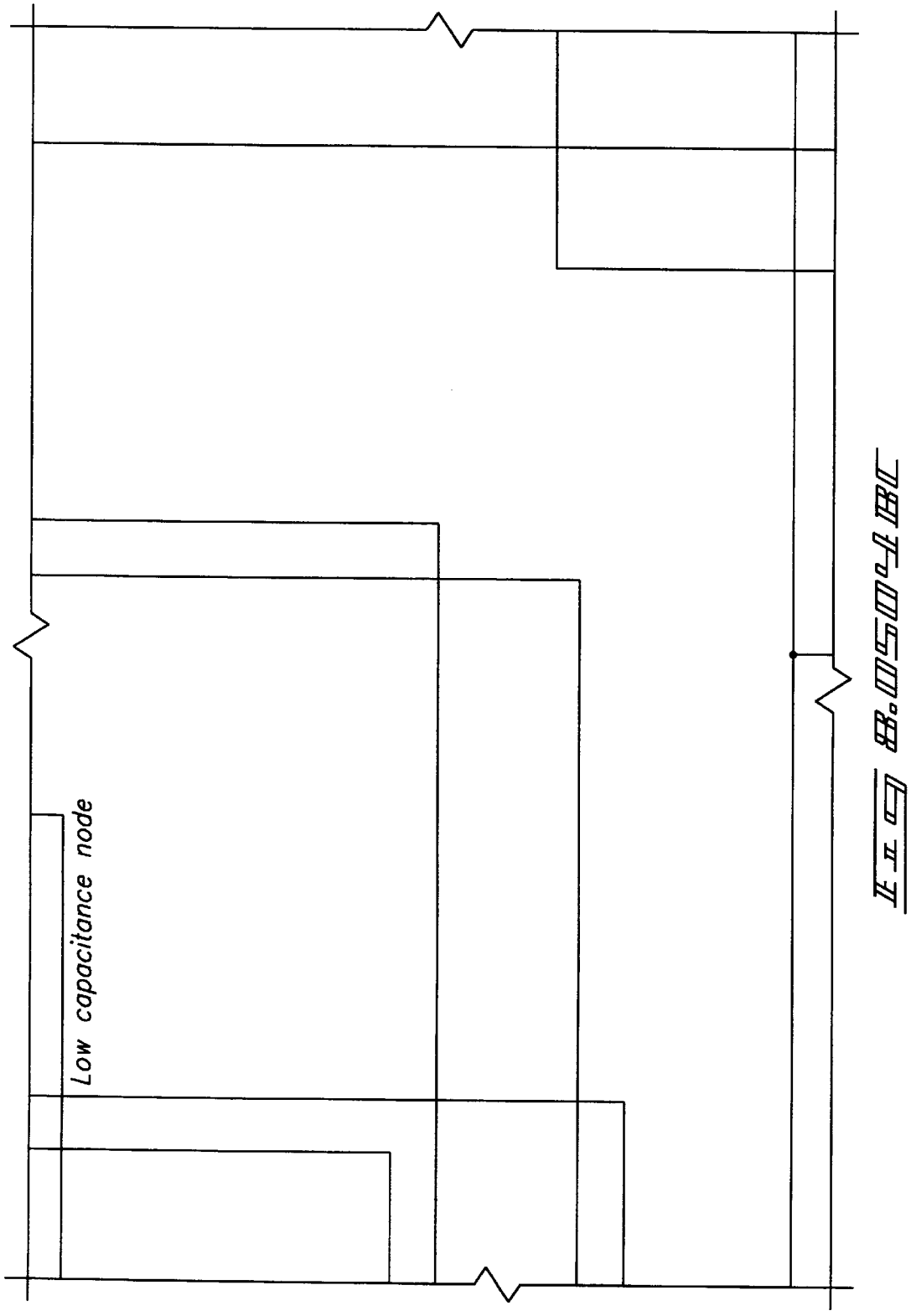


FIG 8,005,888


Low capacitance node
FIG. 88,050

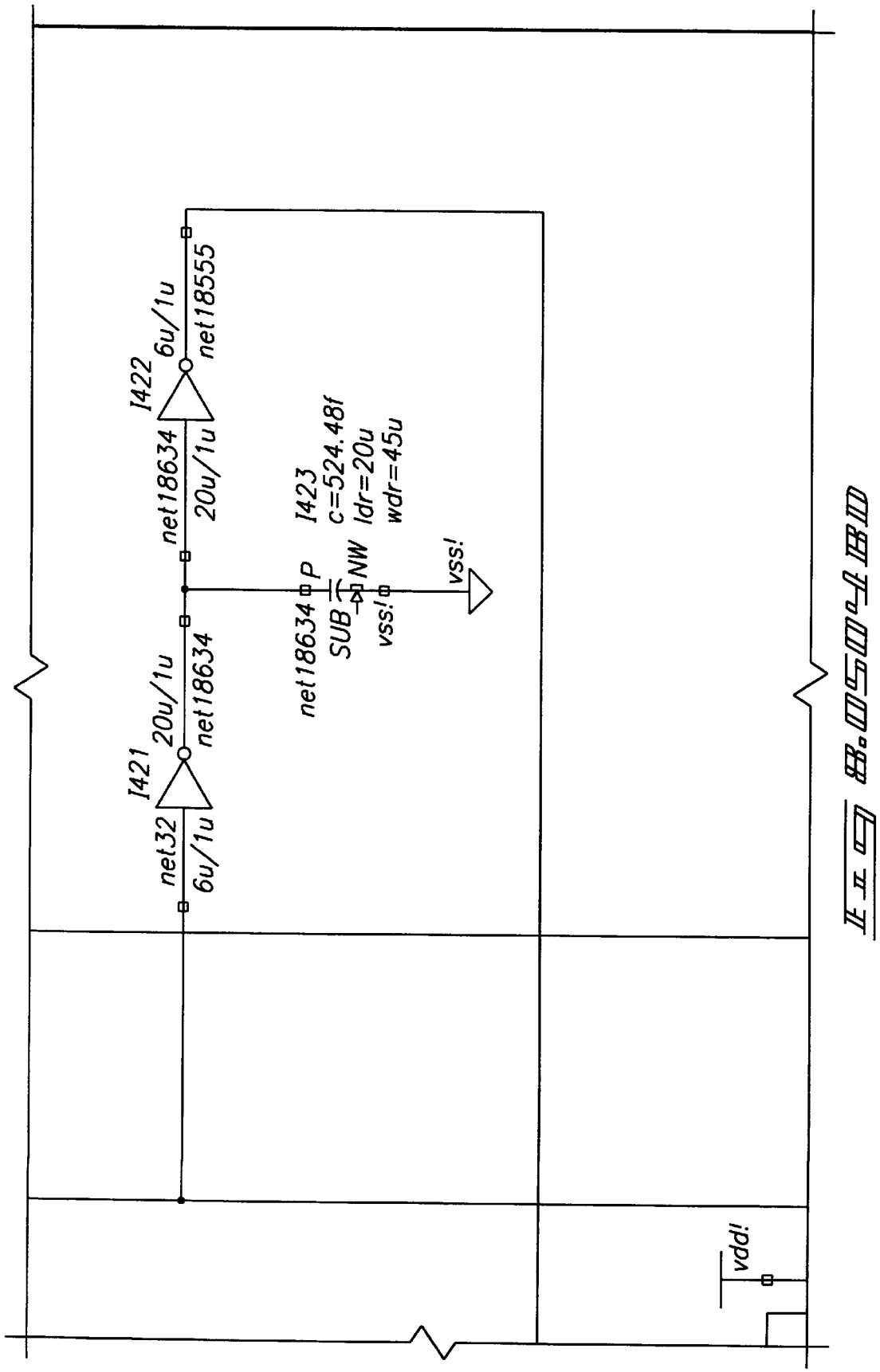

I422
6u/1u
net18555
net18634
20u/1u
I423
c=524.48f
ldr=20u
wdr=45u
net18634
P
SUB
NW
vss!
vss!
I421
20u/1u
net18634
net32
6u/1u
vdd!

FIG 8,005,000

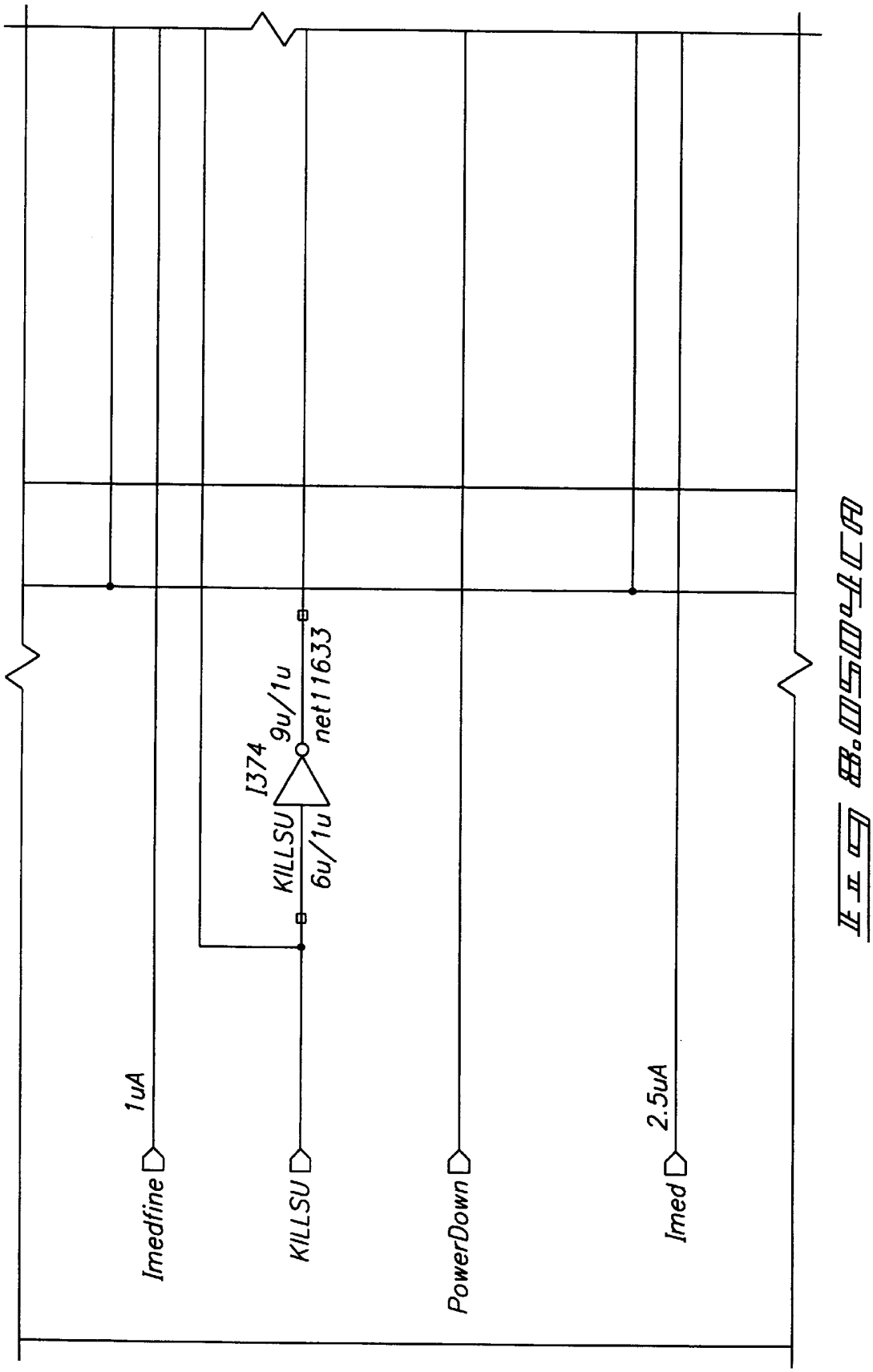

1uA
Imedfine
I374
9u/1u
net11633
KILLSU
6u/1u
KILLSU
PowerDown
2.5uA
Imed

FIG 88.005A

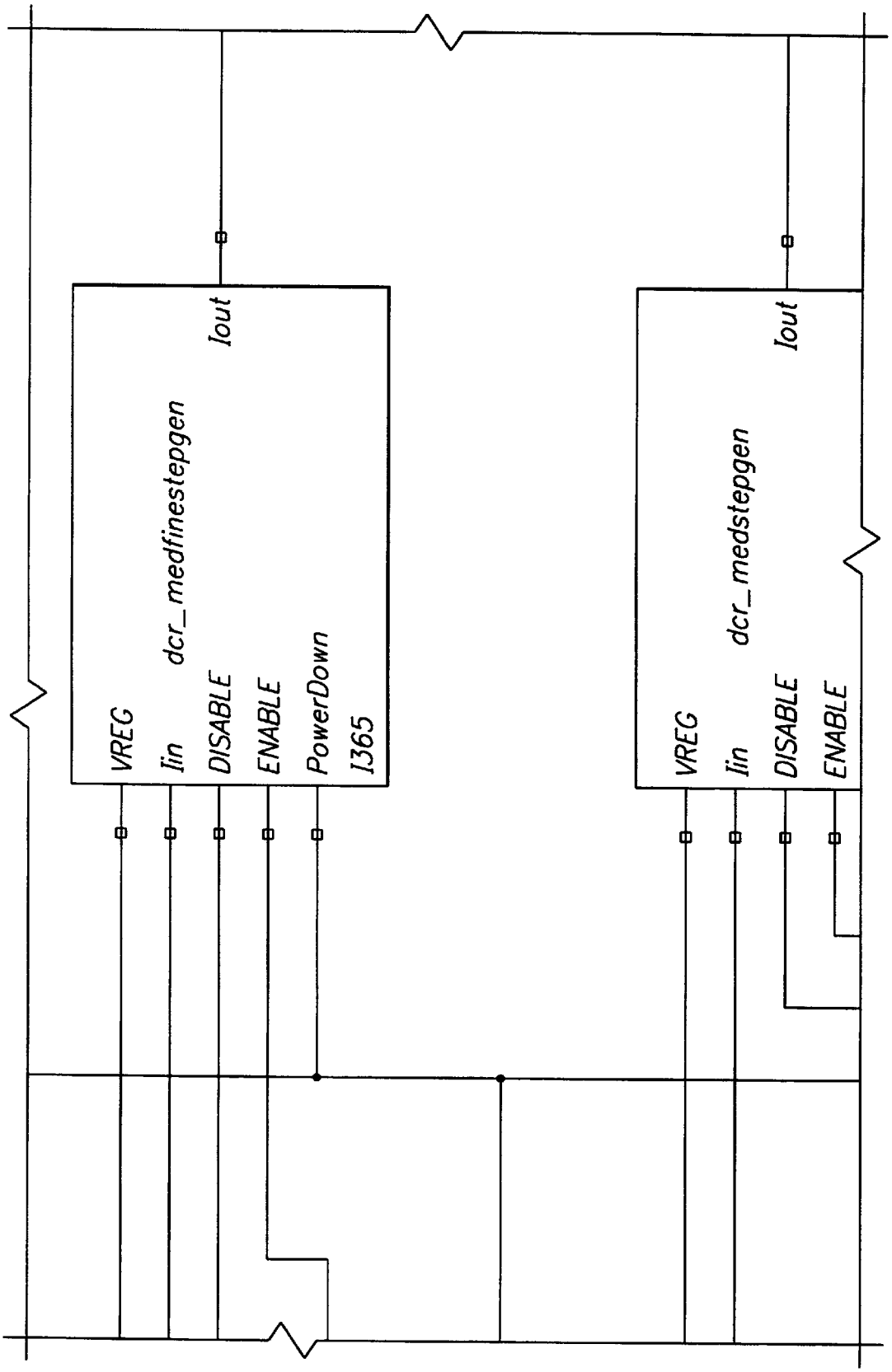

dcr_medfinestepgen
VREG
Iin
DISABLE
ENABLE
PowerDown
I365
Iout
dcr_medstepgen
VREG
Iin
DISABLE
ENABLE
Iout

FIG 88.0504B

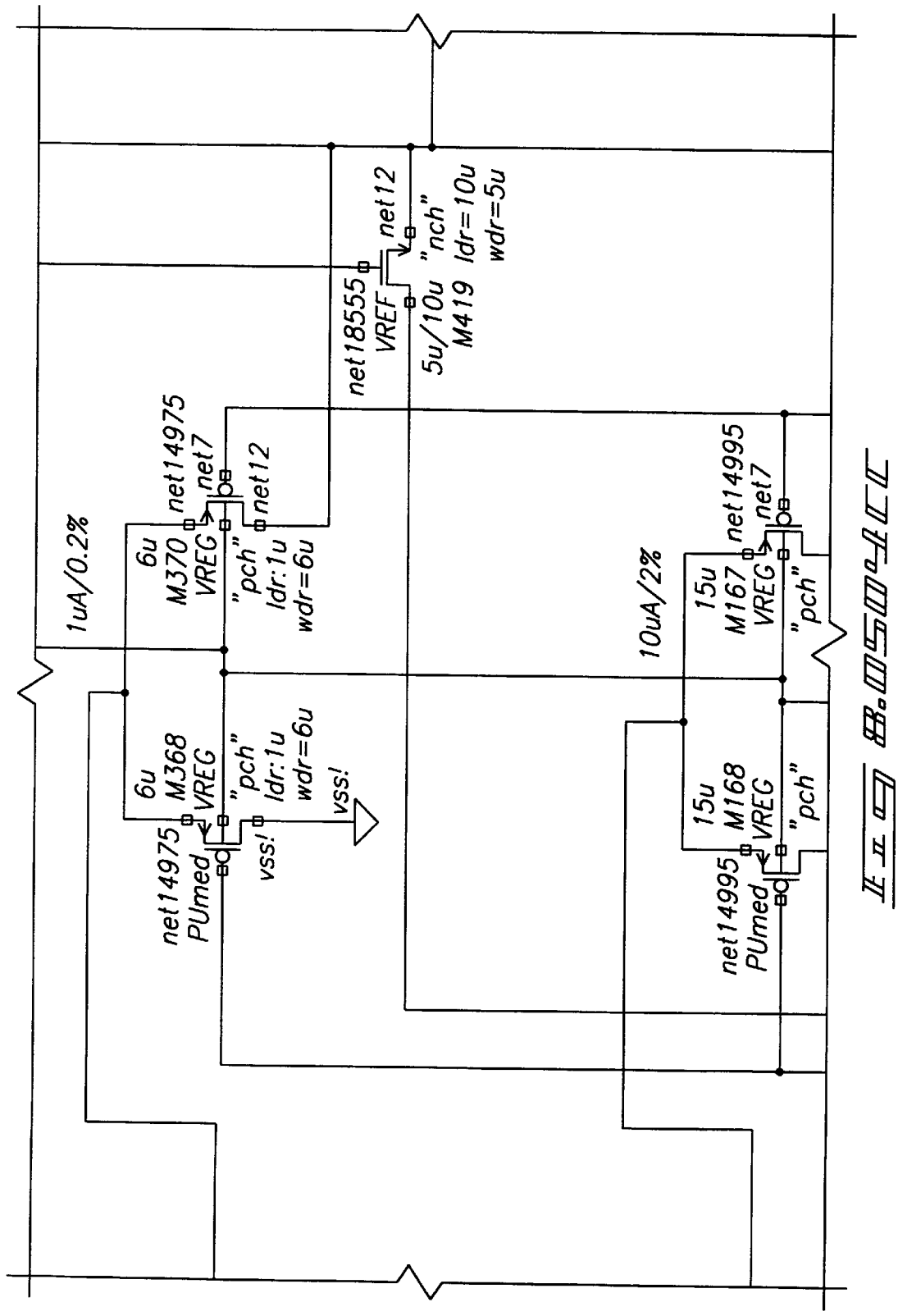

net12
"nch"
ldr=10u
wdr=5u
net18555
VREF
5u/10u
M419
net14975
net7
net12
6u
M370
VREG
"pch"
ldr:1u
wdr=6u
1uA/0.2%
net14995
net7
10uA/2%
15u
M167
VREG
"pch"
6u
M368
VREG
"pch"
ldr:1u
wdr=6u
vss!
net14975
PUmed
vss!
15u
M168
VREG
"pch"
net14995
PUmed

FIG. 8.0504

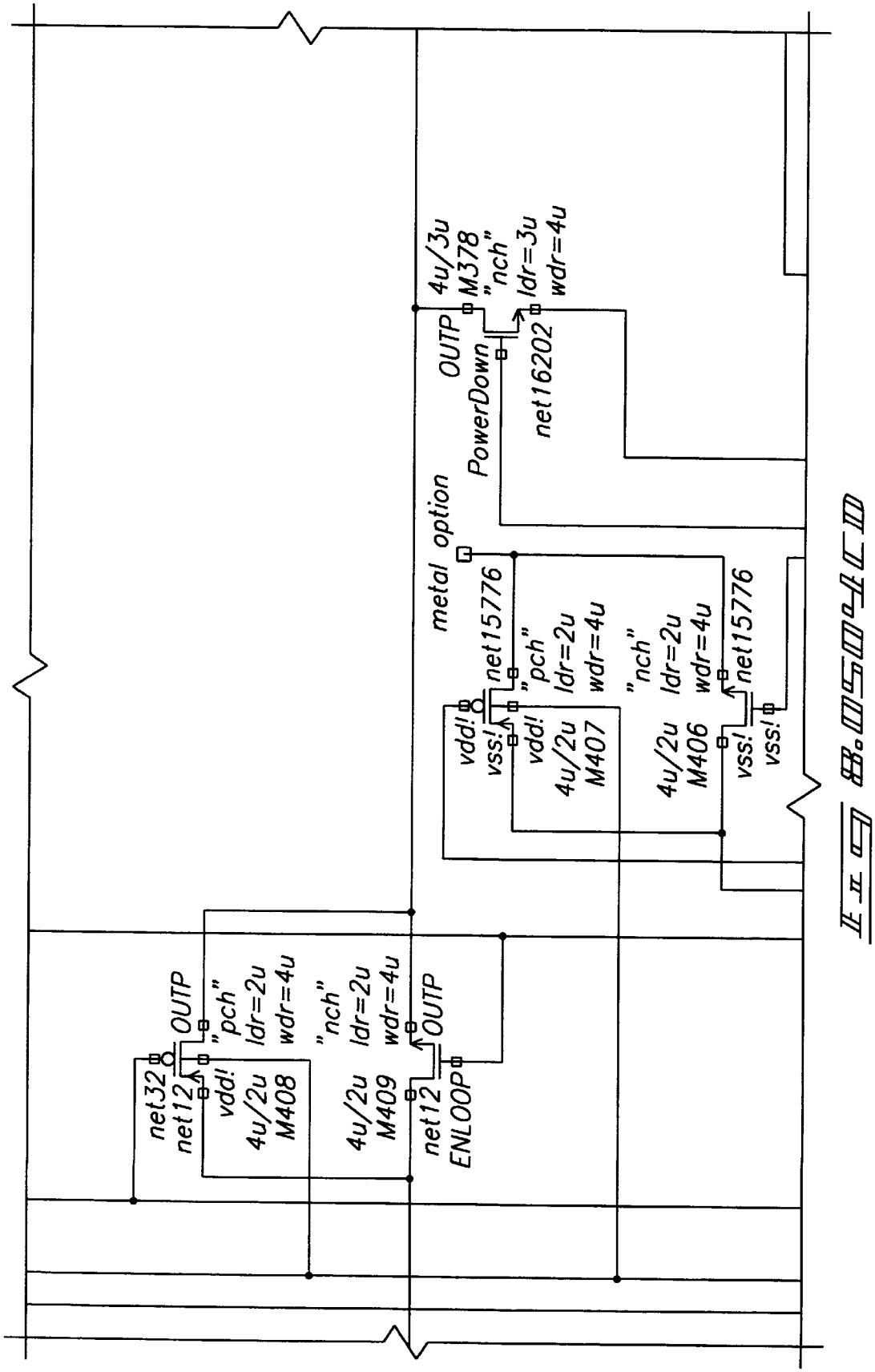

4u/3u
M378
"nch"
ldr=3u
wdr=4u
OUTP
PowerDown
net16202
metal option
net15776
"pch"
ldr=2u
wdr=4u
vdd!
vss!
4u/2u
M407
"nch"
ldr=2u
wdr=4u
4u/2u
M406
net15776
vss!
net32
net12
vdd!
4u/2u
M408
"pch"
ldr=2u
wdr=4u
OUTP
"nch"
ldr=2u
wdr=4u
4u/2u
M409
net12
ENLOOP
OUTP

FIG 88.00578

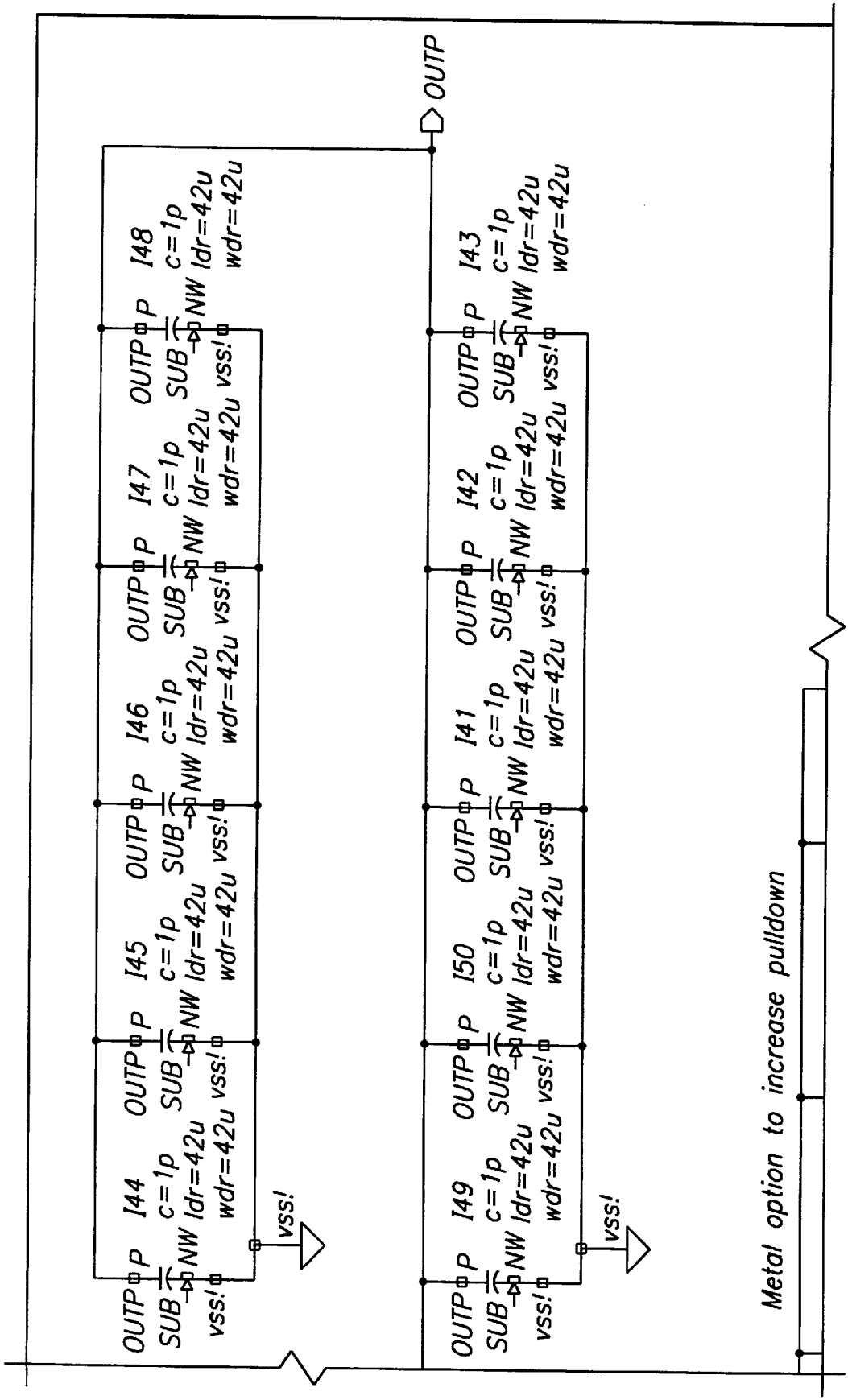
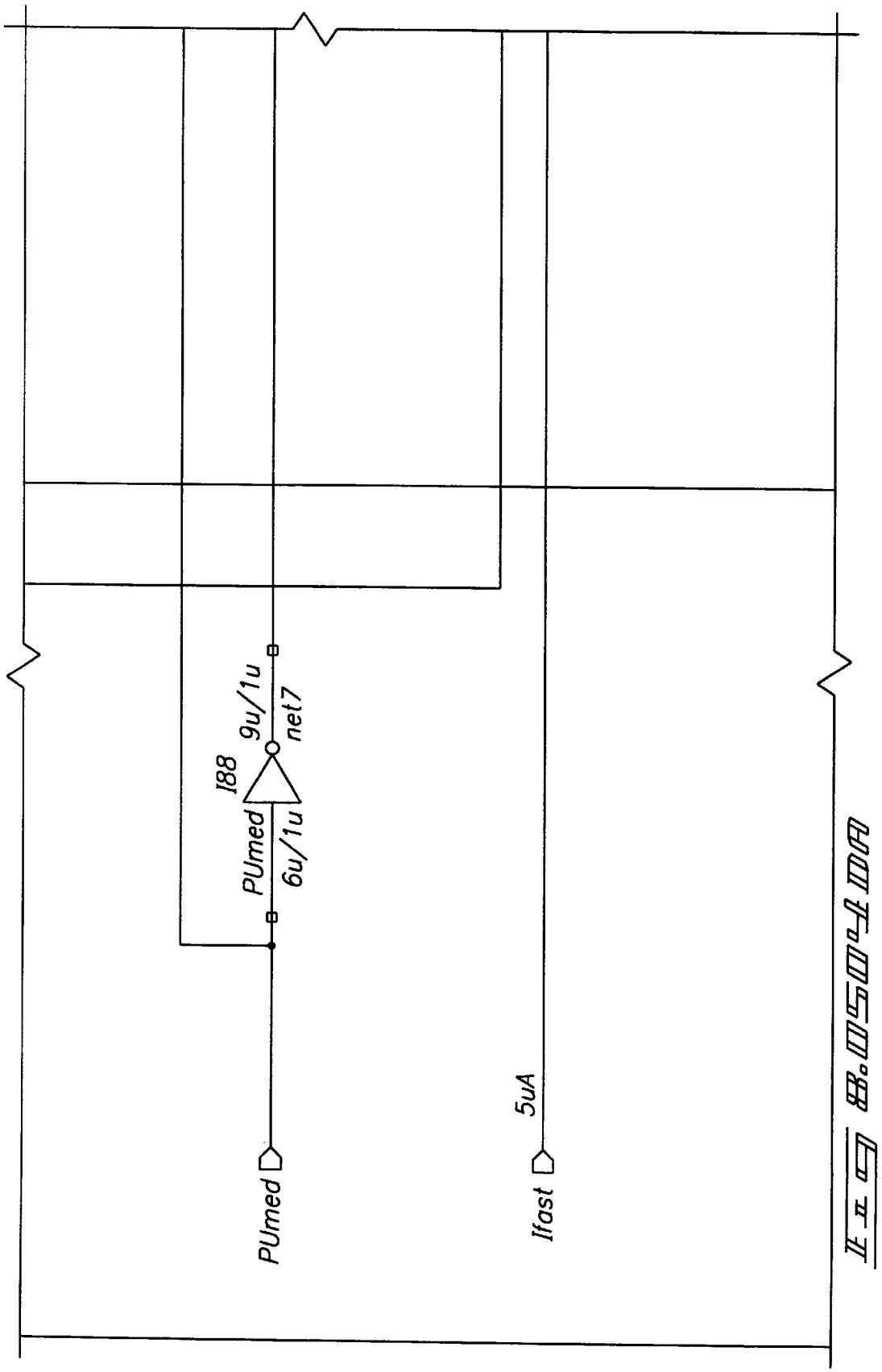
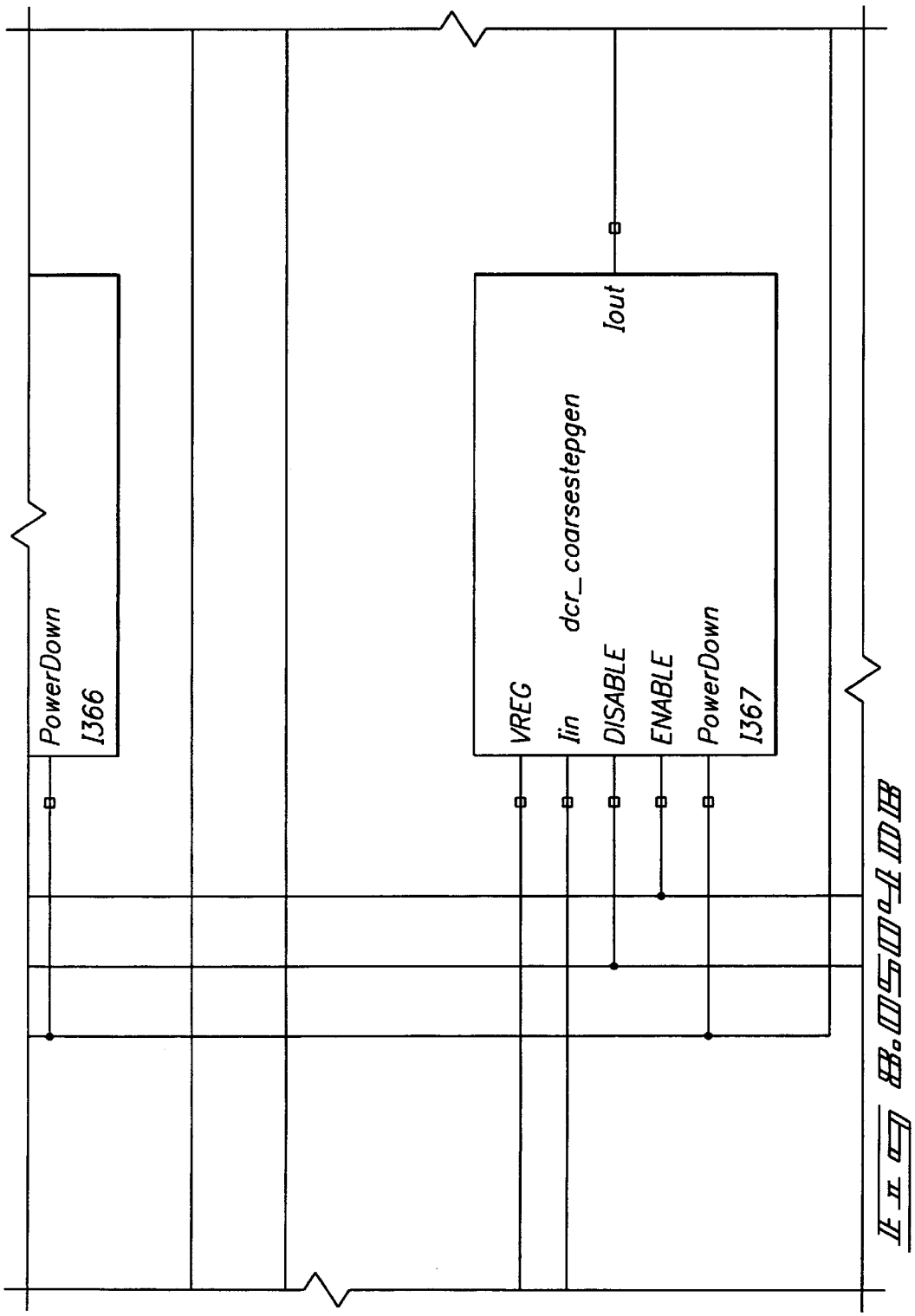

OUTP
I44 c=1p ldr=42u wdr=42u
I45 c=1p ldr=42u wdr=42u
I46 c=1p ldr=42u wdr=42u
I47 c=1p ldr=42u wdr=42u
I48 c=1p ldr=42u wdr=42u
I49 c=1p ldr=42u wdr=42u
I50 c=1p ldr=42u wdr=42u
I41 c=1p ldr=42u wdr=42u
I42 c=1p ldr=42u wdr=42u
I43 c=1p ldr=42u wdr=42u
OUTP
SUB
NW
P
vss!
Metal option to increase pulldown

FIG 88.0050


I88
9u/1u
net7
PUmed
6u/1u
PUmed
5uA
Ifast
VDD tpdn50 8.050 FIG 51


PowerDown
I366
dcr_coarsestepgen
Iout
VREG
Iin
DISABLE
ENABLE
PowerDown
I367
FIG 8,050,338

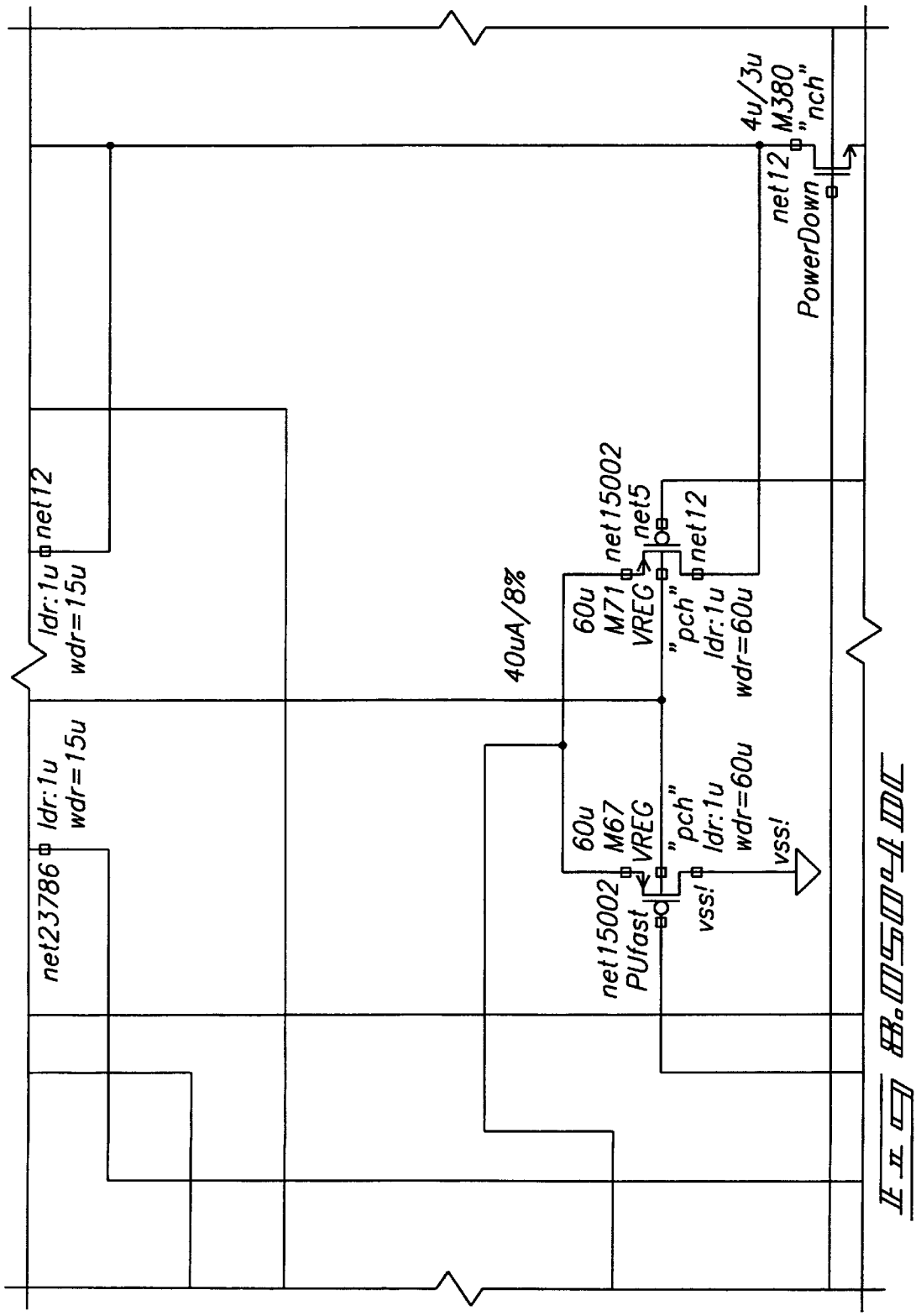

4u/3u
M380
"nch"
net12
PowerDown
net12
ldr:1u
wdr=15u
40uA/8%
60u
M71
VREG
net15002
net5
"pch"
ldr:1u
wdr=60u
net12
ldr:1u
wdr=15u
net23786
60u
M67
VREG
net15002
PUfast
"pch"
ldr:1u
wdr=60u
vss!
vss!

FIG. 8,05,00

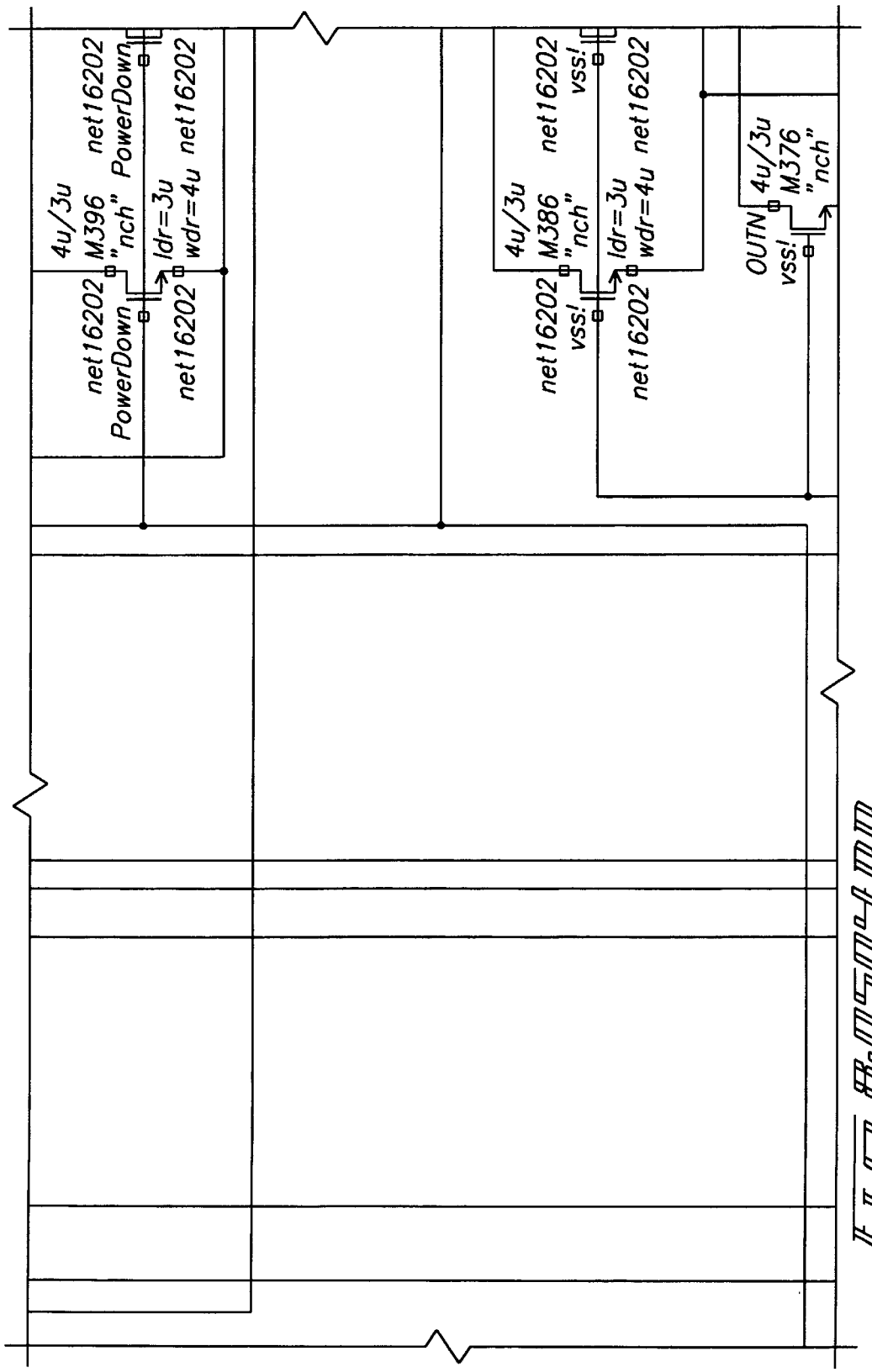
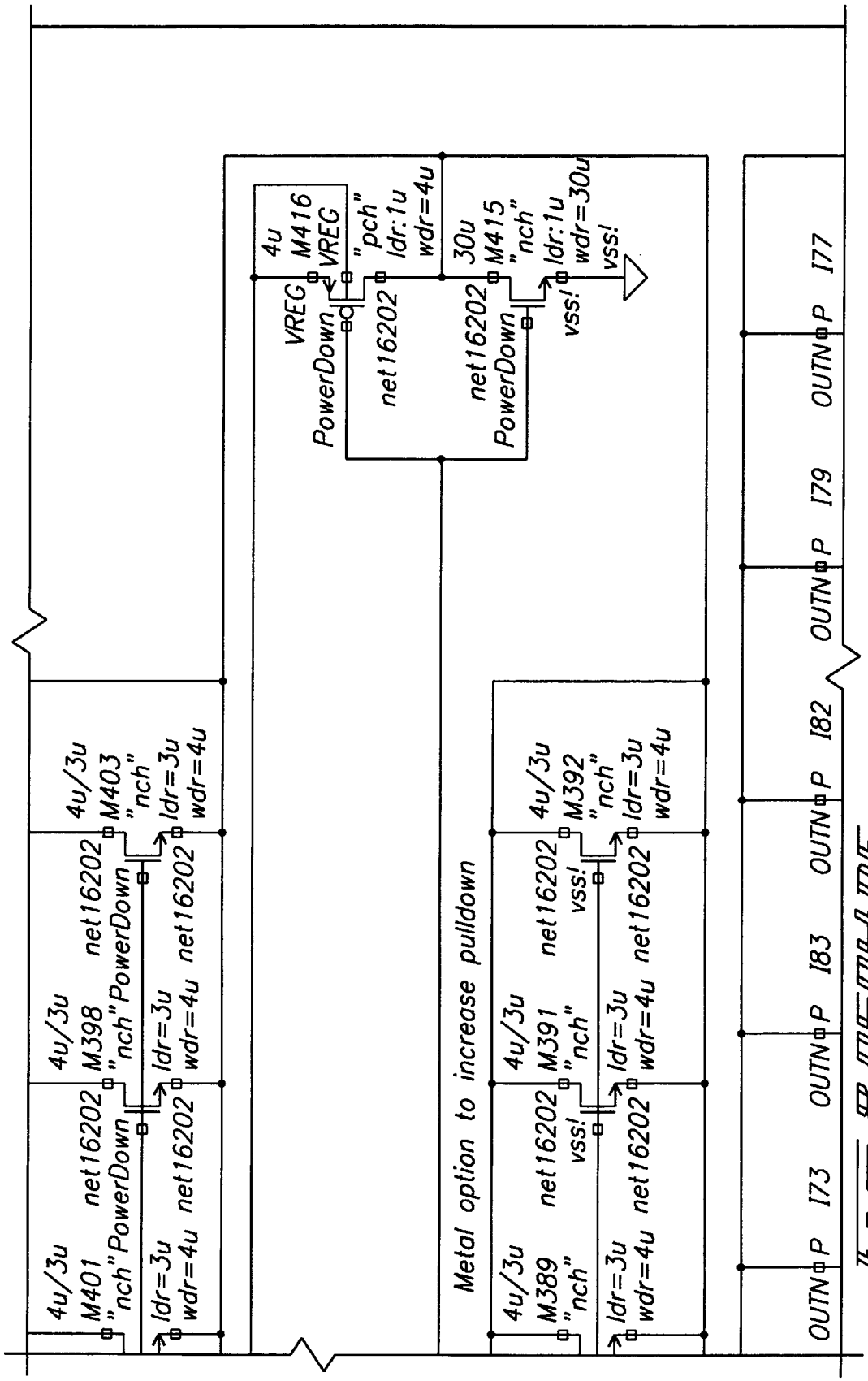
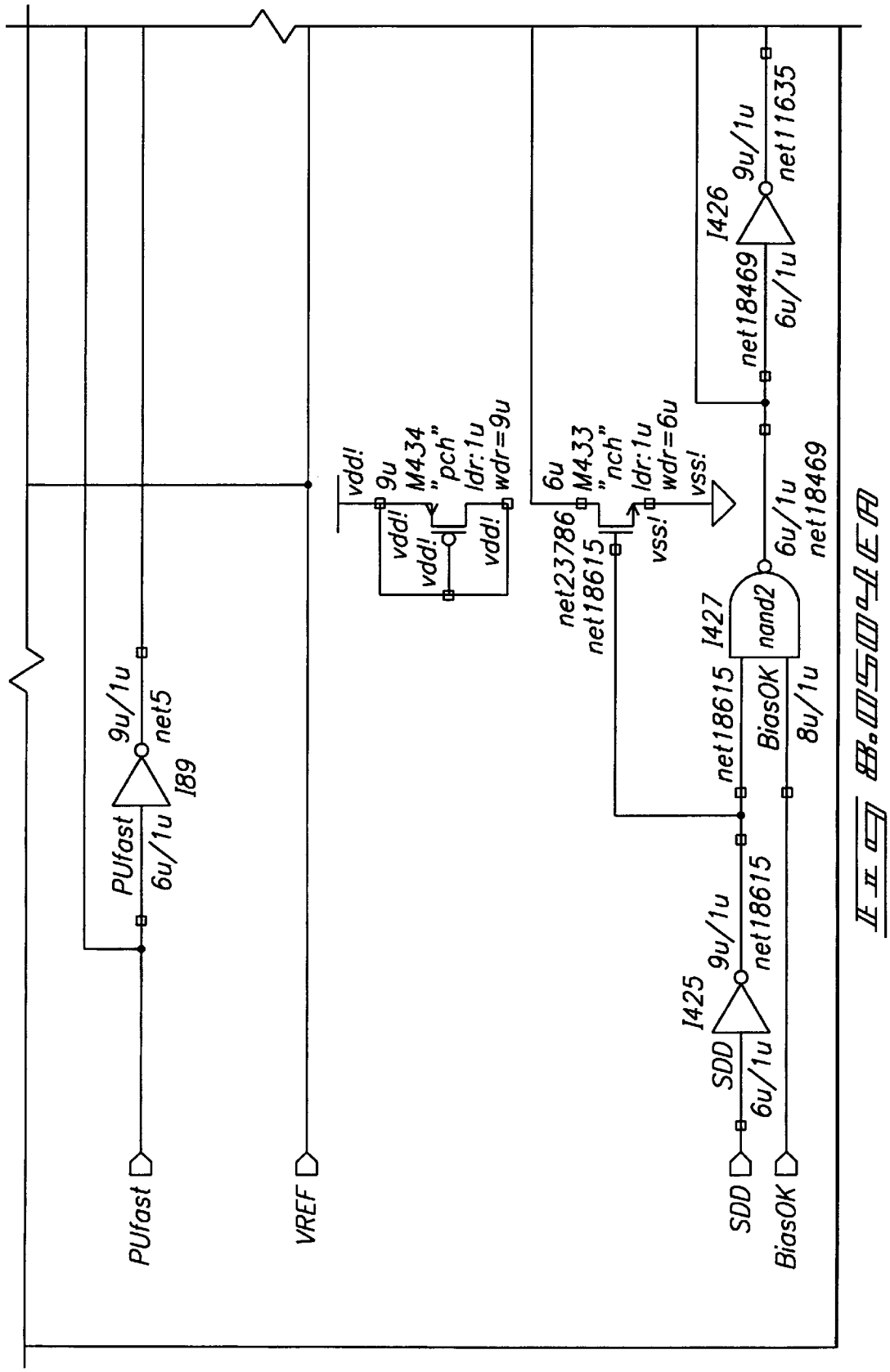

4u/3u
M396
"nch"
ldr=3u
wdr=4u
net16202
PowerDown
net16202
PowerDown
net16202
net16202
4u/3u
M386
"nch"
ldr=3u
wdr=4u
net16202
vss!
net16202
vss!
net16202
OUTN
4u/3u
M376
"nch"
vss!

FIG 8.0570


4u/3u
M401
"nch"
PowerDown
net16202
ldr=3u
wdr=4u
4u/3u
M398
"nch"
PowerDown
net16202
ldr=3u
wdr=4u
4u/3u
M403
"nch"
net16202
ldr=3u
wdr=4u
4u
M416
VREG
"pch"
ldr:1u
wdr=4u
VREG
PowerDown
net16202
30u
M415
"nch"
ldr:1u
wdr=30u
vss!
net16202
PowerDown
vss!
Metal option to increase pulldown
4u/3u
M389
"nch"
net16202
ldr=3u
wdr=4u
4u/3u
M391
"nch"
vss!
net16202
ldr=3u
wdr=4u
4u/3u
M392
"nch"
vss!
net16202
ldr=3u
wdr=4u
OUTN
P
I73
OUTN
P
I83
OUTN
P
I82
OUTN
P
I79
OUTN
P
I77


PUfast
VREF
SDD
BiasOK
I89
I425
I426
I427
nand2
M434
M433
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"nch"
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net5
net18615
net18469
net11635
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6u/1u
8u/1u
6u
9u
ldr:1u
wdr=9u
wdr=6u

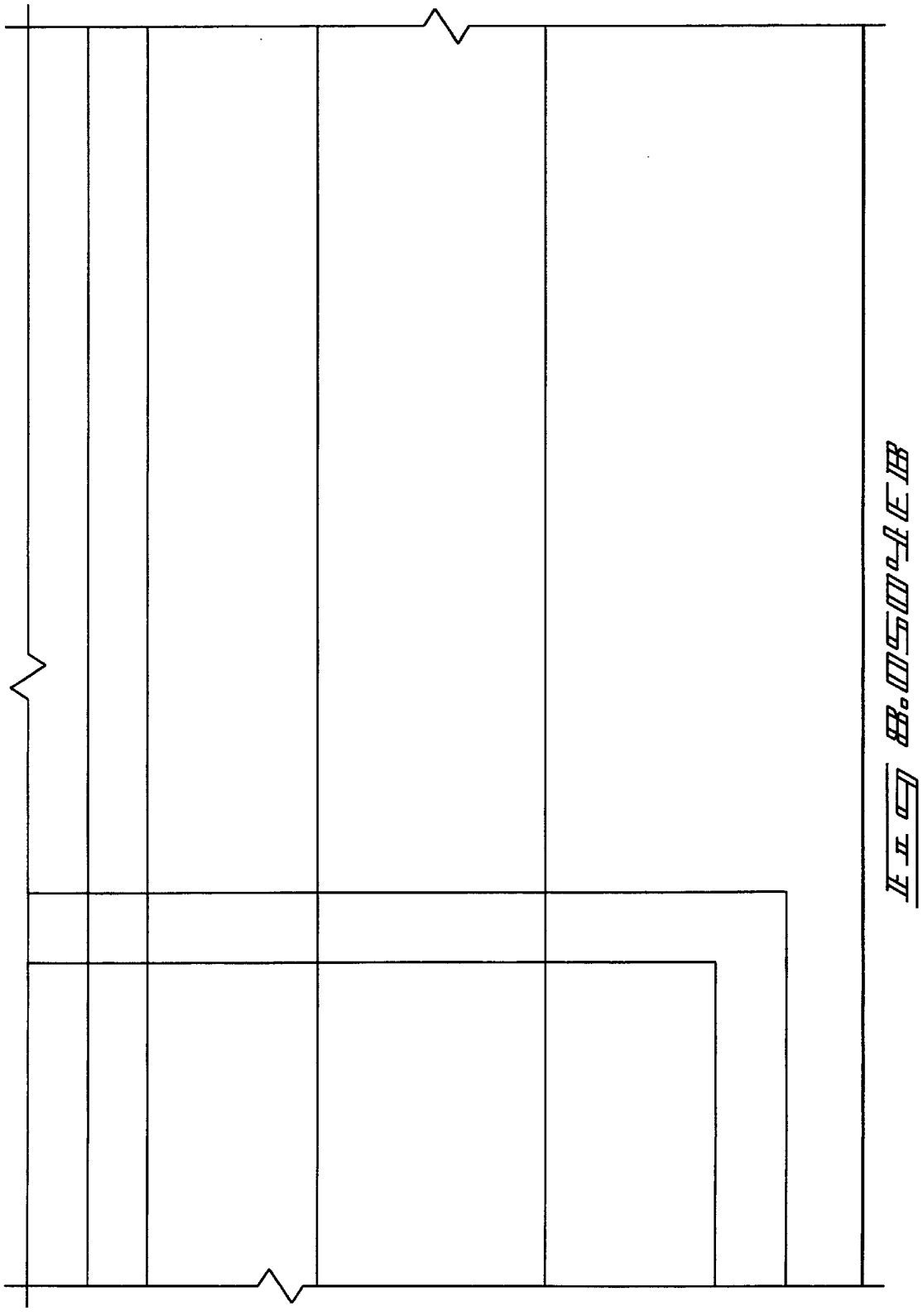
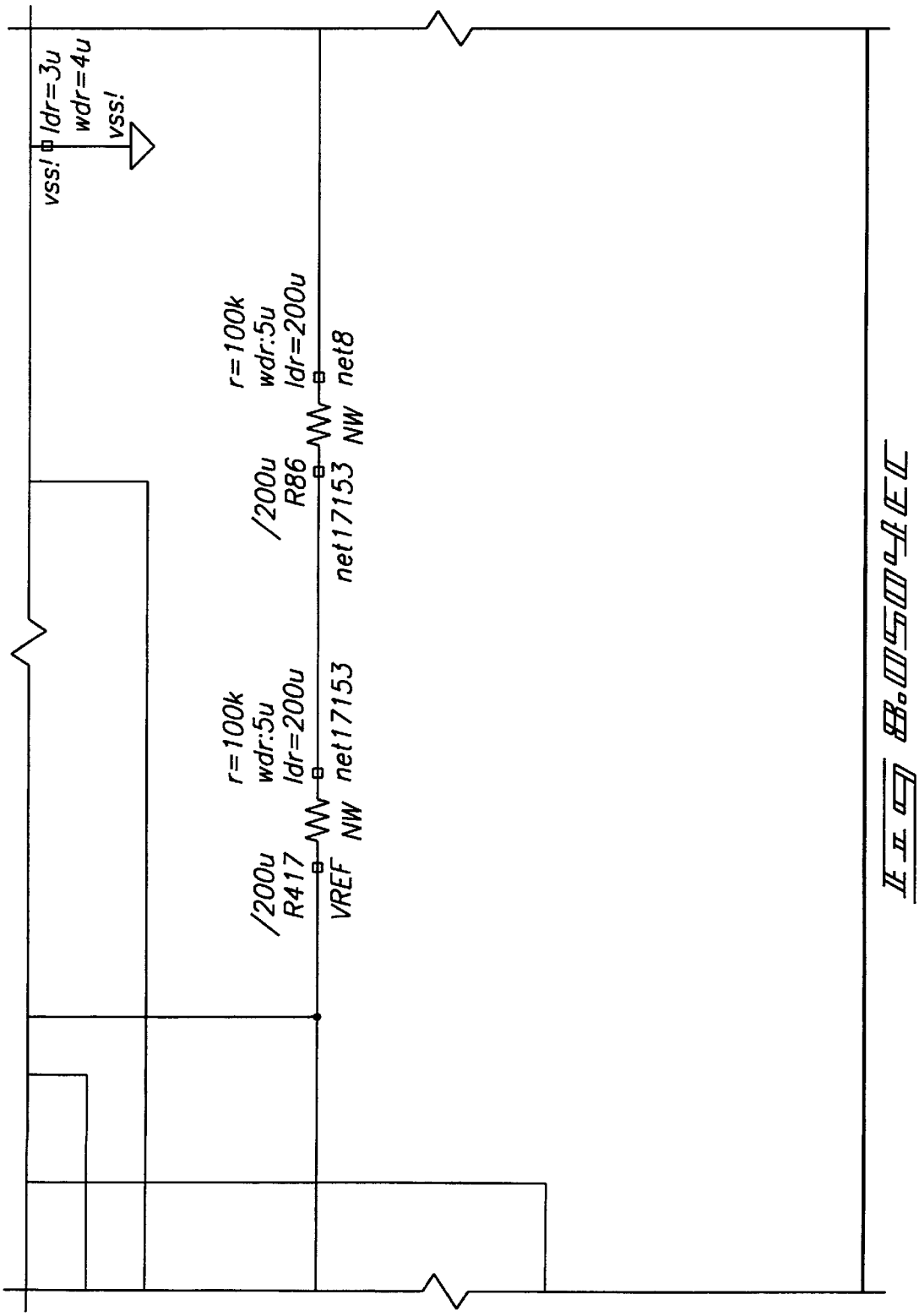


FIG 88,505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wdr=4u
vss!
r=100k
wdr:5u
ldr=200u
net8
/200u
R86
NW
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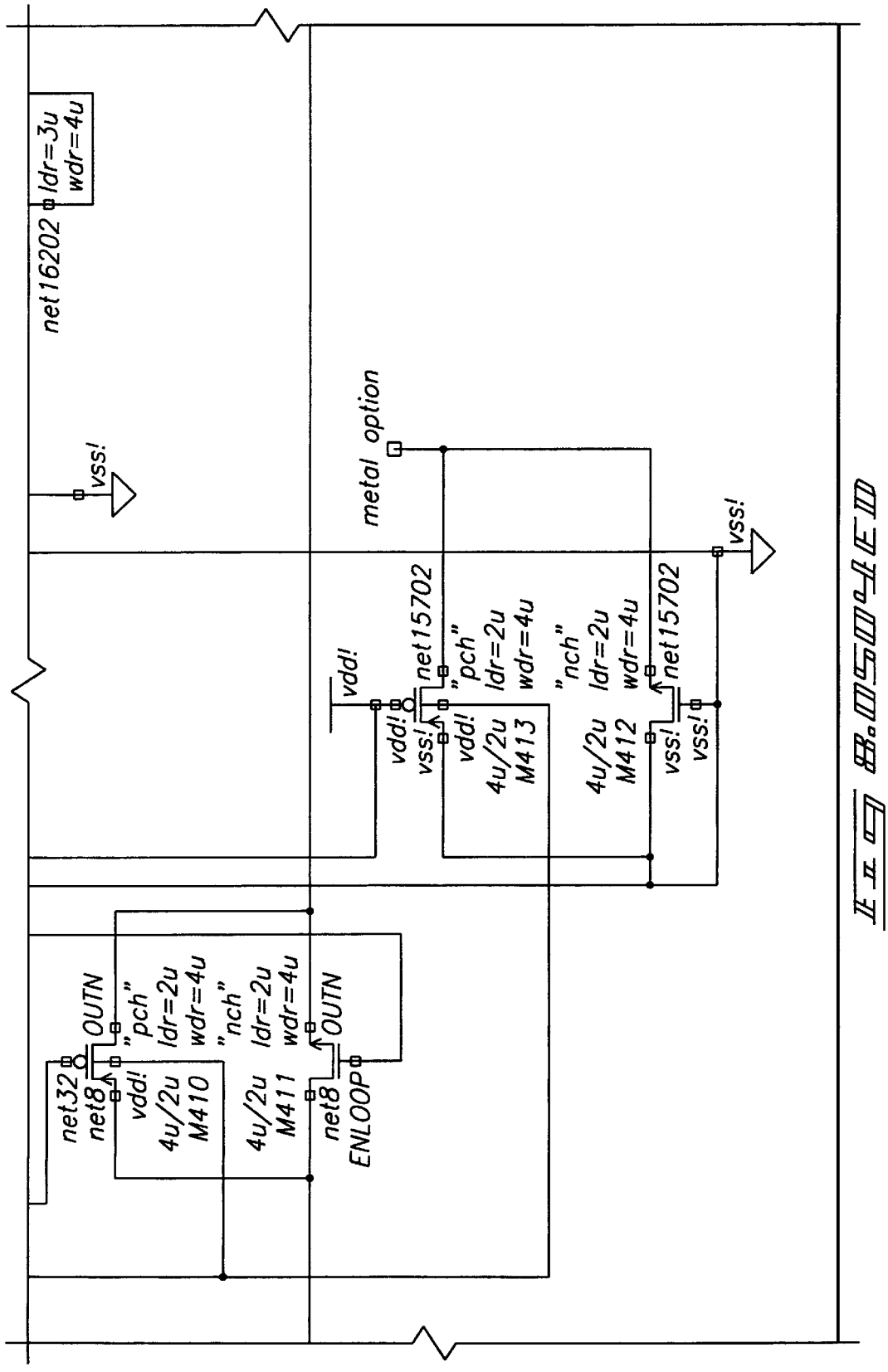
r=100k
wdr:5u
ldr=200u
net17153
/200u
R417
NW
VREF

FIG. 8,054E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vss!
vdd!
net15702
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ldr=2u
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"nch"
ldr=2u
wdr=4u
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vss!
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M412
vss!
vss!
net32
net8
OUTN
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ldr=2u
wdr=4u
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FIG. 88,005

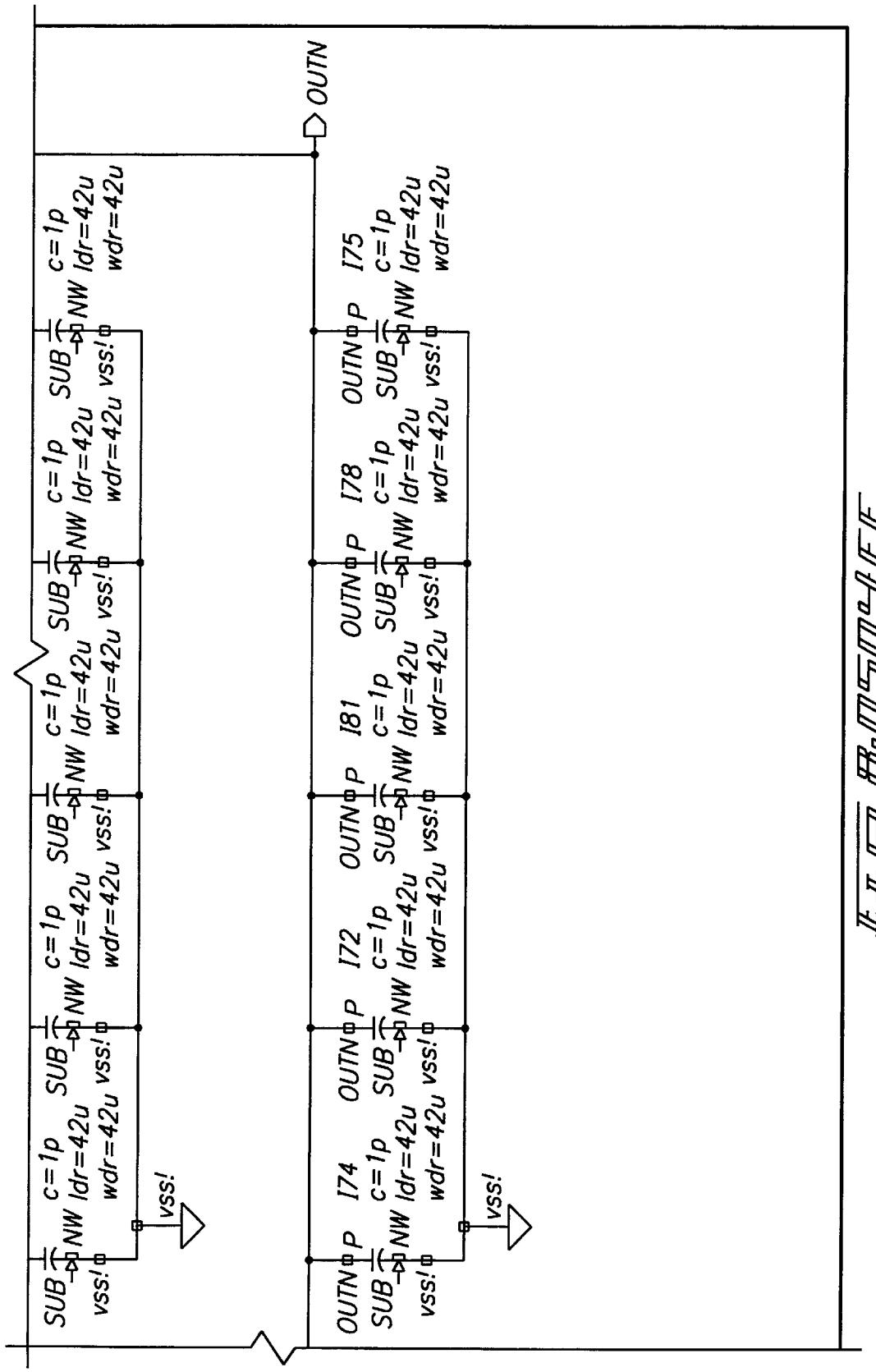


FIG. 8,054E

8.050401AA	8.050401AB	8.050401AC	8.050401AD	8.050401AE	8.050401AF	8.050401AG	8.050401AH	8.050401AI	8.050401AJ
8.050401BA	8.050401BB	8.050401BC	8.050401BD	8.050401BE	8.050401BF	8.050401BG	8.050401BH	8.050401BI	8.050401BJ
8.050401CA	8.050401CB	8.050401CC	8.050401CD	8.050401CE	8.050401CF	8.050401CG	8.050401CH	8.050401CI	8.050401CJ

FIG. 8.050401

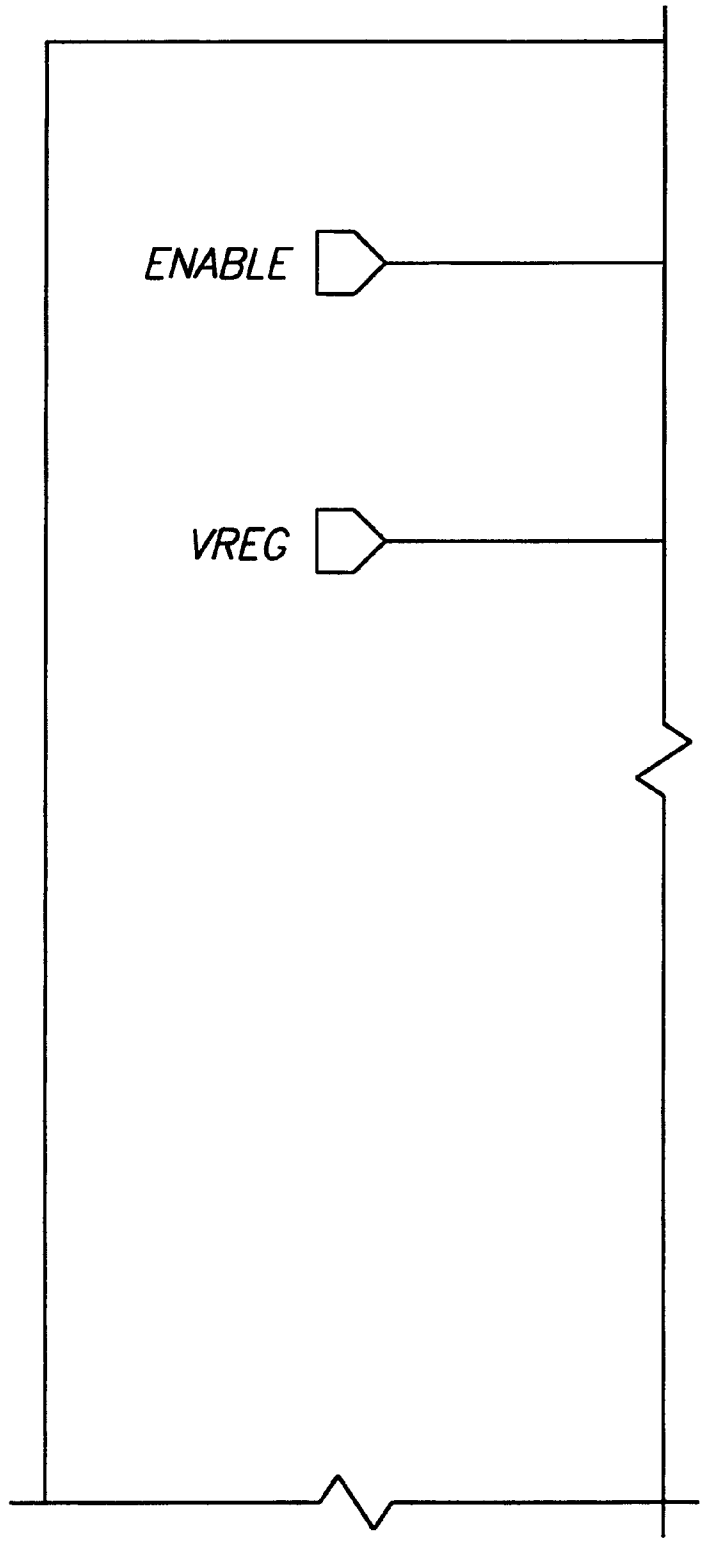


FIG 8.0504.01AA

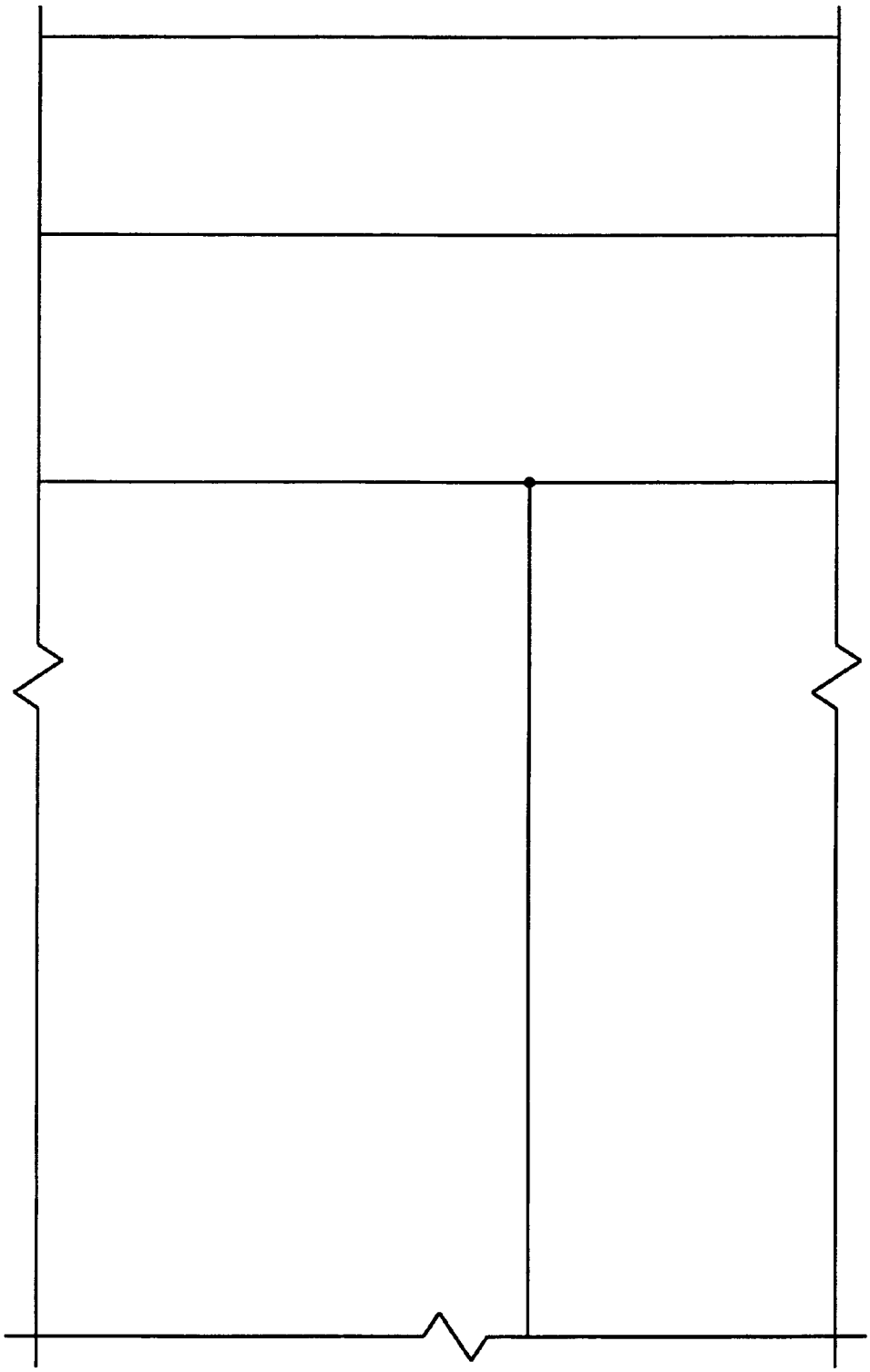


Fig 8.0504.01AB

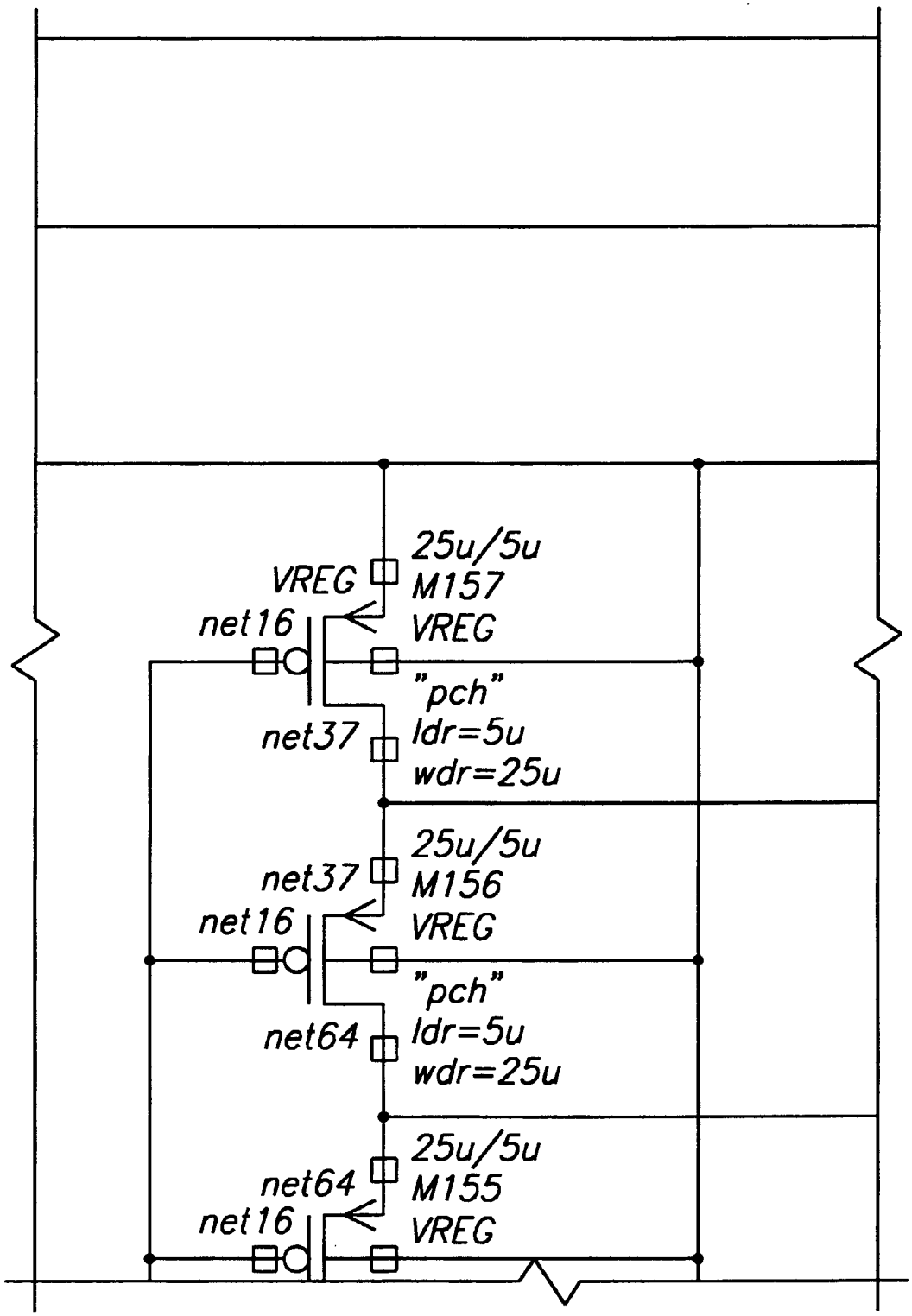


FIG 88.0050401AC

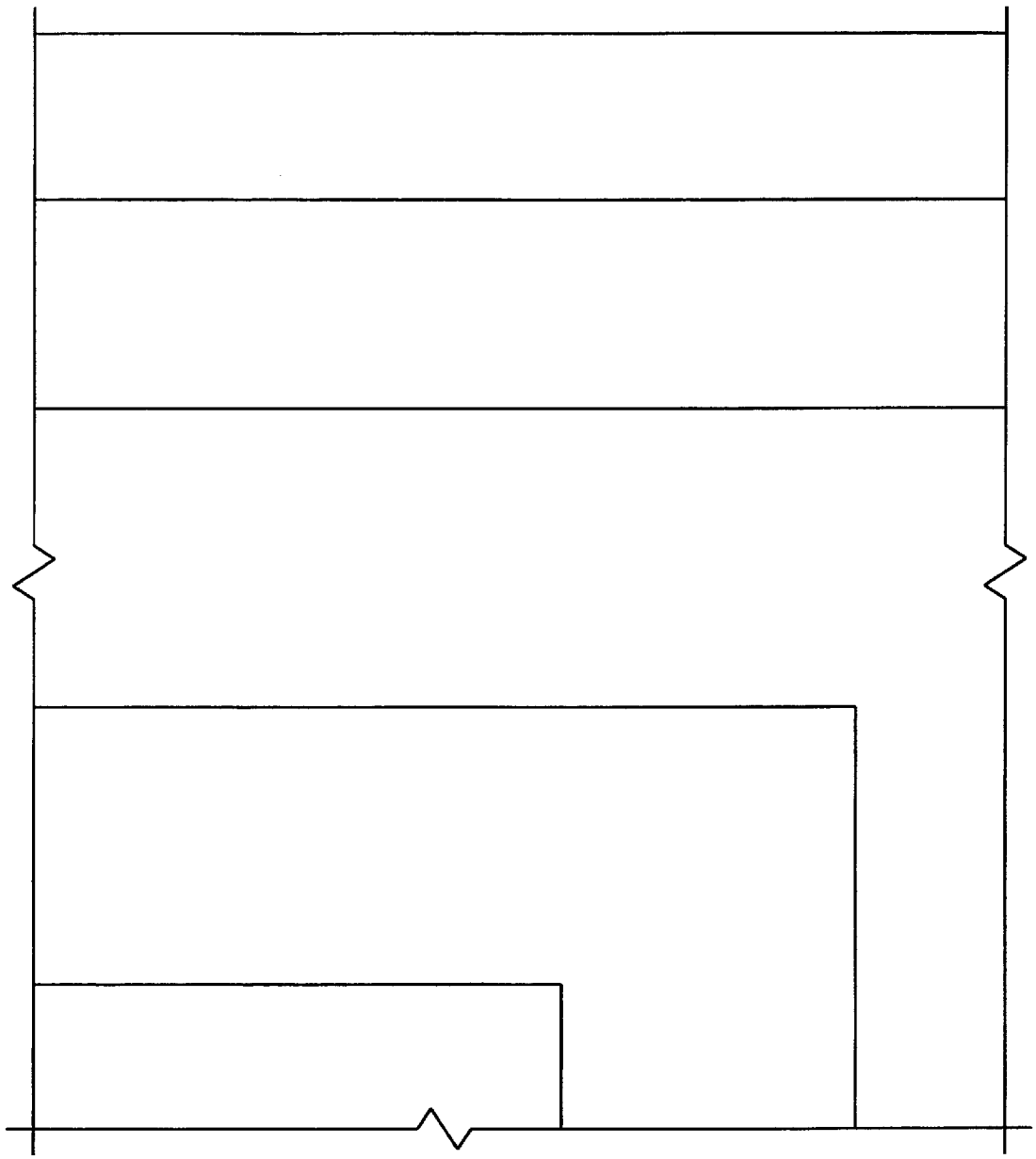


Fig 8.0504AD1AD

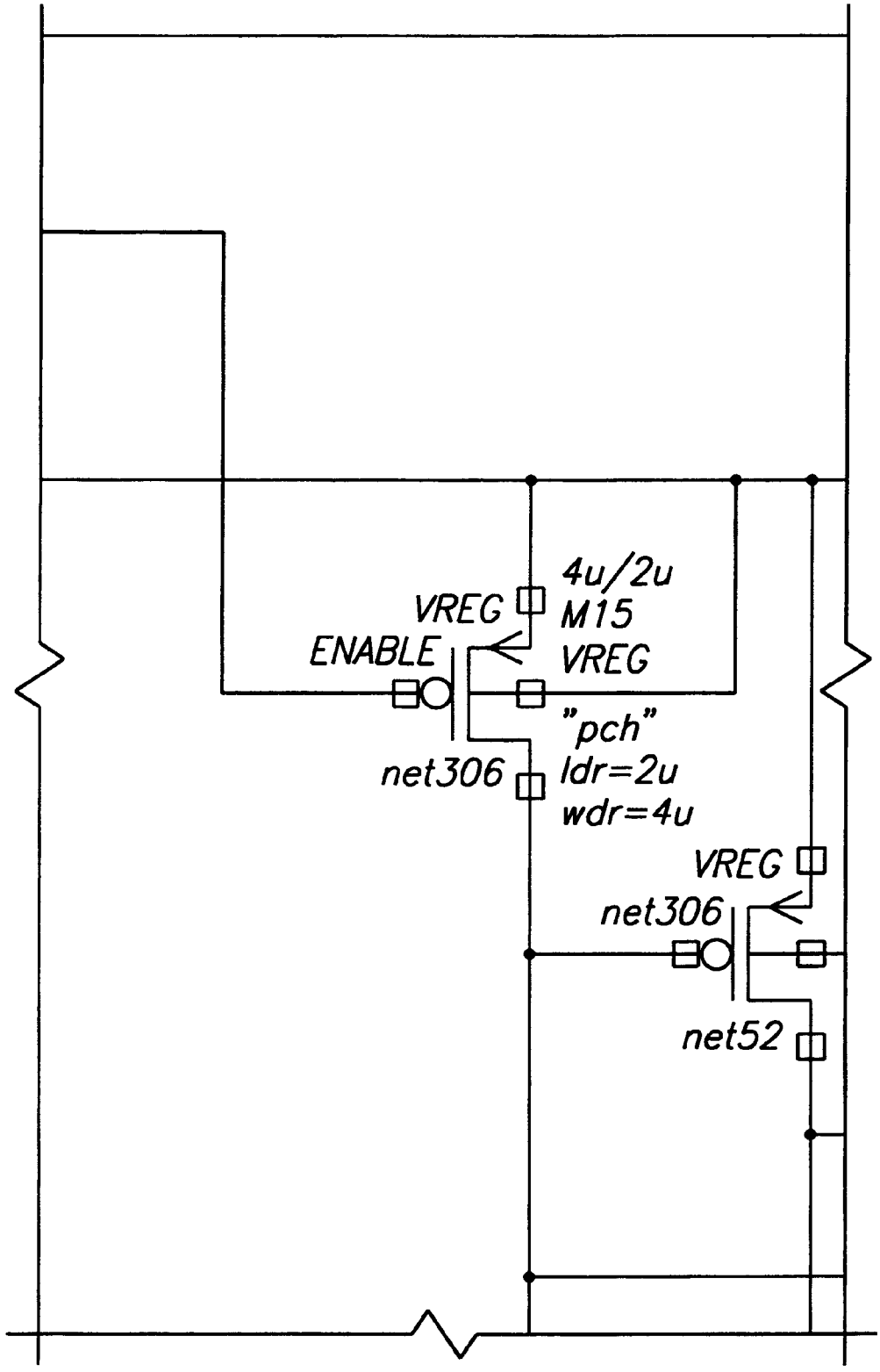


FIG 88,050,401AE

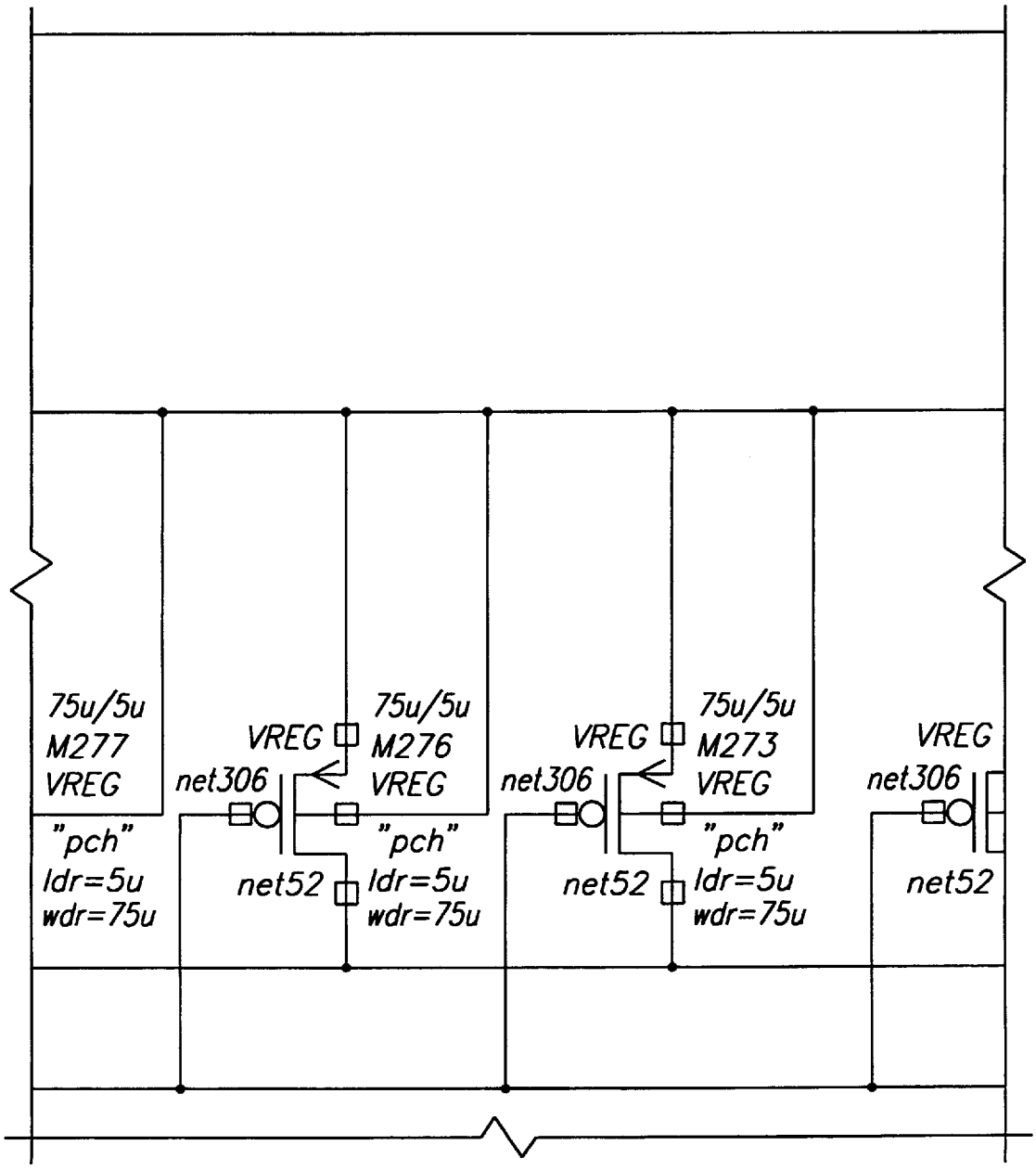


Fig 88.0504001AF

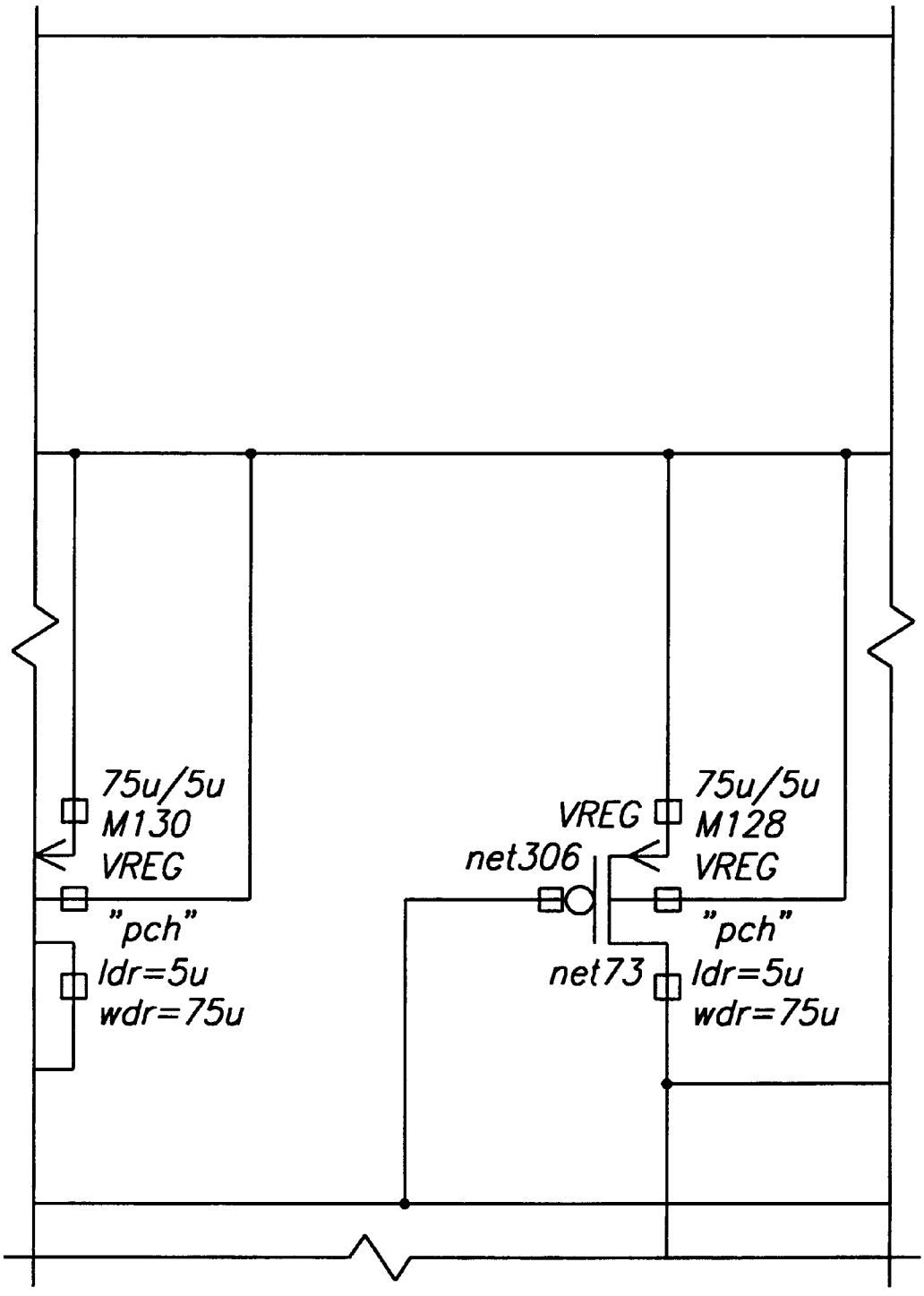


FIG 8,050,401AG

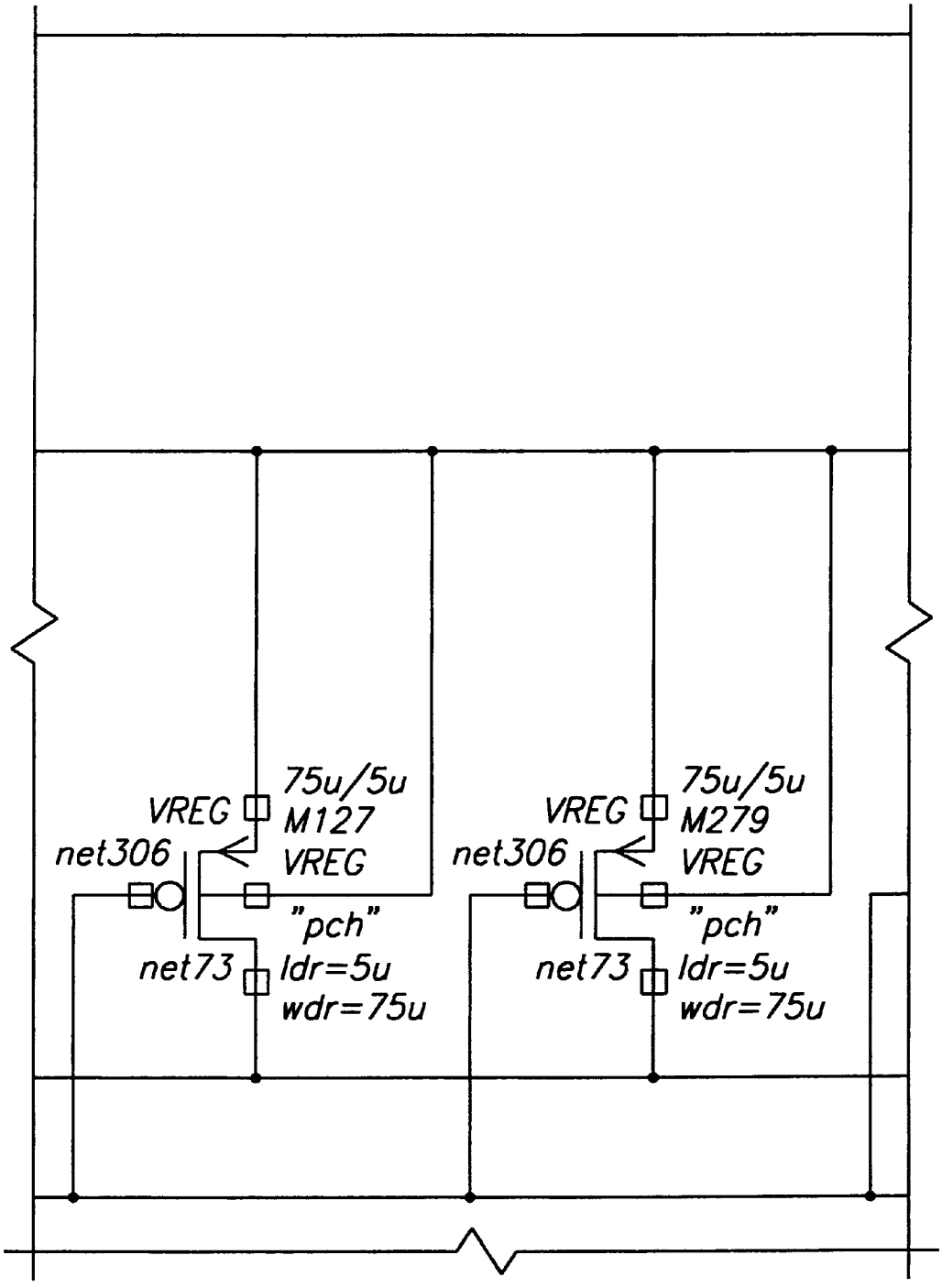


Fig 8,050,401AH

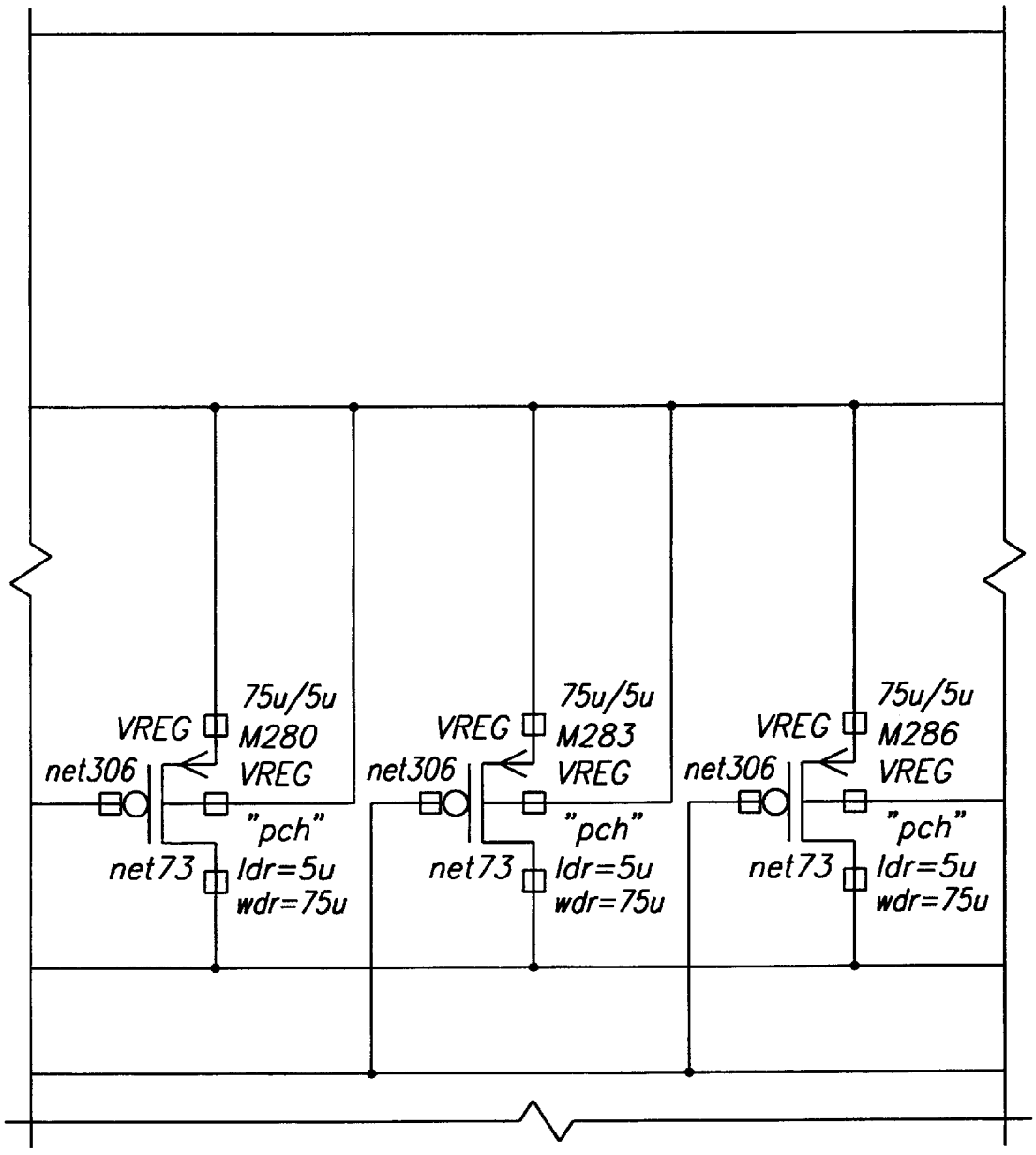


Fig 8,050,401AII

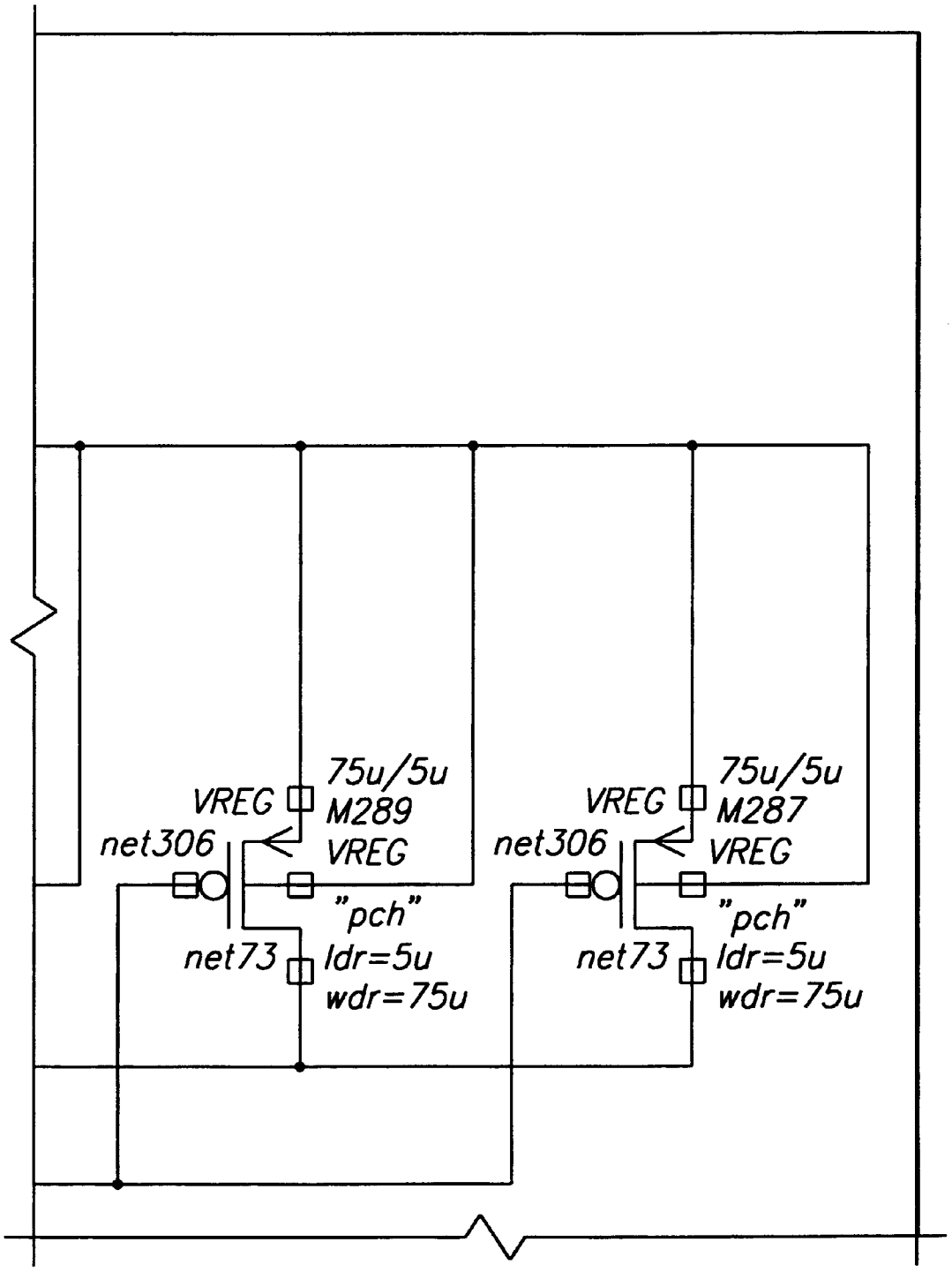


Fig 8,054,011A1

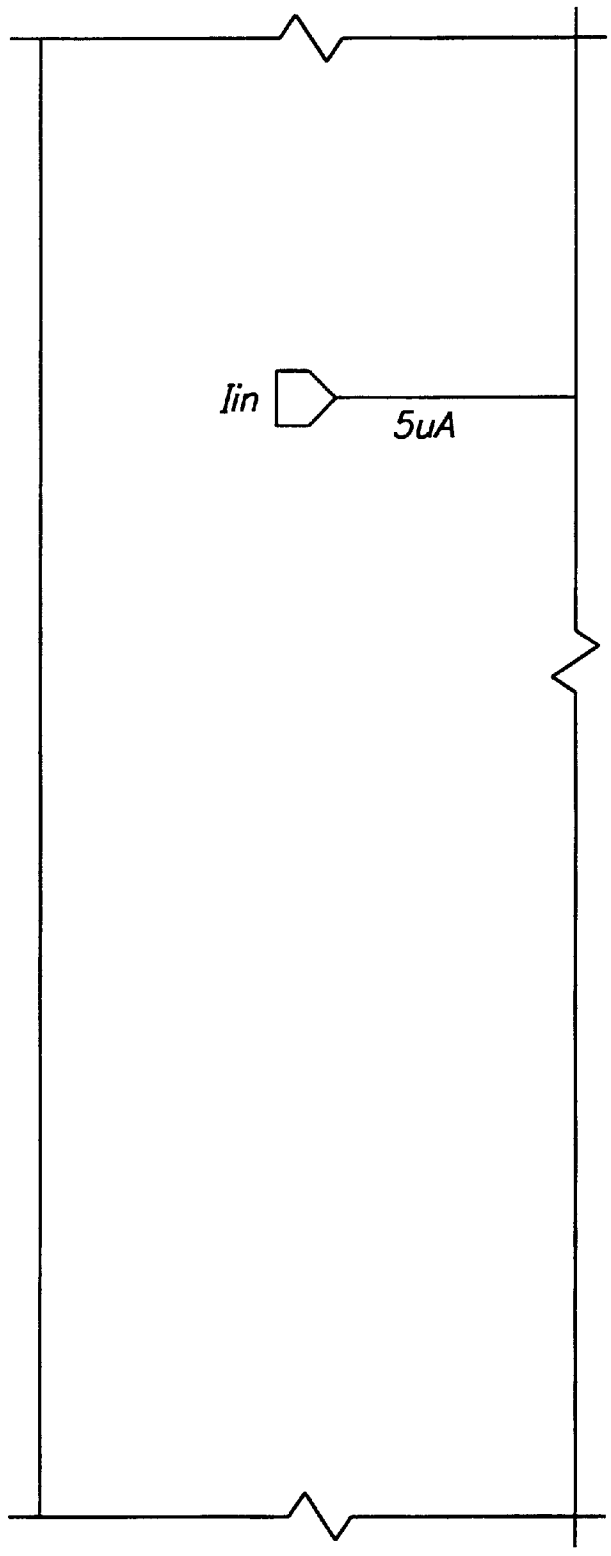
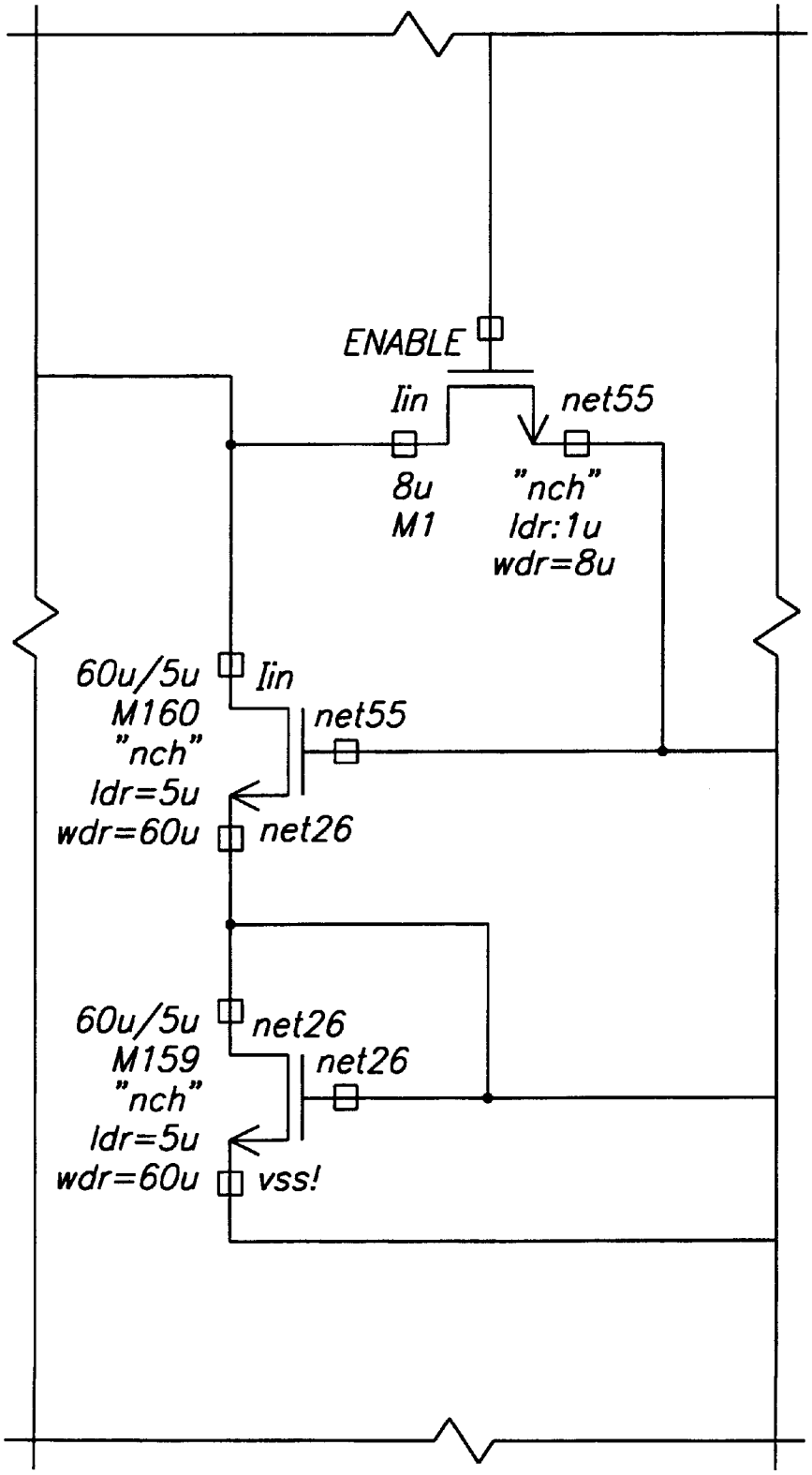


Fig 8,050,401BA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8u
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ldr:1u
wdr=8u
60u/5u
M160
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ldr=5u
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Iin
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net26
60u/5u
M159
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net26
net26
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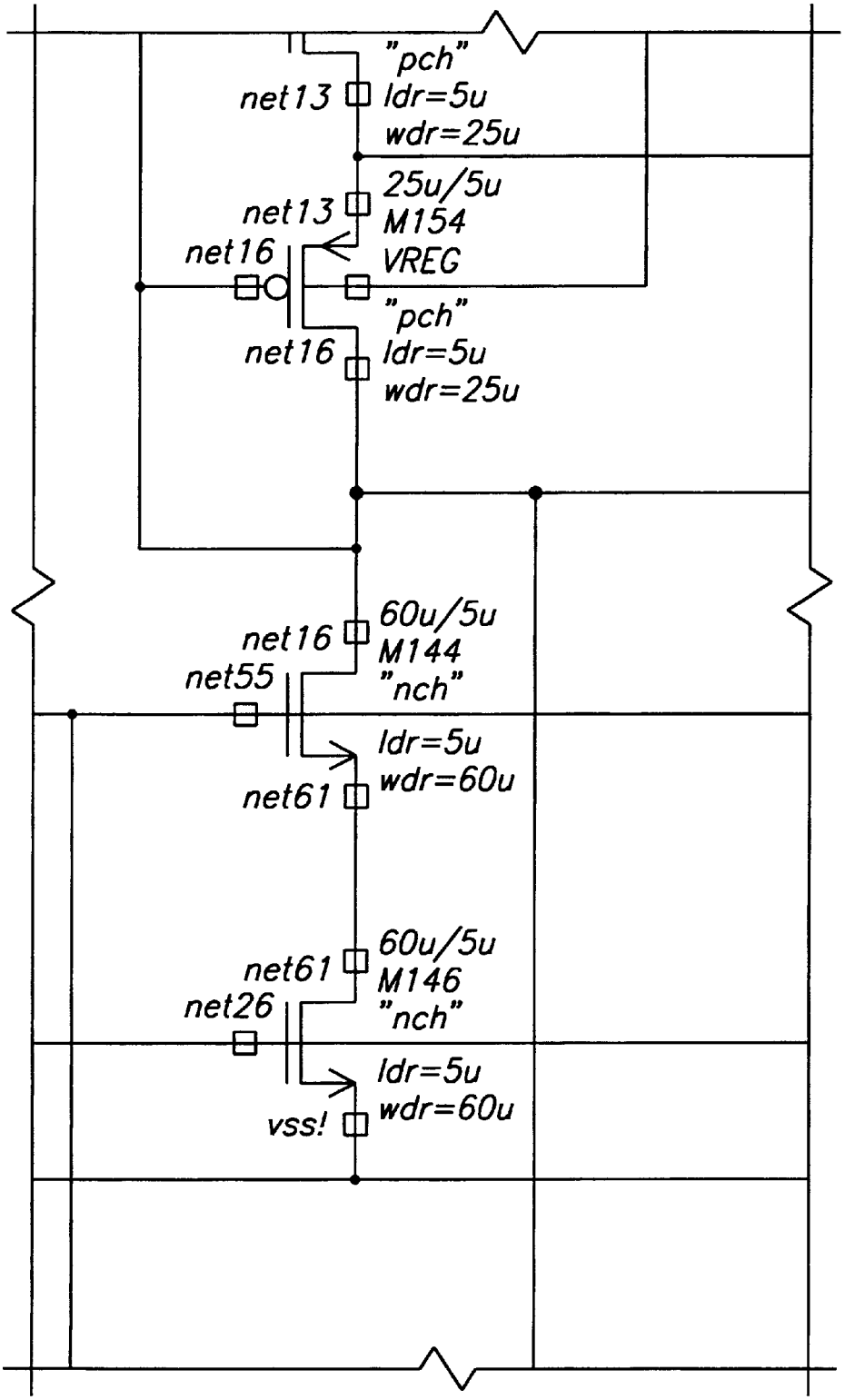


Fig 6,050,401BC

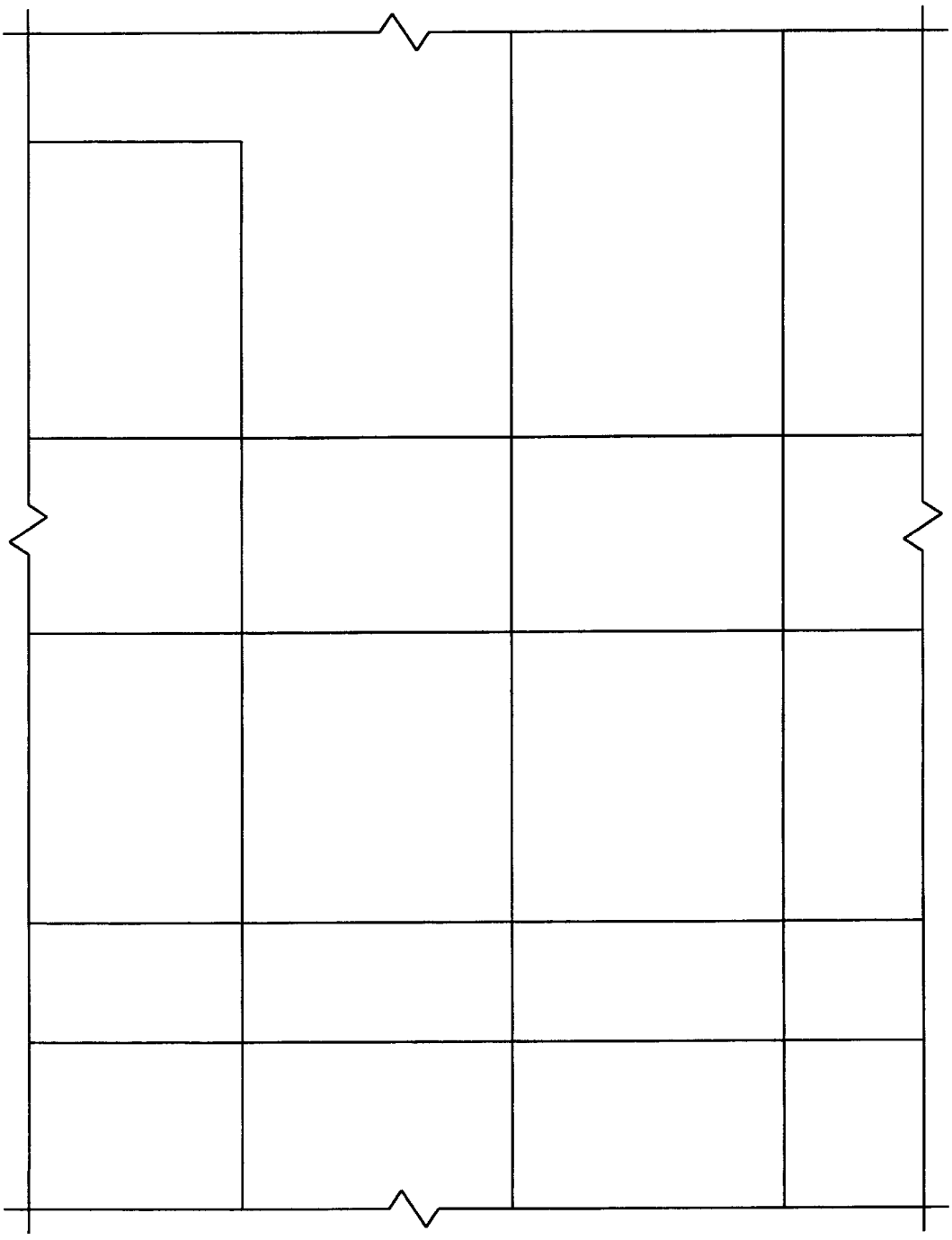


Fig 8.0504.01BD

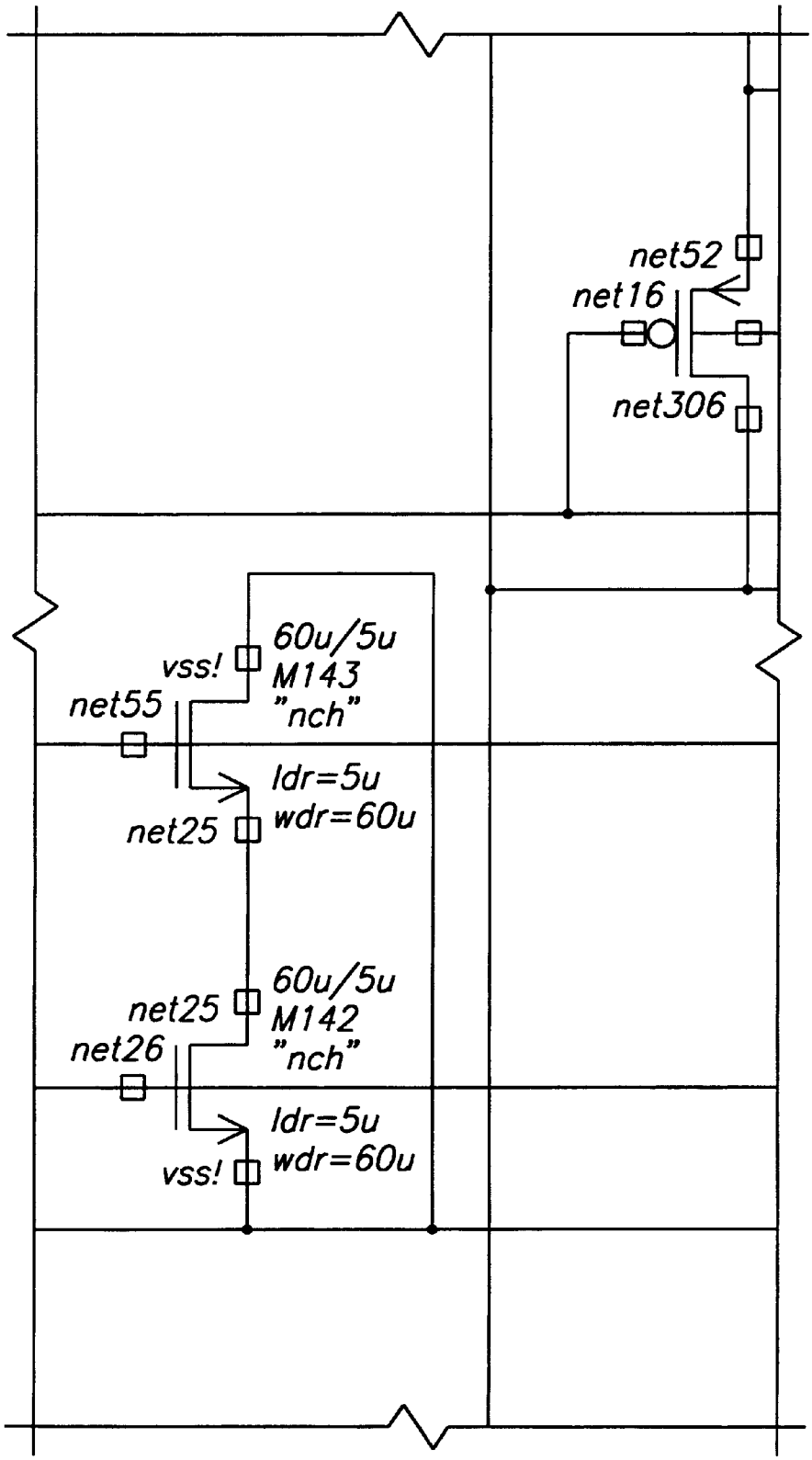


Fig 88,050,011BE

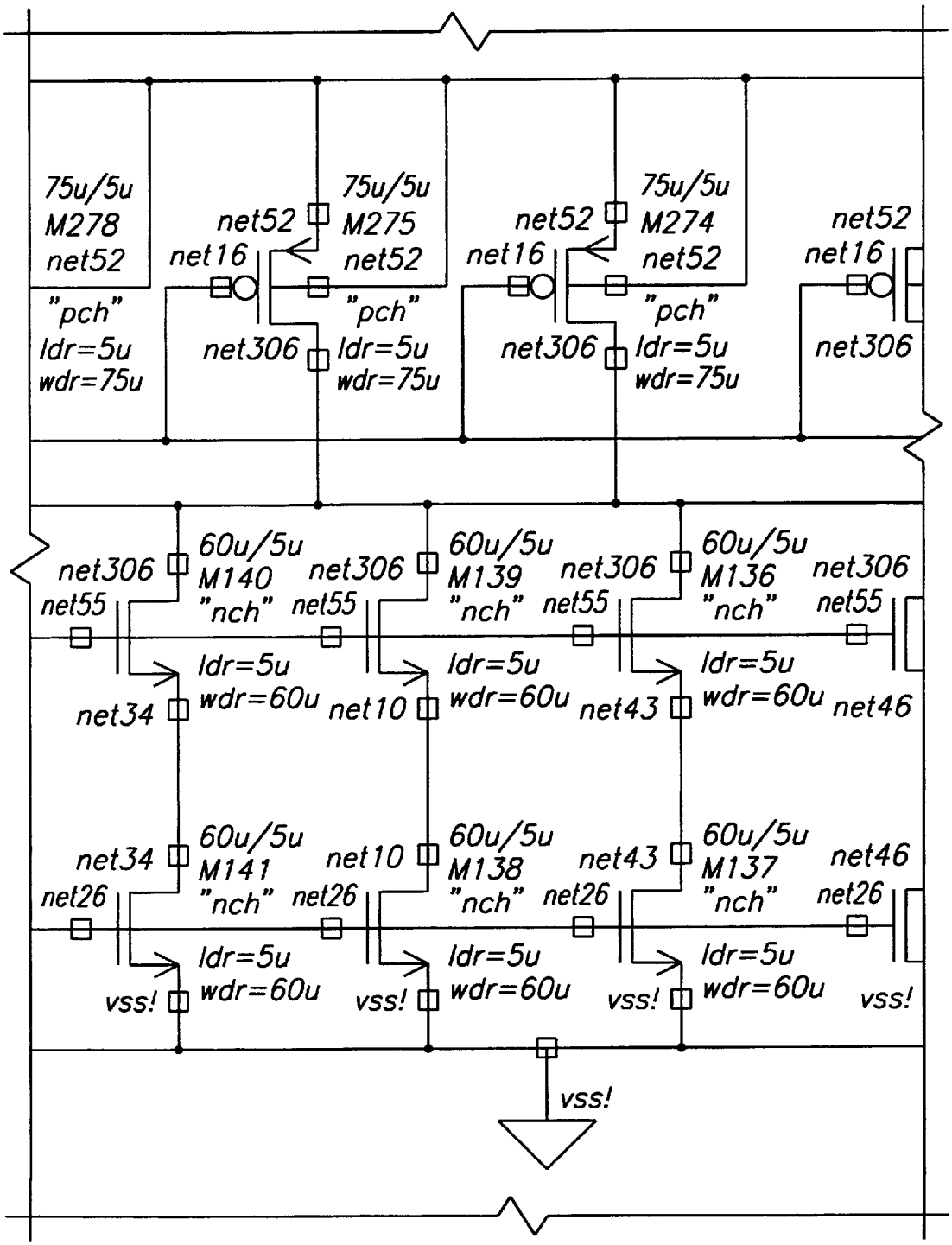
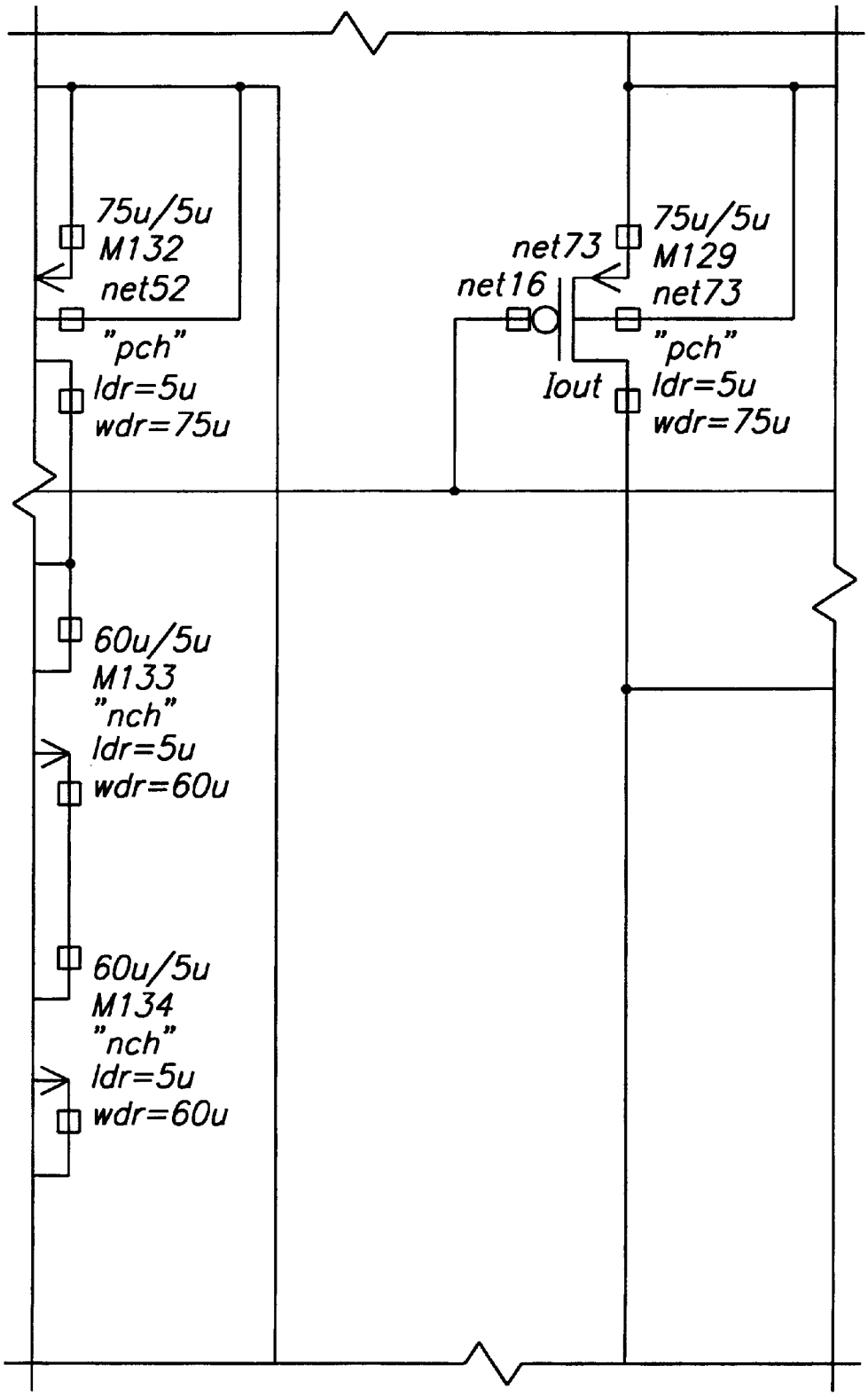


Fig 8,050,401 BF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wdr=60u

Fig 8,054,018

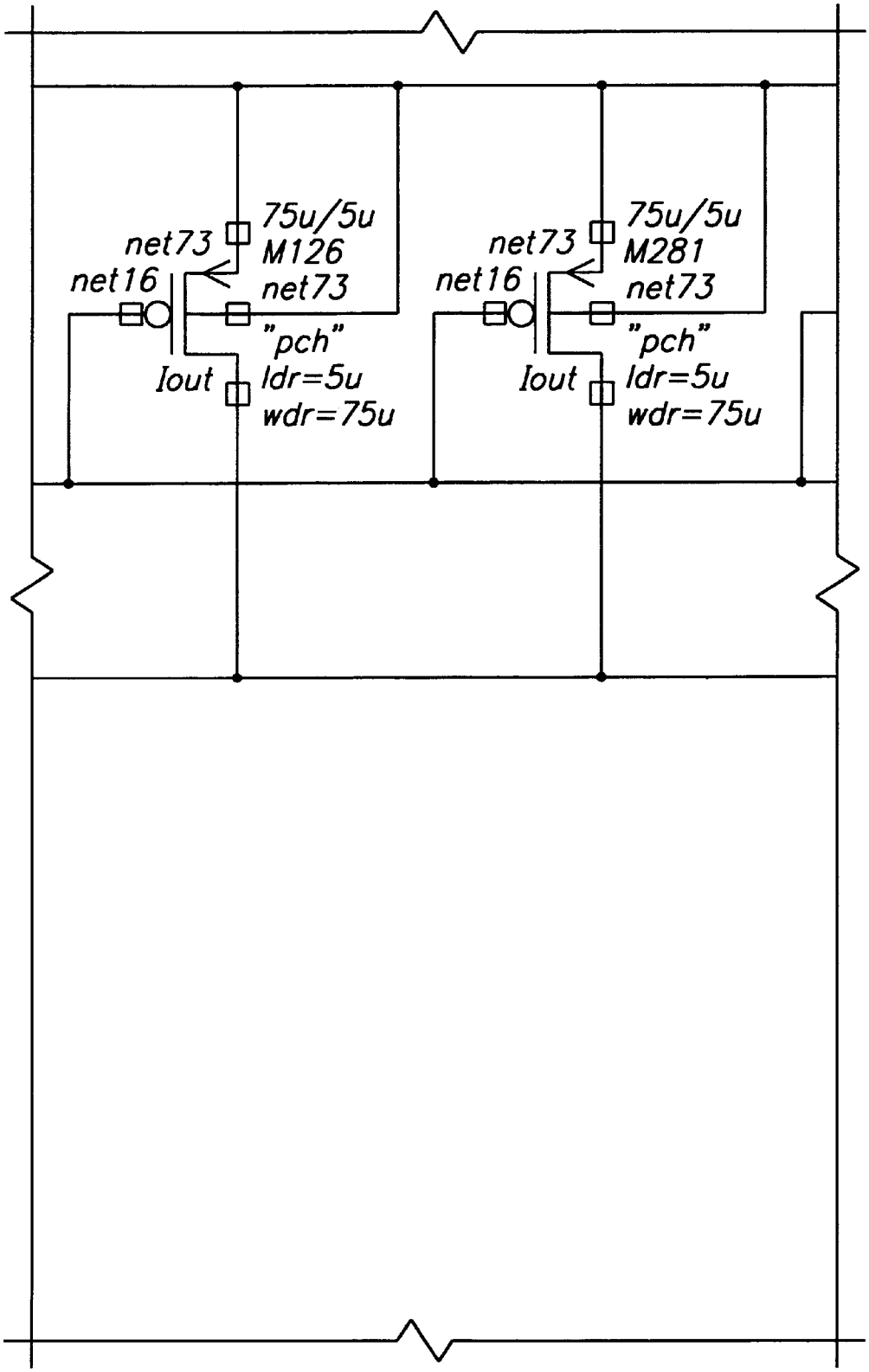


Fig 88.0504.01BH

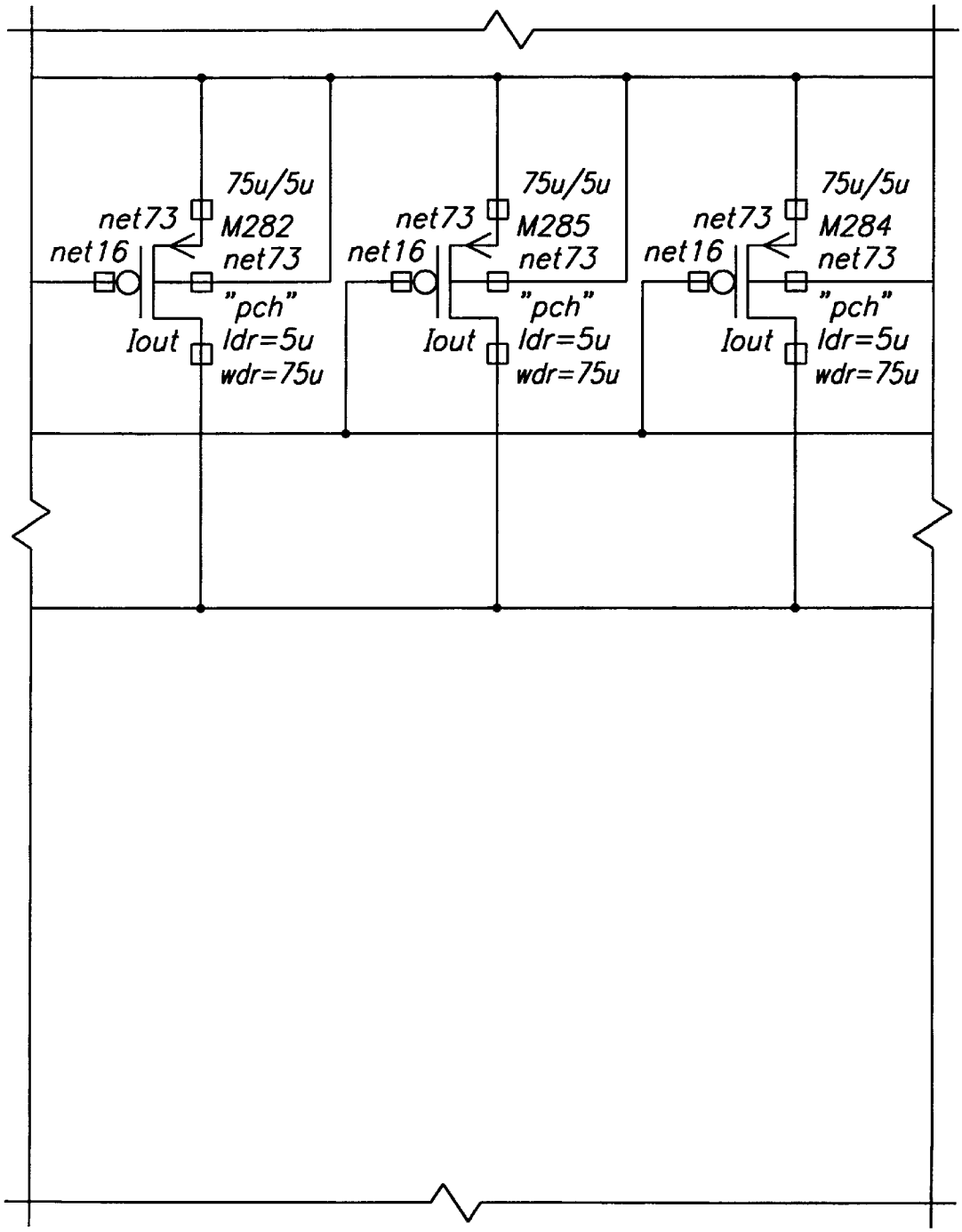


FIG 88.0500401B1

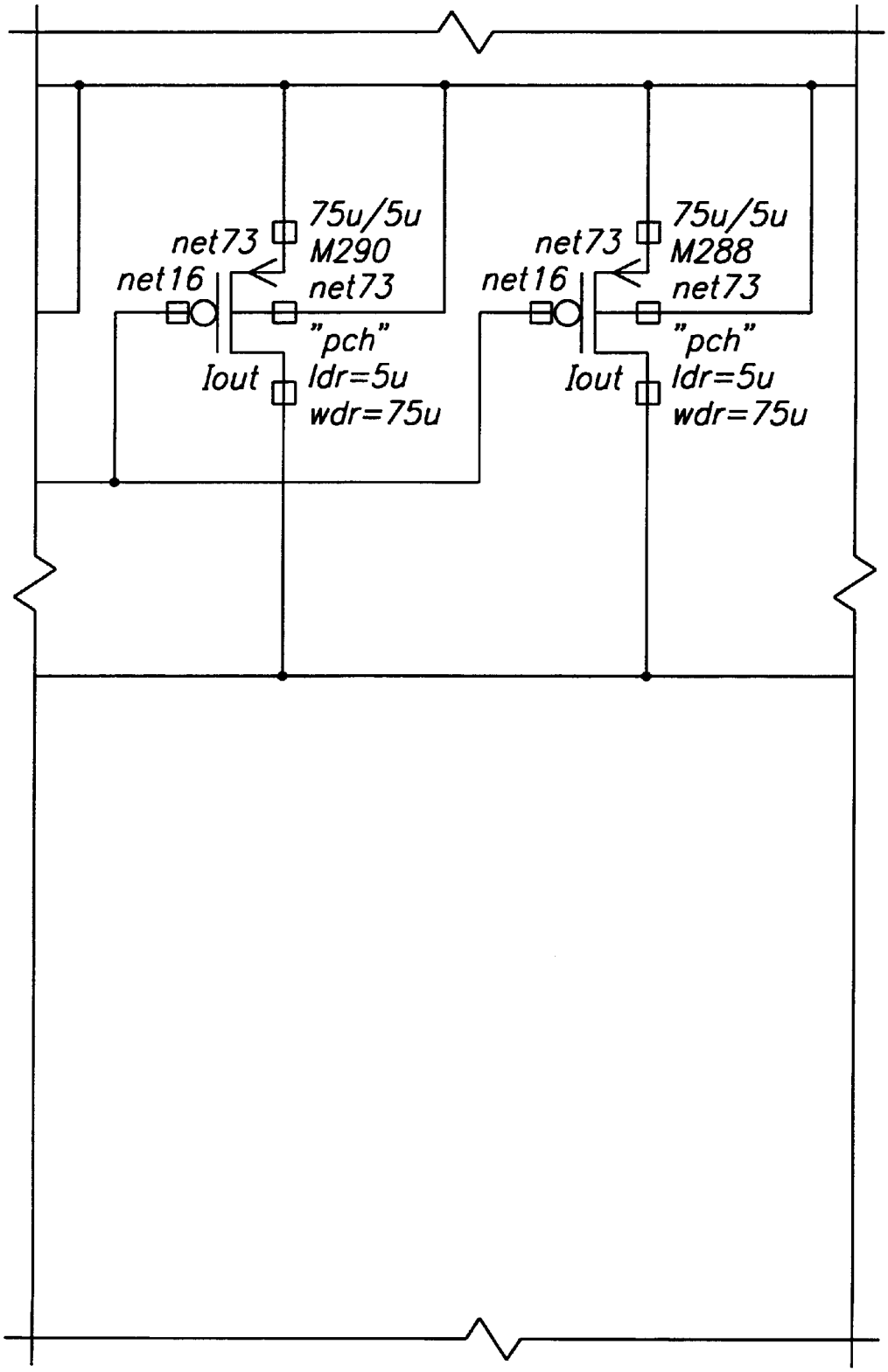


Fig 8,054,011B1

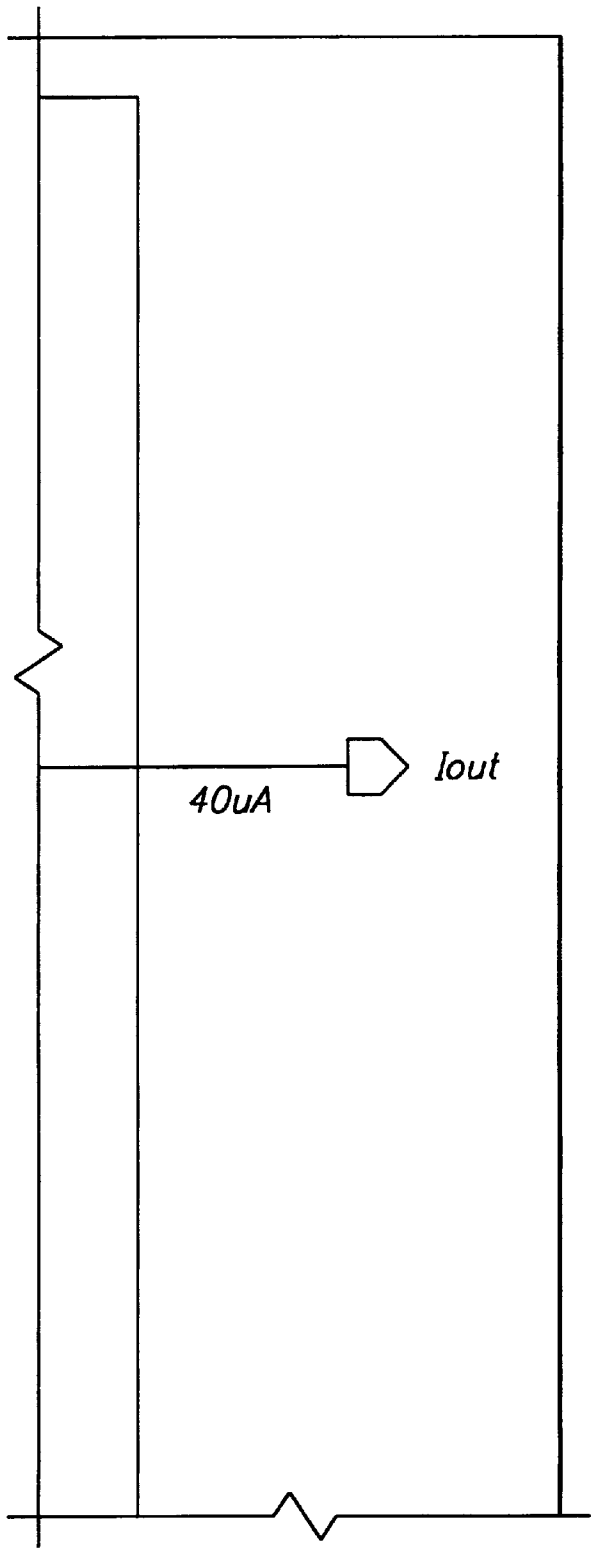


Fig 8.0504.01BK

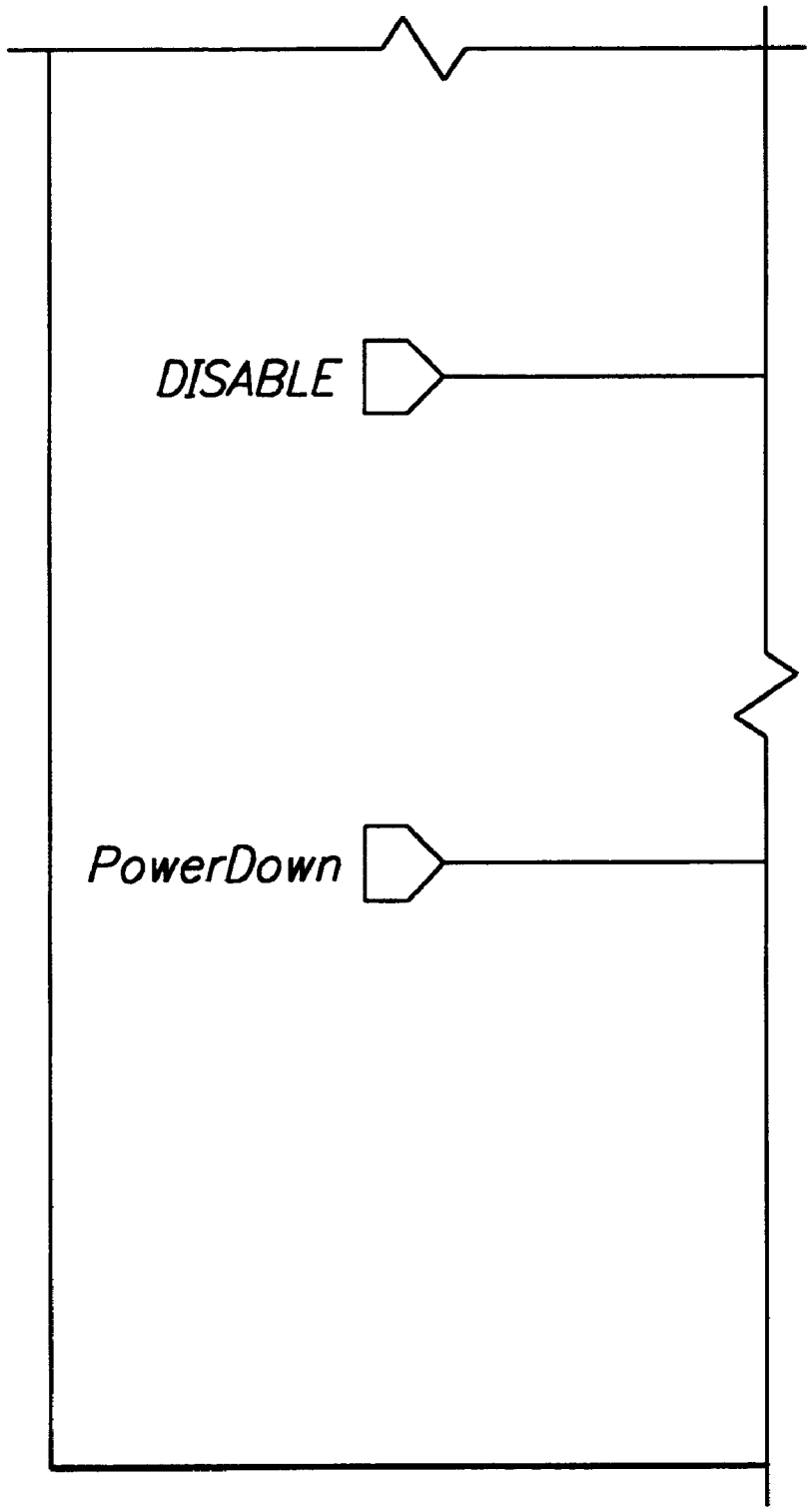


Fig 88.0504MICA

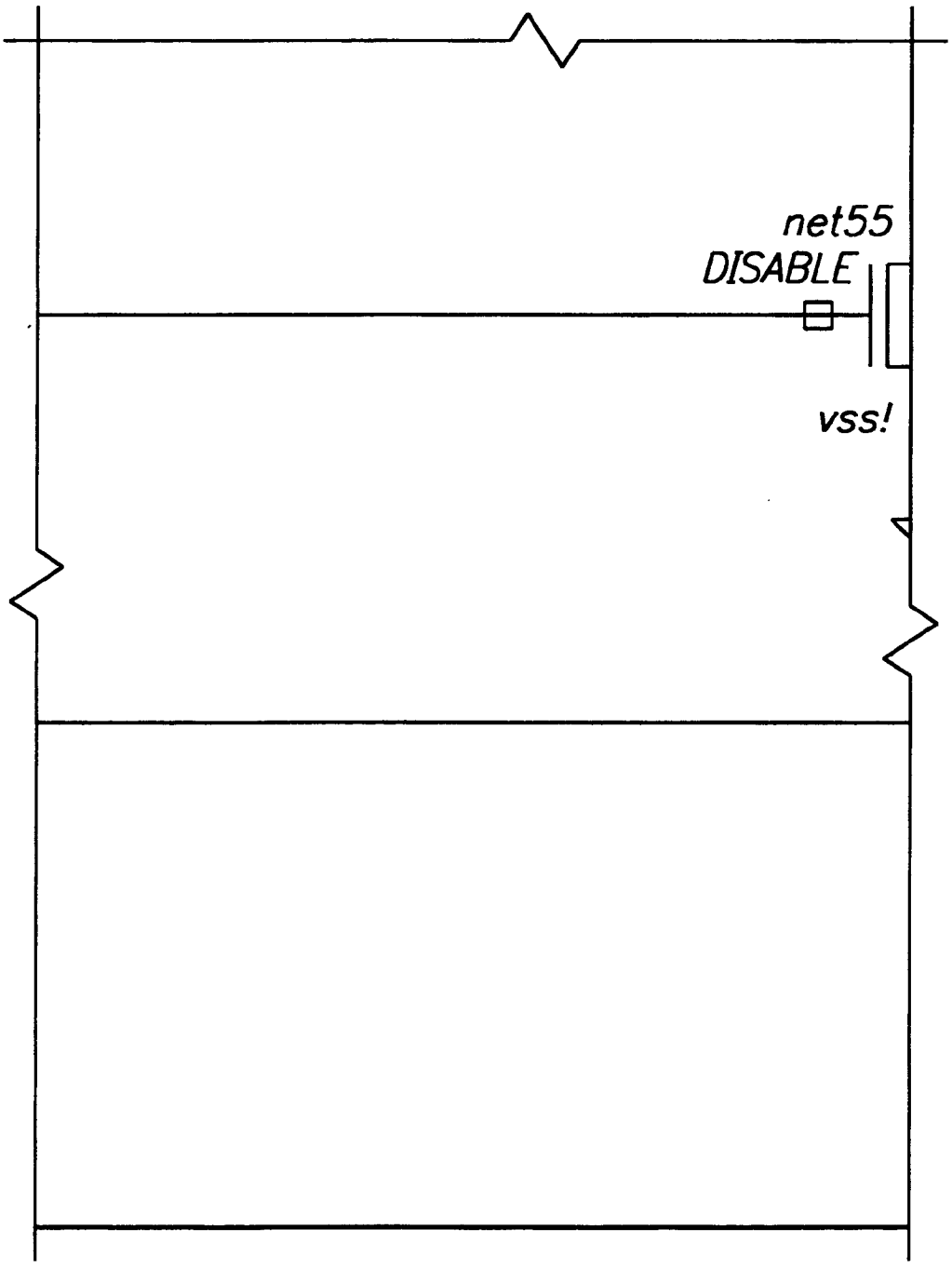


Fig 8.0504MICB

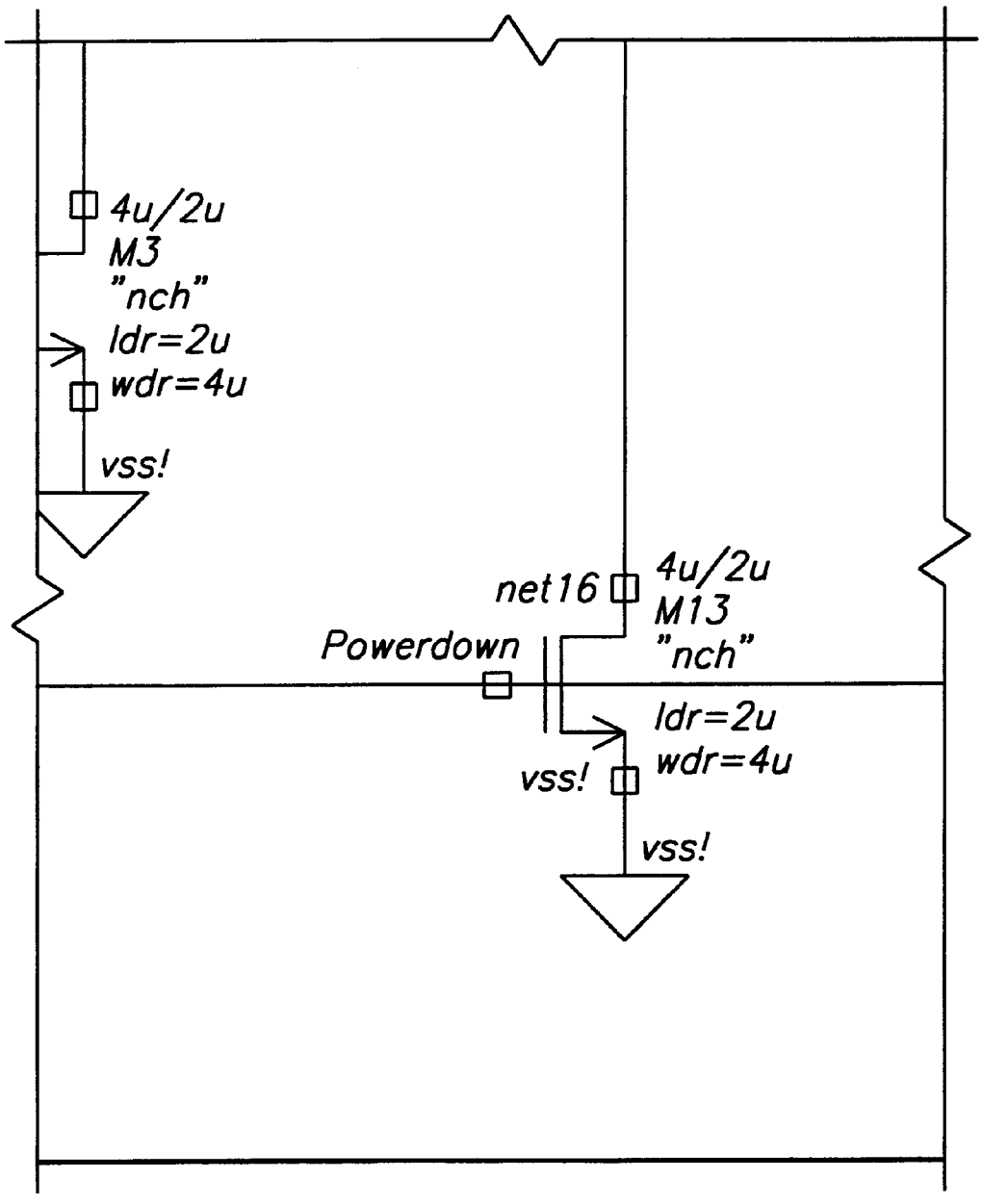


Fig 8,054,011C

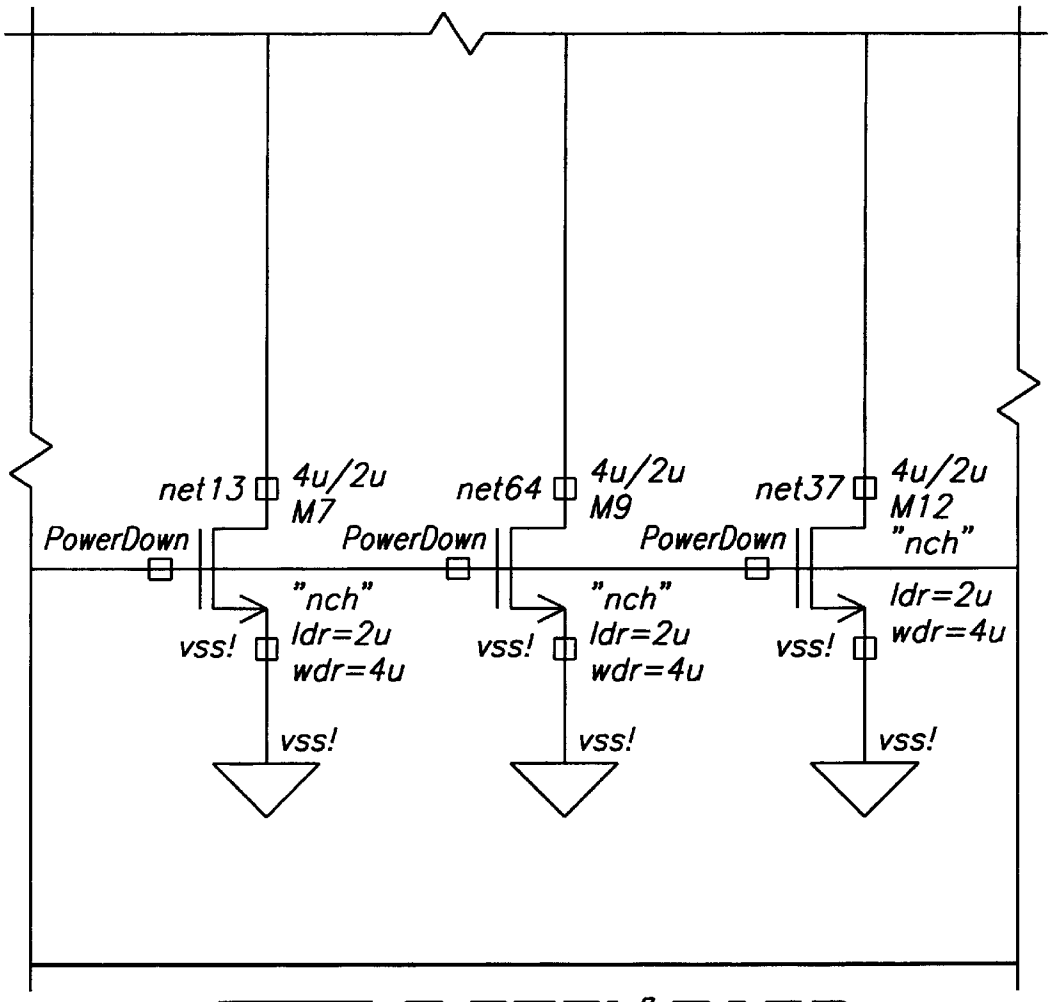


Fig 8,050,401C

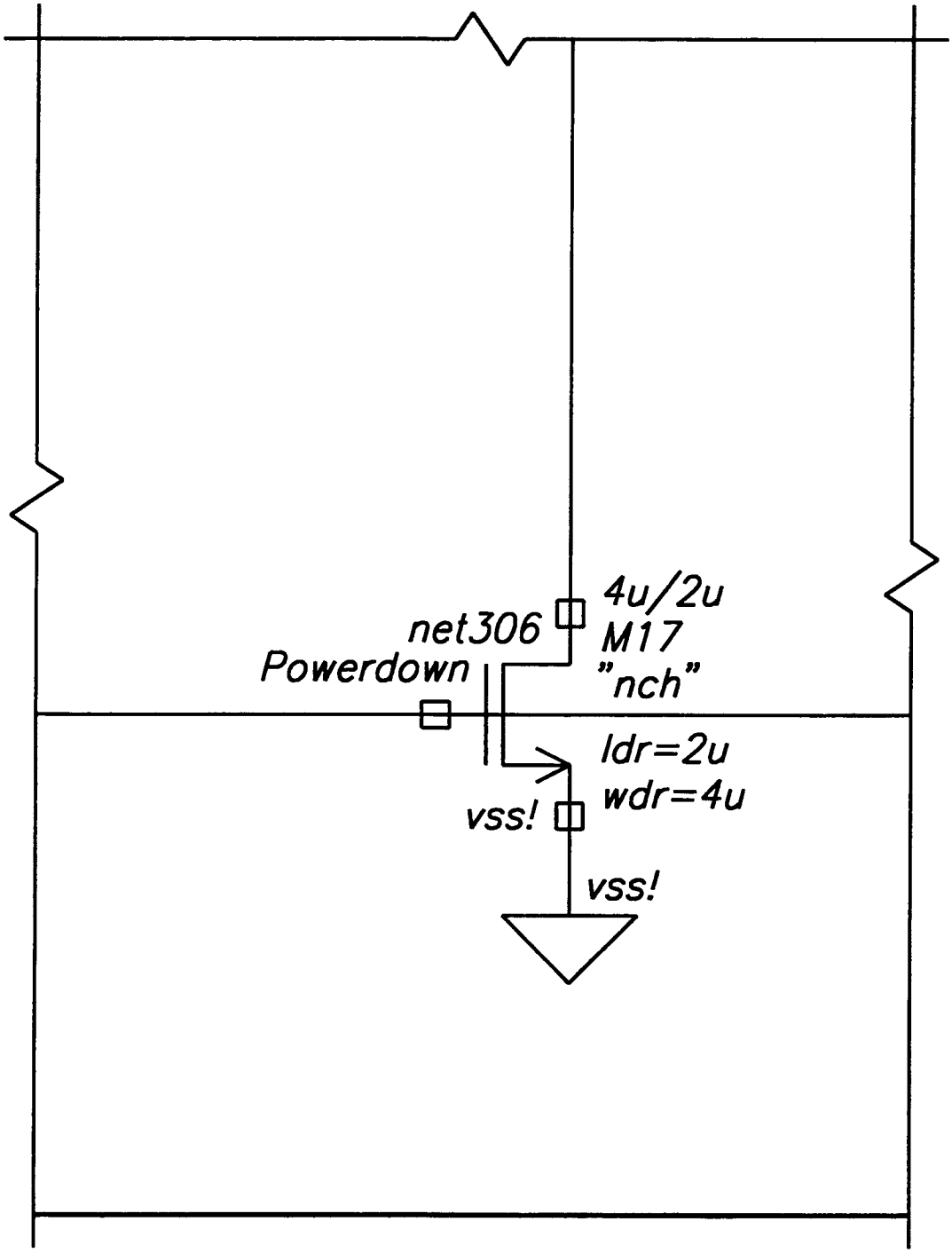


FIG 8B0504001CE

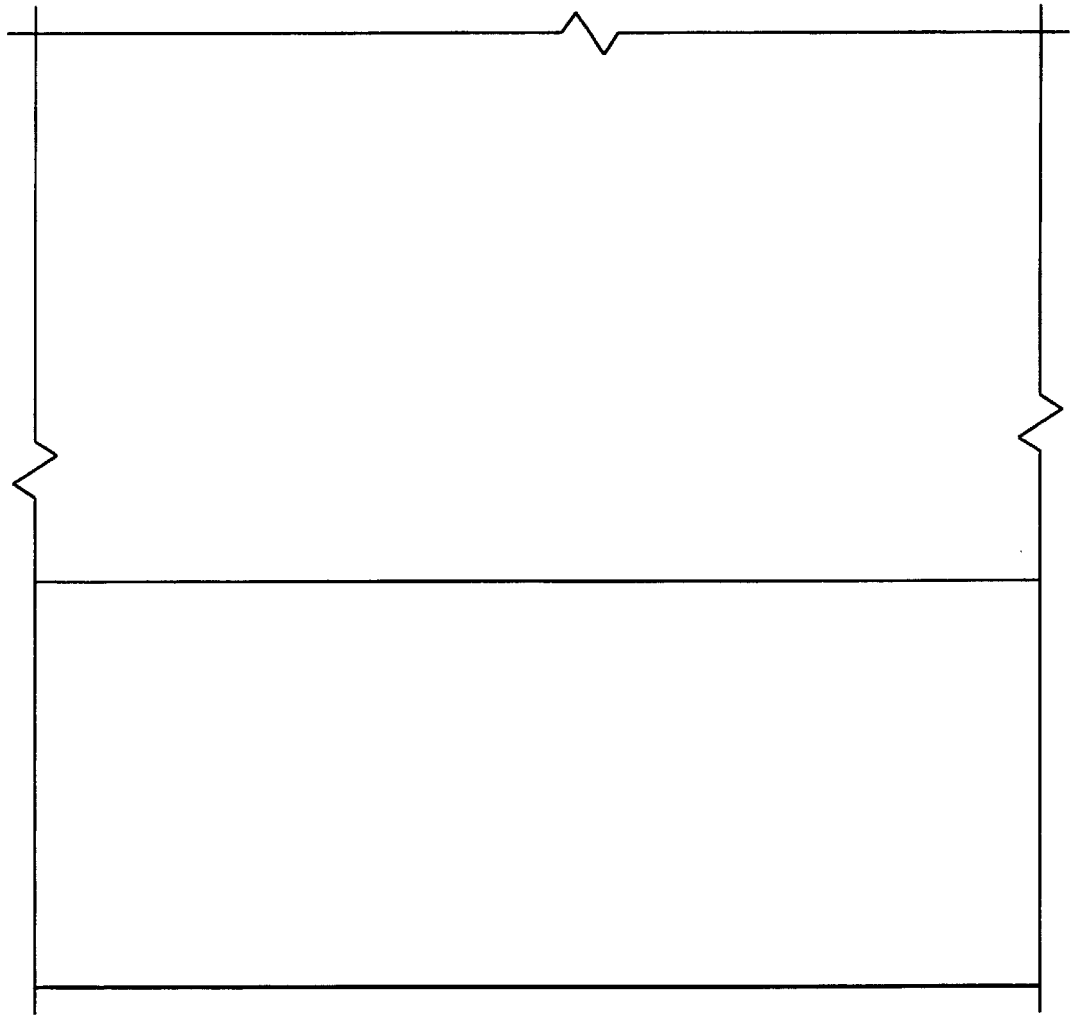


Fig 8.0504.01CF

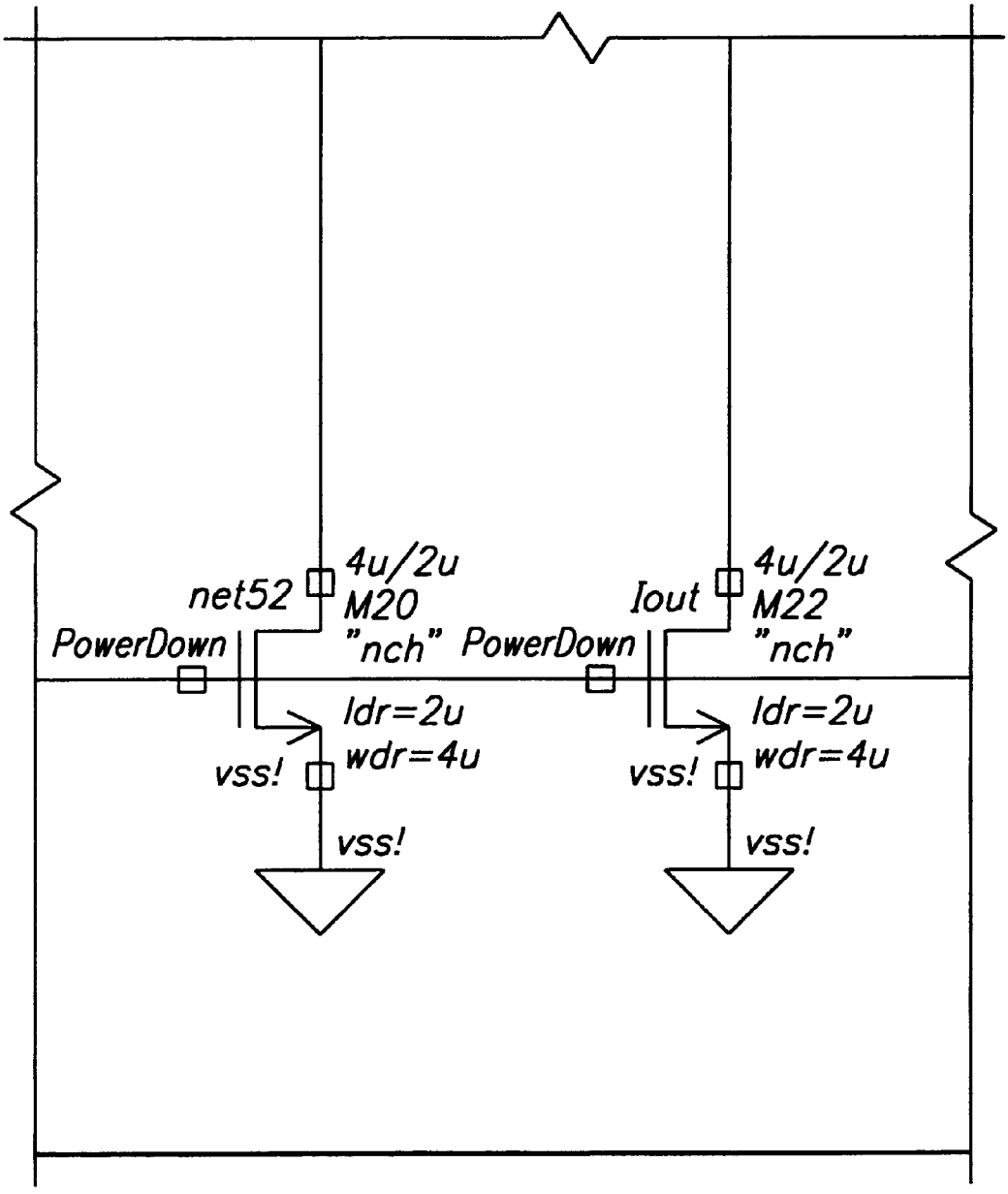


Fig 8,050,401C6

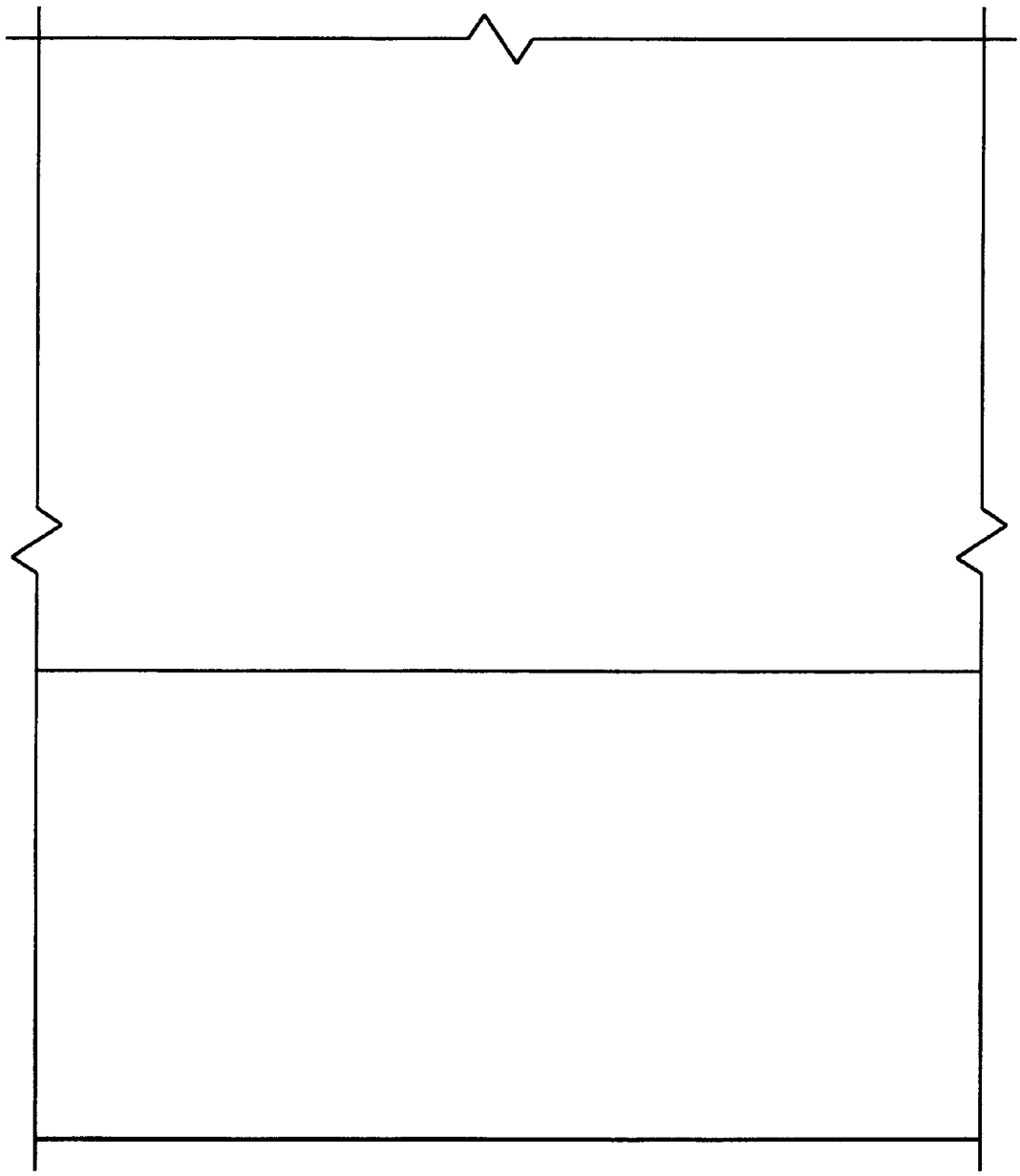


Fig 80504

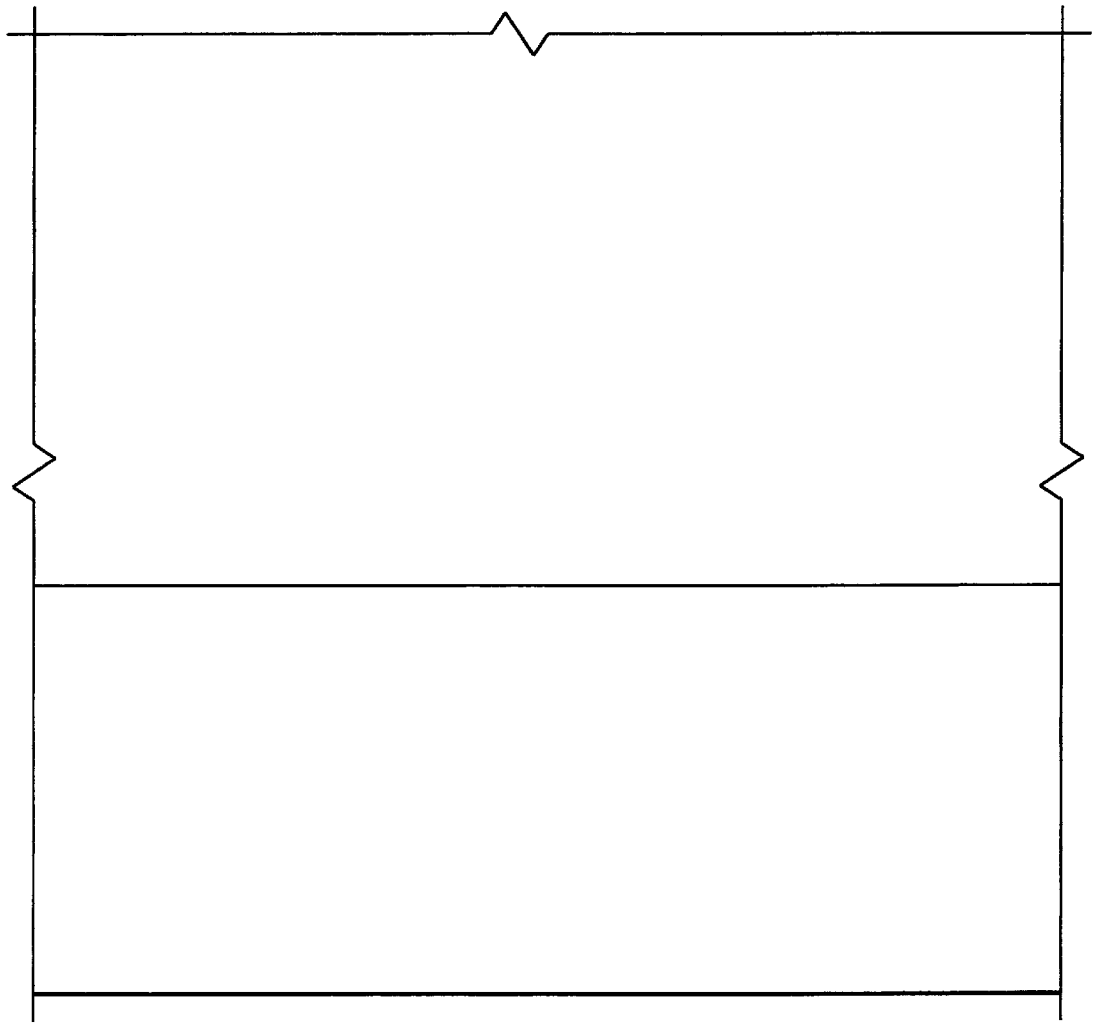


Fig 8.0504.0IC2

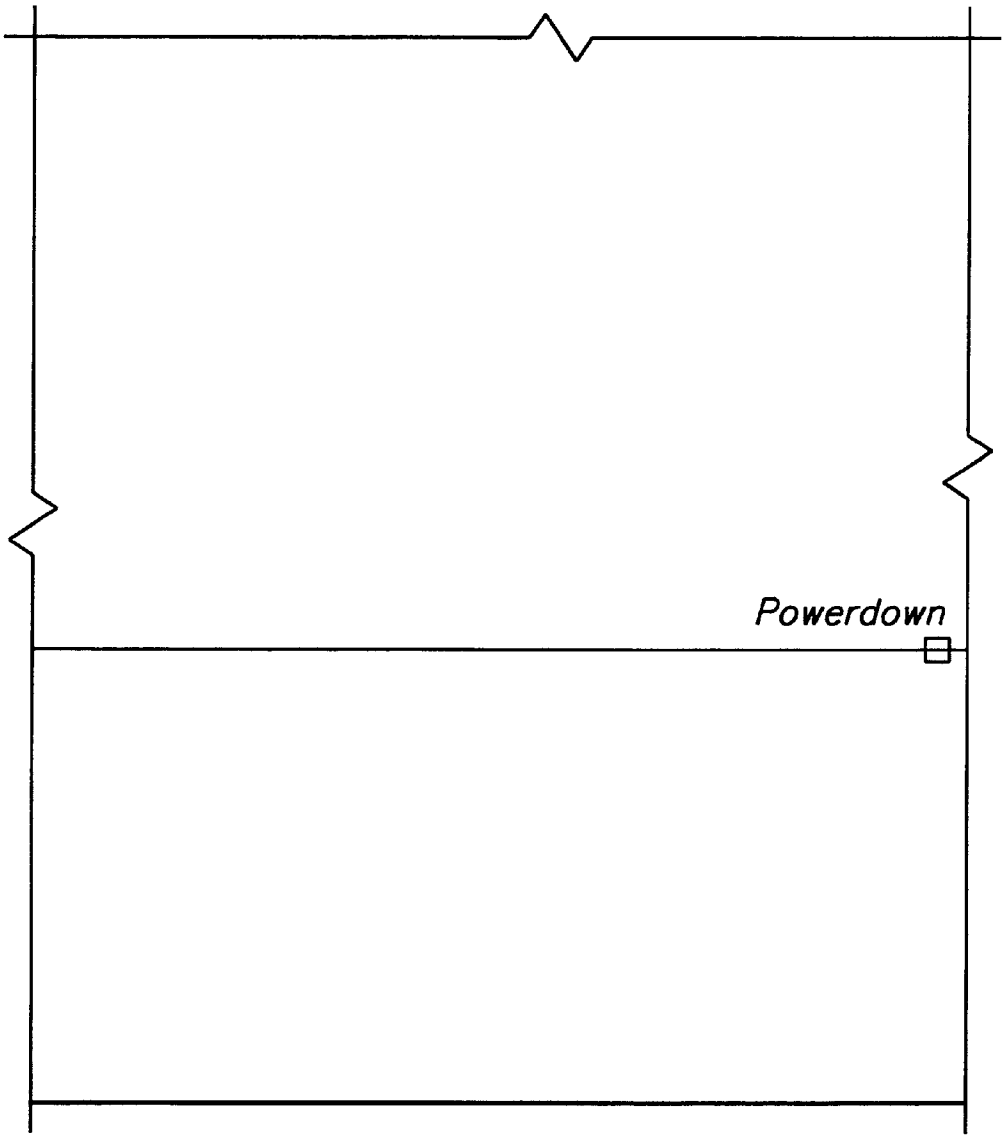


Fig 8050401Cal

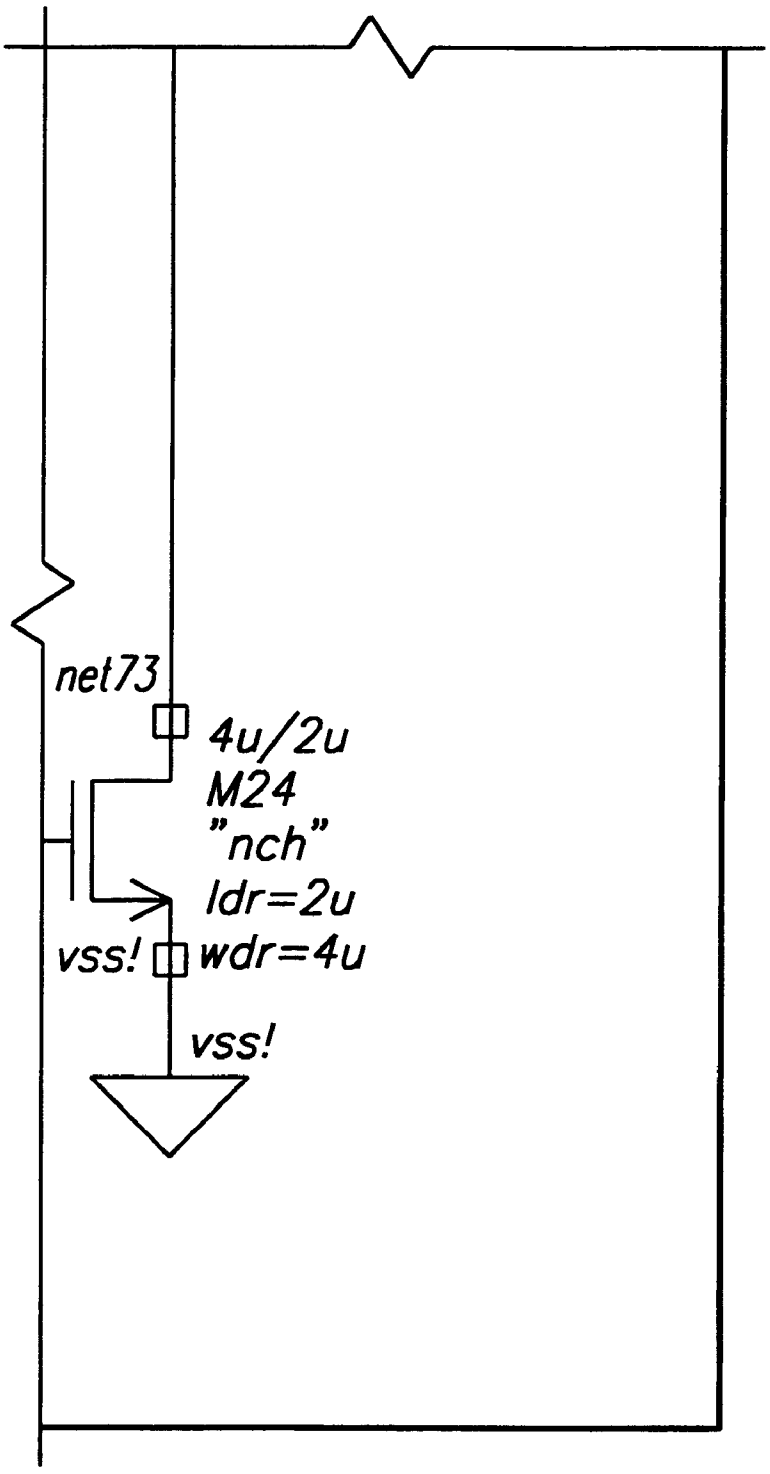


Fig 8.0504MICK

8.050402AA	8.050402AB	8.050402AC	8.050402AD	8.050402AE	8.050402AF	8.050402AG	8.050402AH	8.050402AI	8.050402AJ
8.050402BA	8.050402BB	8.050402BC	8.050402BD	8.050402BE	8.050402BF	8.050402BG	8.050402BH	8.050402BI	8.050402BJ
8.050402CA	8.050402CB	8.050402CC	8.050402CD	8.050402CE	8.050402CF	8.050402CG	8.050402CH	8.050402CI	8.050402CJ

FIG. 8.050402

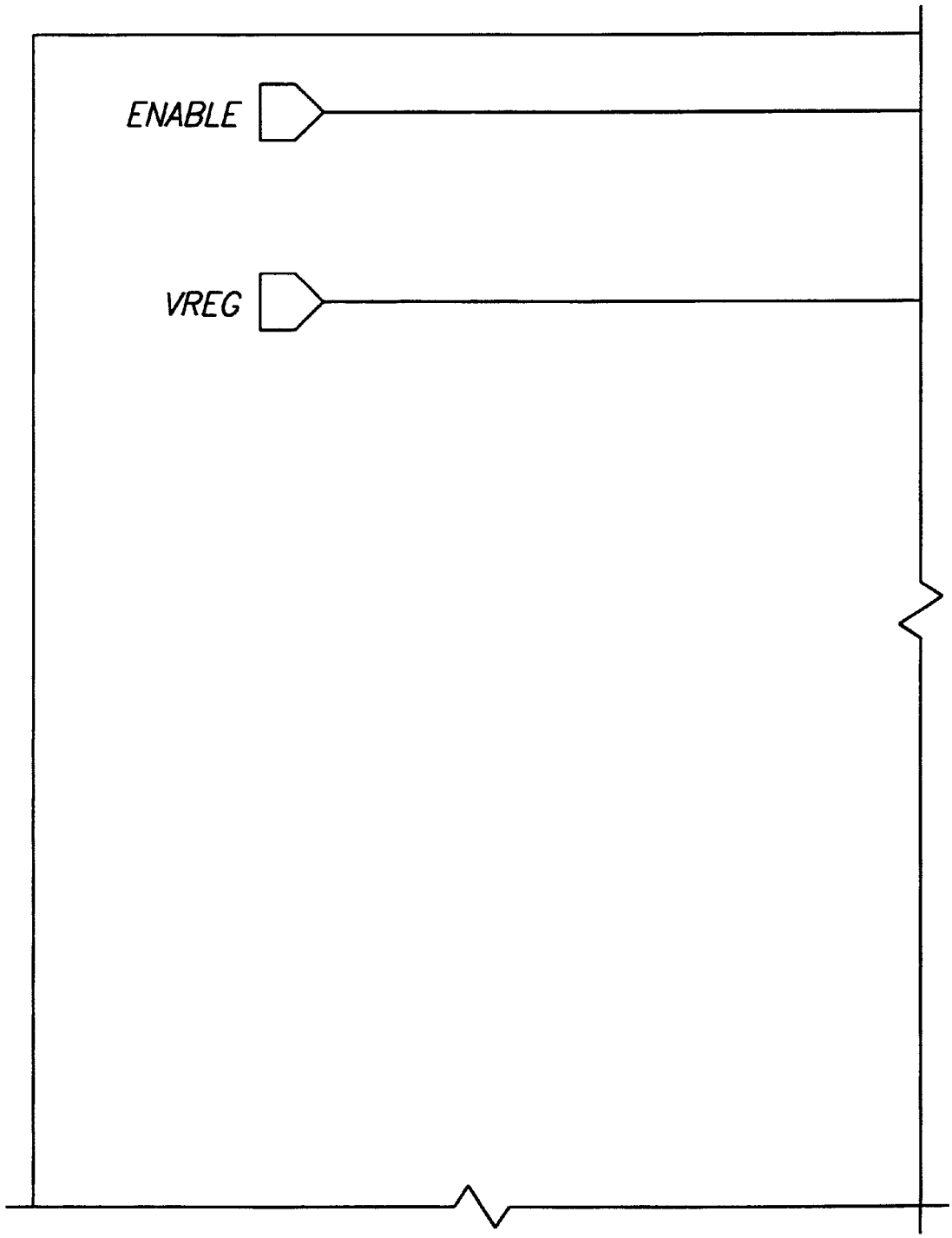


Fig 8.0504.02AA

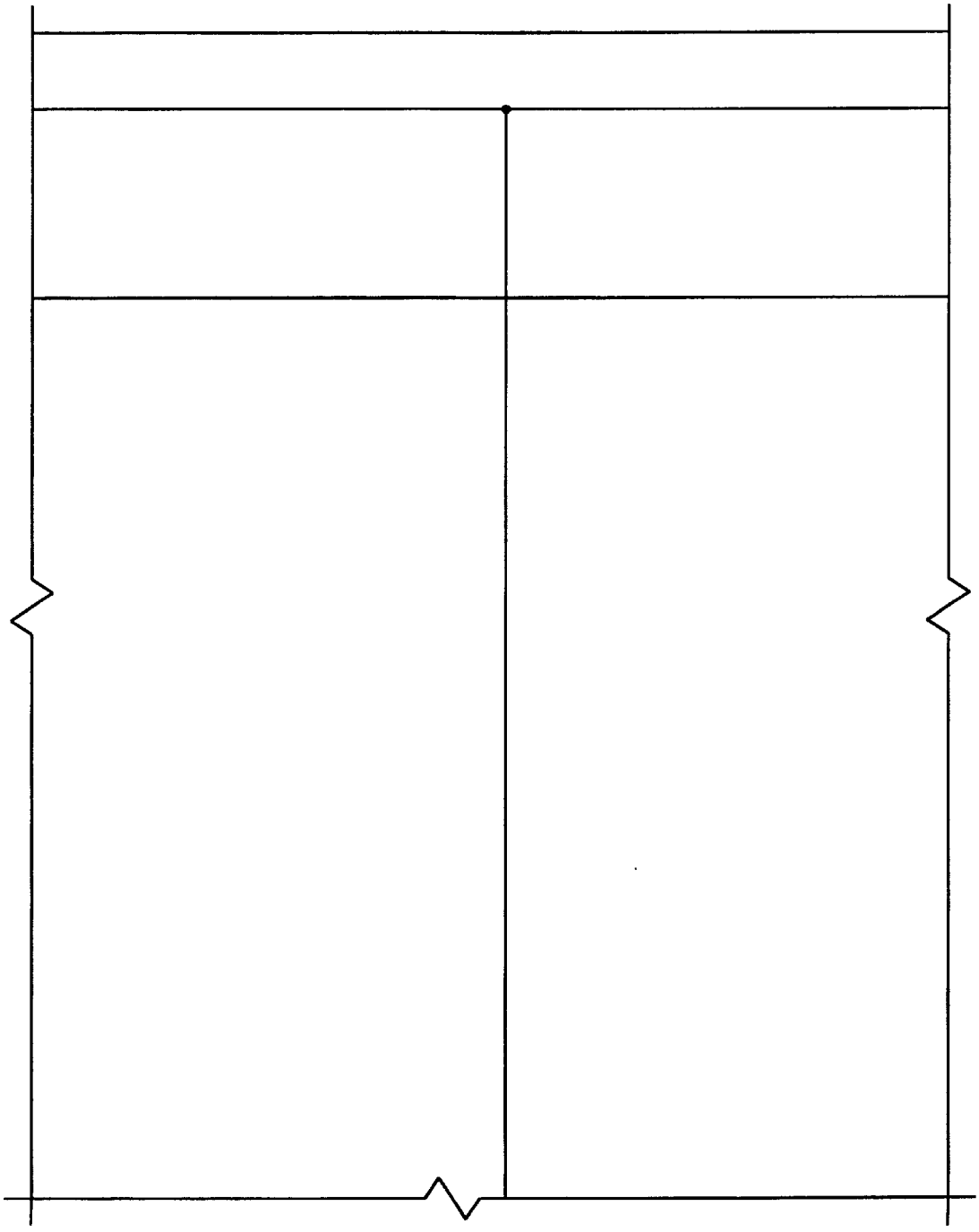


Fig 8.0504.02AB

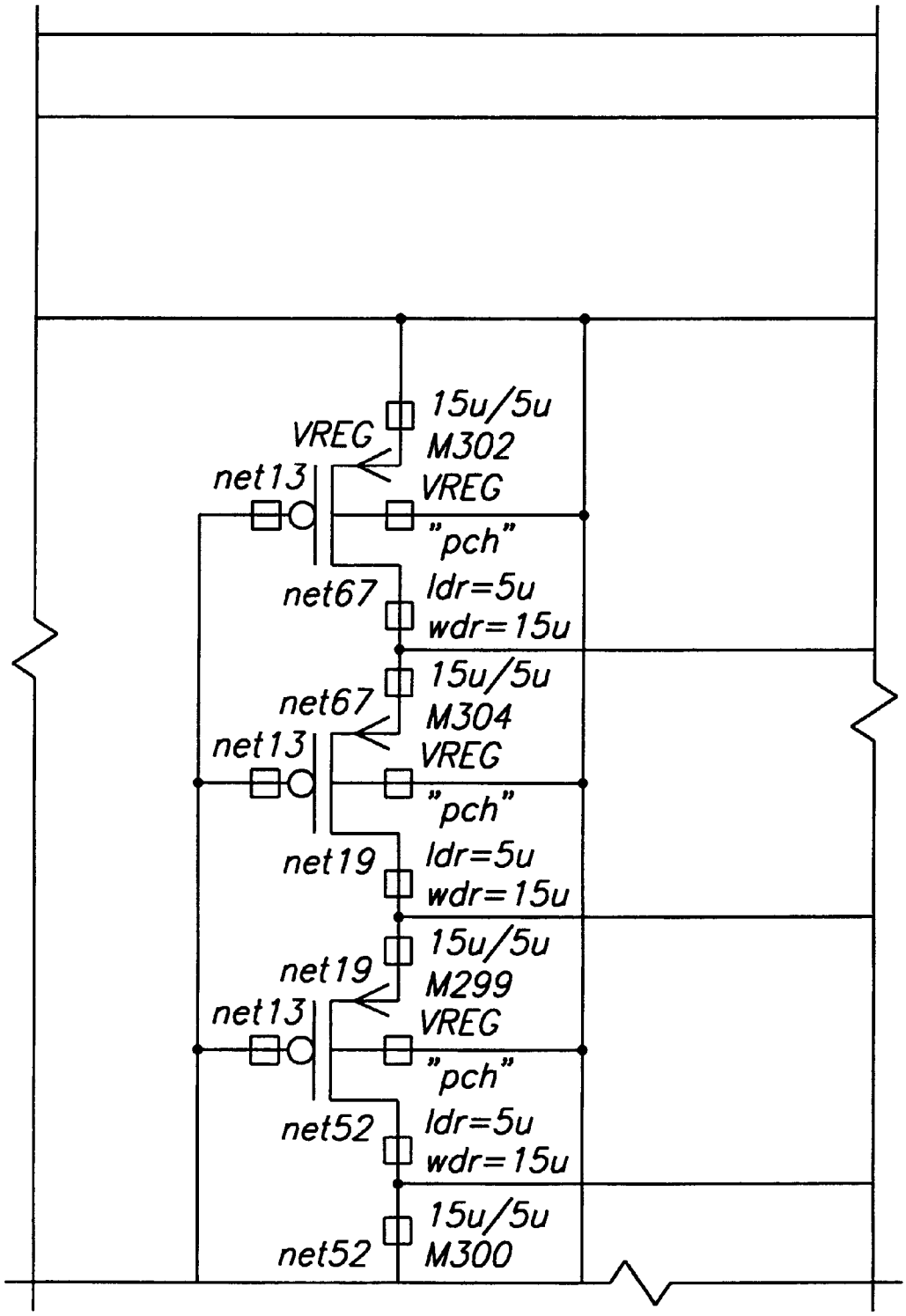


Fig 8.0504.02AC

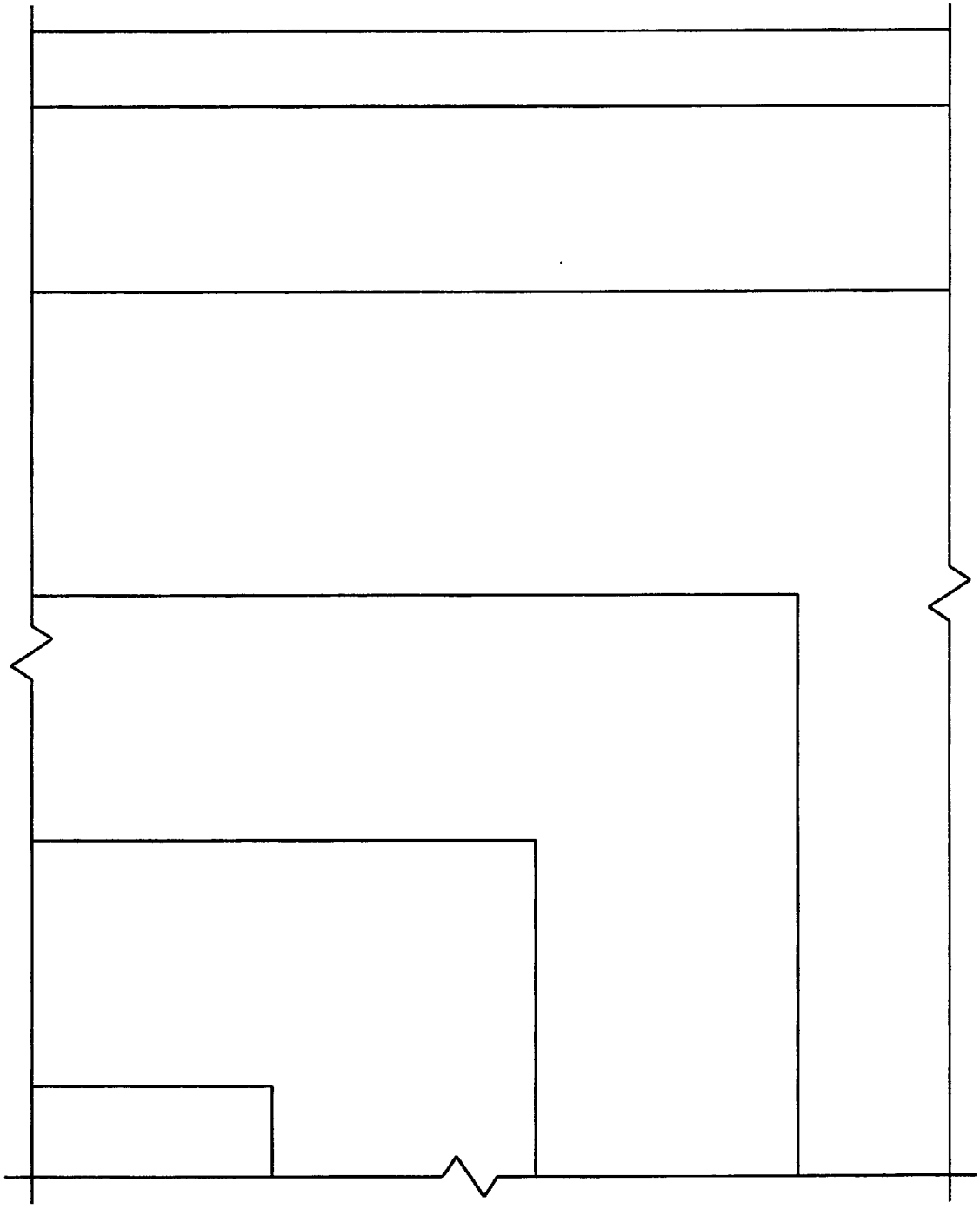


Fig 88.0504.02AD

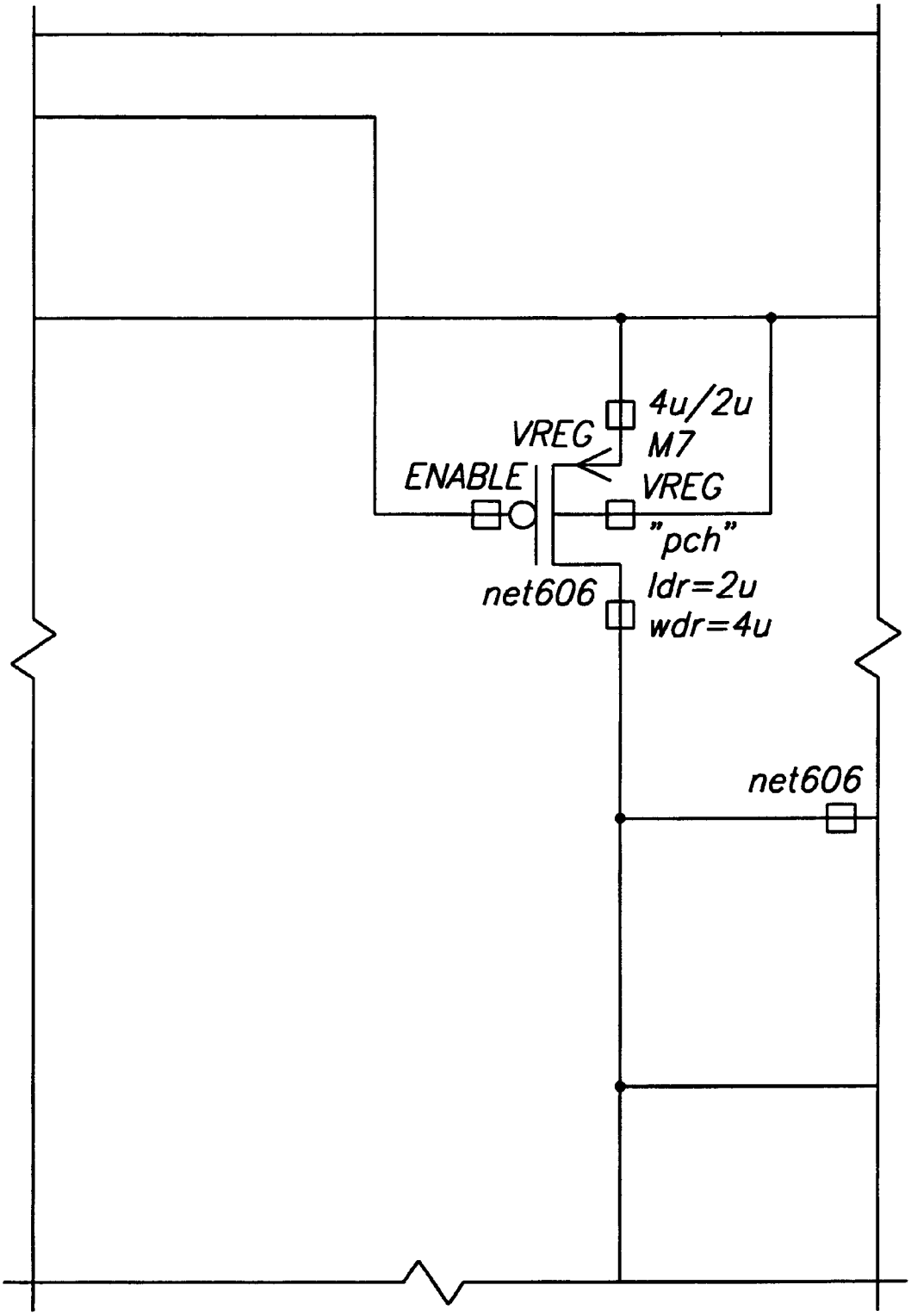


Fig 8.0504.02AE

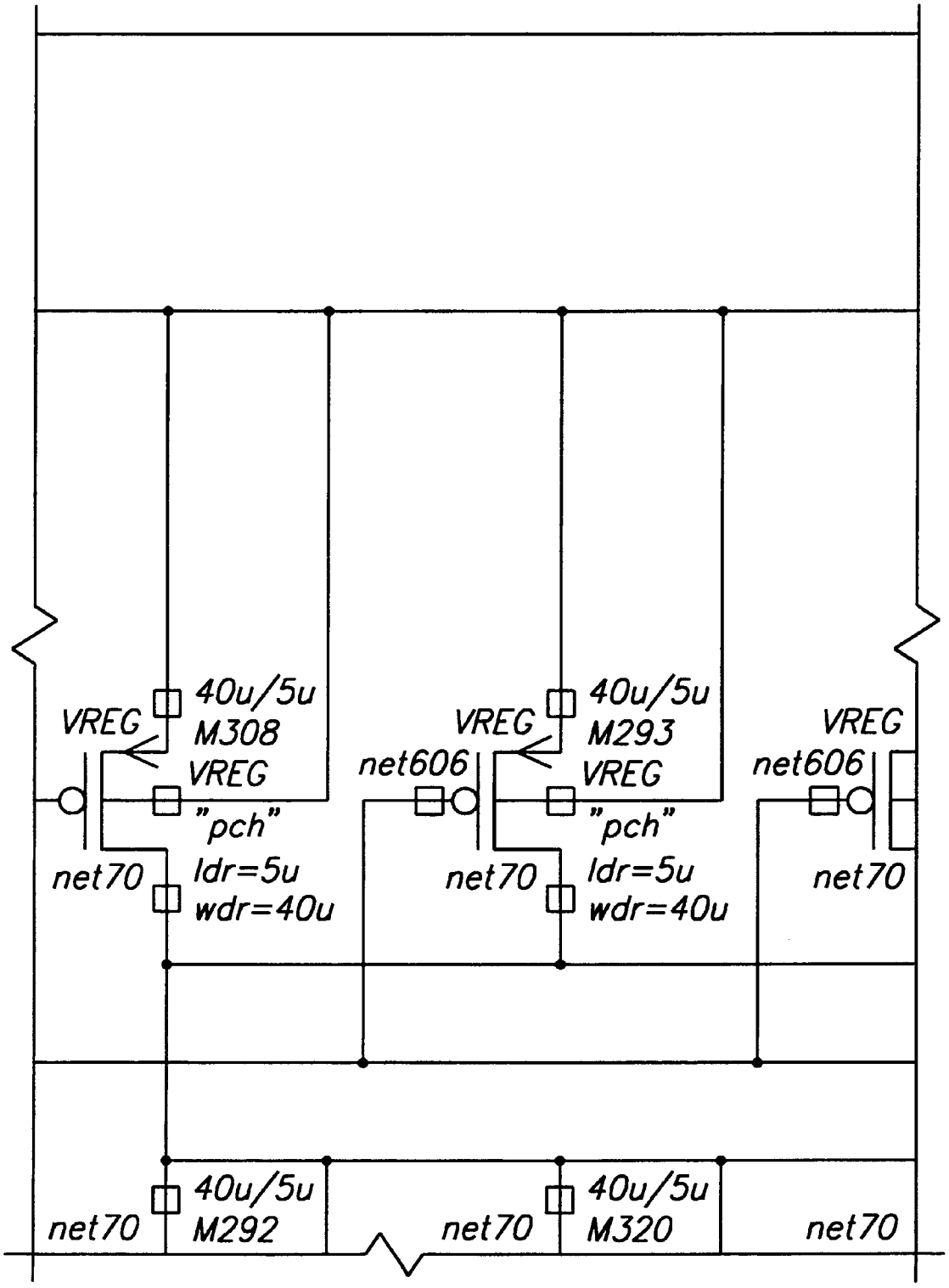
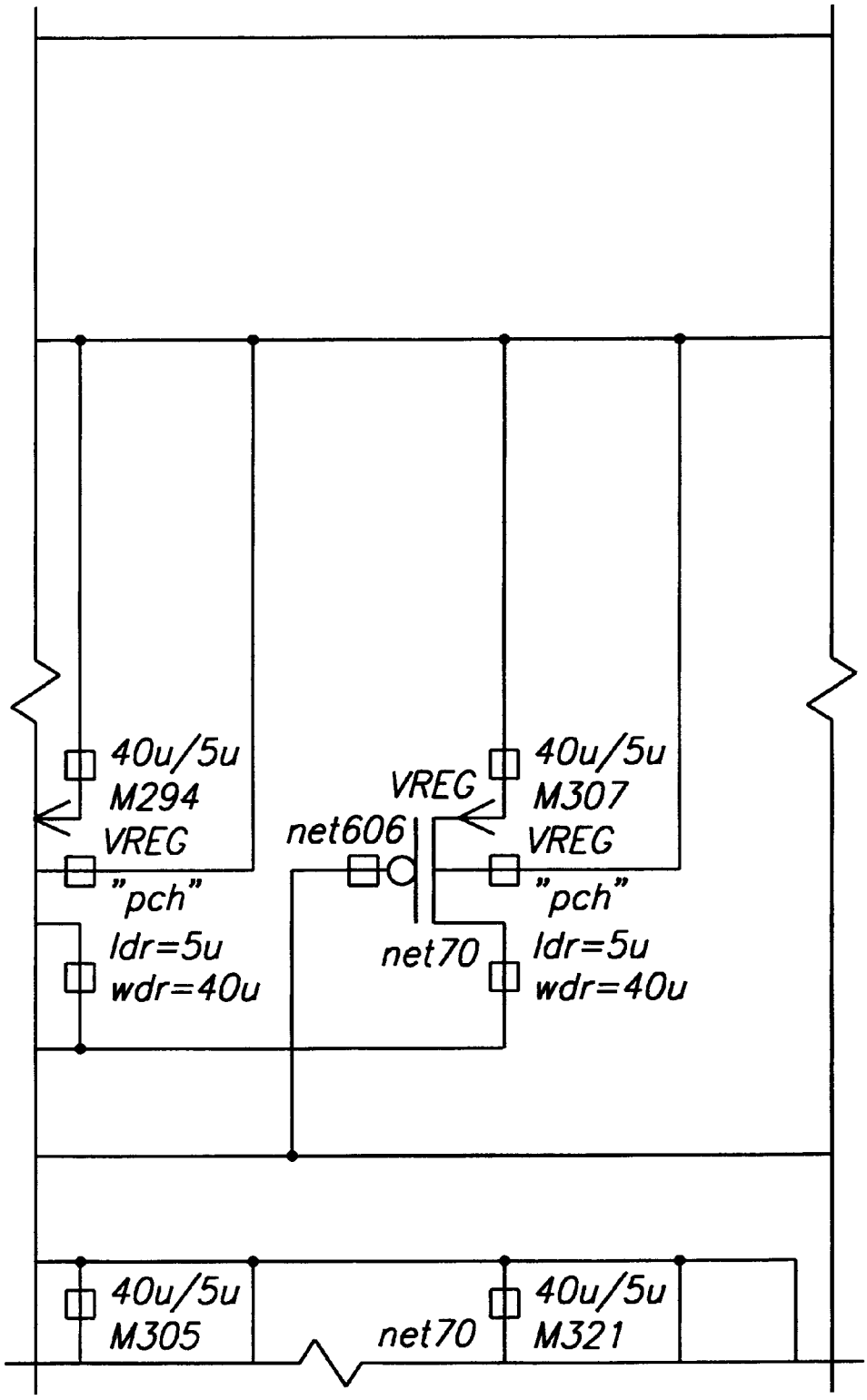


Fig 8,050,402AF



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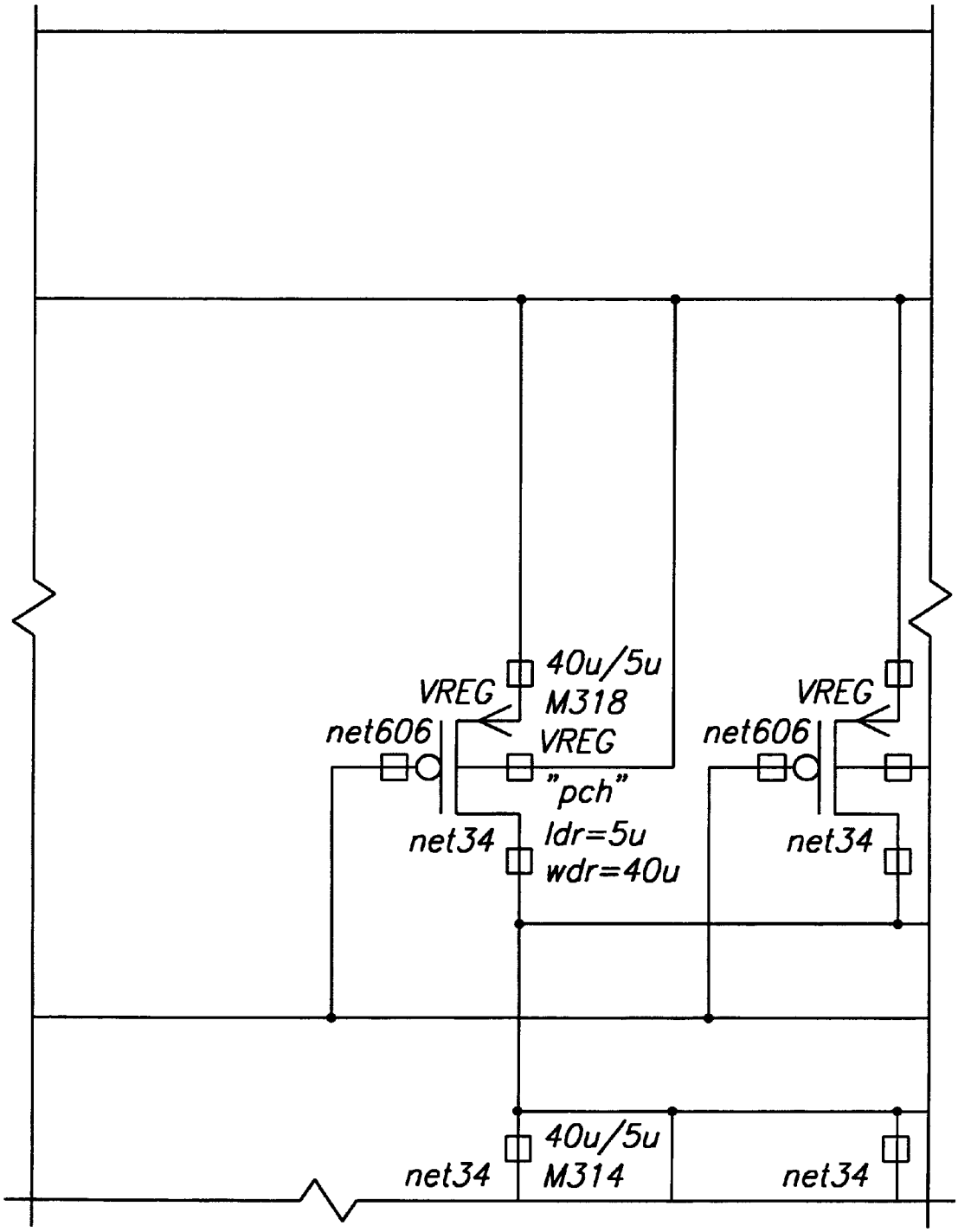


Fig 8.0504.02AH

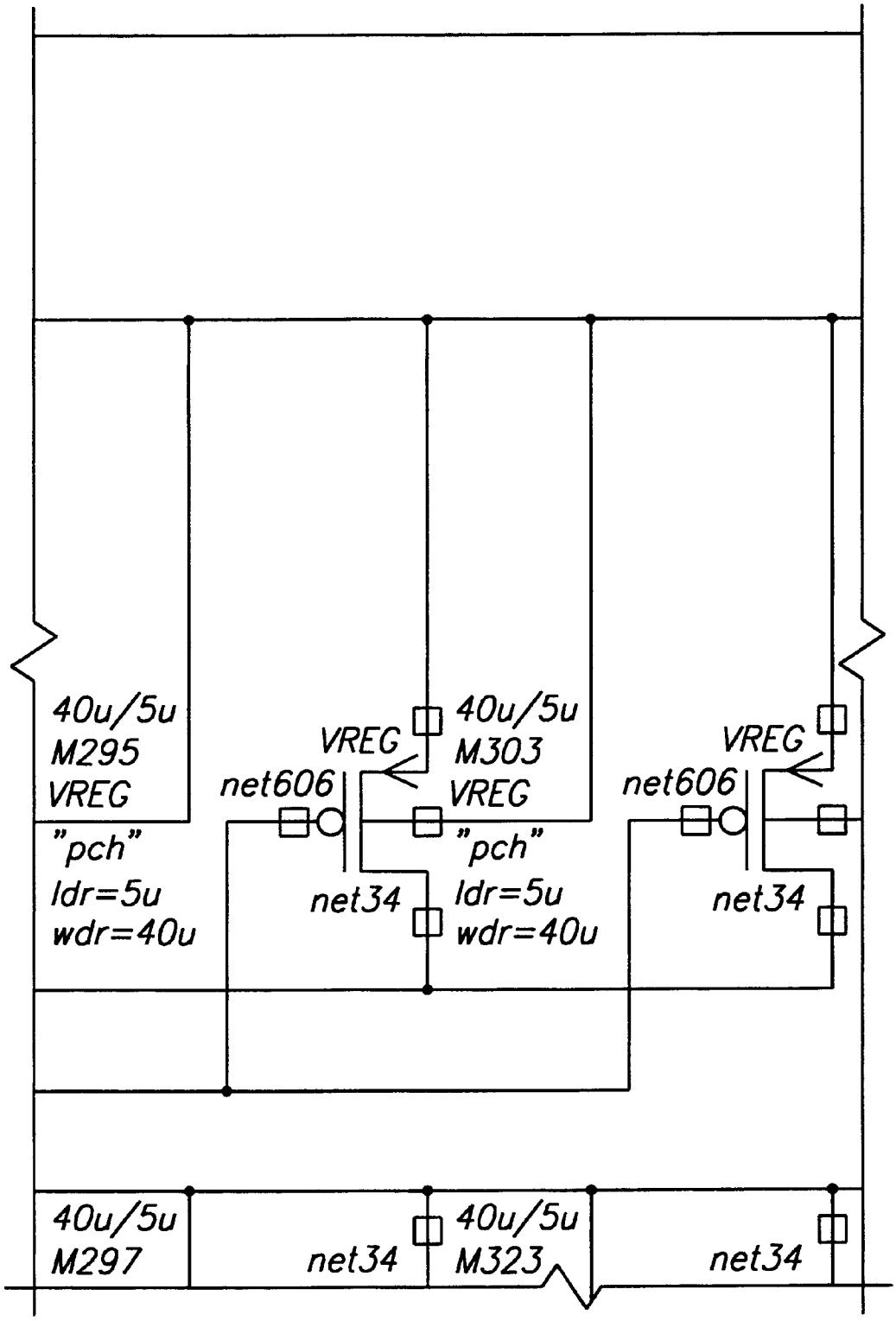


FIG 88.0500402AII

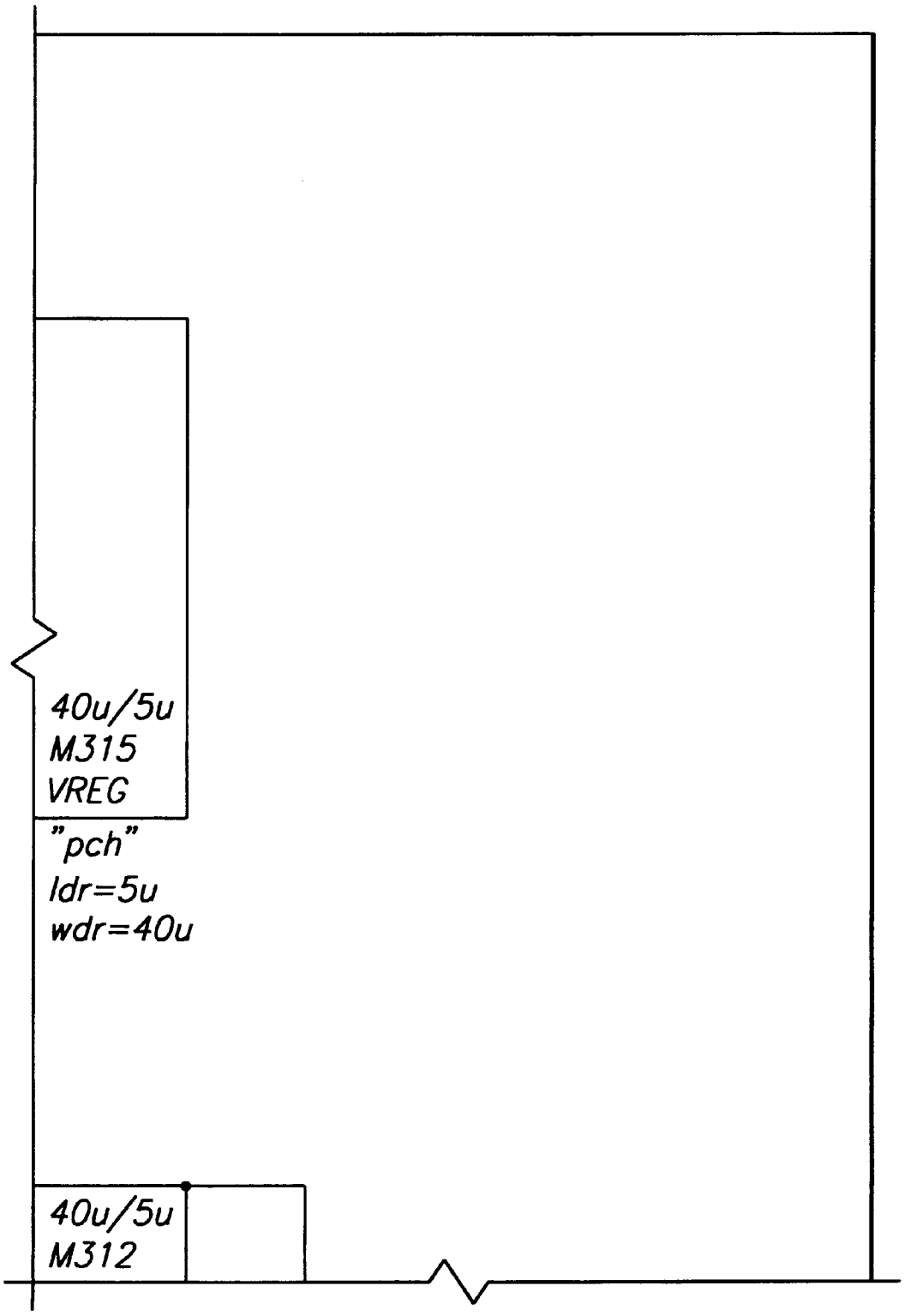


Fig 8.0504.02Ad

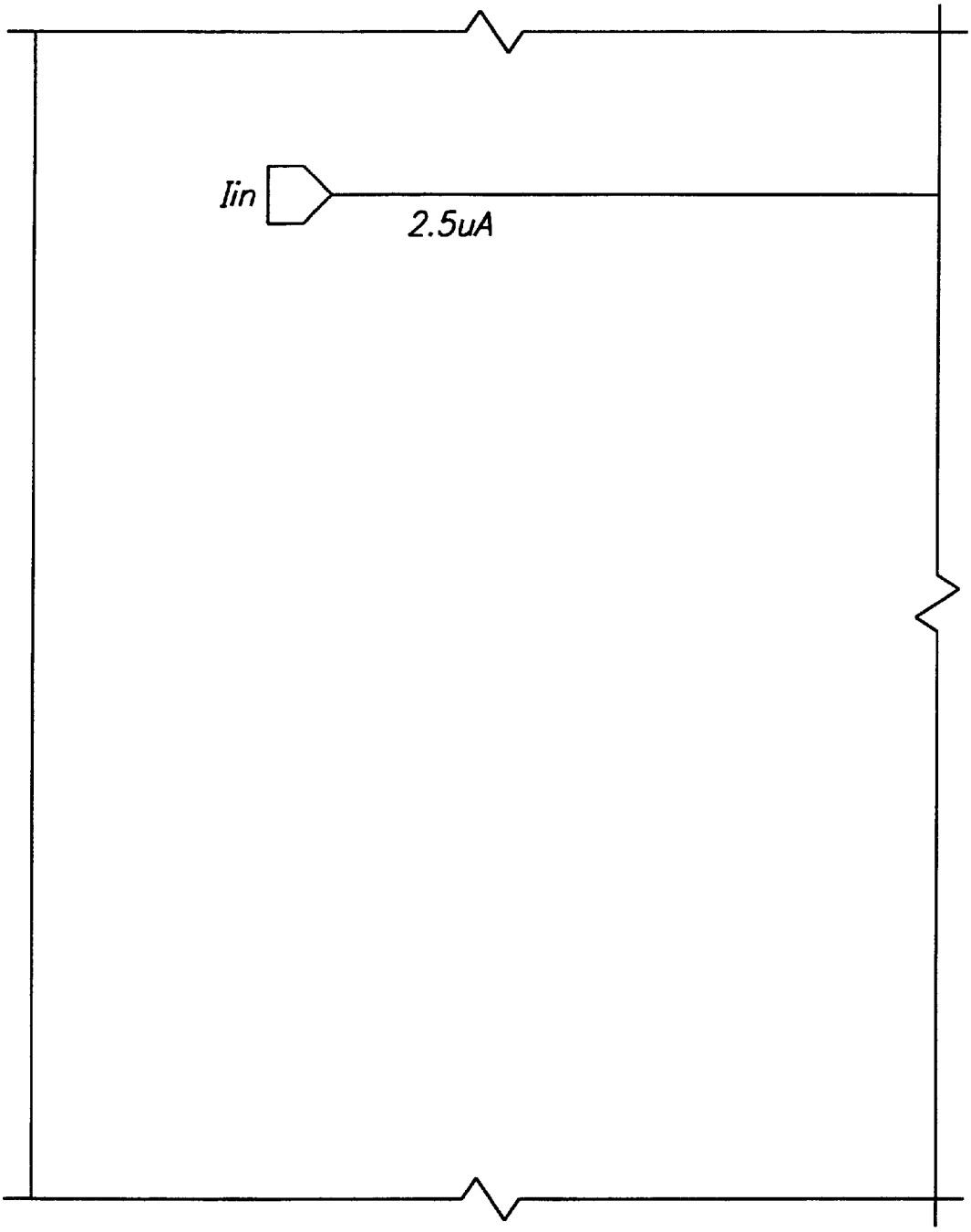


Fig 8.0504028A

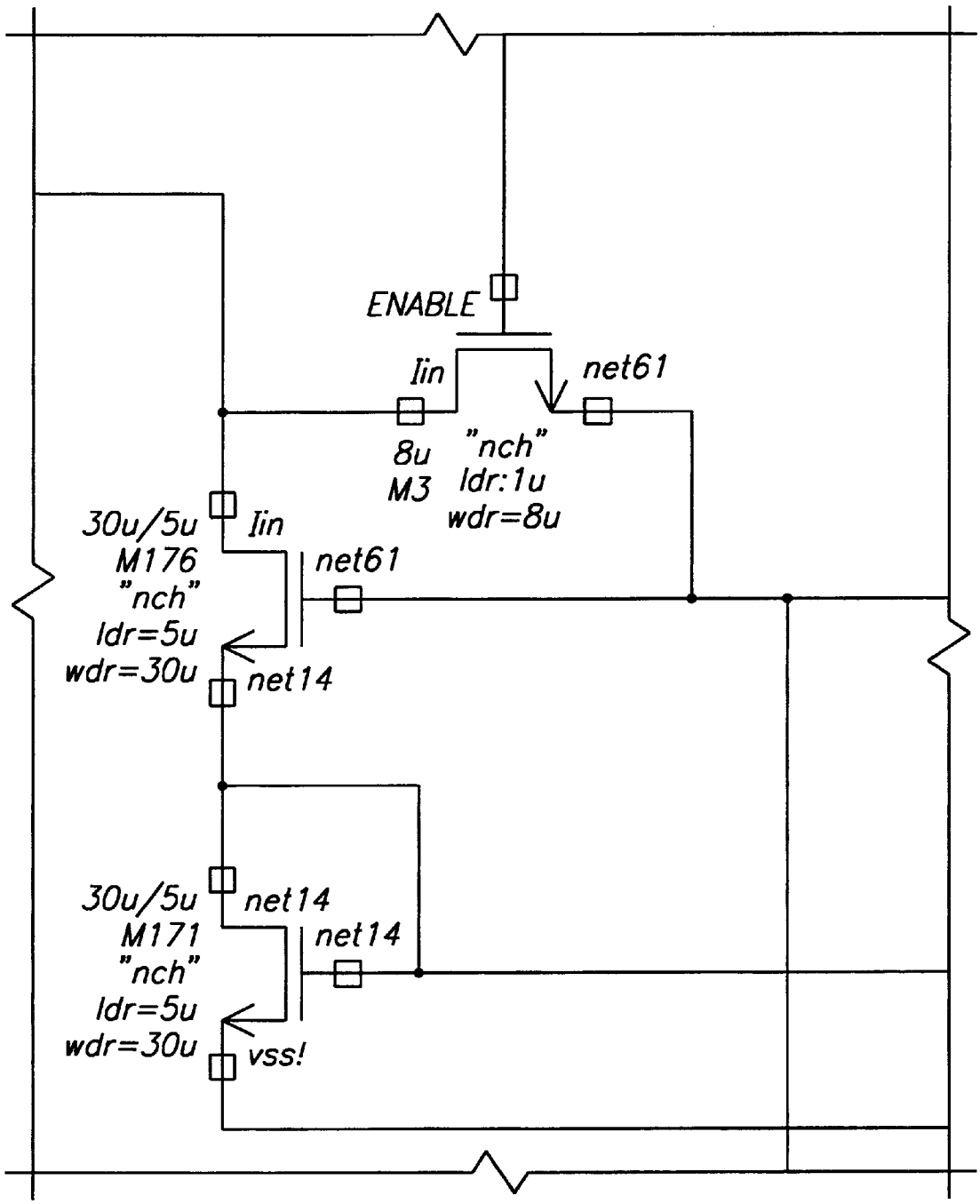


Fig 8,050,402BB

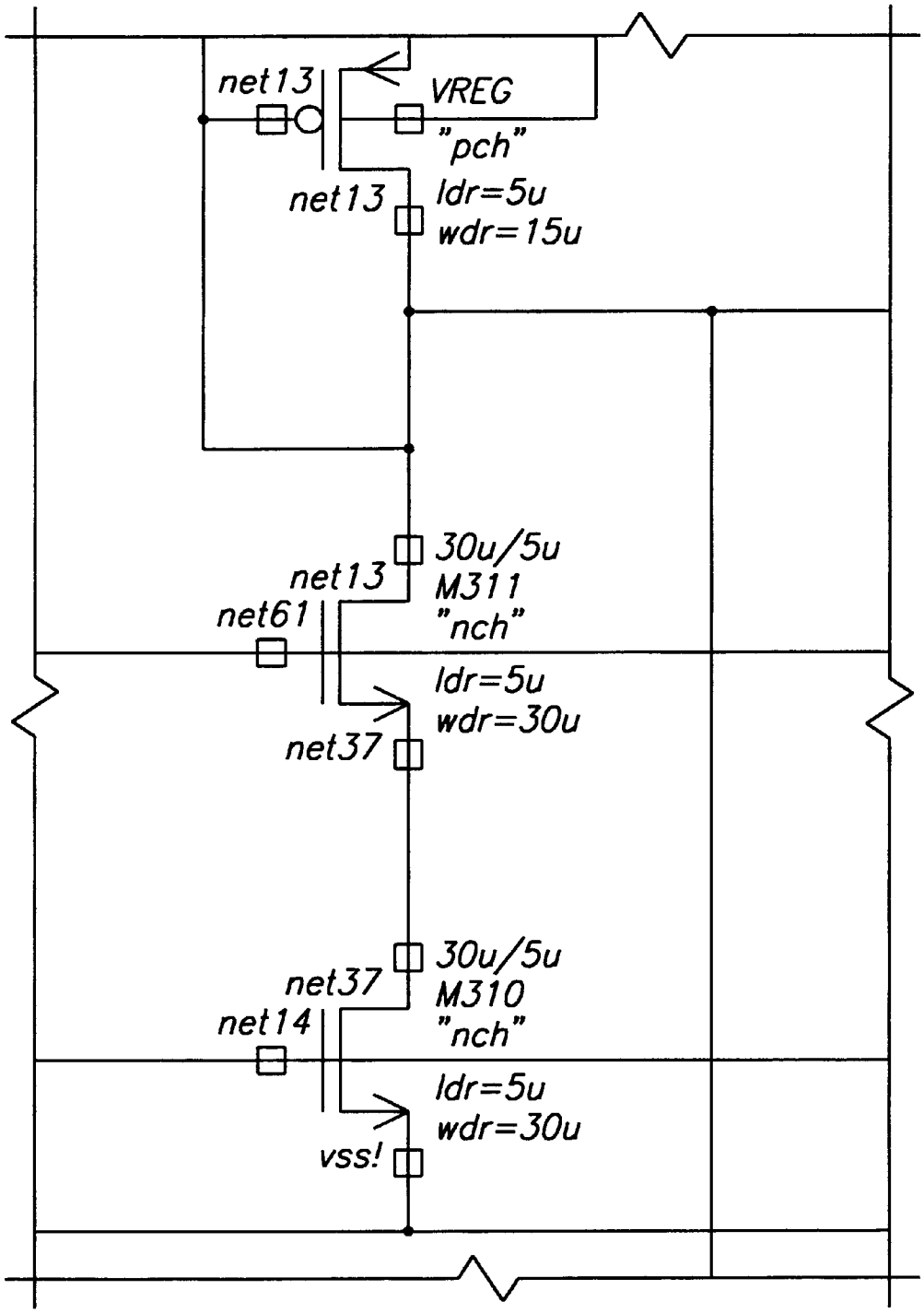


Fig 8,050,402BC

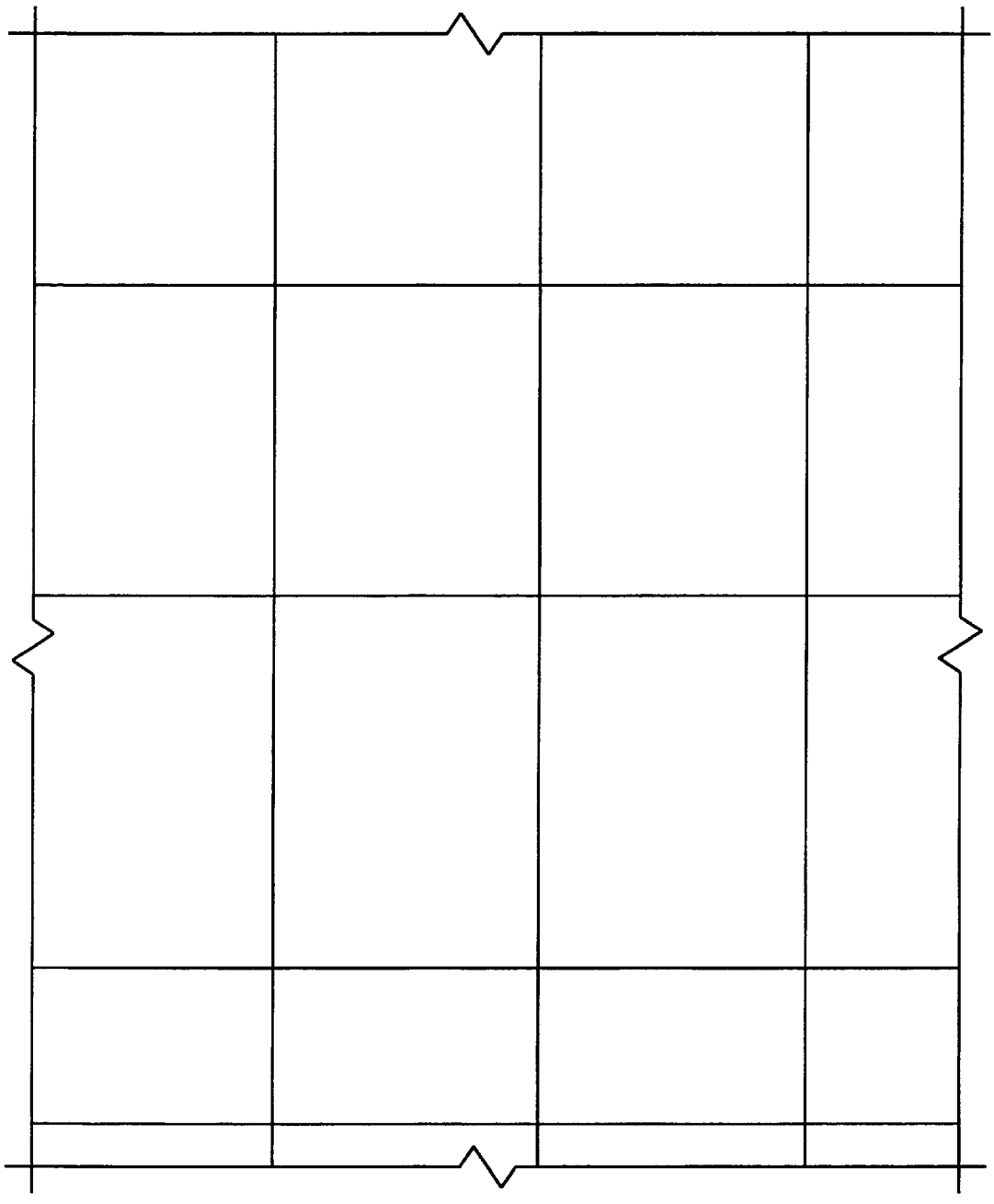


Fig 8.0504002BD

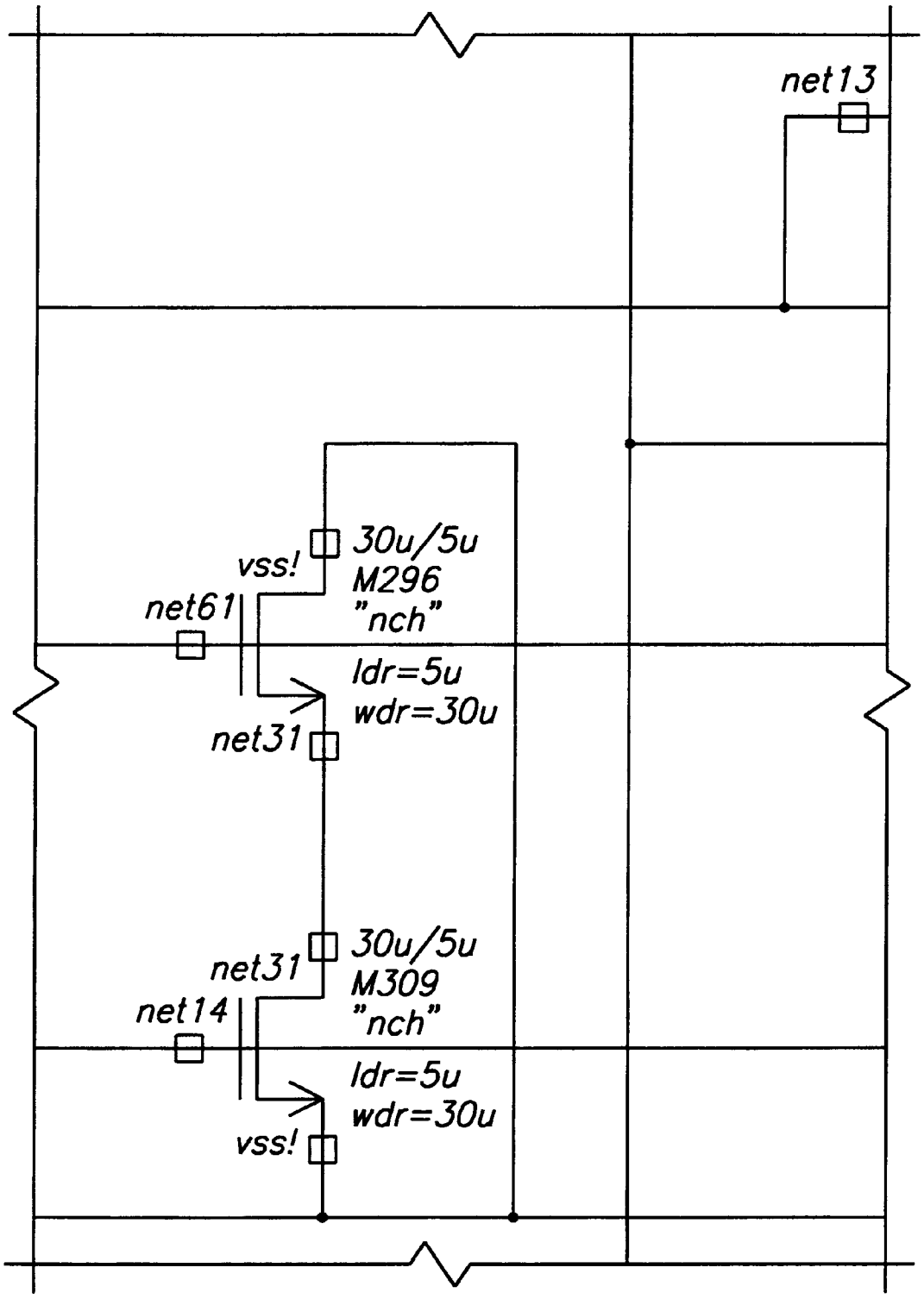
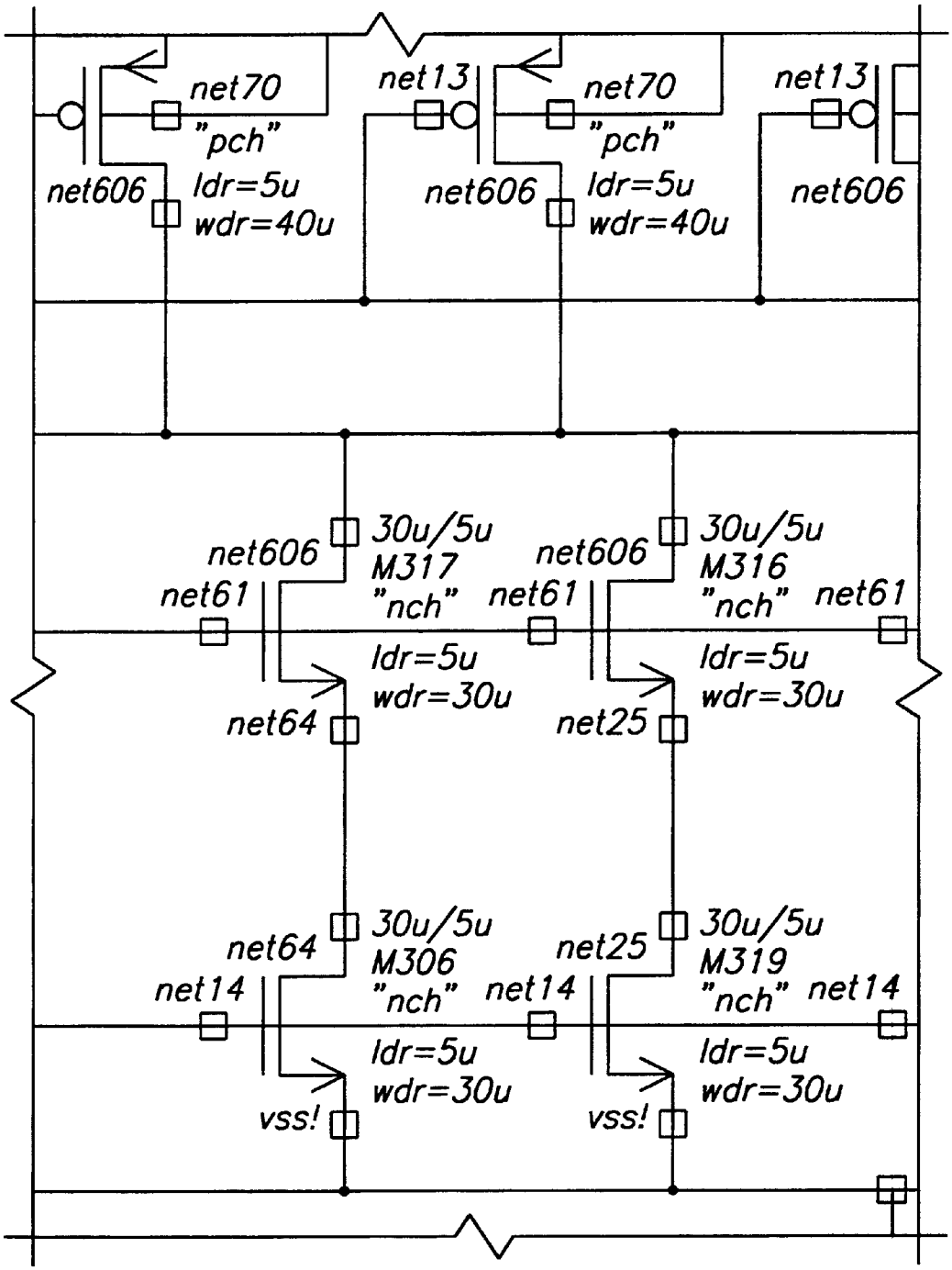


FIG 8,050,402BE



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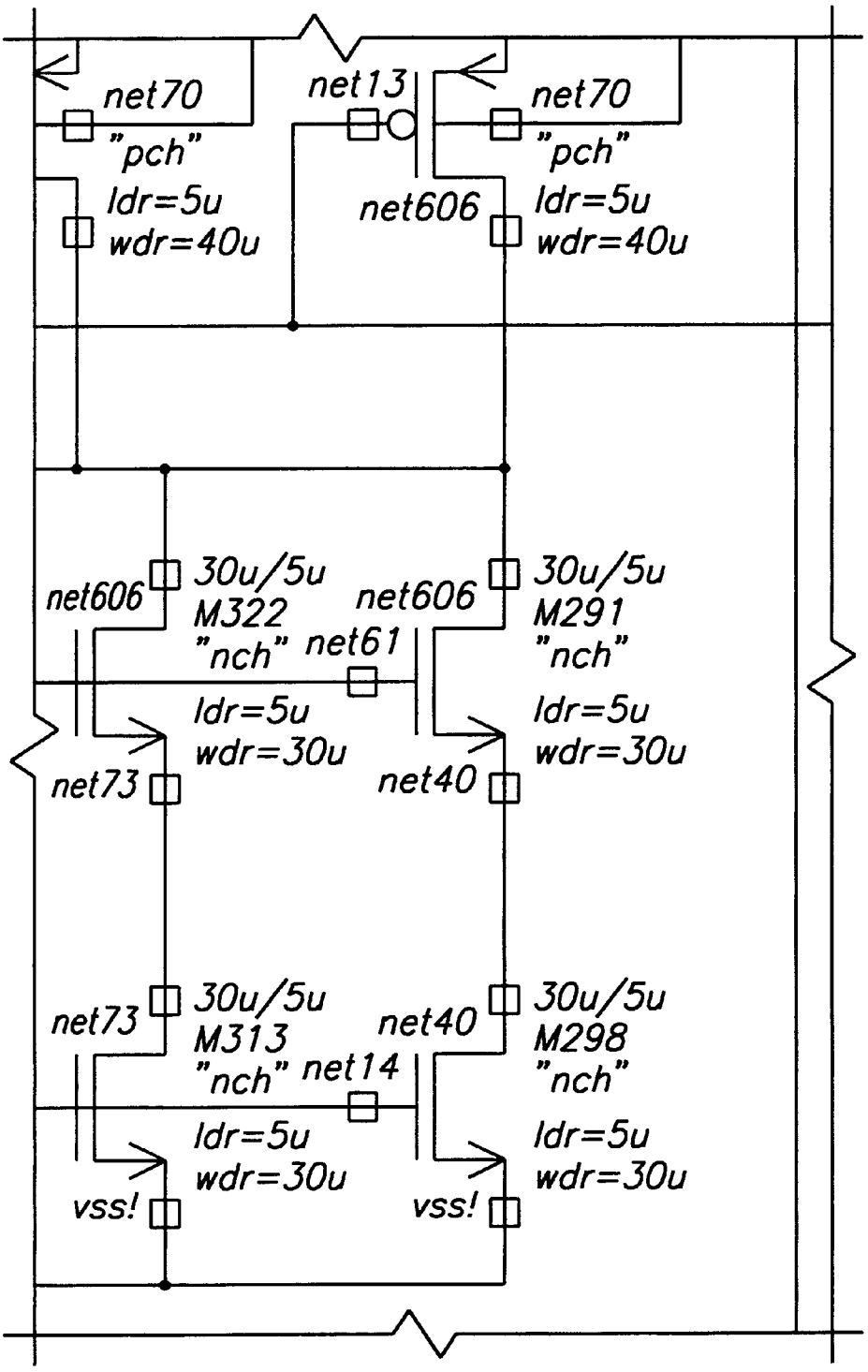
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Fig 6,130,602

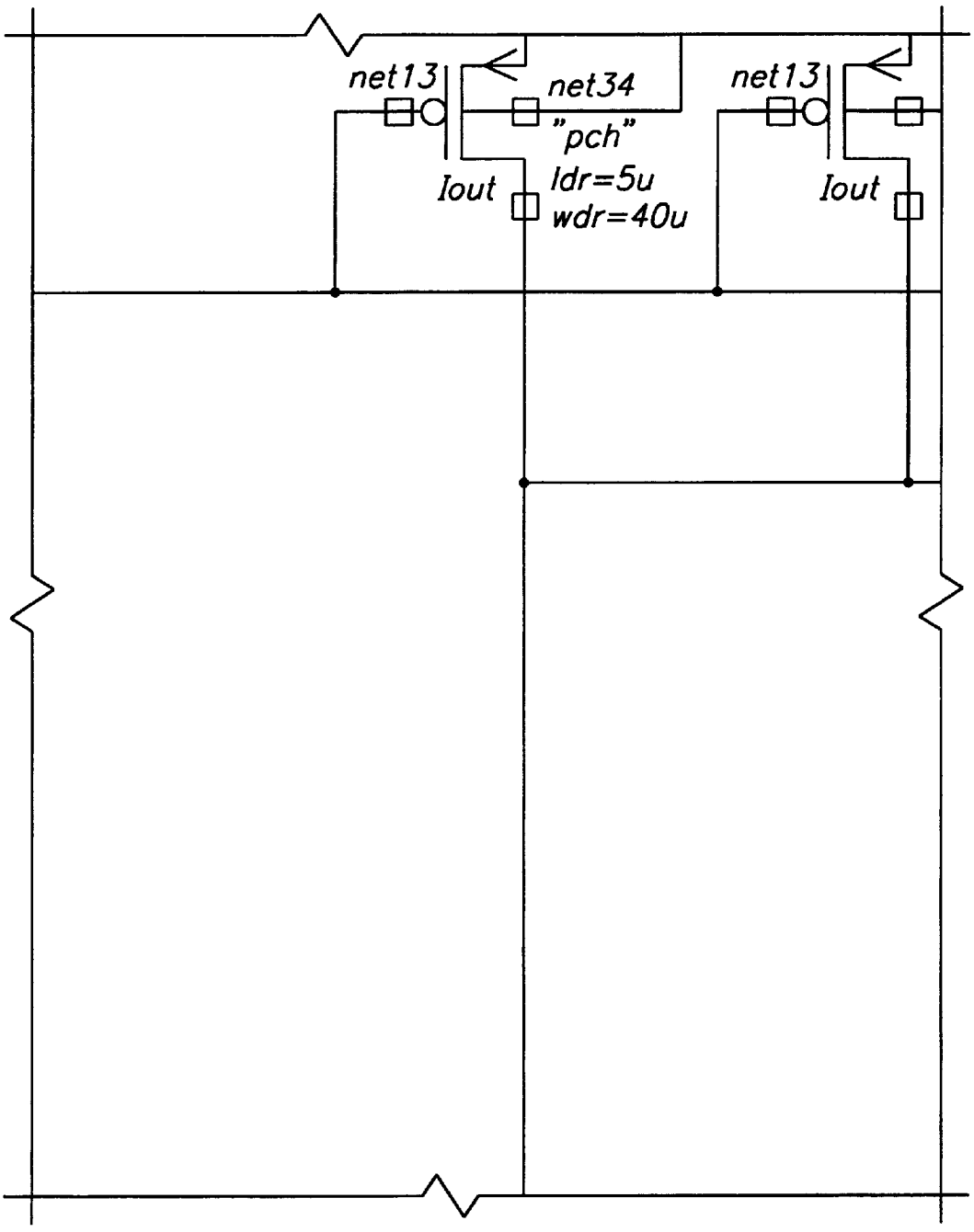


Fig 8.0504028H

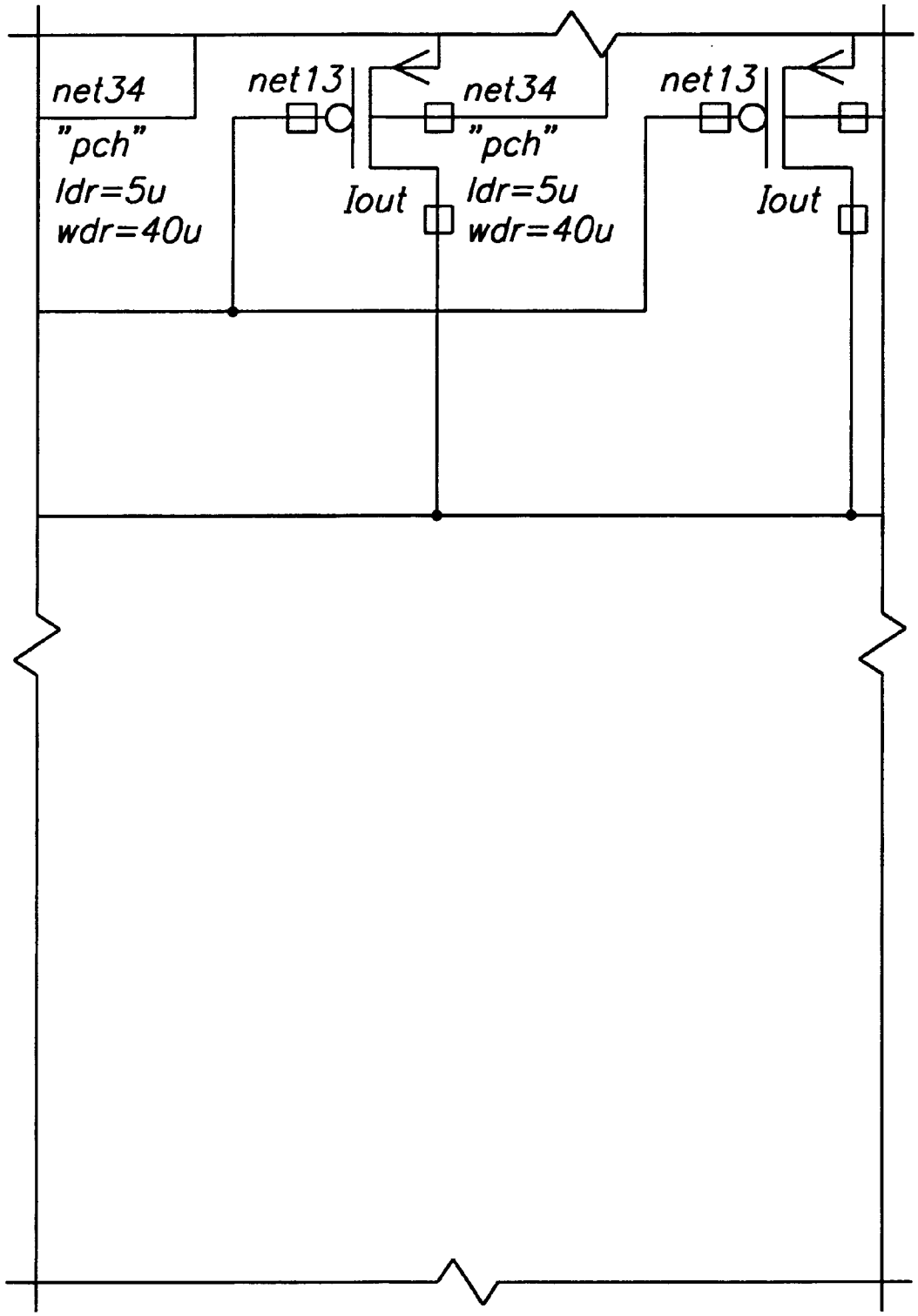


Fig 8,050,402B1

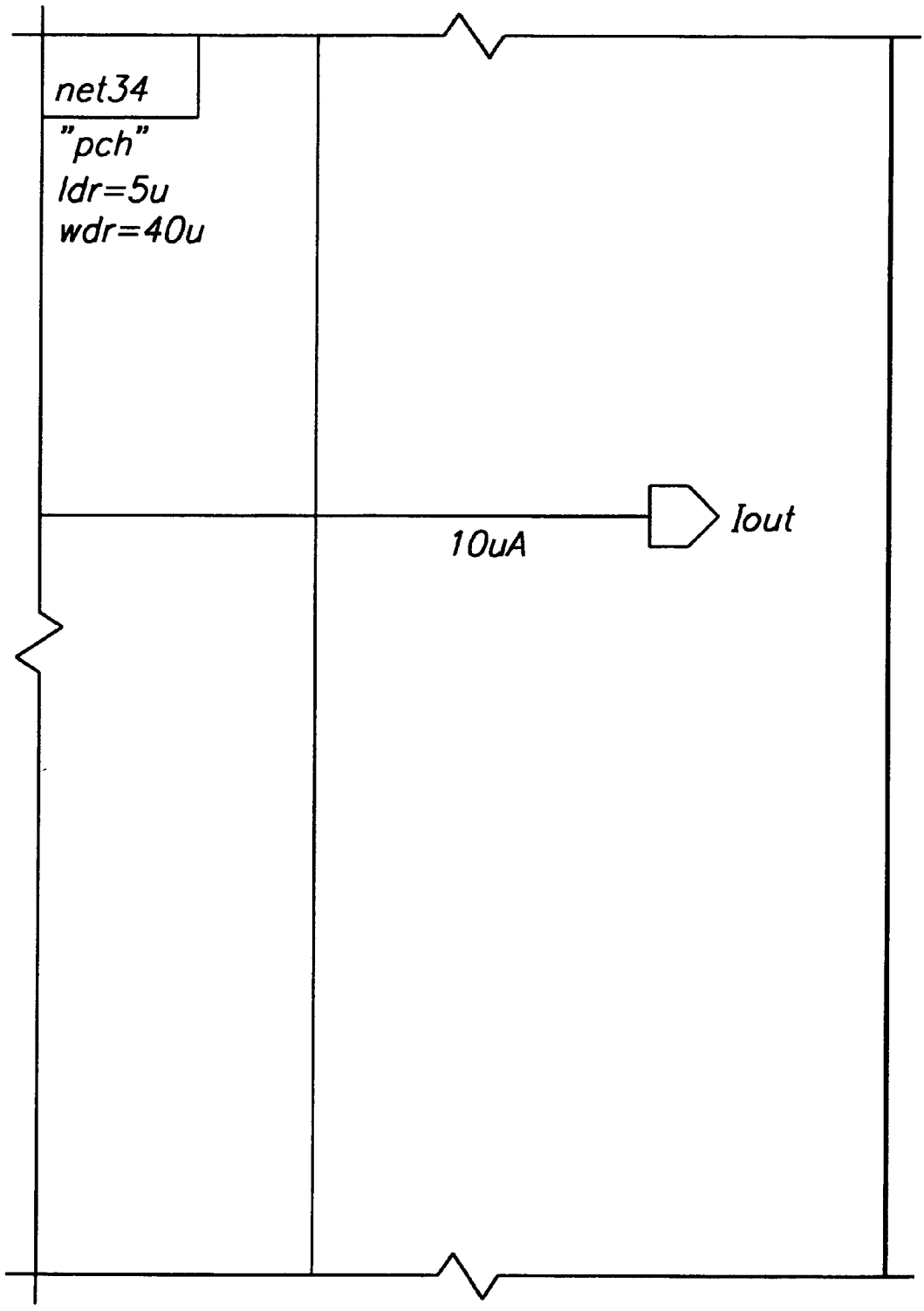


Fig 8,050,402B1

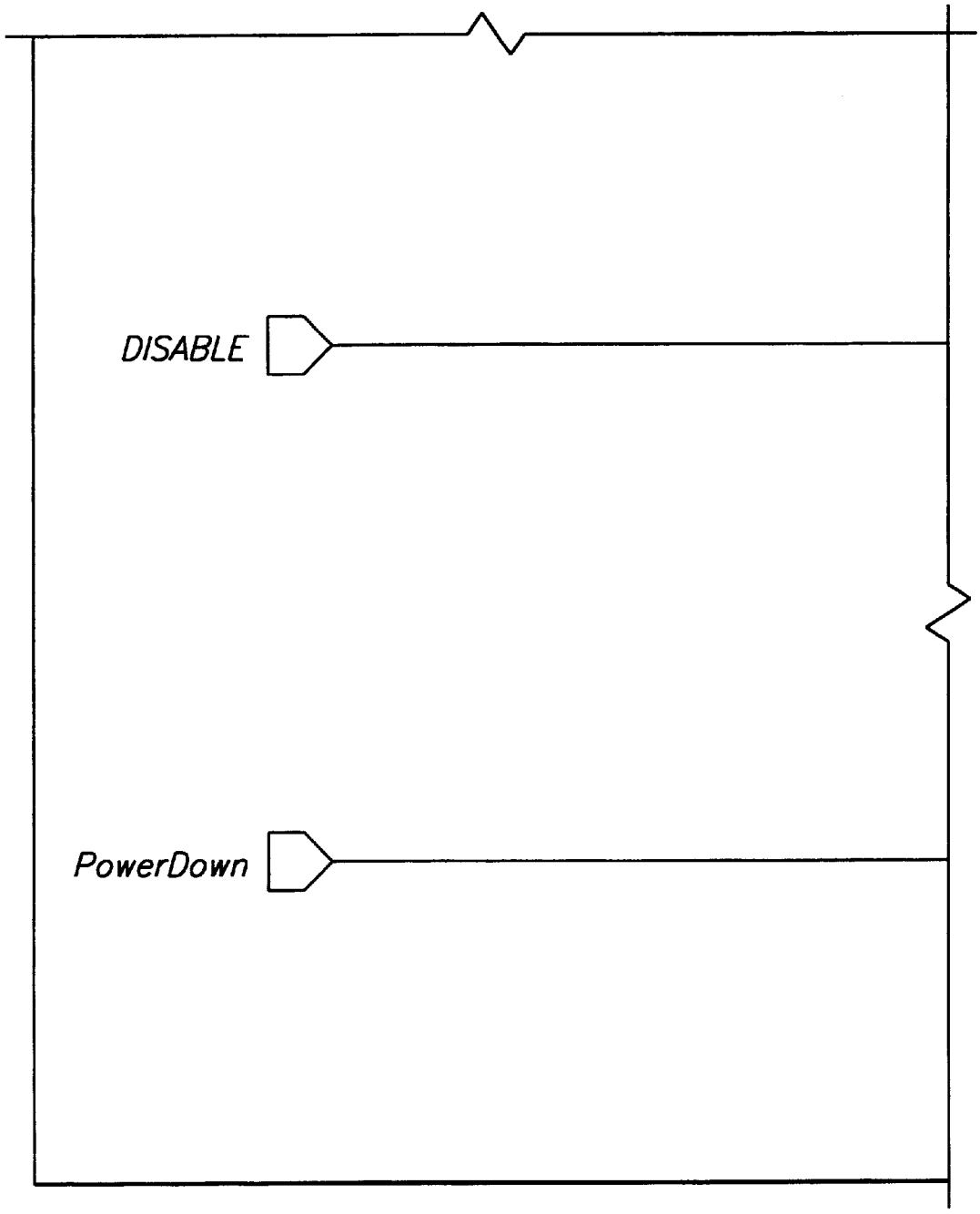


Fig 8.0504.02CA

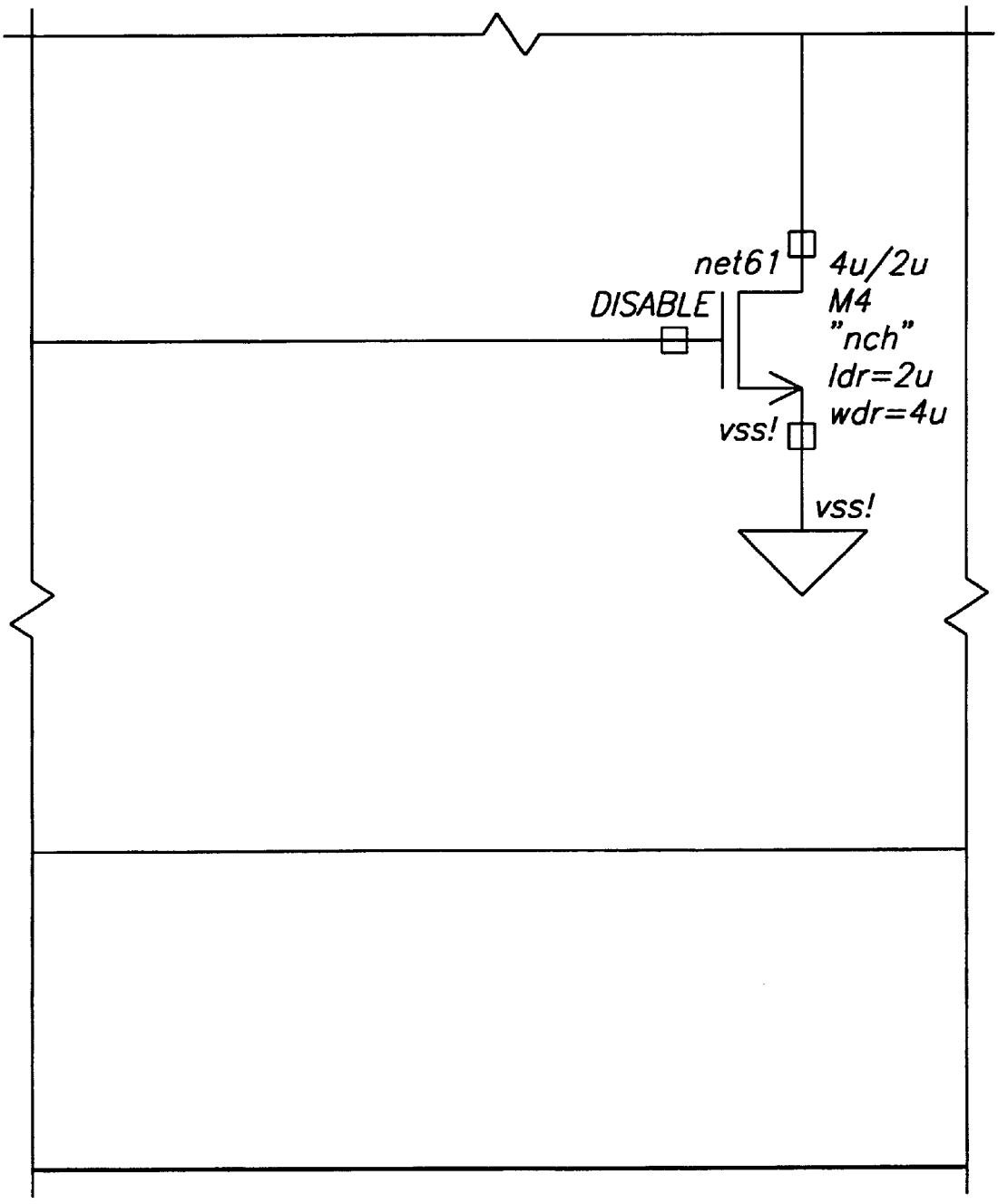
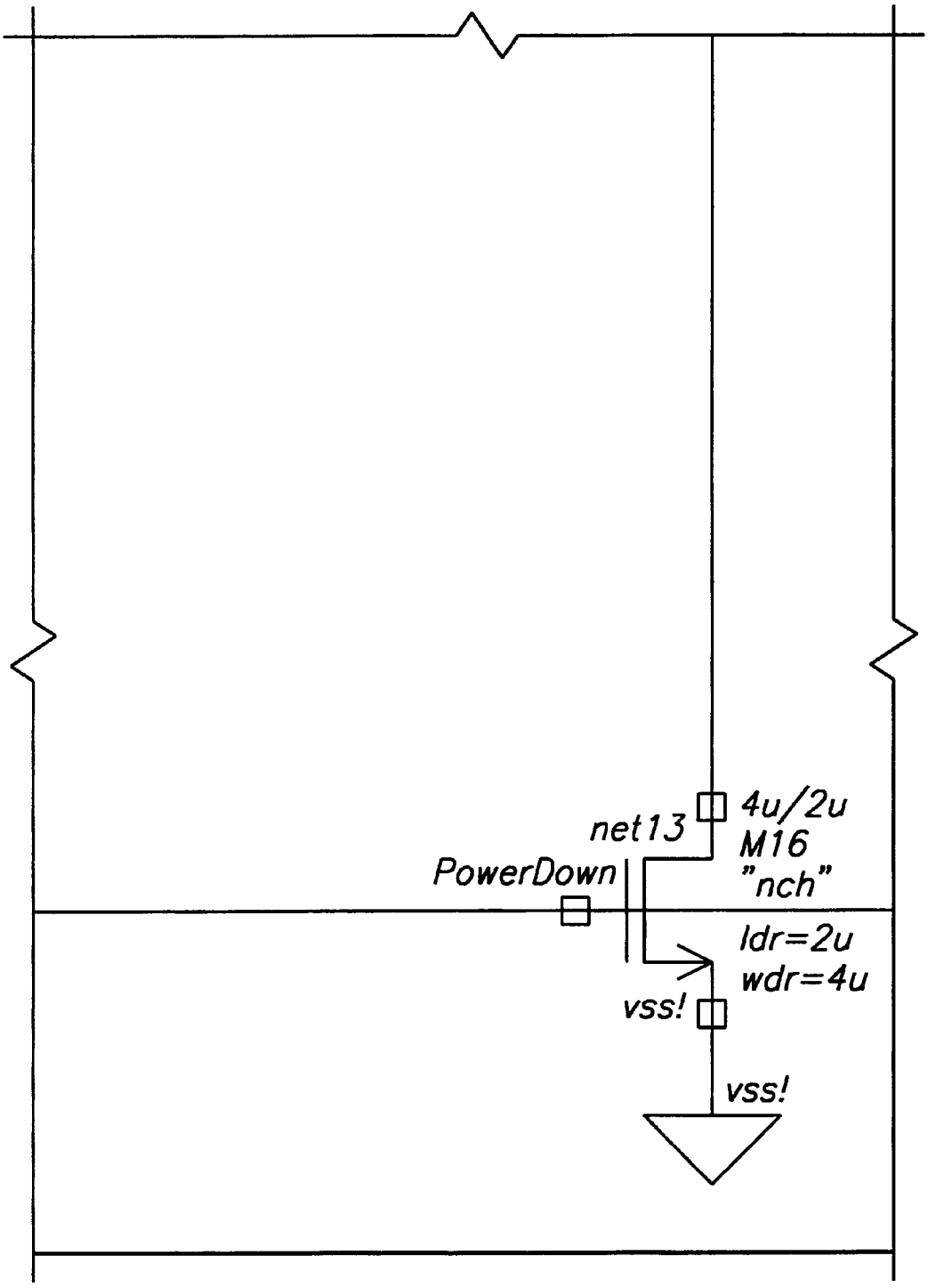


Fig 8.0504402CB



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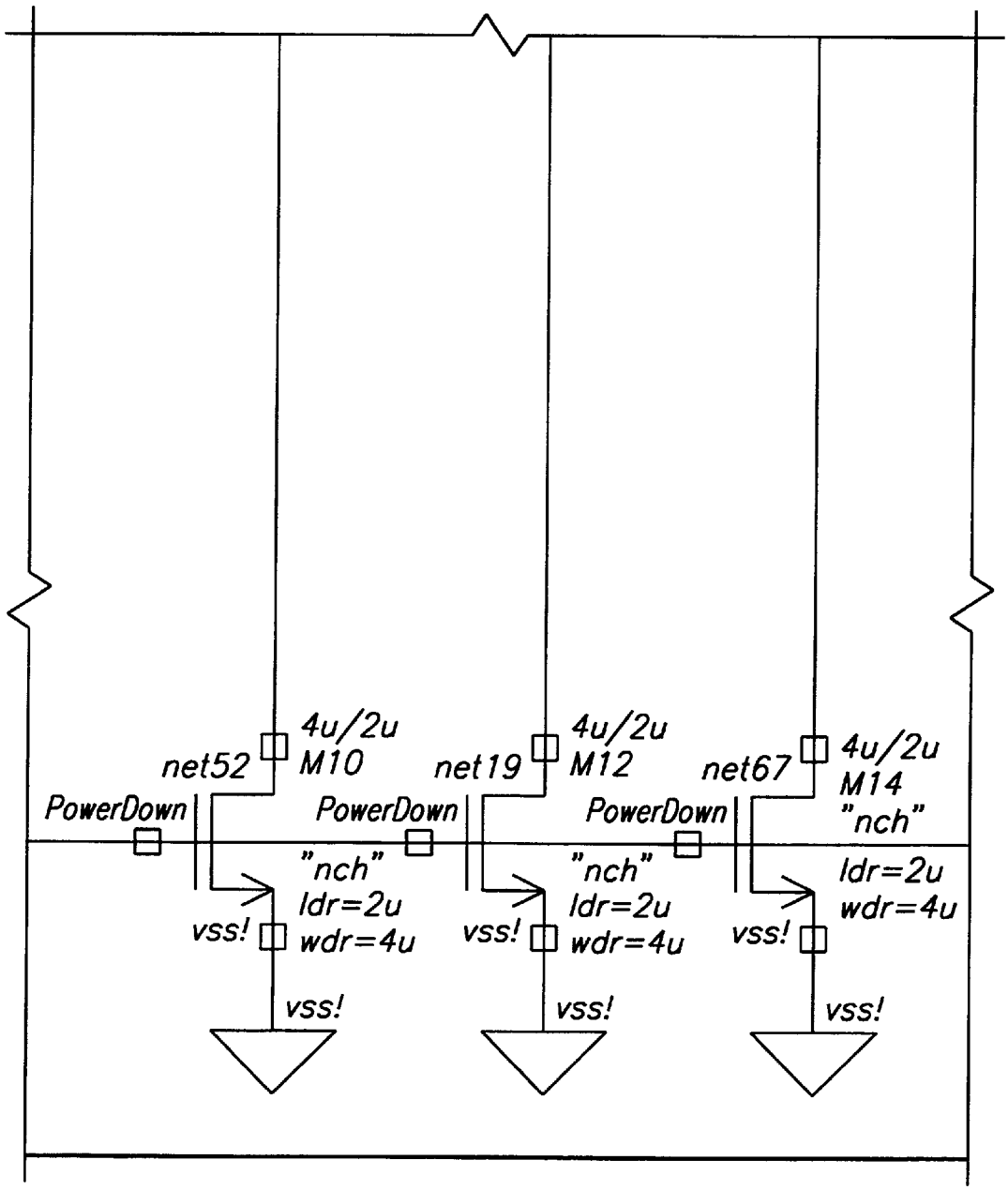


Fig 8,050,402CD

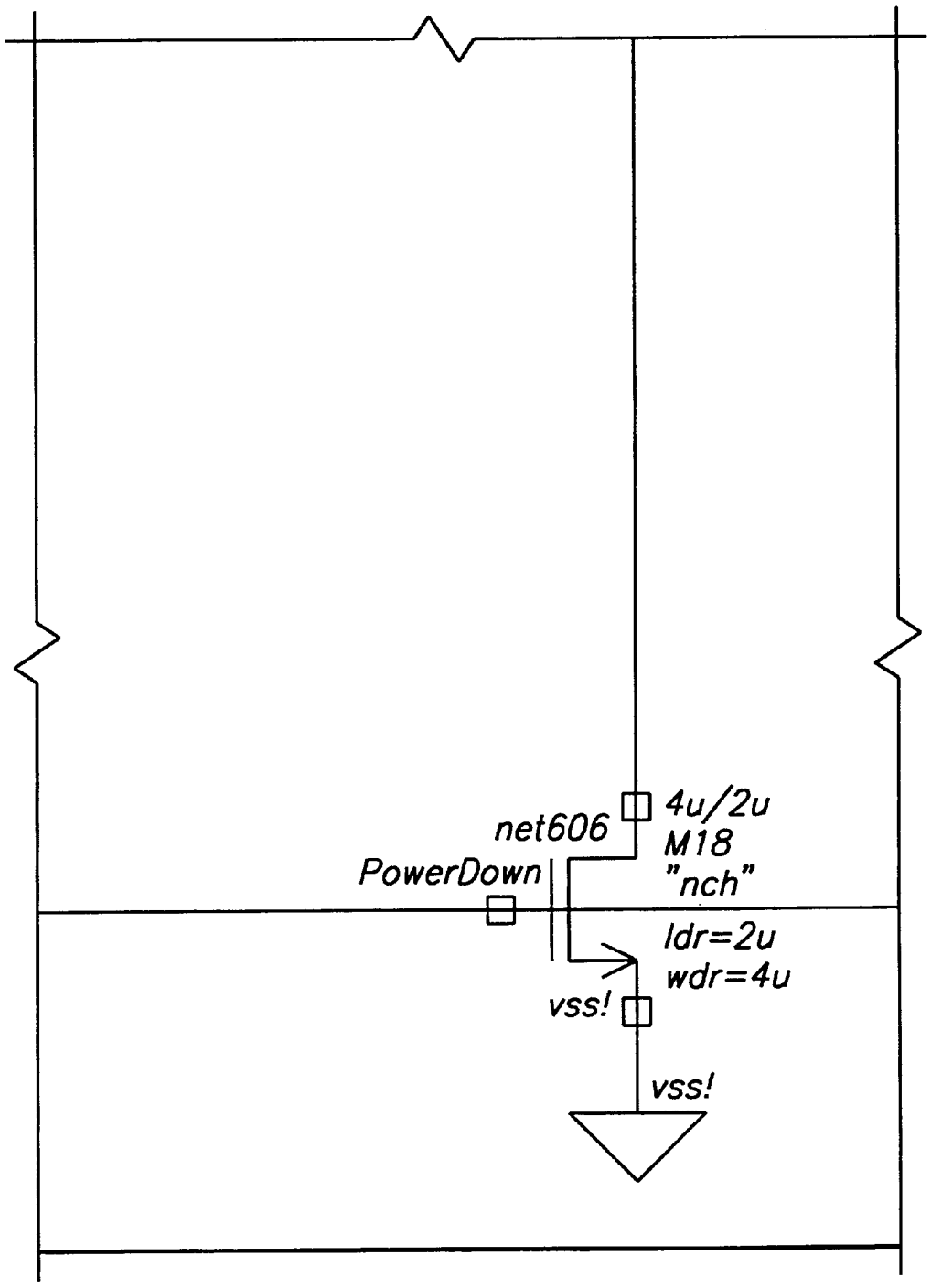


Fig 8.0504020E

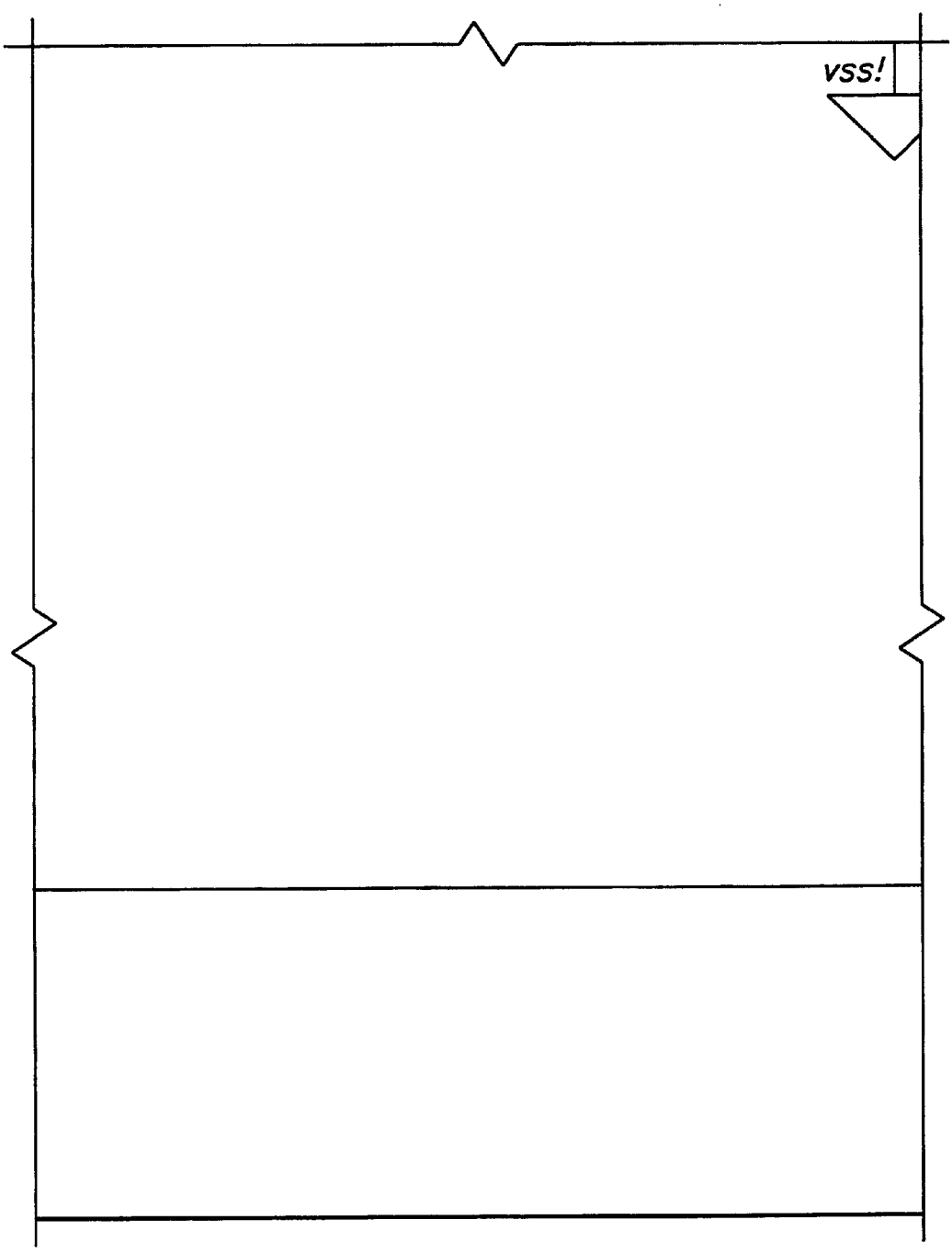


Fig 8.0504002CF

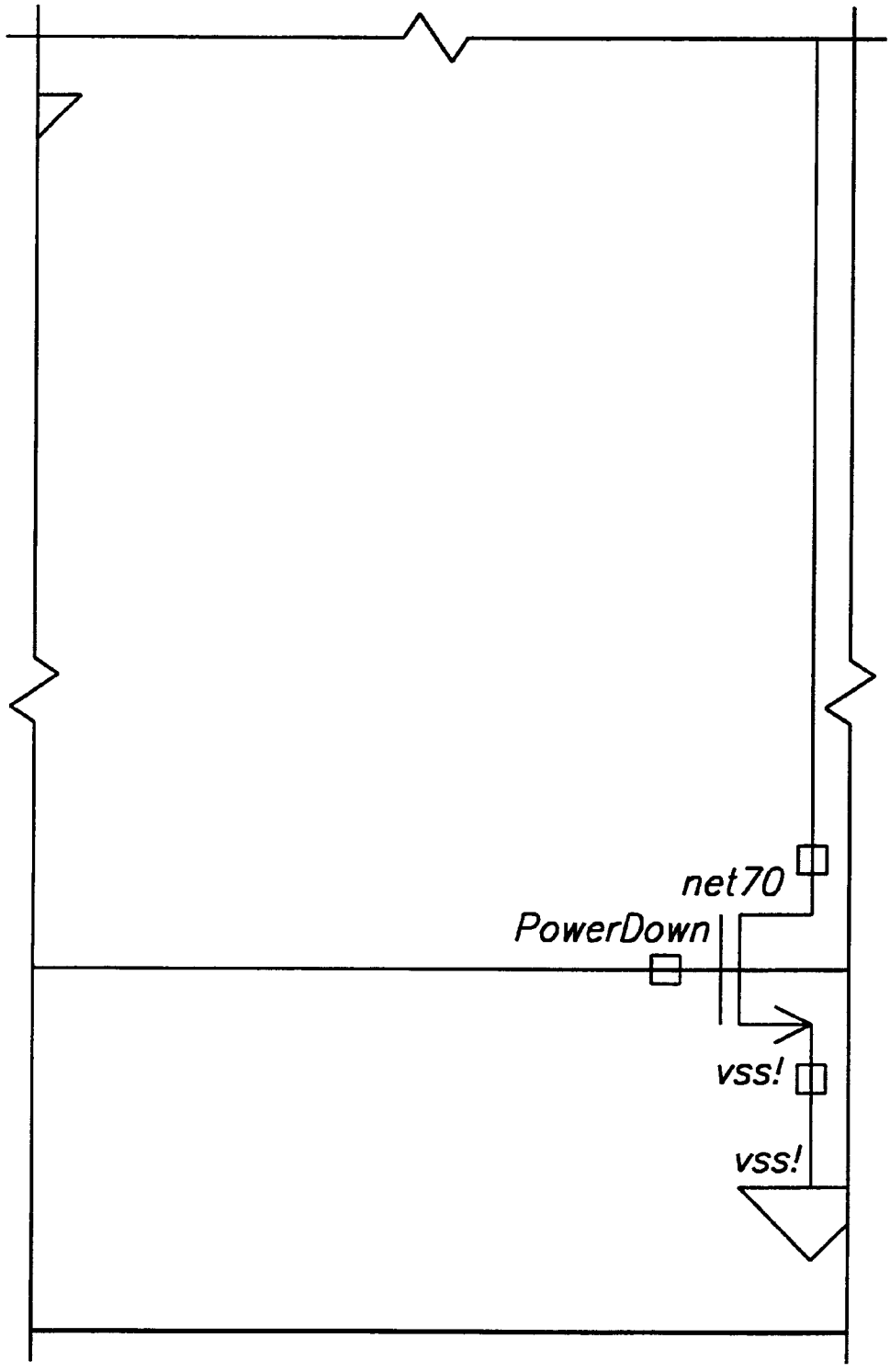


Fig 8.0504026

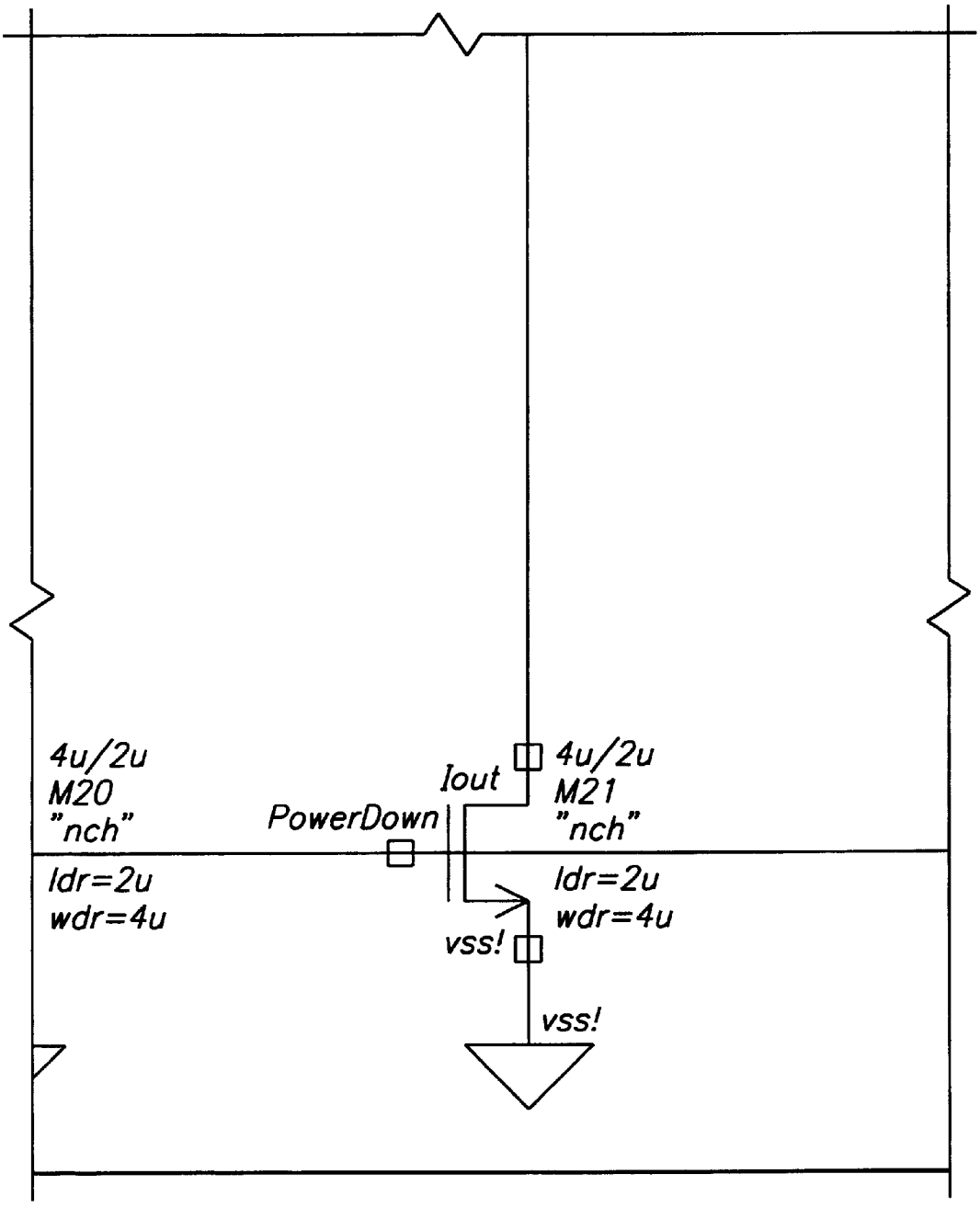


Fig 8,050,402CH

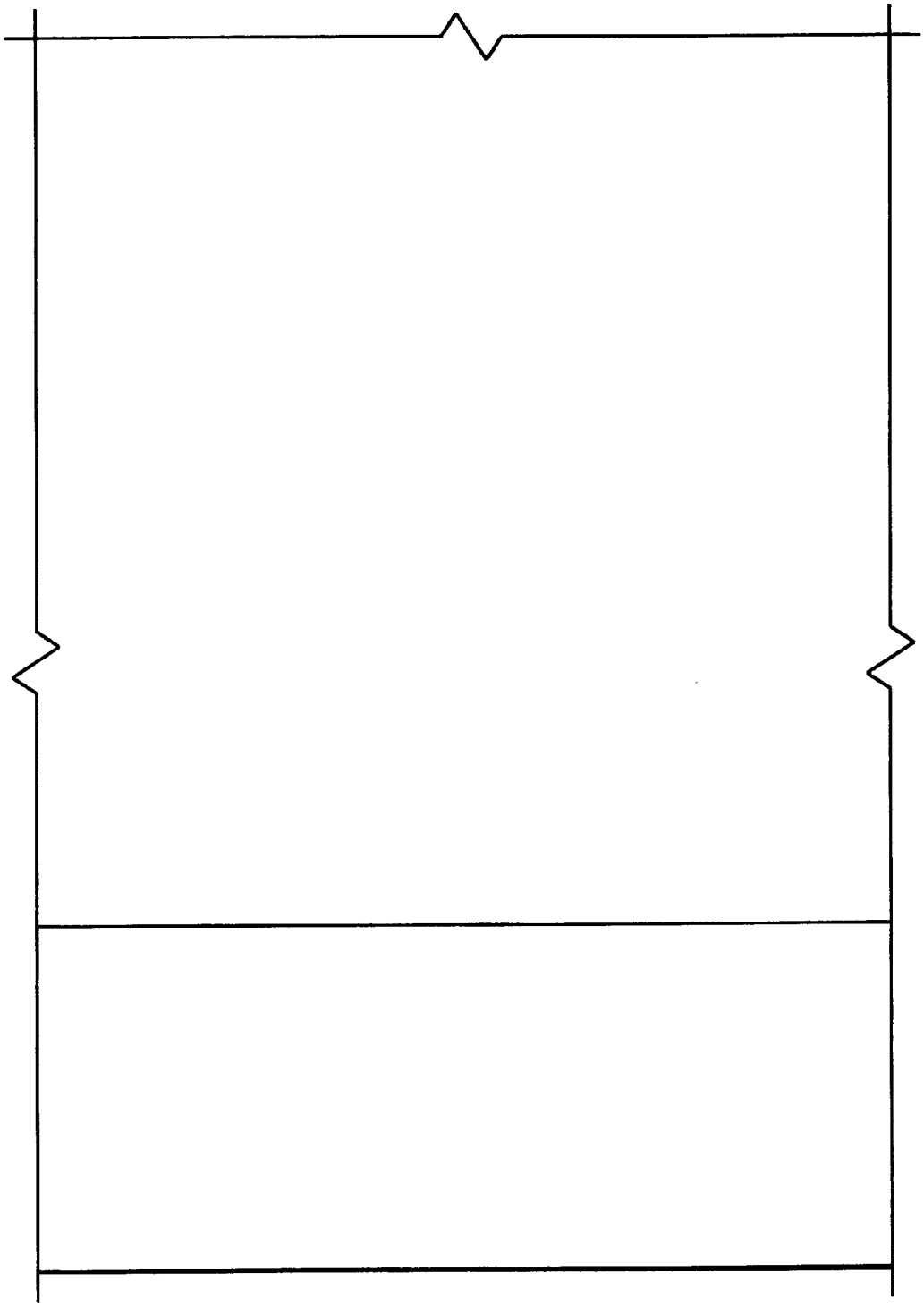


Fig 8.05040201

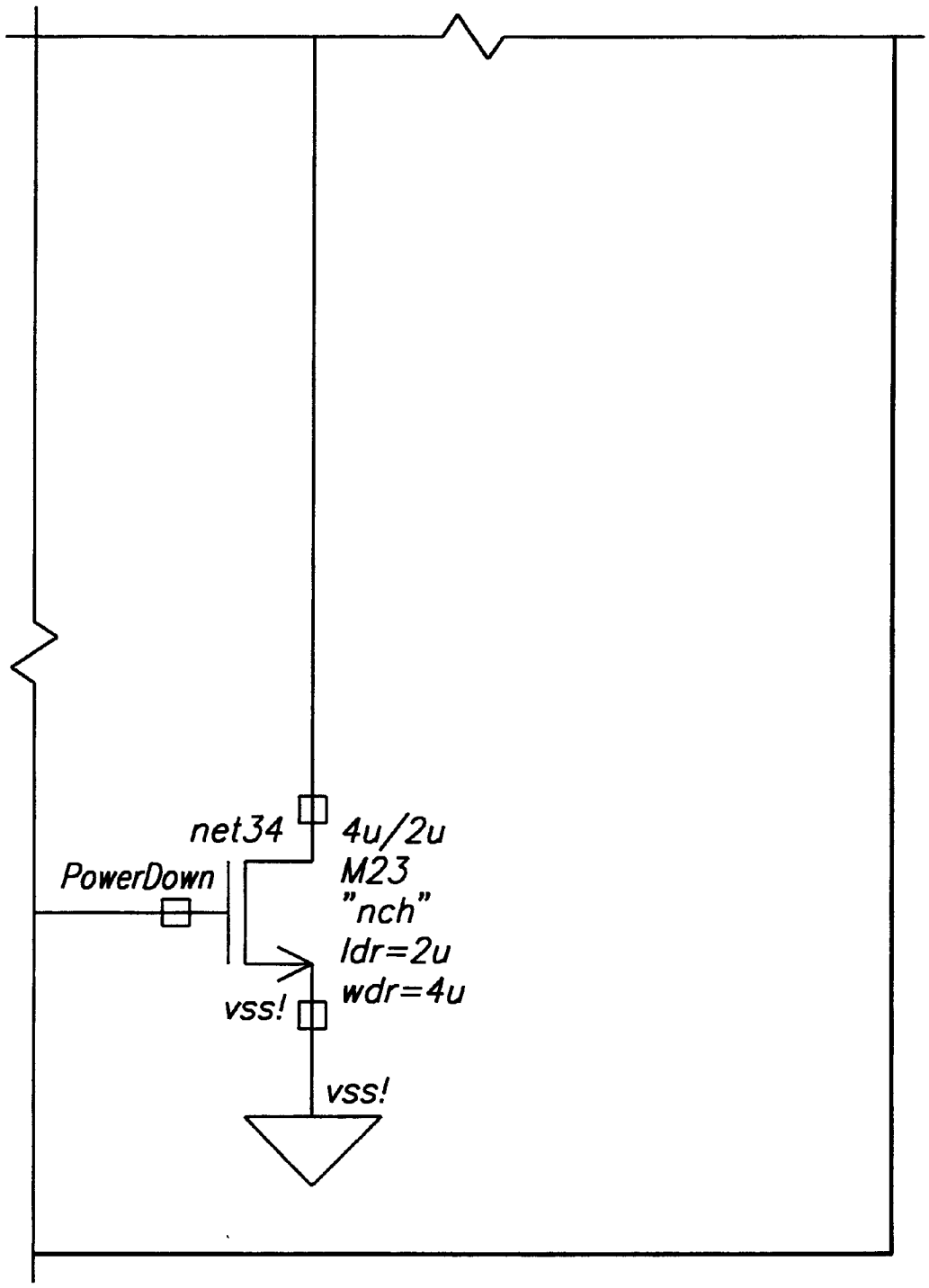


Fig 8,050,402C1

8.050403AA	8.050403AB	8.050403AC	8.050403AD	8.050403AE	8.050403AF	8.050403AG	8.050403AH	8.050403AI
8.050403BA	8.050403BB	8.050403BC	8.050403BD	8.050403BE	8.050403BF	8.050403BG	8.050403BH	8.050403BI

FIG. 8.0503

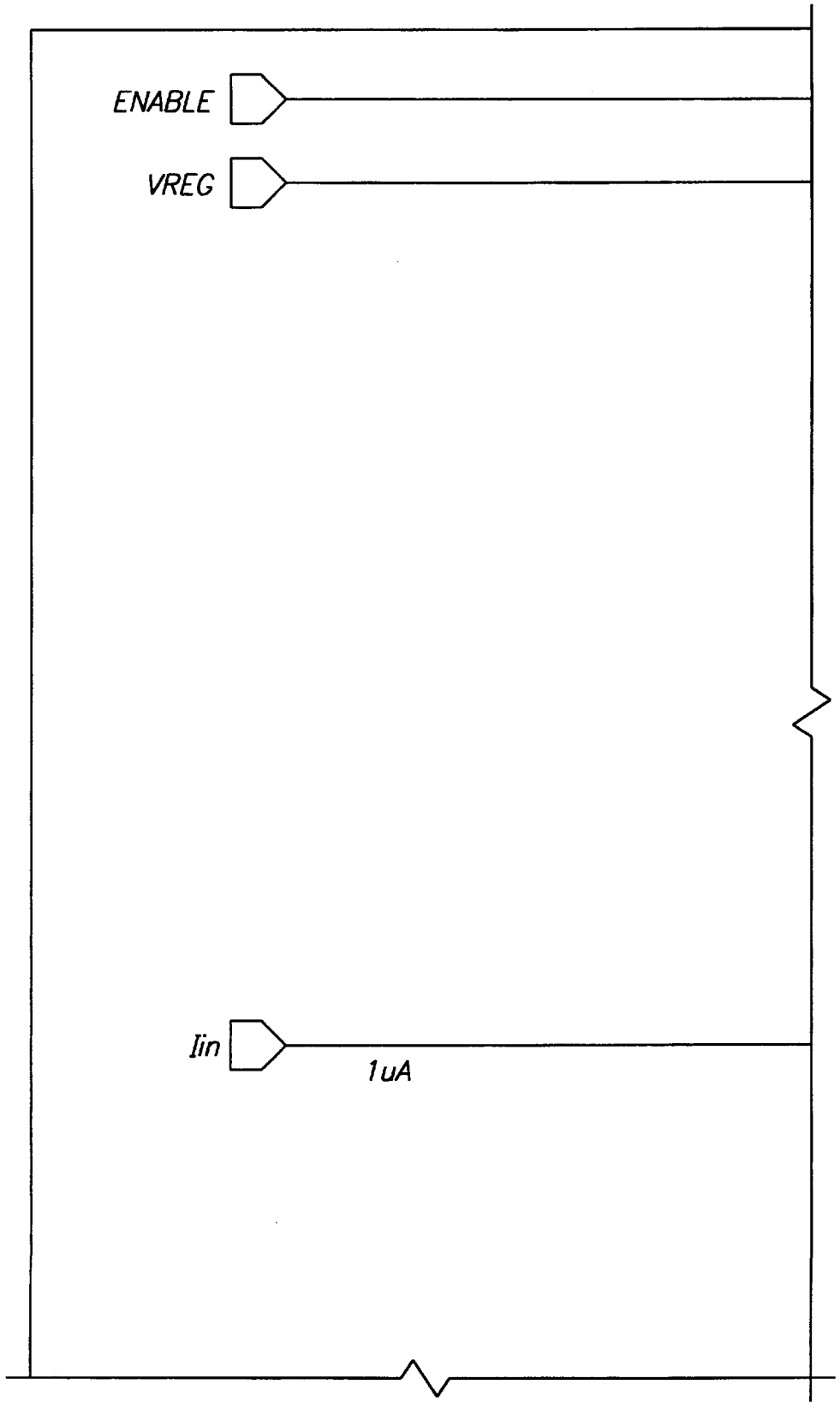


Fig 88.0504003AA

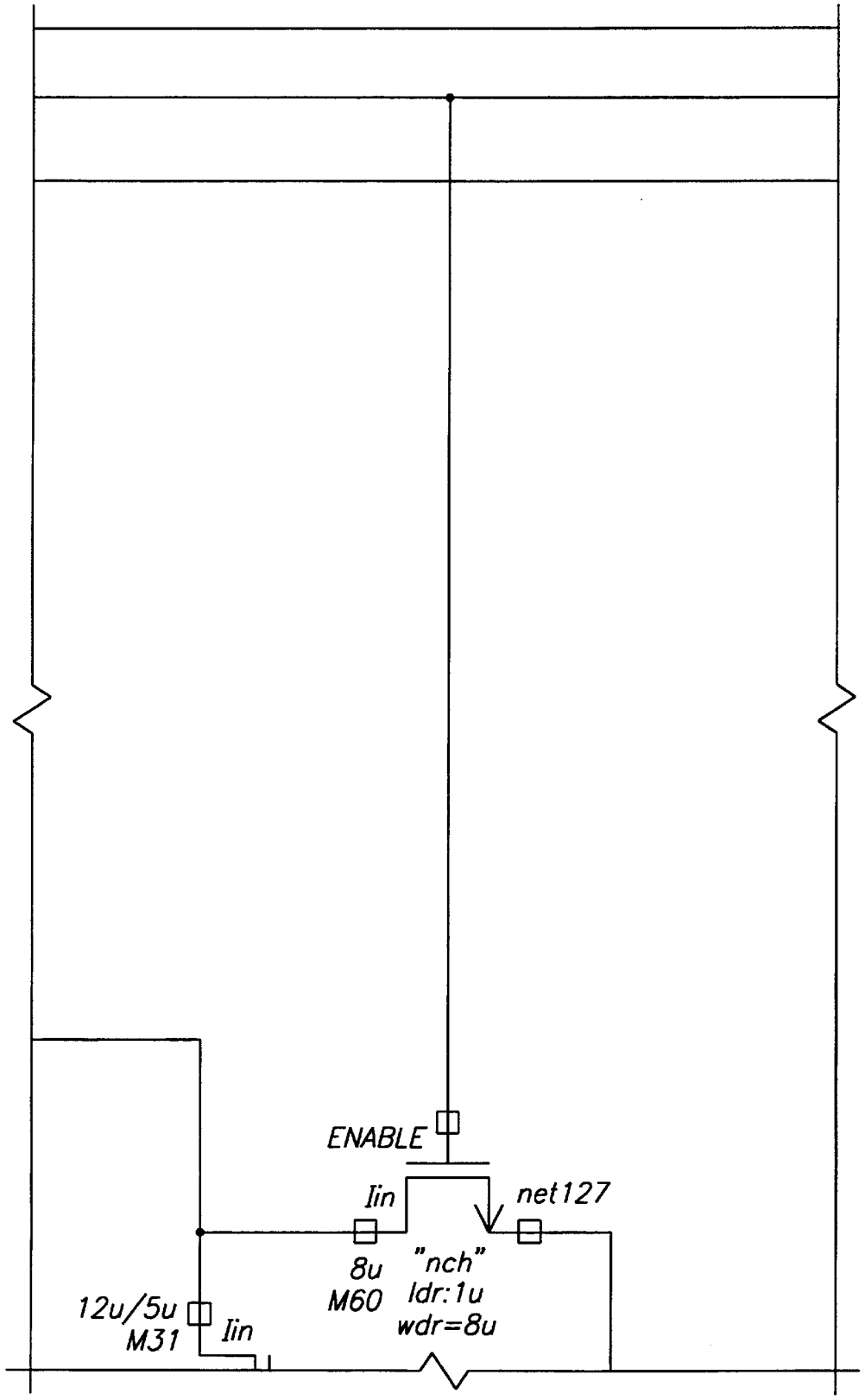


Fig 8,050,403AB

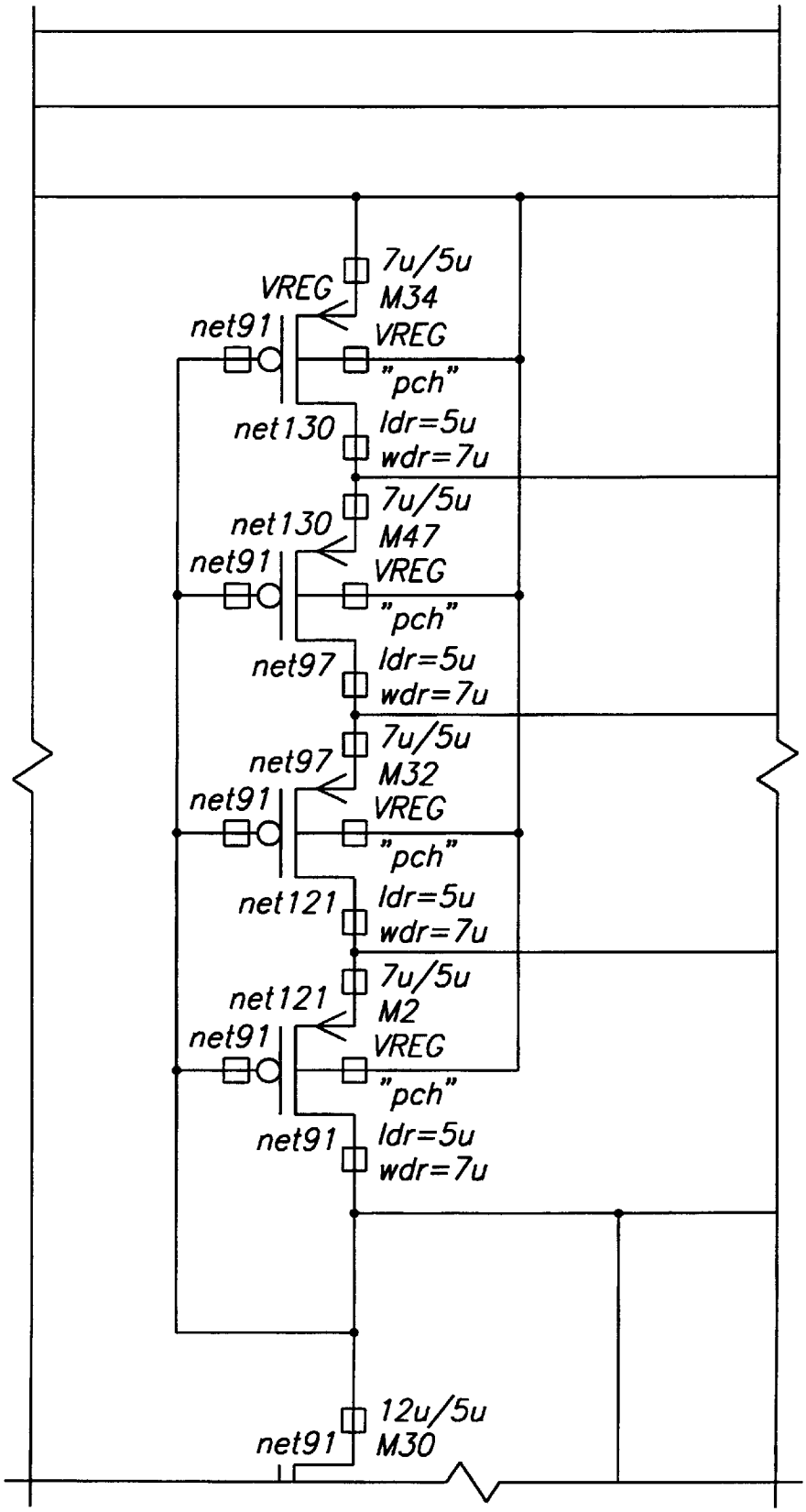


Fig 8,050,403AC

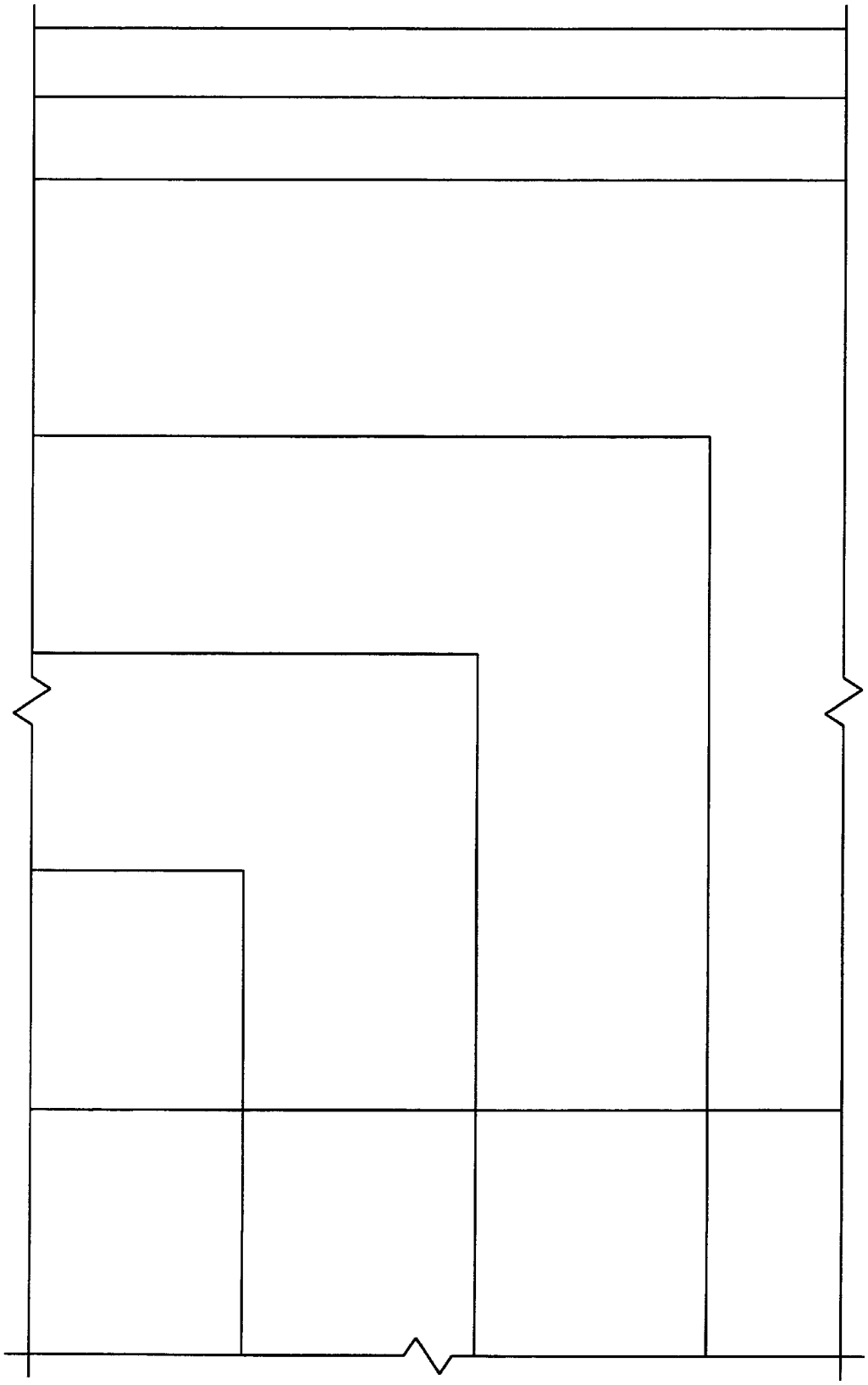


FIG 8.0504.03AD

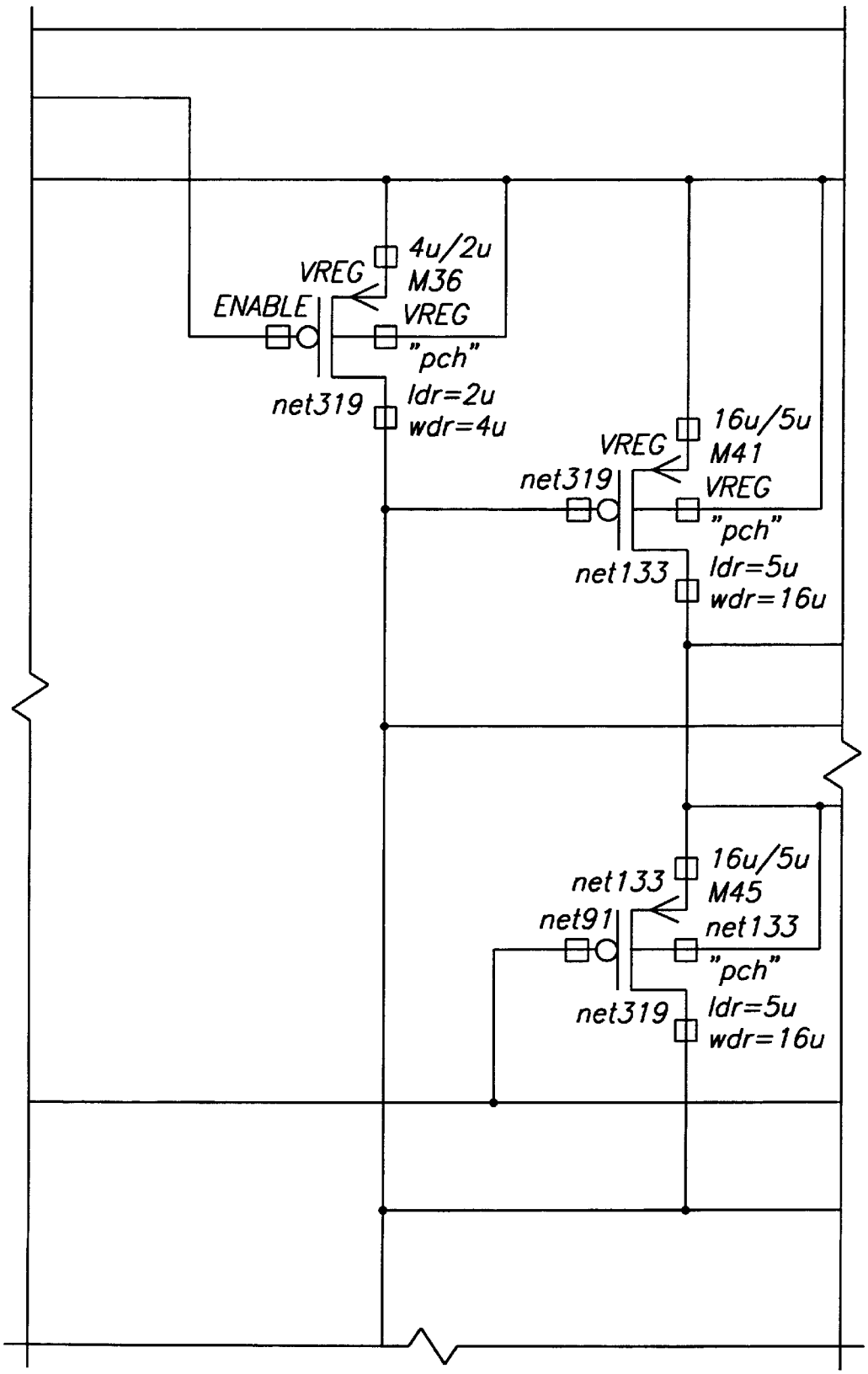


Fig 8.0504003AE

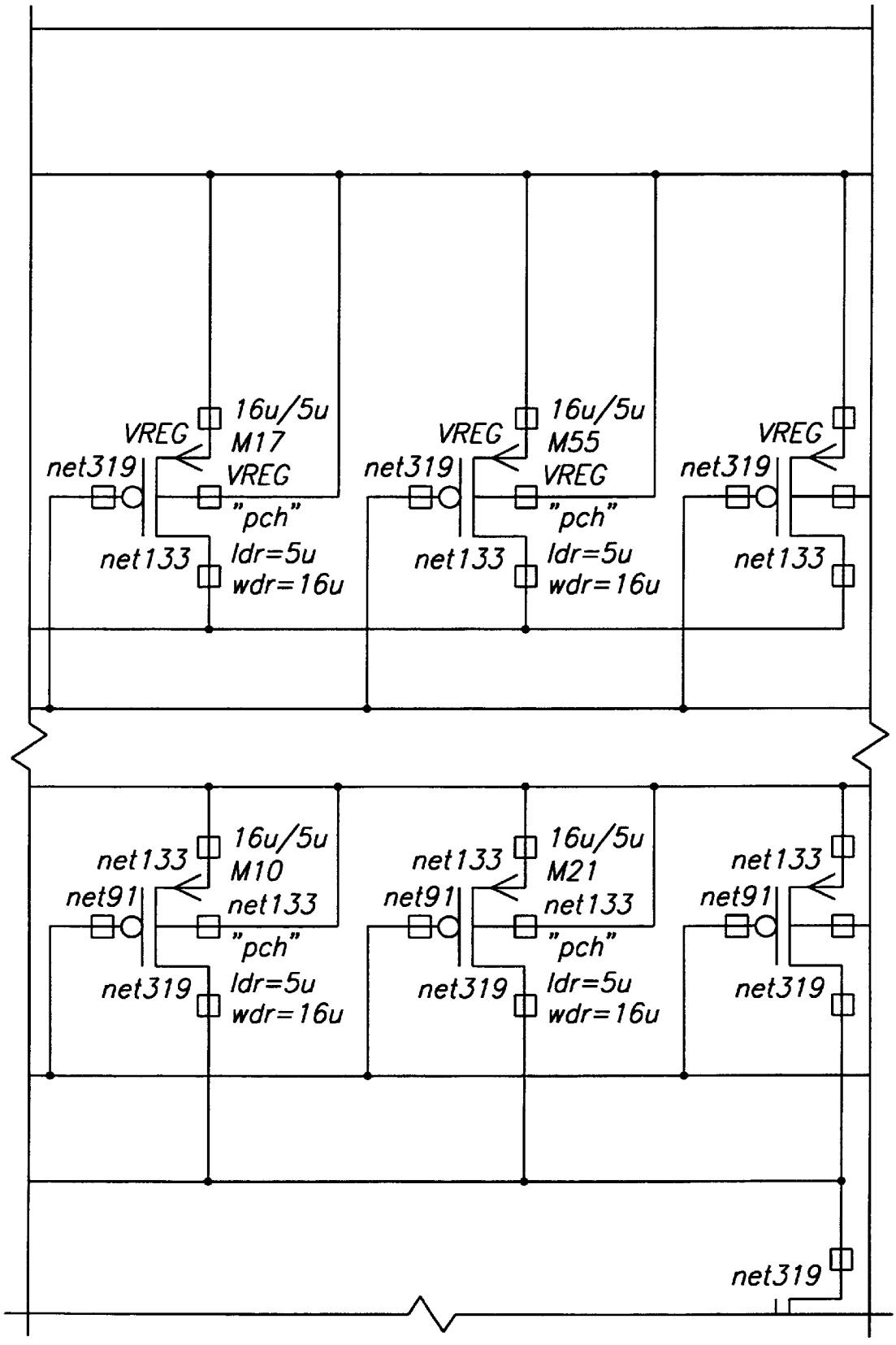


FIG 8,050,403AF

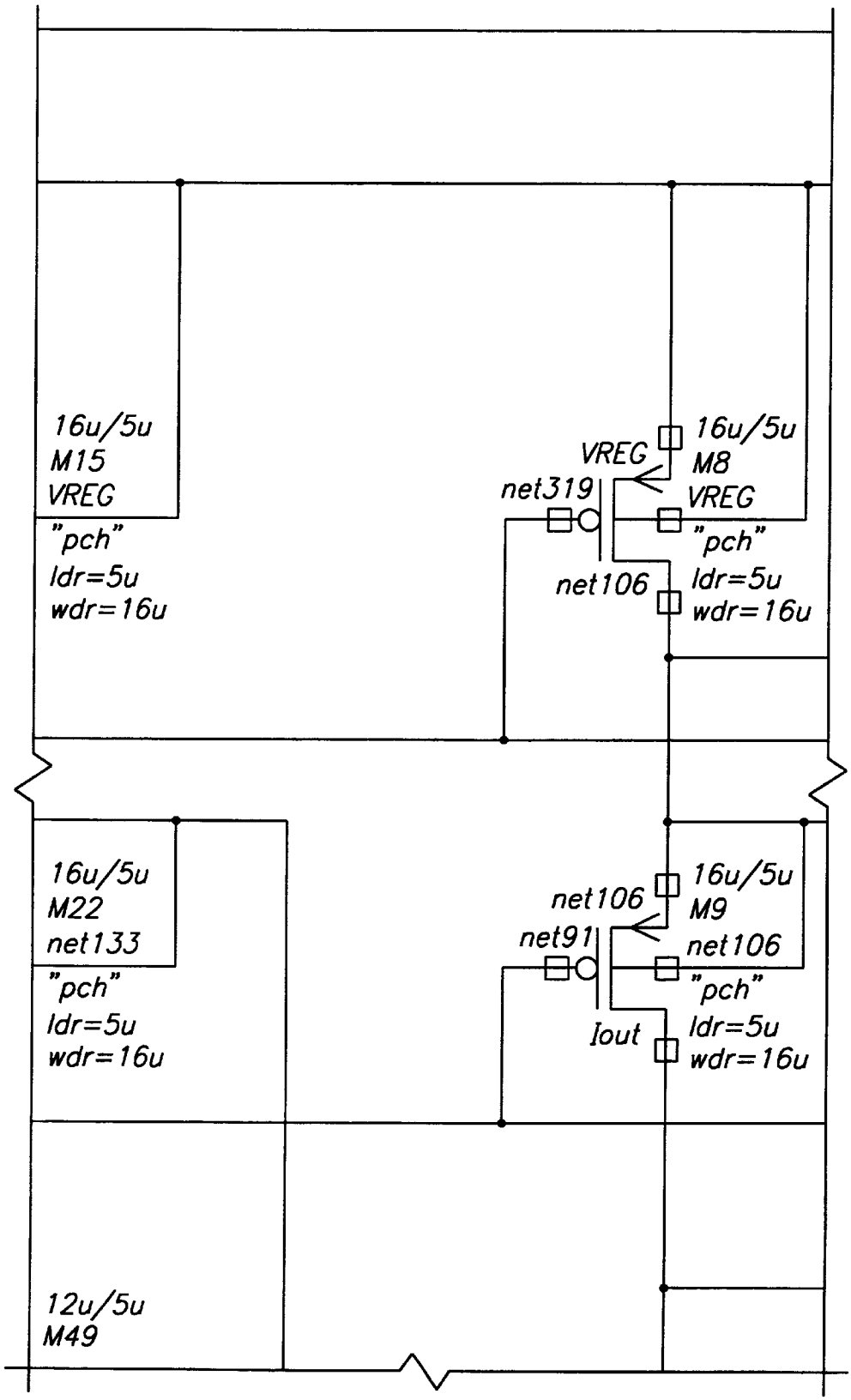


Fig 8.0504036

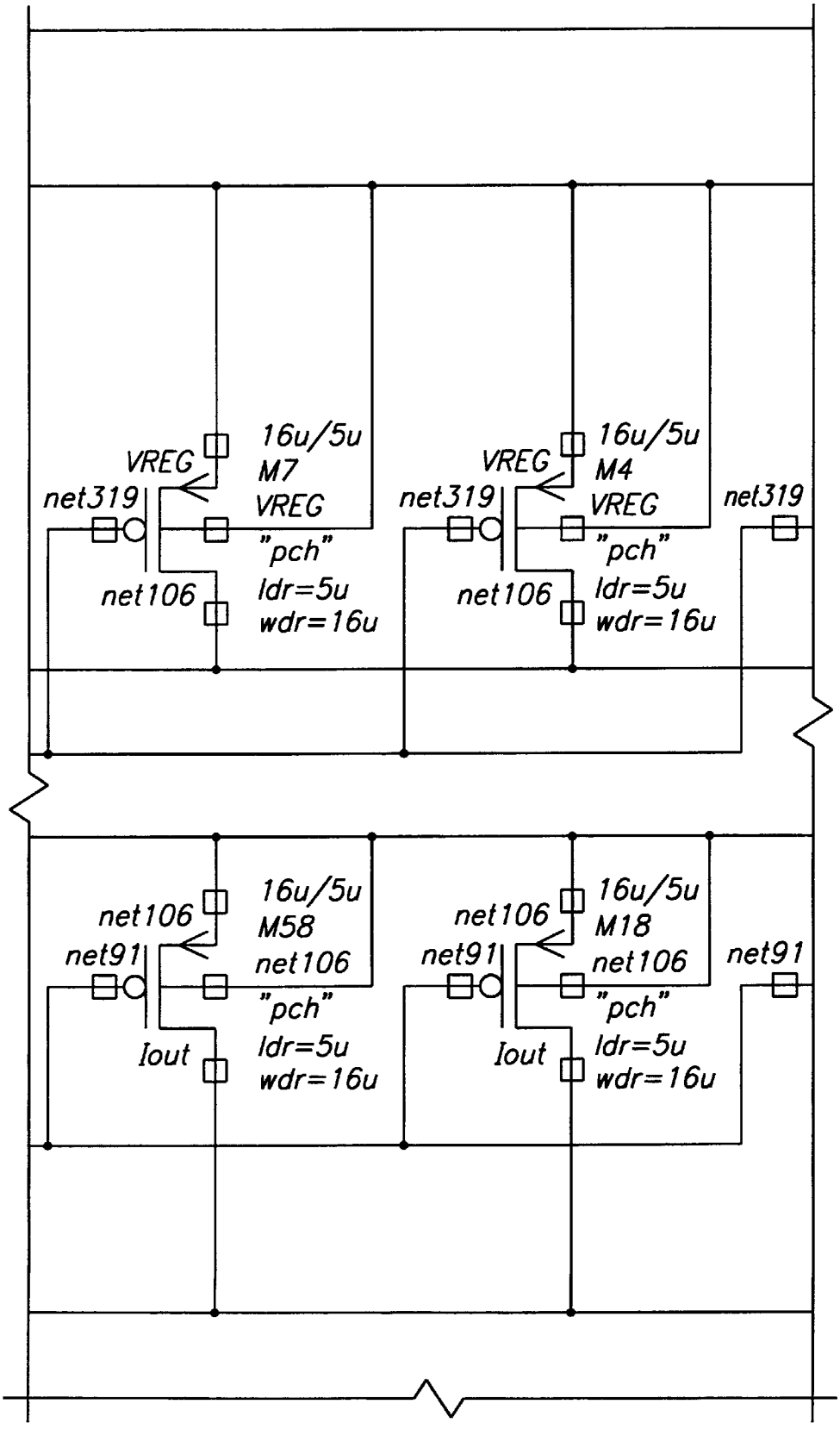


FIG 8,050,403AH

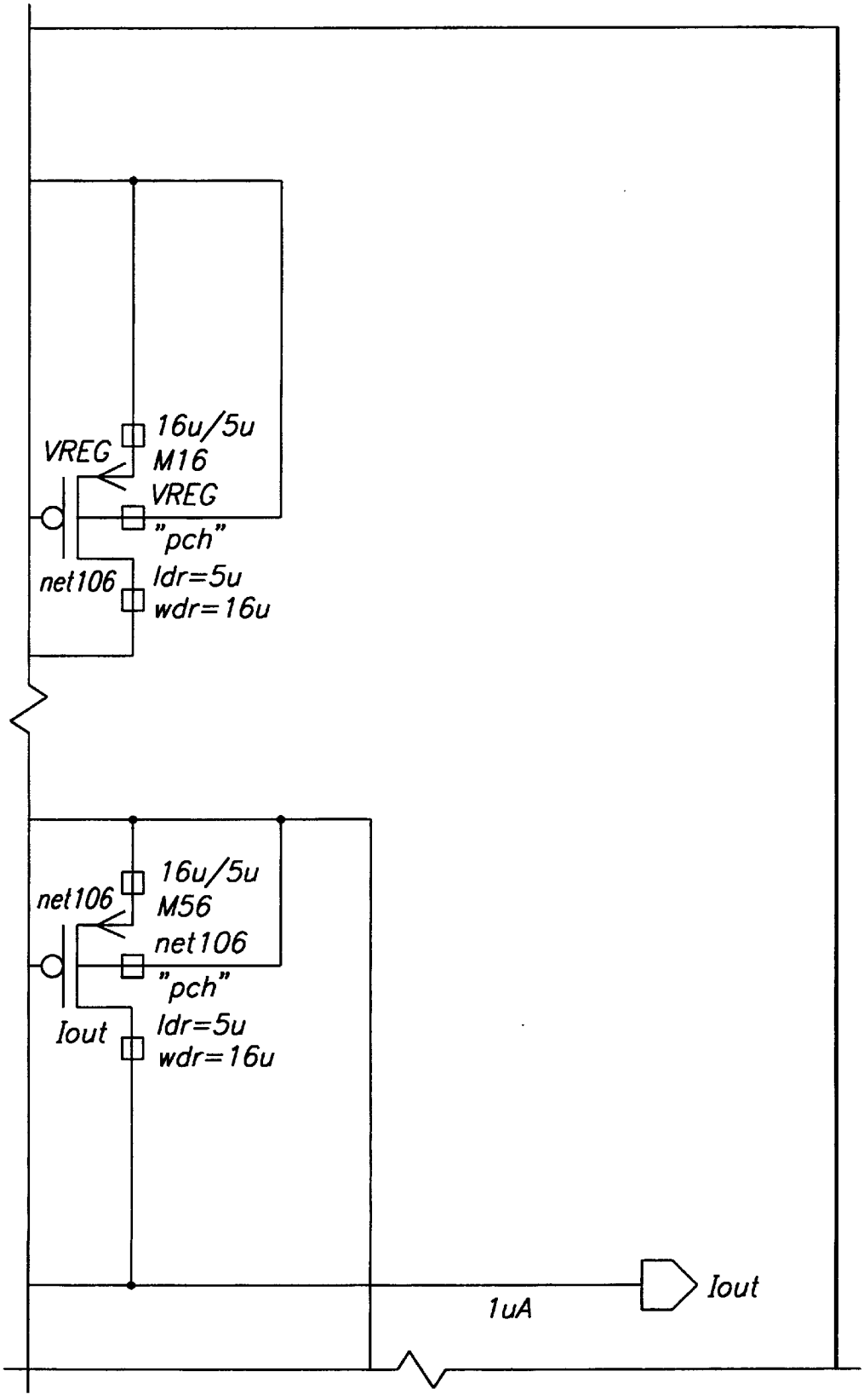


Fig 8.0504.03AI

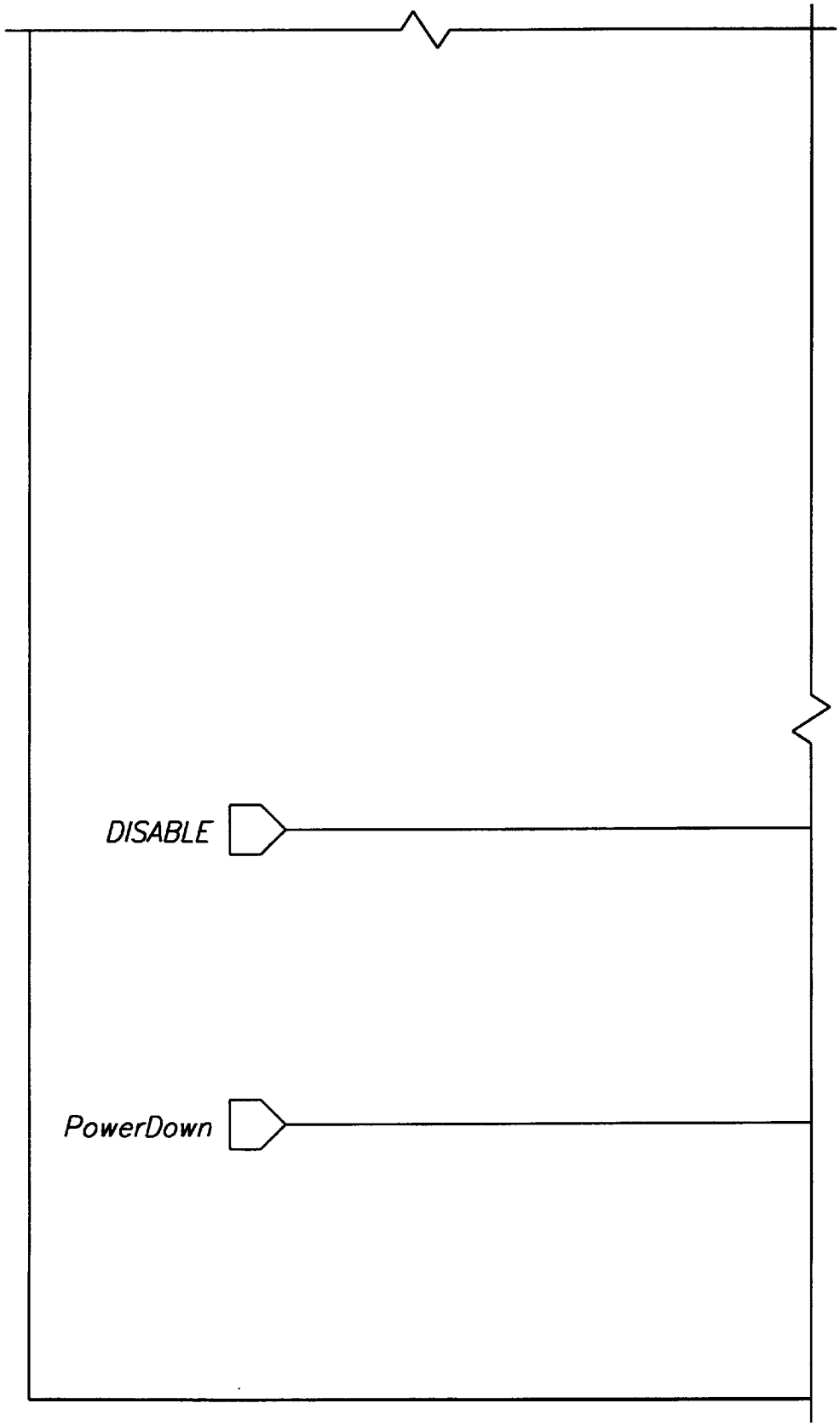


Fig 88.0504.0318A

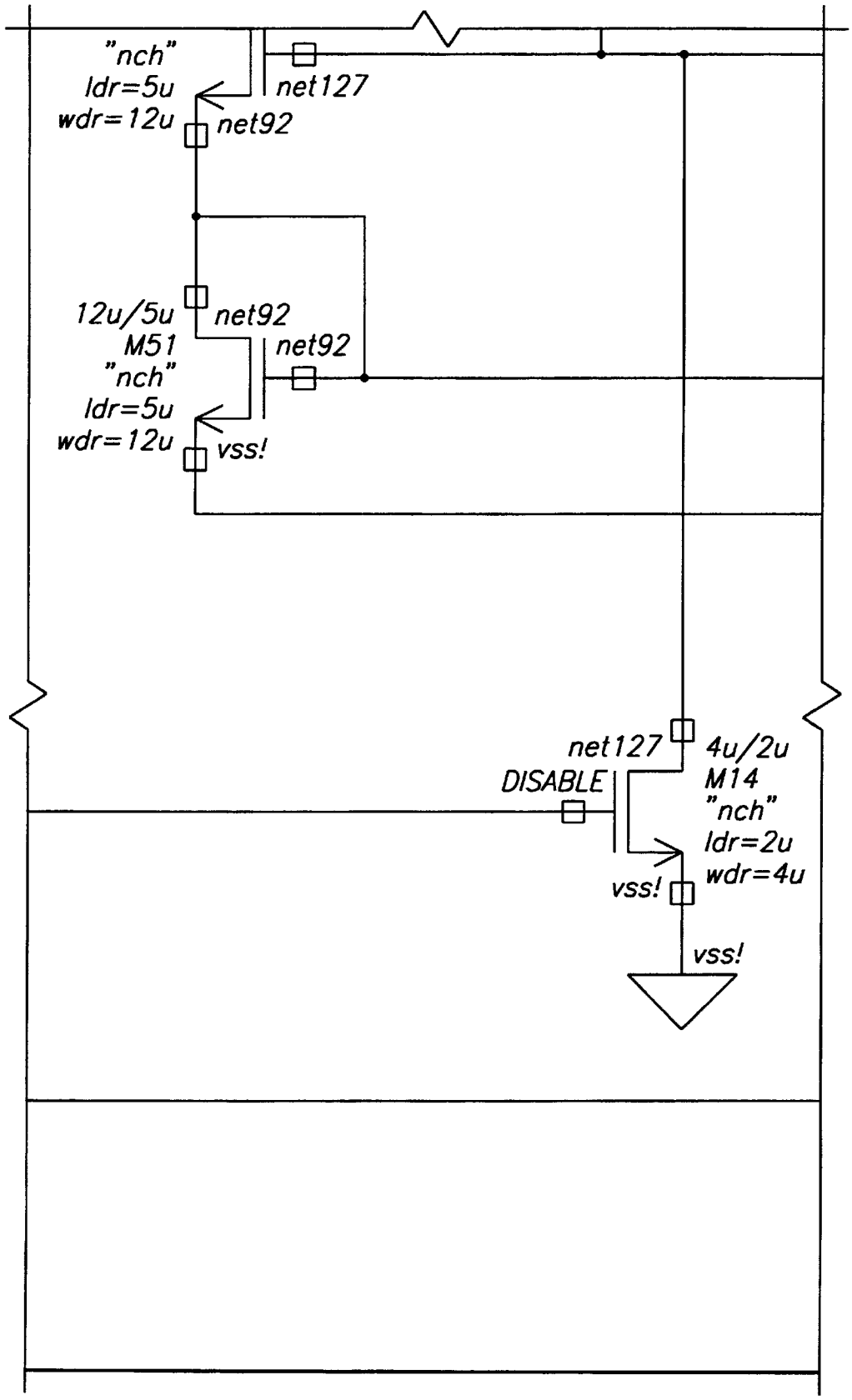


Fig 8,050,403,B8

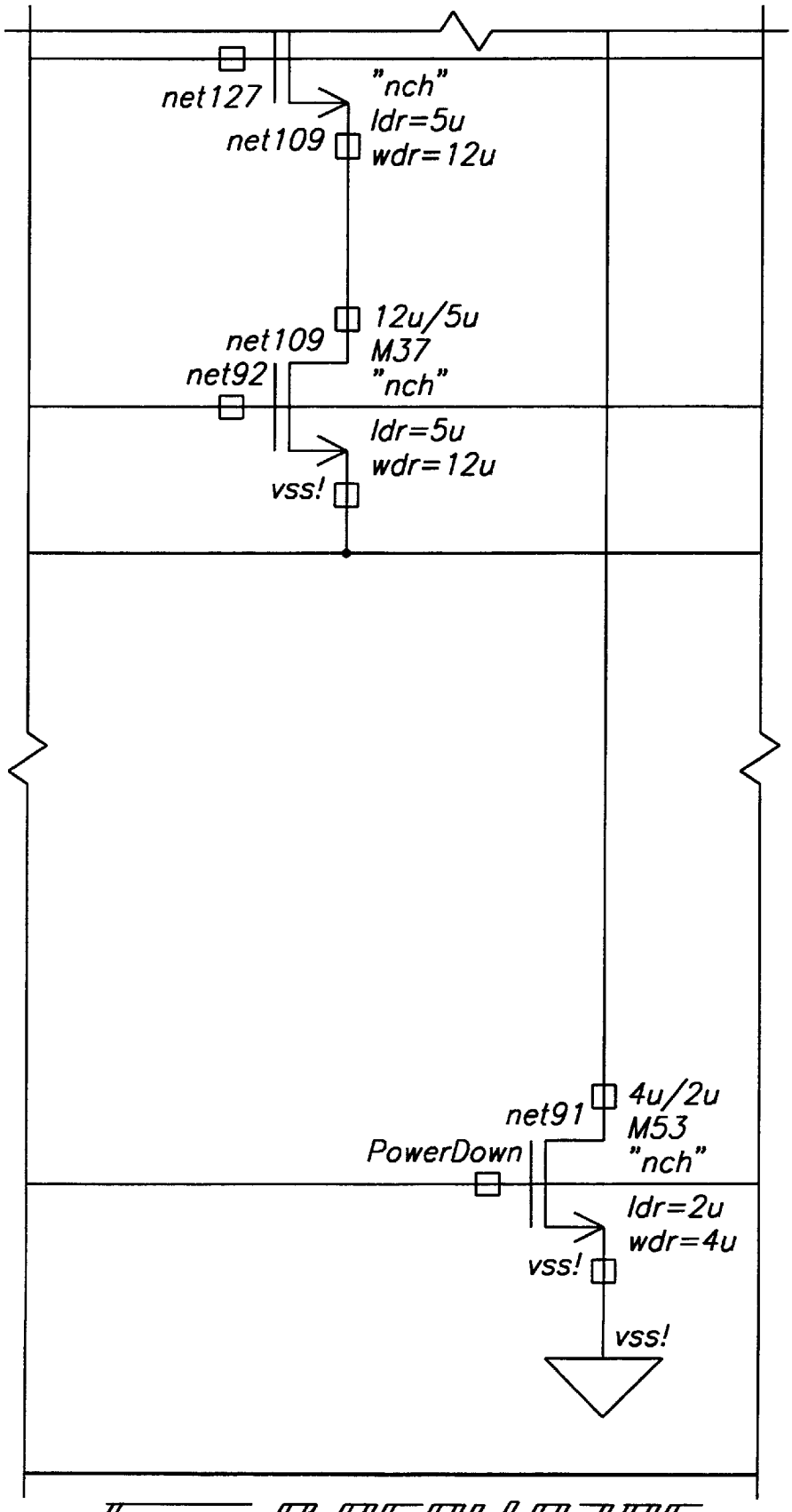


Fig 8,050,403BC

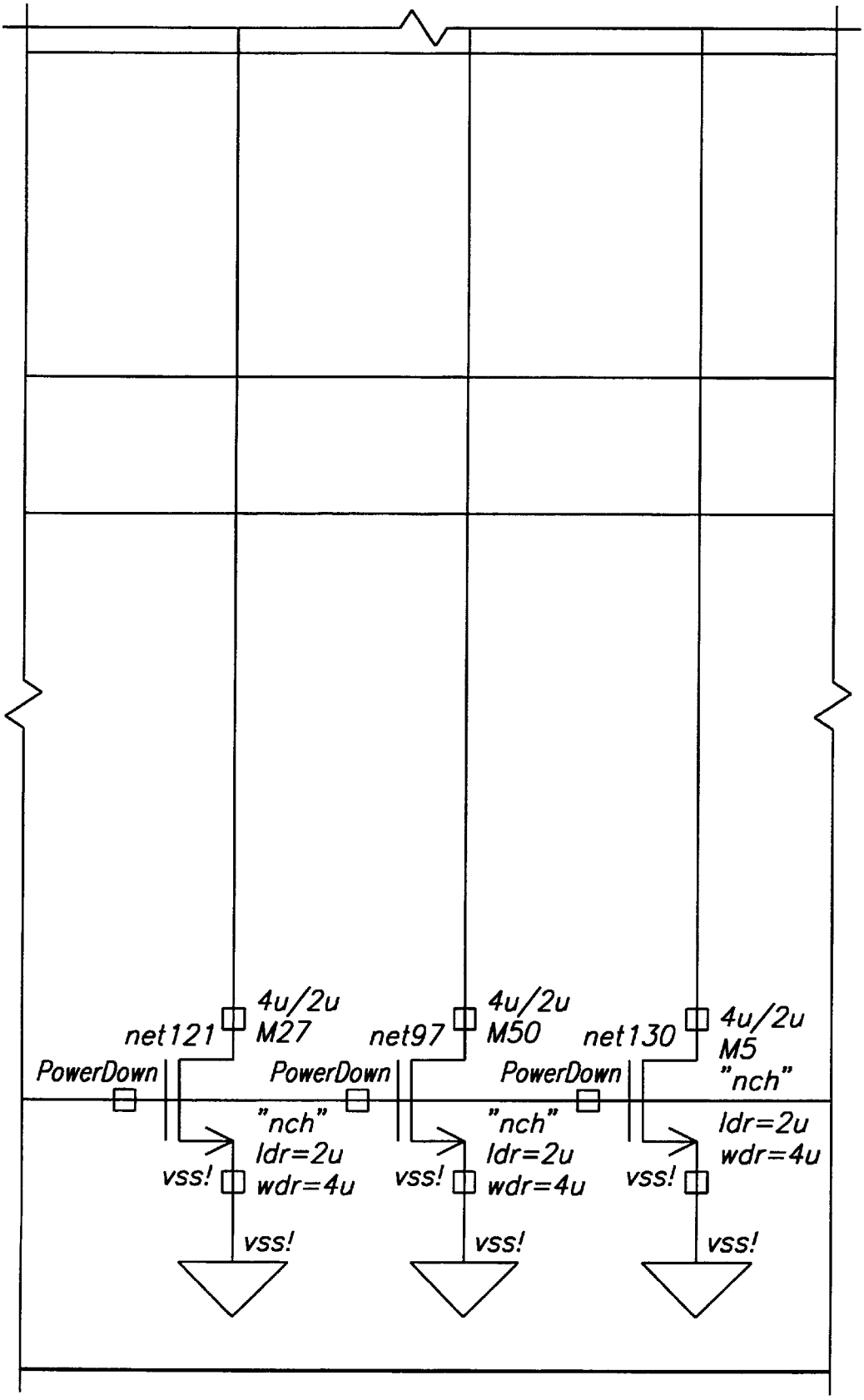


Fig 8,050,403BD

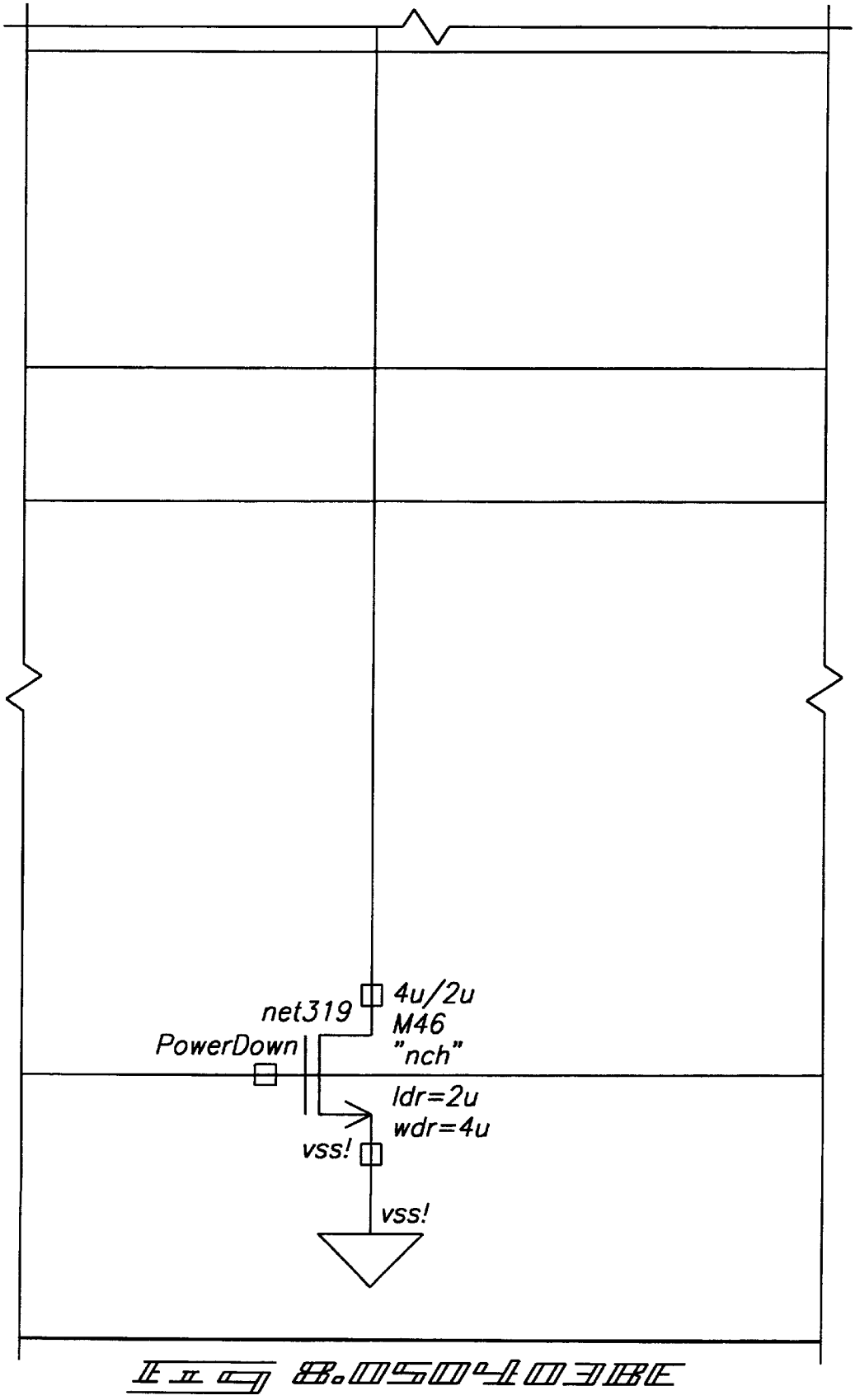


Fig 8,050,403BE

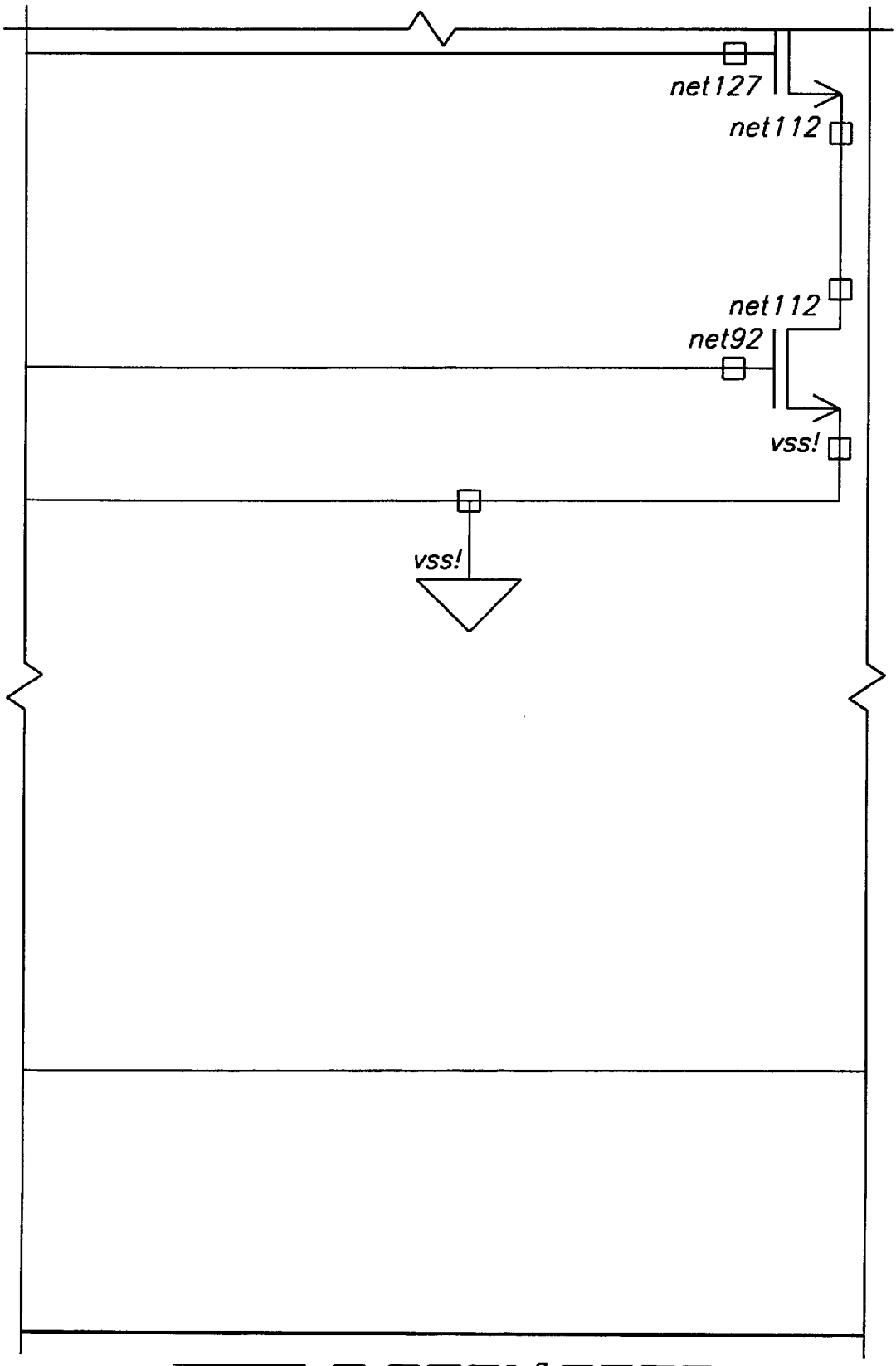


Fig 88.0504038F

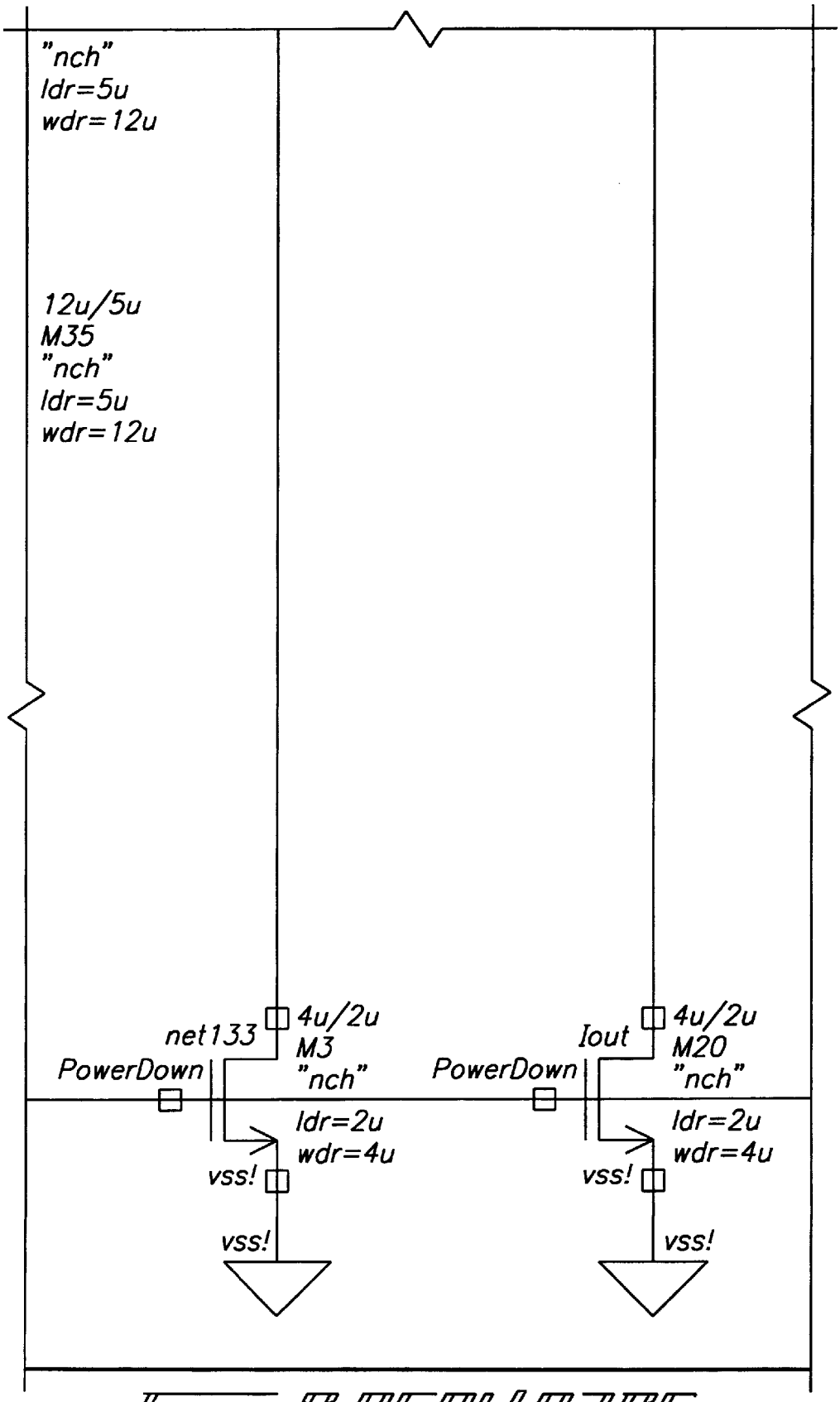
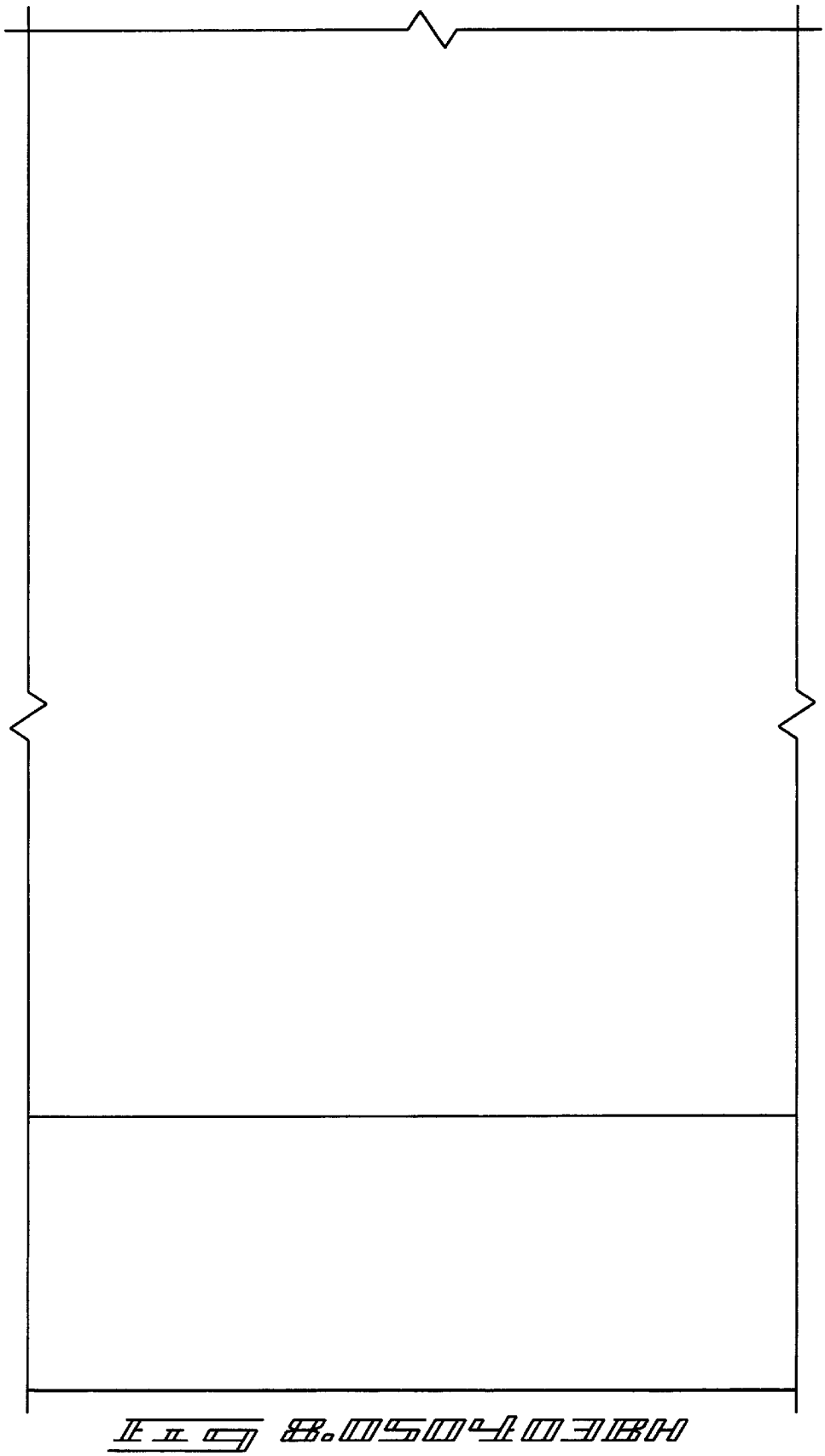


Fig 8,050,403,B6



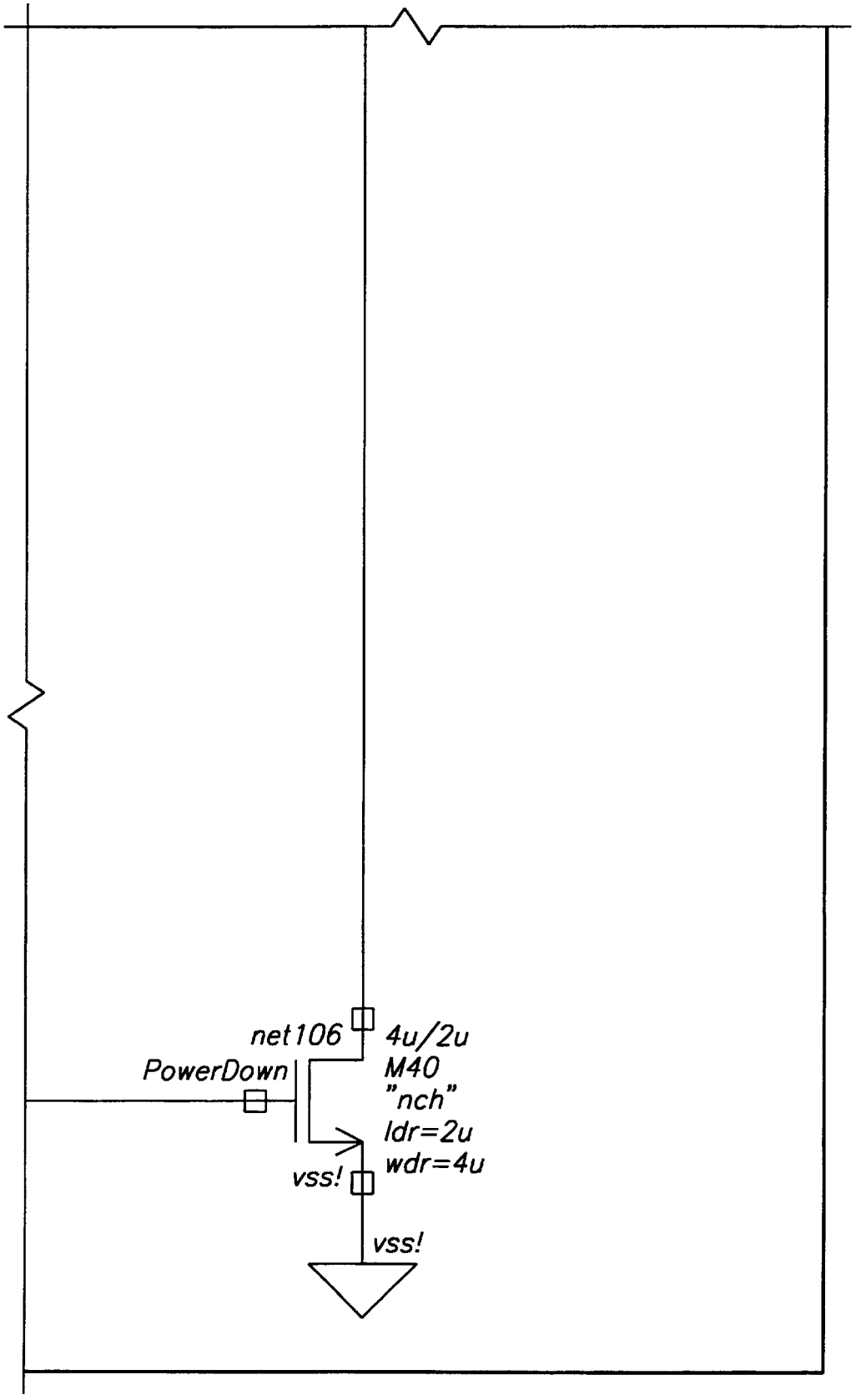


Fig 8,050,403B1

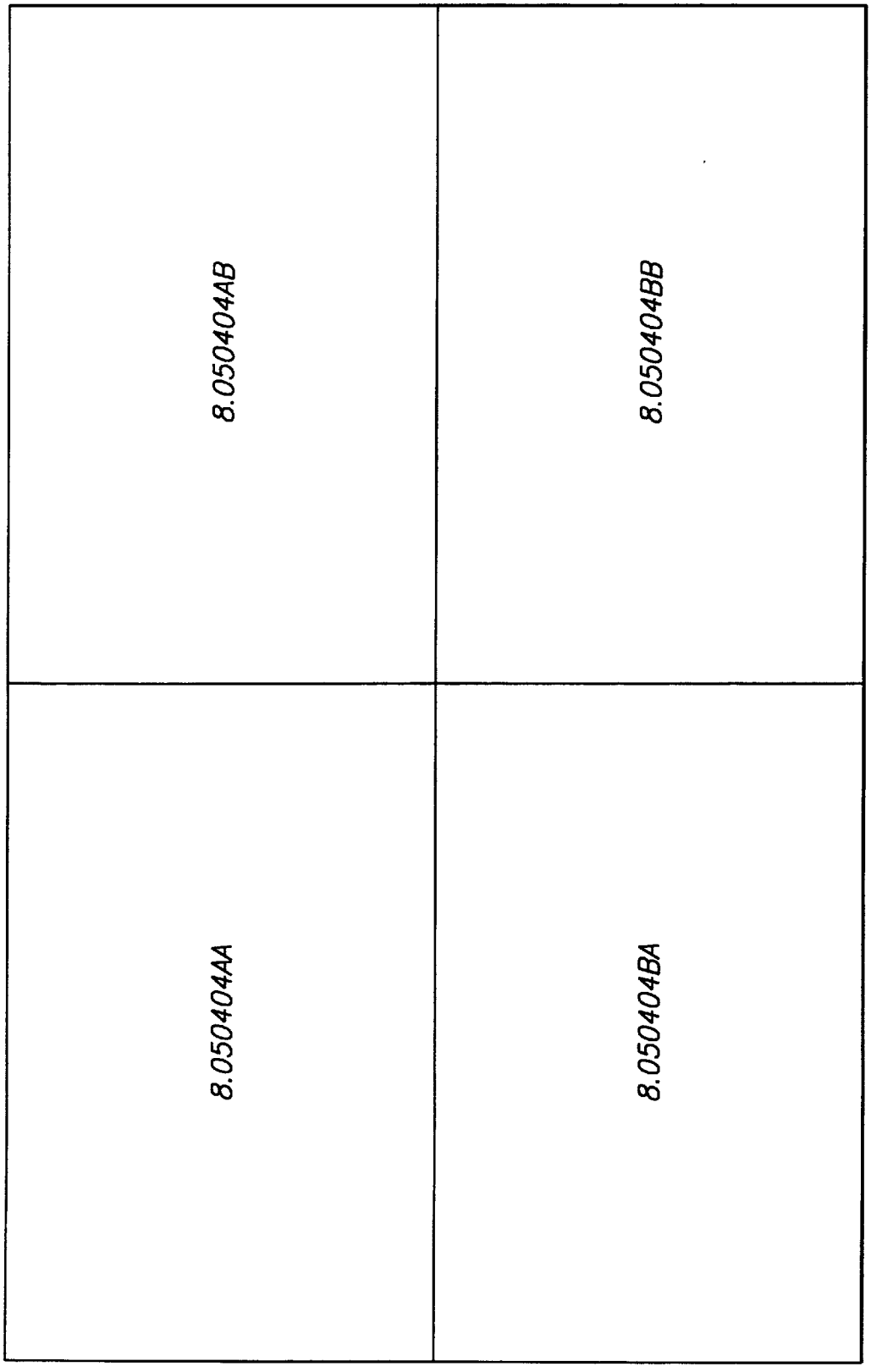


FIG 8.050404

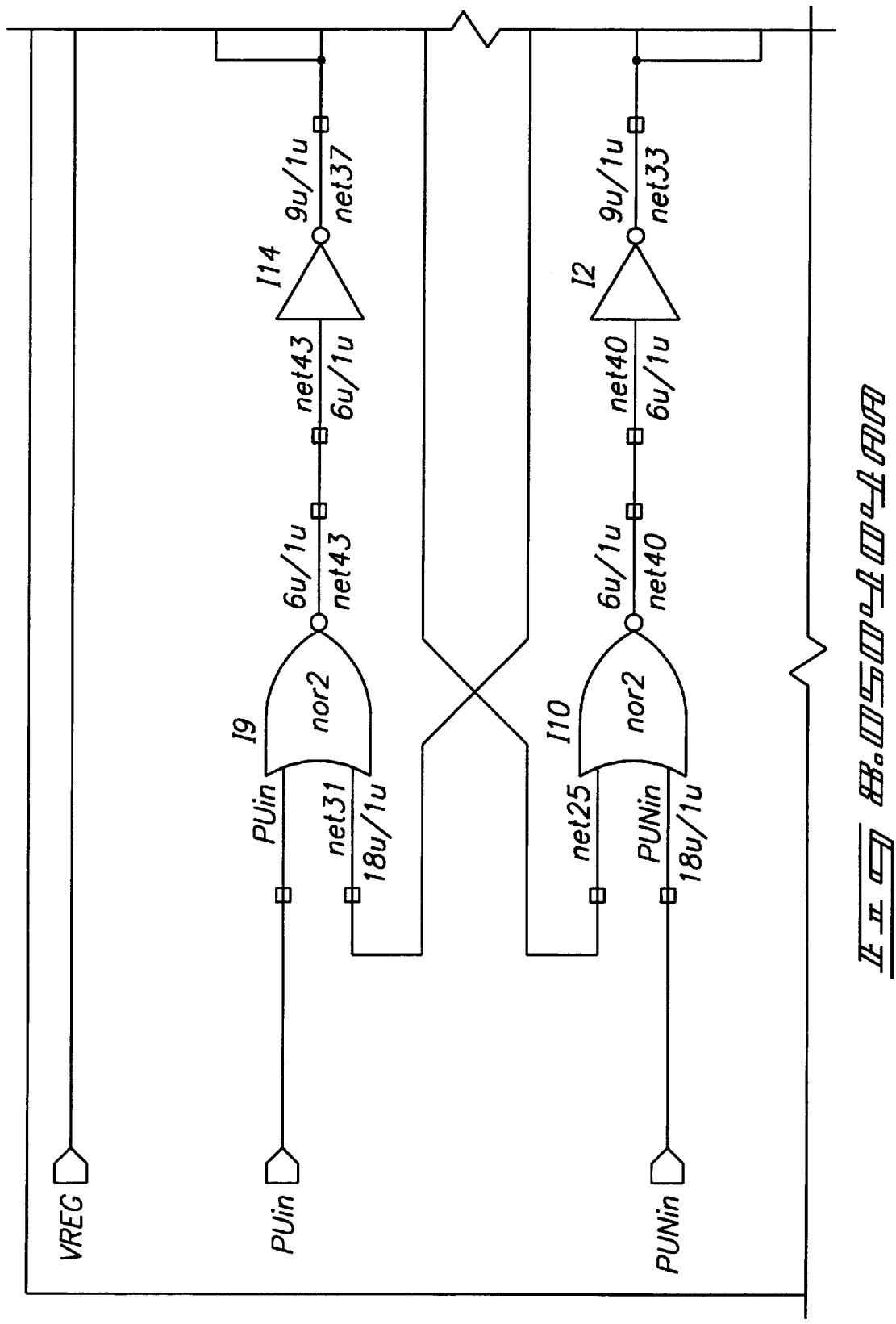


FIG 88.0504AA

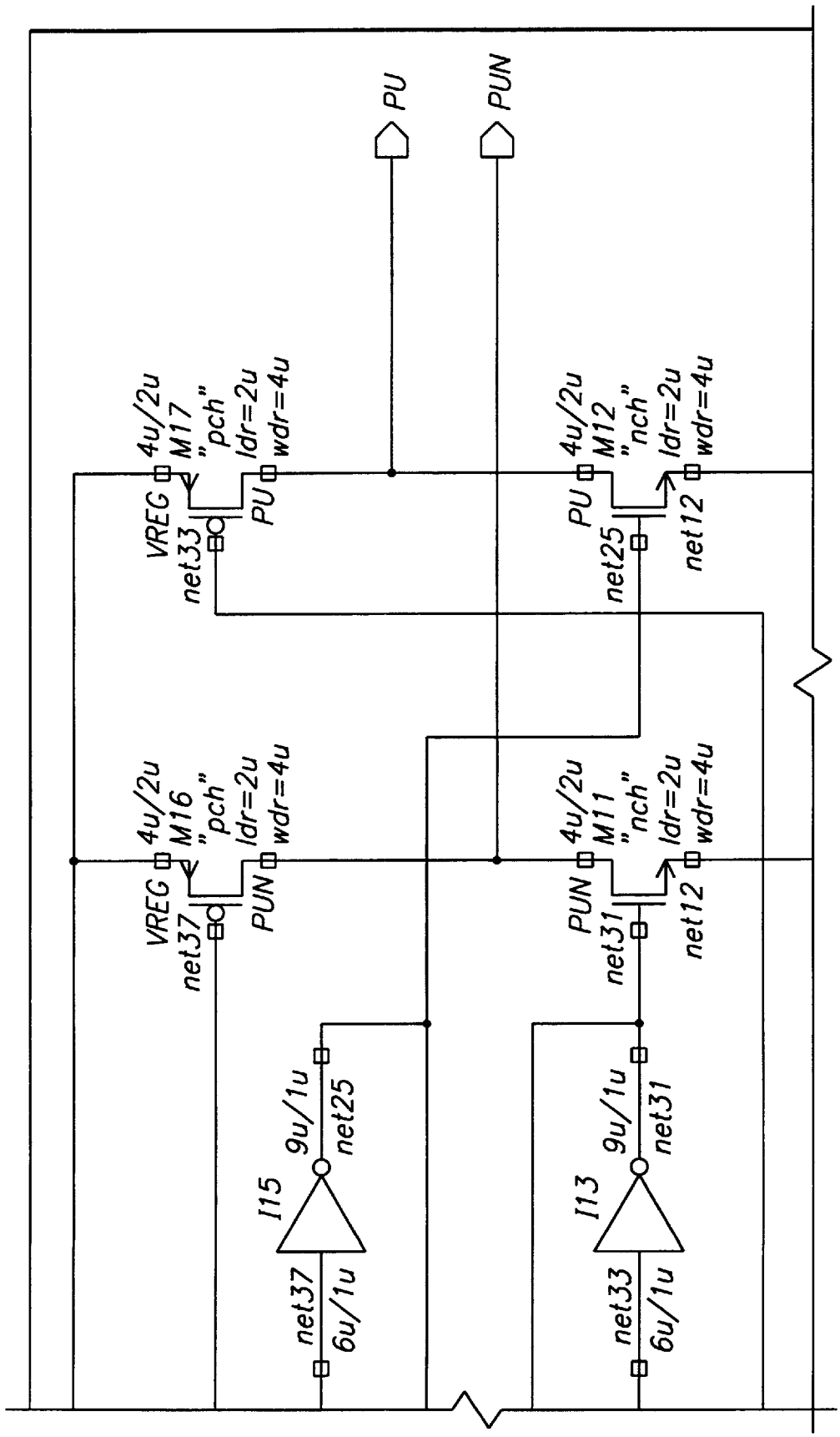

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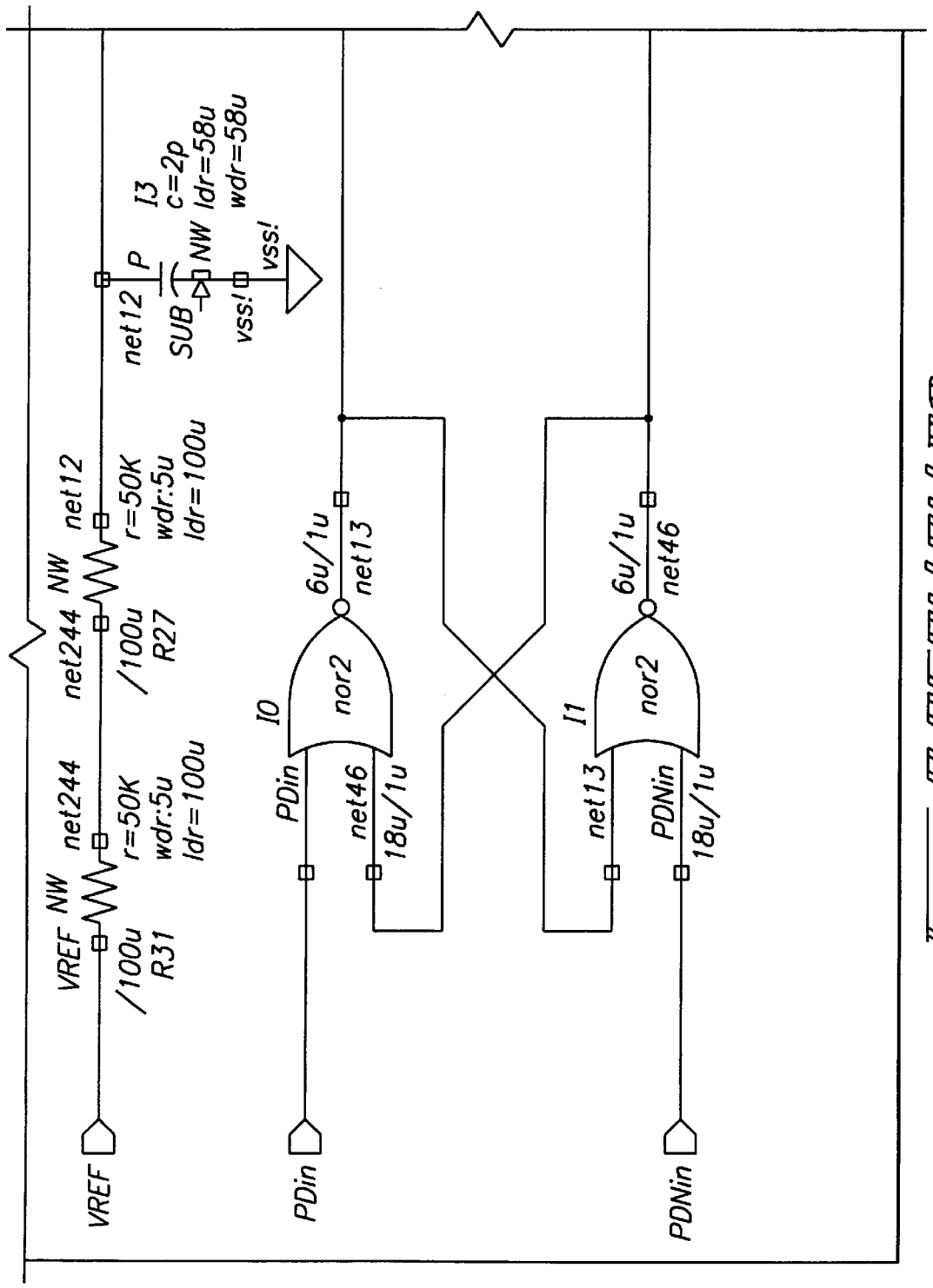
FIG 8,050,408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P
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vss!
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FIG. 8.0504B

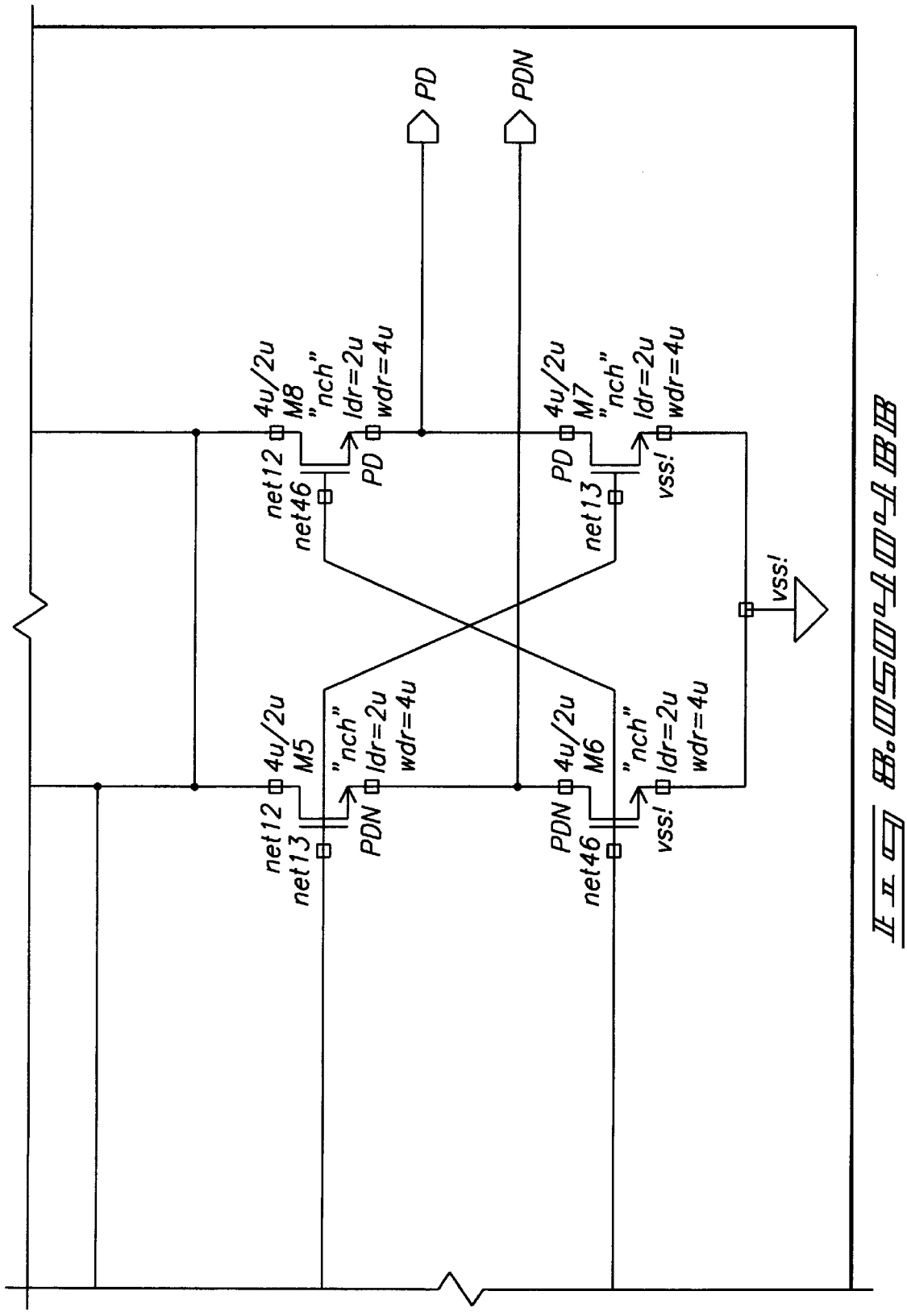

Fig 8.0504 IBM

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8.050405CA	8.050405CB	8.050405CC	8.050405CD	8.050405CE	8.050405CF	8.050405CG	8.050405CH	8.050405CI	8.050405CJ	8.050405CK	8.050405CL	8.050405CM
8.050405DA	8.050405DB	8.050405DC	8.050405DD	8.050405DE	8.050405DF	8.050405DG	8.050405DH	8.050405DI	8.050405DJ			
8.050405EA	8.050405EB	8.050405EC	8.050405ED	8.050405EE	8.050405EF	8.050405EG	8.050405EH	8.050405EI	8.050405EJ			

FIG. 88.050405

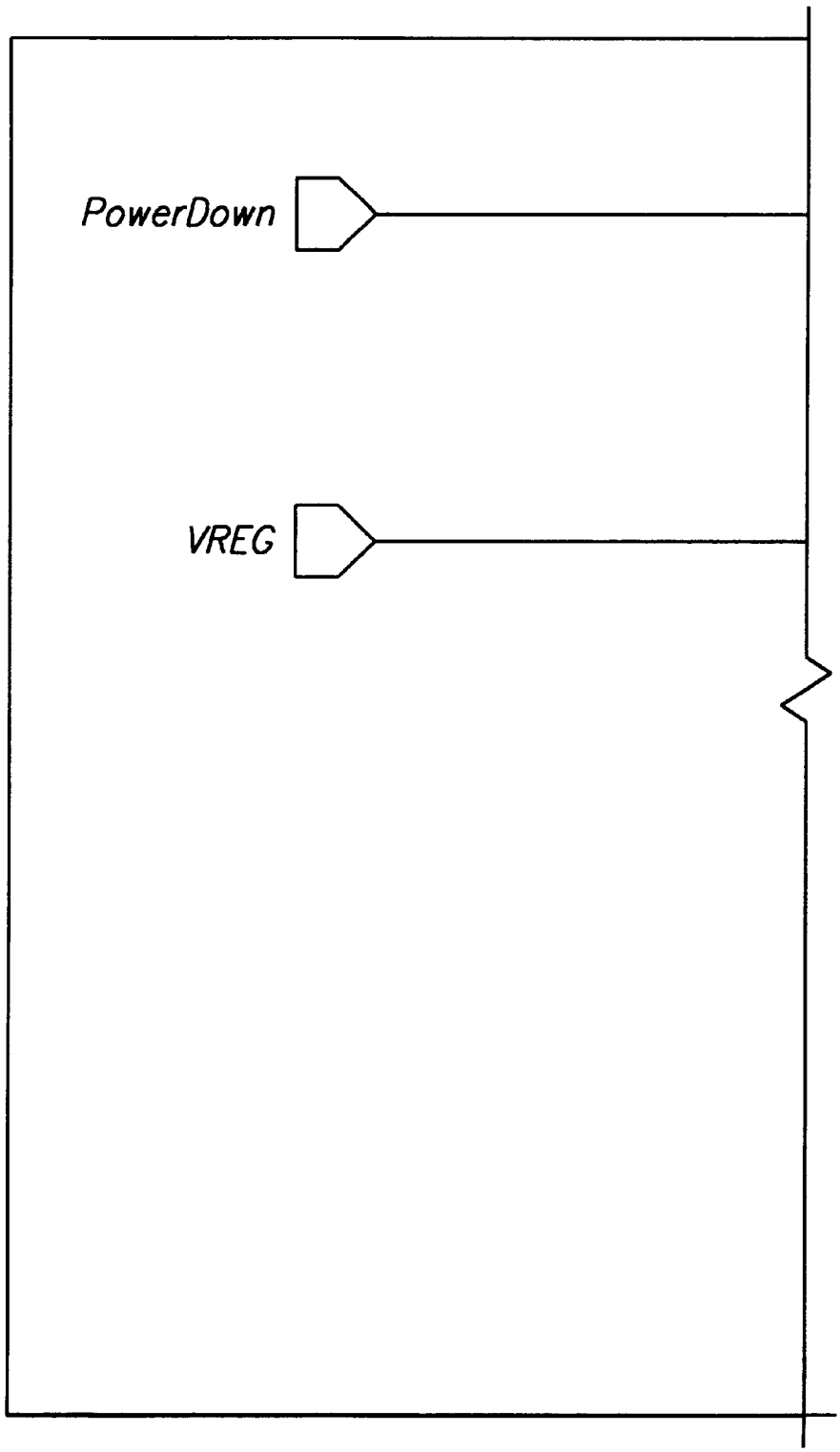


Fig 8.0504050AA

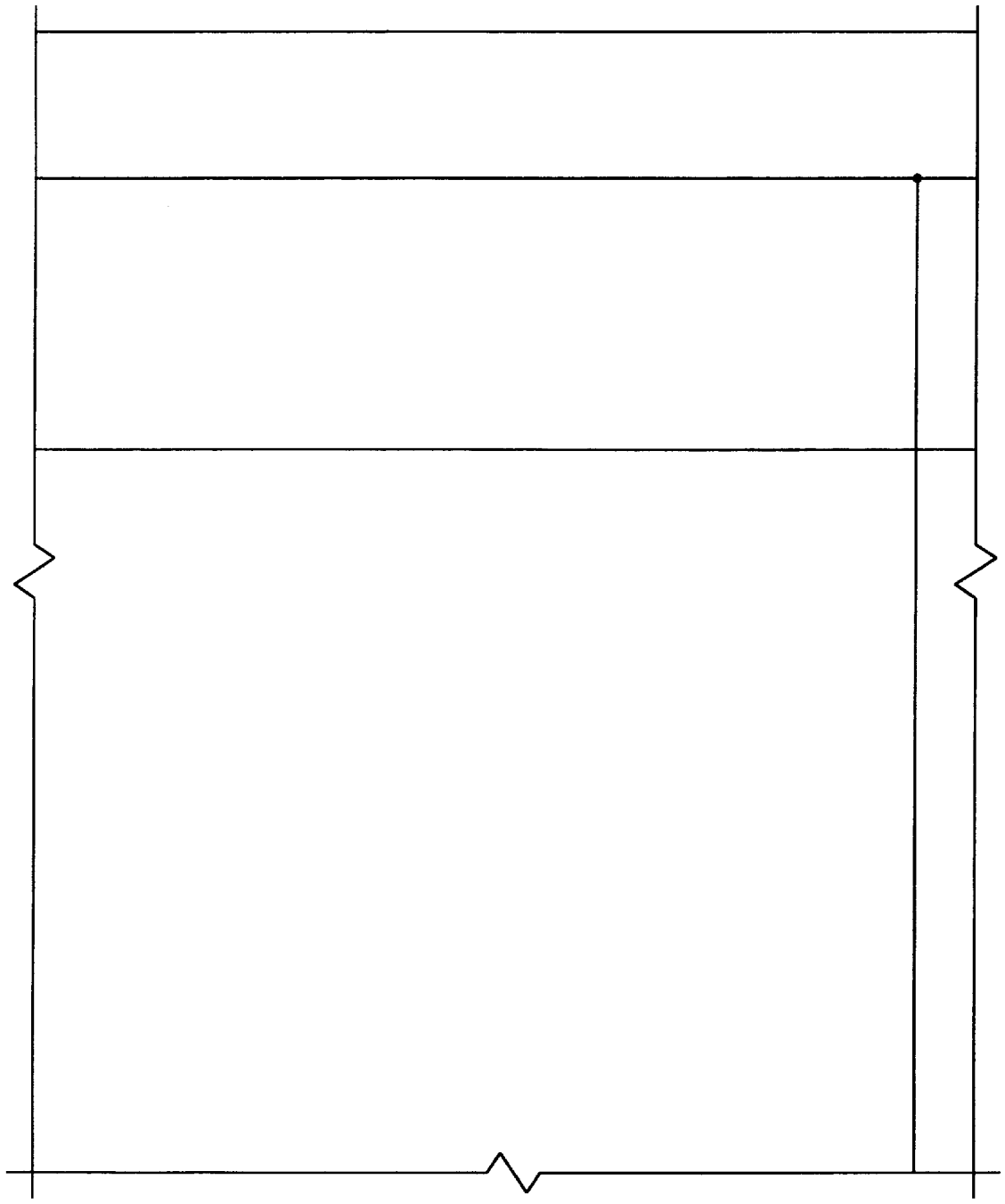


Fig 8.0504.0548

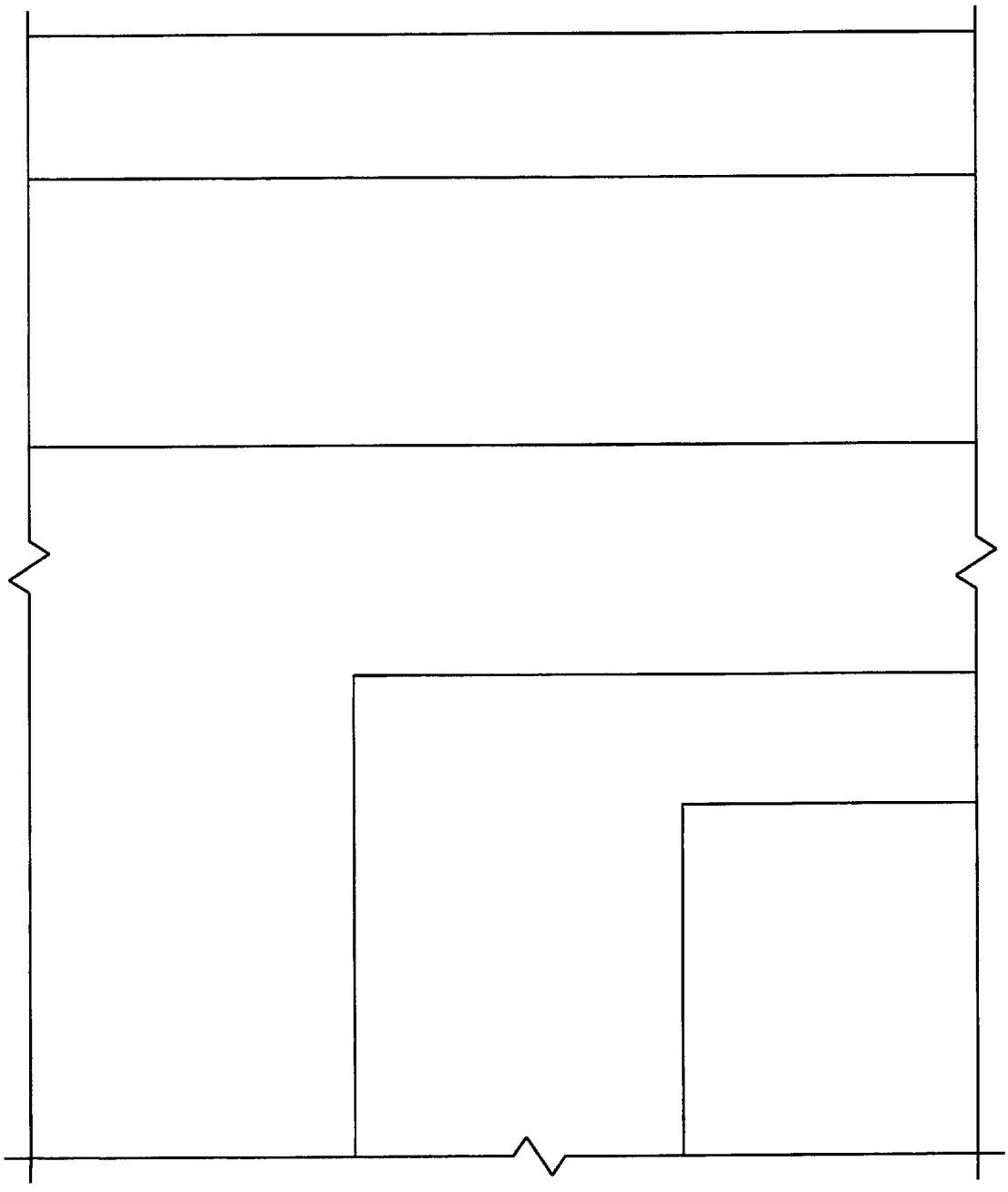


Fig 8.0504.0SAC

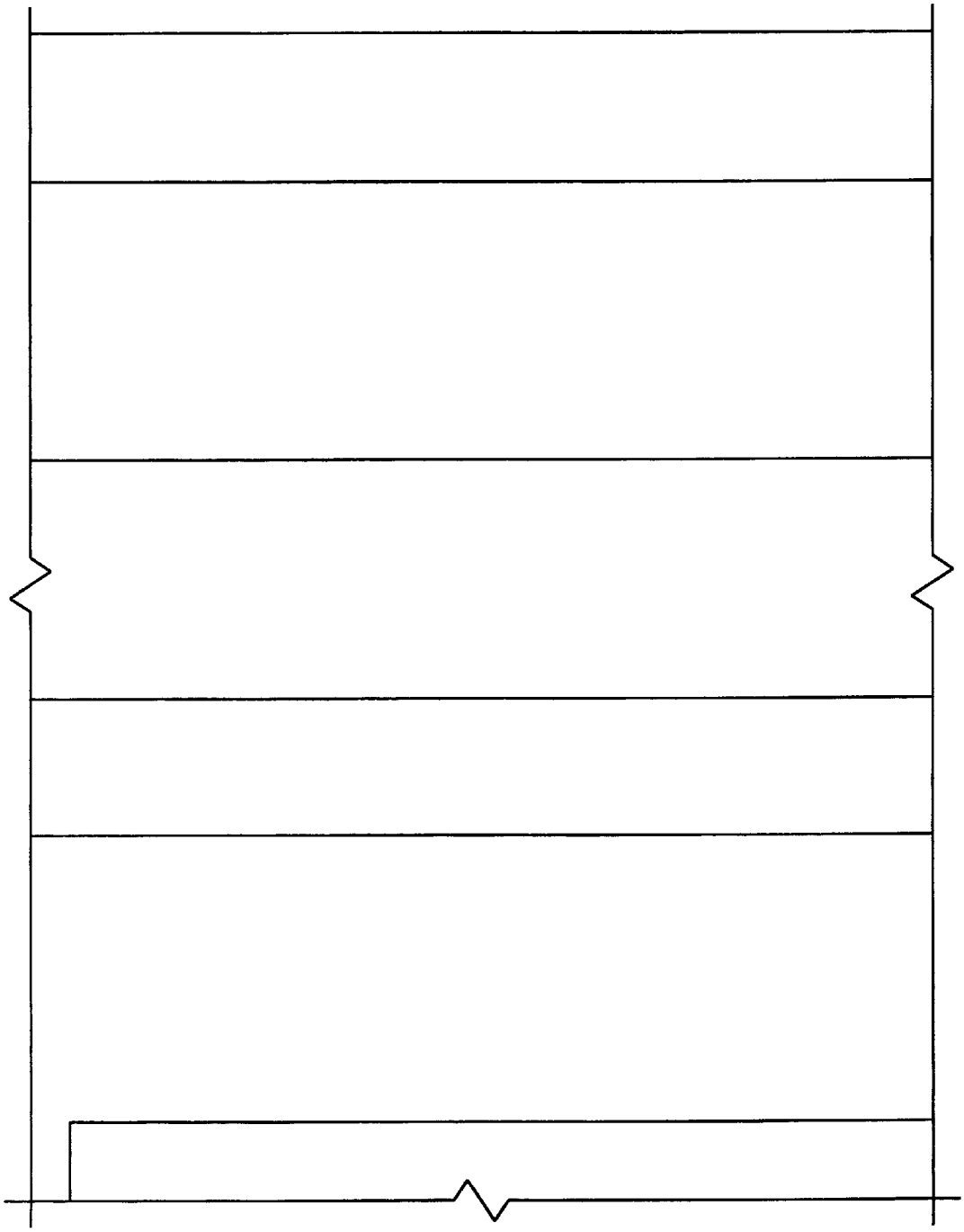


Fig 8.0504.05AD

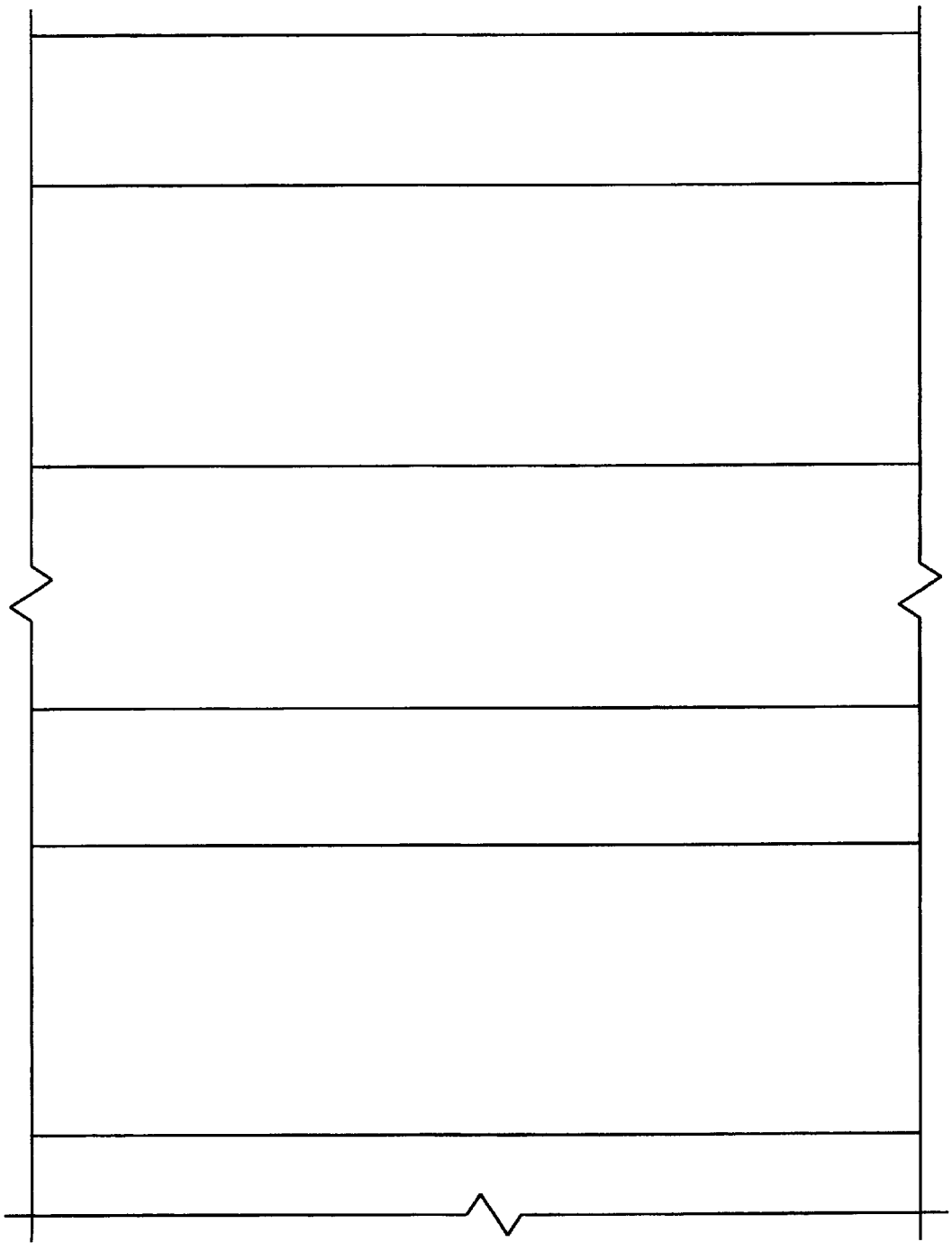


Fig 88.05041.05AE

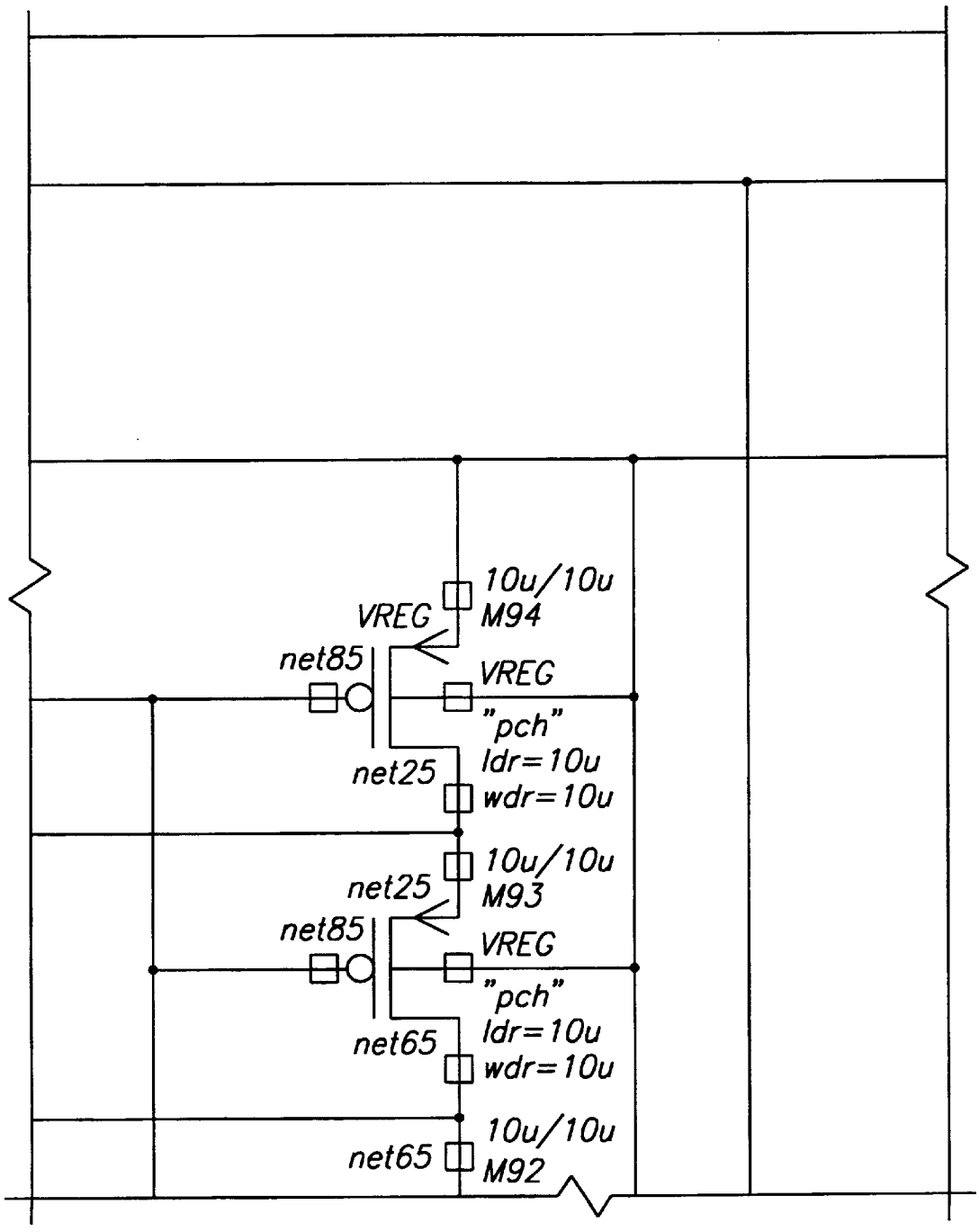
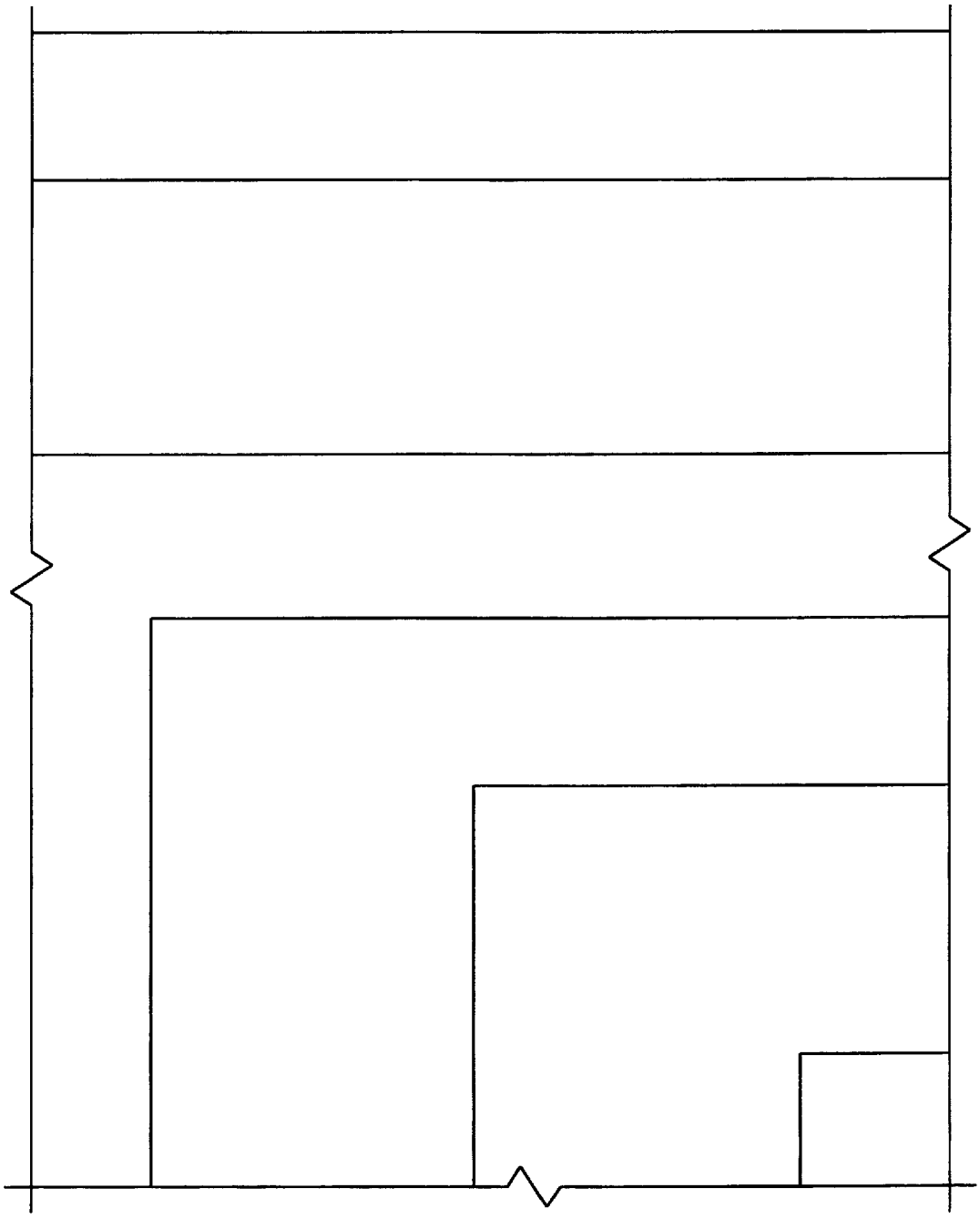


Fig 8,054,054AF



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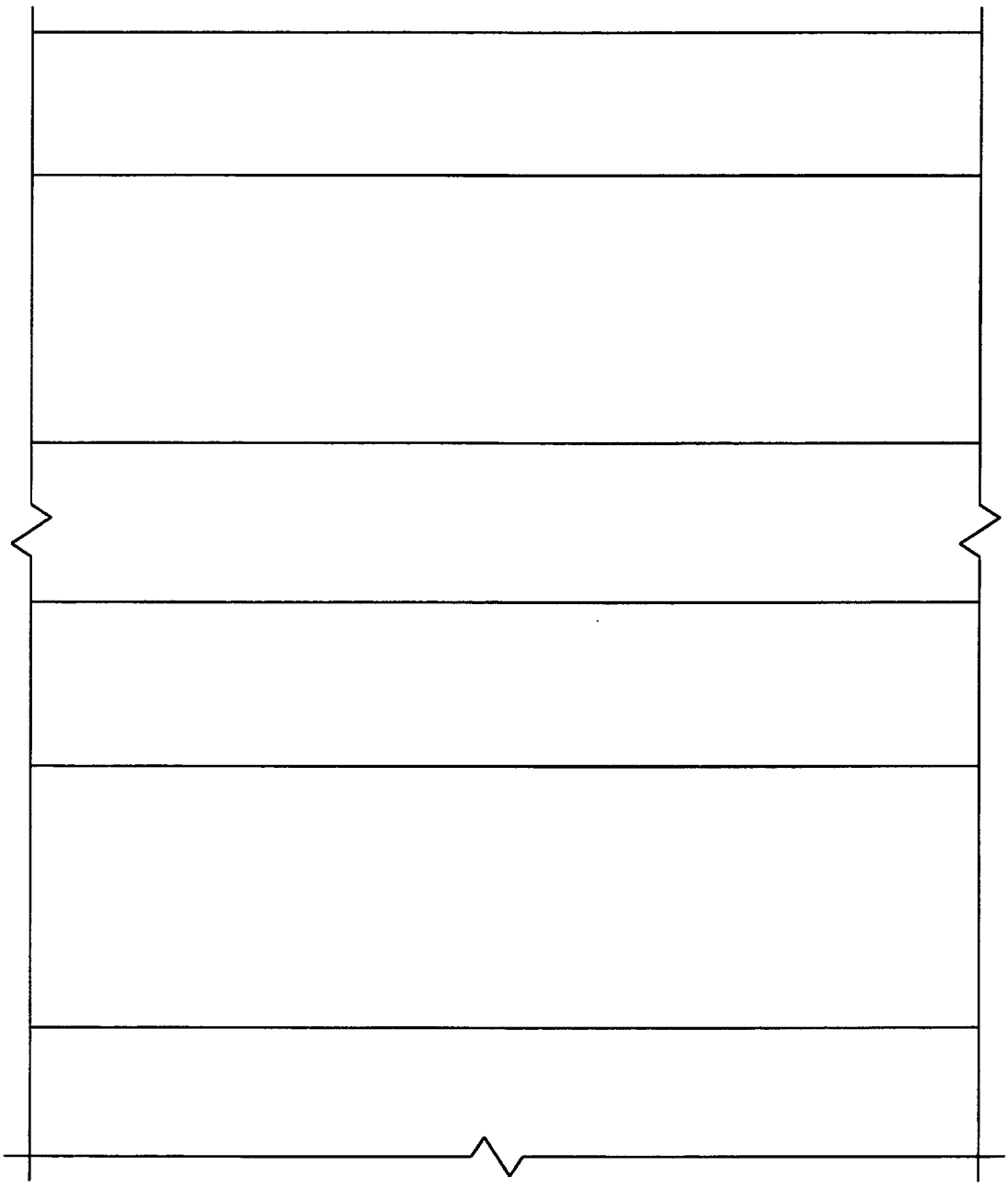

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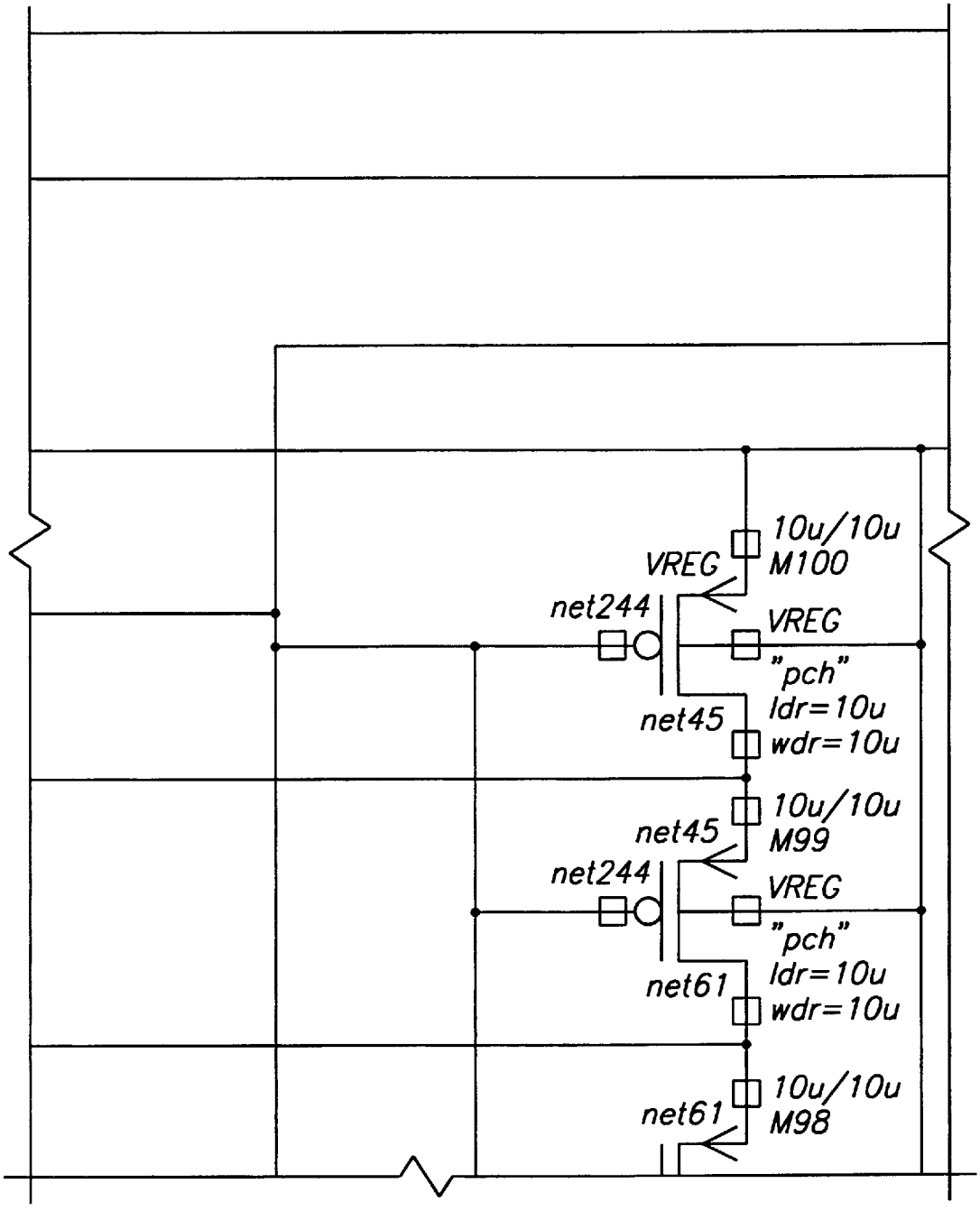
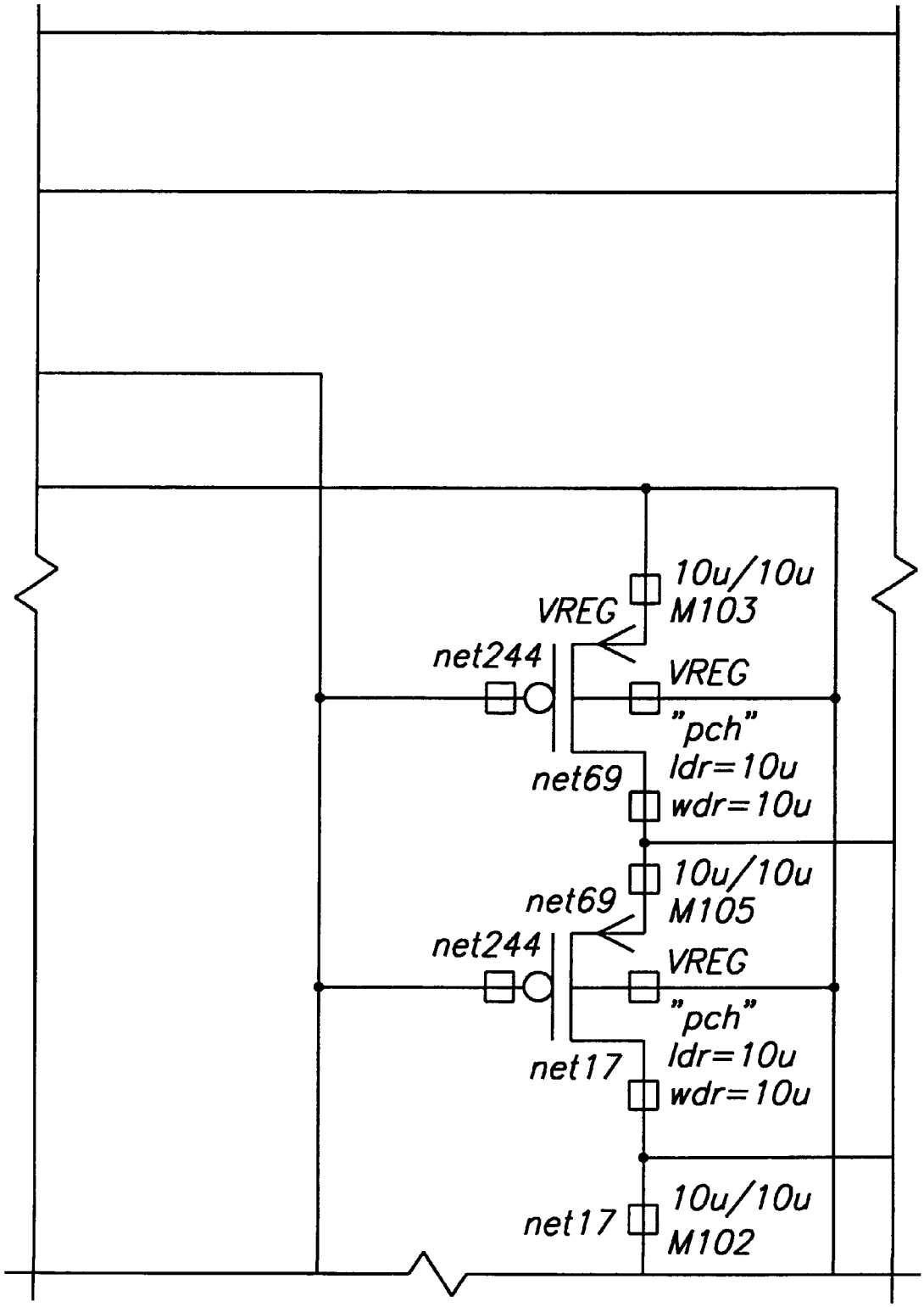


Fig 8.050405AII



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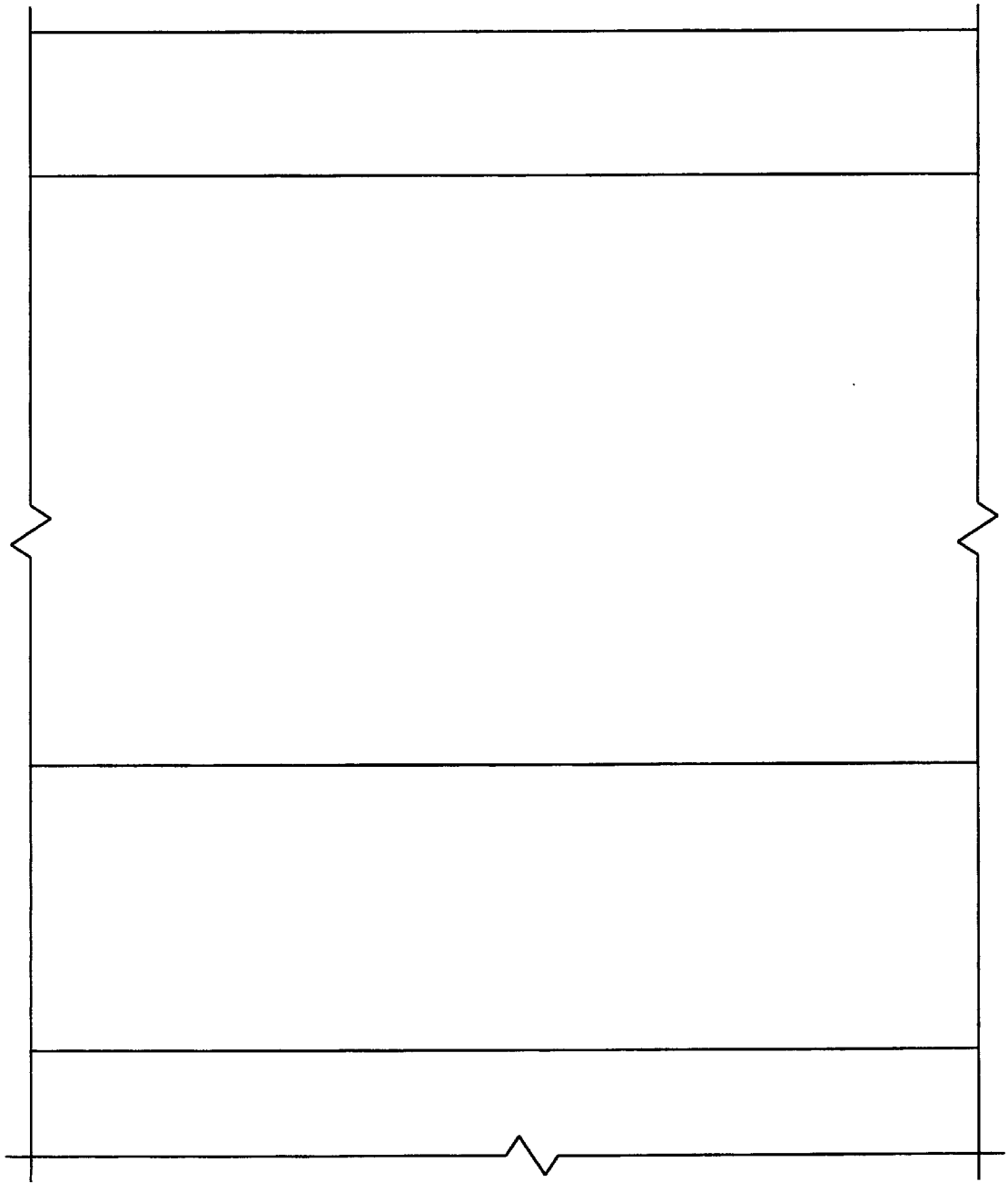

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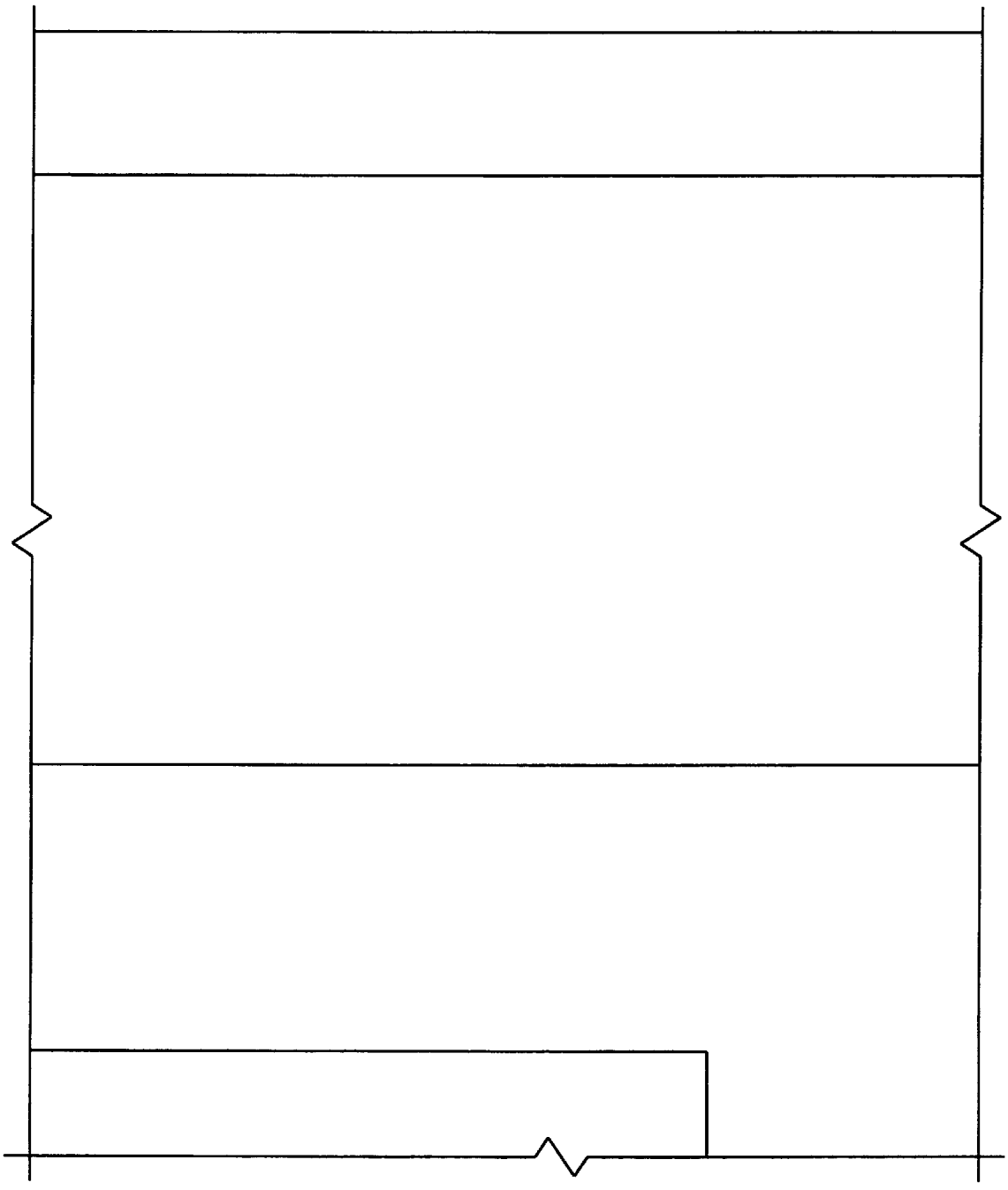

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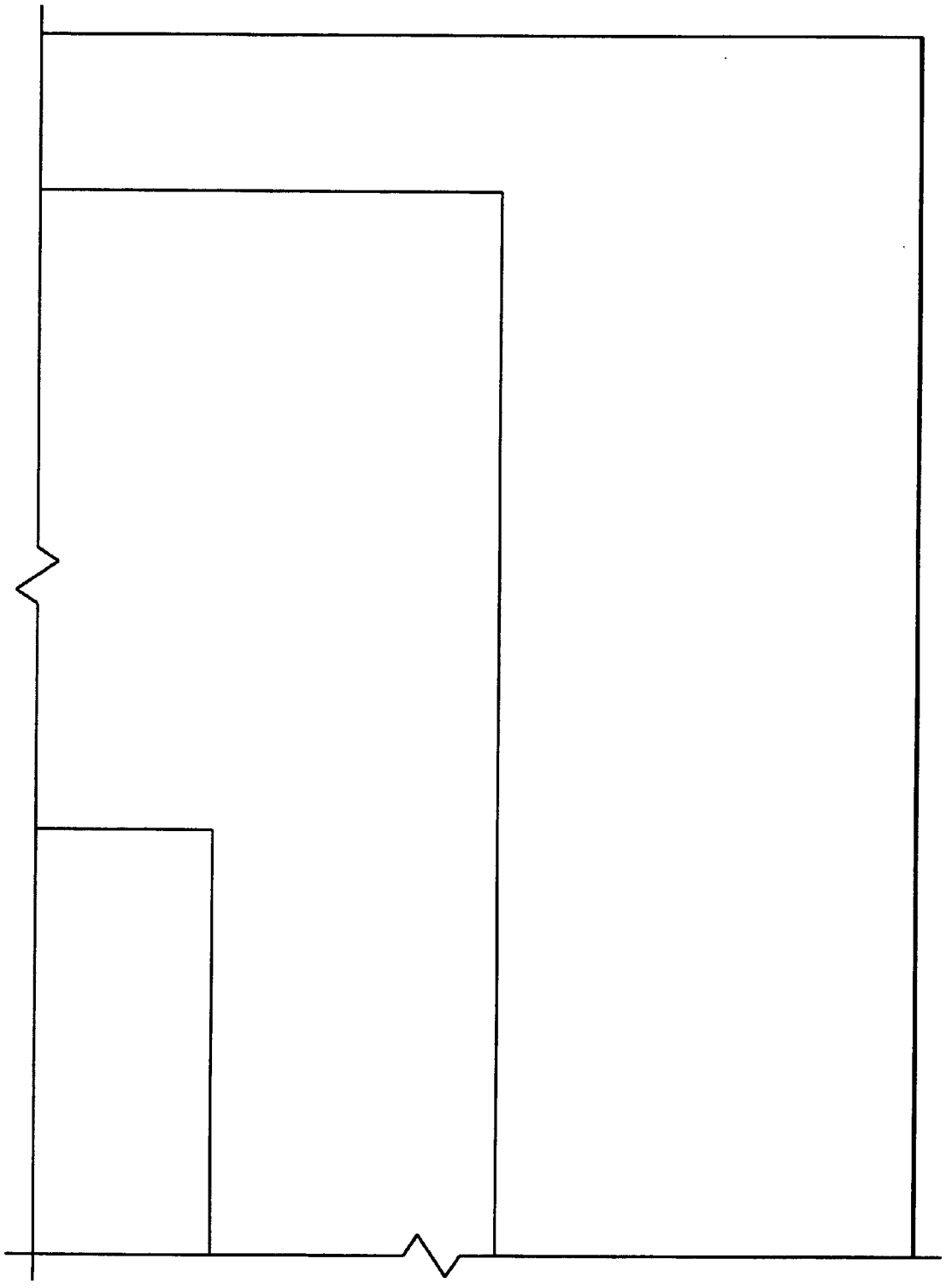

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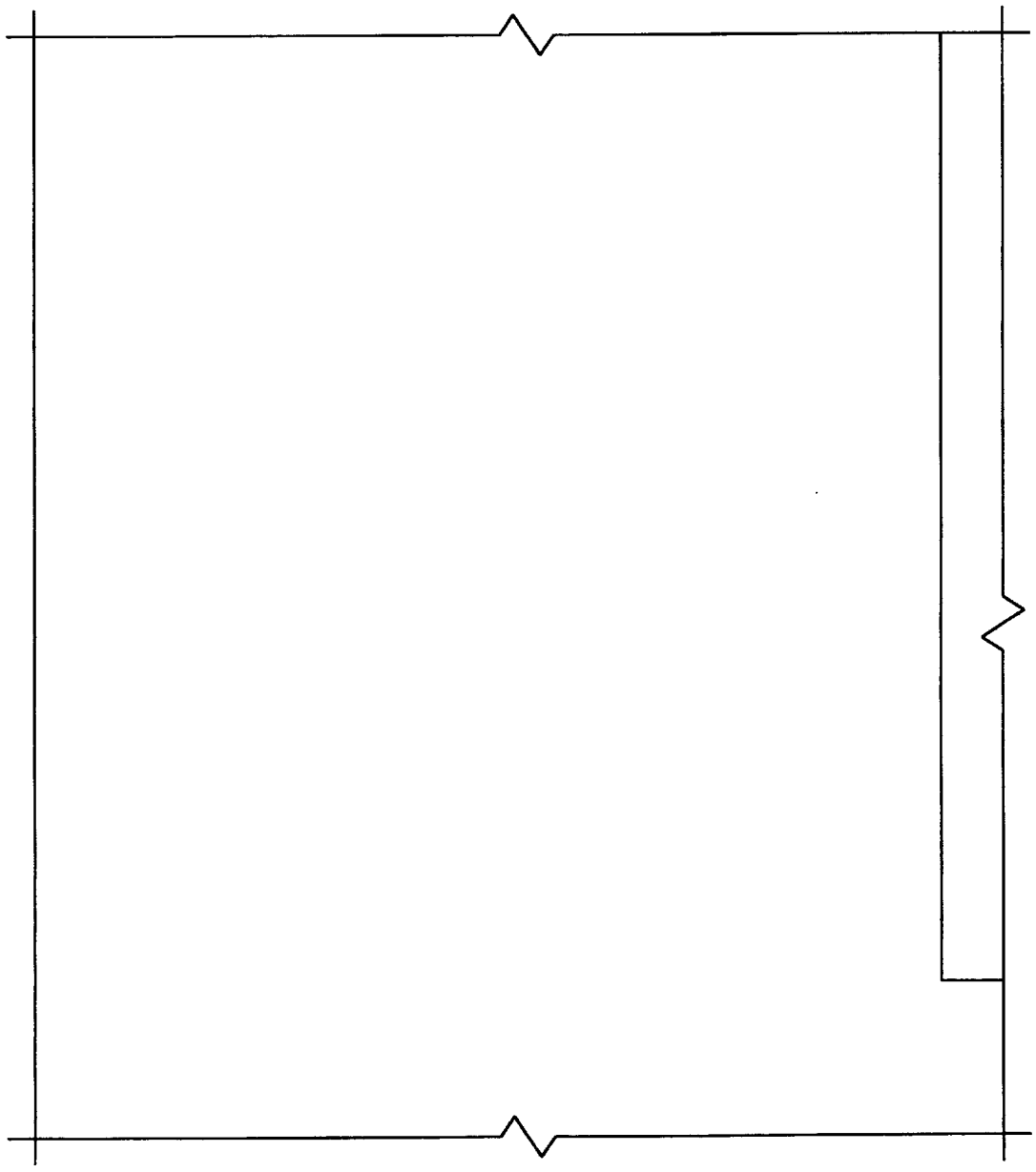

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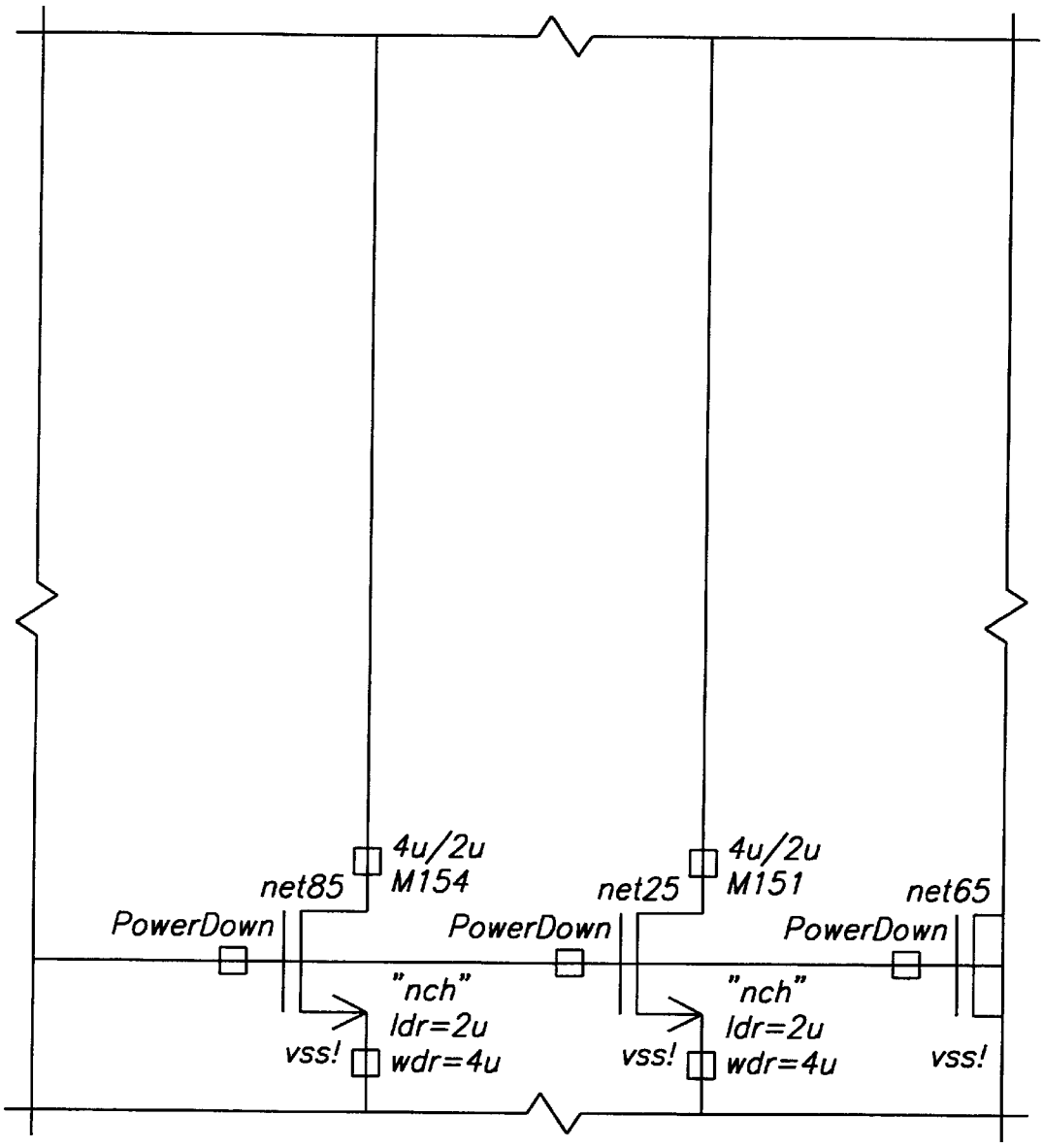

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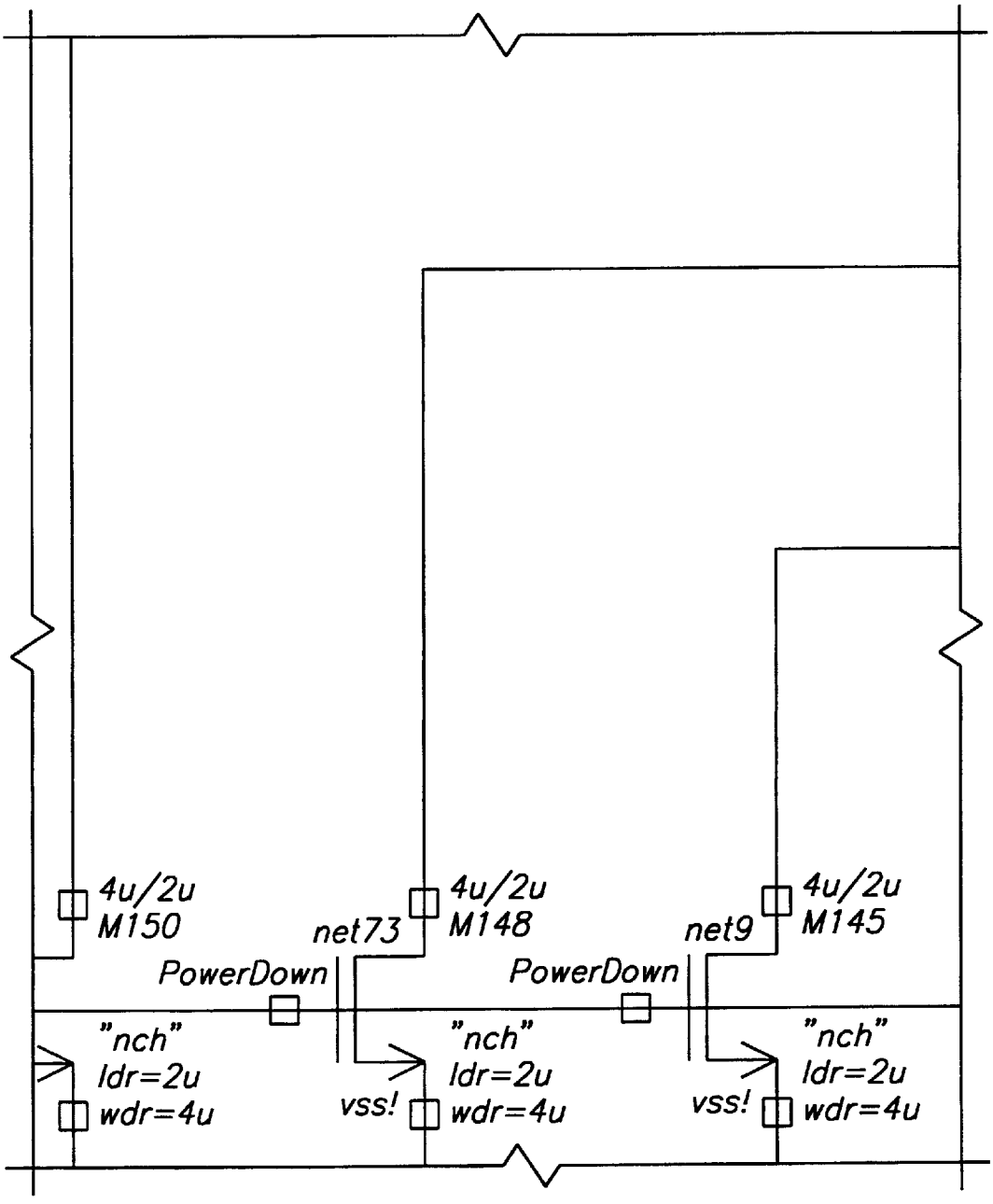

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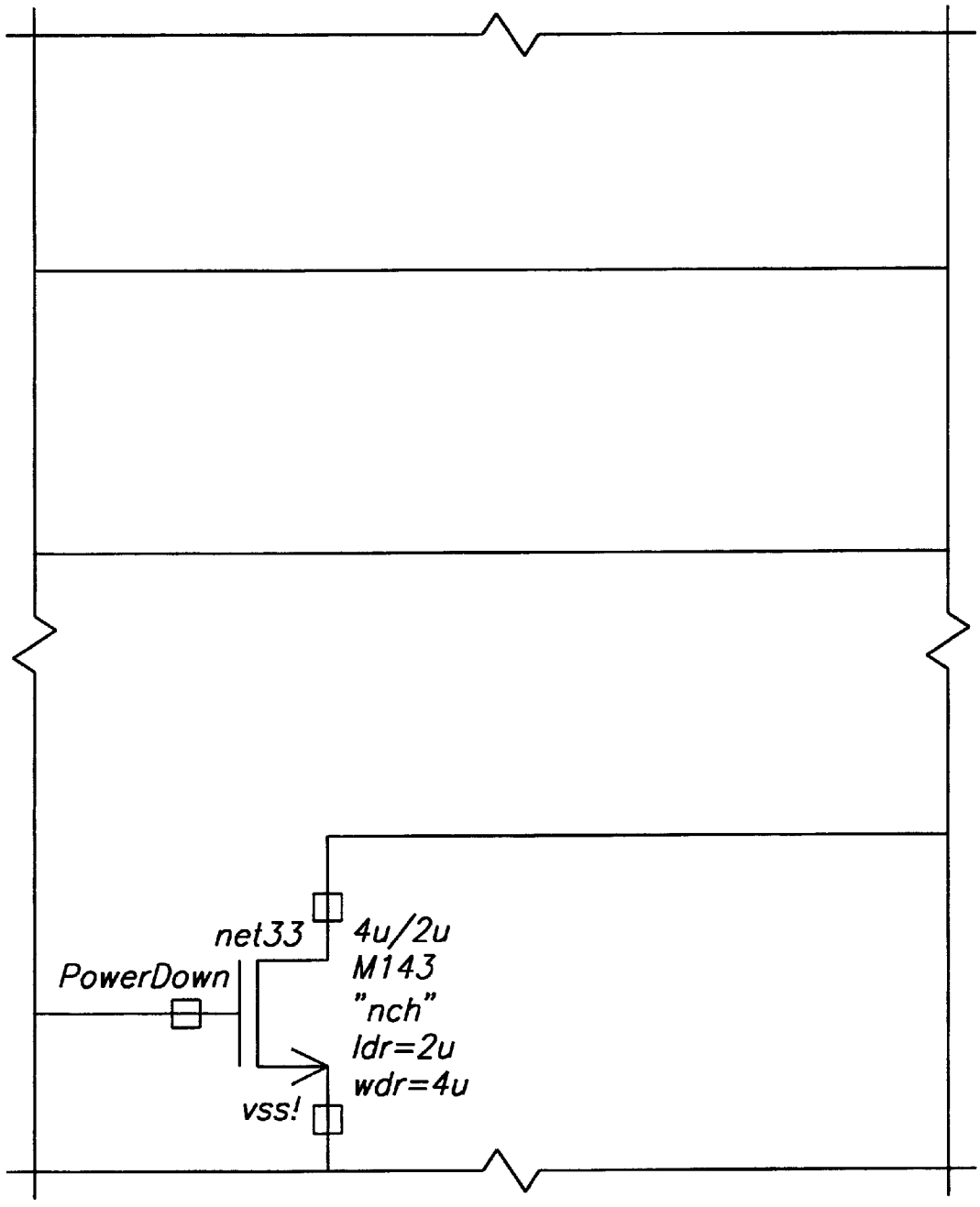

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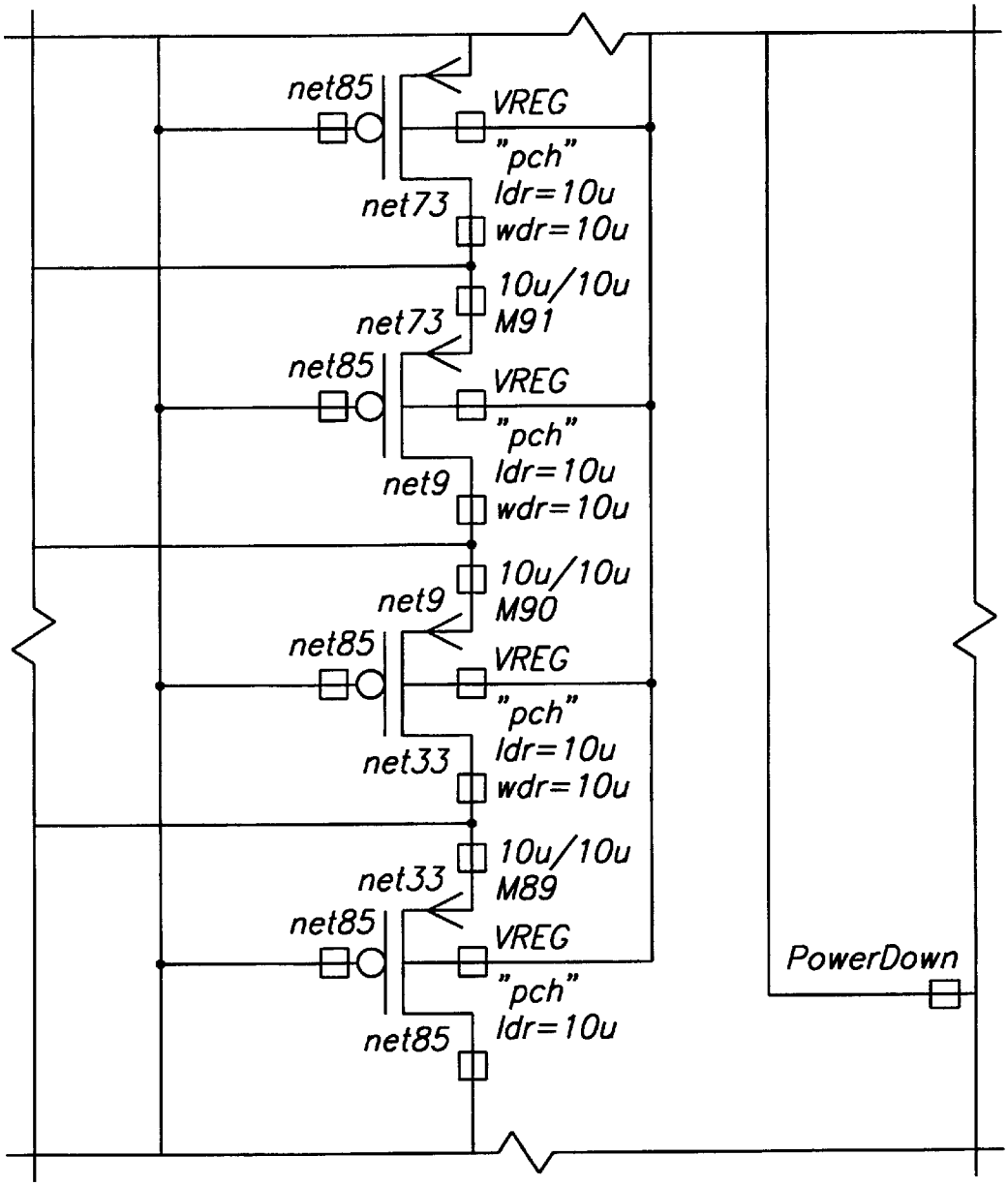

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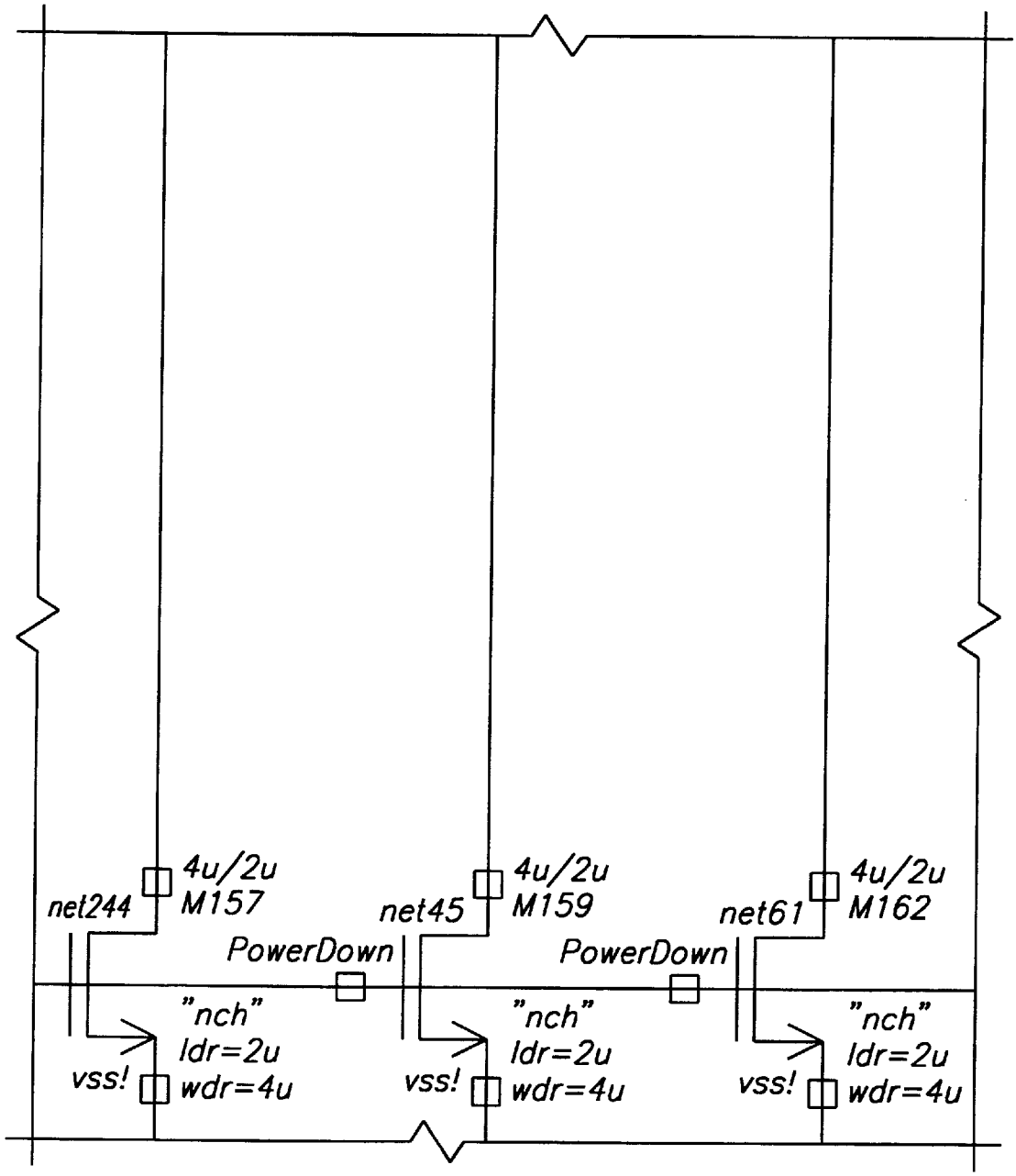
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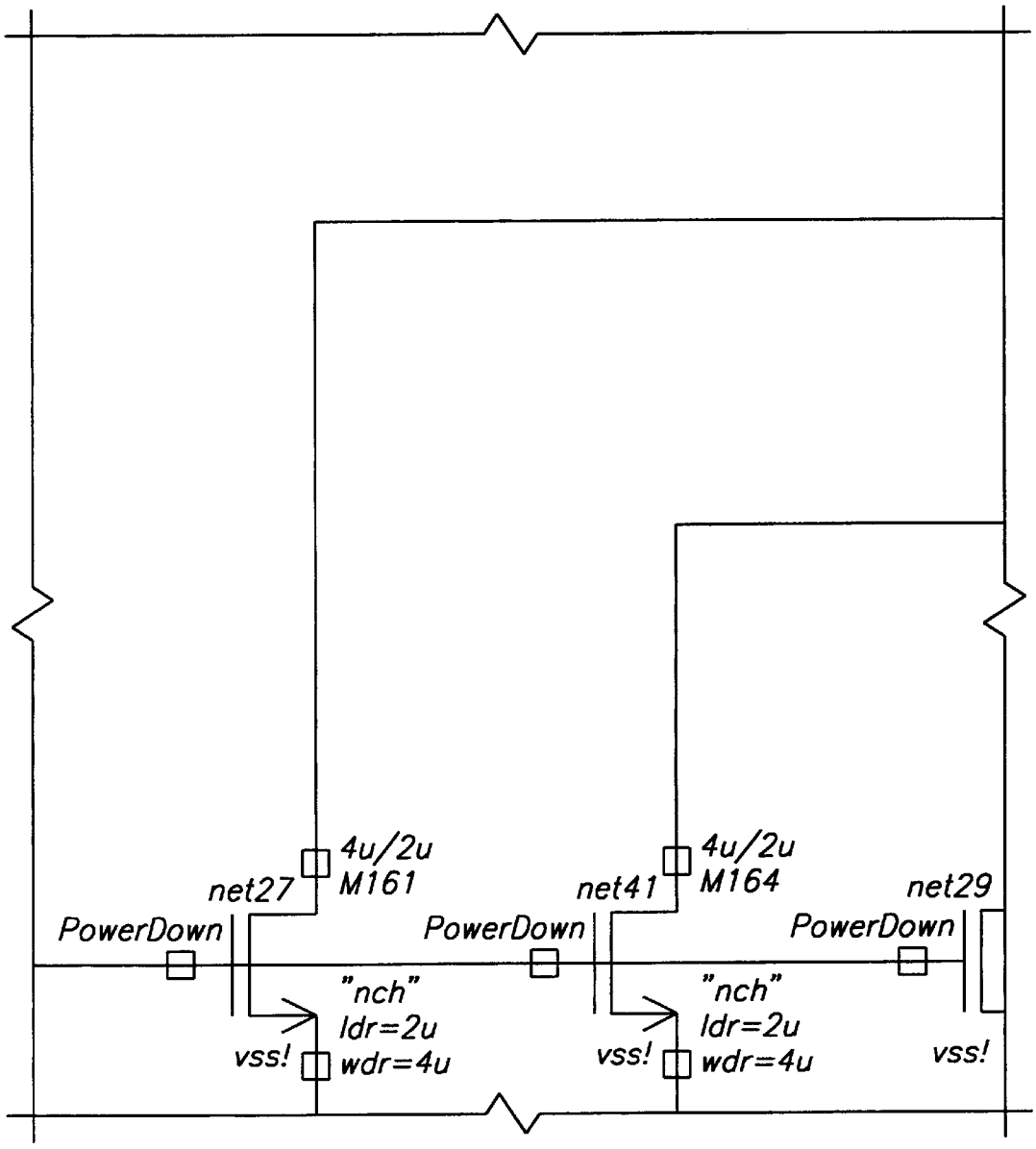

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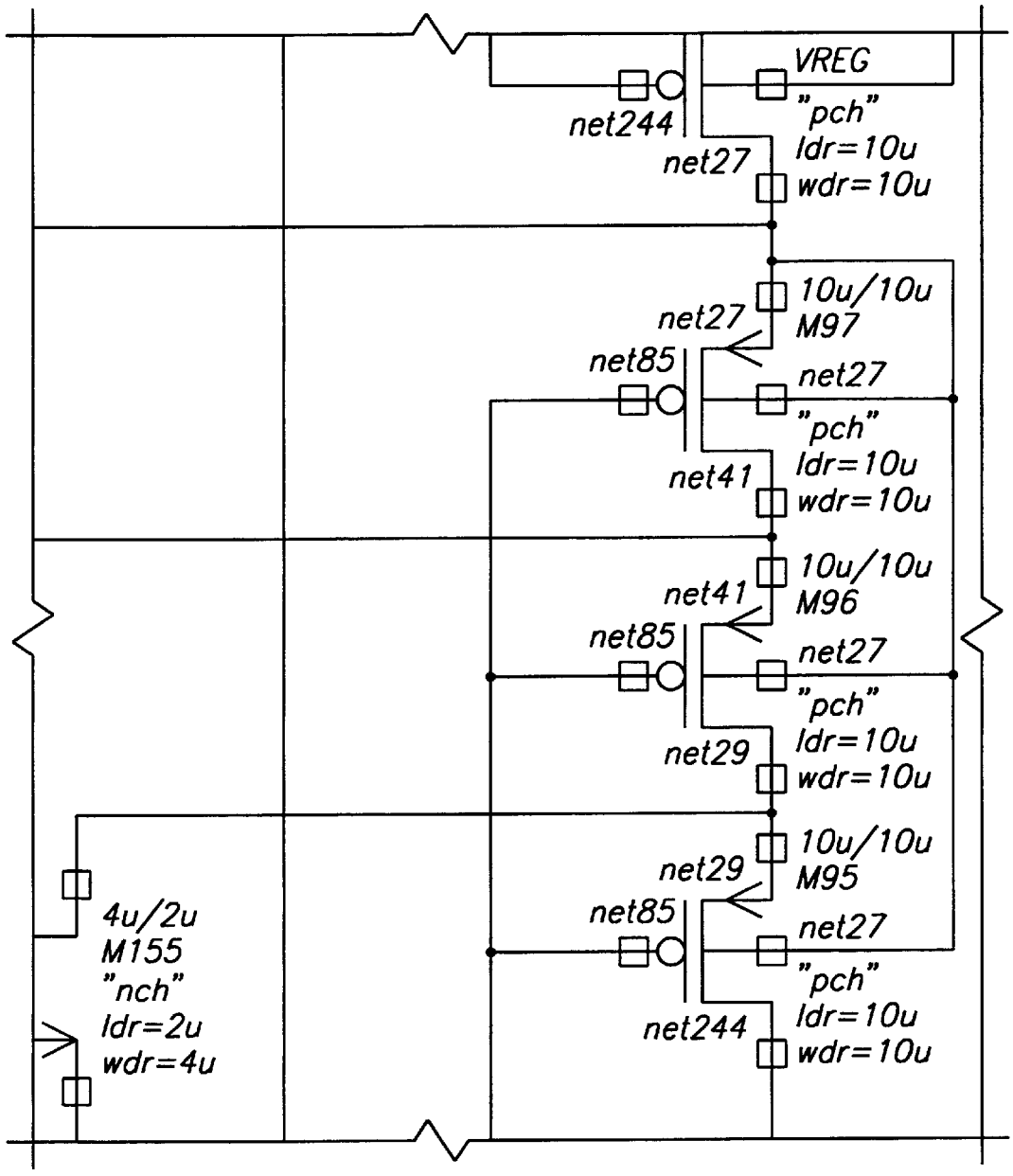

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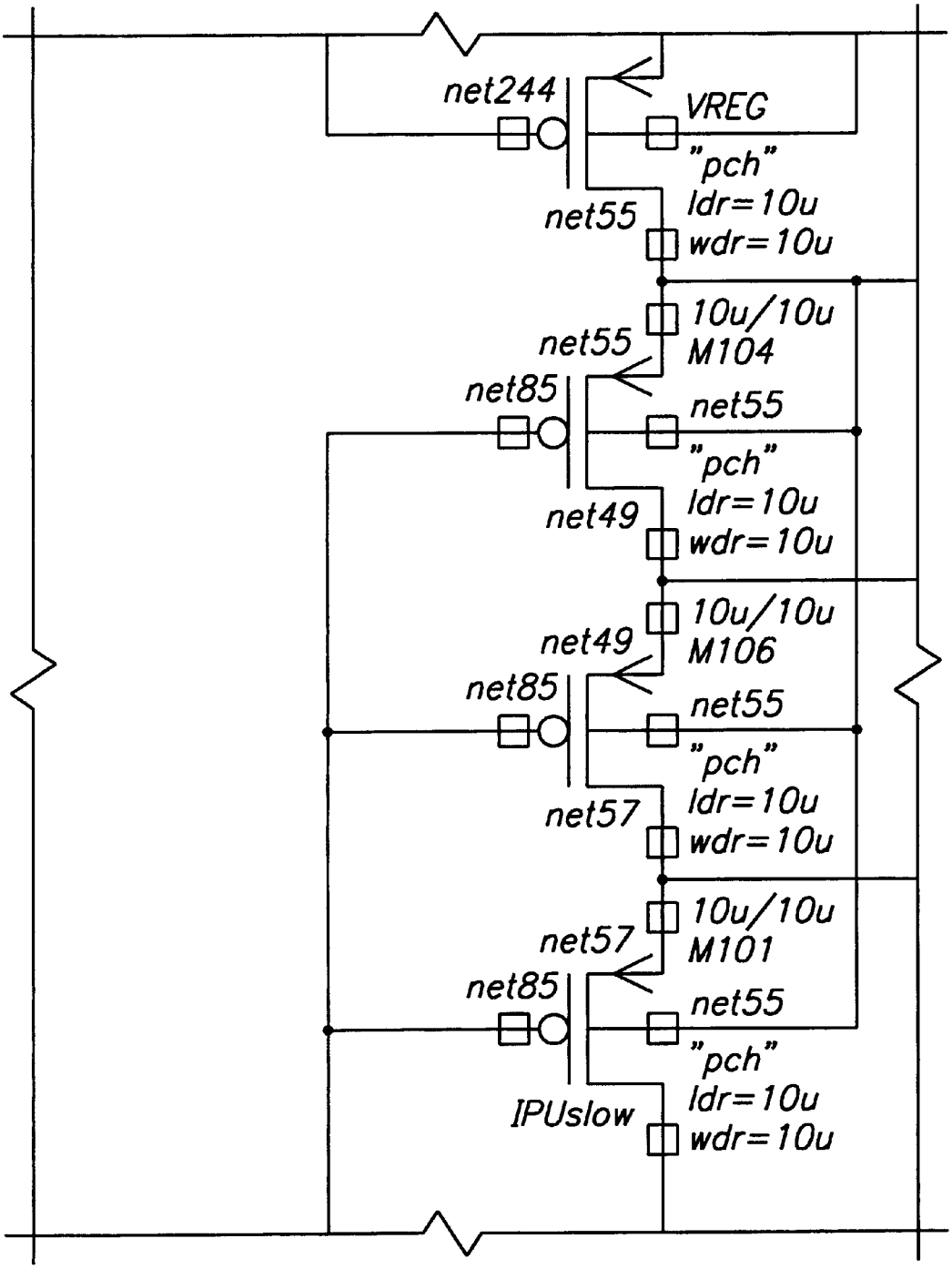

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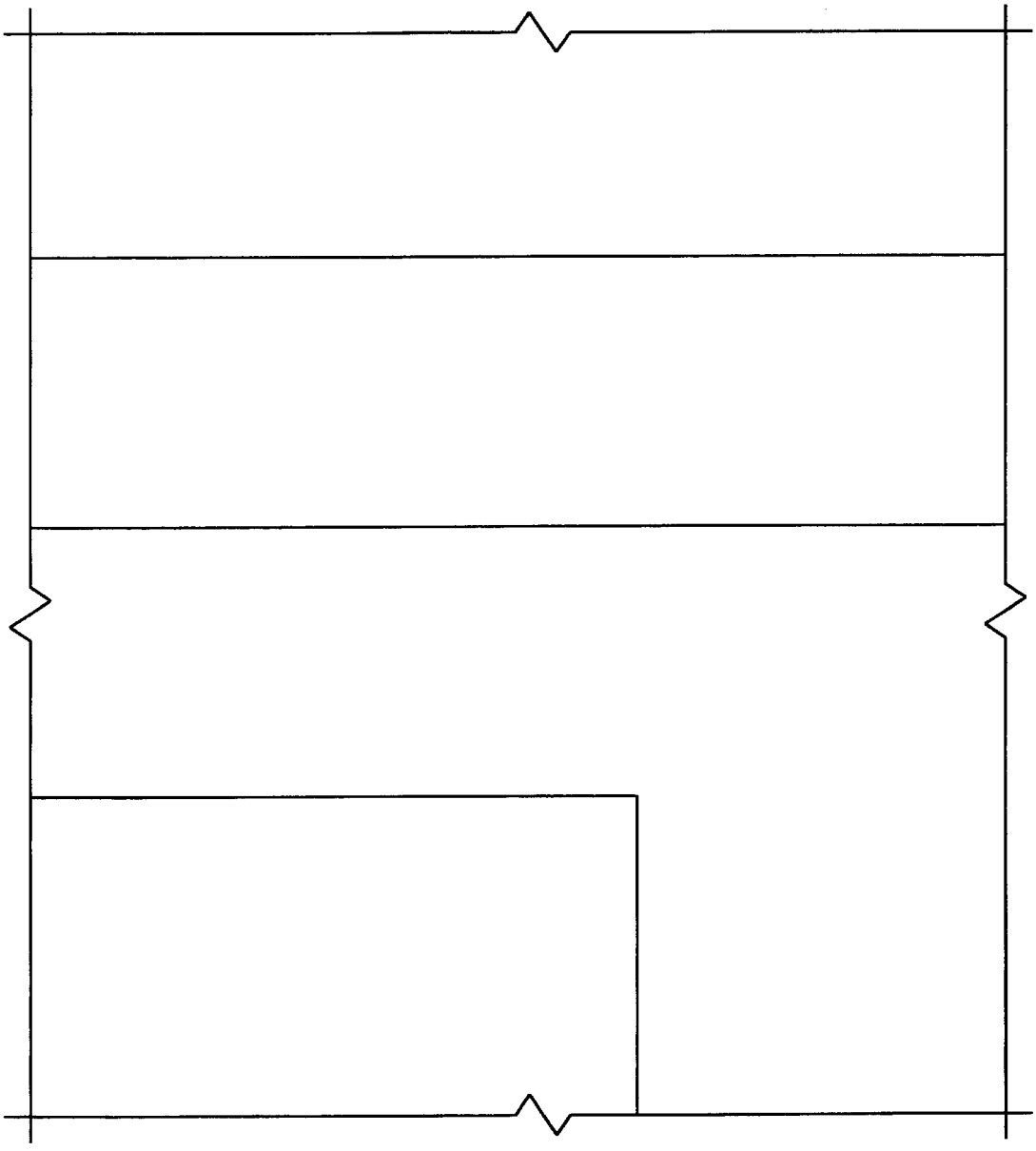

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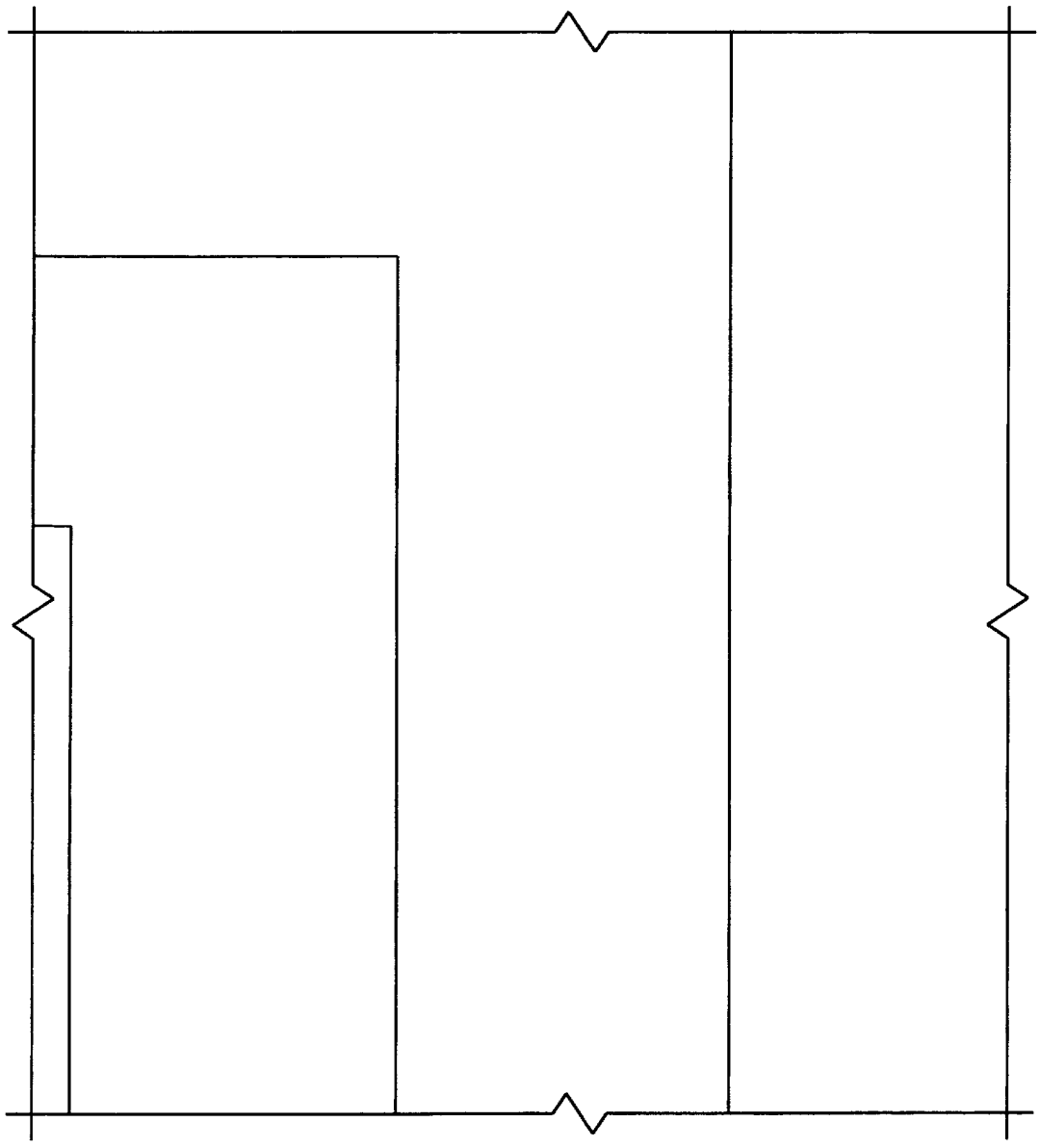

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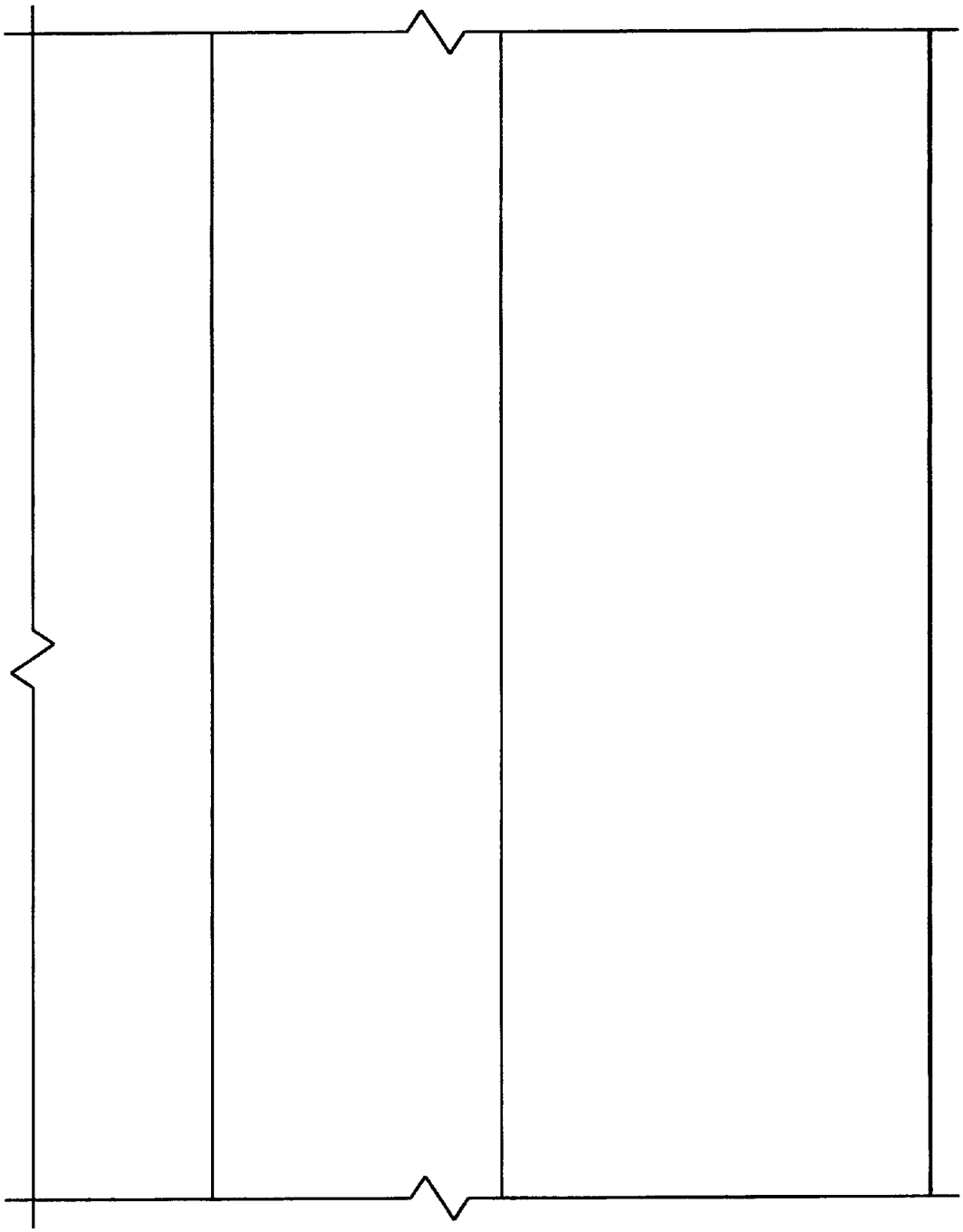

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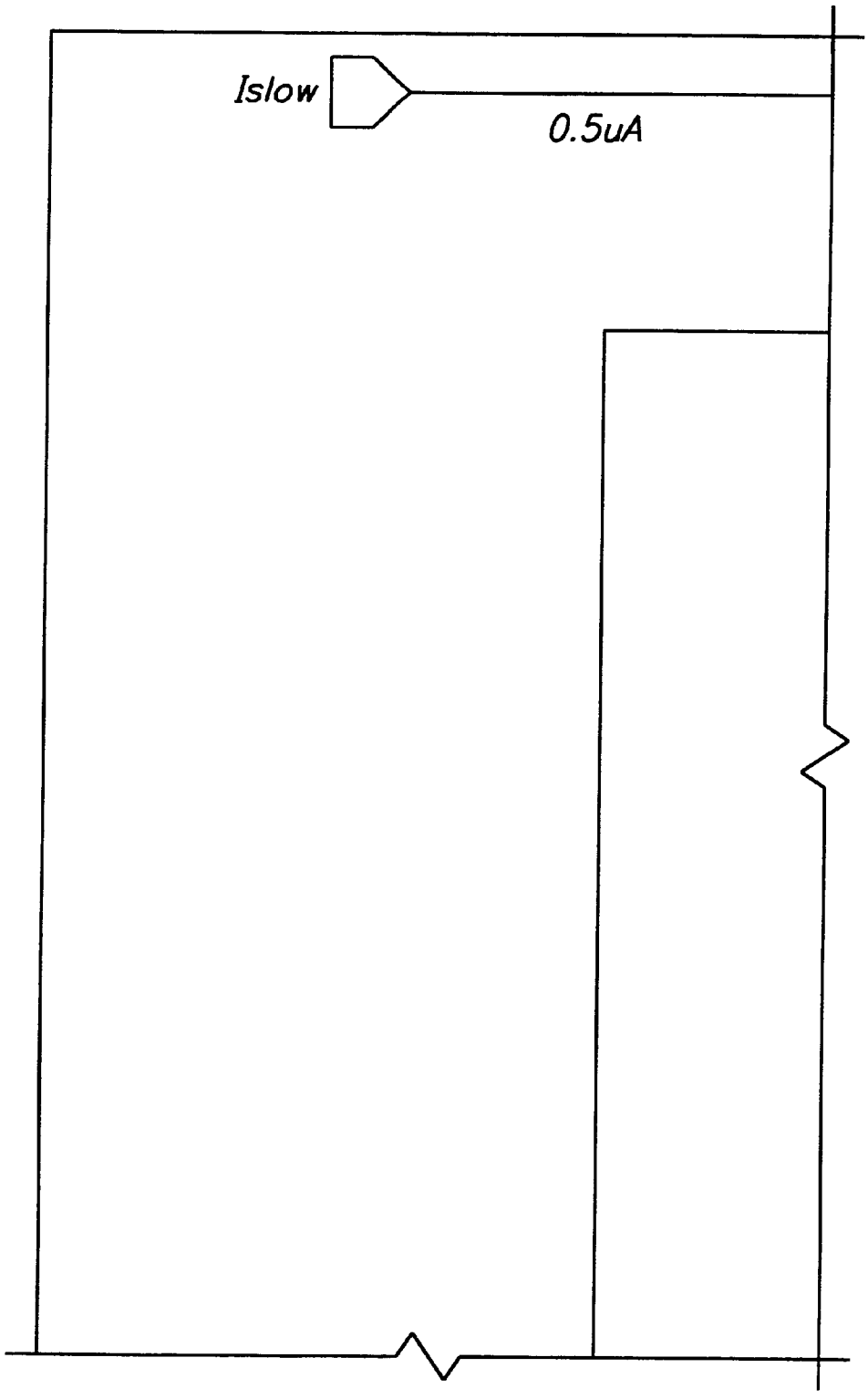

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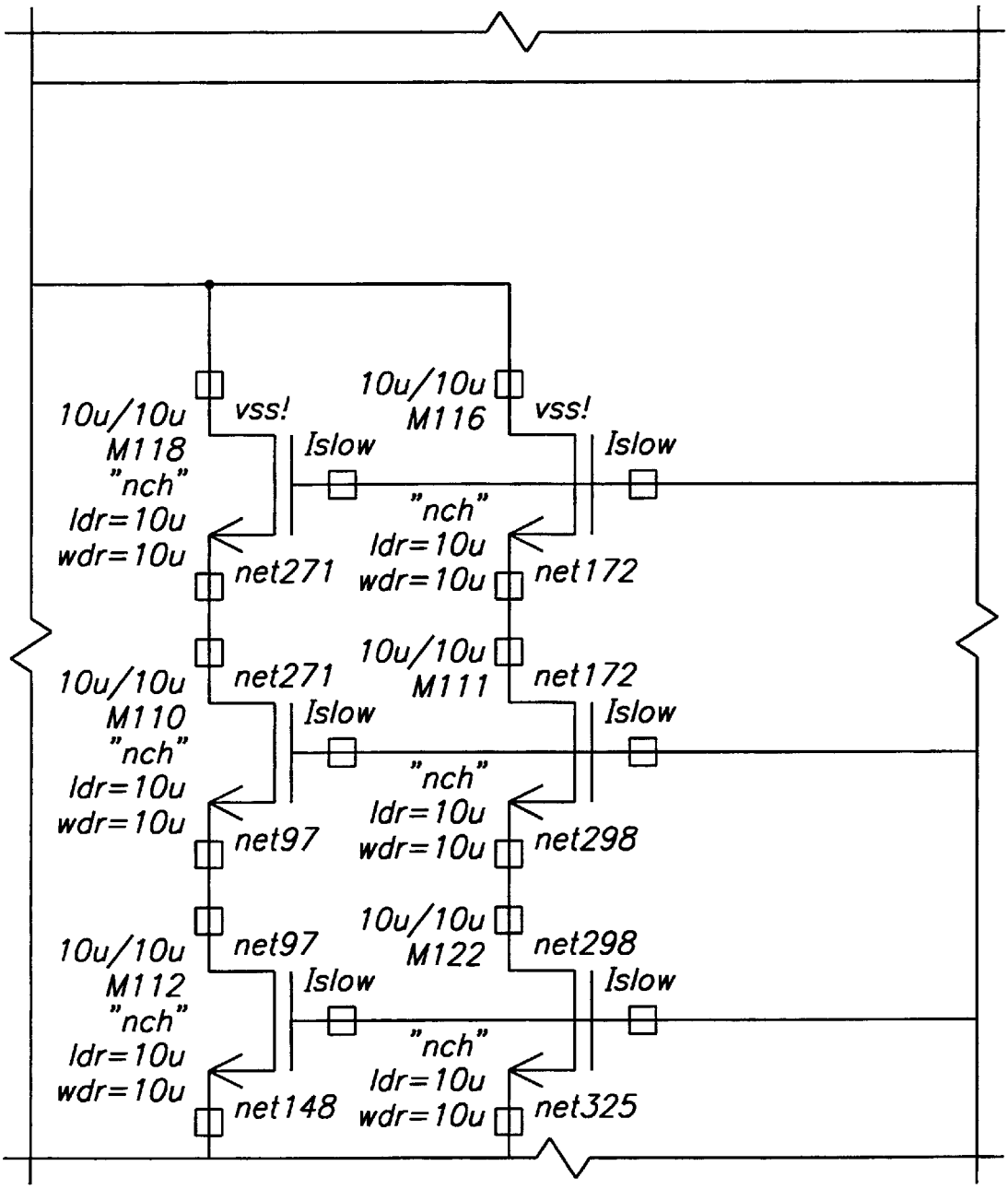
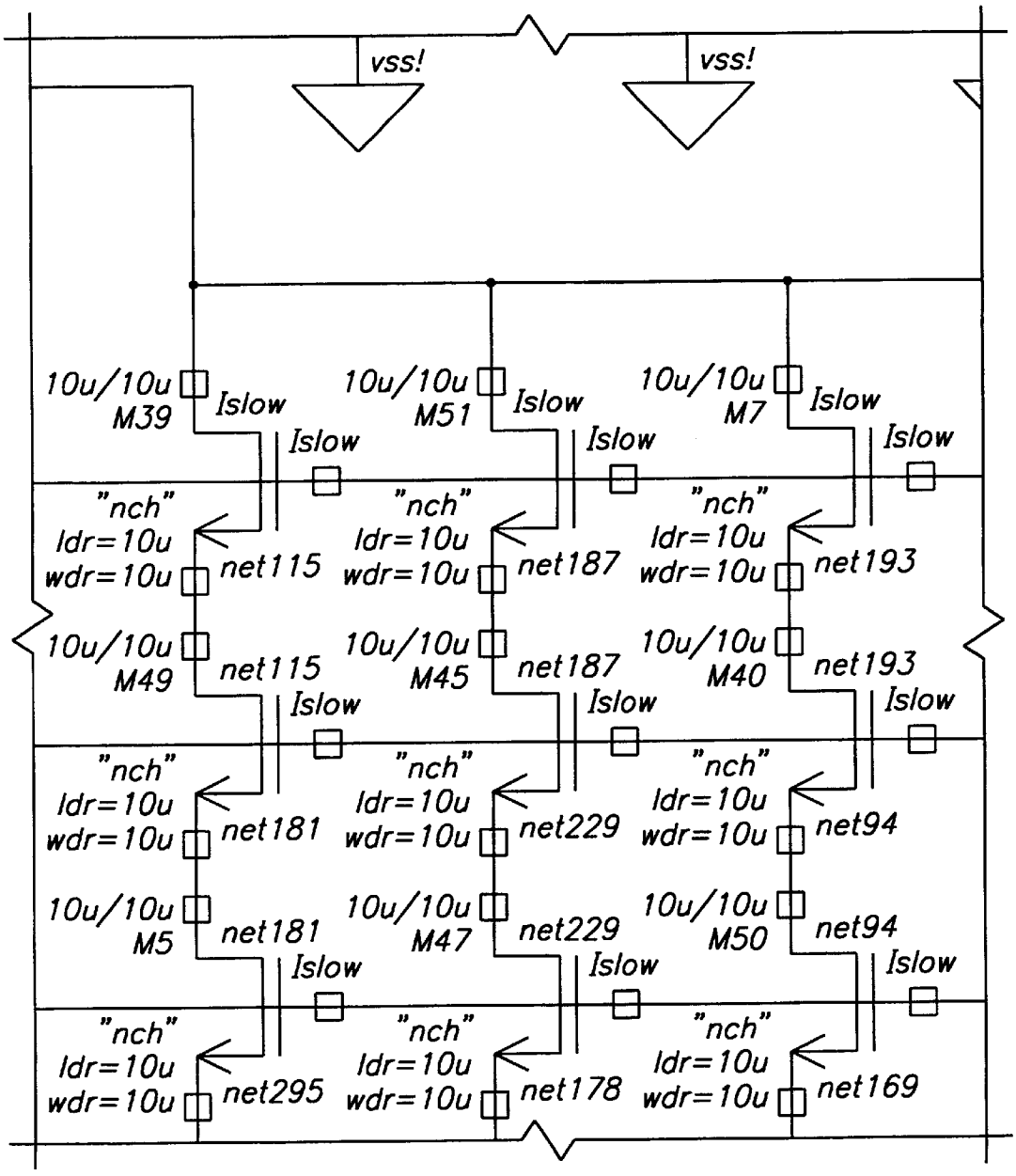


Fig 8,050,405C



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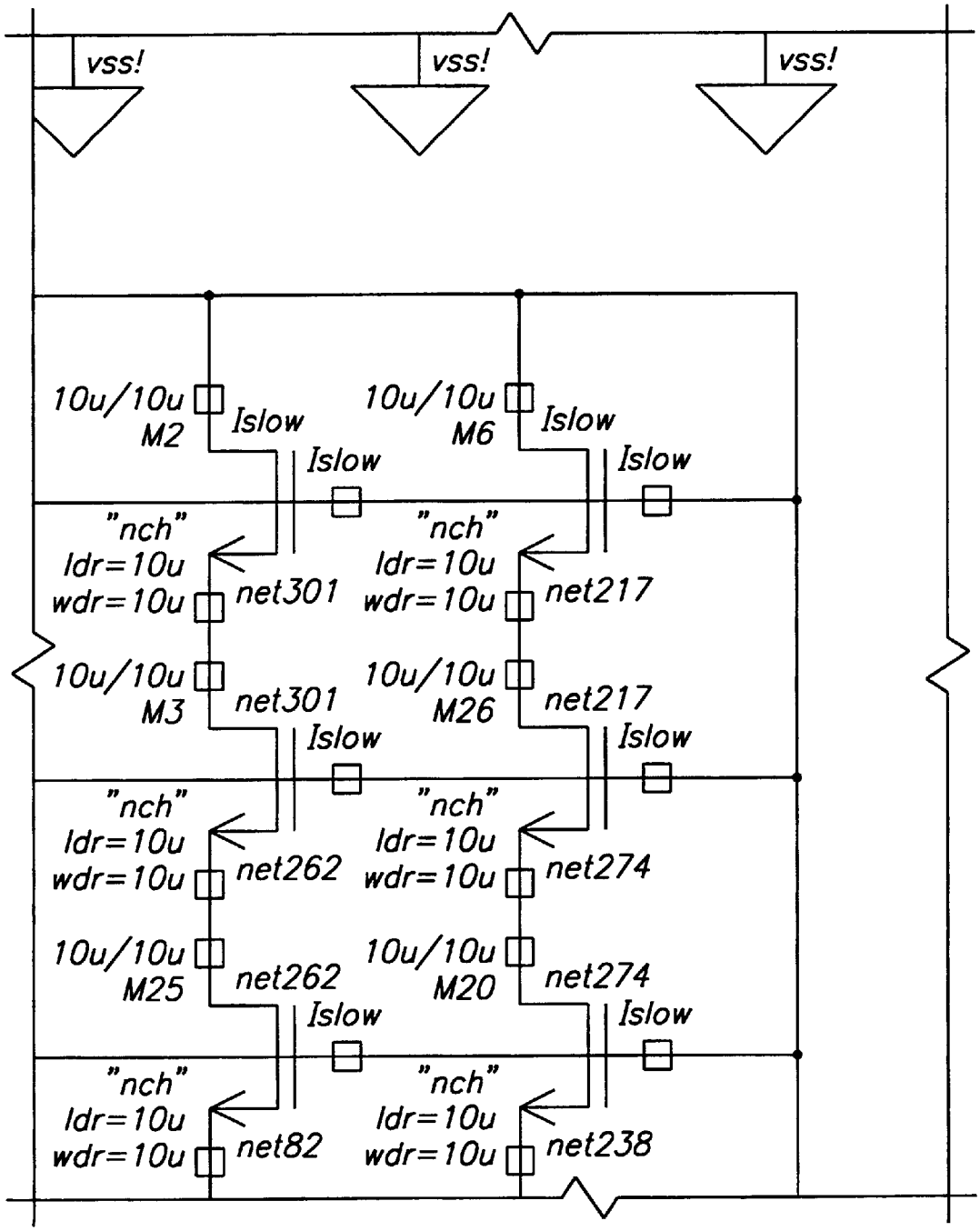

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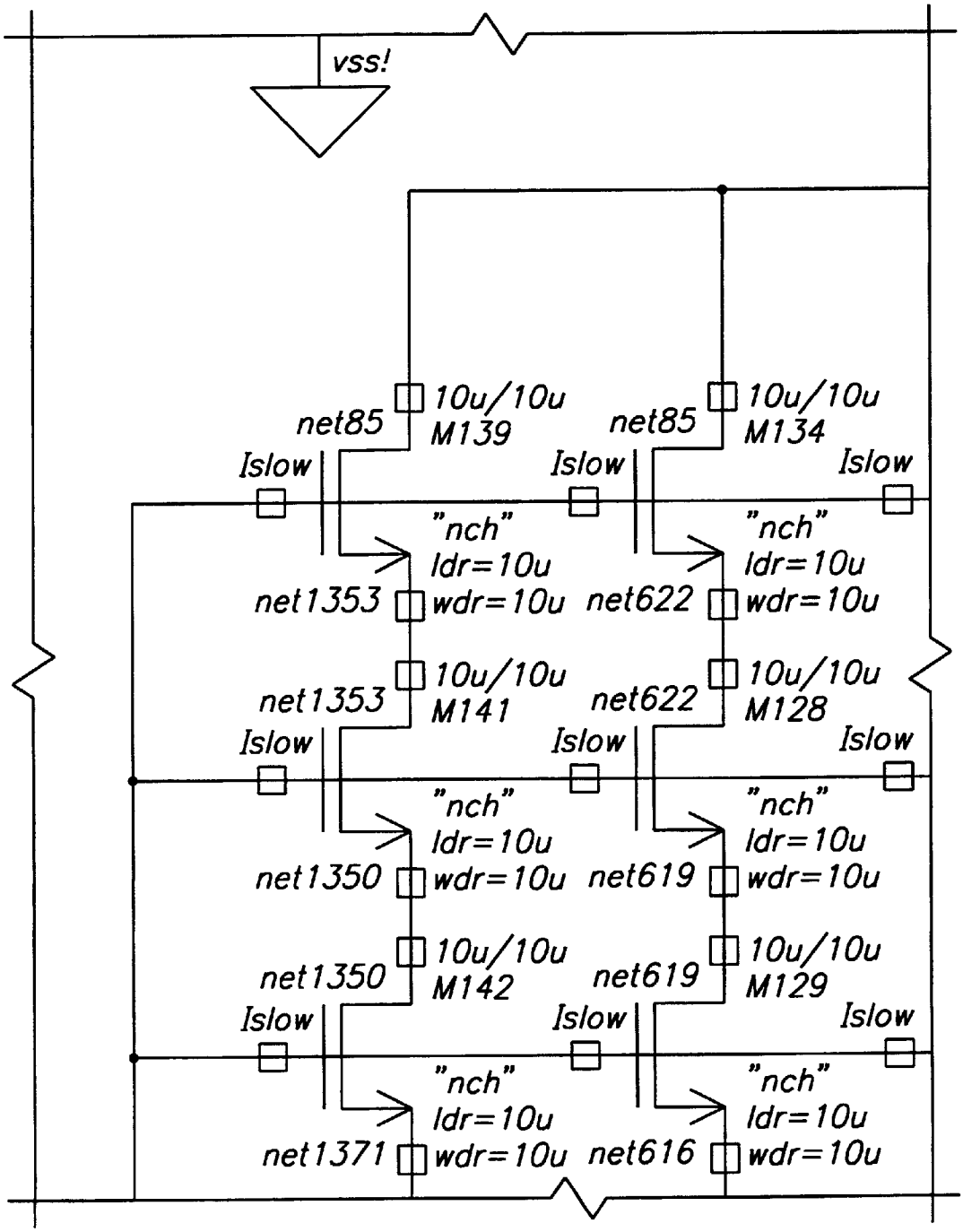
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Fig 8,054,056

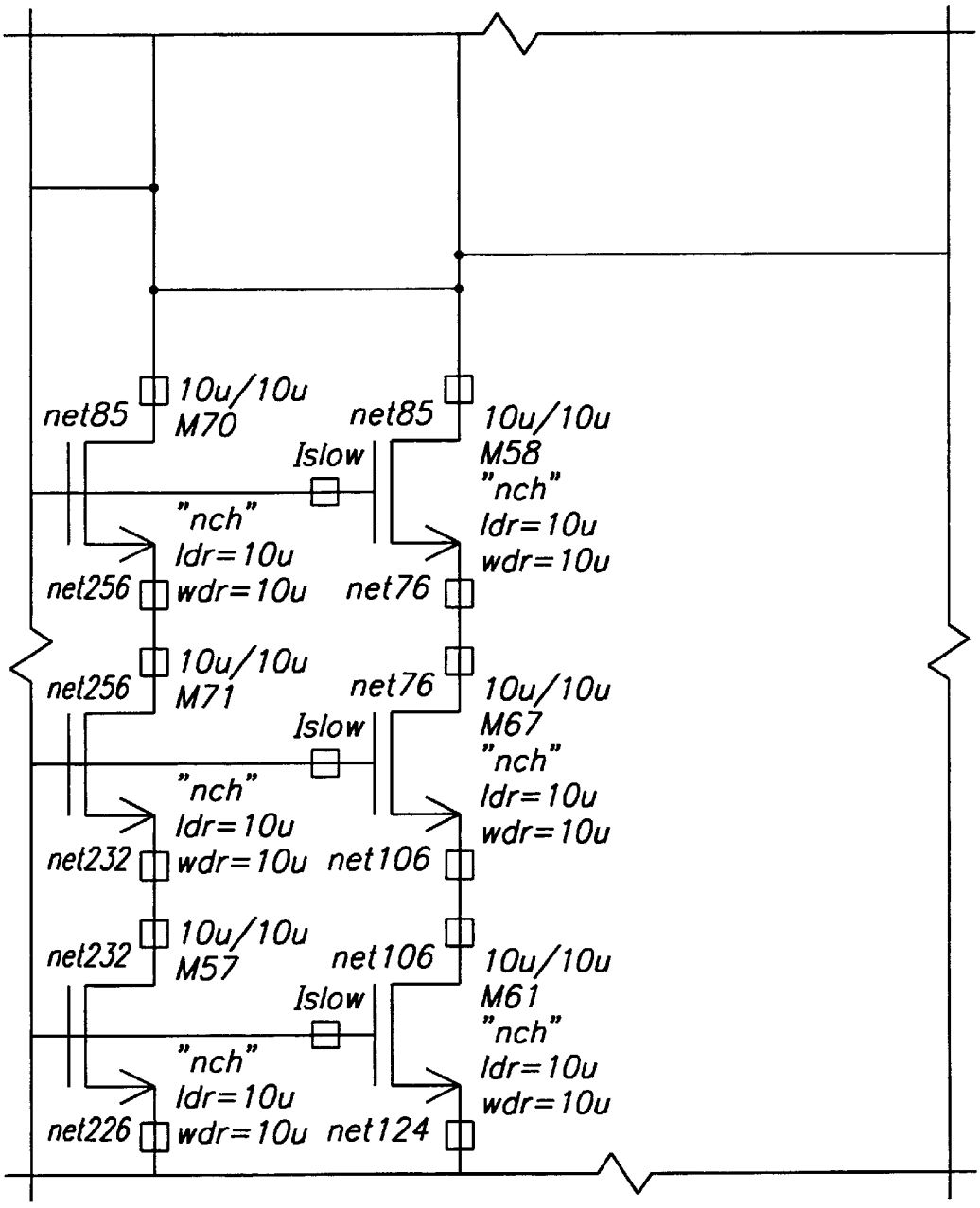
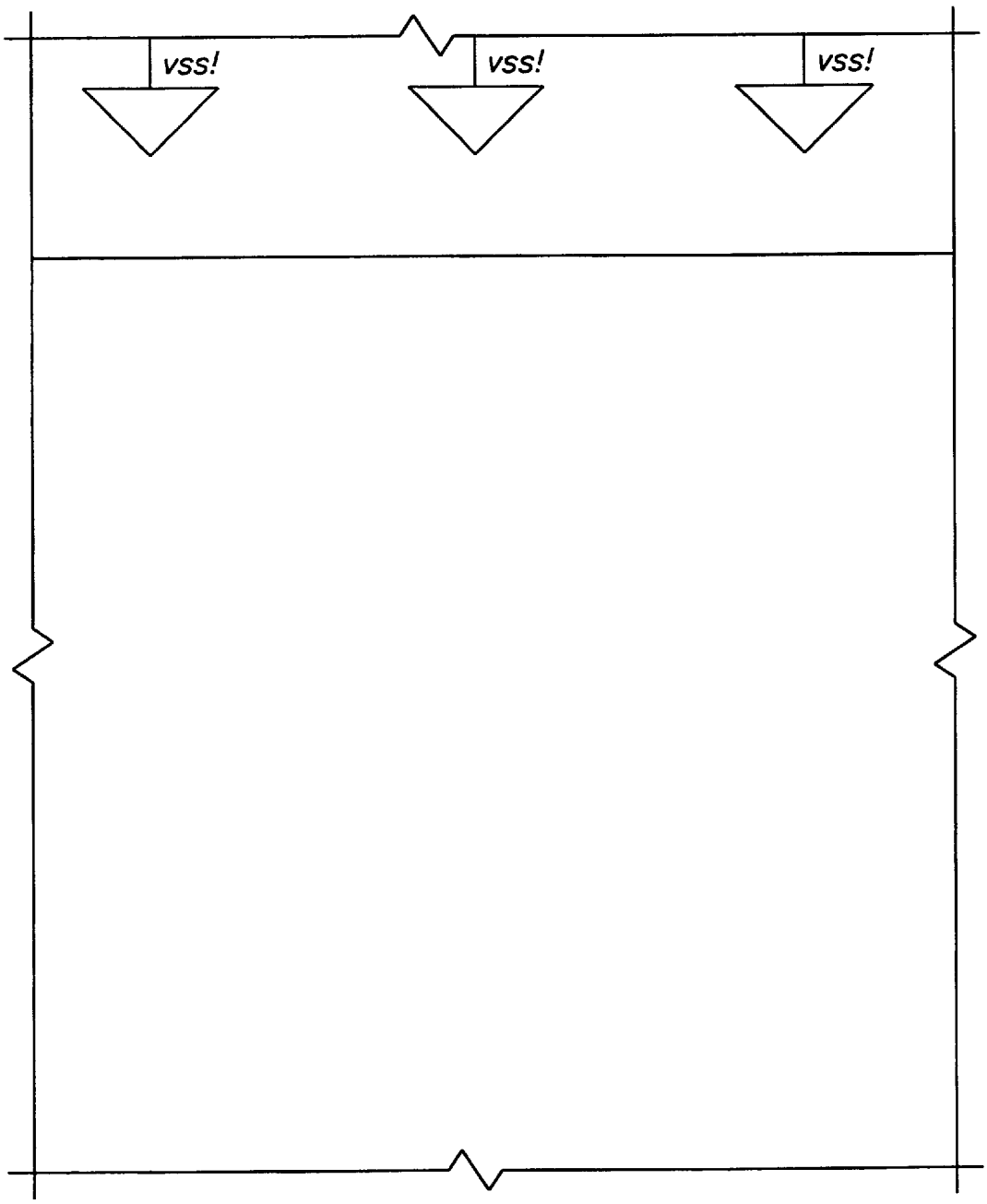


Fig 8.0504.05CF



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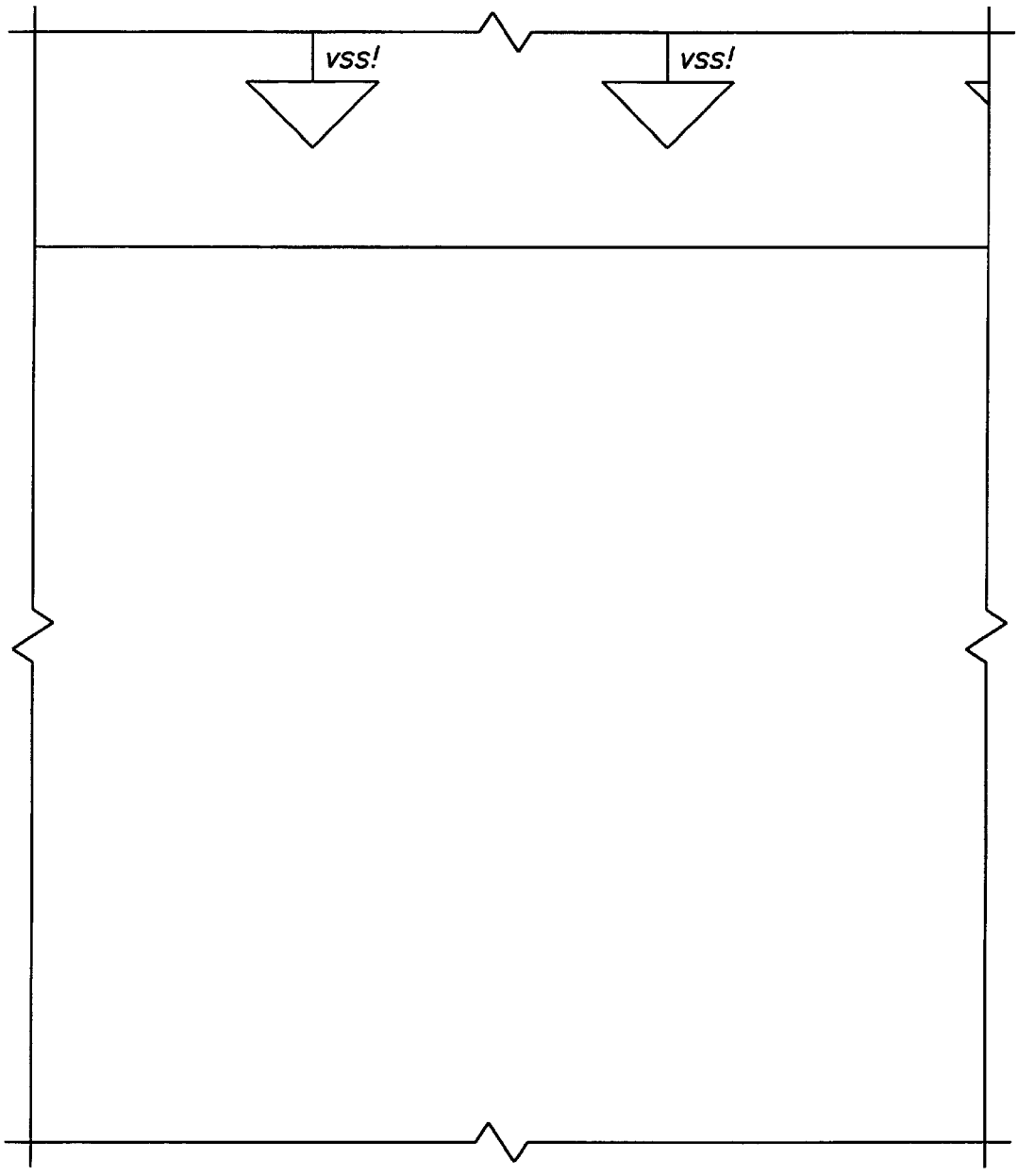

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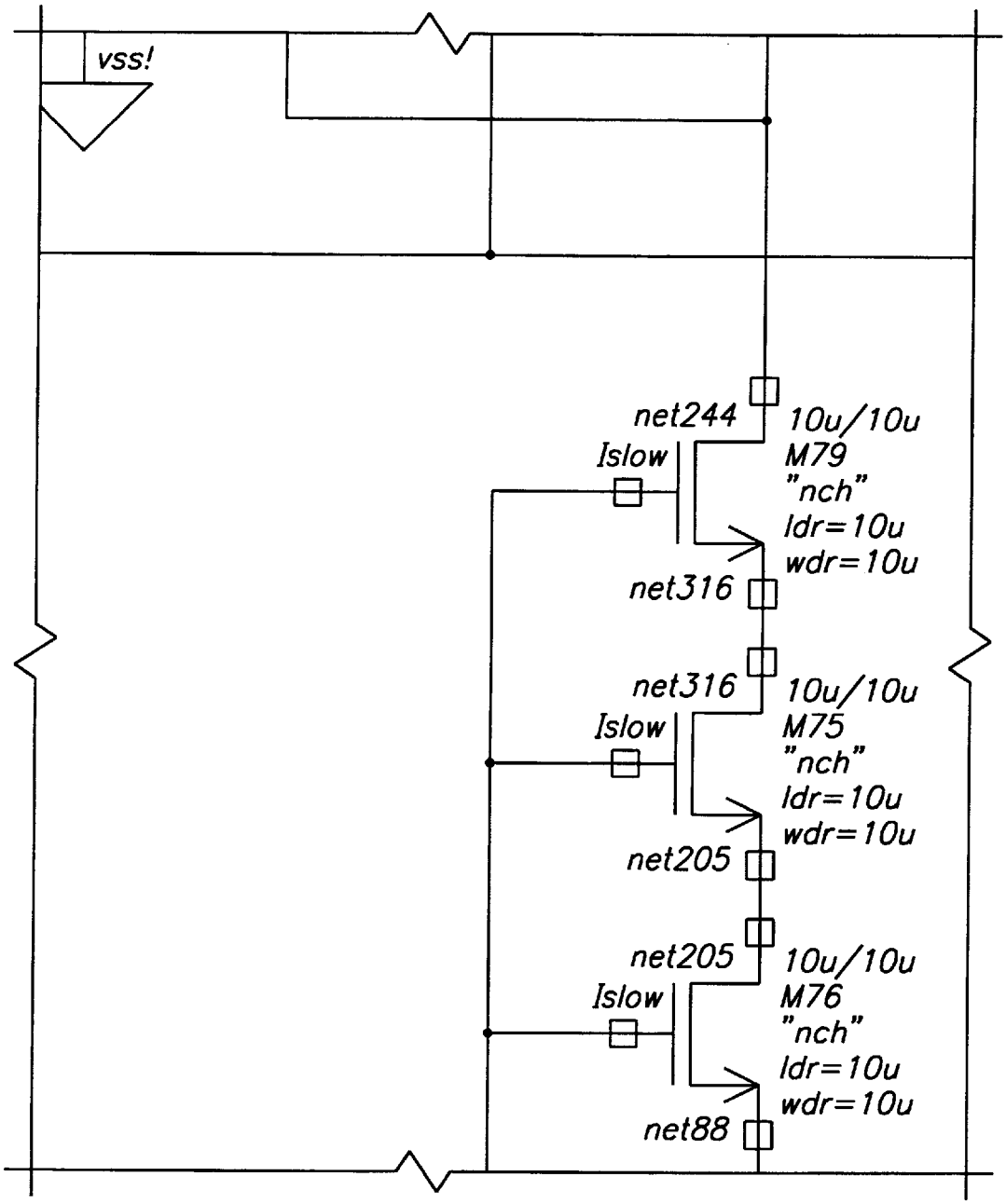
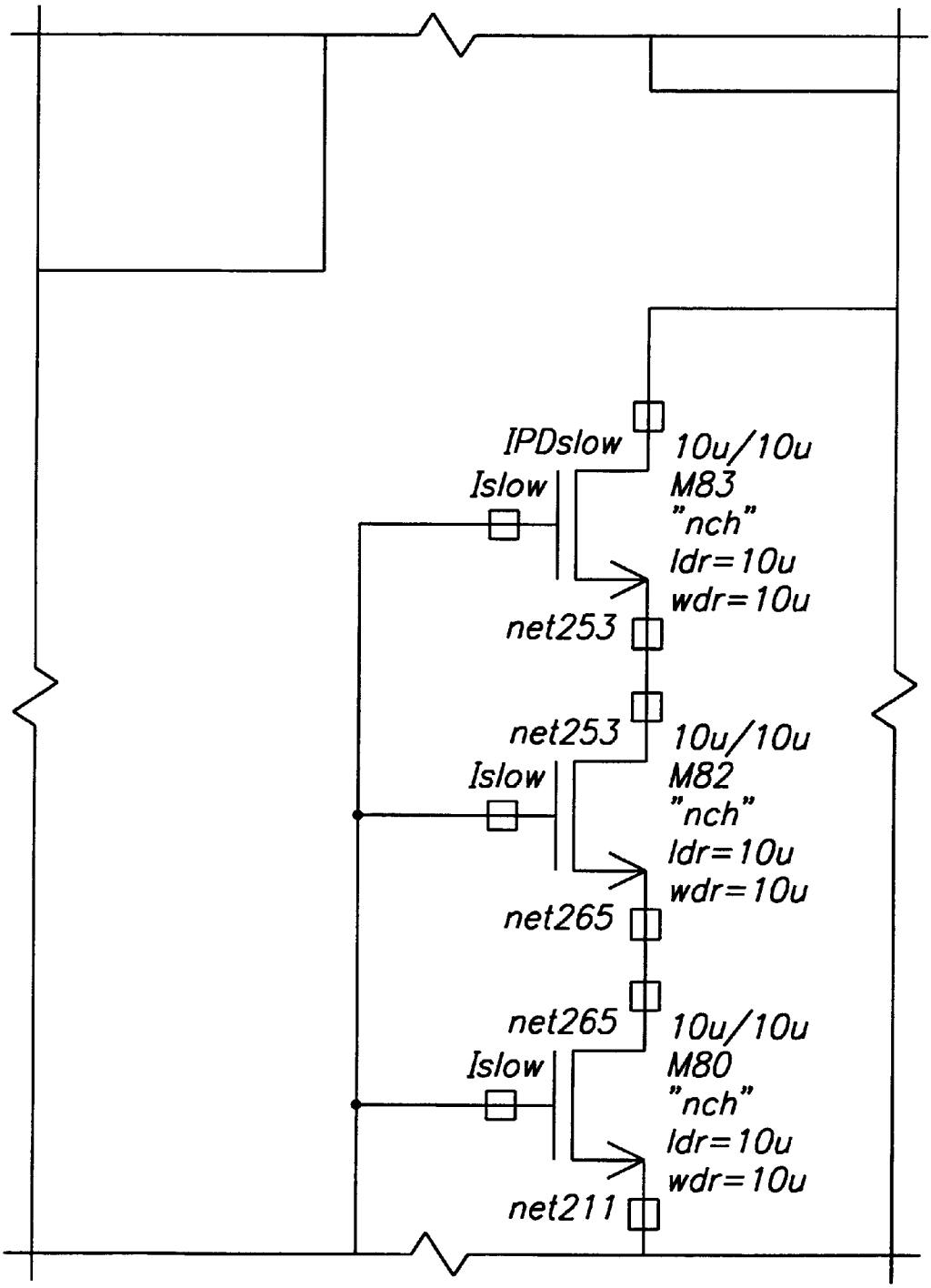


Fig 8,050,405C



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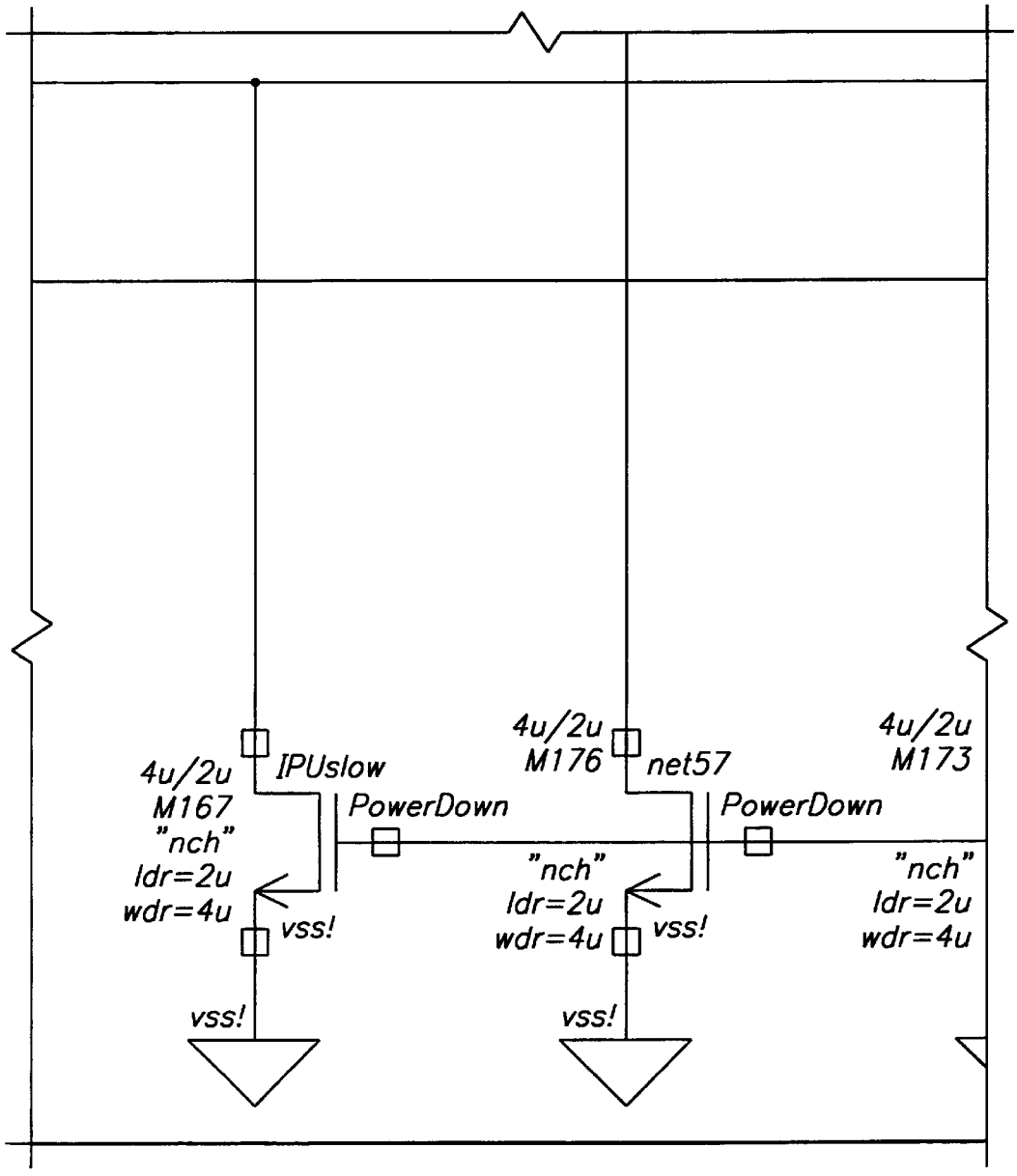

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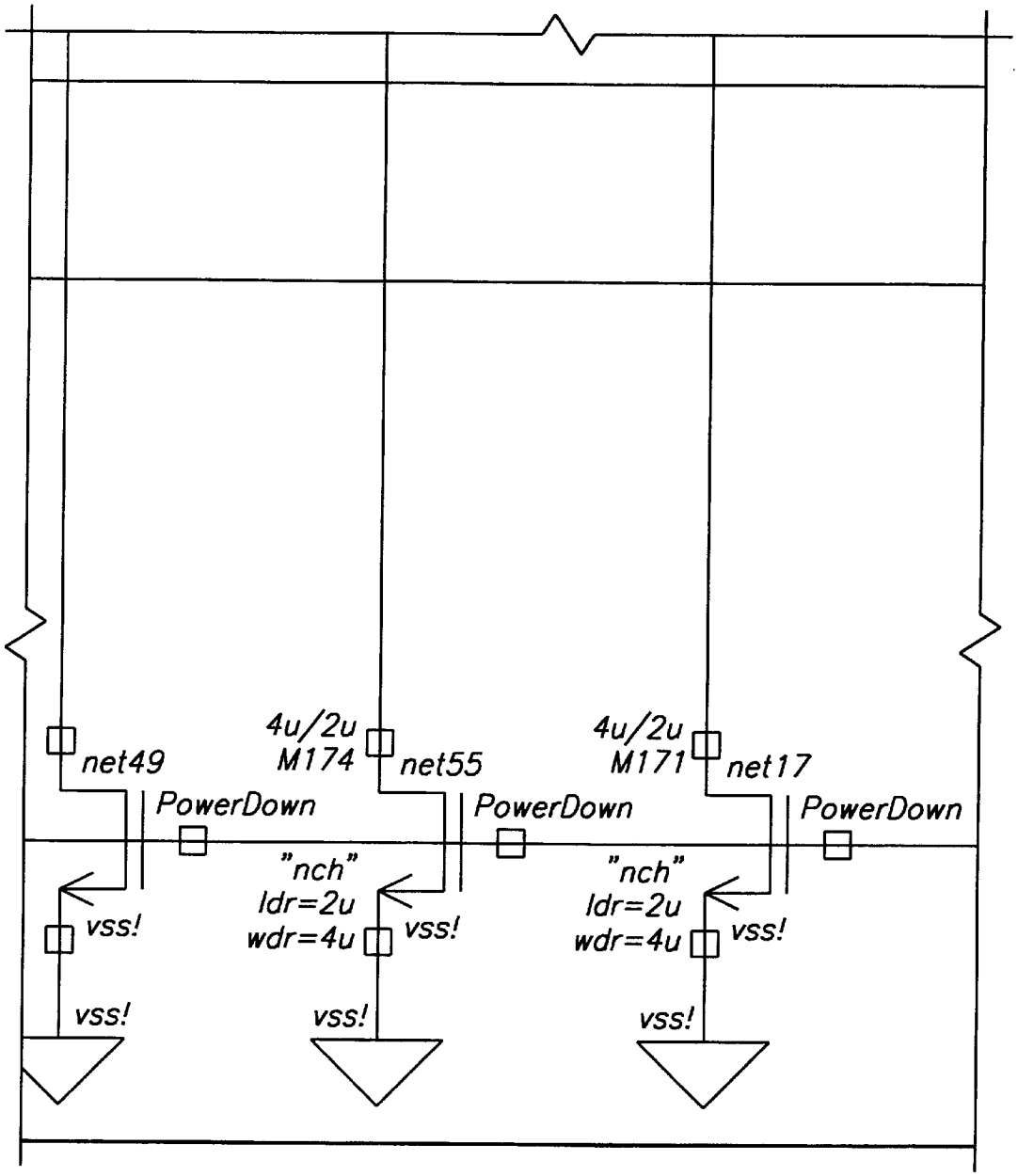

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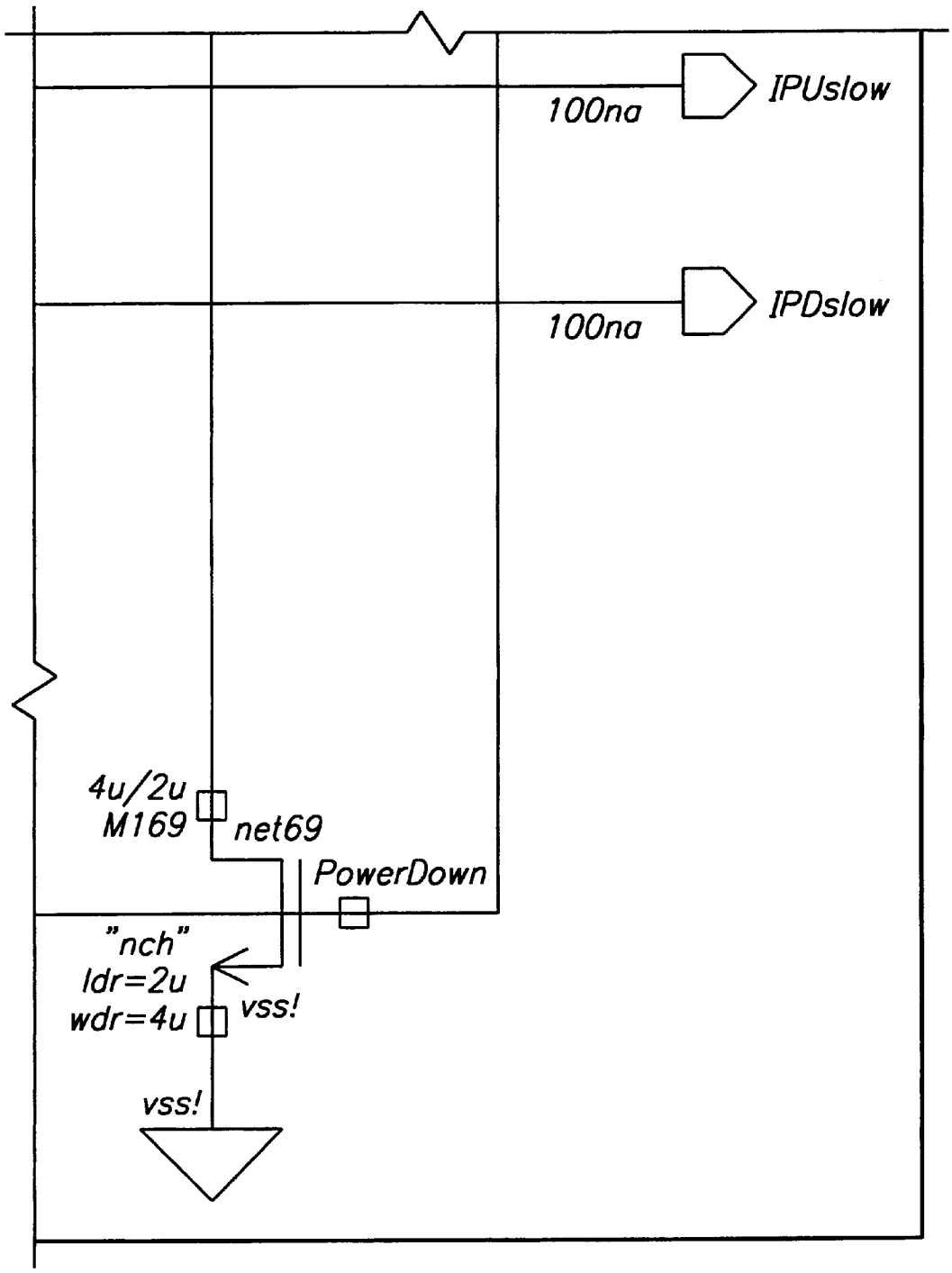

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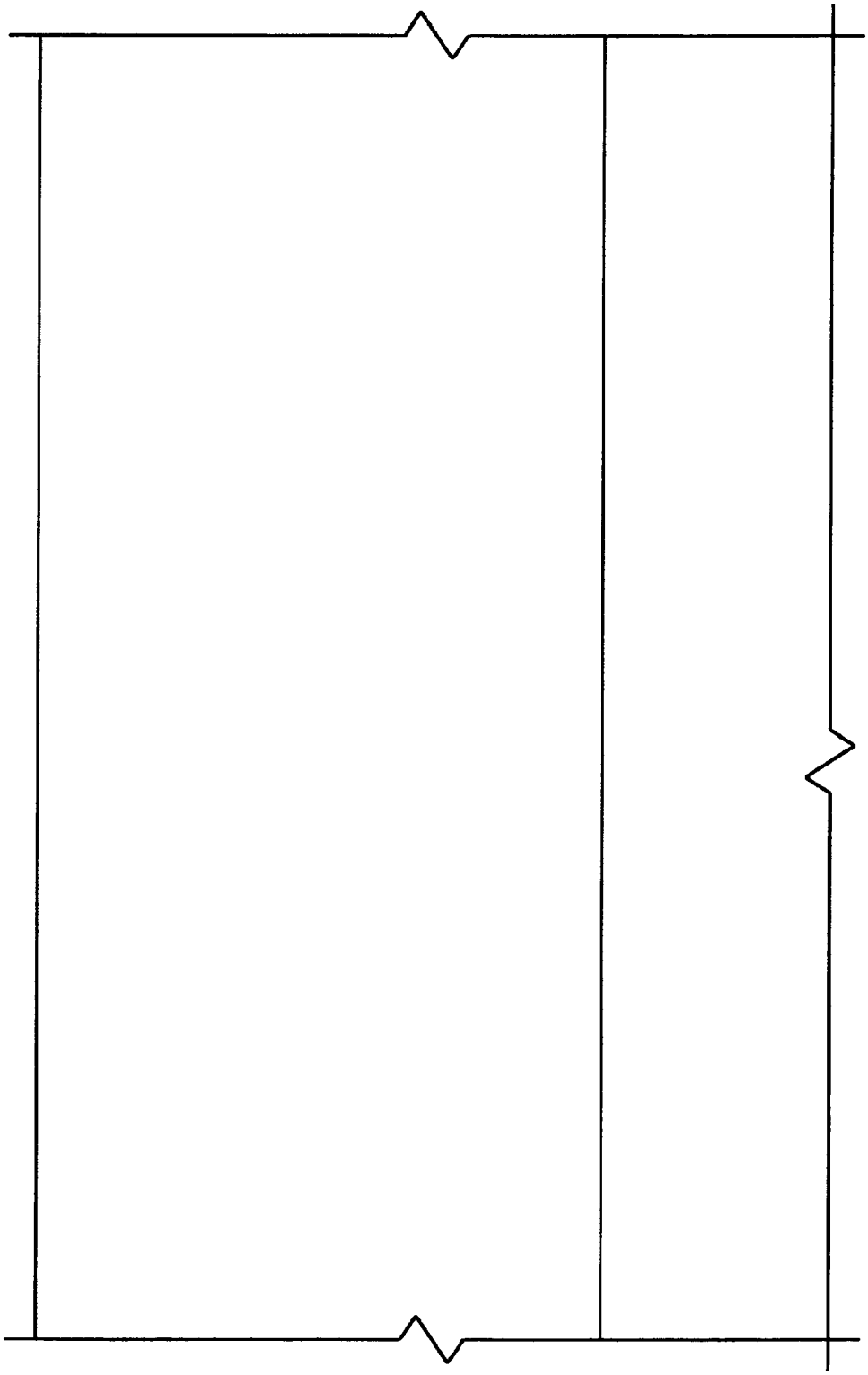

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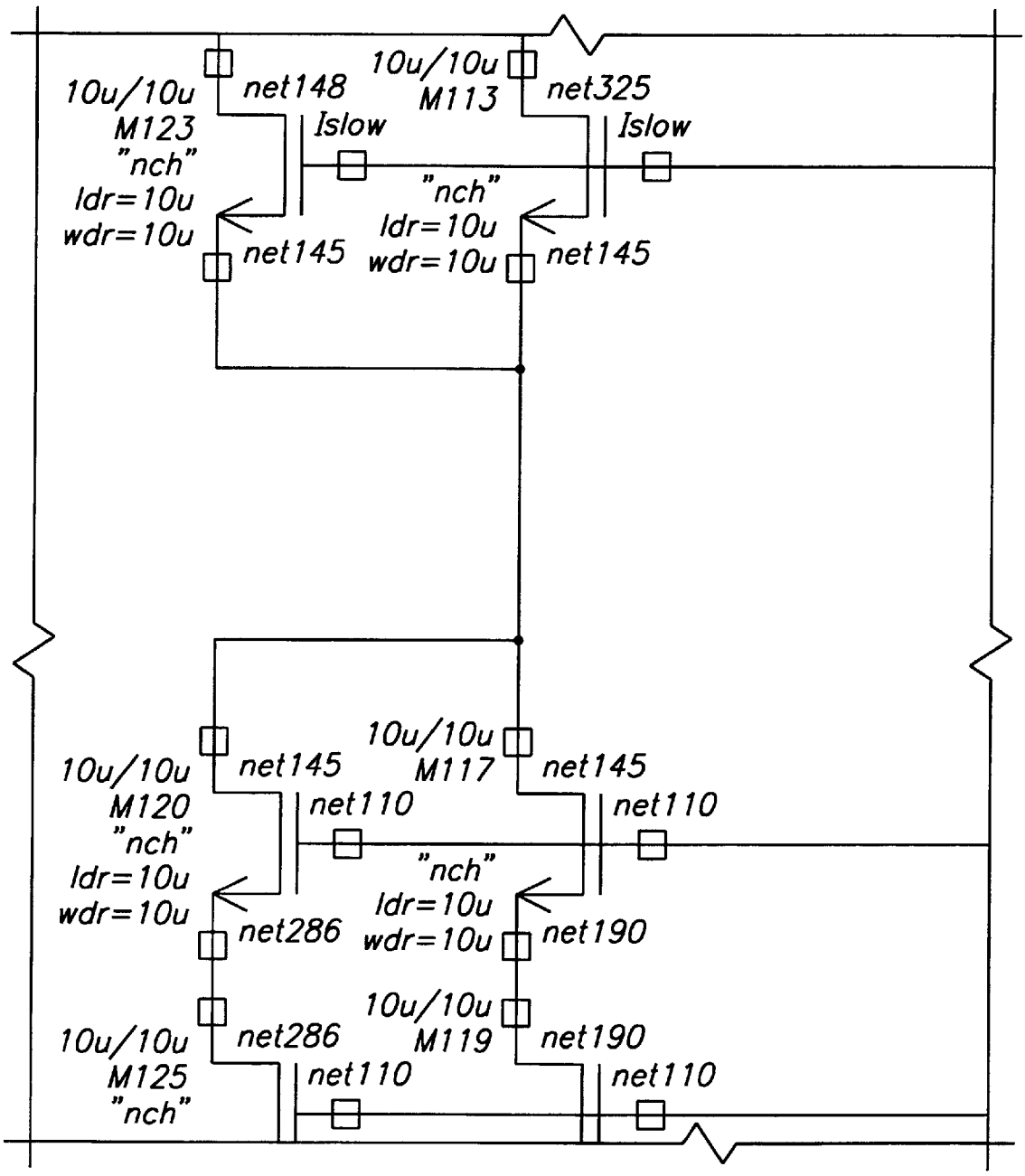

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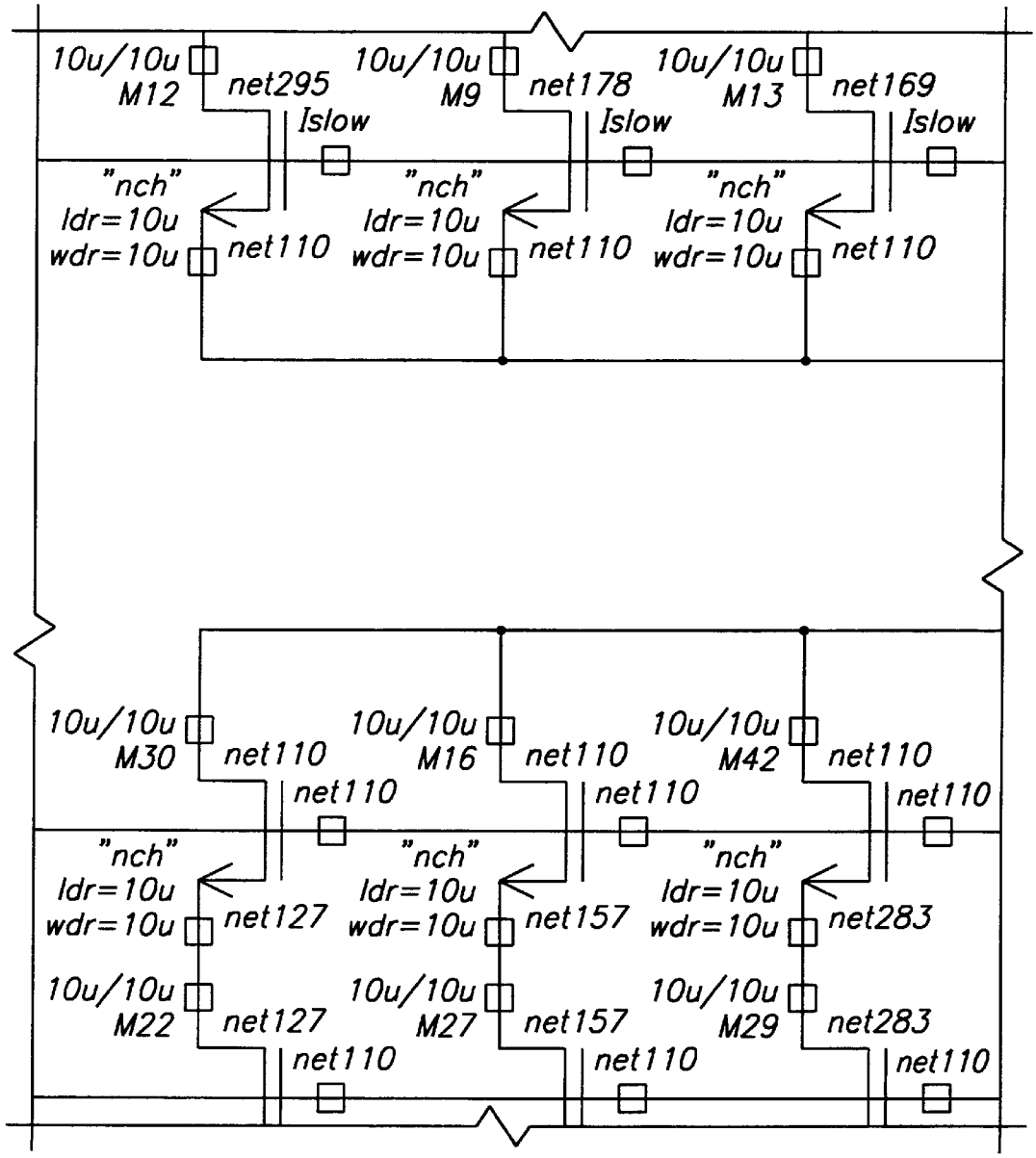

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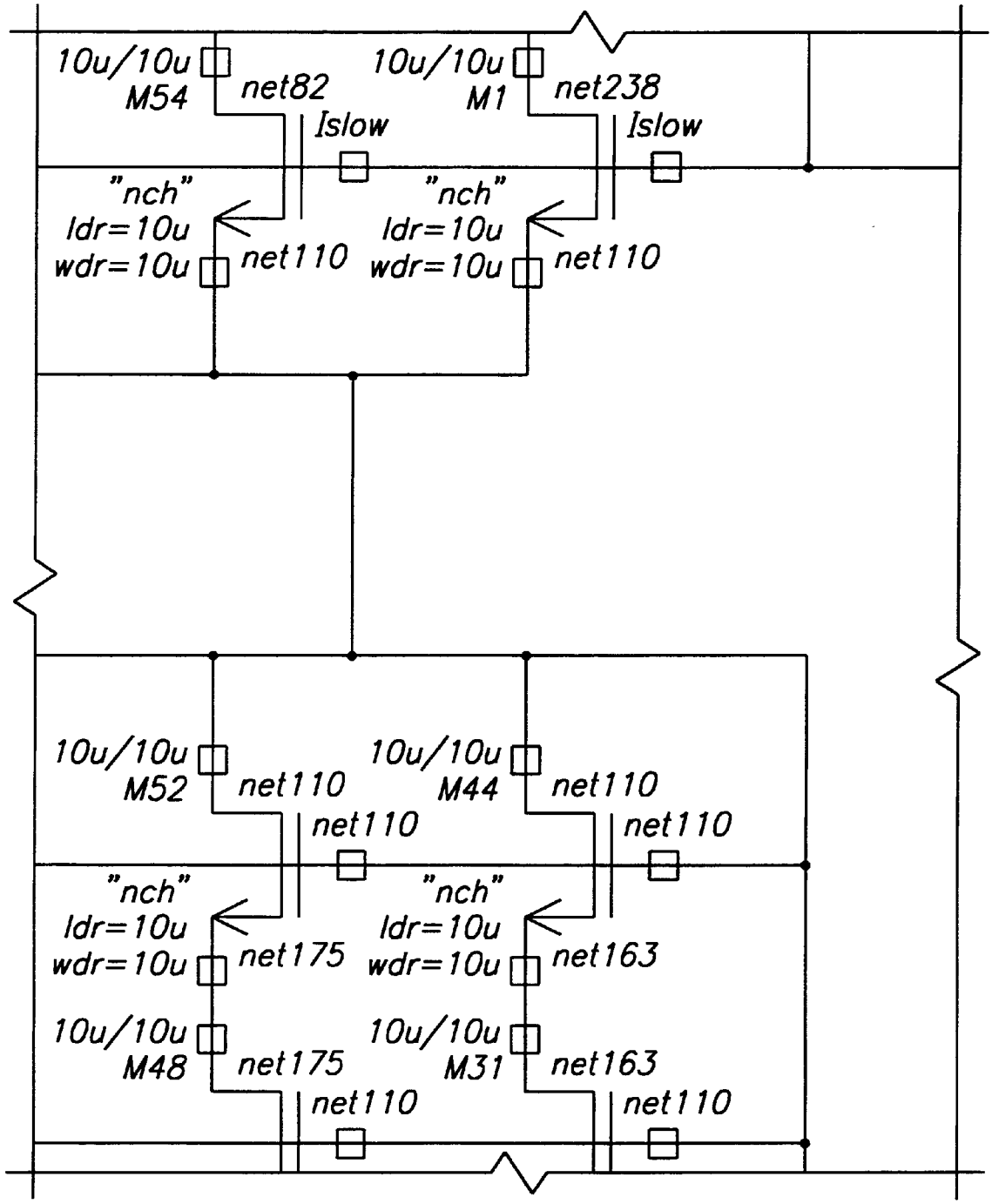

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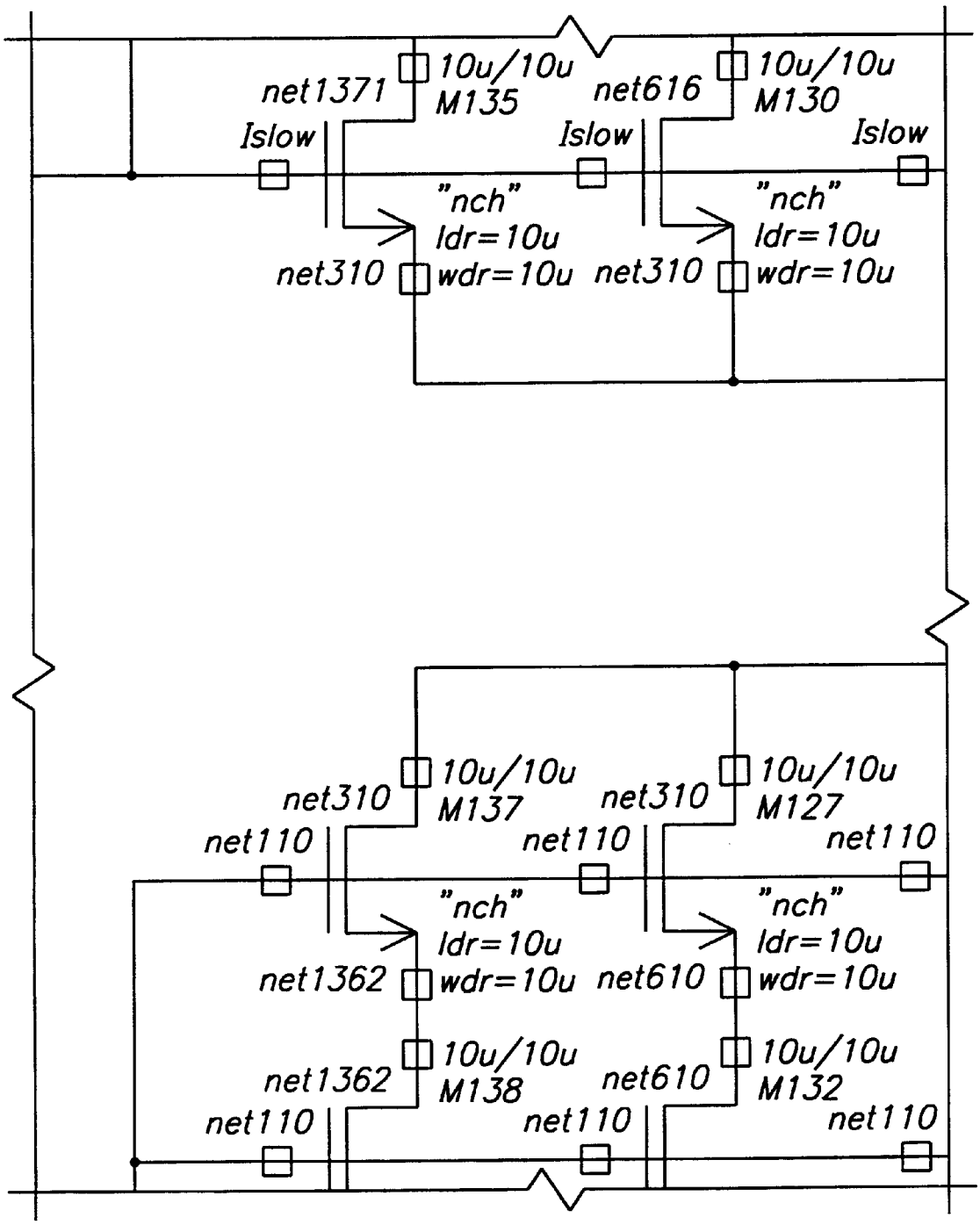

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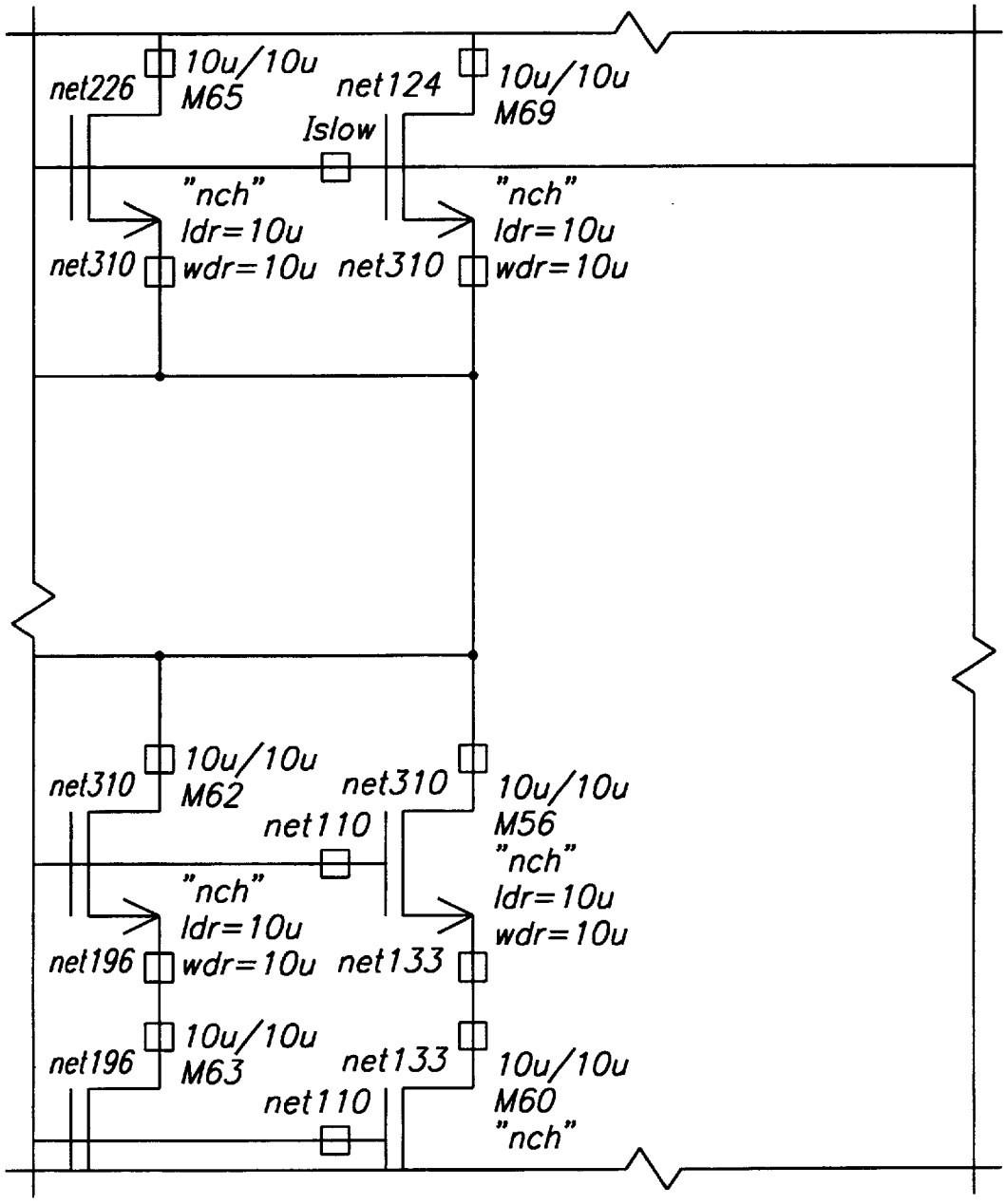

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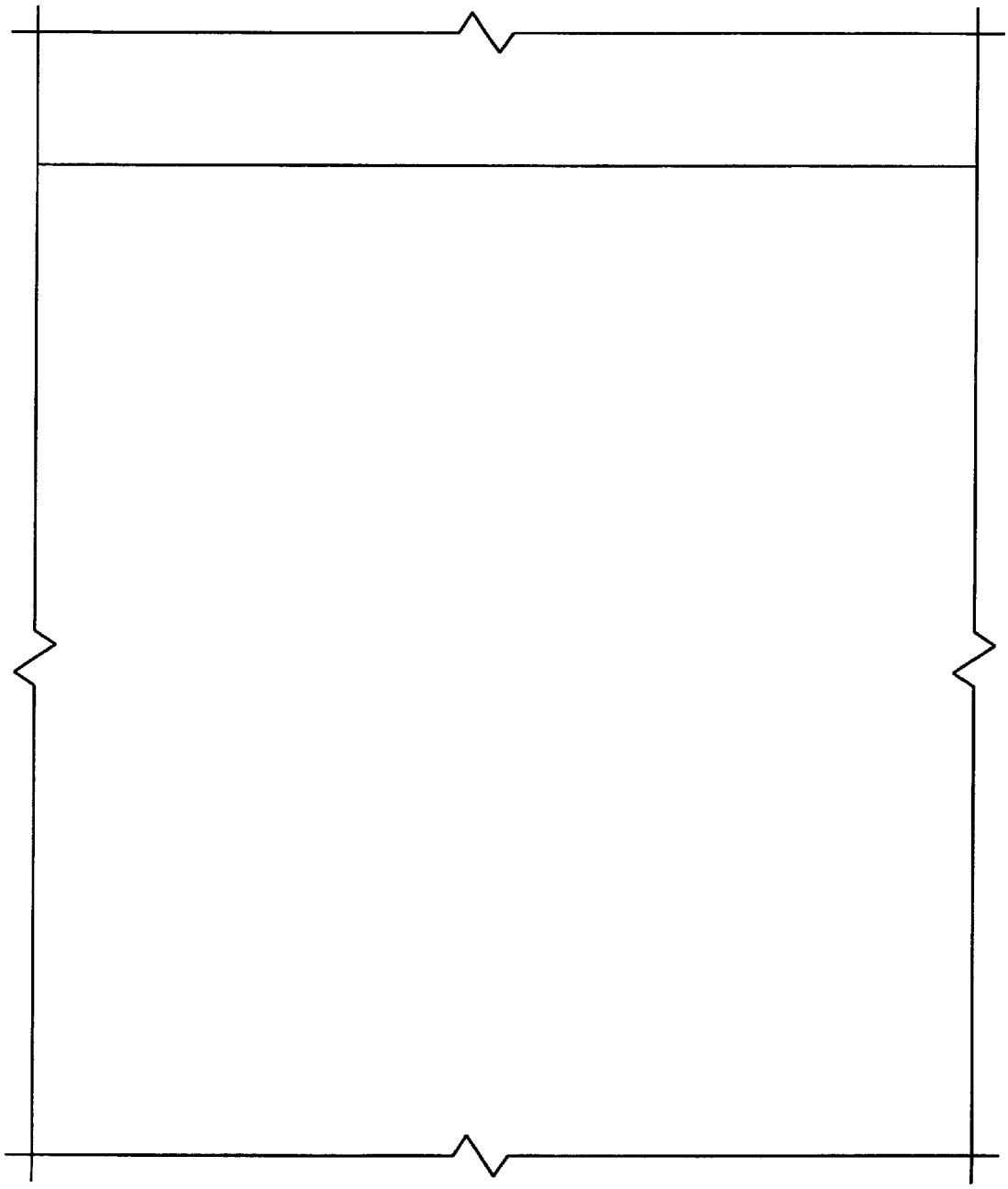

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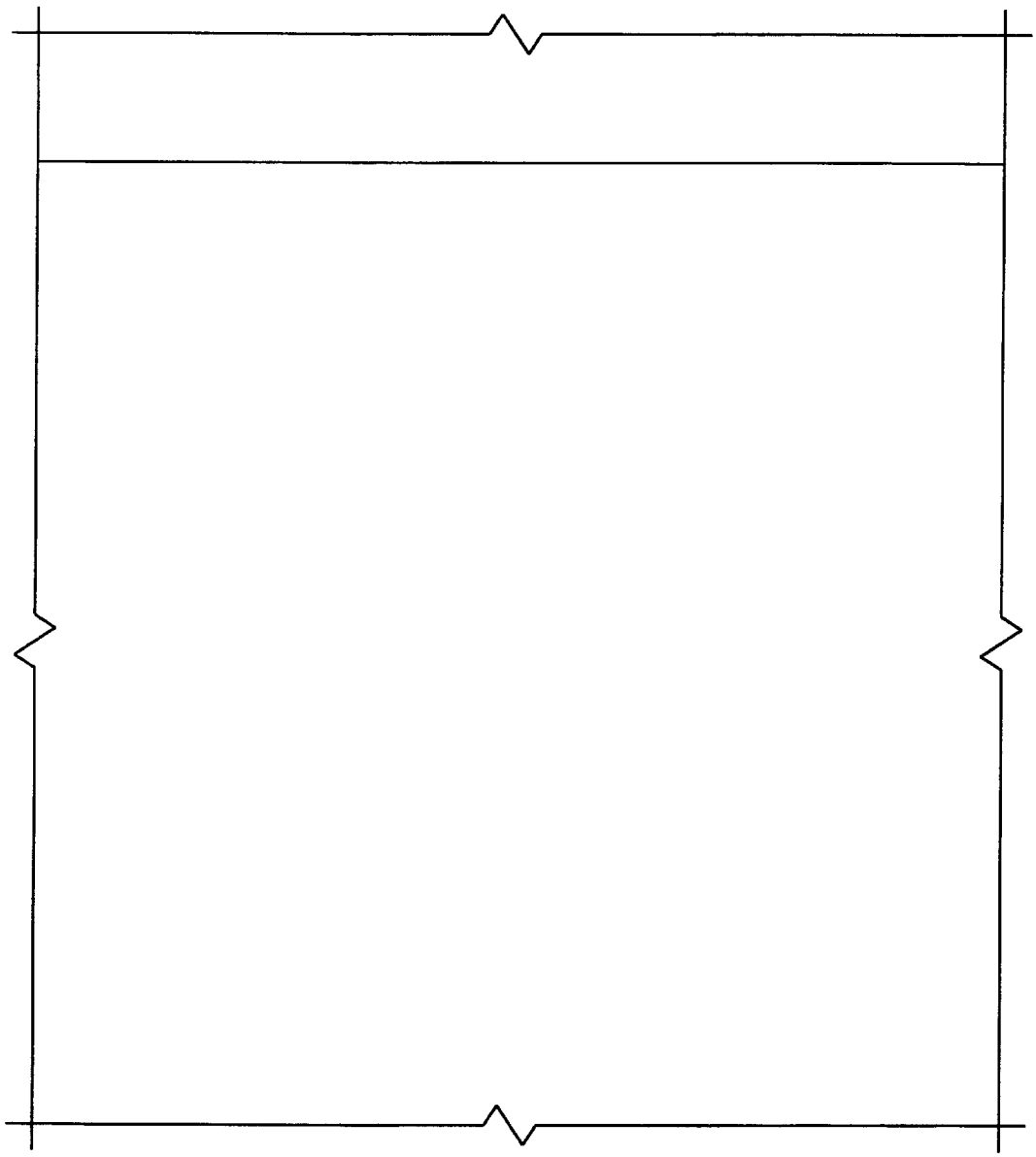

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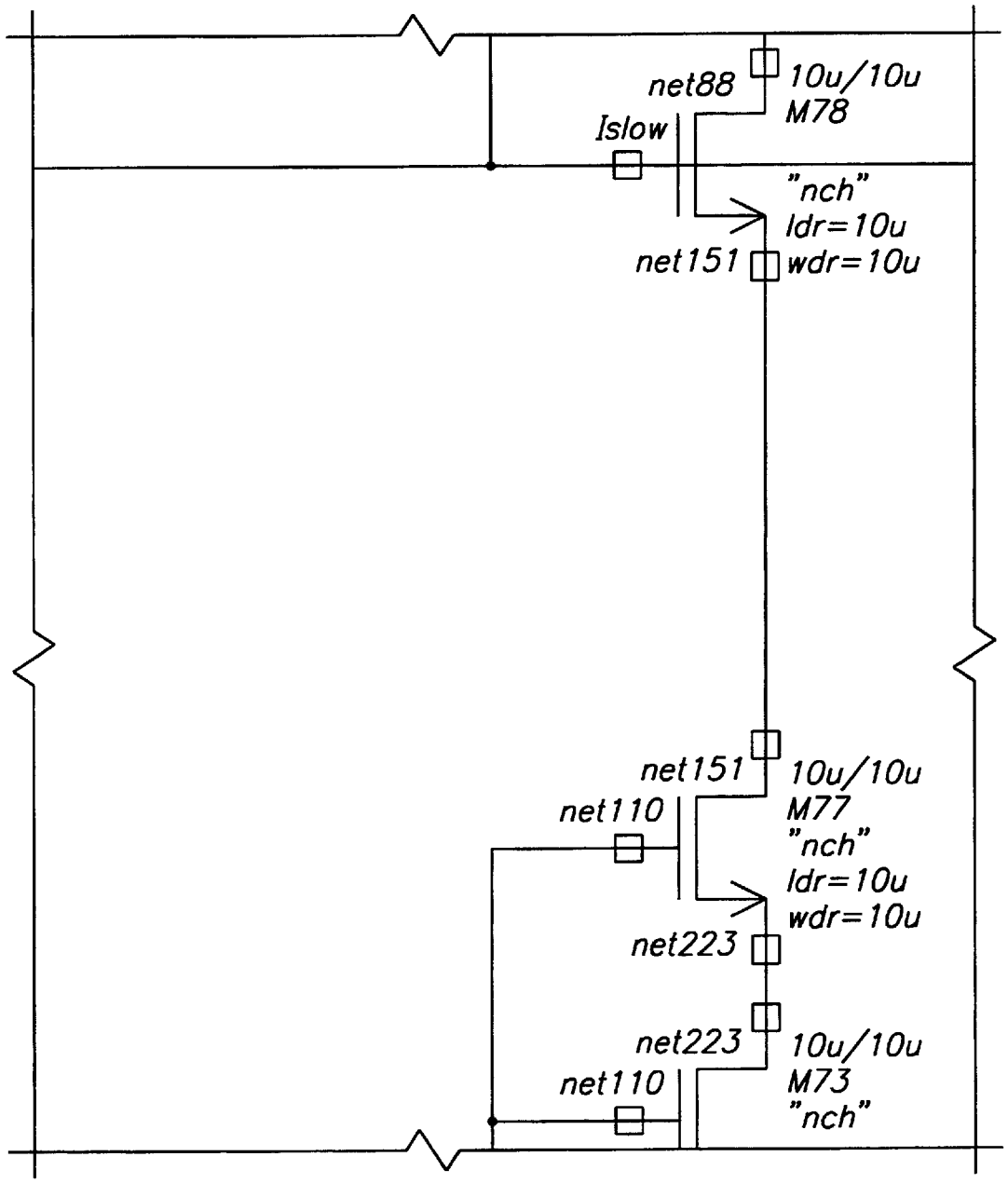
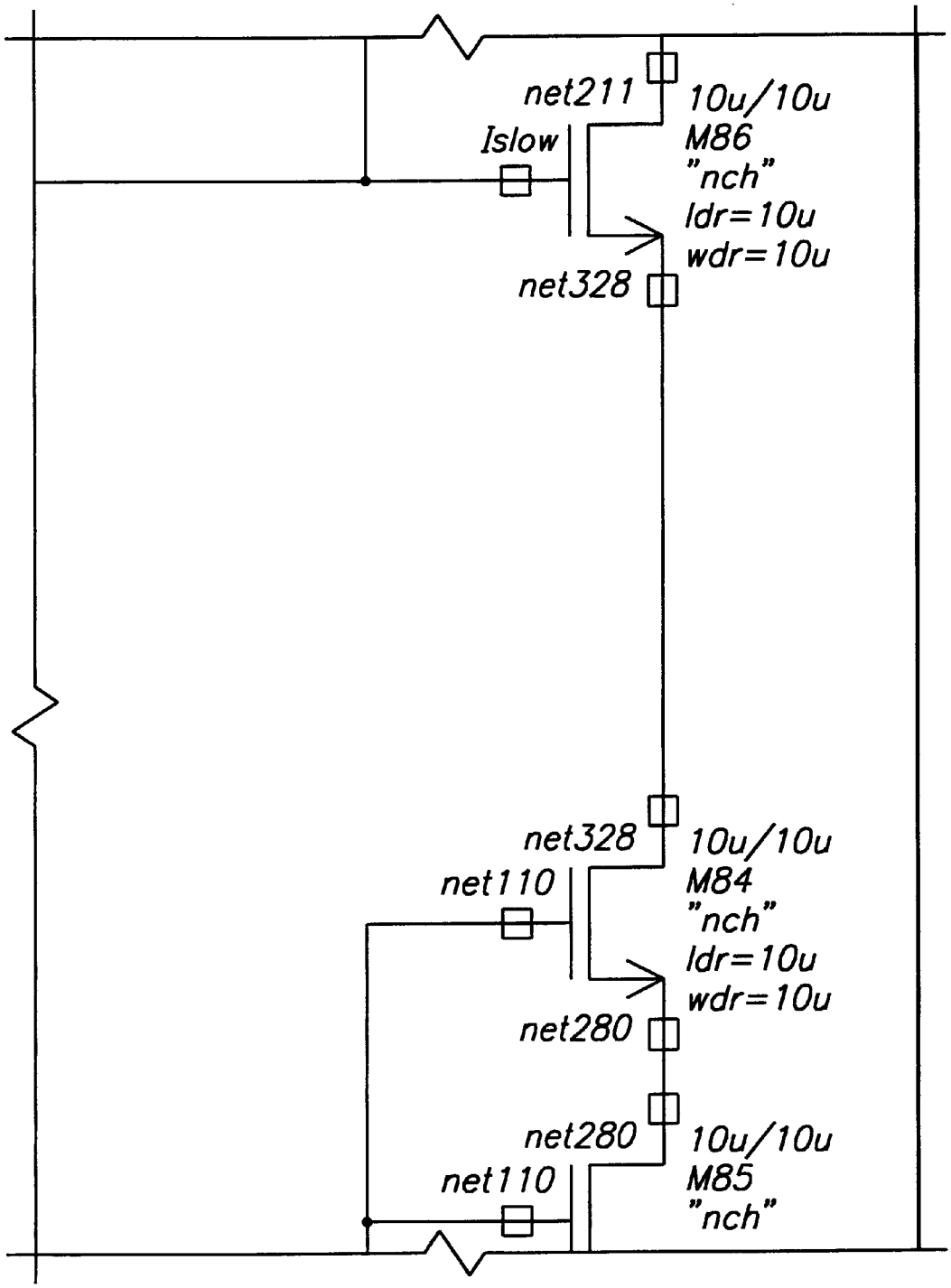


Fig 8,054,050,II



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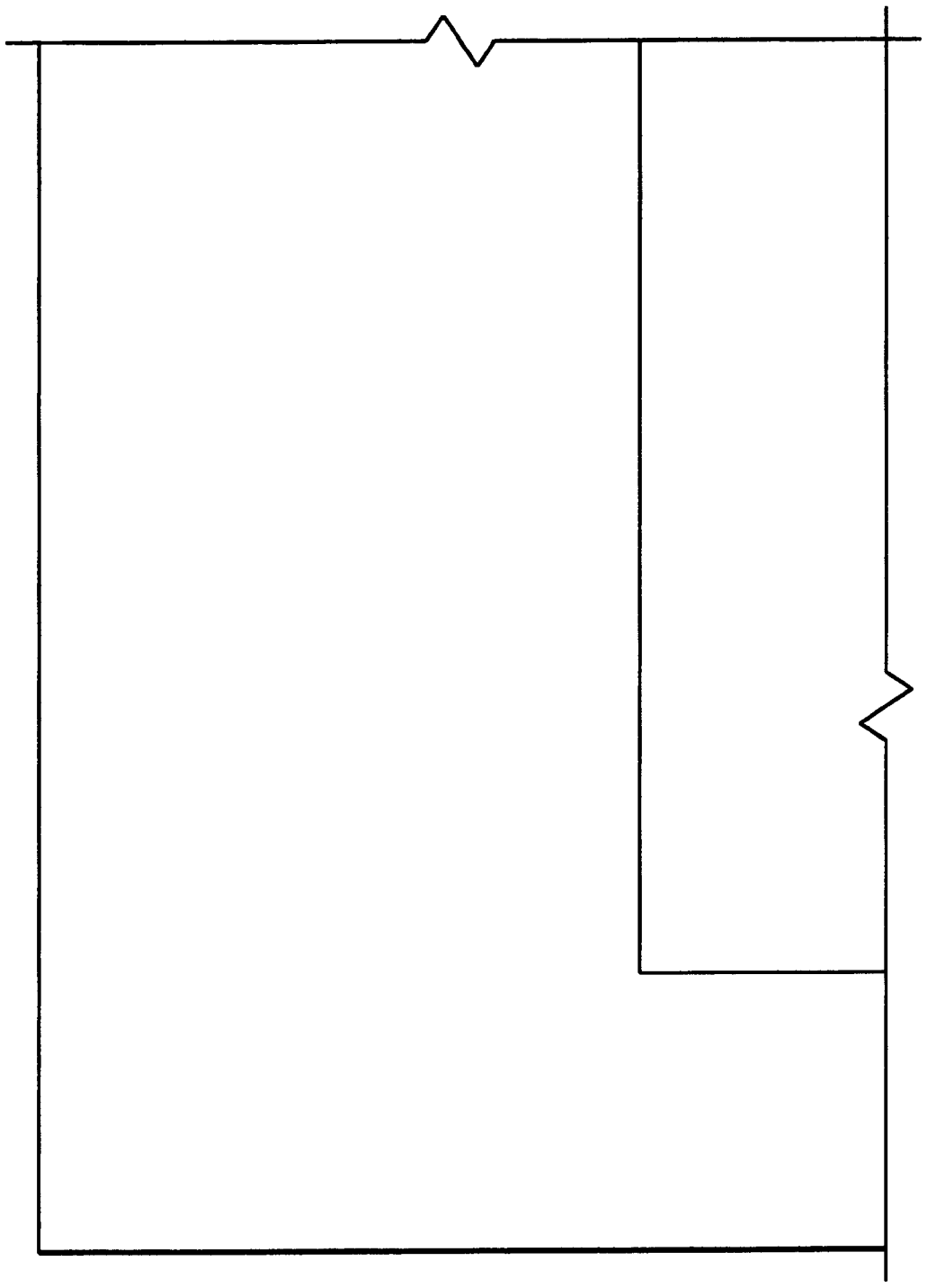

FIG 8.0504050EA

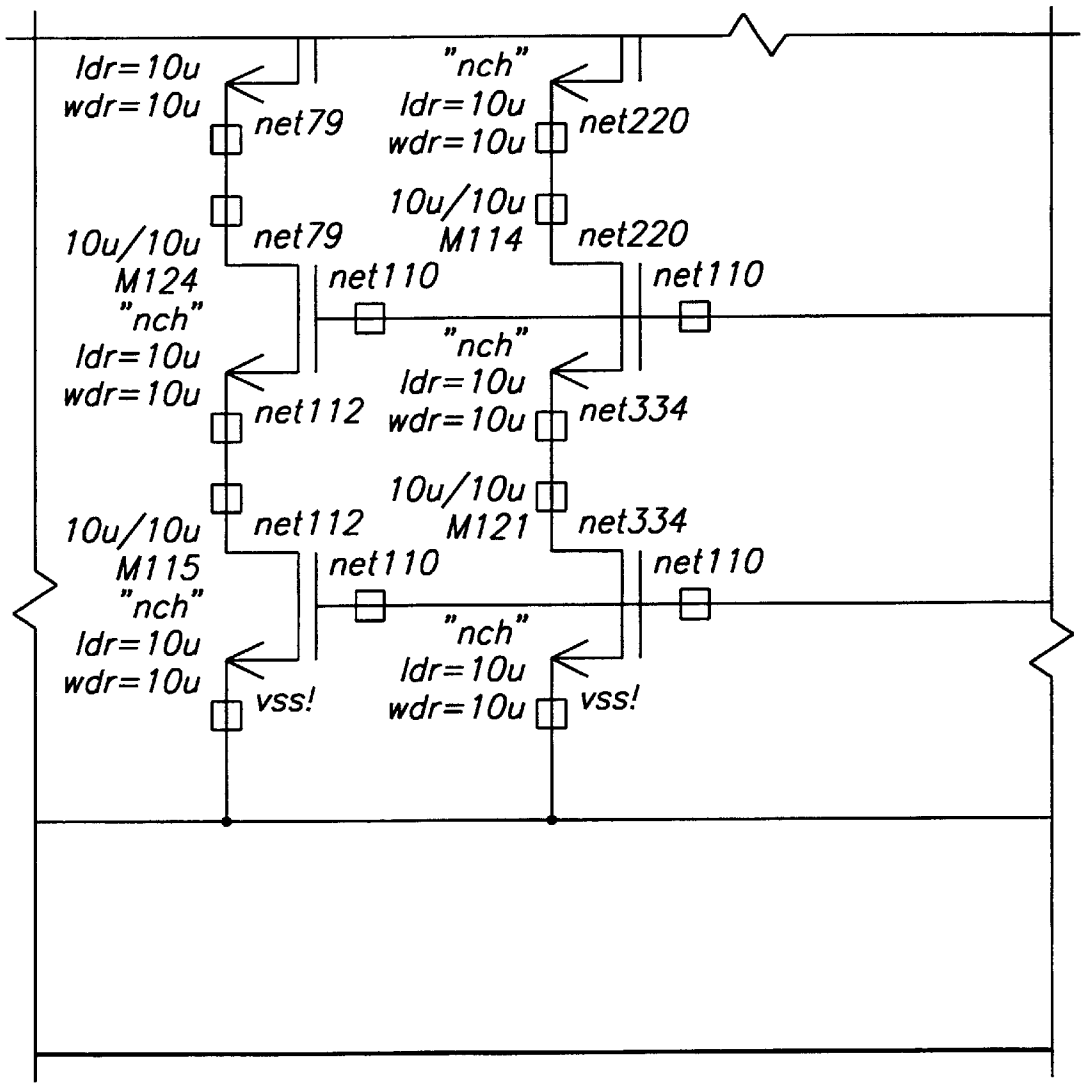
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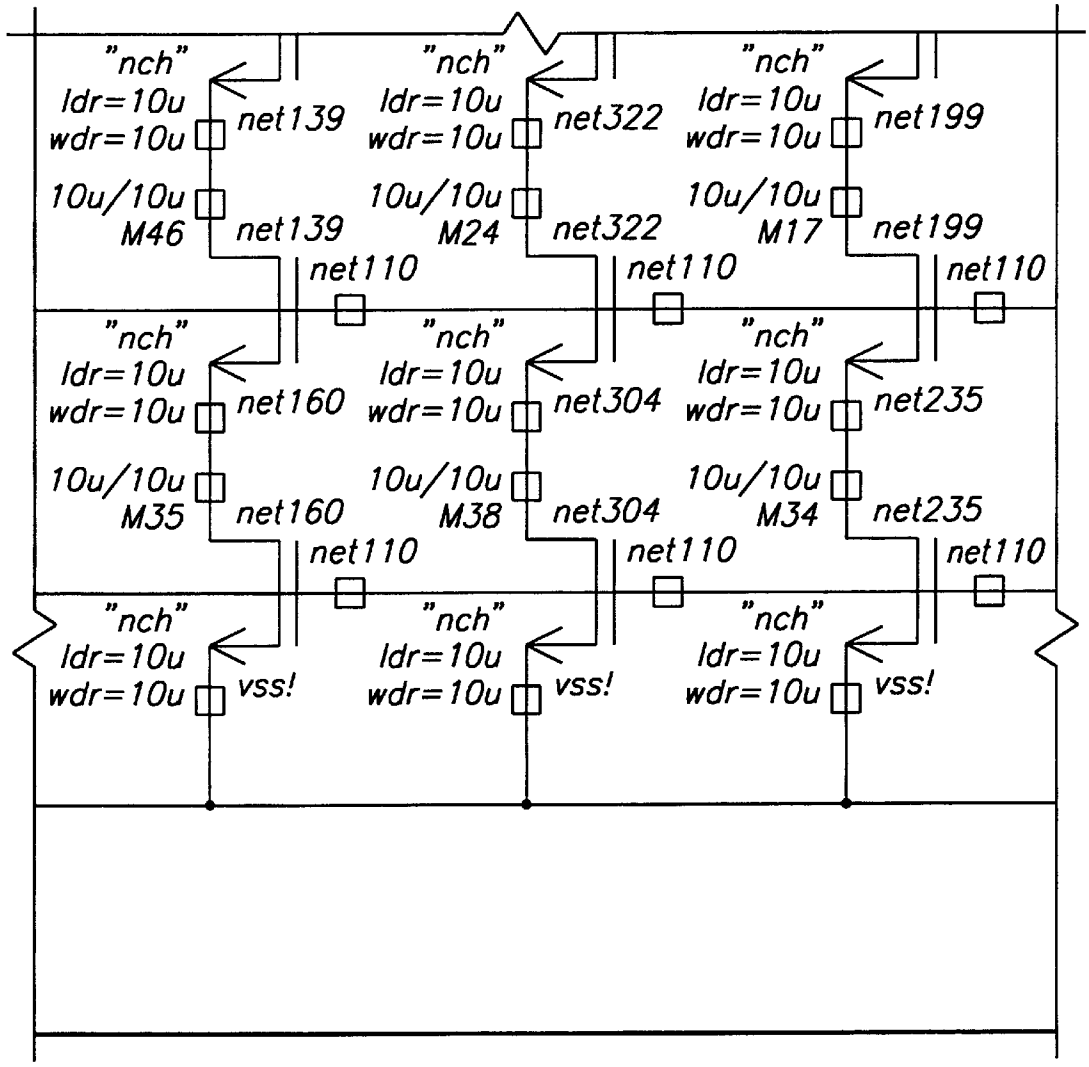
Fig 6,054,856



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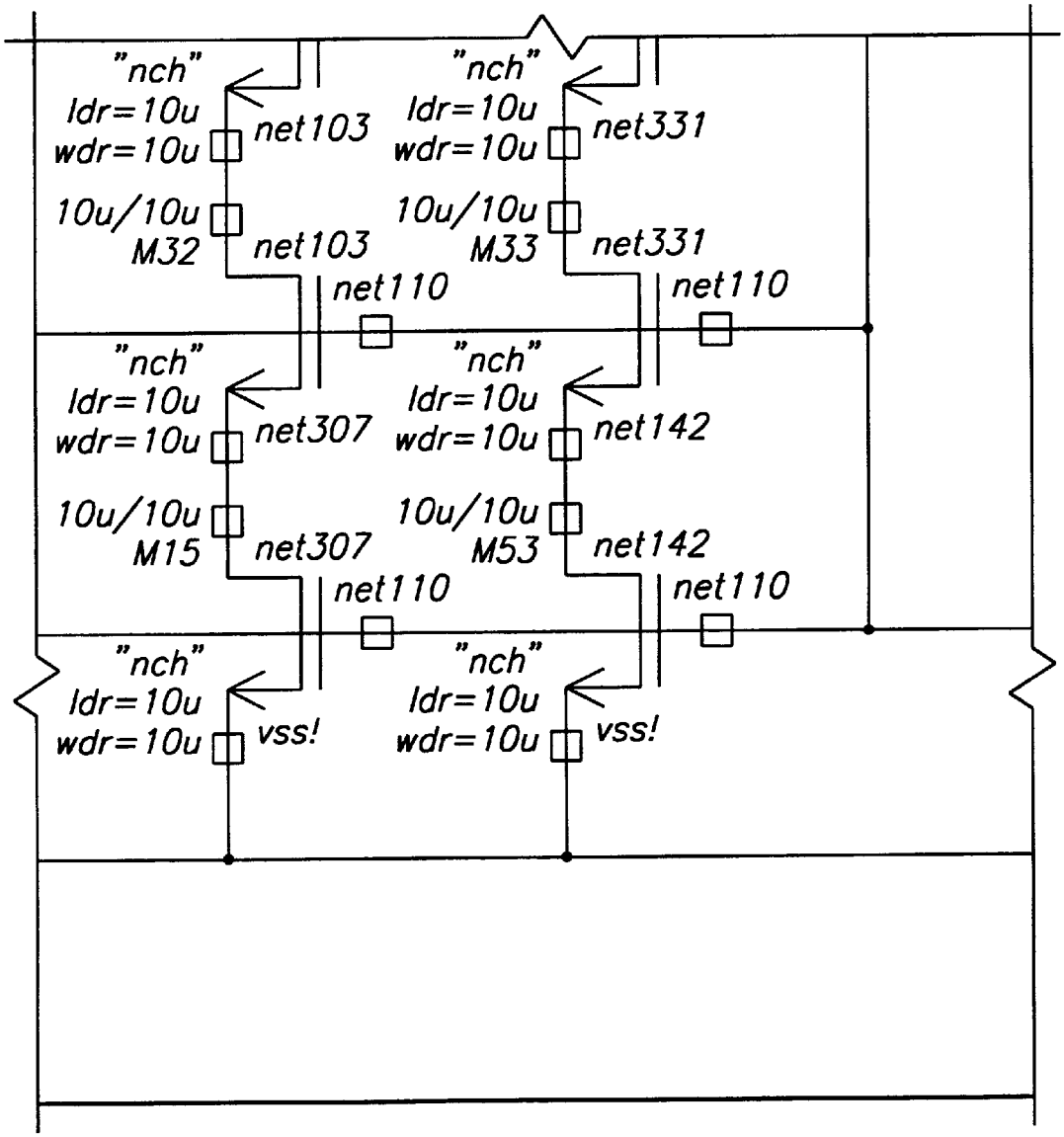

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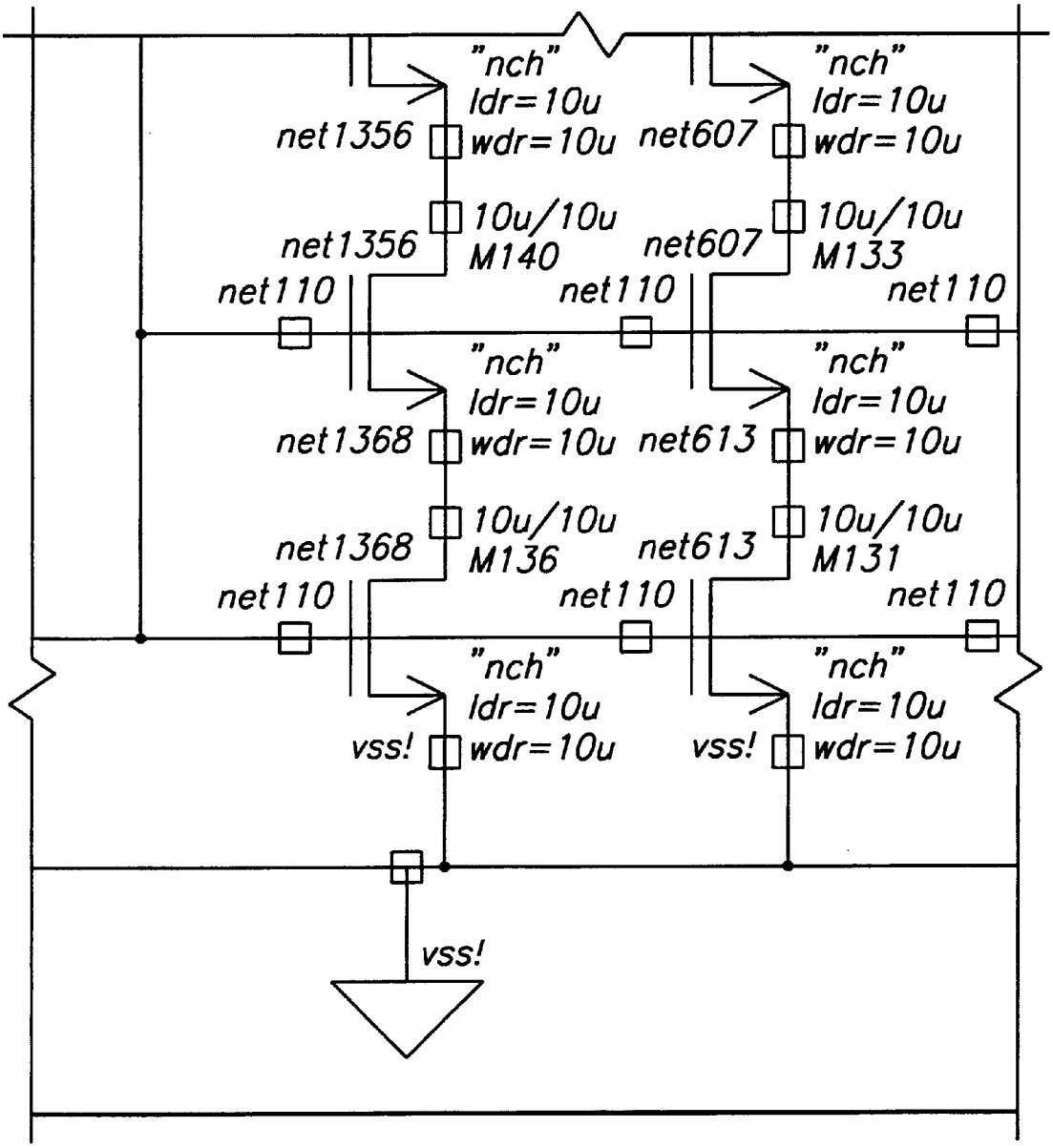

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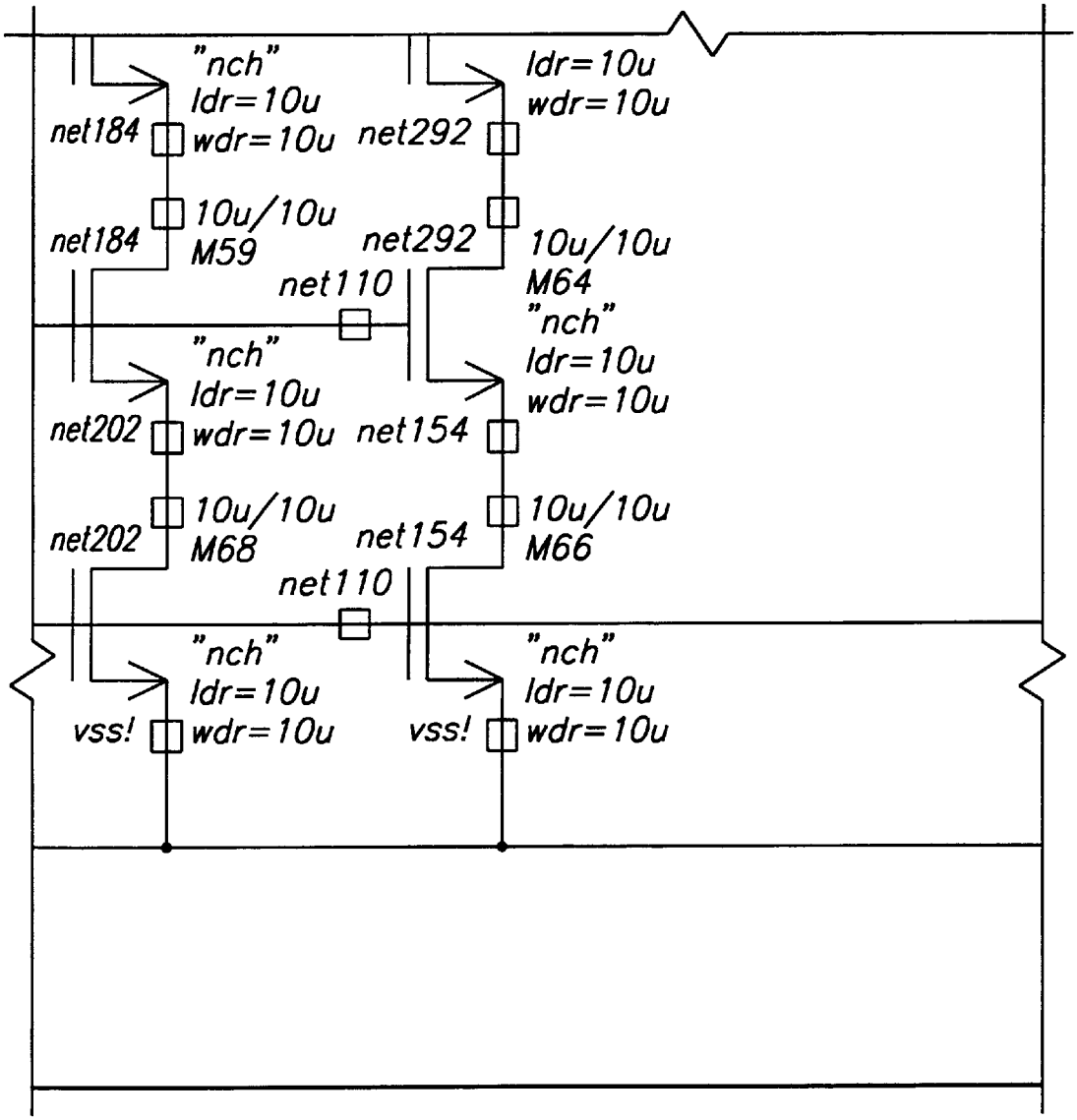

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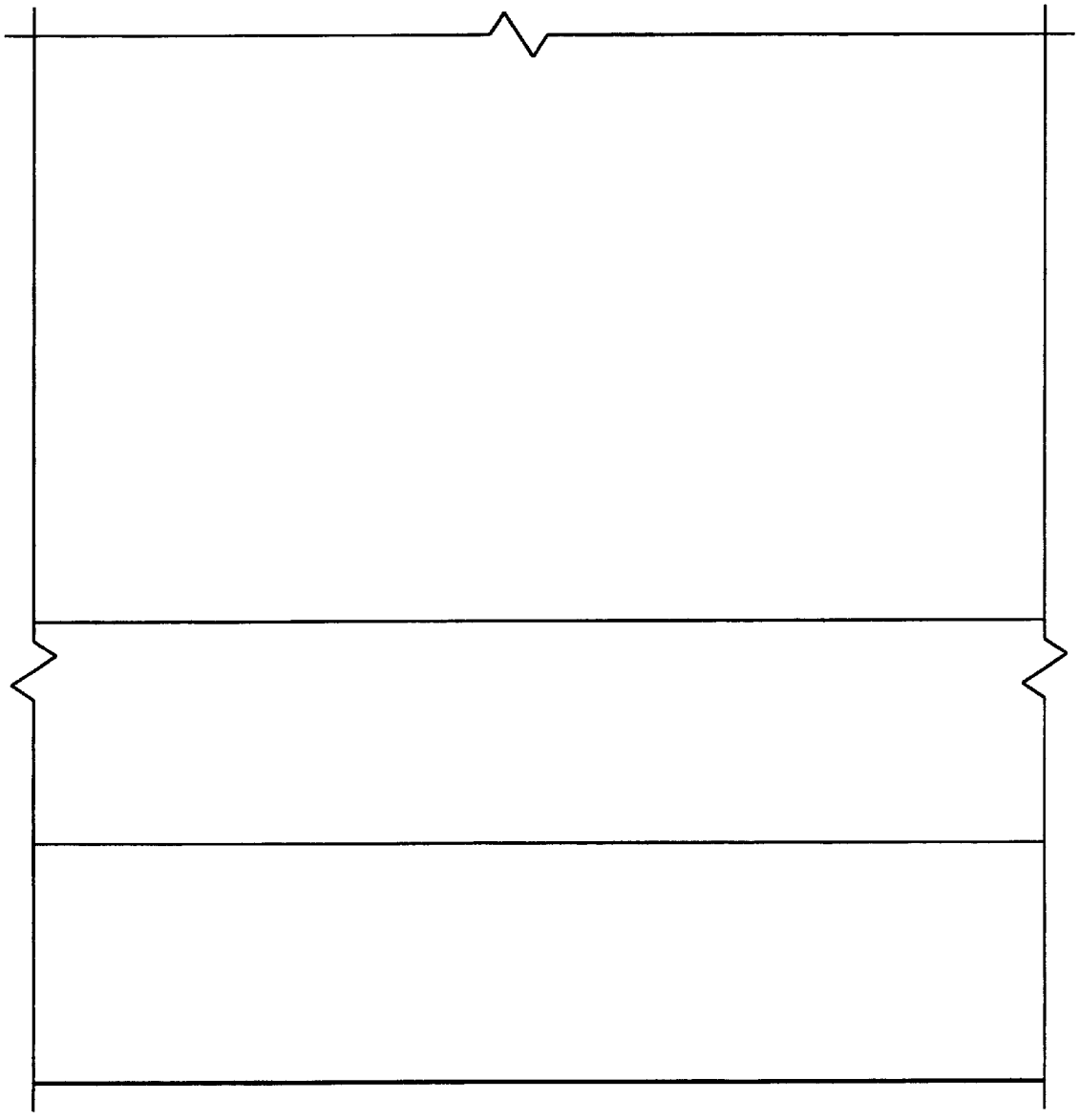
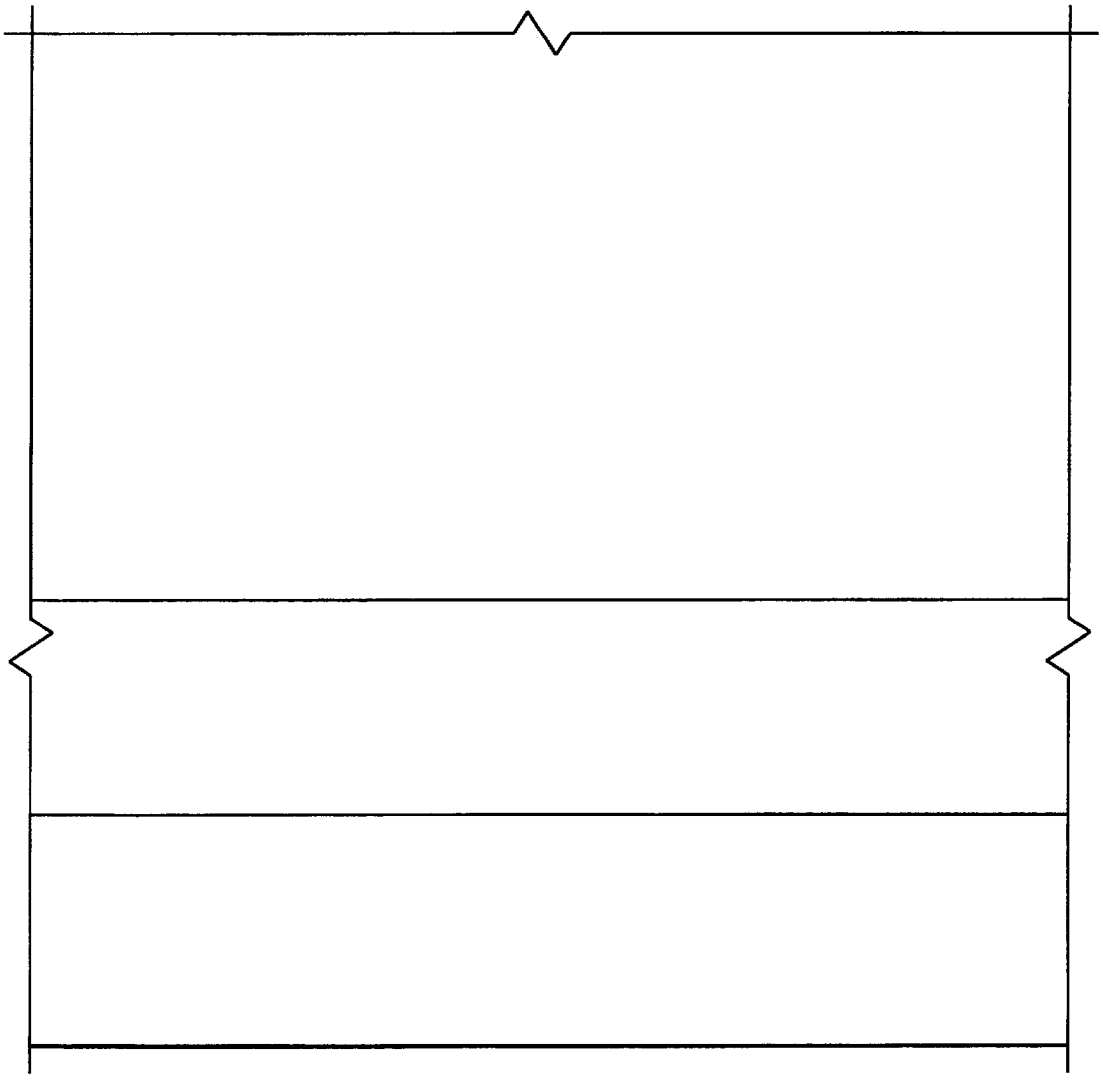


Fig 88.0504056



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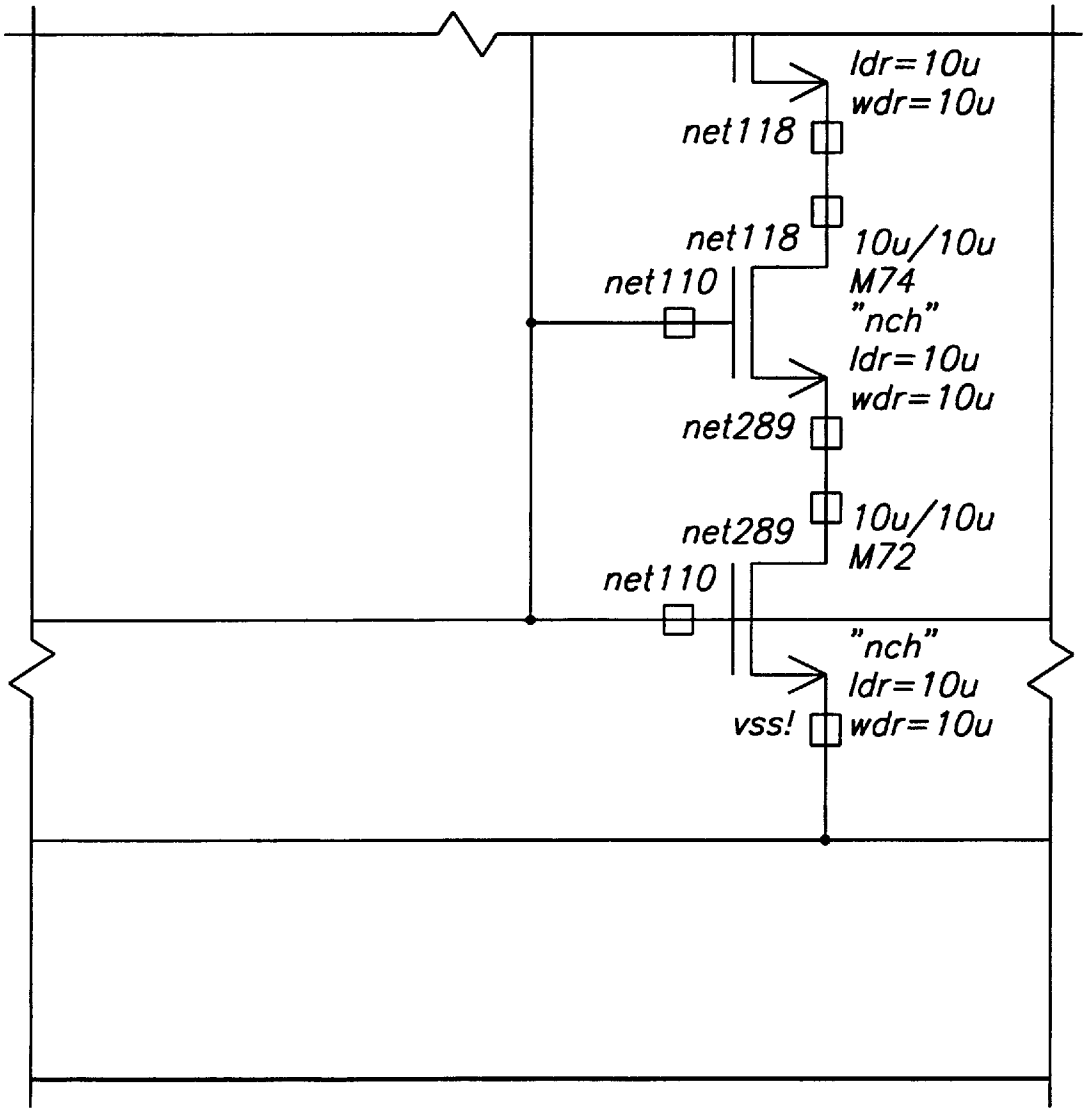

Fig 8,050,405E

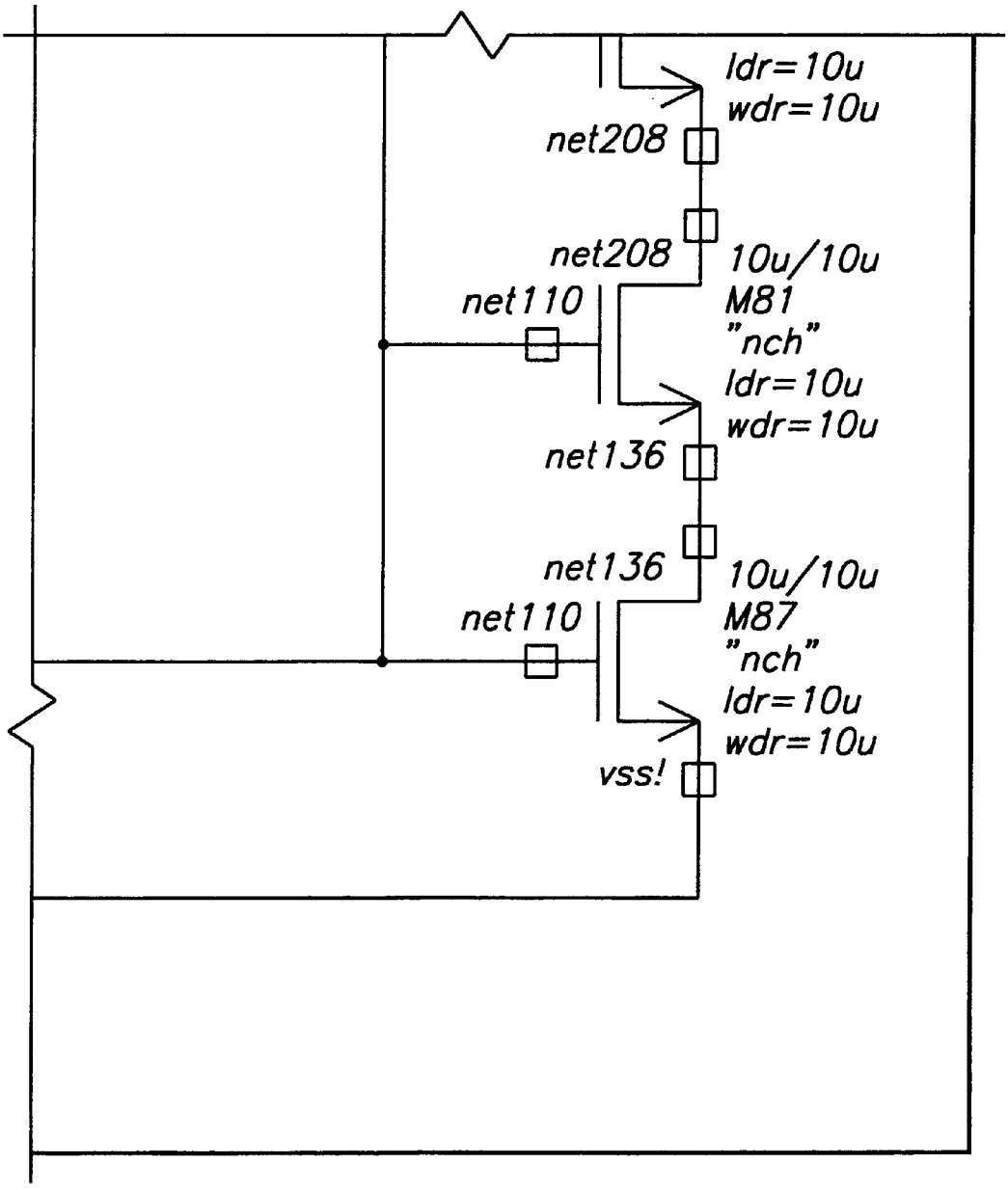

Fig 88,050,405E,1

8.0505A	8.0505AB	8.0505AC	8.0505AD	8.0505AE	8.0505AF	8.0505AG	8.0505AH	8.0505AI	8.0505AJ	8.0505AK	8.0505AL	8.0505AM	8.0505AN
8.0505BA	8.0505BB	8.0505BC	8.0505BD	8.0505BE	8.0505BF	8.0505BG	8.0505BH	8.0505BI	8.0505BJ	8.0505BK	8.0505BL	8.0505BM	8.0505BN
8.0505CA	8.0505CB	8.0505CC	8.0505CD	8.0505CE	8.0505CF	8.0505CG	8.0505CH	8.0505CI	8.0505CJ	8.0505CK	8.0505CL	8.0505CM	8.0505CN
8.0505DA	8.0505DB	8.0505DC	8.0505DD	8.0505DE	8.0505DF	8.0505DG	8.0505DH	8.0505DI	8.0505DJ	8.0505DK	8.0505DL	8.0505DM	8.0505DN
8.0505EA	8.0505EB	8.0505EC	8.0505ED	8.0505EE	8.0505EF								

FIG 8.0505

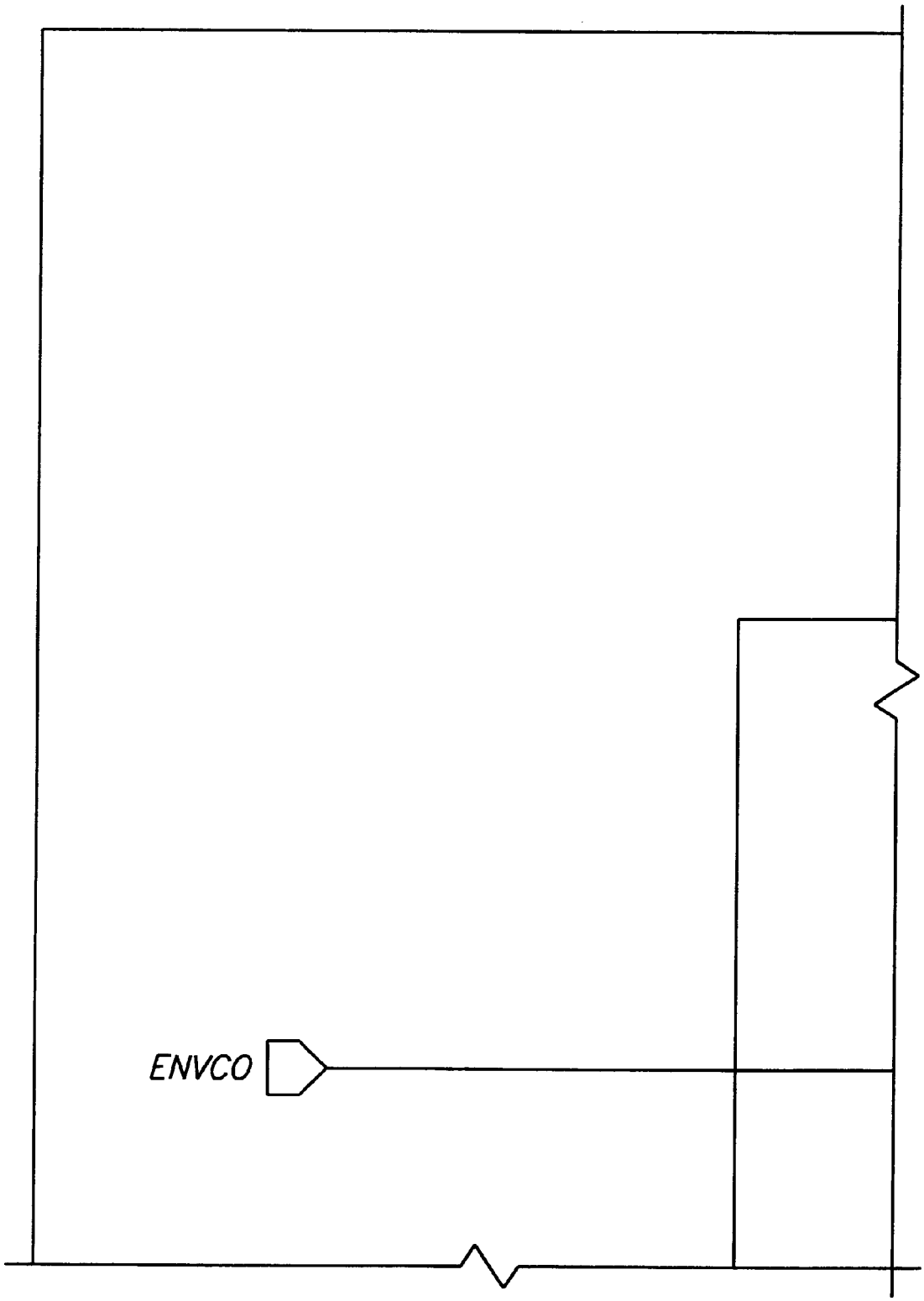

Fig 88.0505AA

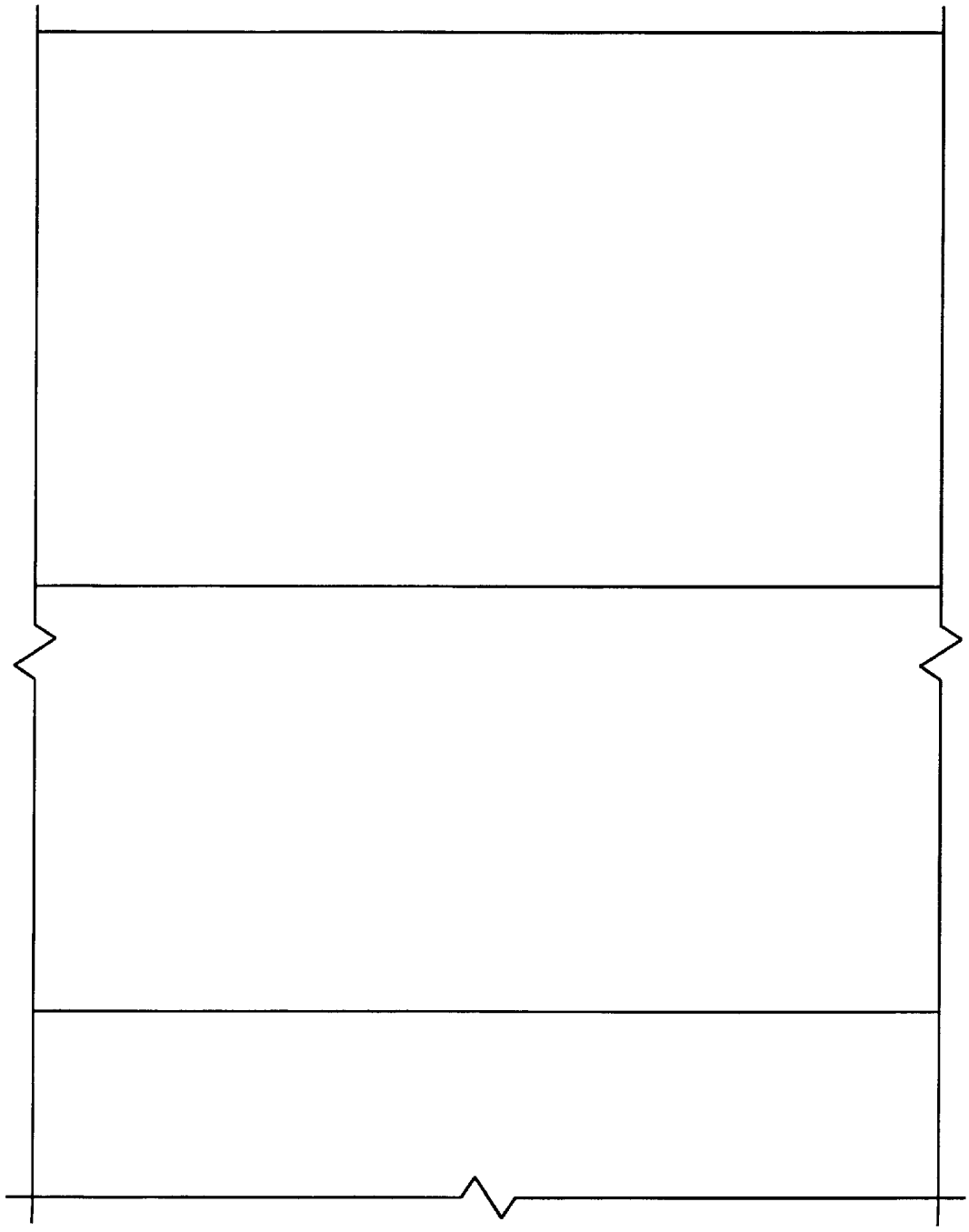

Fig 8.0505AB

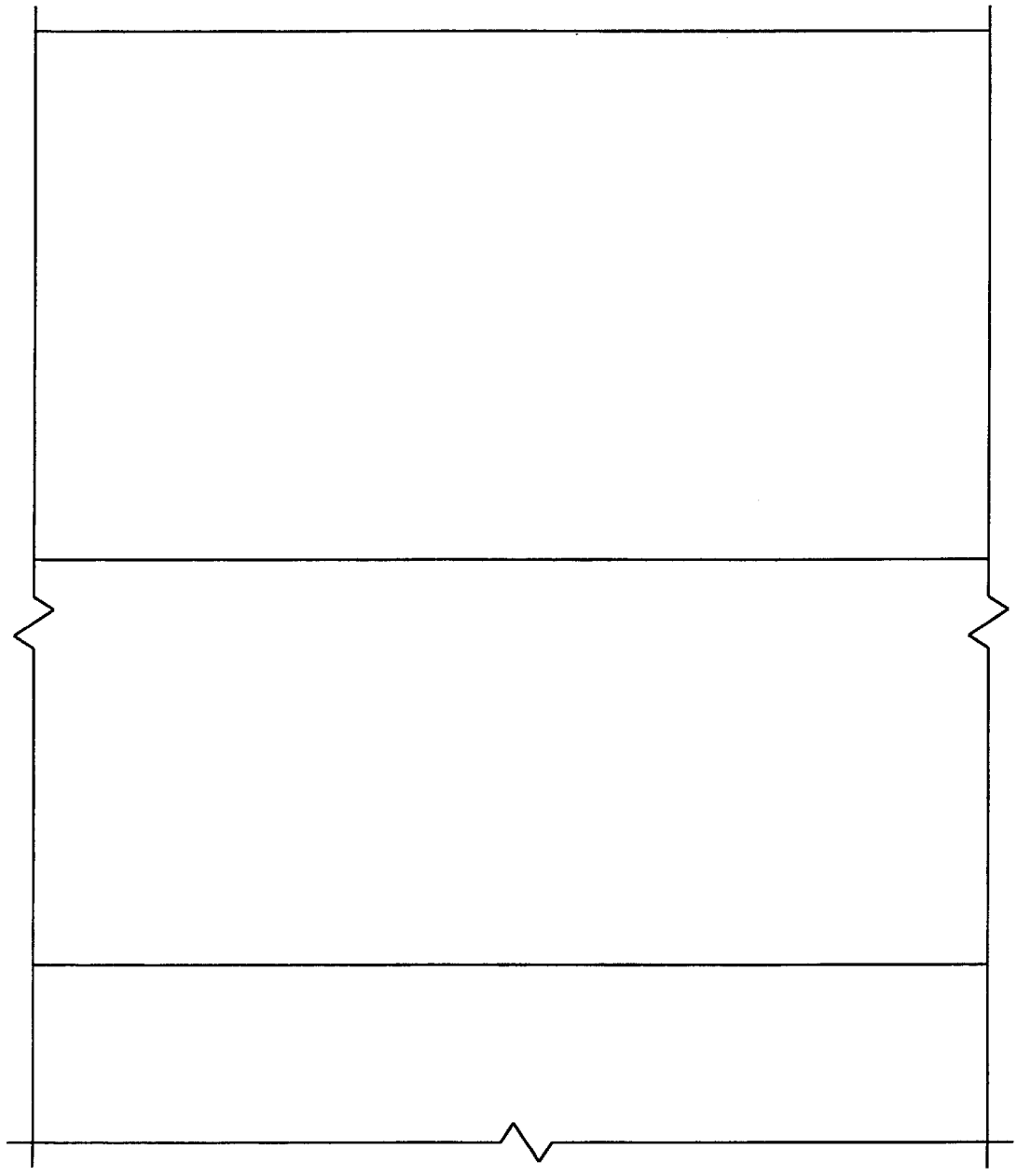

Fig 88.0505AC

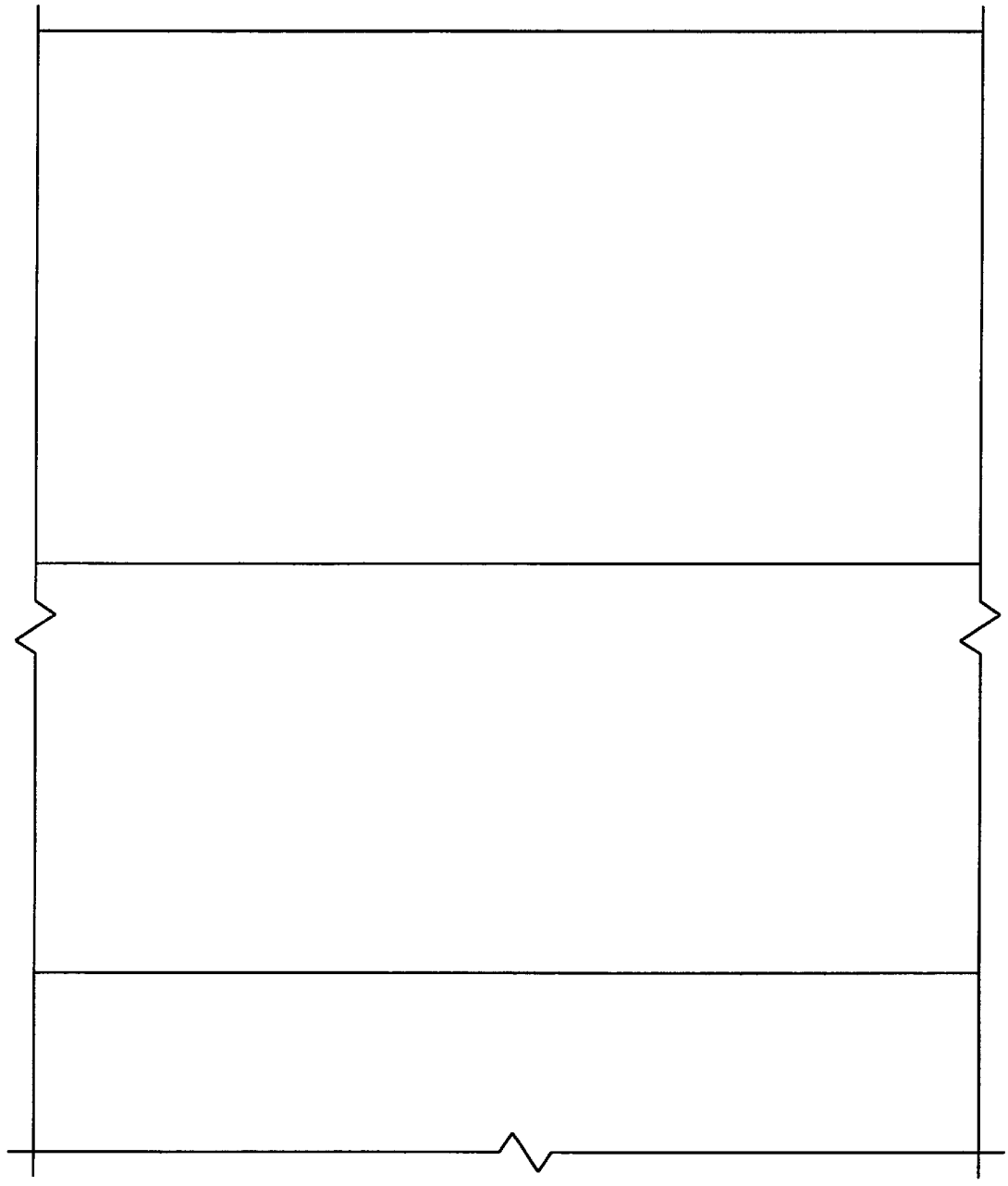

Fig 8.0505AD

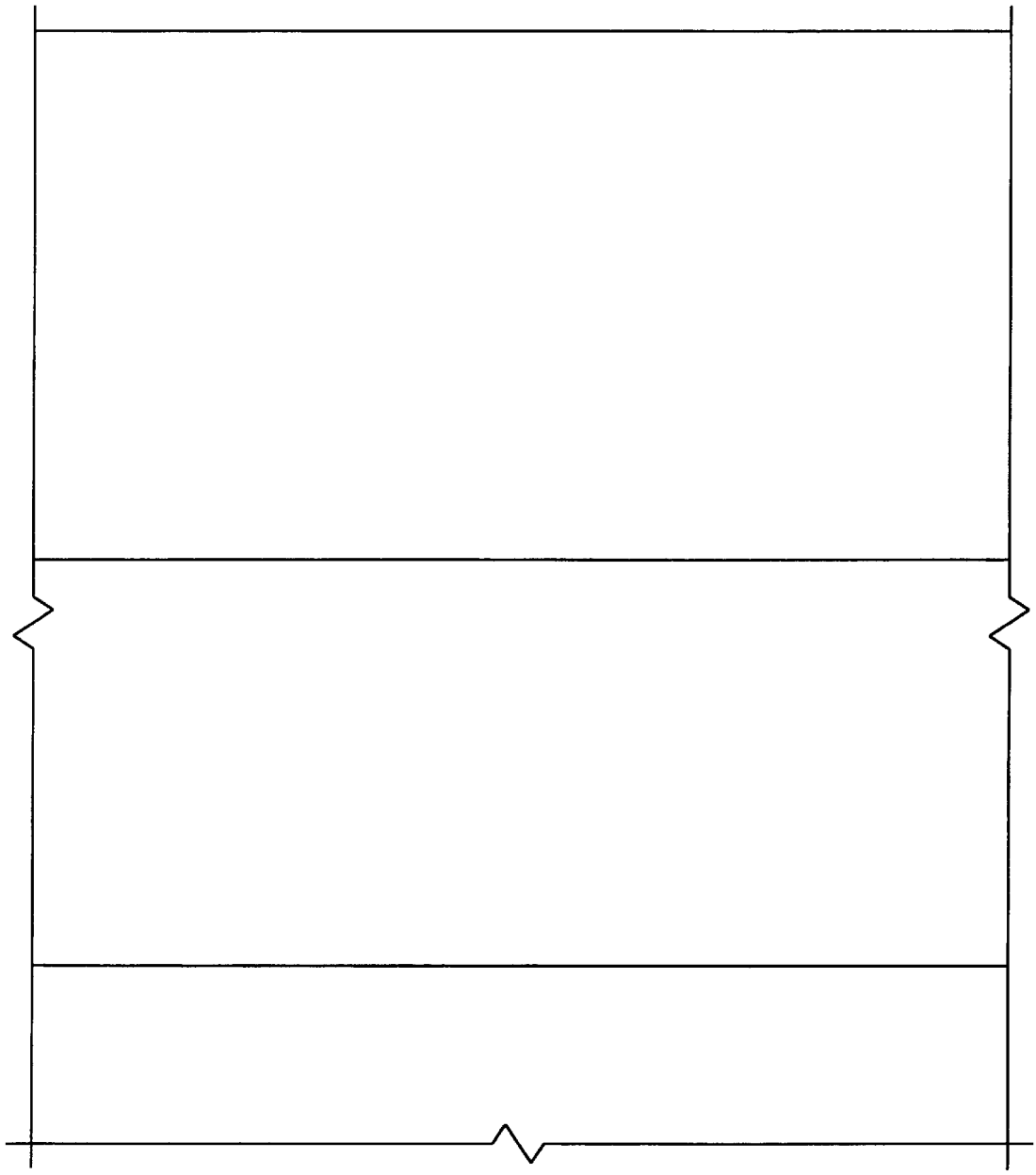

Fig 8.0505AE

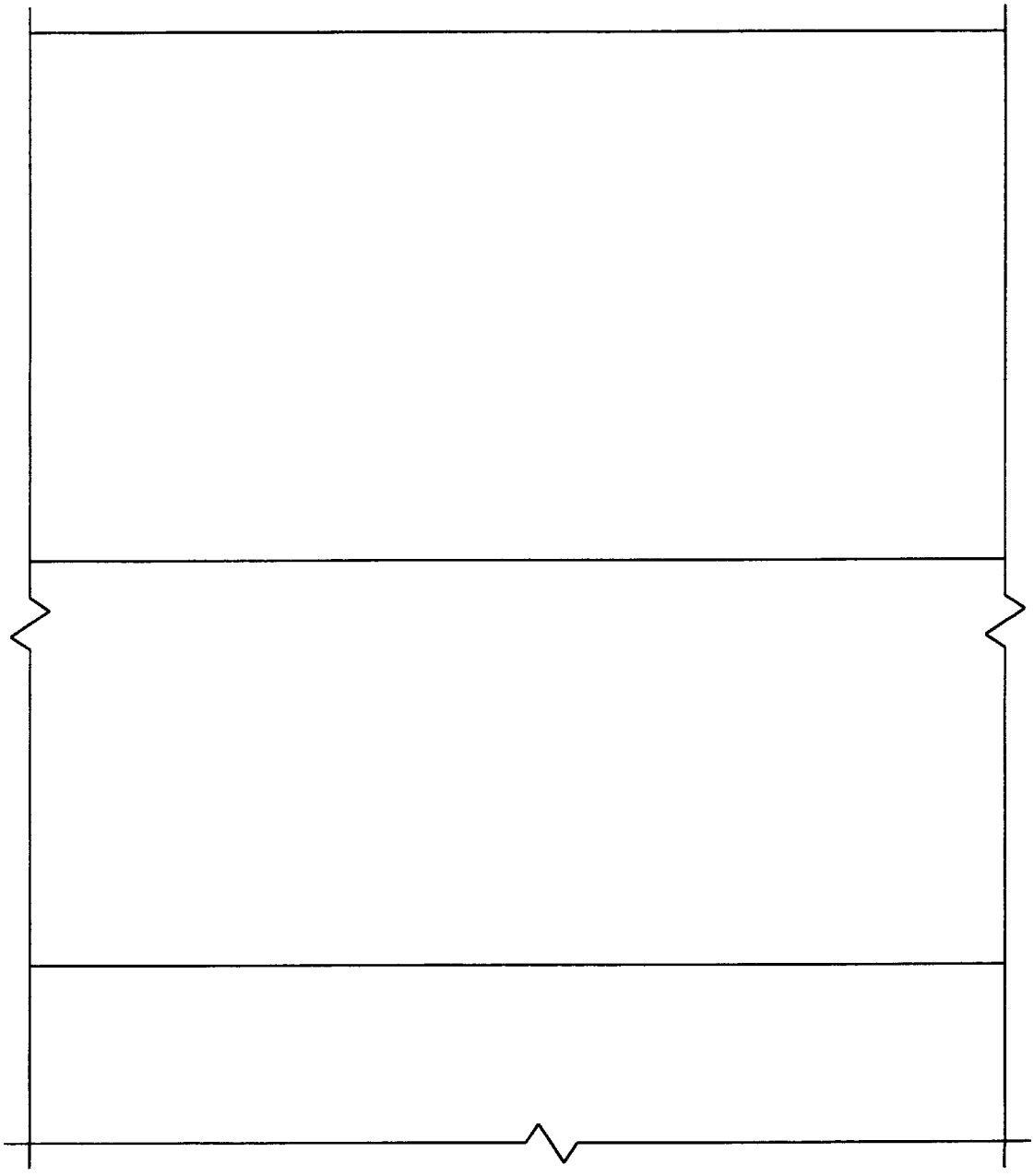

Fig 8.0505AF

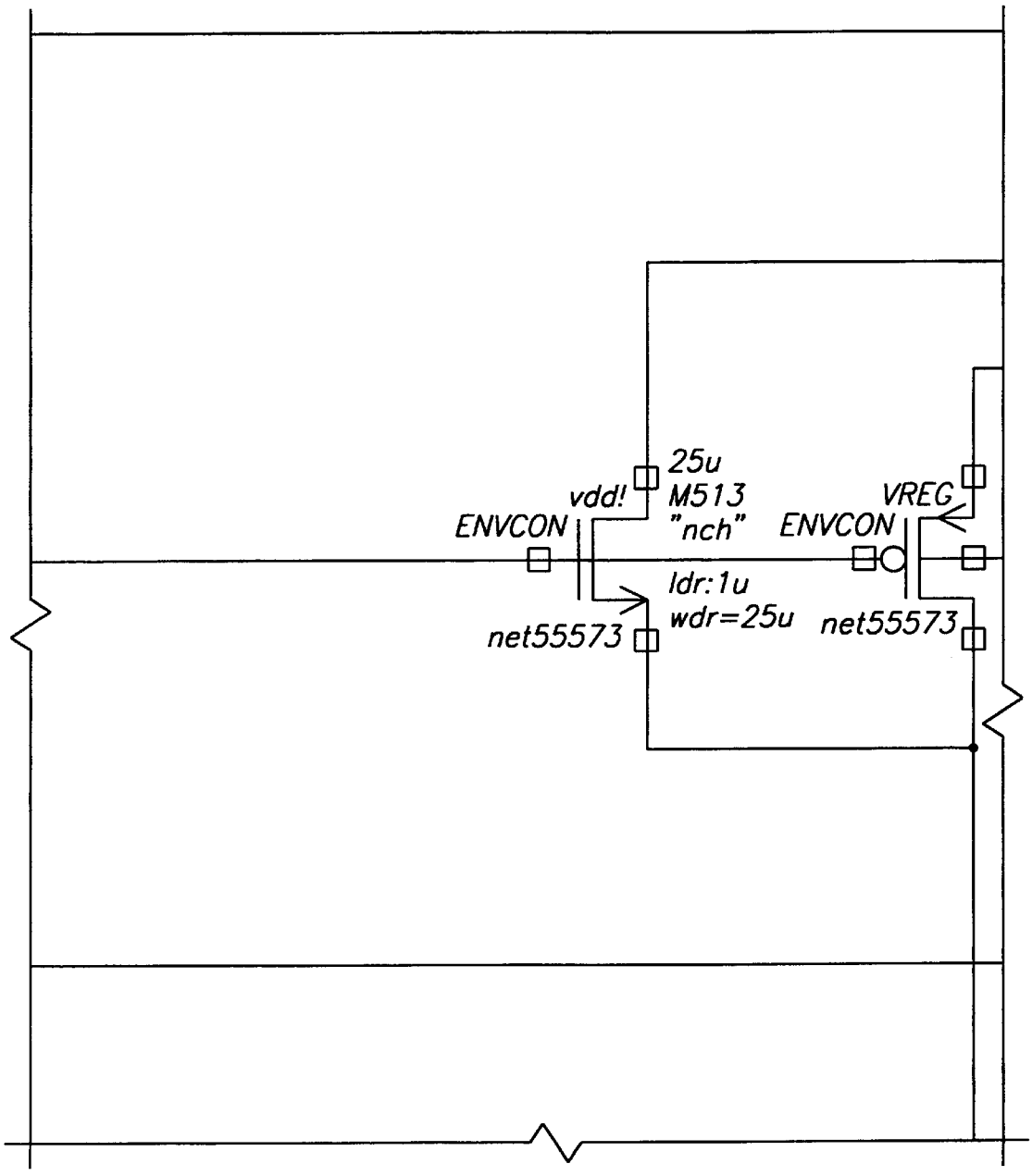
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Fig 8,058,AG

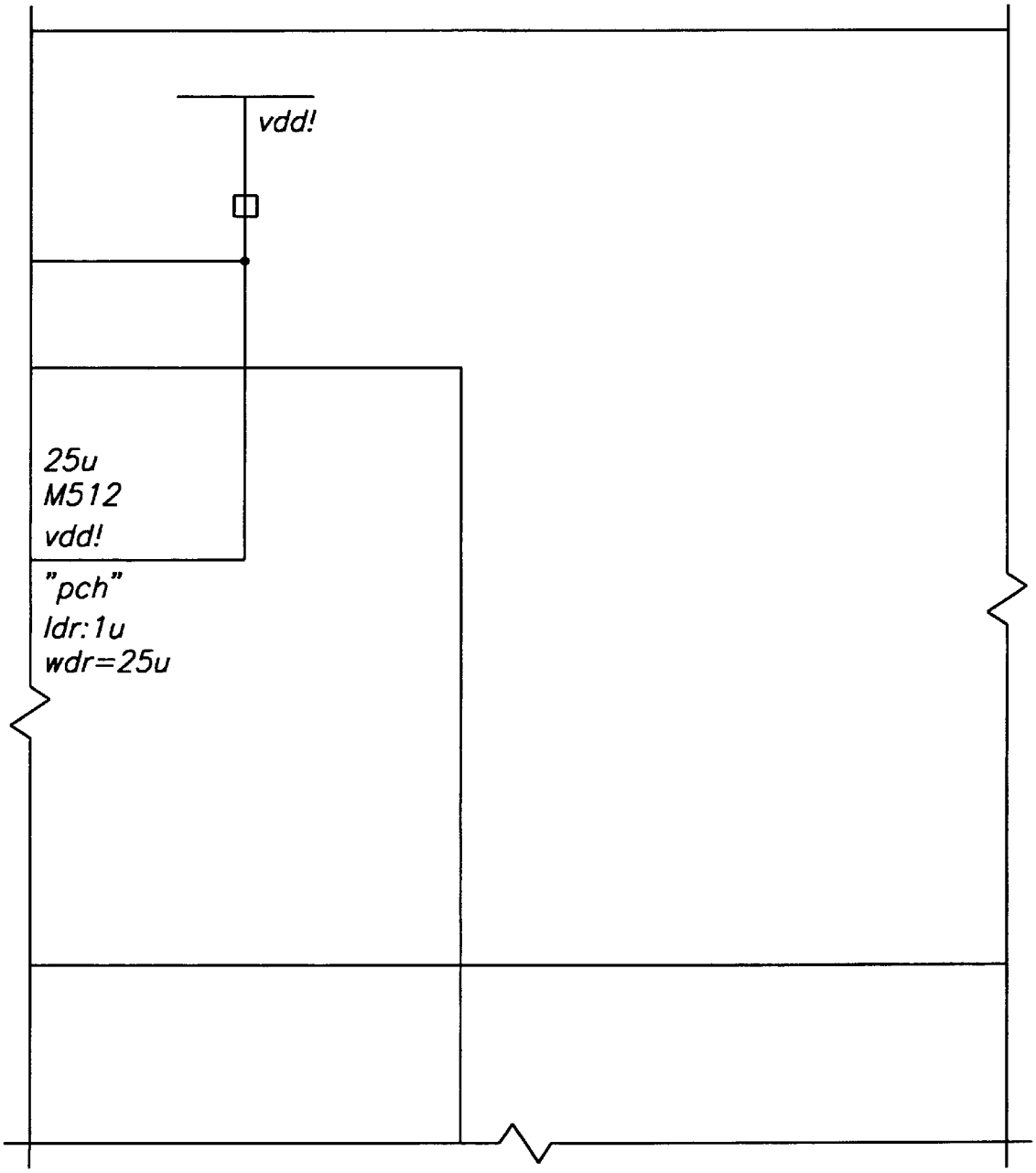

Fig 8.0505AH

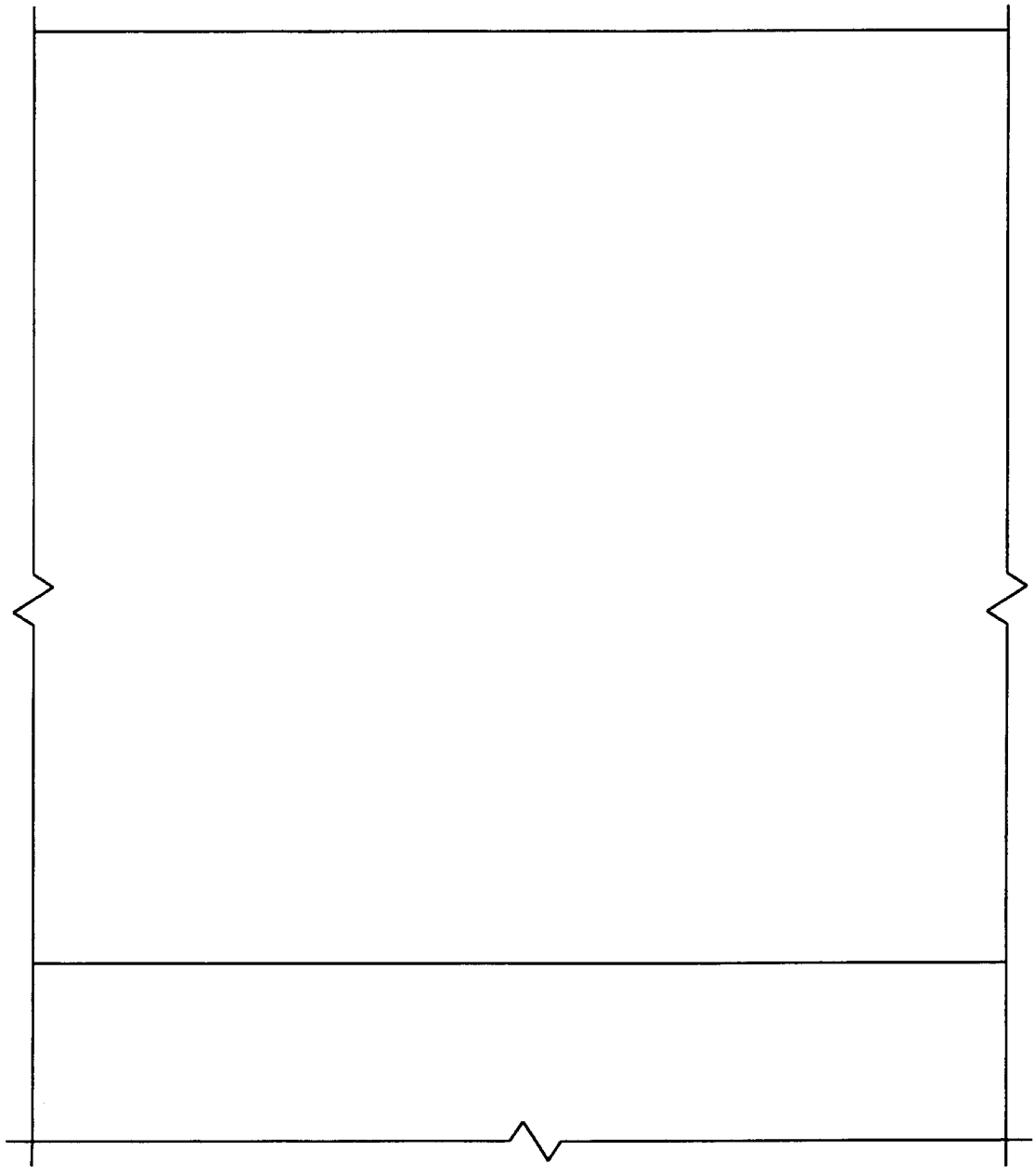

Fig 8.0508AI

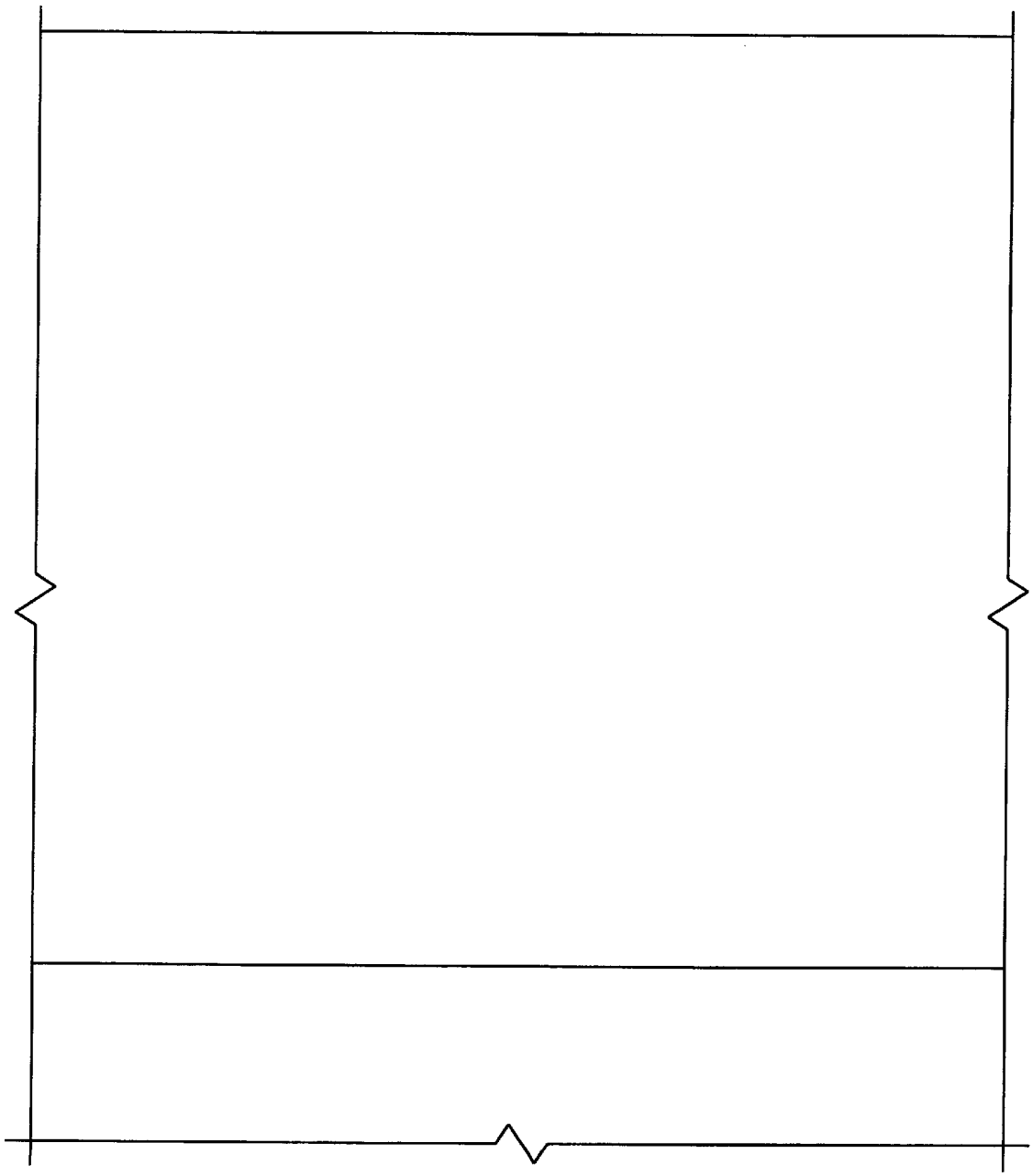

Fig 8.0505Aa

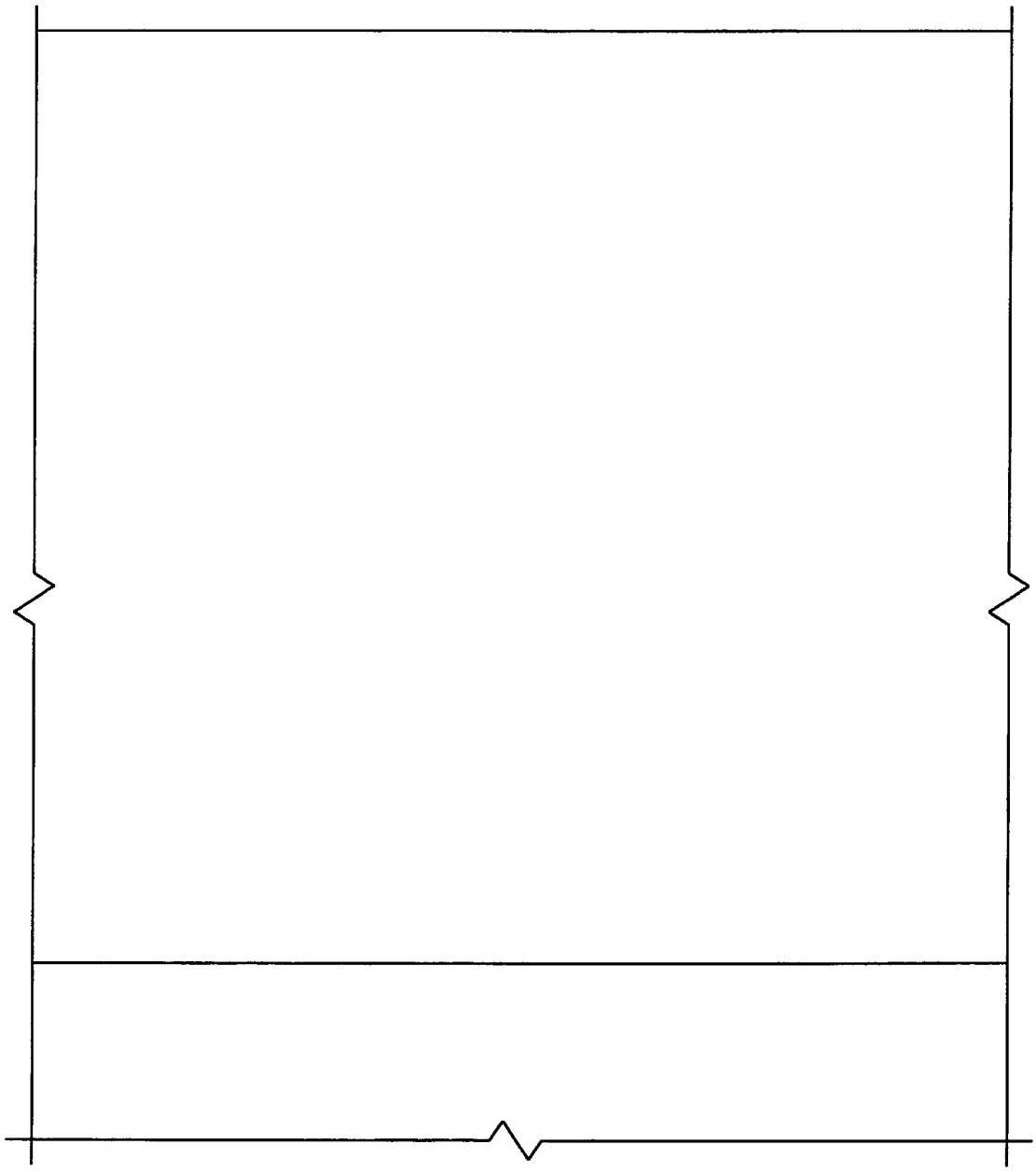

Fig 8.0505AK

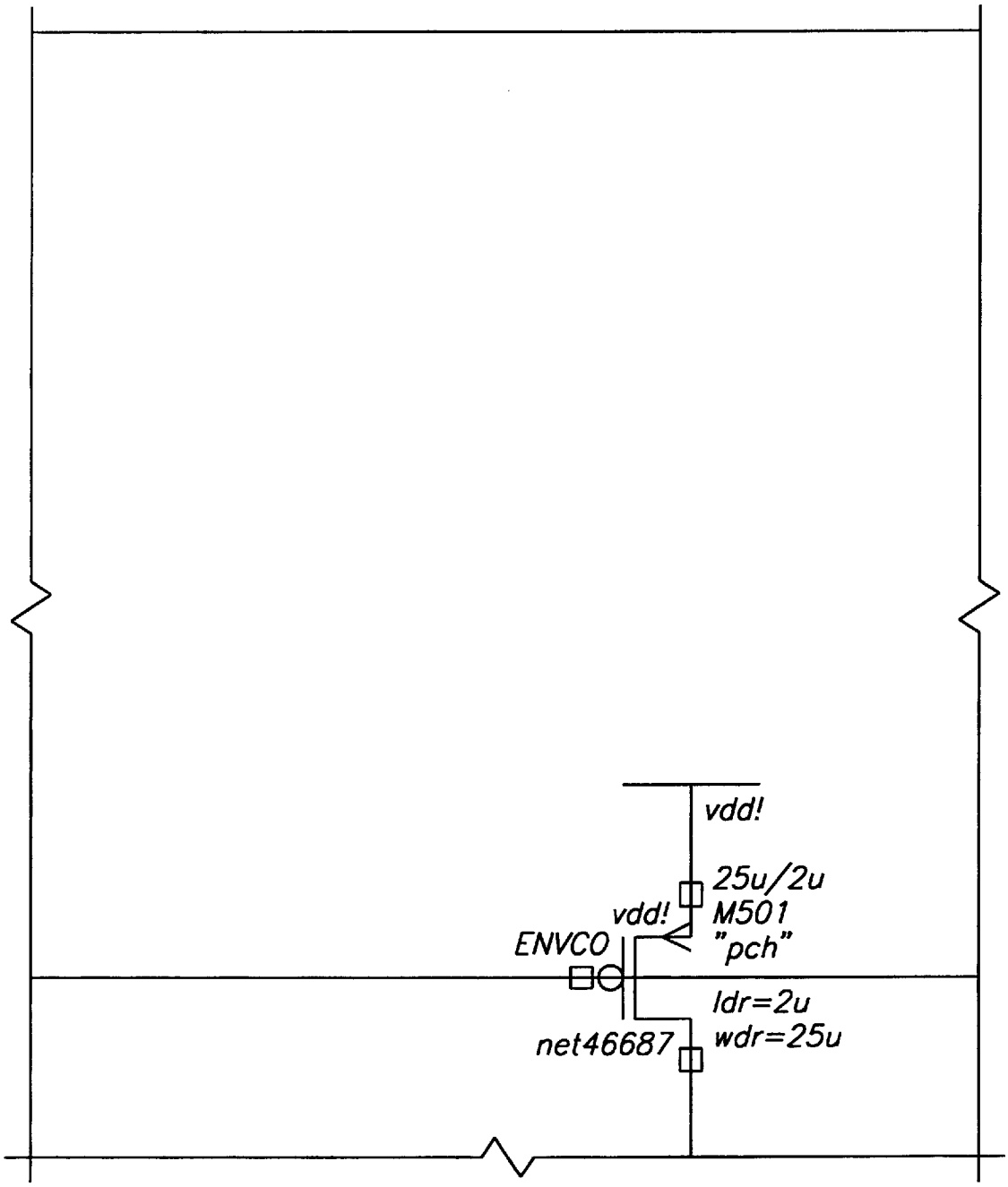

Fig 8.0505AL

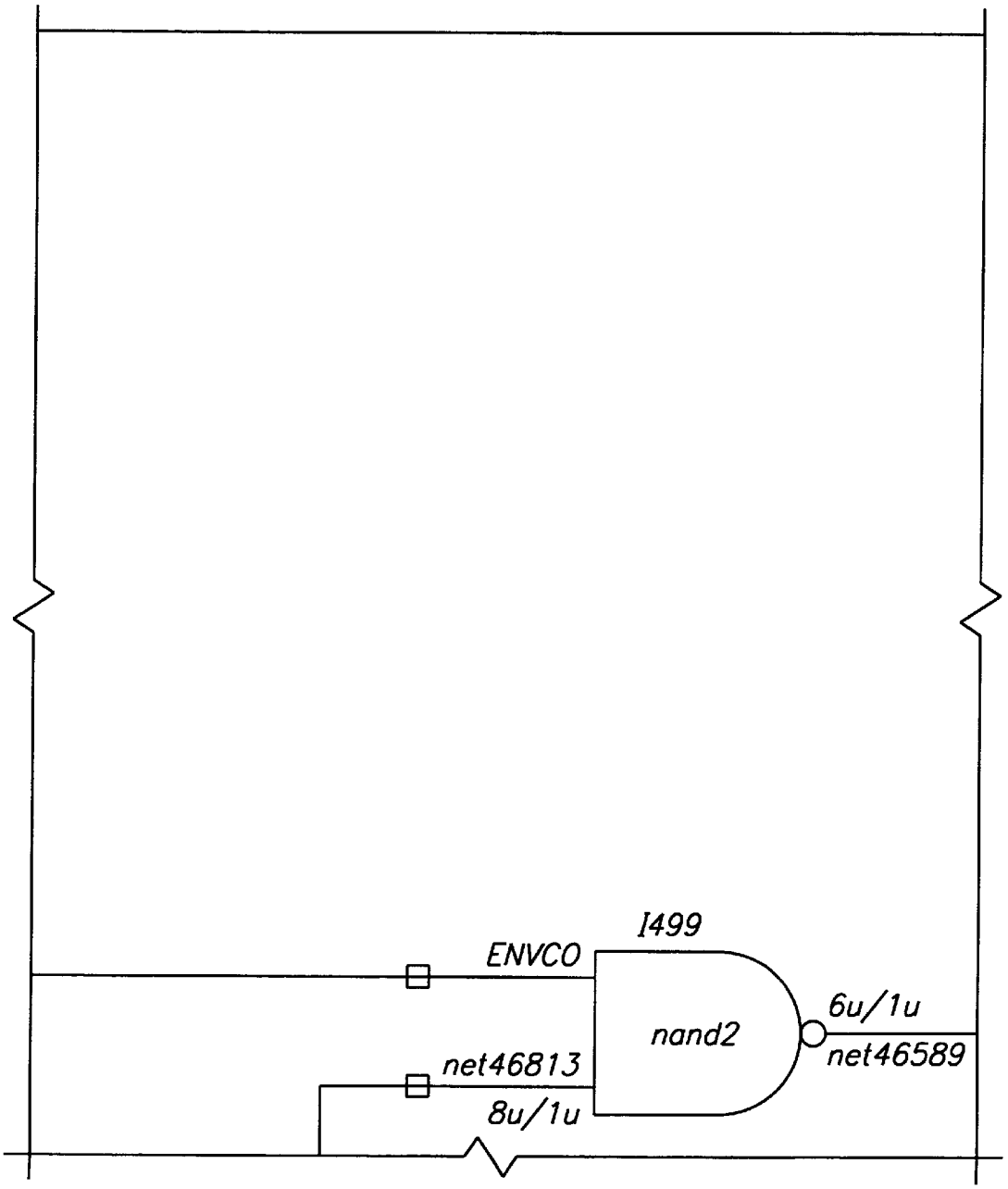

Fig 8,050,SAM

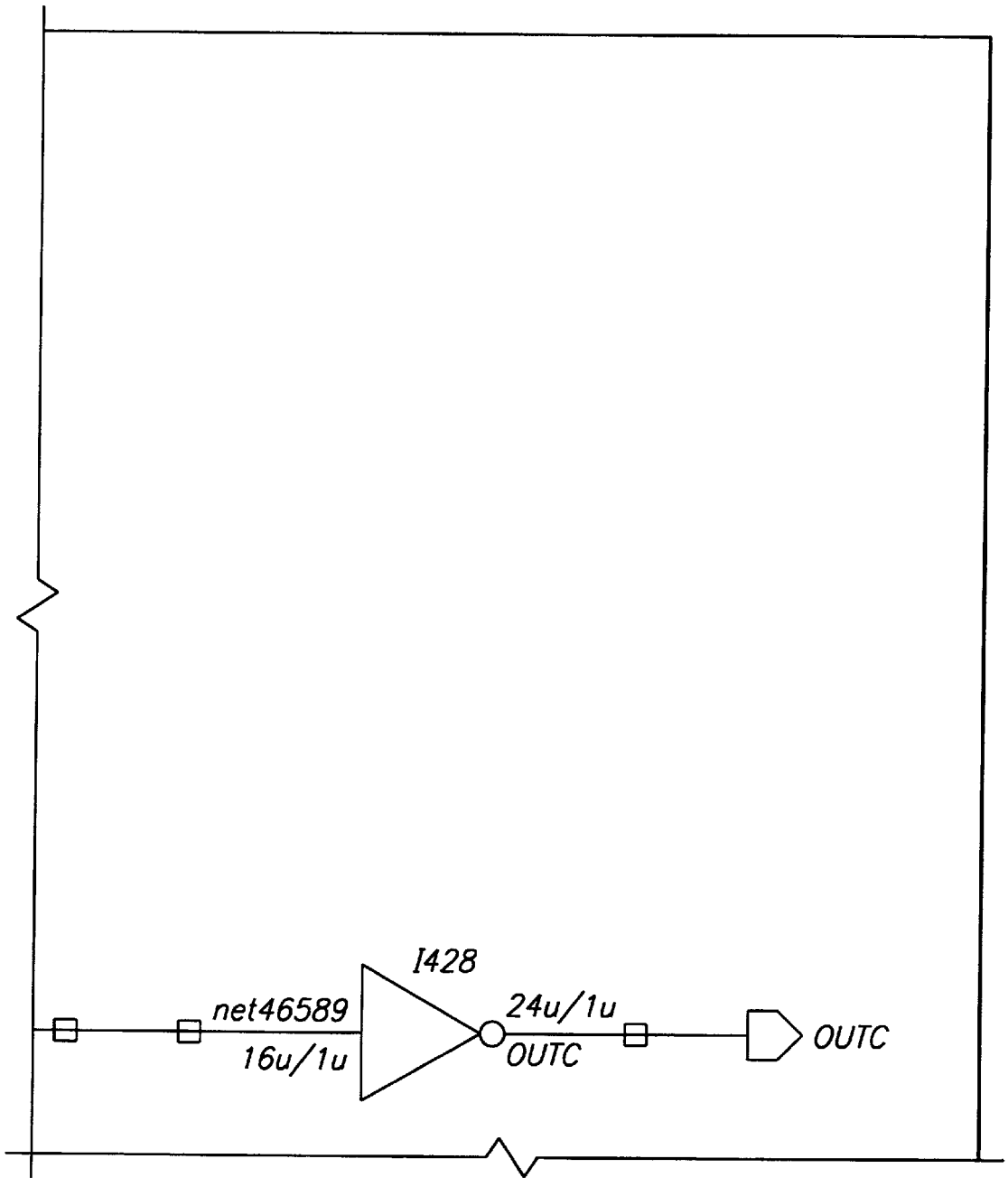

Fig 8.0505AN

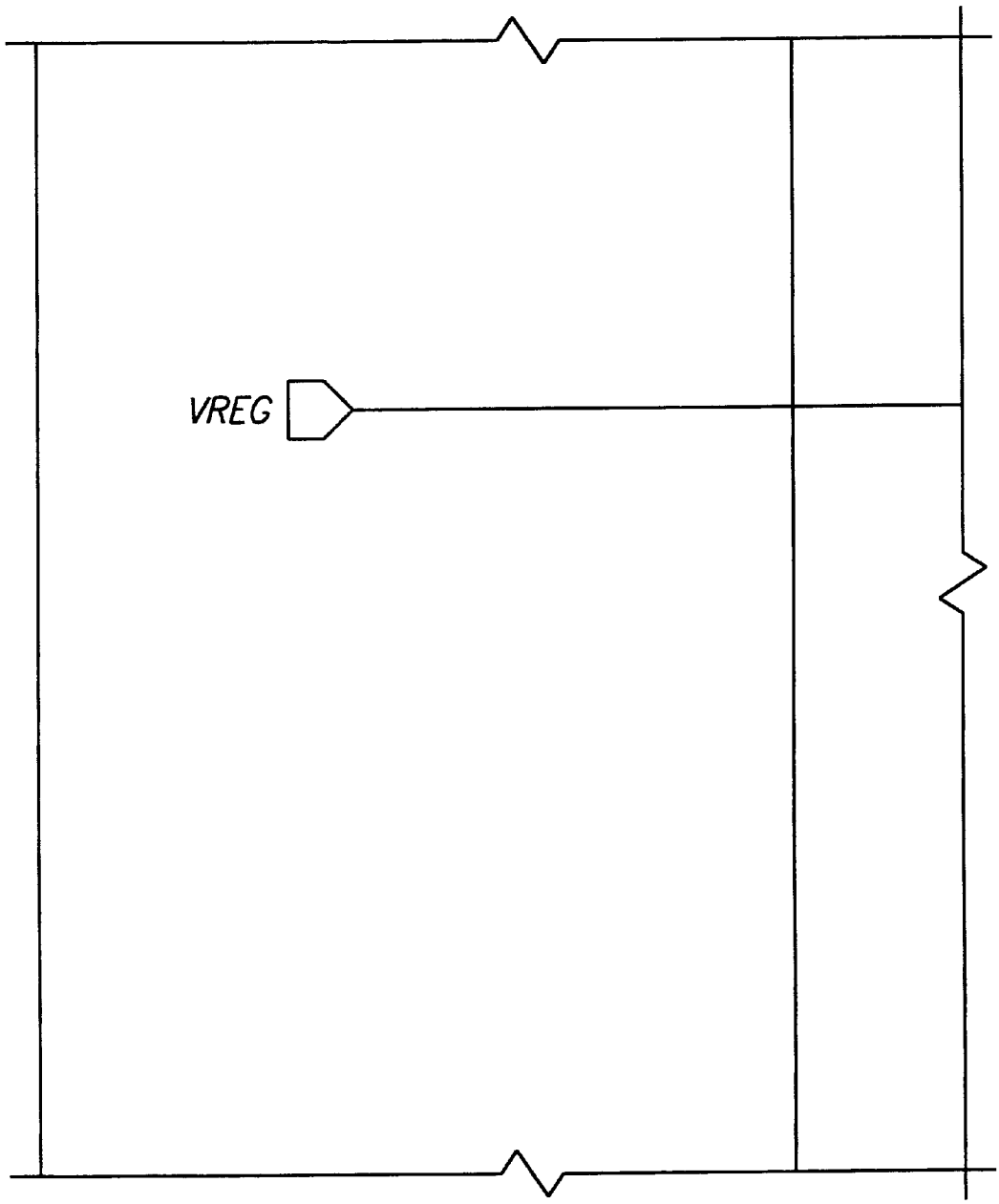

Fig 8.0505BA

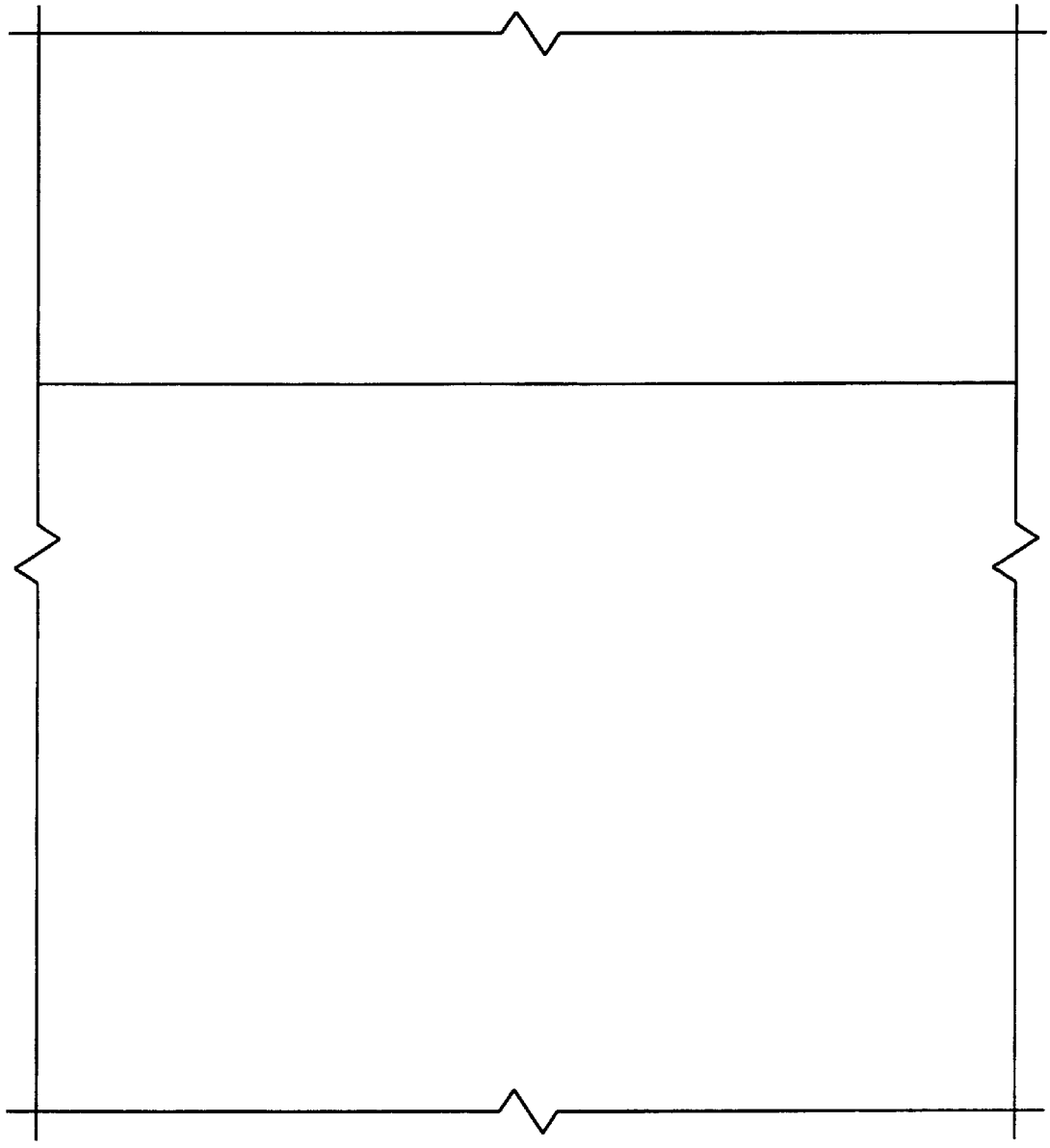

Fig 8.0505BB

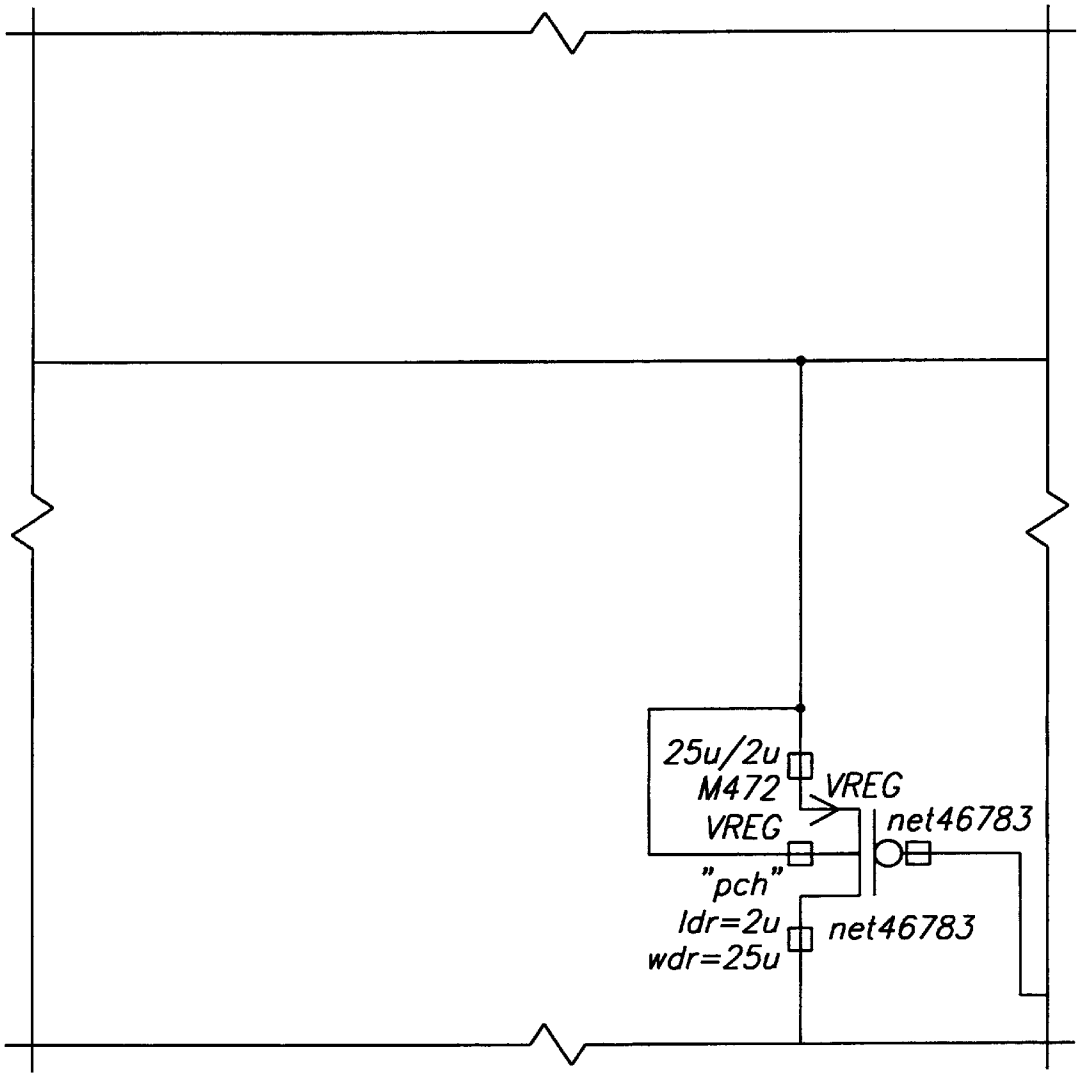

Fig 88,05058C

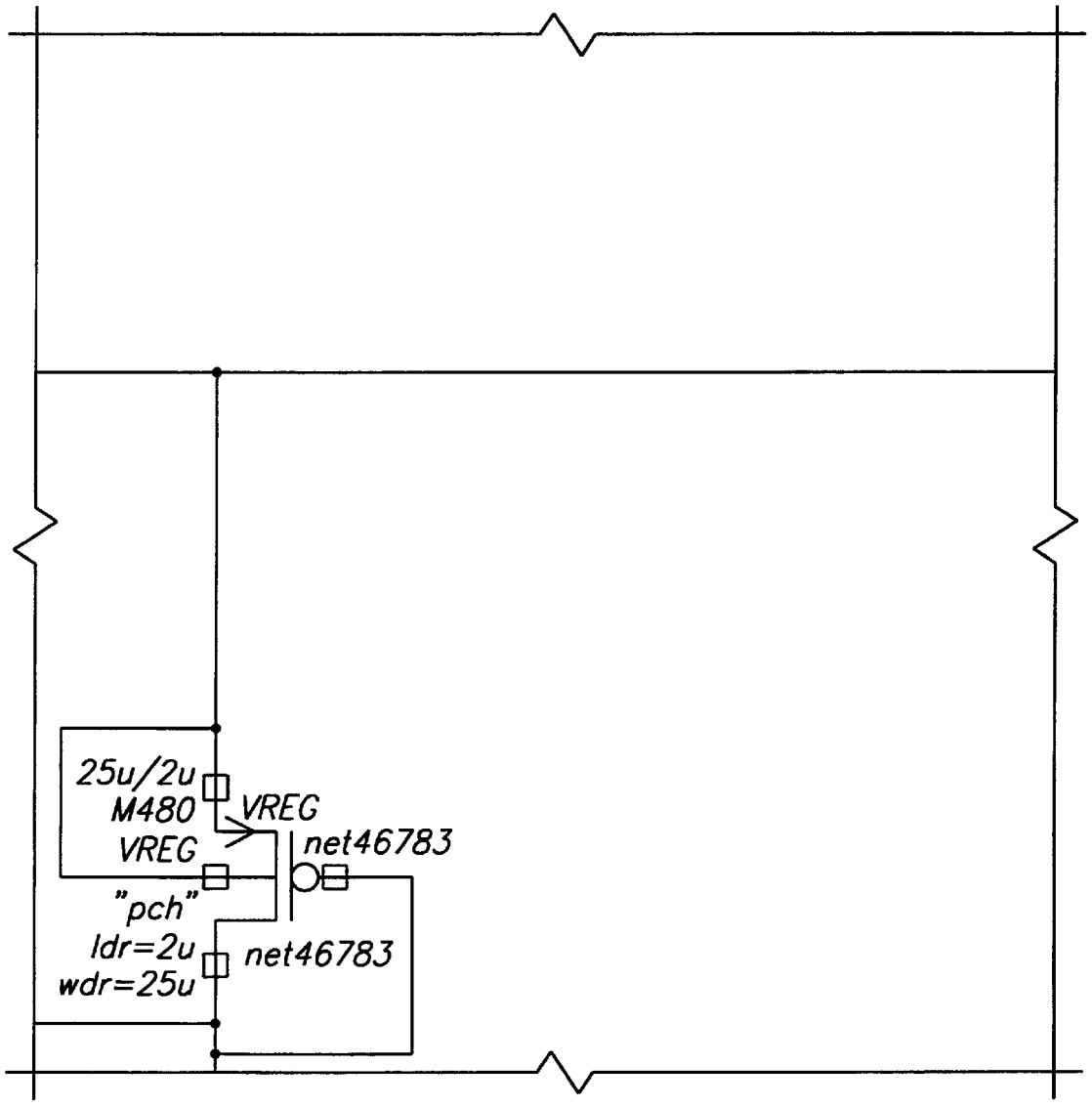

Fig 8.0505BD

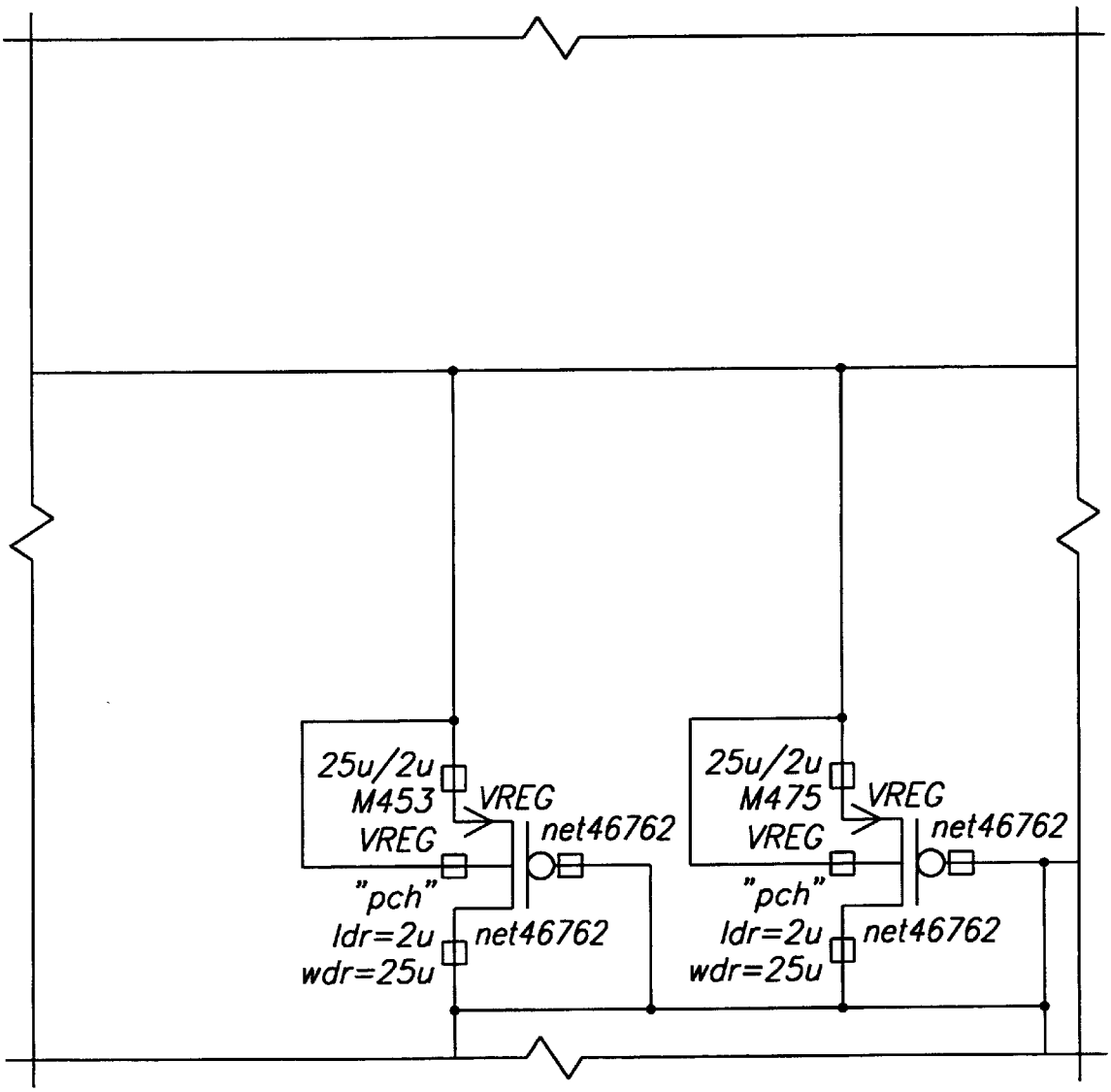
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Fig 8,058,BE

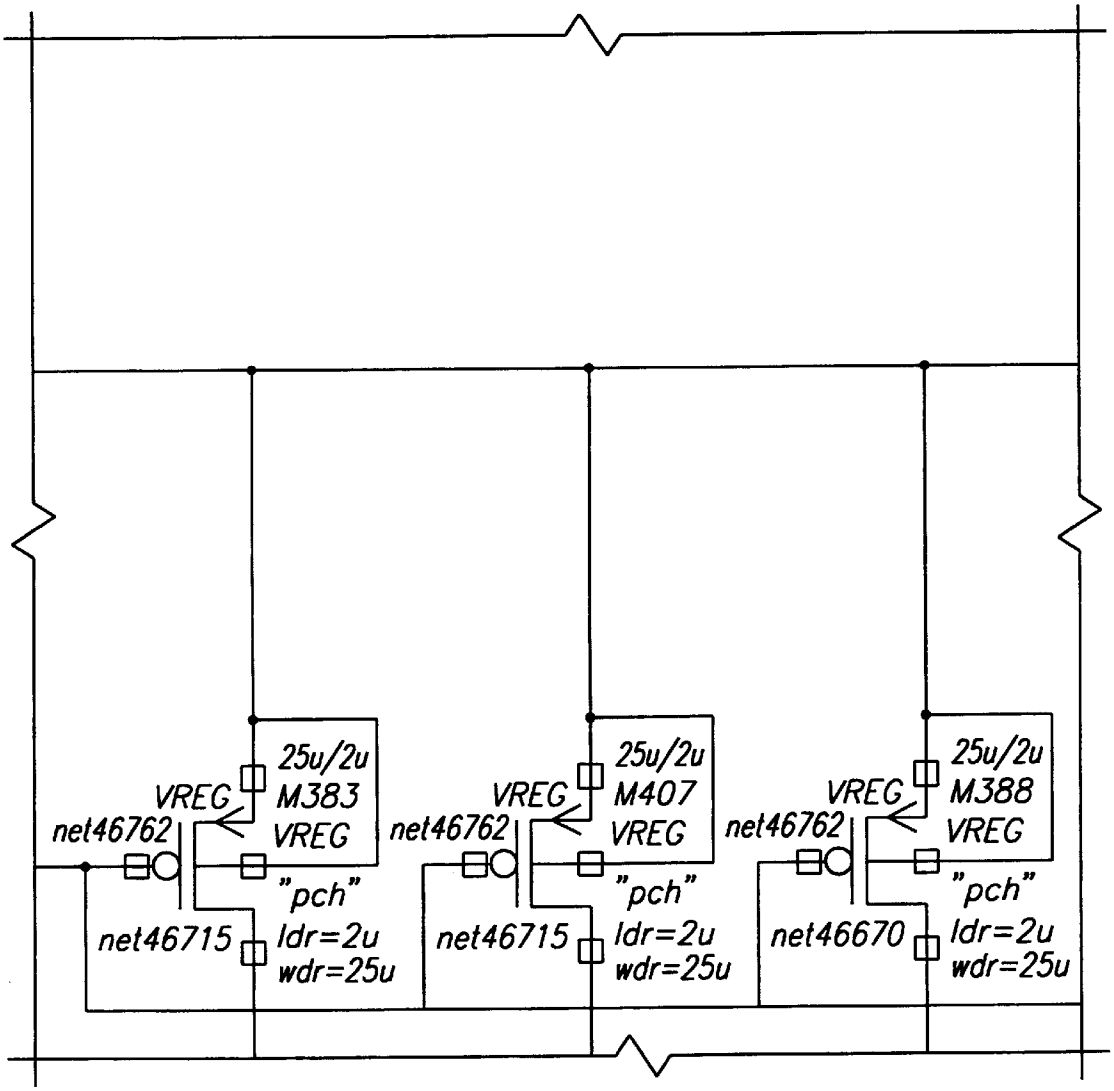
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Fig 8,005,187

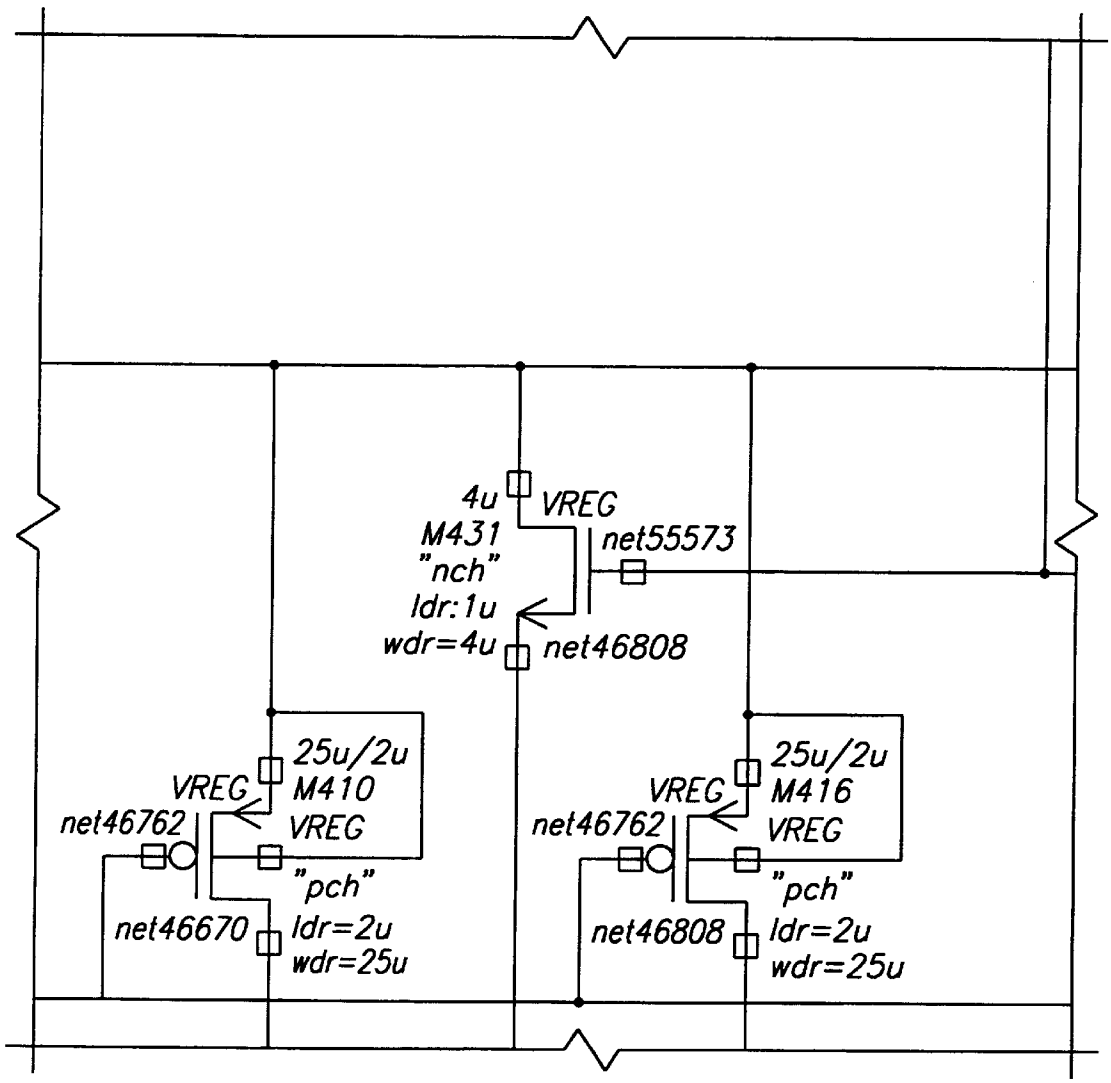
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FIG 8,005,186

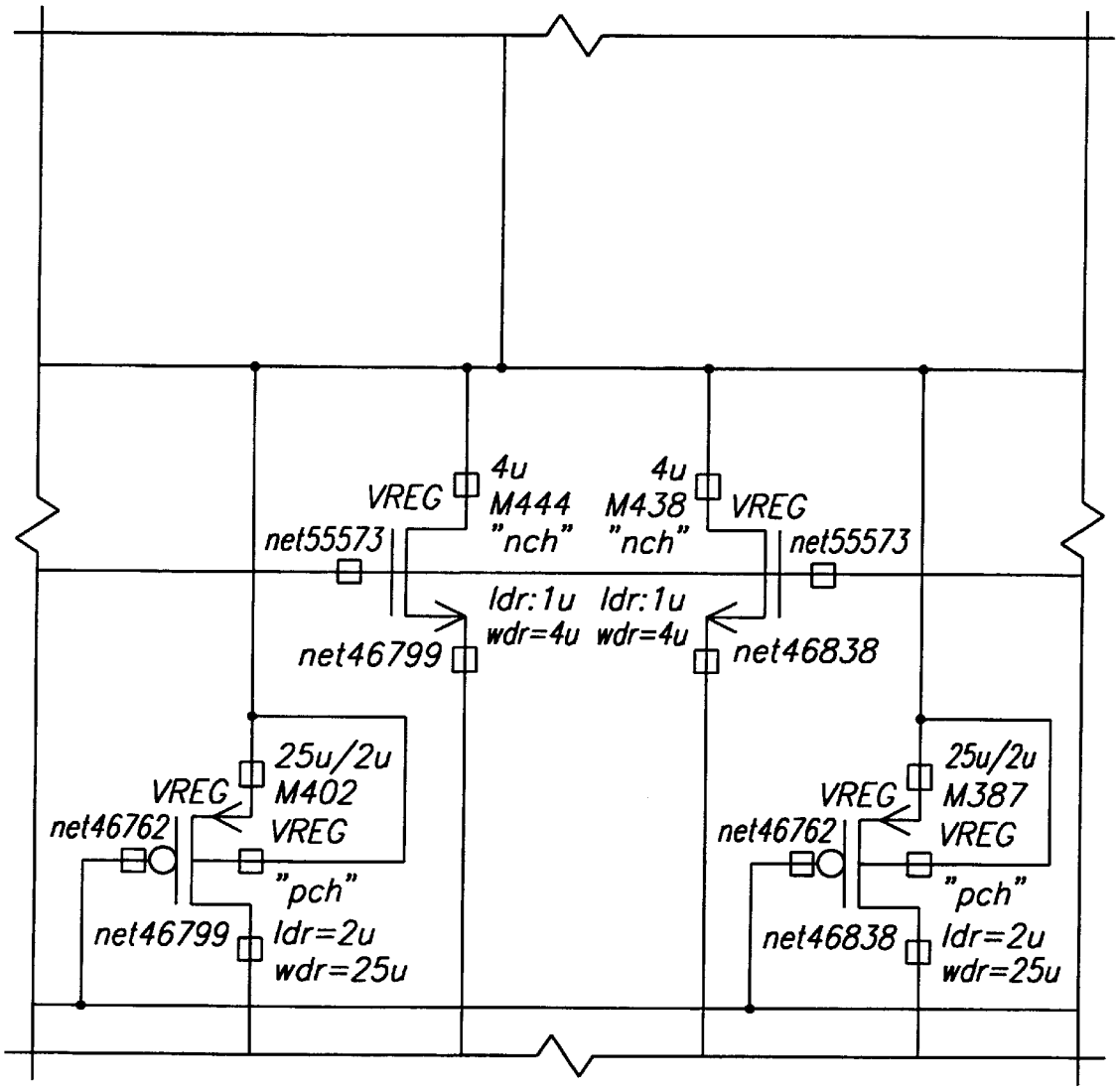
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Fig 8.0505BH

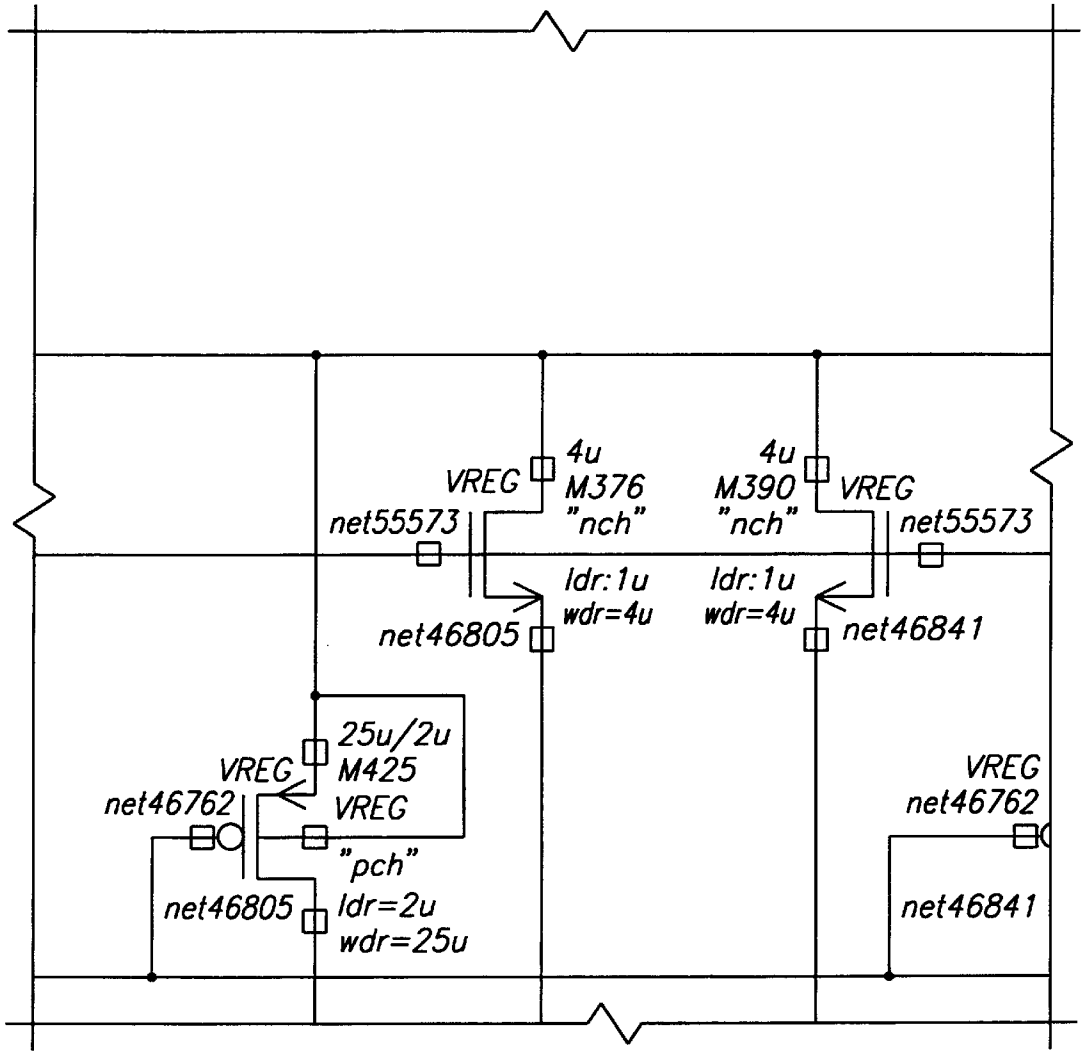
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Fig 8.0505B1

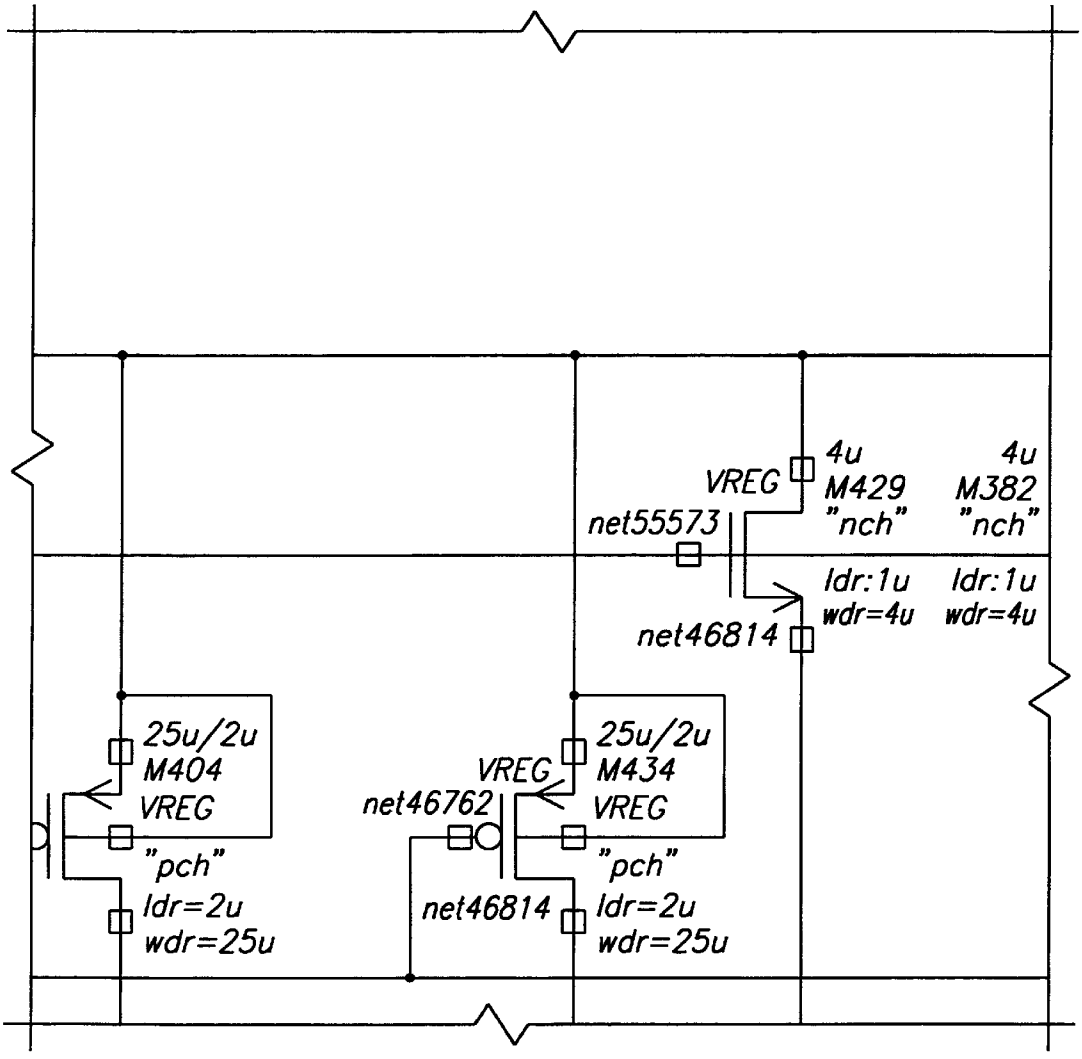
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Fig 8,050,801

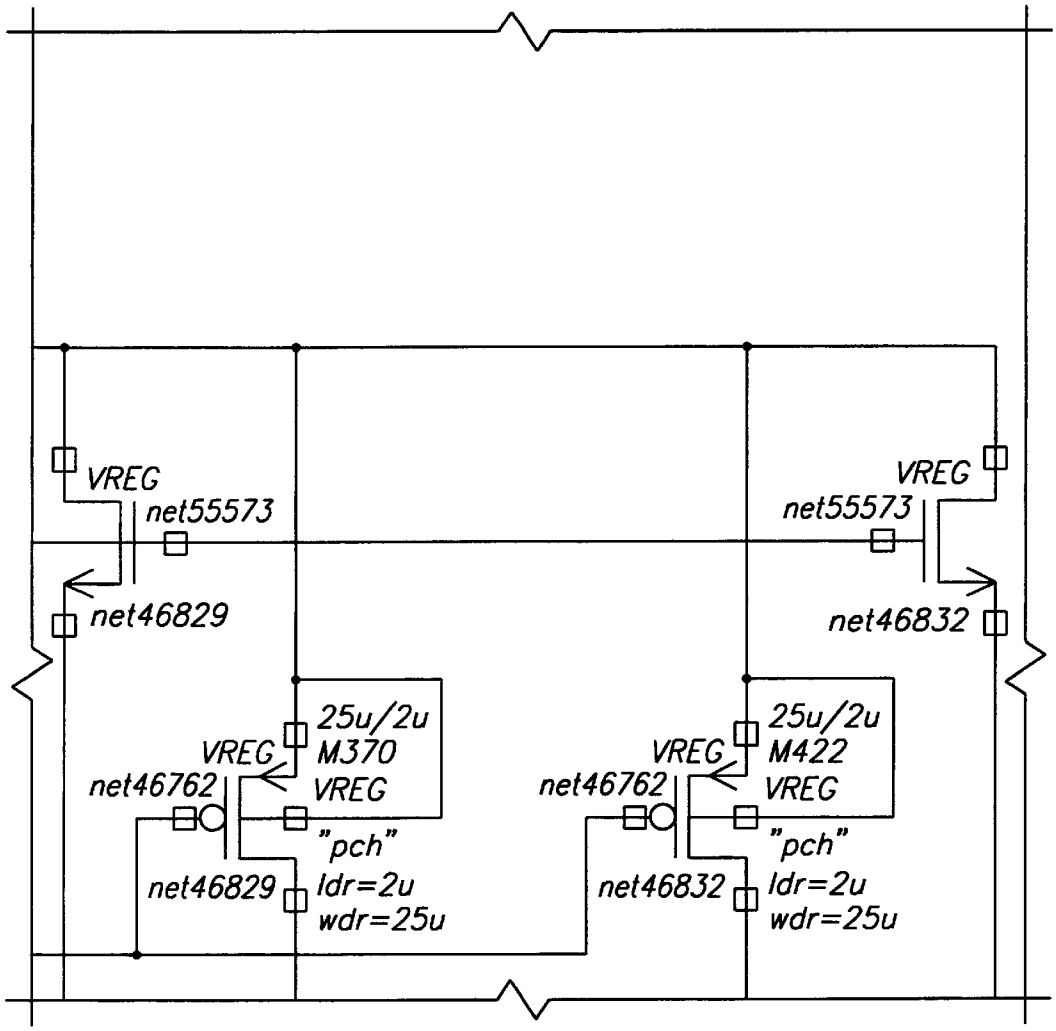
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Fig 8,050,BK

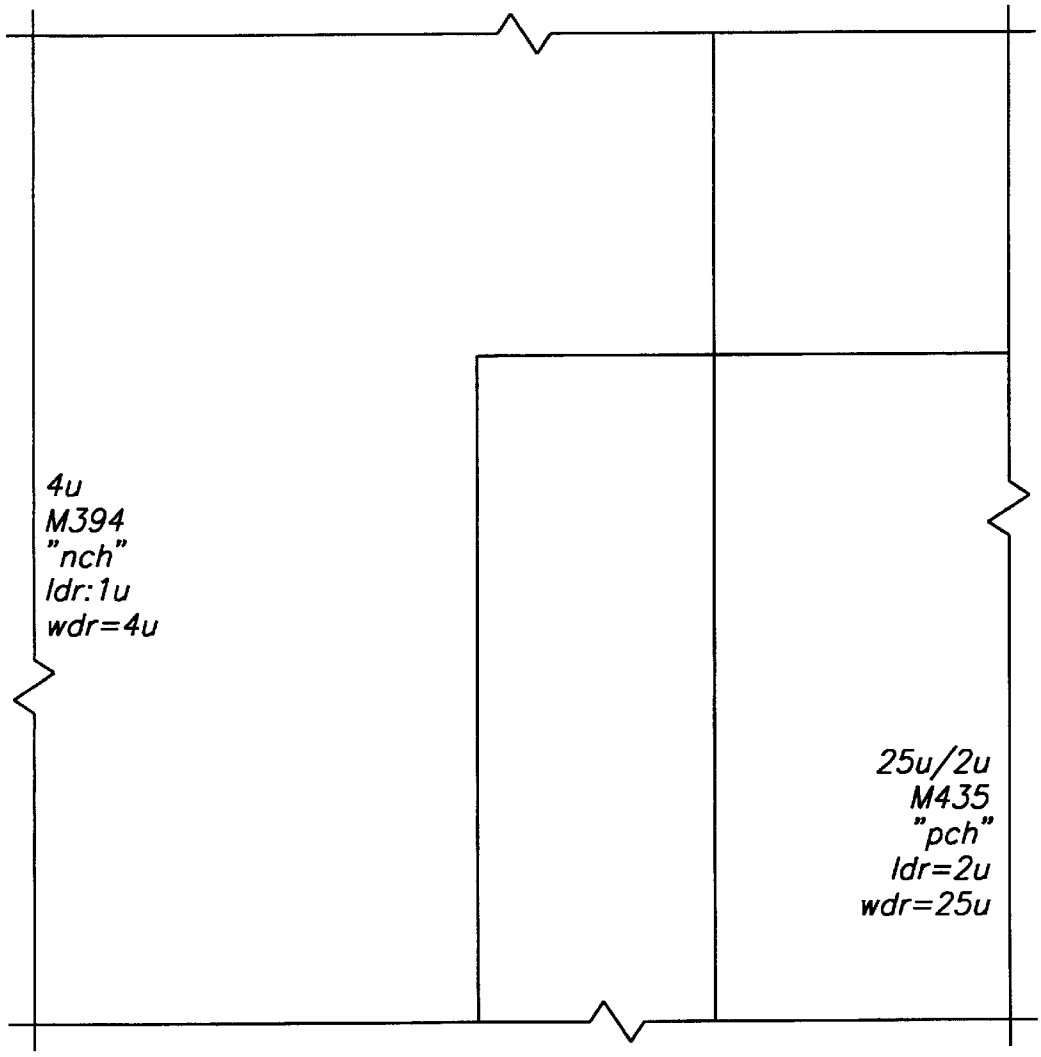

Fig 8,050,81

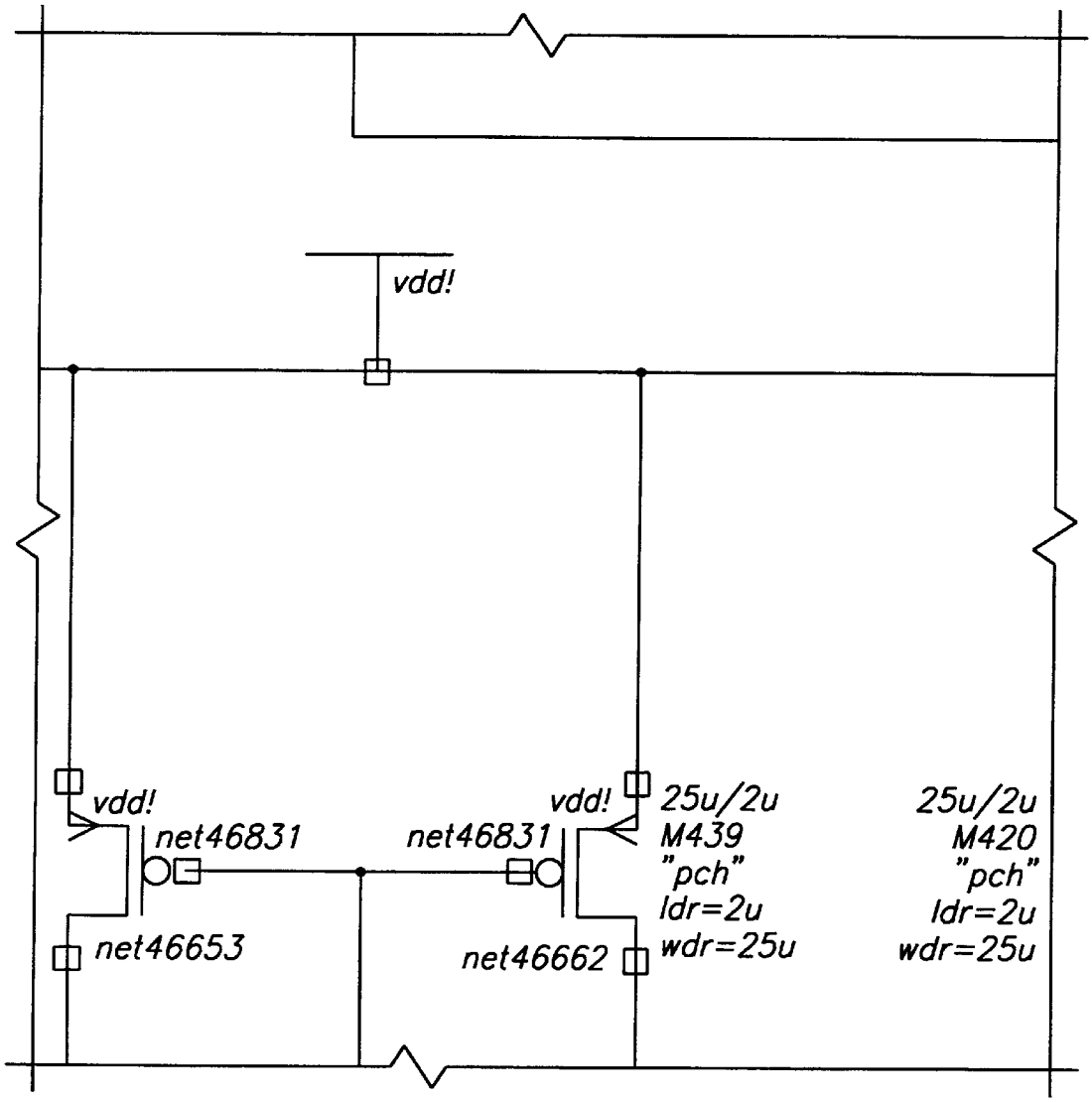
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Fig 8.0505BM

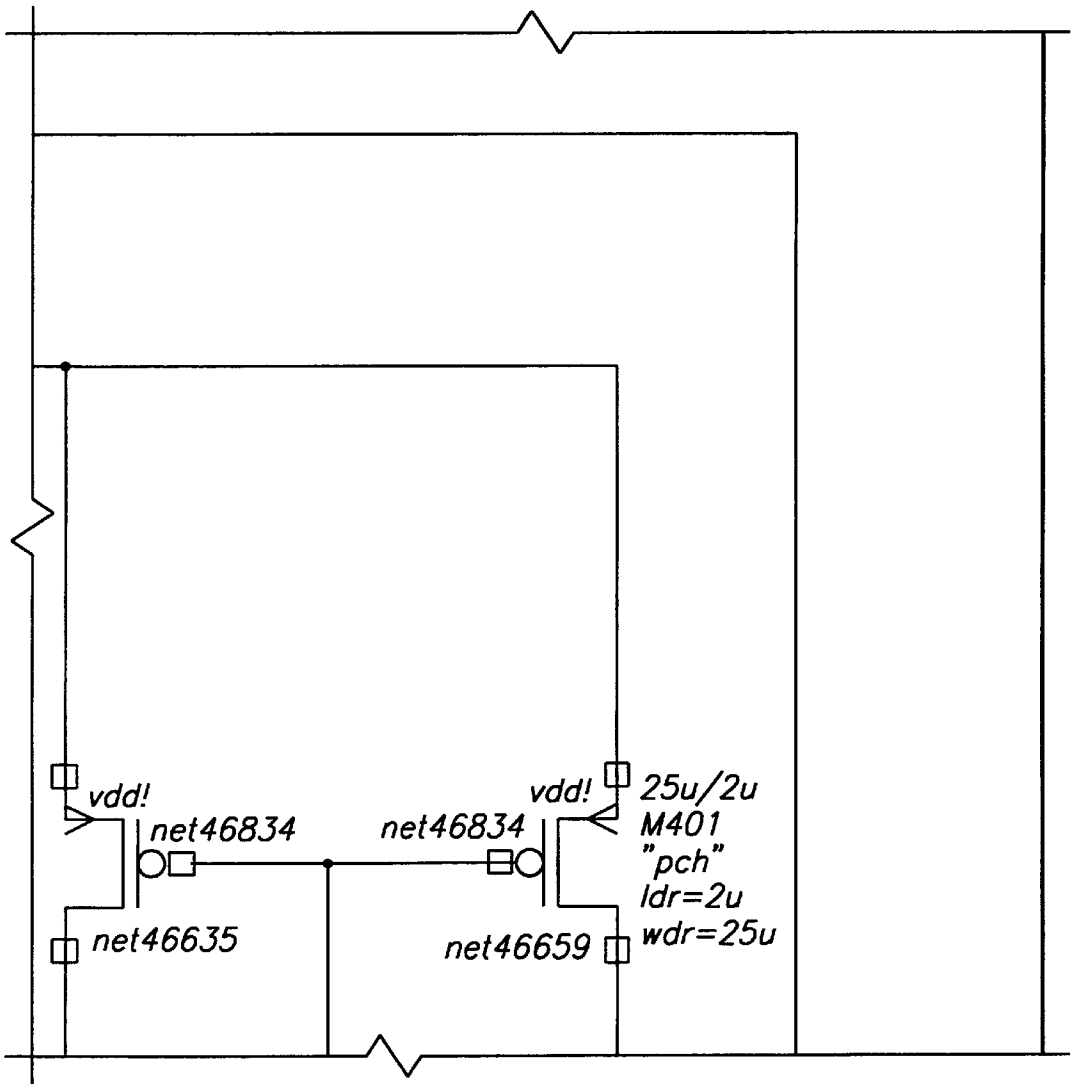
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FIG 8,050,BN

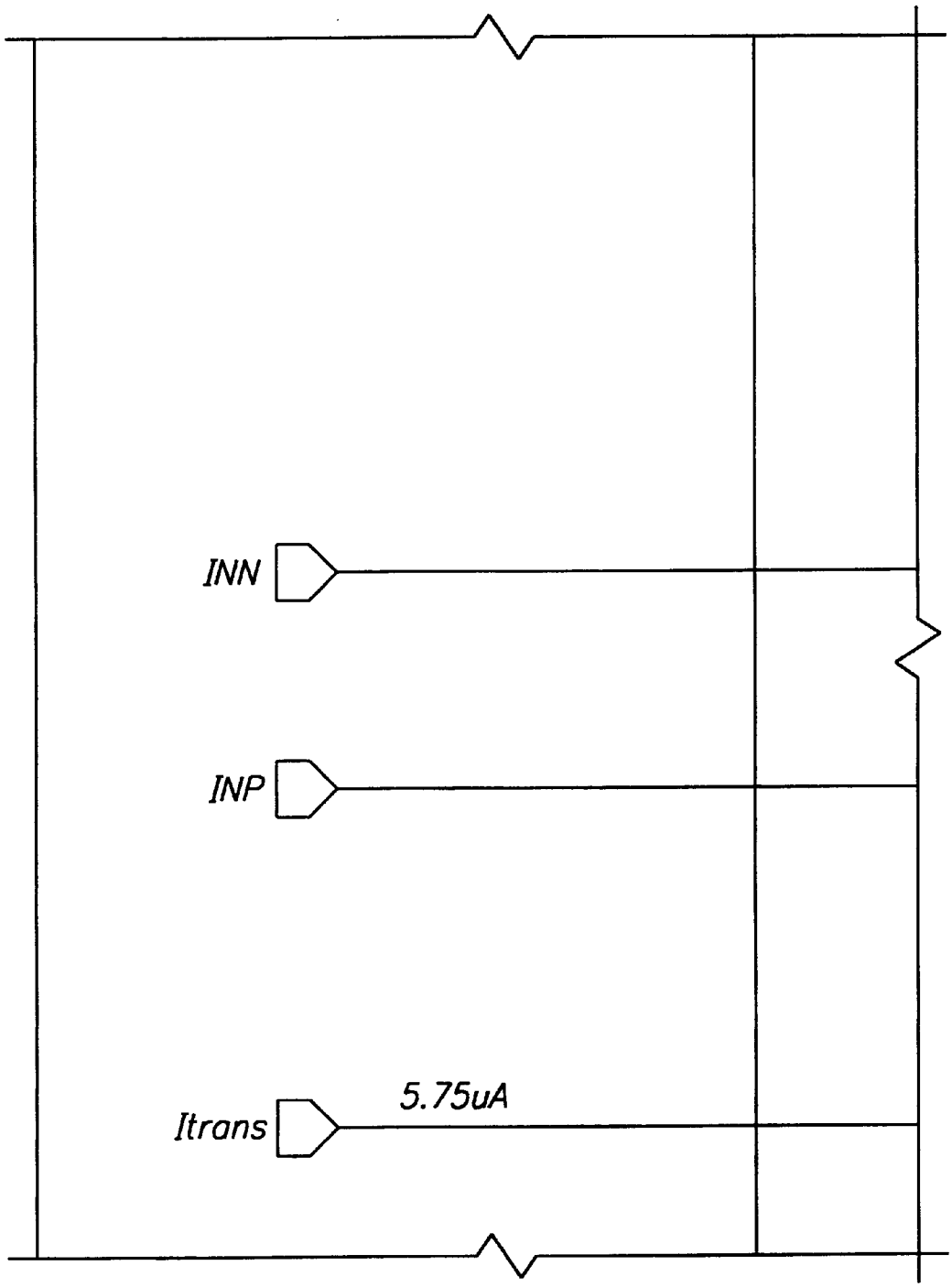
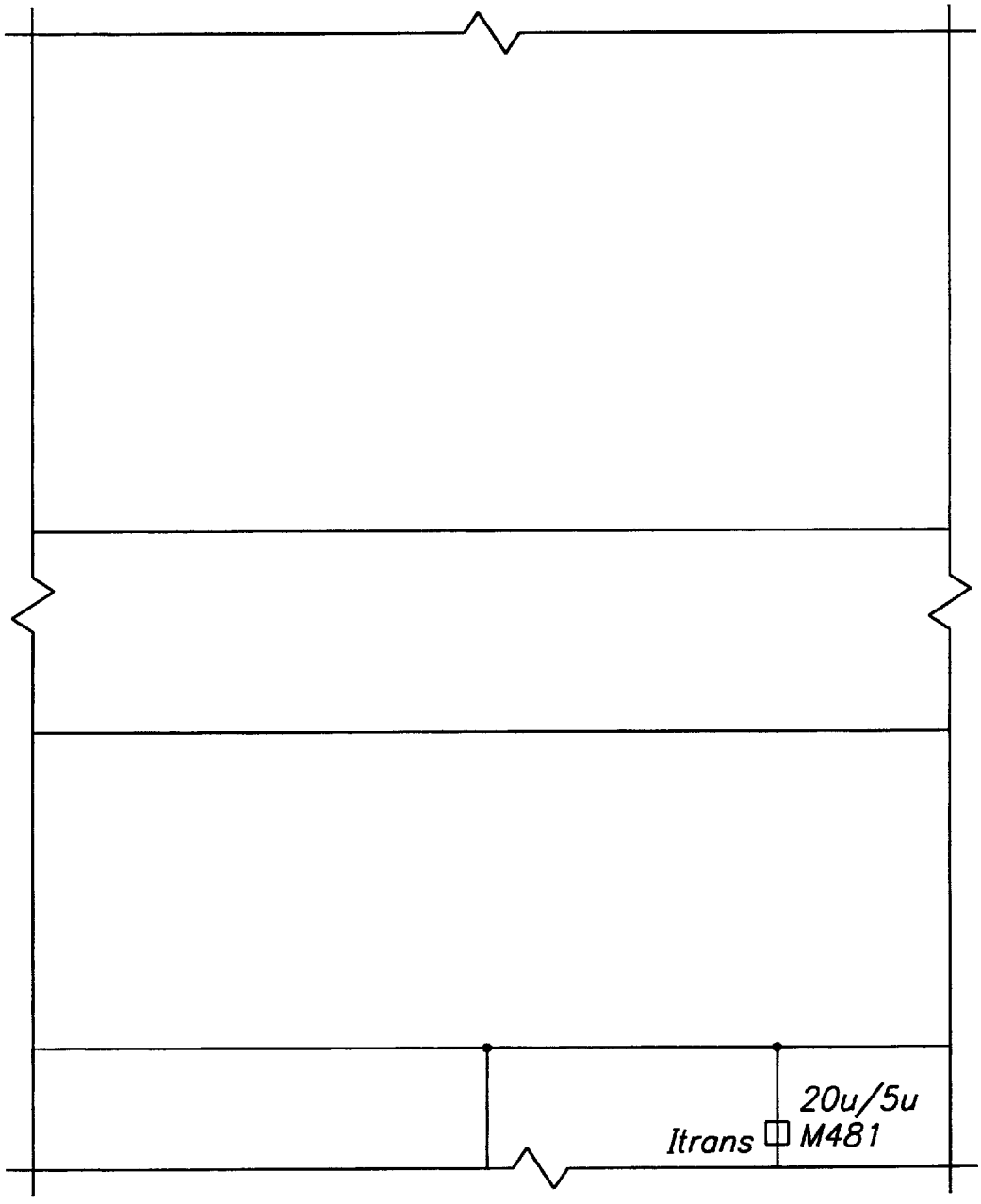


Fig 88.0505CA



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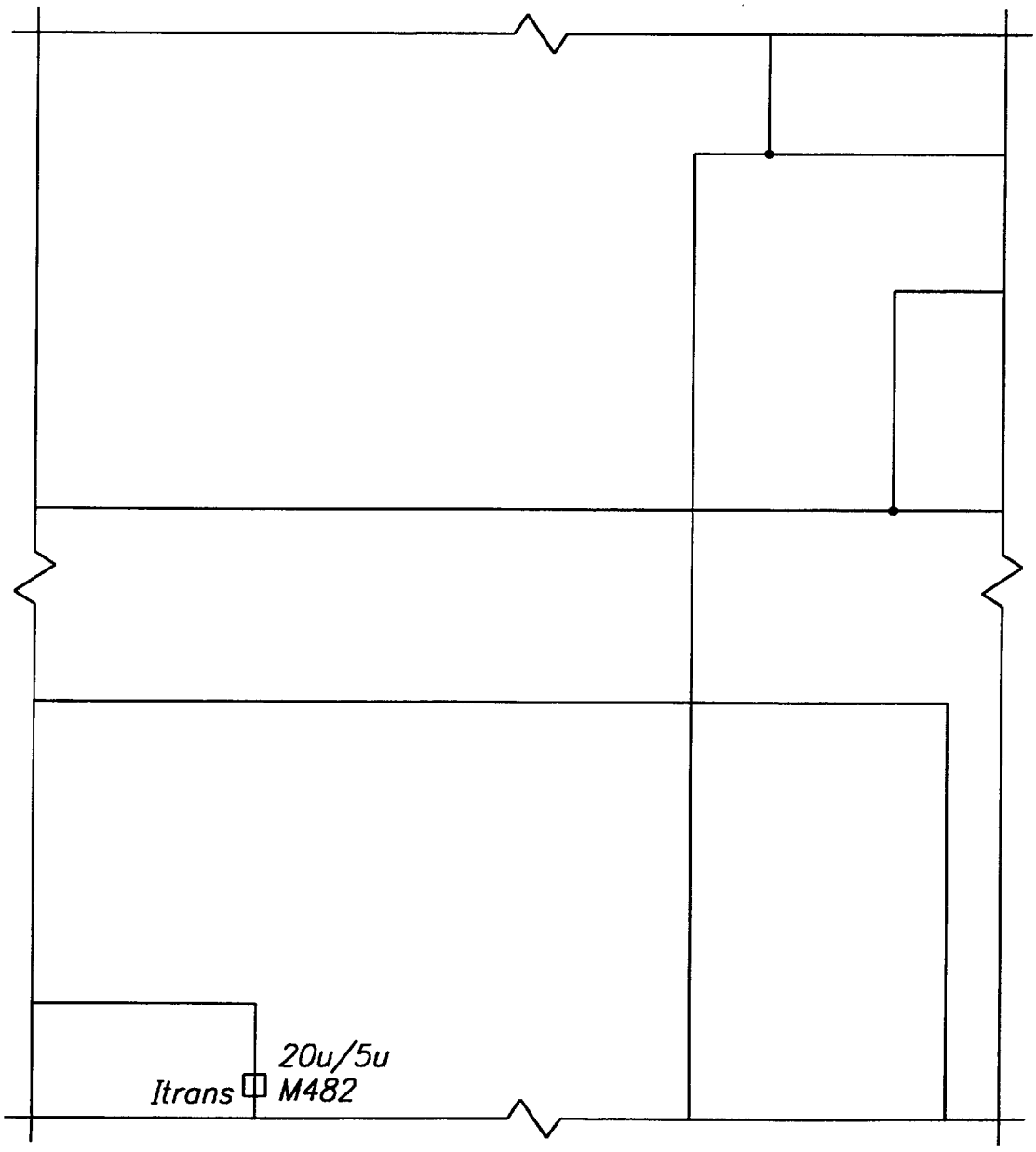

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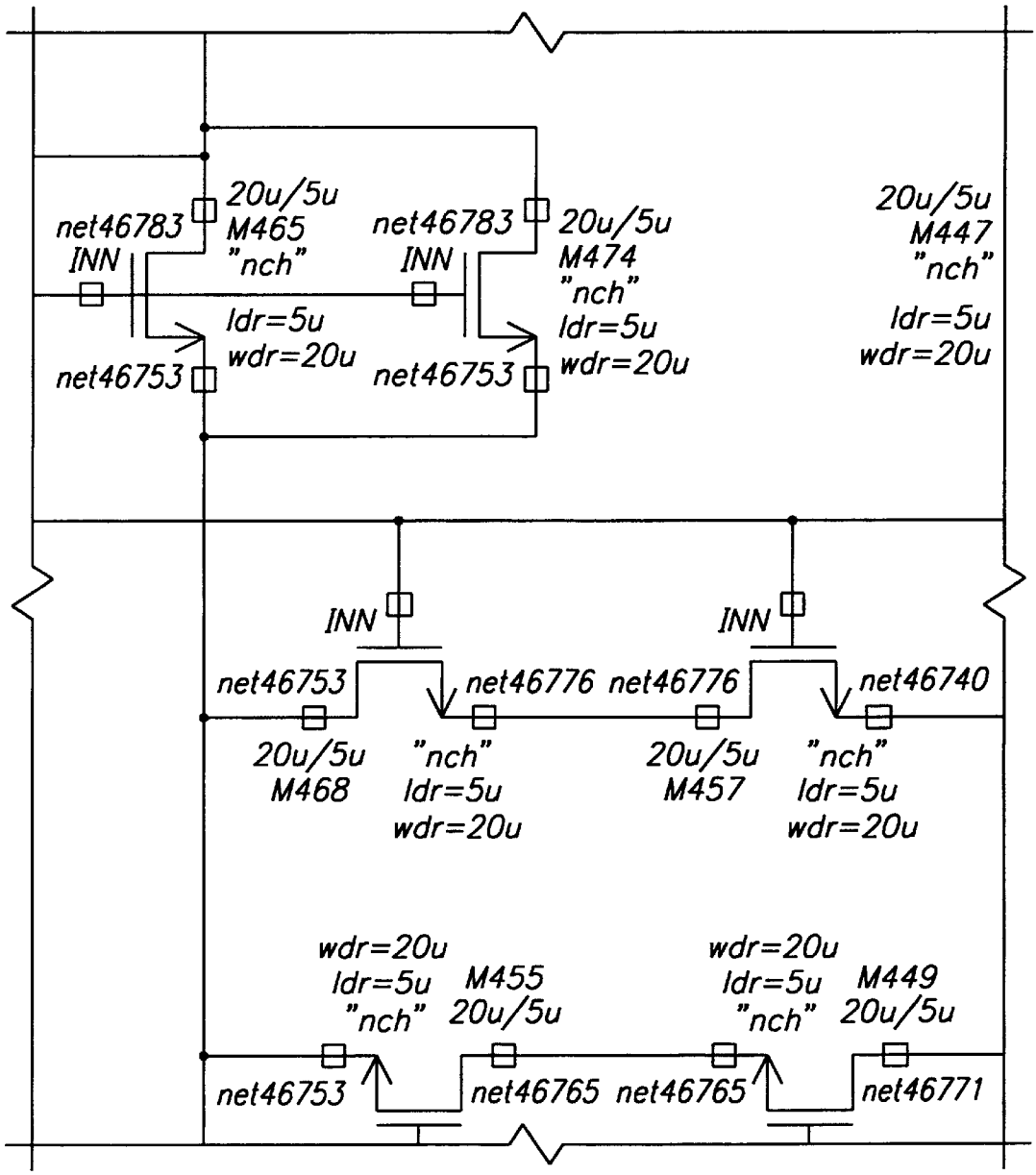
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Fig 8.0505CD

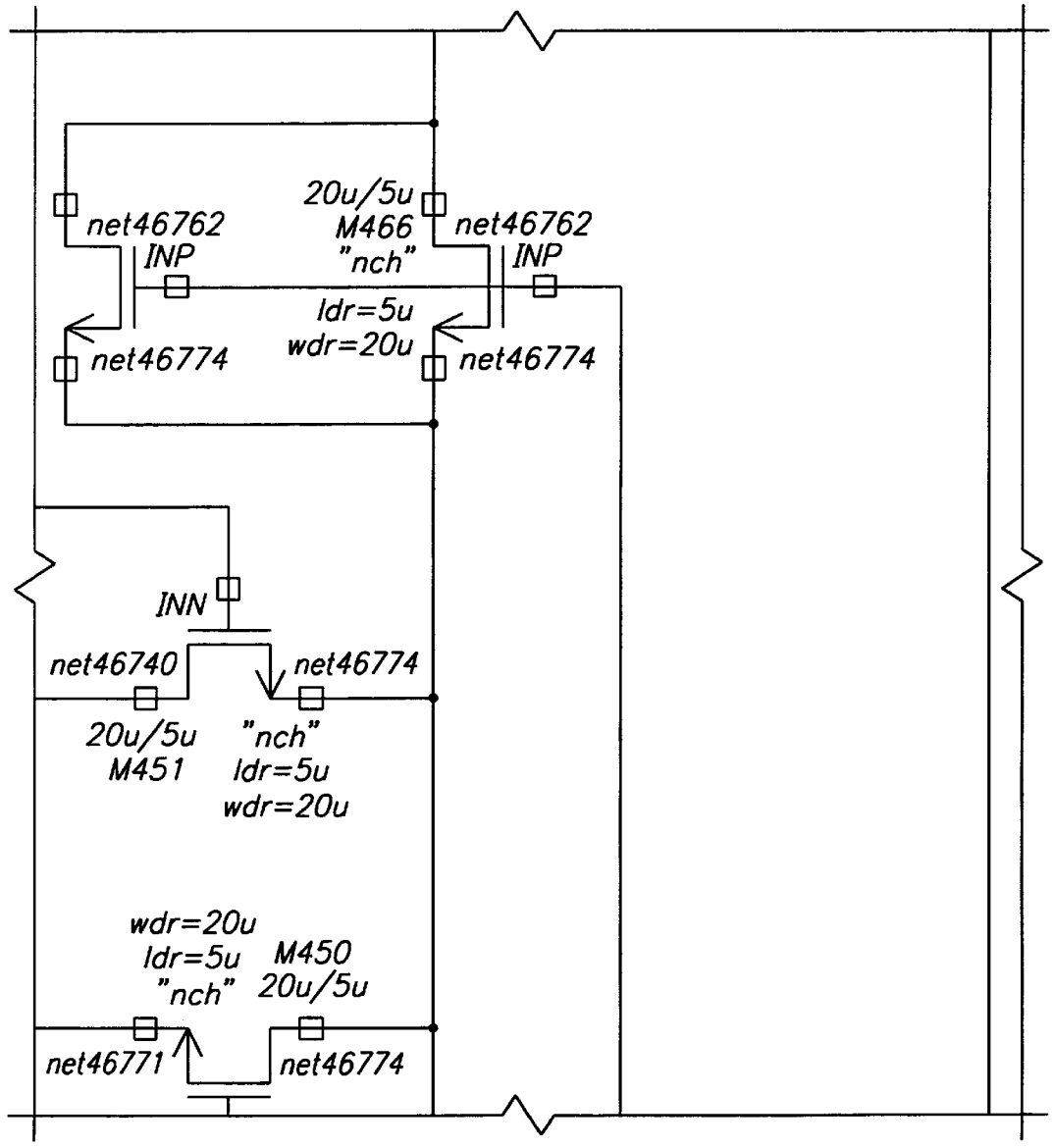
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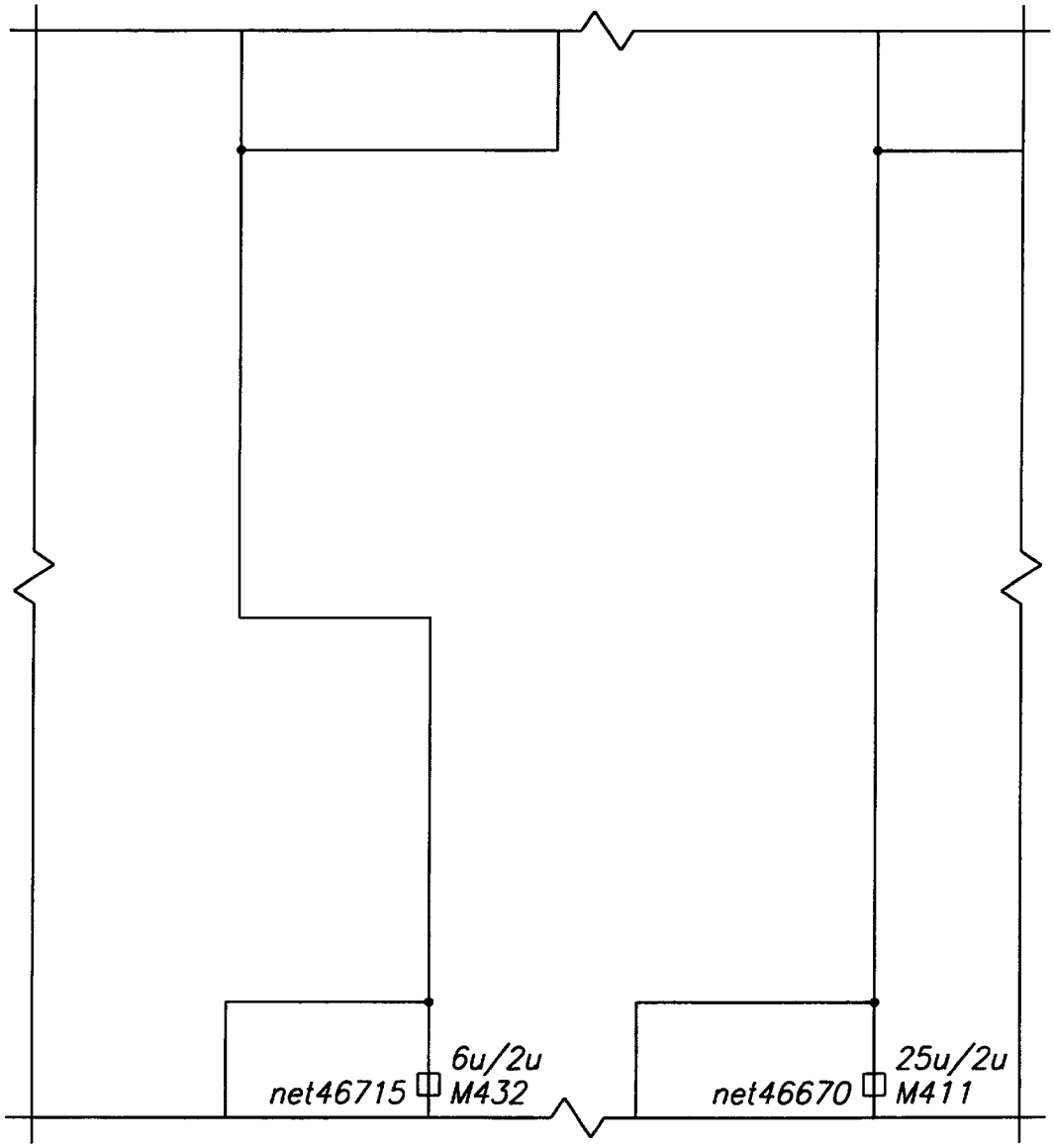
Fig 8.0505CE



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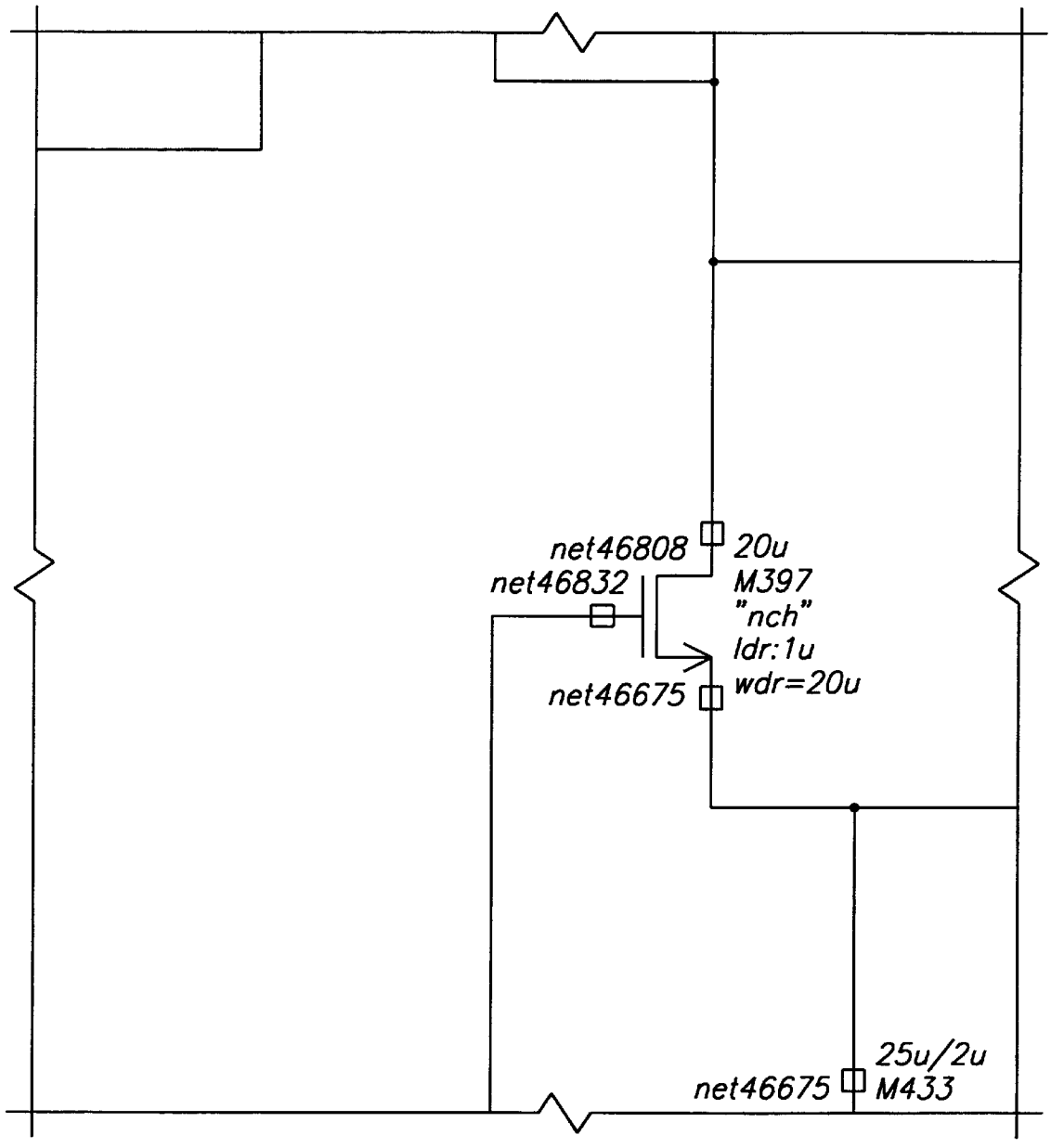
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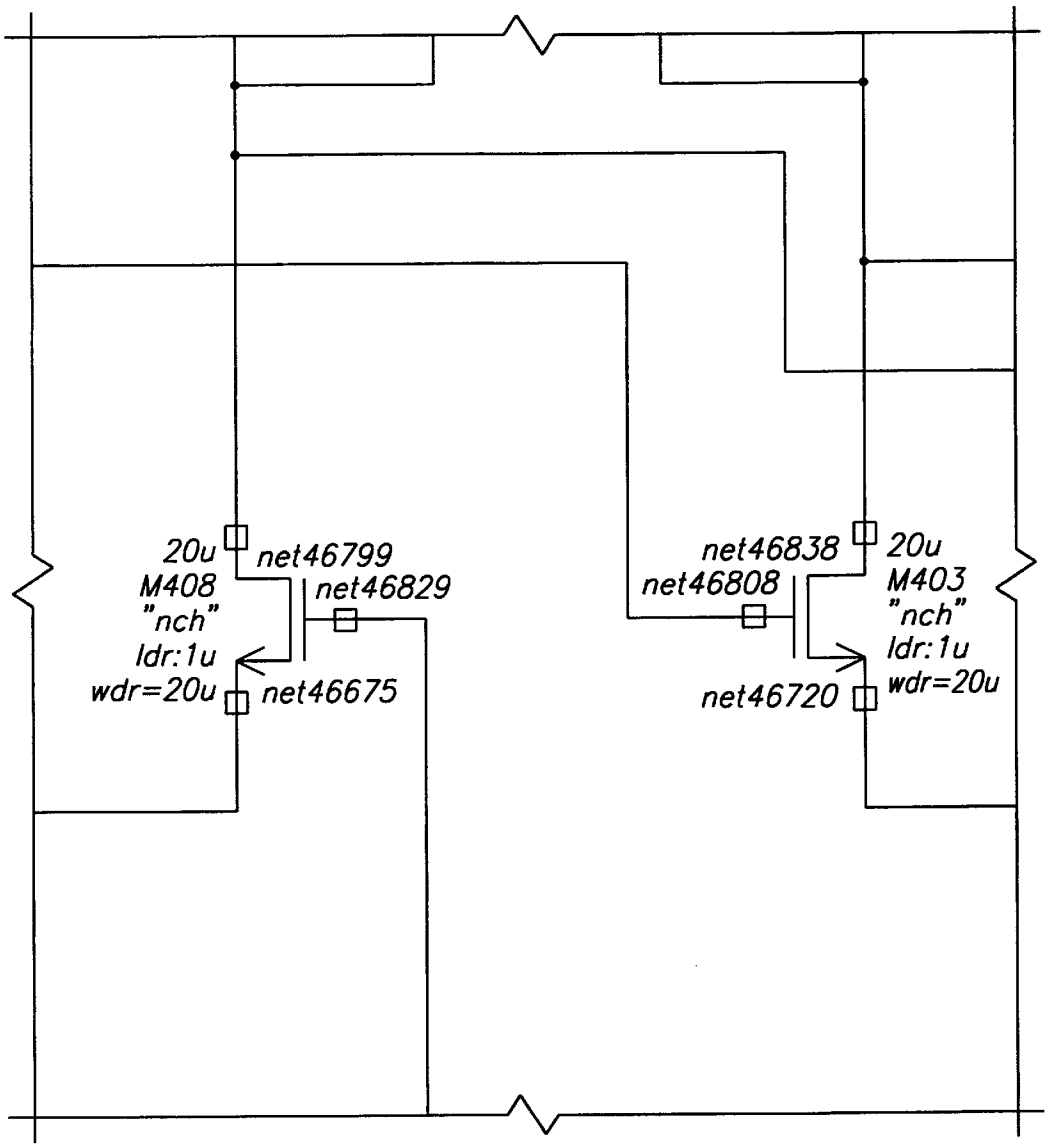
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Fig 8.0505CH

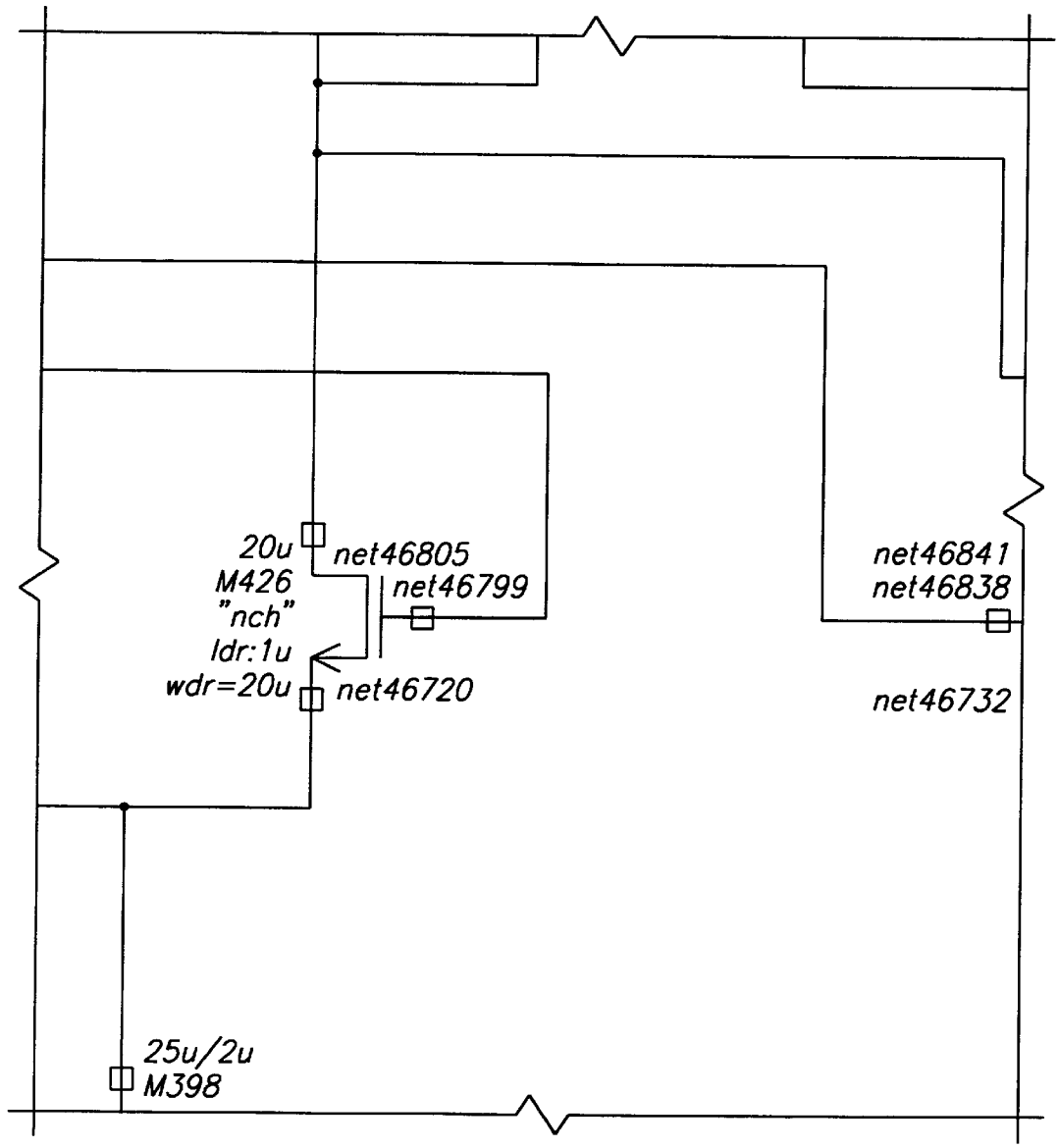
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Fig 8.0505CI

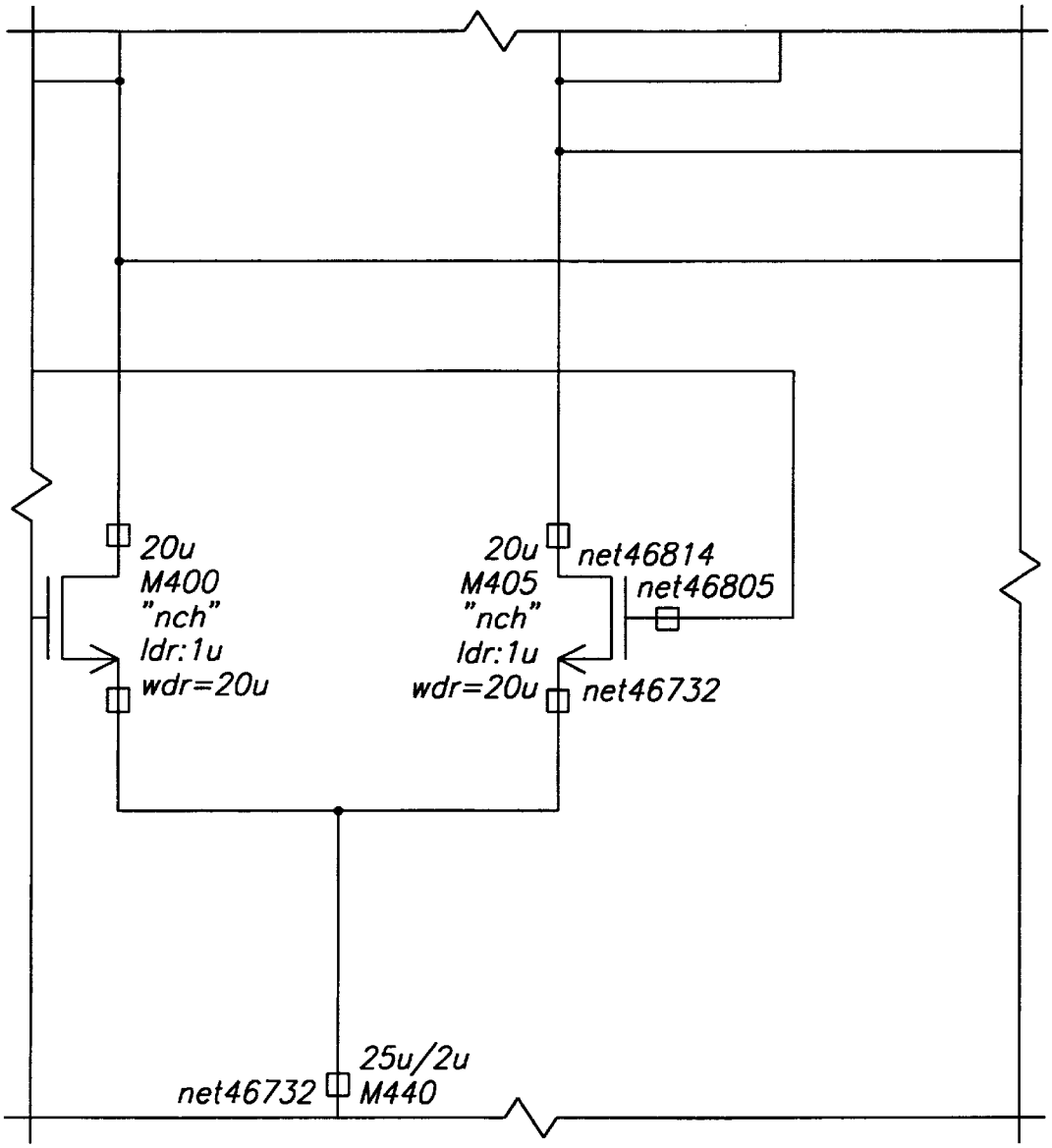
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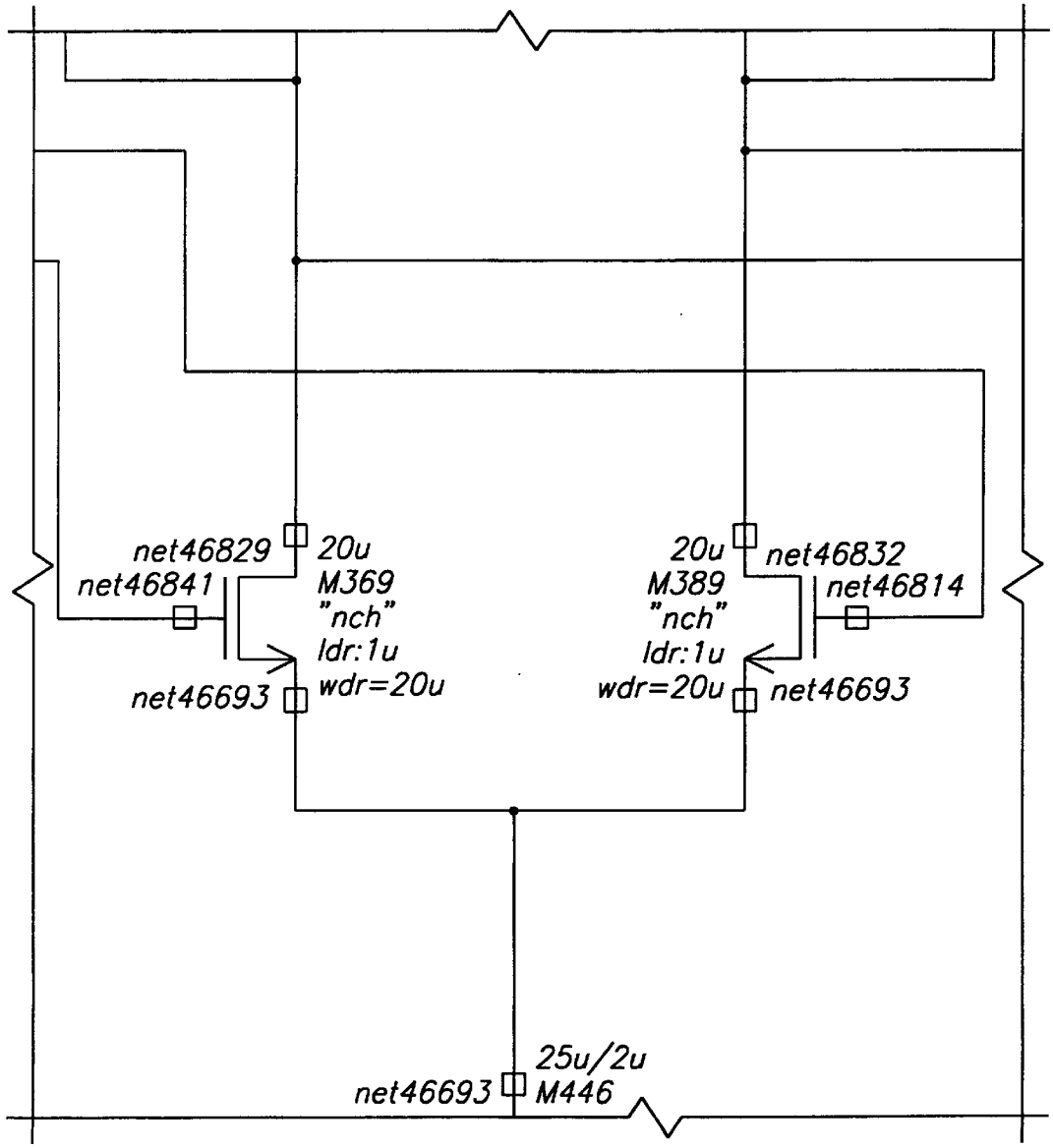
Fig 8.0505(a)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20u
M389
"nch"
ldr:1u
wdr=20u
net46832
net46814
net46693
25u/2u
M446
net46693

FIG 8,050,CK

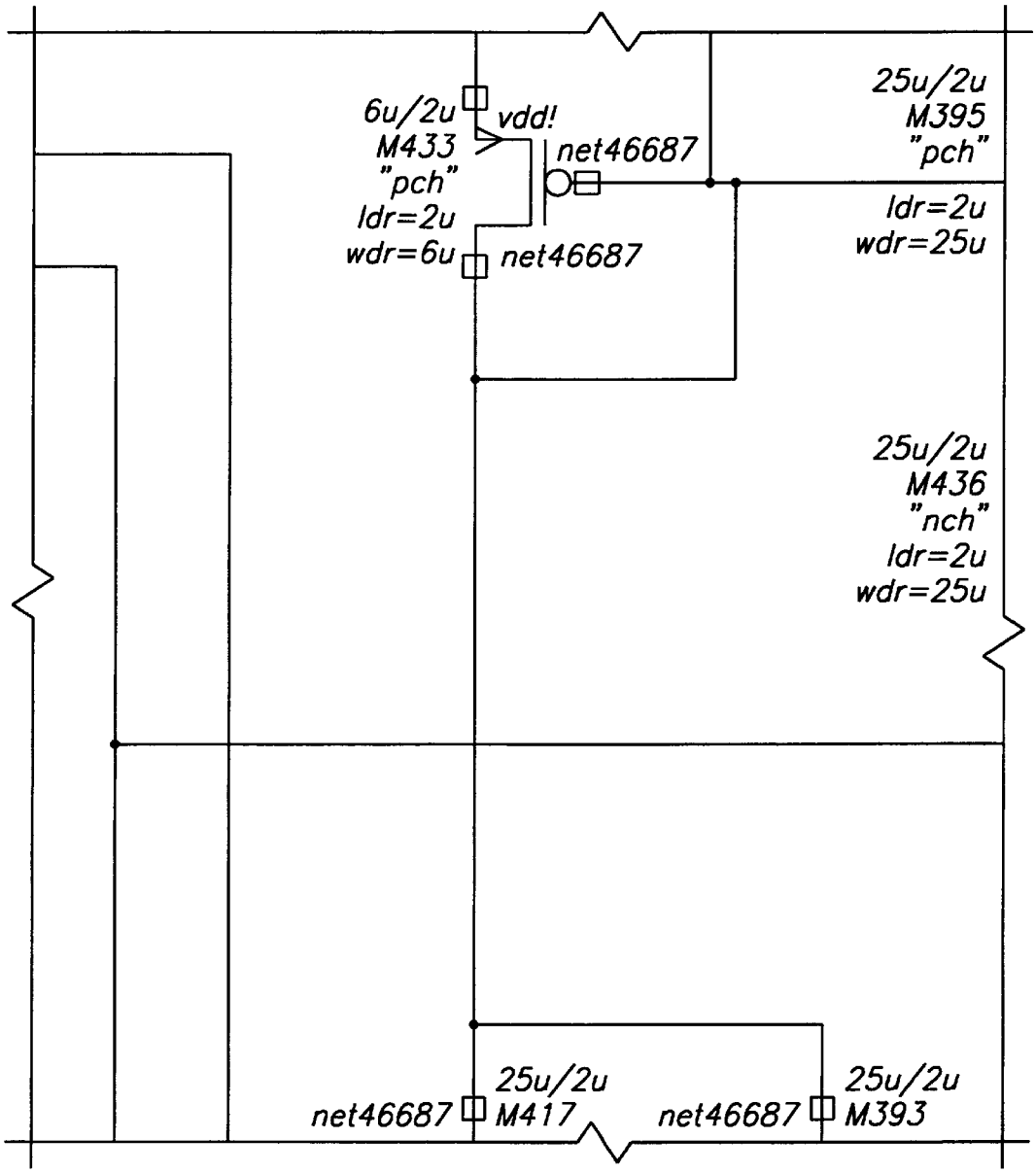

6u/2u
M433
"pch"
ldr=2u
wdr=6u
vdd!
net46687
net46687
25u/2u
M395
"pch"
ldr=2u
wdr=25u
25u/2u
M436
"nch"
ldr=2u
wdr=25u
net46687
25u/2u
M417
net46687
25u/2u
M393

Fig 8.0505CL

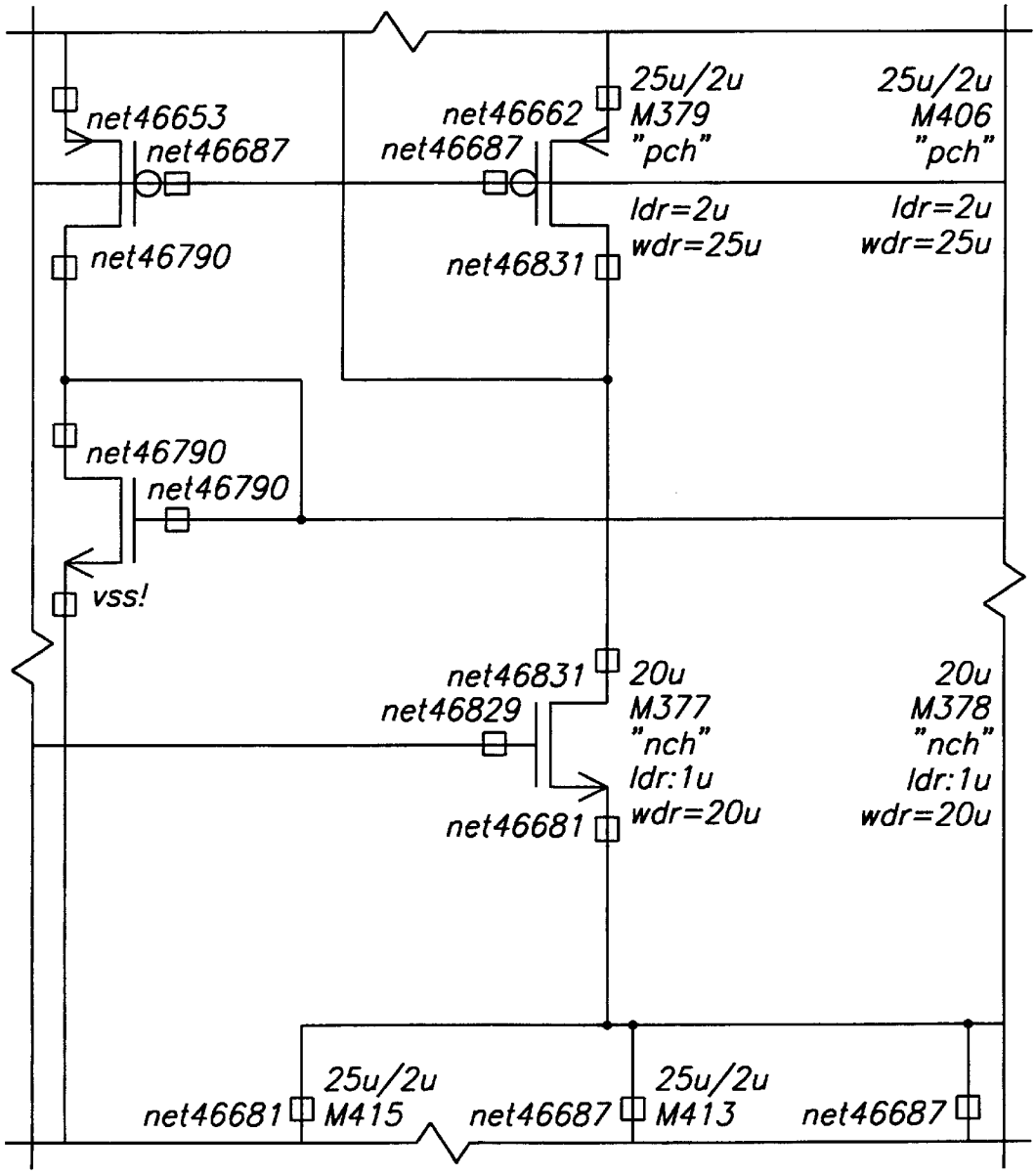

net46653
net46687
net46790
net46662
net46687
net46831
25u/2u
M379
"pch"
ldr=2u
wdr=25u
25u/2u
M406
"pch"
ldr=2u
wdr=25u
net46790
net46790
vss!
net46831
net46829
net46681
20u
M377
"nch"
ldr:1u
wdr=20u
20u
M378
"nch"
ldr:1u
wdr=20u
net46681
25u/2u
M415
net46687
25u/2u
M413
net46687

Fig 8.0505CM

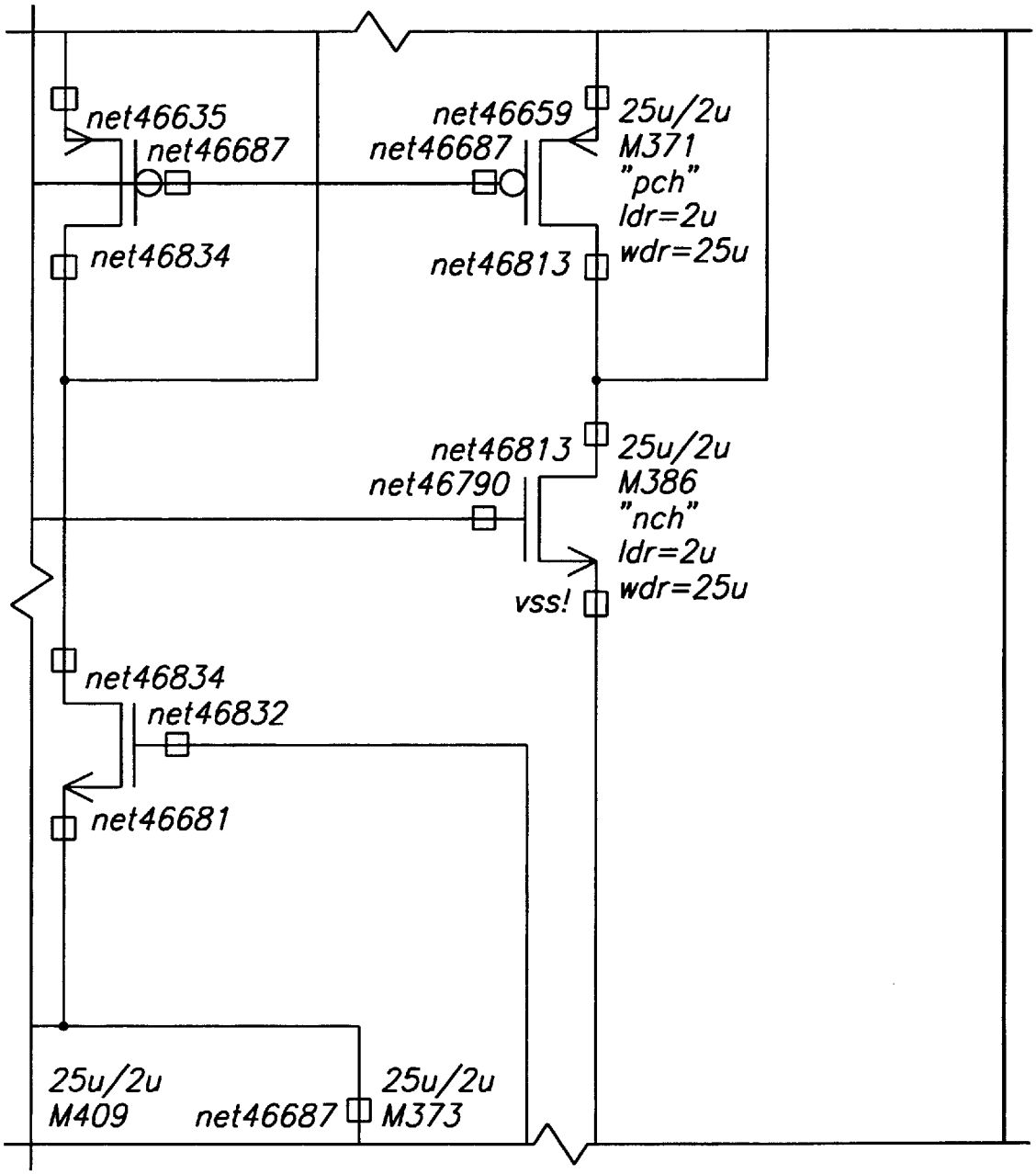

net46635
net46687
net46834
net46659
net46687
net46813
25u/2u
M371
"pch"
ldr=2u
wdr=25u
net46813
net46790
vss!
25u/2u
M386
"nch"
ldr=2u
wdr=25u
net46834
net46832
net46681
25u/2u
M409
net46687
25u/2u
M373

FIG 8.0505CN

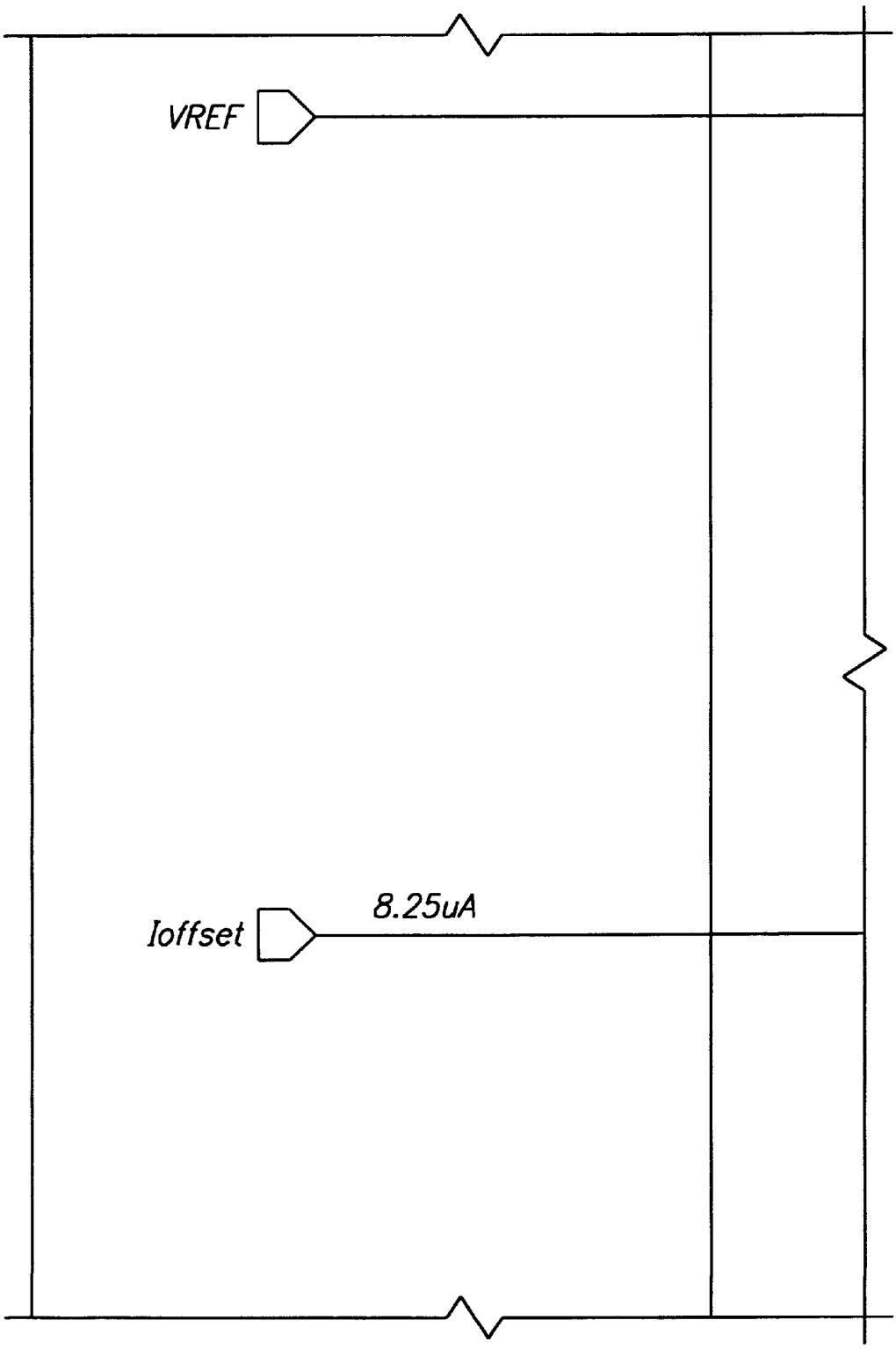


Fig 8.0505DA

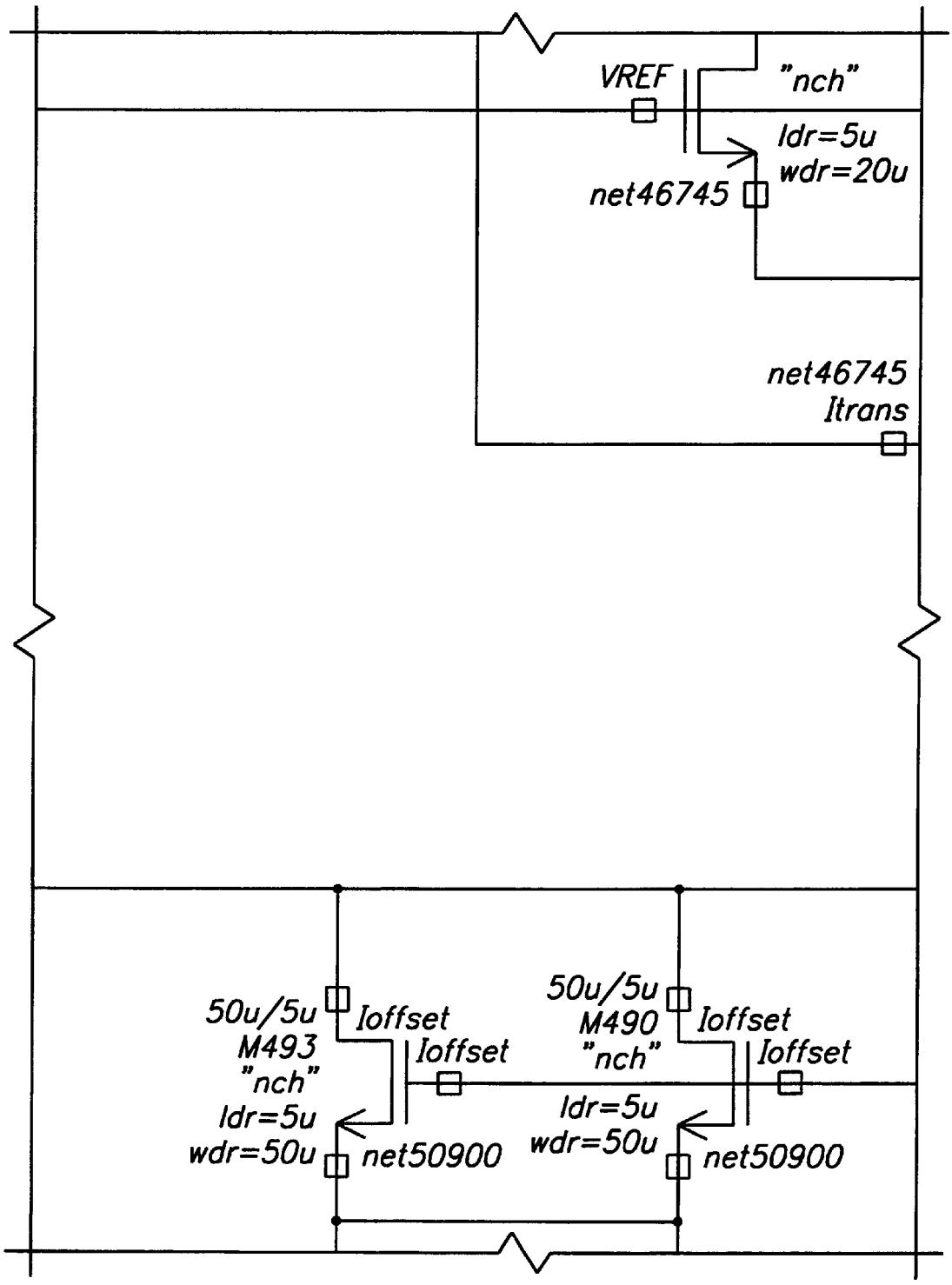

VREF
"nch"
ldr=5u
wdr=20u
net46745
net46745
Itrans
50u/5u
M493
"nch"
ldr=5u
wdr=50u
Ioffset
Ioffset
net50900
50u/5u
M490
"nch"
ldr=5u
wdr=50u
Ioffset
Ioffset
net50900

FIG 8.0505DB

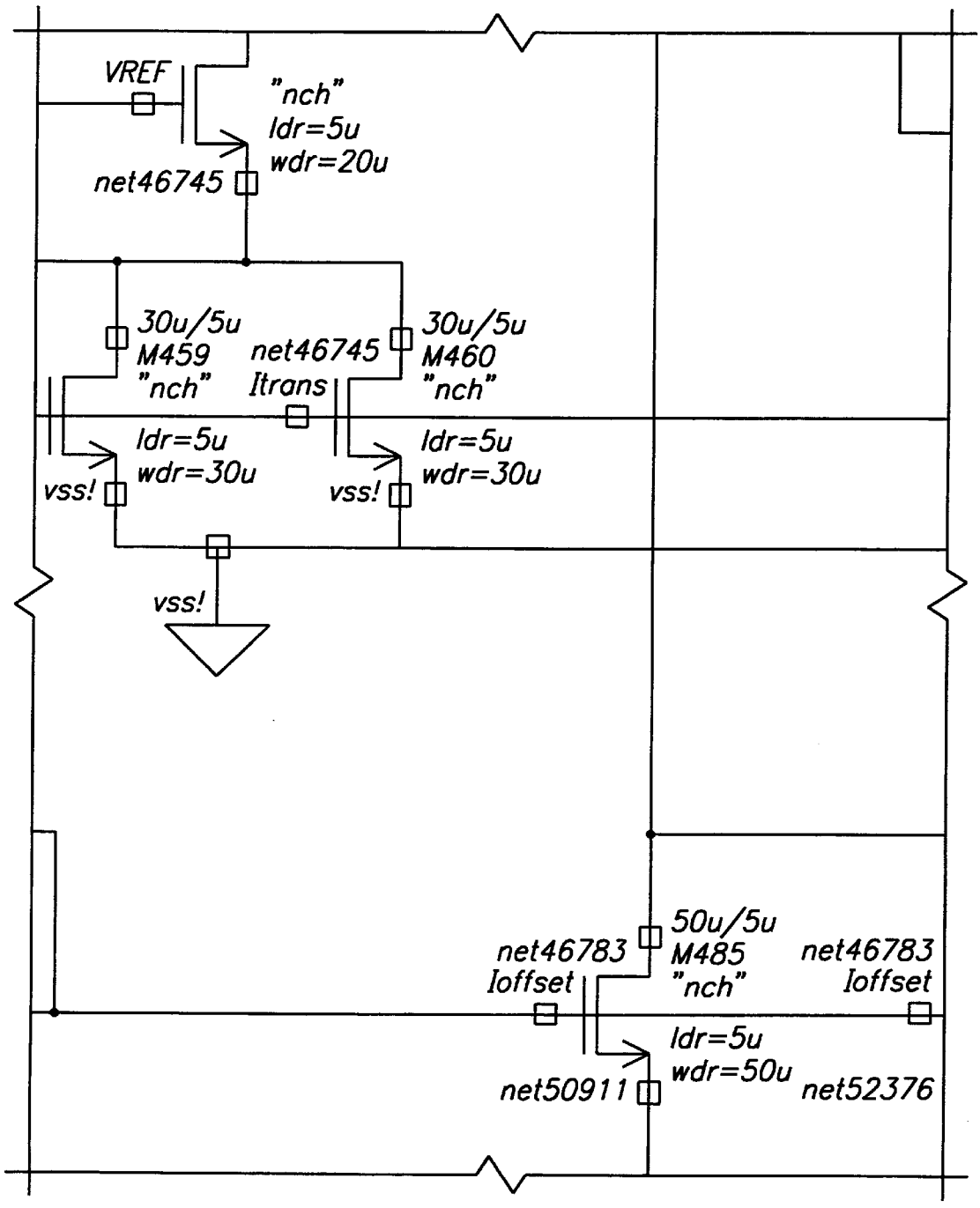


Fig 8.005005C

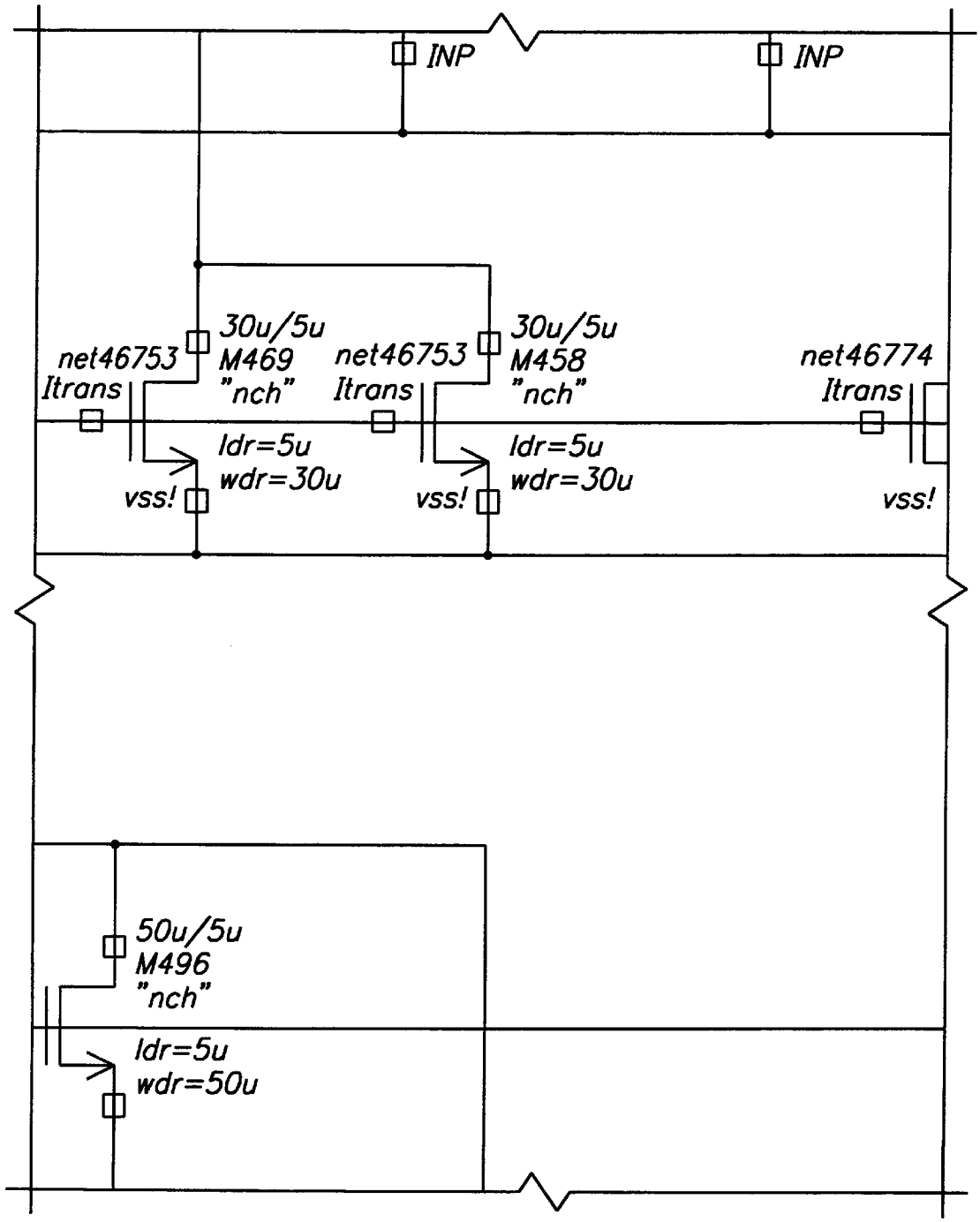


Fig 8.005005D

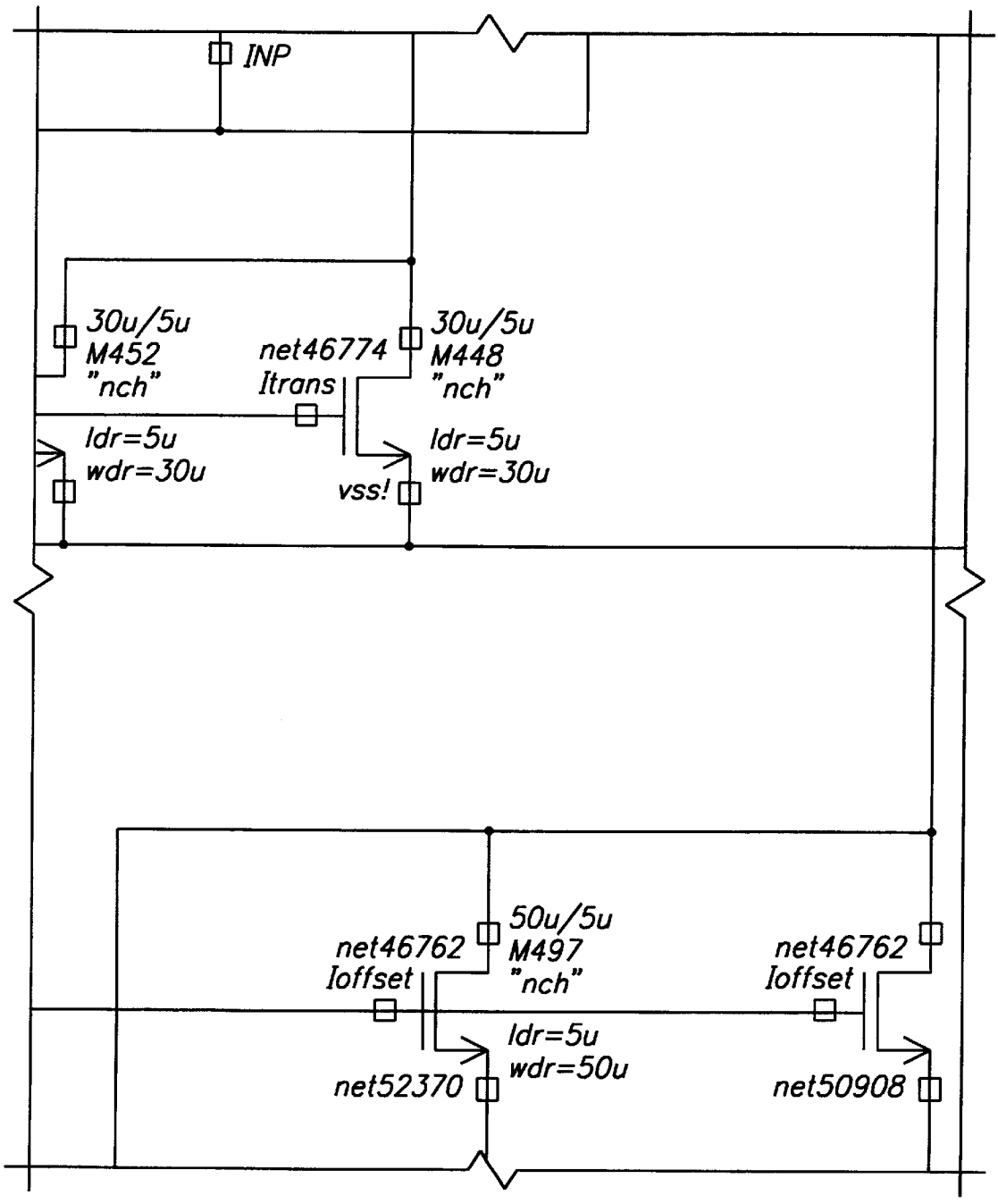

INP
30u/5u
M452
"nch"
net46774
Itrans
30u/5u
M448
"nch"
ldr=5u
wdr=30u
vss!
ldr=5u
wdr=30u
50u/5u
M497
"nch"
net46762
Ioffset
ldr=5u
wdr=50u
net52370
net46762
Ioffset
net50908

Fig 8.0505DE

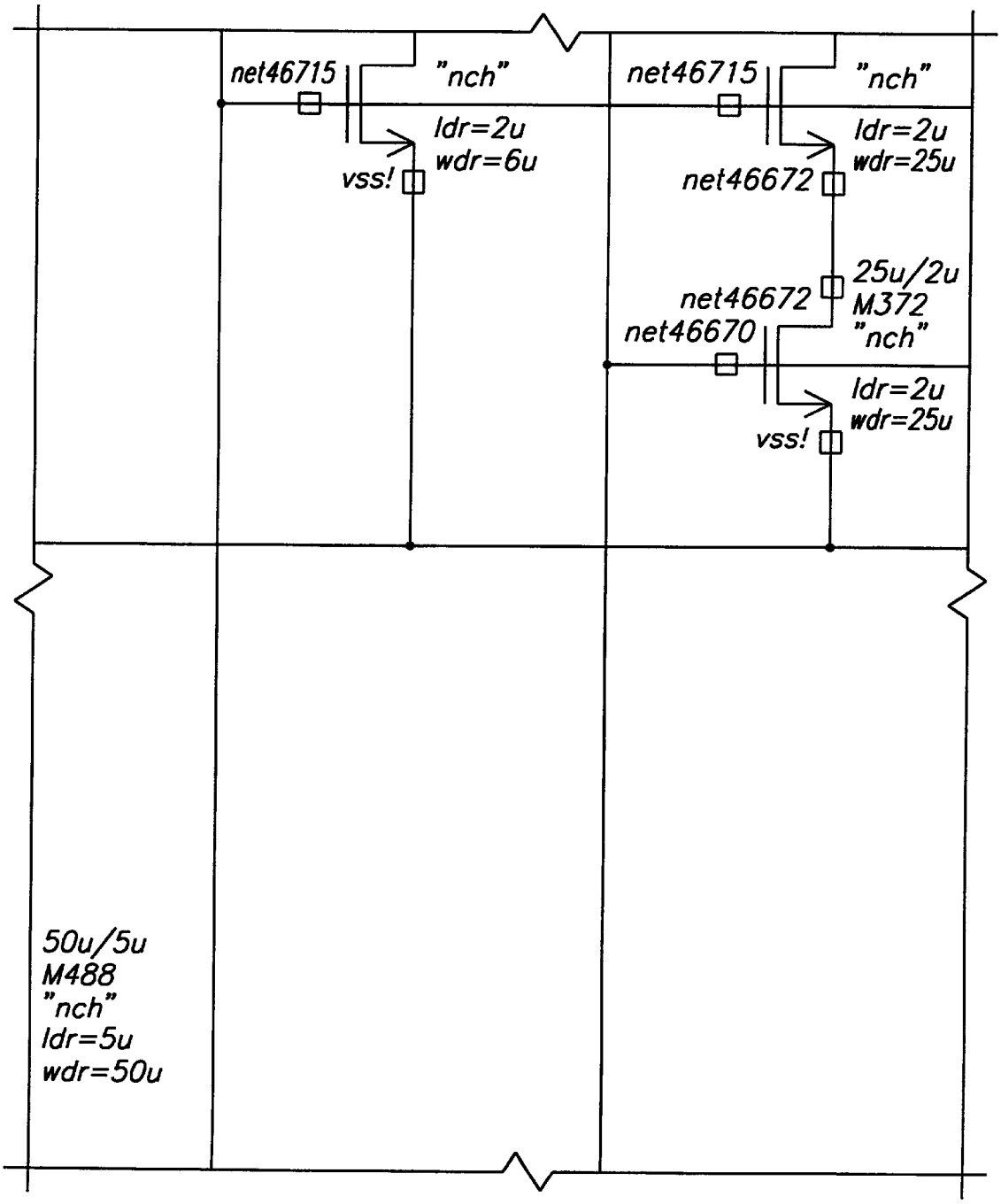

net46715
"nch"
ldr=2u
wdr=6u
vss!
net46715
"nch"
ldr=2u
wdr=25u
net46672
25u/2u
M372
"nch"
net46672
net46670
ldr=2u
wdr=25u
vss!
50u/5u
M488
"nch"
ldr=5u
wdr=50u

Fig 8.0505DF

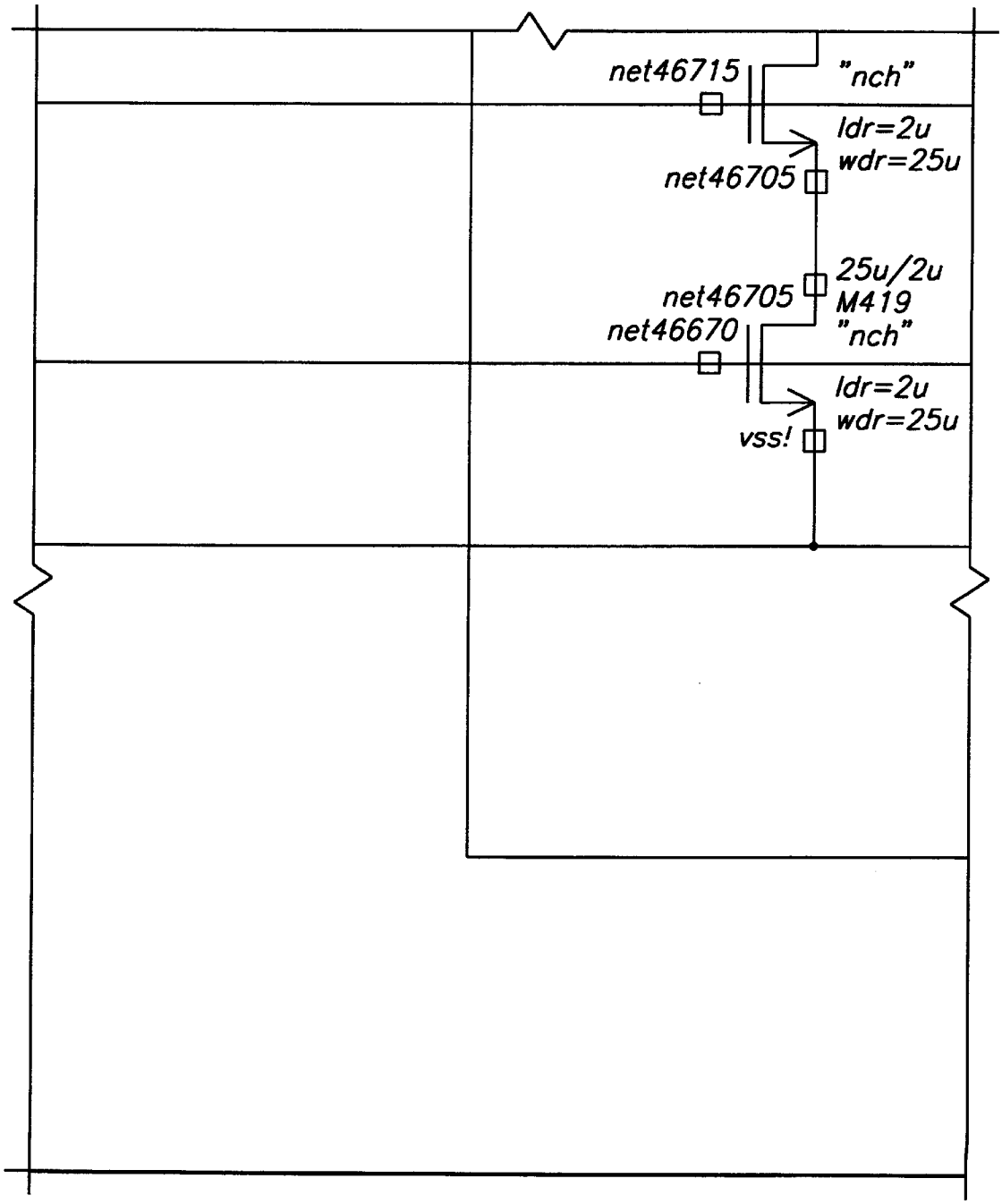

net46715
"nch"
ldr=2u
wdr=25u
net46705
25u/2u
M419
"nch"
net46705
net46670
ldr=2u
wdr=25u
vss!

Fig 8.0505D6

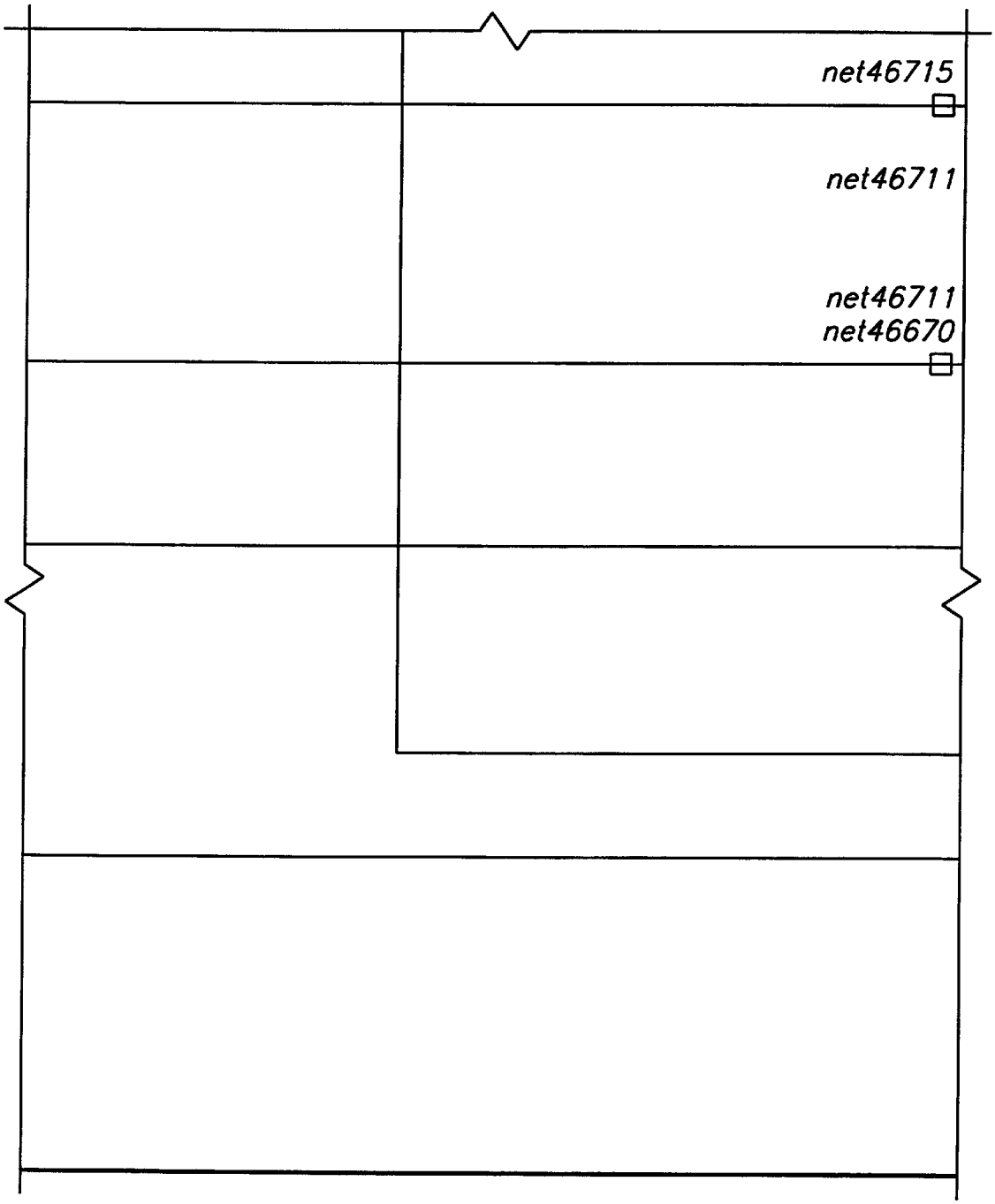


Fig 8.0505DH

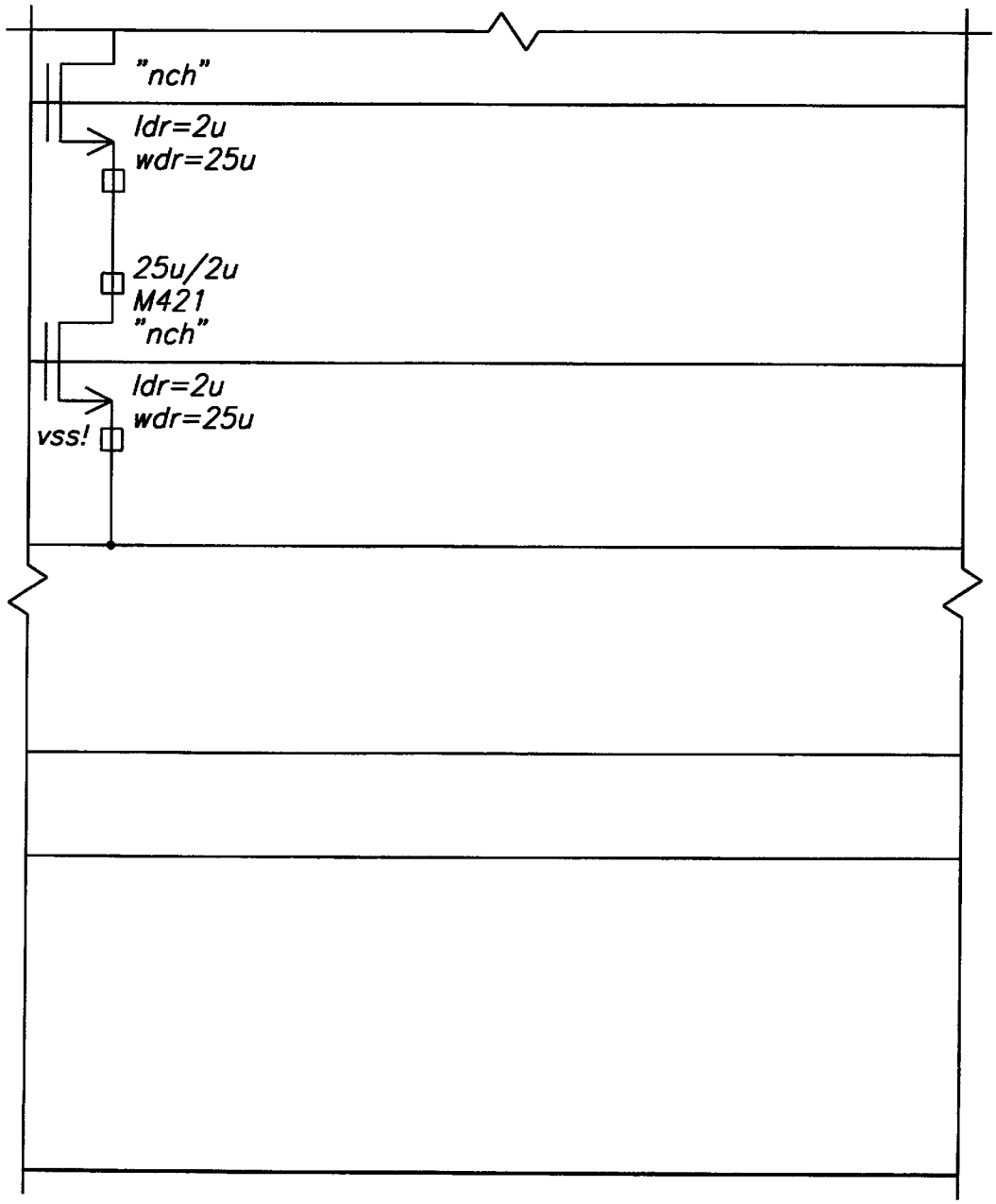


Fig 8.0505D1

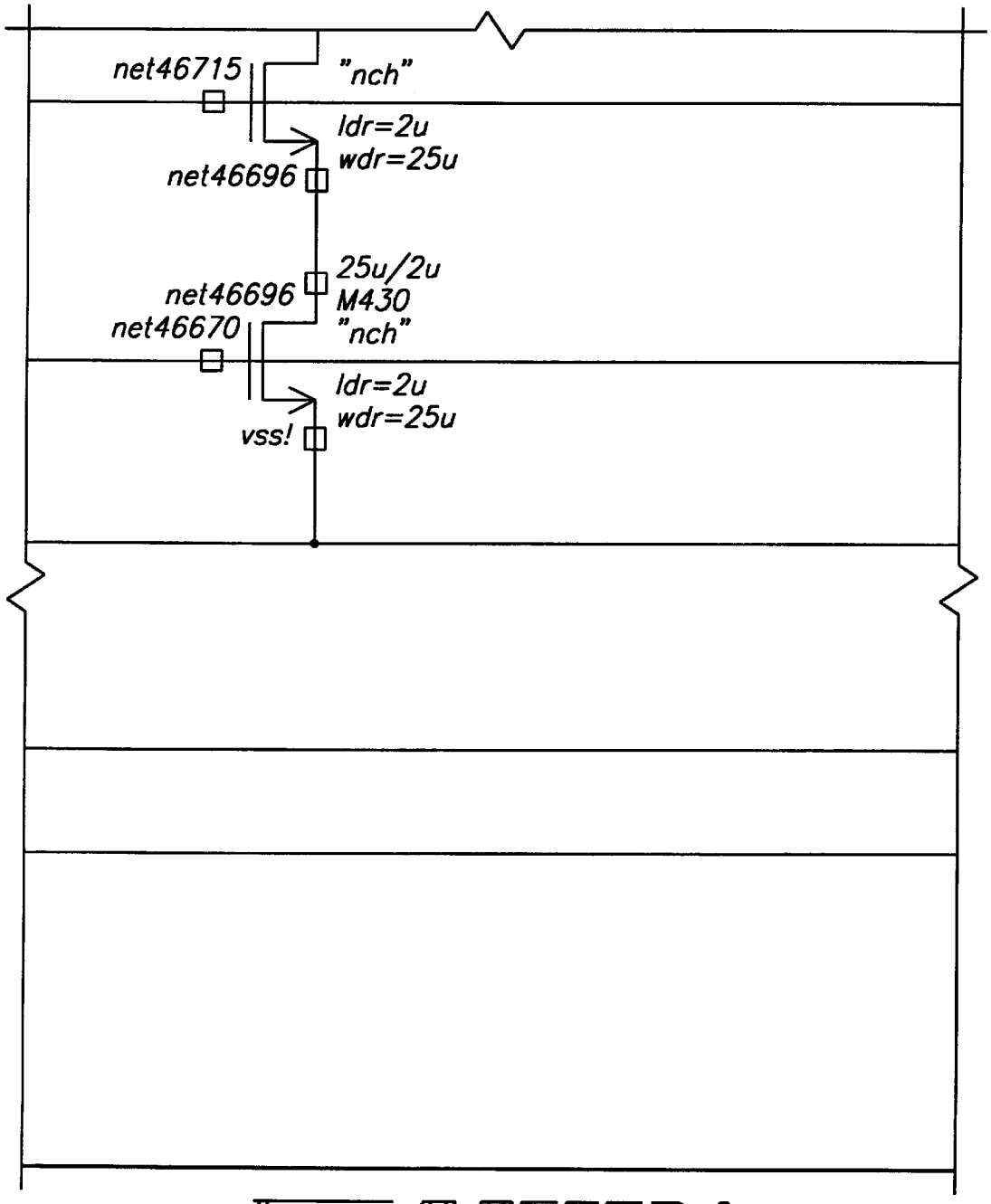

net46715
"nch"
ldr=2u
wdr=25u
net46696
25u/2u
M430
net46696
"nch"
net46670
ldr=2u
wdr=25u
vss!

Fig 8.0505Dd

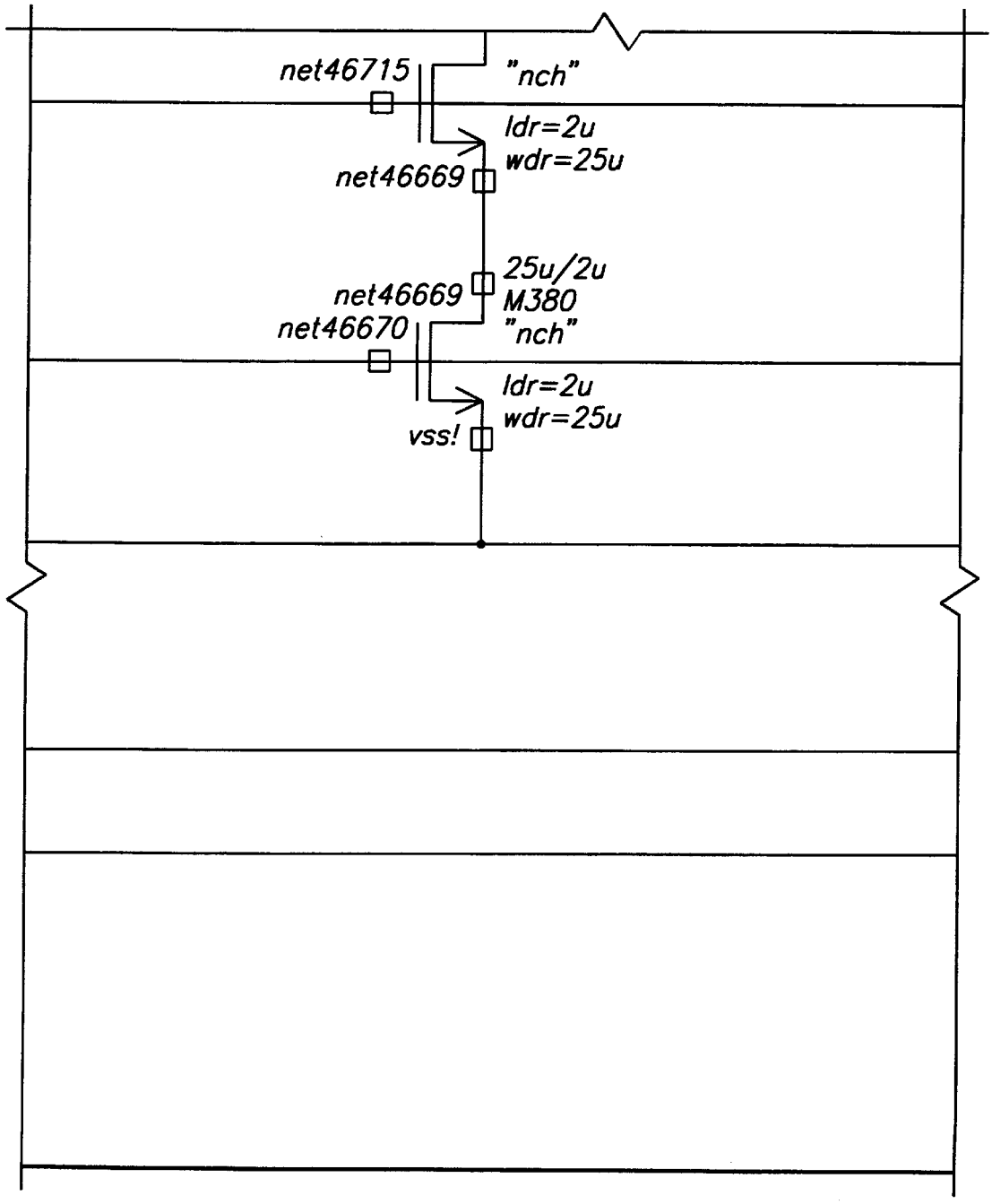

net46715
"nch"
ldr=2u
wdr=25u
net46669
25u/2u
M380
net46669
net46670
"nch"
ldr=2u
wdr=25u
vss!

Fig 8.0505DK

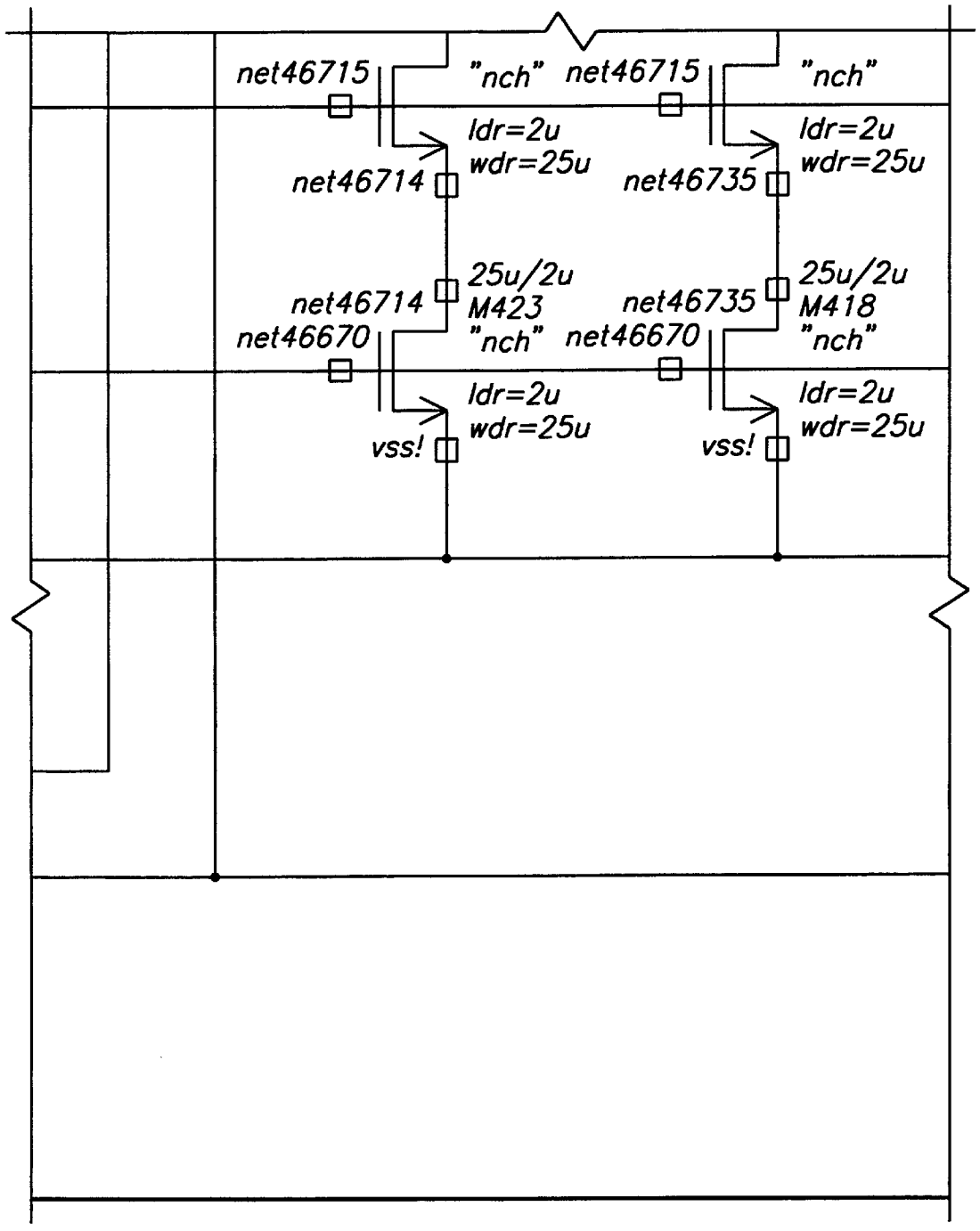

net46715
"nch"
net46715
"nch"
ldr=2u
wdr=25u
net46714
net46735
ldr=2u
wdr=25u
25u/2u
M423
"nch"
net46714
net46670
net46735
net46670
25u/2u
M418
"nch"
ldr=2u
wdr=25u
vss!
ldr=2u
wdr=25u
vss!

Fig 8.0505DL

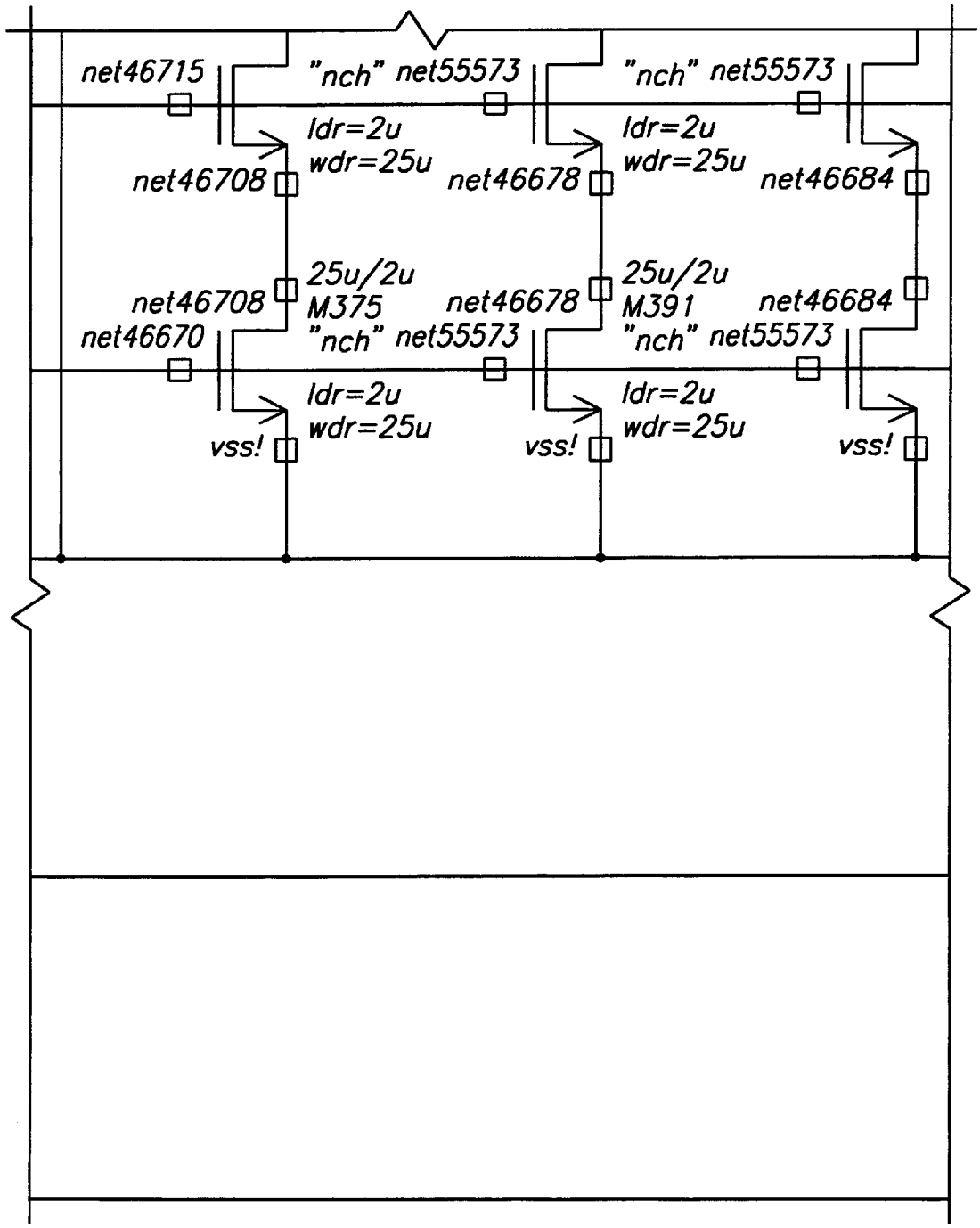

net46715
"nch" net55573
"nch" net55573
ldr=2u
wdr=25u
ldr=2u
wdr=25u
net46708
net46678
net46684
25u/2u
M375
25u/2u
M391
net46708
net46678
net46684
net46670
"nch" net55573
"nch" net55573
ldr=2u
wdr=25u
ldr=2u
wdr=25u
vss!
vss!
vss!

Fig 8.0505DM

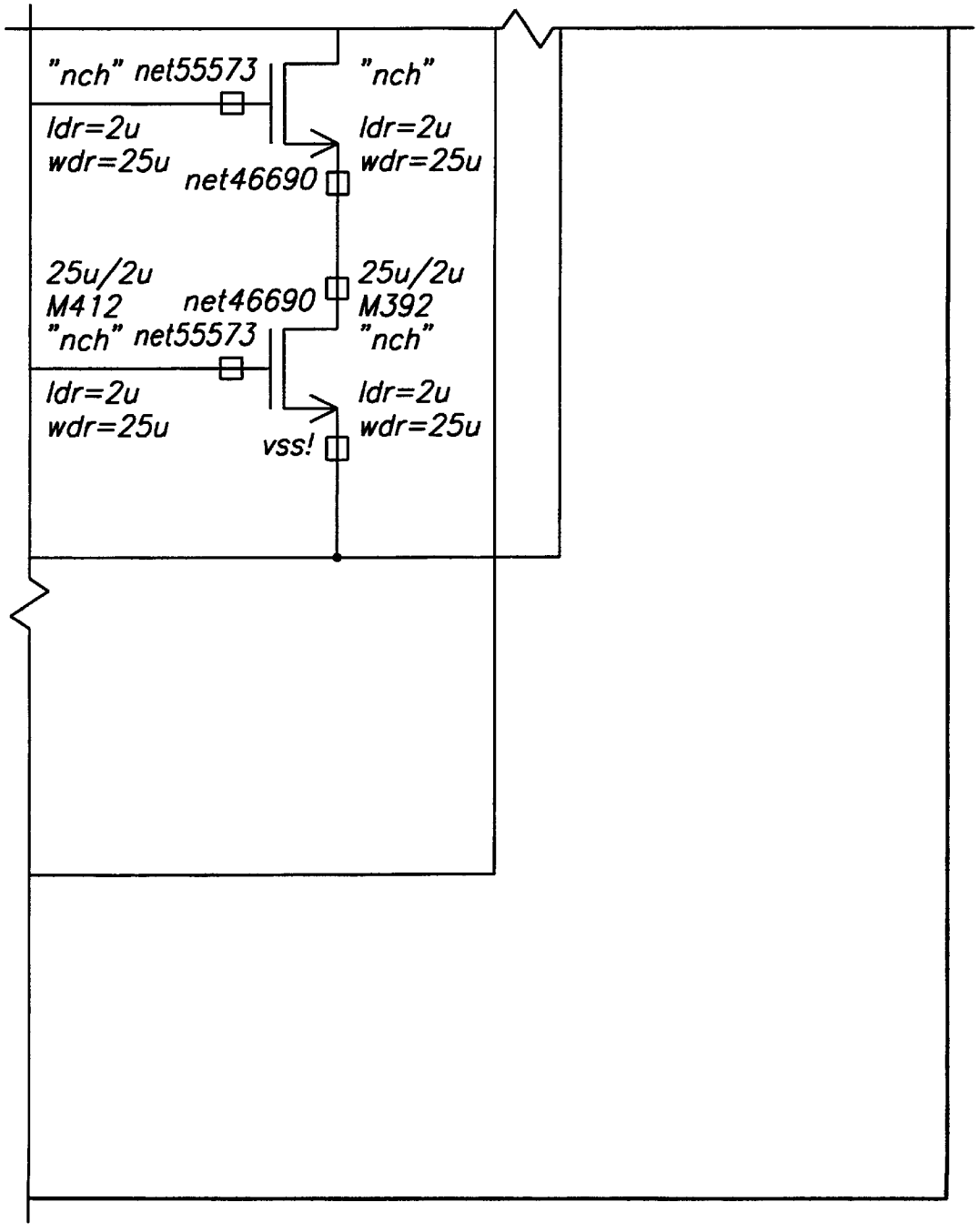

"nch" net55573
ldr=2u
wdr=25u
net46690
"nch"
ldr=2u
wdr=25u
25u/2u
M412
"nch" net55573
ldr=2u
wdr=25u
net46690
25u/2u
M392
"nch"
ldr=2u
wdr=25u
vss!

FIG 8.0505DN

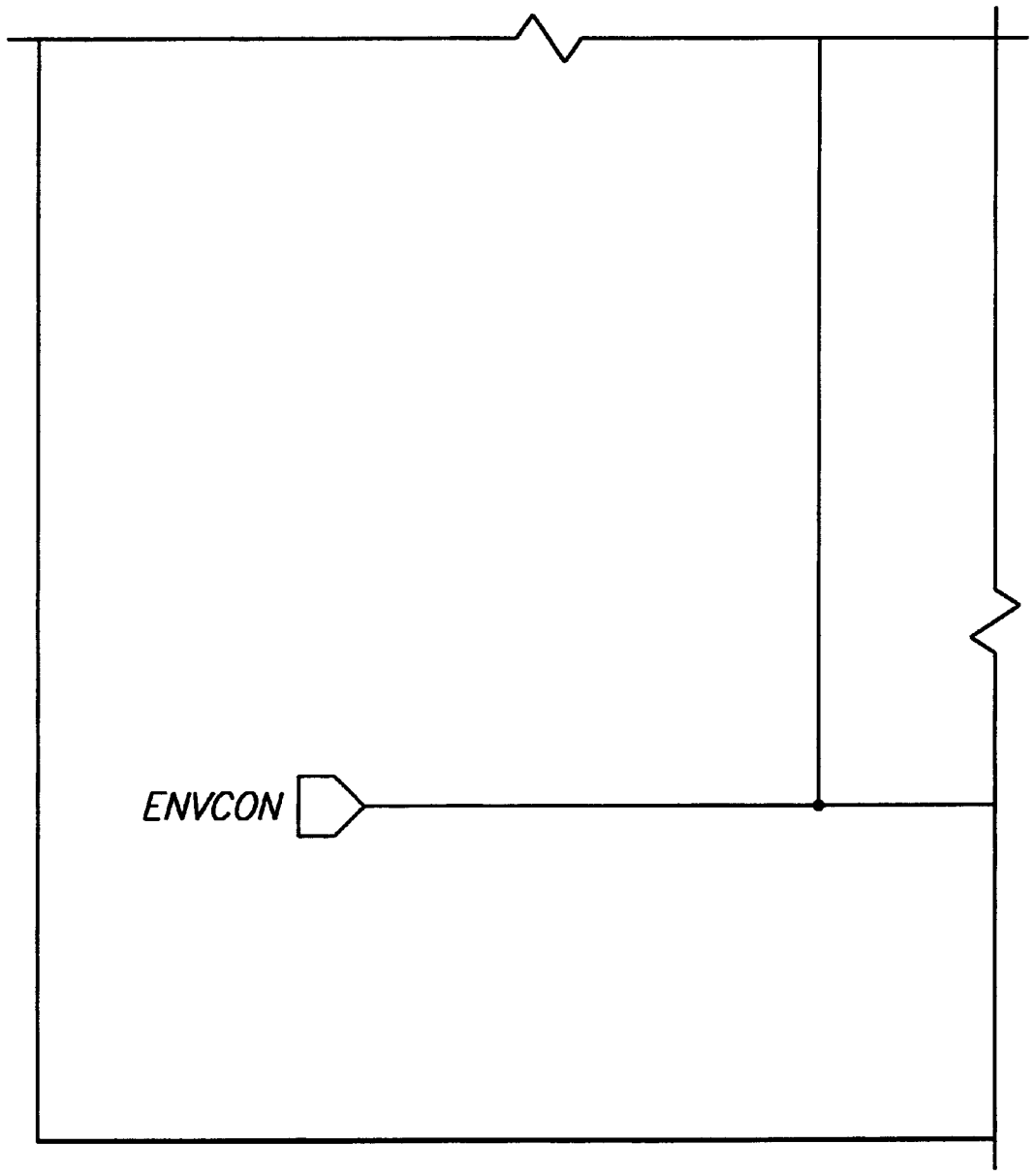


Fig 8.0505EA

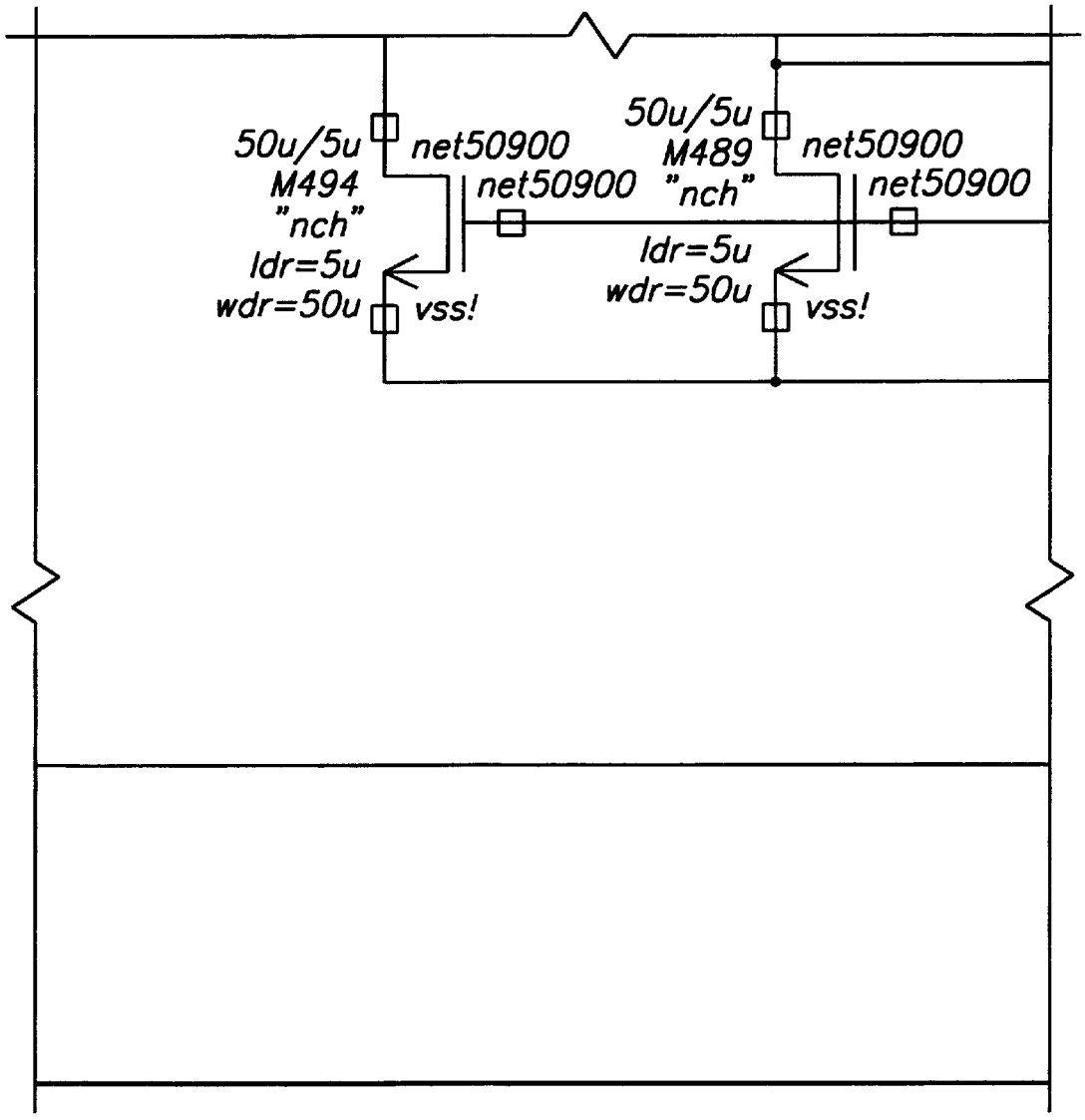

50u/5u
M494
"nch"
ldr=5u
wdr=50u
net50900
vss!
net50900
50u/5u
M489
"nch"
ldr=5u
wdr=50u
net50900
vss!
net50900

Fig 8.0505EB

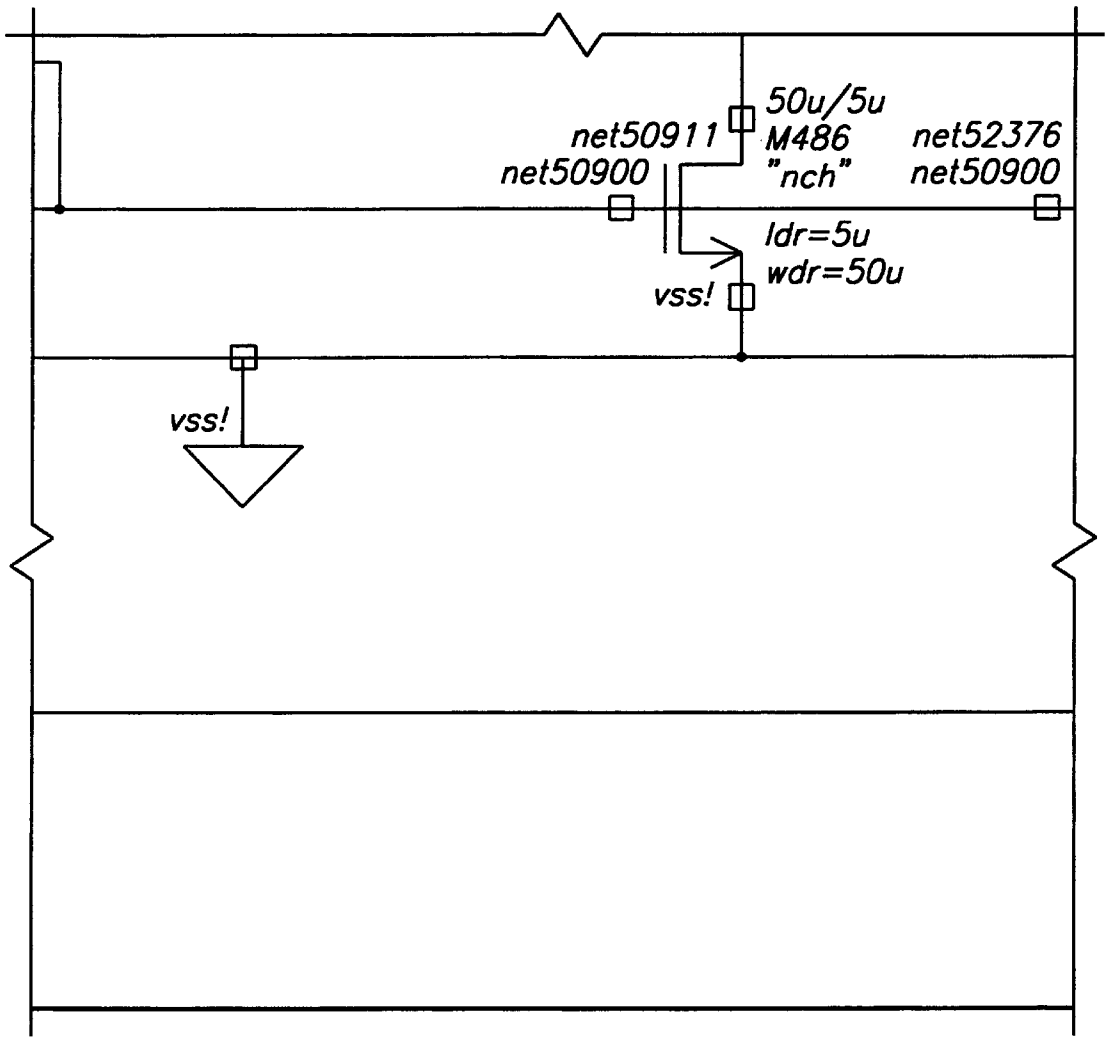

50u/5u
M486
"nch"
net50911
net50900
net52376
net50900
ldr=5u
wdr=50u
vss!
vss!

Fig 8.0505EC

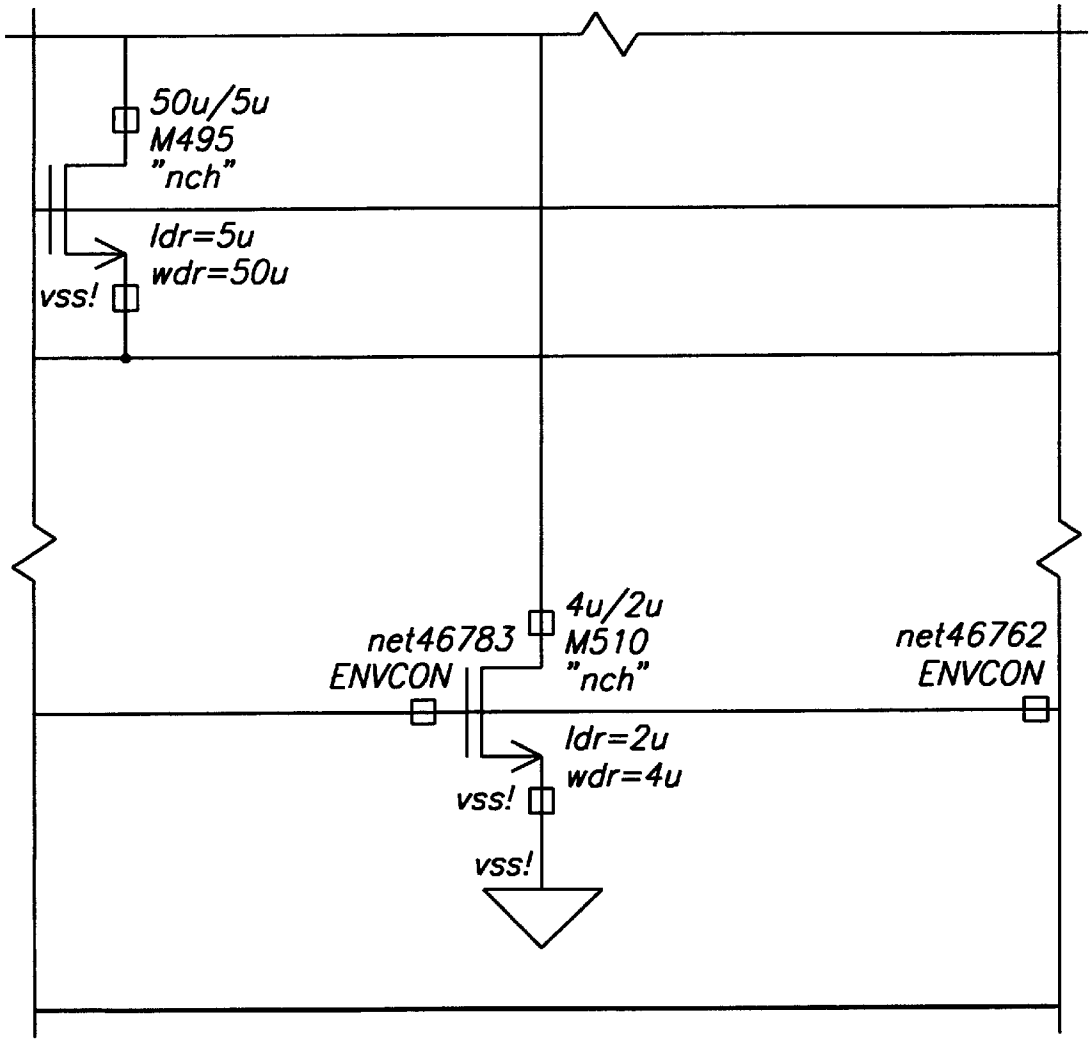

50u/5u
M495
"nch"
ldr=5u
wdr=50u
vss!
4u/2u
M510
"nch"
net46783
ENVCON
net46762
ENVCON
ldr=2u
wdr=4u
vss!
vss!

FIG 80505ED

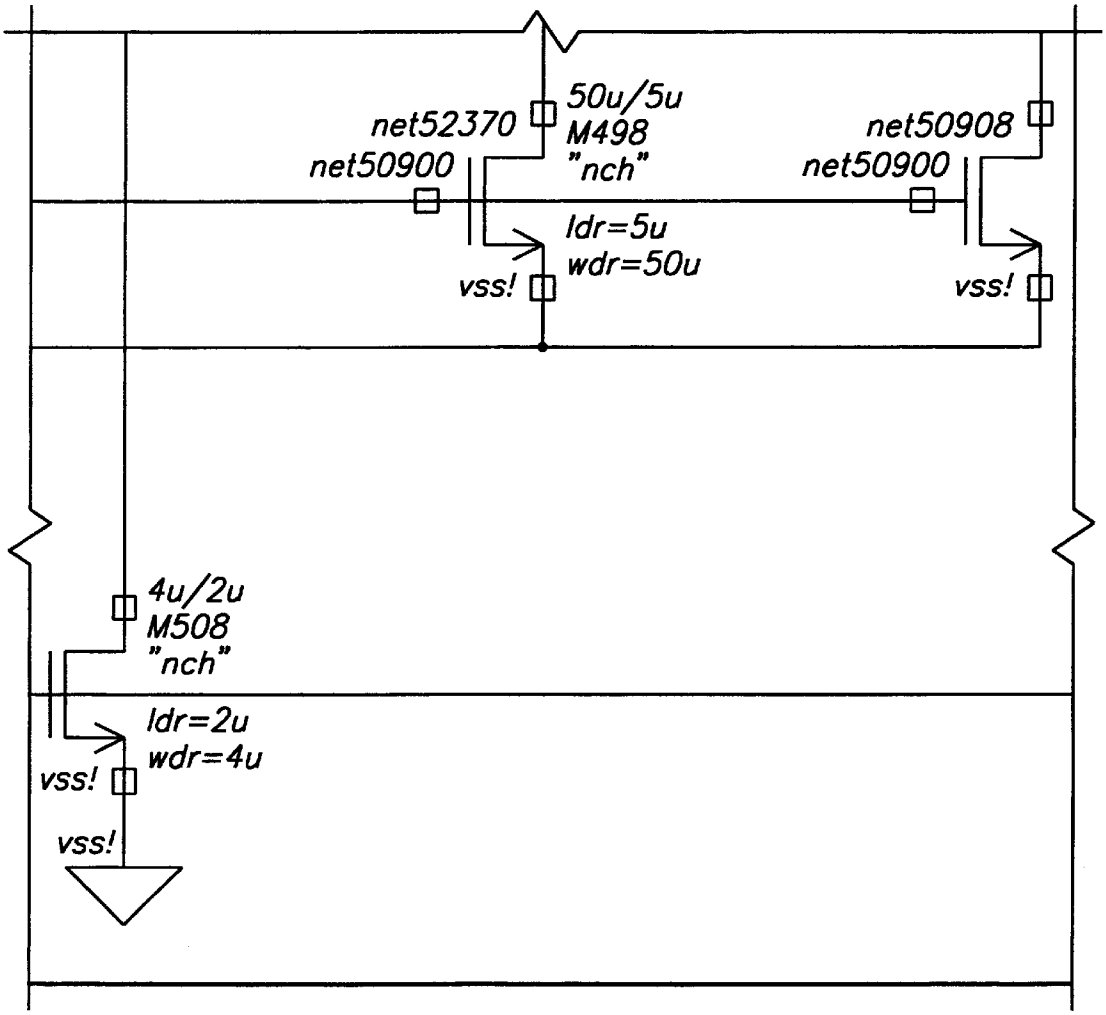

50u/5u
M498
"nch"
net52370
net50900
net50908
net50900
ldr=5u
wdr=50u
vss!
vss!
4u/2u
M508
"nch"
ldr=2u
wdr=4u
vss!
vss!

Fig 8.0505E

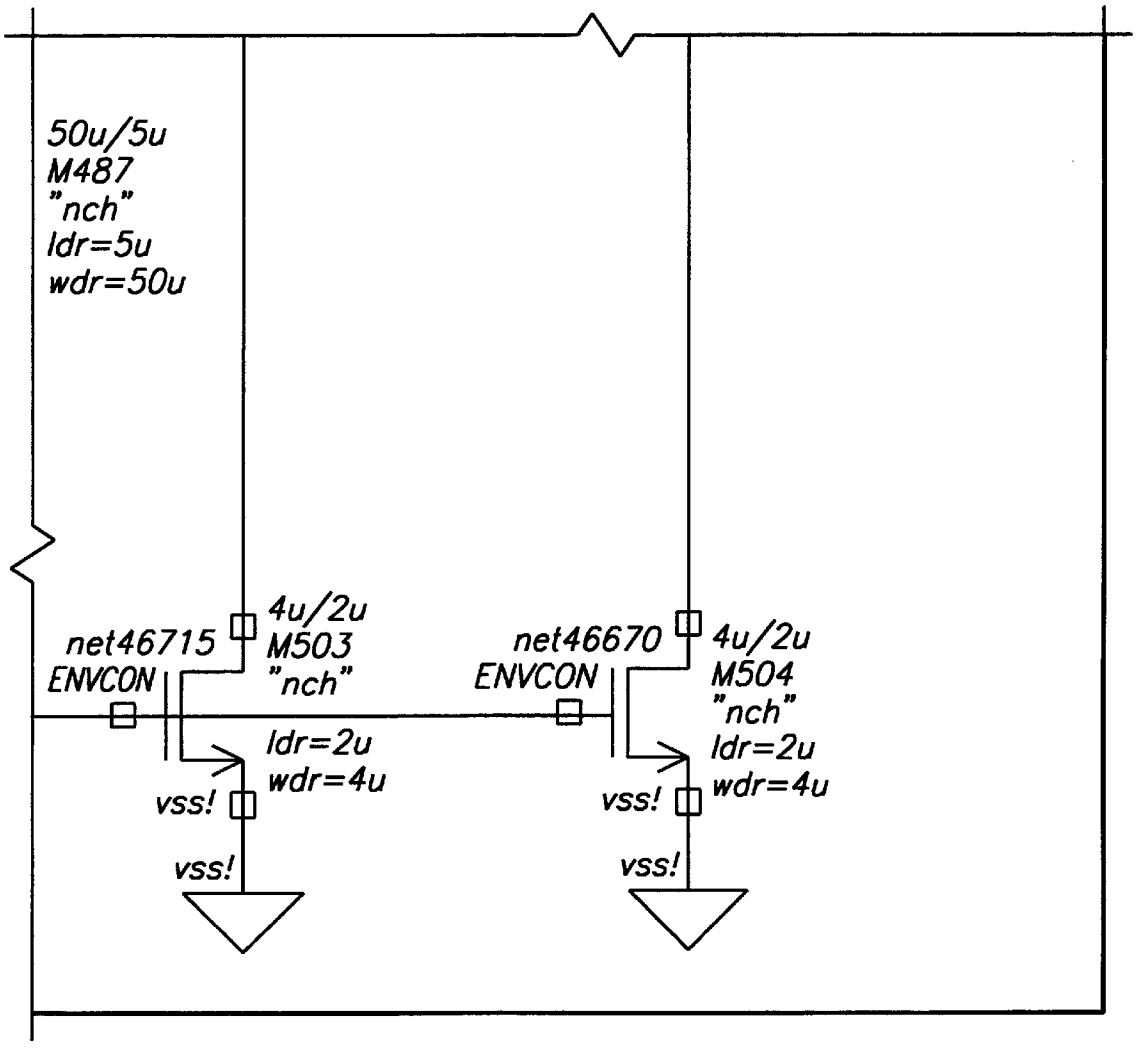

50u/5u
M487
"nch"
ldr=5u
wdr=50u
net46715
ENVCON
4u/2u
M503
"nch"
ldr=2u
wdr=4u
vss!
vss!
net46670
ENVCON
4u/2u
M504
"nch"
ldr=2u
wdr=4u
vss!
vss!

Fig 8.0505EF

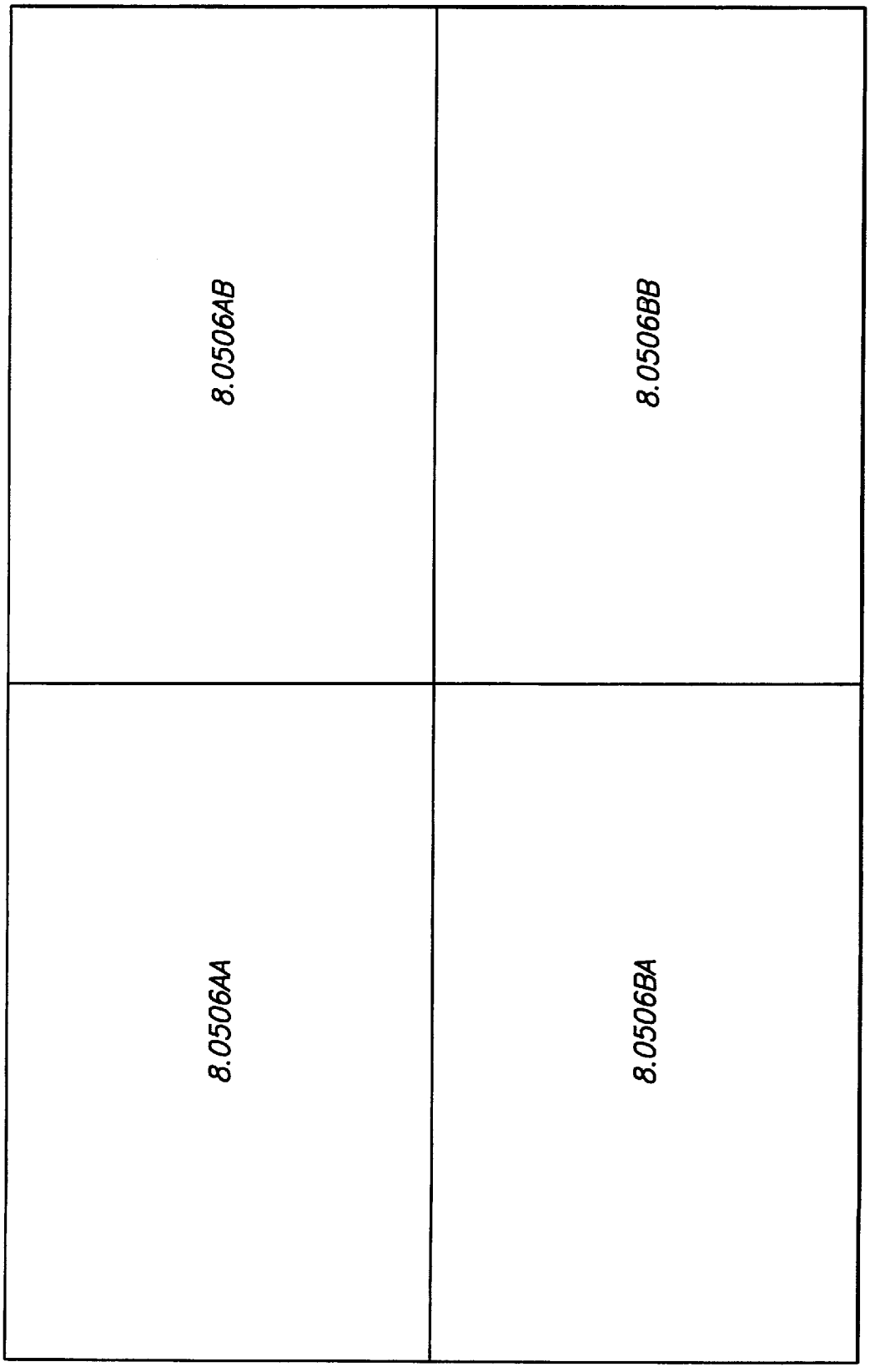


FIG 8.0506

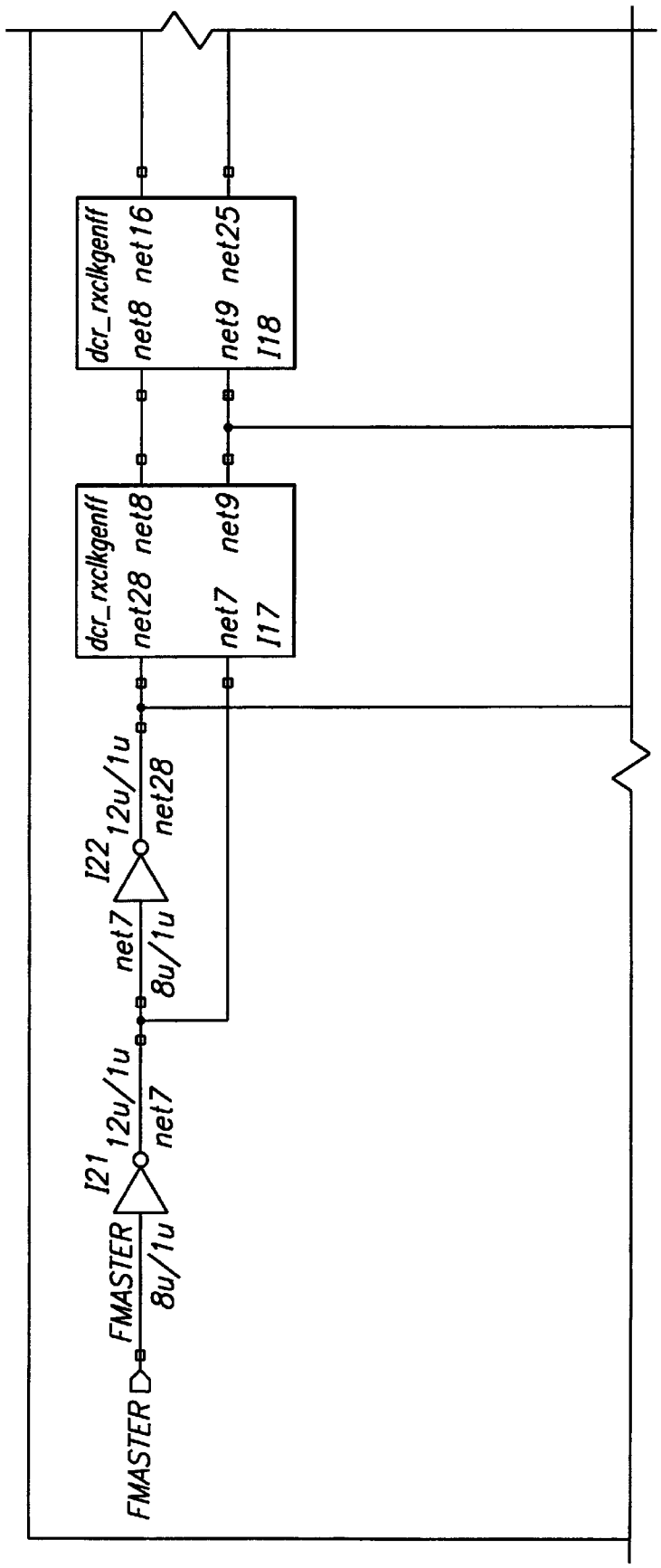
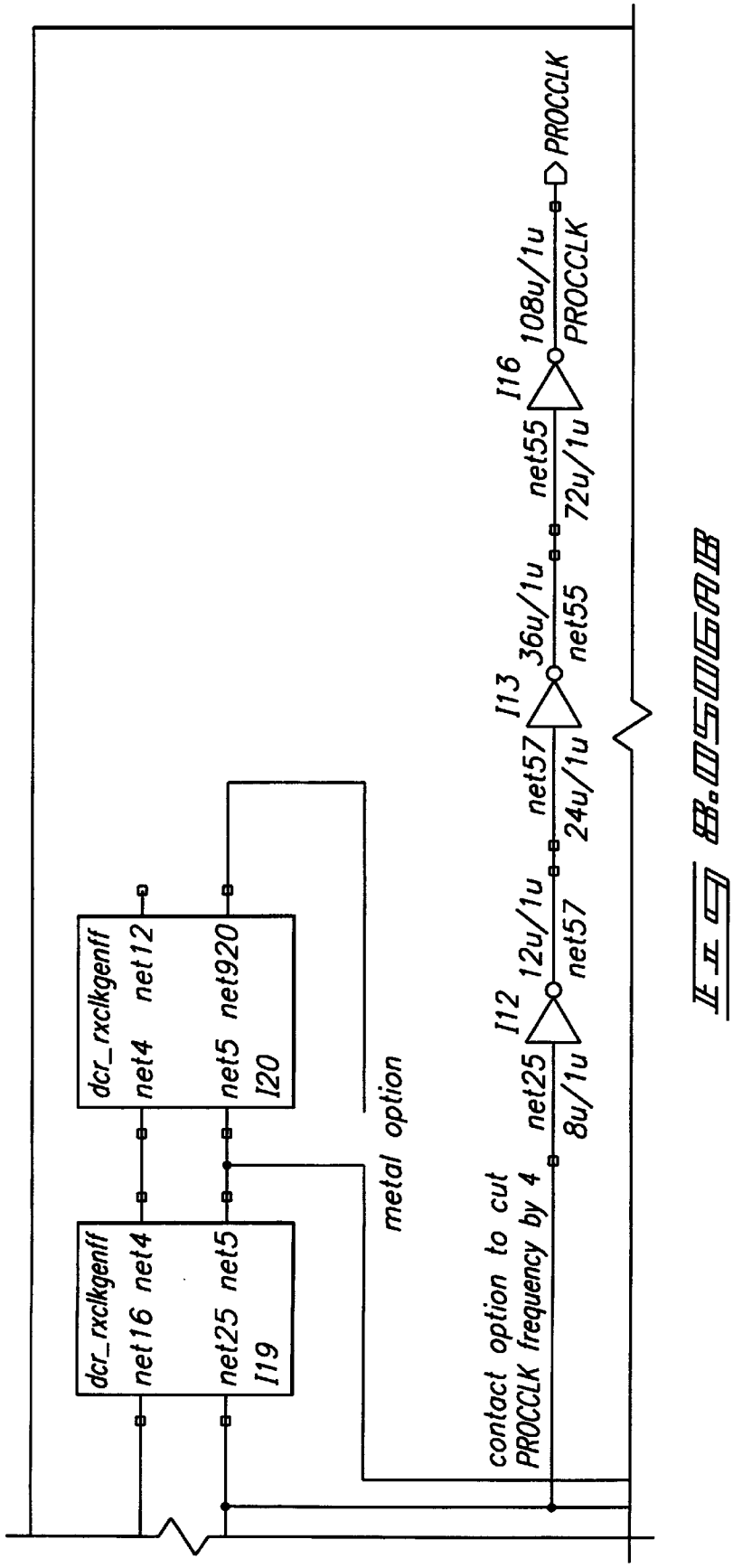

dcr_rxclkgenff
net8
net16
net9
net25
I18
dcr_rxclkgenff
net28
net8
net7
net9
I17
I22
12u/1u
net28
net7
8u/1u
I21
12u/1u
net7
FMASTER
8u/1u
FMASTER

FIG 89


dcr_rxclkgenff
net4 net12
net5 net920
I20
dcr_rxclkgenff
net16 net4
net25 net5
I19
metal option
contact option to cut
PROCCLK frequency by 4
net25
8u/1u
I12
12u/1u
net57
net57
24u/1u
I13
36u/1u
net55
net55
72u/1u
I16
108u/1u
PROCCLK
PROCCLK

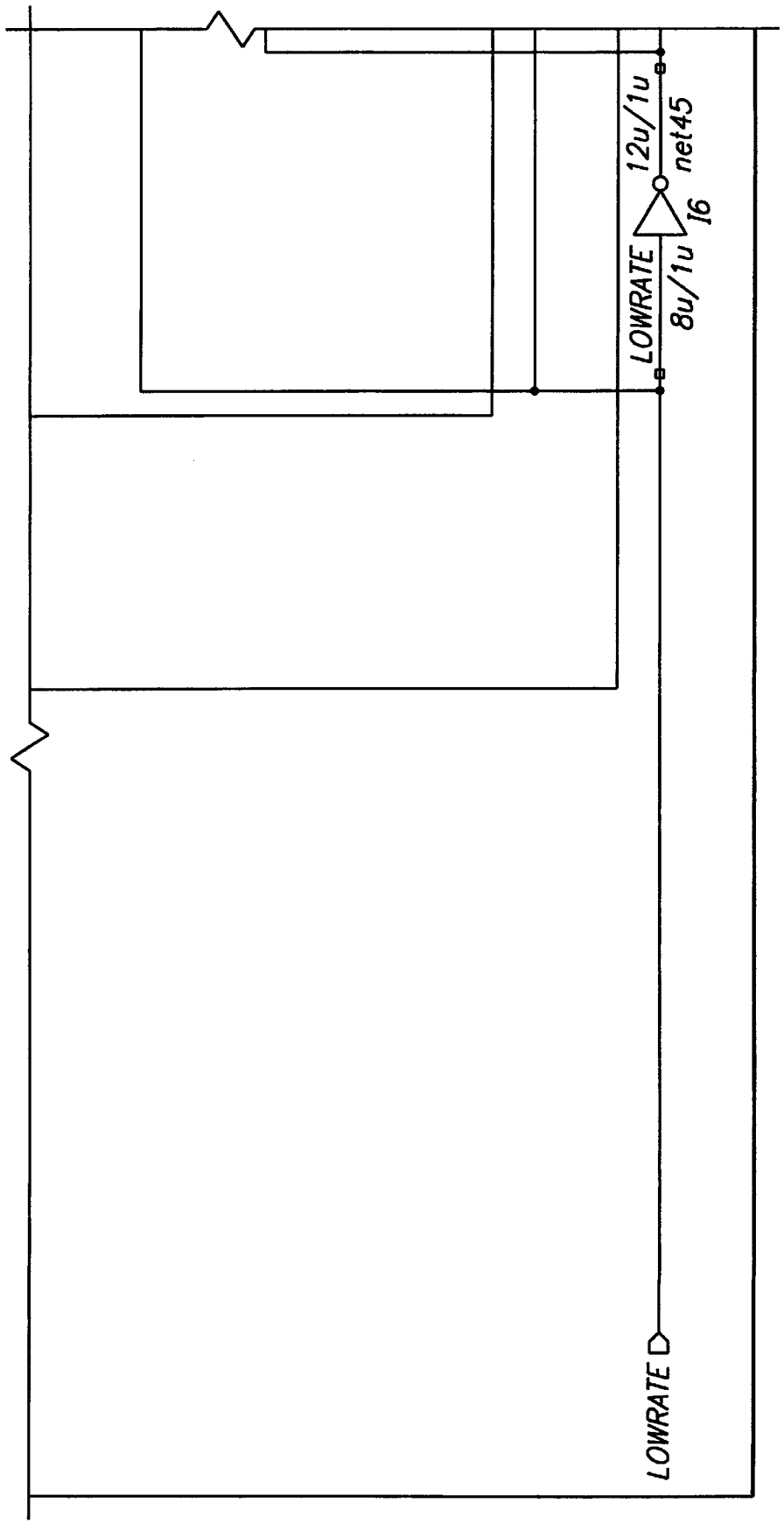


FIG 8,050,184A

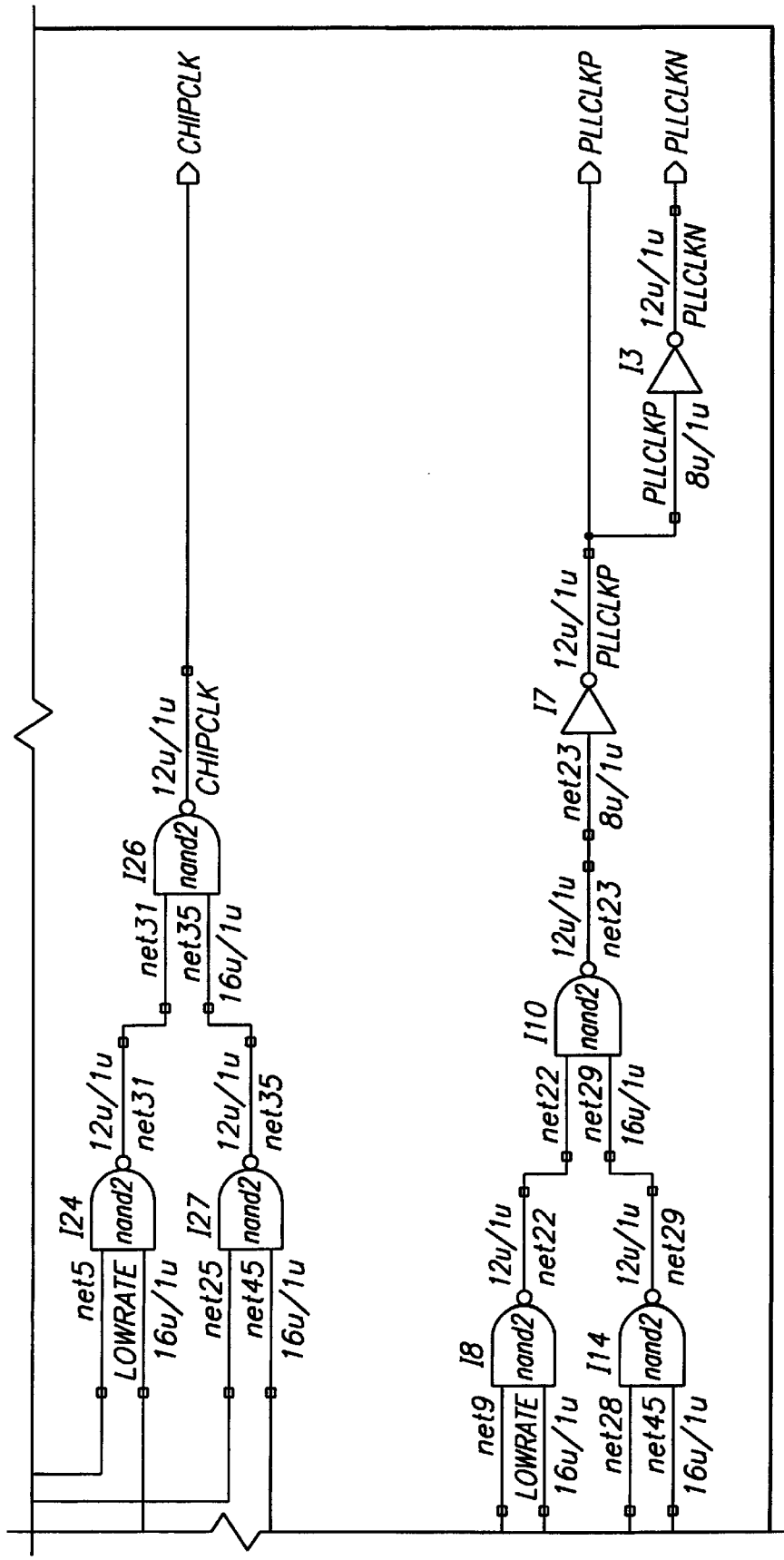

CHIPCLK
PLLCLKP
PLLCLKN
I26
nand2
12u/1u
16u/1u
net31
net35
I24
I27
net5
net25
LOWRATE
net45
I7
I10
I8
I14
net23
net22
net29
net9
net28
I3
8u/1u

FIG. 8.0056BB

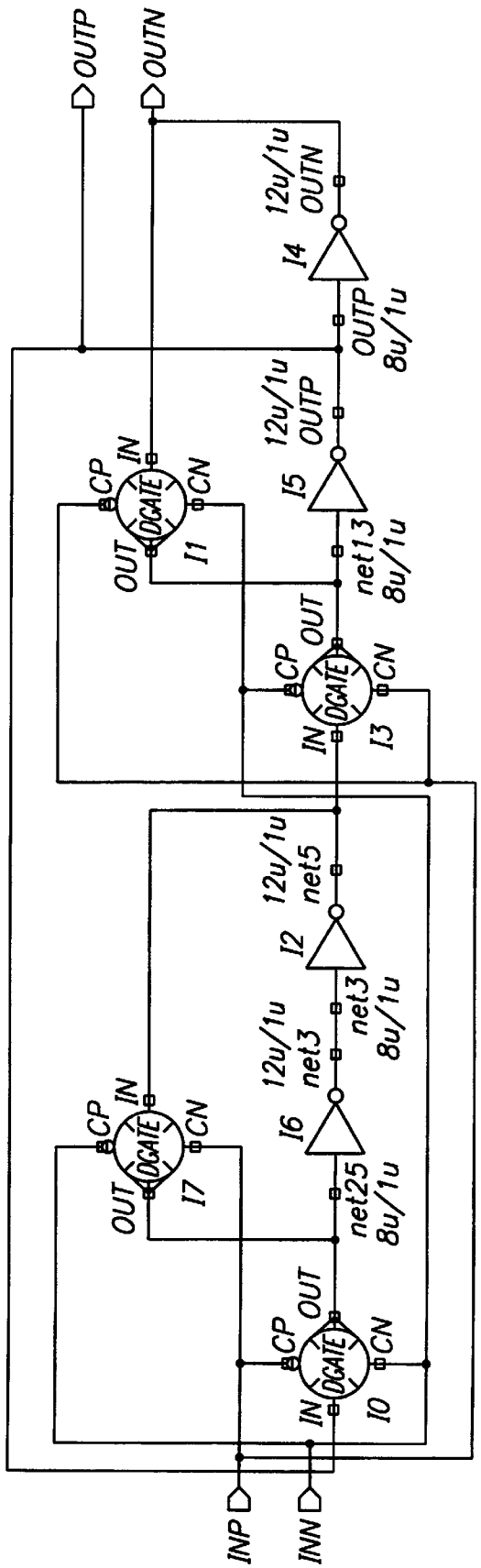
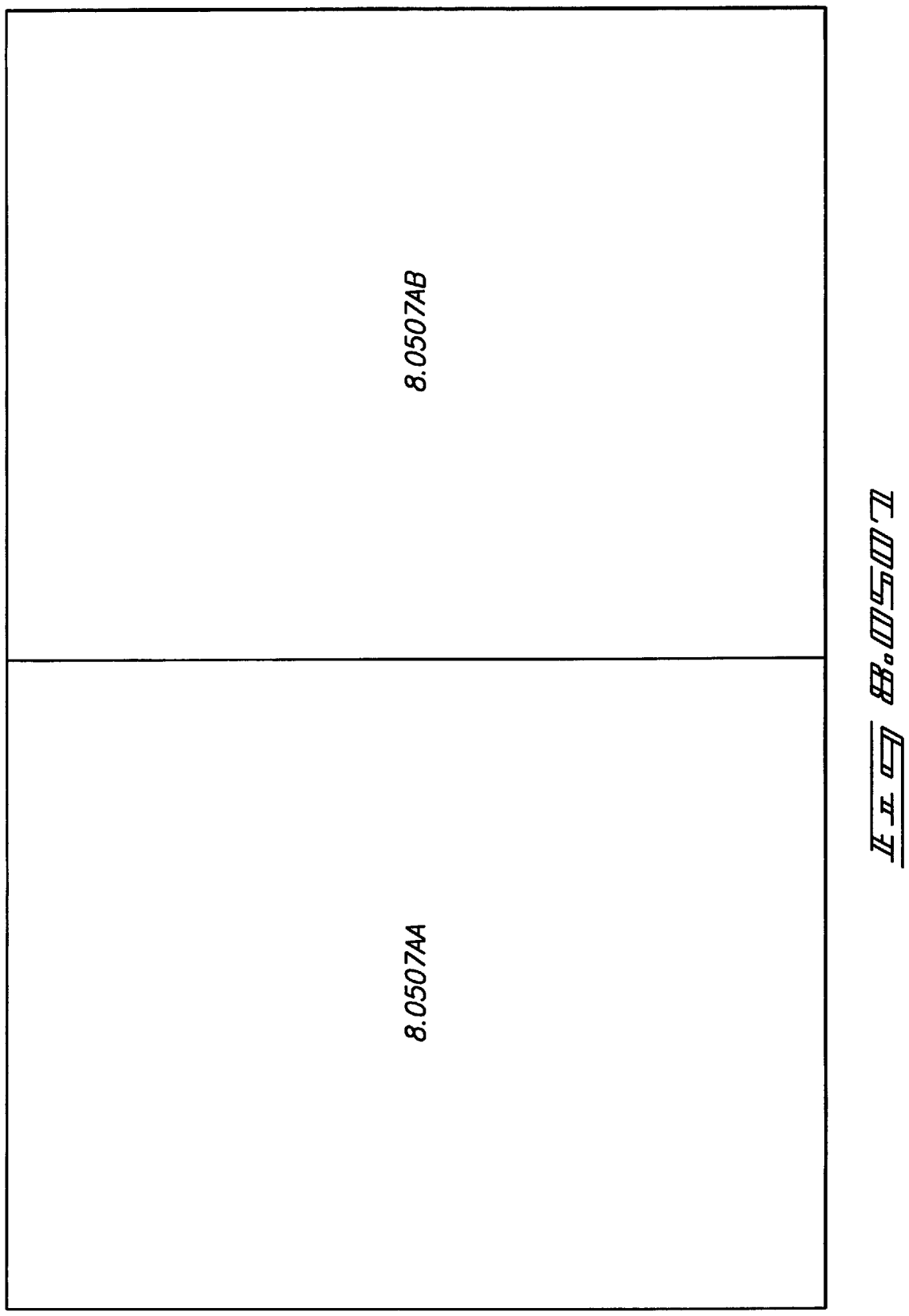

OUTP
OUTN
12u/1u
OUTN
I4
OUTP
8u/1u
12u/1u
OUTP
I5
net13
8u/1u
CP
IN
DGATE
CN
OUT
I1
CP
OUT
IN
DGATE
CN
I3
12u/1u
net5
I2
net3
8u/1u
12u/1u
net3
I6
net25
8u/1u
CP
IN
DGATE
CN
OUT
I7
CP
OUT
IN
DGATE
CN
I0
INP
INN

FIG 8.0S0S01


8.0507AB
8.0507AA
L.0508.88 FIT

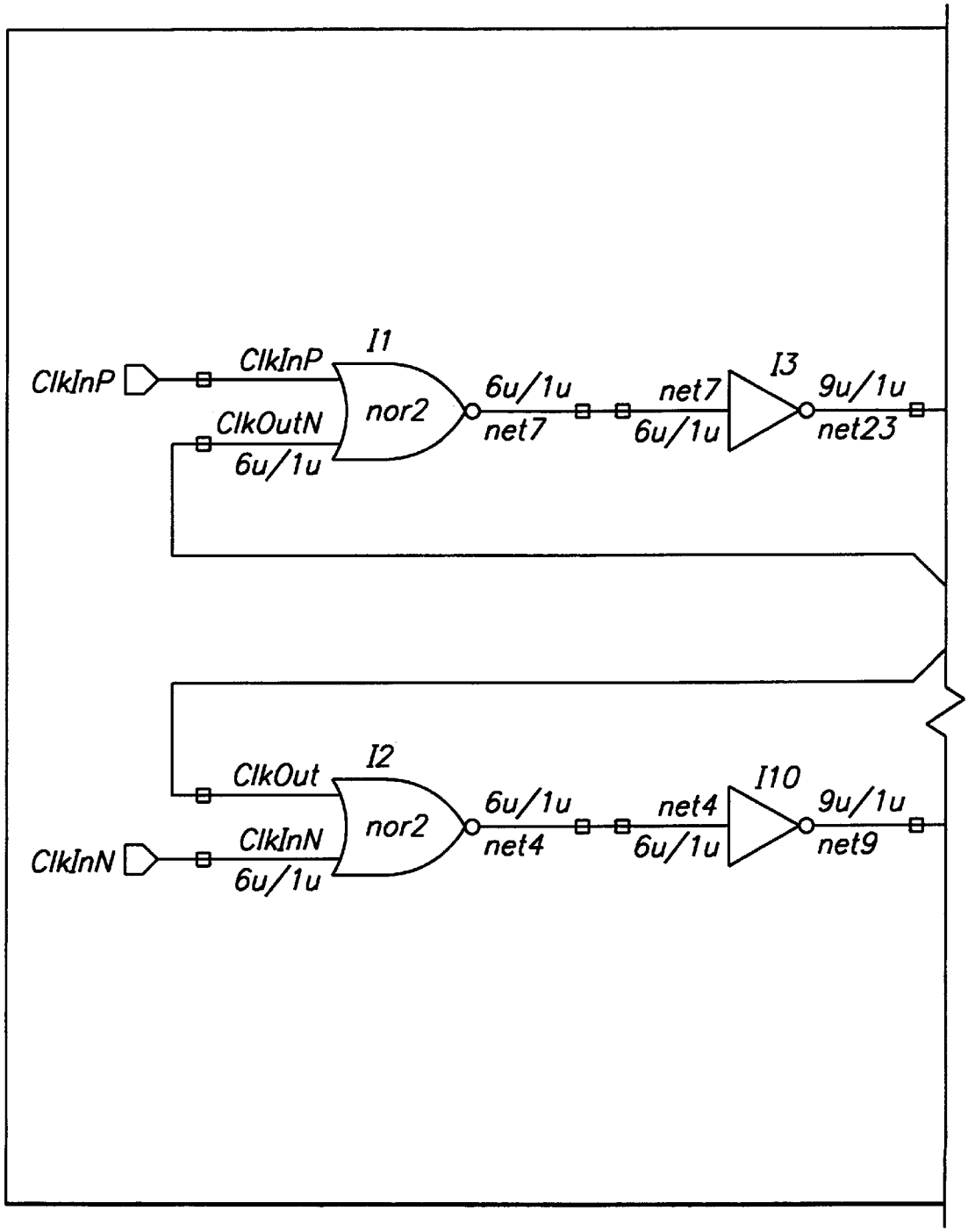

ClkInP
ClkInP
ClkOutN
6u/1u
I1
nor2
6u/1u
net7
net7
6u/1u
I3
9u/1u
net23
ClkOut
6u/1u
I2
nor2
6u/1u
net4
net4
6u/1u
I10
9u/1u
net9
ClkInN
ClkInN
6u/1u

Fig 8.0501AA

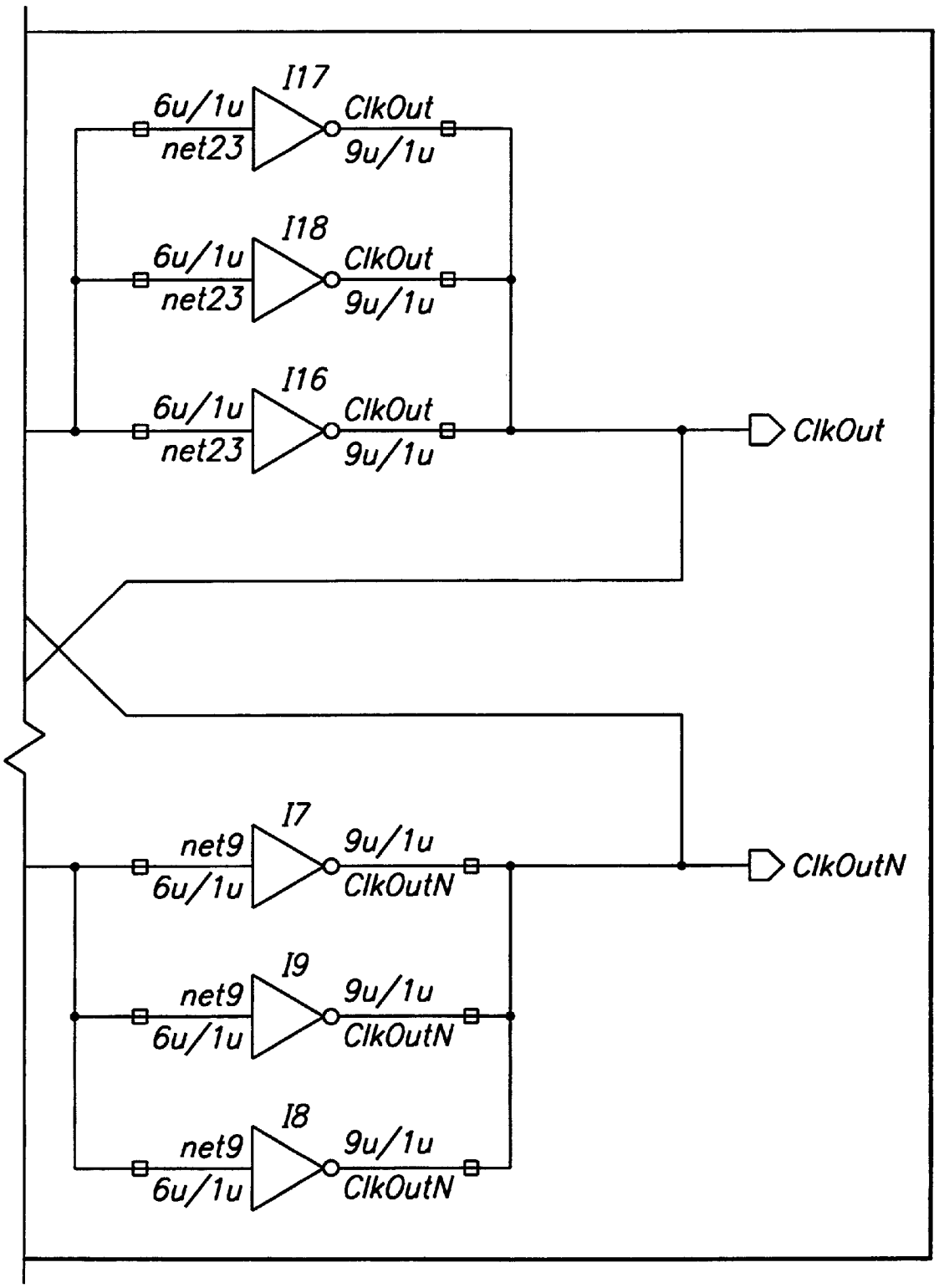

I17
6u/1u
net23
ClkOut
9u/1u
I18
6u/1u
net23
ClkOut
9u/1u
I16
6u/1u
net23
ClkOut
9u/1u
ClkOut
I7
net9
6u/1u
9u/1u
ClkOutN
ClkOutN
I9
net9
6u/1u
9u/1u
ClkOutN
I8
net9
6u/1u
9u/1u
ClkOutN

Fig 8.0501AB

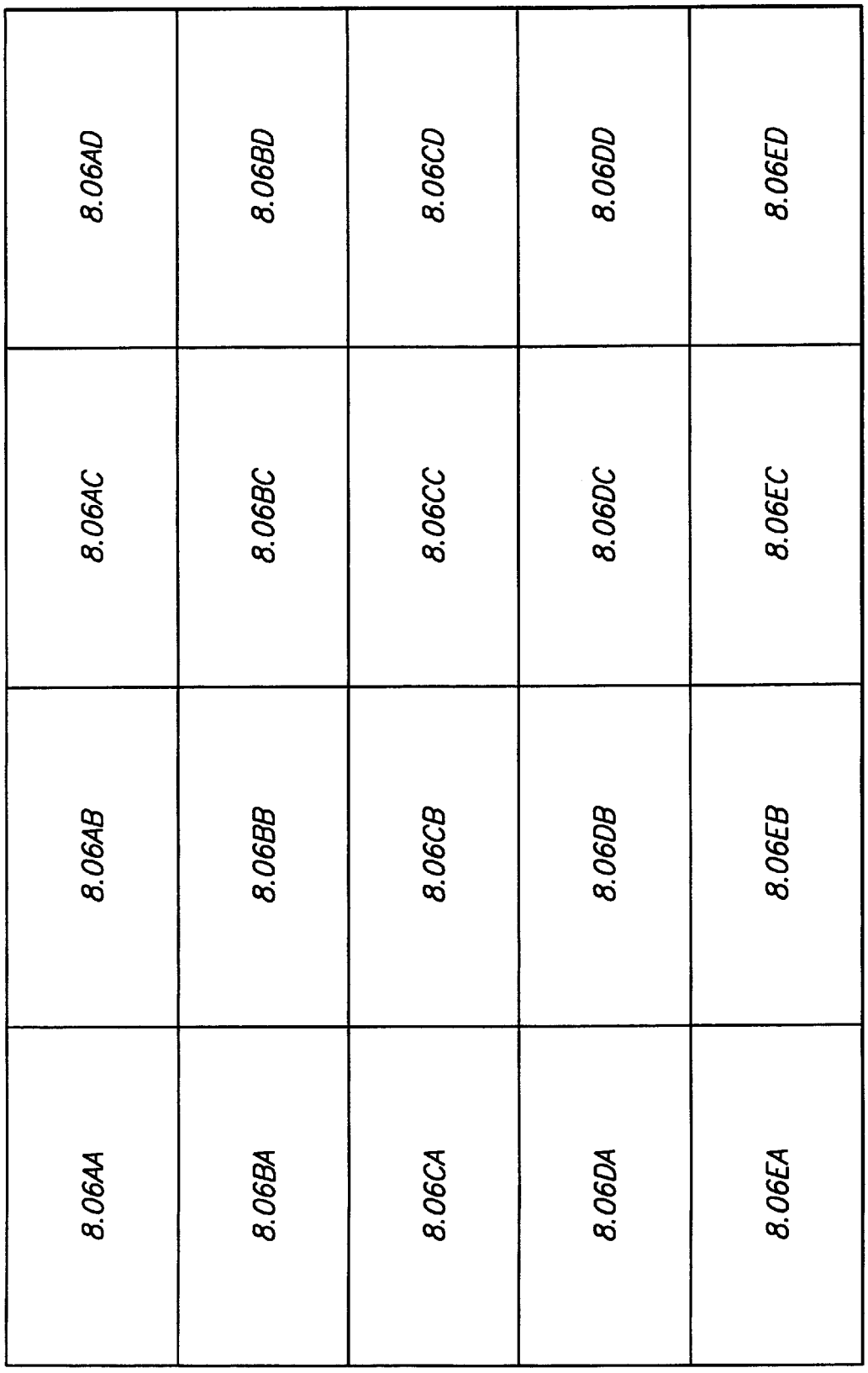
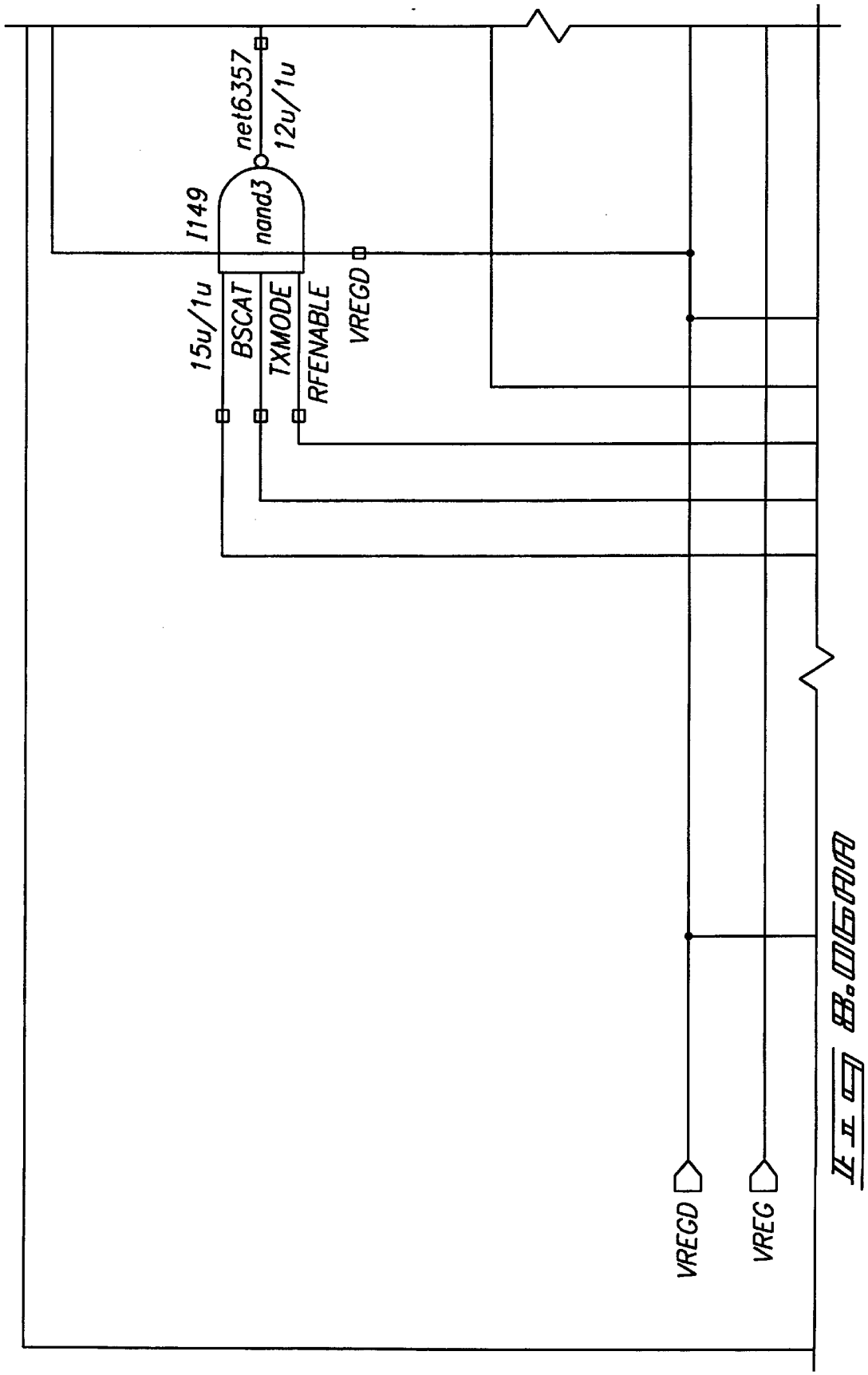
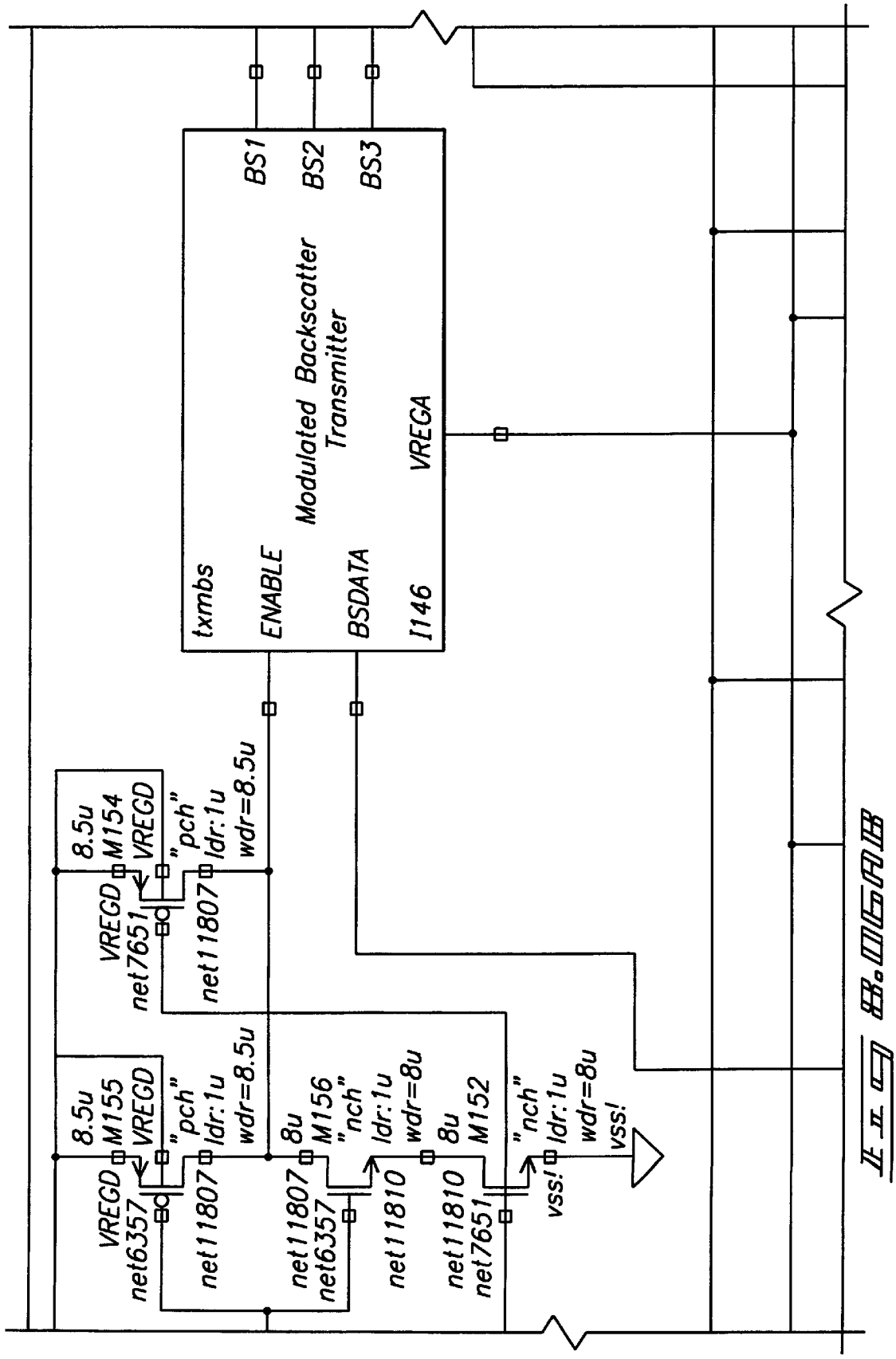
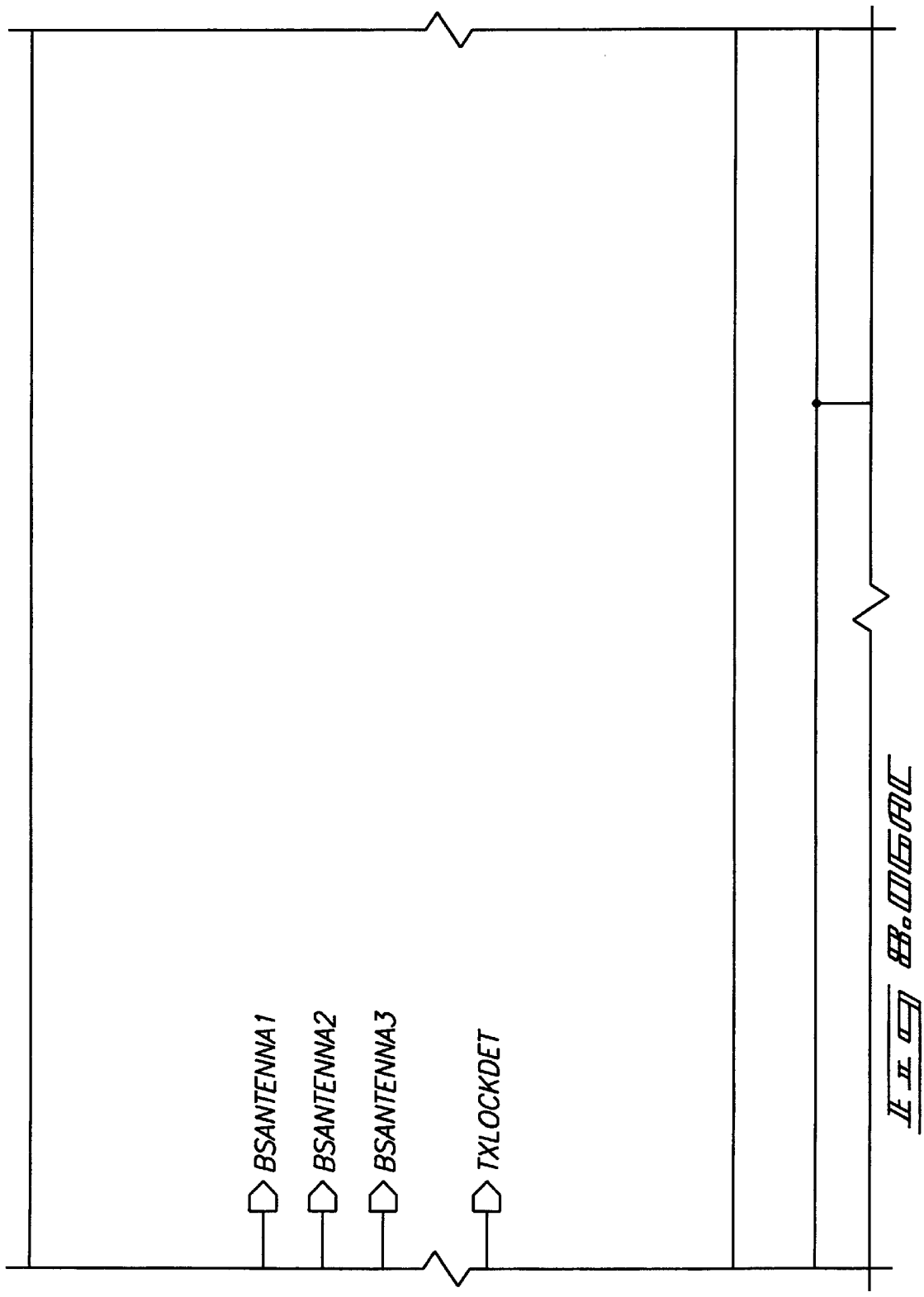

8.06AD
8.06BD
8.06CD
8.06DD
8.06ED
8.06AC
8.06BC
8.06CC
8.06DC
8.06EC
8.06AB
8.06BB
8.06CB
8.06DB
8.06EB
8.06AA
8.06BA
8.06CA
8.06DA
8.06EA

FIG. 8.0065


net6357
12u/1u
I149
nand3
15u/1u
BSCAT
TXMODE
RFENABLE
VREGD
VREGD
VREG


BS1
BS2
BS3
Modulated Backscatter Transmitter
txmbs
ENABLE
BSDATA
I146
VREGA
8.5u
M154
VREGD
"pch"
ldr:1u
wdr=8.5u
VREGD
net7651
net11807
8.5u
M155
VREGD
"pch"
ldr:1u
wdr=8.5u
VREGD
net6357
net11807
8u
M156
"nch"
ldr:1u
wdr=8u
net11807
net6357
net11810
8u
M152
"nch"
ldr:1u
wdr=8u
net11810
net7651
vss!
vss!


BSANTENNA1
BSANTENNA2
BSANTENNA3
TXLOCKDET
FIG. 88.0GAC

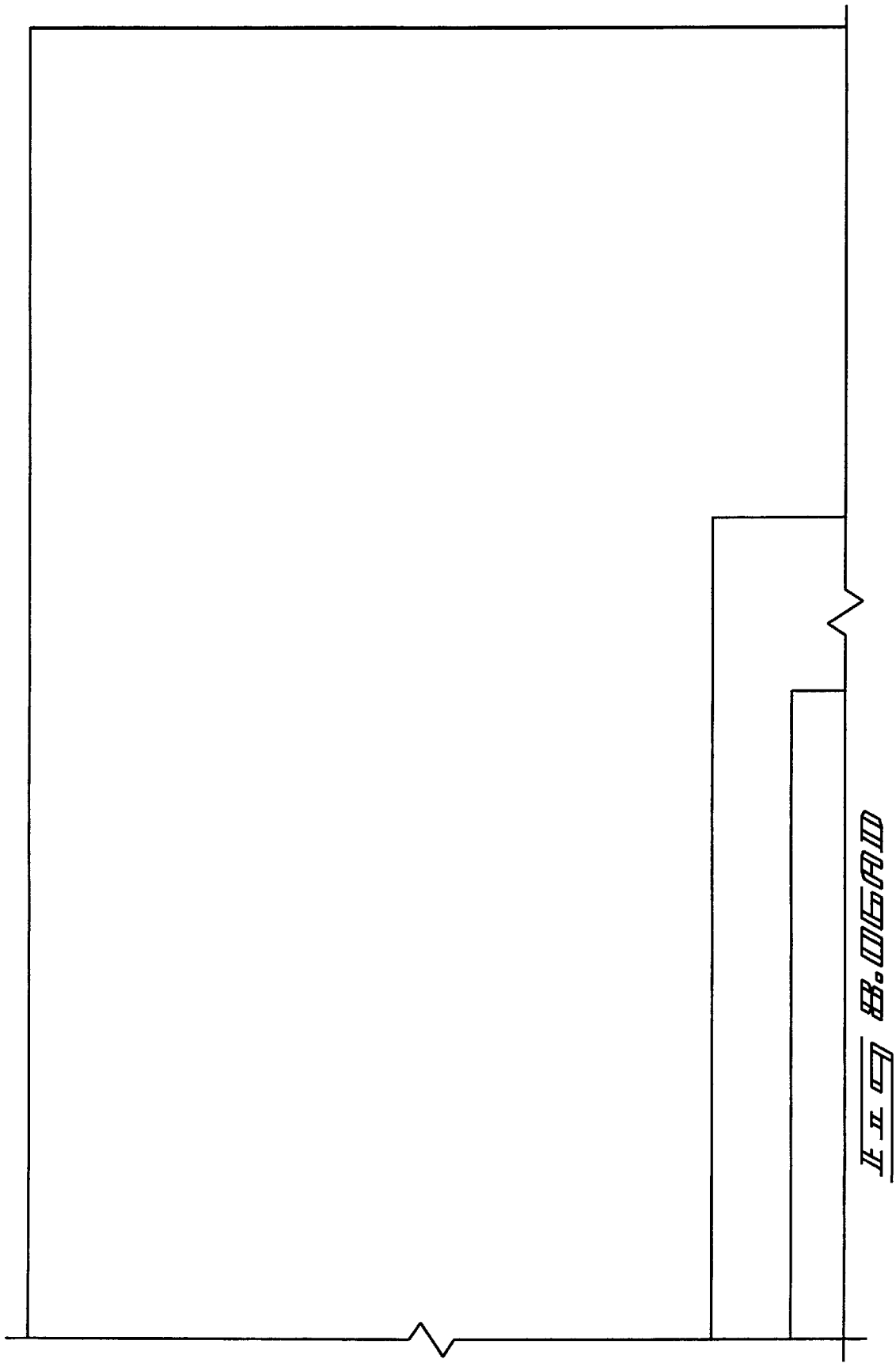


FIG. 88.05AD

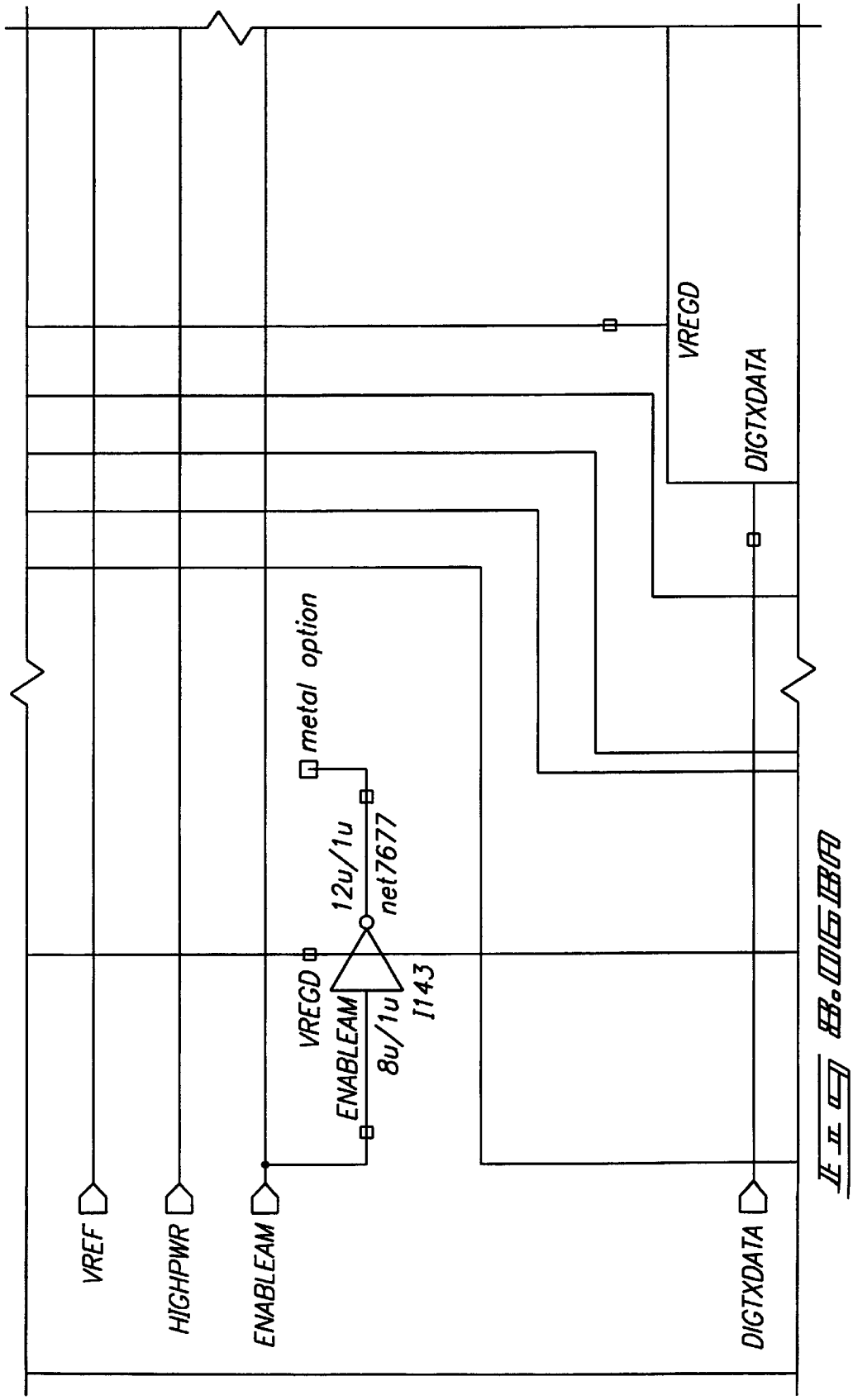
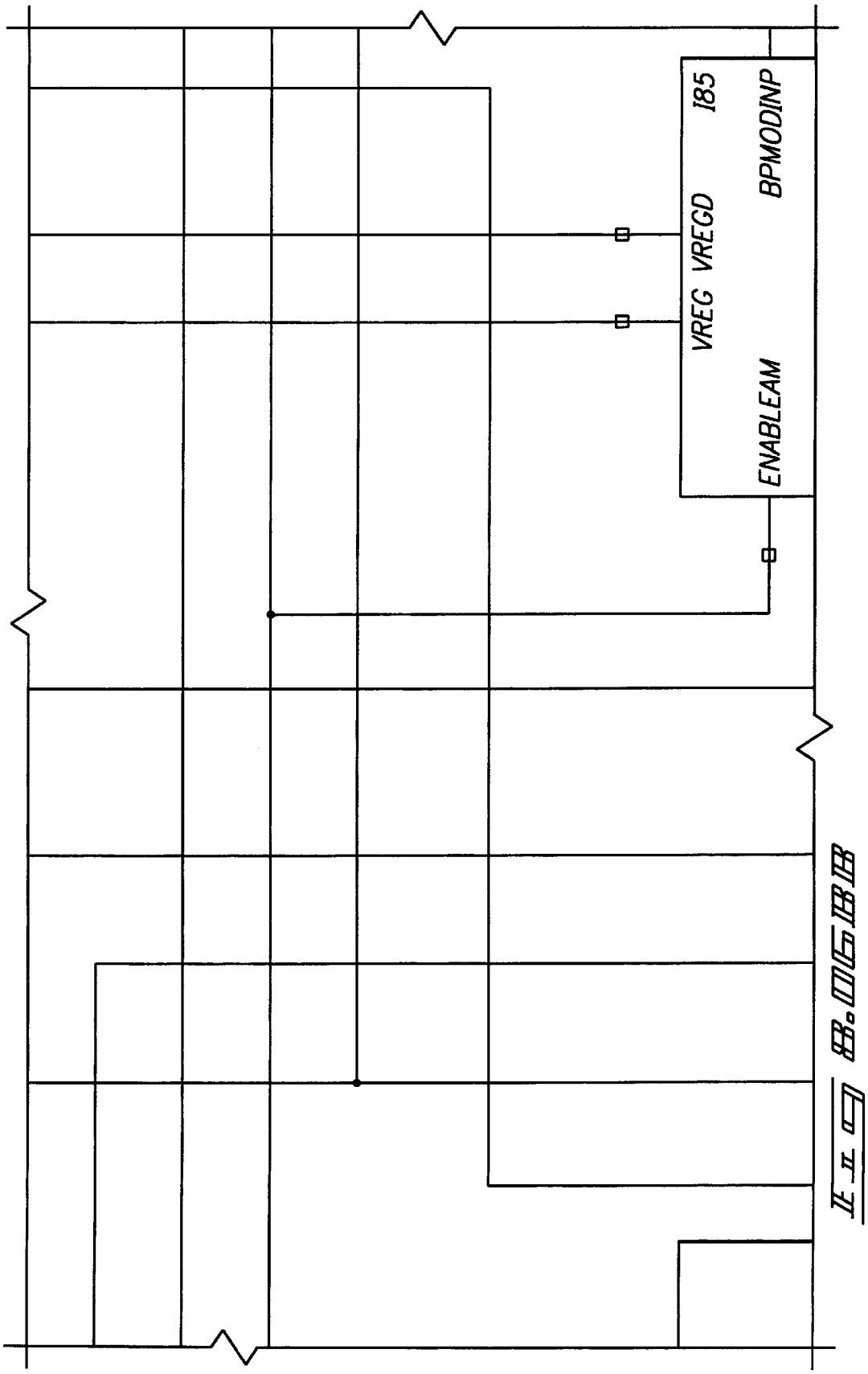

VREGD
DIGTXDATA
metal option
12u/1u
net7677
VREGD
ENABLEAM
8u/1u
I143
VREF
HIGHPWR
ENABLEAM
DIGTXDATA

Fig 8.0618A


I85
BPMODINP
VREG
VREGD
ENABLEAM

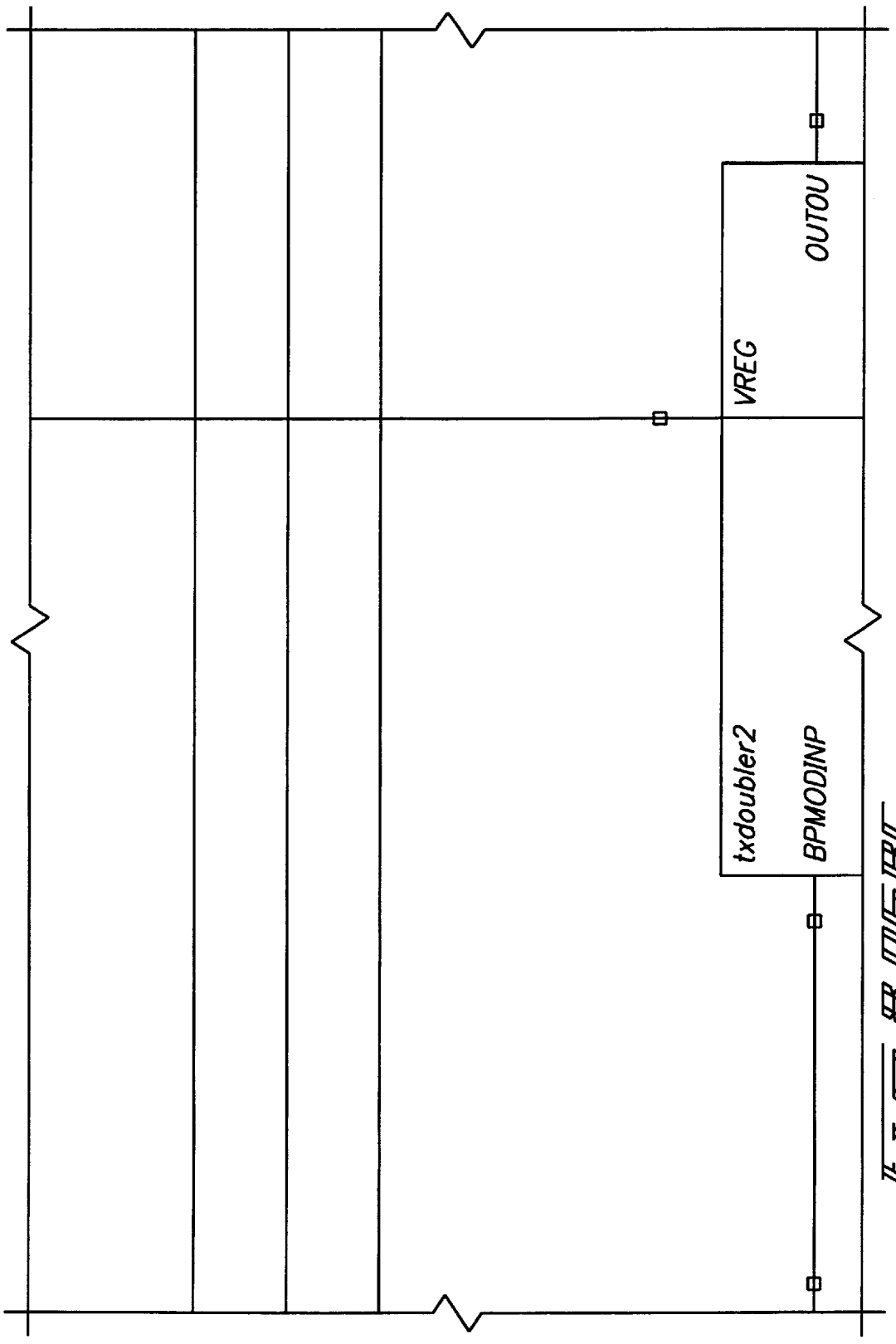
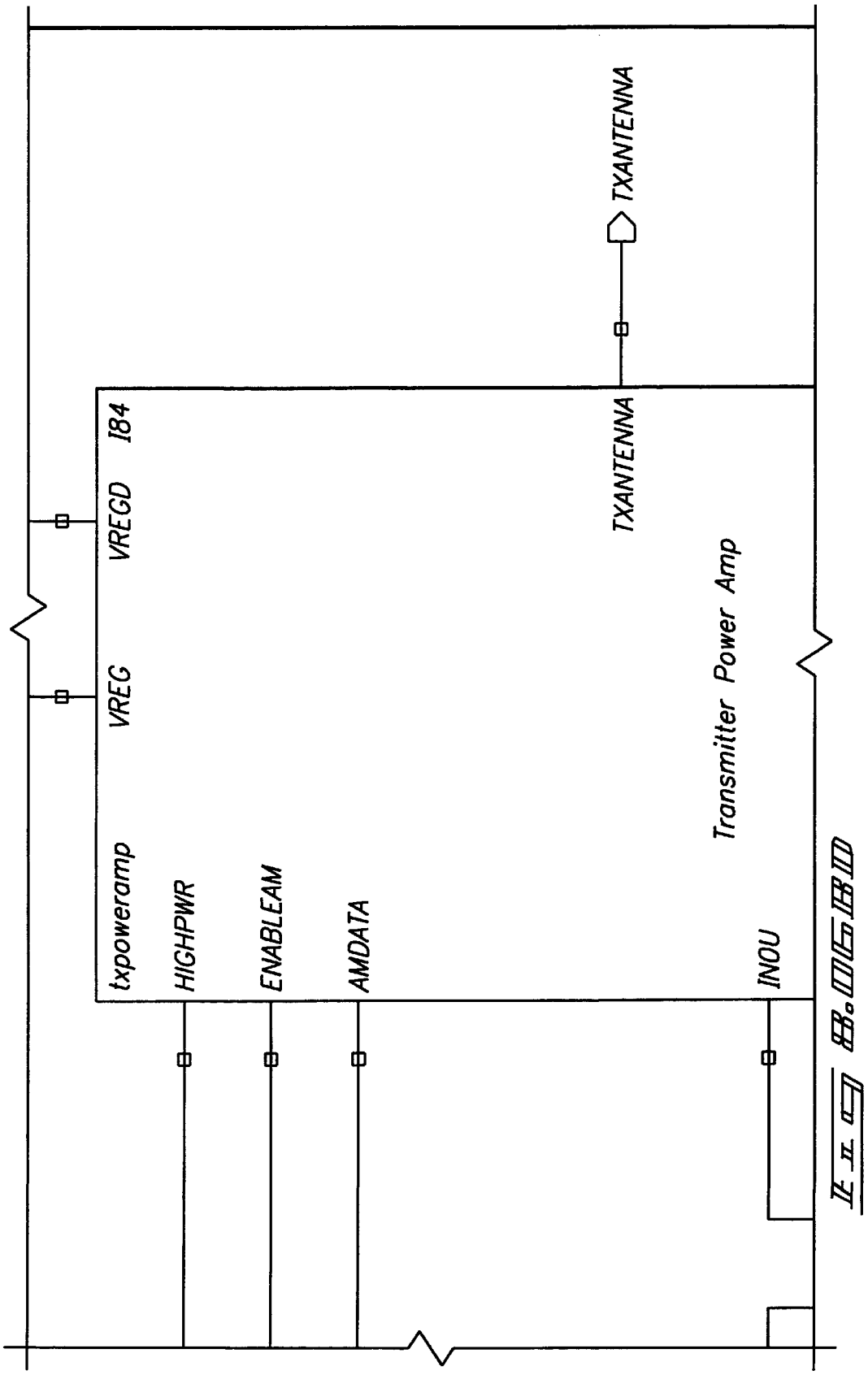


FIG. 88.00516IBIC


TXANTENNA
TXANTENNA
I84
VREGD
VREG
txpoweramp
HIGHPWR
ENABLEAM
AMDATA
Transmitter Power Amp
INOU

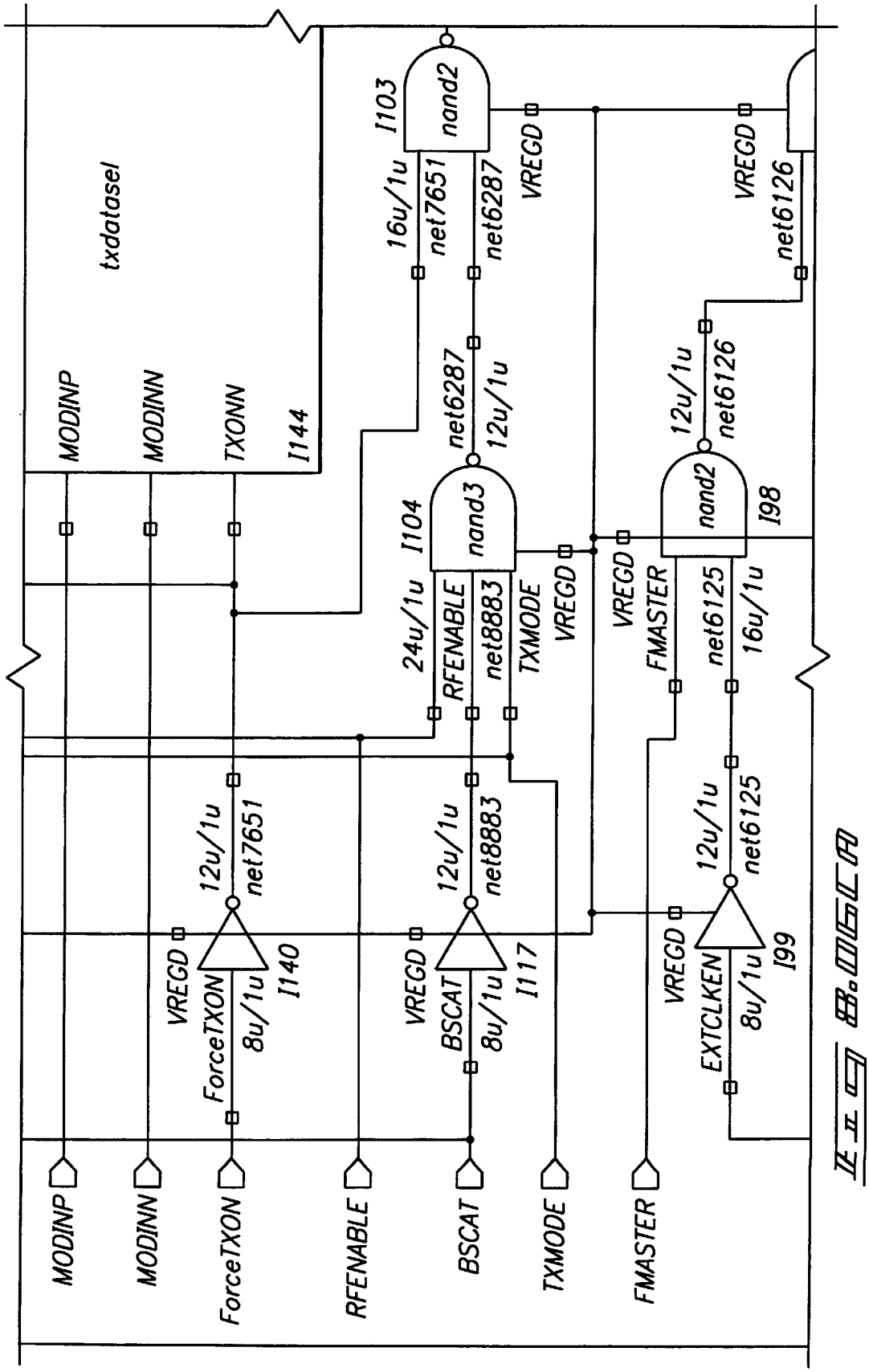

txdatasel
MODINP
MODINN
TXONN
I144
I103
nand2
16u/1u
net7651
net6287
VREGD
net6126
I104
nand3
24u/1u
RFENABLE
net8883
TXMODE
12u/1u
I98
FMASTER
net6125
I140
ForceTXON
8u/1u
I117
BSCAT
I99
EXTCLKEN

FIG. 88.0056A

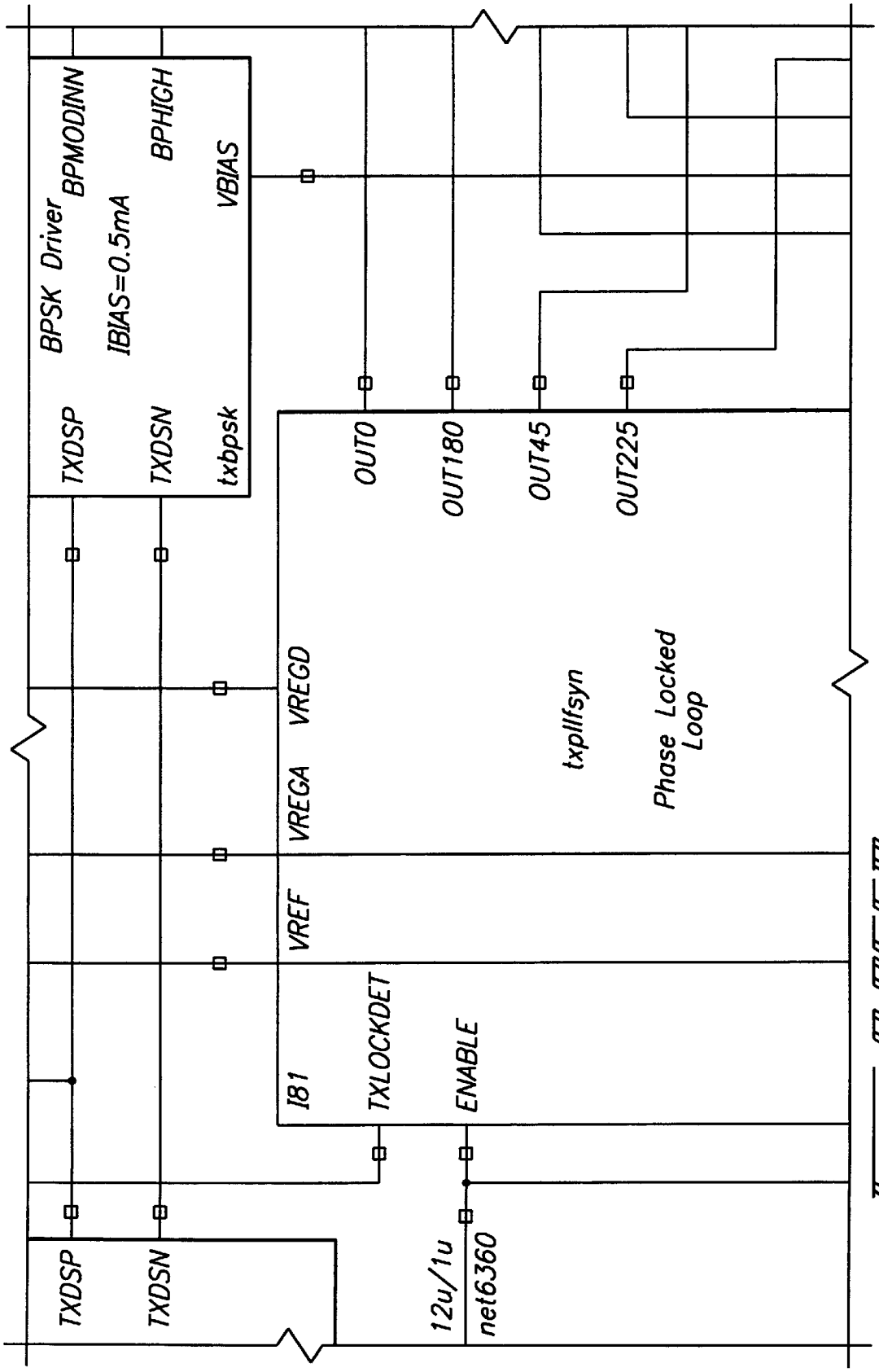

BPSK Driver
BPMODINN
IBIAS=0.5mA
BPHIGH
VBIAS
TXDSP
TXDSN
txbpsk
OUT0
OUT180
OUT45
OUT225
VREGD
VREGA
txpllfsyn
Phase Locked Loop
VREF
I81
TXLOCKDET
ENABLE
TXDSP
TXDSN
12u/1u
net6360

FIG. 88.0050

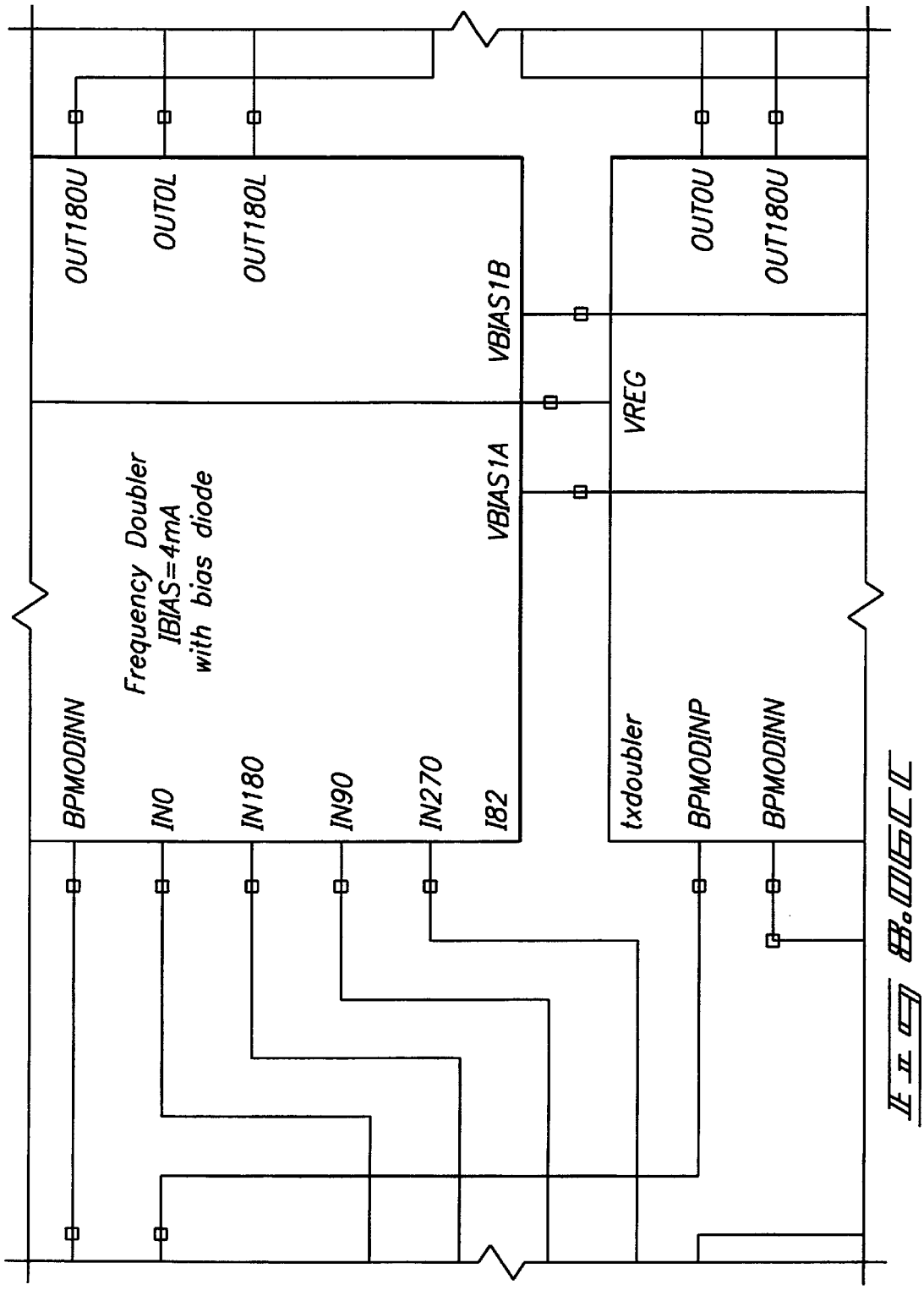

OUT180U
OUT0L
OUT180L
VBIAS1B
OUT0U
OUT180U
VREG
Frequency Doubler
IBIAS=4mA
with bias diode
VBIAS1A
BPMODINN
IN0
IN180
IN90
IN270
I82
txdoubler
BPMODINP
BPMODINN

FIG 88.00796

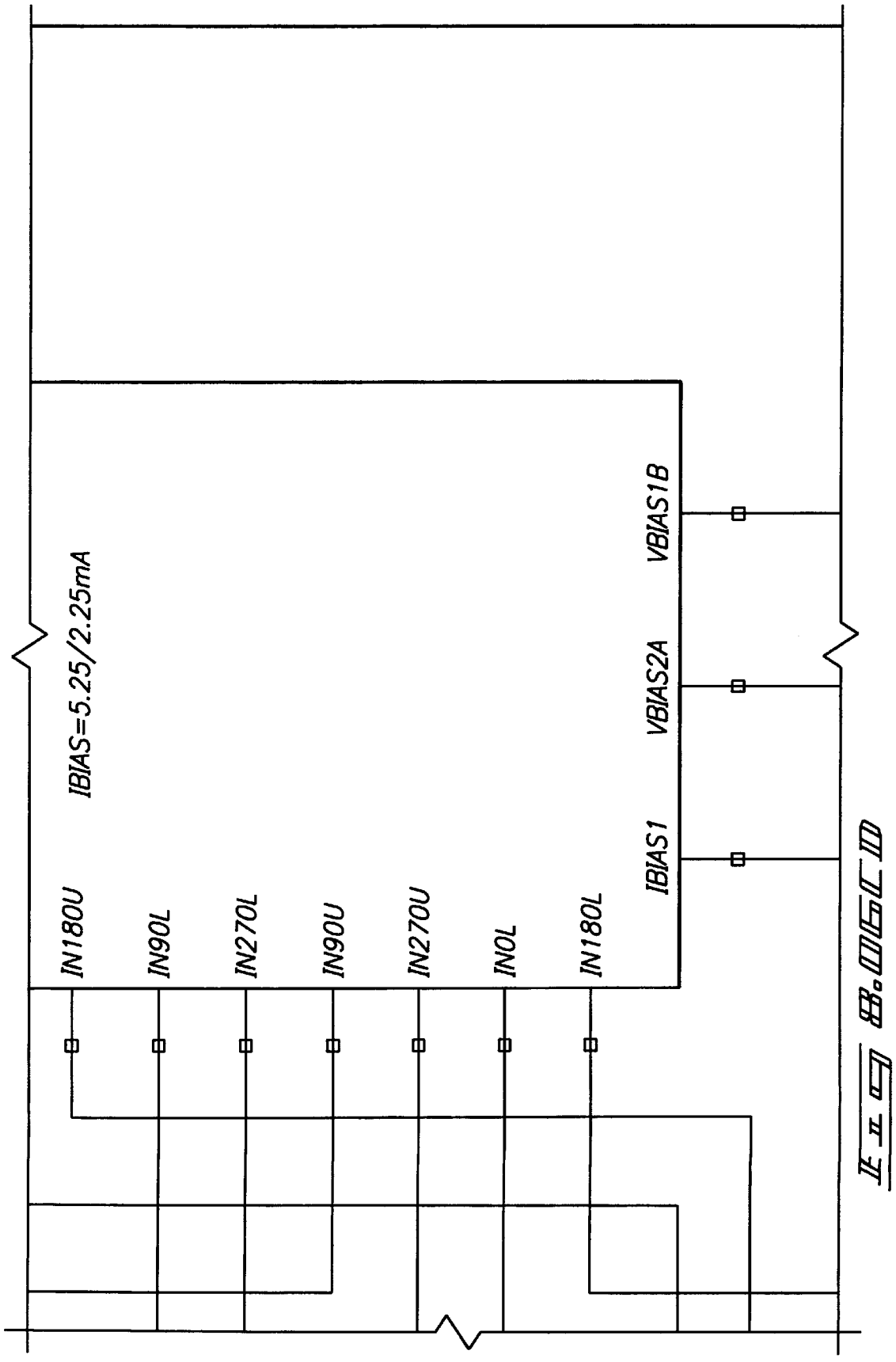

IBIAS=5.25/2.25mA
VBIAS1B
VBIAS2A
IBIAS1
IN180U
IN90L
IN270L
IN90U
IN270U
IN0L
IN180L

FIG 8.0500

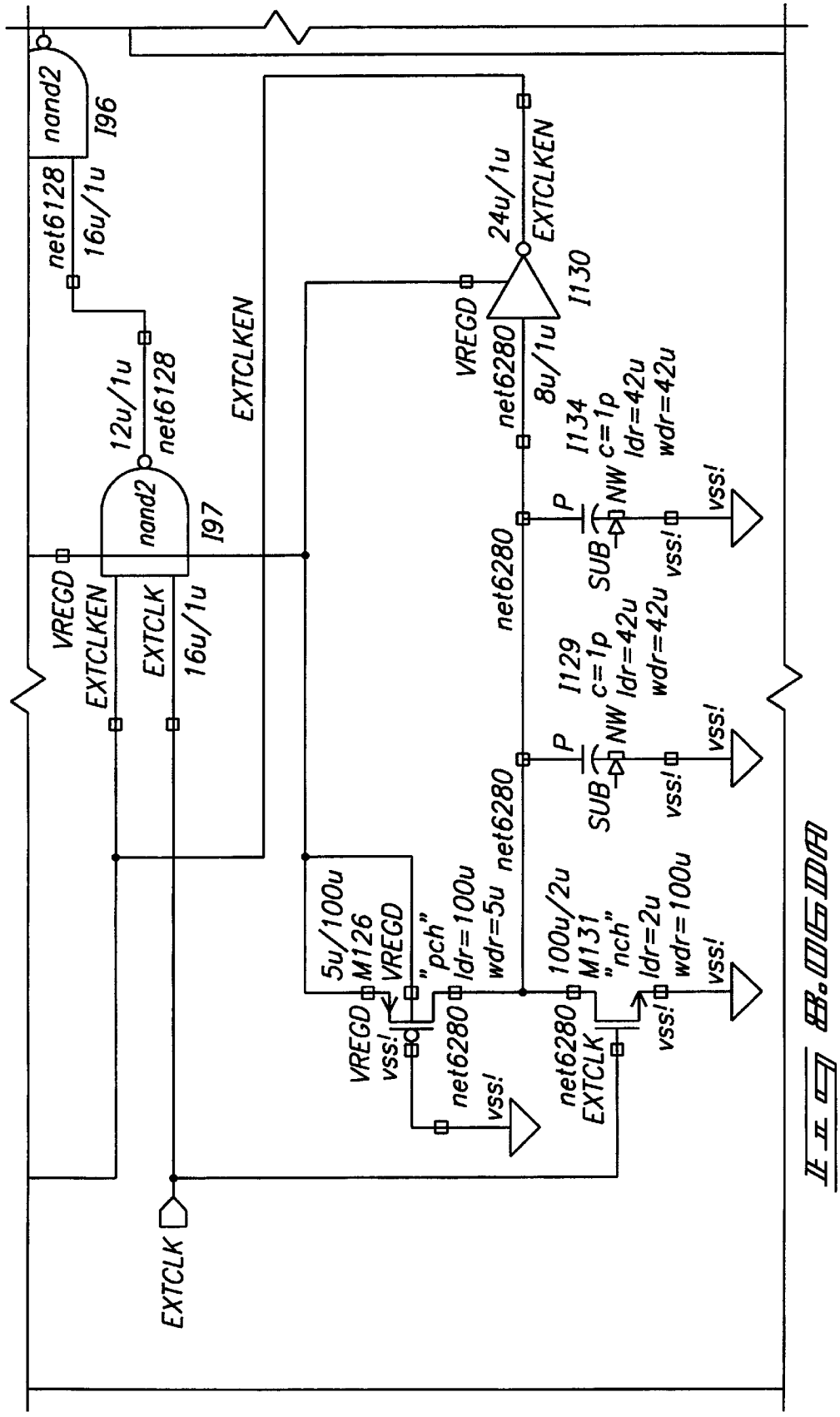

nand2
I96
net6128
16u/1u
12u/1u
net6128
nand2
I97
VREGD
EXTCLKEN
EXTCLK
16u/1u
EXTCLKEN
EXTCLK
24u/1u
EXTCLKEN
I130
VREGD
net6280
8u/1u
I134
c=1p
ldr=42u
wdr=42u
P
NW
SUB
vss!
net6280
I129
c=1p
ldr=42u
wdr=42u
P
NW
SUB
vss!
net6280
5u/100u
M126
VREGD
"pch"
ldr=100u
wdr=5u
VREGD
vss!
net6280
vss!
100u/2u
M131
"nch"
ldr=2u
wdr=100u
net6280
EXTCLK
vss!
vss!
EXTCLK

FIG. 88.1054A

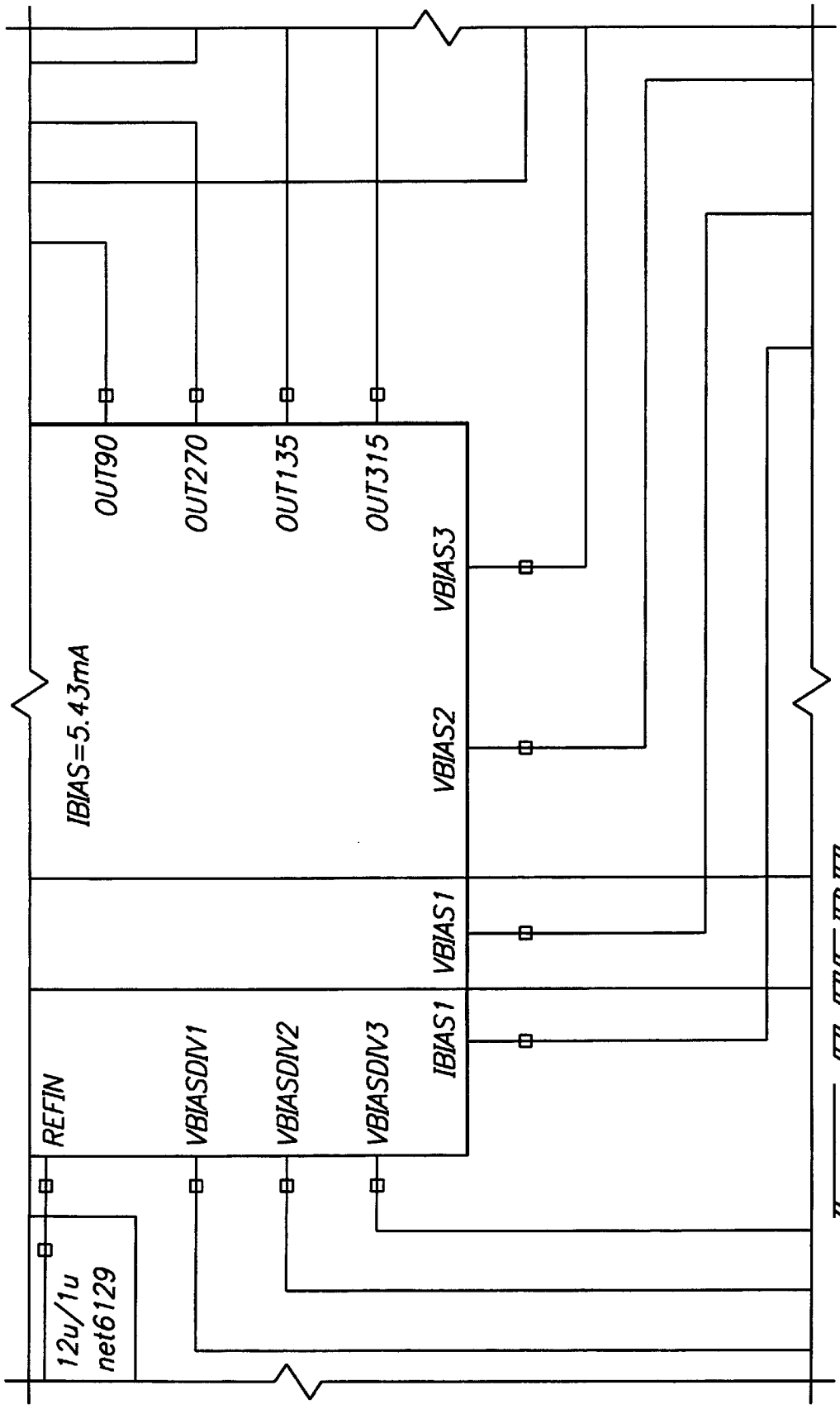


Fig 88.005.018

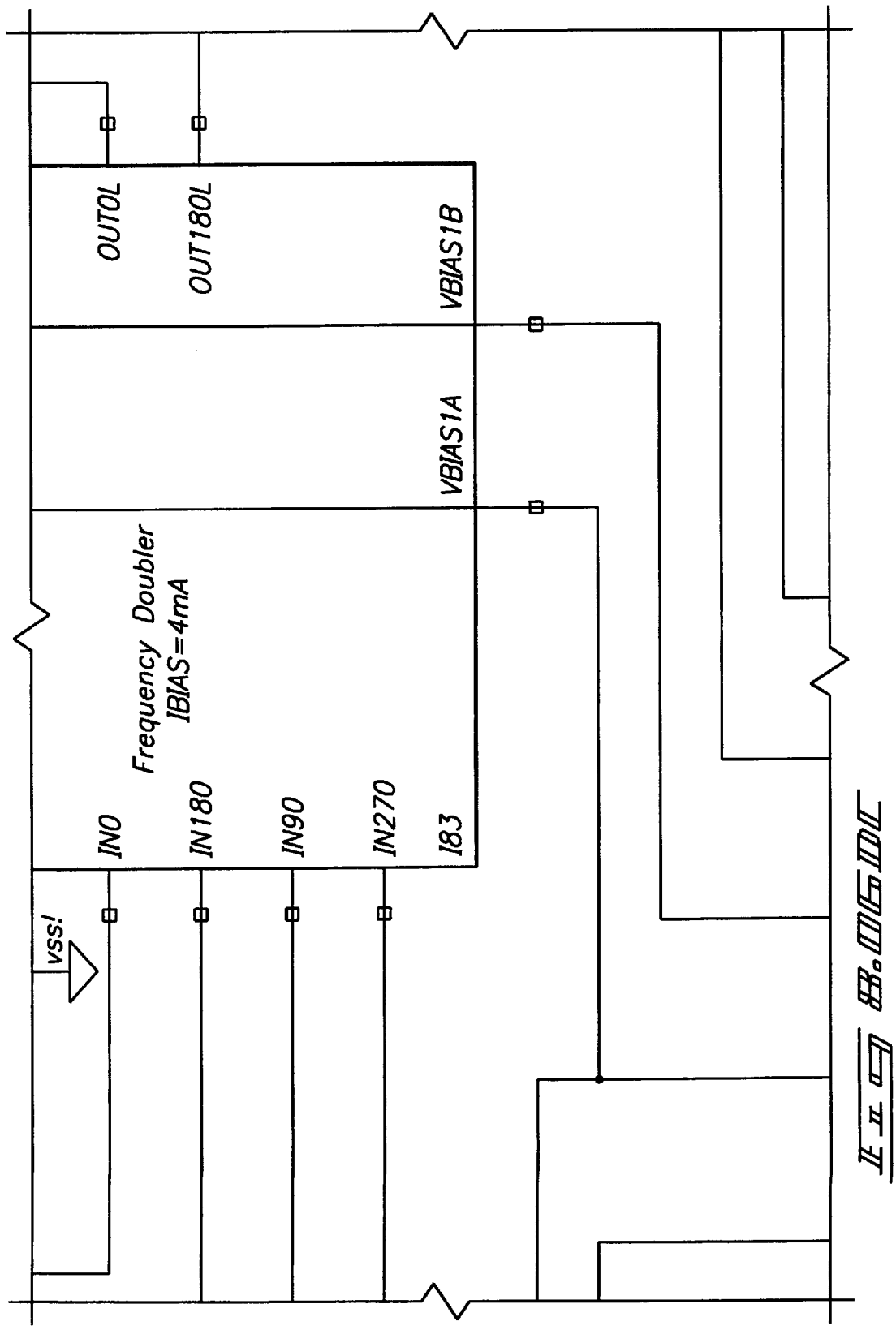

OUT0L
OUT180L
VBIAS1B
VBIAS1A
Frequency Doubler
IBIAS=4mA
IN0
IN180
IN90
IN270
I83
vss!

FIG. 1843

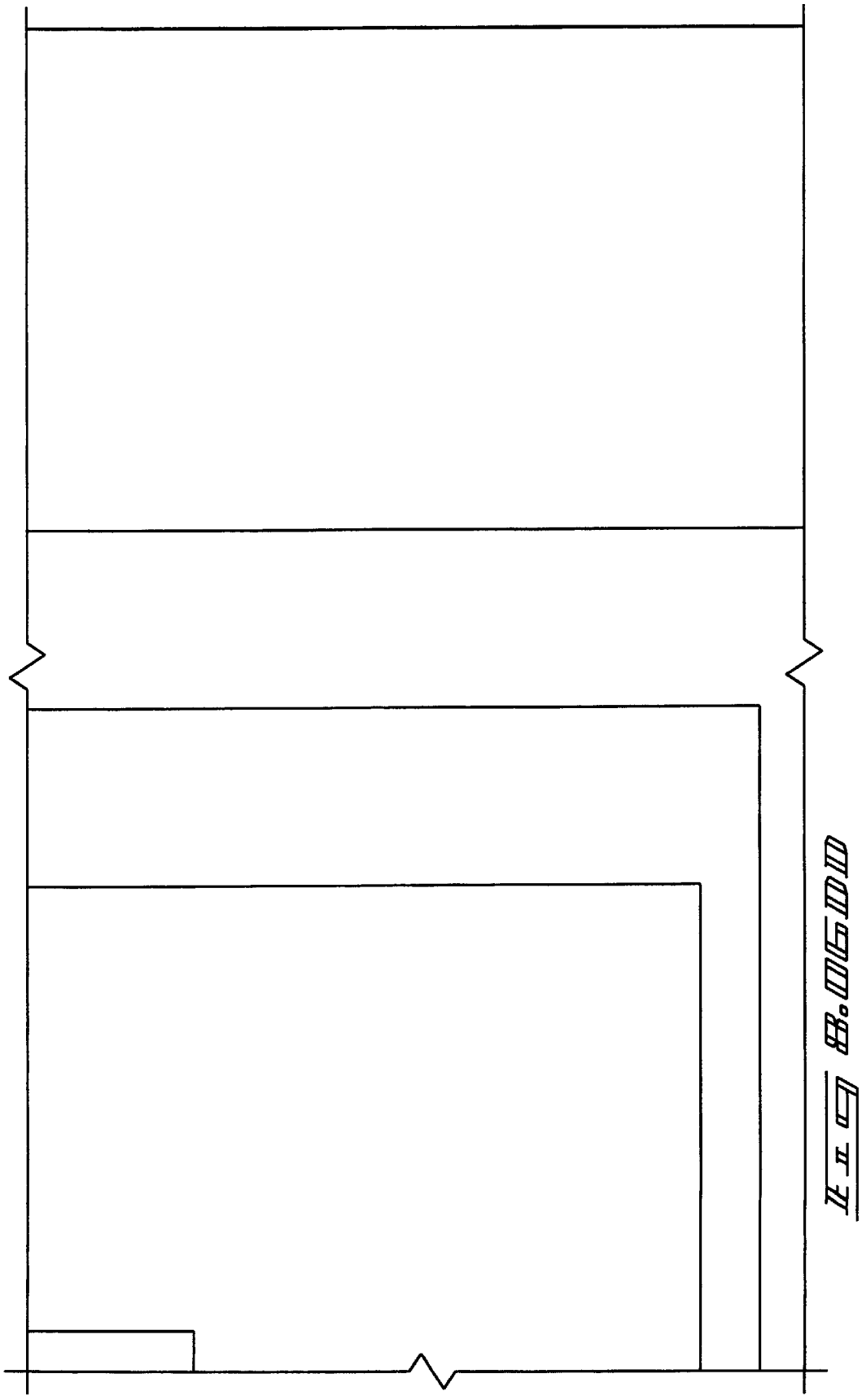


FIG 88.0000

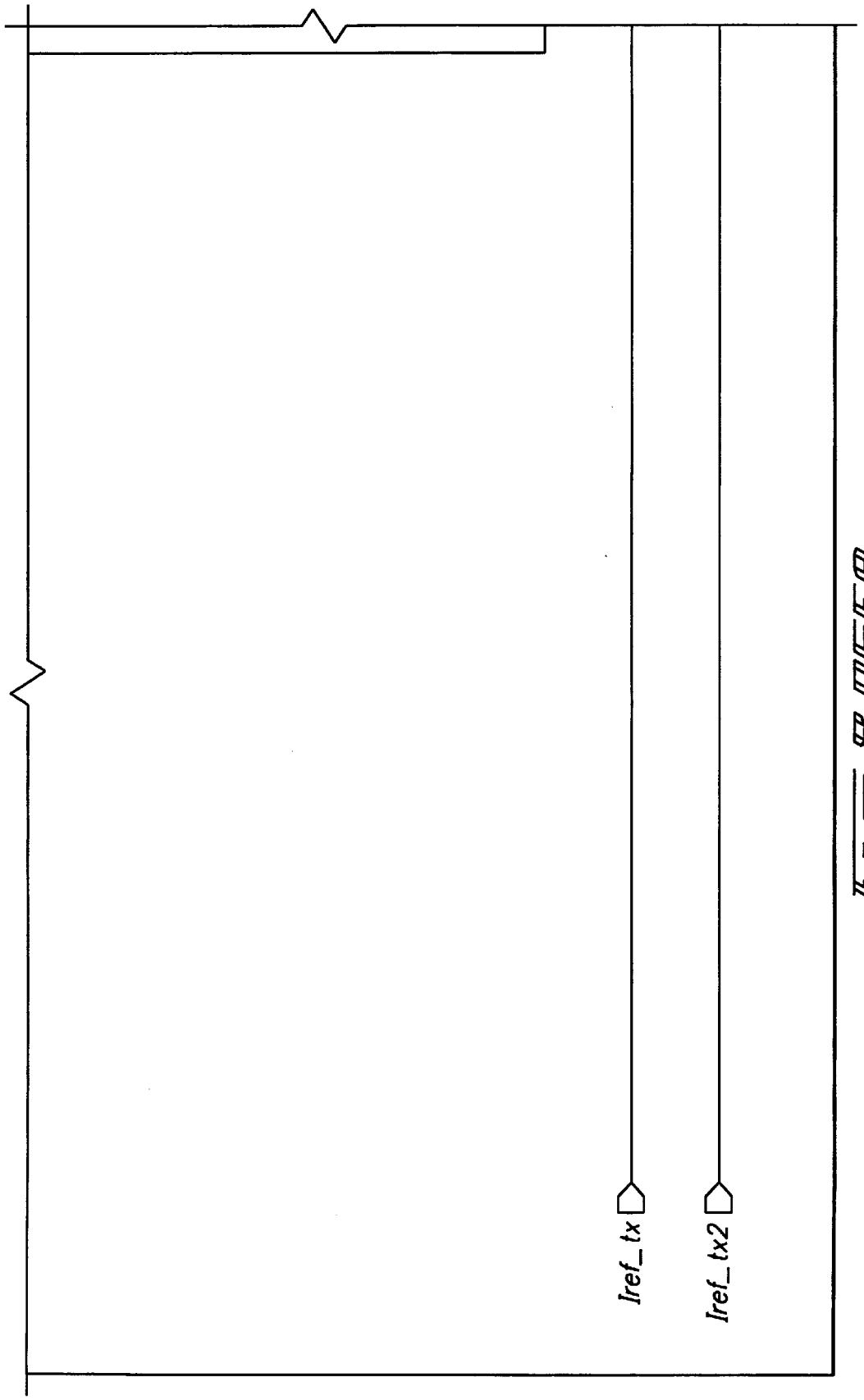


FIG 88.0654

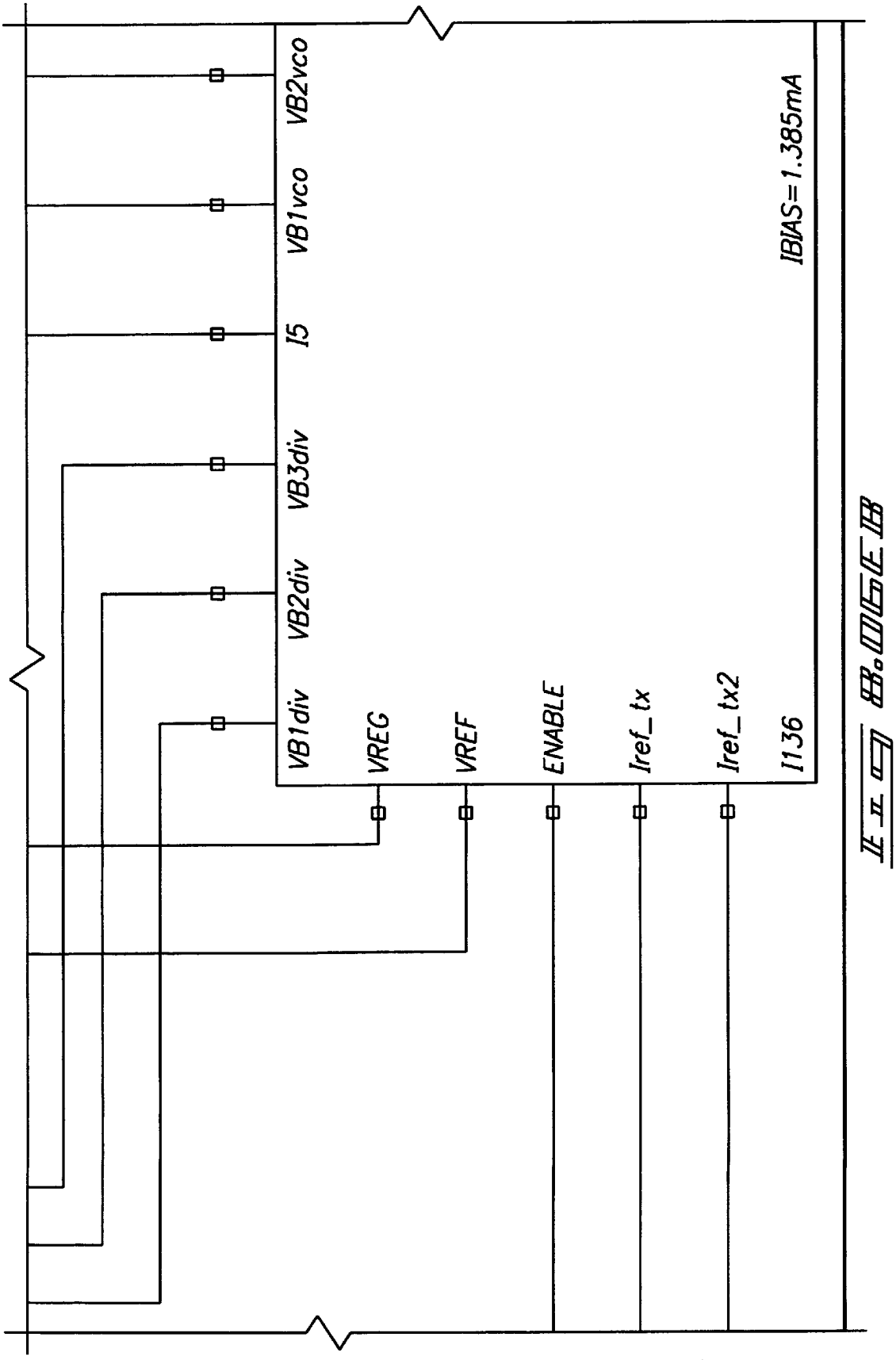
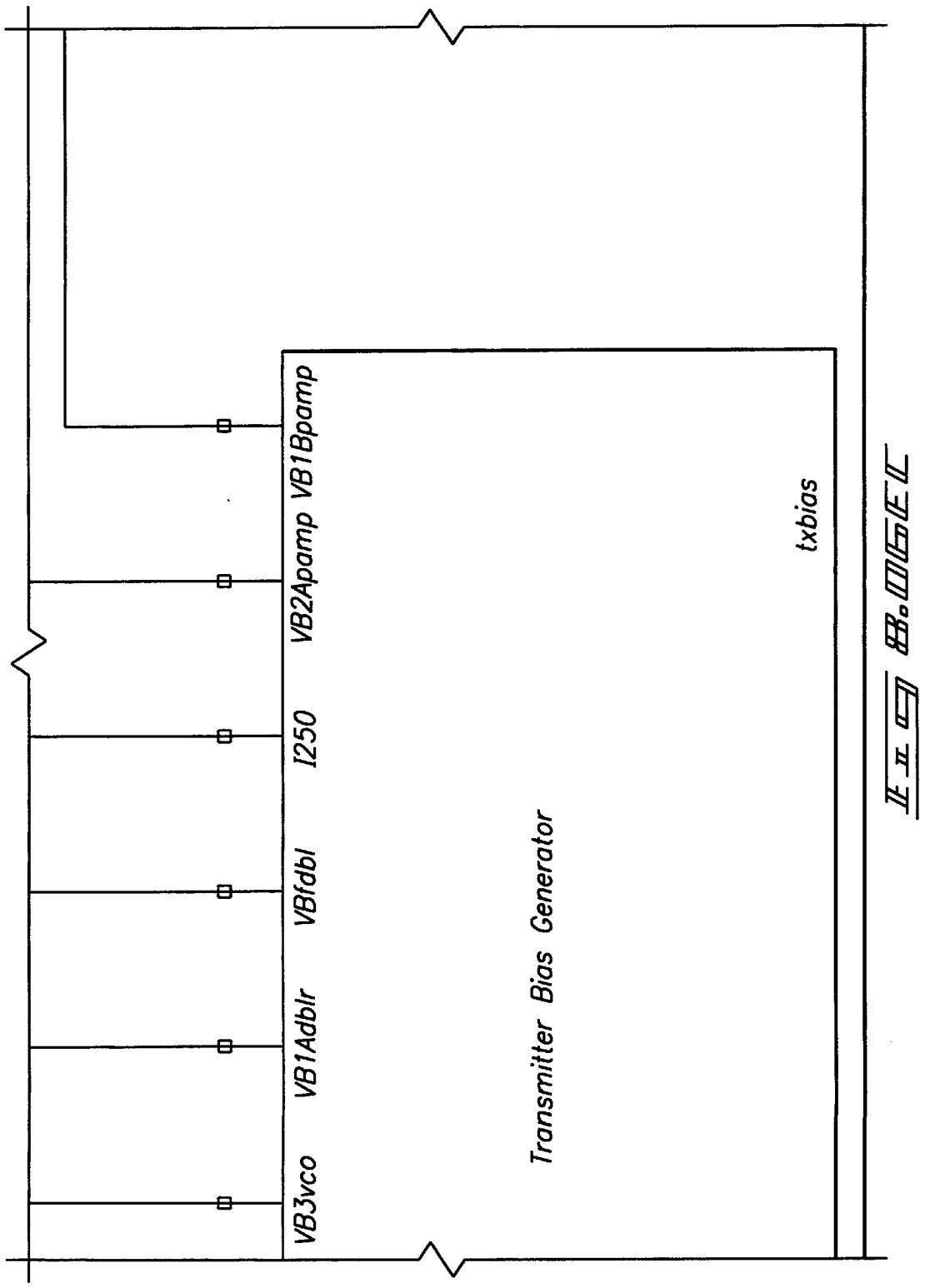

VB2vco
VB1vco
I5
VB3div
VB2div
VB1div
VREG
VREF
ENABLE
Iref_tx
Iref_tx2
I136
IBIAS=1.385mA

FIG. 88.00516


VB3vco
VB1Adblr
VBfdbl
I250
VB2Apamp
VB1Bpamp
Transmitter Bias Generator
txbias

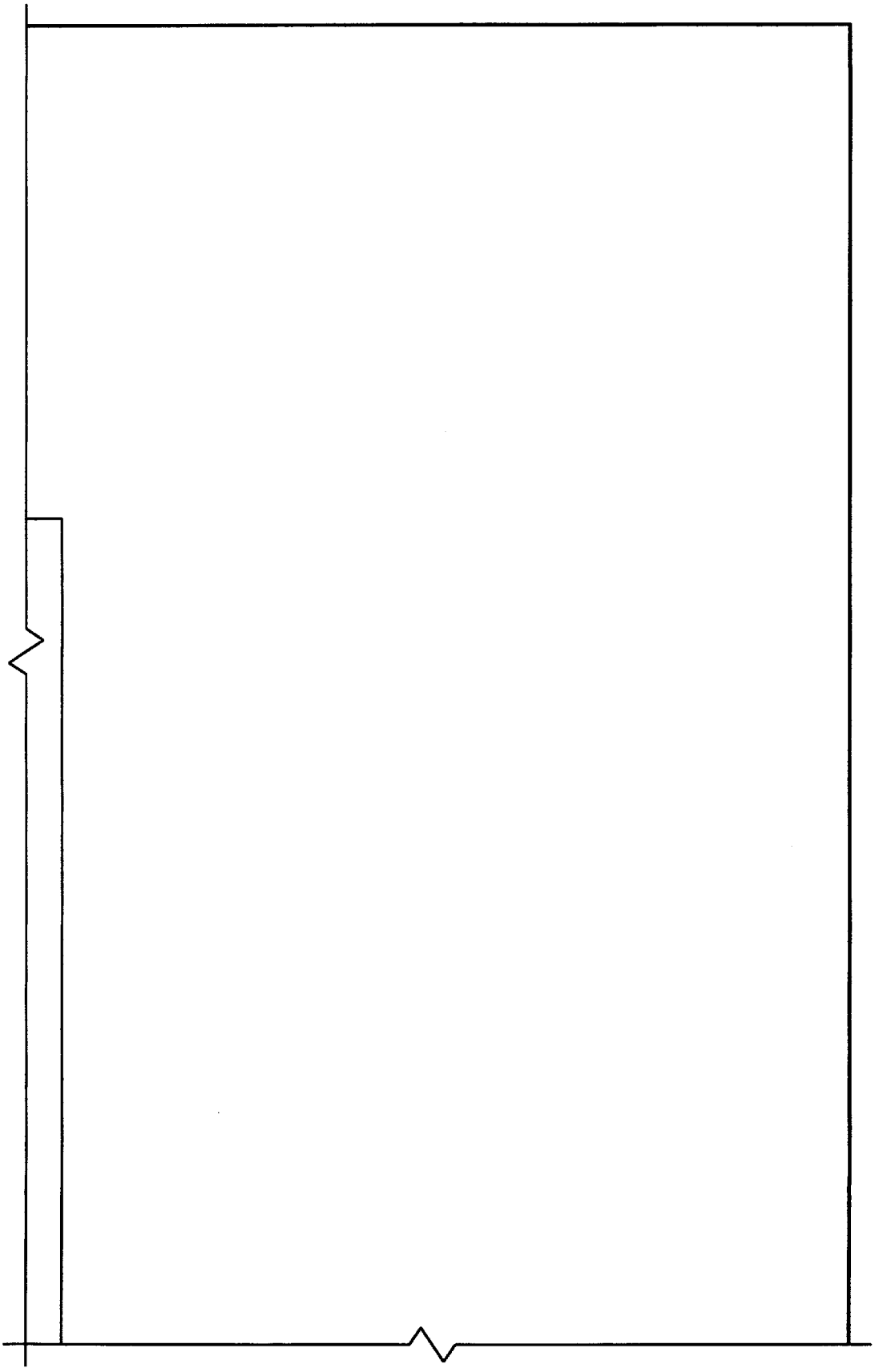


FIG. 88,065D

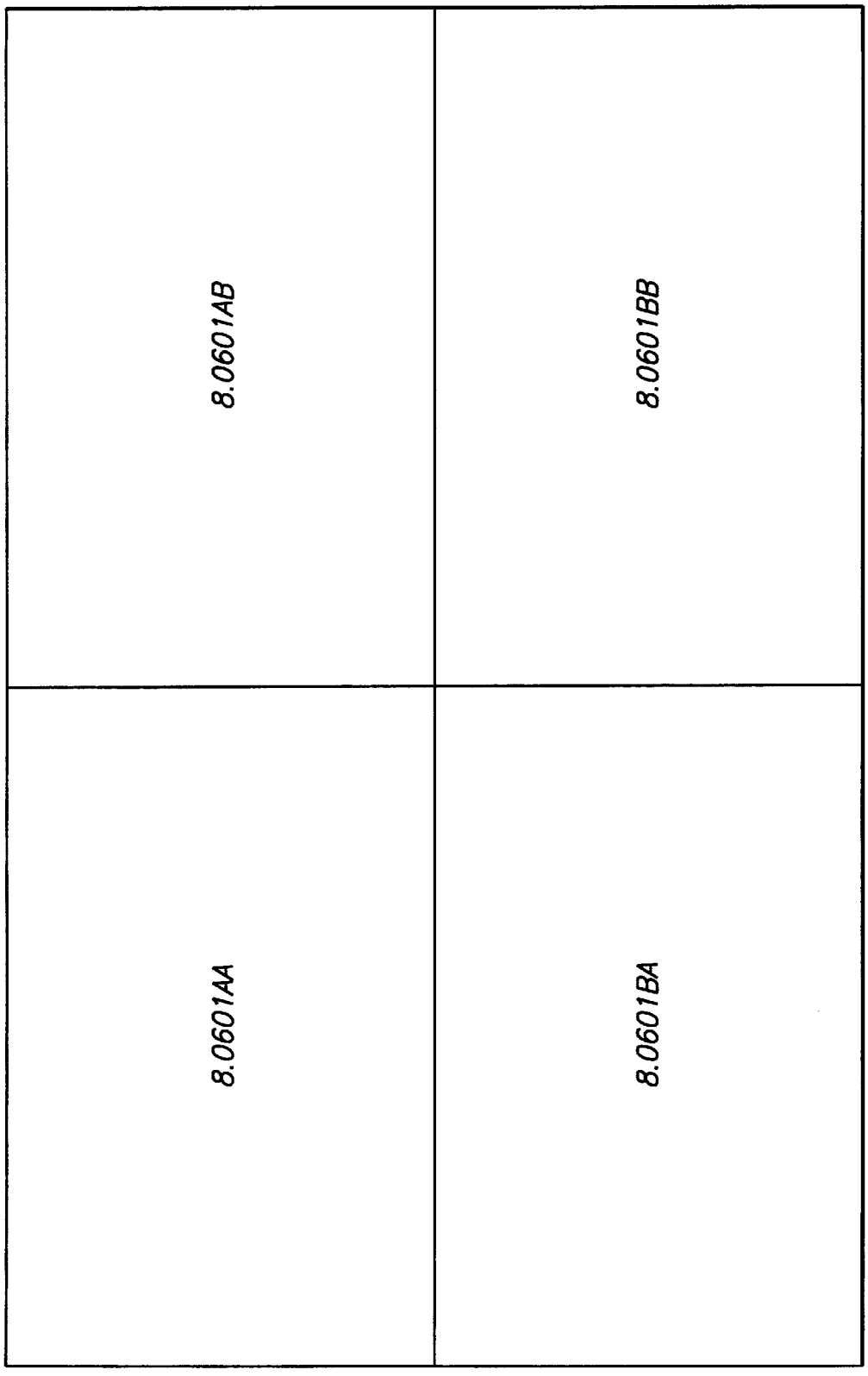


FIG 8.0601

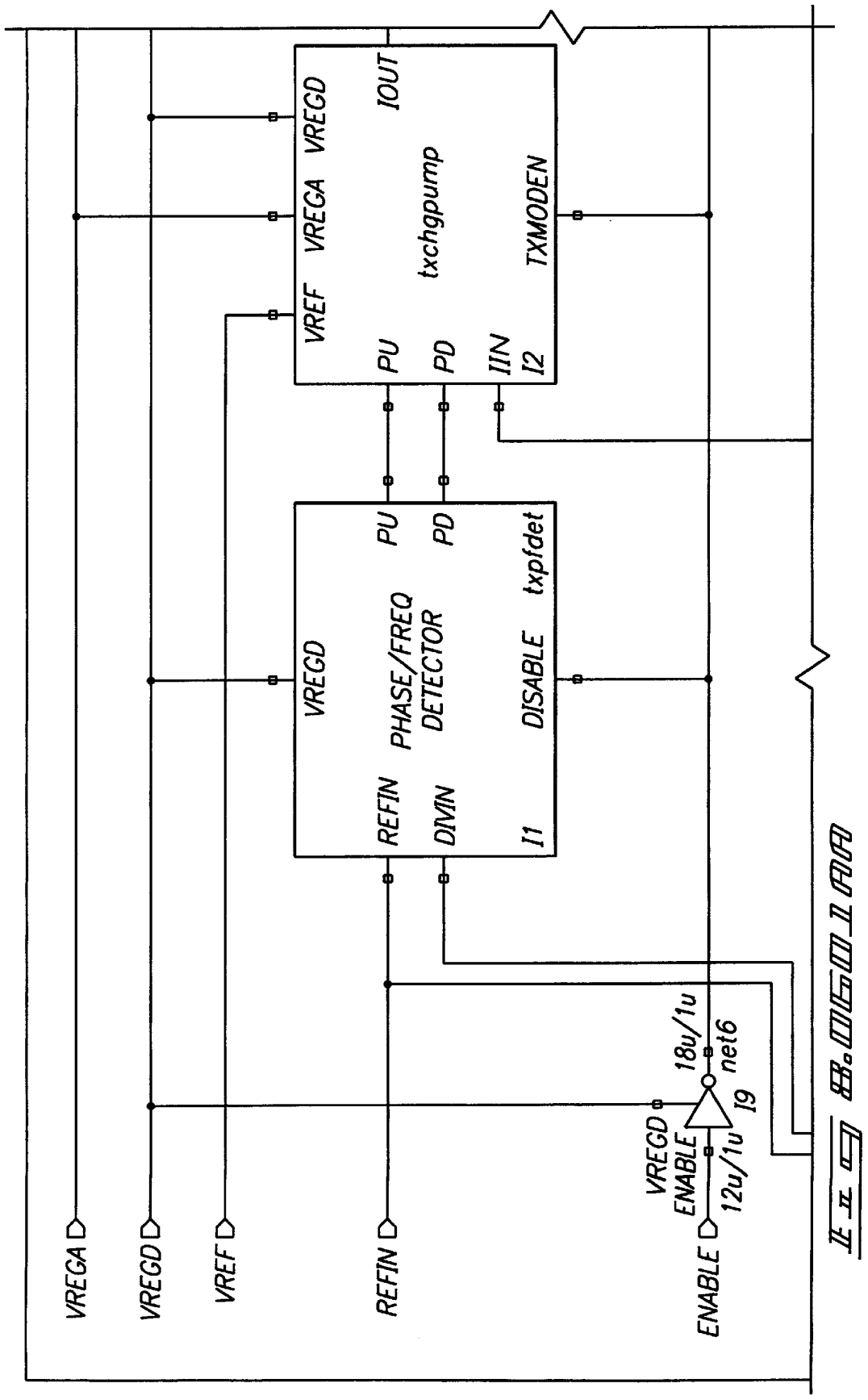
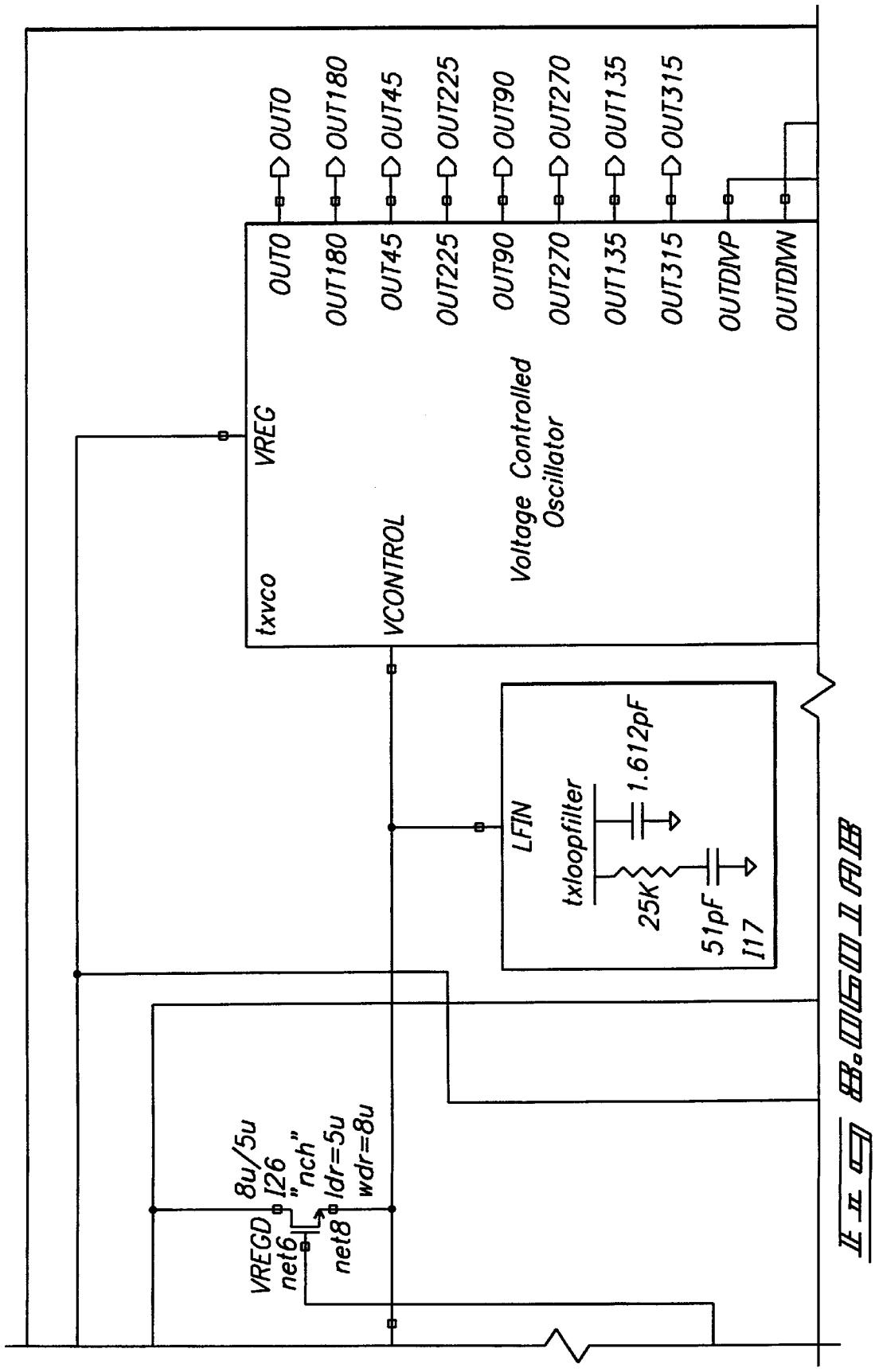


FIG 89.0050011A


OUT0
OUT180
OUT45
OUT225
OUT90
OUT270
OUT135
OUT315
OUTDVP
OUTDVN
VREG
VCONTROL
txvco
Voltage Controlled Oscillator
LFIN
txloopfilter
1.612pF
25K
51pF
I17
8u/5u
I26
"nch"
ldr=5u
wdr=8u
VREGD
net6
net8

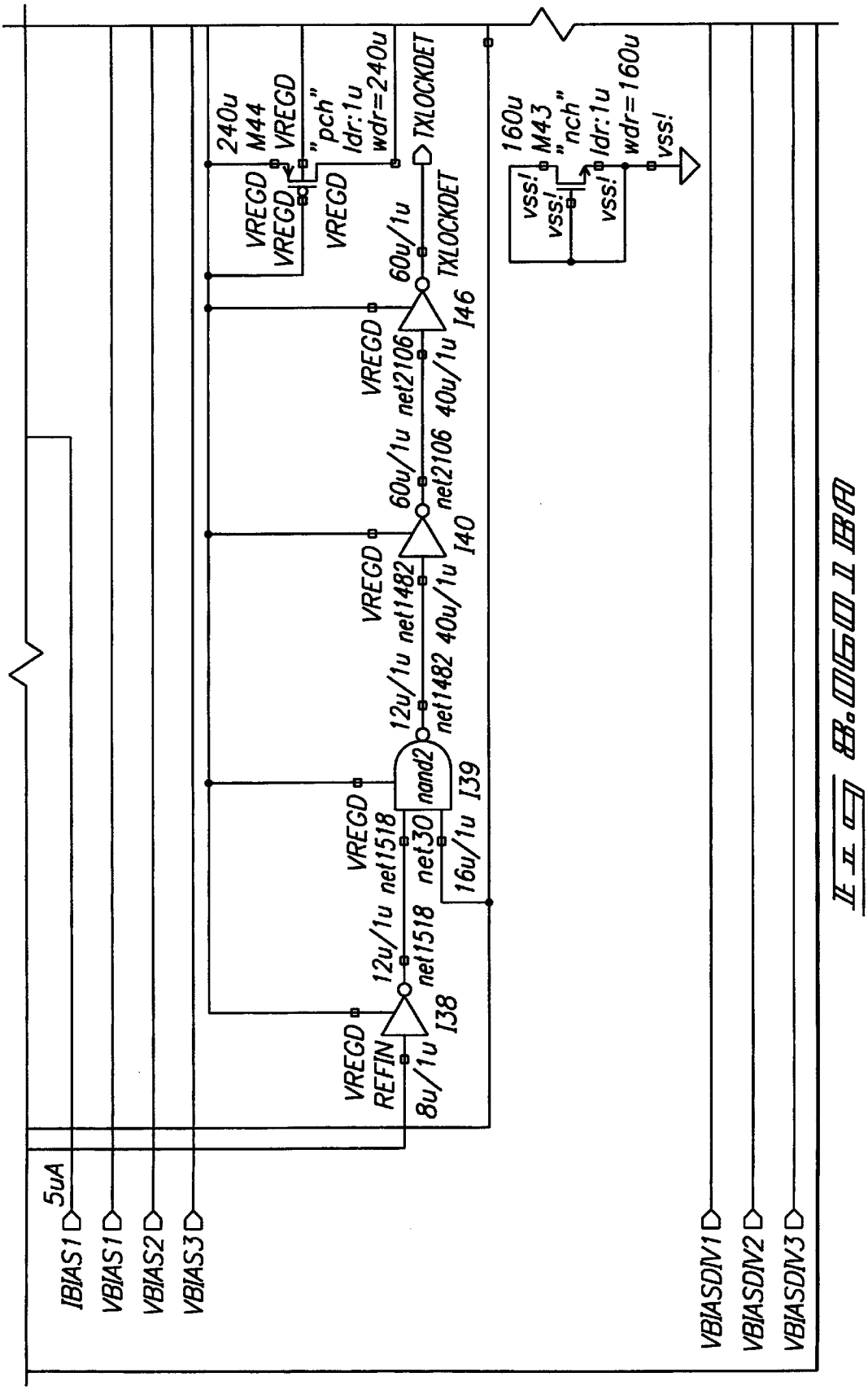

IBIAS1
5uA
VBIAS1
VBIAS2
VBIAS3
VBIASDIV1
VBIASDIV2
VBIASDIV3
VREGD
REFIN
8u/1u
I38
12u/1u
net1518
nand2
net30
16u/1u
I39
net1482
40u/1u
I40
net2106
60u/1u
I46
TXLOCKDET
240u
M44
"pch"
ldr:1u
wdr=240u
160u
M43
"nch"
wdr=160u
vss!

FIG. 88.0050

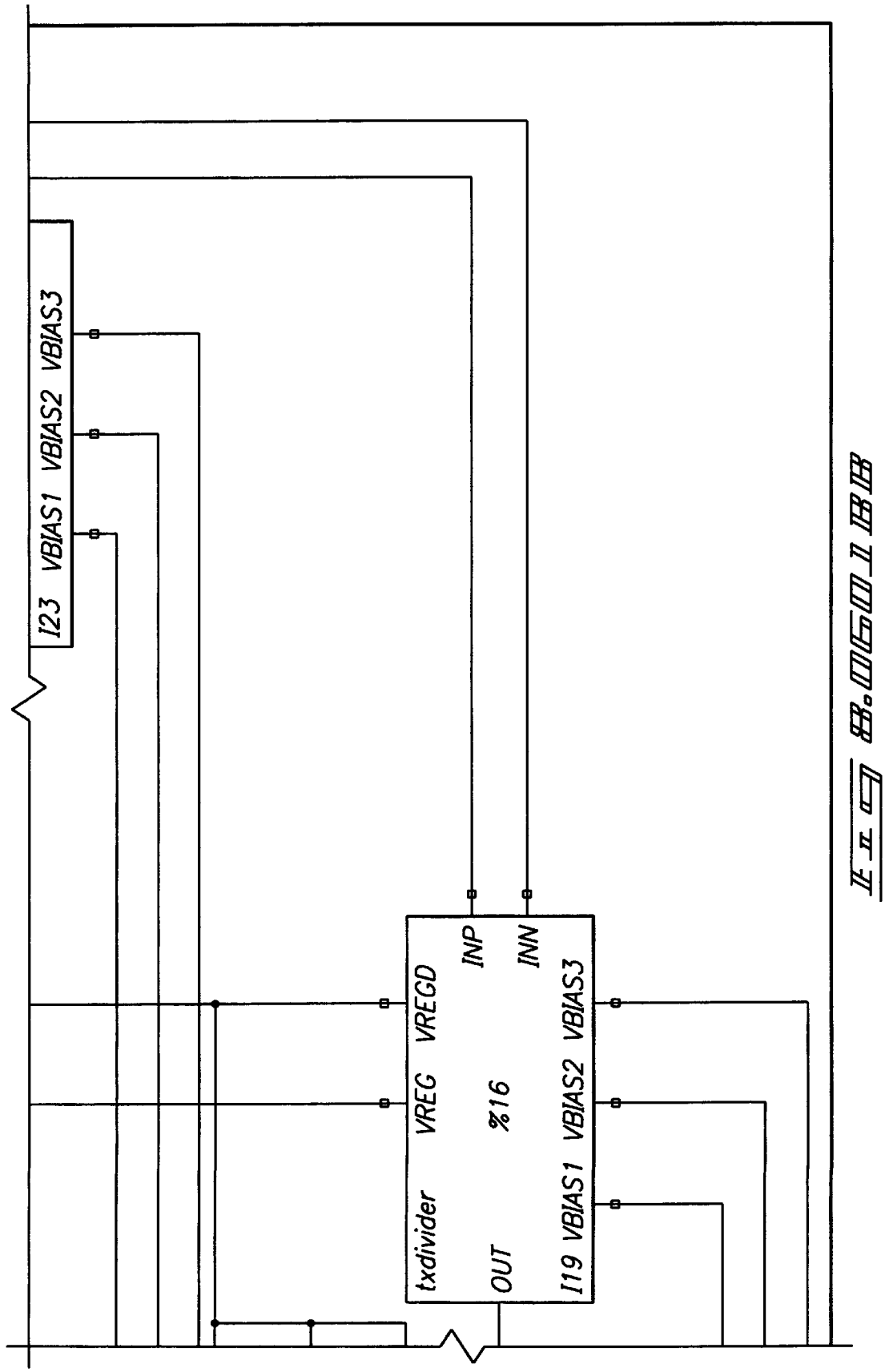

I23 VBIAS1 VBIAS2 VBIAS3
txdivider VREG VREGD
OUT
%16
INP INN
I19 VBIAS1 VBIAS2 VBIAS3

FIG. 6,130,602

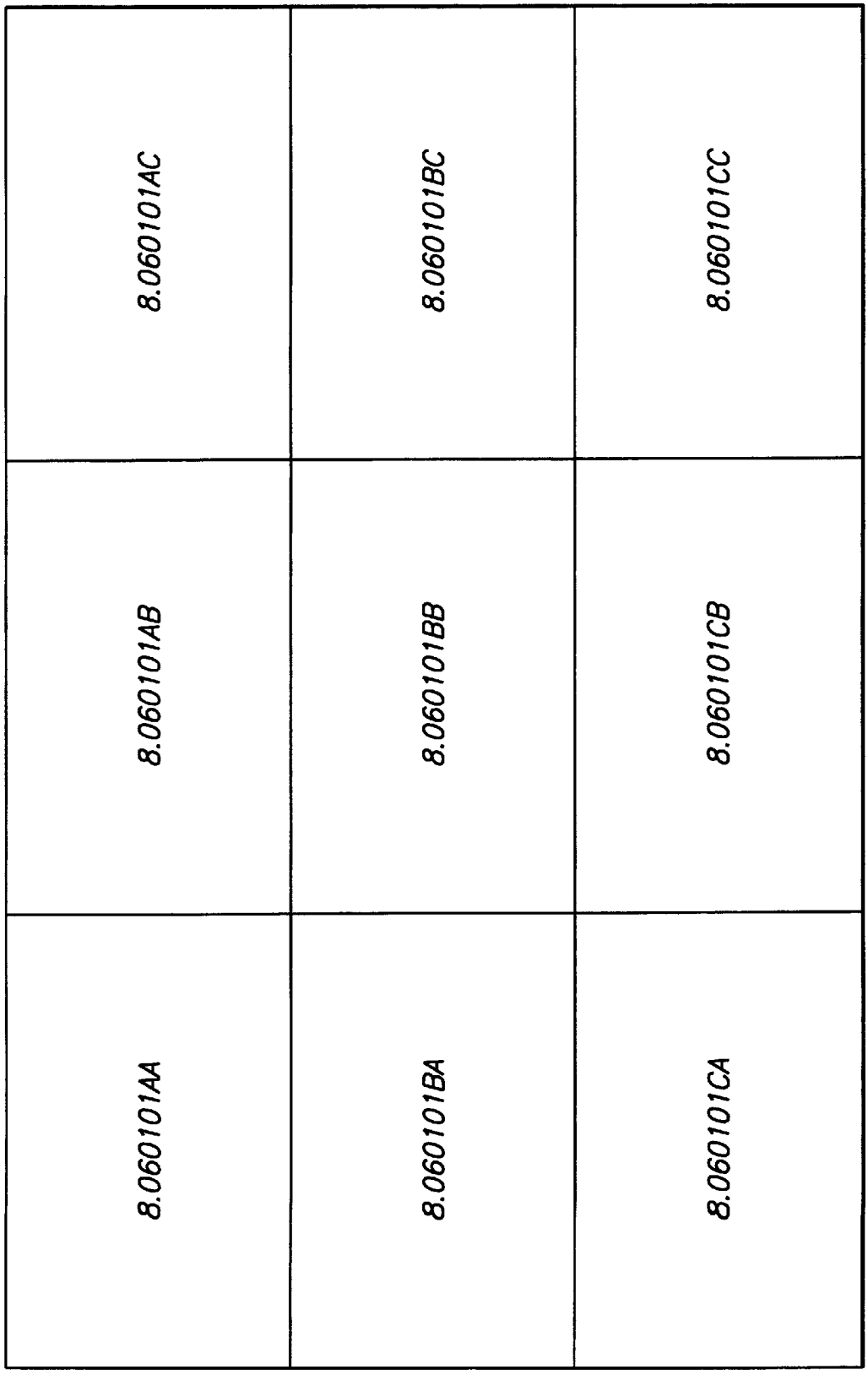

8.060101AC
8.060101BC
8.060101CC
8.060101AB
8.060101BB
8.060101CB
8.060101AA
8.060101BA
8.060101CA

FIG 8.060101

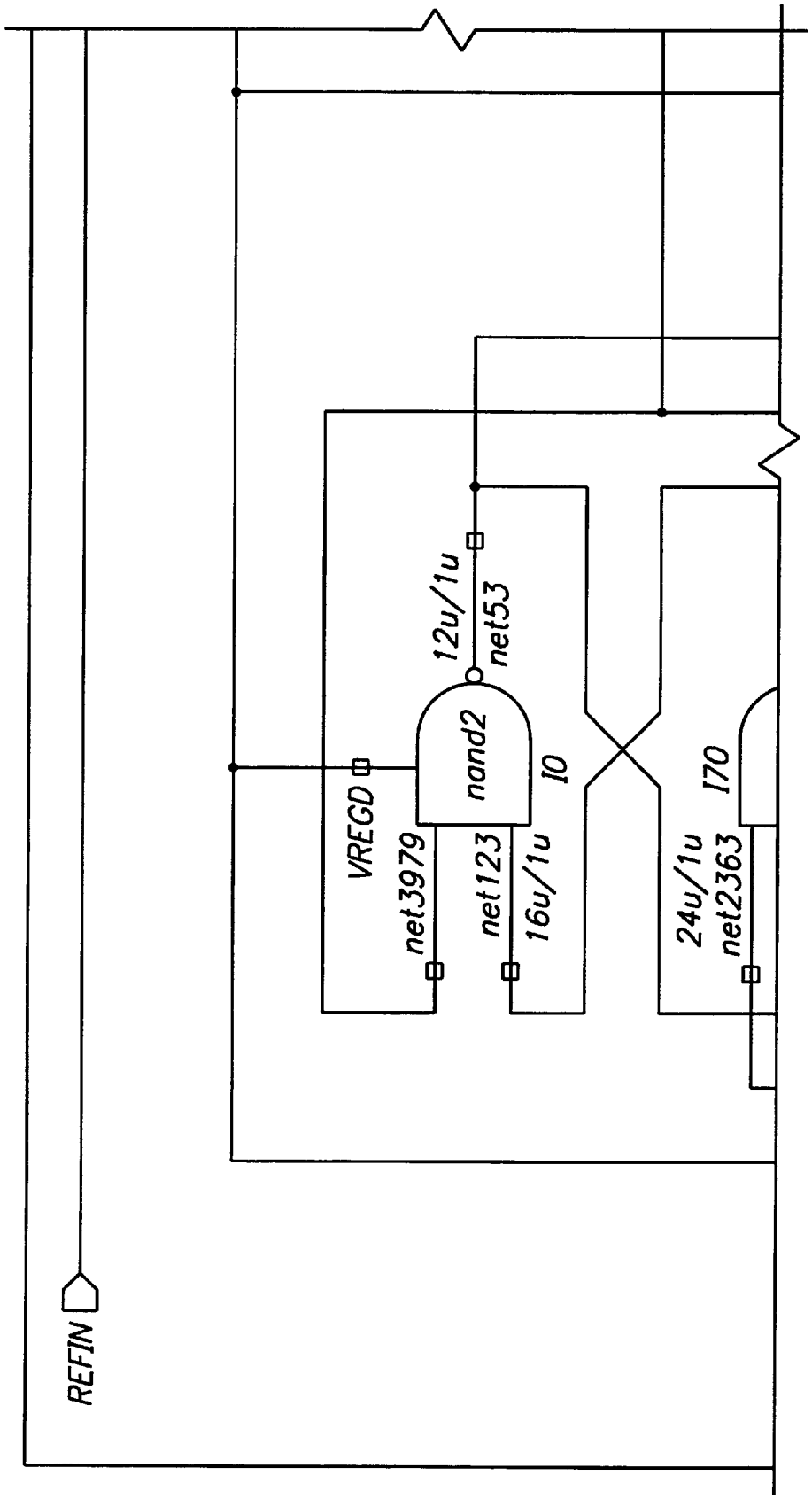


FIG 88.0050011AA

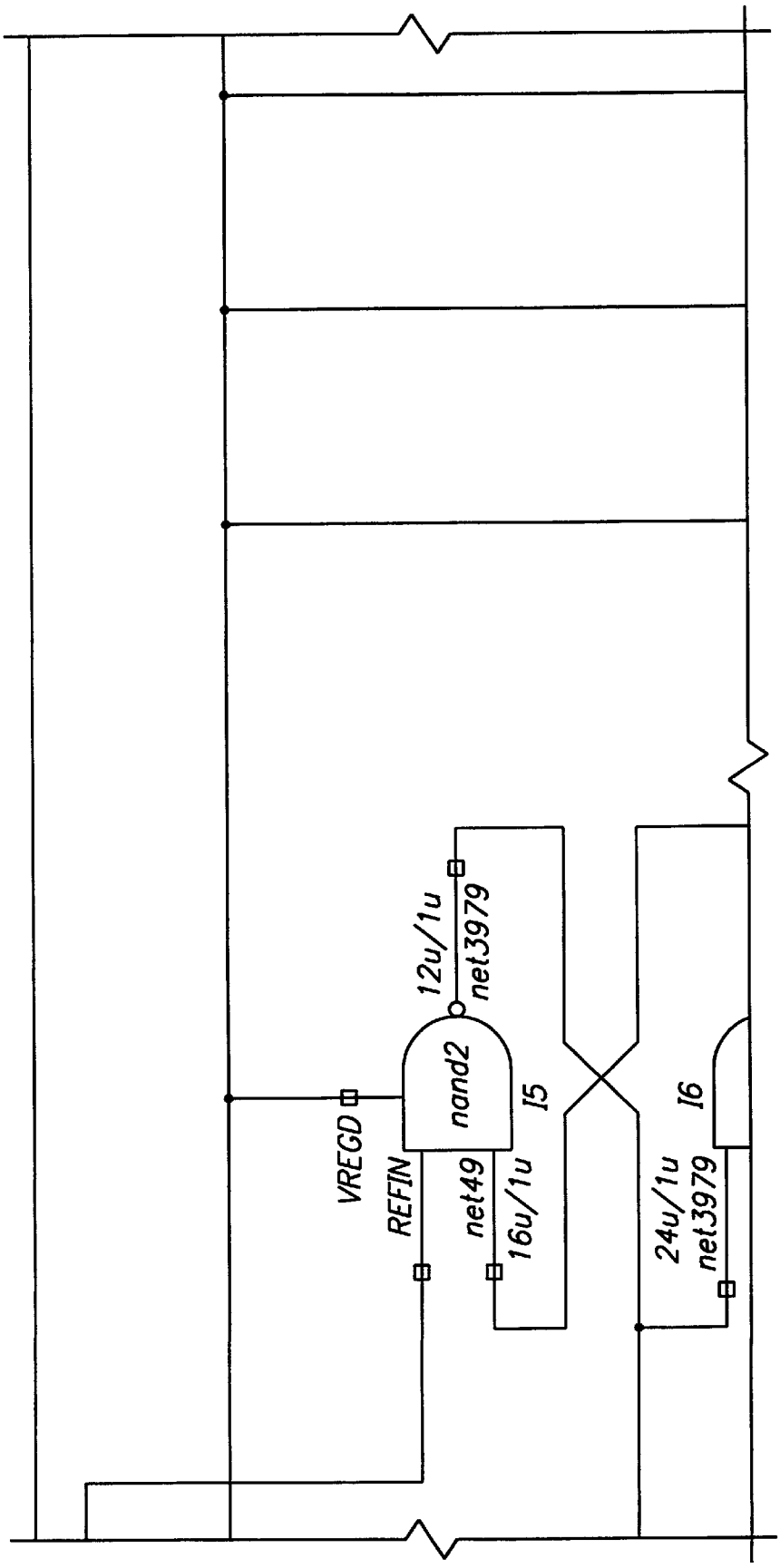
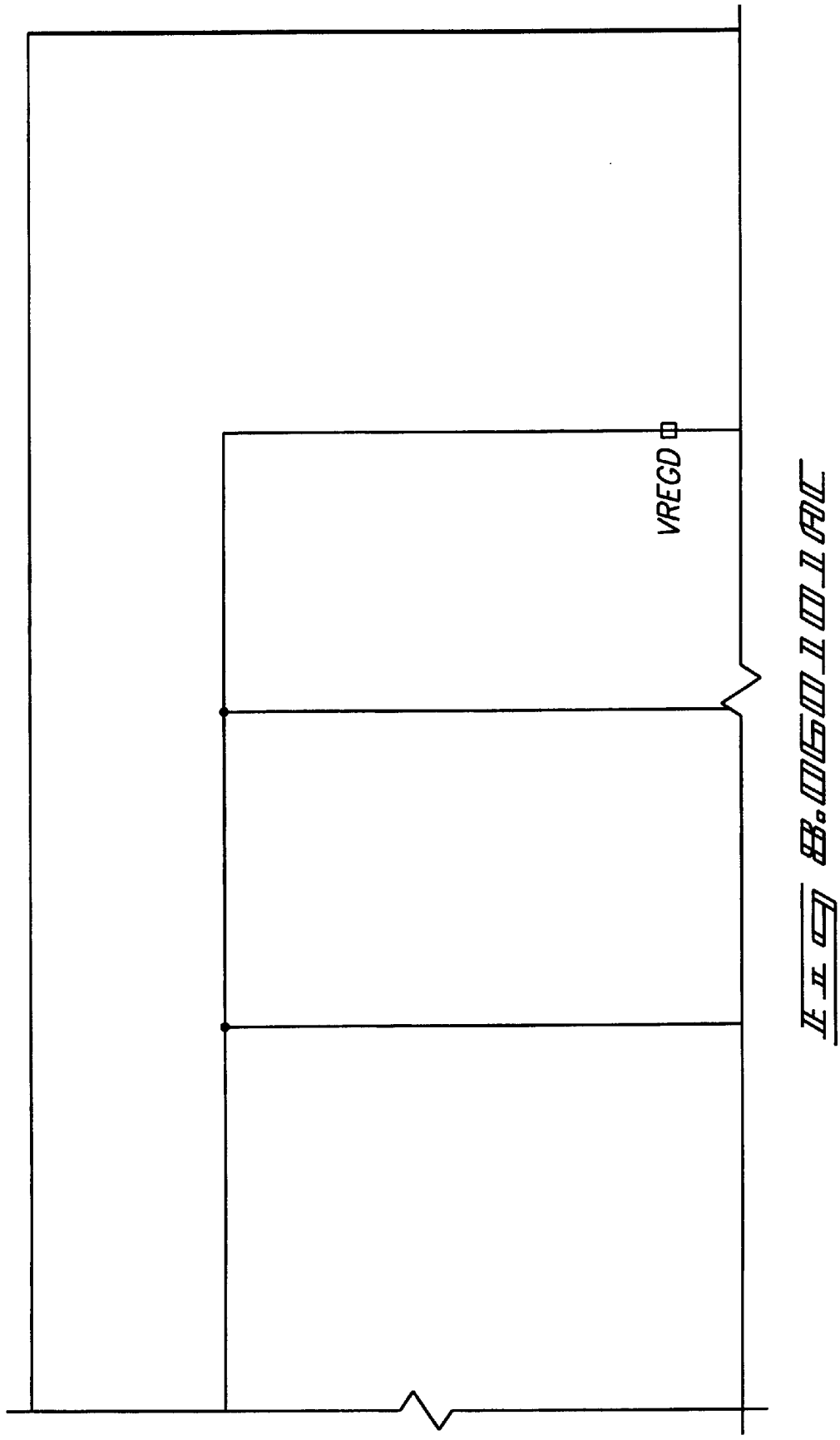


FIG. 88.0501101AB


VREGD
FIG 98,050

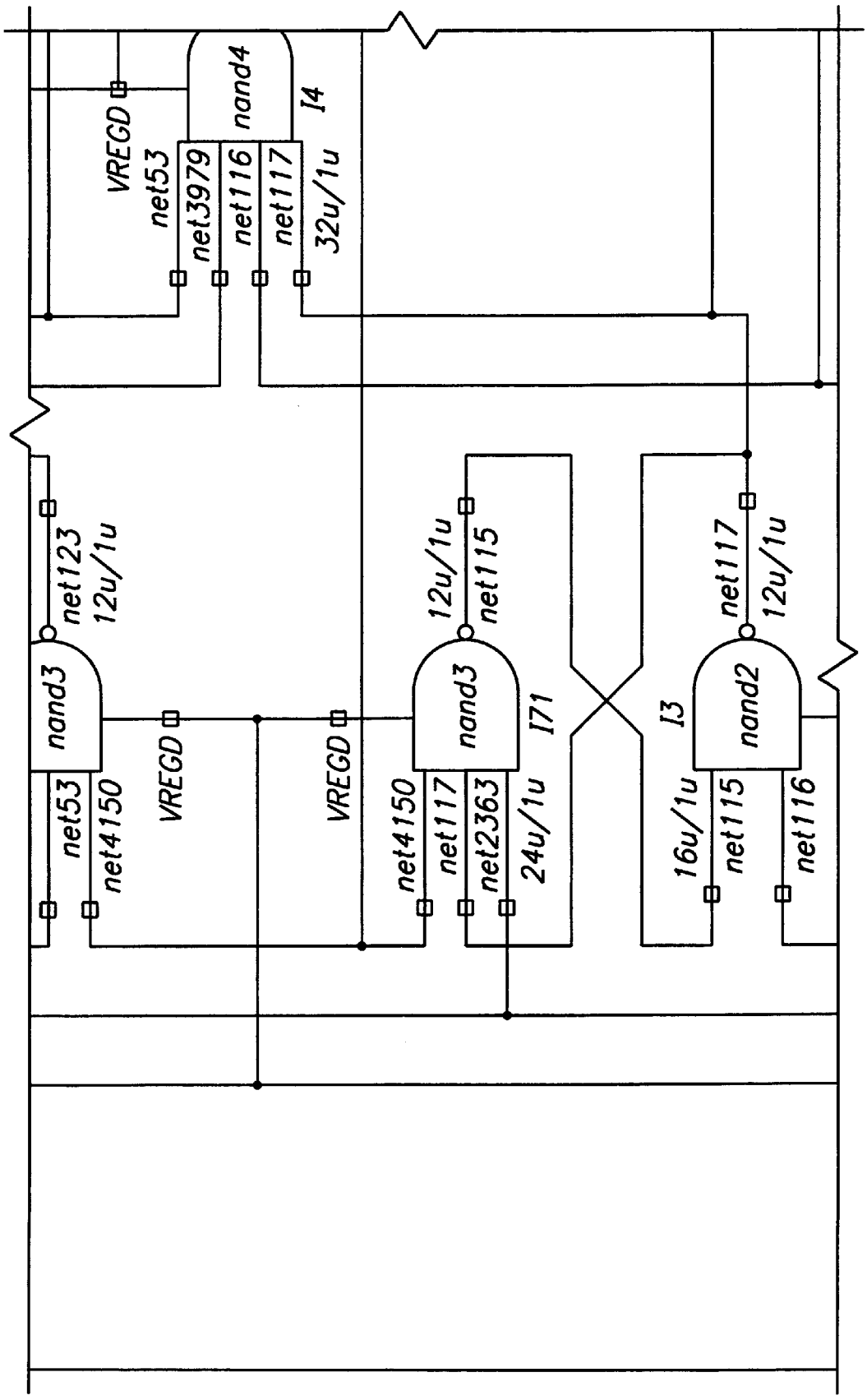


FIG. 88.00611.1884

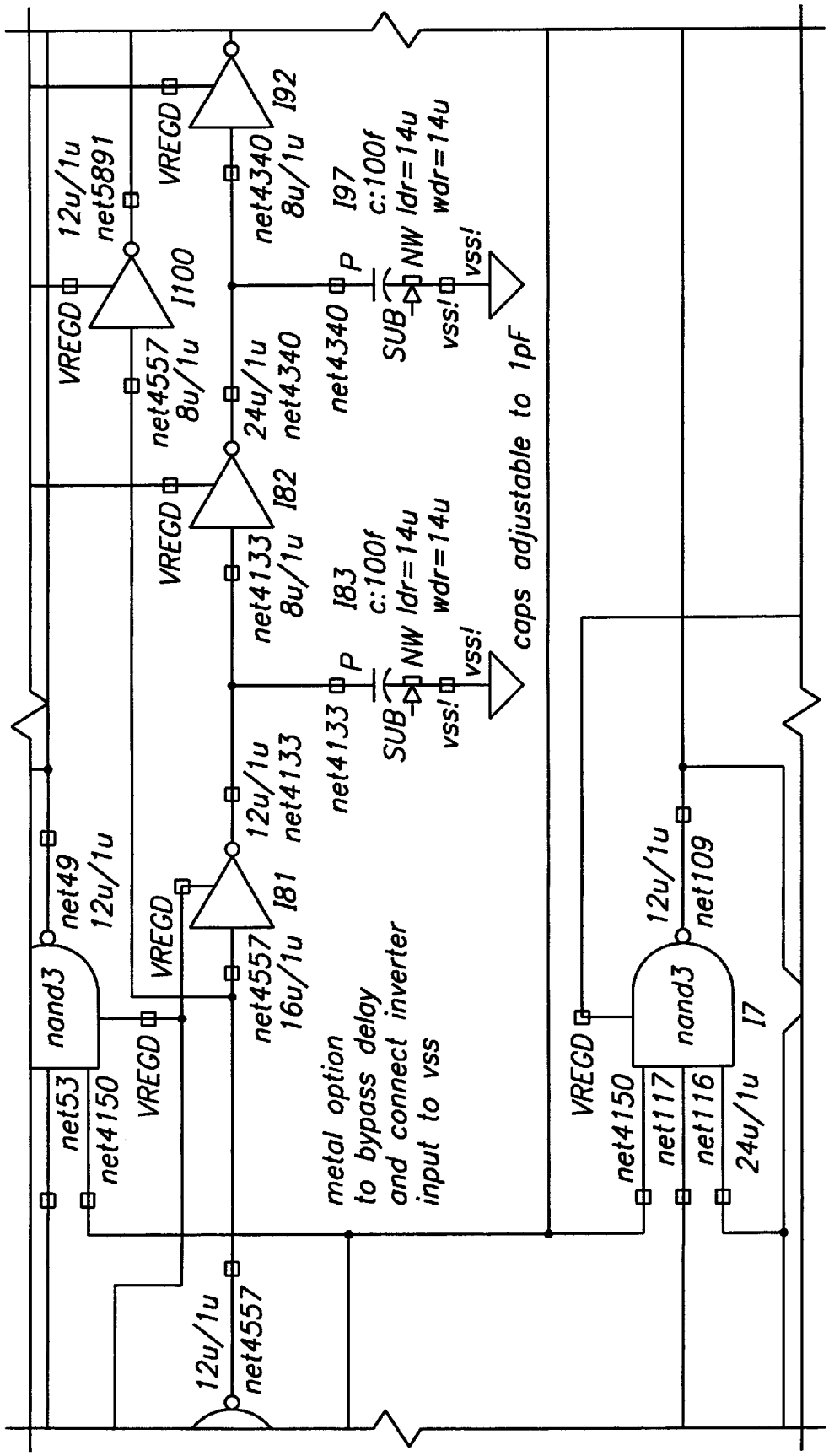

VREGD
12u/1u
net5891
I92
net4340
8u/1u
I97
c:100f
ldr=14u
wdr=14u
I100
net4557
8u/1u
24u/1u
net4340
P
NW
SUB
vss!
I82
net4133
I83
caps adjustable to 1pF
nand3
net49
I81
net4150
net53
net109
net117
net116
I7
metal option
to bypass delay
and connect inverter
input to vss

FIG. 88.0056

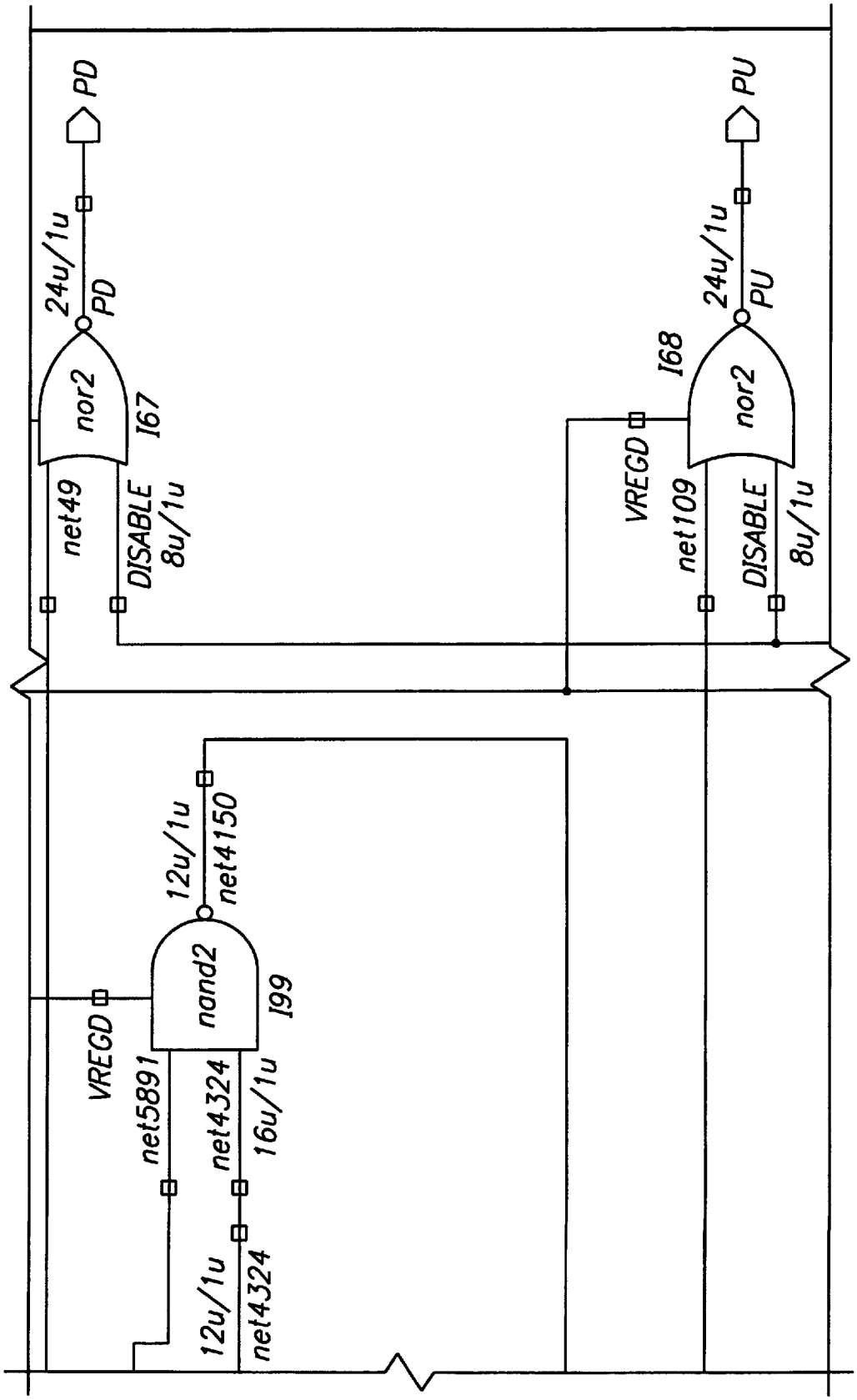


FIG 88.0600 I00 I IBC

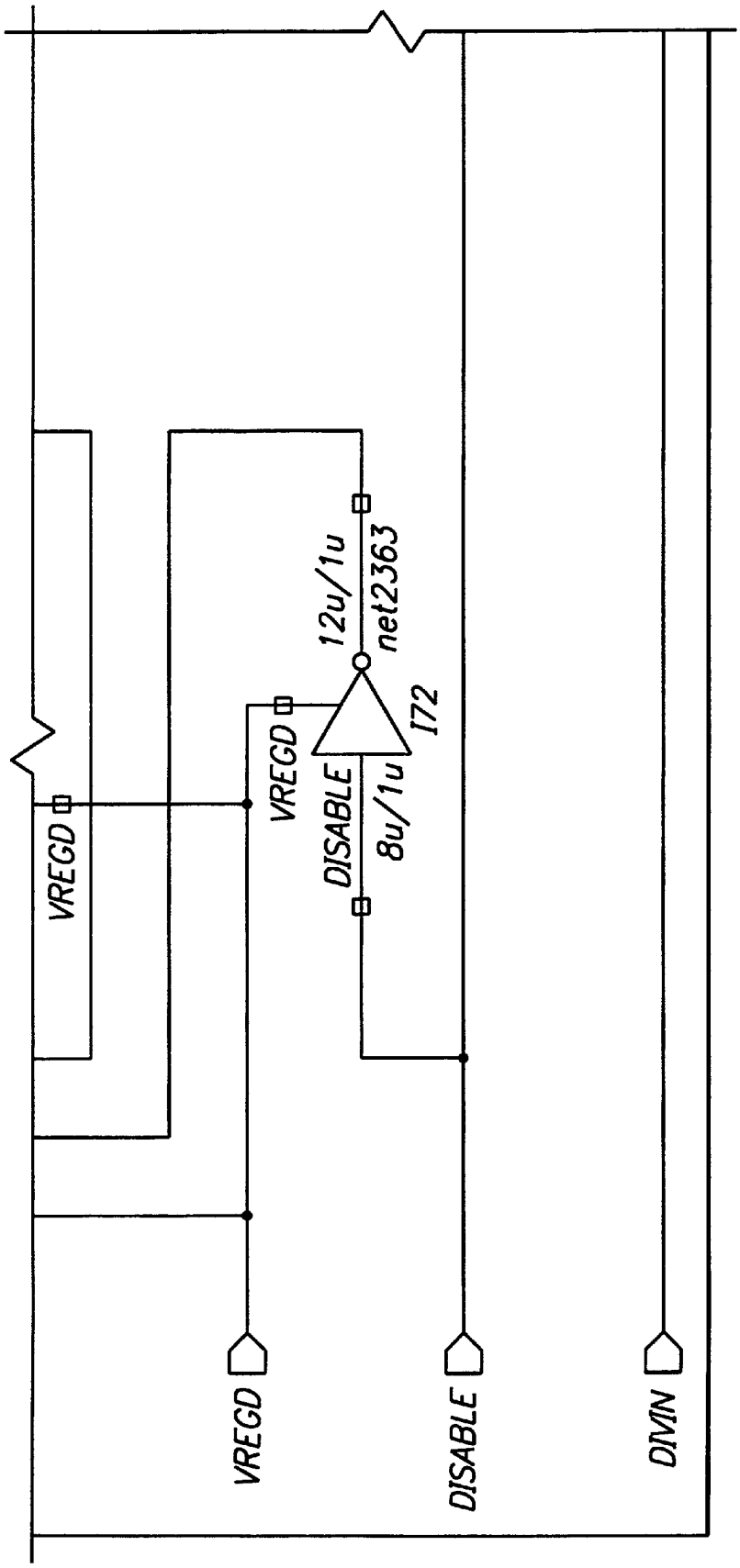


FIG 88.0501101CA

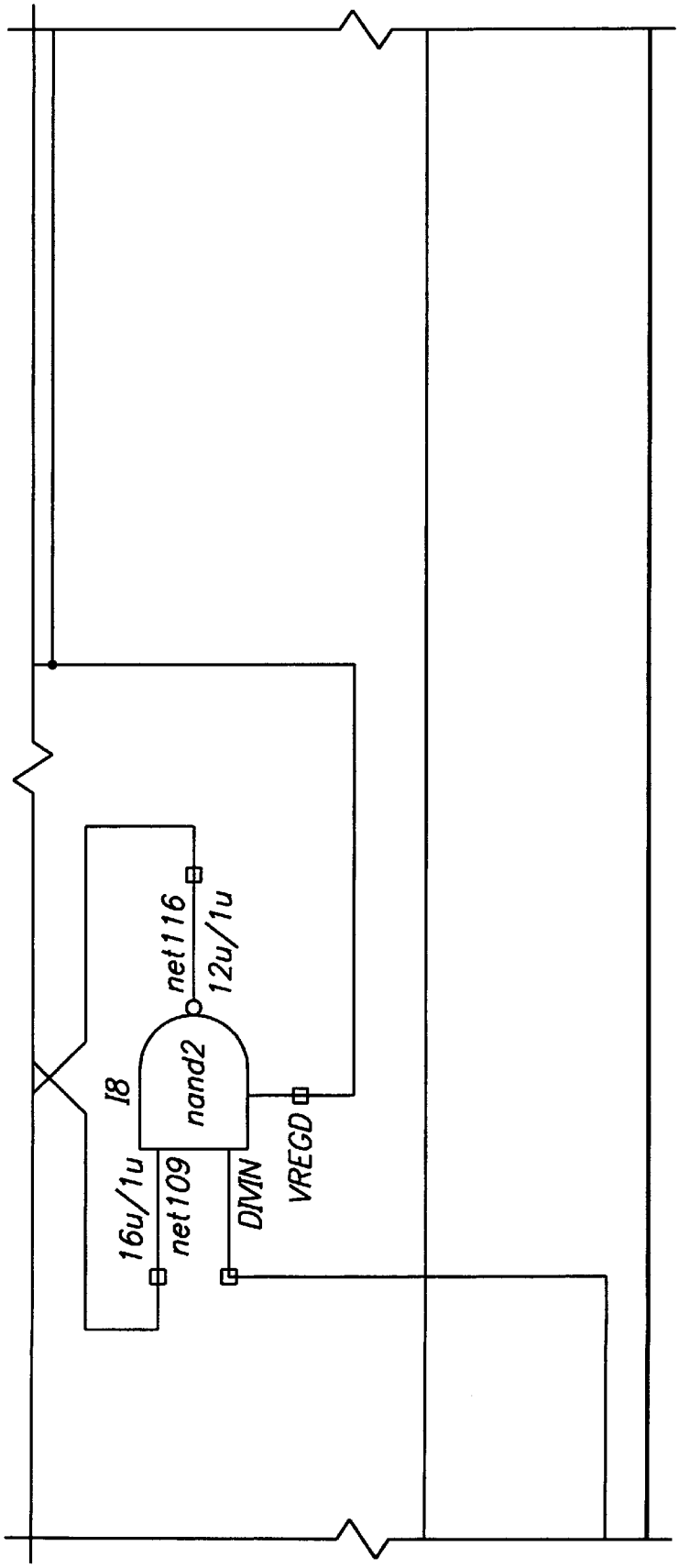


FIG 88.0501IC1B

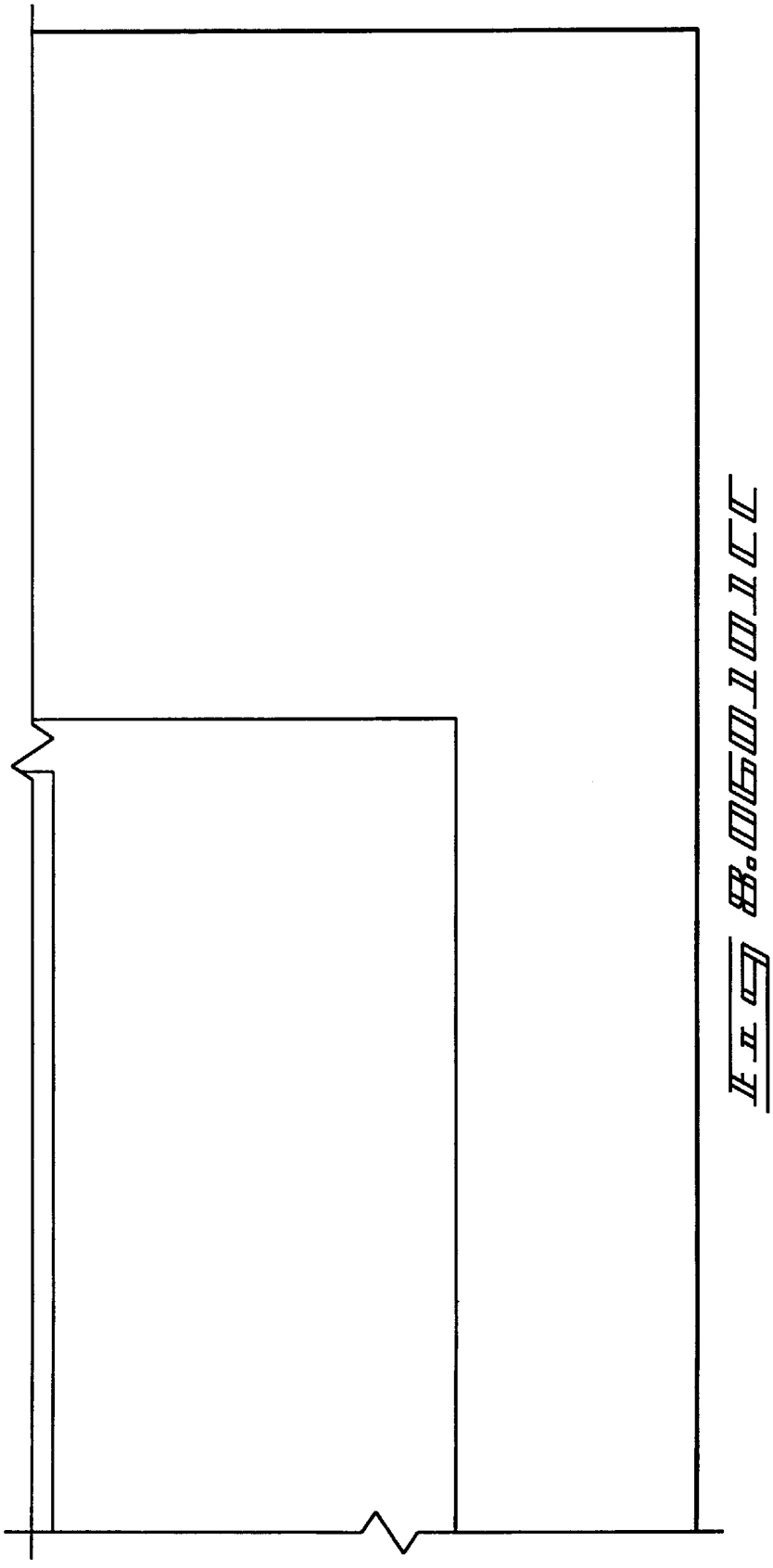


FIG 98.00500A

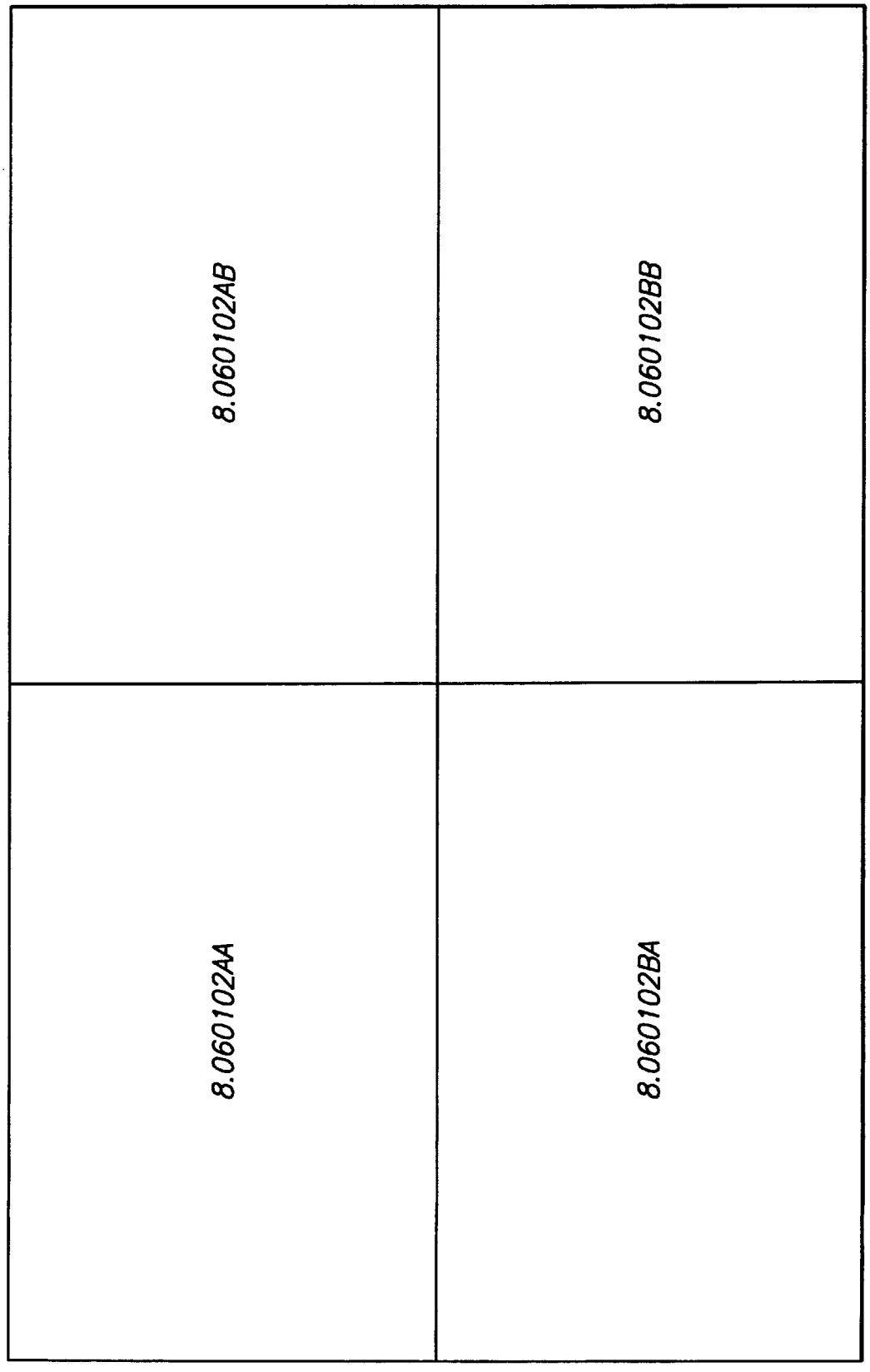


FIG 8.060102

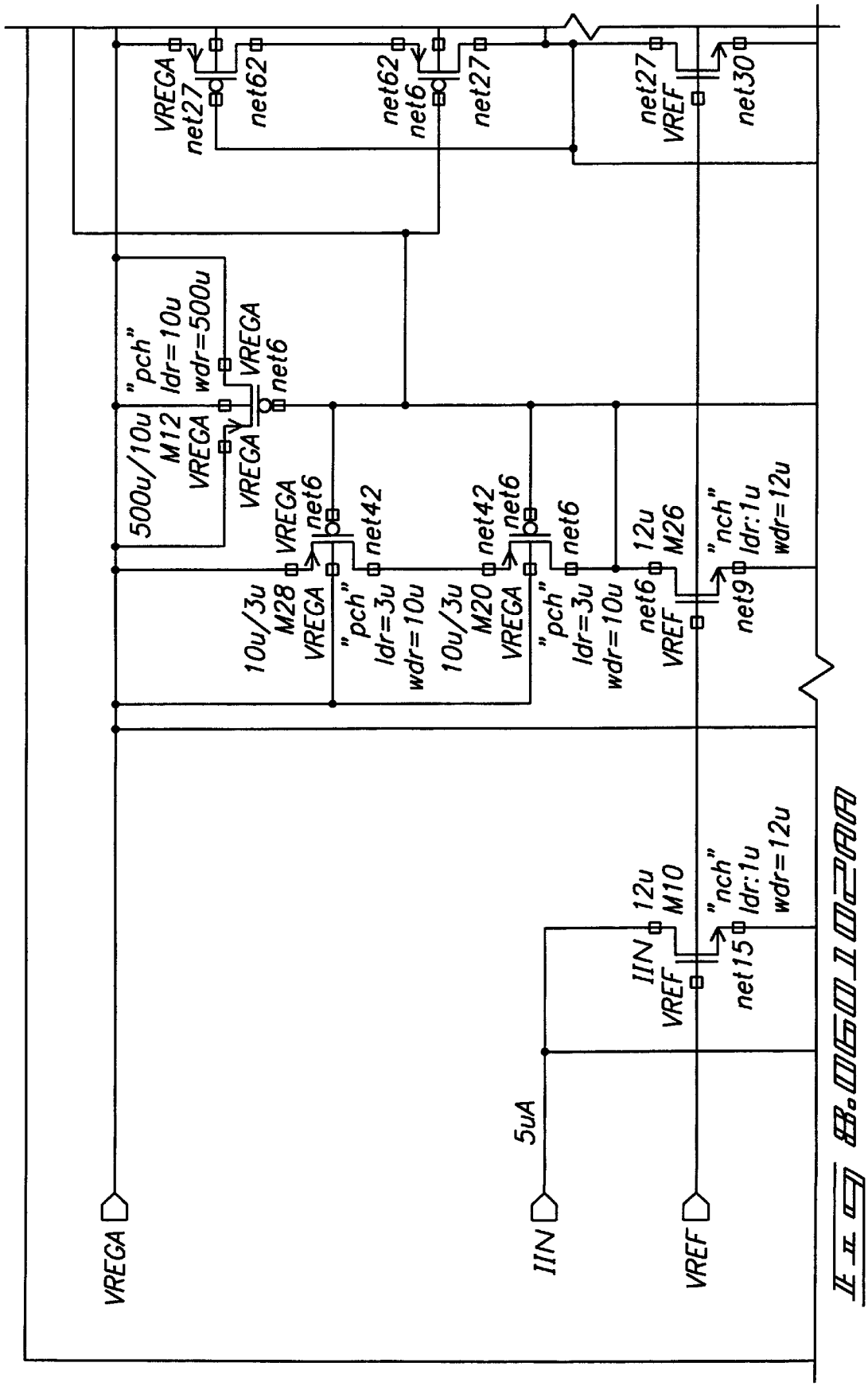
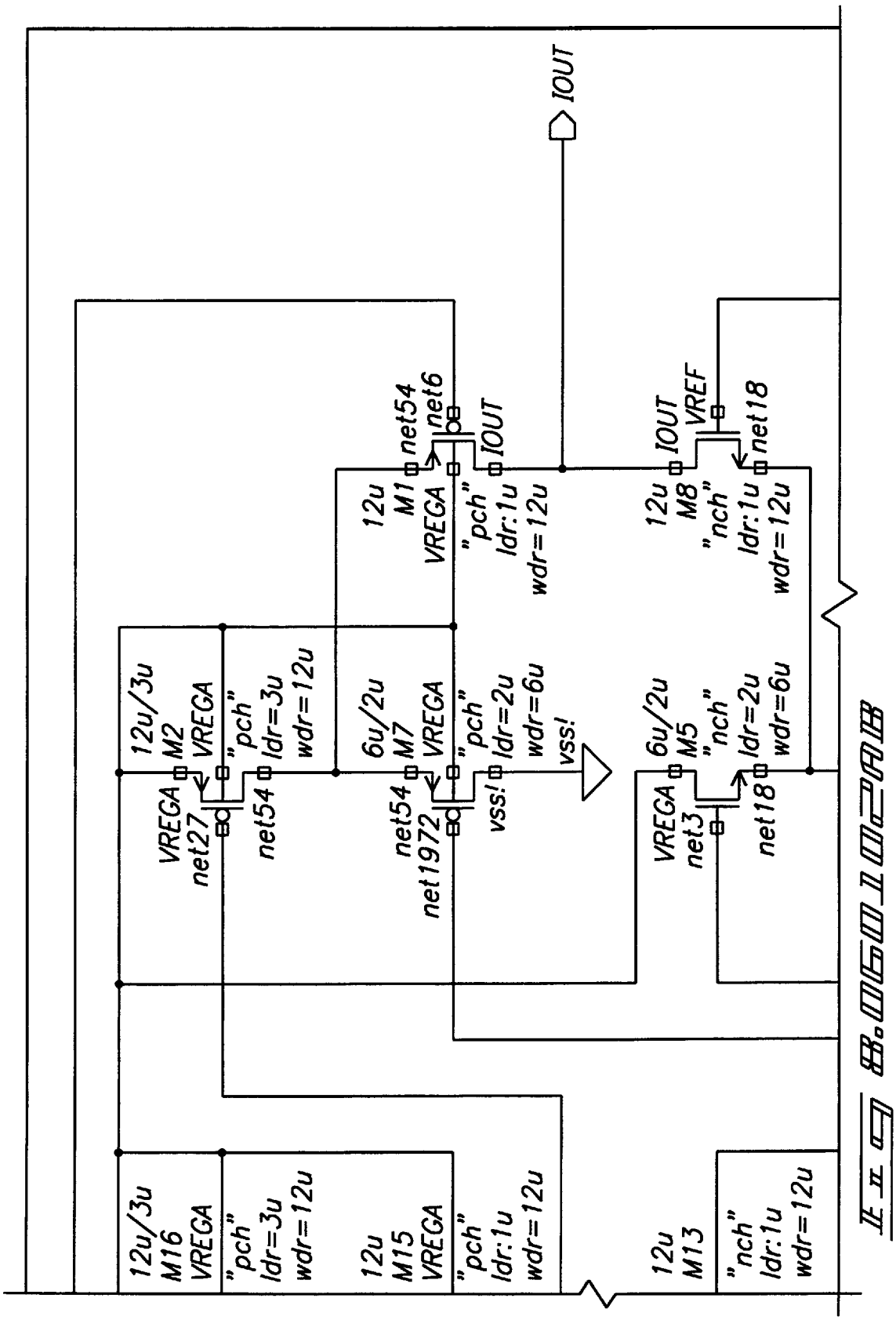


Fig. 8.0501 00AA


IOUT
12u
M1
VREGA
net54
net6
IOUT
"pch"
ldr:1u
wdr=12u
12u
M8
"nch"
ldr:1u
wdr=12u
IOUT
VREF
net18
12u/3u
M2
VREGA
VREGA
net27
"pch"
ldr=3u
wdr=12u
net54
6u/2u
M7
VREGA
net54
net1972
"pch"
ldr=2u
wdr=6u
vss!
vss!
6u/2u
M5
"nch"
ldr=2u
wdr=6u
VREGA
net3
net18
12u/3u
M16
VREGA
"pch"
ldr=3u
wdr=12u
12u
M15
VREGA
"pch"
ldr:1u
wdr=12u
12u
M13
"nch"
ldr:1u
wdr=12u

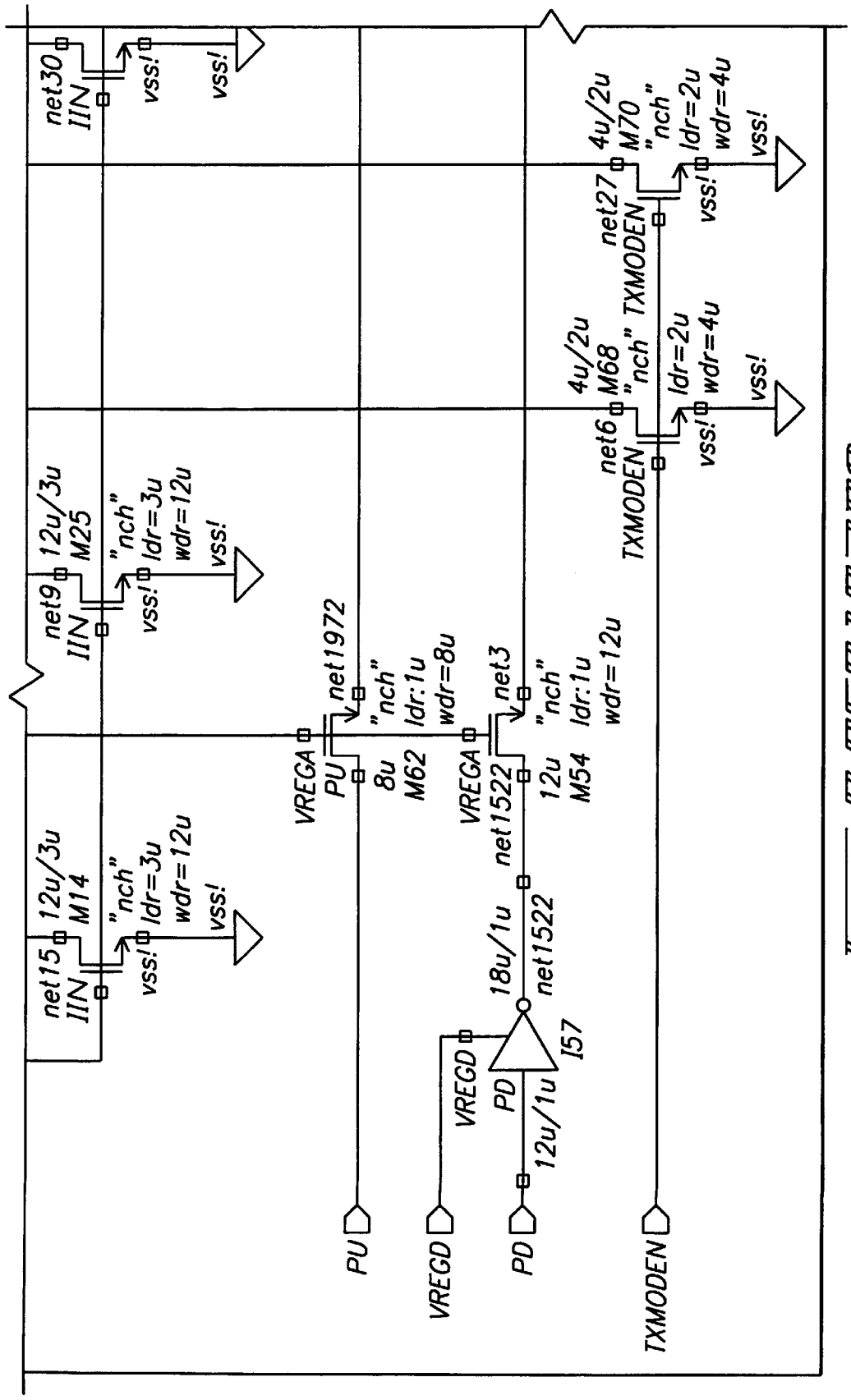


FIG 8.0500 II 00 2BA

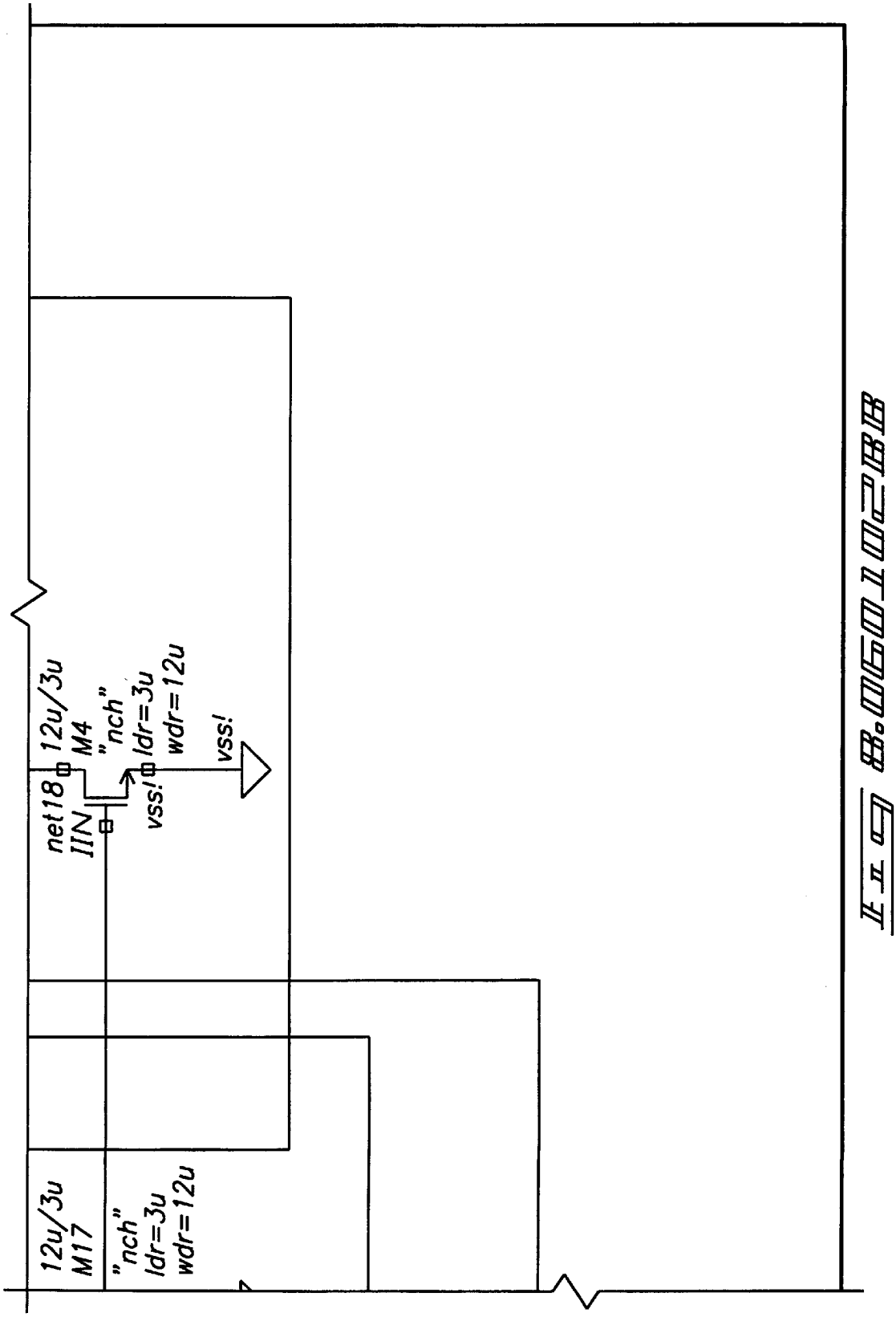


FIG 8,050,018
12u/3u
M17
"nch"
ldr=3u
wdr=12u
net18
IIN
12u/3u
M4
"nch"
ldr=3u
wdr=12u
vss!
vss!

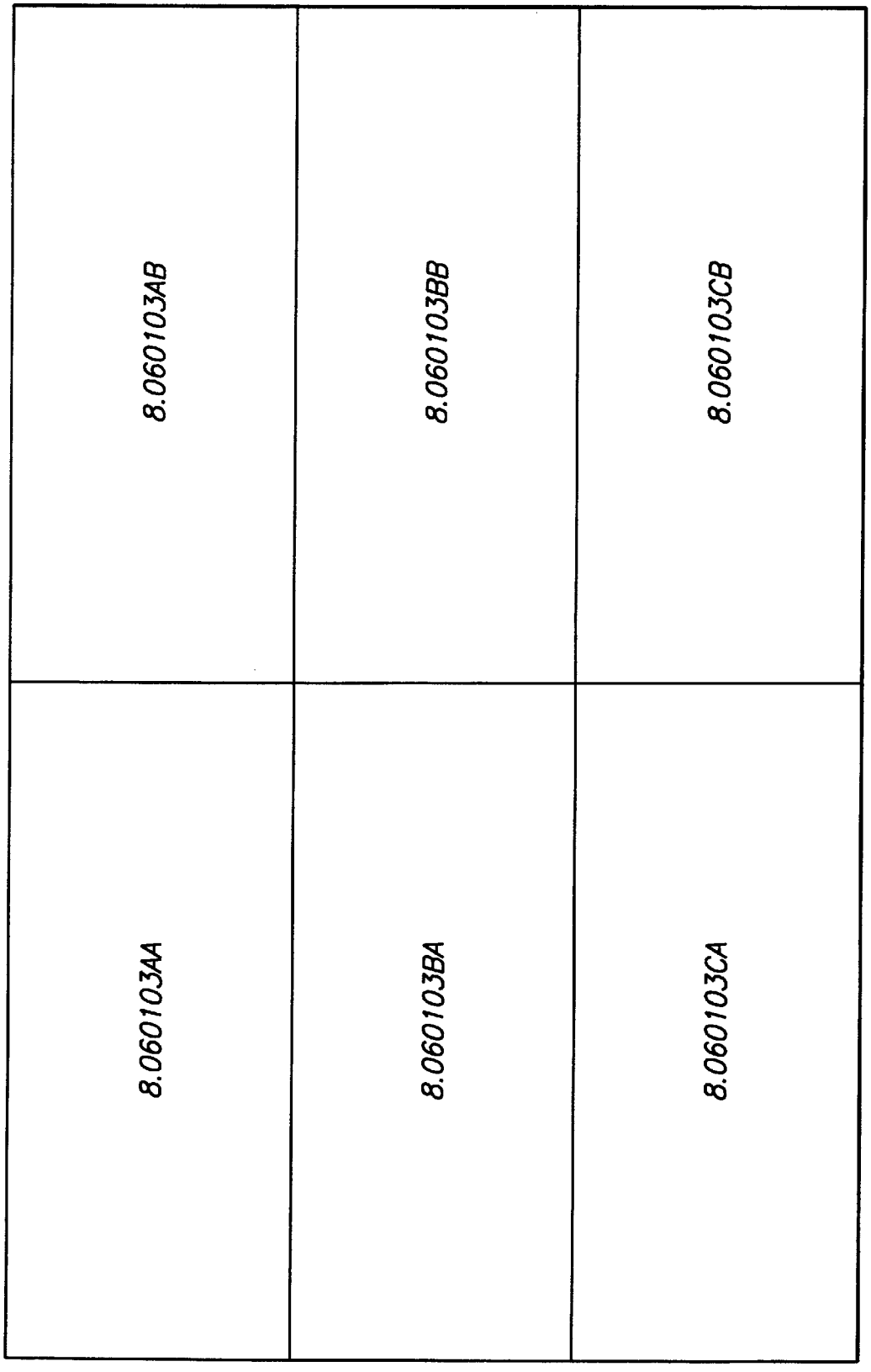
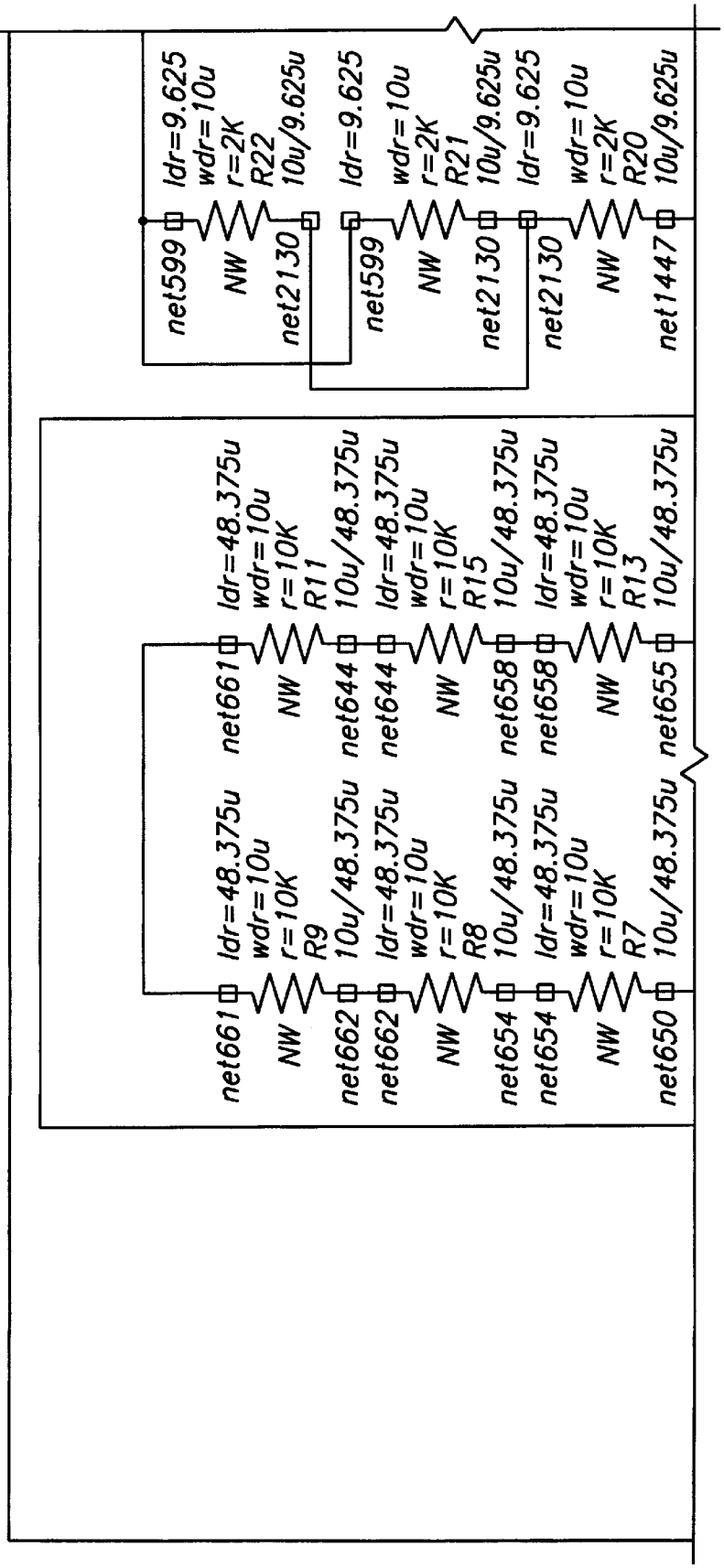

8.060103AB
8.060103BB
8.060103CB
8.060103AA
8.060103BA
8.060103CA

FIG 8.060103



도 면 88.0050 II 00 3AAA

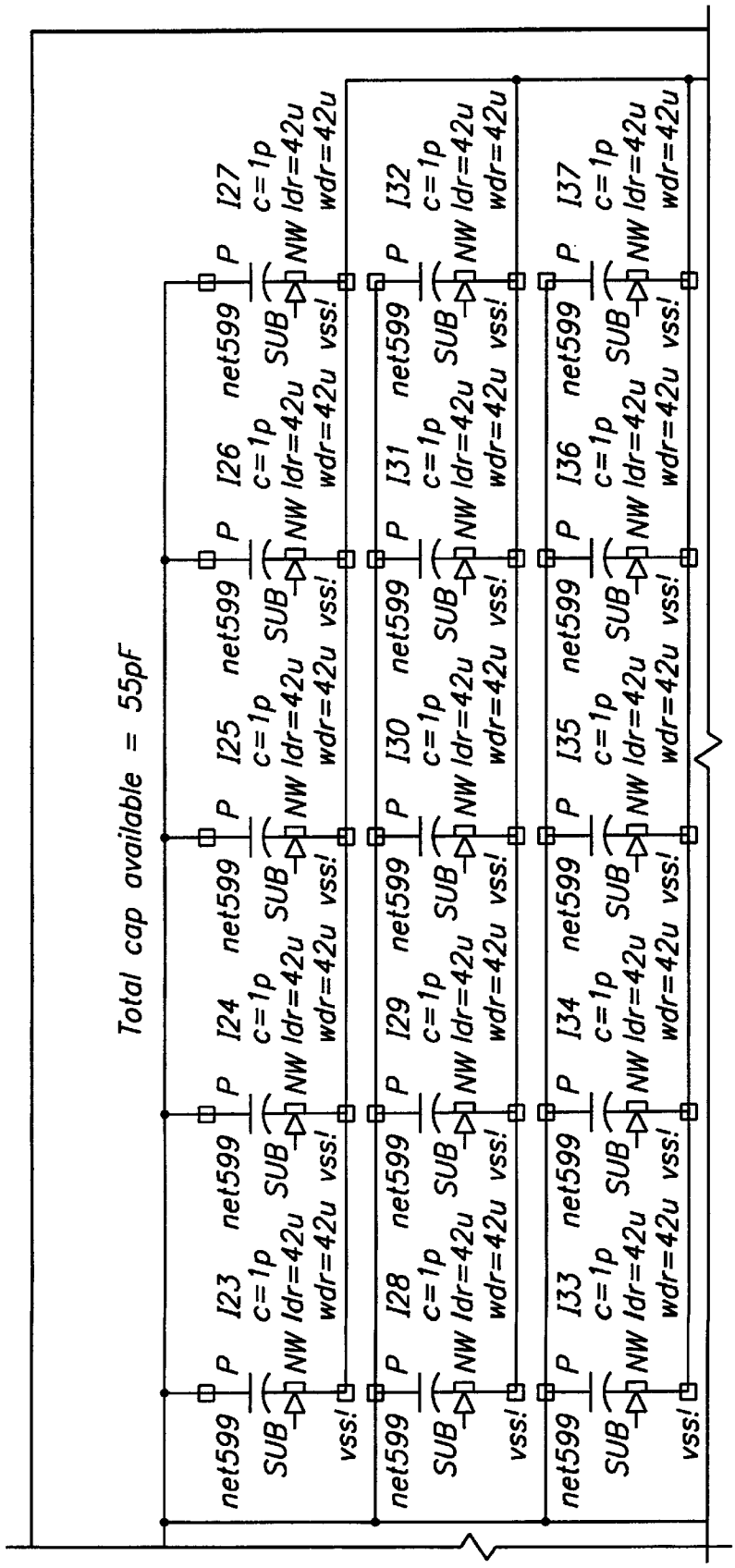

Total cap available = 55pF
net599
P
SUB
NW
vss!
I23
I24
I25
I26
I27
I28
I29
I30
I31
I32
I33
I34
I35
I36
I37
c=1p
ldr=42u
wdr=42u

FIG. 88,005

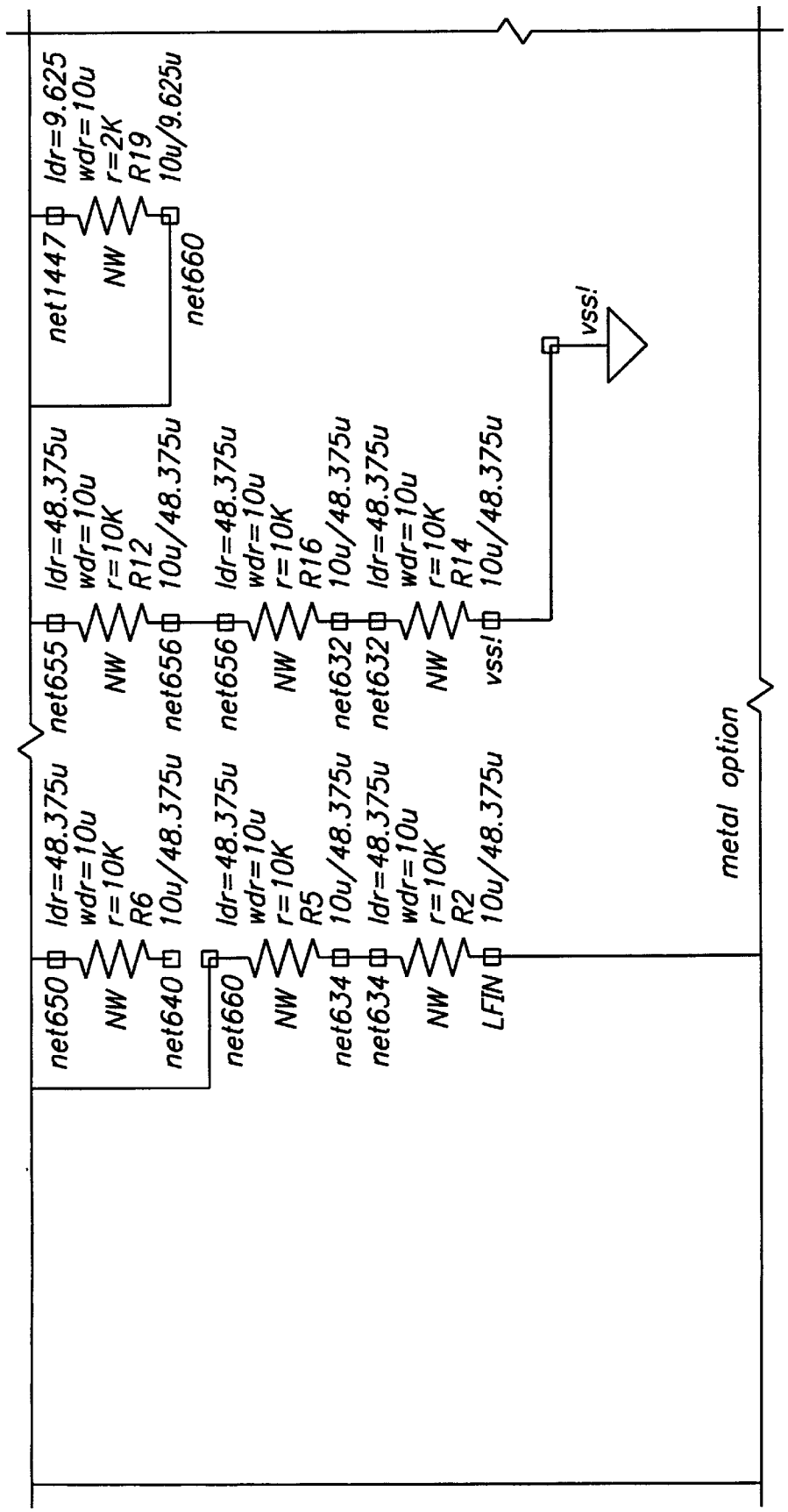
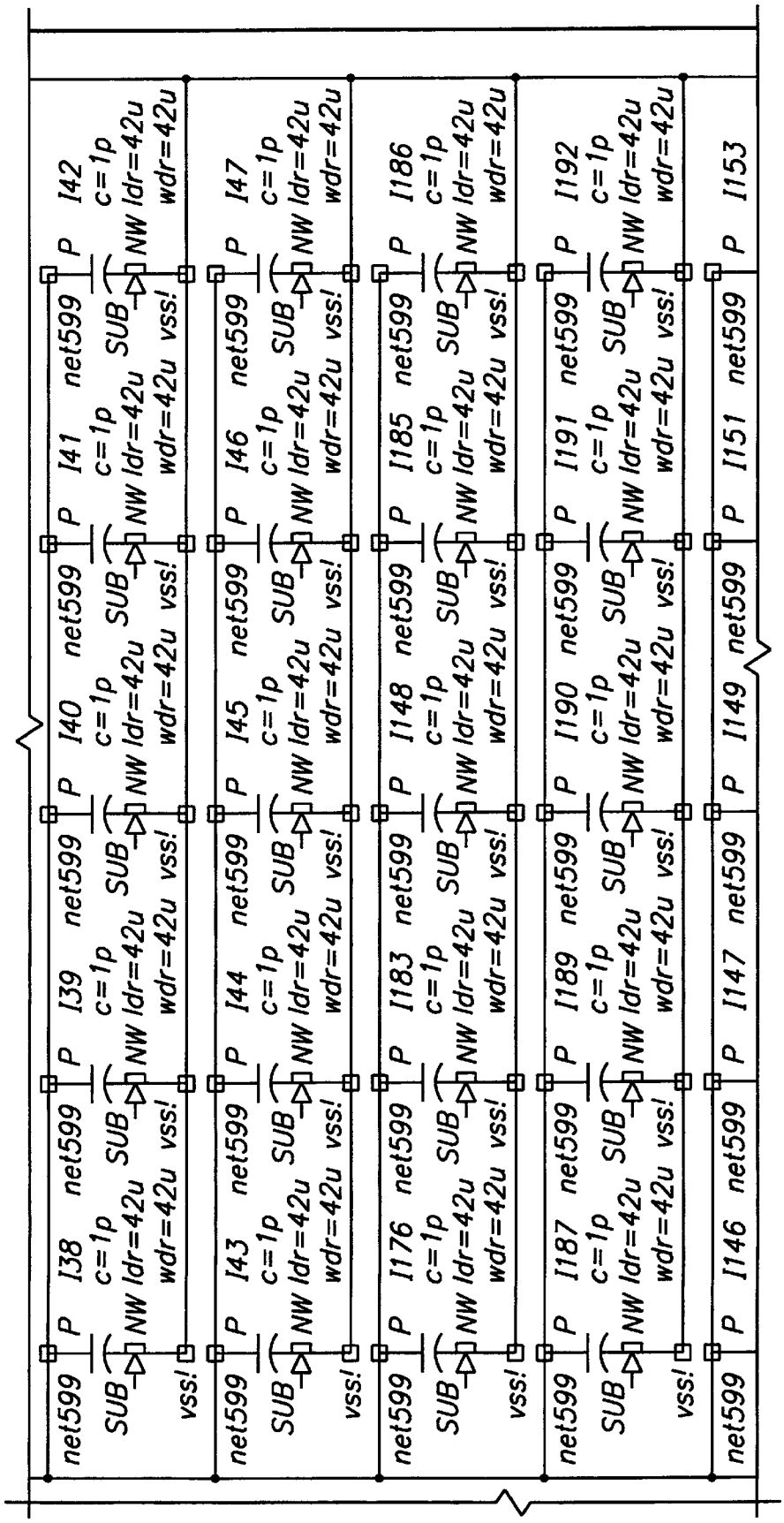

net1447
ldr=9.625
wdr=10u
r=2K
R19
10u/9.625u
NW
net660
vss!
net650
ldr=48.375u
wdr=10u
r=10K
R6
10u/48.375u
NW
net640
net655
ldr=48.375u
wdr=10u
r=10K
R12
10u/48.375u
NW
net656
net656
ldr=48.375u
wdr=10u
r=10K
R16
10u/48.375u
NW
net632
net632
ldr=48.375u
wdr=10u
r=10K
R14
10u/48.375u
NW
vss!
net660
ldr=48.375u
wdr=10u
r=10K
R5
10u/48.375u
NW
net634
net634
ldr=48.375u
wdr=10u
r=10K
R2
10u/48.375u
NW
LFIN
metal option

FIG. 88.0050


net599 P I38 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I39 c=1p SUB NW ldr=42u wdr=42u vss!
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net599 P I41 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I42 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I43 c=1p SUB NW ldr=42u wdr=42u vss!
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net599 P I45 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I46 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I47 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I176 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I183 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I148 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I185 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I186 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I187 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I189 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I190 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I191 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I192 c=1p SUB NW ldr=42u wdr=42u vss!
net599 P I146 net599 P I147 net599 P I149 net599 P I151 net599 P I153

FIG. 1873

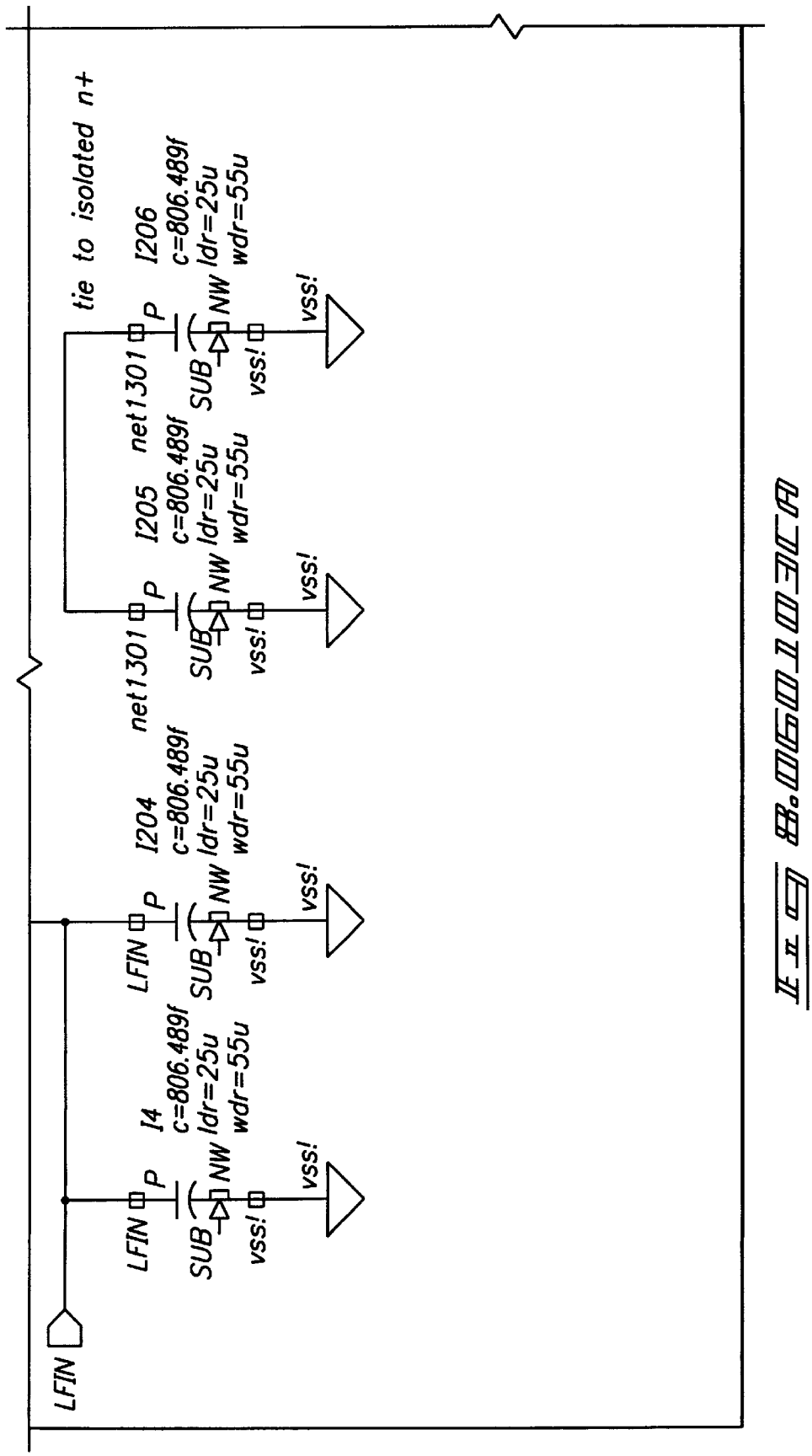


FIG 98.0500.0100.0001

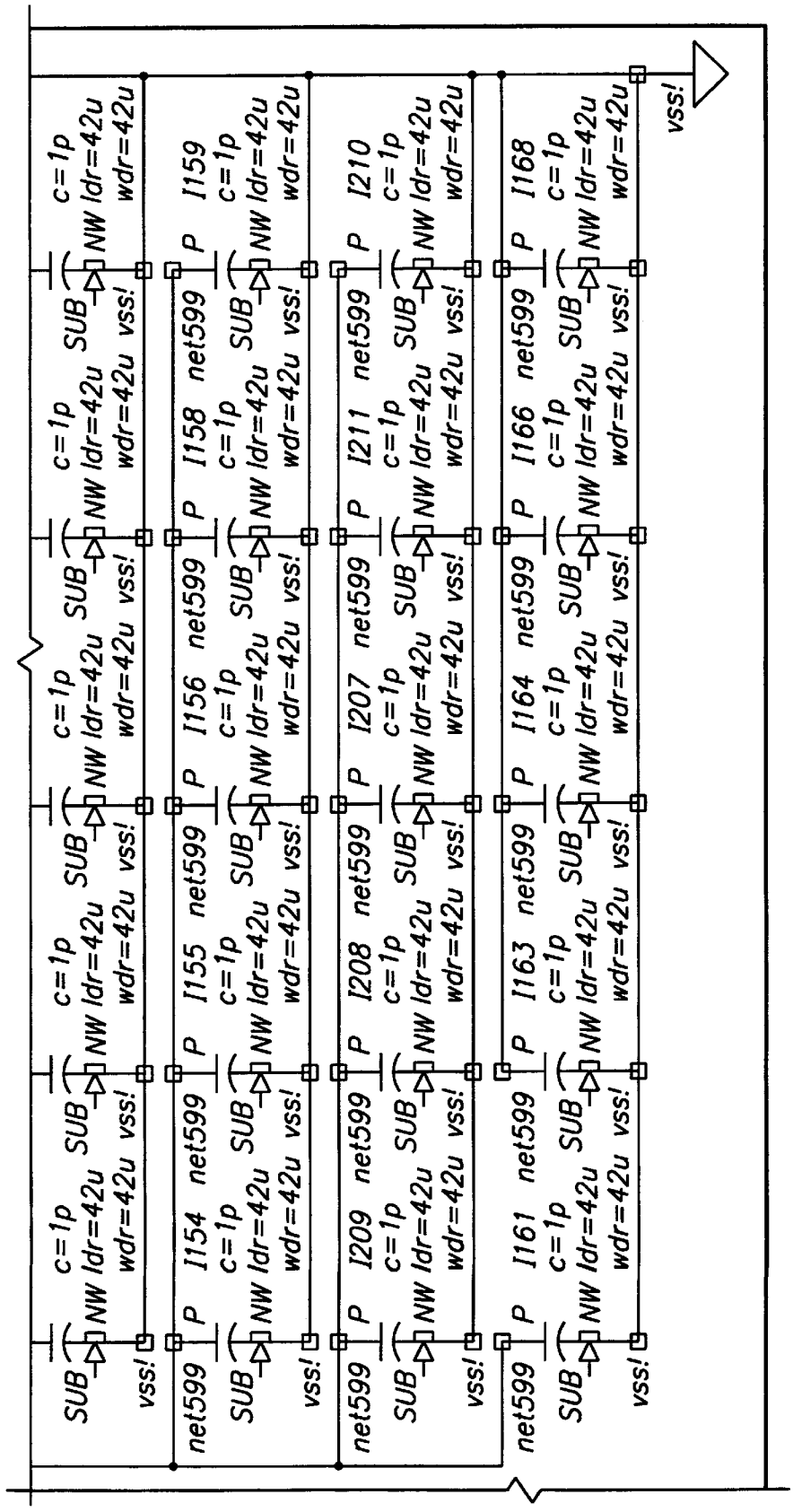

SUB
NW
P
net599
vss!
c=1p
ldr=42u
wdr=42u
I154
I155
I156
I158
I159
I161
I163
I164
I166
I168
I207
I208
I209
I210
I211

FIG. 1875

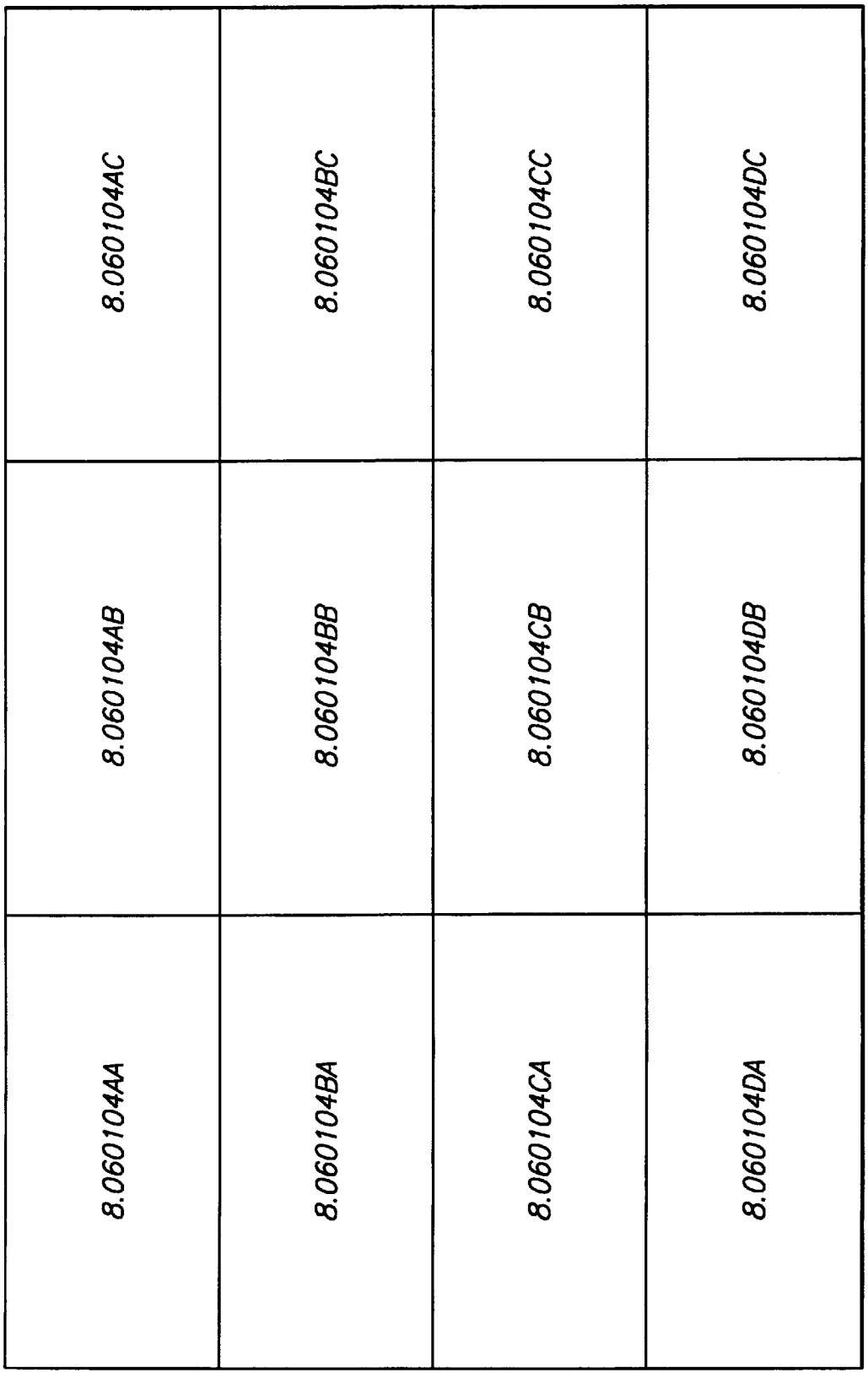

8.060104AC
8.060104BC
8.060104CC
8.060104DC
8.060104AB
8.060104BB
8.060104CB
8.060104DB
8.060104AA
8.060104BA
8.060104CA
8.060104DA

FIG. 8.060104

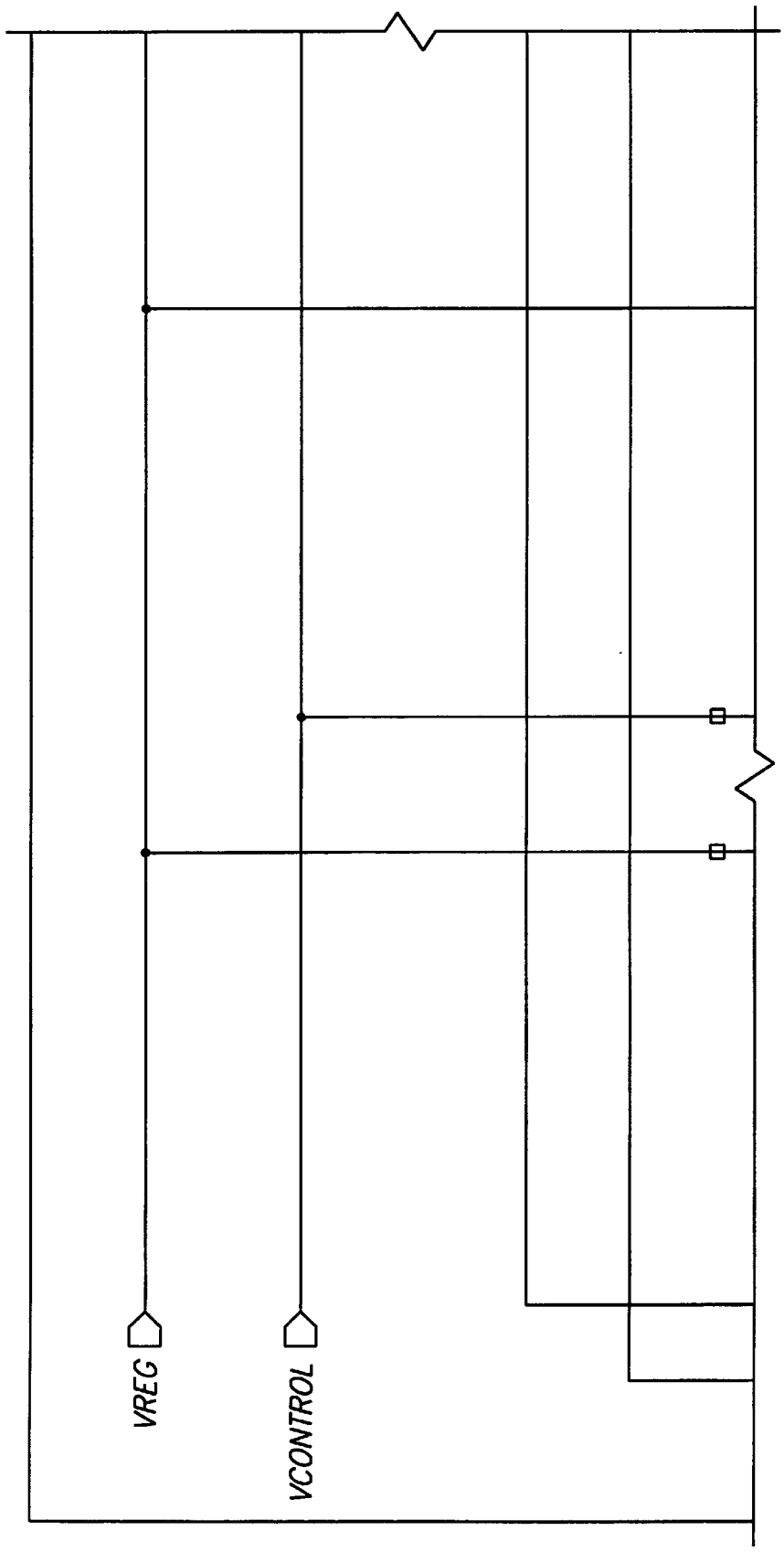


FIG 8,050,108AA

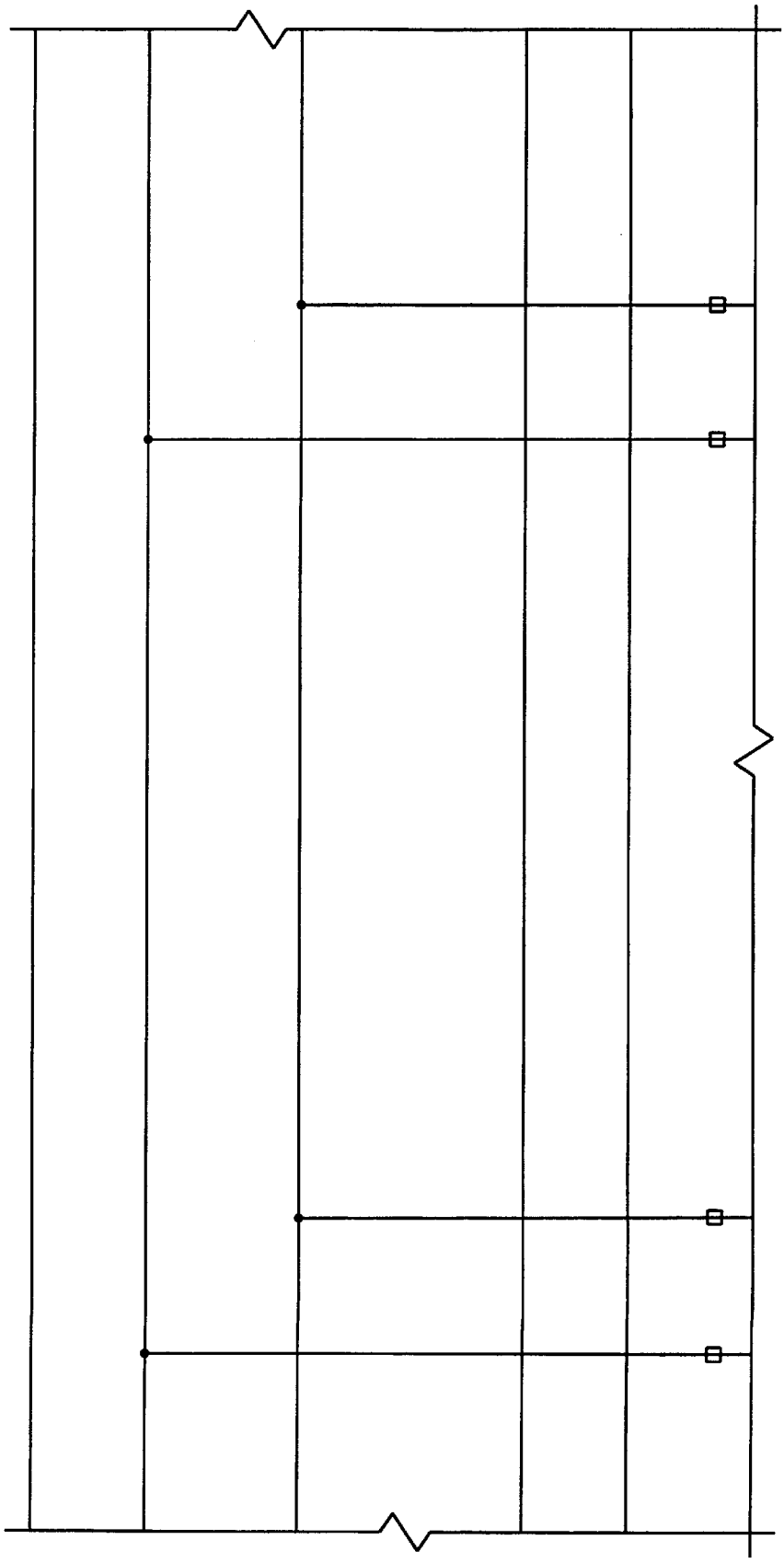


FIG 88.0501A1B

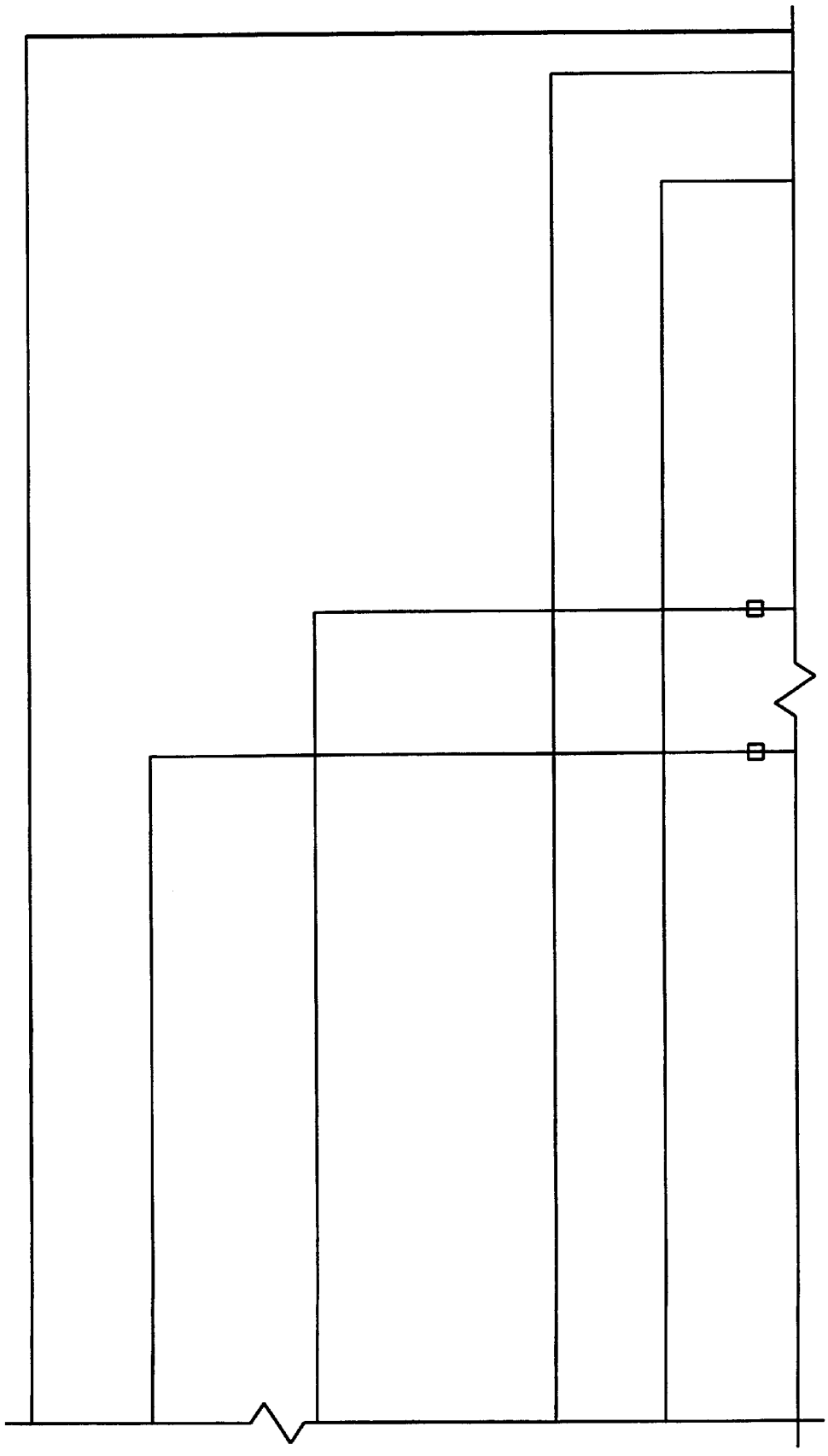


FIG 8.0501AC

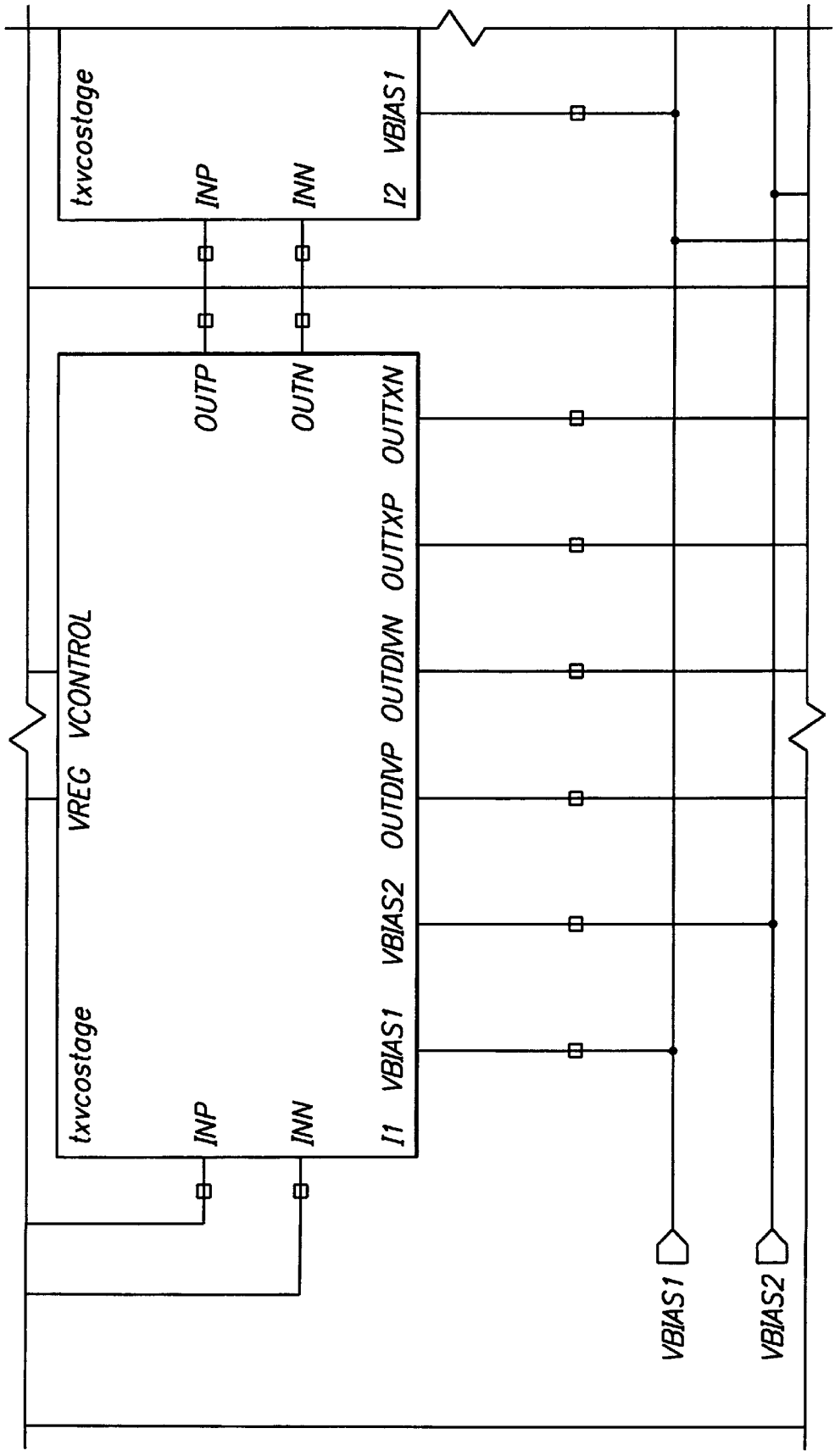

txvcostage
INP
INN
I2 VBIAS1
OUTP
OUTN
OUTTXN
OUTTXP
OUTDIVN
OUTDIVP
VBIAS2
VBIAS1
VREG VCONTROL
txvcostage
INP
INN
I1
VBIAS1
VBIAS2

FIG 88.00500

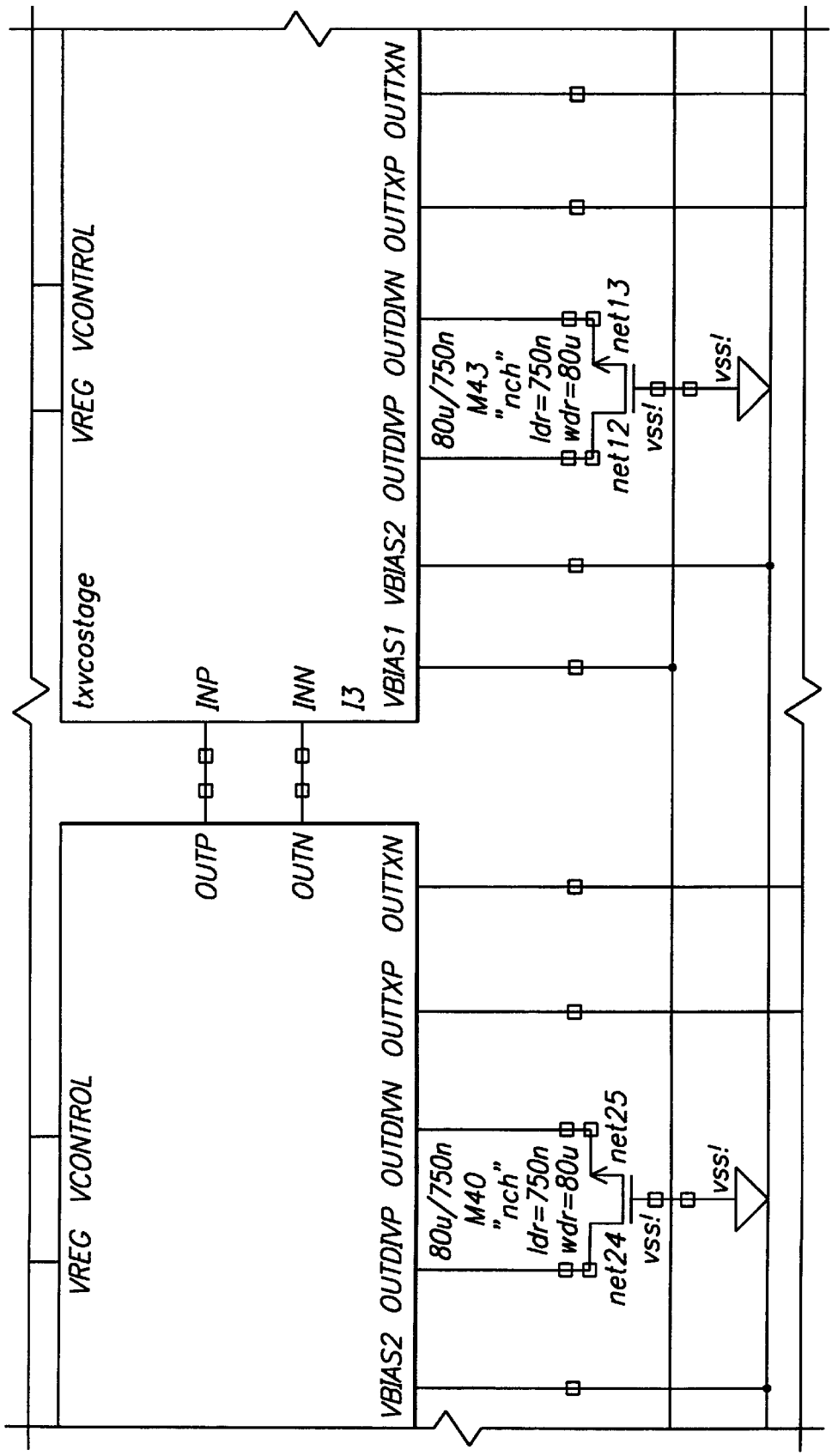


FIG 8.0601104B

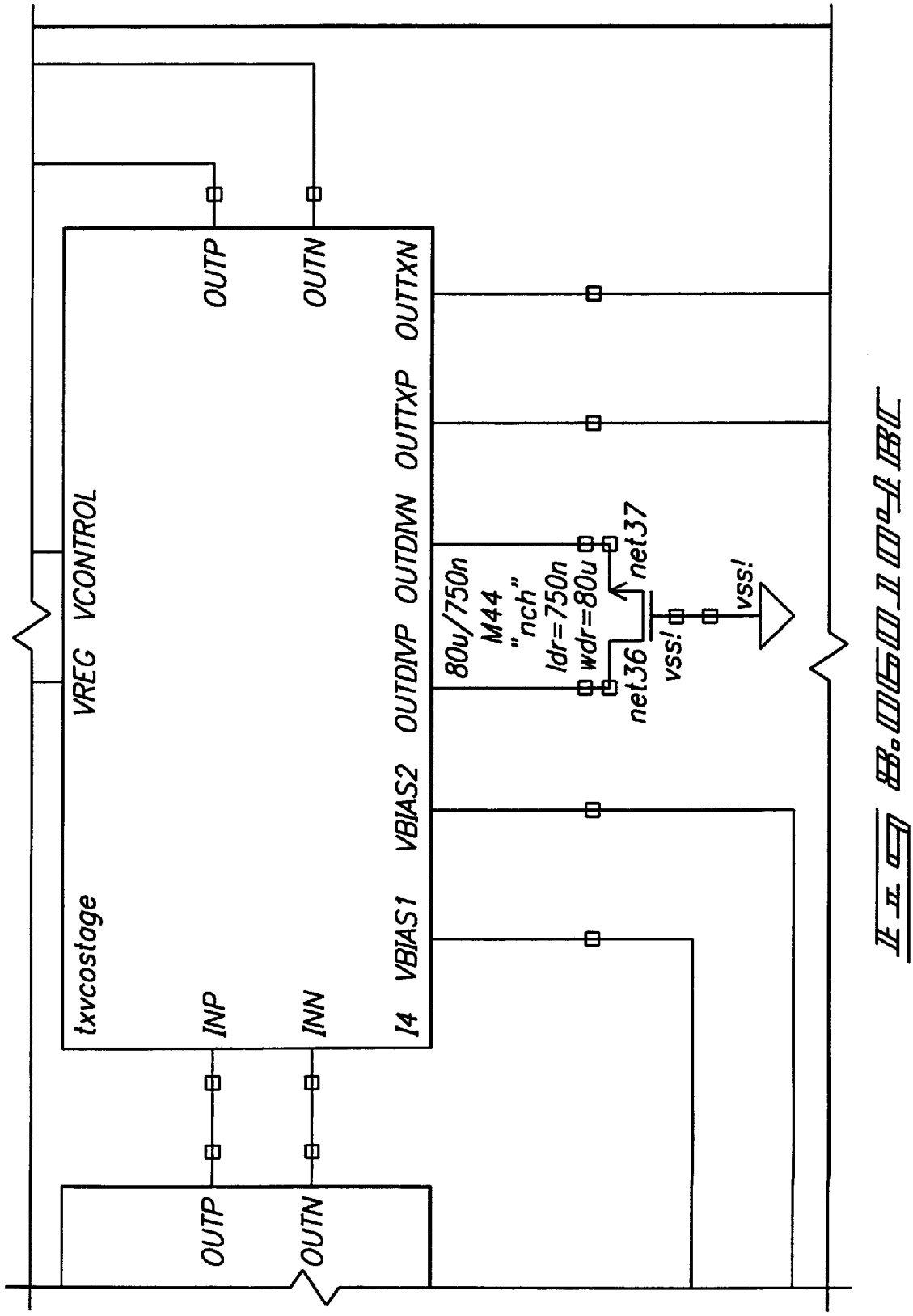


FIG. 88.00500 11 00 4 IBIC

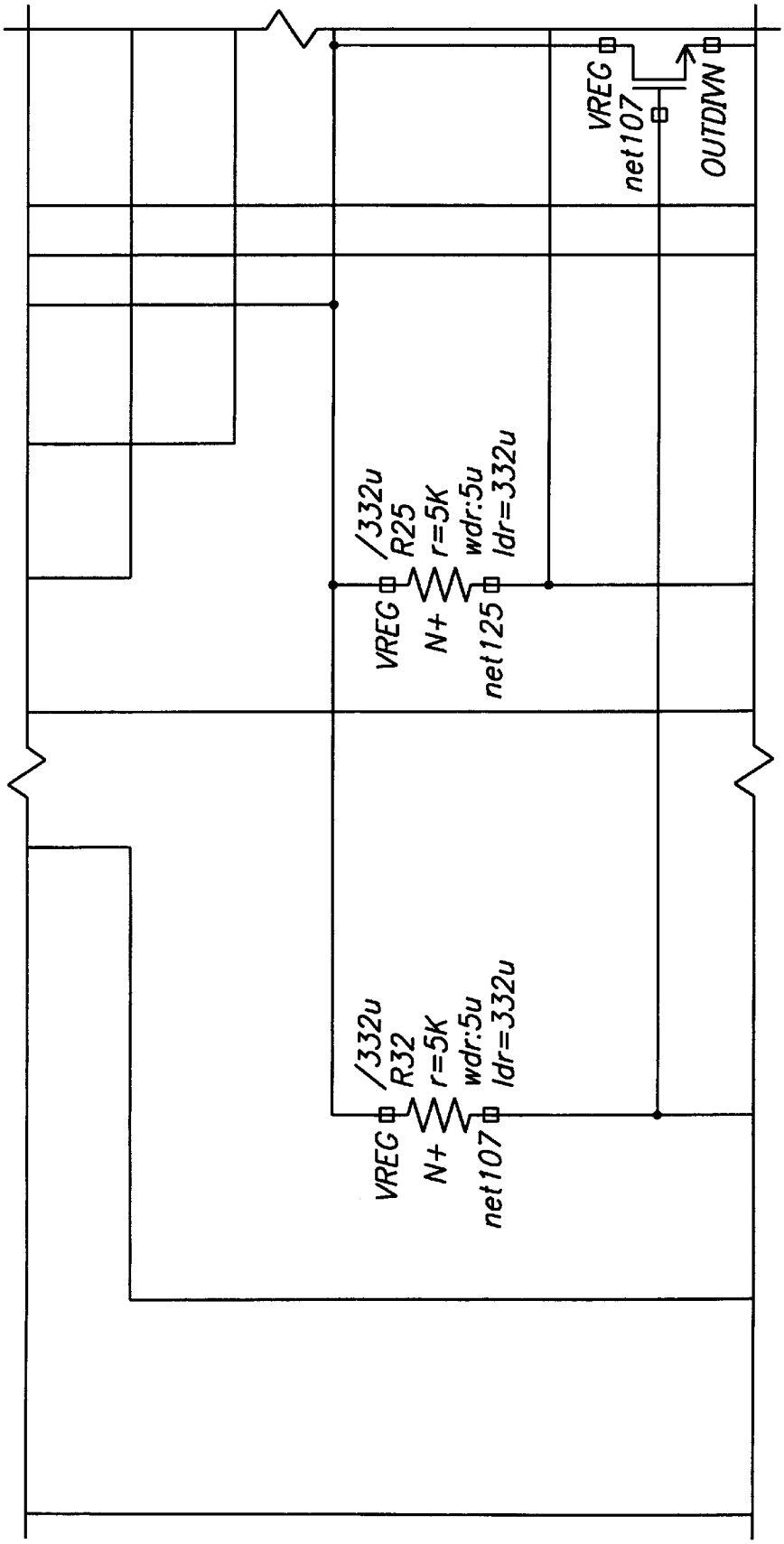


FIG 88.0501 (PRIOR ART)

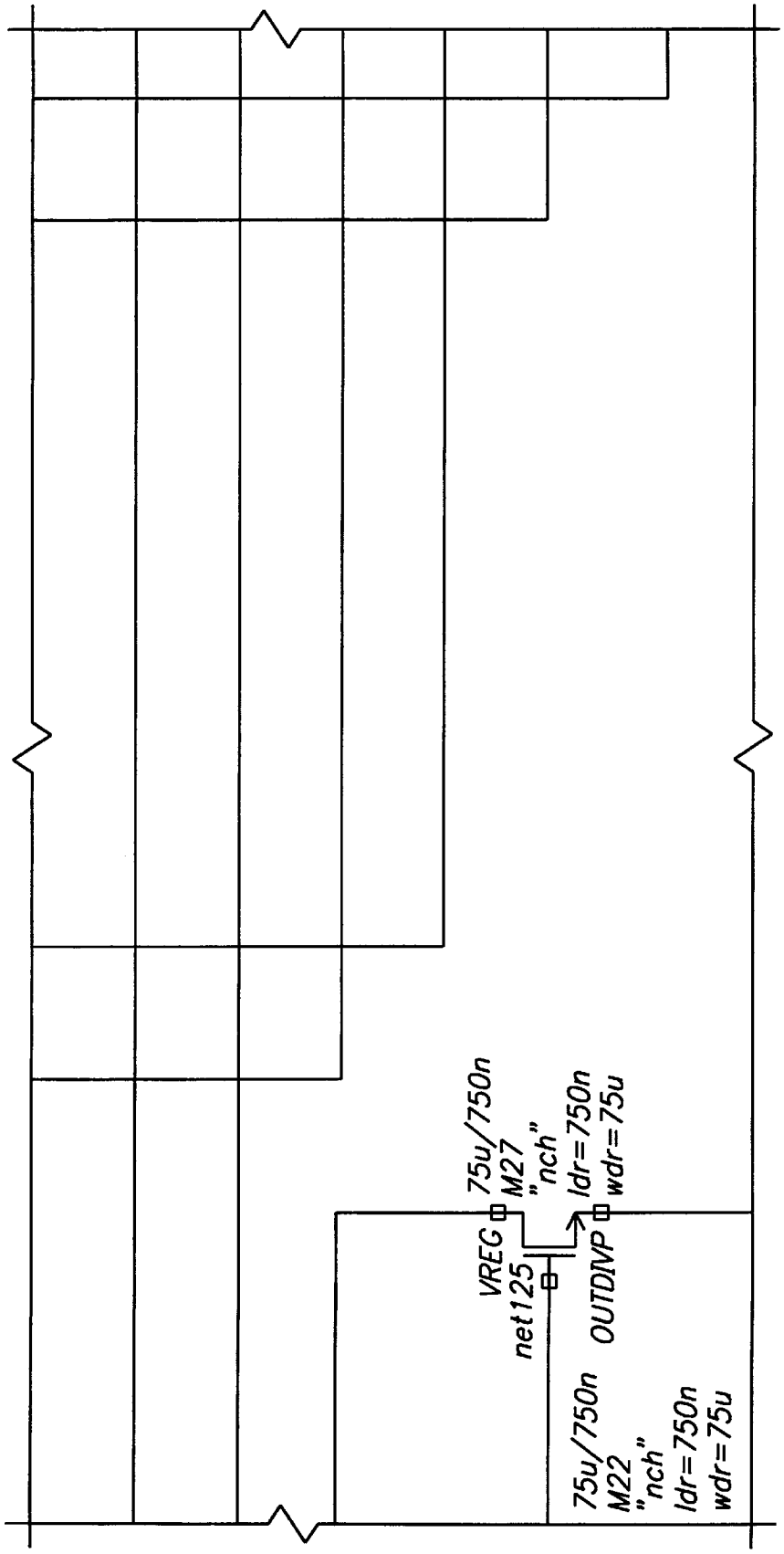


Fig. 88.0050110-4

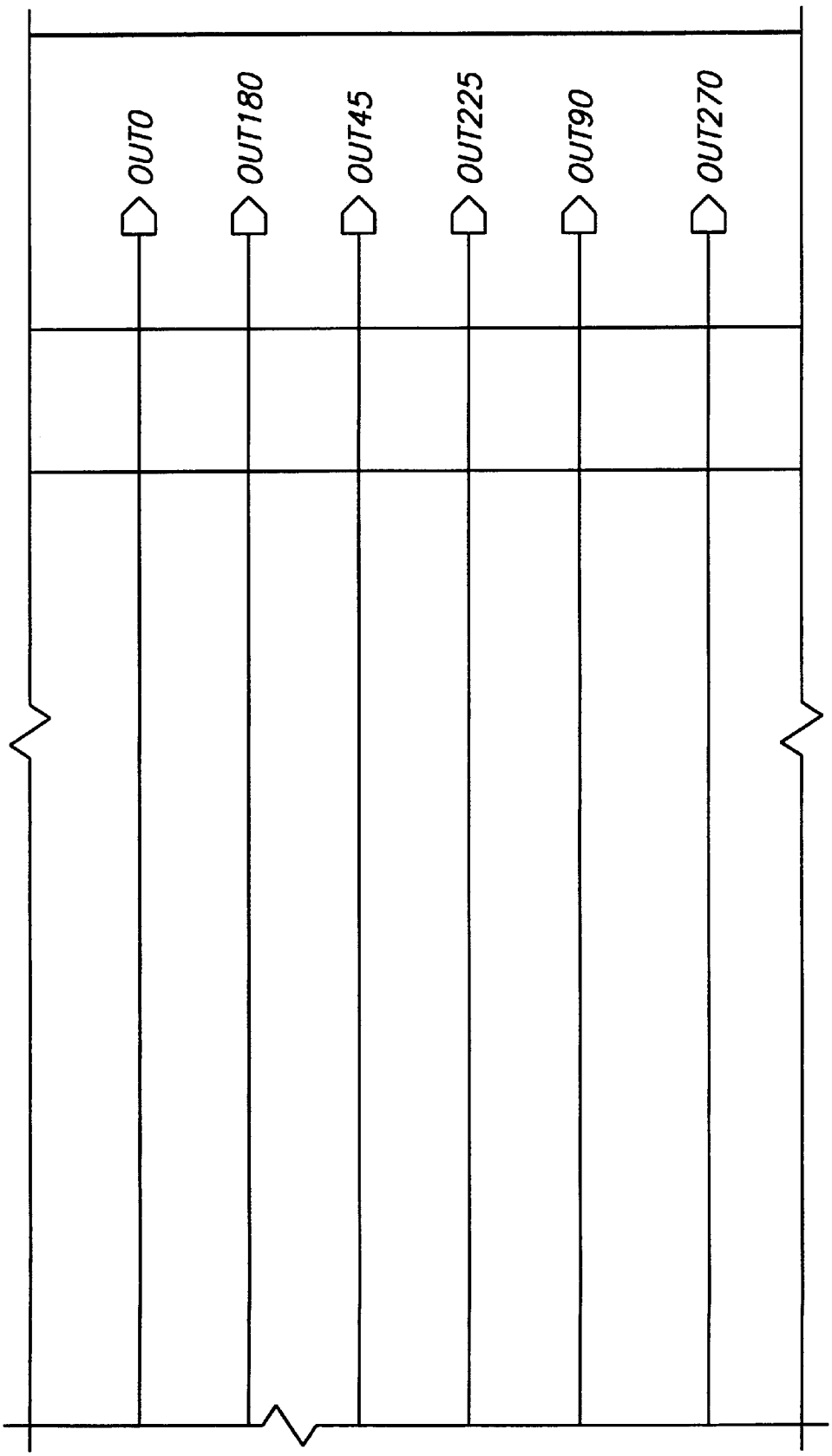


FIG 8,050,108

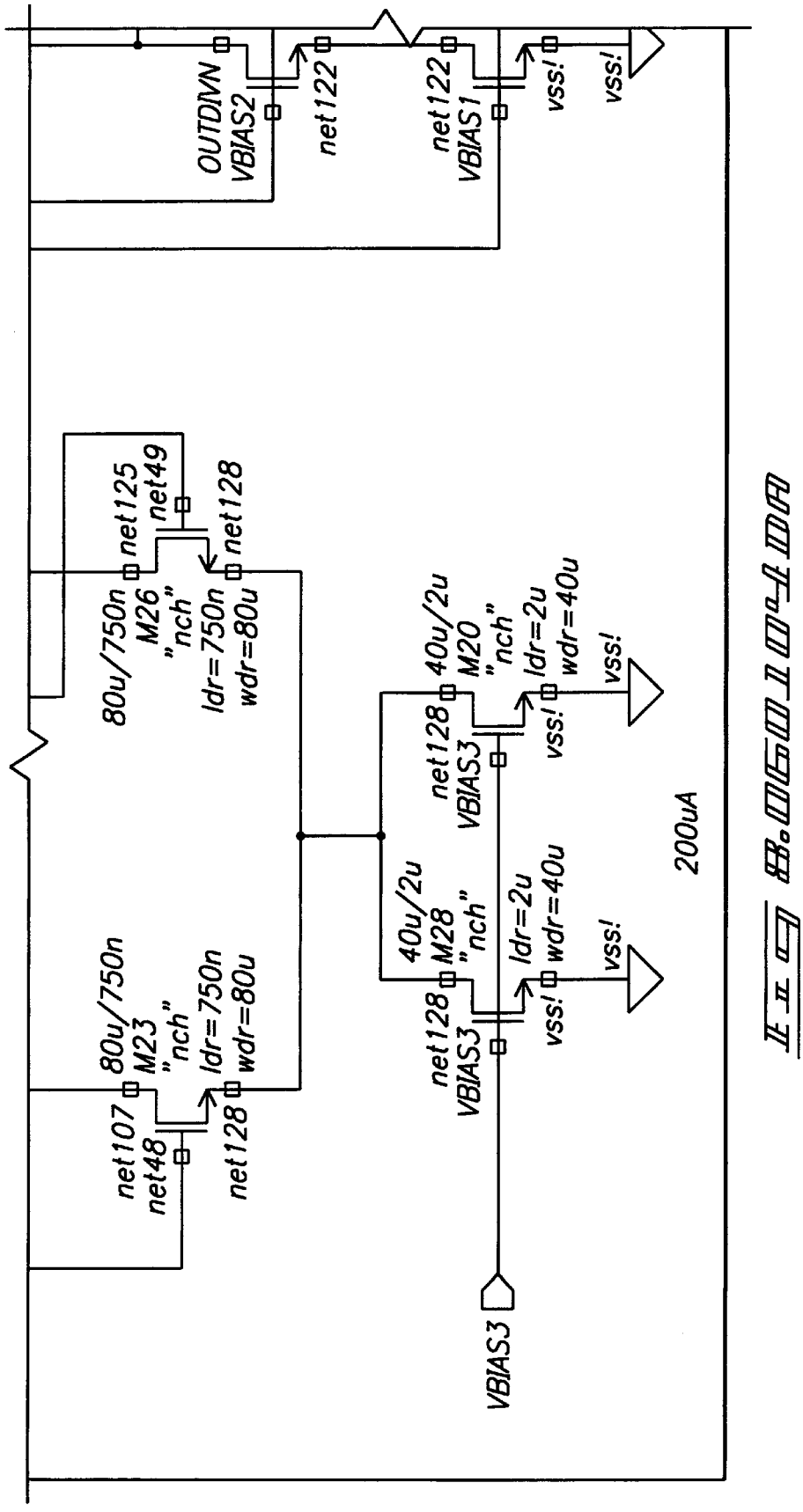

OUTDIVN
VBIAS2
net122
net122
VBIAS1
vss!
vss!
net125
net49
net128
80u/750n
M26
"nch"
ldr=750n
wdr=80u
40u/2u
M20
"nch"
ldr=2u
wdr=40u
vss!
net128
VBIAS3
vss!
40u/2u
M28
"nch"
ldr=2u
wdr=40u
vss!
net128
VBIAS3
vss!
80u/750n
M23
"nch"
ldr=750n
wdr=80u
net107
net48
net128
200uA
VBIAS3

FIG. 1886

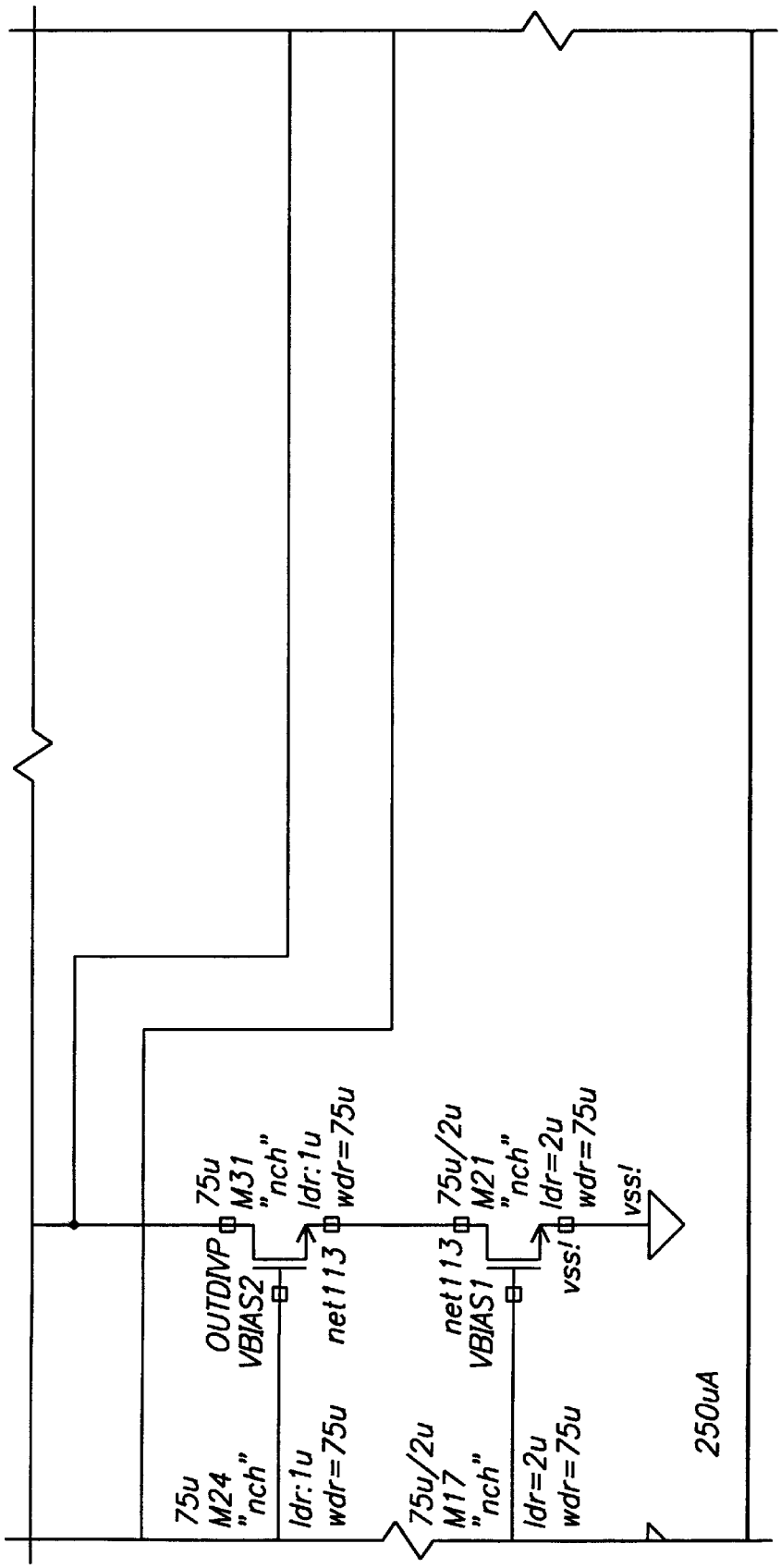


FIG 89.0501004DB

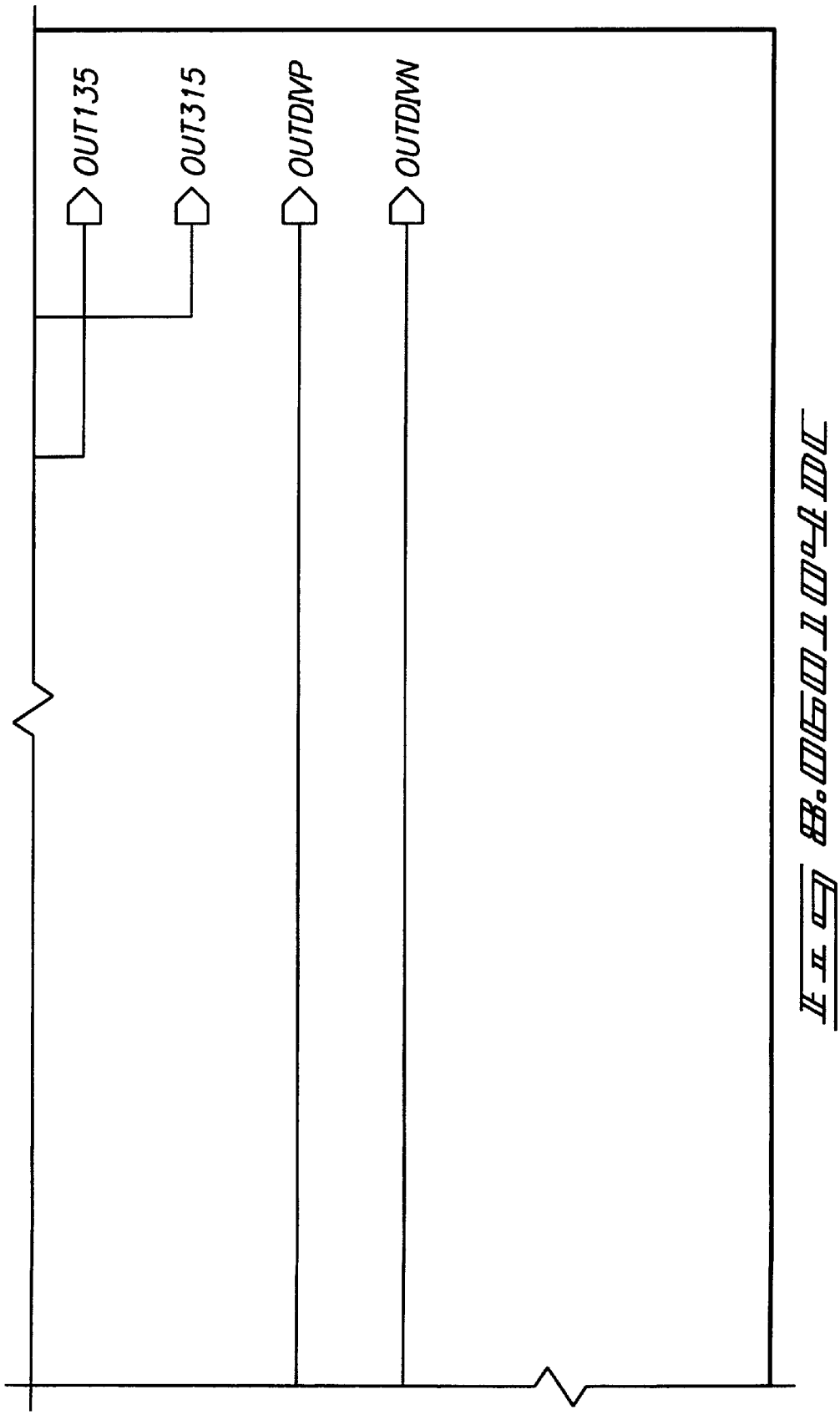


FIG 98,050,704

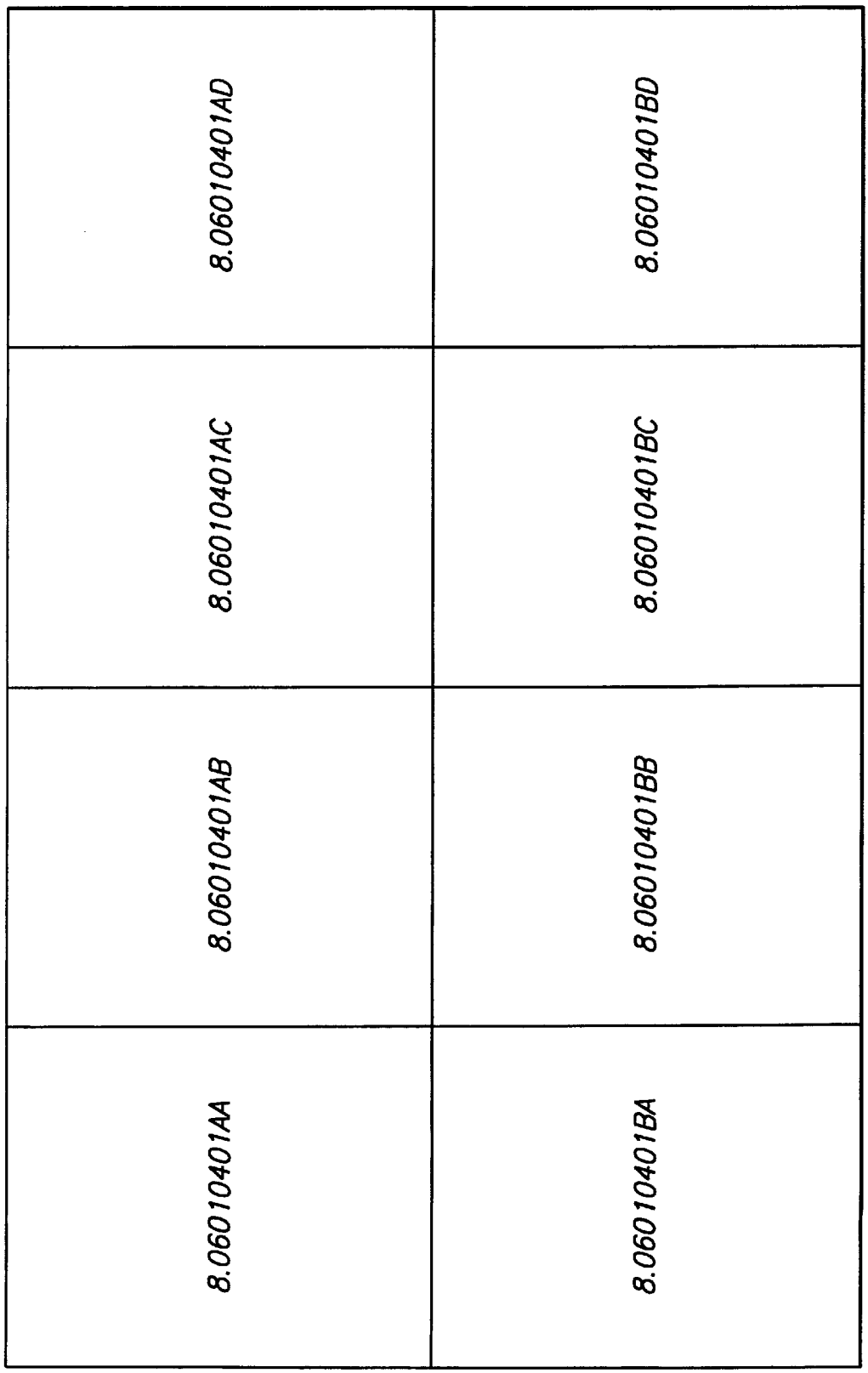


FIG 88.0501100

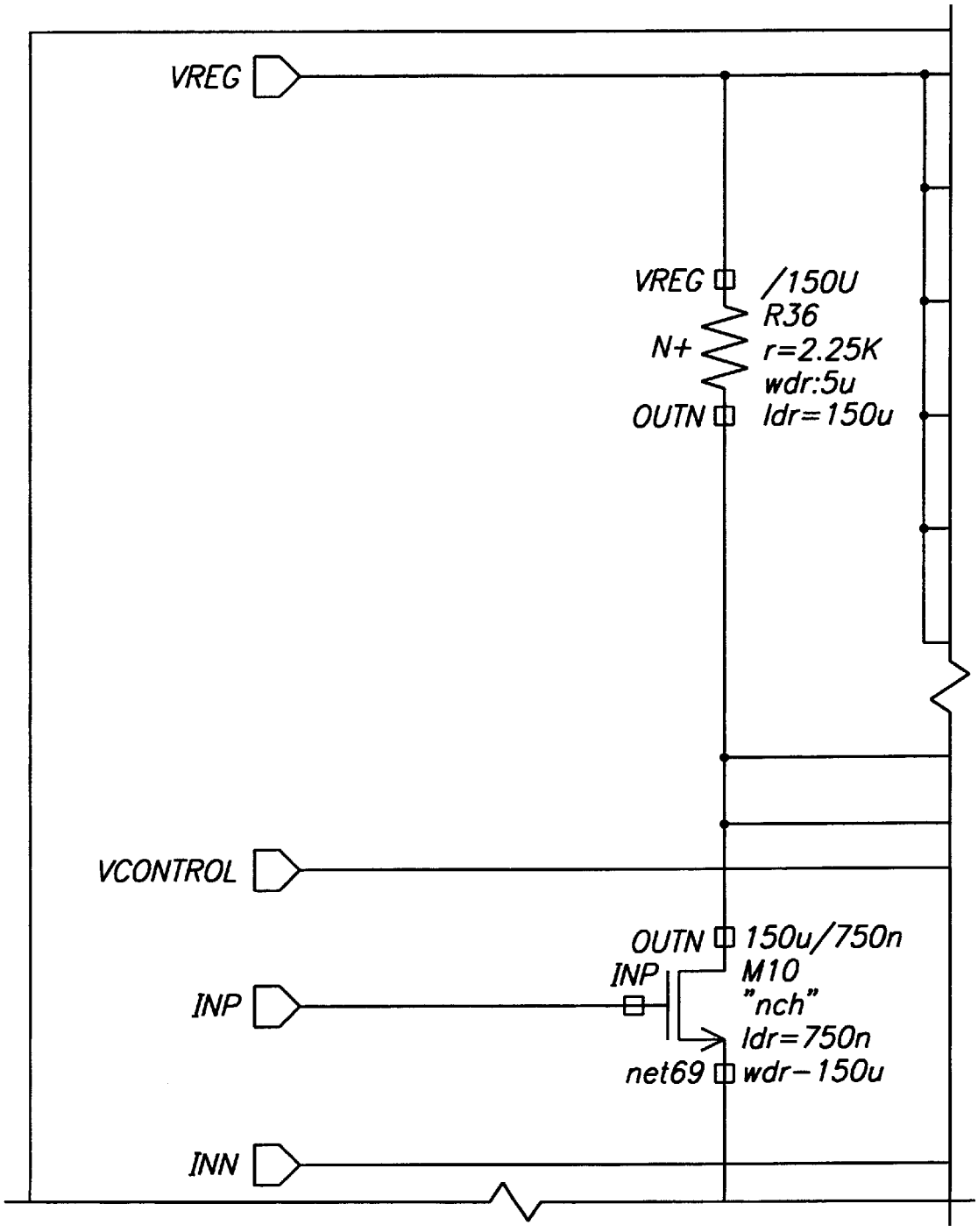


Fig 8.0601040104AA

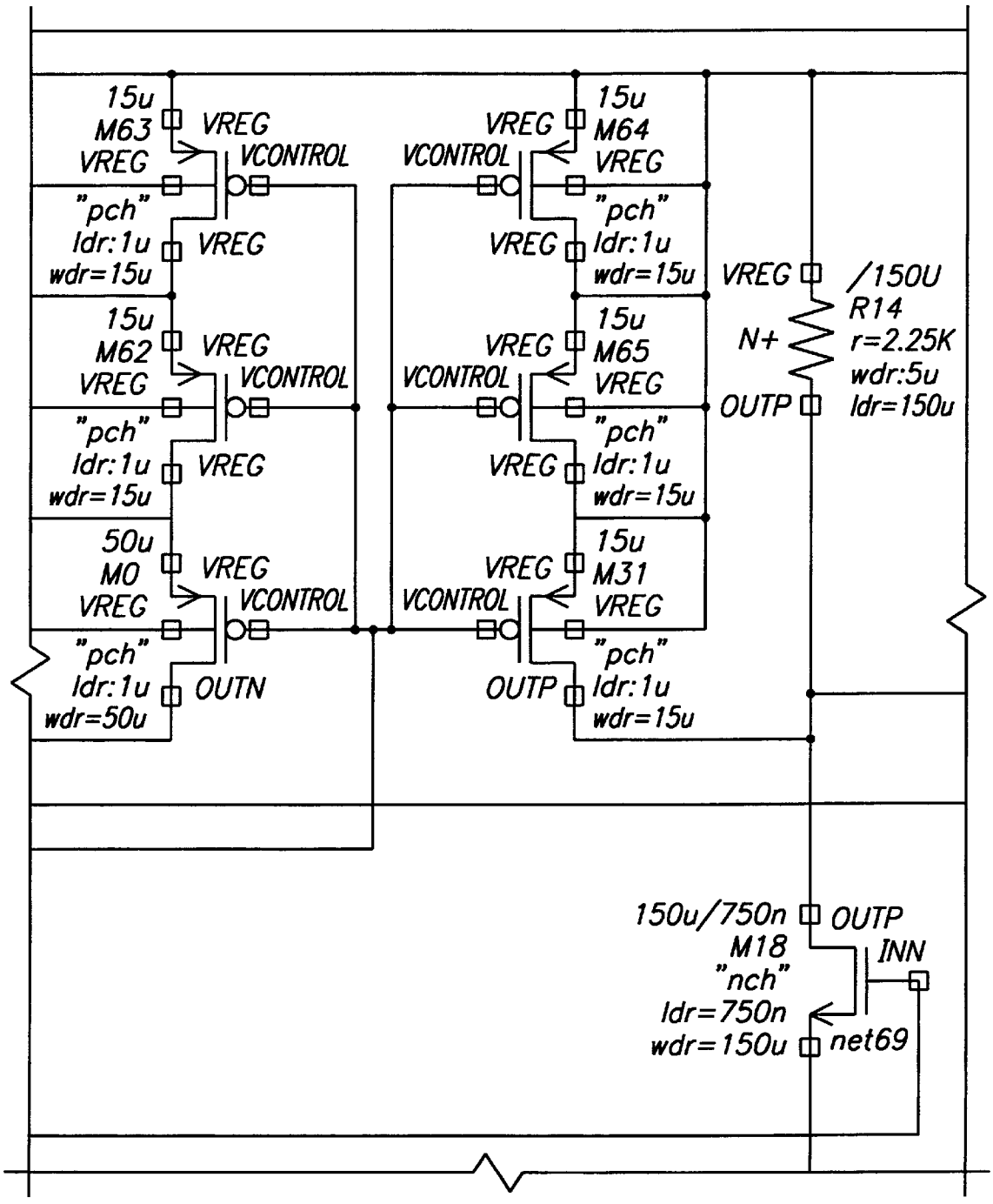


Fig. 8,060,104,018B

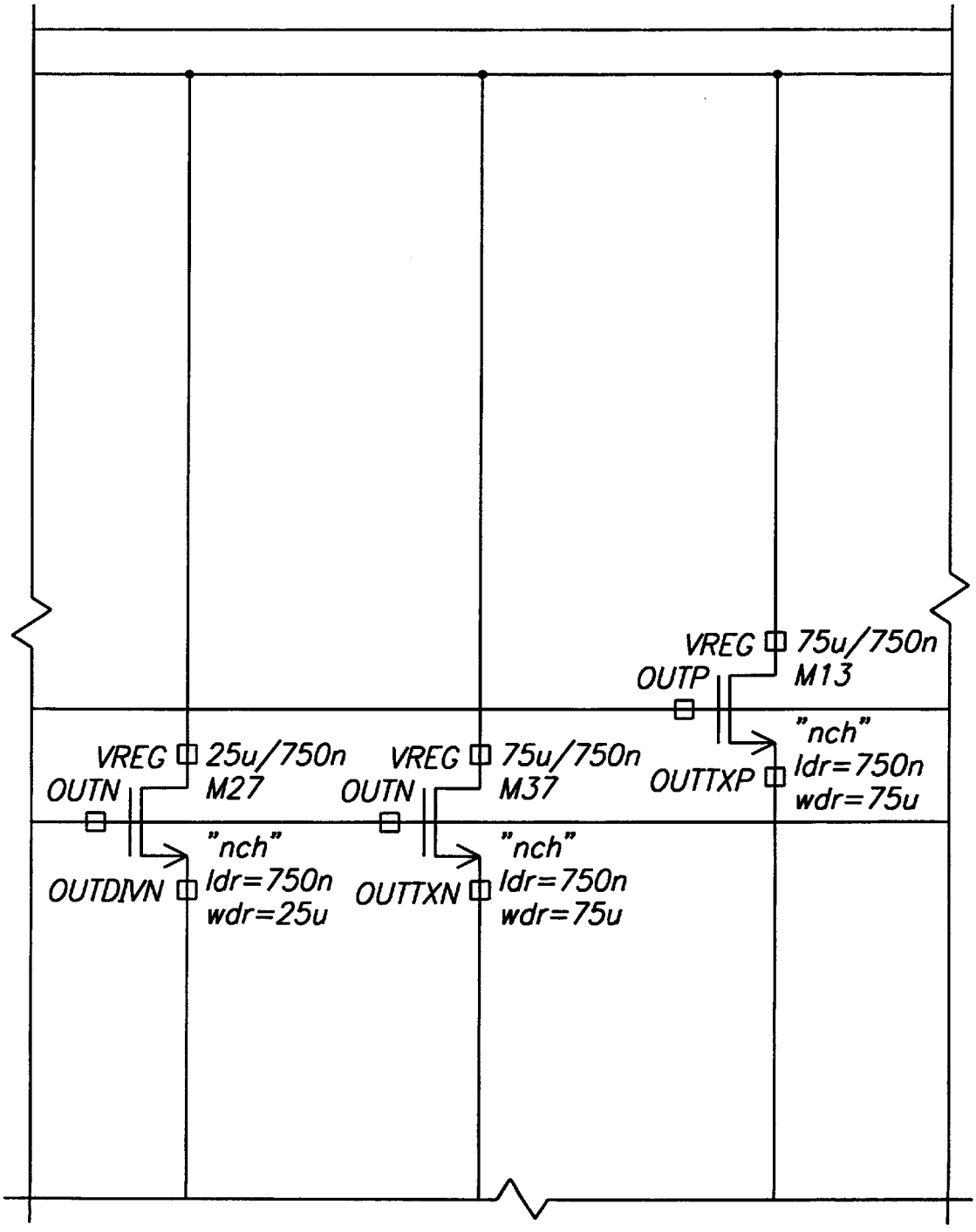


Fig 8.0610104010AC

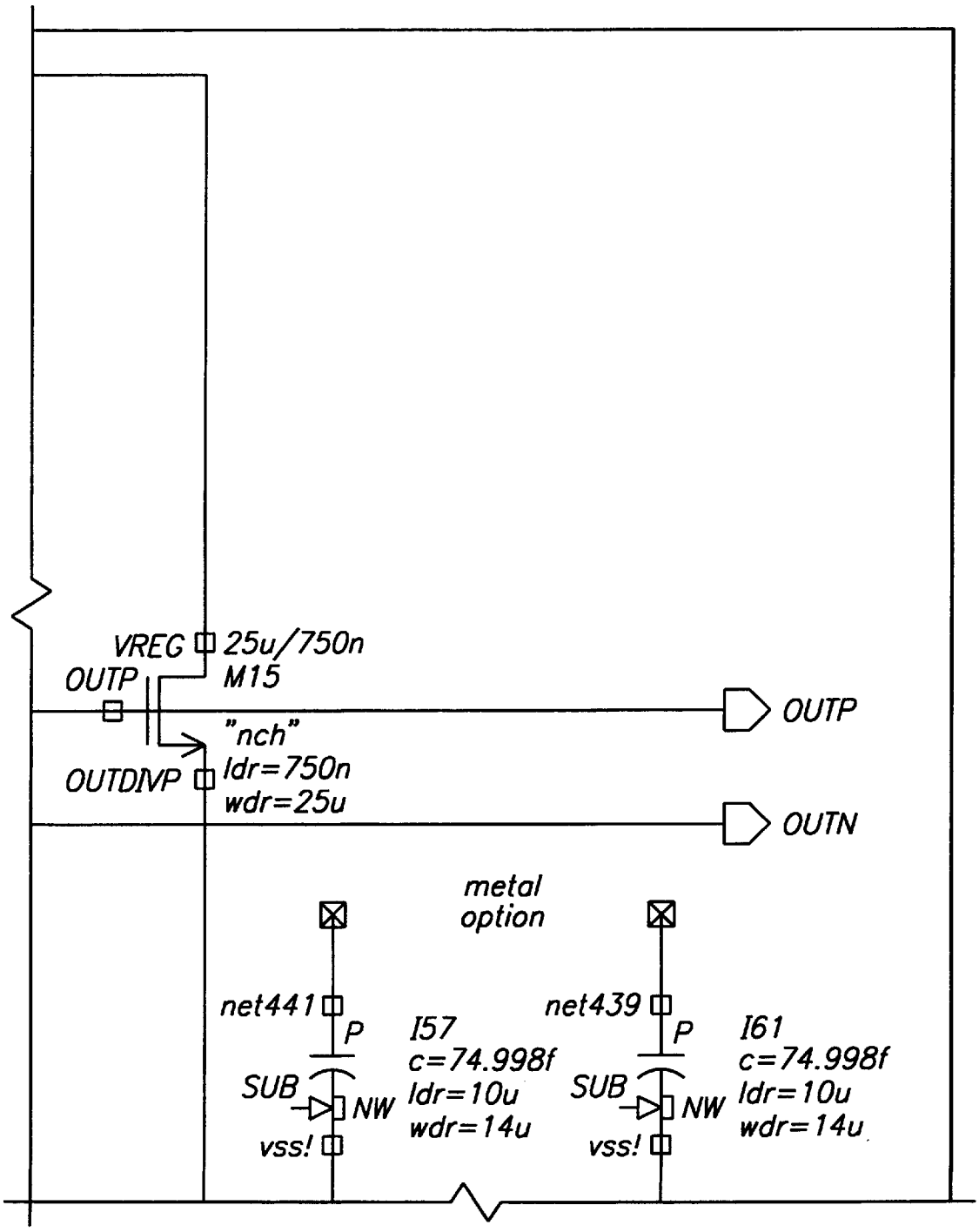


Fig 8,060,104,010

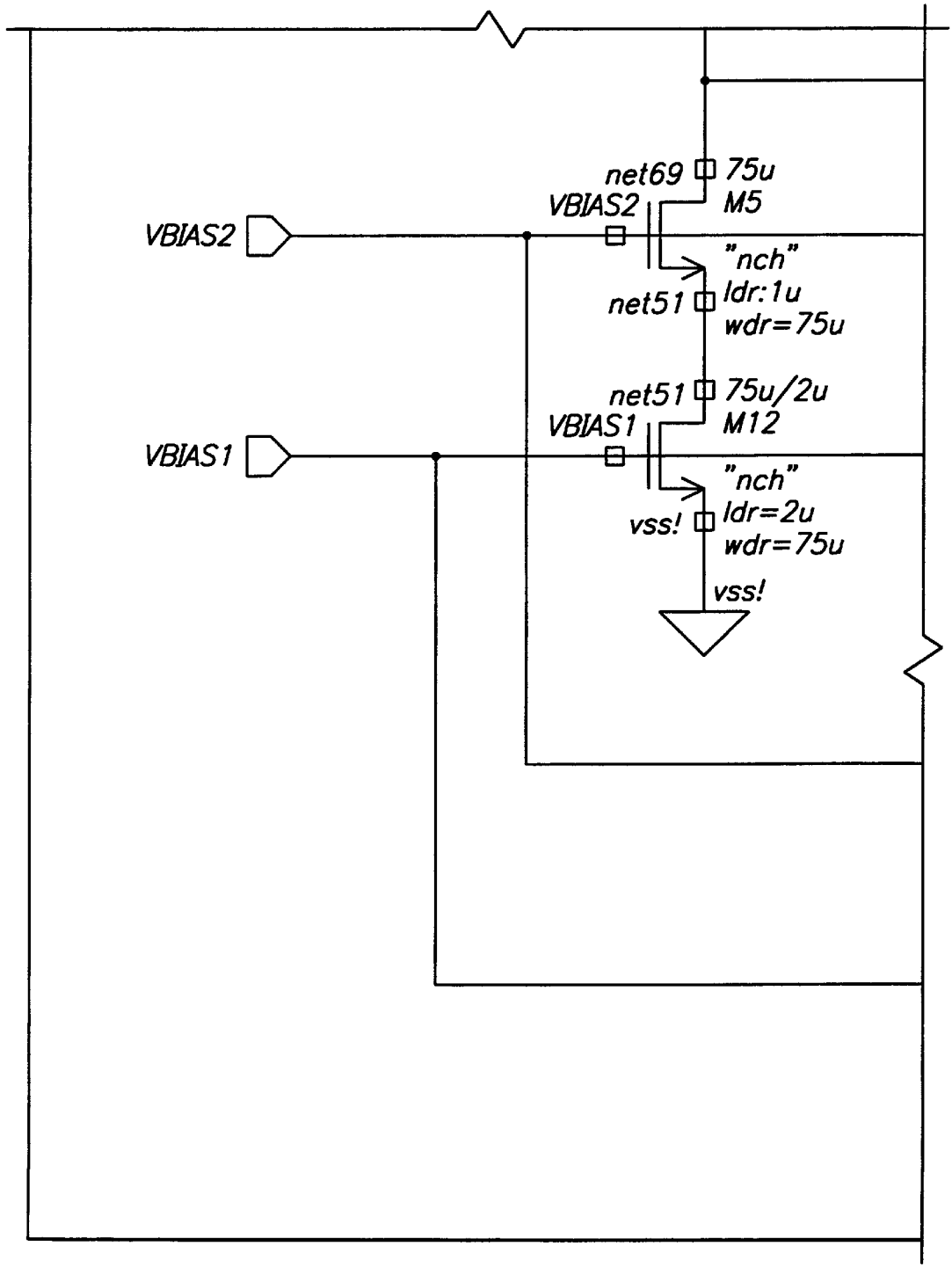


FIG 8,060104018A

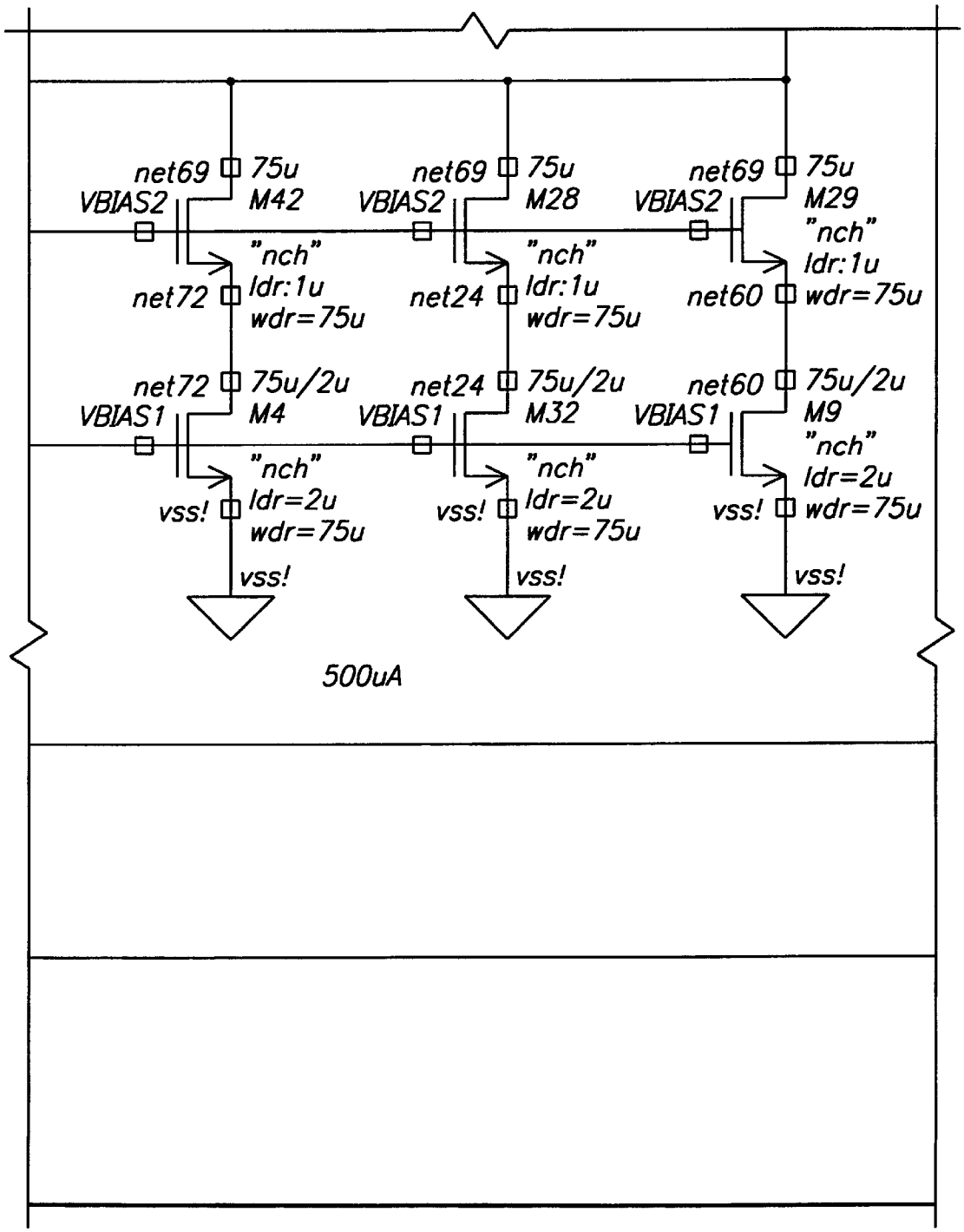


Fig 8,060,102,188

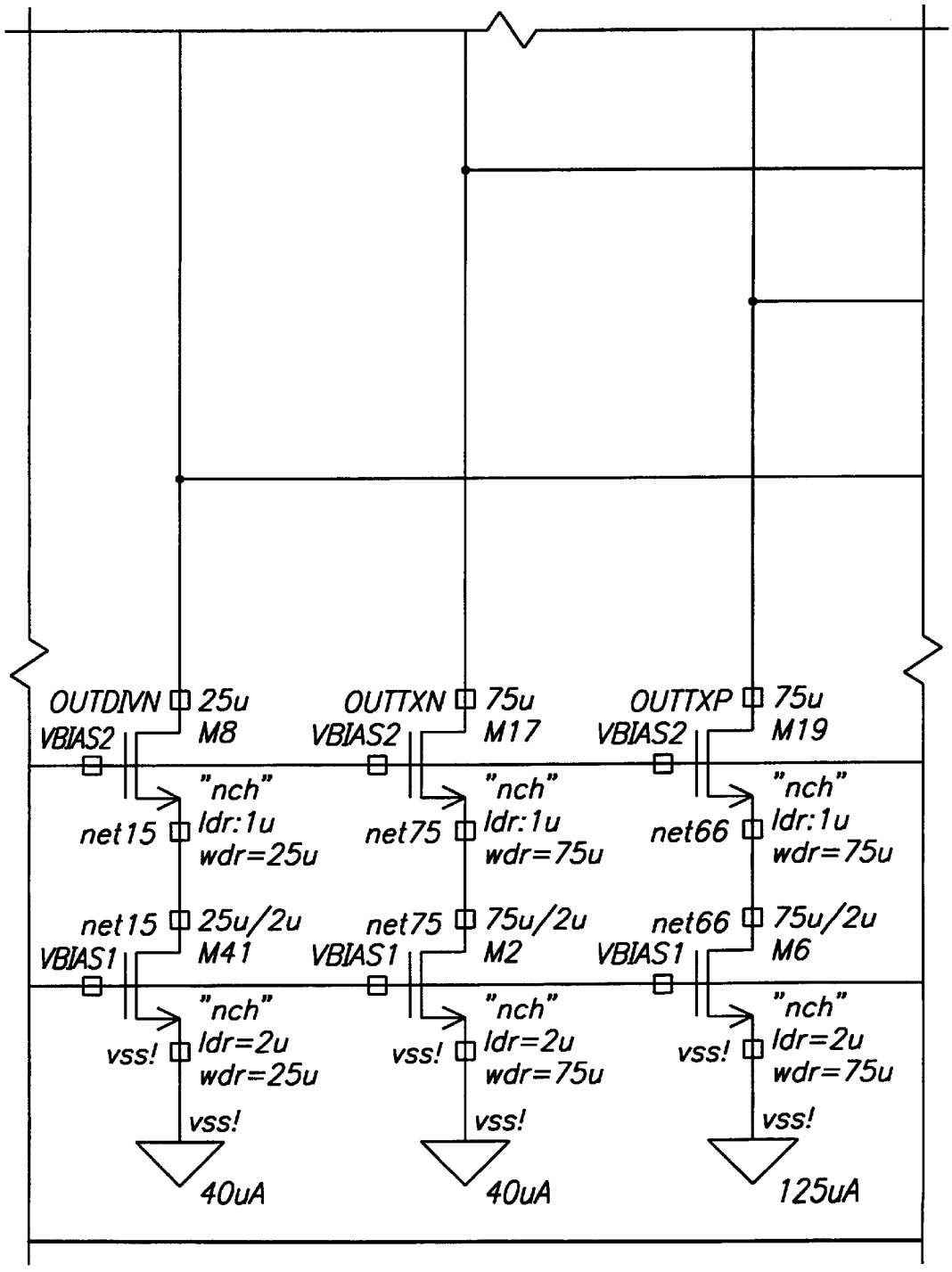


Fig 8.0601040118C

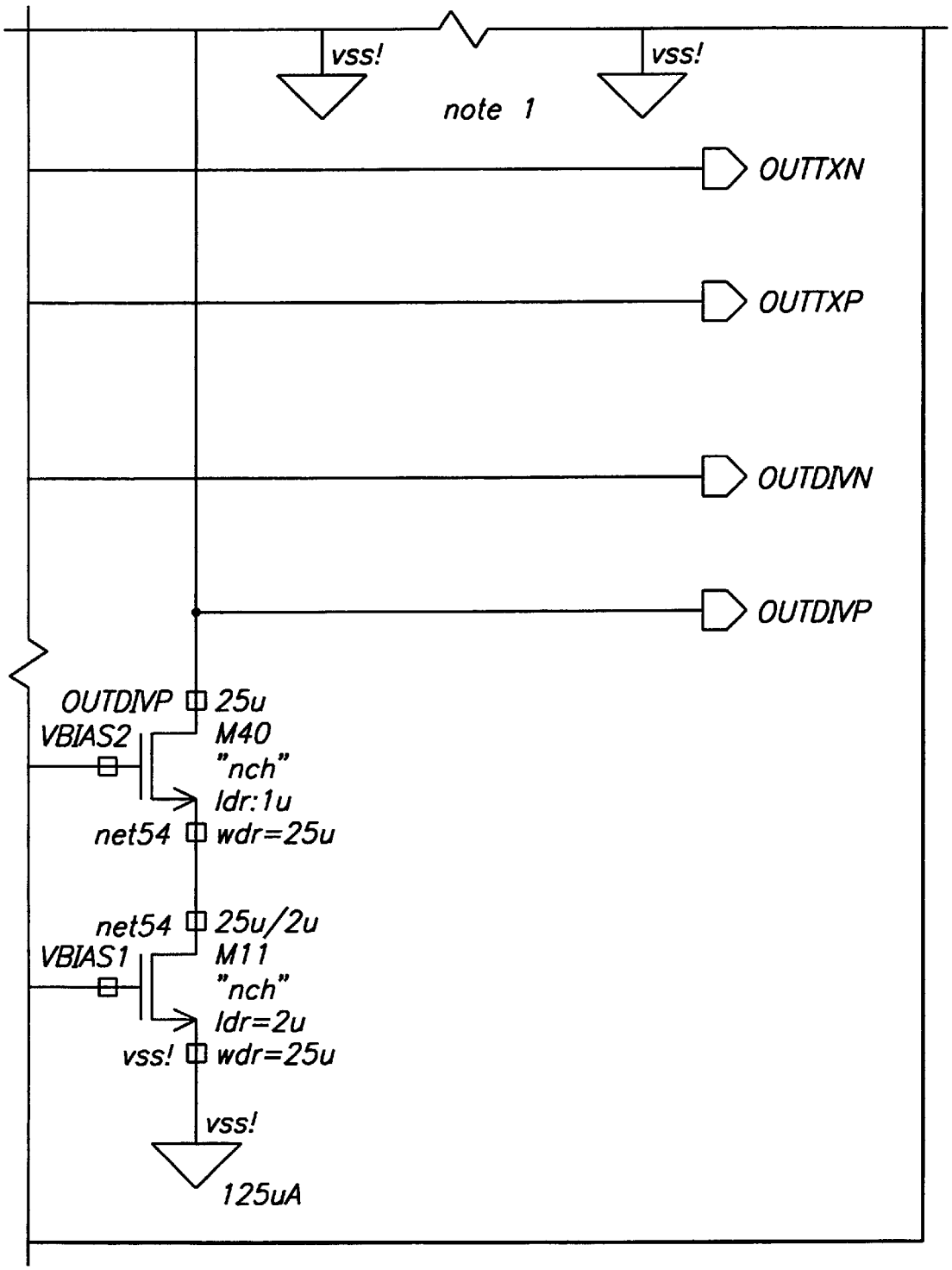


Fig 8.060102401BD

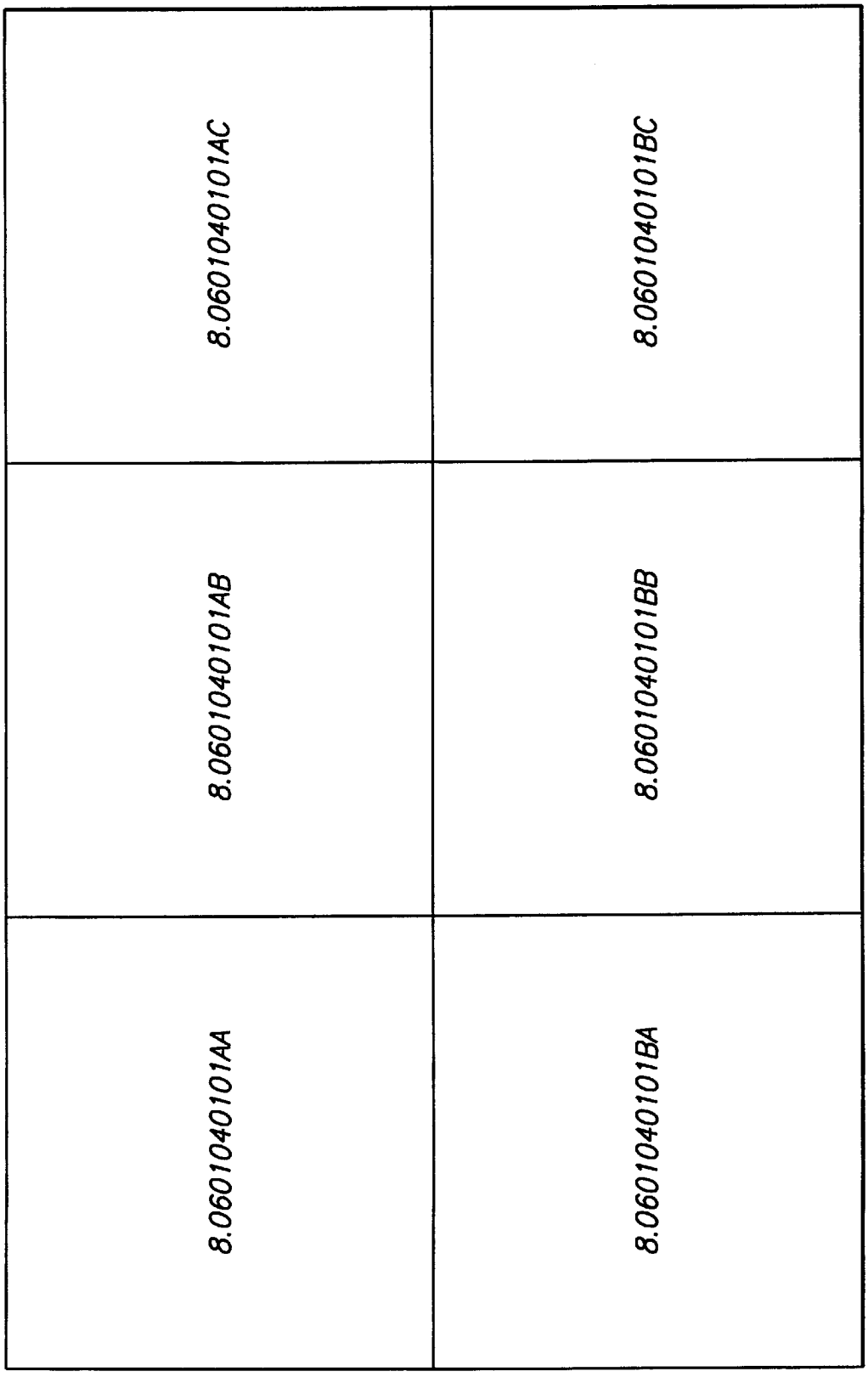


FIG. 8.060104010000

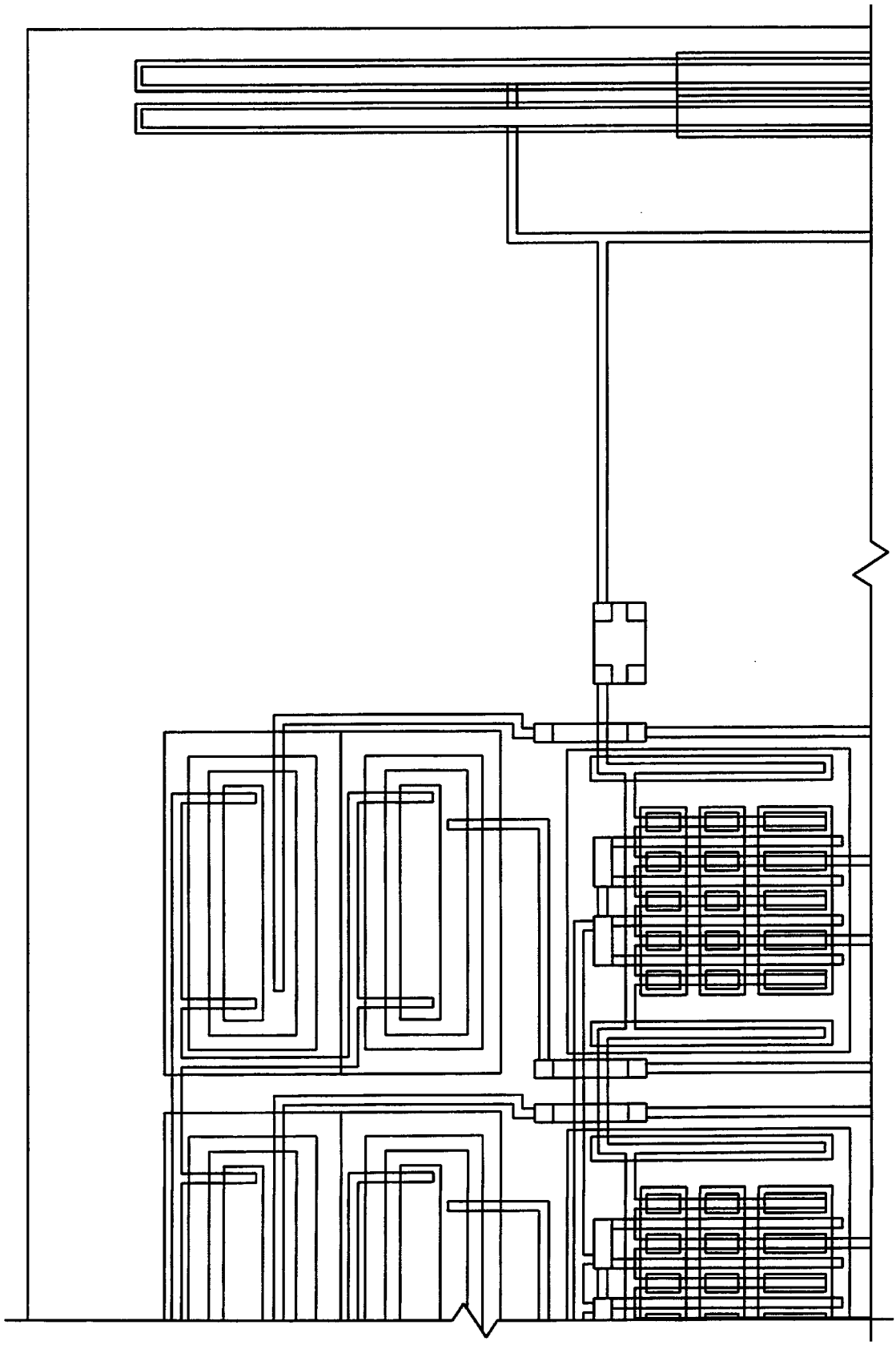


Fig. 8,060,10-4,010,10,10,10,AA

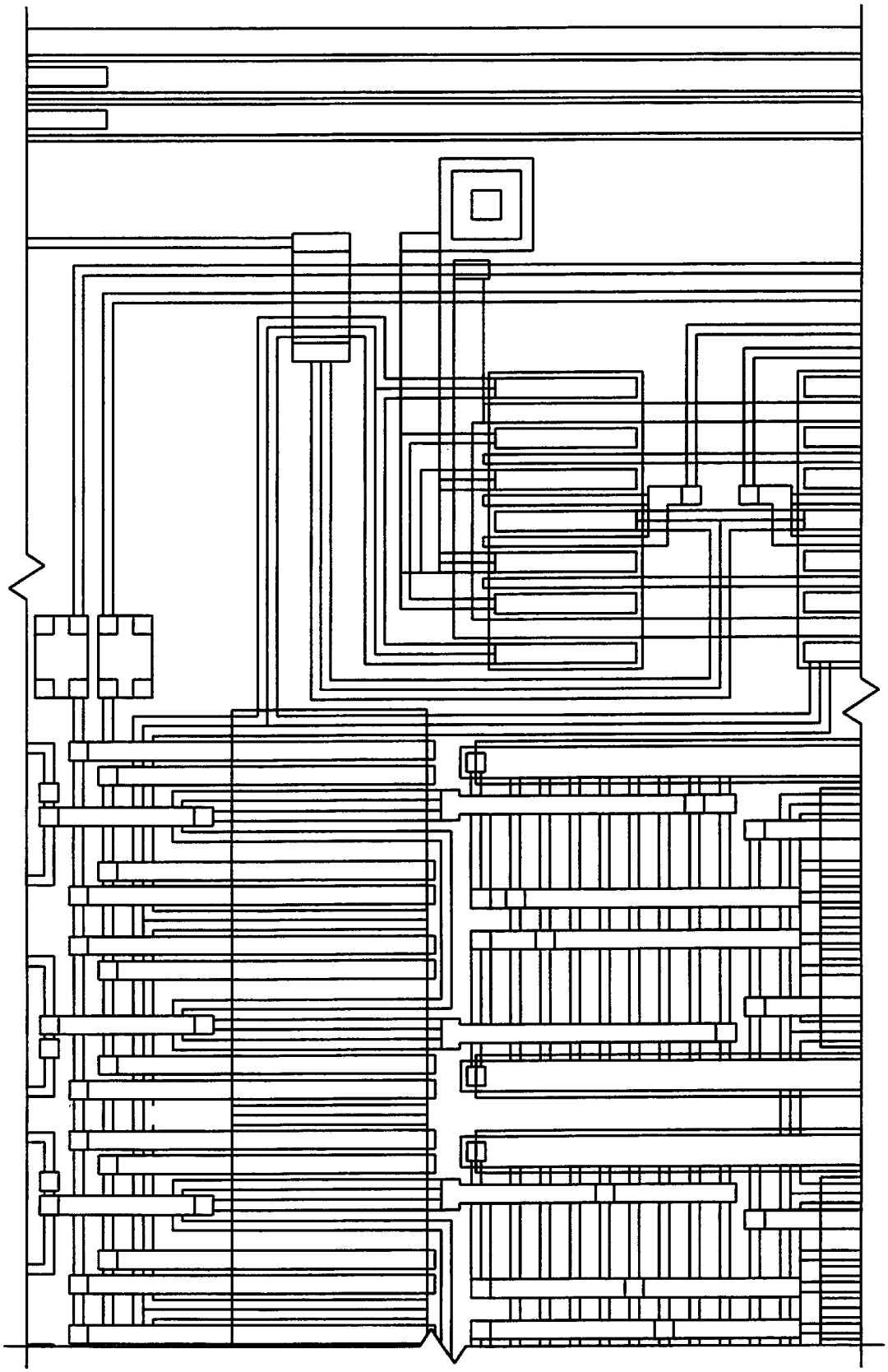


Fig 88.0600100400100AB

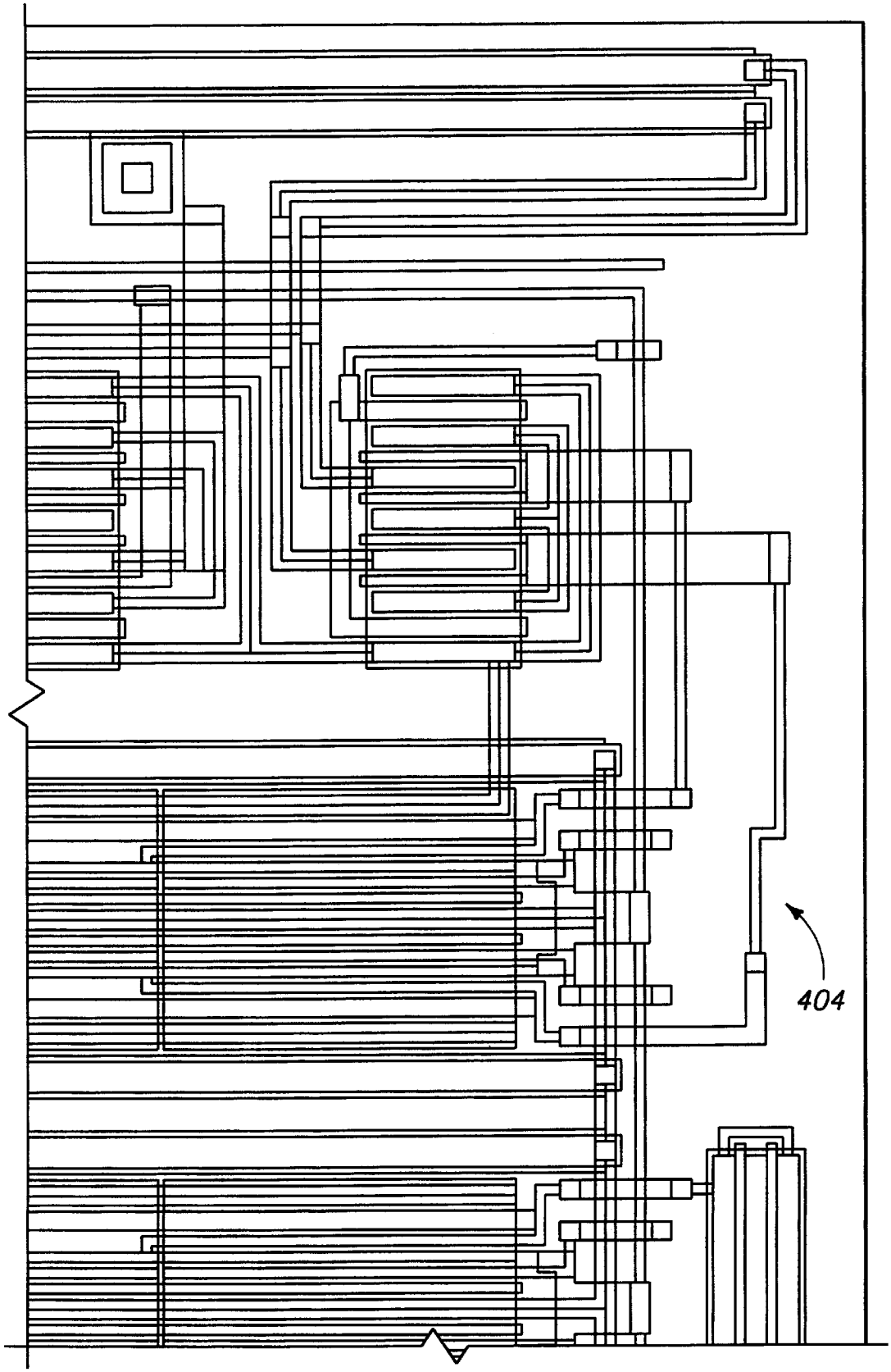


FIG 8.0600100-40100AC

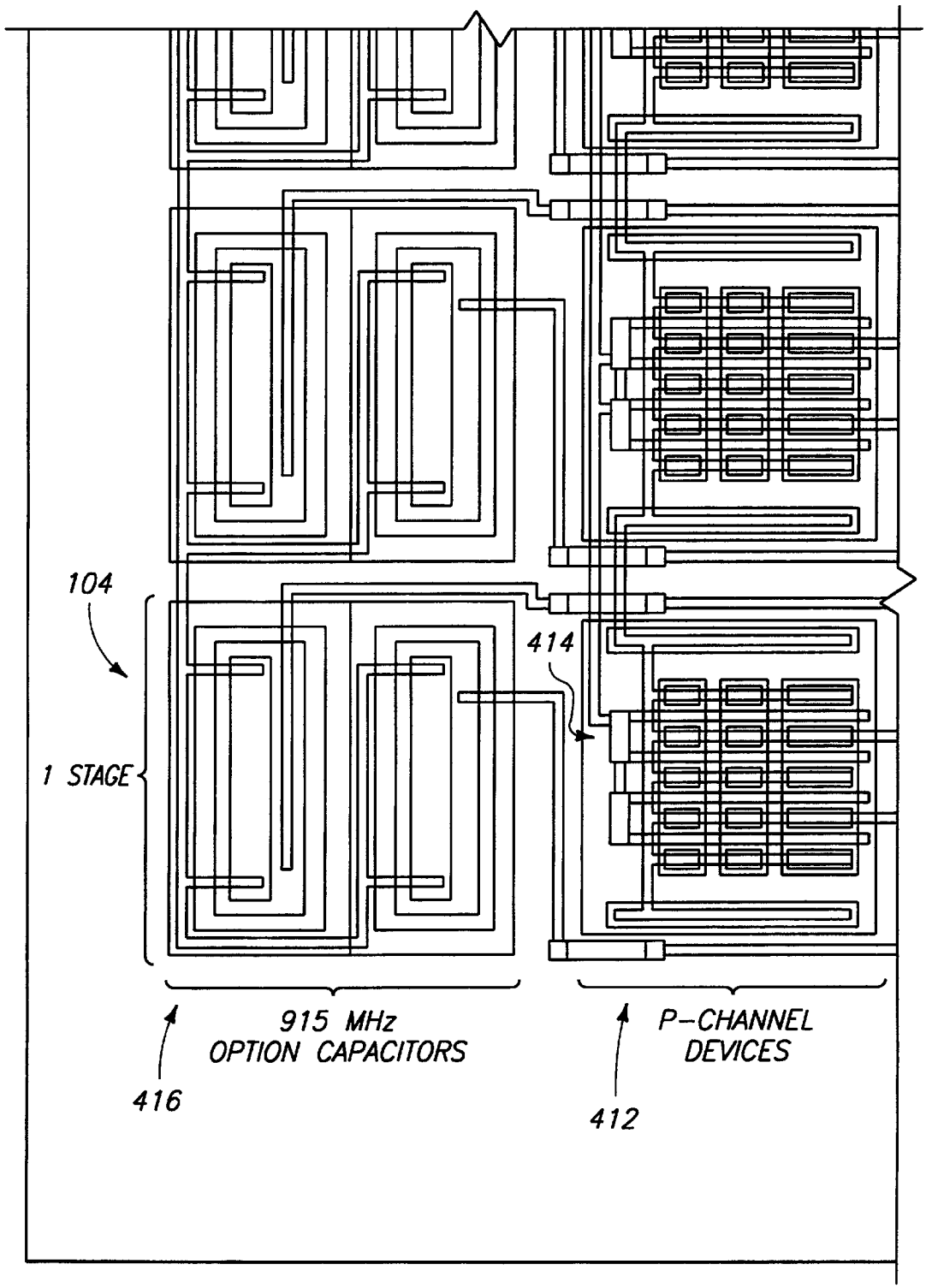


Fig 8B.0601-0101BA

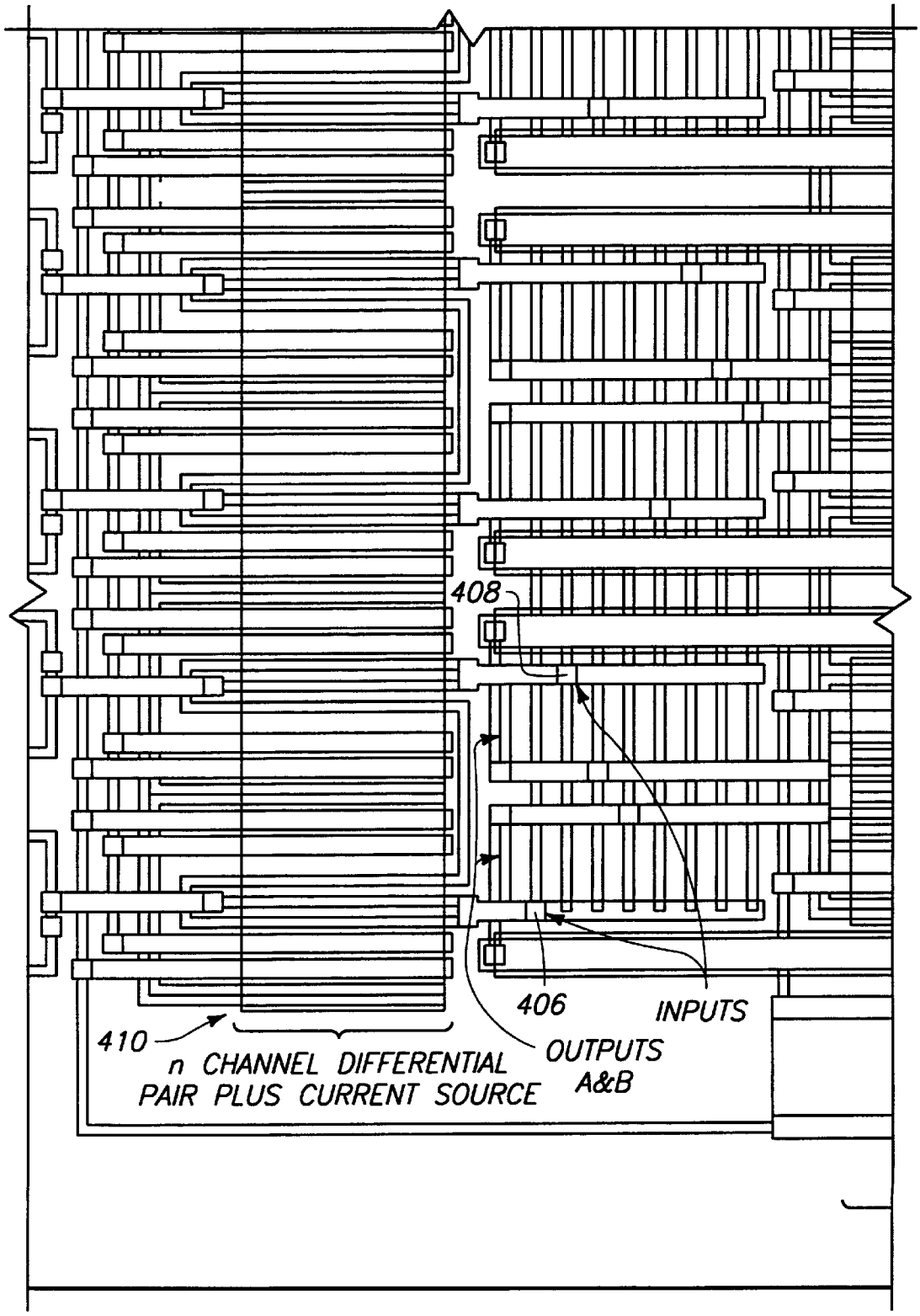


Fig 8B0601-0100188

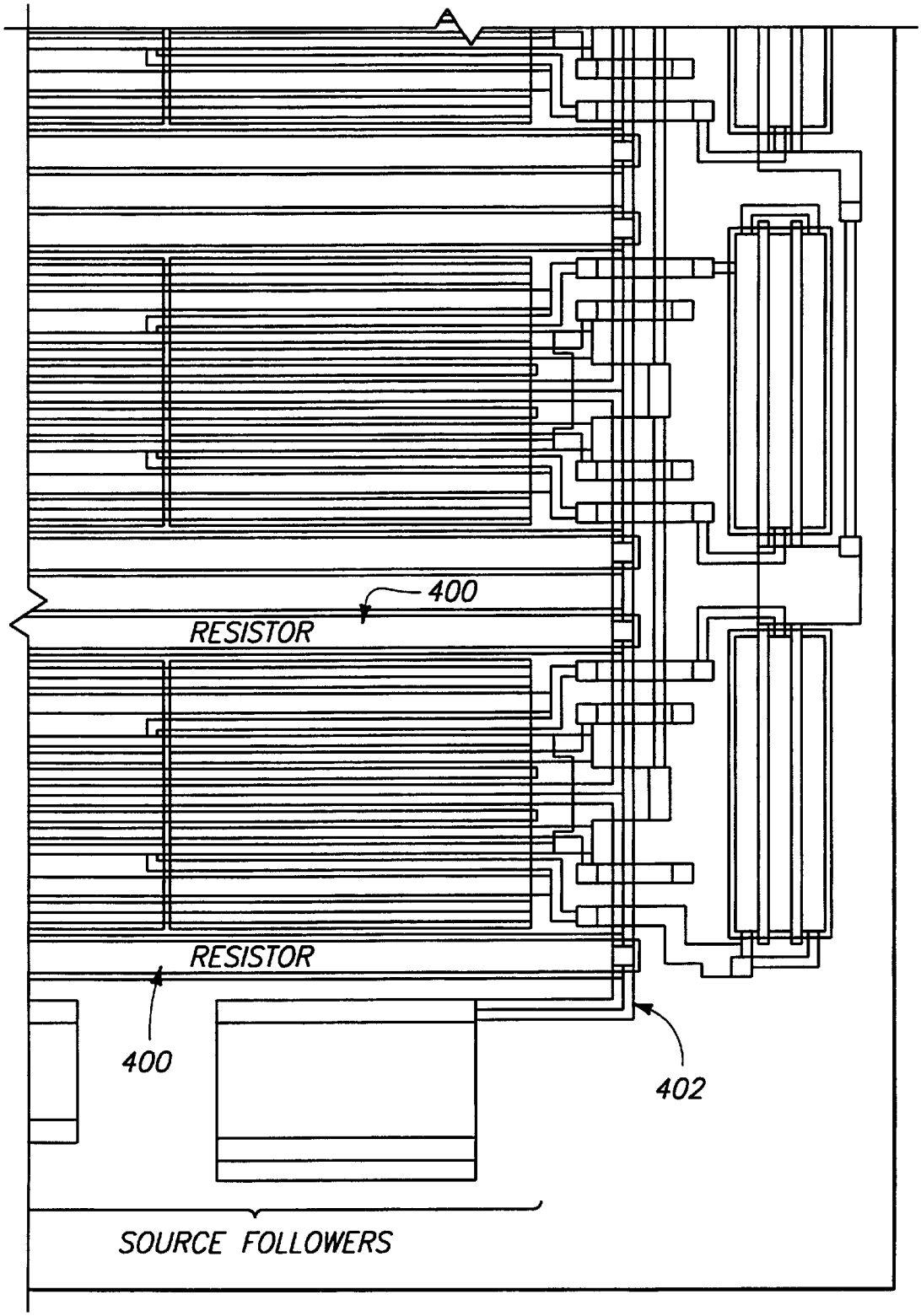
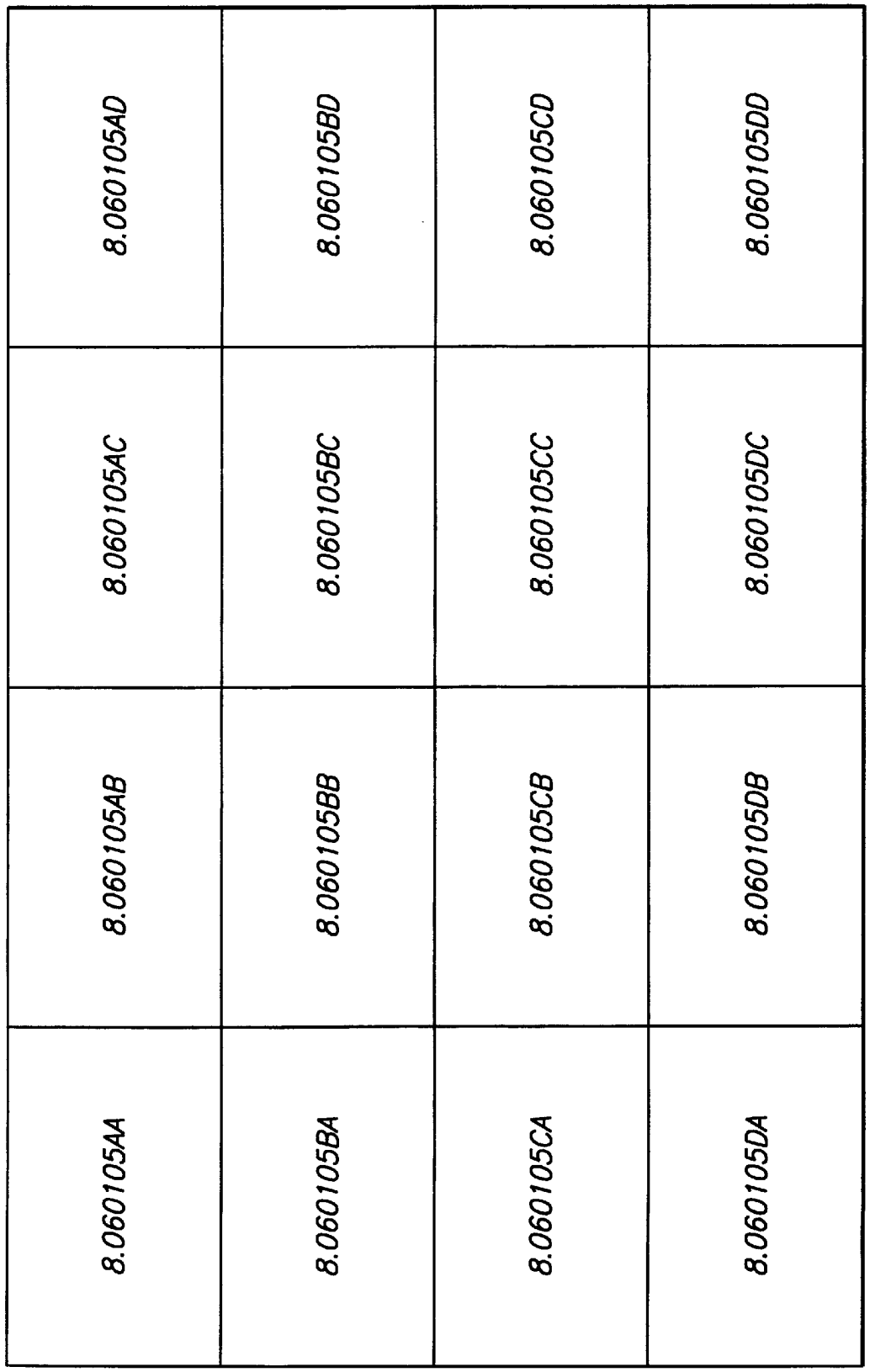


Fig 88.0610401BC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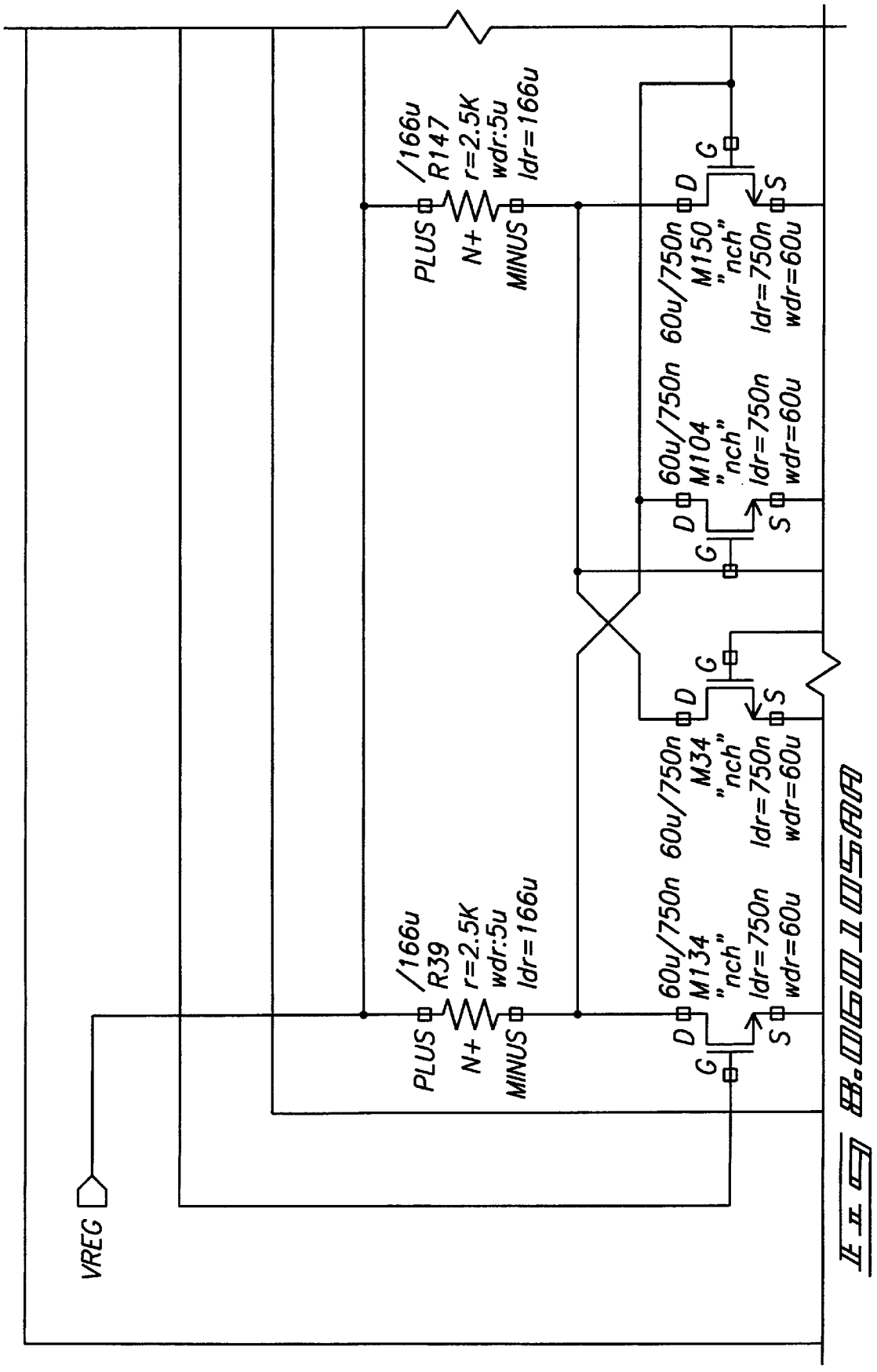
8.060105AB
8.060105AC
8.060105AD
8.060105BA
8.060105BB
8.060105BC
8.060105BD
8.060105CA
8.060105CB
8.060105CC
8.060105CD
8.060105DA
8.060105DB
8.060105DC
8.060105DD

FIG 8.060105



Фиг. 89.0050 II

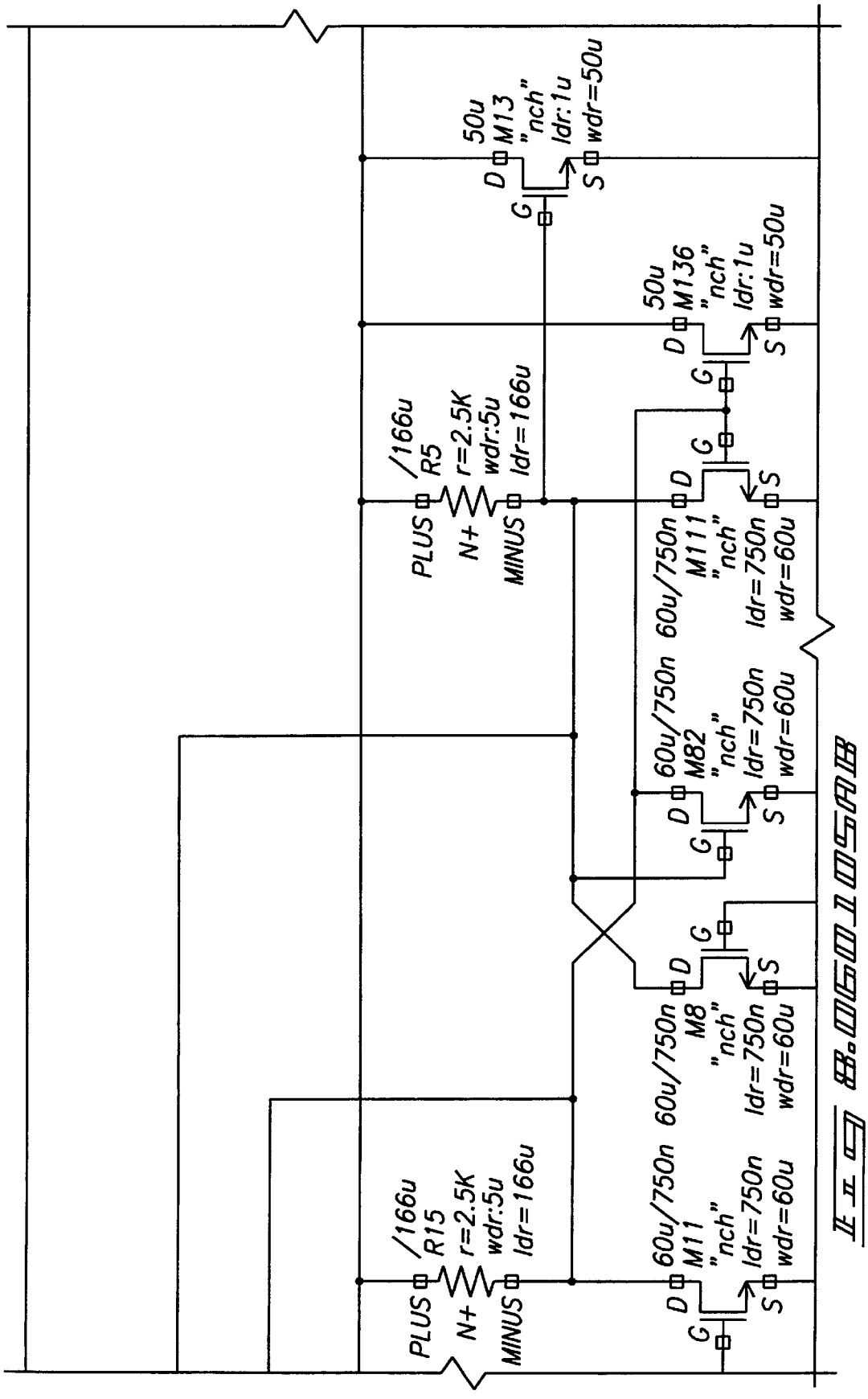
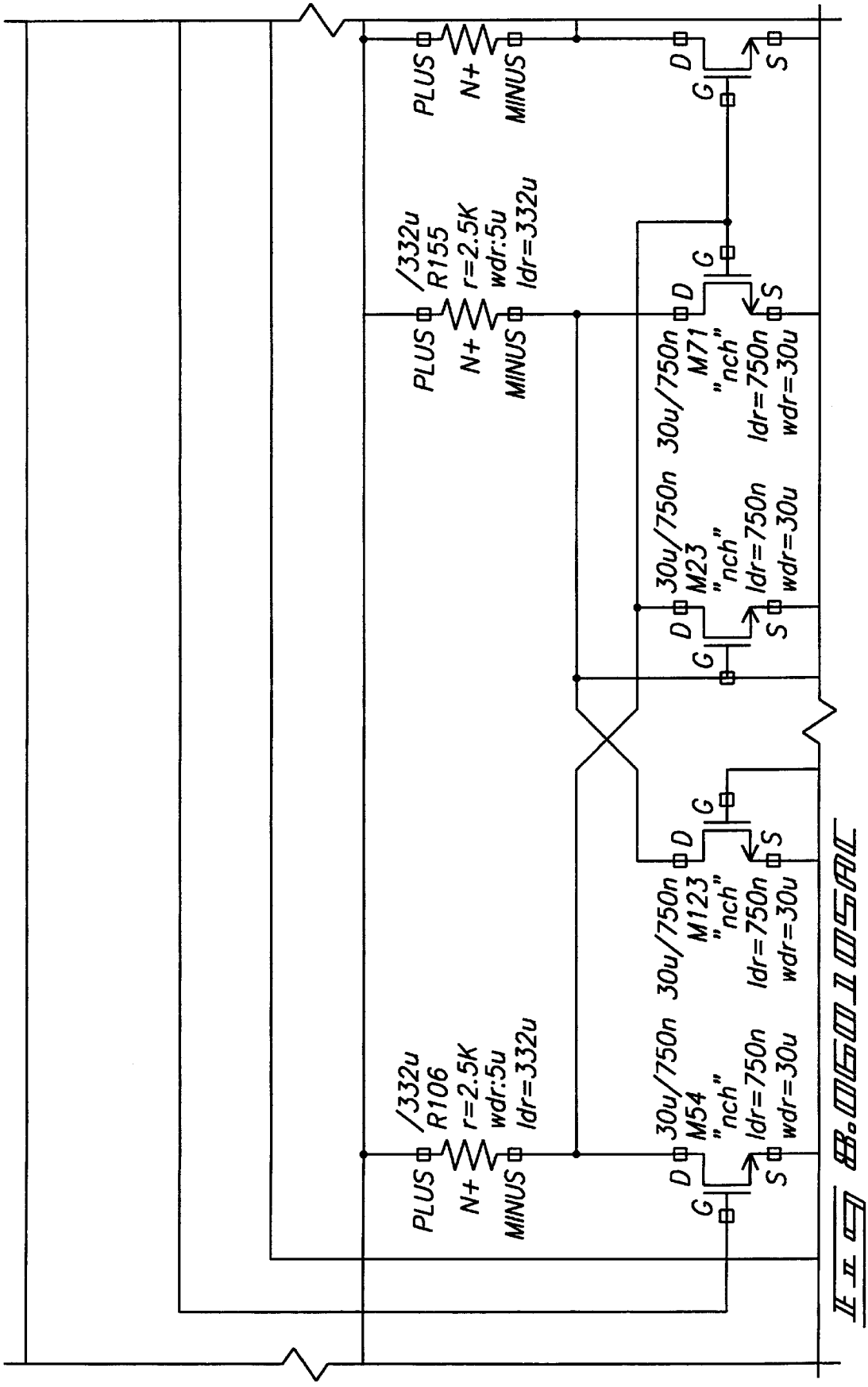
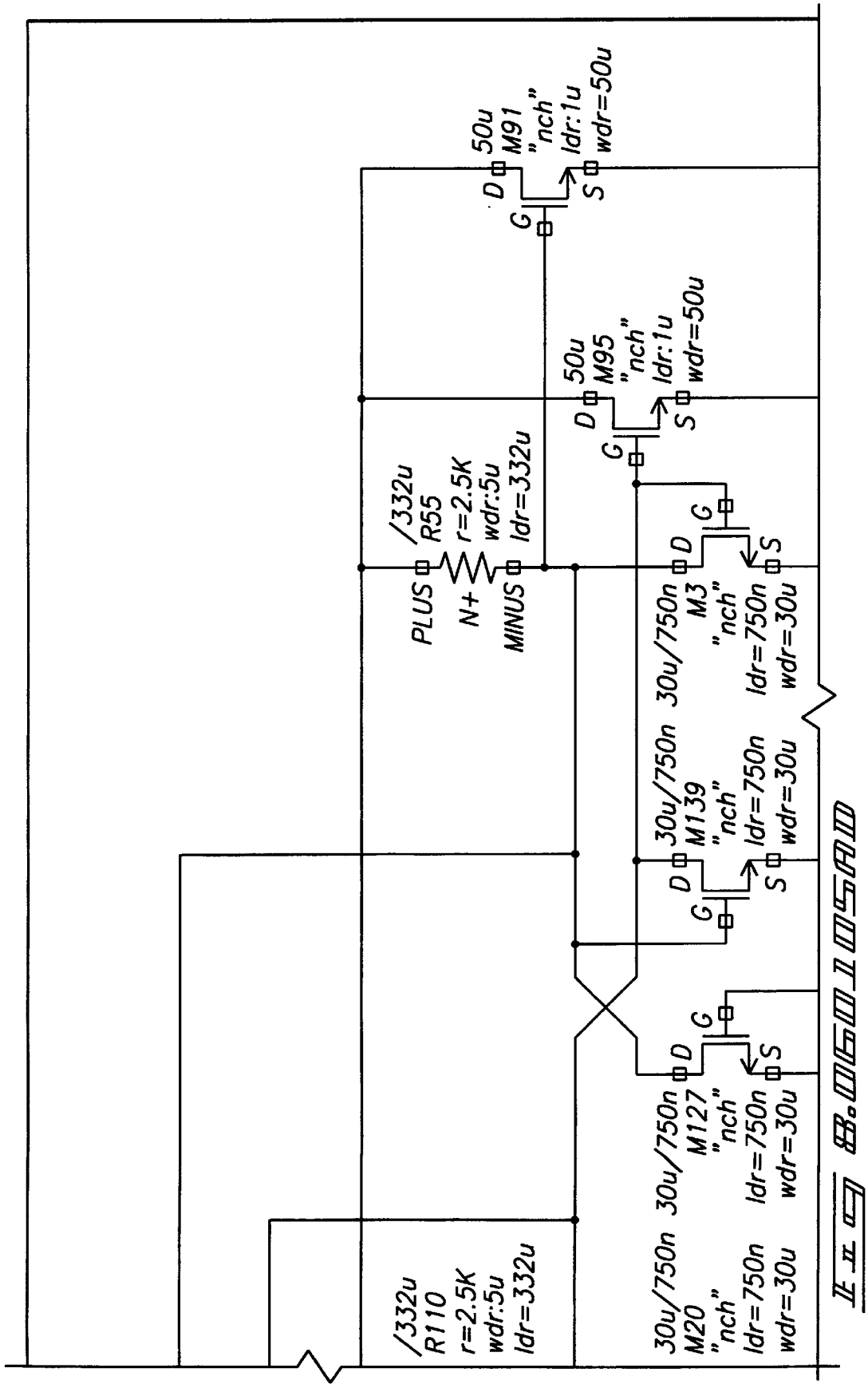


Fig. 88. MOSCAP


PLUS
N+
MINUS
/332u
R155
r=2.5K
wdr:5u
ldr=332u
/332u
R106
r=2.5K
wdr:5u
ldr=332u
D
G
S
30u/750n
M71
"nch"
ldr=750n
wdr=30u
M23
M123
M54


50u
M91
"nch"
ldr:1u
wdr=50u
D
G
S
50u
M95
"nch"
ldr:1u
wdr=50u
/332u
R55
r=2.5K
wdr:5u
ldr=332u
PLUS
N+
MINUS
30u/750n
M3
"nch"
ldr=750n
wdr=30u
30u/750n
M139
"nch"
ldr=750n
wdr=30u
30u/750n
M127
"nch"
ldr=750n
wdr=30u
/332u
R110
r=2.5K
wdr:5u
ldr=332u
30u/750n
M20
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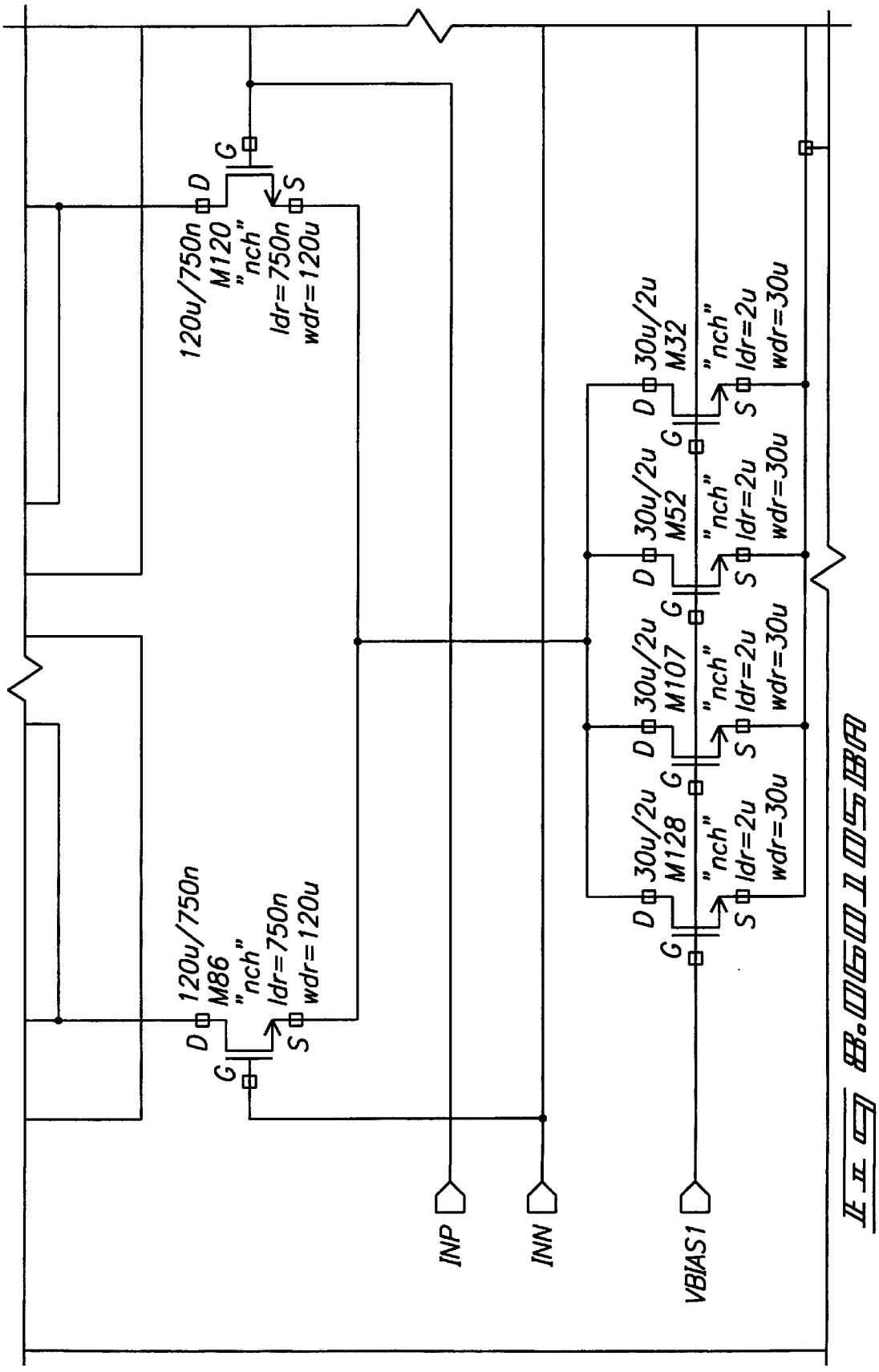
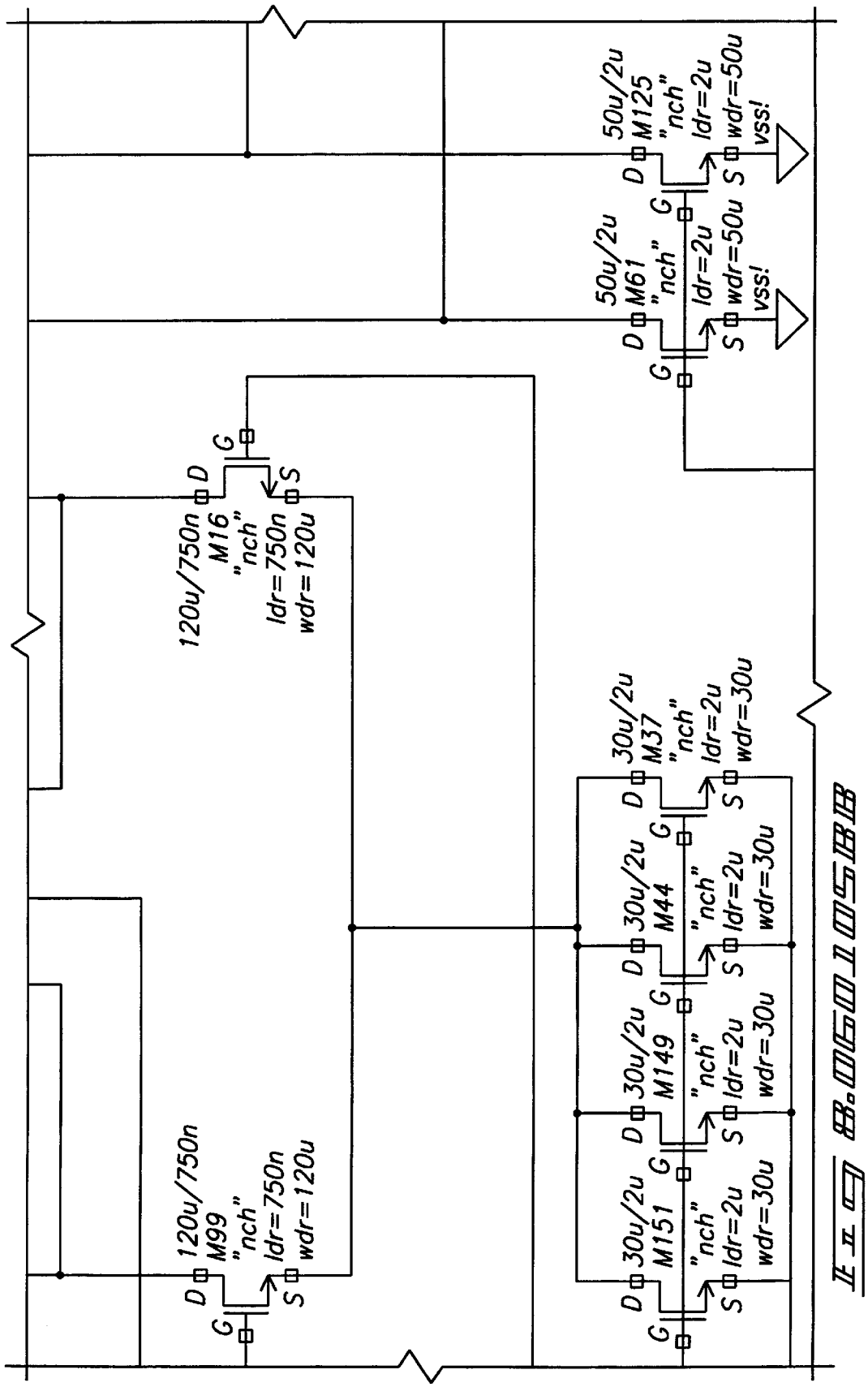
ldr=750n
wdr=30u
FIG. 88.0050 1005A00


120u/750n
M120
"nch"
ldr=750n
wdr=120u
D
G
S
120u/750n
M86
"nch"
ldr=750n
wdr=120u
30u/2u
M32
30u/2u
M52
30u/2u
M107
30u/2u
M128
"nch"
ldr=2u
wdr=30u
INP
INN
VBIAS1

Фиг. 1910


50u/2u
M125
"nch"
ldr=2u
wdr=50u
vss!
50u/2u
M61
"nch"
ldr=2u
wdr=50u
vss!
120u/750n
M16
"nch"
ldr=750n
wdr=120u
30u/2u
M37
"nch"
ldr=2u
wdr=30u
30u/2u
M44
"nch"
ldr=2u
wdr=30u
30u/2u
M149
"nch"
ldr=2u
wdr=30u
30u/2u
M151
"nch"
ldr=2u
wdr=30u
120u/750n
M99
"nch"
ldr=750n
wdr=120u
D
G
S

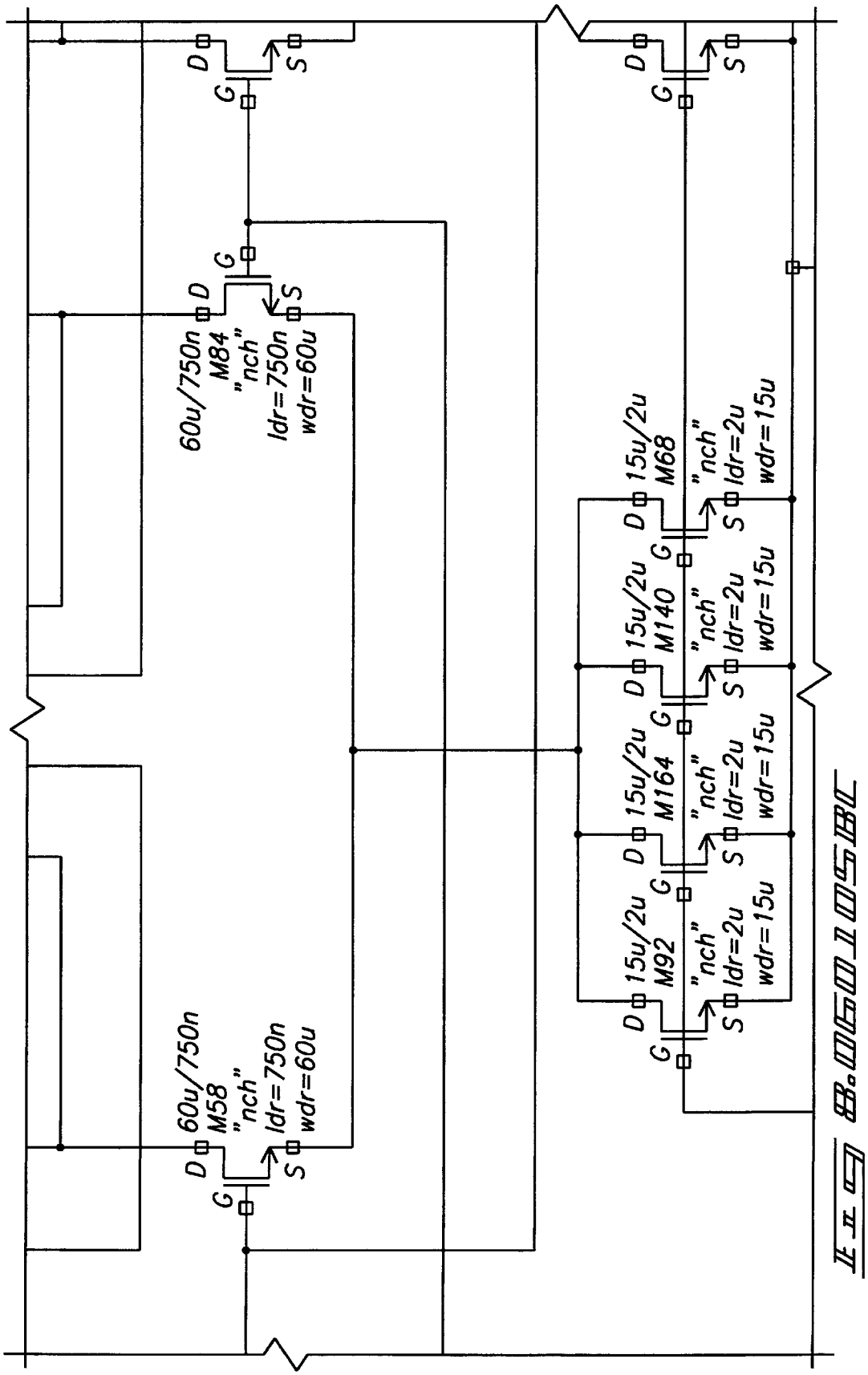


Fig. 88,005,188

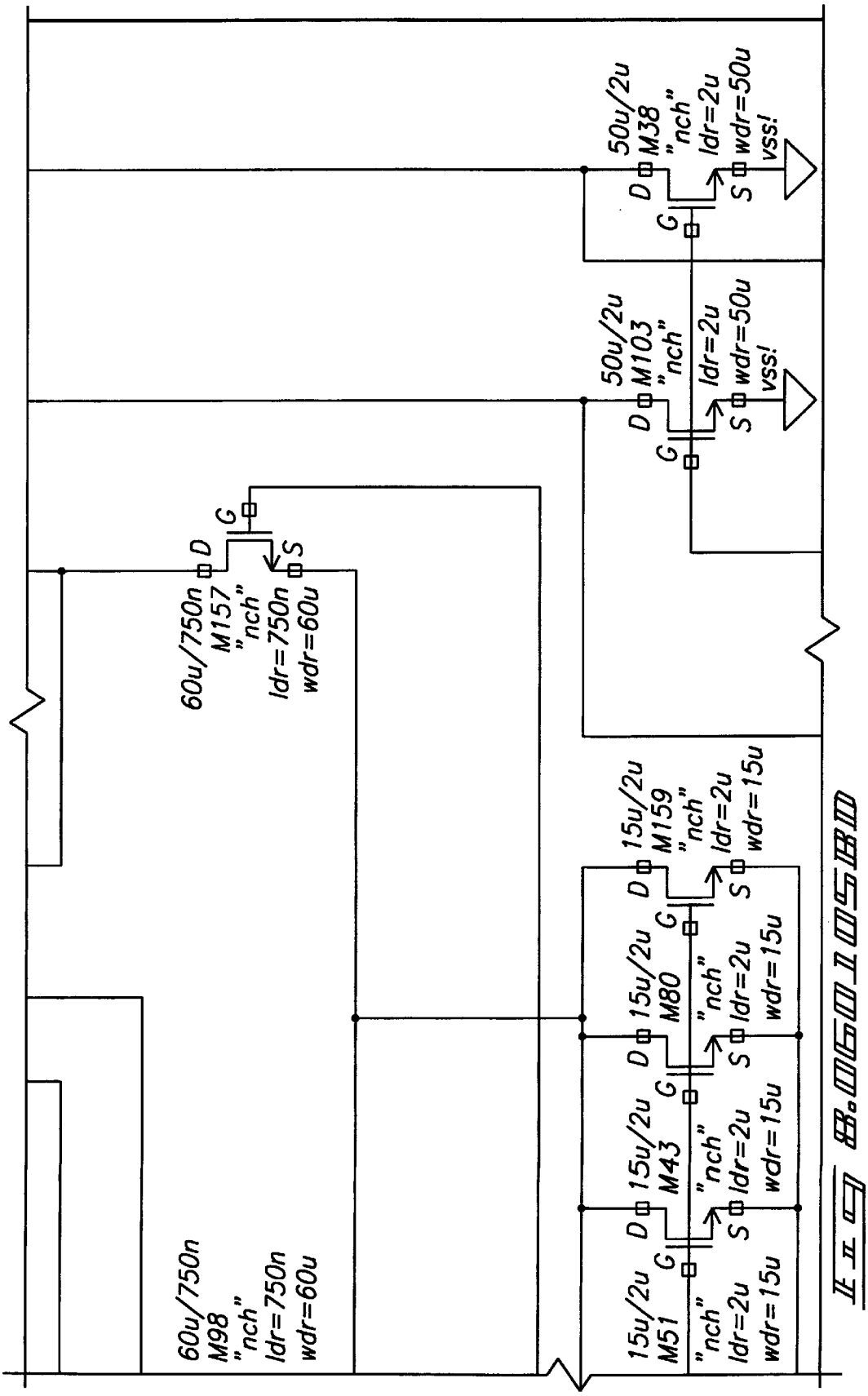

50u/2u
M38
"nch"
ldr=2u
wdr=50u
vss!
50u/2u
M103
"nch"
ldr=2u
wdr=50u
vss!
60u/750n
M157
"nch"
ldr=750n
wdr=60u
15u/2u
M159
"nch"
ldr=2u
wdr=15u
15u/2u
M80
"nch"
ldr=2u
wdr=15u
15u/2u
M43
"nch"
ldr=2u
wdr=15u
15u/2u
M51
"nch"
ldr=2u
wdr=15u
60u/750n
M98
"nch"
ldr=750n
wdr=60u
D
G
S

FIG. 88.0050

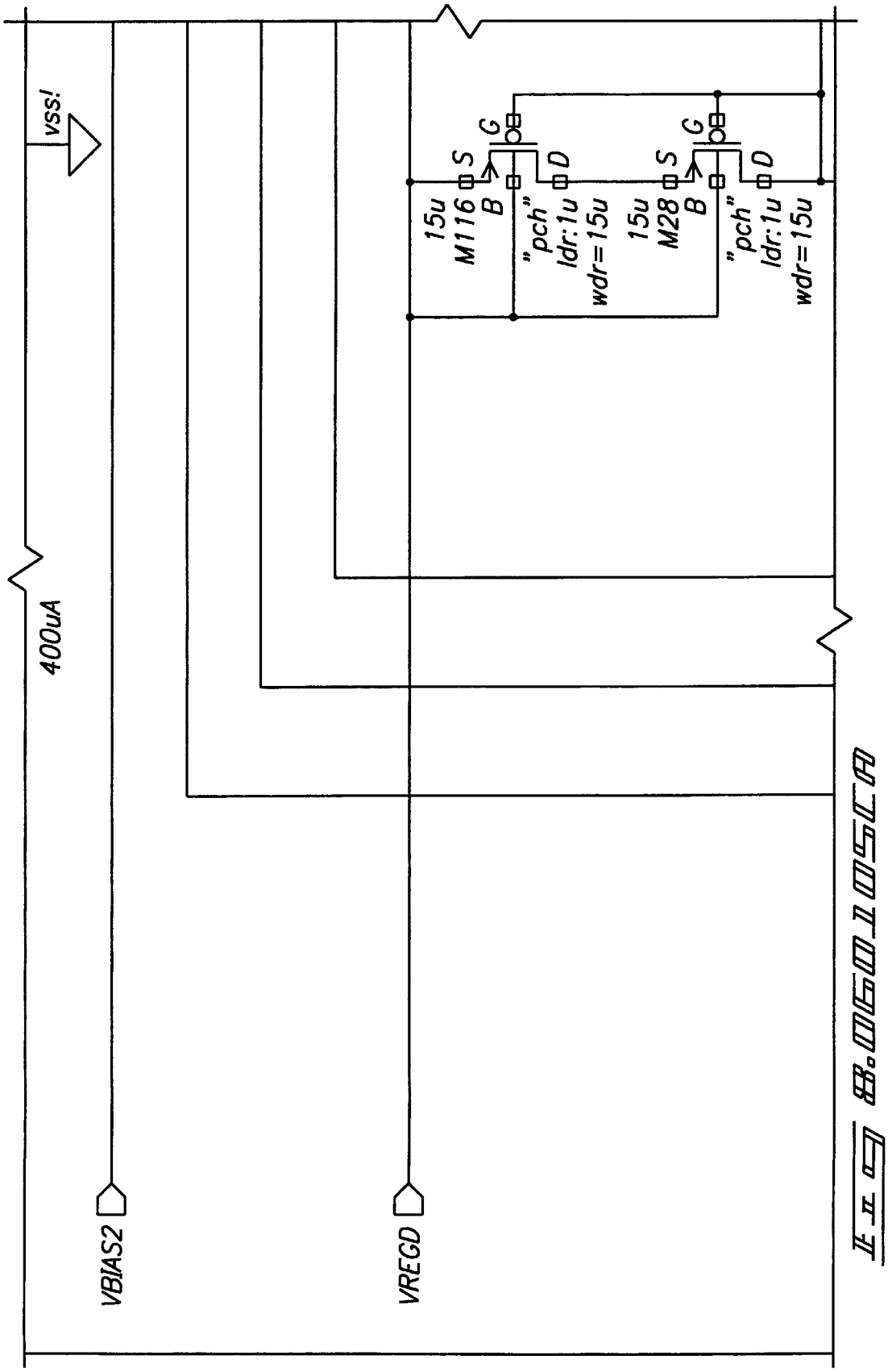
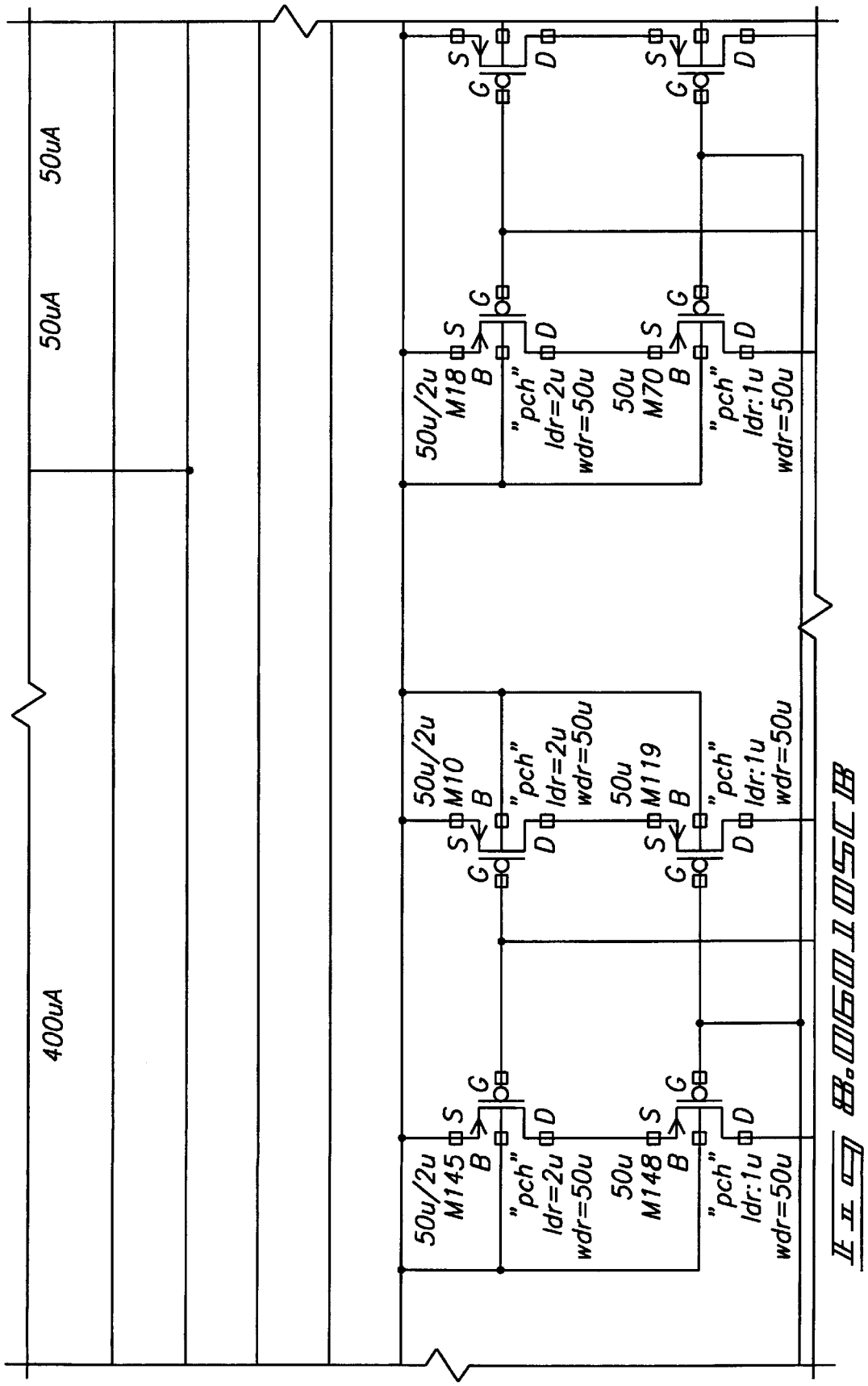
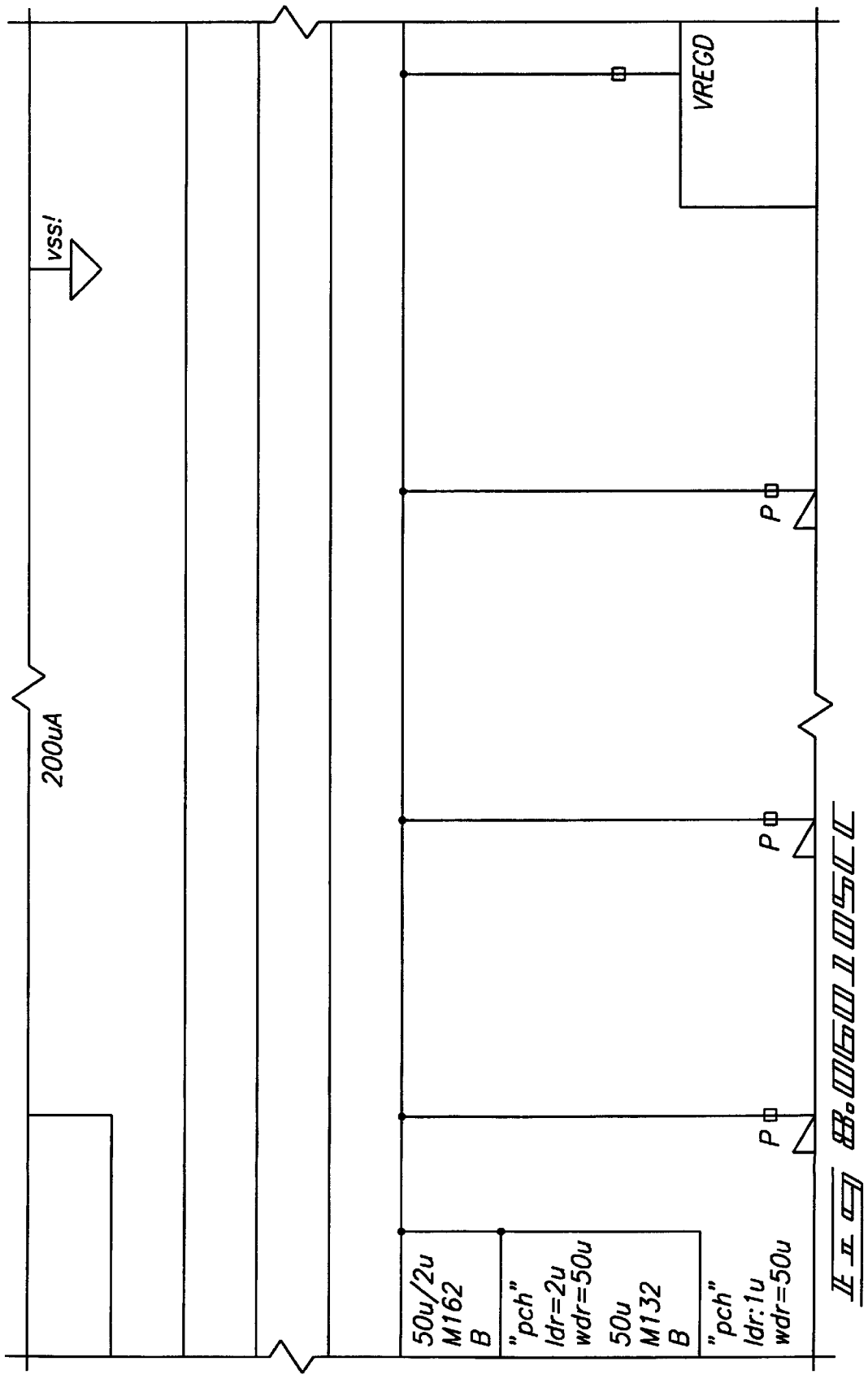
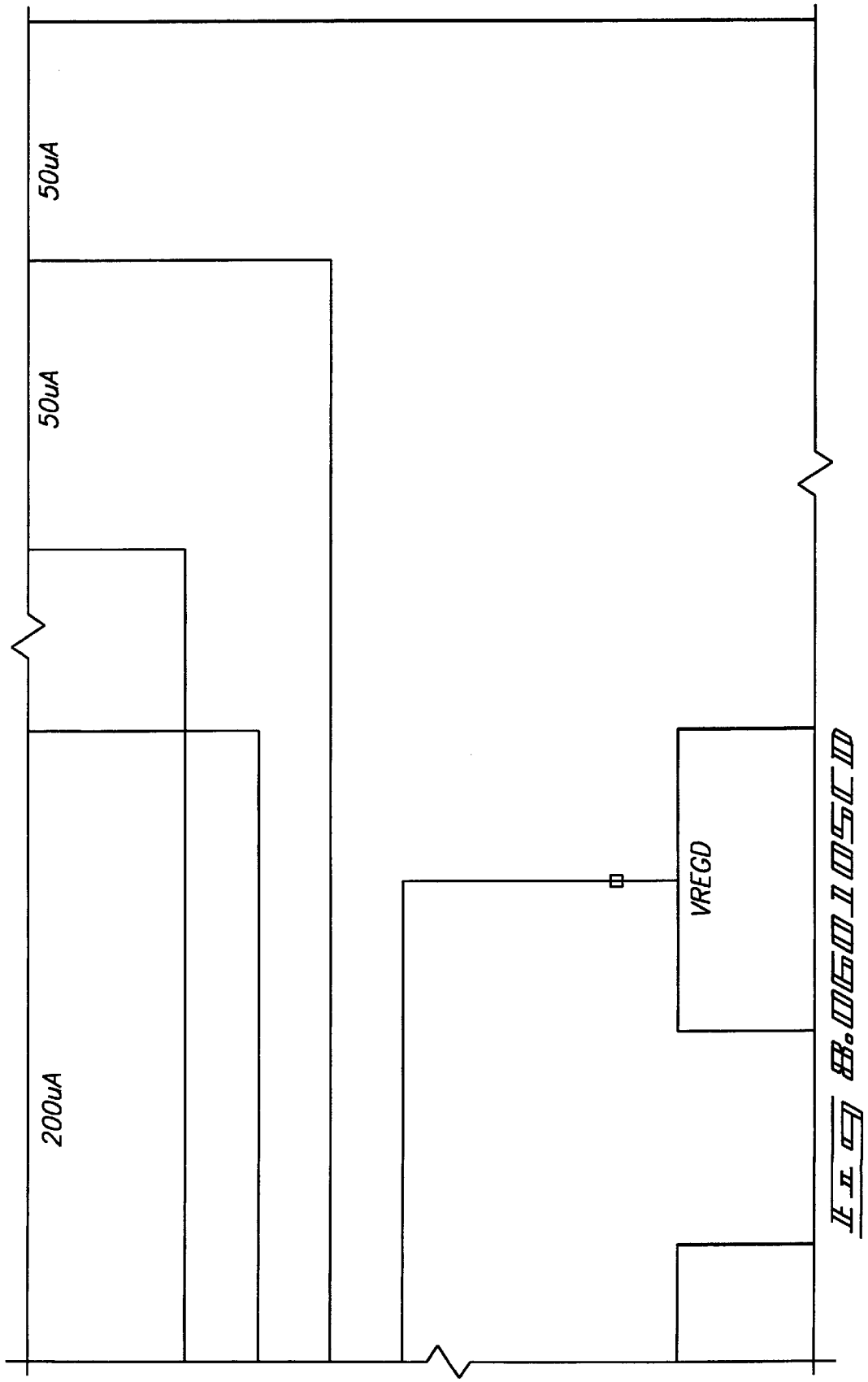

vss!
400uA
VBIAS2
VREGD
15u
M116
B
S
G
D
"pch"
ldr:1u
wdr=15u
15u
M28
B
S
G
D
"pch"
ldr:1u
wdr=15u

Fig 88.0500A


50uA
50uA
400uA
50u/2u M18 B "pch" ldr=2u wdr=50u
50u M70 B "pch" ldr:1u wdr=50u
50u/2u M10 B "pch" ldr=2u wdr=50u
50u M119 B "pch" ldr:1u wdr=50u
50u/2u M145 B "pch" ldr=2u wdr=50u
50u M148 B "pch" ldr:1u wdr=50u
S G D

Фиг. 88.00500


VREGD
vss!
200uA
P
P
P
50u/2u
M162
B
"pch"
ldr=2u
wdr=50u
50u
M132
B
"pch"
ldr:1u
wdr=50u


50uA
50uA
200uA
VREGD
FIG. 98.0500.1050

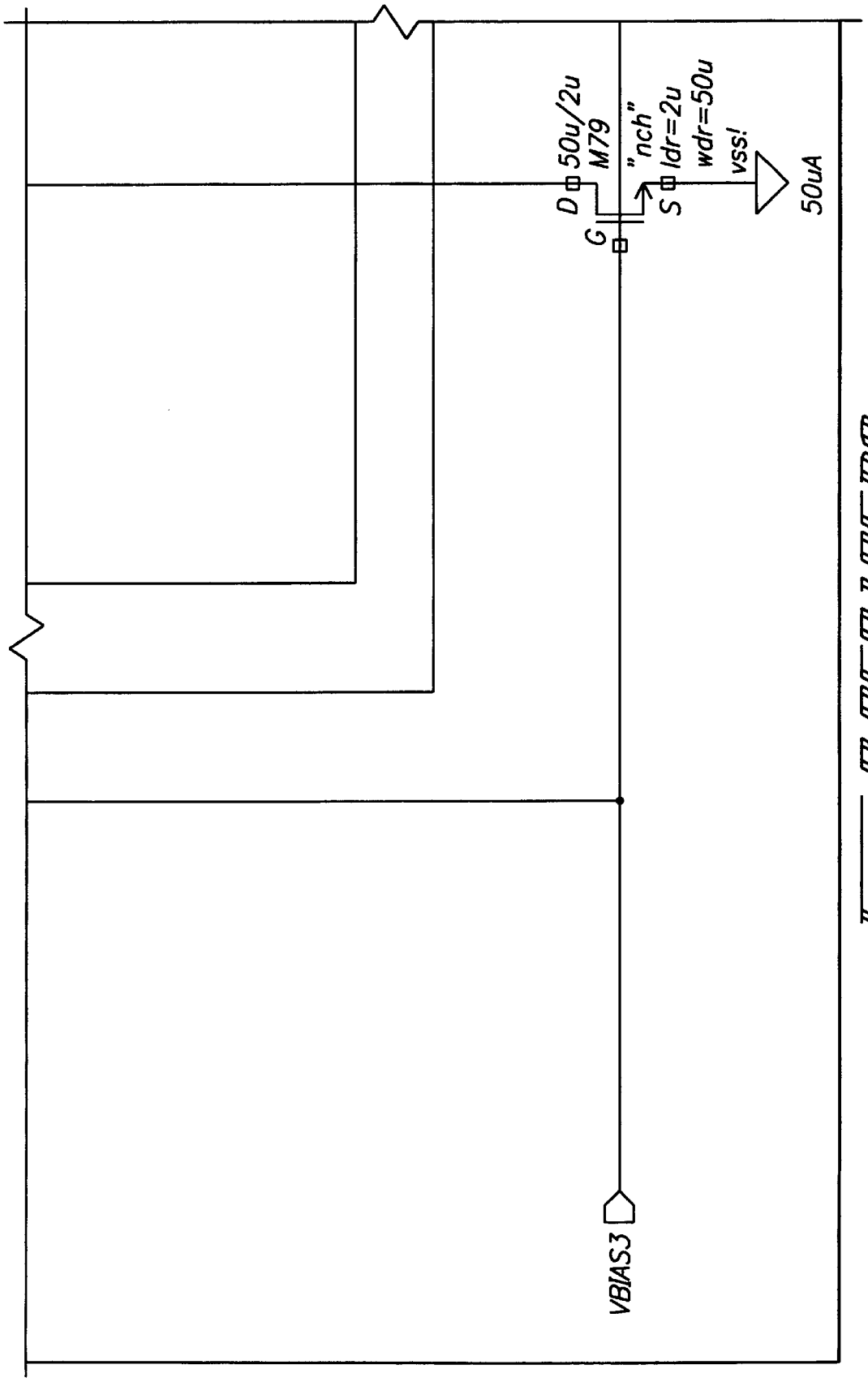
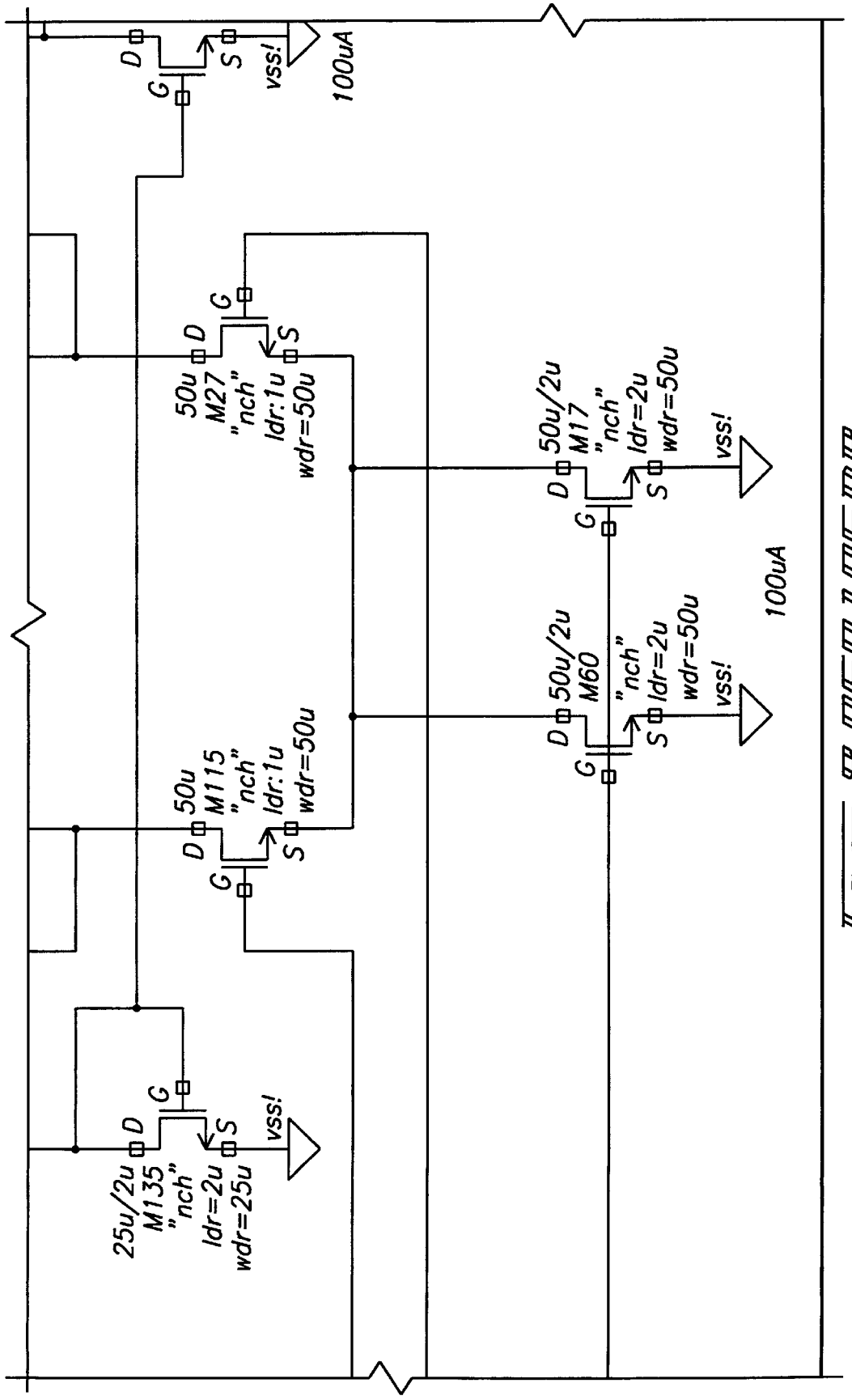


FIG 8.0501DA


D
G
S
vss!
100uA
50u
M27
"nch"
ldr:1u
wdr=50u
50u/2u
M17
"nch"
ldr=2u
wdr=50u
50u/2u
M60
"nch"
ldr=2u
wdr=50u
50u
M115
"nch"
ldr:1u
wdr=50u
25u/2u
M135
"nch"
ldr=2u
wdr=25u

Фиг. 88.0050

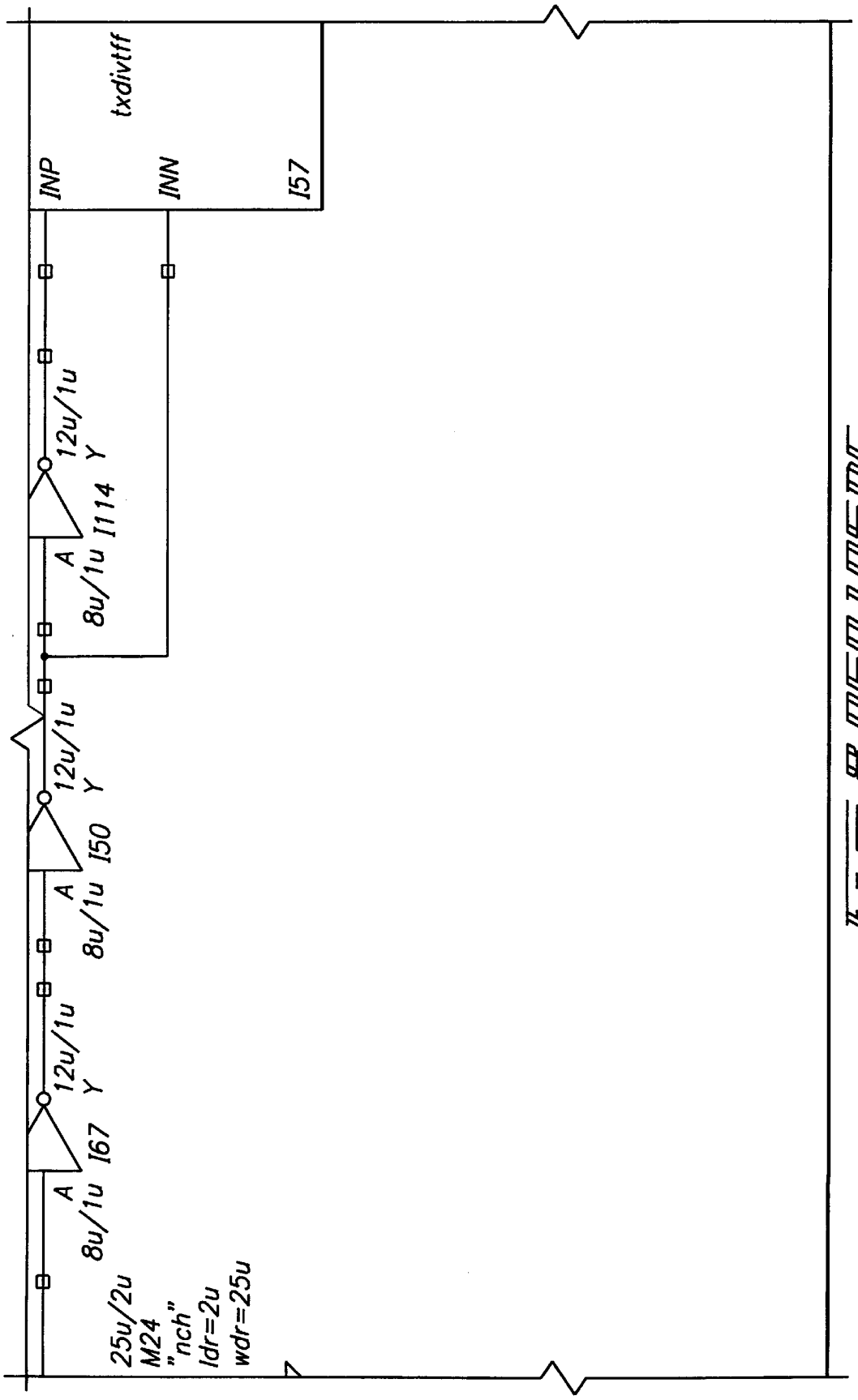

txdivtff
INP
INN
I57
12u/1u
Y
I114
A
8u/1u
12u/1u
Y
I50
A
8u/1u
12u/1u
Y
I67
A
8u/1u
25u/2u
M24
"nch"
ldr=2u
wdr=25u

FIG 1050.8

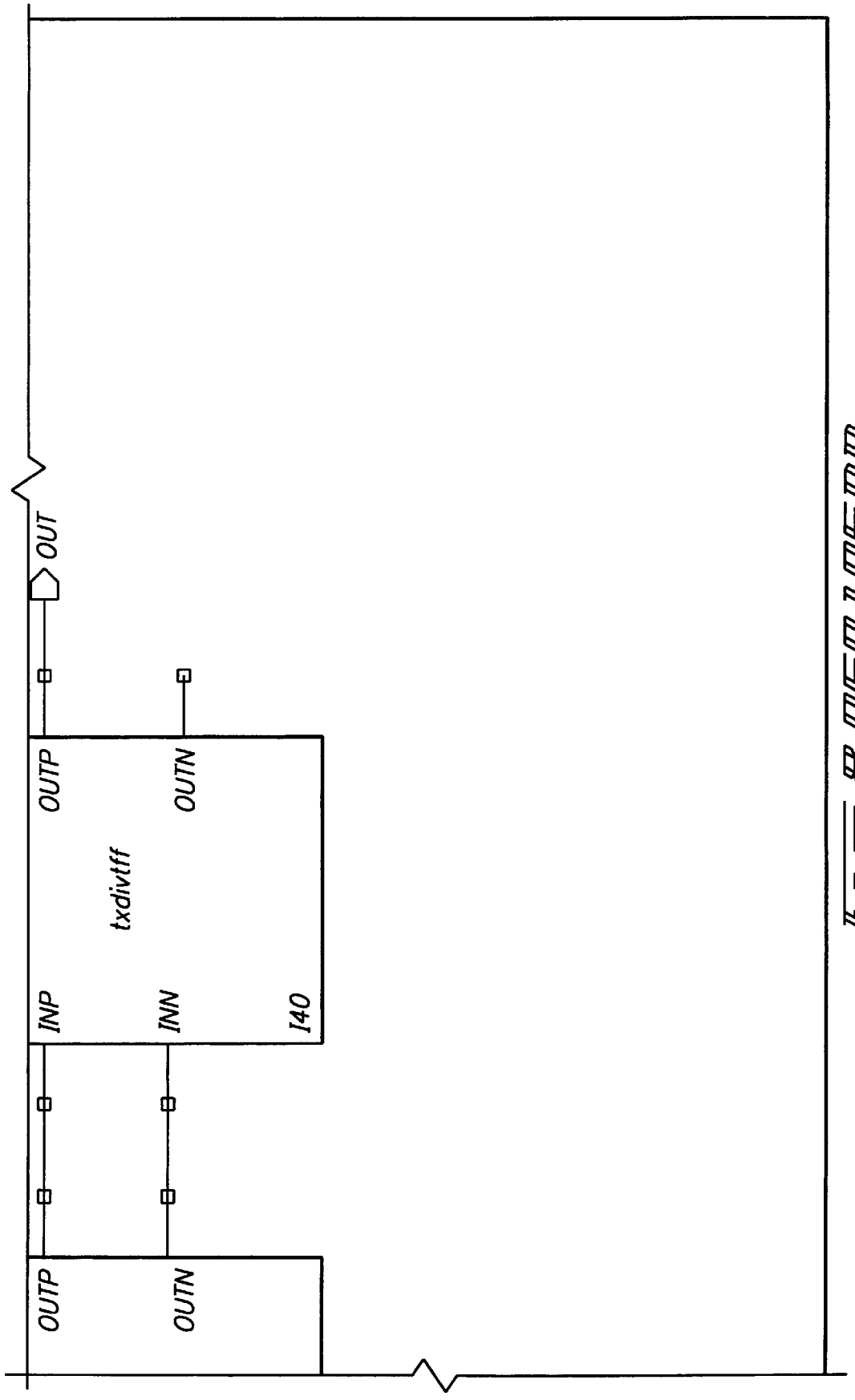


FIG 8,050,1050

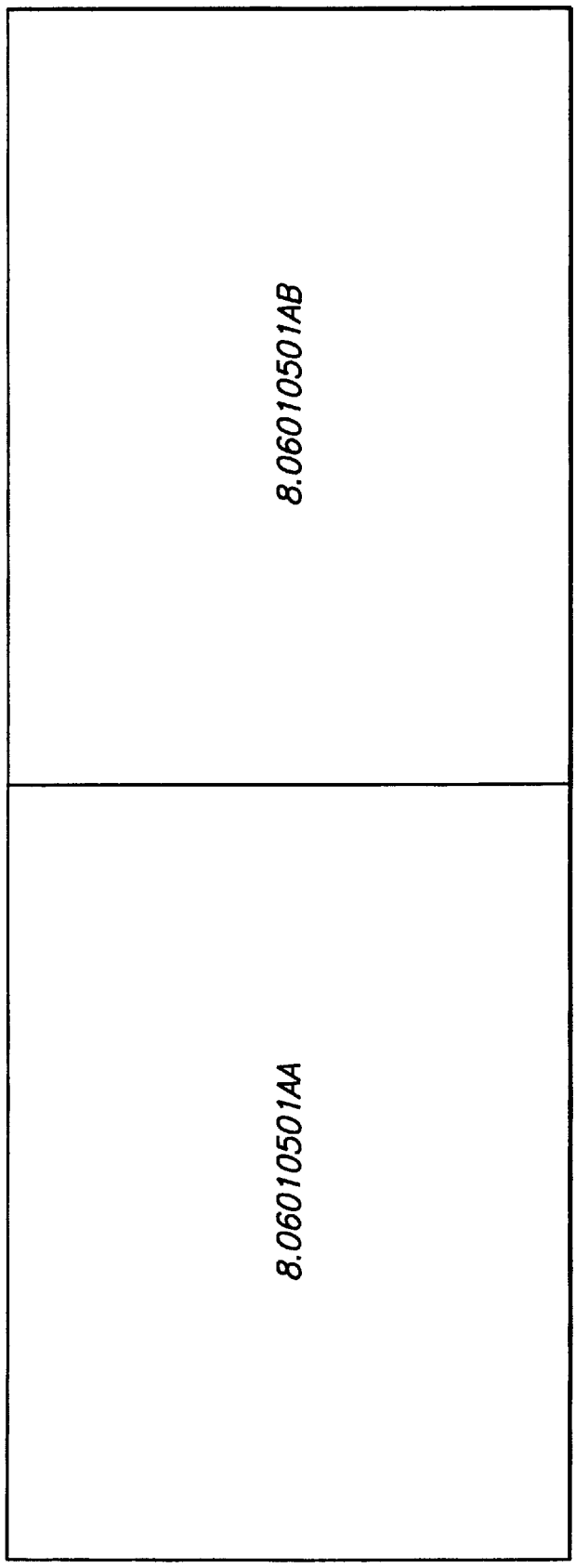


FIG 8.06010501

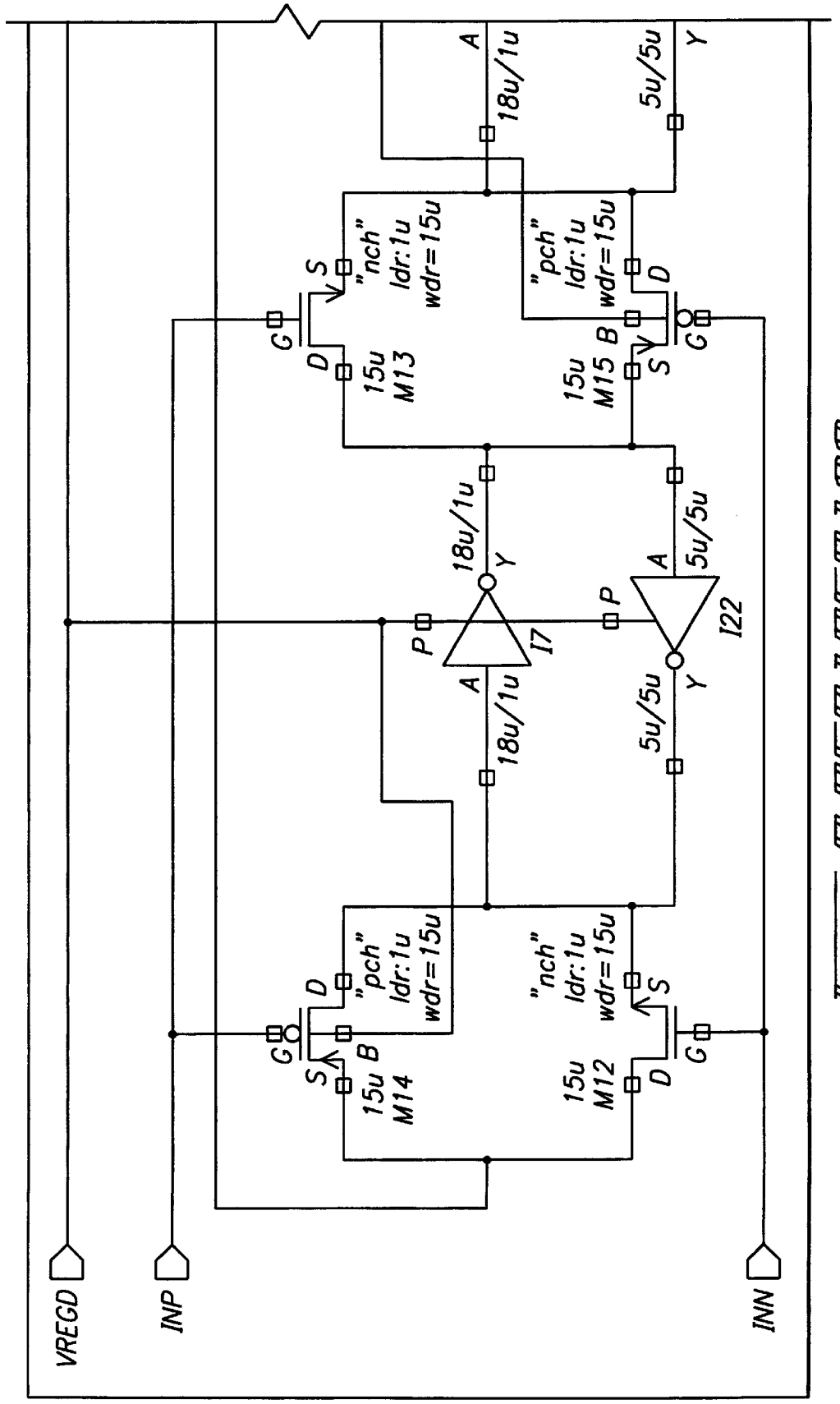

VREGD
INP
INN
A
18u/1u
Y
5u/5u
"nch"
ldr:1u
wdr=15u
"pch"
ldr:1u
wdr=15u
S
D
G
B
15u
M13
15u
M15
15u
M14
15u
M12
P
I7
I22

FIG 8.0501AA

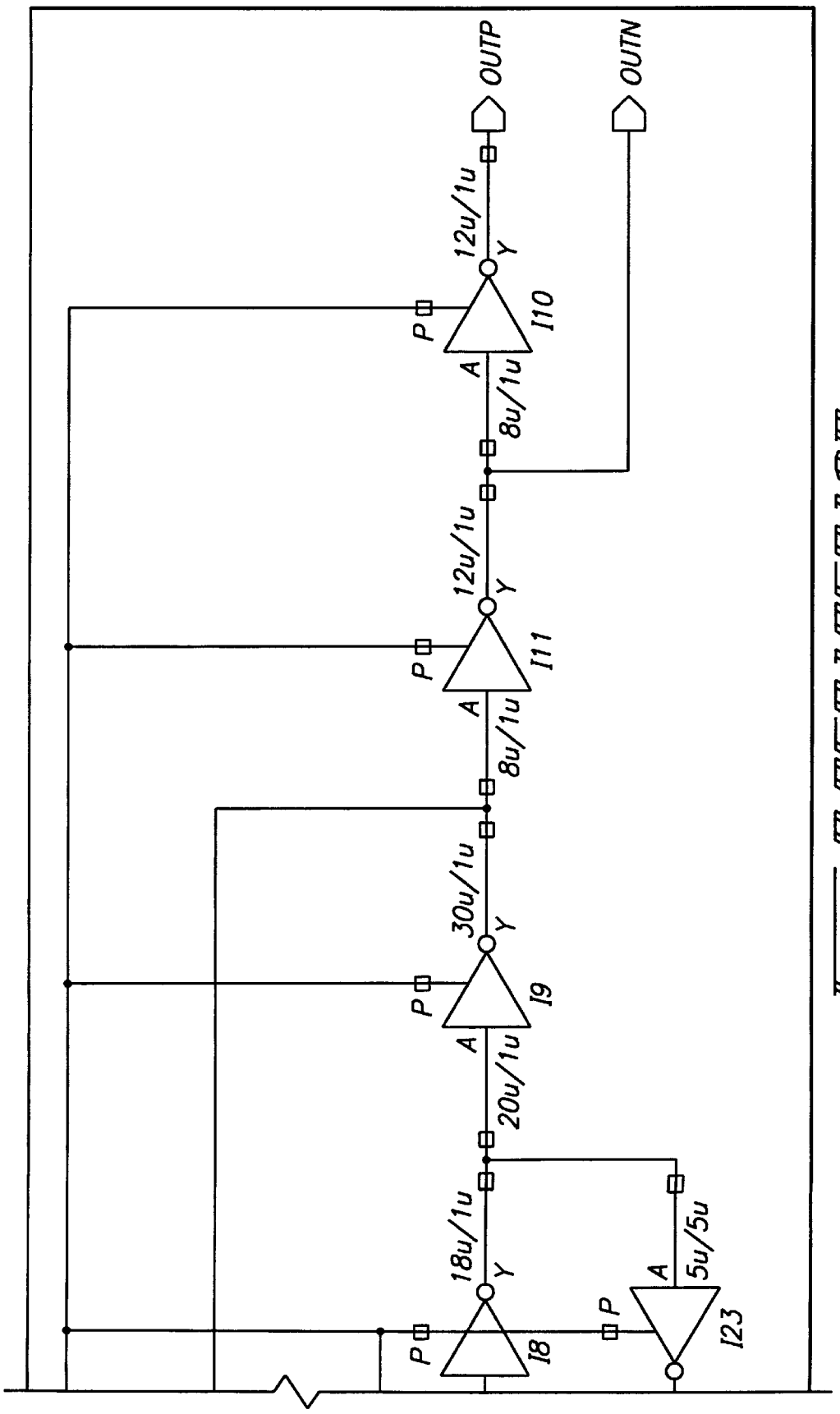
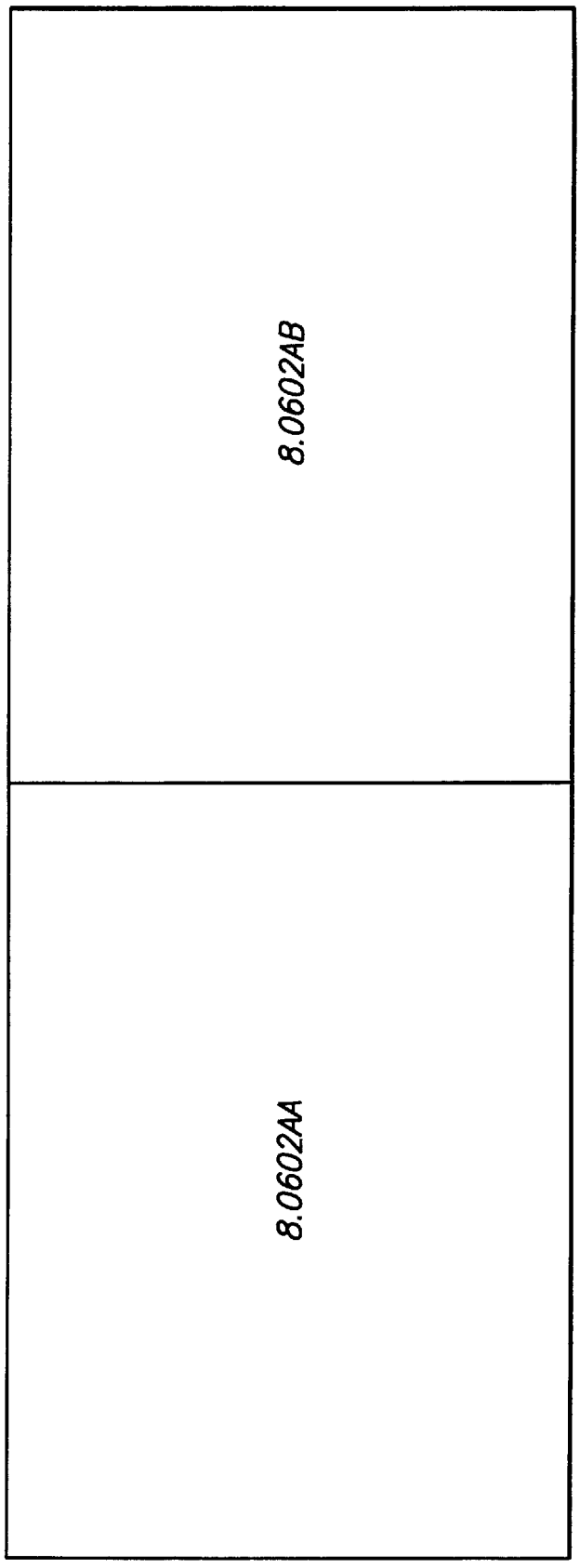

OUTP
OUTN
12u/1u
Y
P
110
A
8u/1u
12u/1u
Y
P
111
A
8u/1u
30u/1u
Y
P
19
A
20u/1u
18u/1u
Y
P
18
A
5u/5u
P
123

FIG 8.0501AB


8.0602AB
8.0602A
FIG 8.0602

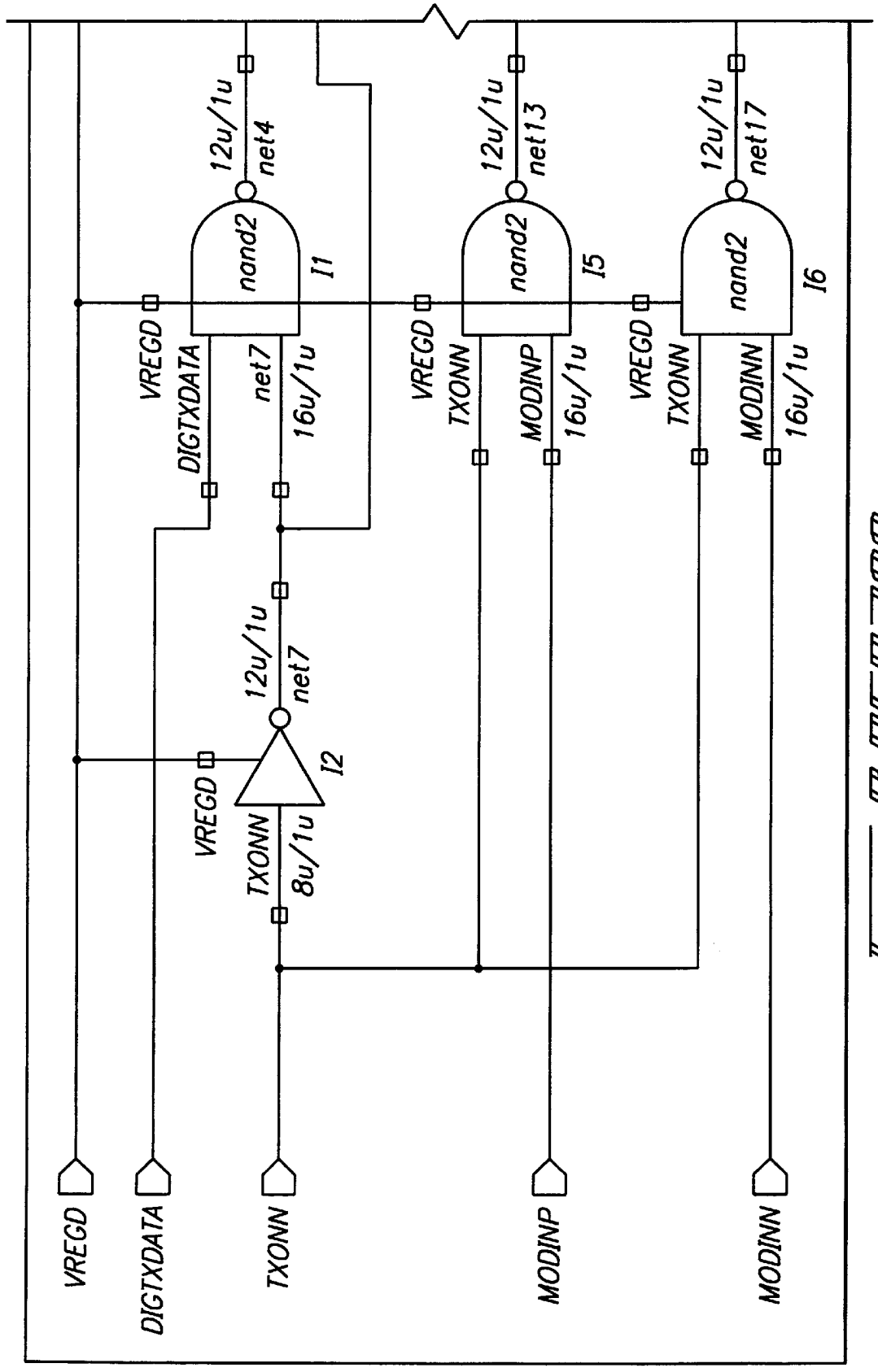

12u/1u
net4
nand2
I1
VREGD
DIGTXDATA
net7
16u/1u
12u/1u
net13
nand2
I5
VREGD
TXONN
MODINP
16u/1u
12u/1u
net17
nand2
I6
VREGD
TXONN
MODINN
16u/1u
12u/1u
net7
I2
VREGD
TXONN
8u/1u
VREGD
DIGTXDATA
TXONN
MODINP
MODINN

FIG 8.0502AA

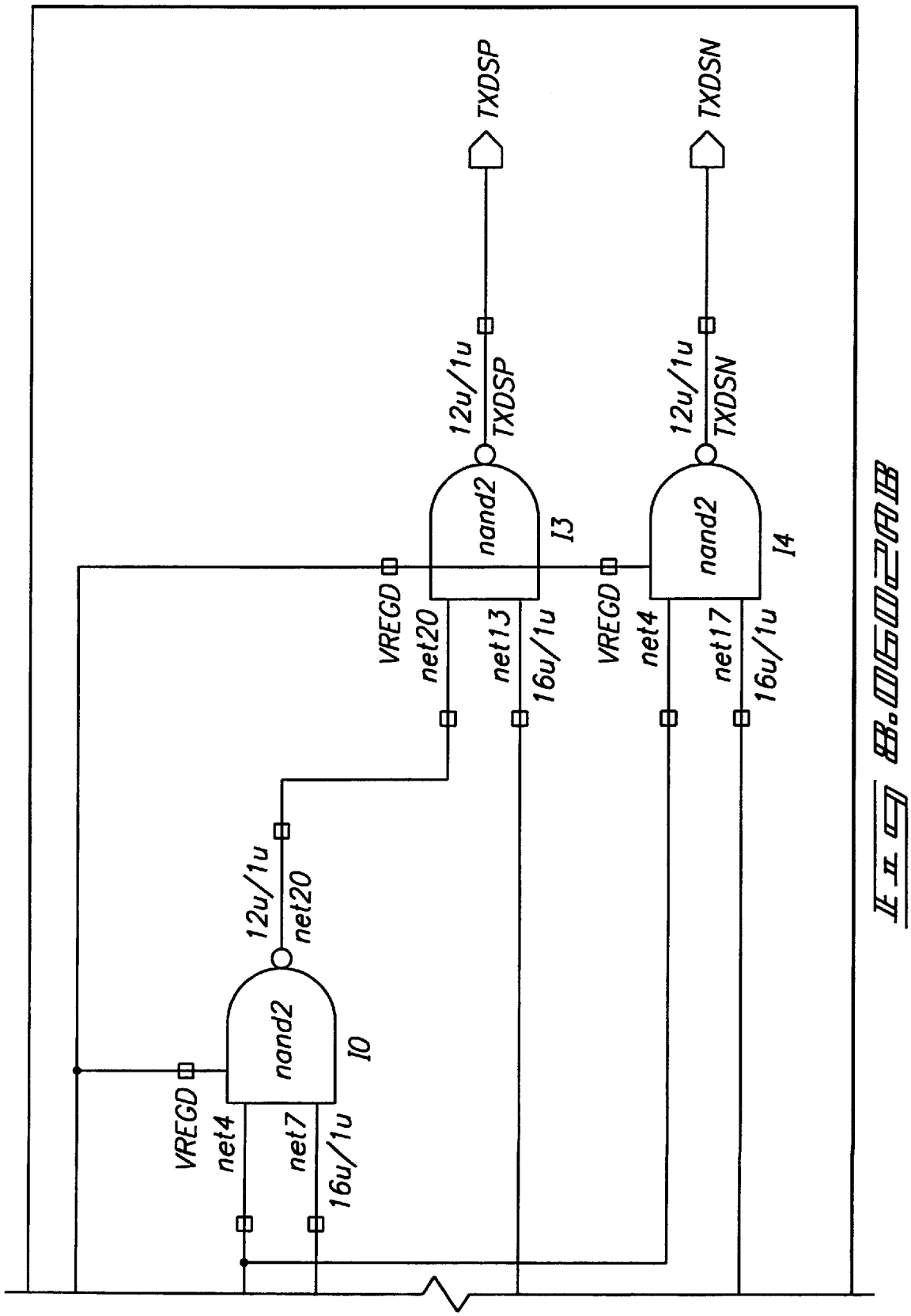
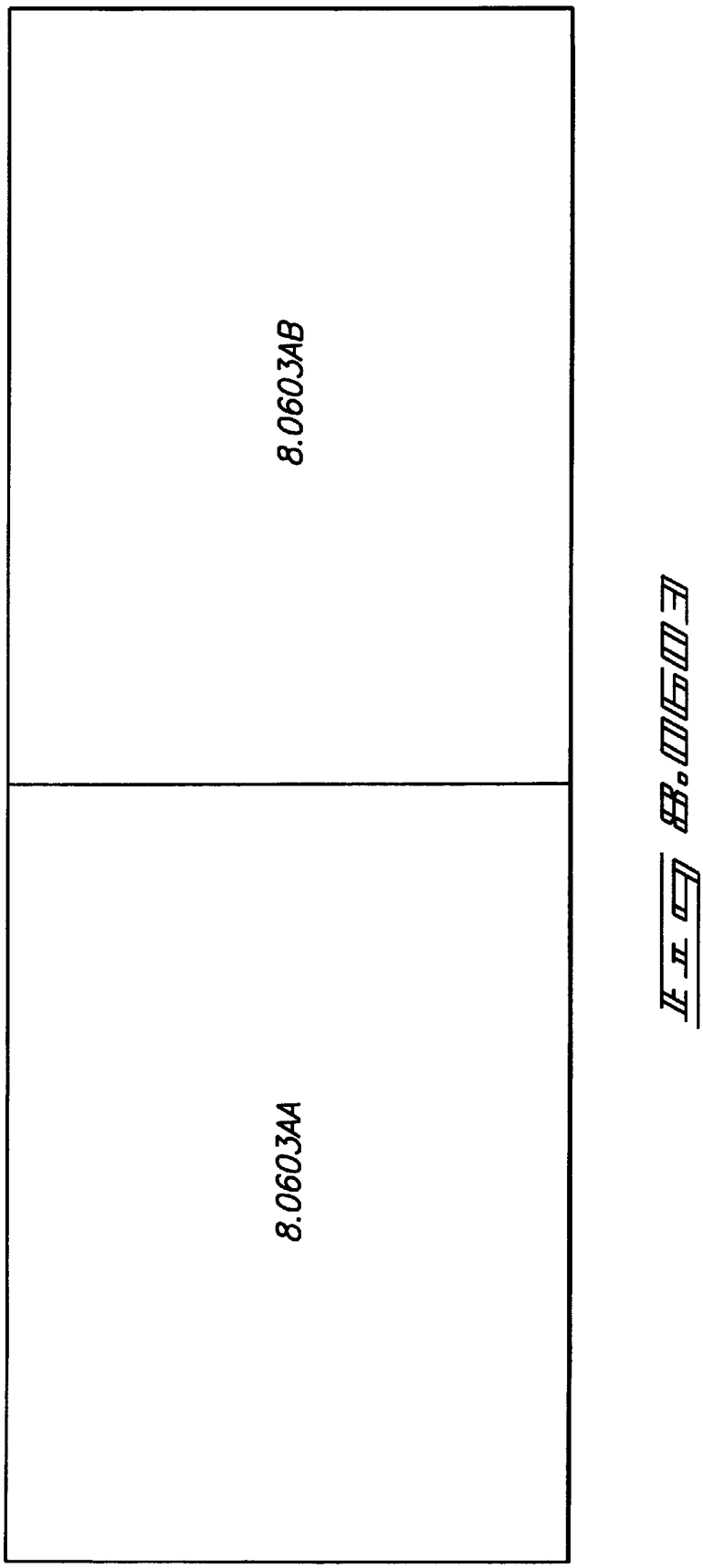


FIG 8.005028B


8.0603AB
8.0603AA
FIG. 8.0603

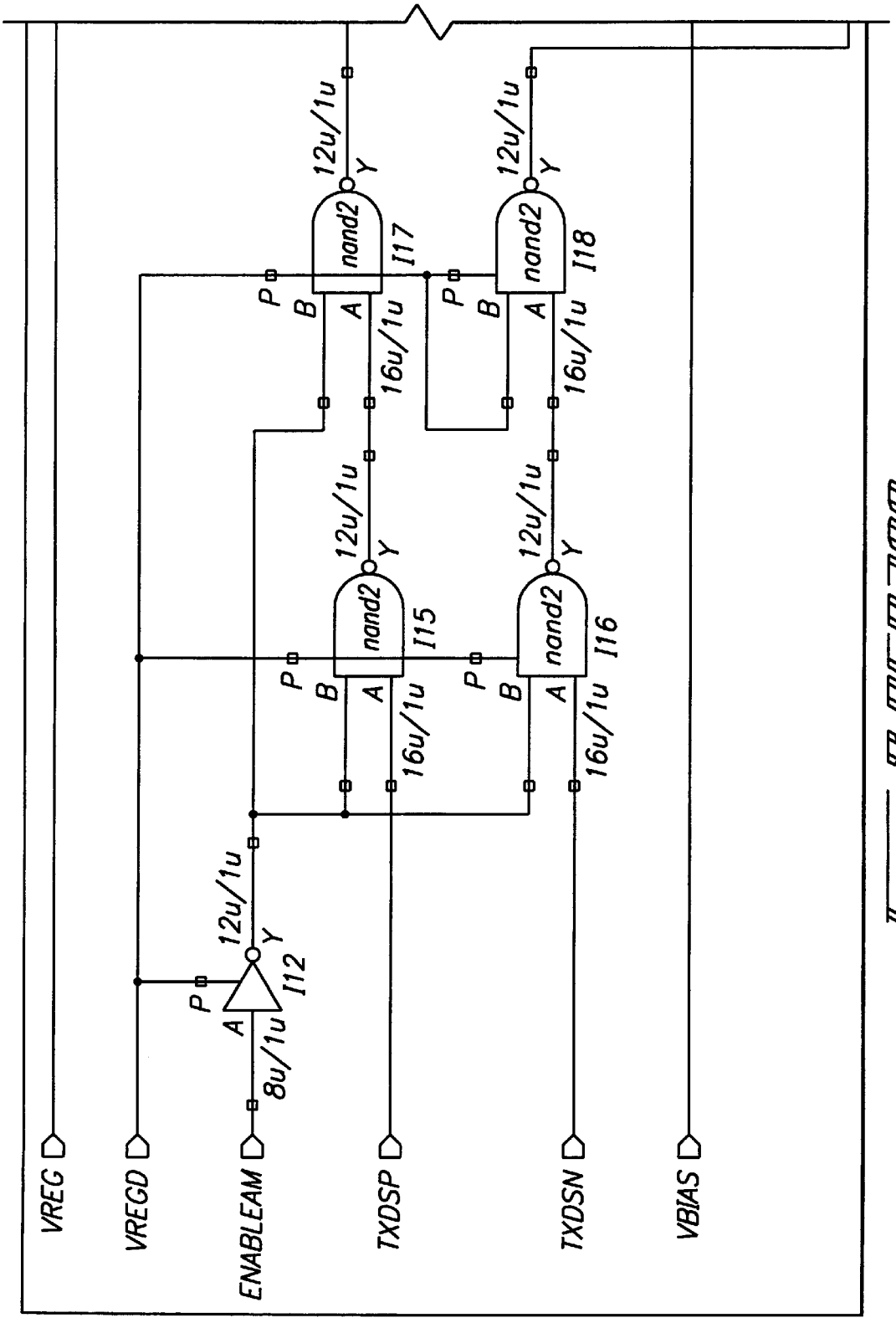

VREG
VREGD
ENABLEAM
TXDSP
TXDSN
VBIAS
I12
I15
I16
I17
I18
nand2
12u/1u
8u/1u
16u/1u
P
A
B
Y

FIG. 88

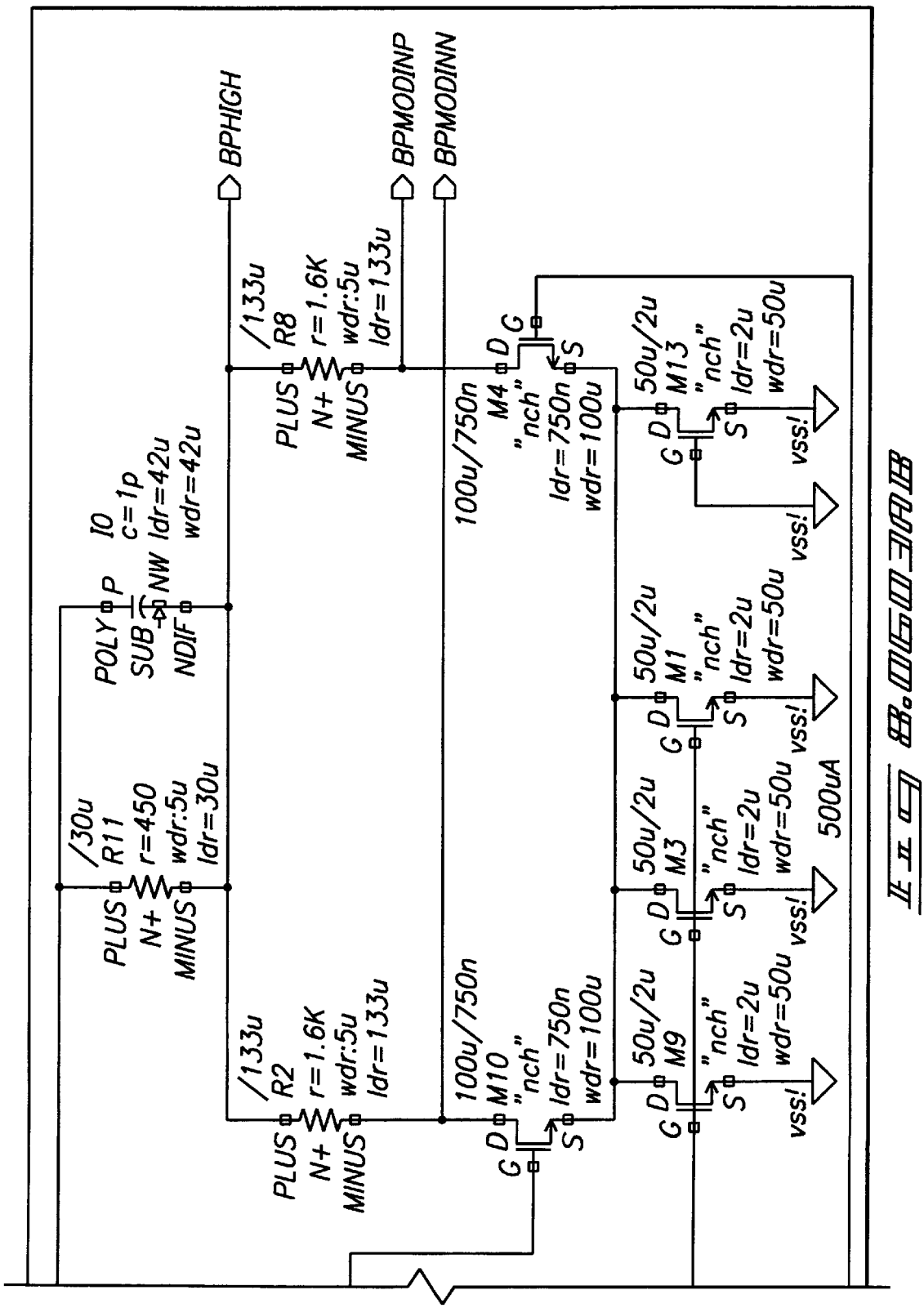
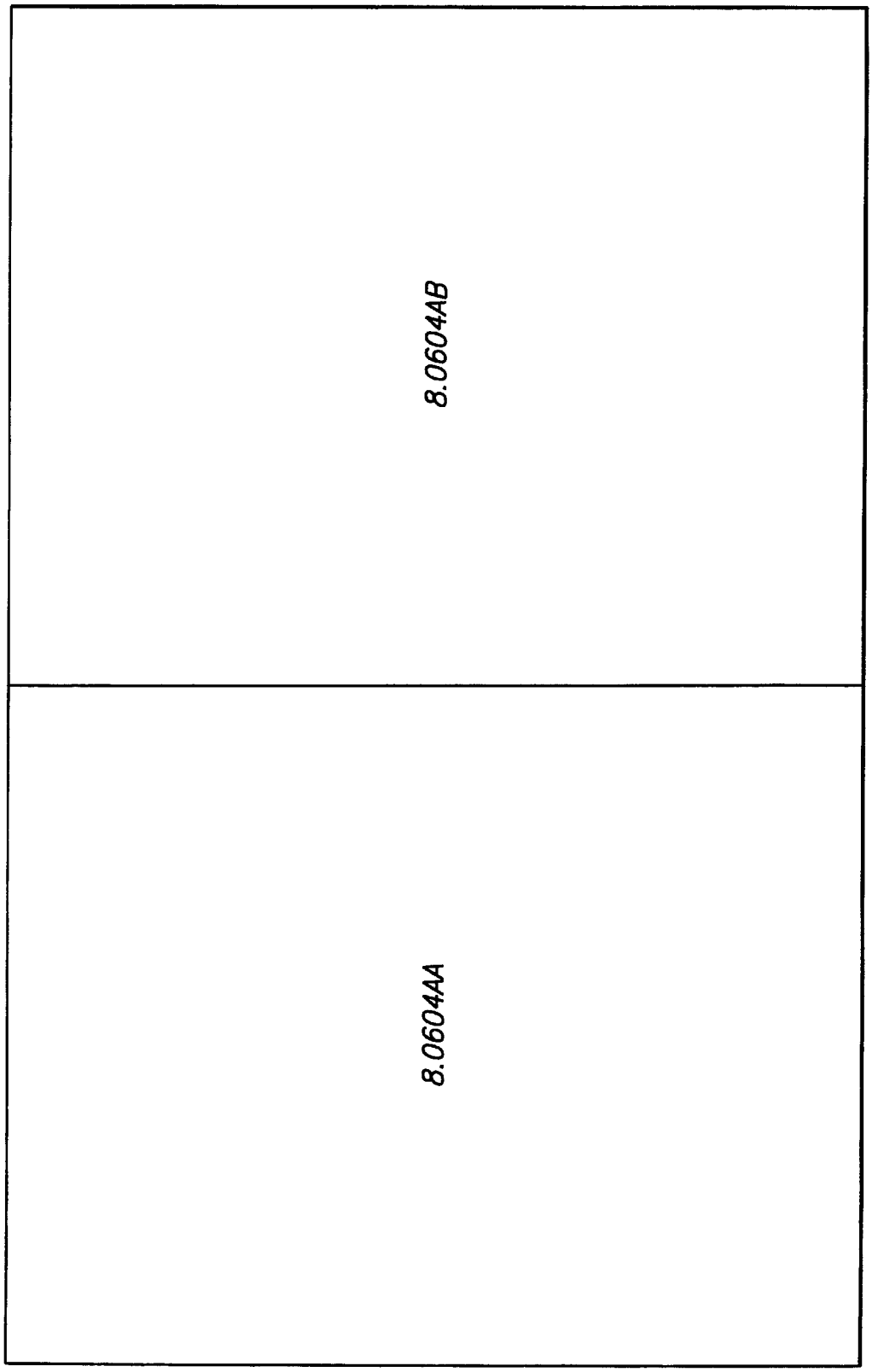

BPHIGH
BPMODINP
BPMODINN
/133u
R8
r=1.6K
wdr:5u
ldr=133u
PLUS
N+
MINUS
100u/750n
M4
"nch"
ldr=750n
wdr=100u
50u/2u
M13
"nch"
ldr=2u
wdr=50u
vss!
I0
c=1p
ldr=42u
wdr=42u
POLY
SUB
NDIF
P
NW
/30u
R11
r=450
wdr:5u
ldr=30u
M1
M3
M9
M10
R2
500uA

FIG. 1130


8.0604AB
8.0604AA
FIG 8,050,4

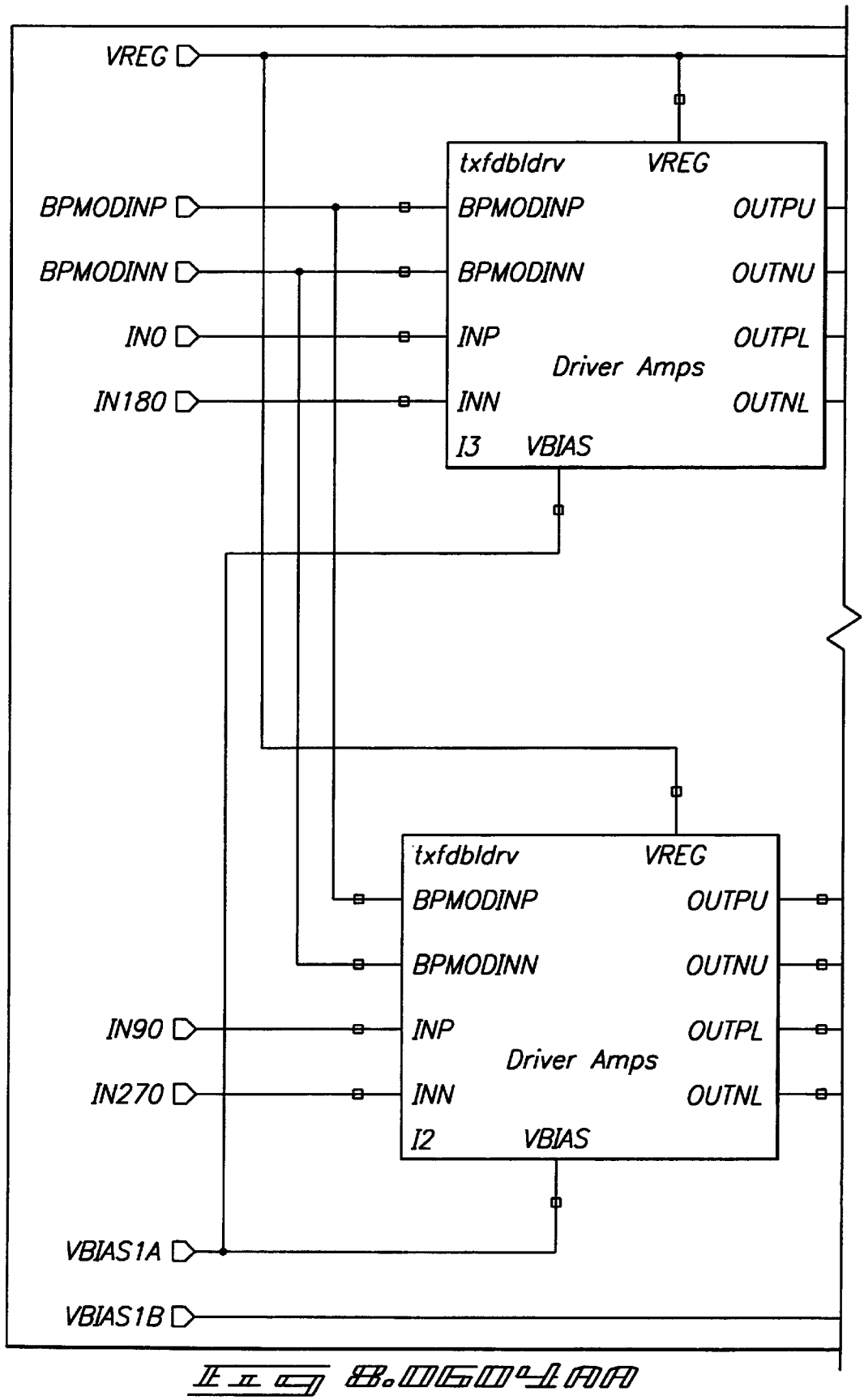

VREG
txfdbldrv
VREG
BPMODINP
BPMODINP
OUTPU
BPMODINN
BPMODINN
OUTNU
IN0
INP
OUTPL
Driver Amps
IN180
INN
OUTNL
I3
VBIAS
txfdbldrv
VREG
BPMODINP
OUTPU
BPMODINN
OUTNU
IN90
INP
OUTPL
Driver Amps
IN270
INN
OUTNL
I2
VBIAS
VBIAS1A
VBIAS1B

Fig 8.0606AA

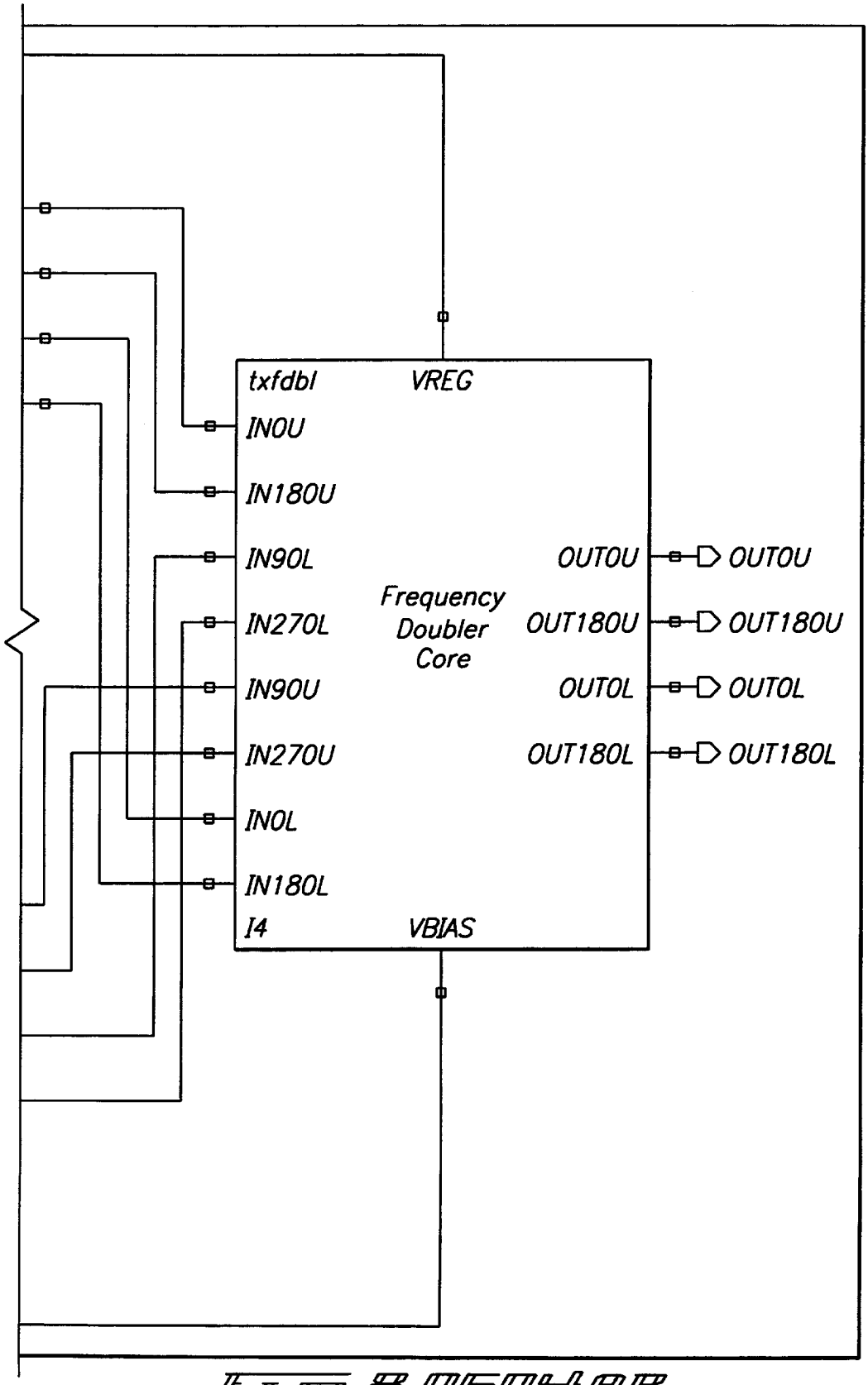
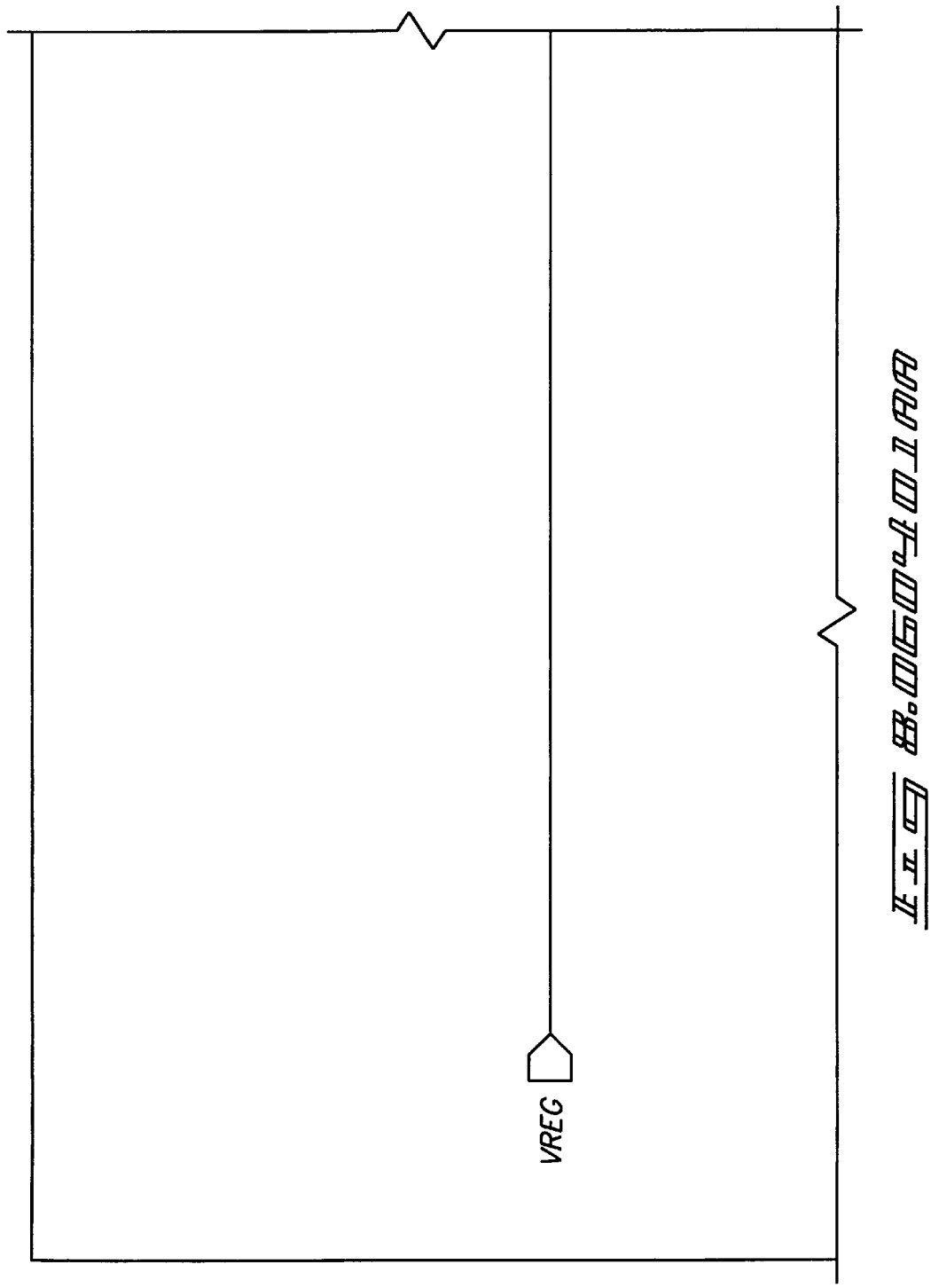

txfdbl
VREG
IN0U
IN180U
IN90L
IN270L
IN90U
IN270U
IN0L
IN180L
I4
VBIAS
Frequency Doubler Core
OUT0U
OUT180U
OUT0L
OUT180L
OUT0U
OUT180U
OUT0L
OUT180L

Fig 8.0604AB

8.060401AA	8.060401AB	8.060401AC	8.060401AD	8.060401AE
8.060401BA	8.060401BB	8.060401BC	8.060401BD	8.060401BE
8.060401CA	8.060401CB	8.060401CC	8.060401CD	8.060401CE
8.060401DA	8.060401DB	8.060401DC	8.060401DD	8.060401DE
8.060401EA	8.060401EB	8.060401EC	8.060401ED	8.060401EE
8.060401FA	8.060401FB	8.060401FC	8.060401FD	8.060401FE

Fig 8.060401


VREG
FIG. 88,059A

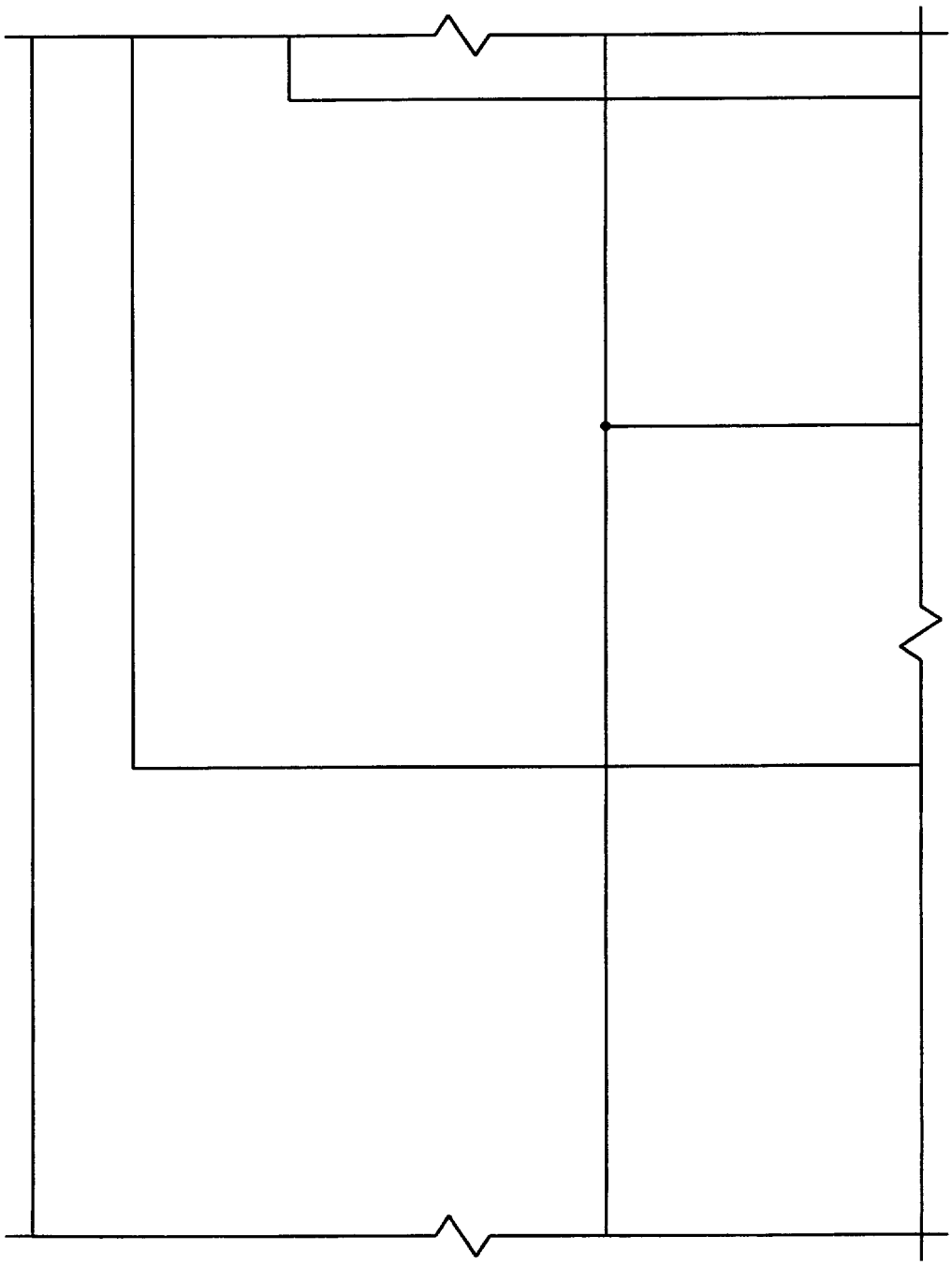


FIG. 8,050,000

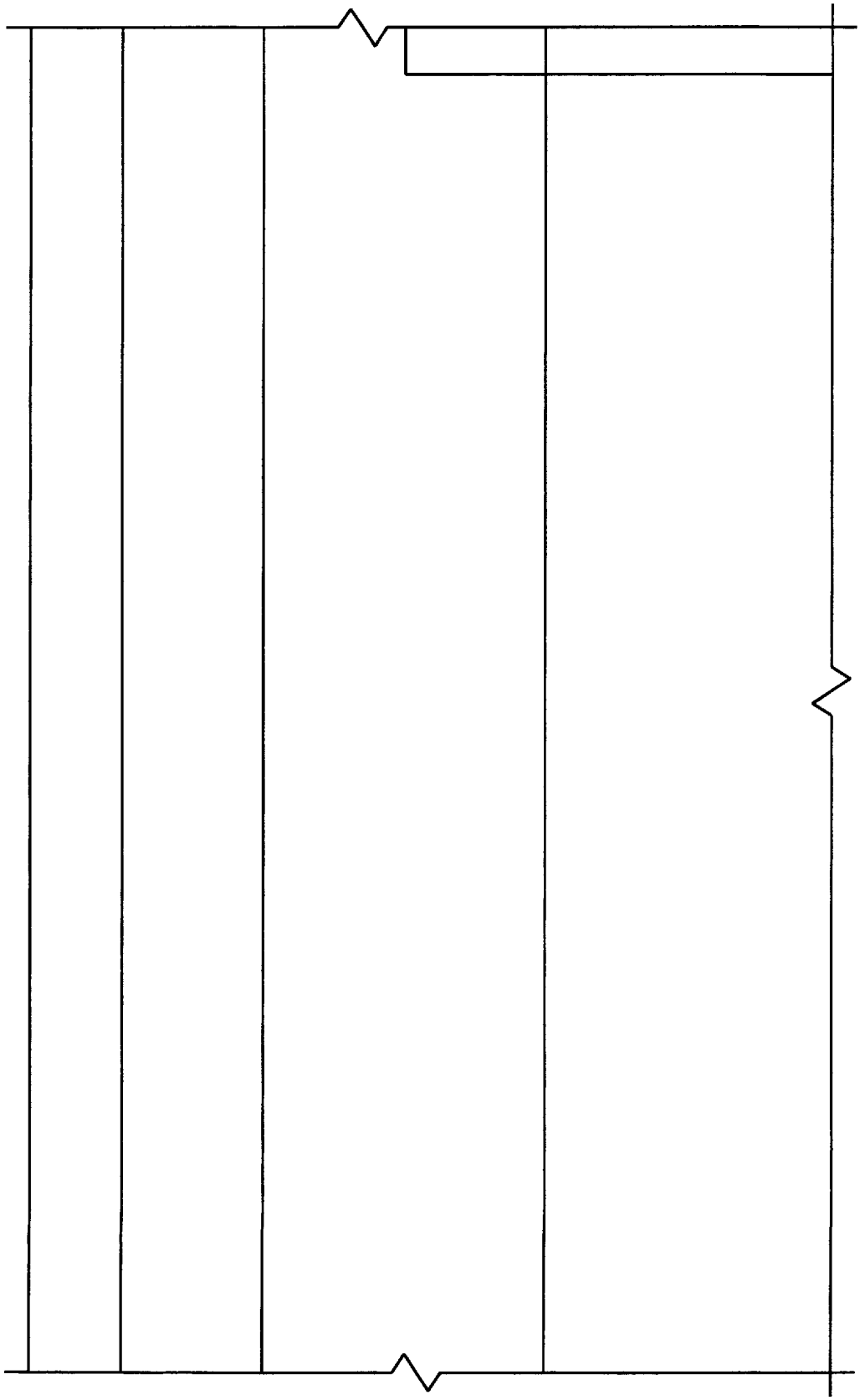


FIG 88,065,401 AC

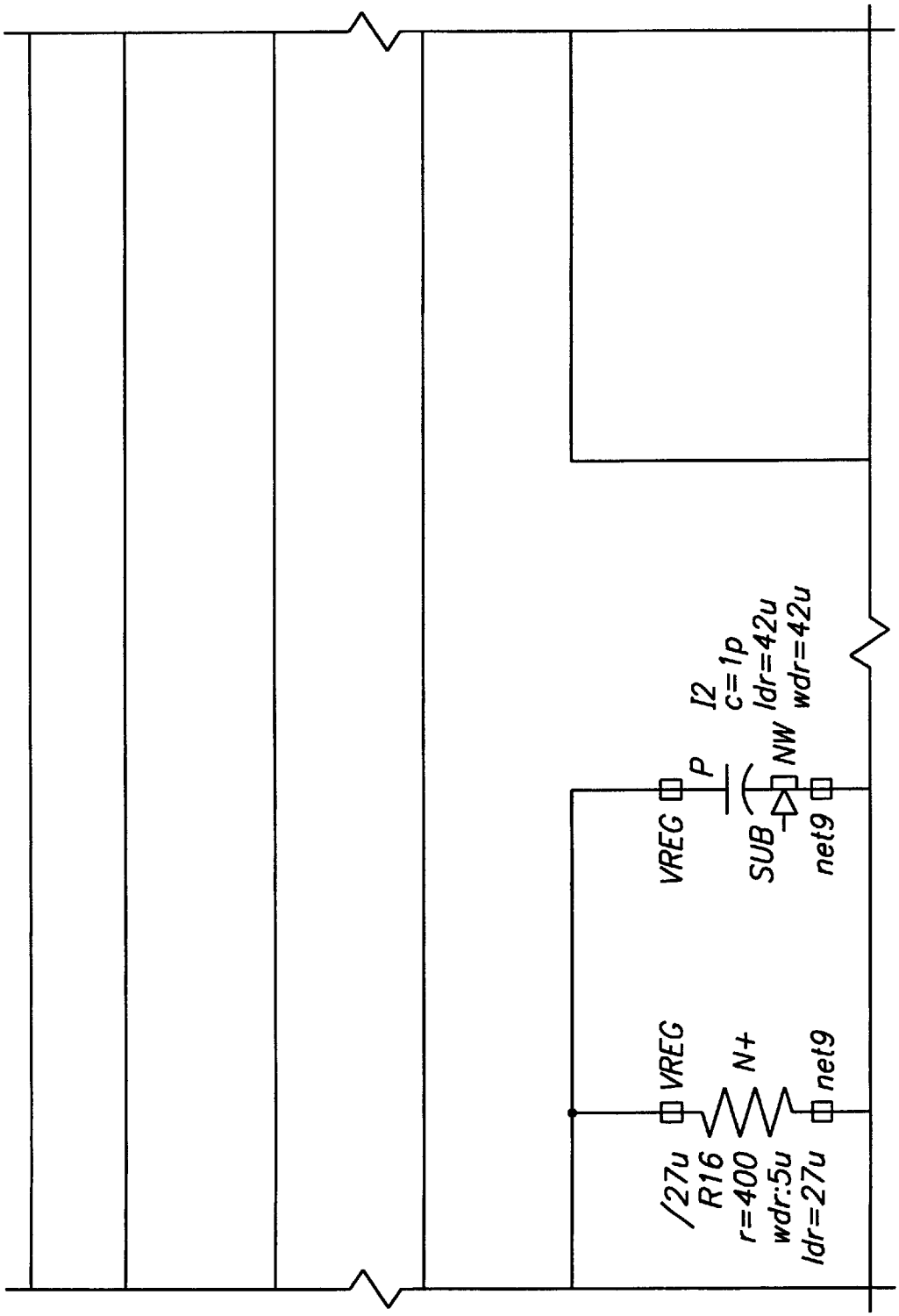
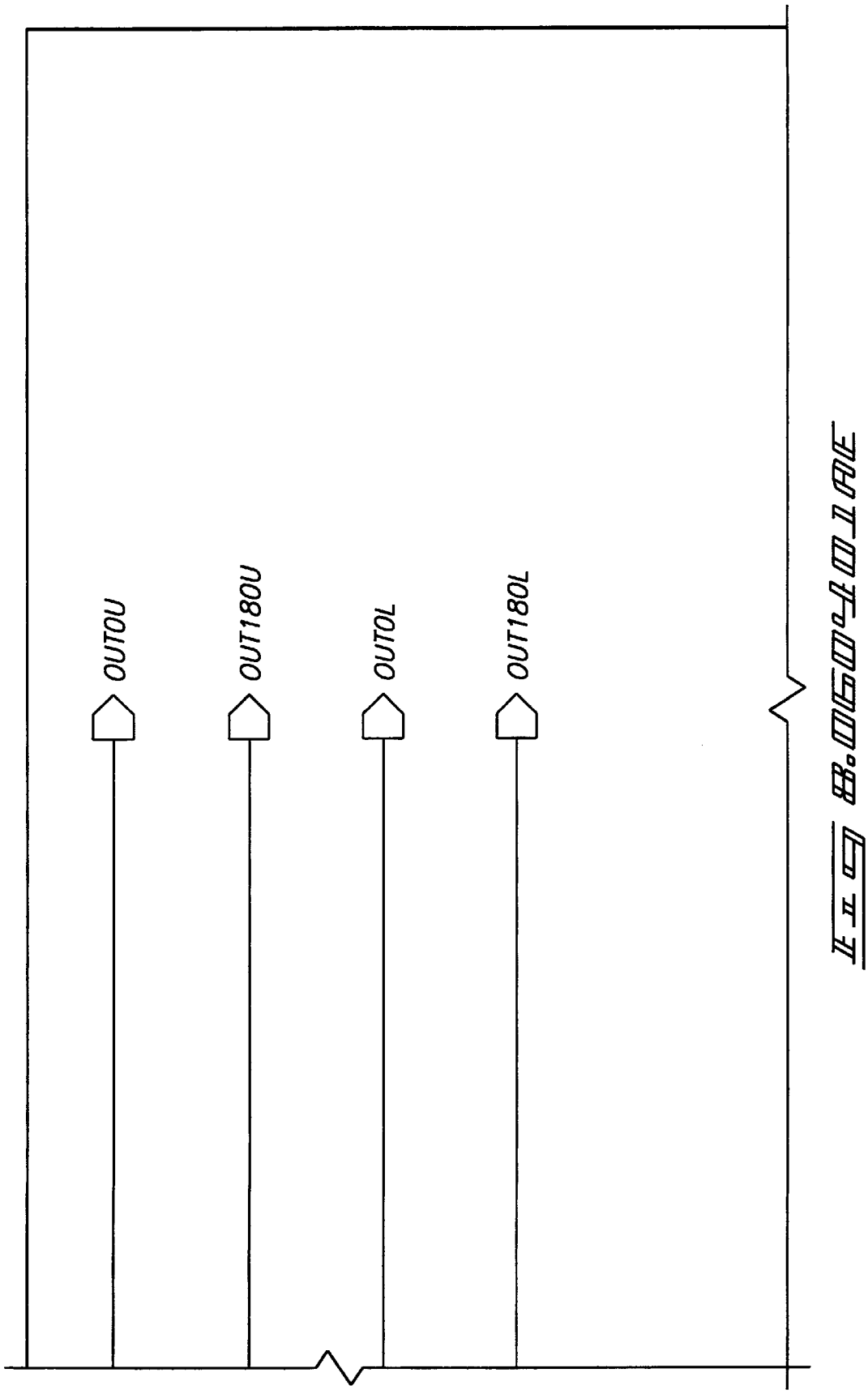


FIG. 88,005,701 A1


OUT0U
OUT180U
OUT0L
OUT180L
FIG 88.0500 ATTACHMENT

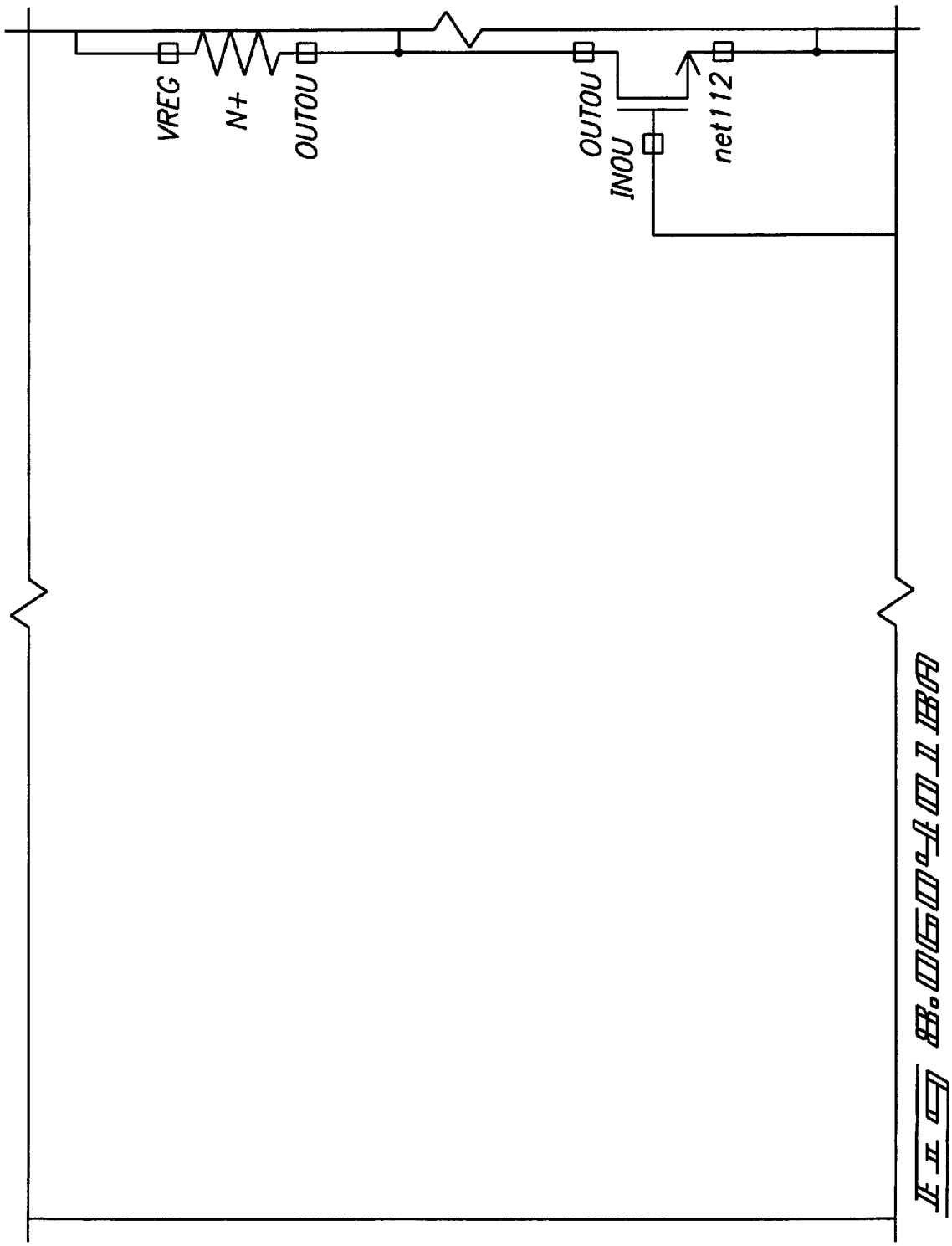


FIG. 1940

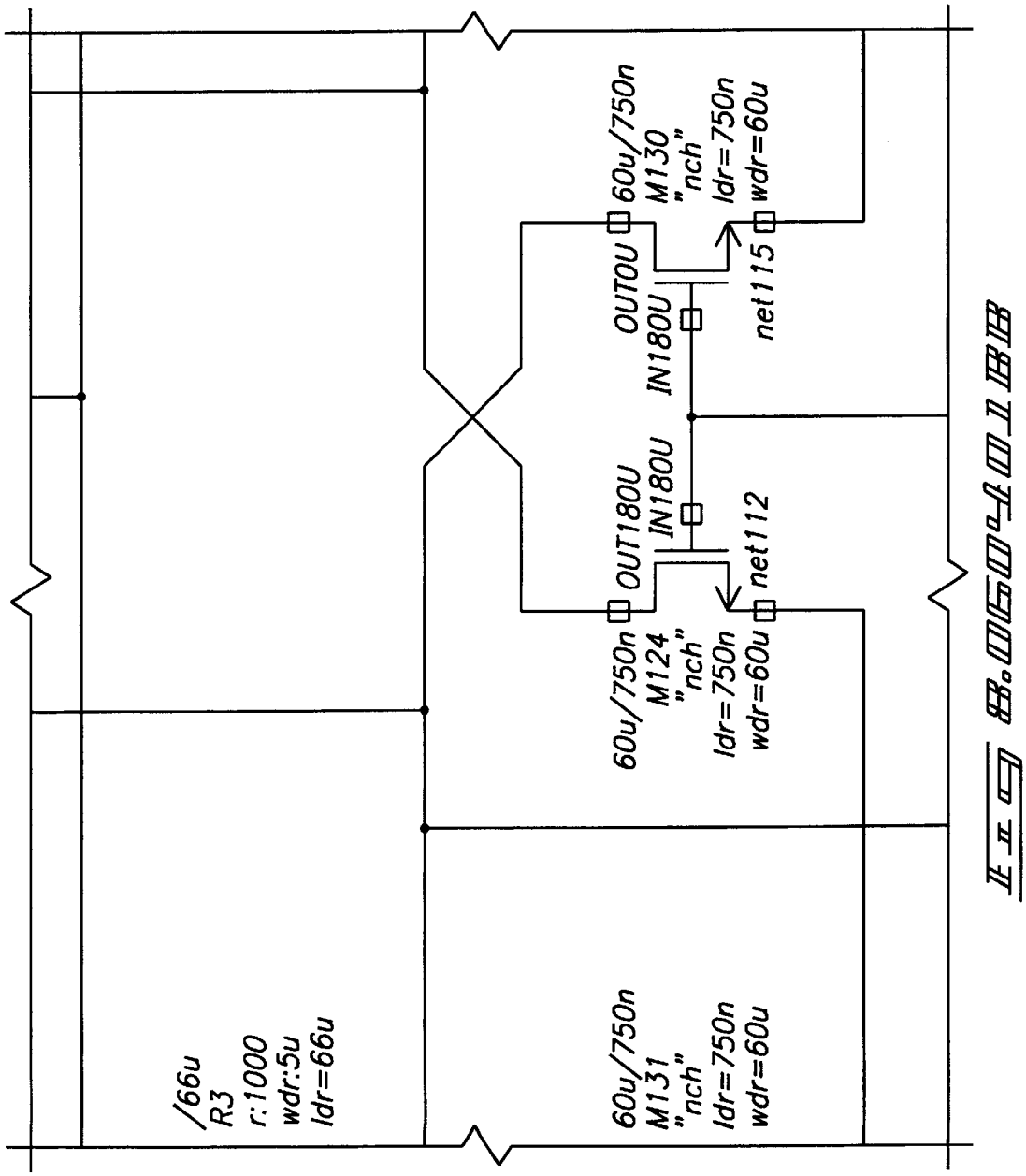

/66u
R3
r:1000
wdr:5u
ldr=66u
60u/750n
M131
"nch"
ldr=750n
wdr=60u
60u/750n
M124
"nch"
ldr=750n
wdr=60u
OUT180U
IN180U
net112
OUT0U
IN180U
net115
60u/750n
M130
"nch"
ldr=750n
wdr=60u

FIG. 8,005,011

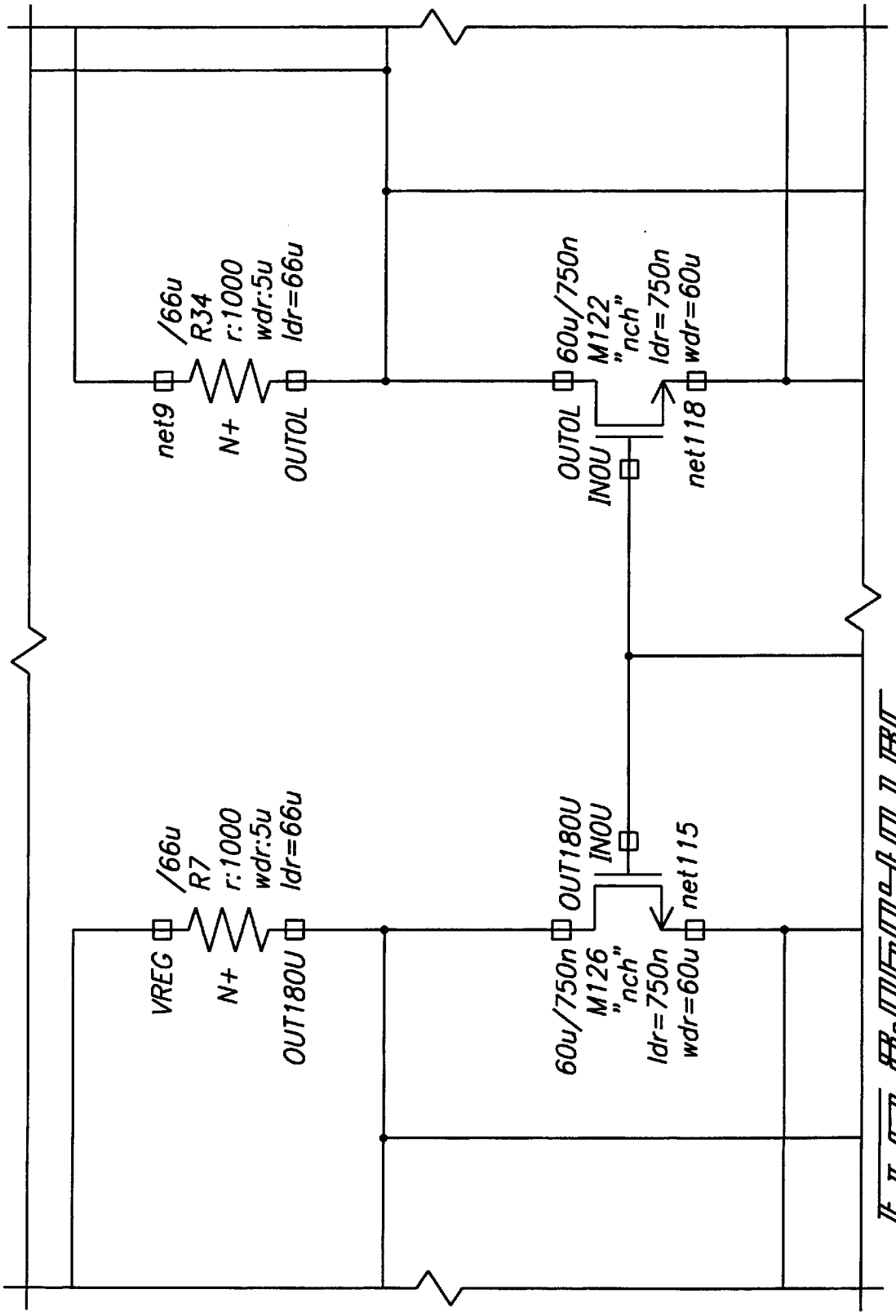
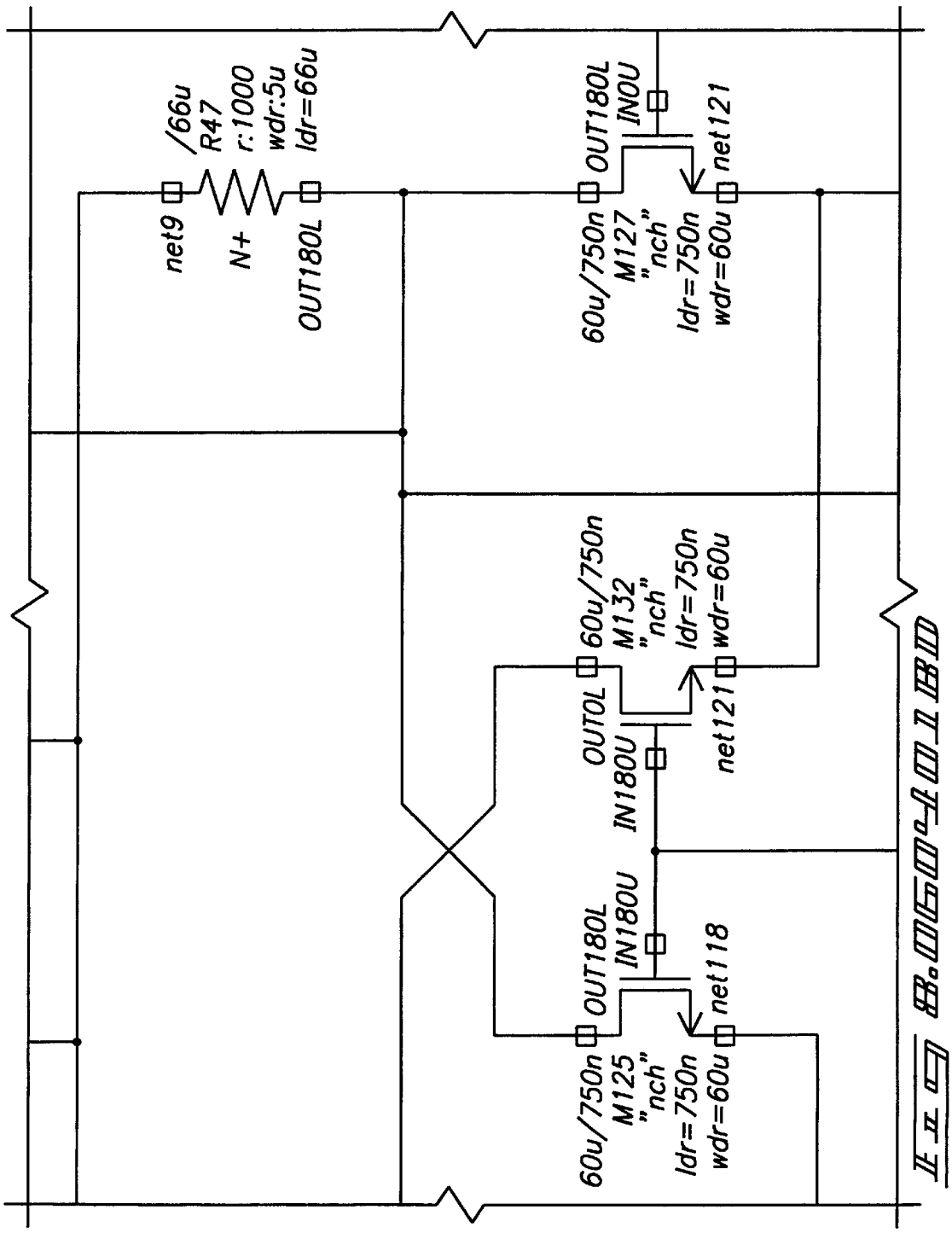

/66u
R34
r:1000
wdr:5u
ldr=66u
net9
N+
OUT0L
60u/750n
M122
"nch"
ldr=750n
wdr=60u
OUT0L
IN0U
net118
/66u
R7
r:1000
wdr:5u
ldr=66u
VREG
N+
OUT180U
OUT180U
IN0U
net115
60u/750n
M126
"nch"
ldr=750n
wdr=60u

Fig 6,006,011


/66u
R47
r:1000
wdr:5u
ldr=66u
net9
N+
OUT180L
OUT180L
IN0U
net121
60u/750n
M127
"nch"
ldr=750n
wdr=60u
60u/750n
M132
"nch"
ldr=750n
wdr=60u
OUT0L
IN180U
net121
OUT180L
IN180U
net118
60u/750n
M125
"nch"
ldr=750n
wdr=60u

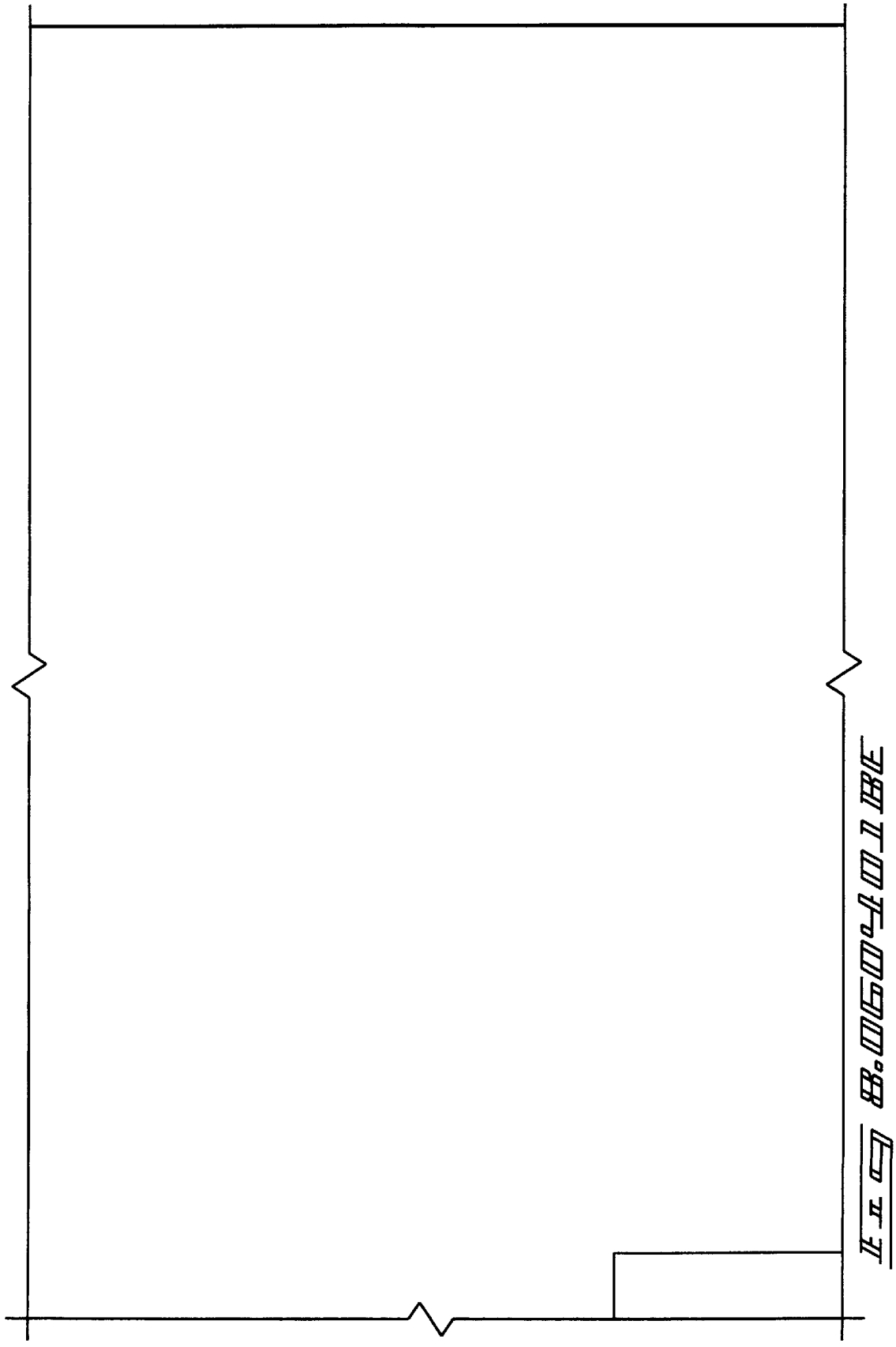


FIG. 88,005

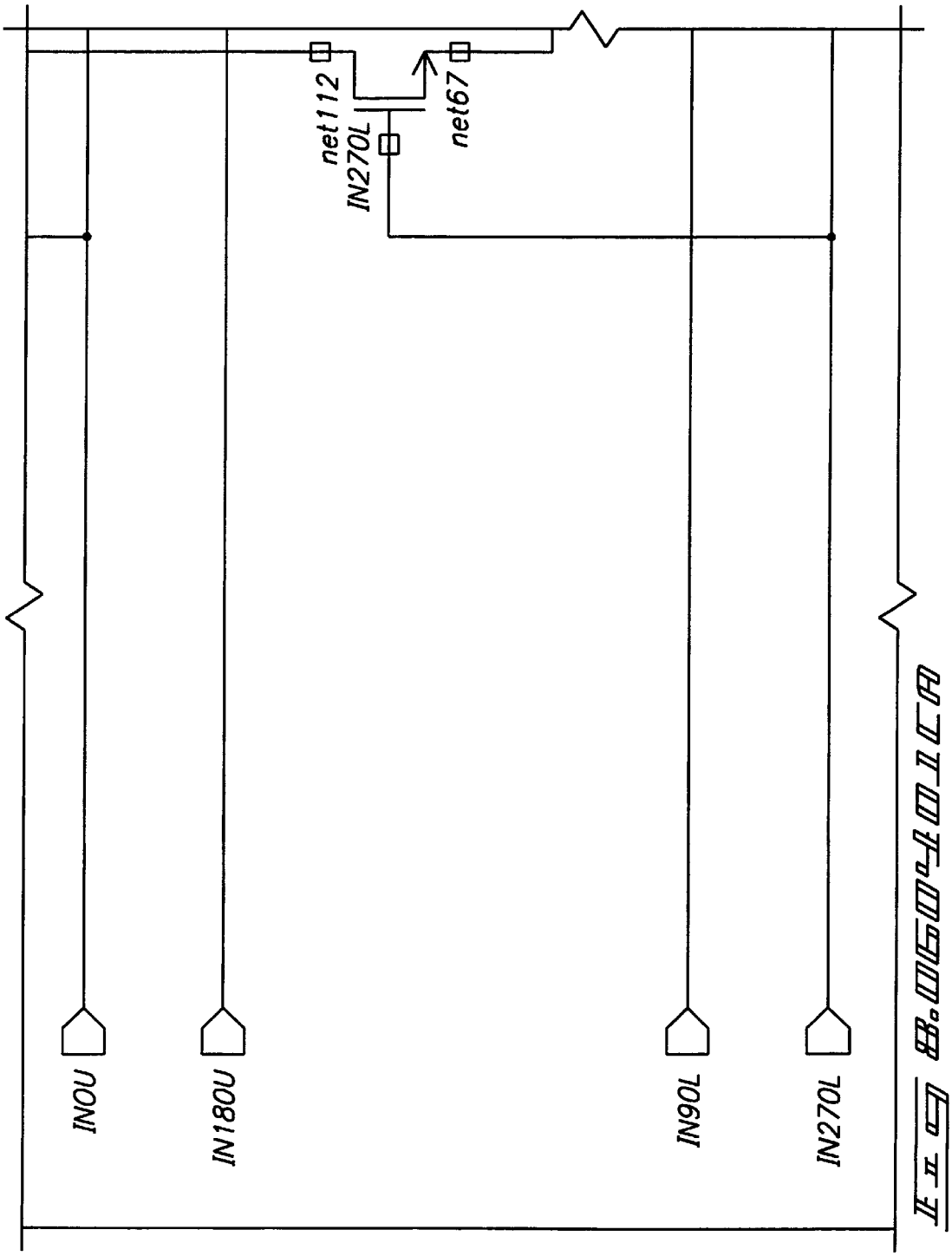


FIG 88,050

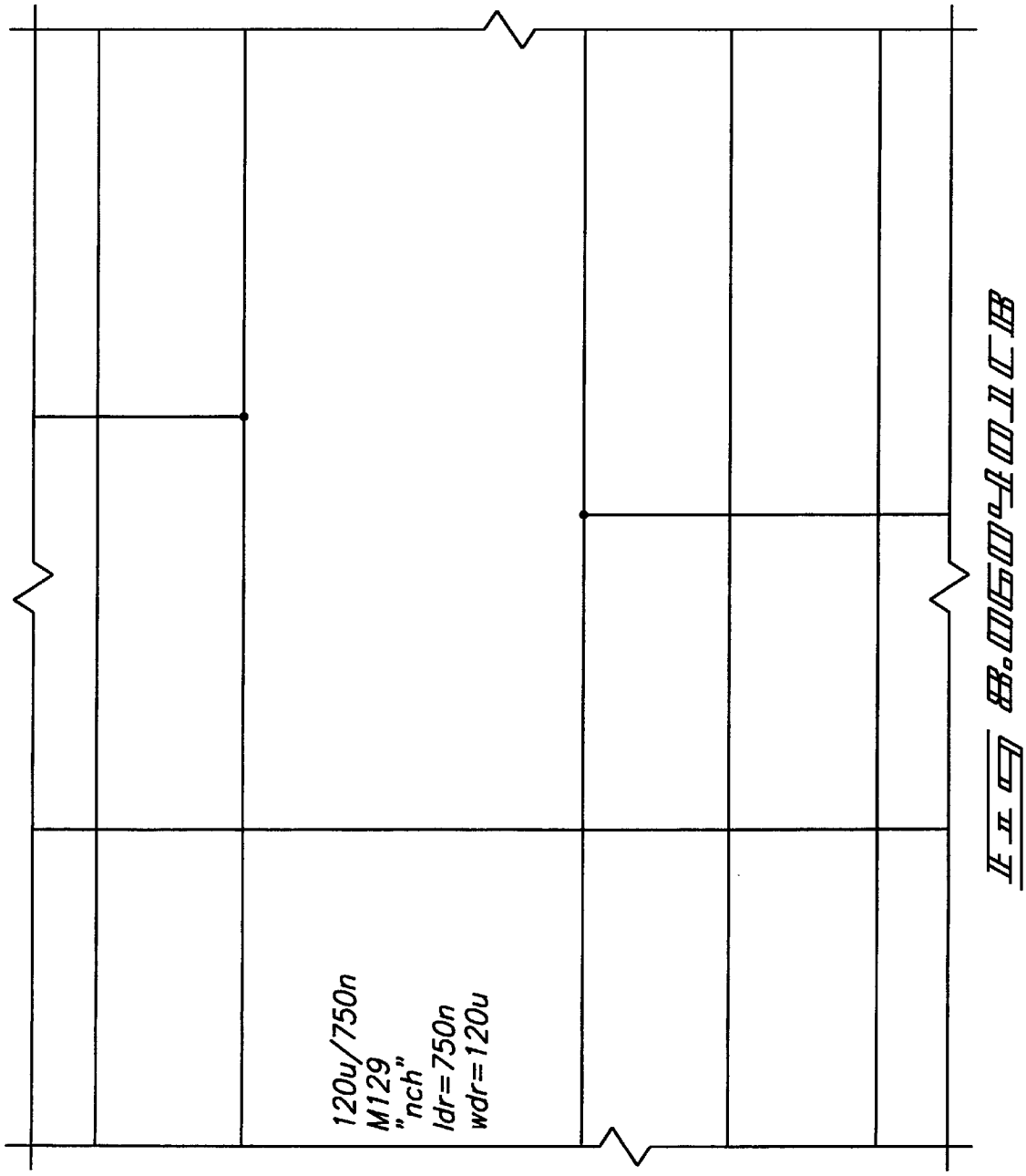


FIG 8,050,008

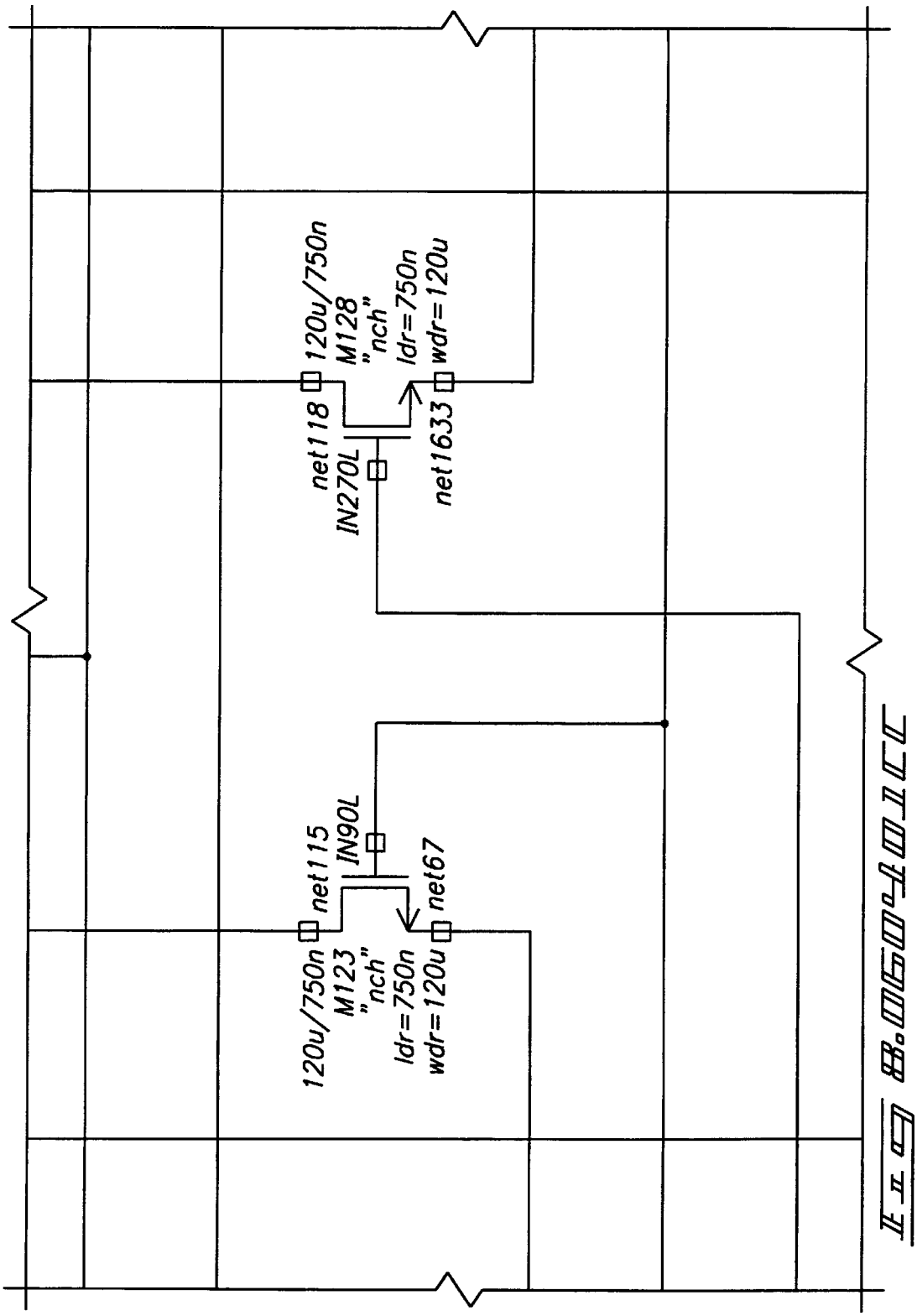
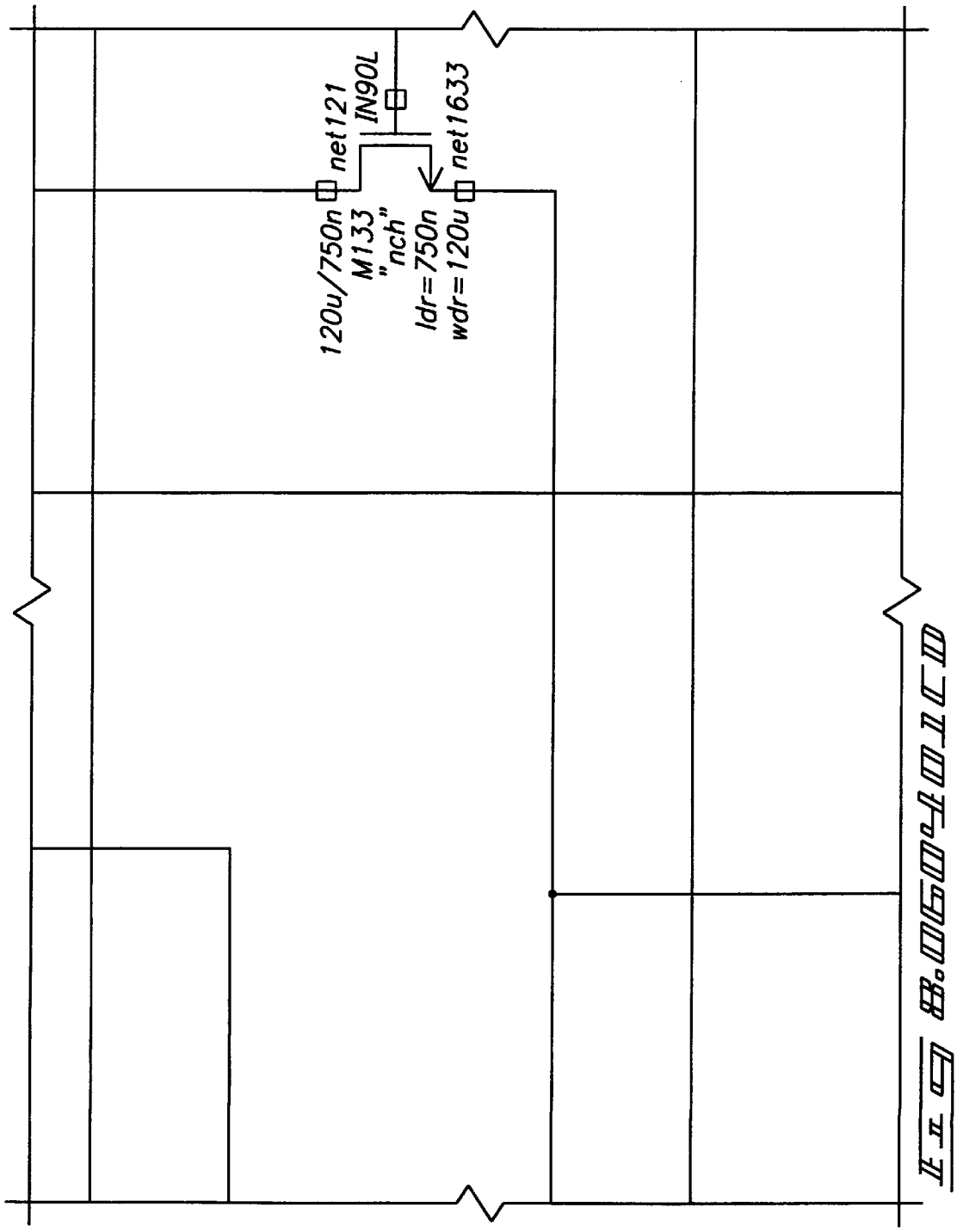


FIG 88,059,408


net121
IN90L
net1633
120u/750n
M133
"nch"
ldr=750n
wdr=120u
FIG. 88,059

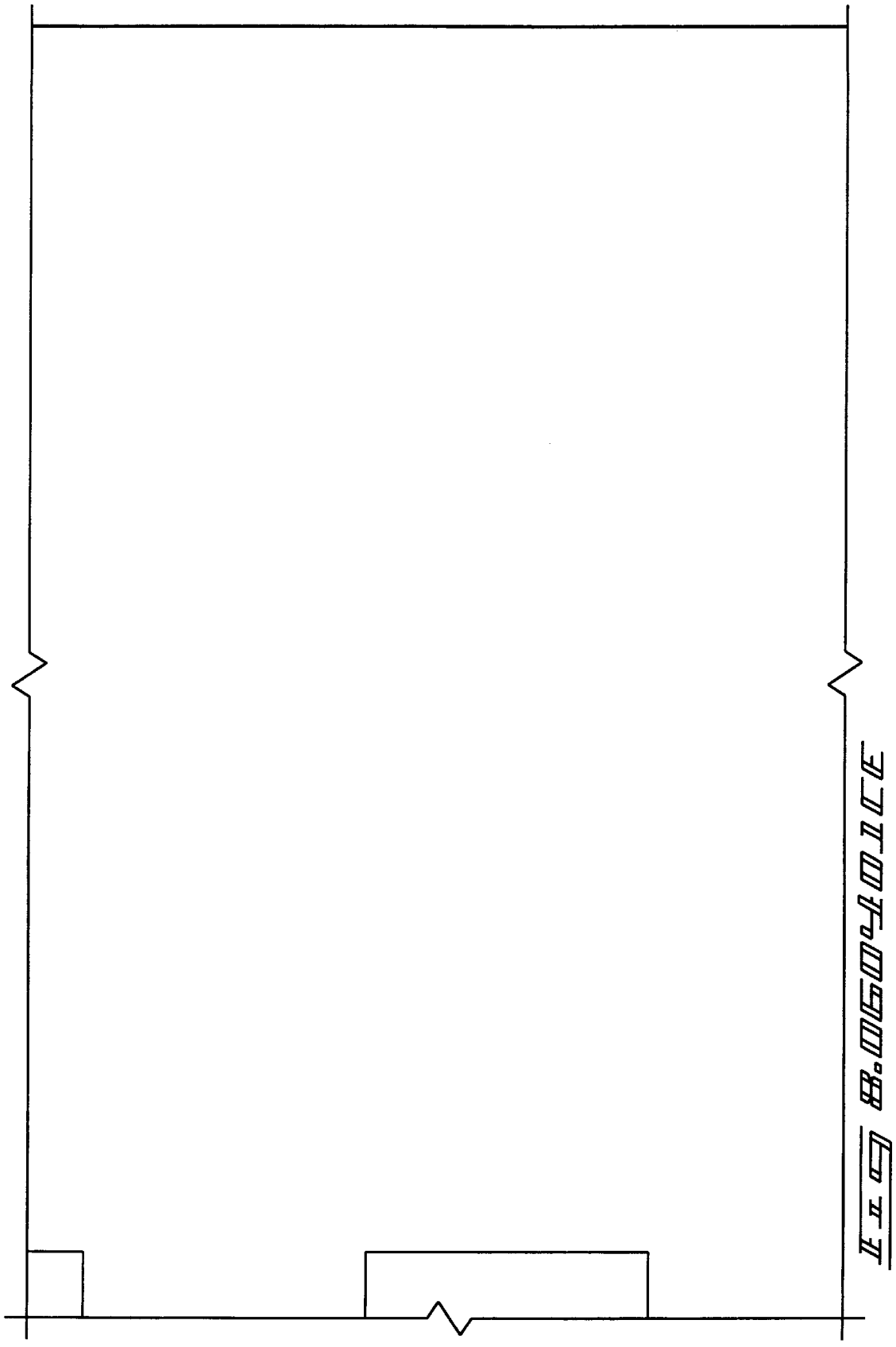


FIG 98,050,478

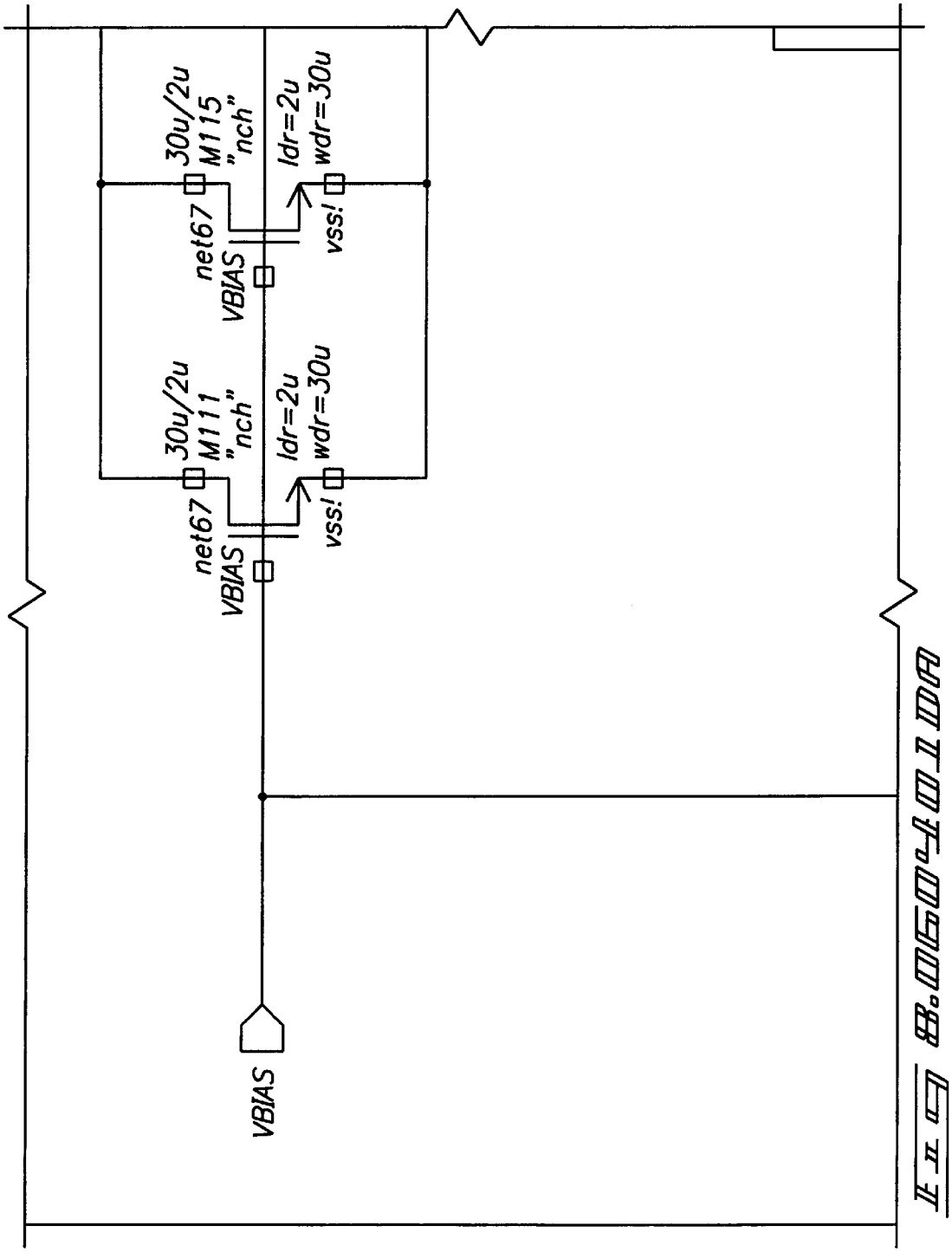


FIG 48,059,004

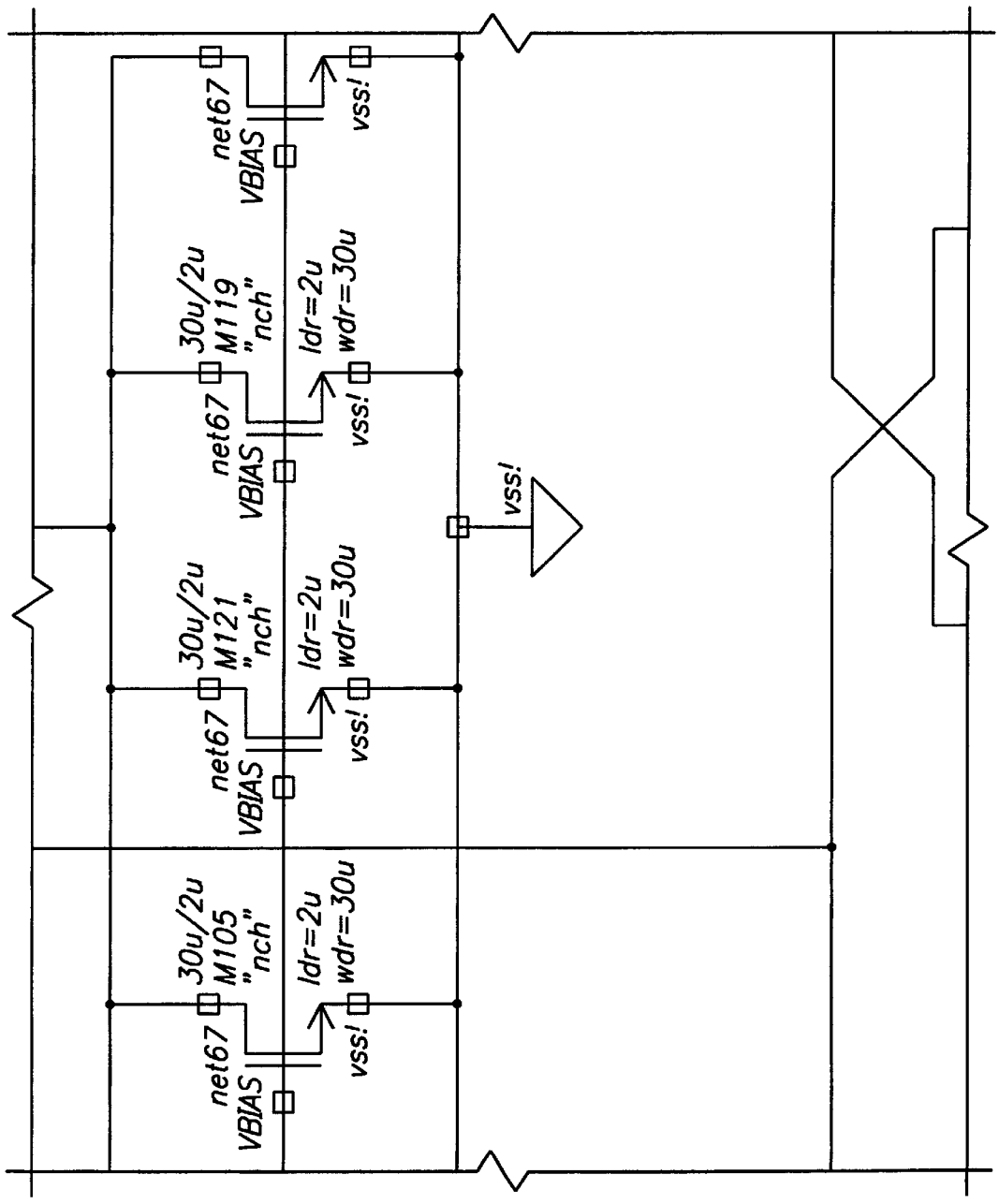

net67
VBIAS
vss!
30u/2u
M119
"nch"
ldr=2u
wdr=30u
vss!
net67
VBIAS
vss!
30u/2u
M121
"nch"
ldr=2u
wdr=30u
vss!
net67
VBIAS
vss!
30u/2u
M105
"nch"
ldr=2u
wdr=30u
vss!
net67
VBIAS

FIG. 1188

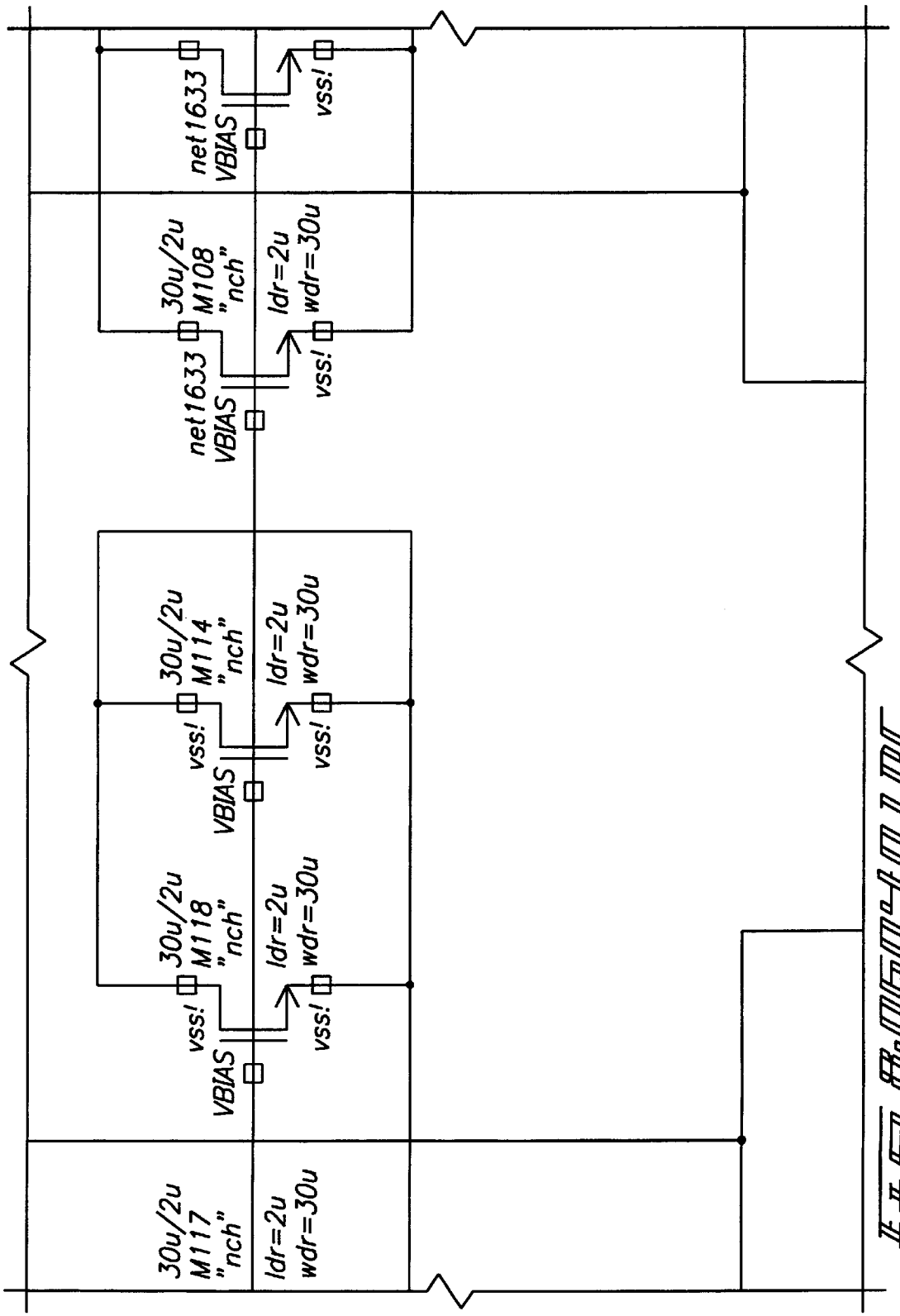
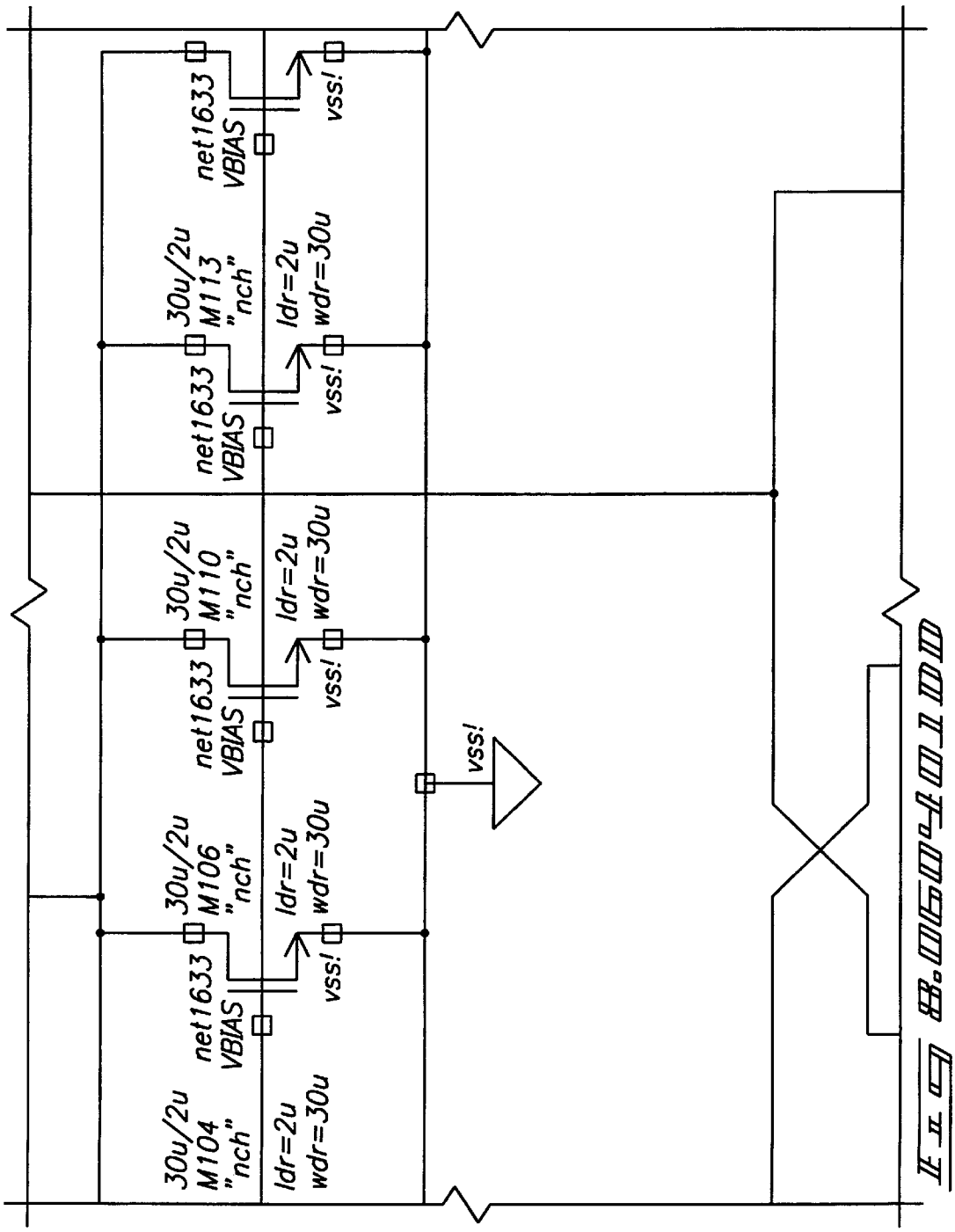

30u/2u
M117
"nch"
ldr=2u
wdr=30u
30u/2u
M118
"nch"
ldr=2u
wdr=30u
VBIAS
vss!
30u/2u
M114
"nch"
ldr=2u
wdr=30u
VBIAS
vss!
30u/2u
M108
"nch"
ldr=2u
wdr=30u
VBIAS
net1633
vss!

FIG. 88.0059


30u/2u
M104
"nch"
ldr=2u
wdr=30u
net1633
VBIAS
30u/2u
M106
"nch"
ldr=2u
wdr=30u
vss!
net1633
VBIAS
30u/2u
M110
"nch"
ldr=2u
wdr=30u
vss!
net1633
VBIAS
30u/2u
M113
"nch"
ldr=2u
wdr=30u
vss!
net1633
VBIAS
vss!

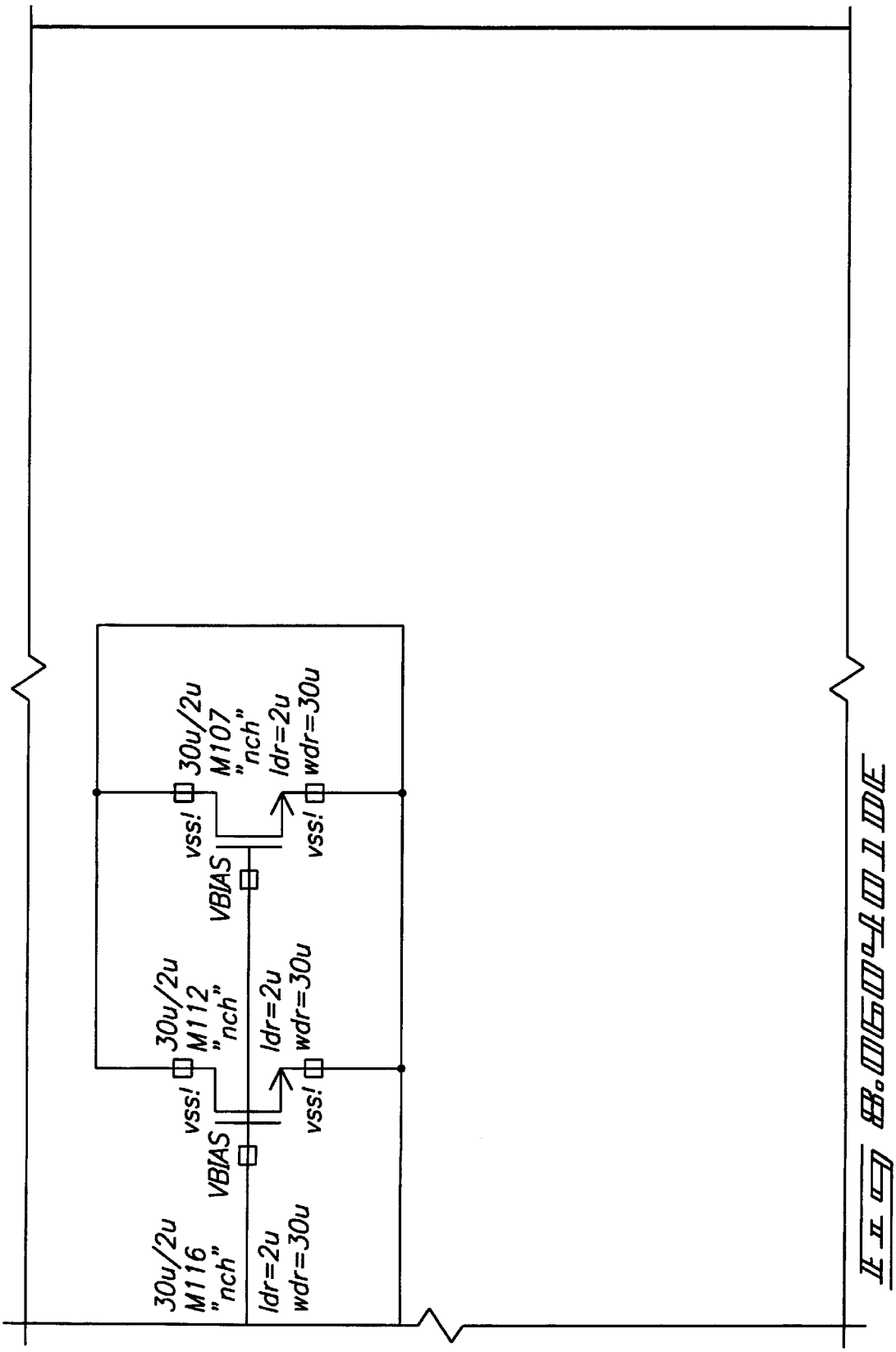


FIG 48.0504 DE 11 00 4F

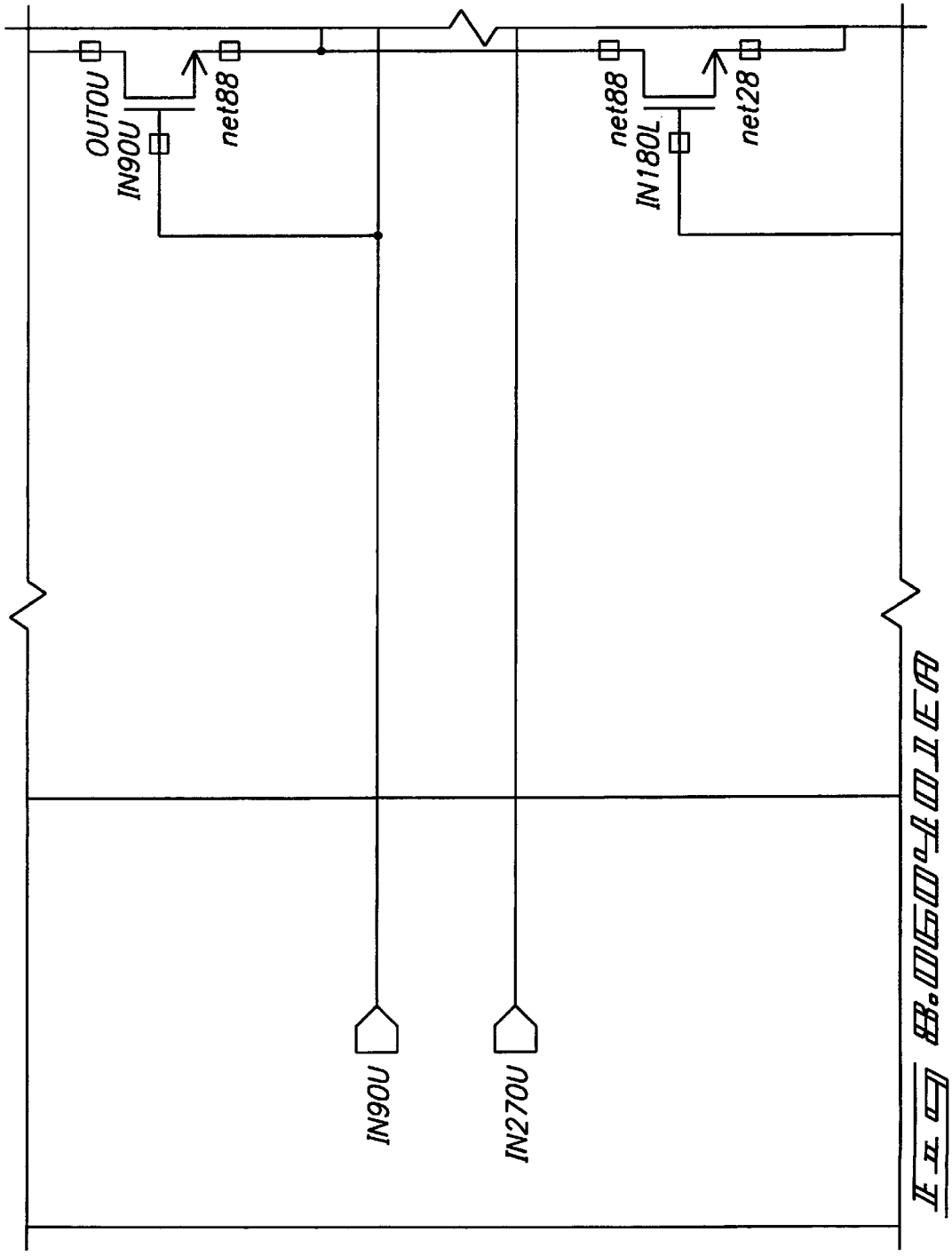


FIG 8,050,088

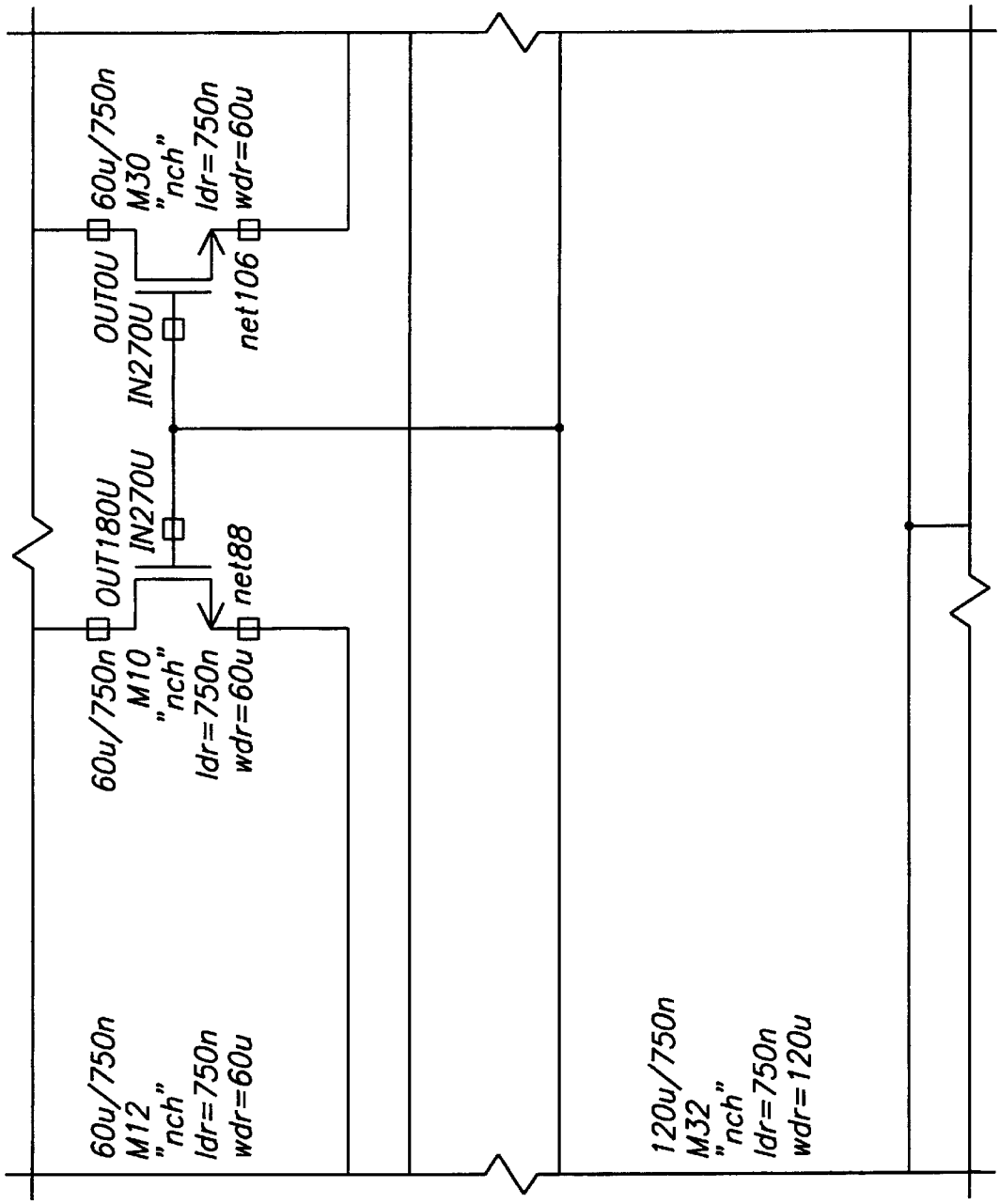

60u/750n
M12
"nch"
ldr=750n
wdr=60u
60u/750n
M10
"nch"
ldr=750n
wdr=60u
OUT180U
IN270U
net88
OUT0U
IN270U
net106
60u/750n
M30
"nch"
ldr=750n
wdr=60u
120u/750n
M32
"nch"
ldr=750n
wdr=120u

FIG. 88,005

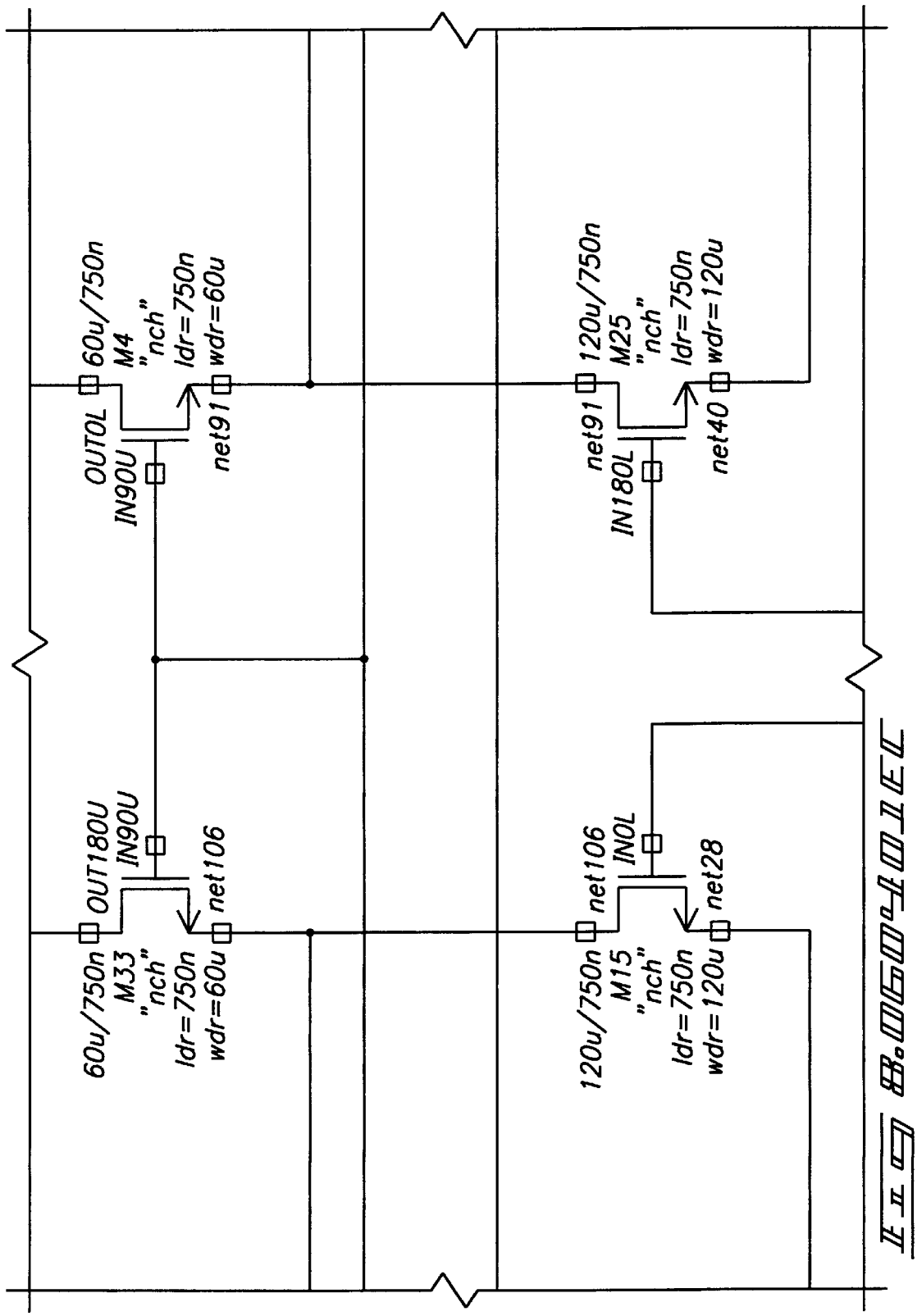

60u/750n
M4
"nch"
ldr=750n
wdr=60u
OUT0L
IN90U
net91
120u/750n
M25
"nch"
ldr=750n
wdr=120u
net91
IN180L
net40
OUT180U
IN90U
net106
60u/750n
M33
"nch"
ldr=750n
wdr=60u
net106
IN0L
net28
120u/750n
M15
"nch"
ldr=750n
wdr=120u

FIG. 8,050,008

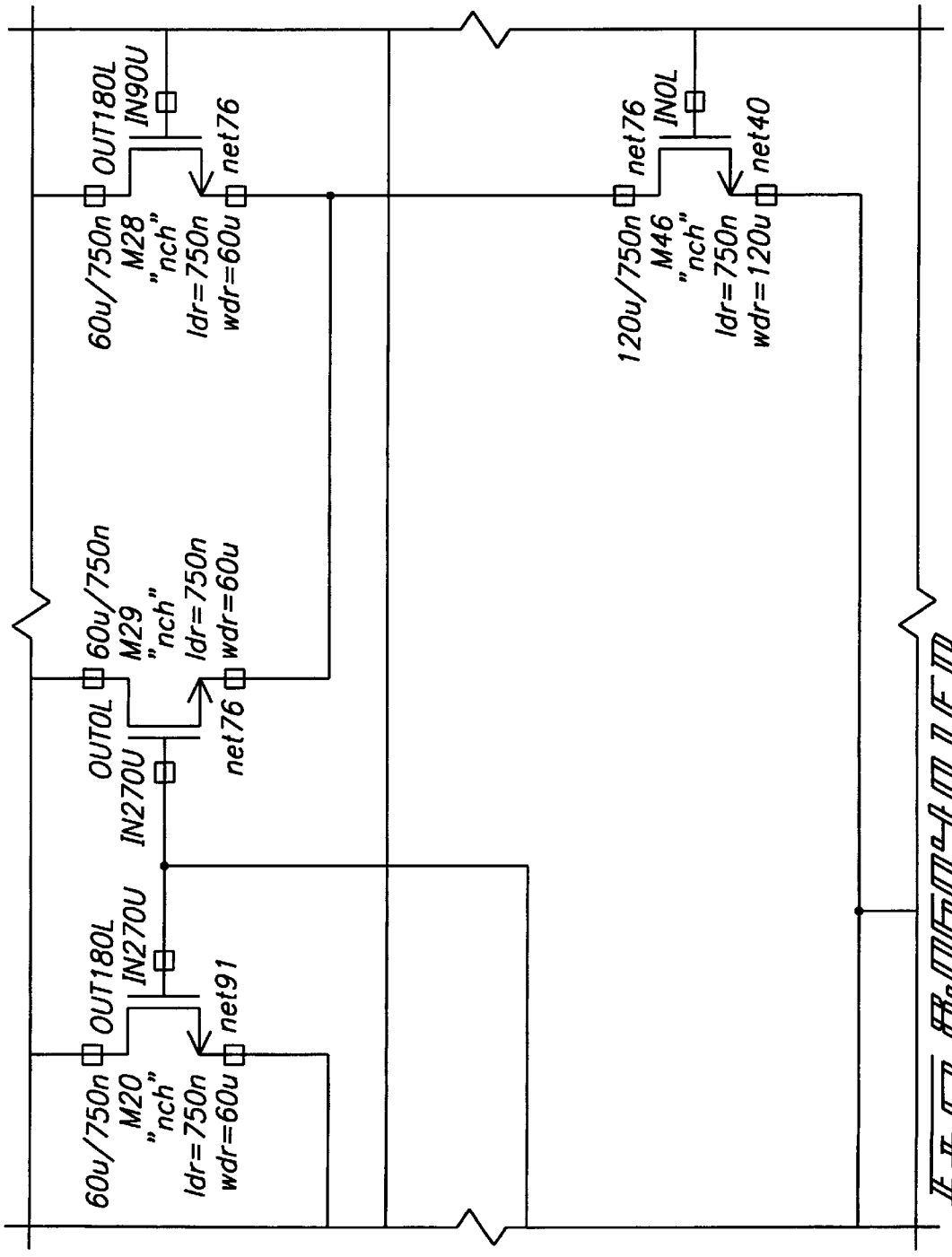

60u/750n
M28
"nch"
ldr=750n
wdr=60u
OUT180L
IN90U
net76
60u/750n
M29
"nch"
ldr=750n
wdr=60u
OUT0L
IN270U
net76
60u/750n
M20
"nch"
ldr=750n
wdr=60u
OUT180L
IN270U
net91
120u/750n
M46
"nch"
ldr=750n
wdr=120u
net76
IN0L
net40

FIG 8,060,401

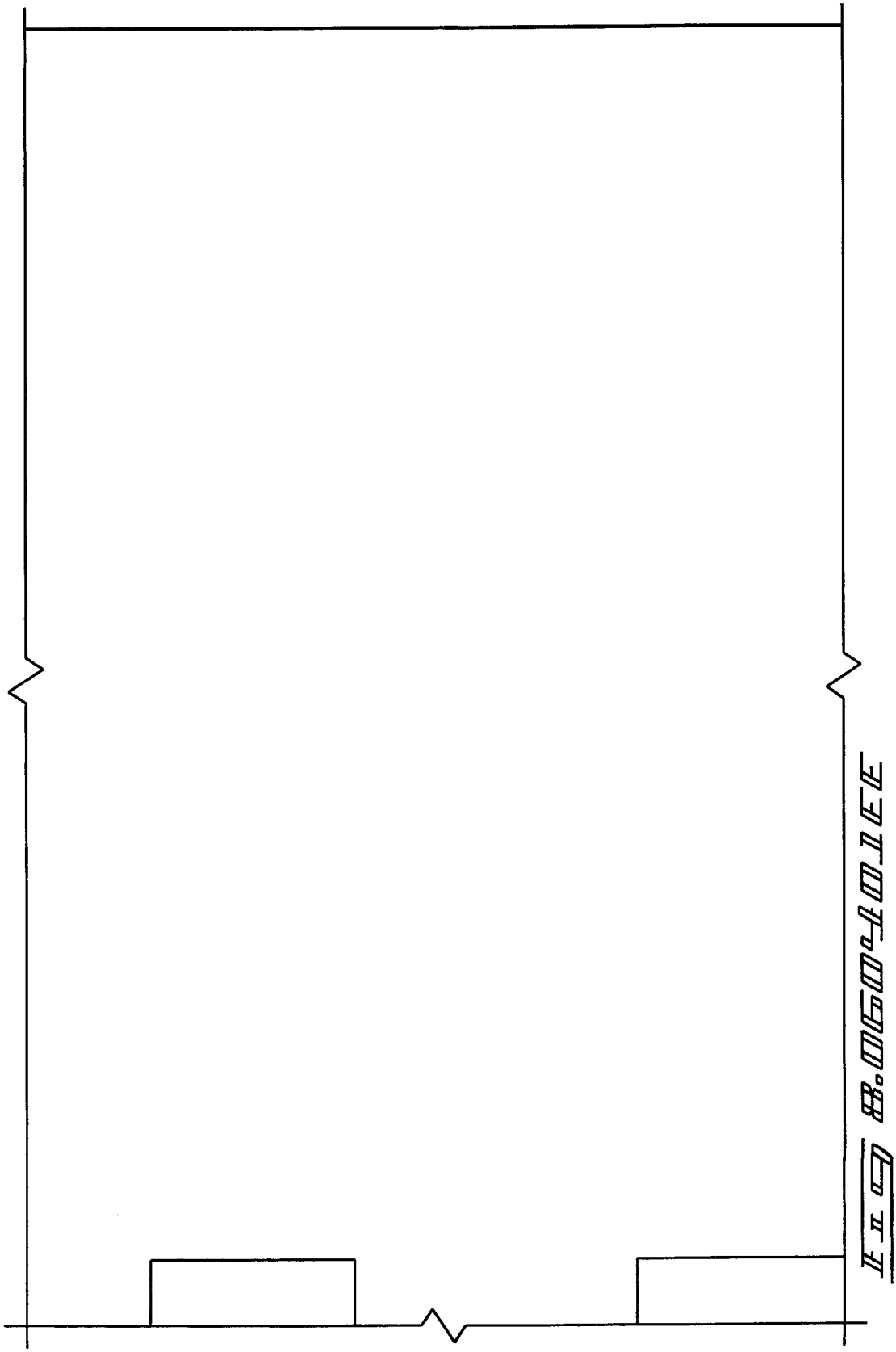


FIG. 8,050,900

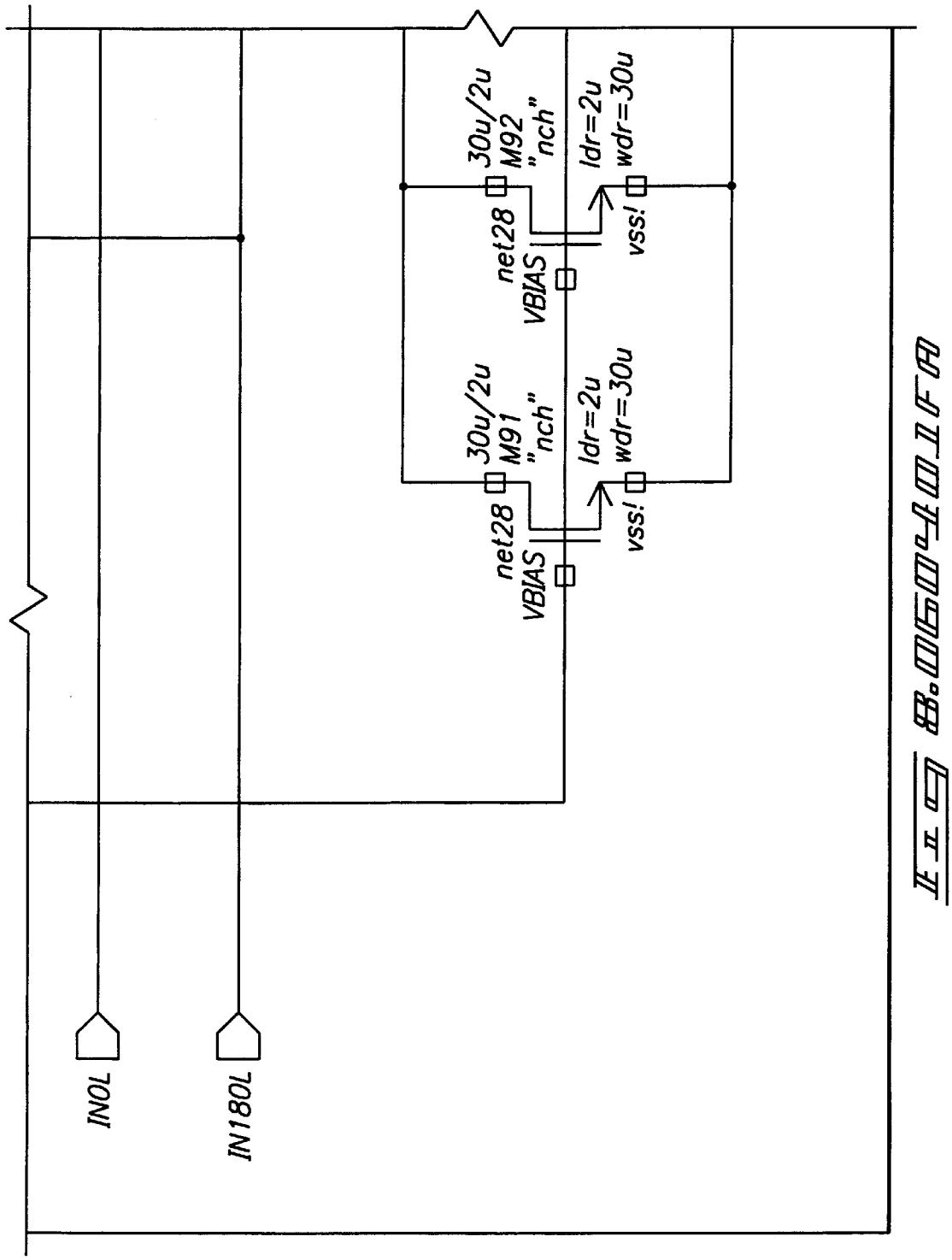

30u/2u
M92
"nch"
ldr=2u
wdr=30u
net28
VBIAS
vss!
30u/2u
M91
"nch"
ldr=2u
wdr=30u
net28
VBIAS
vss!
IN0L
IN180L

FIG. 88,059

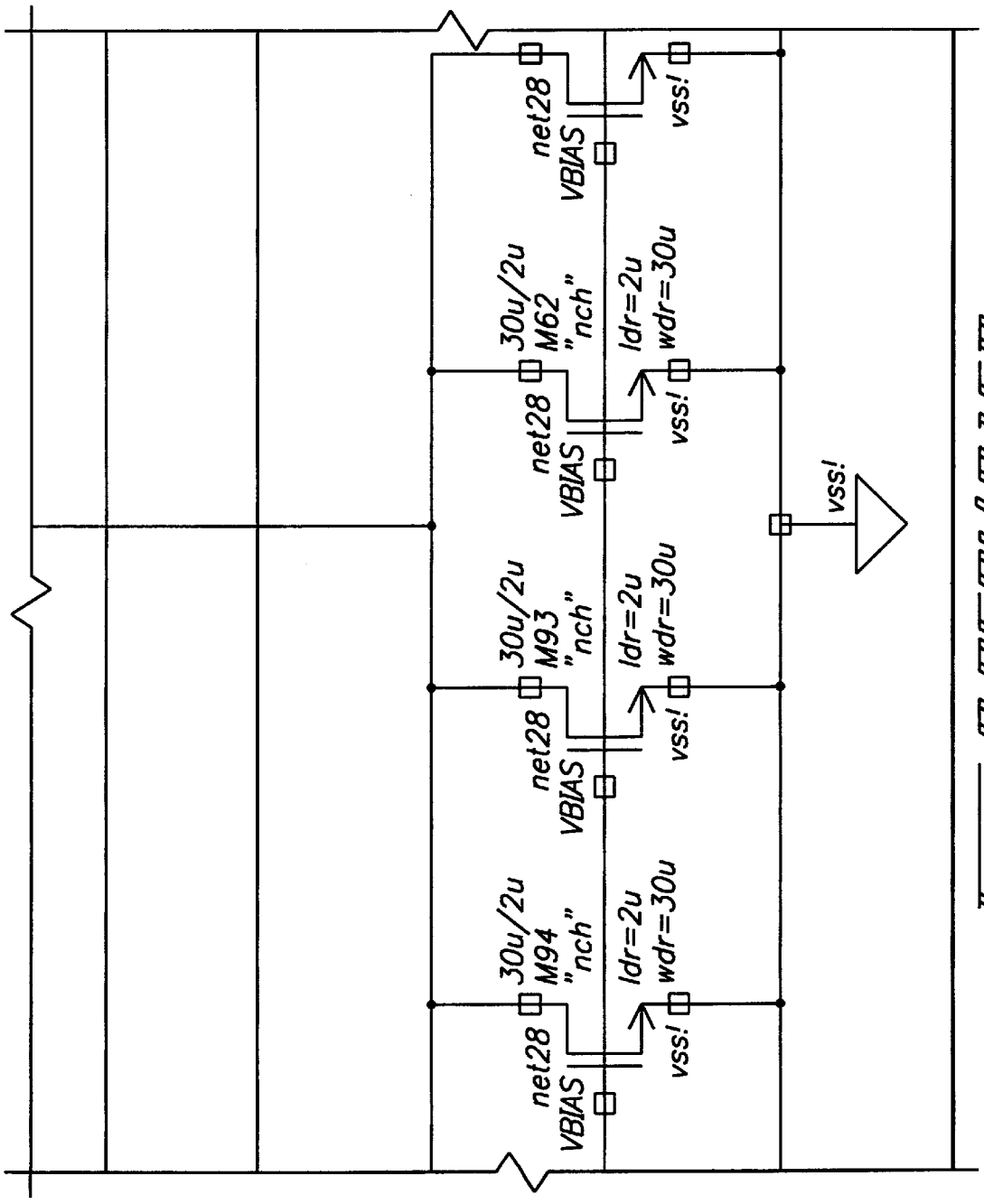


FIG. 88.0050 of 188

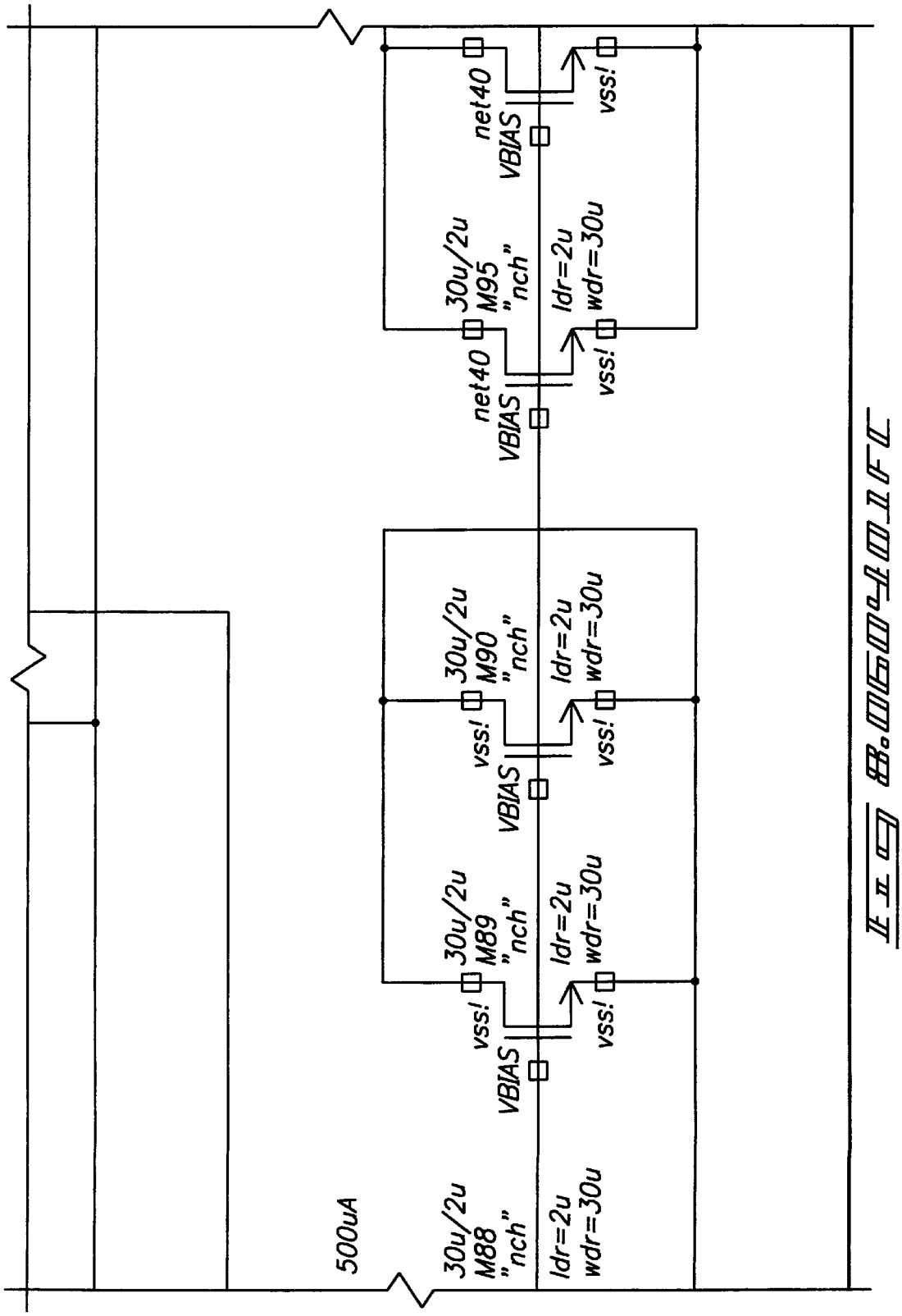


Fig 88.0604.0011FC

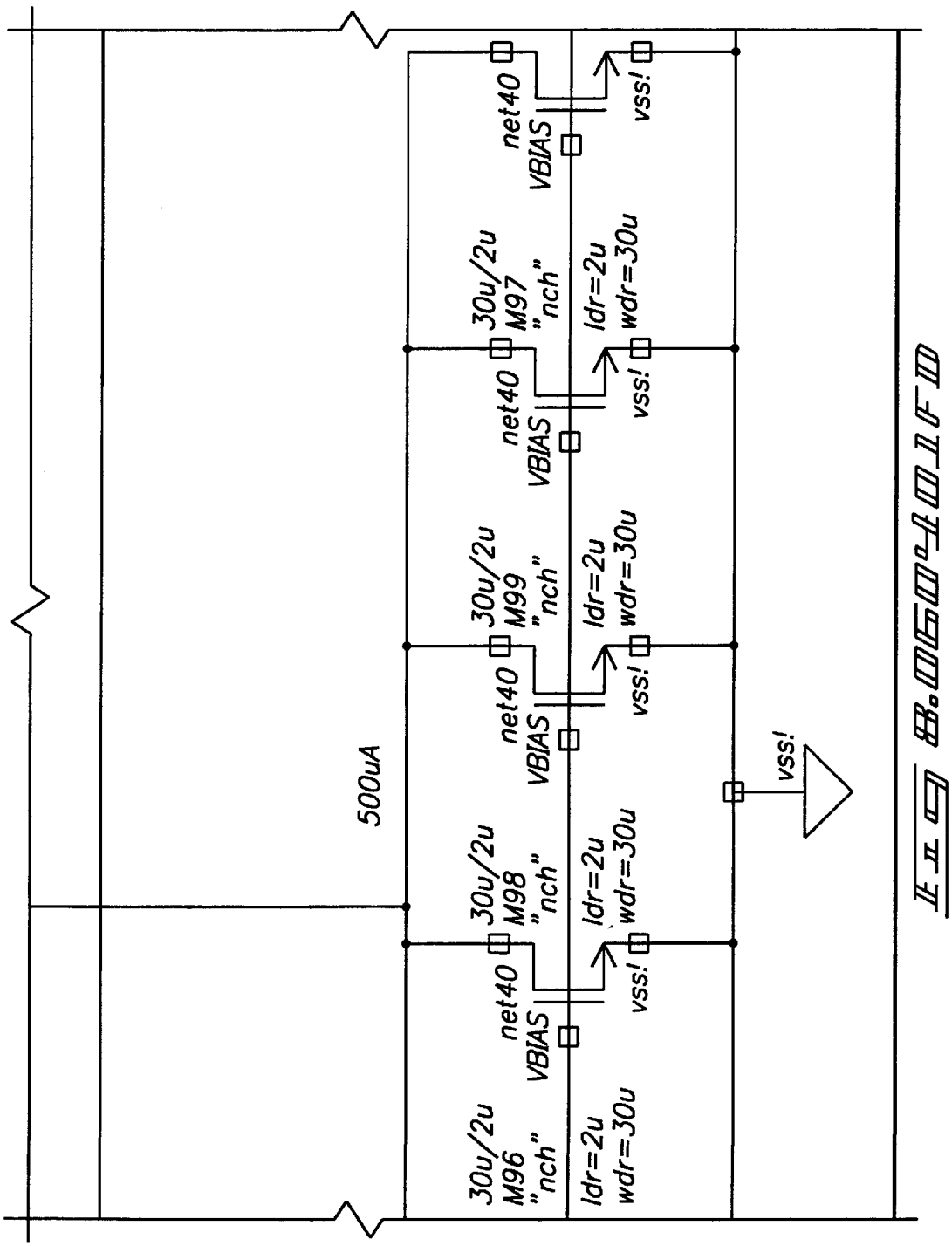


FIG 8.0500.01.0

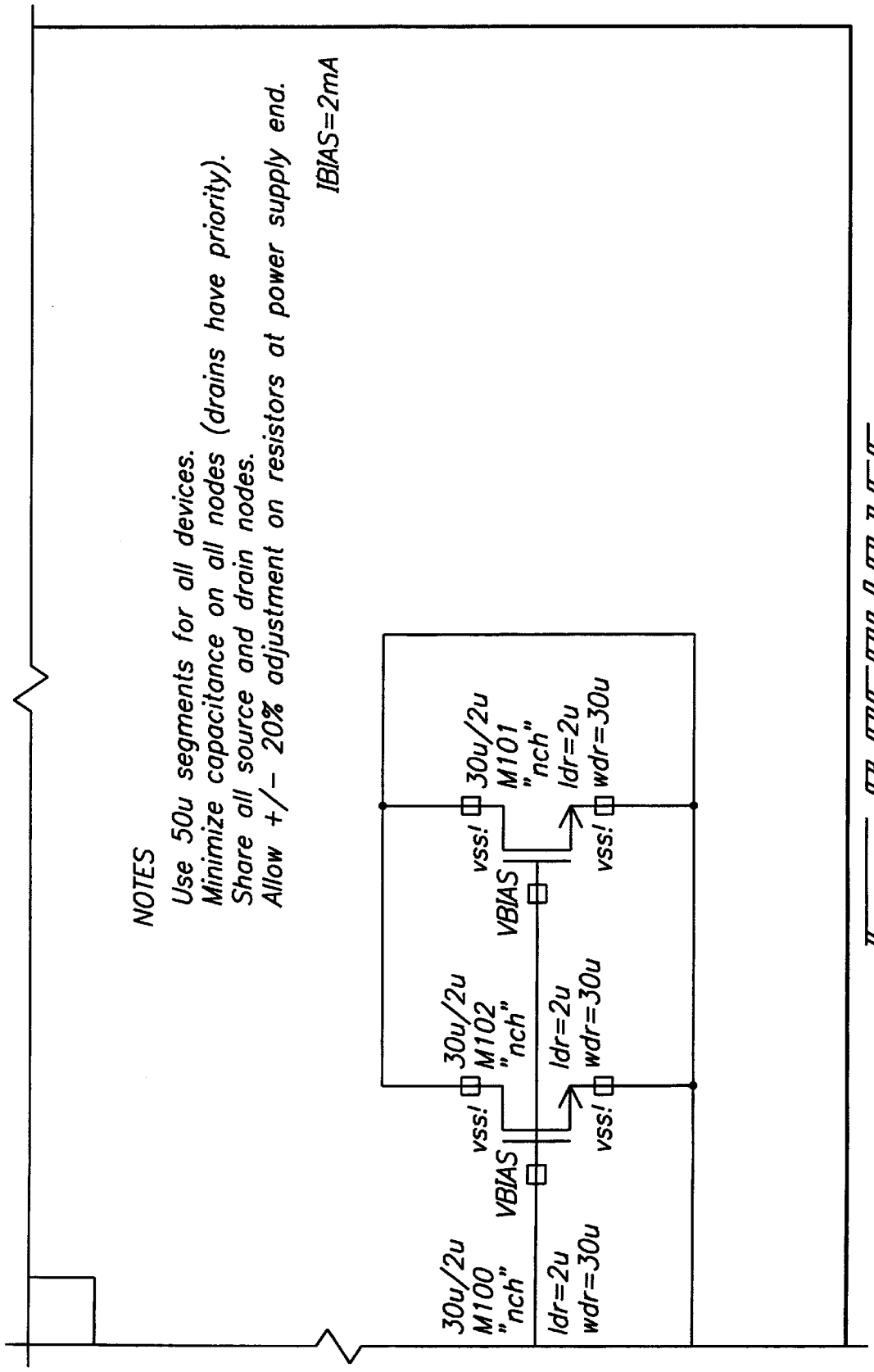
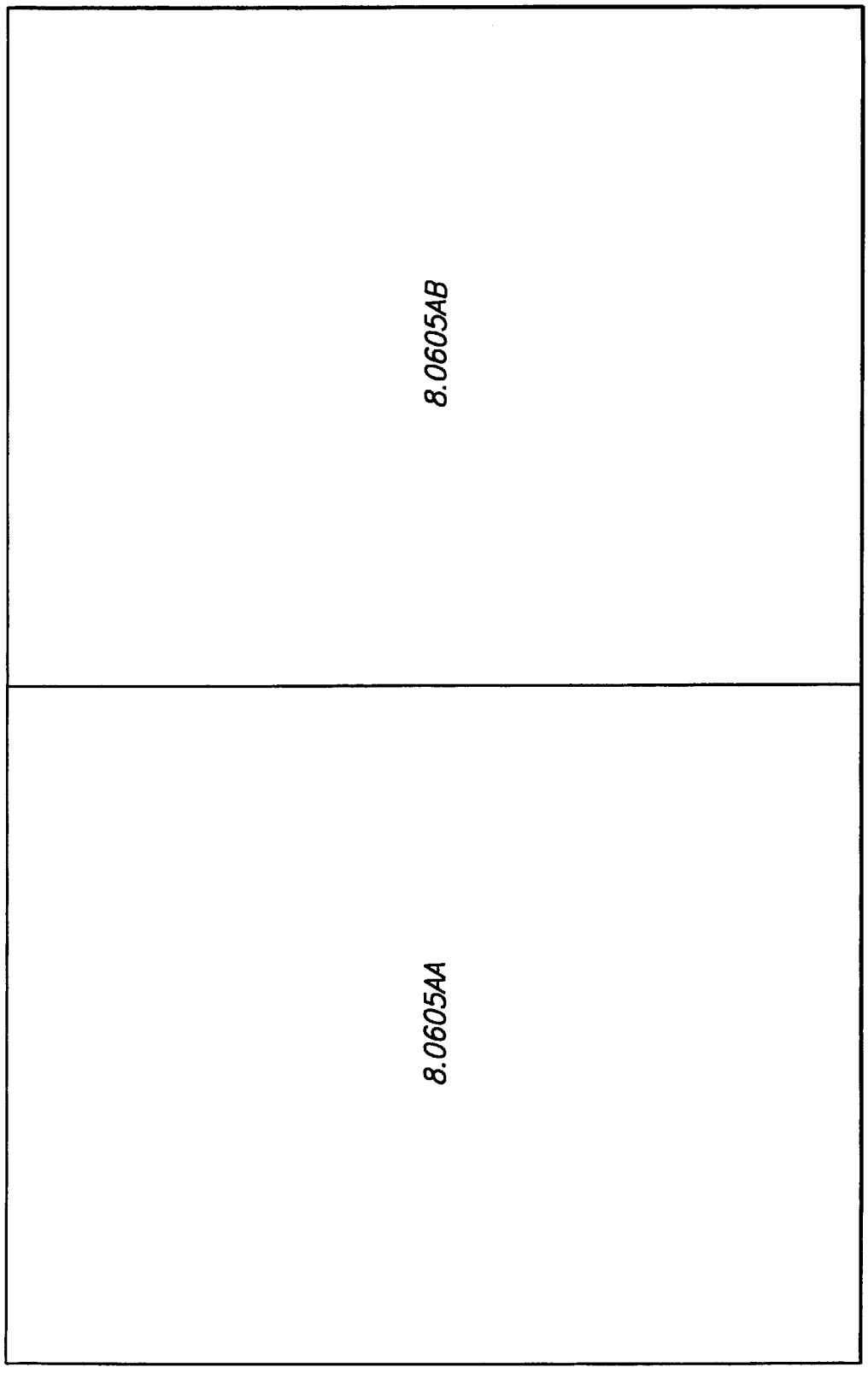


FIG 88.0056 ALIFE


8.0605AB
8.0605AA
FIG. 8.0605

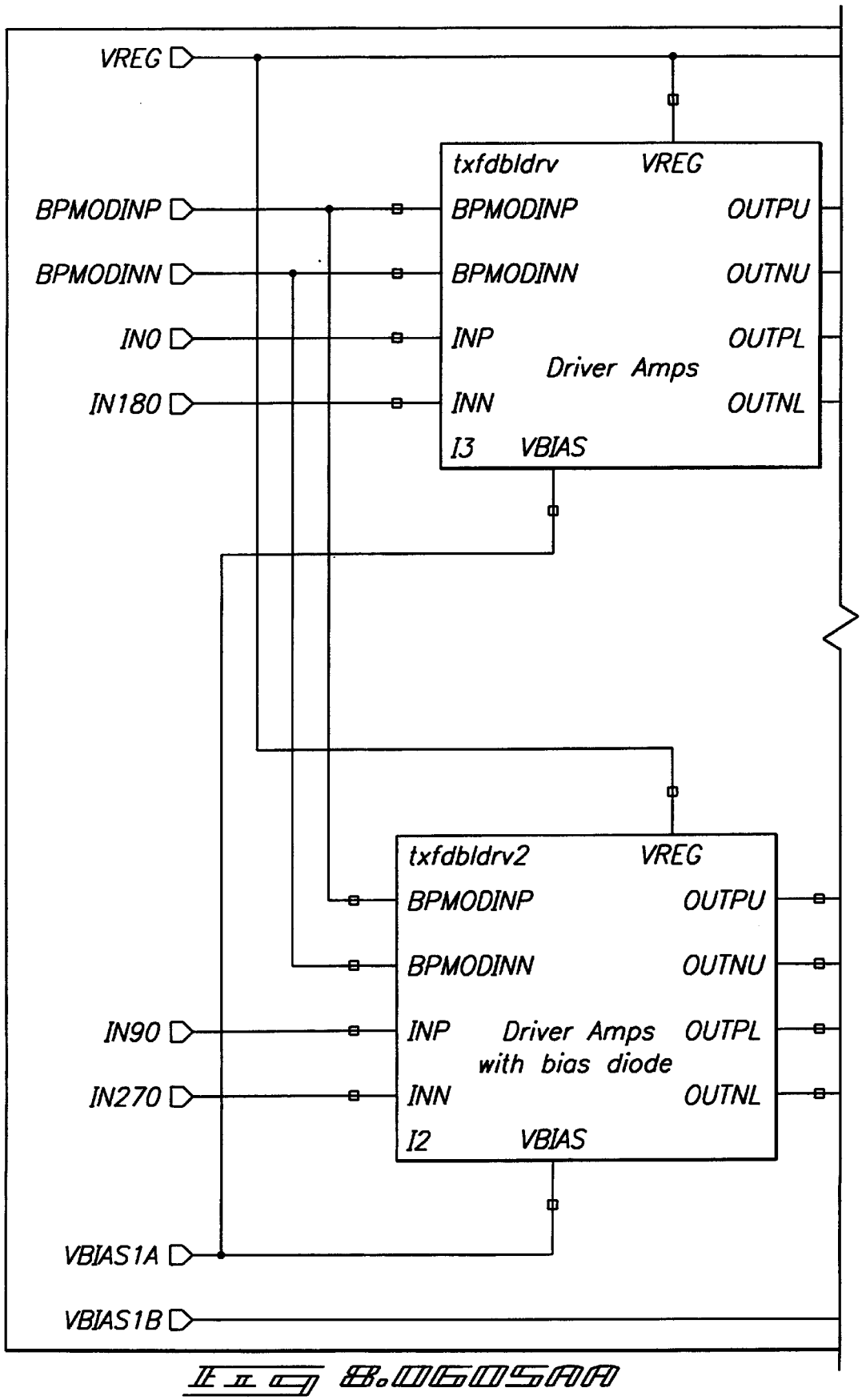

VREG
txfdbldrv
VREG
BPMODINP
BPMODINP
OUTPU
BPMODINN
BPMODINN
OUTNU
IN0
INP
OUTPL
Driver Amps
IN180
INN
OUTNL
I3
VBIAS
txfdbldrv2
VREG
BPMODINP
OUTPU
BPMODINN
OUTNU
IN90
INP
Driver Amps
OUTPL
with bias diode
IN270
INN
OUTNL
I2
VBIAS
VBIAS1A
VBIAS1B

Fig 8.0605AA

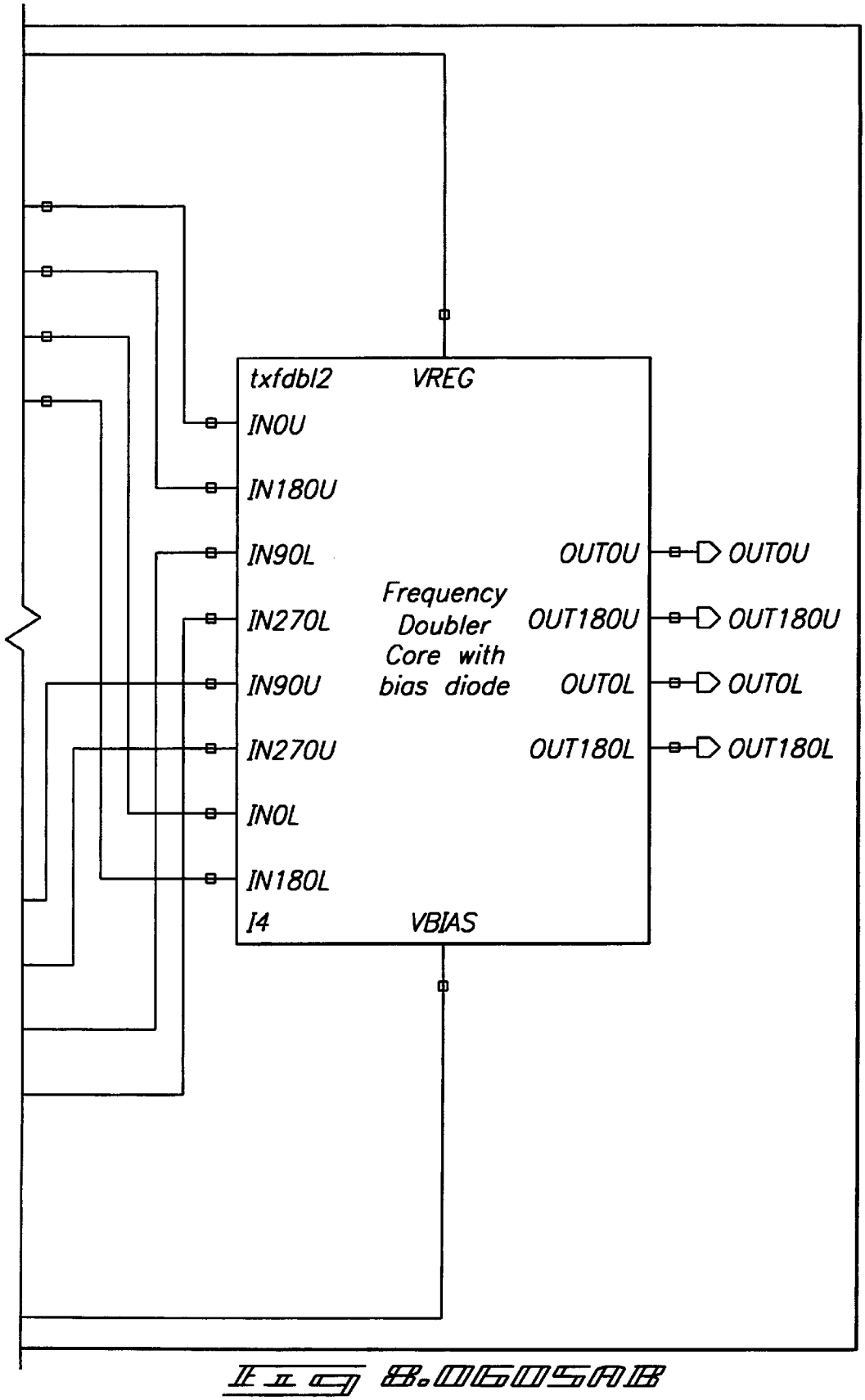


Fig 88.0605AB

8.060501AA	8.060501AB	8.060501AC	8.060501AD
8.060501BA	8.060501BB	8.060501BC	8.060501BD
8.060501CA	8.060501CB	8.060501CC	8.060501CD

Fig 8.060501

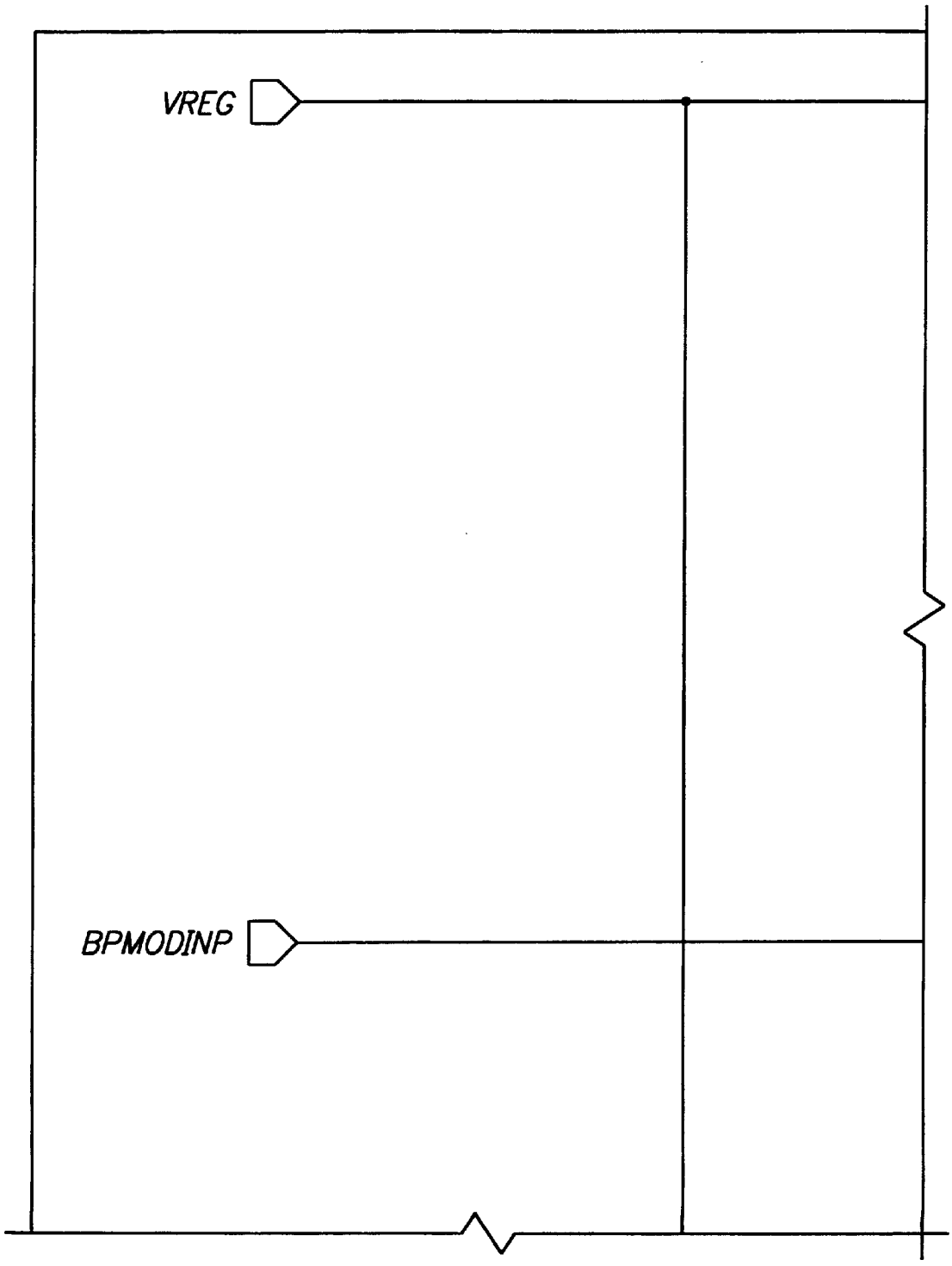


Fig 88.0605011AA

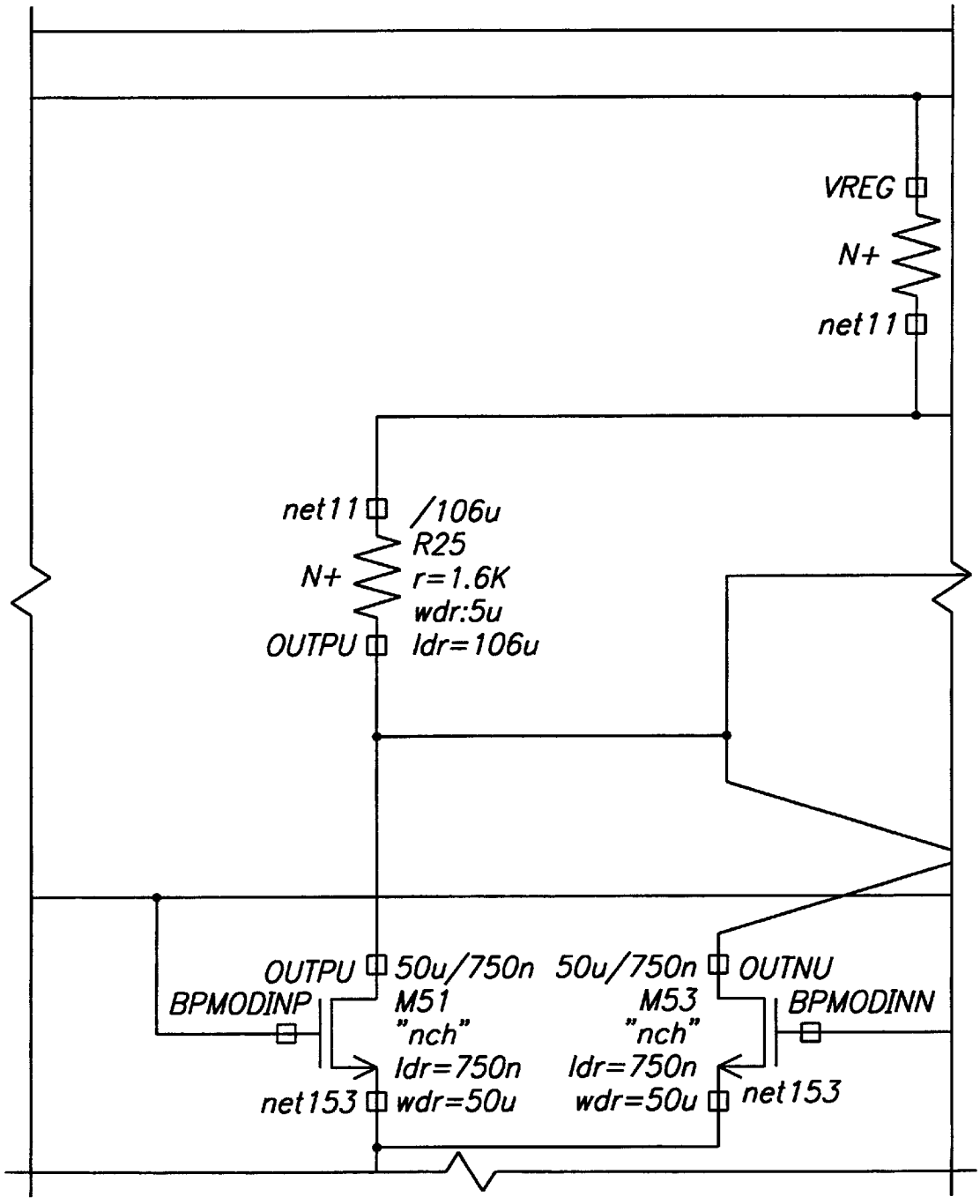


Fig 8.0605012AB

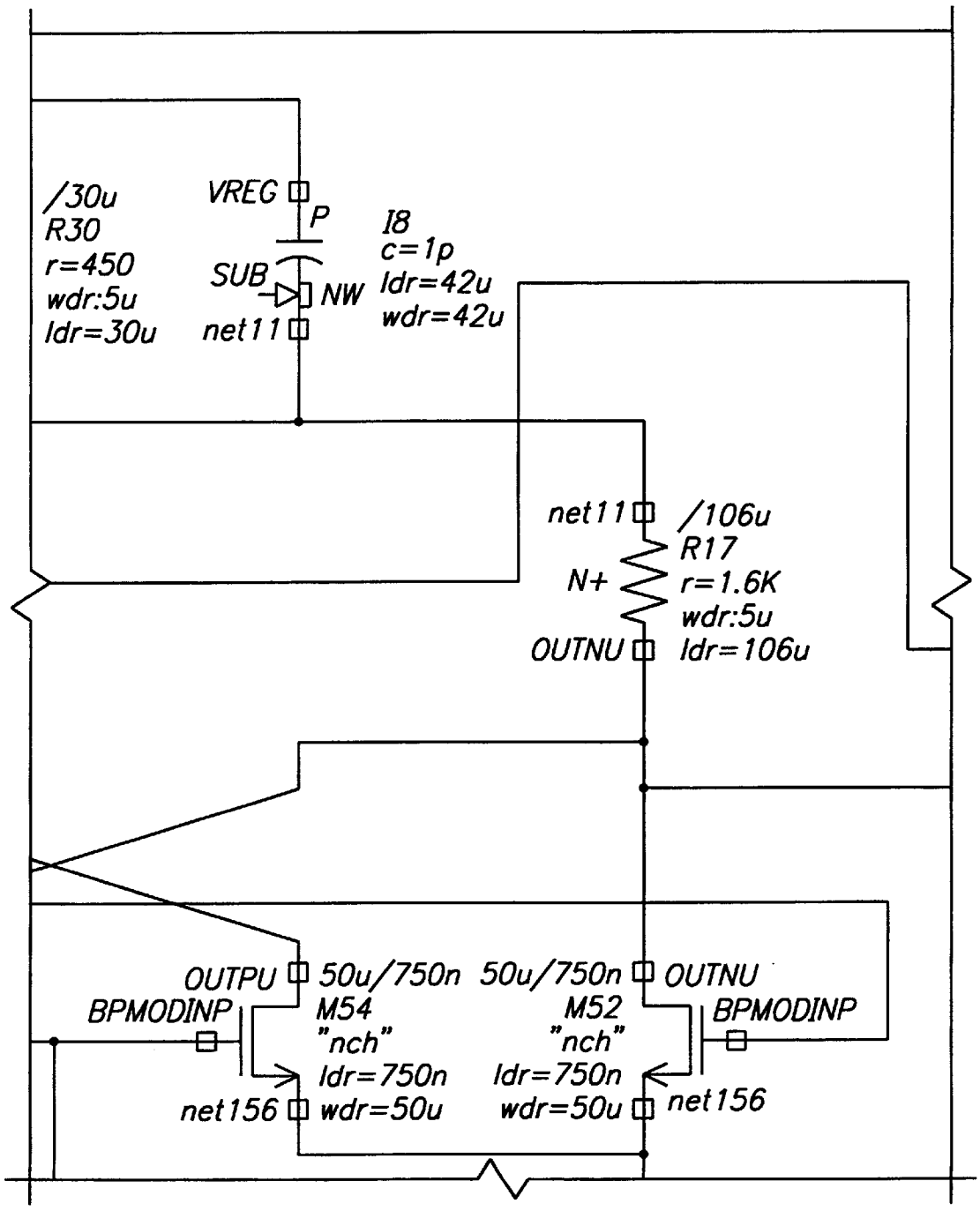


Fig 8.060501AC

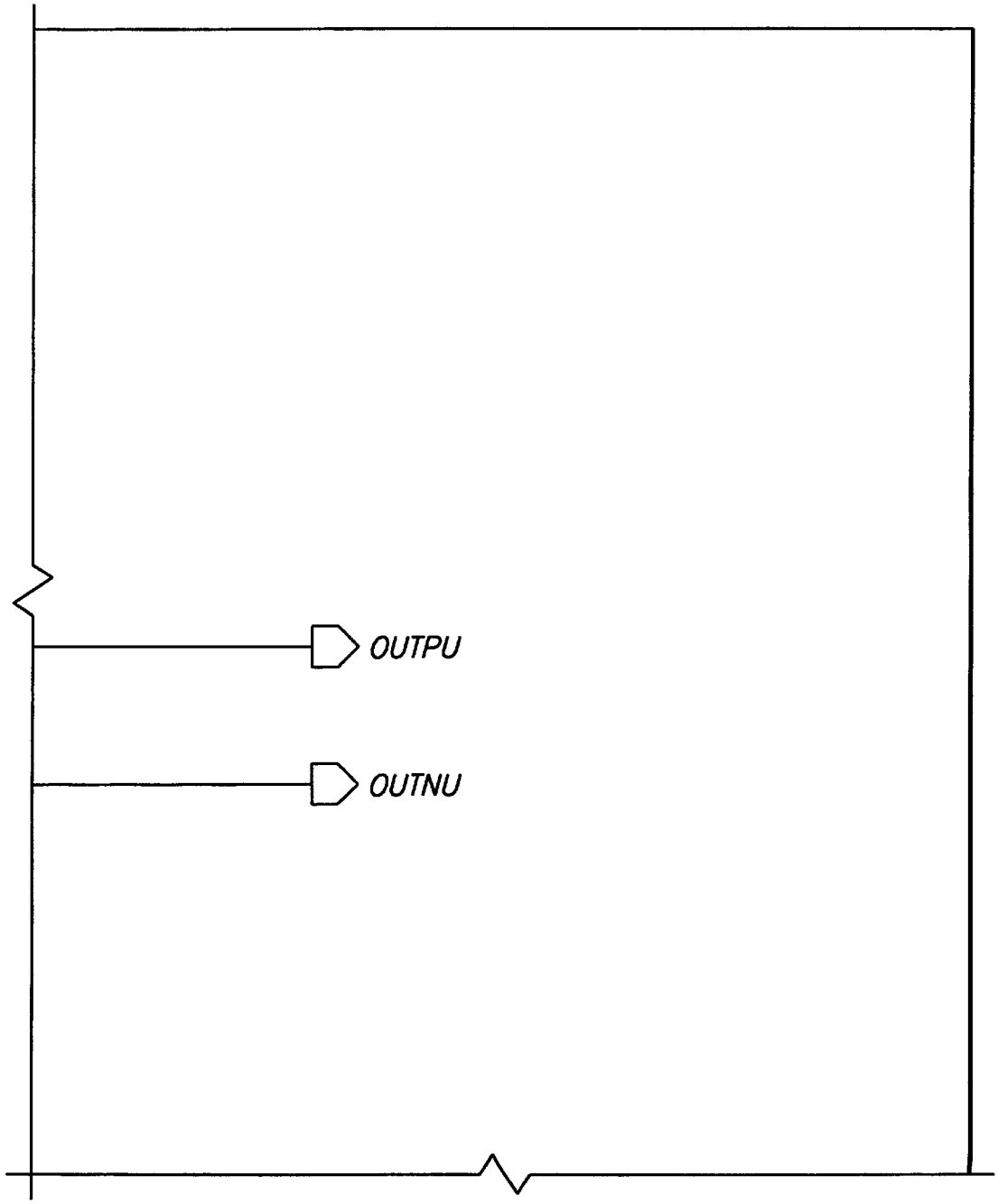


Fig 8.060501AD

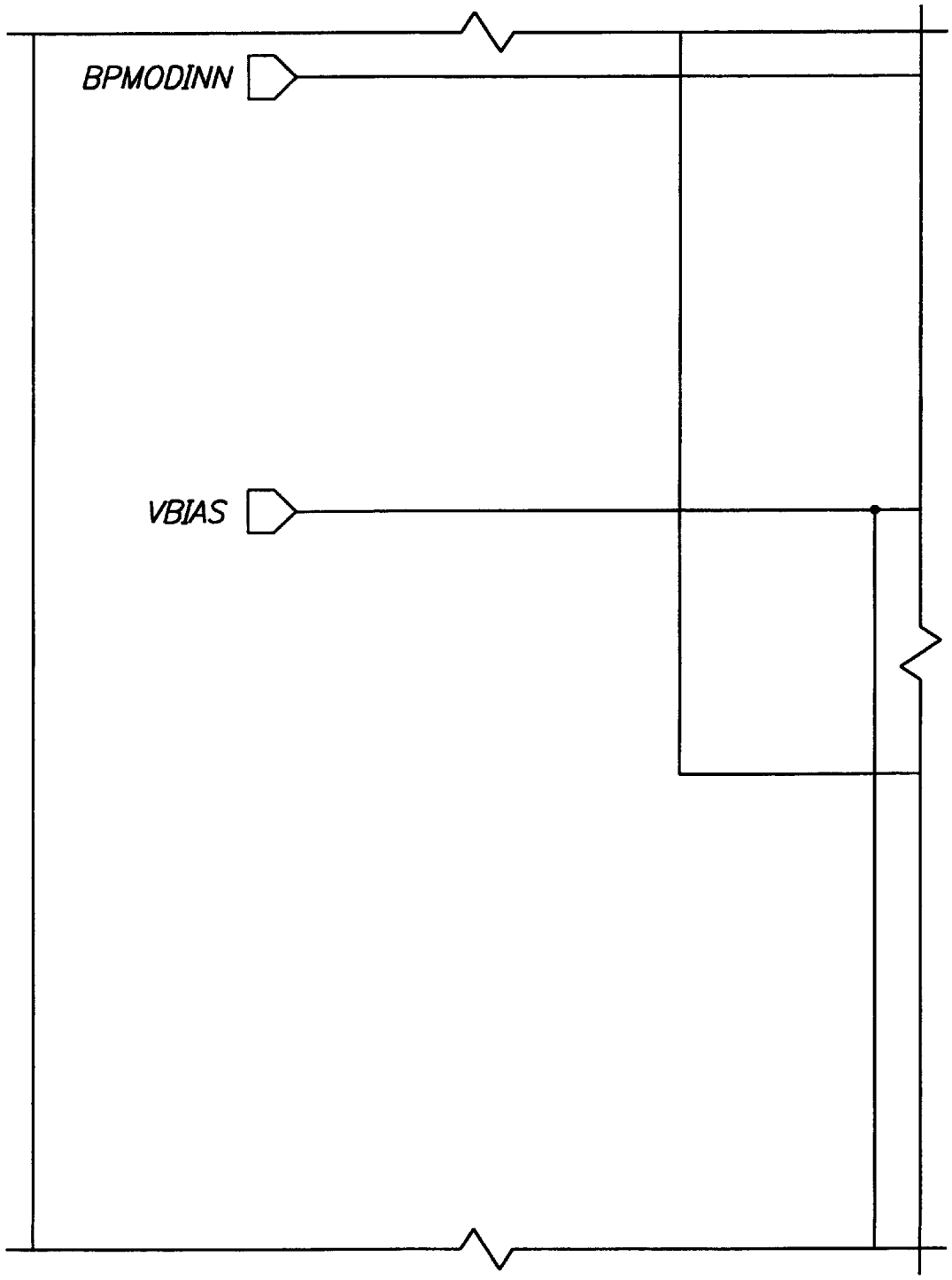


Fig 8.060501BA

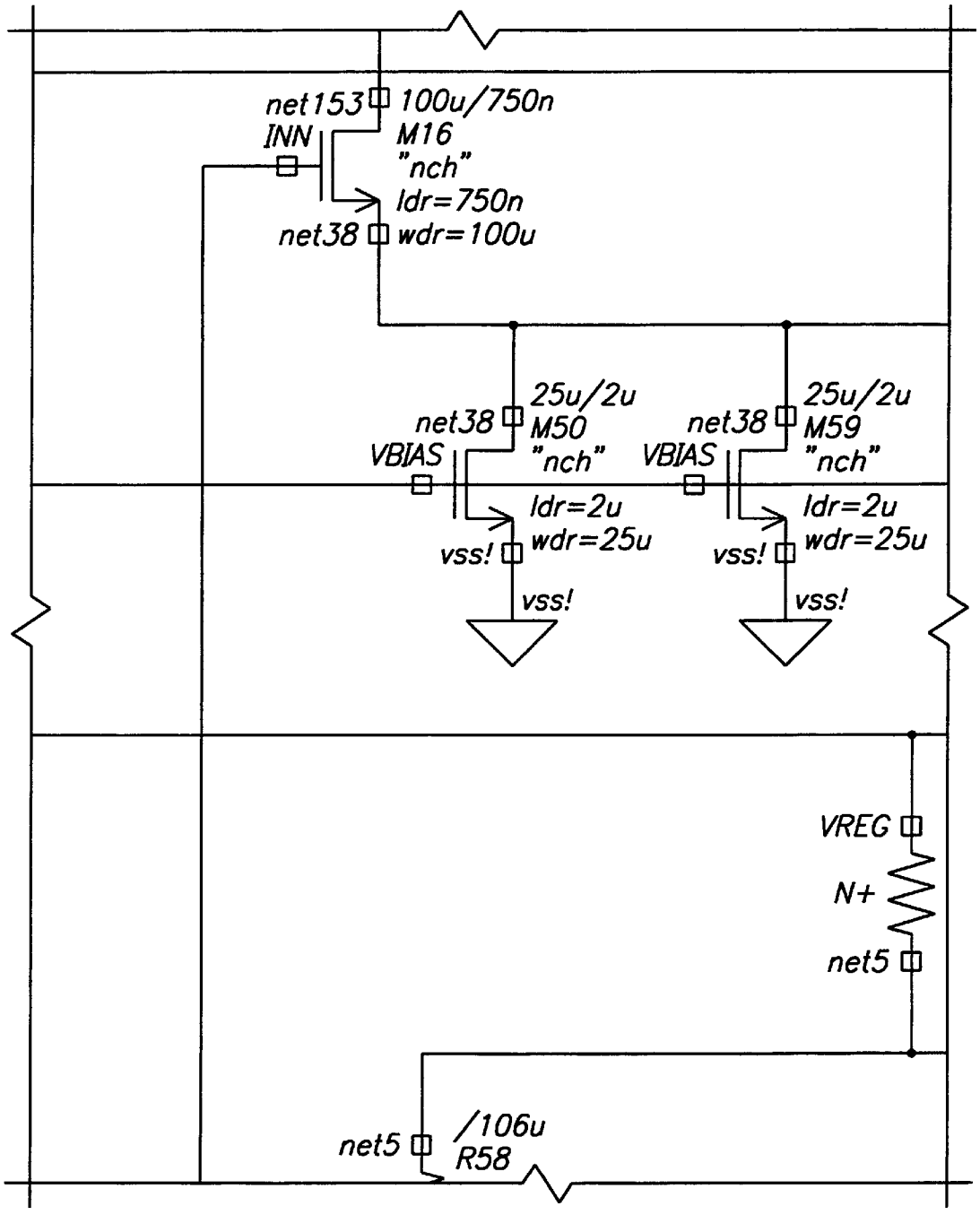


Fig 8,060,501 BB

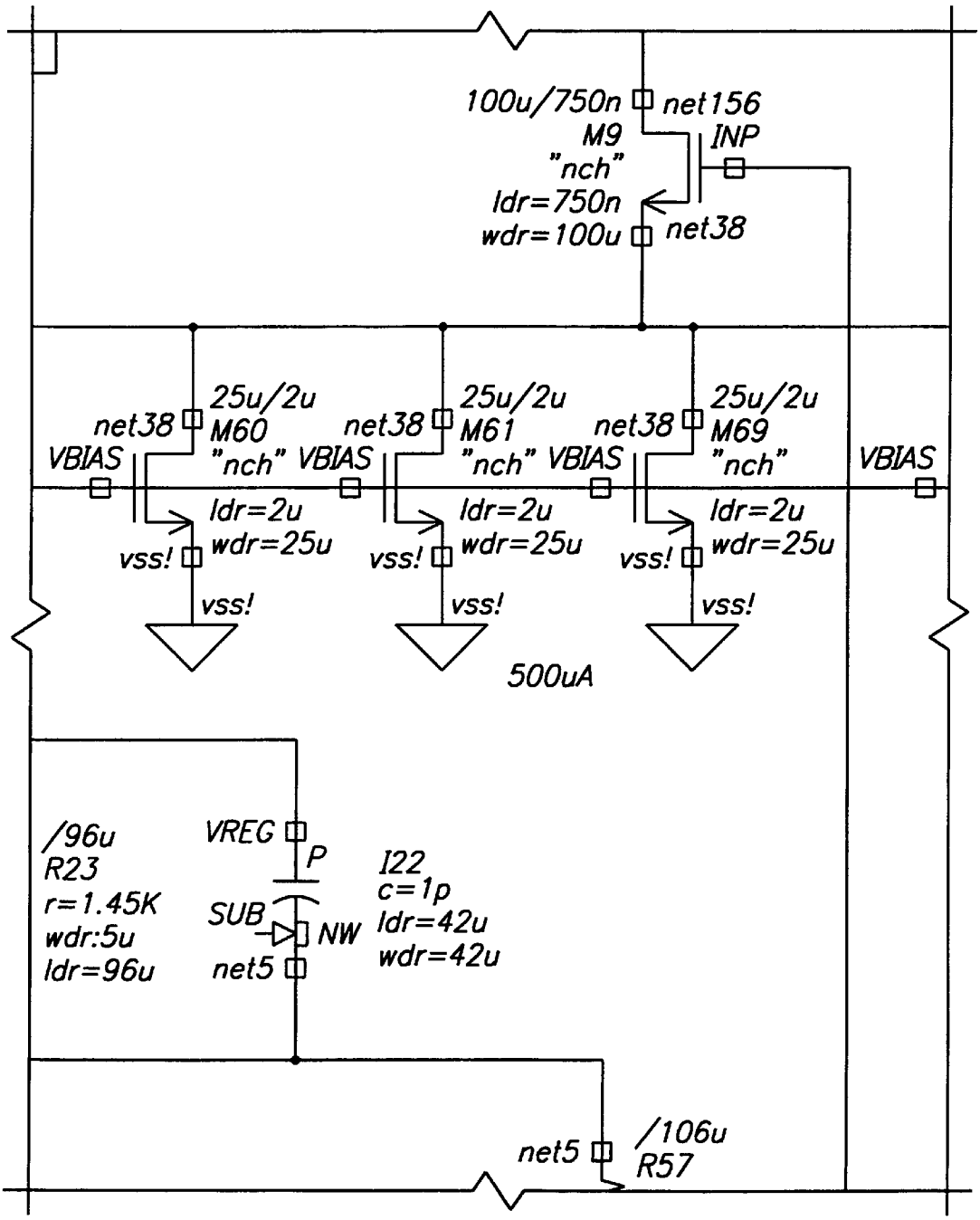


Fig 8.060501BC

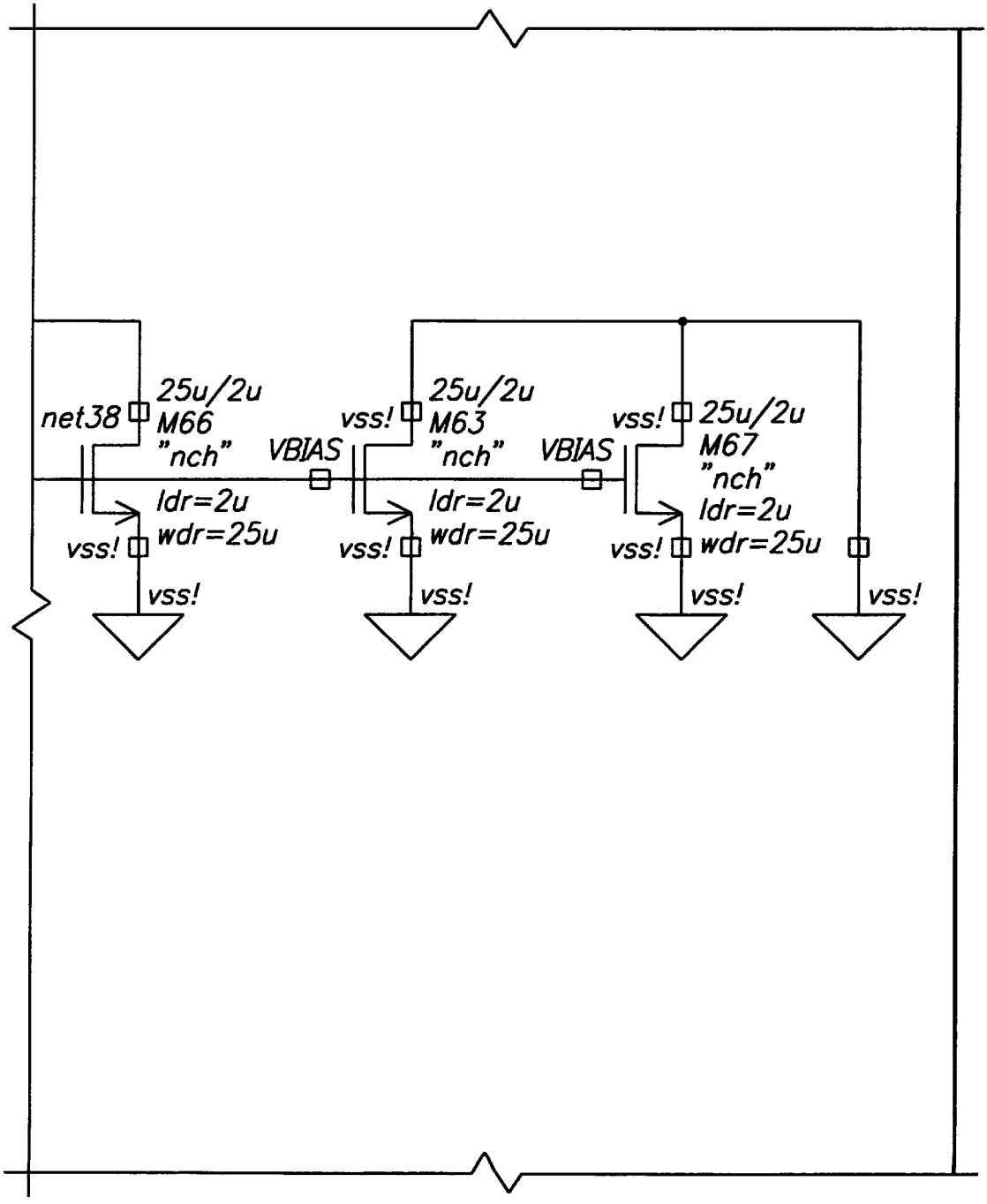


Fig 8.0605012D

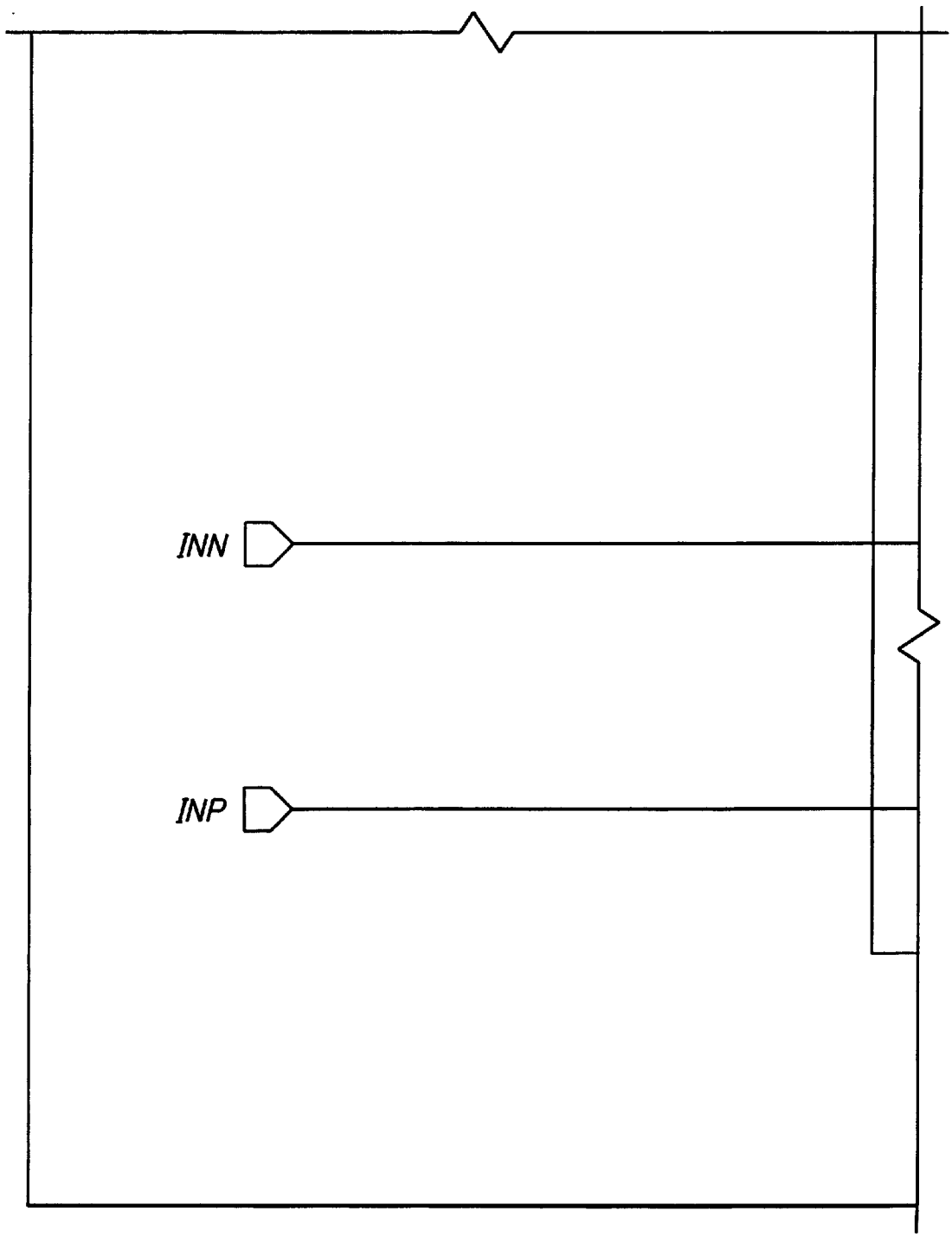


Fig 8.060501CA

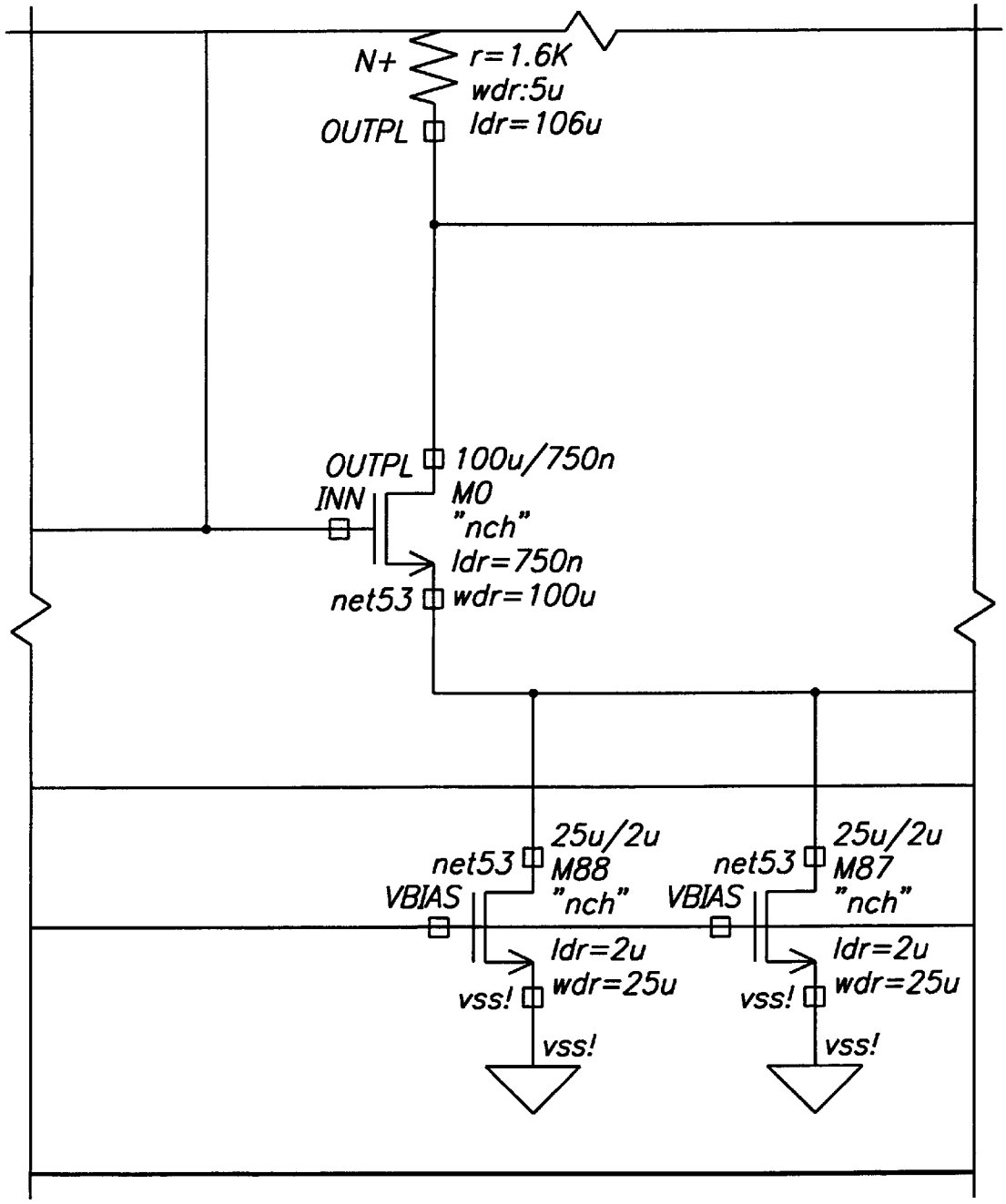


Fig 8.0605011CB

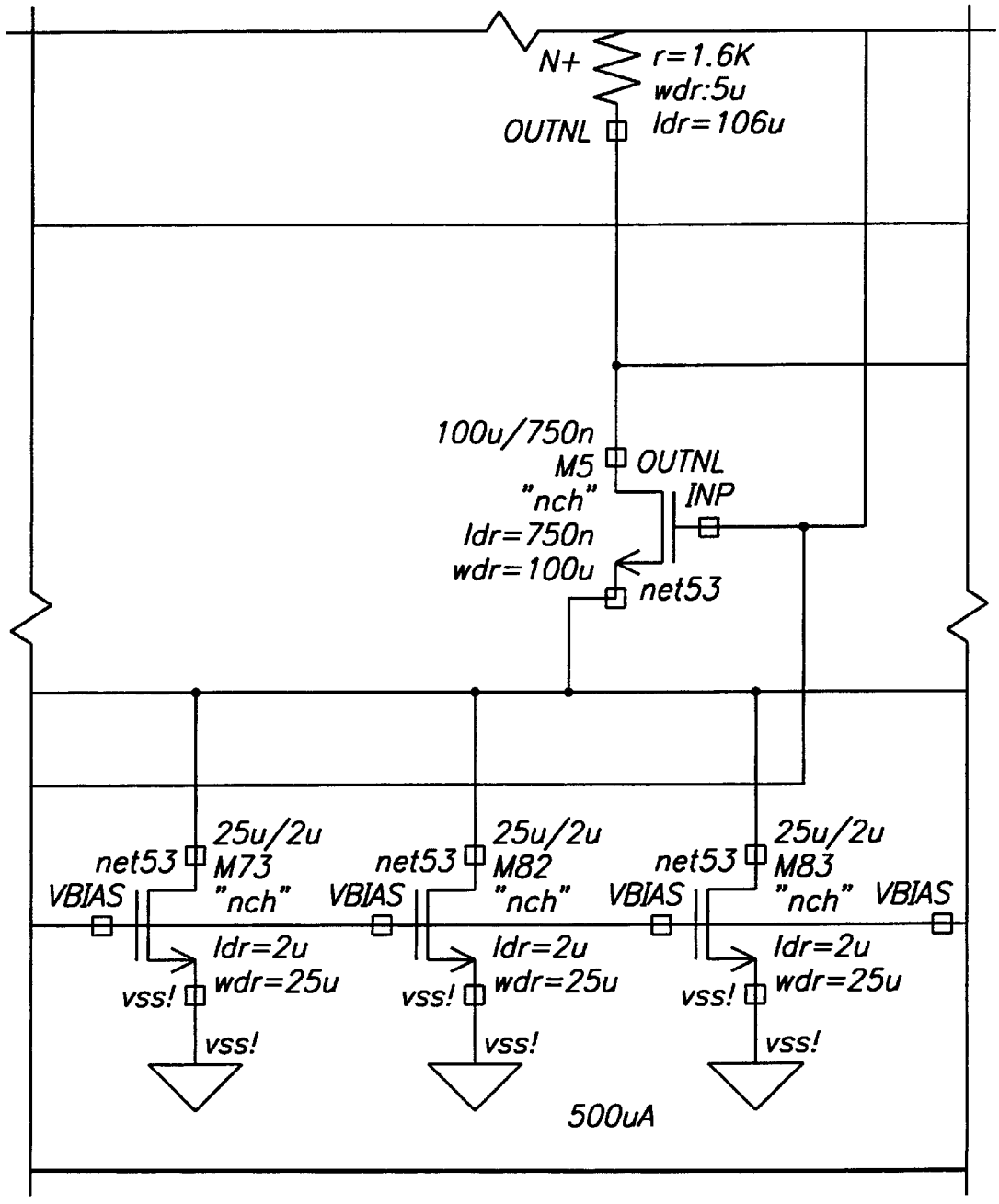


Fig 8.0605011C

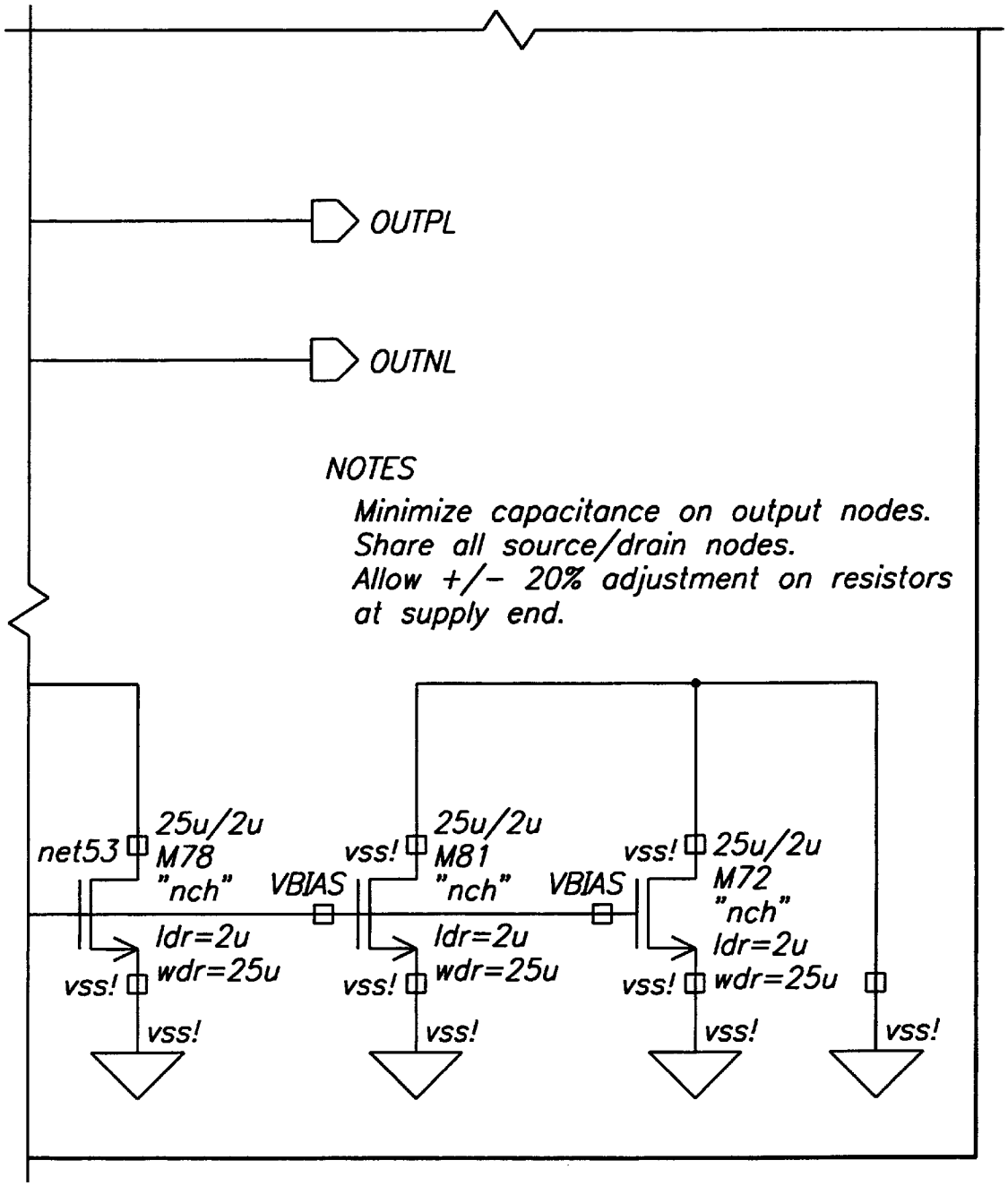


Fig 8.060501CD

8.060502AA	8.060502AB	8.060502AC	8.060502AD
8.060502BA	8.060502BB	8.060502BC	8.060502BD
8.060502CA	8.060502CB	8.060502CC	8.060502CD

Fig 8.060502

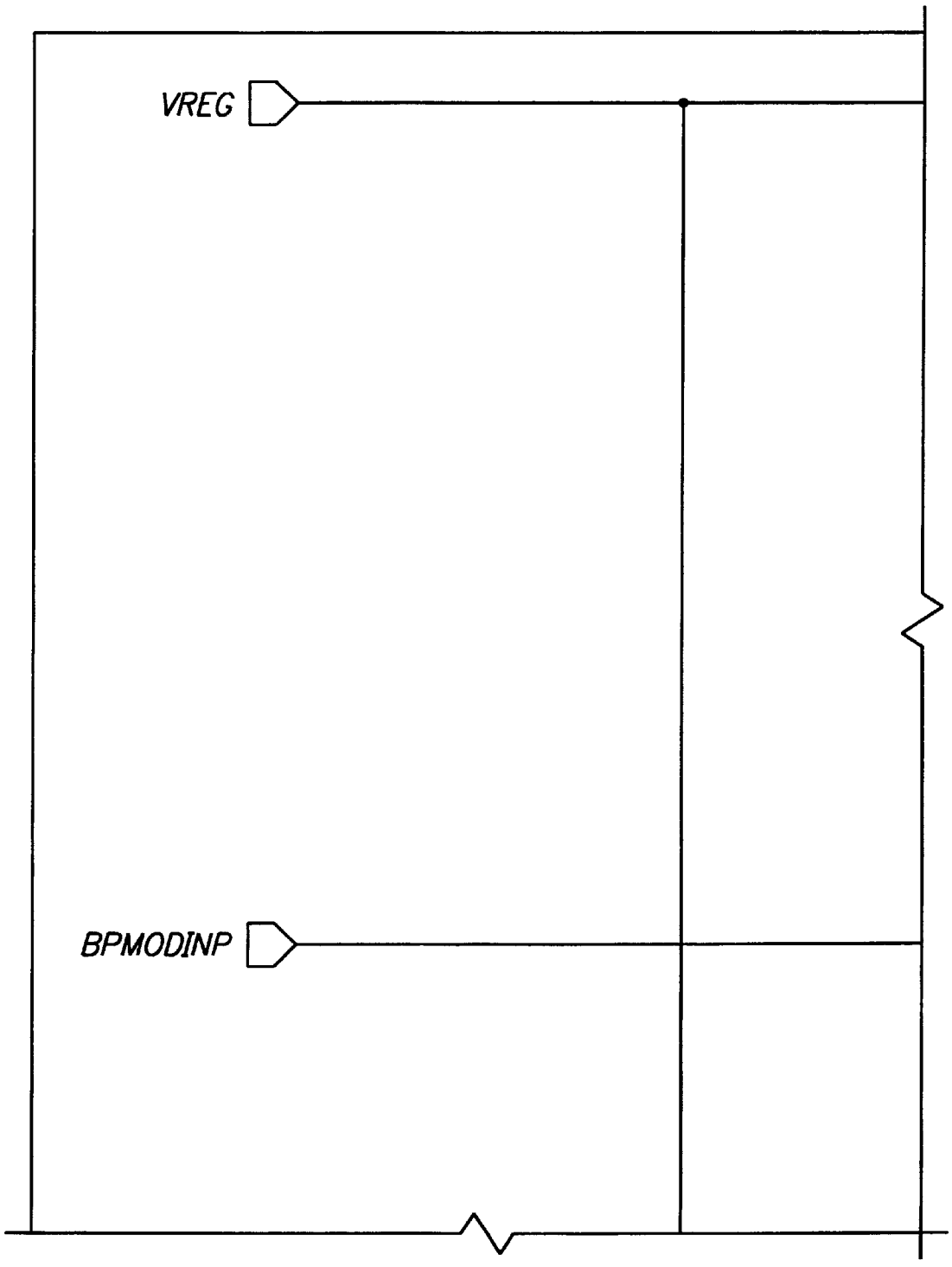


Fig 88.0605002AA

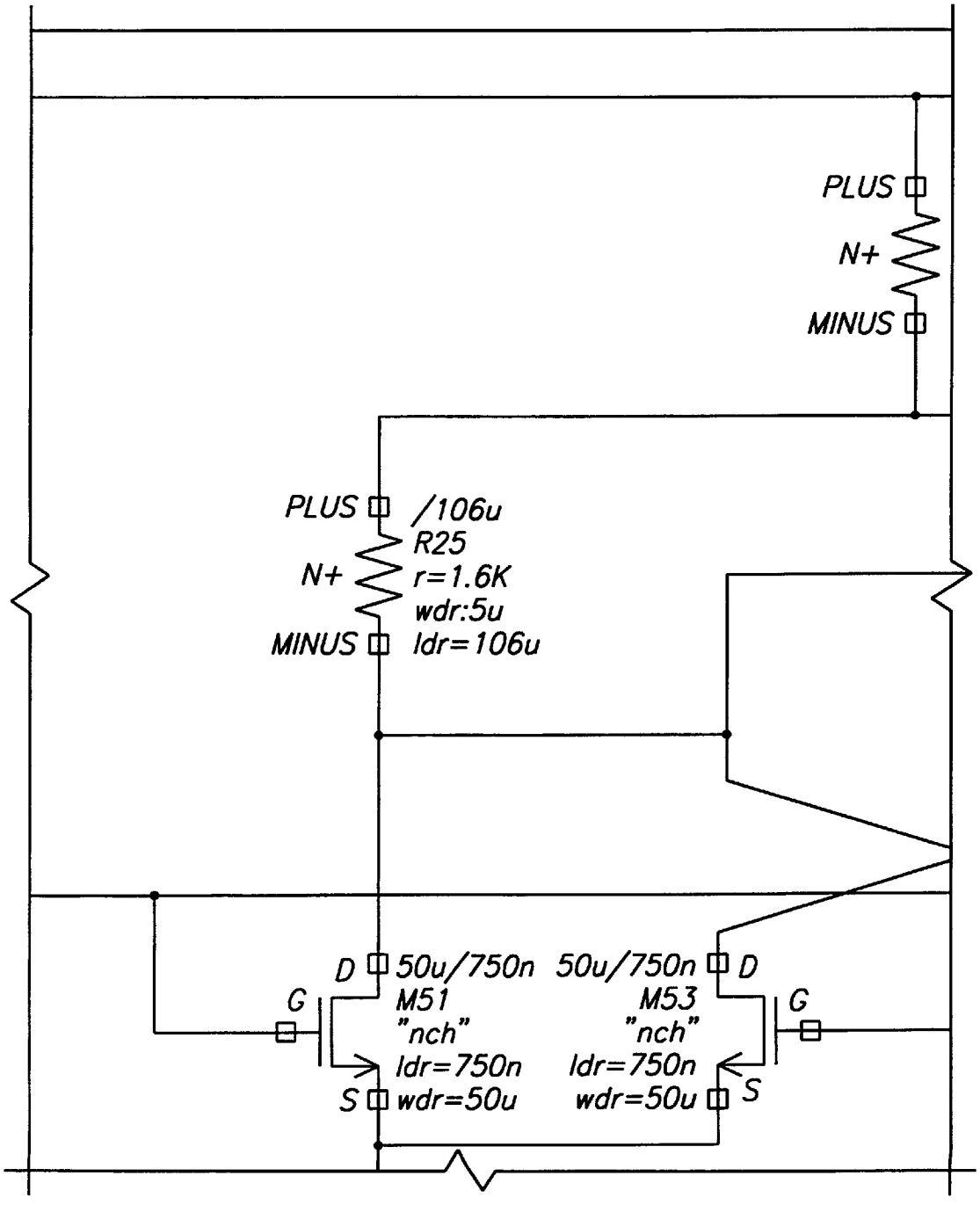


Fig 8.060502AB

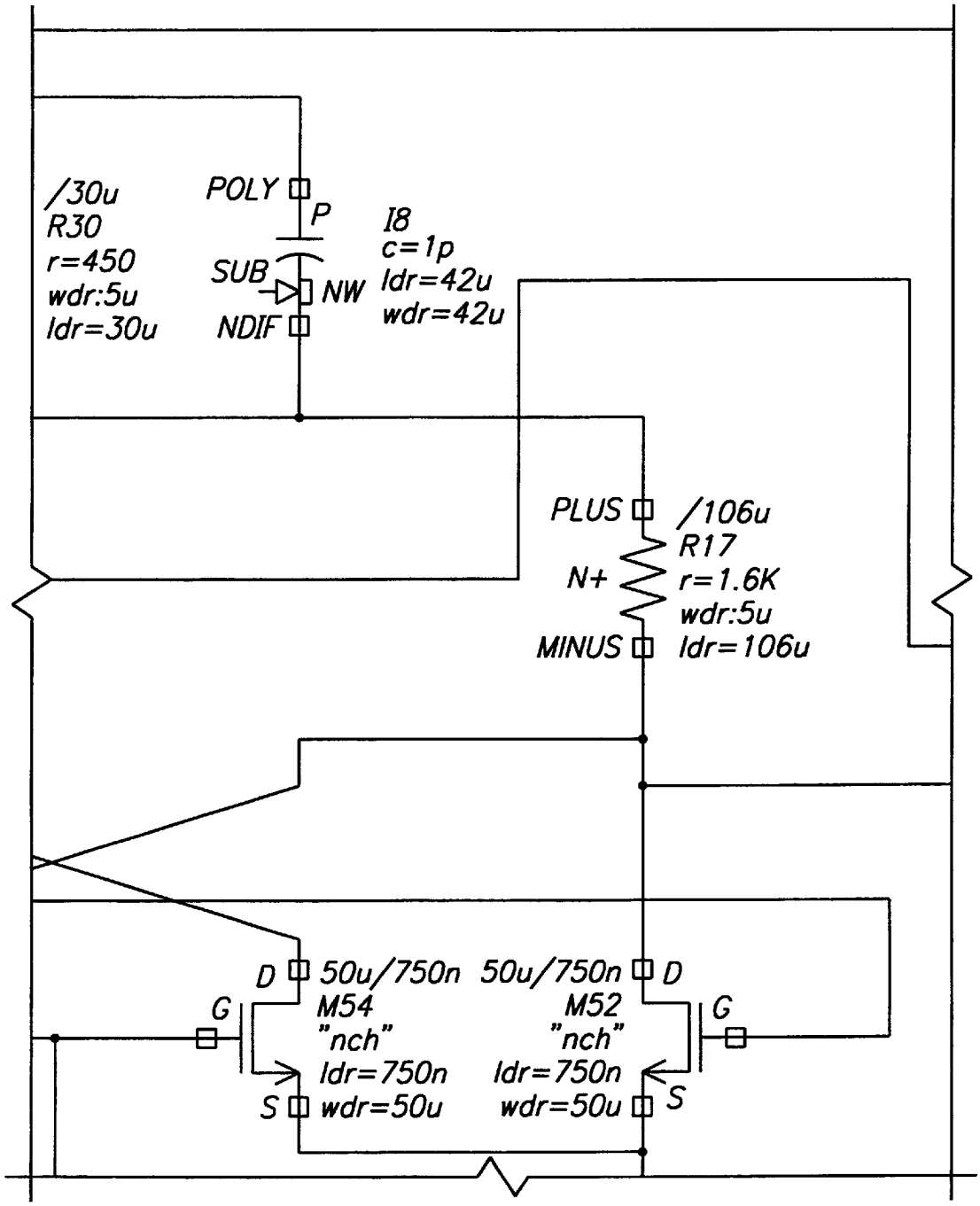


Fig 8.060502AC

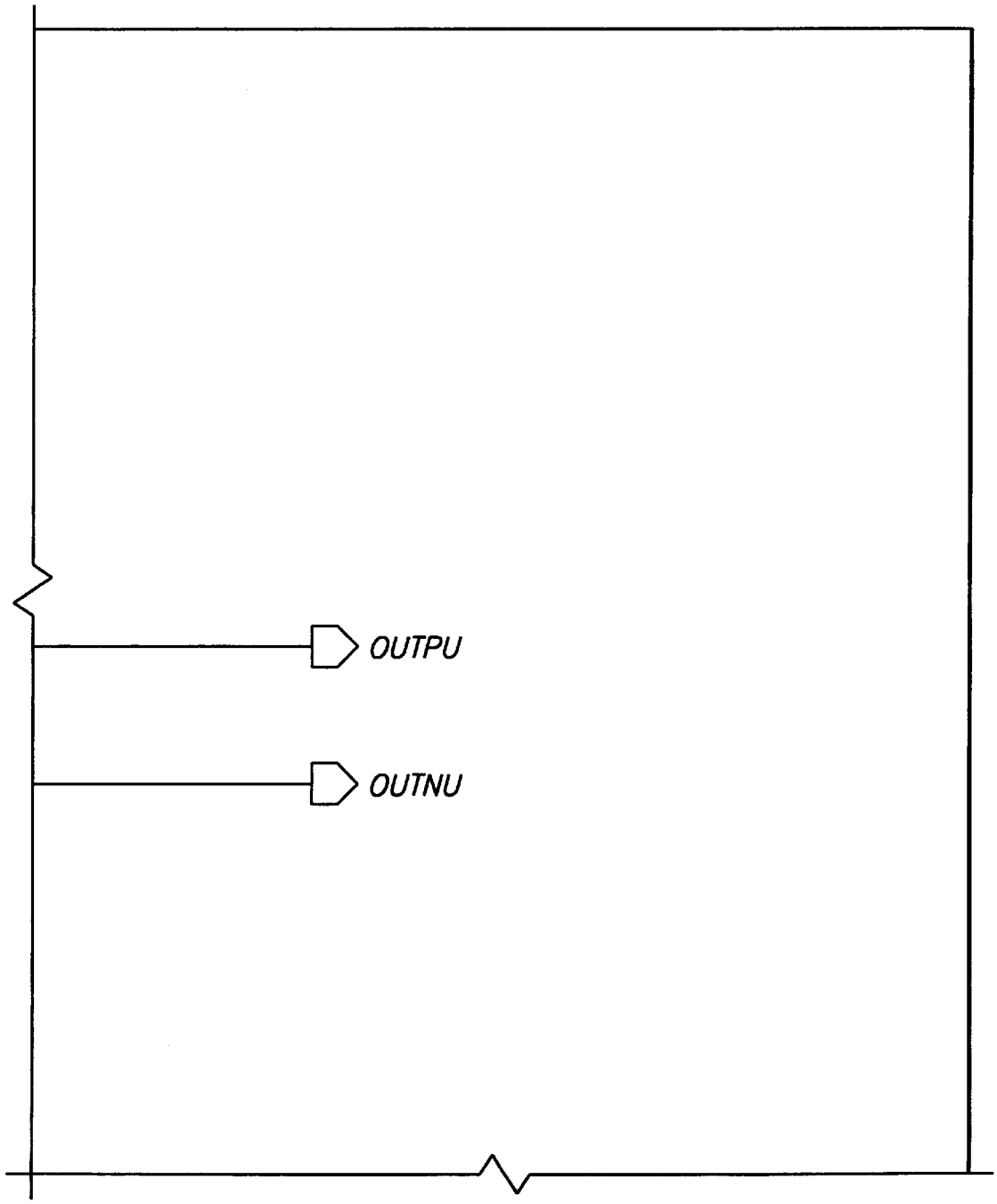


Fig 8.0605002AD

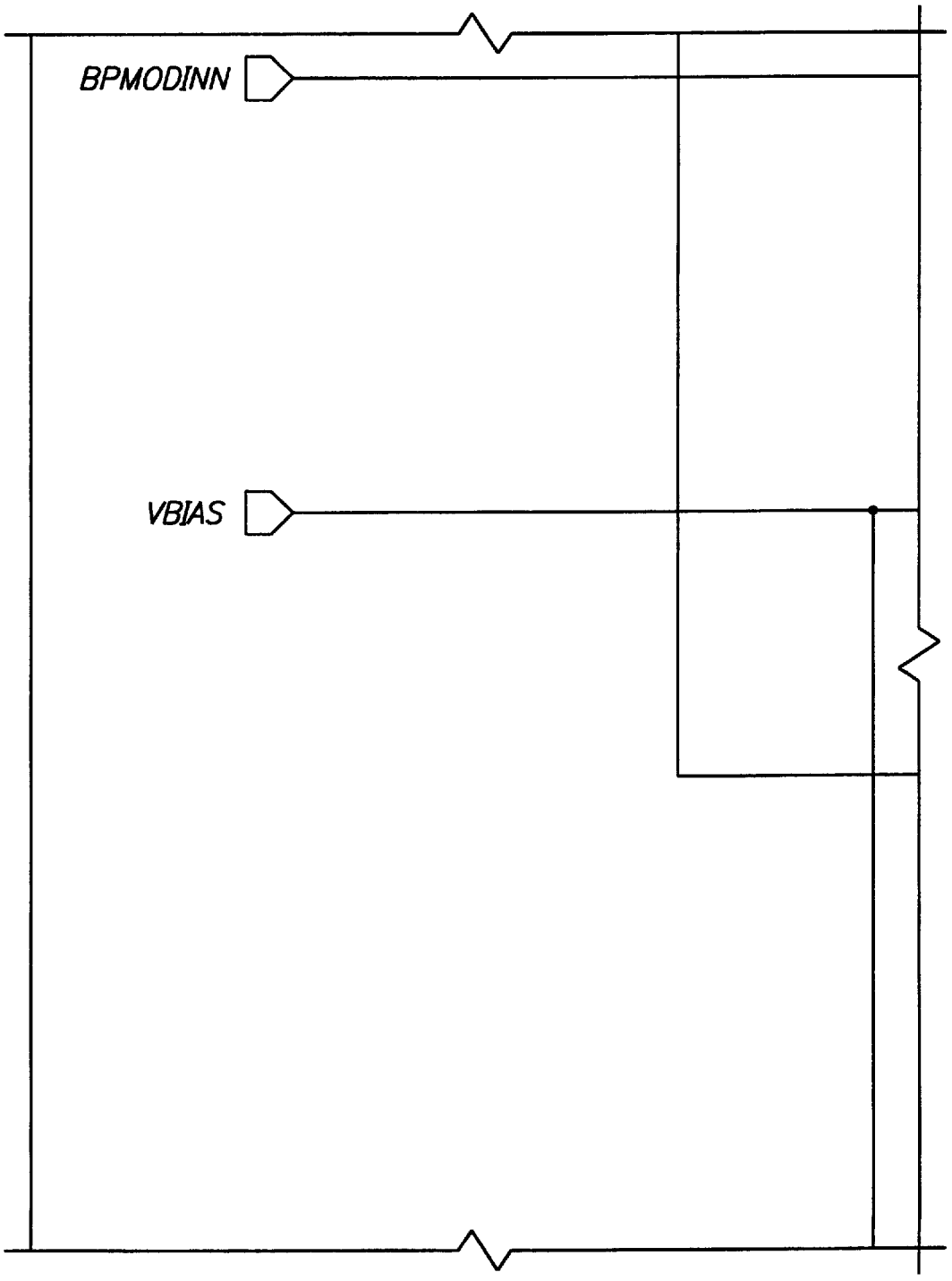


Fig 8.0605028A

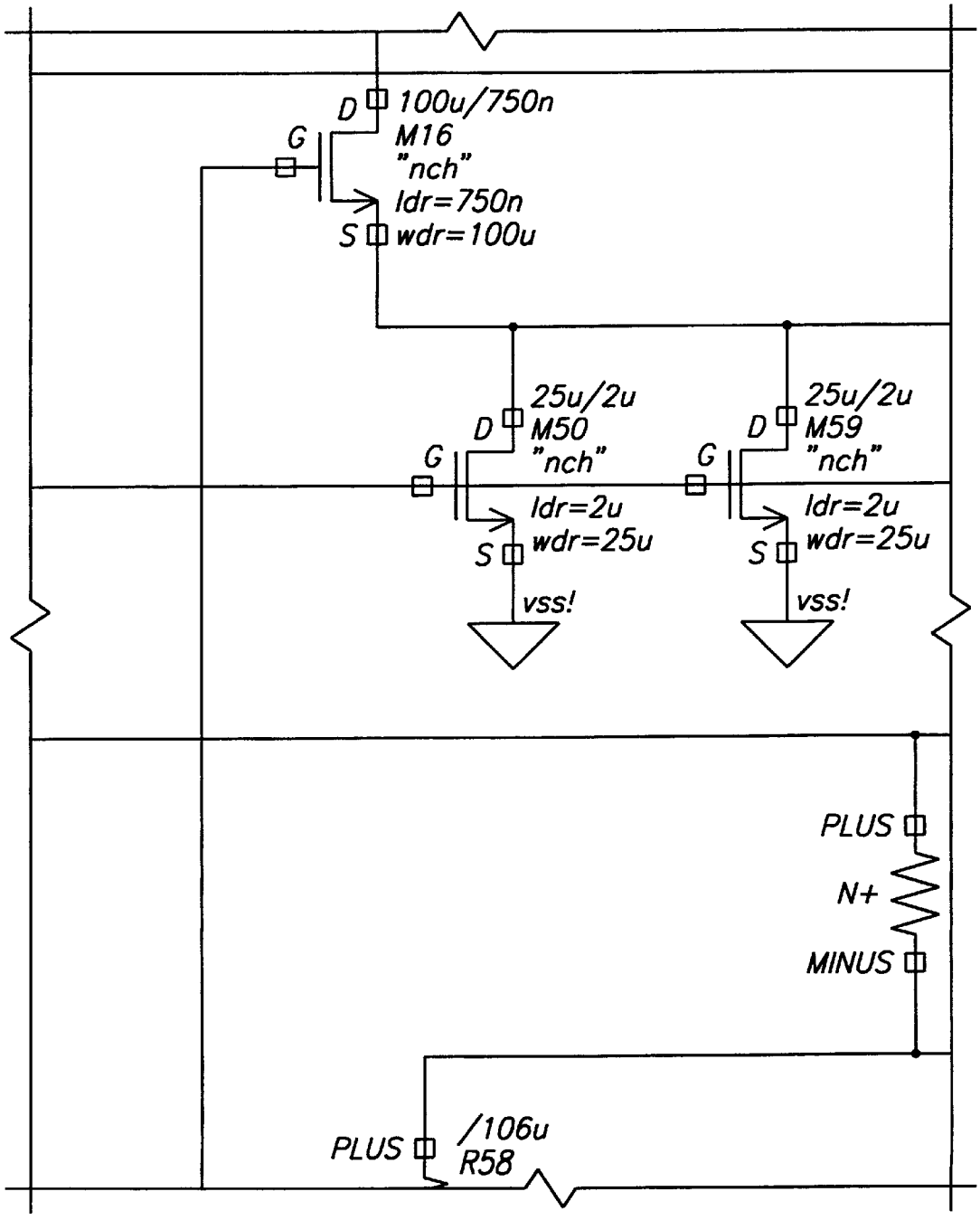


Fig 8,060,502BB

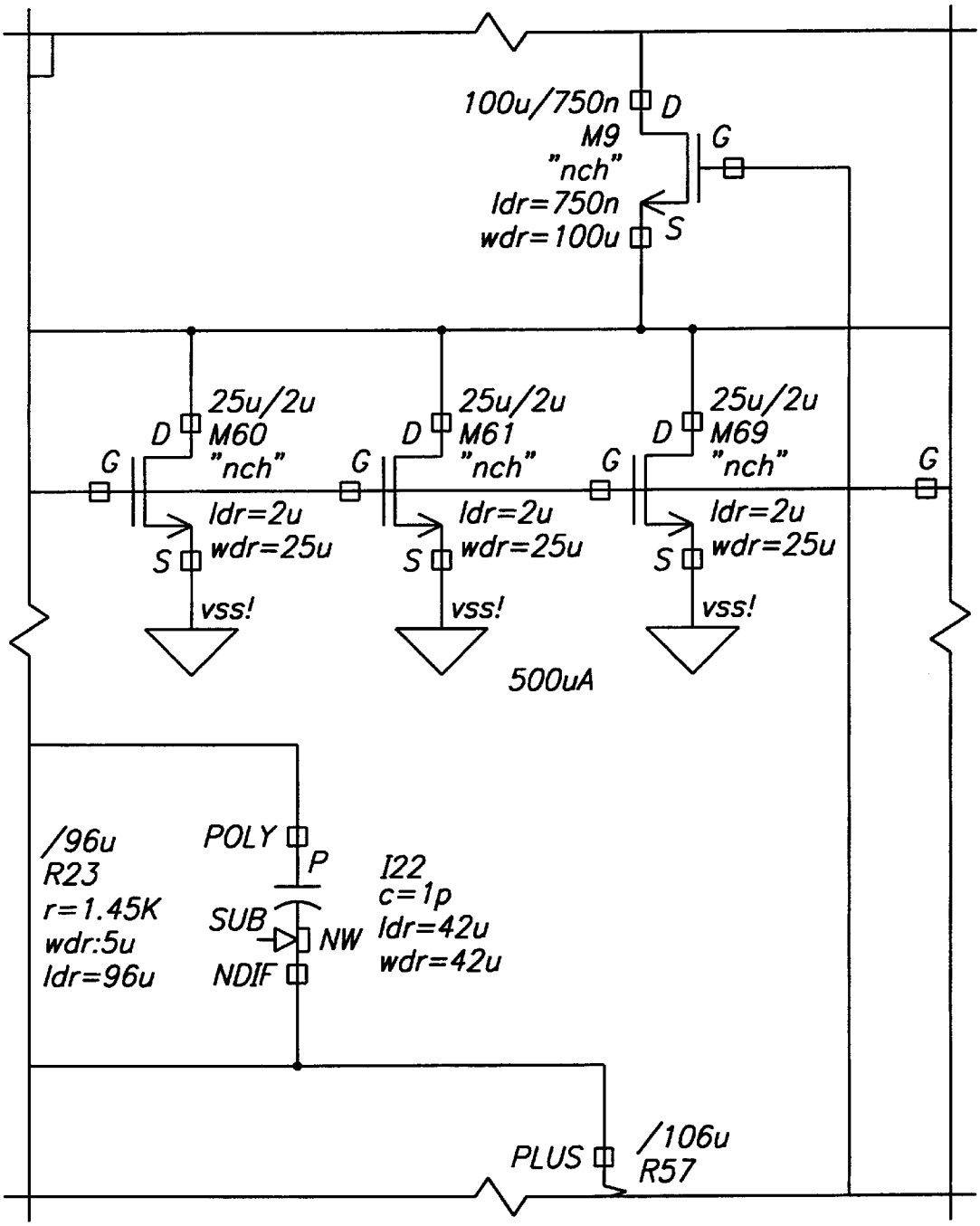


Fig 8.0605028C

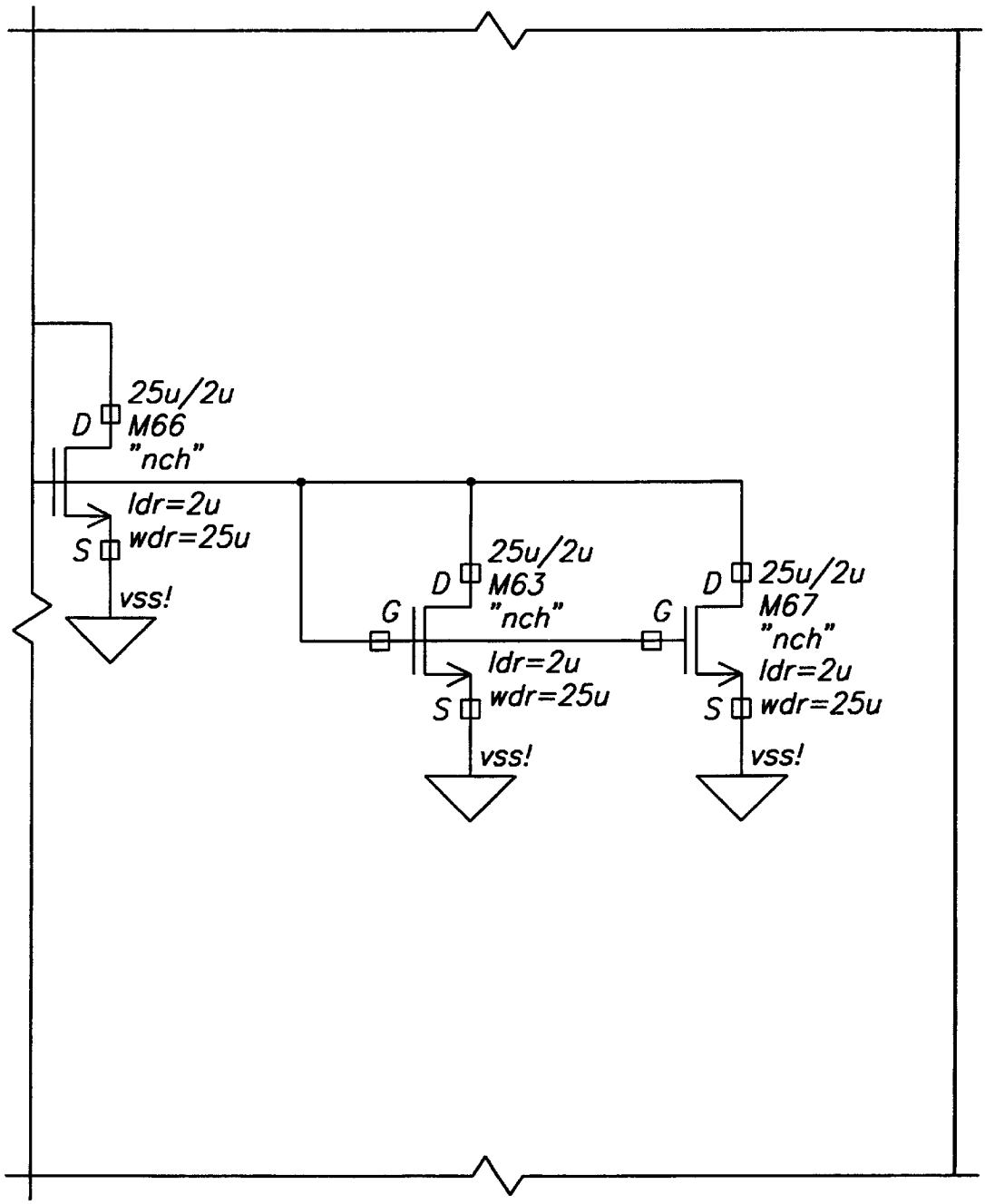


Fig 8.06050218D

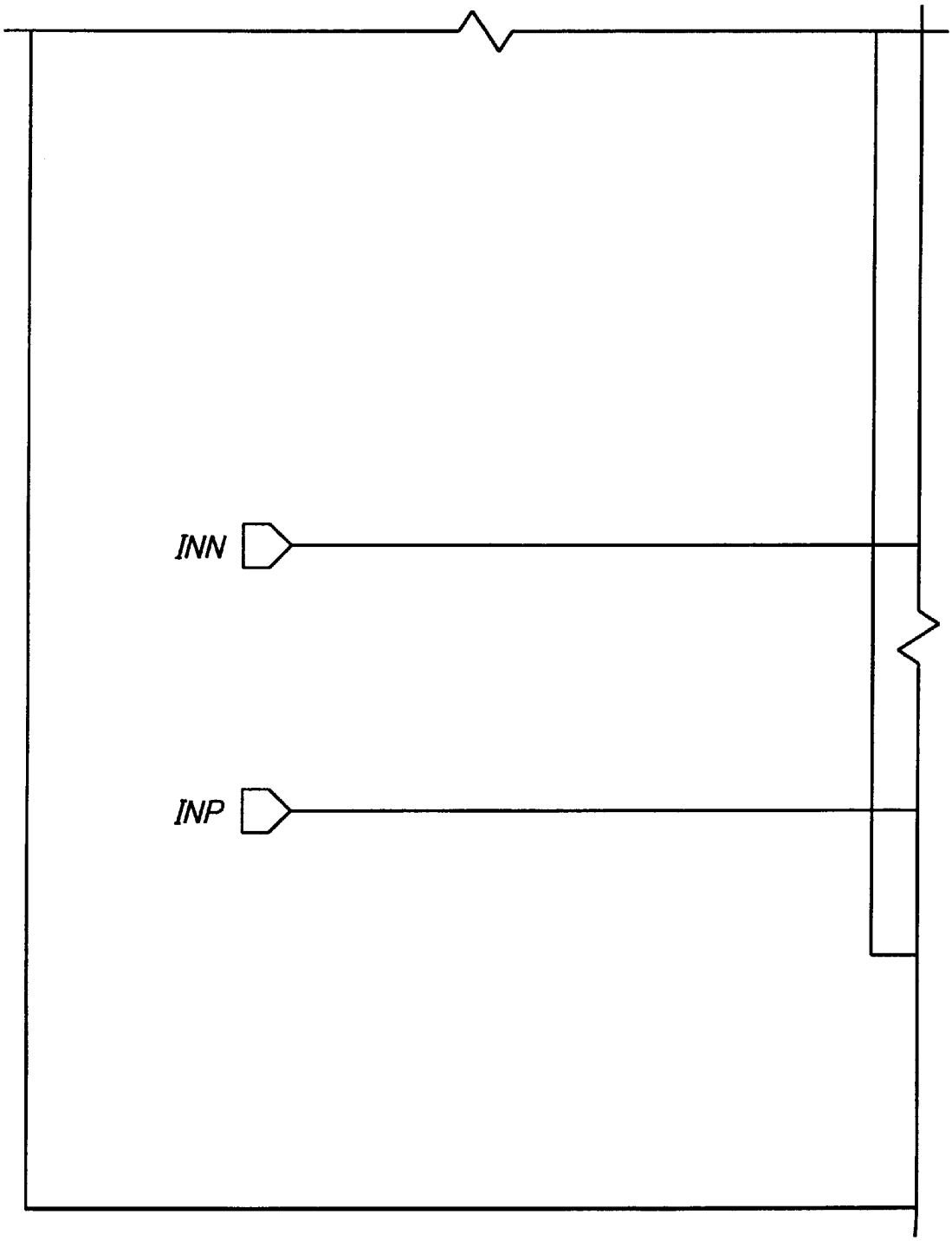


Fig 8.060502CA

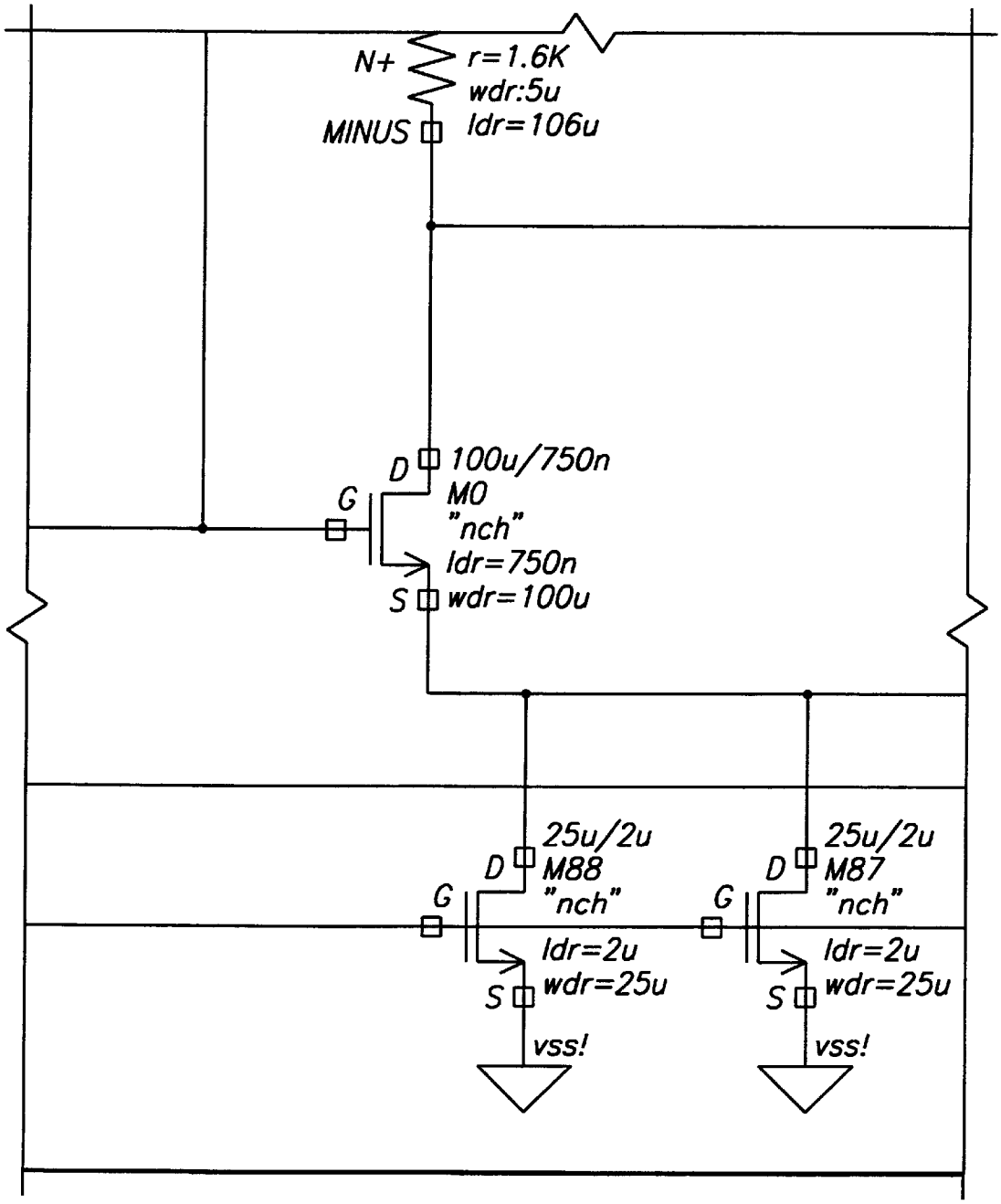


Fig 8,060,502CB

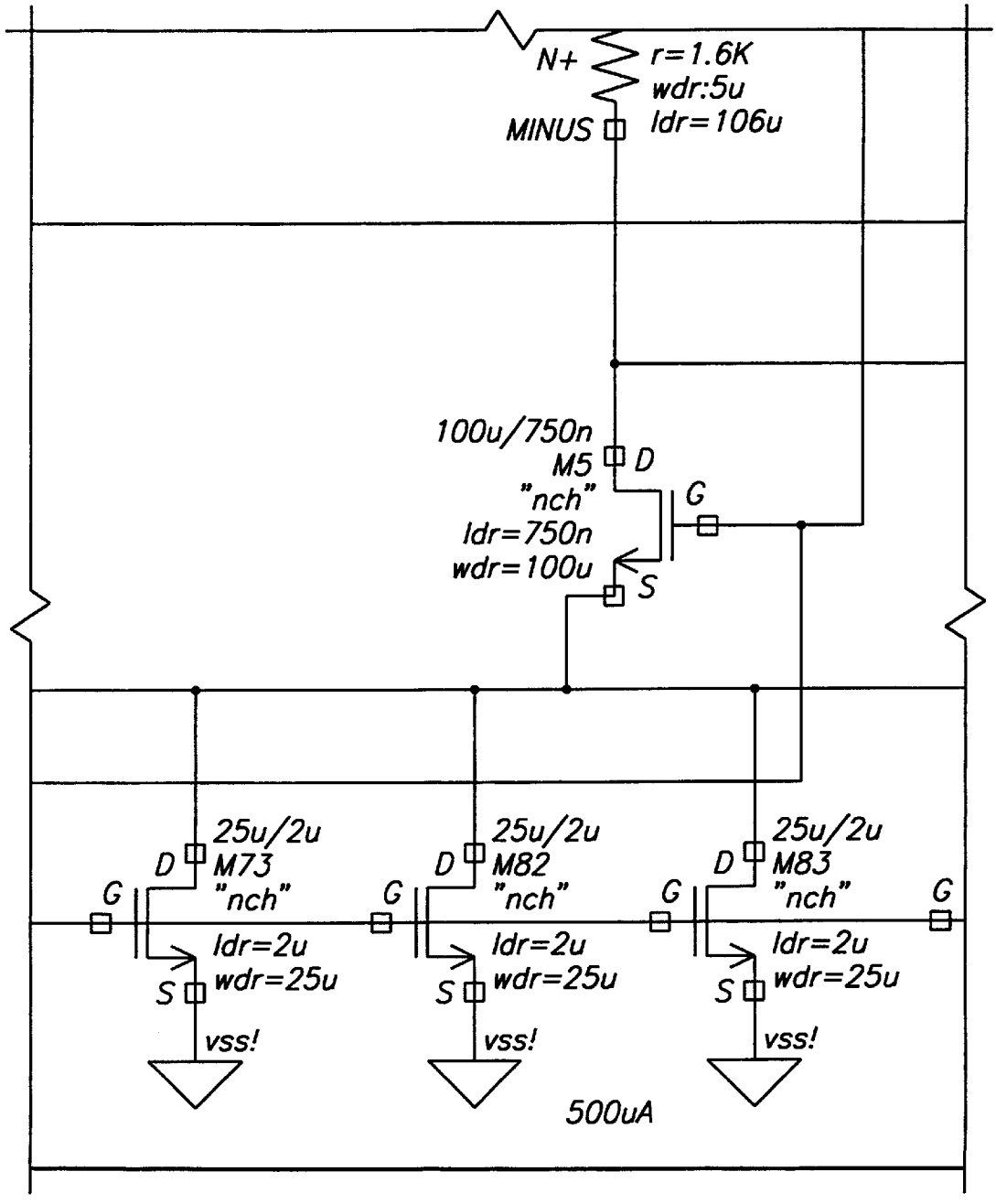


Fig 8,060,502CC

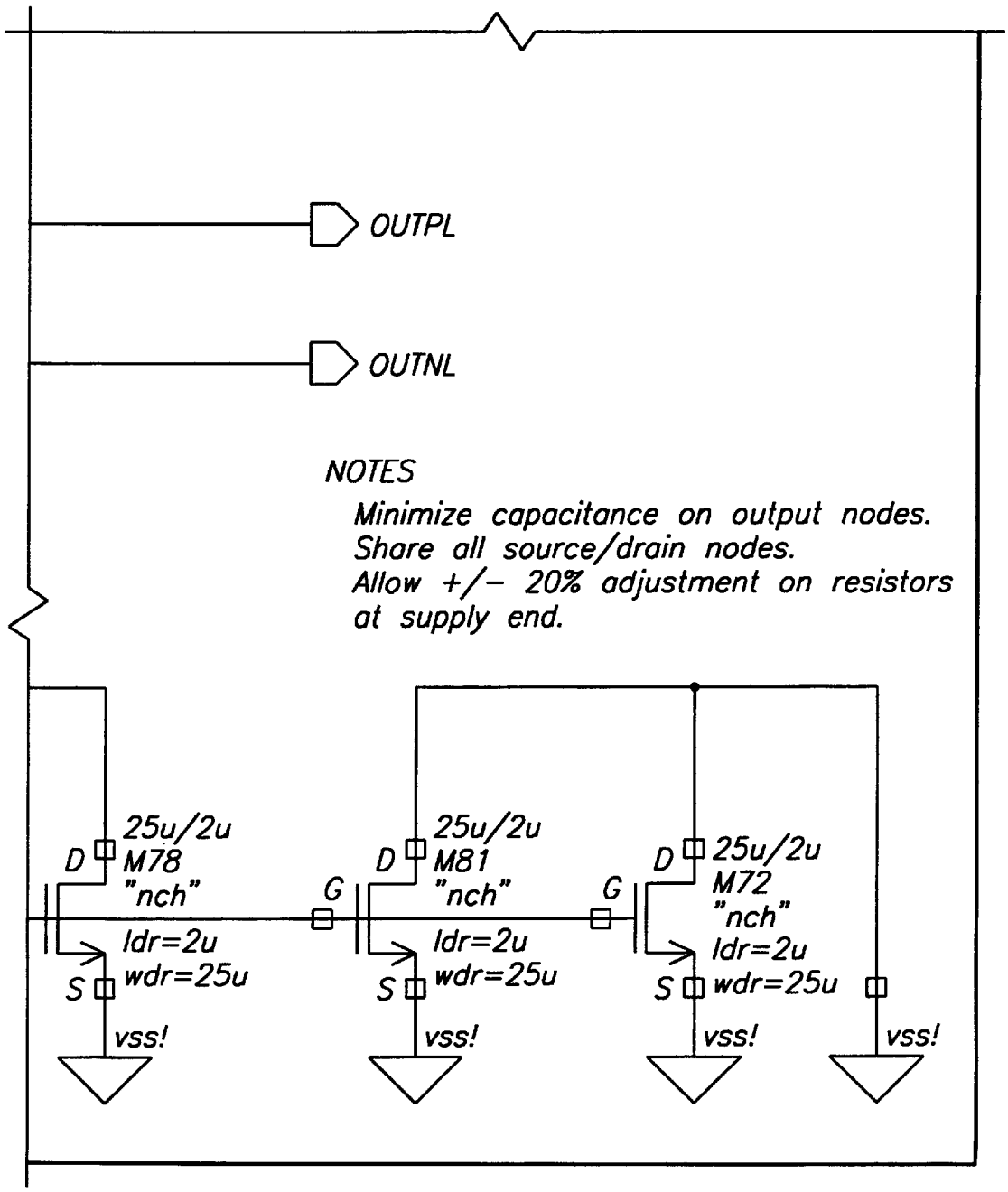
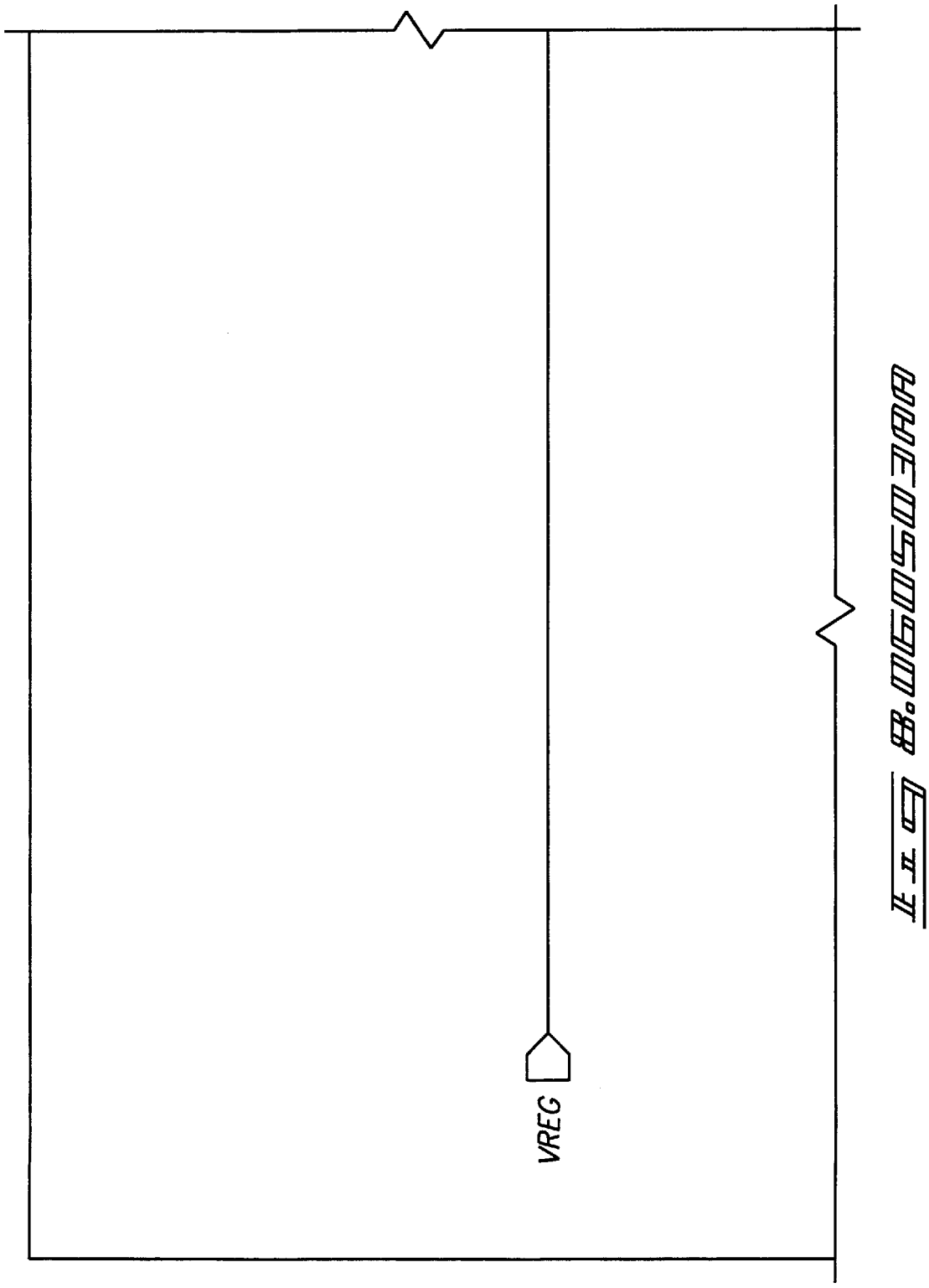


Fig 8.060502CD

8.060503AA	8.060503AB	8.060503AC	8.060503AD	8.060503AE
8.060503BA	8.060503BB	8.060503BC	8.060503BD	8.060503BE
8.060503CA	8.060503CB	8.060503CC	8.060503CD	8.060503CE
8.060503DA	8.060503DB	8.060503DC	8.060503DD	8.060503DE
8.060503EA	8.060503EB	8.060503EC	8.060503ED	8.060503EE
8.060503FA	8.060503FB	8.060503FC	8.060503FD	8.060503FE

FIG 8.060503


VREG
FIG. 88,005,004

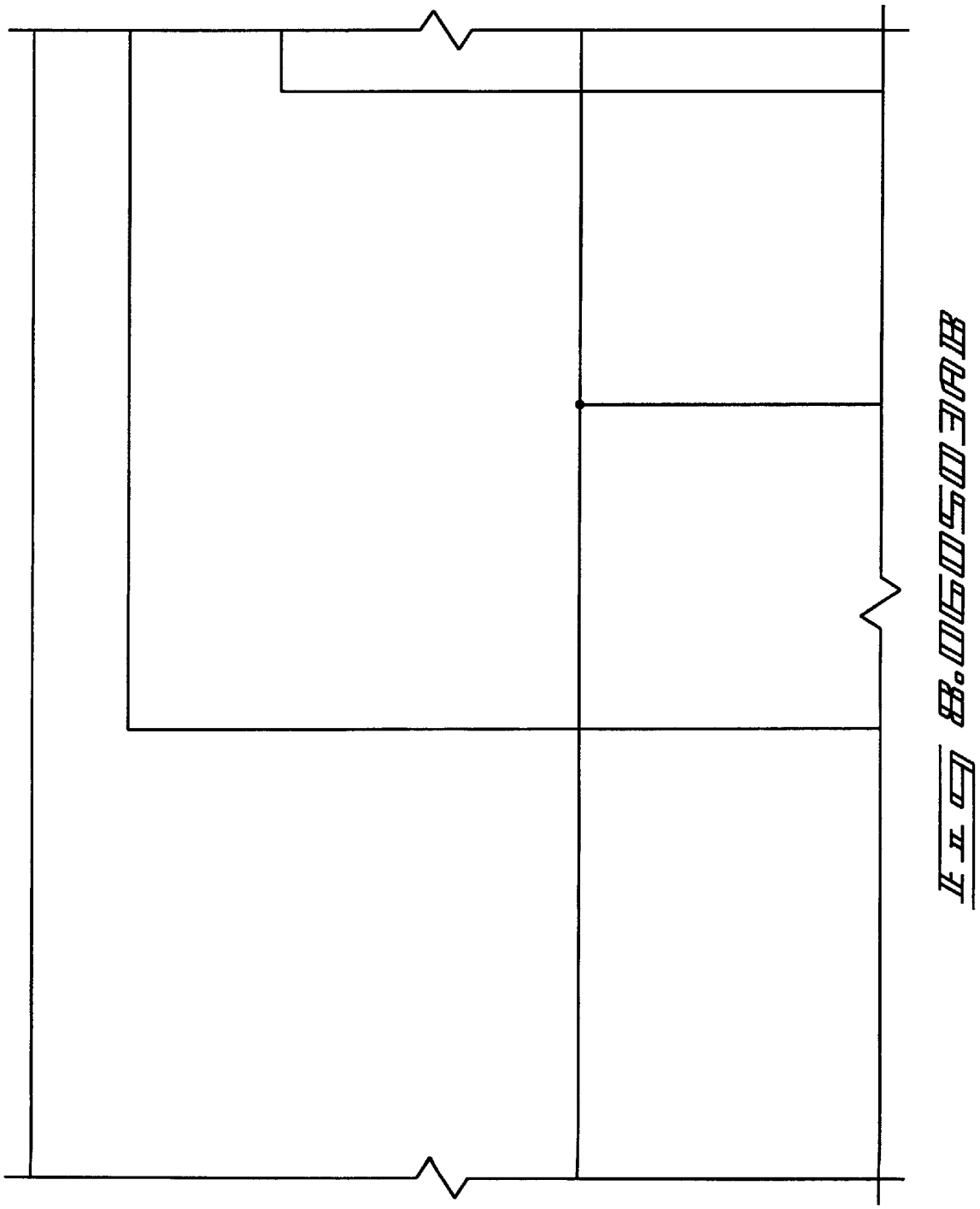


FIG. 88

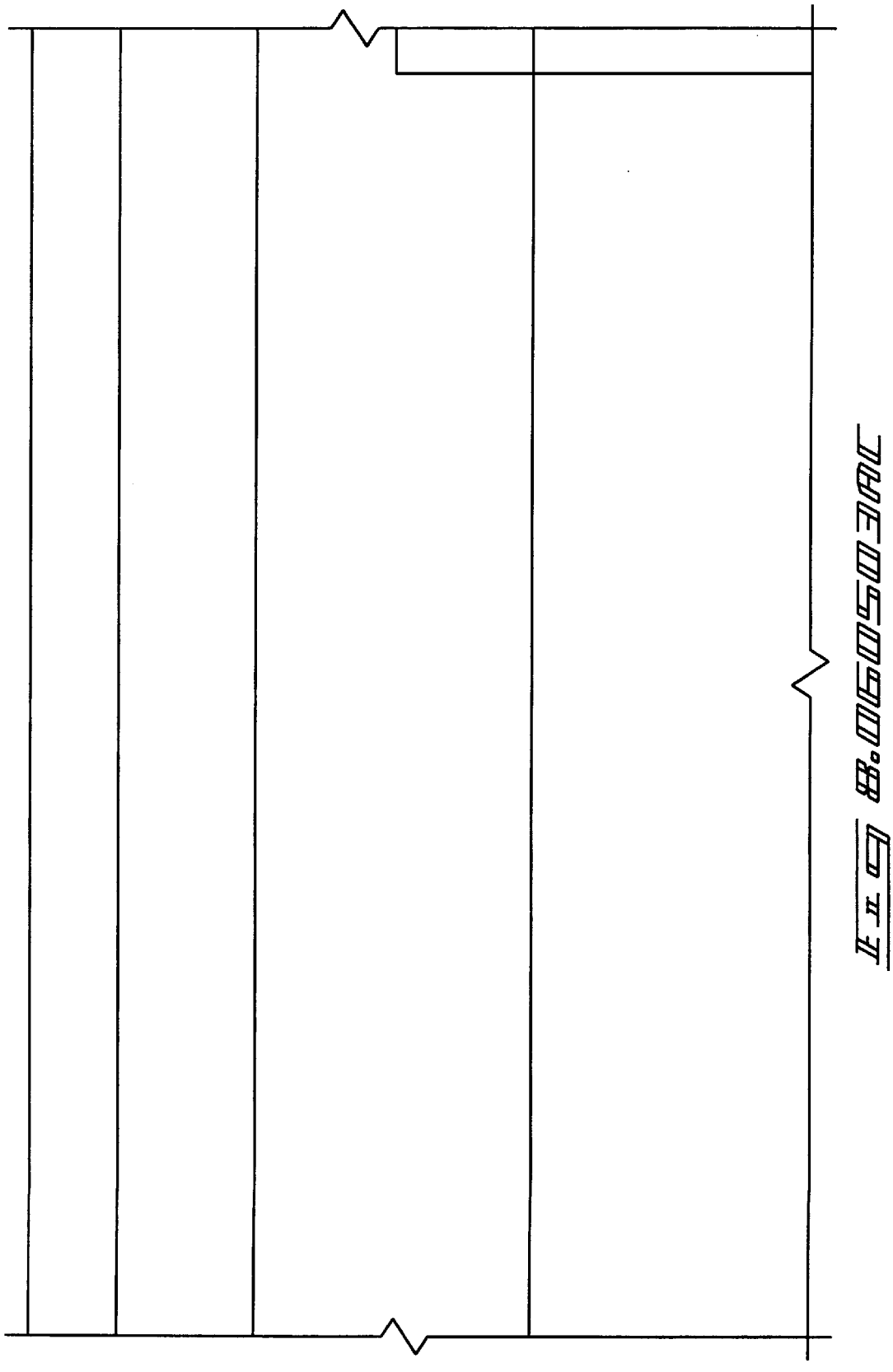


FIG. 88.0500.1997

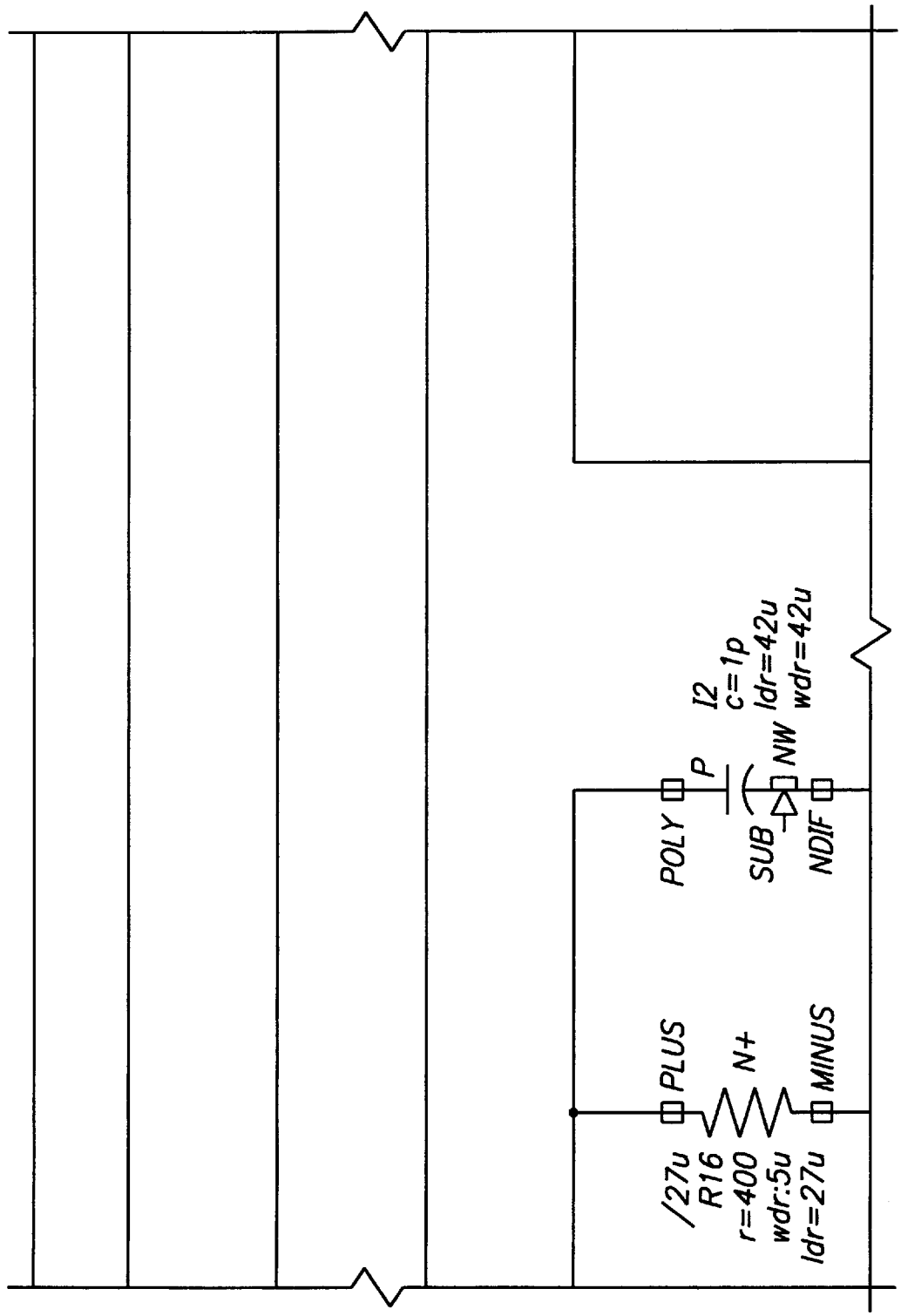
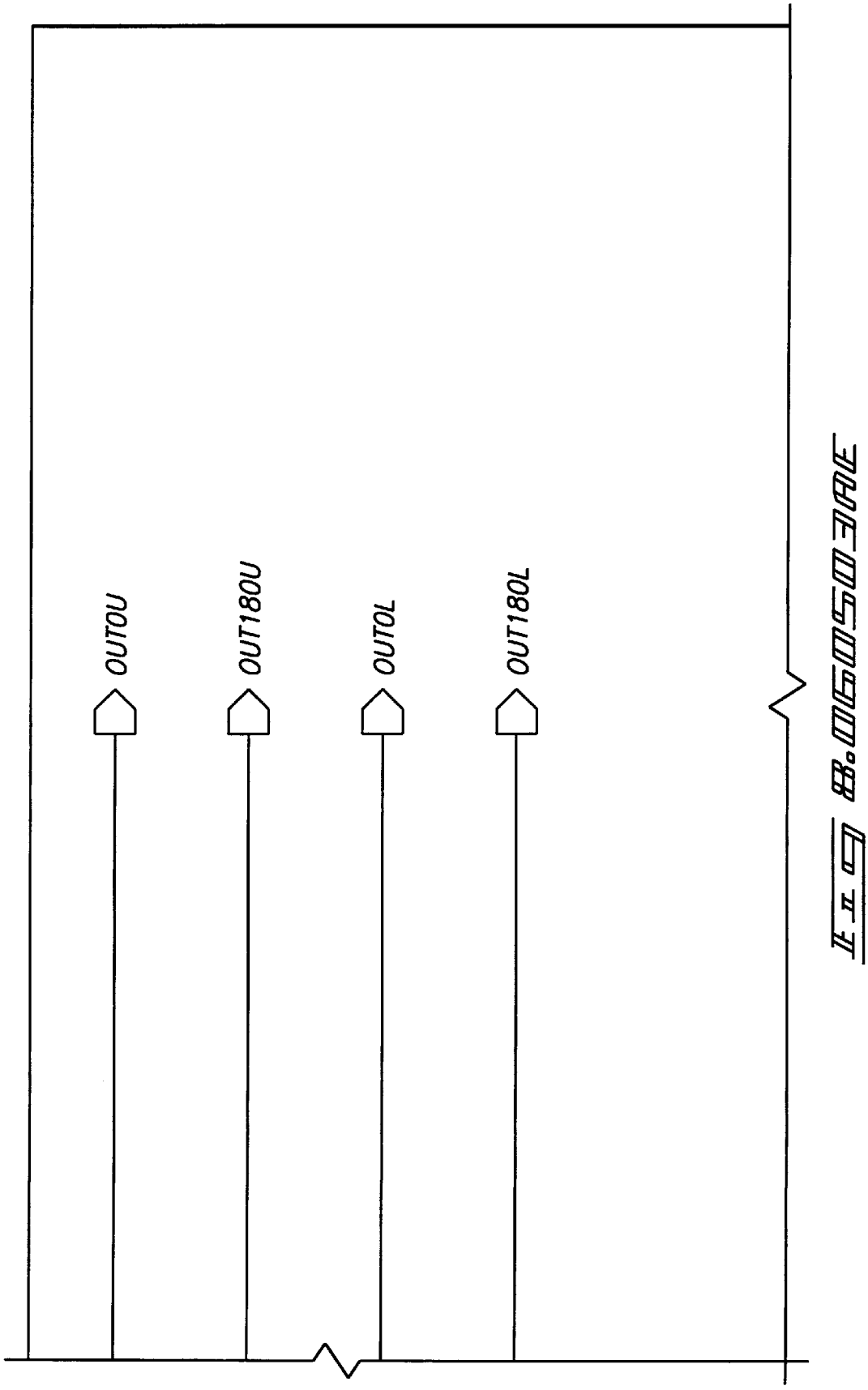

/27u
R16
r=400
wdr:5u
ldr=27u
PLUS
N+
MINUS
POLY
P
SUB
NW
NDIF
I2
c=1p
ldr=42u
wdr=42u

FIG 8,050,000


OUT0U
OUT180U
OUT0L
OUT180L
FIG 88,005,003 PAGE

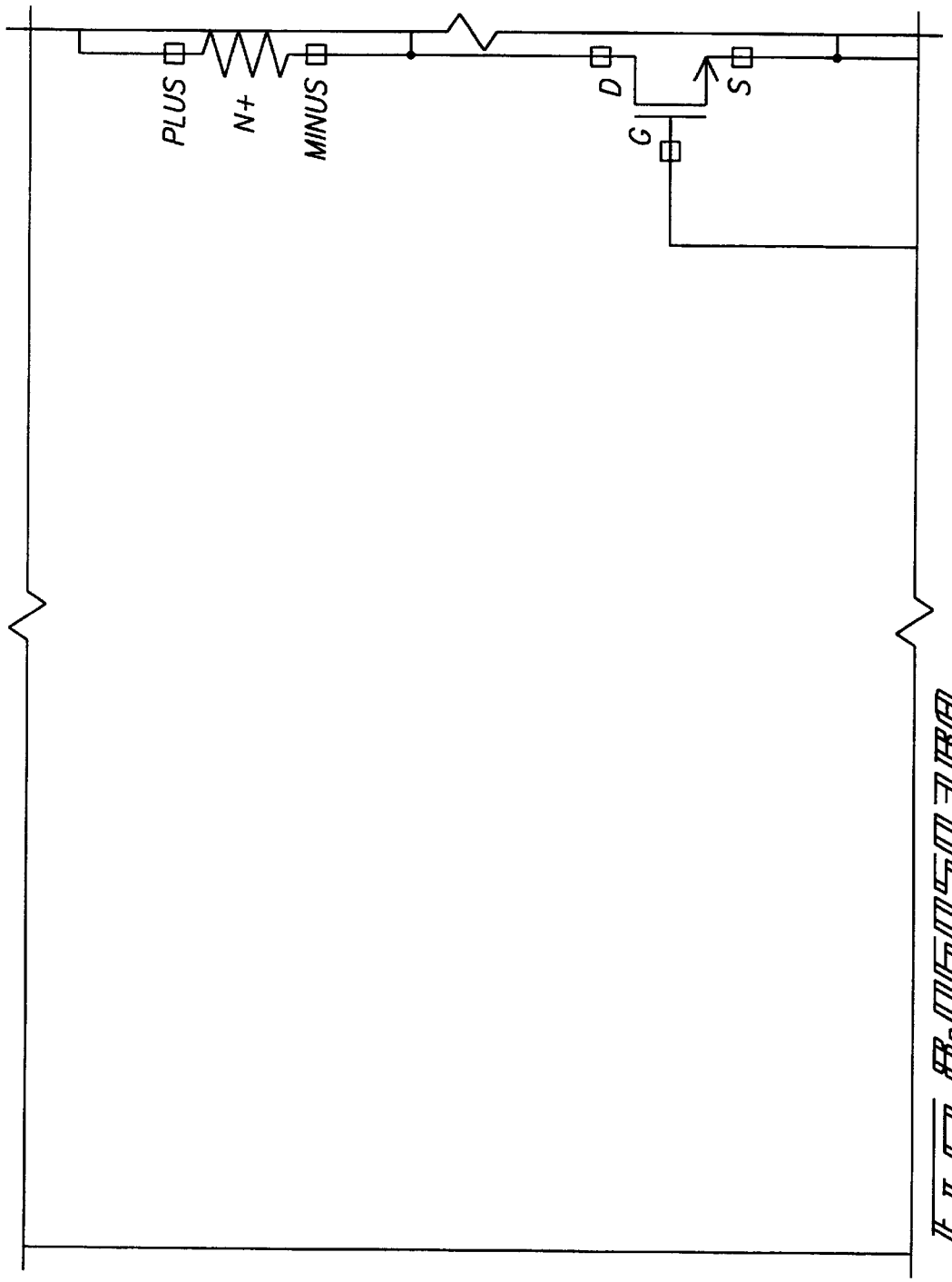


FIG 6,130,602

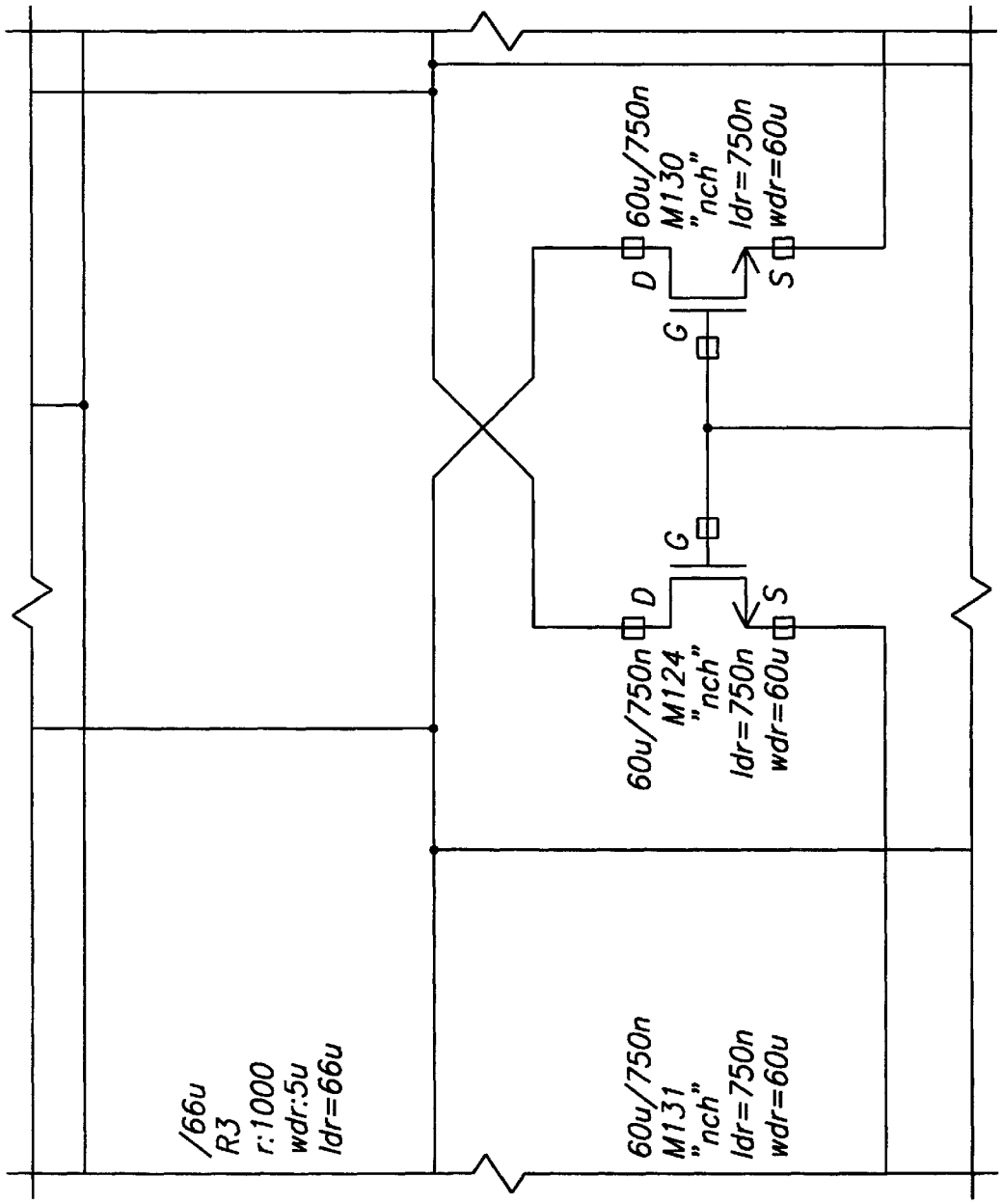

60u/750n
M130
"nch"
ldr=750n
wdr=60u
D
G
S
60u/750n
M124
"nch"
ldr=750n
wdr=60u
/66u
R3
r:1000
wdr:5u
ldr=66u
60u/750n
M131
"nch"
ldr=750n
wdr=60u

Fig. 8,005,003

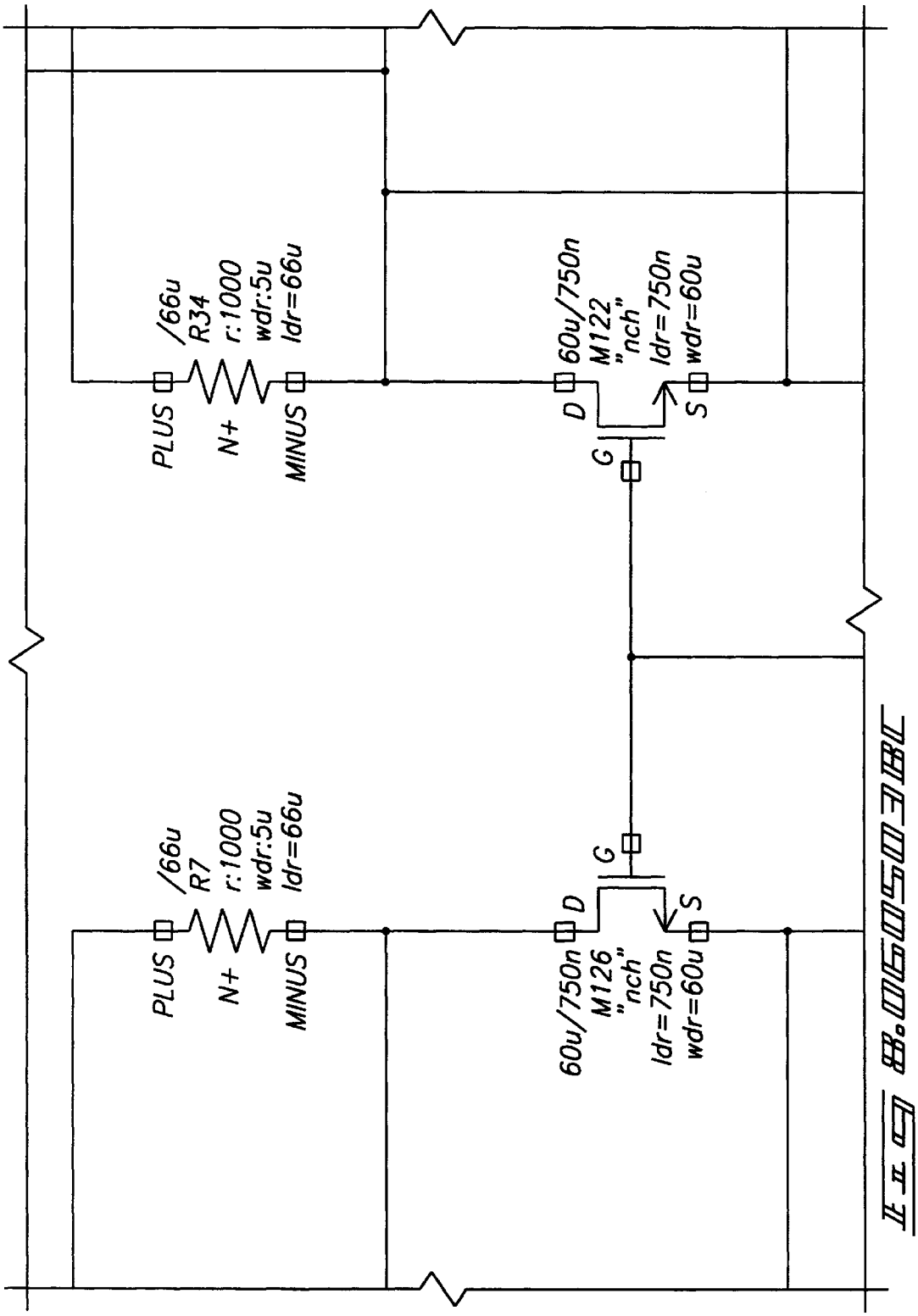
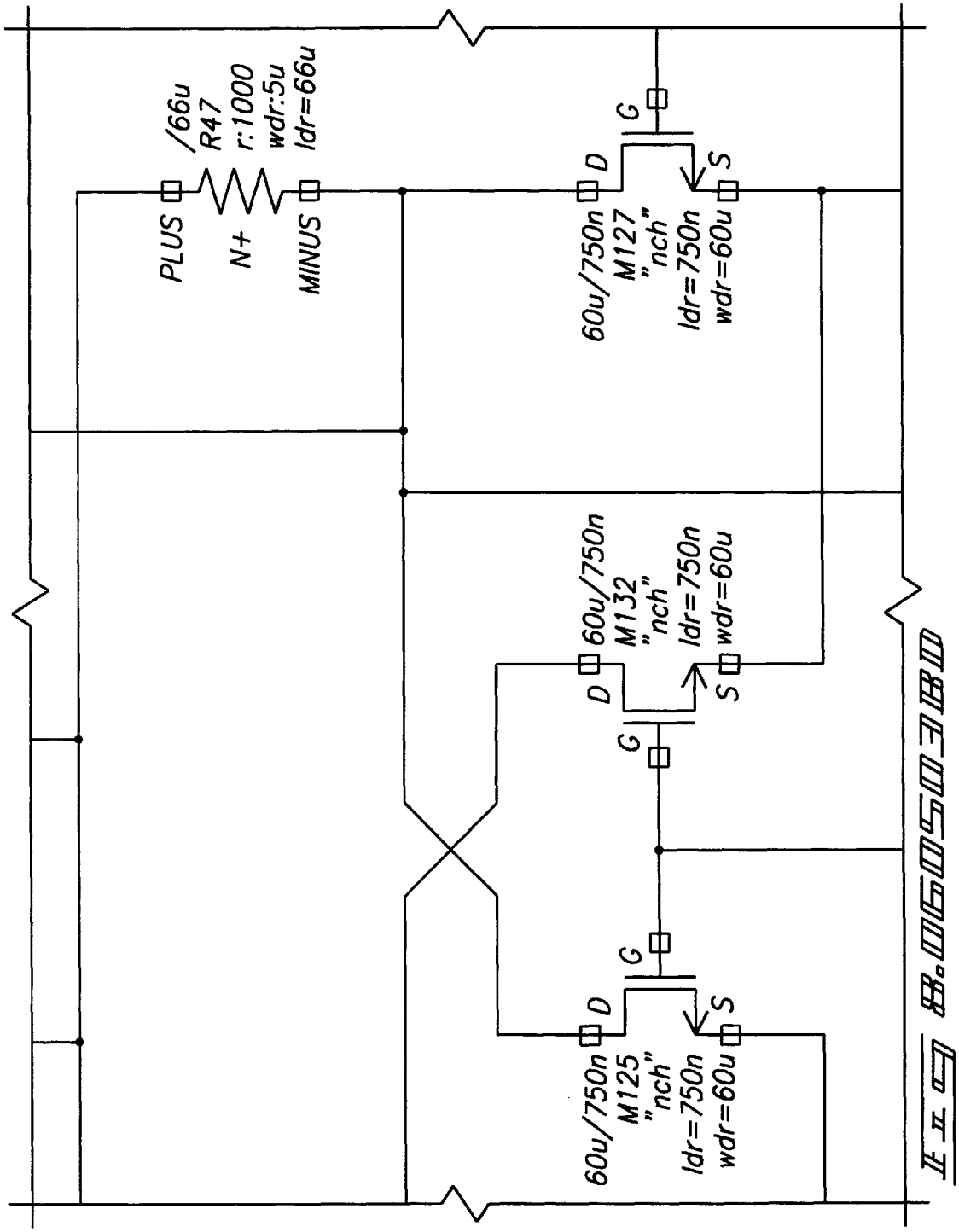

/66u
R34
r:1000
wdr:5u
ldr=66u
PLUS
N+
MINUS
60u/750n
M122
"nch"
ldr=750n
wdr=60u
D
G
S
/66u
R7
r:1000
wdr:5u
ldr=66u
PLUS
N+
MINUS
60u/750n
M126
"nch"
ldr=750n
wdr=60u
D
G
S

Fig. 8,005,005


/66u
R47
r:1000
wdr:5u
ldr=66u
PLUS
N+
MINUS
G
D
S
60u/750n
M127
"nch"
ldr=750n
wdr=60u
60u/750n
M132
"nch"
ldr=750n
wdr=60u
60u/750n
M125
"nch"
ldr=750n
wdr=60u

Фиг. 8,050,900

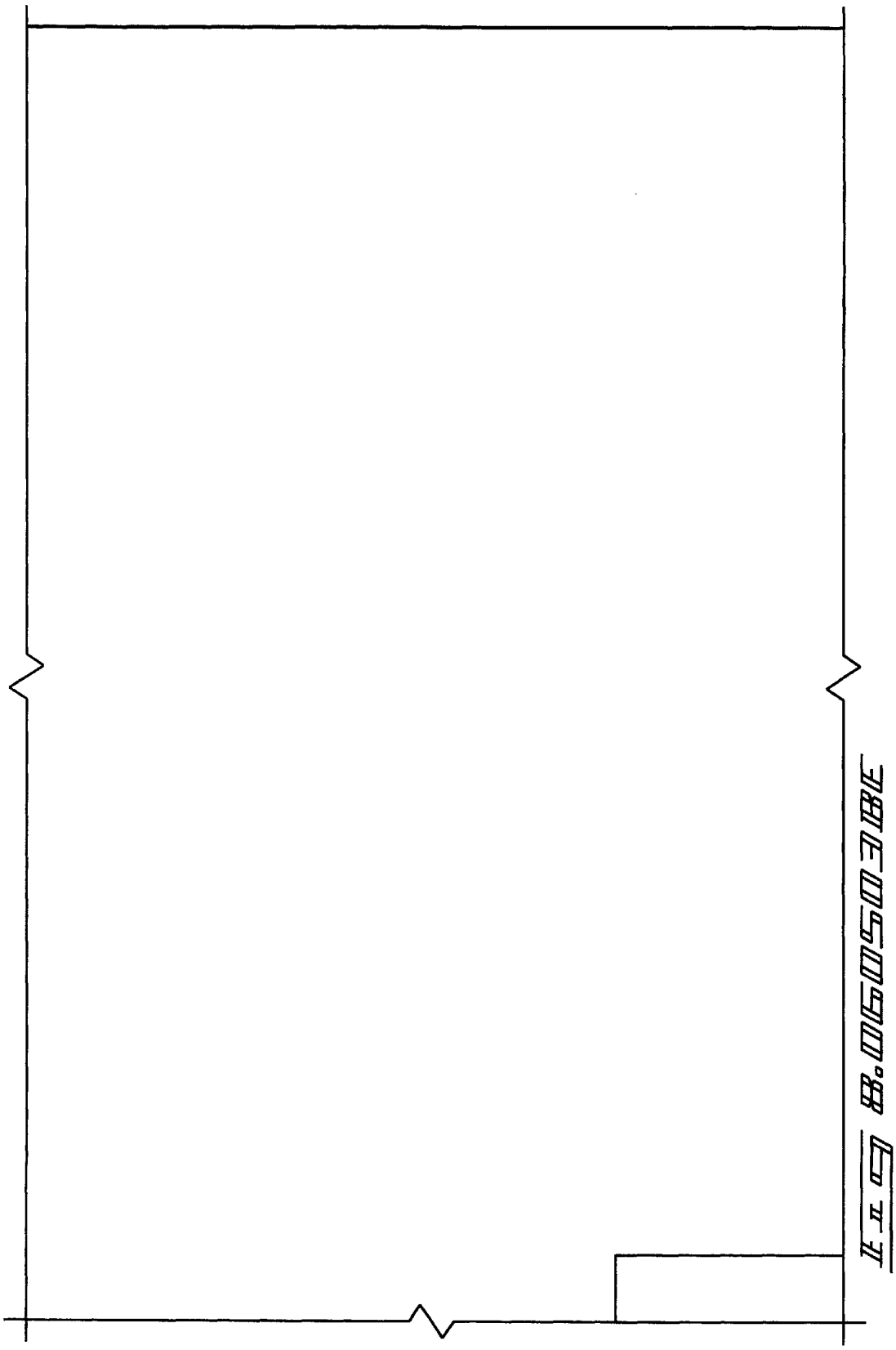
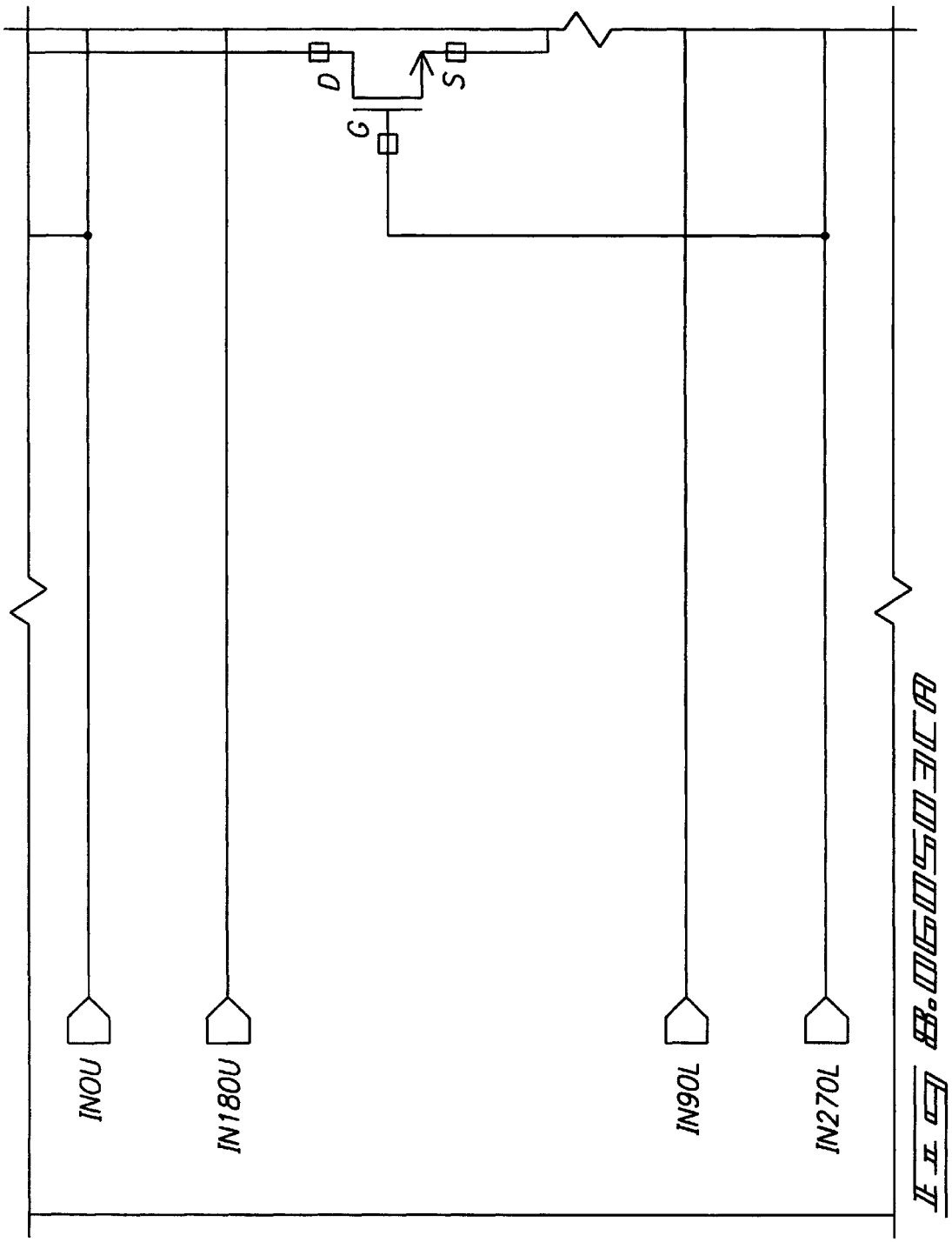


FIG 8.005ME


D
S
G
IN0U
IN180U
IN90L
IN270L

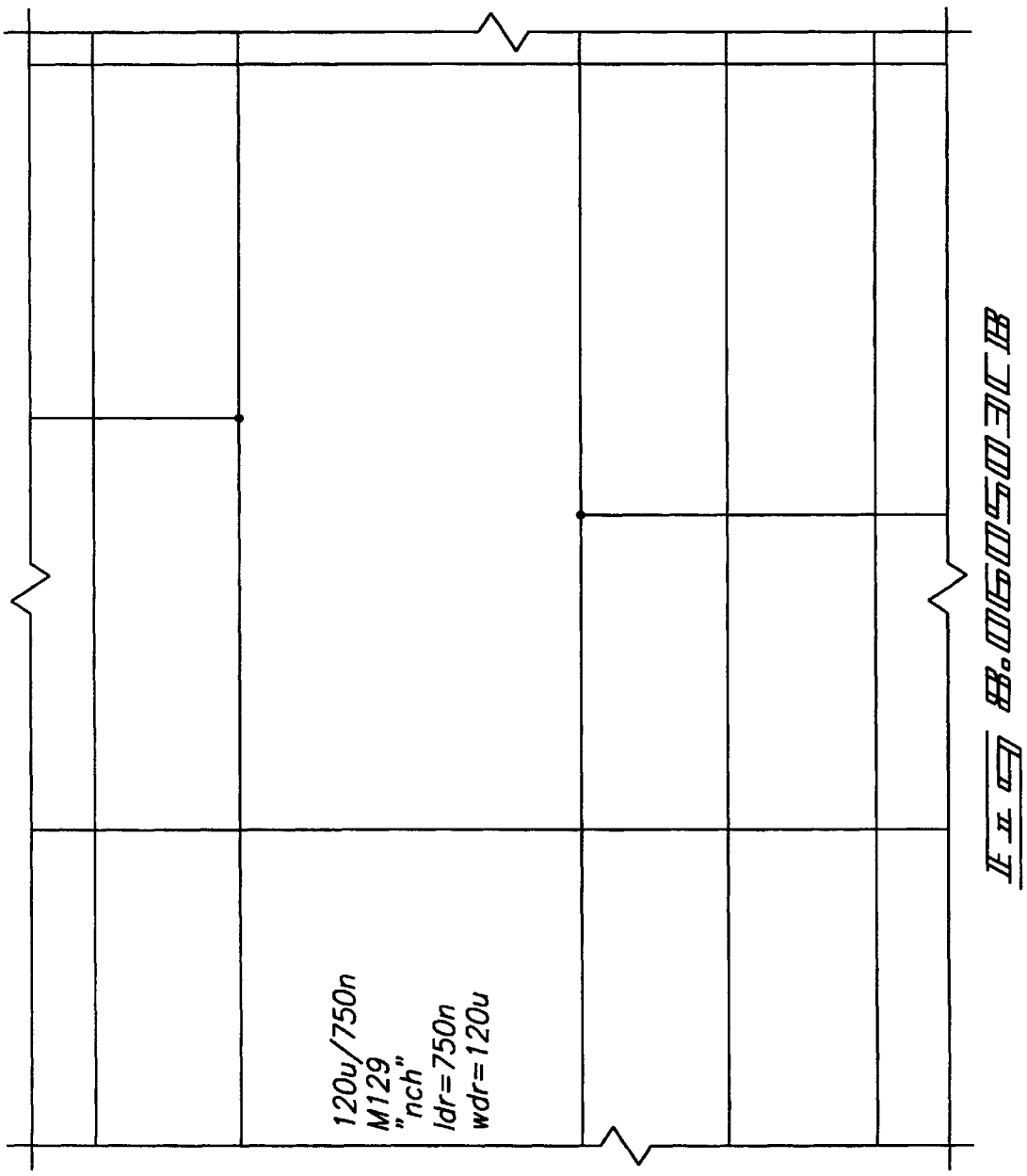


FIG 858
120u/750n
M129
"nch"
ldr=750n
wdr=120u

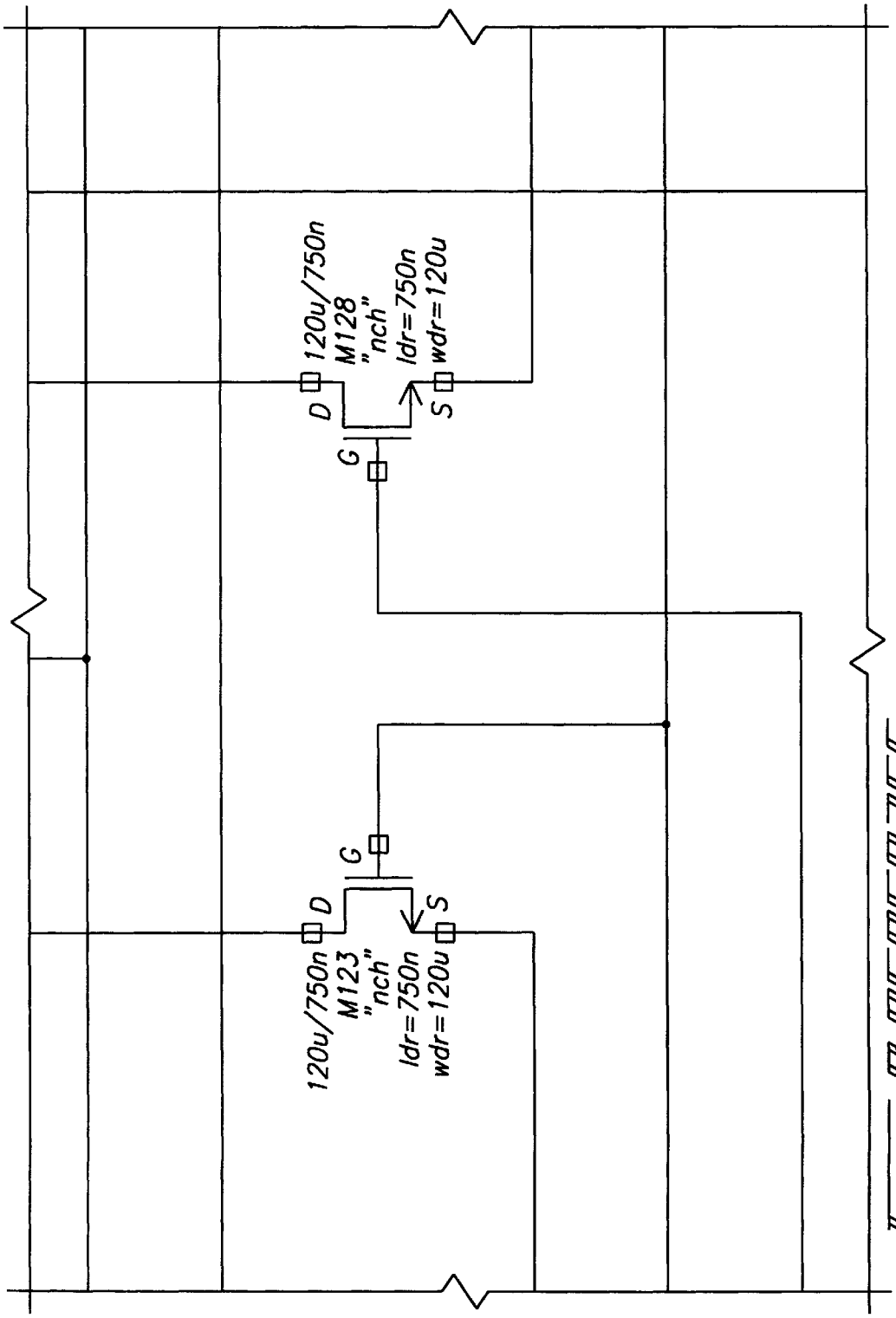
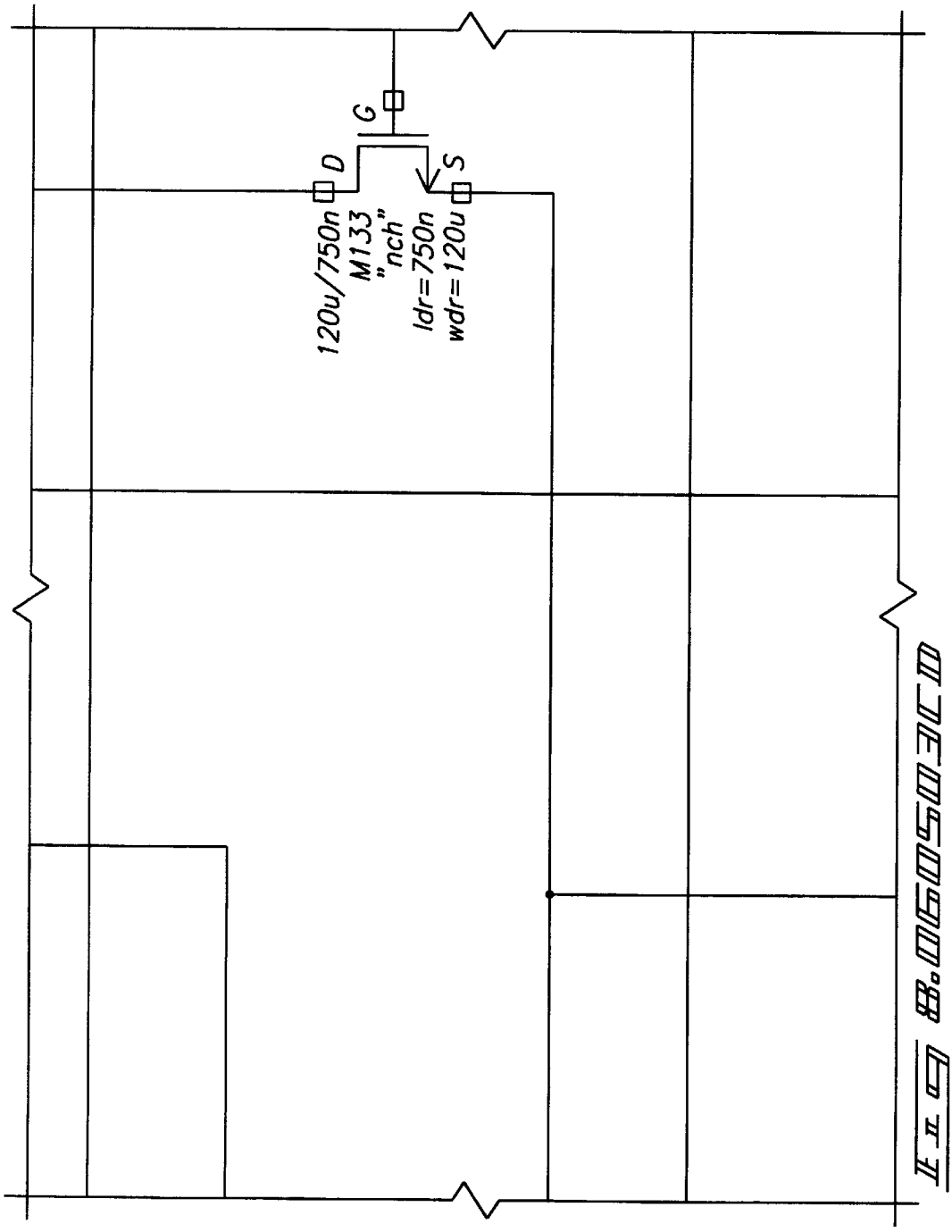


Fig 68,050,008


G
D
S
120u/750n
M133
"nch"
ldr=750n
wdr=120u
FIG. 8,050,900

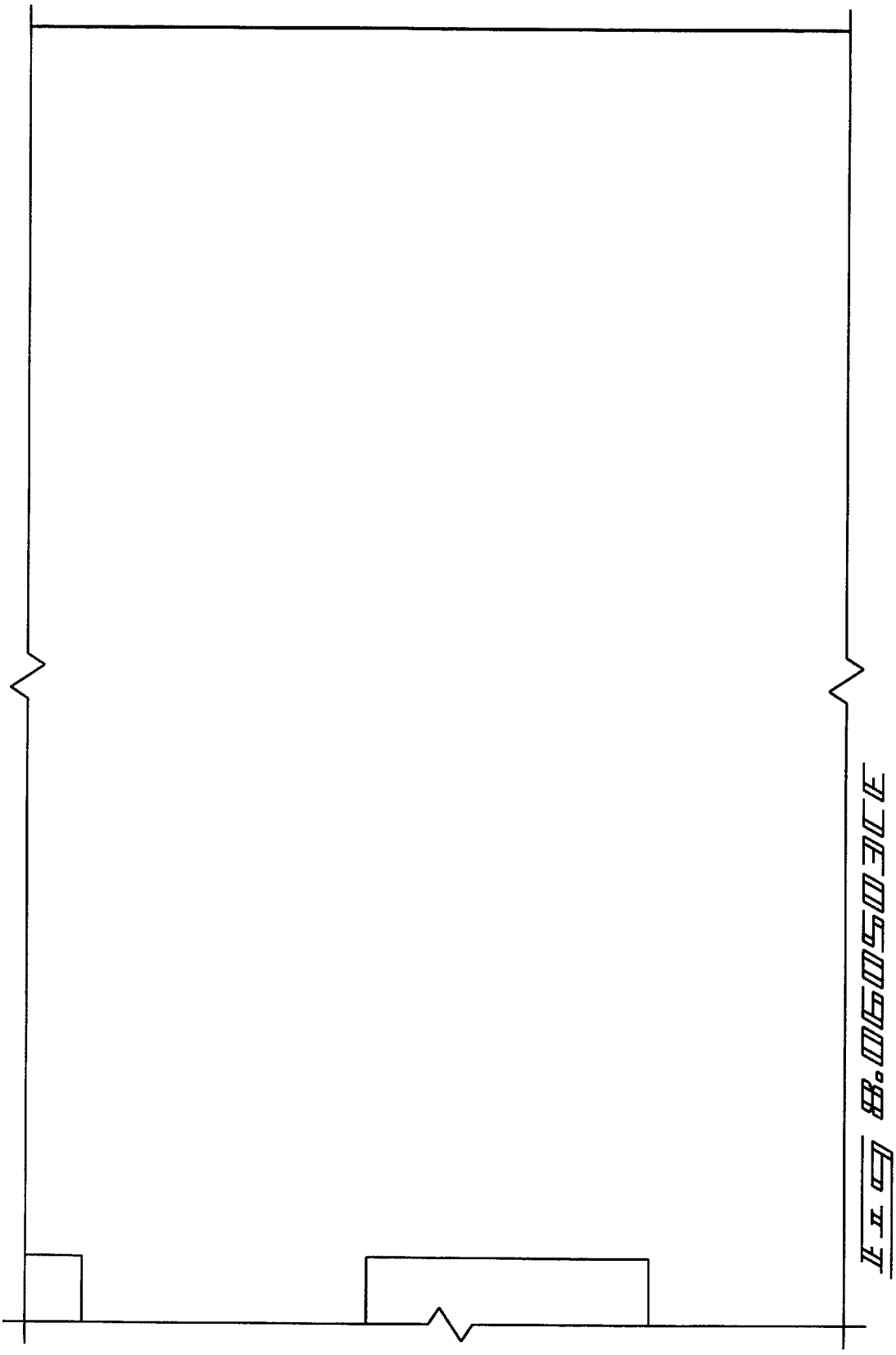
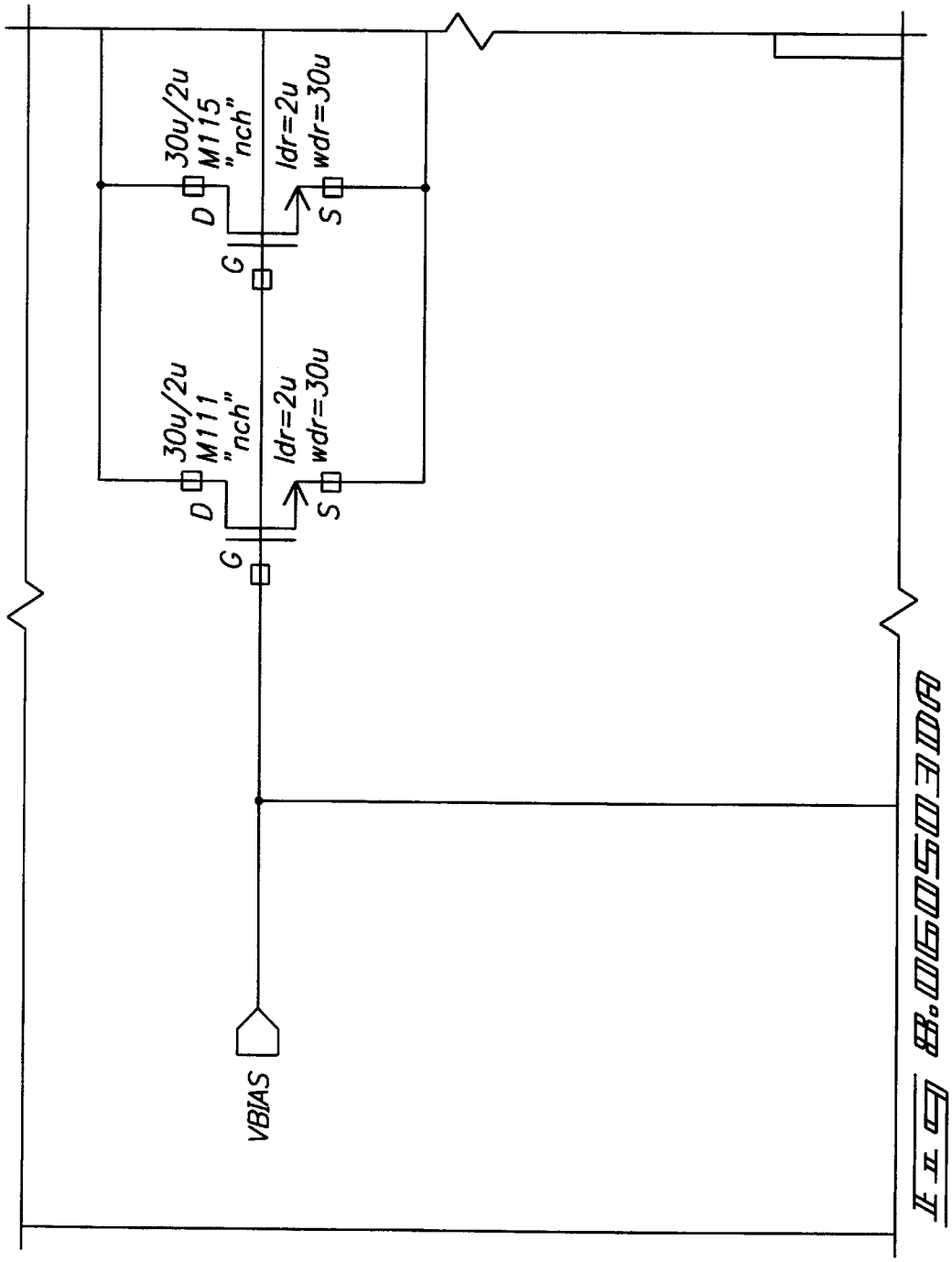


FIG 88.06500E


30u/2u
M115
"nch"
ldr=2u
wdr=30u
D
S
G
30u/2u
M111
"nch"
ldr=2u
wdr=30u
D
S
G
VBIAS

Фиг. 8.0050.8

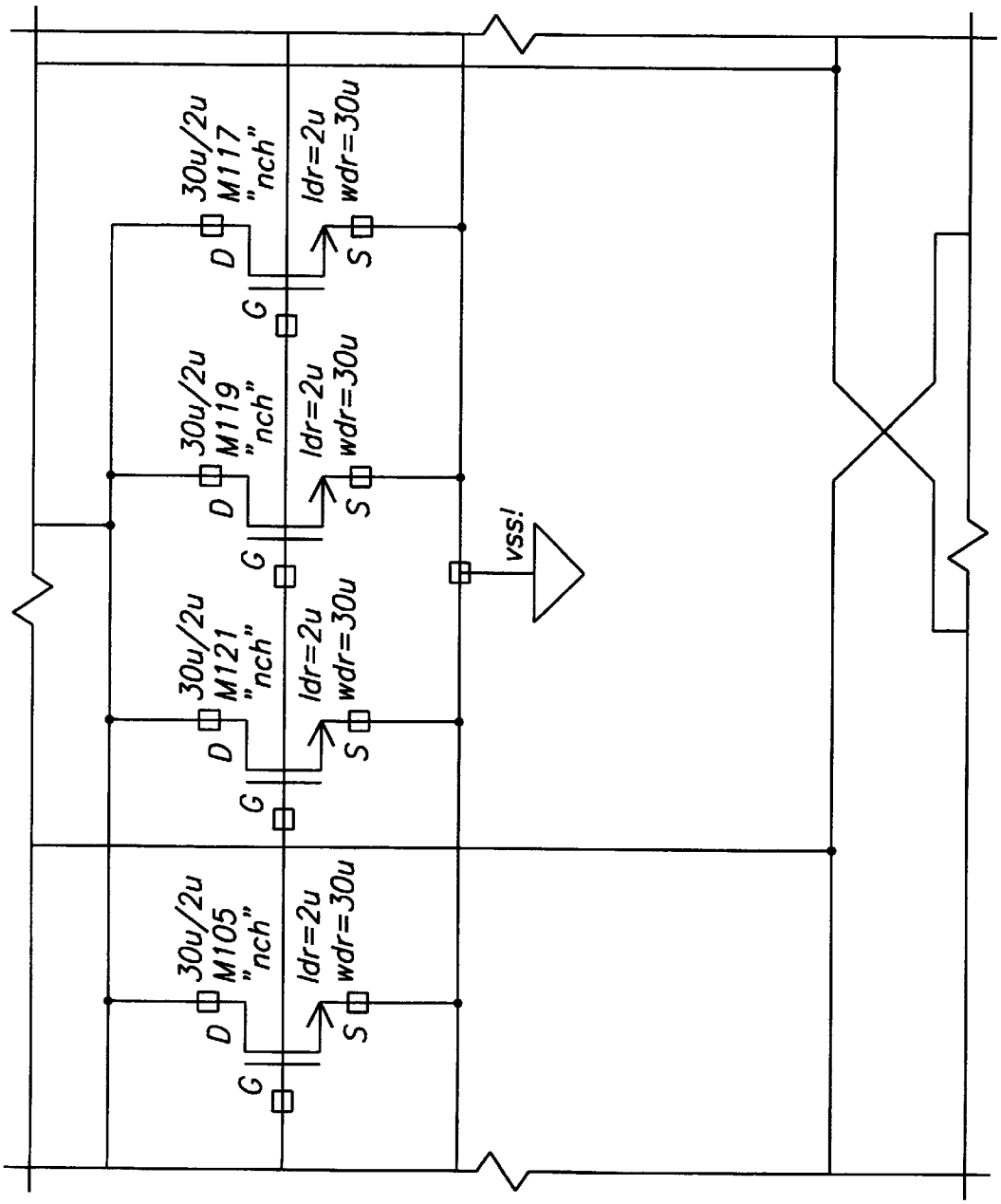

30u/2u
M117
"nch"
ldr=2u
wdr=30u
30u/2u
M119
"nch"
ldr=2u
wdr=30u
30u/2u
M121
"nch"
ldr=2u
wdr=30u
30u/2u
M105
"nch"
ldr=2u
wdr=30u
D
G
S
vss!

Fig 8.0050

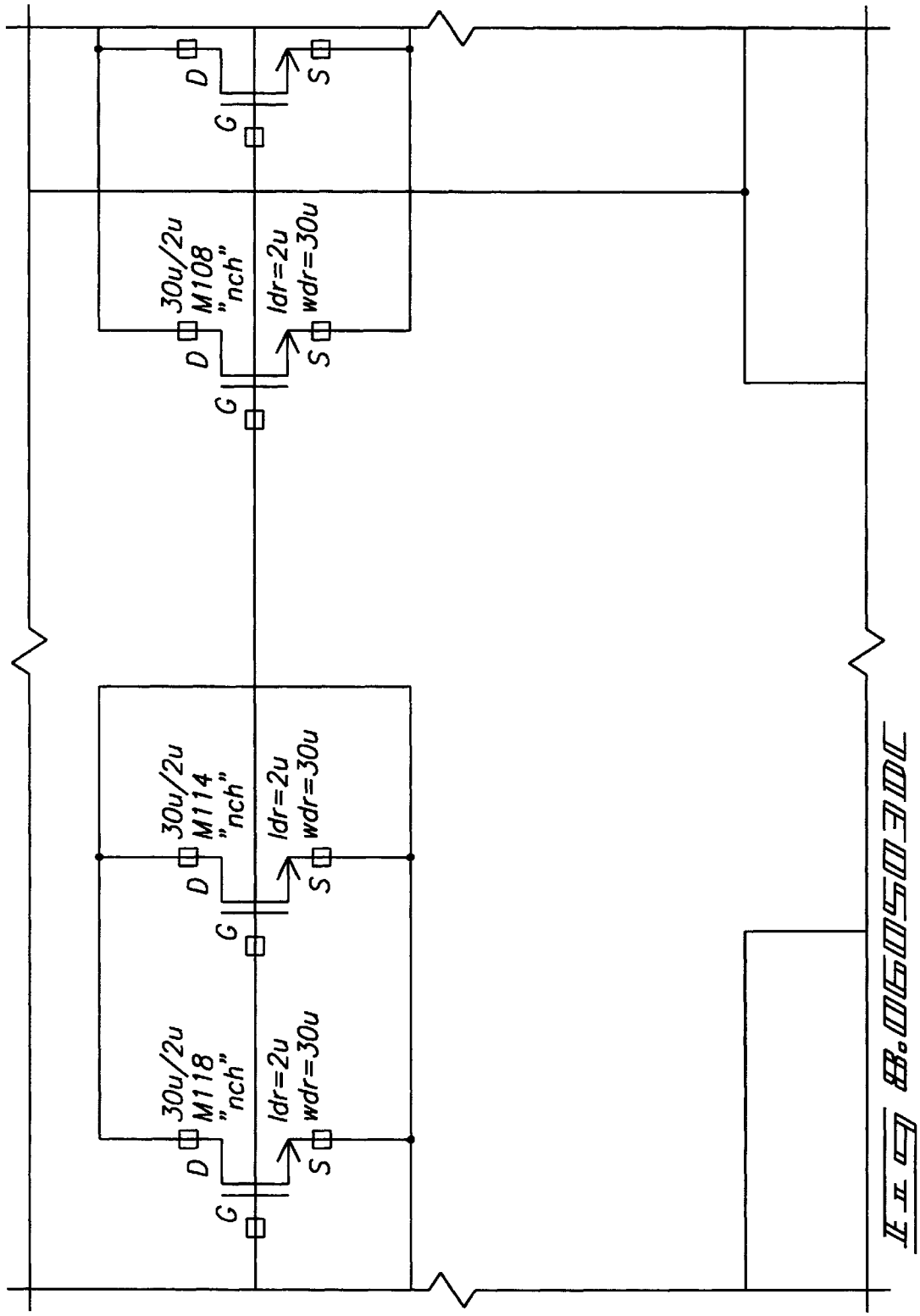
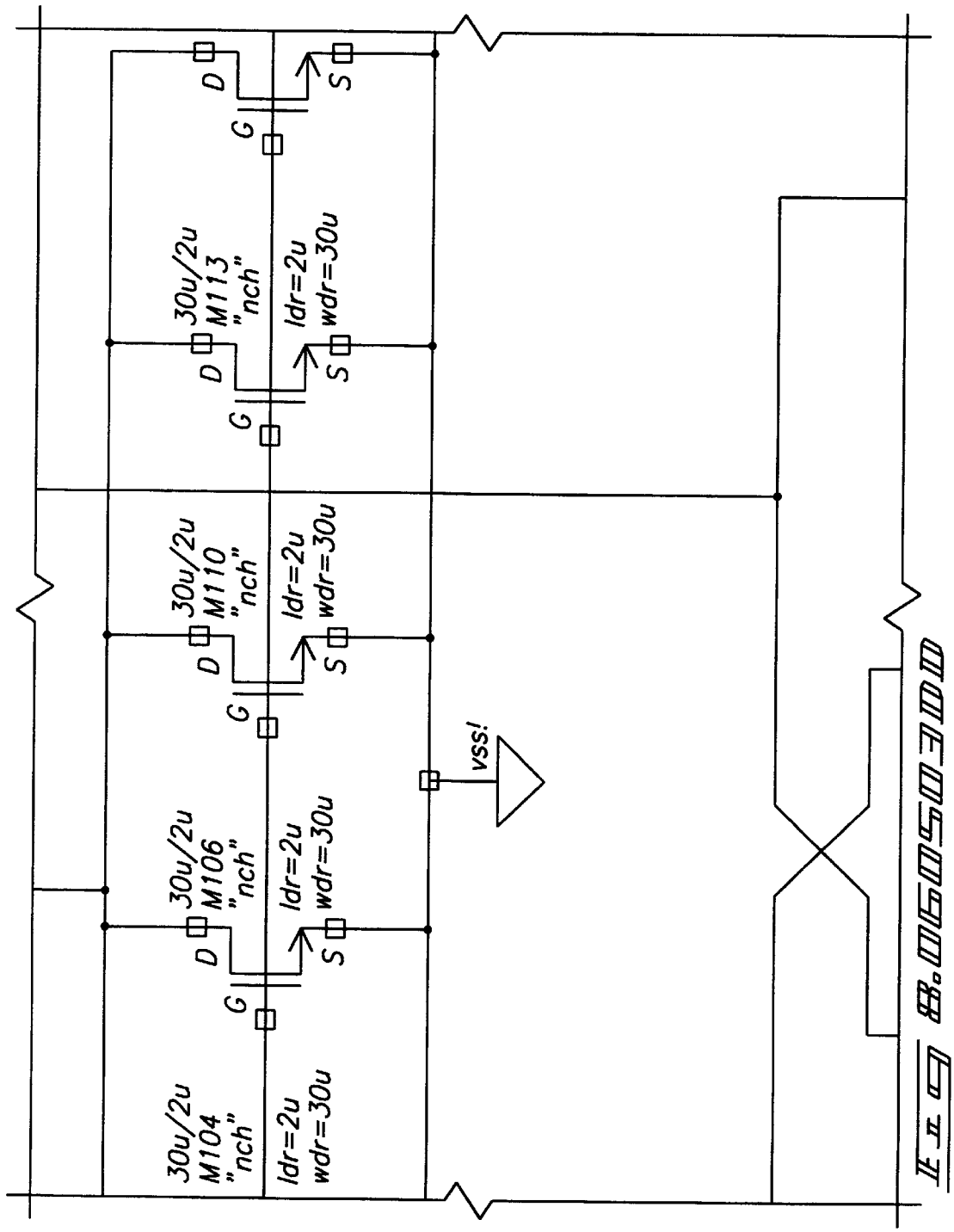

D
G
S
30u/2u
M108
"nch"
ldr=2u
wdr=30u
30u/2u
M114
"nch"
ldr=2u
wdr=30u
30u/2u
M118
"nch"
ldr=2u
wdr=30u

FIG 8


30u/2u
M104
"nch"
ldr=2u
wdr=30u
30u/2u
M106
"nch"
ldr=2u
wdr=30u
30u/2u
M110
"nch"
ldr=2u
wdr=30u
30u/2u
M113
"nch"
ldr=2u
wdr=30u
vss!
D
G
S

Фиг 59

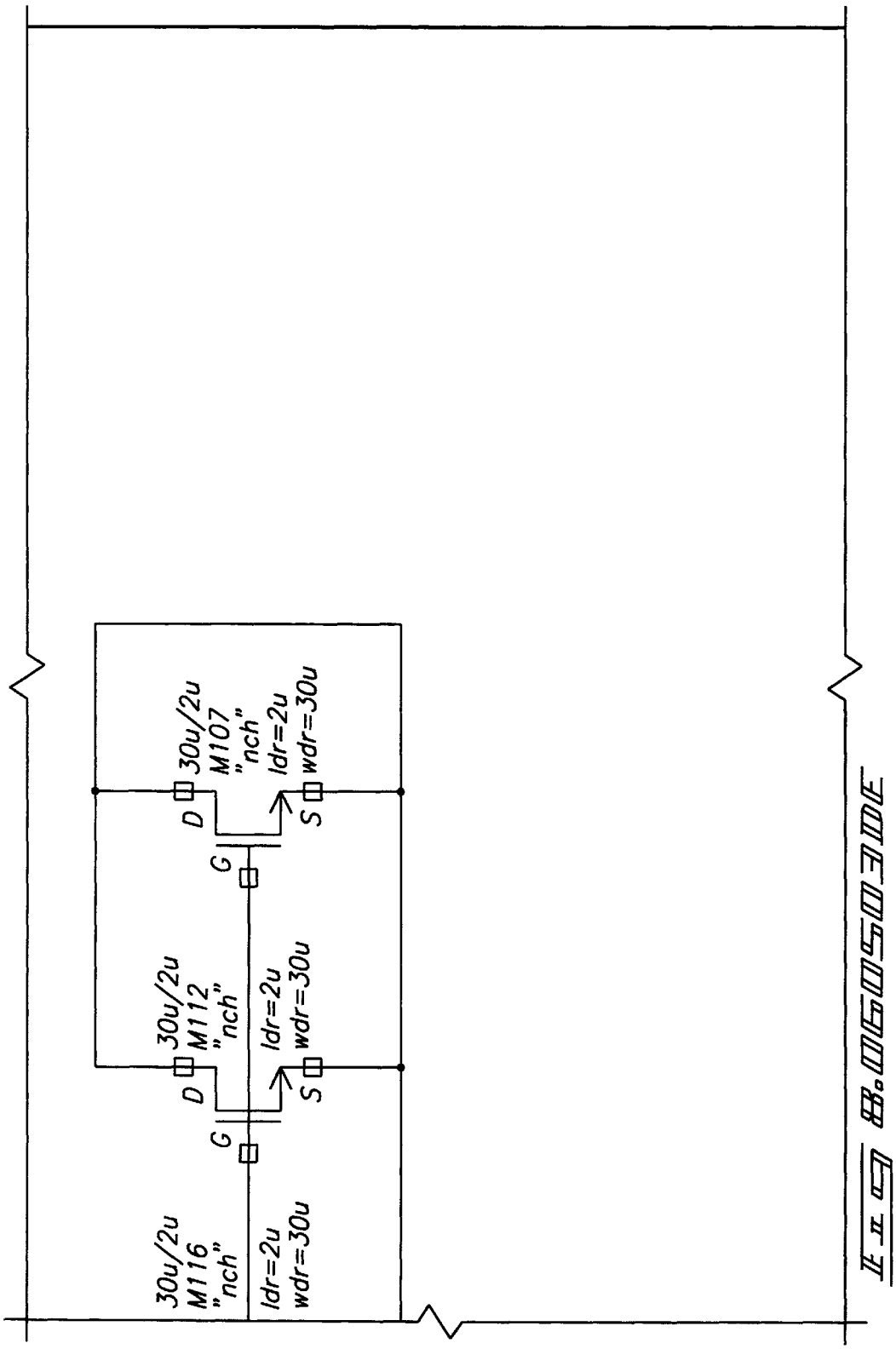
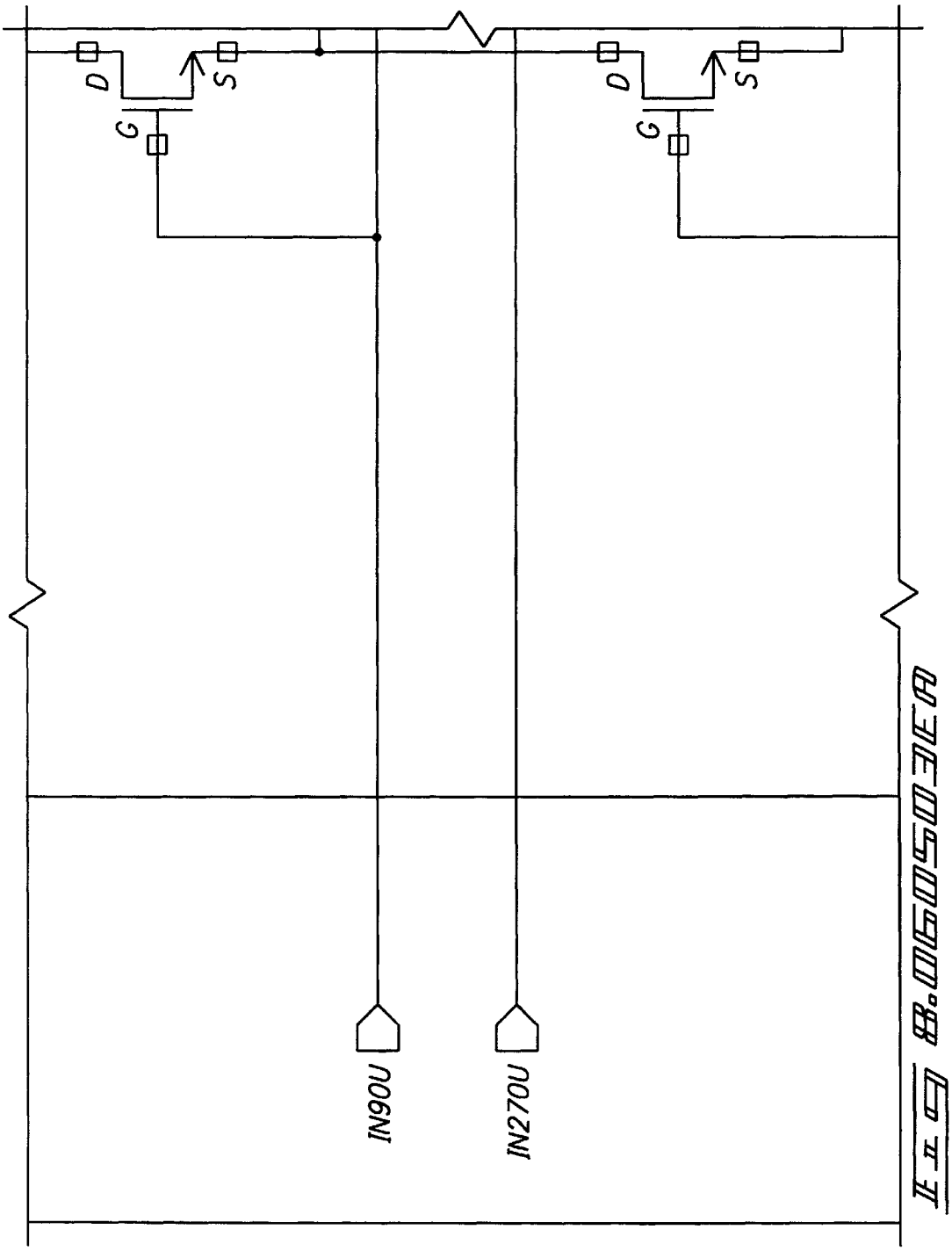
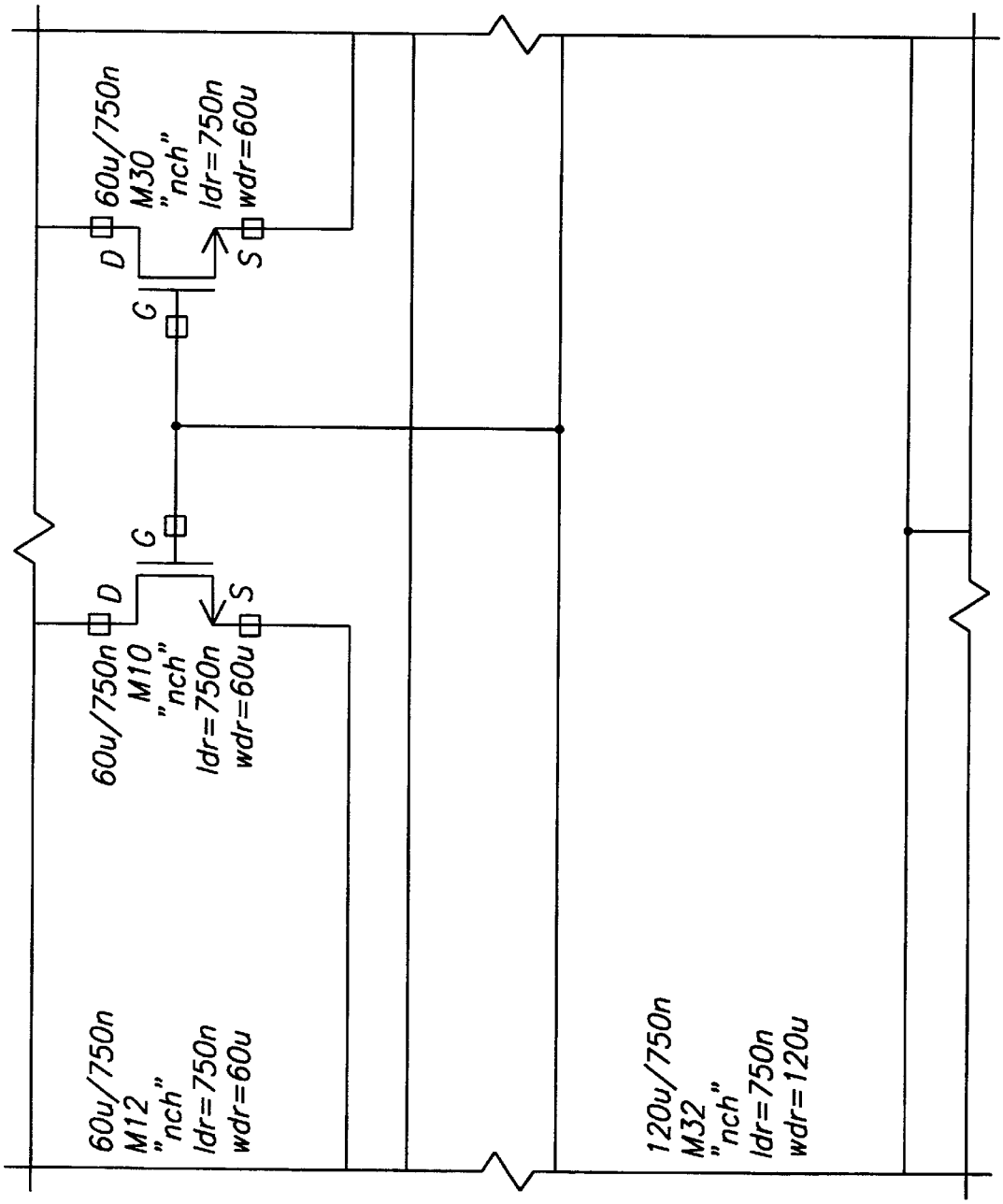
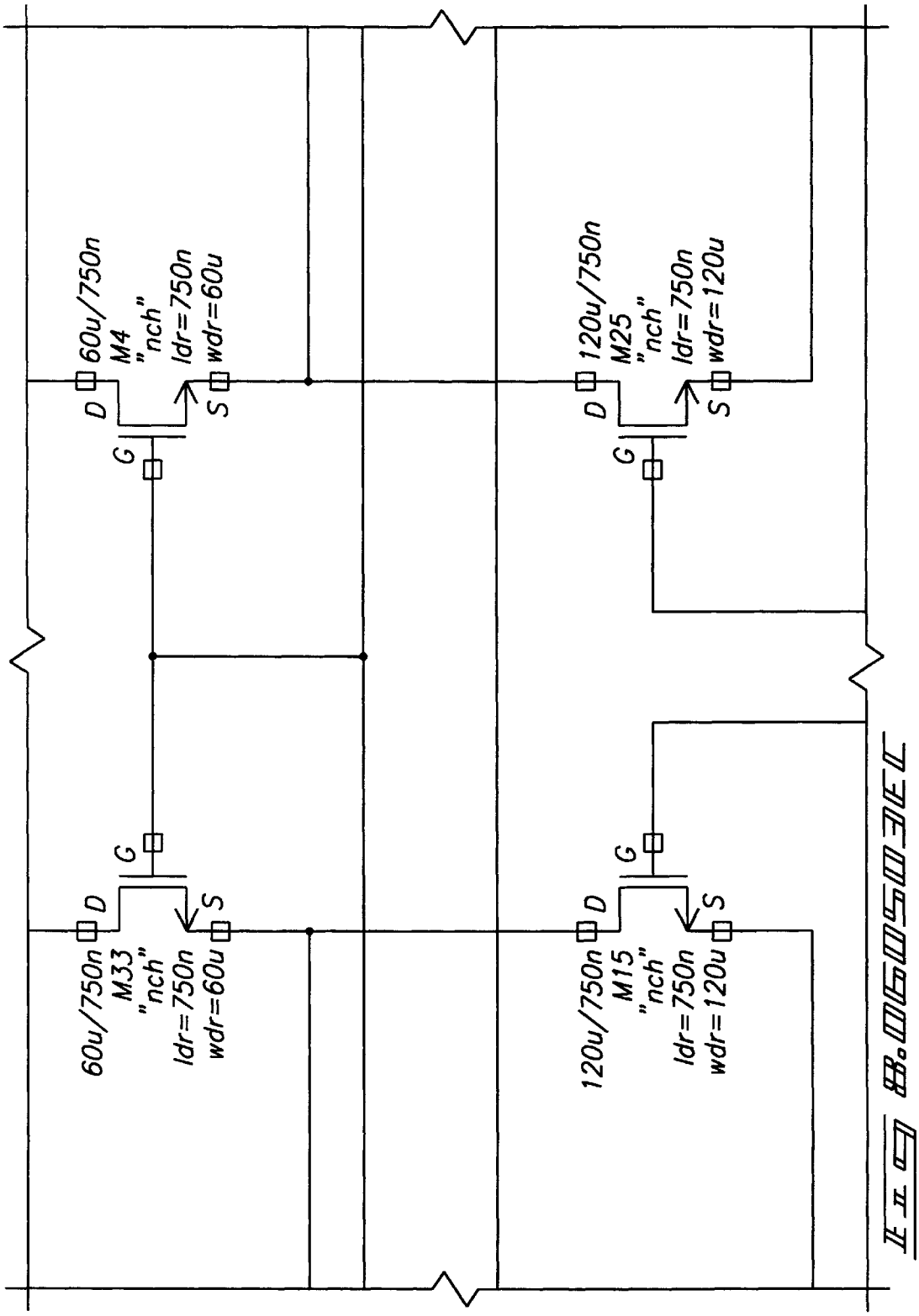

30u/2u
M107
"nch"
ldr=2u
wdr=30u
D
G
S
30u/2u
M112
"nch"
ldr=2u
wdr=30u
D
G
S
30u/2u
M116
"nch"
ldr=2u
wdr=30u

FIG. 8,005,005

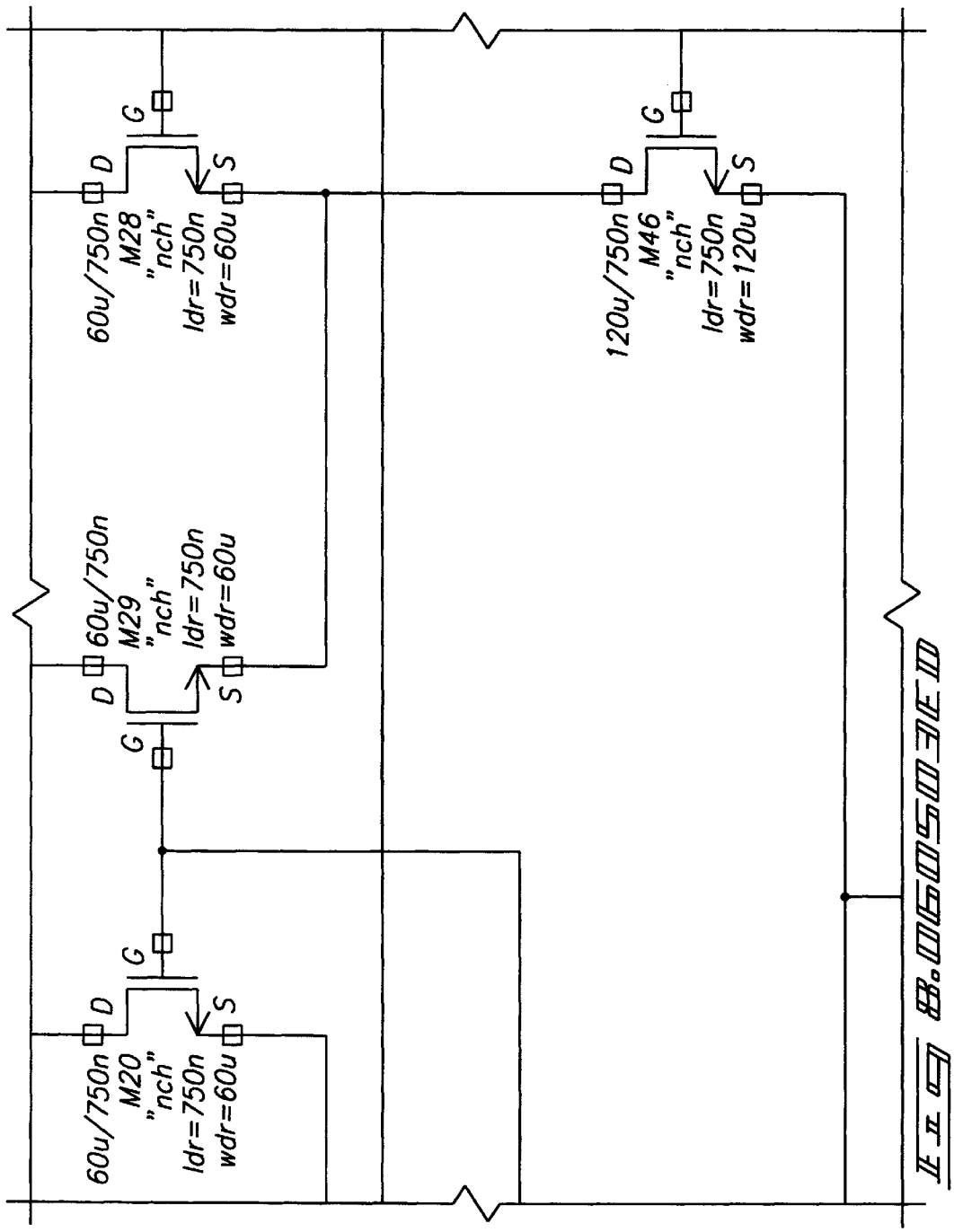

D
S
G
D
S
G
IN90U
IN270U
VSS
VCC
VEE
GND


60u/750n
M30
"nch"
ldr=750n
wdr=60u
D
G
S
60u/750n
M10
"nch"
ldr=750n
wdr=60u
60u/750n
M12
"nch"
ldr=750n
wdr=60u
120u/750n
M32
"nch"
ldr=750n
wdr=120u

Фиг. 8,0509E


60u/750n
M4
"nch"
ldr=750n
wdr=60u
120u/750n
M25
"nch"
ldr=750n
wdr=120u
60u/750n
M33
"nch"
ldr=750n
wdr=60u
120u/750n
M15
"nch"
ldr=750n
wdr=120u
D
G
S

Фиг 8.0500.8


60u/750n
M28
"nch"
ldr=750n
wdr=60u
120u/750n
M46
"nch"
ldr=750n
wdr=120u
60u/750n
M29
"nch"
ldr=750n
wdr=60u
60u/750n
M20
"nch"
ldr=750n
wdr=60u
G
D
S

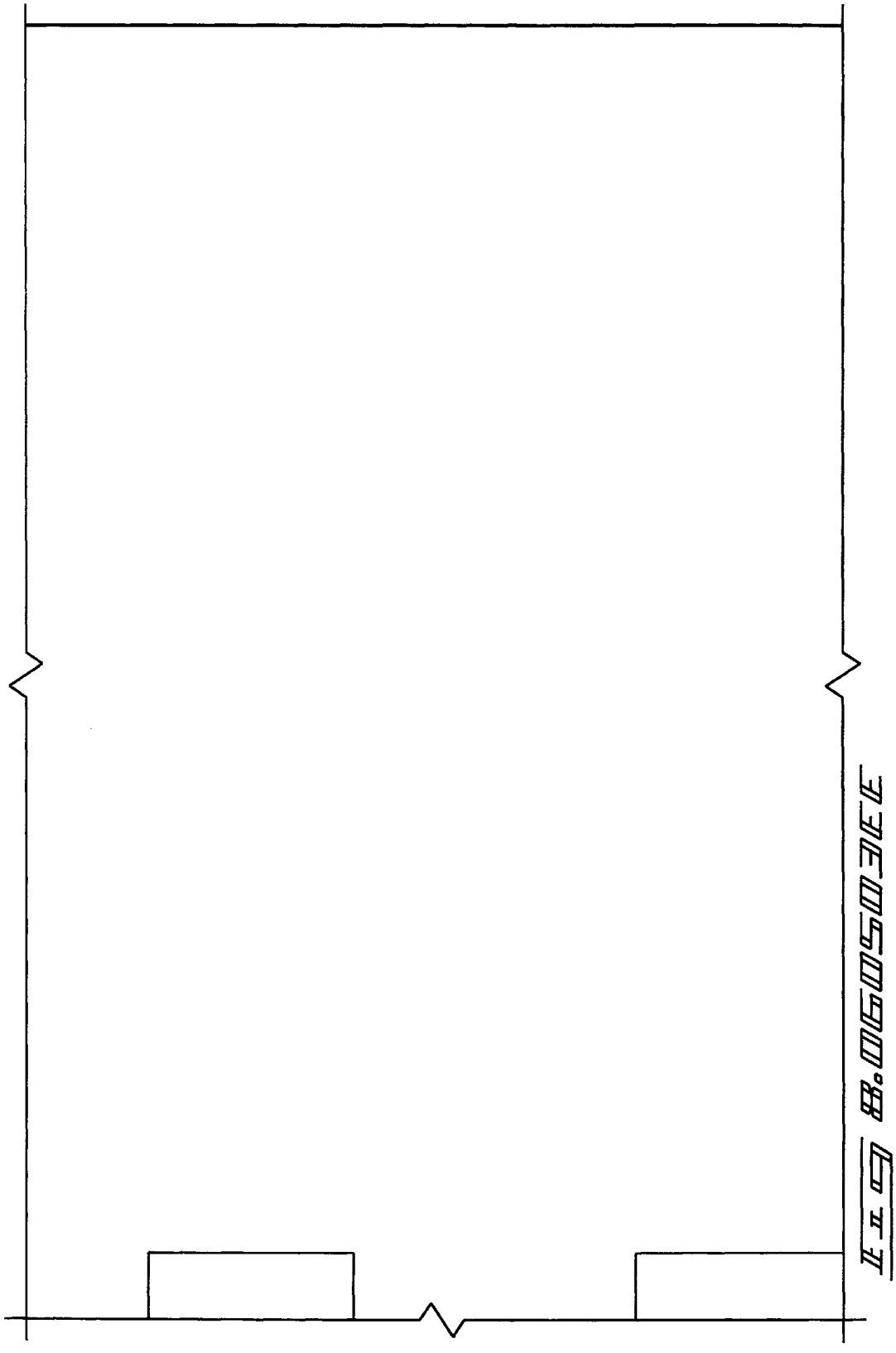
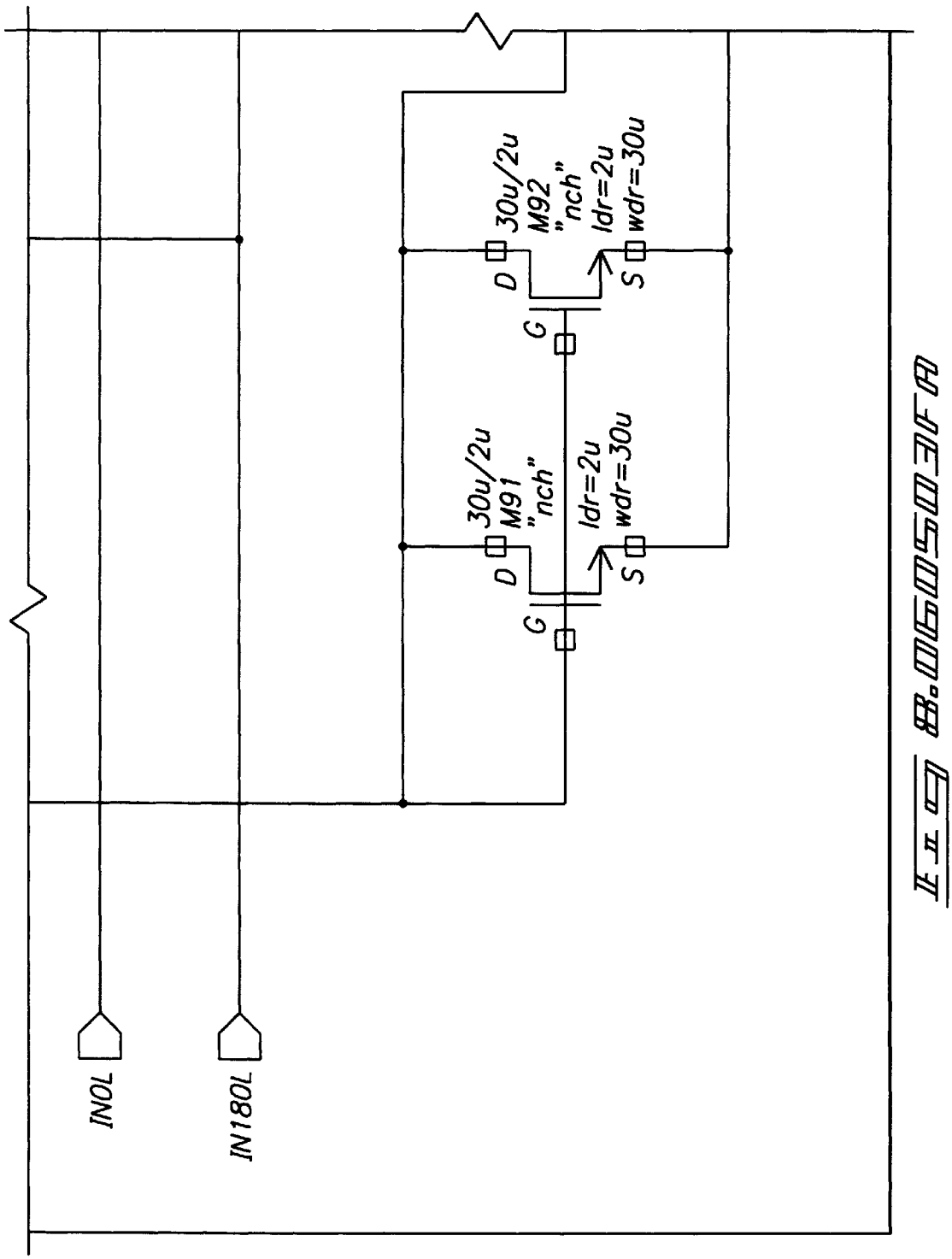
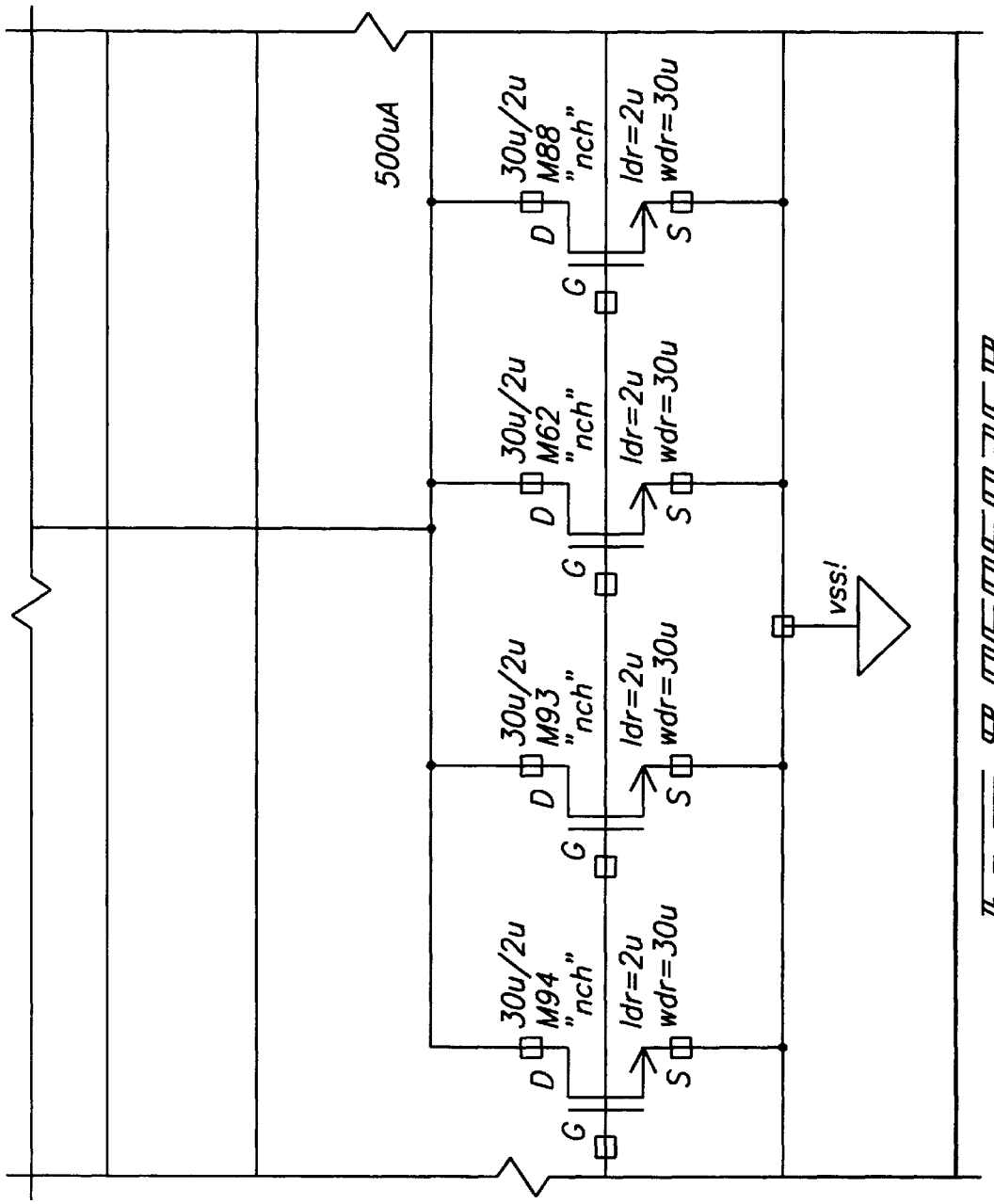


FIG. 89.0050E



Фиг. 88.0505.0ЭГА


500uA
30u/2u
M88
"nch"
ldr=2u
wdr=30u
30u/2u
M62
"nch"
ldr=2u
wdr=30u
30u/2u
M93
"nch"
ldr=2u
wdr=30u
30u/2u
M94
"nch"
ldr=2u
wdr=30u
D
G
S
vss!

Фиг 6,130,602

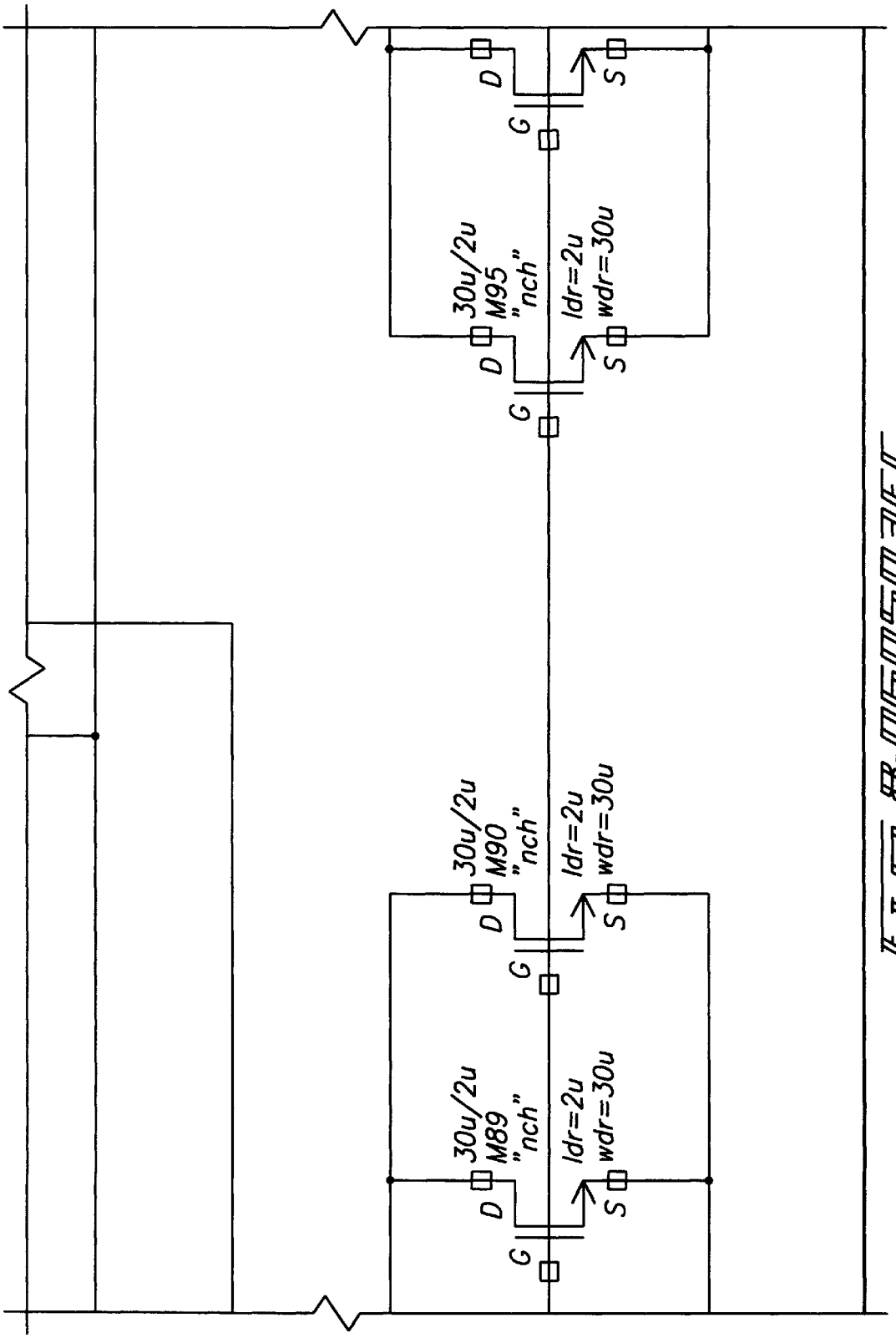

D
G
S
30u/2u
M95
"nch"
ldr=2u
wdr=30u
30u/2u
M90
"nch"
ldr=2u
wdr=30u
30u/2u
M89
"nch"
ldr=2u
wdr=30u

FIG 88.0050

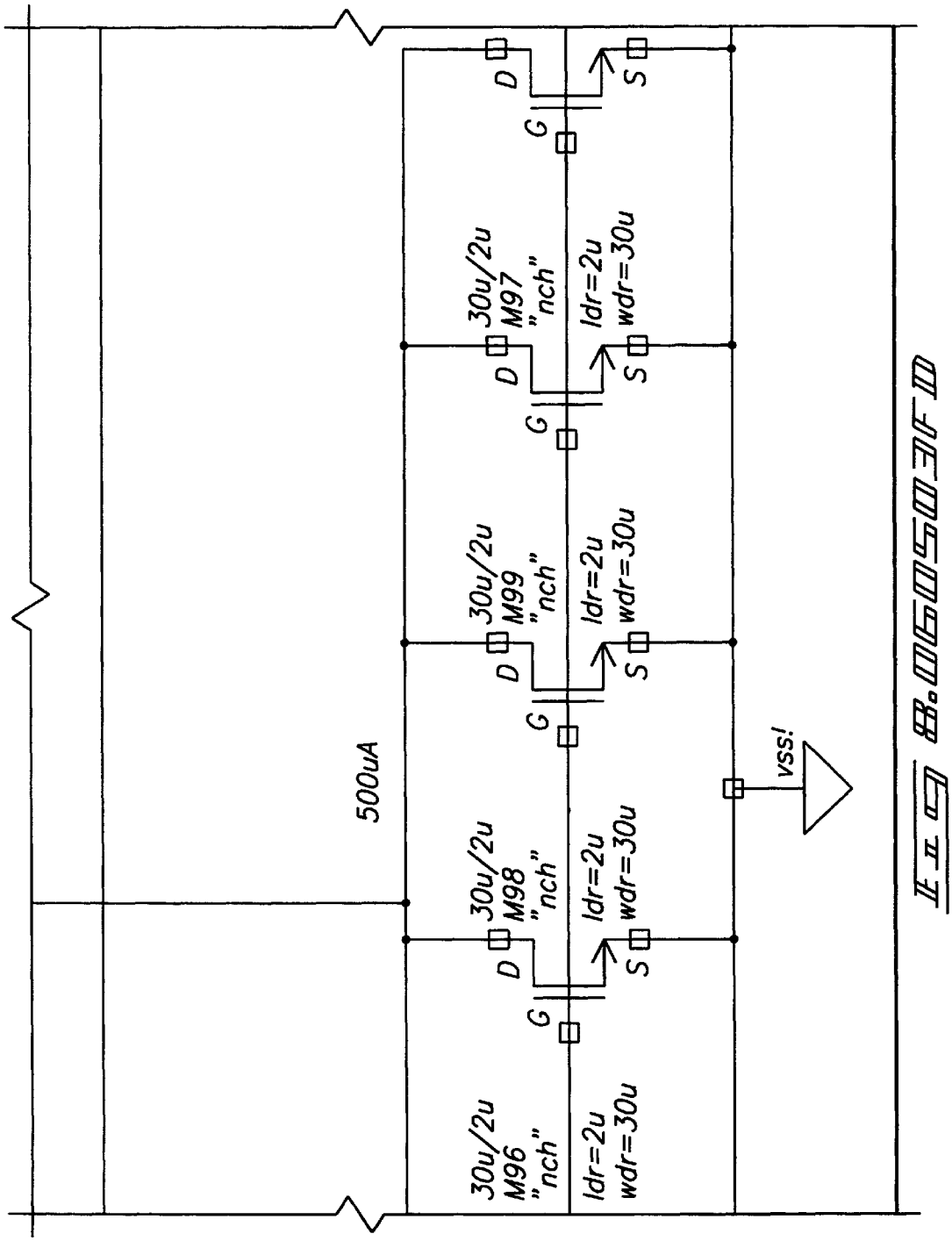

D
G
S
30u/2u
M97
"nch"
ldr=2u
wdr=30u
30u/2u
M99
"nch"
ldr=2u
wdr=30u
500uA
30u/2u
M98
"nch"
ldr=2u
wdr=30u
vss!
30u/2u
M96
"nch"
ldr=2u
wdr=30u

FIG. 8,056,037

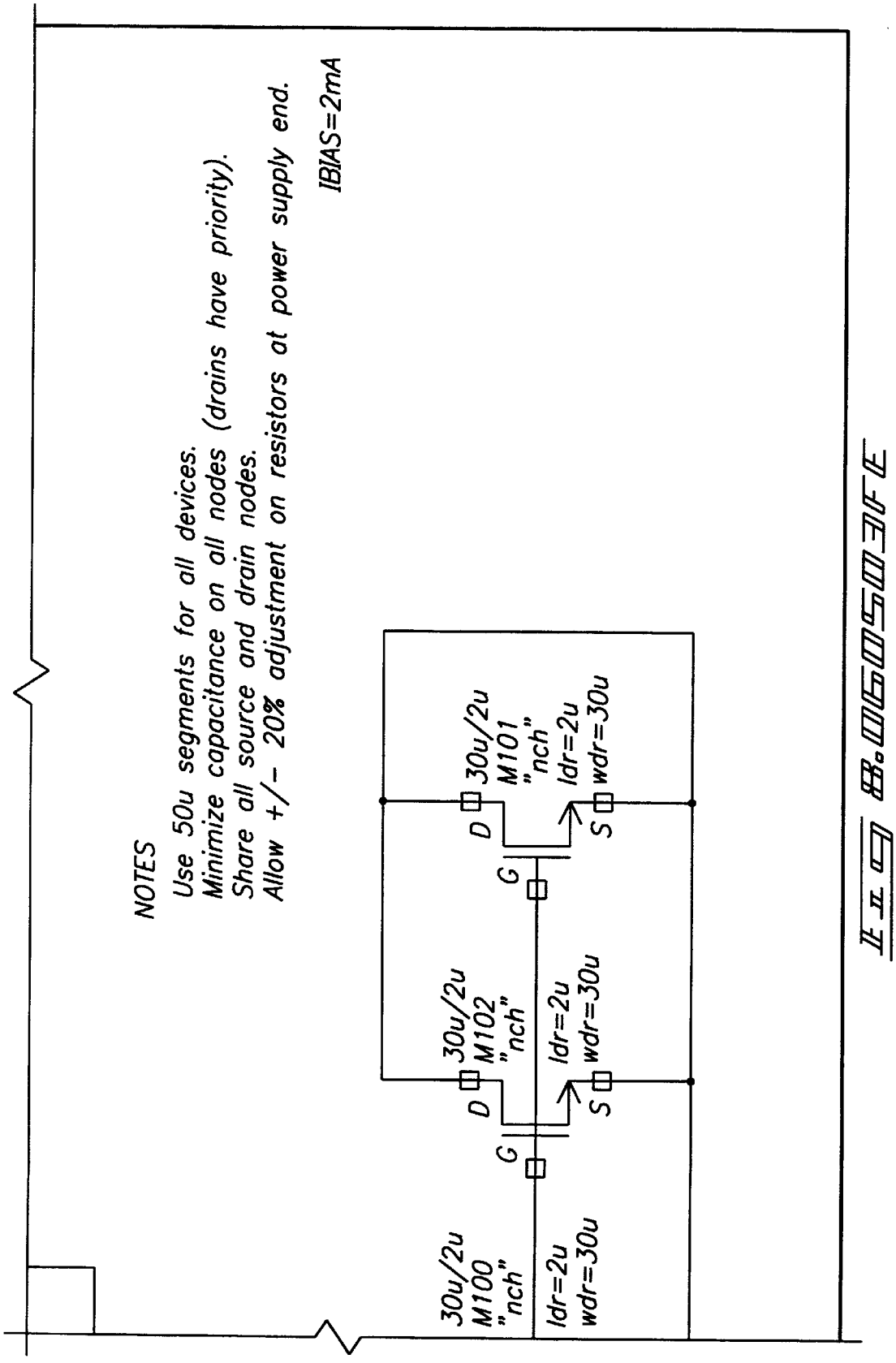


FIG. 8.0SOOSJFE

8.0606AA	8.0606AB	8.0606AC	8.0606AD	8.0606AE	8.0606AF	8.0606AG	8.0606AH	
8.0606BA	8.0606BB	8.0606BC	8.0606BD	8.0606BE	8.0606BF	8.0606BG	8.0606BH	
8.0606CA	8.0606CB	8.0606CC	8.0606CD	8.0606CE	8.0606CF	8.0606CG	8.0606CH	8.0606CI
8.0606DA	8.0606DB	8.0606DC	8.0606DD	8.0606DE	8.0606DF	8.0606DG	8.0606DH	8.0606DI
8.0606EA	8.0606EB	8.0606EC	8.0606ED	8.0606EE	8.0606EF	8.0606EG	8.0606EH	8.0606EI
8.0606FA	8.0606FB	8.0606FC	8.0606FD	8.0606FE	8.0606FF	8.0606FG	8.0606FH	8.0606FI
		8.0606GC	8.0606GD	8.0606GE				
	8.0606HB	8.0606HC	8.0606HD	8.0606HE				
8.0606HA								
		8.0606IC	8.0606ID	8.0606IE				

FIG 8.0606

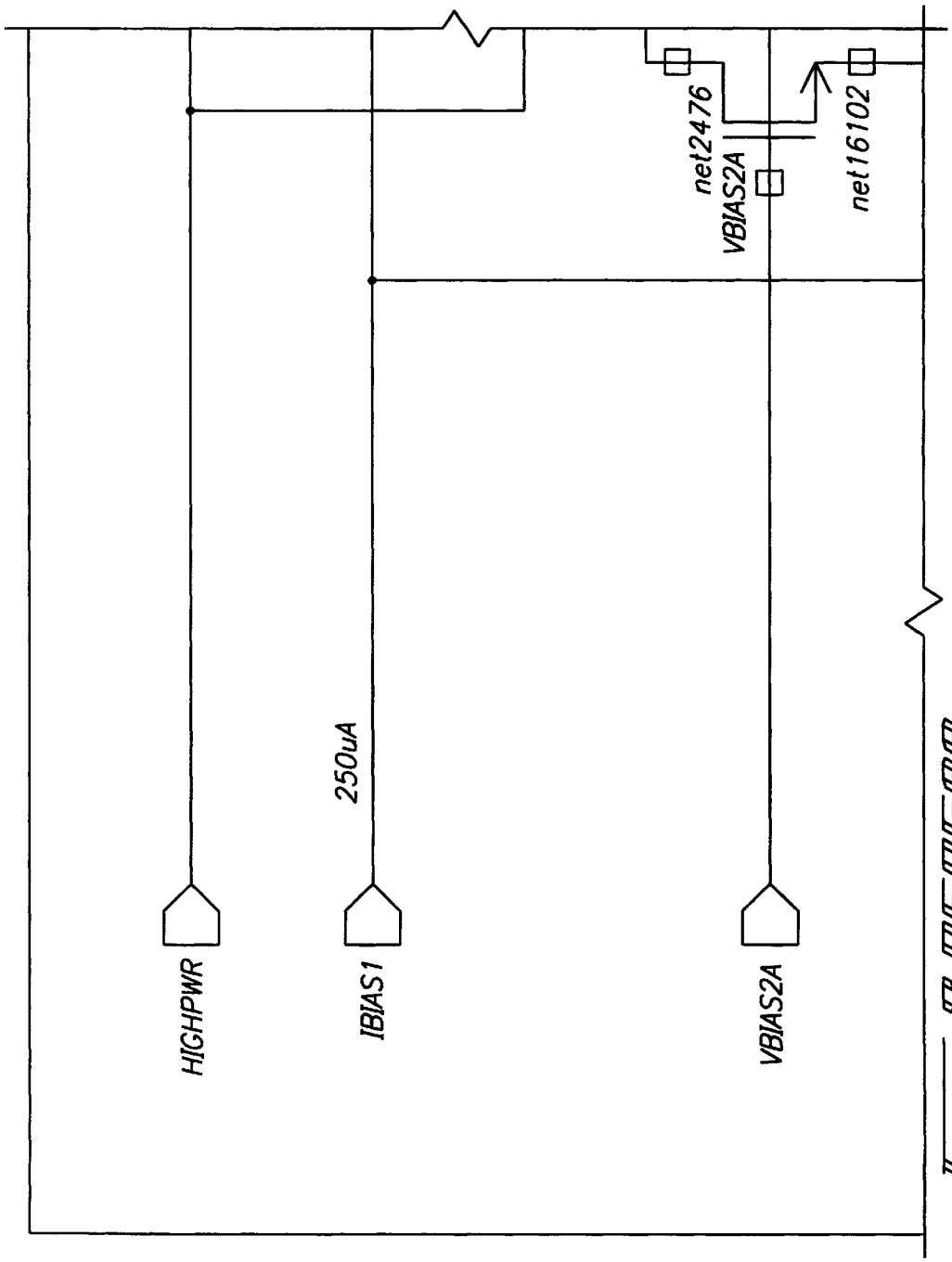
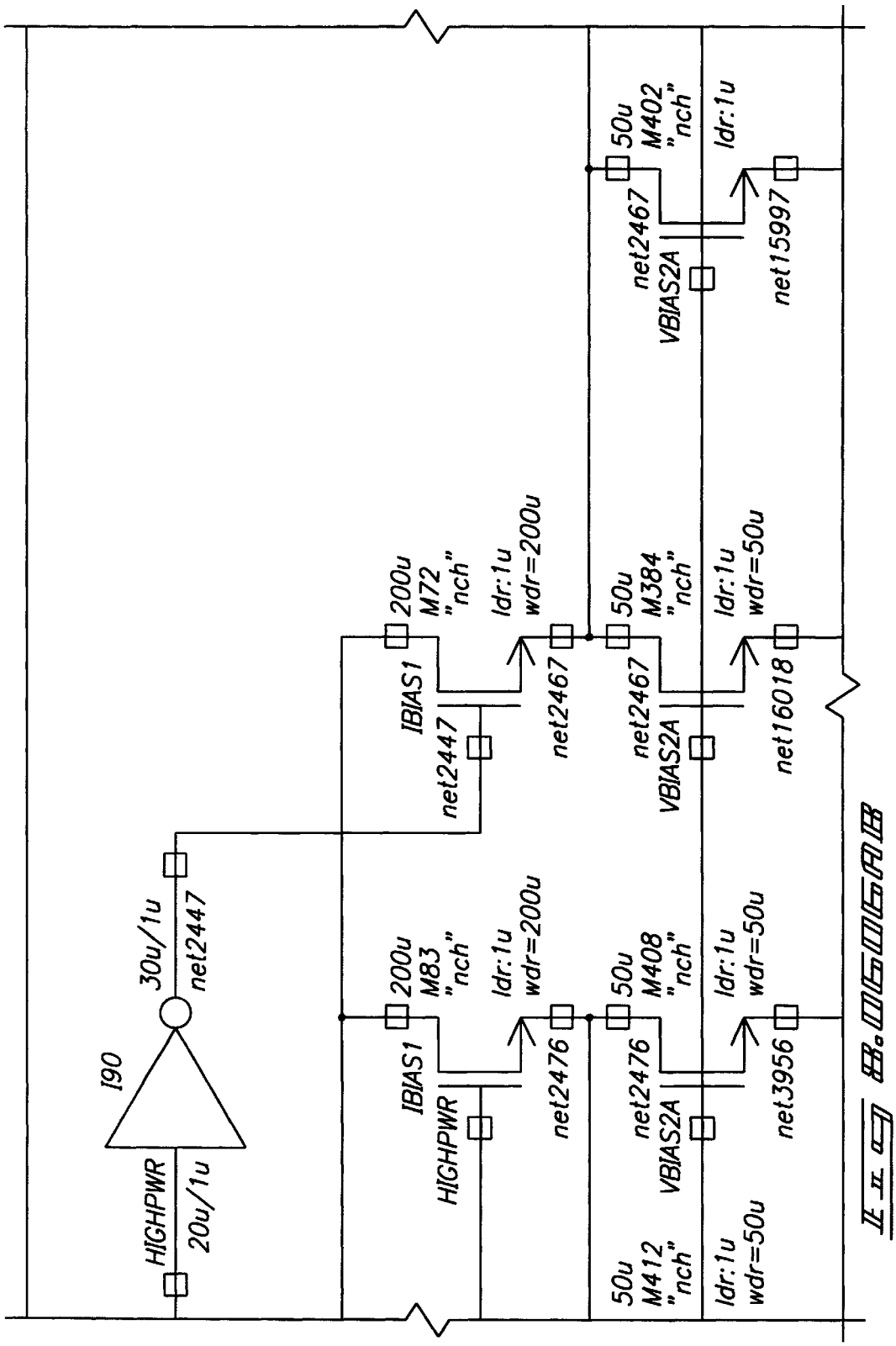
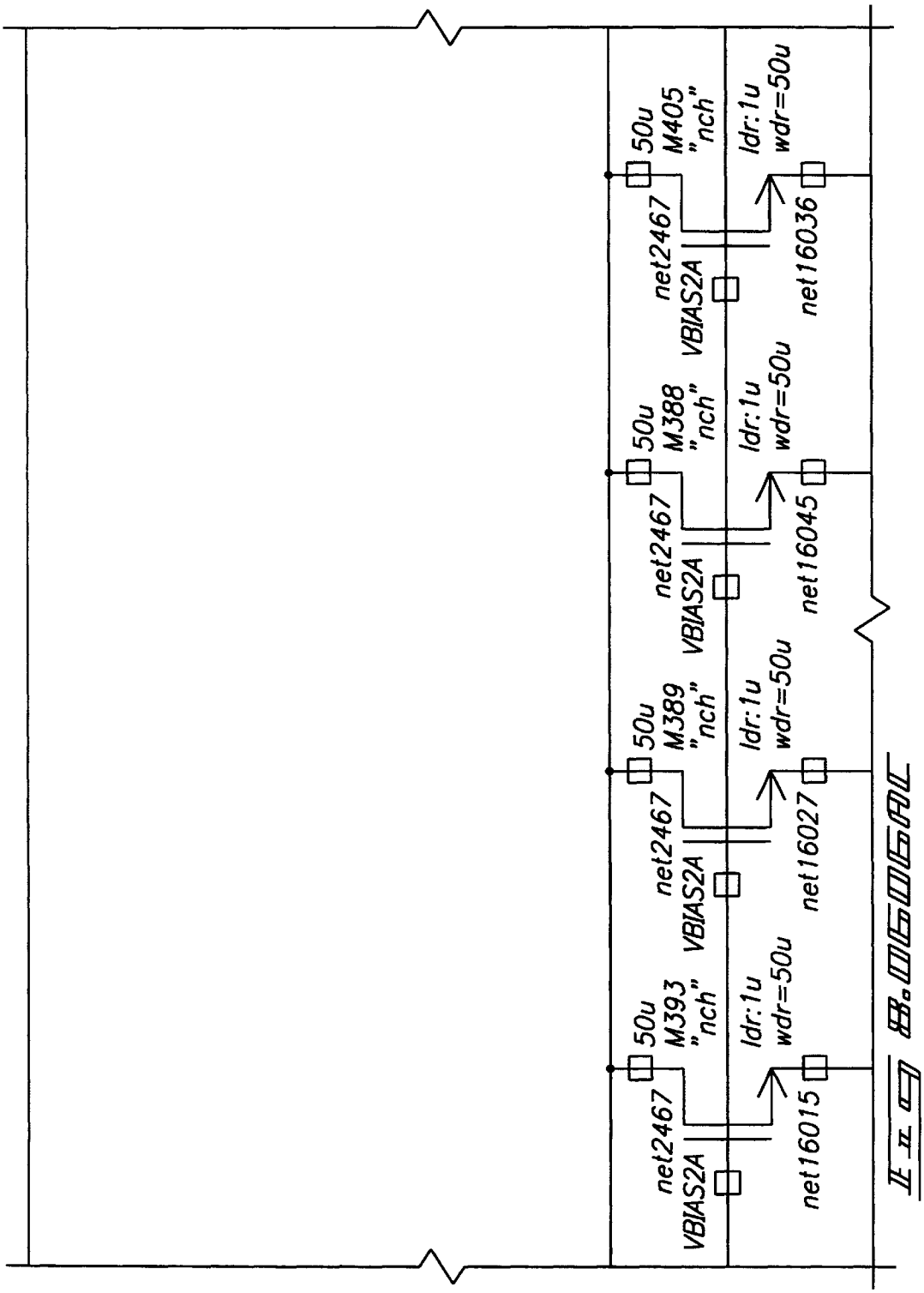
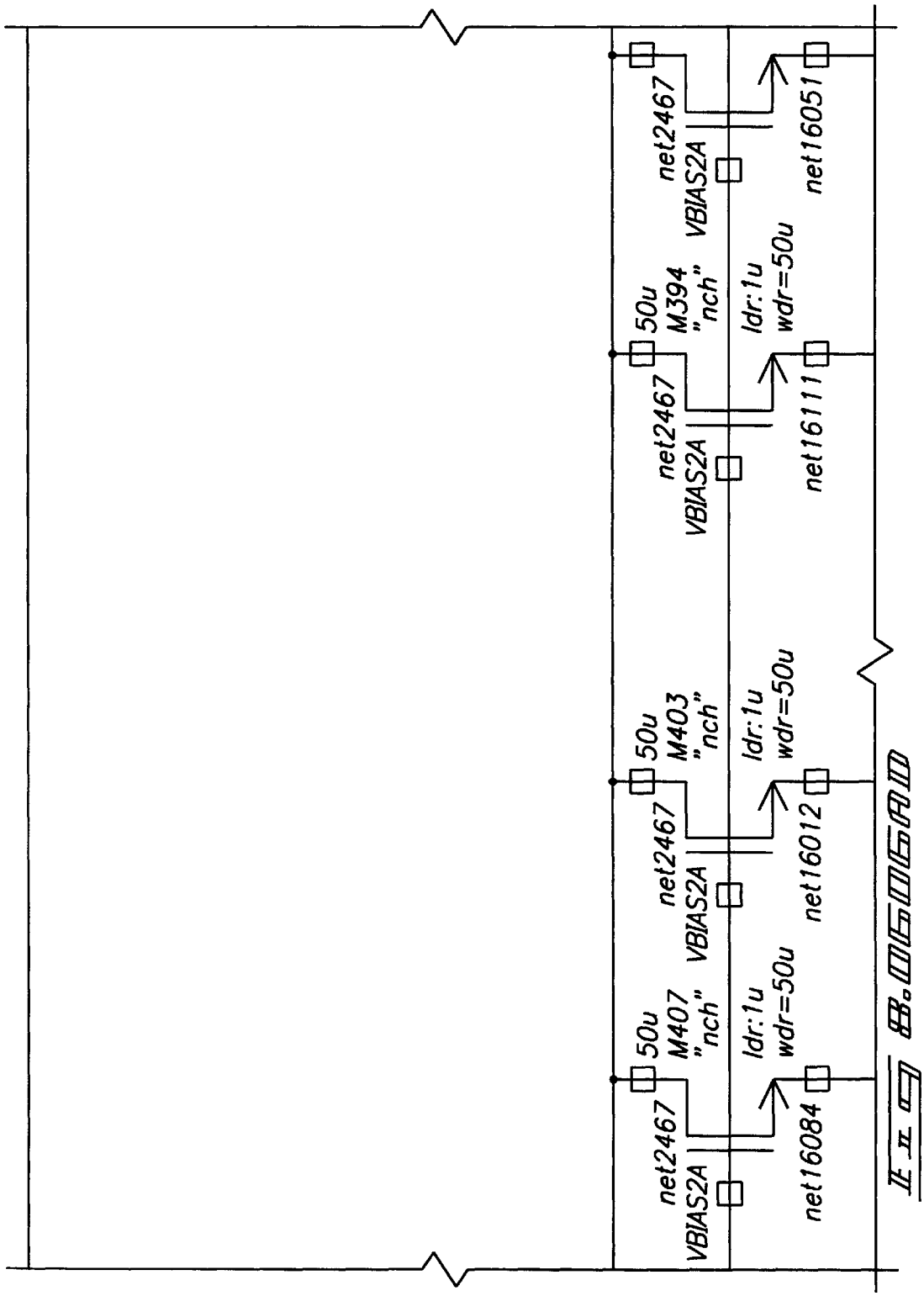


Fig. 88,056,044


I90
30u/1u
net2447
HIGHPWR
20u/1u
IBIAS1
net2447
200u
M83
"nch"
ldr:1u
wdr=200u
net2476
IBIAS1
HIGHPWR
200u
M72
"nch"
ldr:1u
wdr=200u
net2467
net2476
VBIAS2A
50u
M408
"nch"
ldr:1u
wdr=50u
net3956
net2467
VBIAS2A
50u
M384
"nch"
ldr:1u
wdr=50u
net16018
50u
M412
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
50u
M402
"nch"
ldr:1u
net15997


50u
M405
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
net16036
50u
M388
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
net16045
50u
M389
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
net16027
50u
M393
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
net16015


net2467
VBIAS2A
net16051
50u
M394
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
net16111
50u
M403
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
net16012
50u
M407
"nch"
ldr:1u
wdr=50u
net2467
VBIAS2A
net16084

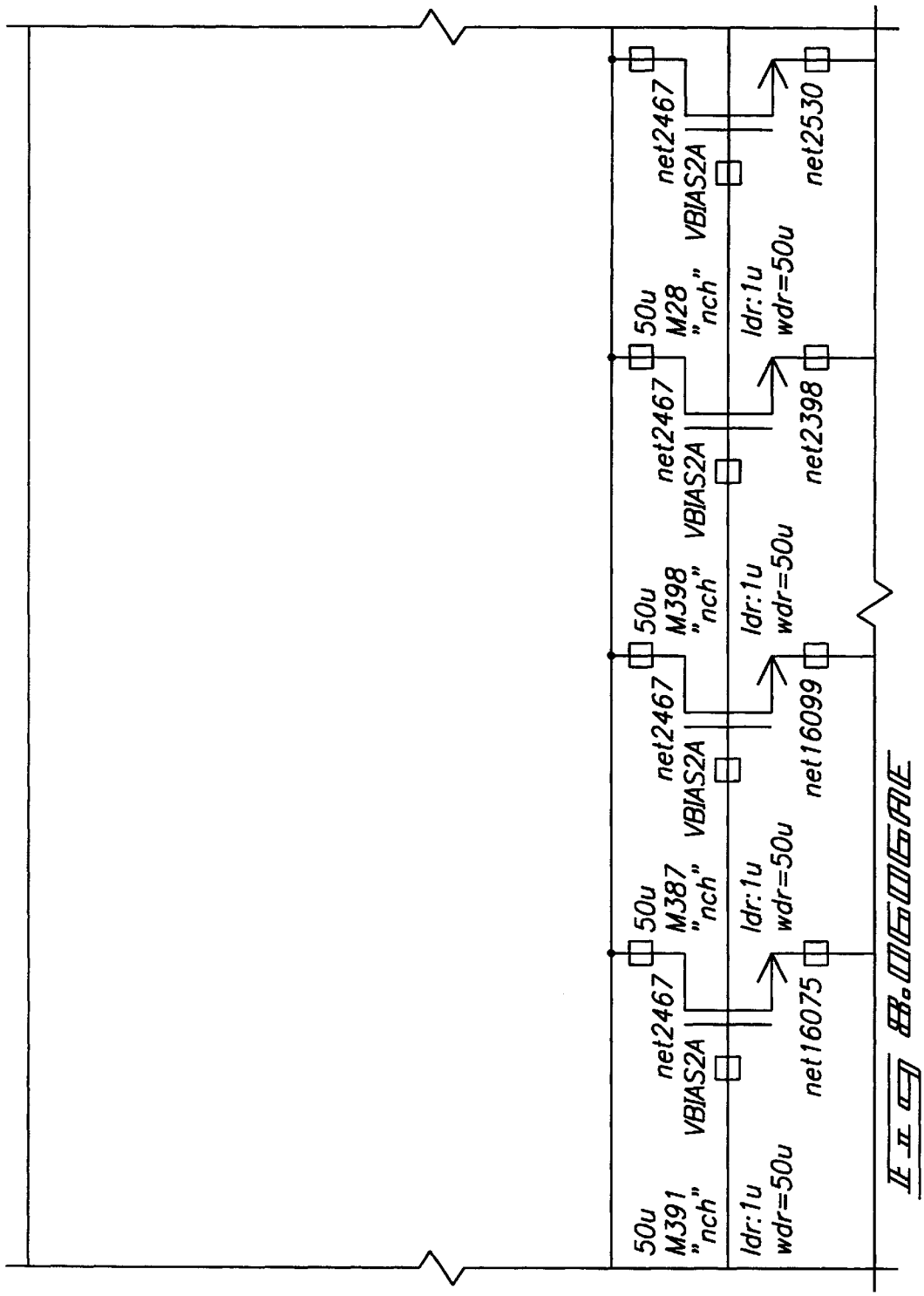


FIG. 88.0SGOSAE

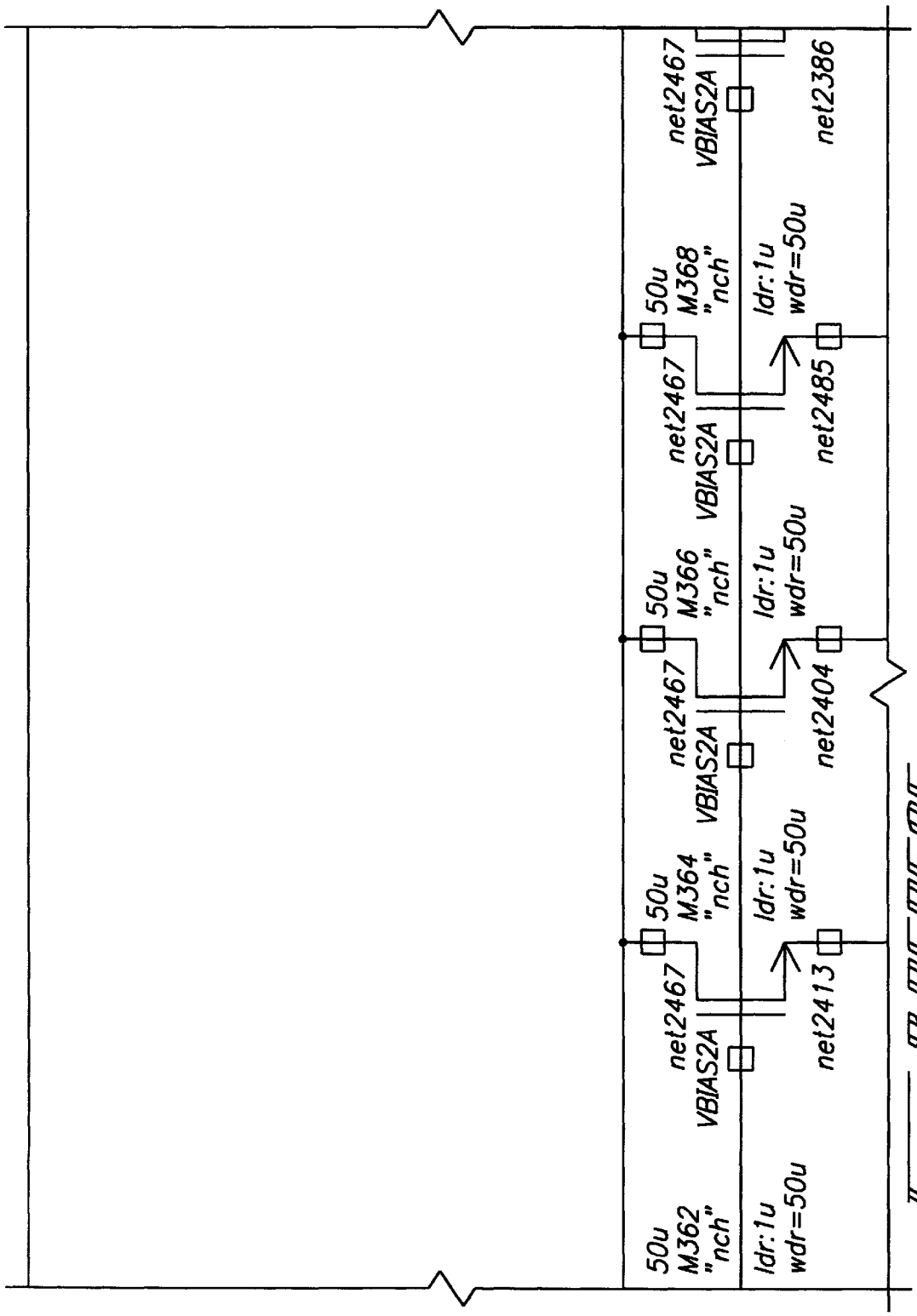
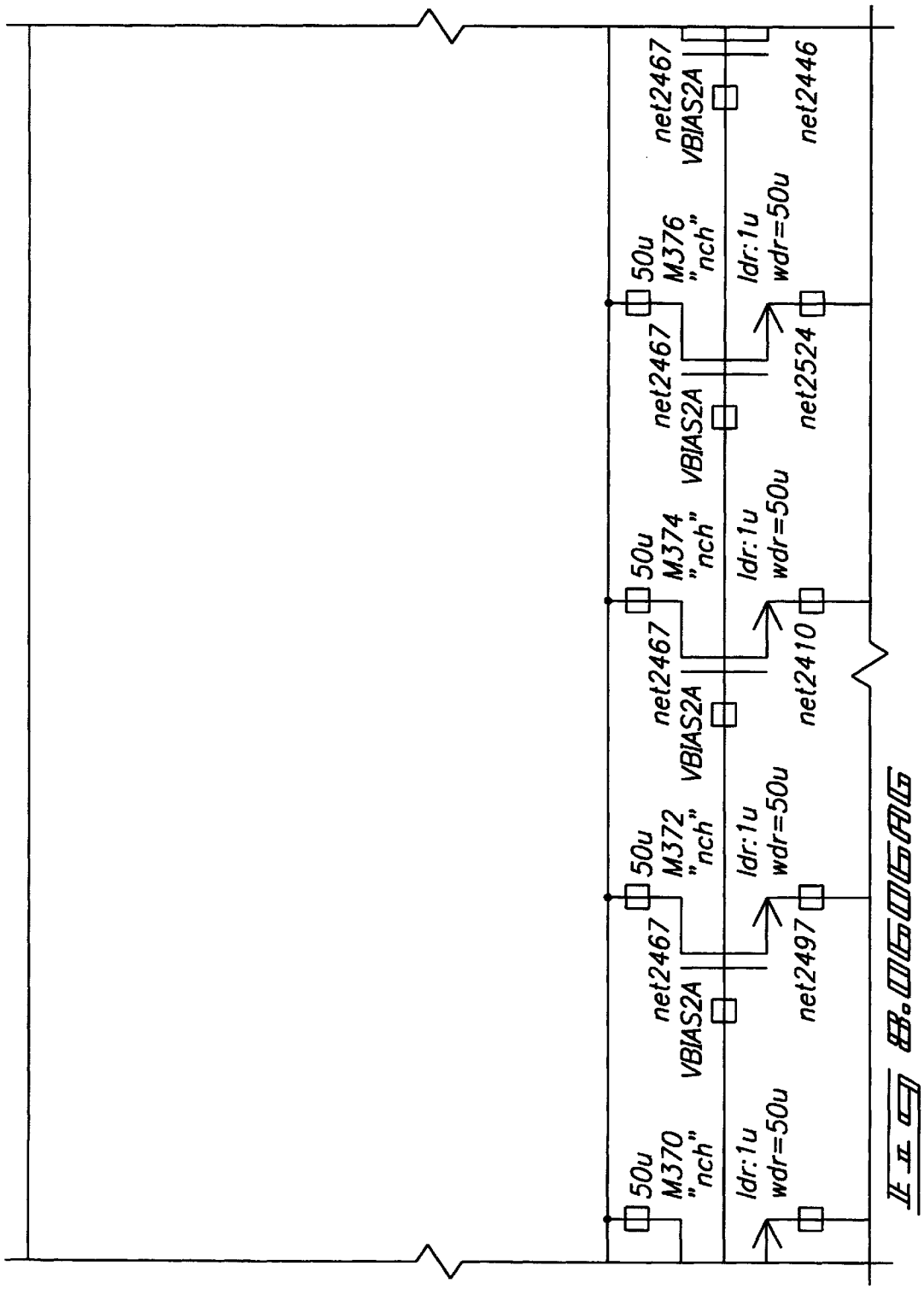


FIG. 88.0056AF


net2467
VBIAS2A
net2446
50u
M376
"nch"
ldr:1u
wdr=50u
net2524
net2410
net2497
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M374
"nch"
50u
M372
"nch"
50u
M370
"nch"

FIG. 8.0650AS

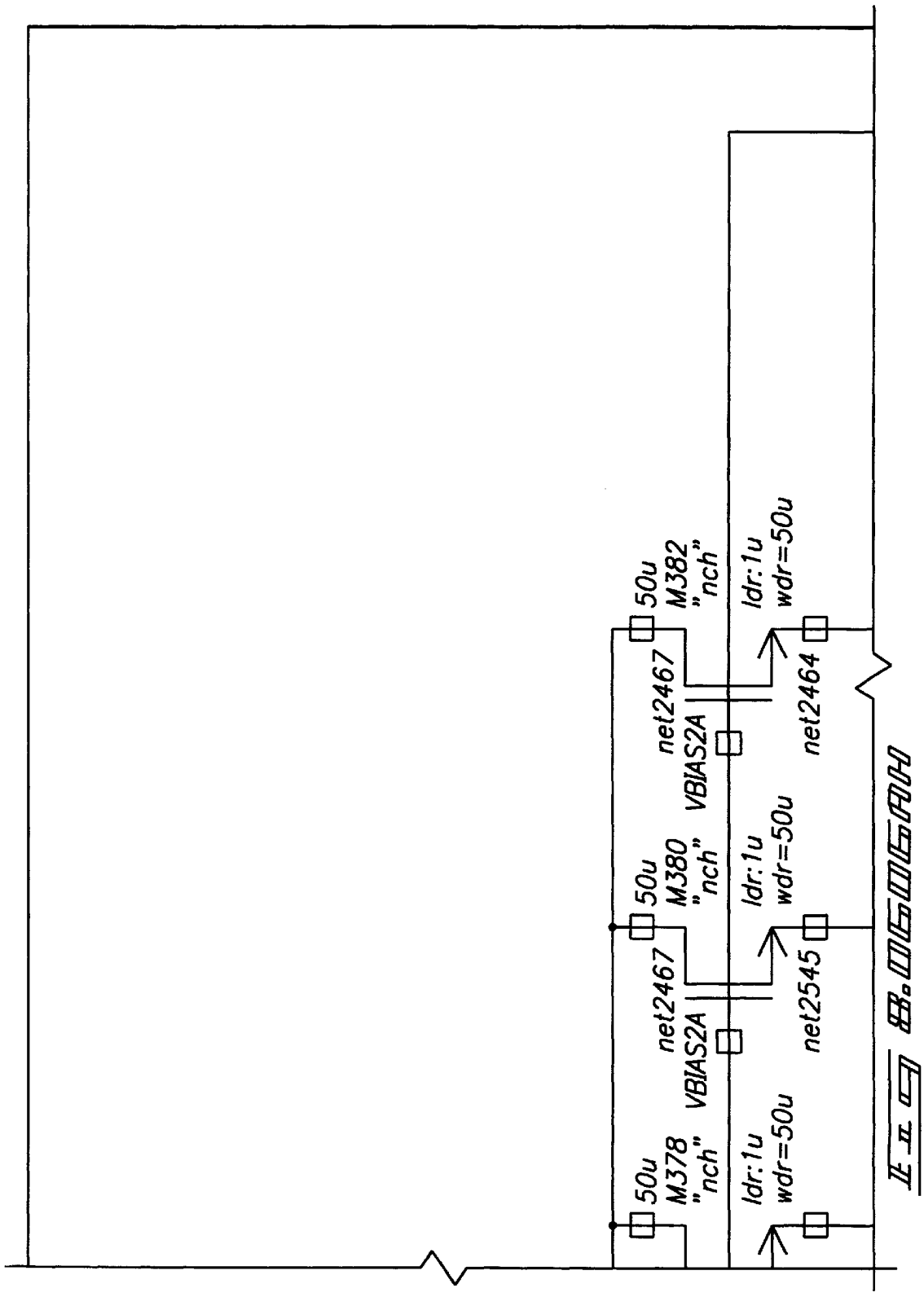


Fig. 6B,0656AH

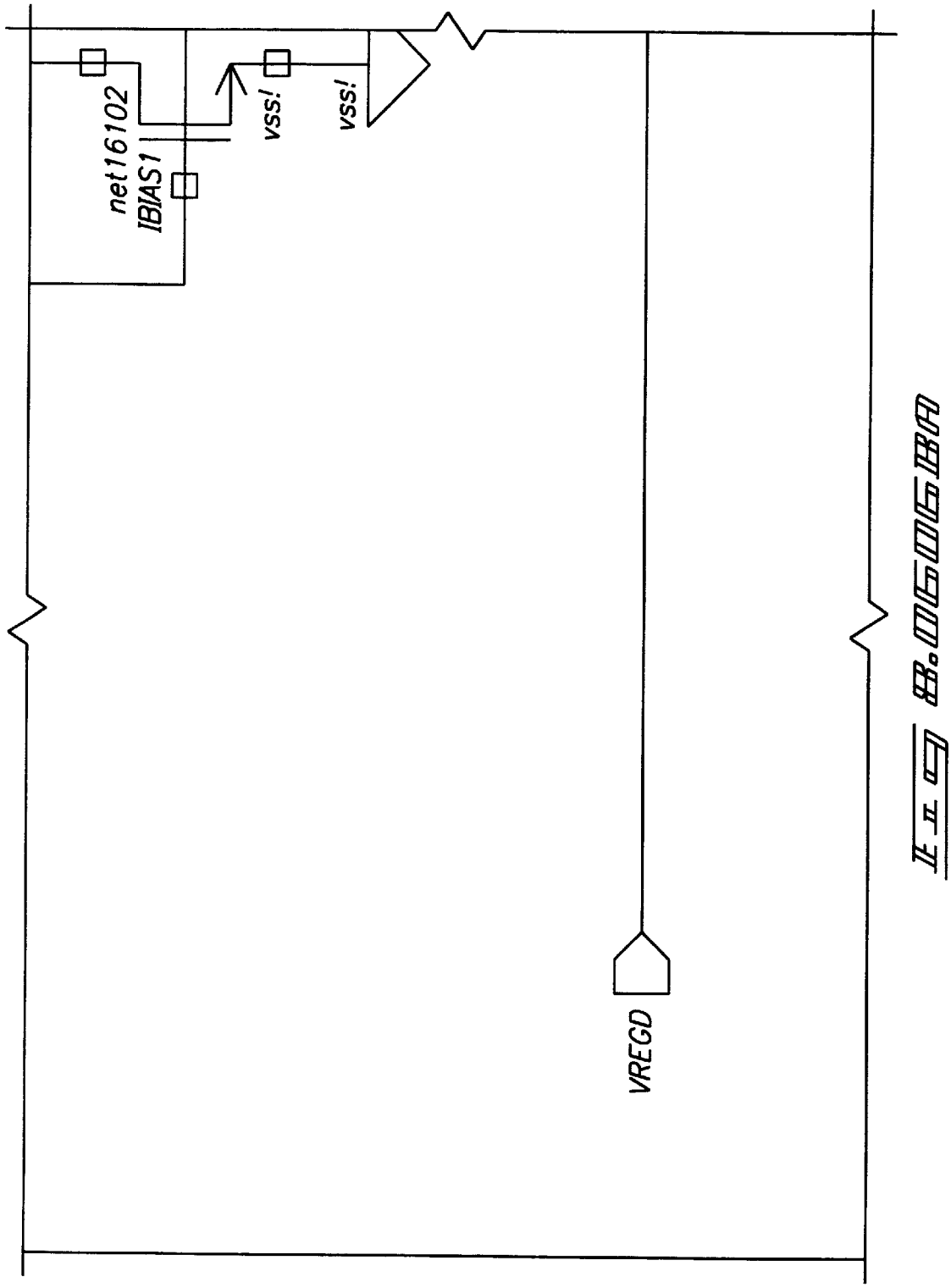


FIG 8.0656BA

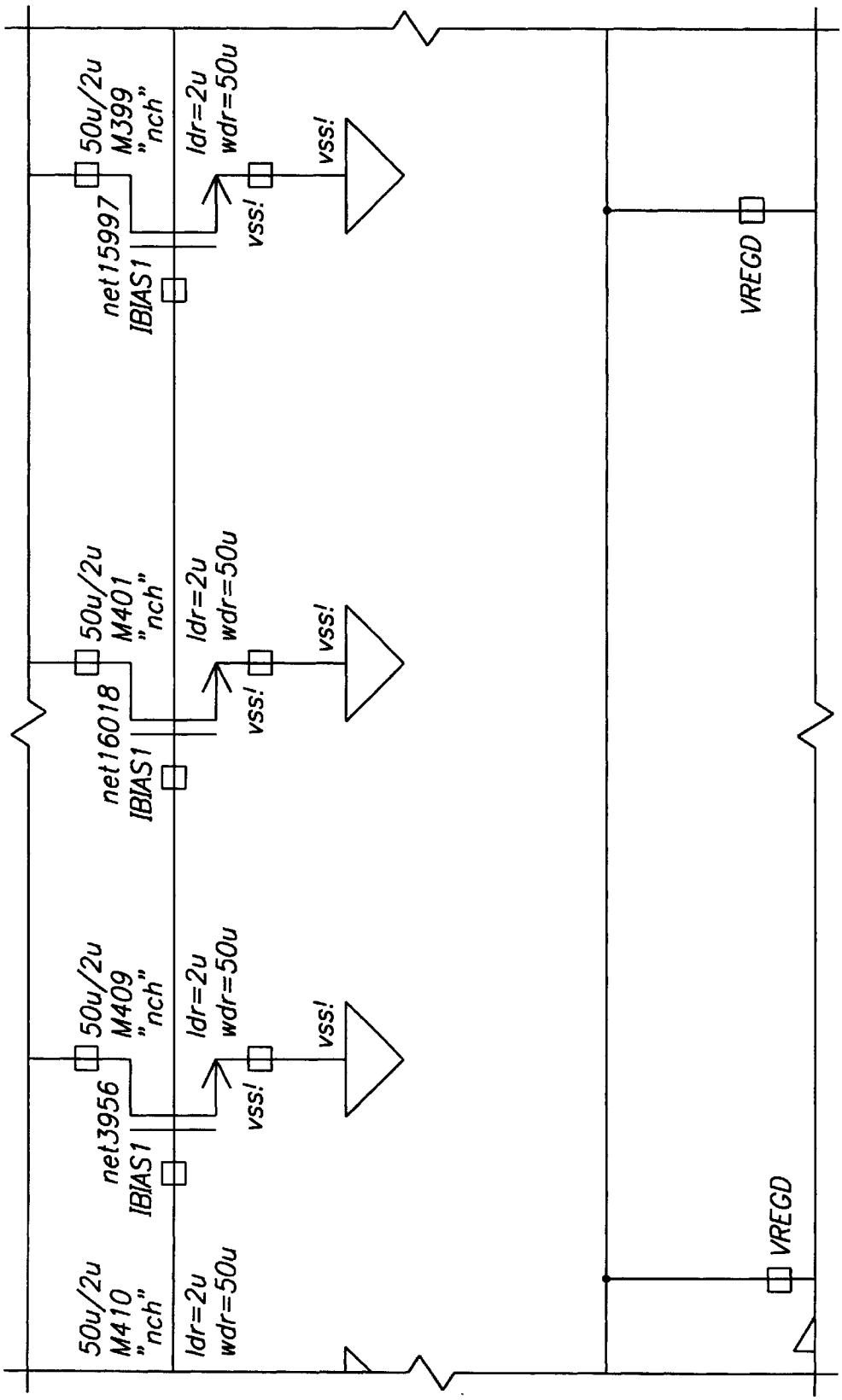

50u/2u
M399
"nch"
ldr=2u
wdr=50u
vss!
net15997
IBIAS1
VREGD
50u/2u
M401
"nch"
net16018
50u/2u
M409
"nch"
net3956
50u/2u
M410
"nch"
VREGD

FIG. 8.005

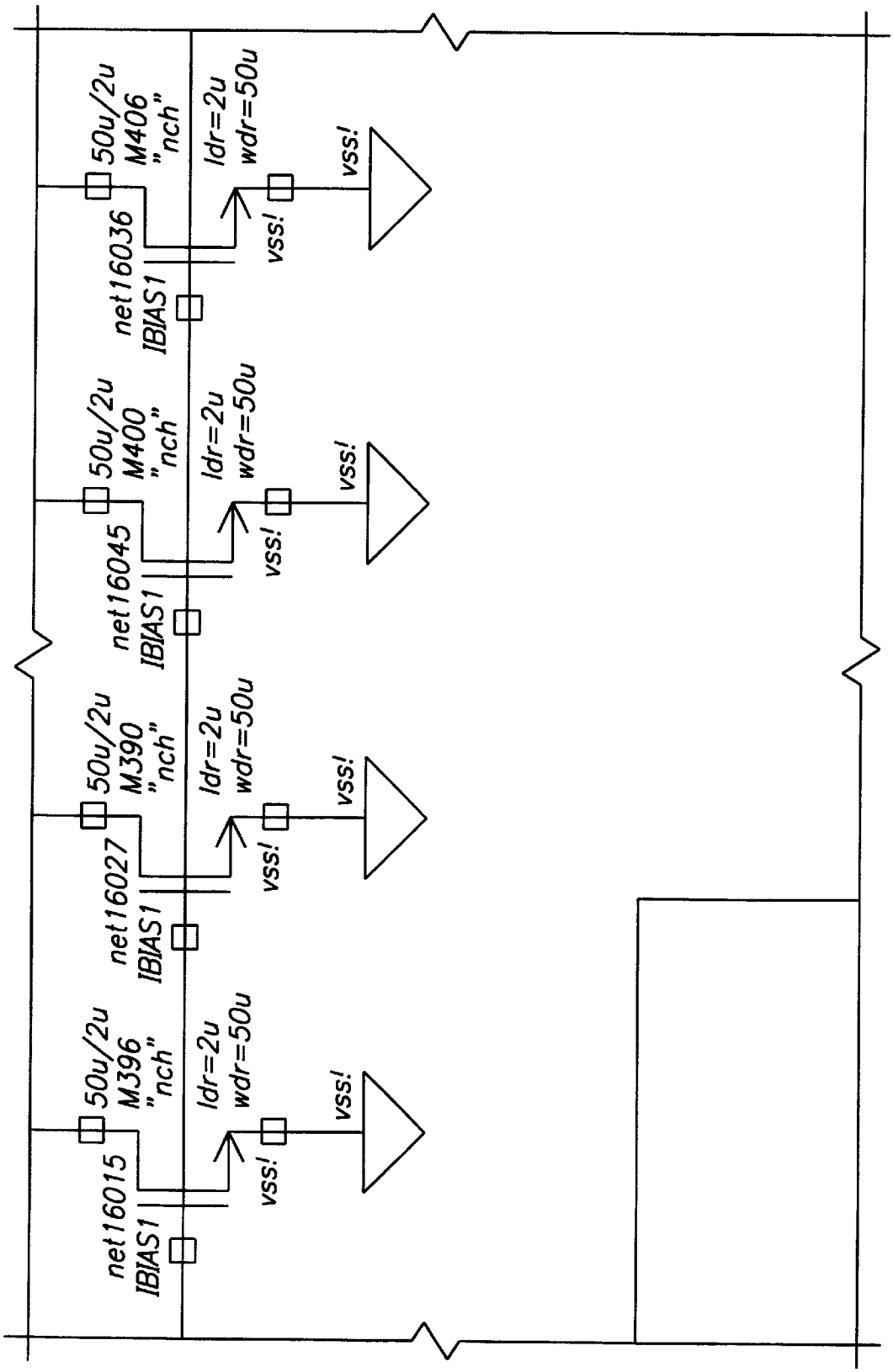


FIG. 8.0606IBIC

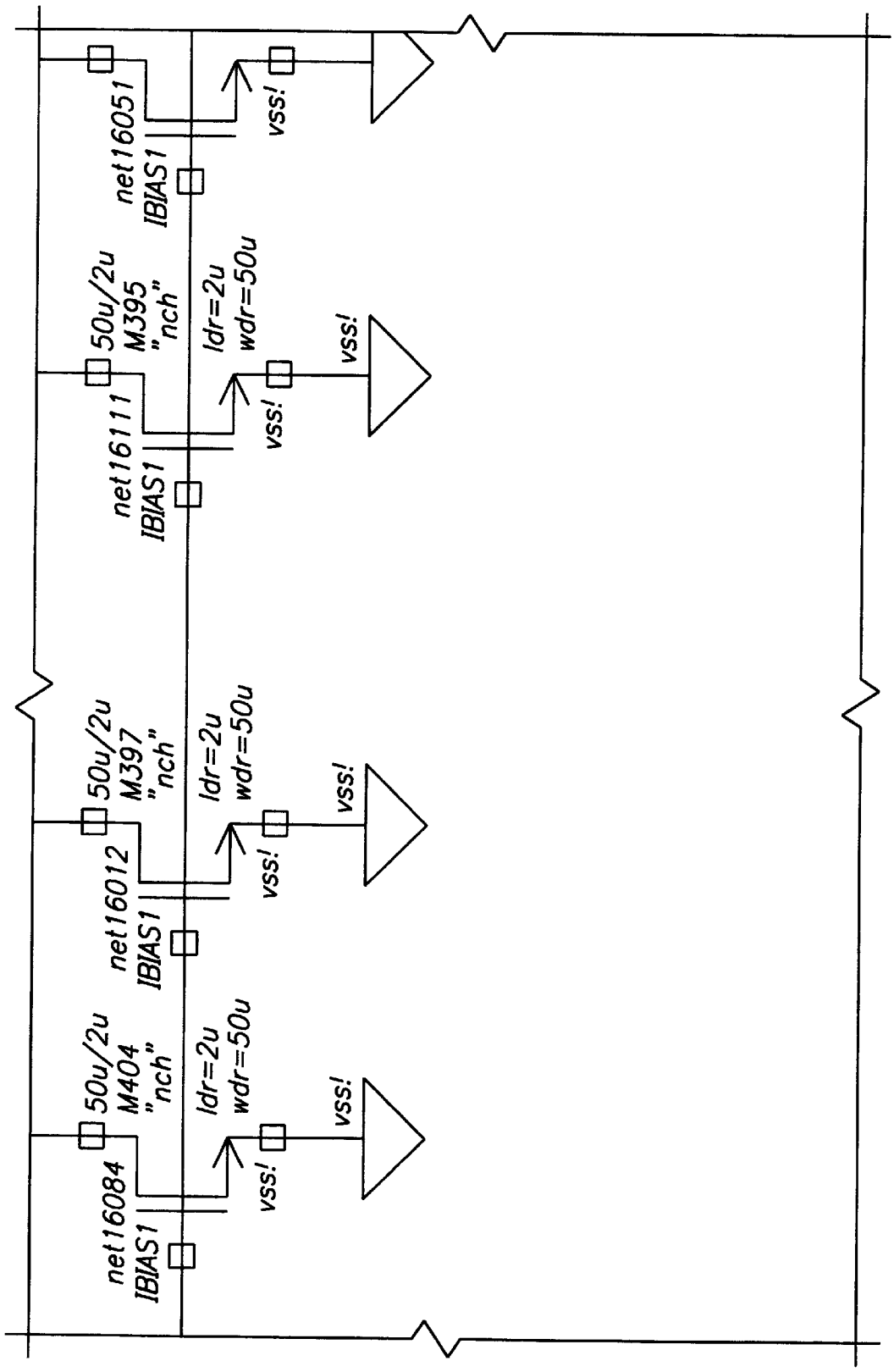


FIG 8.0059IBM

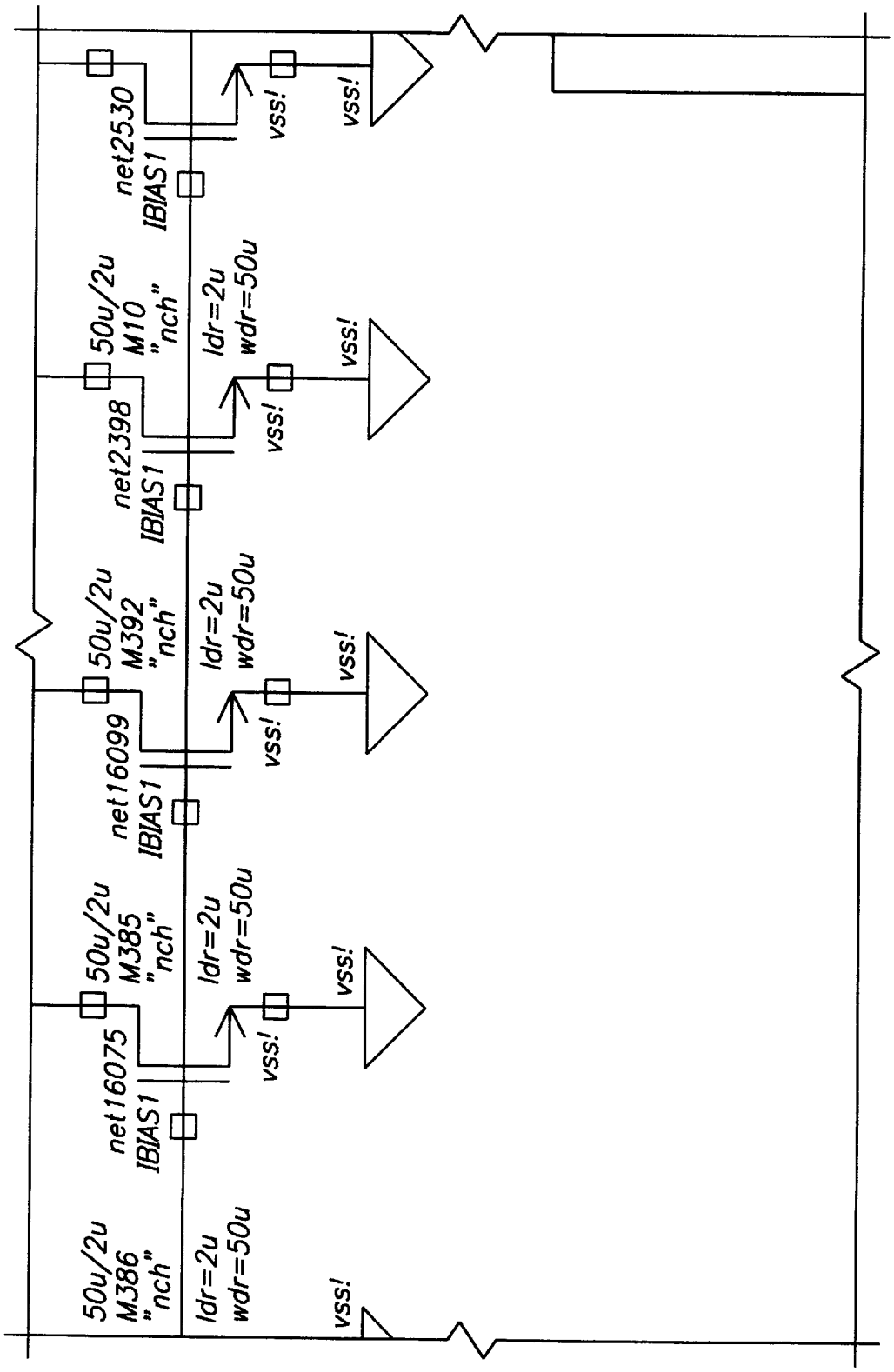


FIG. 8,065,IBIE

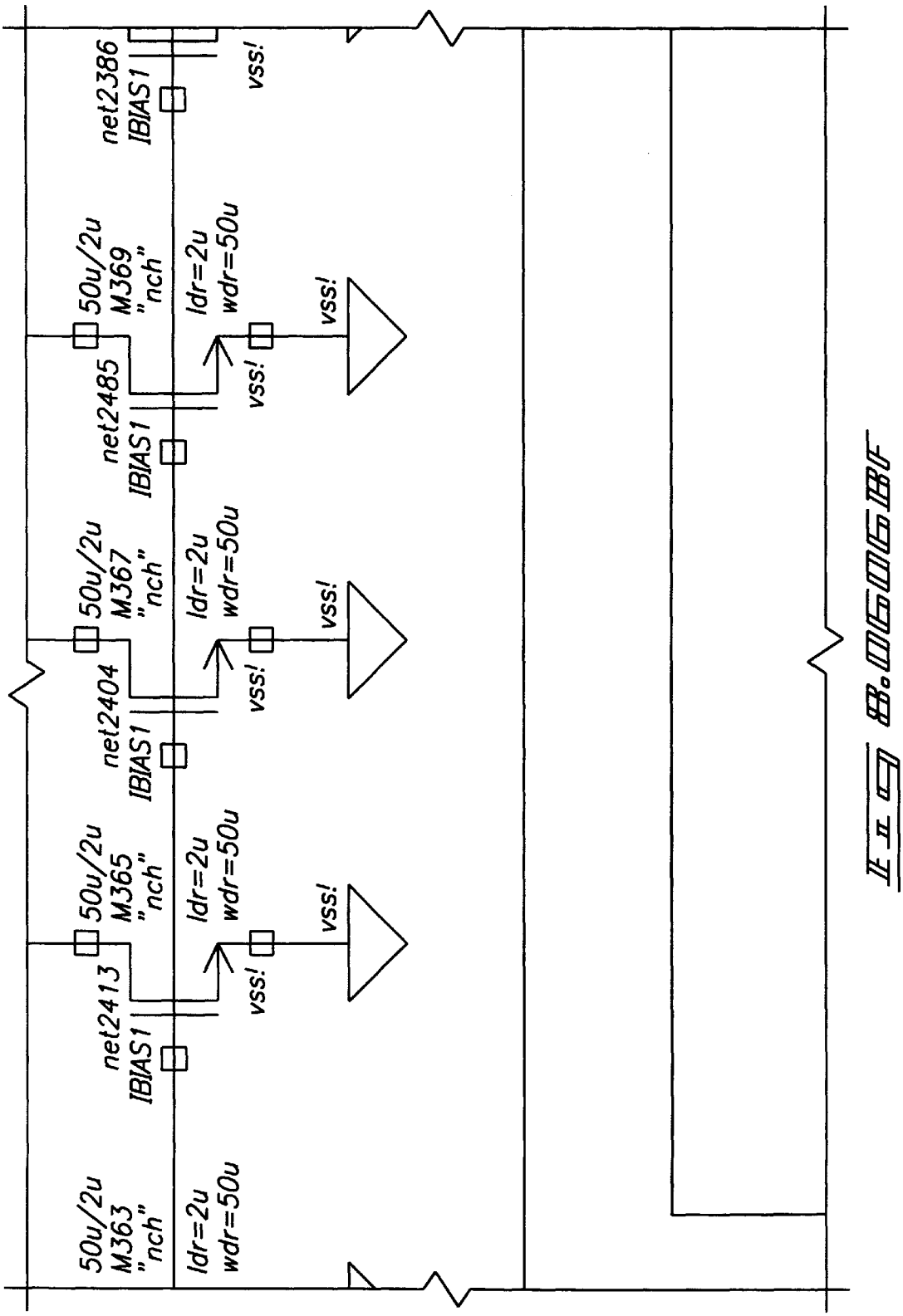


FIG 88.0S0S1BF

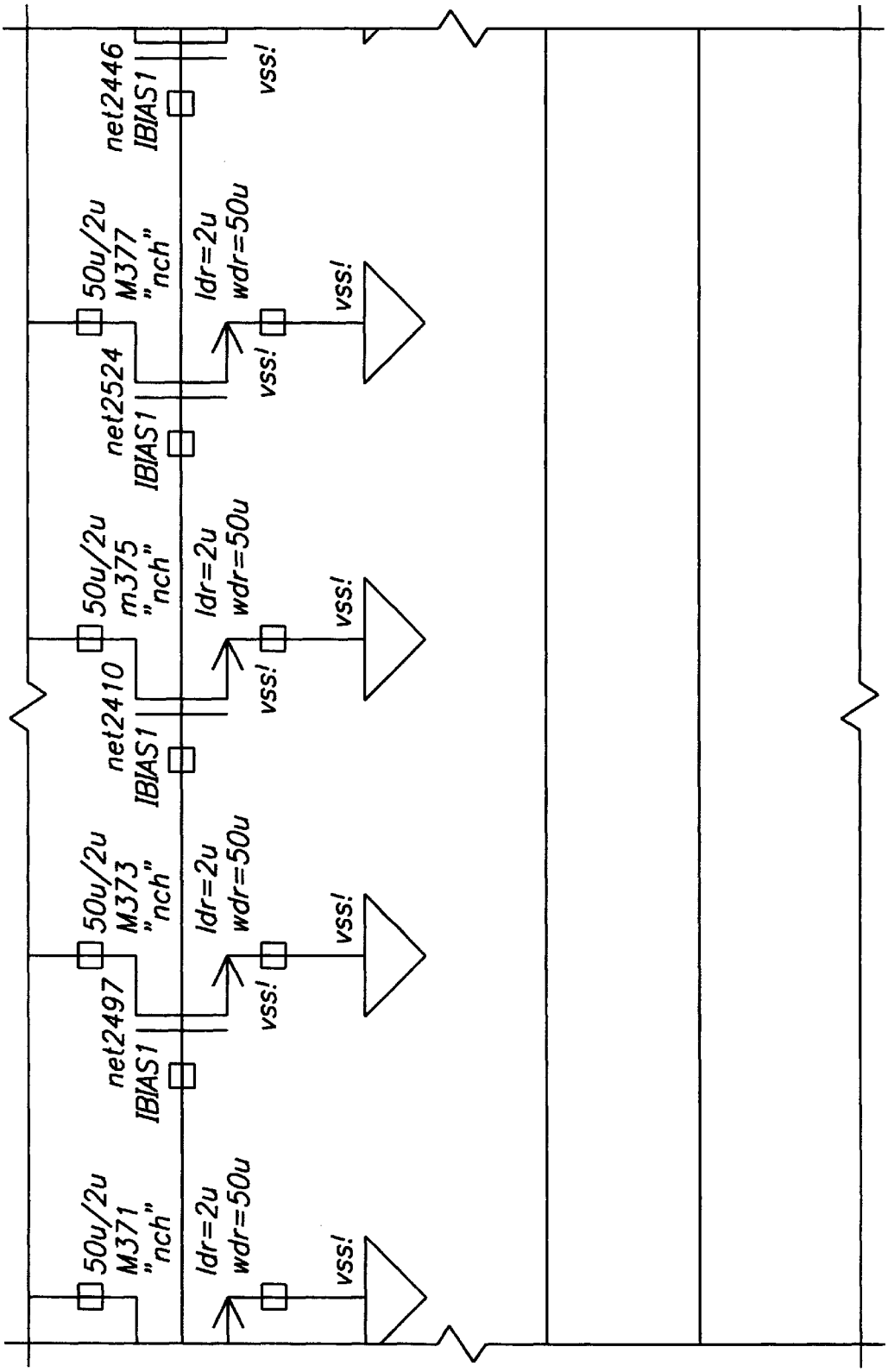

50u/2u
M371
"nch"
ldr=2u
wdr=50u
vss!
net2497
IBIAS1
50u/2u
M373
"nch"
ldr=2u
wdr=50u
vss!
net2410
IBIAS1
50u/2u
m375
"nch"
ldr=2u
wdr=50u
vss!
net2524
IBIAS1
50u/2u
M377
"nch"
ldr=2u
wdr=50u
vss!
net2446
IBIAS1
vss!

FIG. 6,006,186

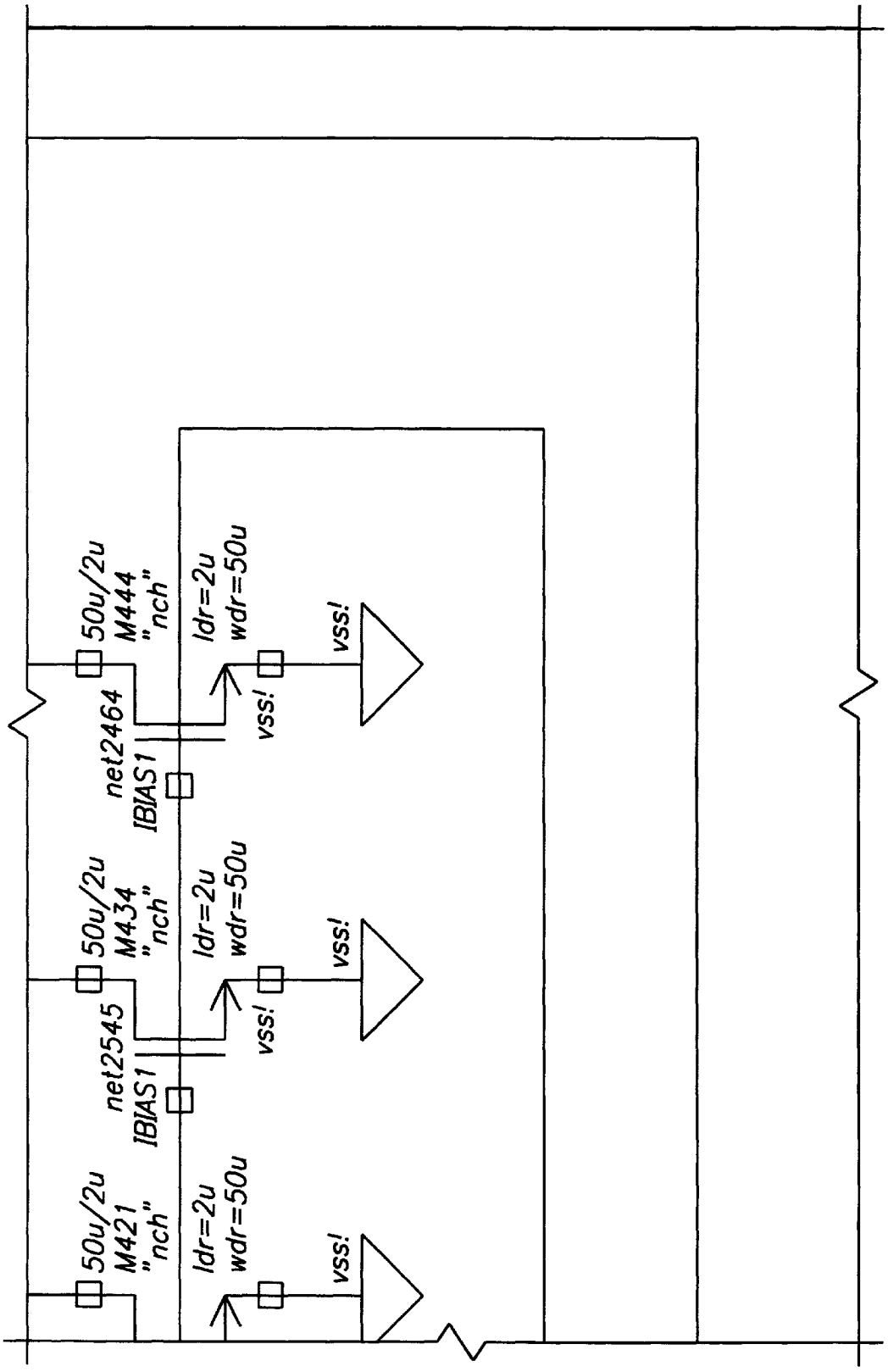
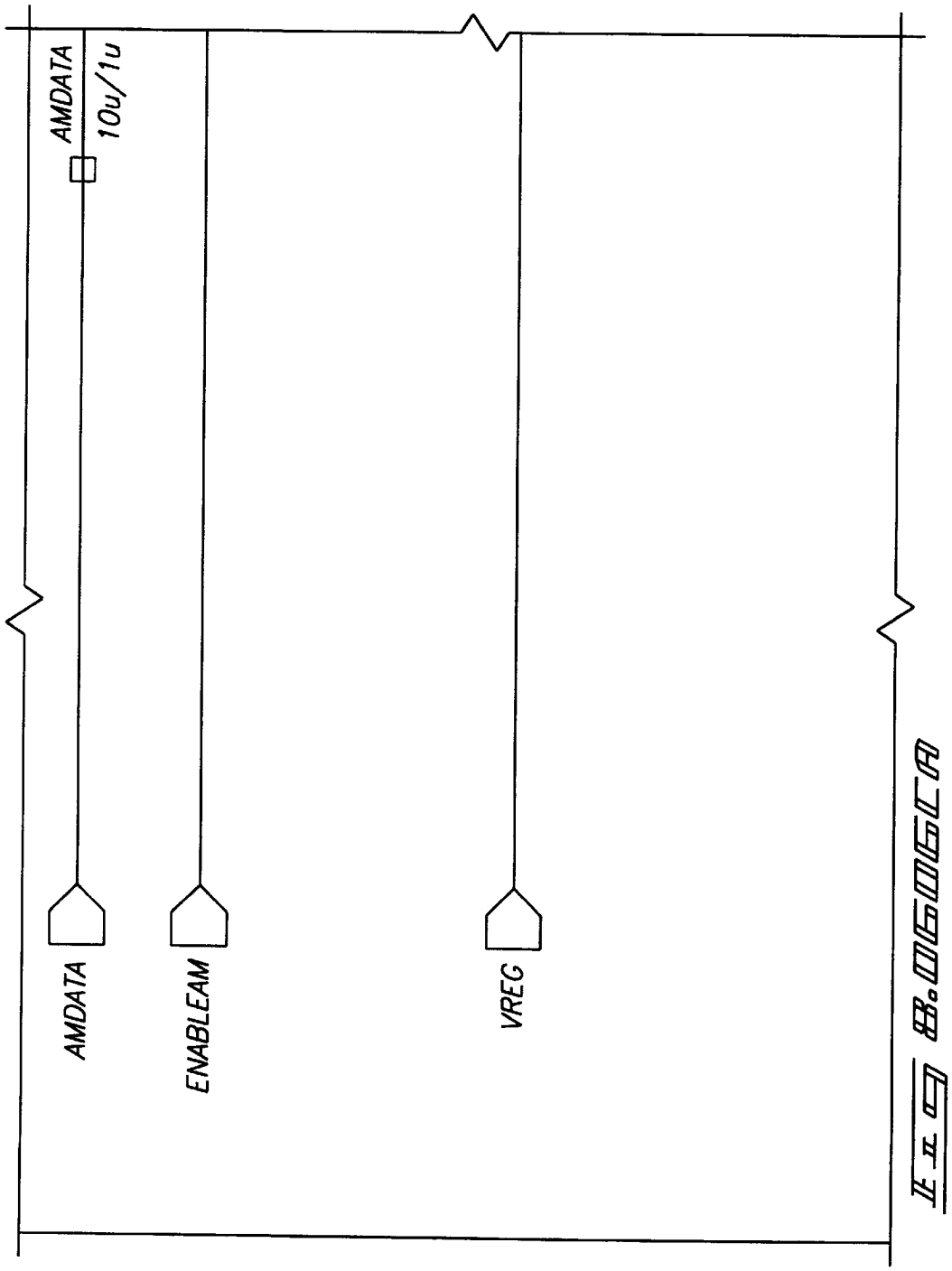

50u/2u
M444
"nch"
ldr=2u
wdr=50u
vss!
net2464
IBIAS1
50u/2u
M434
"nch"
ldr=2u
wdr=50u
vss!
net2545
IBIAS1
50u/2u
M421
"nch"
ldr=2u
wdr=50u
vss!

FIG. 88.0059


AMDATA
10u/1u
AMDATA
ENABLEAM
VREG
88.0650CA

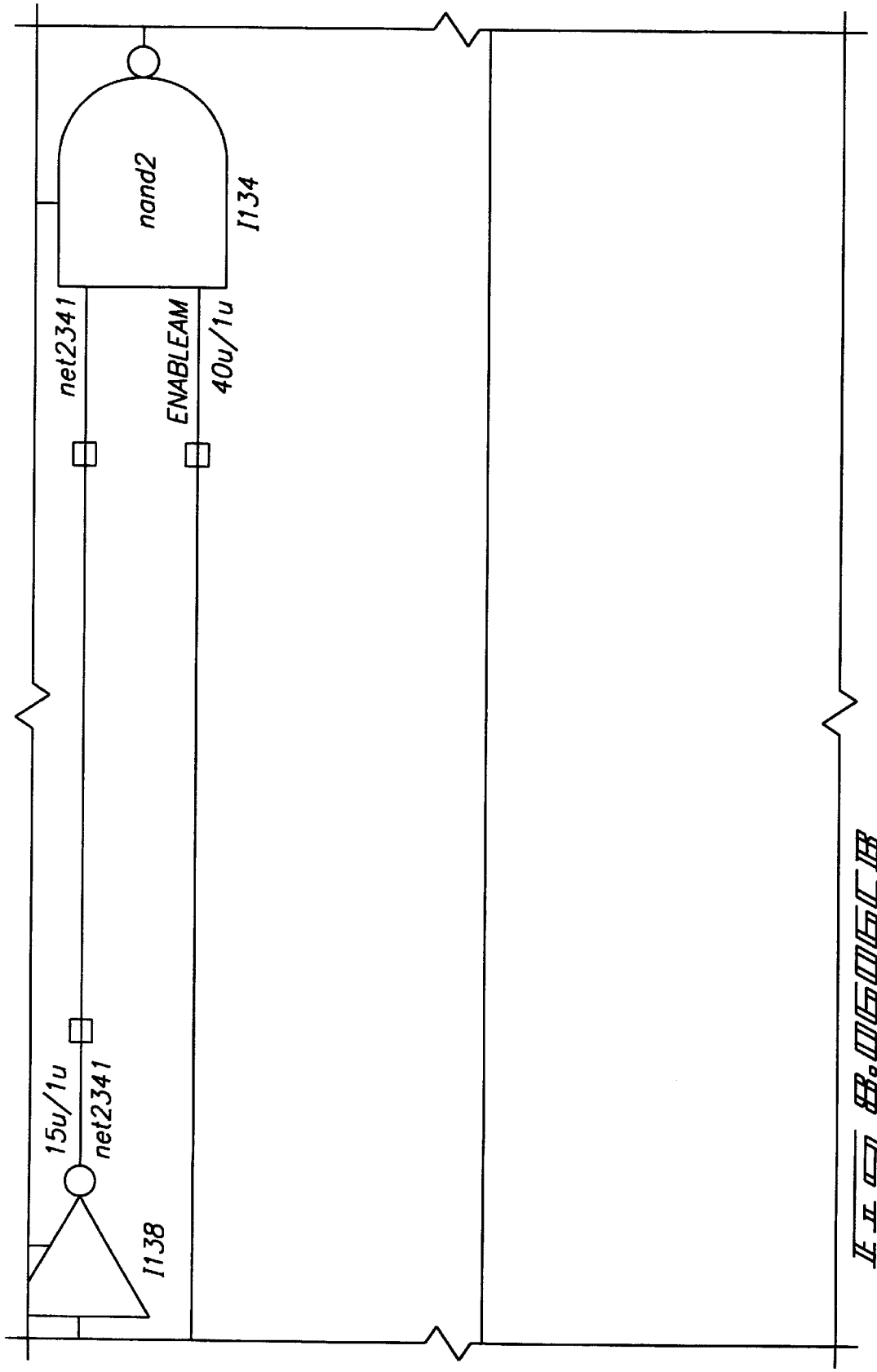


FIG 8,050,038

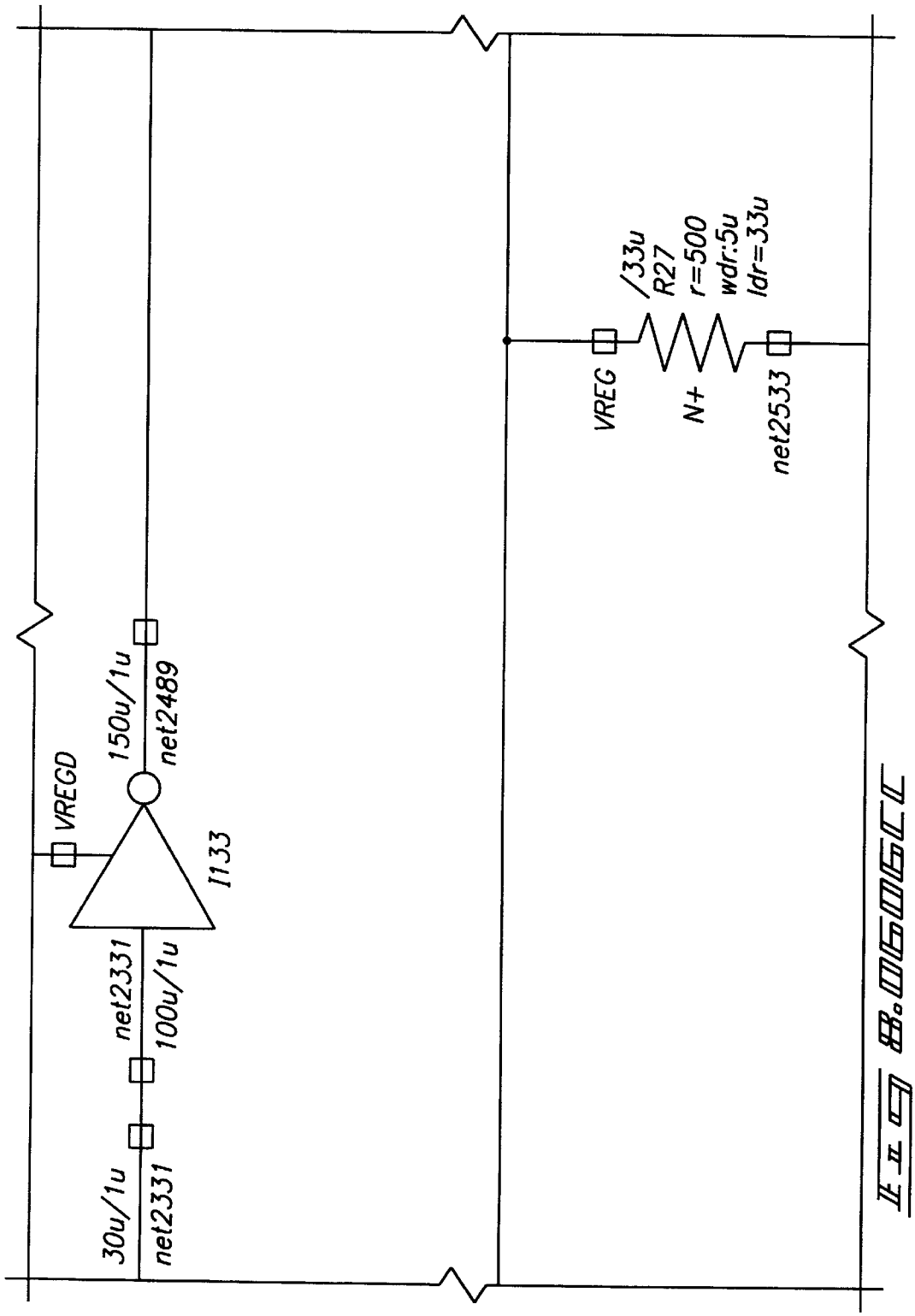

/33u
R27
r=500
wdr:5u
ldr=33u
VREG
N+
net2533
150u/1u
net2489
VREGD
I133
net2331
100u/1u
30u/1u
net2331

FIG 8.0050

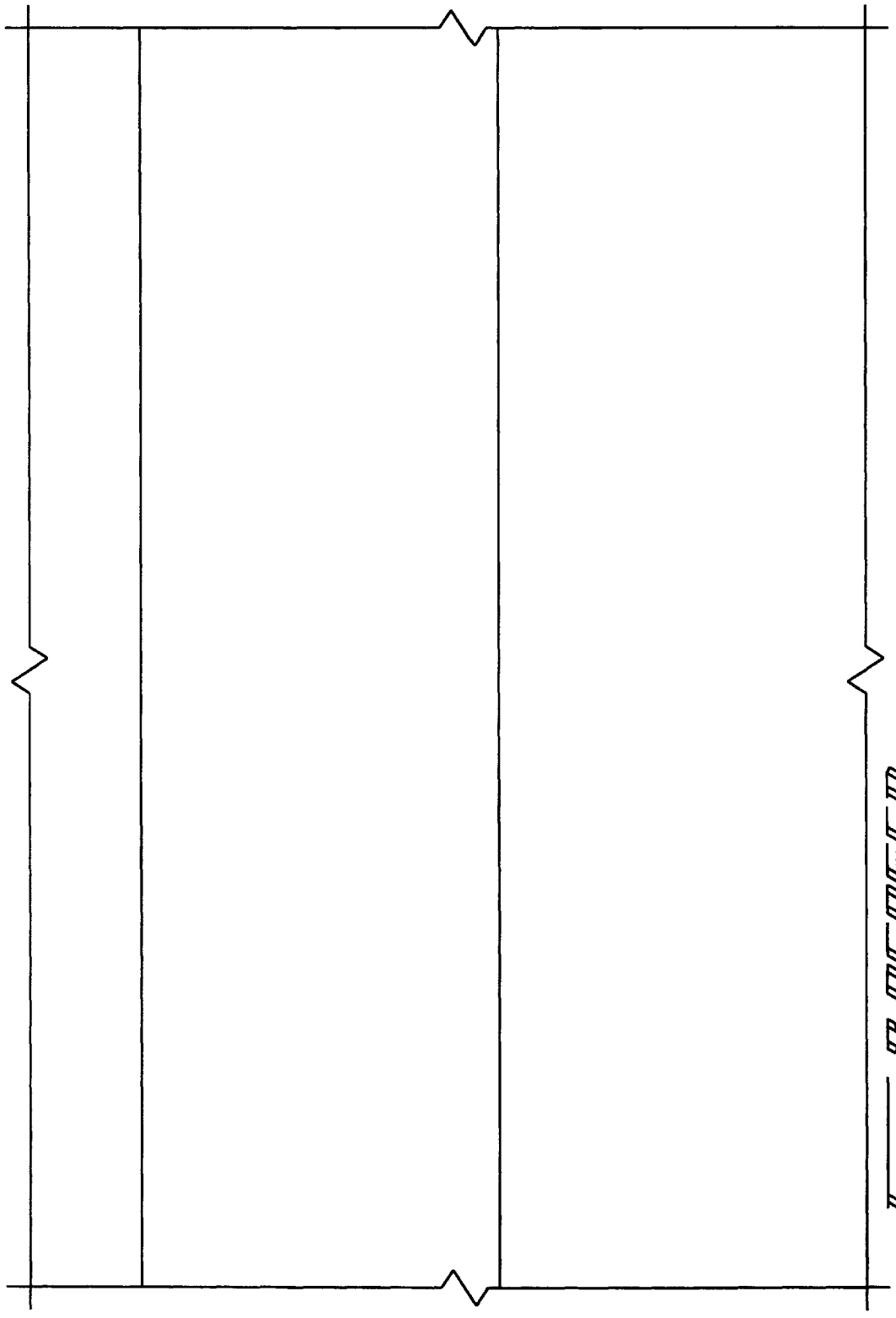
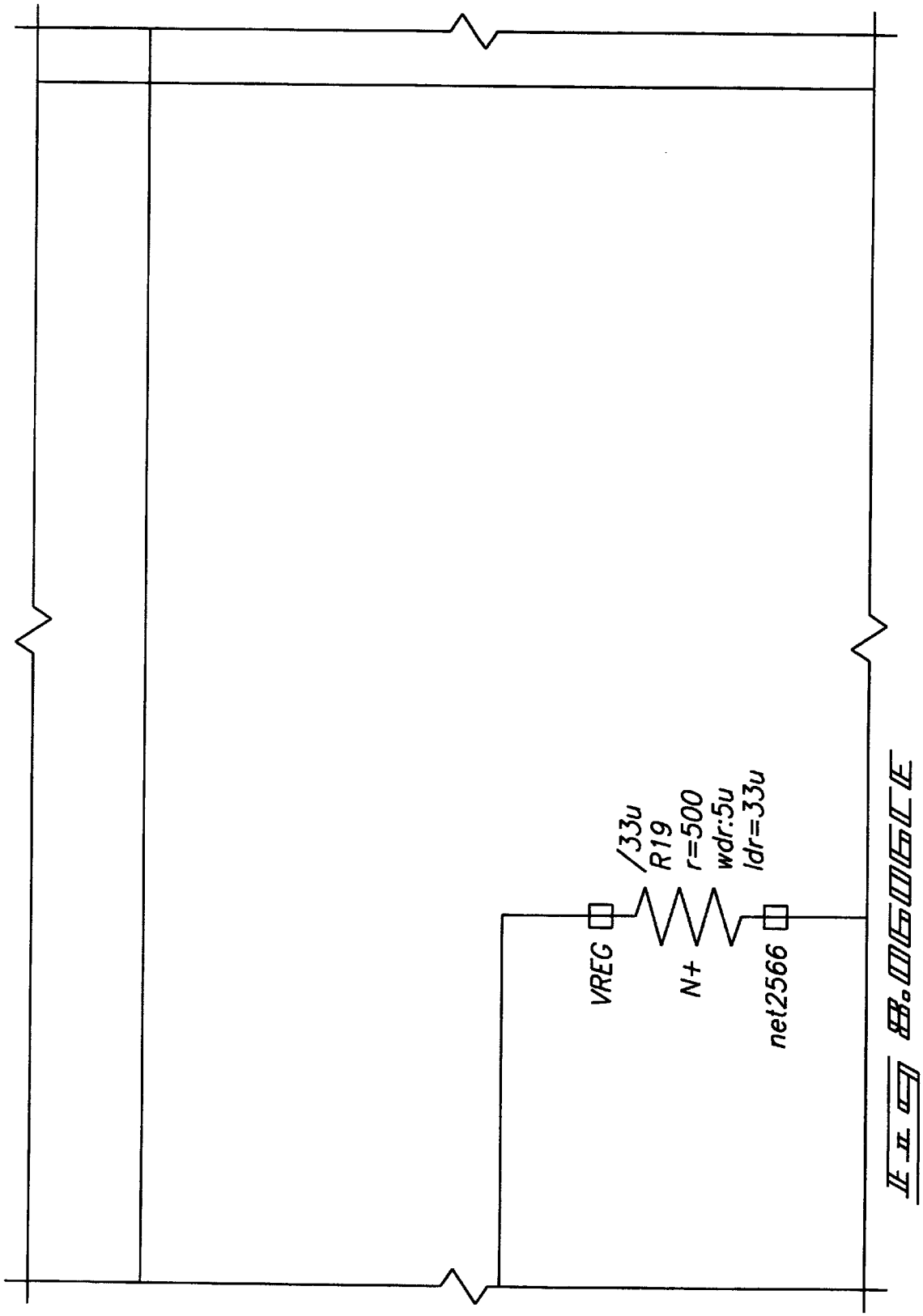


FIG 8,060,010


/33u
R19
r=500
wdr:5u
ldr=33u
VREG
N+
net2566

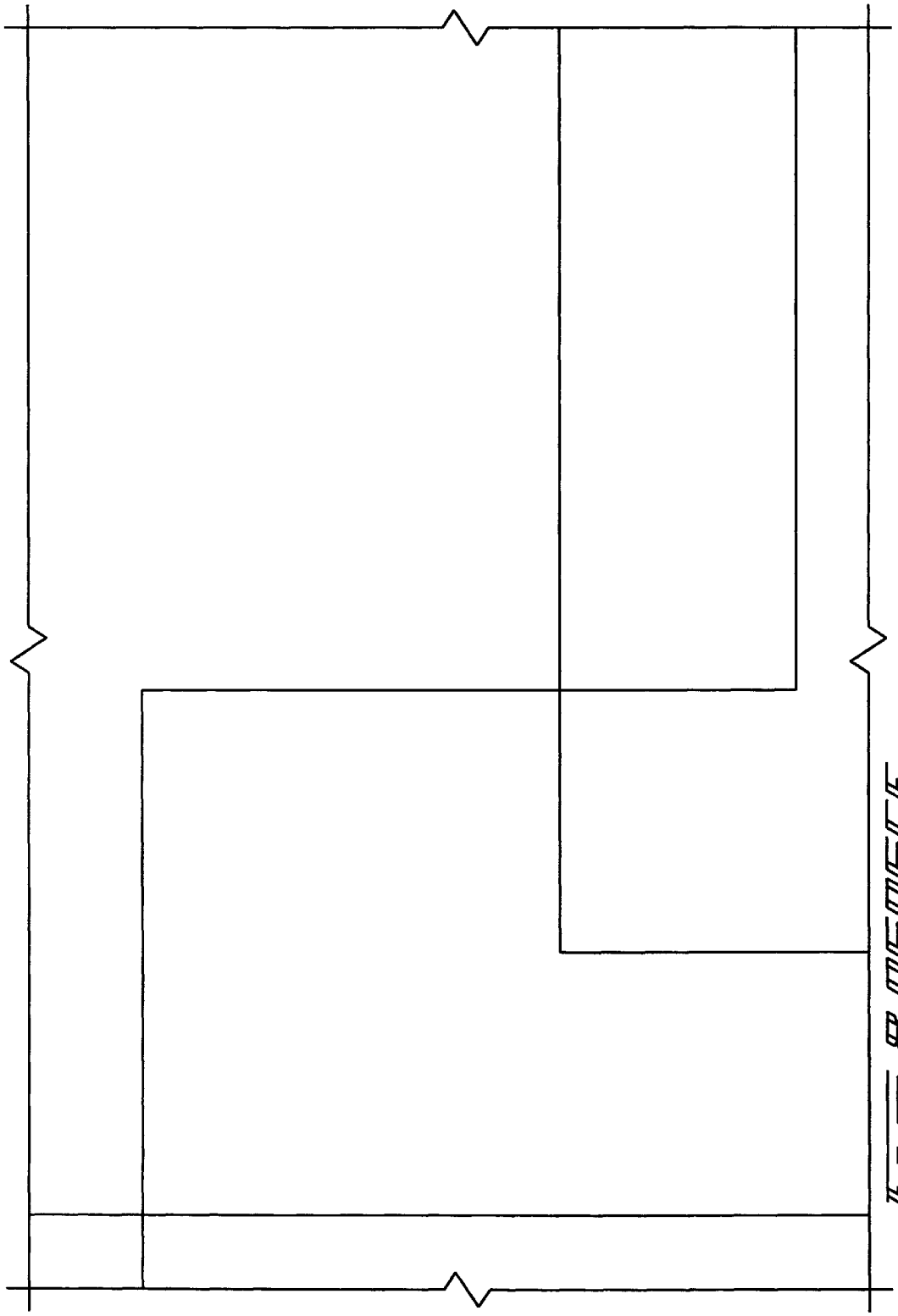


FIG. 98,056F

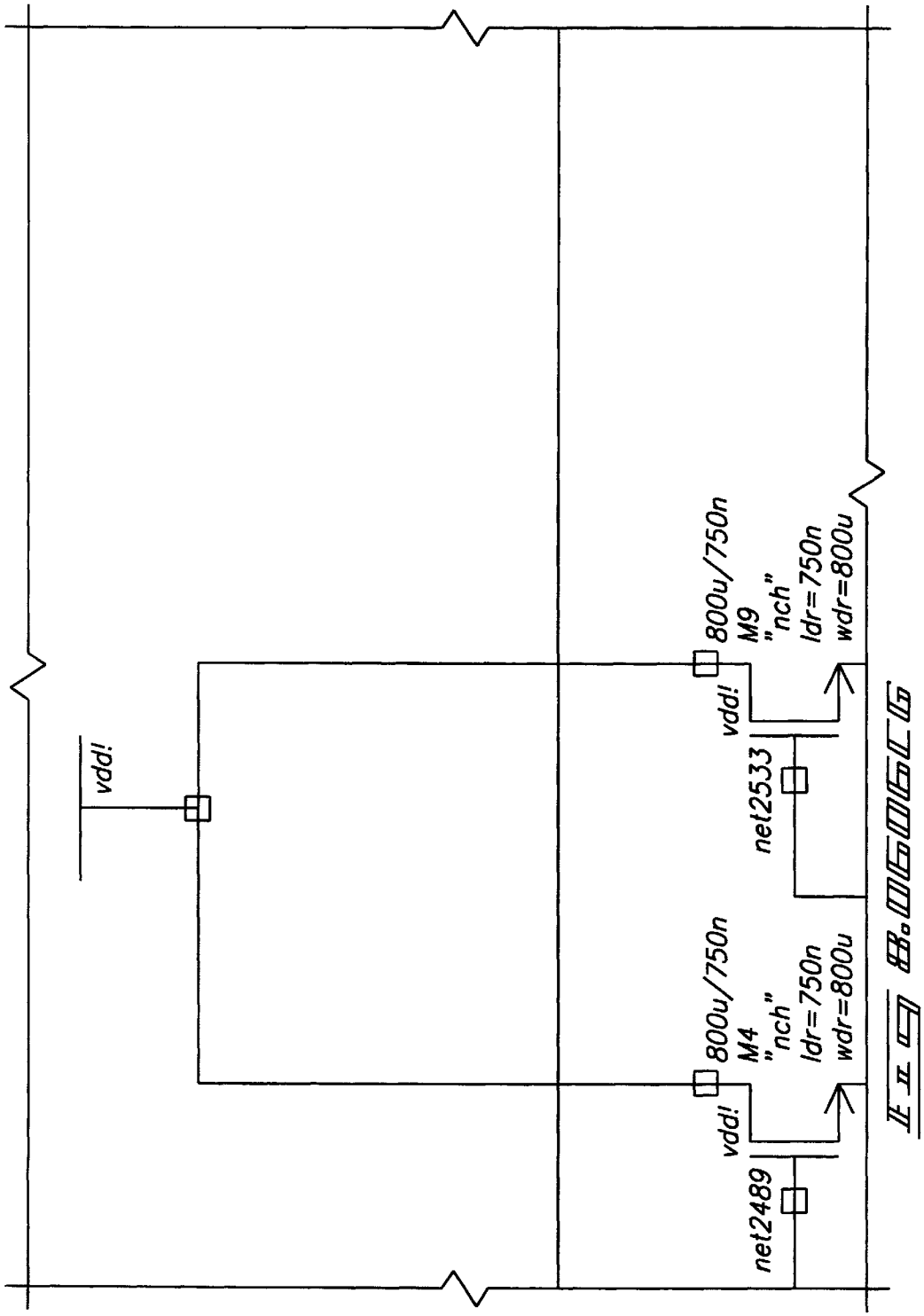
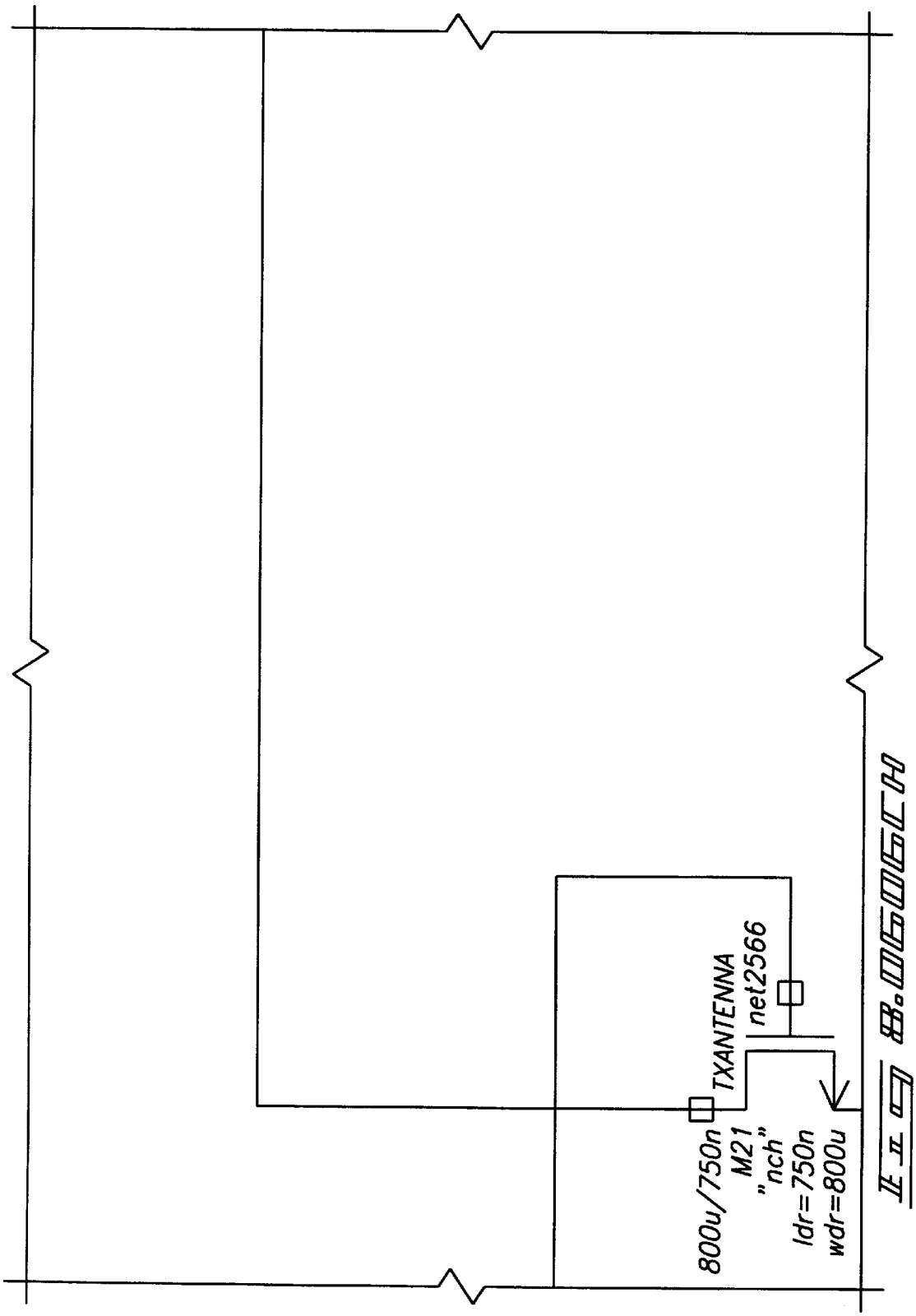


FIG. 88,005,978


TXANTENNA
net2566
800u/750n
M21
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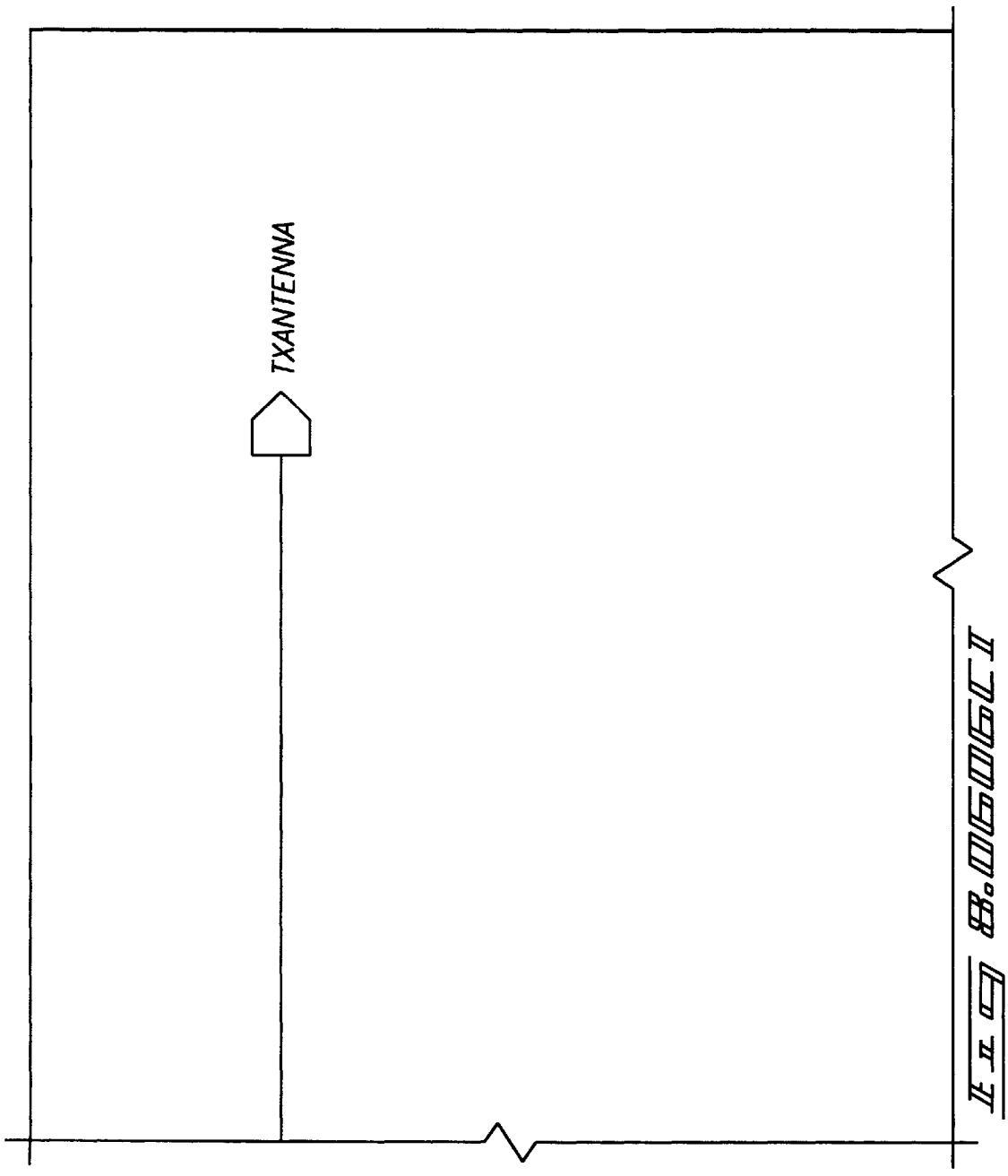
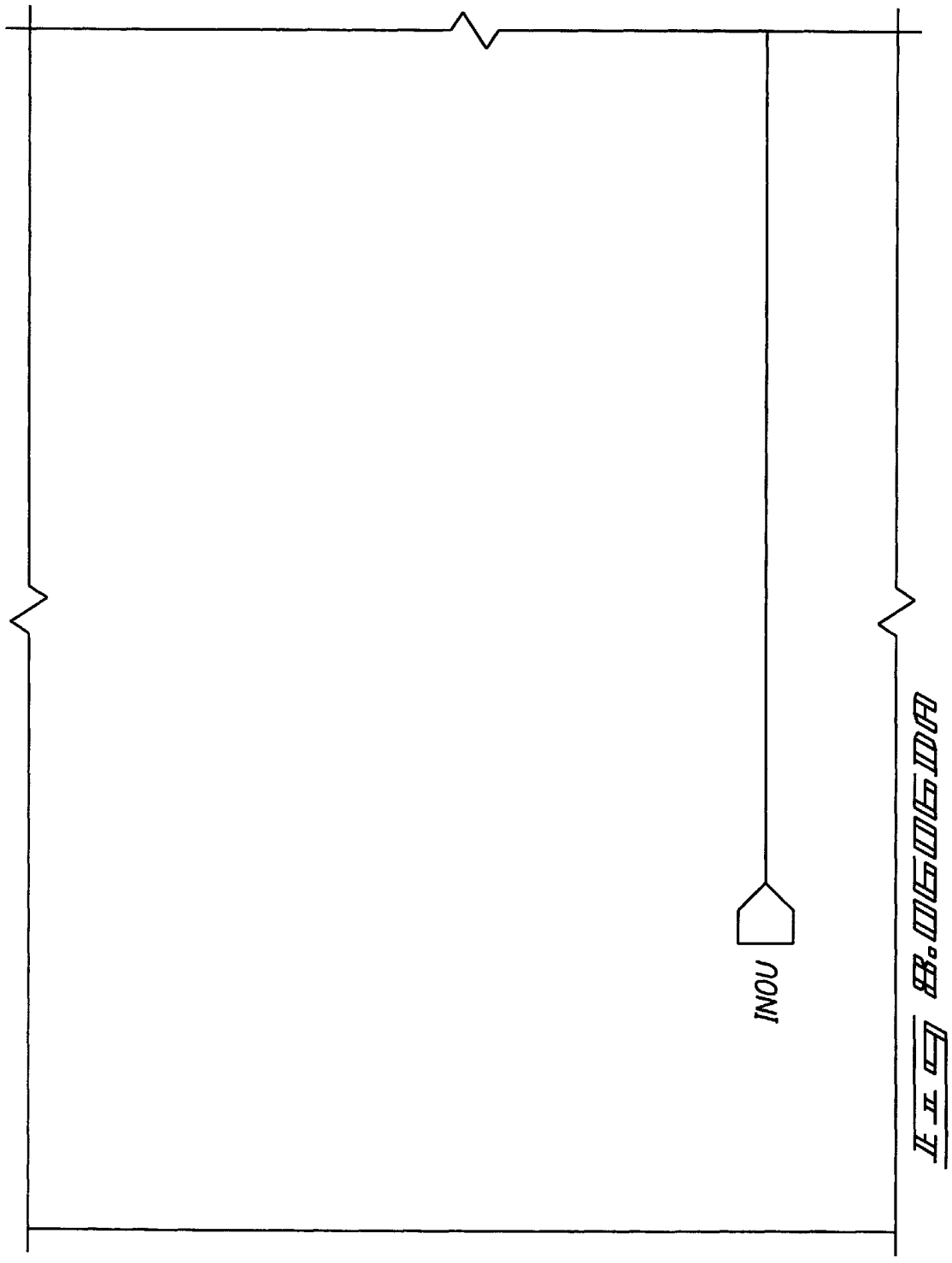
ldr=750n
wdr=800u


TXANTENNA
FIG 8.0650 II


INOU
FIG. 8,050

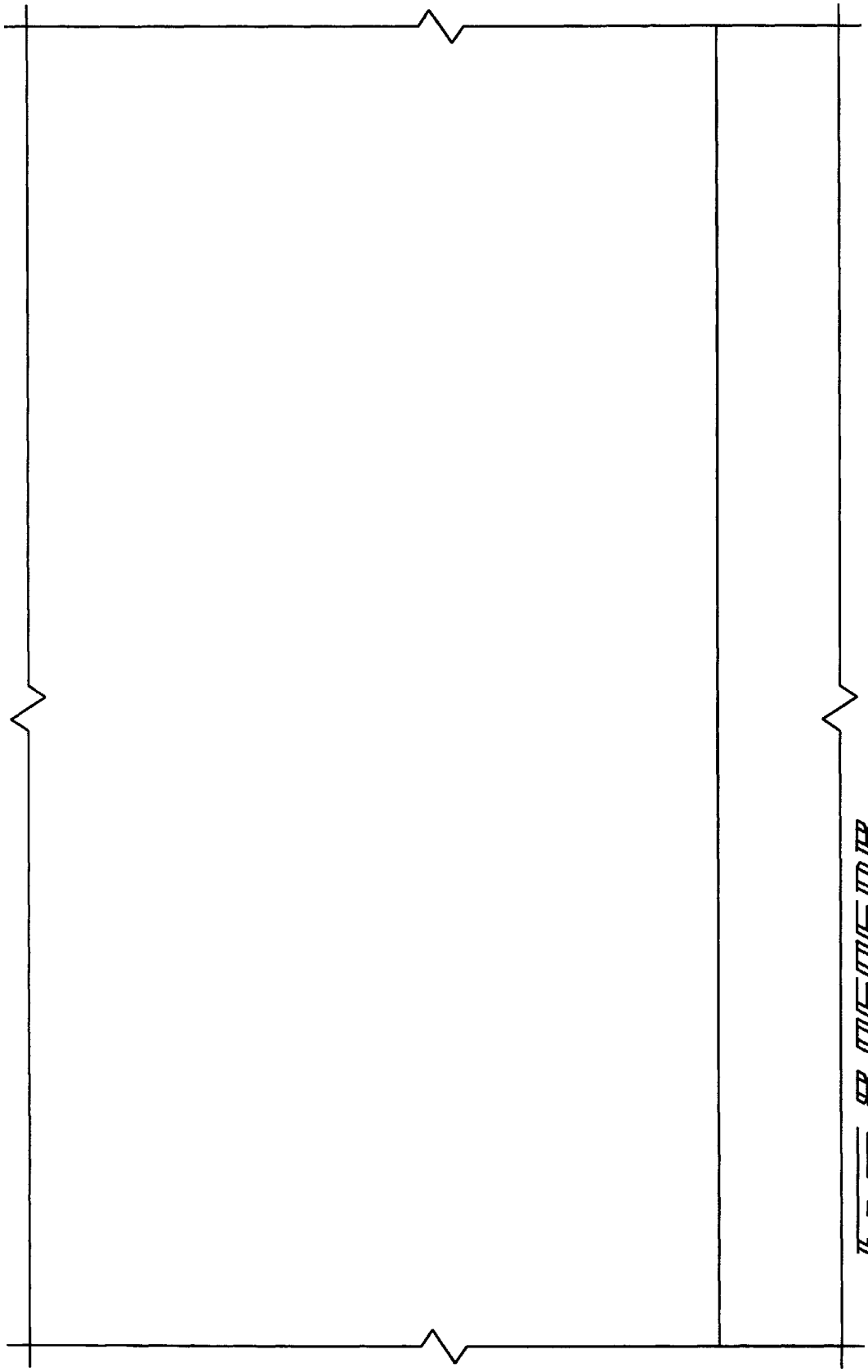


FIG. 88,005

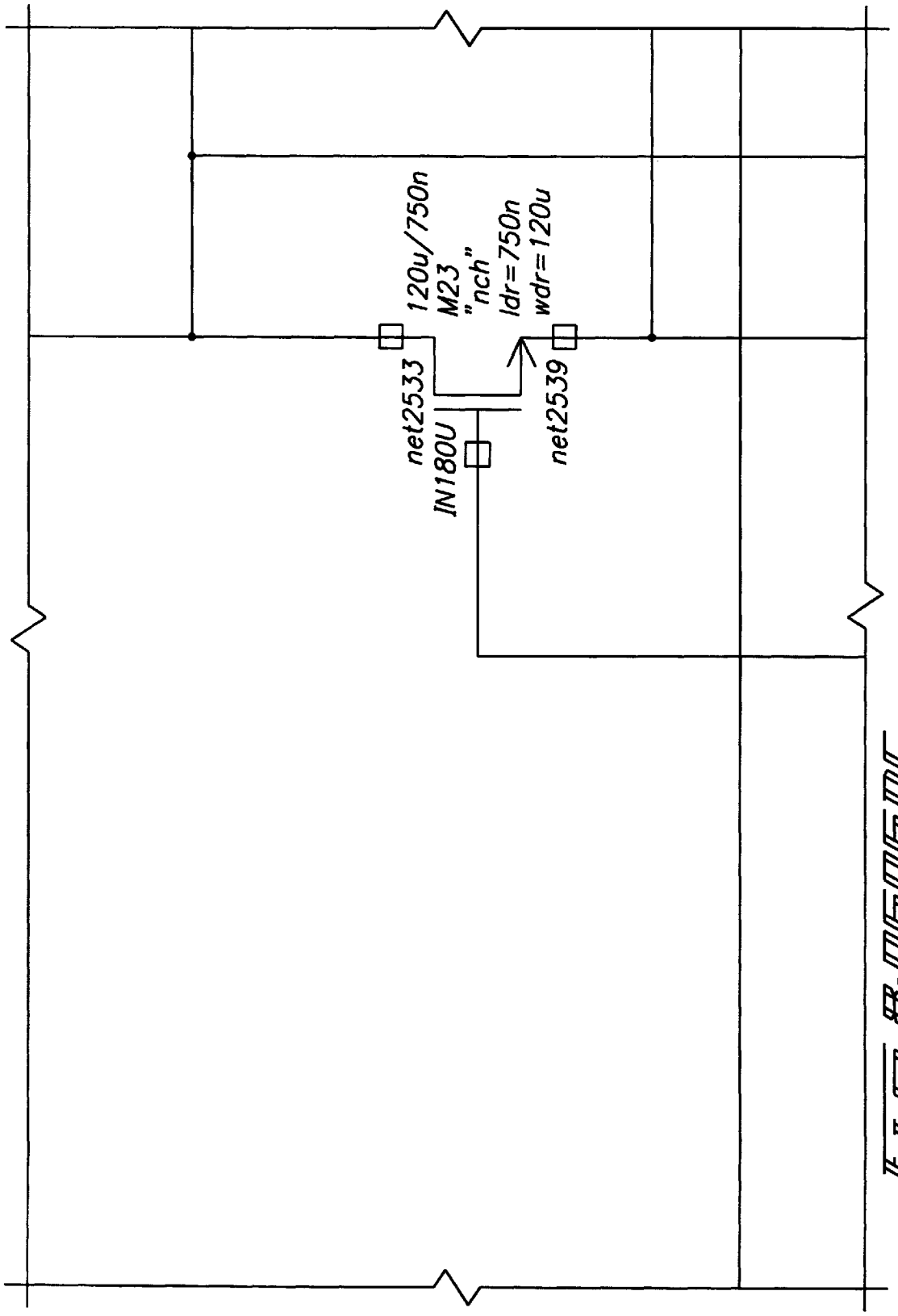


FIG 8.0606DC

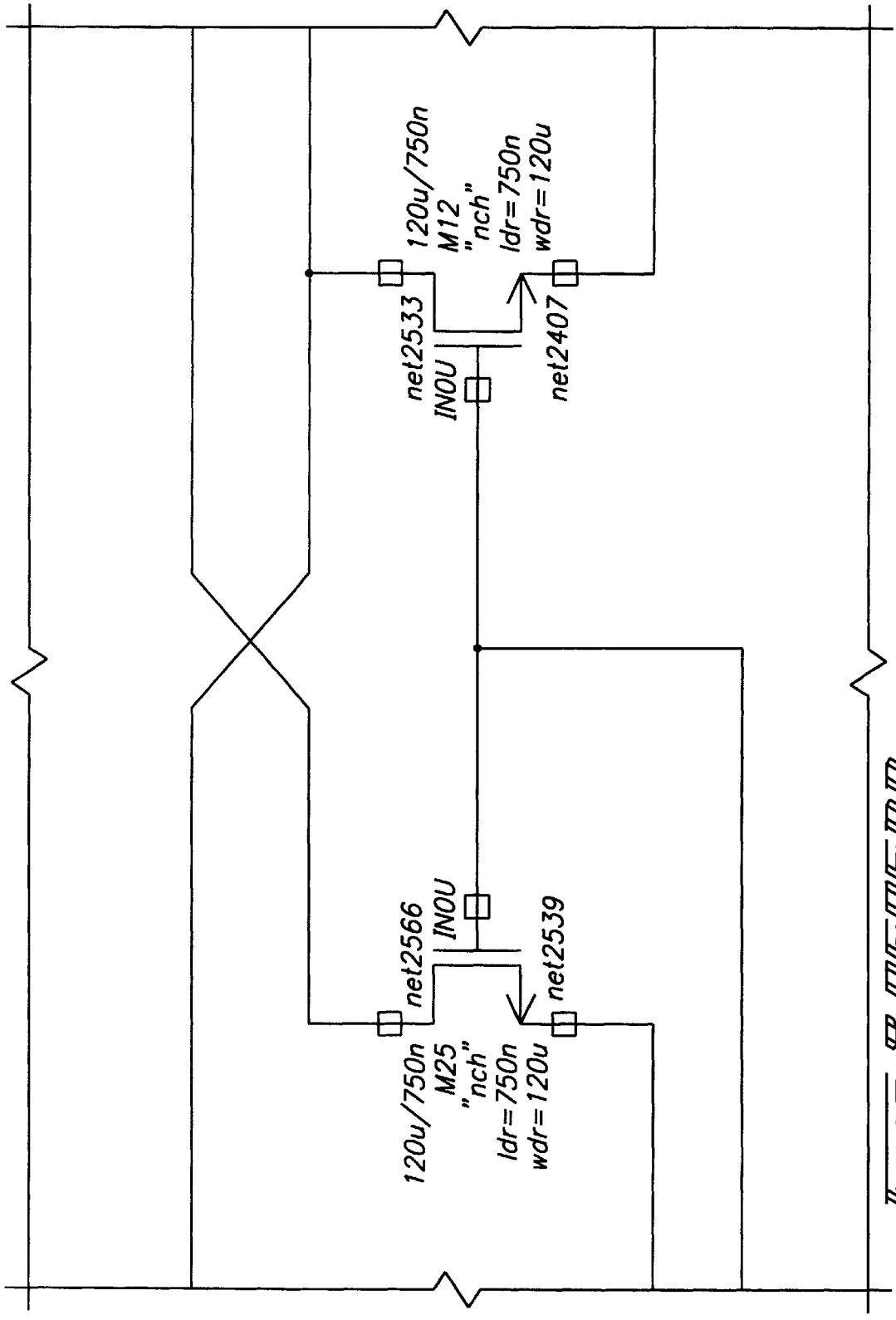

120u/750n
M12
"nch"
ldr=750n
wdr=120u
net2533
IN0U
net2407
net2566
IN0U
net2539
120u/750n
M25
"nch"
ldr=750n
wdr=120u

FIG 8,056,010

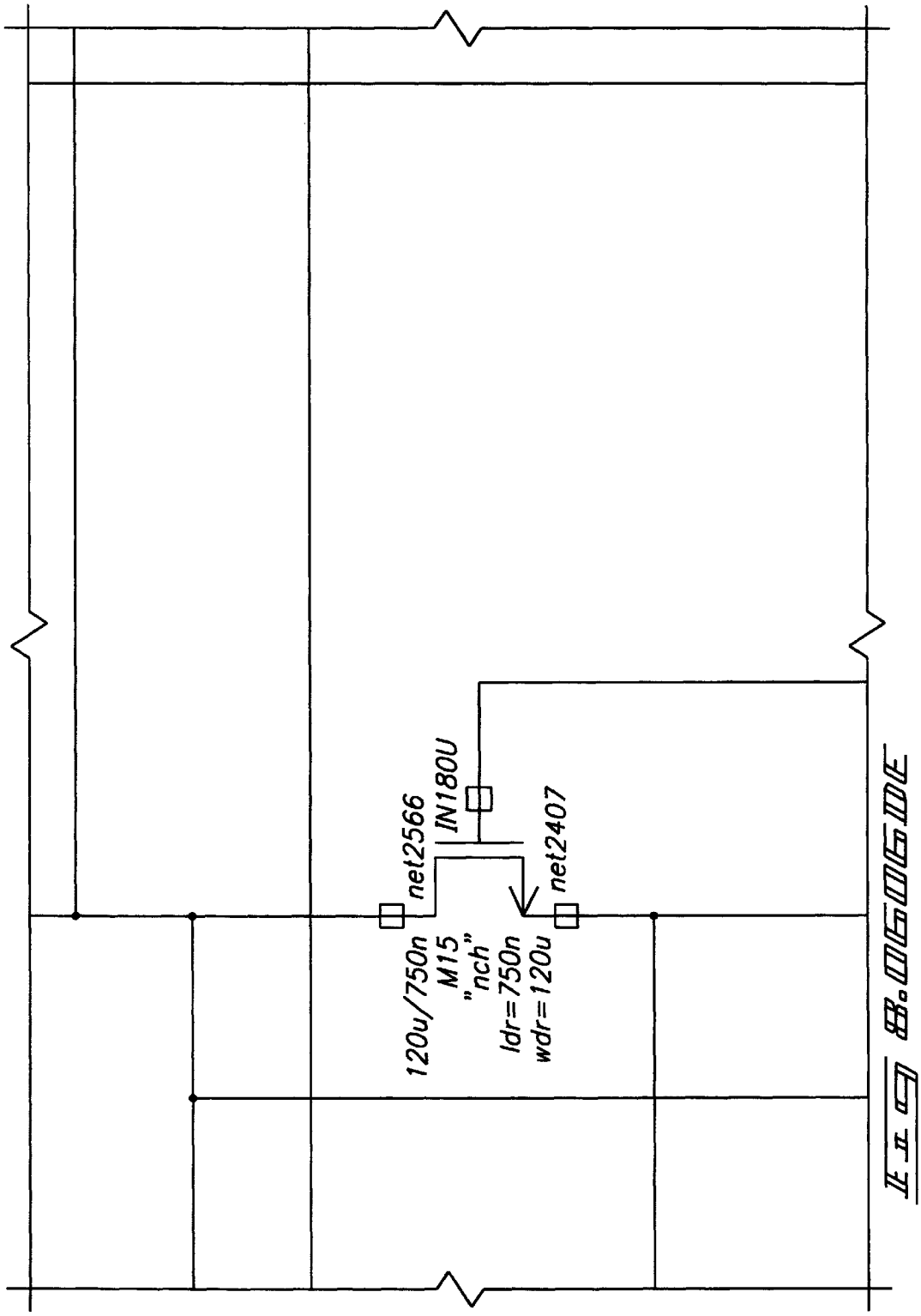


FIG 88.0560E

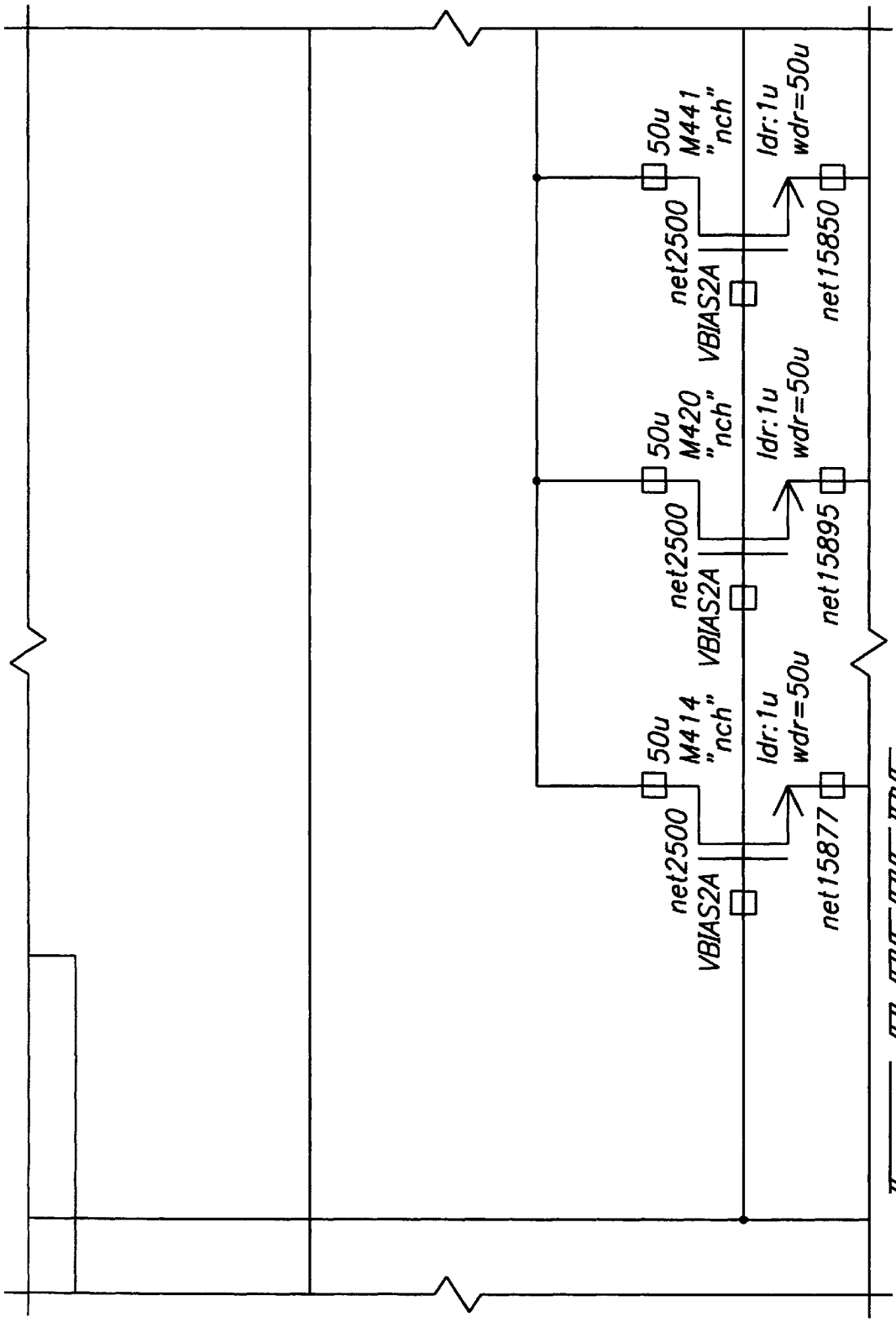

50u
M441
"nch"
ldr:1u
wdr=50u
net2500
VBIAS2A
net15850
50u
M420
"nch"
ldr:1u
wdr=50u
net2500
VBIAS2A
net15895
50u
M414
"nch"
ldr:1u
wdr=50u
net2500
VBIAS2A
net15877

FIG. 88.005

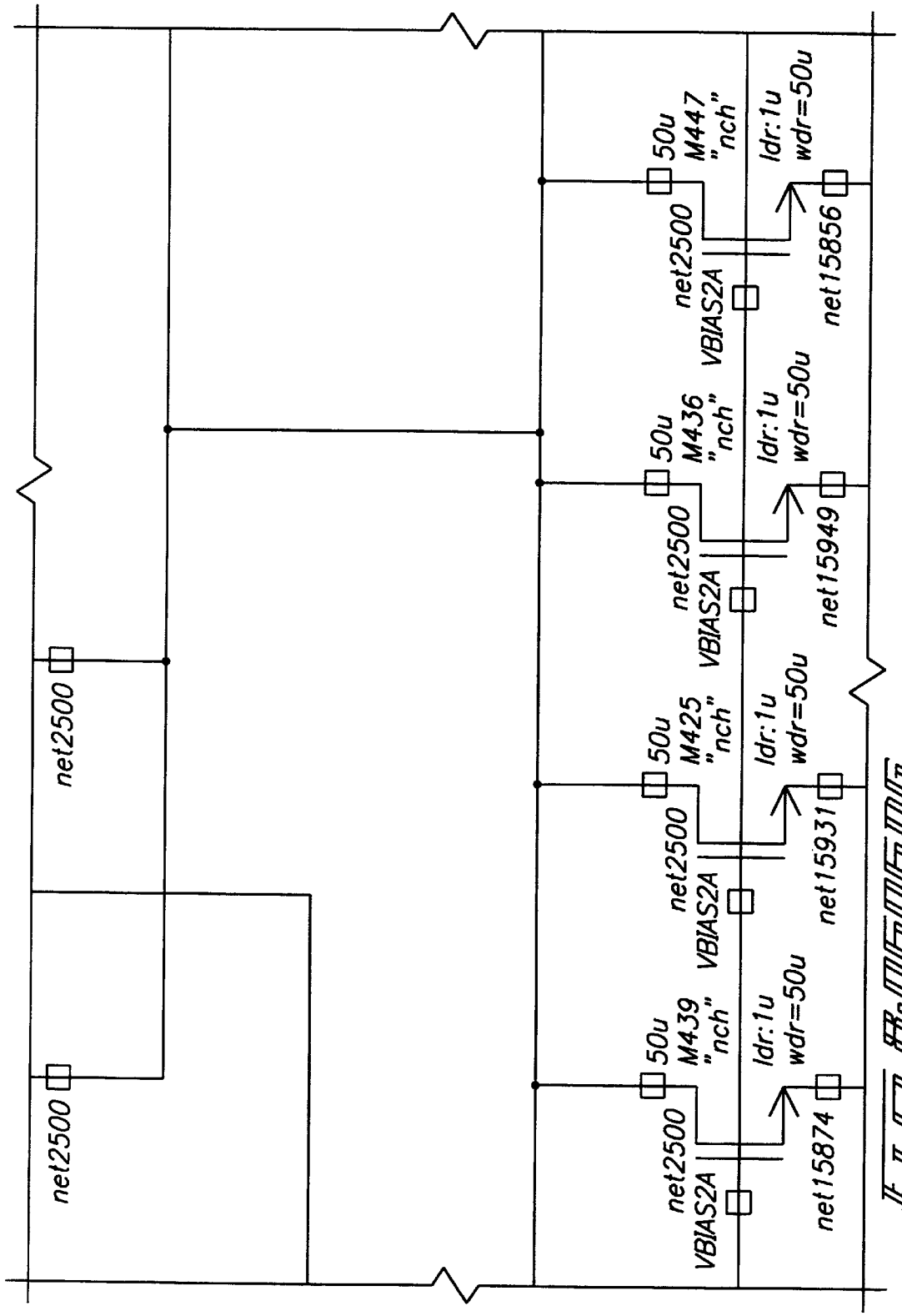

net2500
net2500
net2500
50u M447 "nch"
ldr:1u wdr=50u
net2500 VBIAS2A
net15856
50u M436 "nch"
ldr:1u wdr=50u
net2500 VBIAS2A
net15949
50u M425 "nch"
ldr:1u wdr=50u
net2500 VBIAS2A
net15931
50u M439 "nch"
ldr:1u wdr=50u
net2500 VBIAS2A
net15874

FIG 89

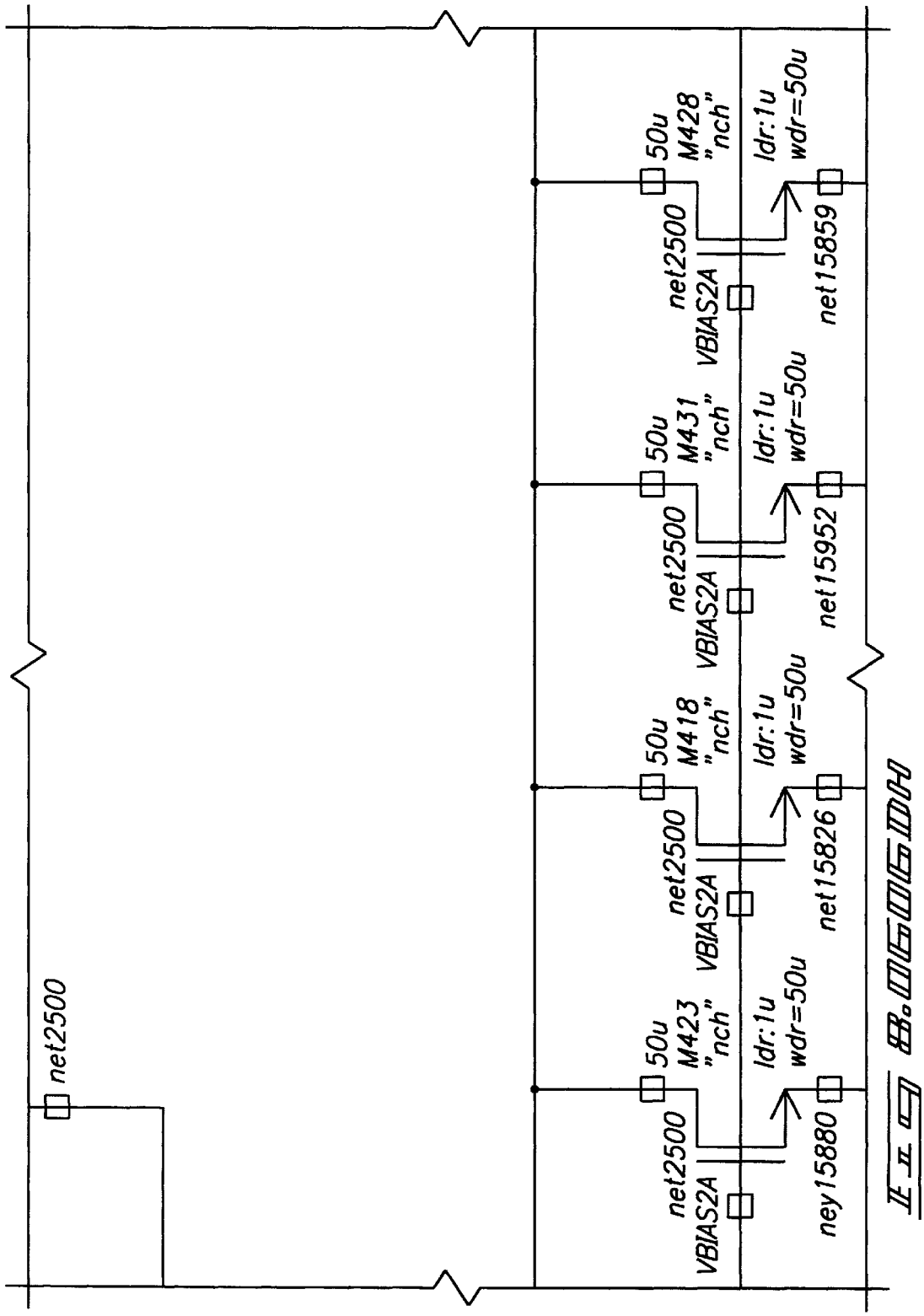


Fig. 88.0(5)(0)(5)(0)(0)

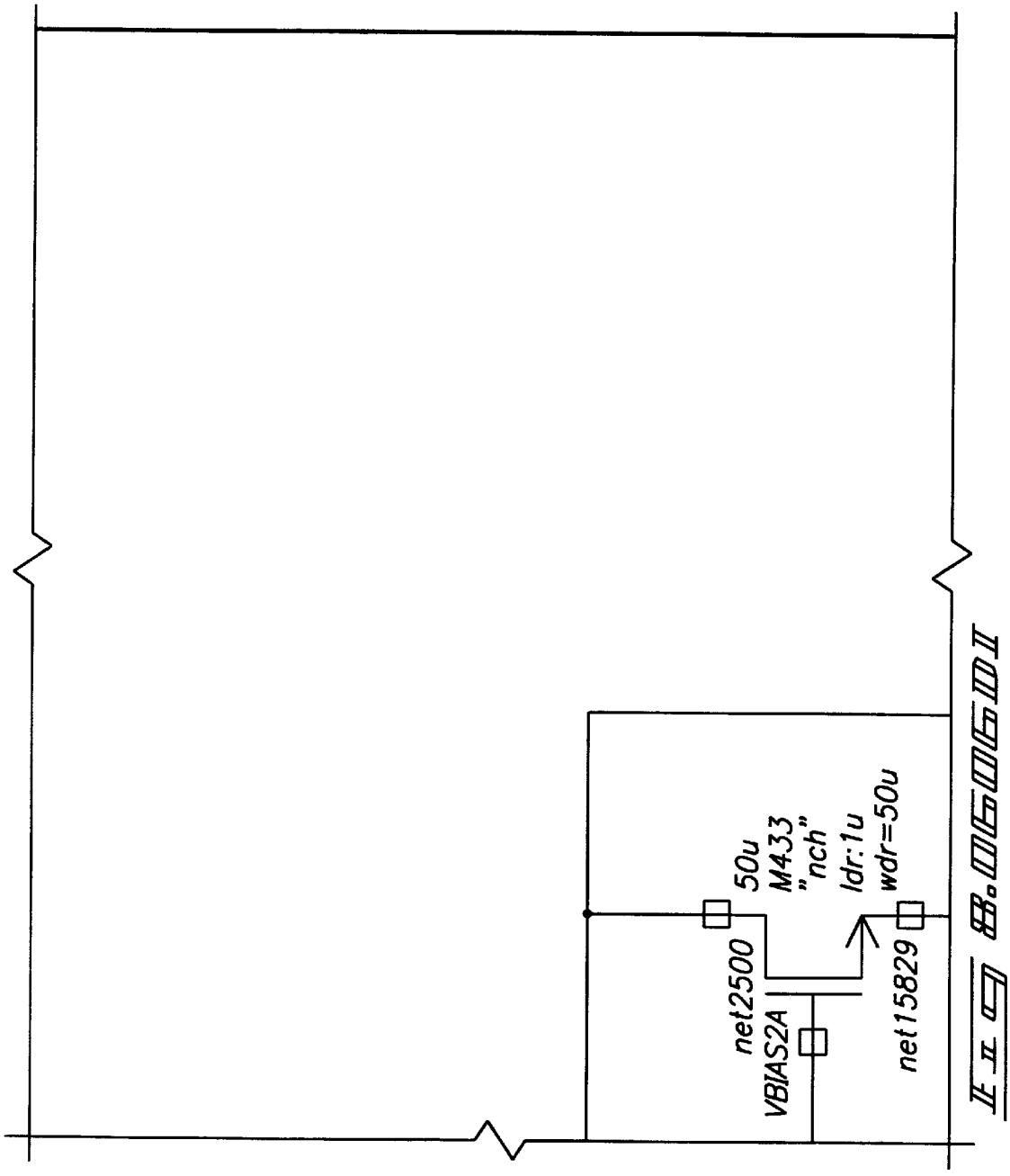


FIG 88.0056011

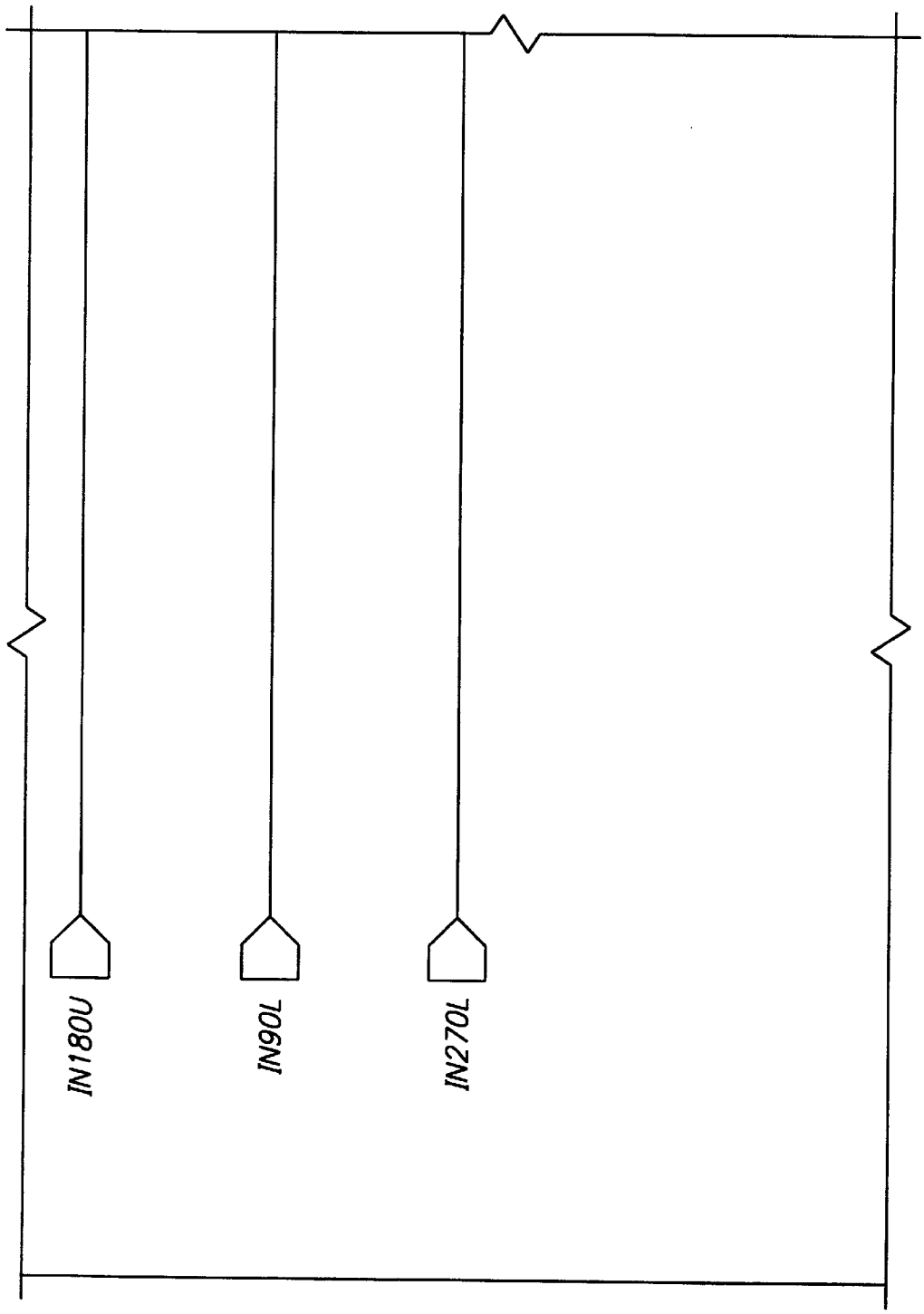


FIG 88.0696EA

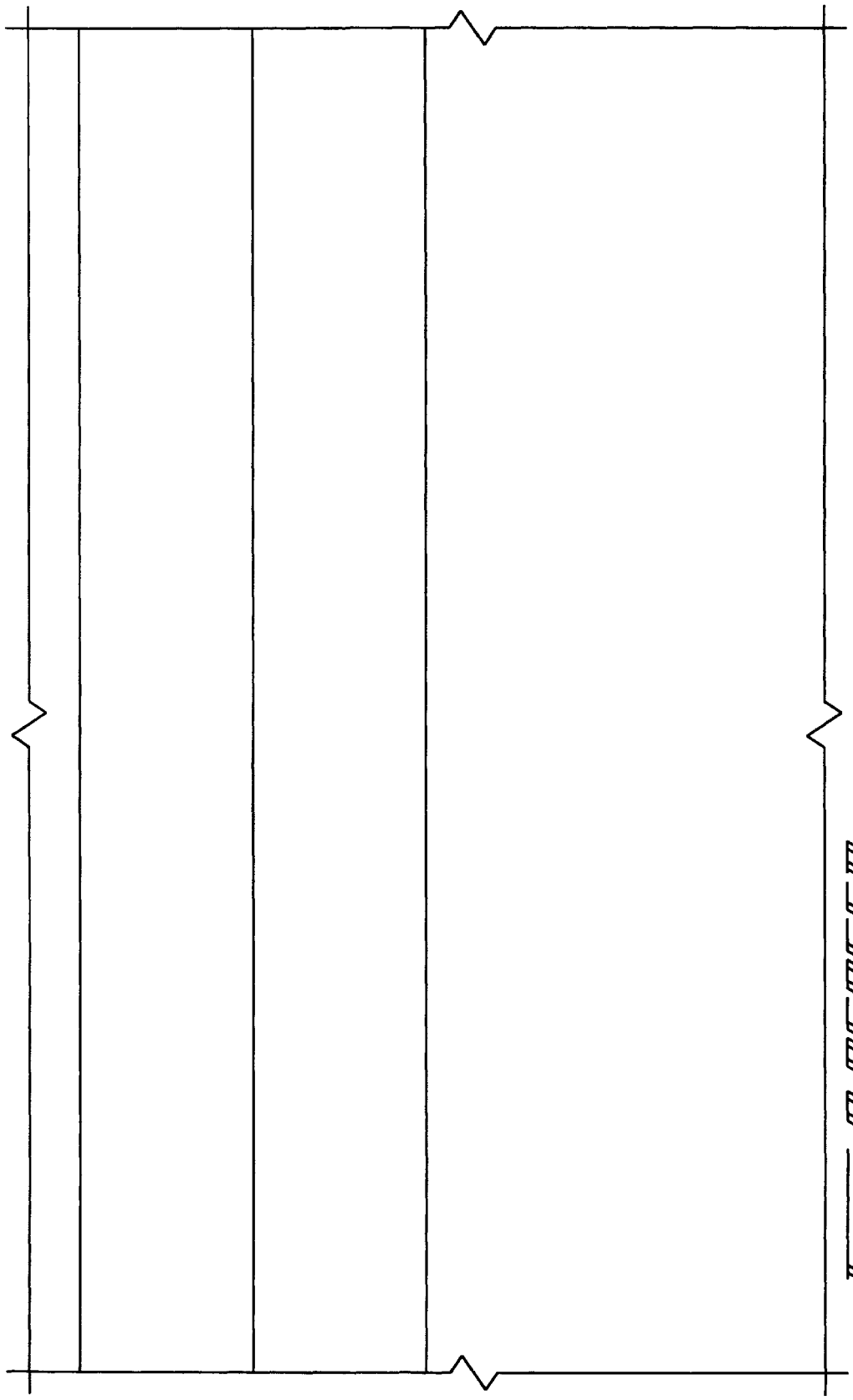
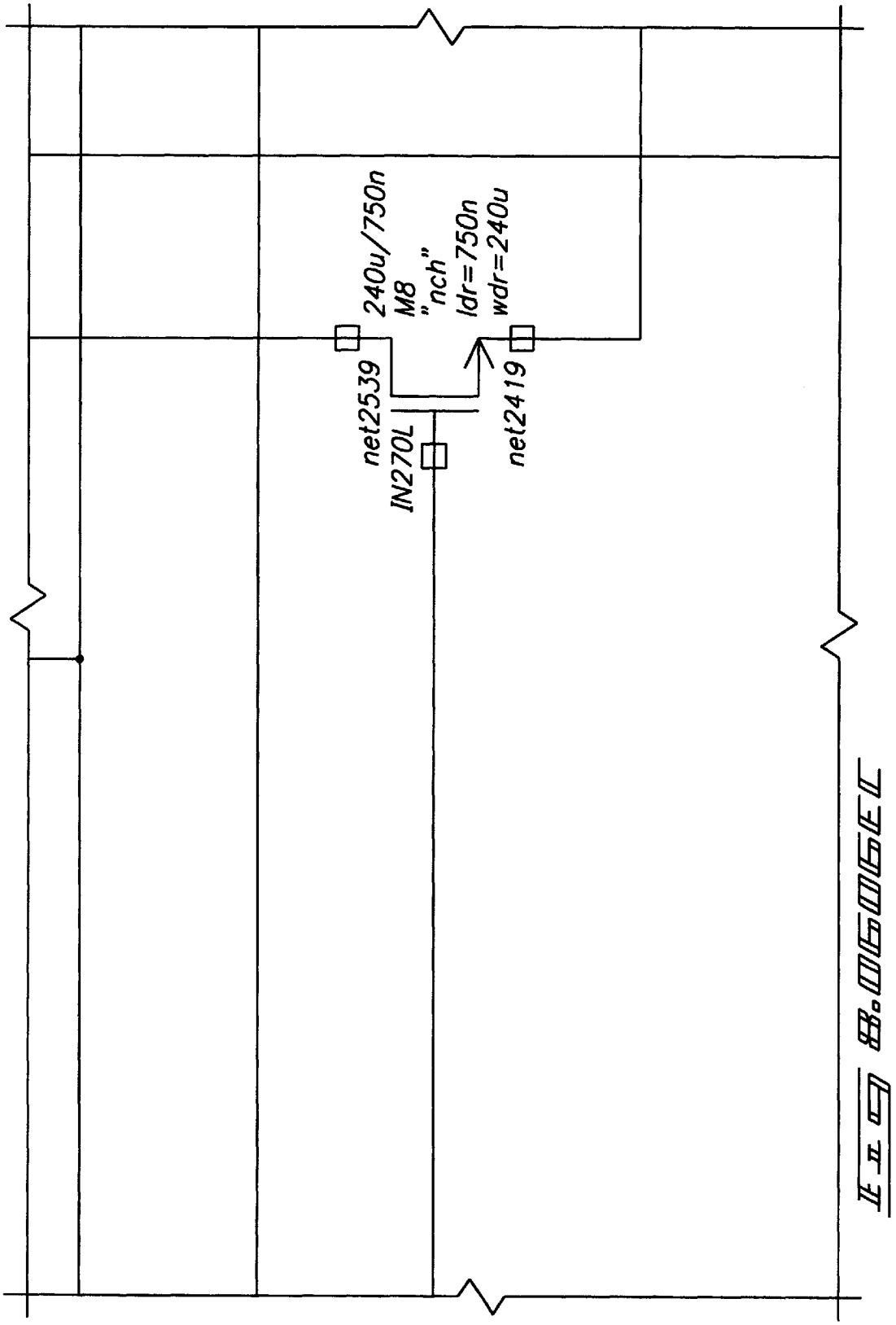
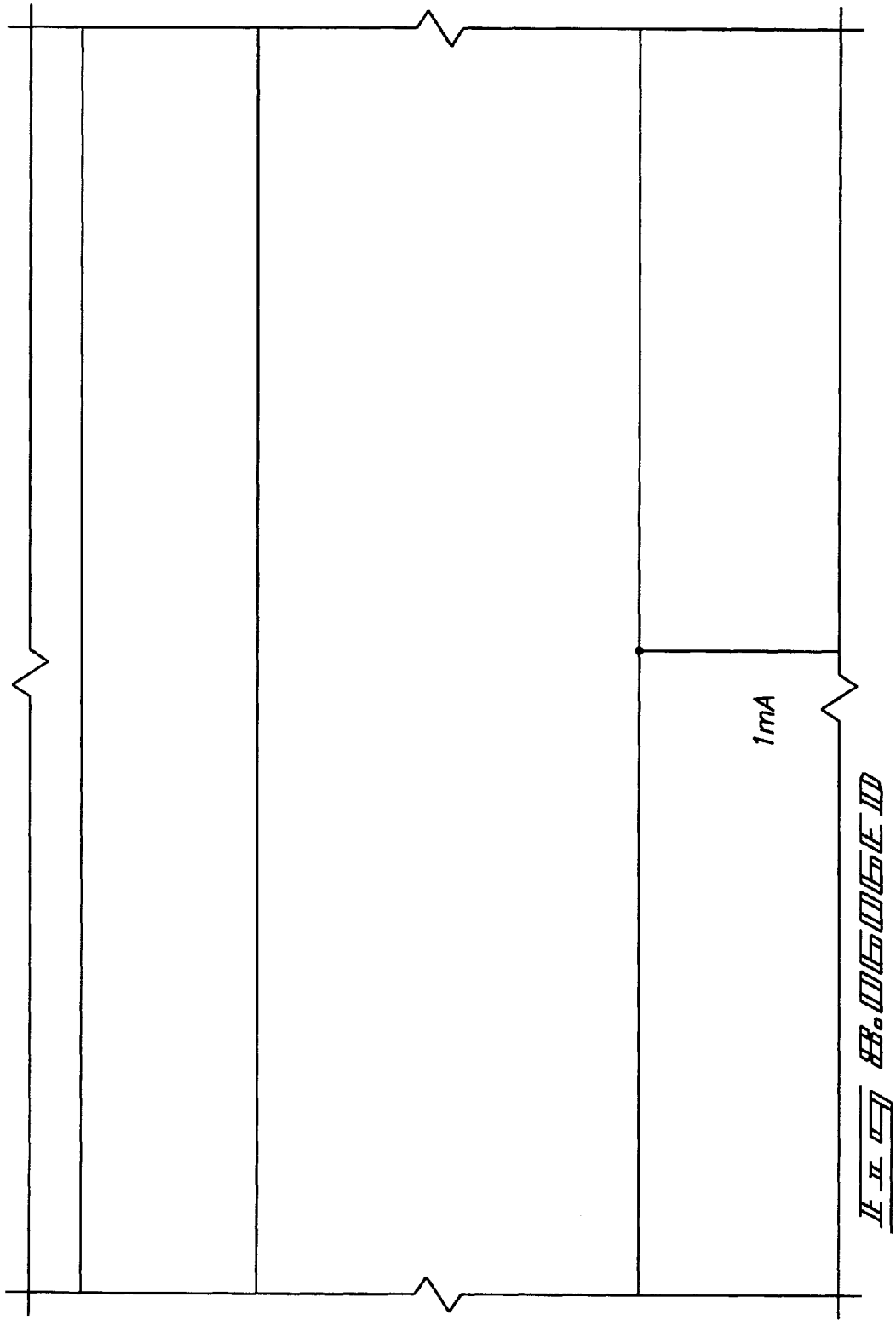


FIG 88.06938


240u/750n
M8
"nch"
ldr=750n
wdr=240u
net2539
IN270L
net2419
FIG. 8,059,837


1mA
FIG 88.0056ED

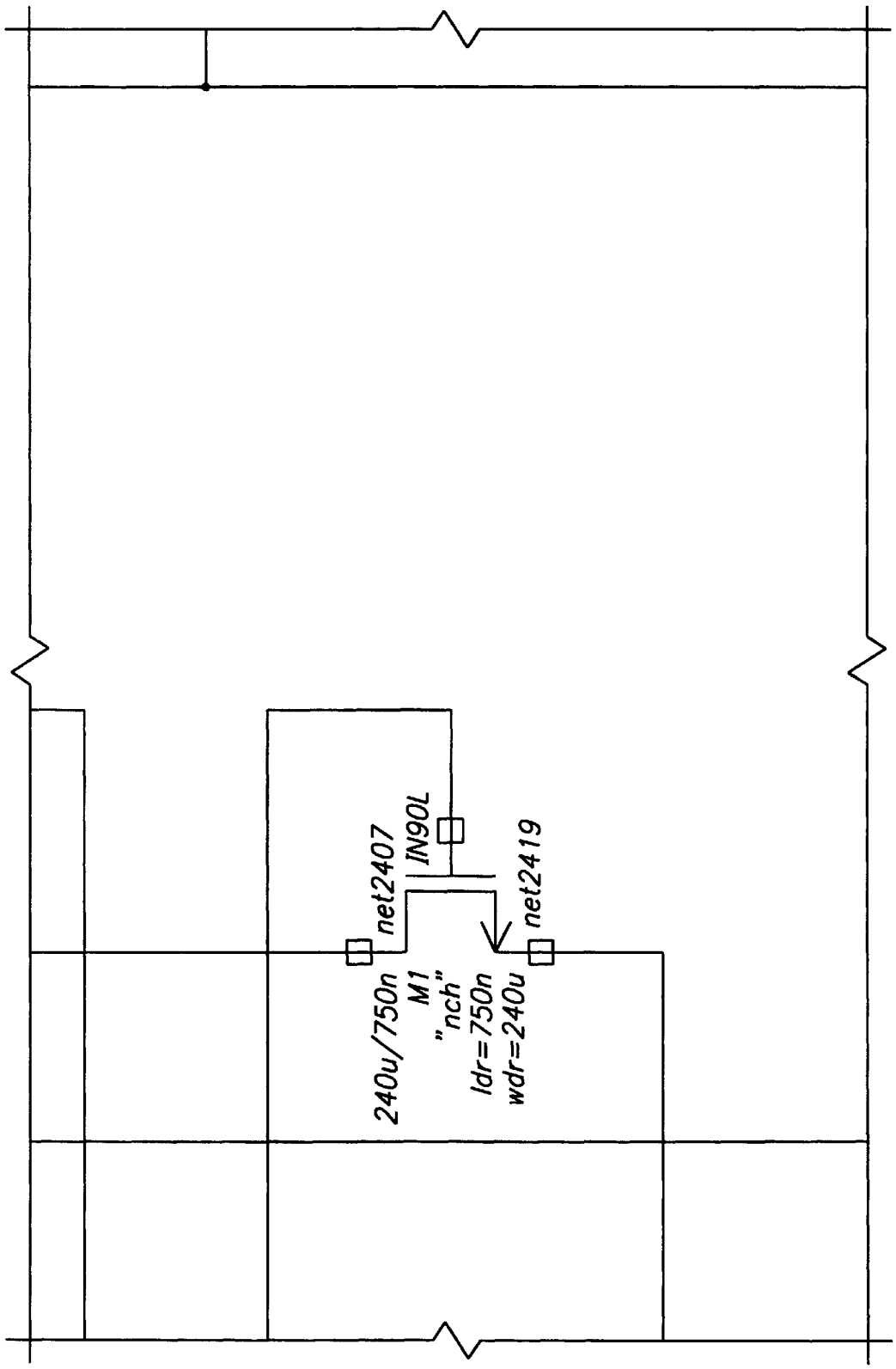


FIG 8.0656E

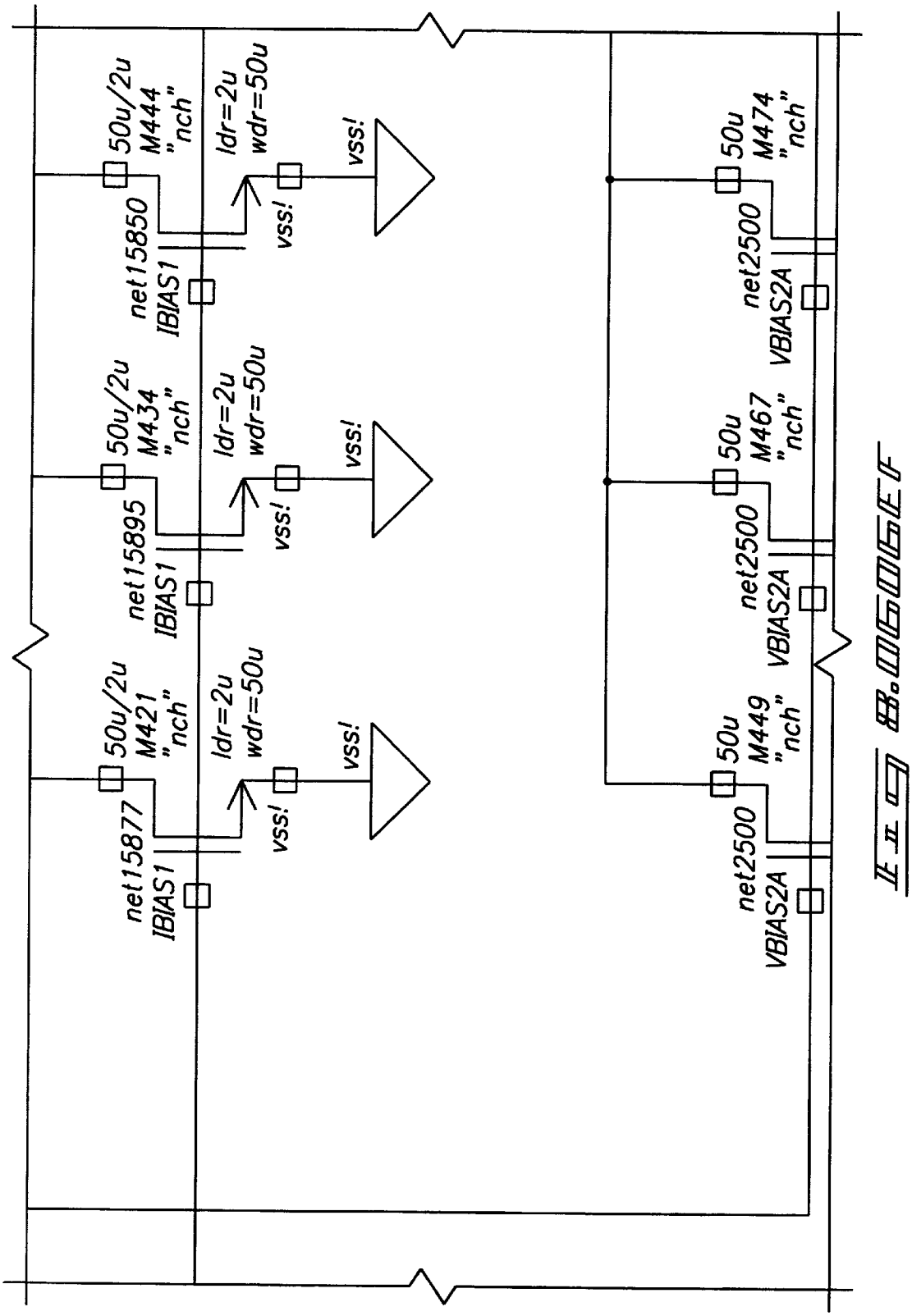


FIG. 88.0050EF

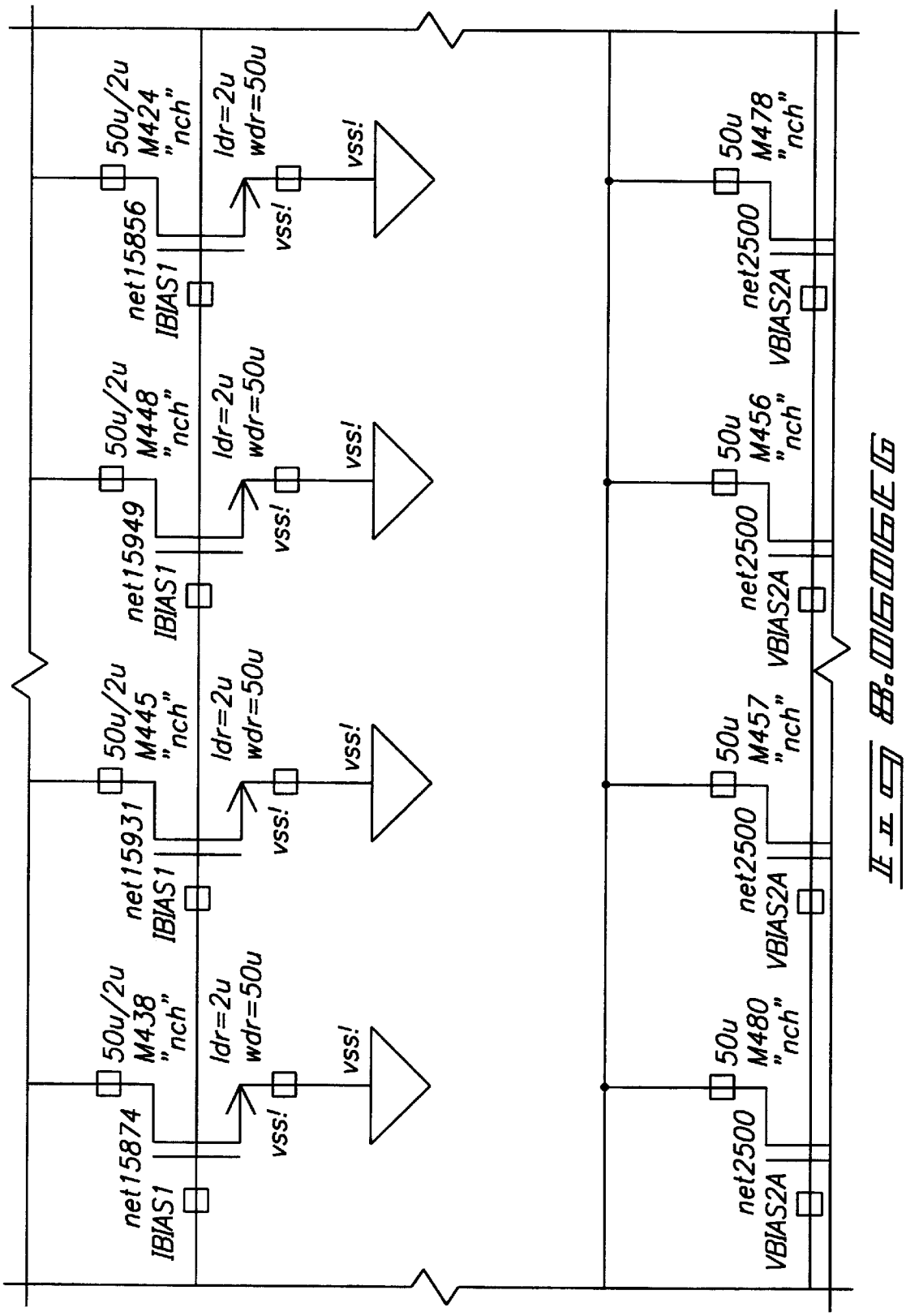
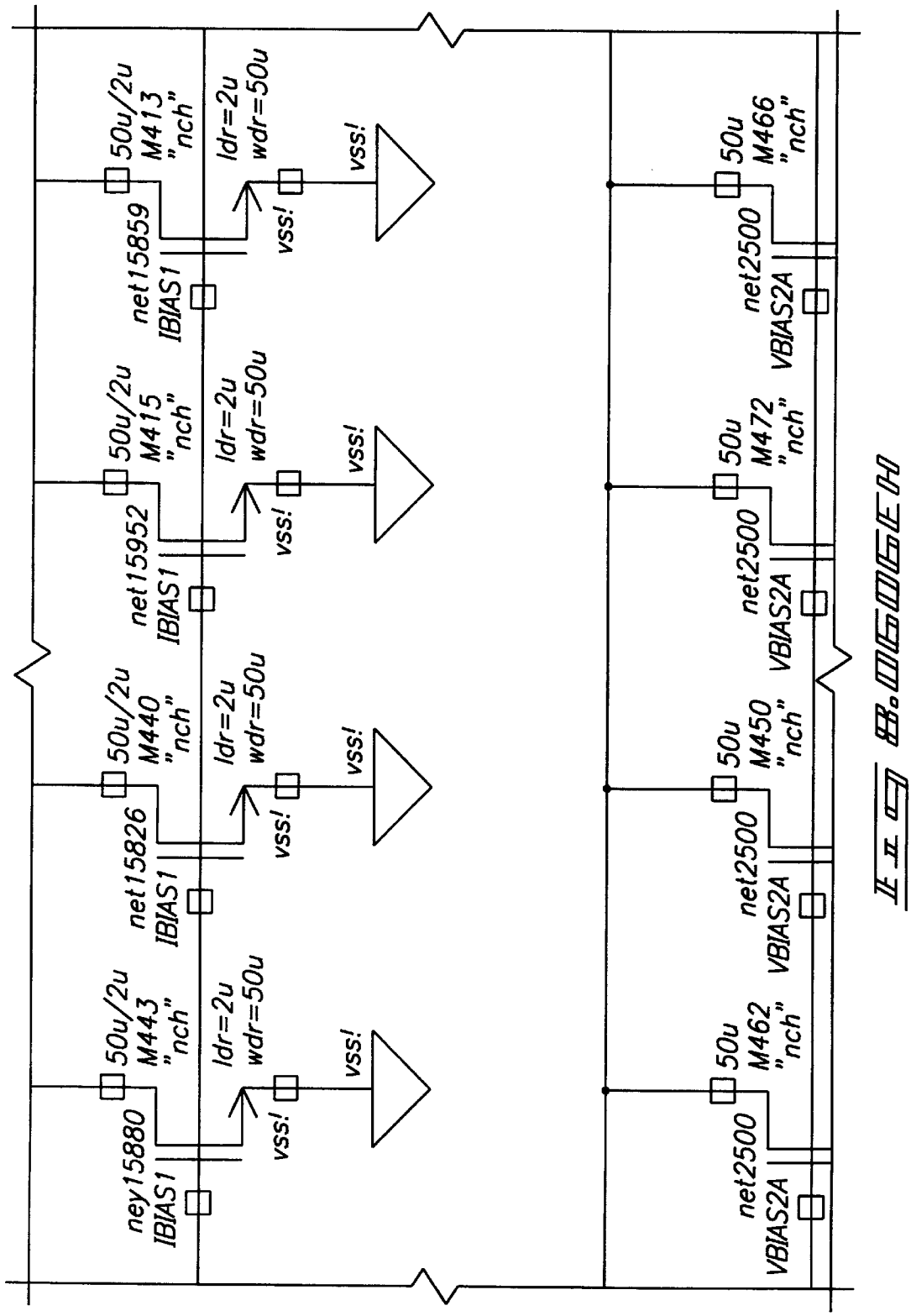


FIG 88.0560E6


50u/2u
M413
"nch"
ldr=2u
wdr=50u
vss!
net15859
IBIAS1
50u
M466
"nch"
net2500
VBIAS2A
50u/2u
M415
"nch"
net15952
50u
M472
"nch"
50u/2u
M440
"nch"
net15826
50u
M450
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M443
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ney15880
50u
M462
"nch"

FIG 88.0056H

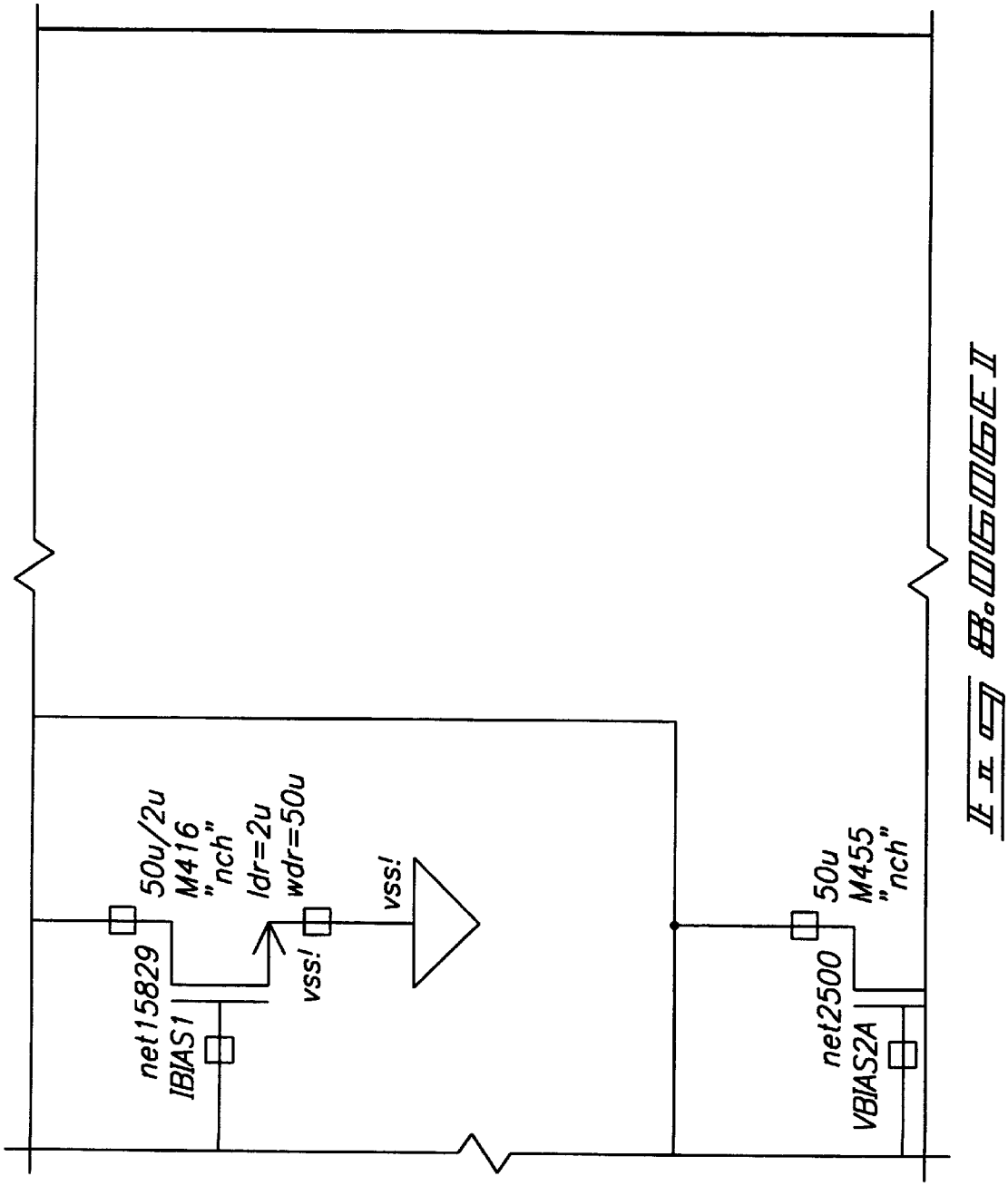
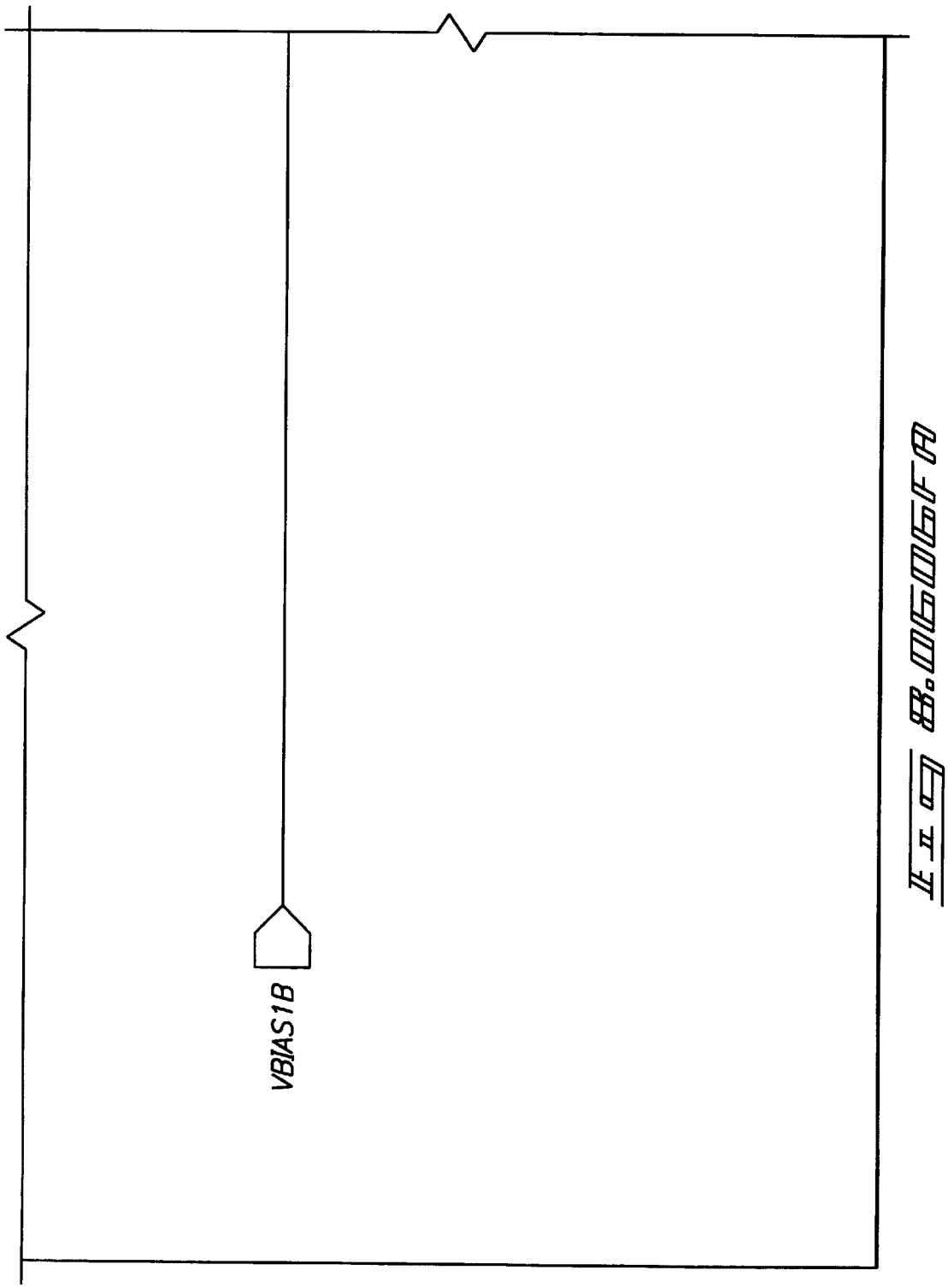


FIG 8.0150E II


VBIAS1B
FIG. 8.0SOSFA

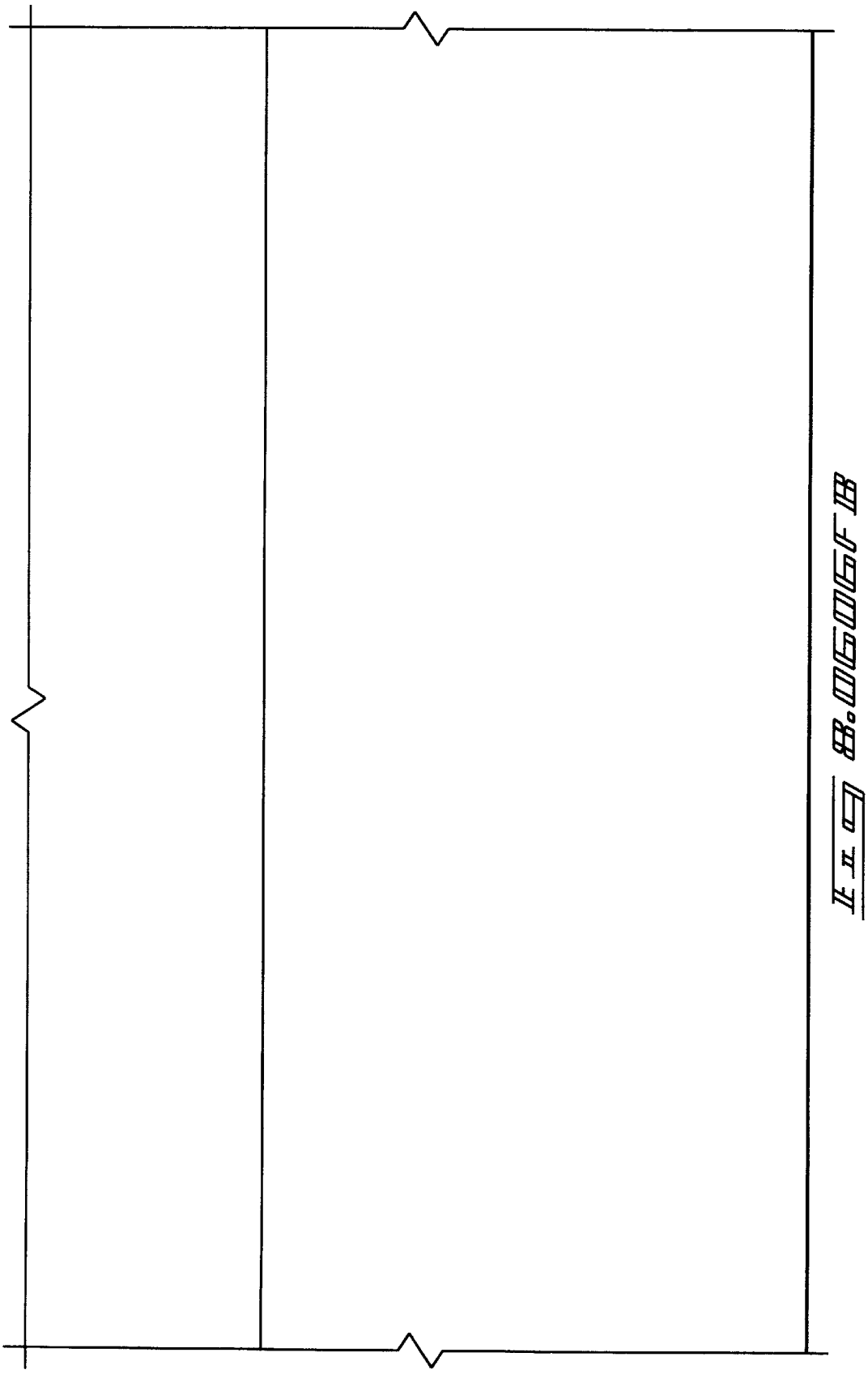


FIG 98.00585F1B

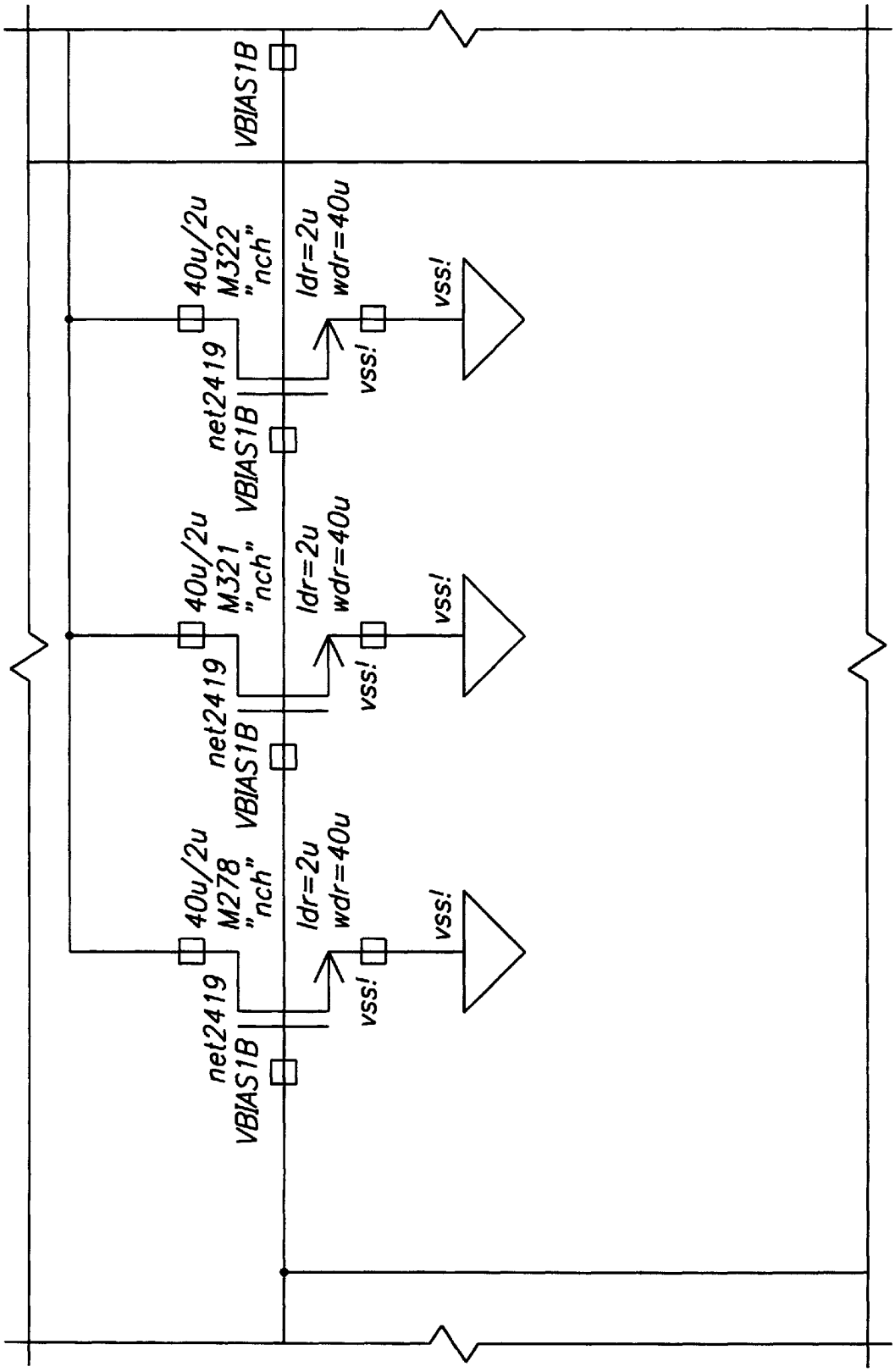
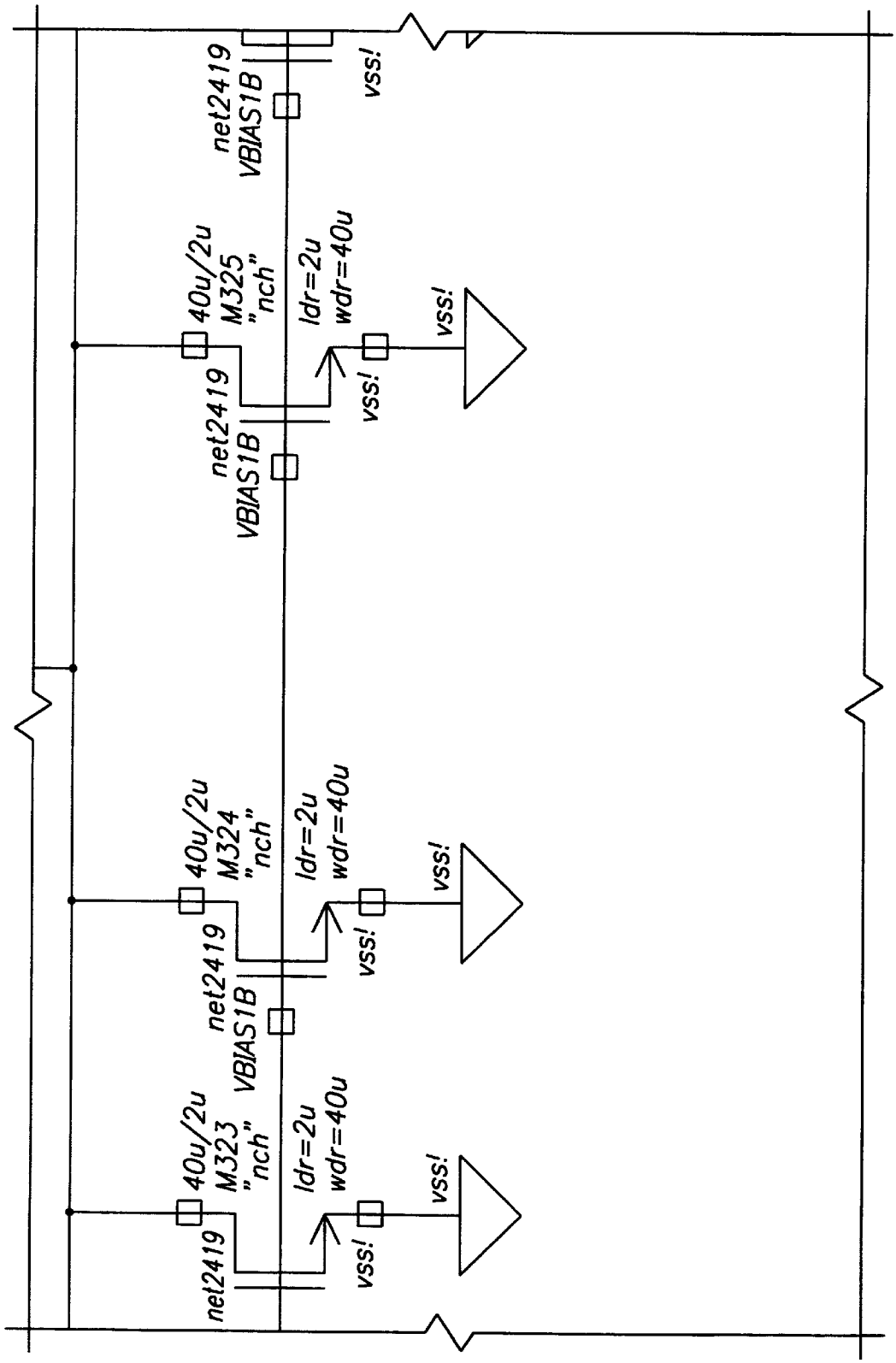

VBIAS1B
40u/2u
M322
"nch"
ldr=2u
wdr=40u
vss!
net2419
VBIAS1B
40u/2u
M321
"nch"
ldr=2u
wdr=40u
vss!
net2419
VBIAS1B
40u/2u
M278
"nch"
ldr=2u
wdr=40u
vss!
net2419
VBIAS1B

FIG 8,056,602


net2419
VBIAS1B
vss!
40u/2u
M325
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ldr=2u
wdr=40u
vss!
vss!
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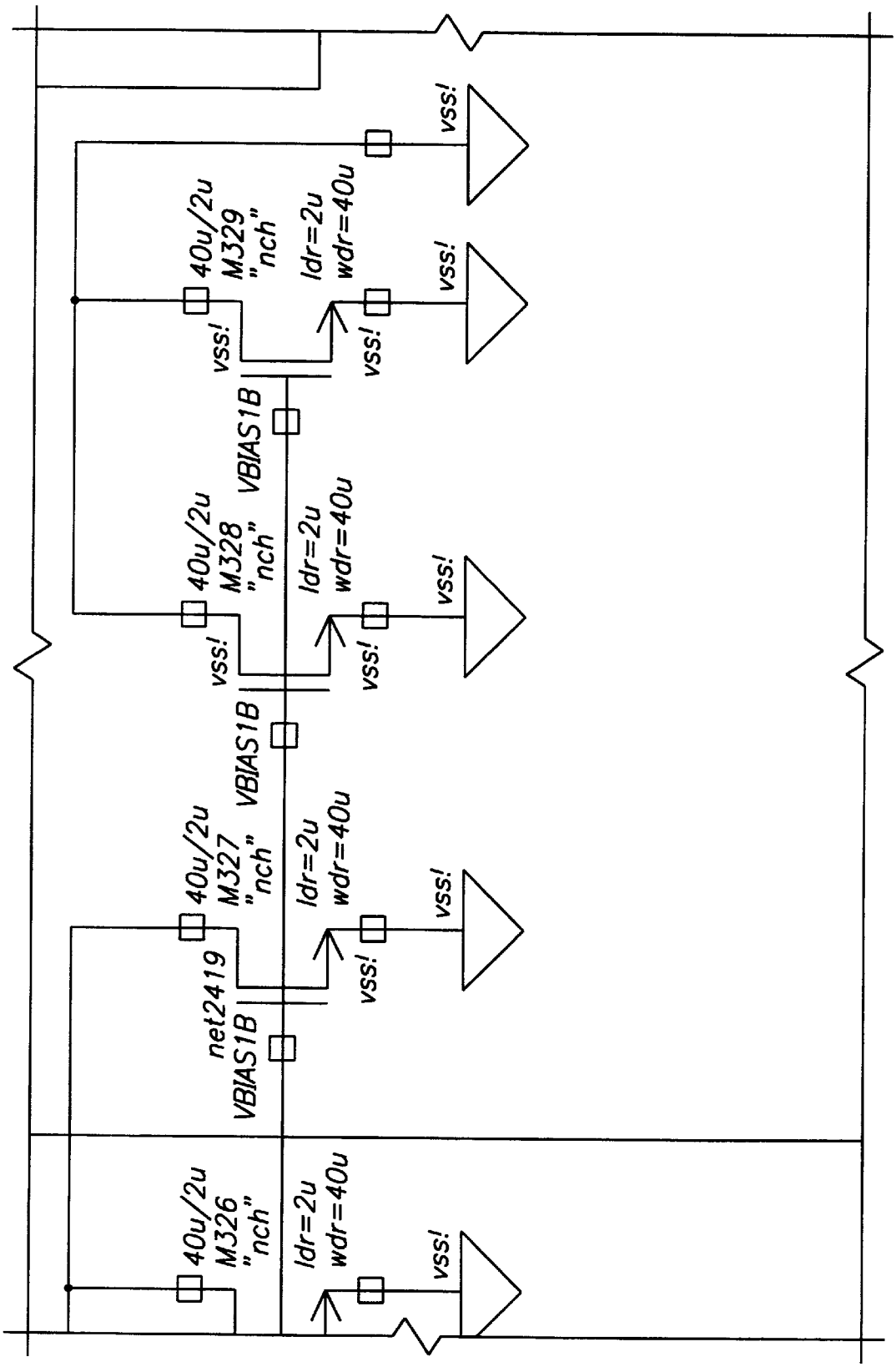
VBIAS1B
40u/2u
M324
"nch"
ldr=2u
wdr=40u
vss!
vss!
net2419
VBIAS1B
40u/2u
M323
"nch"
ldr=2u
wdr=40u
vss!
vss!
net2419

FIG 88.0606F


40u/2u
M326
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ldr=2u
wdr=40u
vss!
net2419
VBIAS1B
40u/2u
M327
"nch"
ldr=2u
wdr=40u
vss!
VBIAS1B
40u/2u
M328
"nch"
ldr=2u
wdr=40u
vss!
VBIAS1B
40u/2u
M329
"nch"
ldr=2u
wdr=40u
vss!

FIG 8.0656F

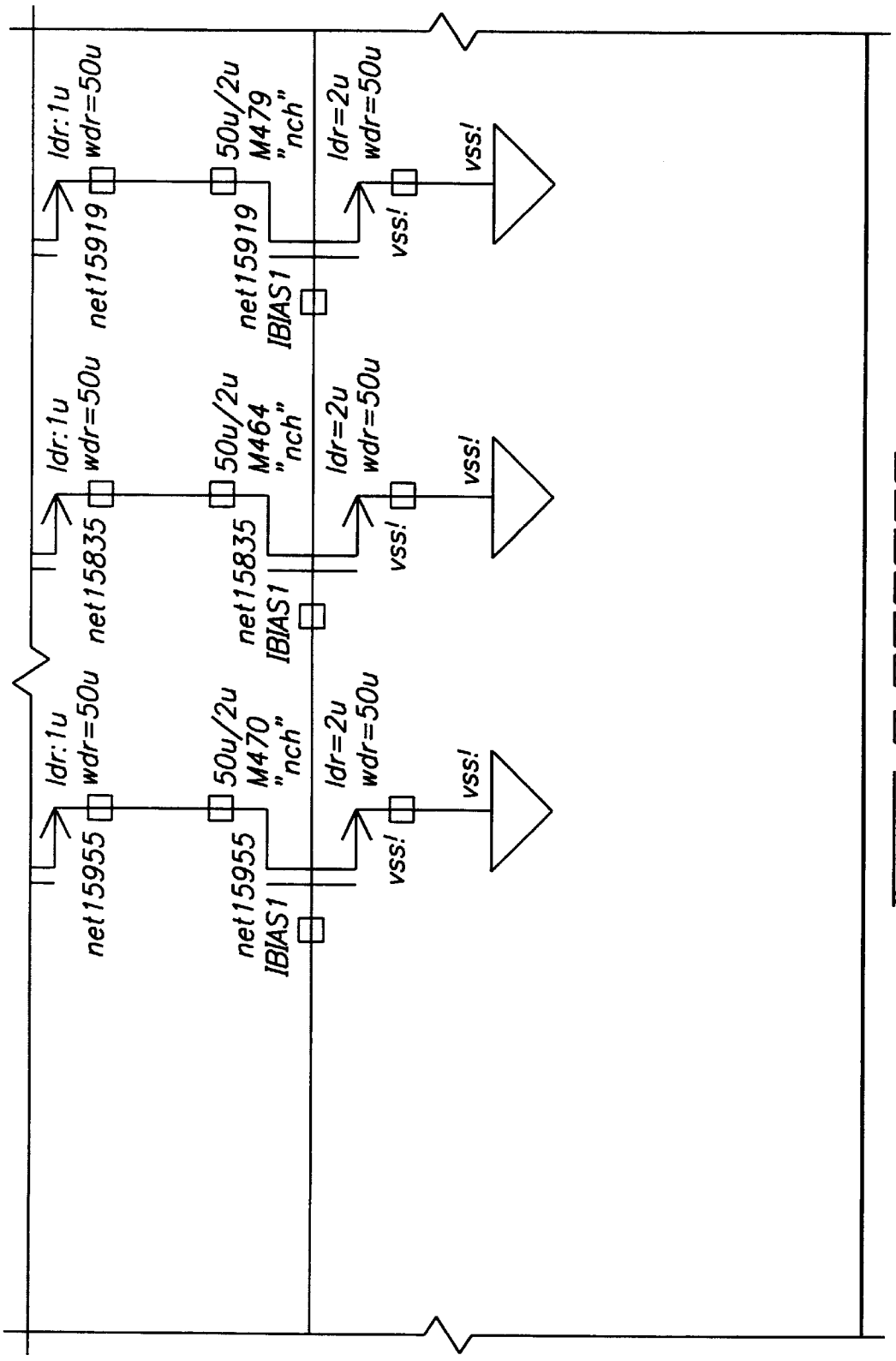

ldr:1u
wdr=50u
net15919
50u/2u
M479
"nch"
IBIAS1
ldr=2u
wdr=50u
vss!
net15835
M464
net15955
M470

FIG 98.0506F

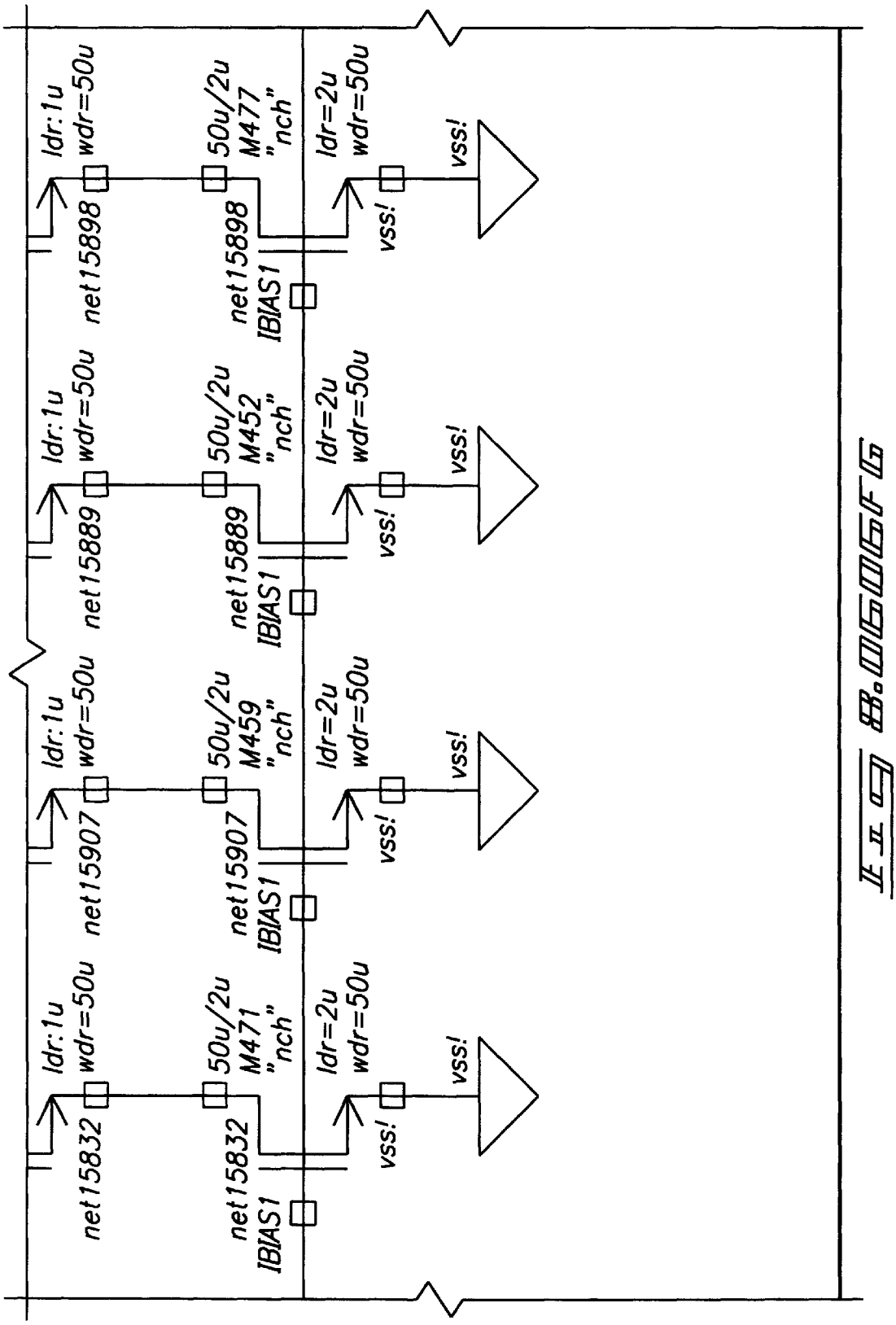
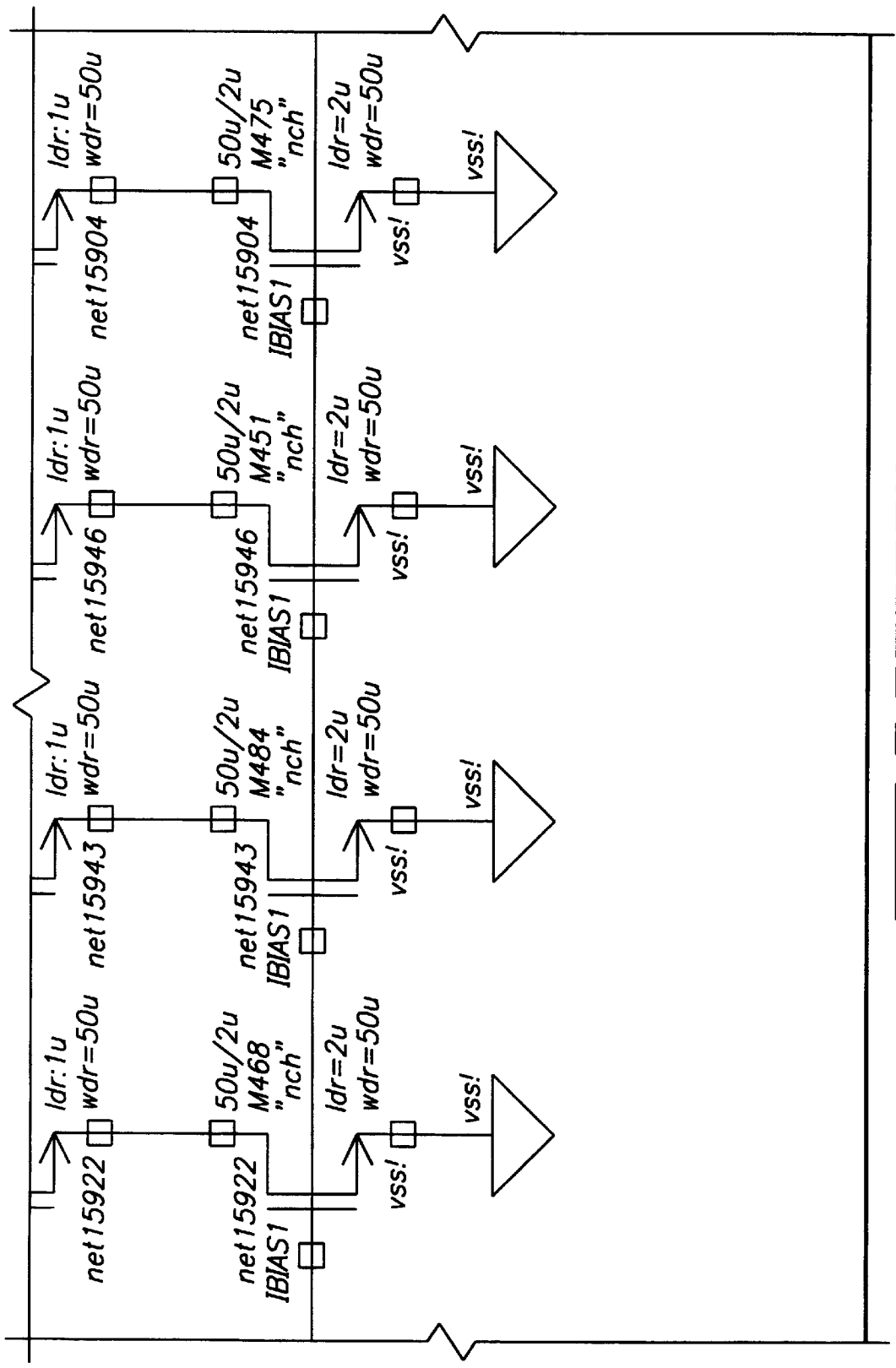


FIG 88.0056FG


ldr:1u
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net15904
50u/2u
M475
"nch"
net15904
IBIAS1
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wdr=50u
vss!
ldr:1u
wdr=50u
net15946
50u/2u
M451
"nch"
net15946
IBIAS1
ldr=2u
wdr=50u
vss!
ldr:1u
wdr=50u
net15943
50u/2u
M484
"nch"
net15943
IBIAS1
ldr=2u
wdr=50u
vss!
ldr:1u
wdr=50u
net15922
50u/2u
M468
"nch"
net15922
IBIAS1
ldr=2u
wdr=50u
vss!

FIG 8.0606FH

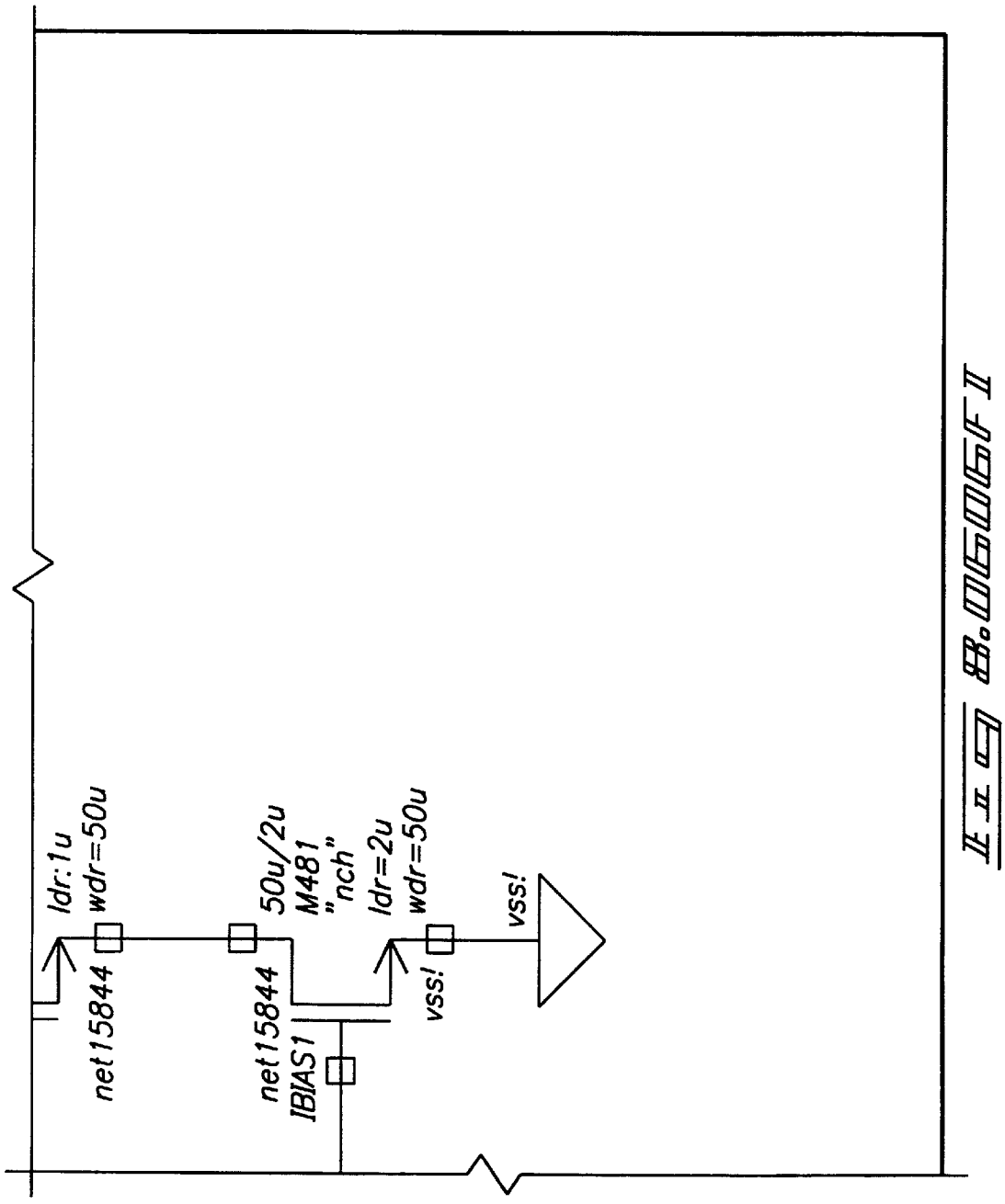

ldr:1u
wdr=50u
net15844
50u/2u
M481
"nch"
ldr=2u
wdr=50u
vss!
net15844
IBIAS1
vss!

FIG. 88,065

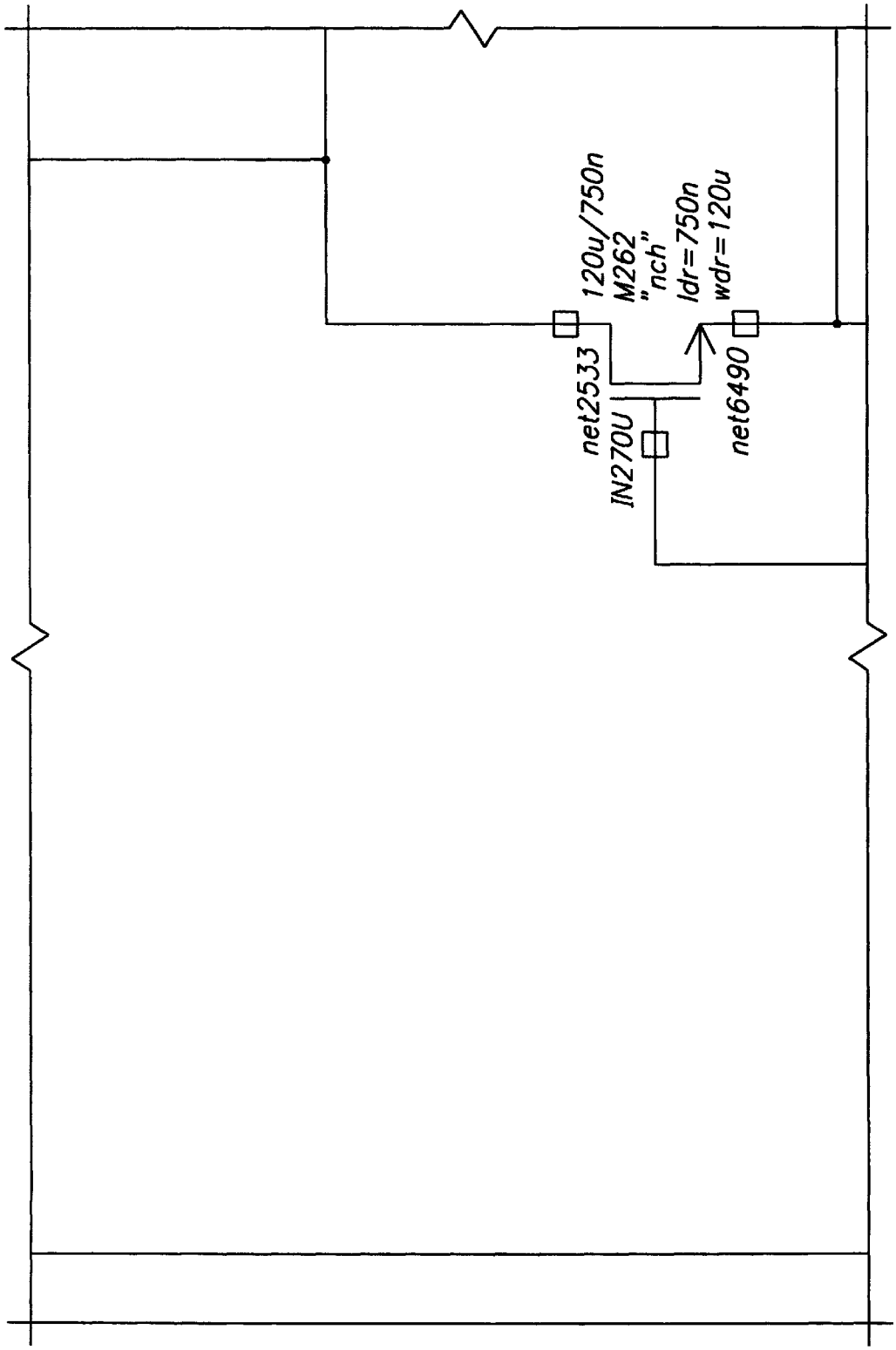


FIG 8.0595C

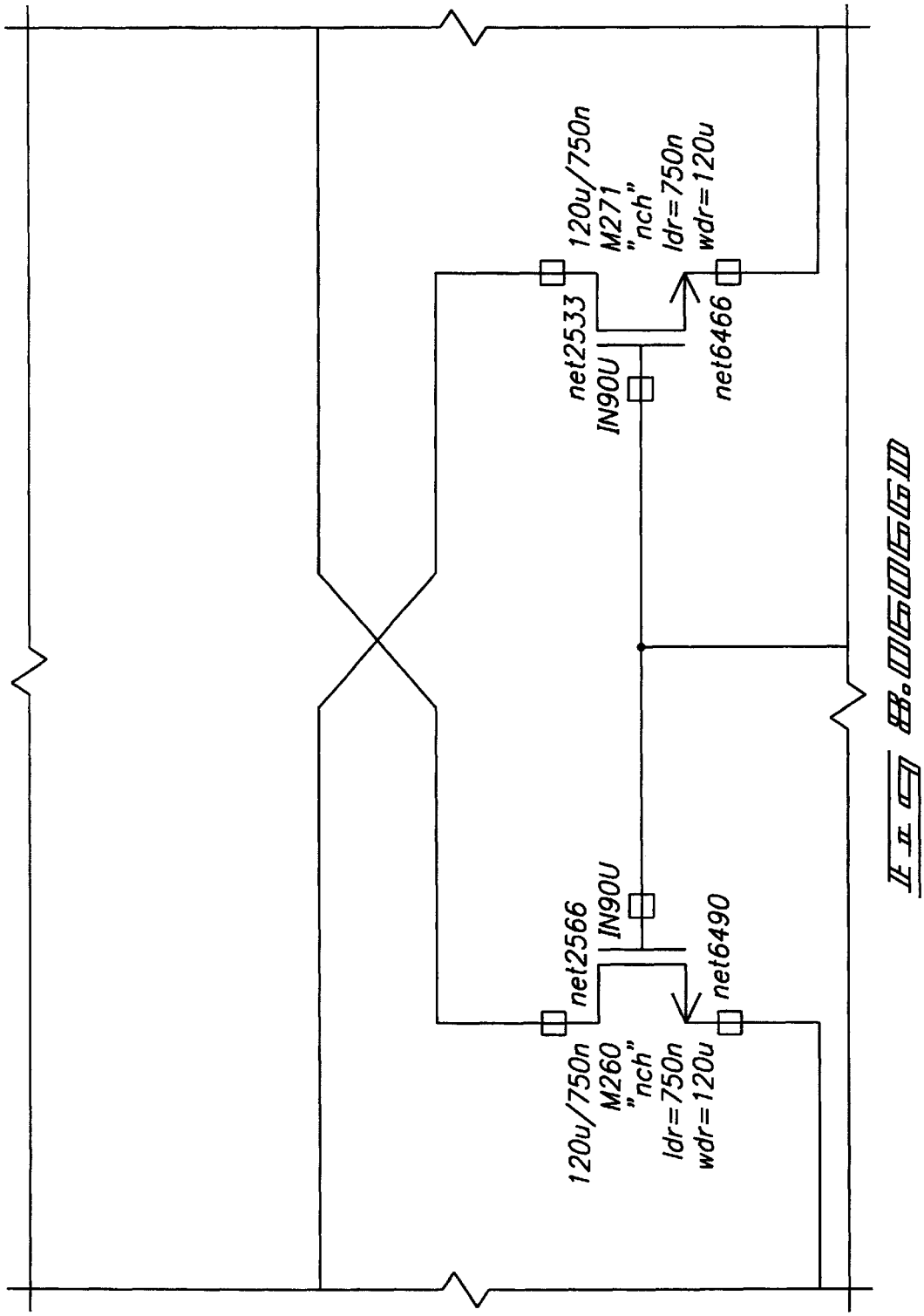


FIG 89,085,610

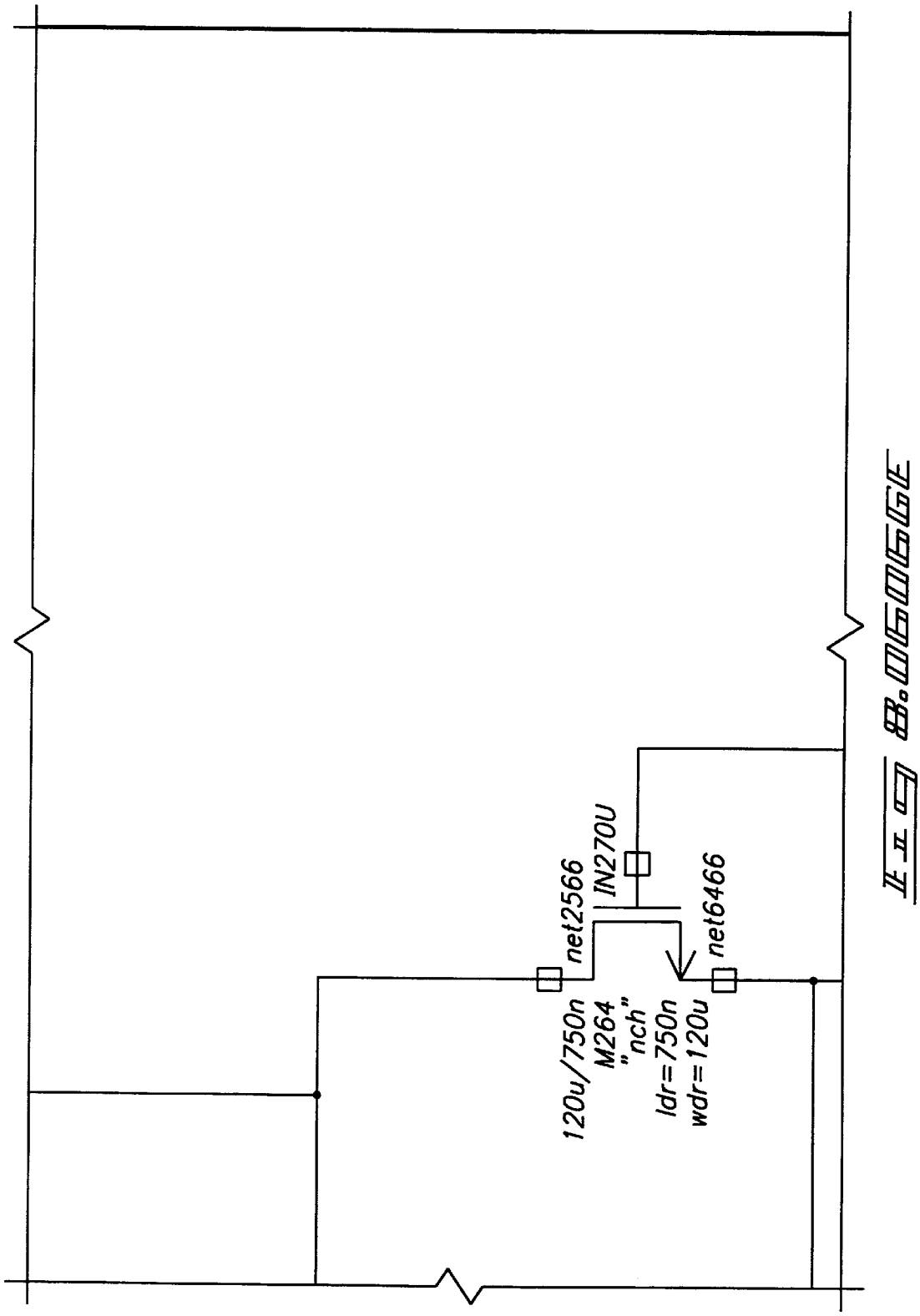


FIG 8.0656E
IN270U
net2566
net6466
120u/750n
M264
"nch"
ldr=750n
wdr=120u

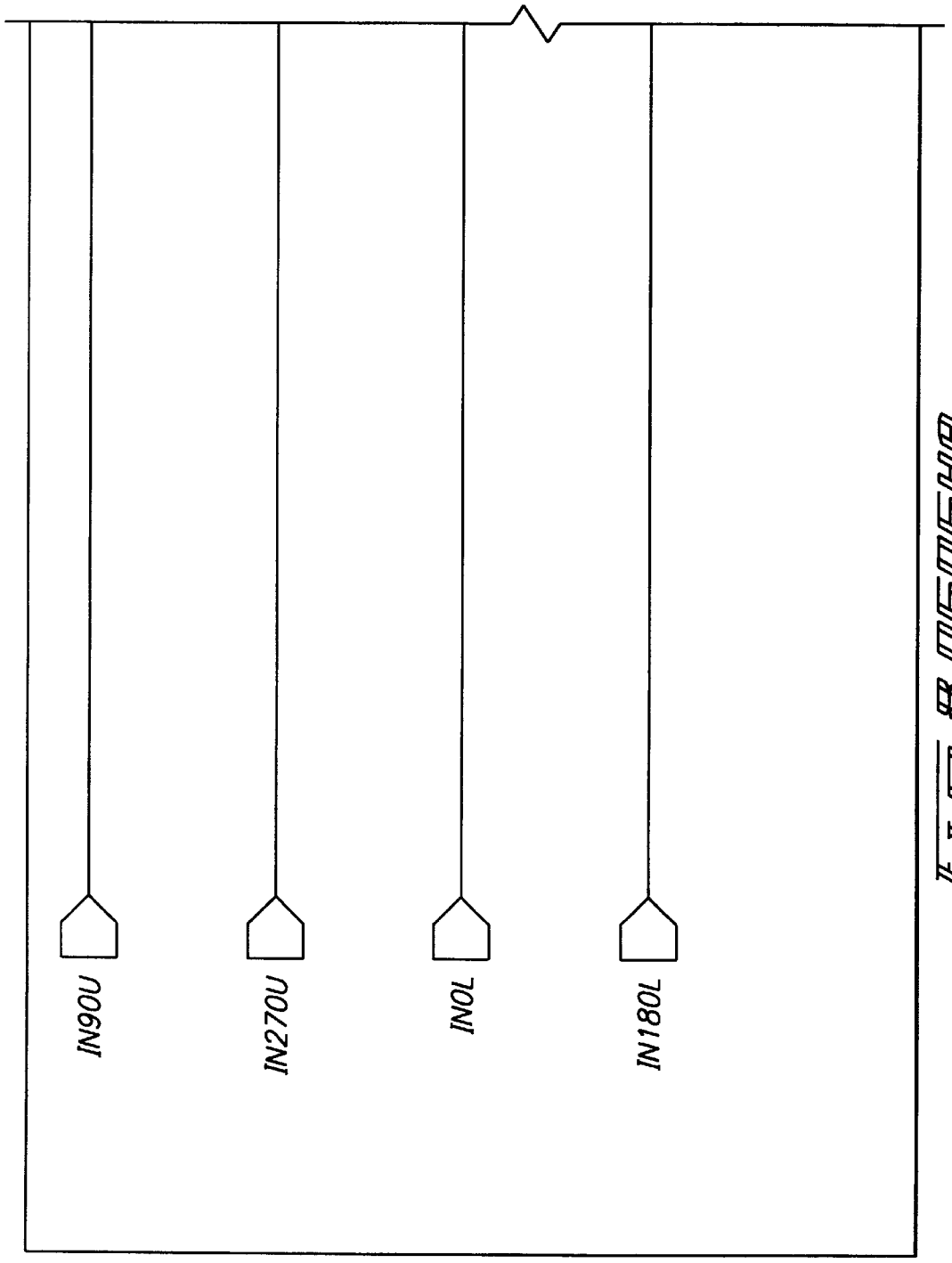


FIG 98,059

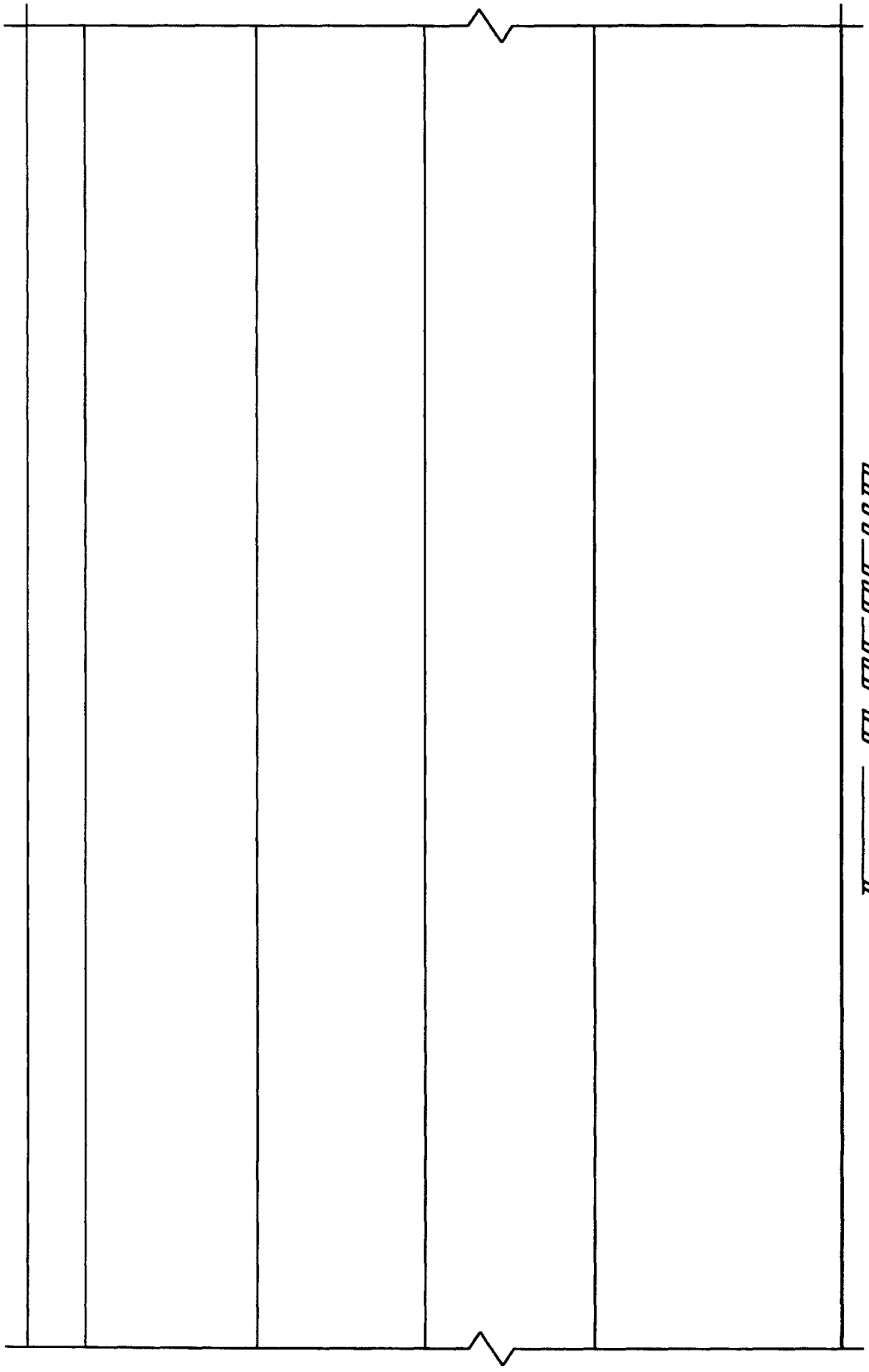


FIG 8,050,418

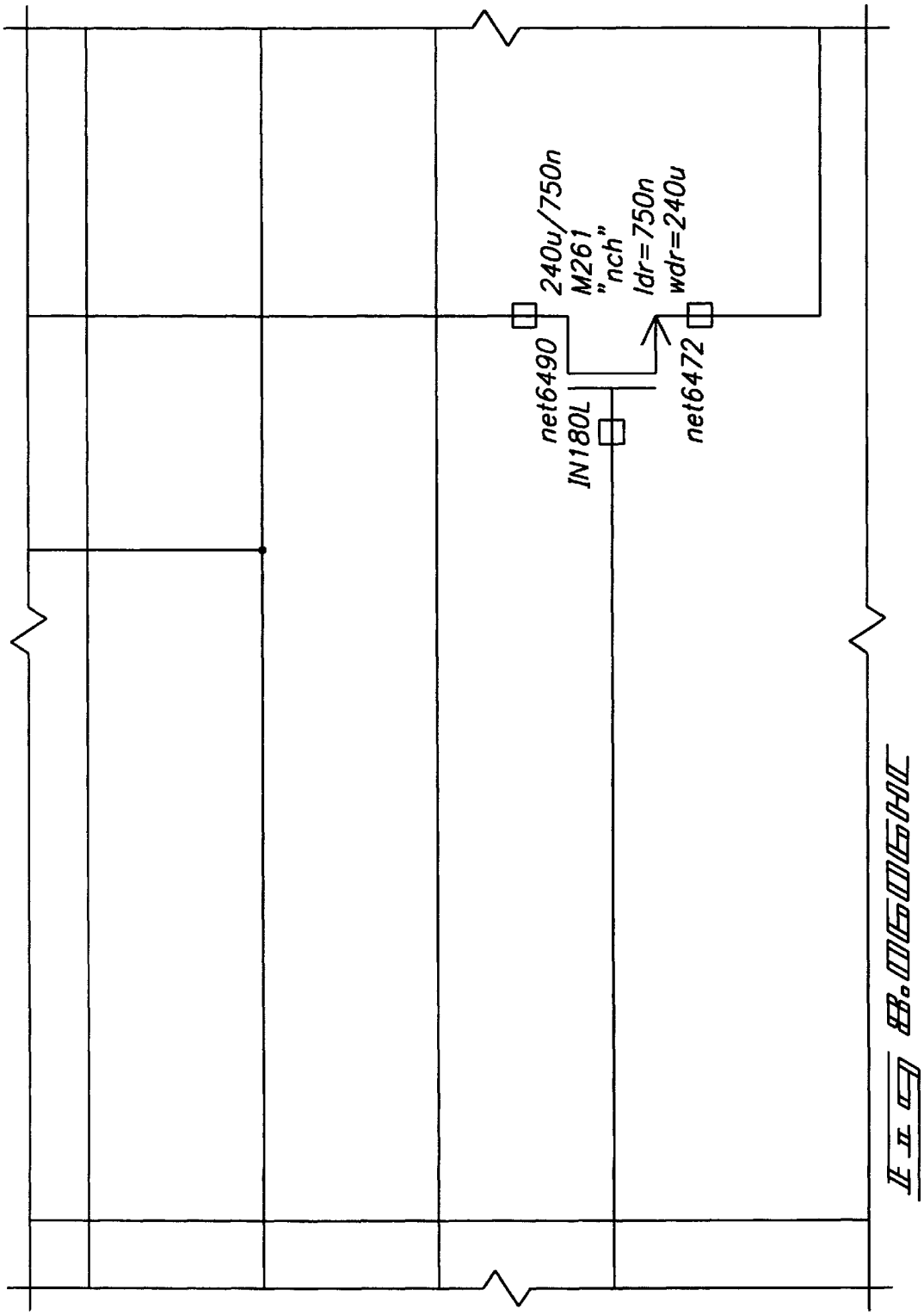


FIG 88.0696HC

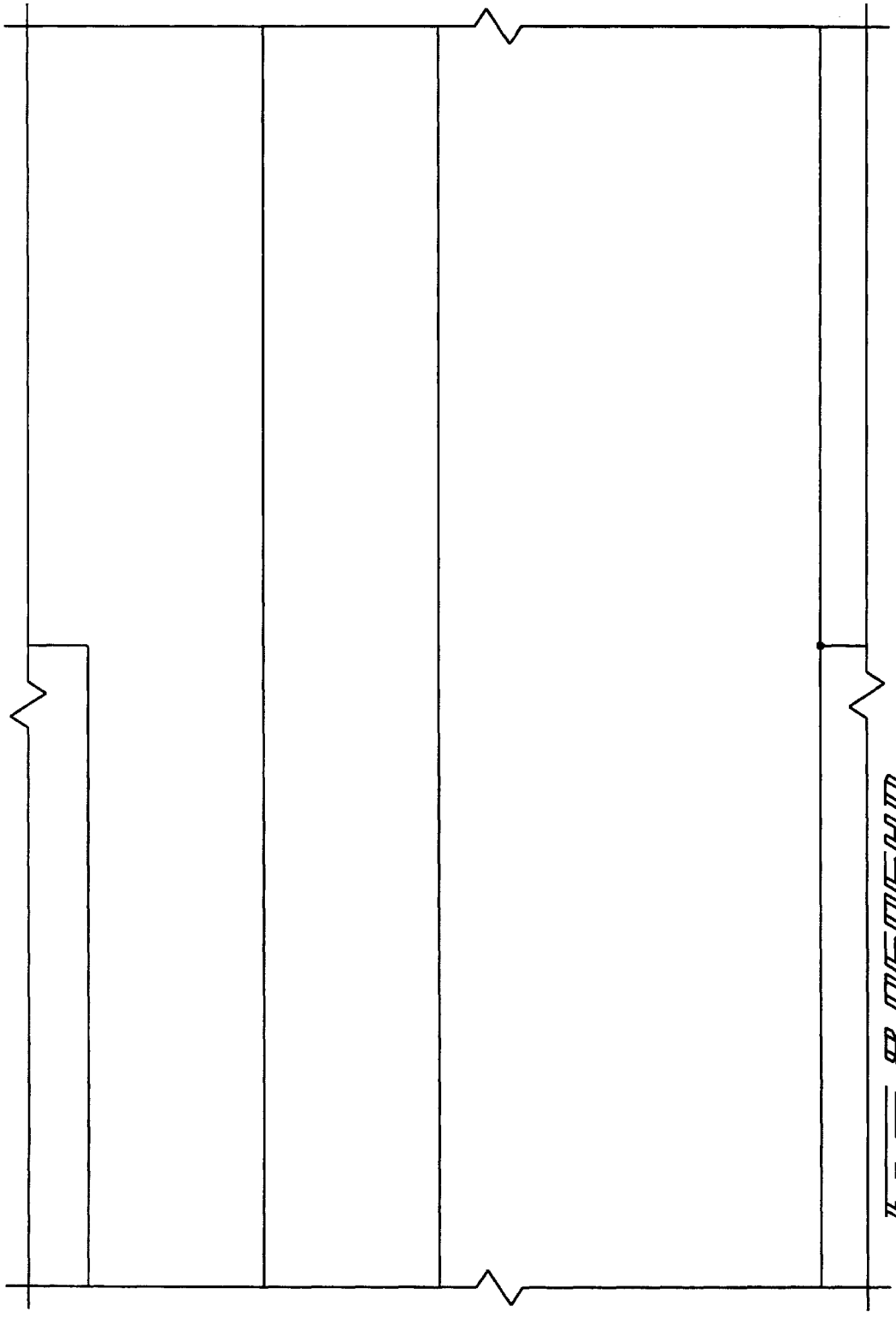
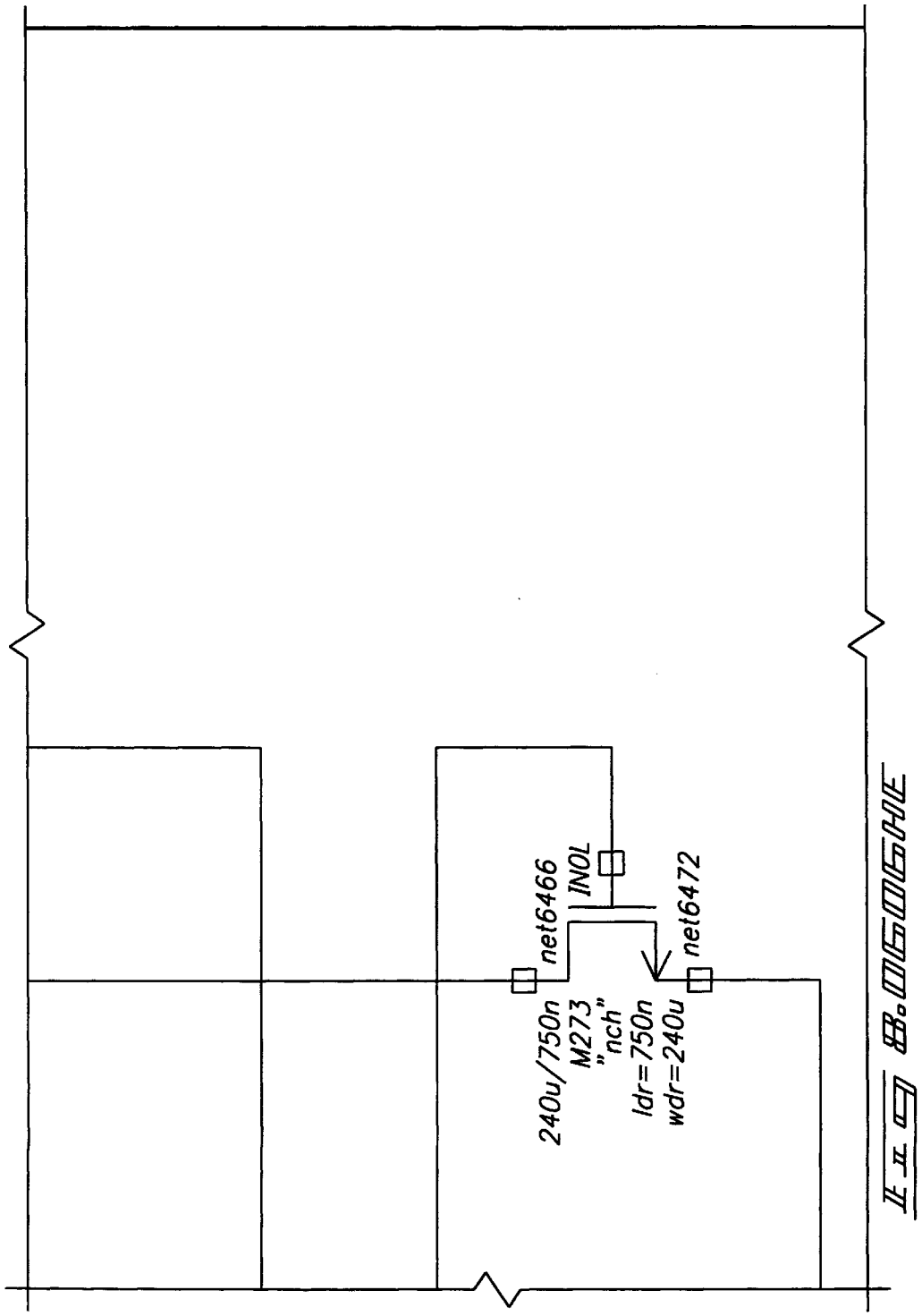


FIG 98.0650HD


net6466
IN0L
net6472
240u/750n
M273
"nch"
ldr=750n
wdr=240u

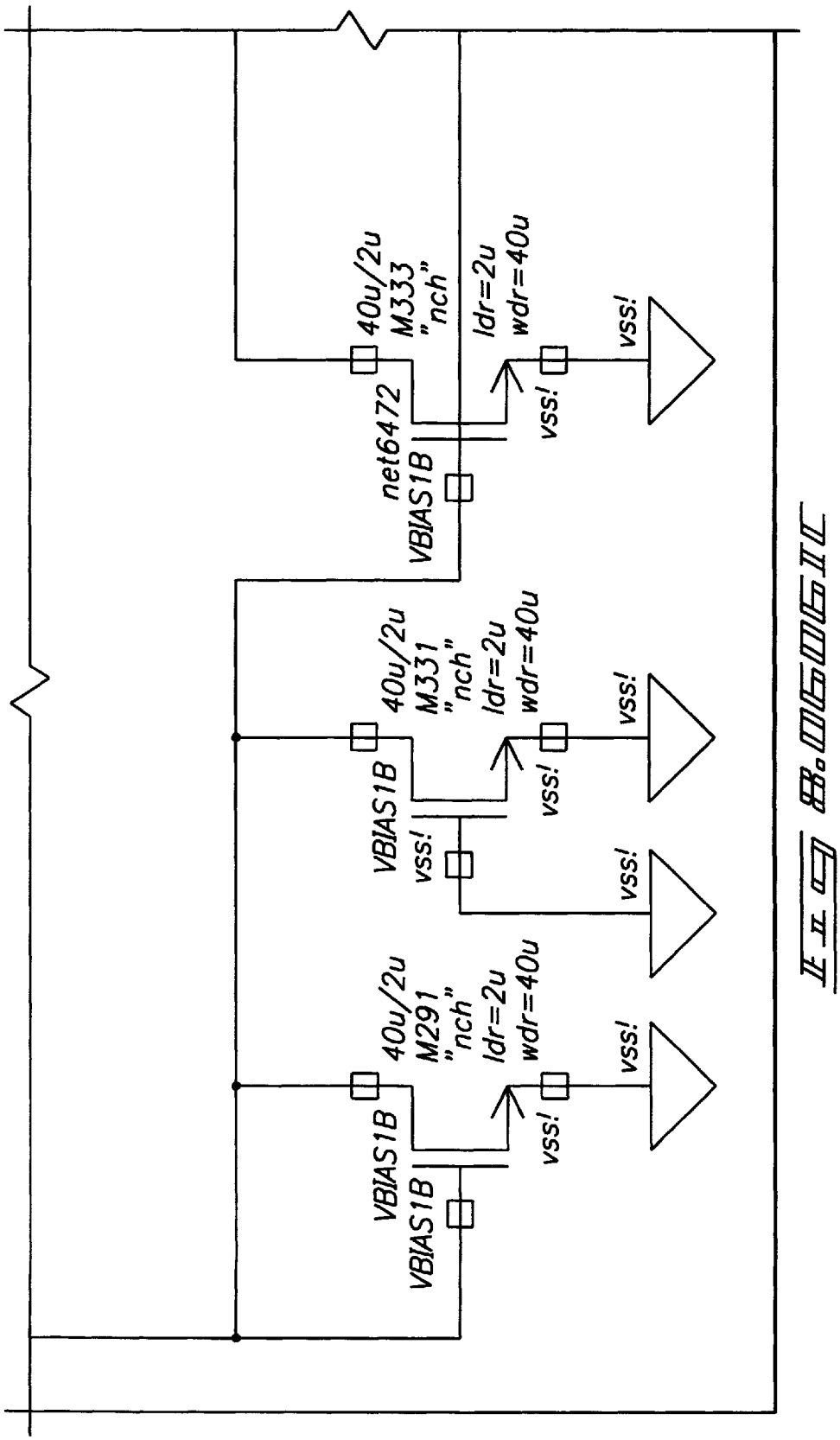


FIG 88.0050IIC

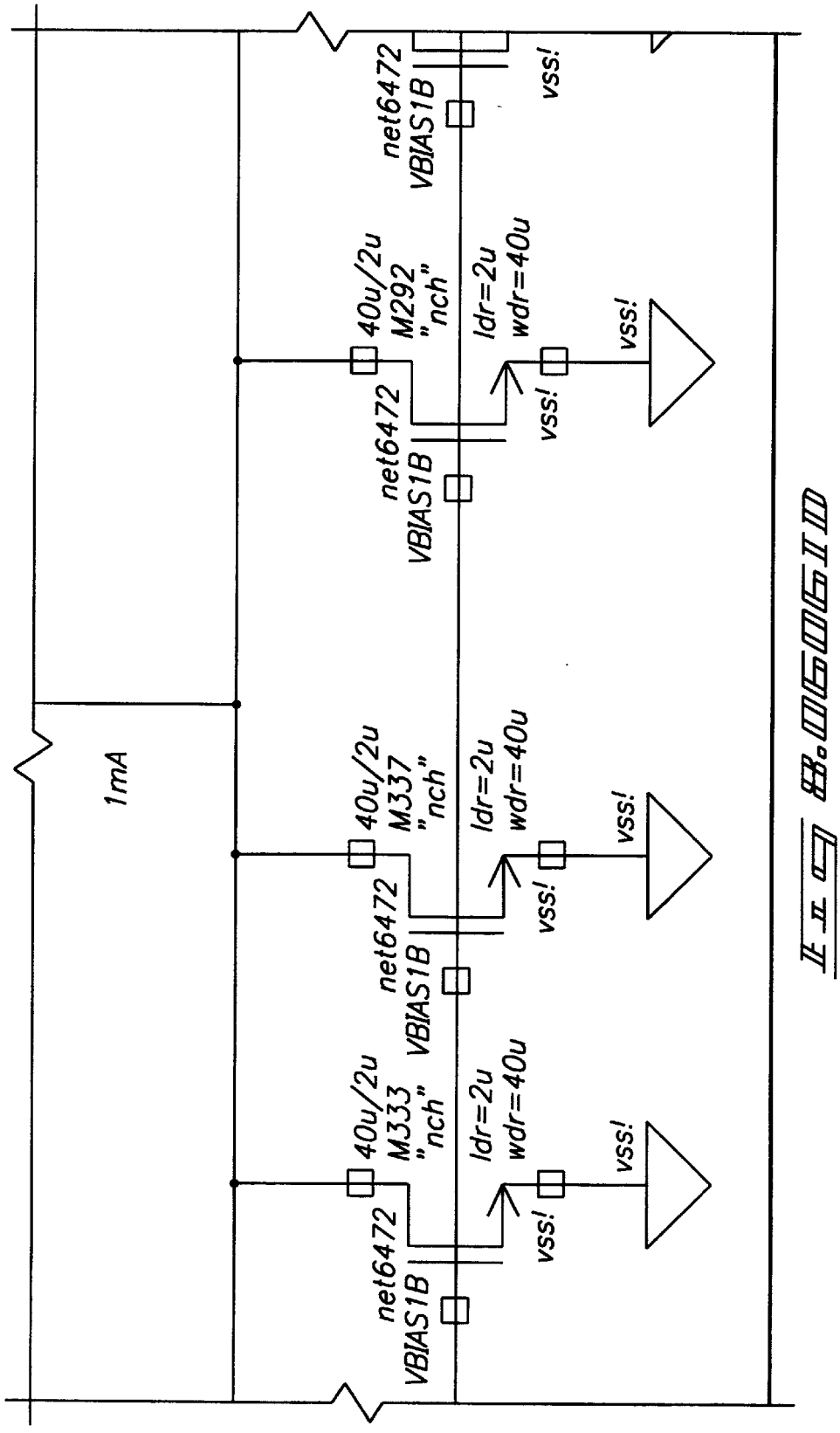


FIG. 88.0(5)(5)(11)(D)

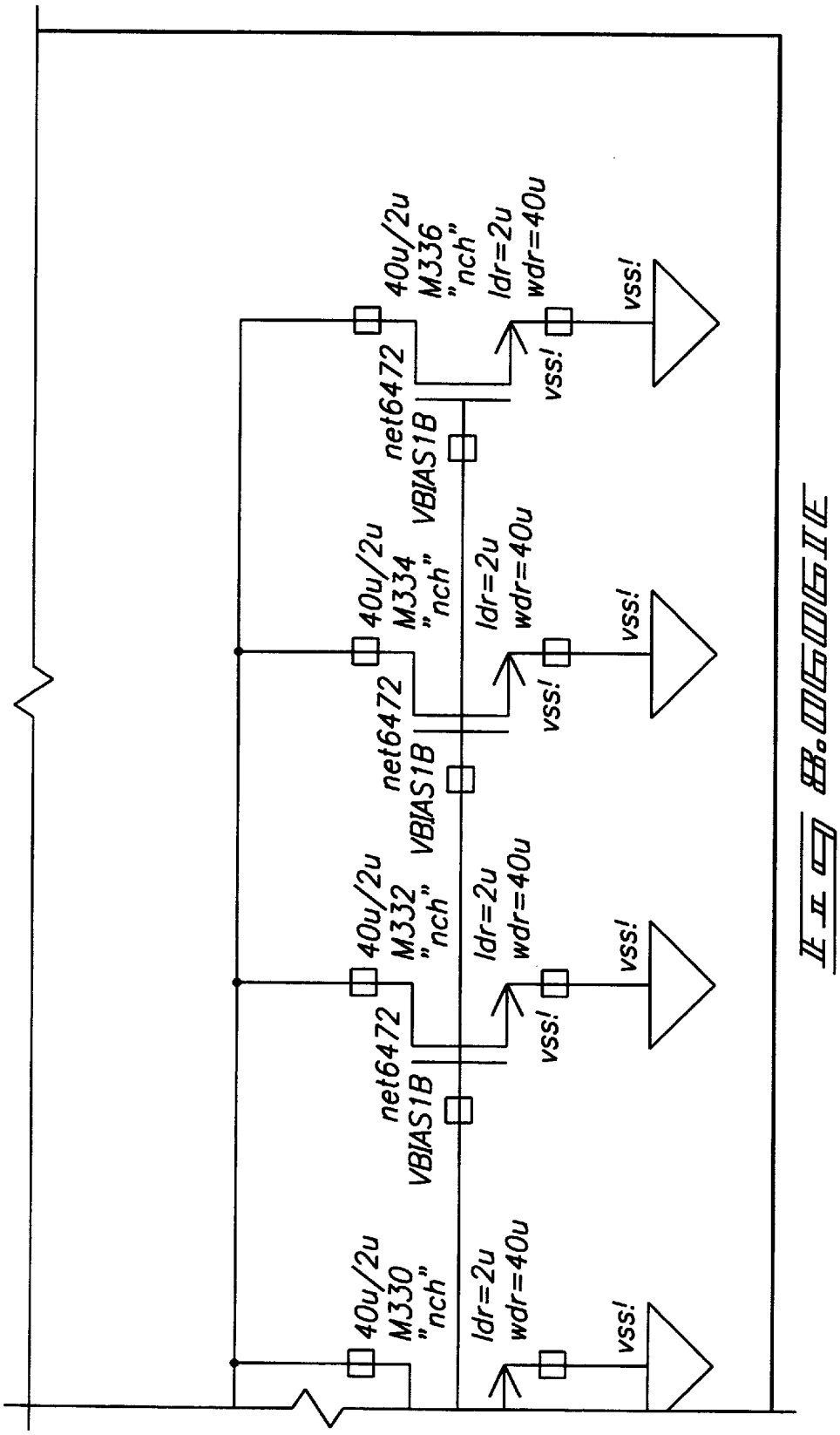
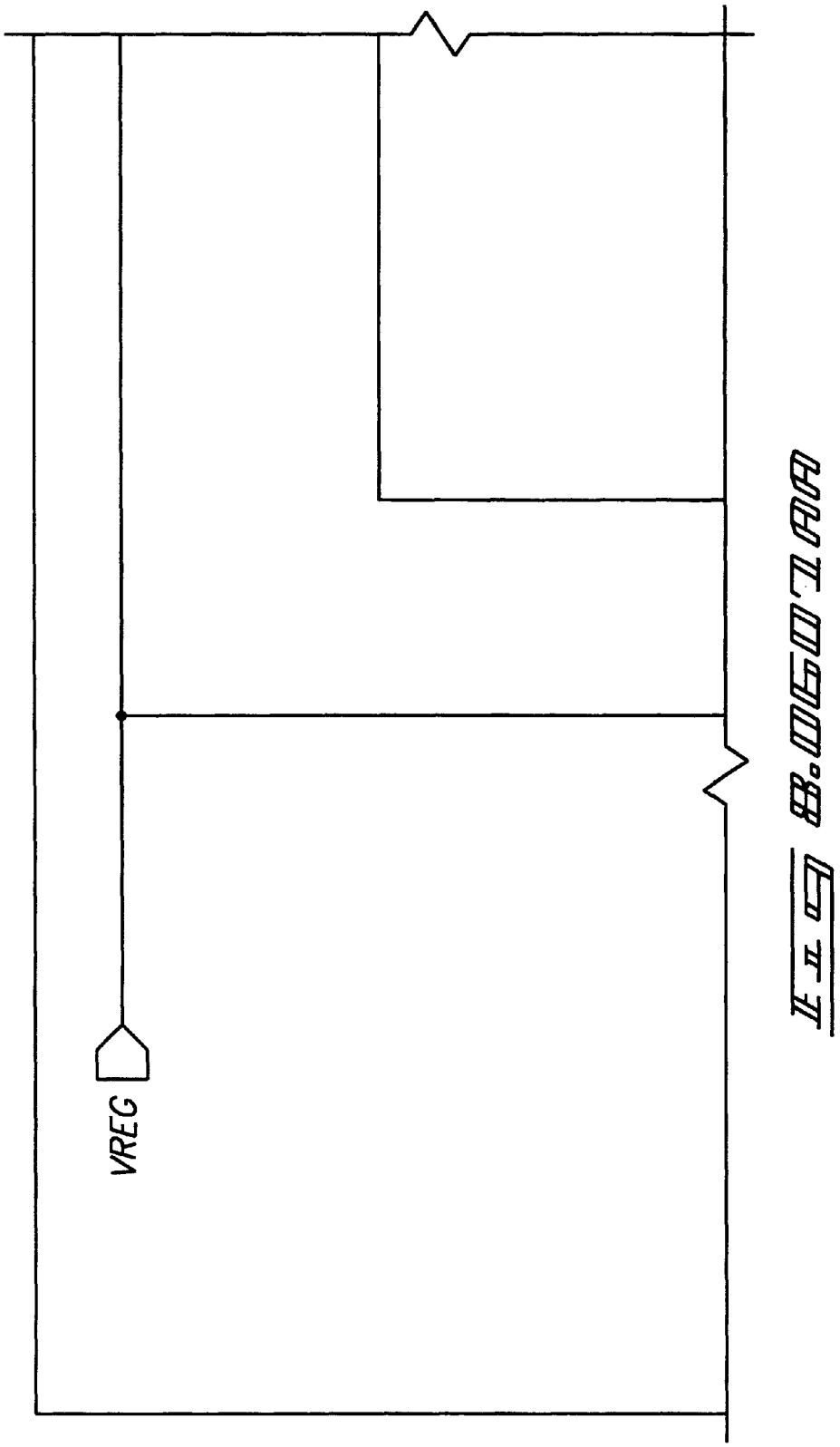


FIG. 88.0S0S11E

8.0607AA	8.0607AB	8.0607AC	8.0607AD	8.0607AE	8.0607AF	8.0607AG	8.0607AH	8.0607AI	8.0607AJ
8.0607BA	8.0607BB	8.0607BC	8.0607BD	8.0607BE	8.0607BF	8.0607BG	8.0607BH	8.0607BI	8.0607BJ
8.0607CA	8.0607CB	8.0607CC	8.0607CD	8.0607CE	8.0607CF	8.0607CG	8.0607CH	8.0607CI	8.0607CJ
8.0607DA	8.0607DB	8.0607DC	8.0607DD	8.0607DE	8.0607DF	8.0607DG	8.0607DH	8.0607DI	8.0607DJ
8.0607EA	8.0607EB	8.0607EC	8.0607ED	8.0607EE	8.0607EF	8.0607EG	8.0607EH	8.0607EI	8.0607EJ
8.0607FA	8.0607FB	8.0607FC	8.0607FD	8.0607FE	8.0607FF	8.0607FG	8.0607FH	8.0607FI	8.0607FJ
8.0607GA	8.0607GB	8.0607GC	8.0607GD	8.0607GE	8.0607GF	8.0607GG	8.0607GH	8.0607GI	8.0607GJ
8.0607HA	8.0607HB	8.0607HC	8.0607HD	8.0607HE	8.0607HF	8.0607HG	8.0607HH	8.0607HI	8.0607HJ
8.0607IA	8.0607IB	8.0607IC	8.0607ID	8.0607IE	8.0607IF	8.0607IG	8.0607IH	8.0607II	8.0607IJ
8.0607JA	8.0607JB	8.0607JC	8.0607JD	8.0607JE	8.0607JF	8.0607JG	8.0607JH	8.0607JI	8.0607JJ

FIG. 8.0607JJ


VREG
88.0850 FIG

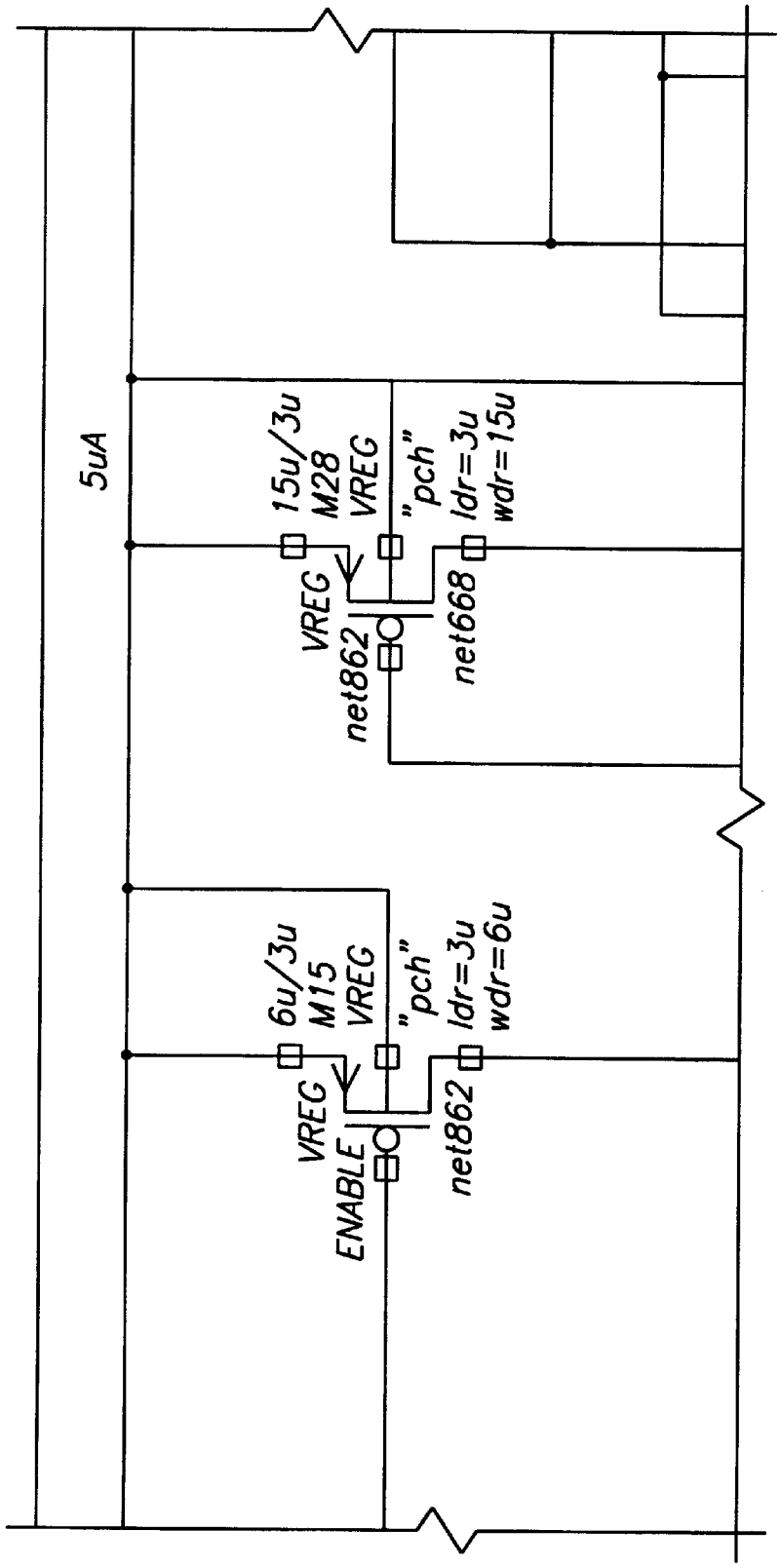


FIG 88.0501AB

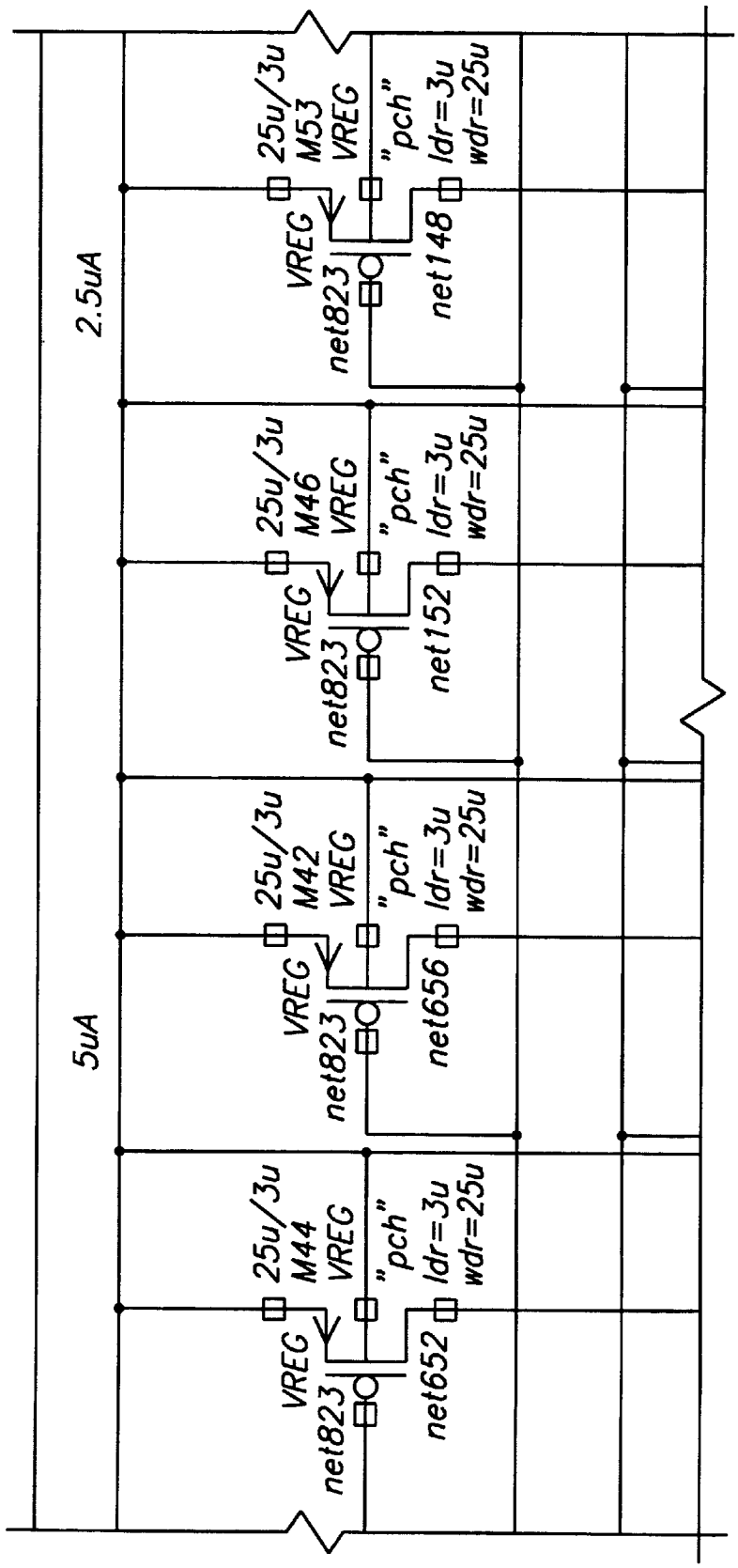


FIG. 88.0050 ALA

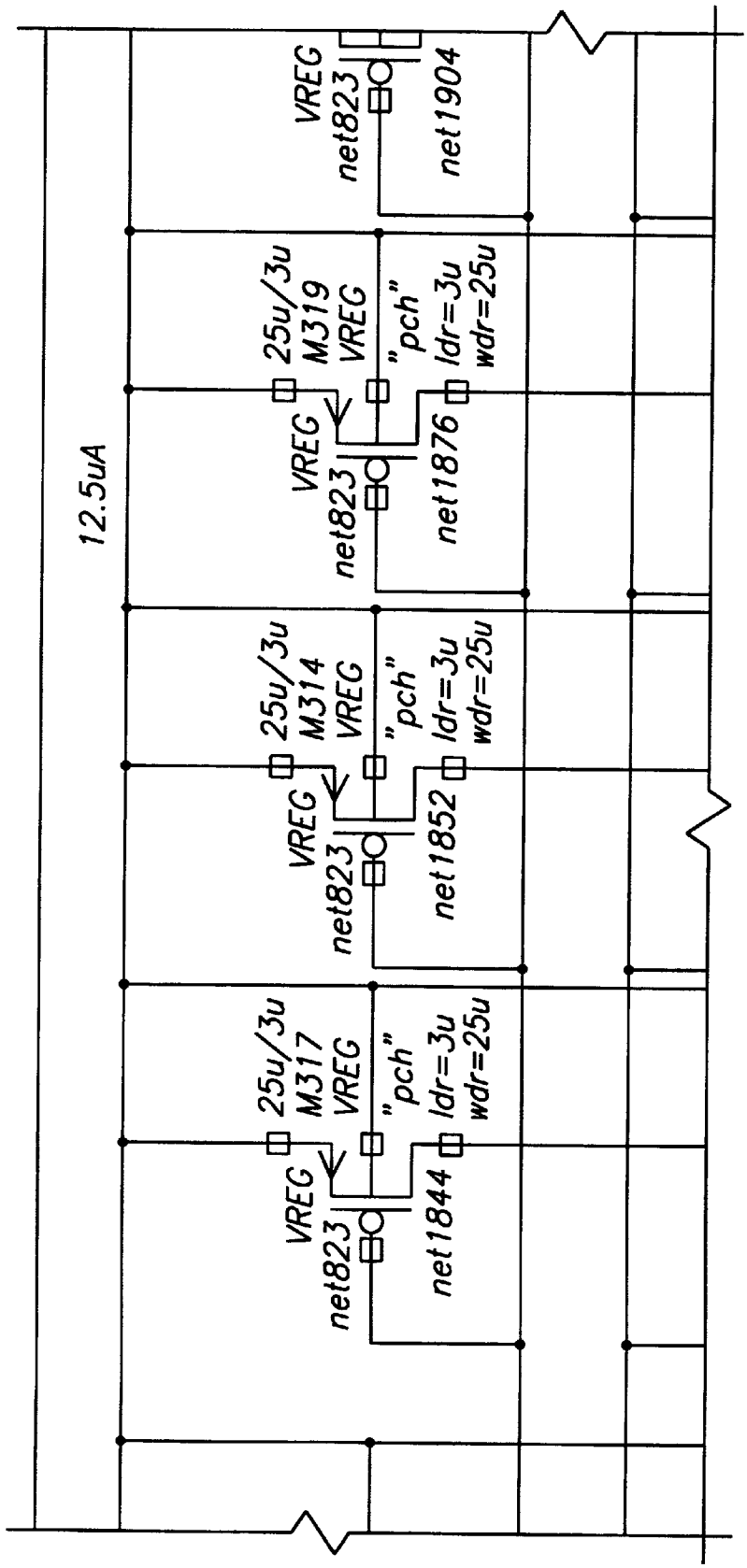


FIG 88.0501AD

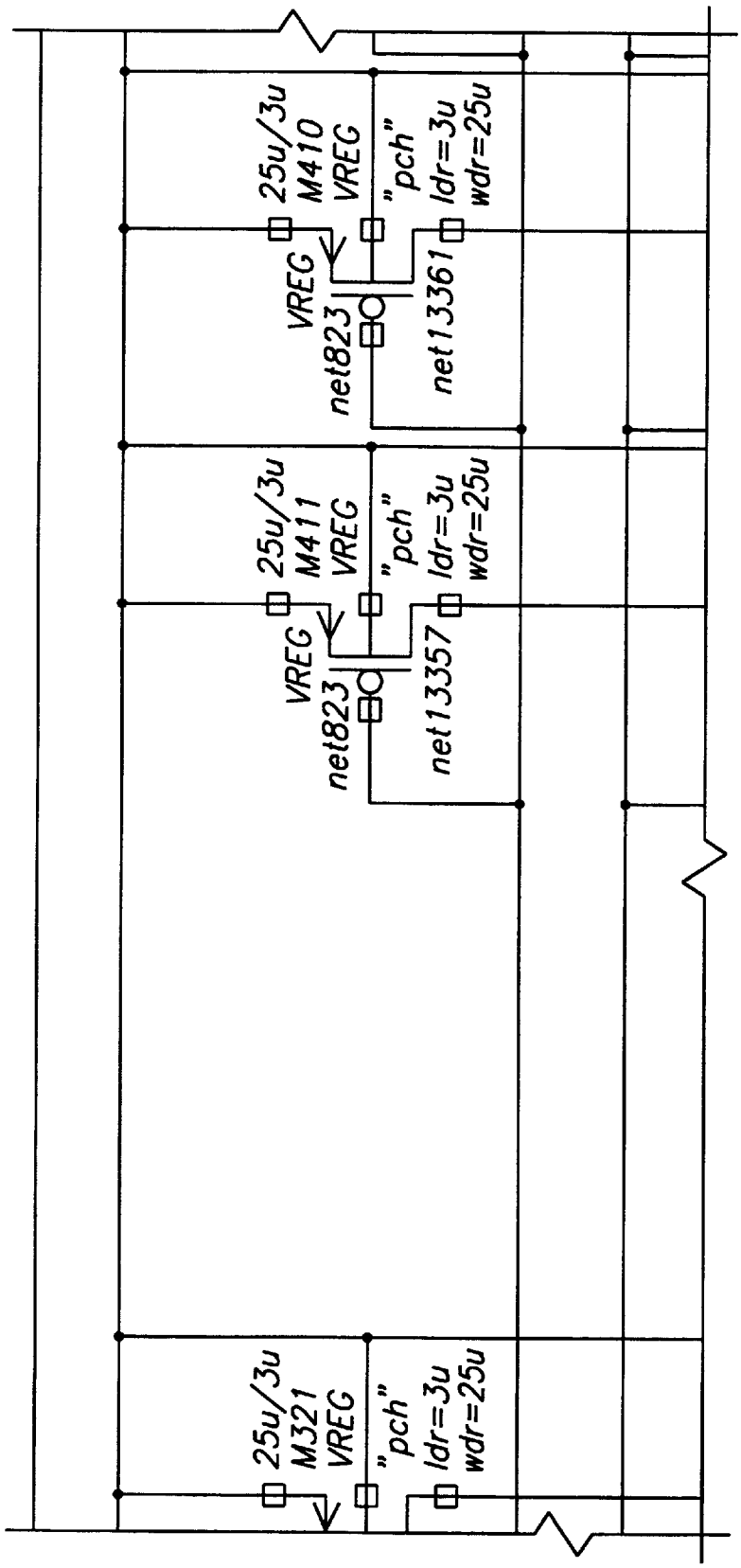


FIG 8.0600 ALE

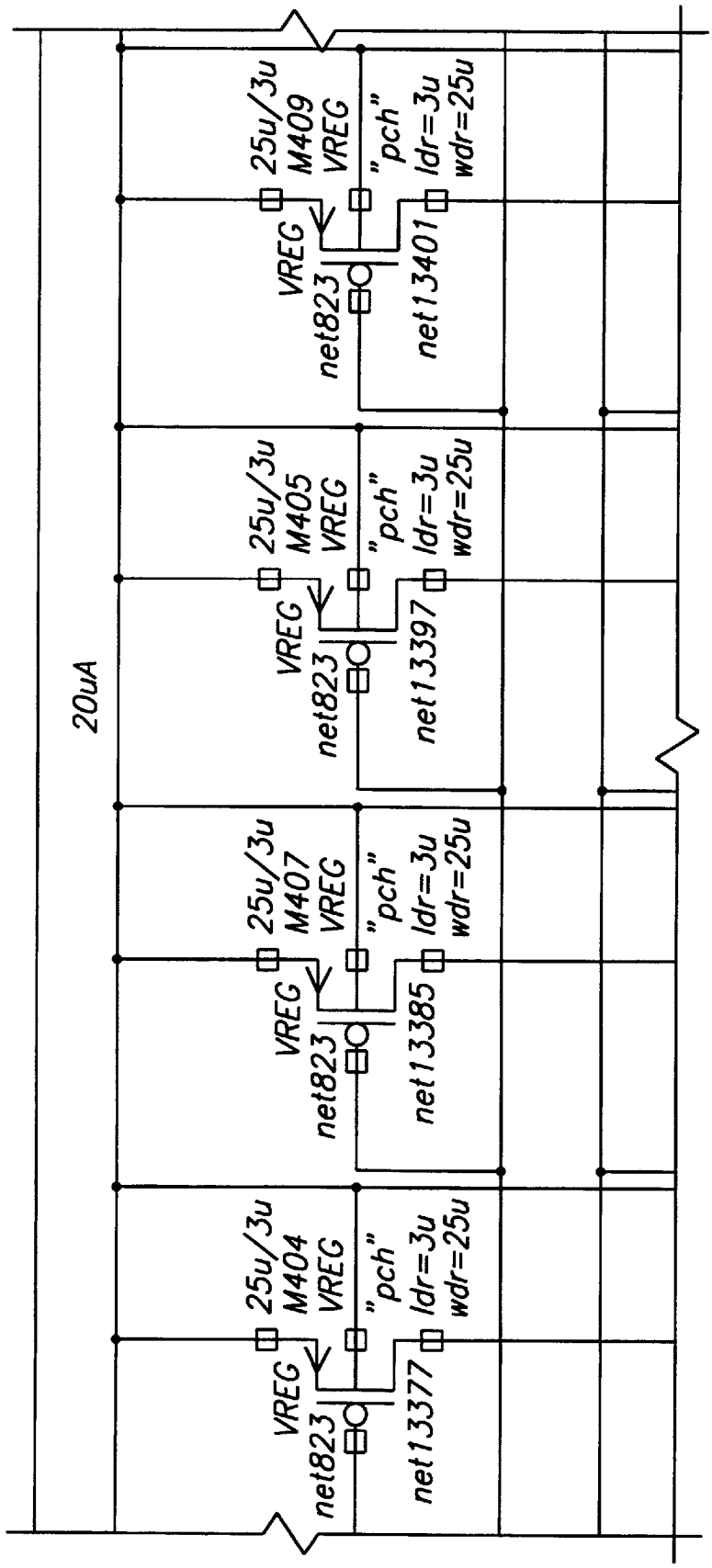

20uA
25u/3u
M409
VREG
"pch"
ldr=3u
wdr=25u
VREG
net823
net13401
25u/3u
M405
VREG
"pch"
ldr=3u
wdr=25u
VREG
net823
net13397
25u/3u
M407
VREG
"pch"
ldr=3u
wdr=25u
VREG
net823
net13385
25u/3u
M404
VREG
"pch"
ldr=3u
wdr=25u
VREG
net823
net13377

FIG 8.0501 AF

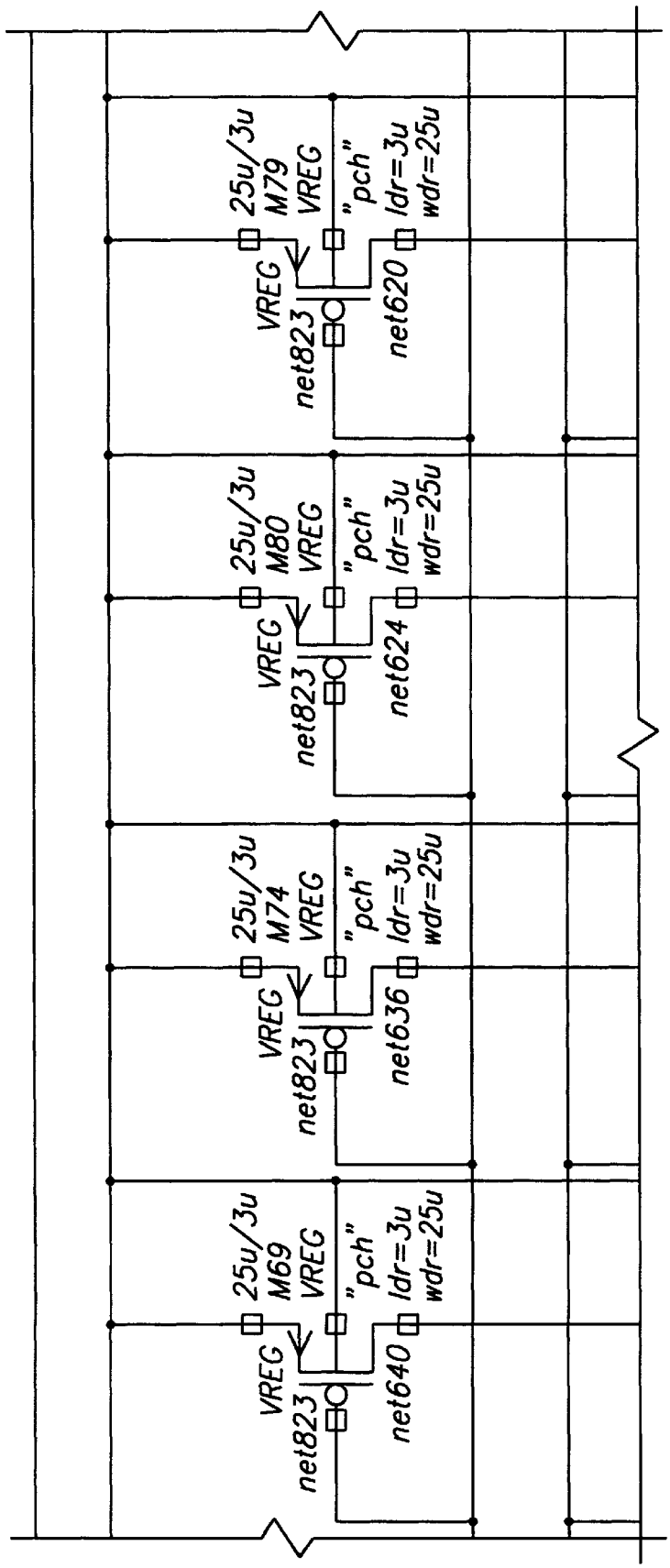


FIG 88.0050 (PRIOR ART)

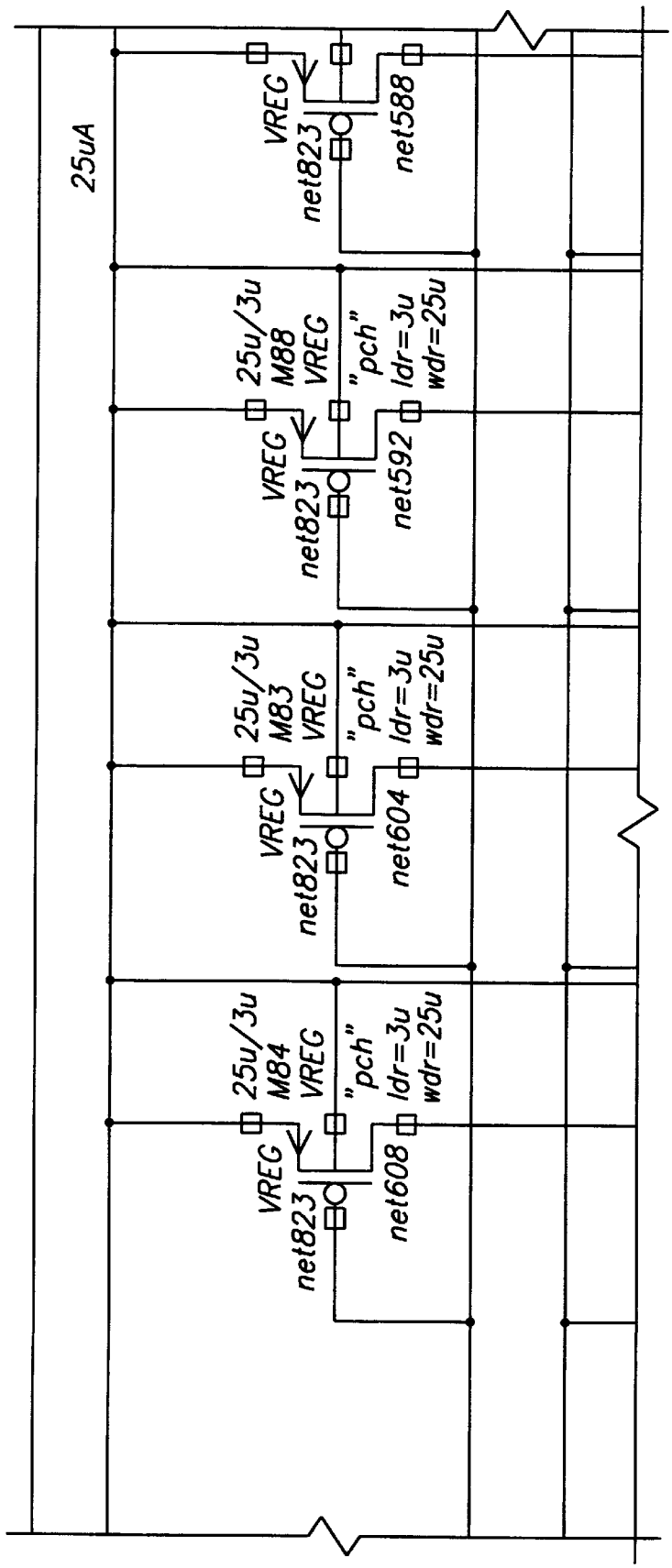

25uA
VREG
net823
net588
25u/3u
M88
VREG
"pch"
ldr=3u
wdr=25u
net592
25u/3u
M83
net604
25u/3u
M84
net608

FIG. 88.005 (AH)

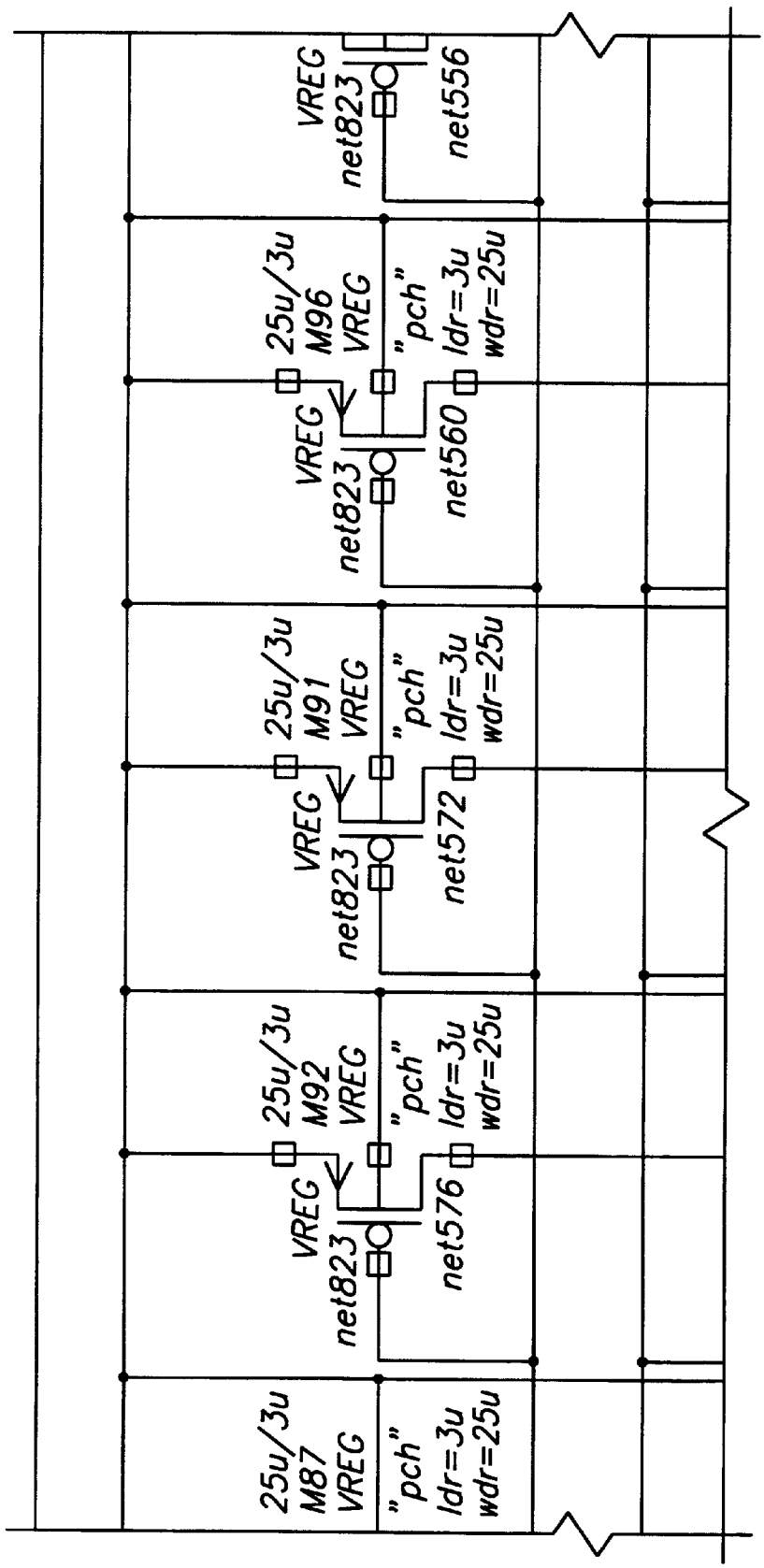
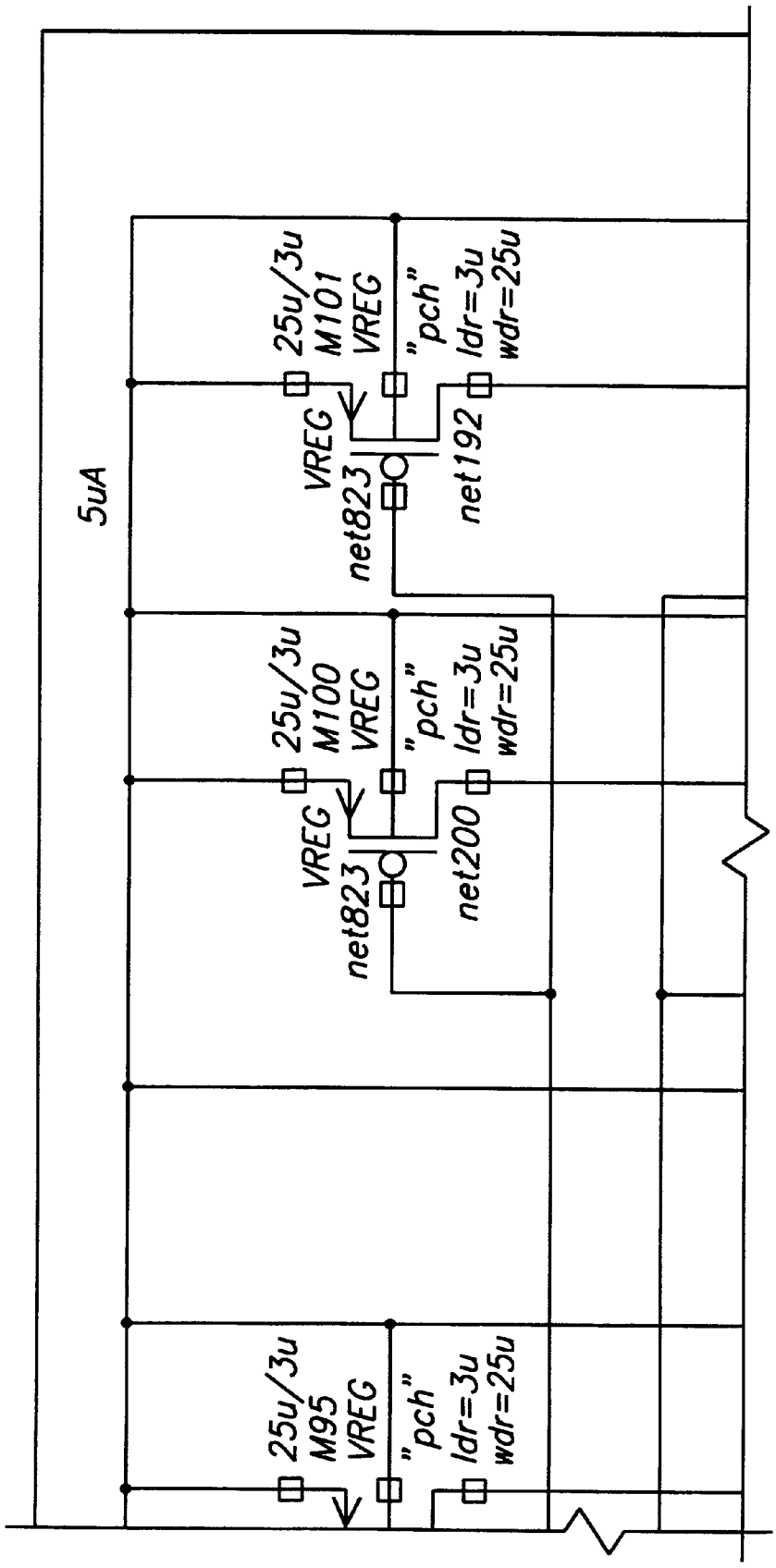
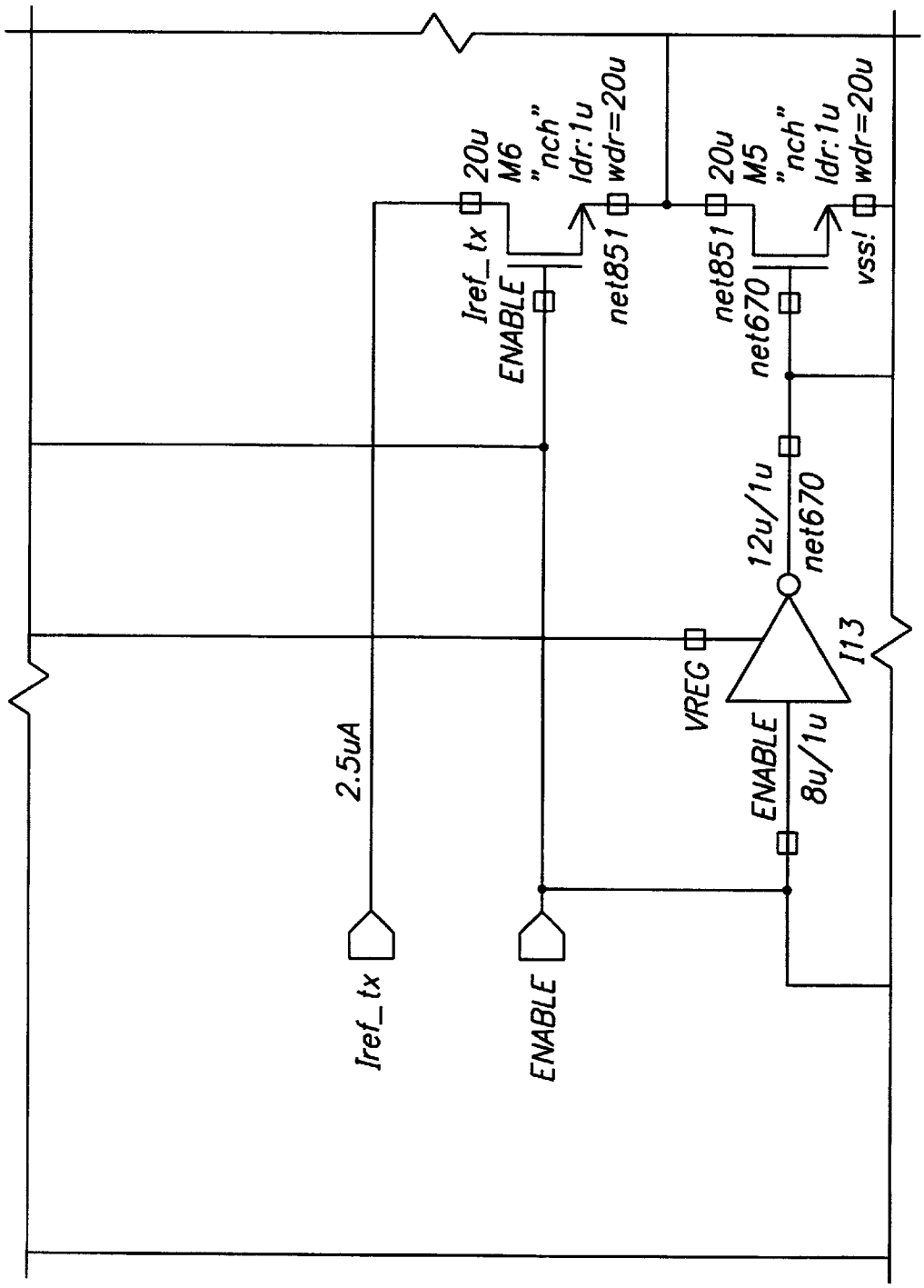


FIG 8.0501 AII


5uA
25u/3u
M101
VREG
"pch"
ldr=3u
wdr=25u
VREG
net823
net192
25u/3u
M100
VREG
"pch"
ldr=3u
wdr=25u
VREG
net823
net200
25u/3u
M95
VREG
"pch"
ldr=3u
wdr=25u

Фиг. 8.0500 Ad



Фиг. 88.00511 IBM

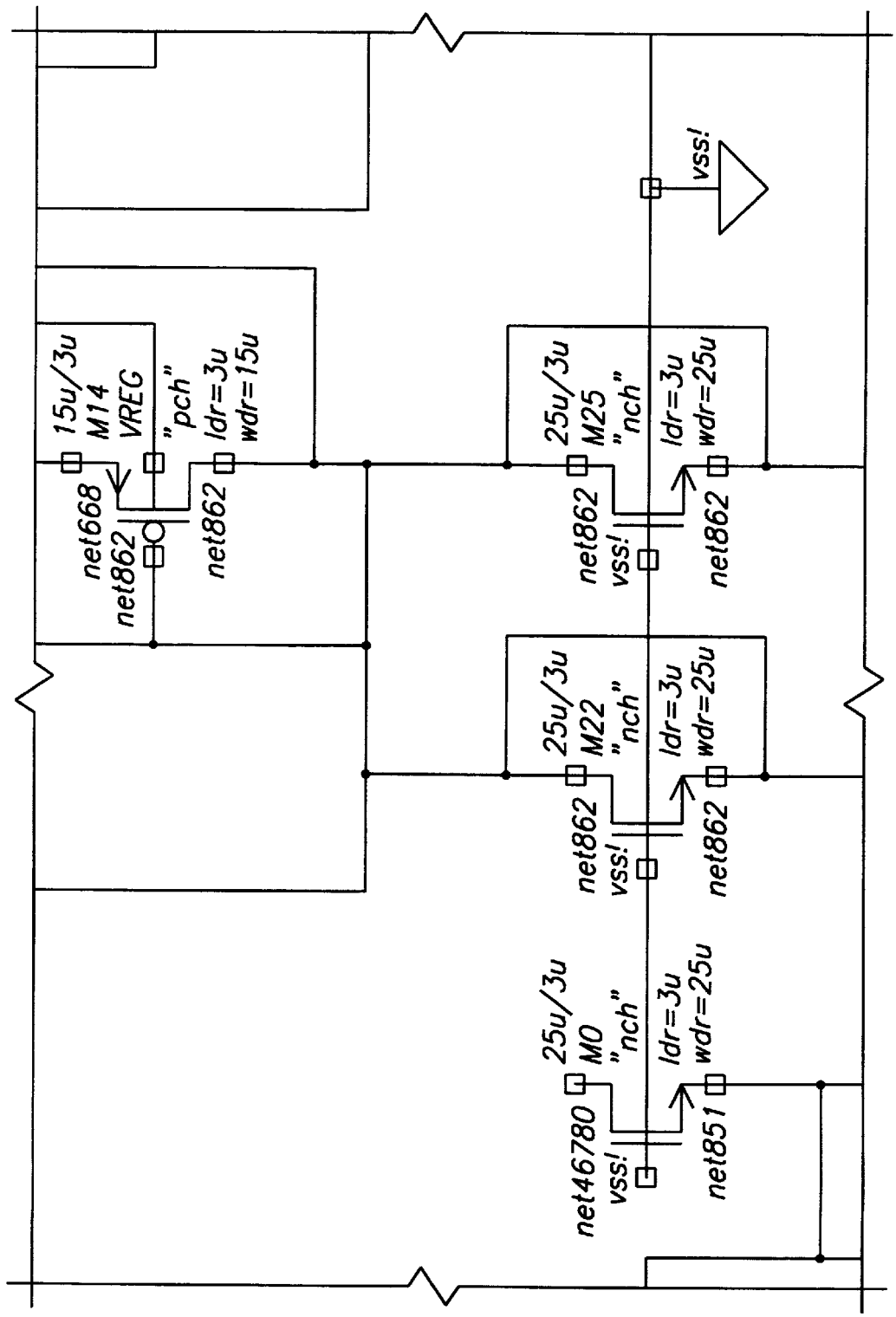

vss!
15u/3u
M14
VREG
"pch"
ldr=3u
wdr=15u
net668
net862
net862
25u/3u
M25
"nch"
ldr=3u
wdr=25u
net862
vss!
net862
25u/3u
M22
"nch"
ldr=3u
wdr=25u
net862
vss!
net862
25u/3u
M0
"nch"
ldr=3u
wdr=25u
net46780
vss!
net851

FIG 88.0050

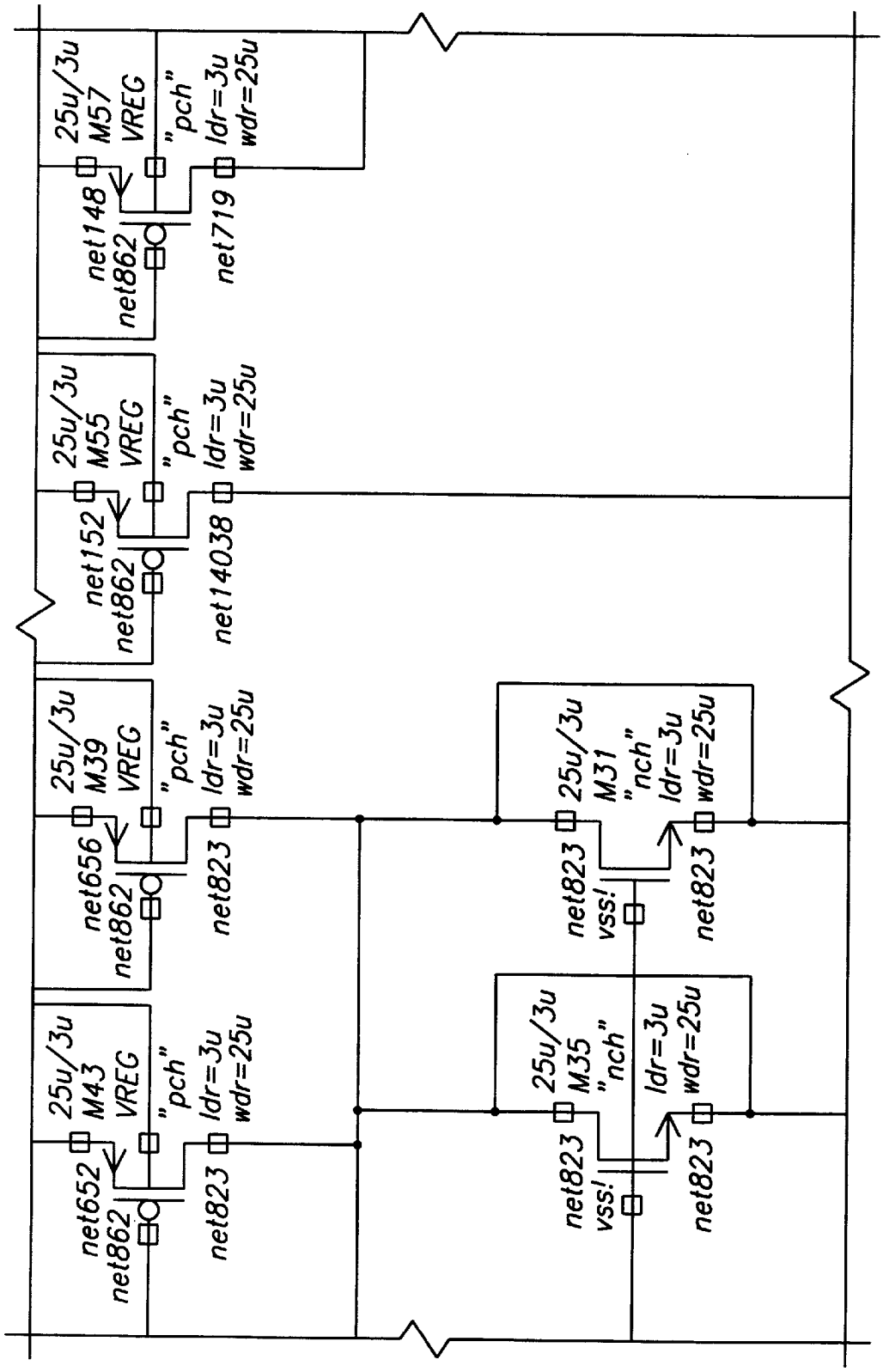


FIG 8.0501 IBC

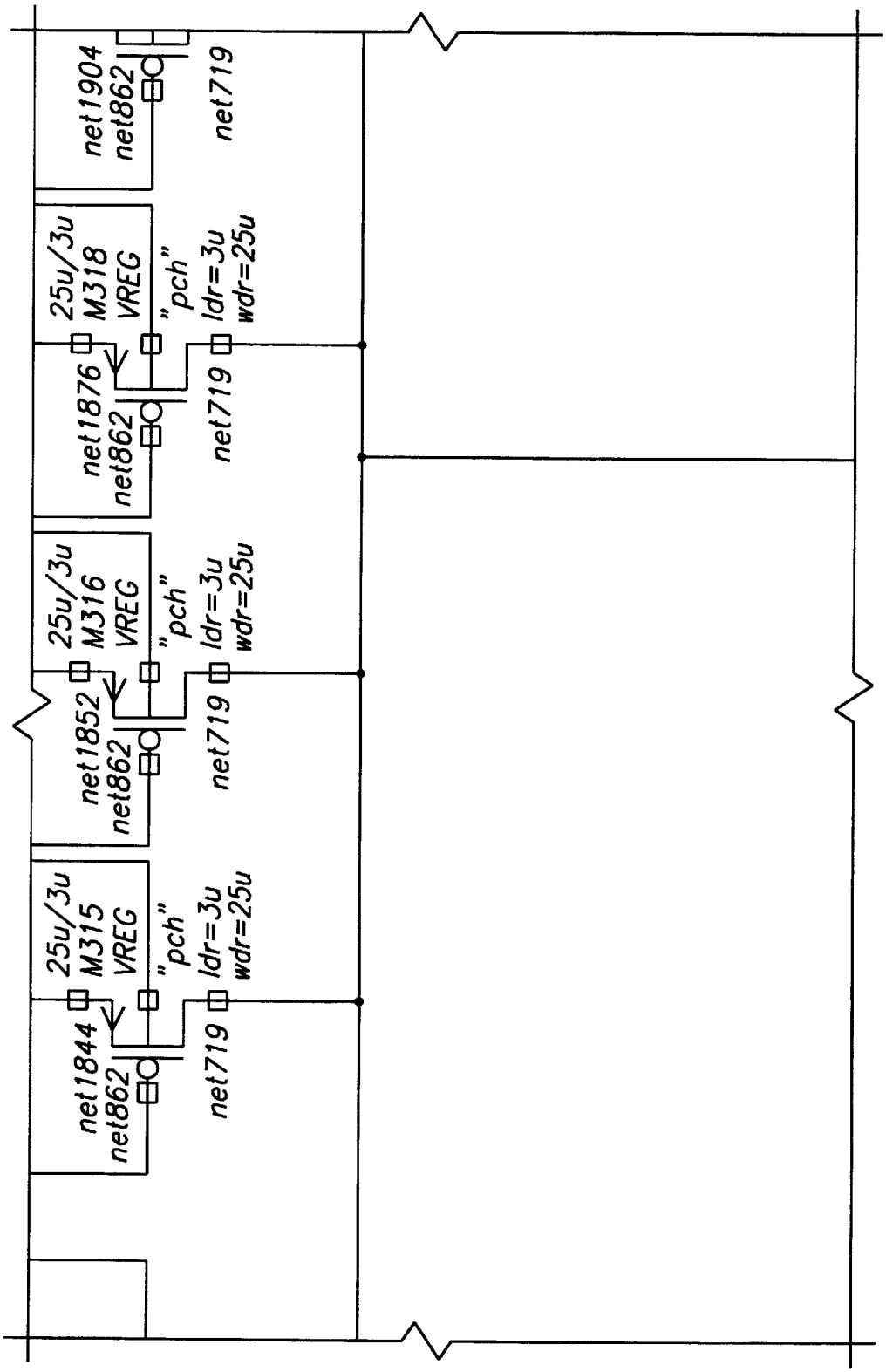


FIG 98,050,188

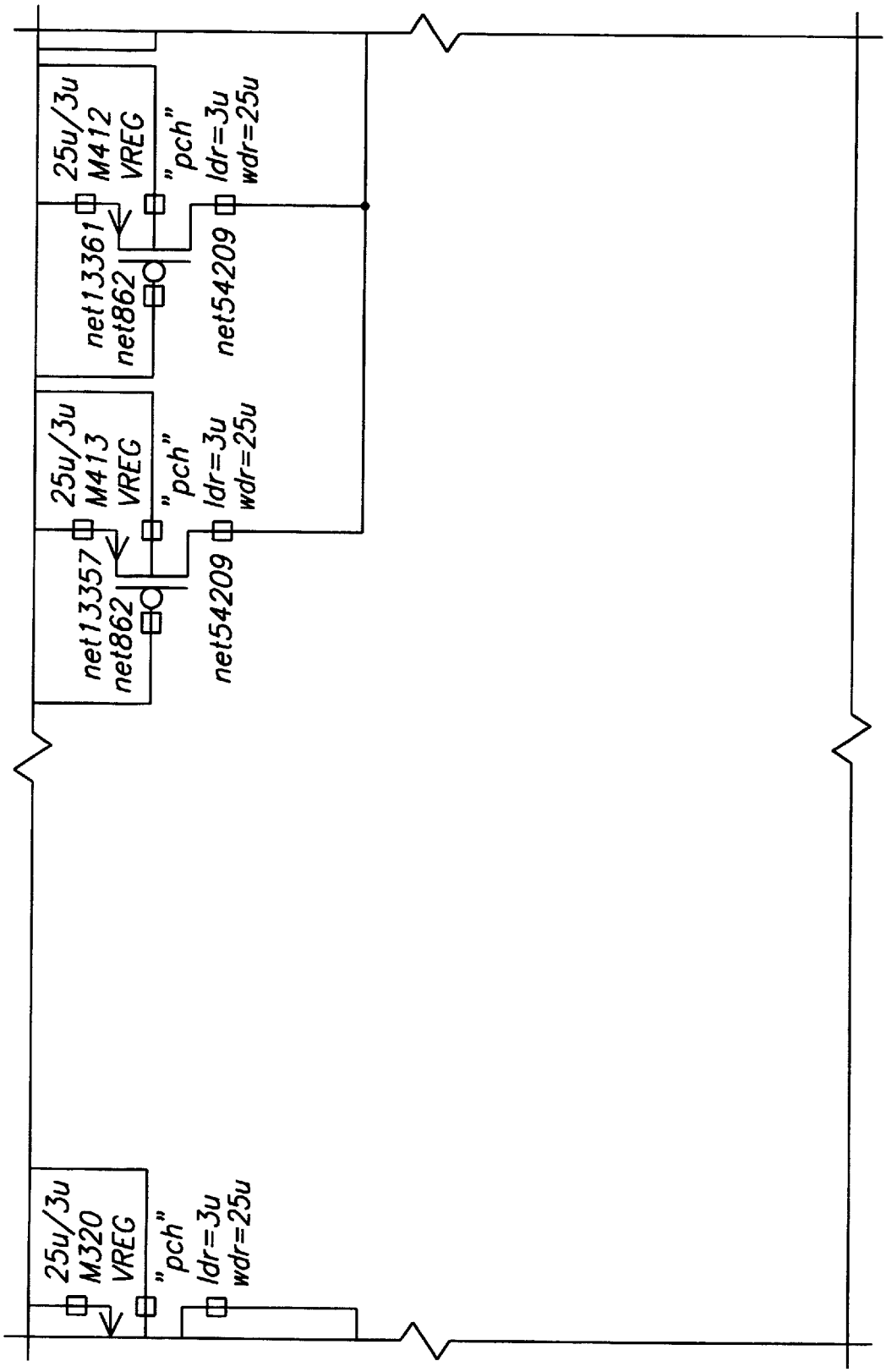


FIG 88.0501 IBE

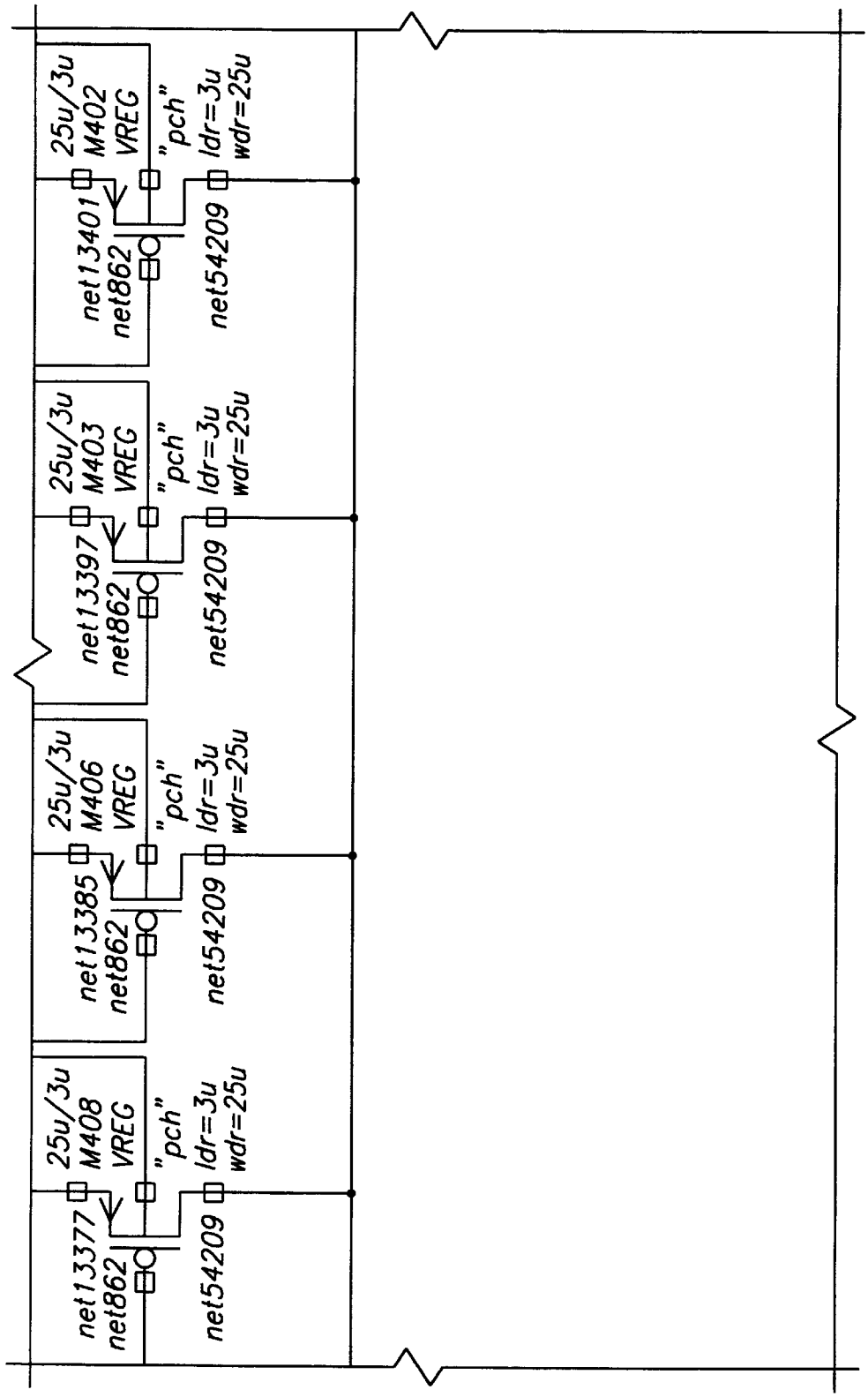


FIG 88.0601A IBF

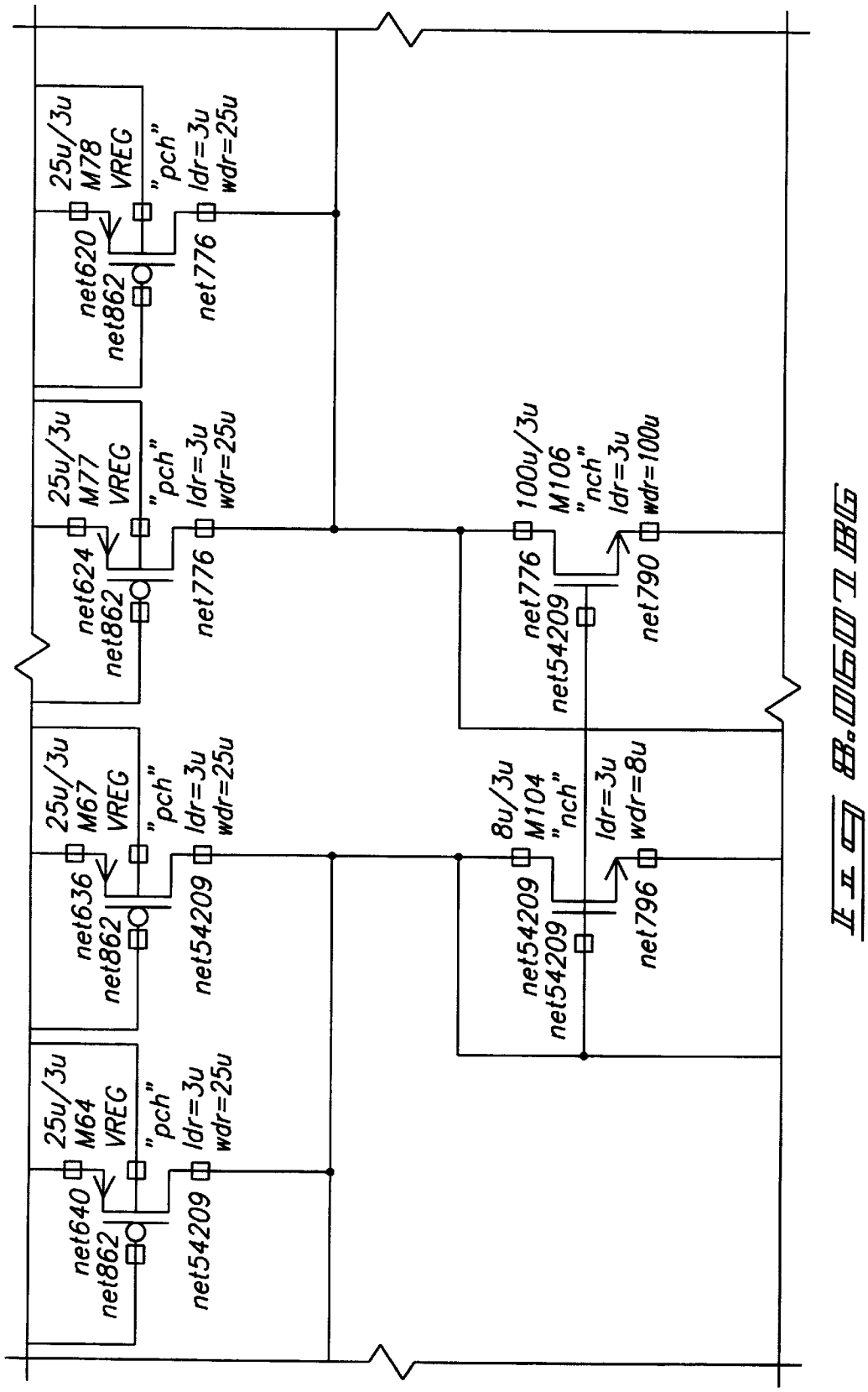

25u/3u
M78
VREG
"pch"
ldr=3u
wdr=25u
net620
net862
net776
25u/3u
M77
VREG
"pch"
ldr=3u
wdr=25u
net624
net862
net776
100u/3u
M106
"nch"
ldr=3u
wdr=100u
net776
net54209
net790
25u/3u
M67
VREG
"pch"
ldr=3u
wdr=25u
net636
net862
net54209
8u/3u
M104
"nch"
ldr=3u
wdr=8u
net54209
net54209
net796
25u/3u
M64
VREG
"pch"
ldr=3u
wdr=25u
net640
net862
net54209

FIG 88.0500

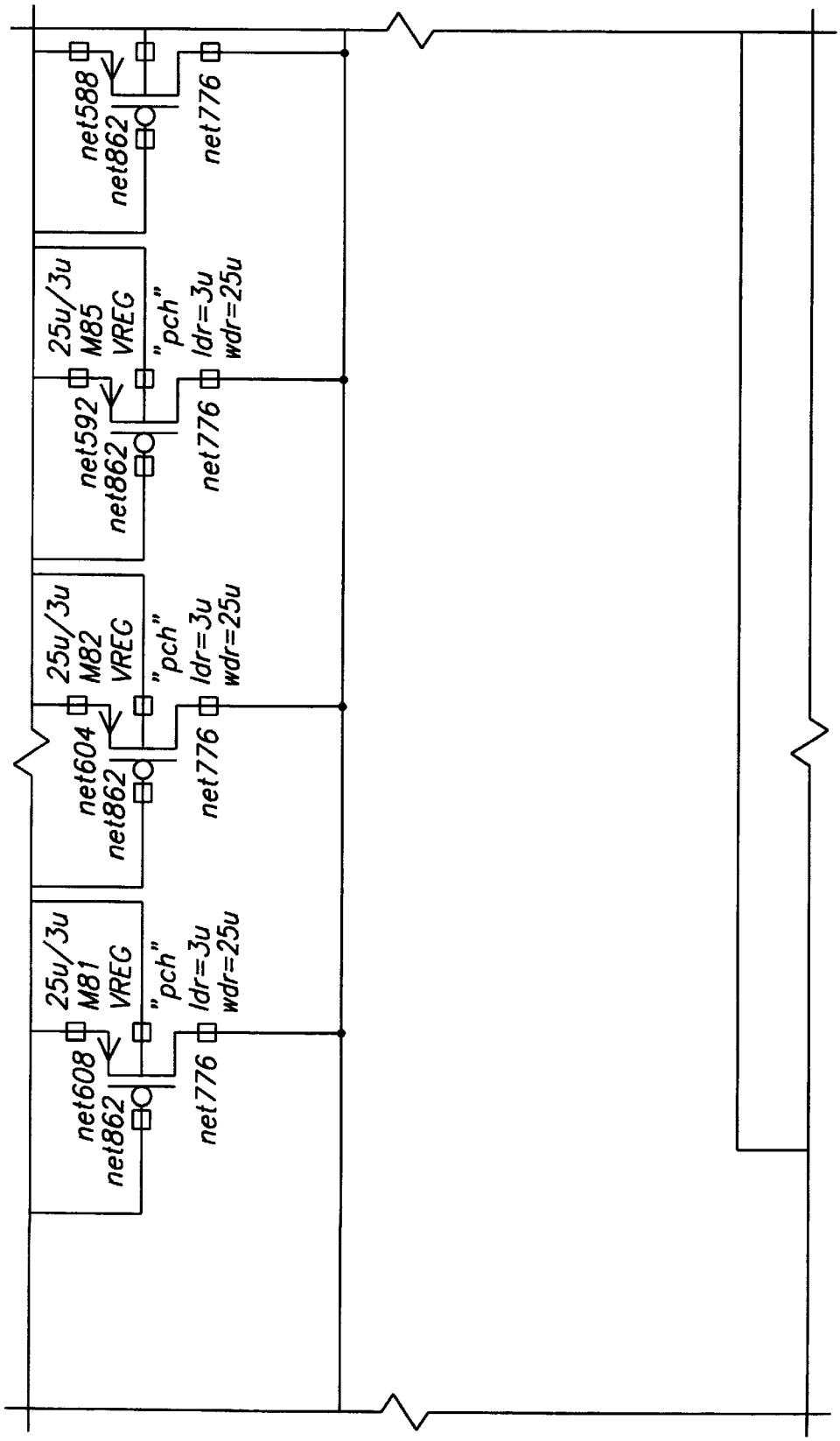


FIG. 88.0501 (BH)

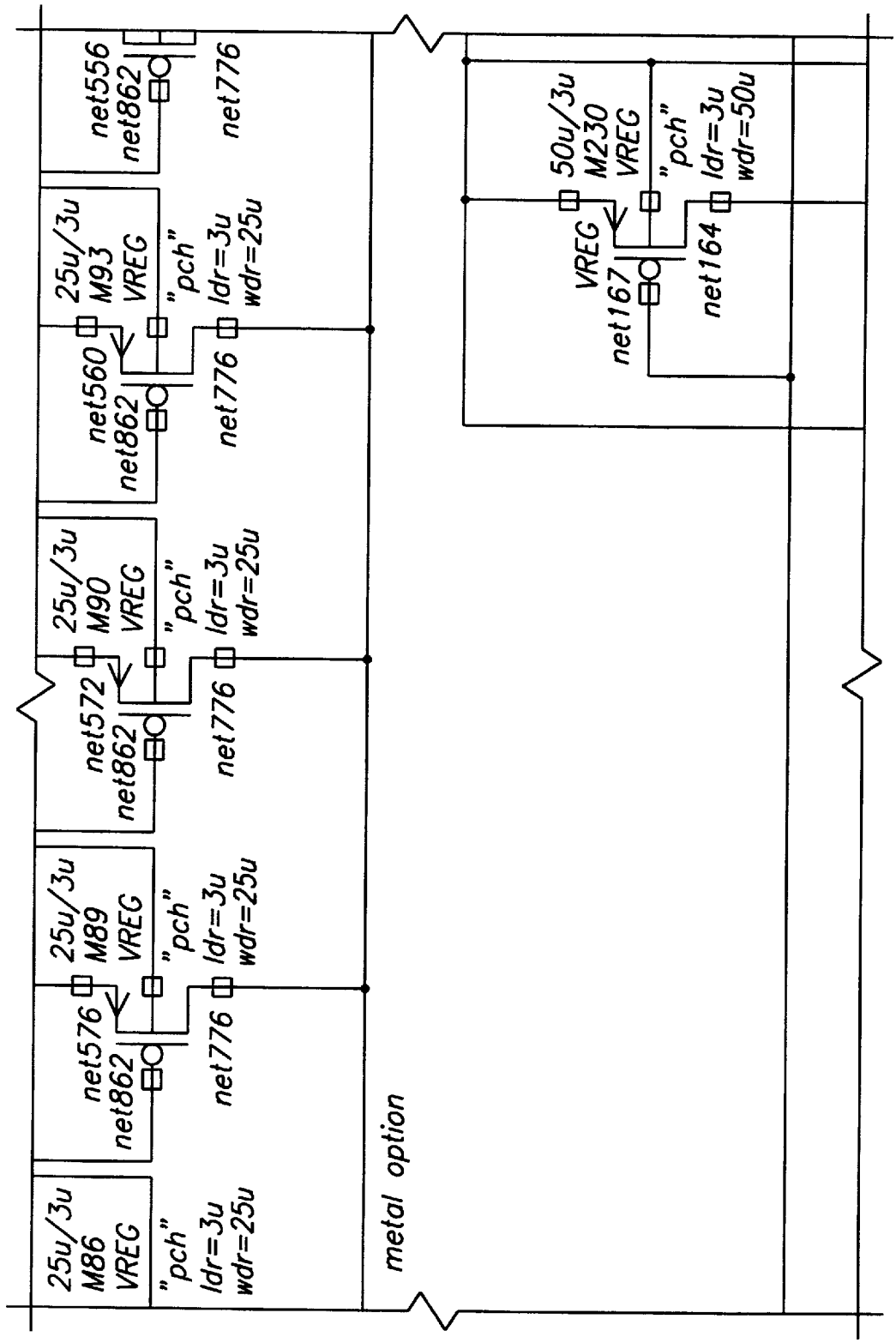

25u/3u
M86
VREG
"pch"
ldr=3u
wdr=25u
net576
net862
net772
net862
net560
net862
net556
net862
net776
metal option
50u/3u
M230
VREG
"pch"
ldr=3u
wdr=50u
VREG
net167
net164

FIG. 8,050,II

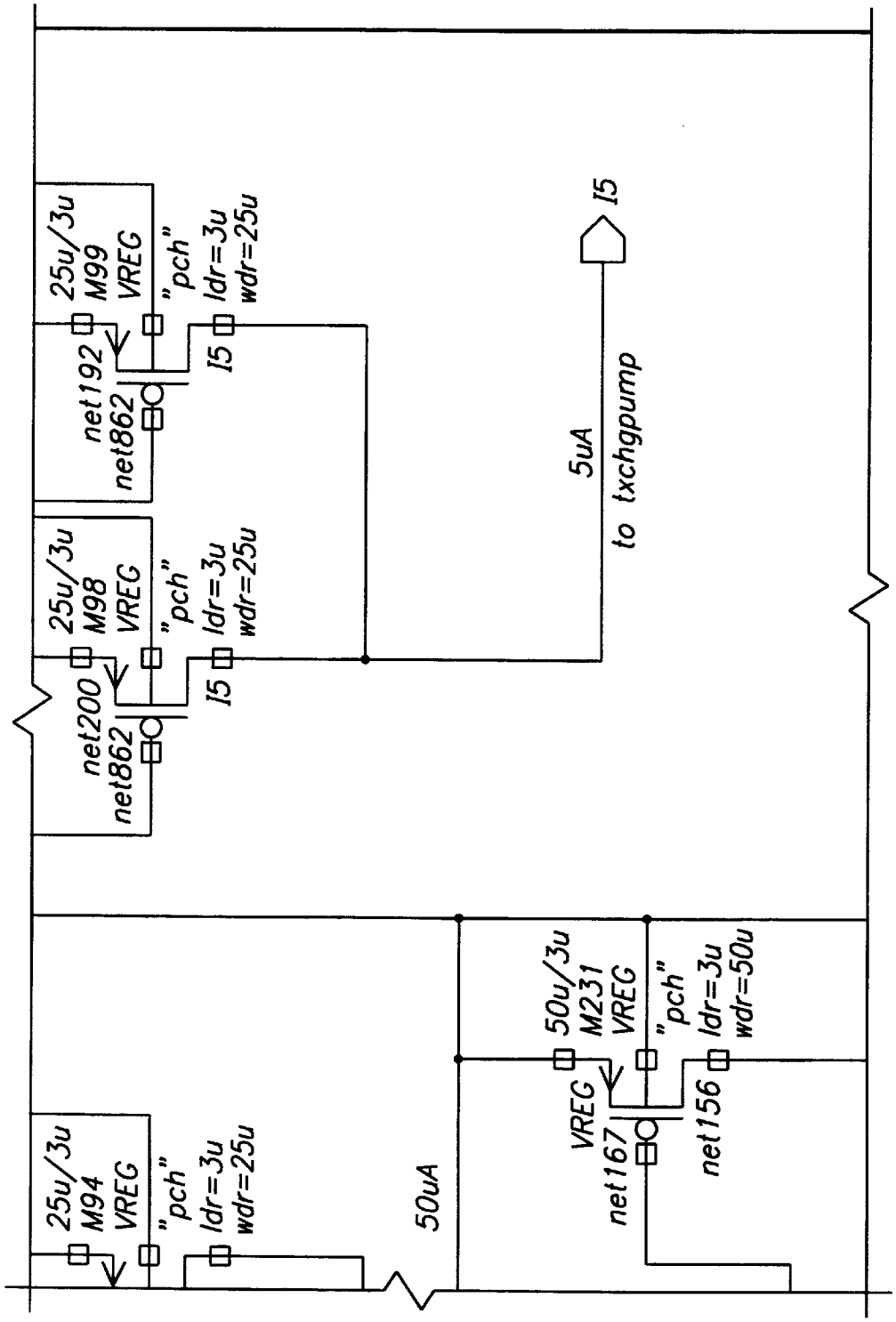
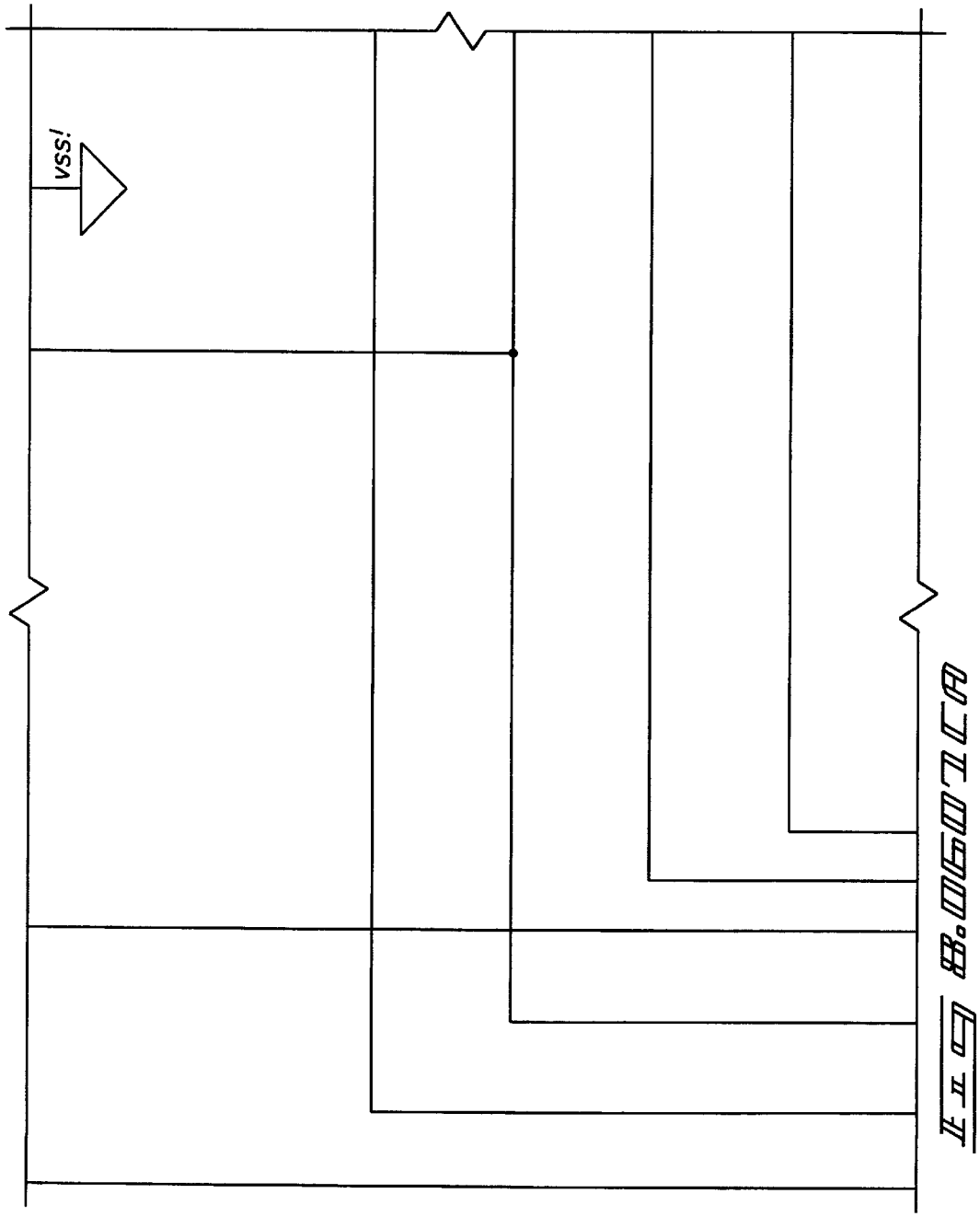

25u/3u
M99
VREG
"pch"
ldr=3u
wdr=25u
I5
net192
net862
25u/3u
M98
VREG
"pch"
ldr=3u
wdr=25u
I5
net200
net862
I5
5uA
to txchgpump
50u/3u
M231
VREG
"pch"
ldr=3u
wdr=50u
VREG
net167
net156
25u/3u
M94
VREG
"pch"
ldr=3u
wdr=25u
50uA

FIG. 88,050


vss!
FIG. 88.0590A

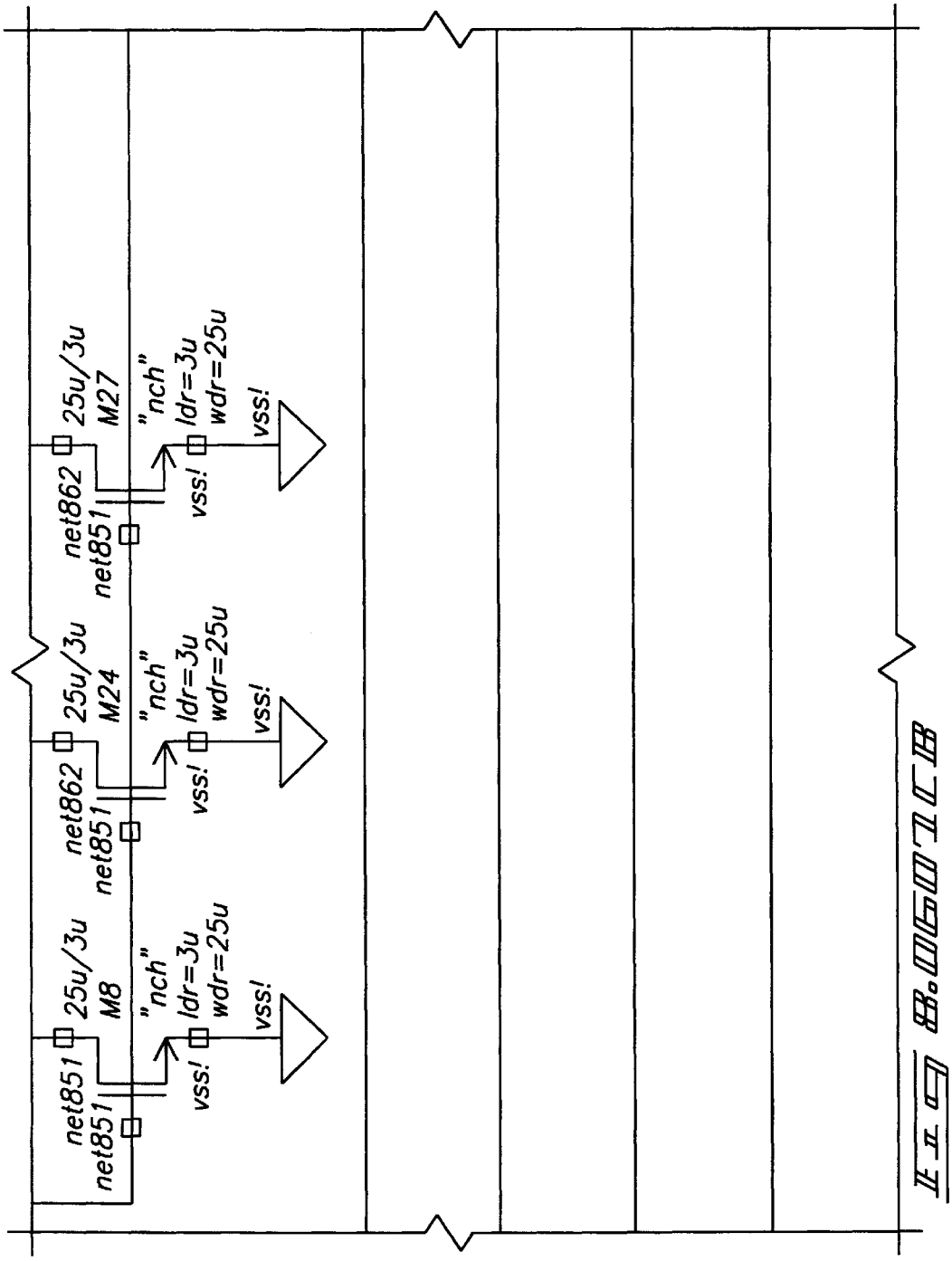

net851
net851
25u/3u
M8
"nch"
ldr=3u
wdr=25u
vss!
vss!
net862
net851
25u/3u
M24
"nch"
ldr=3u
wdr=25u
vss!
vss!
net862
net851
25u/3u
M27
"nch"
ldr=3u
wdr=25u
vss!
vss!

FIG 31

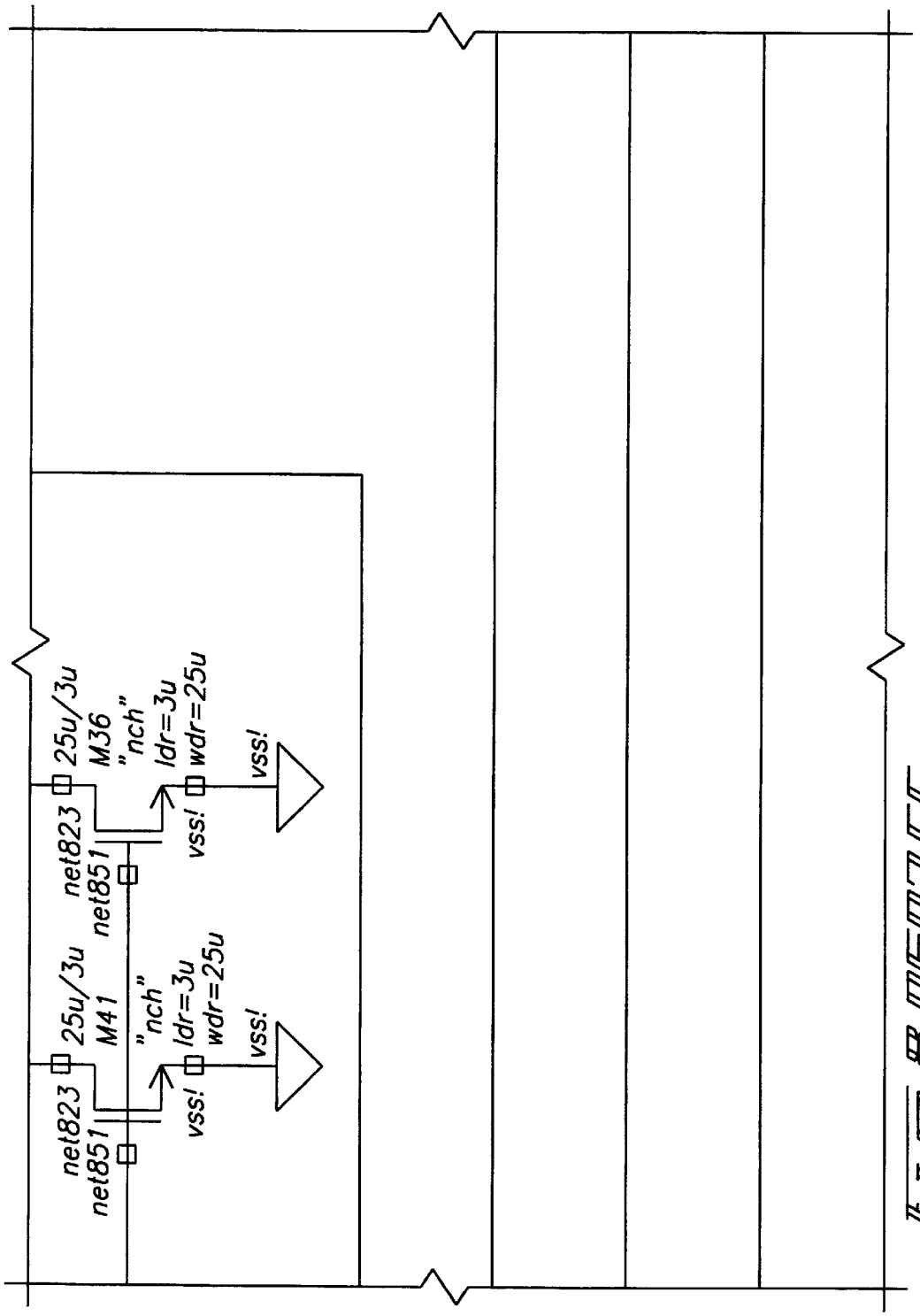

25u/3u
M36
"nch"
ldr=3u
wdr=25u
vss!
net823
net851
vss!
25u/3u
M41
"nch"
ldr=3u
wdr=25u
vss!
net823
net851
vss!

FIG. 8,050,211

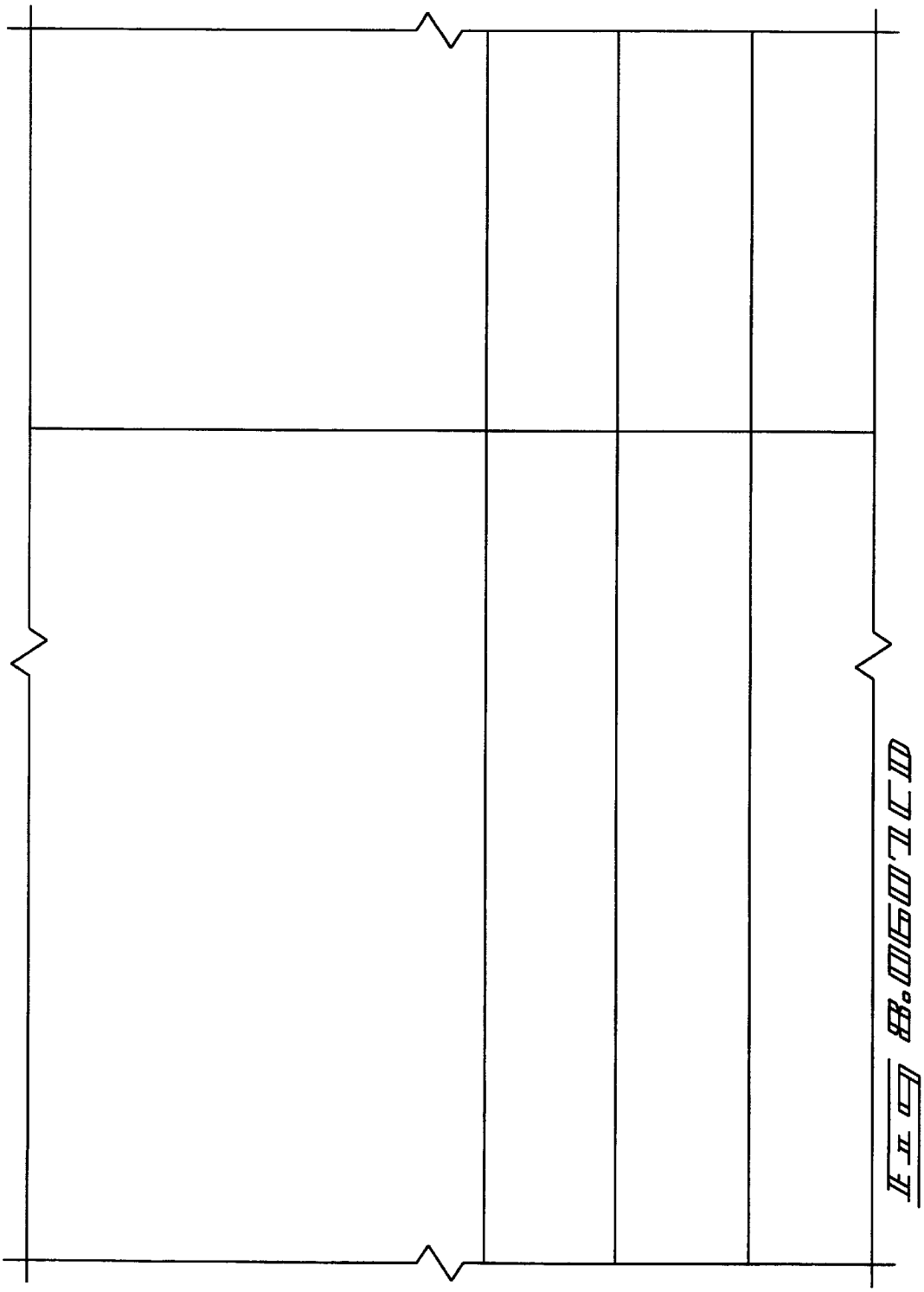


FIG 8,090,000

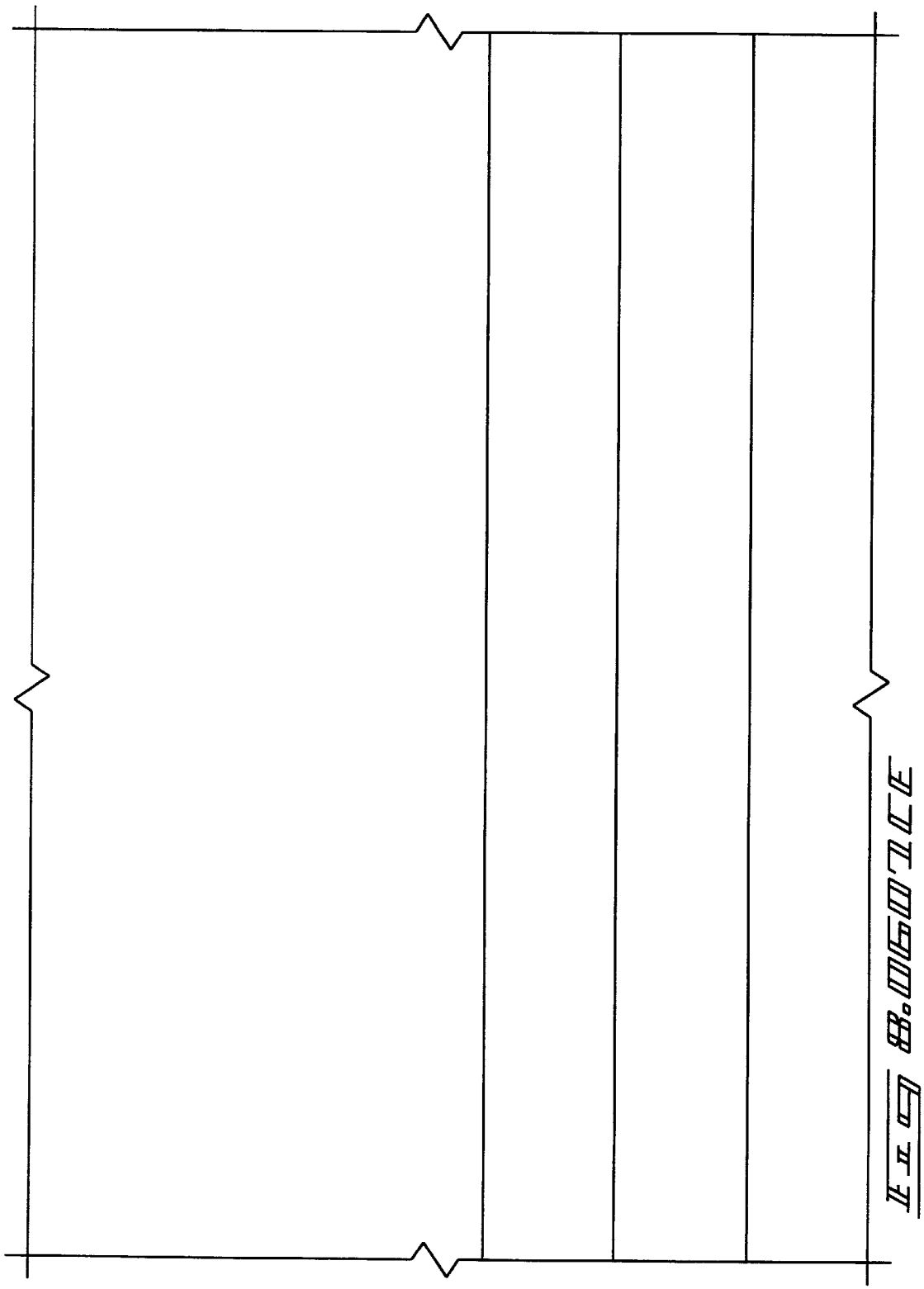


FIG 88.0600E

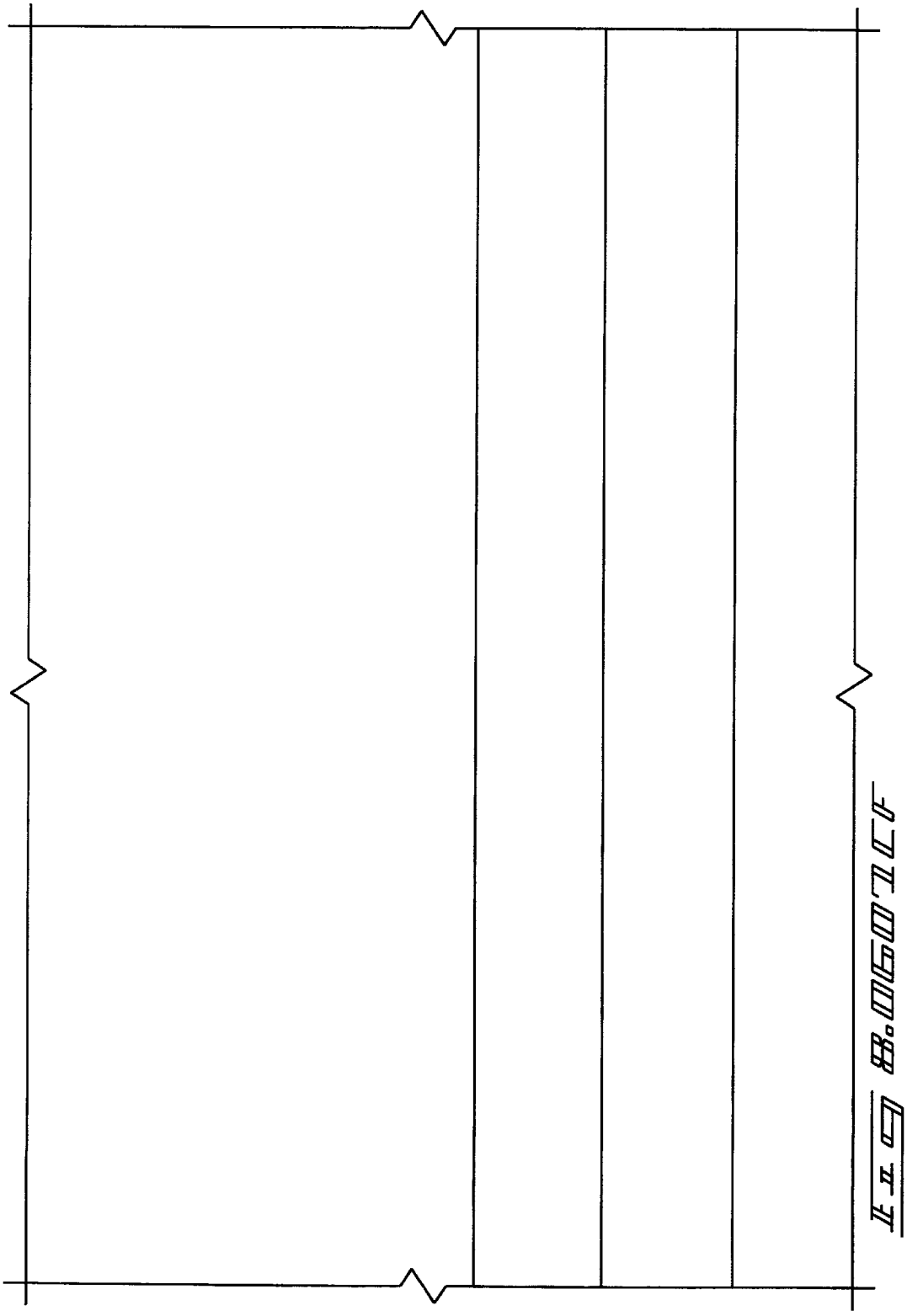


FIG 88.0600.F

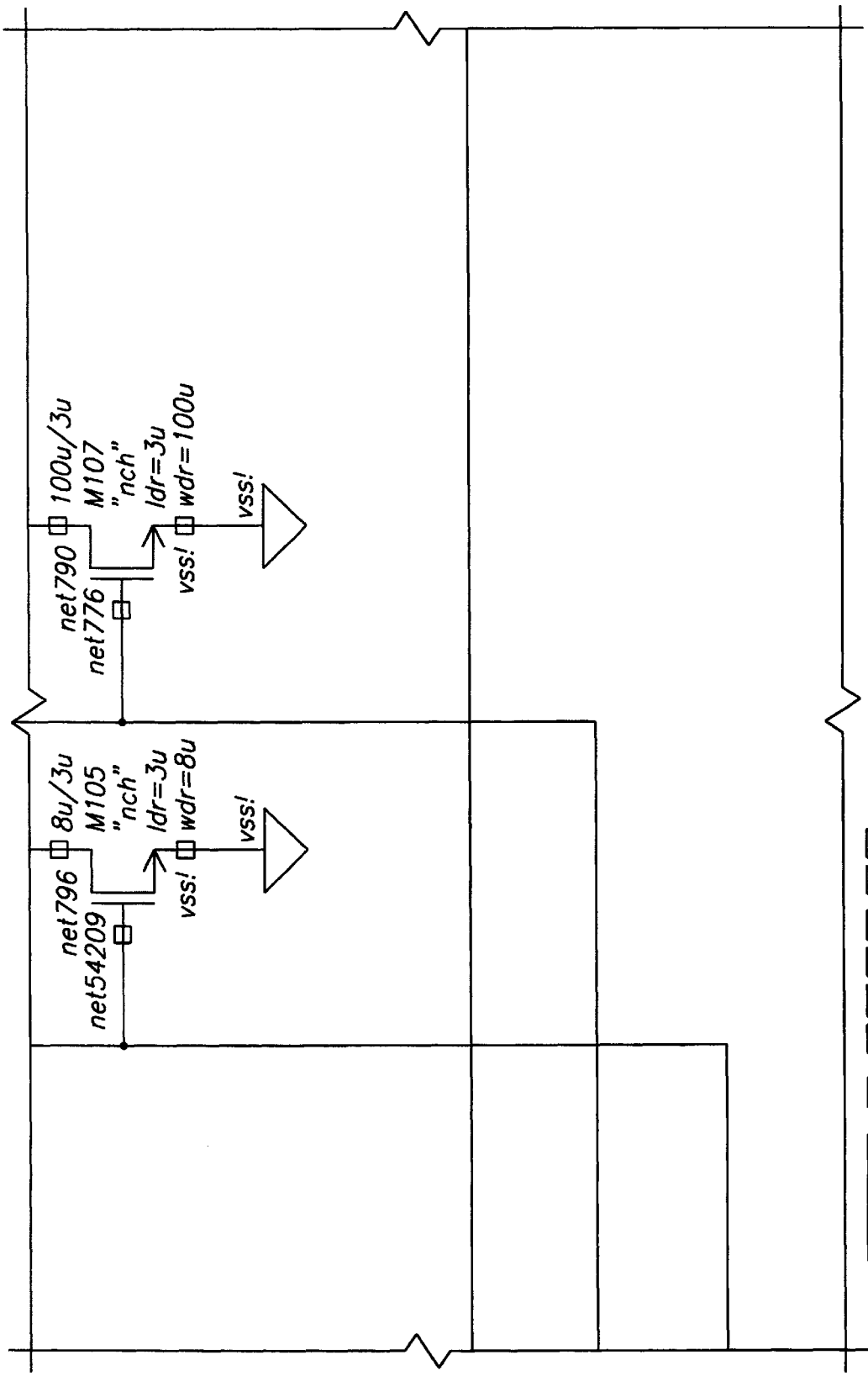

100u/3u
M107
"nch"
ldr=3u
wdr=100u
vss!
net790
net776
vss!
8u/3u
M105
"nch"
ldr=3u
wdr=8u
vss!
net796
net54209
vss!

FIG 8,050,715

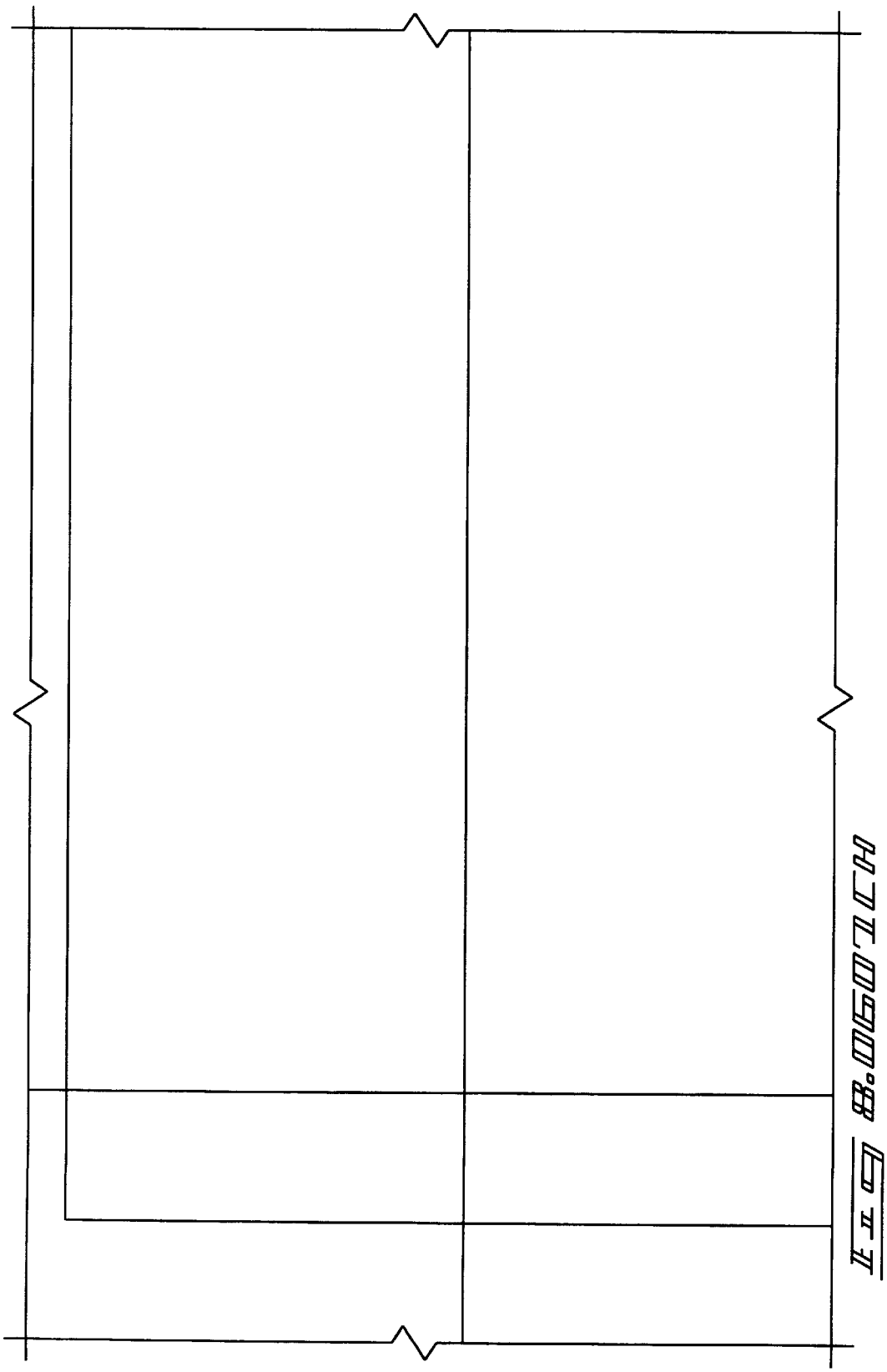


FIG. 8,060,H

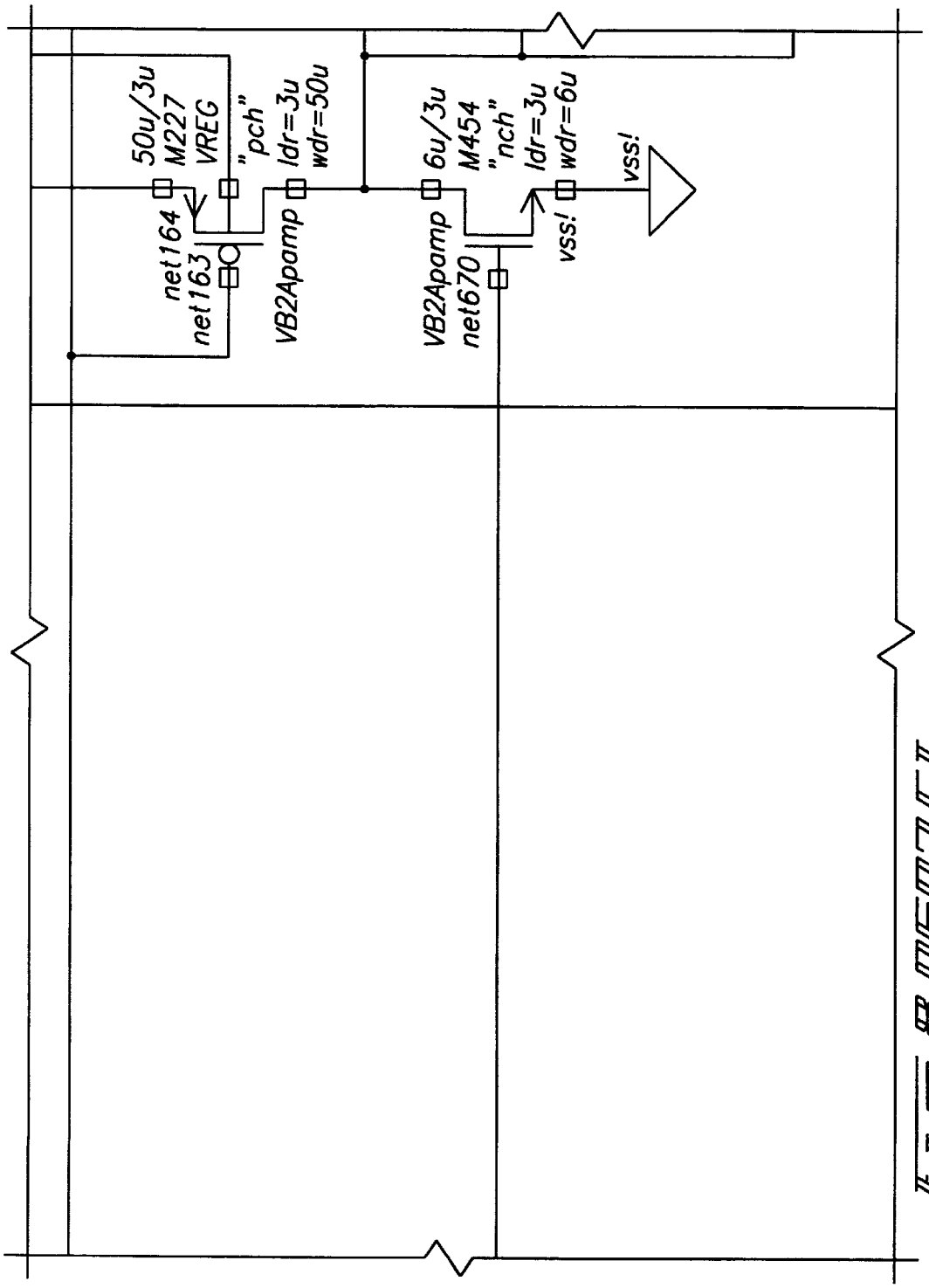
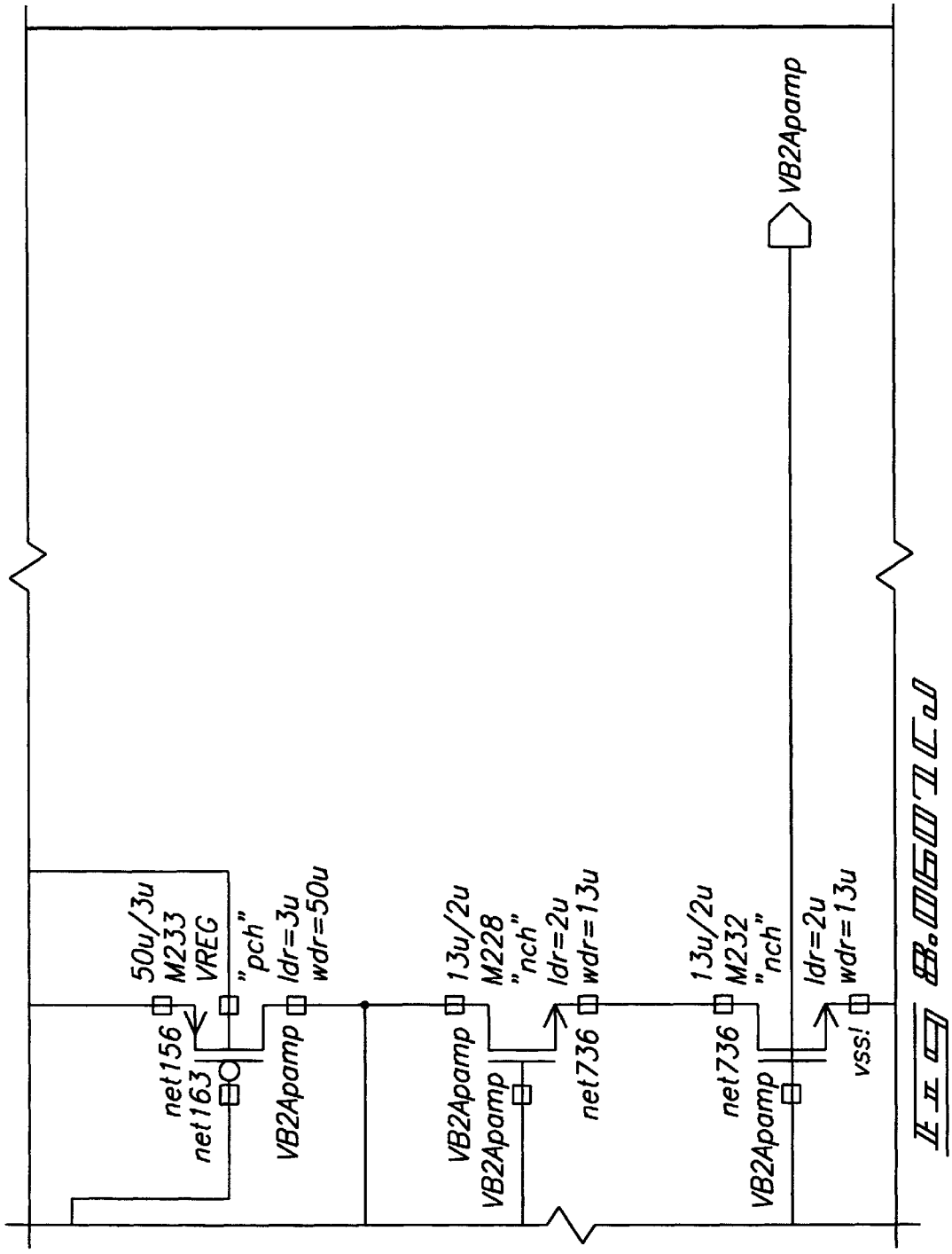

50u/3u
M227
VREG
"pch"
ldr=3u
wdr=50u
6u/3u
M454
"nch"
ldr=3u
wdr=6u
vss!
net164
net163
VB2Apamp
VB2Apamp
net670
vss!

FIG. 88,059


VB2Apamp
50u/3u
M233
VREG
"pch"
ldr=3u
wdr=50u
net156
net163
VB2Apamp
13u/2u
M228
"nch"
ldr=2u
wdr=13u
VB2Apamp
VB2Apamp
net736
13u/2u
M232
"nch"
ldr=2u
wdr=13u
net736
VB2Apamp
vss!

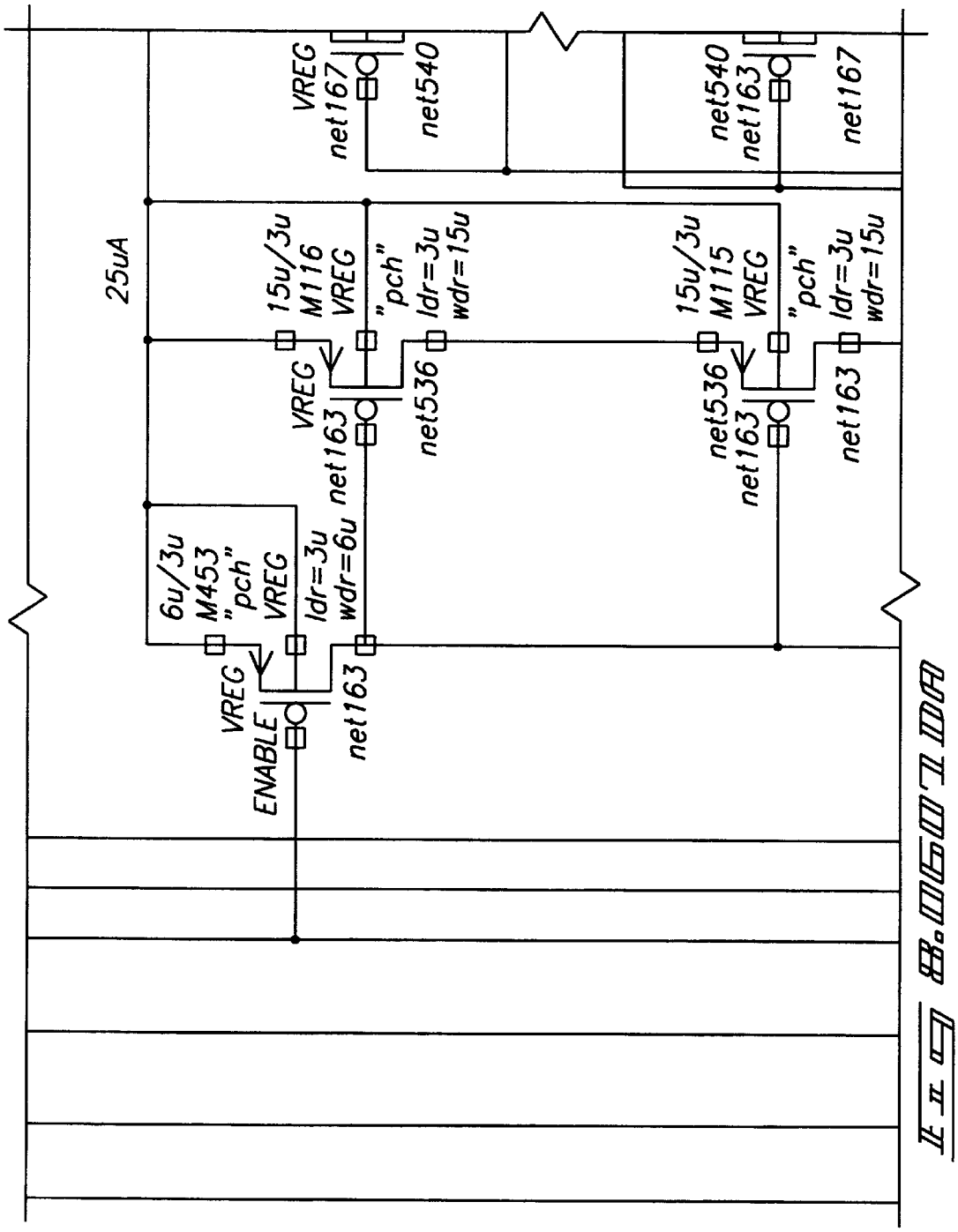
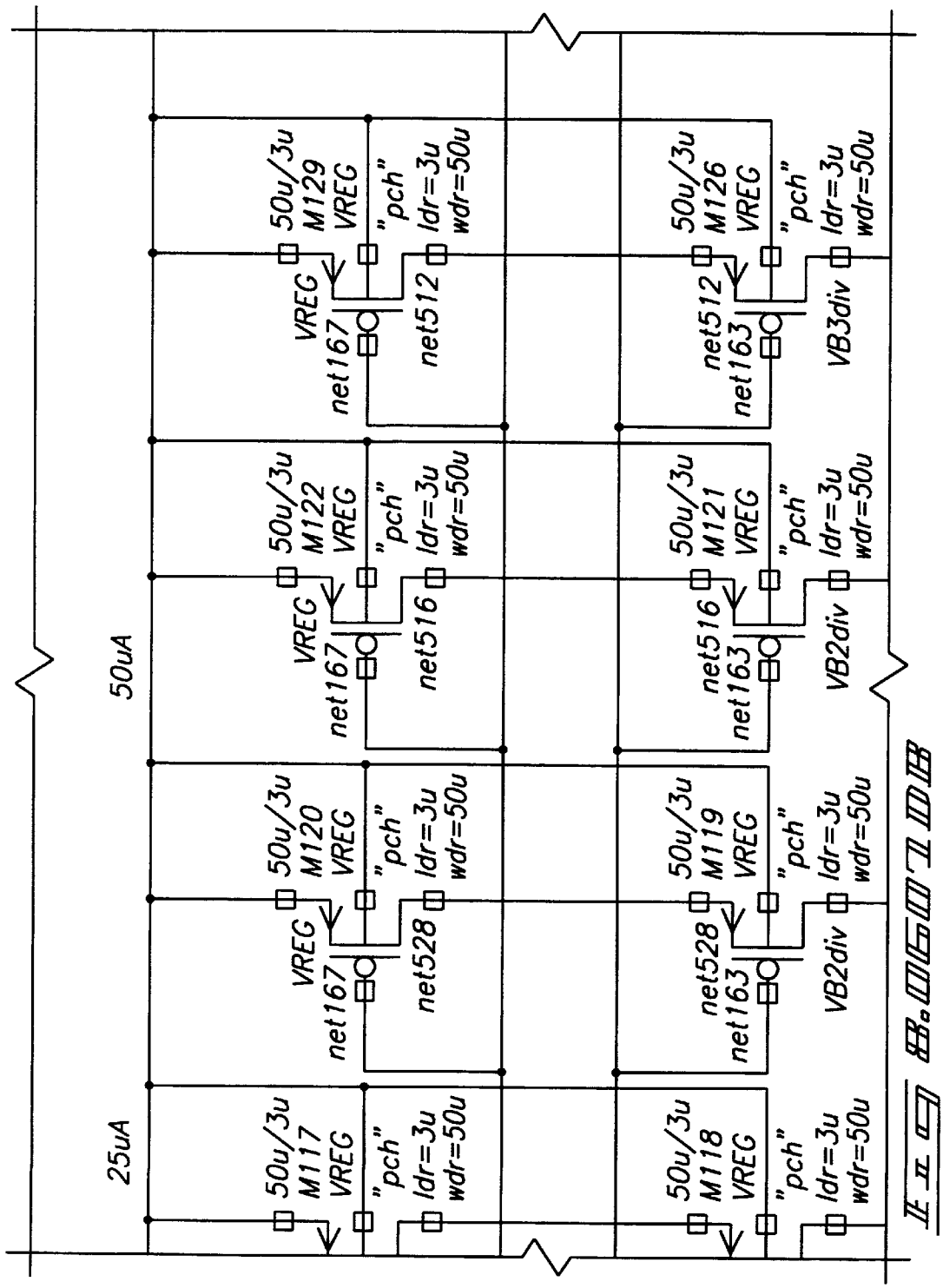
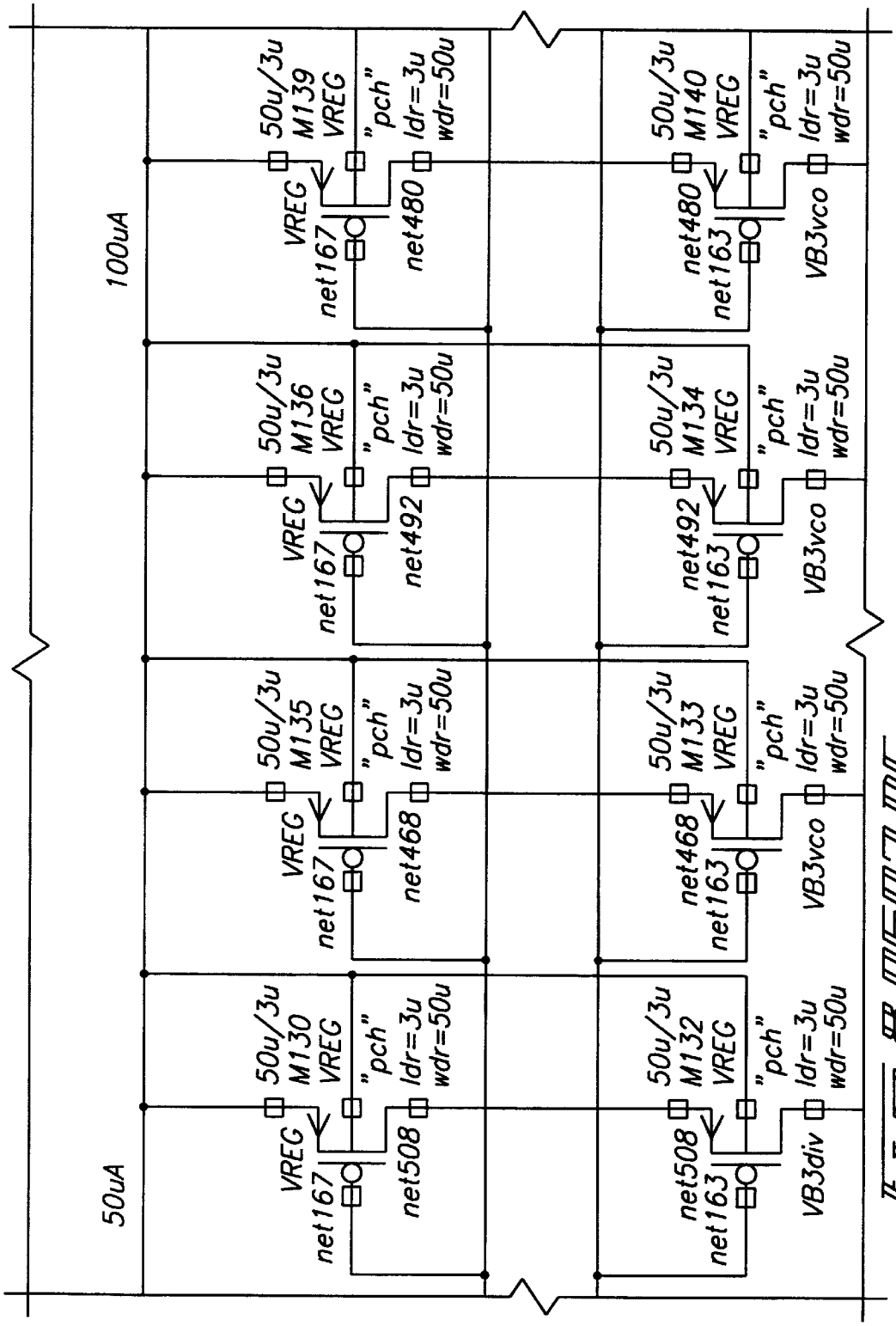
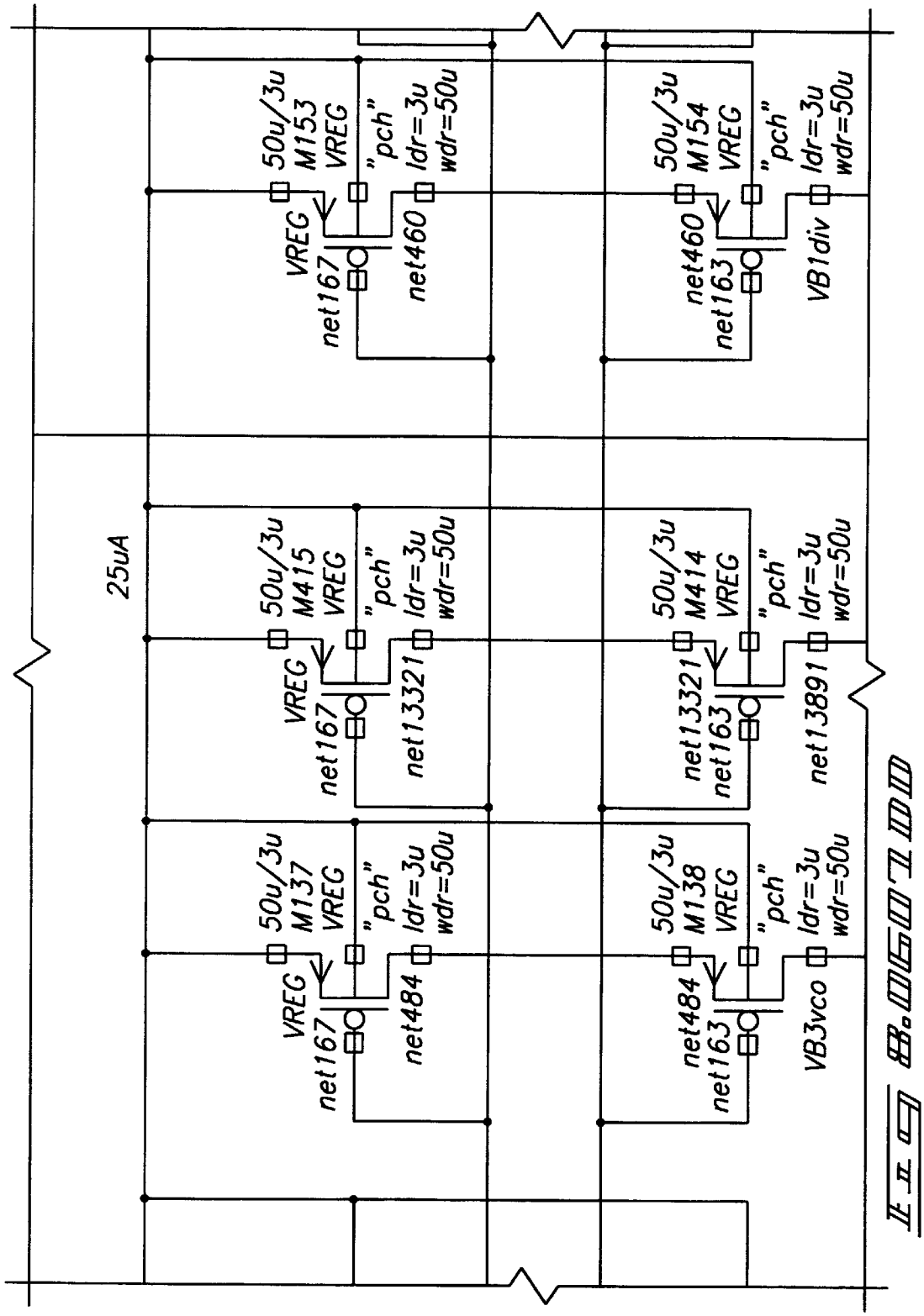

25uA
VREG
net167
net540
net540
net163
net167
15u/3u
M116
VREG
"pch"
ldr=3u
wdr=15u
15u/3u
M115
VREG
"pch"
ldr=3u
wdr=15u
VREG
net163
net536
net536
net163
net163
6u/3u
M453
"pch"
VREG
ldr=3u
wdr=6u
VREG
ENABLE
net163

FIG. 8.0601DA


50uA
25uA
50u/3u M129 VREG "pch" ldr=3u wdr=50u
VREG net167 net512
50u/3u M126 VREG "pch" ldr=3u wdr=50u
net512 net163 VB3div
50u/3u M122 VREG "pch" ldr=3u wdr=50u
VREG net167 net516
50u/3u M121 VREG "pch" ldr=3u wdr=50u
net516 net163 VB2div
50u/3u M120 VREG "pch" ldr=3u wdr=50u
VREG net167 net528
50u/3u M119 VREG "pch" ldr=3u wdr=50u
net528 net163 VB2div
50u/3u M117 VREG "pch" ldr=3u wdr=50u
50u/3u M118 VREG "pch" ldr=3u wdr=50u


100uA
50uA
50u/3u M139 VREG "pch" ldr=3u wdr=50u
VREG net167 net480
50u/3u M140 VREG "pch" ldr=3u wdr=50u
net480 net163 VB3vco
50u/3u M136 VREG "pch" ldr=3u wdr=50u
VREG net167 net492
50u/3u M134 VREG "pch" ldr=3u wdr=50u
net492 net163 VB3vco
50u/3u M135 VREG "pch" ldr=3u wdr=50u
VREG net167 net468
50u/3u M133 VREG "pch" ldr=3u wdr=50u
net468 net163 VB3vco
50u/3u M130 VREG "pch" ldr=3u wdr=50u
VREG net167 net508
50u/3u M132 VREG "pch" ldr=3u wdr=50u
net508 net163 VB3div


25uA
50u/3u M153 VREG "pch" ldr=3u wdr=50u
VREG net167 net460
50u/3u M154 VREG "pch" ldr=3u wdr=50u
net460 net163 VB1div
50u/3u M415 VREG "pch" ldr=3u wdr=50u
VREG net167 net13321
50u/3u M414 VREG "pch" ldr=3u wdr=50u
net13321 net163 net13891
50u/3u M137 VREG "pch" ldr=3u wdr=50u
VREG net167 net484
50u/3u M138 VREG "pch" ldr=3u wdr=50u
net484 net163 VB3vco

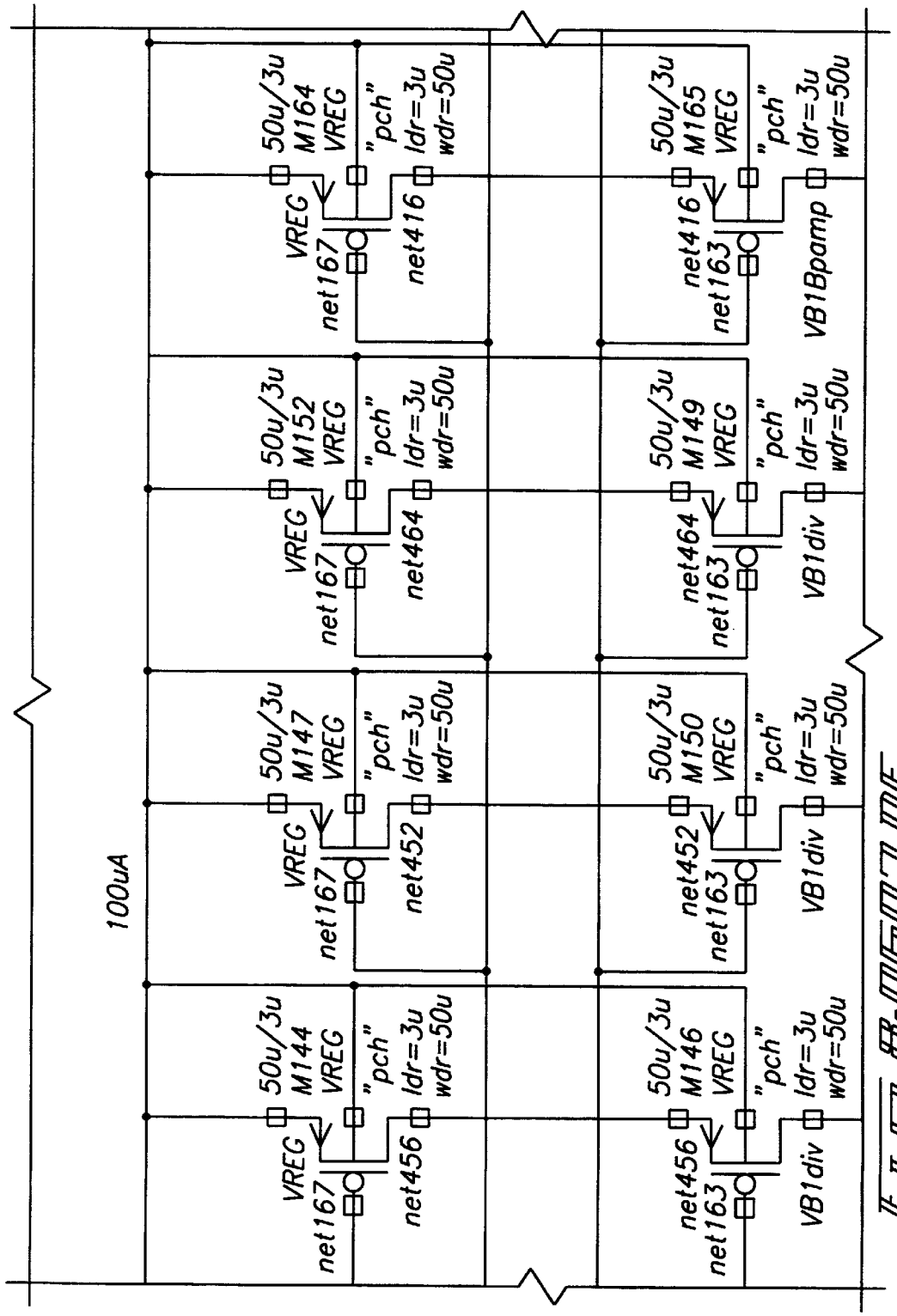


FIG. 88. CONTINUE

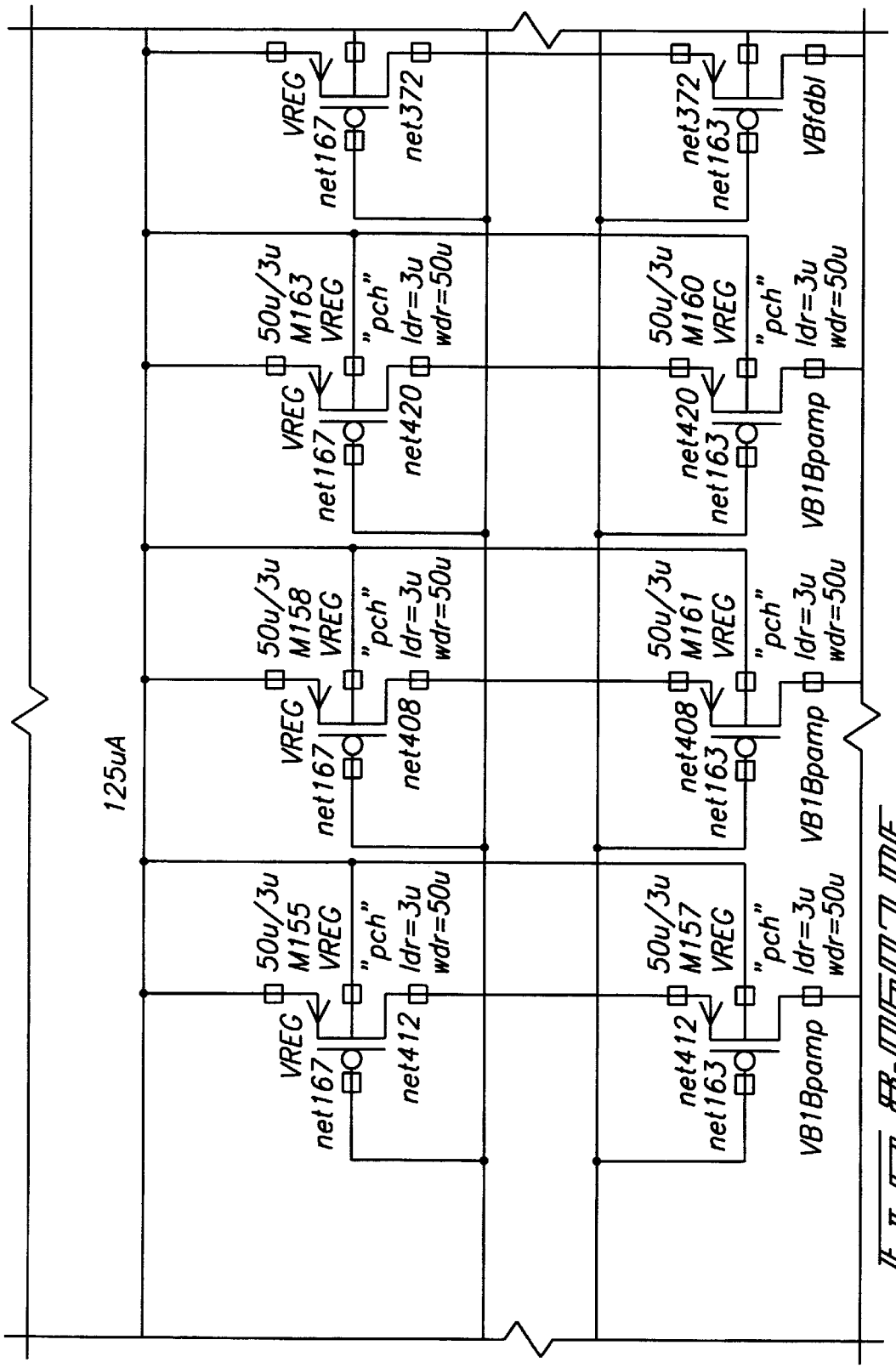


FIG. 88.0056 IDF

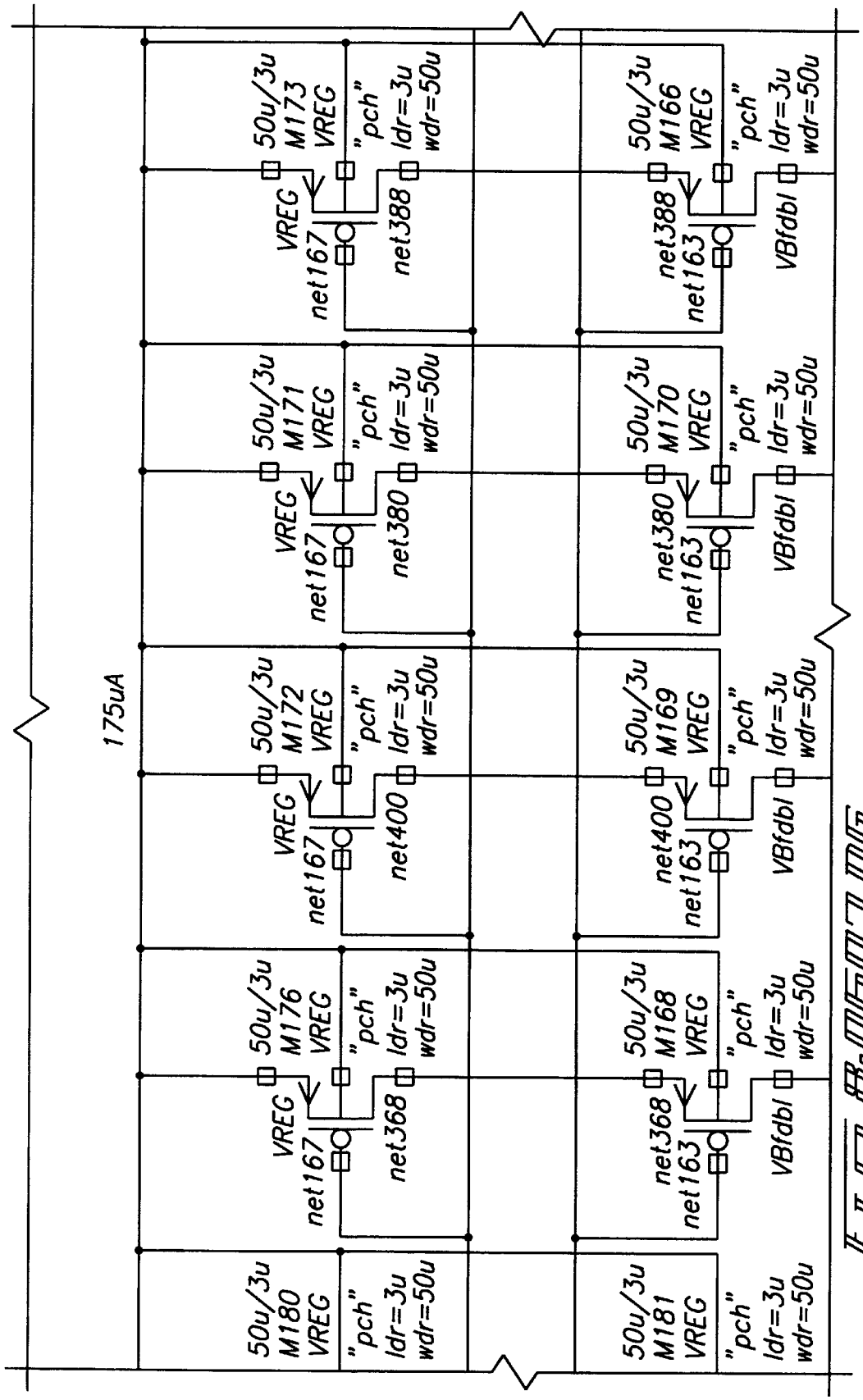


FIG. 88.00011.DGS

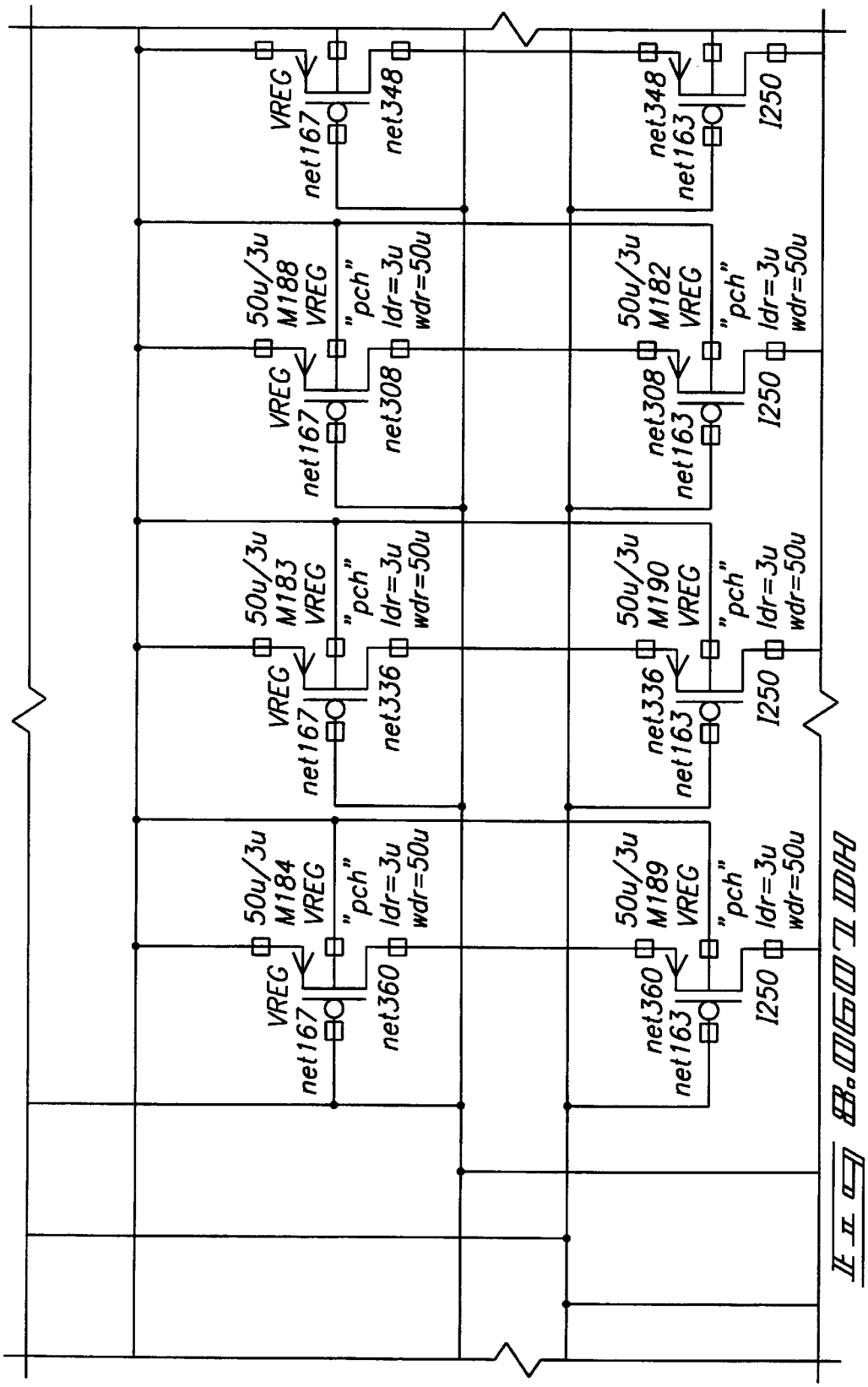


FIG 8.0600 IDH

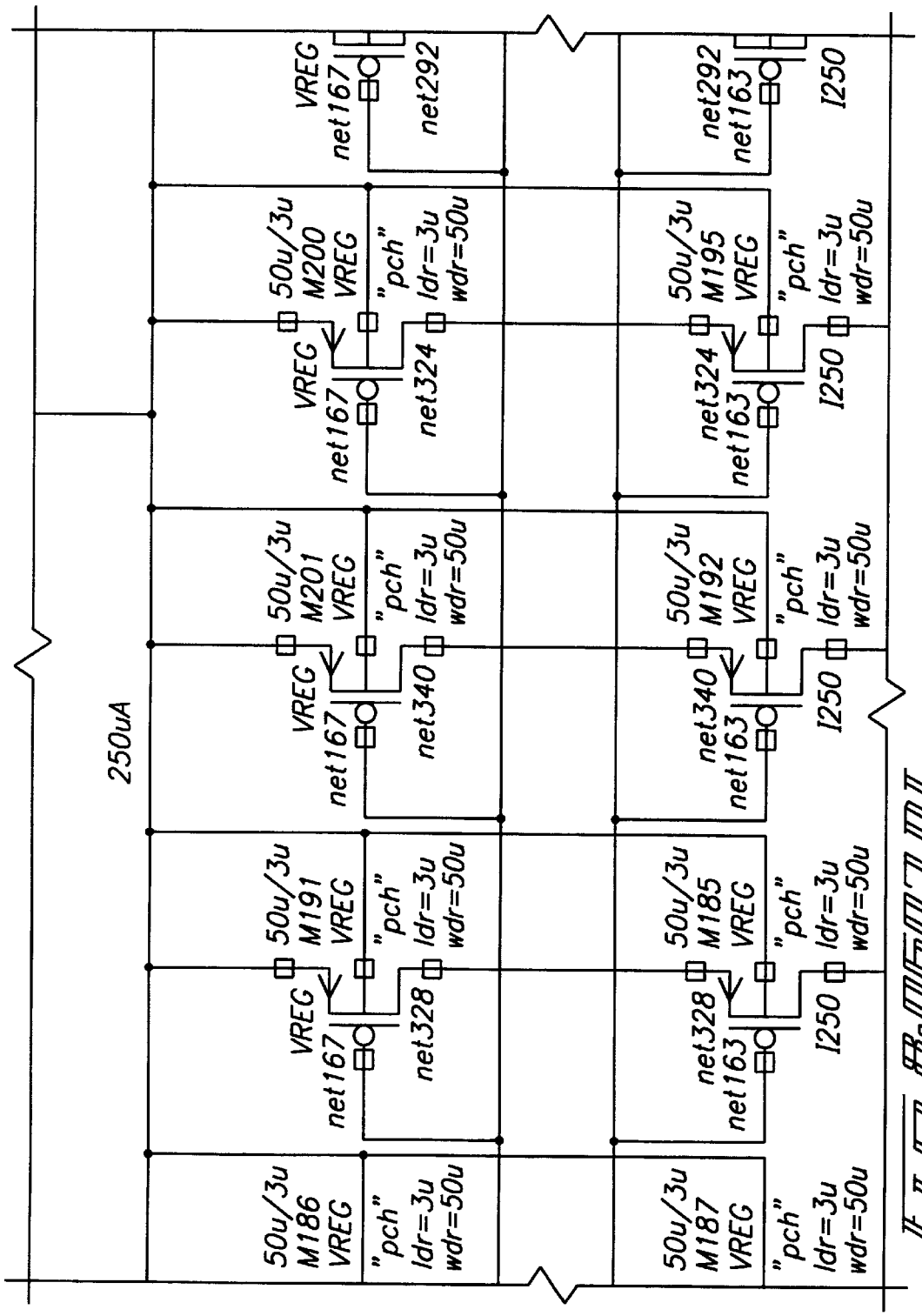


FIG. 88.0050 II

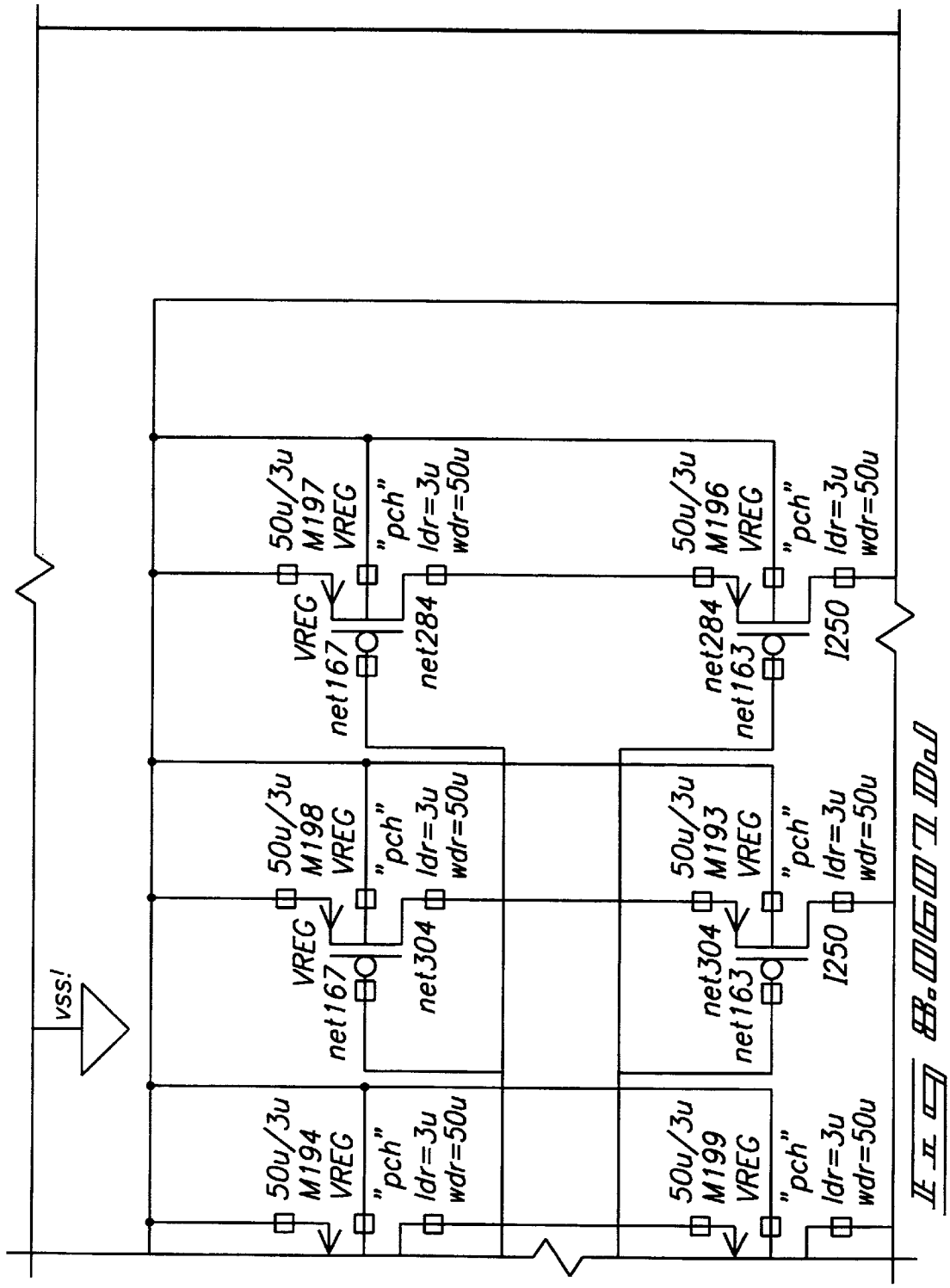


FIG. 88.00611.00

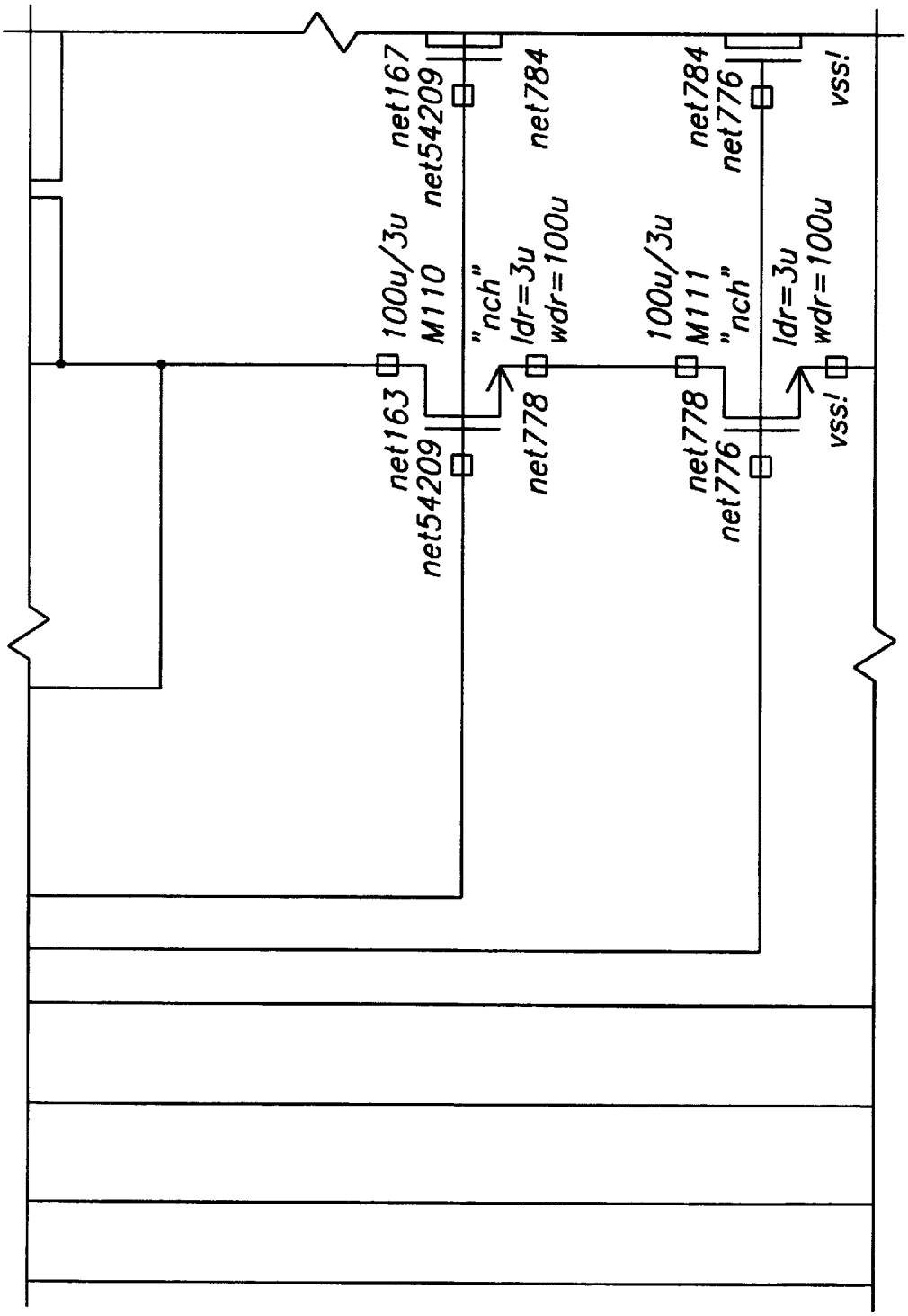
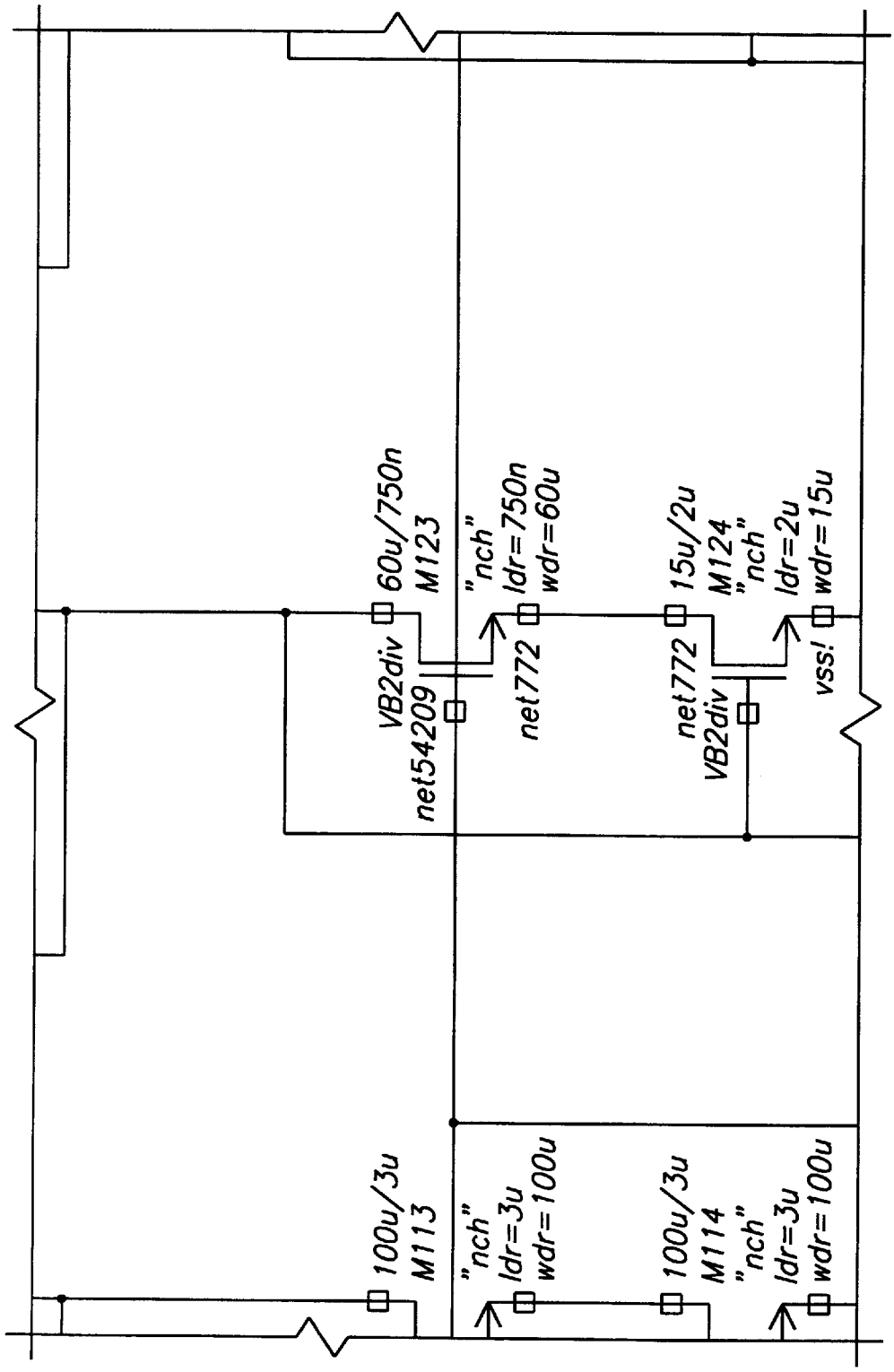


FIG 88.0050EA


60u/750n
M123
"nch"
ldr=750n
wdr=60u
15u/2u
M124
"nch"
ldr=2u
wdr=15u
VB2div
net54209
net772
net772
VB2div
vss!
100u/3u
M113
"nch"
ldr=3u
wdr=100u
100u/3u
M114
"nch"
ldr=3u
wdr=100u

Фиг. 2131

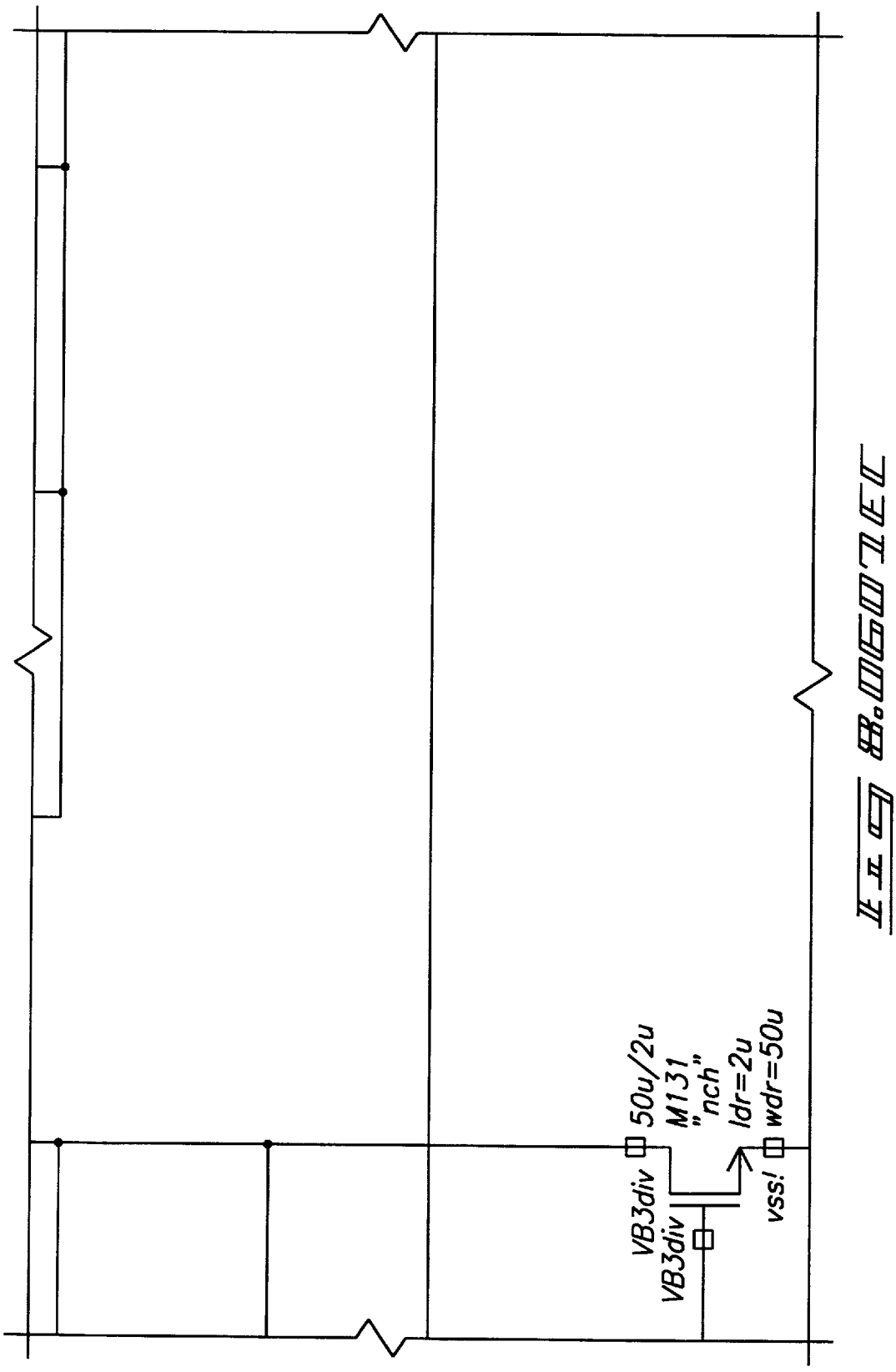


FIG 88.0600

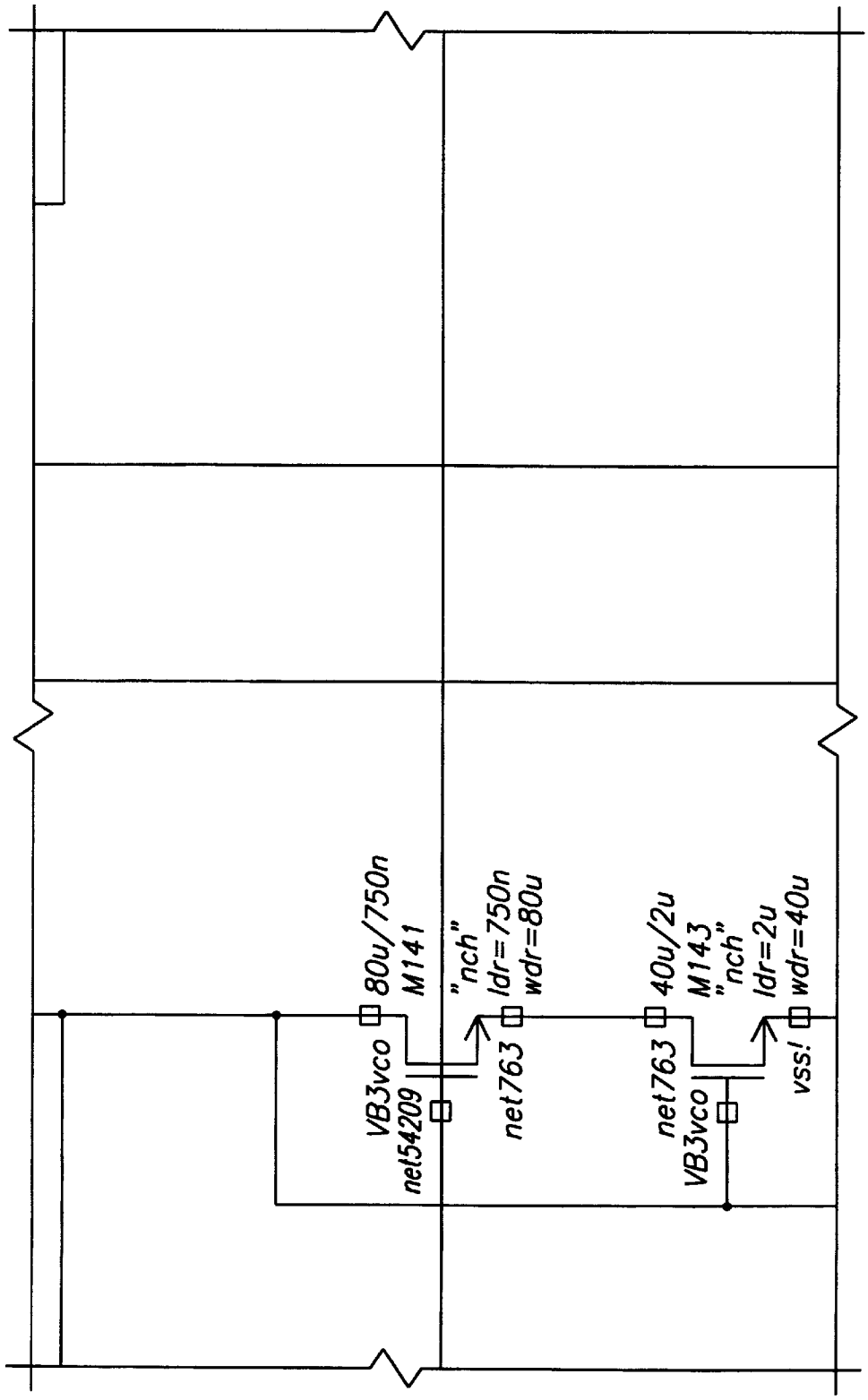


FIG 88.0650ED

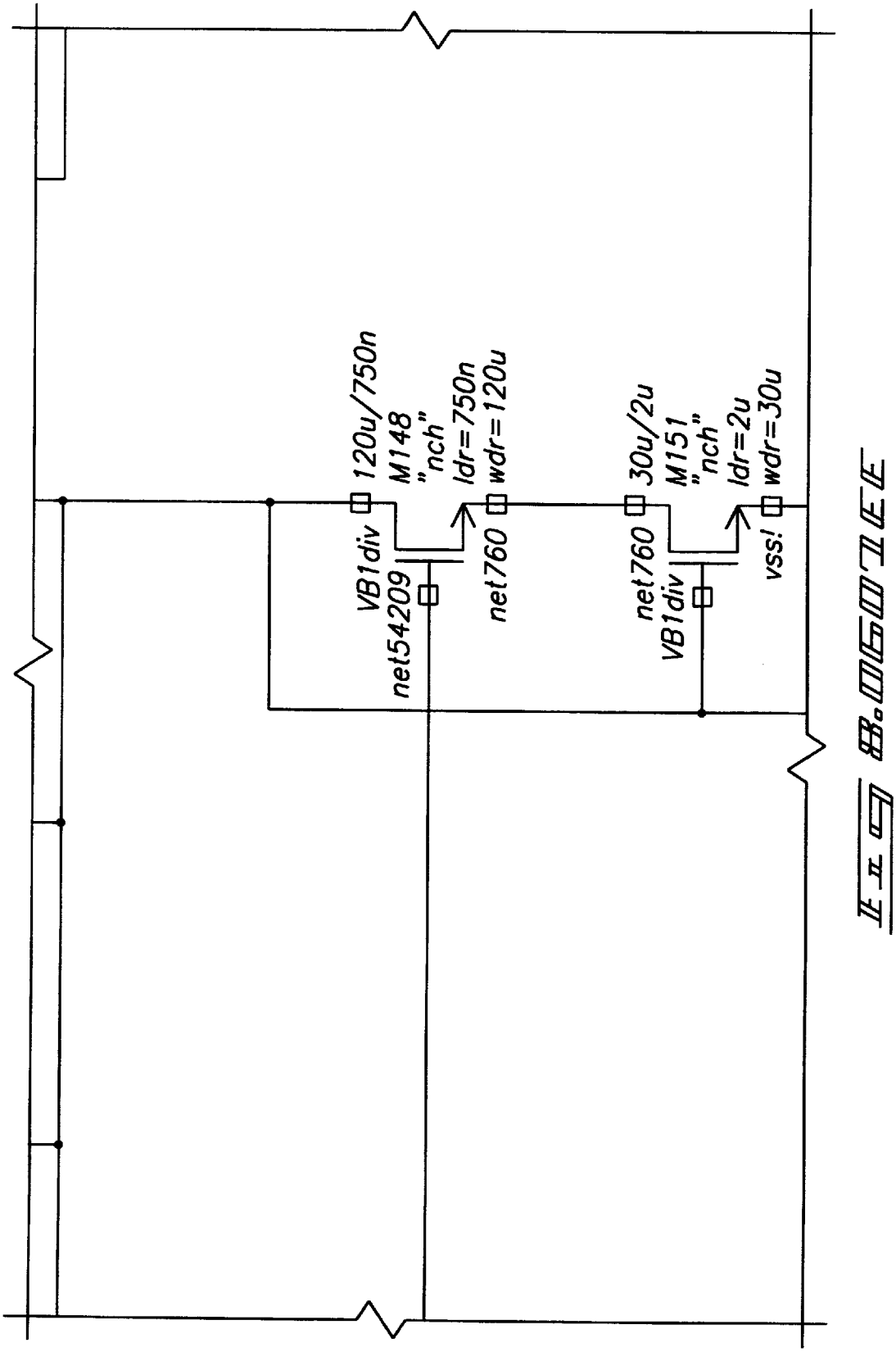


FIG. 88.0050 TIE

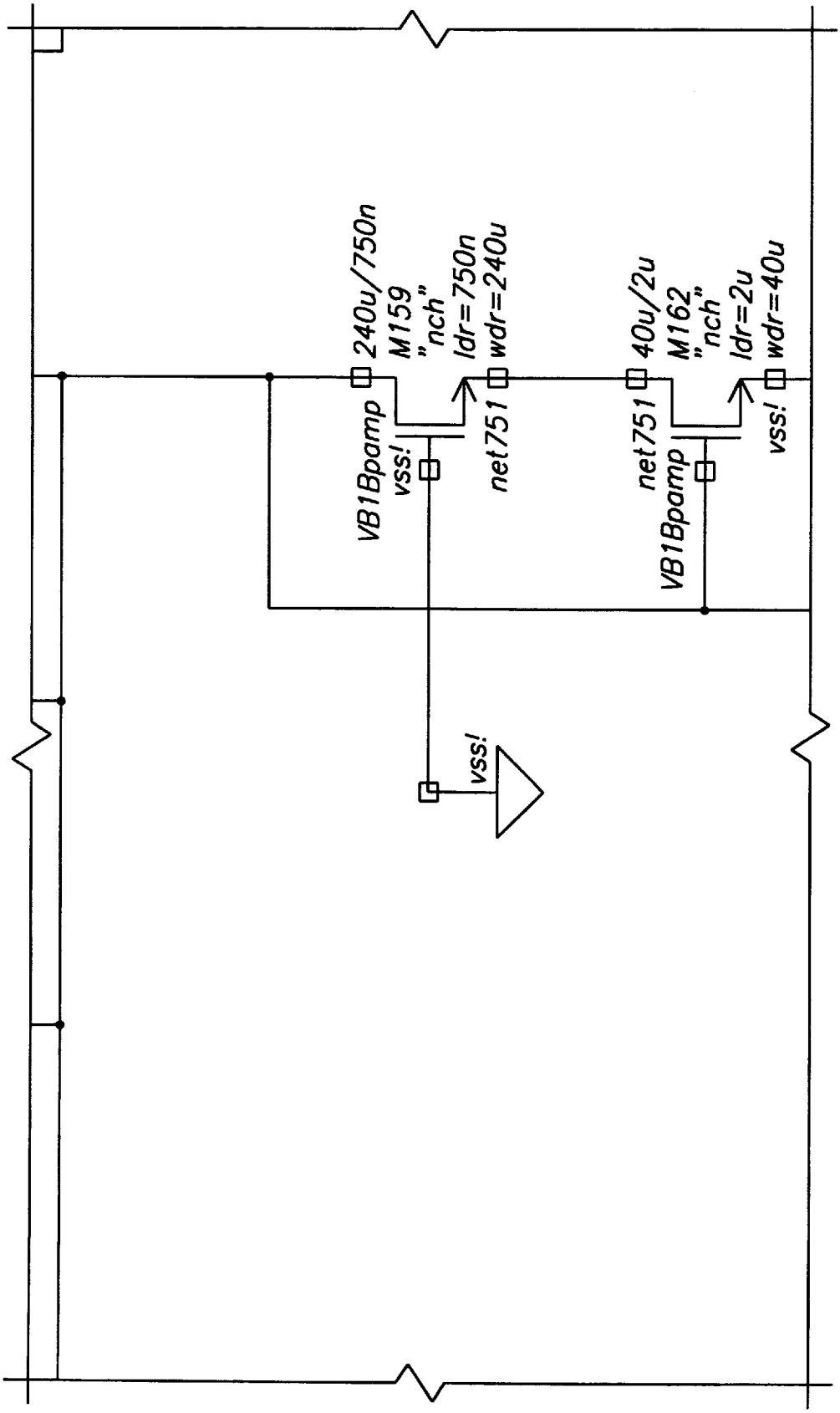


FIG 88.00600LEF

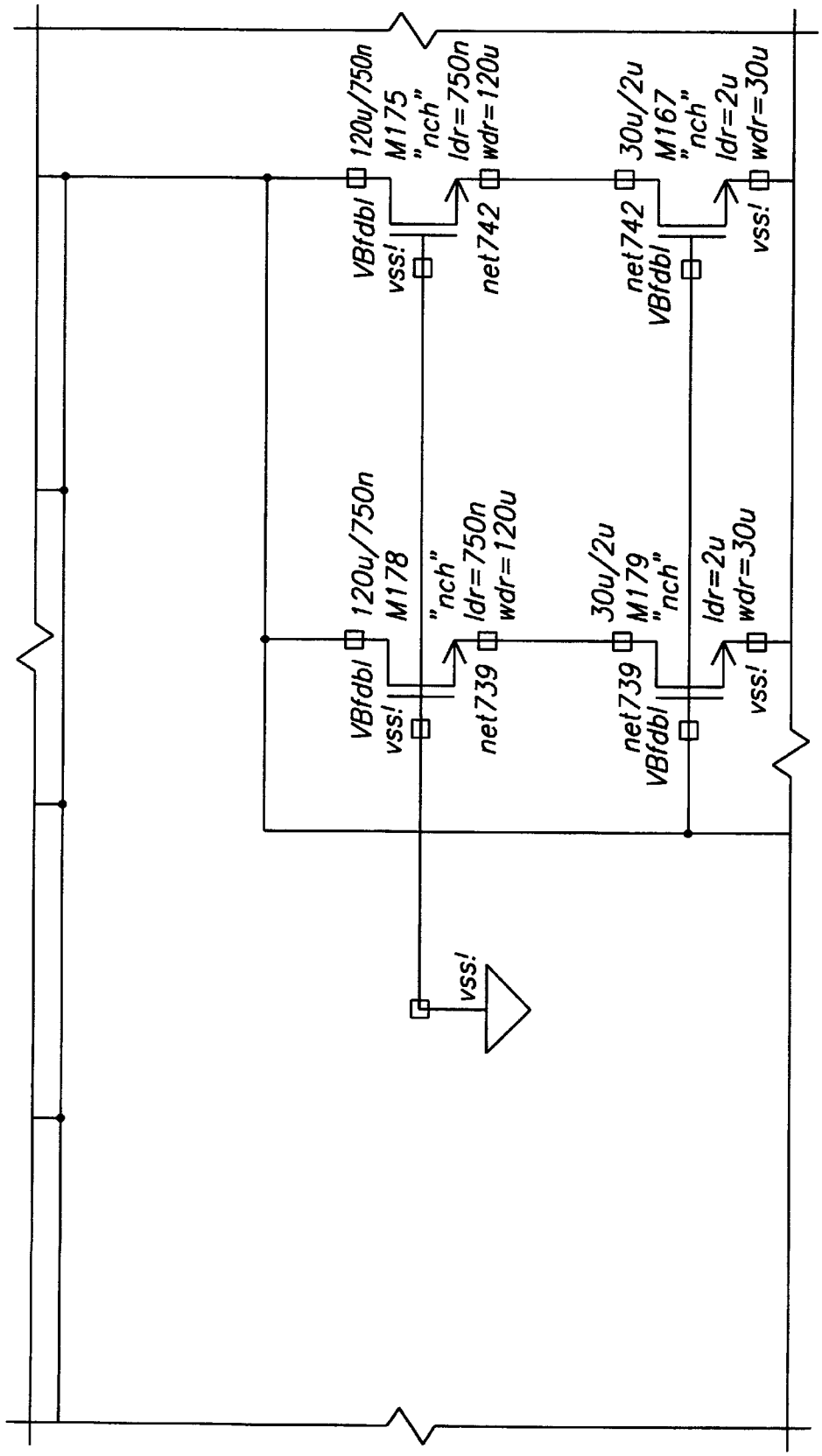

120u/750n
M175
"nch"
ldr=750n
wdr=120u
VBfdbl
vss!
net742
30u/2u
M167
"nch"
ldr=2u
wdr=30u
net742
VBfdbl
vss!
120u/750n
M178
"nch"
ldr=750n
wdr=120u
VBfdbl
vss!
net739
30u/2u
M179
"nch"
ldr=2u
wdr=30u
net739
VBfdbl
vss!
vss!

FIG. 88.0050

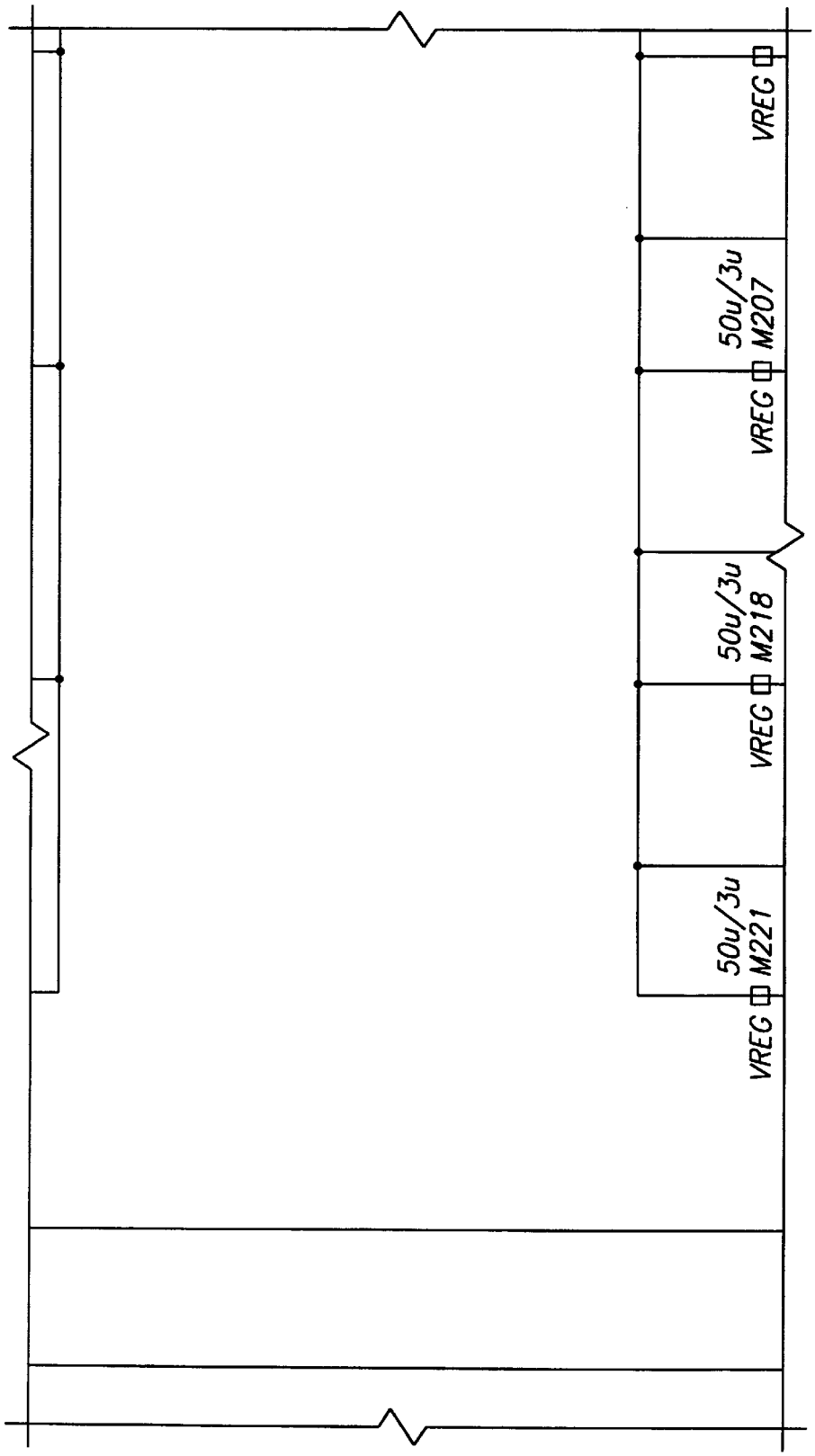


Fig. 88.0600 (PRIOR ART)

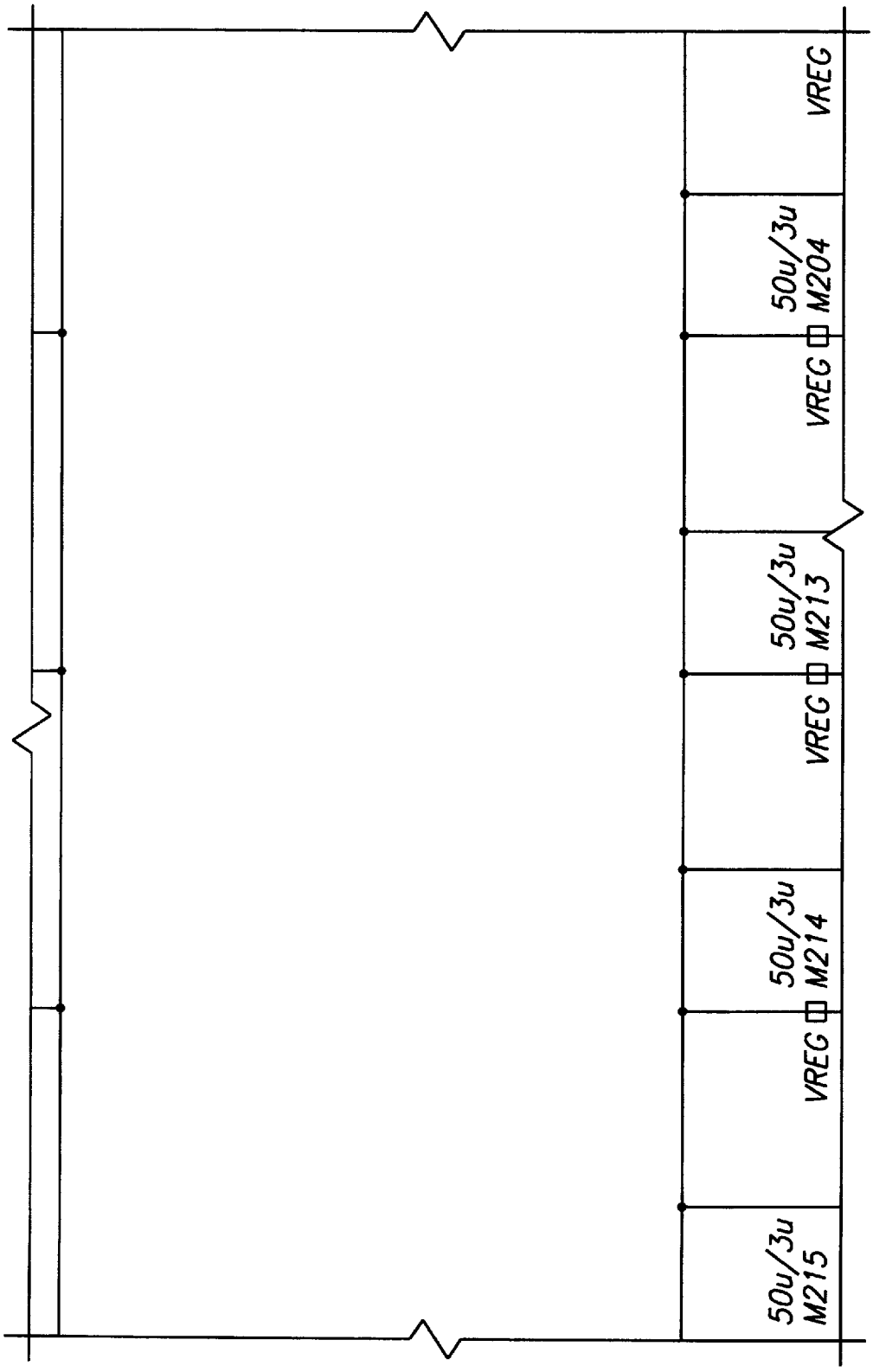


FIG. 88.0050E II

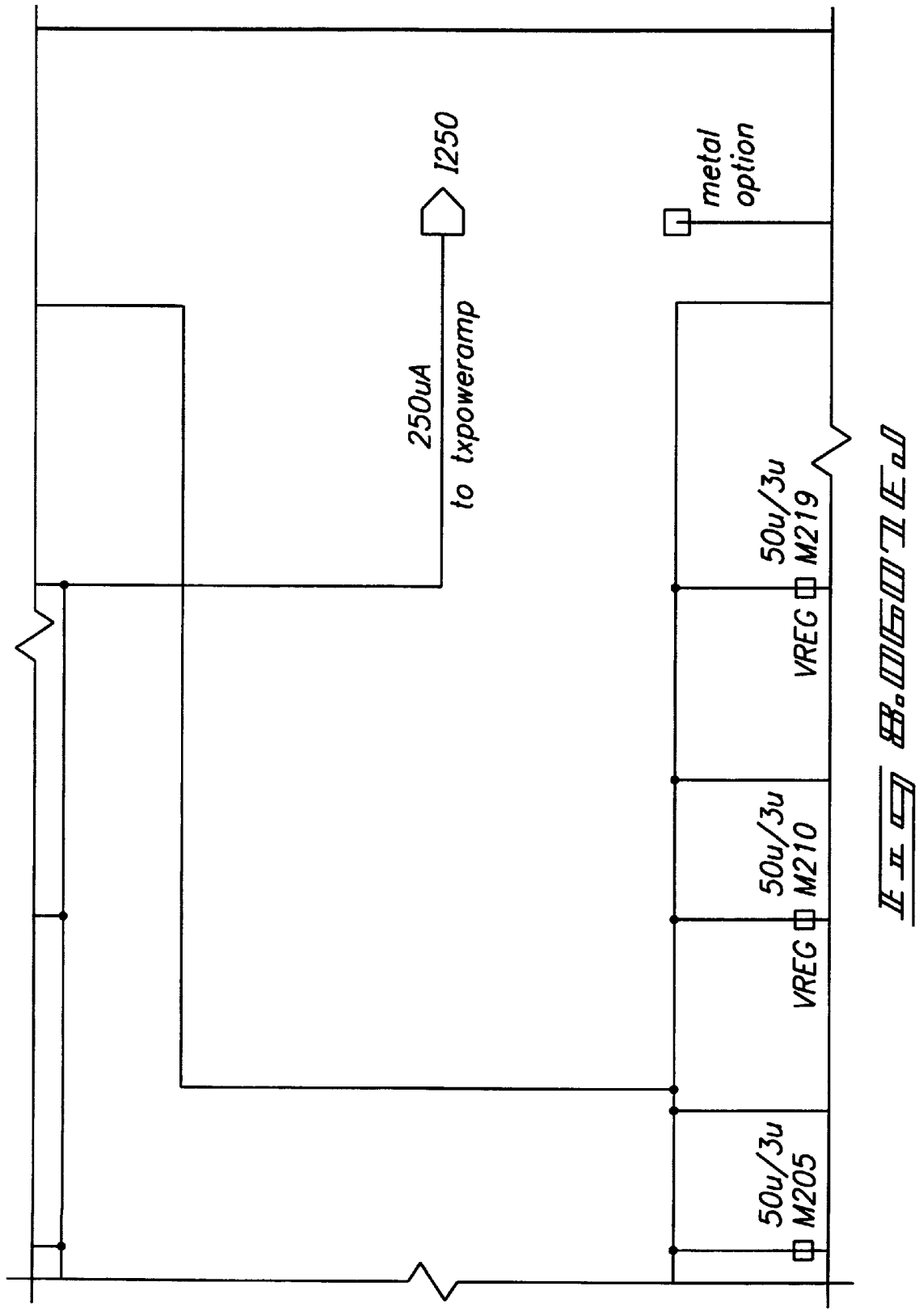

I250
250uA
to txpoweramp
metal
option
50u/3u
M219
VREG
50u/3u
M210
VREG
50u/3u
M205

FIG. 8.005LEd

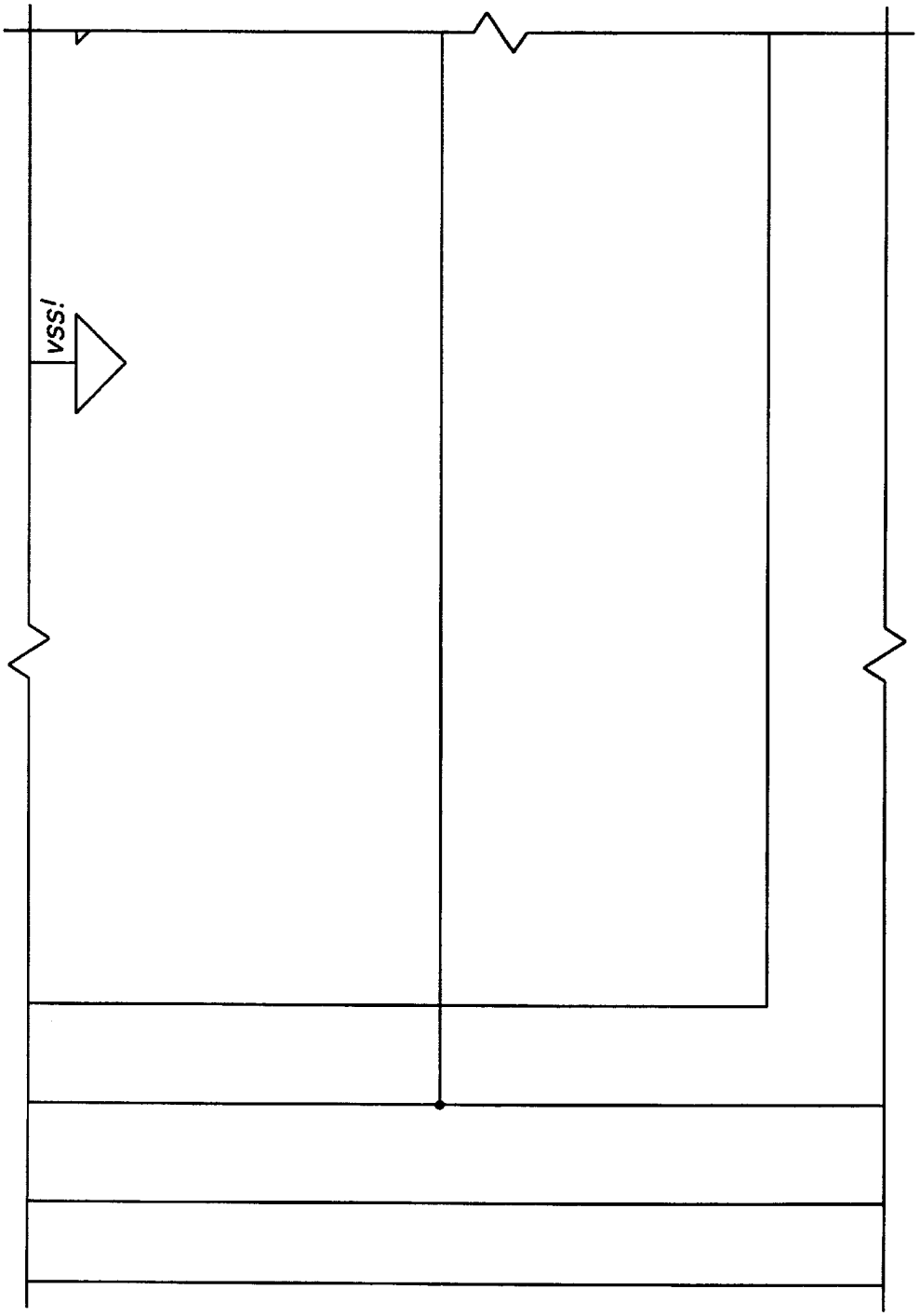


FIG. 8,050

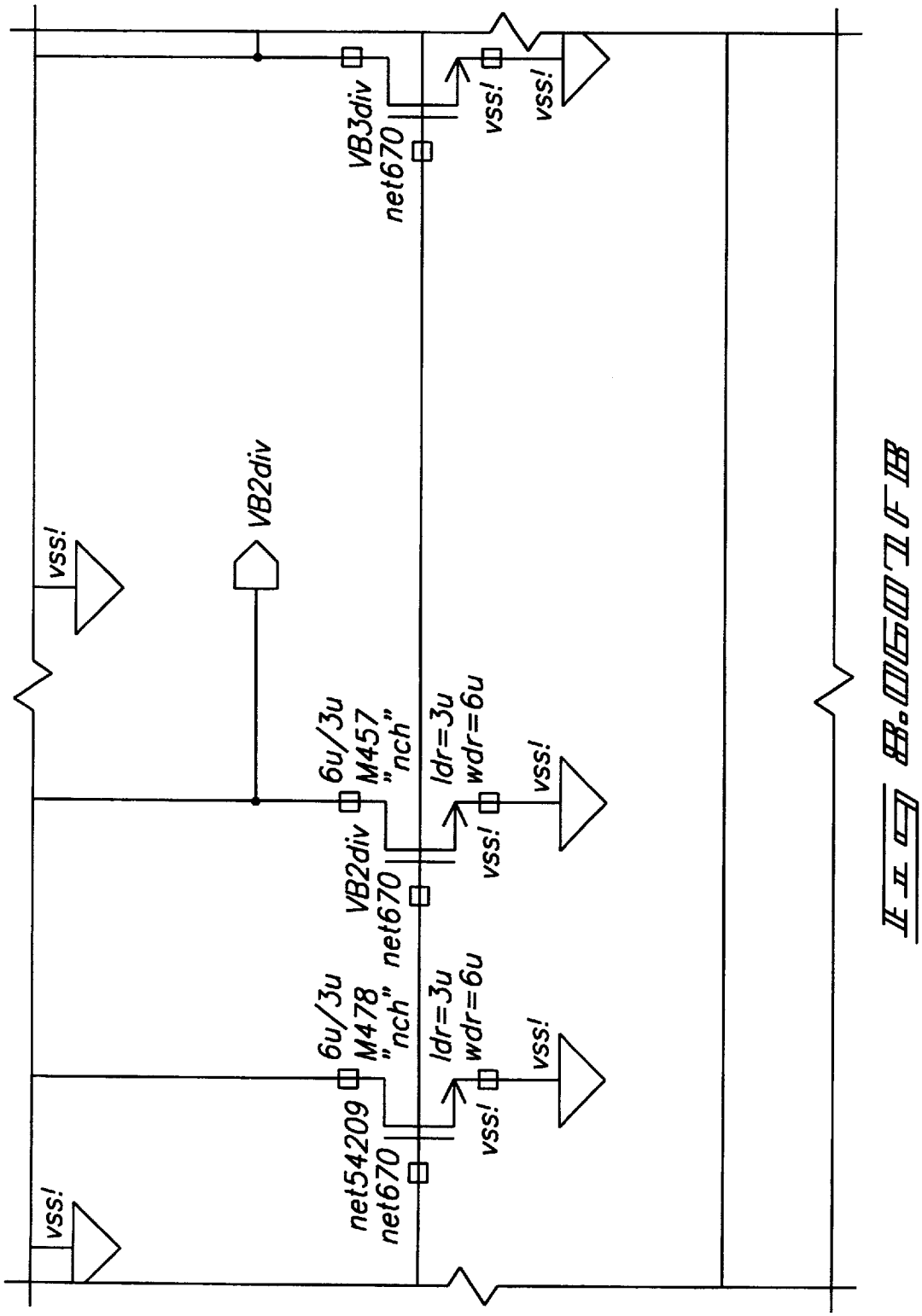

VB3div
net670
vss!
vss!
VB2div
vss!
6u/3u
M457
"nch"
ldr=3u
wdr=6u
vss!
VB2div
net670
vss!
6u/3u
M478
"nch"
ldr=3u
wdr=6u
vss!
net54209
net670
vss!
vss!

FIG. 2141

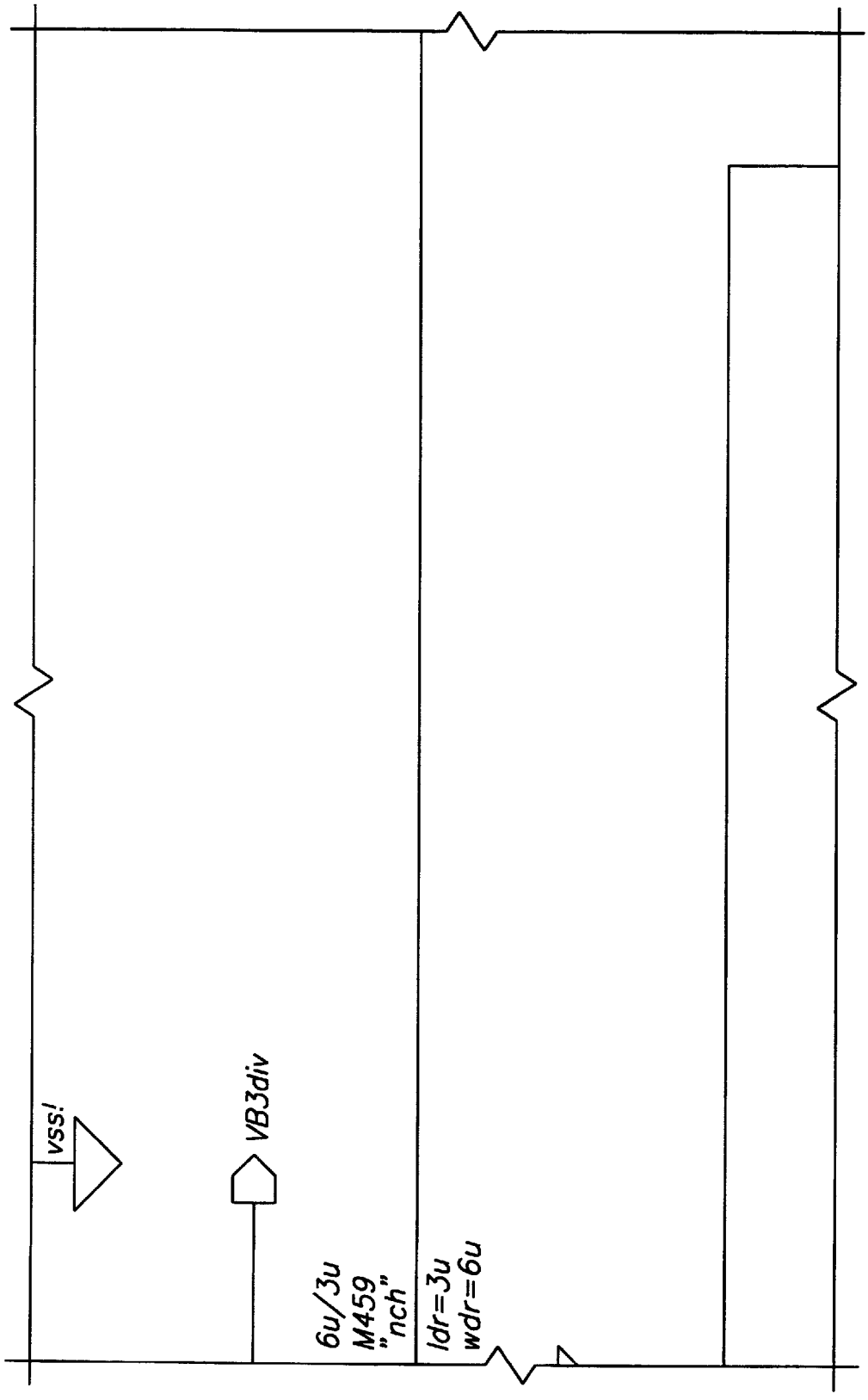


FIG 98.0560FC

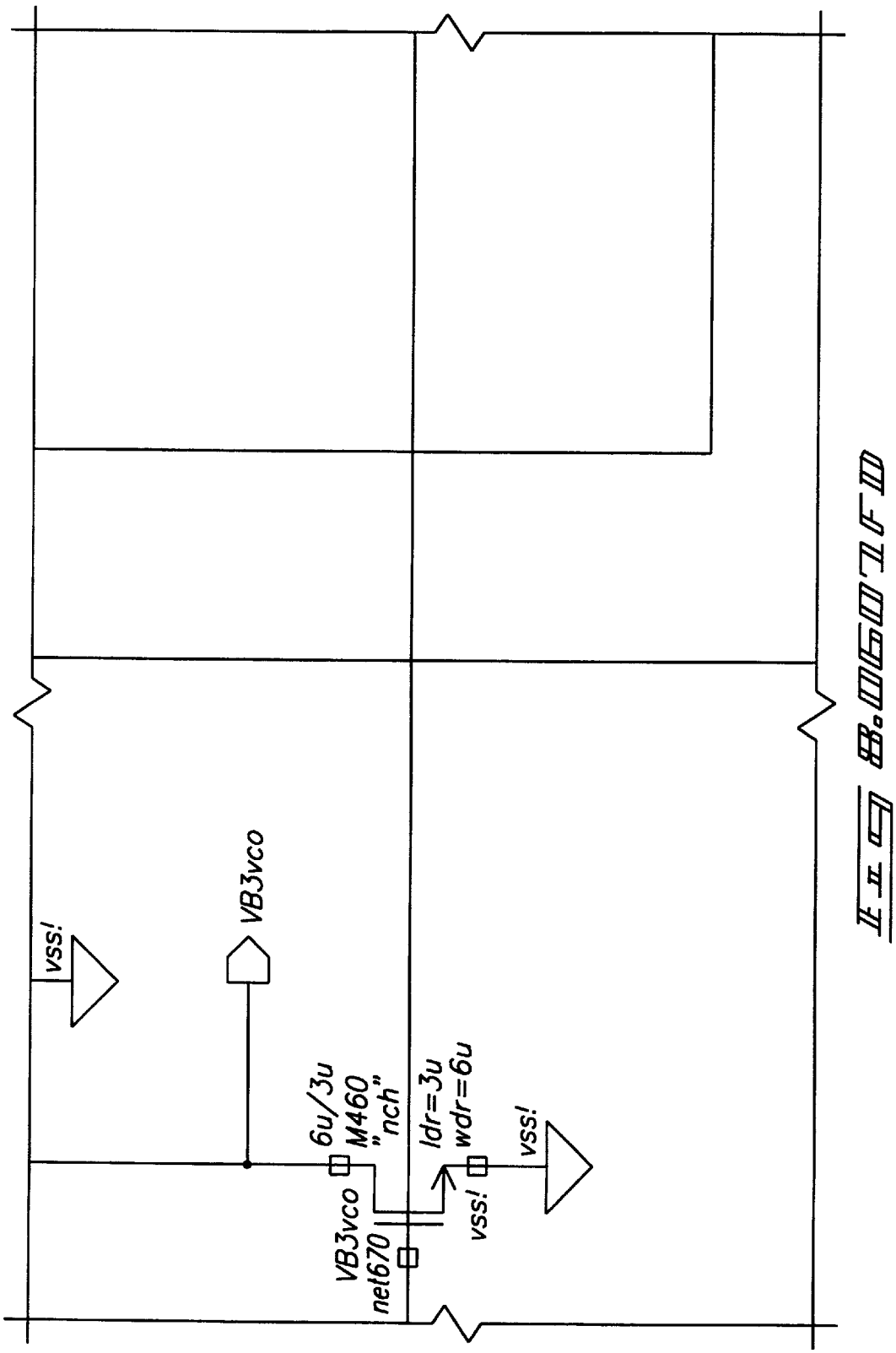


FIG. 8,050
vss!
VB3vco
6u/3u
M460
"nch"
ldr=3u
wdr=6u
vss!
VB3vco
net670
vss!

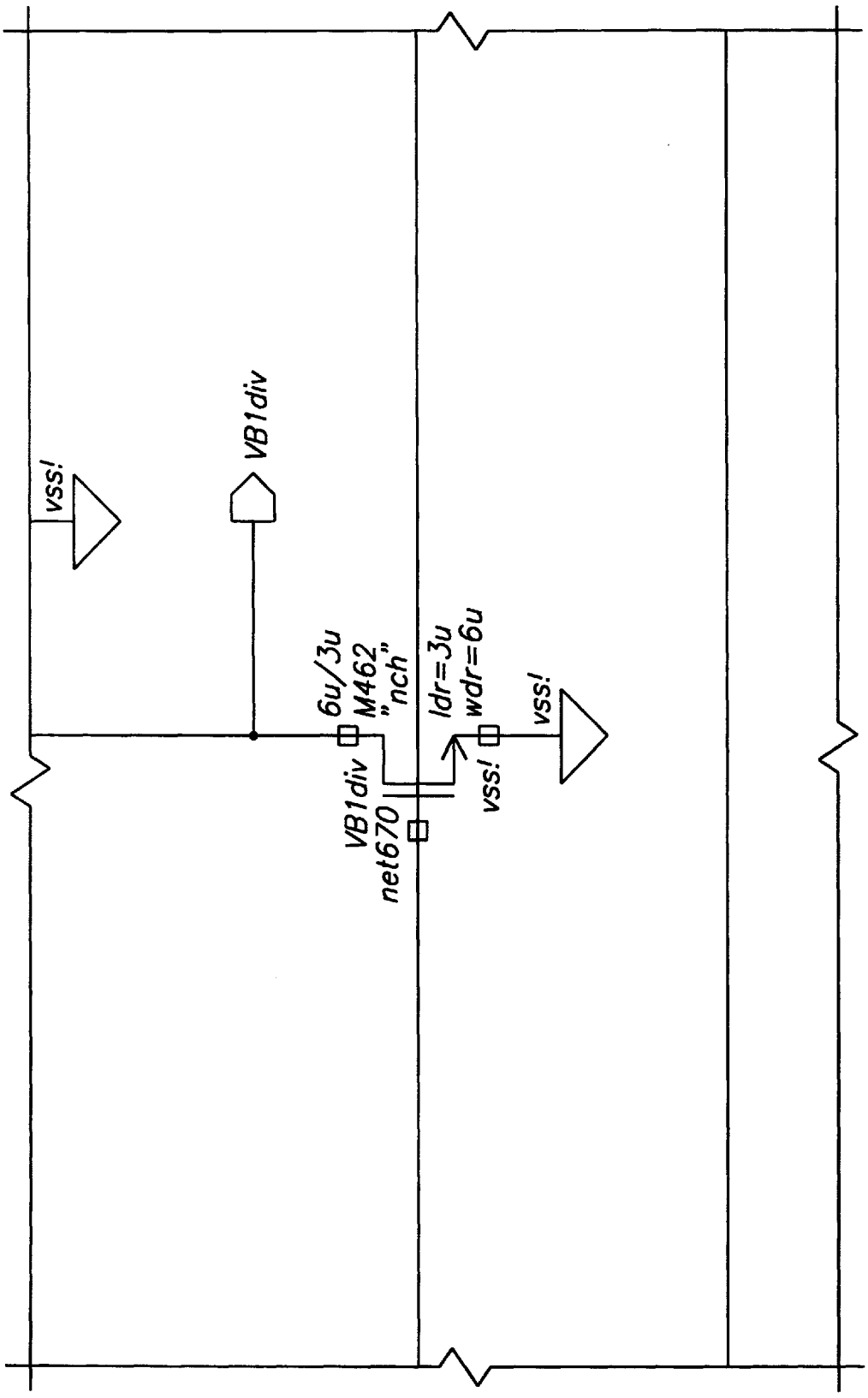
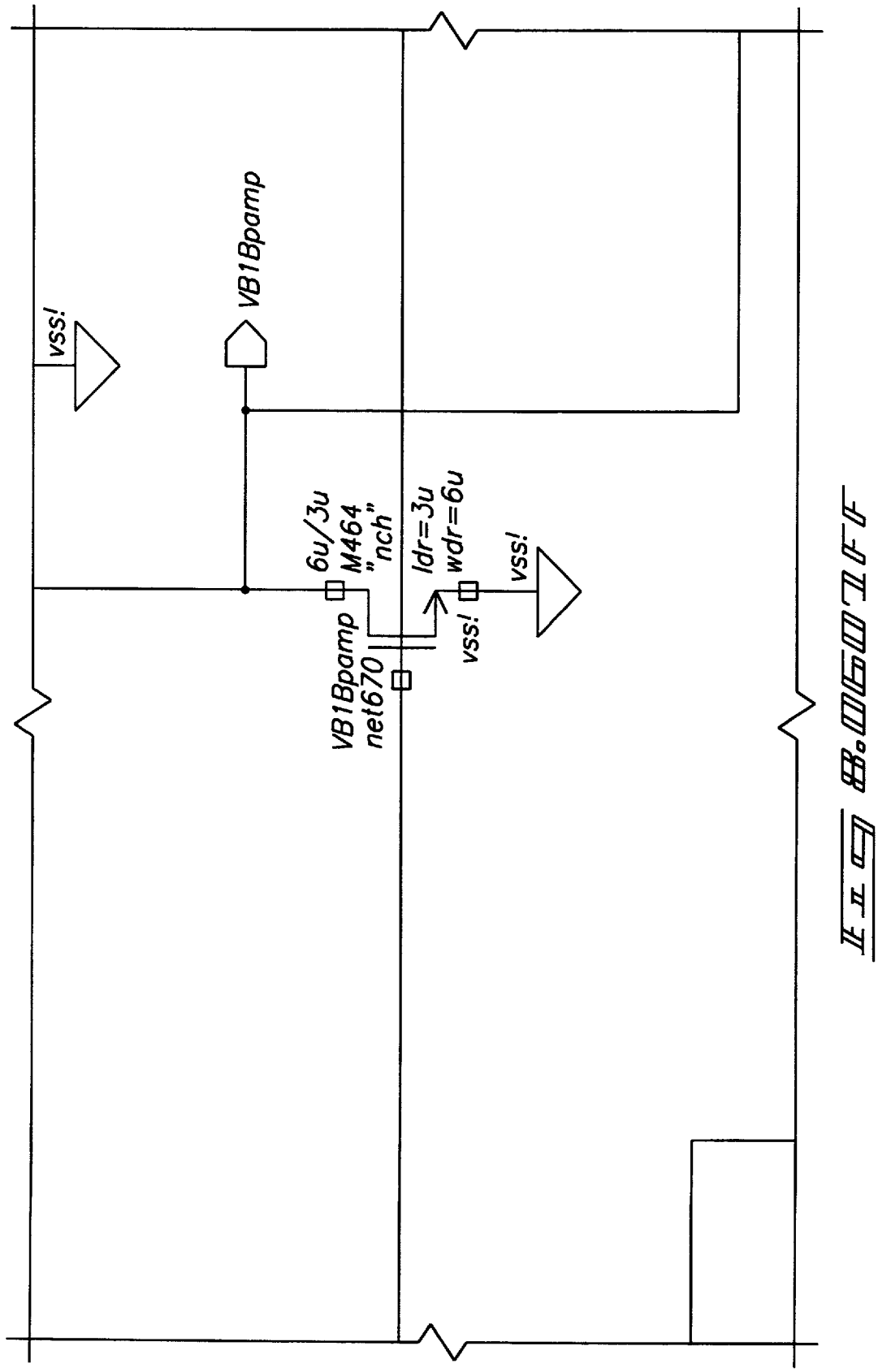


FIG 8.0050


vss!
VB1Bpamp
6u/3u
M464
"nch"
ldr=3u
wdr=6u
vss!
vss!
VB1Bpamp
net670
FIG 8.0601F

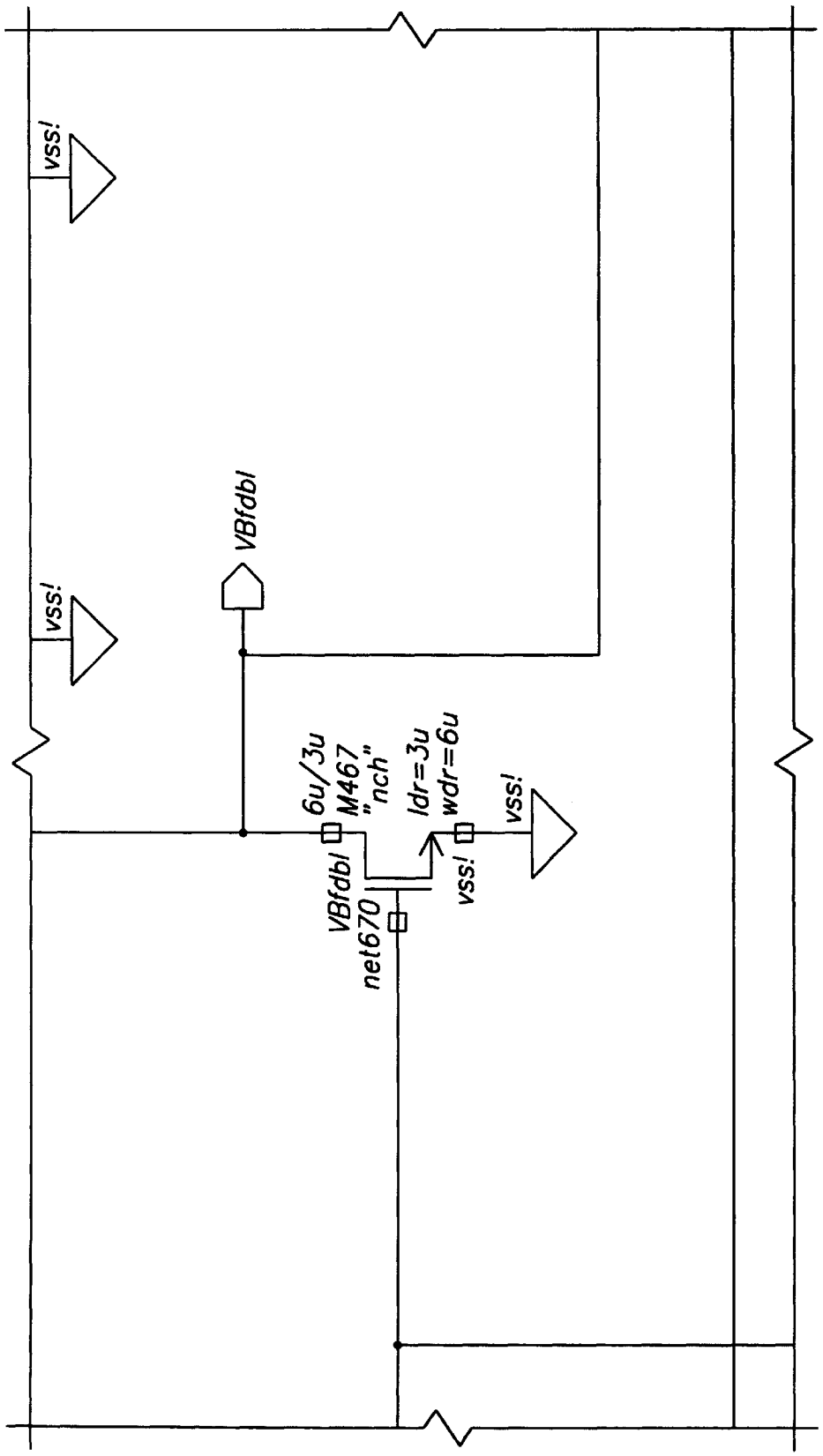


FIG 88.00500.IF5

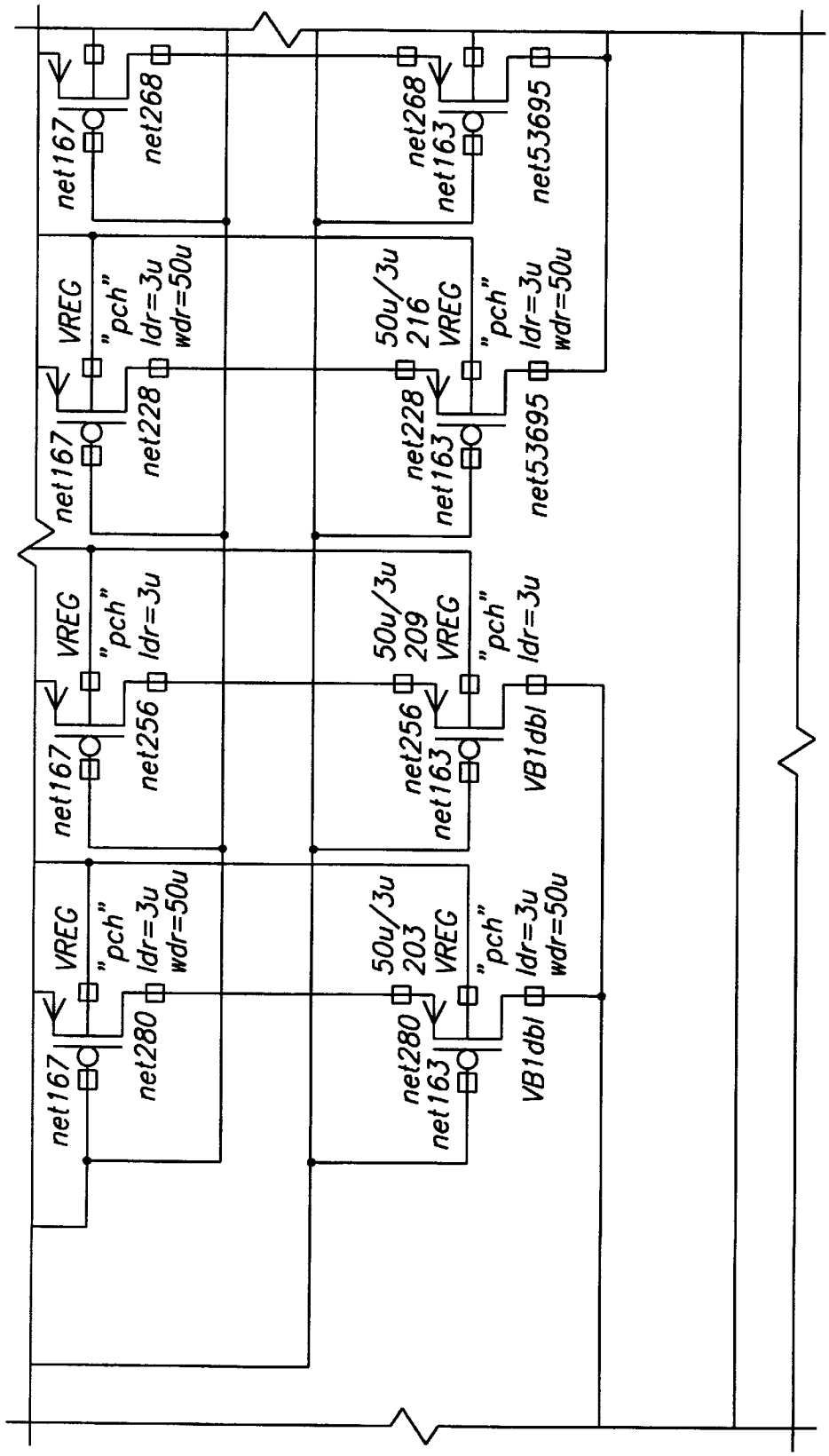

net167
net268
net268
net163
net53695
VREG
"pch"
ldr=3u
wdr=50u
50u/3u
216
net228
net167
net163
net53695
50u/3u
209
net256
net167
net163
VB1dbl
50u/3u
203
net280
net167
net163
VB1dbl

FIG. 88.0501H

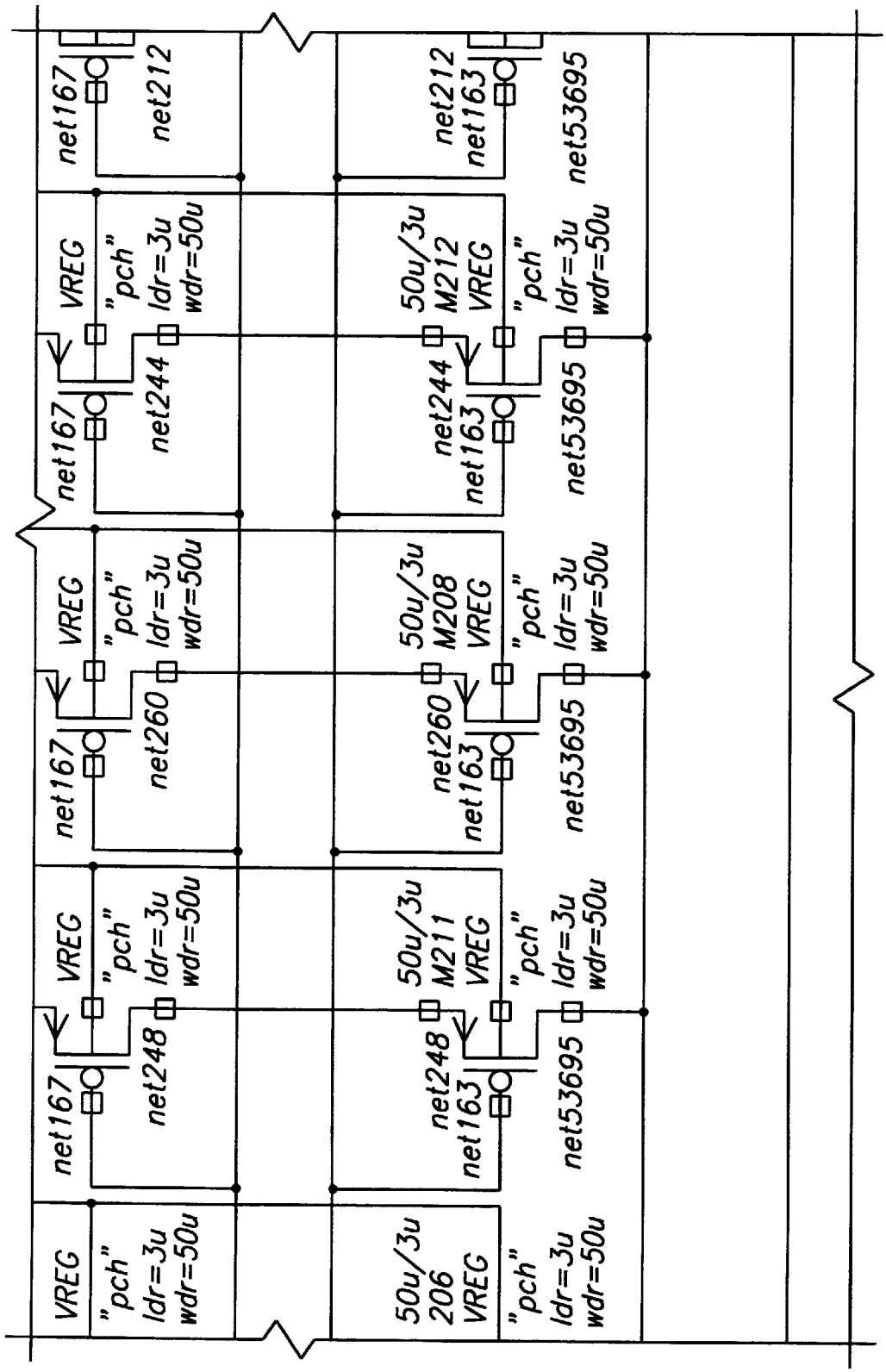

VREG
"pch"
ldr=3u
wdr=50u
50u/3u
206
VREG
net167
net248
net163
net53695
50u/3u
M211
net212
net260
M208
net244
M212
net163

FIG. 88.0050

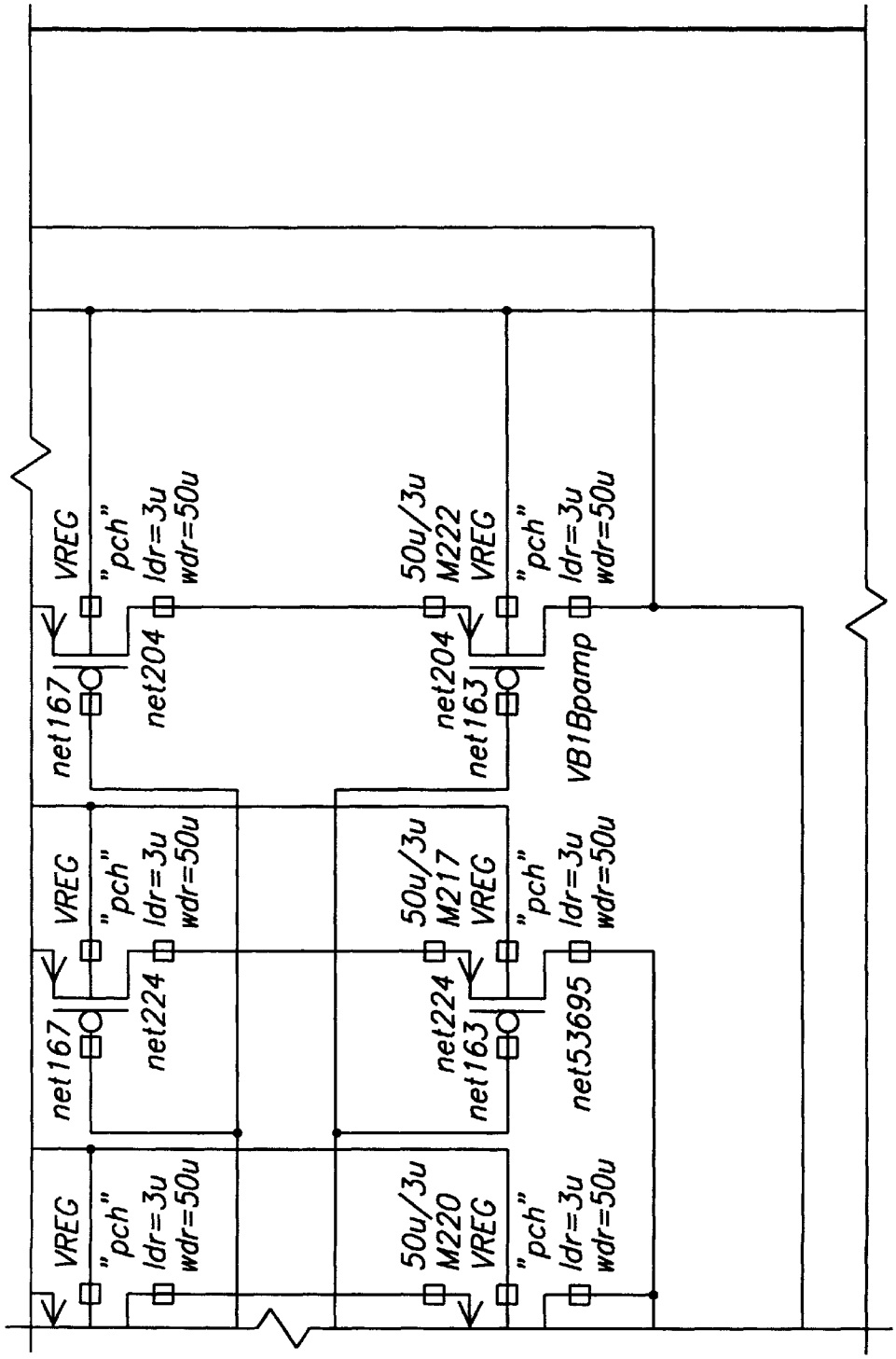

VREG
"pch"
ldr=3u
wdr=50u
net167
net204
50u/3u
M222
net163
VB1Bpamp
M217
net224
net53695
M220

FIG 8.0601F.0

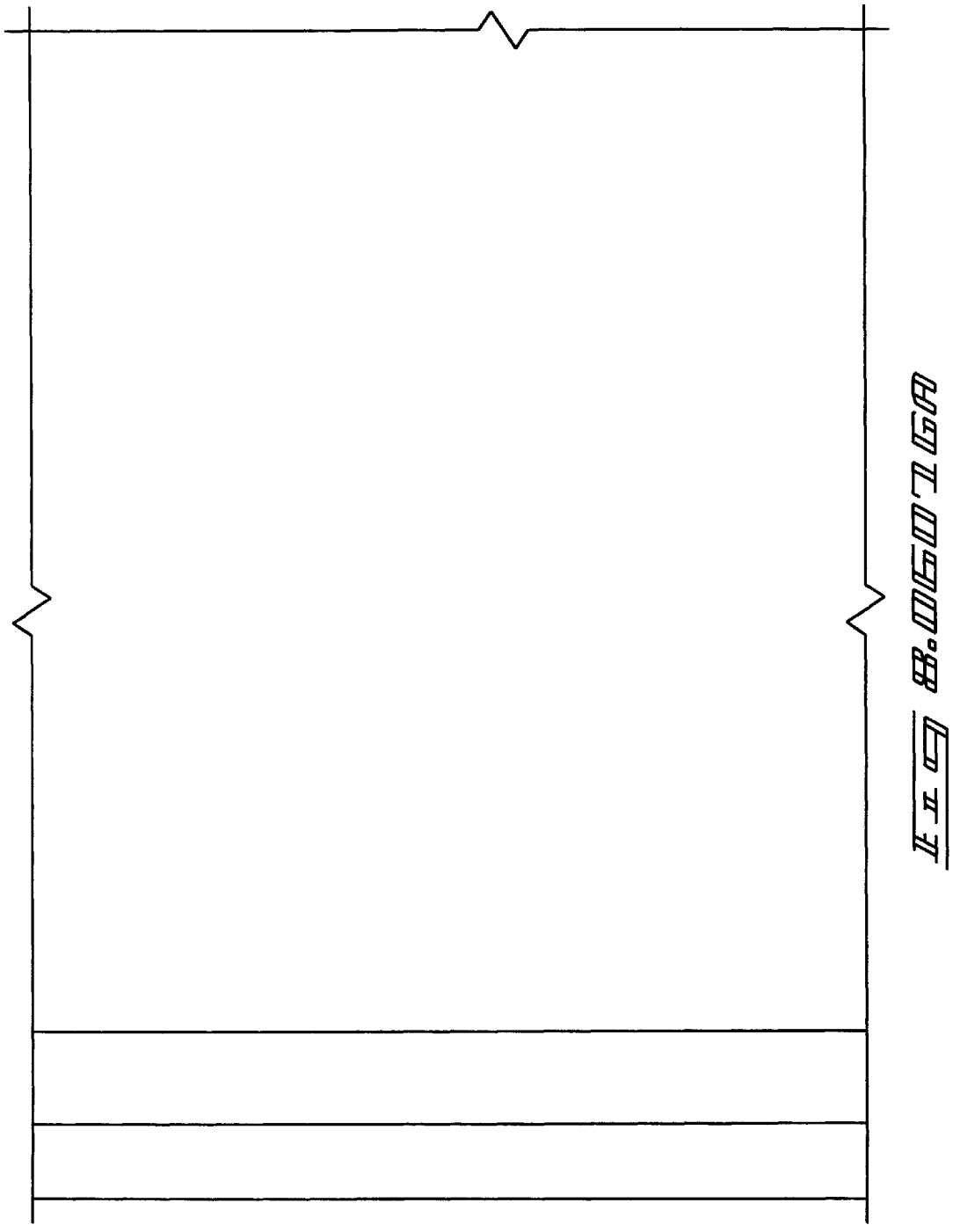


FIG 8,050,154

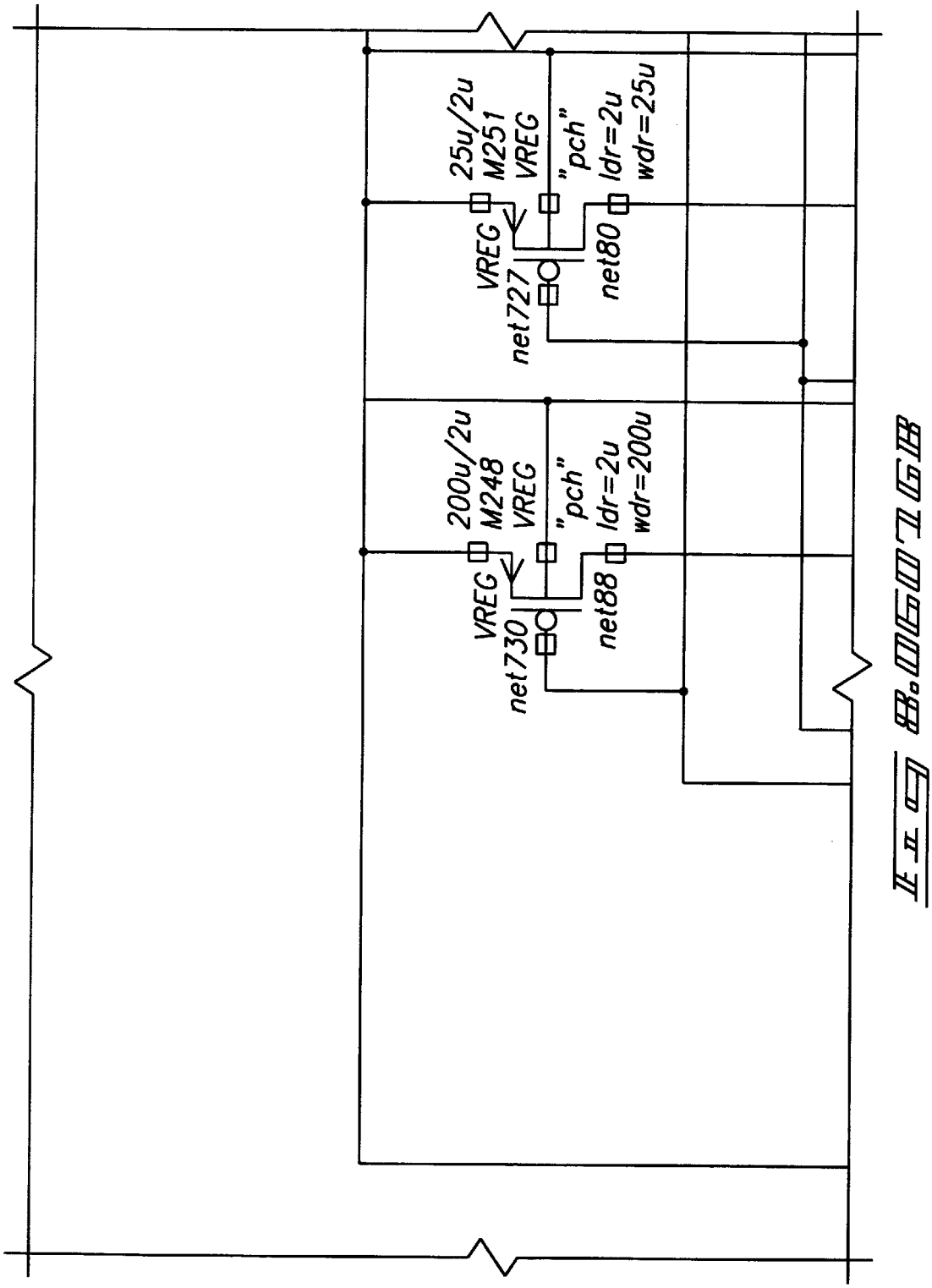

25u/2u
M251
VREG
"pch"
ldr=2u
wdr=25u
VREG
net727
net80
200u/2u
M248
VREG
"pch"
ldr=2u
wdr=200u
VREG
net730
net88

FIG 8.0501 ЕЛ

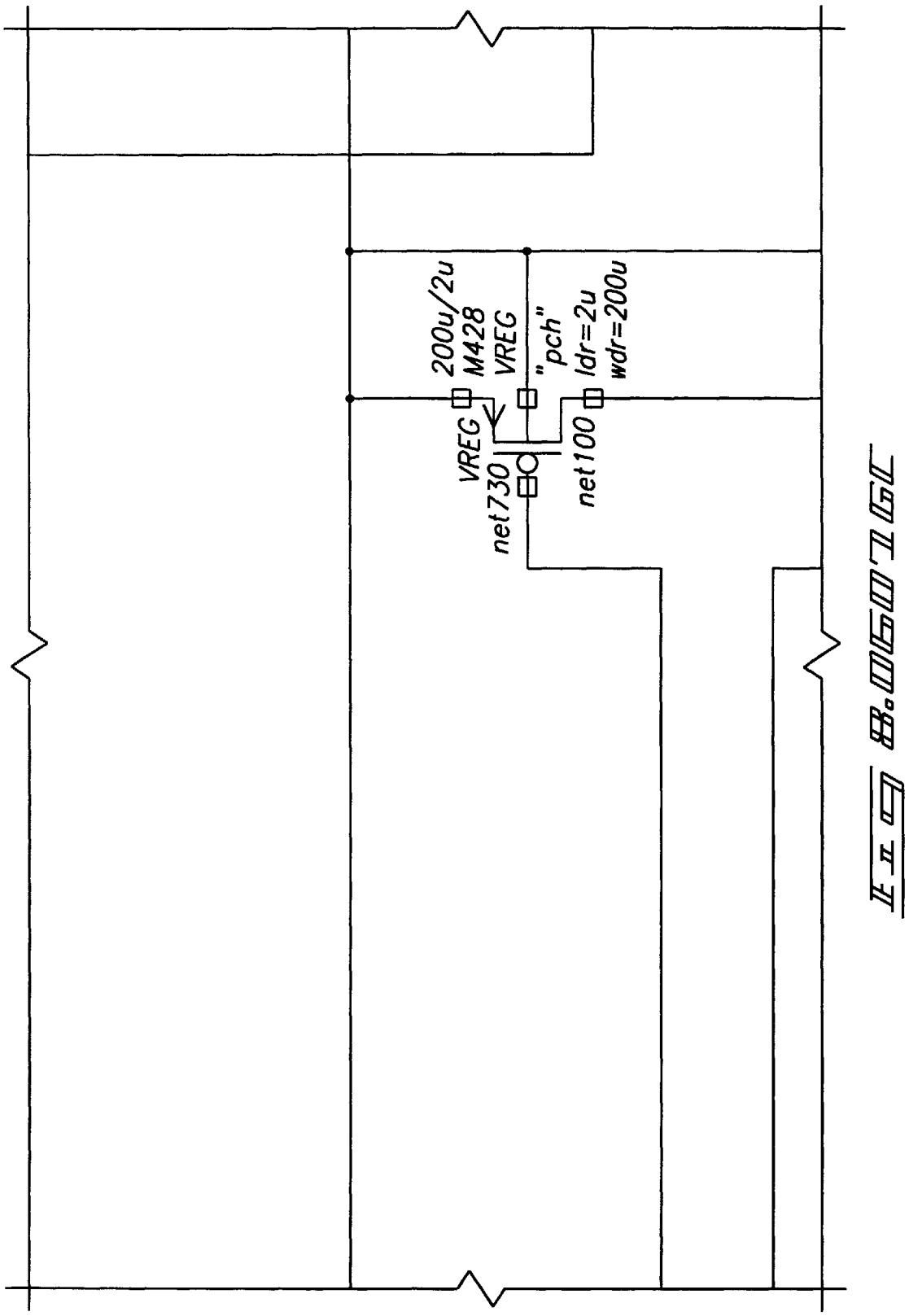


FIG. 8.0500 TO 8.0510

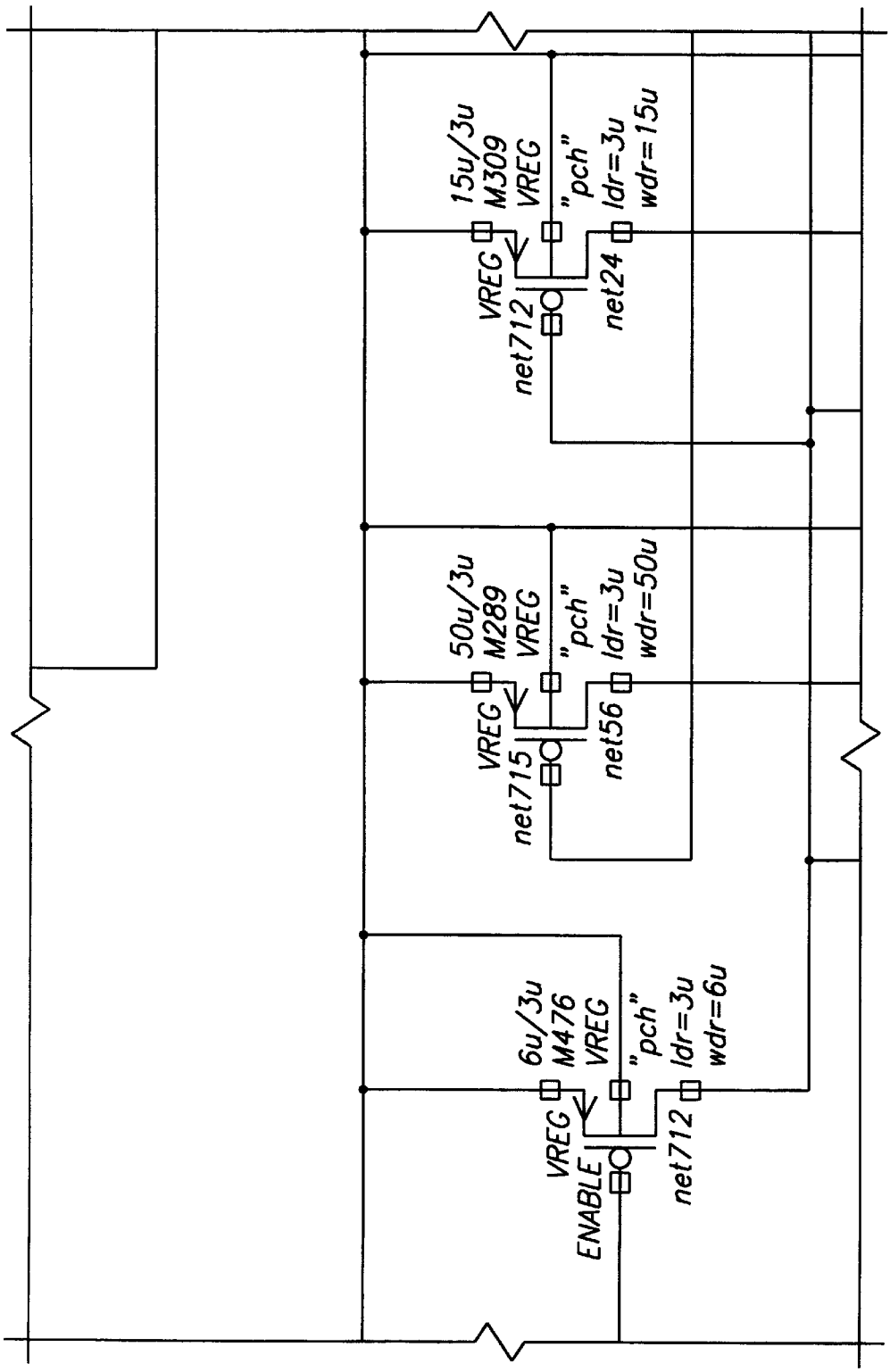

15u/3u
M309
VREG
"pch"
ldr=3u
wdr=15u
VREG
net712
net24
50u/3u
M289
VREG
"pch"
ldr=3u
wdr=50u
VREG
net715
net56
6u/3u
M476
VREG
"pch"
ldr=3u
wdr=6u
VREG
ENABLE
net712

FIG. 88,005

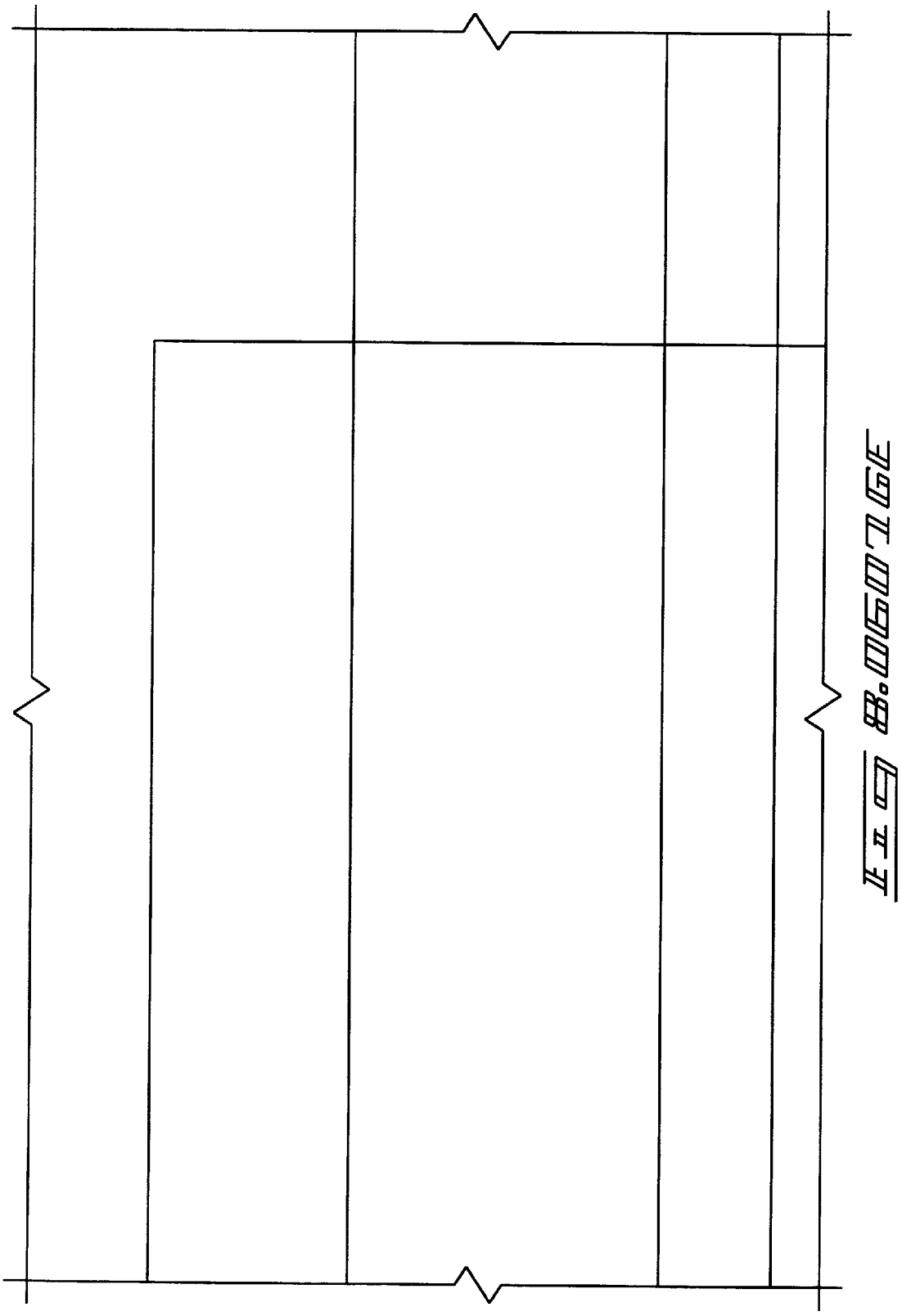


FIG 98.0507A

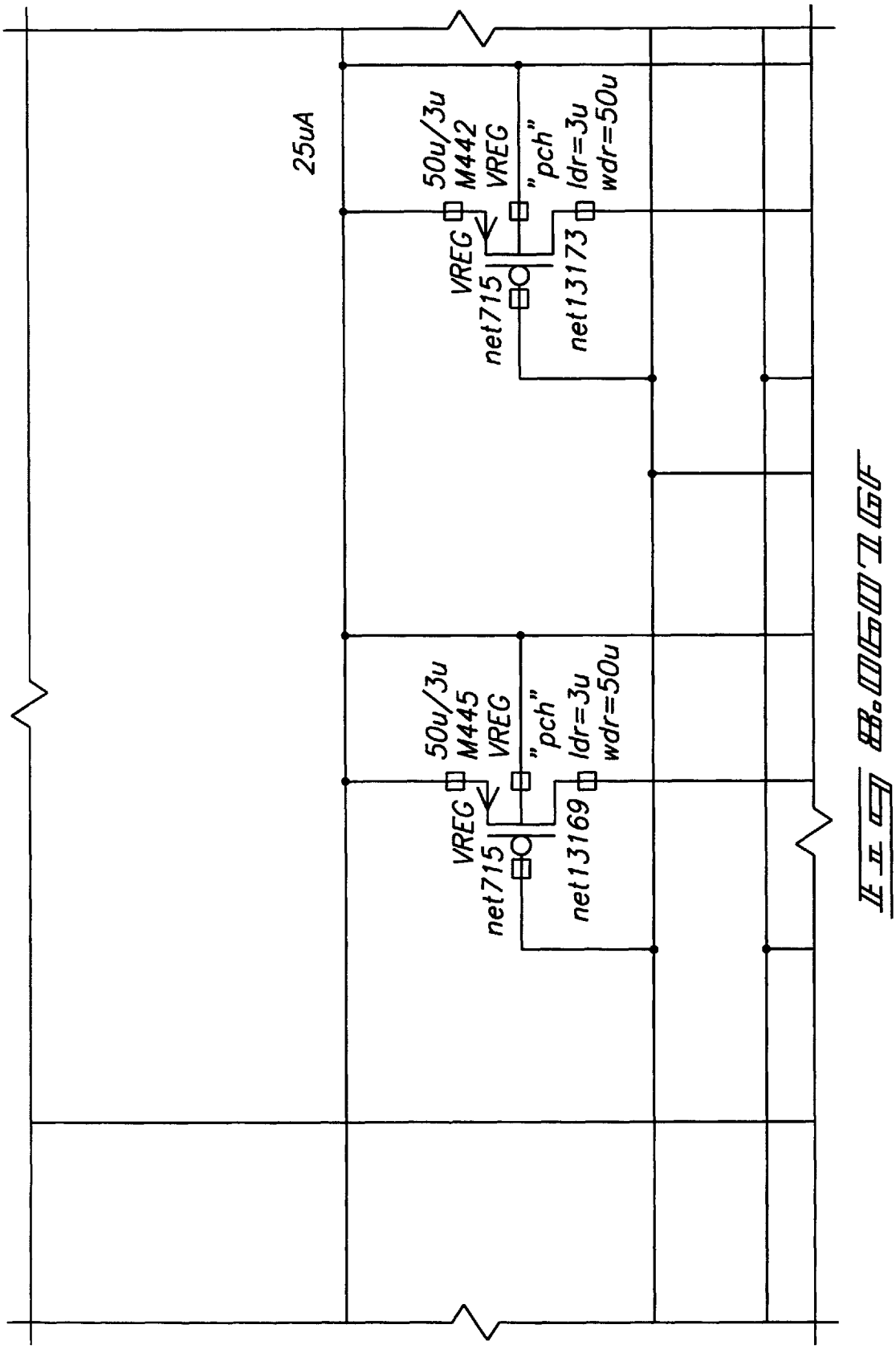


FIG. 1005.00.1.GIF

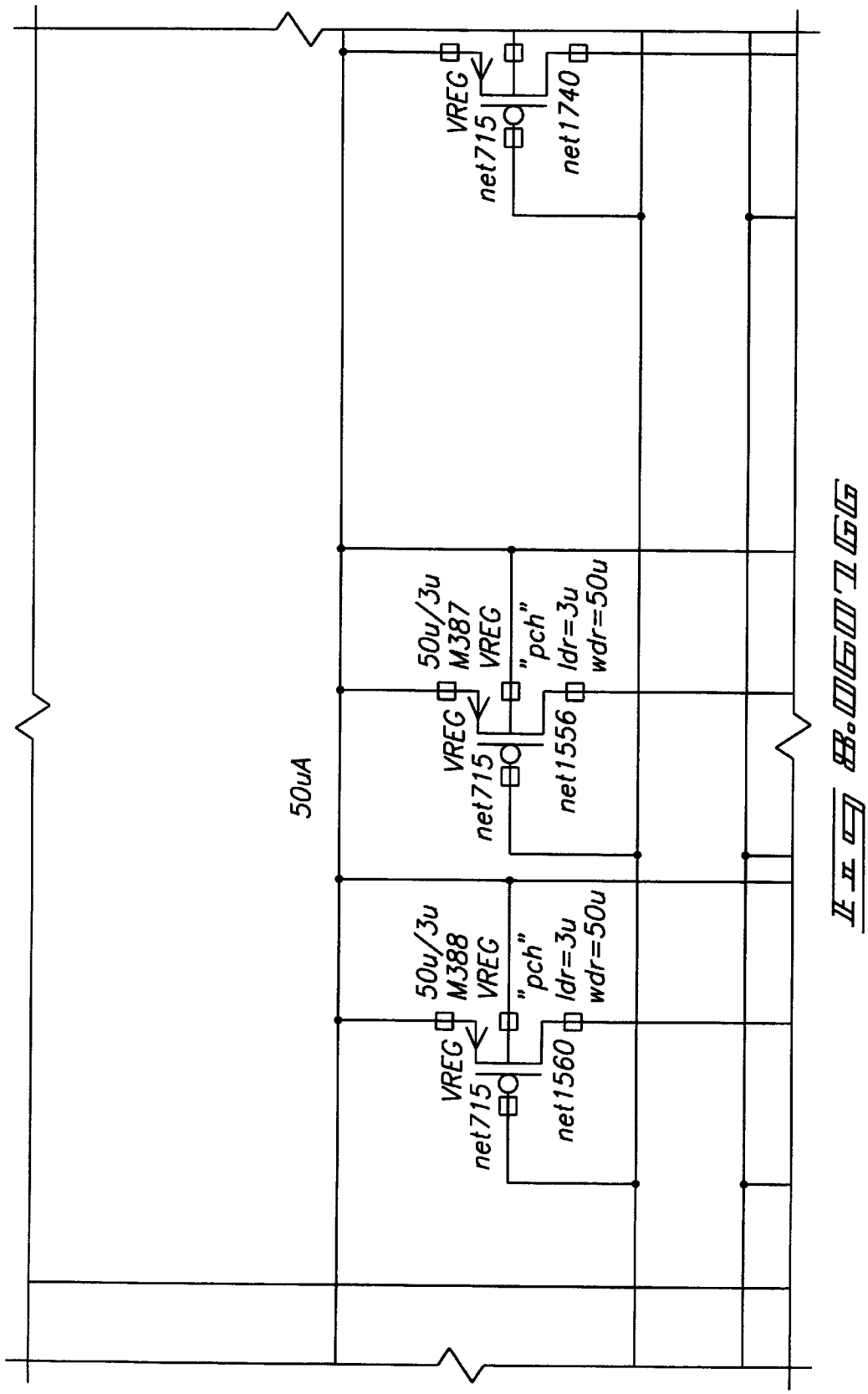


Fig. 88.0500.1169

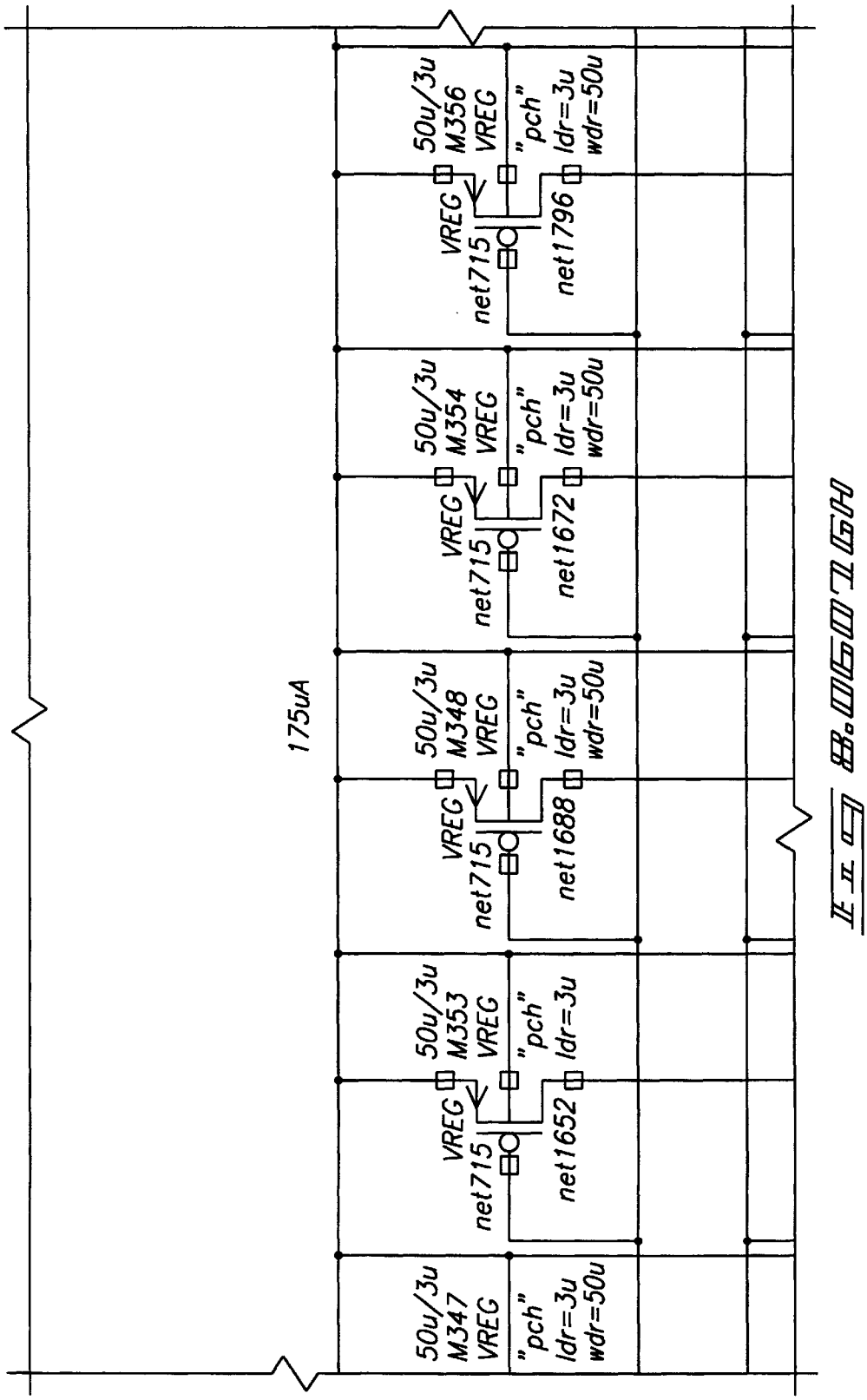


FIG. 88.0050 (1 OF 1)

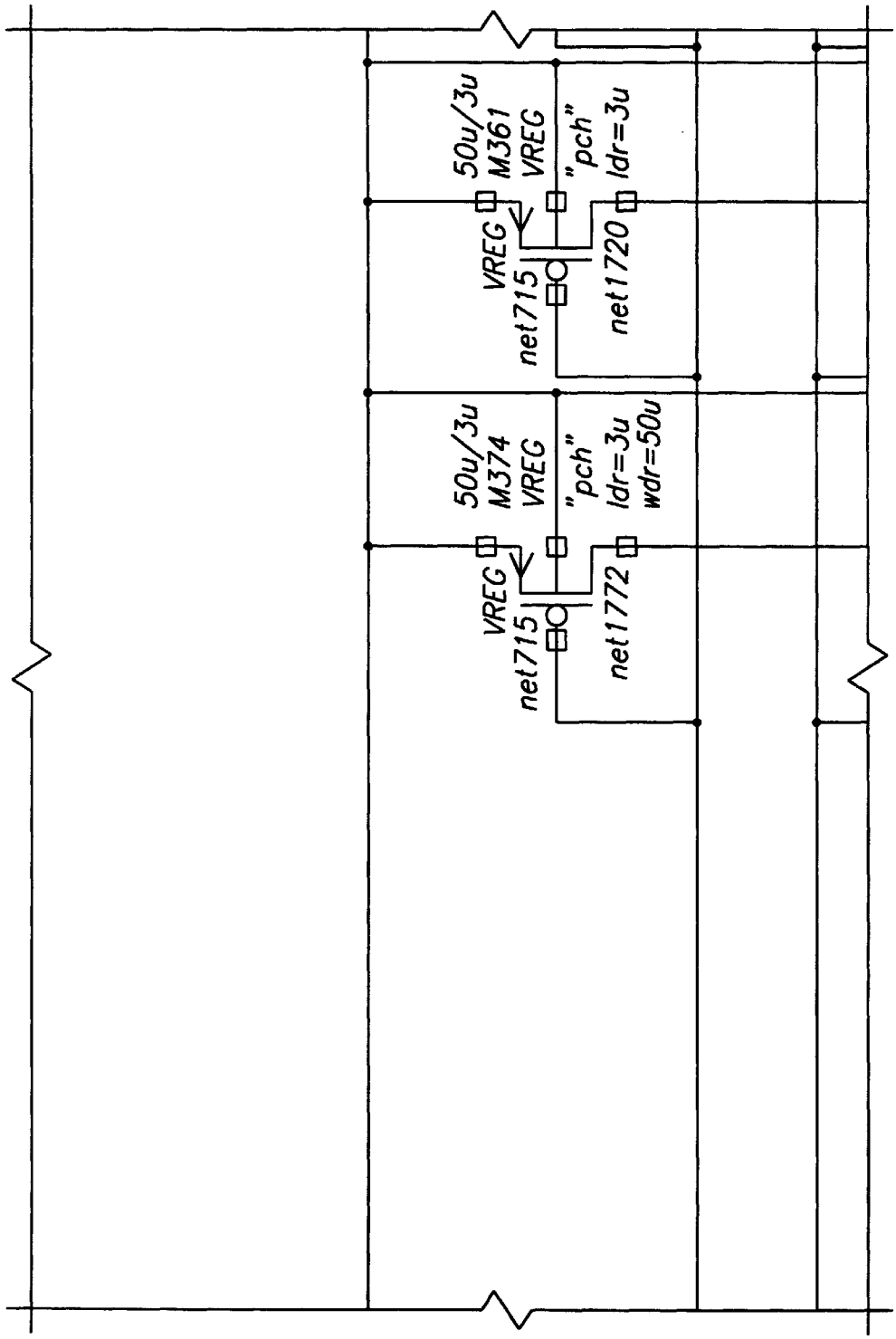

50u/3u
M361
VREG
"pch"
ldr=3u
VREG
net715
net1720
50u/3u
M374
VREG
"pch"
ldr=3u
wdr=50u
VREG
net715
net1772

FIG 8.0501

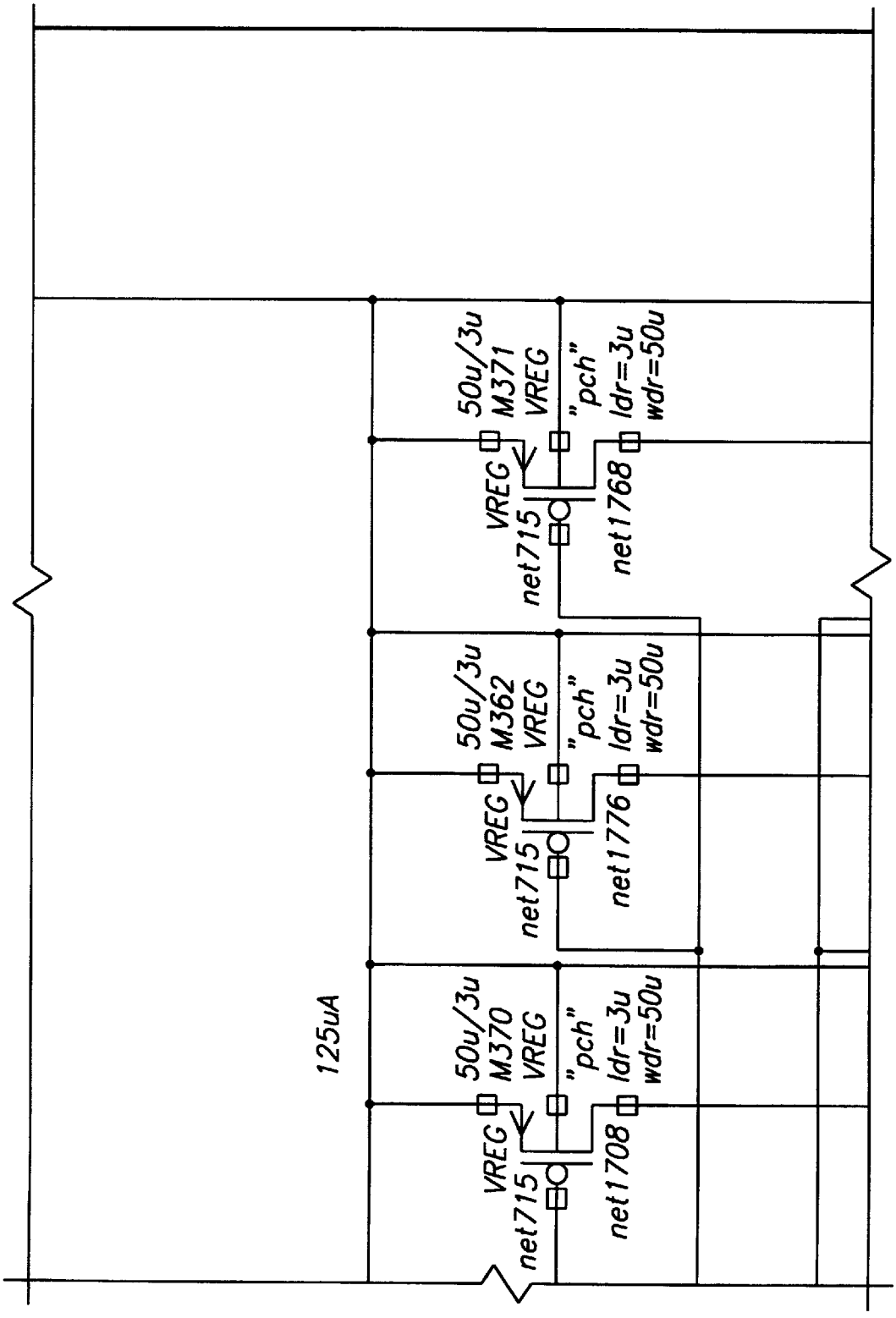

125uA
50u/3u
M370
VREG
"pch"
ldr=3u
wdr=50u
VREG
net715
net1708
50u/3u
M362
VREG
"pch"
ldr=3u
wdr=50u
VREG
net715
net1776
50u/3u
M371
VREG
"pch"
ldr=3u
wdr=50u
VREG
net715
net1768

FIG 88.0601

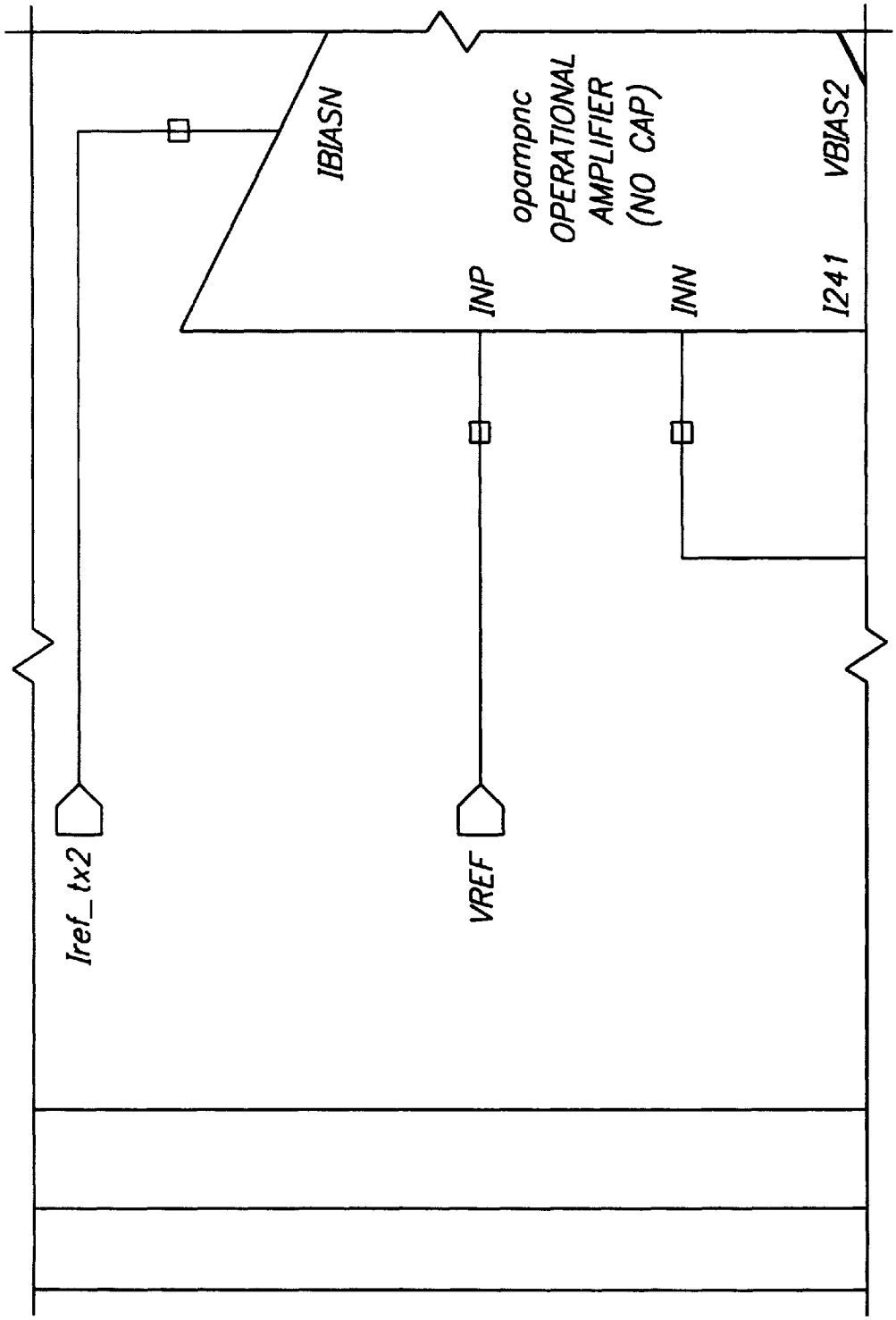


FIG. 88.0500.1H4

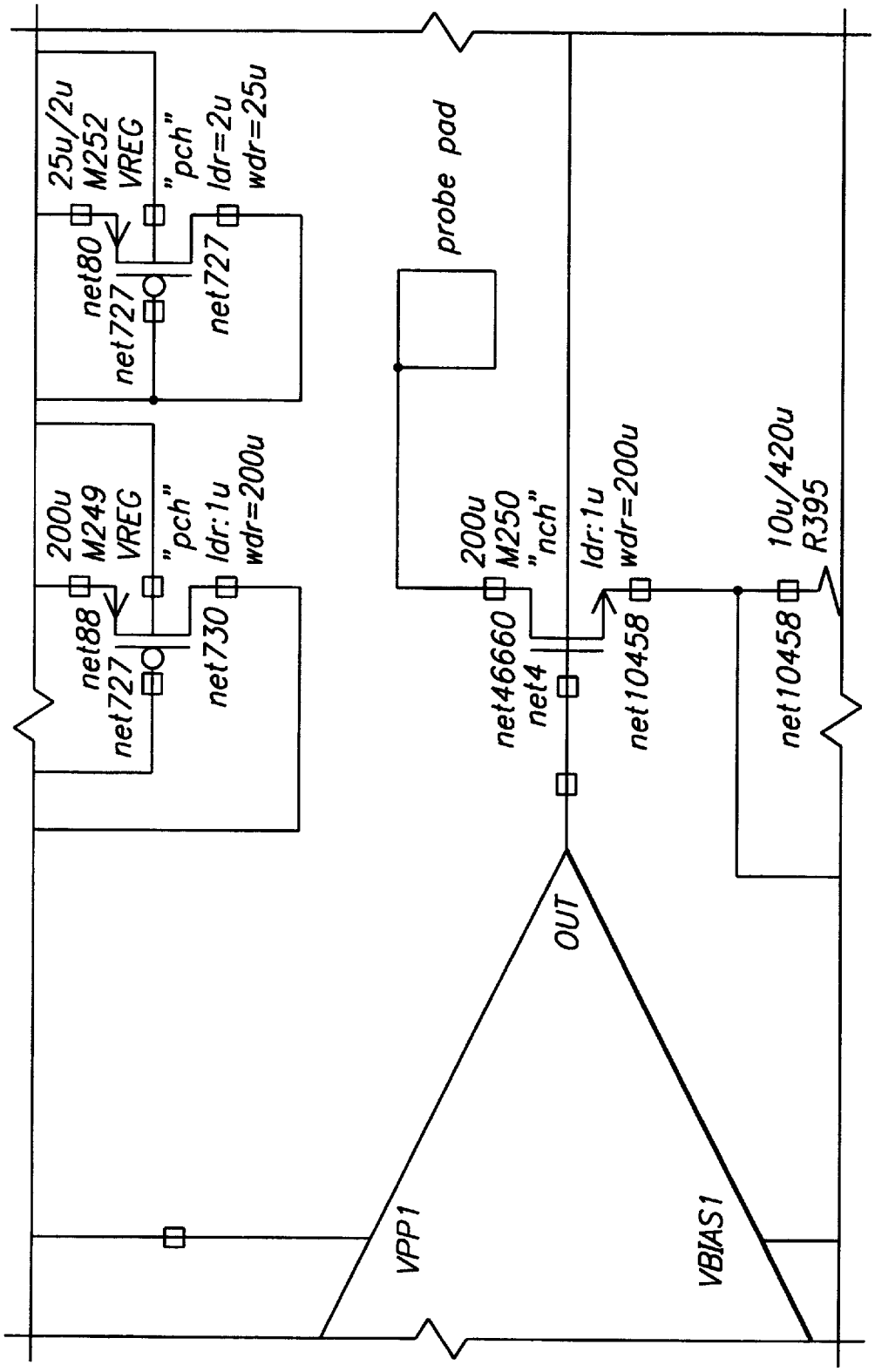

25u/2u
M252
VREG
"pch"
ldr=2u
wdr=25u
net80
net727
net727
probe pad
200u
M249
VREG
"pch"
ldr:1u
wdr=200u
net88
net727
net730
200u
M250
"nch"
ldr:1u
wdr=200u
10u/420u
R395
net46660
net4
net10458
net10458
OUT
VPP1
VBIAS1

Fig. 88,005

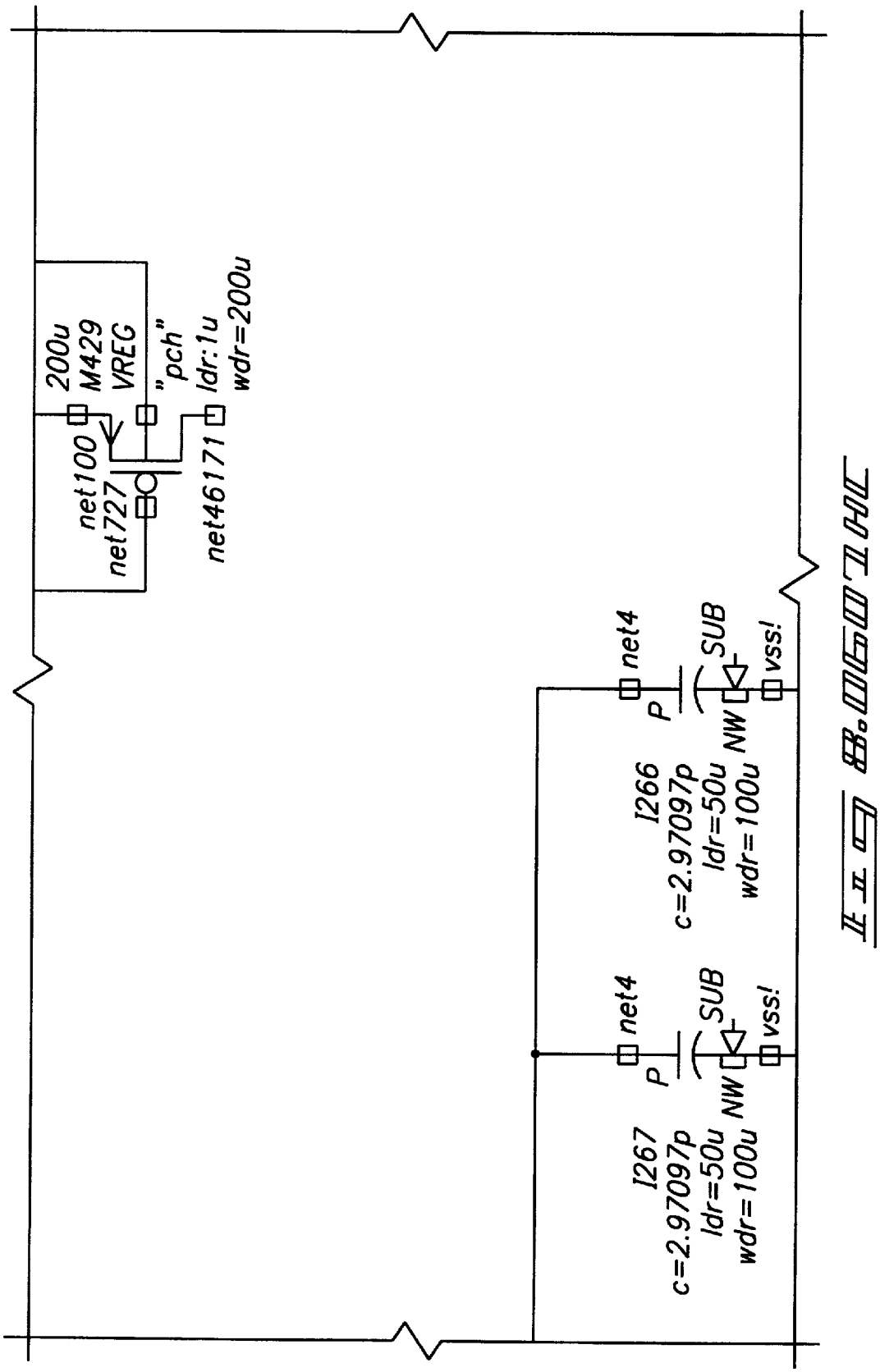

200u
M429
VREG
"pch"
ldr:1u
wdr=200u
net100
net727
net46171
net4
P
SUB
vss!
NW
I266
c=2.97097p
ldr=50u
wdr=100u
net4
P
SUB
vss!
NW
I267
c=2.97097p
ldr=50u
wdr=100u

FIG. 88,005

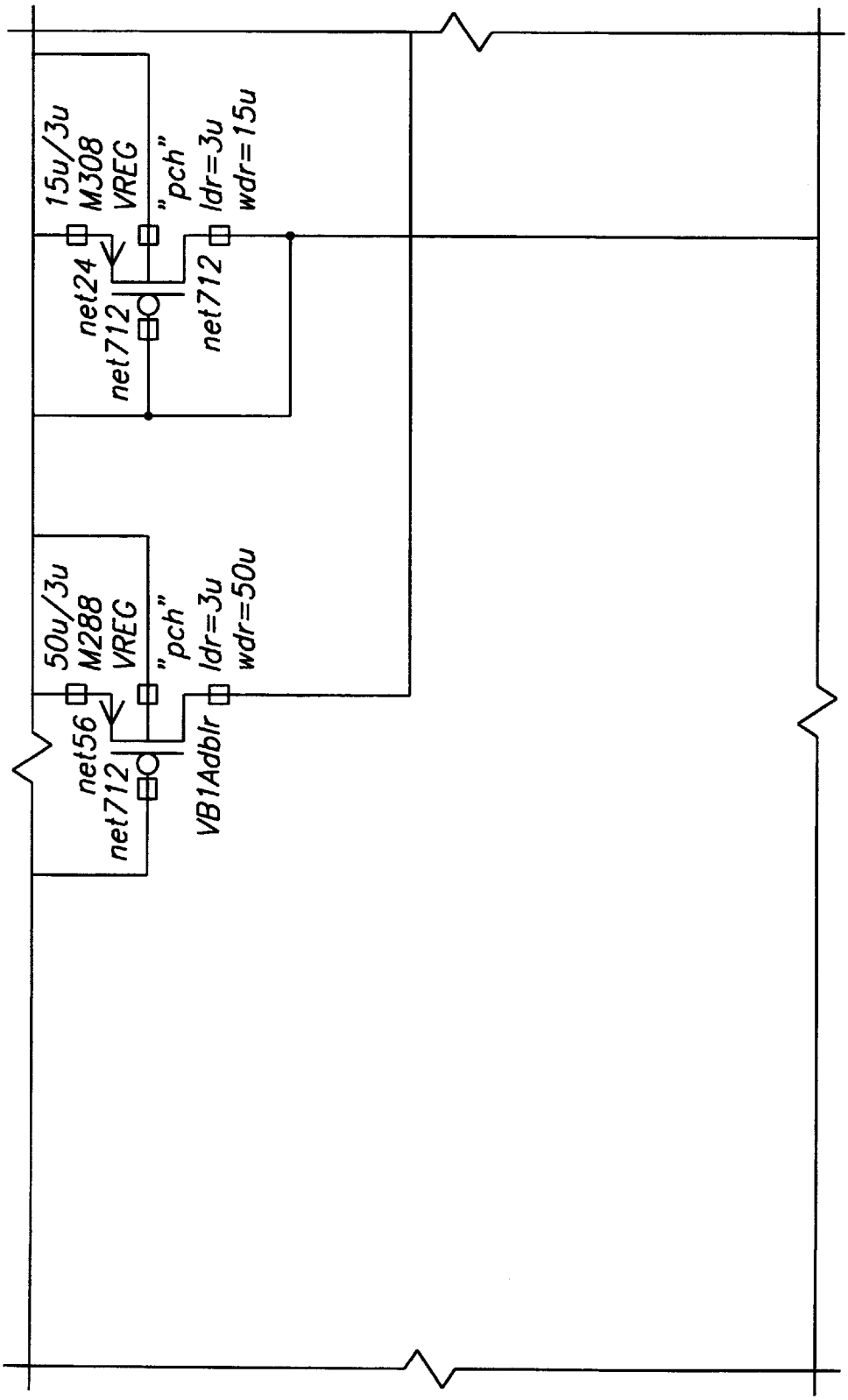

15u/3u
M308
VREG
"pch"
ldr=3u
wdr=15u
net24
net712
net712
50u/3u
M288
VREG
"pch"
ldr=3u
wdr=50u
net56
net712
VB1Adblr

FIG 8,059,711

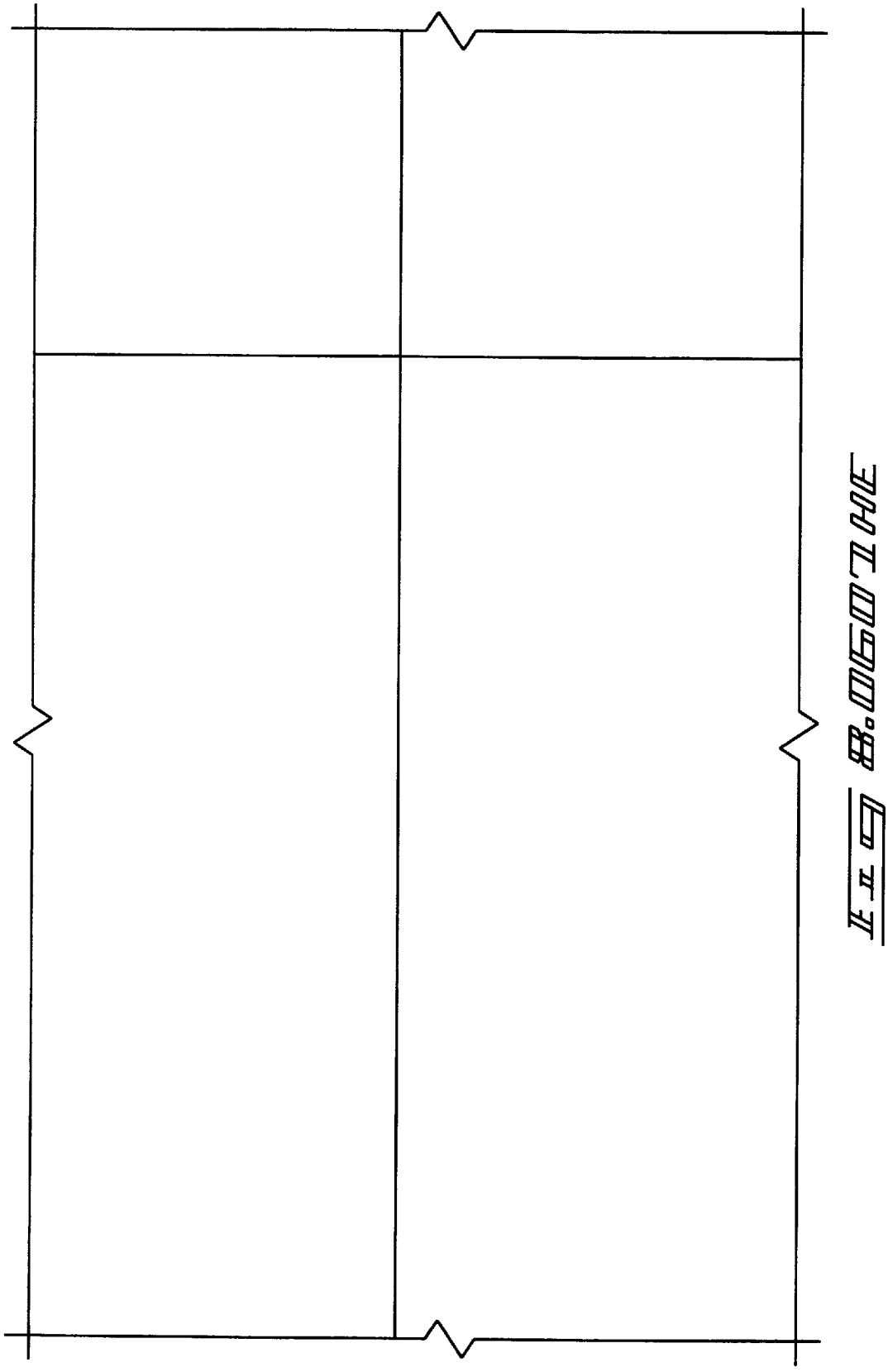


FIG 88,005 ALA

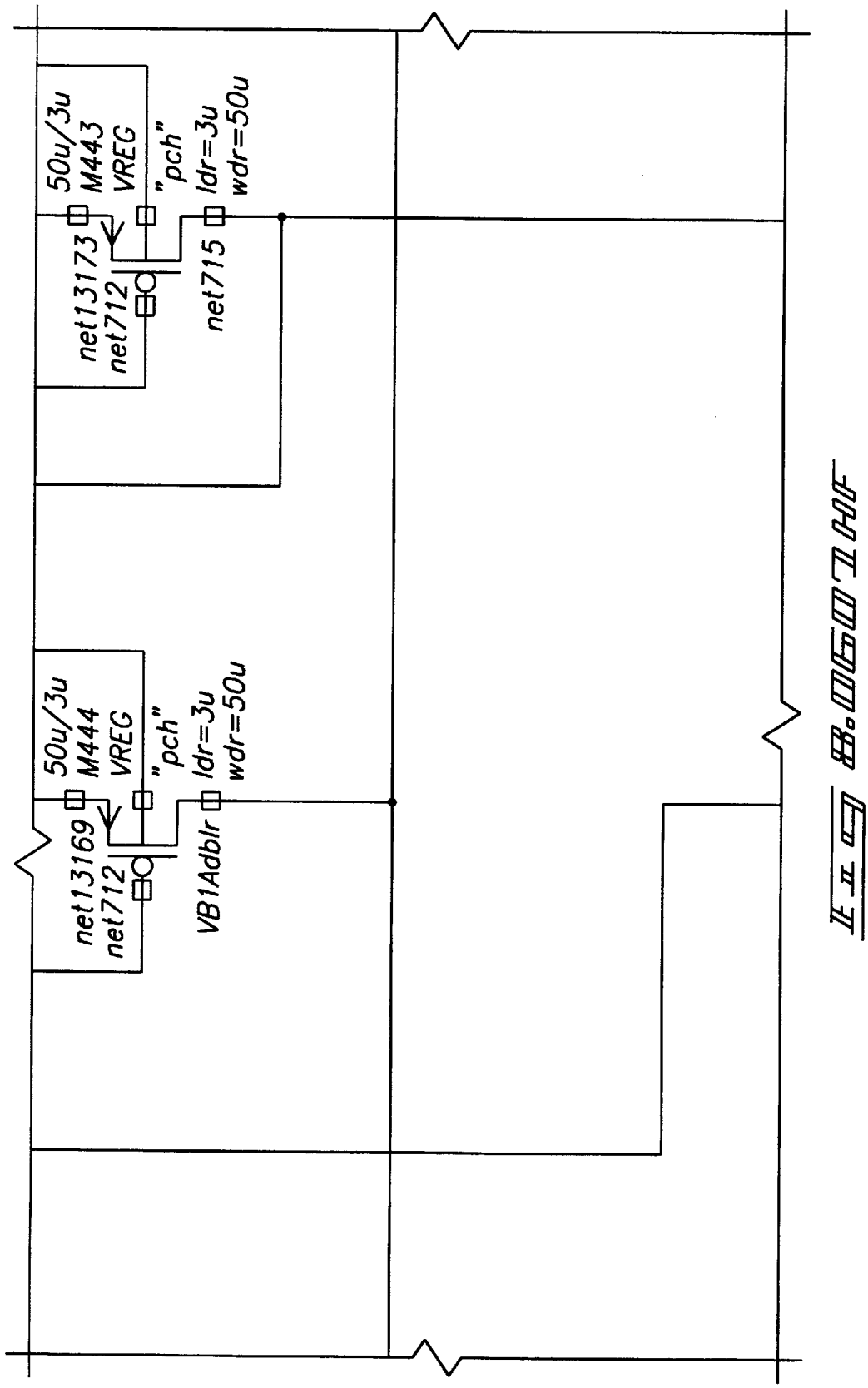

50u/3u
M443
VREG
"pch"
ldr=3u
wdr=50u
net13173
net712
net715
50u/3u
M444
VREG
"pch"
ldr=3u
wdr=50u
net13169
net712
VB1Adblr

FIG. 88,005

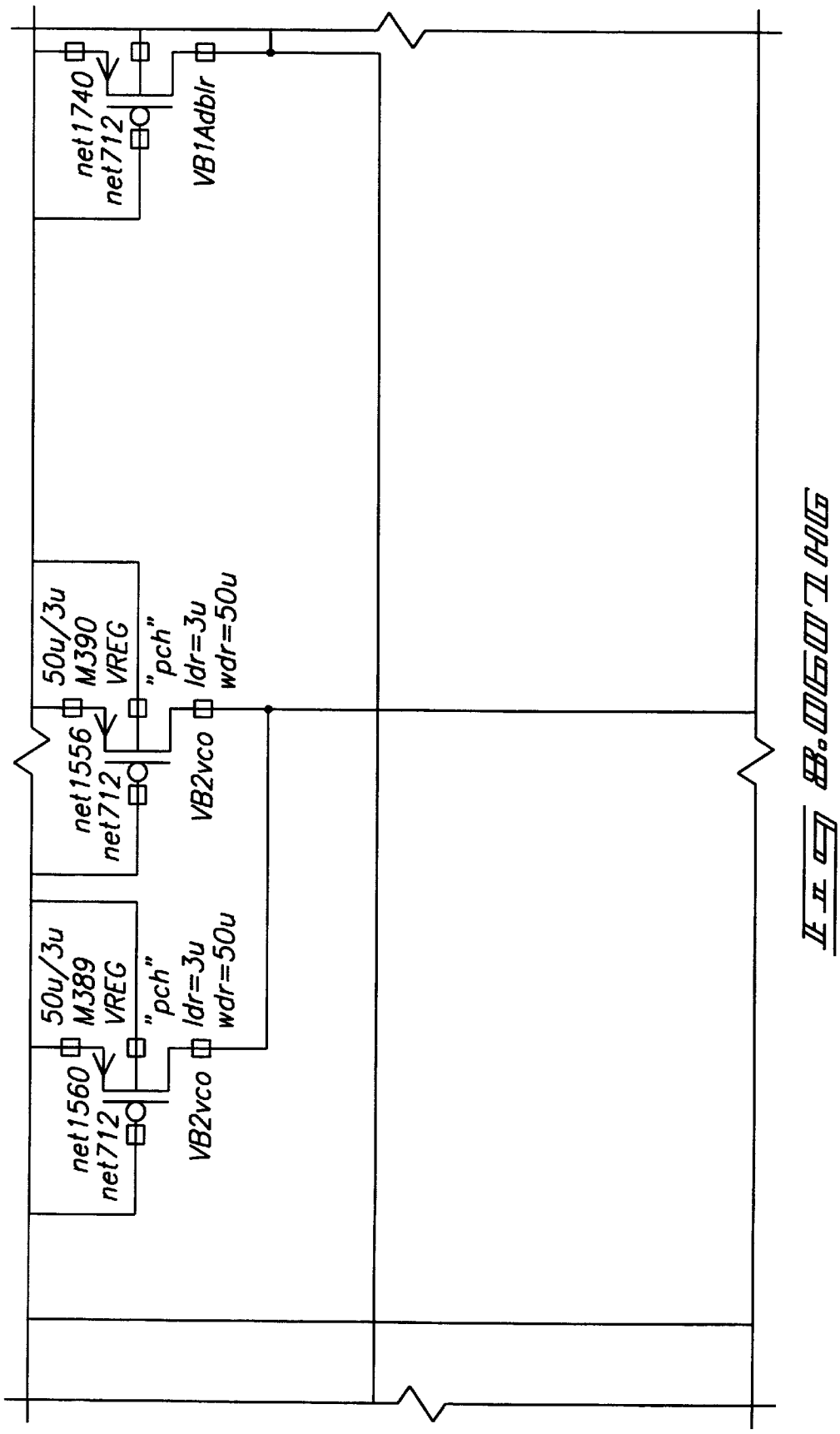

net1740
net712
VB1Adblr
50u/3u
M390
VREG
"pch"
ldr=3u
wdr=50u
net1556
net712
VB2vco
50u/3u
M389
VREG
"pch"
ldr=3u
wdr=50u
net1560
net712
VB2vco

FIG. 88.0056

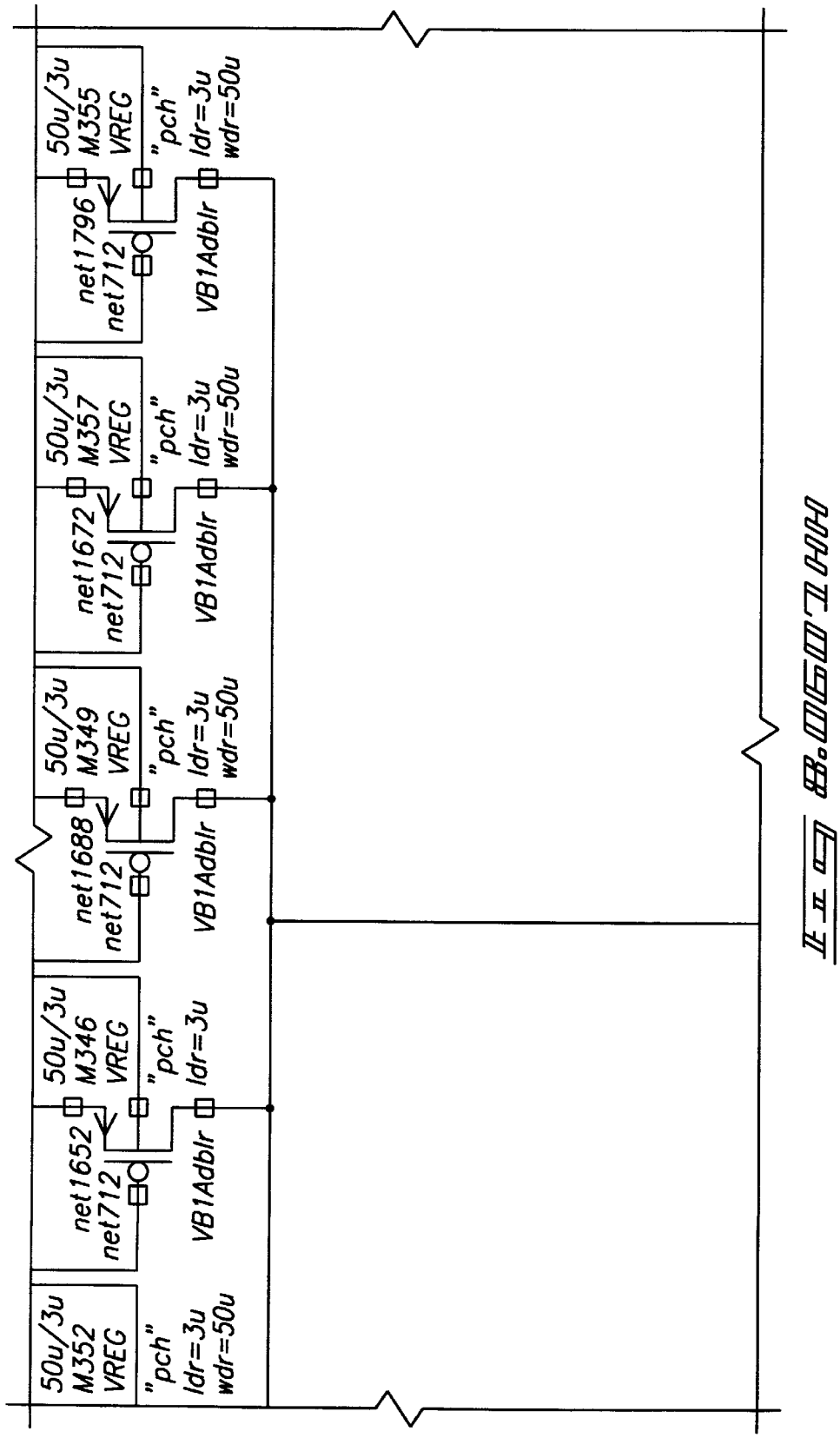


FIG. 88.0950 (PRIOR ART)

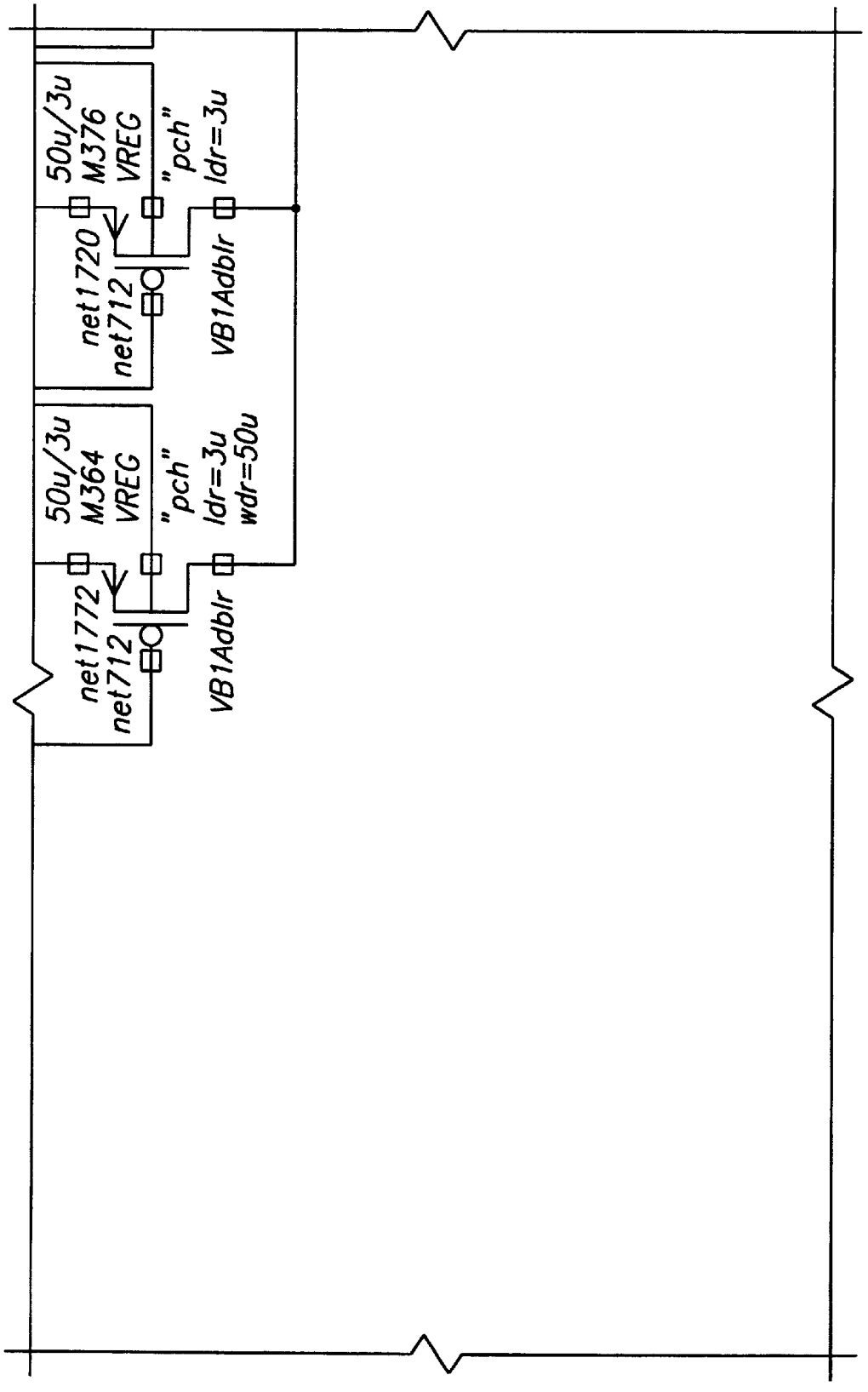

50u/3u
M376
VREG
"pch"
ldr=3u
net1720
net712
VB1Adblr
50u/3u
M364
VREG
"pch"
ldr=3u
wdr=50u
net1772
net712
VB1Adblr

FIG. 88,005

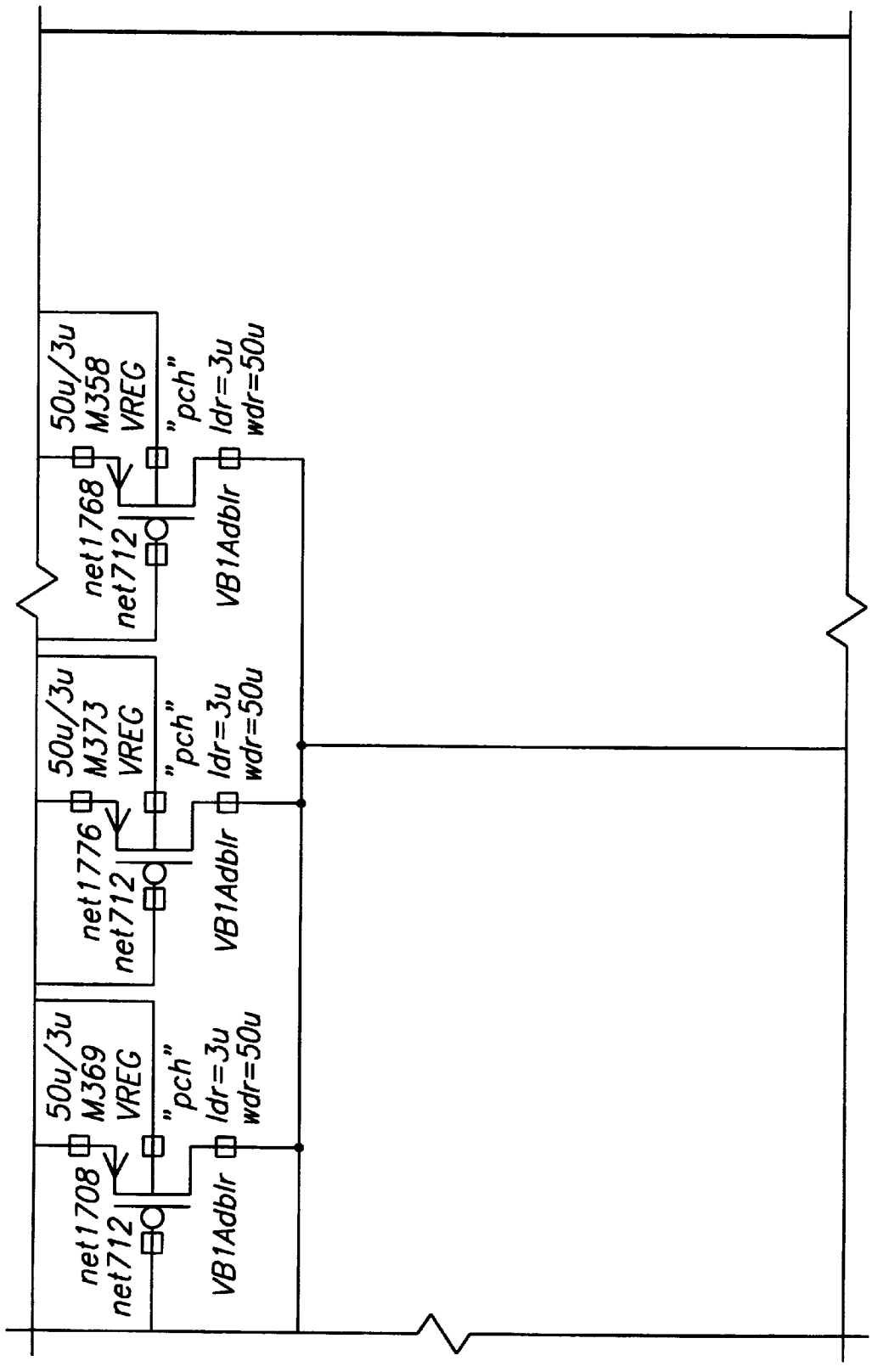

50u/3u
M358
VREG
"pch"
ldr=3u
wdr=50u
net1768
net712
VB1Adblr
50u/3u
M373
VREG
"pch"
ldr=3u
wdr=50u
net1776
net712
VB1Adblr
50u/3u
M369
VREG
"pch"
ldr=3u
wdr=50u
net1708
net712
VB1Adblr

Fig 88.0500

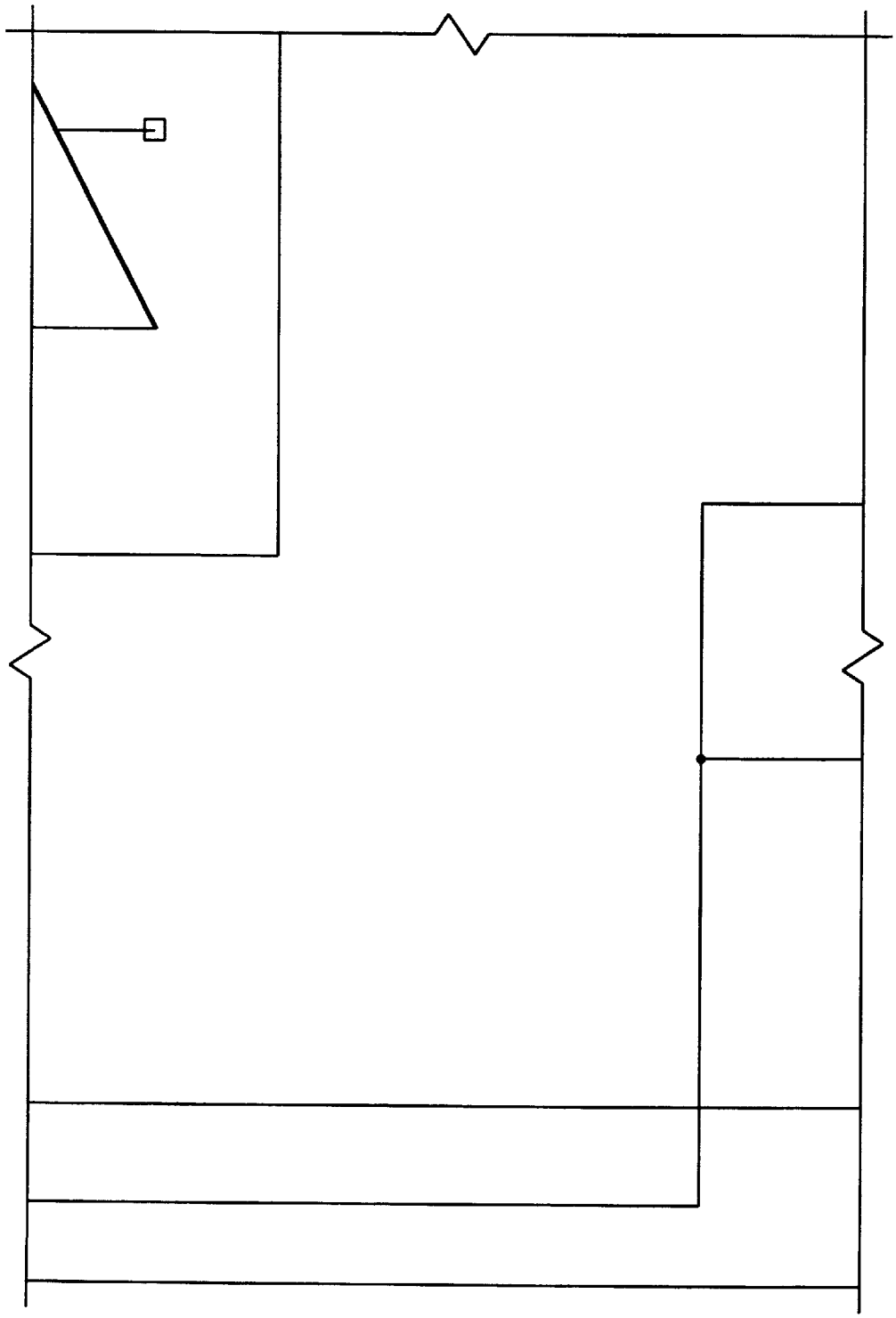
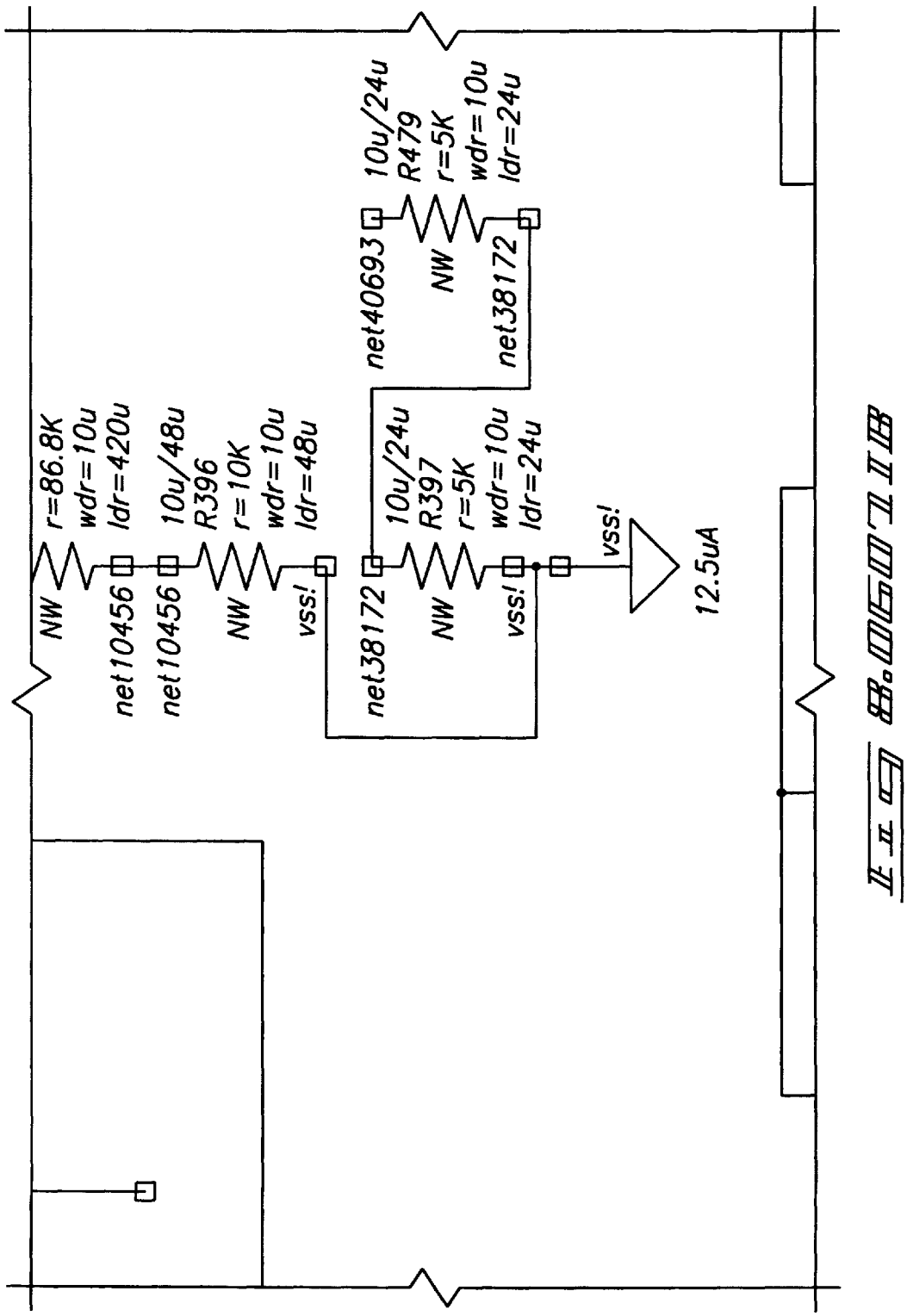


FIG 98,005A


r=86.8K
wdr=10u
ldr=420u
NW
net10456
10u/48u
R396
r=10K
wdr=10u
ldr=48u
net10456
NW
vss!
net38172
10u/24u
R397
r=5K
wdr=10u
ldr=24u
net38172
NW
vss!
net40693
10u/24u
R479
r=5K
wdr=10u
ldr=24u
net38172
NW
vss!
12.5uA

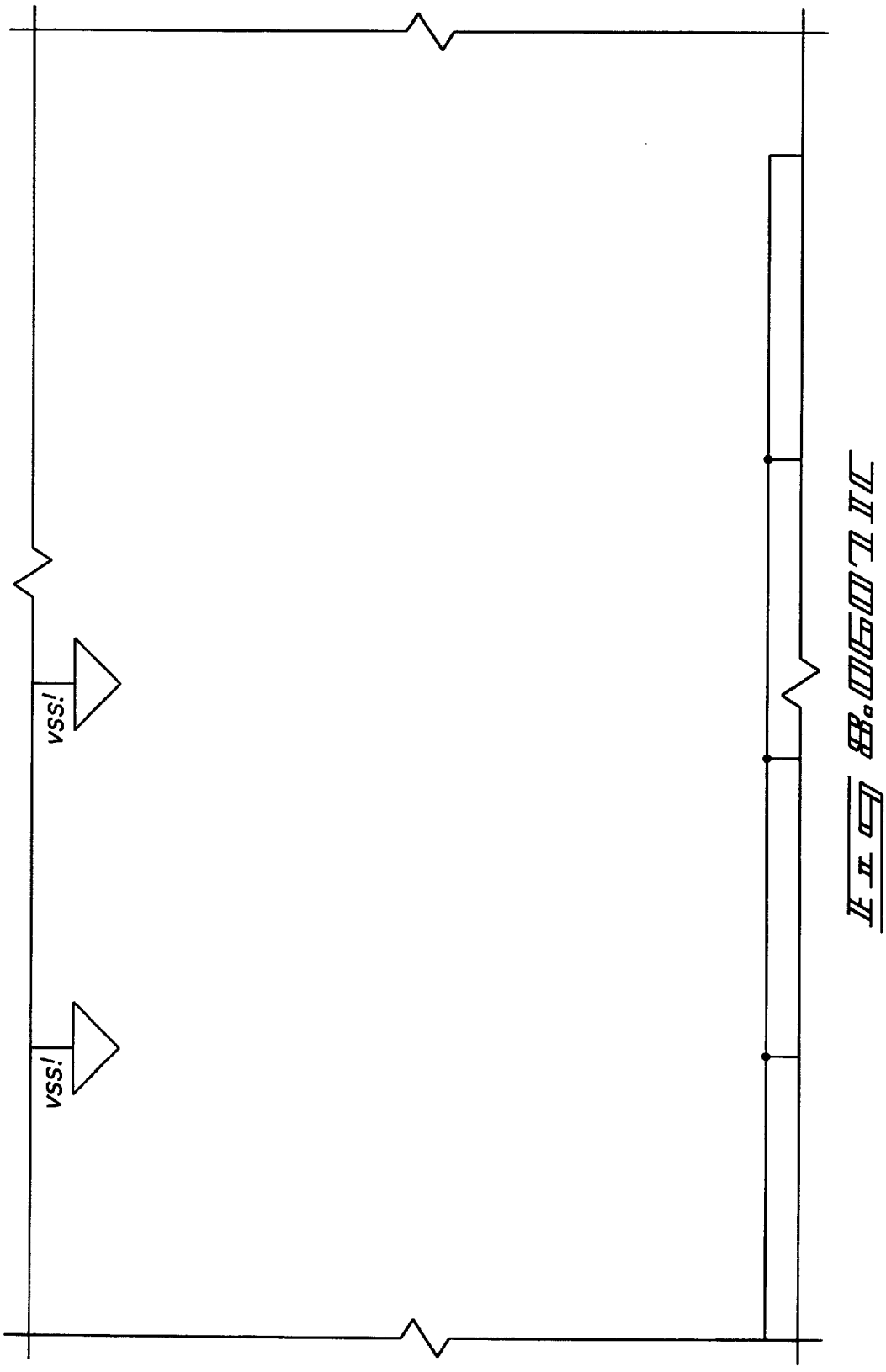


FIG 88

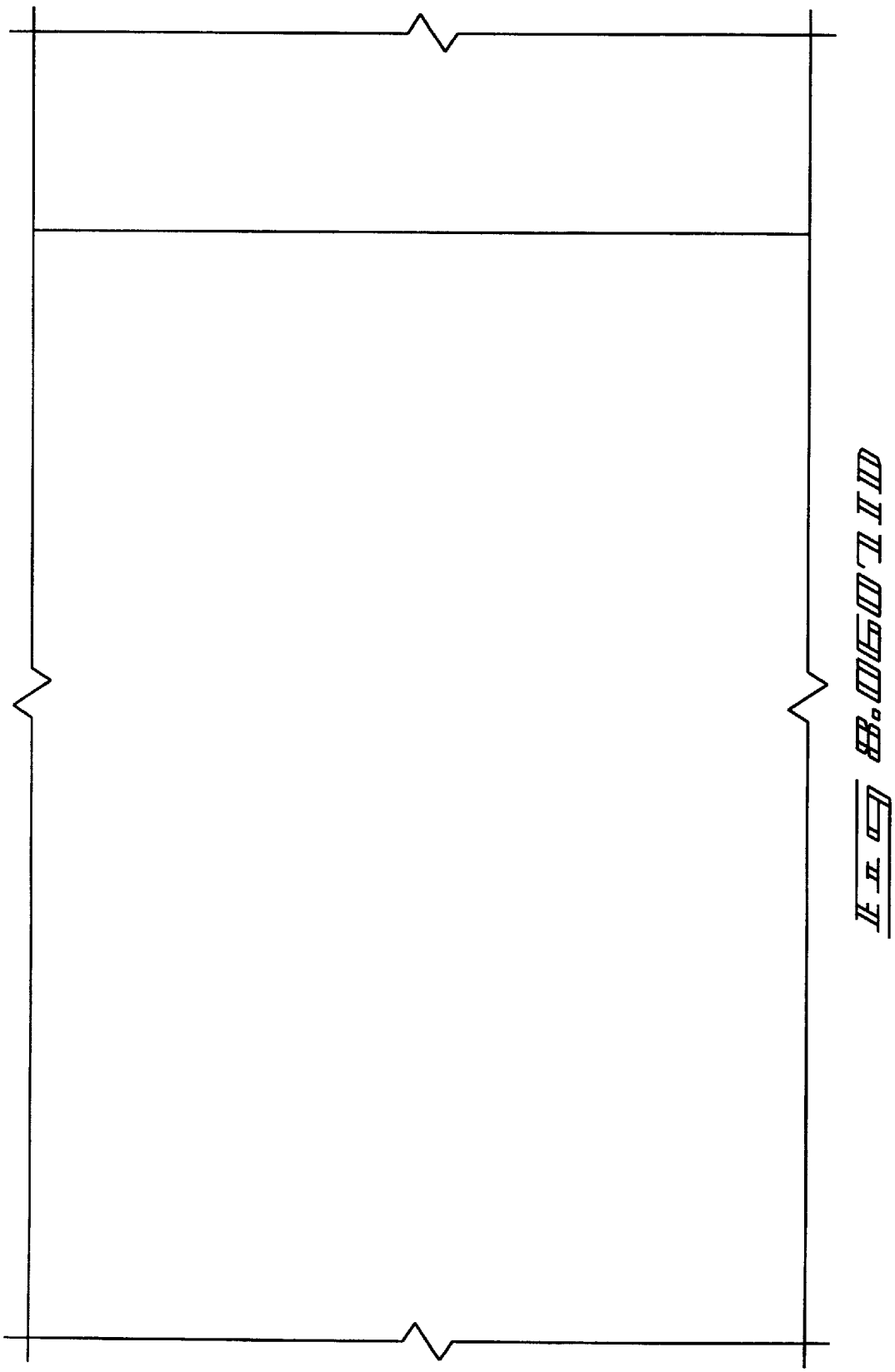


FIG 98,050.11

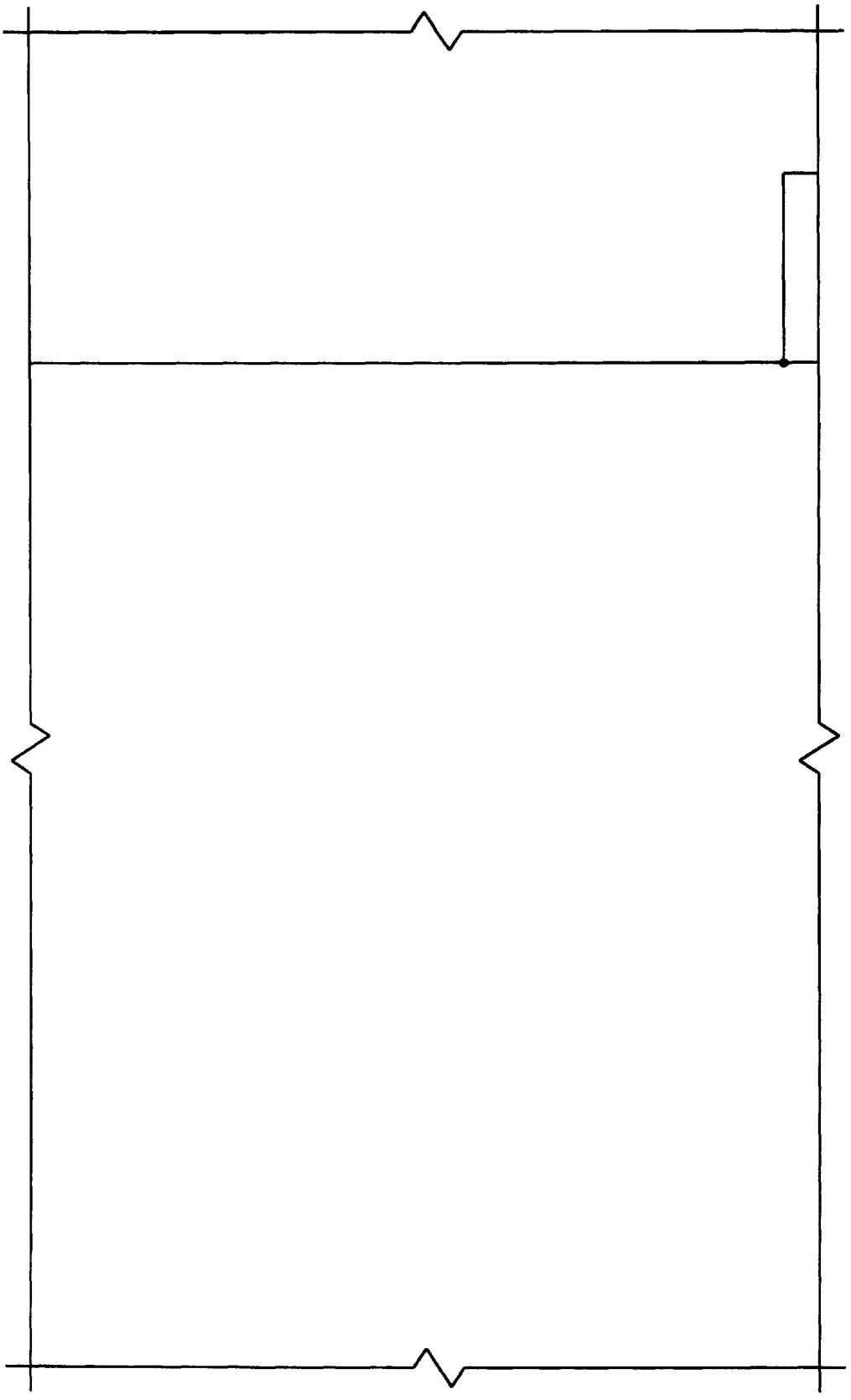


FIG 88.00511E

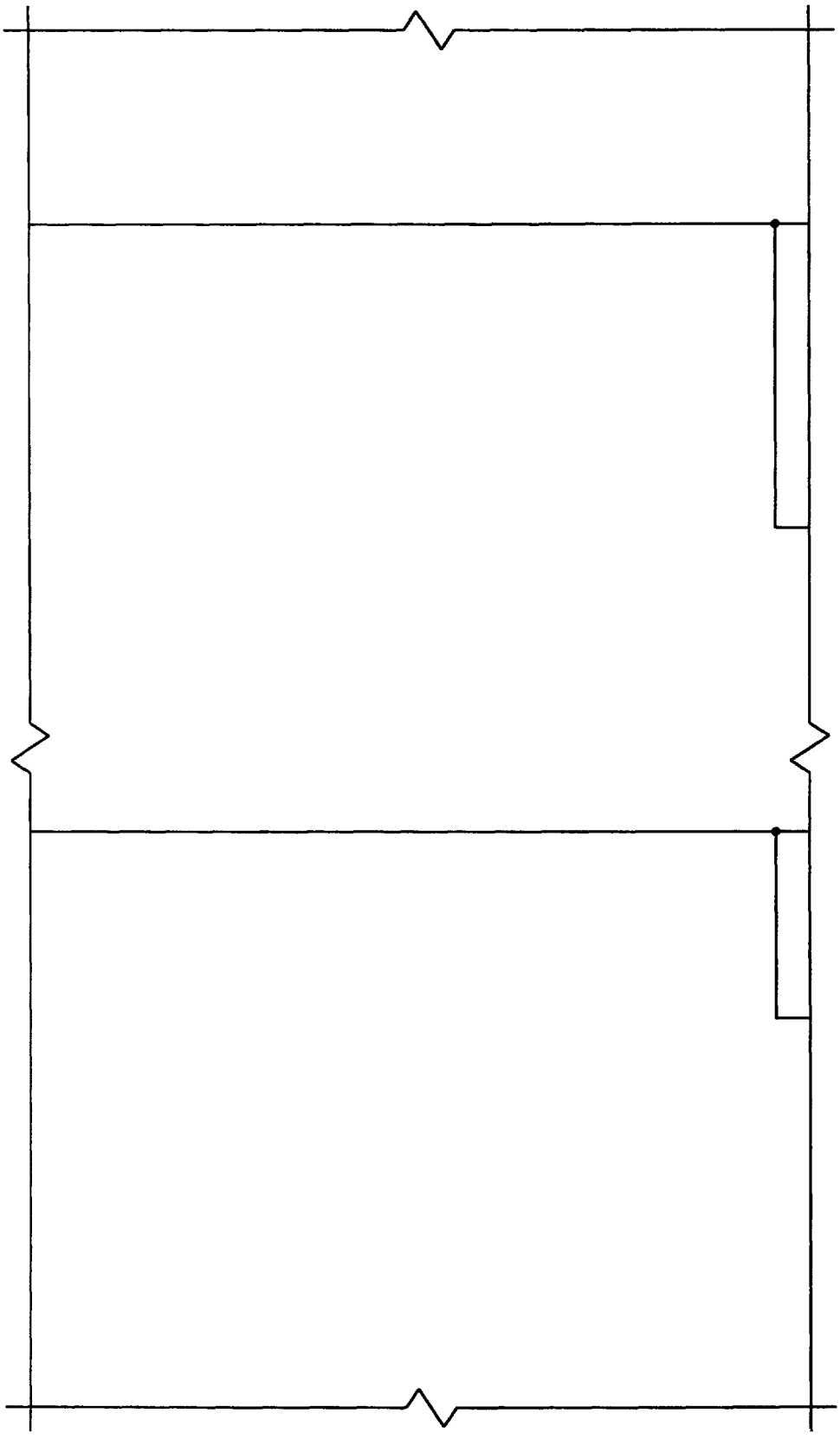


FIG 88.0501F

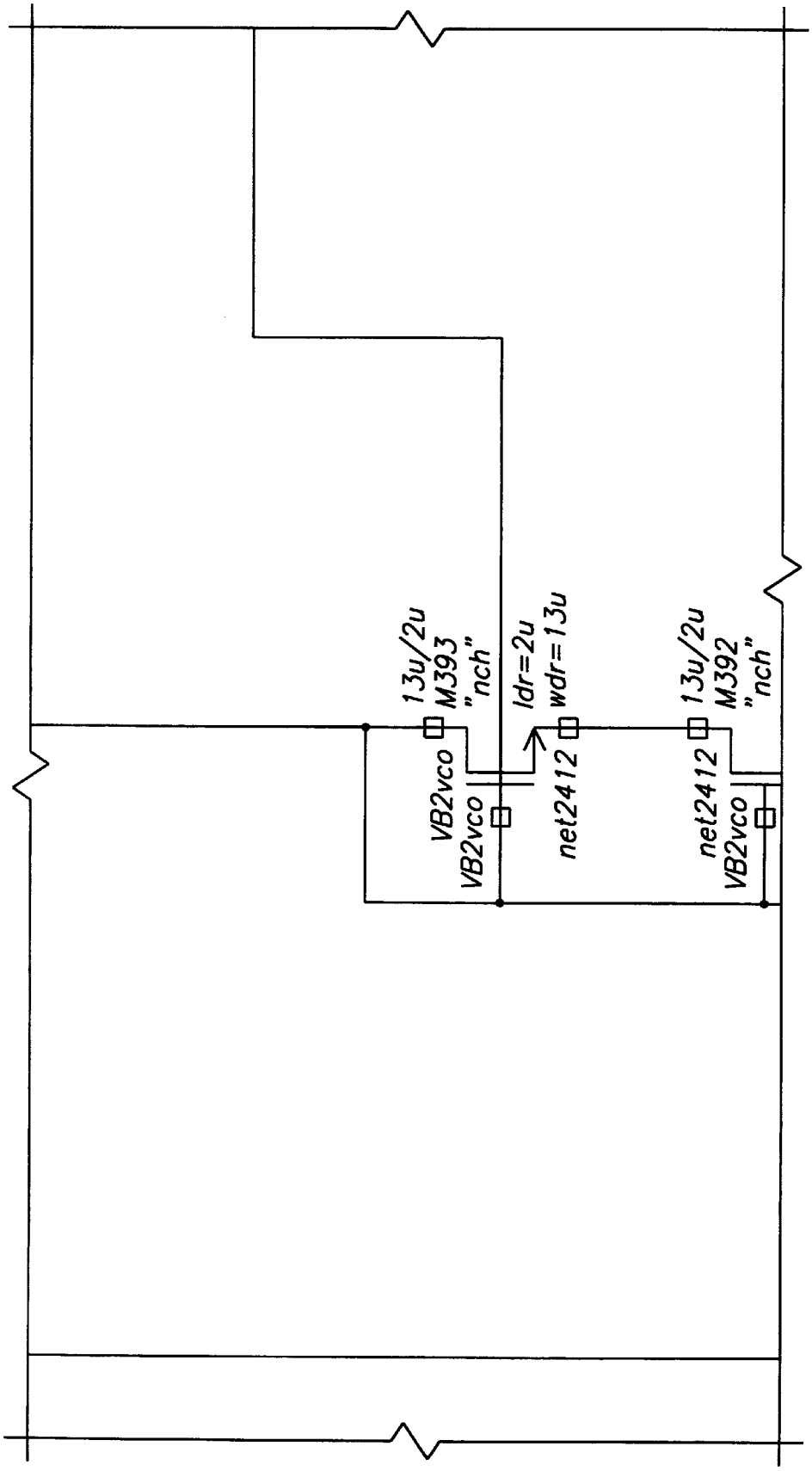


FIG 88.0501US

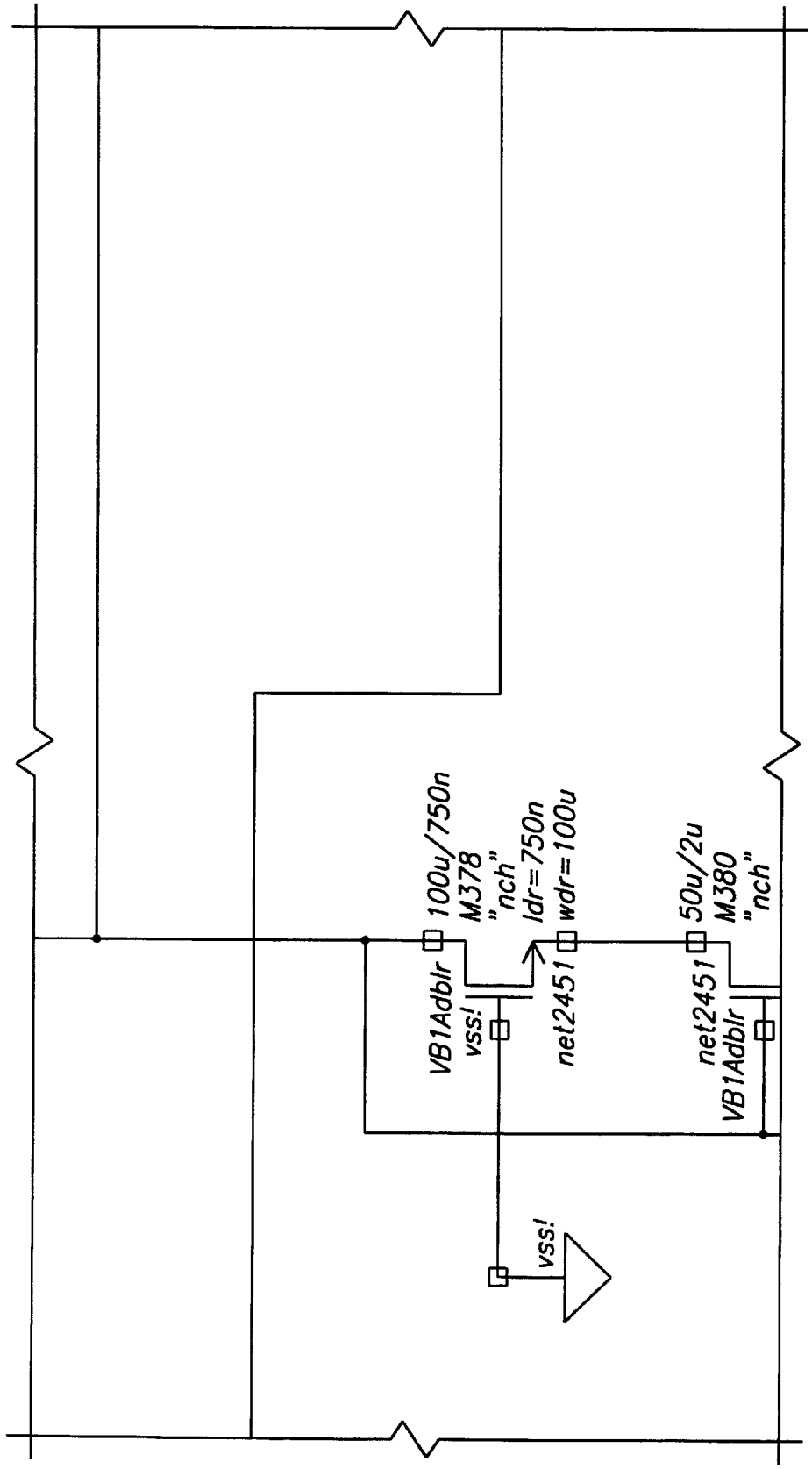

100u/750n
M378
"nch"
ldr=750n
wdr=100u
50u/2u
M380
"nch"
VB1Adblr
vss!
net2451
net2451
VB1Adblr
vss!

Fig 8.0501H

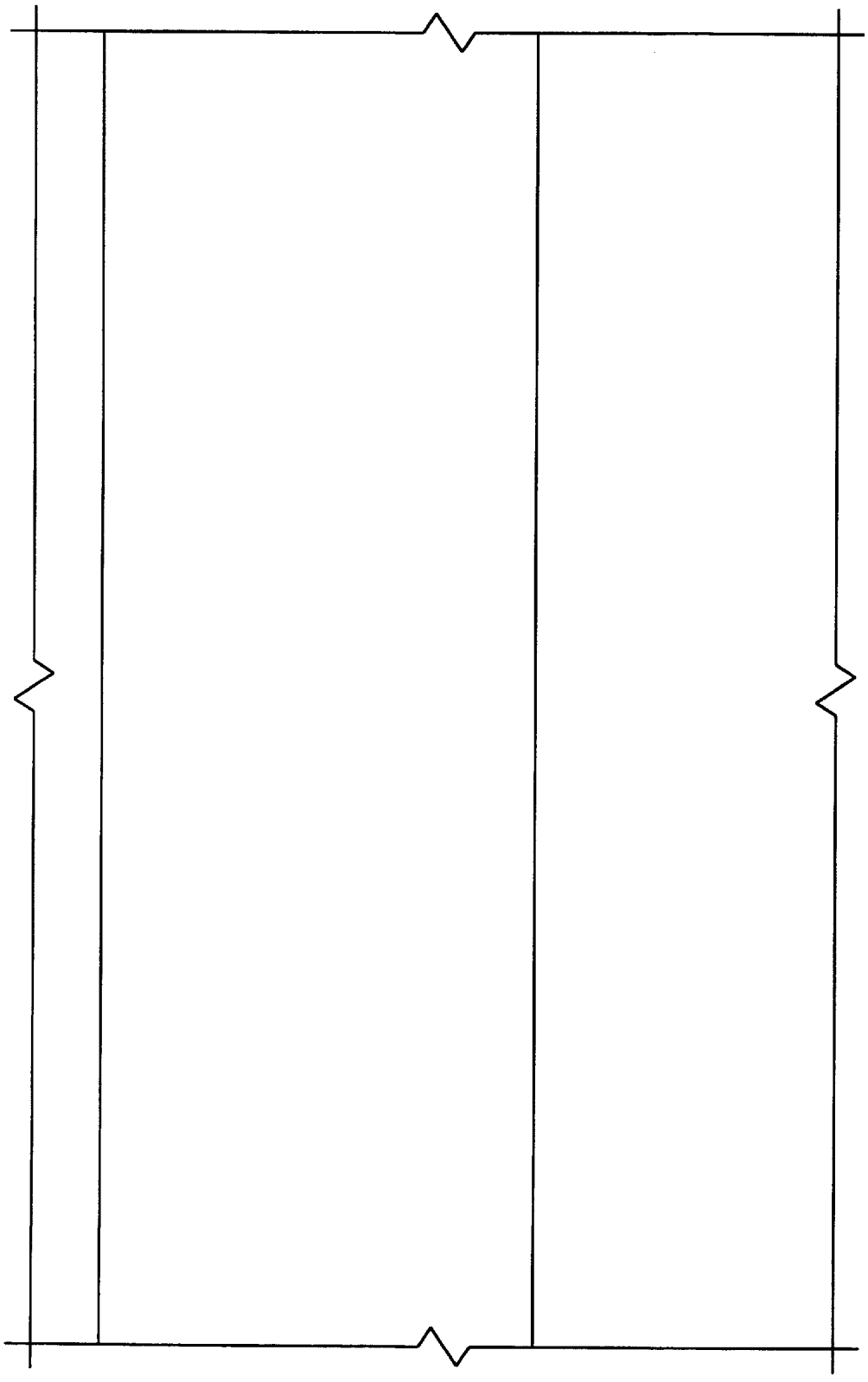


FIG 88,060 II II

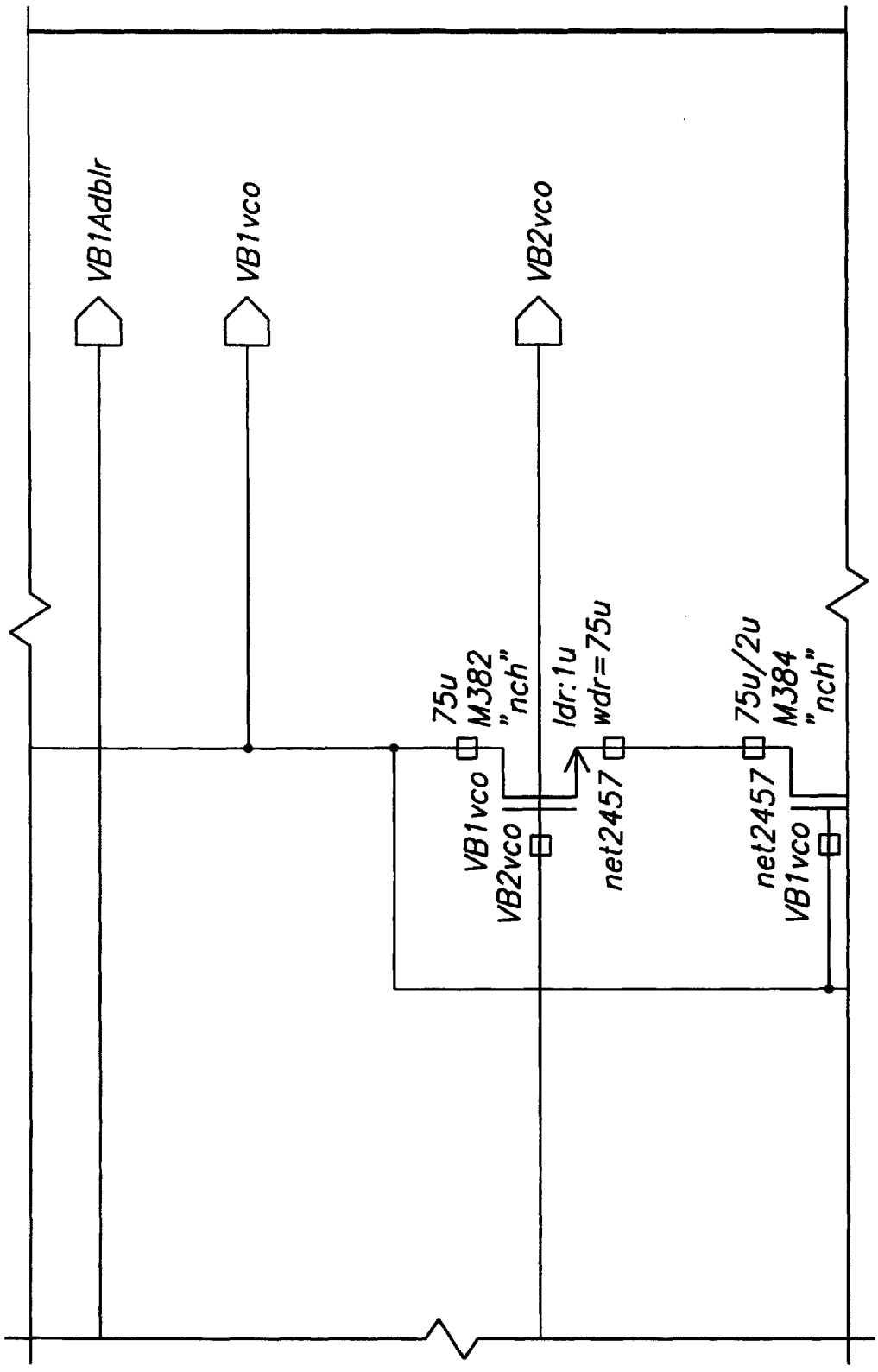
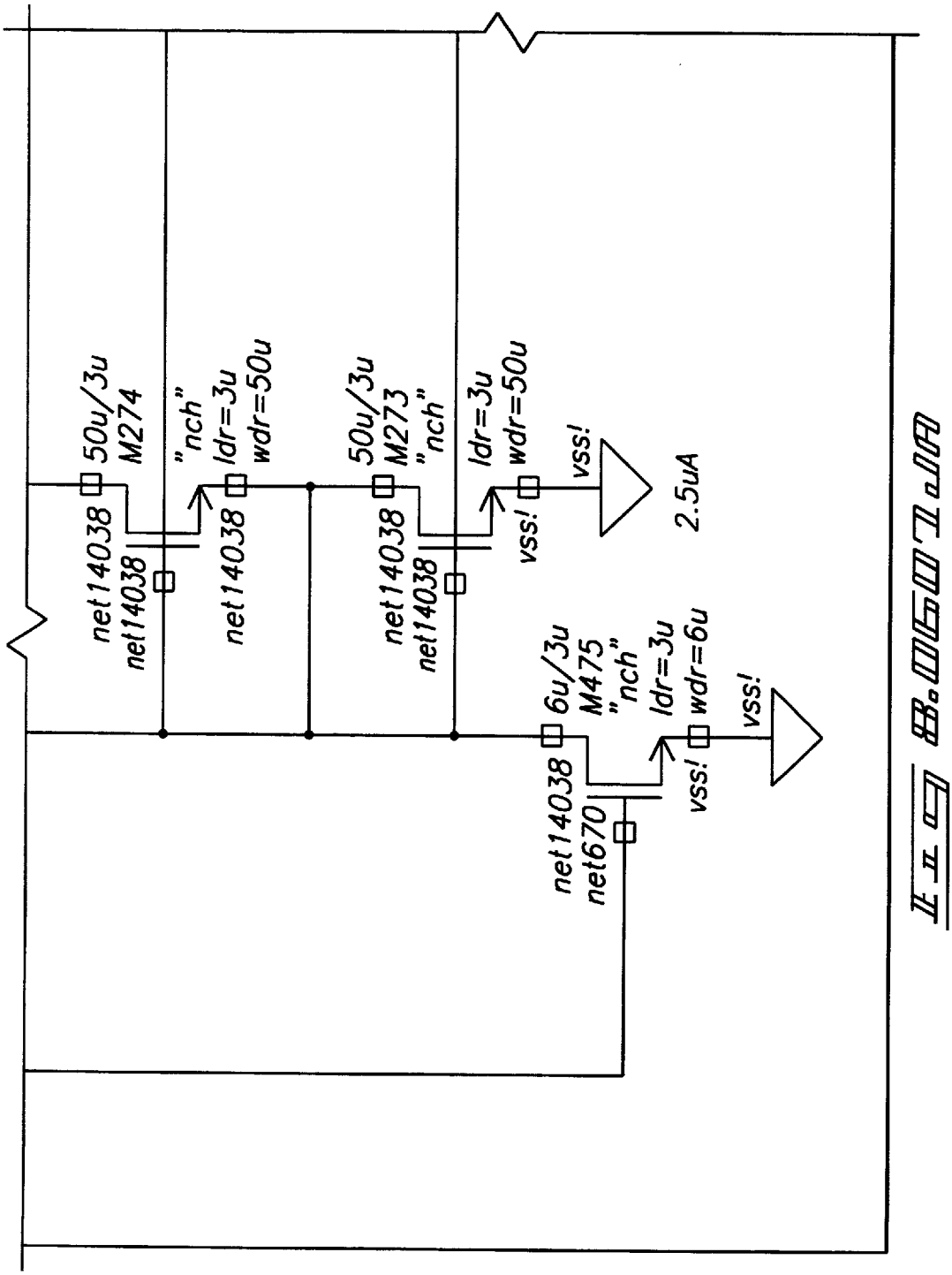
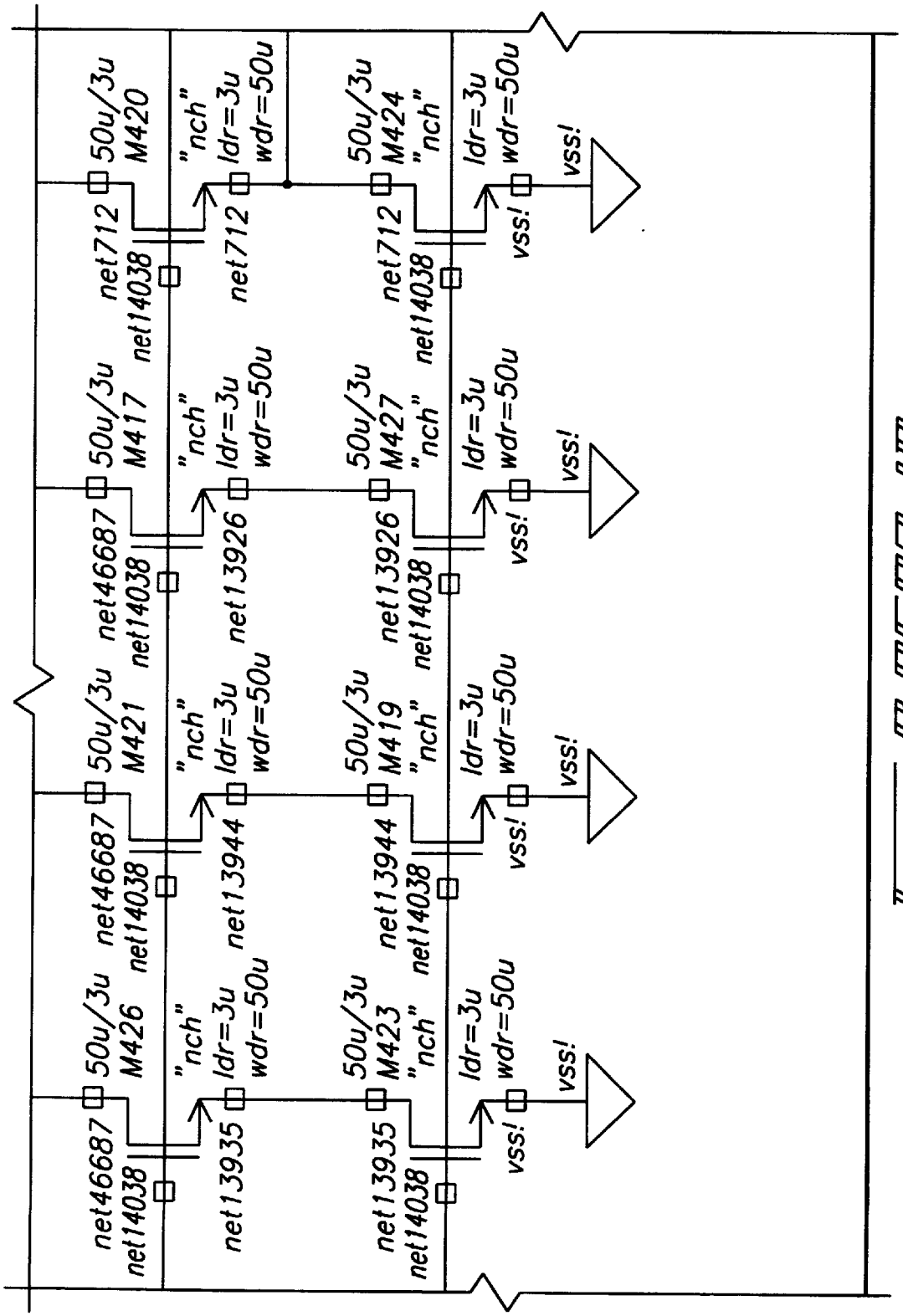

VB1Adblr
VB1vco
VB2vco
75u
M382
"nch"
ldr:1u
wdr=75u
75u/2u
M384
"nch"
VB1vco
VB2vco
net2457
net2457
VB1vco

Fig 88.0050


50u/3u
M274
"nch"
ldr=3u
wdr=50u
net14038
net14038
net14038
50u/3u
M273
"nch"
ldr=3u
wdr=50u
net14038
net14038
vss!
vss!
2.5uA
6u/3u
M475
"nch"
ldr=3u
wdr=6u
net14038
net670
vss!
vss!


50u/3u
M420
"nch"
ldr=3u
wdr=50u
net712
net14038
vss!
50u/3u
M424
"nch"
ldr=3u
wdr=50u
net712
net14038
vss!
50u/3u
M417
"nch"
ldr=3u
wdr=50u
net46687
net14038
net13926
50u/3u
M427
"nch"
ldr=3u
wdr=50u
net13926
net14038
vss!
50u/3u
M421
"nch"
ldr=3u
wdr=50u
net46687
net14038
net13944
50u/3u
M419
"nch"
ldr=3u
wdr=50u
net13944
net14038
vss!
50u/3u
M426
"nch"
ldr=3u
wdr=50u
net46687
net14038
net13935
50u/3u
M423
"nch"
ldr=3u
wdr=50u
net13935
net14038
vss!

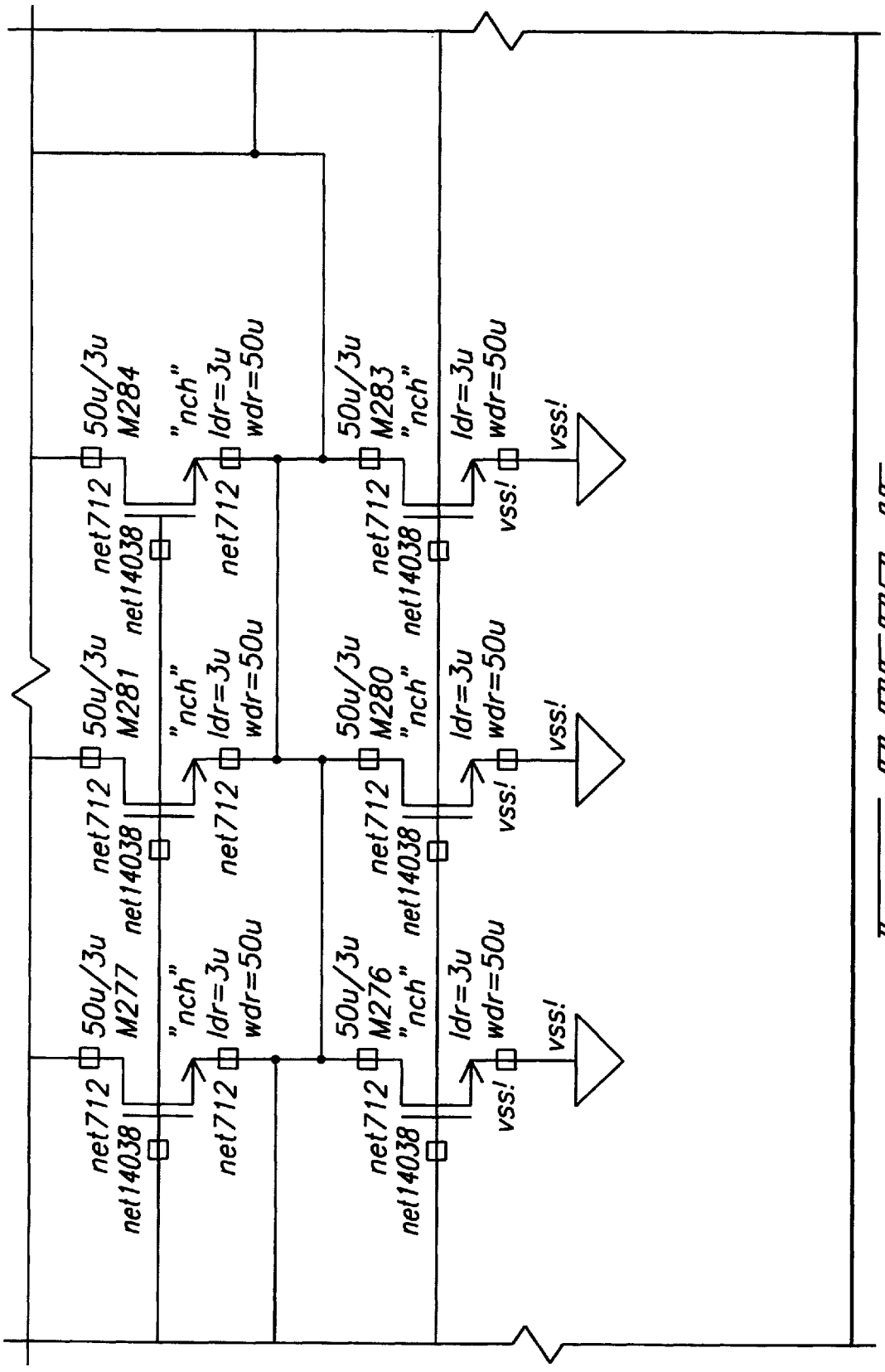

50u/3u
M284
"nch"
ldr=3u
wdr=50u
50u/3u
M283
"nch"
ldr=3u
wdr=50u
vss!
net712
net14038
50u/3u
M281
"nch"
ldr=3u
wdr=50u
50u/3u
M280
"nch"
ldr=3u
wdr=50u
50u/3u
M277
"nch"
ldr=3u
wdr=50u
50u/3u
M276
"nch"
ldr=3u
wdr=50u

FIG. 8,050,A

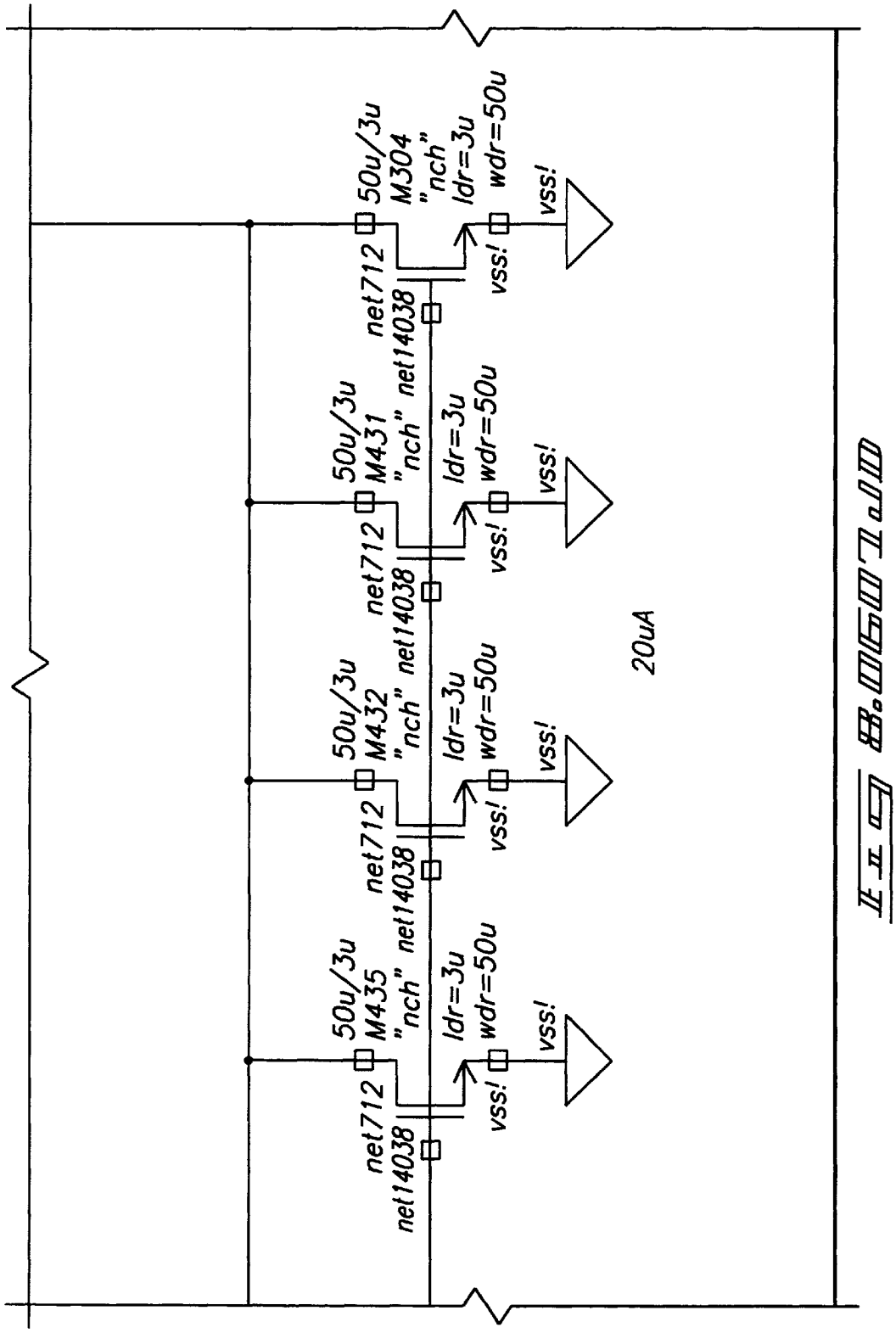

50u/3u
M304
"nch"
ldr=3u
wdr=50u
vss!
net712
net14038
50u/3u
M431
"nch"
ldr=3u
wdr=50u
vss!
net712
net14038
50u/3u
M432
"nch"
ldr=3u
wdr=50u
vss!
net712
net14038
50u/3u
M435
"nch"
ldr=3u
wdr=50u
vss!
net712
net14038
20uA

FIG. 88.0050

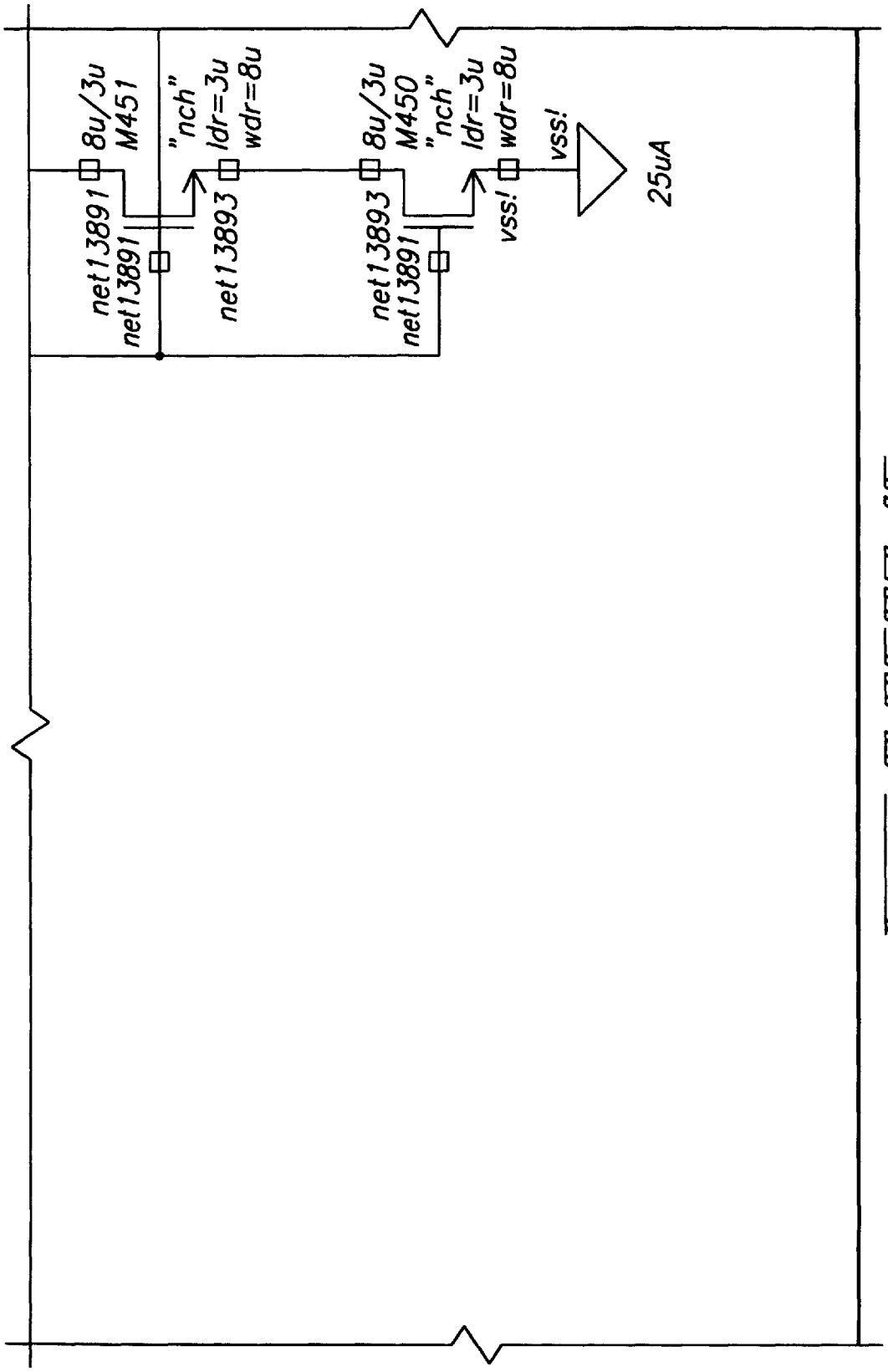
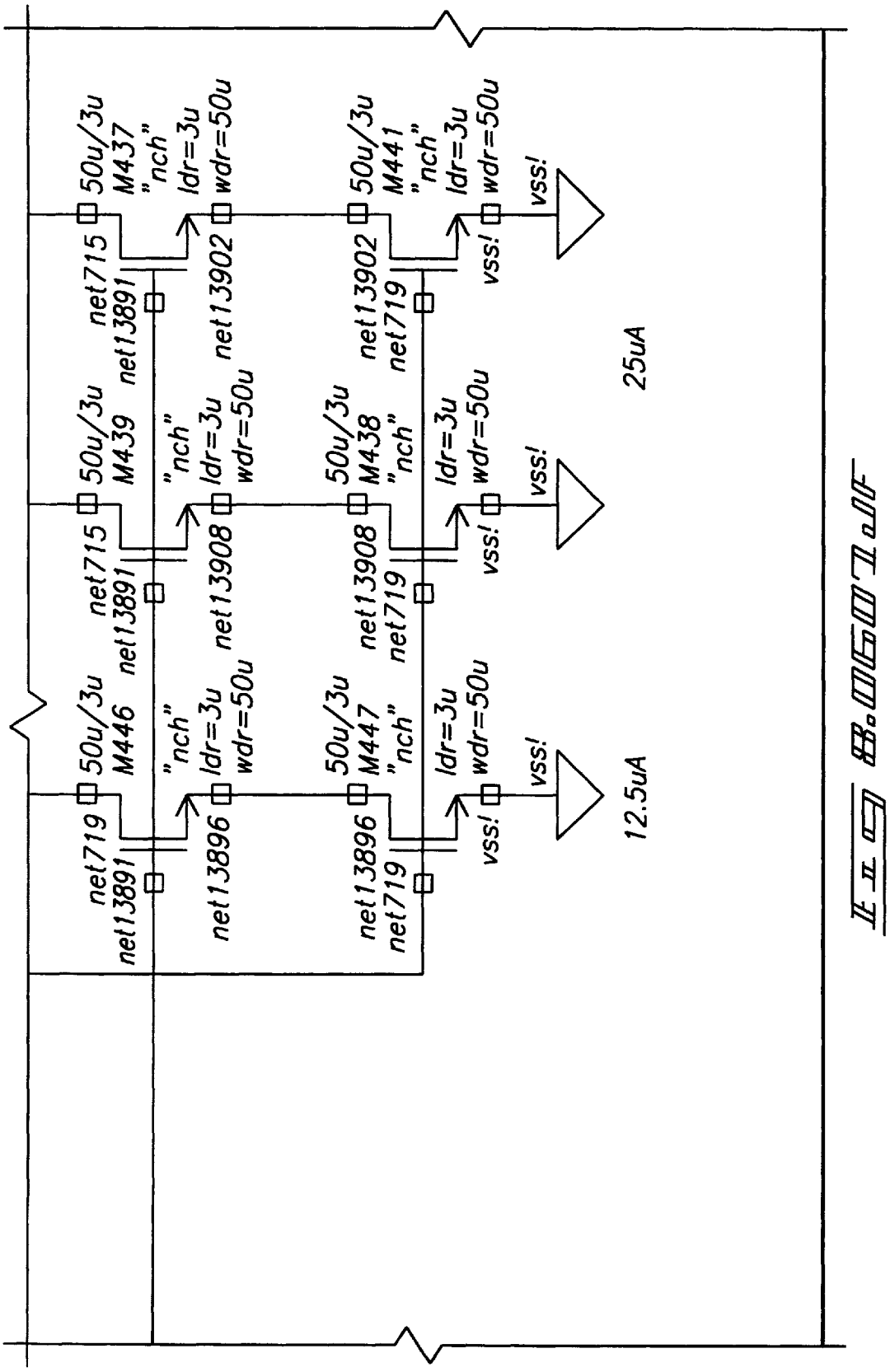

8u/3u
M451
"nch"
ldr=3u
wdr=8u
8u/3u
M450
"nch"
ldr=3u
wdr=8u
vss!
25uA
net13891
net13891
net13893
net13893
net13891
vss!

FIG. 88.0650.0


50u/3u
M437
"nch"
ldr=3u
wdr=50u
net715
net13891
net13902
50u/3u
M441
"nch"
ldr=3u
wdr=50u
vss!
net719
25uA
50u/3u
M439
"nch"
ldr=3u
wdr=50u
net13908
50u/3u
M438
"nch"
ldr=3u
wdr=50u
50u/3u
M446
"nch"
ldr=3u
wdr=50u
net13896
50u/3u
M447
"nch"
ldr=3u
wdr=50u
12.5uA

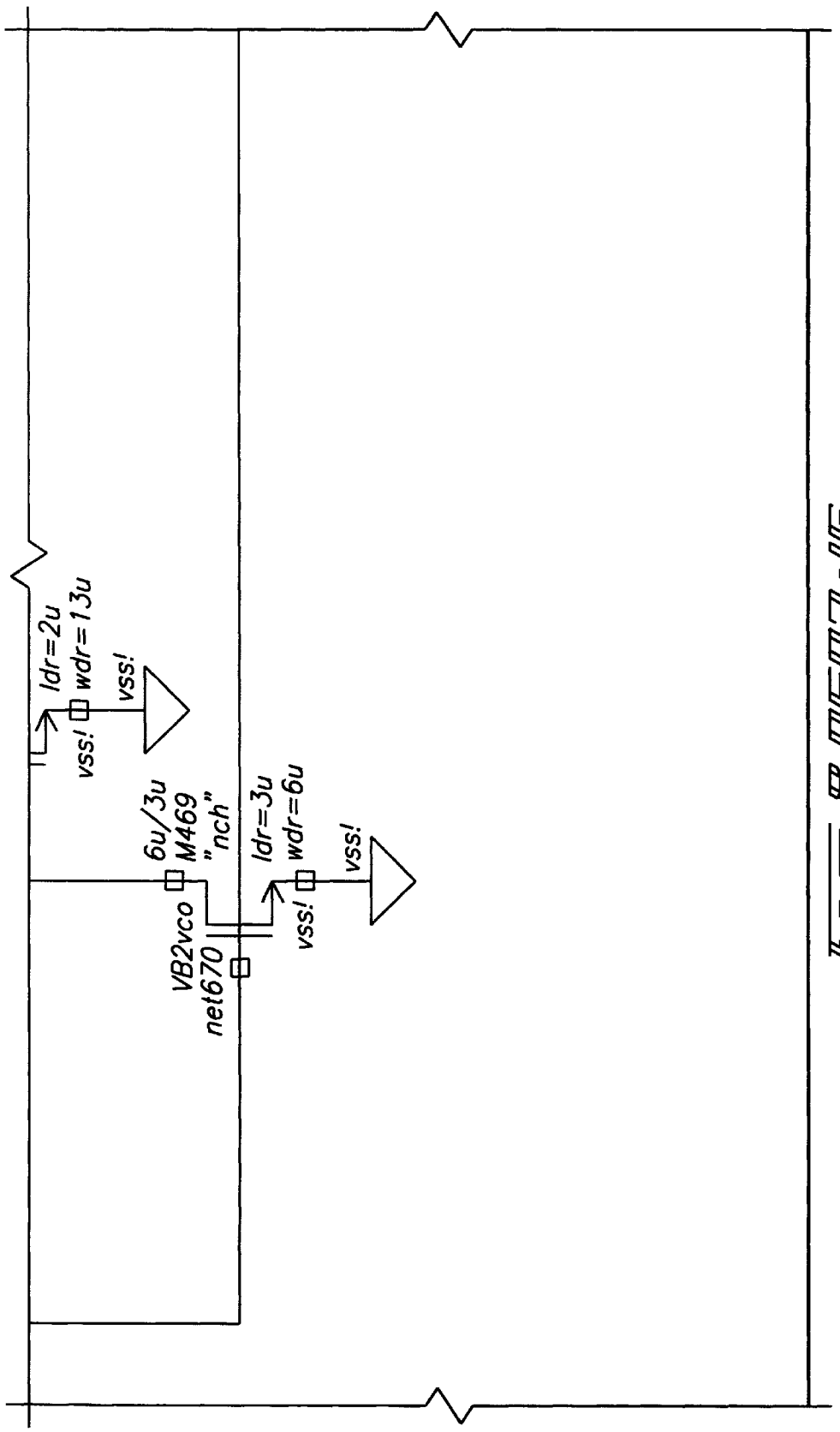

ldr=2u
wdr=1.3u
vss!
vss!
6u/3u
M469
"nch"
ldr=3u
wdr=6u
vss!
vss!
VB2vco
net670

FIG 88.0600

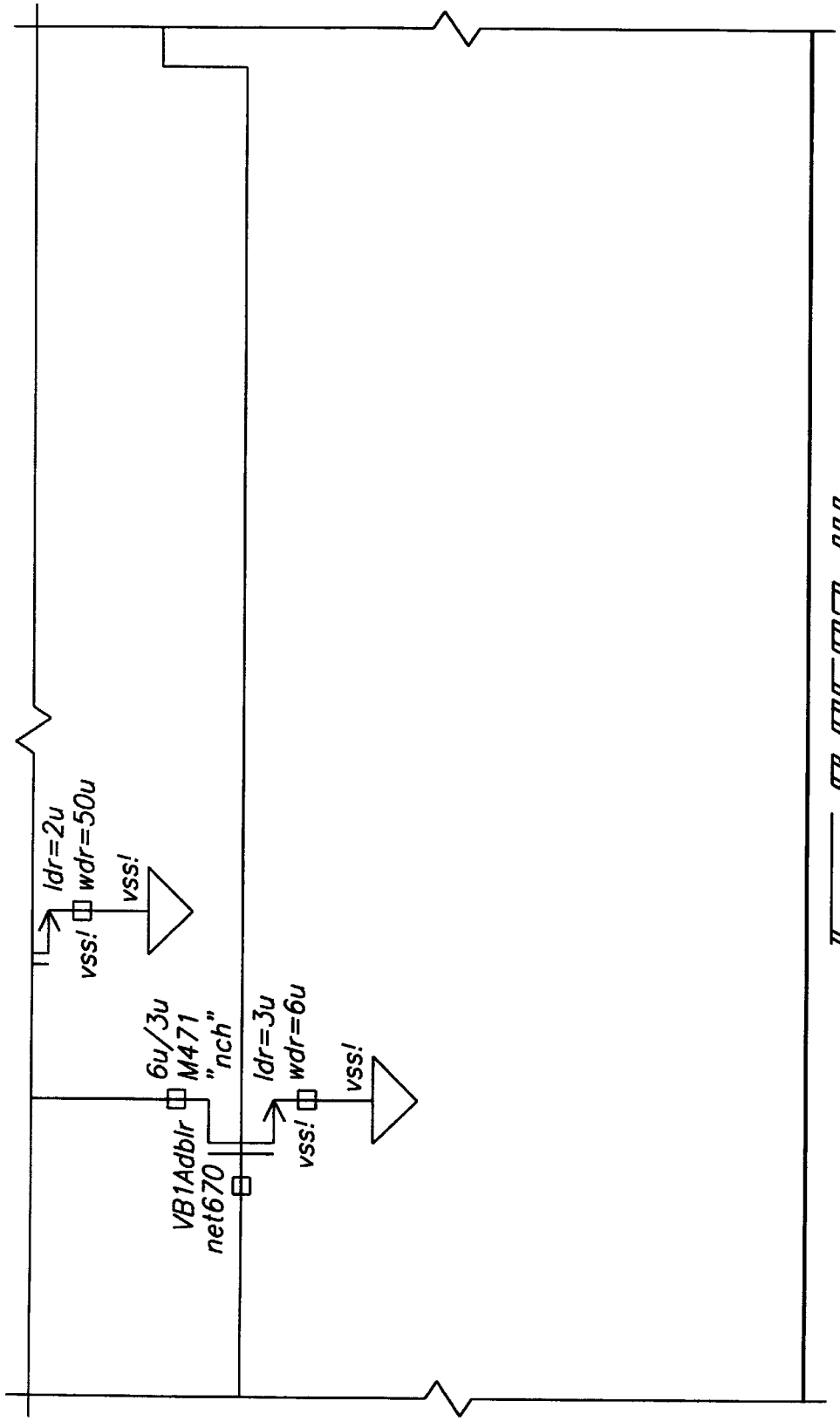


FIG. 8,050
ldr=2u
wdr=50u
vss!
vss!
6u/3u
M471
"nch"
ldr=3u
wdr=6u
vss!
vss!
VB1Adblr
net670

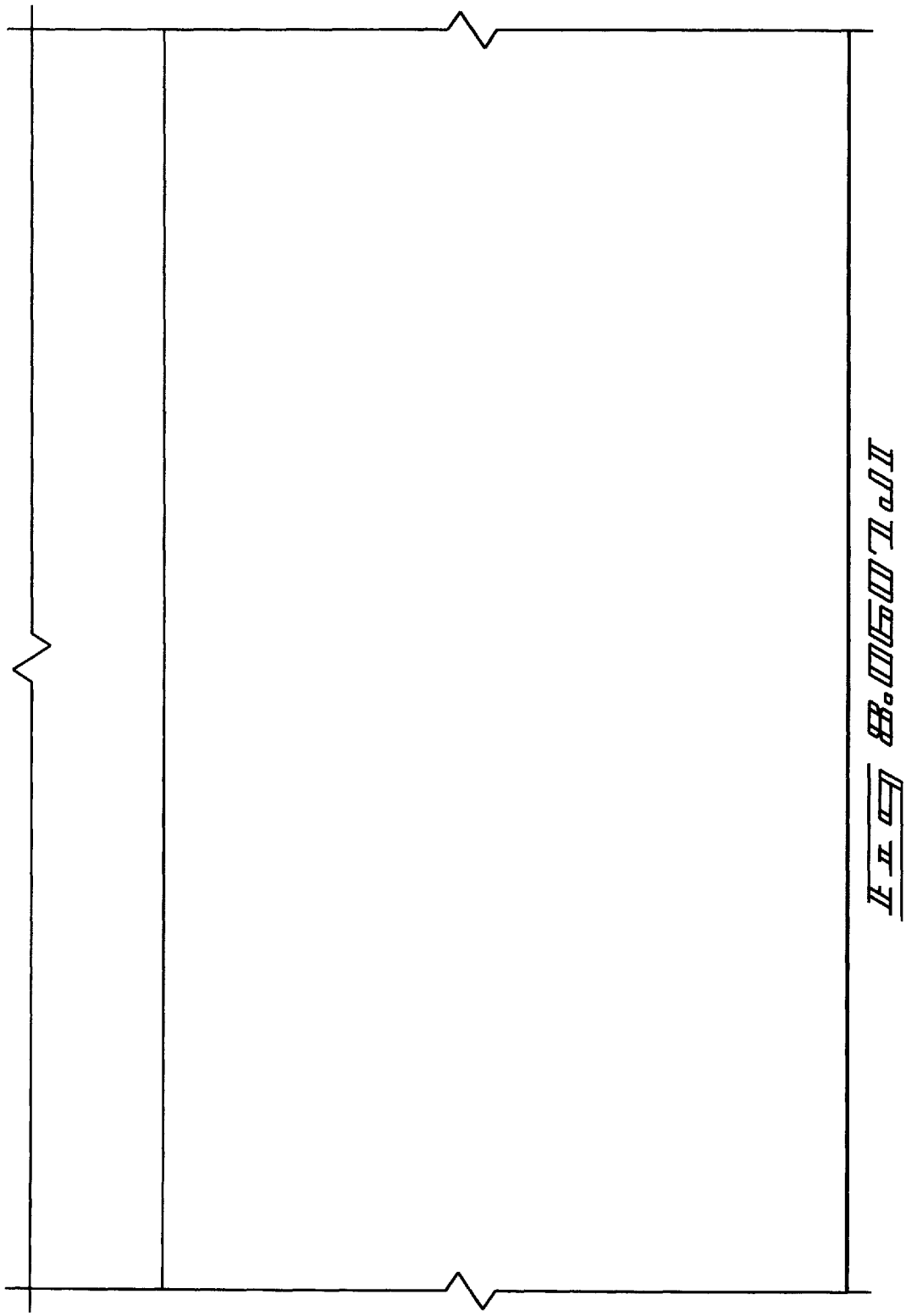


FIG 8,050

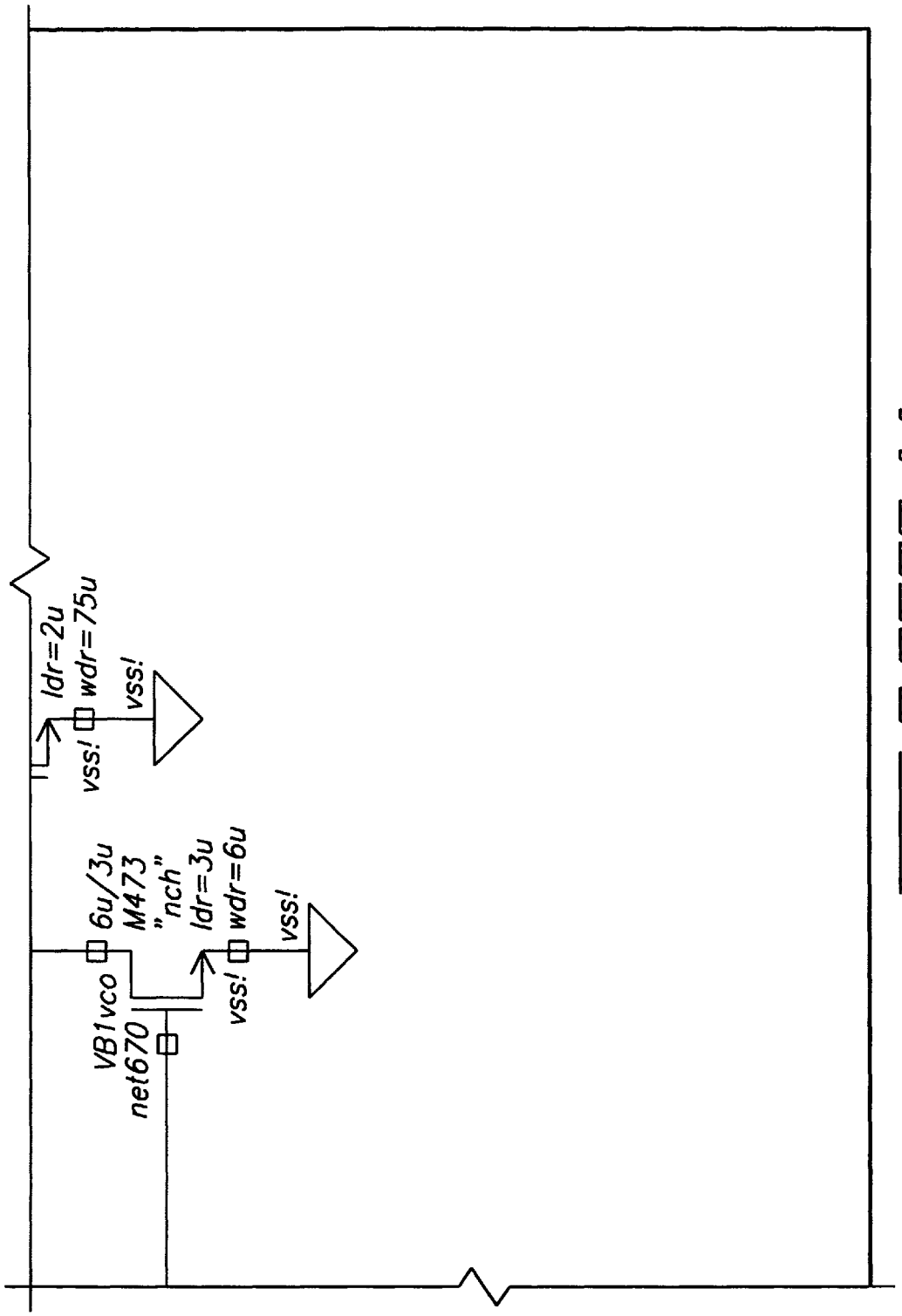

ldr=2u
wdr=75u
vss!
vss!
6u/3u
M473
"nch"
ldr=3u
wdr=6u
vss!
vss!
VB1vco
net670

FIG. 8.0590

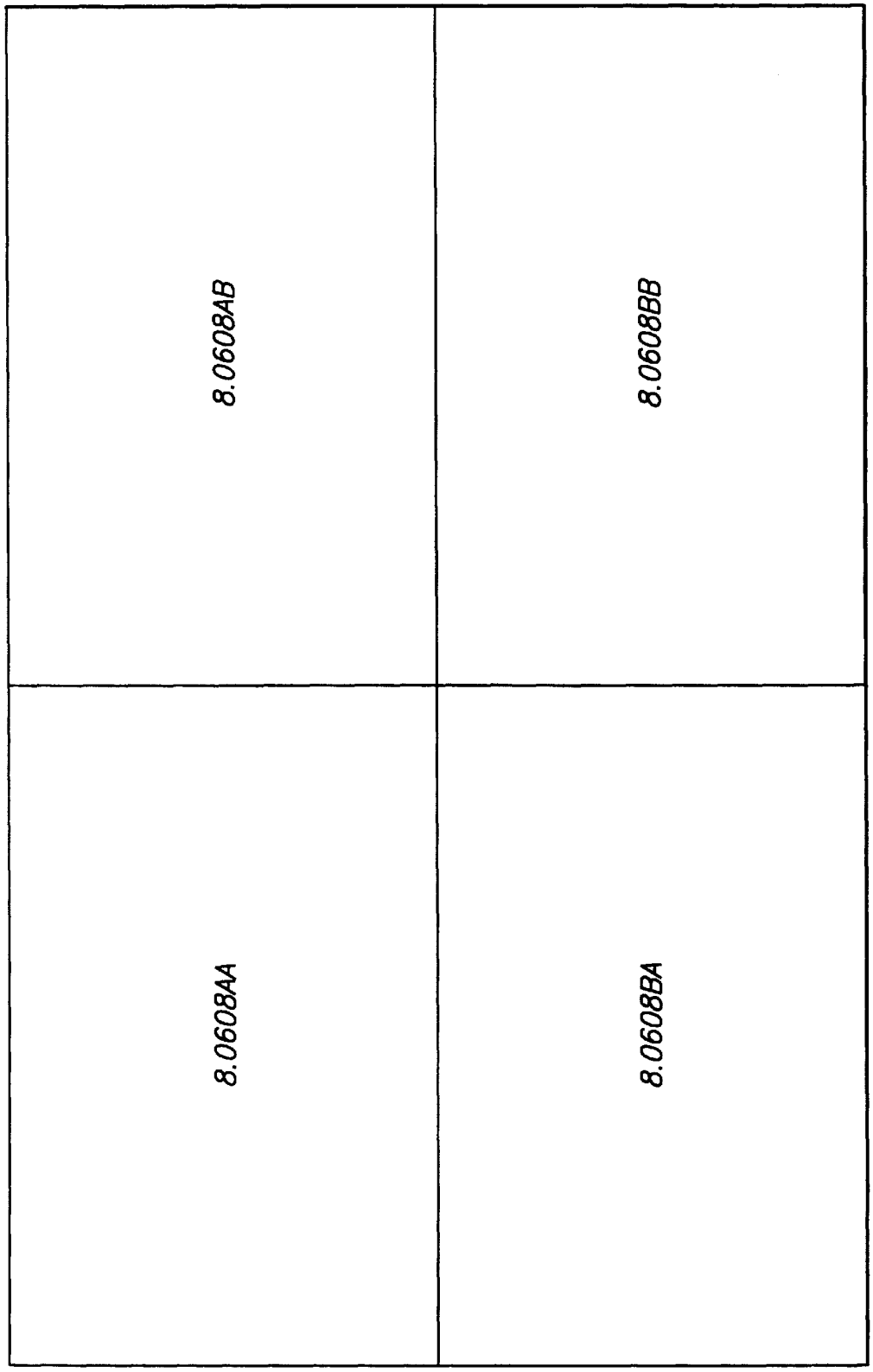


FIG 8.0608

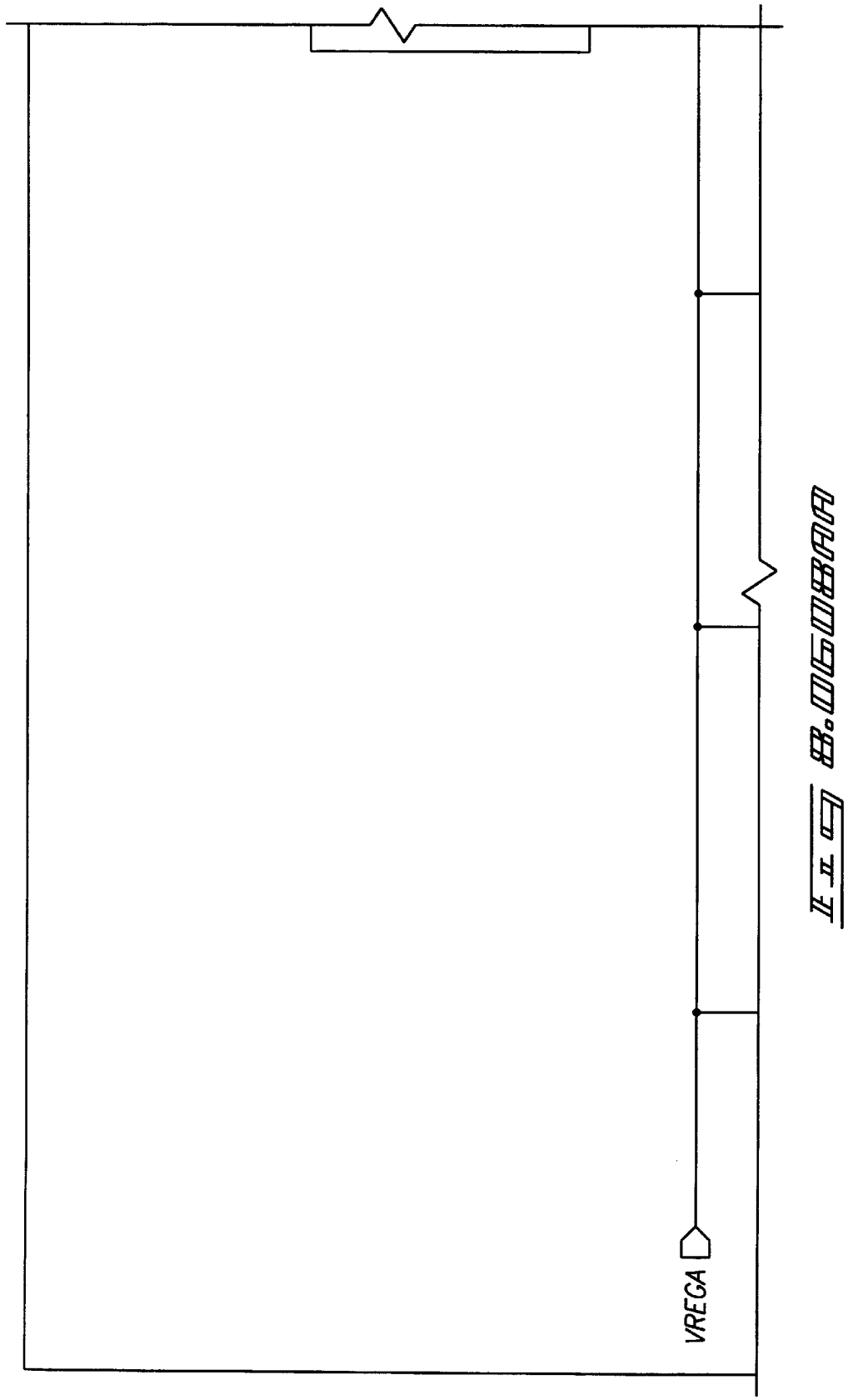
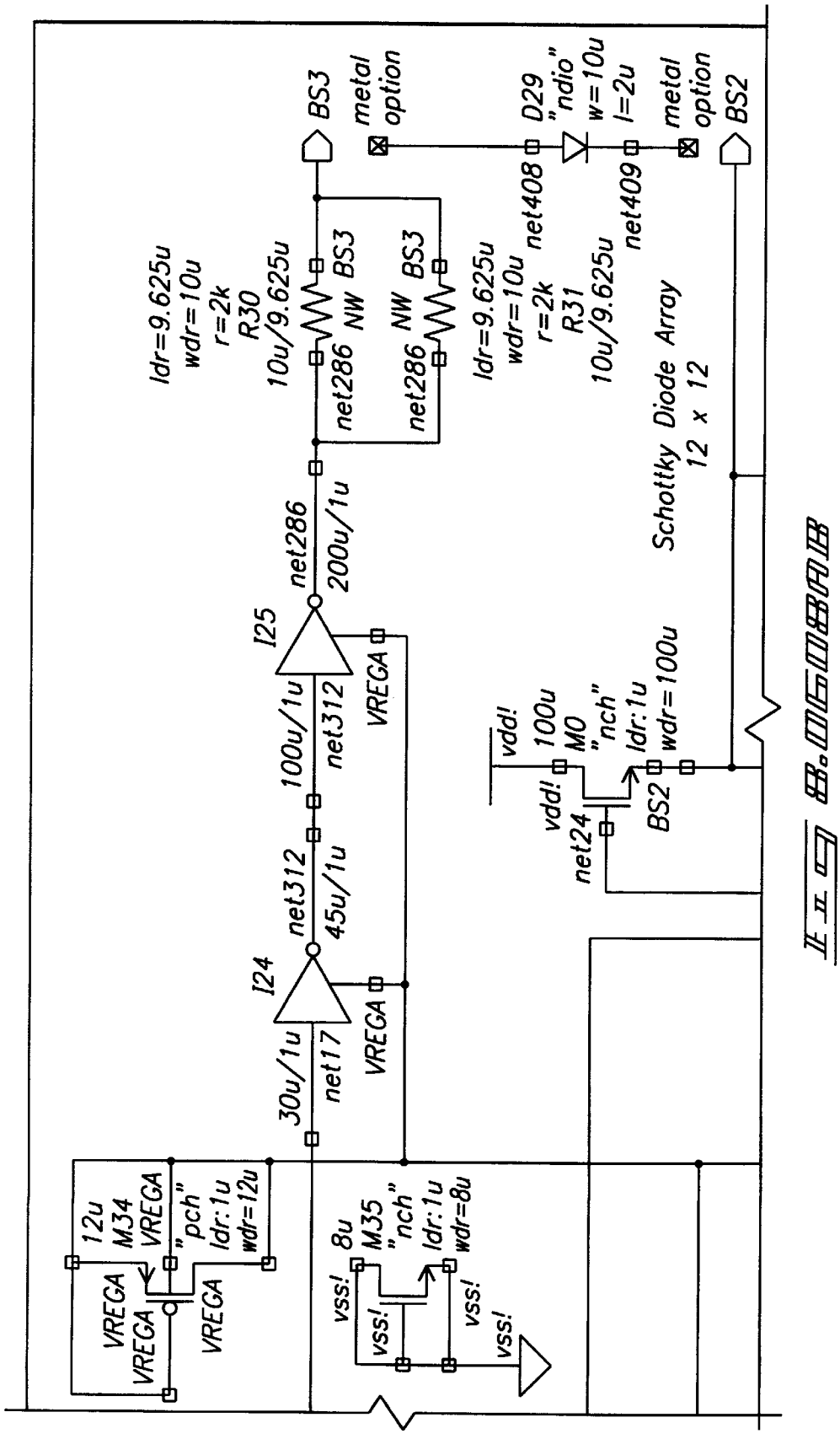


FIG. 88.
VREGA


BS3
metal
option
D29
"ndio"
w=10u
l=2u
metal
option
BS2
ldr=9.625u
wdr=10u
r=2k
R30
10u/9.625u
net286
NW
BS3
net286
NW
BS3
ldr=9.625u
wdr=10u
net408
r=2k
R31
10u/9.625u
net409
Schottky Diode Array
12 x 12
I25
net286
200u/1u
100u/1u
net312
VREGA
vdd!
100u
M0
"nch"
ldr:1u
wdr=100u
BS2
net24
I24
net312
45u/1u
30u/1u
net17
VREGA
12u
M34
VREGA
"pch"
ldr:1u
wdr=12u
VREGA
VREGA
VREGA
8u
M35
"nch"
ldr:1u
wdr=8u
vss!
vss!
vss!
vss!

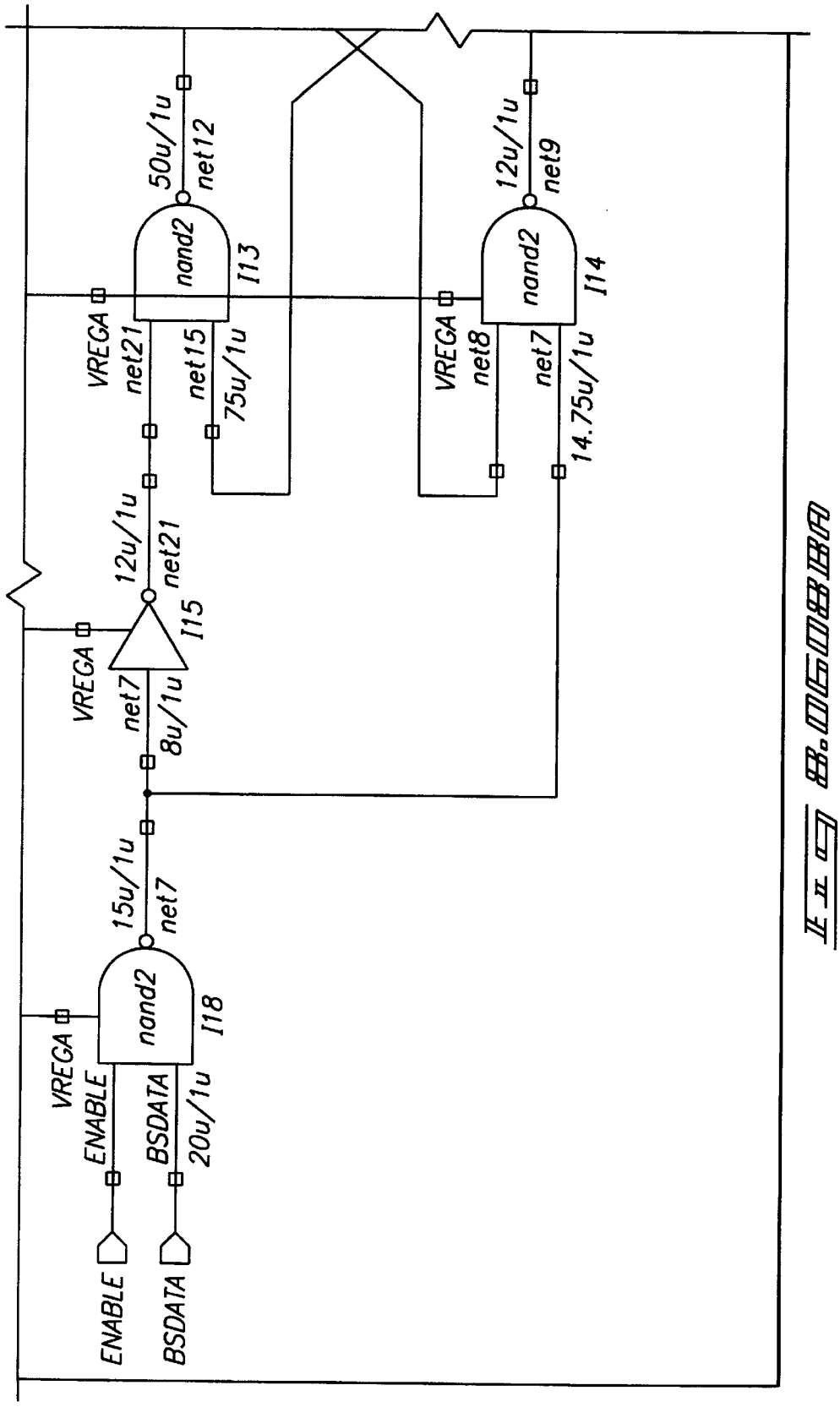
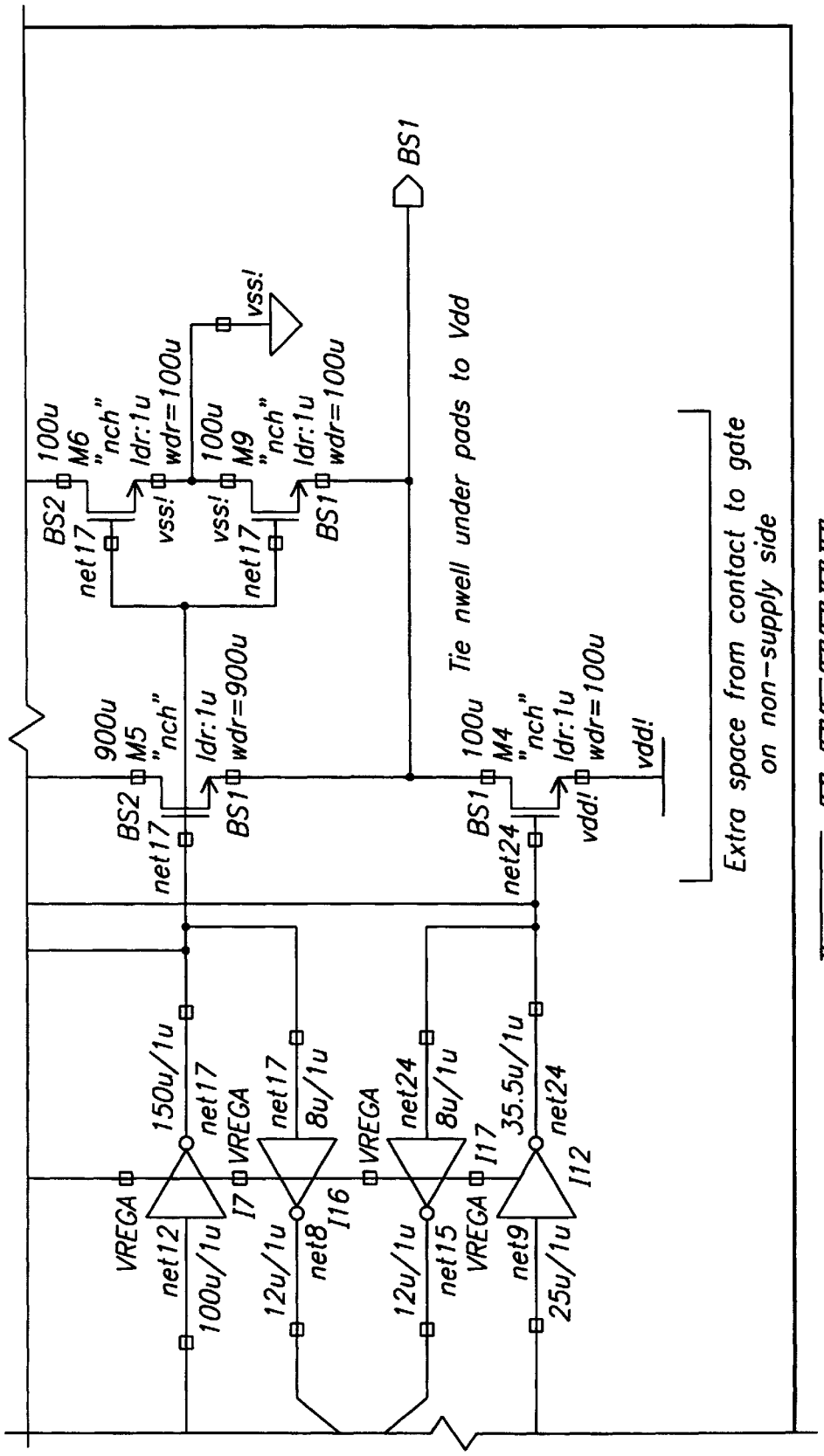


FIG 88.00598A


BS1
Tie nwell under pads to Vdd
Extra space from contact to gate
on non-supply side
100u M6 "nch" ldr:1u wdr=100u
BS2 net17
vss!
100u M9 "nch" ldr:1u wdr=100u
vss!
net17
BS1
900u M5 "nch" ldr:1u wdr=900u
BS2 net17
BS1
100u M4 "nch" ldr:1u wdr=100u
BS1 net24
vdd!
vdd!
150u/1u net17 VREGA I7
8u/1u net17 VREGA I16
8u/1u net24 VREGA I17
35.5u/1u net24 I12
VREGA net12 100u/1u
12u/1u net8
12u/1u net15
VREGA net9 25u/1u

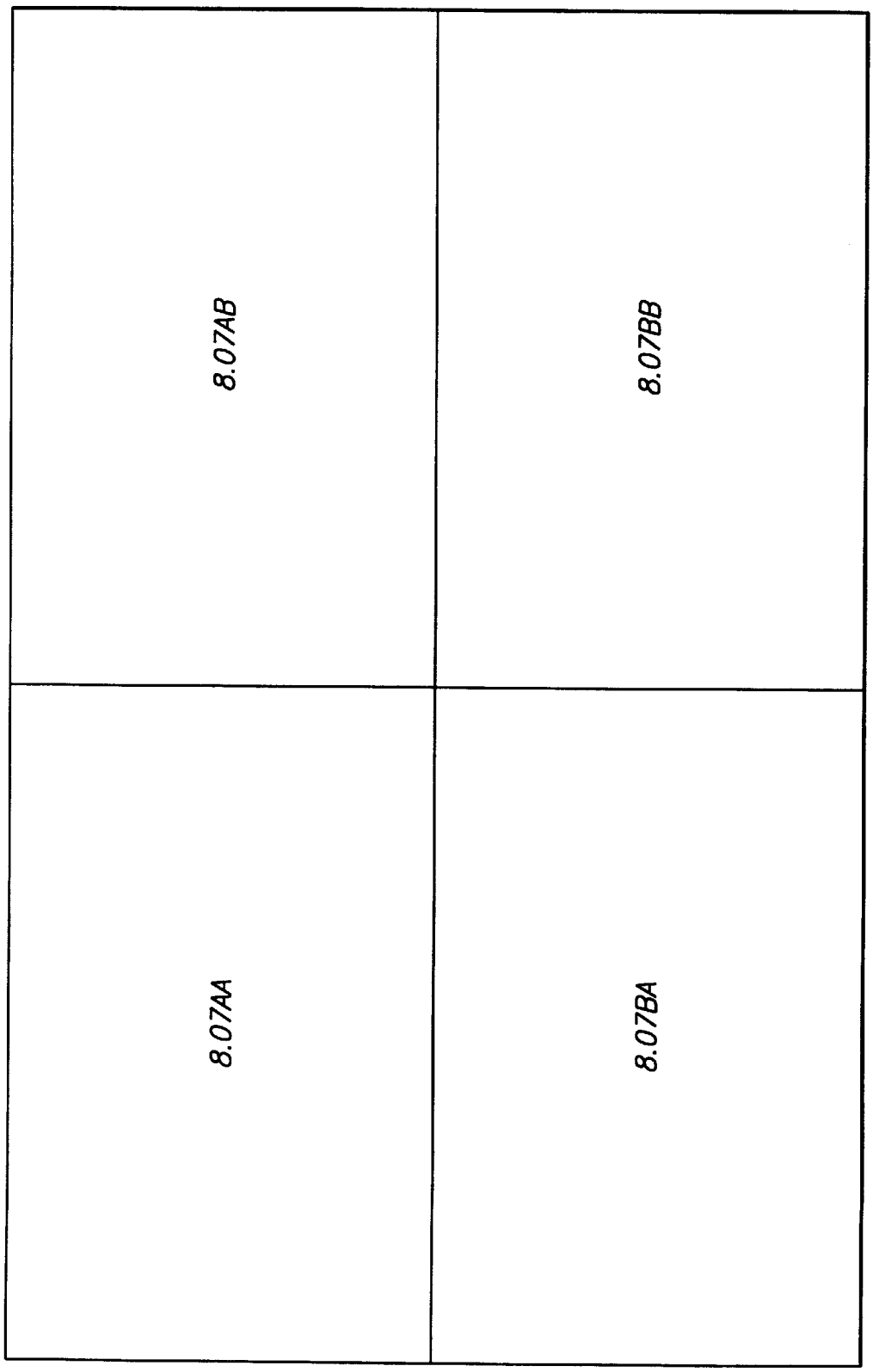
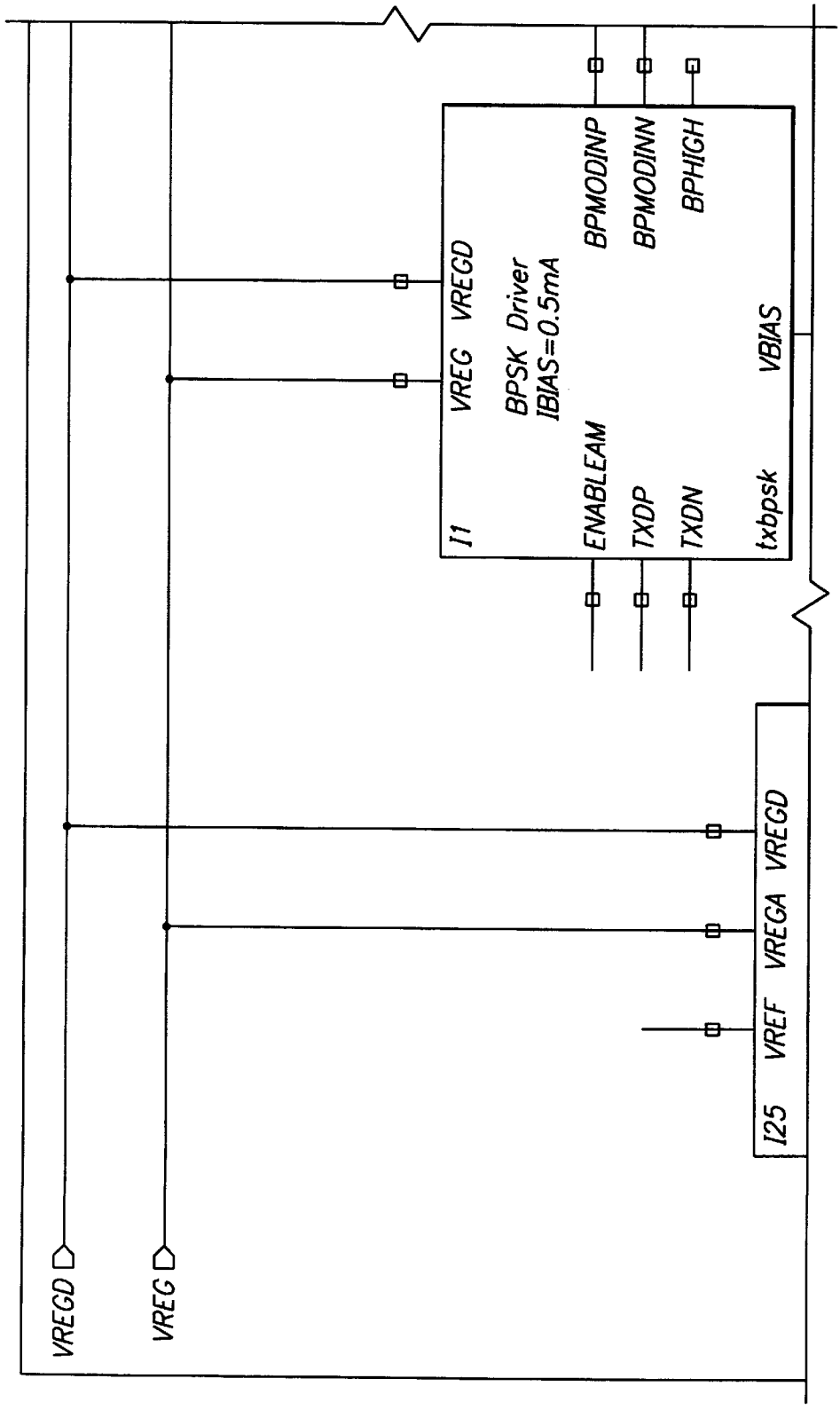
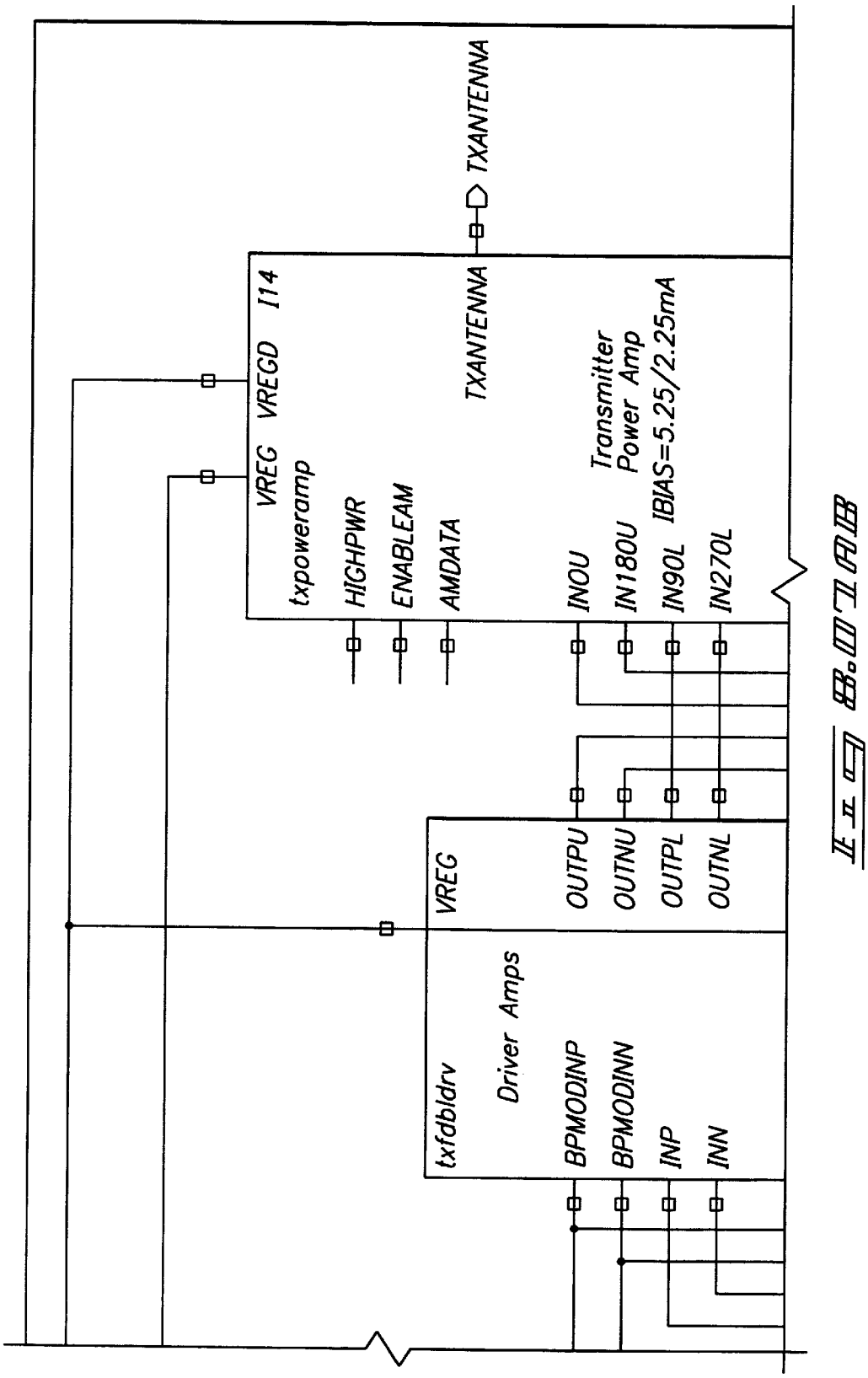


FIG 8.07L


VREGD
VREG
I25
VREF
VREGA
VREGD
I1
ENABLEAM
TXDP
TXDN
txbpsk
VREG
VREGD
BPSK Driver
IBIAS=0.5mA
BPMODINP
BPMODINN
BPHIGH
VBIAS


TXANTENNA
VREG VREGD I14
txpoweramp
HIGHPWR
ENABLEAM
AMDATA
TXANTENNA
Transmitter Power Amp
IBIAS=5.25/2.25mA
INOU
IN180U
IN90L
IN270L
VREG
OUTPU
OUTNU
OUTPL
OUTNL
txfdbldrv
Driver Amps
BPMODINP
BPMODINN
INP
INN

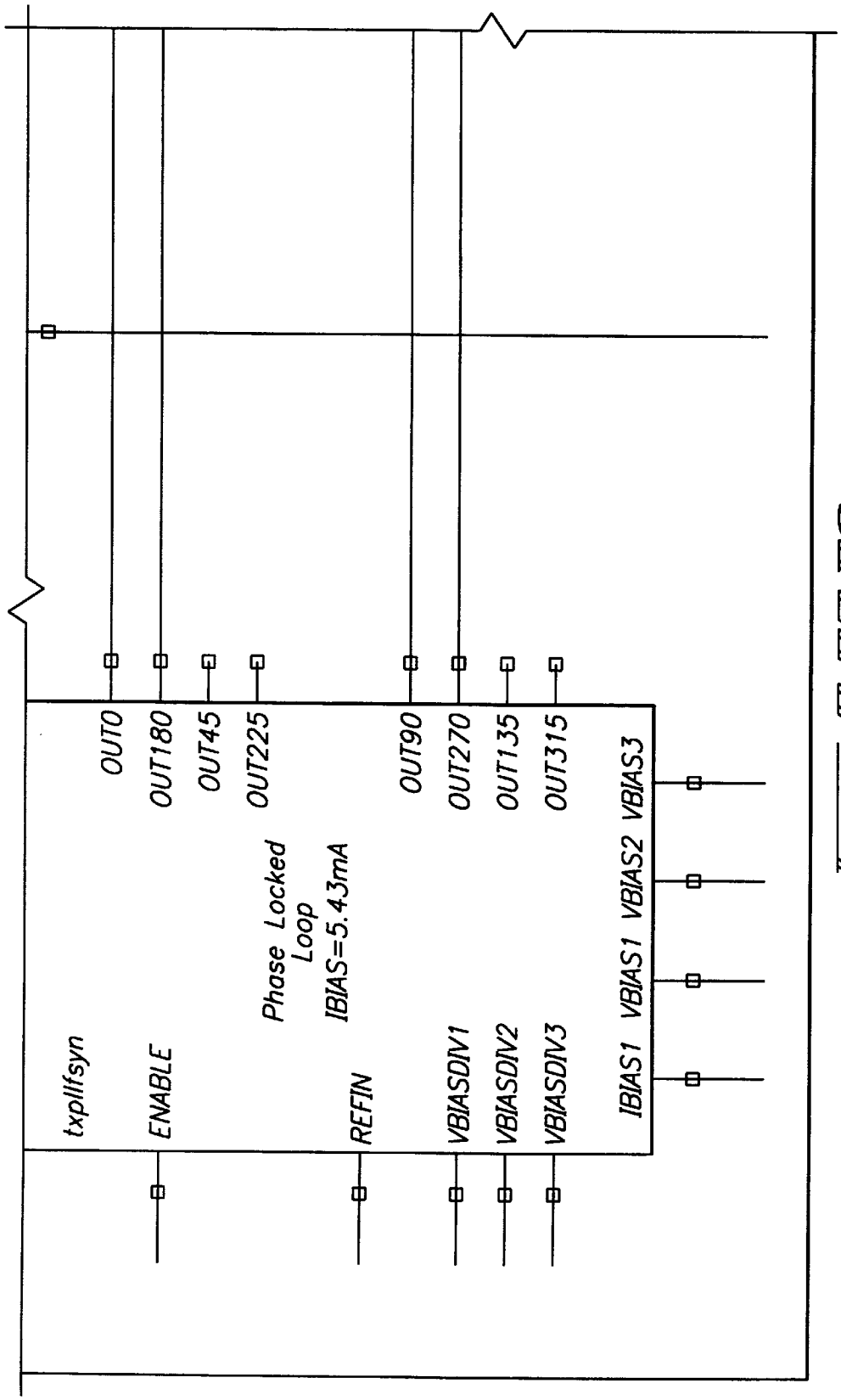


FIG. 88.111 IBIAS

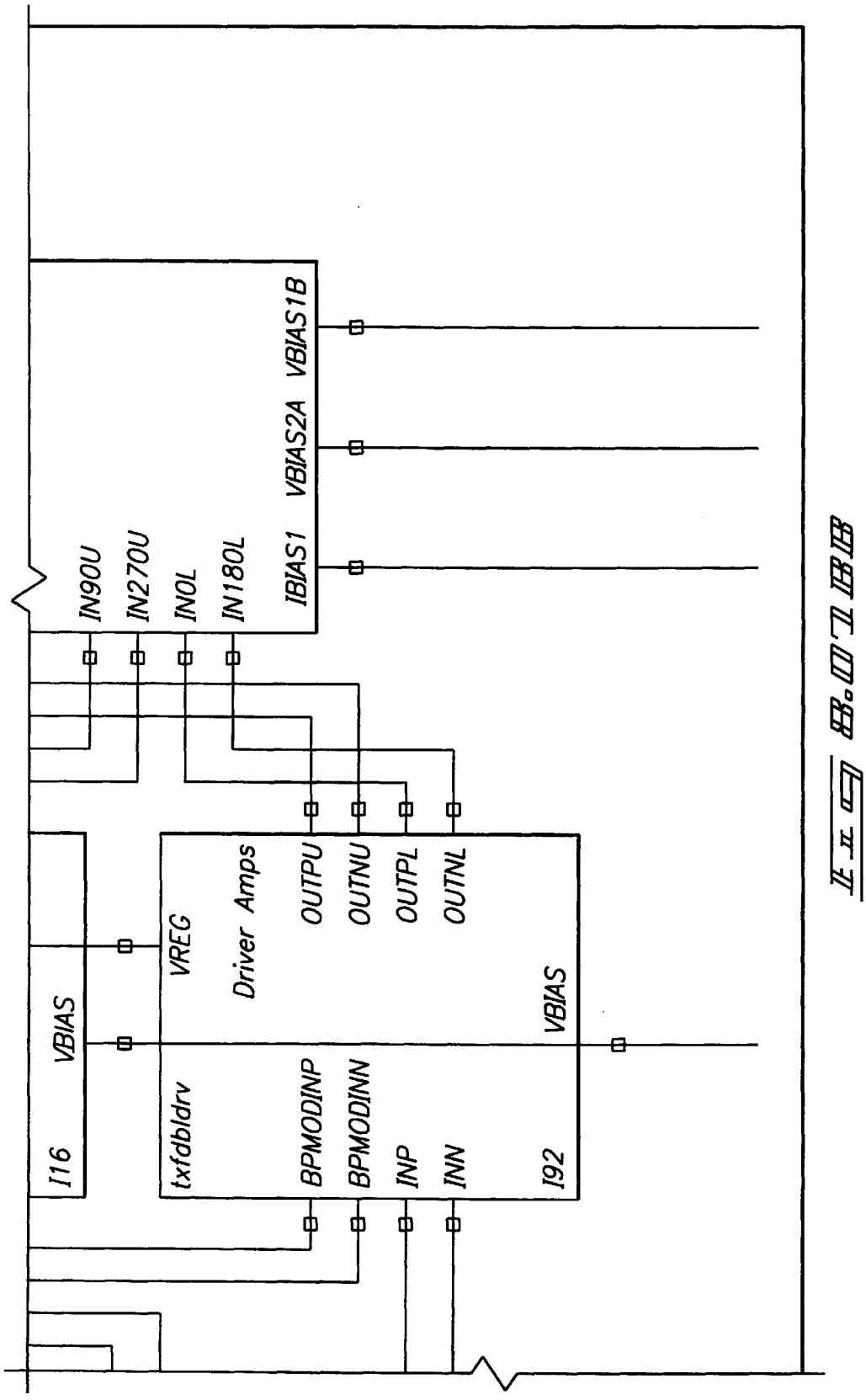


FIG. 88.00 BLANK

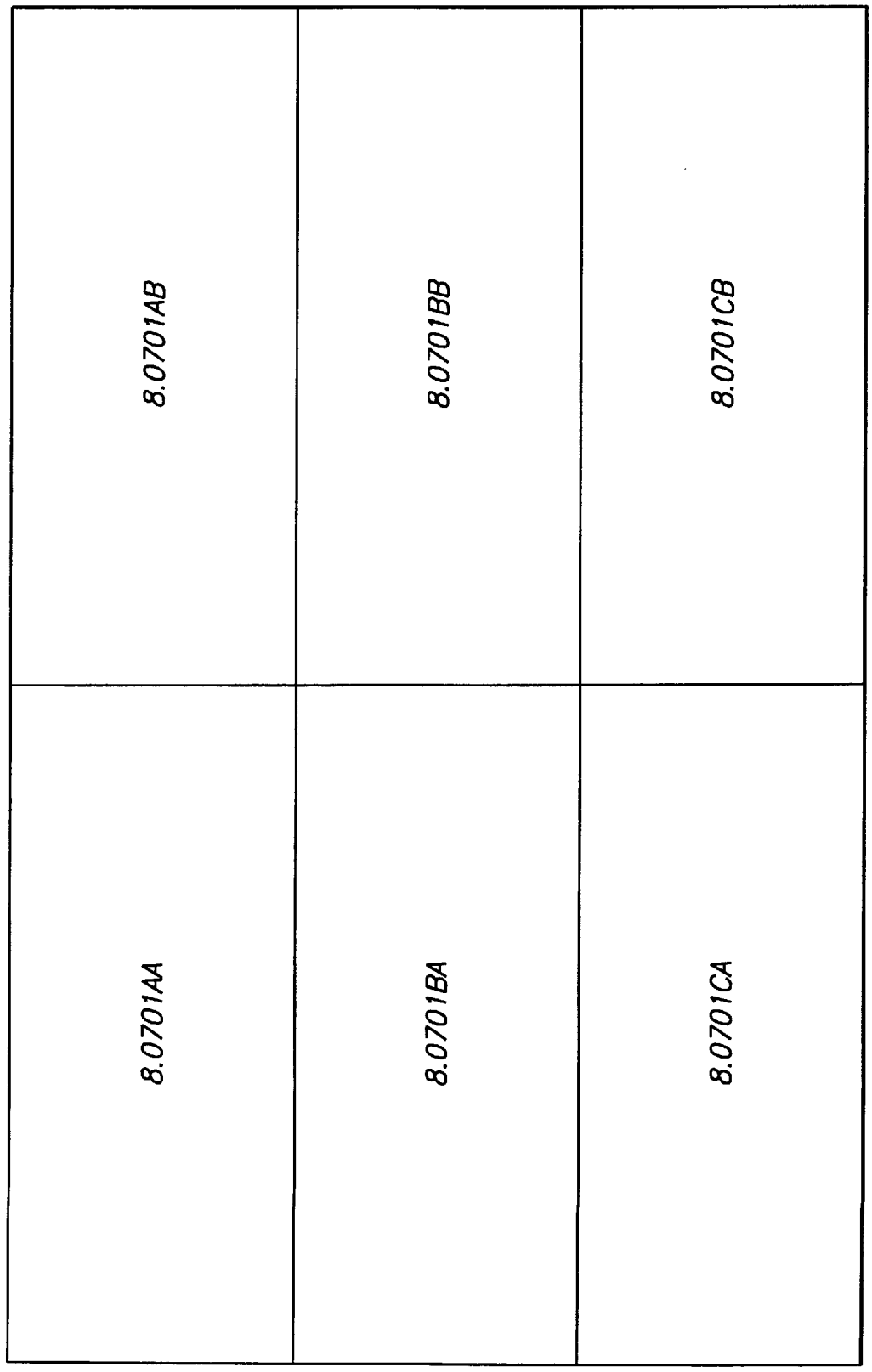
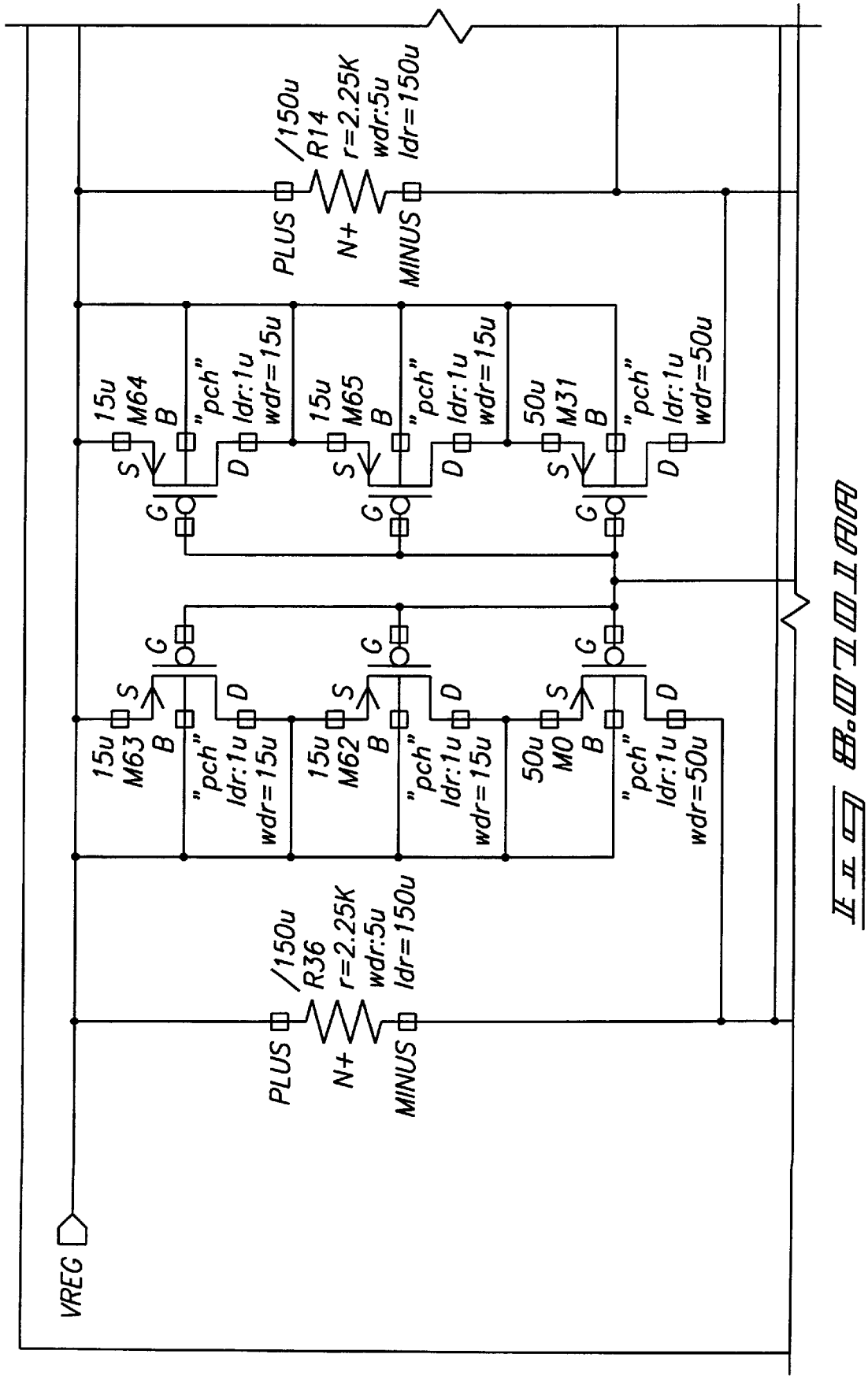
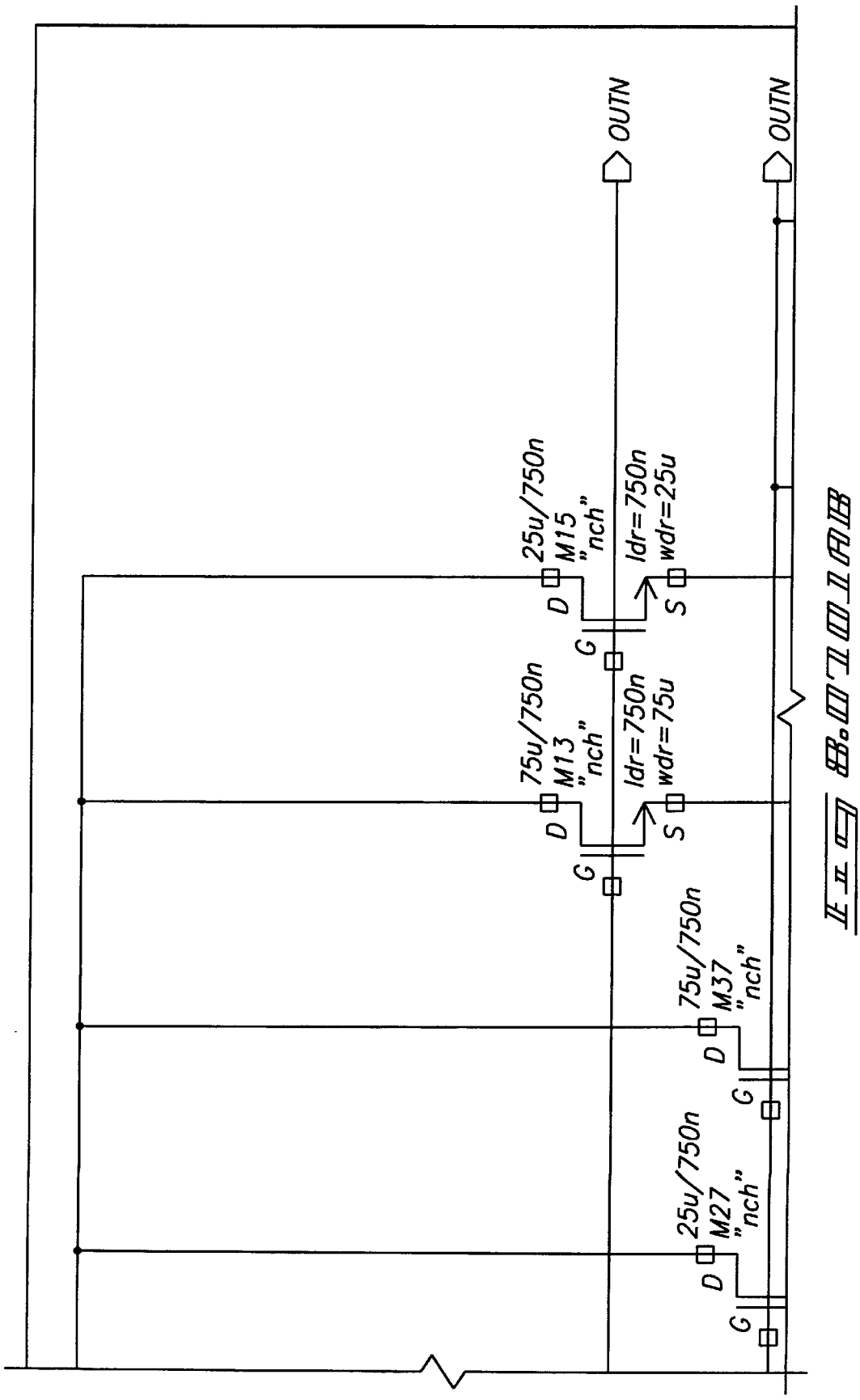


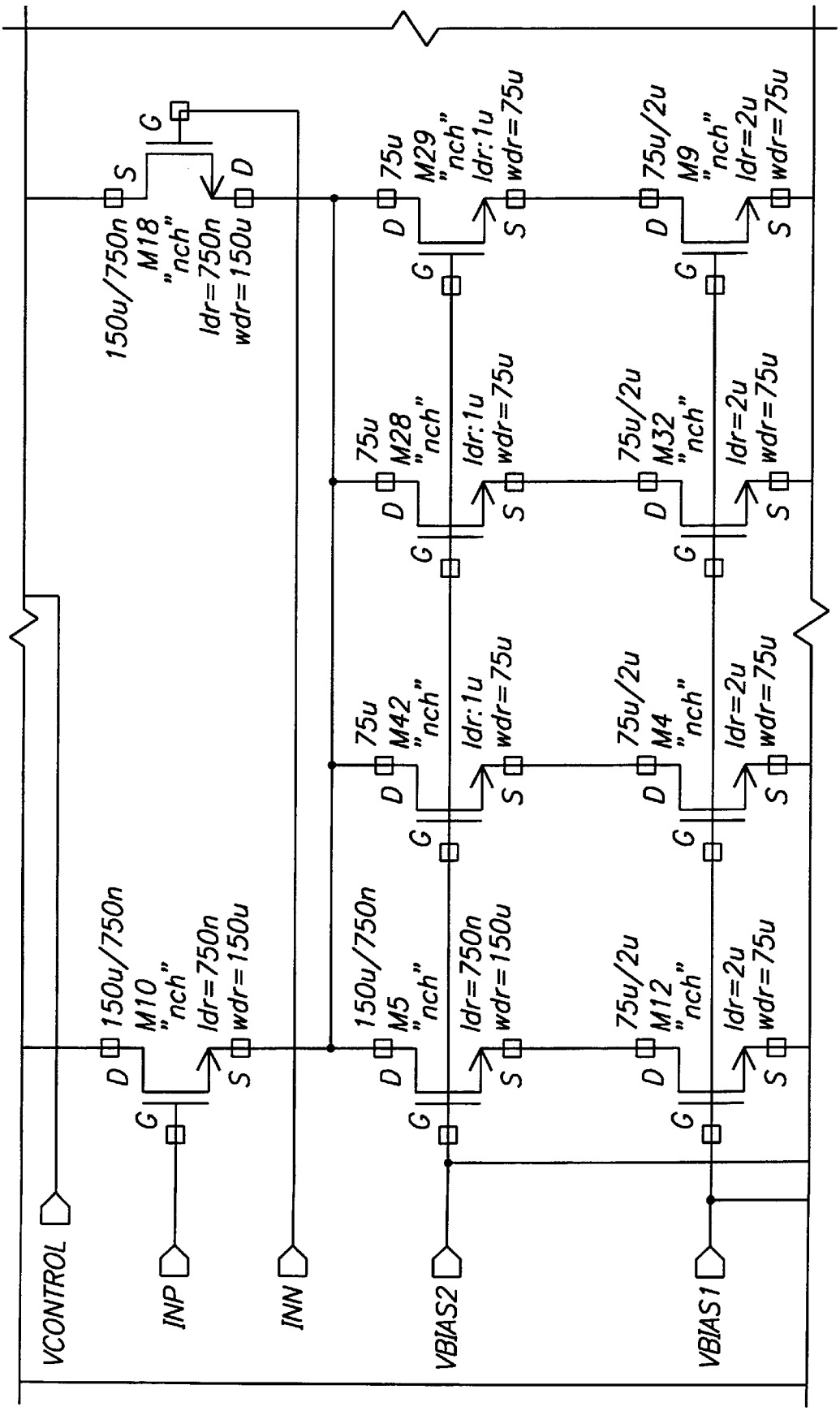
FIG. 8.0701



Фиг. 88.00LLAA


OUTN
OUTN
25u/750n
M15
"nch"
ldr=750n
wdr=25u
D
G
S
75u/750n
M13
"nch"
ldr=750n
wdr=75u
D
G
S
75u/750n
M37
"nch"
D
G
25u/750n
M27
"nch"
D
G

Фиг. 2202


VCONTROL
INP
INN
VBIAS2
VBIAS1
150u/750n M10 "nch" ldr=750n wdr=150u
150u/750n M18 "nch" ldr=750n wdr=150u
150u/750n M5 "nch" ldr=750n wdr=150u
75u M42 "nch" ldr:1u wdr=75u
75u M28 "nch" ldr:1u wdr=75u
75u M29 "nch" ldr:1u wdr=75u
75u/2u M12 "nch" ldr=2u wdr=75u
75u/2u M4 "nch" ldr=2u wdr=75u
75u/2u M32 "nch" ldr=2u wdr=75u
75u/2u M9 "nch" ldr=2u wdr=75u
D
G
S

ФИГ. 2203

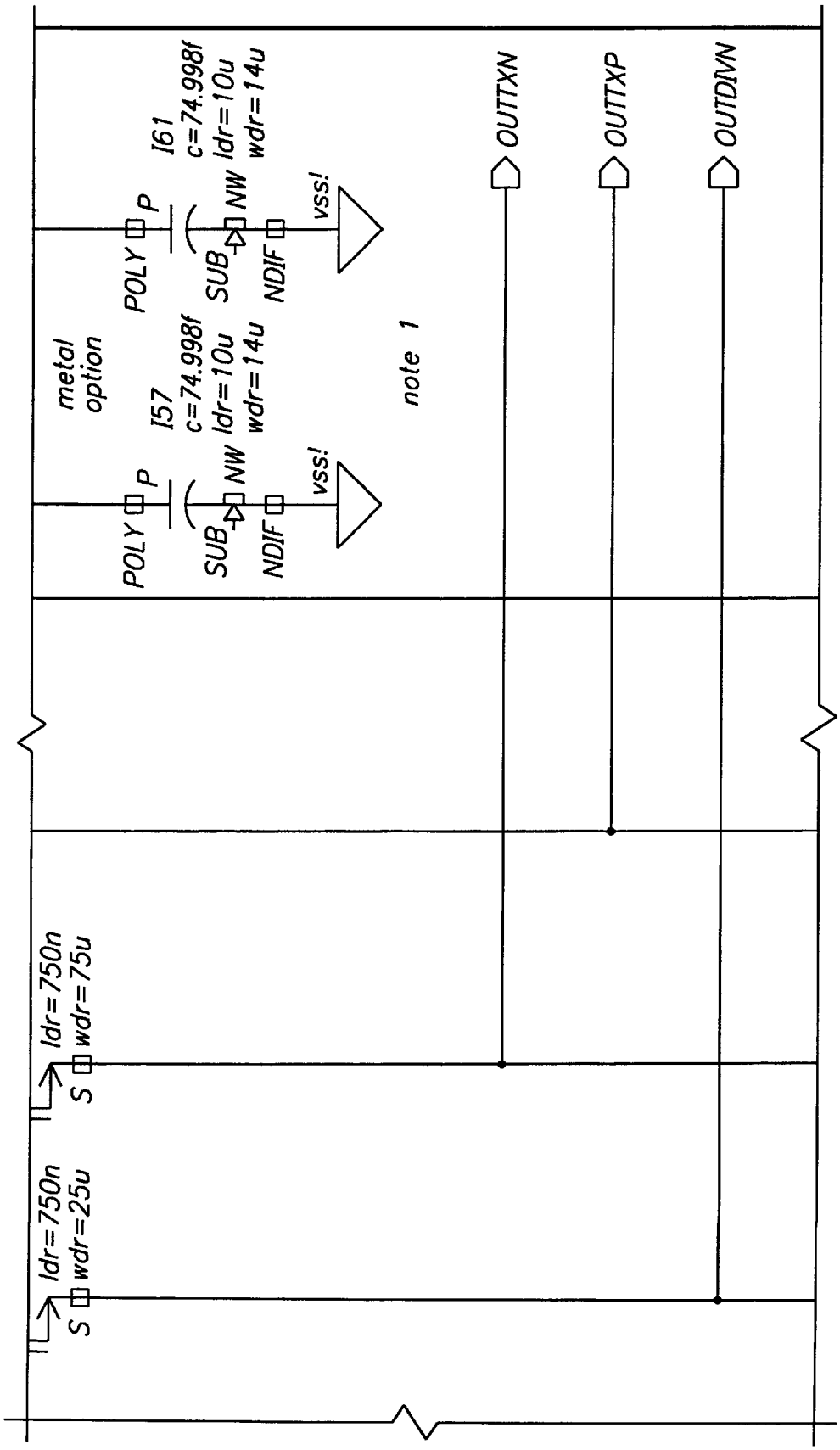


FIG 84.00 LL 00 II 88 BB

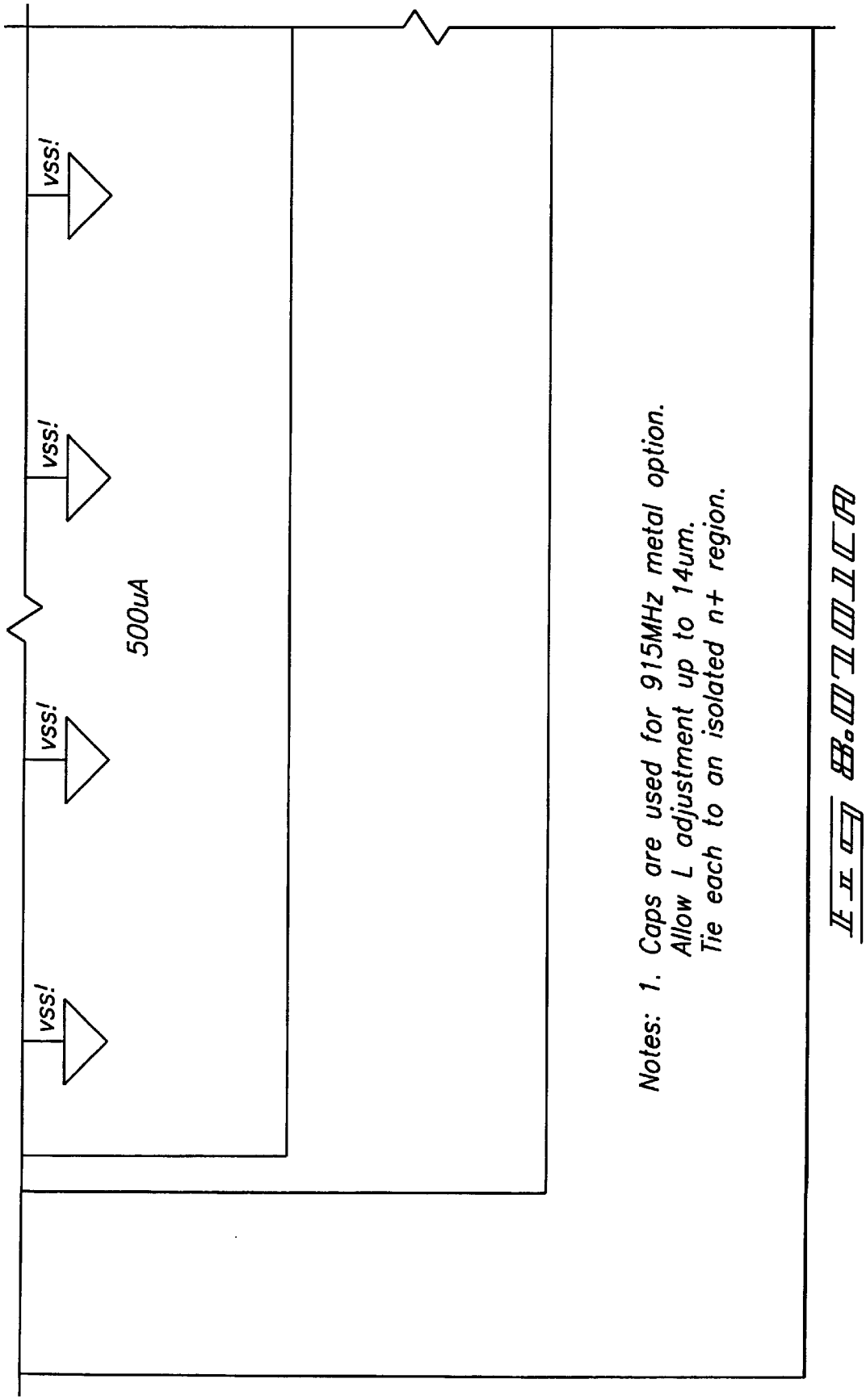

vss!
vss!
vss!
vss!
500uA
Notes: 1. Caps are used for 915MHz metal option.
Allow L adjustment up to 14um.
Tie each to an isolated n+ region.

FIG 8.00116A

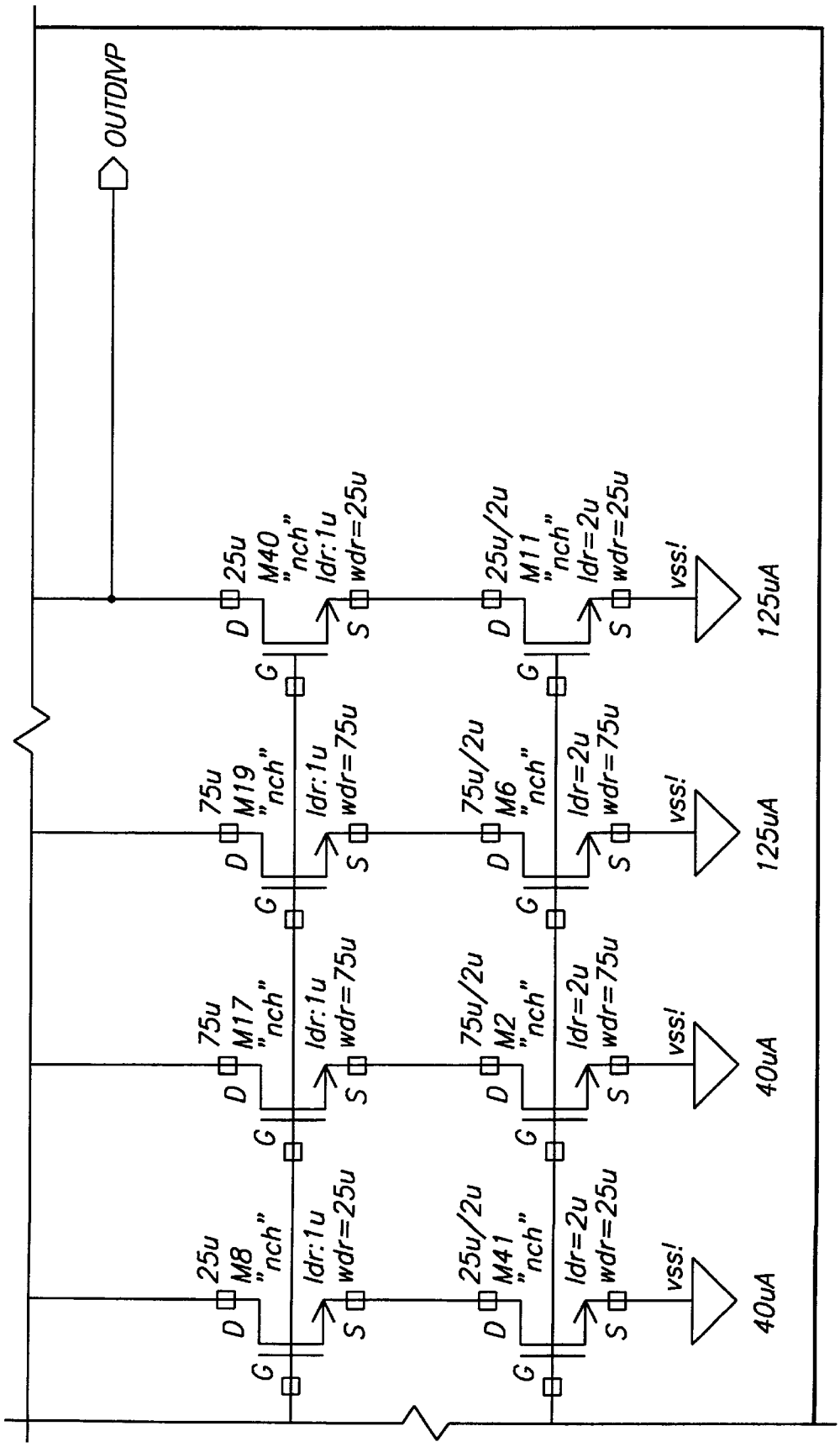

OUTDIVP
25u
M40
"nch"
ldr:1u
wdr=25u
25u/2u
M11
"nch"
ldr=2u
wdr=25u
vss!
125uA
75u
M19
"nch"
ldr:1u
wdr=75u
75u/2u
M6
"nch"
ldr=2u
wdr=75u
vss!
125uA
75u
M17
"nch"
ldr:1u
wdr=75u
75u/2u
M2
"nch"
ldr=2u
wdr=75u
vss!
40uA
25u
M8
"nch"
ldr:1u
wdr=25u
25u/2u
M41
"nch"
ldr=2u
wdr=25u
vss!
40uA
D
G
S

FIG. 2206

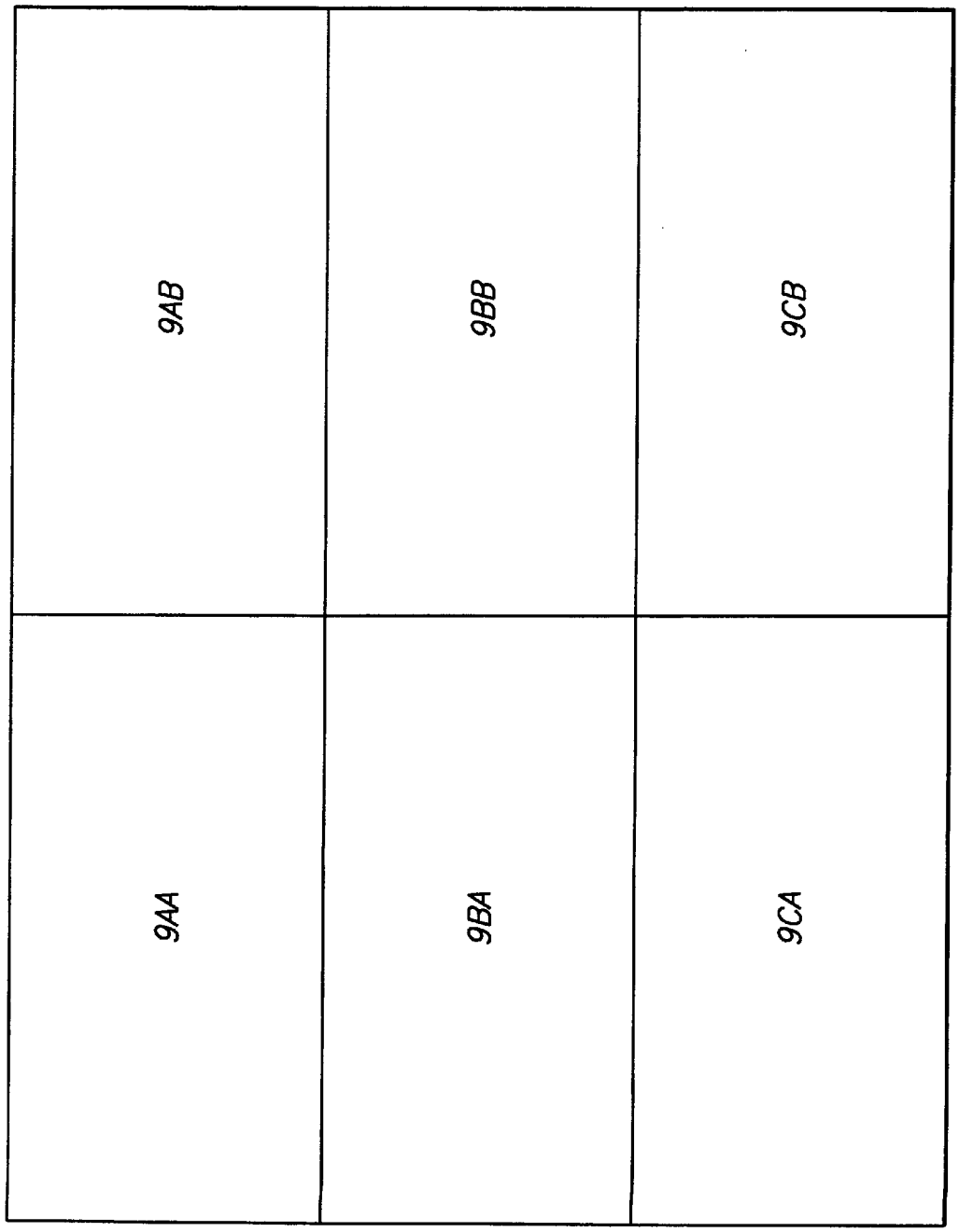
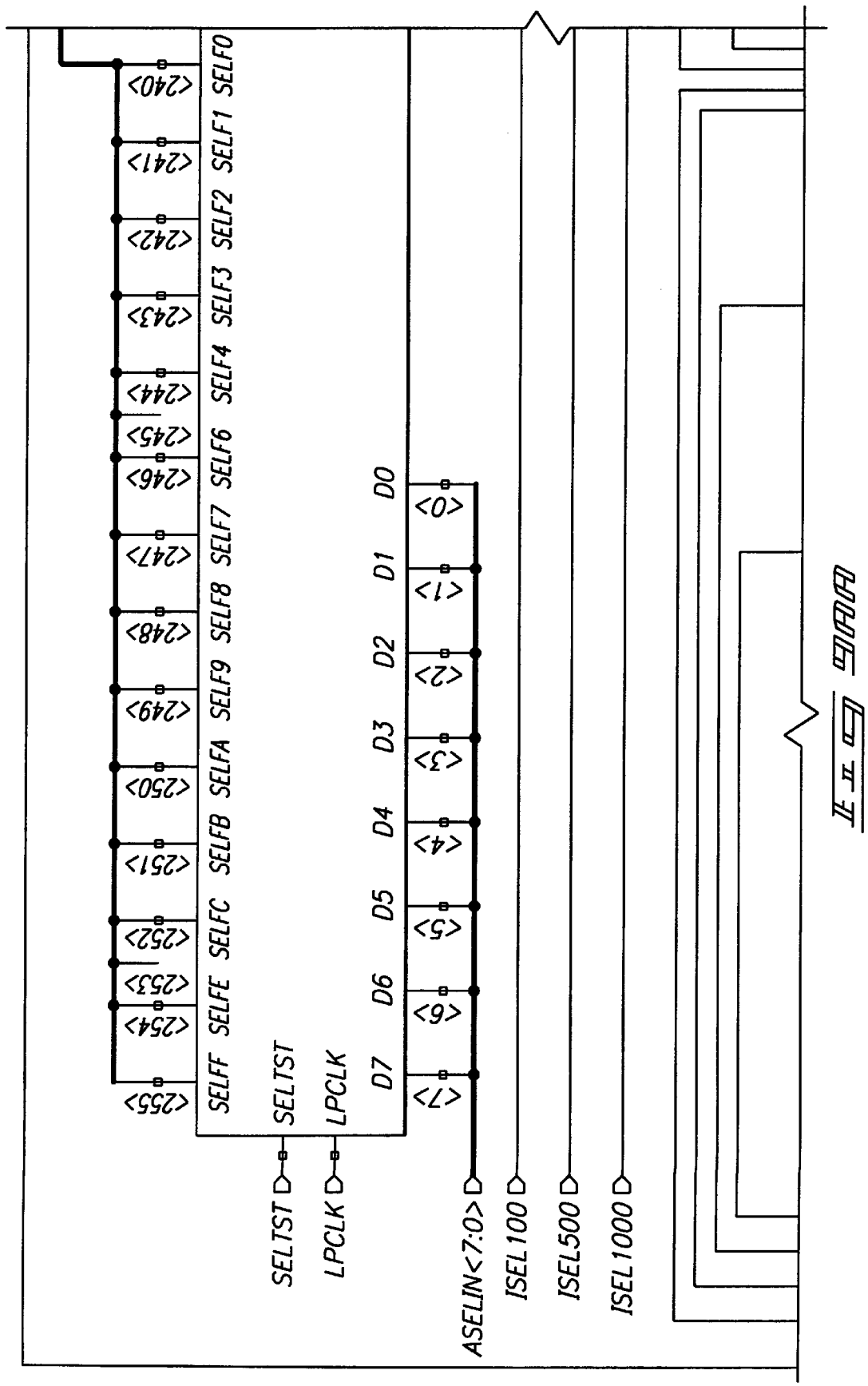


Fig. 9


SELF0
SELF1
SELF2
SELF3
SELF4
SELF6
SELF7
SELF8
SELF9
SELFA
SELFB
SELFC
SELFE
SELFF
SELTST
LPCLK
D0
D1
D2
D3
D4
D5
D6
D7
<240>
<241>
<242>
<243>
<244>
<245>
<246>
<247>
<248>
<249>
<250>
<251>
<252>
<253>
<254>
<255>
<0>
<1>
<2>
<3>
<4>
<5>
<6>
<7>
SELTST
LPCLK
ASELIN<7:0>
ISEL100
ISEL500
ISEL1000
VDD
GND

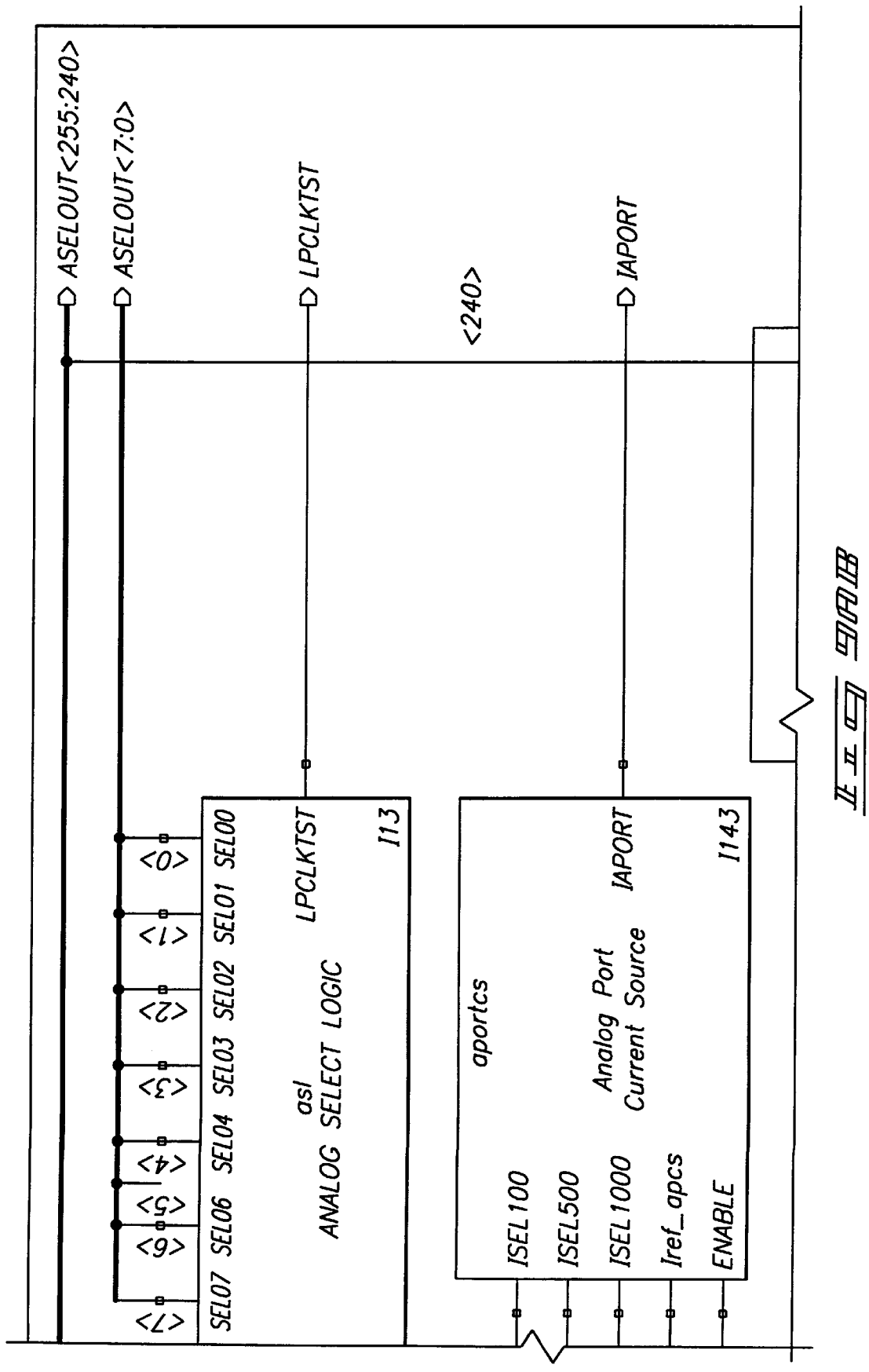

ASELOUT<255:240>
ASELOUT<7:0>
LPCLKTST
<240>
IAPORT
<0>
<1>
<2>
<3>
<4>
<5>
<6>
<7>
SEL07 SEL06 SEL04 SEL03 SEL02 SEL01 SEL00
asl
ANALOG SELECT LOGIC
LPCLKTST
I13
aportcs
ISEL100
ISEL500
ISEL1000
Iref_apcs
ENABLE
Analog Port
Current Source
IAPORT
I143

FIG 5A

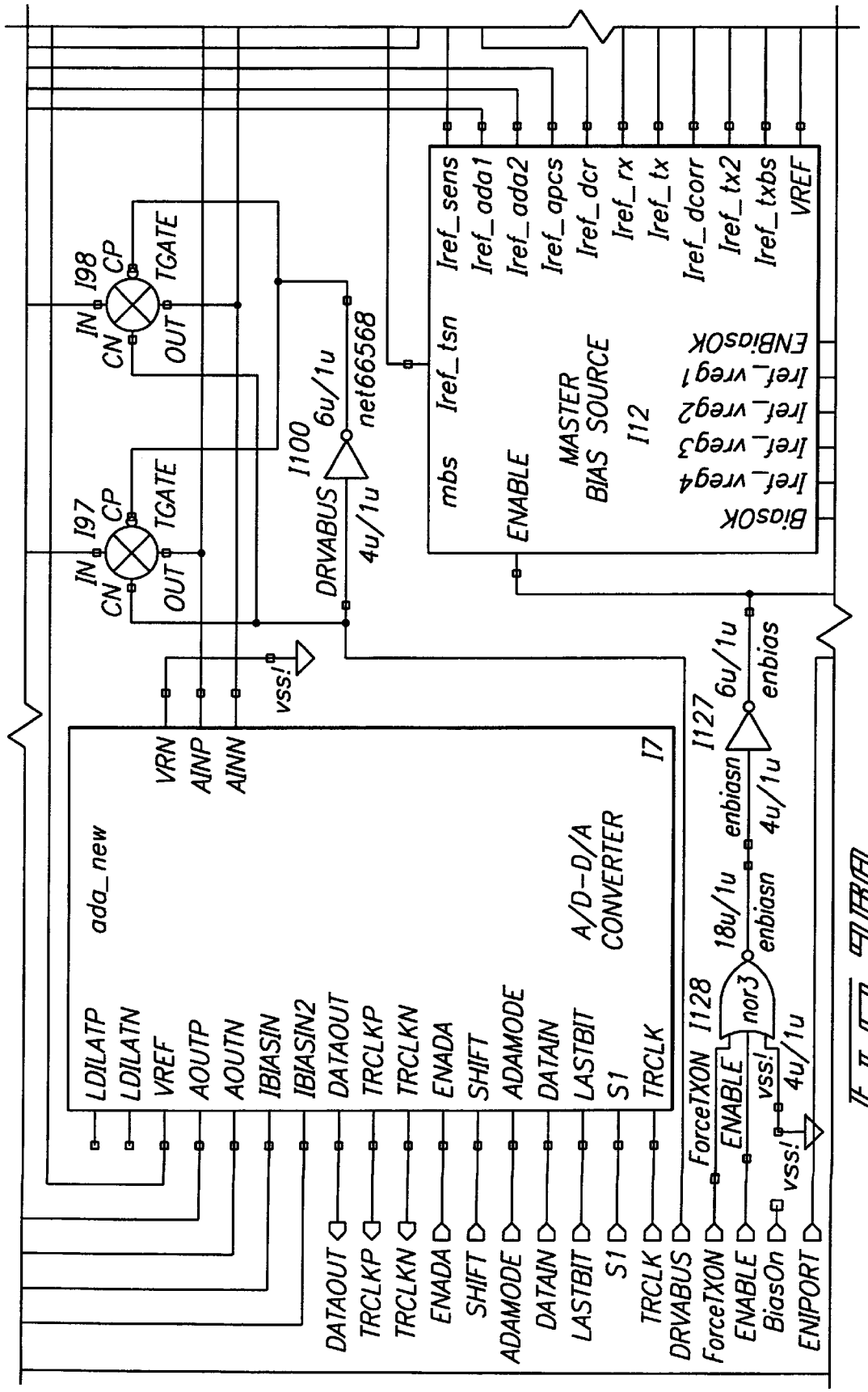
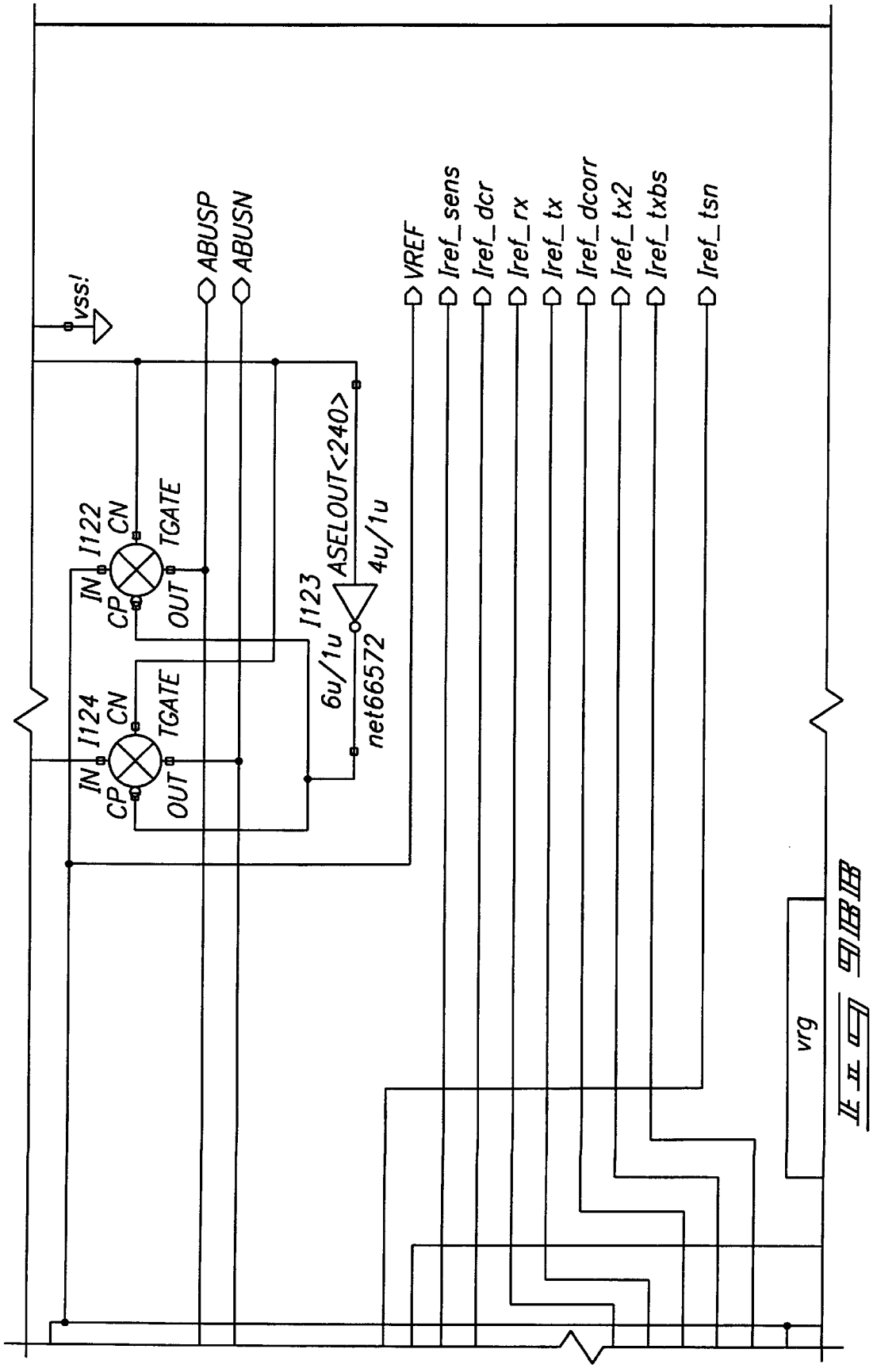

I98
CP
IN
CN
OUT
TGATE
I97
CP
IN
CN
OUT
TGATE
I100
6u/1u
4u/1u
DRVABUS
net66568
vss!
VRN
AINP
AINN
ada_new
LDILATP
LDILATN
VREF
AOUTP
AOUTN
IBIASIN
IBIASIN2
DATAOUT
TRCLKP
TRCLKN
ENADA
SHIFT
ADAMODE
DATAIN
LASTBIT
S1
TRCLK
A/D-D/A
CONVERTER
I7
DRVABUS
ForceTXON
ENABLE
BiasOn
ENIPORT
I128
nor3
18u/1u
4u/1u
I127
6u/1u
enbias
enbiasn
mbs
Iref_tsn
ENABLE
MASTER
BIAS SOURCE
I12
Iref_sens
Iref_ada1
Iref_ada2
Iref_apcs
Iref_dcr
Iref_rx
Iref_tx
Iref_dcorr
Iref_tx2
Iref_txbs
VREF
BiasOK
Iref_vreg4
Iref_vreg3
Iref_vreg2
Iref_vreg1
ENBiasOK

FIG 113A


vss!
ABUSP
ABUSN
VREF
Iref_sens
Iref_dcr
Iref_rx
Iref_tx
Iref_dcorr
Iref_tx2
Iref_txbs
Iref_tsn
I122
CN
IN
CP
TGATE
OUT
I124
CN
IN
CP
TGATE
OUT
I123
6u/1u
ASELOUT<240>
4u/1u
net66572
vrg

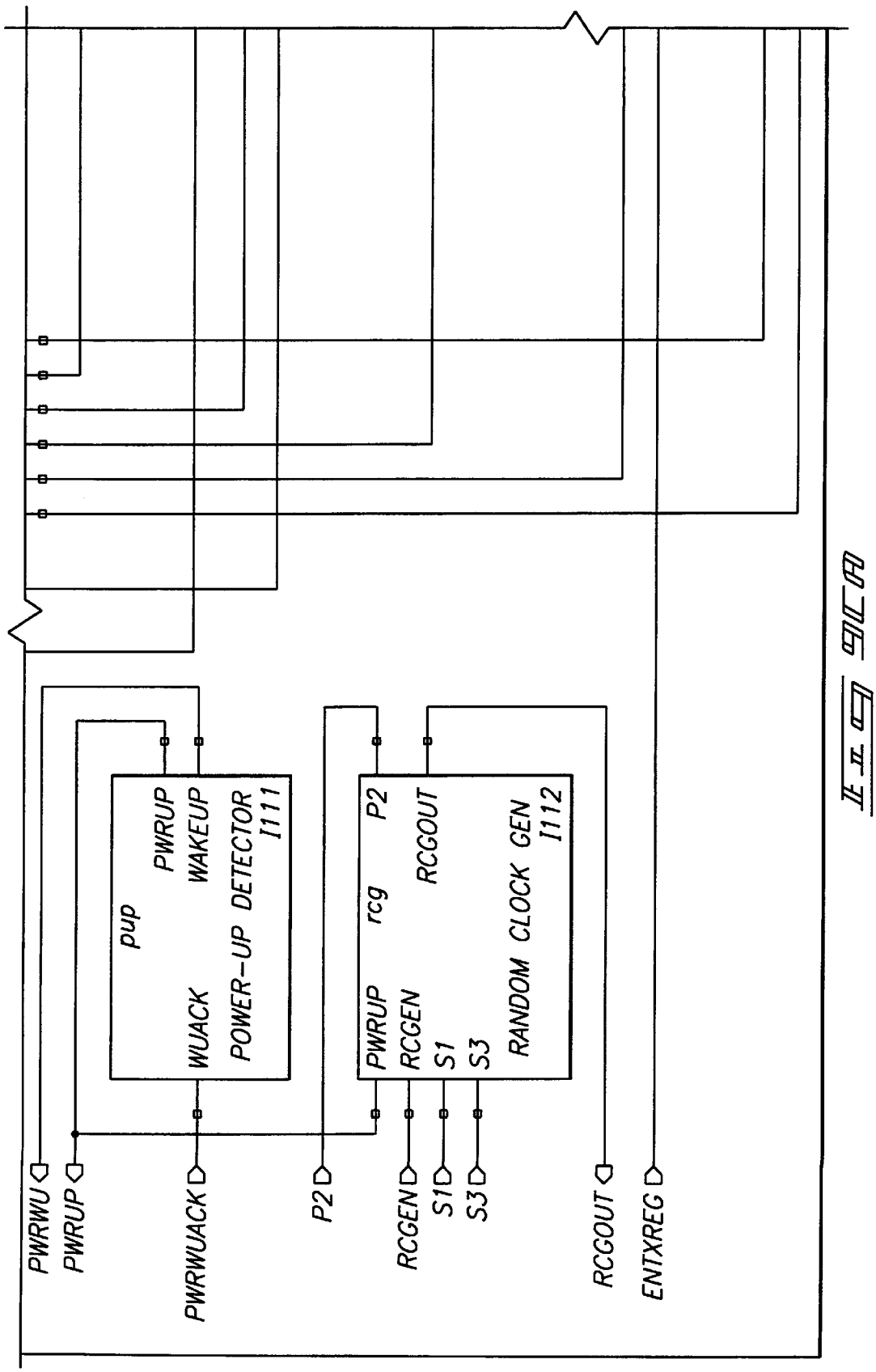

PWRWU
PWRUP
PWRWUACK
P2
RCGEN
S1
S3
RCGOUT
ENTXREG
pup
PWRUP
WAKEUP
WUACK
POWER-UP DETECTOR
1111
rcg
P2
RCGOUT
PWRUP
RCGEN
S1
S3
RANDOM CLOCK GEN
1112

FIG 95A

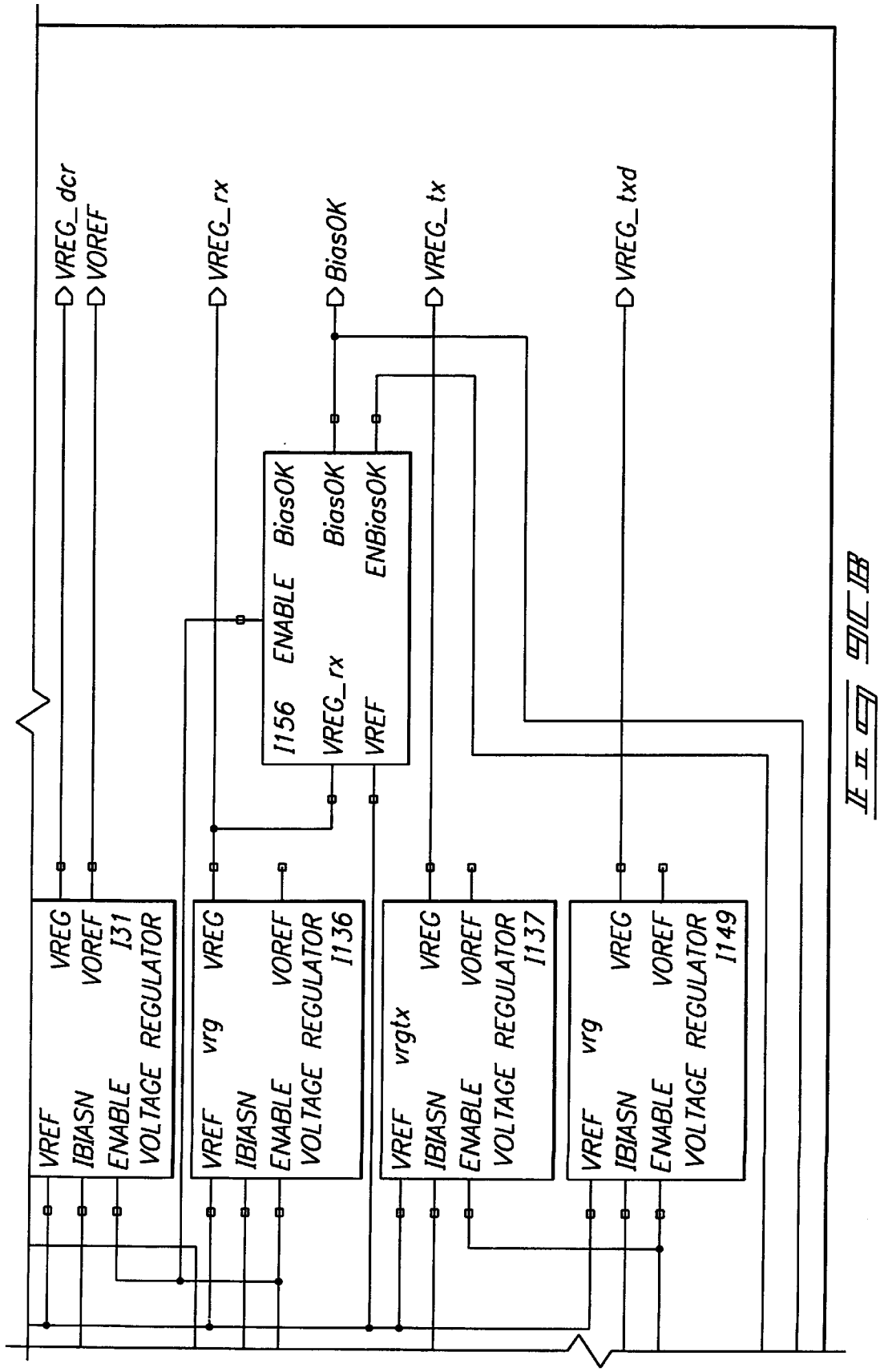

VREG_dcr
VOREF
VREG_rx
BiasOK
VREG_tx
VREG_txd
I156 ENABLE BiasOK
VREG_rx
VREF
BiasOK
ENBiasOK
VREF IBIASN ENABLE VOLTAGE REGULATOR
VREG VOREF I31
VREF vrg IBIASN ENABLE VOLTAGE REGULATOR
VREG VOREF I136
VREF vrgtx IBIASN ENABLE VOLTAGE REGULATOR
VREG VOREF I137
VREF vrg IBIASN ENABLE VOLTAGE REGULATOR
VREG VOREF I149

Fig. 159

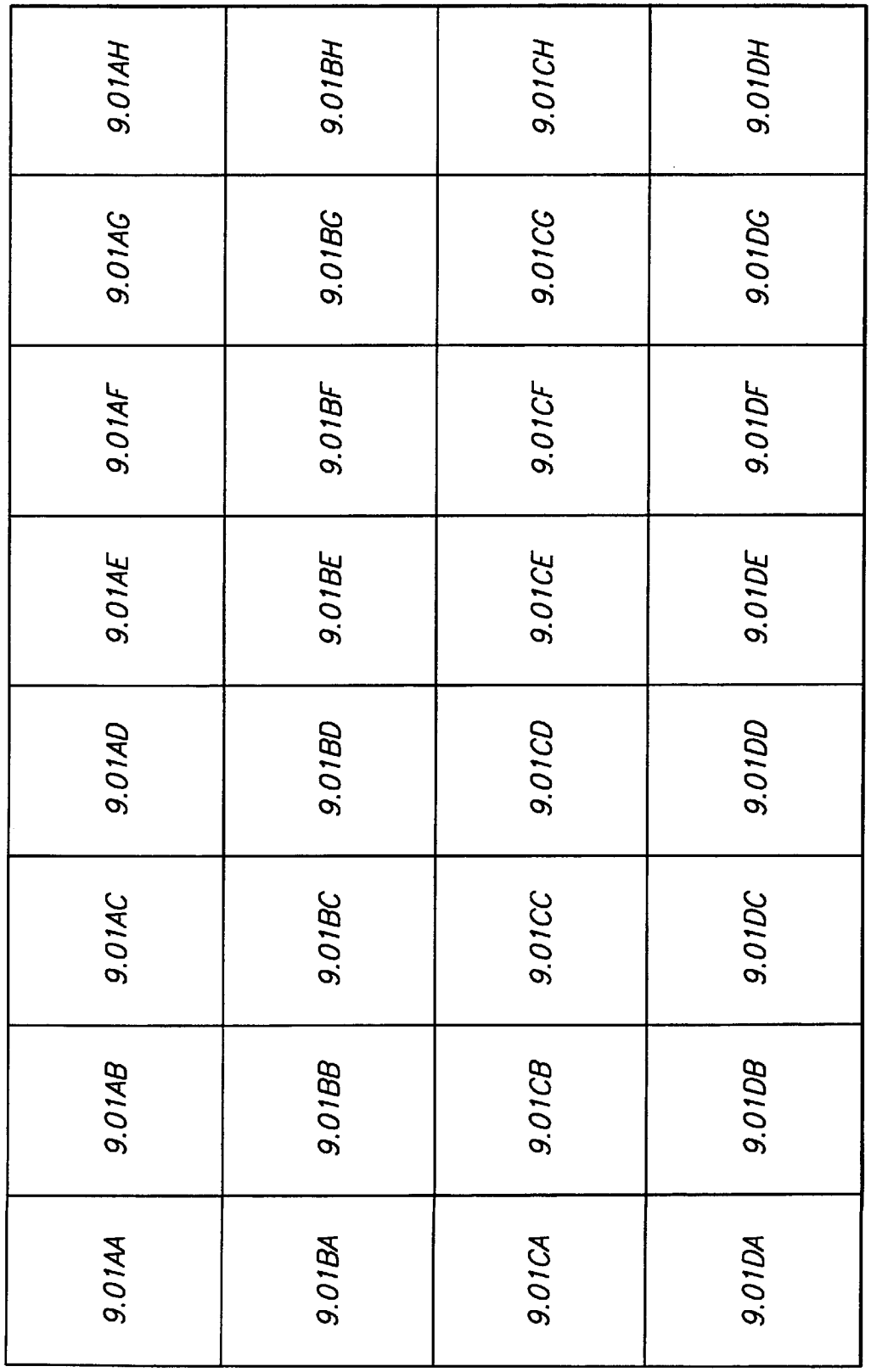

9.01AH
9.01BH
9.01CH
9.01DH
9.01AG
9.01BG
9.01CG
9.01DG
9.01AF
9.01BF
9.01CF
9.01DF
9.01AE
9.01BE
9.01CE
9.01DE
9.01AD
9.01BD
9.01CD
9.01DD
9.01AC
9.01BC
9.01CC
9.01DC
9.01AB
9.01BB
9.01CB
9.01DB
9.01AA
9.01BA
9.01CA
9.01DA

FIG. 9.01H

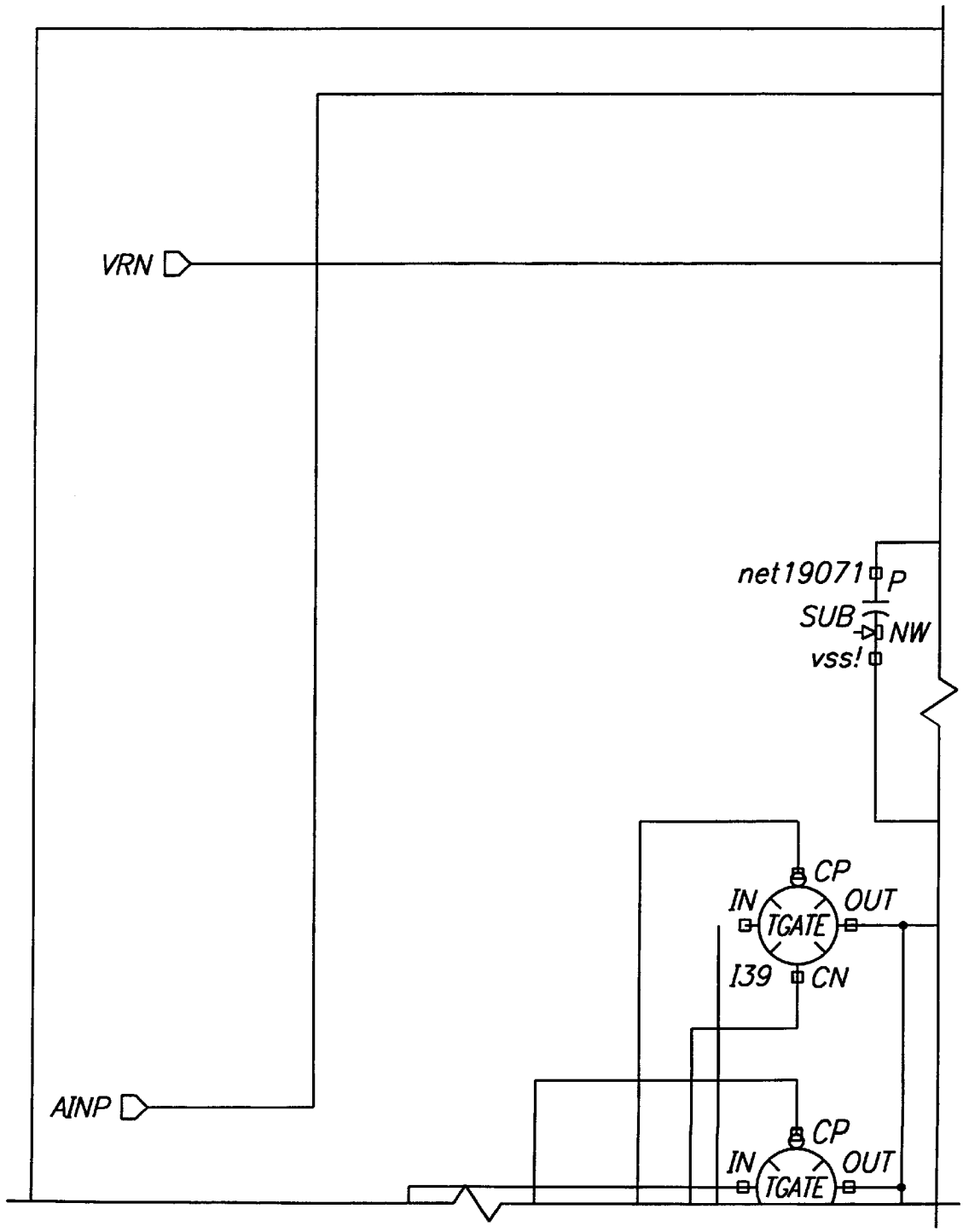

VRN
net19071
P
SUB
NW
vss!
CP
IN
OUT
TGATE
I39
CN
AINP
CP
IN
OUT
TGATE

Fig 9.01AA

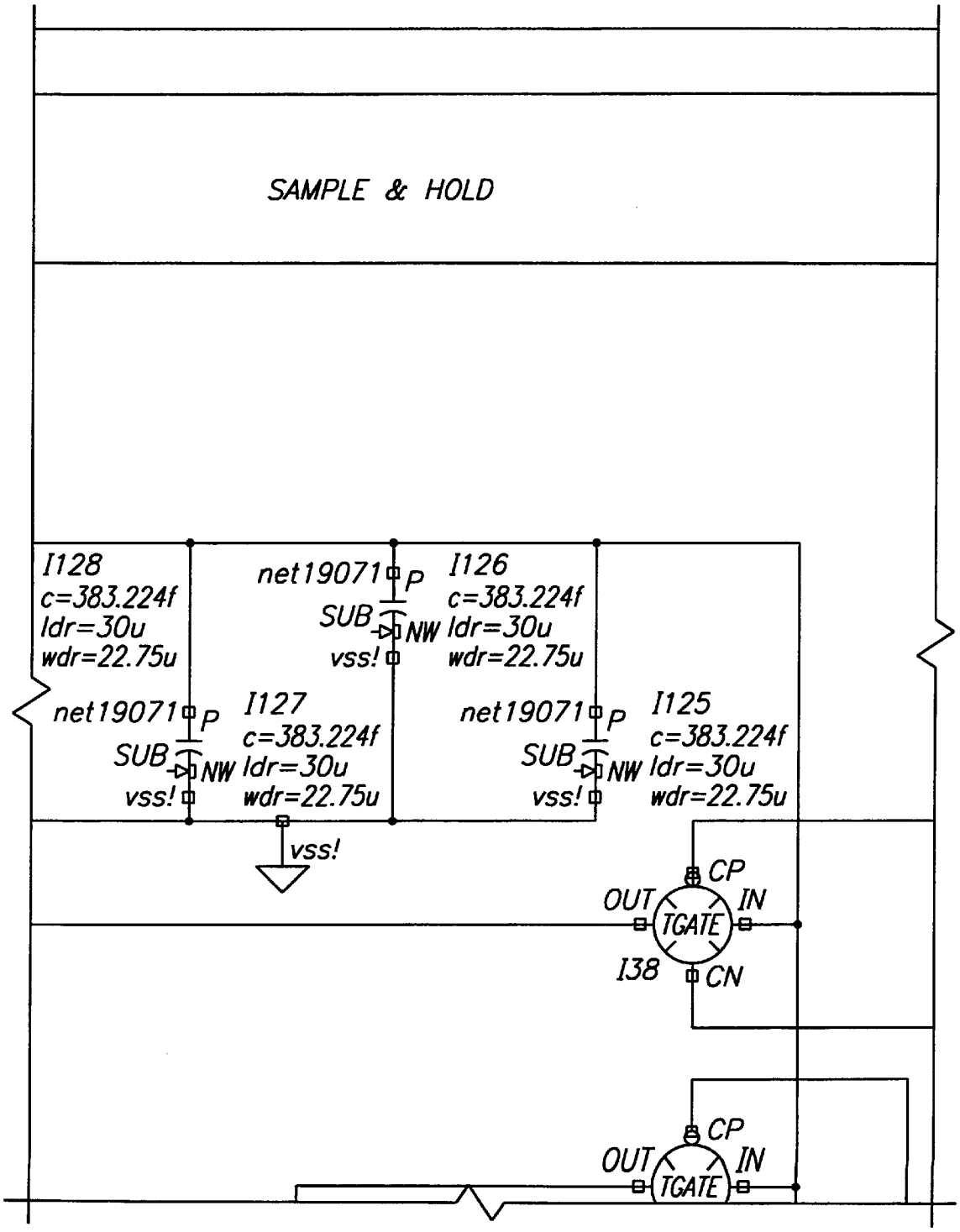

SAMPLE & HOLD
I128
c=383.224f
ldr=30u
wdr=22.75u
net19071
P
SUB
NW
vss!
I127
c=383.224f
ldr=30u
wdr=22.75u
net19071
P
SUB
NW
vss!
I126
c=383.224f
ldr=30u
wdr=22.75u
net19071
P
SUB
NW
vss!
I125
c=383.224f
ldr=30u
wdr=22.75u
vss!
CP
OUT
IN
TGATE
I38
CN
CP
OUT
IN
TGATE

Fig 9.01AB

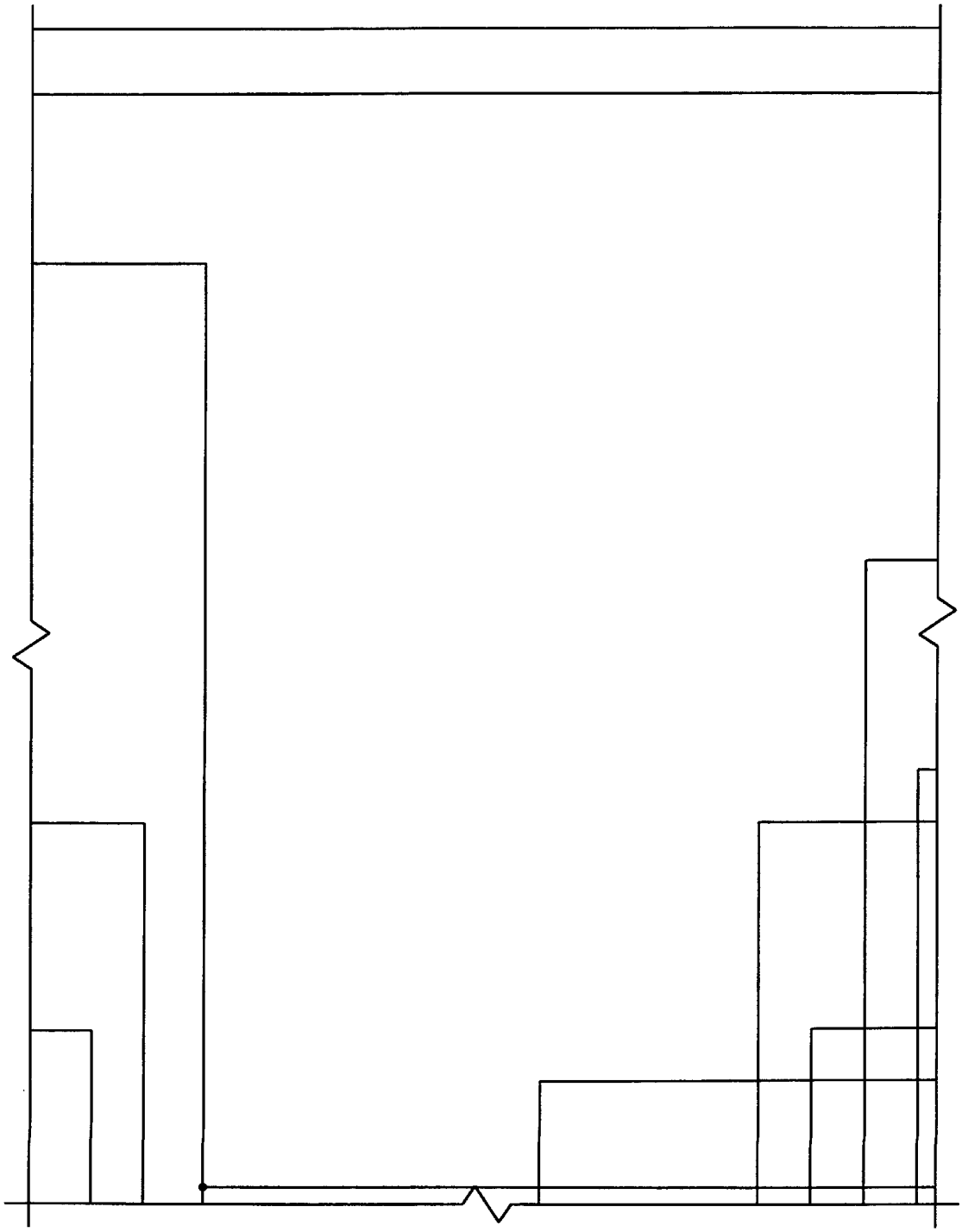


Fig 9.01AC

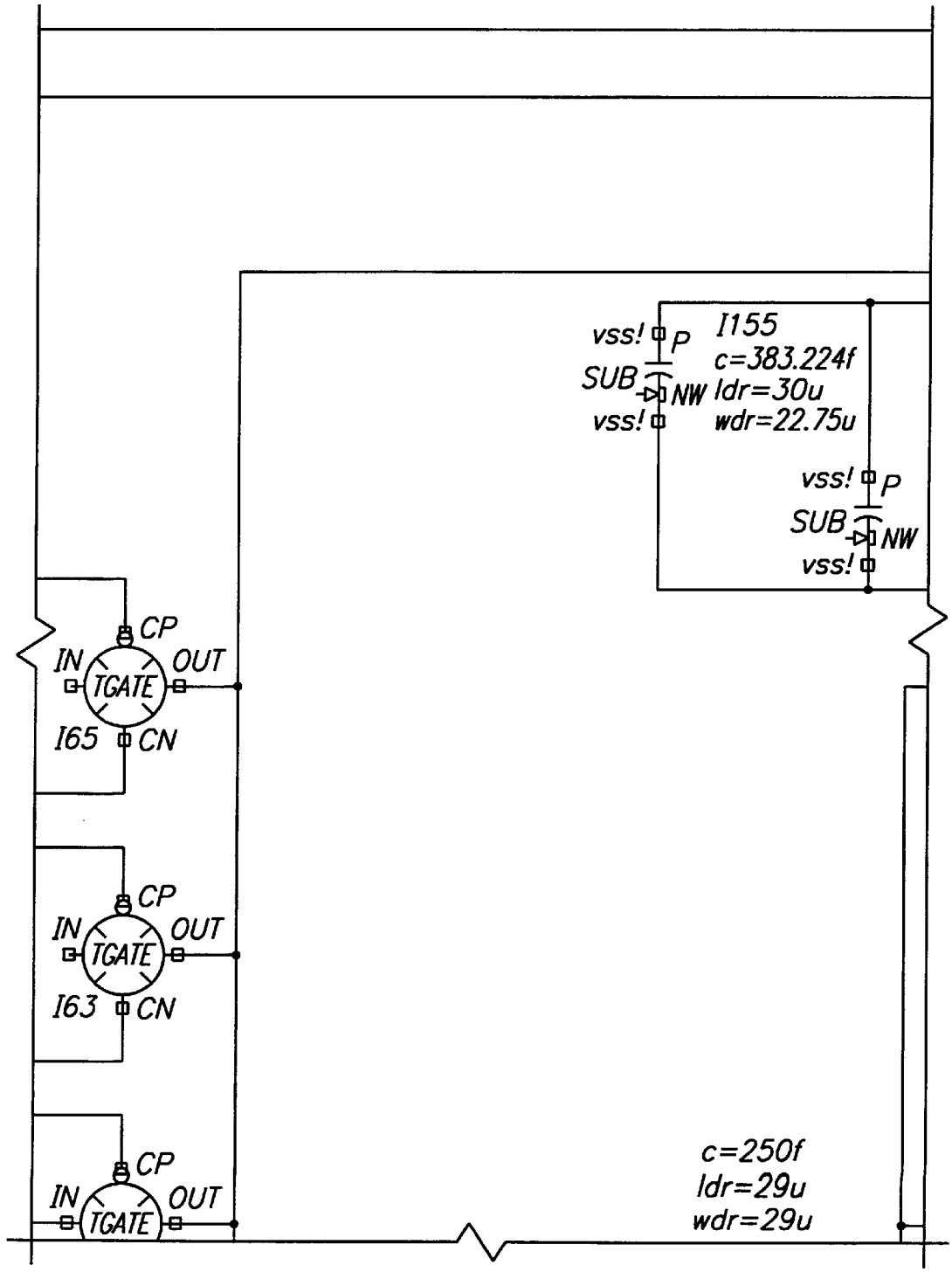

vss!
P
SUB
NW
vss!
I155
c=383.224f
ldr=30u
wdr=22.75u
vss!
P
SUB
NW
vss!
CP
IN
OUT
TGATE
I65
CN
CP
IN
OUT
TGATE
I63
CN
CP
IN
OUT
TGATE
c=250f
ldr=29u
wdr=29u

Fig 9.01AD

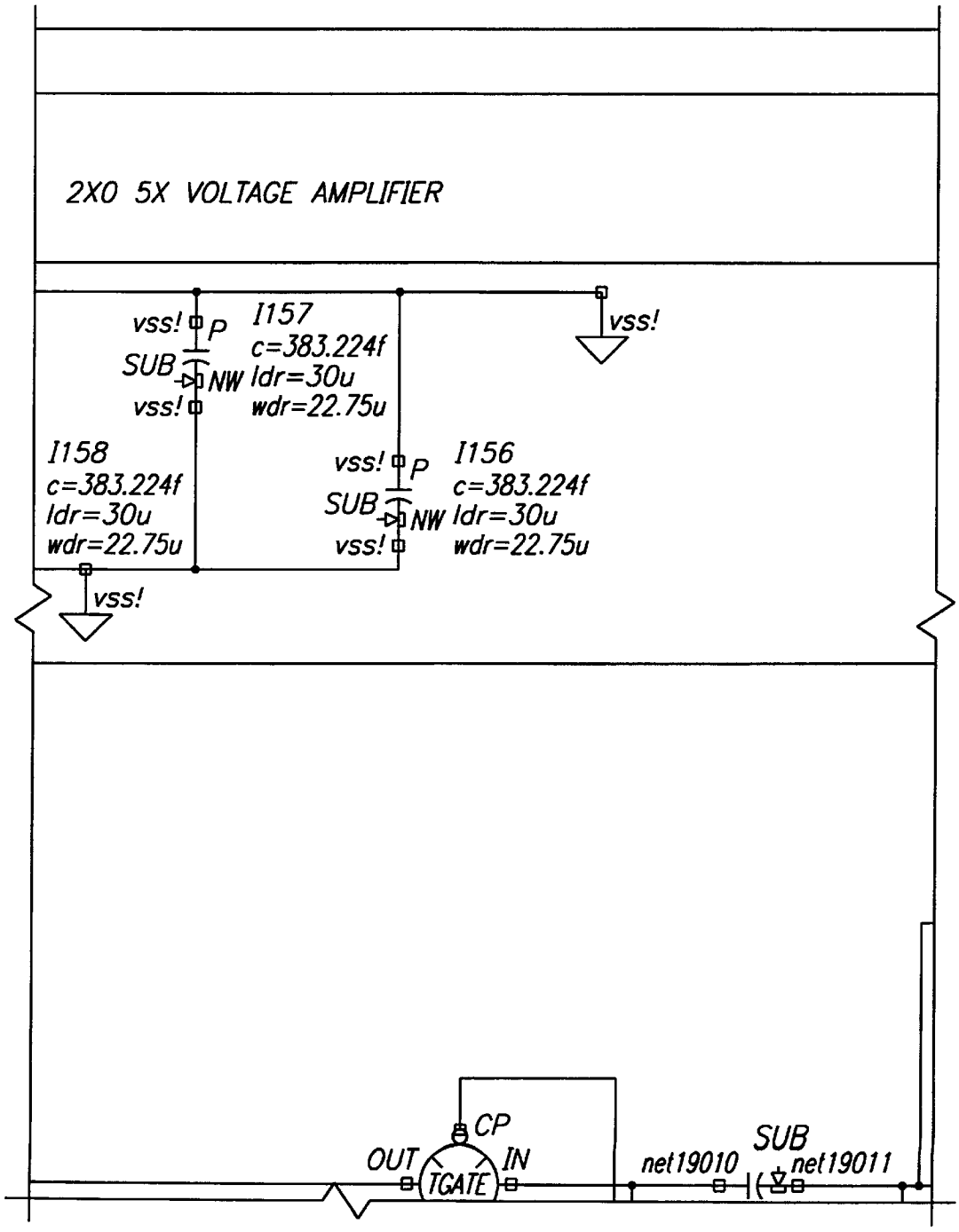

2X0 5X VOLTAGE AMPLIFIER
vss!
P
SUB
NW
vss!
I157
c=383.224f
ldr=30u
wdr=22.75u
vss!
I158
c=383.224f
ldr=30u
wdr=22.75u
vss!
vss!
P
SUB
NW
vss!
I156
c=383.224f
ldr=30u
wdr=22.75u
CP
OUT
IN
TGATE
net19010
SUB
net19011

Fig 9.01AE

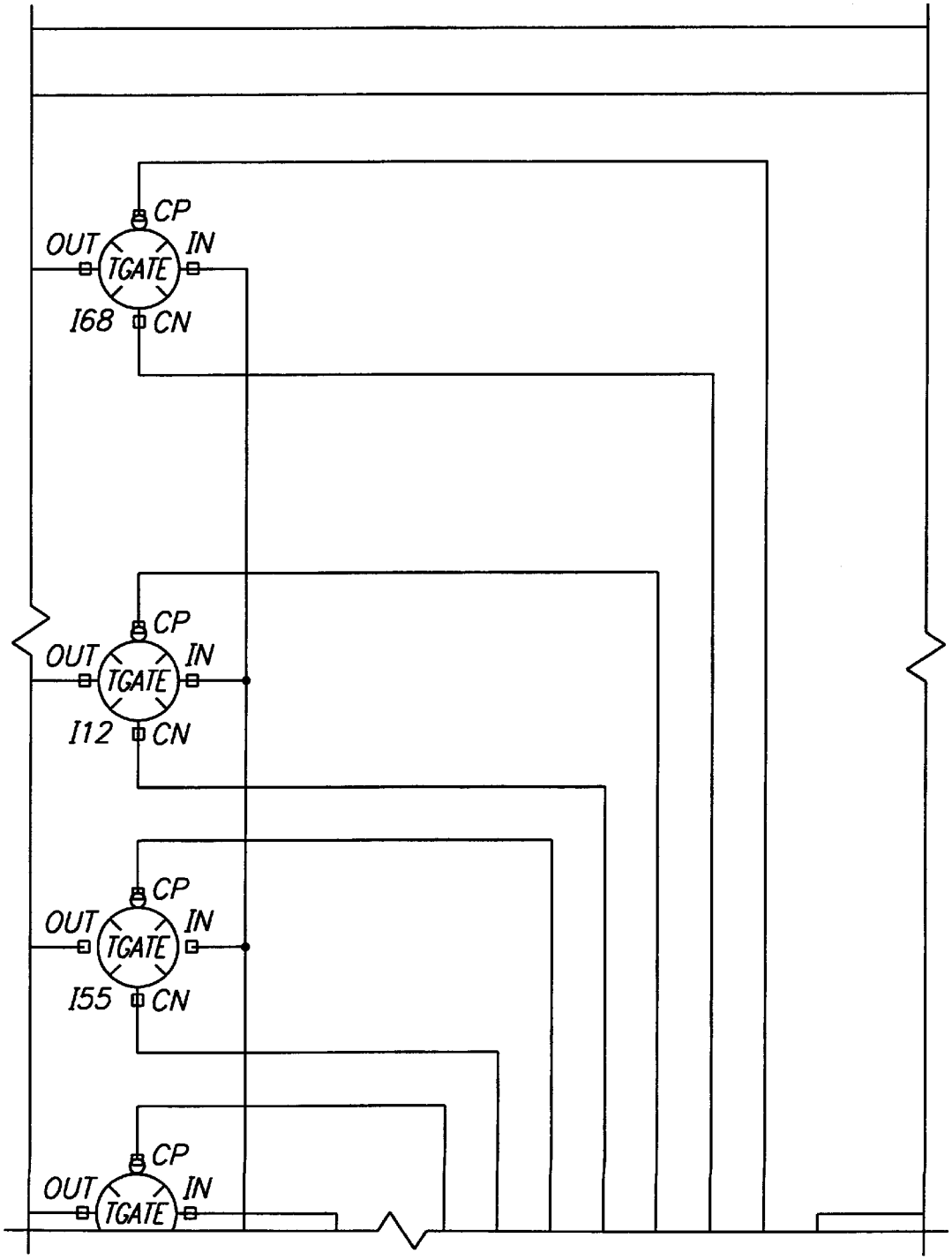

CP
OUT
IN
TGATE
I68
CN
CP
OUT
IN
TGATE
I12
CN
CP
OUT
IN
TGATE
I55
CN
CP
OUT
IN
TGATE

Fig 9.01AF

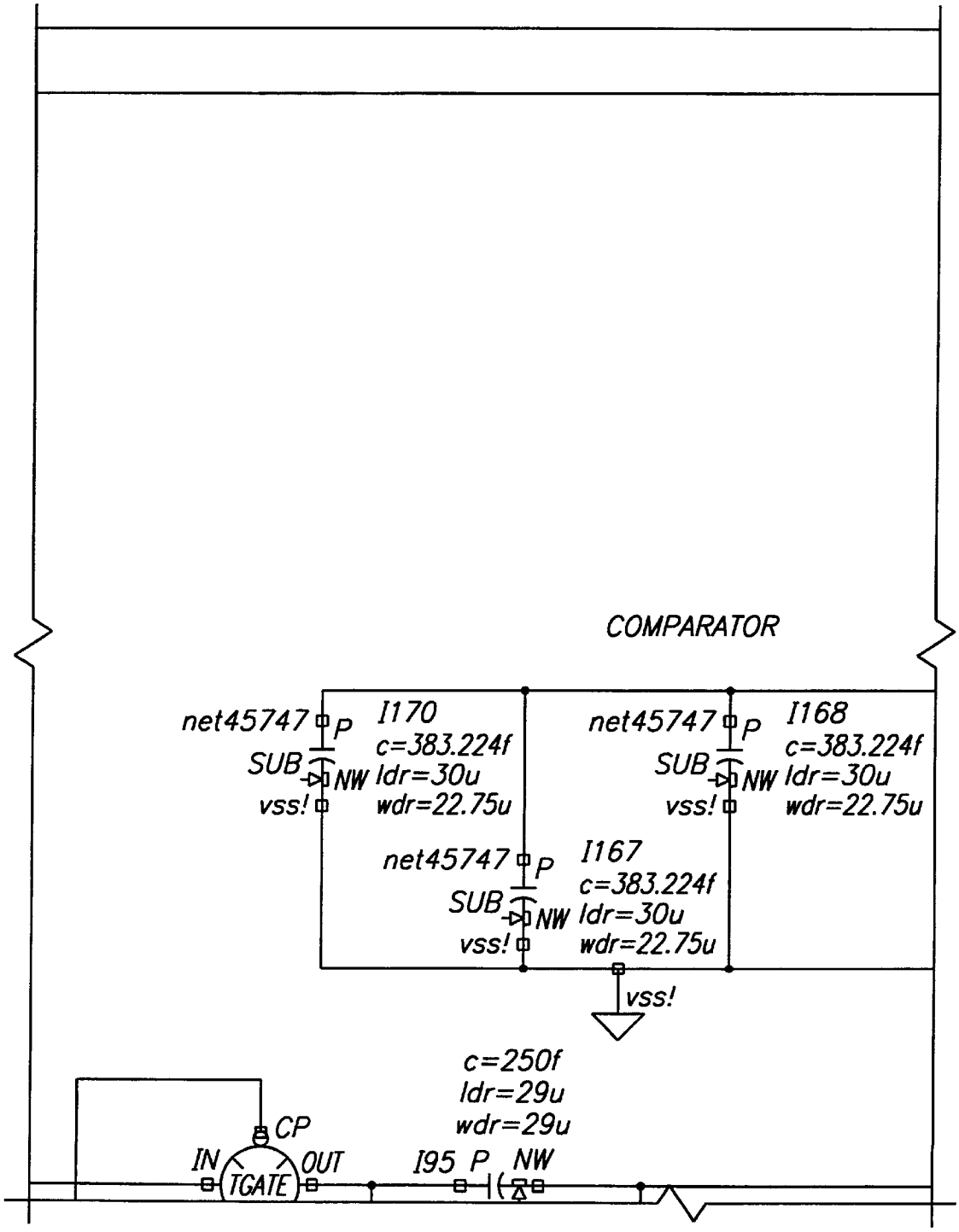

COMPARATOR
net45747
P
SUB
NW
vss!
I170
c=383.224f
ldr=30u
wdr=22.75u
net45747
P
SUB
NW
vss!
I168
c=383.224f
ldr=30u
wdr=22.75u
net45747
P
SUB
NW
vss!
I167
c=383.224f
ldr=30u
wdr=22.75u
vss!
c=250f
ldr=29u
wdr=29u
CP
IN
TGATE
OUT
I95 P NW

Fig 9.01AG

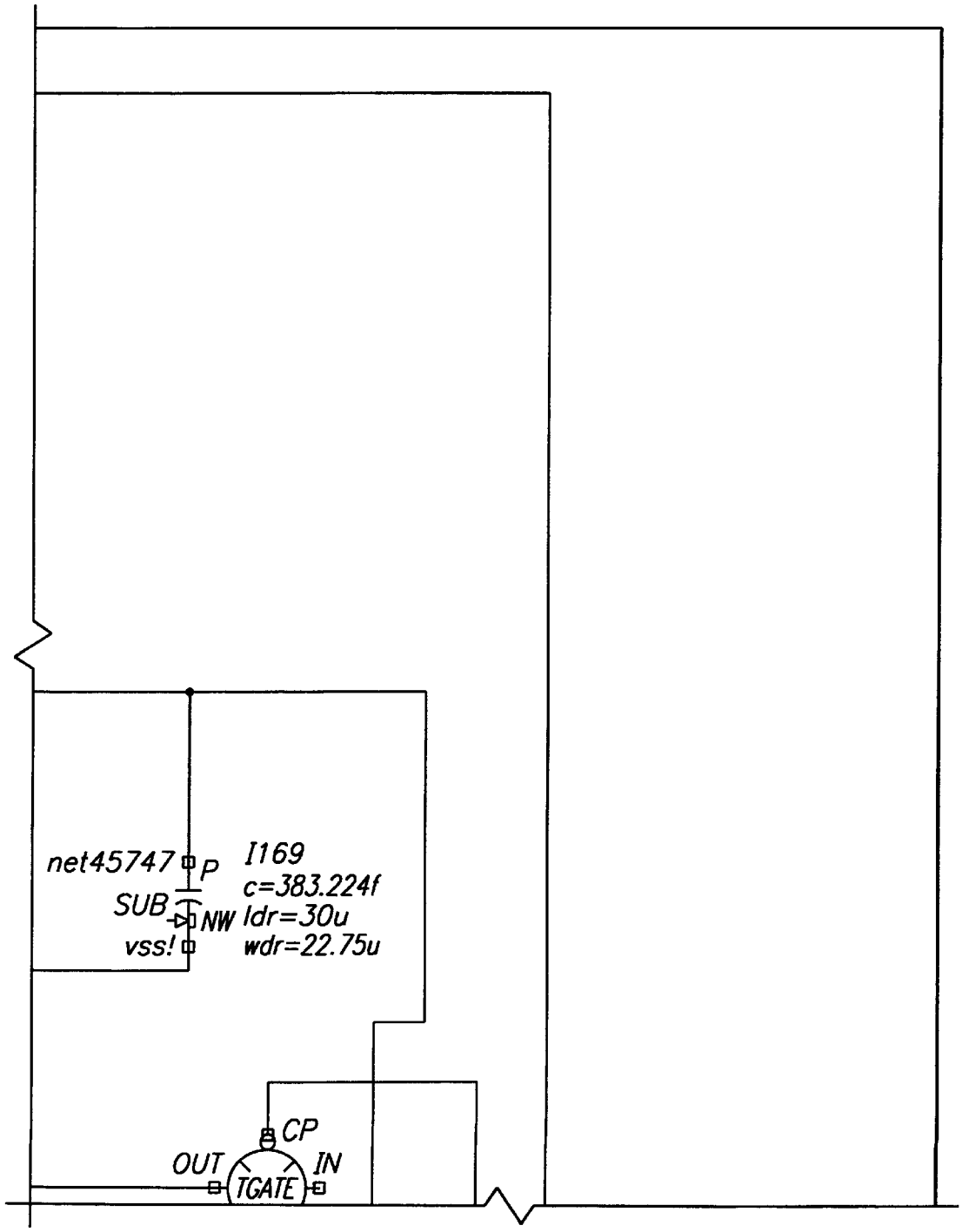

net45747
P
I169
c=383.224f
SUB
NW
ldr=30u
vss!
wdr=22.75u
CP
OUT
IN
TGATE

Fig 9.01AH

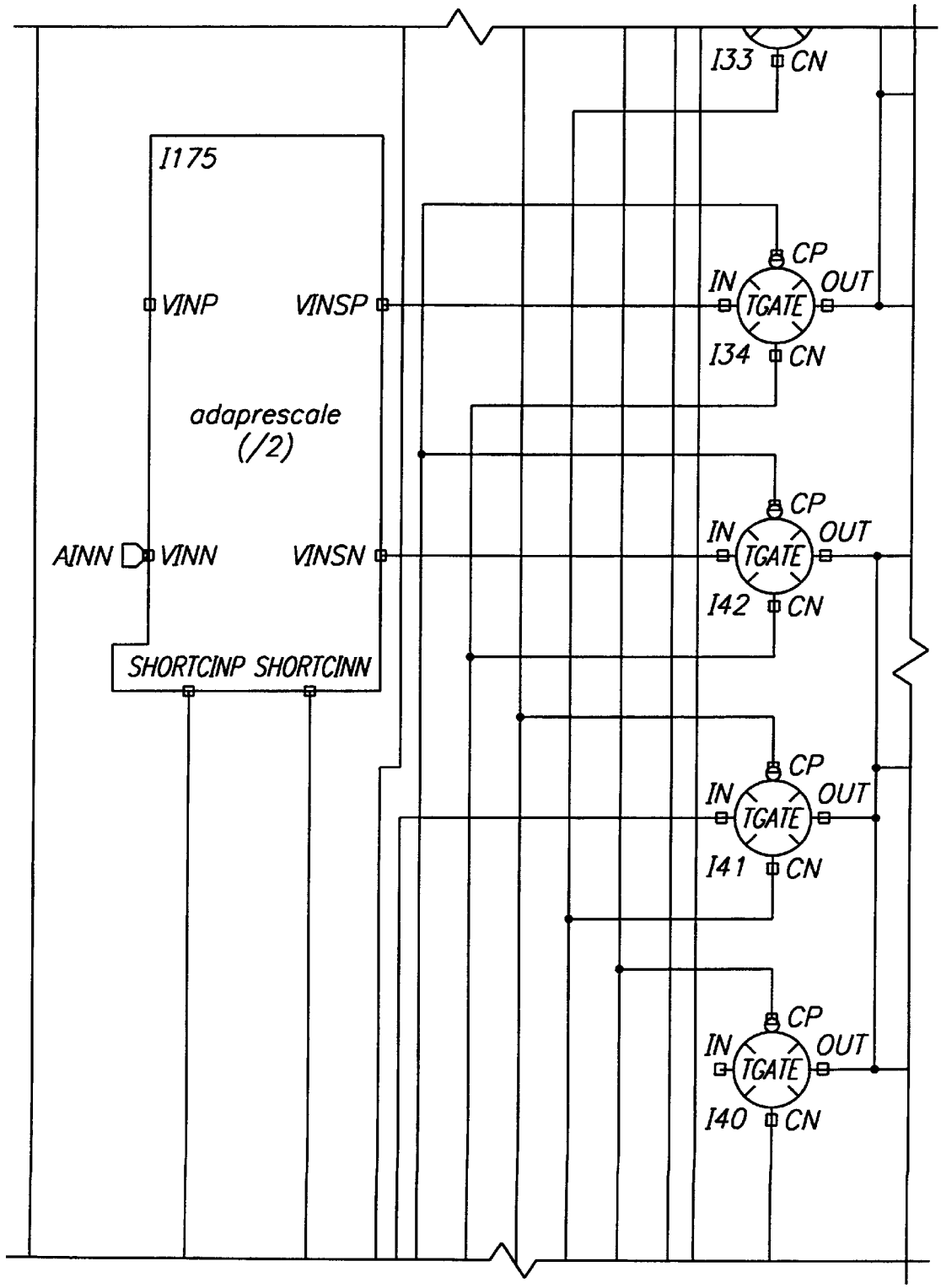

I33
CN
I175
CP
IN
OUT
TGATE
VINP
VINSP
I34
CN
adaprescale
(/2)
CP
IN
OUT
TGATE
AINN
VINN
VINSN
I42
CN
SHORTCINP
SHORTCINN
CP
IN
OUT
TGATE
I41
CN
CP
IN
OUT
TGATE
I40
CN

Fig 9.01BA

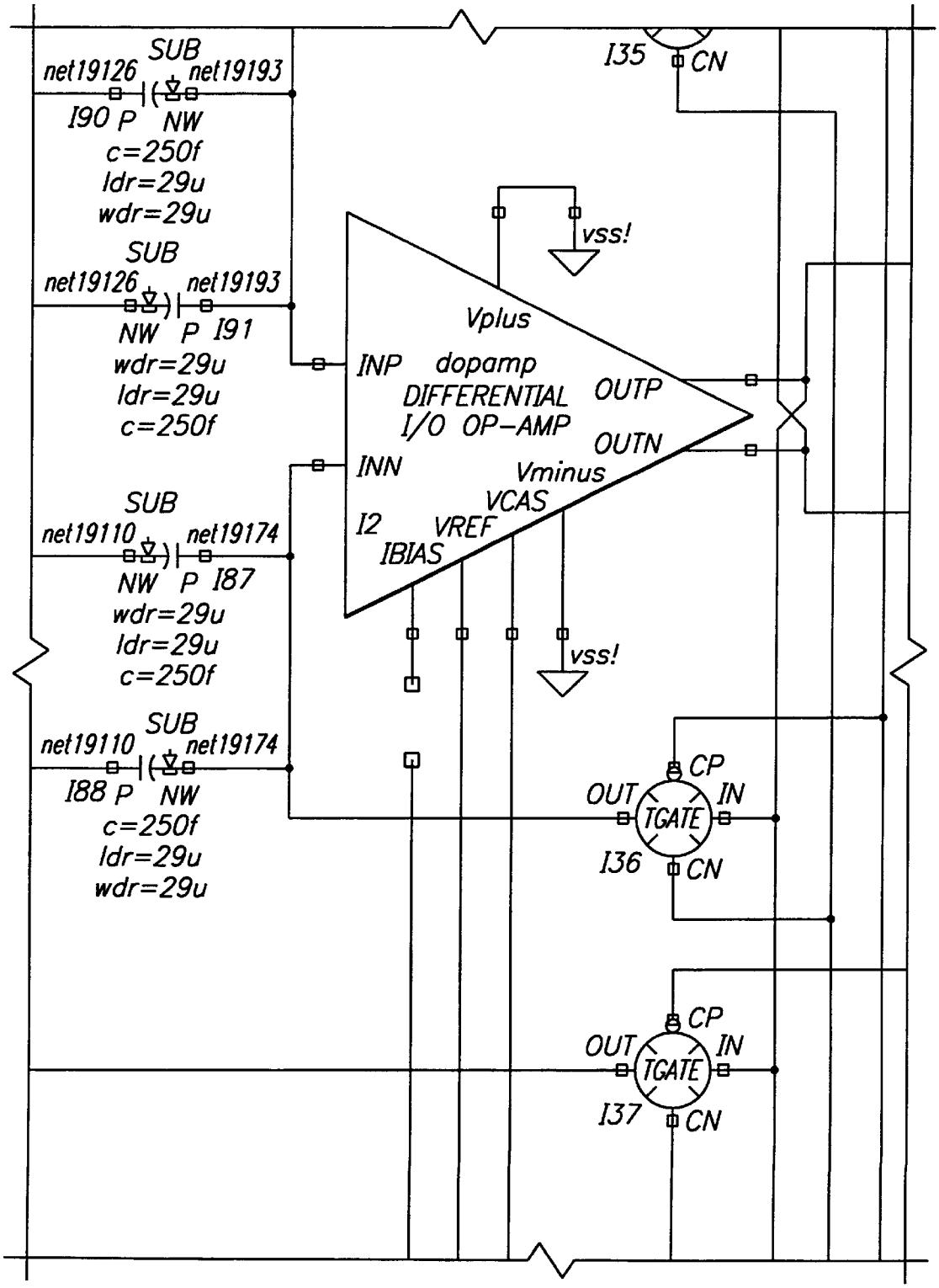

SUB
net19126
net19193
I90 P NW
c=250f
ldr=29u
wdr=29u
SUB
net19126
net19193
NW P I91
wdr=29u
ldr=29u
c=250f
SUB
net19110
net19174
NW P I87
wdr=29u
ldr=29u
c=250f
SUB
net19110
net19174
I88 P NW
c=250f
ldr=29u
wdr=29u
I35
CN
vss!
Vplus
INP
dopamp
DIFFERENTIAL
I/O OP-AMP
OUTP
OUTN
INN
Vminus
VCAS
I2
VREF
IBIAS
vss!
CP
OUT
IN
TGATE
I36
CN
CP
OUT
IN
TGATE
I37
CN

FIG 9.011BB

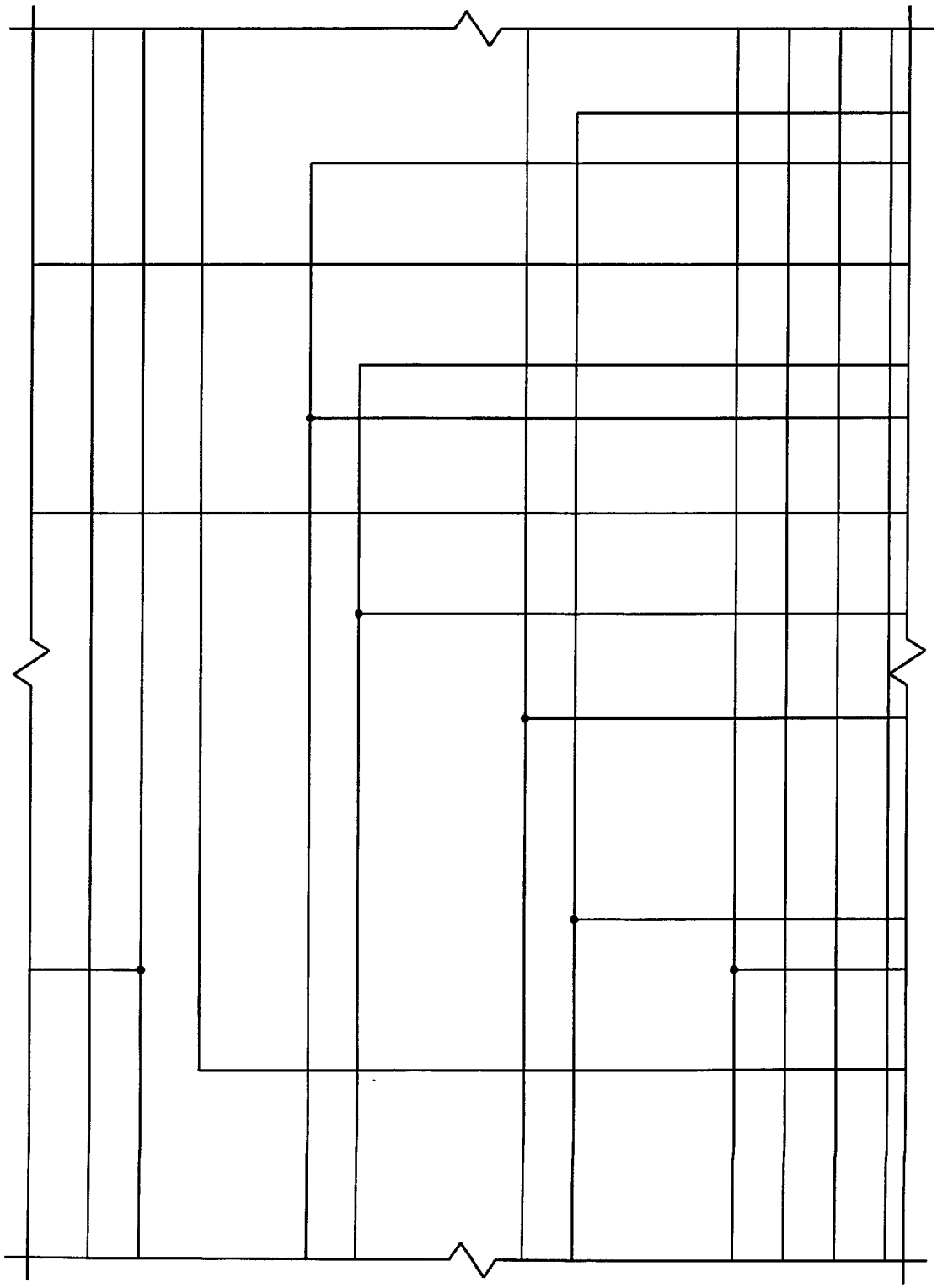


Fig 9.01BC

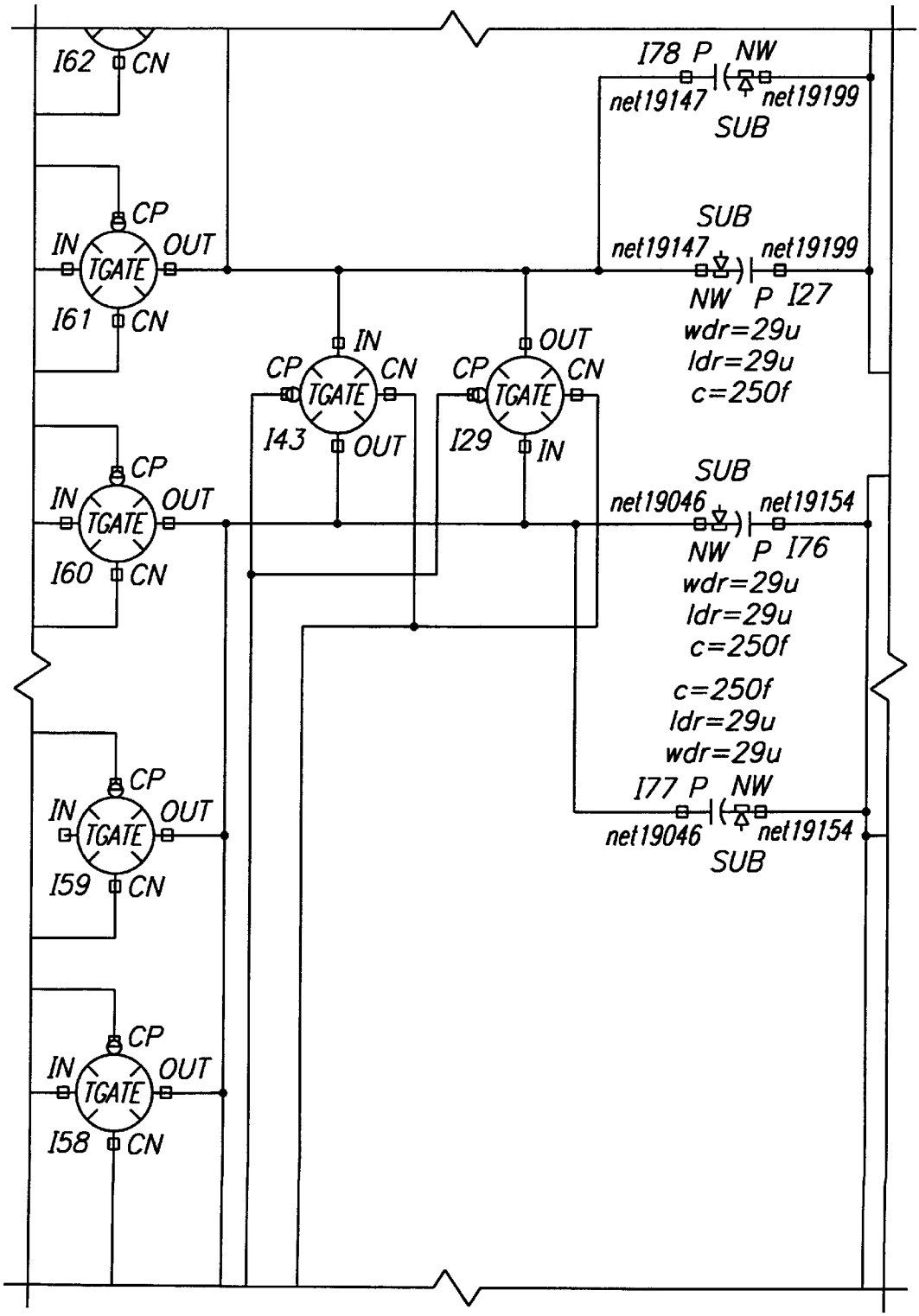

I62 CN
CP
IN TGATE OUT
I61 CN
CP
IN TGATE OUT
I60 CN
CP
IN TGATE OUT
I59 CN
CP
IN TGATE OUT
I58 CN
IN
CP TGATE CN
I43 OUT
OUT
CP TGATE CN
I29 IN
I78 P NW
net19147 net19199
SUB
SUB
net19147 net19199
NW P I27
wdr=29u
ldr=29u
c=250f
SUB
net19046 net19154
NW P I76
wdr=29u
ldr=29u
c=250f
c=250f
ldr=29u
wdr=29u
I77 P NW
net19046 net19154
SUB

Fig 9.011BD

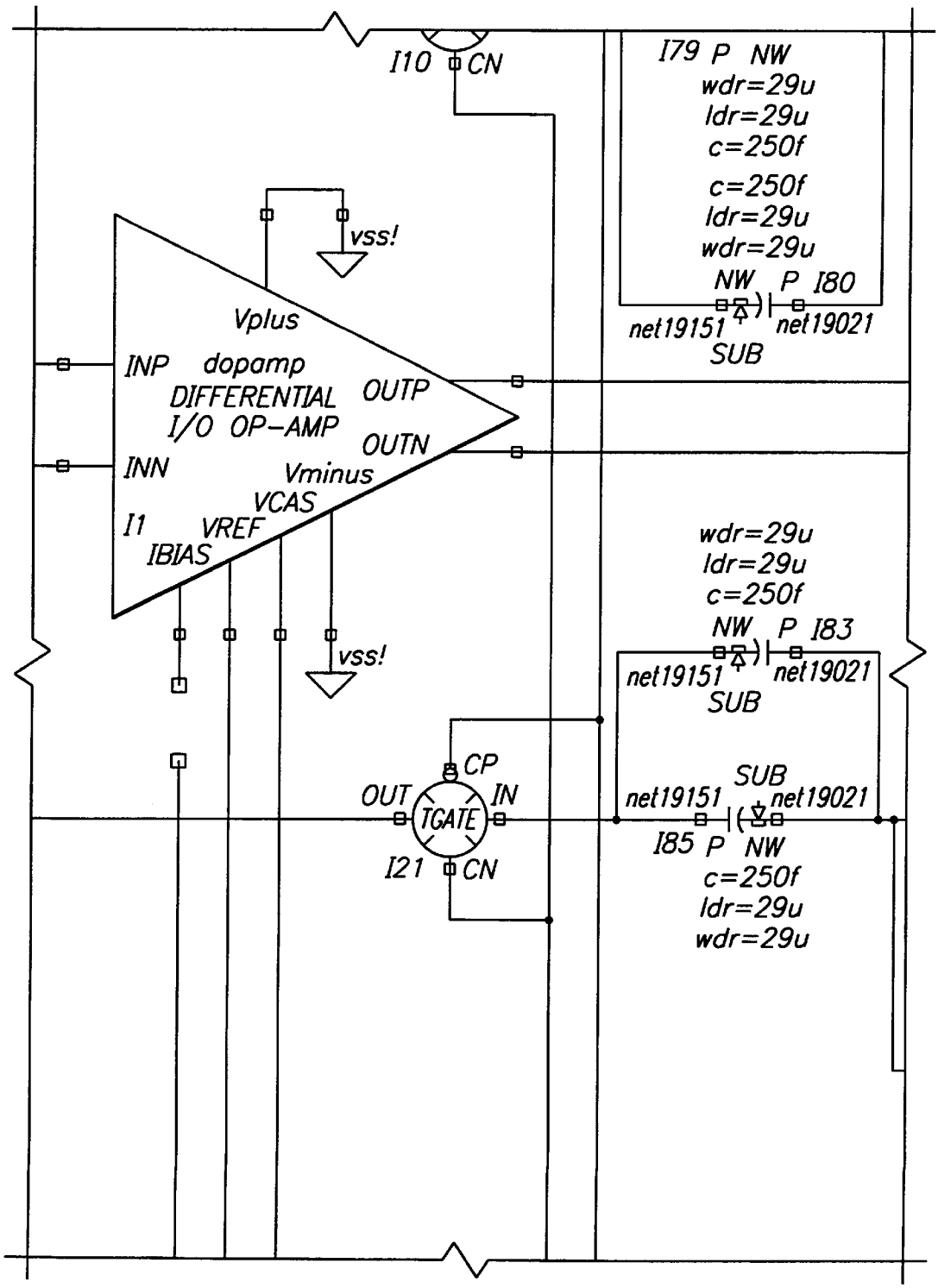

I10
CN
vss!
Vplus
INP
dopamp
DIFFERENTIAL
I/O OP-AMP
OUTP
OUTN
INN
Vminus
VCAS
I1
VREF
IBIAS
vss!
CP
OUT
IN
TGATE
I21
CN
I79 P NW
wdr=29u
ldr=29u
c=250f
c=250f
ldr=29u
wdr=29u
NW P I80
net19151
net19021
SUB
wdr=29u
ldr=29u
c=250f
NW P I83
net19151
net19021
SUB
SUB
net19151
net19021
I85 P NW
c=250f
ldr=29u
wdr=29u

FIG 9.01BE

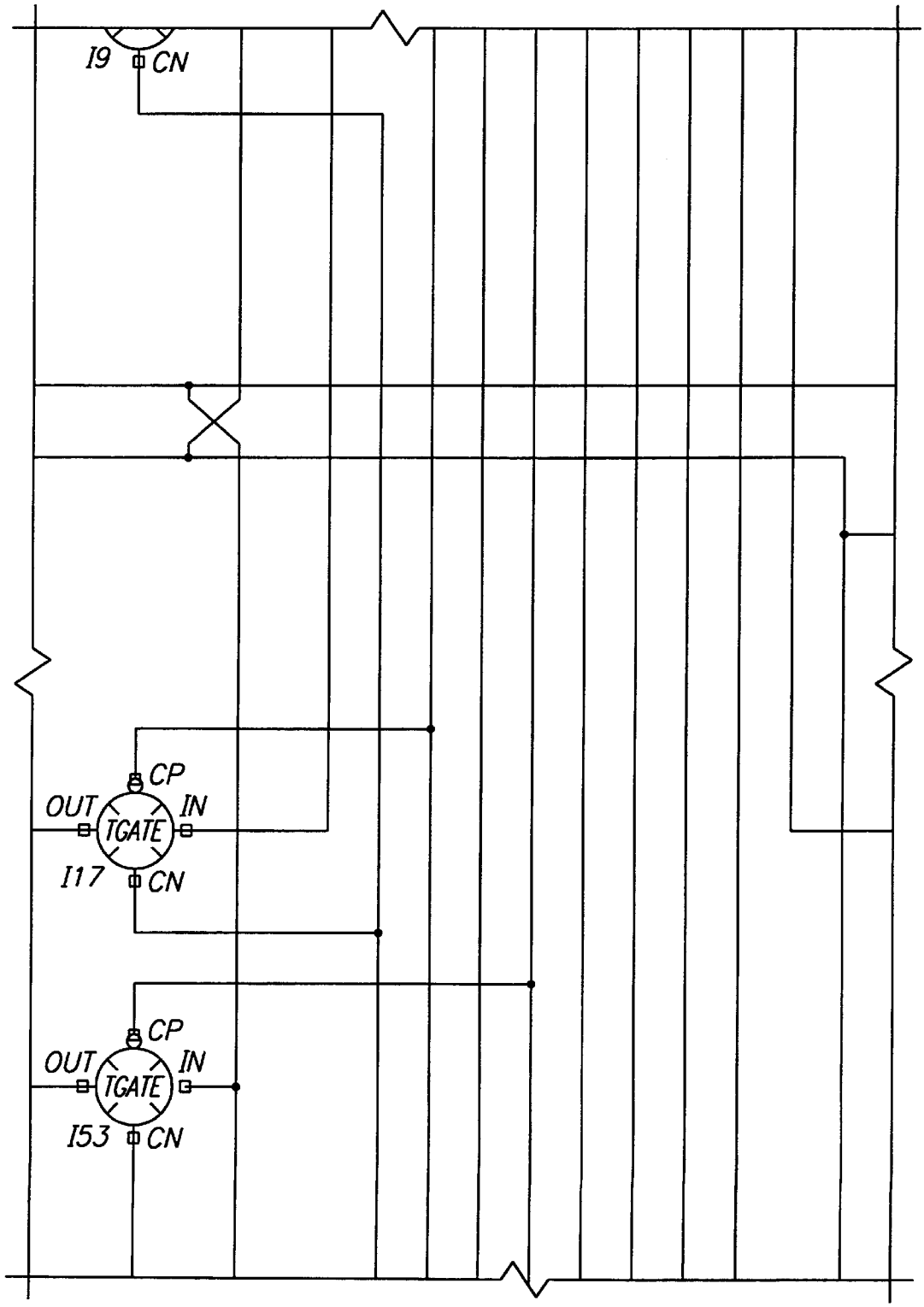


Fig 9.01BF

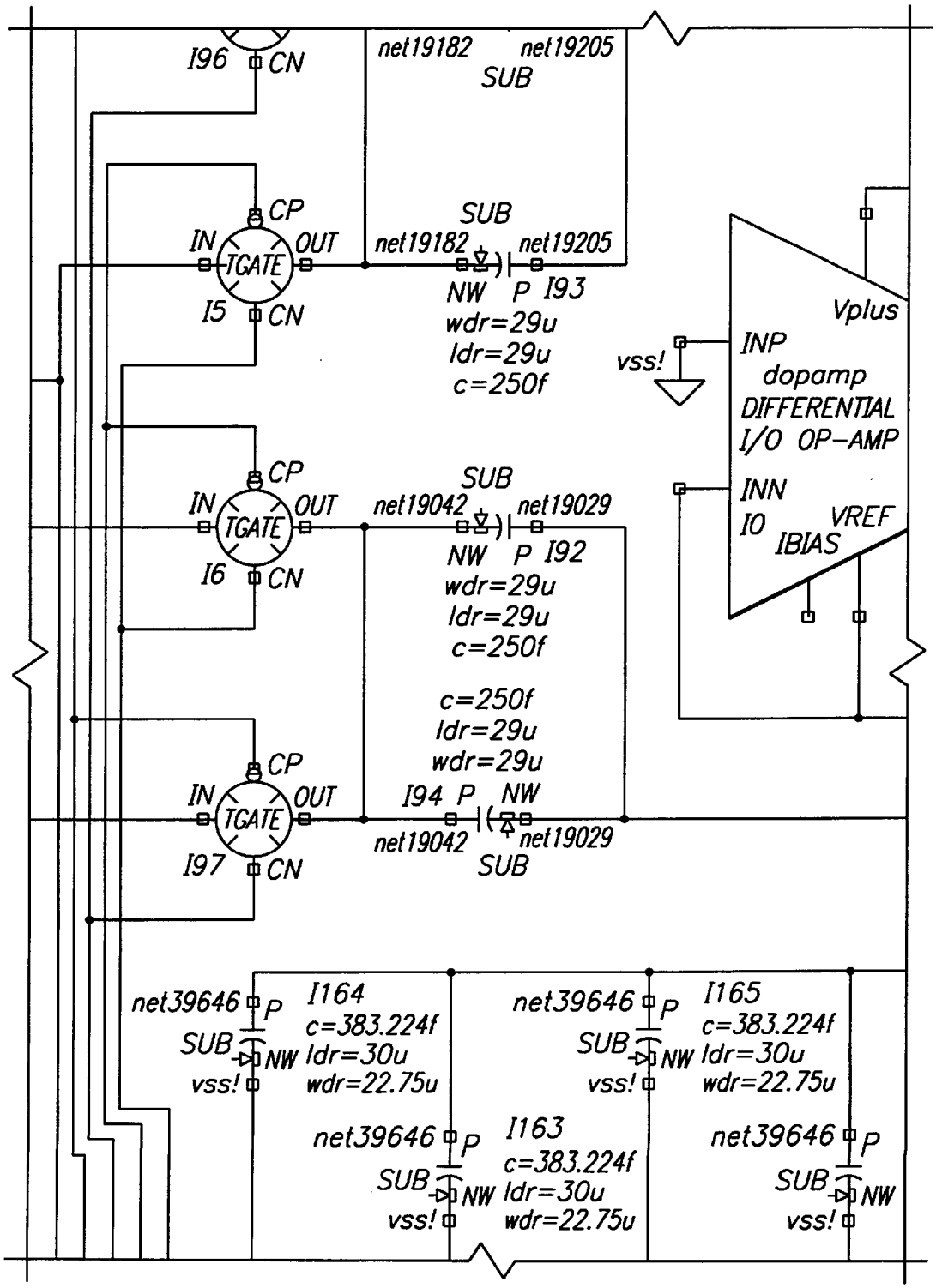

I96
CN
net19182
net19205
SUB
CP
IN
OUT
TGATE
I5
CN
SUB
net19182
net19205
NW P I93
wdr=29u
ldr=29u
c=250f
vss!
Vplus
INP
dopamp
DIFFERENTIAL
I/O OP-AMP
INN
IO
VREF
IBIAS
CP
IN
OUT
TGATE
I6
CN
SUB
net19042
net19029
NW P I92
wdr=29u
ldr=29u
c=250f
c=250f
ldr=29u
wdr=29u
CP
IN
OUT
TGATE
I97
CN
I94 P NW
net19042
net19029
SUB
net39646
P
SUB
NW
vss!
I164
c=383.224f
ldr=30u
wdr=22.75u
net39646
P
SUB
NW
vss!
I165
c=383.224f
ldr=30u
wdr=22.75u
net39646
P
SUB
NW
vss!
I163
c=383.224f
ldr=30u
wdr=22.75u
net39646
P
SUB
NW
vss!

Fig 9.01186

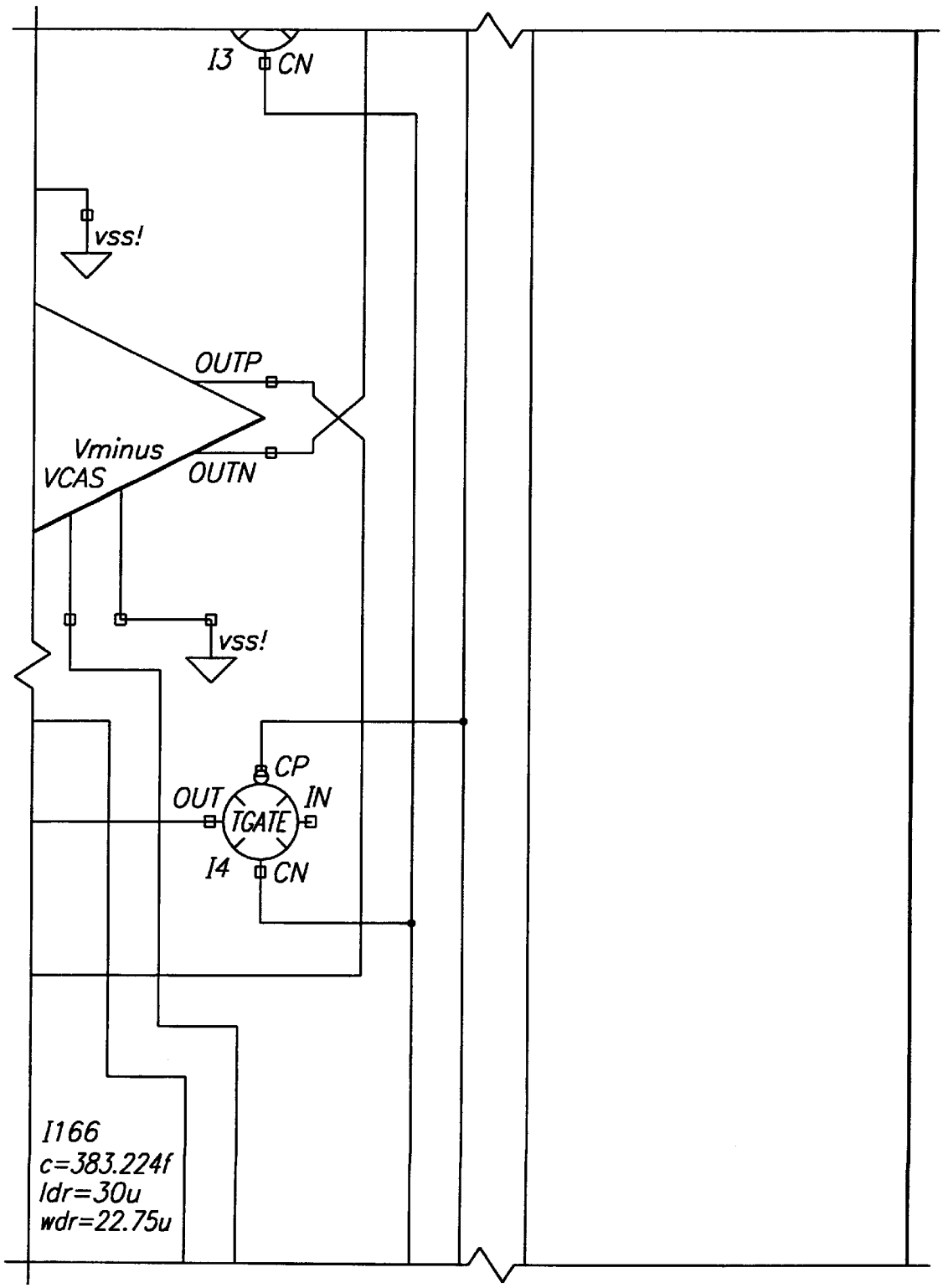

I3
CN
vss!
OUTP
Vminus
VCAS
OUTN
vss!
CP
OUT
IN
TGATE
I4
CN
I166
c=383.224f
ldr=30u
wdr=22.75u

Fig 9.01BH

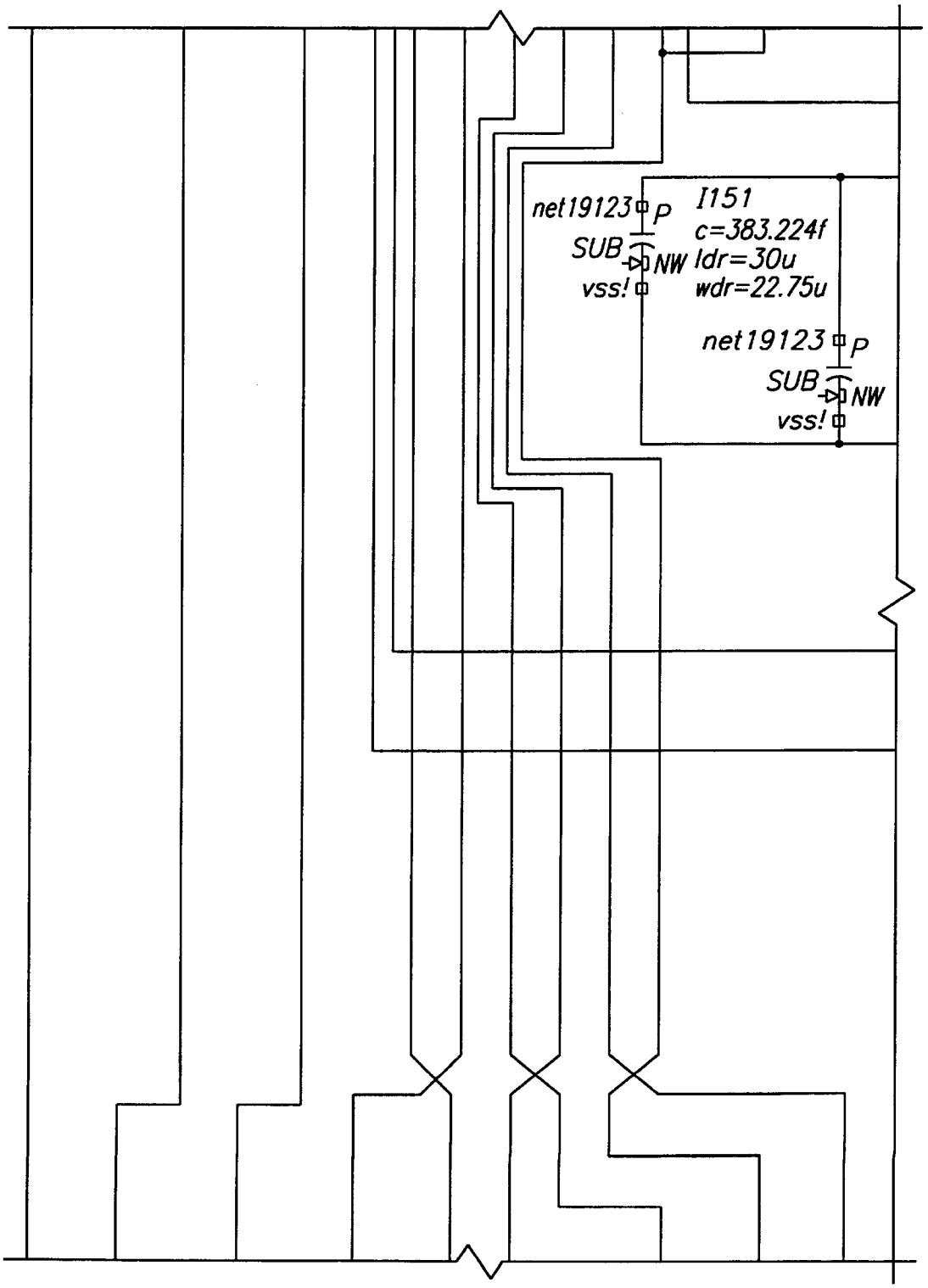

net19123
P
SUB
NW
vss!
I151
c=383.224f
ldr=30u
wdr=22.75u
net19123
P
SUB
NW
vss!

Fig 9.01CA

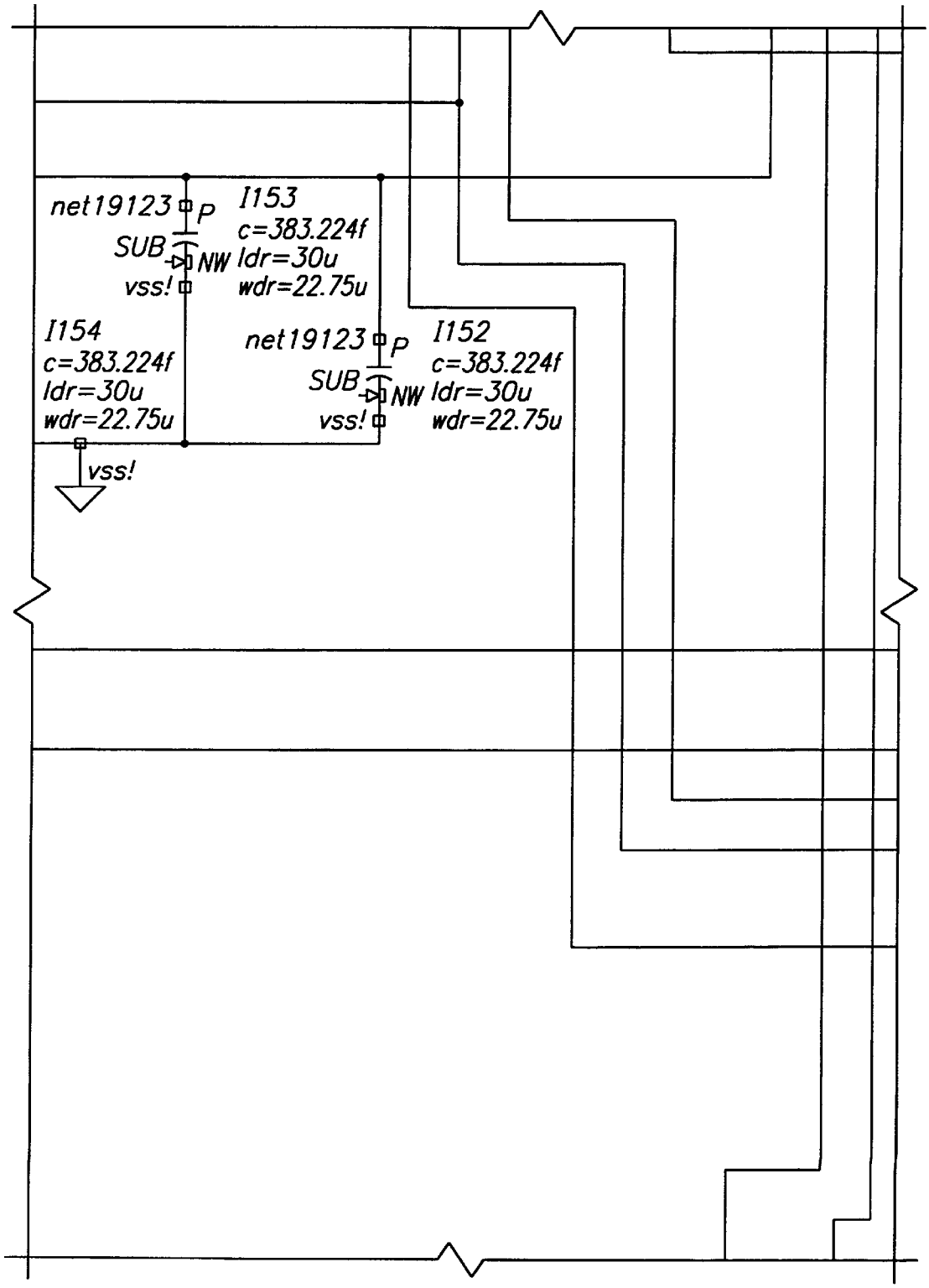

net19123
P
SUB
NW
vss!
I153
c=383.224f
ldr=30u
wdr=22.75u
I154
c=383.224f
ldr=30u
wdr=22.75u
vss!
net19123
P
SUB
NW
vss!
I152
c=383.224f
ldr=30u
wdr=22.75u

Fig 9.01CB

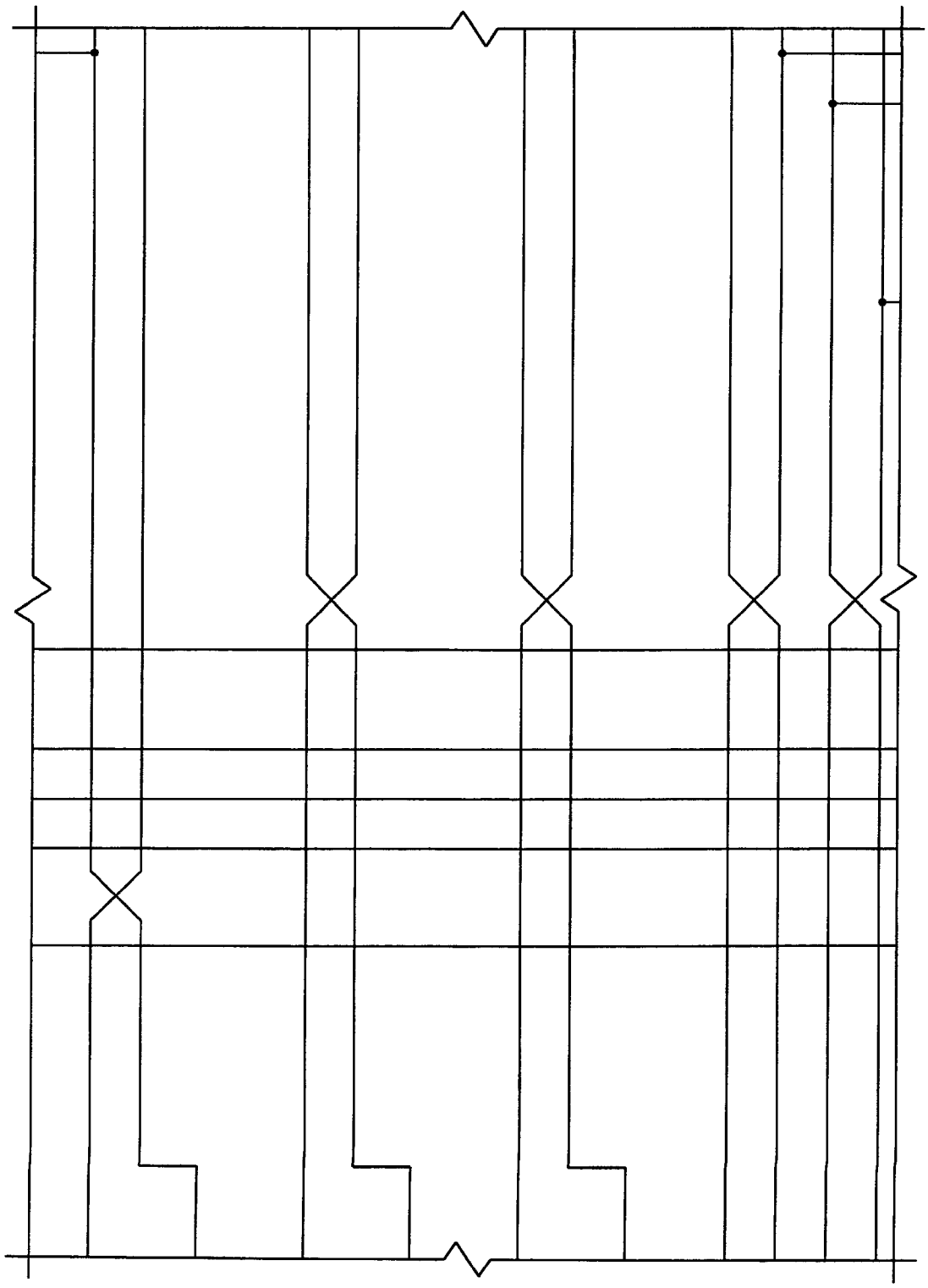


Fig 9.01CC

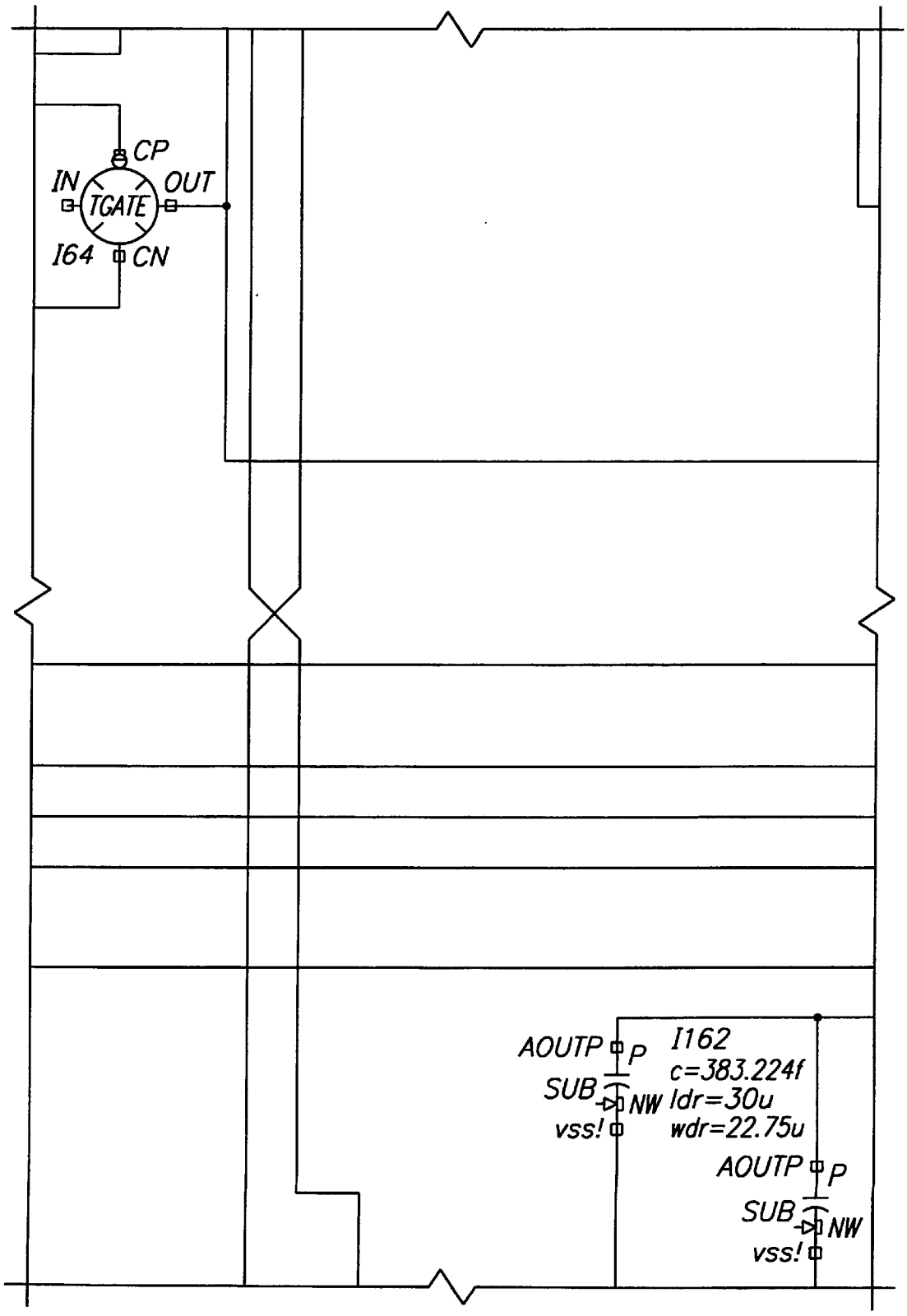

CP
IN
TGATE
OUT
I64
CN
AOUTP
P
SUB
NW
vss!
I162
c=383.224f
ldr=30u
wdr=22.75u
AOUTP
P
SUB
NW
vss!

Fig 9.01CD

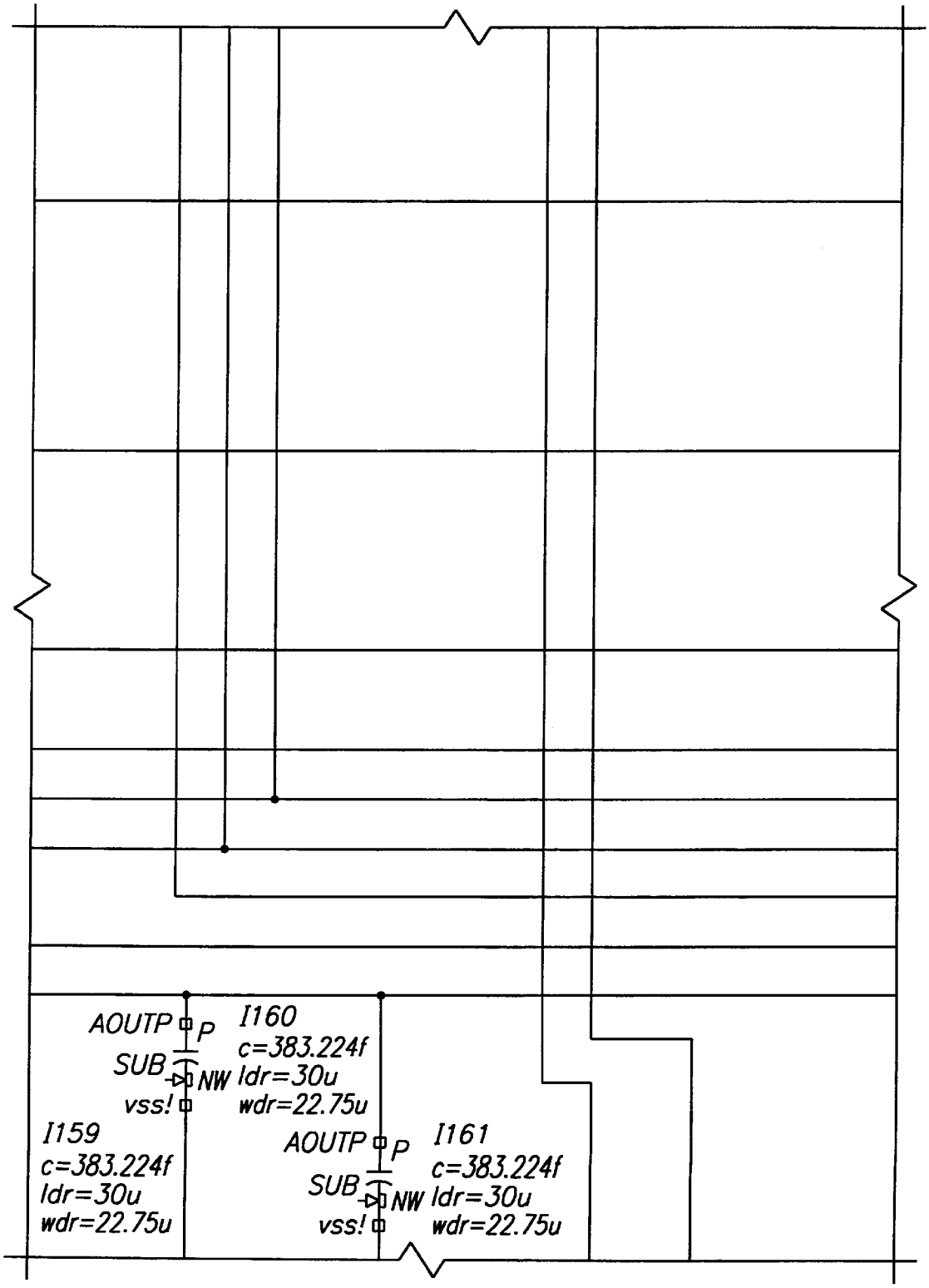

AOUTP
P
SUB
NW
vss!
I160
c=383.224f
ldr=30u
wdr=22.75u
I159
c=383.224f
ldr=30u
wdr=22.75u
AOUTP
P
SUB
NW
vss!
I161
c=383.224f
ldr=30u
wdr=22.75u

Fig 9.0116

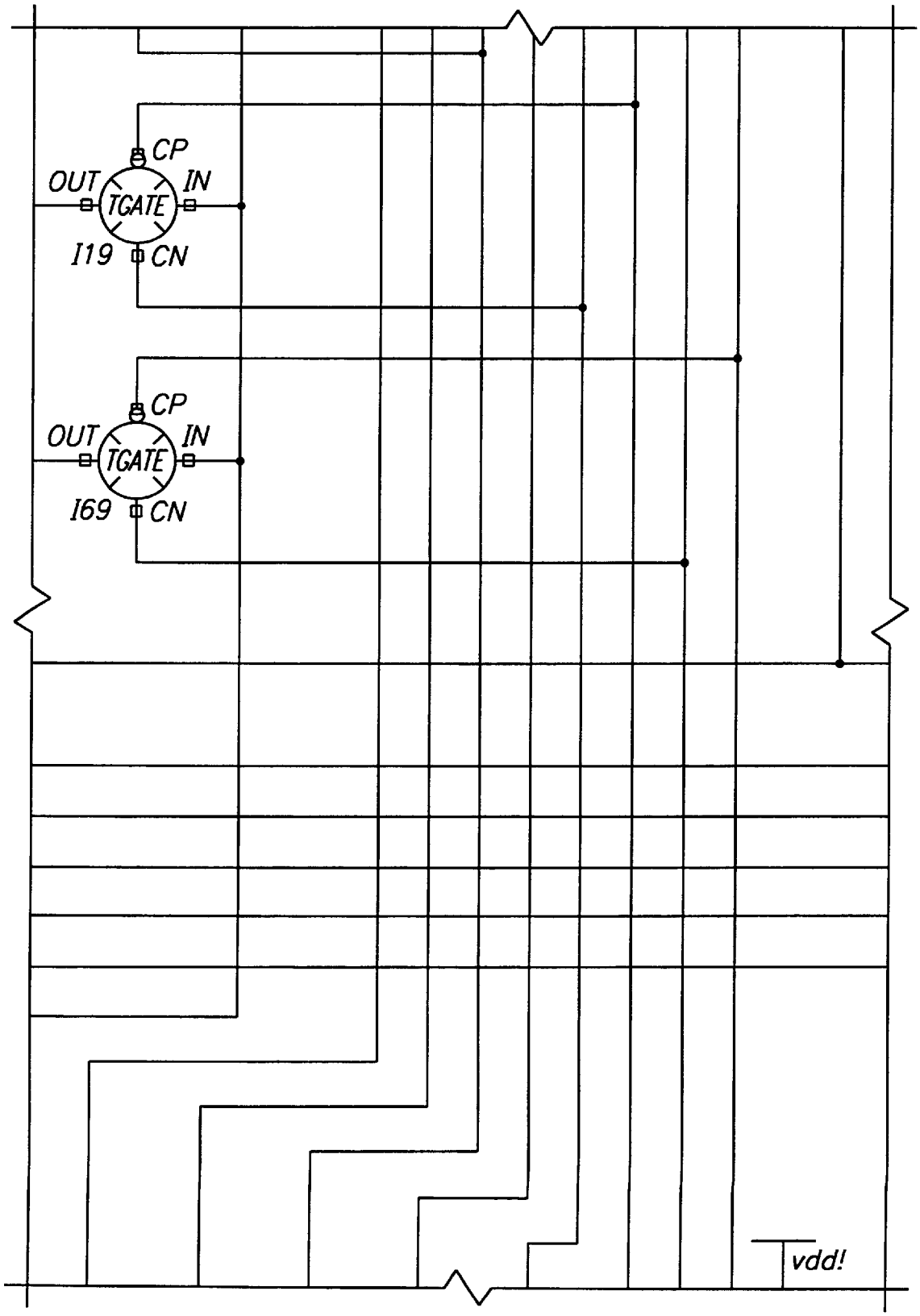


Fig 9.011CF

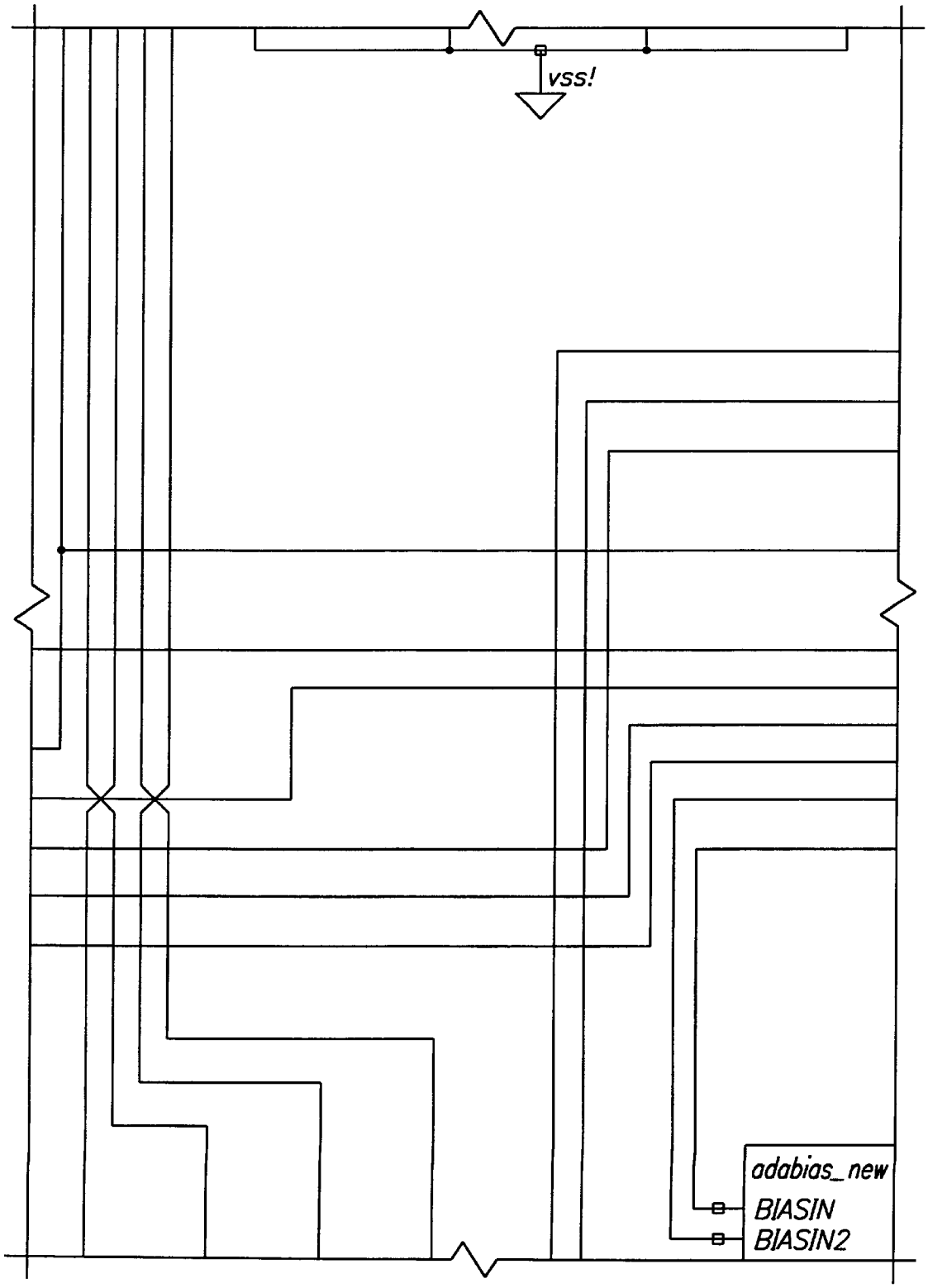


Fig 9.01C6

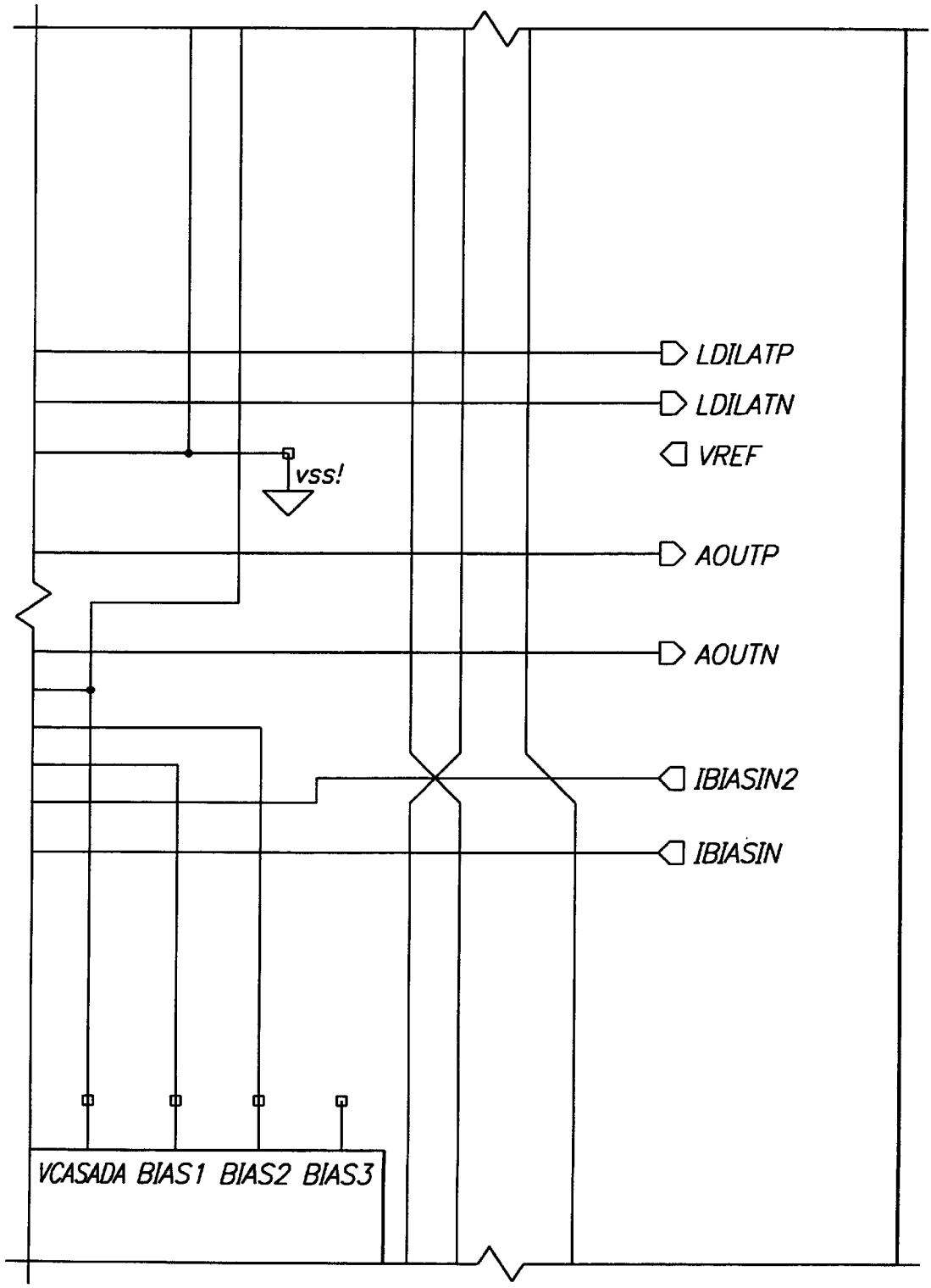

LDILATP
LDILATN
VREF
vss!
AOUTP
AOUTN
IBIASIN2
IBIASIN
VCASADA BIAS1 BIAS2 BIAS3

Fig 9.011CH

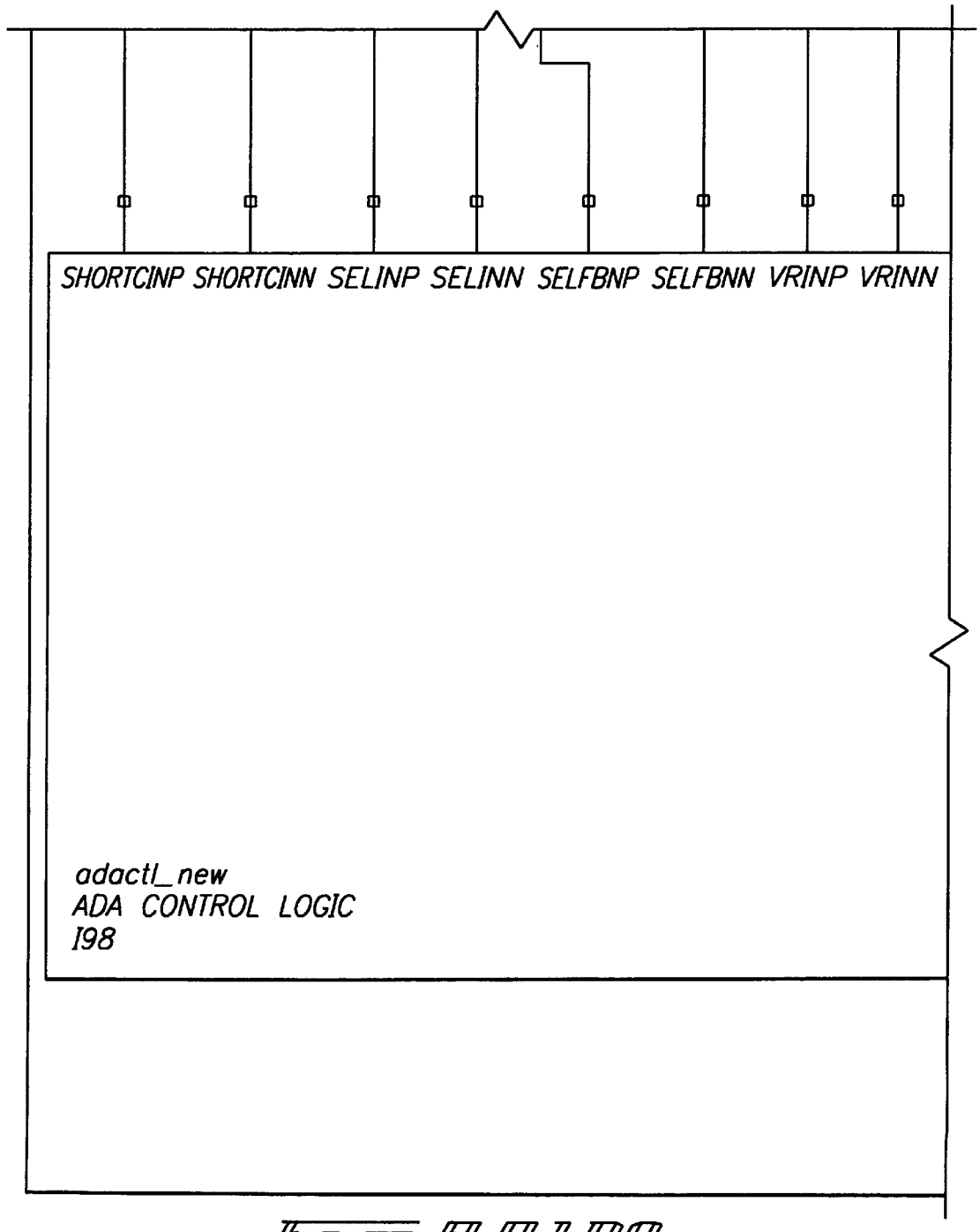

SHORTCINP SHORTCINN SELINP SELINN SELFBNP SELFBNN VRINP VRINN
adactl_new
ADA CONTROL LOGIC
I98

Fig 9.01DA

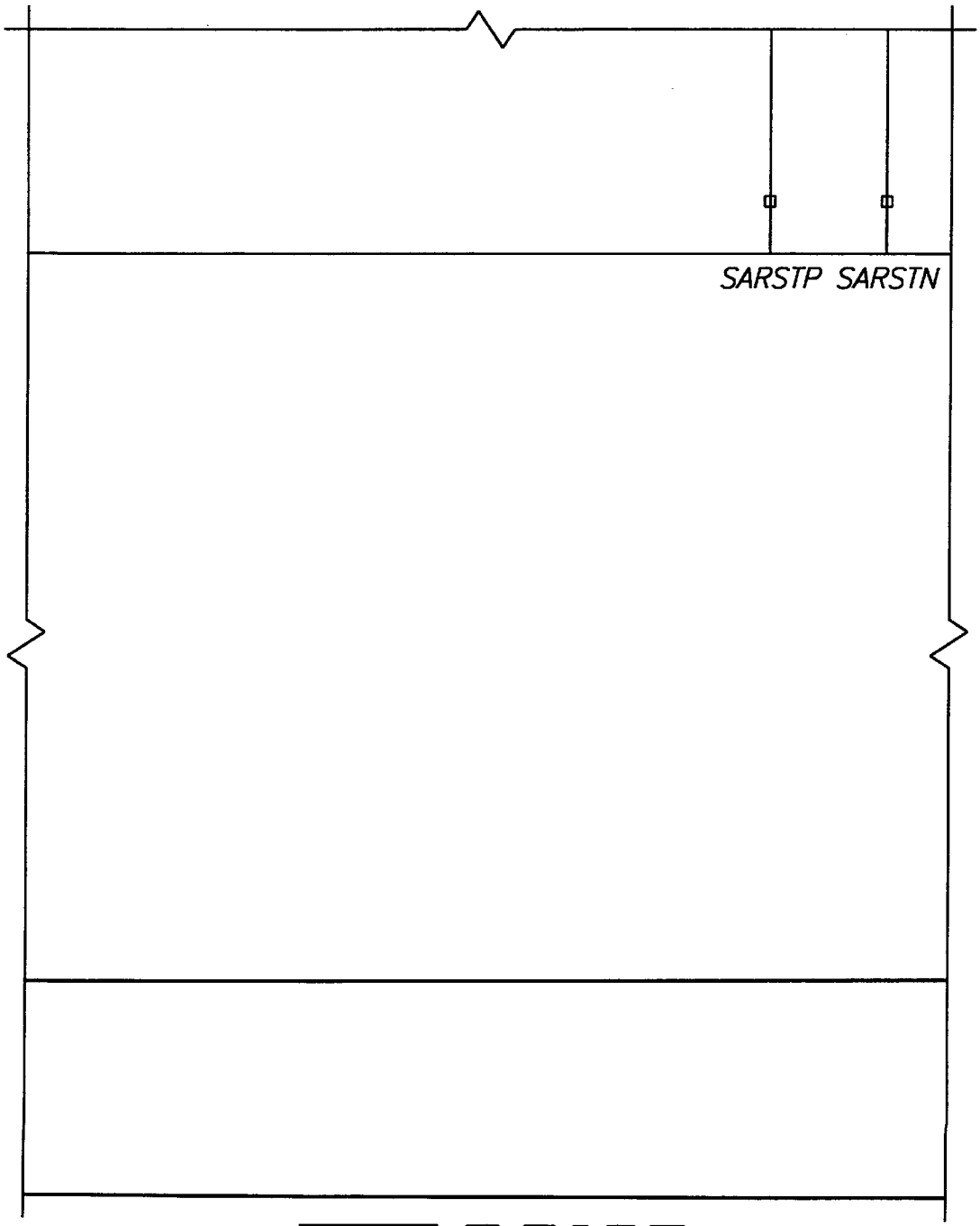


Fig 9.0108

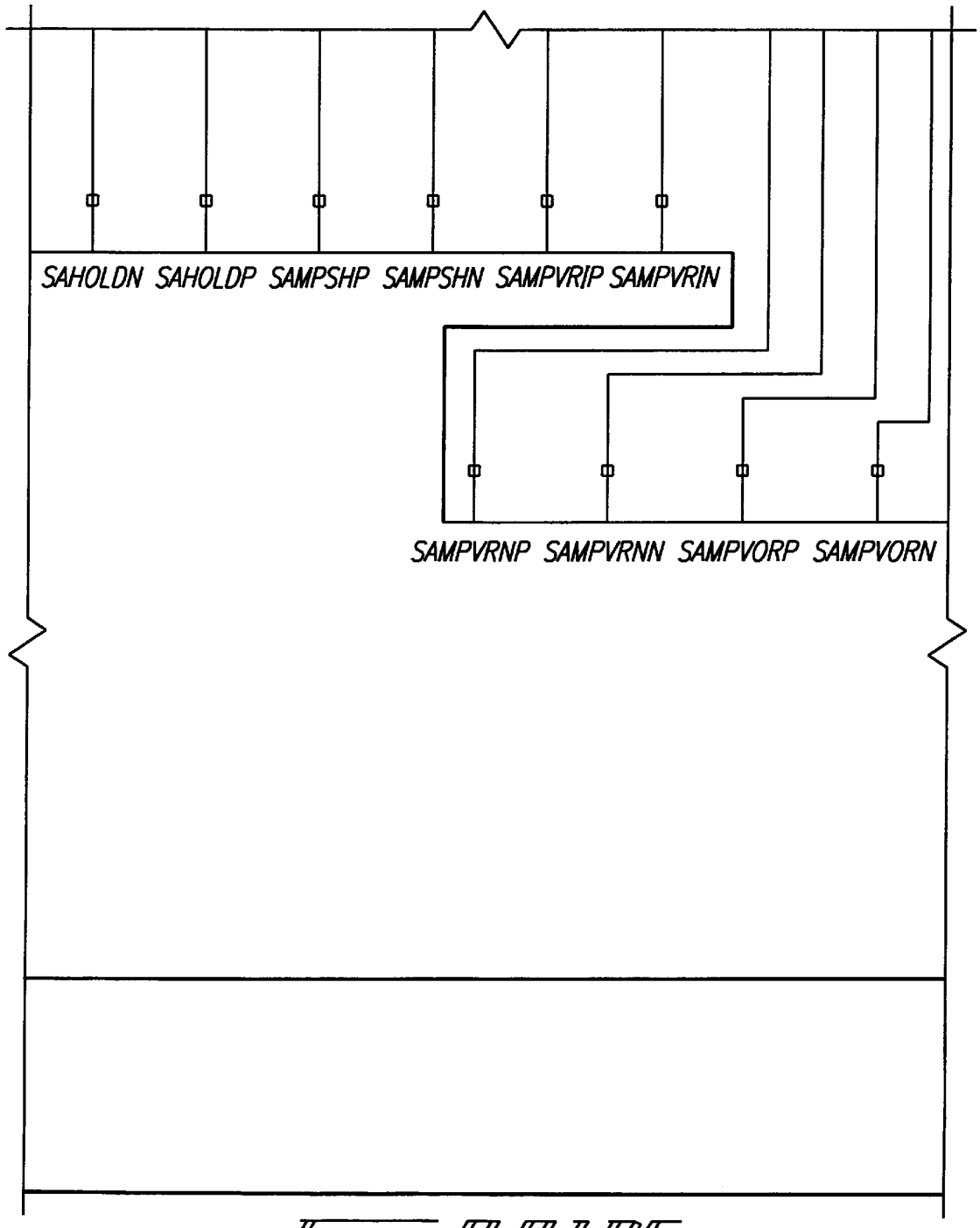

SAHOLDN SAHOLDP SAMPSHP SAMPSHN SAMPVRIP SAMPVRIN
SAMPVRNP SAMPVRNN SAMPVORP SAMPVORN

Fig 9.001DC

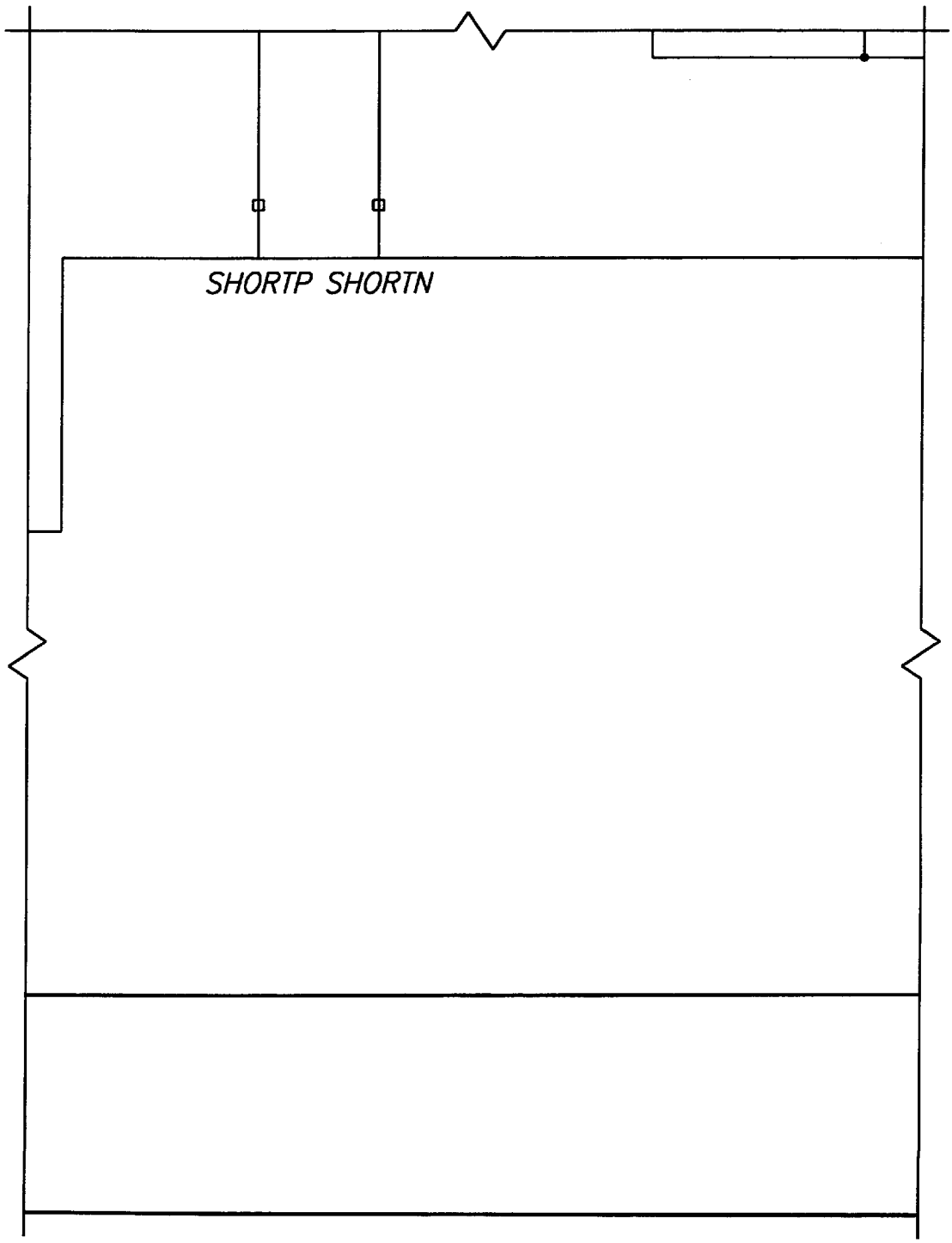


Fig 9.0100

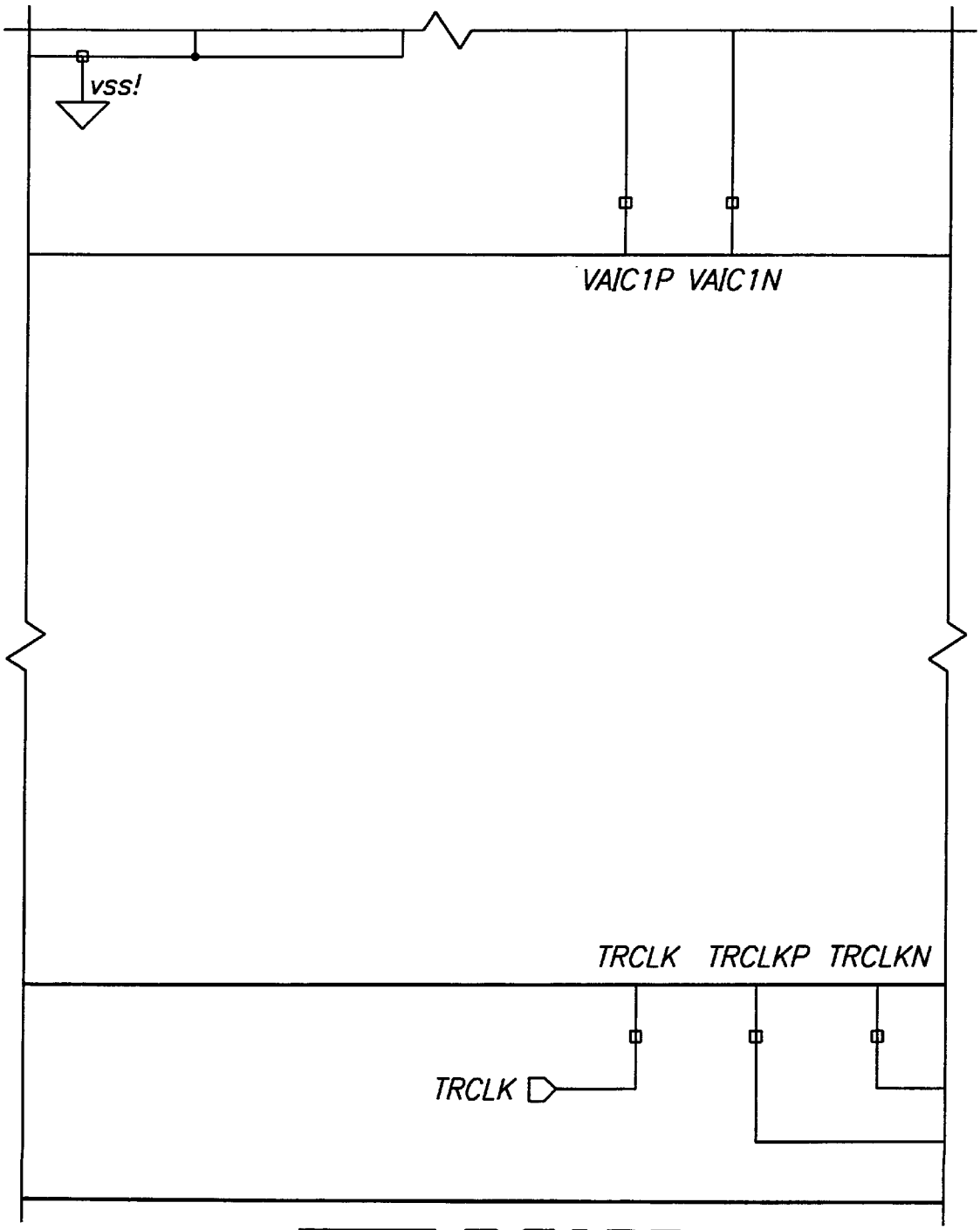


Fig 9.011DE

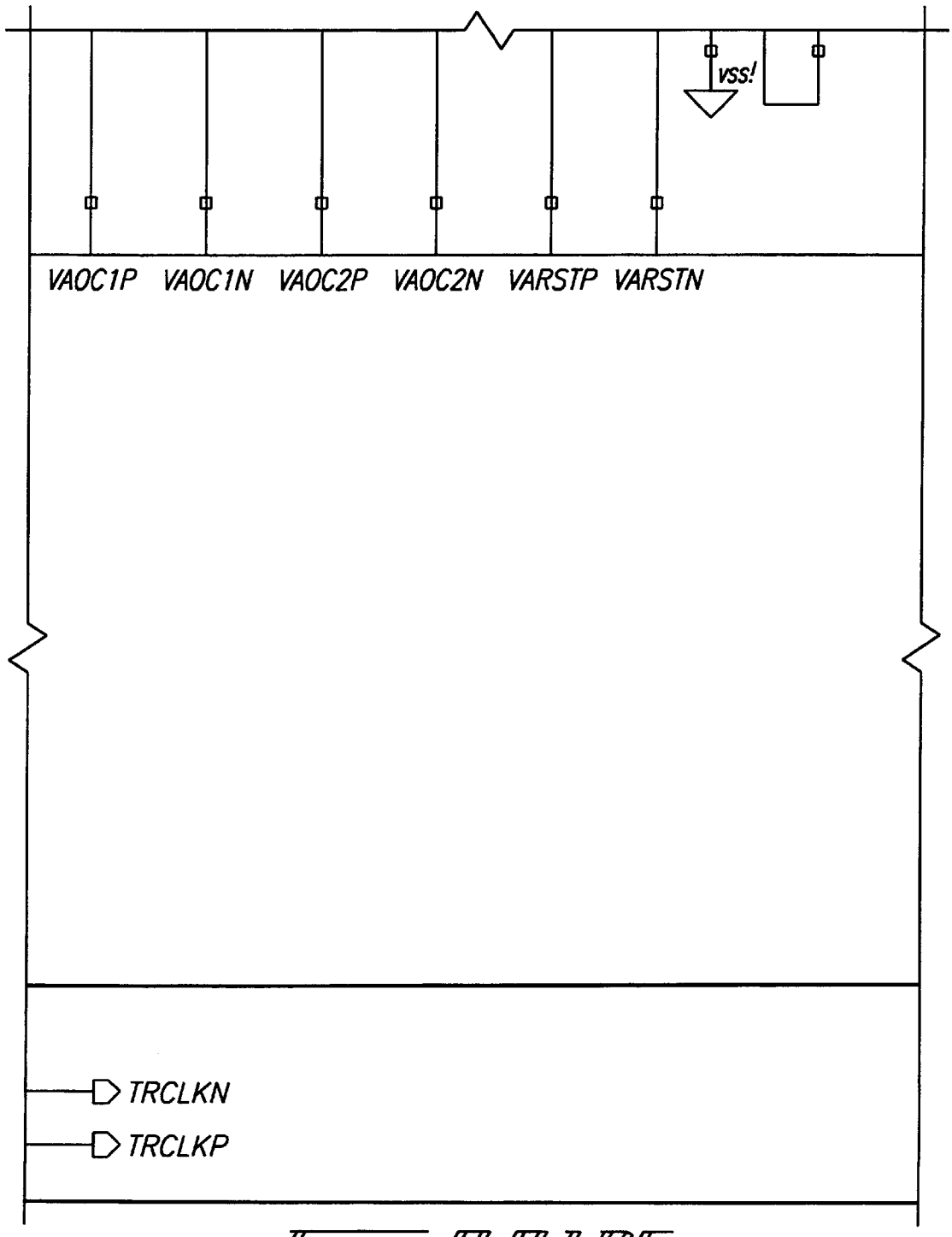

VSS!
VAOC1P
VAOC1N
VAOC2P
VAOC2N
VARSTP
VARSTN
TRCLKN
TRCLKP

Fig 9.01DF

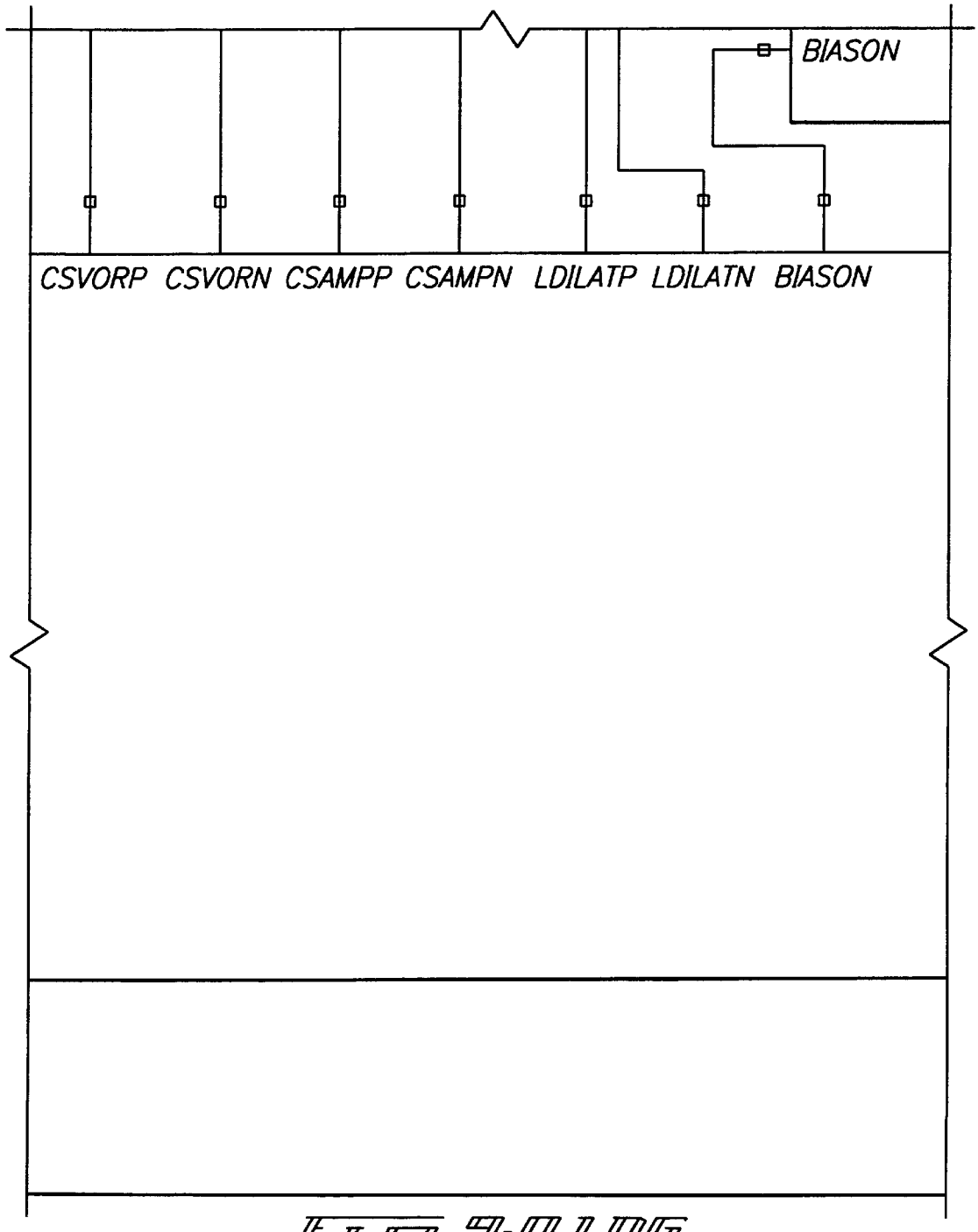

BIASON
CSVORP CSVORN CSAMPP CSAMPN LDILATP LDILATN BIASON

Fig 9.0110G

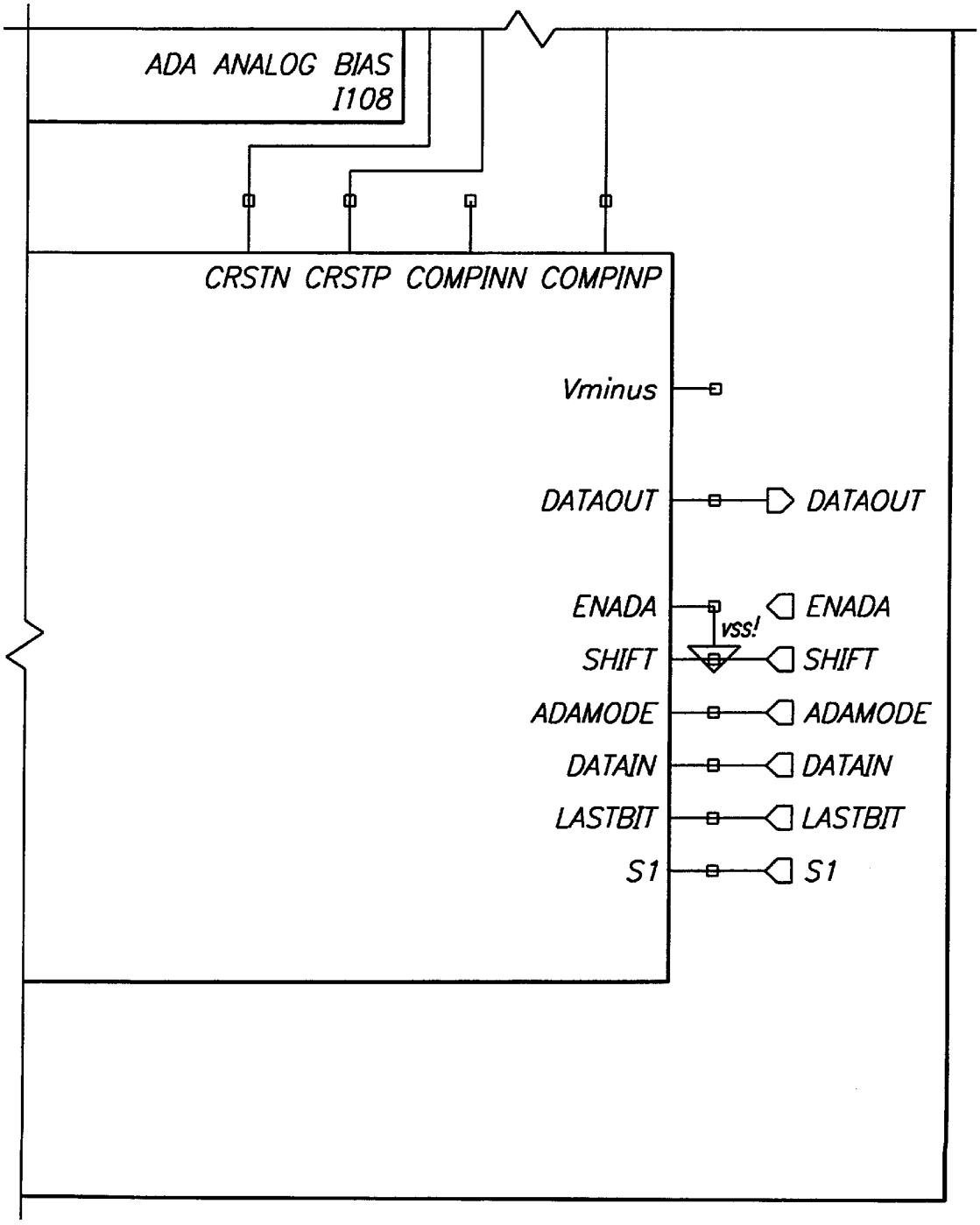

ADA ANALOG BIAS
I108
CRSTN CRSTP COMPINN COMPINP
Vminus
DATAOUT
DATAOUT
ENADA
ENADA
vss!
SHIFT
SHIFT
ADAMODE
ADAMODE
DATAIN
DATAIN
LASTBIT
LASTBIT
S1
S1

Fig 9.01DH

9.0101AA	9.0101AB	9.0101AC	9.0101AD	9.0101AE	9.0101AF	9.0101AG	9.0101AH	9.0101AI	9.0101AJ	9.0101AK
9.0101BA	9.0101BB	9.0101BC	9.0101BD	9.0101BE	9.0101BF	9.0101BG	9.0101BH	9.0101BI	9.0101BJ	9.0101BK
9.0101CA	9.0101CB	9.0101CC	9.0101CD	9.0101CE	9.0101CF	9.0101CG	9.0101CH	9.0101CI	9.0101CJ	9.0101CK

FIG 9.0101

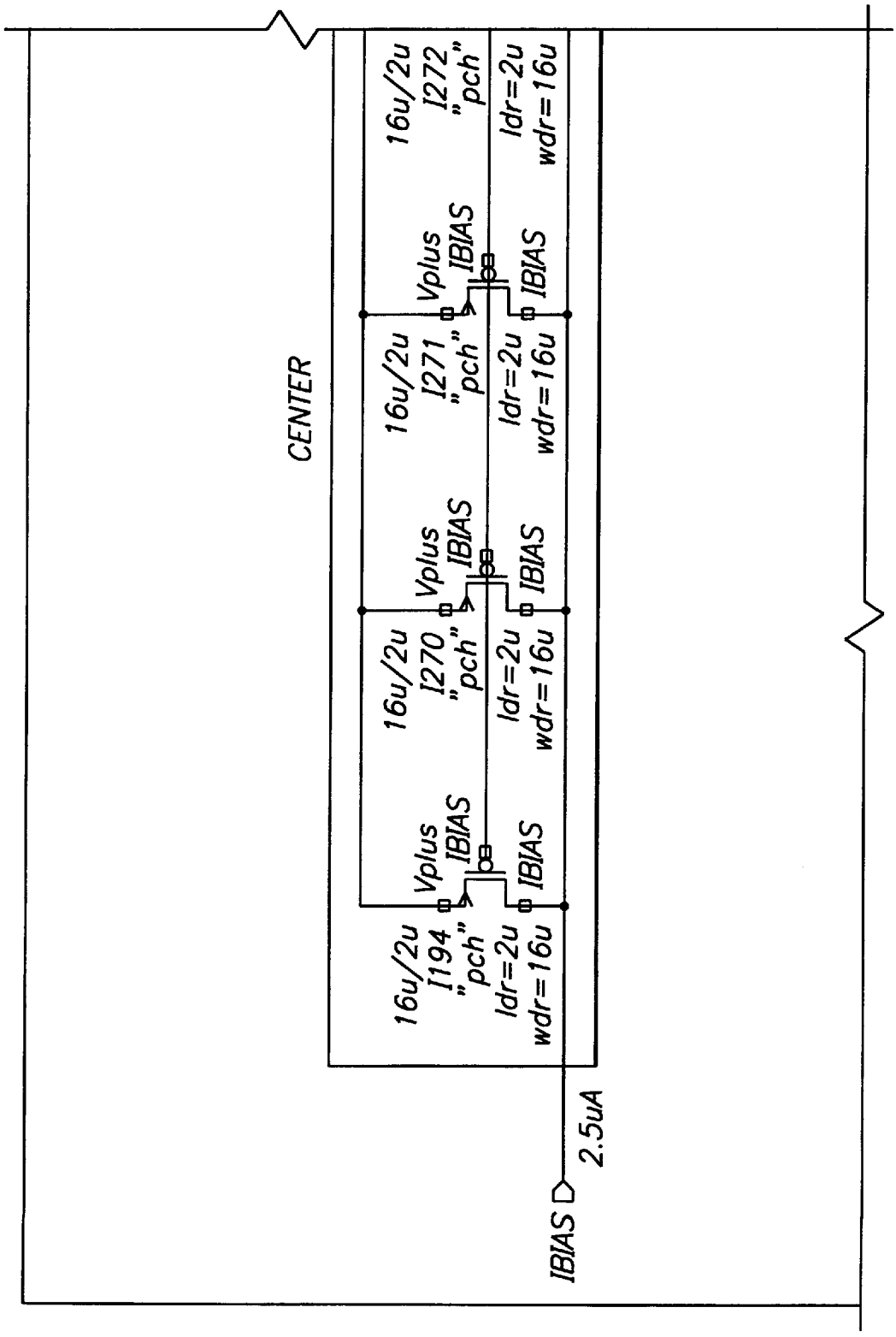

CENTER
16u/2u
I272
"pch"
ldr=2u
wdr=16u
Vplus
IBIAS
16u/2u
I271
"pch"
ldr=2u
wdr=16u
Vplus
IBIAS
16u/2u
I270
"pch"
ldr=2u
wdr=16u
Vplus
IBIAS
16u/2u
I194
"pch"
ldr=2u
wdr=16u
IBIAS
2.5uA
IBIAS

FIG. 9.00110A

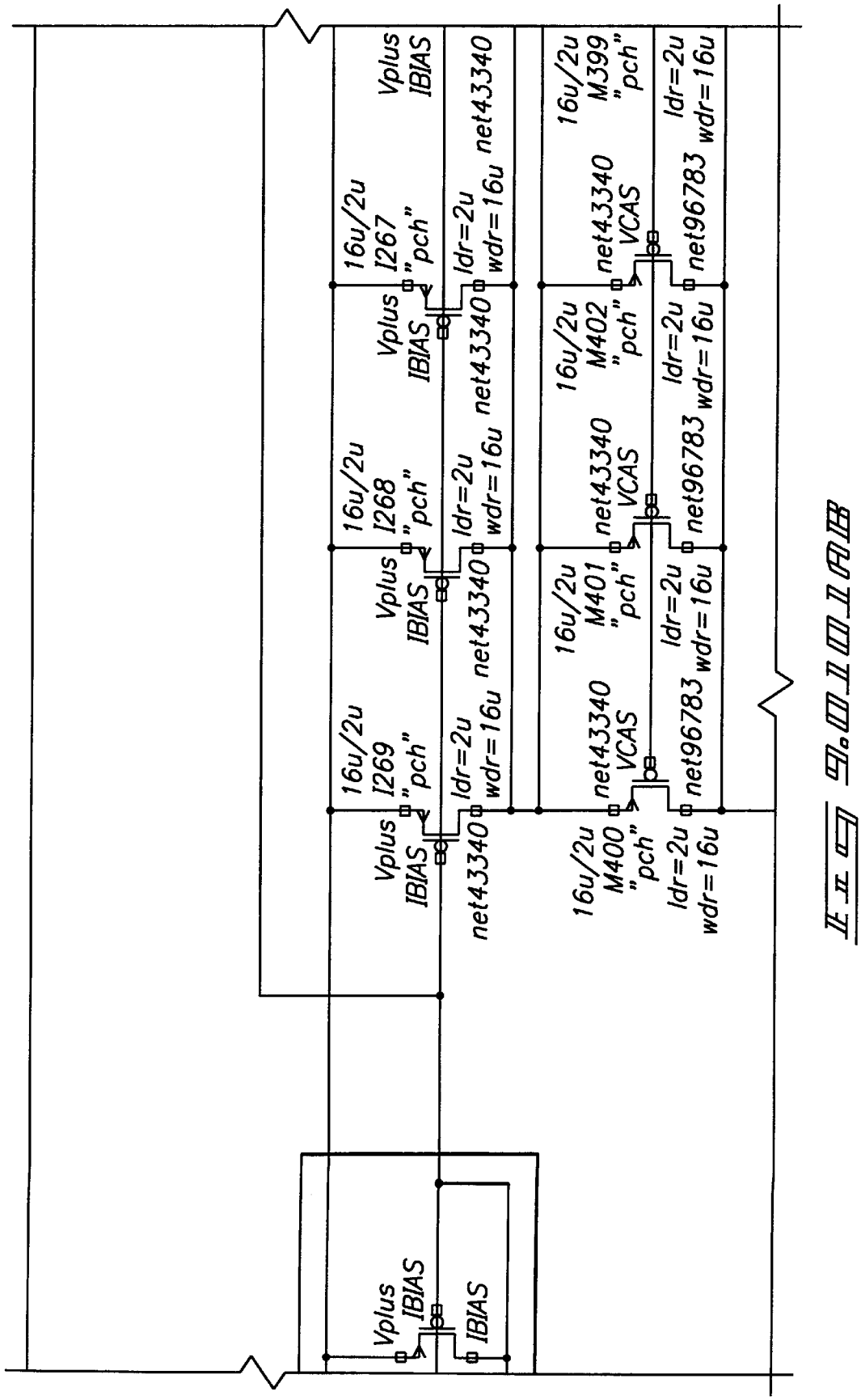

Vplus
IBIAS
16u/2u
I267
"pch"
ldr=2u
wdr=16u
net43340
16u/2u
M399
"pch"
net96783
VCAS
16u/2u
I268
"pch"
16u/2u
M402
"pch"
16u/2u
I269
"pch"
16u/2u
M401
"pch"
16u/2u
M400
"pch"

FIG. 2249

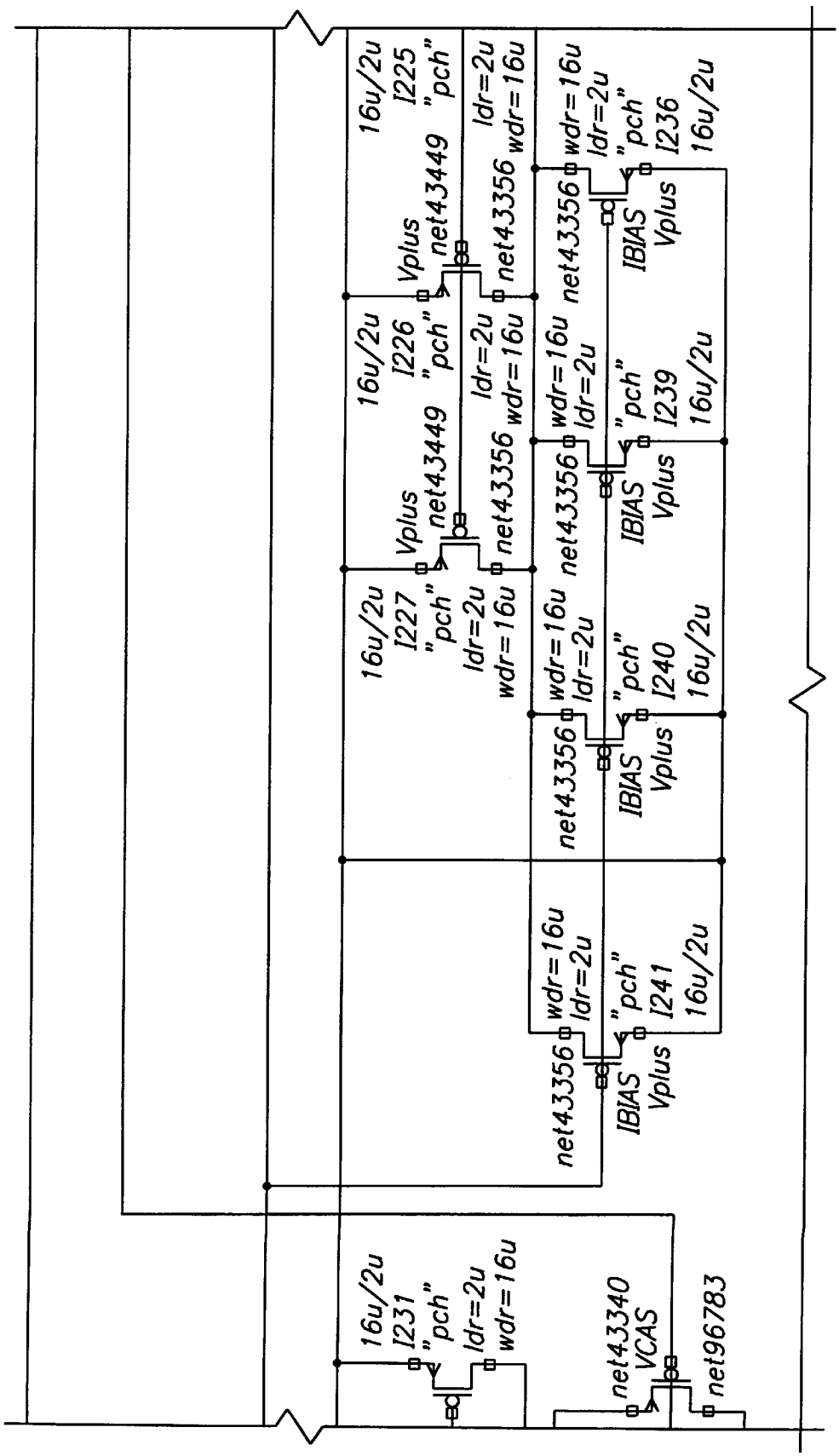

16u/2u
I225
"pch"
wdr=16u
ldr=2u
net43449
Vplus
net43356
16u/2u
I226
"pch"
wdr=16u
ldr=2u
net43449
Vplus
net43356
16u/2u
I227
"pch"
wdr=16u
ldr=2u
net43356
IBIAS
Vplus
16u/2u
I231
"pch"
wdr=16u
ldr=2u
net43340
VCAS
net96783
wdr=16u
ldr=2u
net43356
IBIAS
Vplus
"pch"
I236
16u/2u
wdr=16u
ldr=2u
net43356
IBIAS
Vplus
"pch"
I239
16u/2u
wdr=16u
ldr=2u
net43356
IBIAS
Vplus
"pch"
I240
16u/2u
wdr=16u
ldr=2u
net43356
IBIAS
Vplus
"pch"
I241
16u/2u

FIG. 911

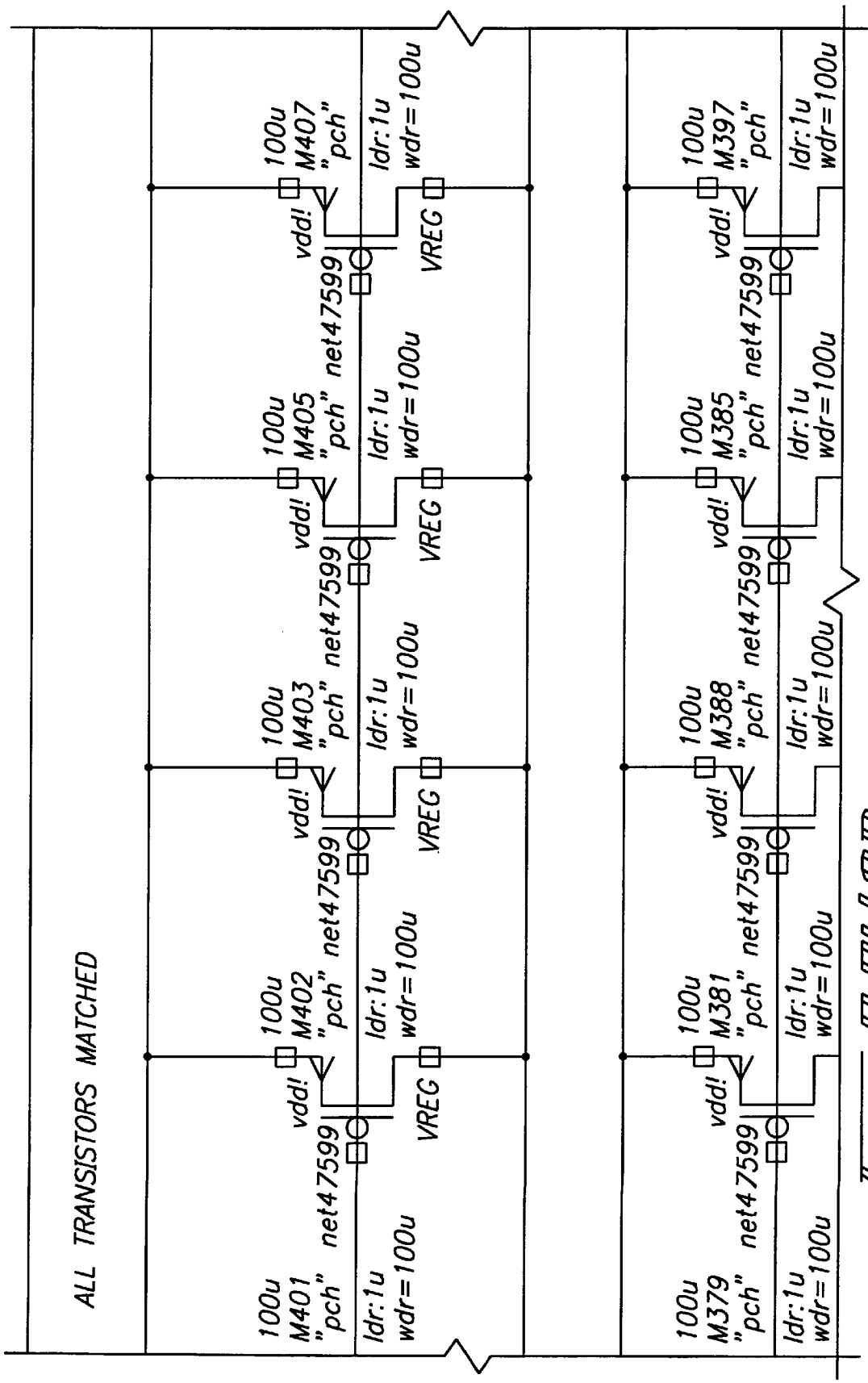

ALL TRANSISTORS MATCHED
100u M401 "pch" net47599 ldr:1u wdr=100u
100u M402 "pch" net47599 ldr:1u wdr=100u
100u M403 "pch" net47599 ldr:1u wdr=100u
100u M405 "pch" net47599 ldr:1u wdr=100u
100u M407 "pch" net47599 ldr:1u wdr=100u
100u M379 "pch" net47599 ldr:1u wdr=100u
100u M381 "pch" net47599 ldr:1u wdr=100u
100u M388 "pch" net47599 ldr:1u wdr=100u
100u M385 "pch" net47599 ldr:1u wdr=100u
100u M397 "pch" net47599 ldr:1u wdr=100u
vdd!
VREG

FIG. 2251

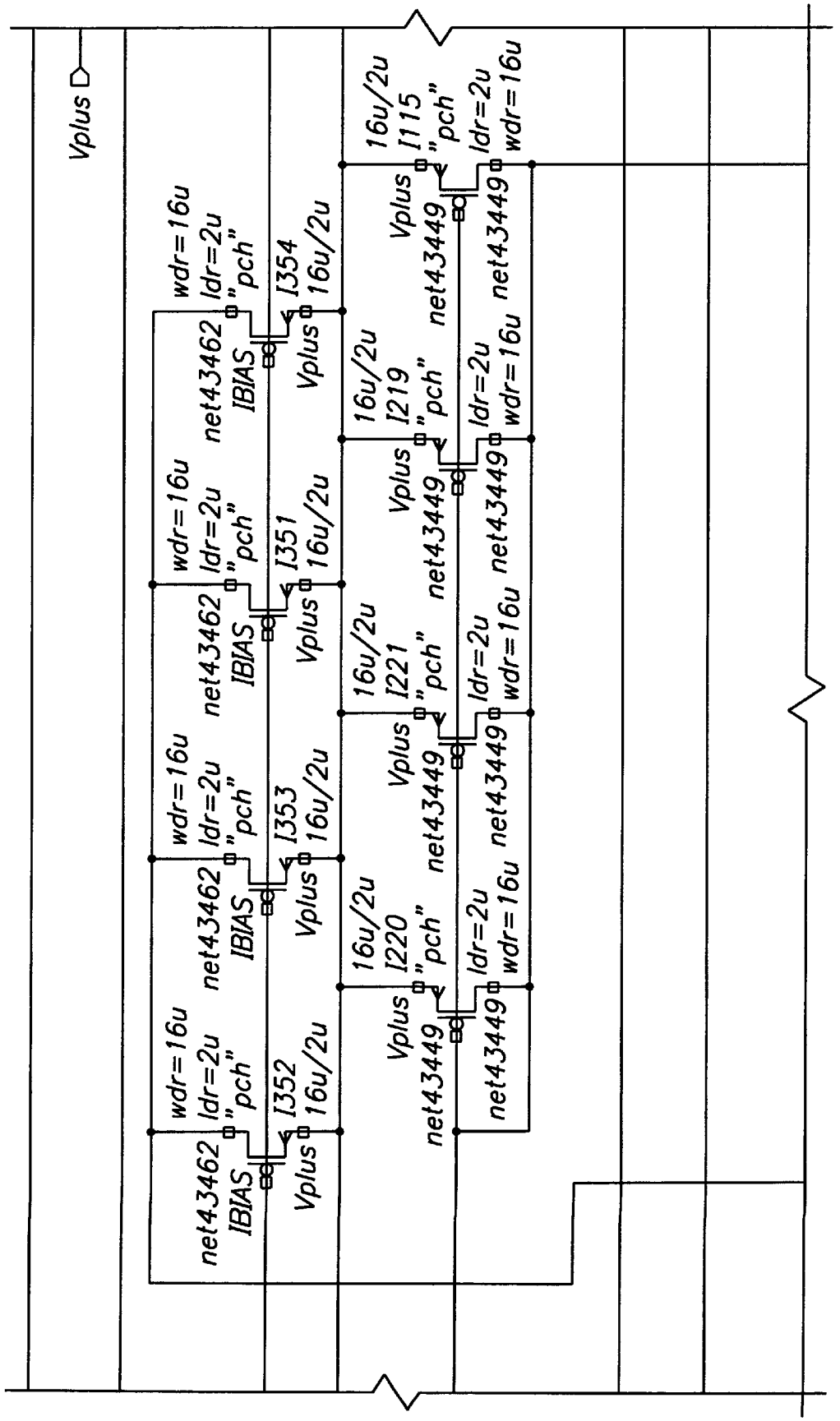

Vplus
net43462
IBIAS
wdr=16u
ldr=2u
"pch"
I352
16u/2u
Vplus
net43449
I220
I353
I221
I351
I219
I354
I115
wdr=16u

FIG 9.00 11 AE

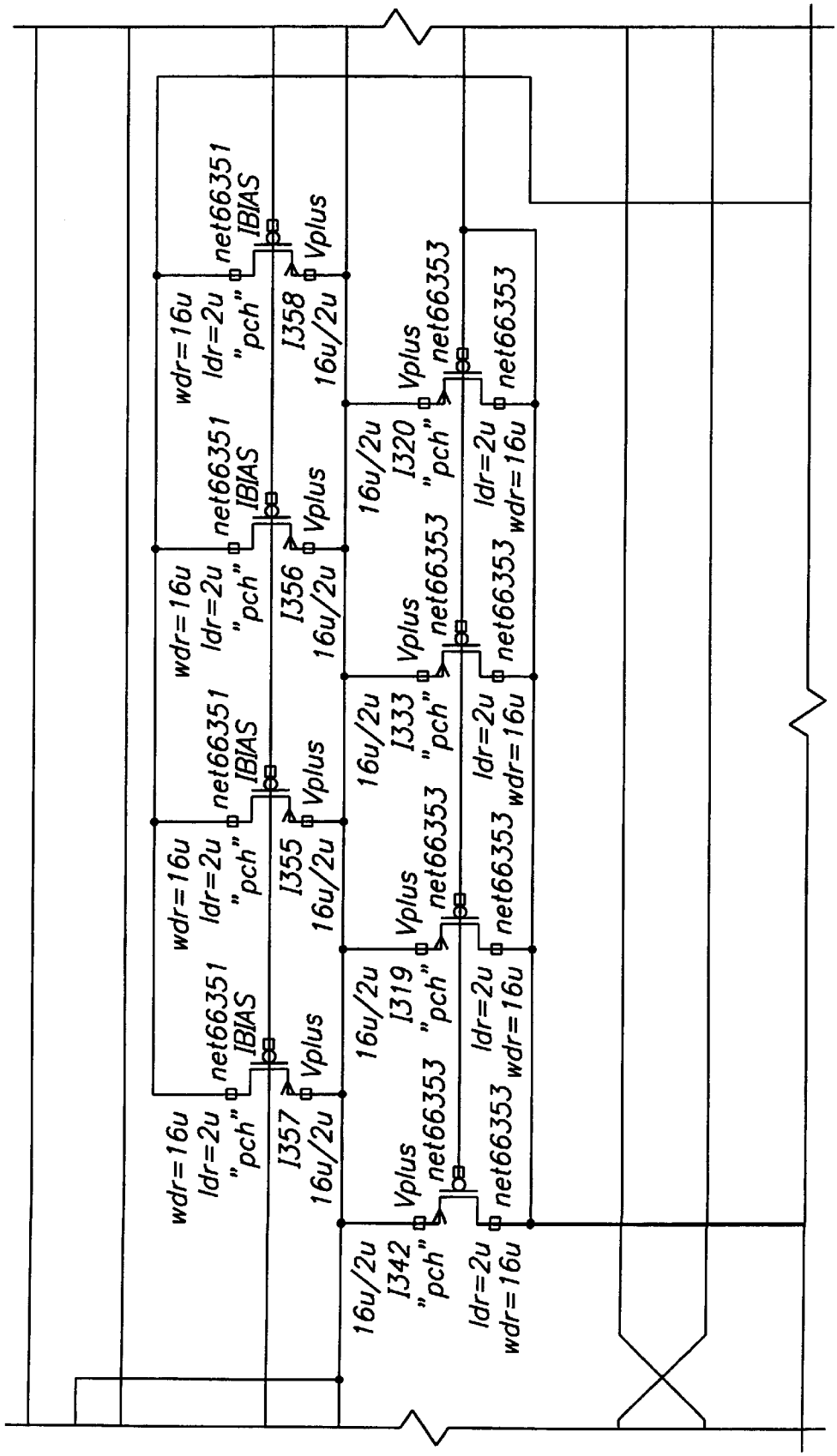


FIG. 59.00 II AIF

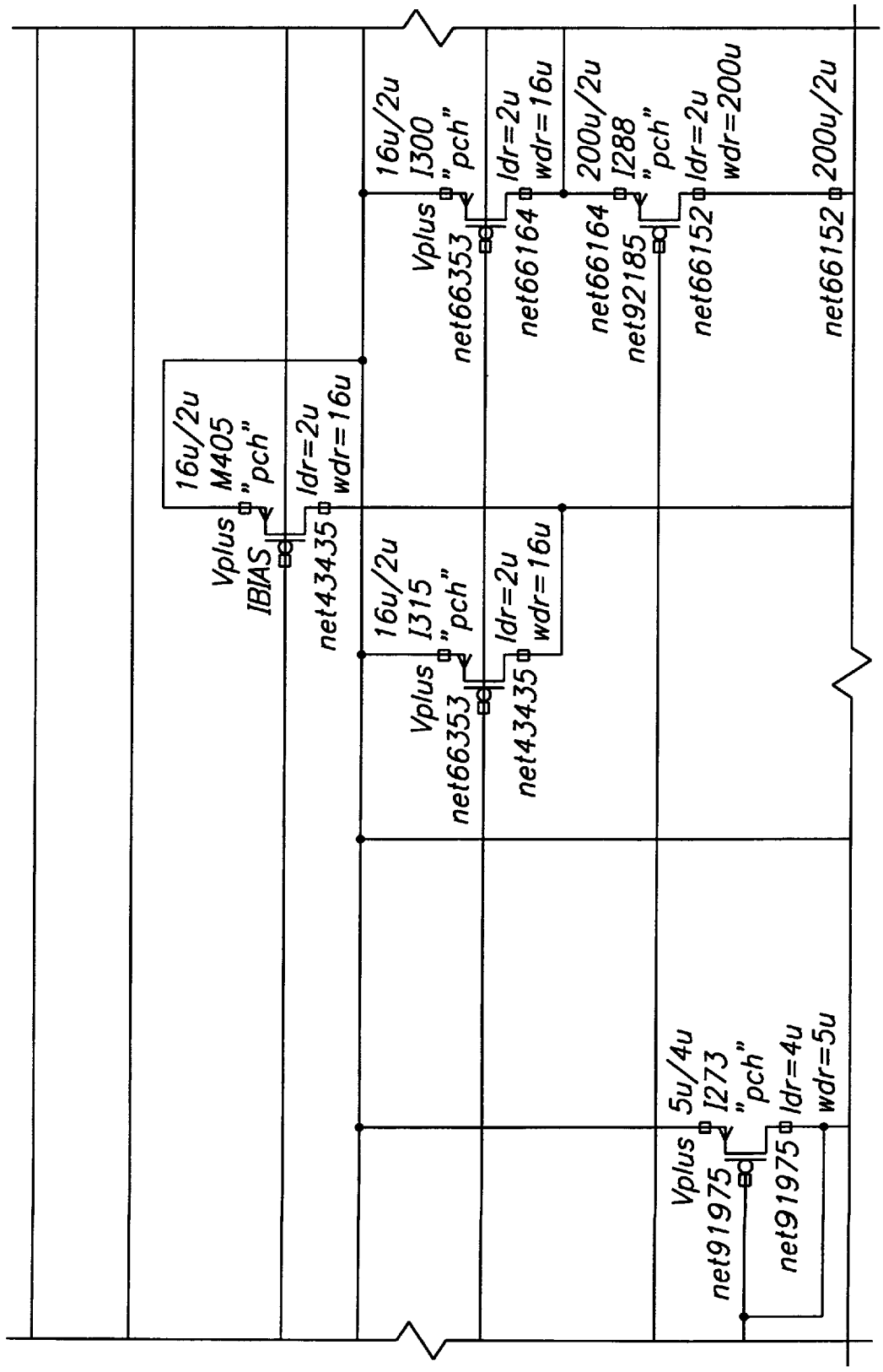

16u/2u
M405
"pch"
ldr=2u
wdr=16u
Vplus
IBIAS
net43435
16u/2u
I315
"pch"
ldr=2u
wdr=16u
Vplus
net66353
net43435
16u/2u
I300
"pch"
ldr=2u
wdr=16u
Vplus
net66353
net66164
200u/2u
I288
"pch"
ldr=2u
wdr=200u
net66164
net92185
net66152
200u/2u
net66152
5u/4u
I273
"pch"
ldr=4u
wdr=5u
Vplus
net91975
net91975

FIG 9.0011AS

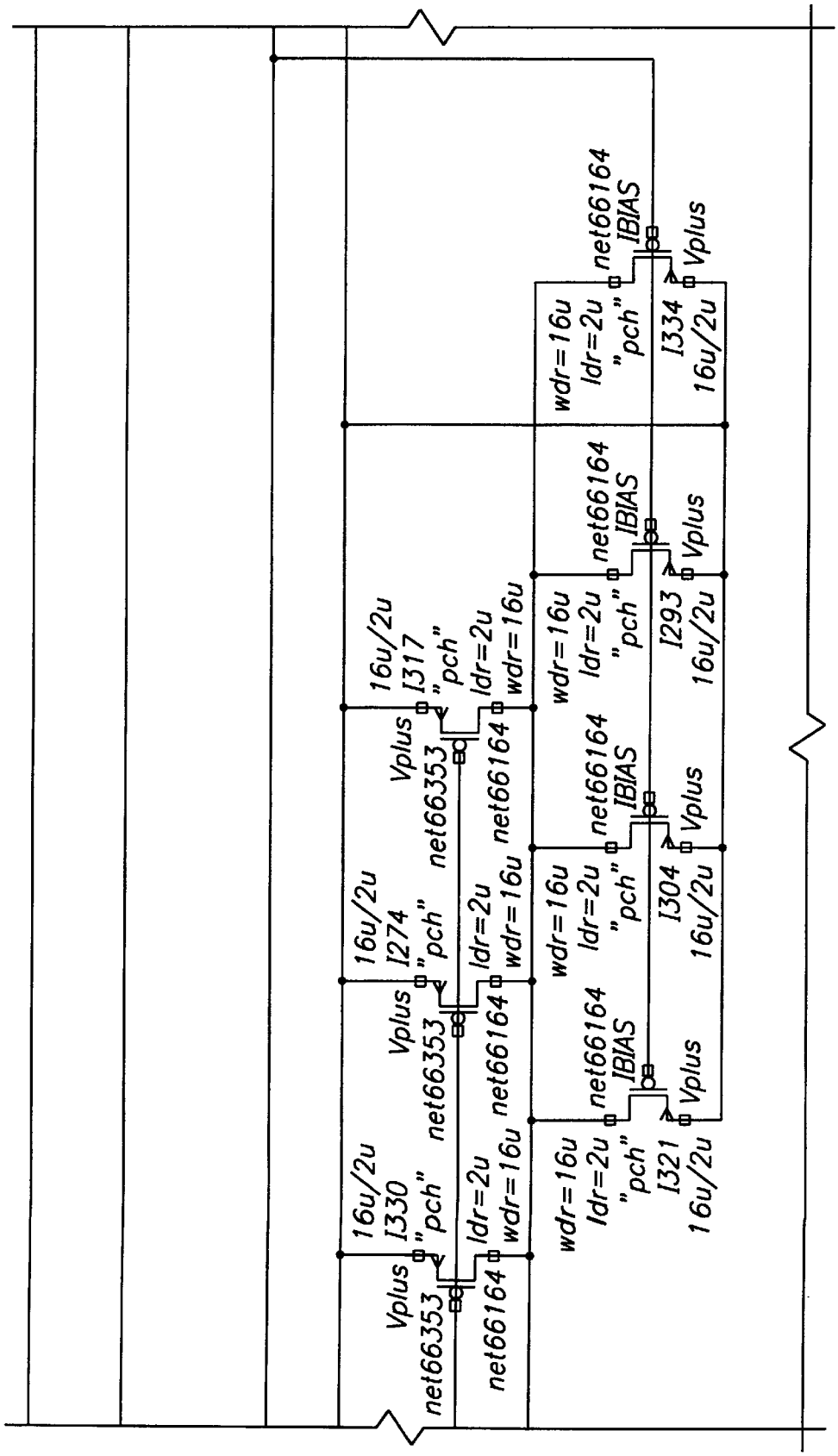

16u/2u
I330
"pch"
ldr=2u
wdr=16u
Vplus
net66353
net66164
wdr=16u
ldr=2u
"pch"
I321
16u/2u
net66164
IBIAS
Vplus
16u/2u
I274
"pch"
ldr=2u
wdr=16u
Vplus
net66353
net66164
wdr=16u
ldr=2u
"pch"
I304
16u/2u
net66164
IBIAS
Vplus
16u/2u
I317
"pch"
ldr=2u
wdr=16u
Vplus
net66353
net66164
wdr=16u
ldr=2u
"pch"
I293
16u/2u
net66164
IBIAS
Vplus
wdr=16u
ldr=2u
"pch"
I334
16u/2u
net66164
IBIAS
Vplus

FIG. 9.0011AH

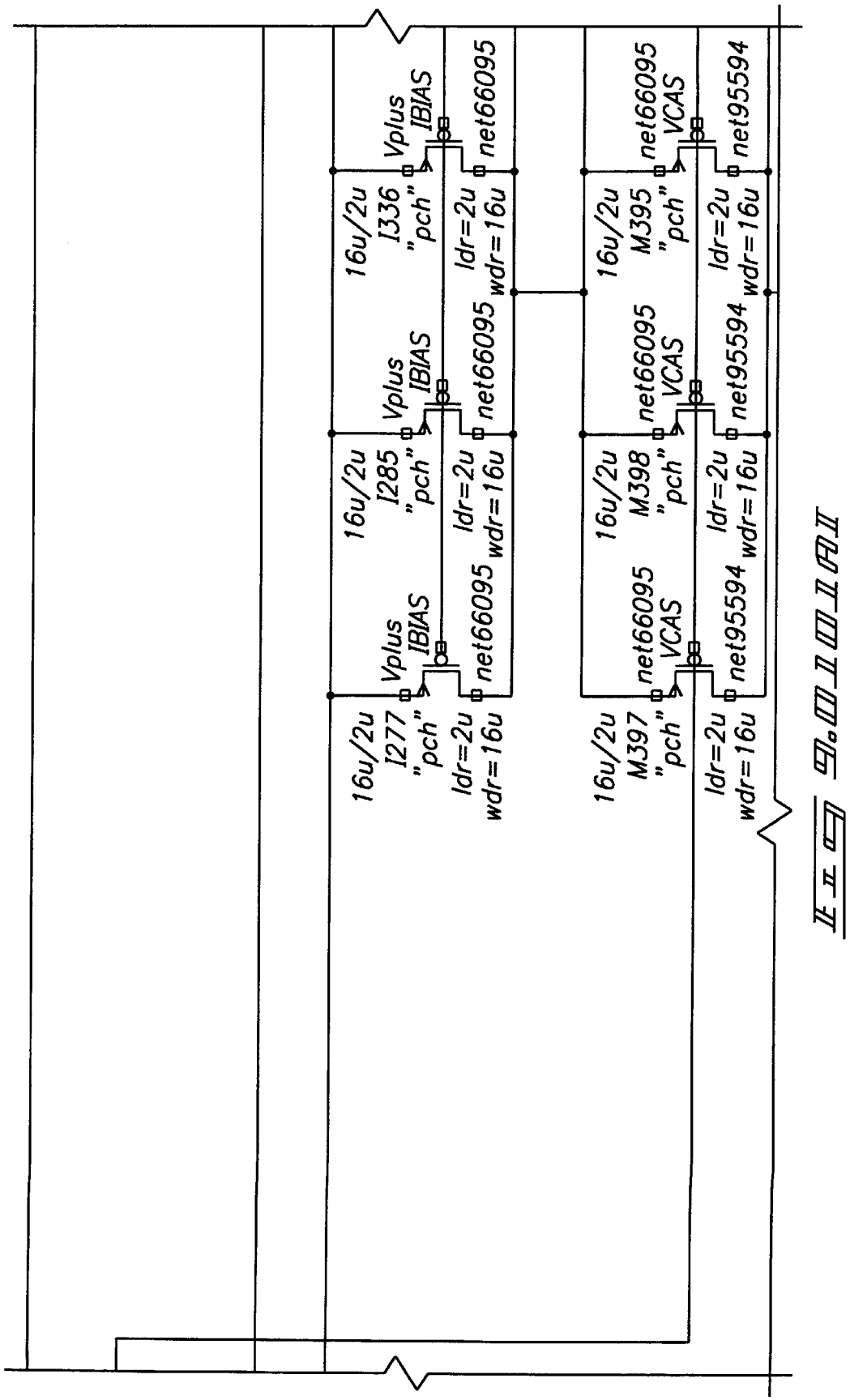


Fig. 9.0011AII

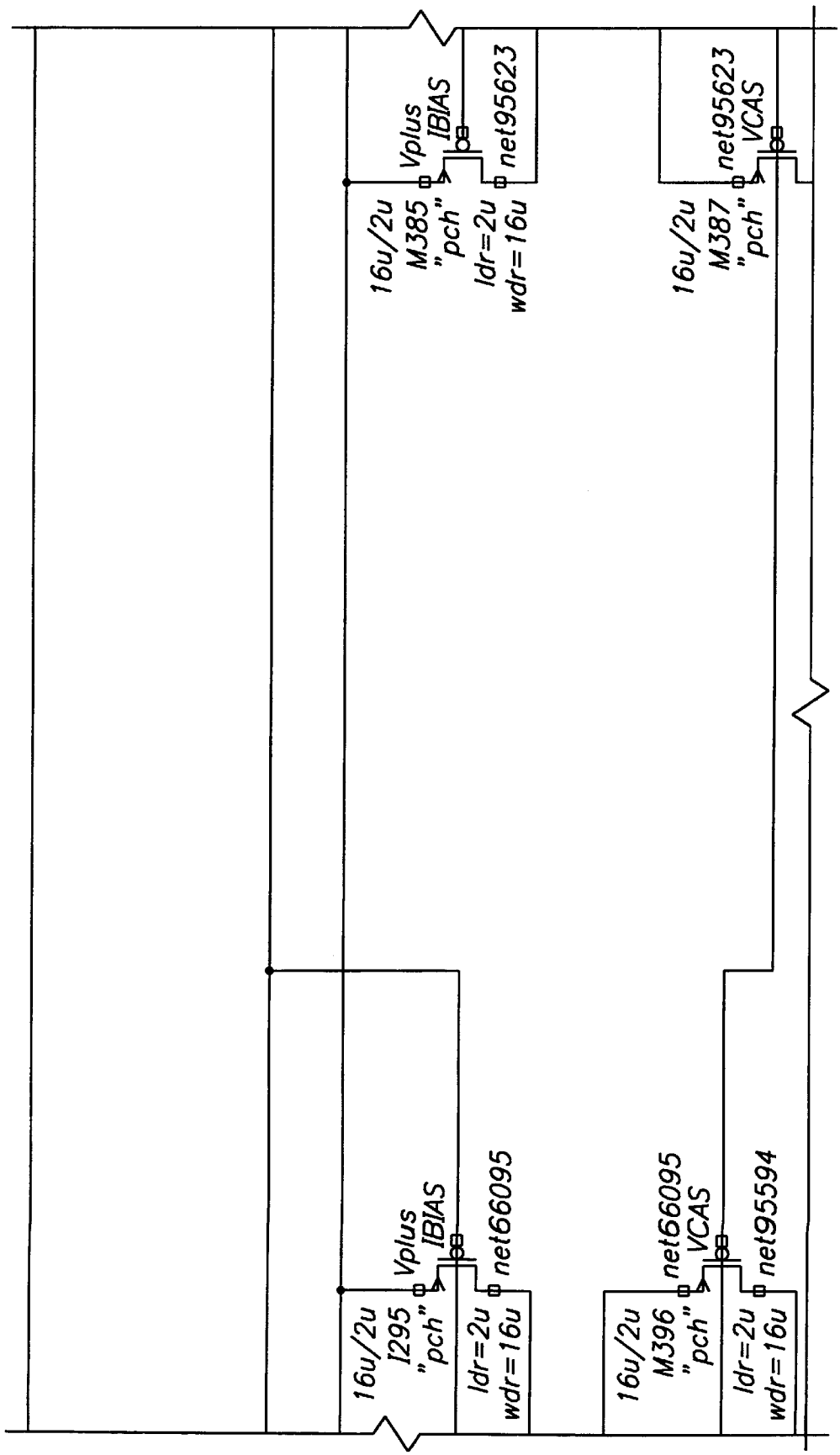


FIG 9.00 (Prior Art)

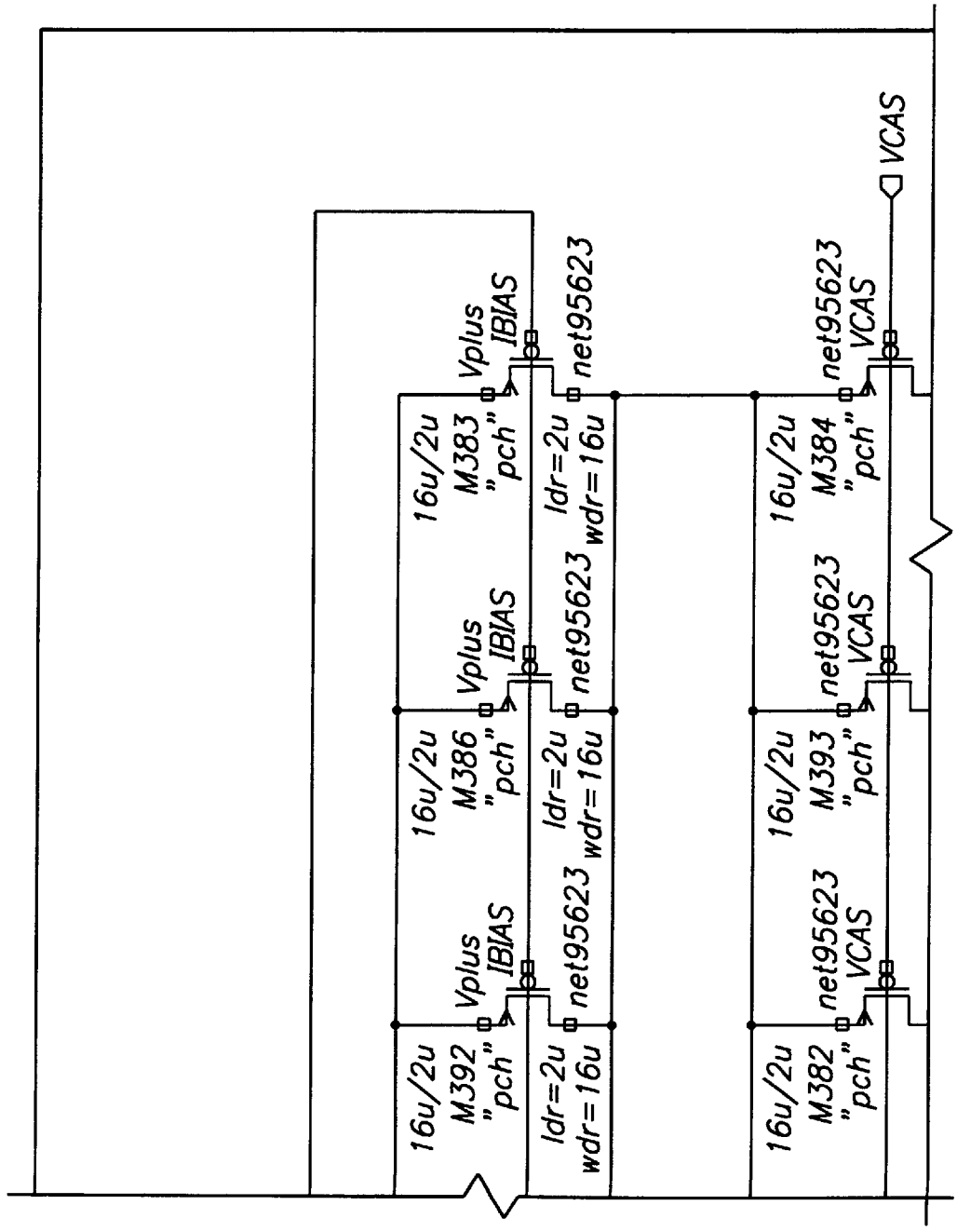

16u/2u
M392
"pch"
Vplus
IBIAS
ldr=2u
wdr=16u
net95623
16u/2u
M386
"pch"
Vplus
IBIAS
ldr=2u
wdr=16u
net95623
16u/2u
M383
"pch"
Vplus
IBIAS
ldr=2u
wdr=16u
net95623
16u/2u
M382
"pch"
net95623
VCAS
16u/2u
M393
"pch"
net95623
VCAS
16u/2u
M384
"pch"
net95623
VCAS
VCAS

FIG. 95

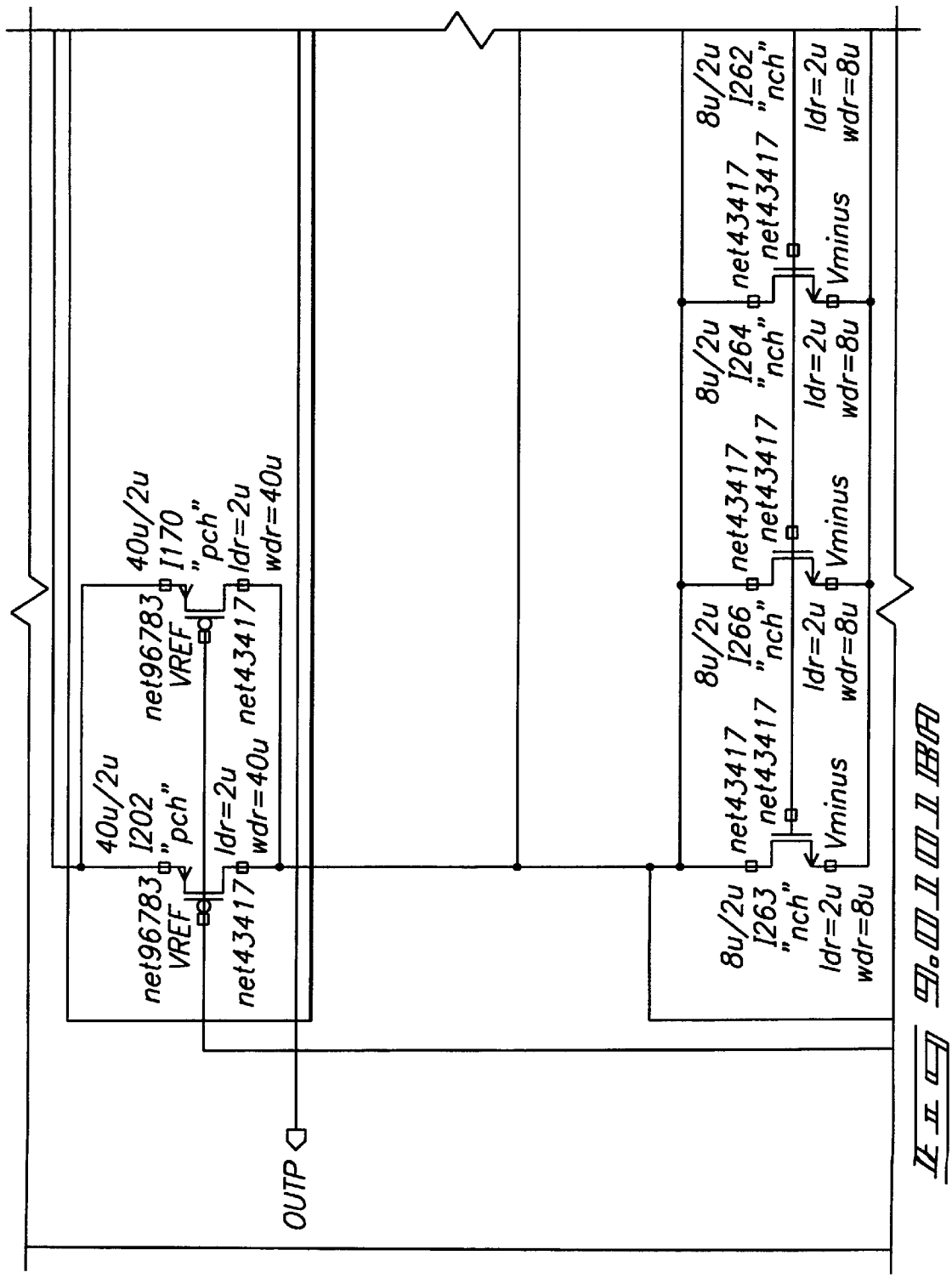

40u/2u
I202
"pch"
ldr=2u
wdr=40u
net96783
VREF
net43417
40u/2u
I170
"pch"
ldr=2u
wdr=40u
net96783
VREF
net43417
OUTP
8u/2u
I263
"nch"
ldr=2u
wdr=8u
net43417
net43417
Vminus
8u/2u
I266
"nch"
ldr=2u
wdr=8u
net43417
net43417
Vminus
8u/2u
I264
"nch"
ldr=2u
wdr=8u
net43417
net43417
Vminus
8u/2u
I262
"nch"
ldr=2u
wdr=8u
net43417
net43417
Vminus

Fig. 1

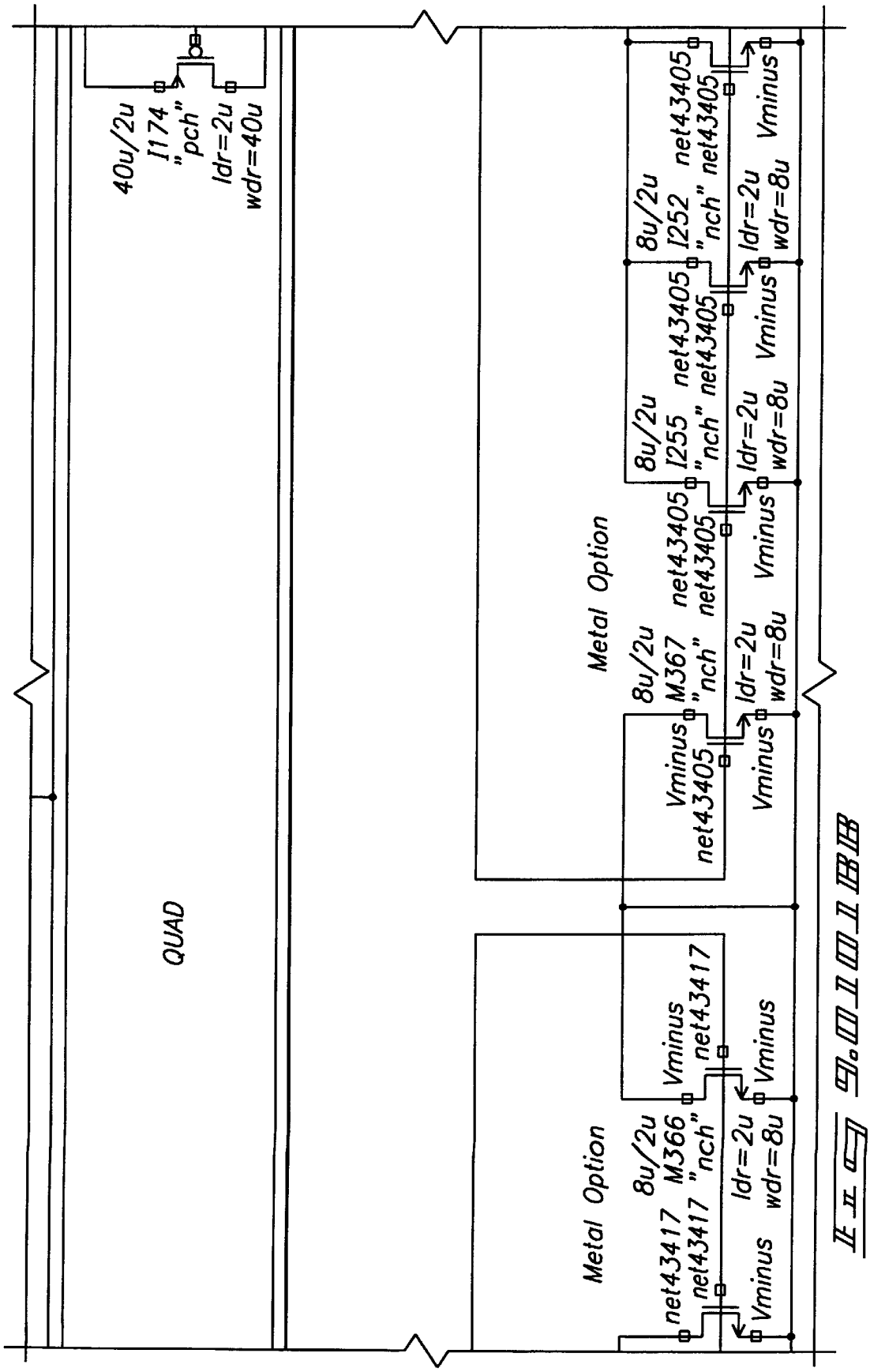

QUAD
40u/2u
I174
"pch"
ldr=2u
wdr=40u
Metal Option
8u/2u
M367
"nch"
ldr=2u
wdr=8u
net43405
Vminus
I255
I252
Metal Option
8u/2u
M366
"nch"
net43417
Vminus

FIG. 2260

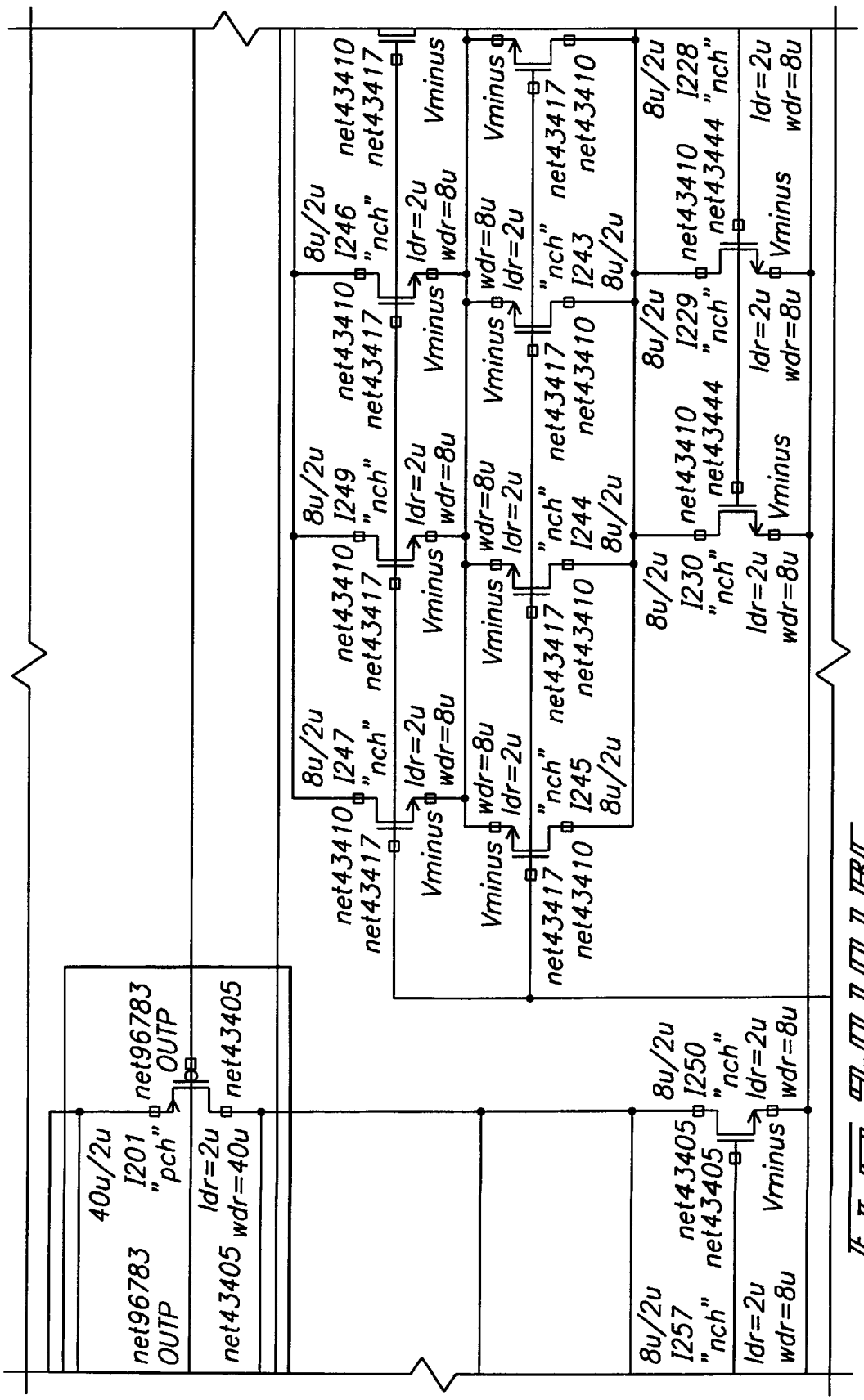


FIG 95.00 II 00

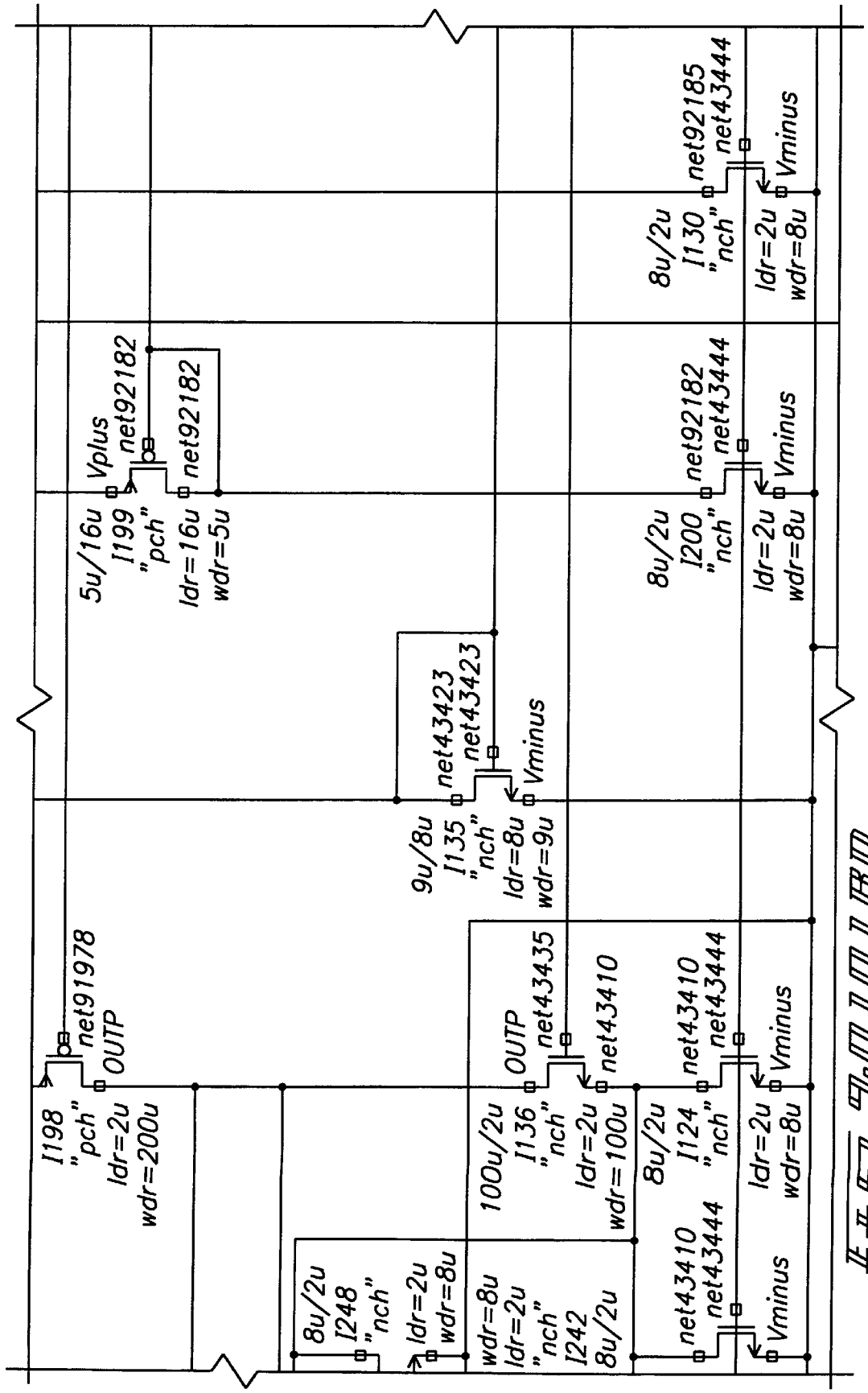
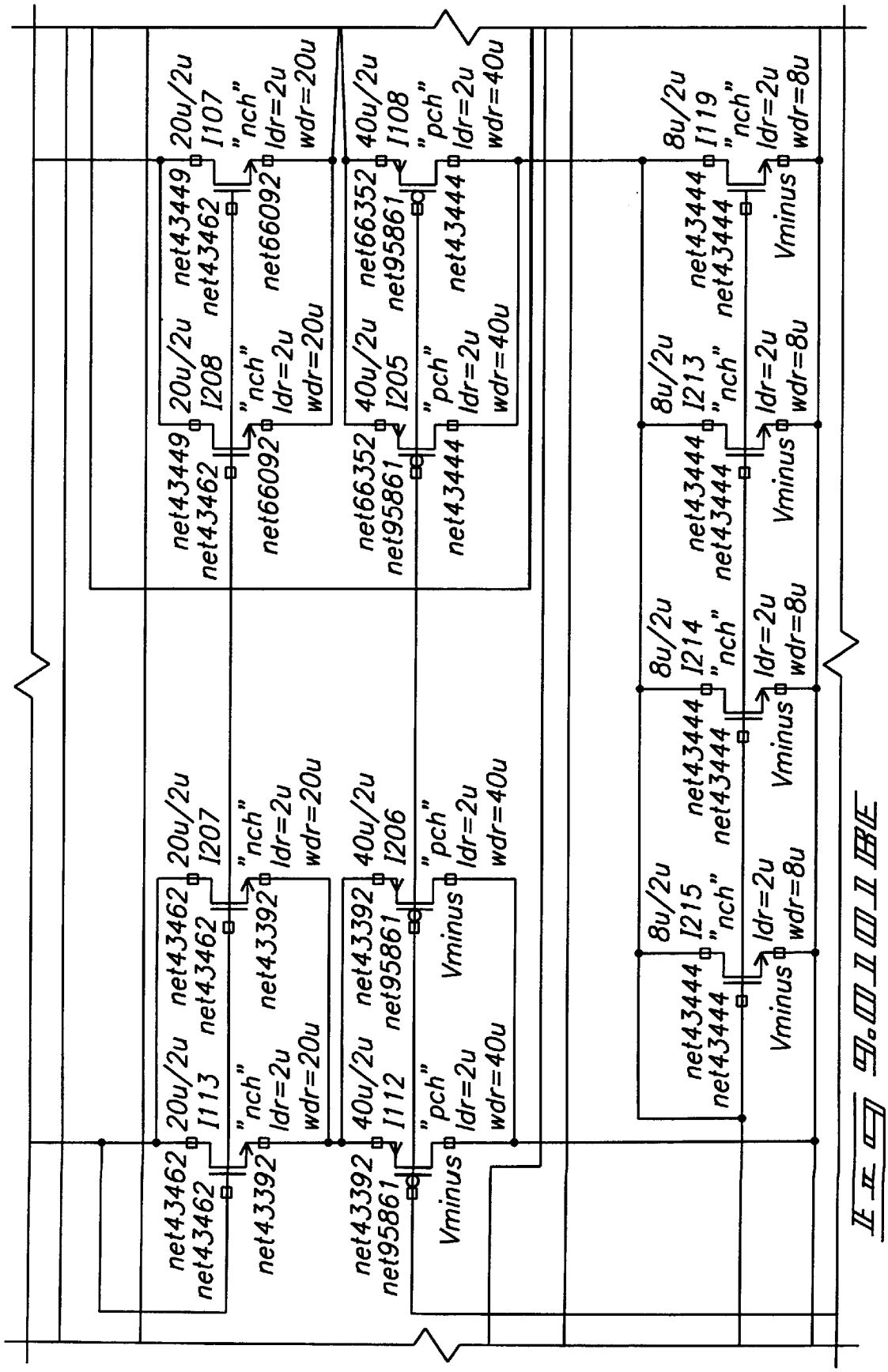


Fig. 99.III.IBM


I107 20u/2u "nch" ldr=2u wdr=20u
I108 40u/2u "pch" ldr=2u wdr=40u
I119 8u/2u "nch" ldr=2u wdr=8u
I208 20u/2u "nch" ldr=2u wdr=20u
I205 40u/2u "pch" ldr=2u wdr=40u
I213 8u/2u "nch" ldr=2u wdr=8u
I207 20u/2u "nch" ldr=2u wdr=20u
I206 40u/2u "pch" ldr=2u wdr=40u
I214 8u/2u "nch" ldr=2u wdr=8u
I113 20u/2u "nch" ldr=2u wdr=20u
I112 40u/2u "pch" ldr=2u wdr=40u
I215 8u/2u "nch" ldr=2u wdr=8u
net43449
net43462
net66092
net66352
net95861
net43444
net43392
Vminus

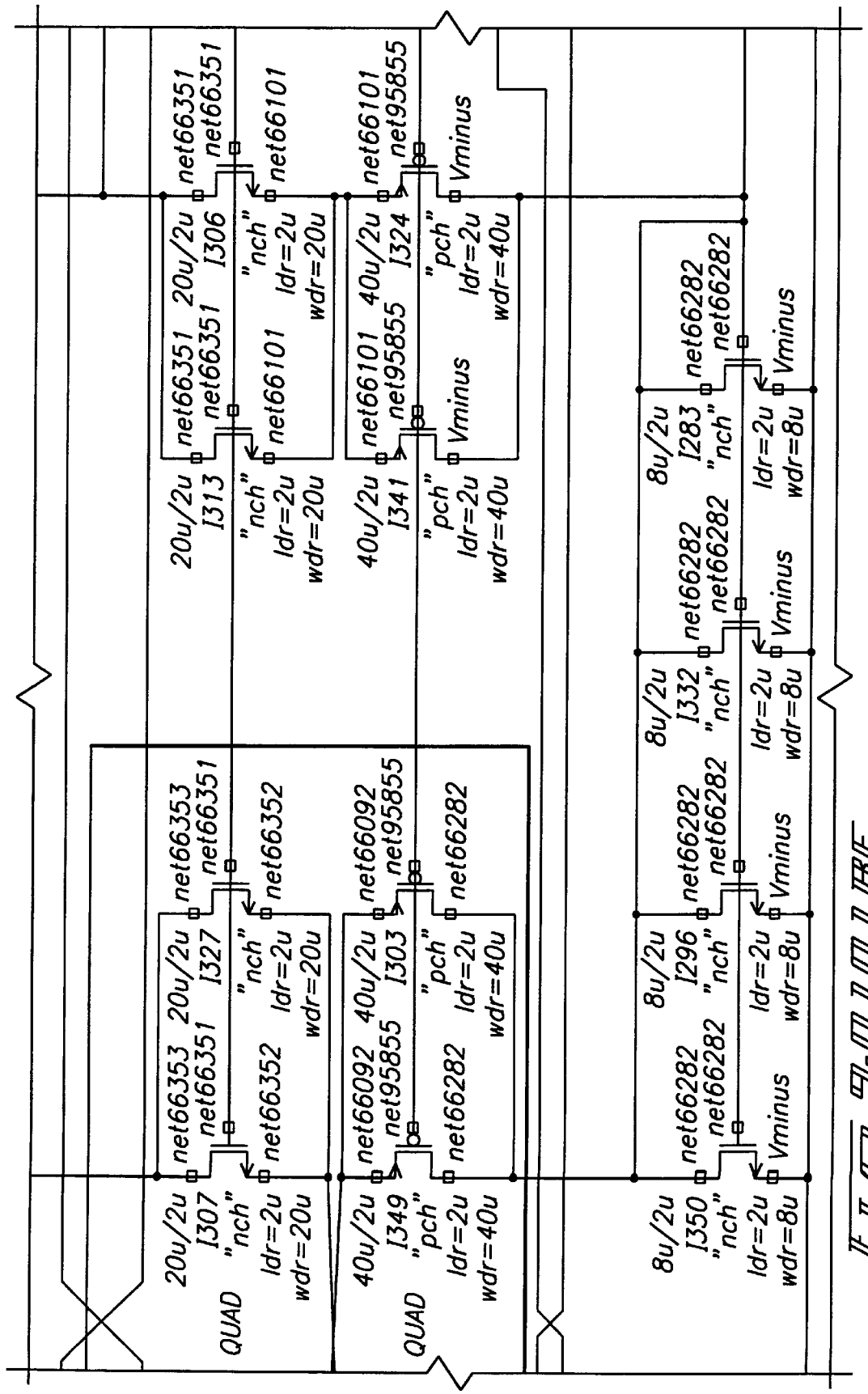


FIG. 9.00 II 00 II IBF

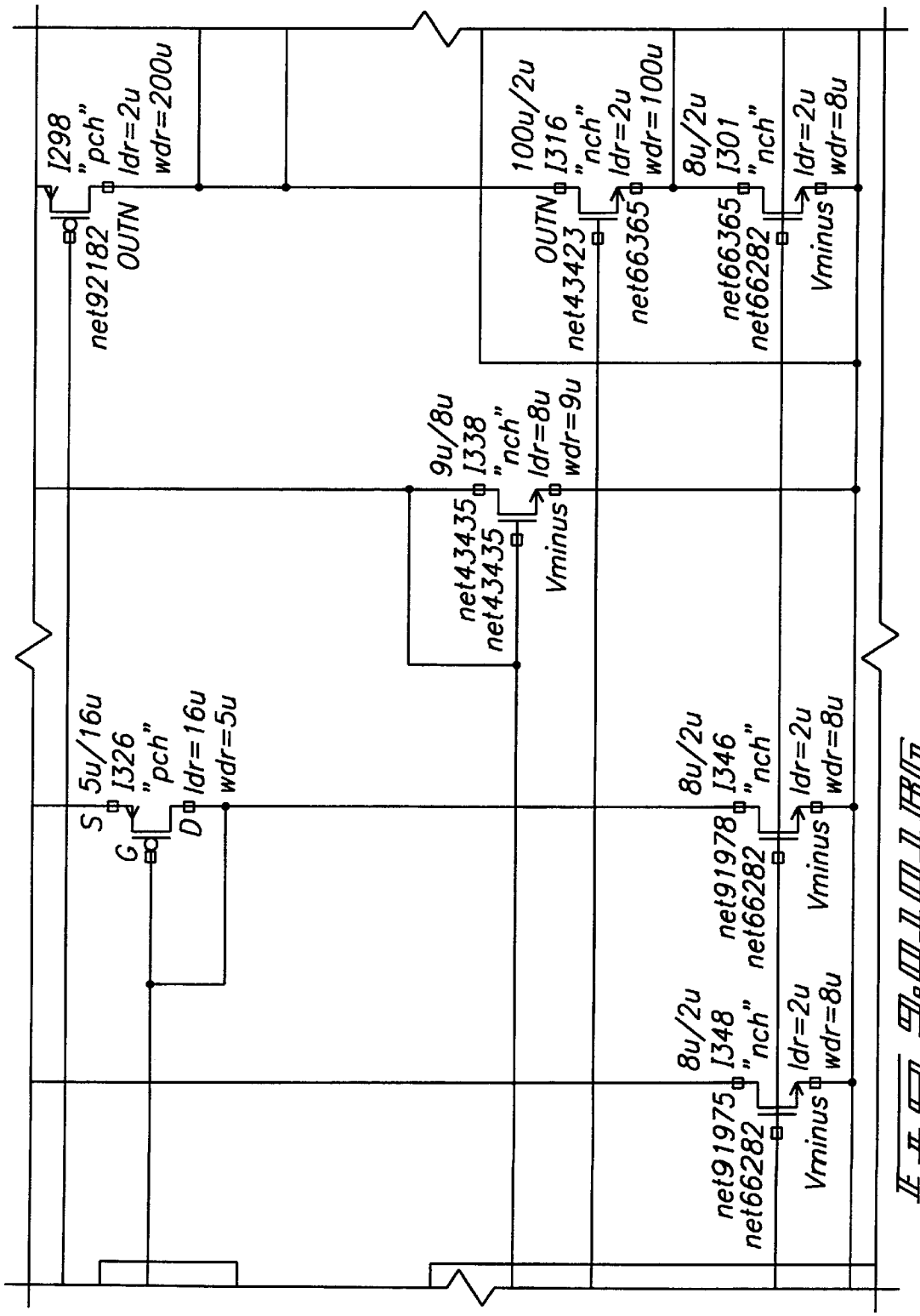


FIG 59.00 II 1885

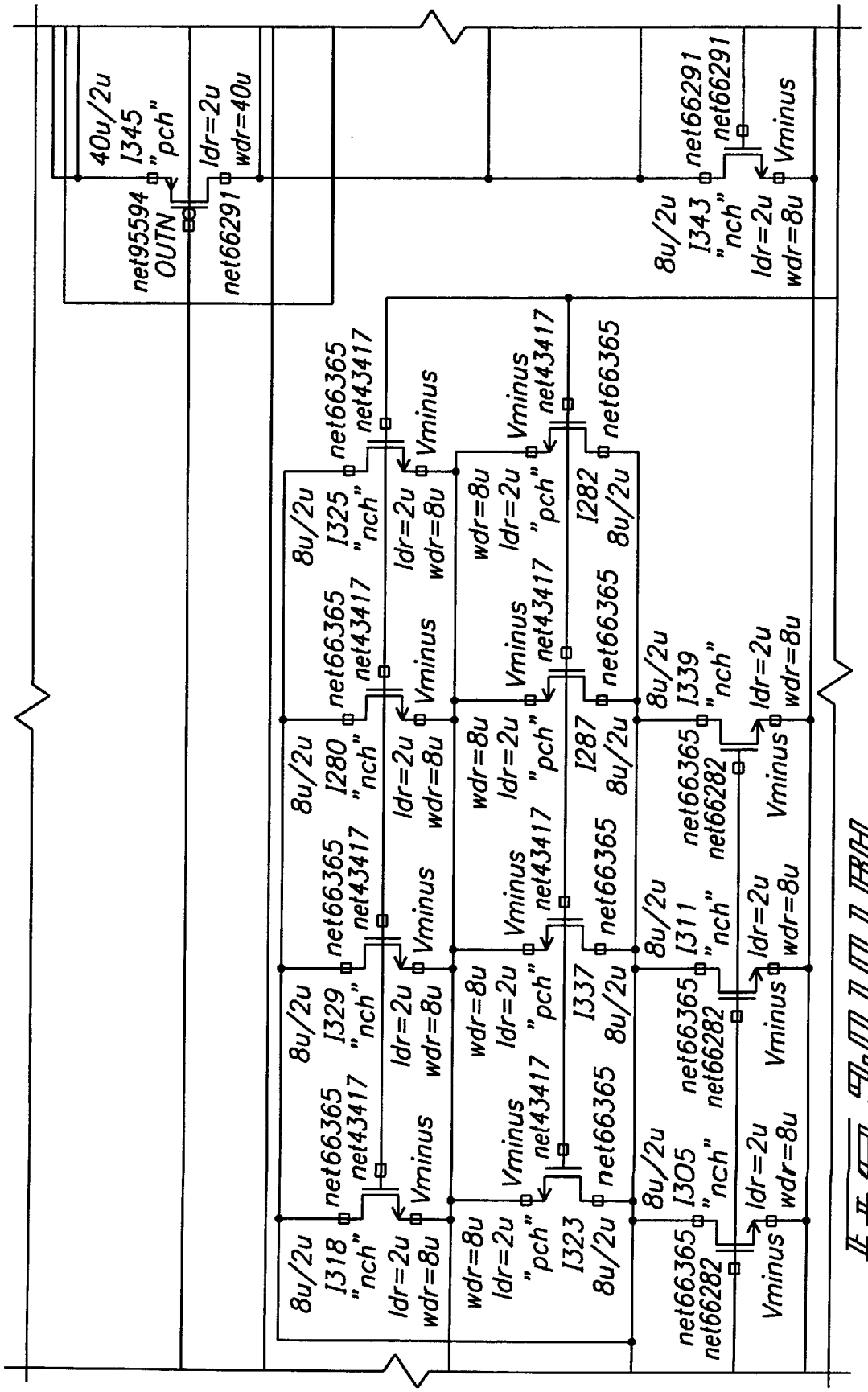

net95594
OUTN
40u/2u
I345
"pch"
ldr=2u
wdr=40u
net66291
8u/2u
I343
"nch"
ldr=2u
wdr=8u
net66291
Vminus
I318
I329
I280
I325
I339
I311
I305
I337
I287
I282
net66365
net43417
net66282
Vminus
wdr=8u
ldr=2u

Fig. 2266

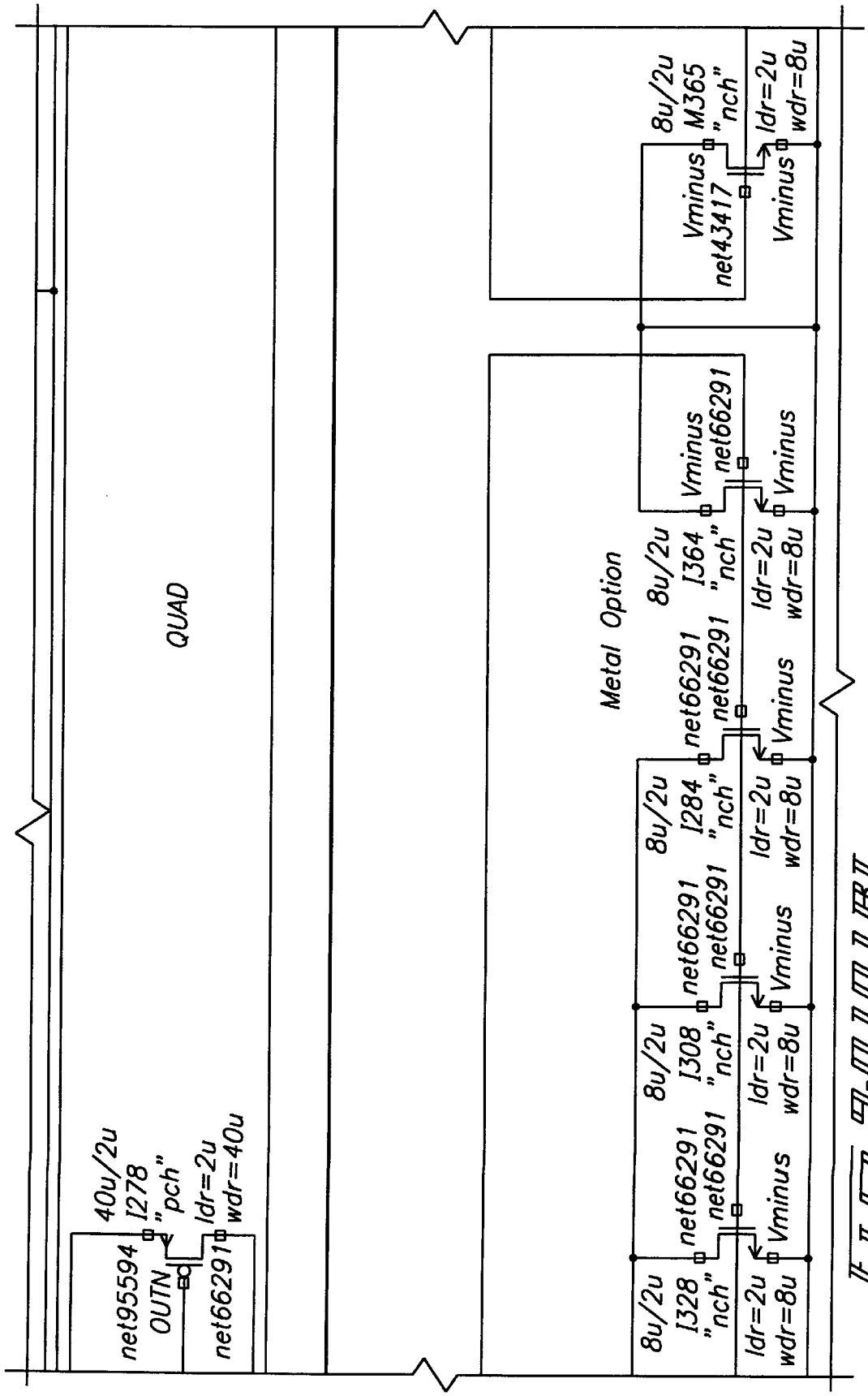

QUAD
Metal Option
net95594
OUTN
40u/2u
I278
"pch"
ldr=2u
wdr=40u
net66291
8u/2u
I328
"nch"
I308
I284
I364
M365
net66291
Vminus
net43417
ldr=2u
wdr=8u

FIG. 2267

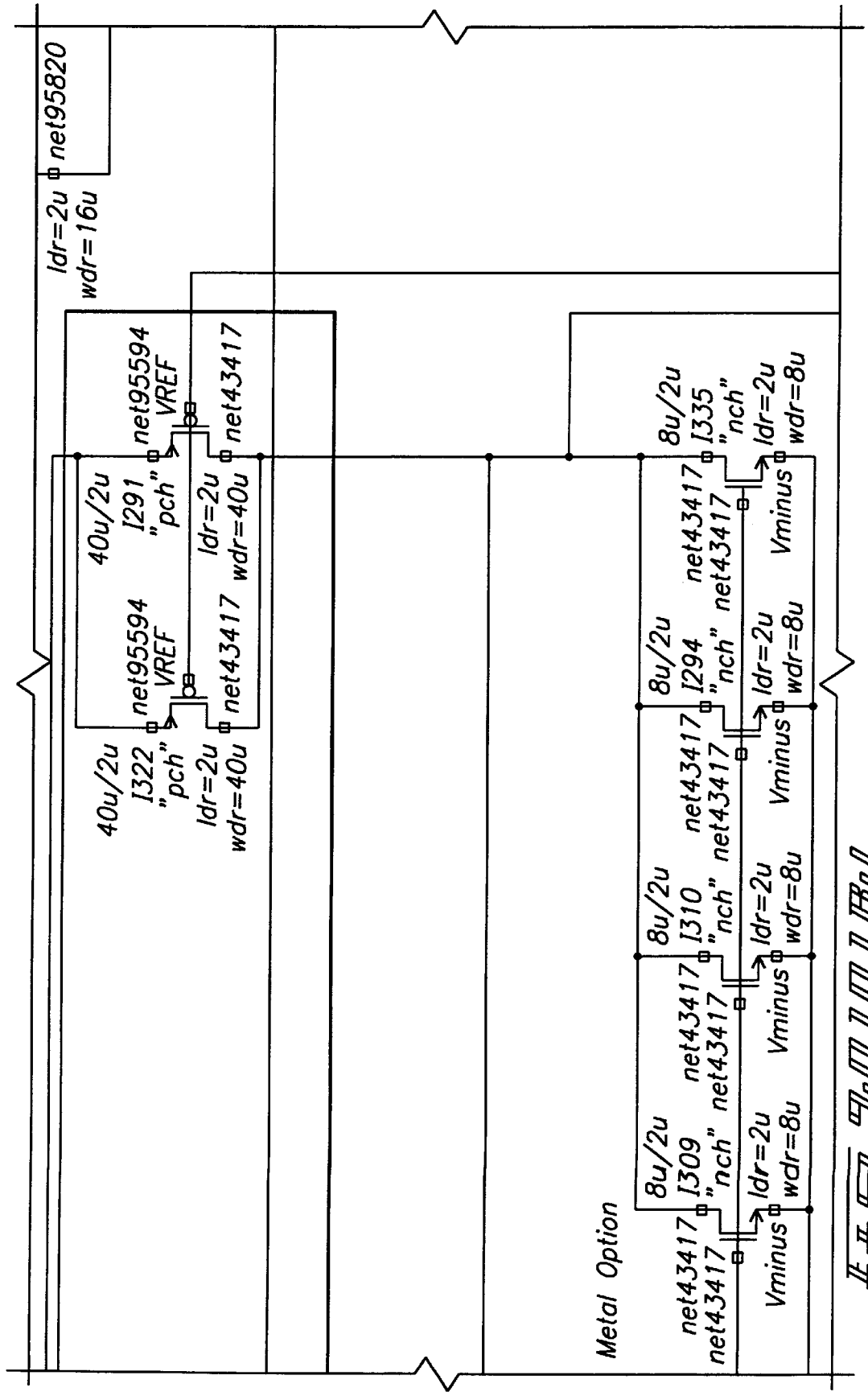


FIG 9.00 II 1800

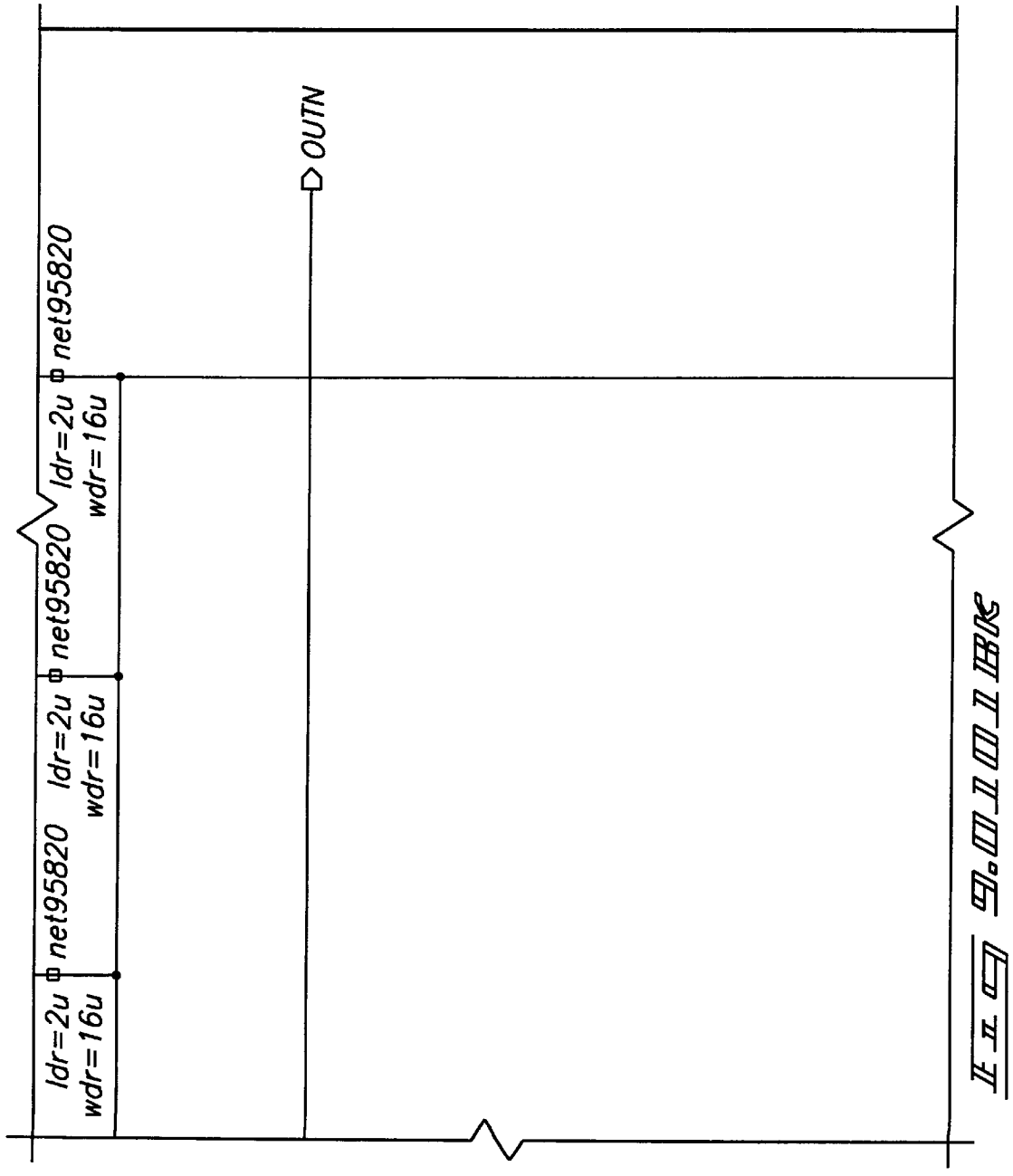

OUTN
net95820
ldr=2u
wdr=16u
net95820
ldr=2u
wdr=16u
net95820
ldr=2u
wdr=16u

FIG. 95.00118

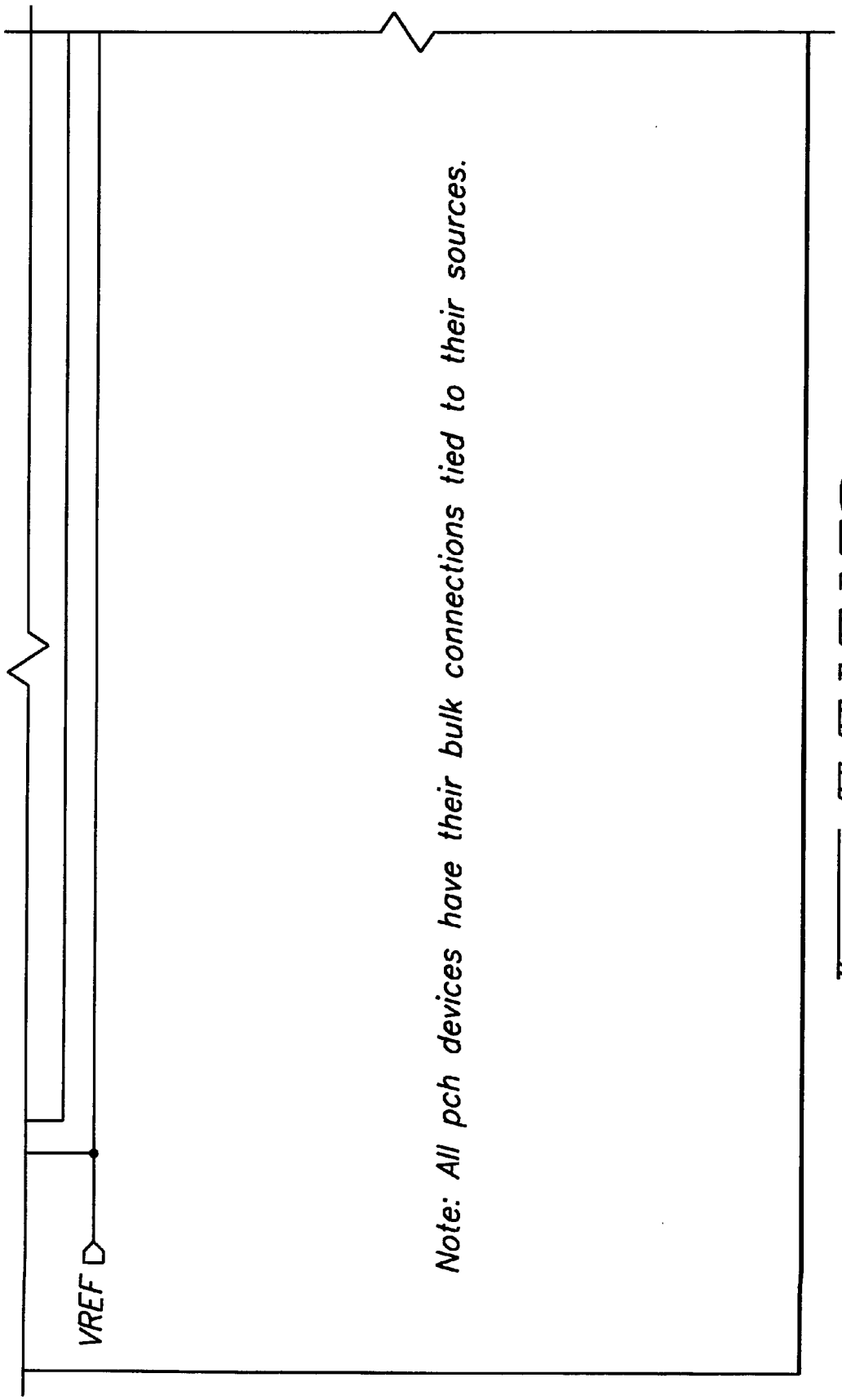

VREF
Note: All pch devices have their bulk connections tied to their sources.

FIG 9.0110A

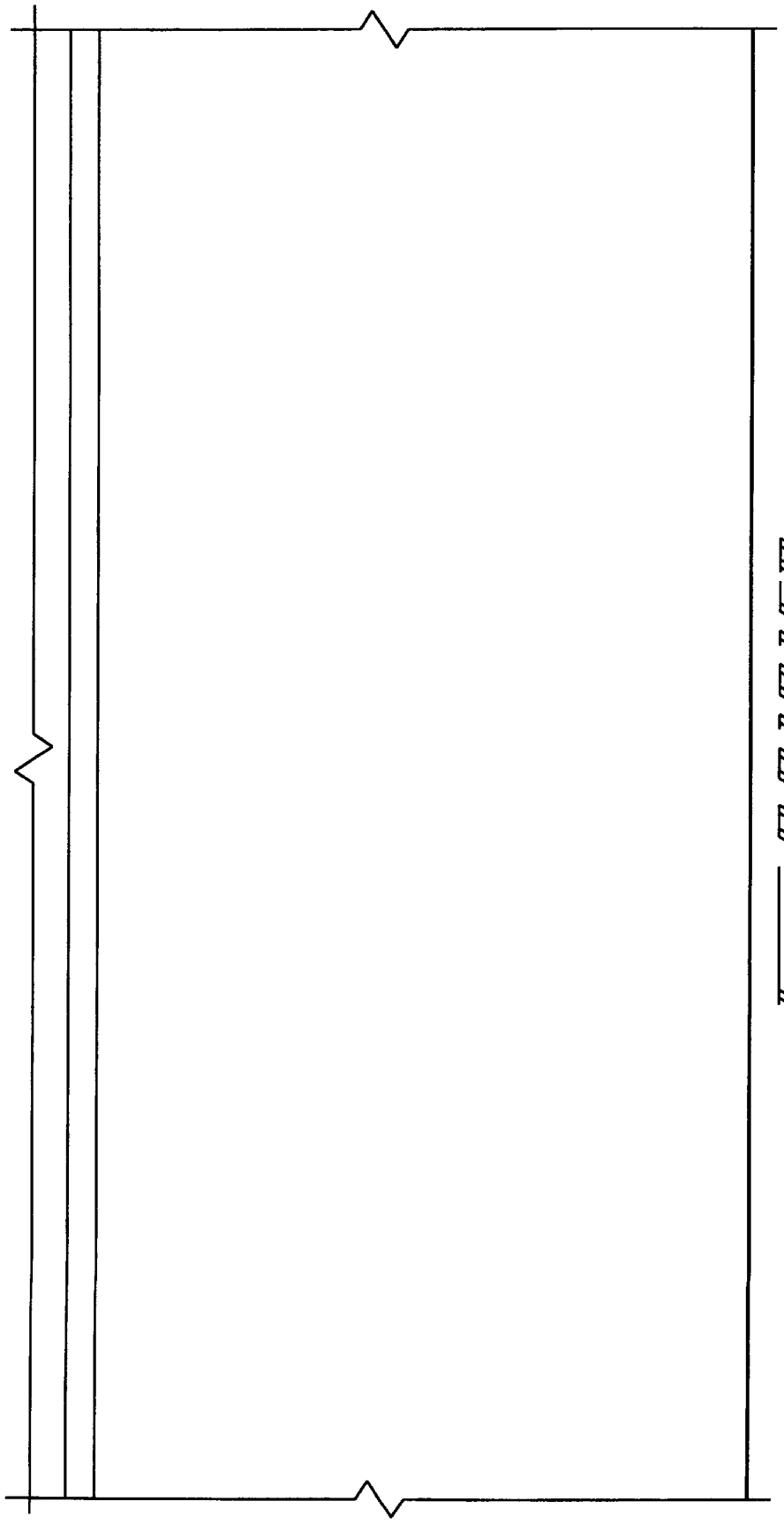


FIG 9,011 BB

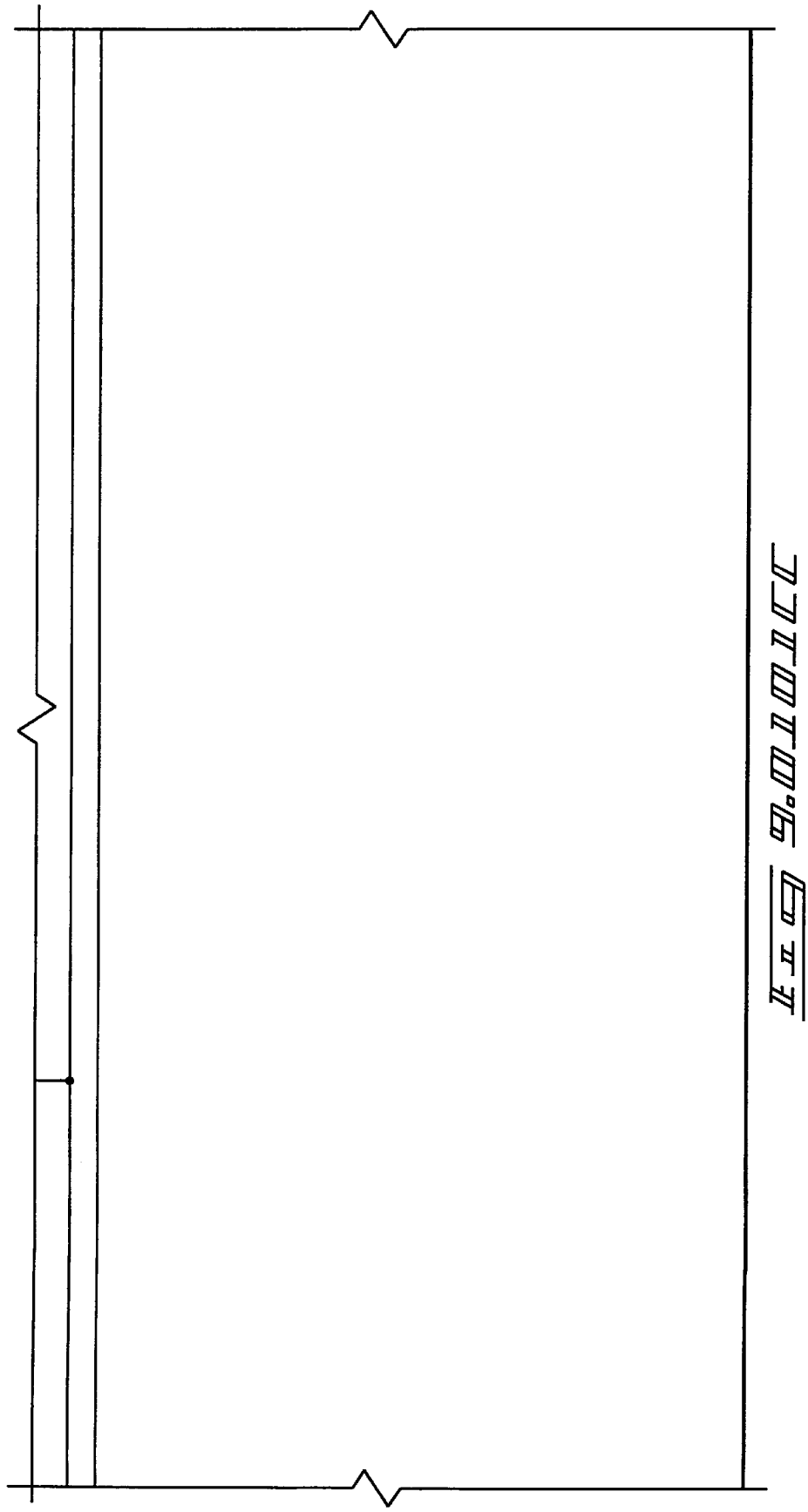


FIG. 9,001,102

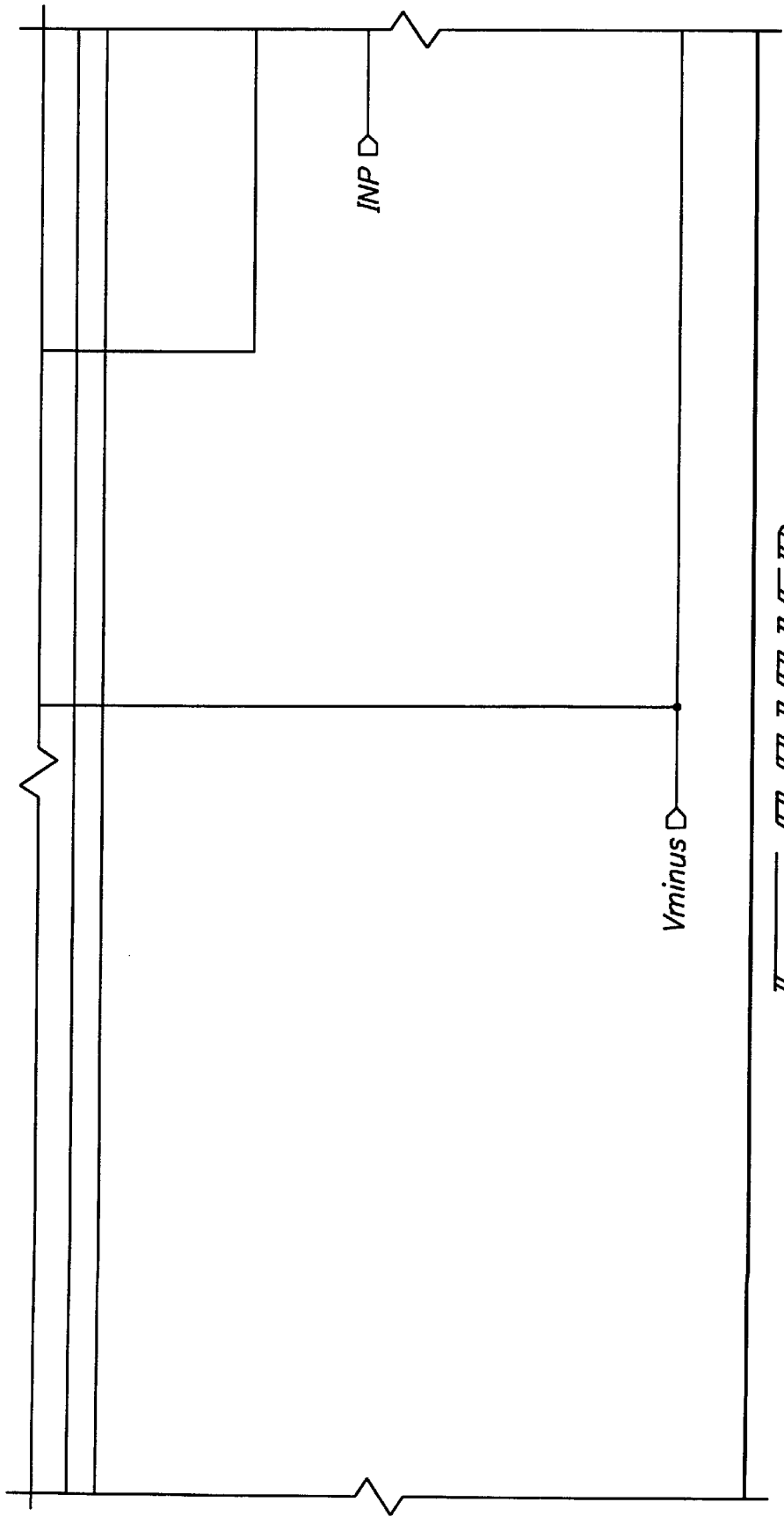


FIG 9,0110

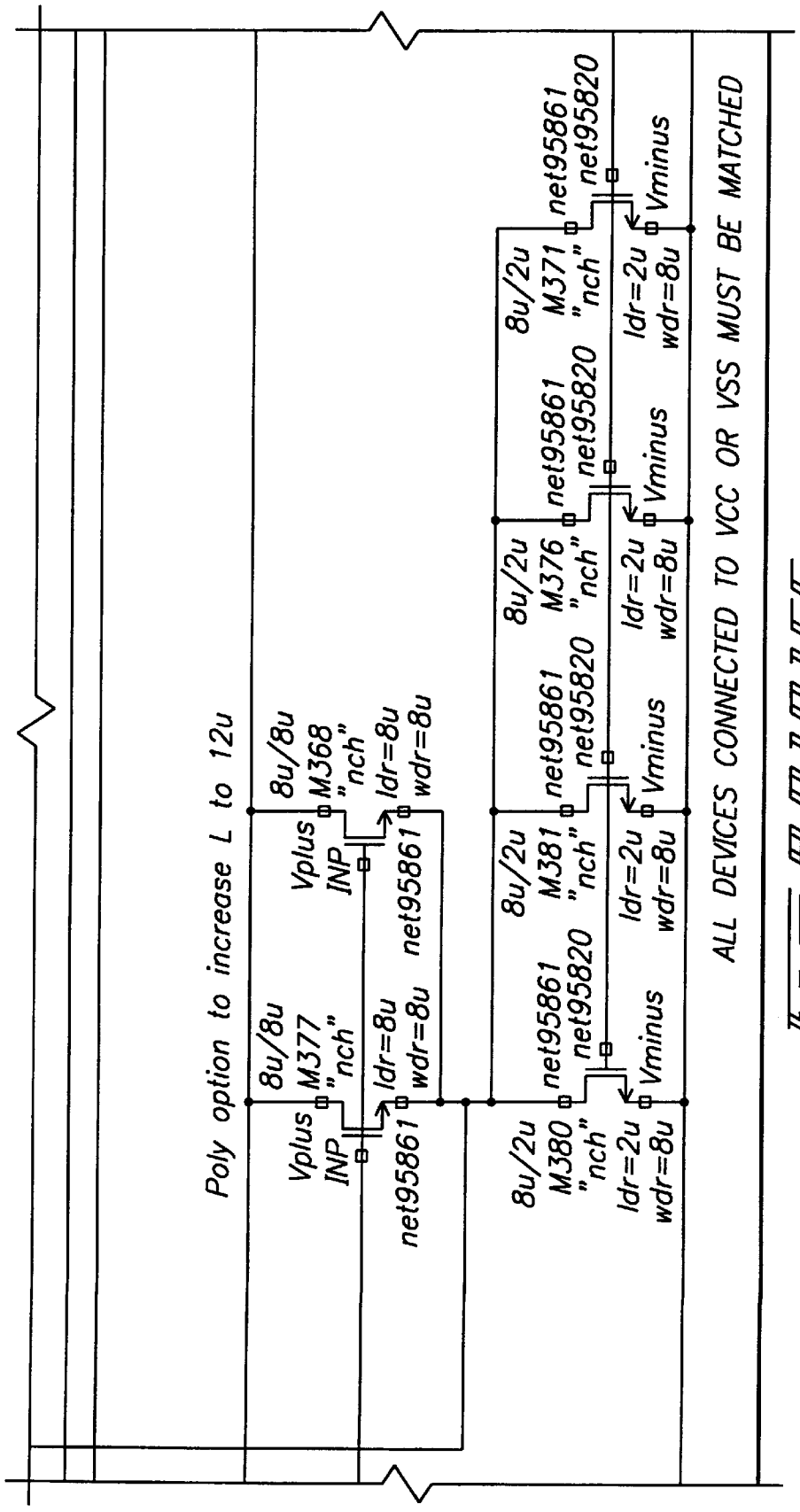


FIG. 9.III.IIIE

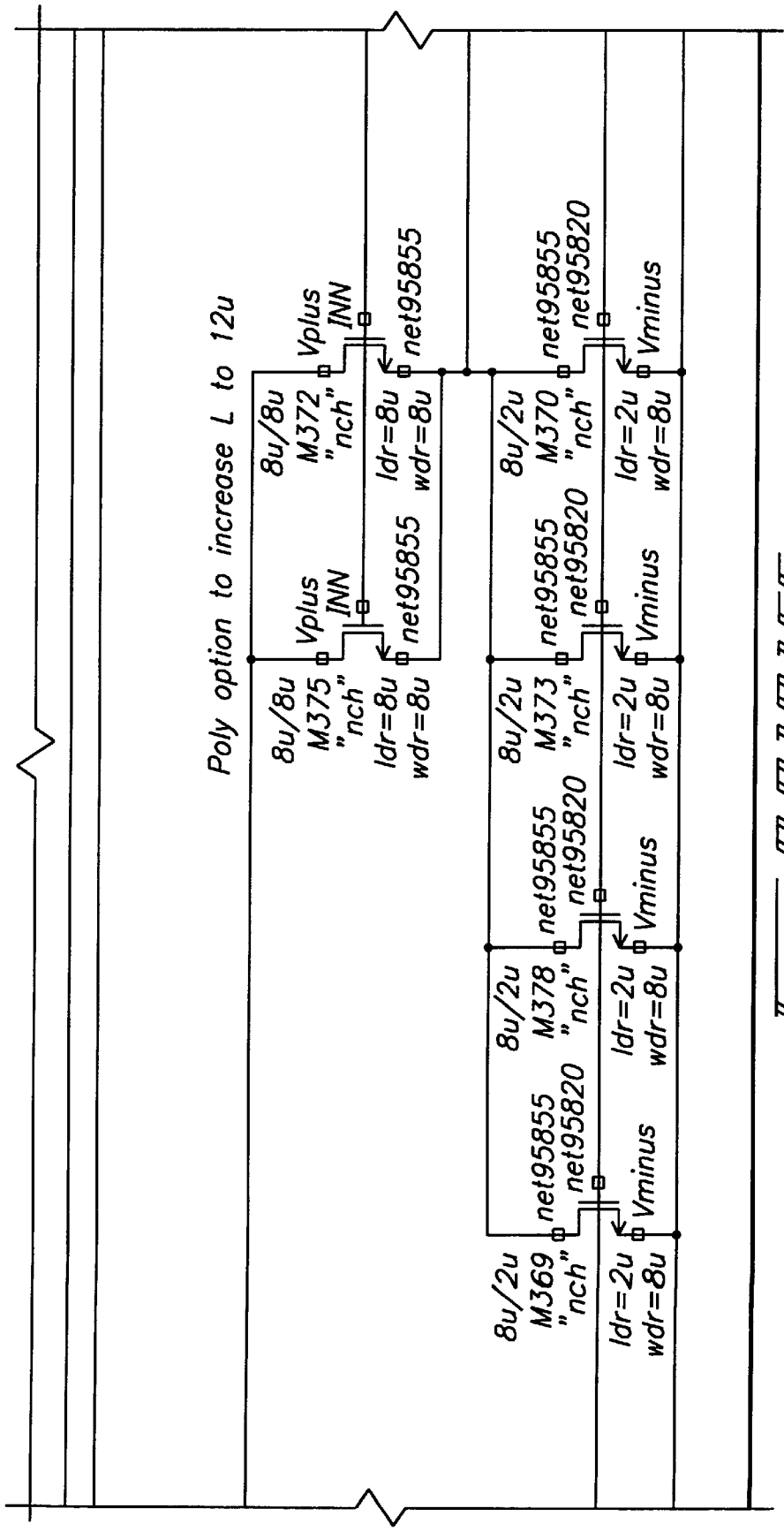

Poly option to increase L to 12u
8u/8u
M372
"nch"
ldr=8u
wdr=8u
Vplus
INN
net95855
8u/8u
M375
"nch"
ldr=8u
wdr=8u
Vplus
INN
net95855
8u/2u
M370
"nch"
ldr=2u
wdr=8u
net95855
net95820
Vminus
8u/2u
M373
"nch"
ldr=2u
wdr=8u
net95855
net95820
Vminus
8u/2u
M378
"nch"
ldr=2u
wdr=8u
net95855
net95820
Vminus
8u/2u
M369
"nch"
ldr=2u
wdr=8u
net95855
net95820
Vminus

FIG. 9,011

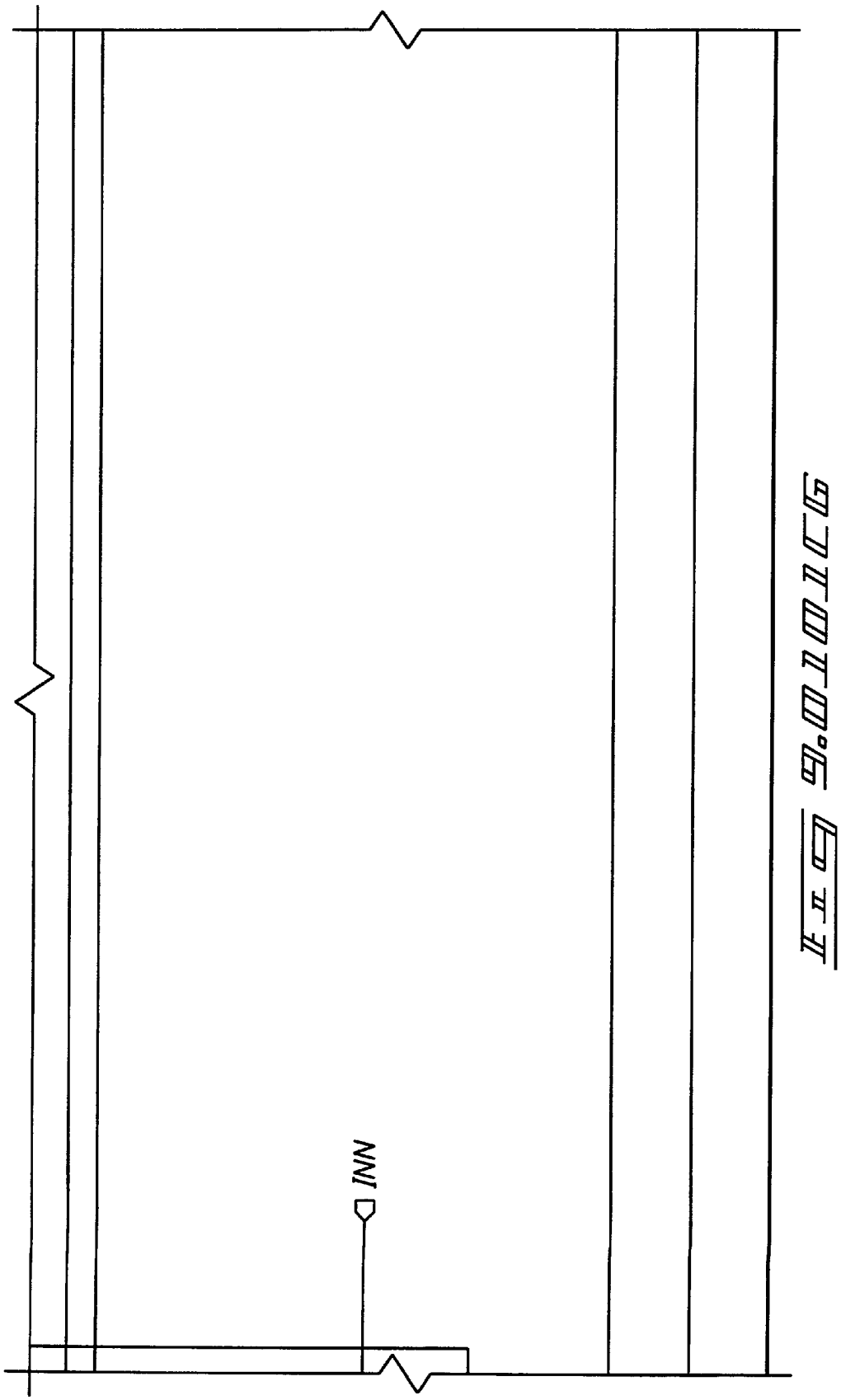


FIG. 95.01
INI

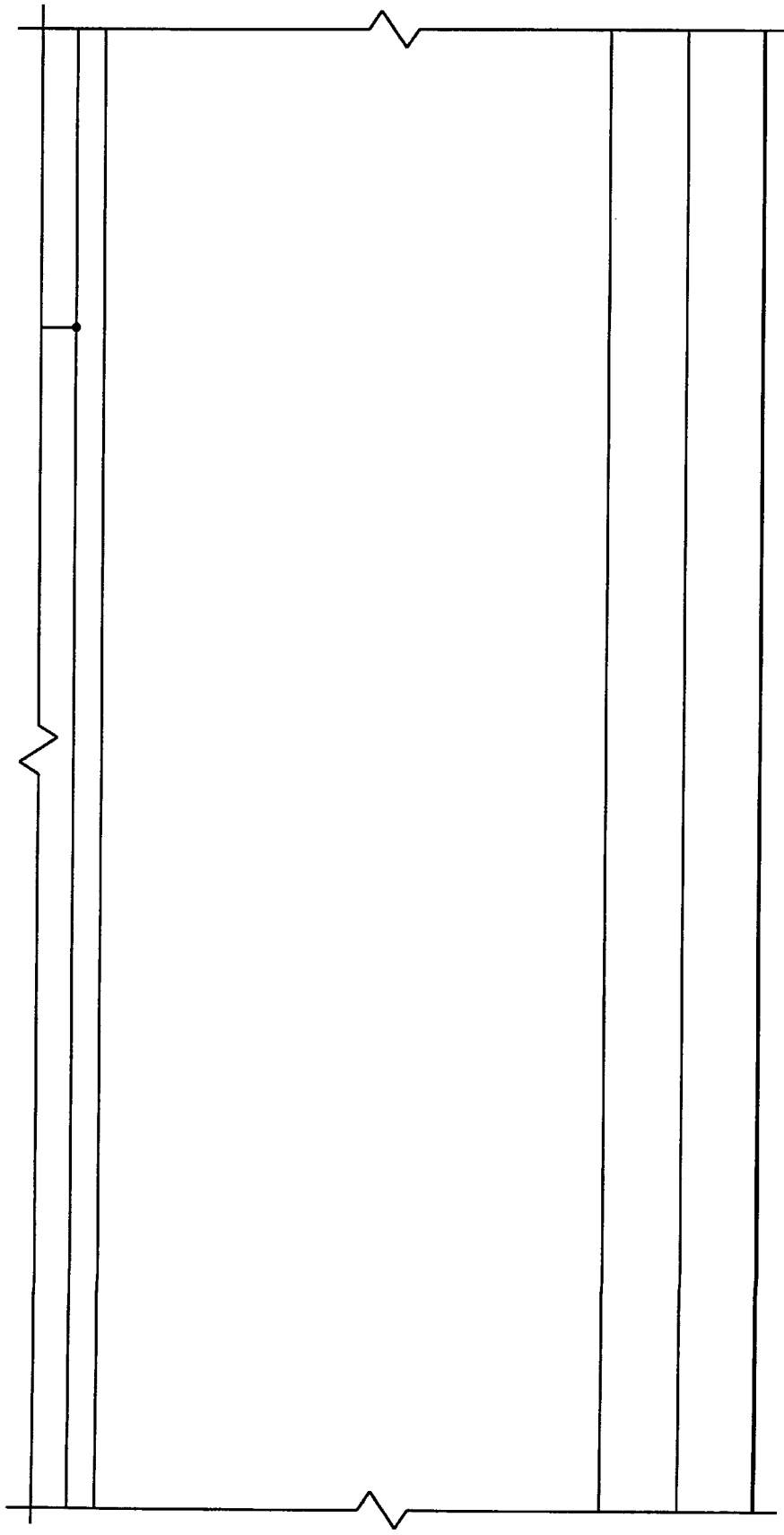


FIG 9,011CH

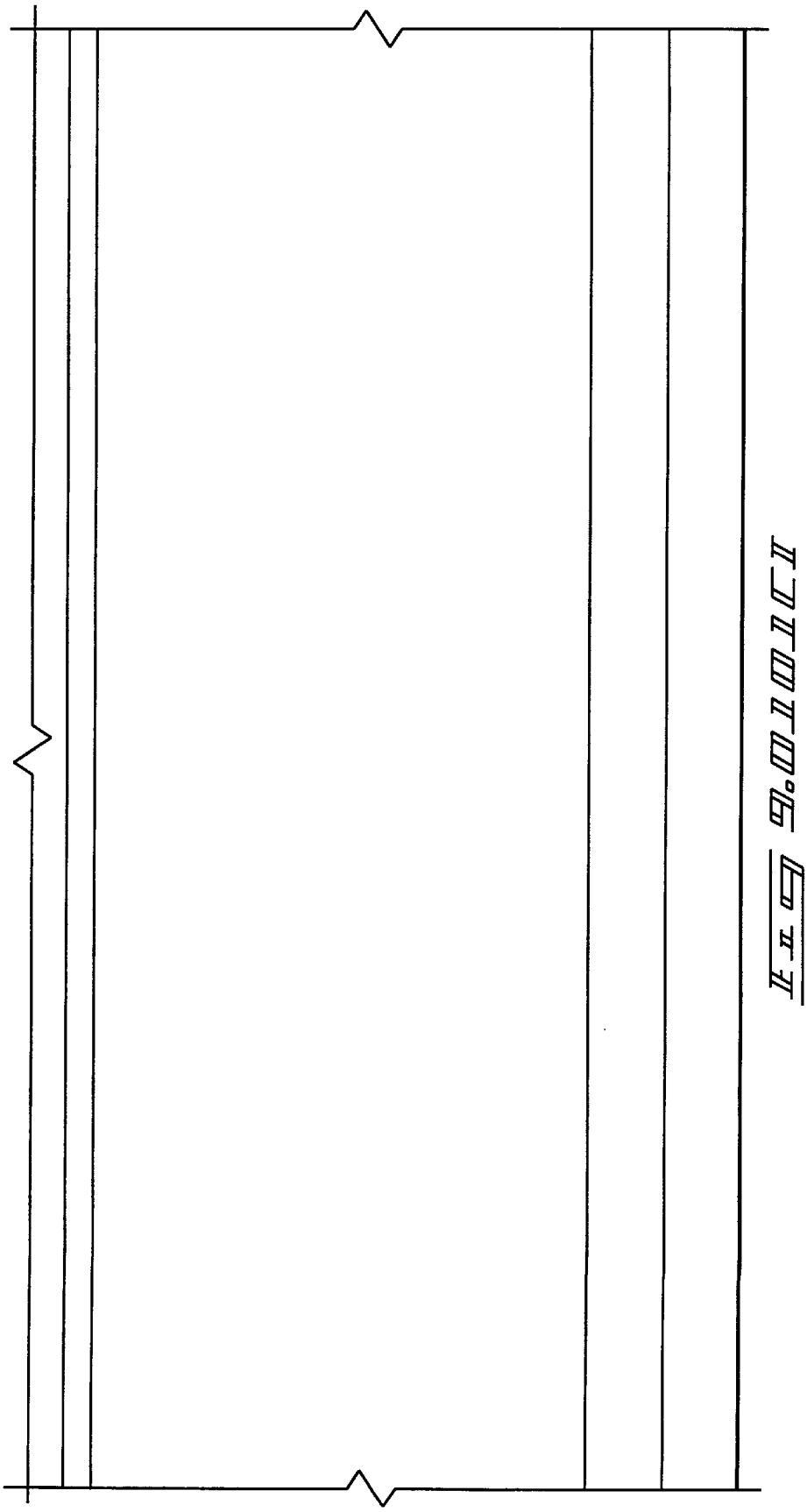


FIG. 95

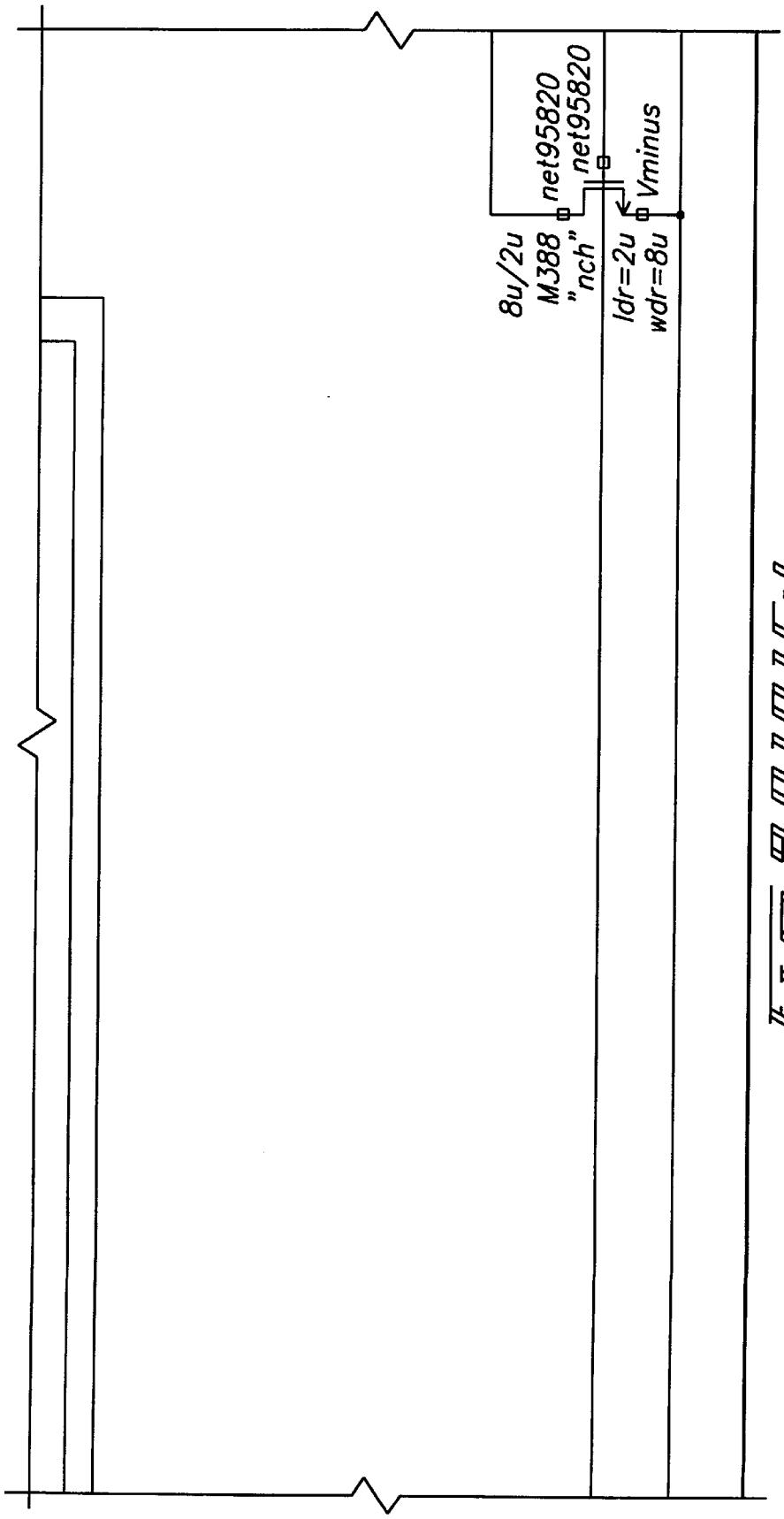


FIG 9.00116

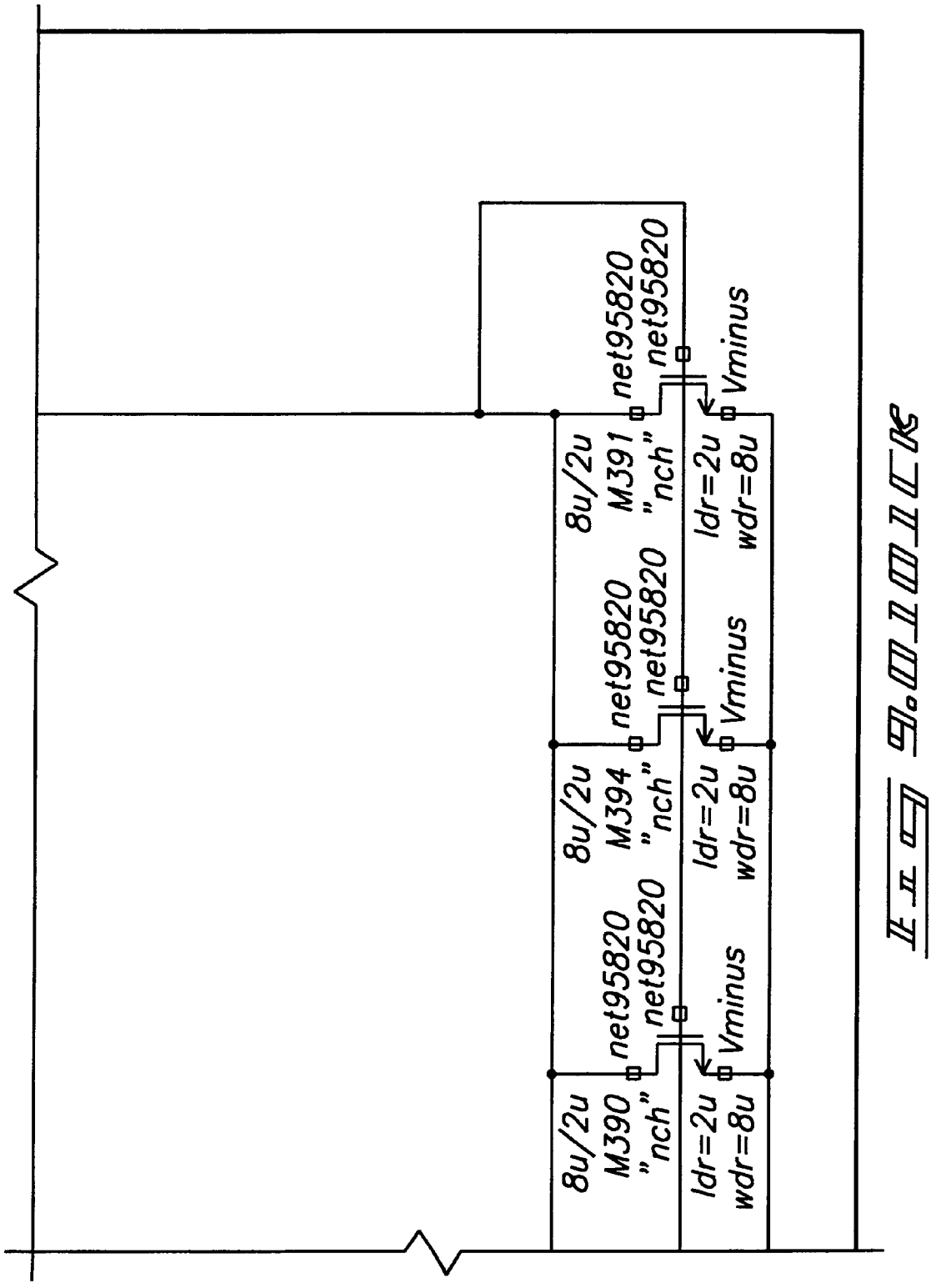

8u/2u
M391
"nch"
ldr=2u
wdr=8u
net95820
net95820
Vminus
8u/2u
M394
"nch"
ldr=2u
wdr=8u
net95820
net95820
Vminus
8u/2u
M390
"nch"
ldr=2u
wdr=8u
net95820
net95820
Vminus

FIG 99

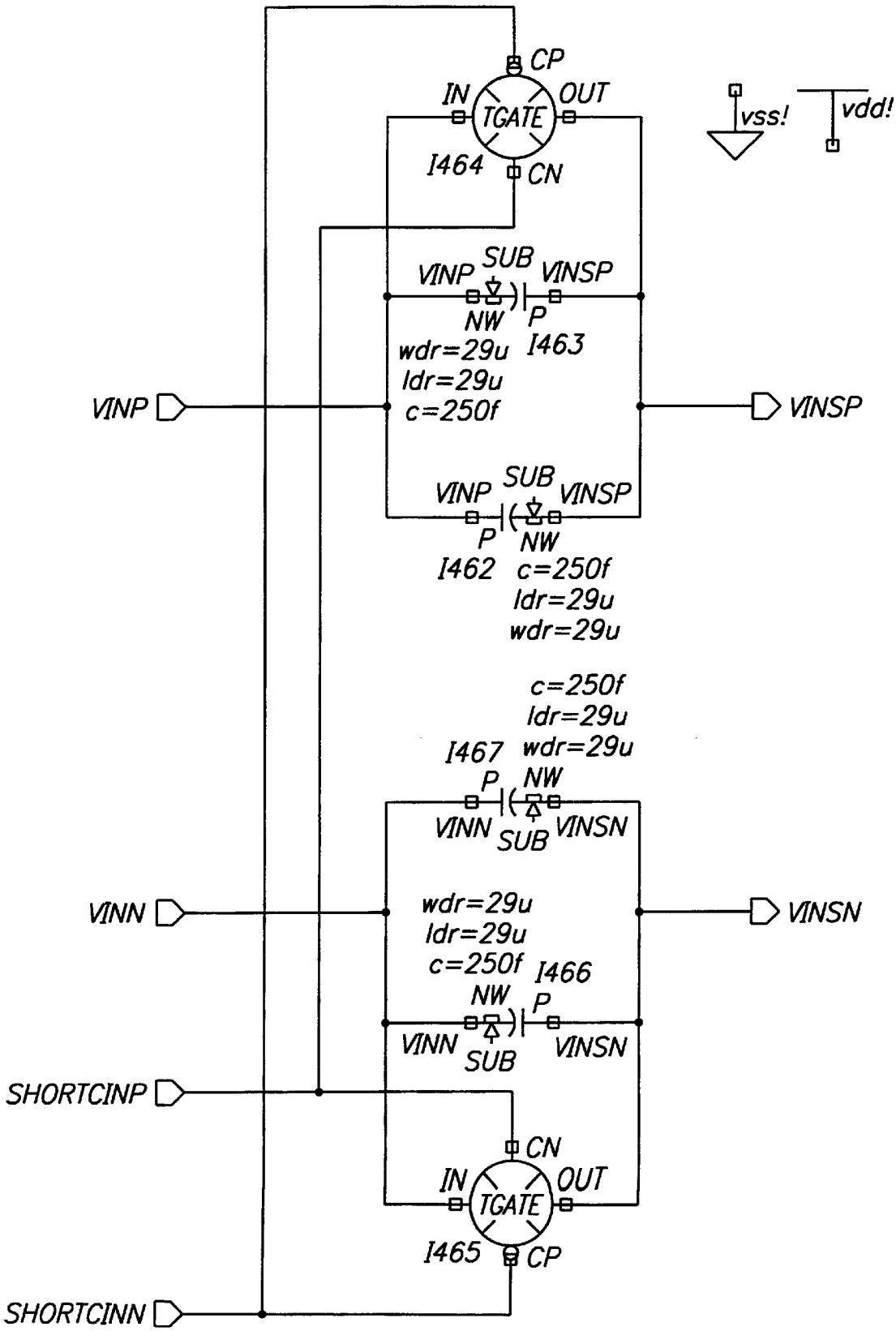

CP
IN
TGATE
OUT
I464
CN
vss!
vdd!
VINP
SUB
VINSP
NW
P
wdr=29u
ldr=29u
c=250f
I463
VINP
VINSP
VINP
SUB
VINSP
P
NW
I462
c=250f
ldr=29u
wdr=29u
c=250f
ldr=29u
I467
wdr=29u
P
NW
VINN
SUB
VINSN
VINN
VINSN
wdr=29u
ldr=29u
c=250f
I466
NW
P
VINN
SUB
VINSN
SHORTCINP
CN
IN
TGATE
OUT
I465
CP
SHORTCINN

Fig 9.0102

9.0103BA	9.0103BB	9.0103BC	9.0103BD	9.0103BE	9.0103BF	9.0103BG	9.0103BH	9.0103AJ	9.0103AK	9.0103AL	9.0103AM	9.0103AN	9.0103AO	9.0103AP
9.0103CA	9.0103CB	9.0103CC	9.0103CD	9.0103CE	9.0103CF	9.0103CG	9.0103CH	9.0103CI	9.0103BJ	9.0103BK	9.0103BL	9.0103BM	9.0103BN	9.0103BO	9.0103BP
9.0103DA	9.0103DB	9.0103DC	9.0103DD	9.0103DE	9.0103DF	9.0103DG	9.0103DH	9.0103DI	9.0103CJ	9.0103CK	9.0103CL	9.0103CM	9.0103CN	9.0103CO	9.0103CP
9.0103EA	9.0103EB	9.0103EC	9.0103ED	9.0103EE	9.0103EF	9.0103EG	9.0103EH	9.0103EI	9.0103DJ	9.0103DK	9.0103DL	9.0103DM	9.0103DN	9.0103DO	9.0103DP
9.0103FA	9.0103FB	9.0103FC	9.0103FD	9.0103FE	9.0103FF	9.0103FG	9.0103FH	9.0103FI	9.0103EJ	9.0103EK	9.0103EL	9.0103EM	9.0103EN	9.0103EO	9.0103EP
									9.0103FJ	9.0103FK	9.0103FL	9.0103FM	9.0103FN	9.0103FO	9.0103FP

FIG. 9.0103E

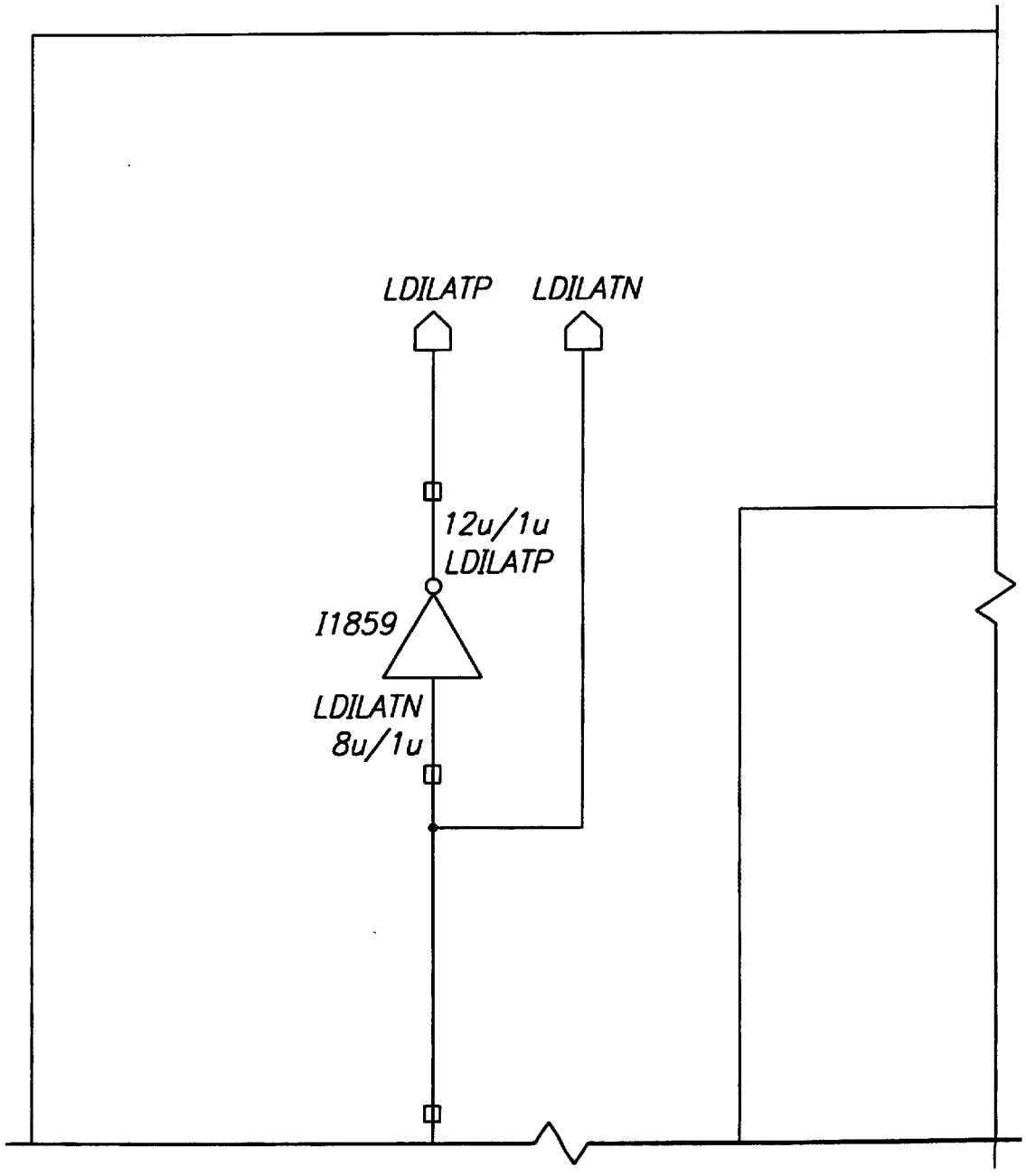


Fig 9.0110Aa

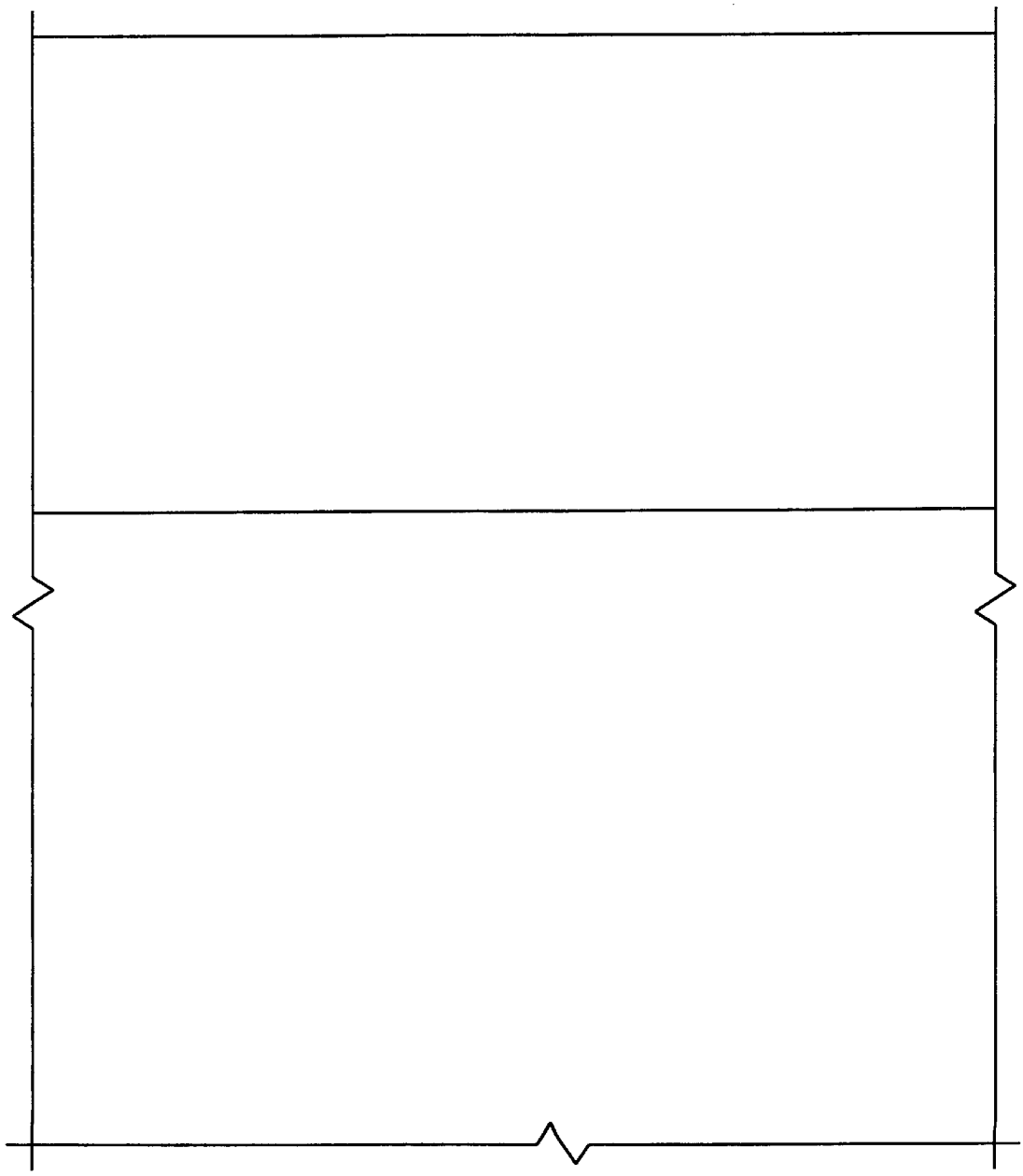


Fig 9.0103AK

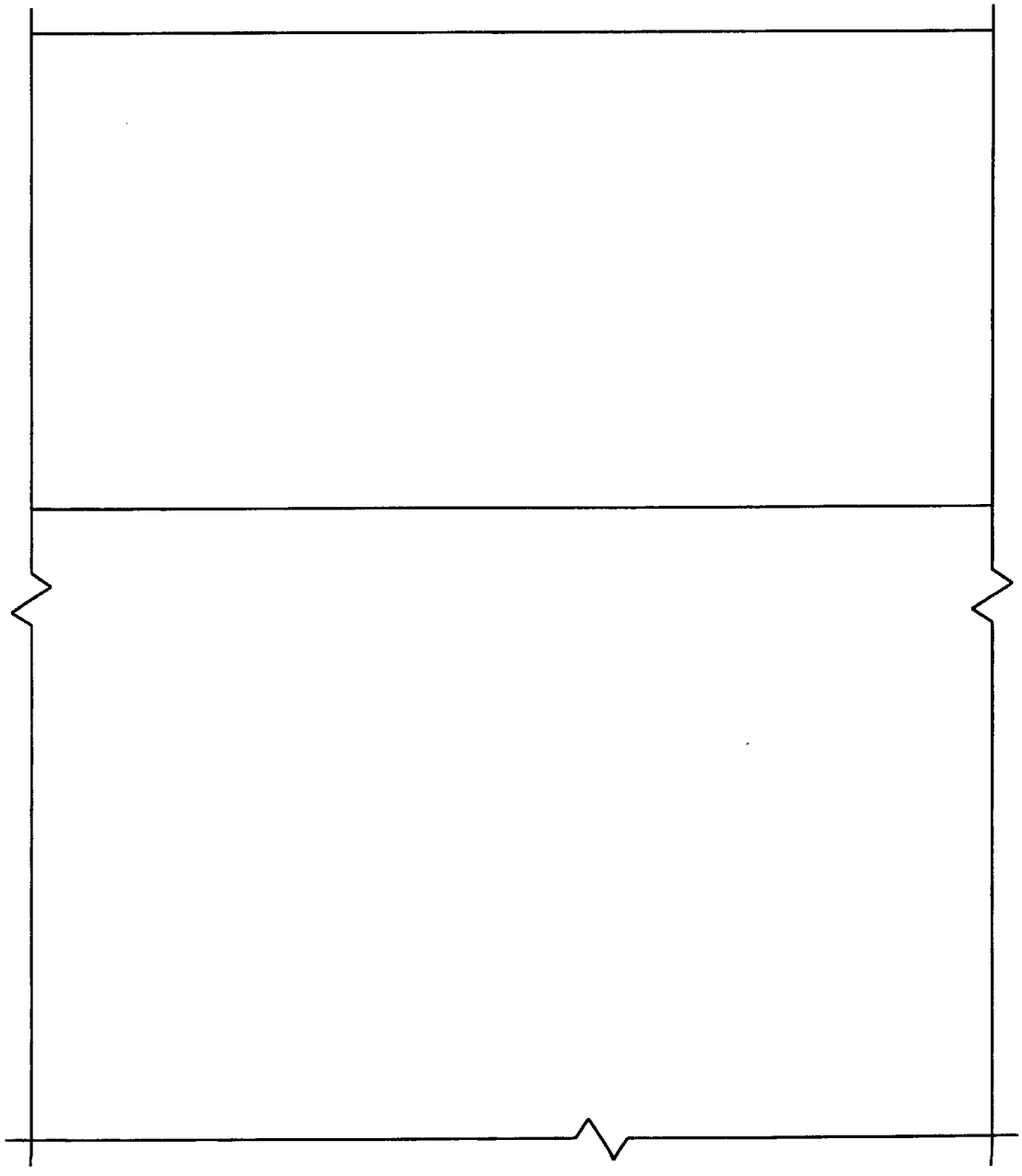


Fig 9.01030AL

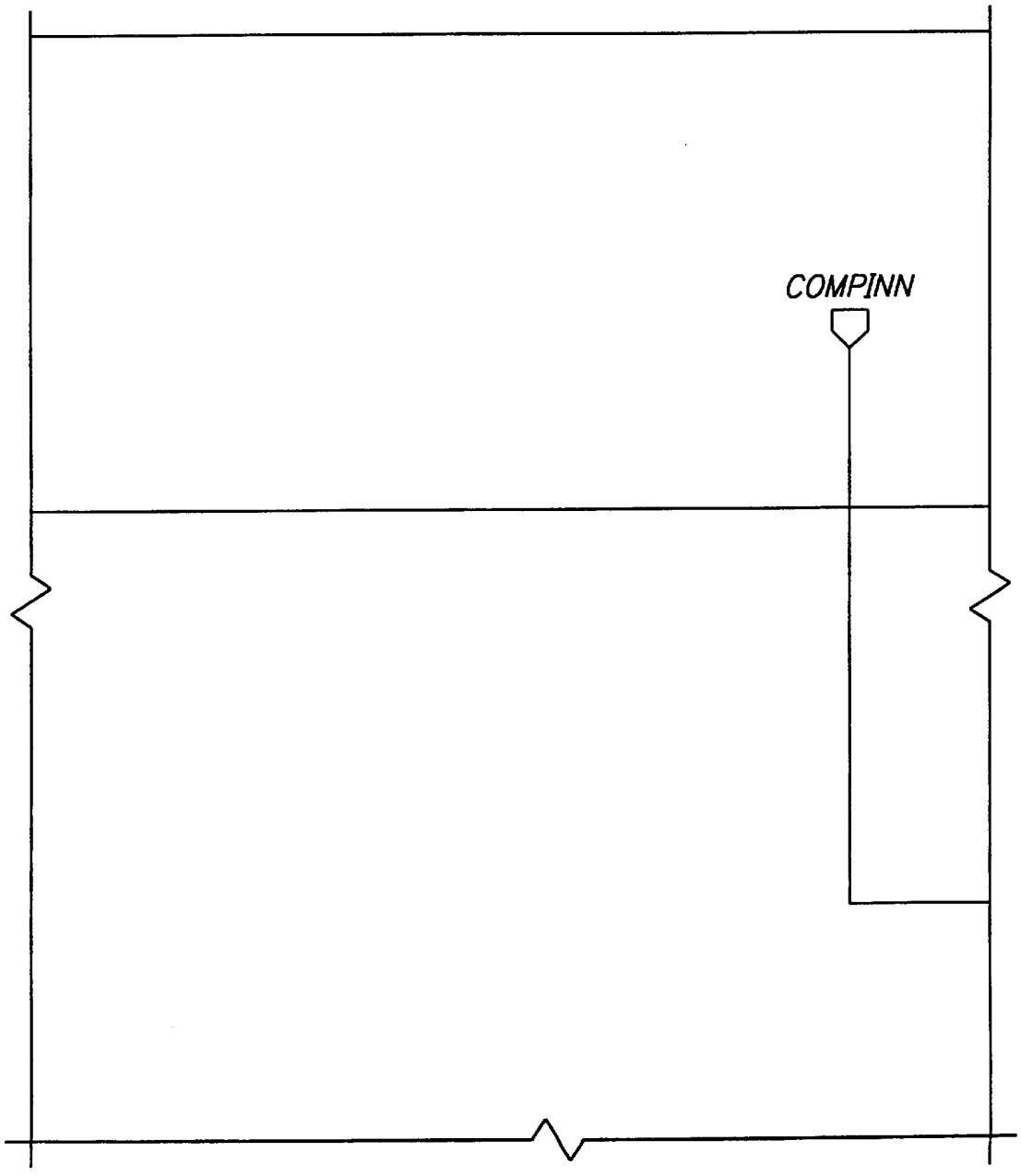


Fig 9.0110AM

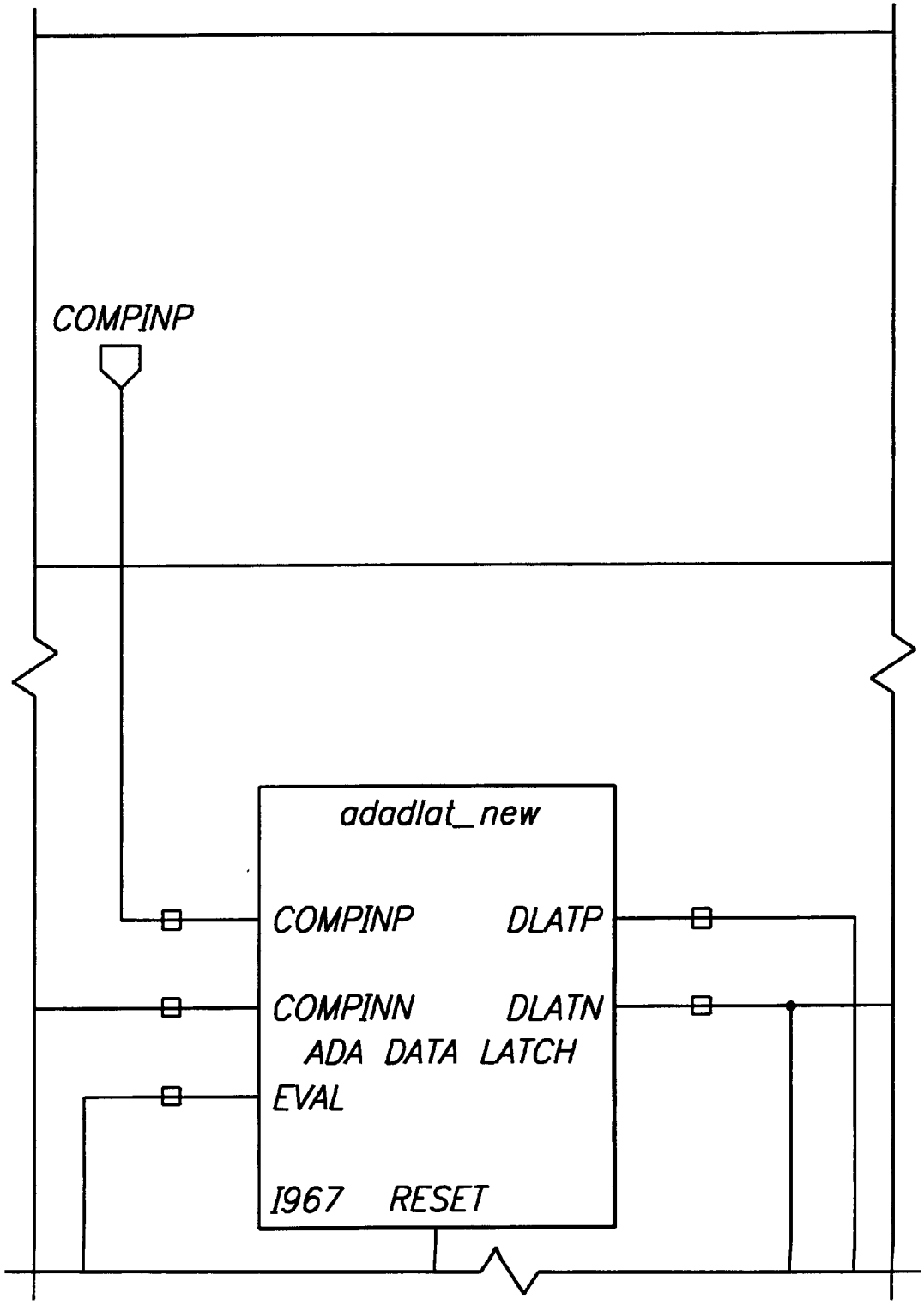

COMPINP
adadlat_new
COMPINP
DLATP
COMPINN
DLATN
ADA DATA LATCH
EVAL
1967 RESET

Fig 9.0103AN

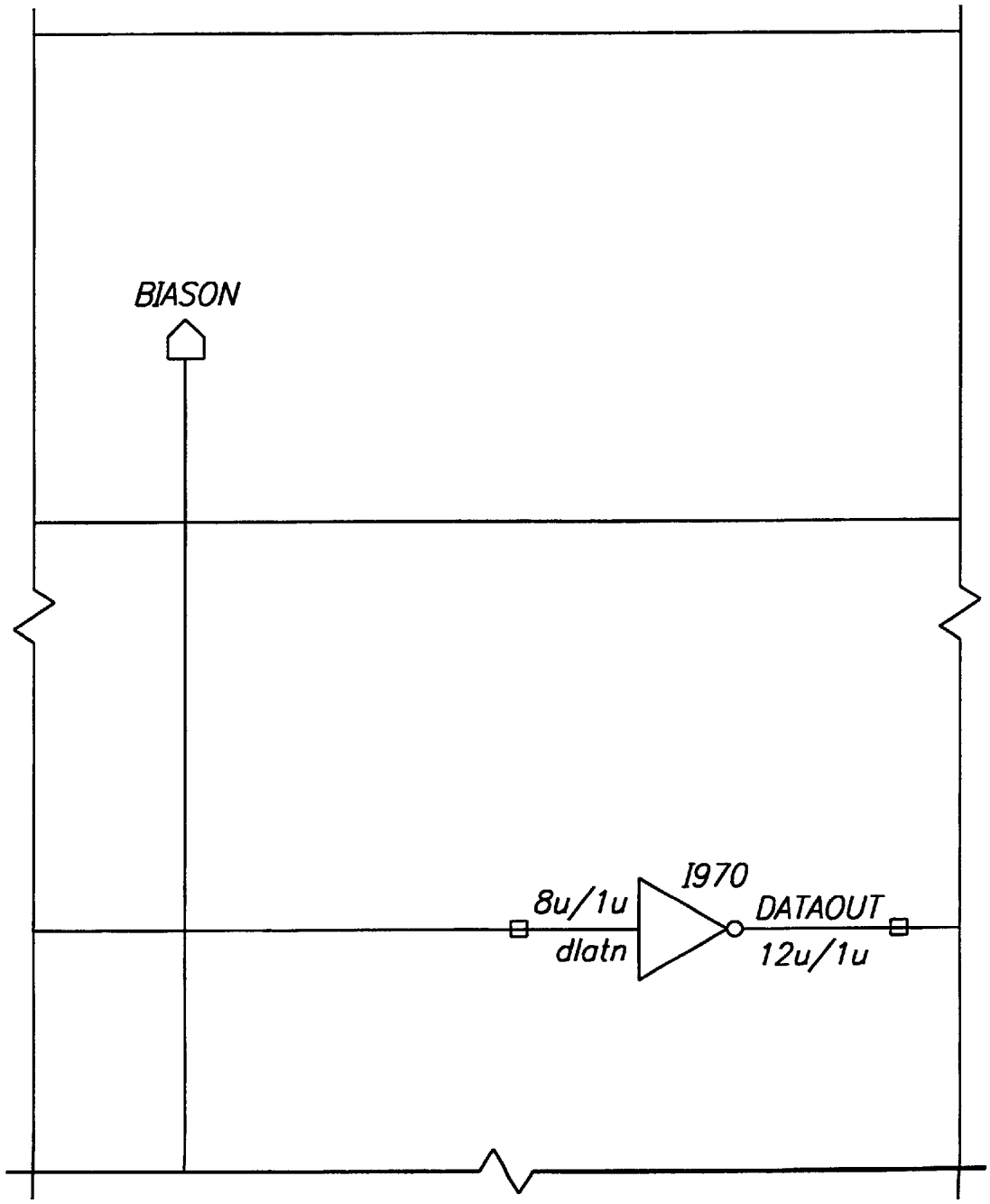


Fig 9.0110300

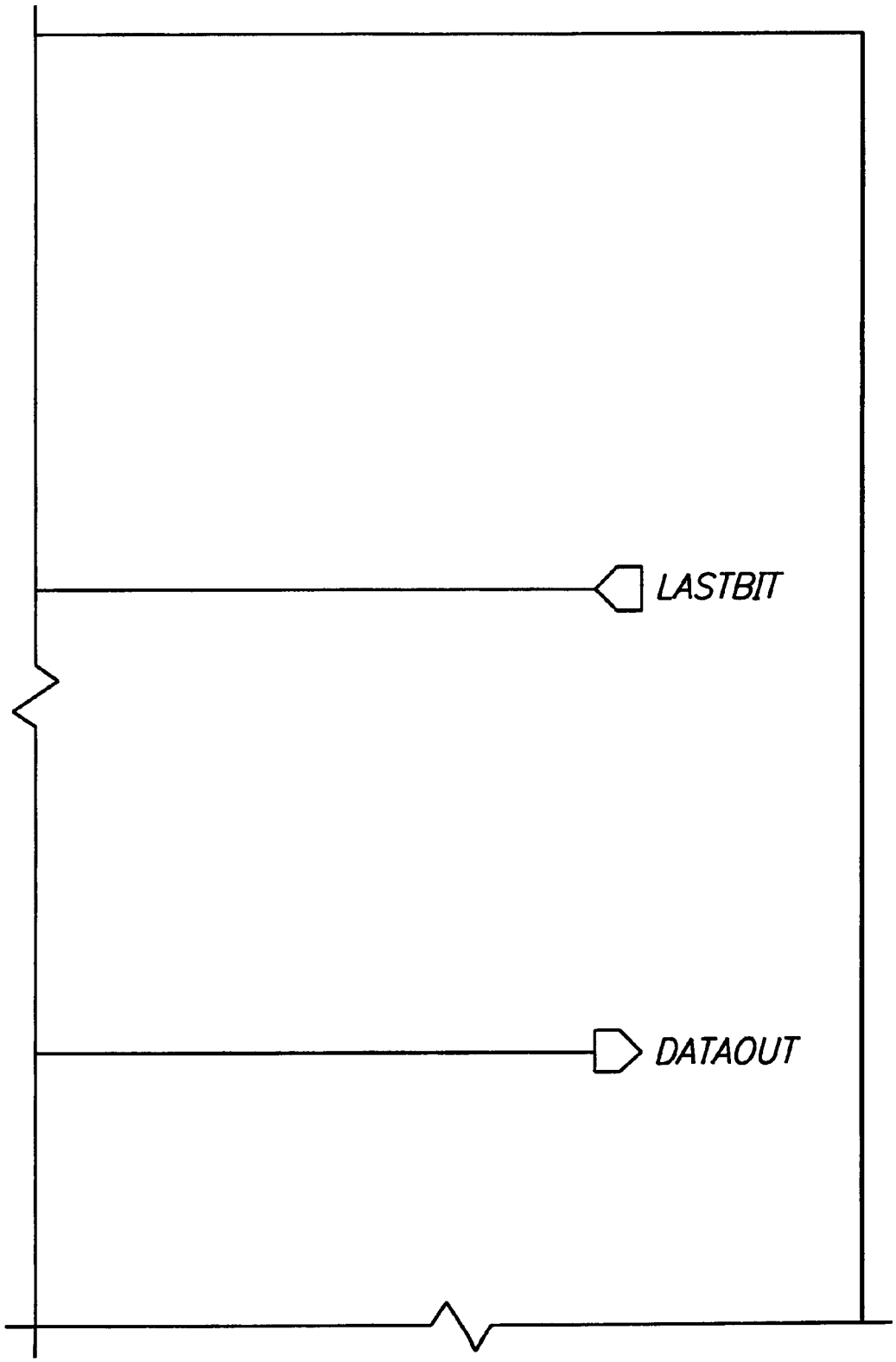


Fig 9.0103AP

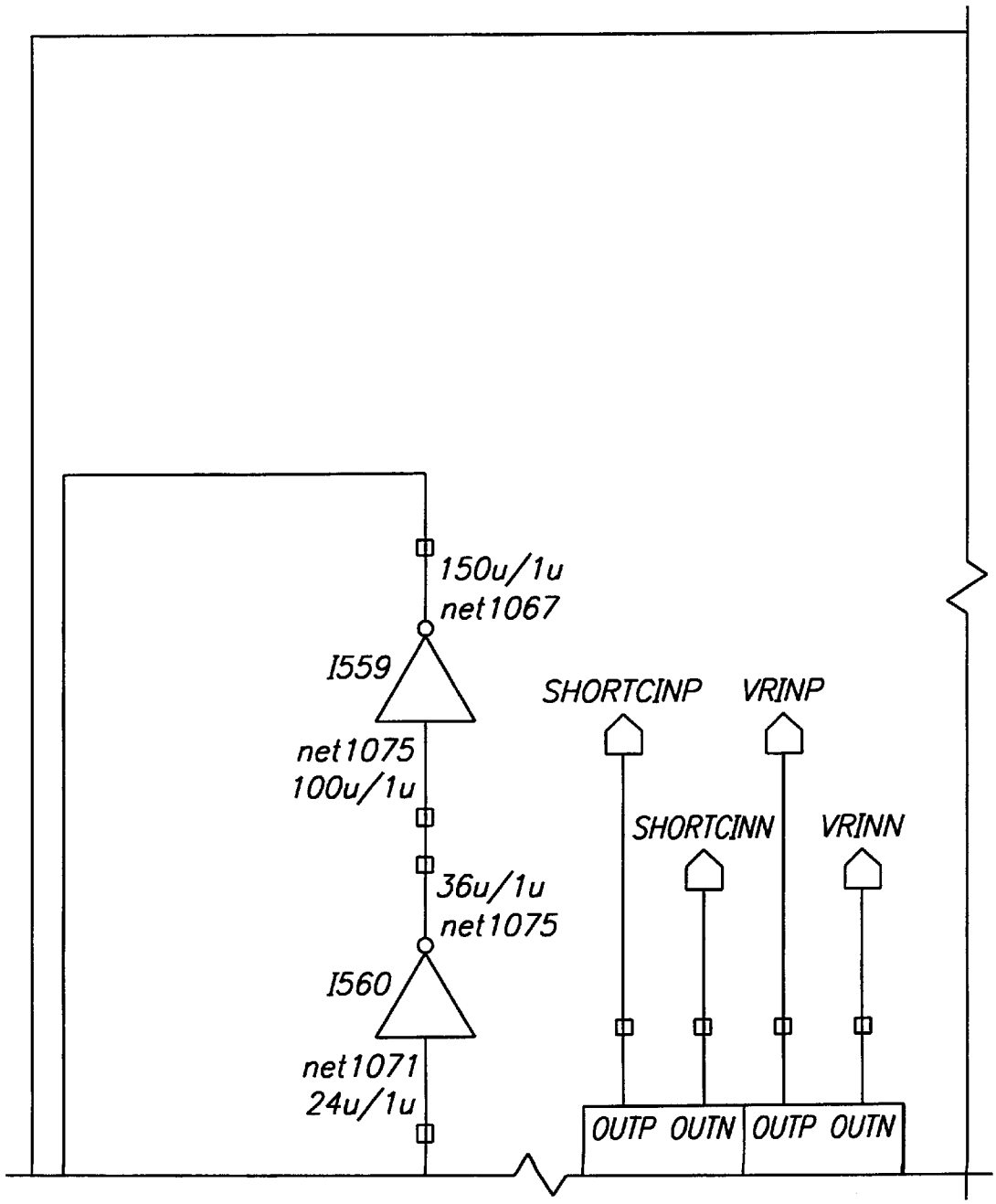

150u/1u
net1067
I559
net1075
100u/1u
36u/1u
net1075
I560
net1071
24u/1u
SHORTCINP
VRINP
SHORTCINN
VRINN
OUTP
OUTN
OUTP
OUTN

Fig 9.0103BA

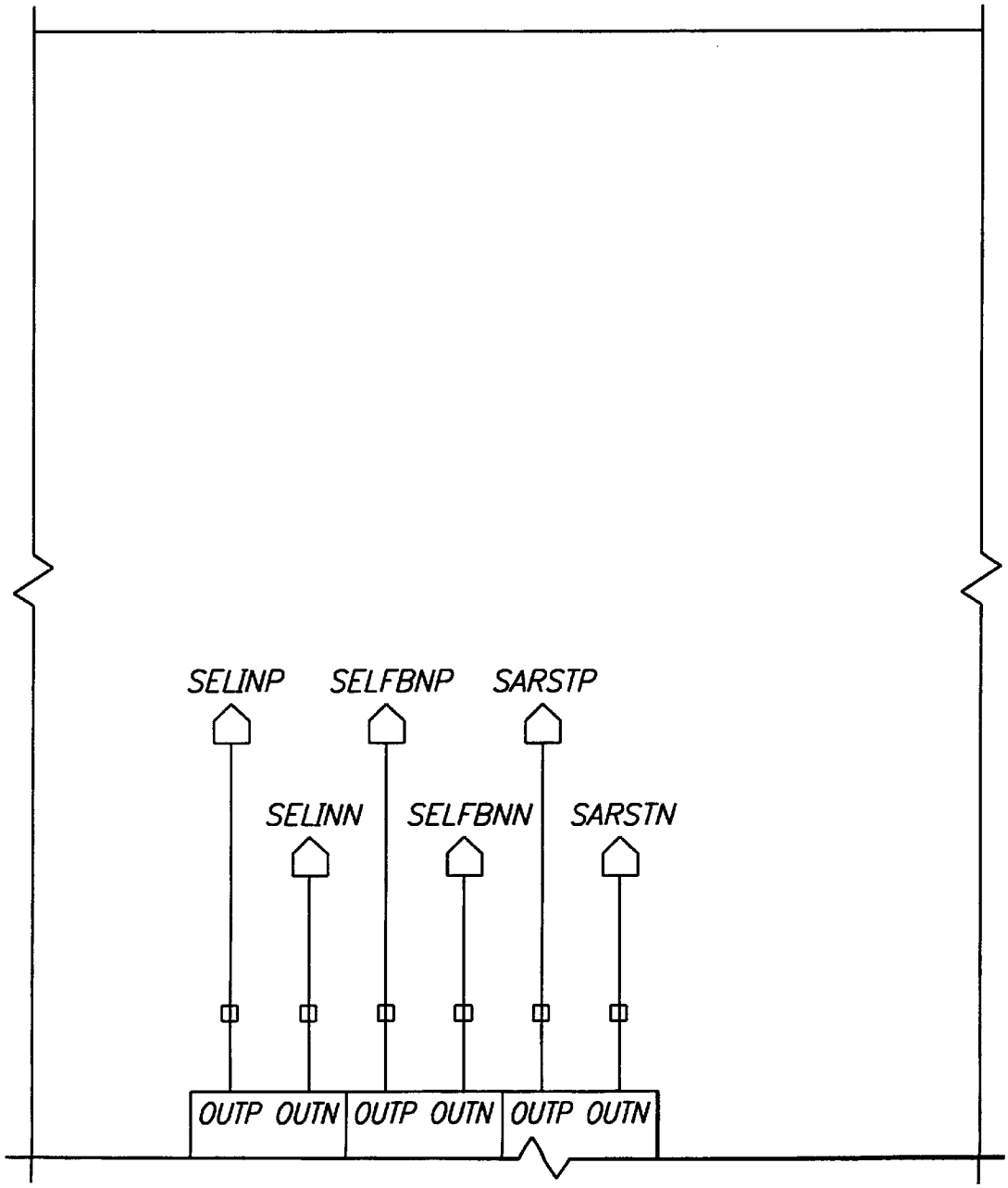


Fig 9.0110388

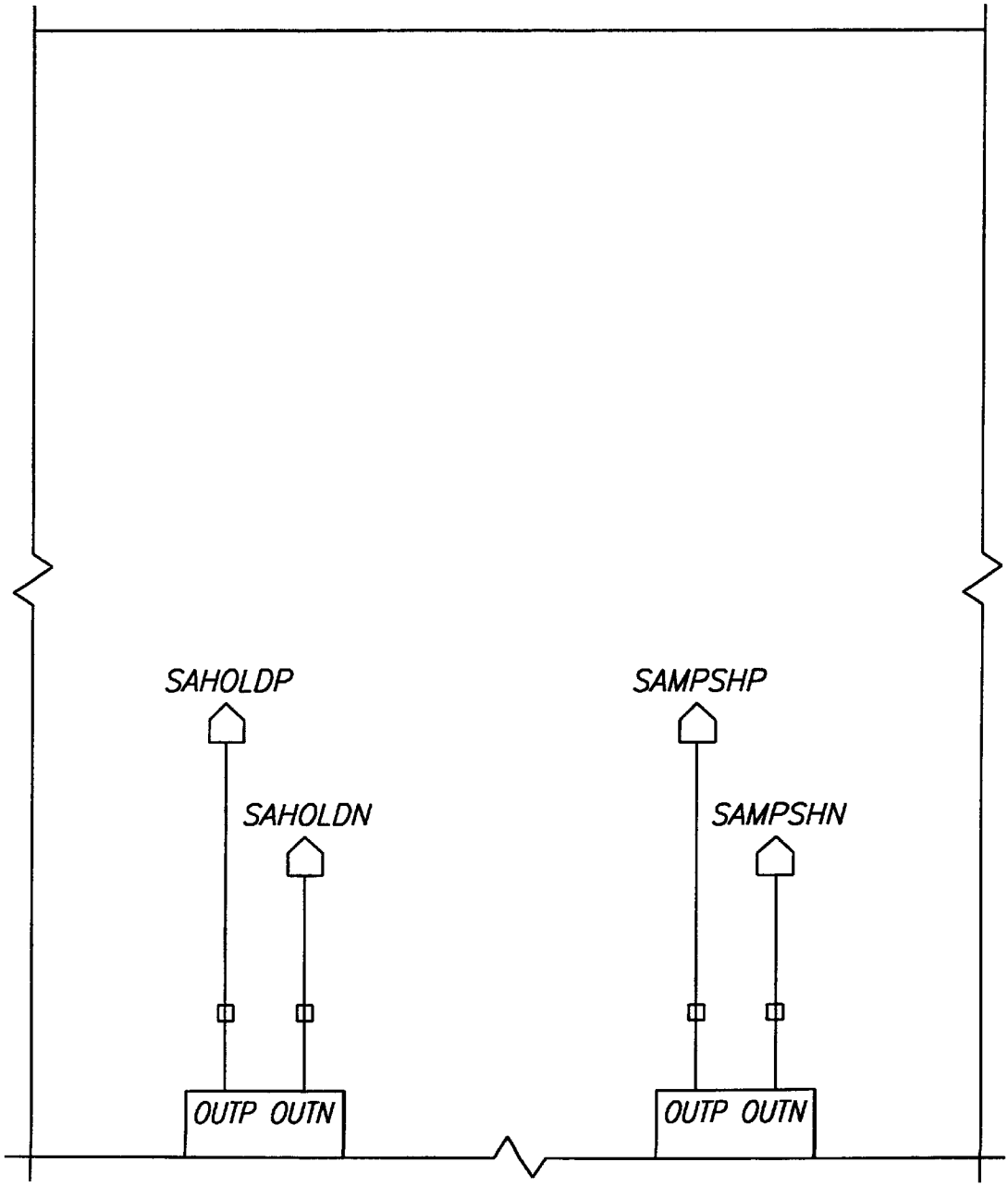


Fig 9.0110BC

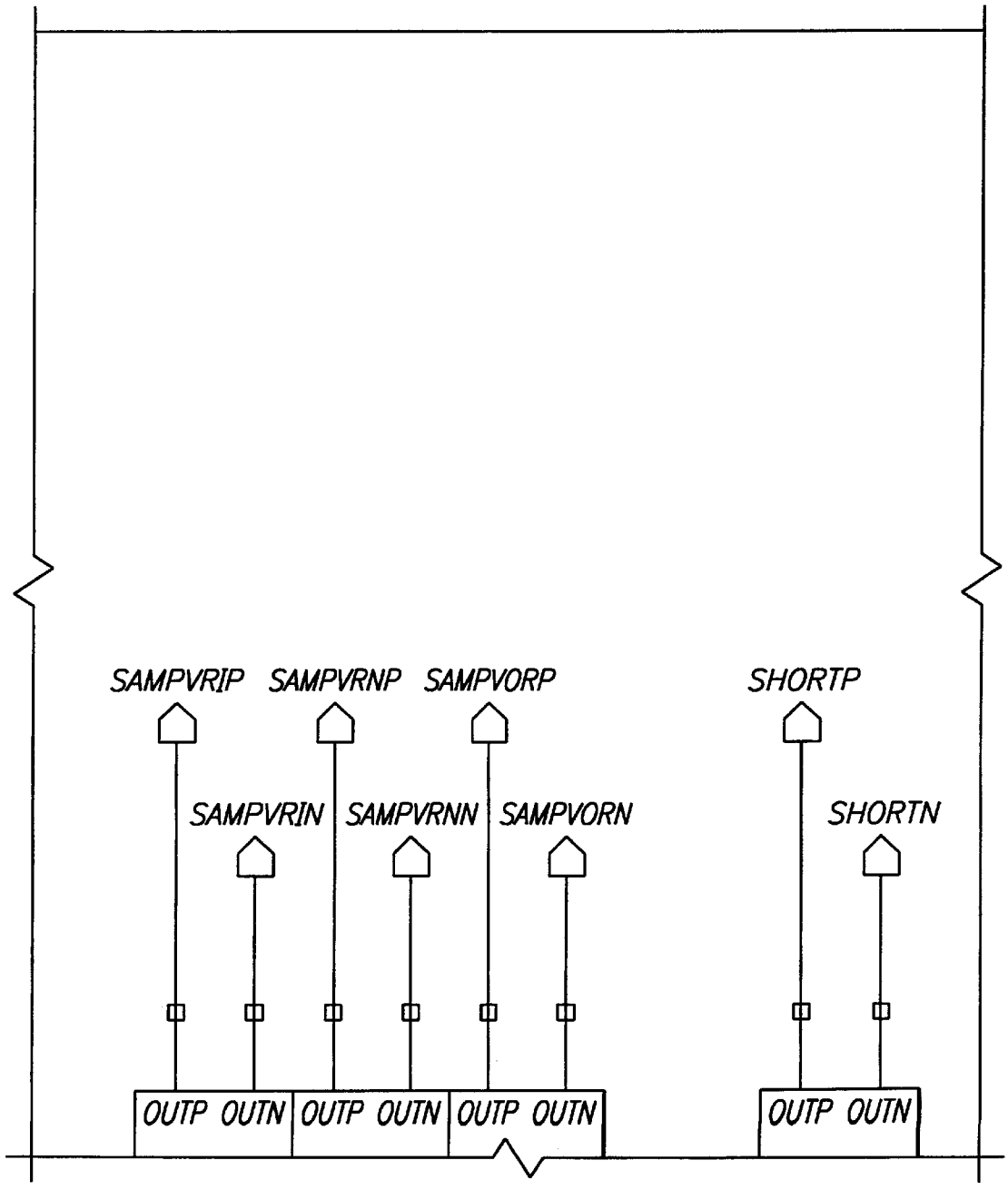

SAMPVRIP
SAMPVRNP
SAMPVORP
SHORTP
SAMPVRIN
SAMPVRNN
SAMPVORN
SHORTN
OUTP OUTN
OUTP OUTN
OUTP OUTN
OUTP OUTN

Fig 9.0103BD

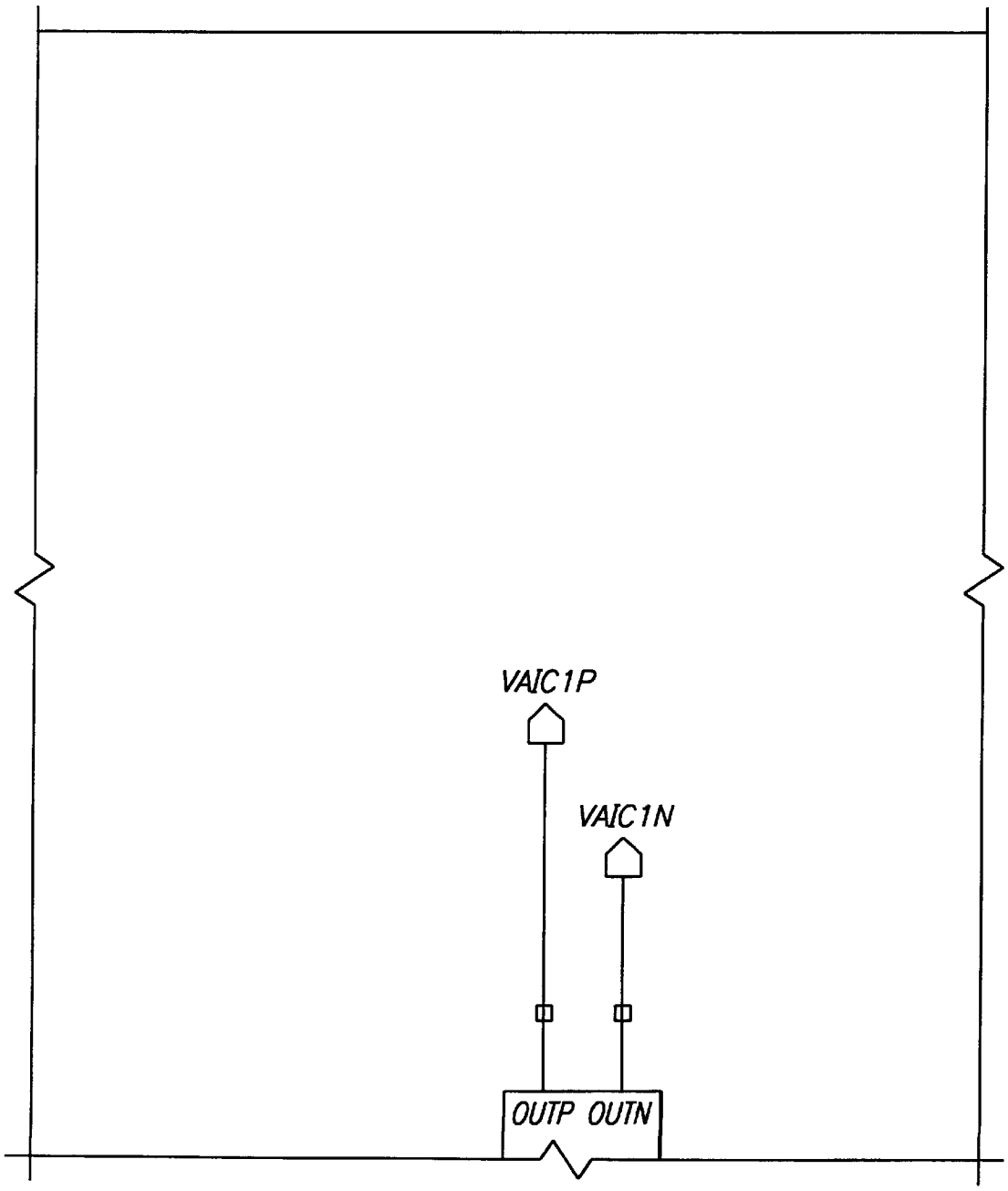


Fig 9.0103BE

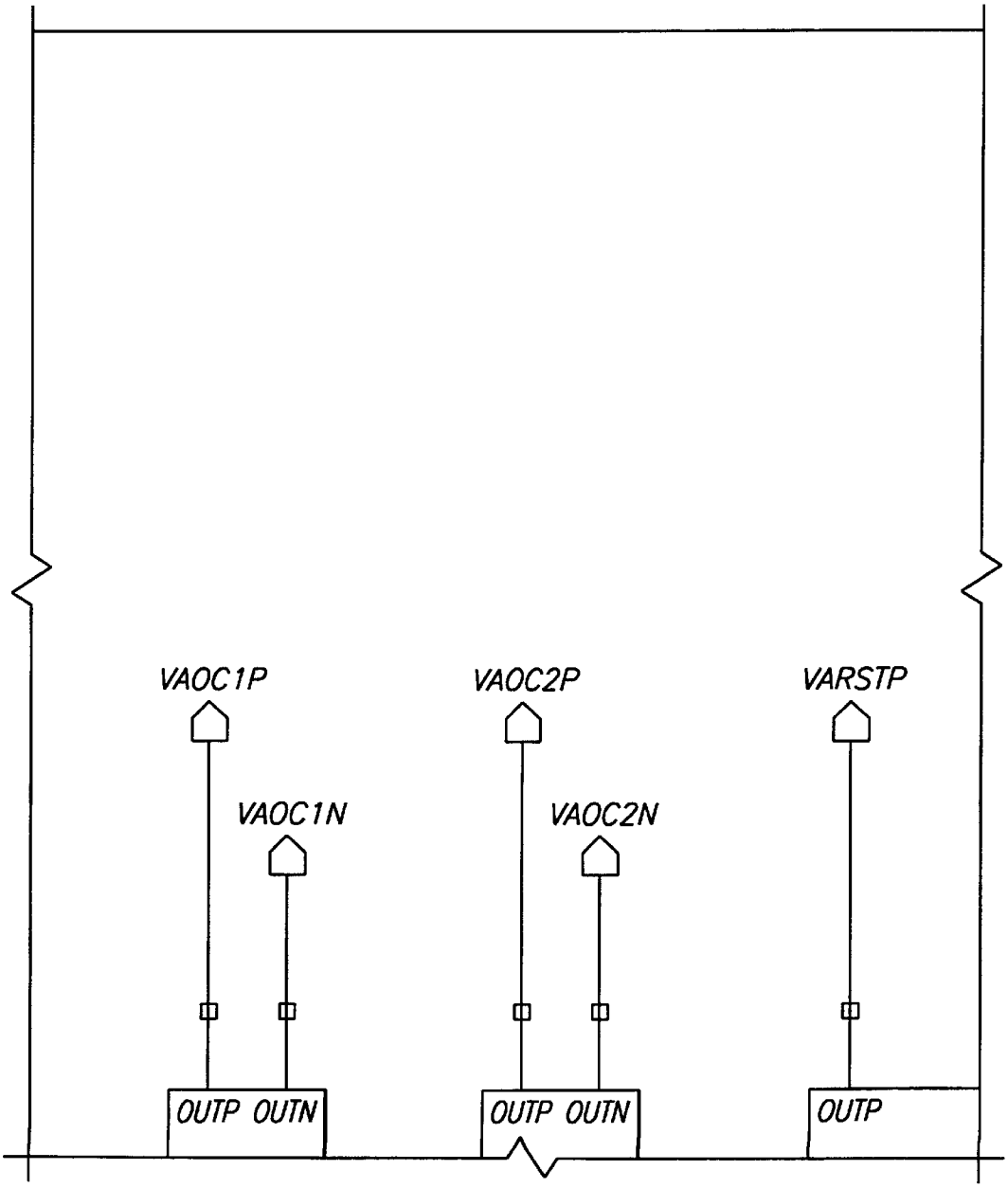

VAOC1P
VAOC2P
VARSTP
VAOC1N
VAOC2N
OUTP OUTN
OUTP OUTN
OUTP

Fig 9.0103BF

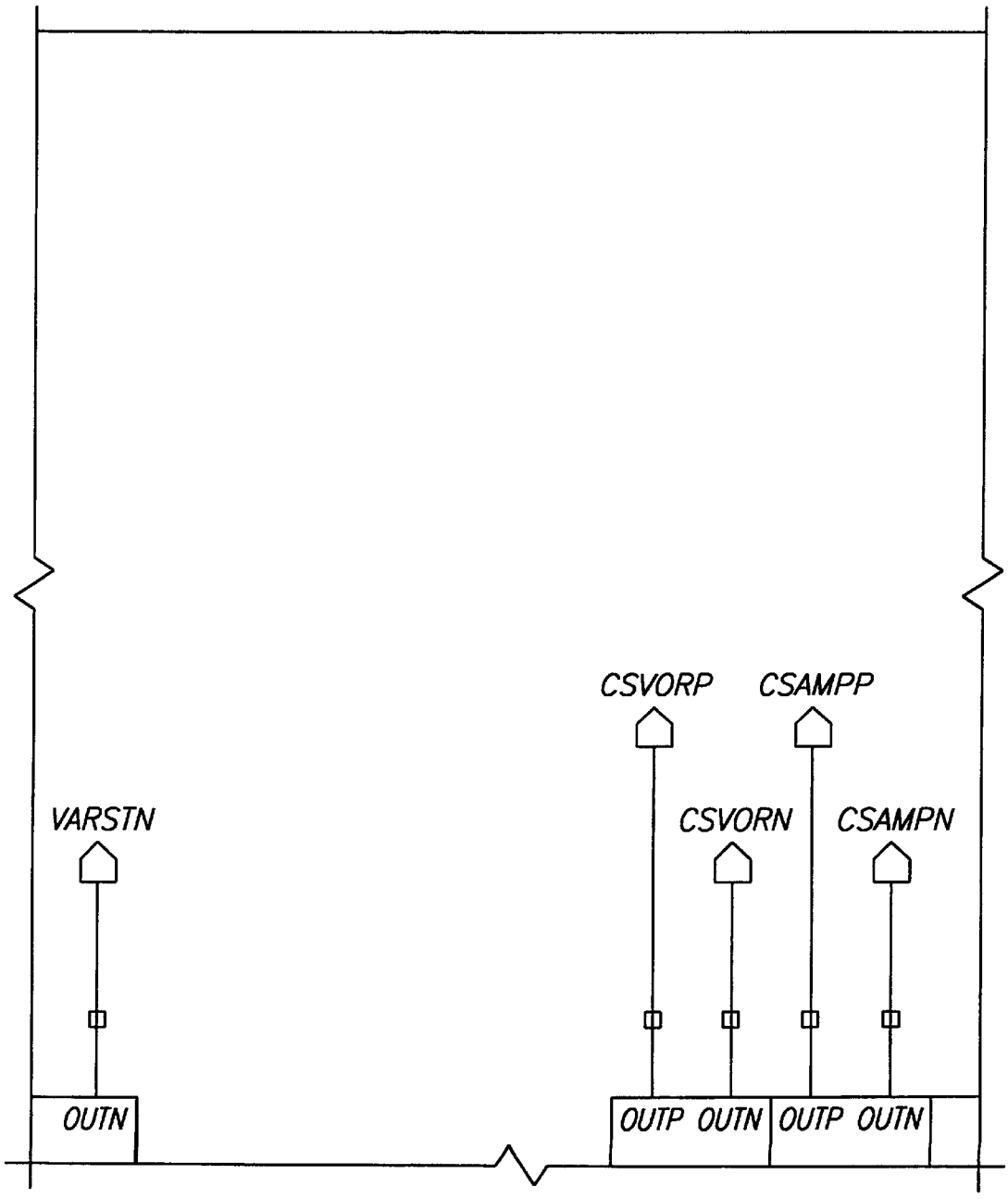

CSVORP
CSAMPP
VARSTN
CSVORN
CSAMPN
OUTN
OUTP OUTN OUTP OUTN

Fig 9.0103B6

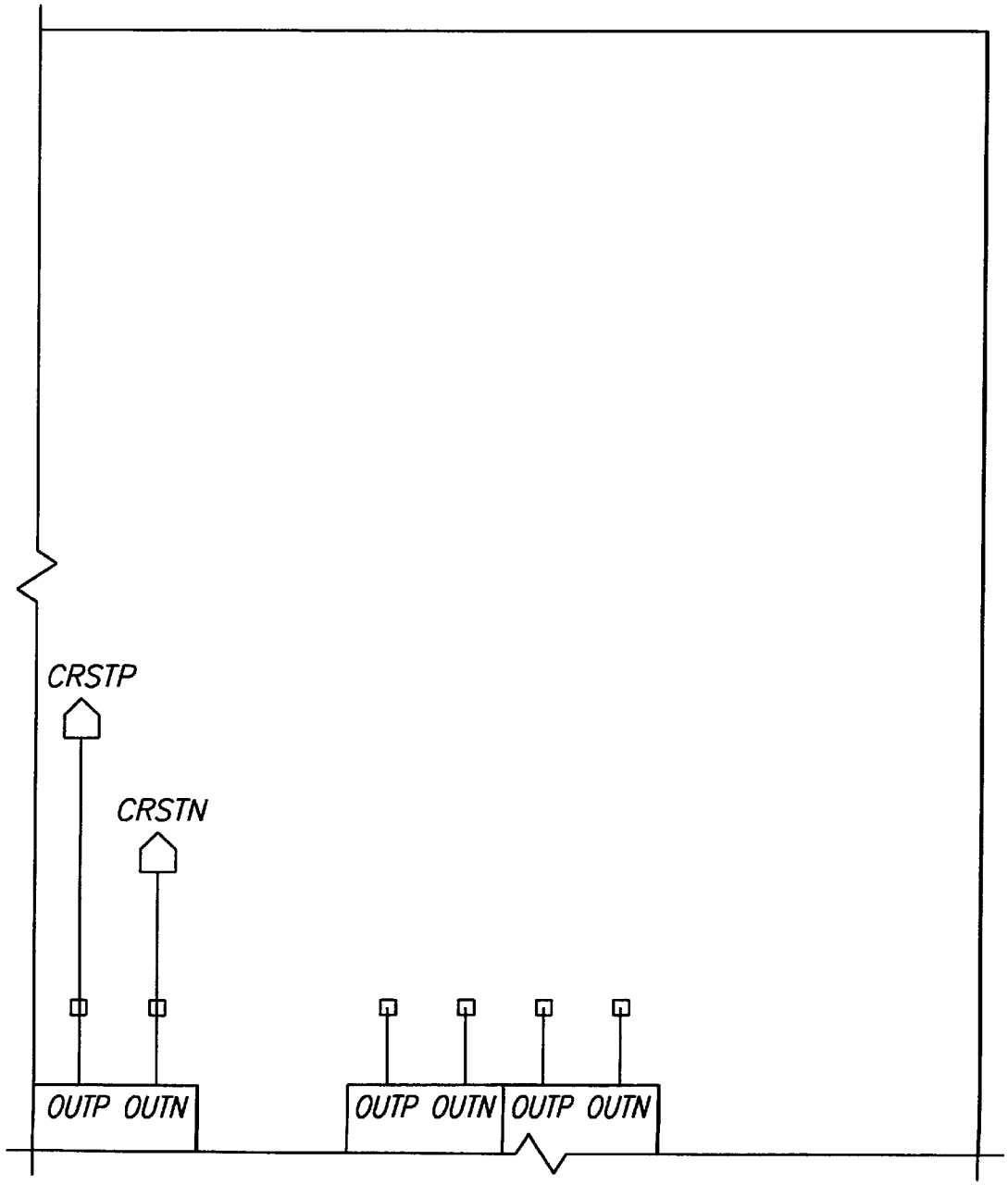


Fig 9.0103BH

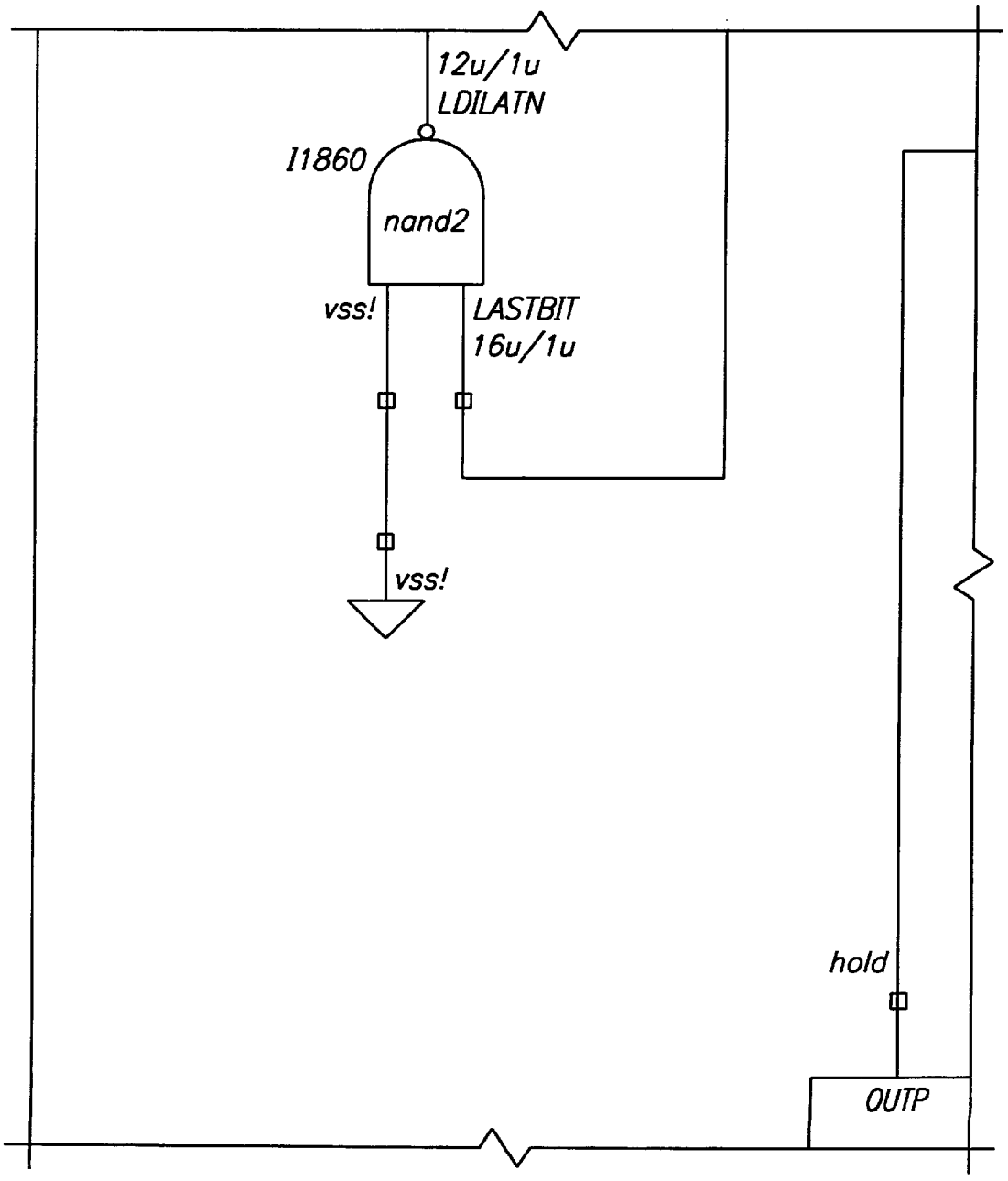


Fig 9.0103Bd

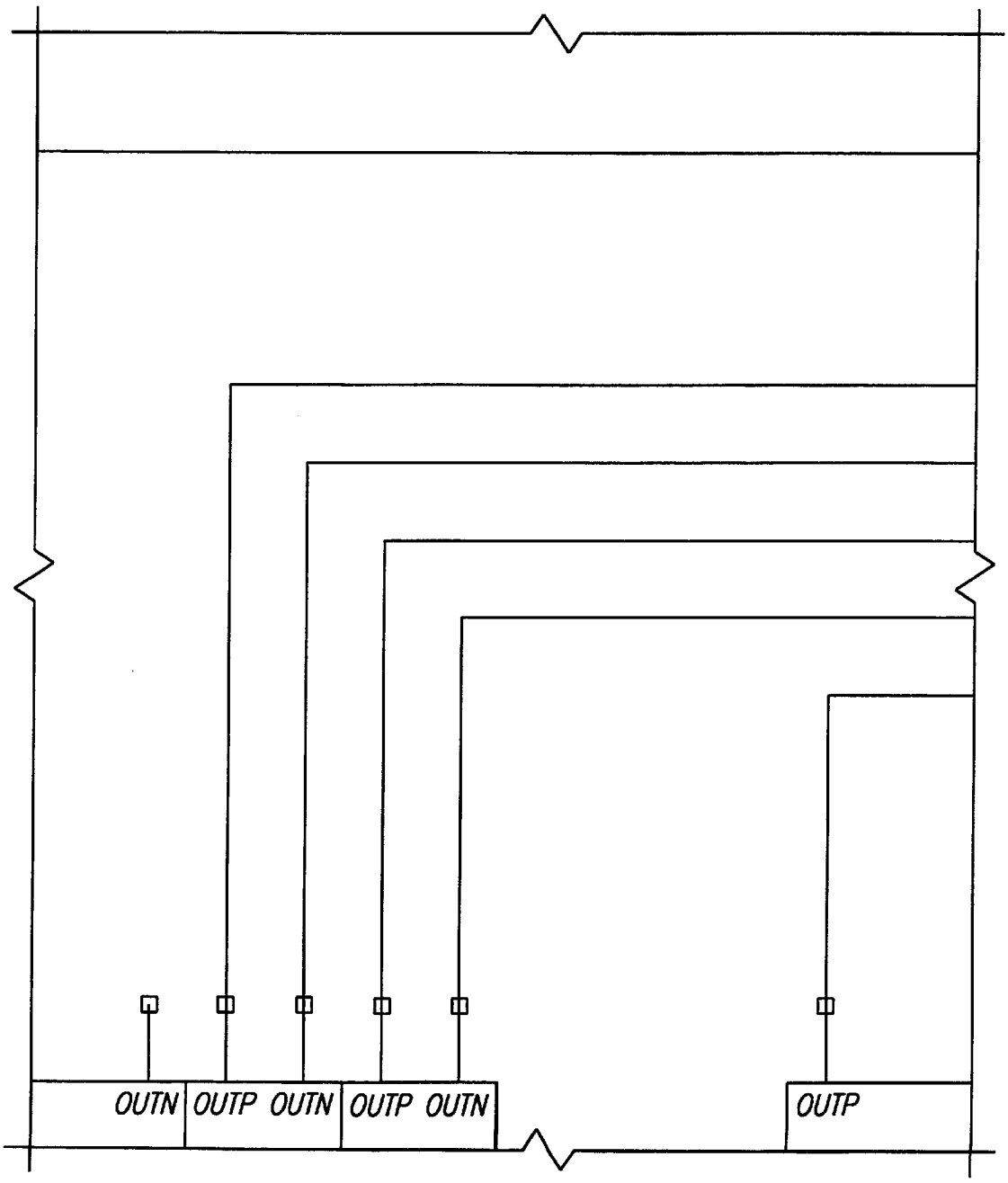


Fig 9.0103BK

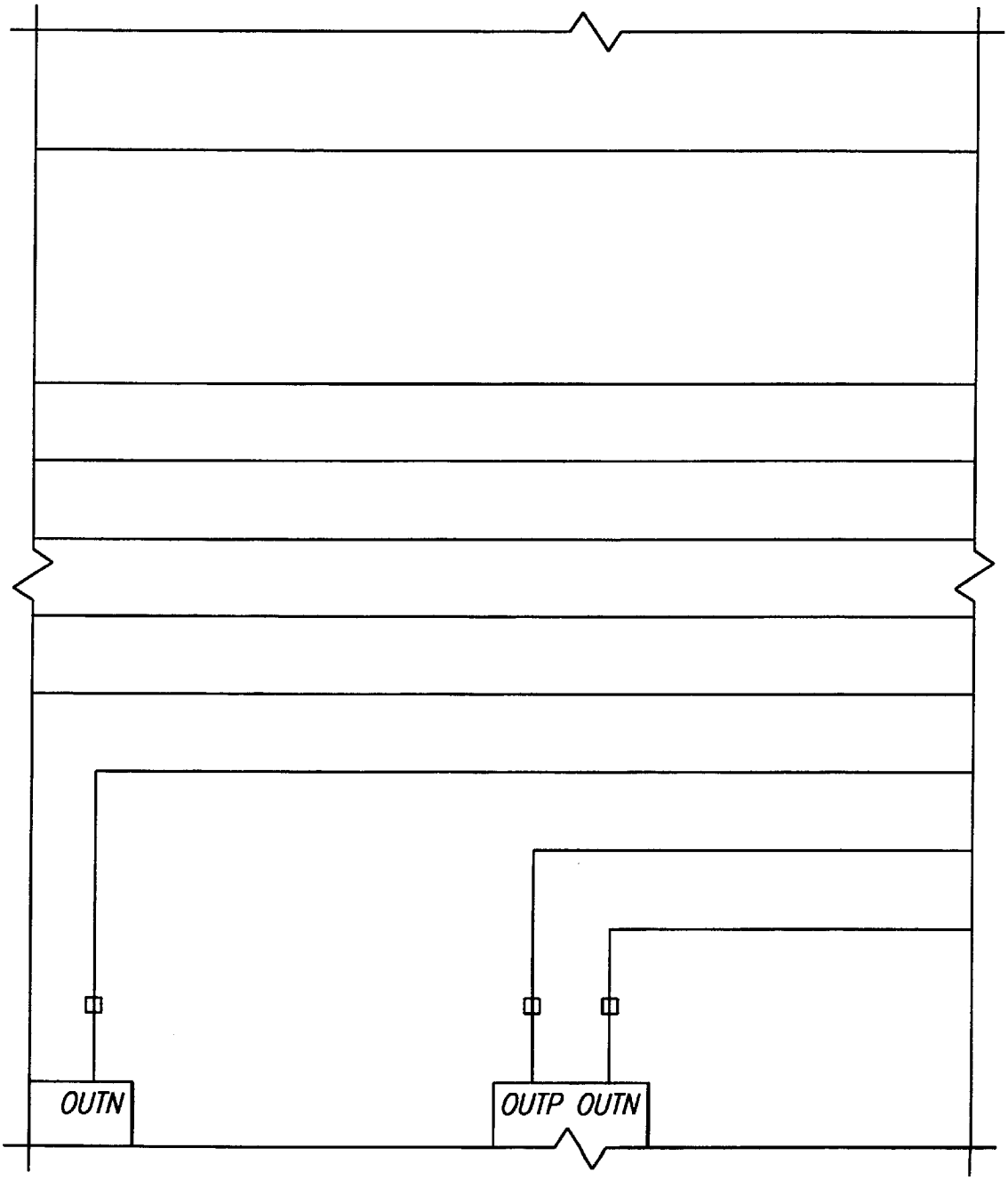


Fig 9.0103BL

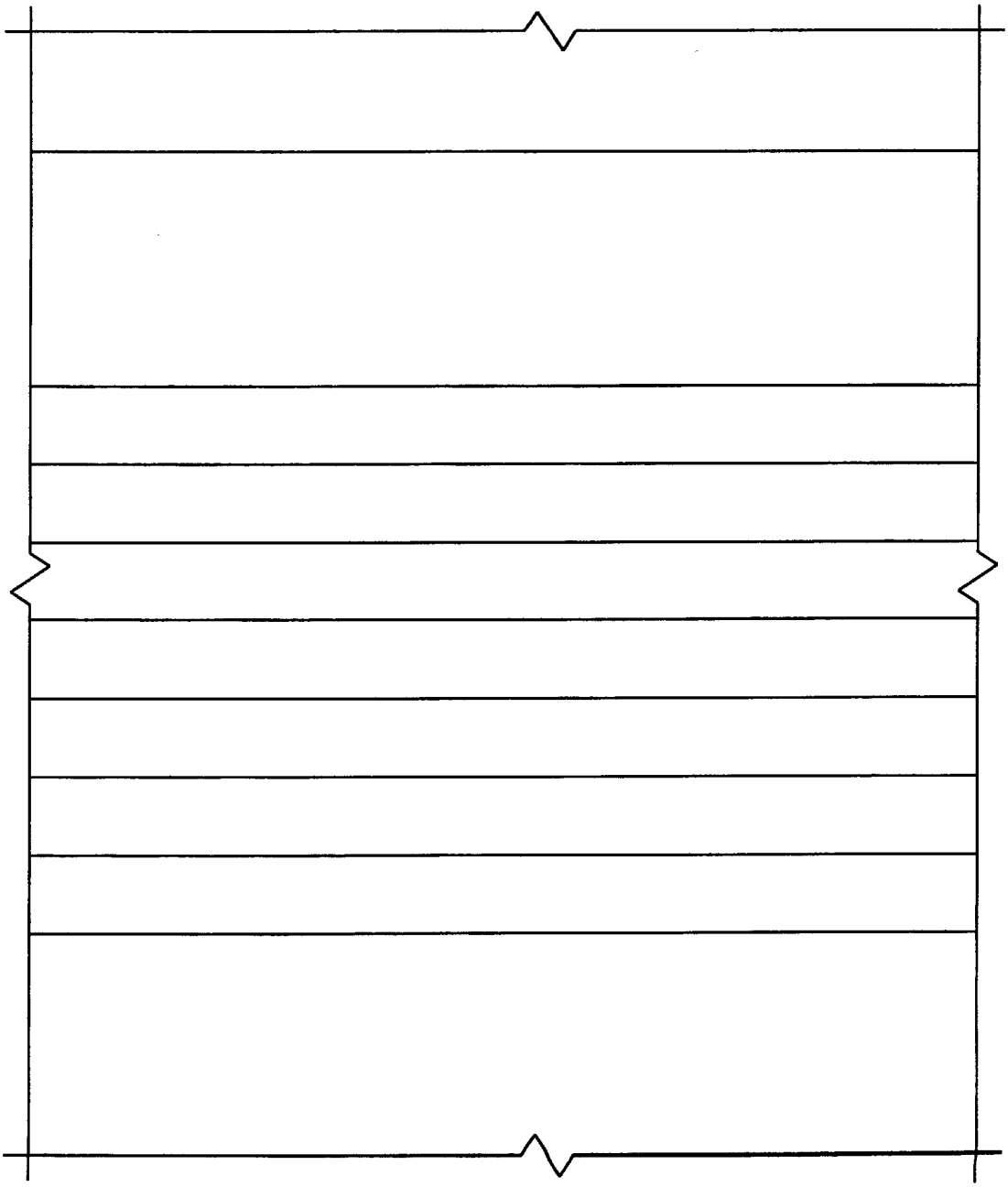


Fig 9.0103BM

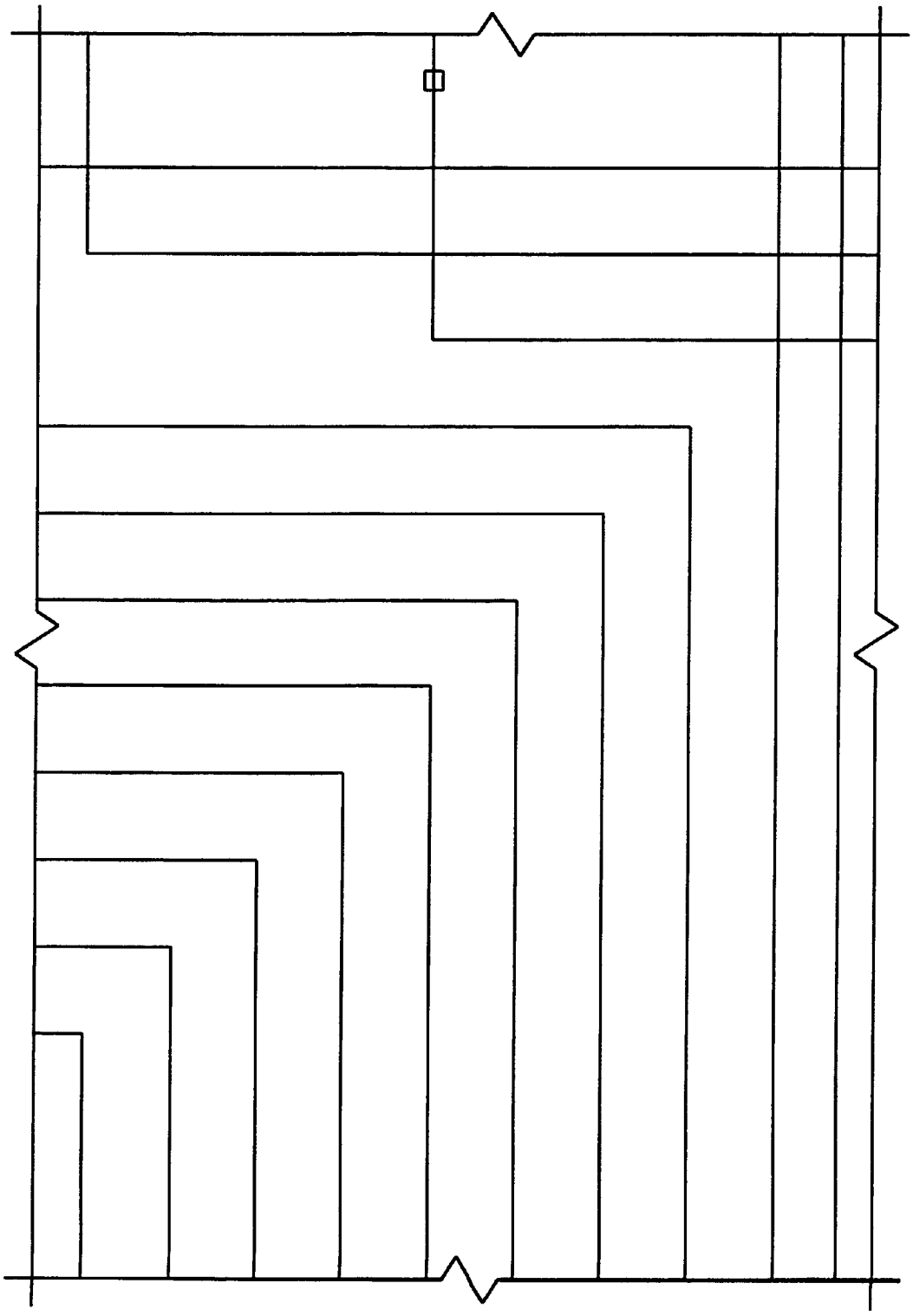


Fig 9.01038N

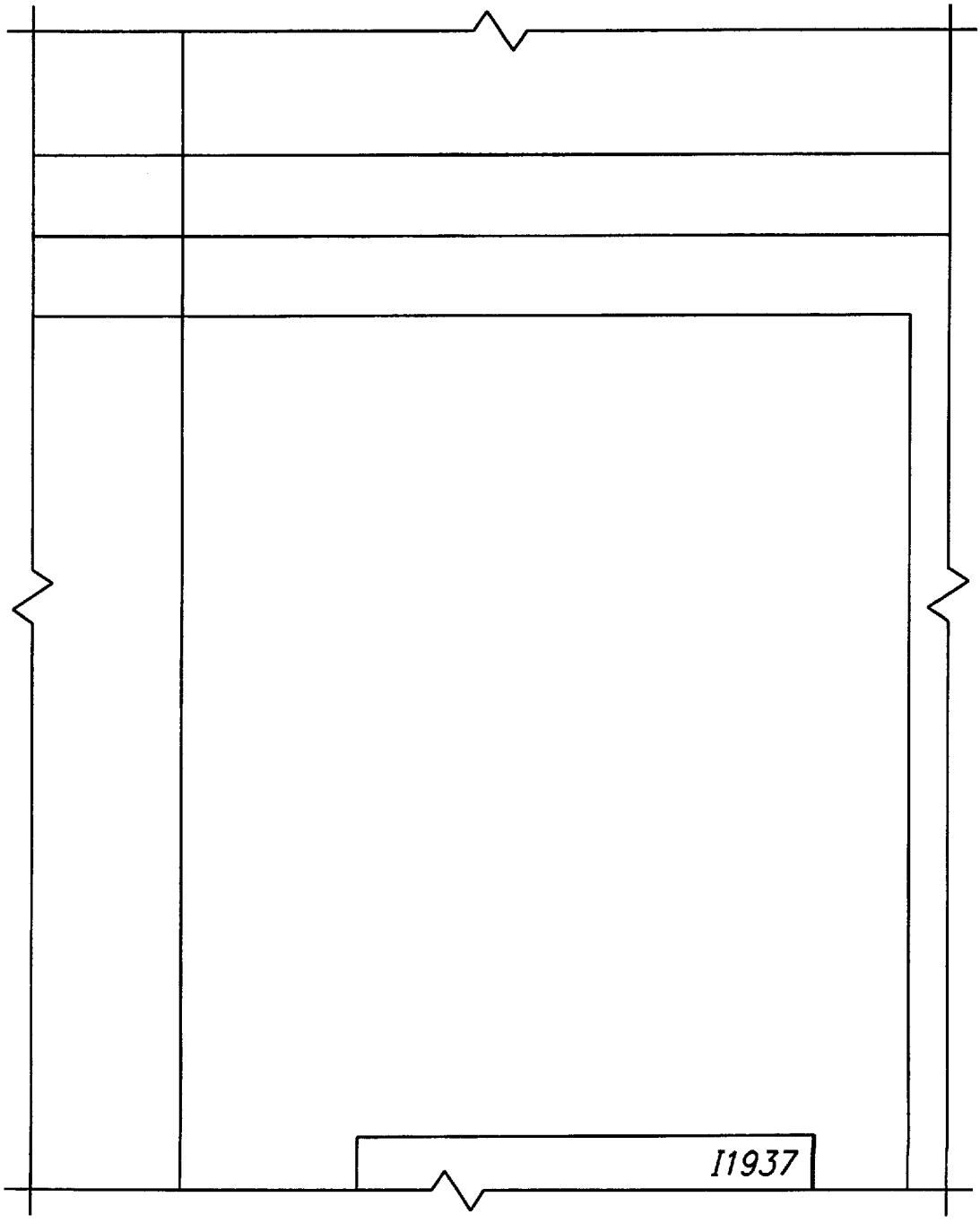


Fig 9.0103B0

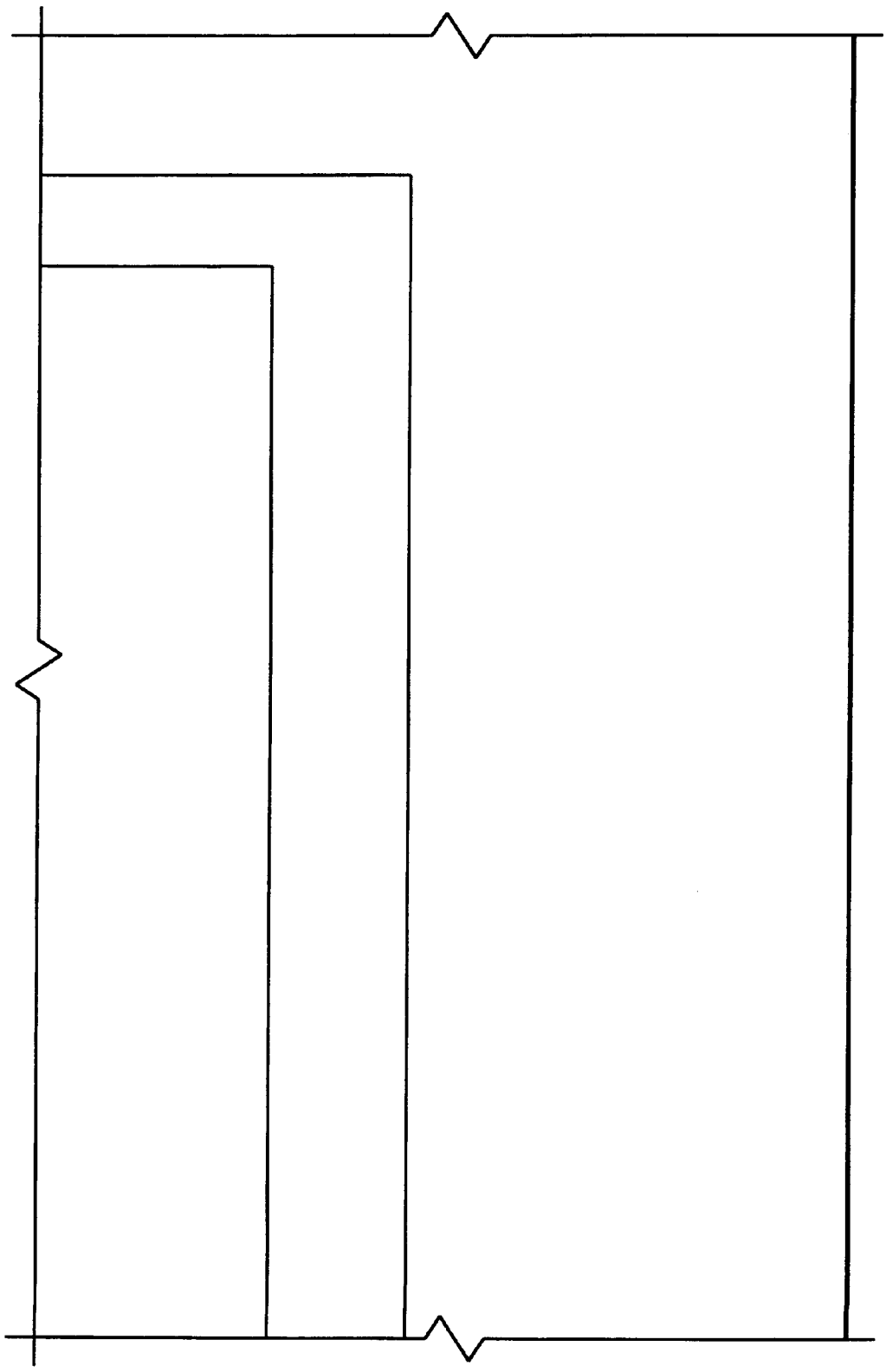


Fig 9.01037BP

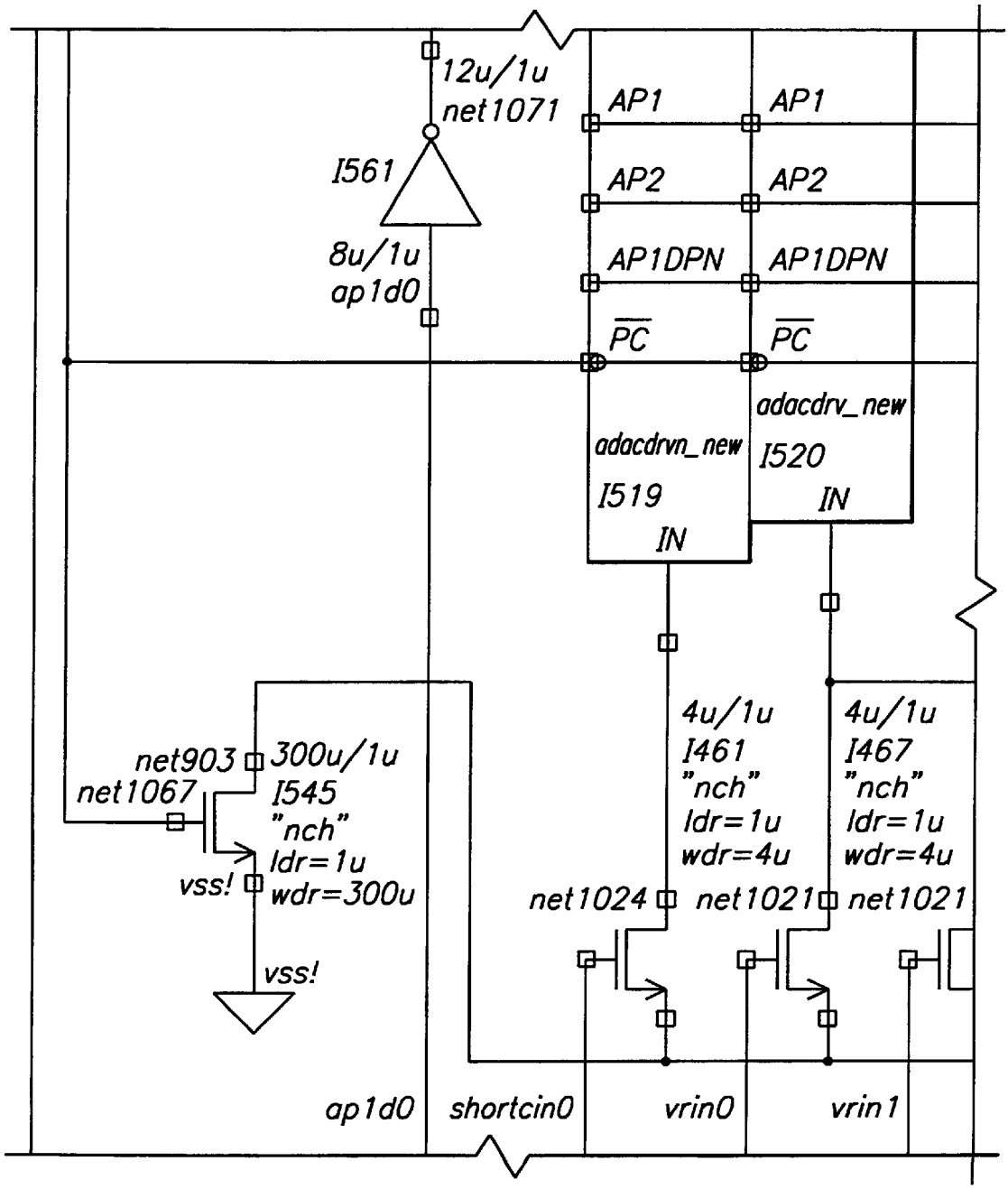

12u/1u
net1071
I561
8u/1u
ap1d0
AP1
AP2
AP1DPN
PC
adacdrvn_new
I519
IN
AP1
AP2
AP1DPN
PC
adacdrv_new
I520
IN
net903
net1067
300u/1u
I545
"nch"
ldr=1u
wdr=300u
vss!
vss!
4u/1u
I461
"nch"
ldr=1u
wdr=4u
net1024
4u/1u
I467
"nch"
ldr=1u
wdr=4u
net1021
net1021
ap1d0
shortcin0
vrin0
vrin1

Fig 9.0103A

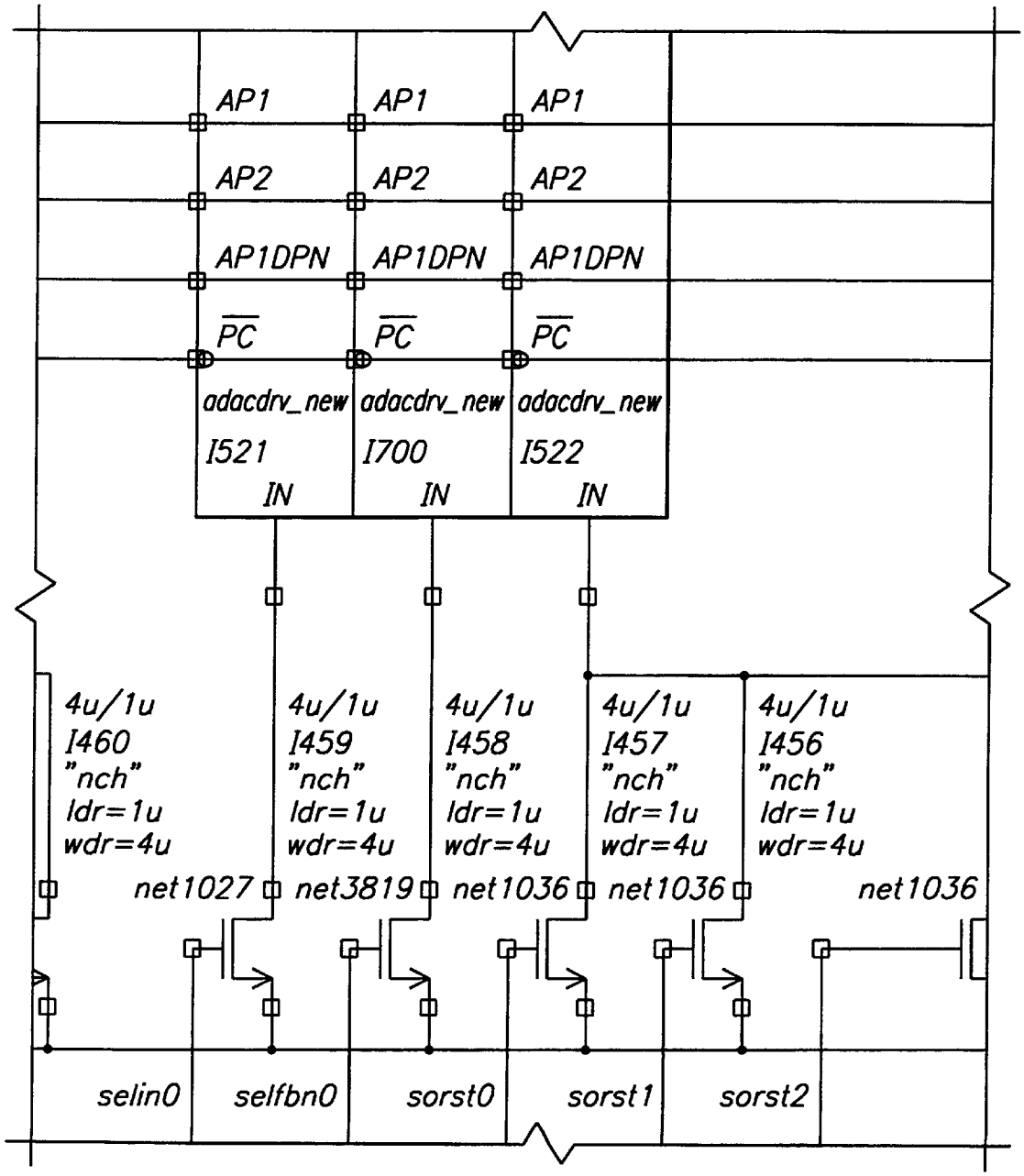

AP1
AP1
AP1
AP2
AP2
AP2
AP1DPN
AP1DPN
AP1DPN
PC
PC
PC
adacdrv_new
I521
IN
adacdrv_new
I700
IN
adacdrv_new
I522
IN
4u/1u
I460
"nch"
ldr=1u
wdr=4u
4u/1u
I459
"nch"
ldr=1u
wdr=4u
4u/1u
I458
"nch"
ldr=1u
wdr=4u
4u/1u
I457
"nch"
ldr=1u
wdr=4u
4u/1u
I456
"nch"
ldr=1u
wdr=4u
net1027
net3819
net1036
net1036
net1036
selin0
selfbn0
sorst0
sorst1
sorst2

Fig 9,010,3CB

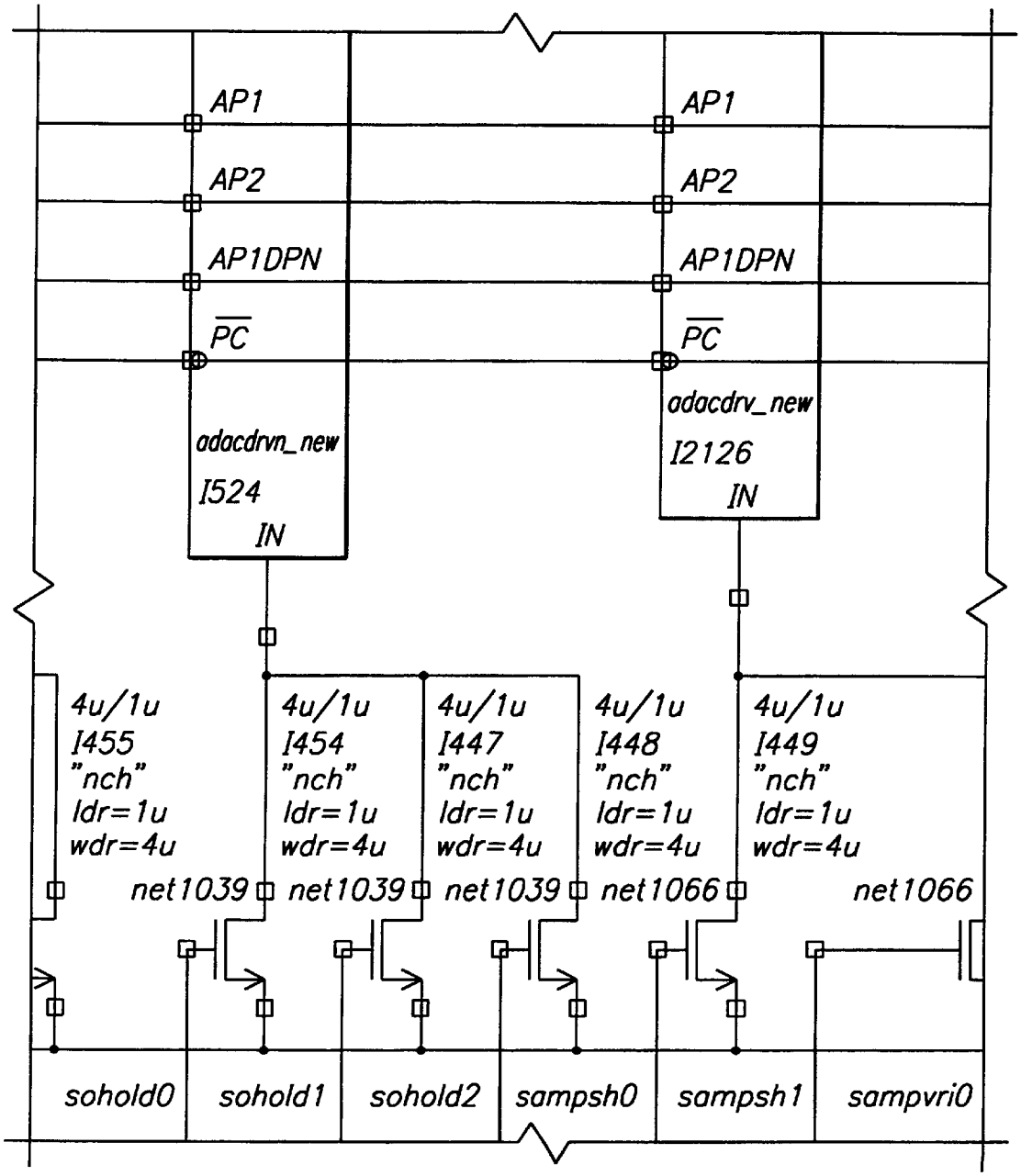

AP1
AP2
AP1DPN
PC
adacdrvn_new
I524
IN
AP1
AP2
AP1DPN
PC
adacdrv_new
I2126
IN
4u/1u
I455
"nch"
ldr=1u
wdr=4u
4u/1u
I454
"nch"
ldr=1u
wdr=4u
4u/1u
I447
"nch"
ldr=1u
wdr=4u
4u/1u
I448
"nch"
ldr=1u
wdr=4u
4u/1u
I449
"nch"
ldr=1u
wdr=4u
net1039
net1039
net1039
net1066
net1066
sohold0
sohold1
sohold2
sampsh0
sampsh1
sampvri0

Fig 9.0103CC

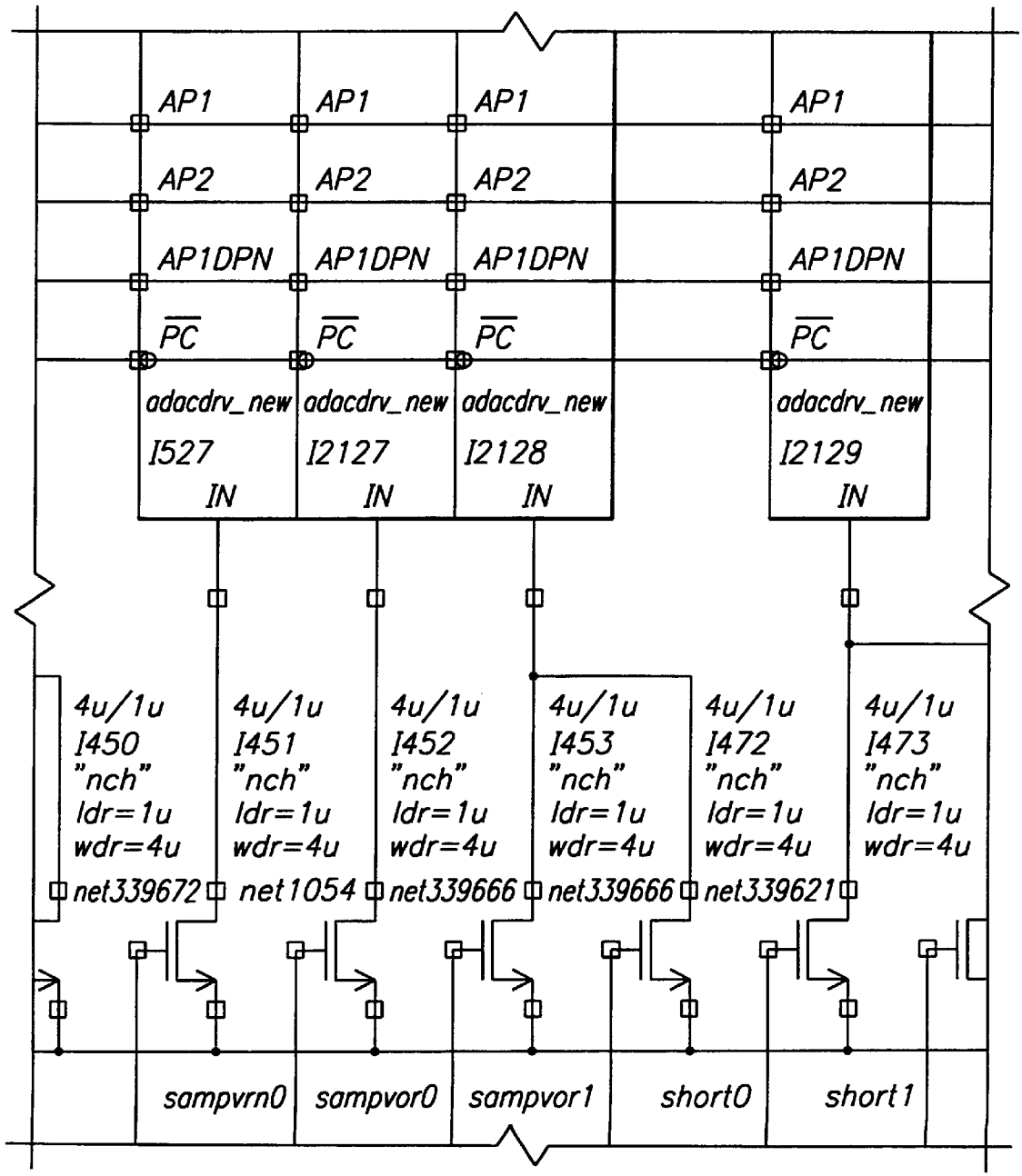

AP1
AP2
AP1DPN
PC
adacdrv_new
I527
IN
I2127
I2128
I2129
4u/1u
I450
"nch"
ldr=1u
wdr=4u
I451
I452
I453
I472
I473
net339672
net1054
net339666
net339621
sampvrn0
sampvor0
sampvor1
short0
short1

Fig 9.0130

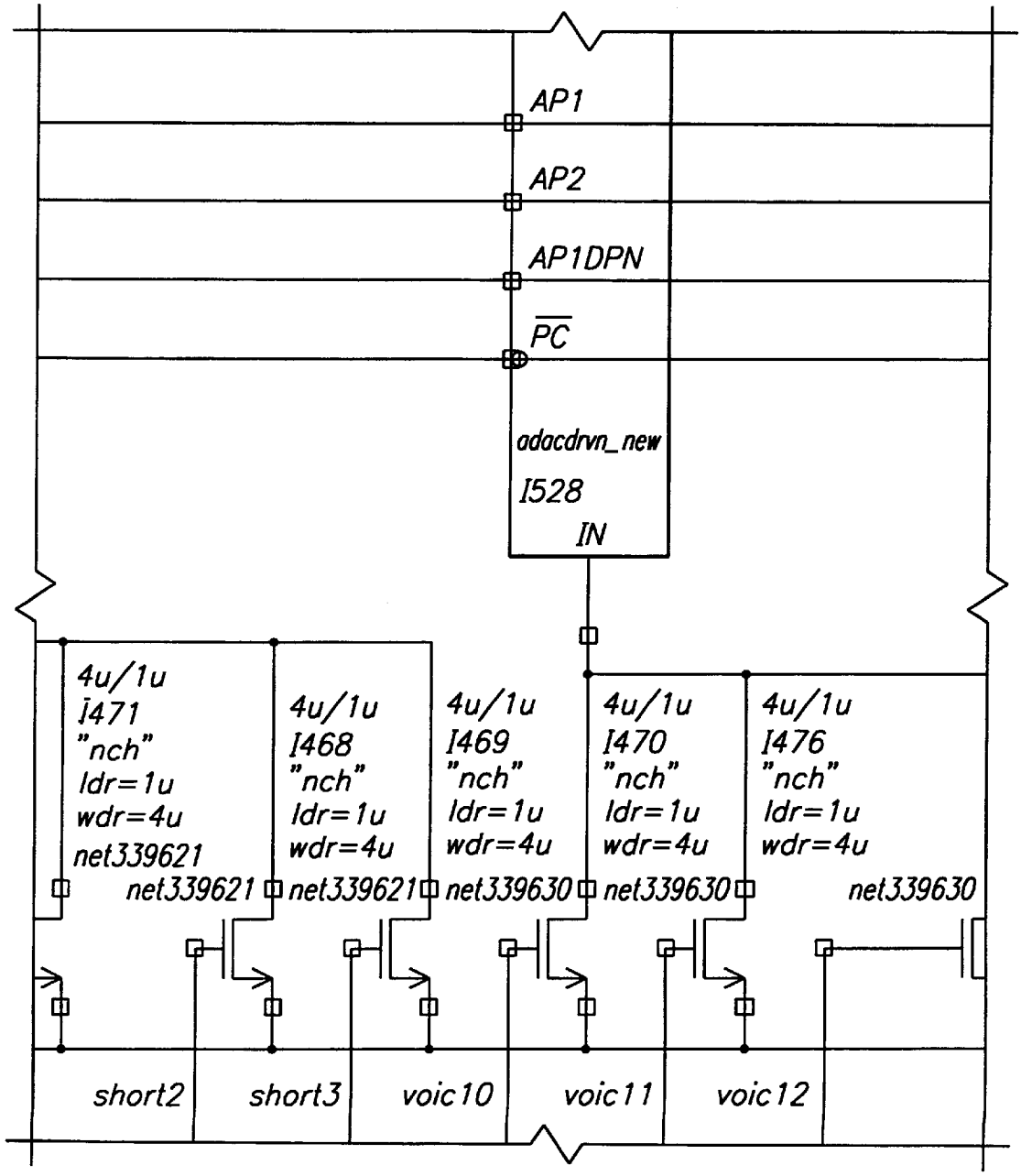

AP1
AP2
AP1DPN
PC
adacdrvn_new
I528
IN
4u/1u
I471
"nch"
ldr=1u
wdr=4u
net339621
4u/1u
I468
"nch"
ldr=1u
wdr=4u
4u/1u
I469
"nch"
ldr=1u
wdr=4u
4u/1u
I470
"nch"
ldr=1u
wdr=4u
4u/1u
I476
"nch"
ldr=1u
wdr=4u
net339621
net339621
net339630
net339630
net339630
short2
short3
voic10
voic11
voic12

Fig 9.0103E

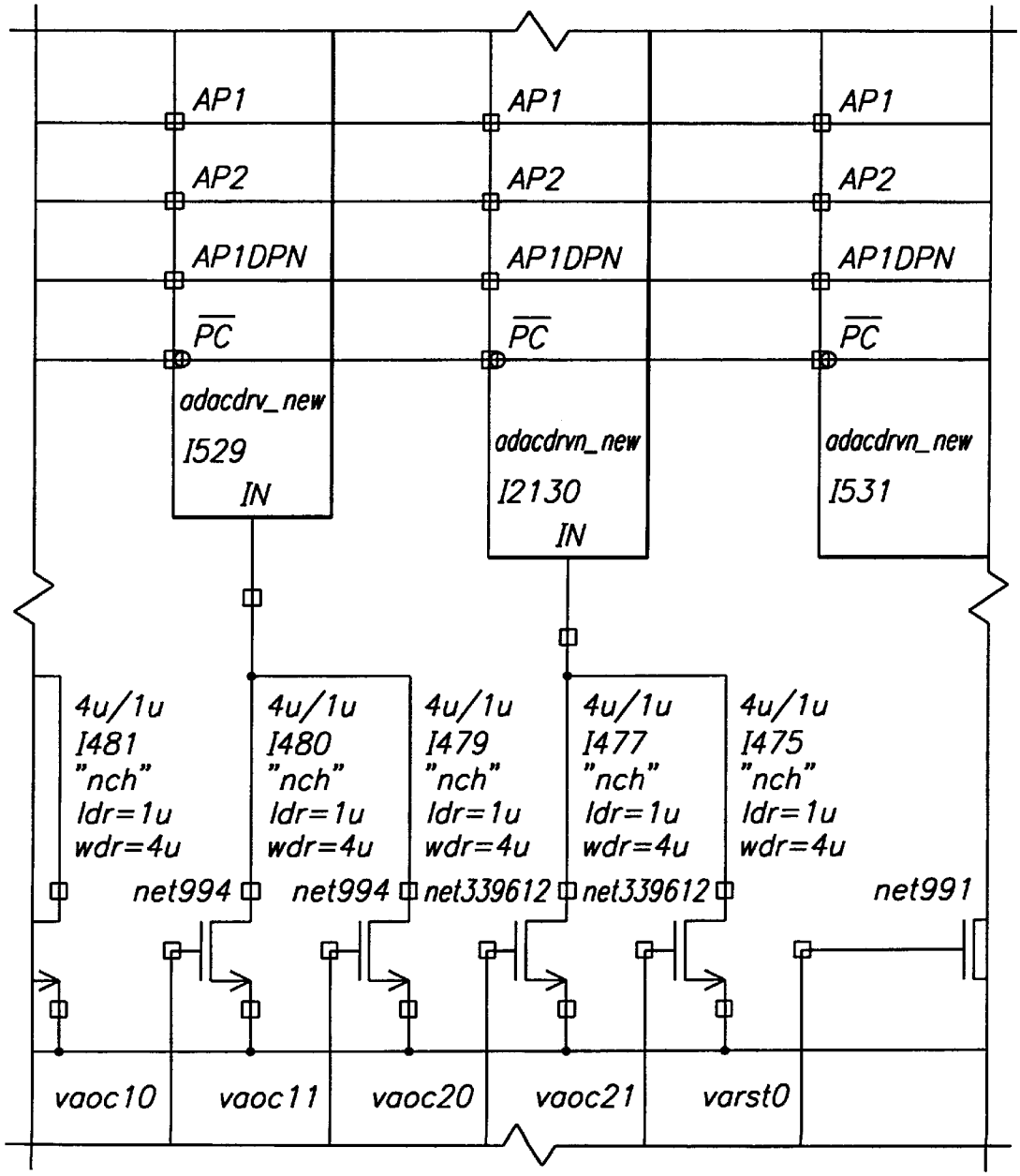

AP1
AP2
AP1DPN
PC
adacdrv_new
I529
IN
AP1
AP2
AP1DPN
PC
adacdrvn_new
I2130
IN
AP1
AP2
AP1DPN
PC
adacdrvn_new
I531
4u/1u
I481
"nch"
ldr=1u
wdr=4u
4u/1u
I480
"nch"
ldr=1u
wdr=4u
4u/1u
I479
"nch"
ldr=1u
wdr=4u
4u/1u
I477
"nch"
ldr=1u
wdr=4u
4u/1u
I475
"nch"
ldr=1u
wdr=4u
net994
net994
net339612
net339612
net991
vaoc10
vaoc11
vaoc20
vaoc21
varst0

Fig 9.0103F

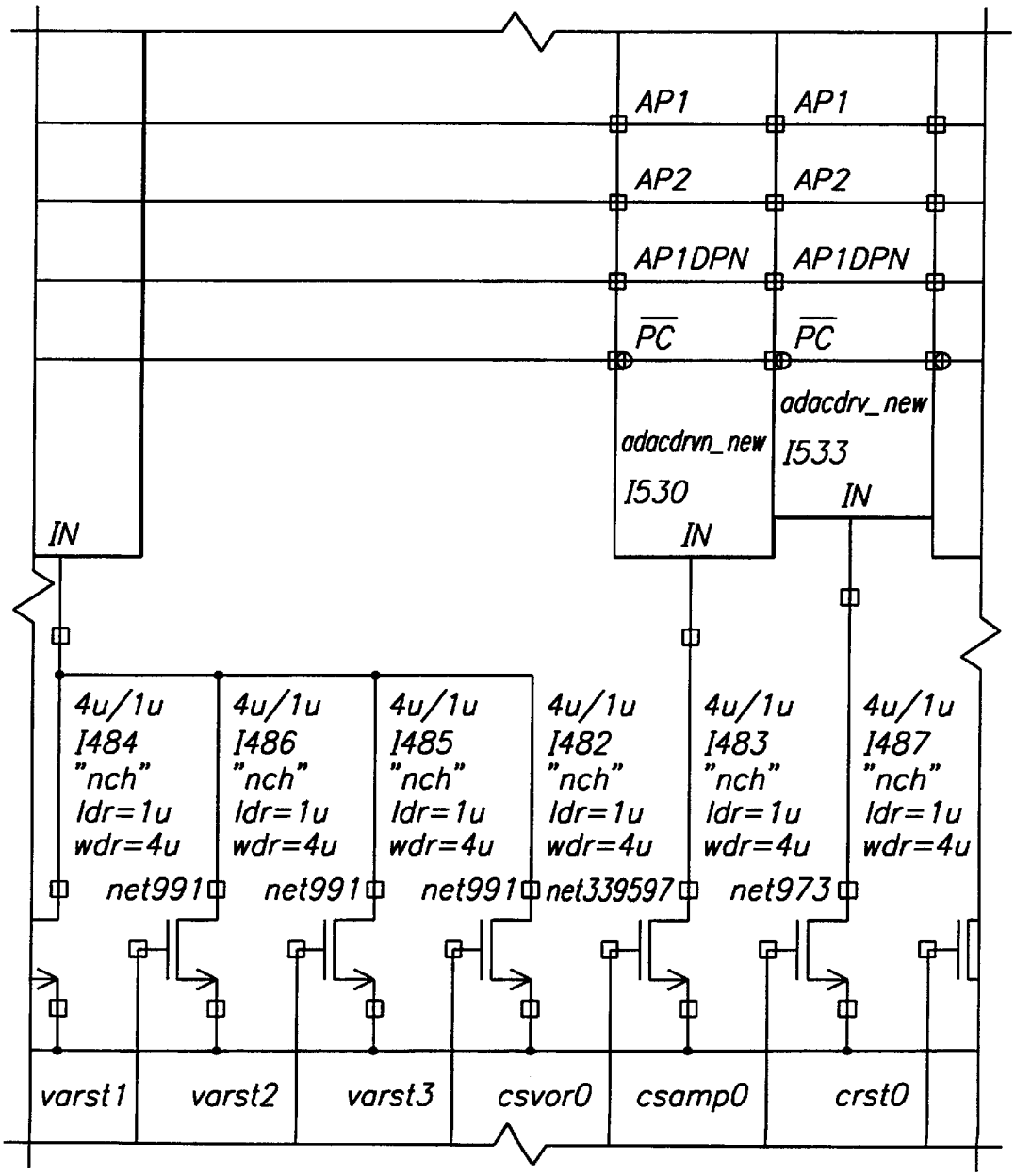

AP1
AP1
AP2
AP2
AP1DPN
AP1DPN
PC
PC
adacdrv_new
adacdrvn_new
I533
I530
IN
IN
IN
4u/1u
I484
"nch"
ldr=1u
wdr=4u
4u/1u
I486
"nch"
ldr=1u
wdr=4u
4u/1u
I485
"nch"
ldr=1u
wdr=4u
4u/1u
I482
"nch"
ldr=1u
wdr=4u
4u/1u
I483
"nch"
ldr=1u
wdr=4u
4u/1u
I487
"nch"
ldr=1u
wdr=4u
net991
net991
net991
net339597
net973
varst1
varst2
varst3
csvor0
csamp0
crst0

Fig 9.00306

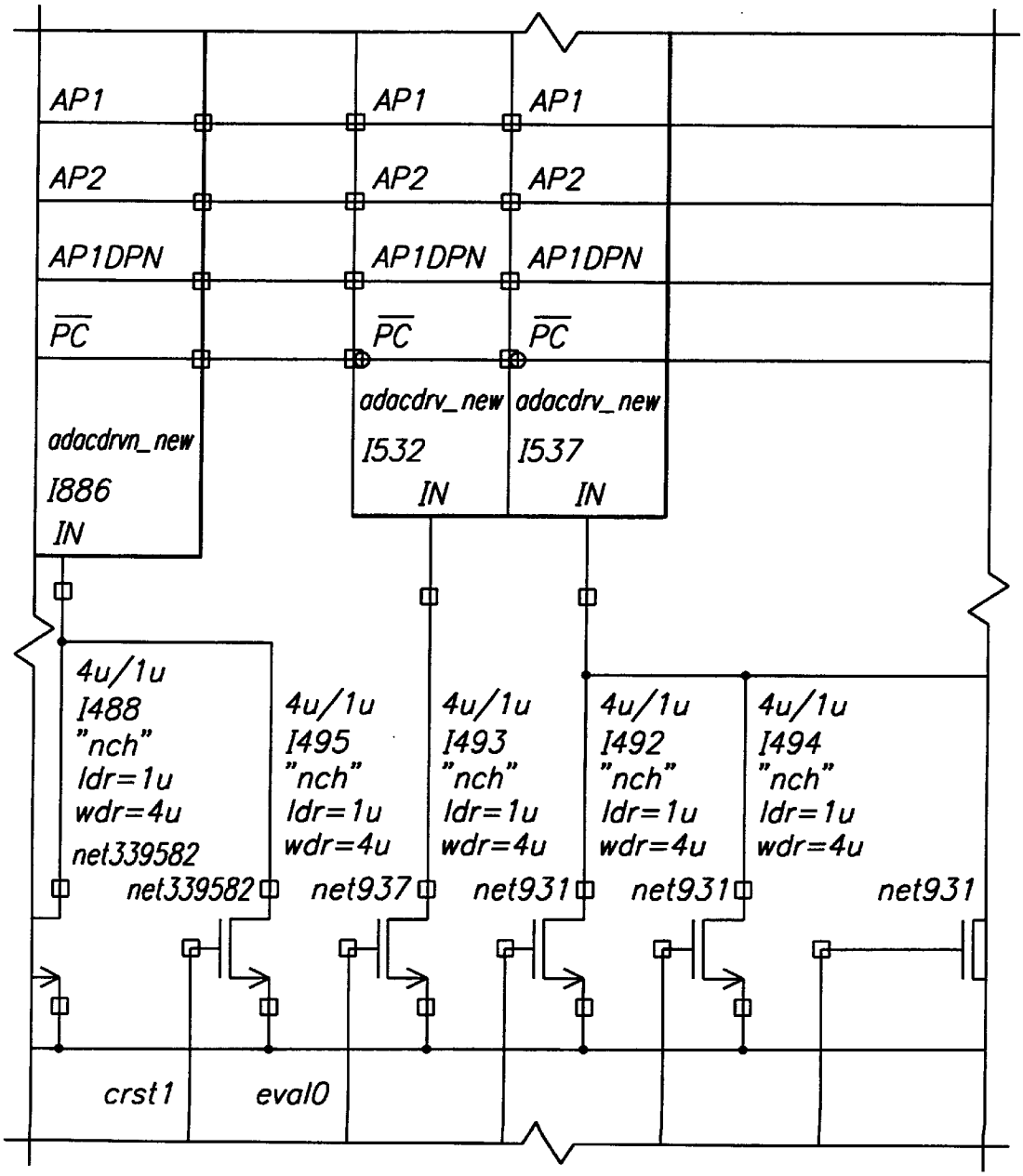

AP1
AP2
AP1DPN
PC
adacdrvn_new
I886
IN
AP1
AP2
AP1DPN
PC
adacdrv_new
I532
IN
AP1
AP2
AP1DPN
PC
adacdrv_new
I537
IN
4u/1u
I488
"nch"
ldr=1u
wdr=4u
net339582
net339582
4u/1u
I495
"nch"
ldr=1u
wdr=4u
net937
4u/1u
I493
"nch"
ldr=1u
wdr=4u
net931
4u/1u
I492
"nch"
ldr=1u
wdr=4u
net931
4u/1u
I494
"nch"
ldr=1u
wdr=4u
net931
crst1
eval0

Fig 9.0130CH

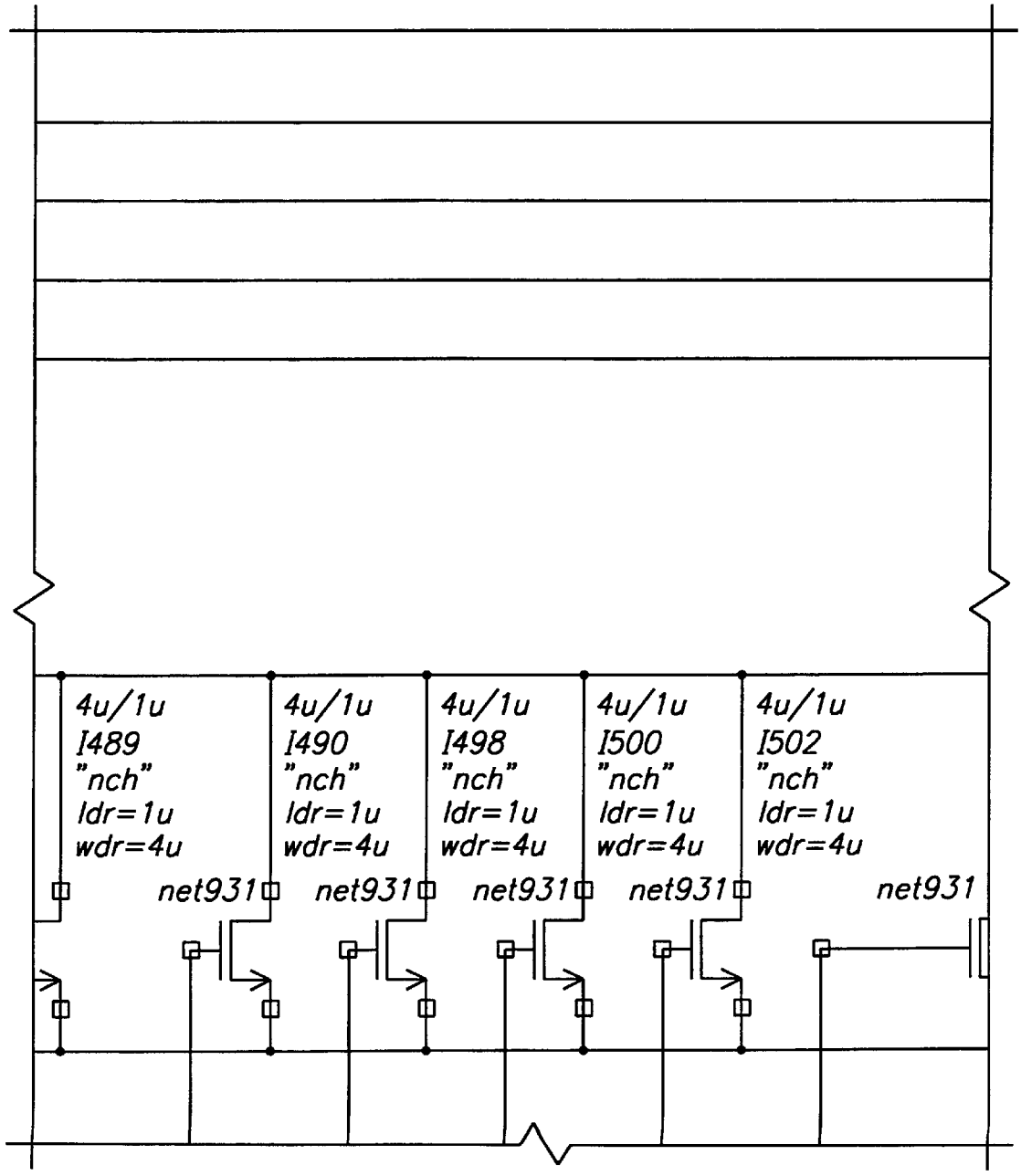


FIG 9.0100E II

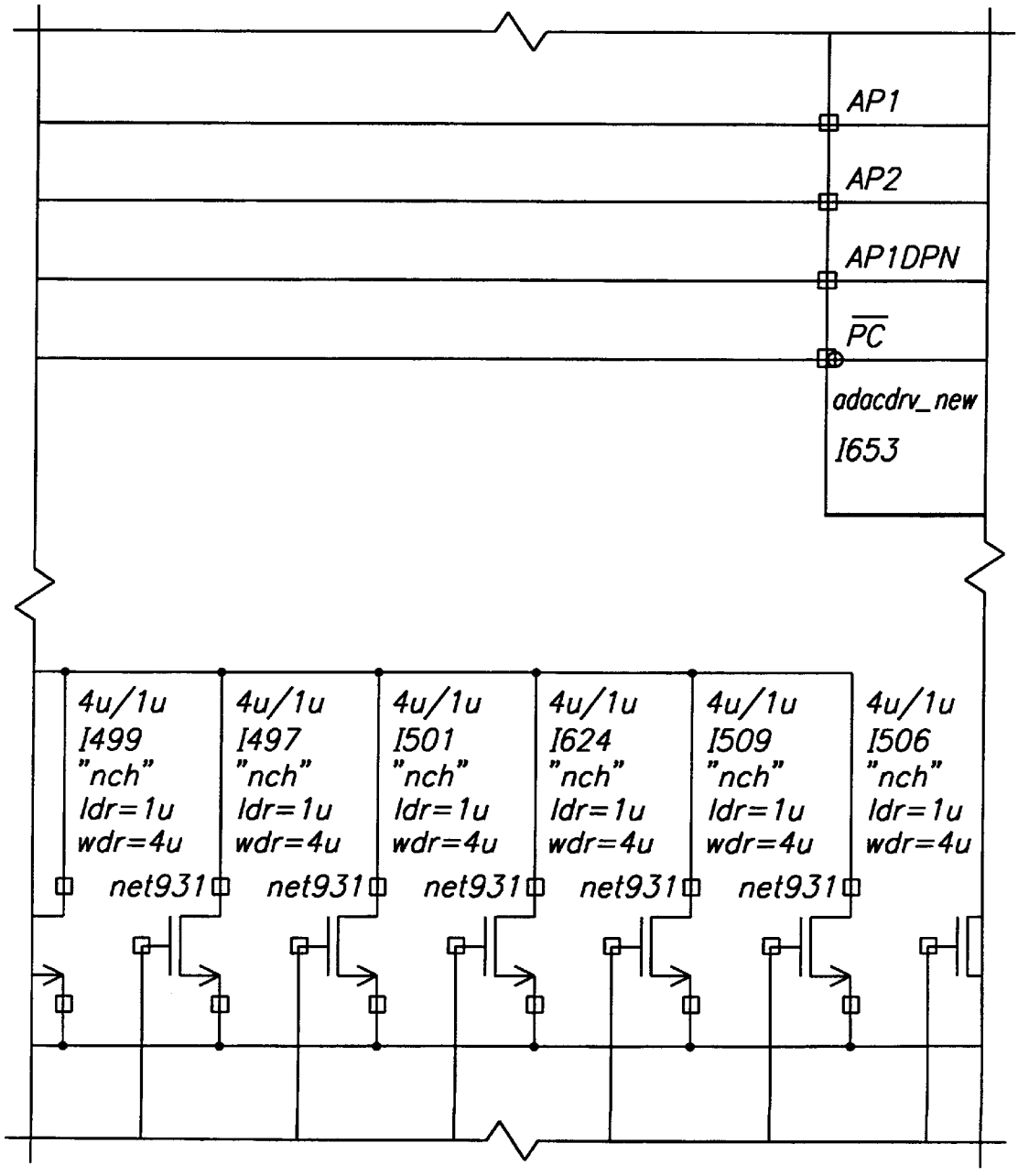

AP1
AP2
AP1DPN
PC
adacdrv_new
I653
4u/1u
I499
"nch"
ldr=1u
wdr=4u
net931
4u/1u
I497
"nch"
ldr=1u
wdr=4u
net931
4u/1u
I501
"nch"
ldr=1u
wdr=4u
net931
4u/1u
I624
"nch"
ldr=1u
wdr=4u
net931
4u/1u
I509
"nch"
ldr=1u
wdr=4u
net931
4u/1u
I506
"nch"
ldr=1u
wdr=4u

Fig 9.01036J

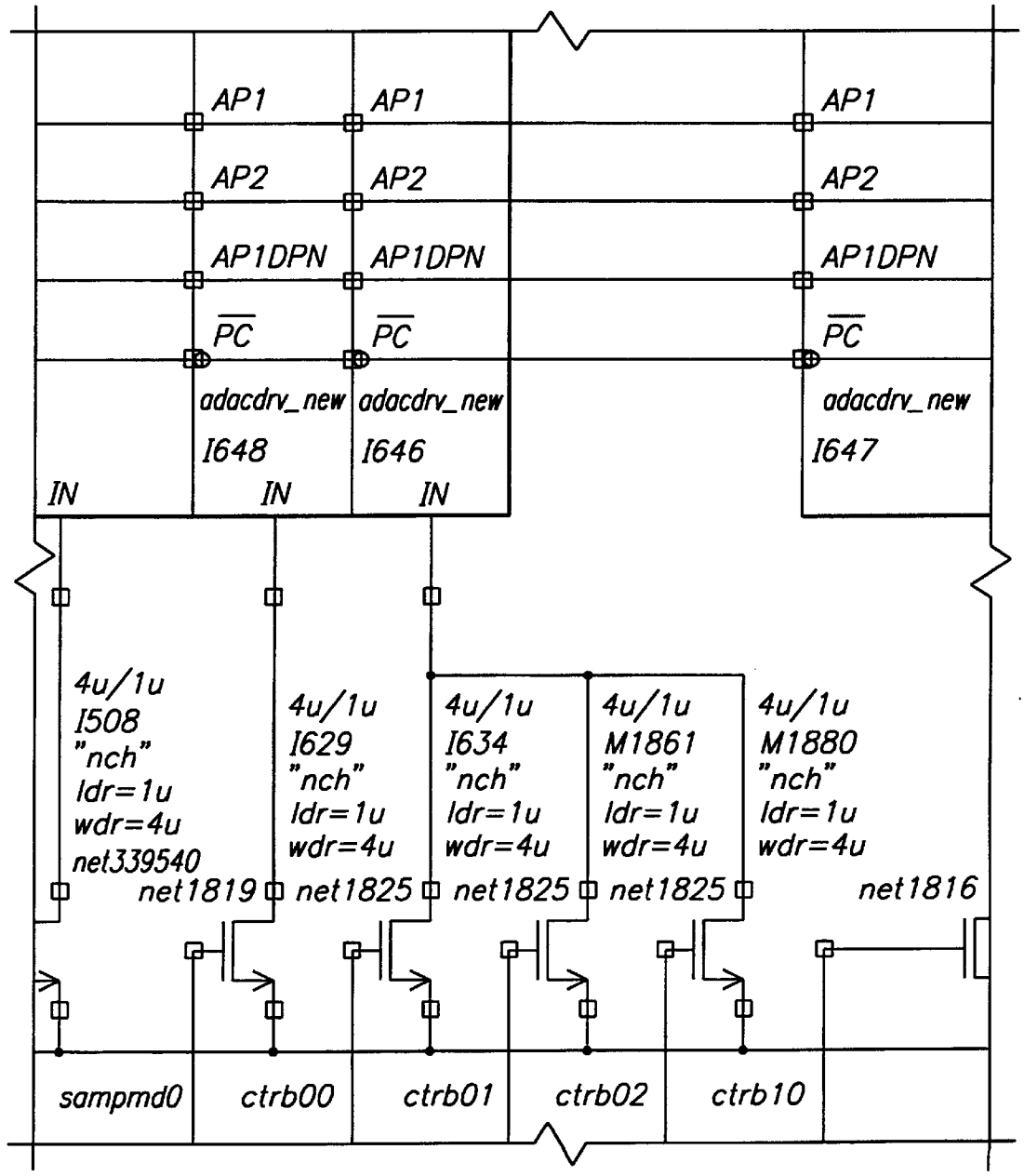

AP1
AP1
AP1
AP2
AP2
AP2
AP1DPN
AP1DPN
AP1DPN
PC
PC
PC
adacdrv_new
I648
adacdrv_new
I646
adacdrv_new
I647
IN
IN
IN
4u/1u
I508
"nch"
ldr=1u
wdr=4u
net339540
4u/1u
I629
"nch"
ldr=1u
wdr=4u
4u/1u
I634
"nch"
ldr=1u
wdr=4u
4u/1u
M1861
"nch"
ldr=1u
wdr=4u
4u/1u
M1880
"nch"
ldr=1u
wdr=4u
net1819
net1825
net1825
net1825
net1816
sampmd0
ctrb00
ctrb01
ctrb02
ctrb10

Fig 9.0.1.0.3.0.K

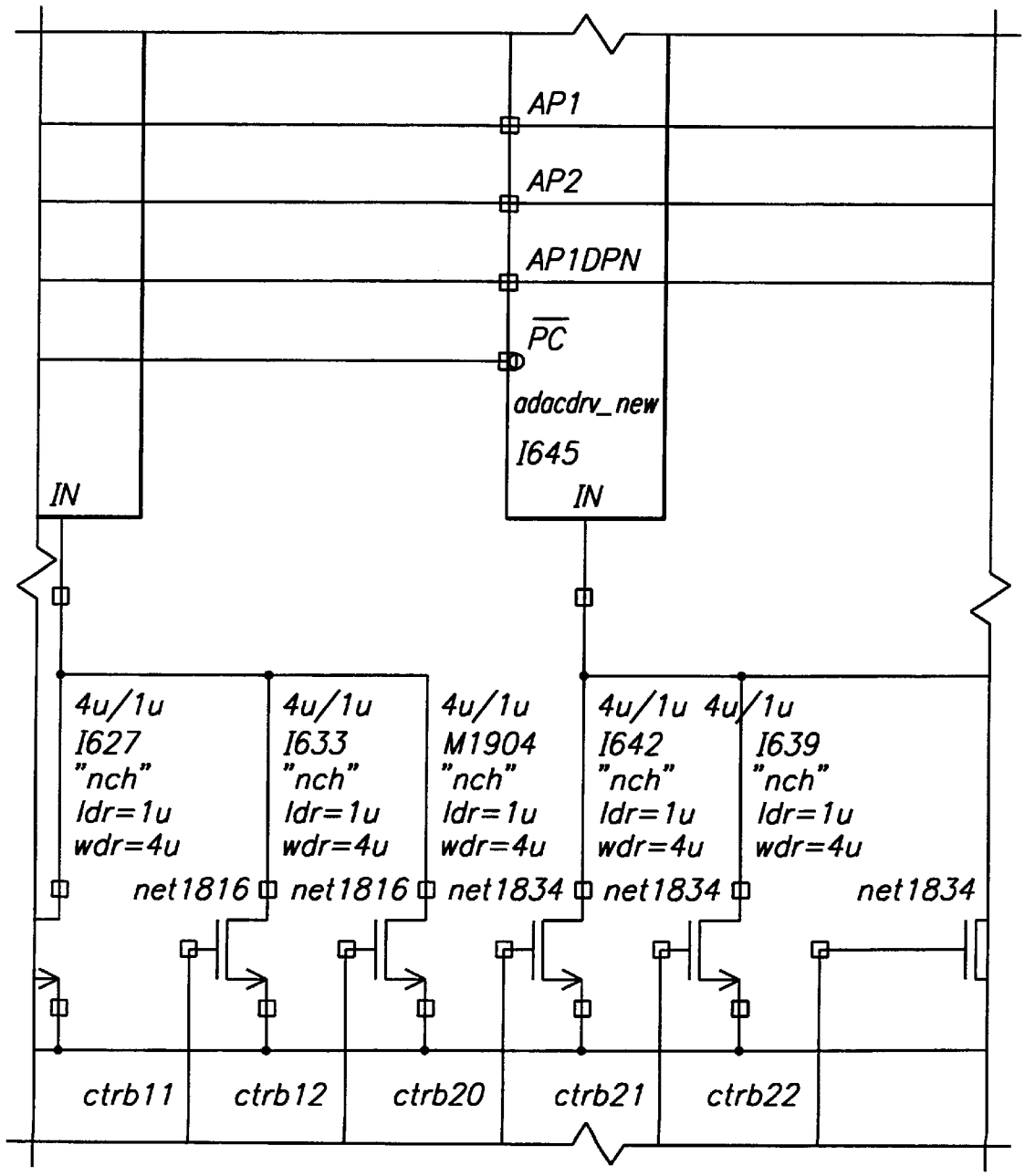

AP1
AP2
AP1DPN
PC
adacdrv_new
I645
IN
IN
4u/1u
I627
"nch"
ldr=1u
wdr=4u
4u/1u
I633
"nch"
ldr=1u
wdr=4u
4u/1u
M1904
"nch"
ldr=1u
wdr=4u
4u/1u
I642
"nch"
ldr=1u
wdr=4u
4u/1u
I639
"nch"
ldr=1u
wdr=4u
net1816
net1816
net1834
net1834
net1834
ctrb11
ctrb12
ctrb20
ctrb21
ctrb22

Fig 9.0103CL

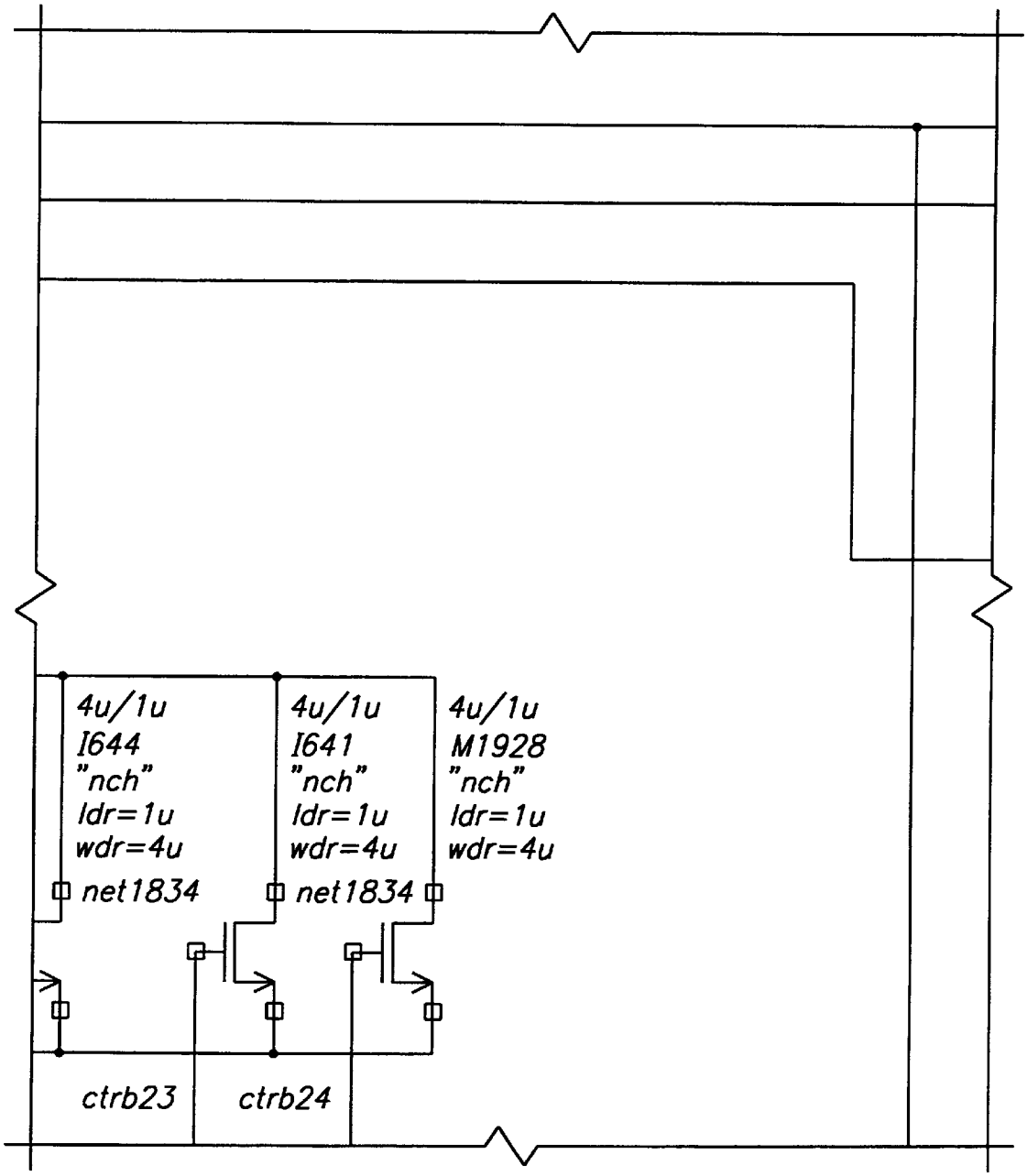

4u/1u
I644
"nch"
ldr=1u
wdr=4u
net1834
4u/1u
I641
"nch"
ldr=1u
wdr=4u
net1834
4u/1u
M1928
"nch"
ldr=1u
wdr=4u
ctrb23
ctrb24

Fig 9.0130CM

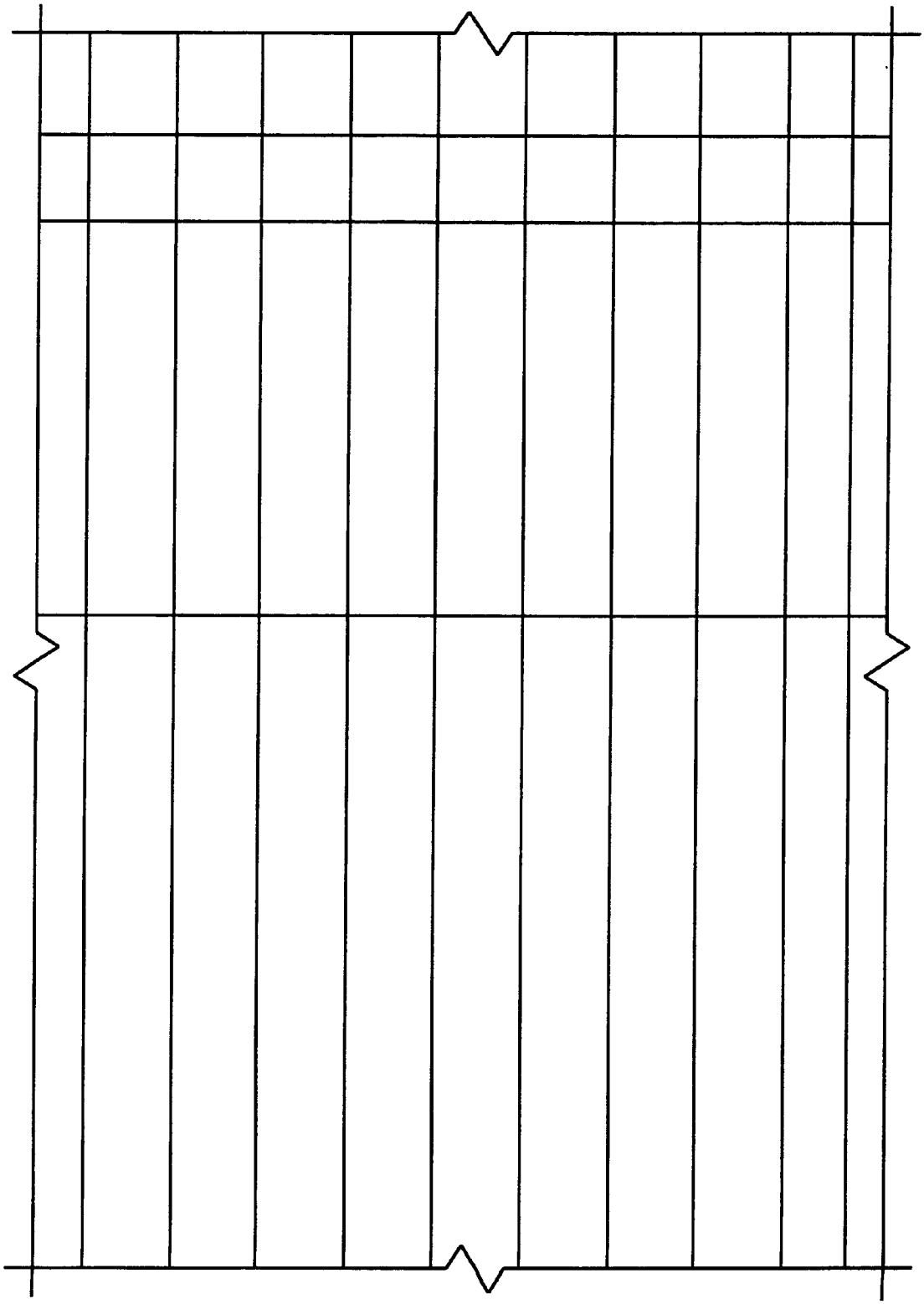


Fig 9.0103CN

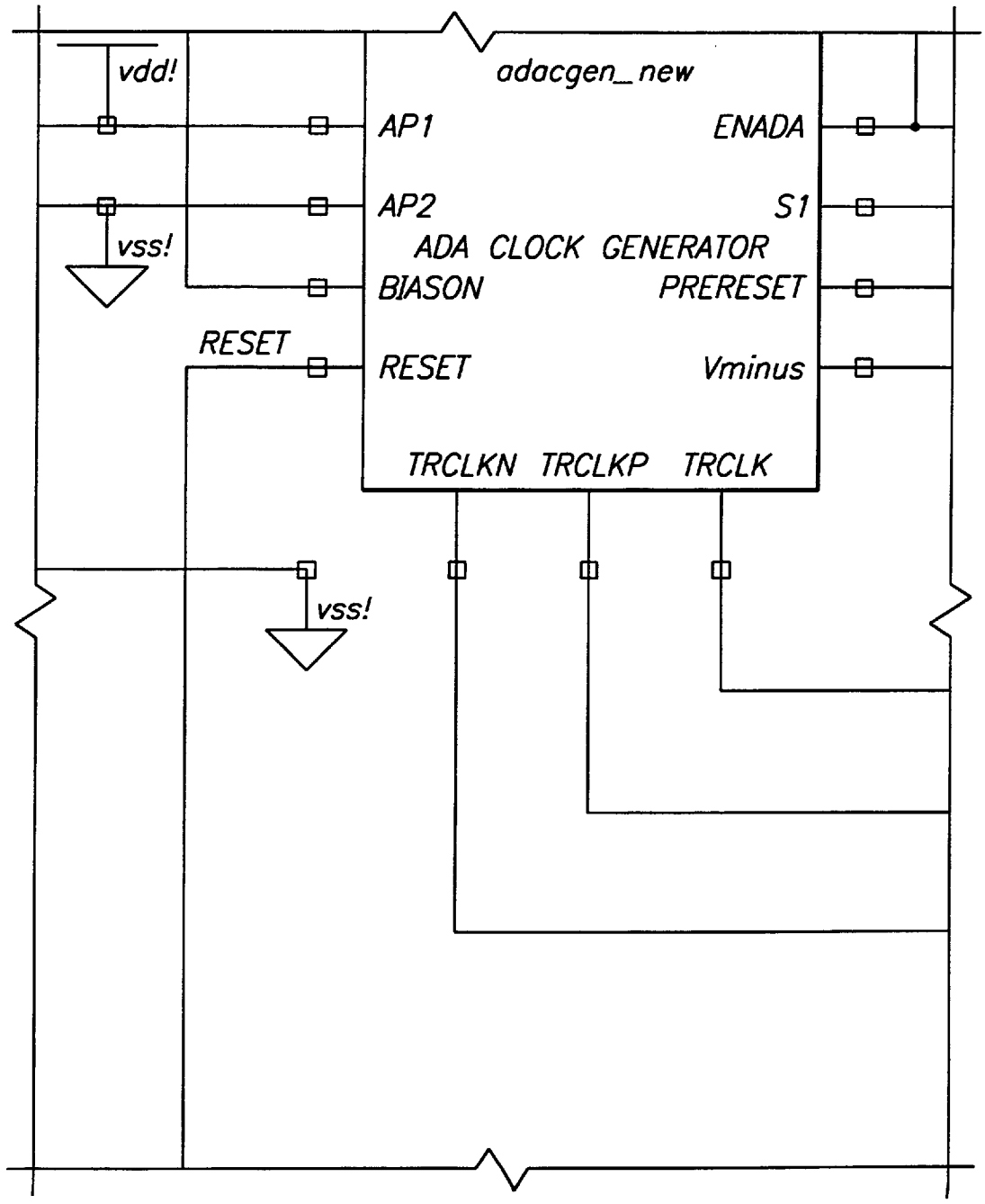

vdd!
adacgen_new
AP1
ENADA
AP2
S1
vss!
ADA CLOCK GENERATOR
BIASON
PRERESET
RESET
RESET
Vminus
TRCLKN TRCLKP TRCLK
vss!

Fig 9.0103C0

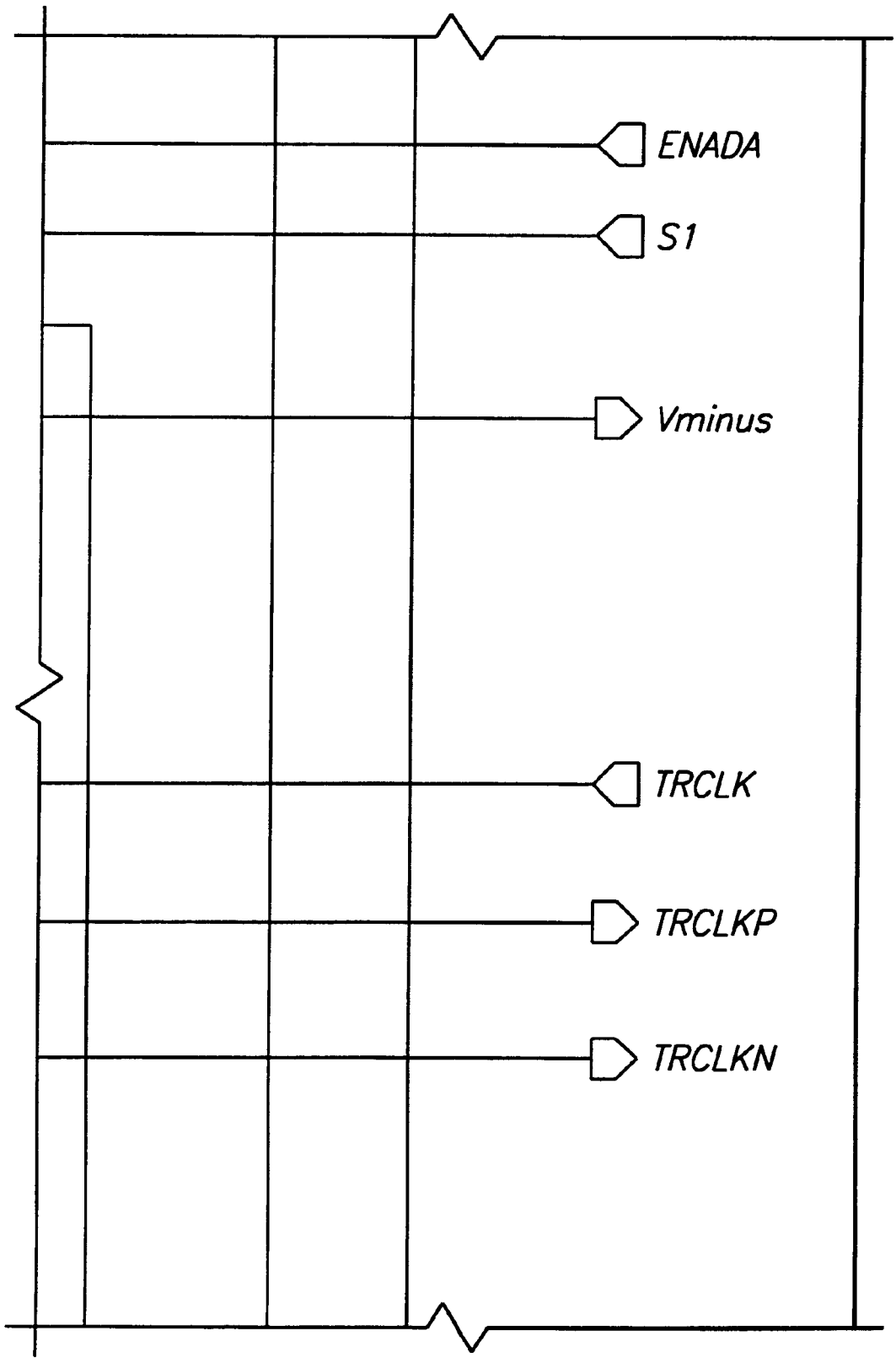


Fig 9.0103CP

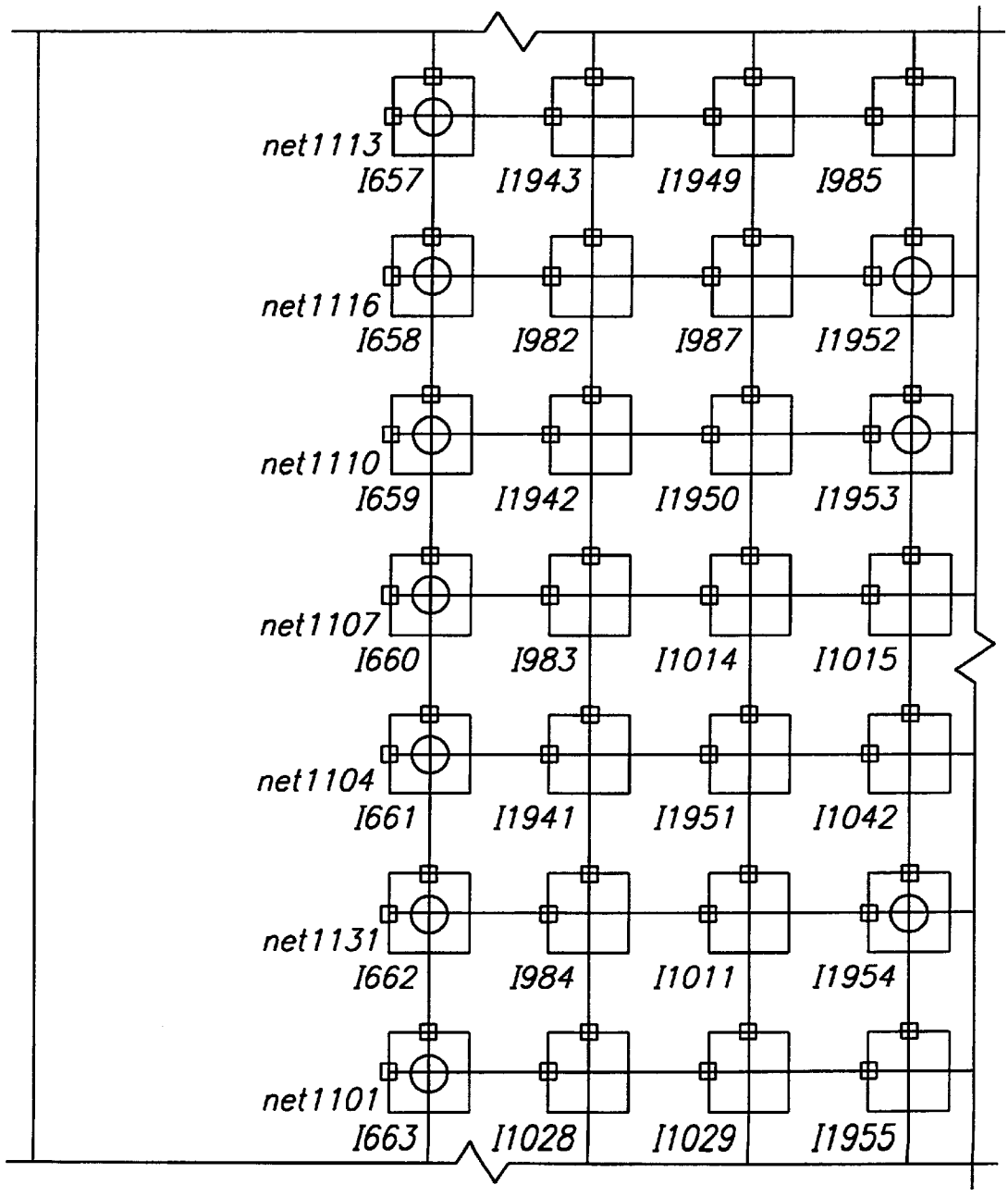

net1113
I657
I1943
I1949
I985
net1116
I658
I982
I987
I1952
net1110
I659
I1942
I1950
I1953
net1107
I660
I983
I1014
I1015
net1104
I661
I1941
I1951
I1042
net1131
I662
I984
I1011
I1954
net1101
I663
I1028
I1029
I1955

Fig 9.0113DA

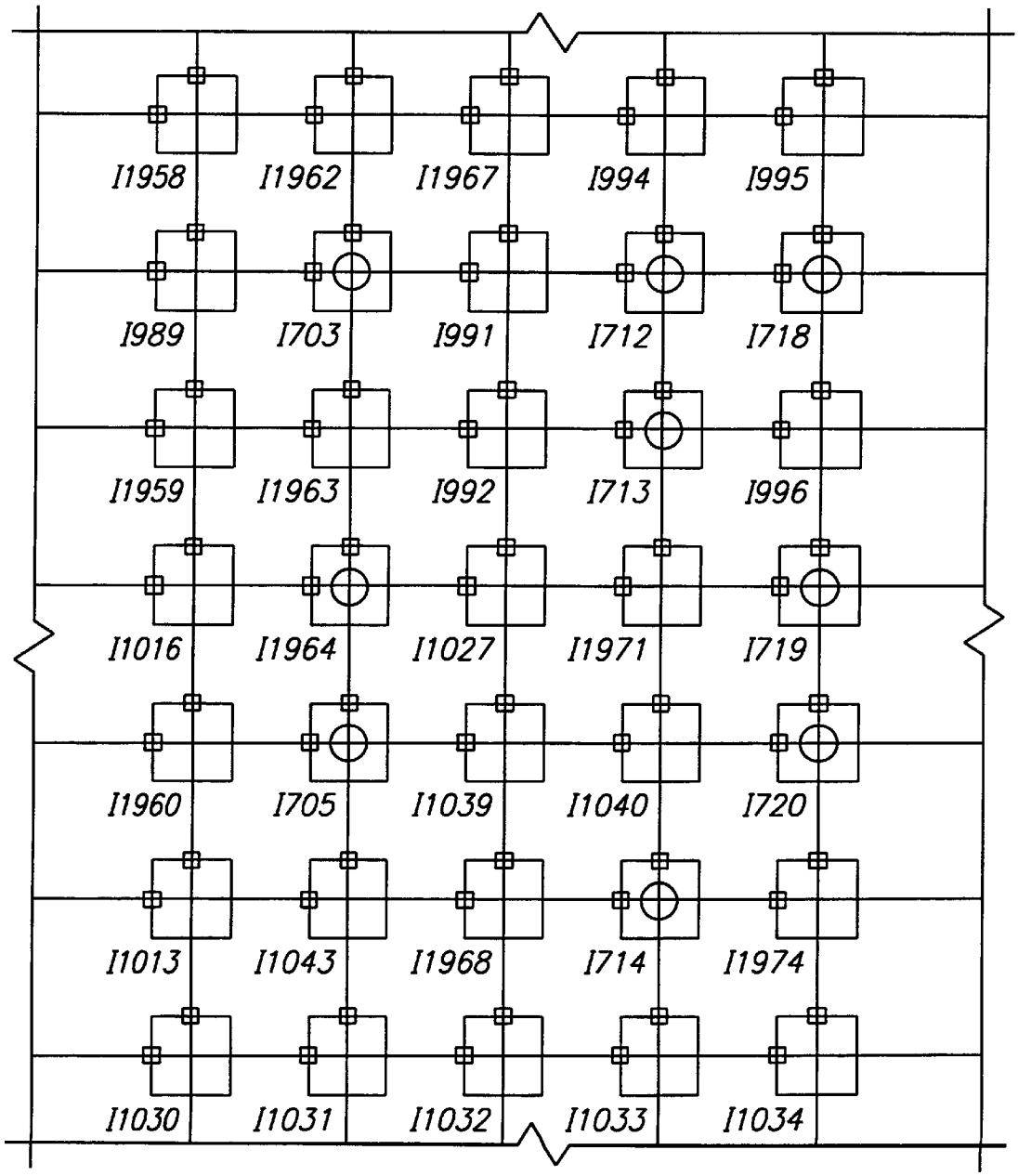


Fig. 9.0110308

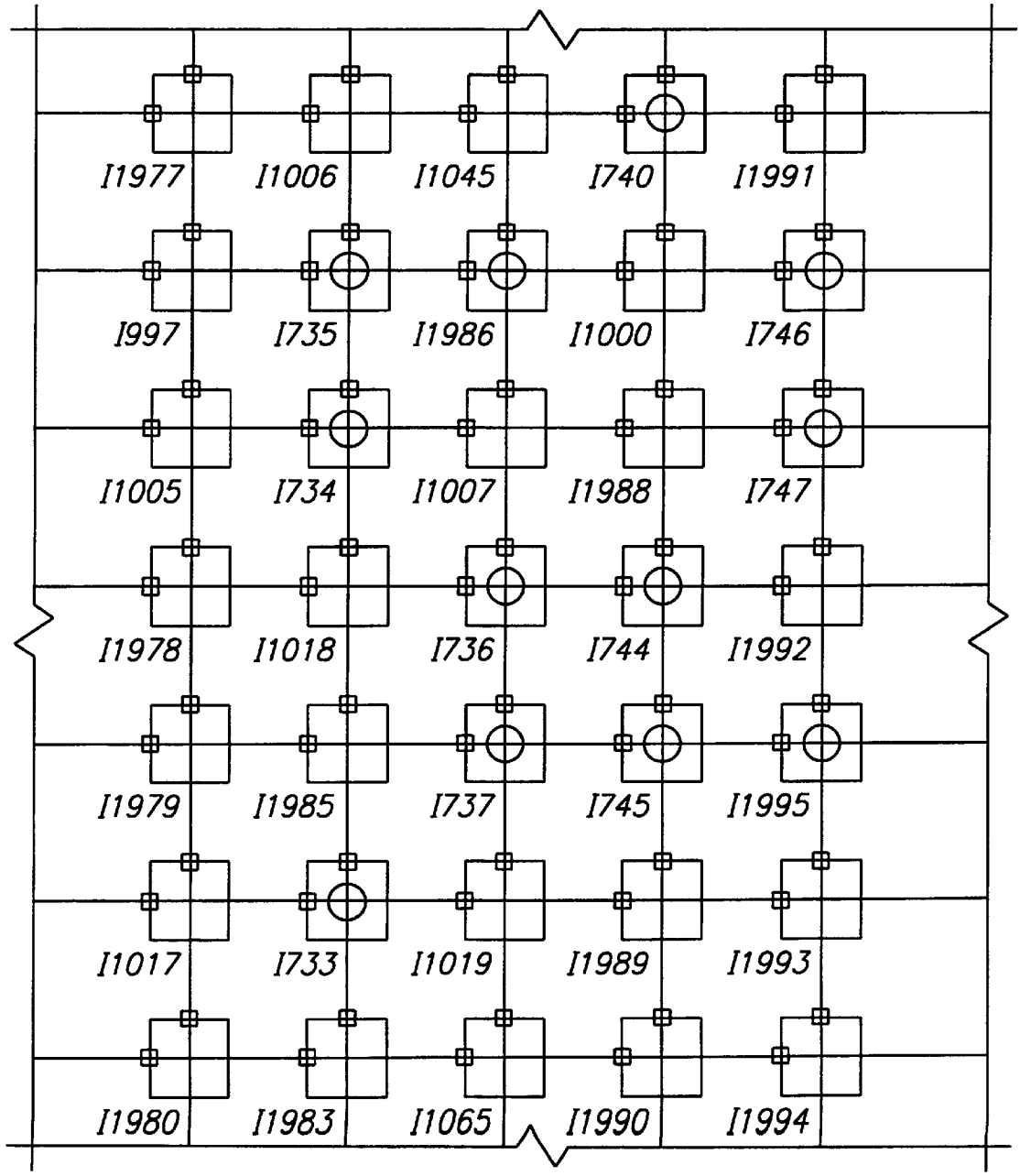

I1977
I1006
I1045
I740
I1991
I997
I735
I1986
I1000
I746
I1005
I734
I1007
I1988
I747
I1978
I1018
I736
I744
I1992
I1979
I1985
I737
I745
I1995
I1017
I733
I1019
I1989
I1993
I1980
I1983
I1065
I1990
I1994

Fig 9.0103DC

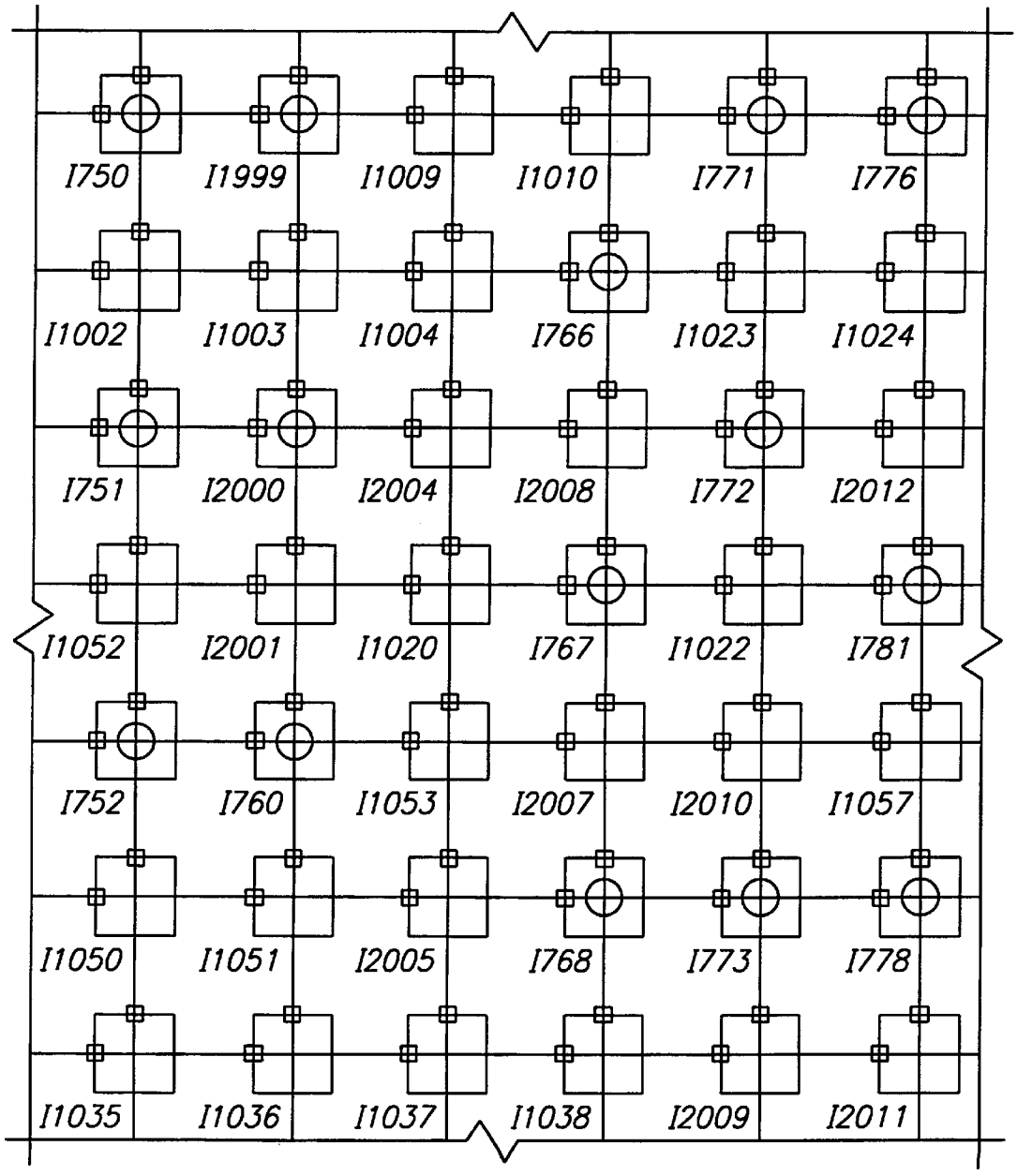
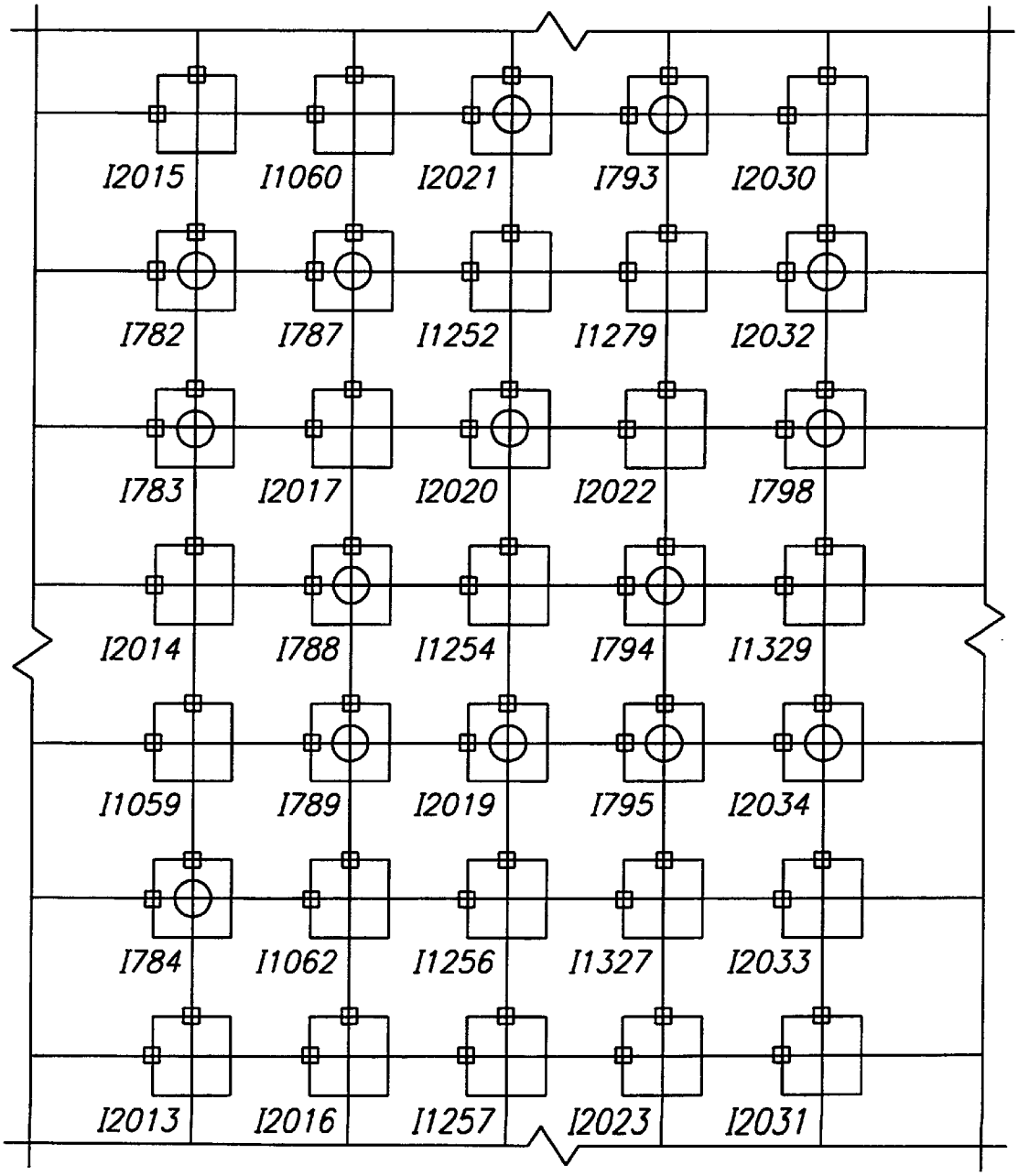

I750
I1999
I1009
I1010
I771
I776
I1002
I1003
I1004
I766
I1023
I1024
I751
I2000
I2004
I2008
I772
I2012
I1052
I2001
I1020
I767
I1022
I781
I752
I760
I1053
I2007
I2010
I1057
I1050
I1051
I2005
I768
I773
I778
I1035
I1036
I1037
I1038
I2009
I2011

Fig 9.01030D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I1279
I2032
I783
I2017
I2020
I2022
I798
I2014
I788
I1254
I794
I1329
I1059
I789
I2019
I795
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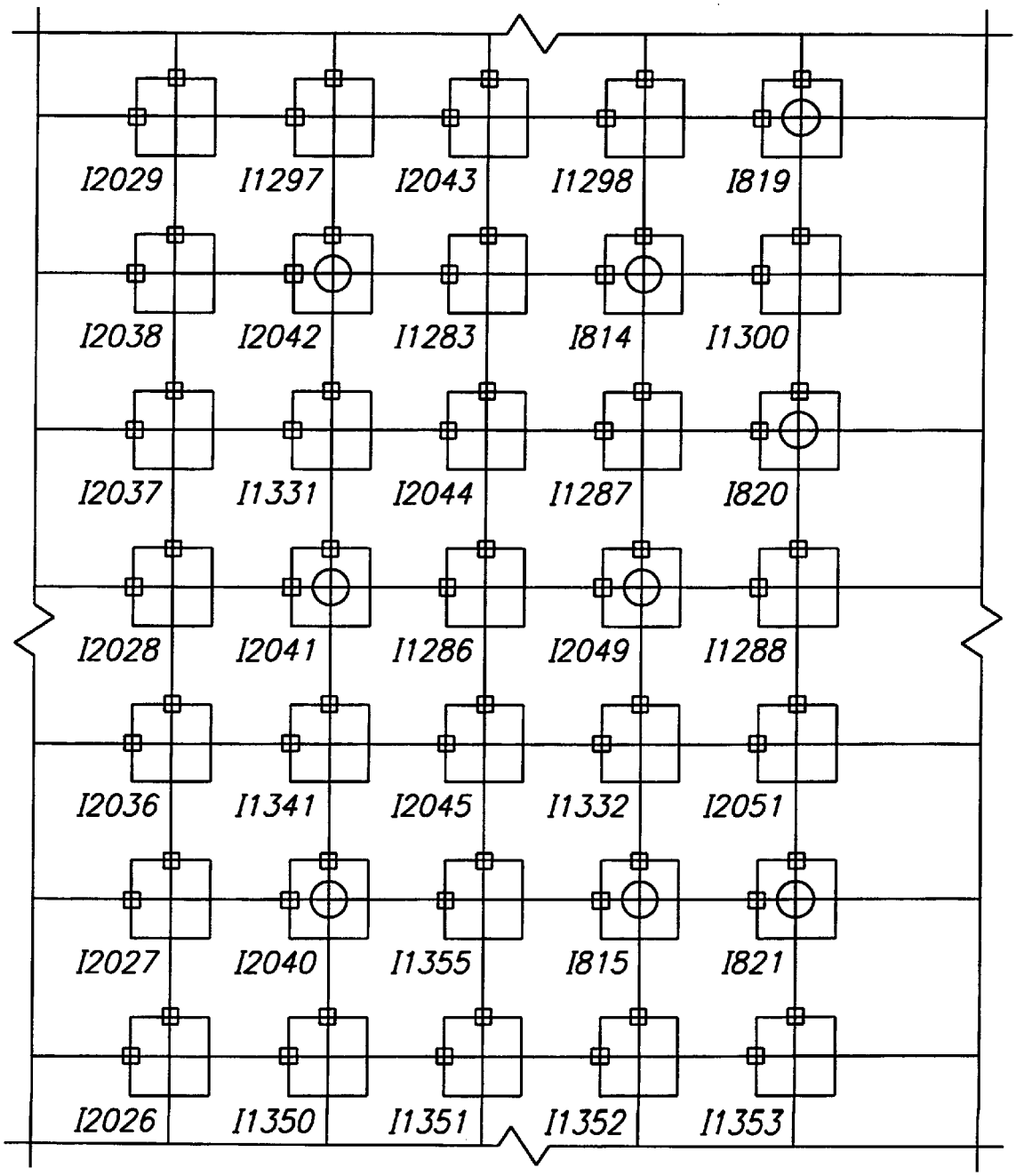
I1327
I2033
I2013
I2016
I1257
I2023
I2031

Fig 9.0103DE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I820
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I2036
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I2045
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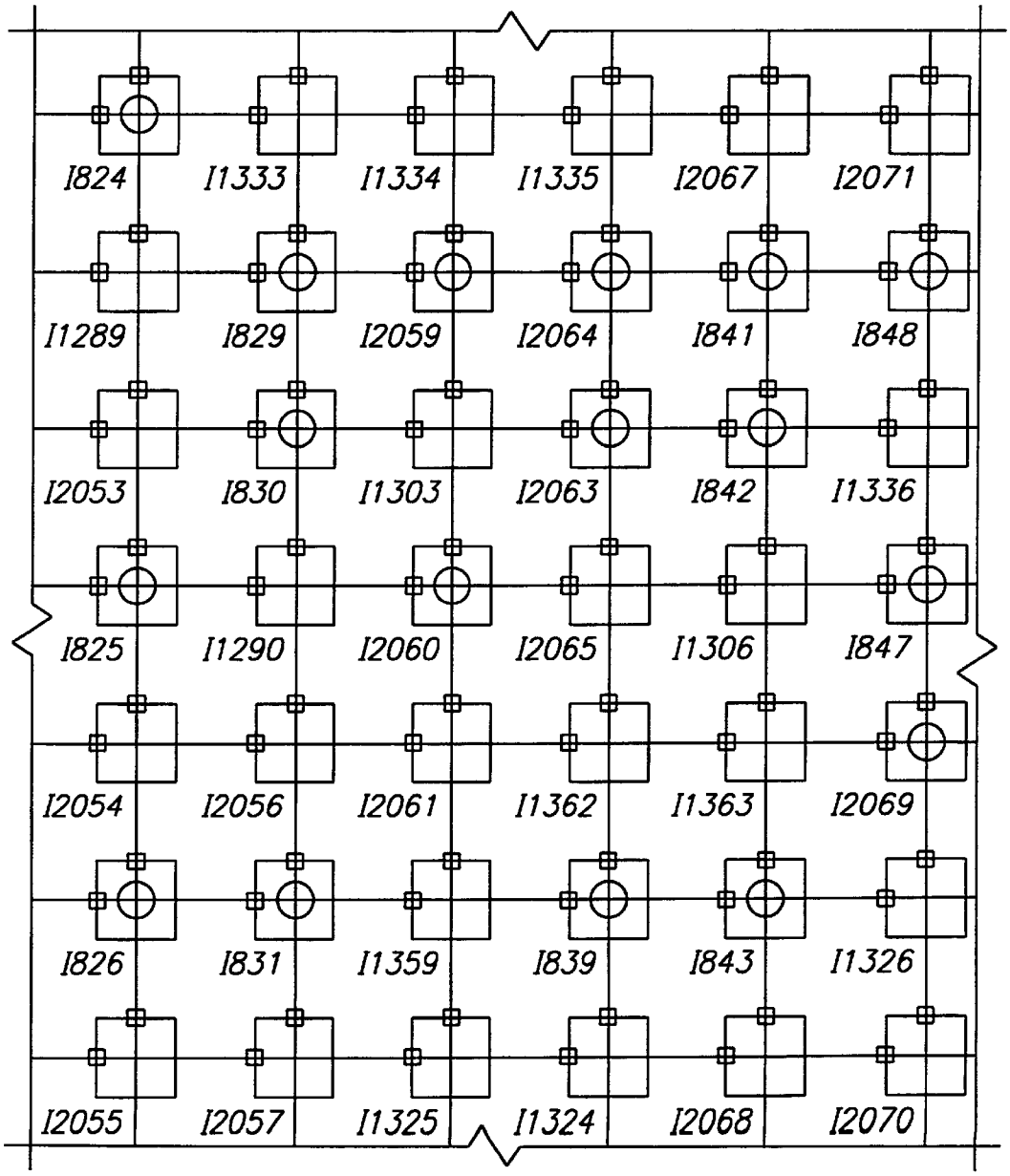
Fig 9.01030F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I2063
I842
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I825
I1290
I2060
I2065
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I2061
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I2069
I826
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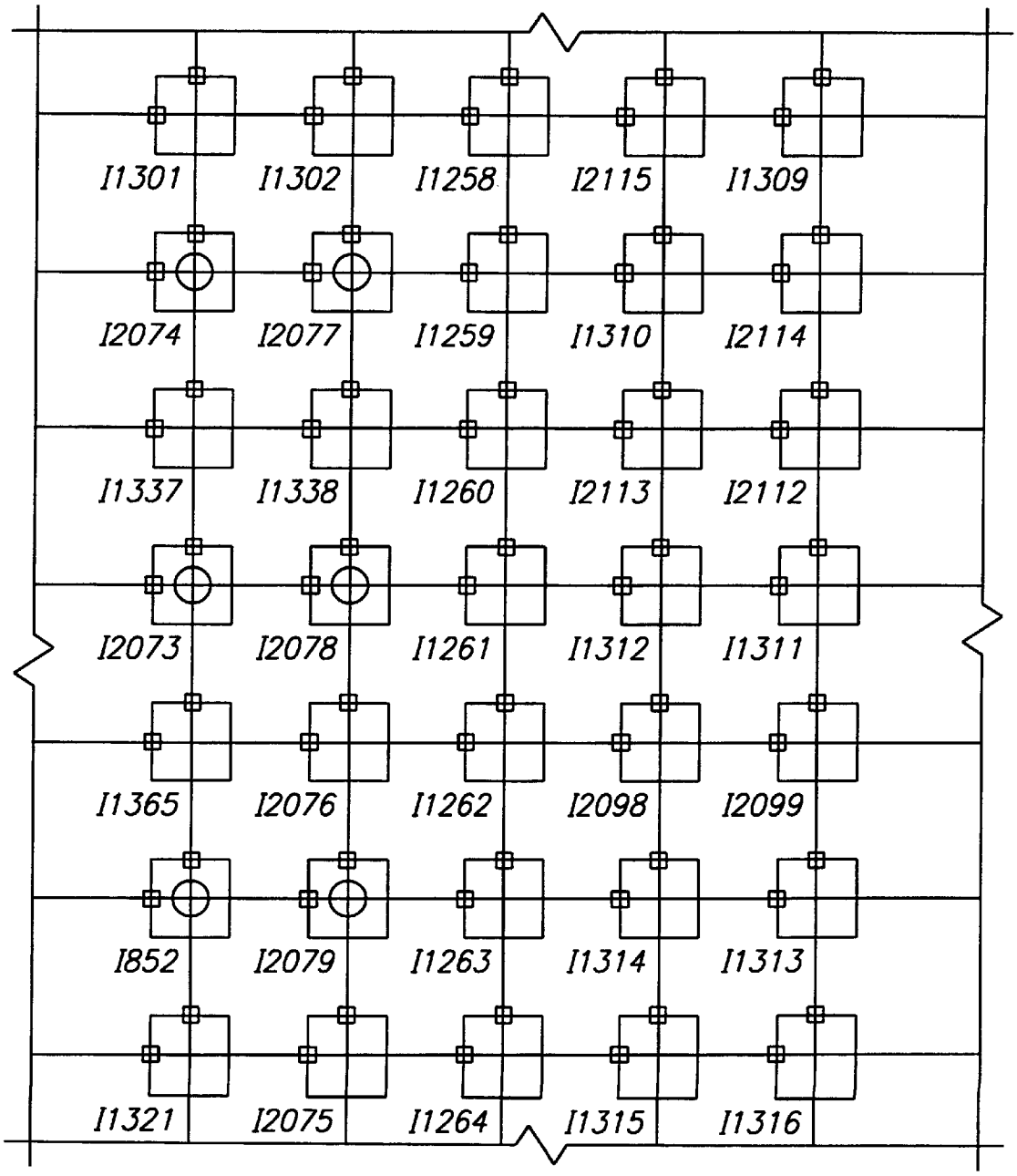
I1324
I2068
I2070

Fig 9.01030G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I1259
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I1260
I2113
I2112
I2073
I2078
I1261
I1312
I1311
I1365
I2076
I1262
I2098
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I1321
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I1264
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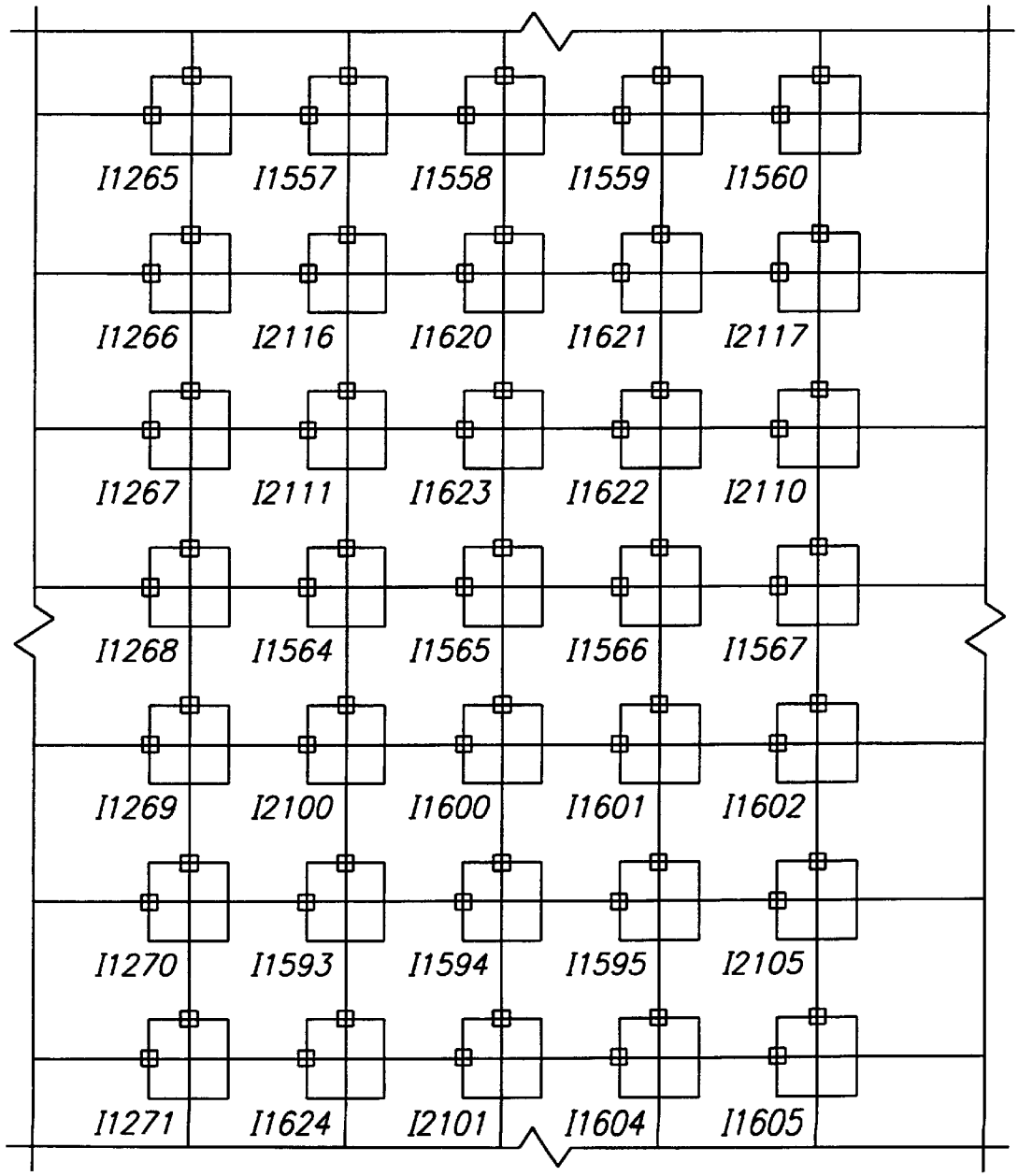
I1316

Fig 9.01030H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I1622
I2110
I1268
I1564
I1565
I1566
I1567
I1269
I2100
I1600
I1601
I1602
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I2105
I1271
I1624
I2101
I1604
I1605

Fig 9.0102

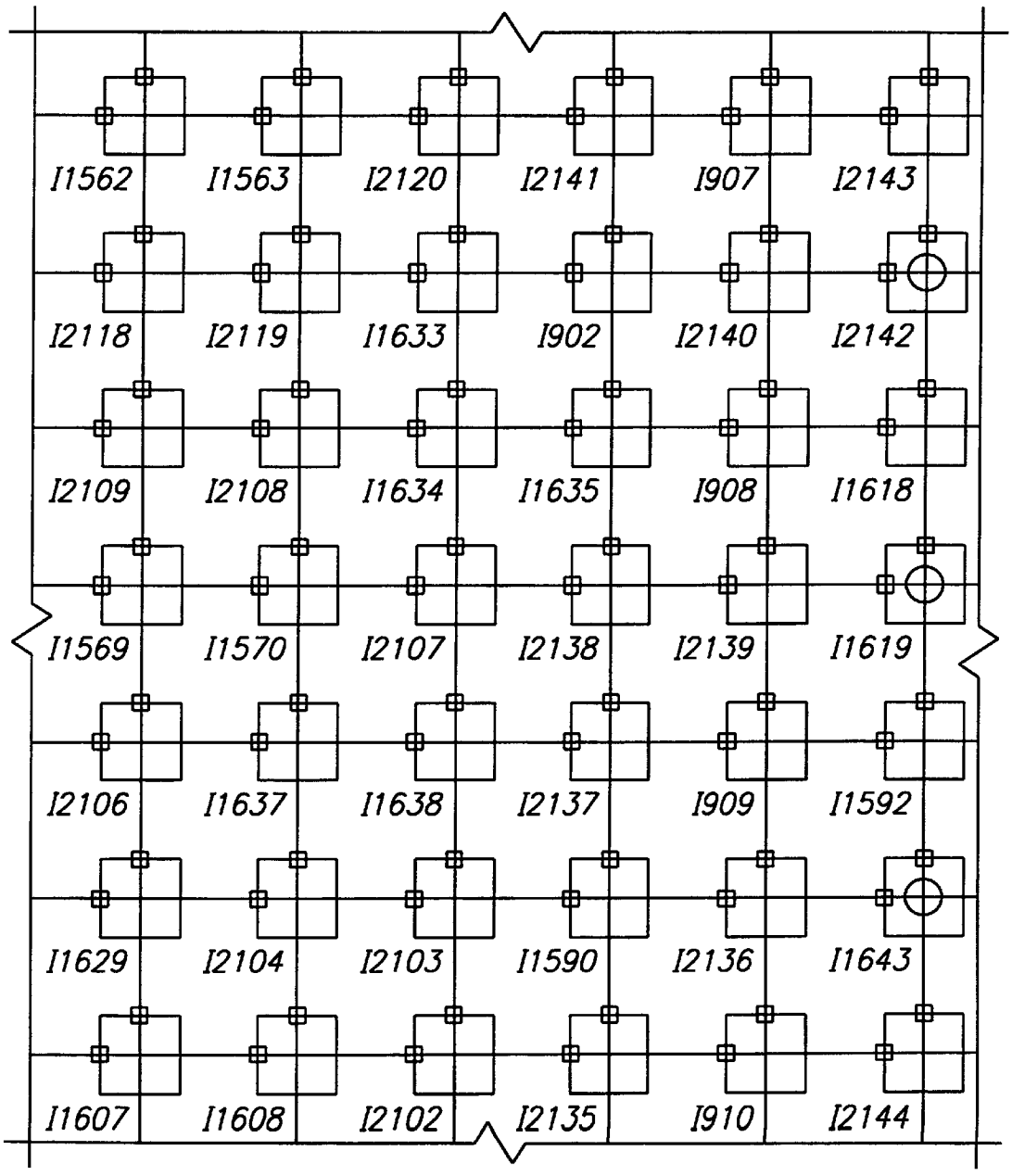
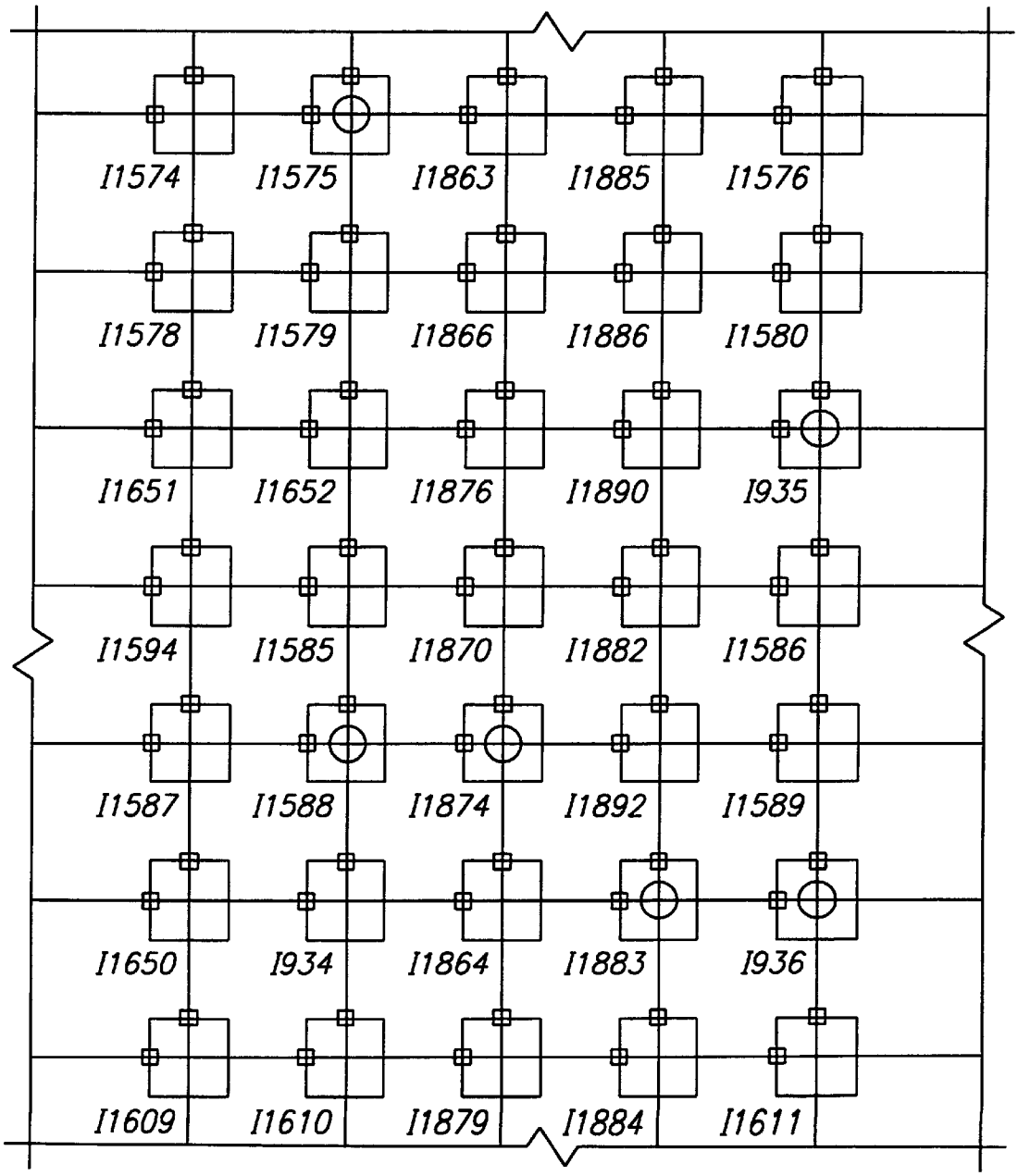


Fig 9.0110300.1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I1870
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I1588
I1874
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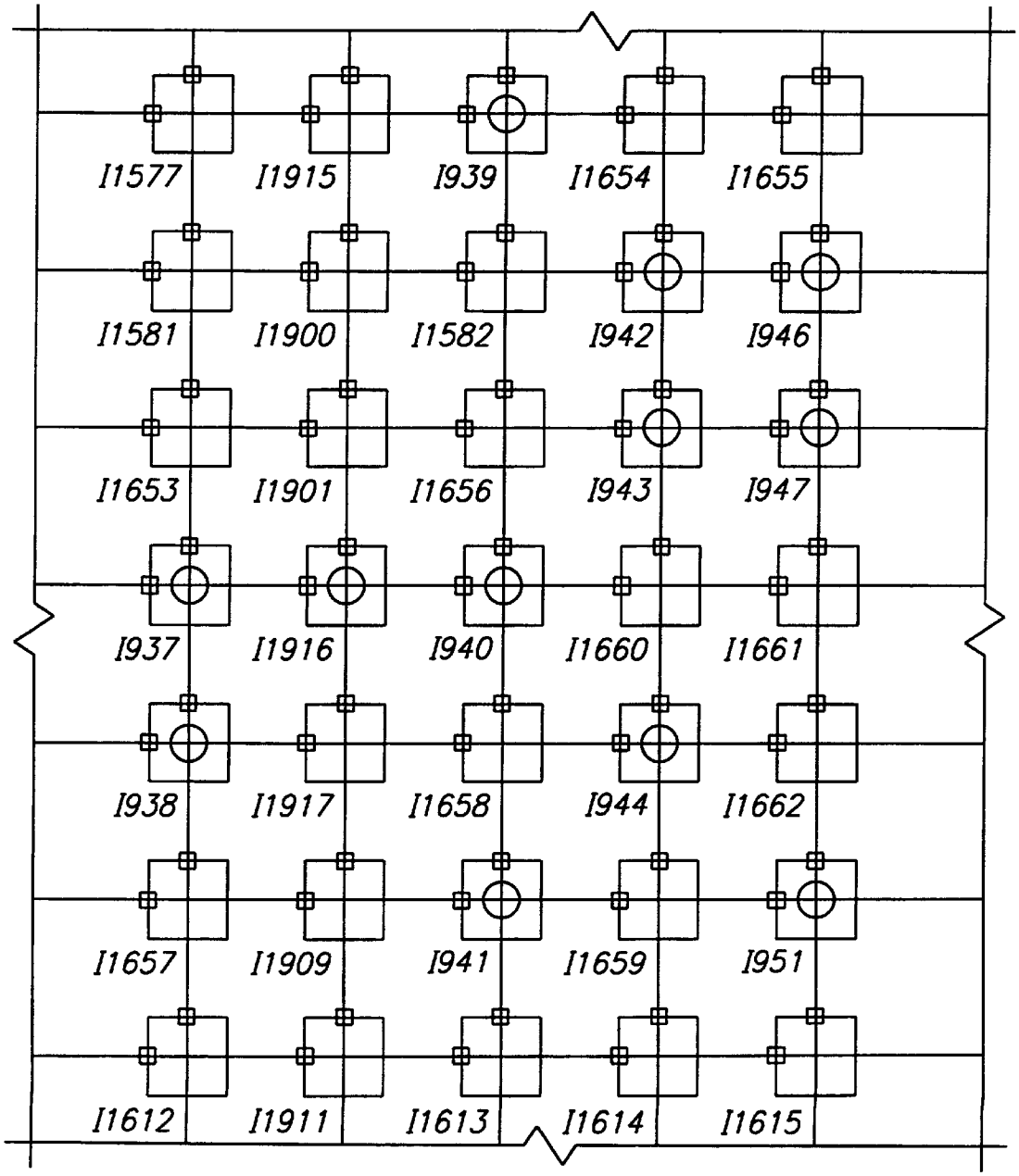
Fig 9.0130K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I1660
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I1658
I944
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I951
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I1615

Fig 9.0110.0L

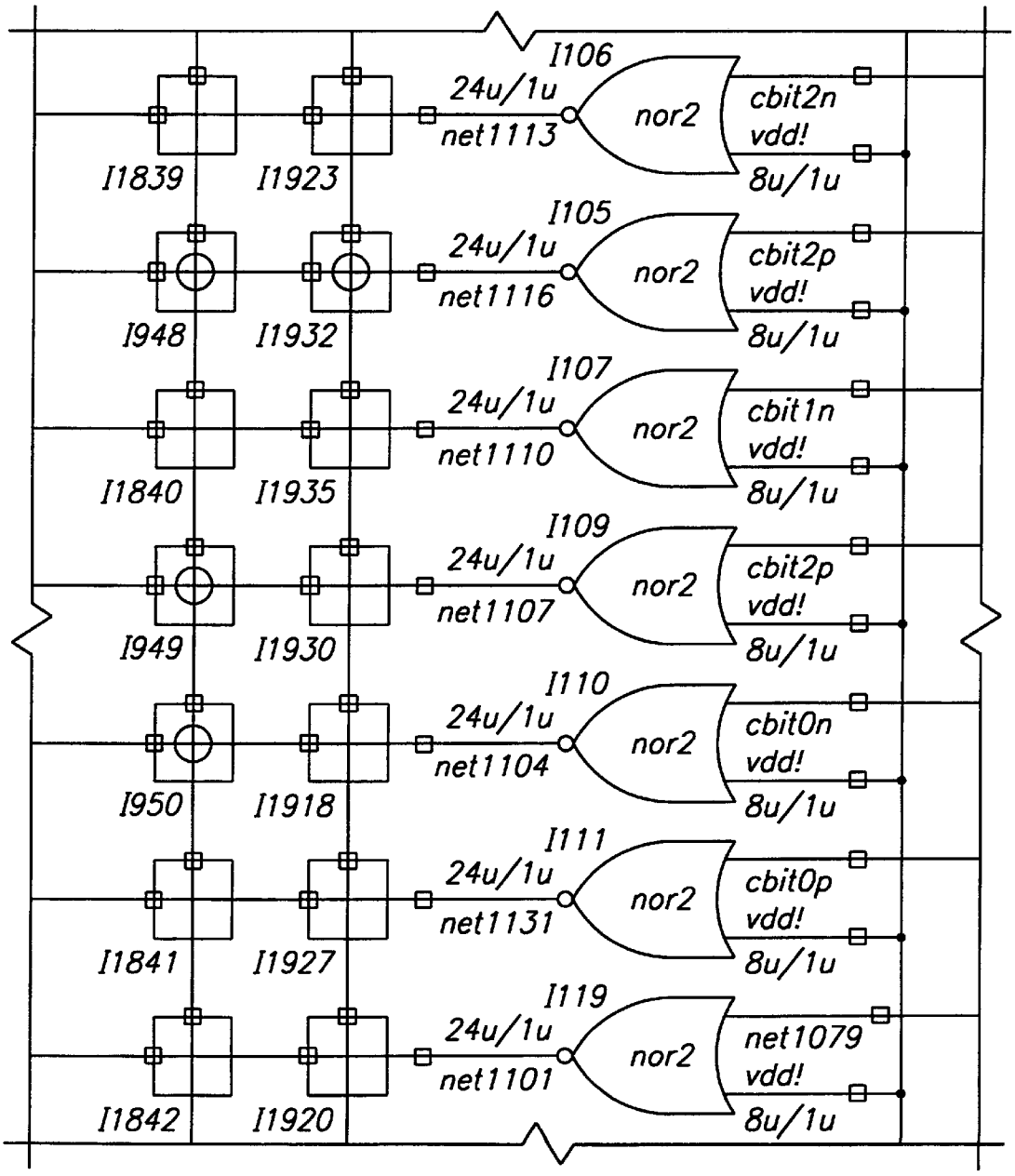


Fig 9.0110300M

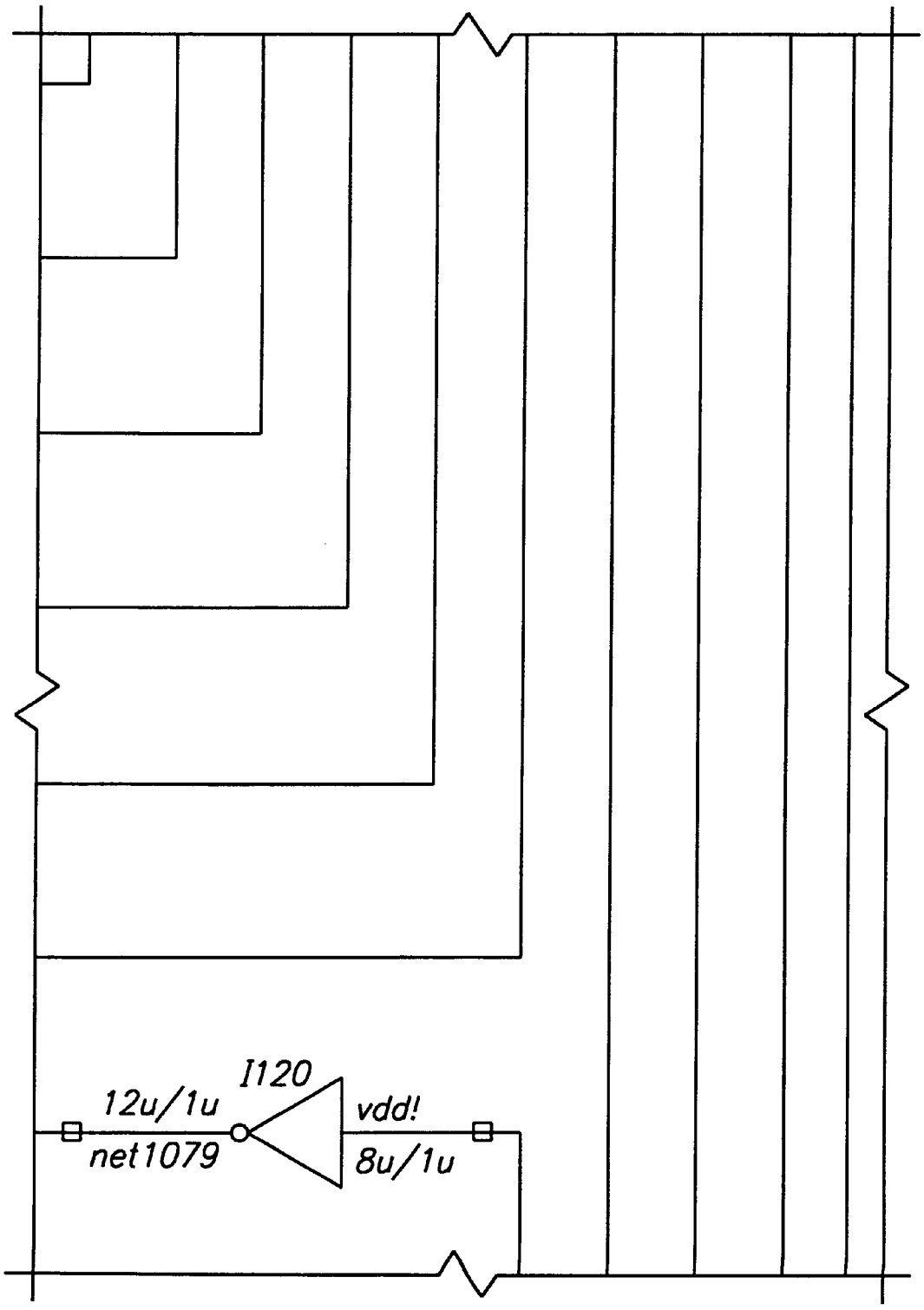


Fig 9.0103DN

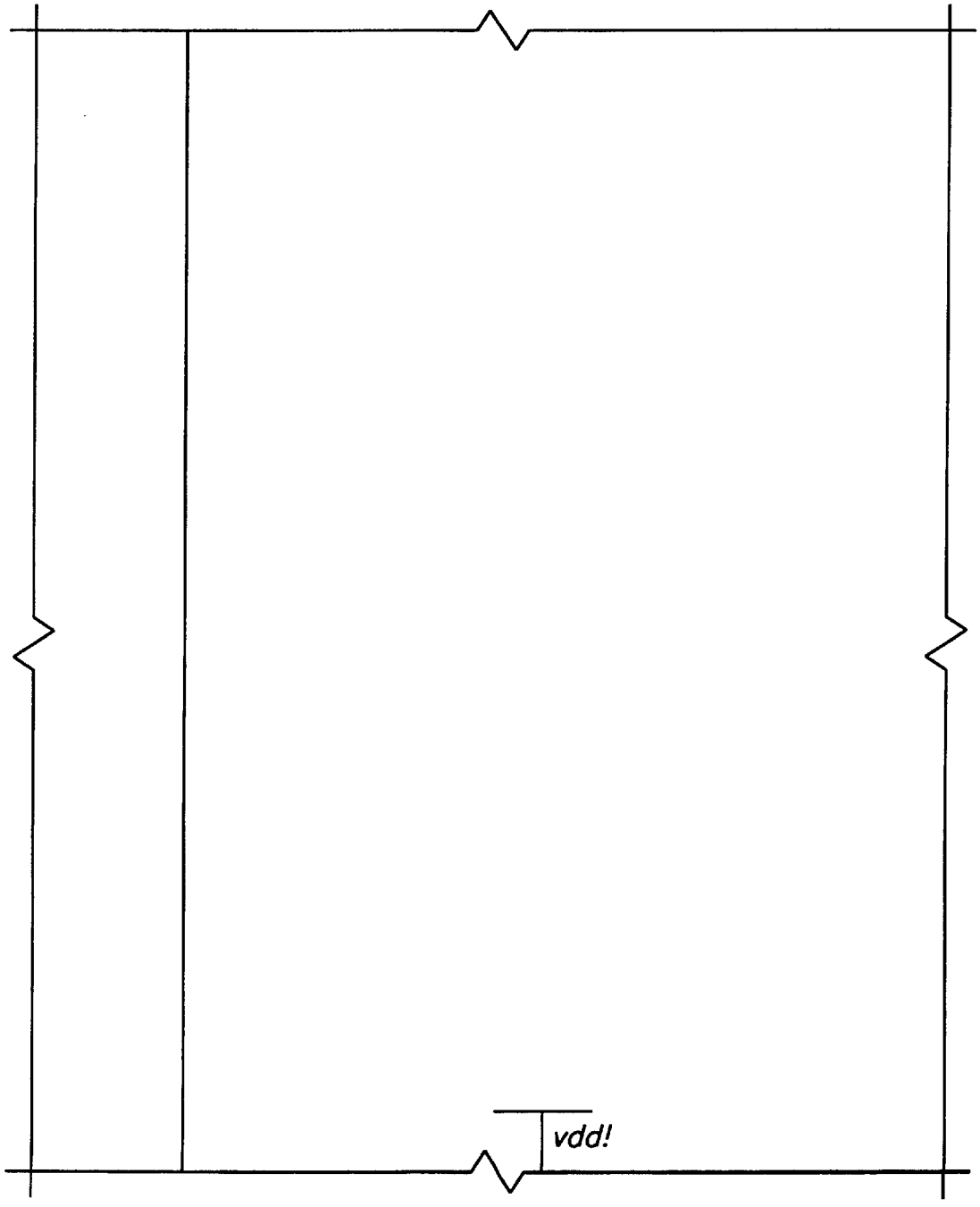


Fig 9.0103000

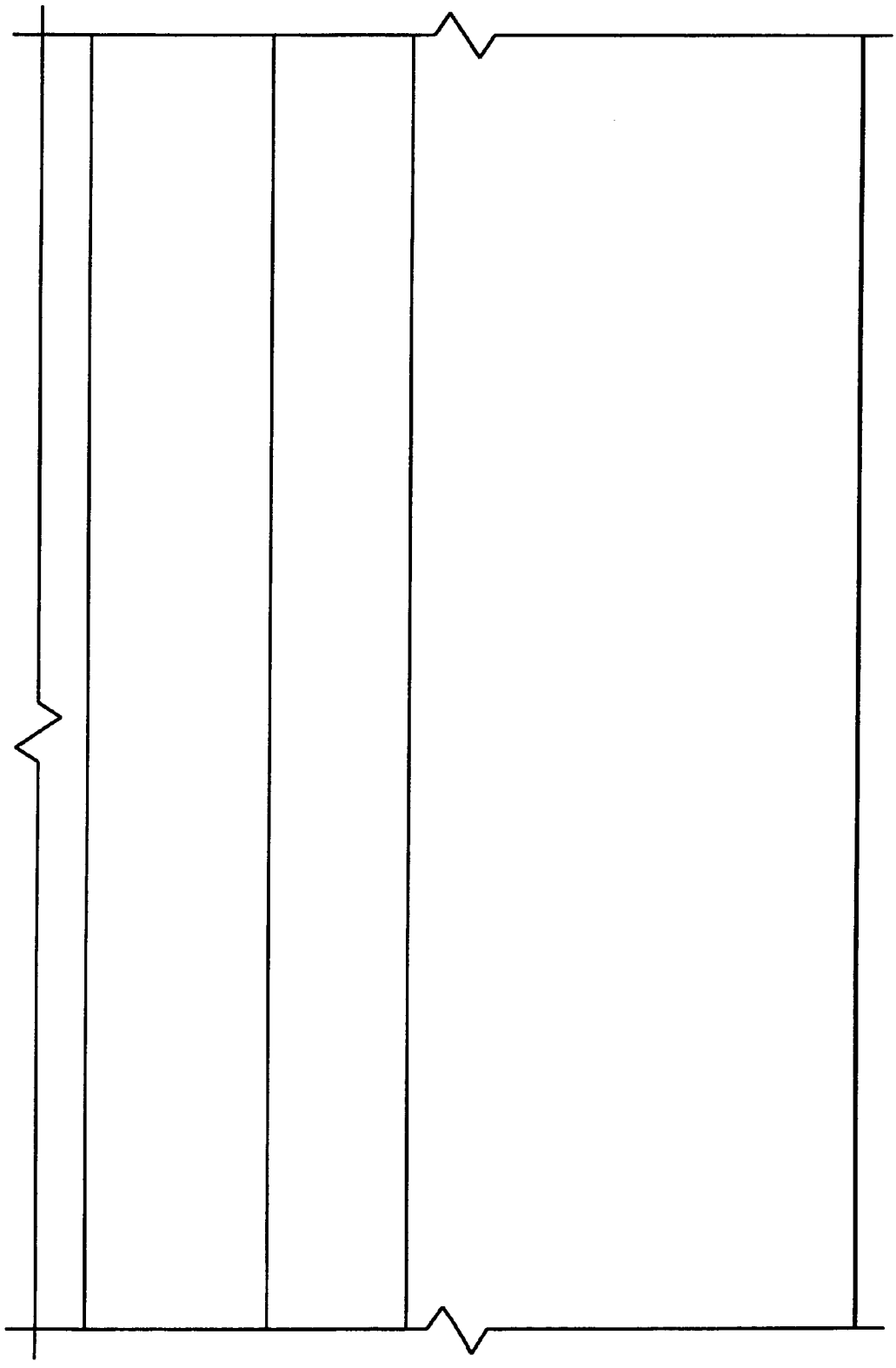
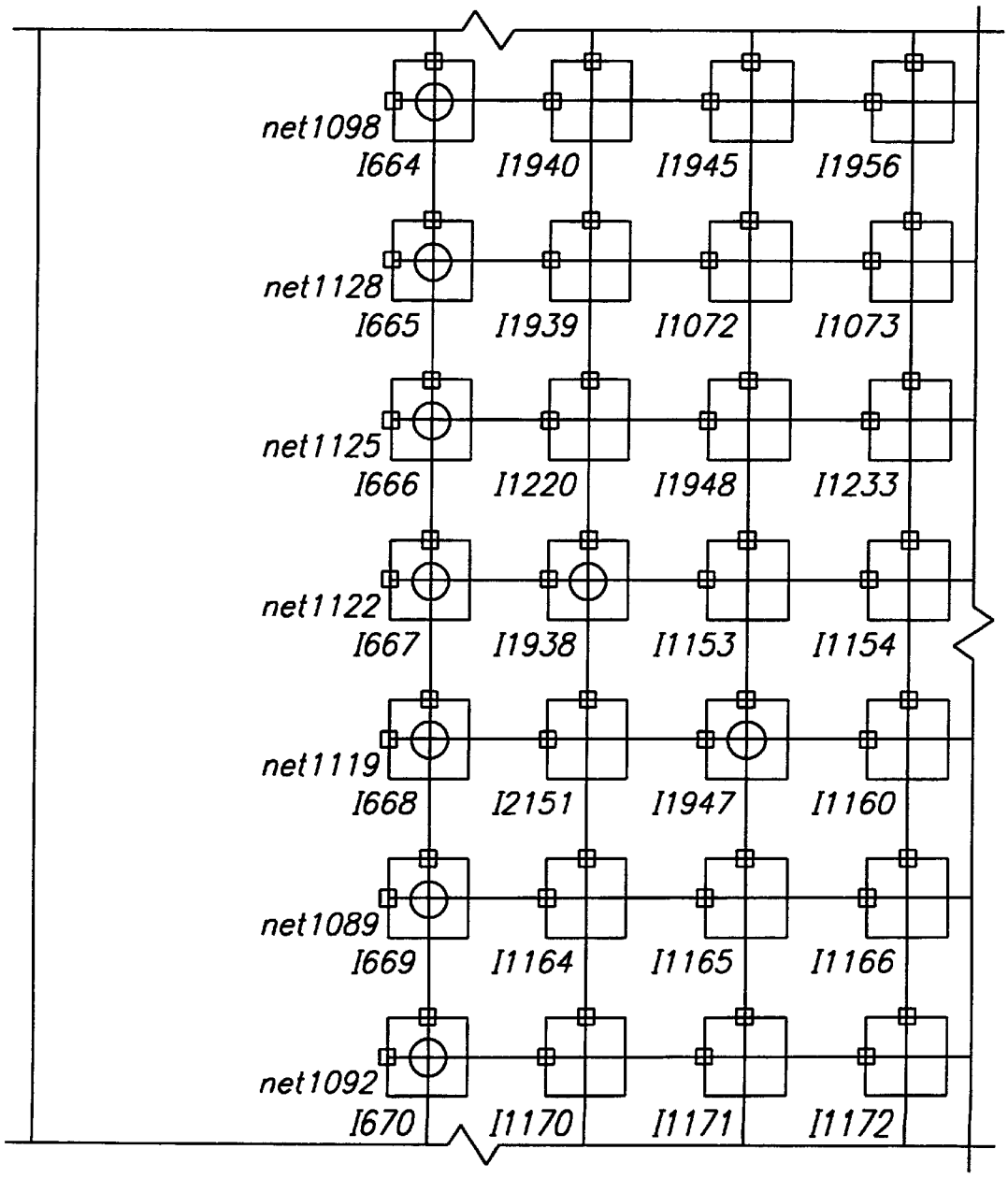


Fig 9.01030P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I1956
net1128
I665
I1939
I1072
I1073
net1125
I666
I1220
I1948
I1233
net1122
I667
I1938
I1153
I1154
net1119
I668
I2151
I1947
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Fig 9.0130EA

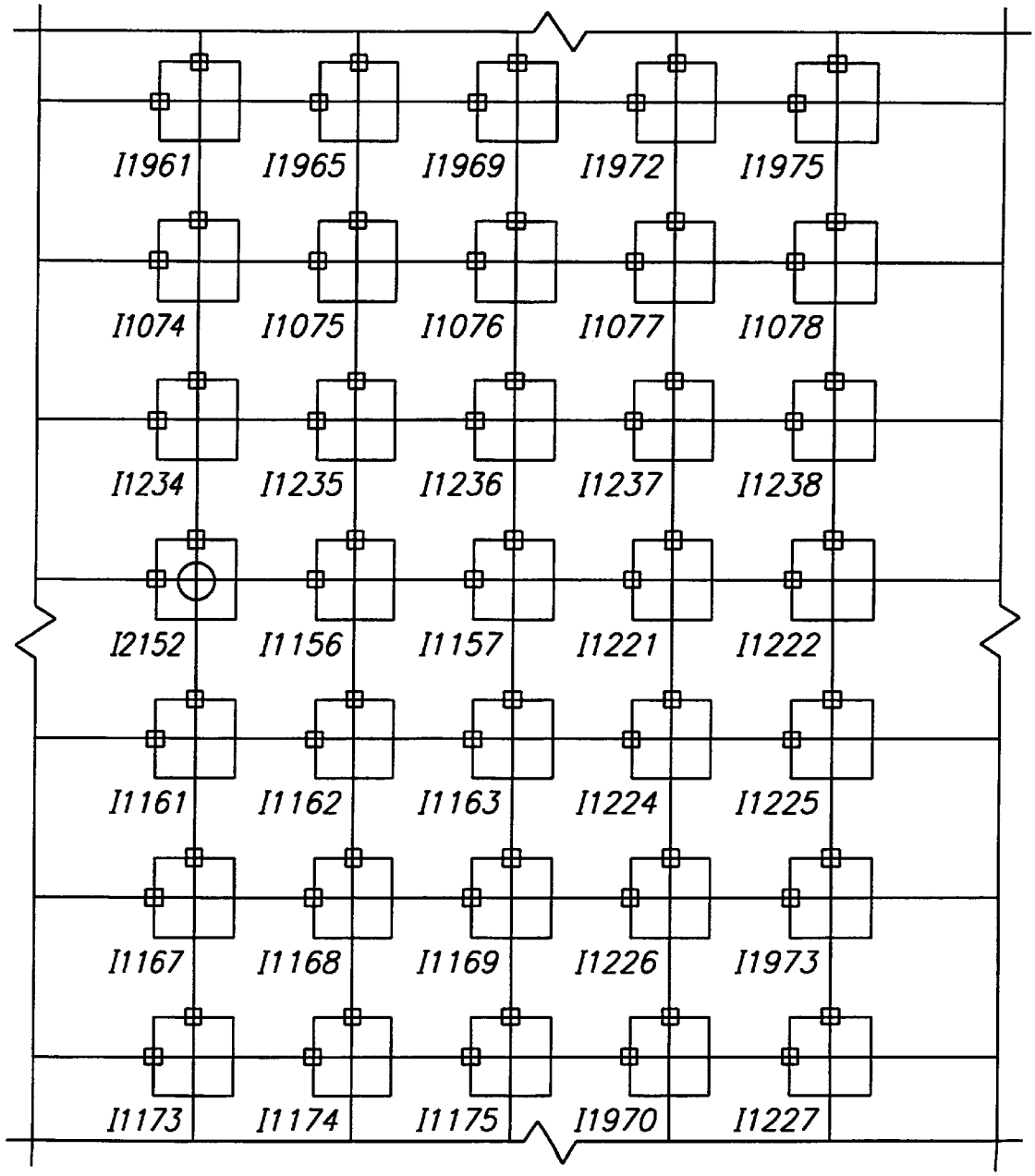
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Fig 9.0103EB

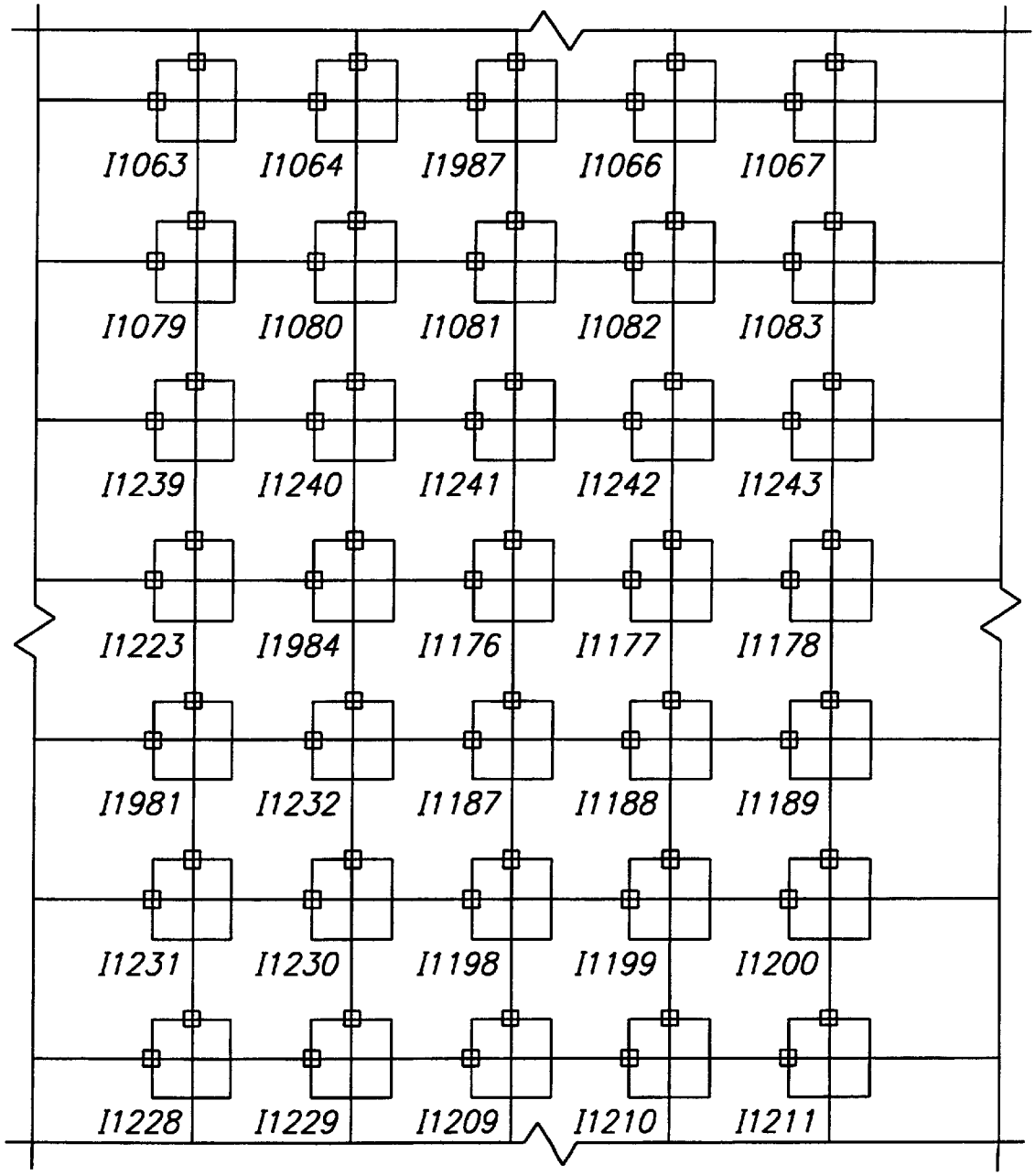
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Fig 9.0110EC

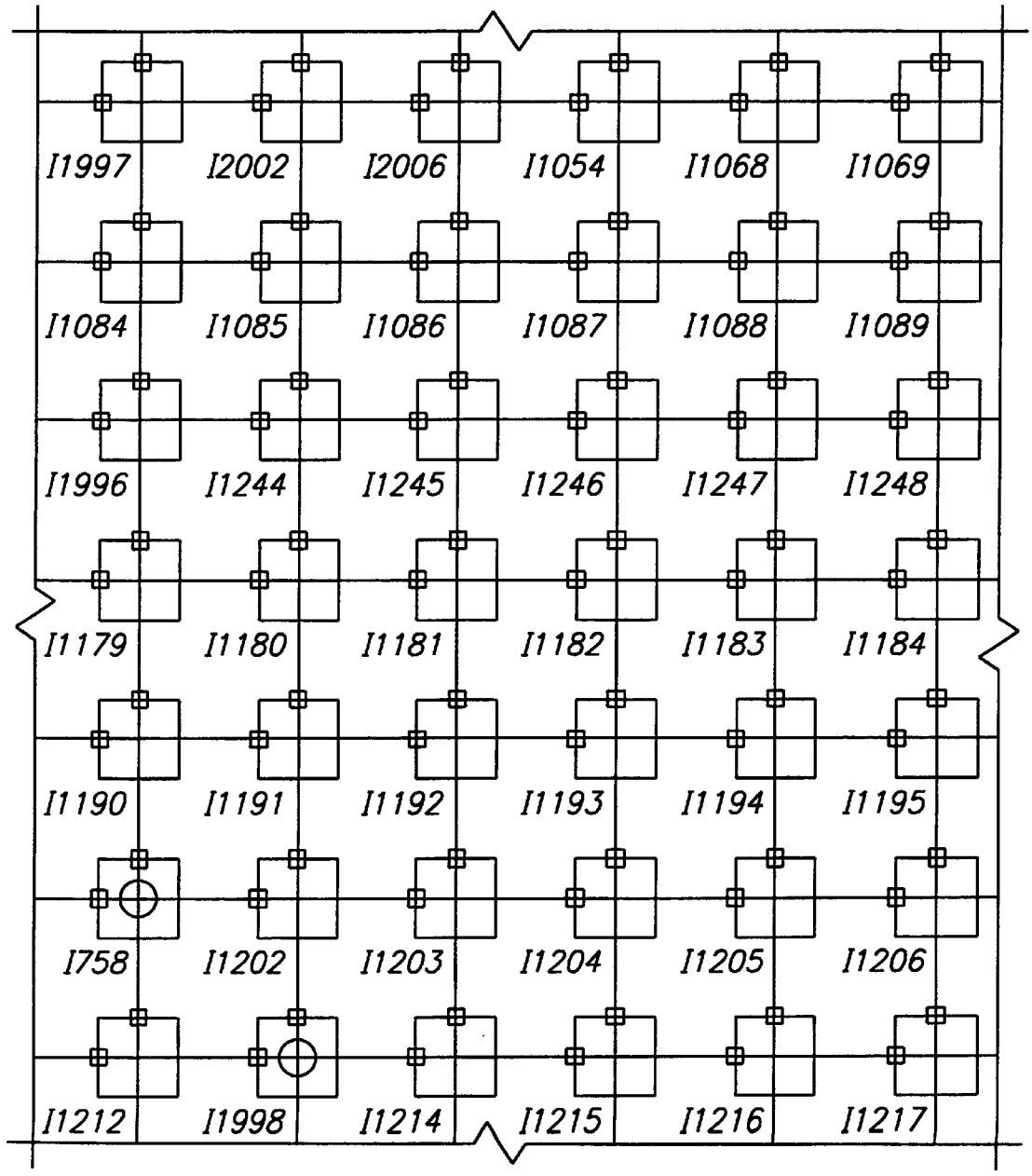
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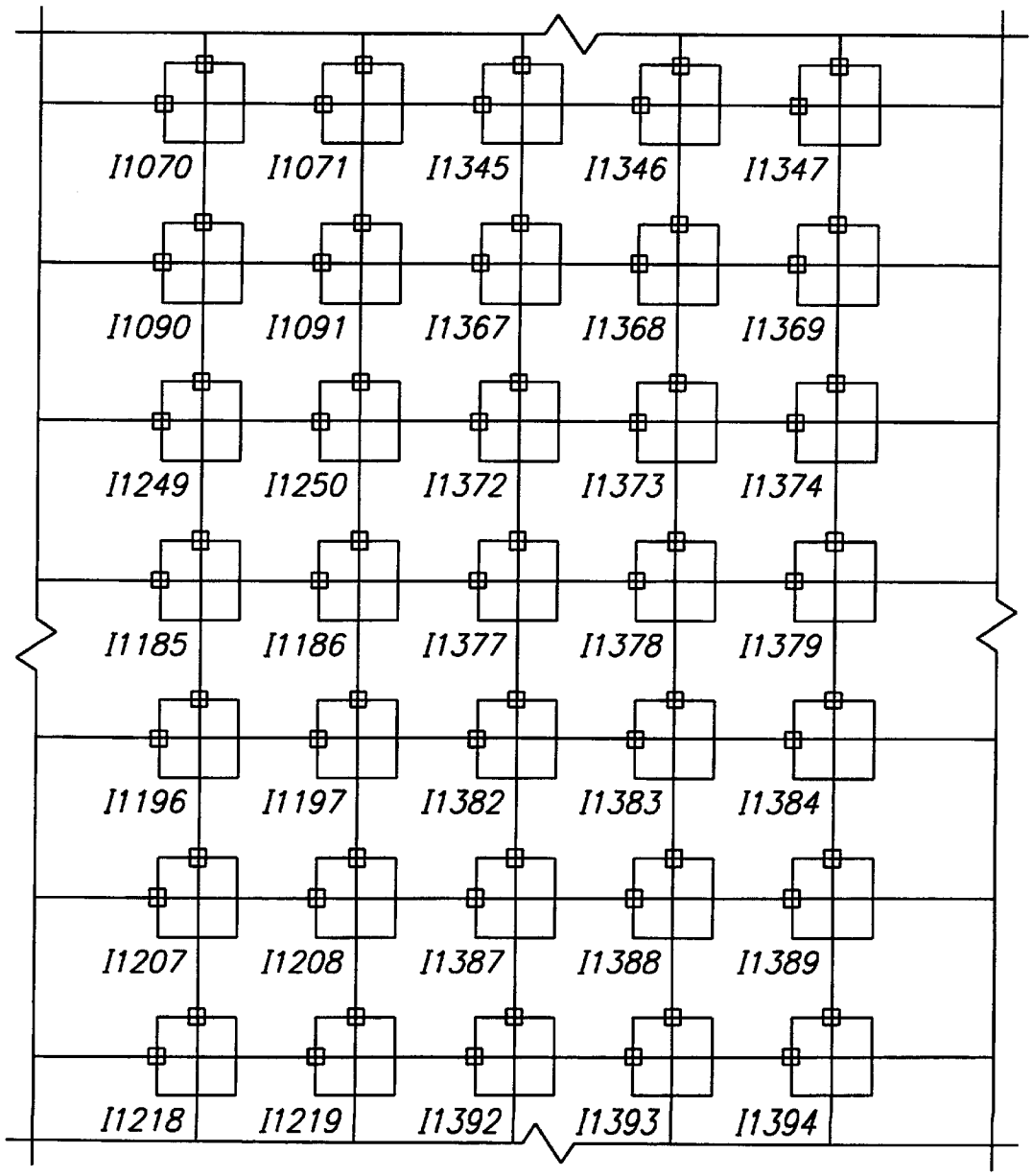
Fig 9.0110E0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I1394

Fig 9.0110E

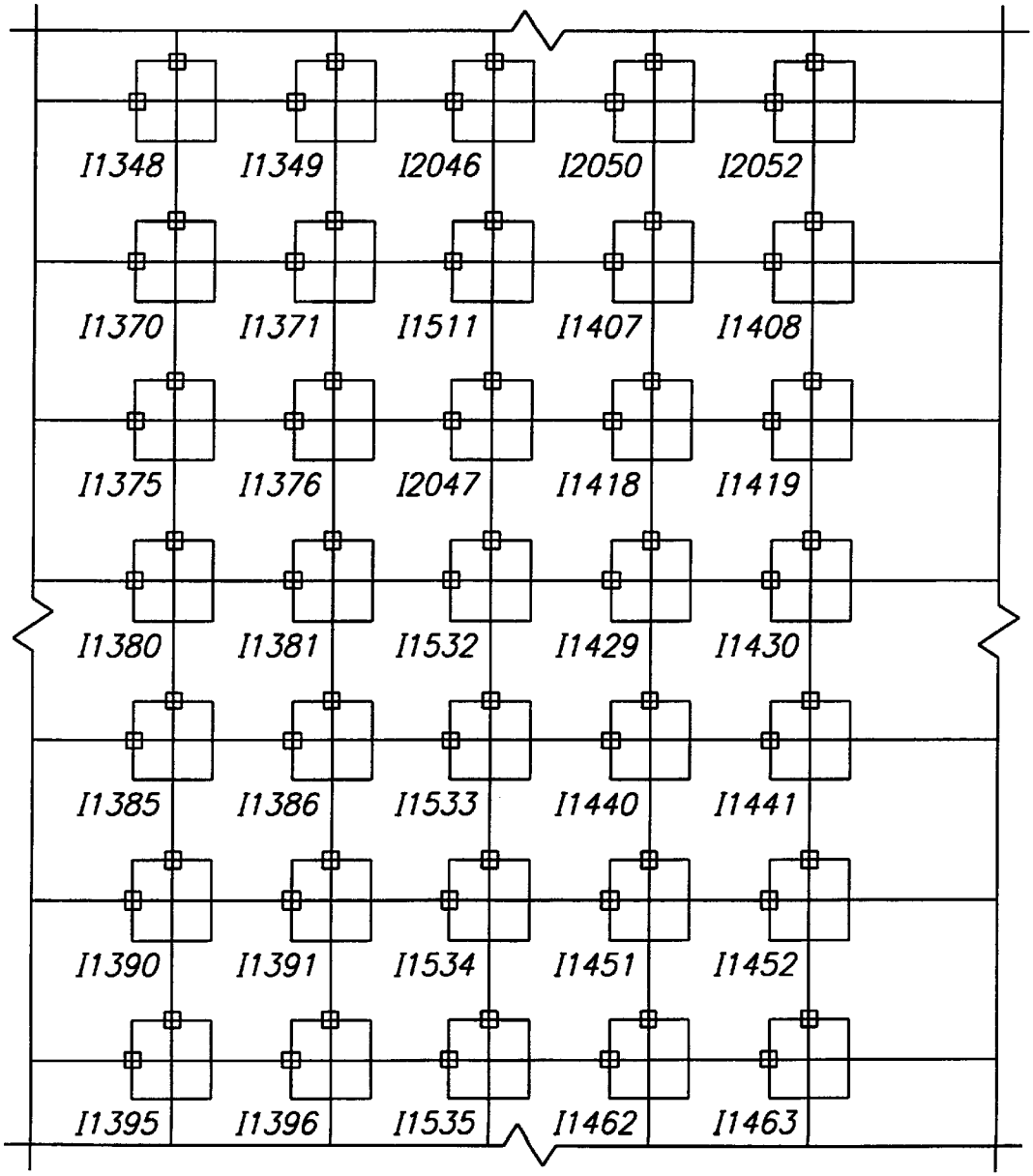
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Fig 9.0110EF

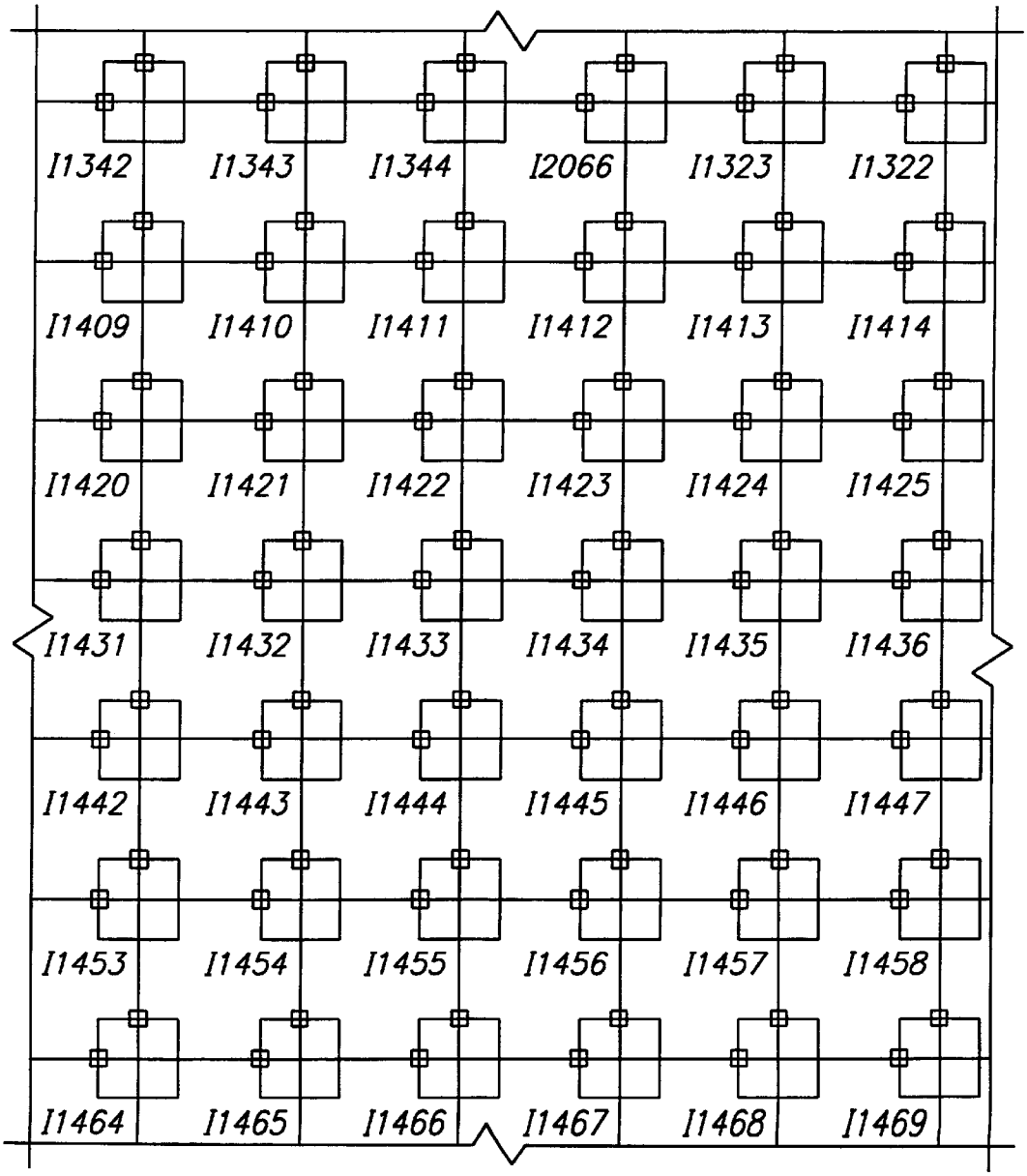
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Fig 9.0103E6

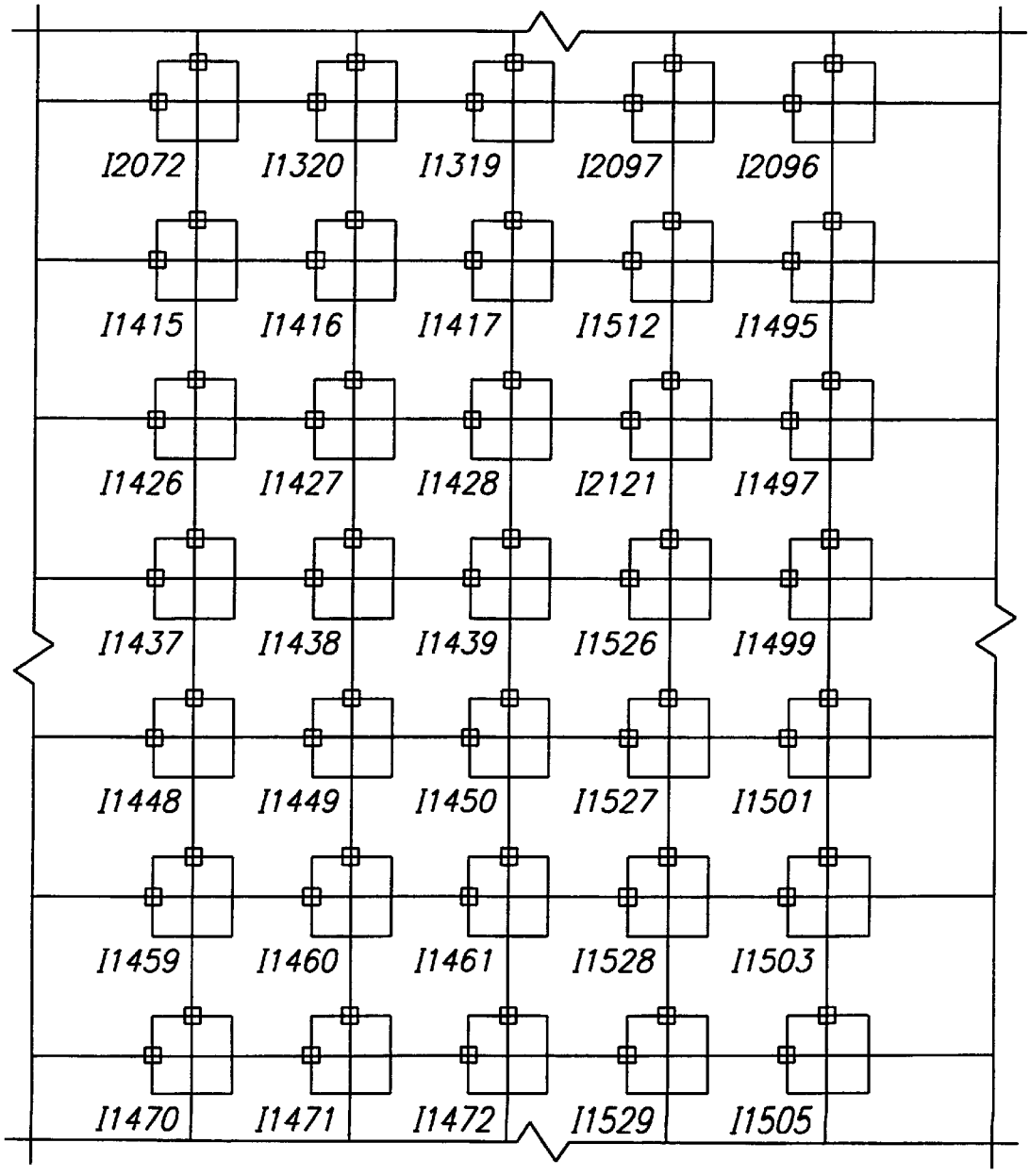
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Fig 9.0110EH

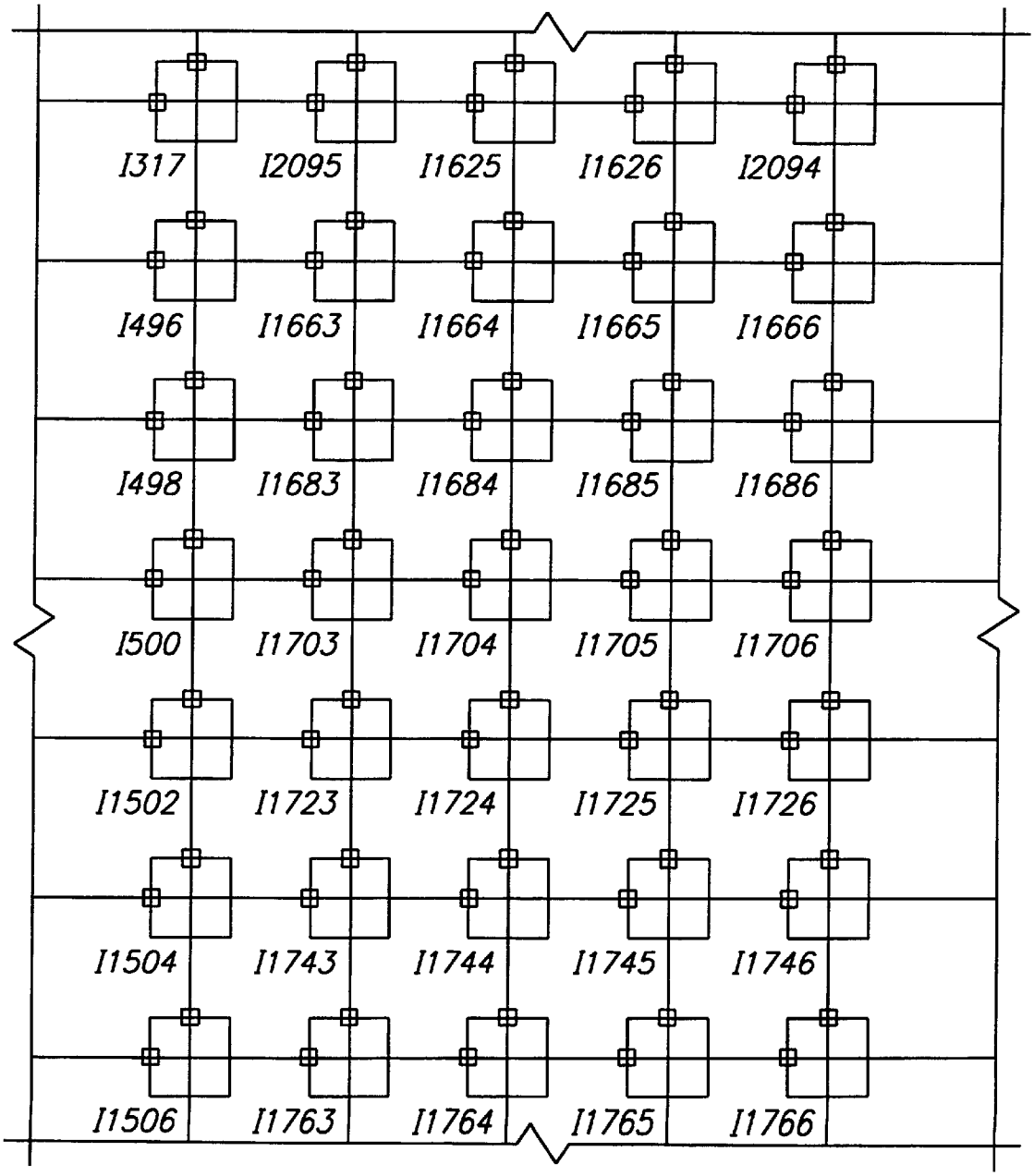

Fig 9.0110E II

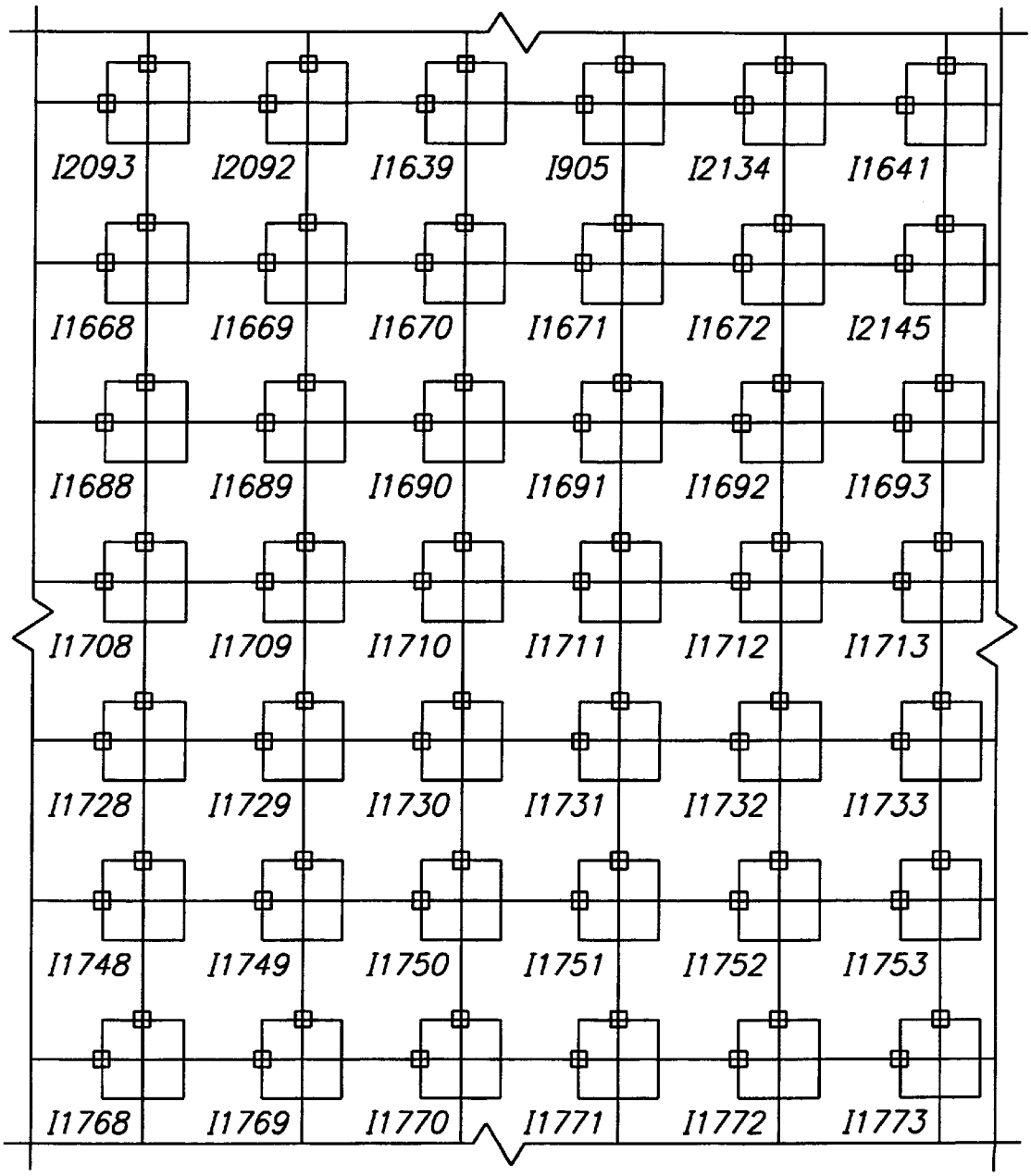
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Fig 9.0110E+1

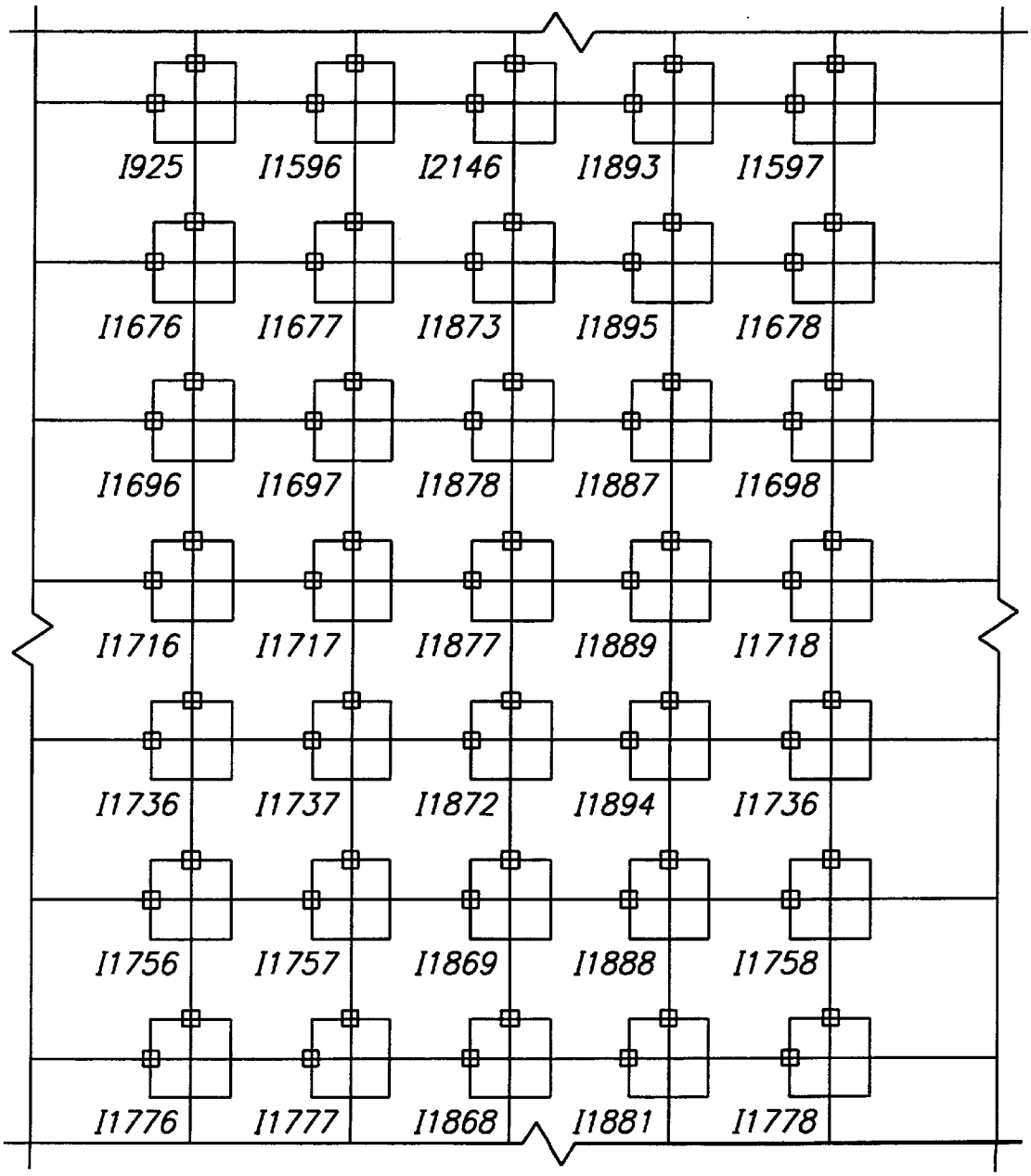
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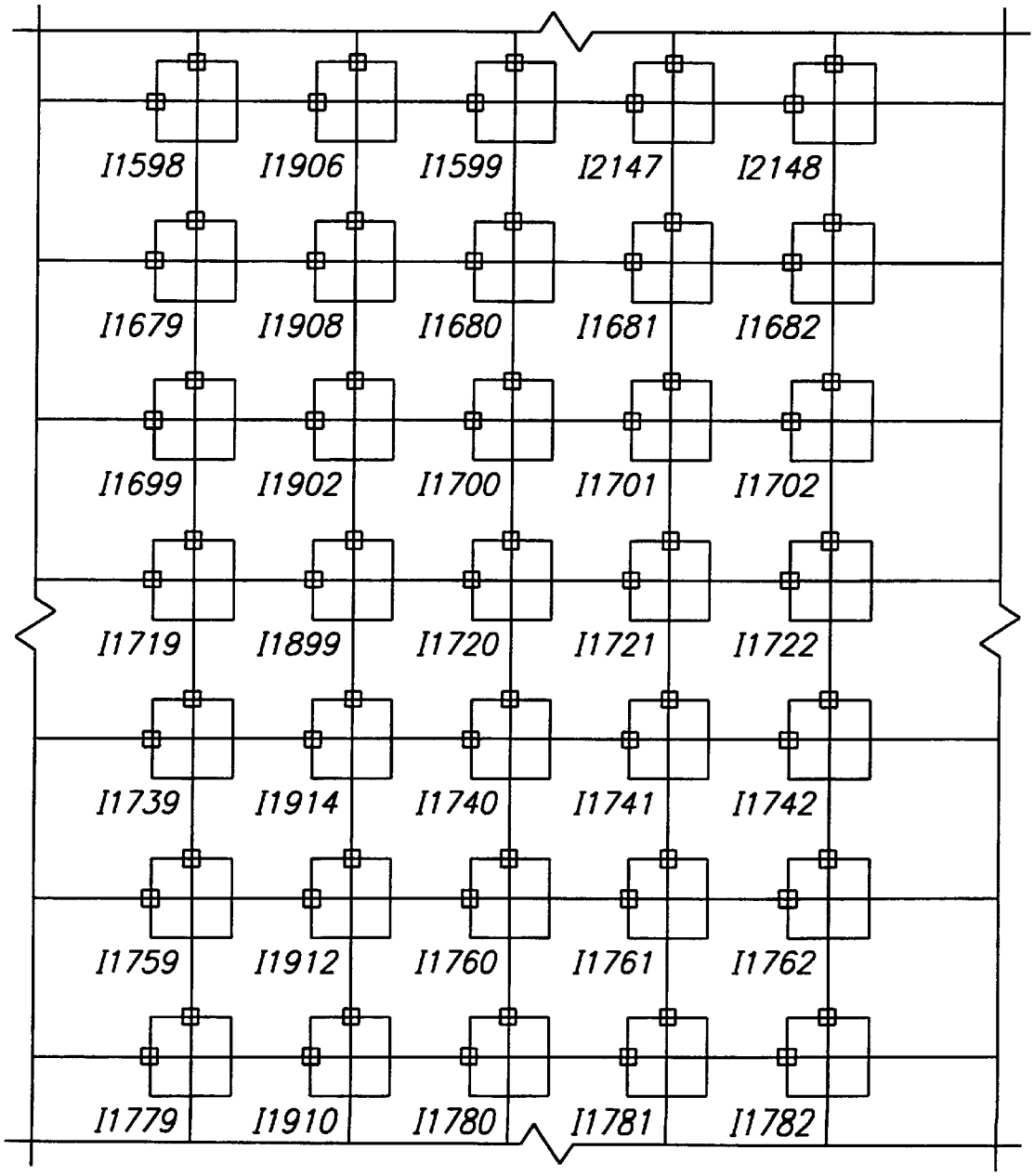
Fig 9.0113EK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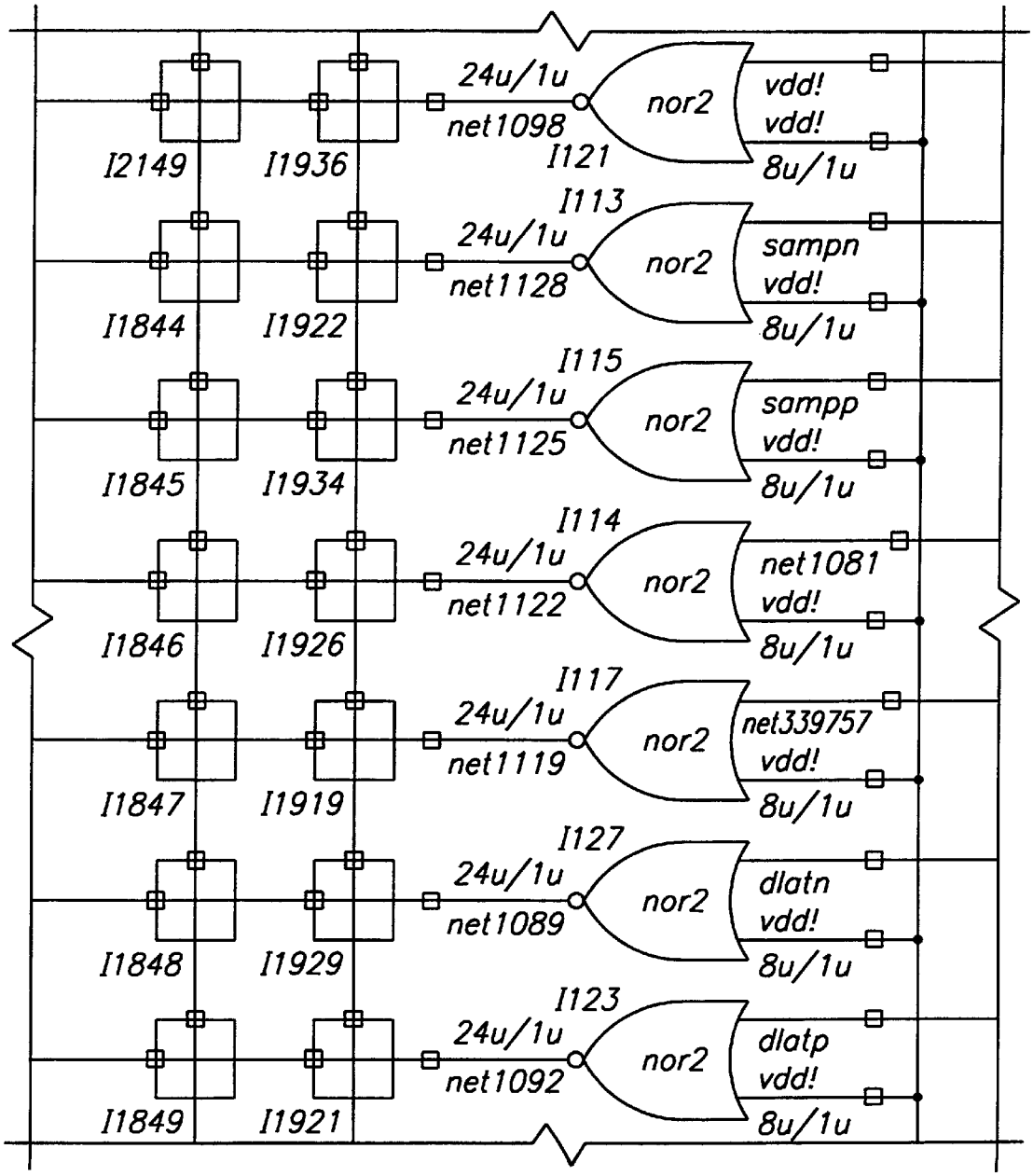
I1781
I1782

Fig 9.0103EL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I121
nor2
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vdd!
8u/1u
I1844
I1922
I113
24u/1u
net1128
nor2
sampn
vdd!
8u/1u
I1845
I1934
I115
24u/1u
net1125
nor2
sampp
vdd!
8u/1u
I1846
I1926
I114
24u/1u
net1122
nor2
net1081
vdd!
8u/1u
I1847
I1919
I117
24u/1u
net1119
nor2
net339757
vdd!
8u/1u
I1848
I1929
I127
24u/1u
net1089
nor2
dlatn
vdd!
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I1849
I1921
I123
24u/1u
net1092
nor2
dlatp
vdd!
8u/1u

Fig 9.0103EM

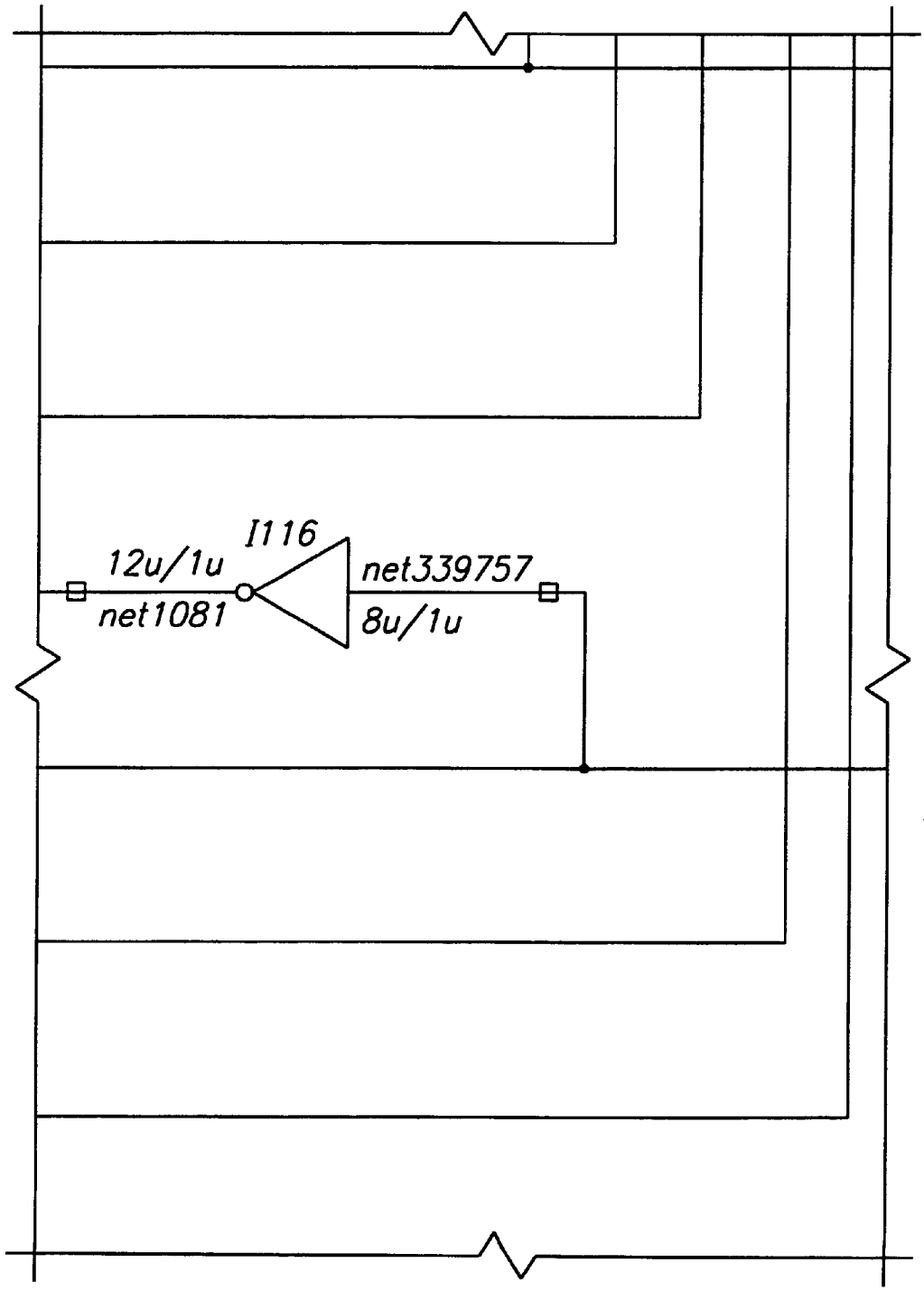


Fig 9.0103EN

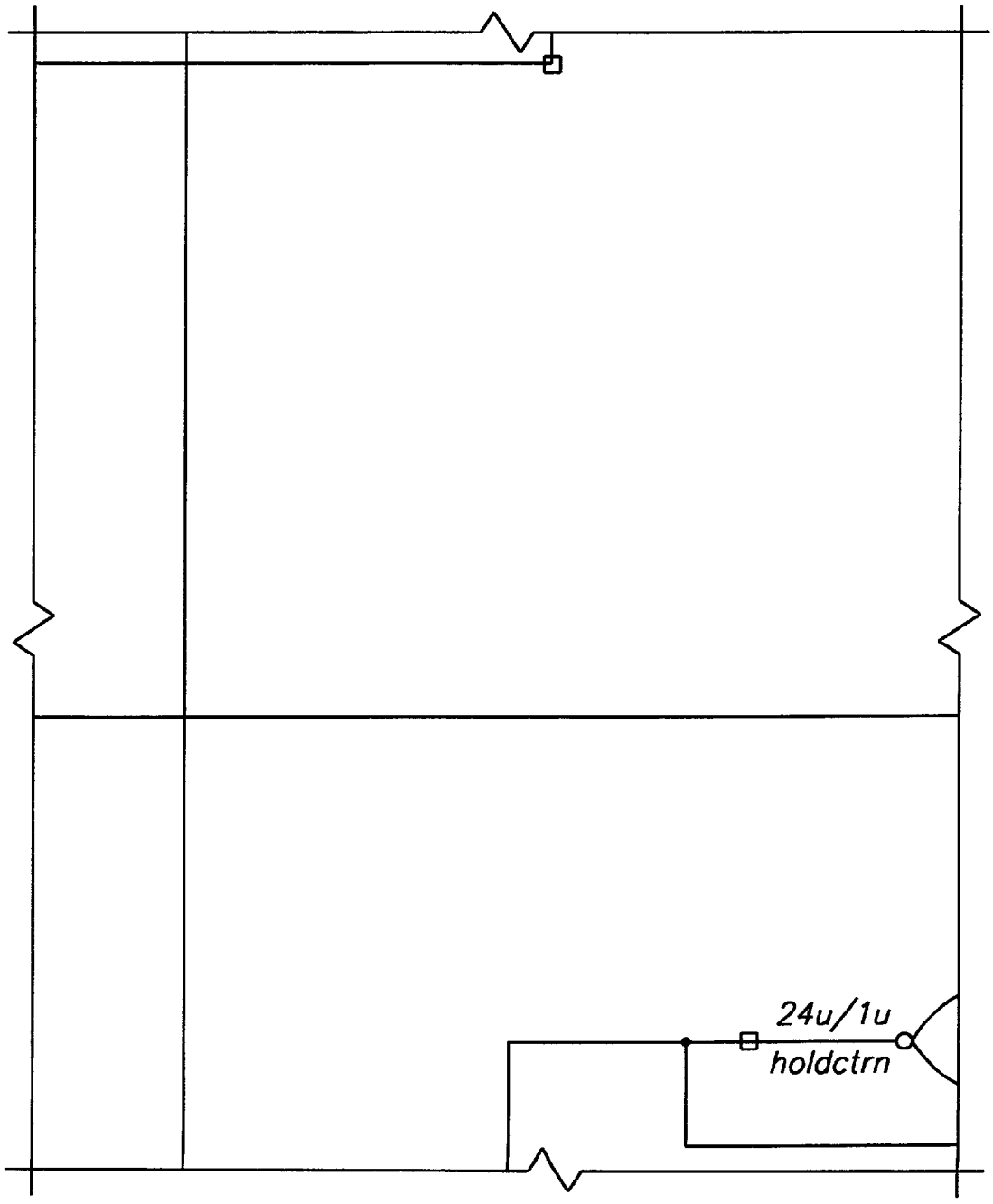


Fig 9.0103E0

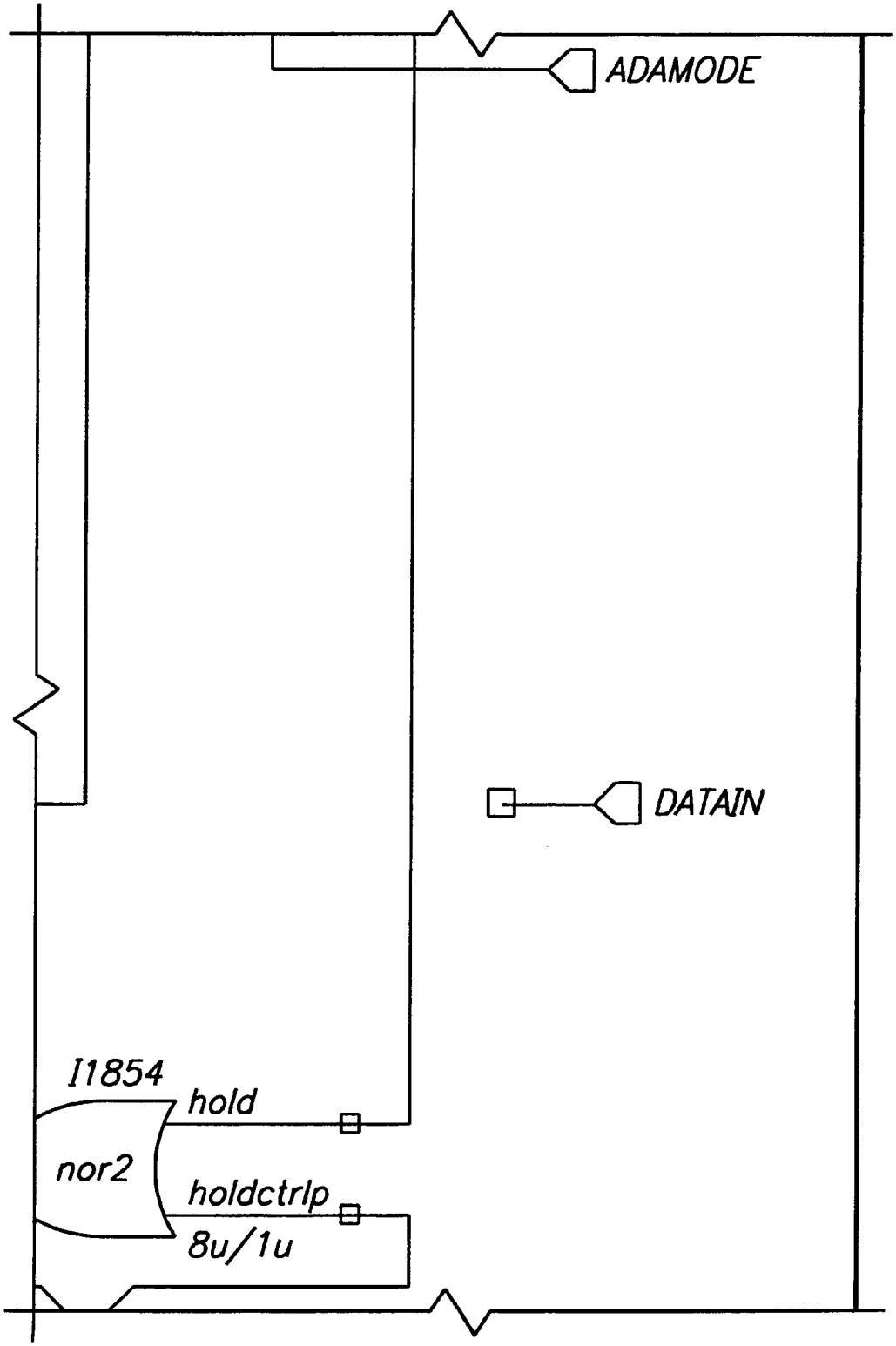
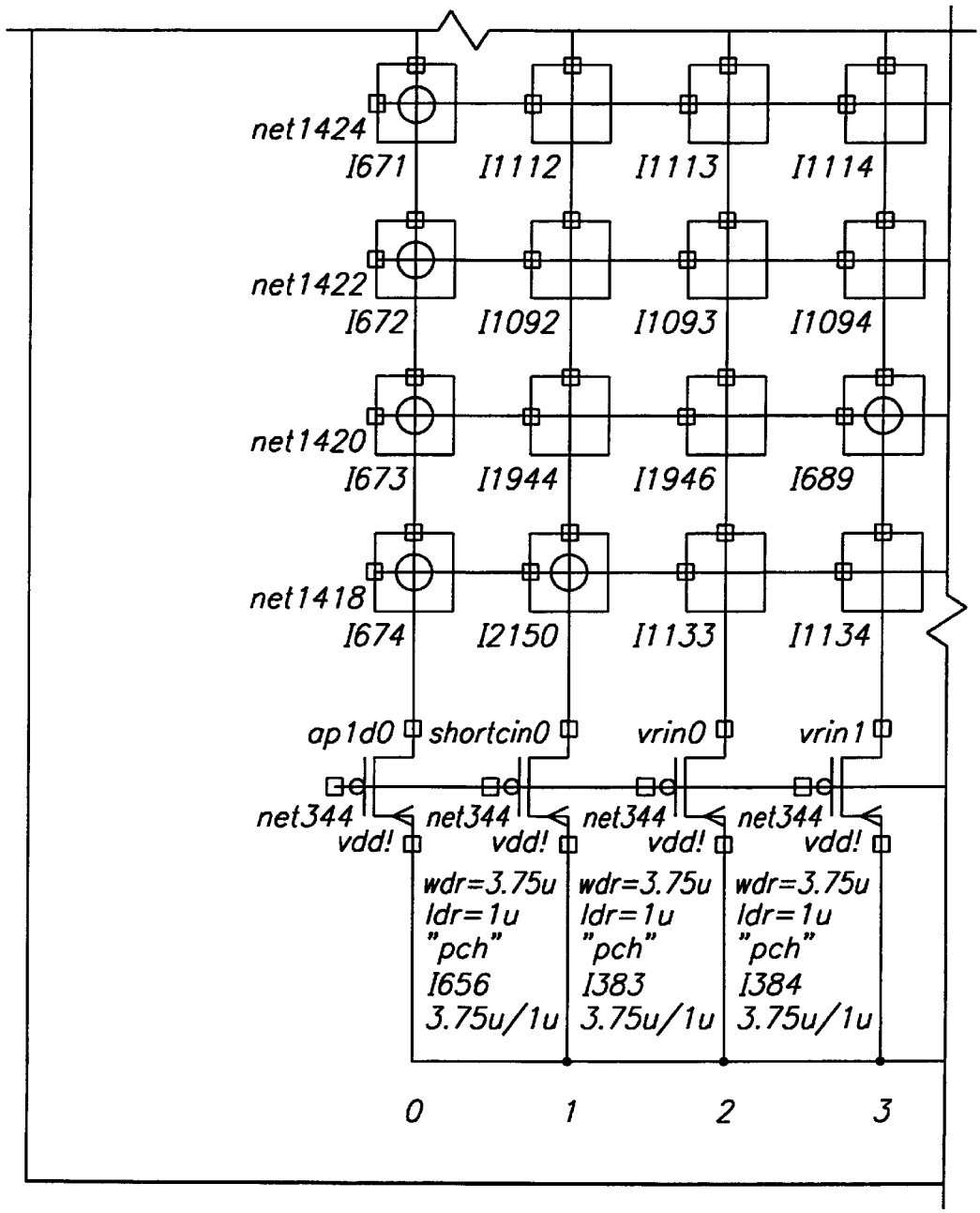


Fig 9.0103EP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net1420
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I1946
I689
net1418
I674
I2150
I1133
I1134
ap1d0
shortcin0
vrin0
vrin1
net344
vdd!
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3.75u/1u
I383
I384
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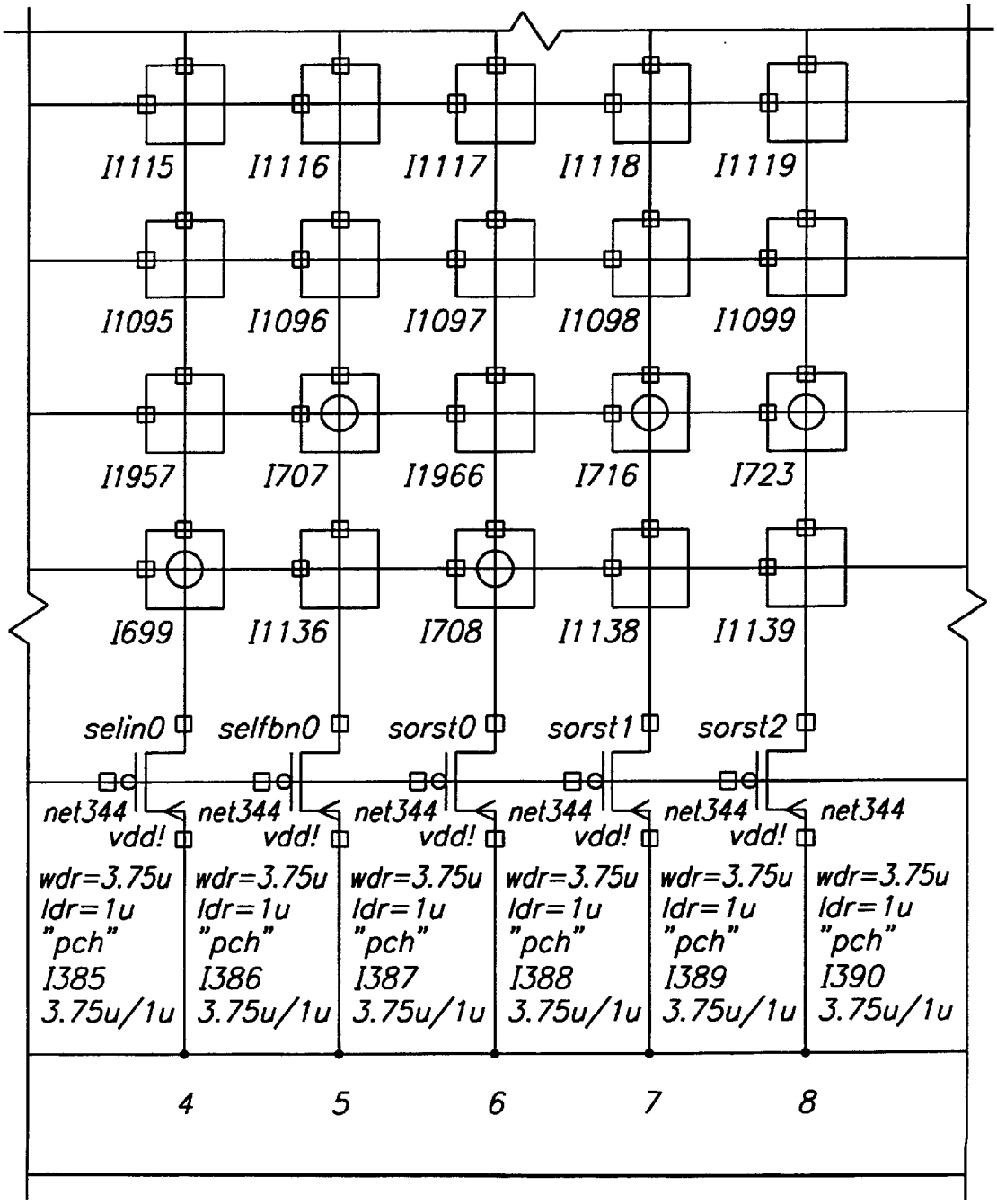
2
3

Fig 9.0103FA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I707
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I716
I723
I699
I1136
I708
I1138
I1139
selin0
selfbn0
sorst0
sorst1
sorst2
net344
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ldr=1u
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3.75u/1u
I386
I387
I388
I389
I390
4
5
6
7
8

Fig 9.0110F/B

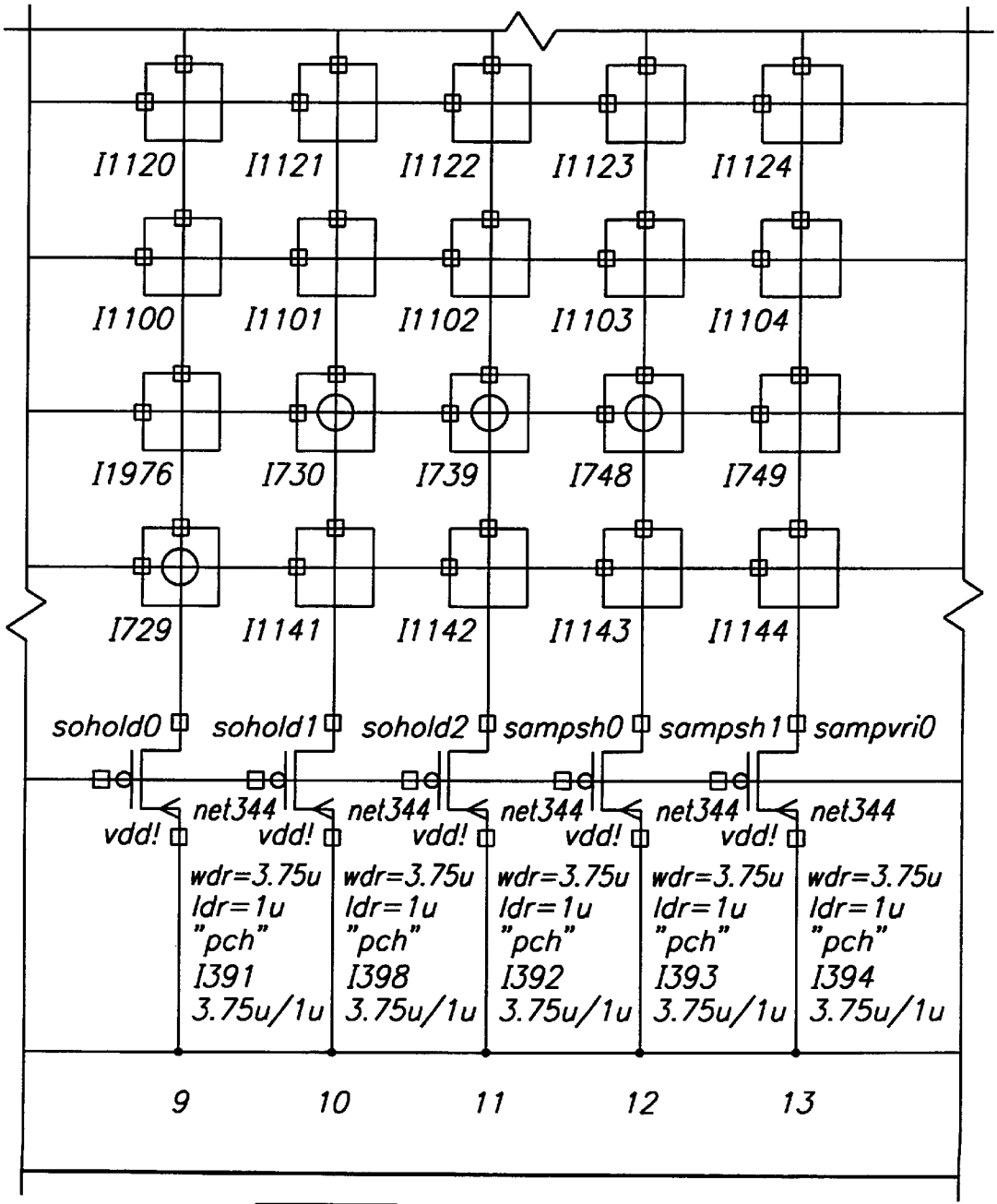

I1120
I1121
I1122
I1123
I1124
I1100
I1101
I1102
I1103
I1104
I1976
I730
I739
I748
I749
I729
I1141
I1142
I1143
I1144
sohold0
sohold1
sohold2
sampsh0
sampsh1
sampvri0
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I391
3.75u/1u
I398
I392
I393
I394
9
10
11
12
13

Fig 9.0110FC

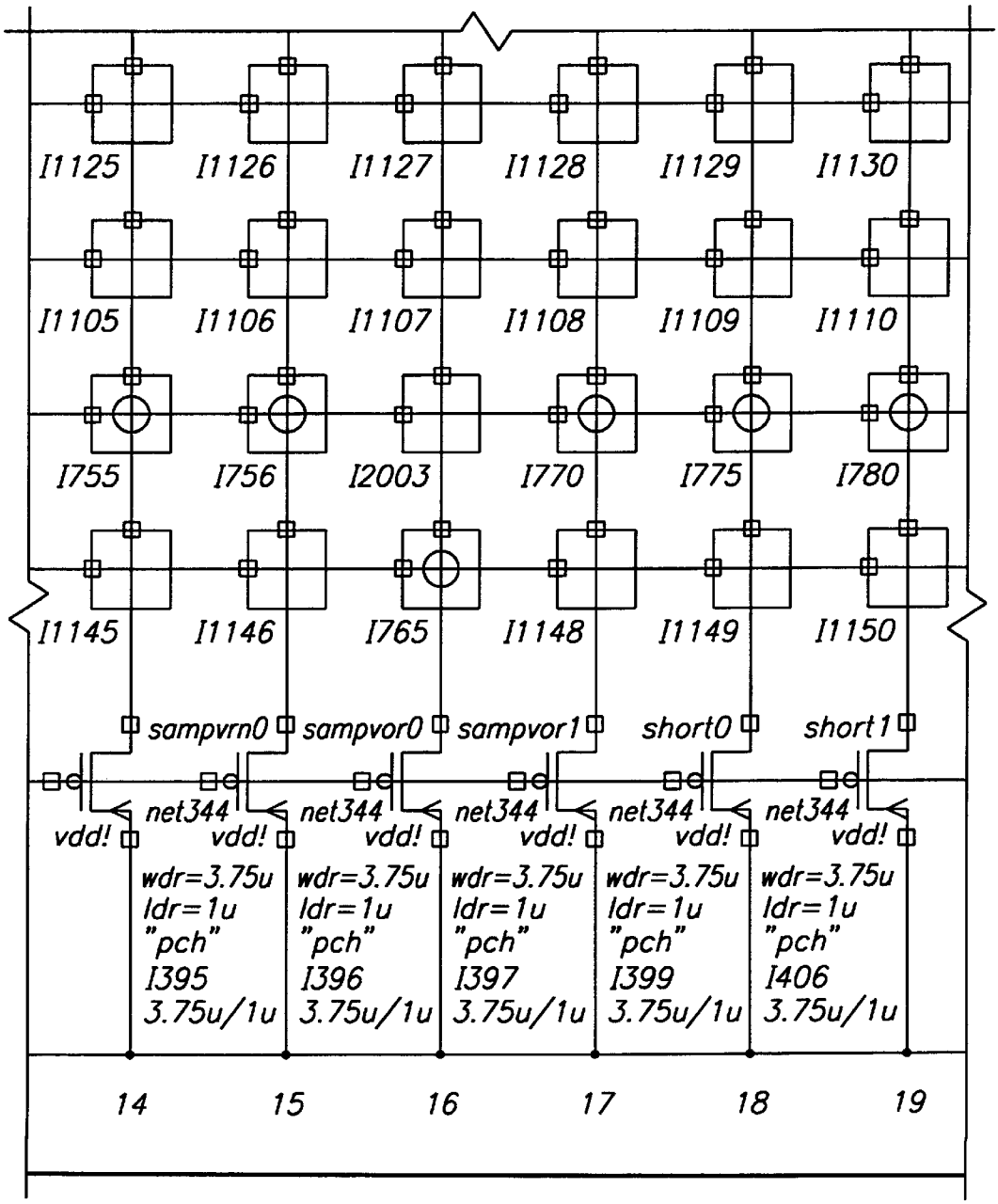

I1125
I1126
I1127
I1128
I1129
I1130
I1105
I1106
I1107
I1108
I1109
I1110
I755
I756
I2003
I770
I775
I780
I1145
I1146
I765
I1148
I1149
I1150
sampvrn0
sampvor0
sampvor1
short0
short1
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I395
3.75u/1u
I396
I397
I399
I406
14
15
16
17
18
19

Fig 9.0103FD

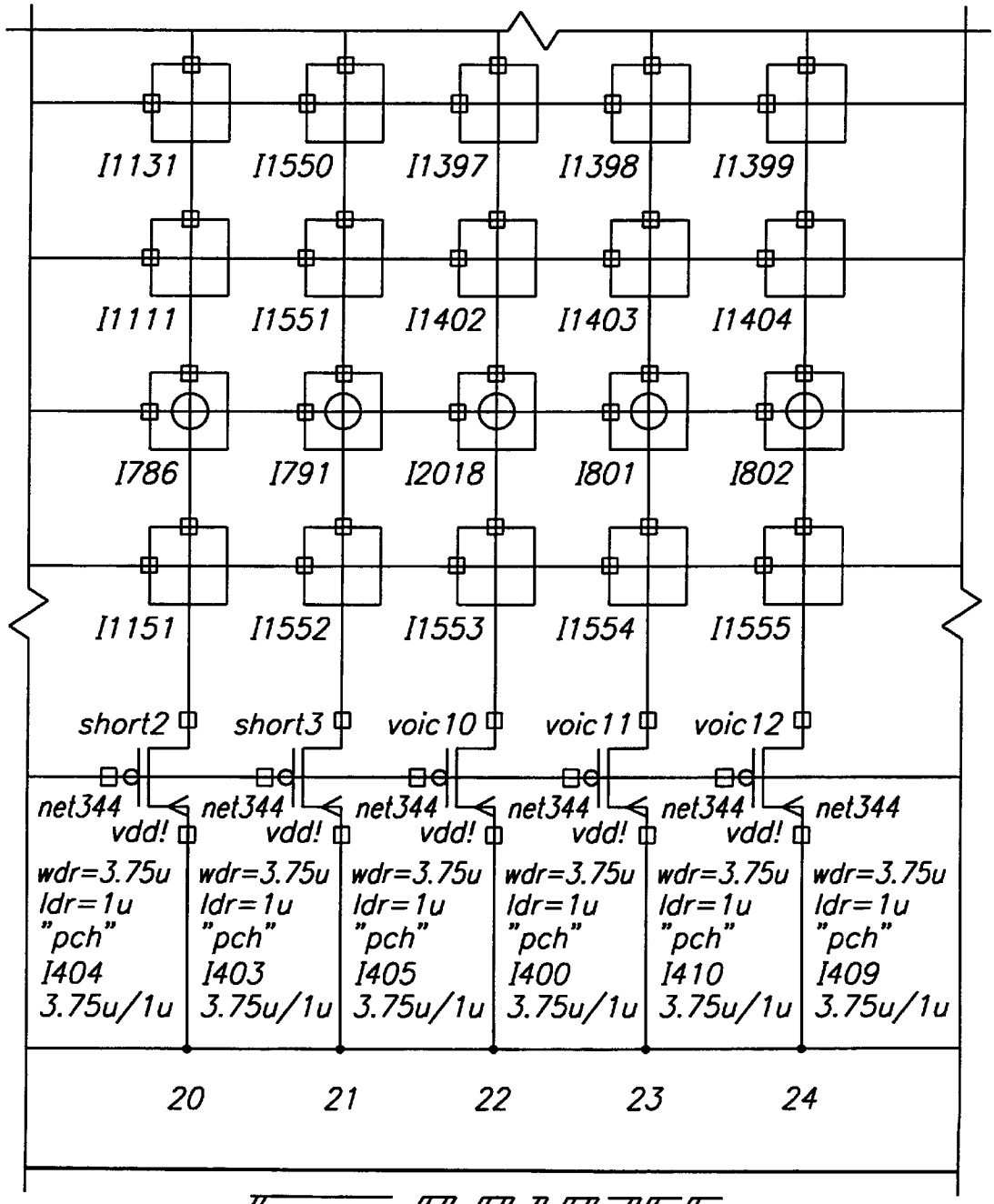

I1131
I1550
I1397
I1398
I1399
I1111
I1551
I1402
I1403
I1404
I786
I791
I2018
I801
I802
I1151
I1552
I1553
I1554
I1555
short2
short3
voic10
voic11
voic12
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I404
3.75u/1u
I403
I405
I400
I410
I409
20
21
22
23
24

Fig 9.0103E

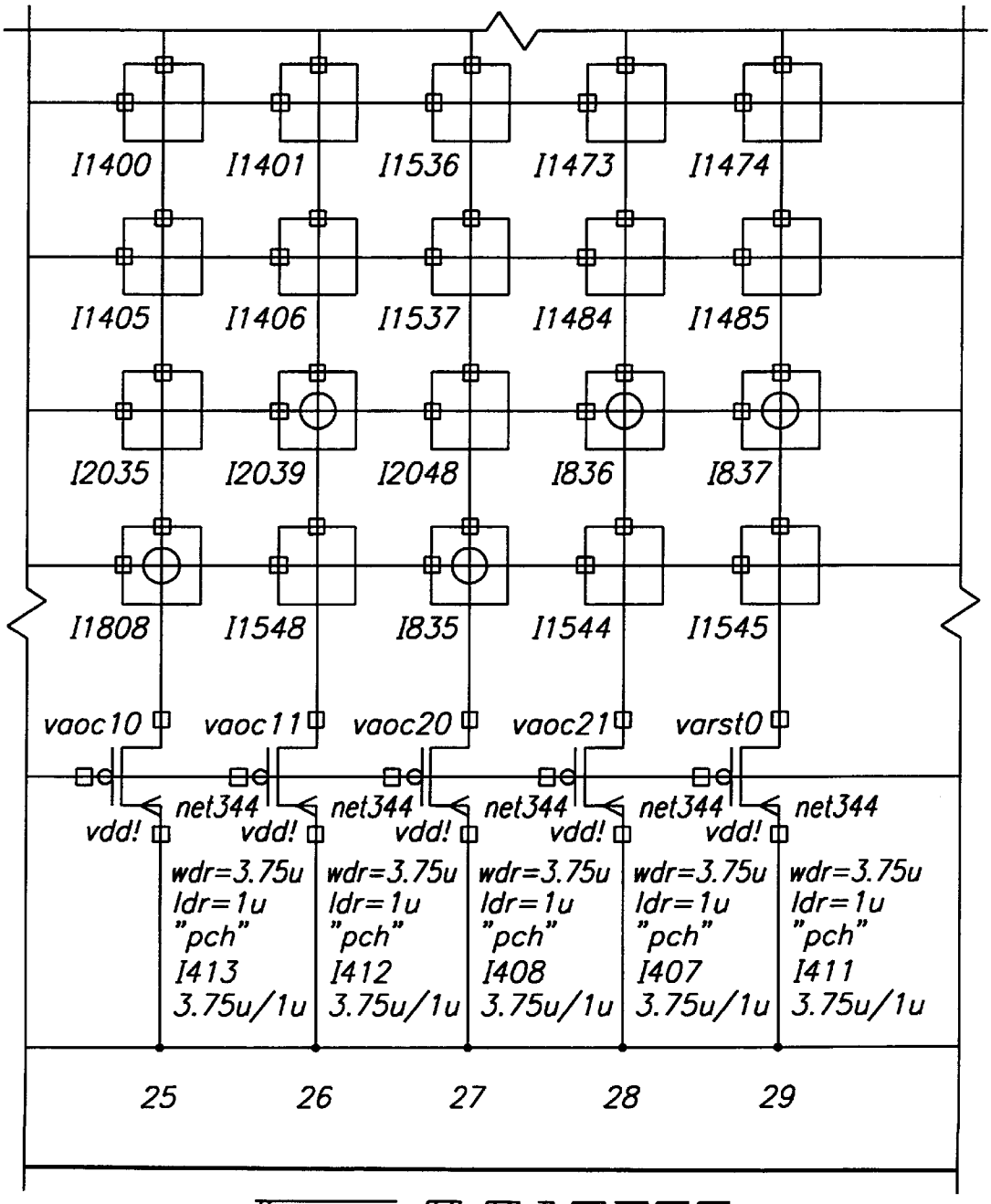

I1400
I1401
I1536
I1473
I1474
I1405
I1406
I1537
I1484
I1485
I2035
I2039
I2048
I836
I837
I1808
I1548
I835
I1544
I1545
vaoc10
vaoc11
vaoc20
vaoc21
varst0
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I413
3.75u/1u
I412
I408
I407
I411
25
26
27
28
29

Fig 9.0110F

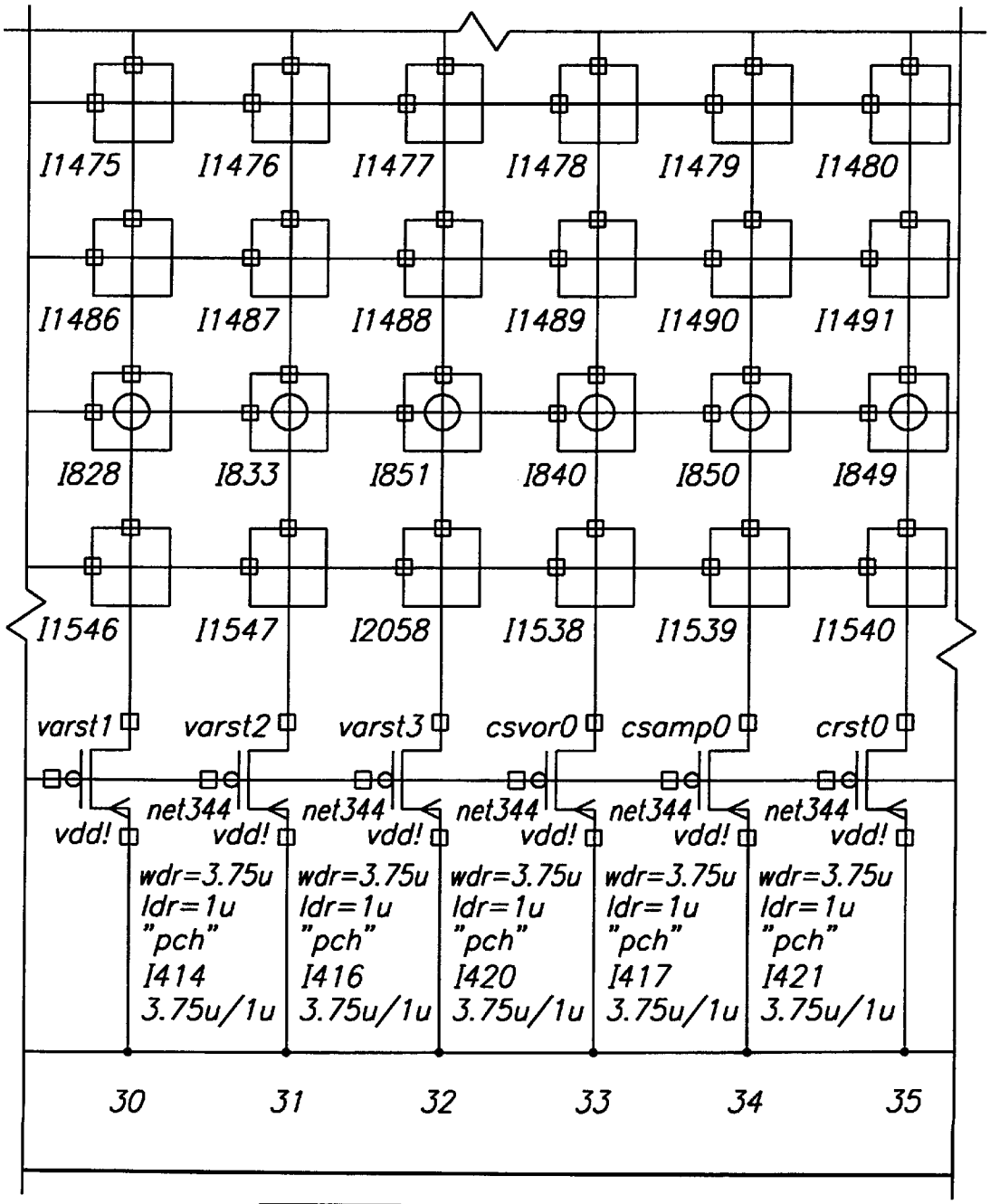

I1475
I1476
I1477
I1478
I1479
I1480
I1486
I1487
I1488
I1489
I1490
I1491
I828
I833
I851
I840
I850
I849
I1546
I1547
I2058
I1538
I1539
I1540
varst1
varst2
varst3
csvor0
csamp0
crst0
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I414
3.75u/1u
I416
I420
I417
I421
30
31
32
33
34
35

Fig 9.0103F6

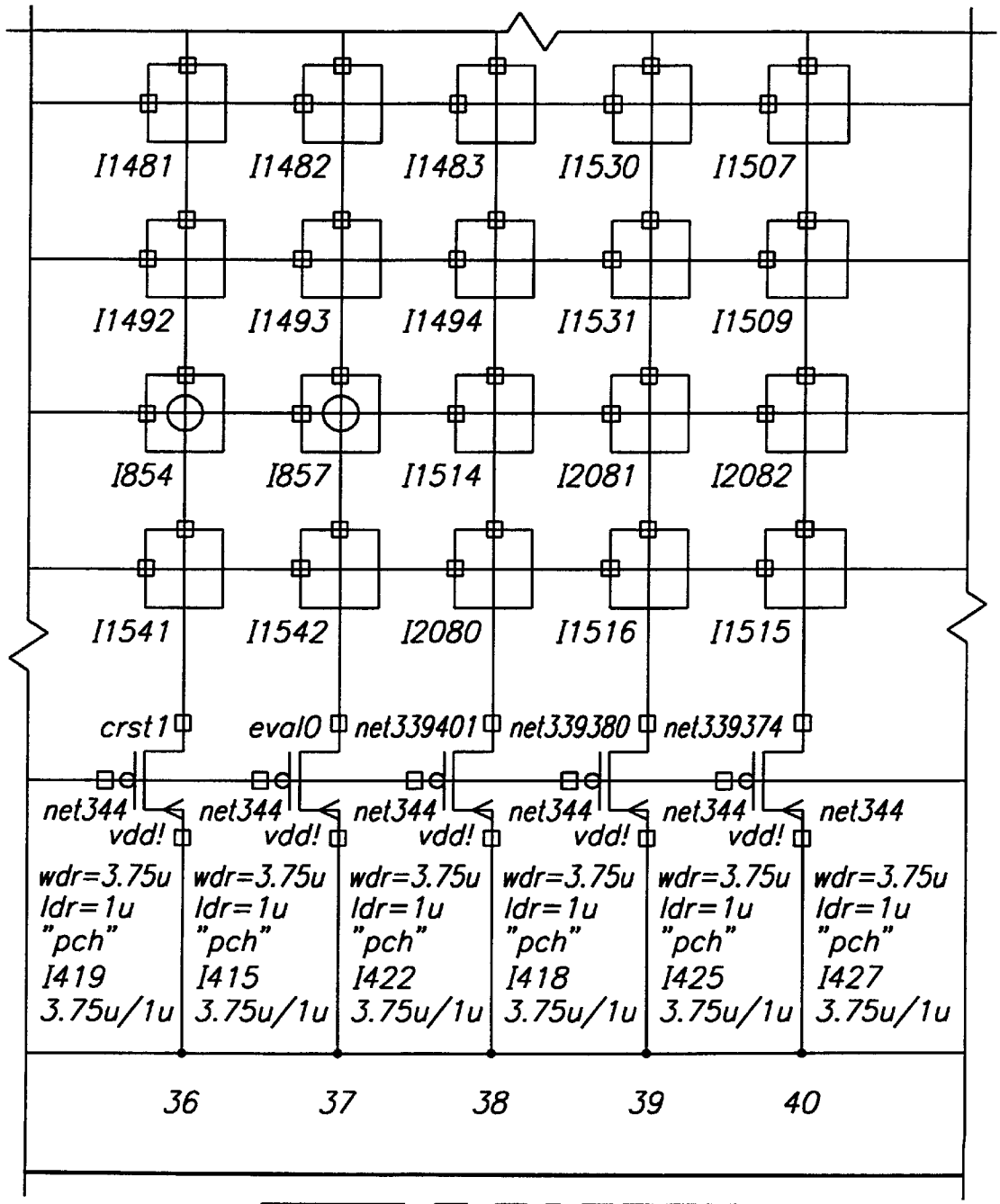

I1481
I1482
I1483
I1530
I1507
I1492
I1493
I1494
I1531
I1509
I854
I857
I1514
I2081
I2082
I1541
I1542
I2080
I1516
I1515
crst1
eval0
net339401
net339380
net339374
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I419
3.75u/1u
I415
I422
I418
I425
I427
36
37
38
39
40

Fig 9.0130FH

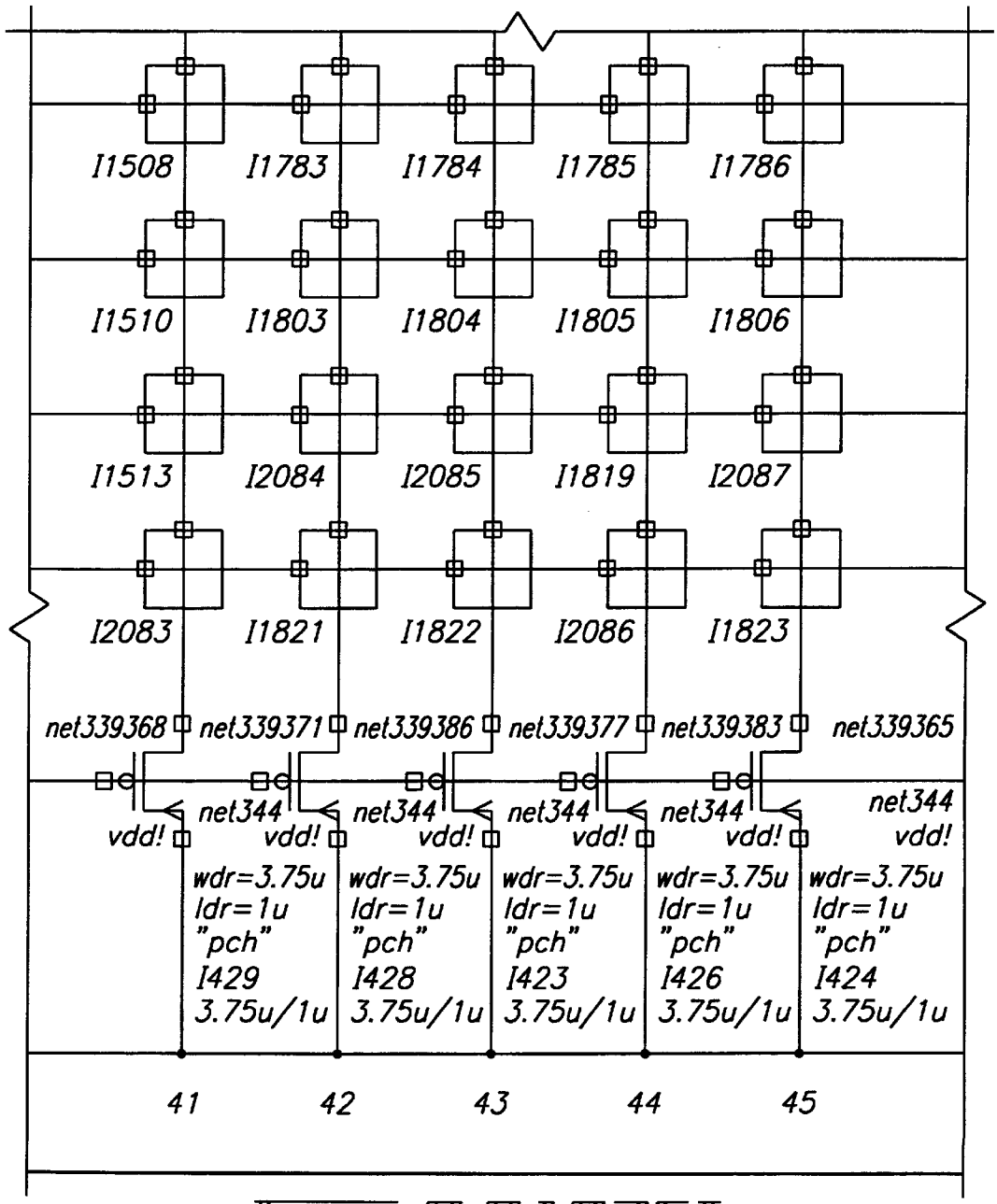


Fig 9.00130F II

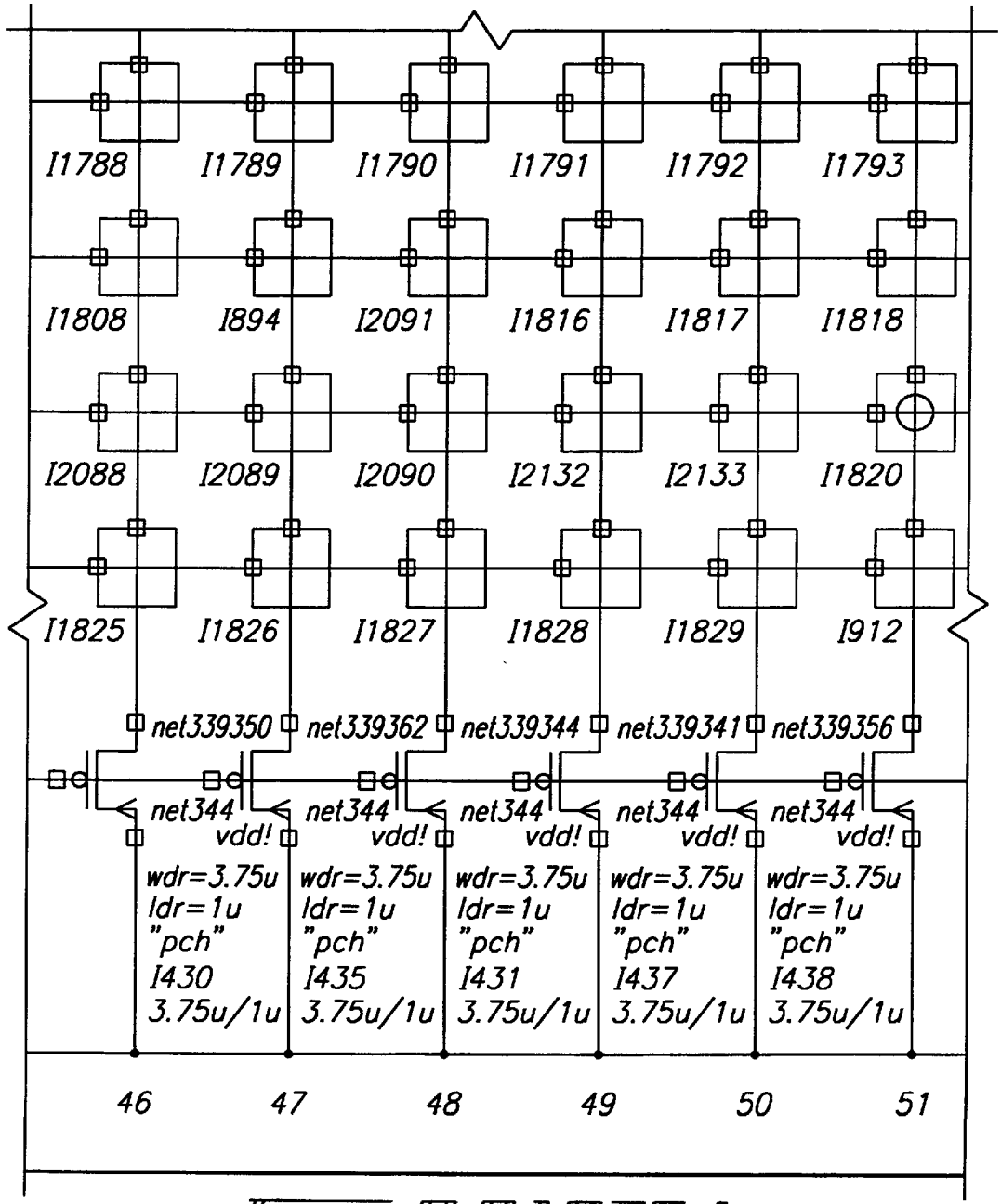

I1788
I1789
I1790
I1791
I1792
I1793
I1808
I894
I2091
I1816
I1817
I1818
I2088
I2089
I2090
I2132
I2133
I1820
I1825
I1826
I1827
I1828
I1829
I912
net339350
net339362
net339344
net339341
net339356
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I430
3.75u/1u
I435
I431
I437
I438
46
47
48
49
50
51

Fig 9.0103Fa

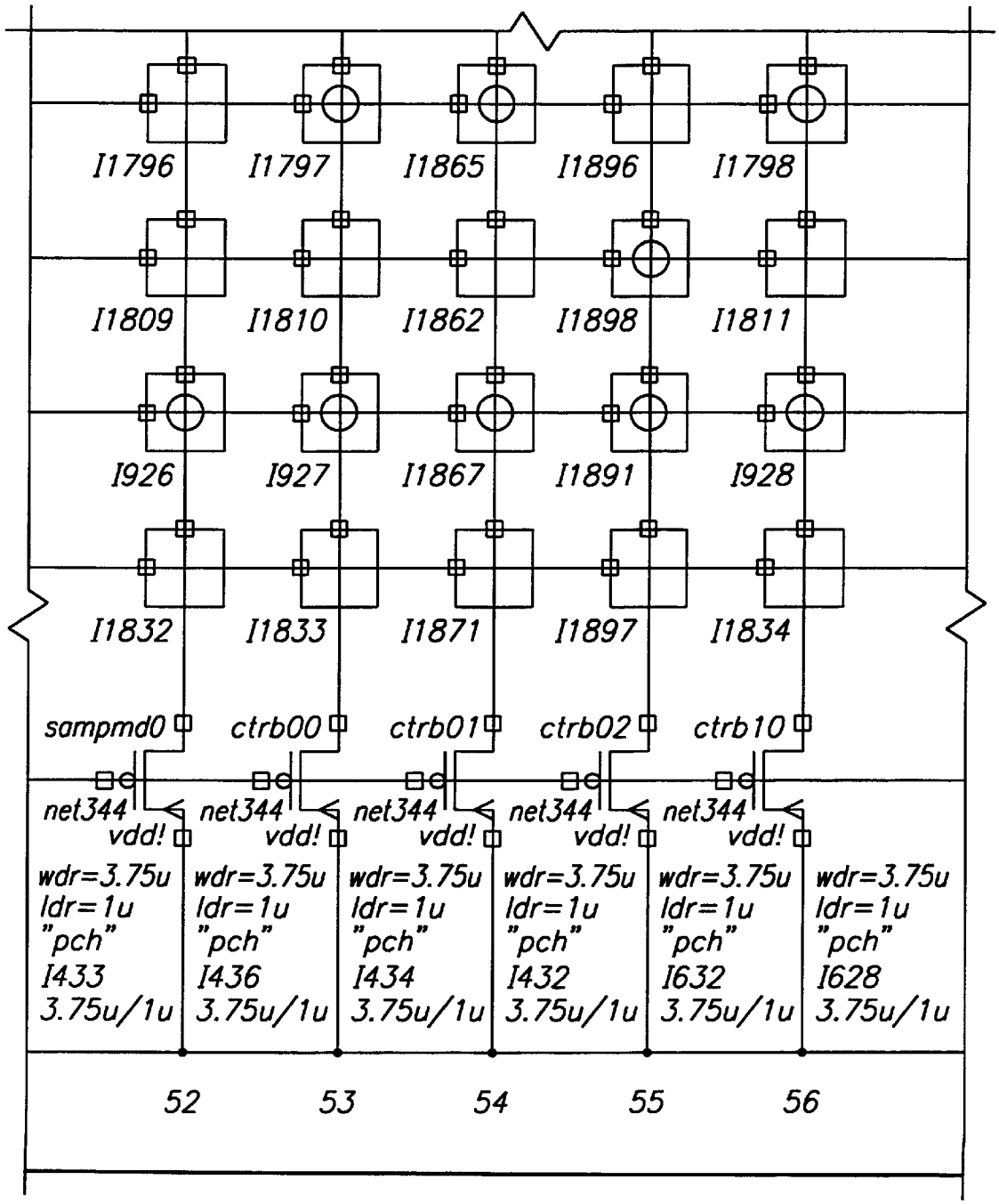

I1796
I1797
I1865
I1896
I1798
I1809
I1810
I1862
I1898
I1811
I926
I927
I1867
I1891
I928
I1832
I1833
I1871
I1897
I1834
sampmd0
ctrb00
ctrb01
ctrb02
ctrb10
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I433
3.75u/1u
I436
I434
I432
I632
I628
52
53
54
55
56

Fig 9.0103FK

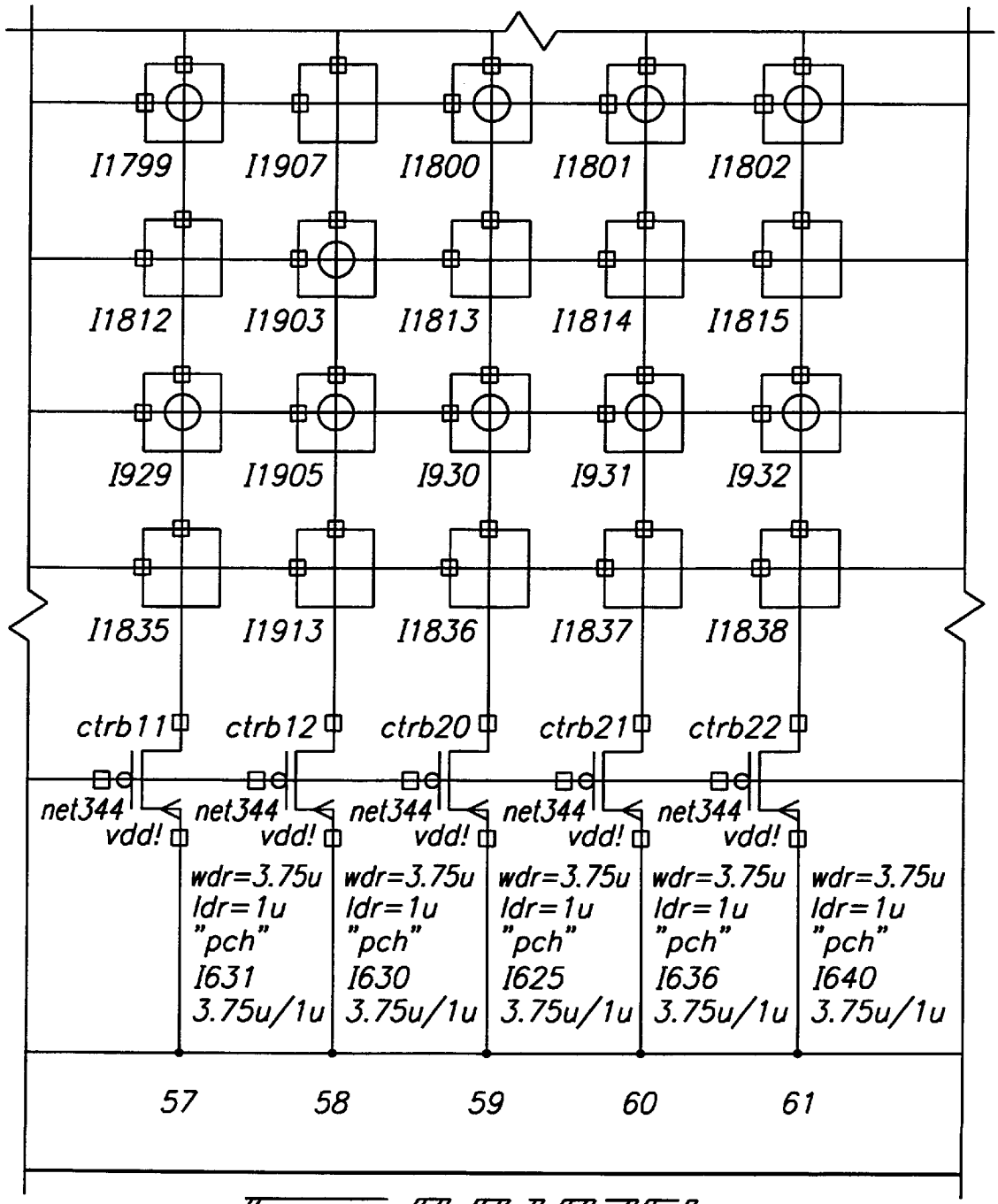

I1799
I1907
I1800
I1801
I1802
I1812
I1903
I1813
I1814
I1815
I929
I1905
I930
I931
I932
I1835
I1913
I1836
I1837
I1838
ctrb11
ctrb12
ctrb20
ctrb21
ctrb22
net344
vdd!
wdr=3.75u
ldr=1u
"pch"
I631
3.75u/1u
I630
I625
I636
I640
57
58
59
60
61

Fig 9.0103fL

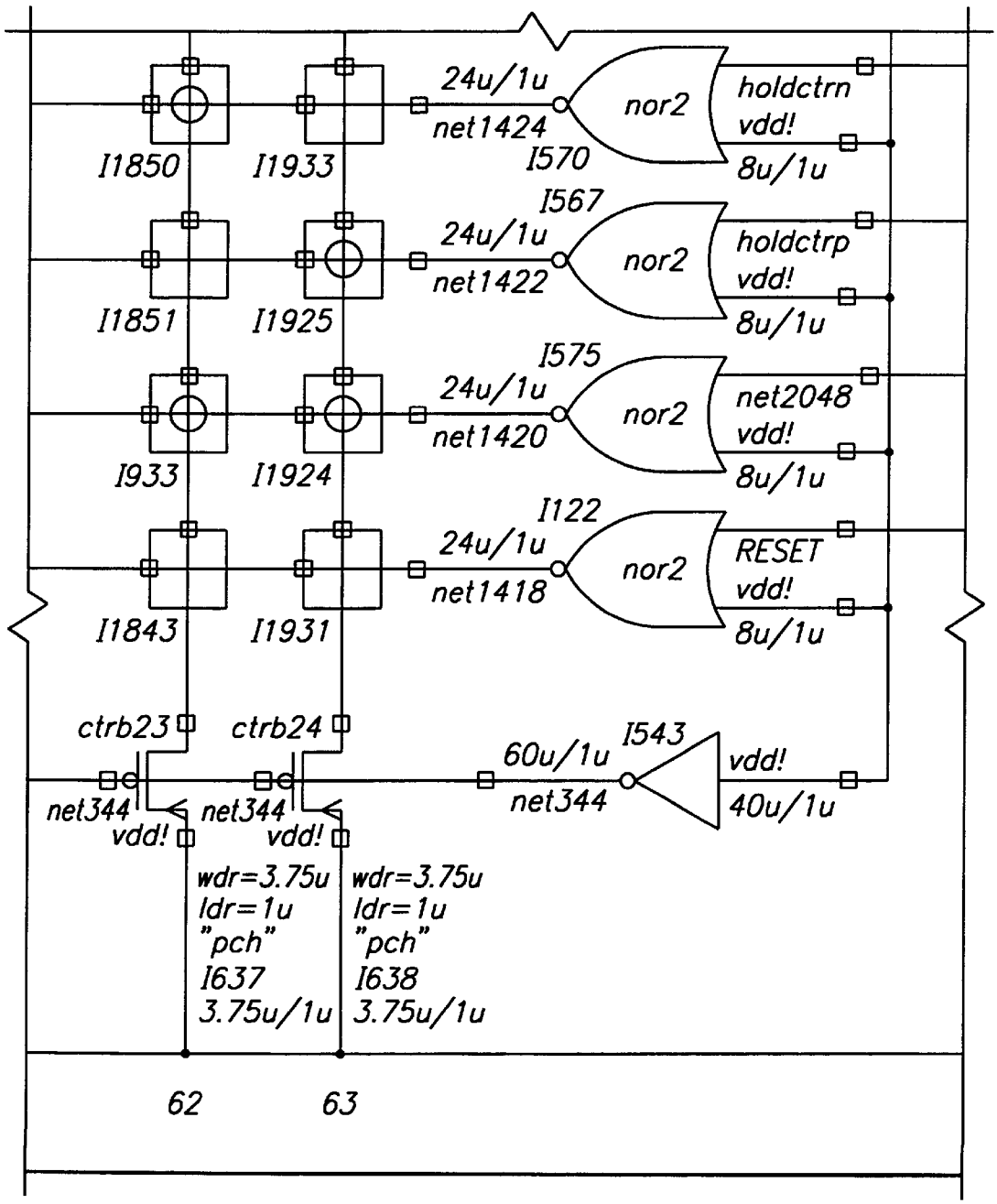

I1850
I1933
24u/1u
net1424
nor2
I570
holdctrn
vdd!
8u/1u
I567
I1851
I1925
24u/1u
net1422
nor2
holdctrp
vdd!
8u/1u
I575
I933
I1924
24u/1u
net1420
nor2
net2048
vdd!
8u/1u
I122
I1843
I1931
24u/1u
net1418
nor2
RESET
vdd!
8u/1u
ctrb23
ctrb24
net344
vdd!
net344
vdd!
60u/1u
net344
I543
vdd!
40u/1u
wdr=3.75u
ldr=1u
"pch"
I637
3.75u/1u
wdr=3.75u
ldr=1u
"pch"
I638
3.75u/1u
62
63

Fig 9.0103FM

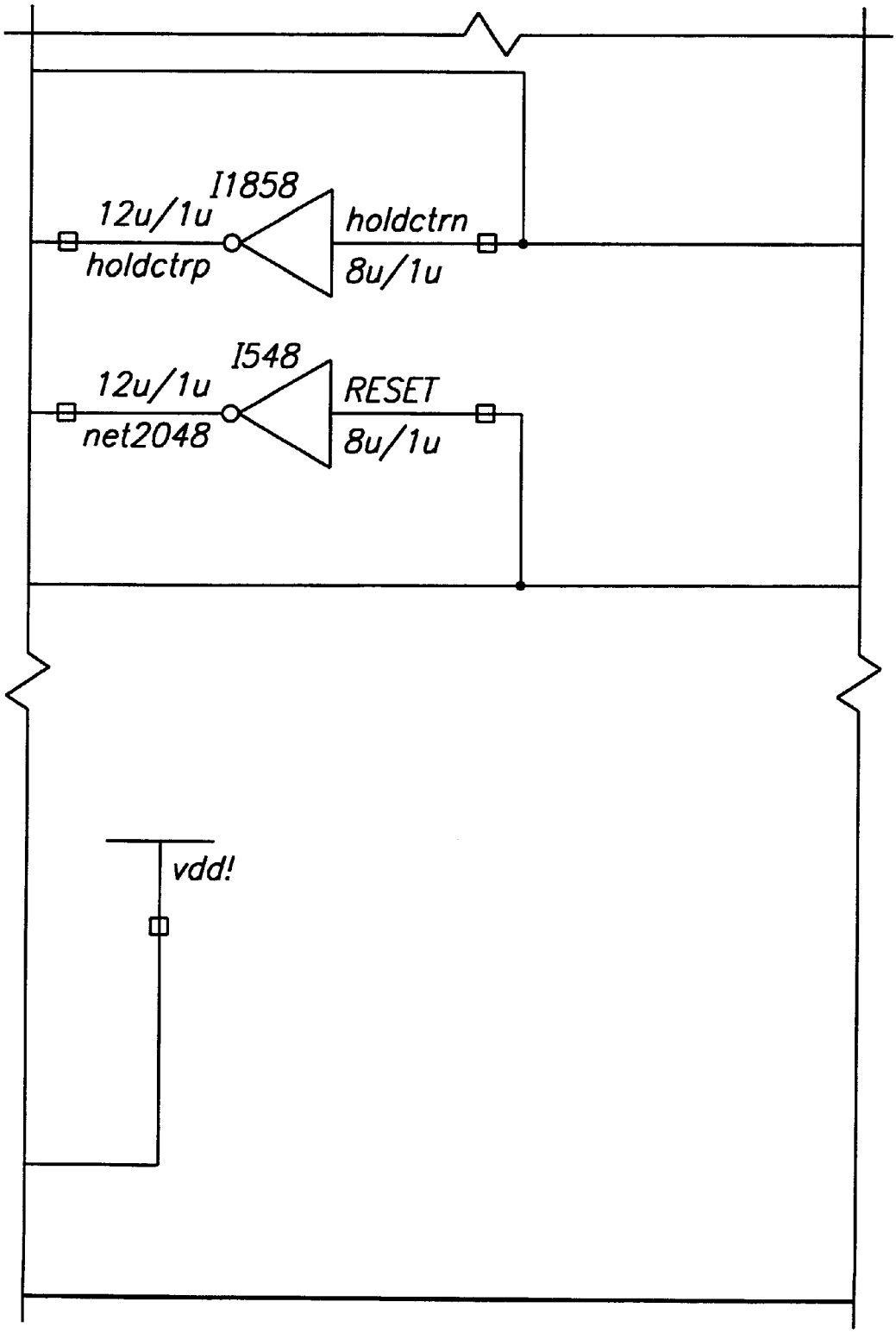

I1858
12u/1u
holdctrp
holdctrn
8u/1u
I548
12u/1u
net2048
RESET
8u/1u
vdd!

FIG 9.0103FN

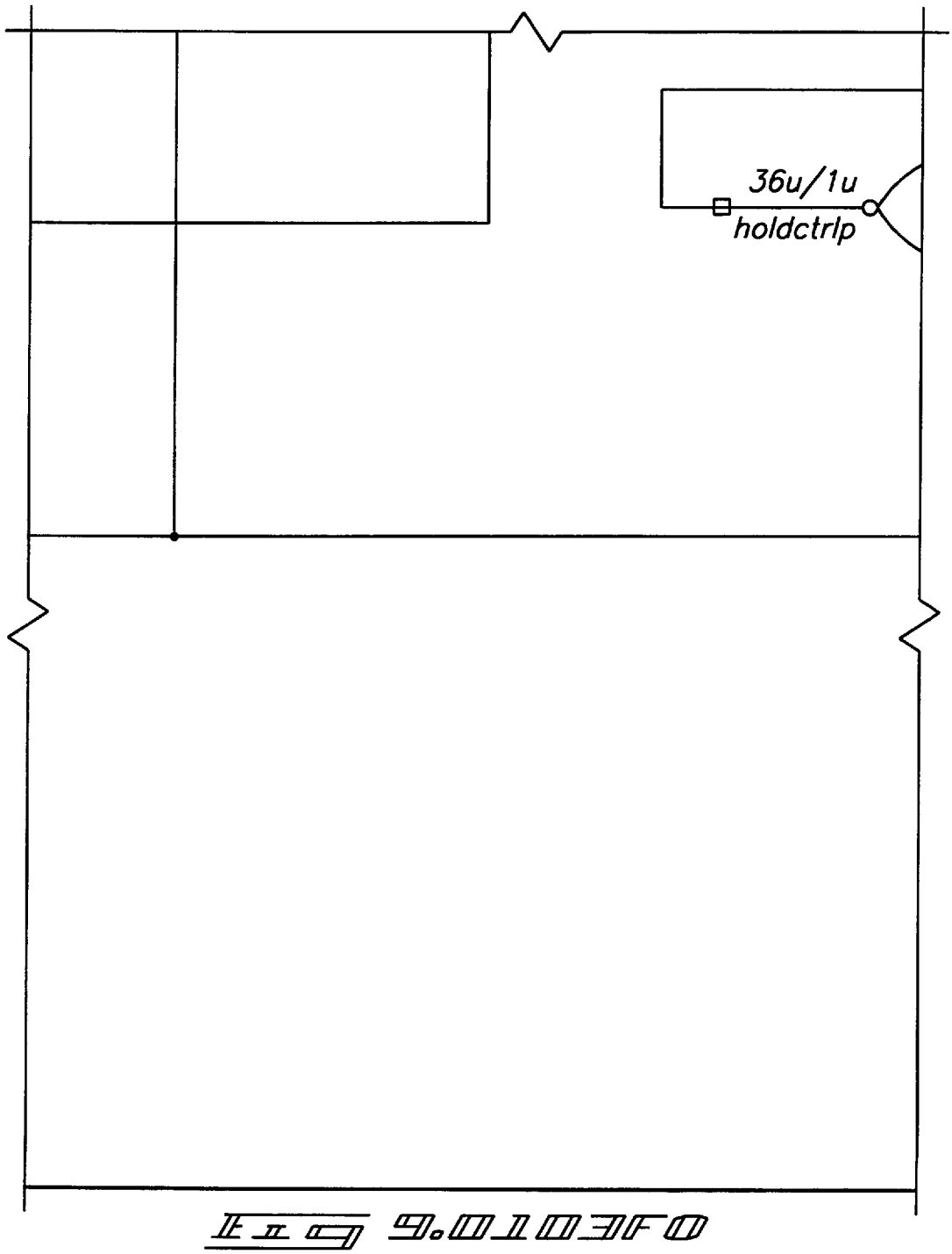


Fig 9.0103F0

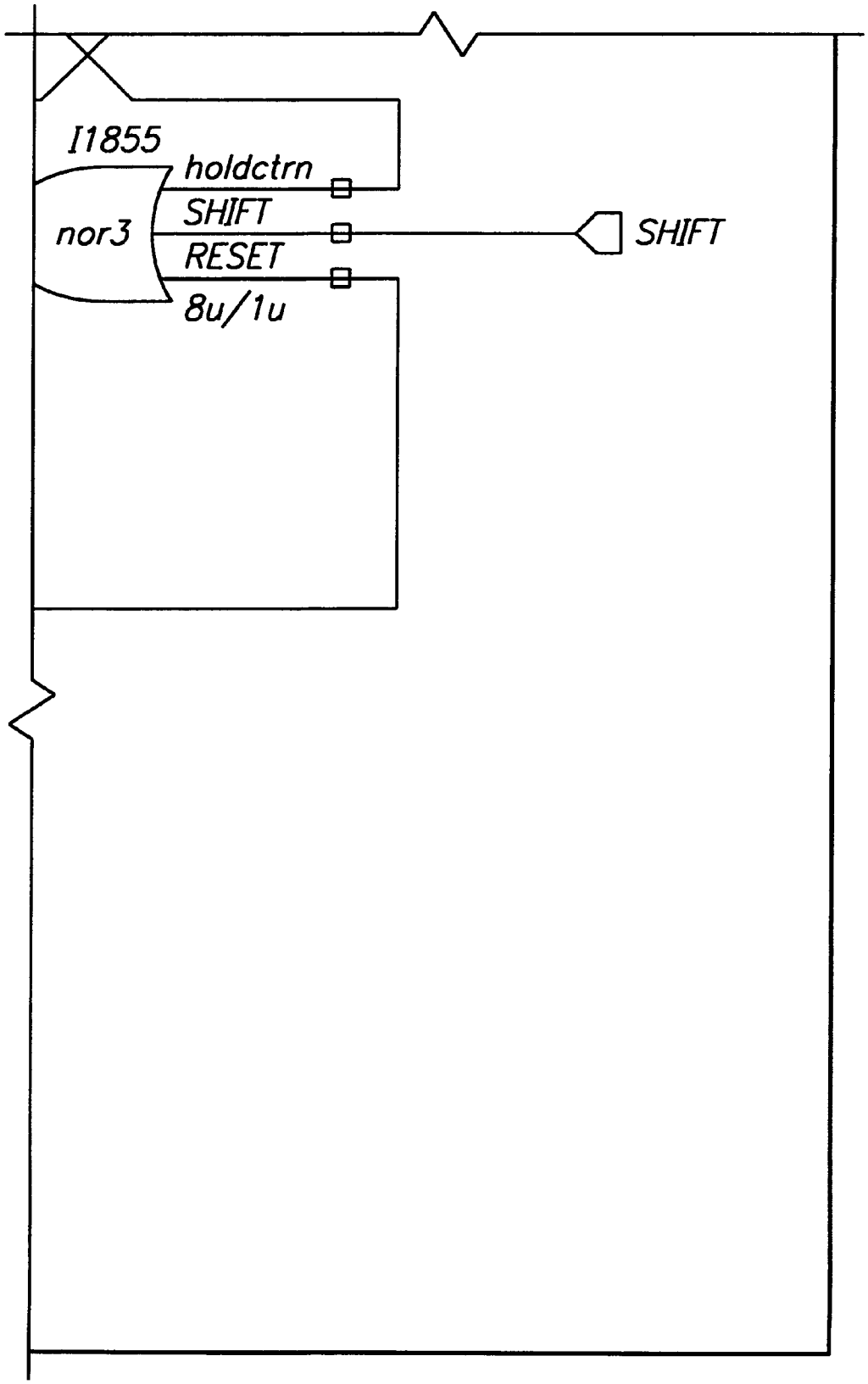


Fig 9.0103F

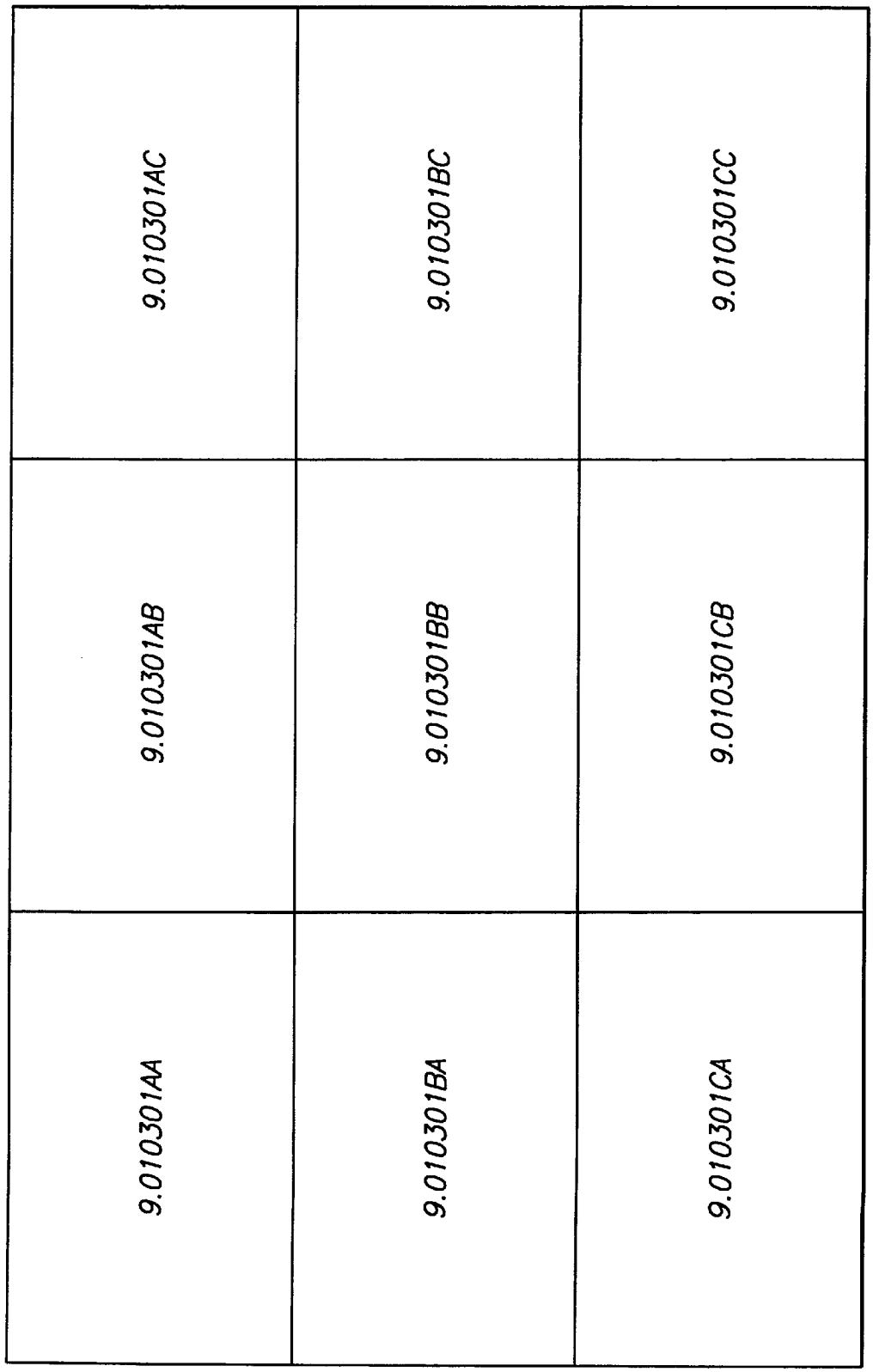

9.010301AC
9.010301BC
9.010301CC
9.010301AB
9.010301BB
9.010301CB
9.010301AA
9.010301BA
9.010301CA

FIG 9.0010.0

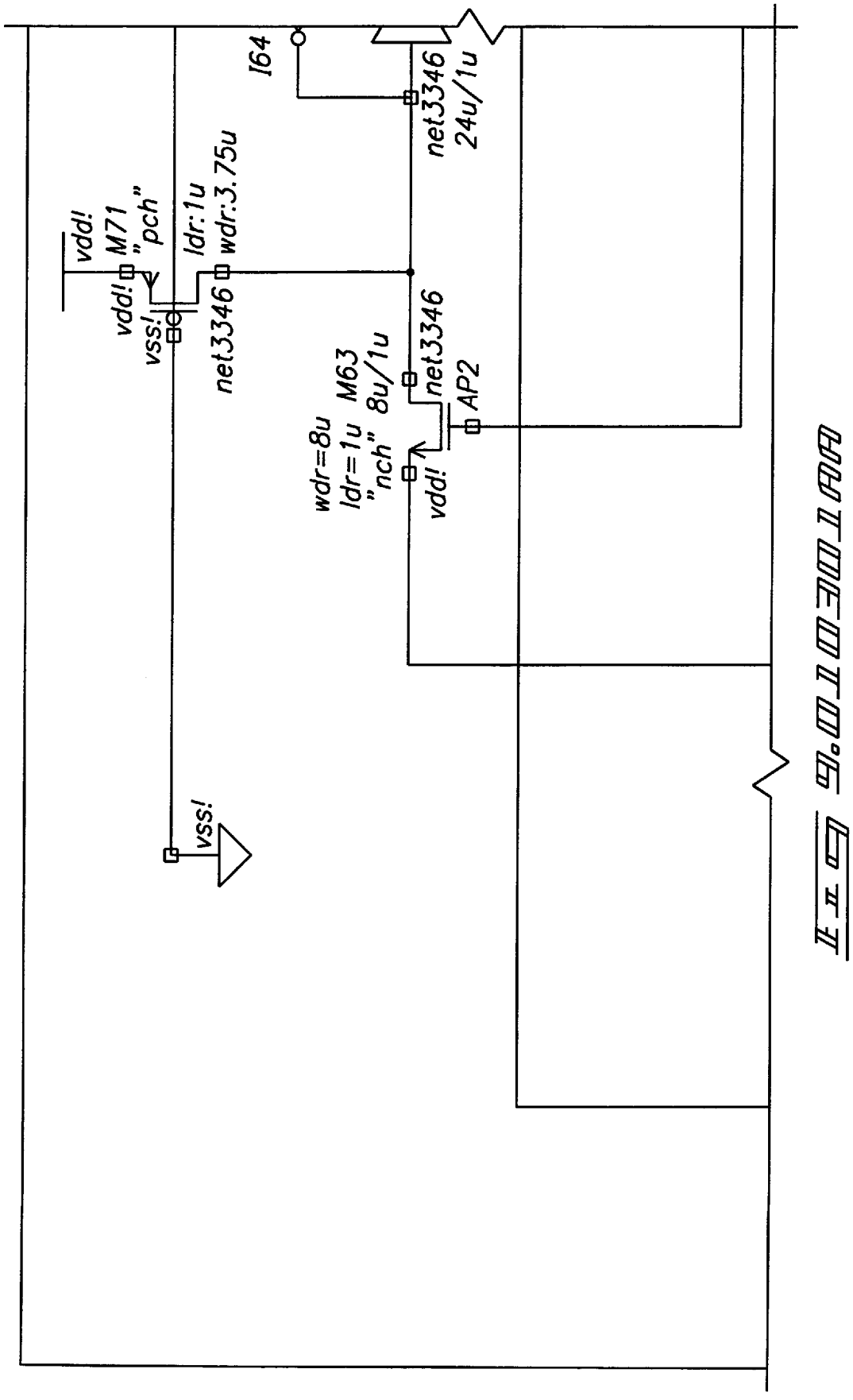

I64
net3346
24u/1u
vdd!
M71
"pch"
ldr:1u
wdr:3.75u
vss!
net3346
wdr=8u
ldr=1u
"nch"
M63
8u/1u
net3346
AP2
vdd!
vss!

FIG 96

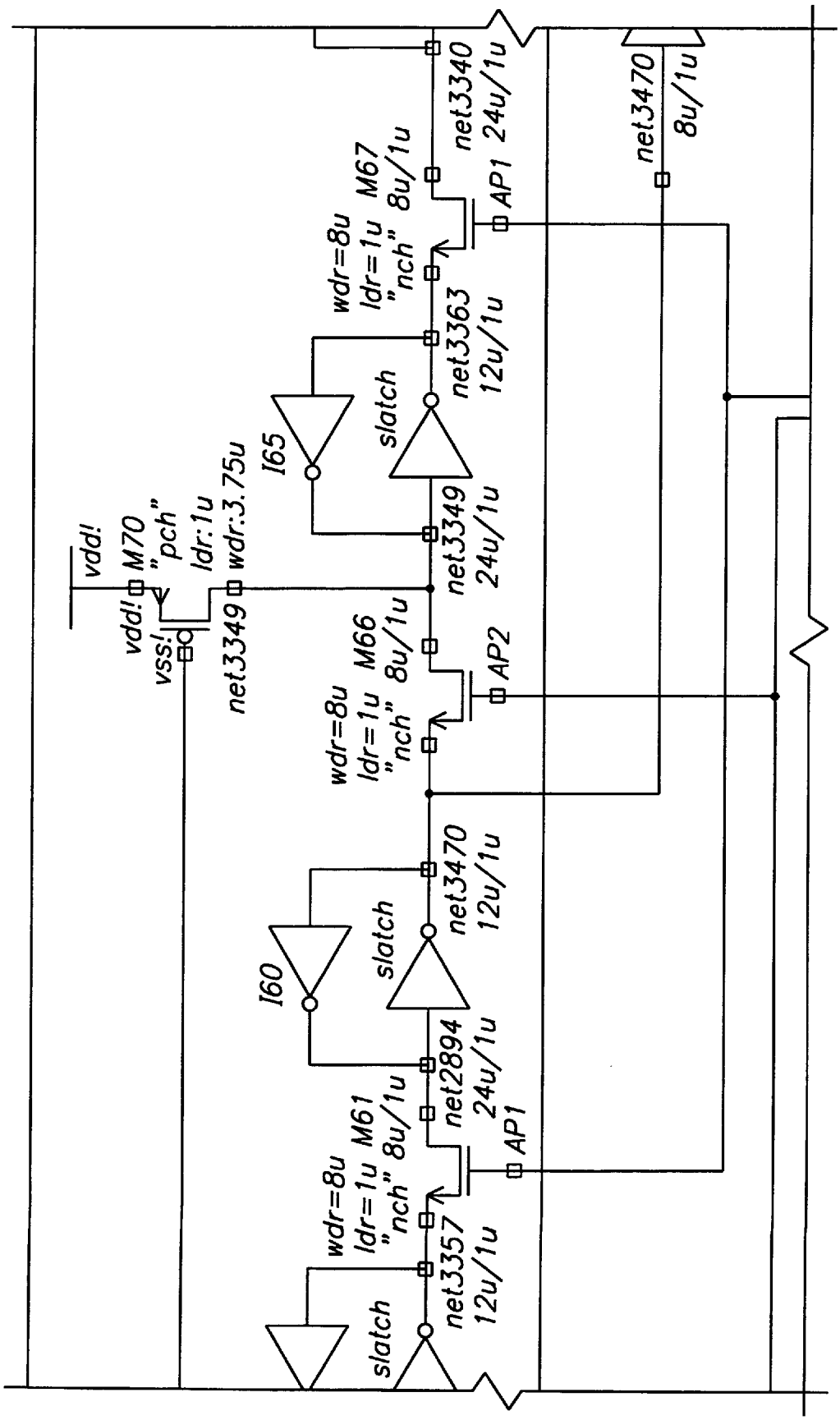
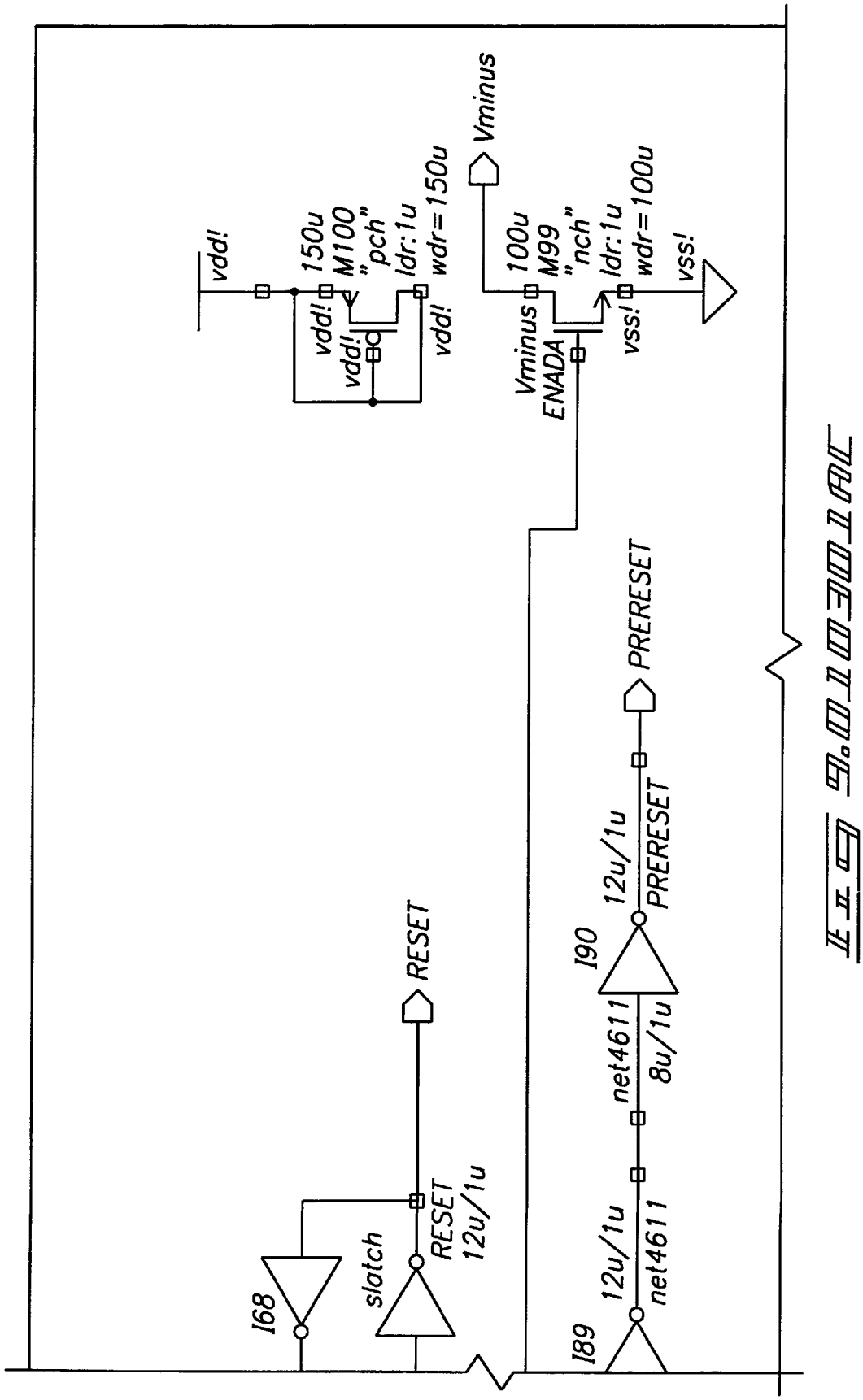


FIG. 9.00100300 IAB


vdd!
150u
M100
"pch"
ldr:1u
wdr=150u
vdd!
vdd!
vdd!
Vminus
100u
M99
"nch"
ldr:1u
wdr=100u
vss!
vss!
Vminus
ENADA
PRERESET
12u/1u
PRERESET
I90
net4611
8u/1u
net4611
12u/1u
I89
RESET
RESET
12u/1u
slatch
I68
FIG 6.0.0.1.0.0.0

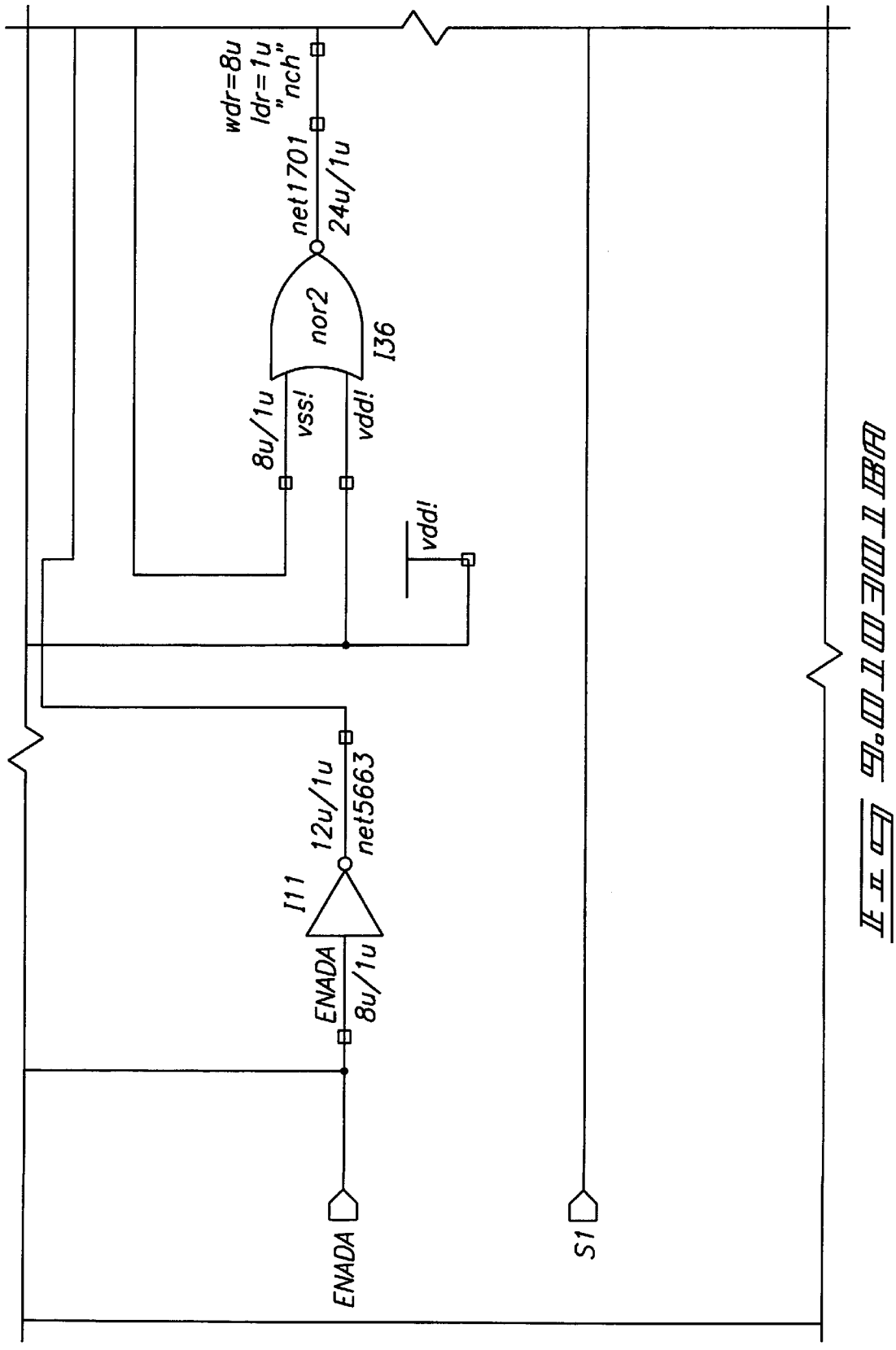

wdr=8u
ldr=1u
"nch"
net1701
24u/1u
nor2
I36
8u/1u
vss!
vdd!
vdd!
12u/1u
net5663
I11
ENADA
8u/1u
ENADA
S1

FIG 95.00

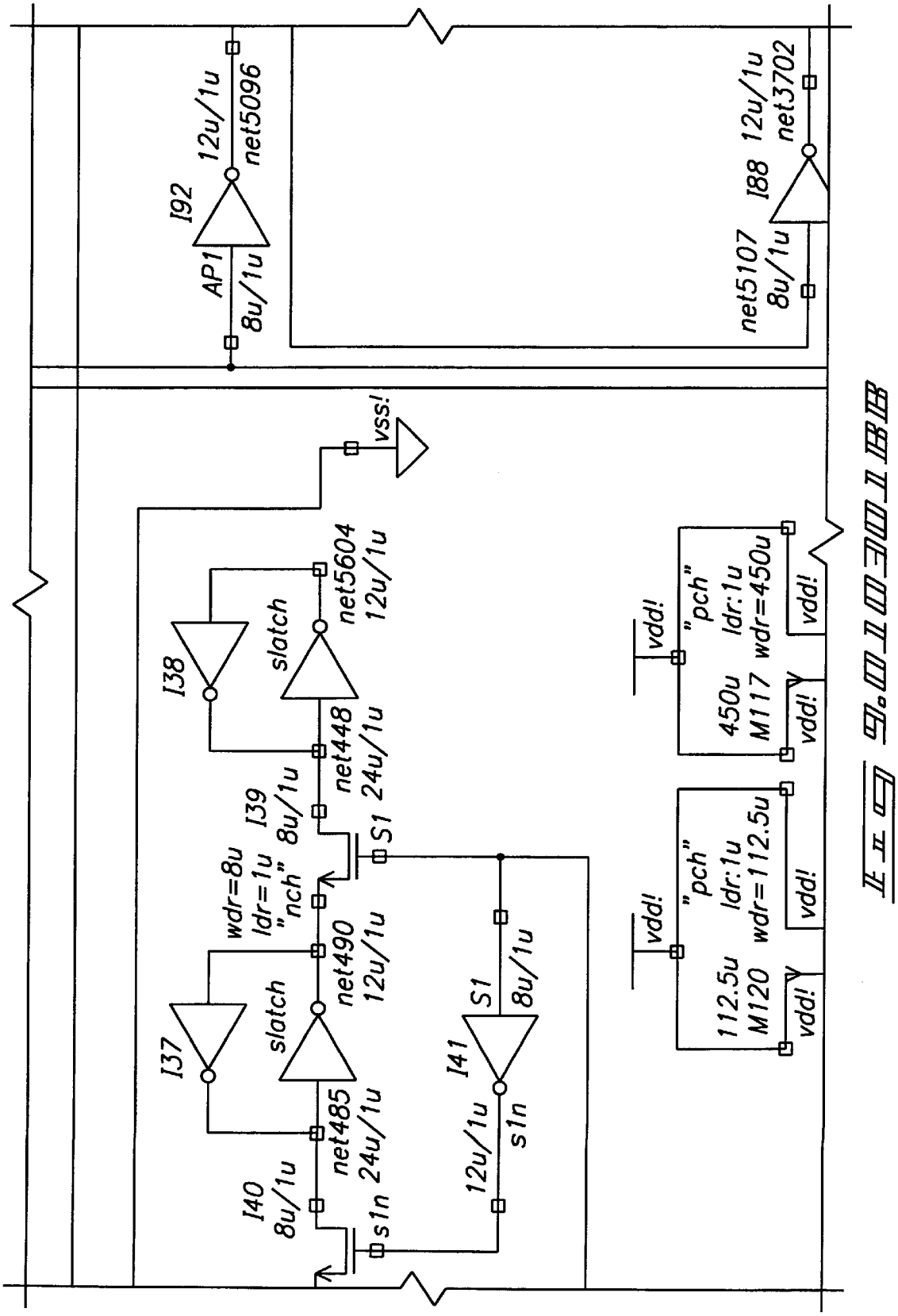

I92
12u/1u
net5096
AP1
8u/1u
I88
12u/1u
net3702
net5107
8u/1u
vss!
I38
slatch
net5604
12u/1u
net448
24u/1u
I39
8u/1u
S1
wdr=8u
ldr=1u
"nch"
net490
12u/1u
I37
slatch
net485
24u/1u
I40
8u/1u
s1n
I41
S1
8u/1u
12u/1u
s1n
vdd!
"pch"
ldr:1u
wdr=450u
450u
M117
vdd!
vdd!
vdd!
"pch"
ldr:1u
wdr=112.5u
112.5u
M120
vdd!
vdd!

FIG. 1E

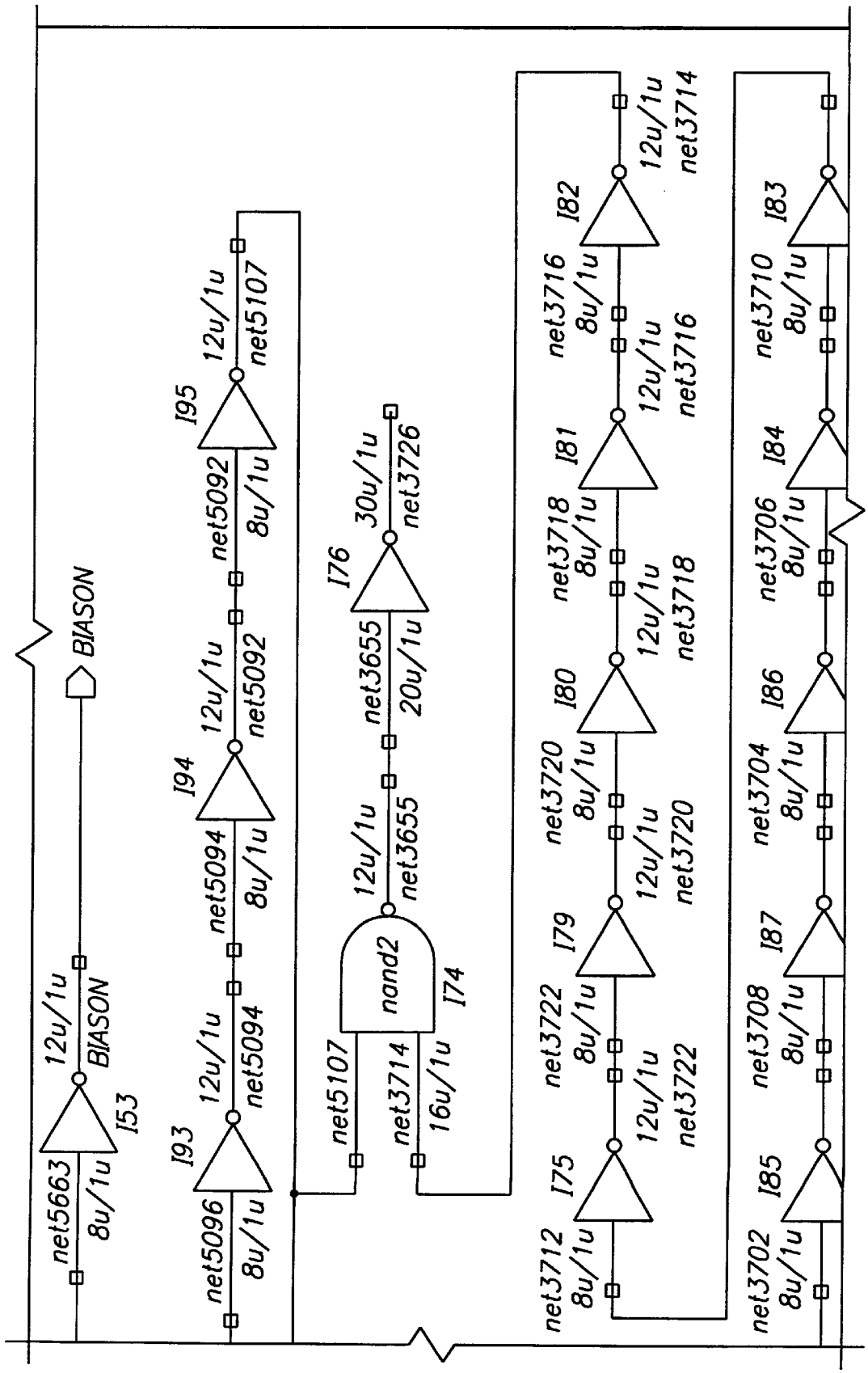

BIASON
I53
12u/1u
BIASON
net5663
8u/1u
I93
12u/1u
net5094
net5096
8u/1u
I94
12u/1u
net5092
net5094
8u/1u
I95
12u/1u
net5107
net5092
8u/1u
I74
nand2
12u/1u
net3655
net5107
net3714
16u/1u
I76
30u/1u
net3726
net3655
20u/1u
I75
net3722
8u/1u
12u/1u
net3722
net3712
8u/1u
I79
net3720
8u/1u
12u/1u
net3720
I80
net3718
8u/1u
12u/1u
net3718
I81
net3716
8u/1u
12u/1u
net3716
I82
12u/1u
net3714
I85
net3708
8u/1u
net3702
8u/1u
I87
net3704
8u/1u
I86
net3706
8u/1u
I84
net3710
8u/1u
I83

FIG 95

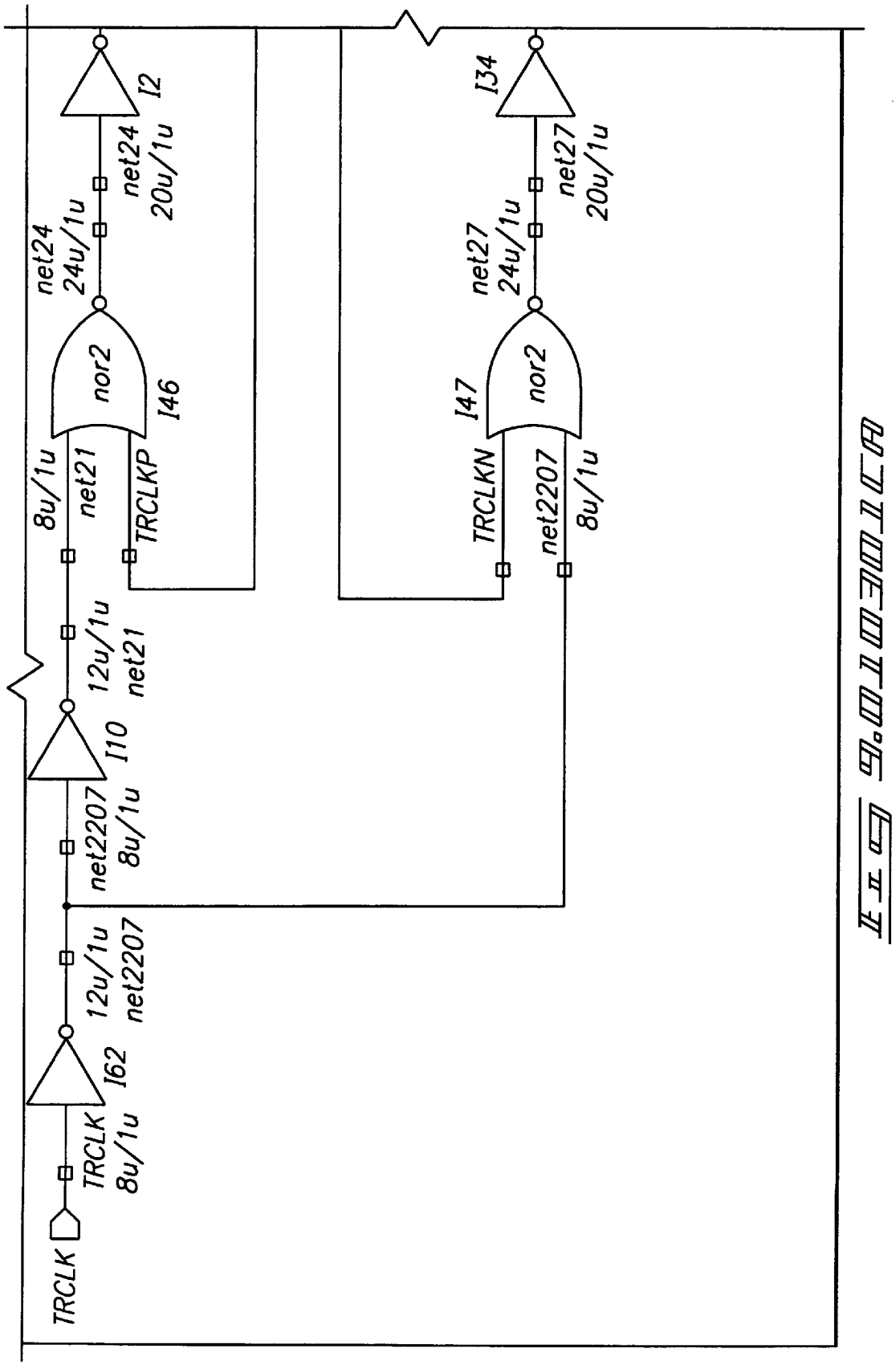

TRCLK
TRCLK
8u/1u
I62
12u/1u
net2207
net2207
8u/1u
I10
12u/1u
net21
net21
8u/1u
net24
24u/1u
net24
20u/1u
I2
nor2
I46
TRCLKP
8u/1u
net21
I34
net27
20u/1u
net27
24u/1u
nor2
I47
TRCLKN
net2207
8u/1u

FIG 95

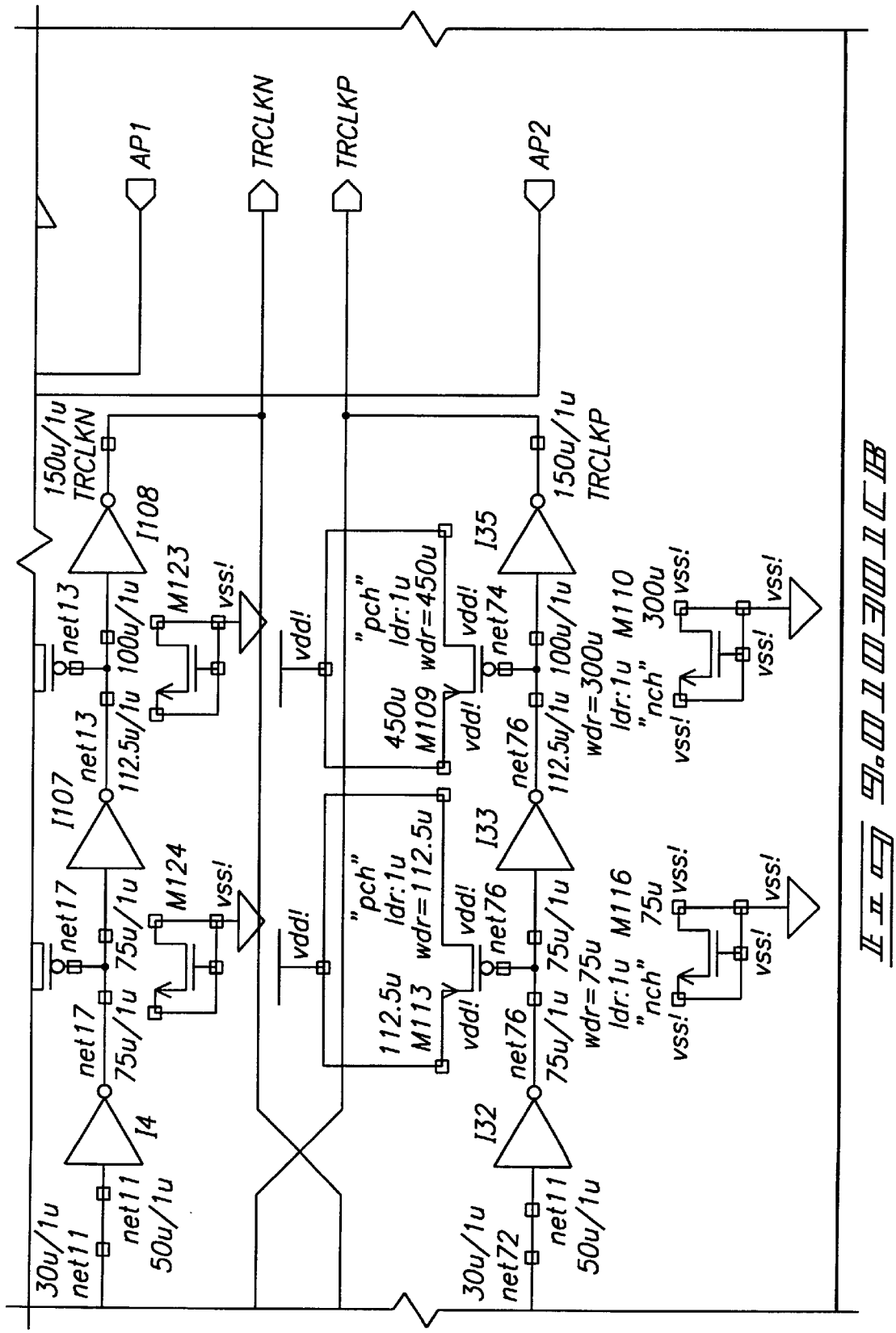
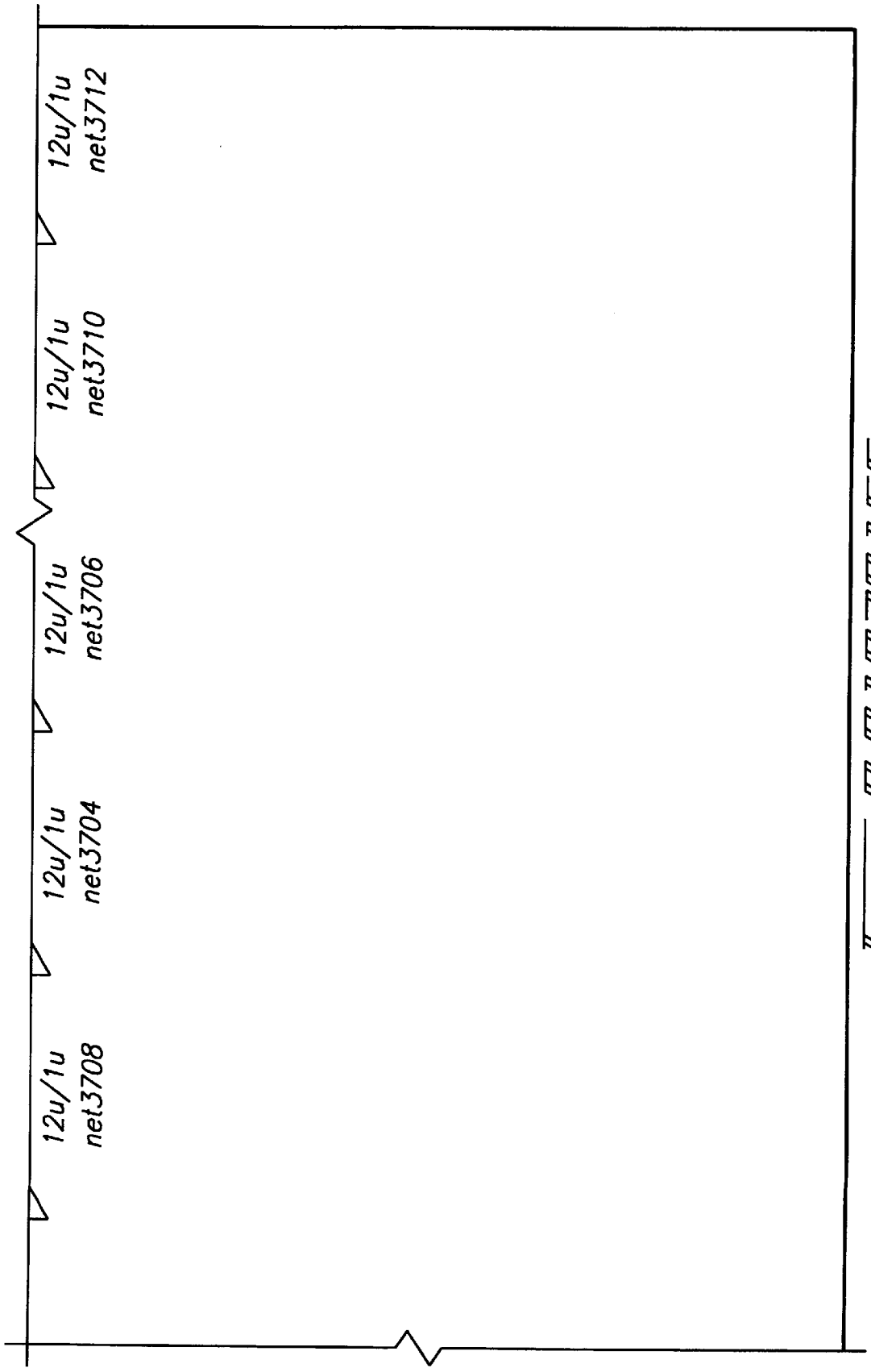
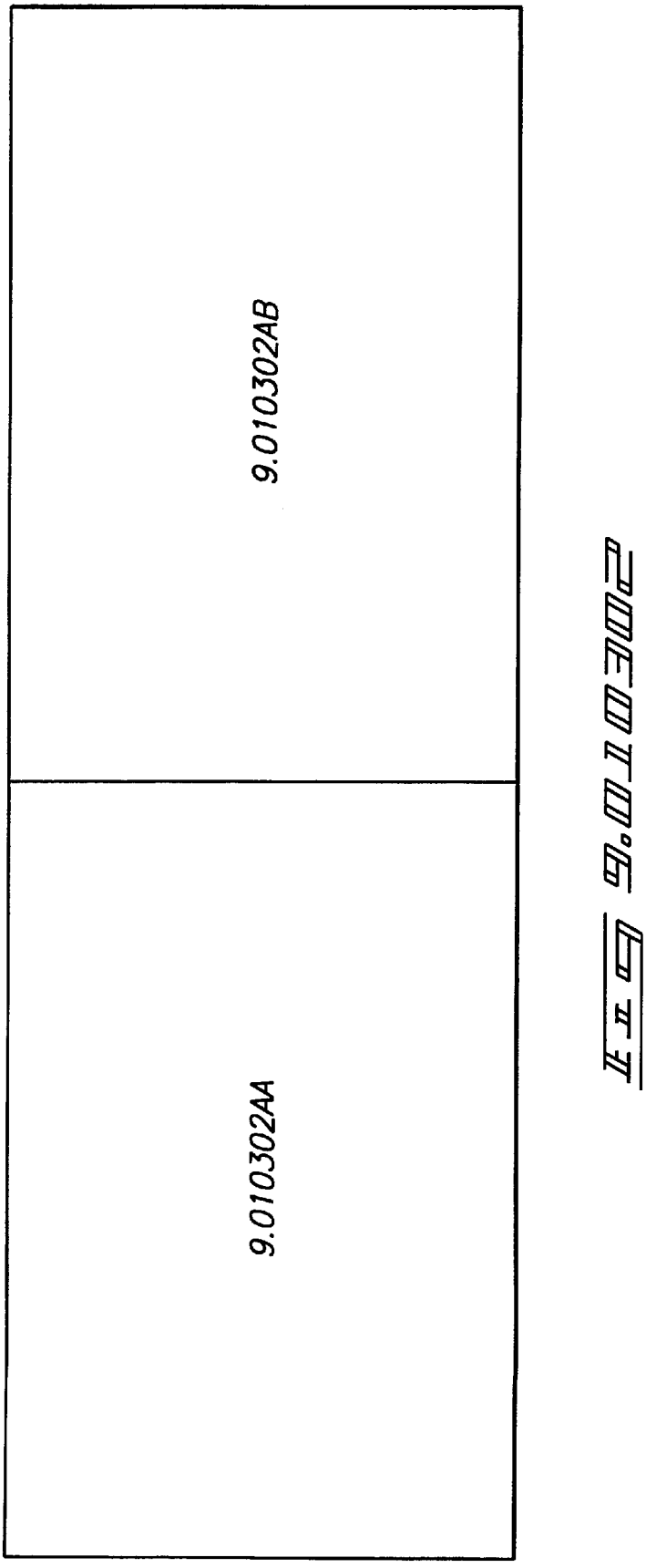

AP1
TRCLKN
TRCLKP
AP2
150u/1u
TRCLKN
I108
M123
vss!
net13
100u/1u
112.5u/1u
net13
I107
M124
net17
75u/1u
net17
I4
net11
50u/1u
30u/1u
net11
vdd!
"pch"
ldr:1u
wdr=112.5u
112.5u
M113
vdd!
net76
75u/1u
wdr=75u
I32
net76
net72
450u
M109
wdr=450u
net74
I35
150u/1u
TRCLKP
100u/1u
112.5u/1u
net76
I33
wdr=300u
ldr:1u M110
"nch" 300u
ldr:1u M116
"nch" 75u
vss!

FIG. 9.00100E


12u/1u net3712
12u/1u net3710
12u/1u net3706
12u/1u net3704
12u/1u net3708
FIG 95


9.010302AB
9.010302AA
FIG 95,00102

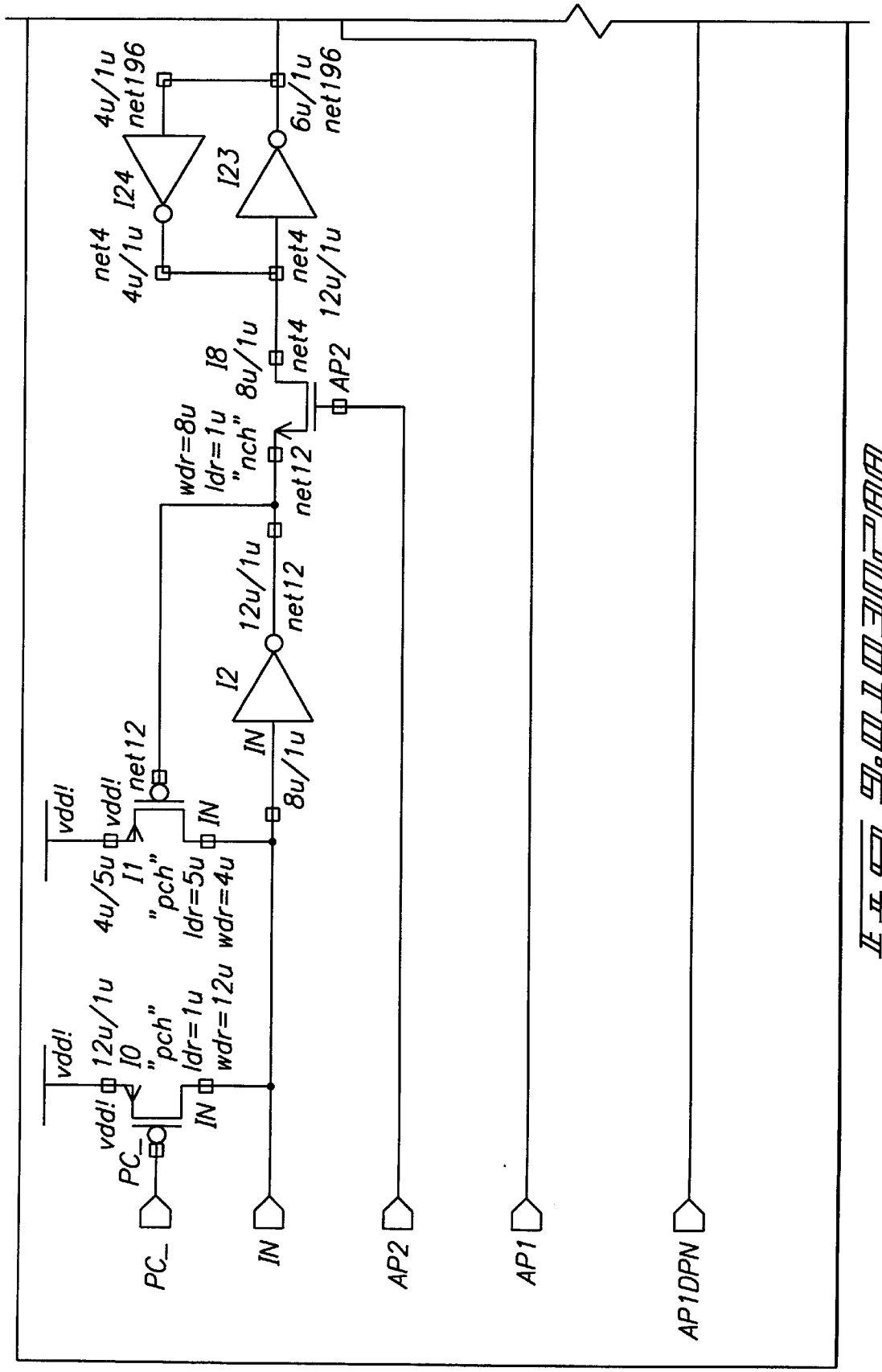


FIG 95 CIRCUIT DIAGRAM

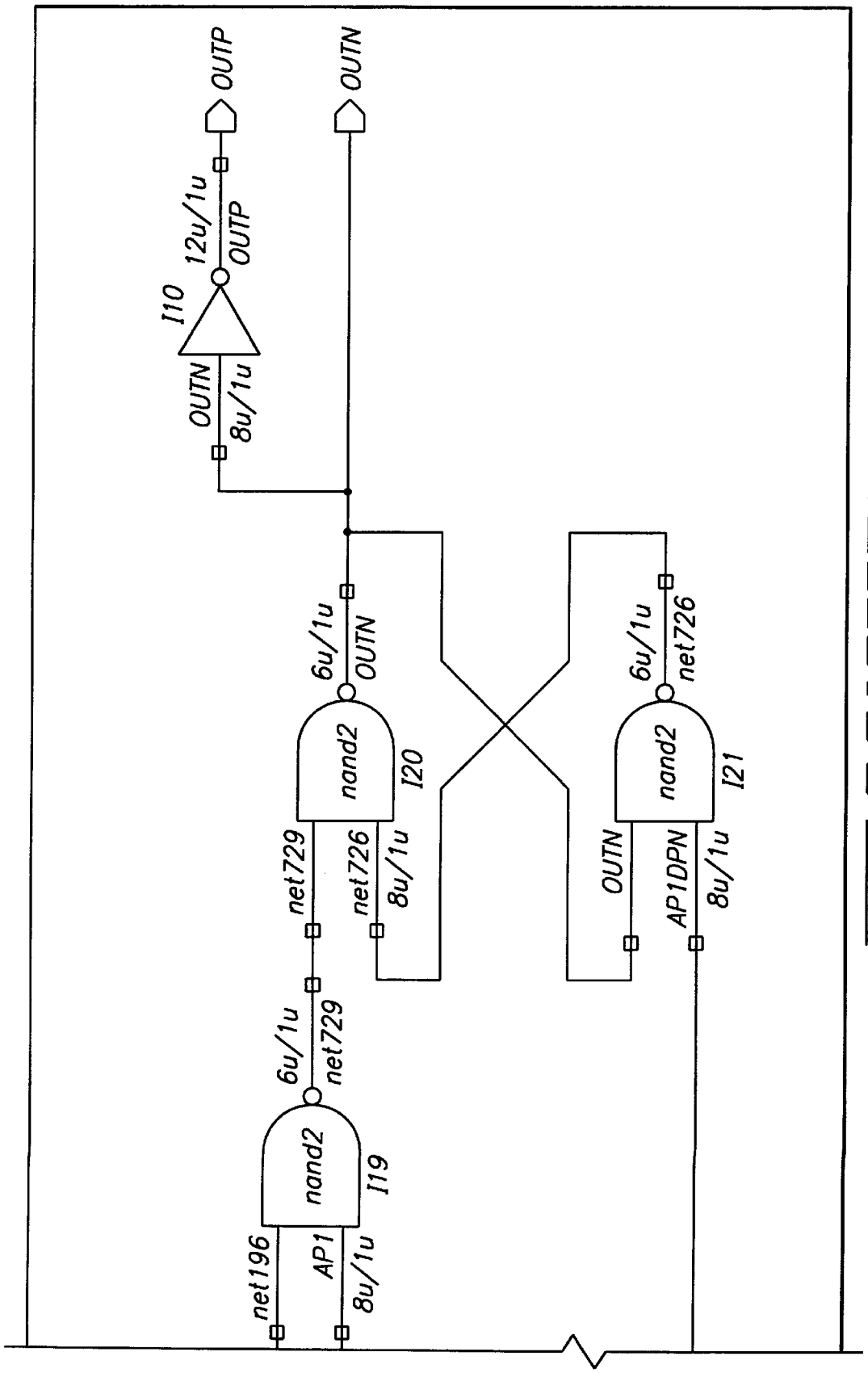
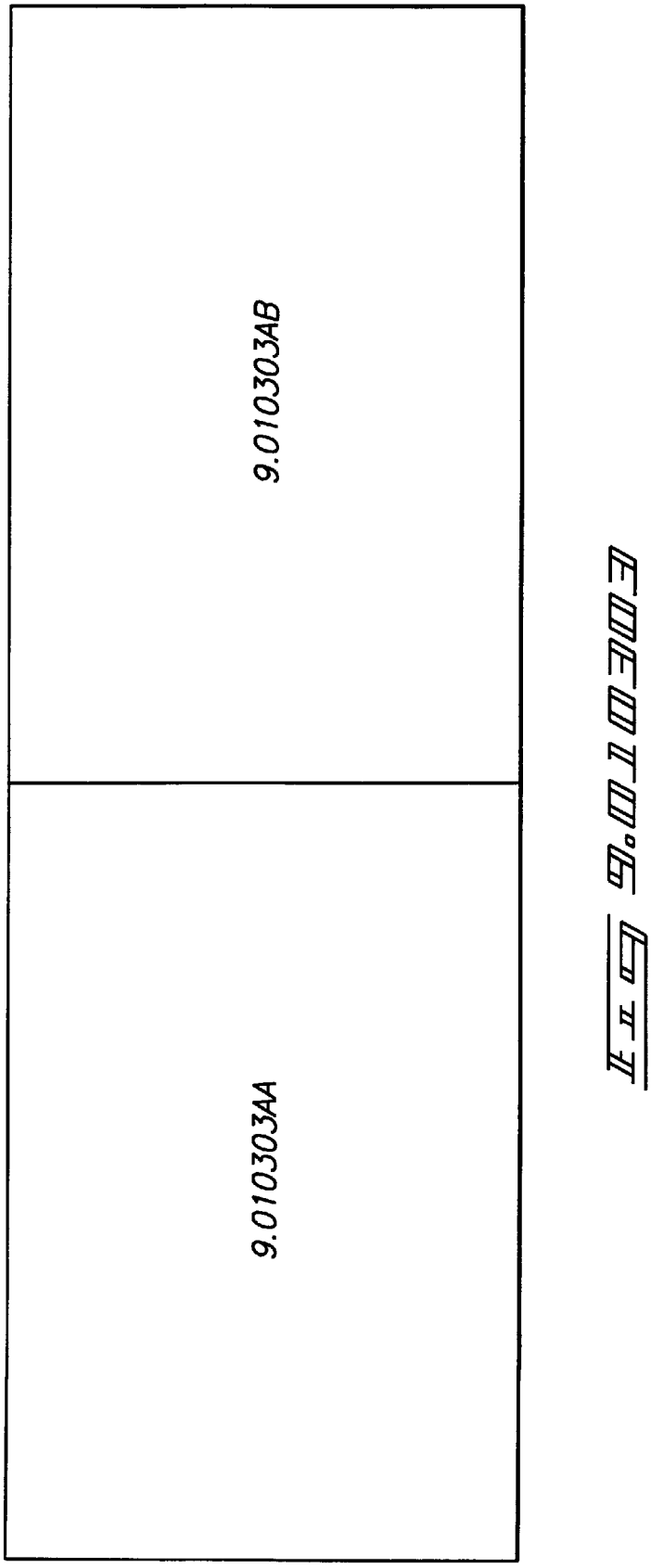

OUTP
OUTN
I10
12u/1u
OUTP
OUTN
8u/1u
6u/1u
OUTN
nand2
I20
net729
net726
8u/1u
6u/1u
net729
nand2
I19
net196
AP1
8u/1u
6u/1u
net726
nand2
I21
OUTN
AP1DPN
8u/1u

FIG 6,130,602


9.010303AB
9.010303AA
FIG. 95

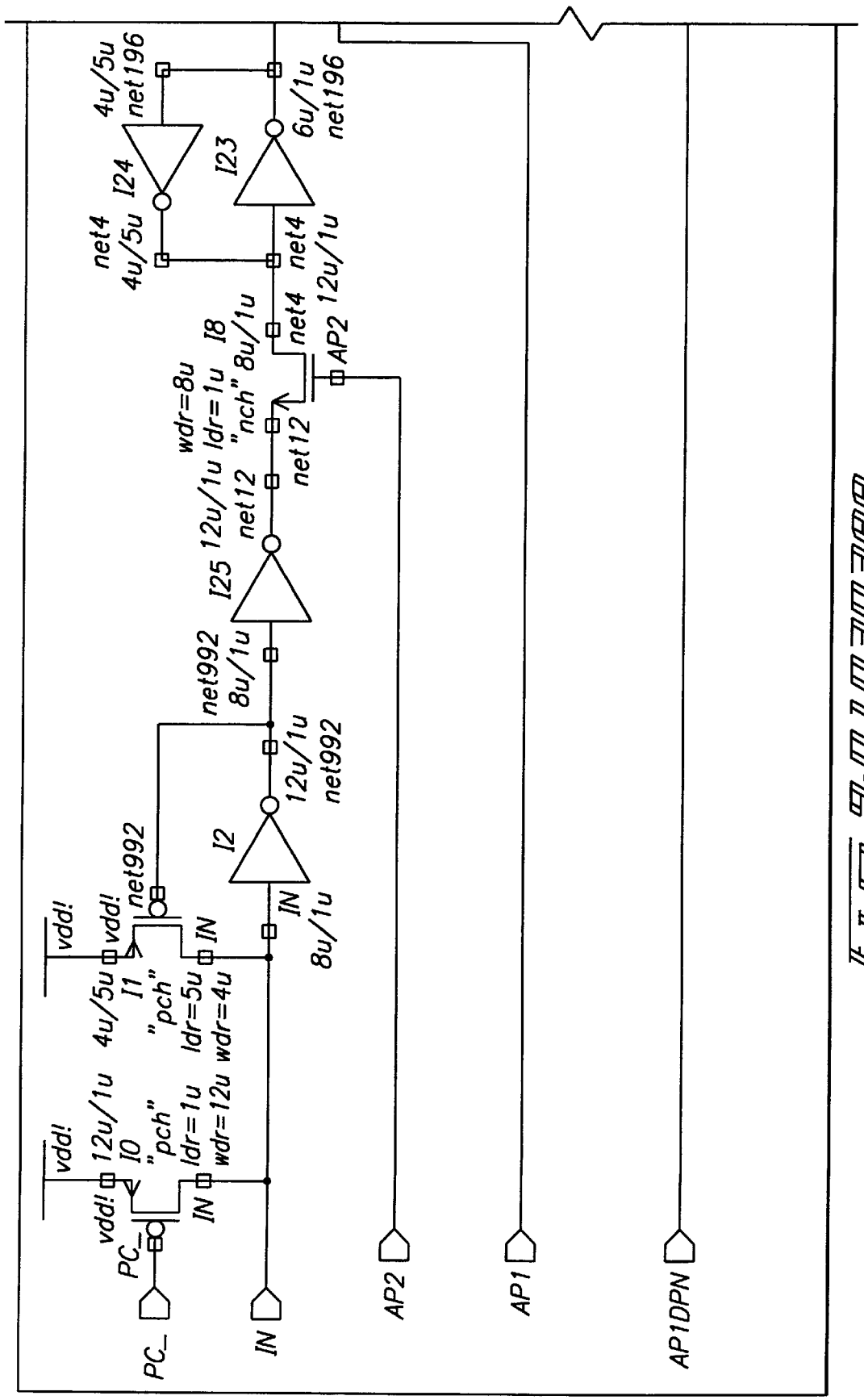

vdd!
PC_
IN
AP2
AP1
AP1DPN
I0 "pch" 12u/1u ldr=1u wdr=12u
I1 "pch" 4u/5u ldr=5u wdr=4u
I2 8u/1u 12u/1u net992
I24 net4 4u/5u 4u/5u net196
I23 6u/1u net196
I25 12u/1u net12 wdr=8u ldr=1u
I8 "nch" 8u/1u net4 12u/1u AP2

FIG 5B

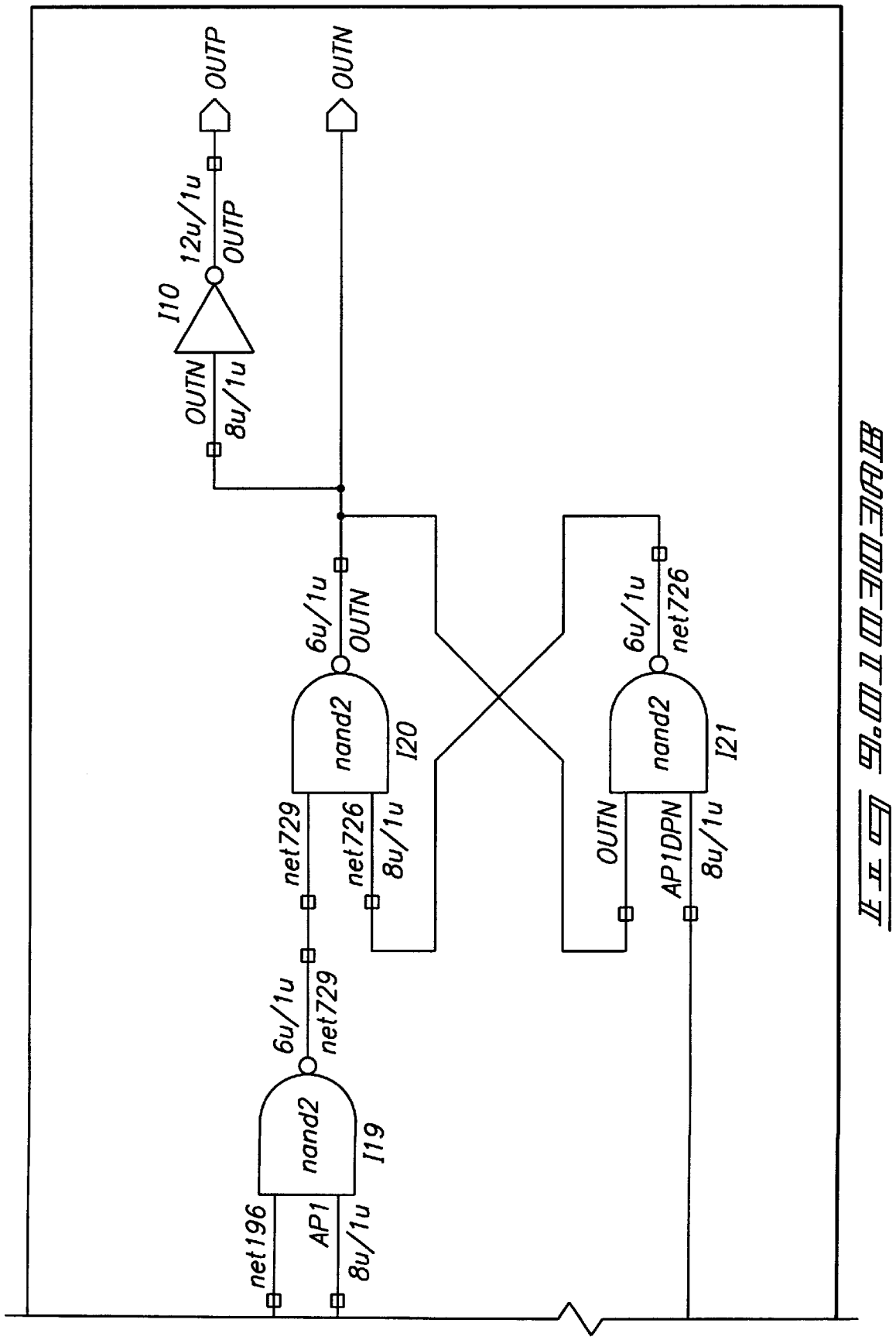


FIG. 91.00 BLOCK DIAGRAM

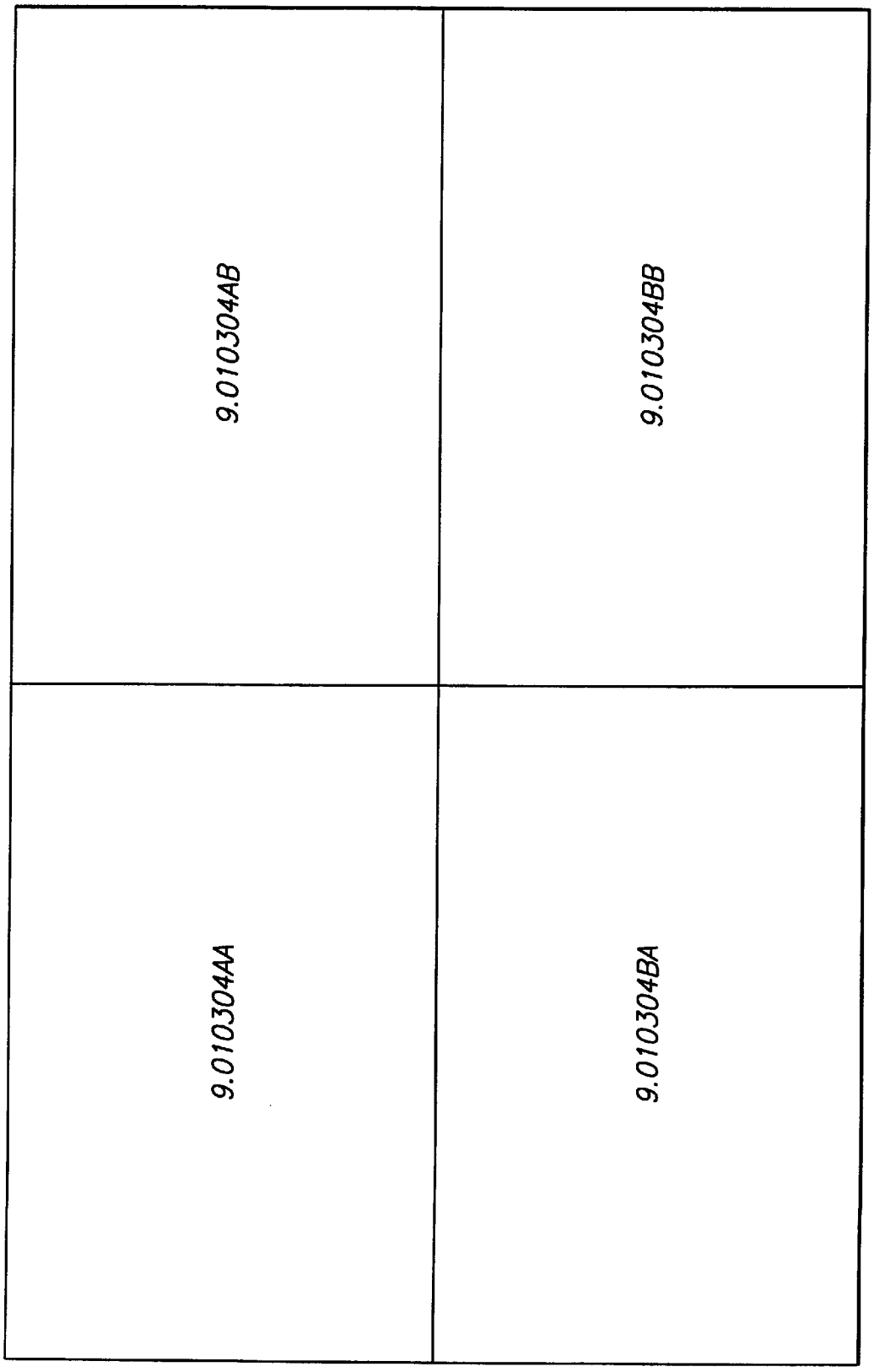


FIG 9.010304

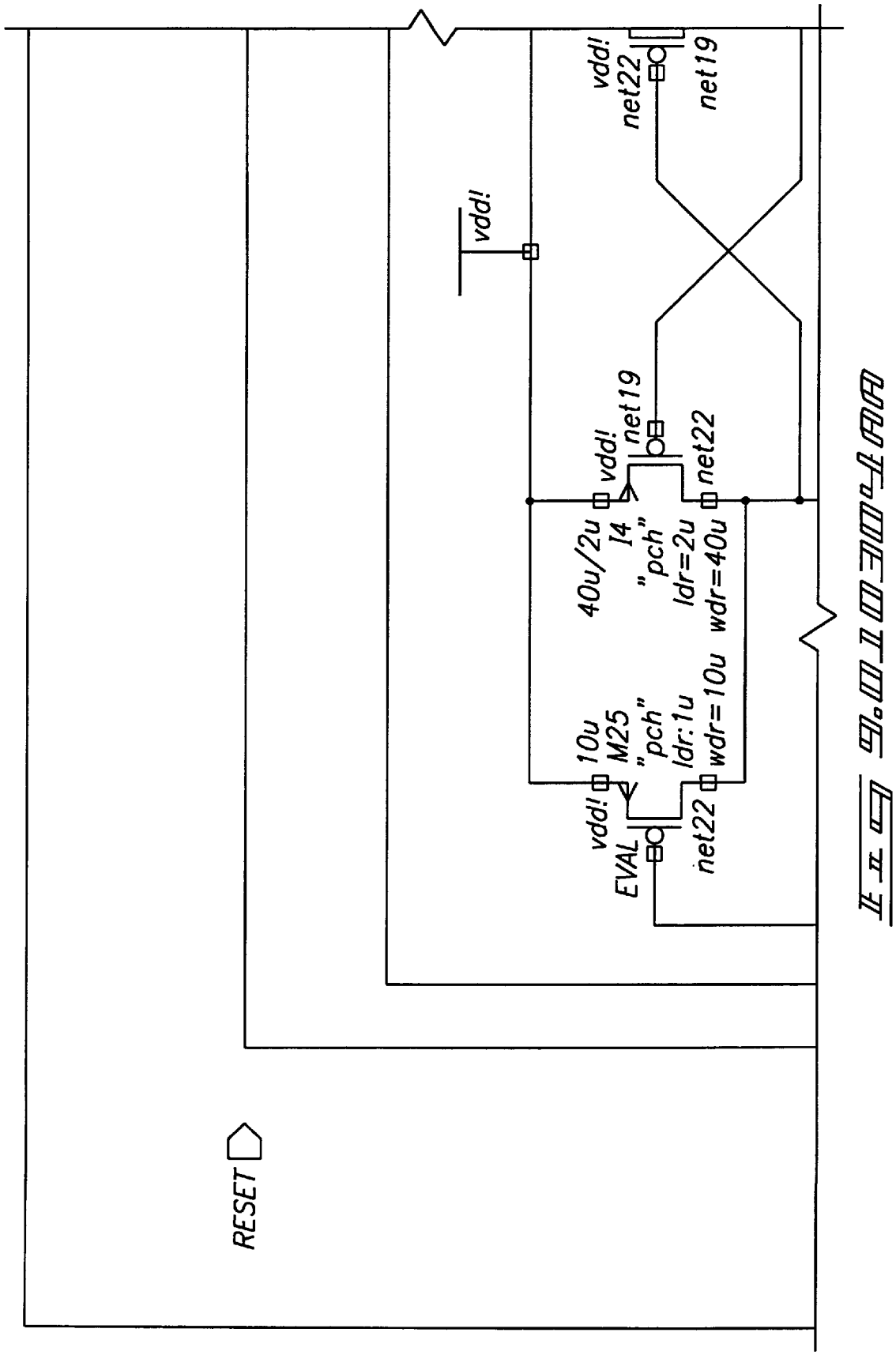

vdd!
net22
net19
vdd!
vdd!
net19
net22
40u/2u
I4
"pch"
ldr=2u
wdr=40u
10u
M25
"pch"
ldr:1u
wdr=10u
vdd!
EVAL
net22
RESET

FIG 6,130,602

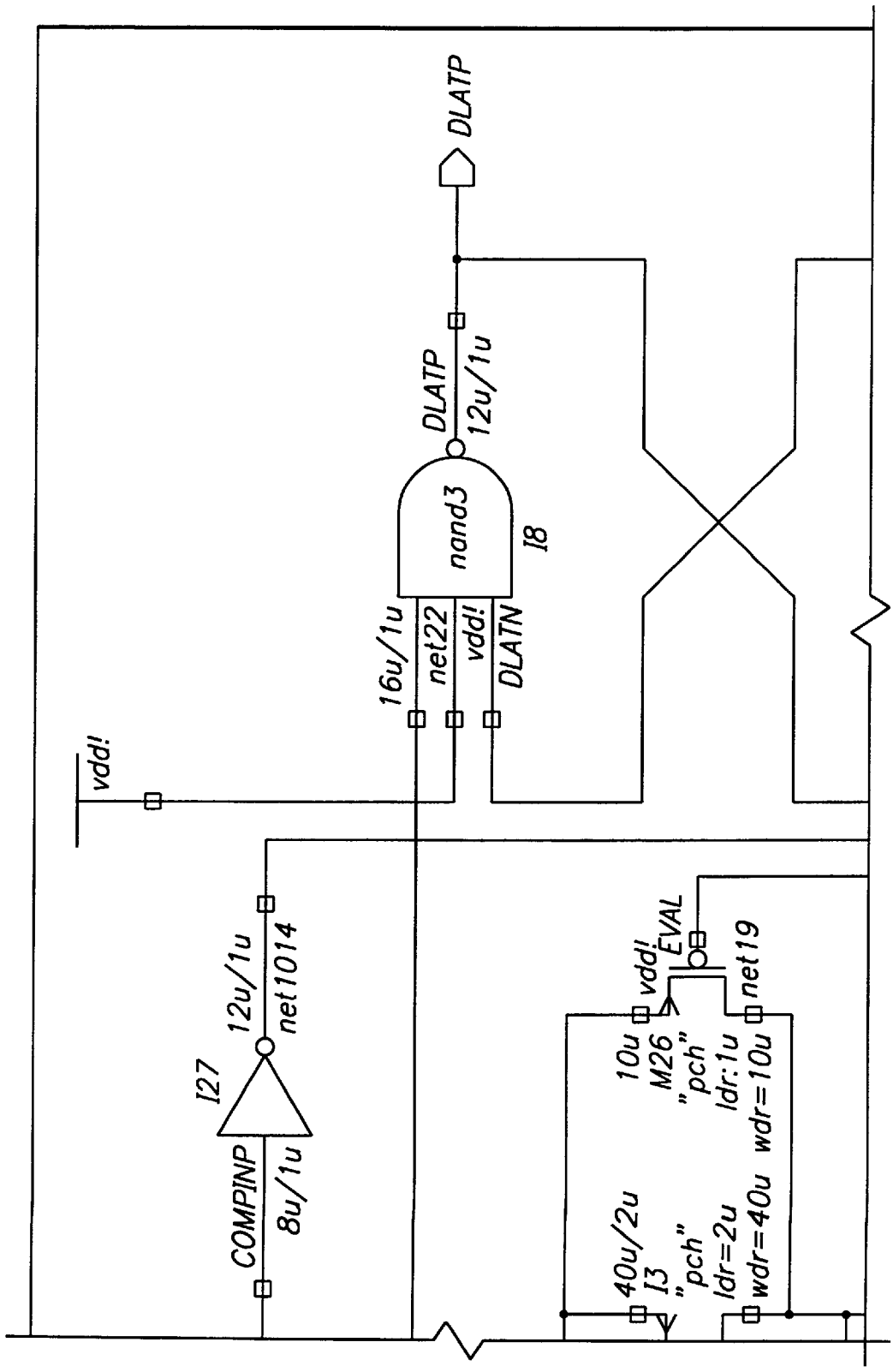

DLATP
DLATP
12u/1u
nand3
I8
16u/1u
net22
vdd!
DLATN
vdd!
12u/1u
net1014
I27
COMPINP
8u/1u
vdd!
EVAL
10u
M26
"pch"
ldr:1u
wdr=10u
net19
40u/2u
I3
"pch"
ldr=2u
wdr=40u

FIG 6

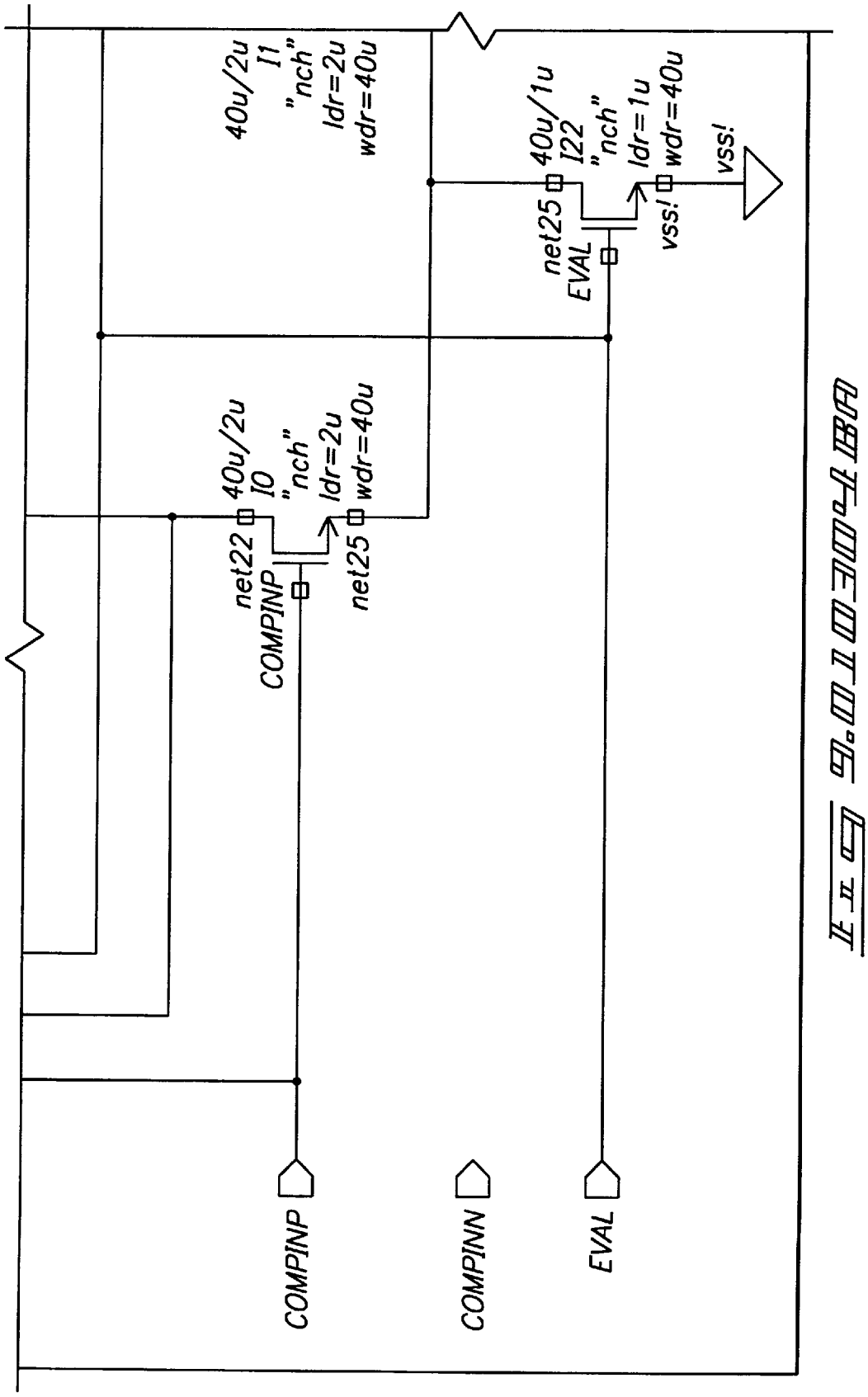

40u/2u
I1
"nch"
ldr=2u
wdr=40u
40u/1u
I22
"nch"
ldr=1u
wdr=40u
vss!
net25
EVAL
vss!
40u/2u
I0
"nch"
ldr=2u
wdr=40u
net22
COMPINP
net25
COMPINP
COMPINN
EVAL

FIG 2388

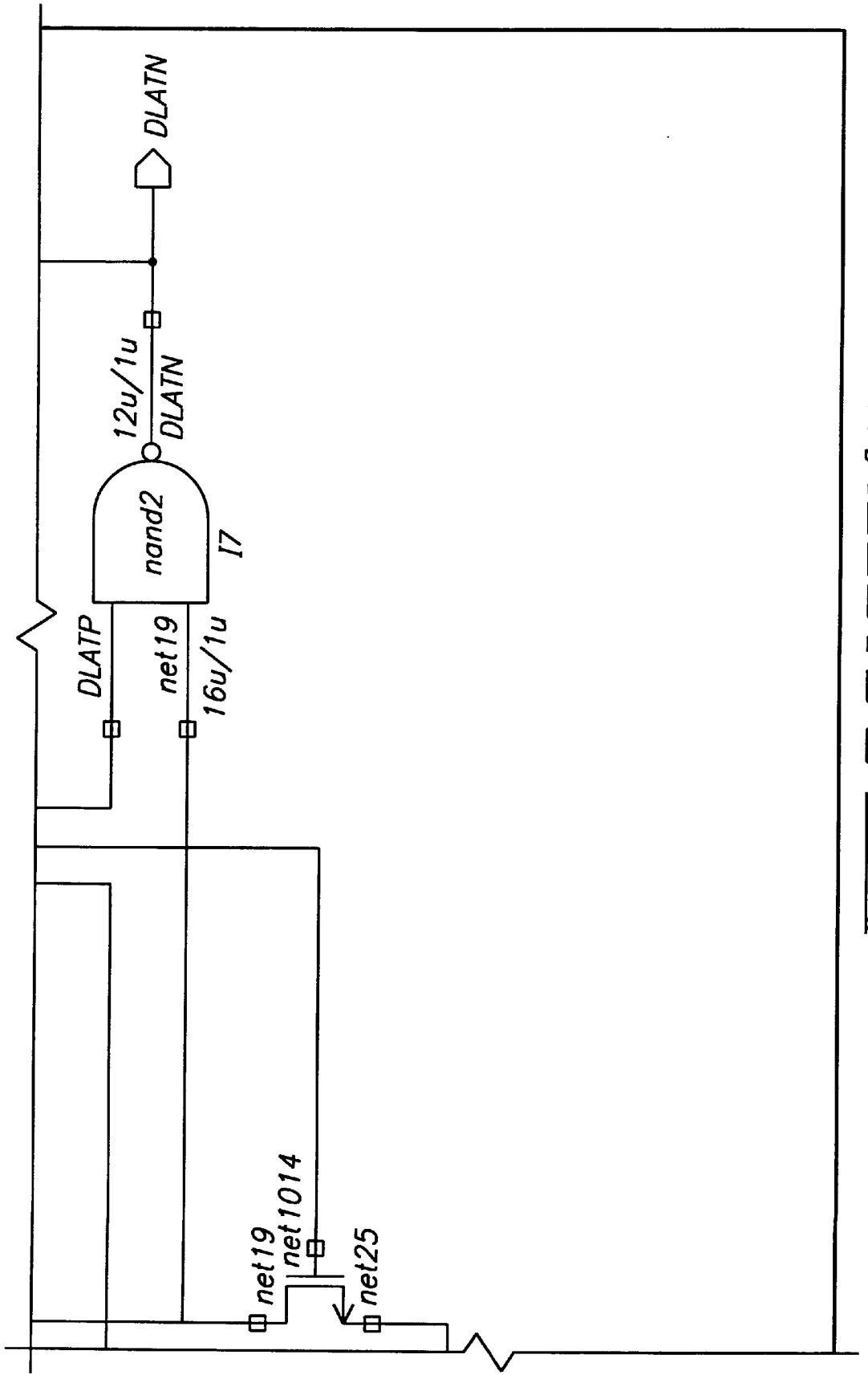

DLATN
12u/1u
DLATN
nand2
I7
DLATP
net19
16u/1u
net19
net1014
net25

FIG 6B

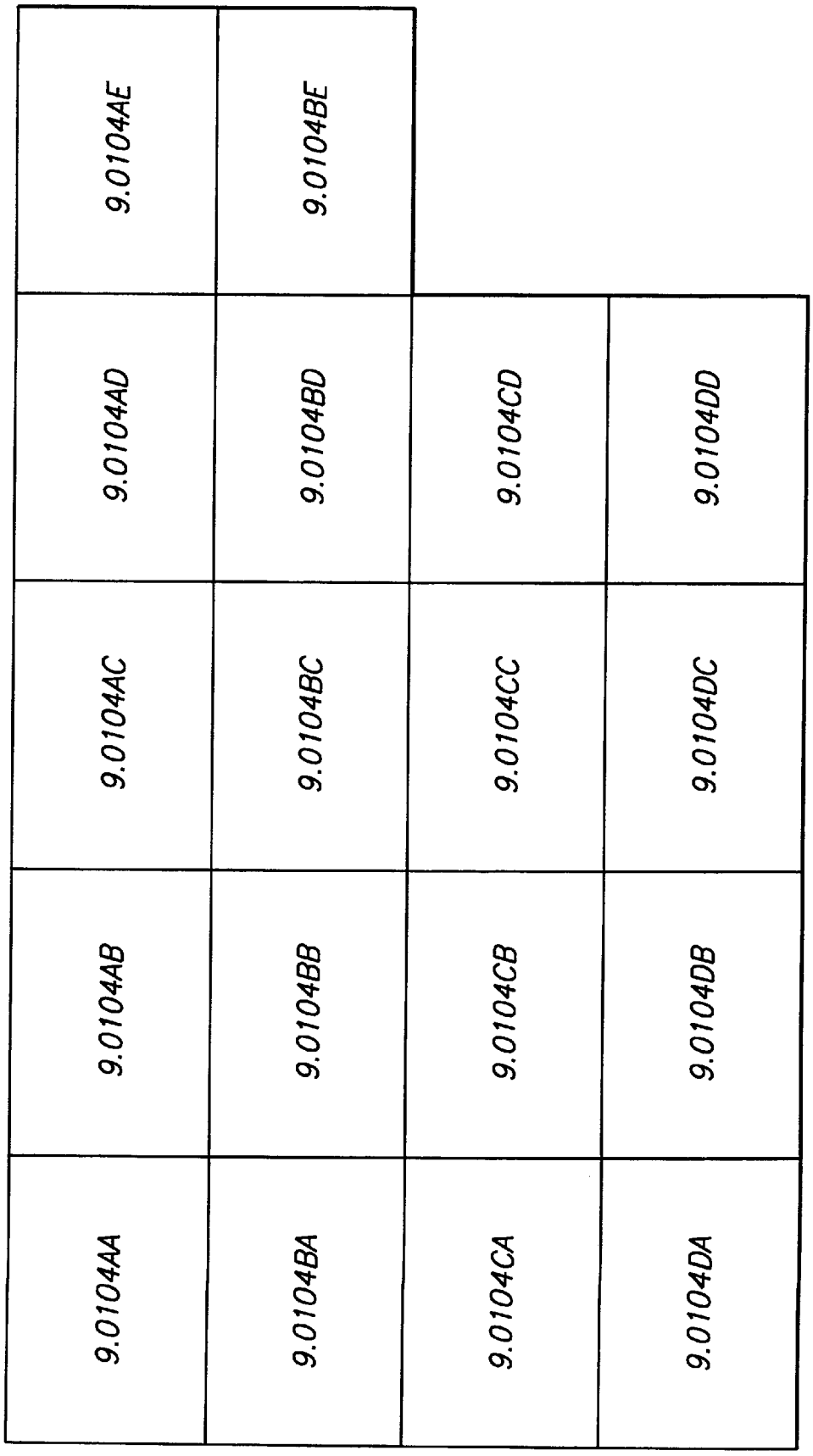

9.0104AA
9.0104AB
9.0104AC
9.0104AD
9.0104AE
9.0104BA
9.0104BB
9.0104BC
9.0104BD
9.0104BE
9.0104CA
9.0104CB
9.0104CC
9.0104CD
9.0104DA
9.0104DB
9.0104DC
9.0104DD

FIG 9.0104

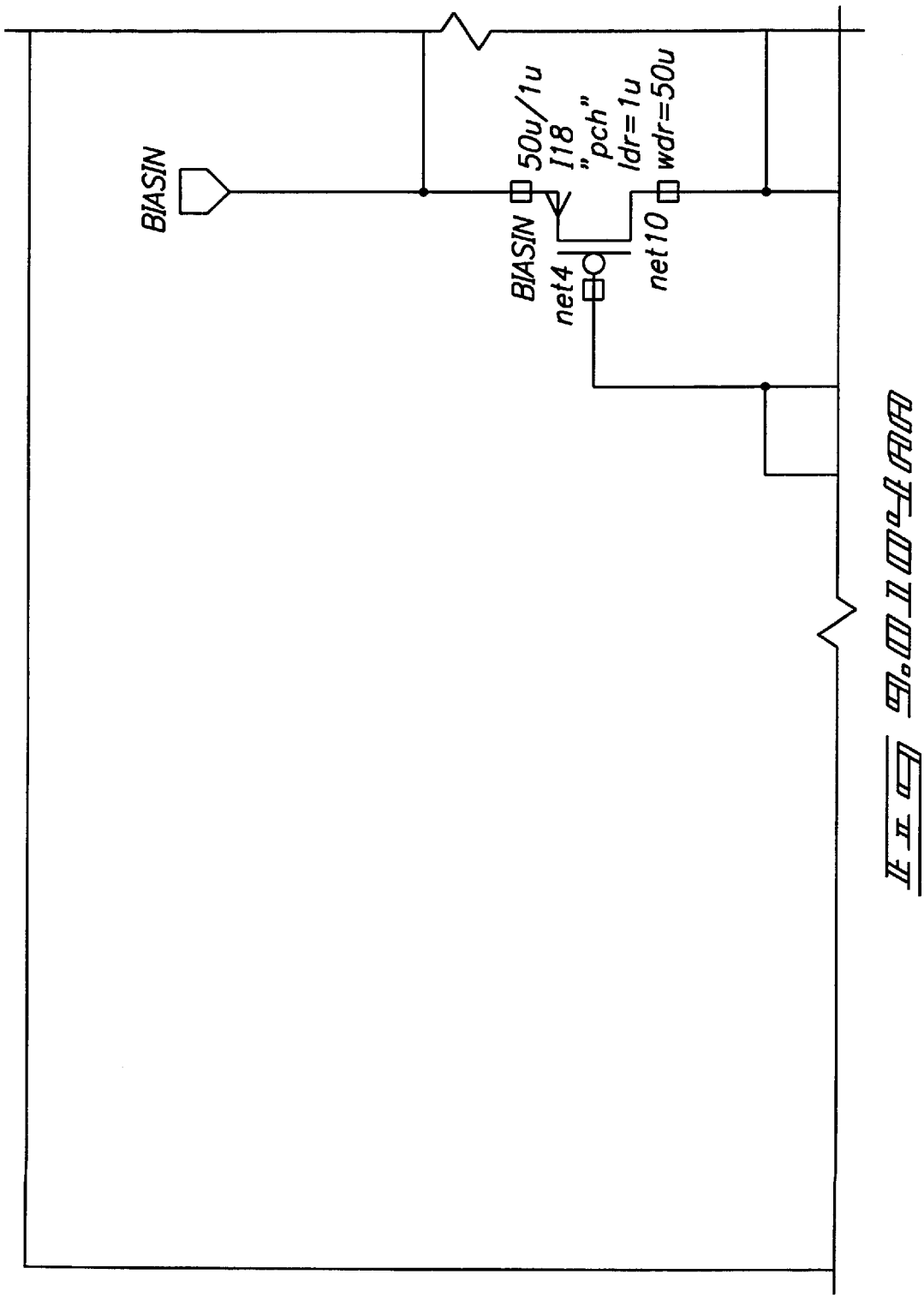


FIG 91.00104AA

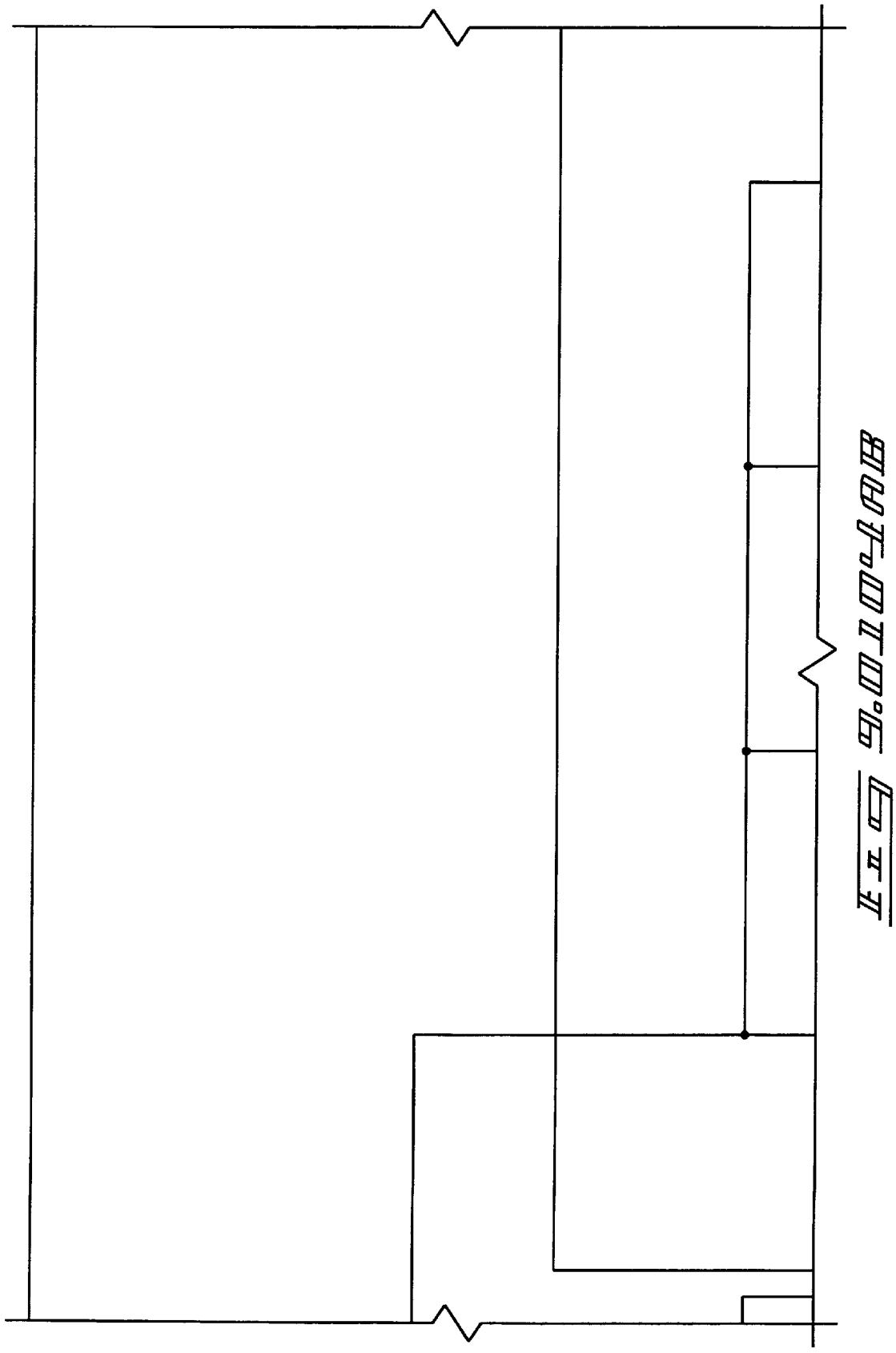
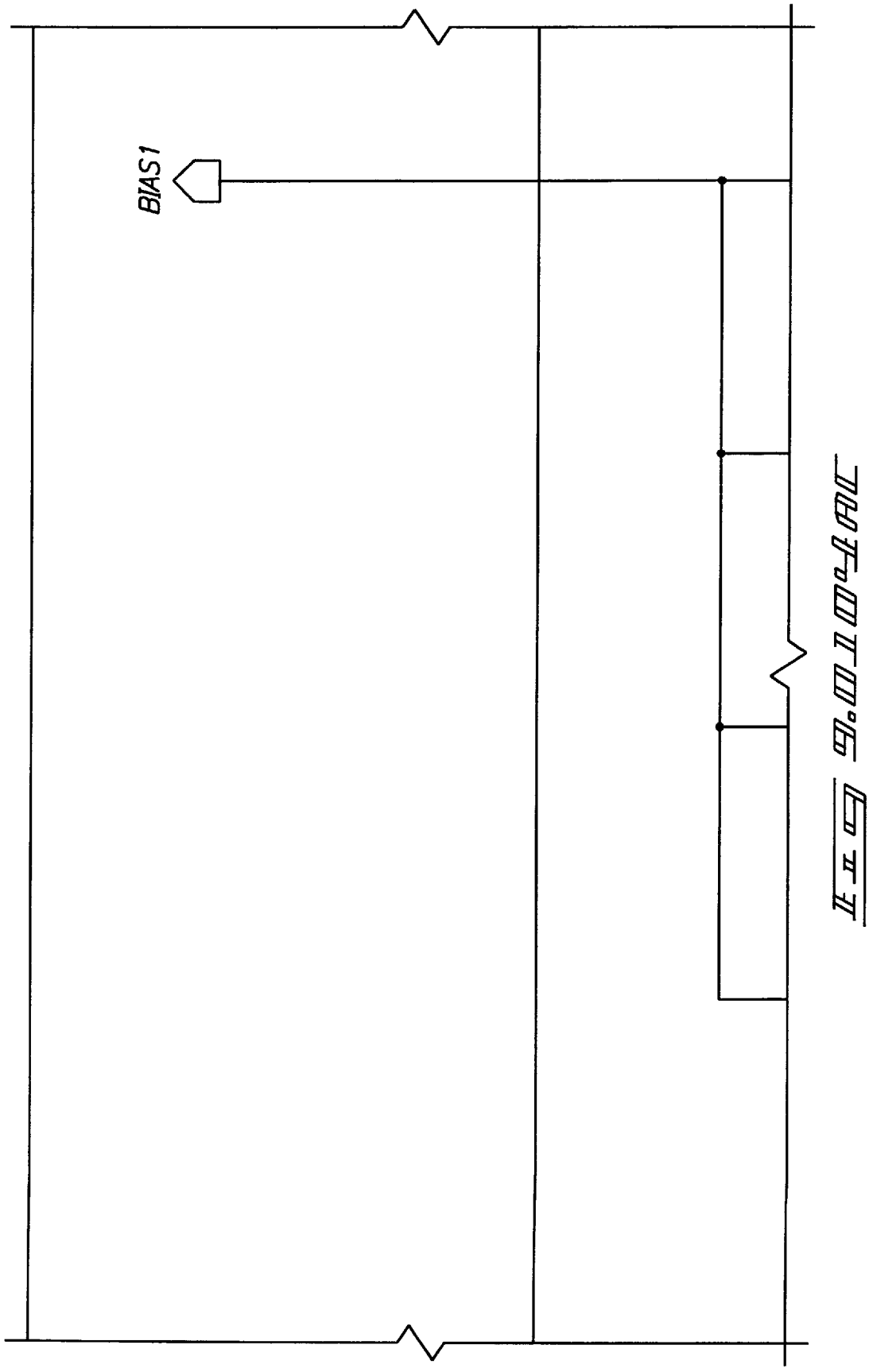
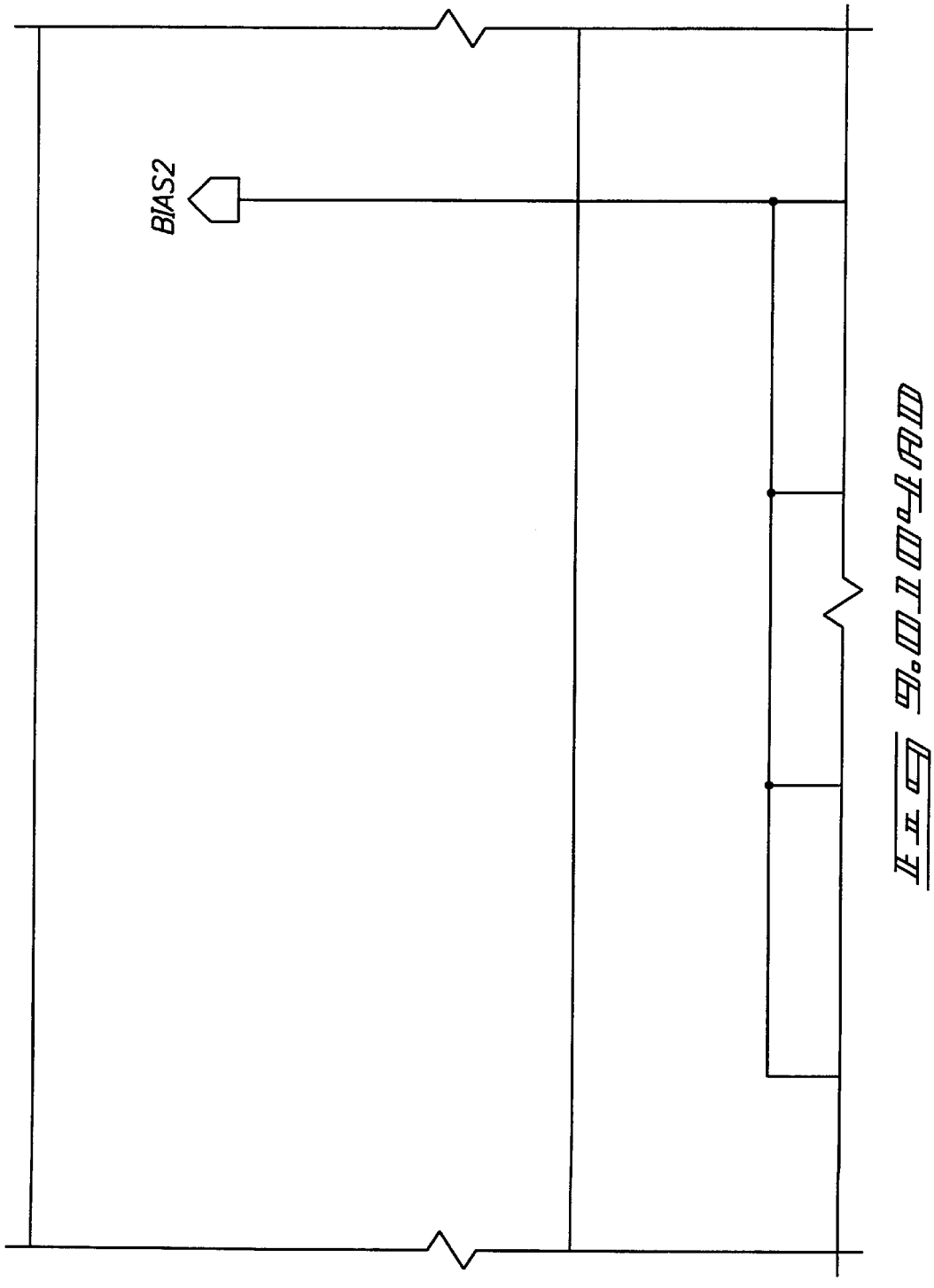
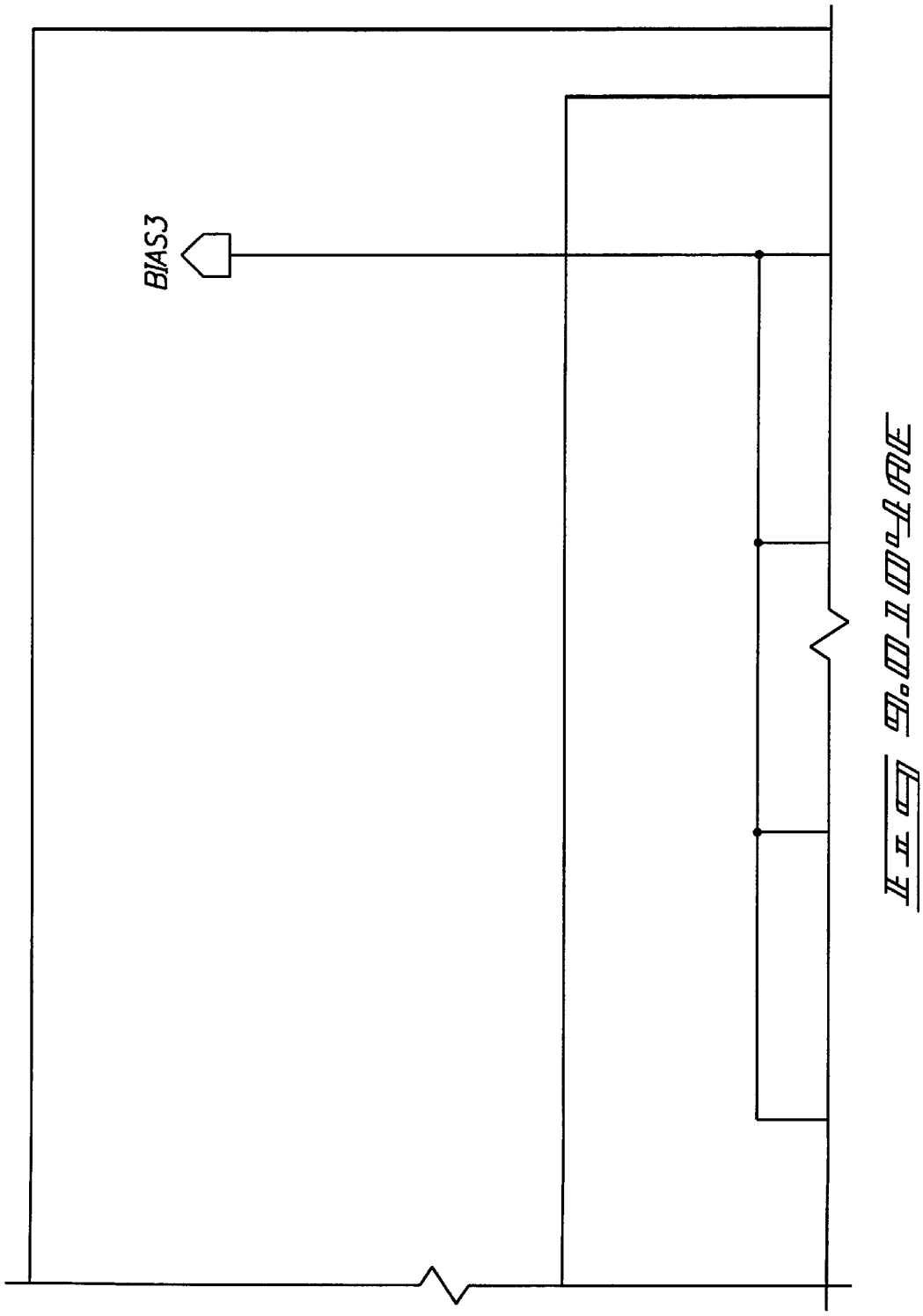


FIG 96,100


BIAS1
FIG. 9,0017


BIAS2
FIG 9,011,044


BIAS3
FIG. 9,001 PAGE

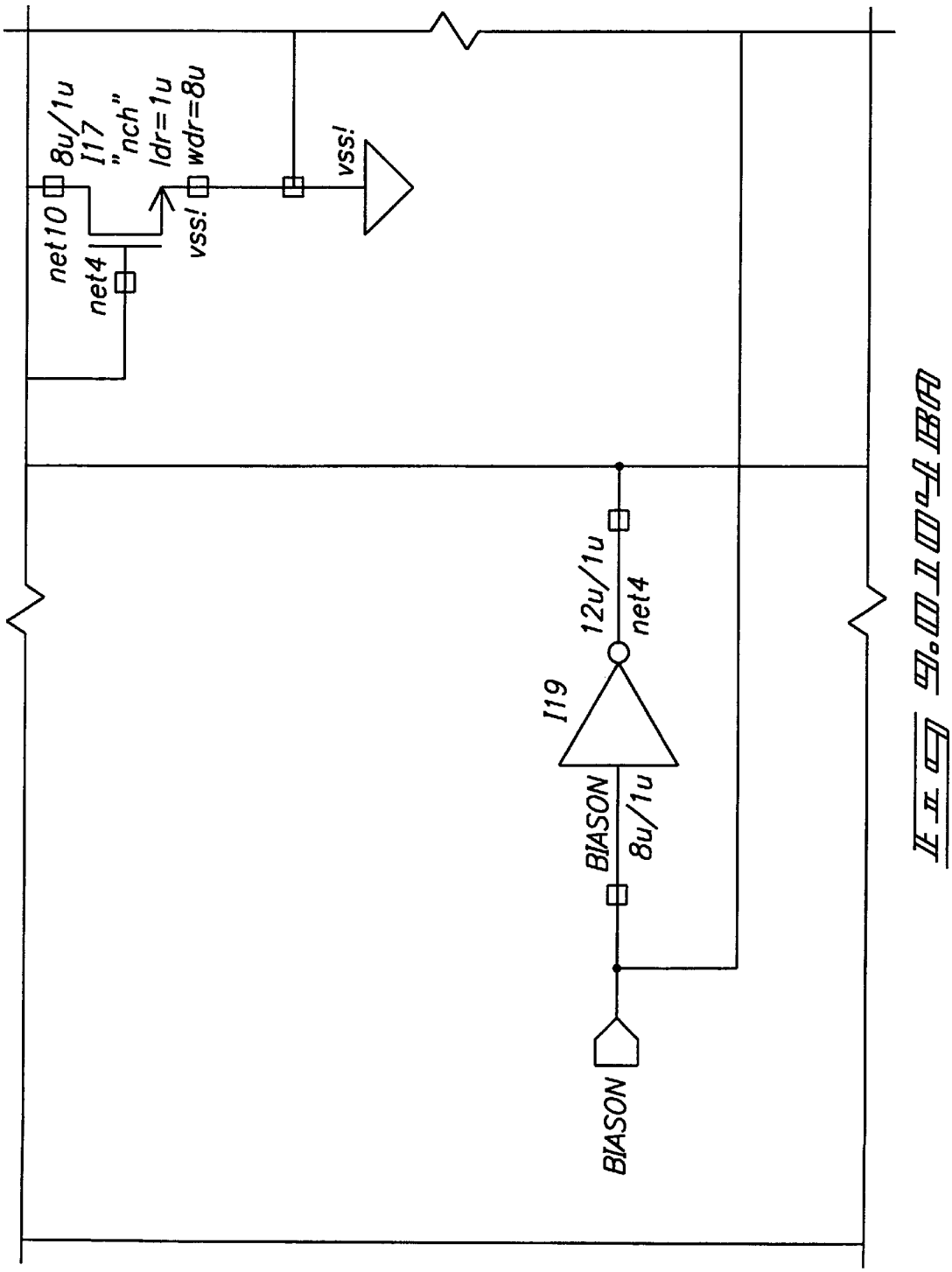

8u/1u
I17
"nch"
ldr=1u
wdr=8u
net10
net4
vss!
vss!
12u/1u
net4
I19
BIASON
8u/1u
BIASON

Fig 9,001,604

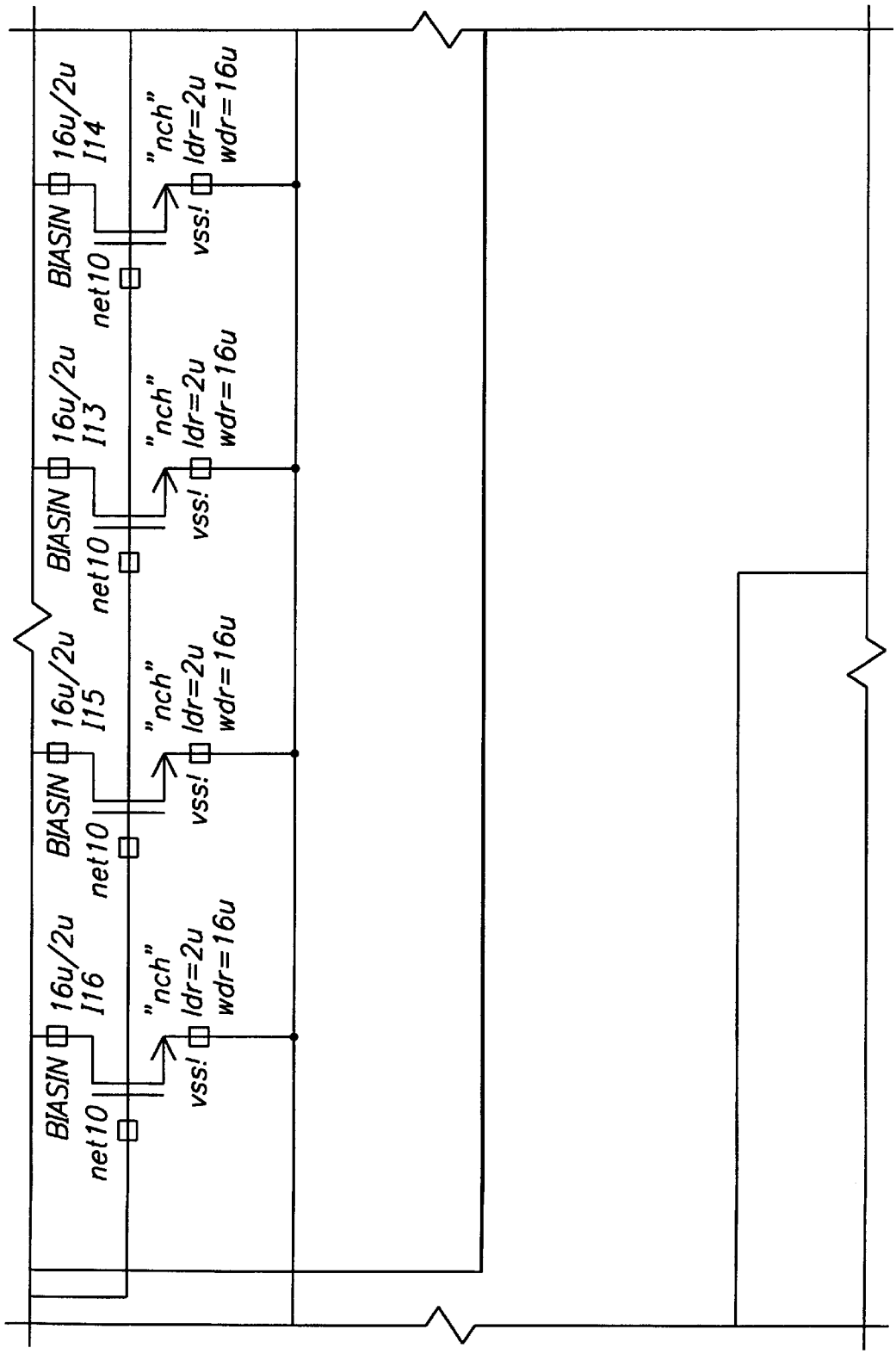
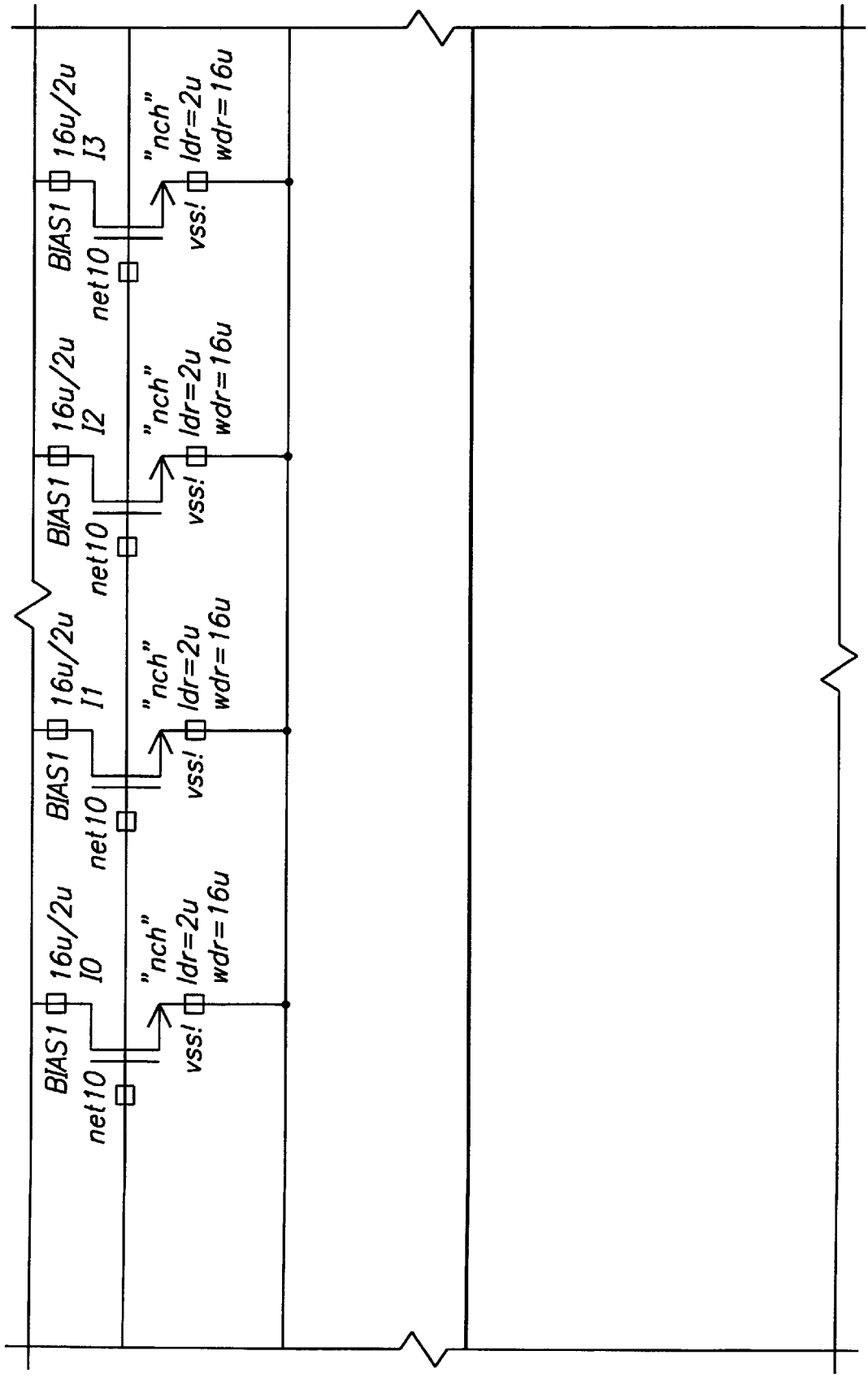

16u/2u
I14
BIASIN
net10
"nch"
ldr=2u
wdr=16u
vss!
16u/2u
I13
BIASIN
net10
"nch"
ldr=2u
wdr=16u
vss!
16u/2u
I15
BIASIN
net10
"nch"
ldr=2u
wdr=16u
vss!
16u/2u
I16
BIASIN
net10
"nch"
ldr=2u
wdr=16u
vss!

FIG. 59,011


16u/2u
I3
BIAS1
net10
"nch"
ldr=2u
wdr=16u
vss!
16u/2u
I2
BIAS1
net10
"nch"
ldr=2u
wdr=16u
vss!
16u/2u
I1
BIAS1
net10
"nch"
ldr=2u
wdr=16u
vss!
16u/2u
I0
BIAS1
net10
"nch"
ldr=2u
wdr=16u
vss!

ИЗГ 9.00 ЧЕРТ

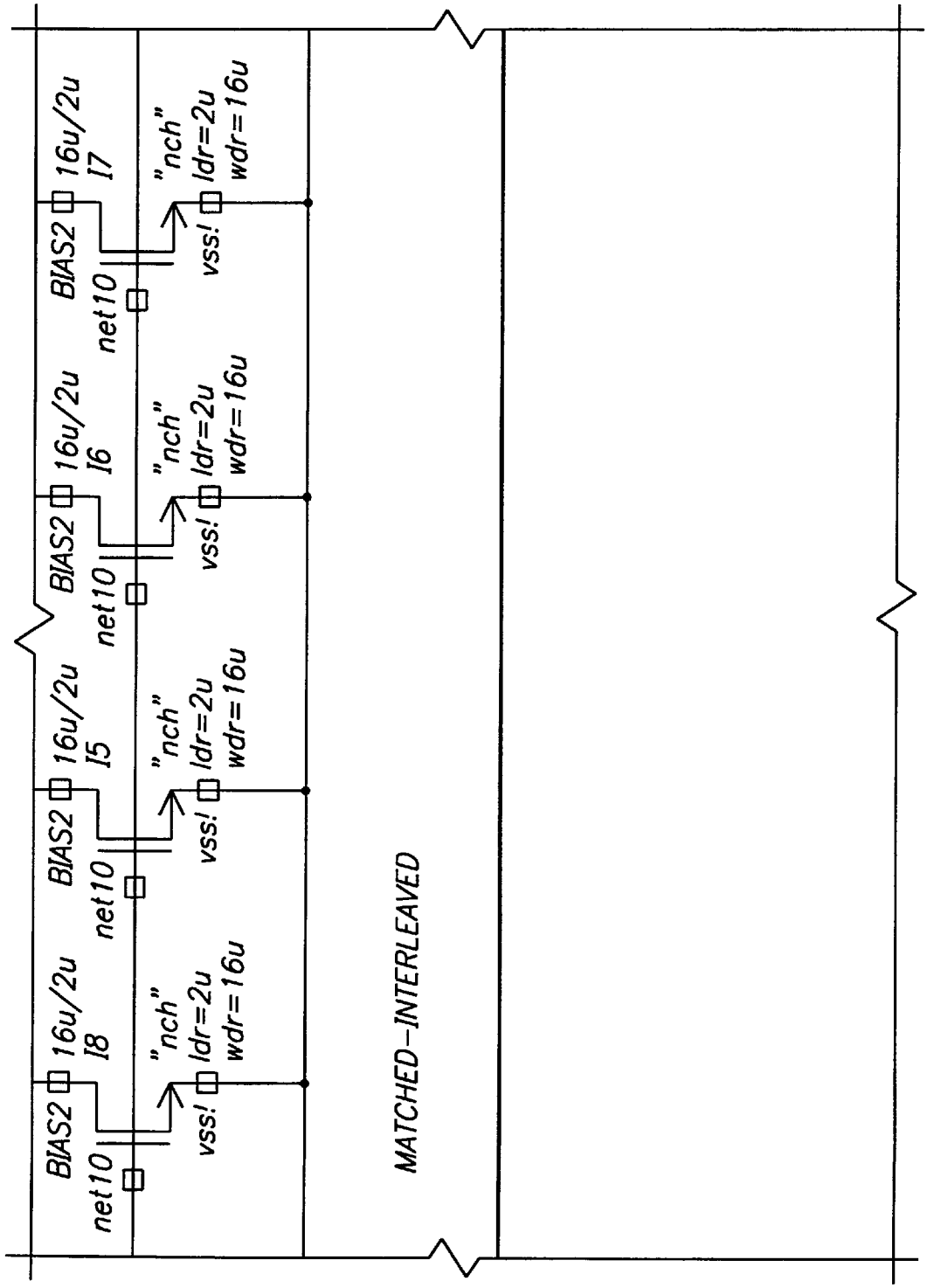

MATCHED–INTERLEAVED
BIAS2
net10
16u/2u
I8
I5
I6
I7
"nch"
ldr=2u
wdr=16u
vss!

FIG 99

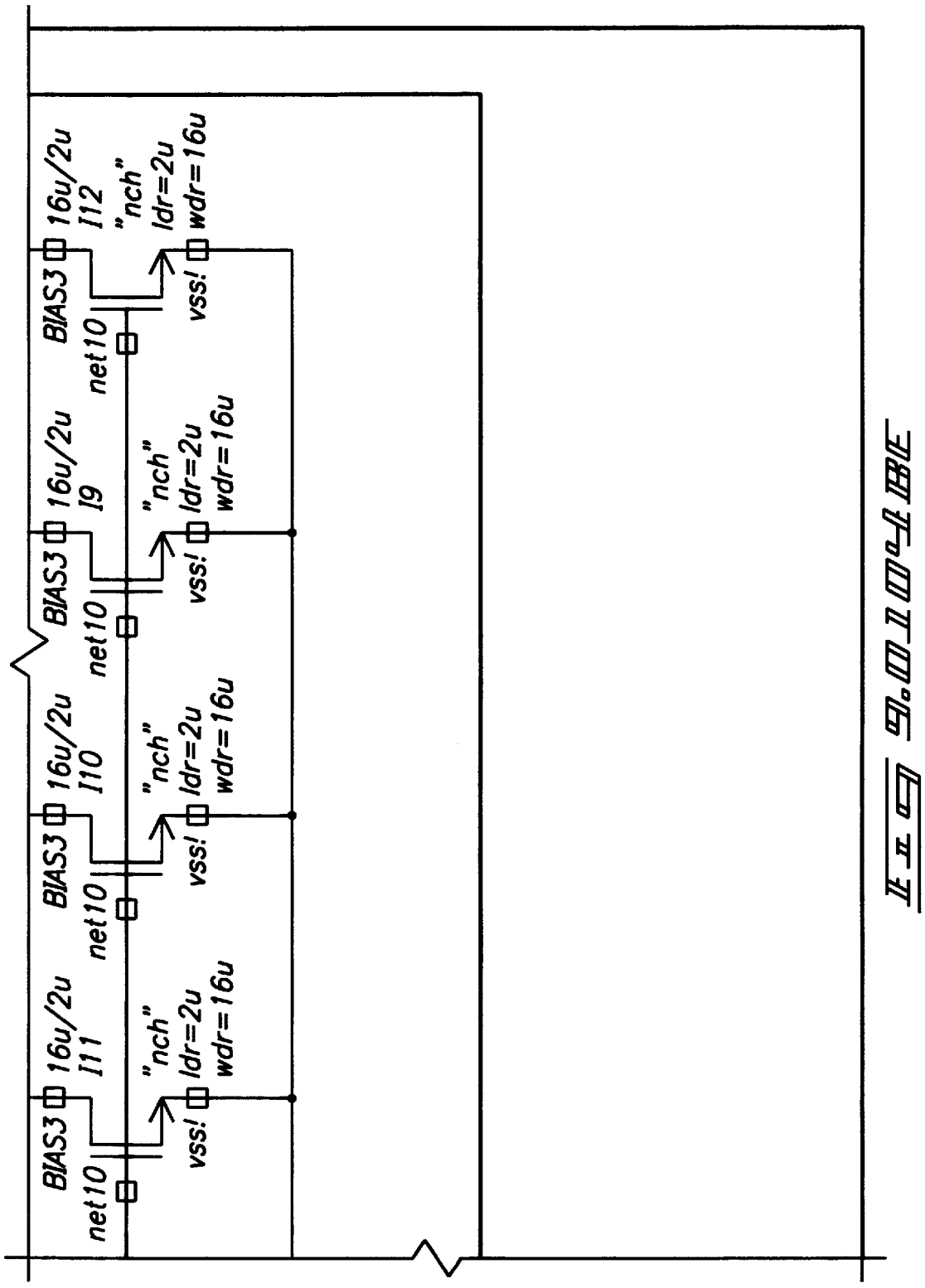

BIAS3
net10
16u/2u
I11
"nch"
ldr=2u
wdr=16u
vss!
BIAS3
net10
16u/2u
I10
"nch"
ldr=2u
wdr=16u
vss!
BIAS3
net10
16u/2u
I9
"nch"
ldr=2u
wdr=16u
vss!
BIAS3
net10
16u/2u
I12
"nch"
ldr=2u
wdr=16u
vss!

FIG 6,601

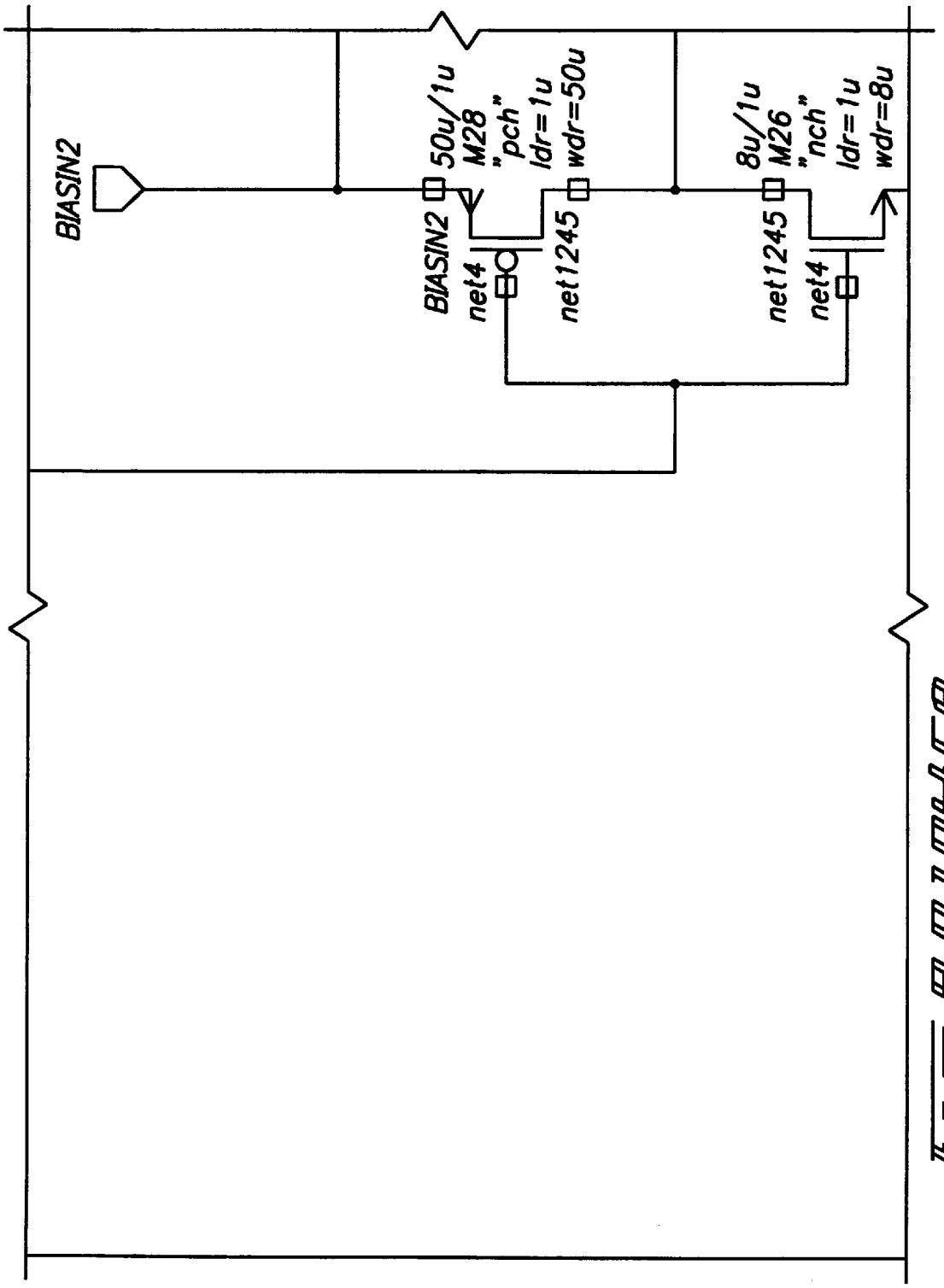

BIASIN2
50u/1u
M28
"pch"
ldr=1u
wdr=50u
8u/1u
M26
"nch"
ldr=1u
wdr=8u
BIASIN2
net4
net1245
net1245
net4

FIG 9.00176A

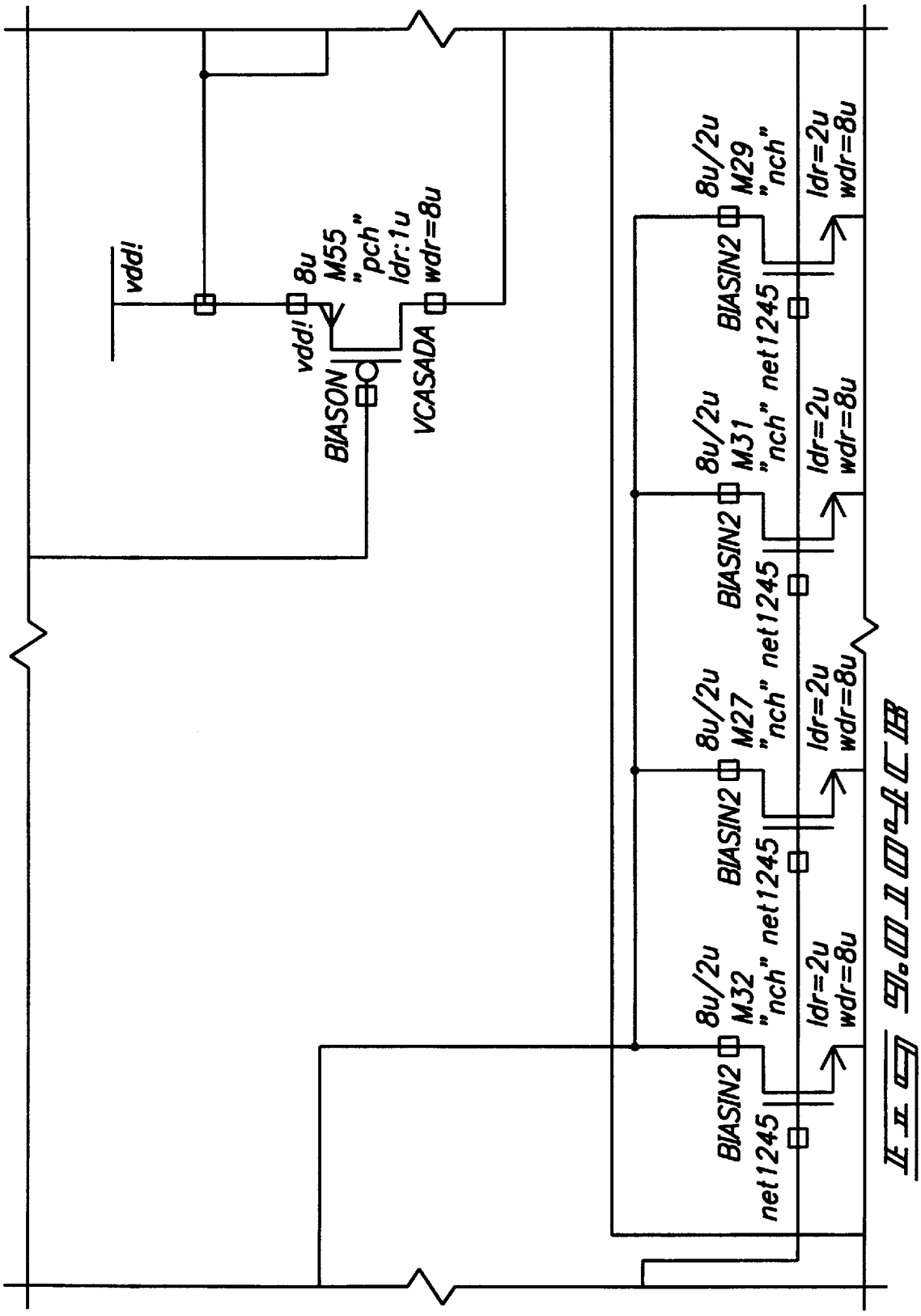

vdd!
8u
M55
"pch"
ldr:1u
wdr=8u
vdd!
BIASON
VCASADA
8u/2u
M29
"nch"
ldr=2u
wdr=8u
BIASIN2
net1245
8u/2u
M31
"nch"
net1245
ldr=2u
wdr=8u
BIASIN2
8u/2u
M27
"nch"
net1245
ldr=2u
wdr=8u
BIASIN2
8u/2u
M32
"nch"
net1245
ldr=2u
wdr=8u
BIASIN2
net1245

FIG. 2402

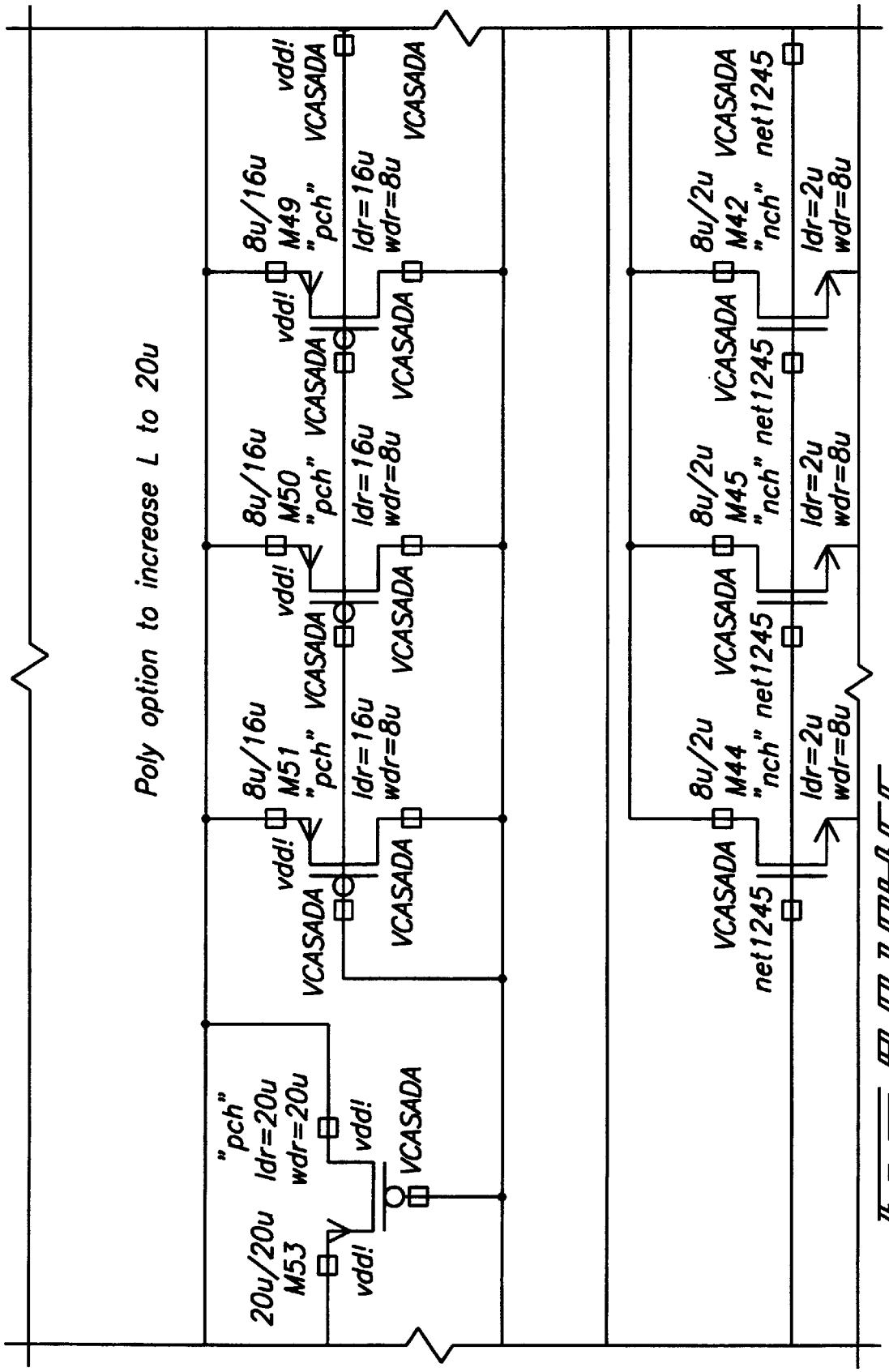
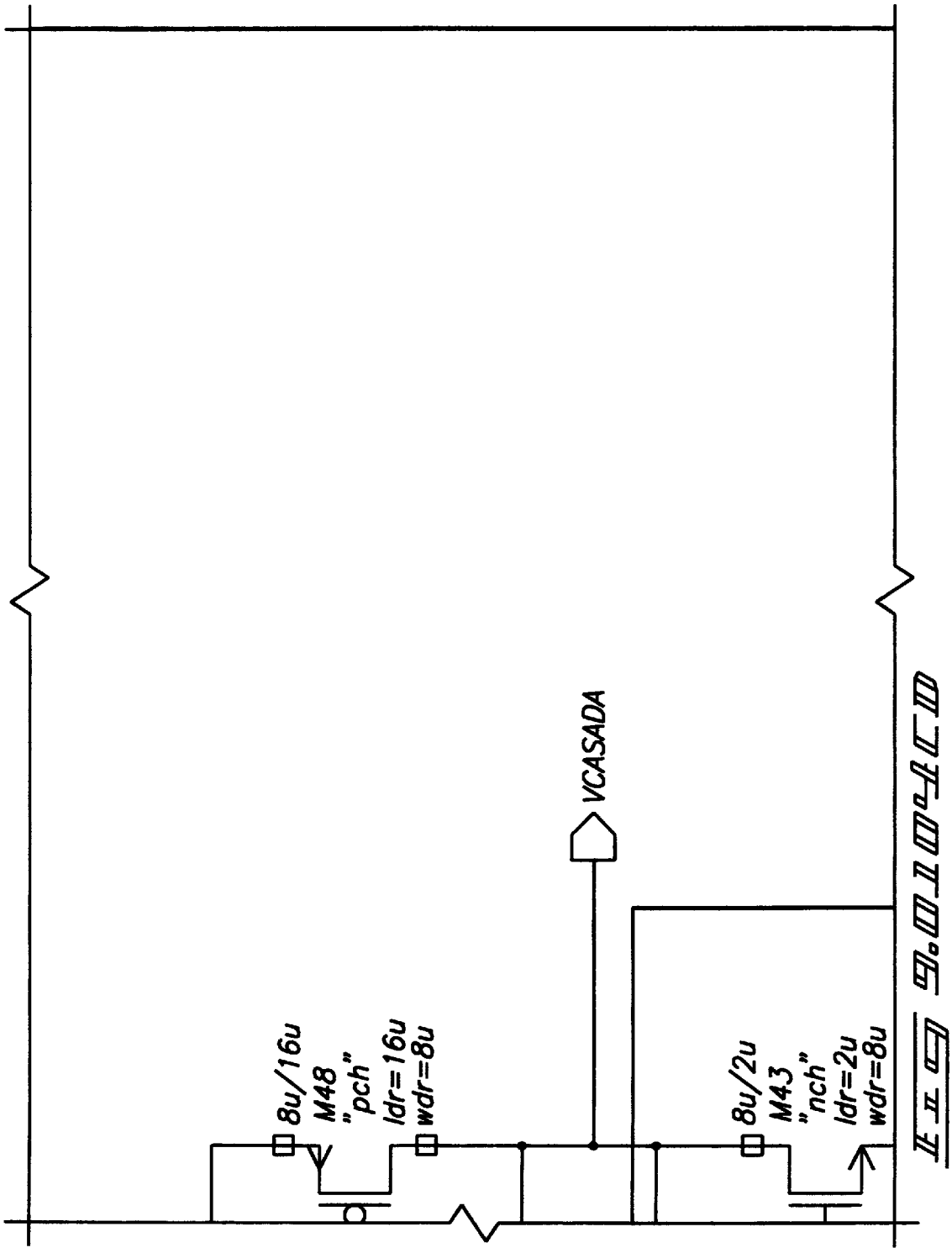

Poly option to increase L to 20u
20u/20u M53 "pch" ldr=20u wdr=20u vdd! VCASADA
8u/16u M51 "pch" ldr=16u wdr=8u vdd! VCASADA VCASADA
8u/16u M50 "pch" ldr=16u wdr=8u vdd! VCASADA VCASADA
8u/16u M49 "pch" ldr=16u wdr=8u vdd! VCASADA VCASADA
8u/2u M44 "nch" ldr=2u wdr=8u VCASADA net1245 VCASADA
8u/2u M45 "nch" ldr=2u wdr=8u VCASADA net1245 VCASADA
8u/2u M42 "nch" ldr=2u wdr=8u VCASADA net1245 VCASADA

FIG 59


VCASADA
8u/16u
M48
"pch"
ldr=16u
wdr=8u
8u/2u
M43
"nch"
ldr=2u
wdr=8u

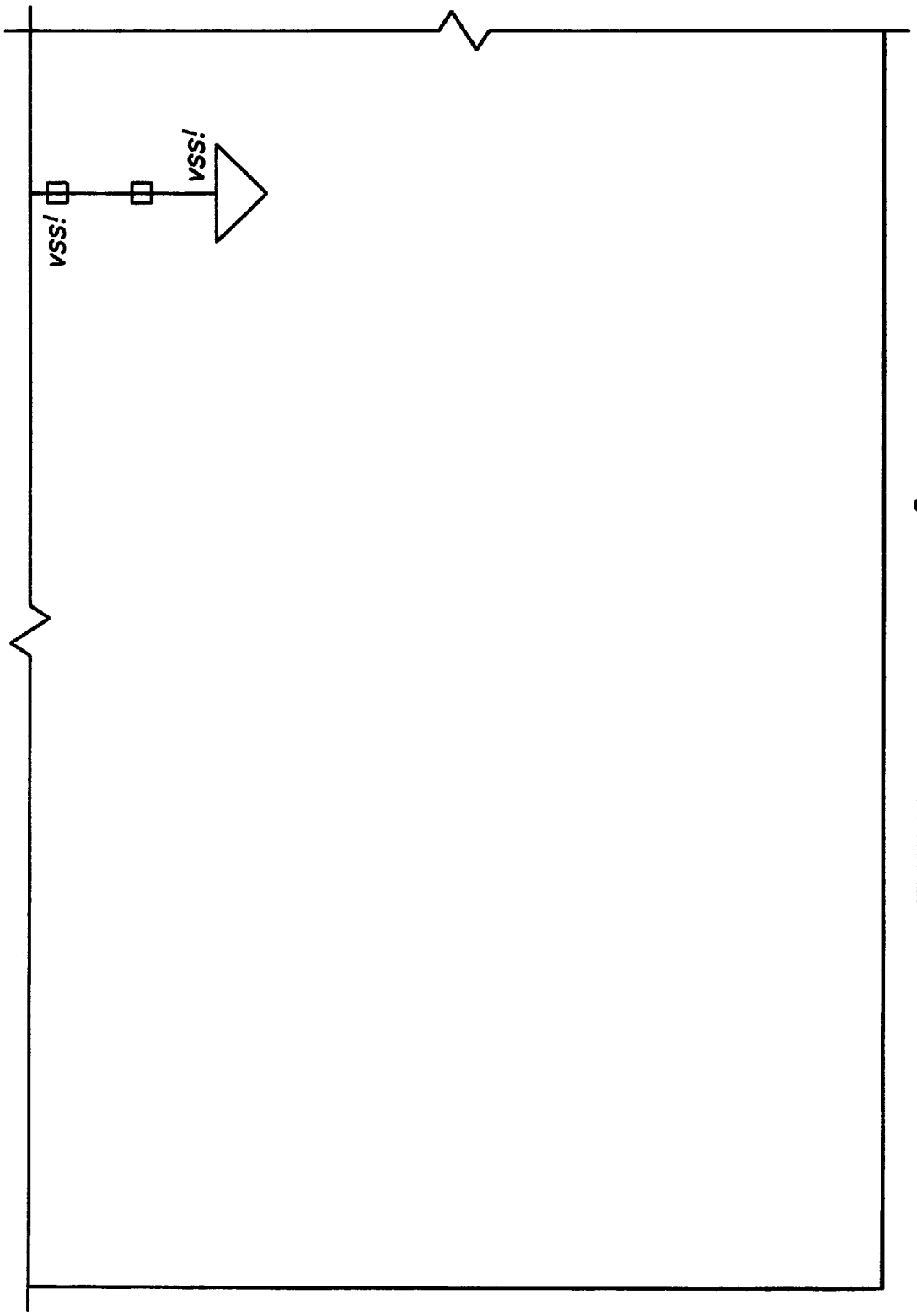


FIG 9,010,06

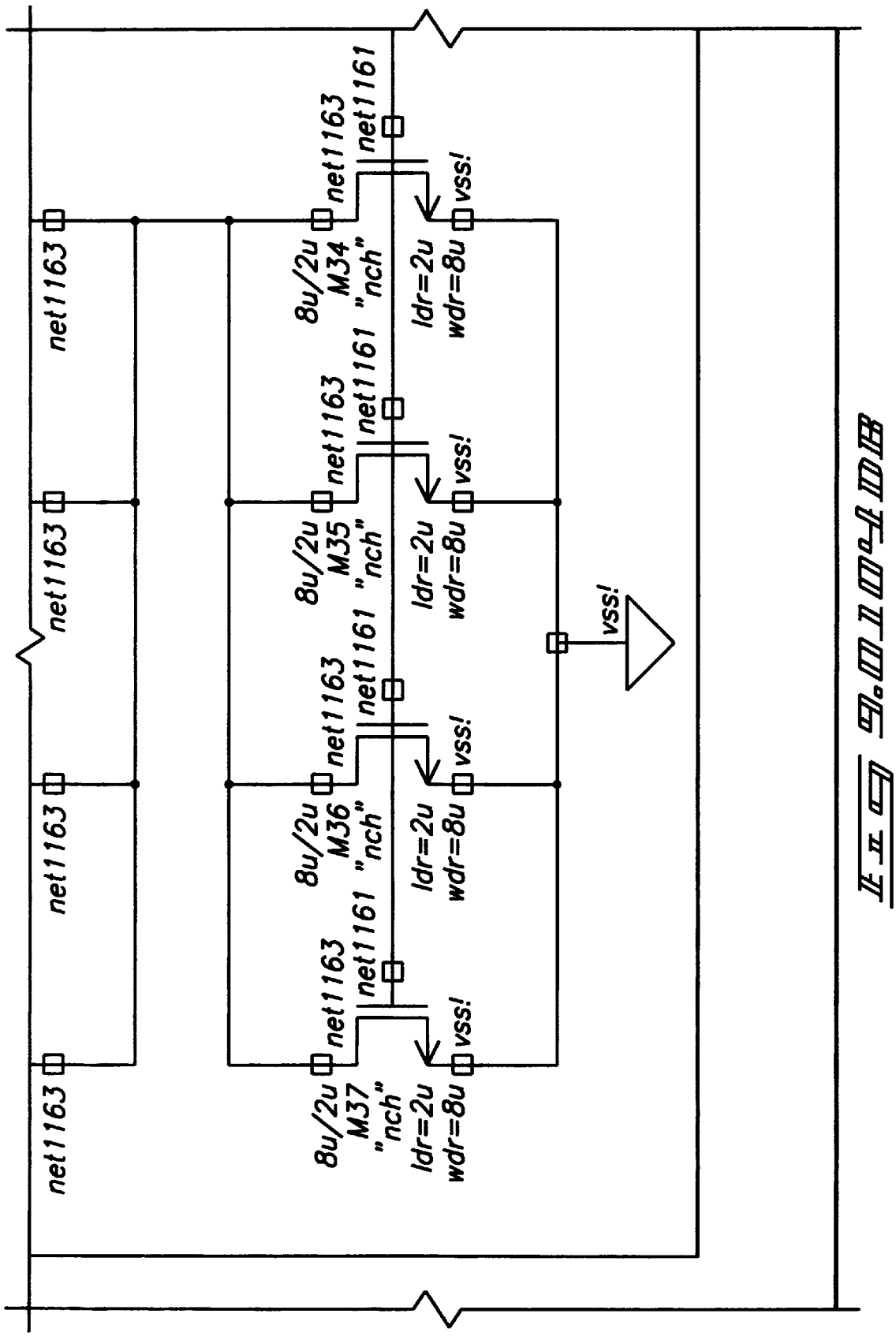

net1163
net1161
8u/2u
M34
"nch"
ldr=2u
wdr=8u
vss!
8u/2u
M35
"nch"
ldr=2u
wdr=8u
vss!
8u/2u
M36
"nch"
ldr=2u
wdr=8u
vss!
8u/2u
M37
"nch"
ldr=2u
wdr=8u
vss!

FIG. 9,011,008

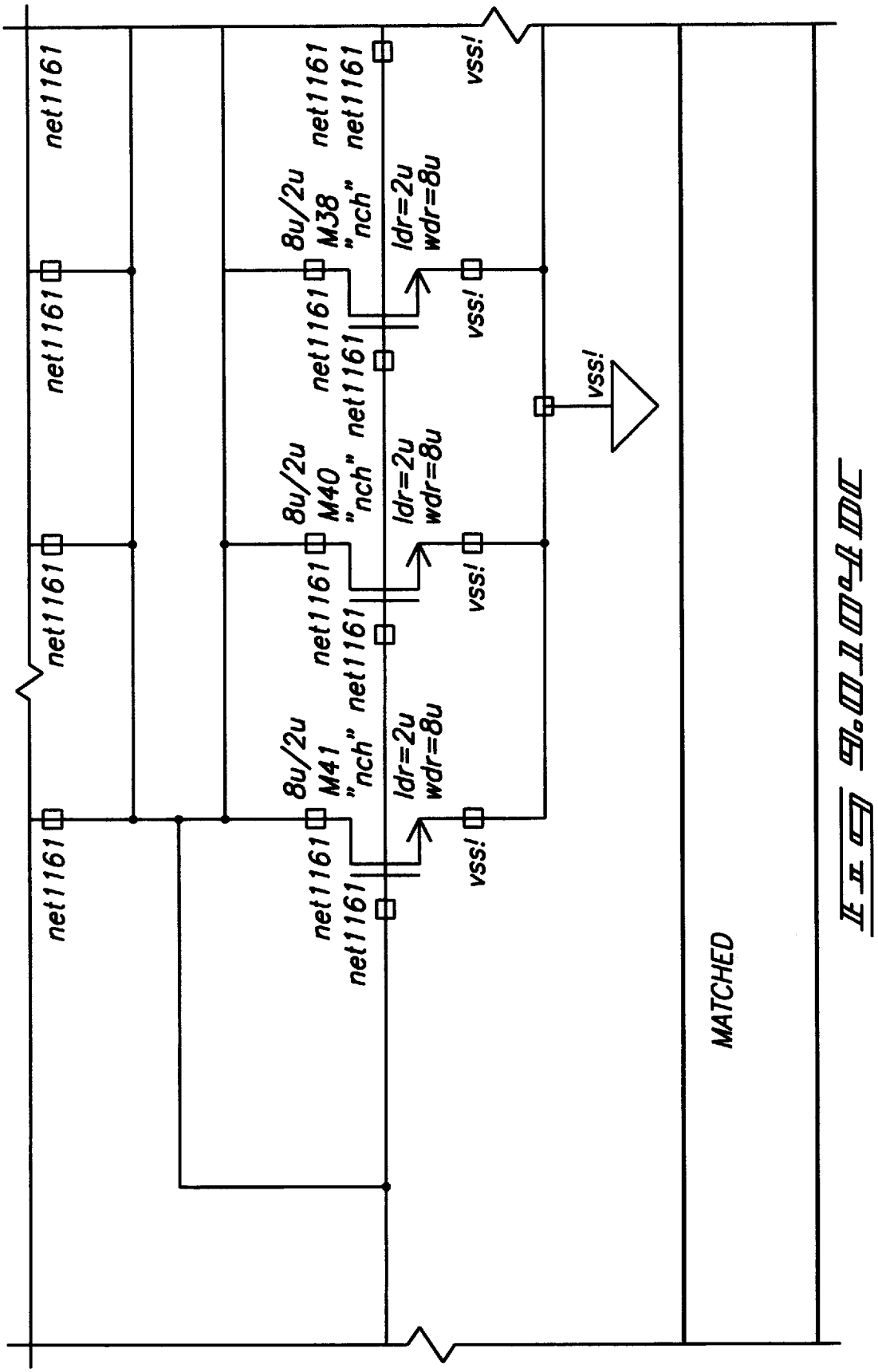

net1161
net1161
net1161
net1161
net1161
net1161
net1161
net1161
net1161
net1161
net1161
net1161
8u/2u
M38
"nch"
ldr=2u
wdr=8u
8u/2u
M40
"nch"
ldr=2u
wdr=8u
8u/2u
M41
"nch"
ldr=2u
wdr=8u
vss!
vss!
vss!
vss!
vss!
MATCHED

FIG 6,130,602

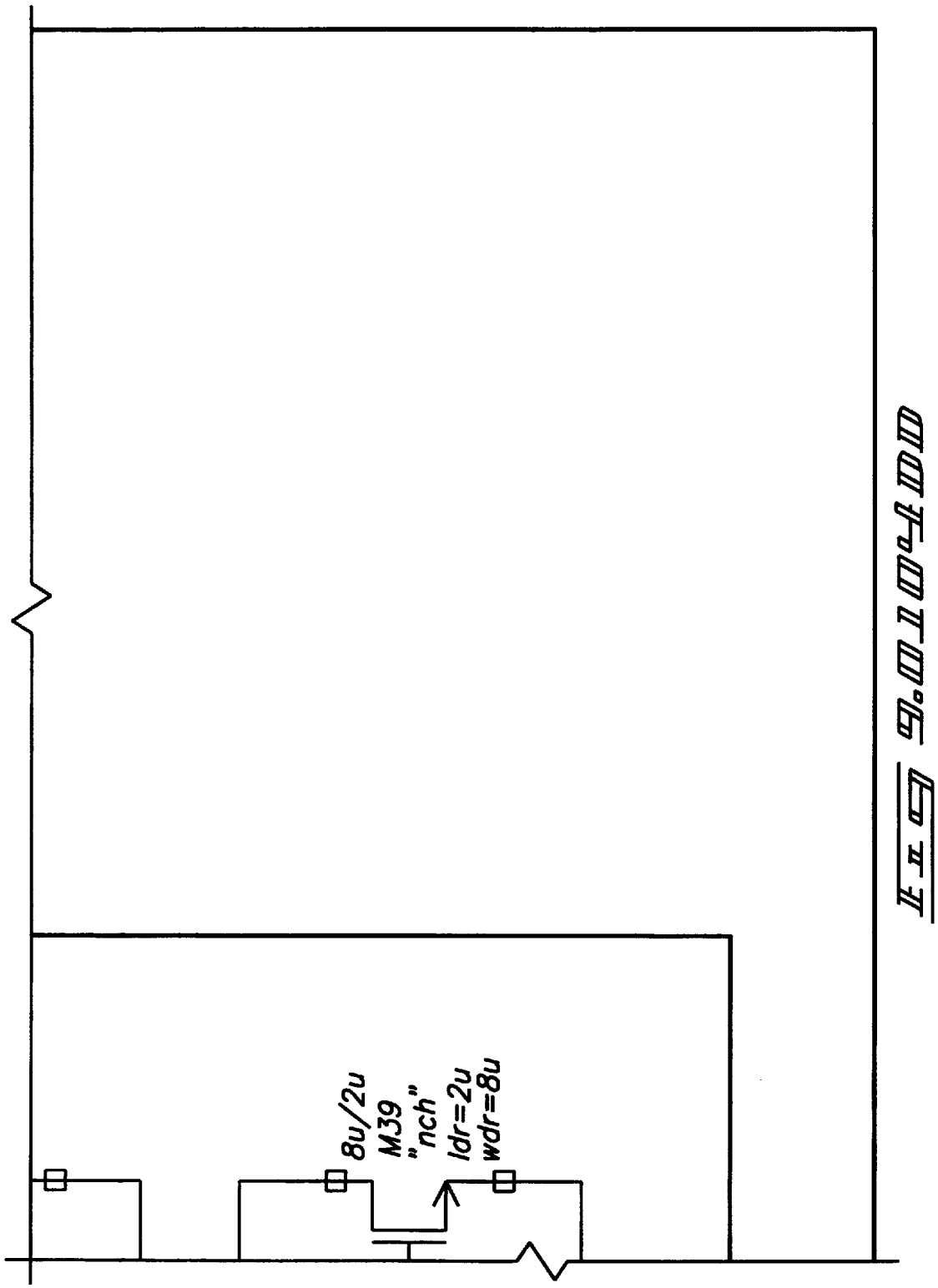


FIG 2408

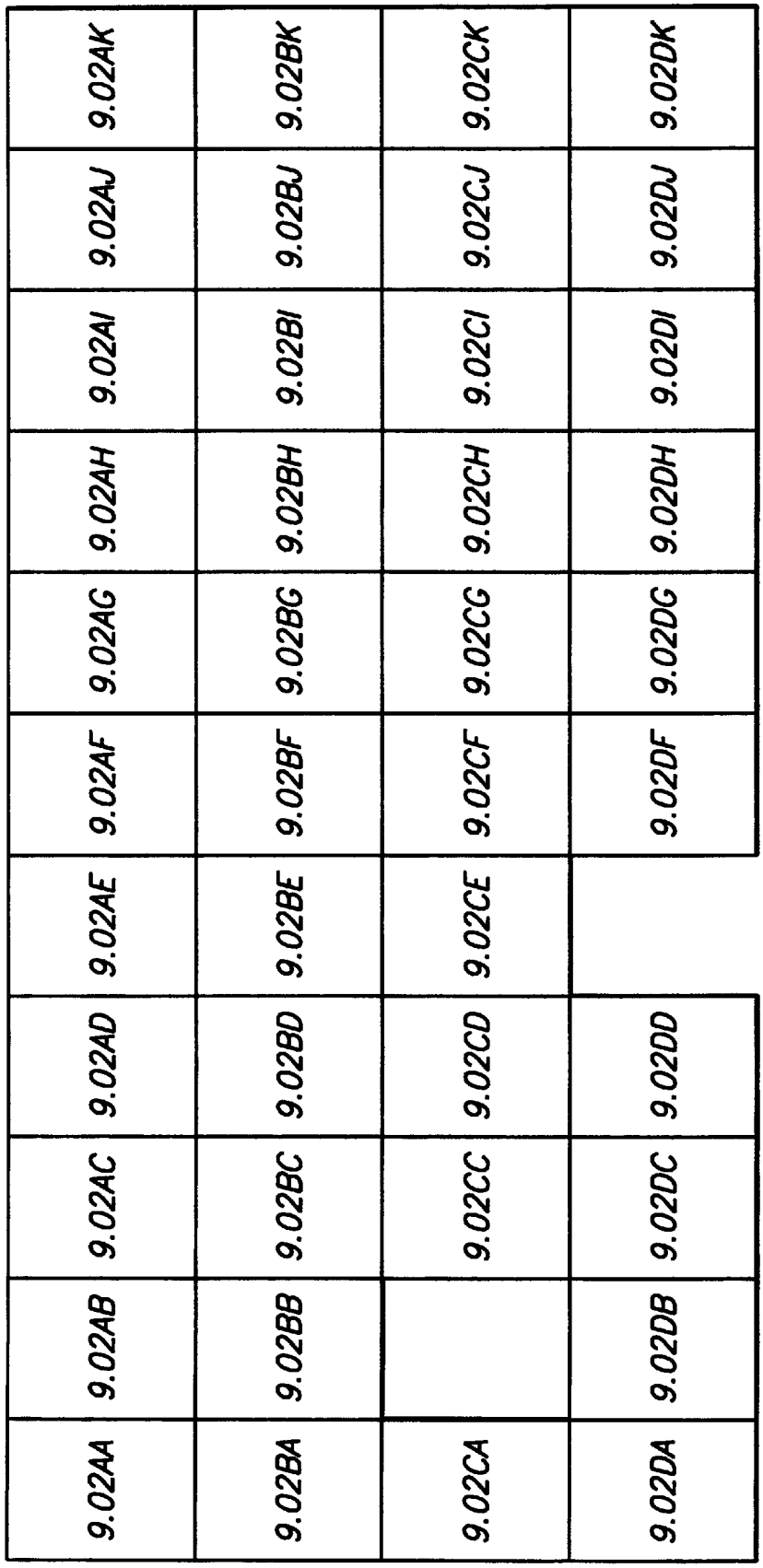

9.02AA 9.02AB 9.02AC 9.02AD 9.02AE 9.02AF 9.02AG 9.02AH 9.02AI 9.02AJ 9.02AK
9.02BA 9.02BB 9.02BC 9.02BD 9.02BE 9.02BF 9.02BG 9.02BH 9.02BI 9.02BJ 9.02BK
9.02CA 9.02CC 9.02CD 9.02CE 9.02CF 9.02CG 9.02CH 9.02CI 9.02CJ 9.02CK
9.02DA 9.02DB 9.02DC 9.02DD 9.02DF 9.02DG 9.02DH 9.02DI 9.02DJ 9.02DK

FIG. 9.02

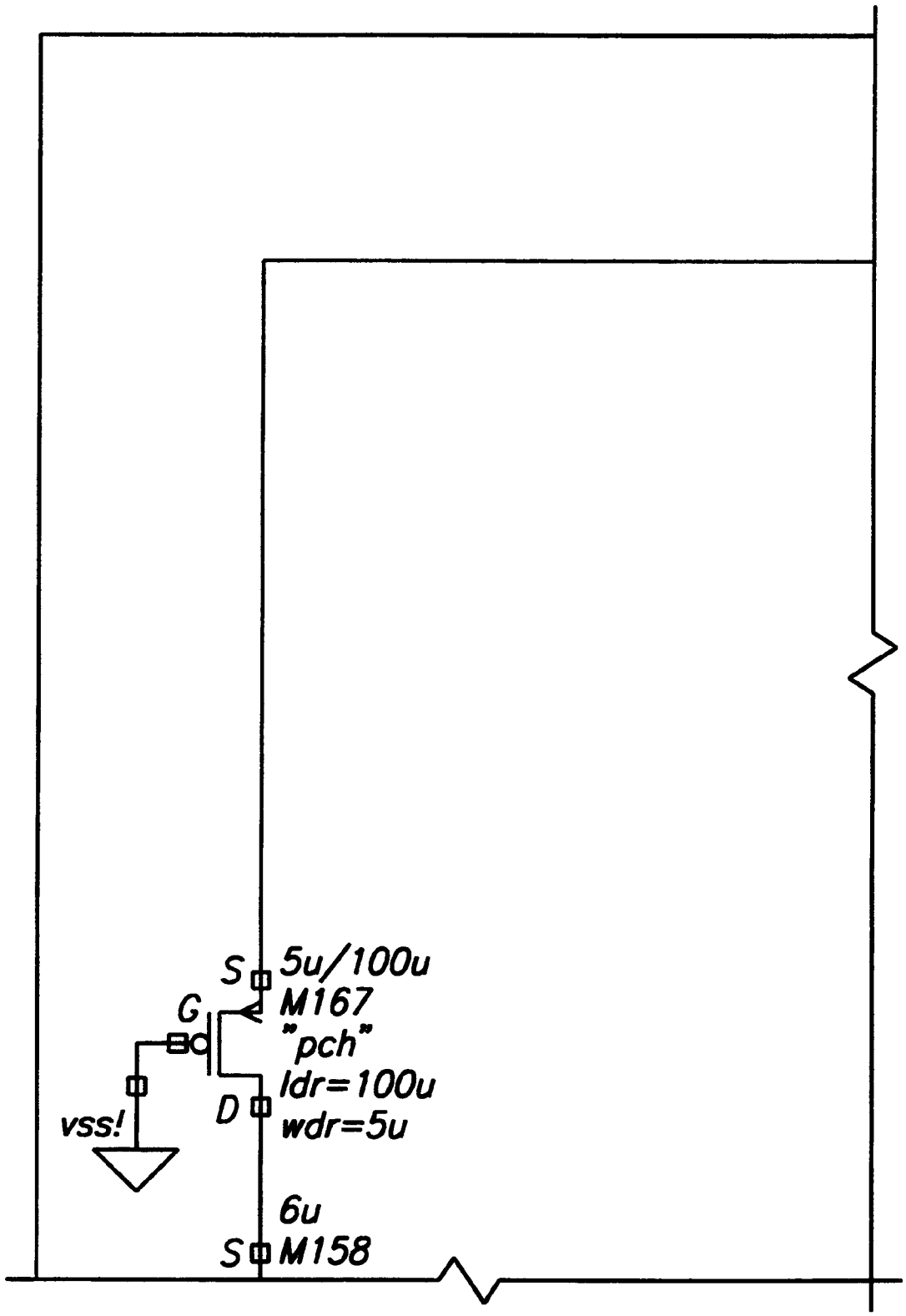


Fig 9.02AA

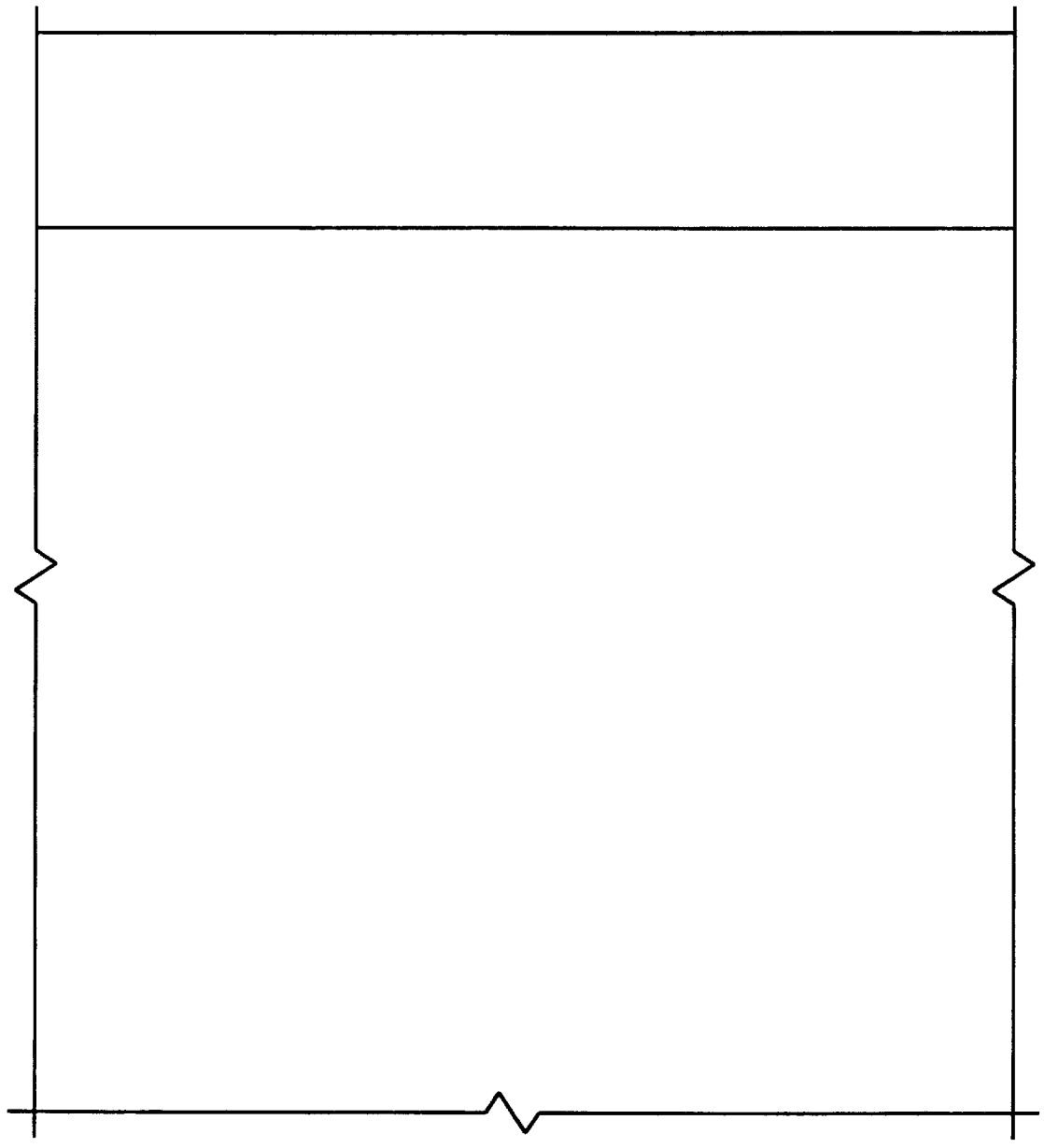


Fig 9.02AB

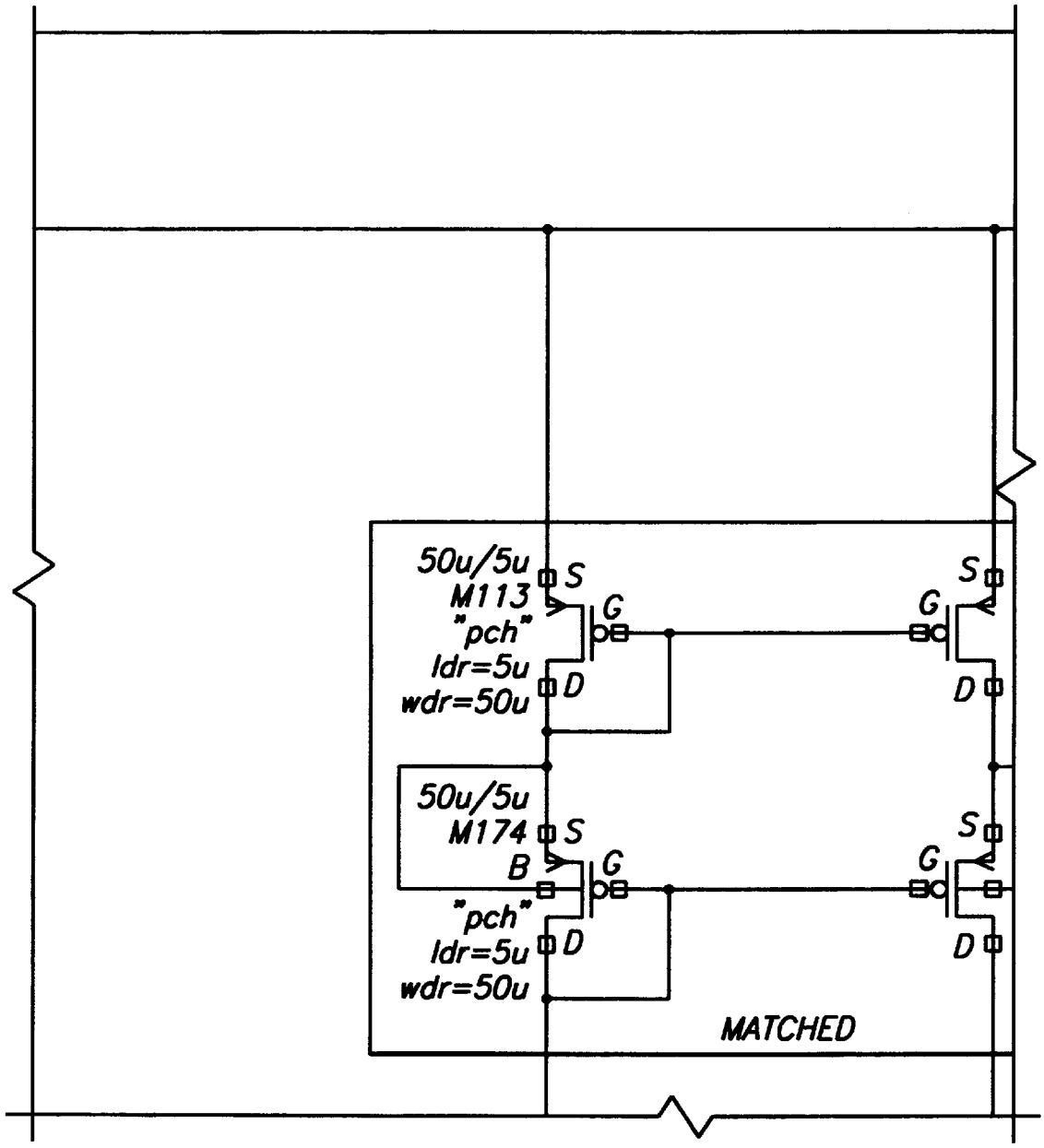

50u/5u
M113
"pch"
ldr=5u
wdr=50u
S
G
D
50u/5u
M174
B
"pch"
ldr=5u
wdr=50u
MATCHED

Fig 9.02AC

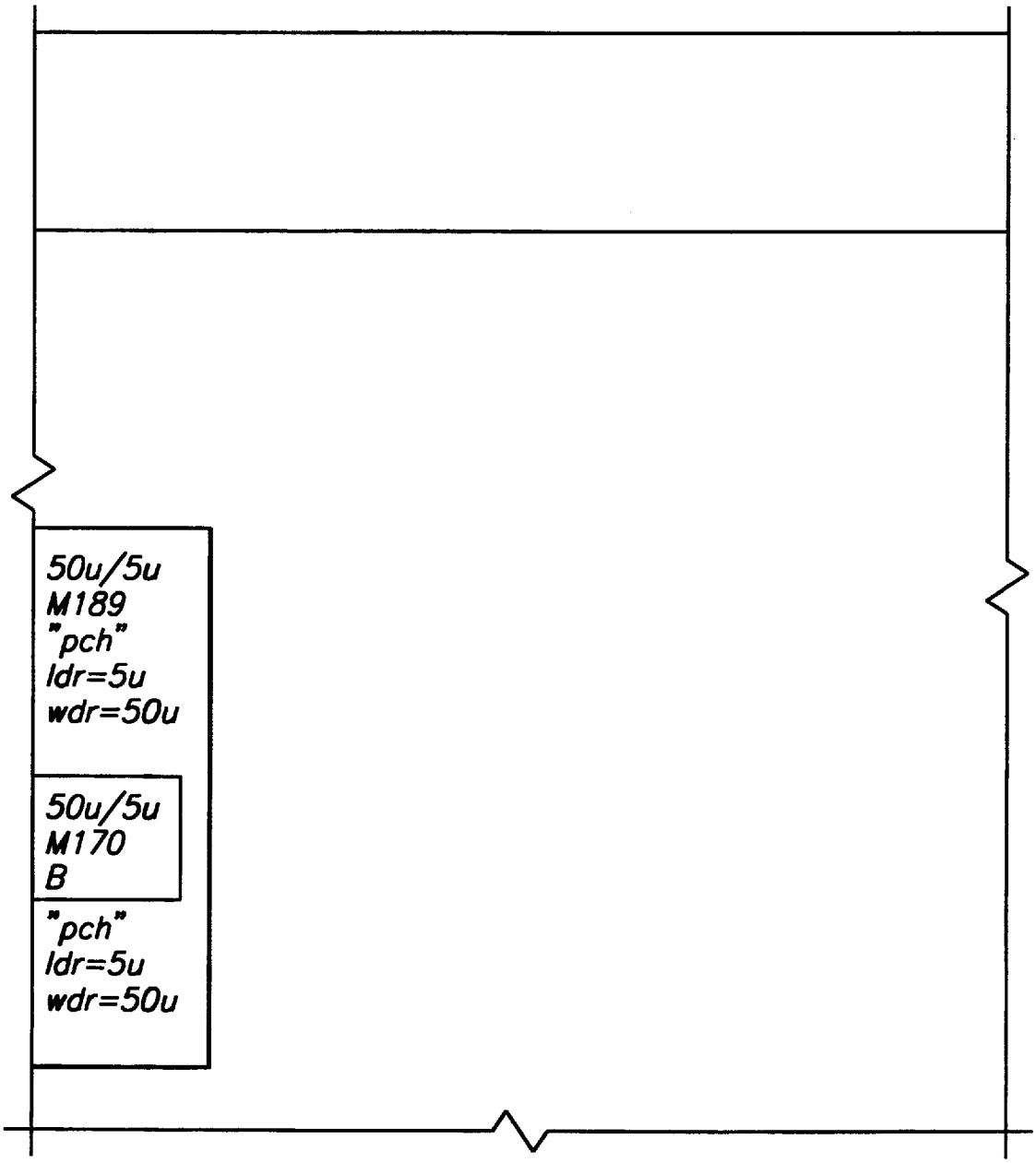


Fig 9.02AD

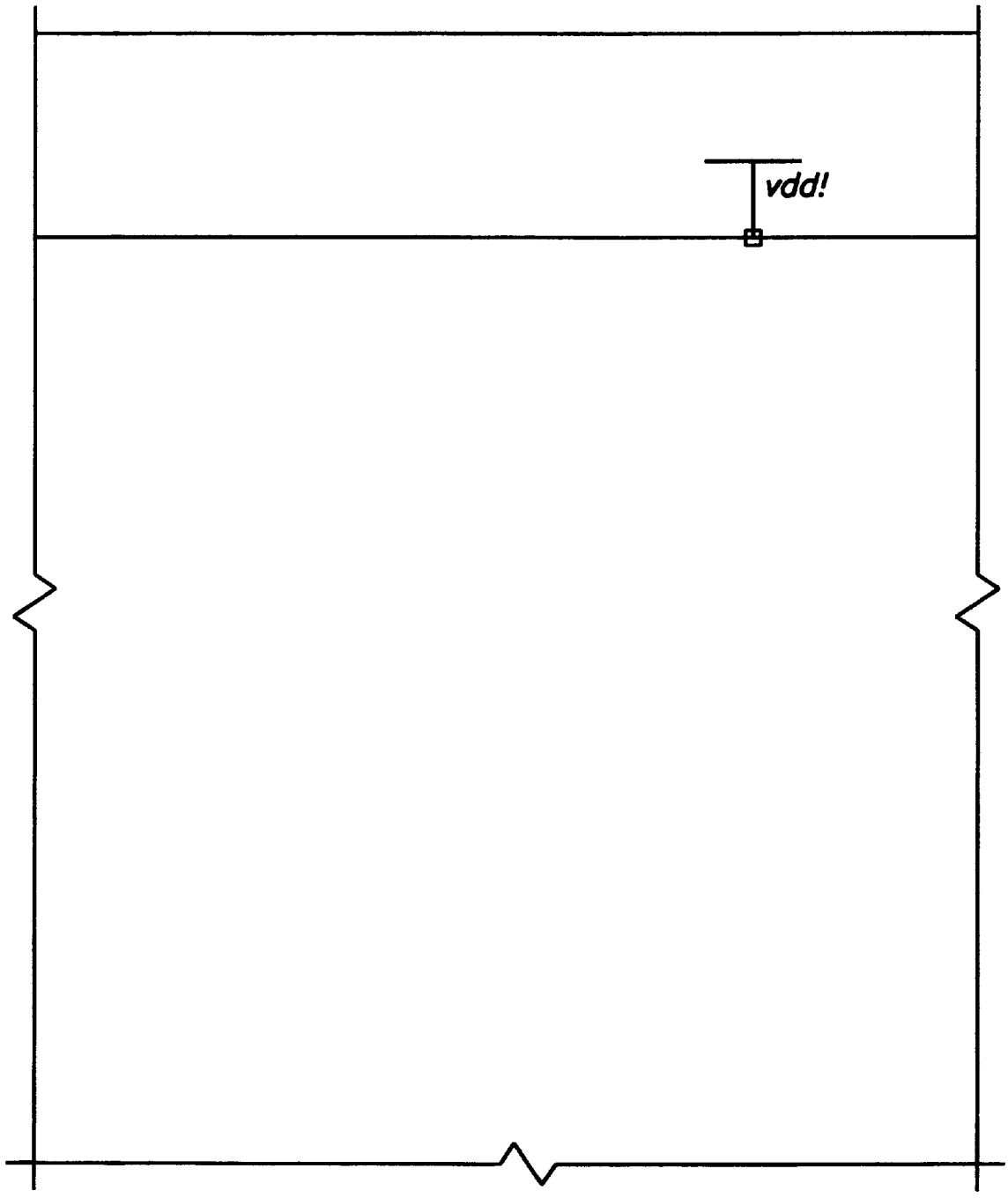


Fig 9.02AE

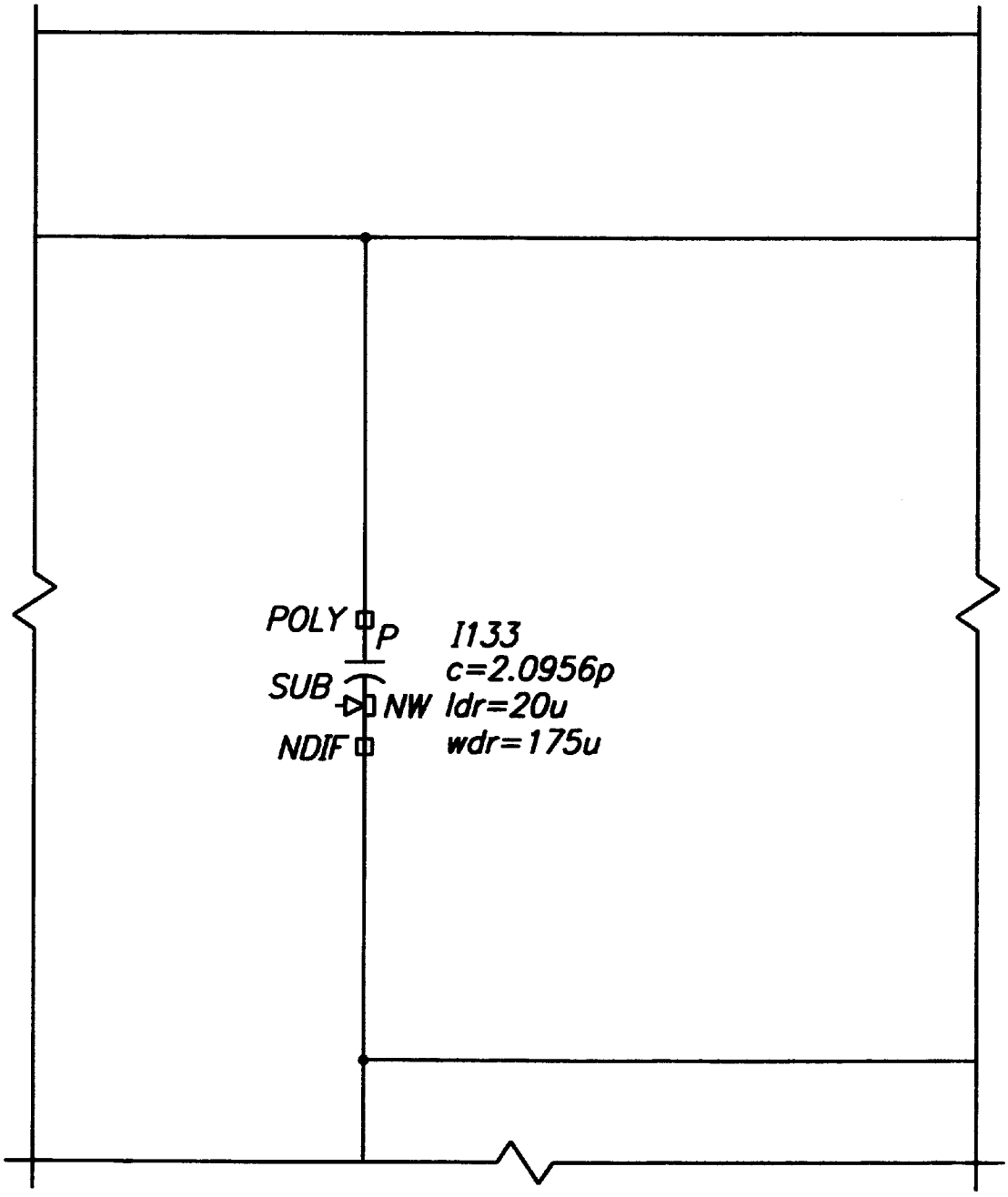


Fig 9.02AF

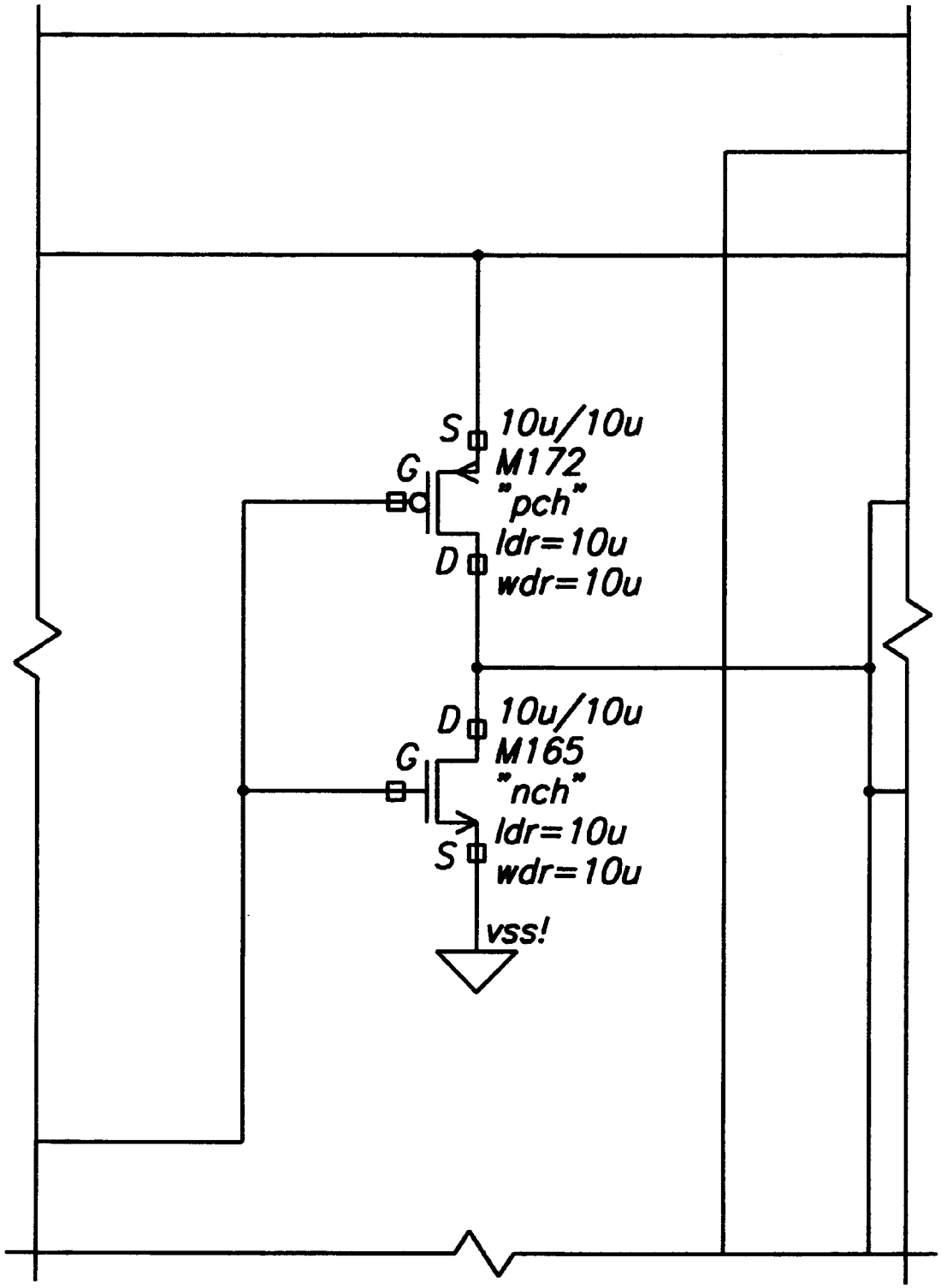

S
10u/10u
M172
"pch"
ldr=10u
wdr=10u
G
D
D
10u/10u
M165
"nch"
ldr=10u
wdr=10u
G
S
vss!

Fig 9.02AG

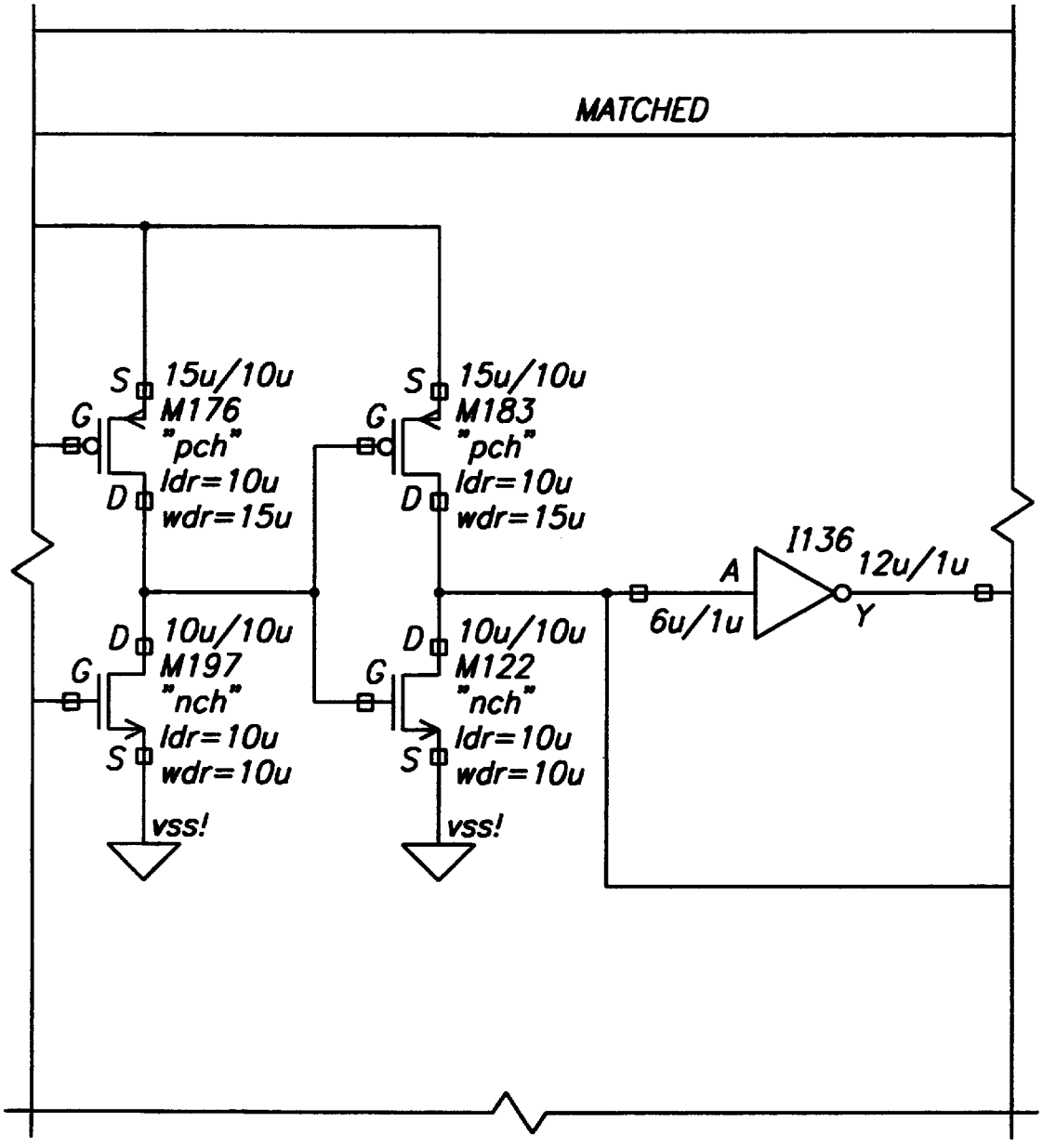

MATCHED
S
15u/10u
M176
"pch"
ldr=10u
wdr=15u
G
D
S
15u/10u
M183
"pch"
ldr=10u
wdr=15u
G
D
I136
A
12u/1u
Y
6u/1u
D
10u/10u
M197
"nch"
ldr=10u
wdr=10u
G
S
vss!
D
10u/10u
M122
"nch"
ldr=10u
wdr=10u
G
S
vss!

Fig 9.02AH

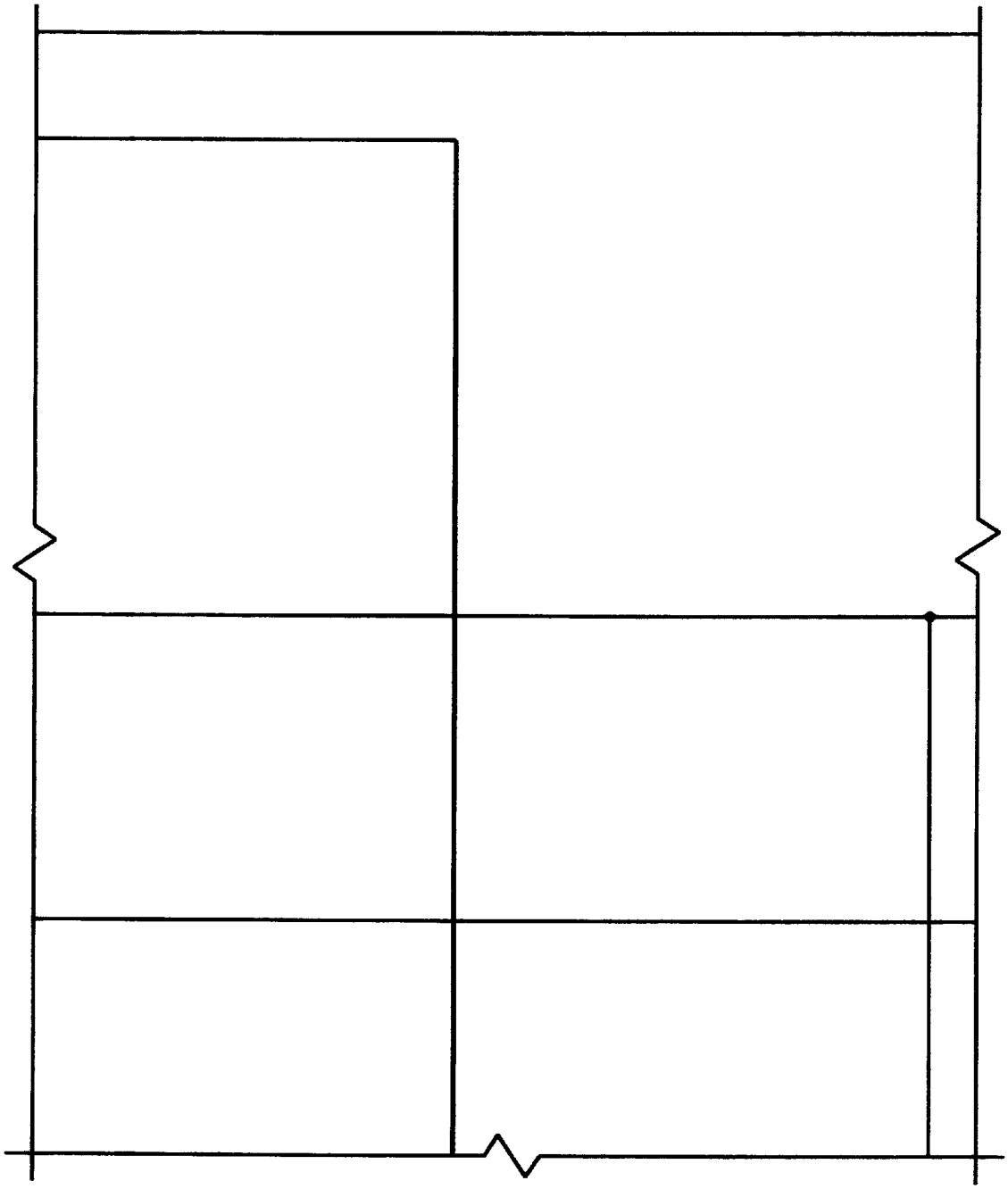


Fig 9.02AII

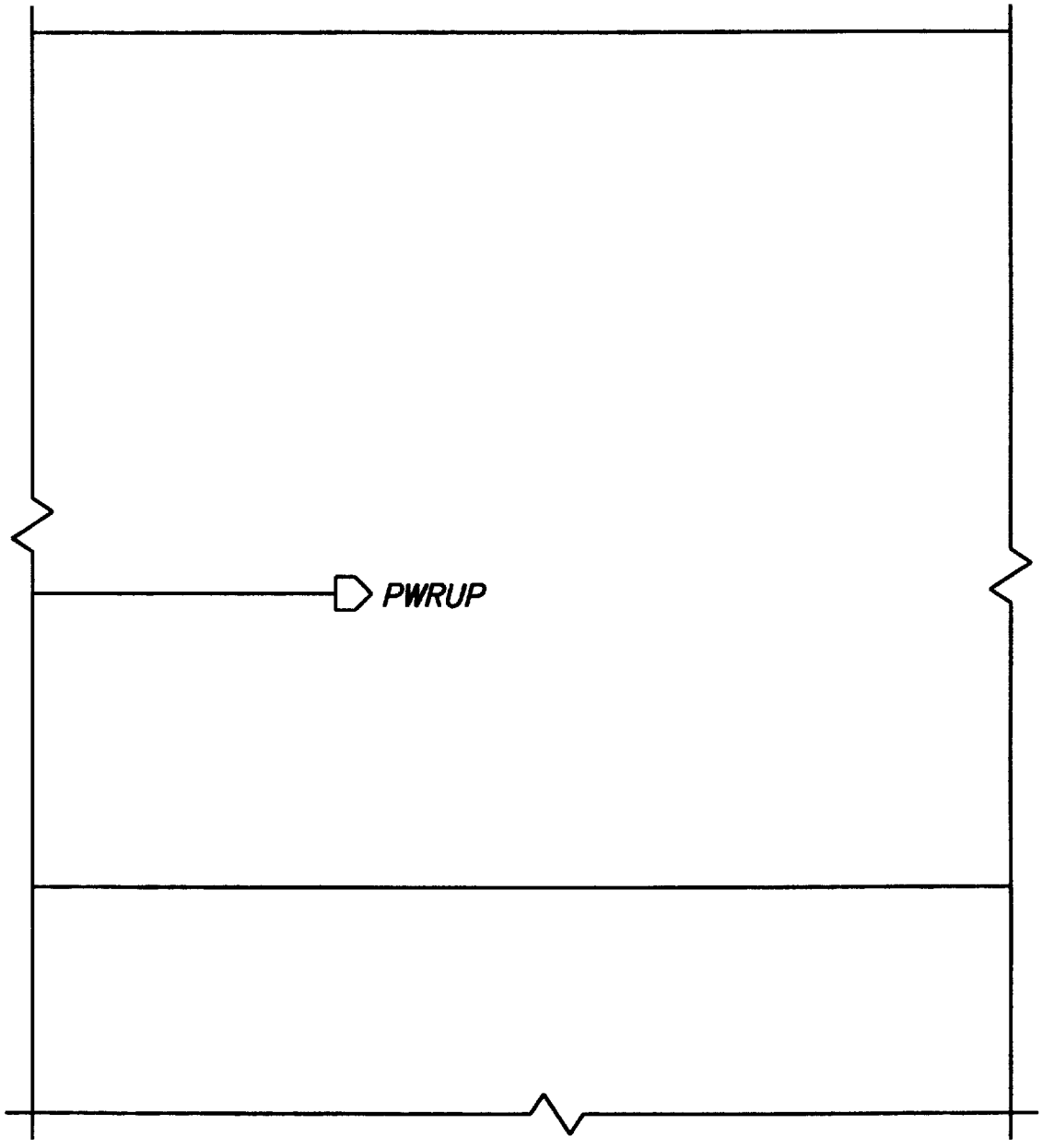


Fig 9.02Aol

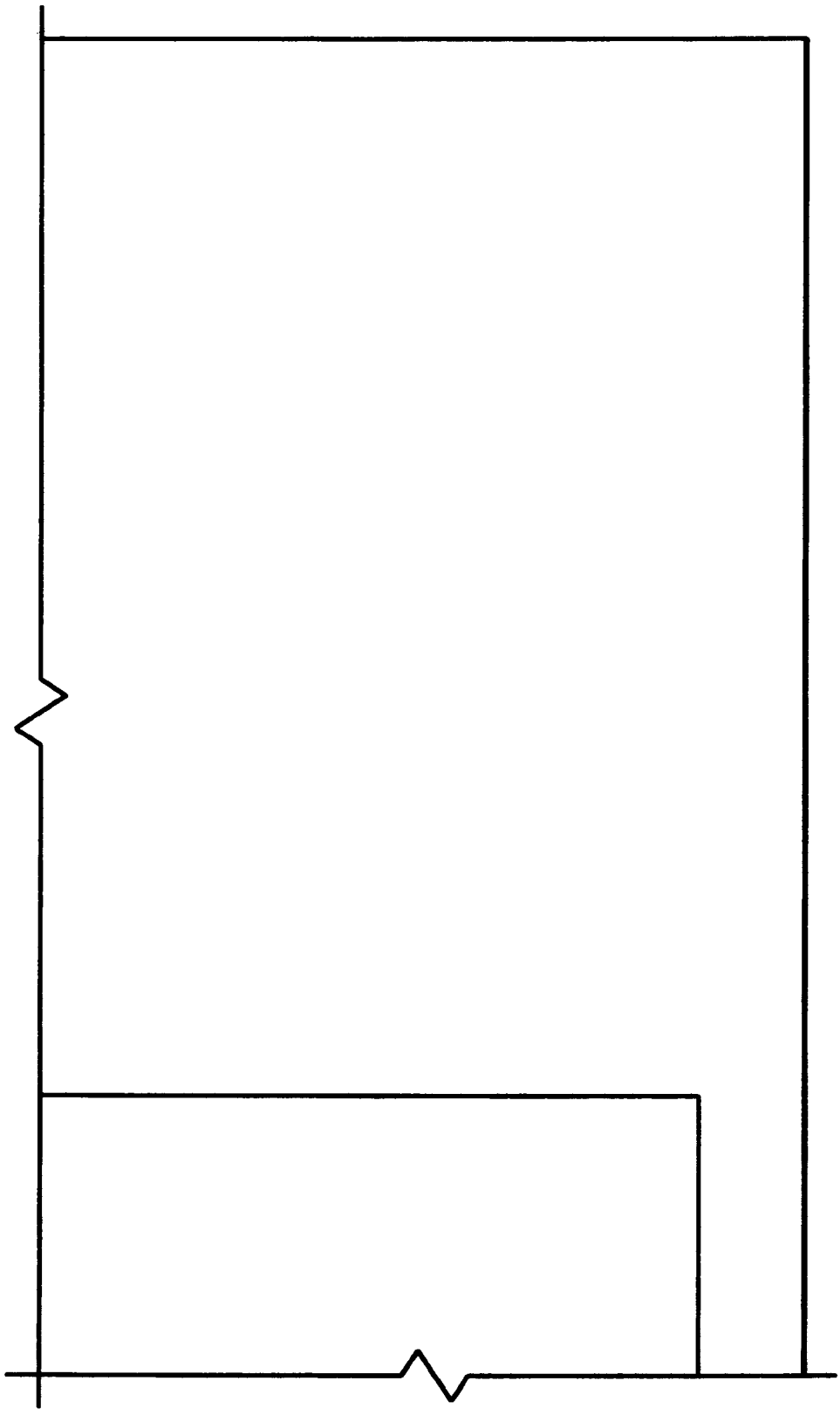


Fig 9.02AK

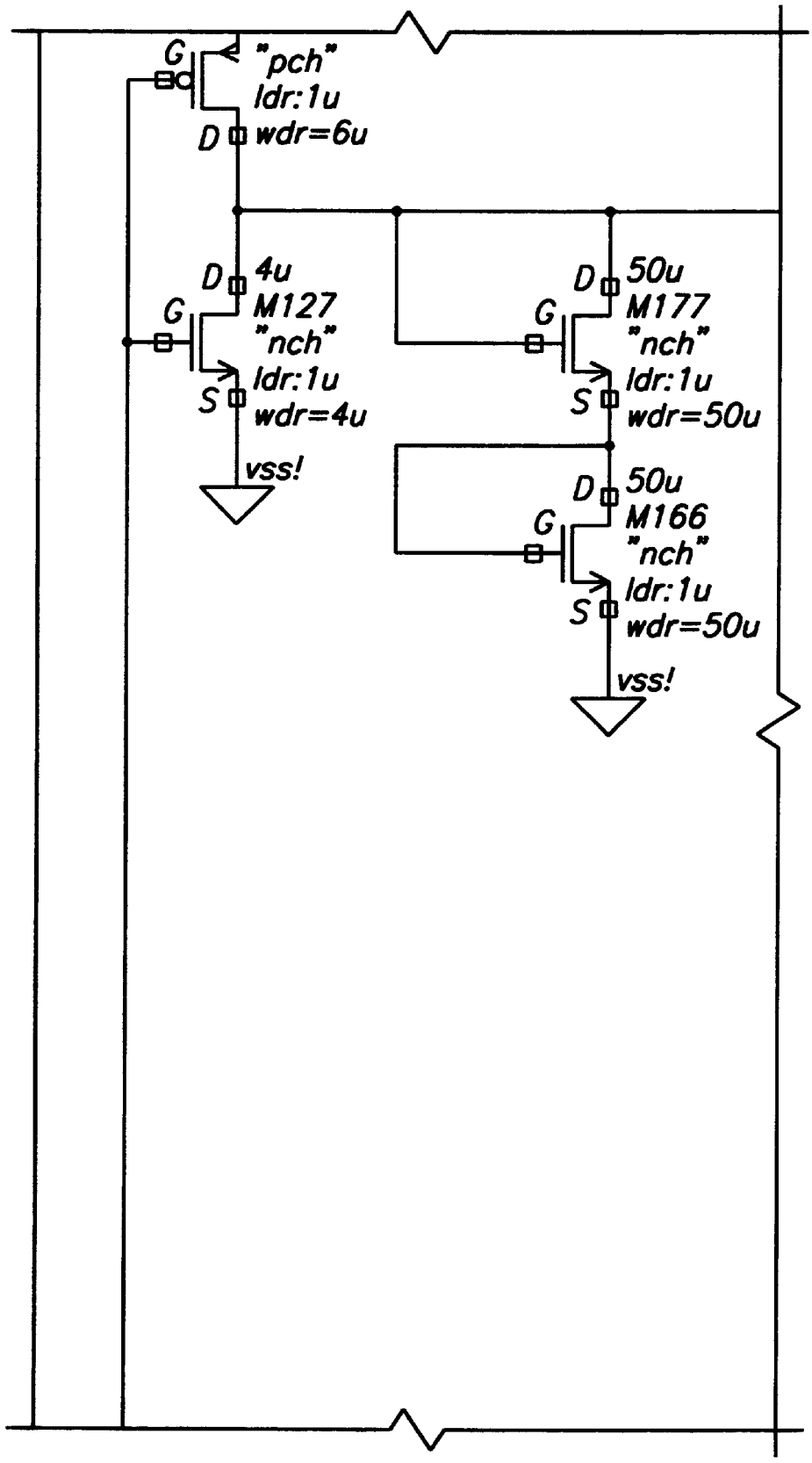

G
"pch"
ldr:1u
D
wdr=6u
D
4u
M127
G
"nch"
ldr:1u
S
wdr=4u
vss!
D
50u
M177
G
"nch"
ldr:1u
S
wdr=50u
D
50u
M166
G
"nch"
ldr:1u
S
wdr=50u
vss!

Fig 9.02BA

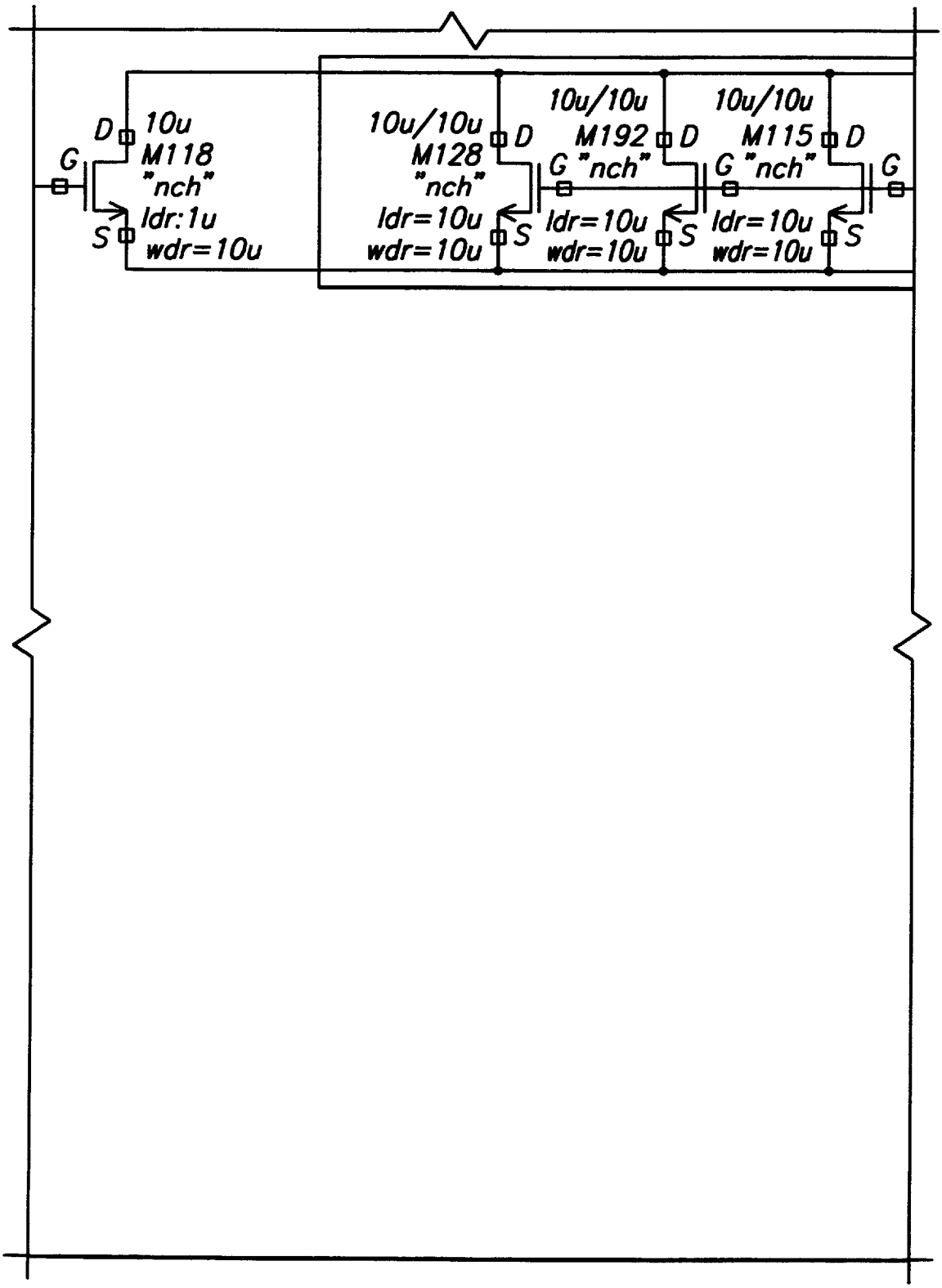

D
10u
M118
"nch"
G
S
ldr:1u
wdr=10u
10u/10u
M128
"nch"
D
S
ldr=10u
wdr=10u
10u/10u
M192
"nch"
G
D
S
ldr=10u
wdr=10u
10u/10u
M115
"nch"
G
D
S
ldr=10u
wdr=10u
G

Fig 9.02BB

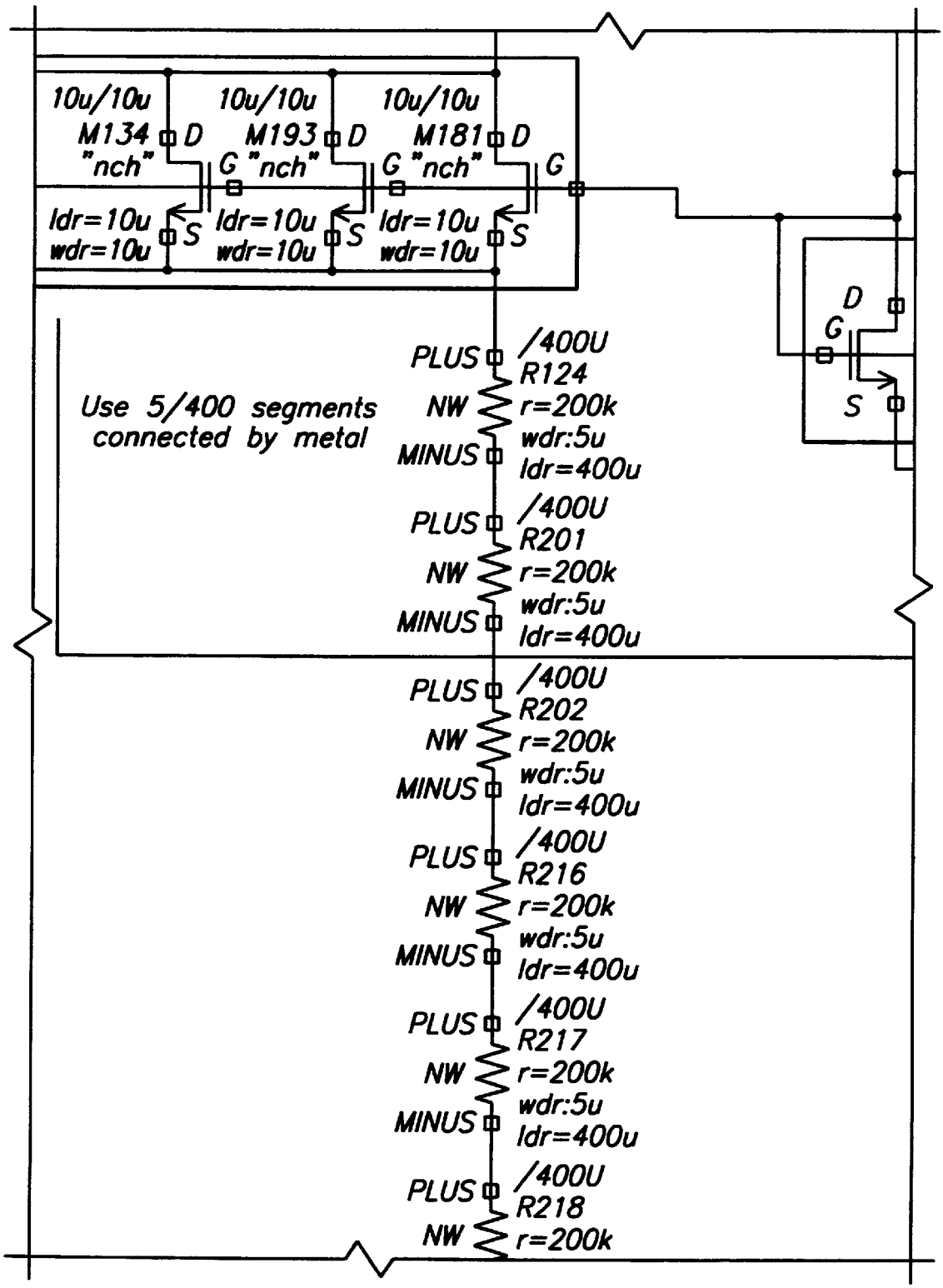

10u/10u
M134
"nch"
D
G
S
ldr=10u
wdr=10u
10u/10u
M193
"nch"
10u/10u
M181
"nch"
Use 5/400 segments
connected by metal
PLUS
NW
MINUS
/400U
R124
r=200k
wdr:5u
ldr=400u
R201
R202
R216
R217
R218

Fig 9.02BC

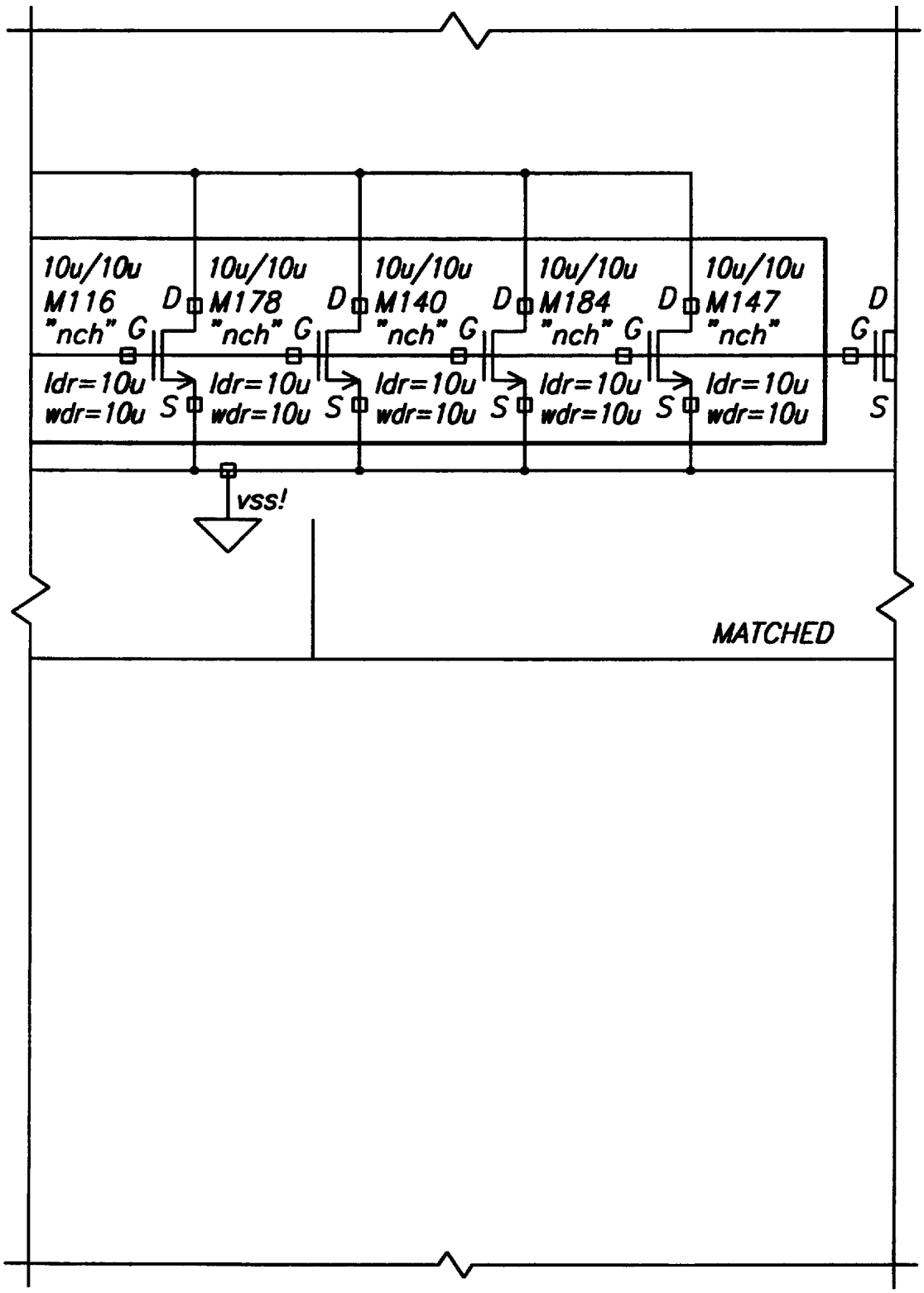

10u/10u
M116
"nch"
ldr=10u
wdr=10u
10u/10u
M178
"nch"
ldr=10u
wdr=10u
10u/10u
M140
"nch"
ldr=10u
wdr=10u
10u/10u
M184
"nch"
ldr=10u
wdr=10u
10u/10u
M147
"nch"
ldr=10u
wdr=10u
D
G
S
vss!
MATCHED

Fig 9.02BD

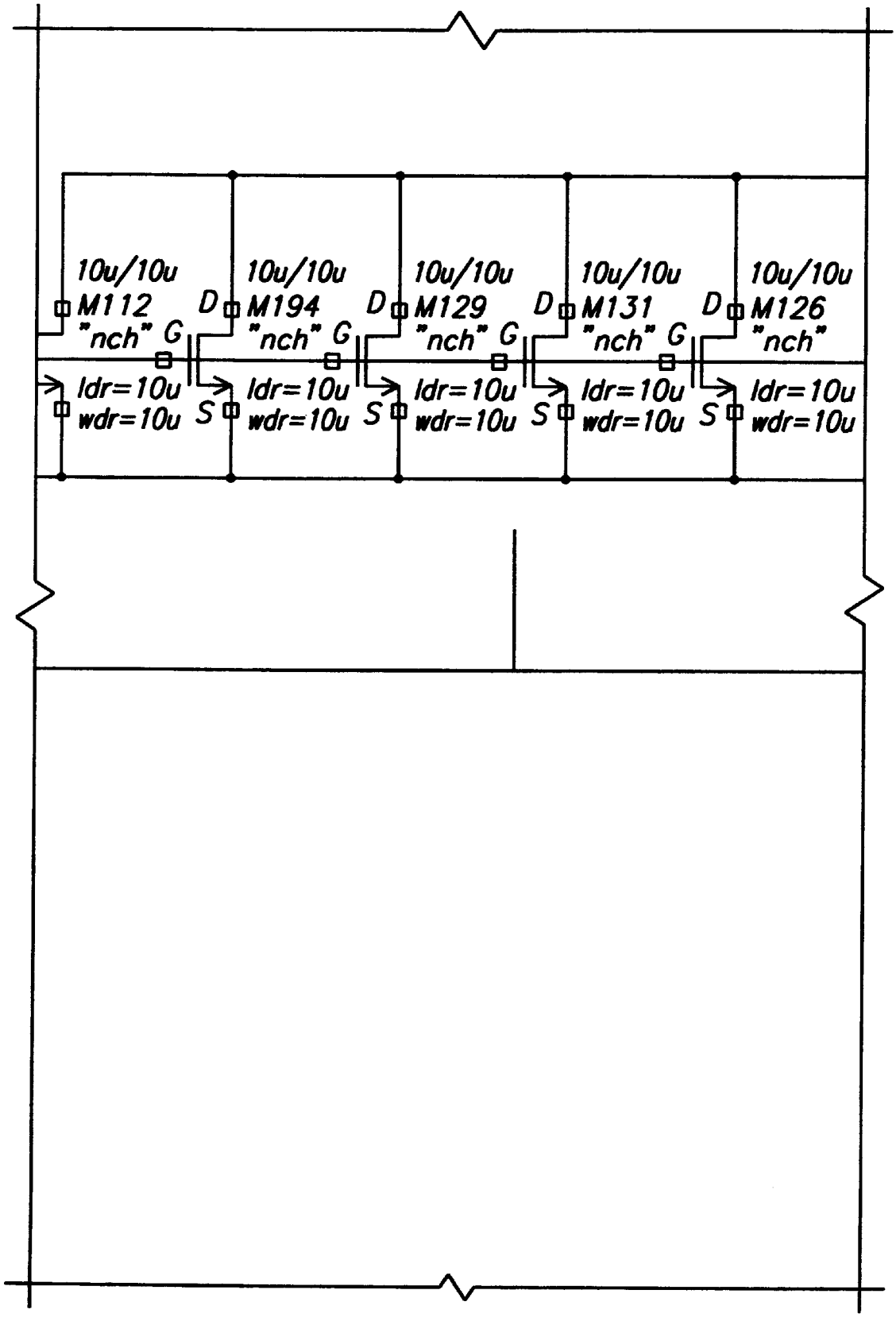

10u/10u
M112
"nch"
D
G
S
ldr=10u
wdr=10u
10u/10u
M194
"nch"
10u/10u
M129
"nch"
10u/10u
M131
"nch"
10u/10u
M126
"nch"

Fig 9.02BE

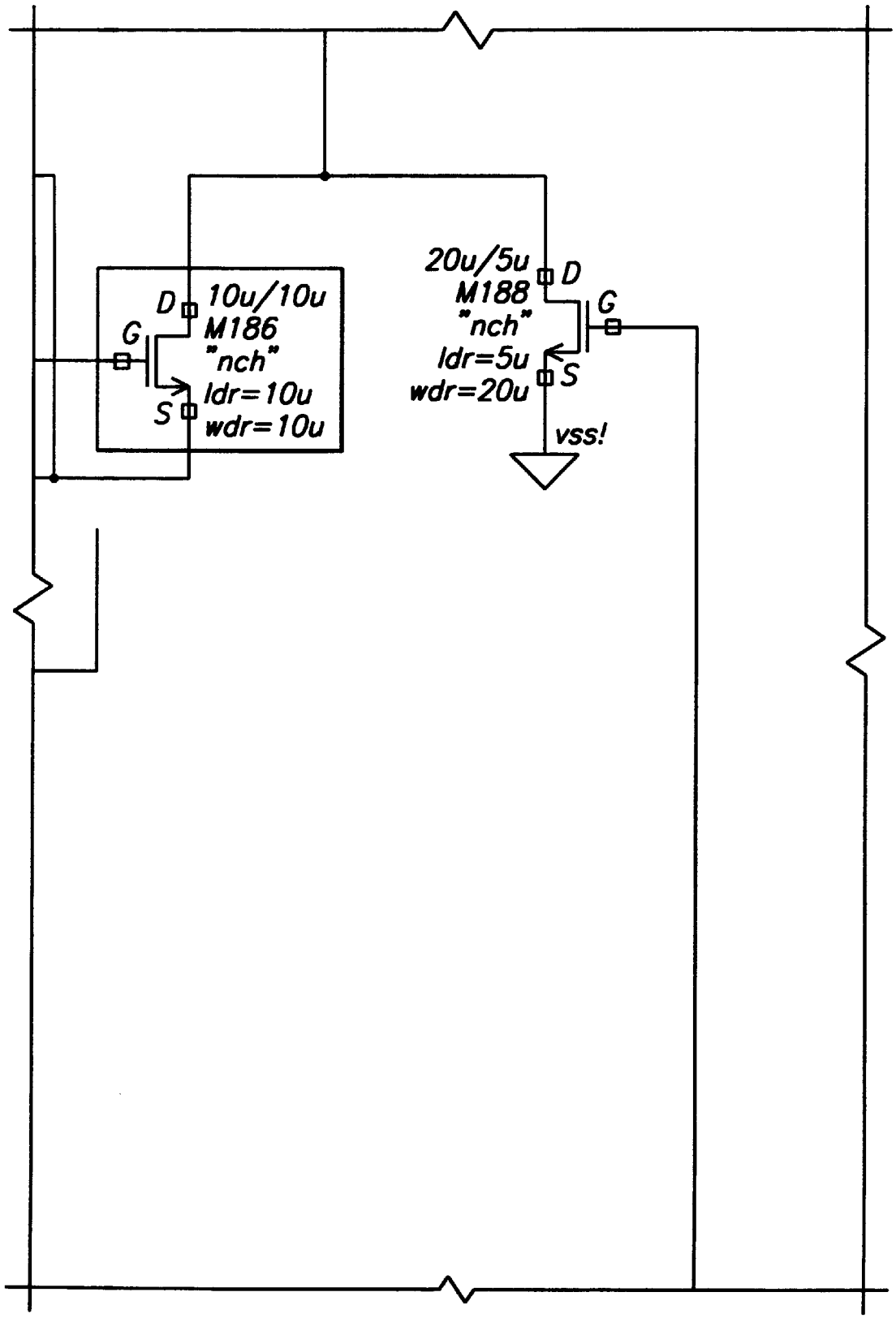

D
10u/10u
M186
"nch"
G
ldr=10u
S
wdr=10u
20u/5u
D
M188
"nch"
G
ldr=5u
S
wdr=20u
vss!

Fig 9.02BF

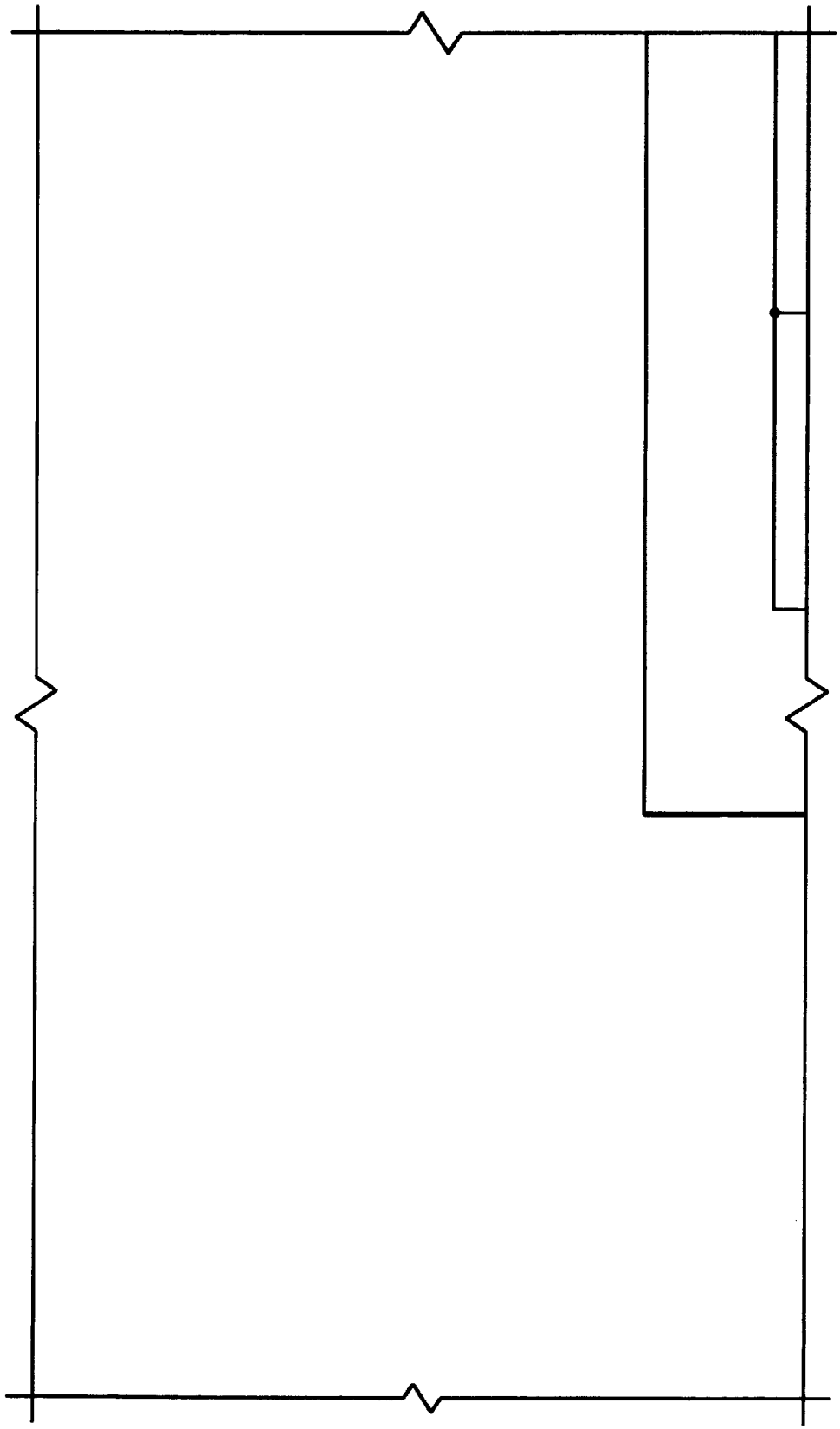


Fig 9.02B6

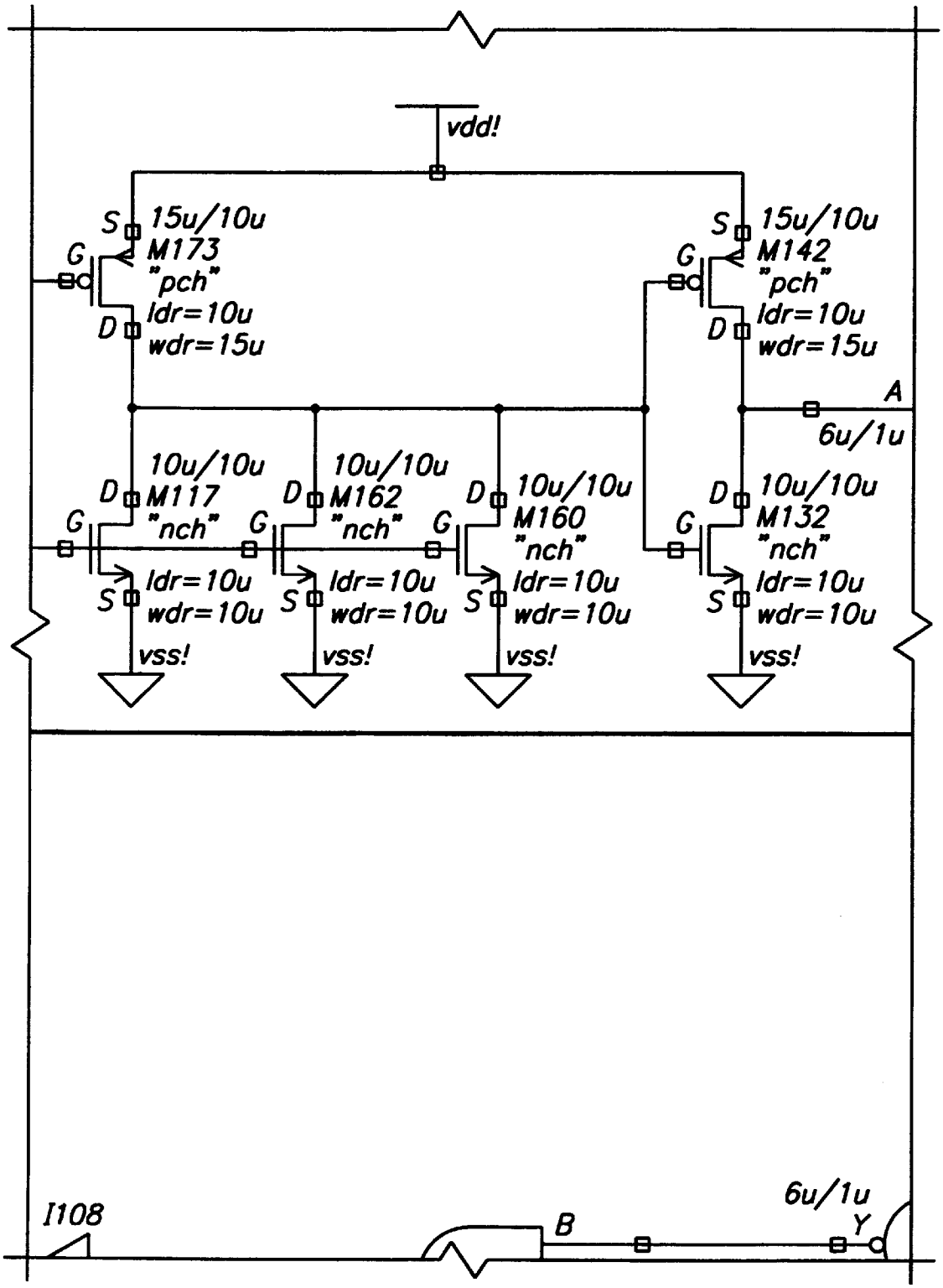

vdd!
S
G
D
15u/10u
M173
"pch"
ldr=10u
wdr=15u
15u/10u
M142
"pch"
ldr=10u
wdr=15u
A
6u/1u
10u/10u
M117
"nch"
10u/10u
M162
"nch"
10u/10u
M160
"nch"
10u/10u
M132
"nch"
ldr=10u
wdr=10u
vss!
I108
B
6u/1u
Y

Fig 9.02BH

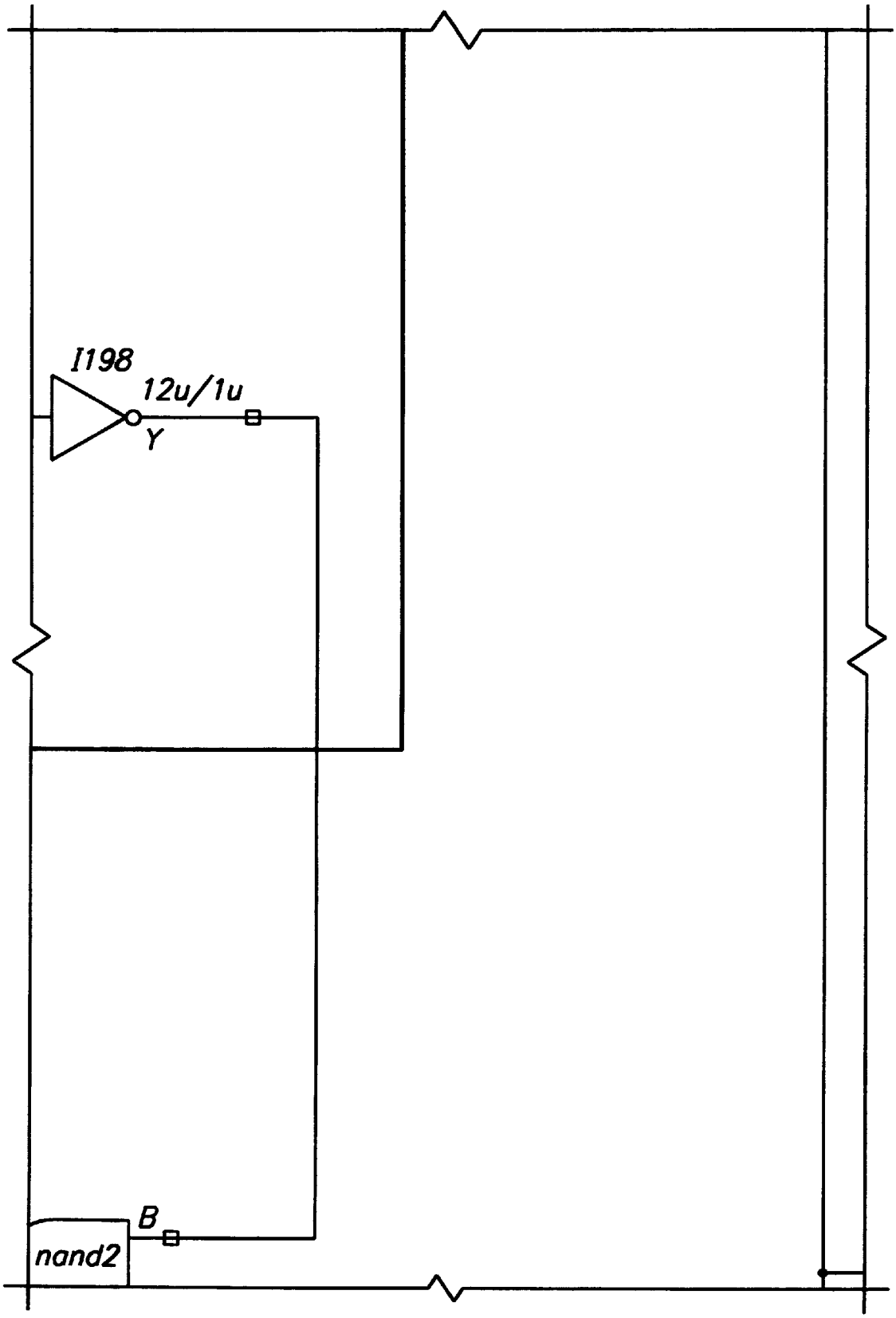


Fig 9.02BII

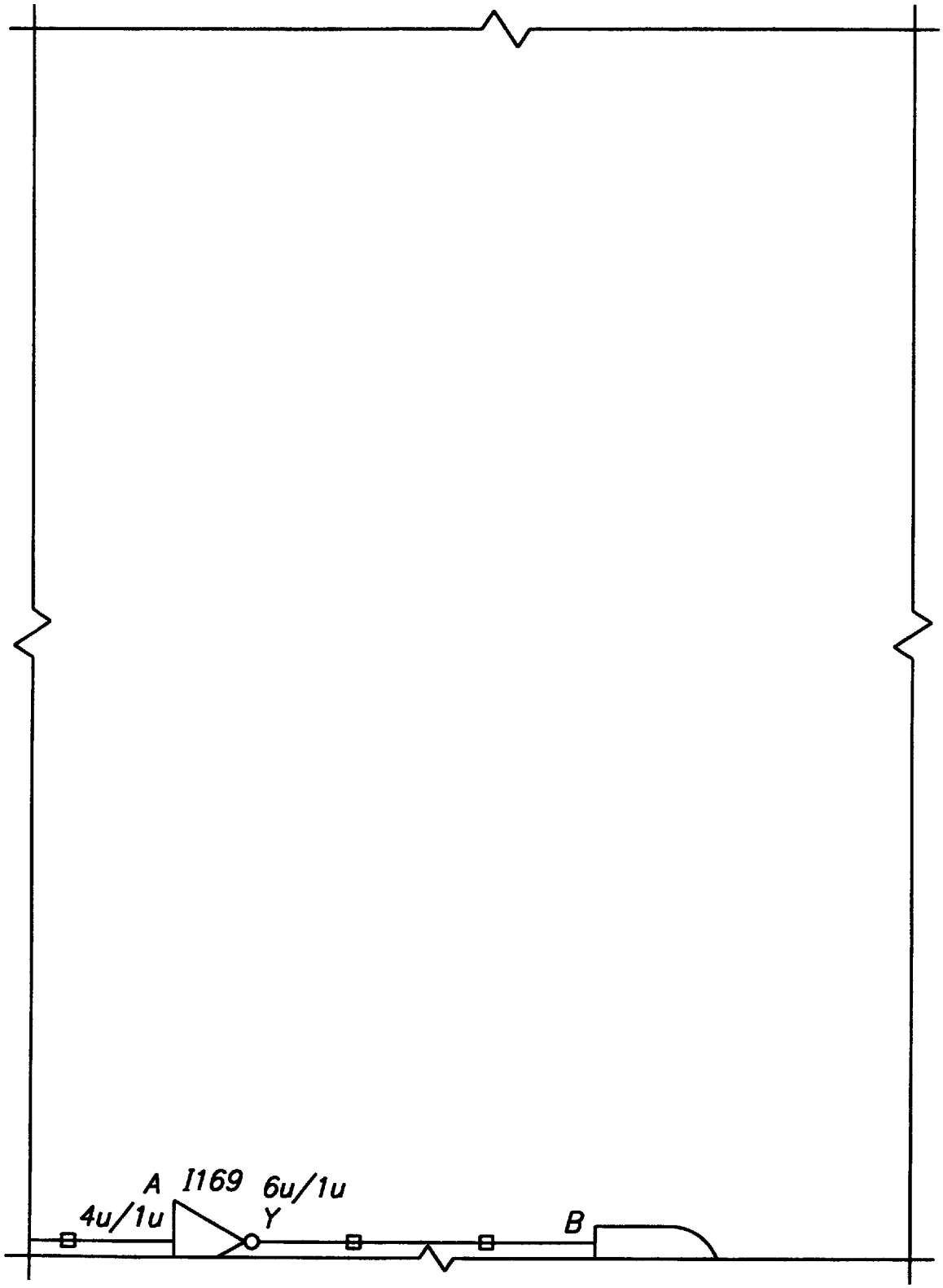


Fig 9.02Bol

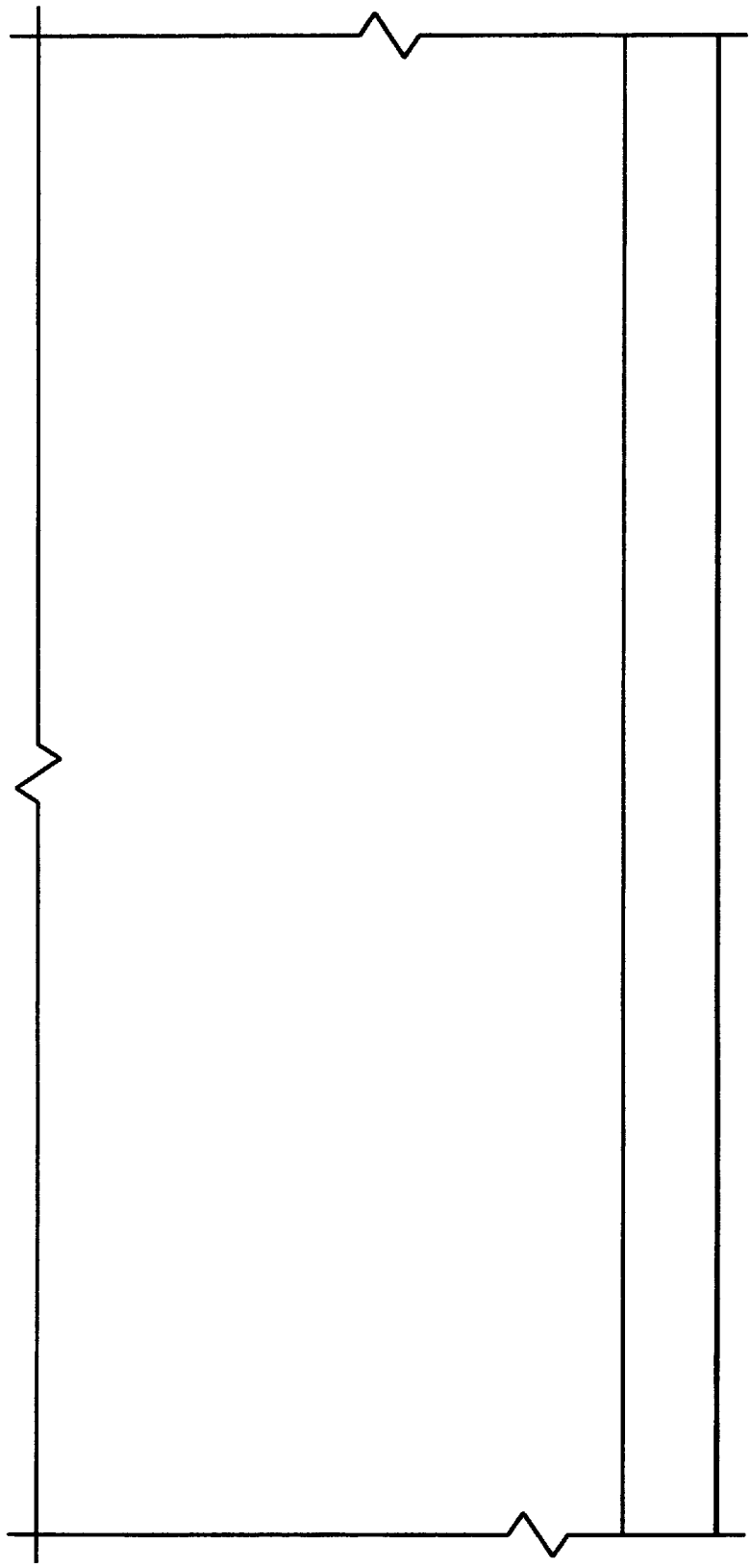


Fig 9.02BK

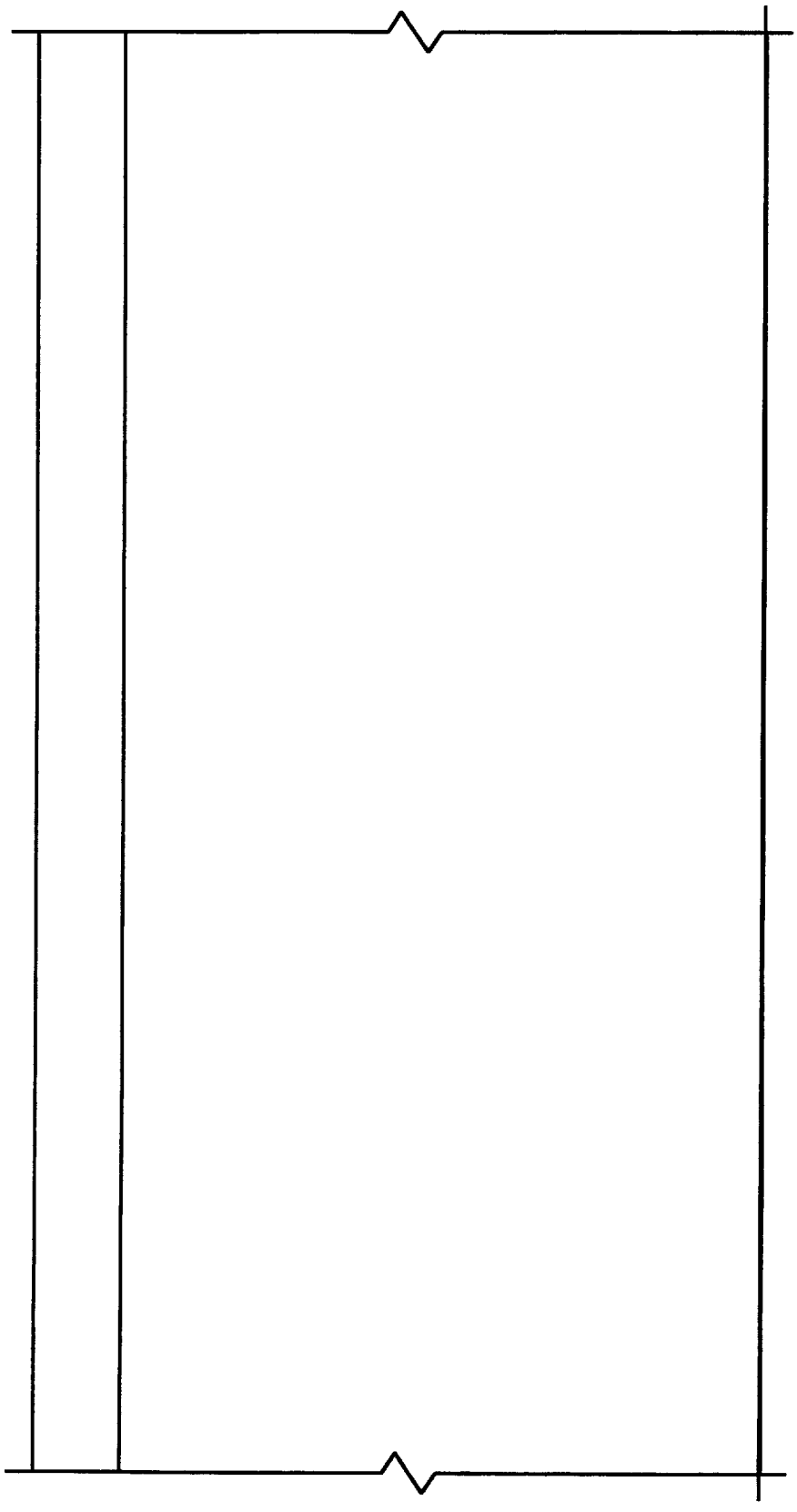


Fig 9.02CA

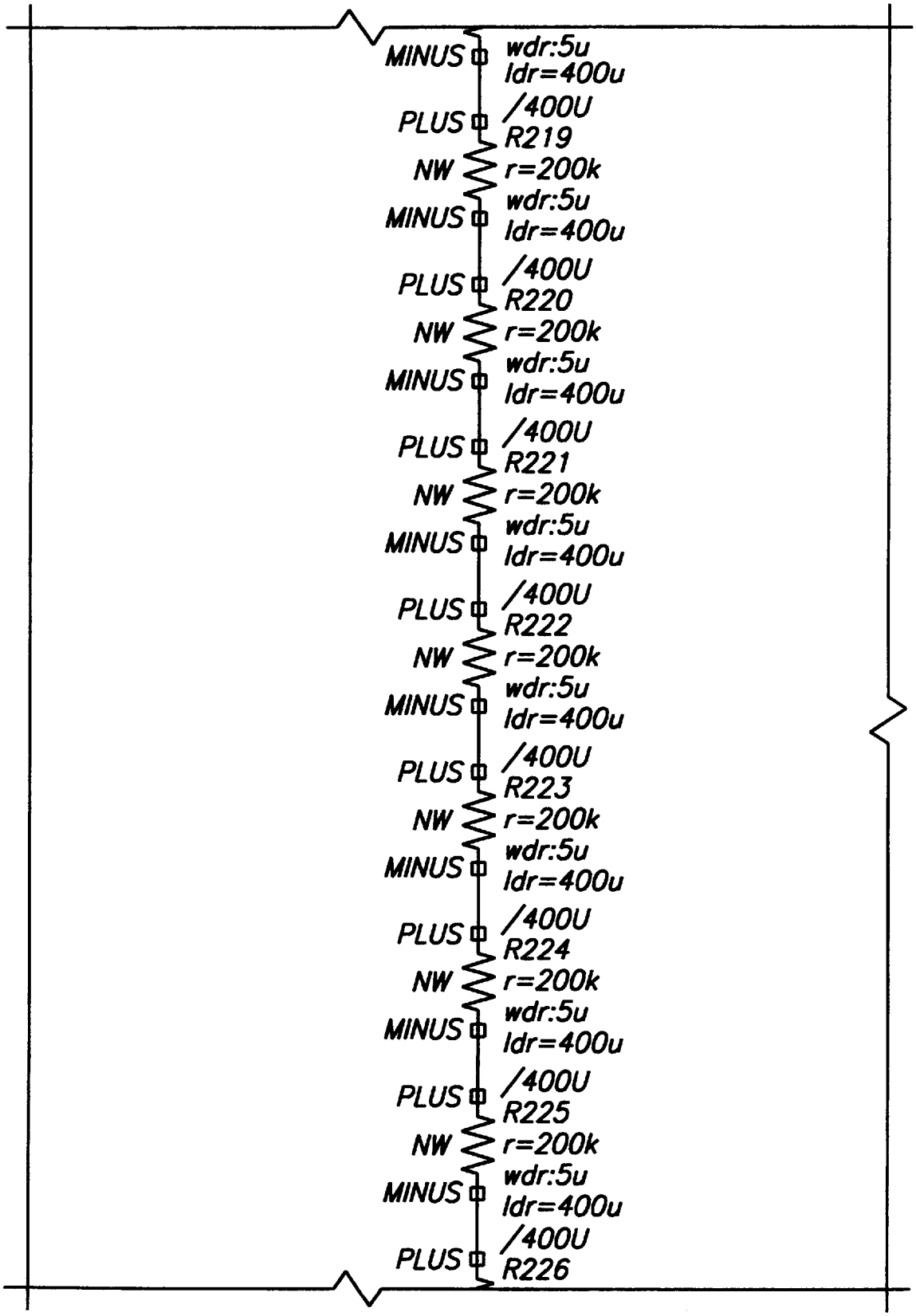

MINUS
wdr:5u
ldr=400u
PLUS
/400U
R219
NW
r=200k
MINUS
wdr:5u
ldr=400u
PLUS
/400U
R220
NW
r=200k
MINUS
wdr:5u
ldr=400u
PLUS
/400U
R221
NW
r=200k
MINUS
wdr:5u
ldr=400u
PLUS
/400U
R222
NW
r=200k
MINUS
wdr:5u
ldr=400u
PLUS
/400U
R223
NW
r=200k
MINUS
wdr:5u
ldr=400u
PLUS
/400U
R224
NW
r=200k
MINUS
wdr:5u
ldr=400u
PLUS
/400U
R225
NW
r=200k
MINUS
wdr:5u
ldr=400u
PLUS
/400U
R226

Fig 9.002CC

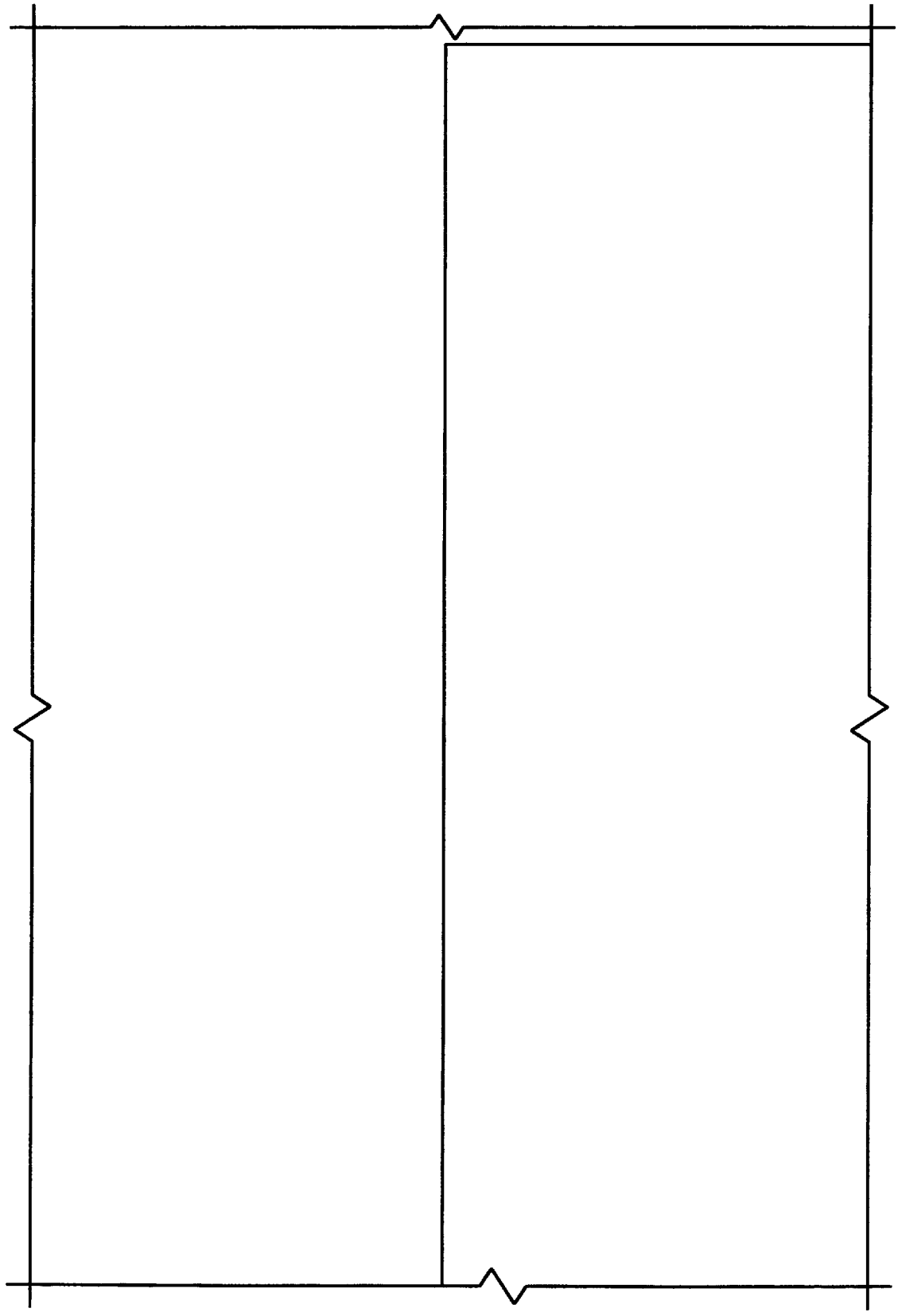


Fig 9.02CD

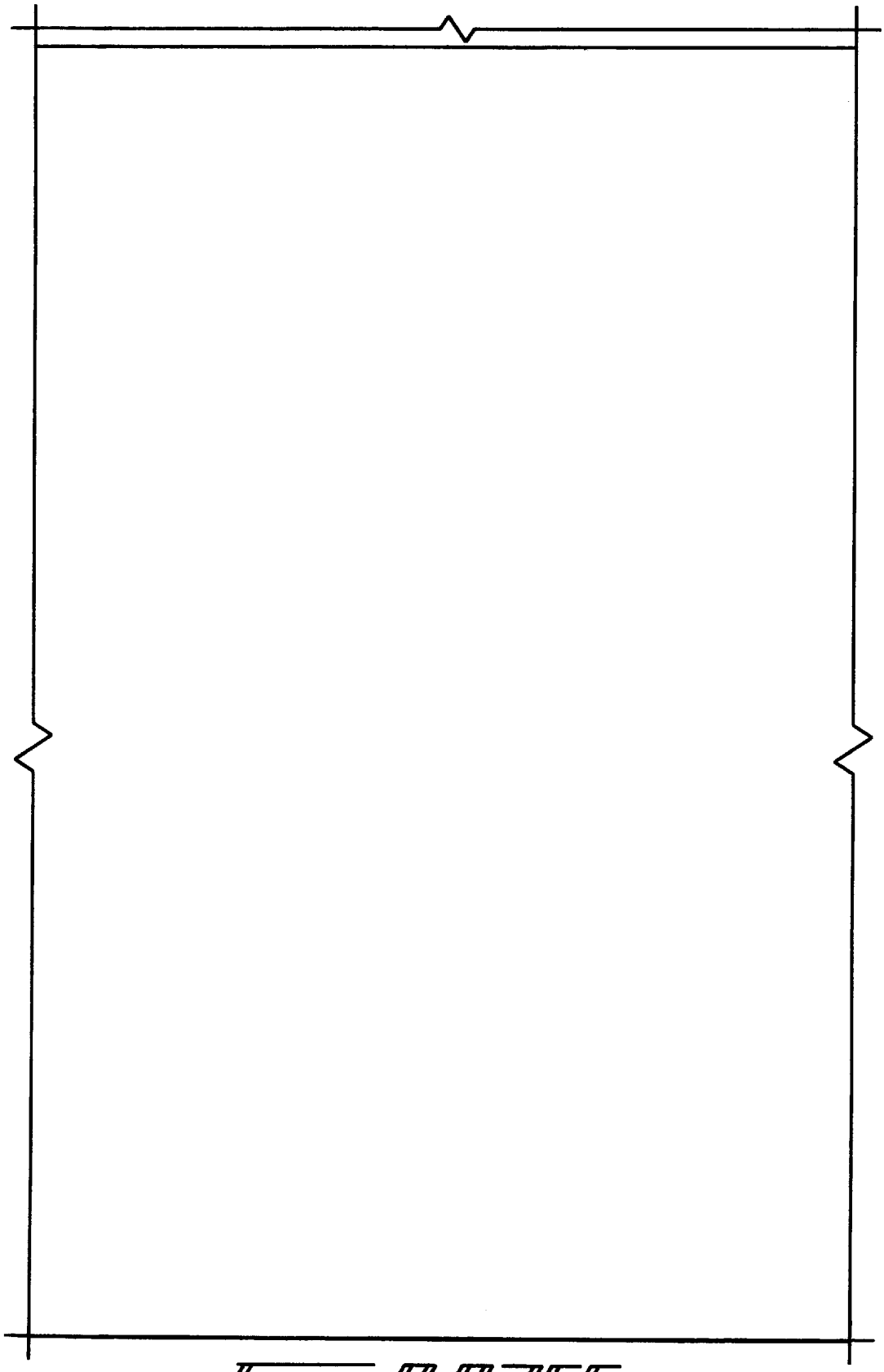


Fig 9.02CE

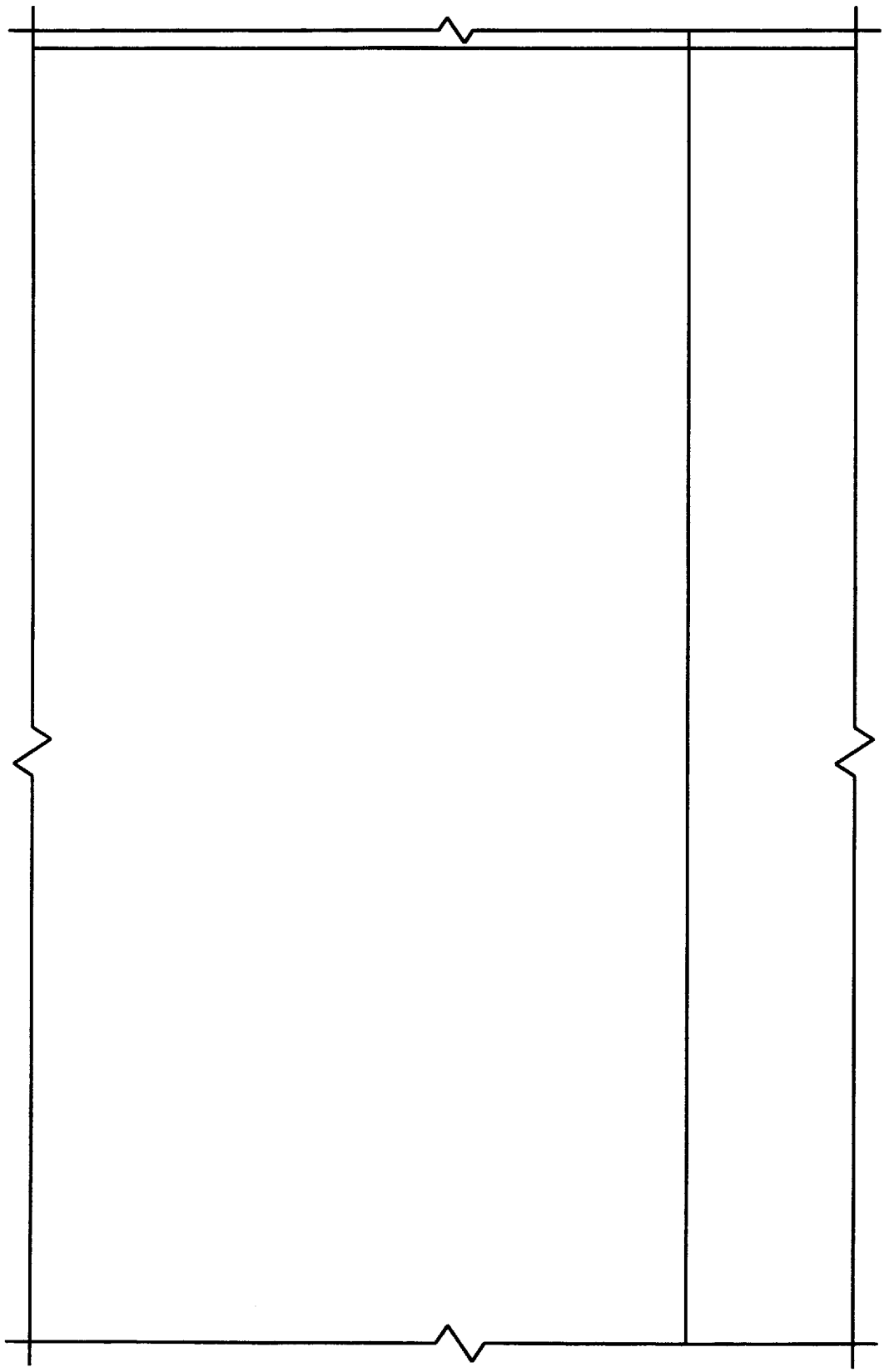


Fig 9.02CF

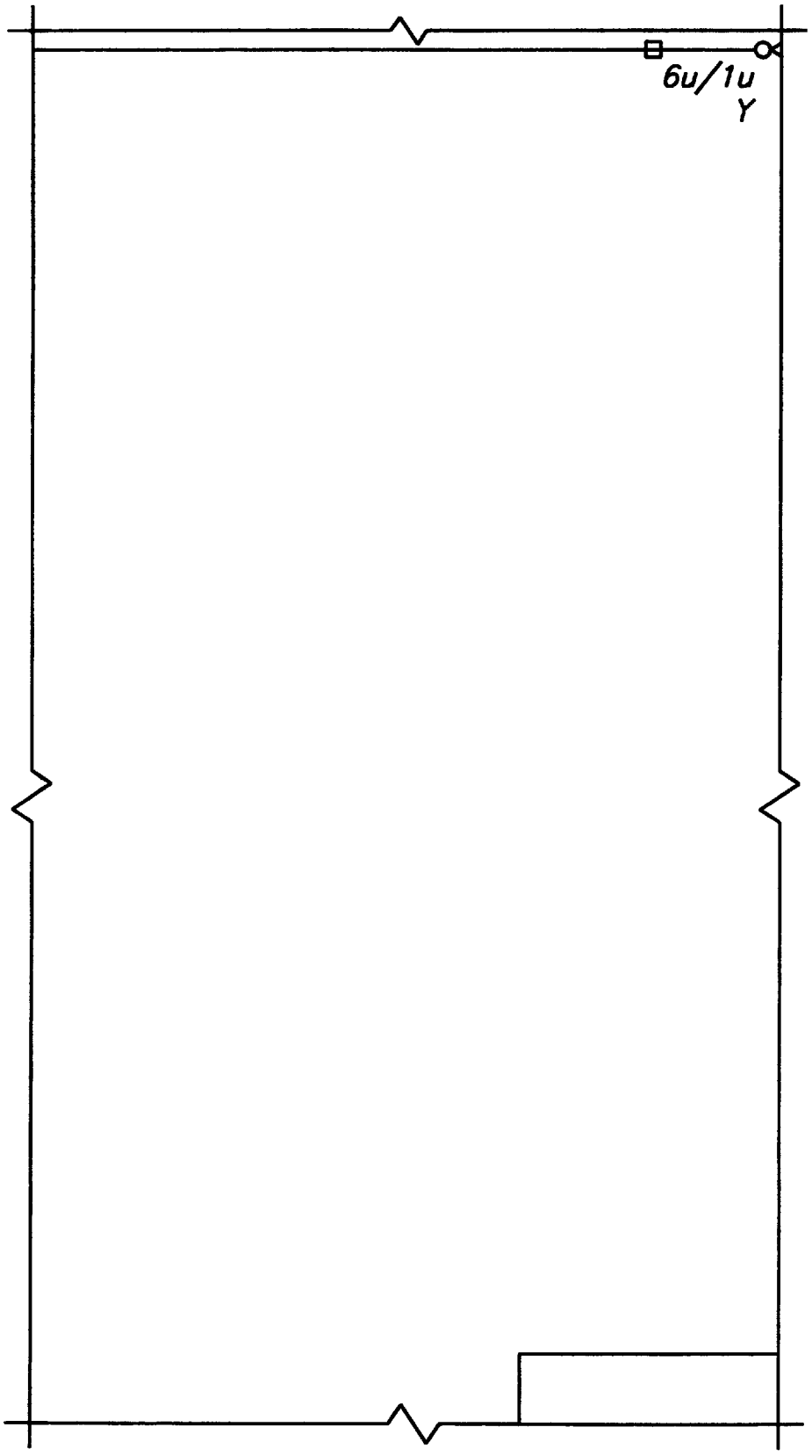


Fig 9.0226

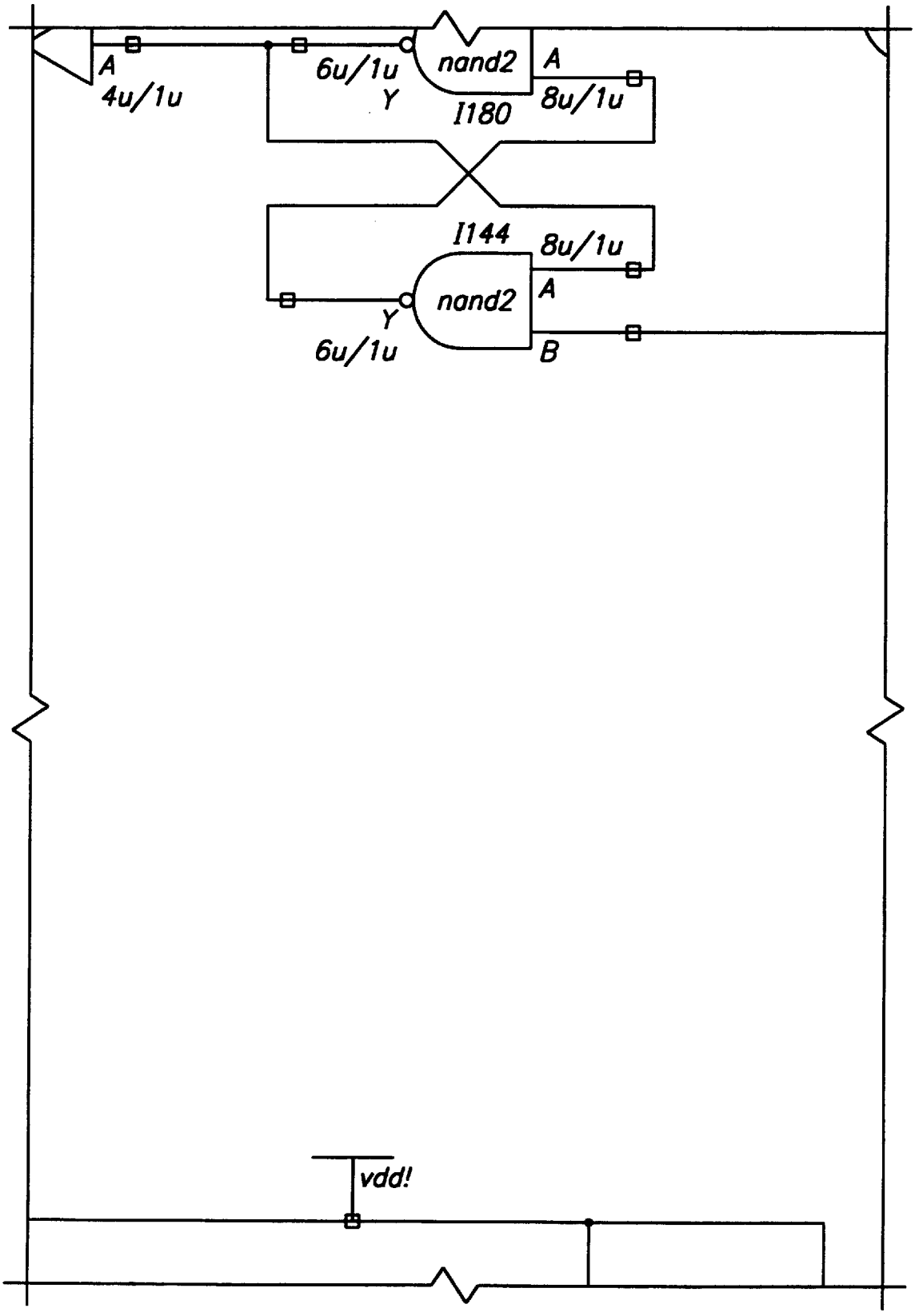


Fig 9.02CH

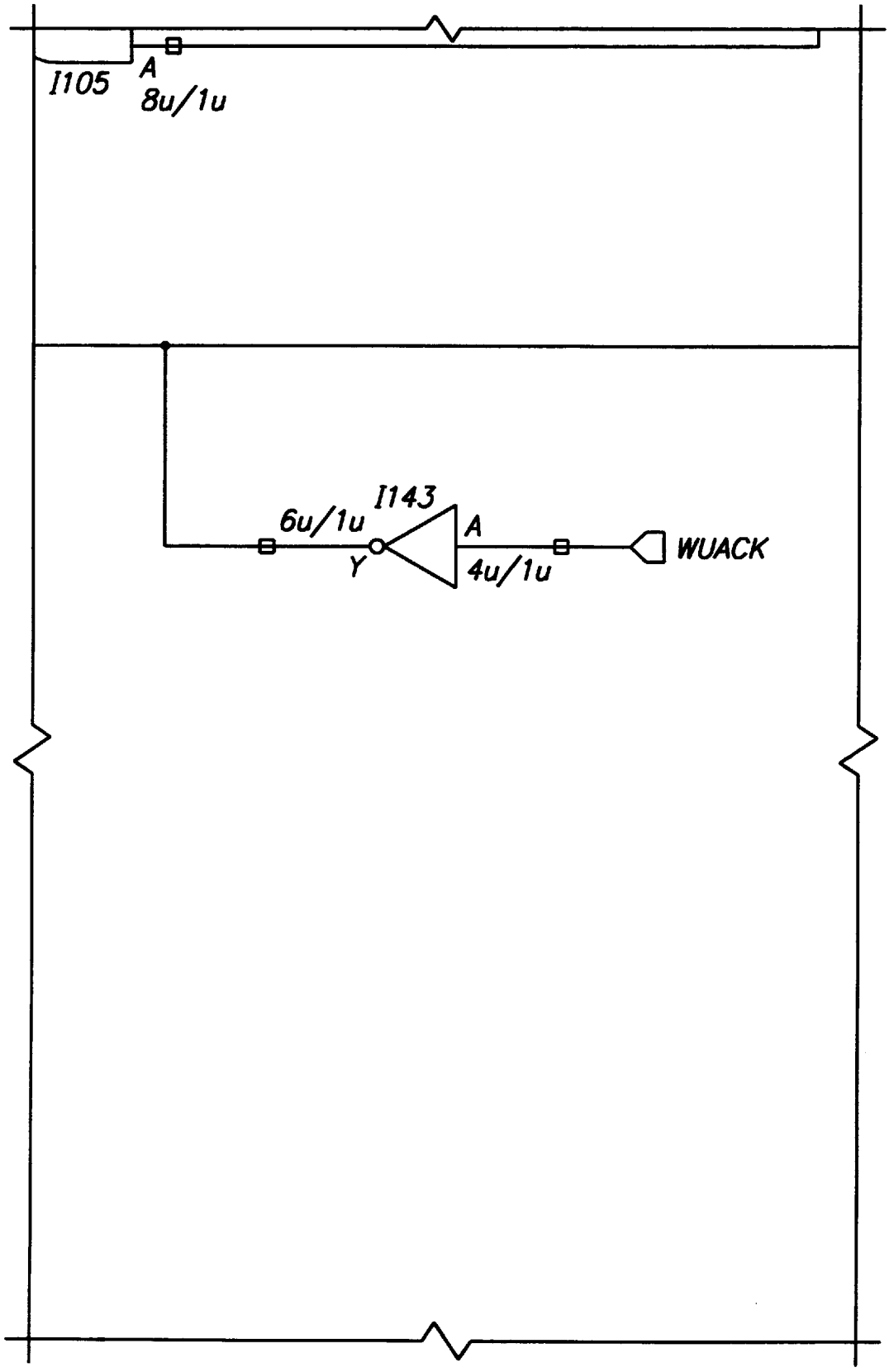


Fig 9.02CII

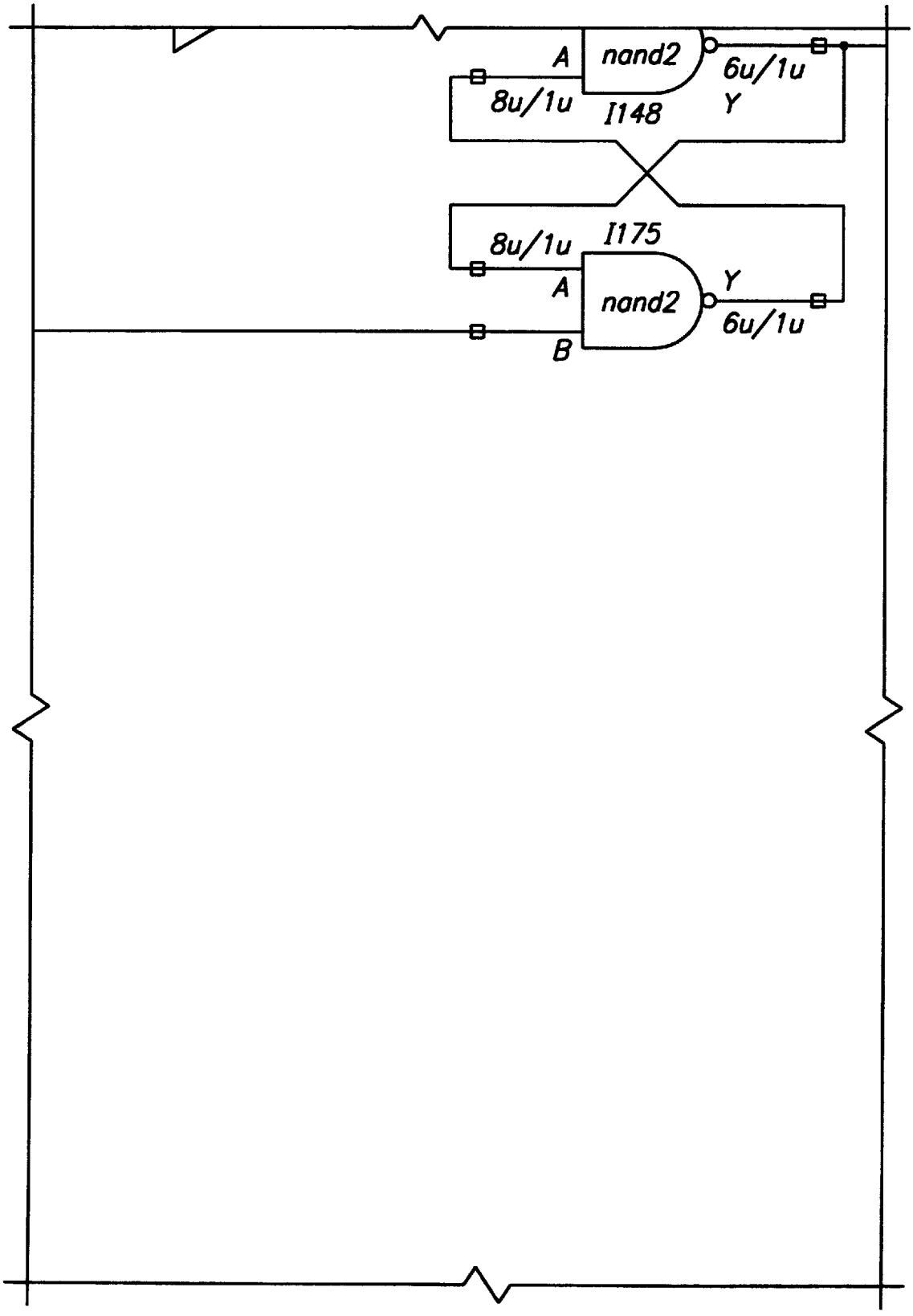


Fig 9.02Cd

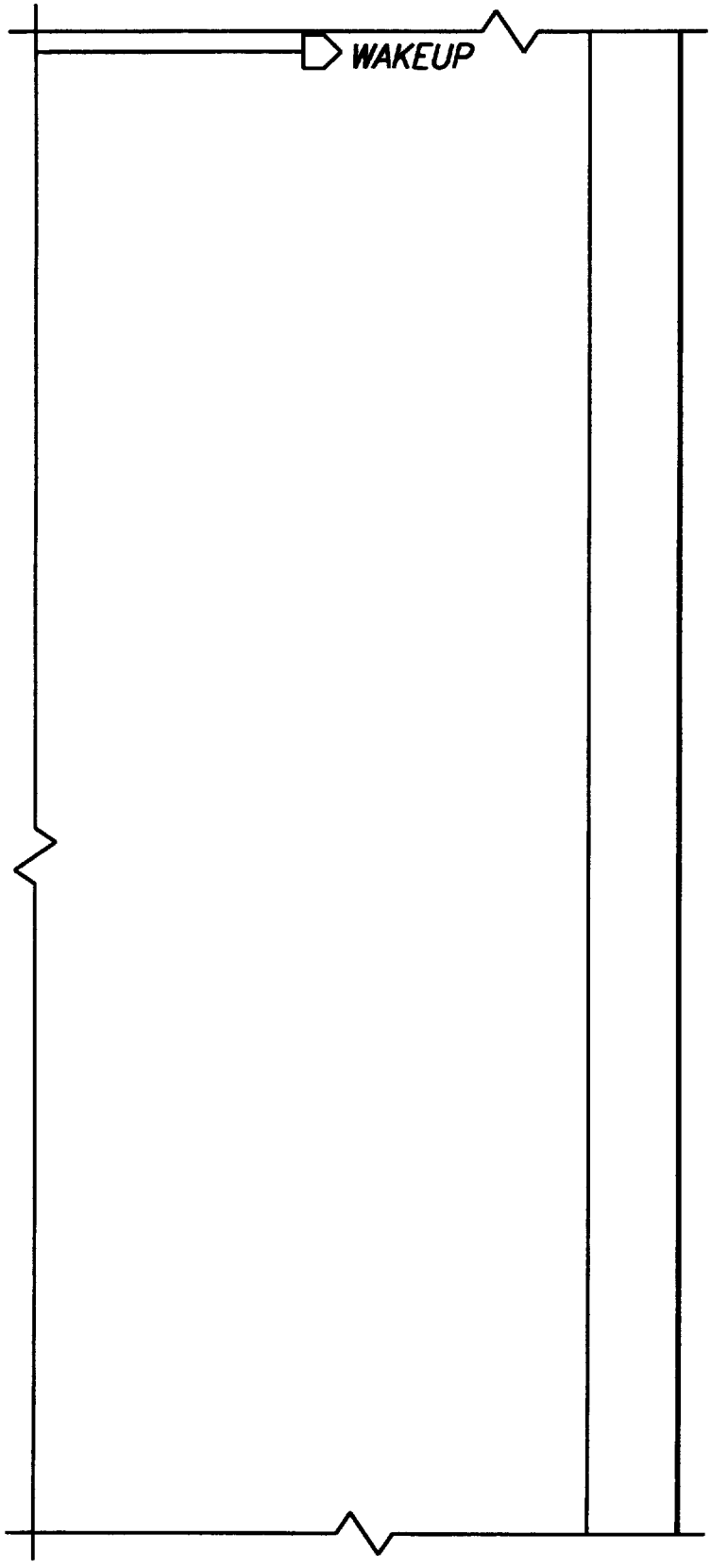


Fig 9.02CK

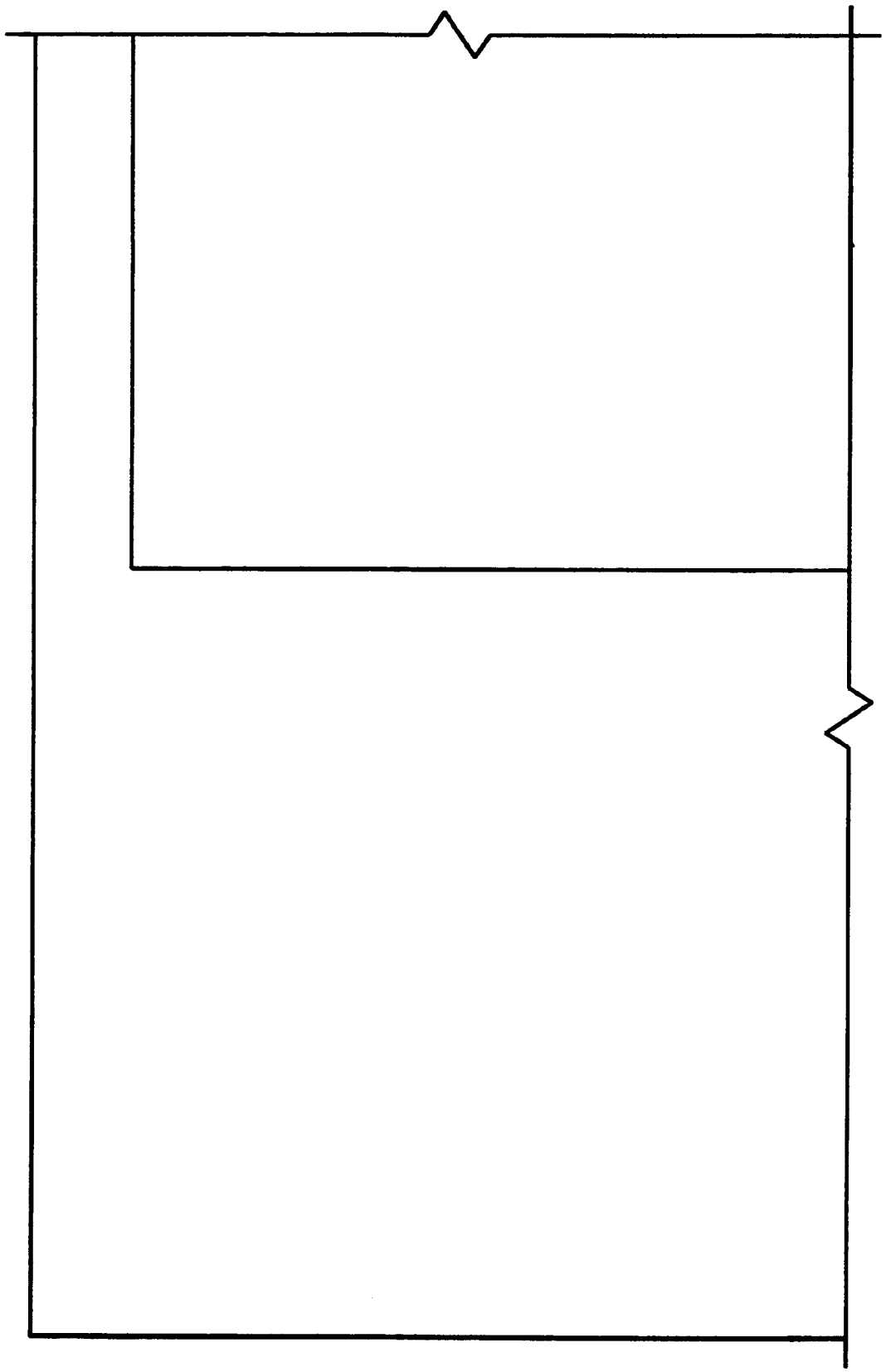


Fig 9.02DA

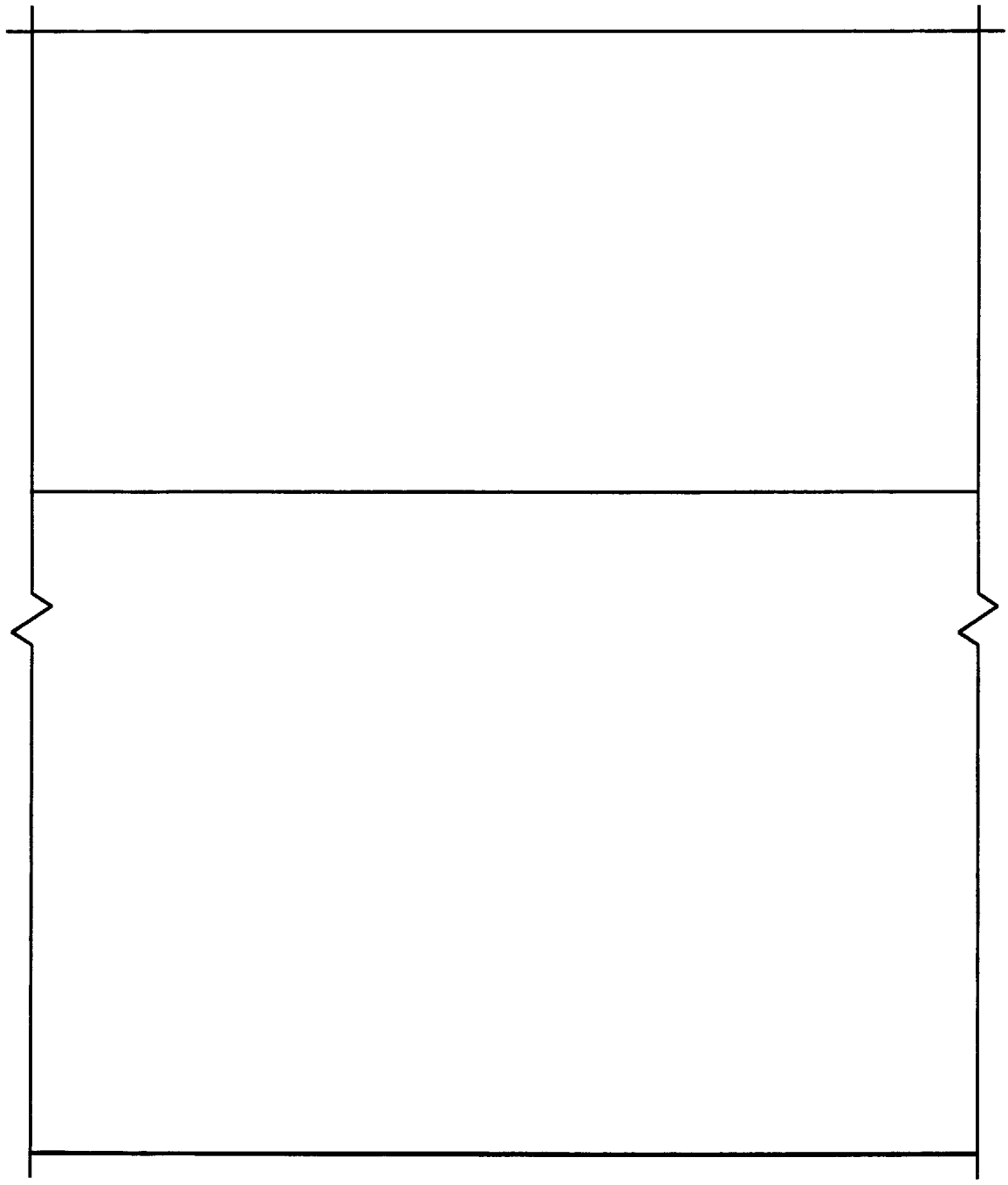


Fig 9.020B

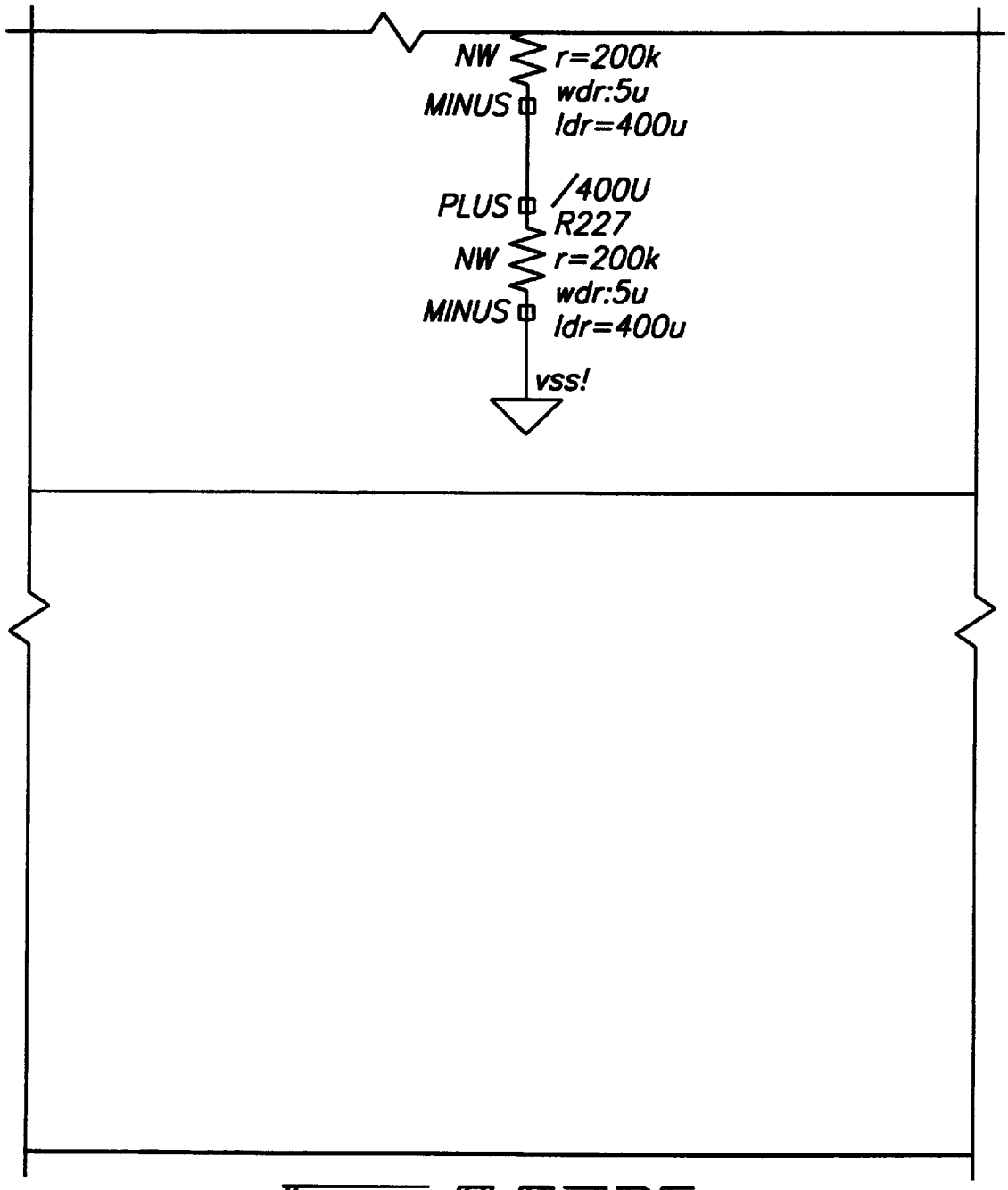

NW
r=200k
wdr:5u
MINUS
ldr=400u
/400U
PLUS
R227
NW
r=200k
wdr:5u
MINUS
ldr=400u
vss!

Fig 9.02DC

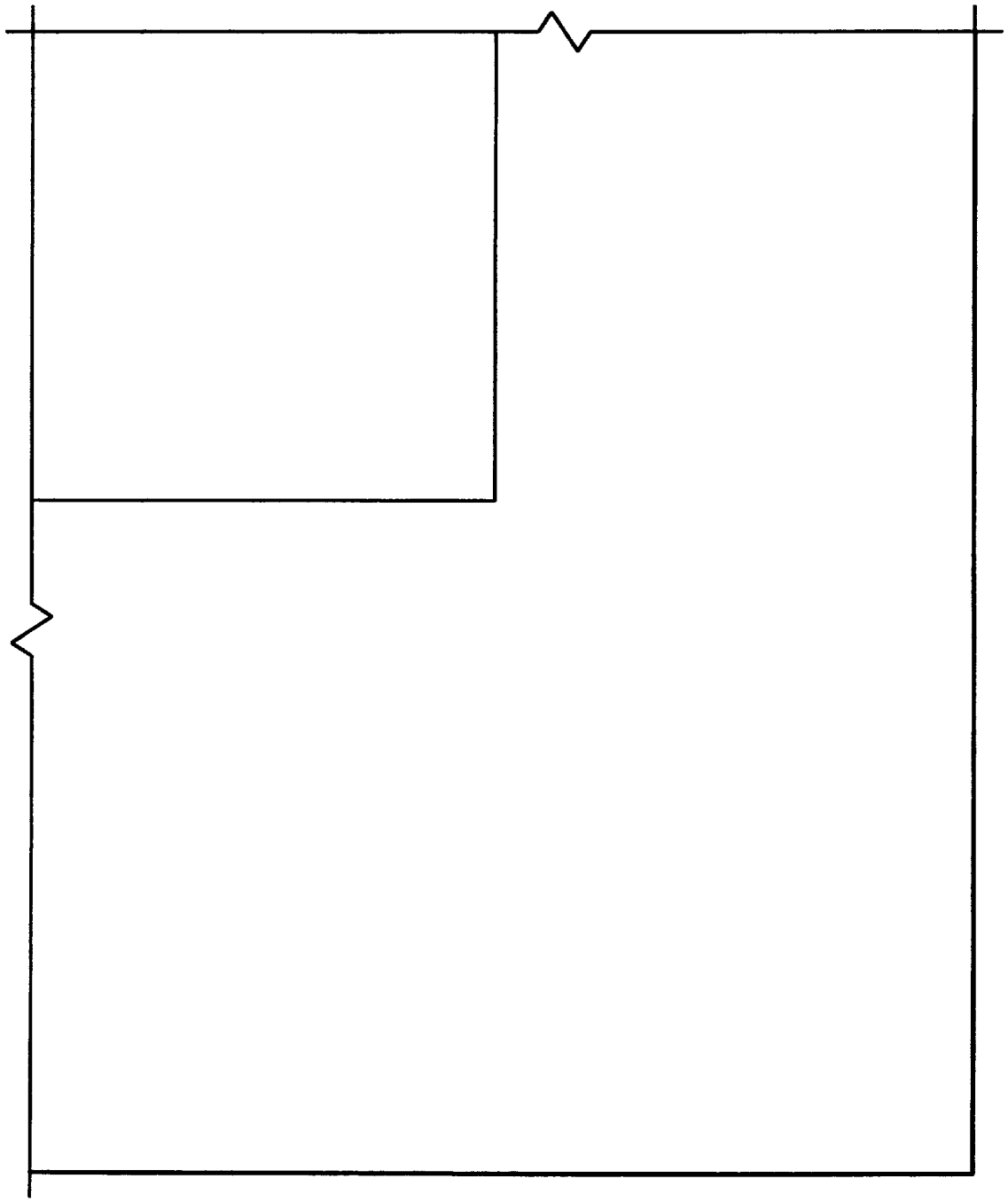


Fig 9.02DD

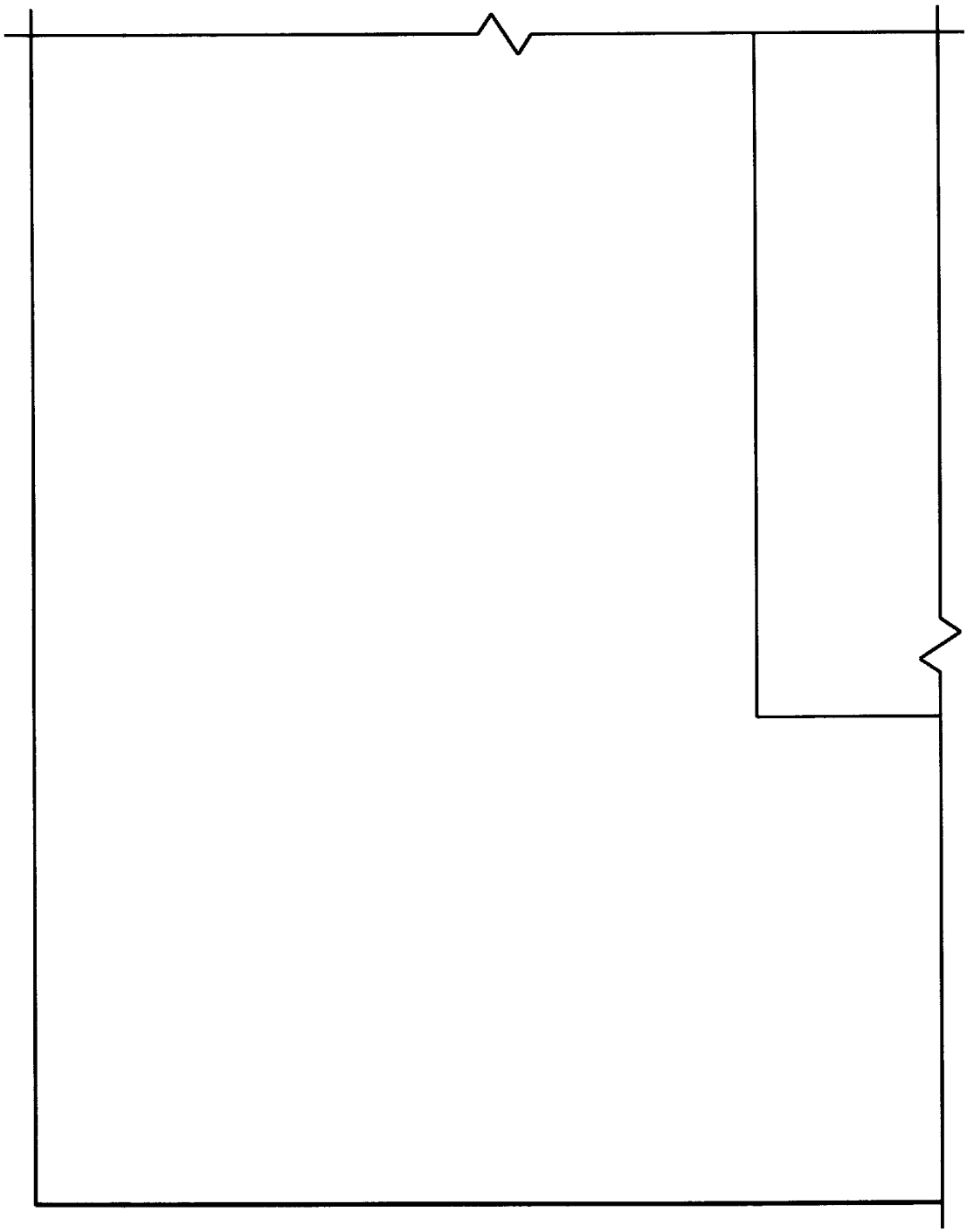


Fig 9.02DF

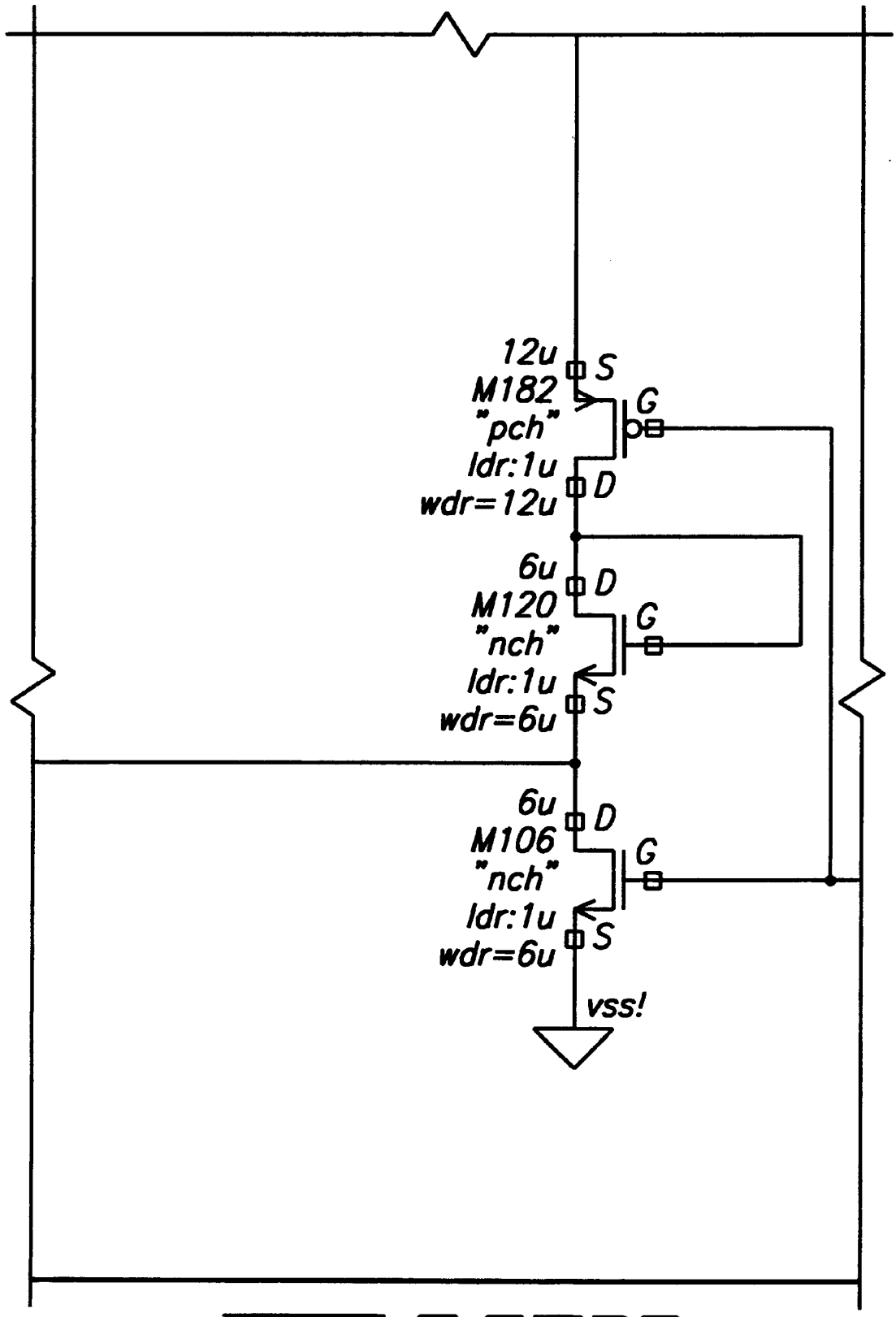

12u
M182
"pch"
ldr:1u
wdr=12u
S
G
D
6u
M120
"nch"
ldr:1u
wdr=6u
D
G
S
6u
M106
"nch"
ldr:1u
wdr=6u
D
G
S
vss!

Fig 9.0206

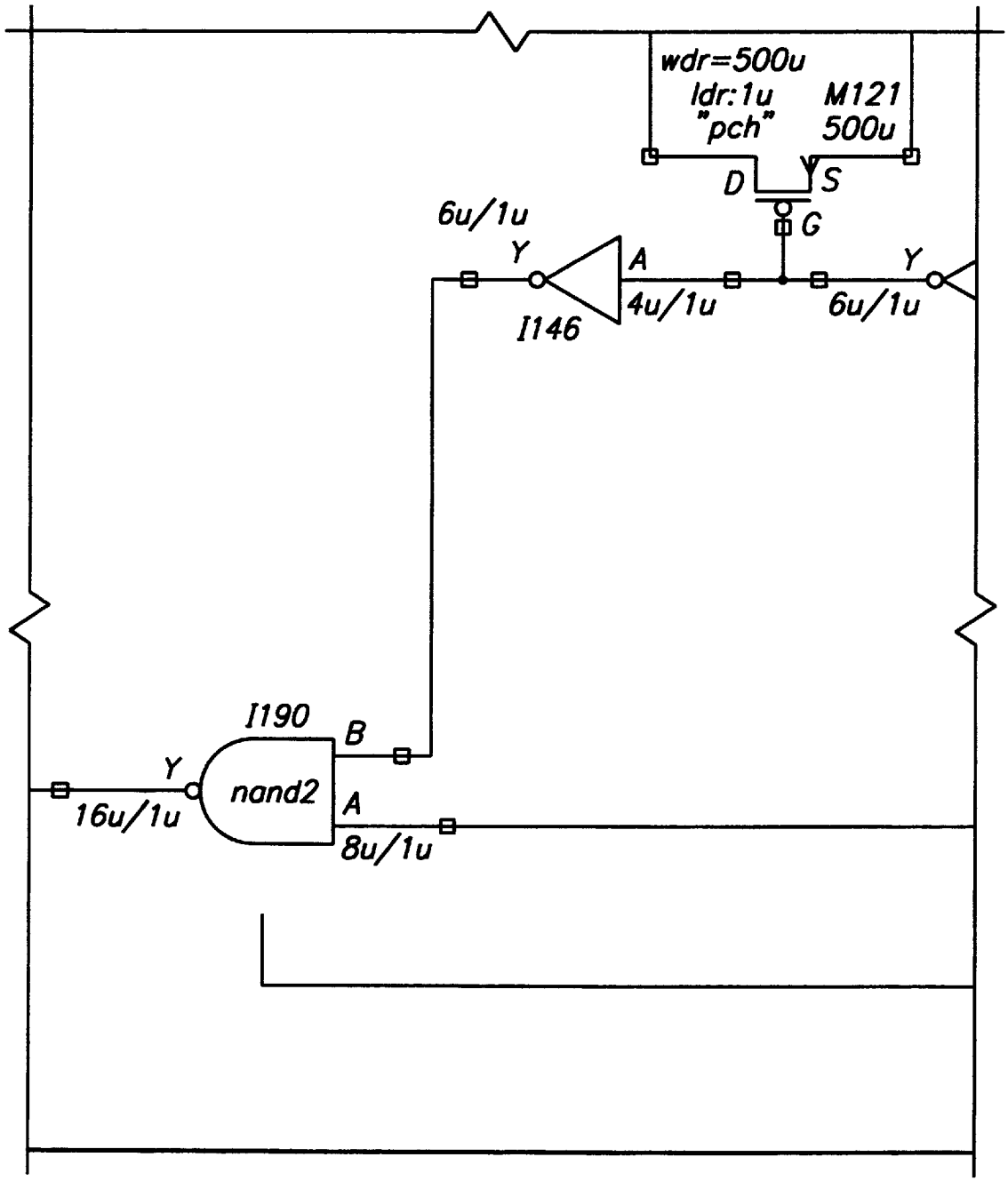
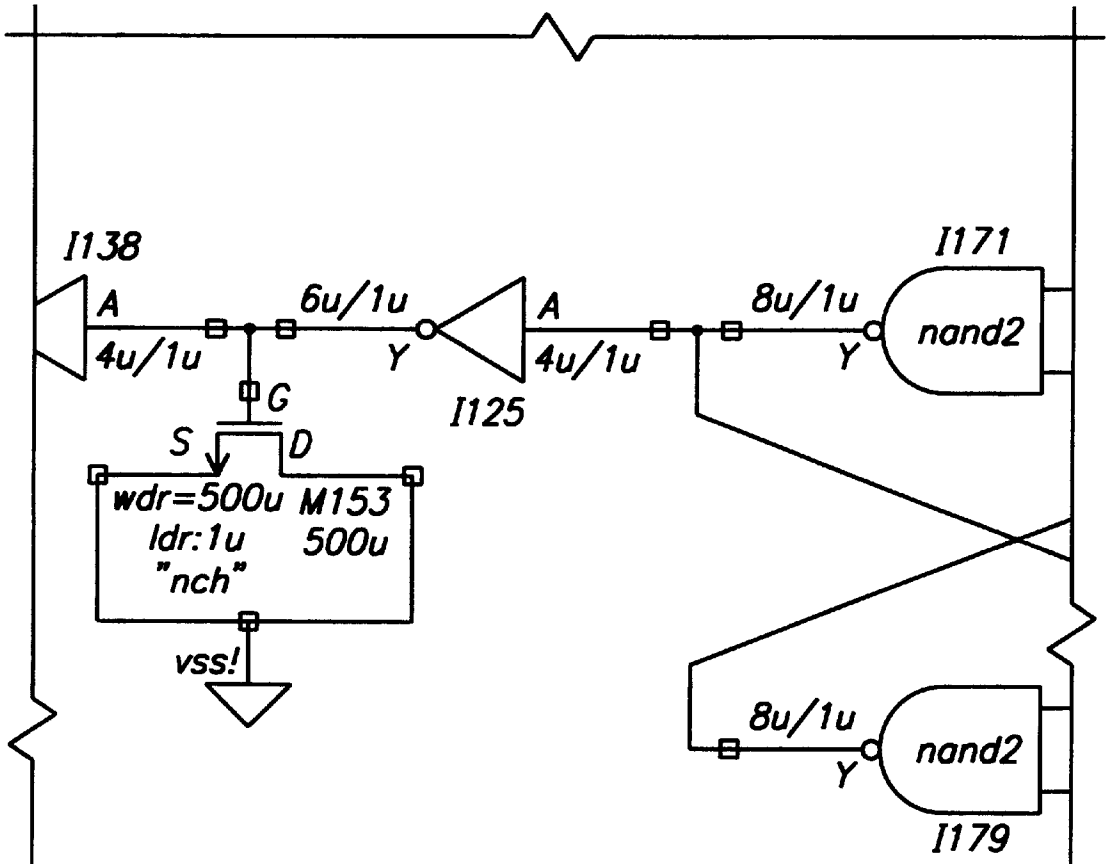

wdr=500u
ldr:1u
"pch"
M121
500u
D
S
G
6u/1u
Y
A
Y
I146
4u/1u
6u/1u
I190
B
Y
nand2
A
16u/1u
8u/1u

Fig 9.02DH



Use 8/1 device segments for all n and p devices in these 3 nand gates

Fig 9.0201

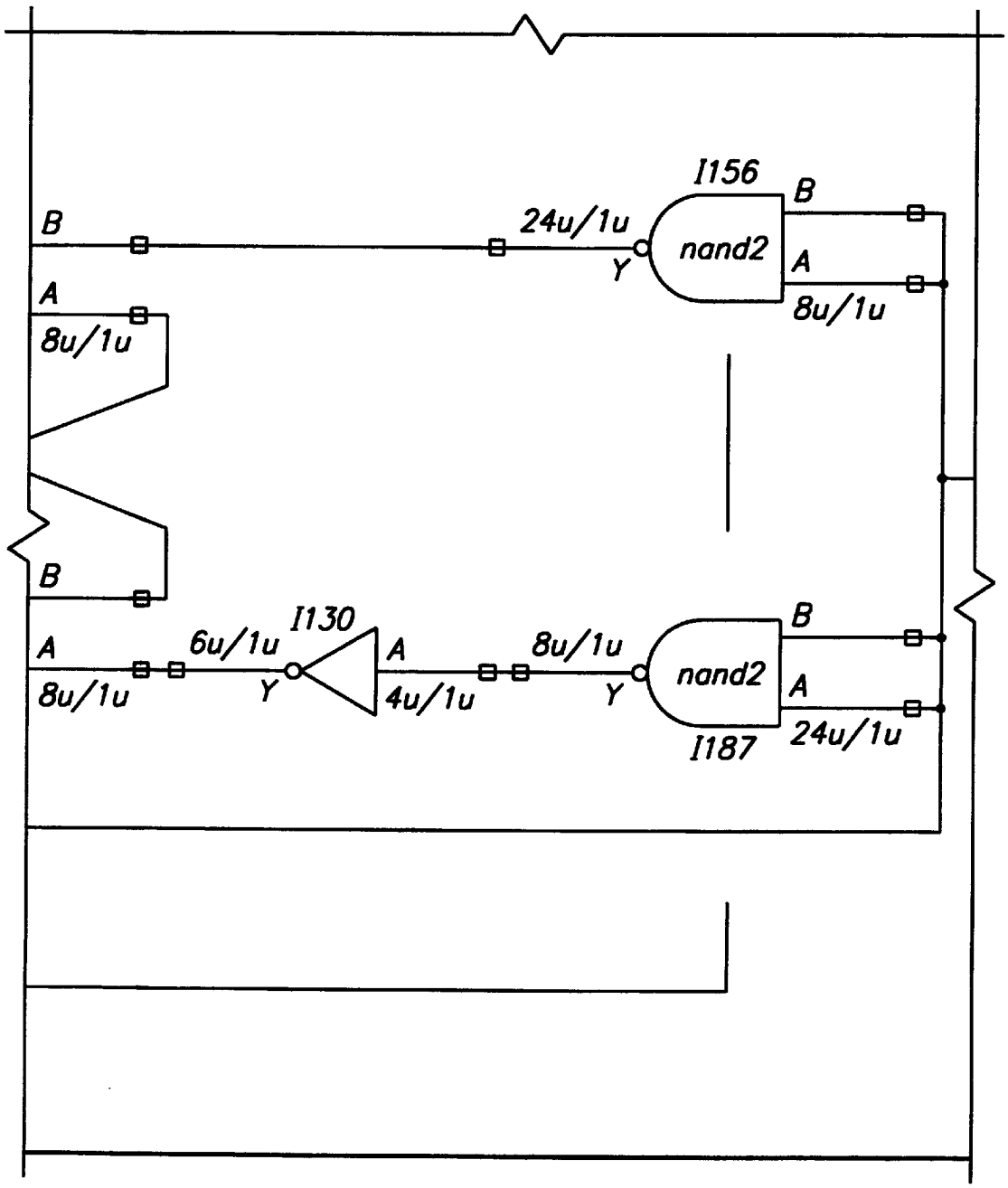

I156
B
24u/1u
nand2
A
8u/1u
Y
B
A
8u/1u
B
I130
A
6u/1u
Y
A
4u/1u
8u/1u
Y
nand2
B
A
24u/1u
I187

Fig 9.02Dal

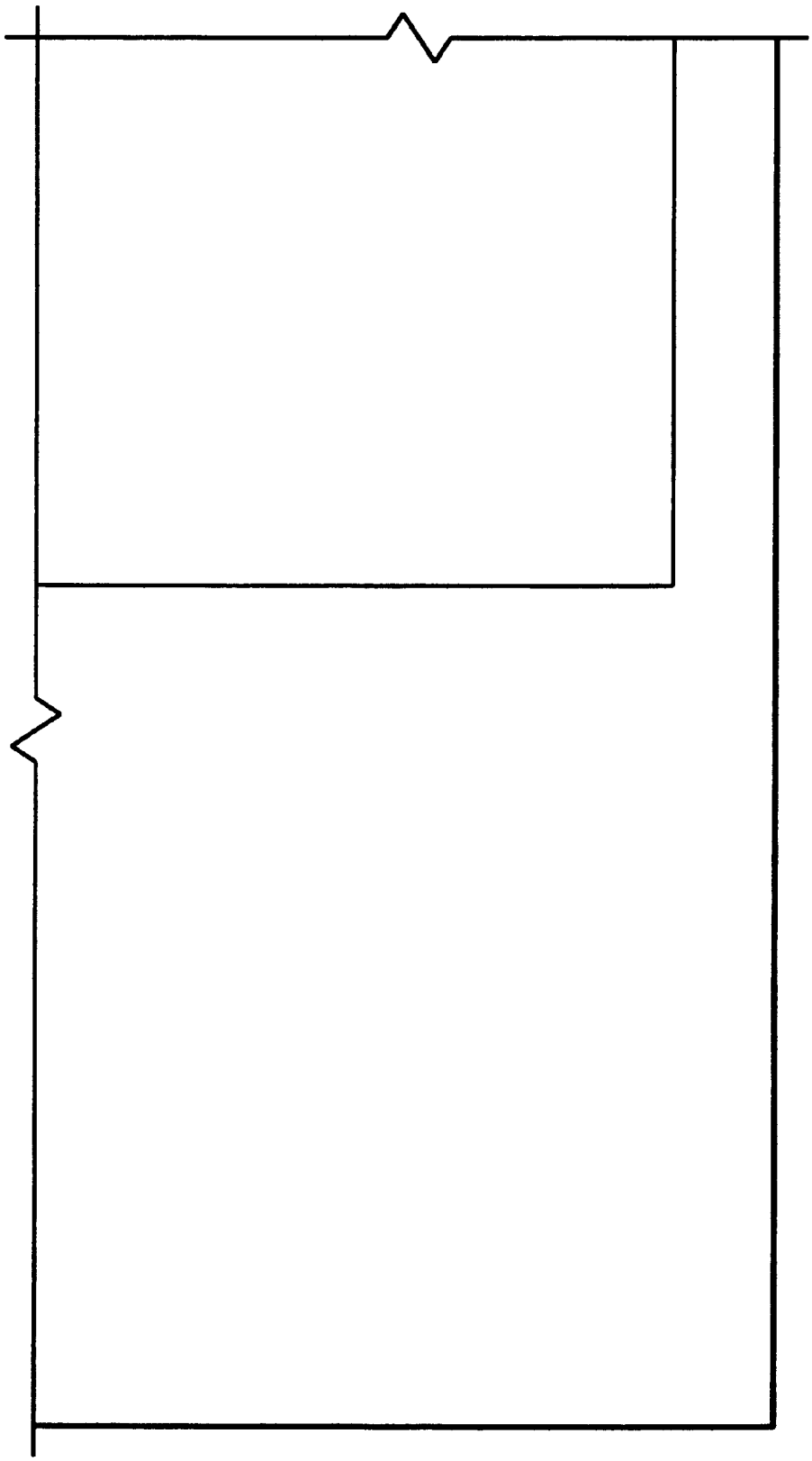


Fig 9.02DK

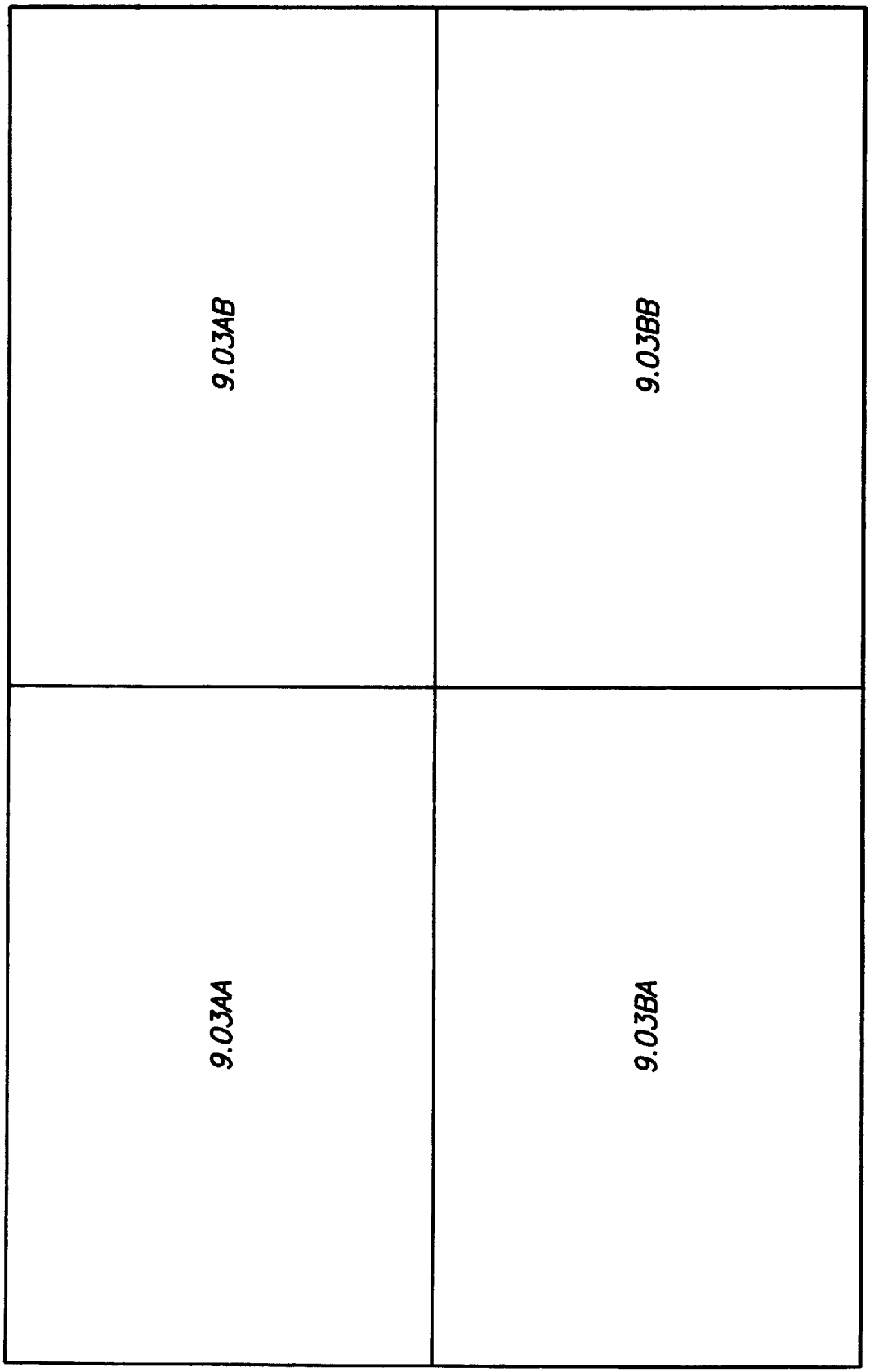


FIG 9.03E

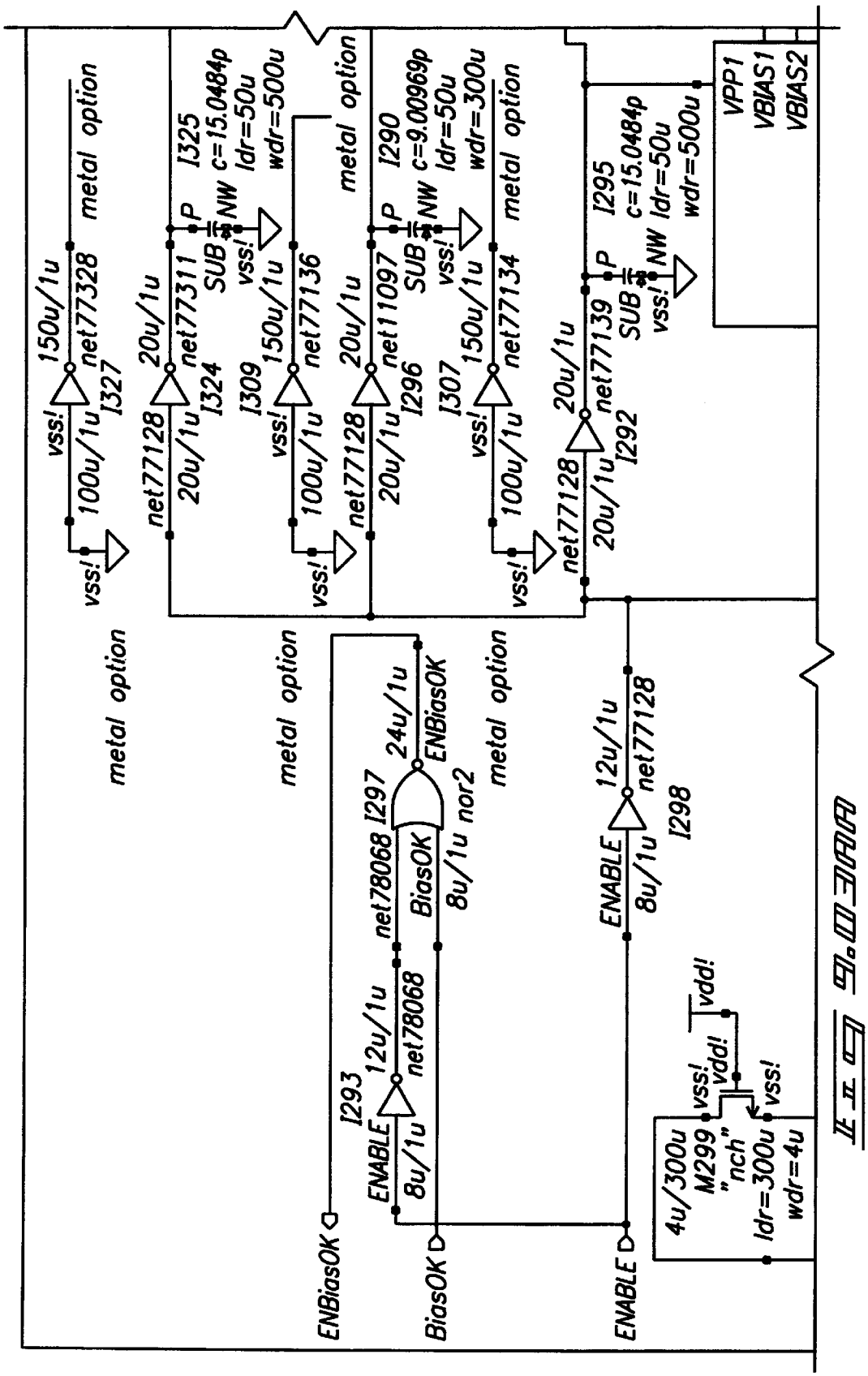
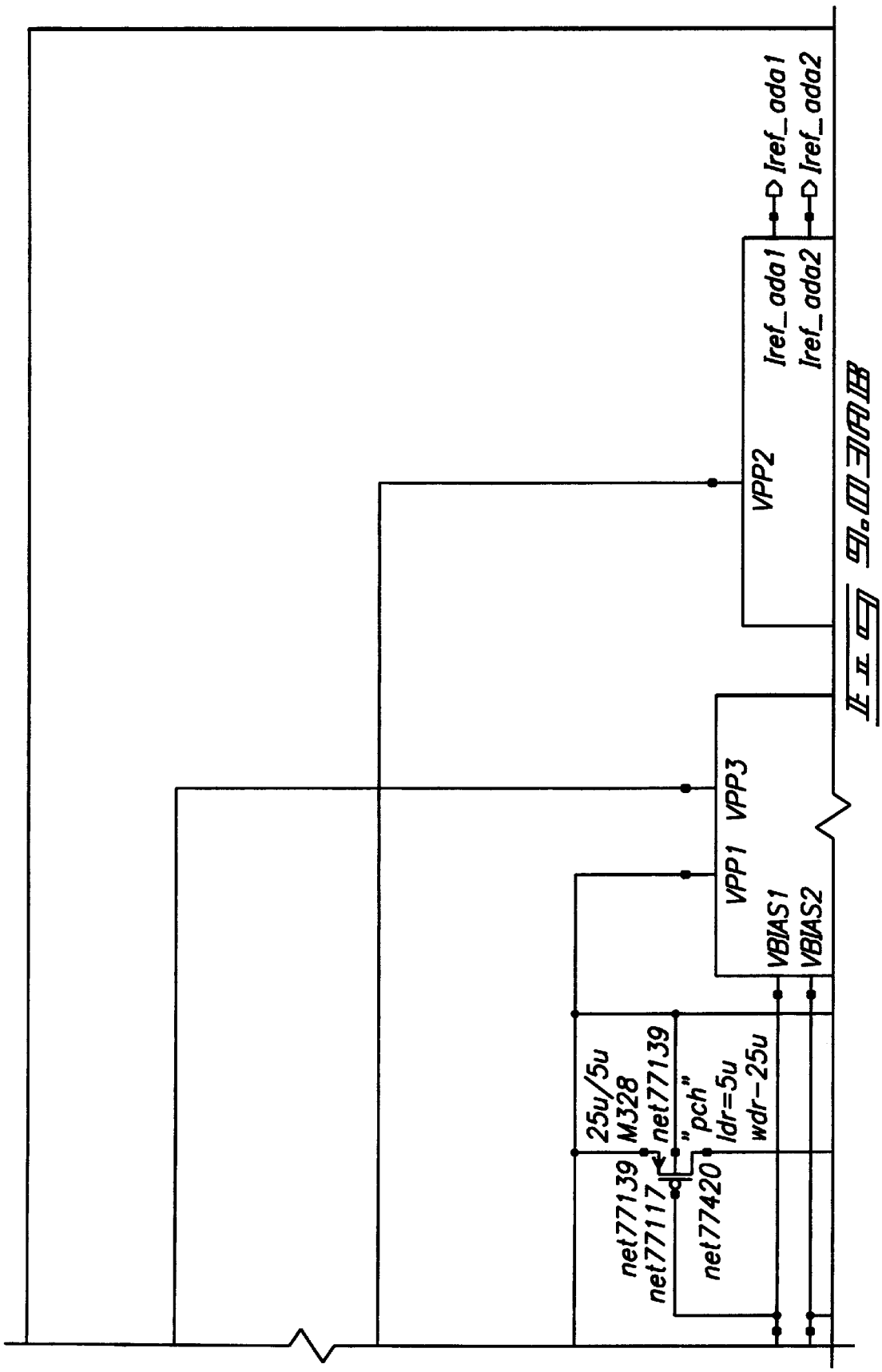

I327
150u/1u
100u/1u
vss!
net77328
metal option
I324
20u/1u
net77128
net77311
P
SUB
NW
I325
c=15.0484p
ldr=50u
wdr=500u
I309
net77136
I296
net11097
c=9.00969p
wdr=300u
I307
net77134
I292
net77139
I295
VPP1
VBIAS1
VBIAS2
I293
12u/1u
ENABLE
8u/1u
net78068
I297
24u/1u
ENBiasOK
BiasOK
nor2
I298
M299
"nch"
4u/300u
ldr=300u
wdr=4u
vdd!
ENBiasOK
BiasOK
ENABLE

FIG. 91


Iref_ada1
Iref_ada2
VPP2
Iref_ada1
Iref_ada2
VPP3
VPP1
VBIAS1
VBIAS2
25u/5u
M328
net77139
"pch"
ldr=5u
wdr=25u
net77139
net77117
net77420

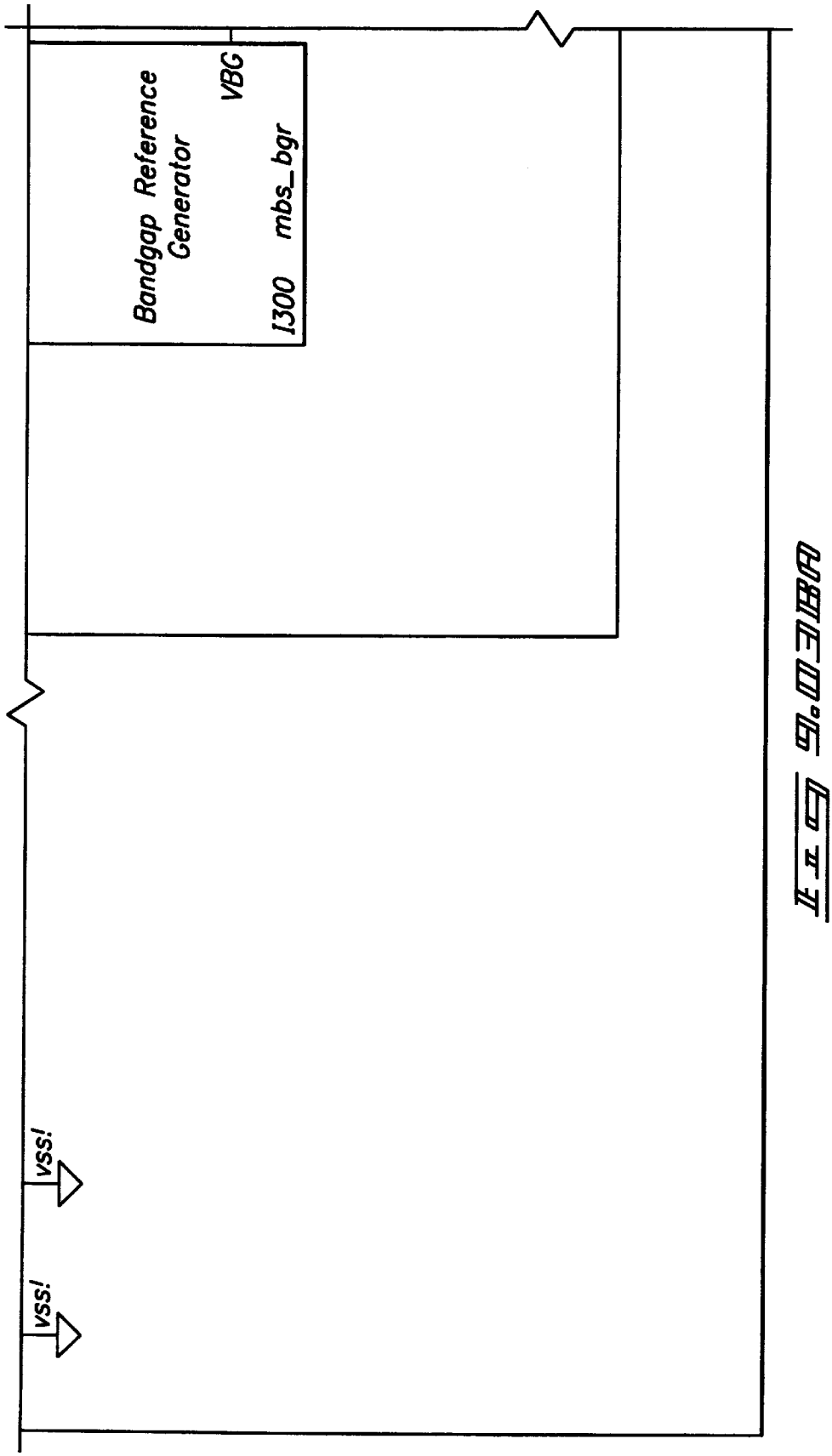


FIG. 96

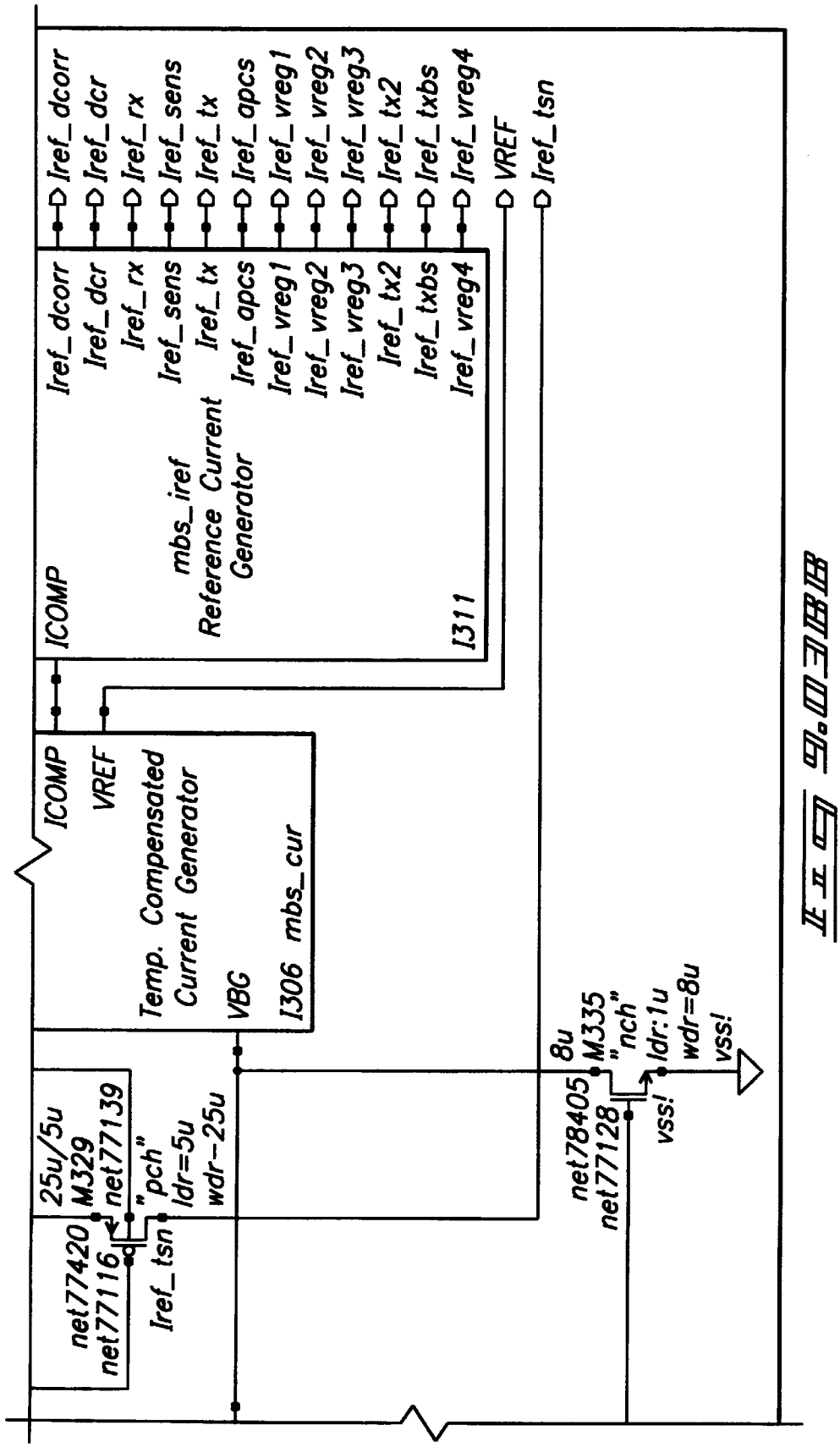

Iref_dcorr
Iref_dcr
Iref_rx
Iref_sens
Iref_tx
Iref_apcs
Iref_vreg1
Iref_vreg2
Iref_vreg3
Iref_tx2
Iref_txbs
Iref_vreg4
VREF
Iref_tsn
ICOMP
mbs_iref
Reference Current
Generator
I311
ICOMP
VREF
Temp. Compensated
Current Generator
VBG
I306 mbs_cur
25u/5u
M329
net77139
"pch"
ldr=5u
wdr=25u
net77420
net77116
Iref_tsn
8u
M335
"nch"
ldr:1u
wdr=8u
vss!
net78405
net77128
vss!

FIG. 6.0E+03

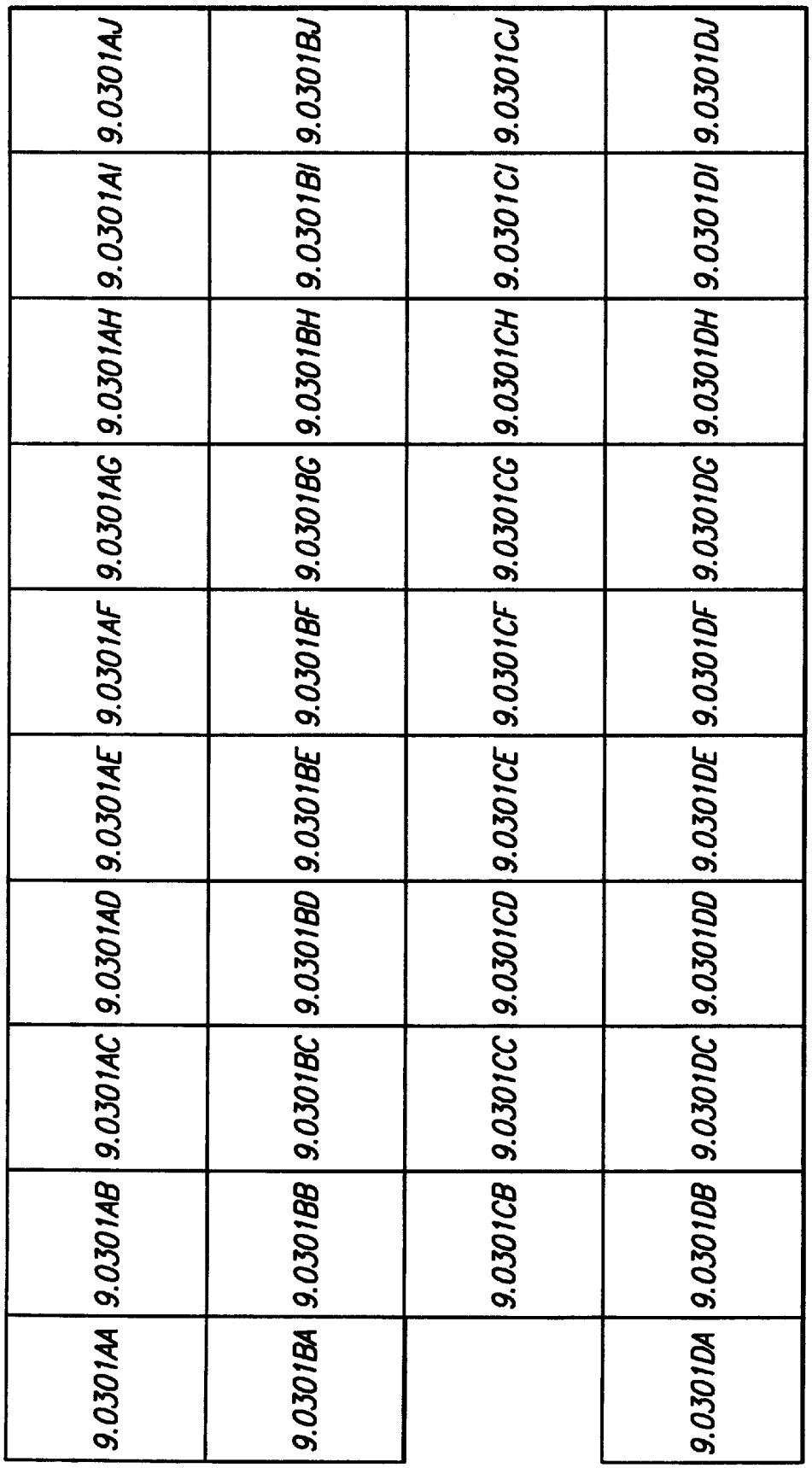

9.0301AA
9.0301AB
9.0301AC
9.0301AD
9.0301AE
9.0301AF
9.0301AG
9.0301AH
9.0301AI
9.0301AJ
9.0301BA
9.0301BB
9.0301BC
9.0301BD
9.0301BE
9.0301BF
9.0301BG
9.0301BH
9.0301BI
9.0301BJ
9.0301CB
9.0301CC
9.0301CD
9.0301CE
9.0301CF
9.0301CG
9.0301CH
9.0301CI
9.0301CJ
9.0301DA
9.0301DB
9.0301DC
9.0301DD
9.0301DE
9.0301DF
9.0301DG
9.0301DH
9.0301DI
9.0301DJ

FIG. 9.0301

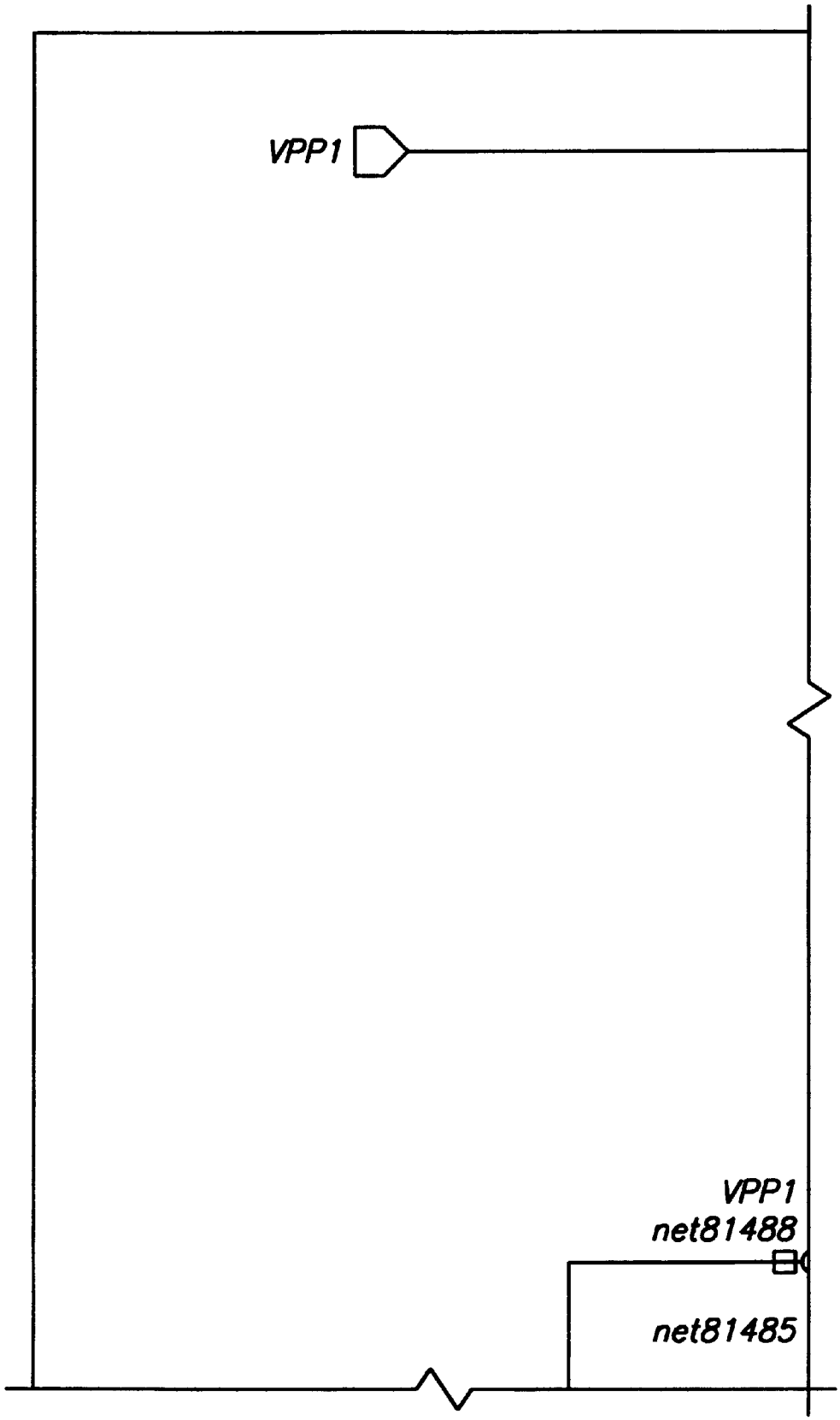


Fig 9.0030AA

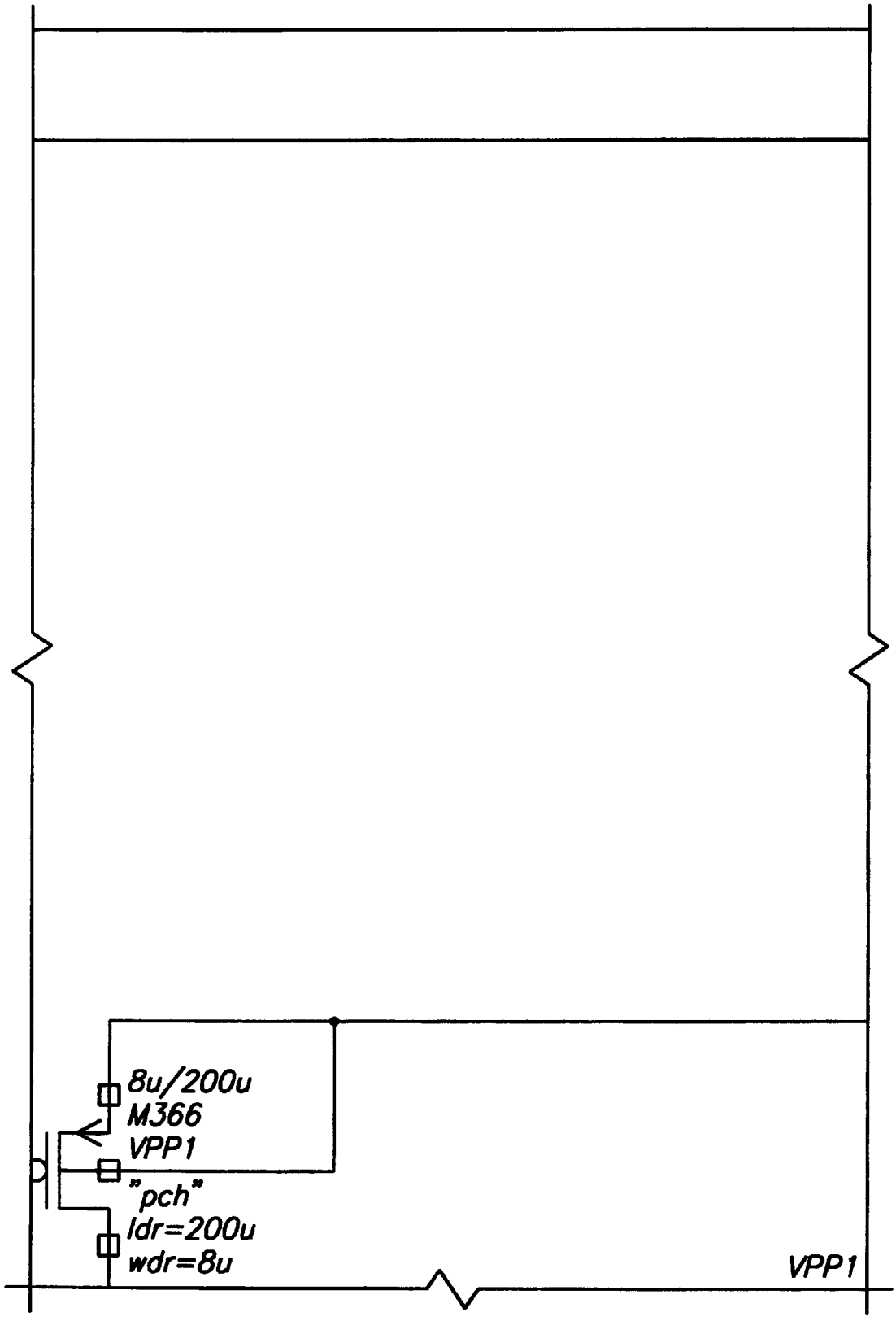
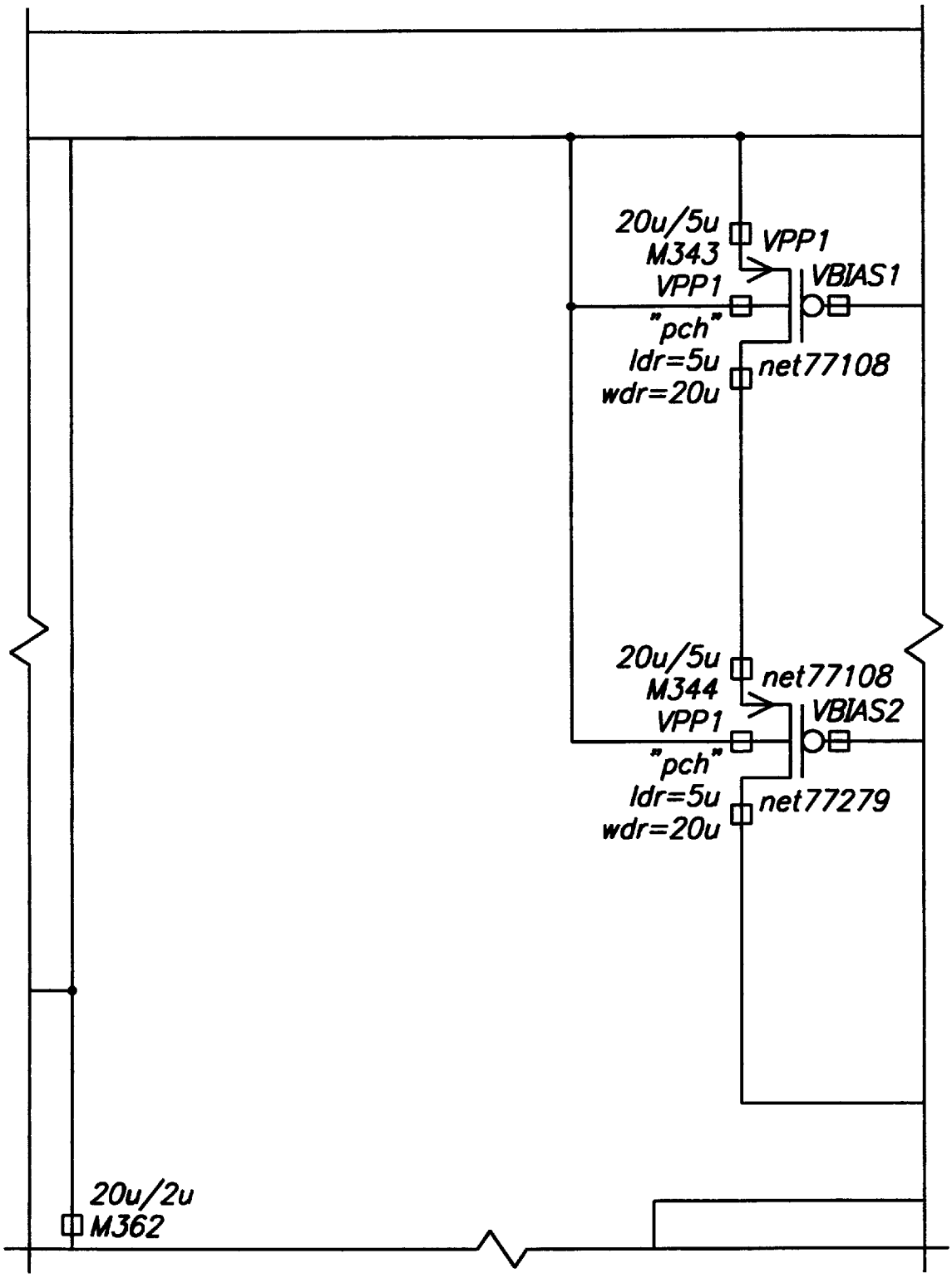


Fig 9.0301AB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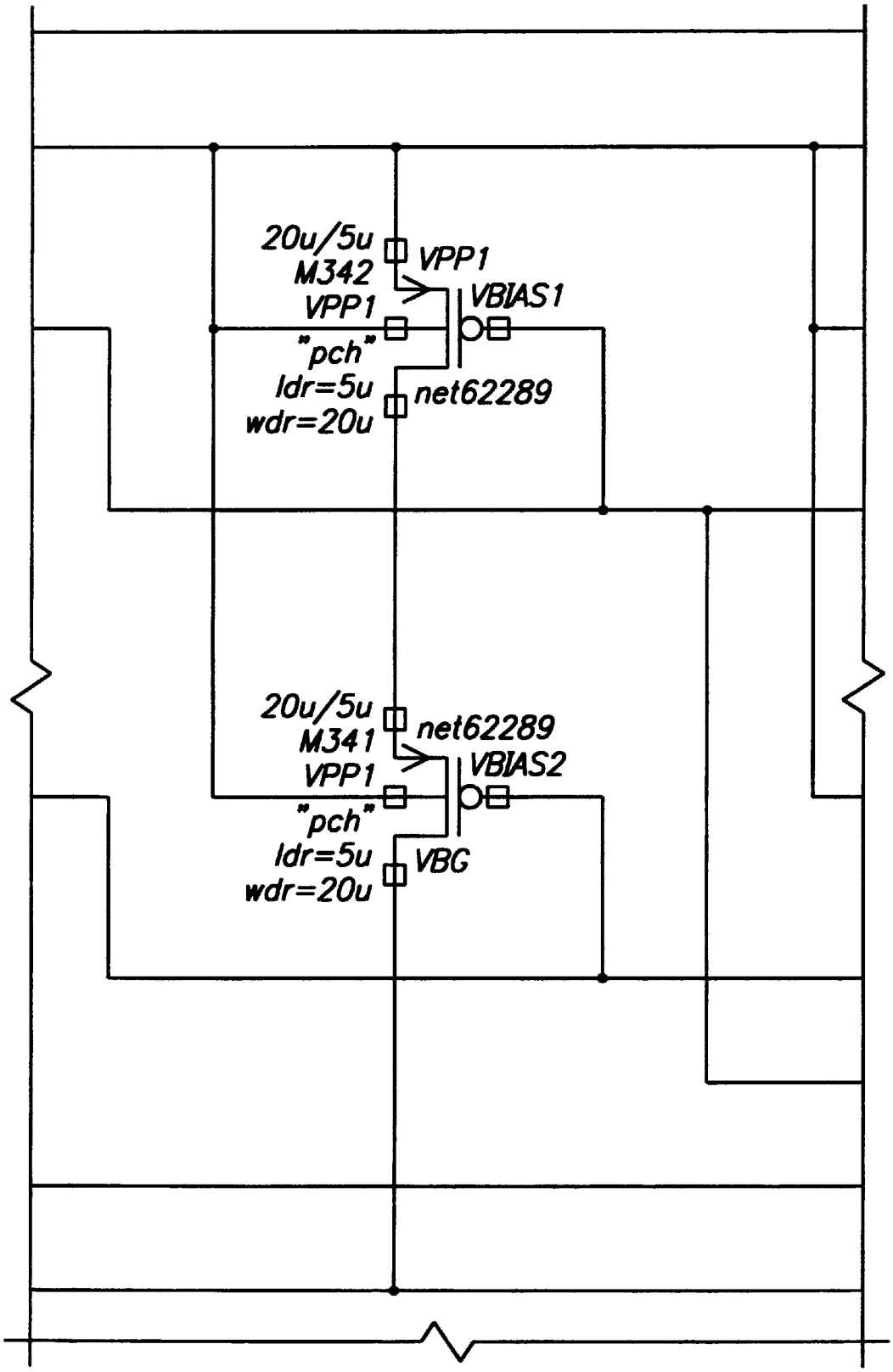
20u/2u
M362

Fig 9.0301AC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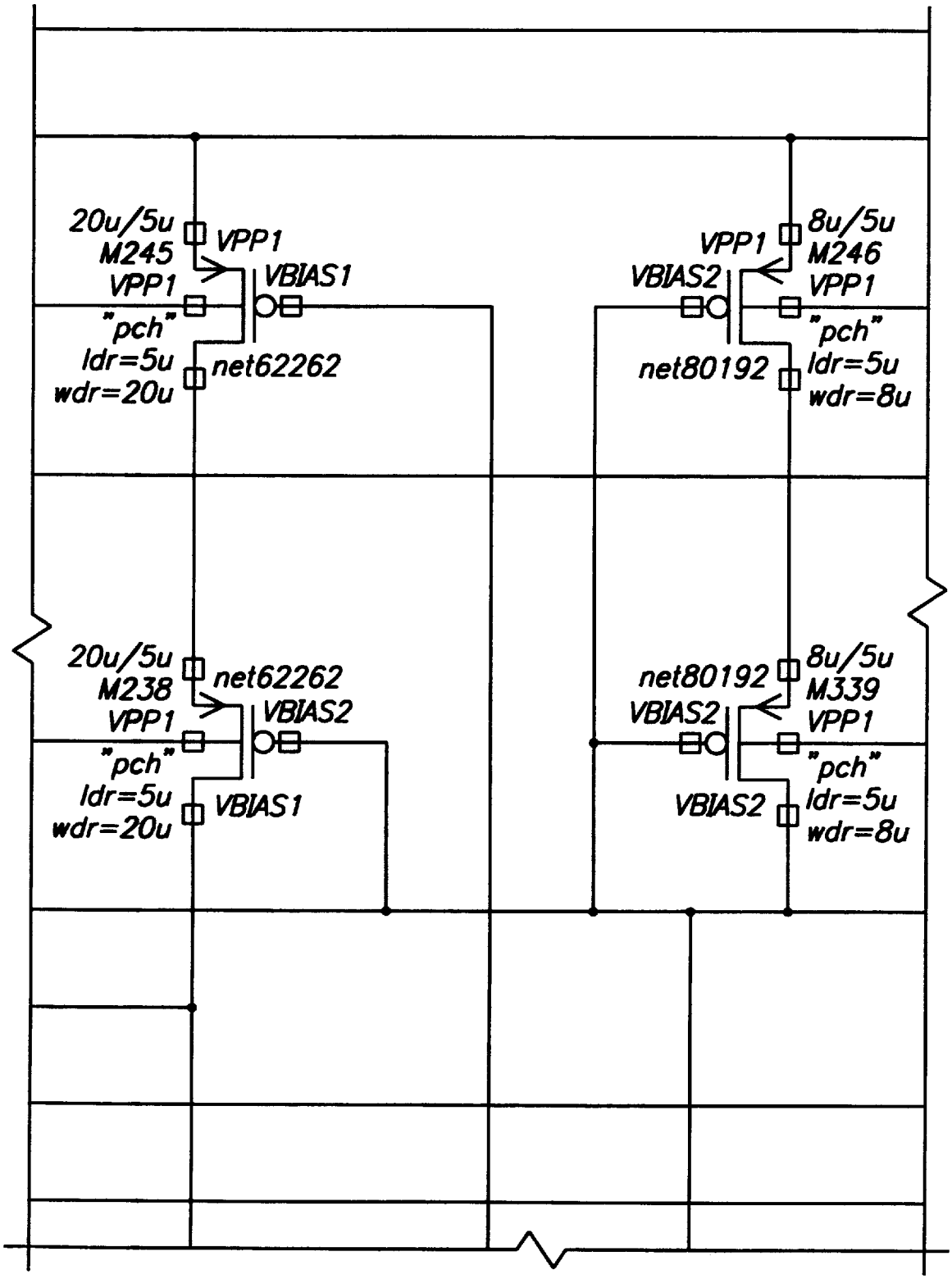
VBIAS2
VBG

Fig 9.0300AD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20u/5u
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VBIAS2
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VPP1
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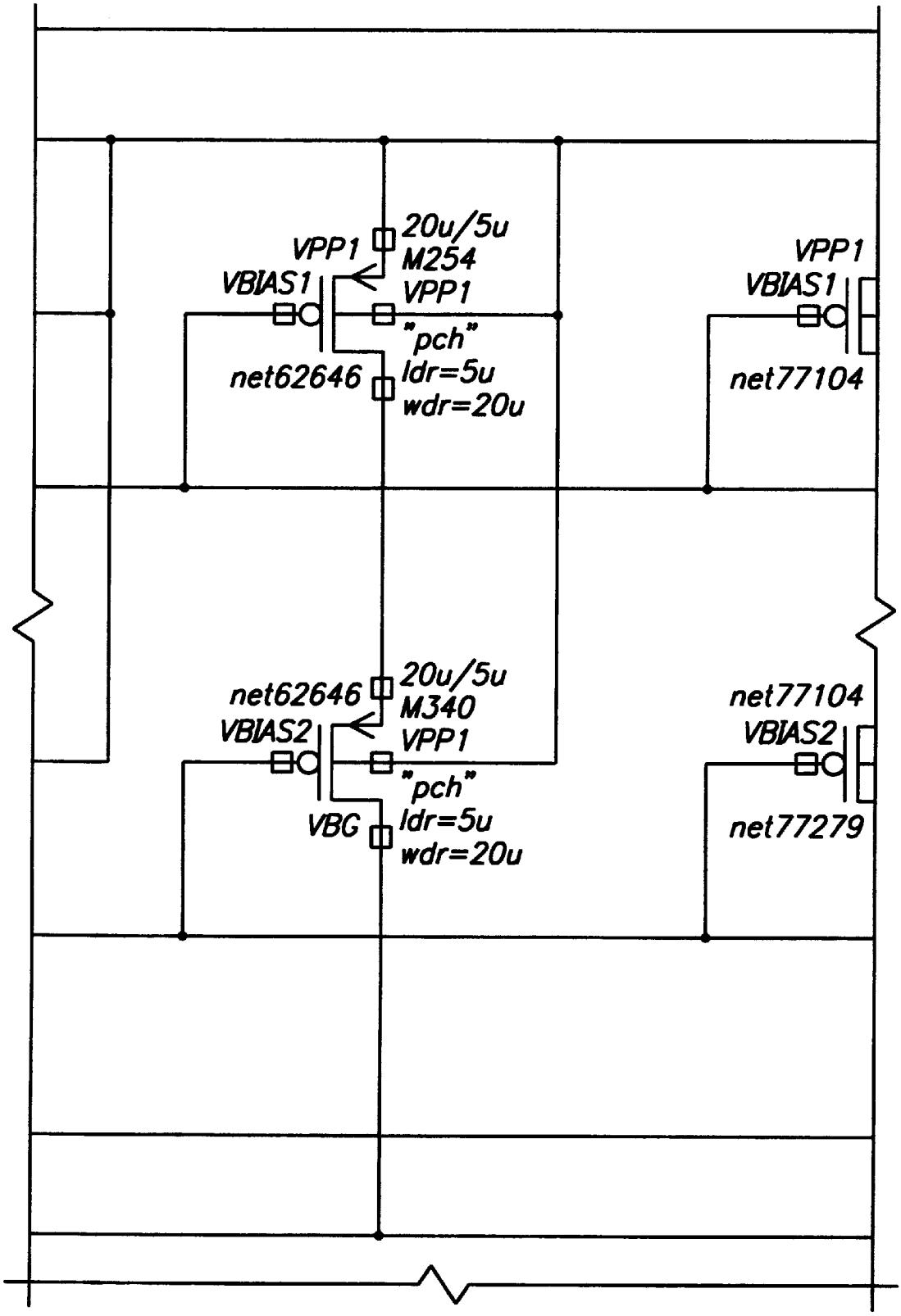
wdr=8u

Fig 9.0301AE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20u/5u
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VBIAS2
net77279

Fig 9.0301AF

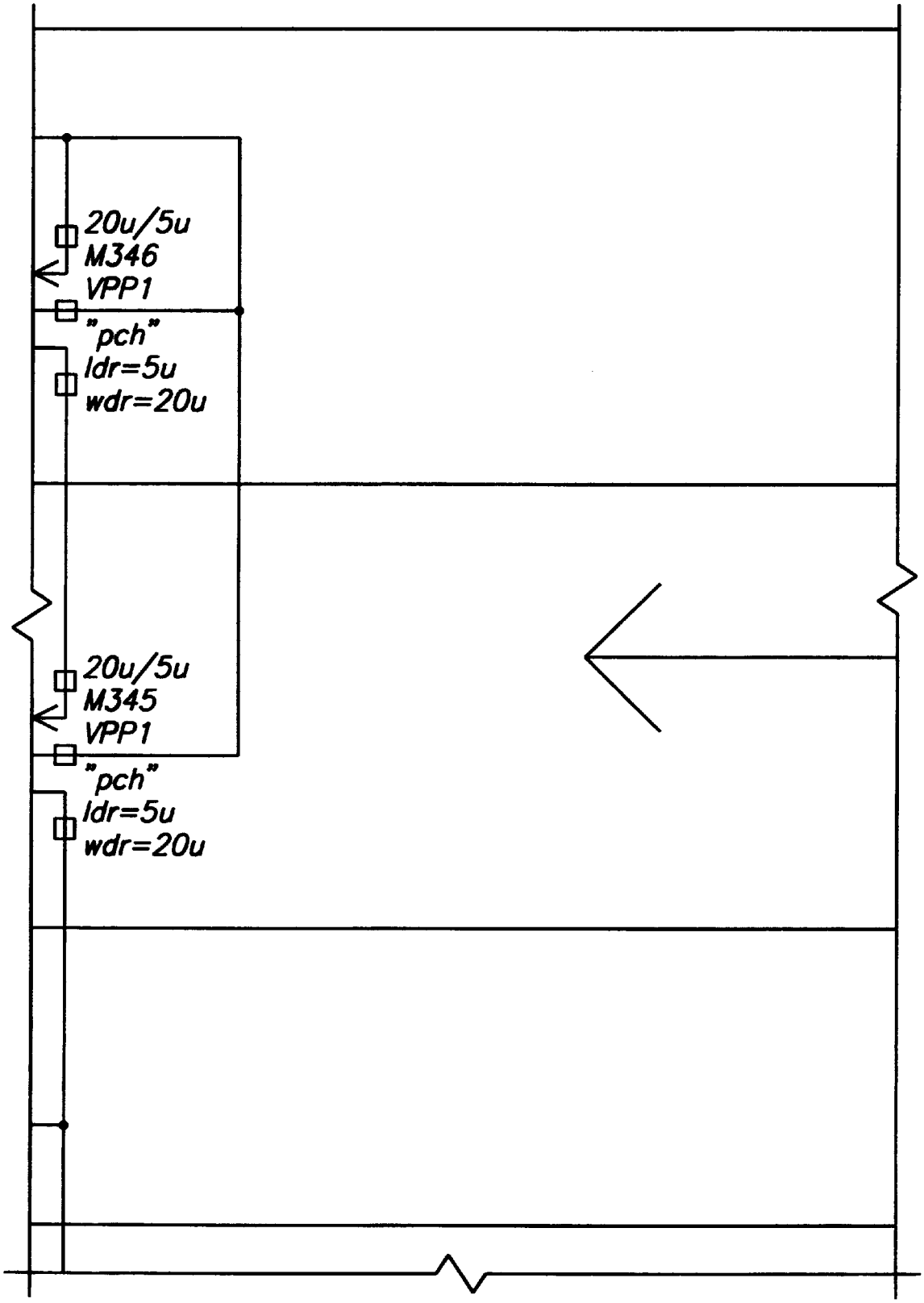


FIG 9.0300 1AG

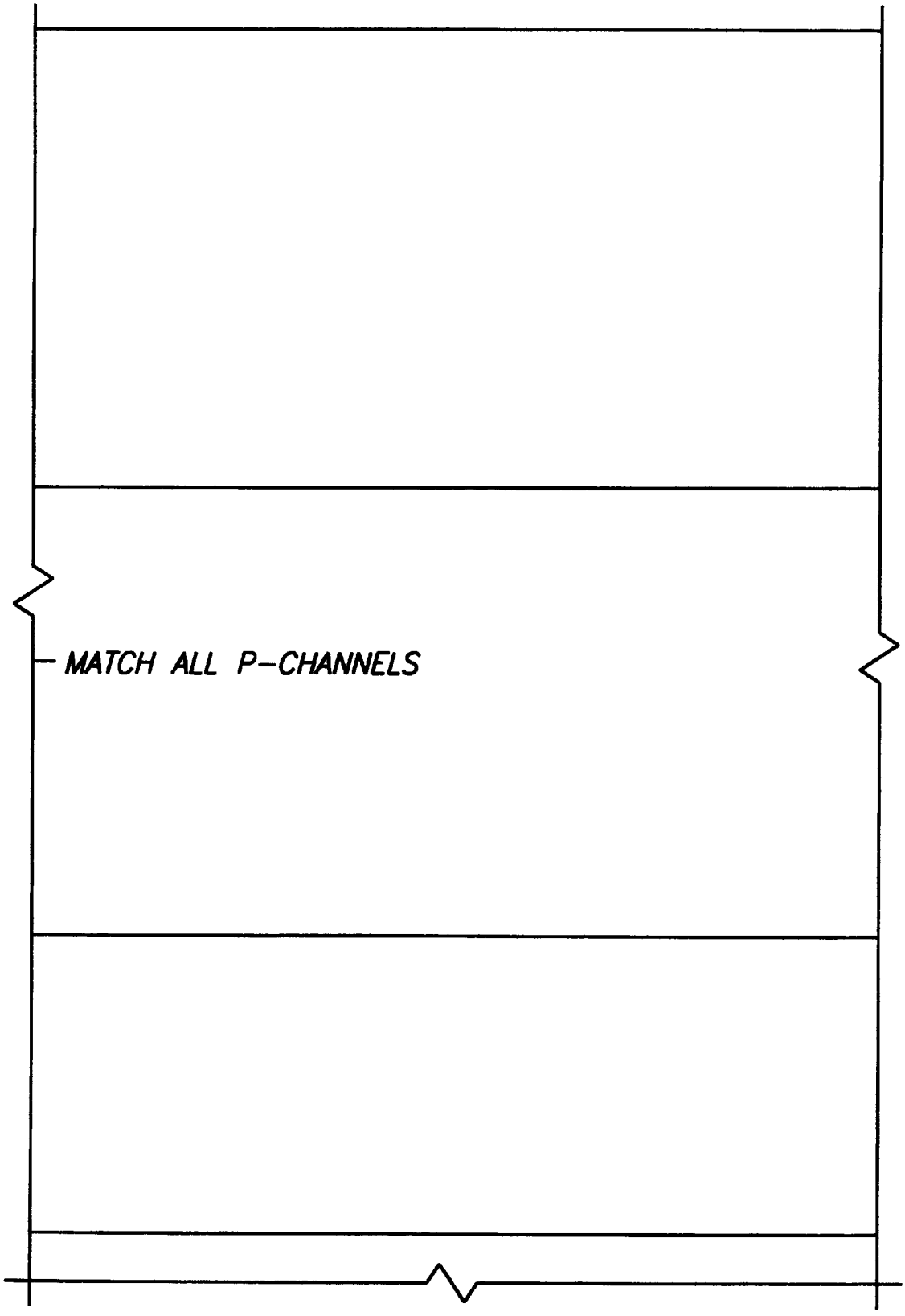


Fig 9.0301AH

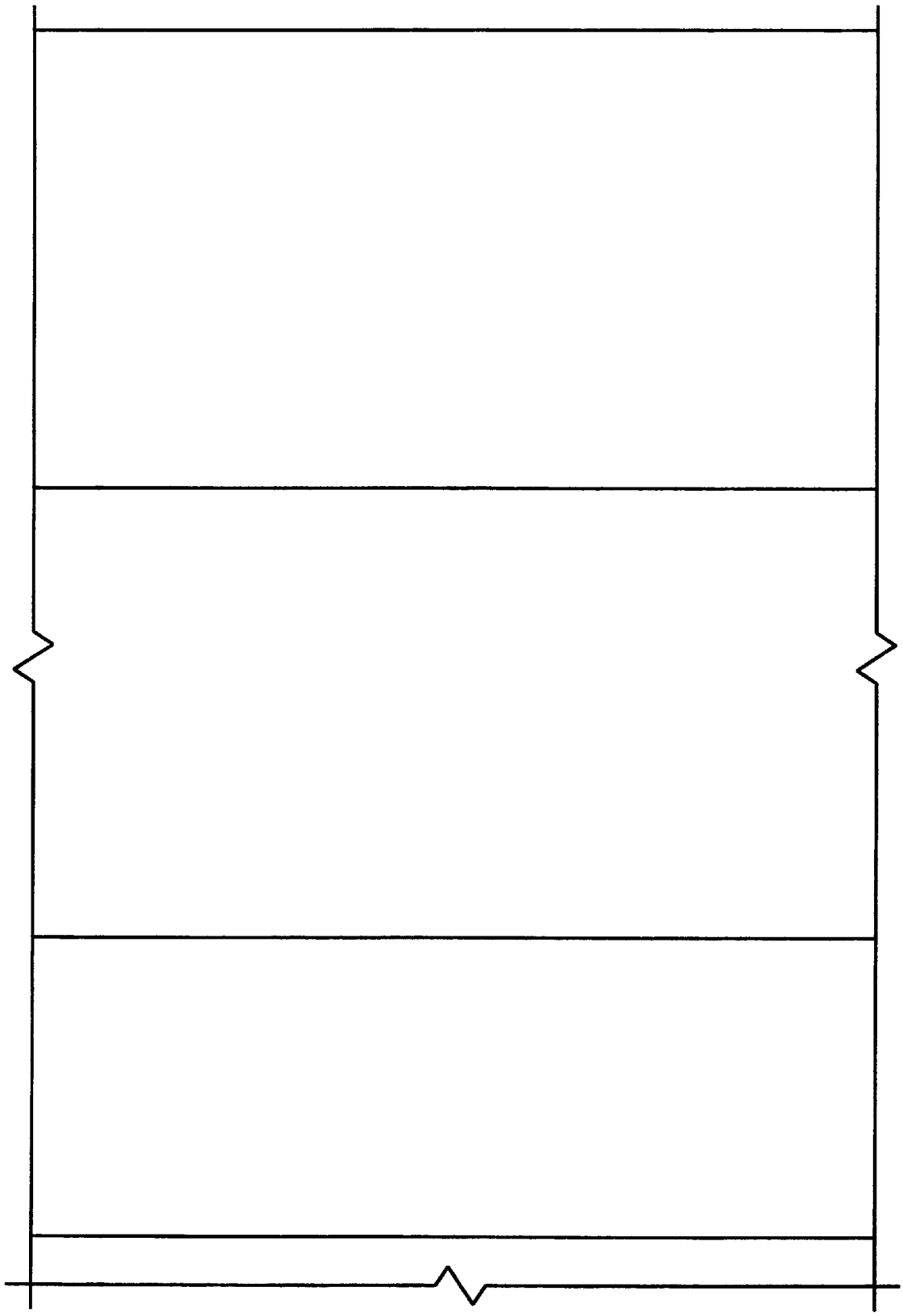


Fig 9.0301AII

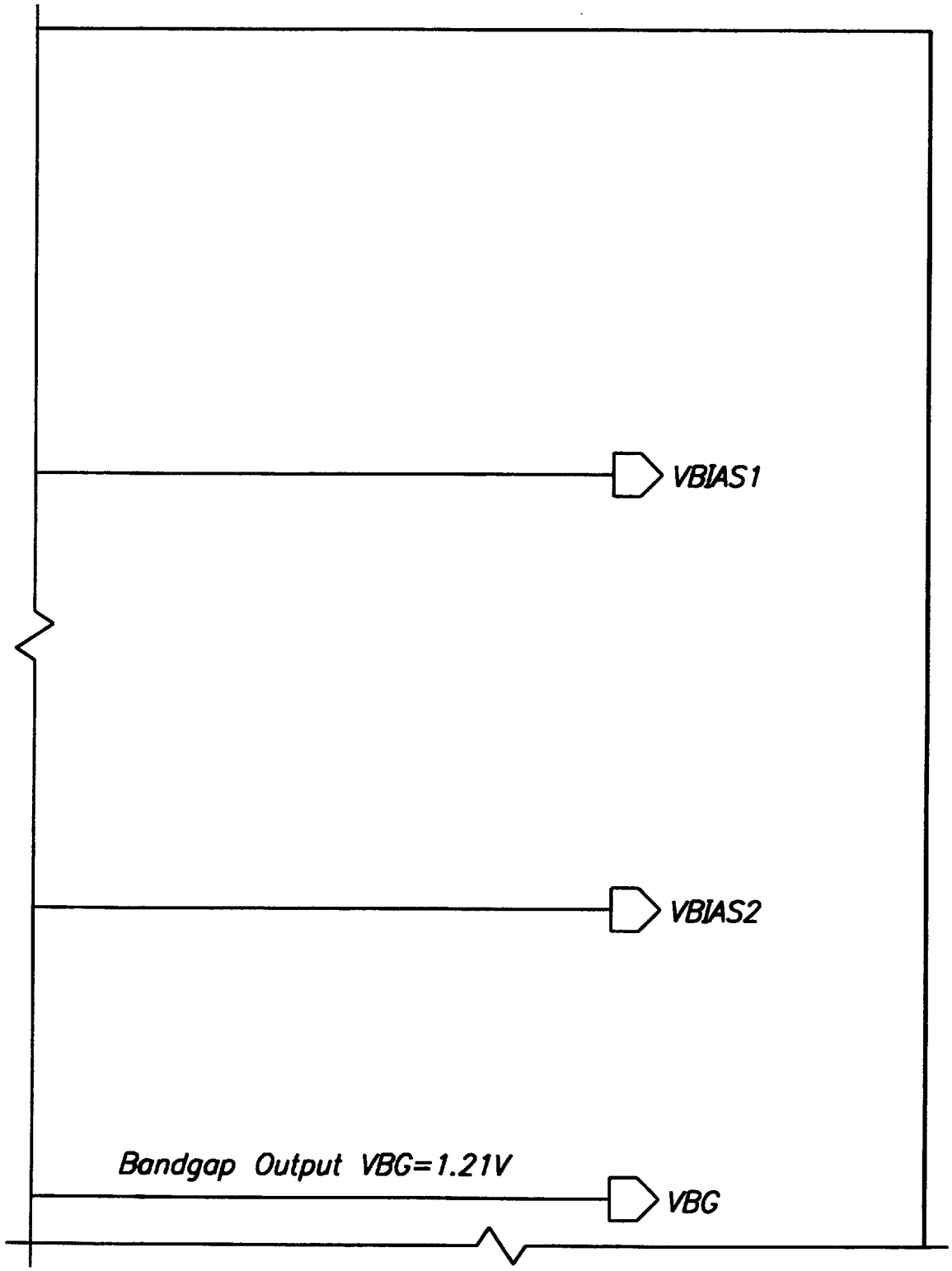
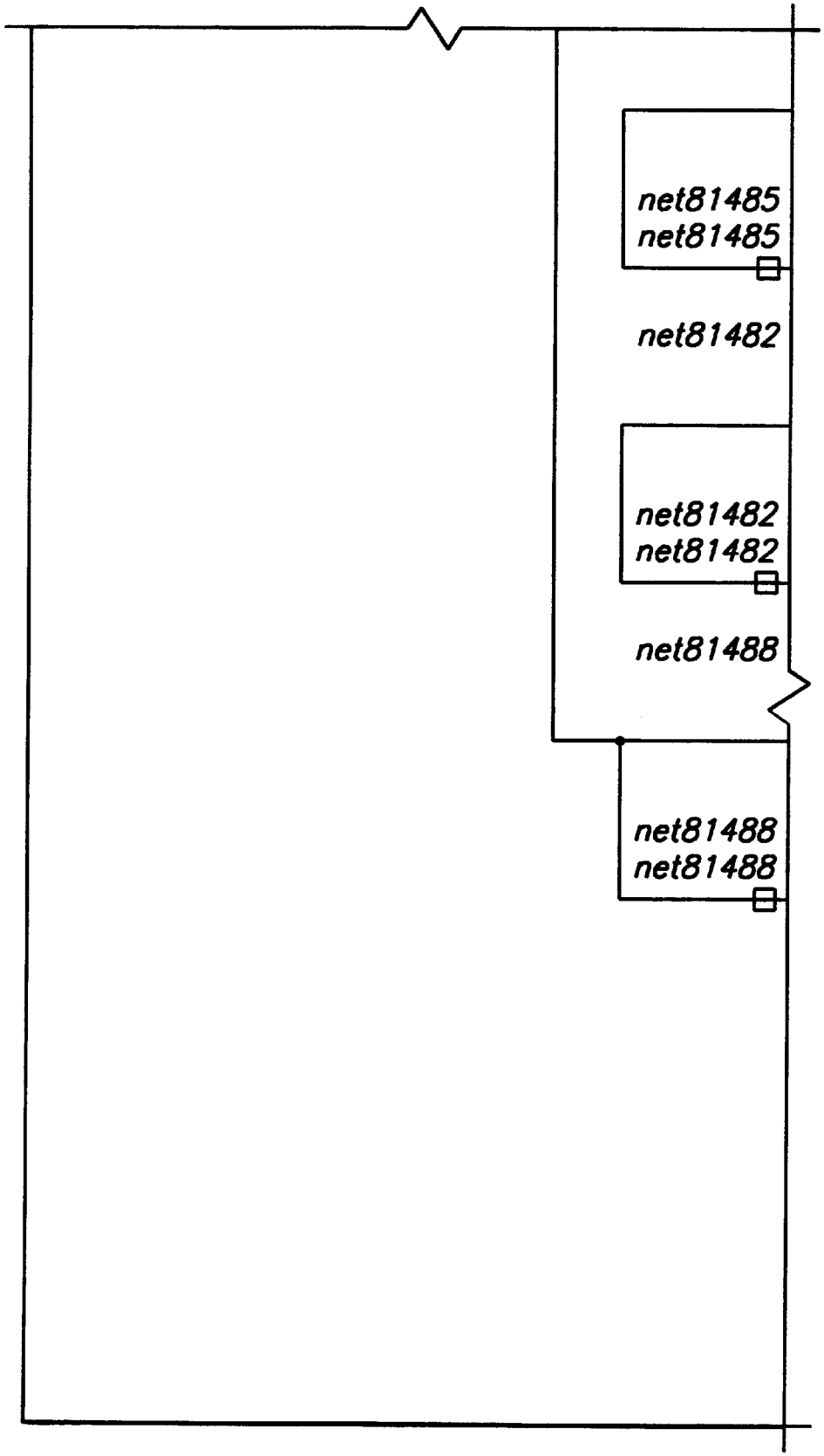


Fig 9.0301Aa1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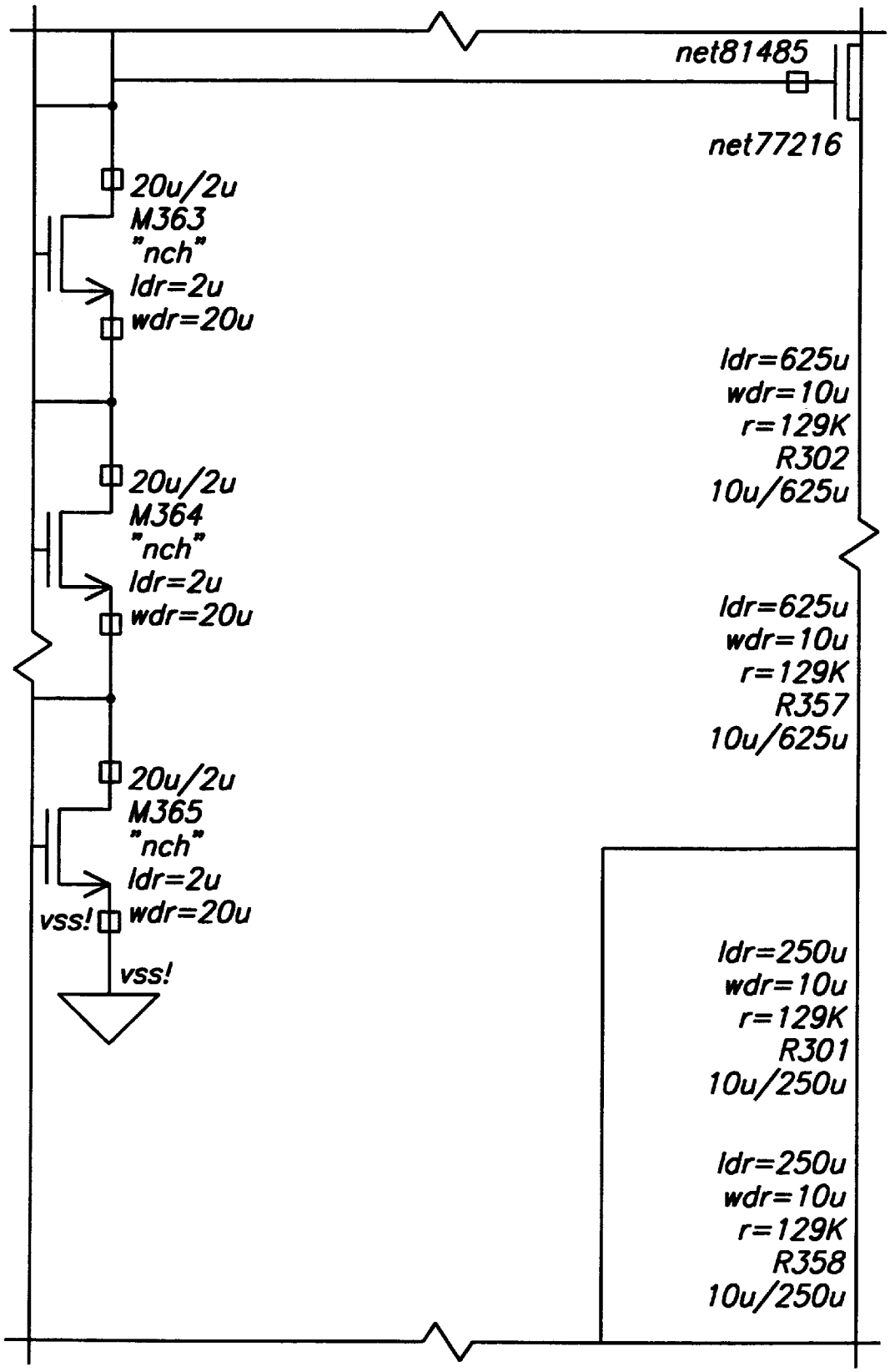
net81488

FIG 9.0301BA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wdr=10u
r=129K
R357
10u/625u
20u/2u
M365
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wdr=20u
vss!
vss!
ldr=250u
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10u/250u
ldr=250u
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r=129K
R358
10u/250u

Fig 9.030188

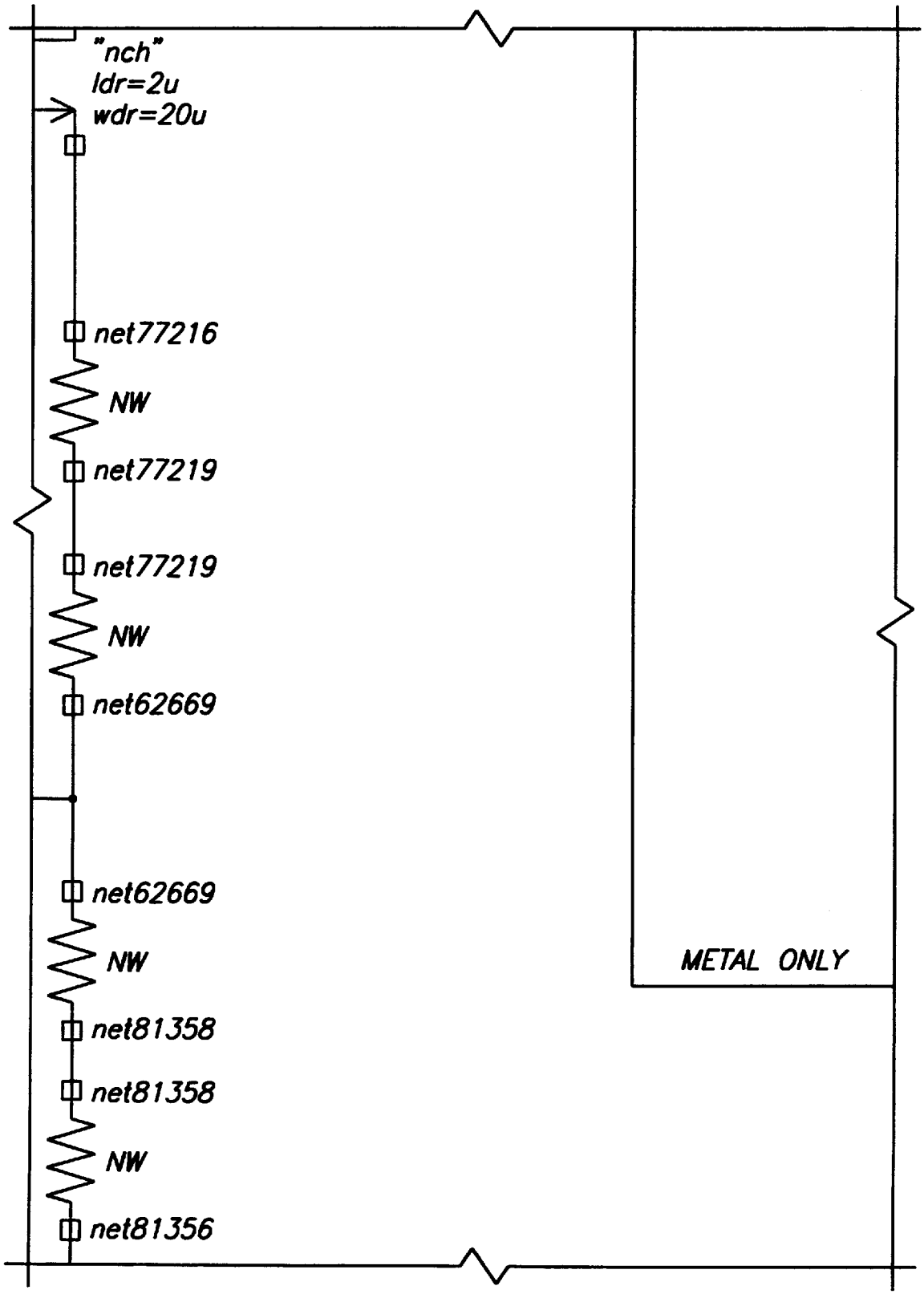


Fig 9.030118C

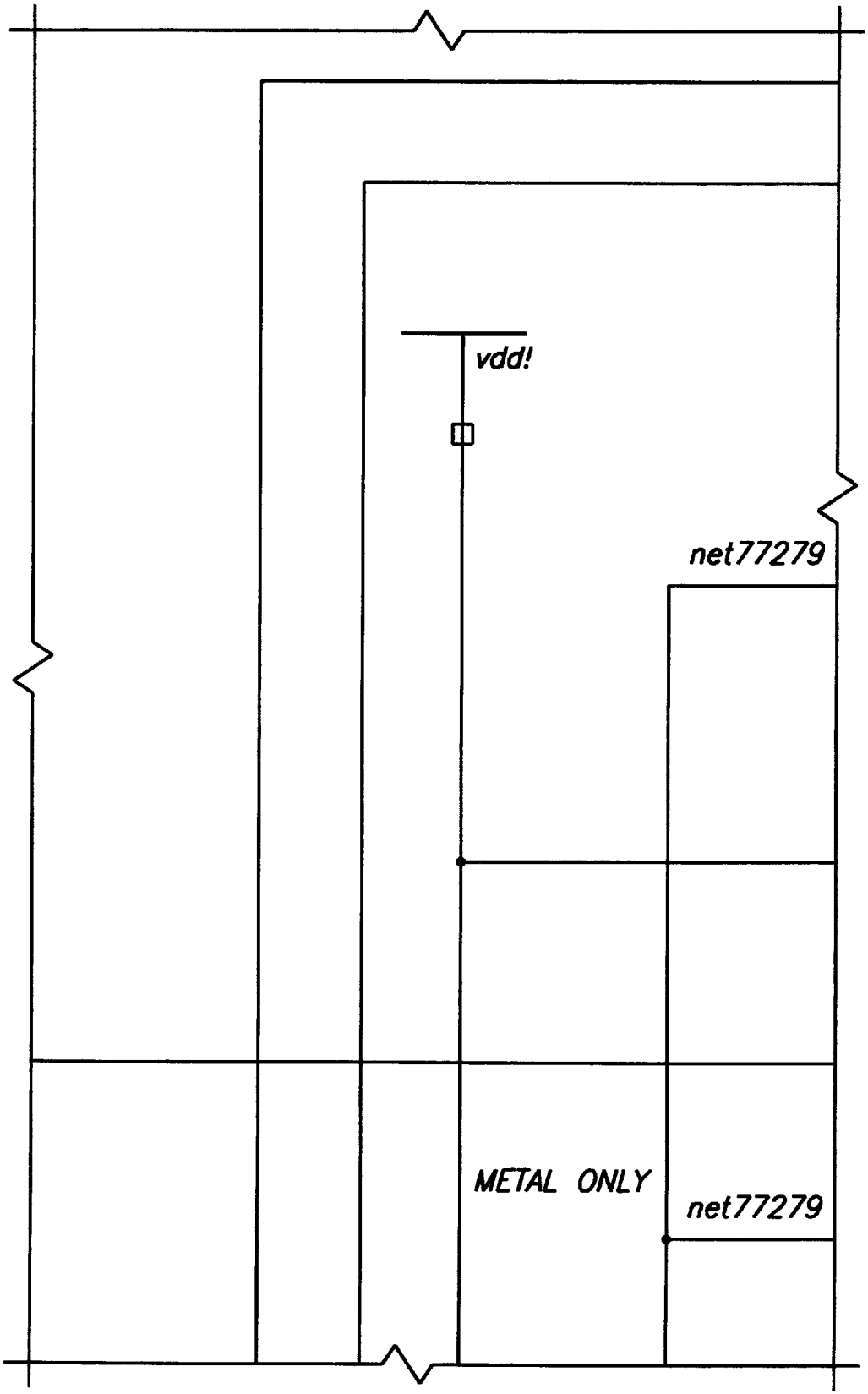


Fig 9.00300IBD

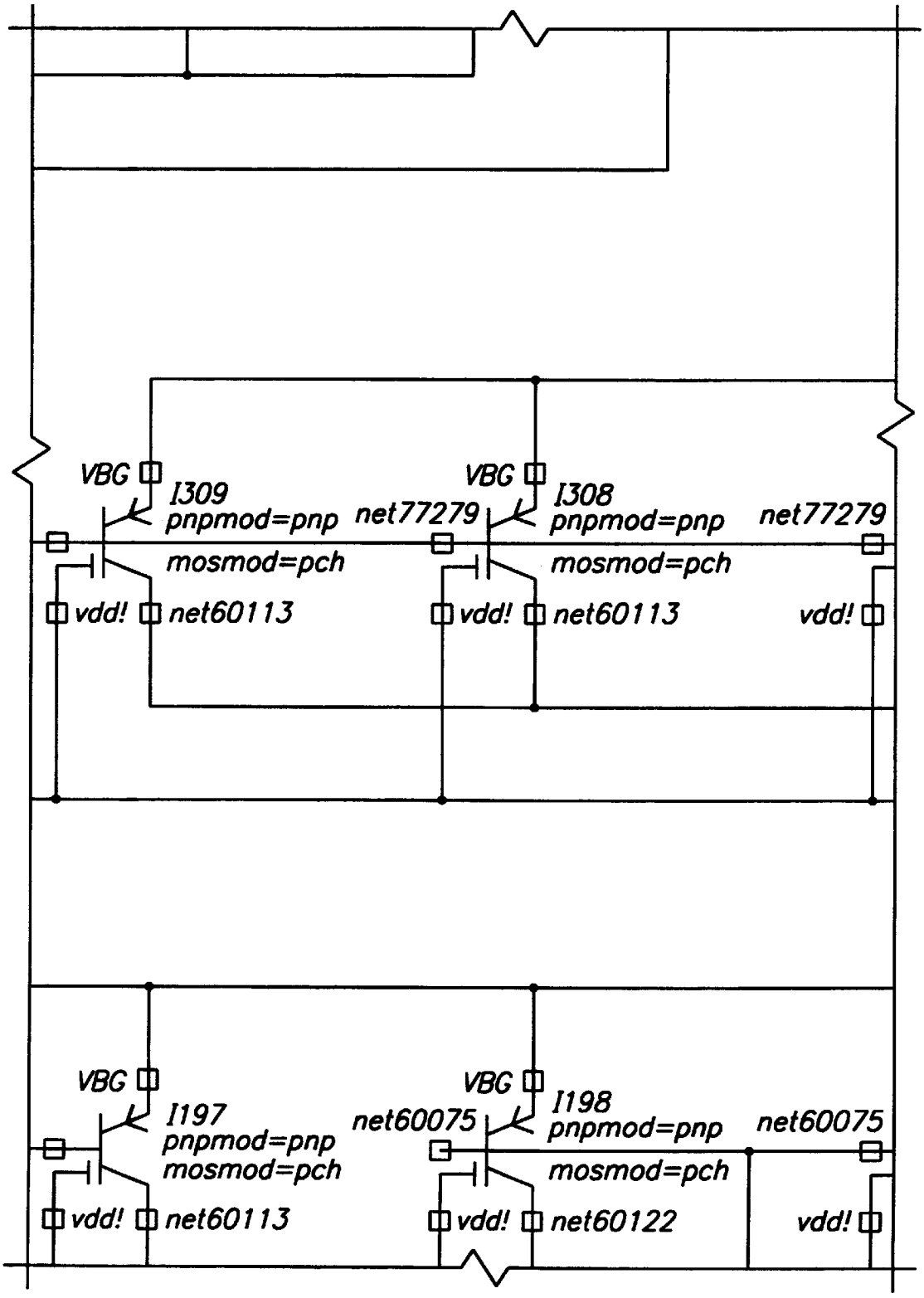
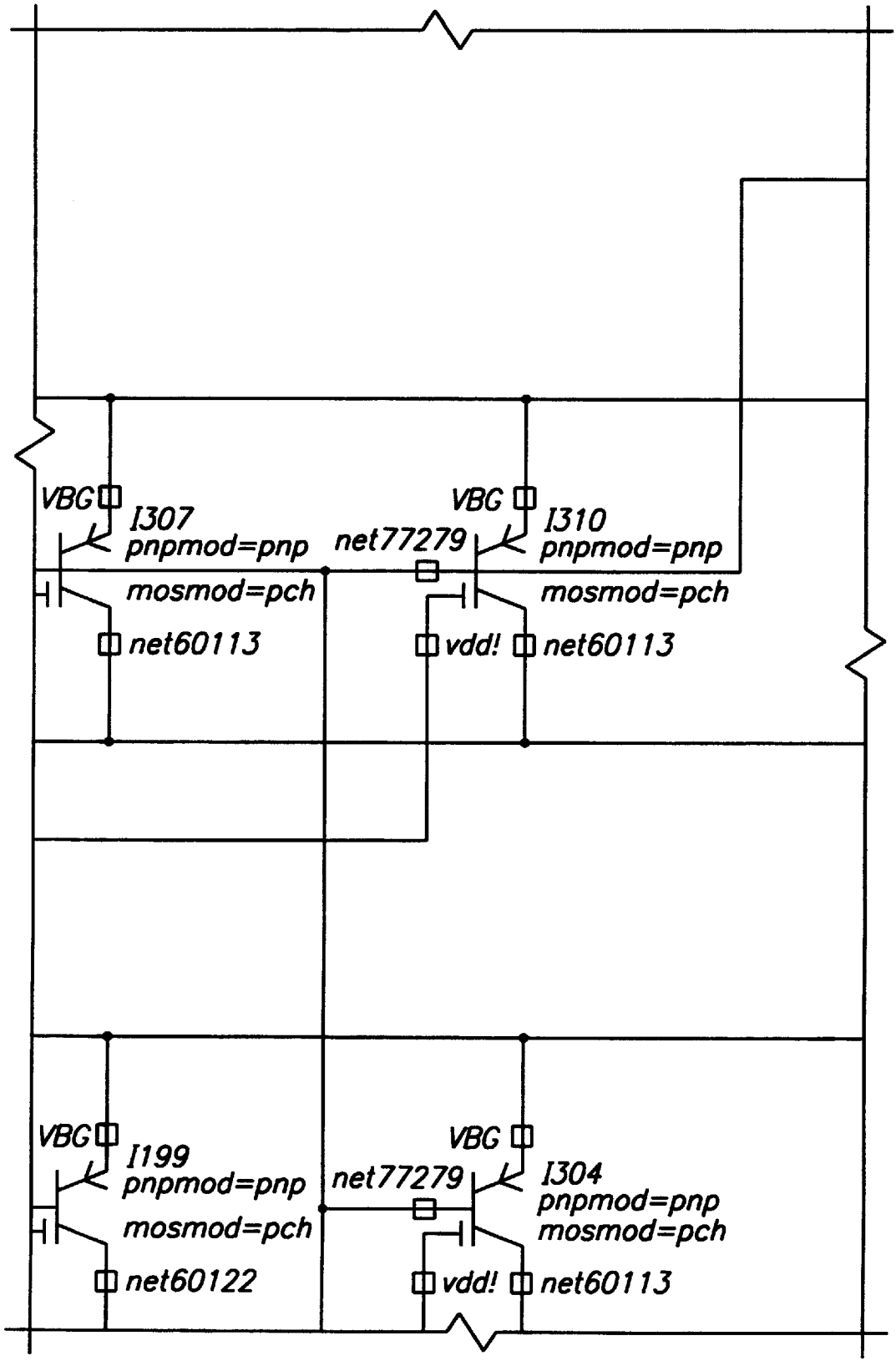


Fig 9.0300 IBE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I199
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mosmod=pch
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net60113

Fig 9.0301BF

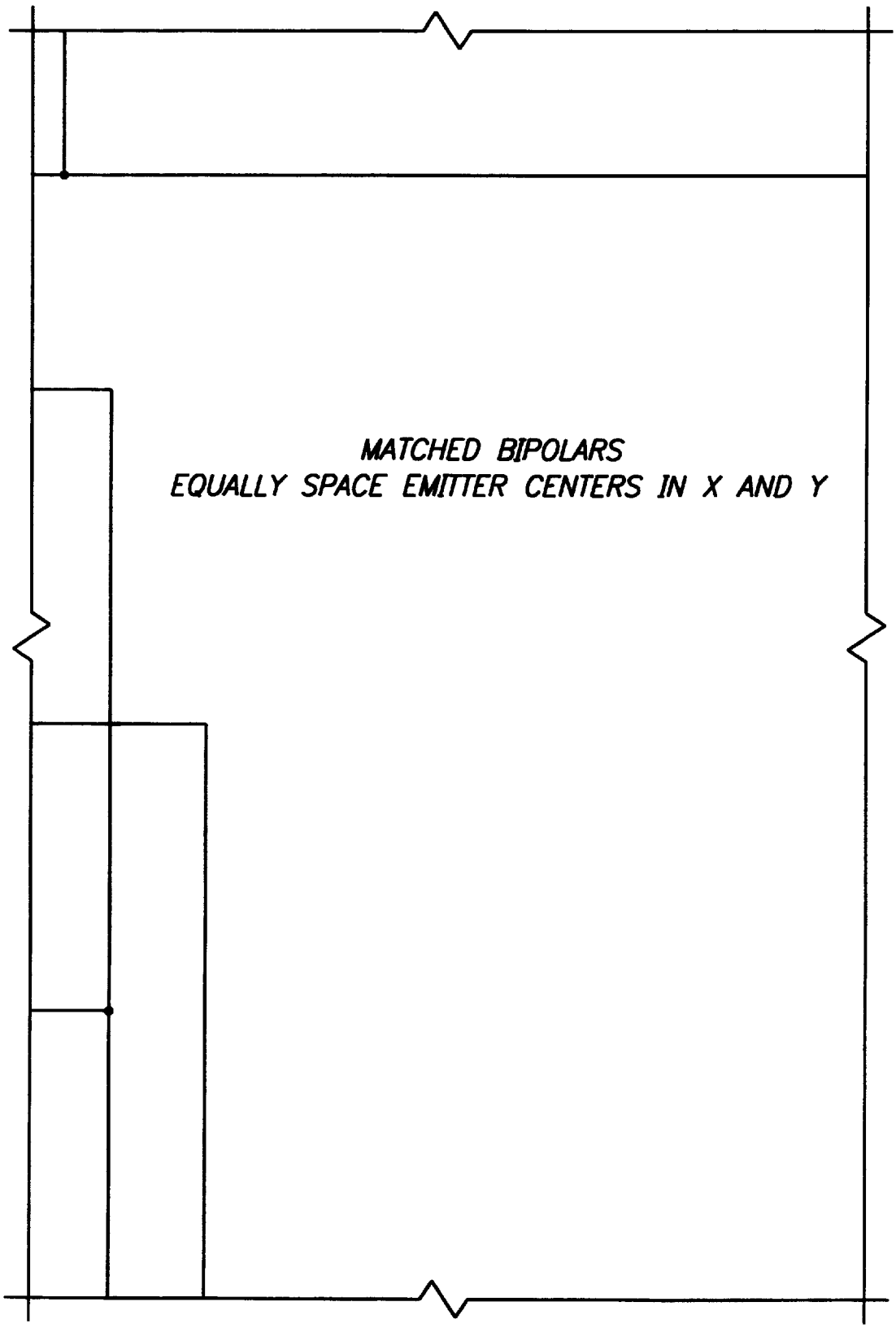

Fig 9.0301186

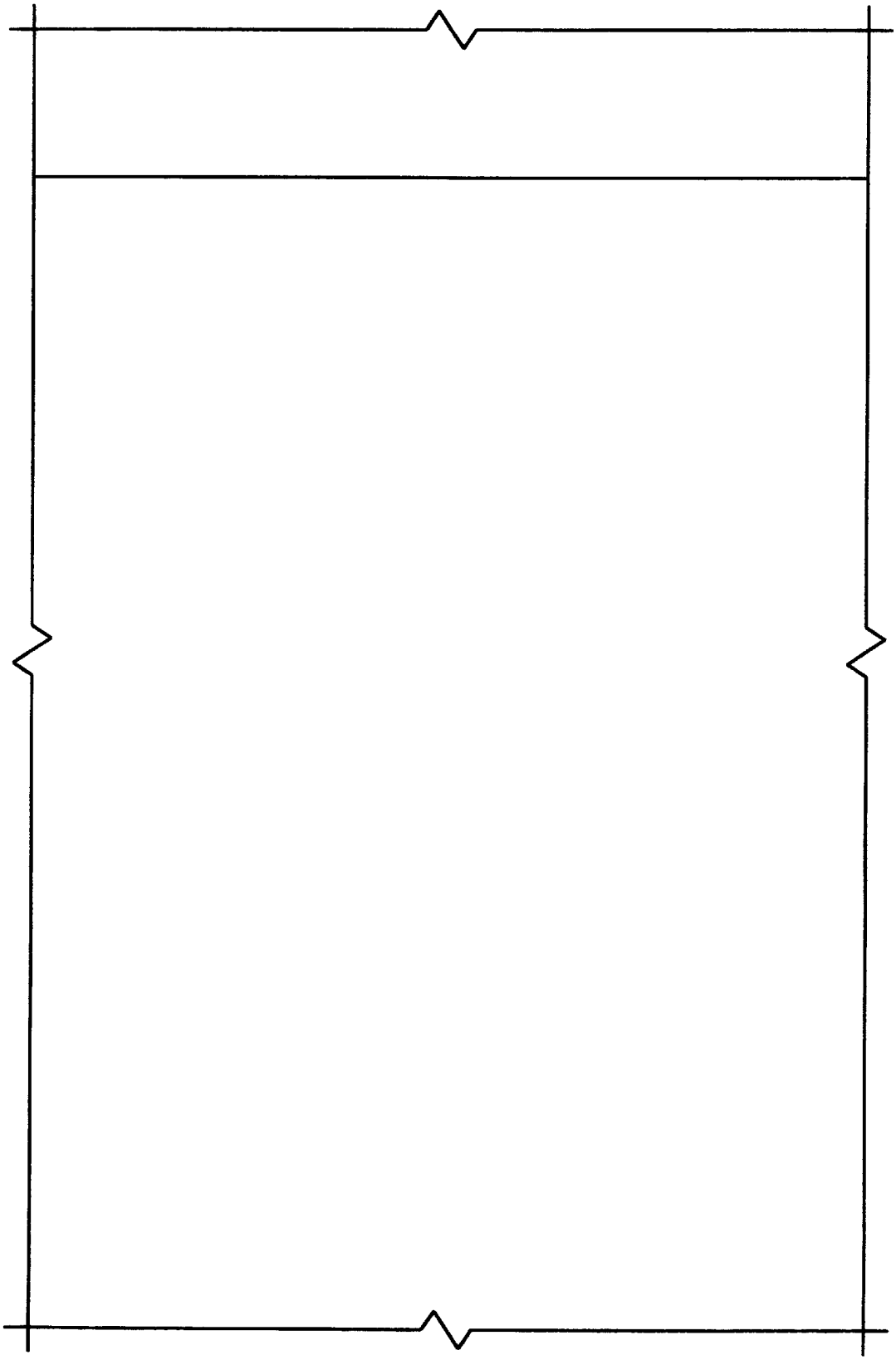

Fig 9.0301BH

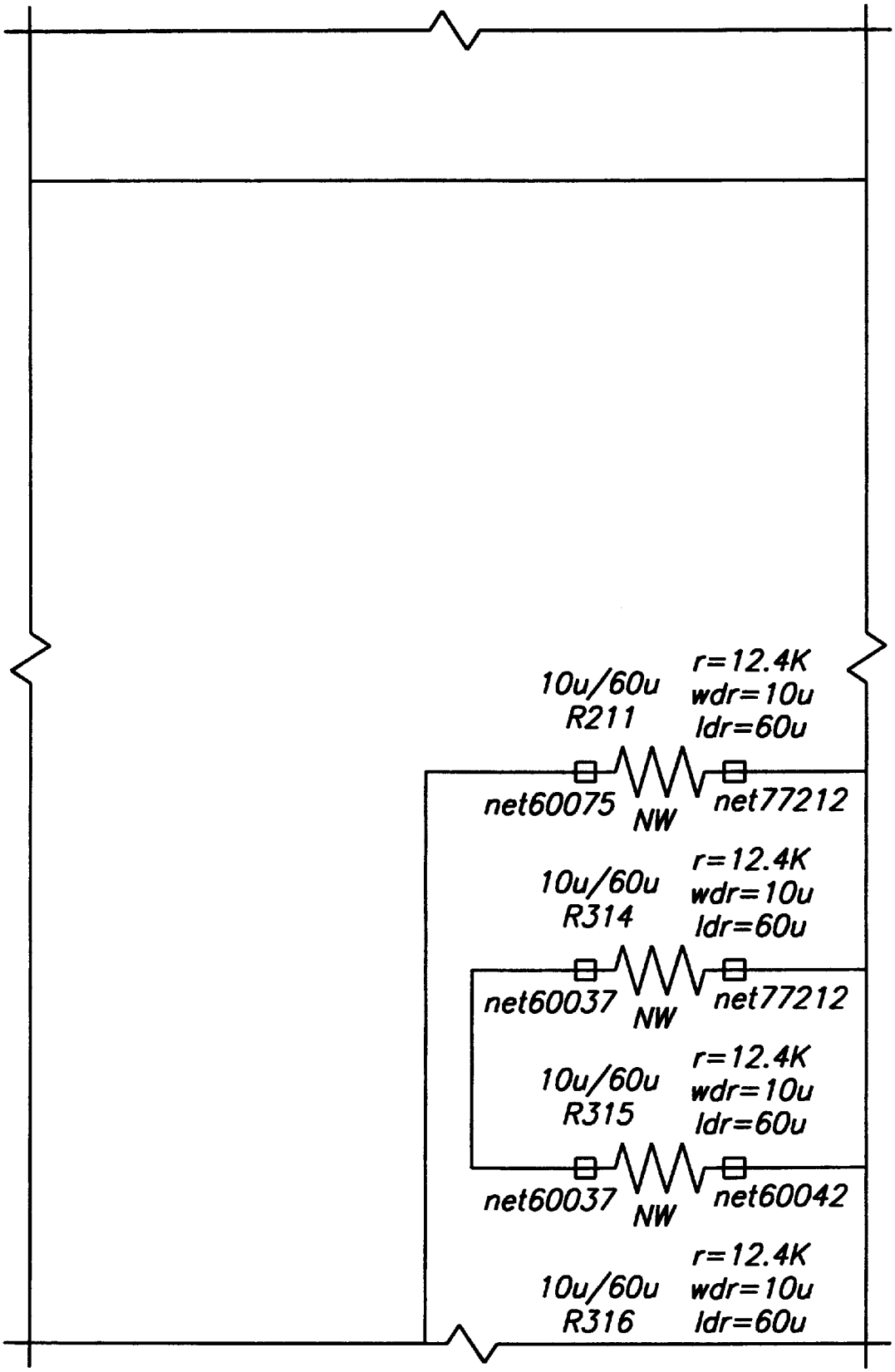

Fig 9.0300IIBII

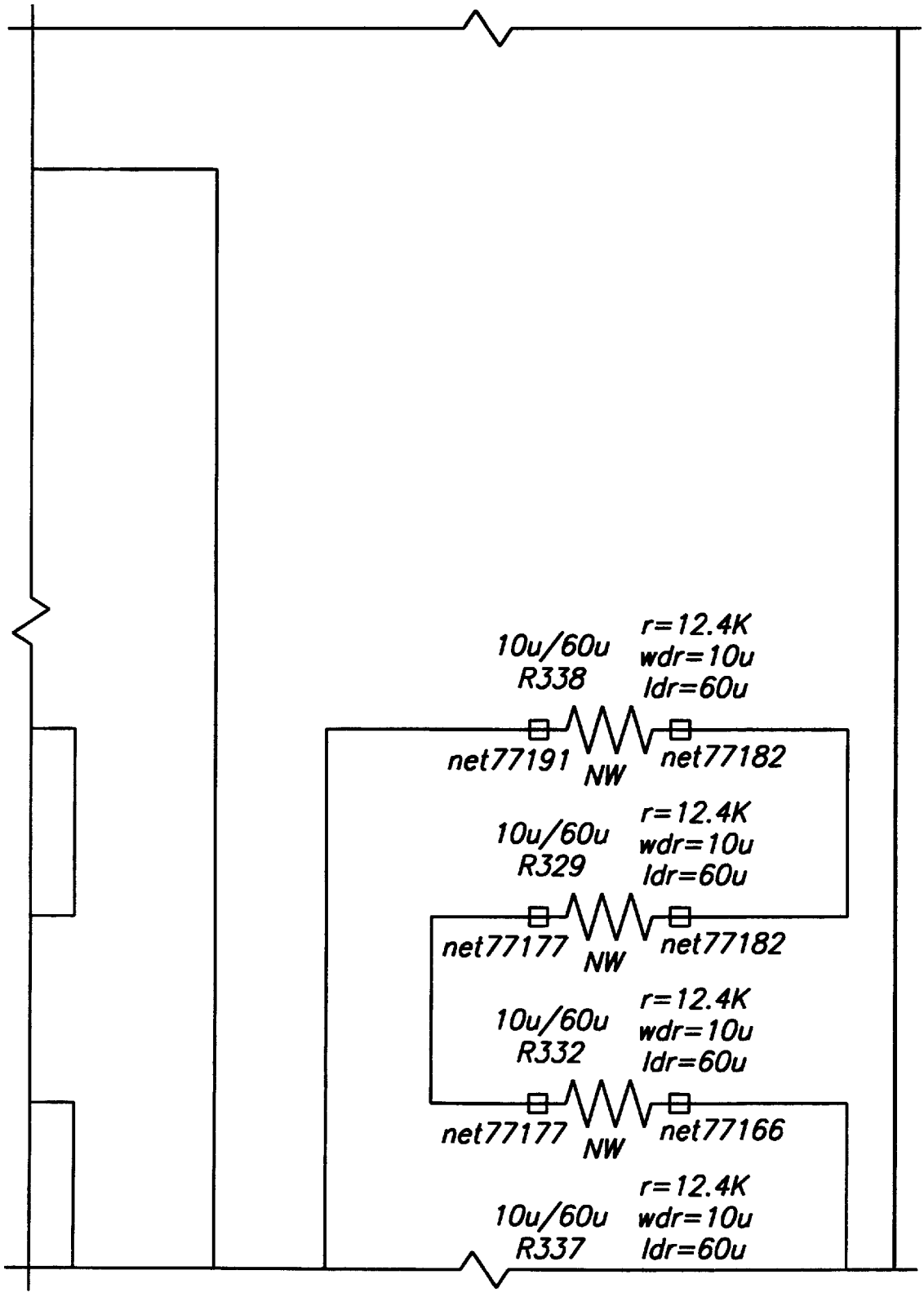
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Fig 9,030,180

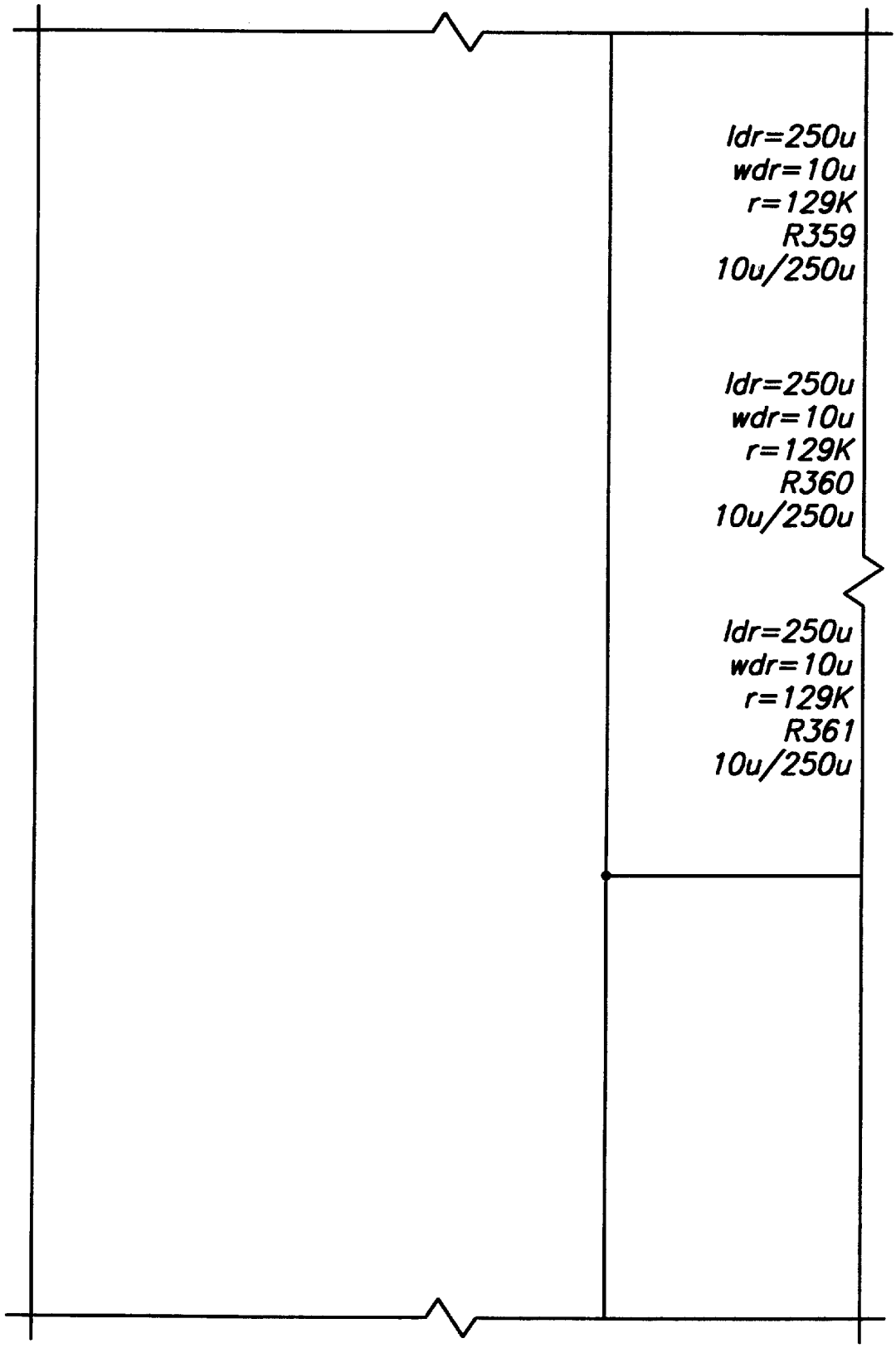

Fig 9.0300ICB

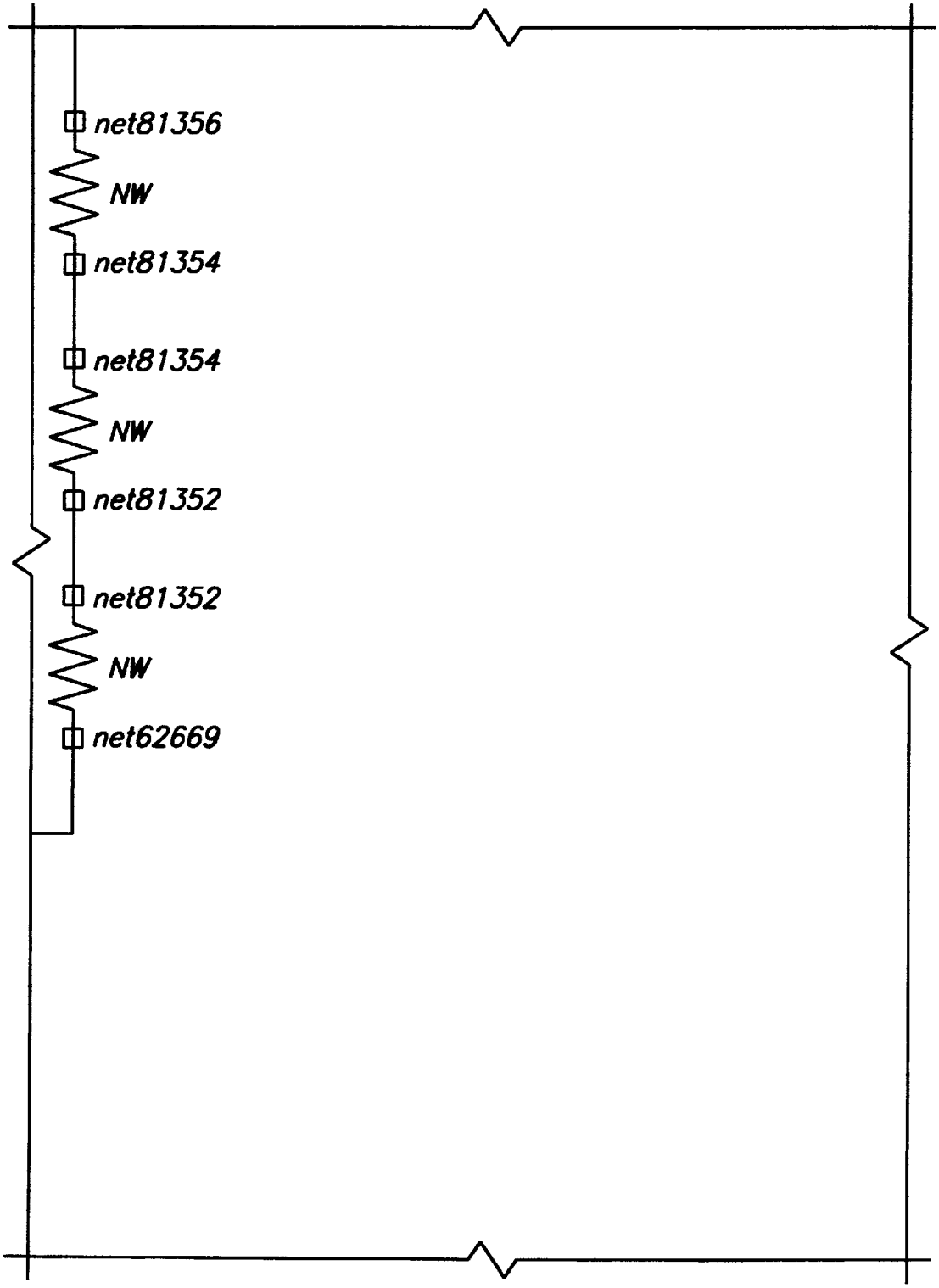
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Fig 9.0301CC

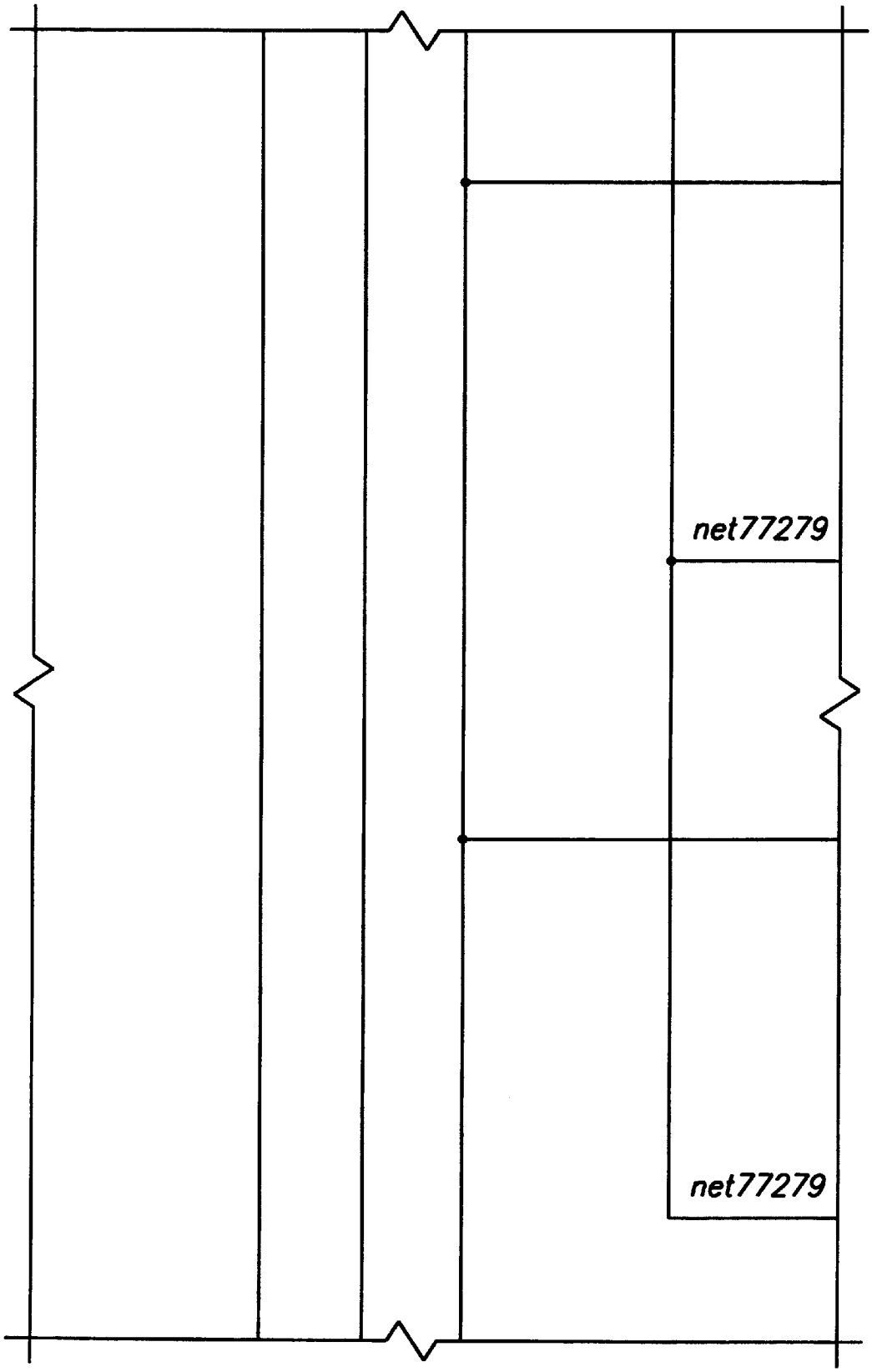
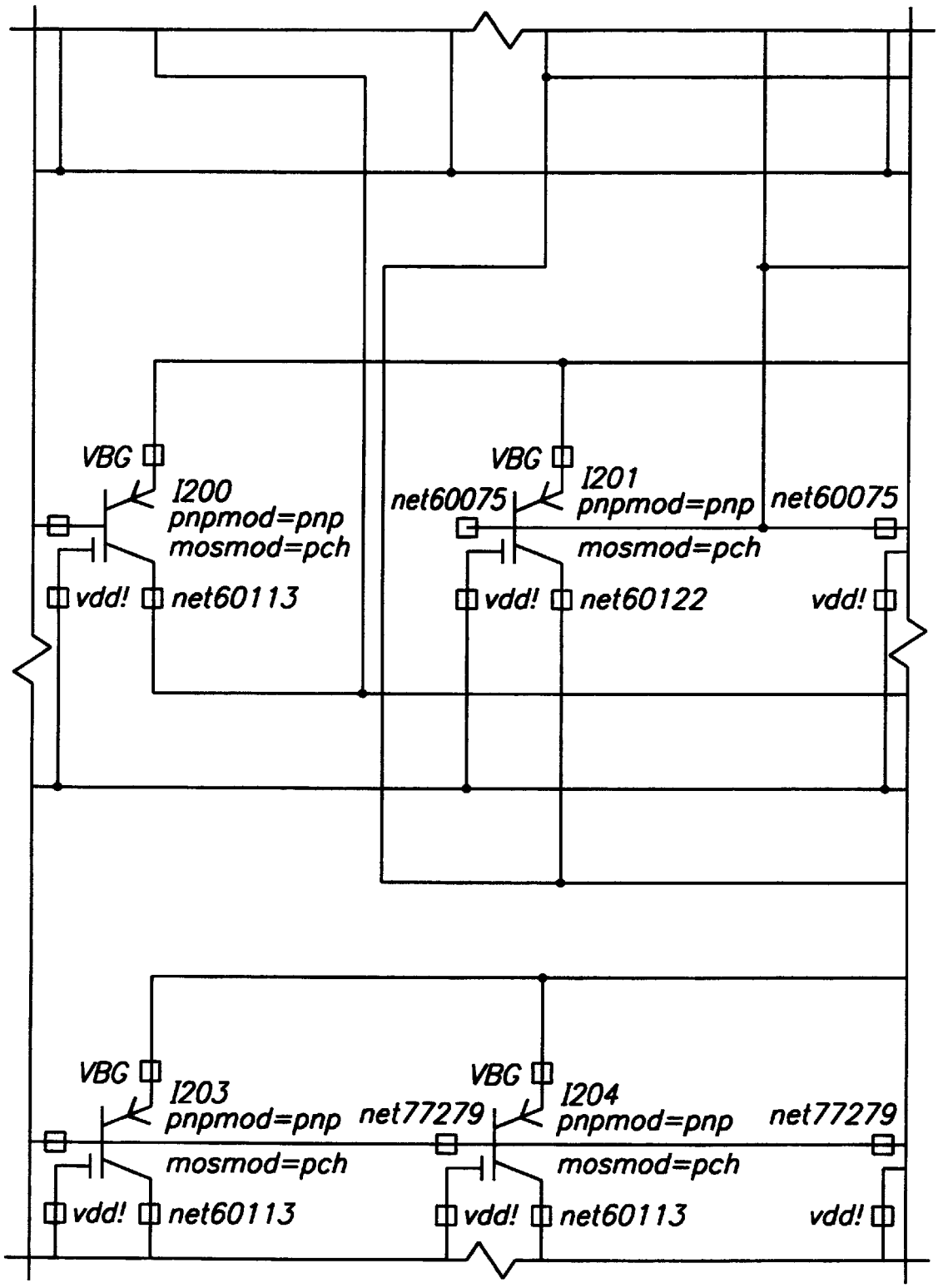


Fig 9.0301CD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mosmod=pch
vdd!
net60122
vdd!
VBG
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vdd!
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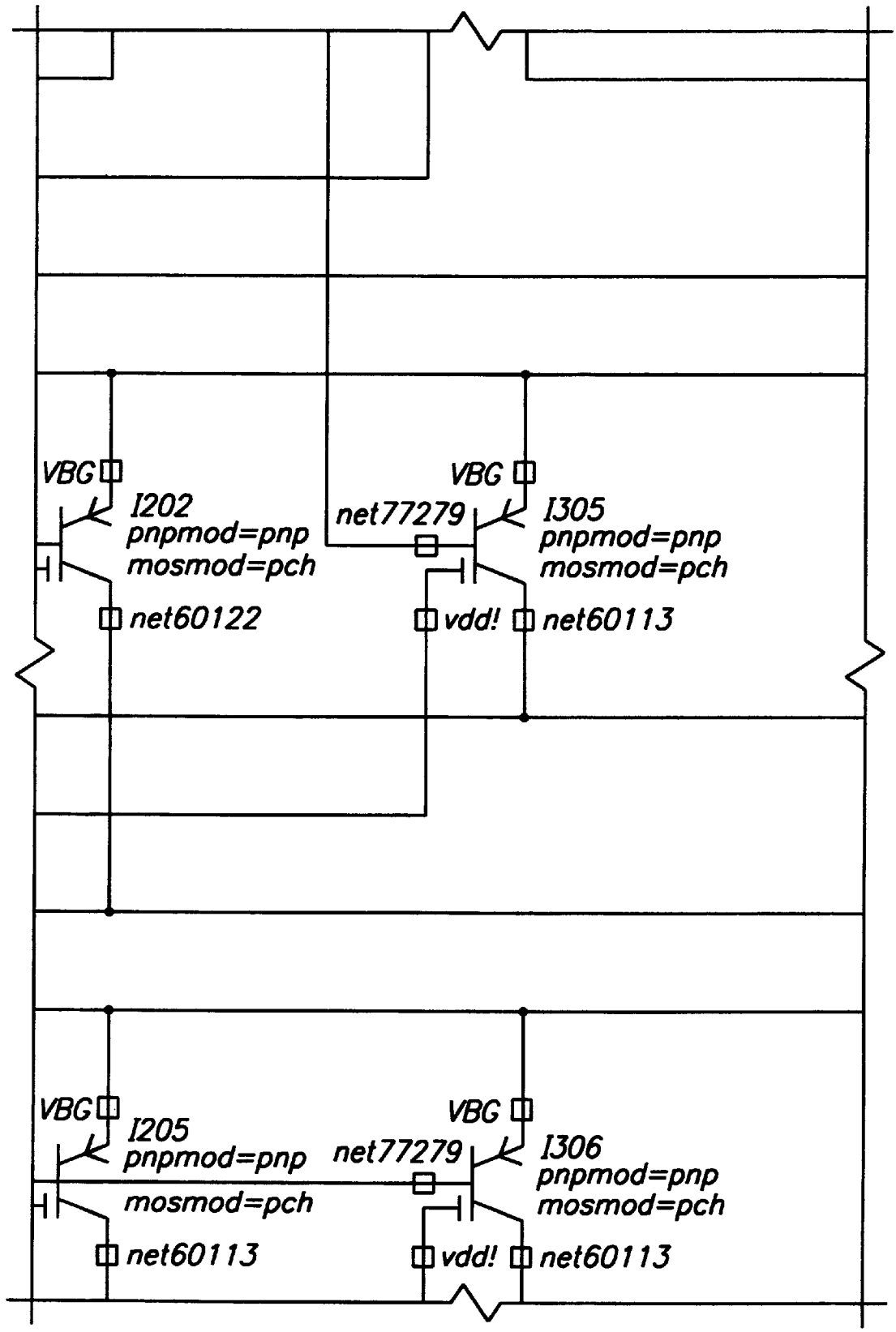
vdd!

Fig 9.0301CE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vdd!
net60113
VBG
I205
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net60113

Fig 9.0301CF

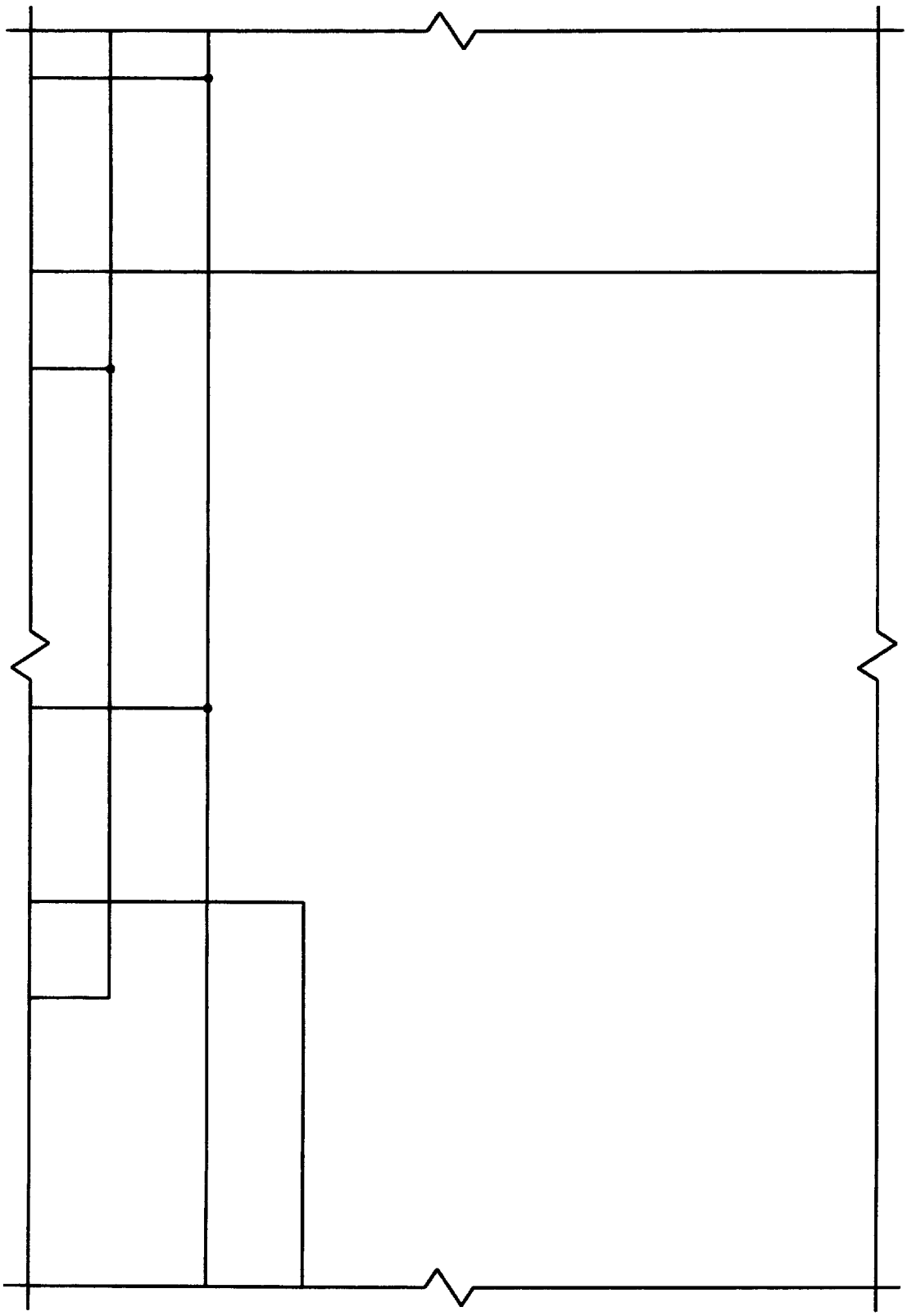

Fig 9.030116

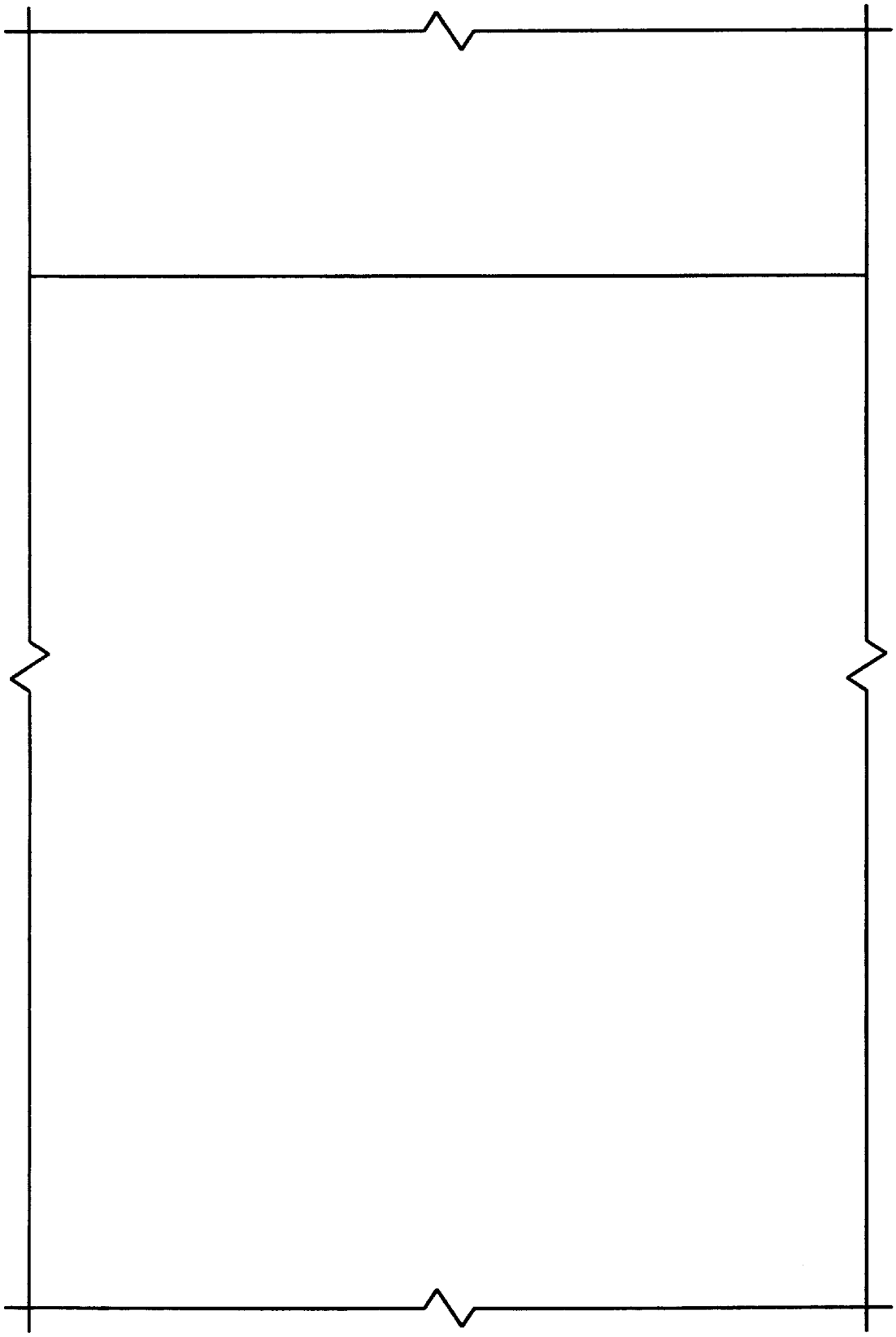

Fig 9.0301CH

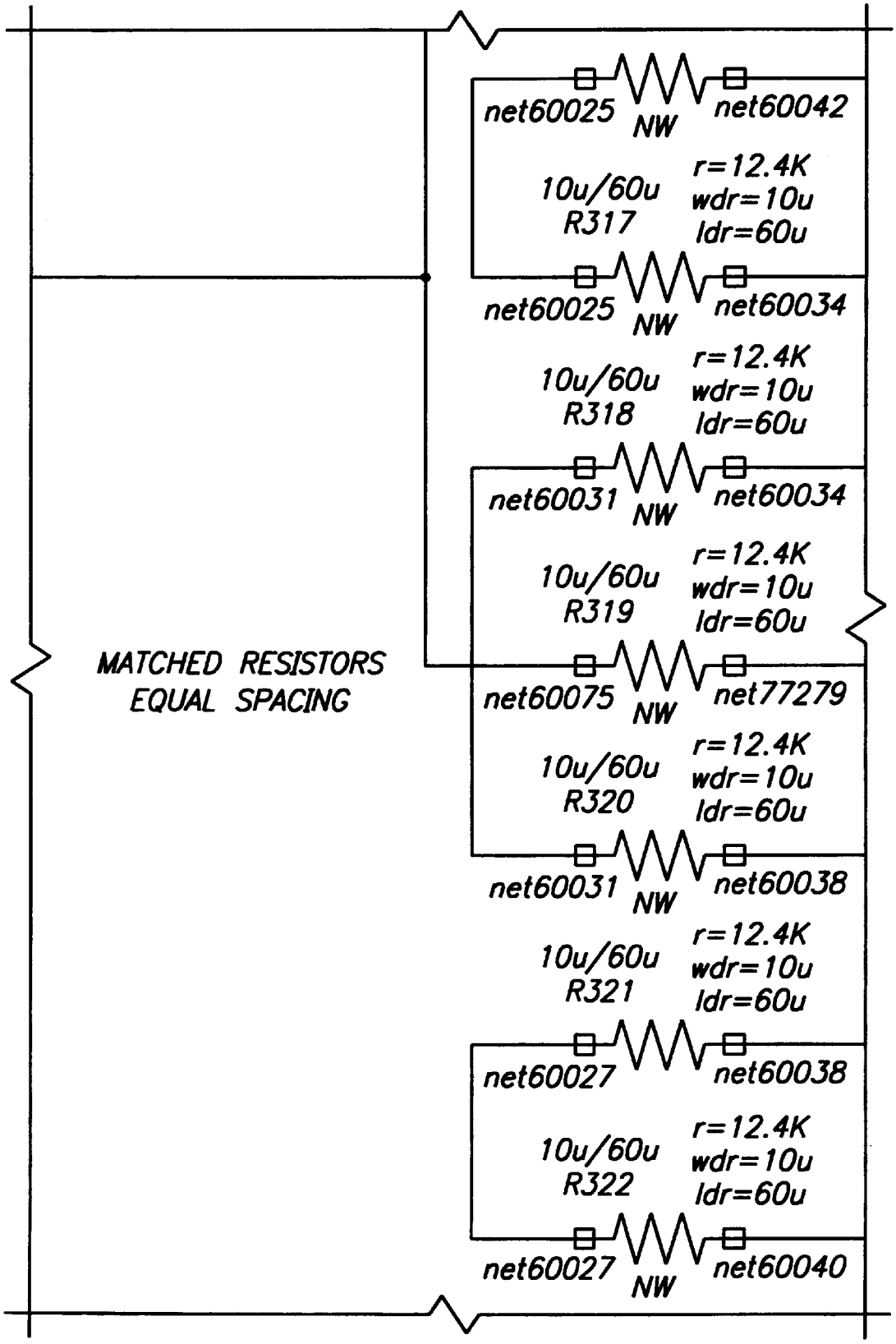
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Fig 9.0300IC

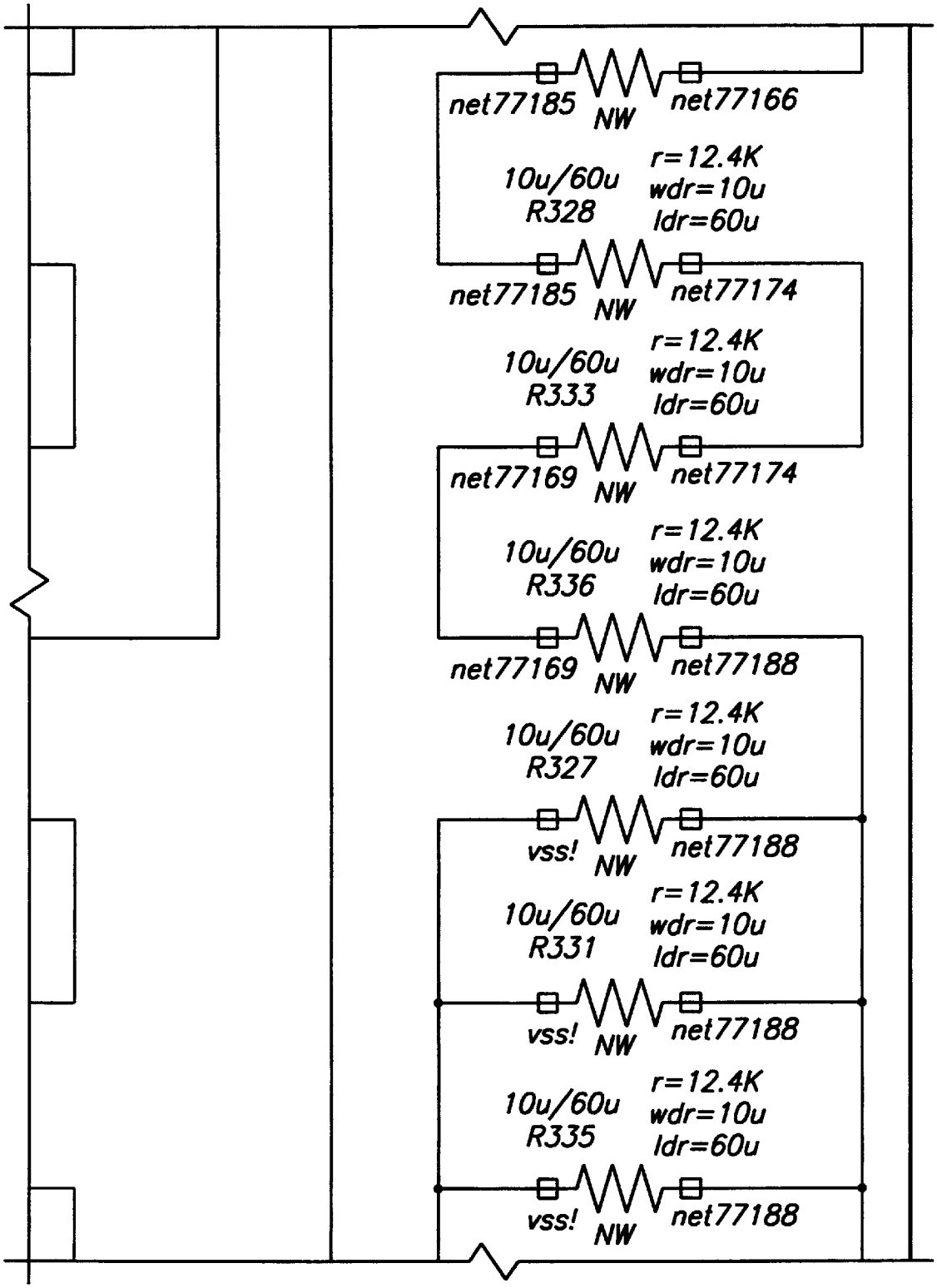


Fig 9.0300Cal

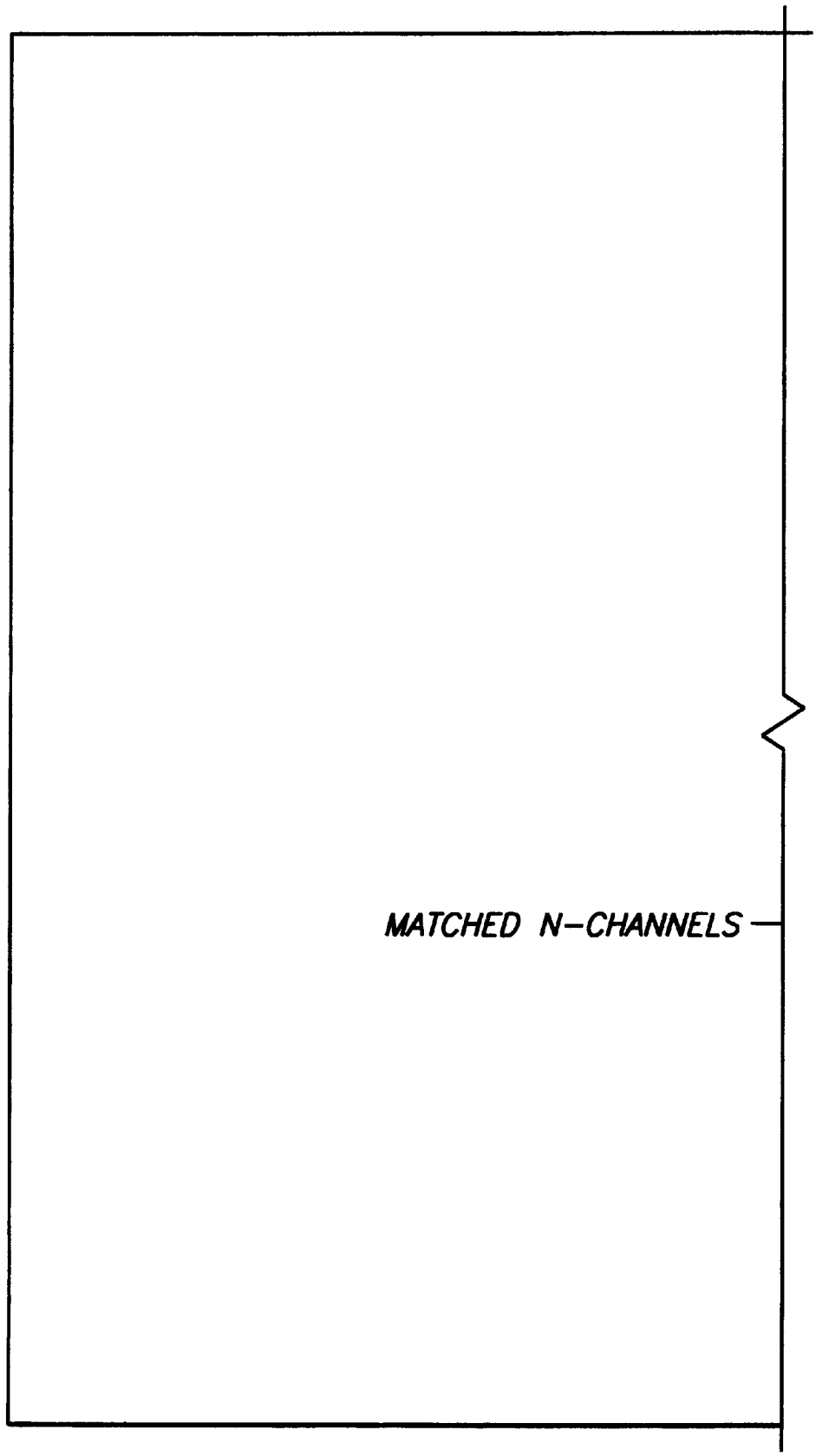


FIG 9.0301DA

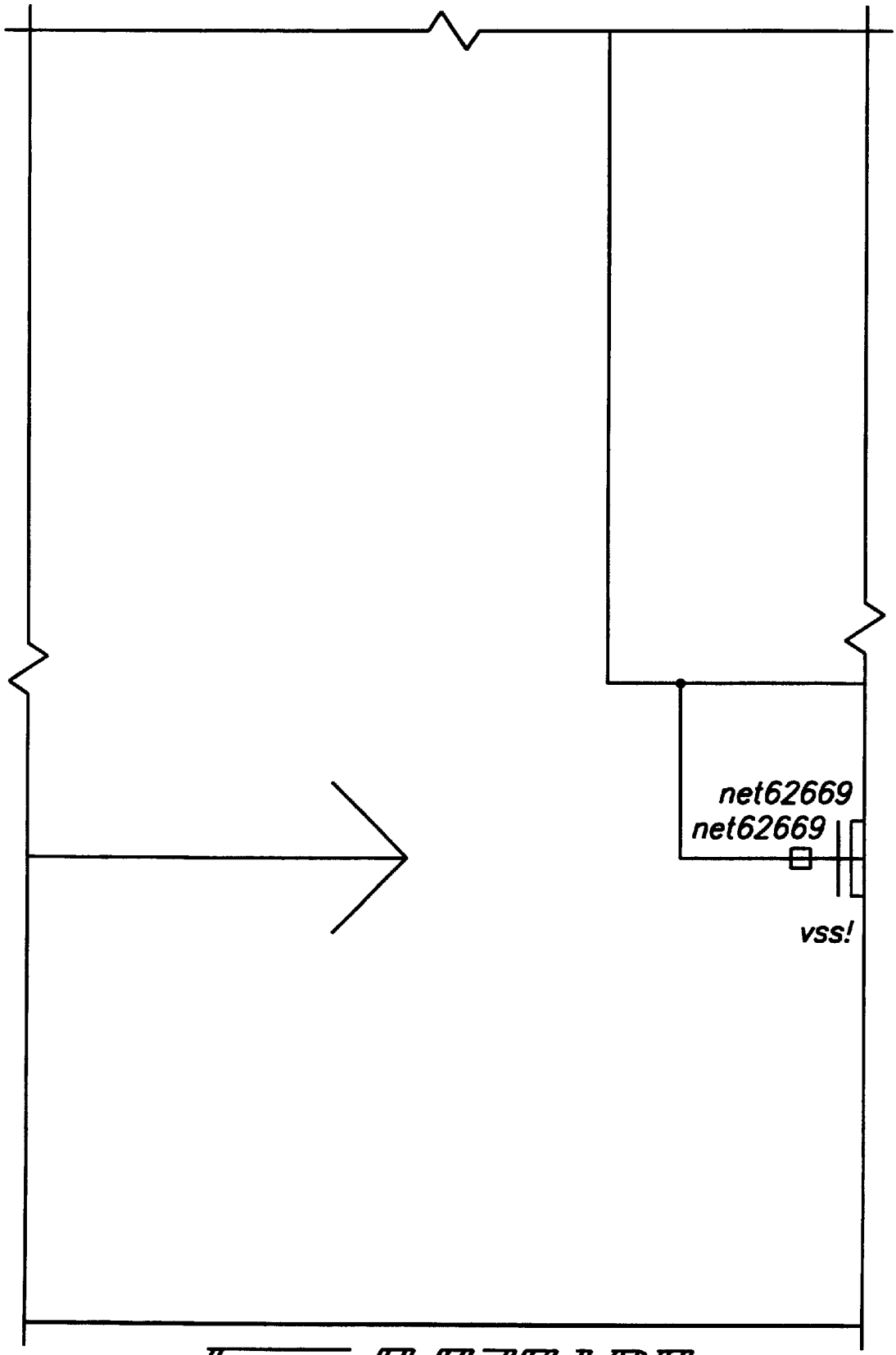
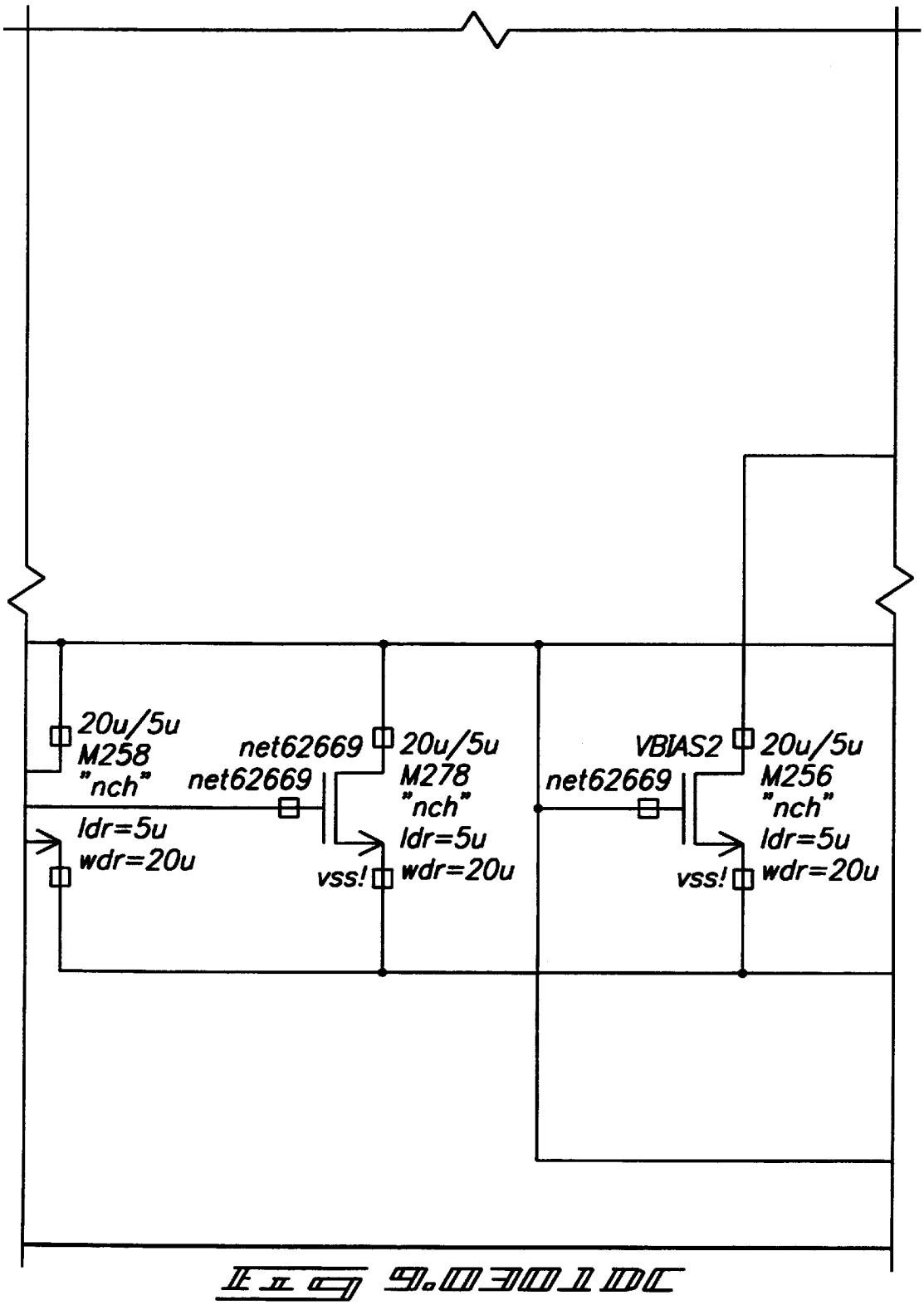


Fig 9.030108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wdr=20u
vss!

Fig 9.0301DC

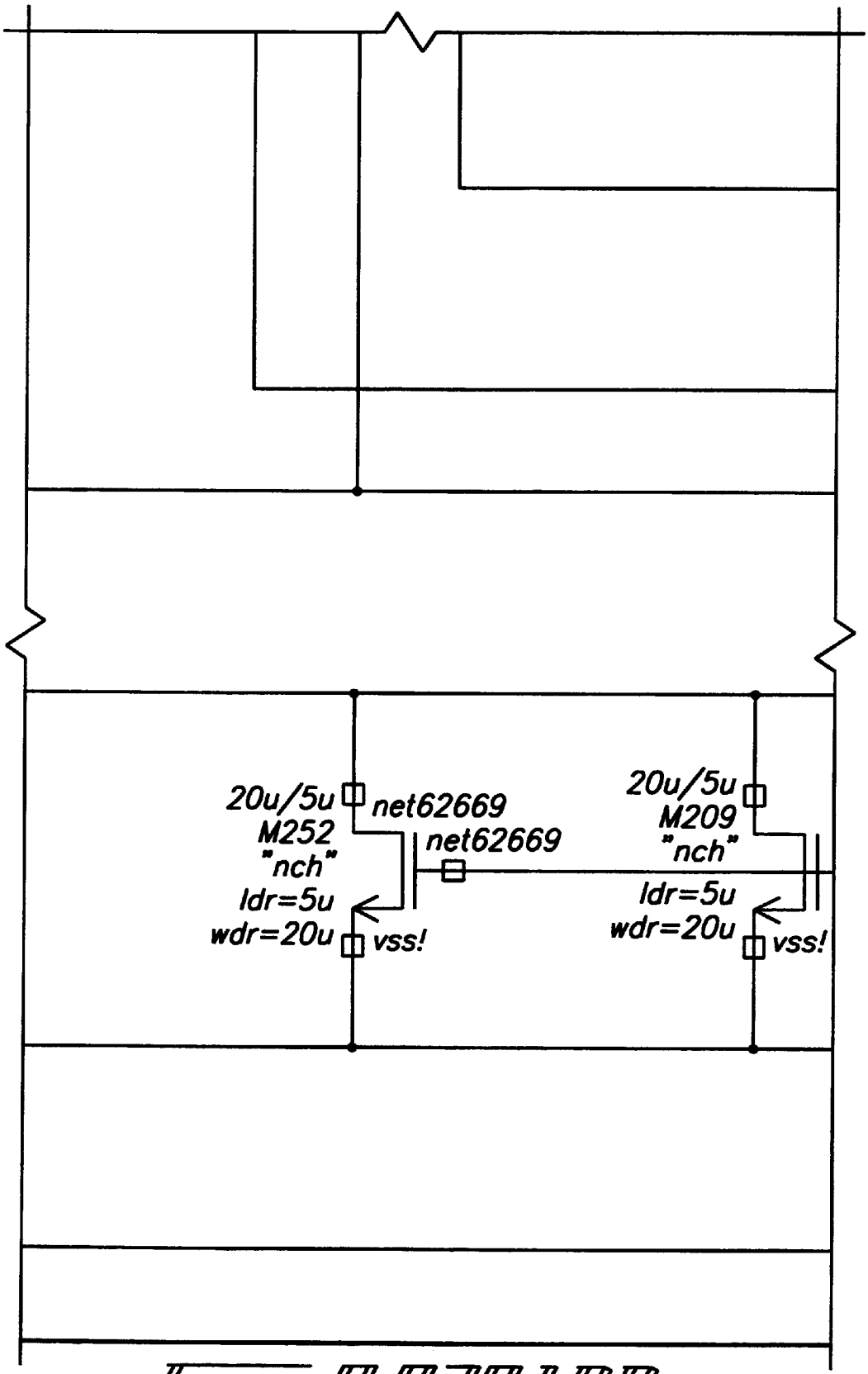
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Fig 9,030,100

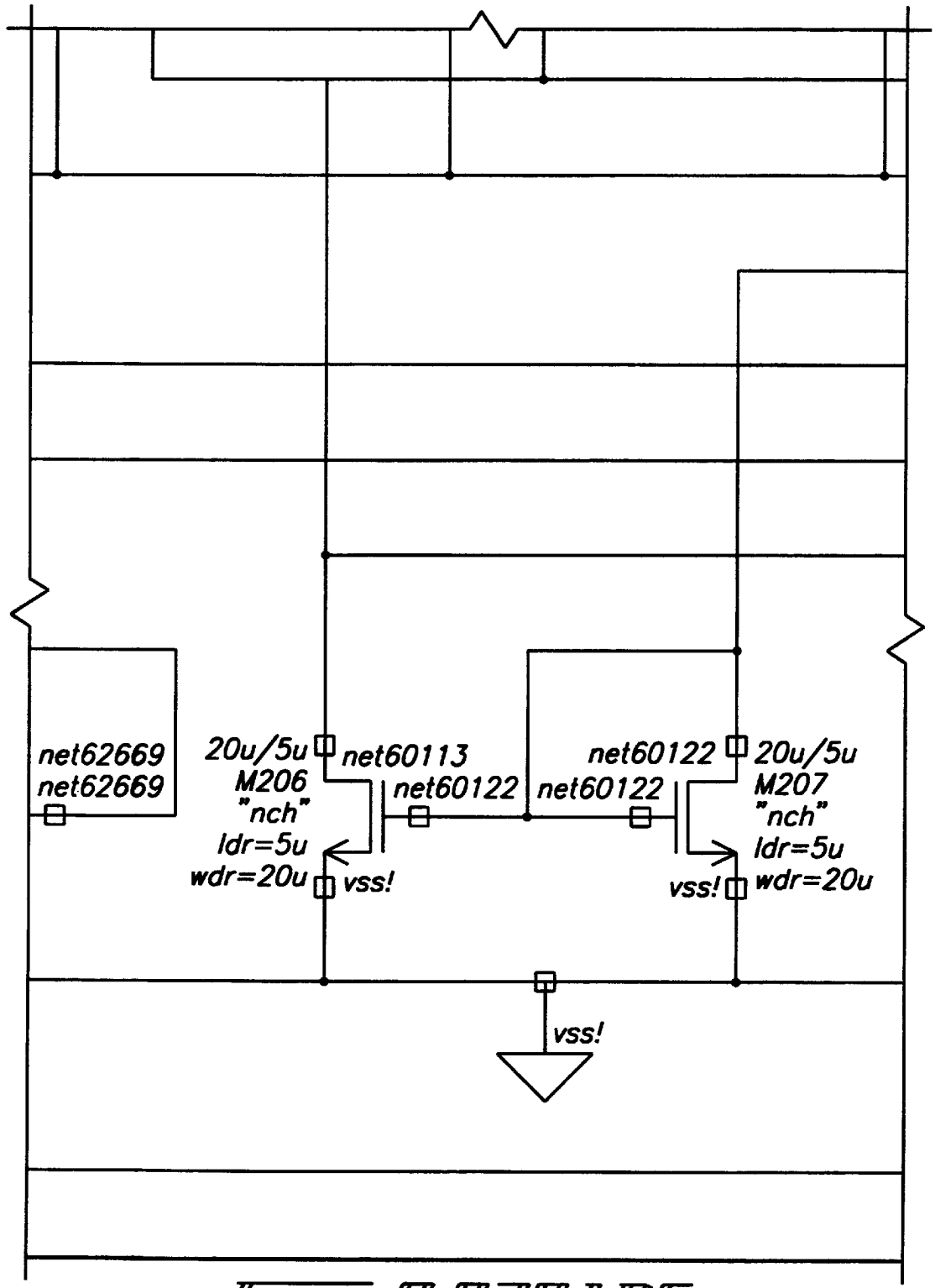
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Fig 9.0301DE

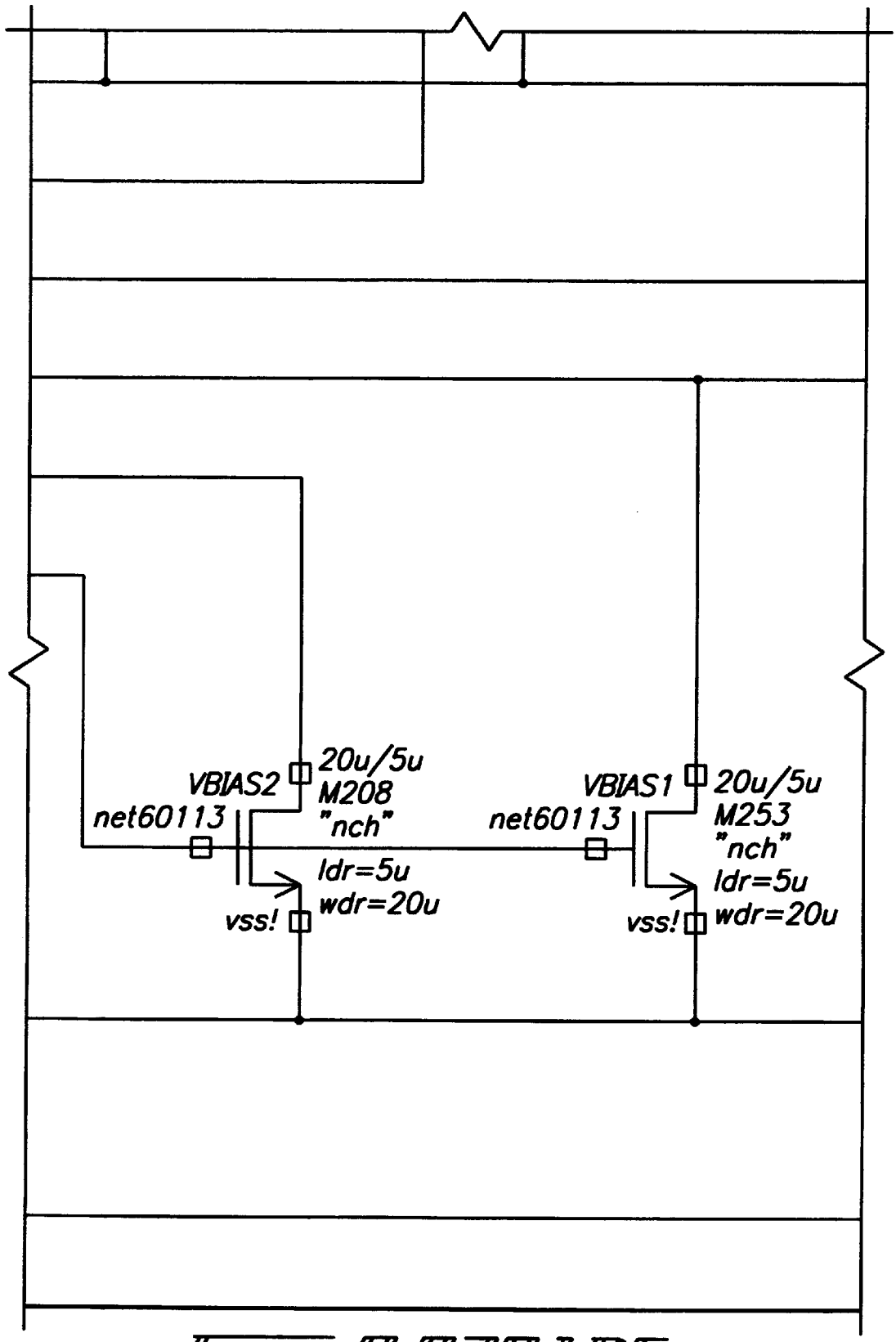
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Fig 9.0301DF

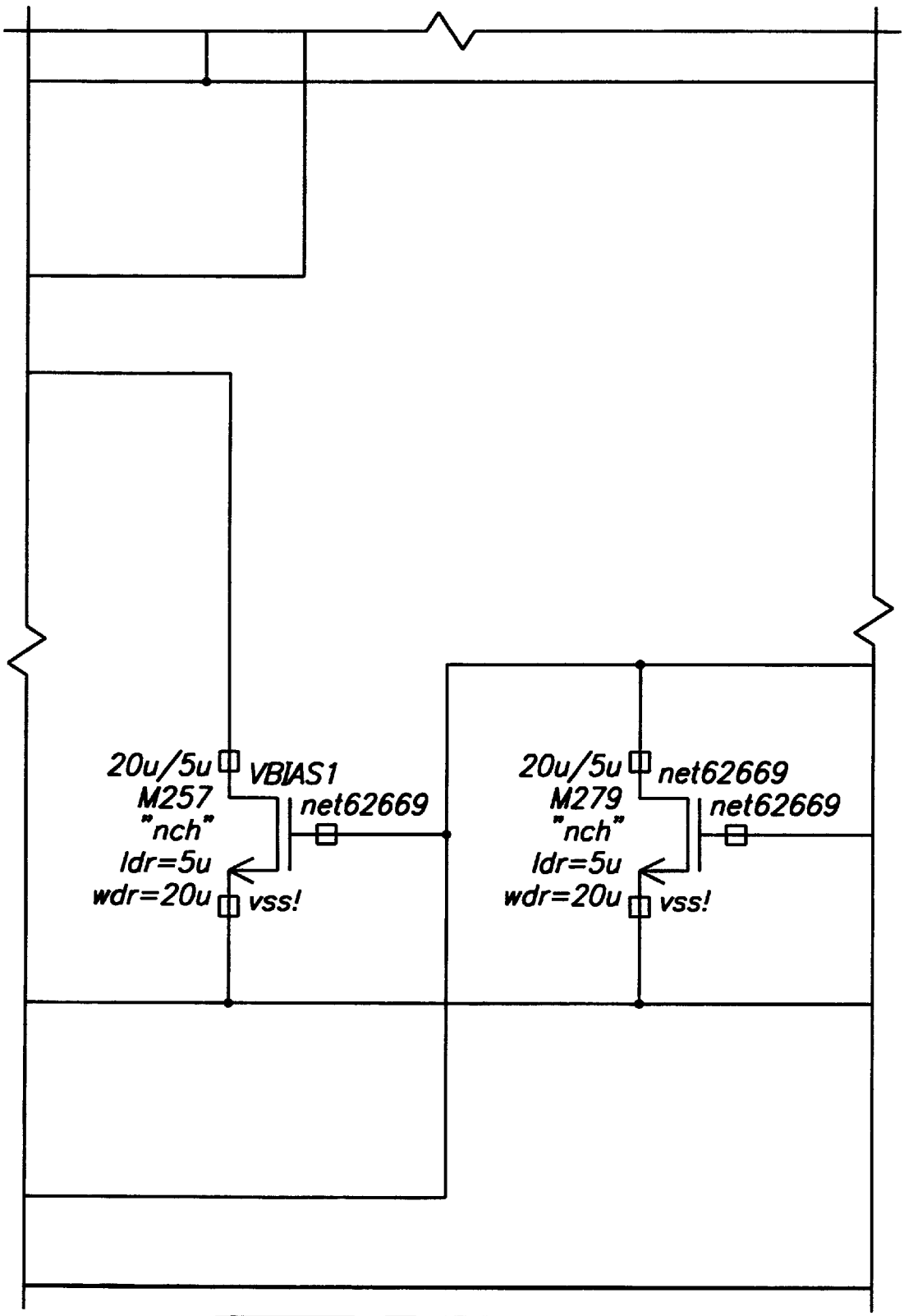
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Fig 9,030,106

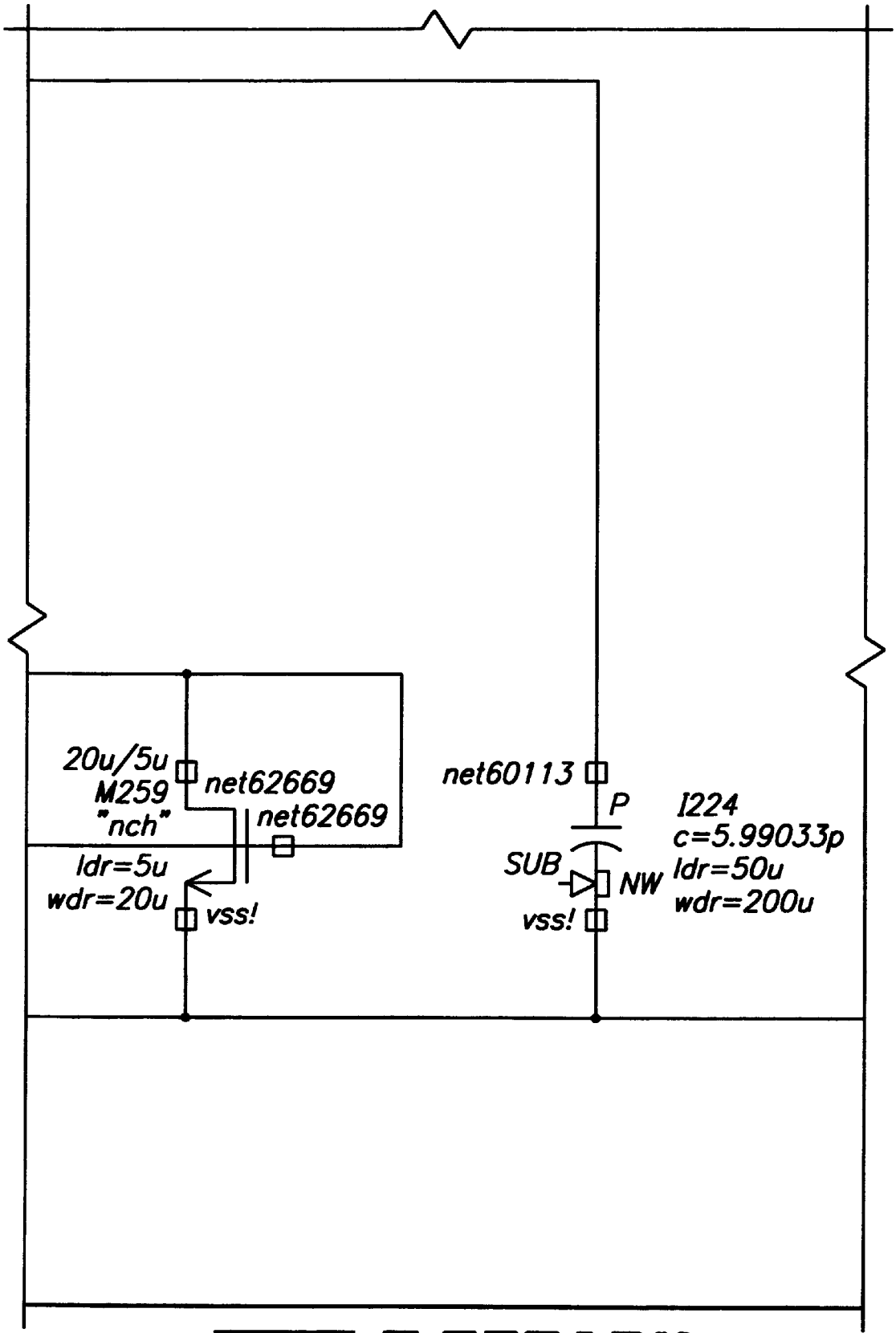


Fig 9.0301.10H

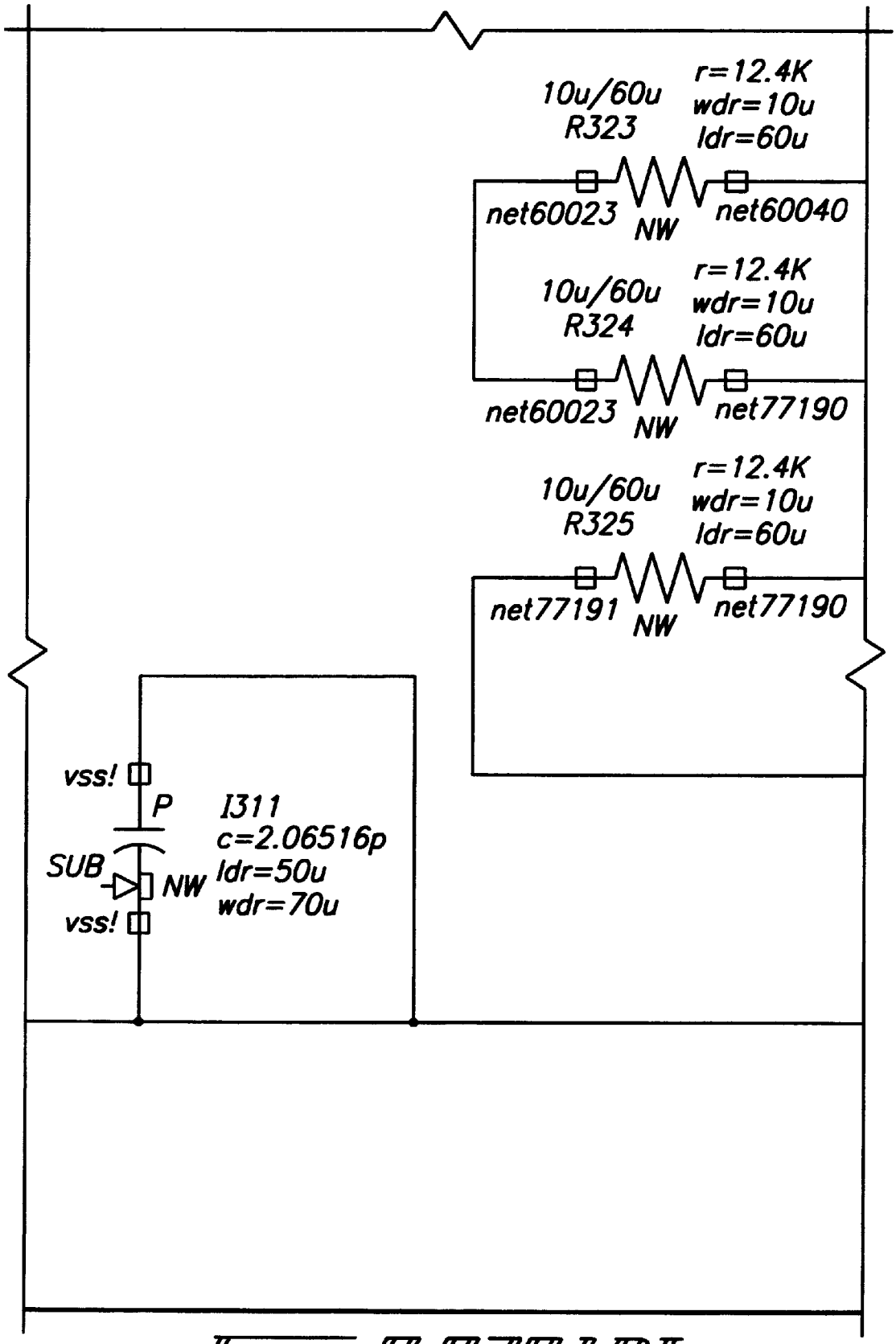
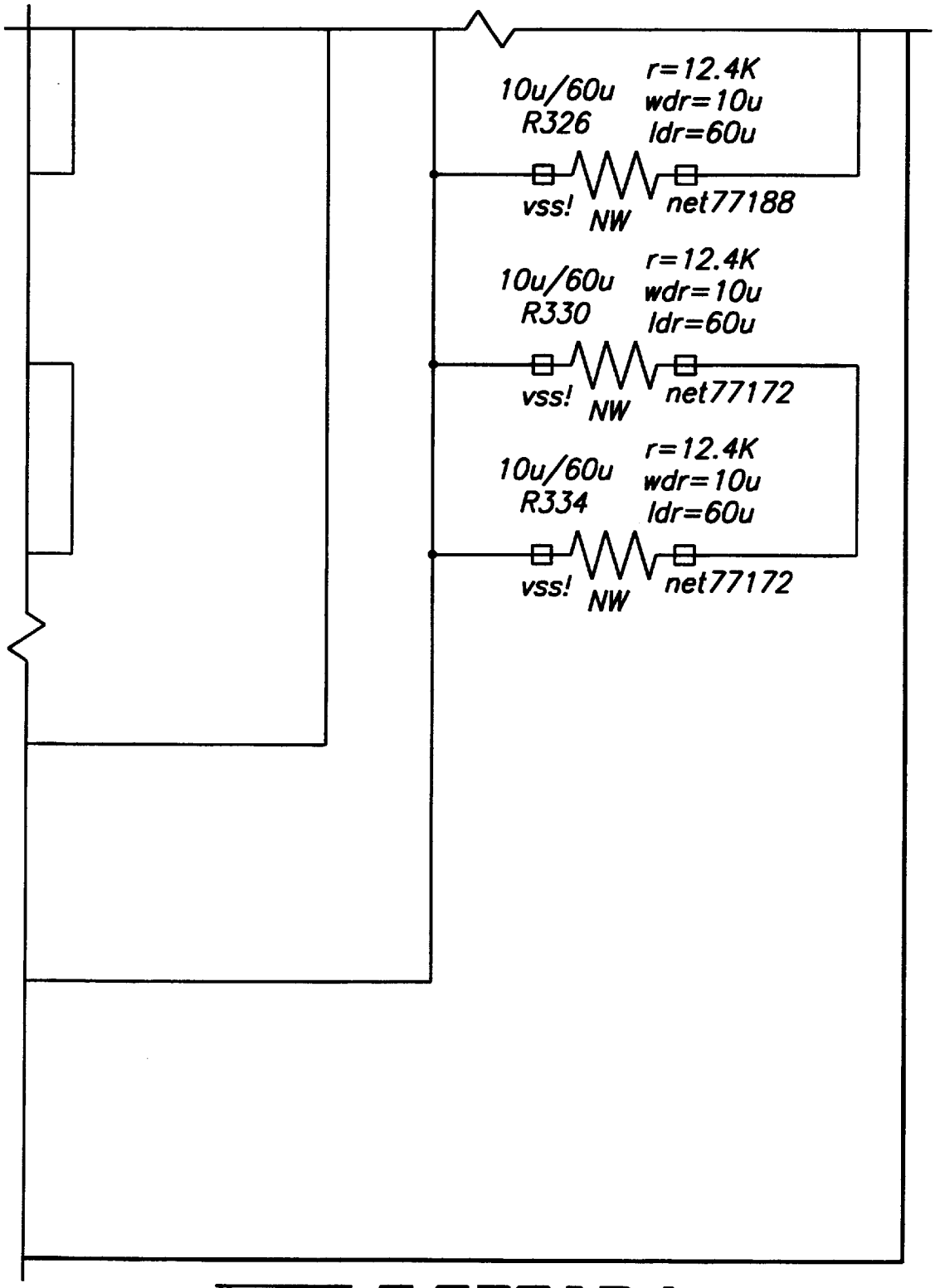


Fig 9.0300100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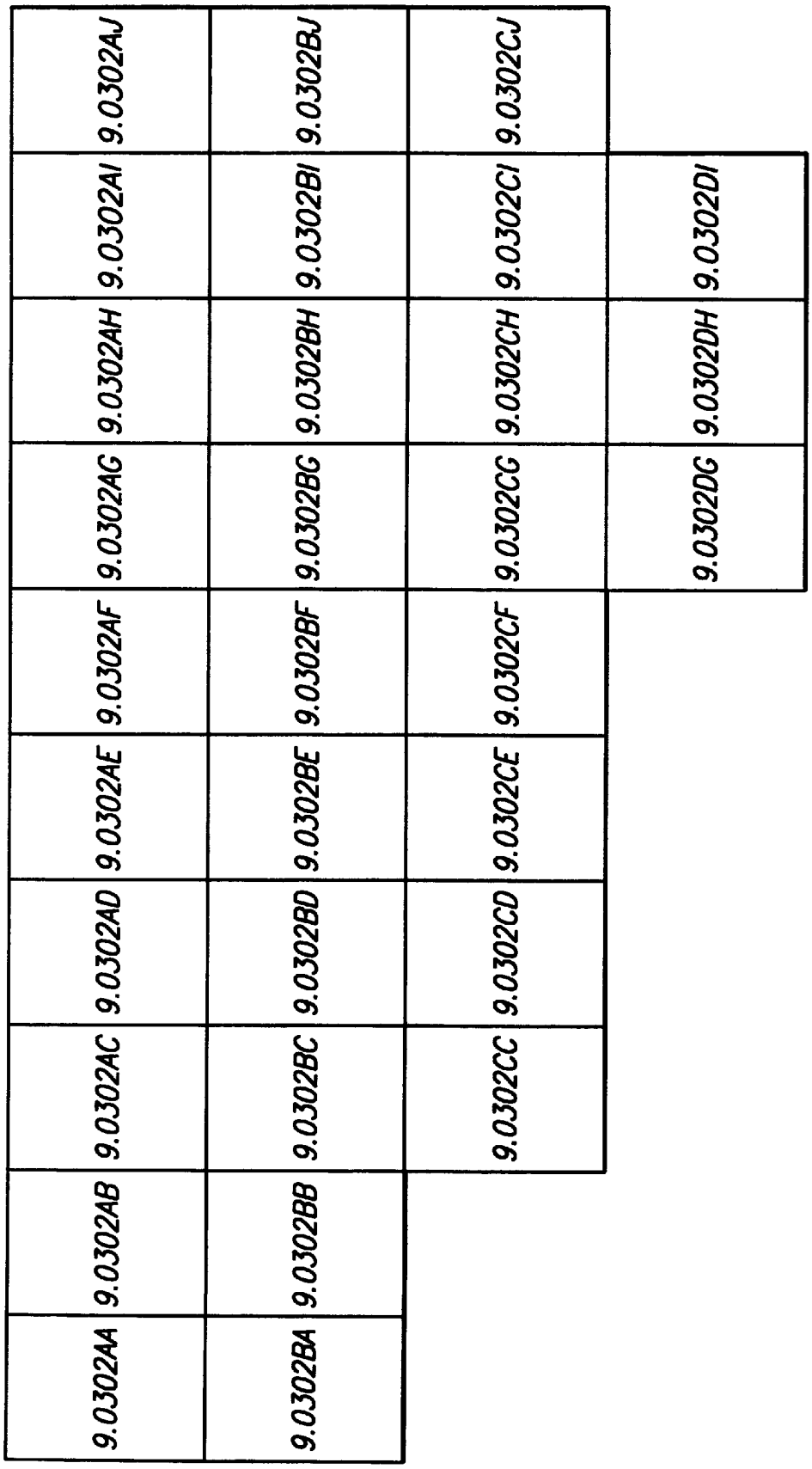
net77172

Fig 9.0301Dd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9.0302BD
9.0302BE
9.0302BF
9.0302BG
9.0302BH
9.0302BI
9.0302BJ
9.0302CC
9.0302CD
9.0302CE
9.0302CF
9.0302CG
9.0302CH
9.0302CI
9.0302CJ
9.0302DG
9.0302DH
9.0302DI

FIG 9.0302E

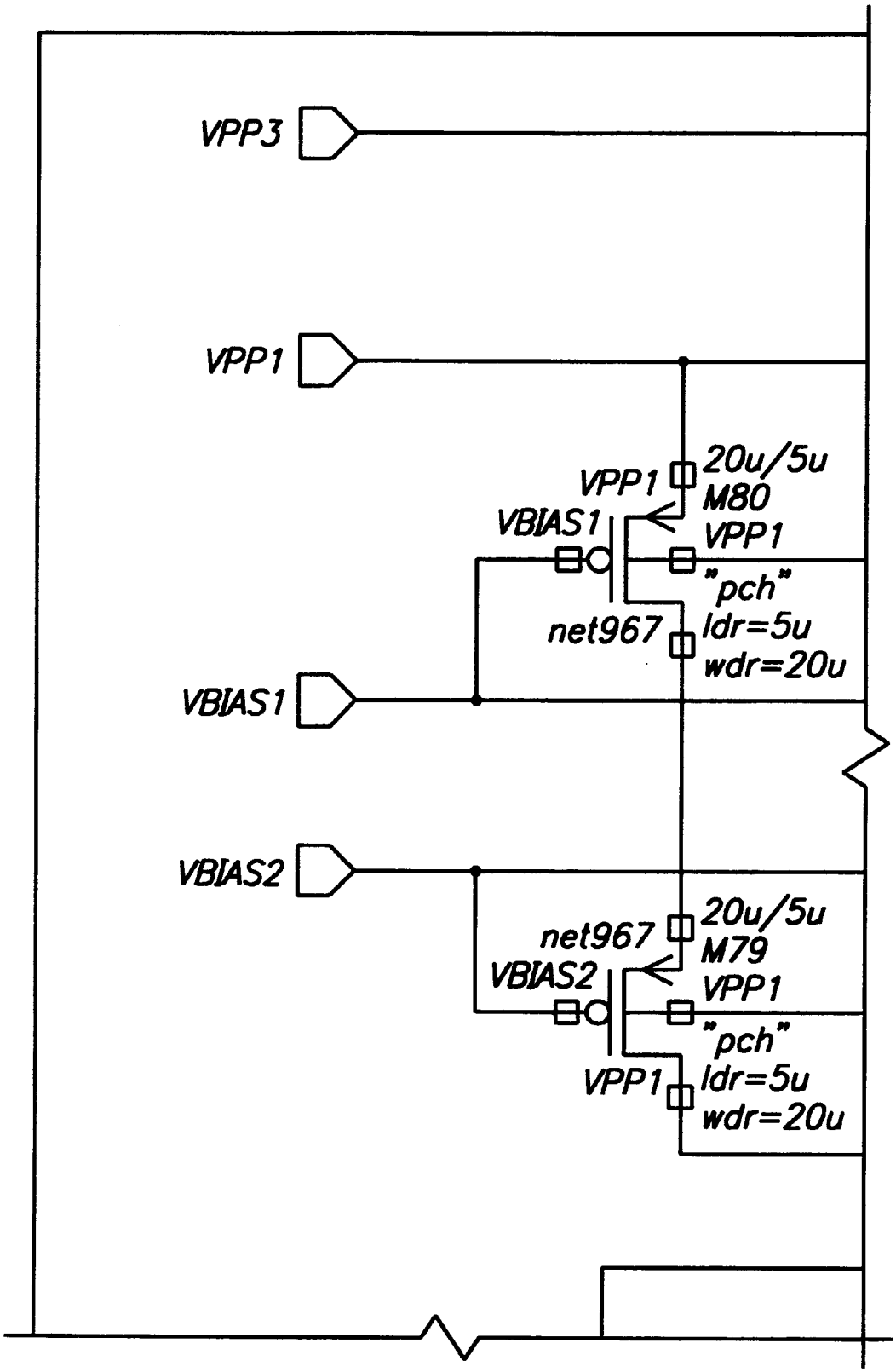

VPP3
VPP1
VPP1
VBIAS1
net967
20u/5u
M80
VPP1
"pch"
ldr=5u
wdr=20u
VBIAS1
VBIAS2
net967
VBIAS2
VPP1
20u/5u
M79
VPP1
"pch"
ldr=5u
wdr=20u

Fig 9.0302AA

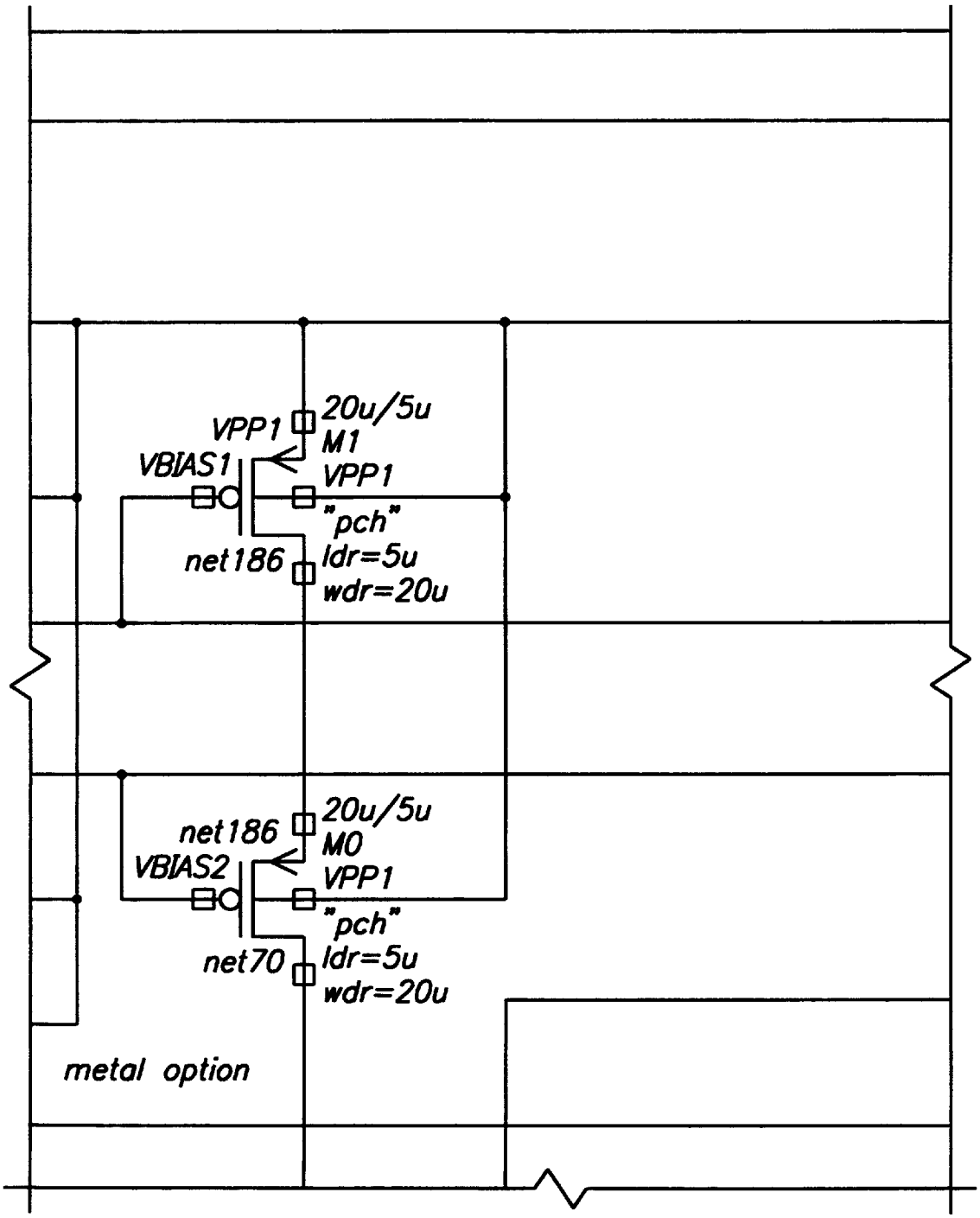

VPP1
20u/5u
M1
VBIAS1
VPP1
"pch"
net186
ldr=5u
wdr=20u
net186
20u/5u
M0
VBIAS2
VPP1
"pch"
net70
ldr=5u
wdr=20u
metal option

Fig 9.0302AB

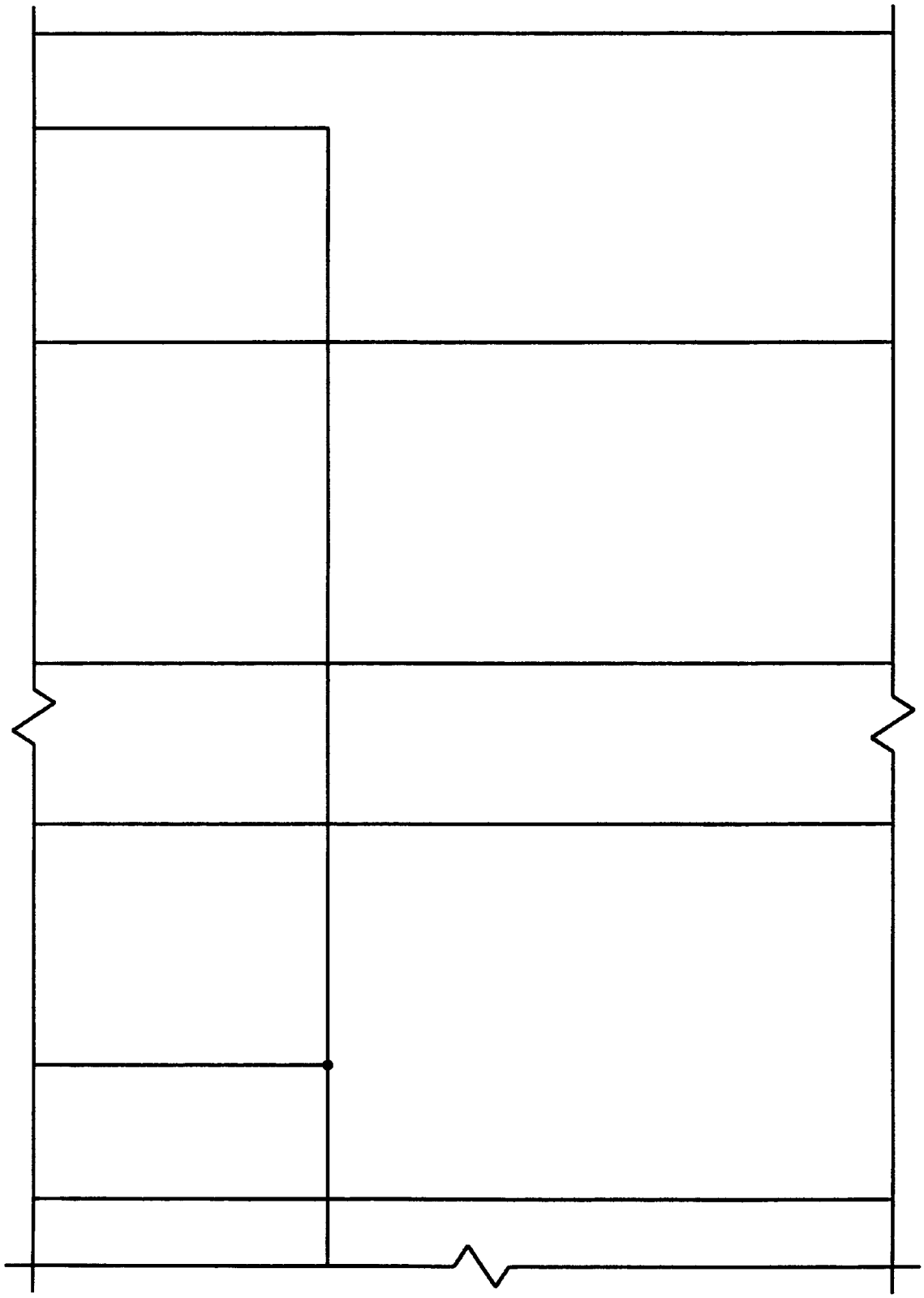


Fig 9.0302AC

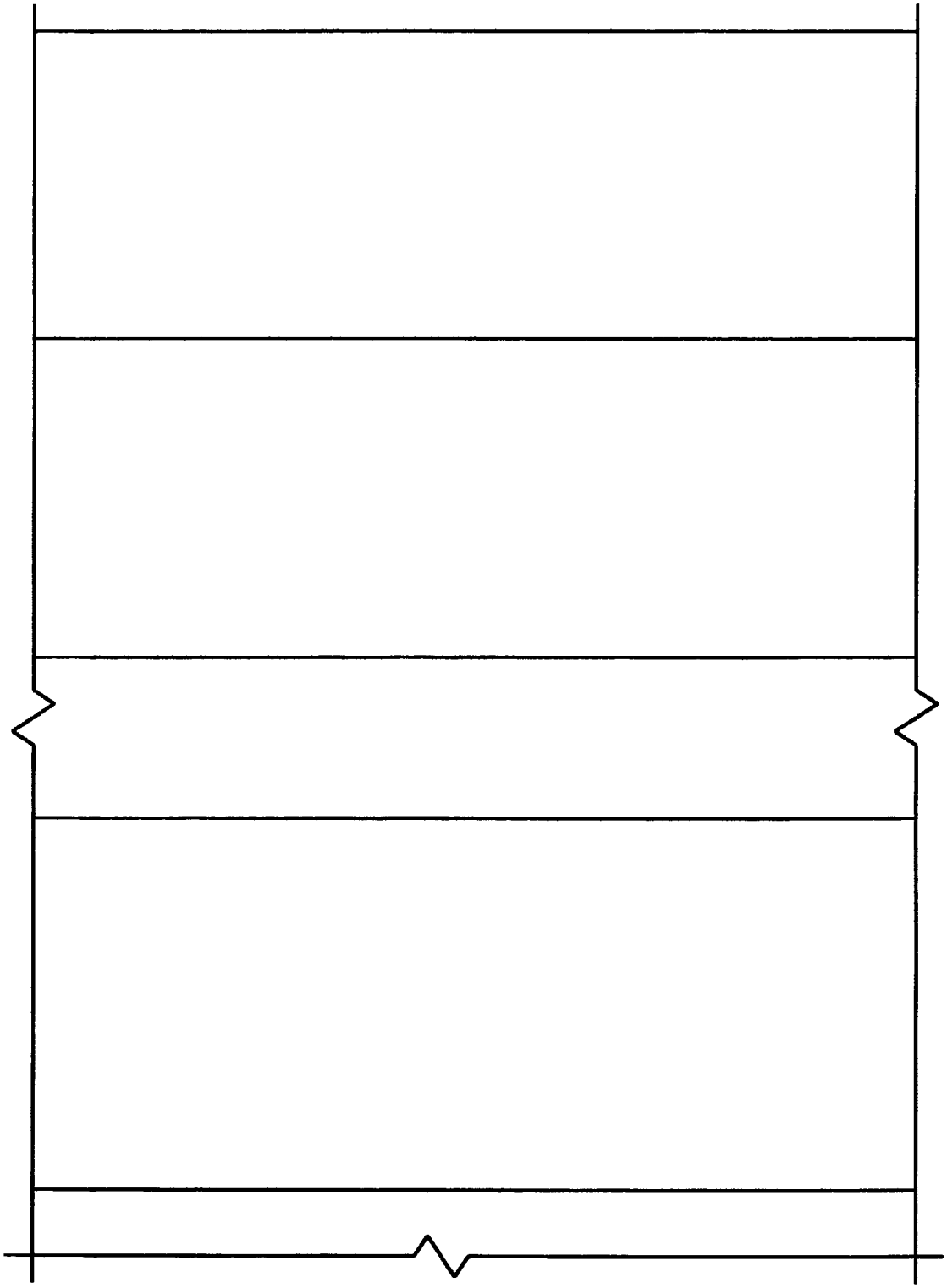


Fig 9.0302AD

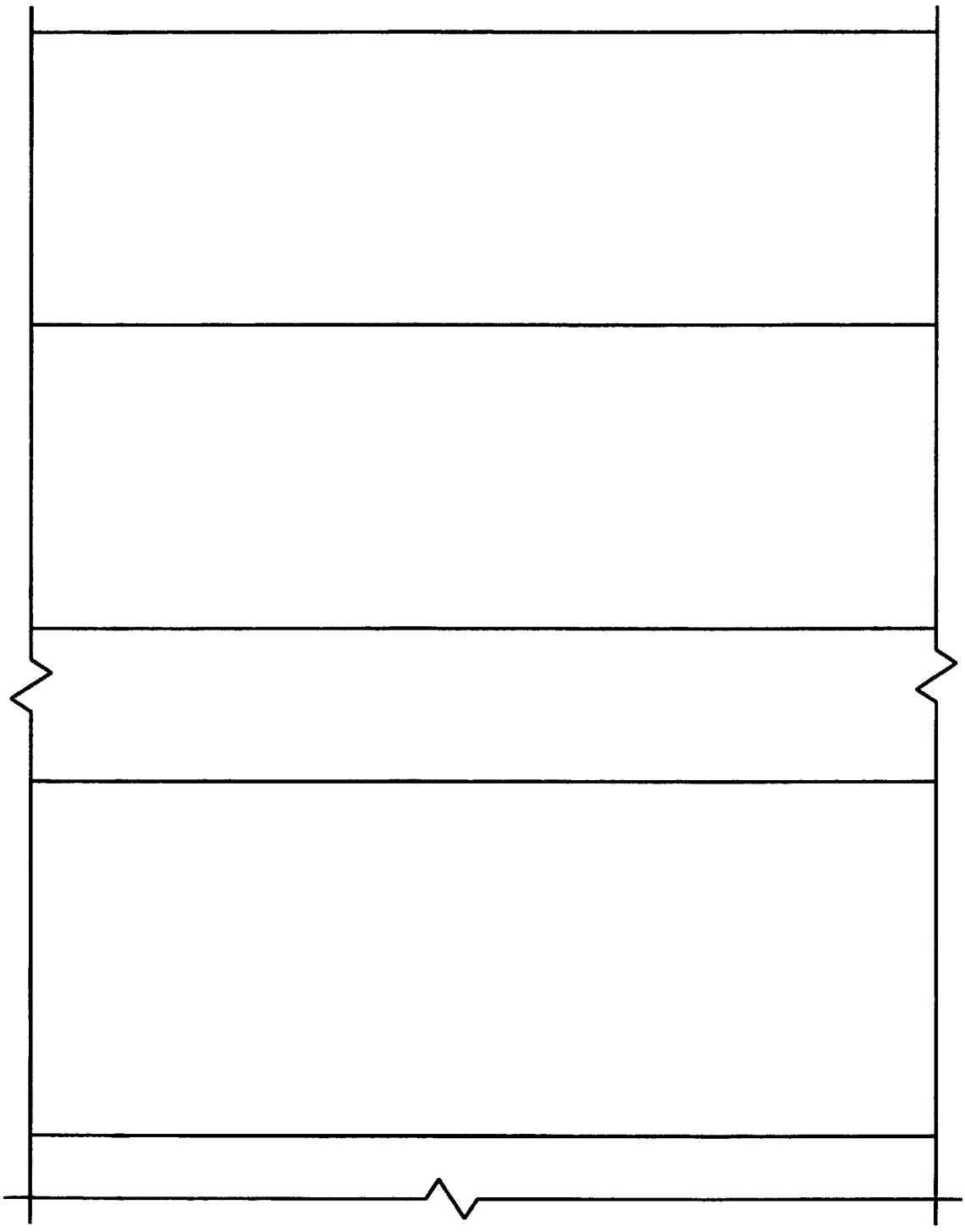


Fig 9.0302AE

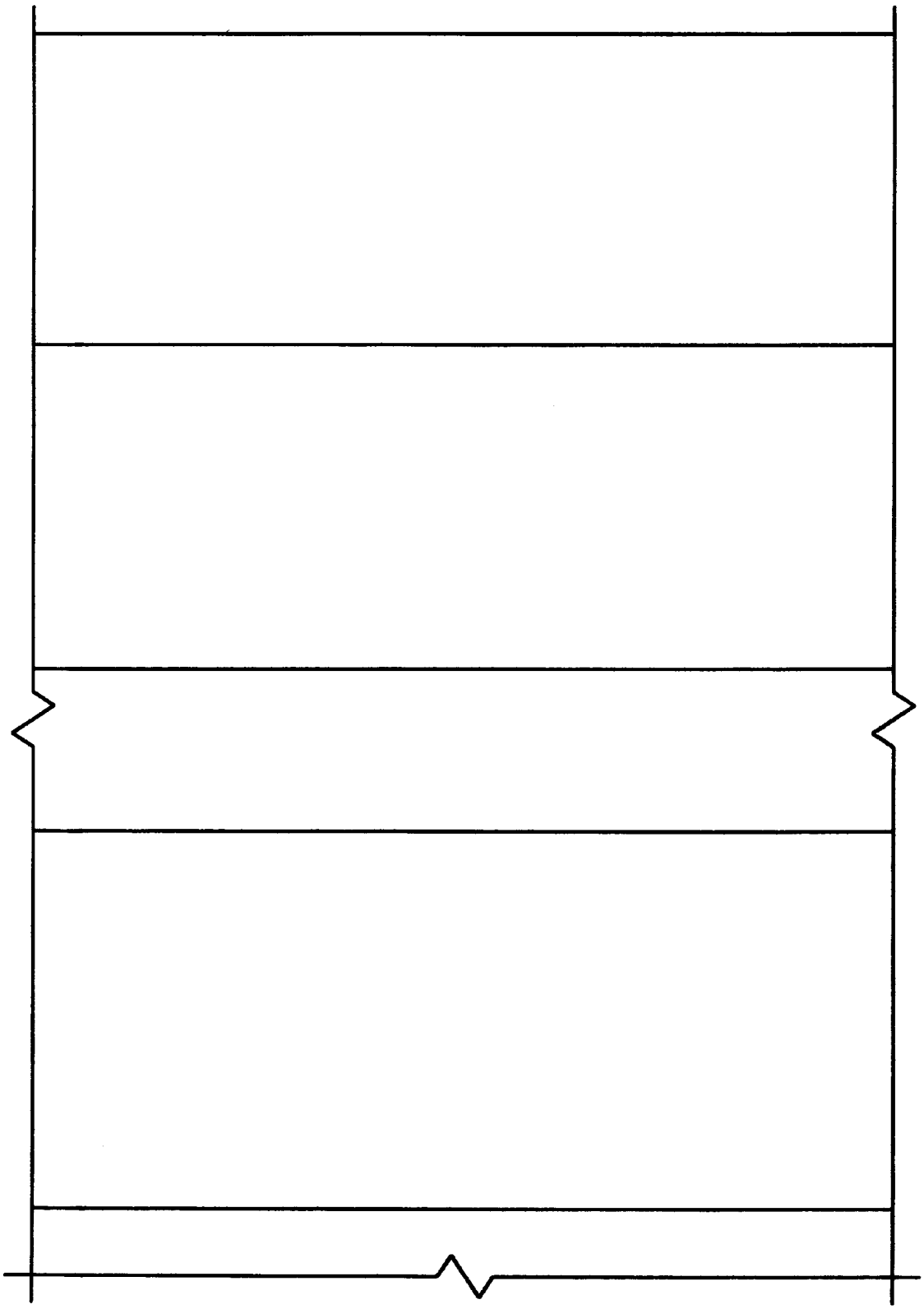


Fig 9.0302AF

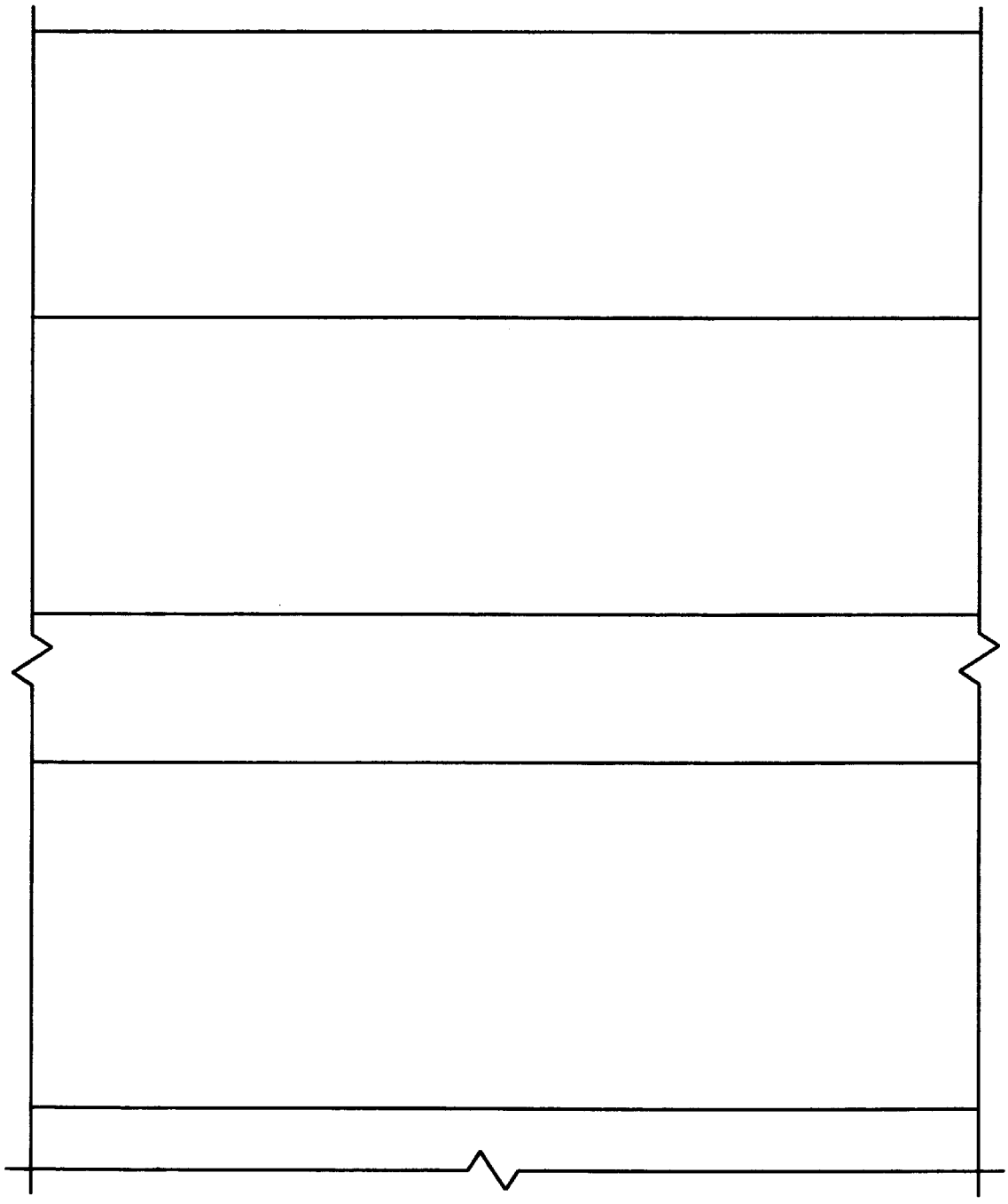


Fig 9.030246

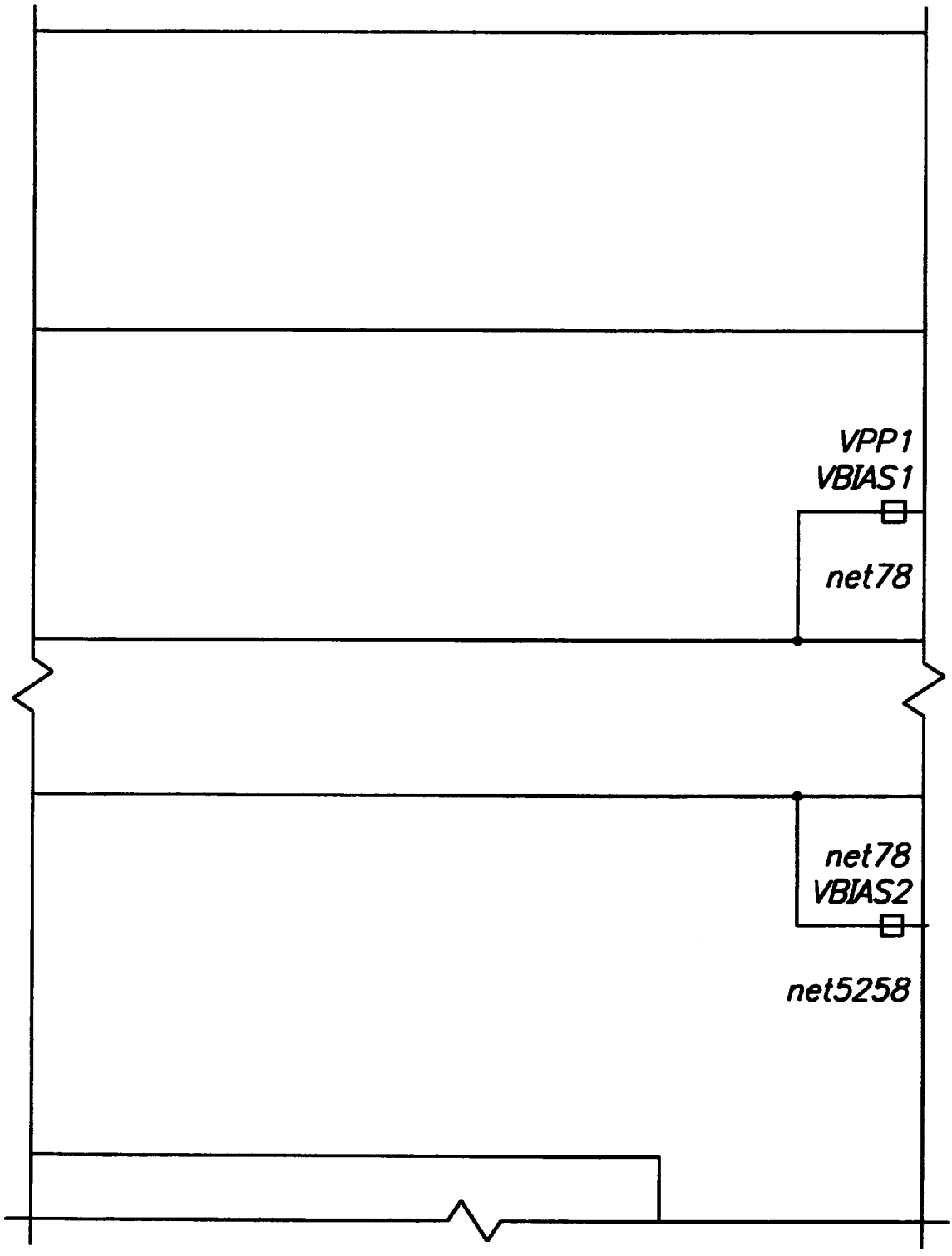


FIG 9.0302AH

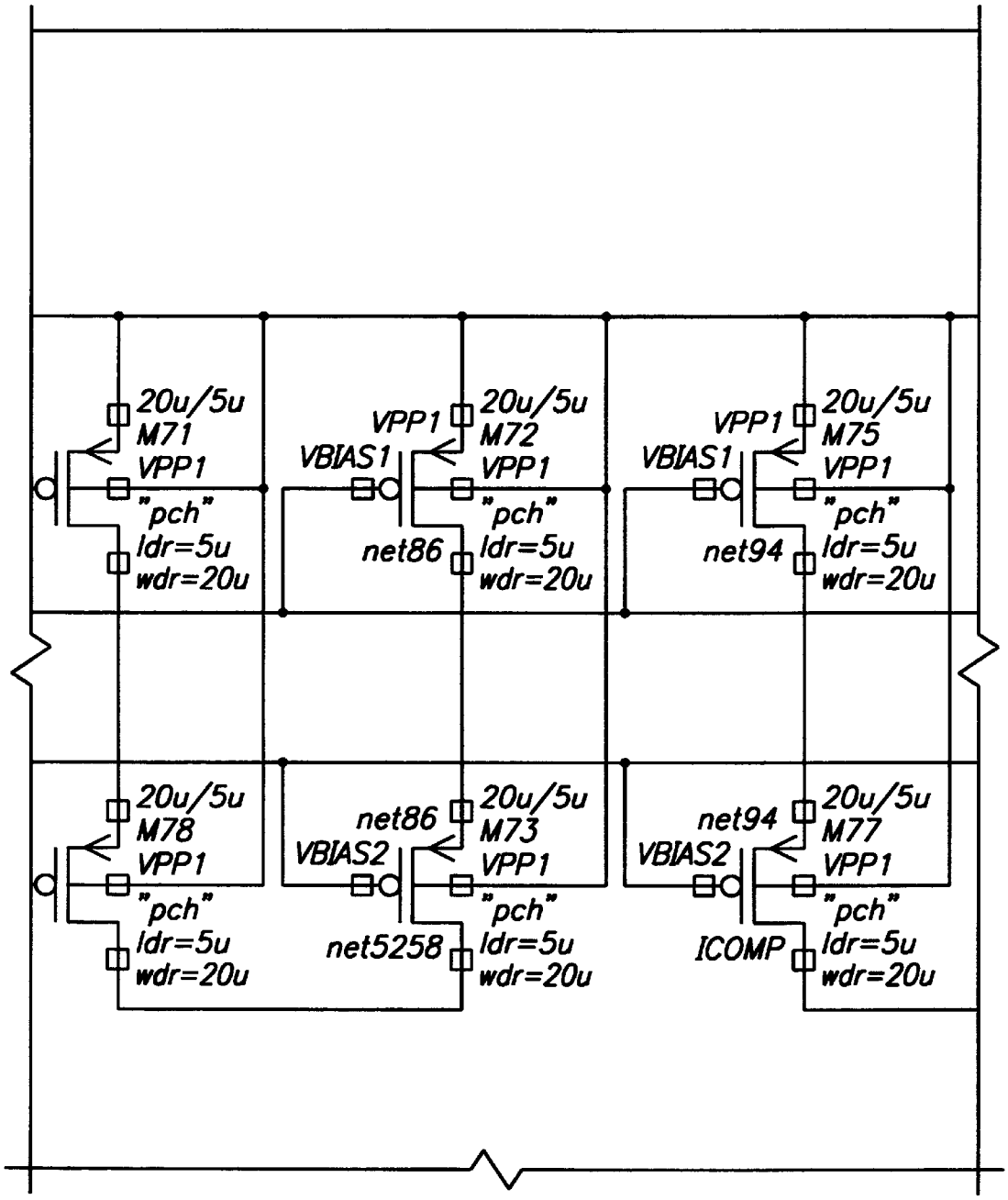


Fig 9.0302AII

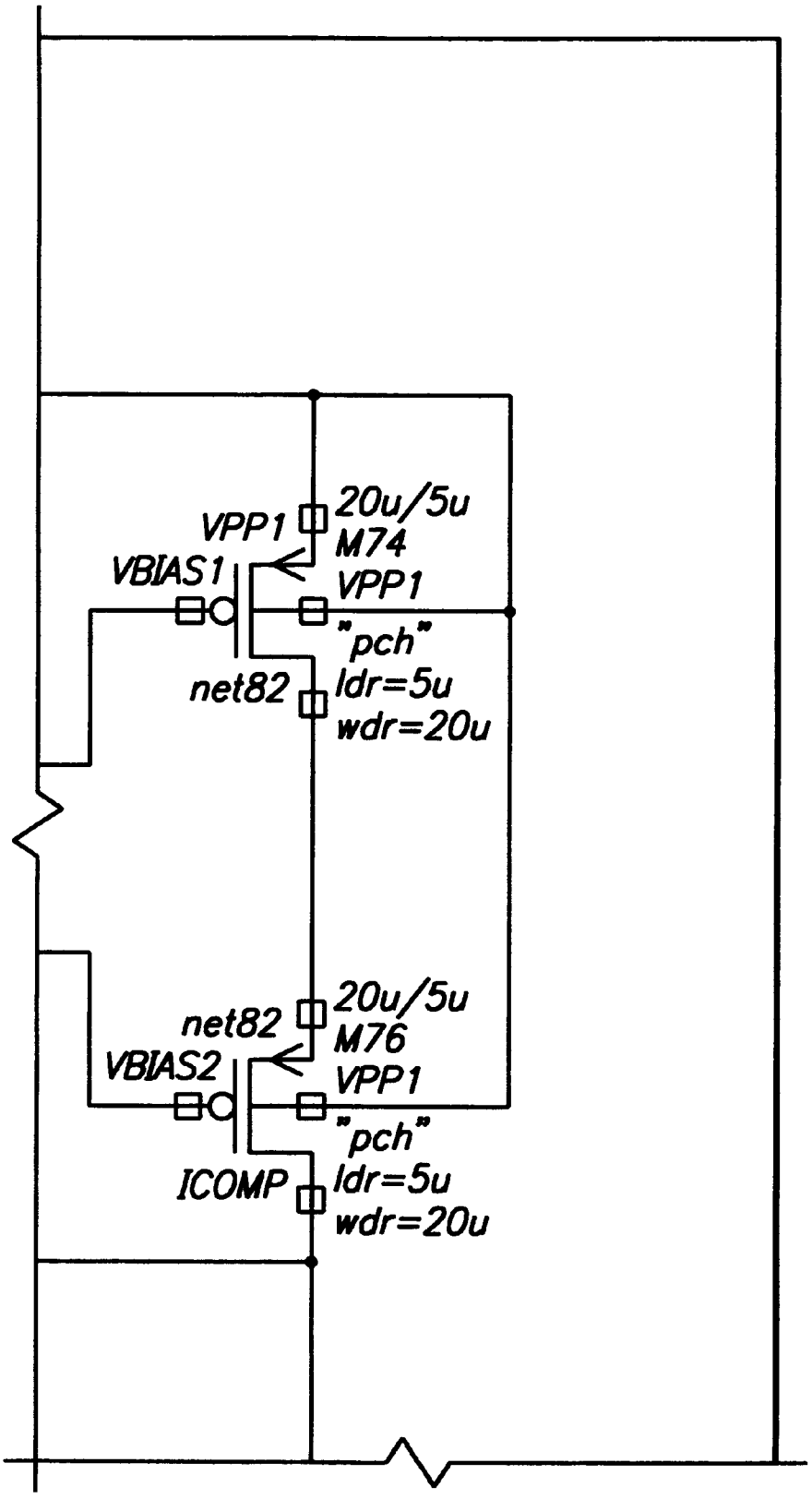

VPP1
20u/5u
M74
VBIAS1
VPP1
"pch"
net82
ldr=5u
wdr=20u
net82
20u/5u
M76
VBIAS2
VPP1
"pch"
ICOMP
ldr=5u
wdr=20u

Fig 9.0302Aa

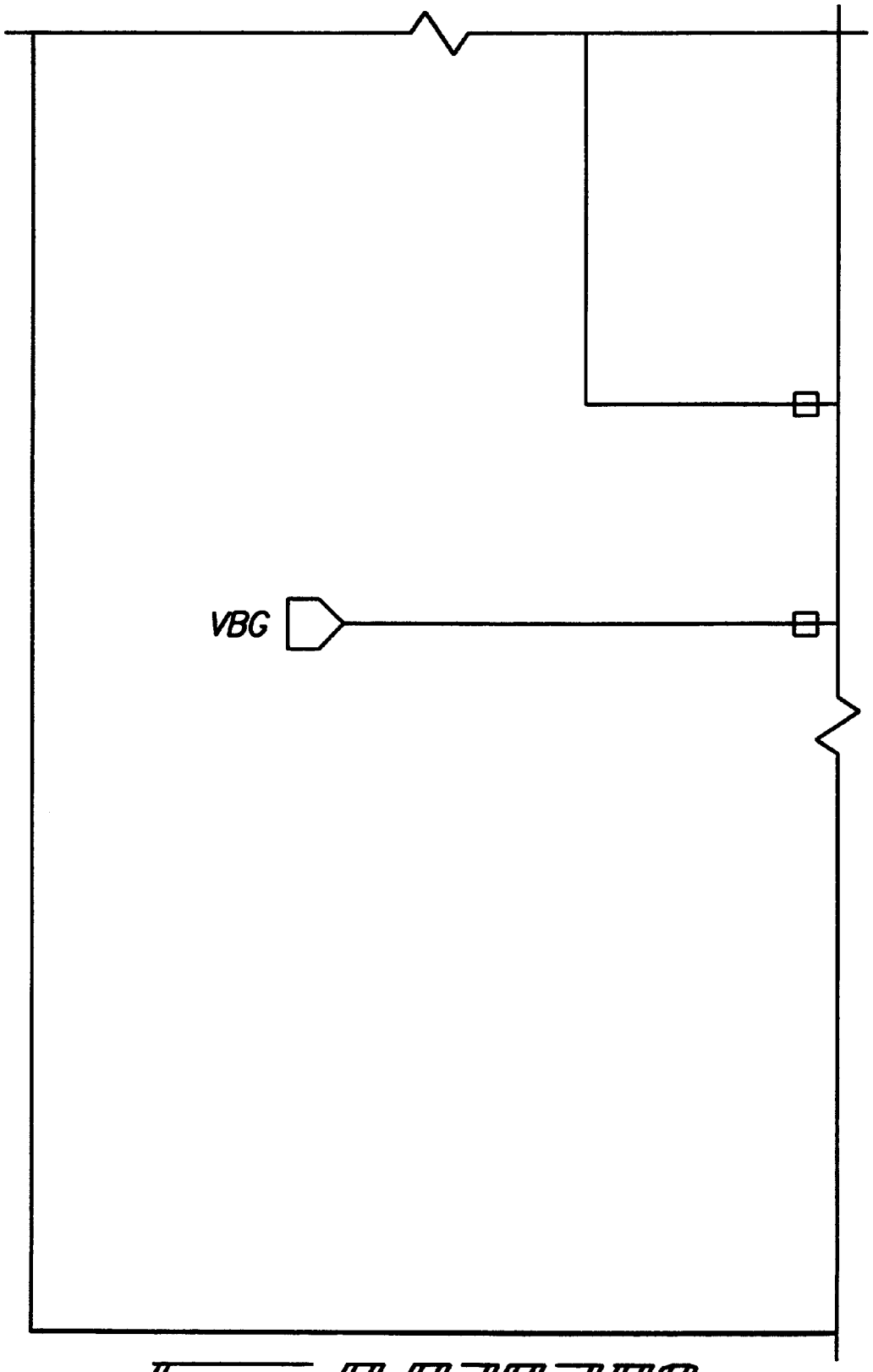


Fig 9.00302BA

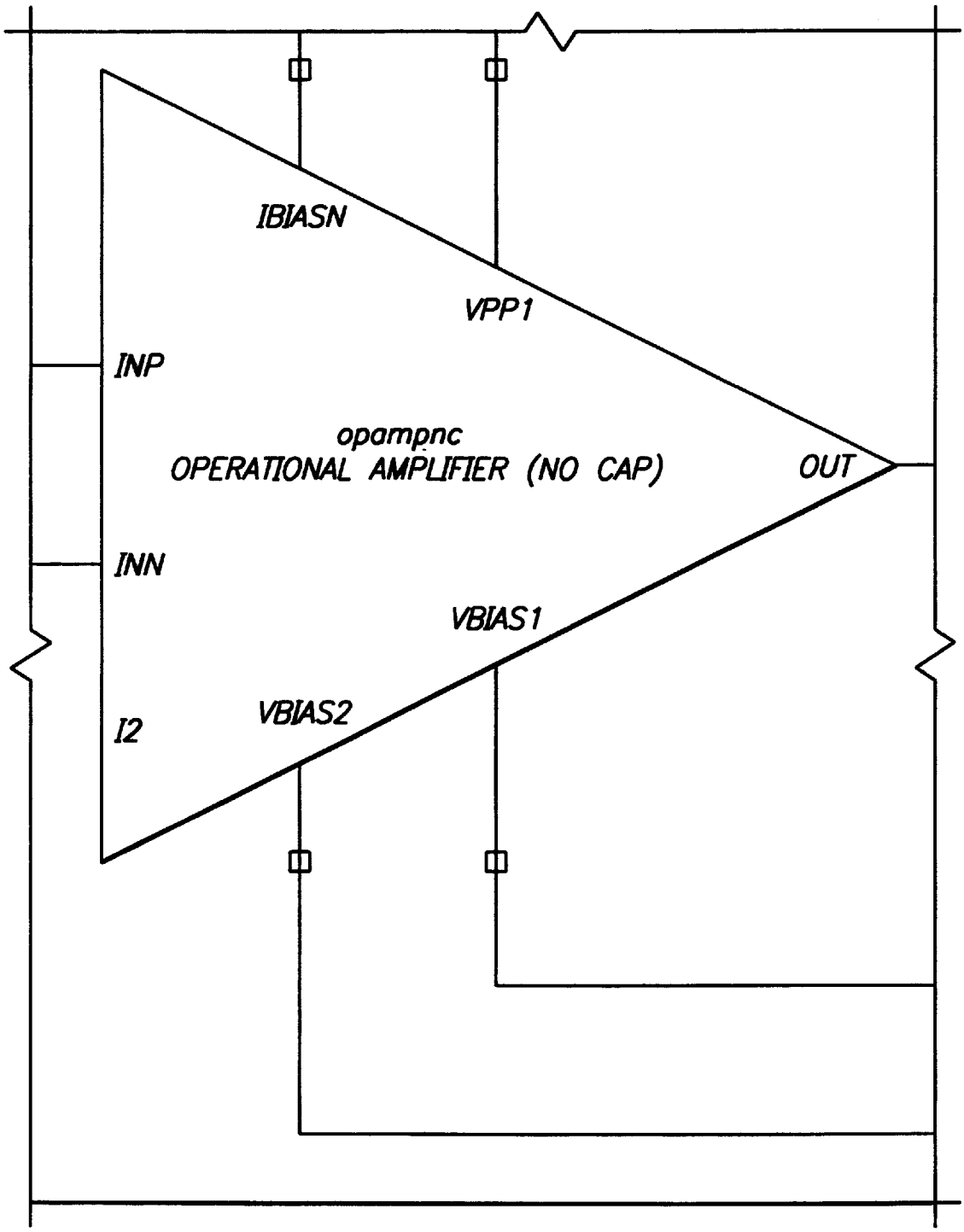

IBIASN
VPP1
INP
opampnc
OPERATIONAL AMPLIFIER (NO CAP)
OUT
INN
VBIAS1
VBIAS2
I2

Fig 9.0302BB

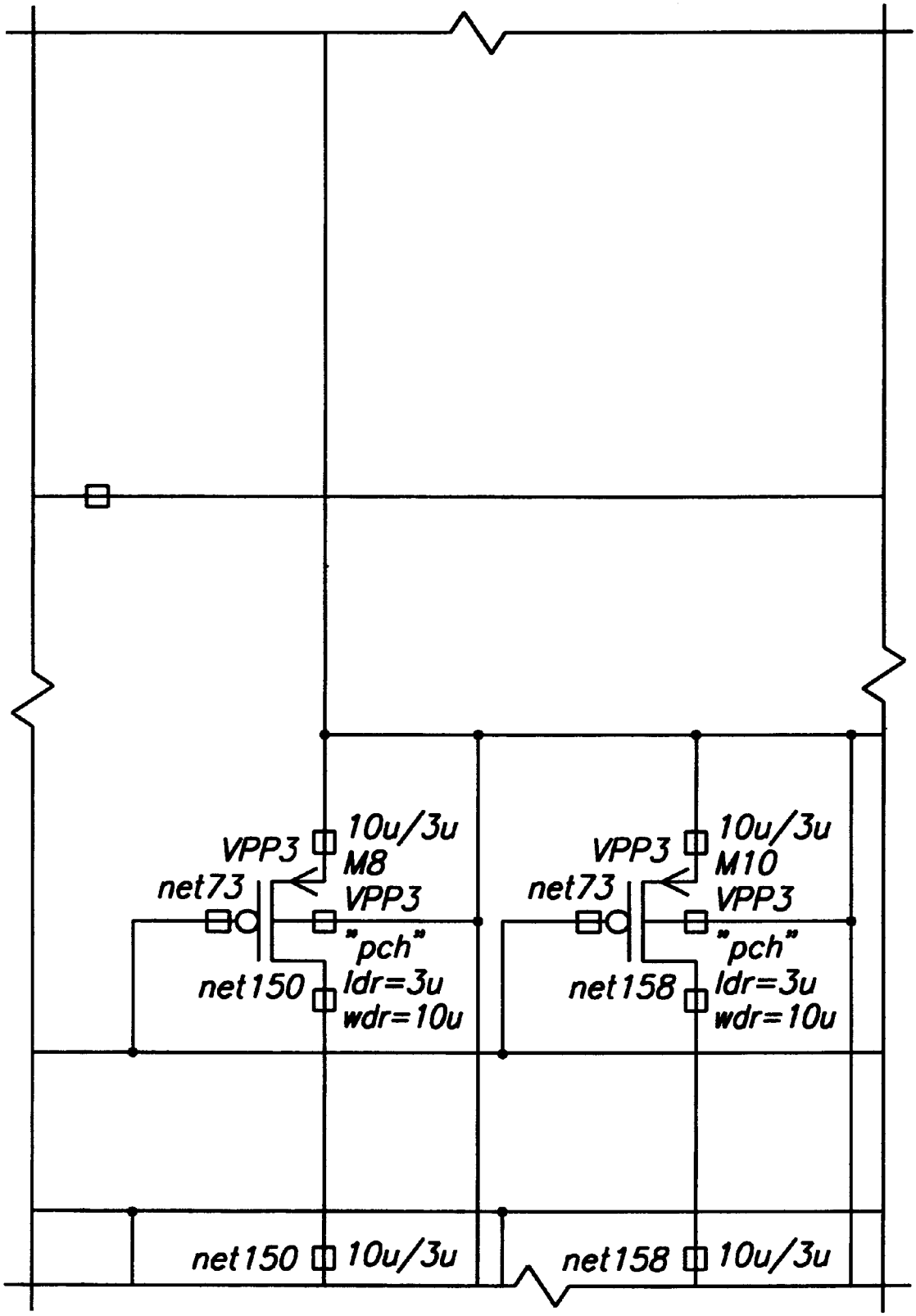


Fig 9.0300zBC

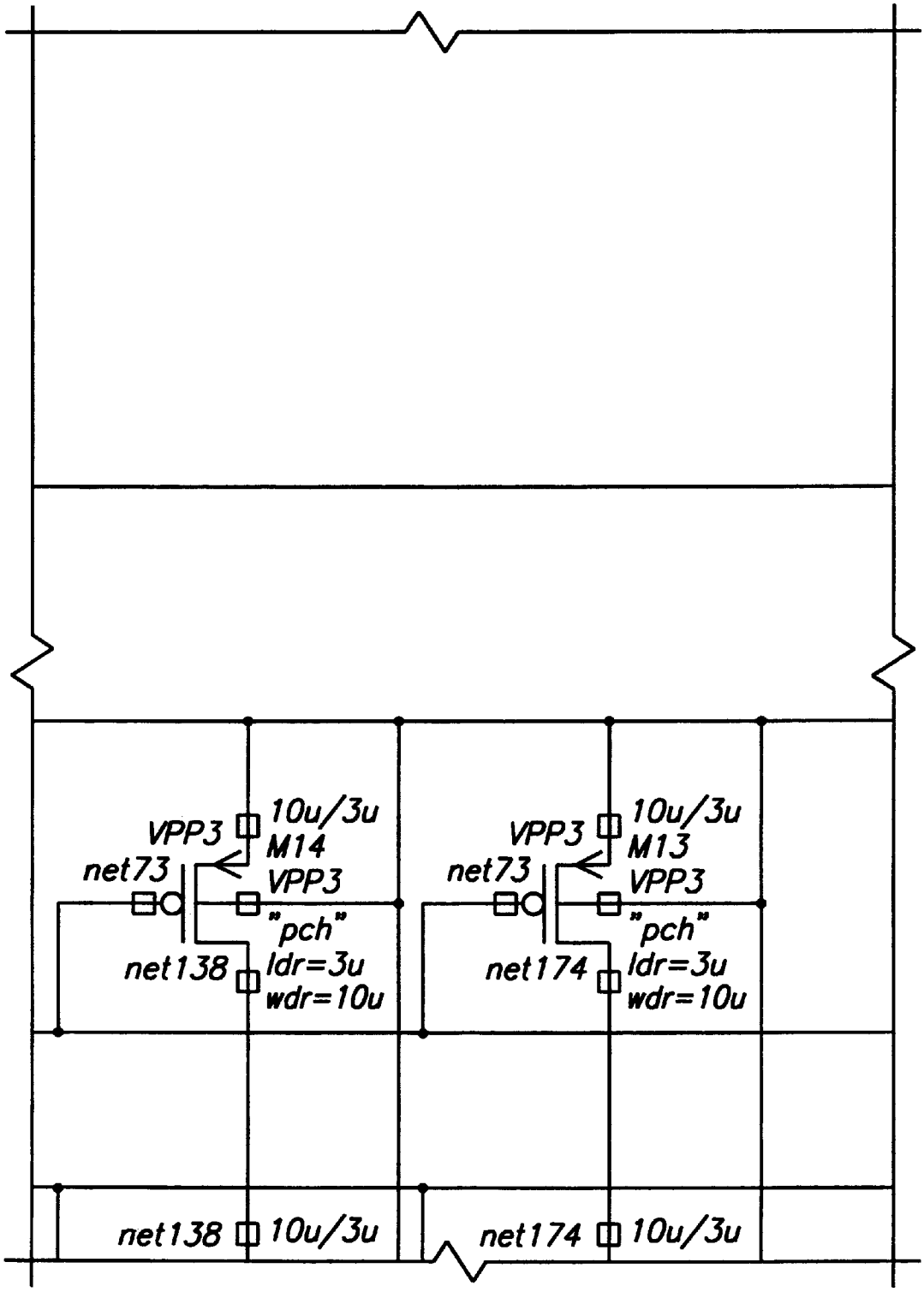

VPP3
10u/3u
M14
net73
VPP3
"pch"
net138
ldr=3u
wdr=10u
VPP3
10u/3u
M13
net73
VPP3
"pch"
net174
ldr=3u
wdr=10u
net138
10u/3u
net174
10u/3u

Fig 9.0302BD

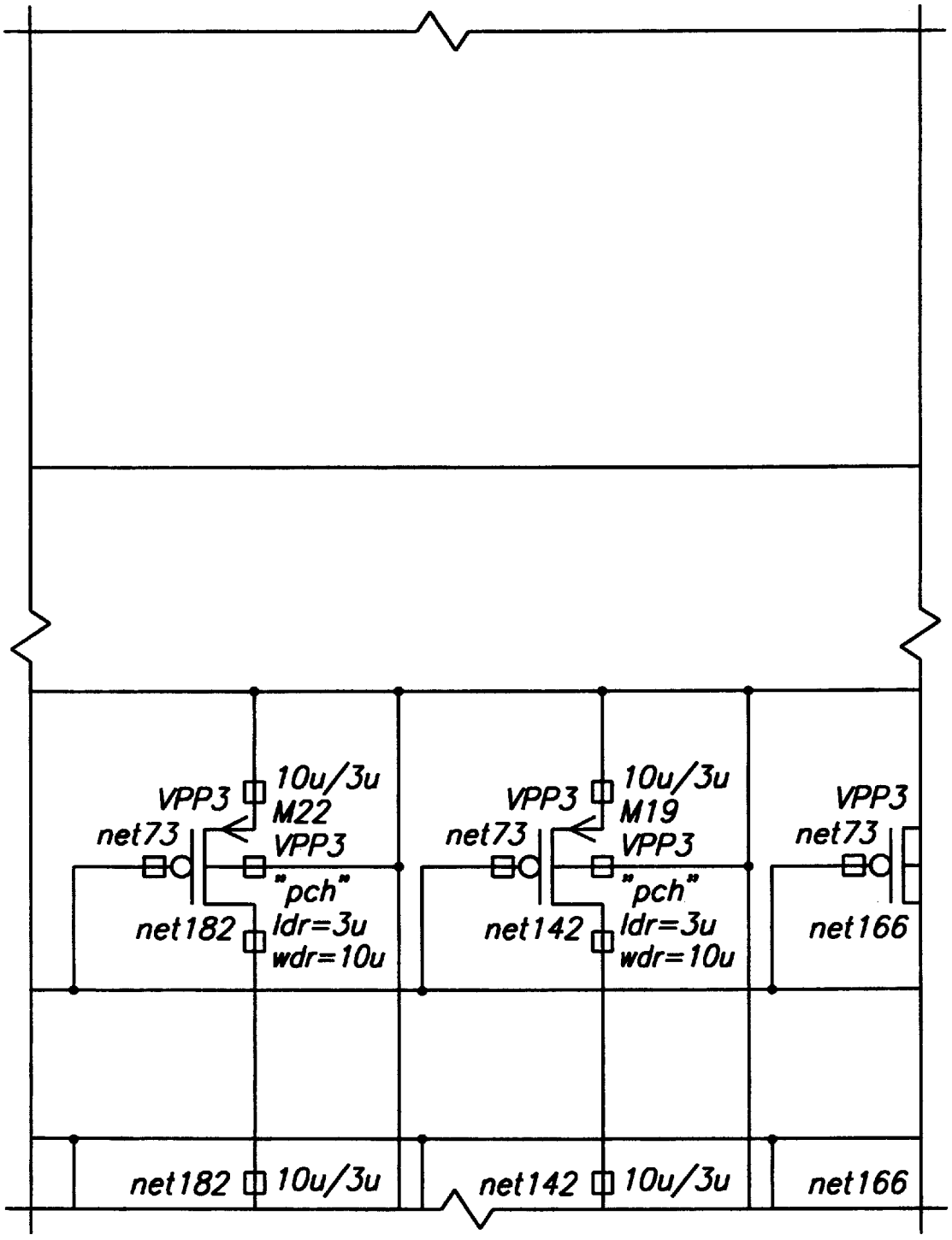

VPP3
10u/3u
M22
net73
VPP3
"pch"
net182
ldr=3u
wdr=10u
VPP3
10u/3u
M19
net73
VPP3
"pch"
net142
ldr=3u
wdr=10u
VPP3
net73
net166
net182
10u/3u
net142
10u/3u
net166

Fig 9.0302BE

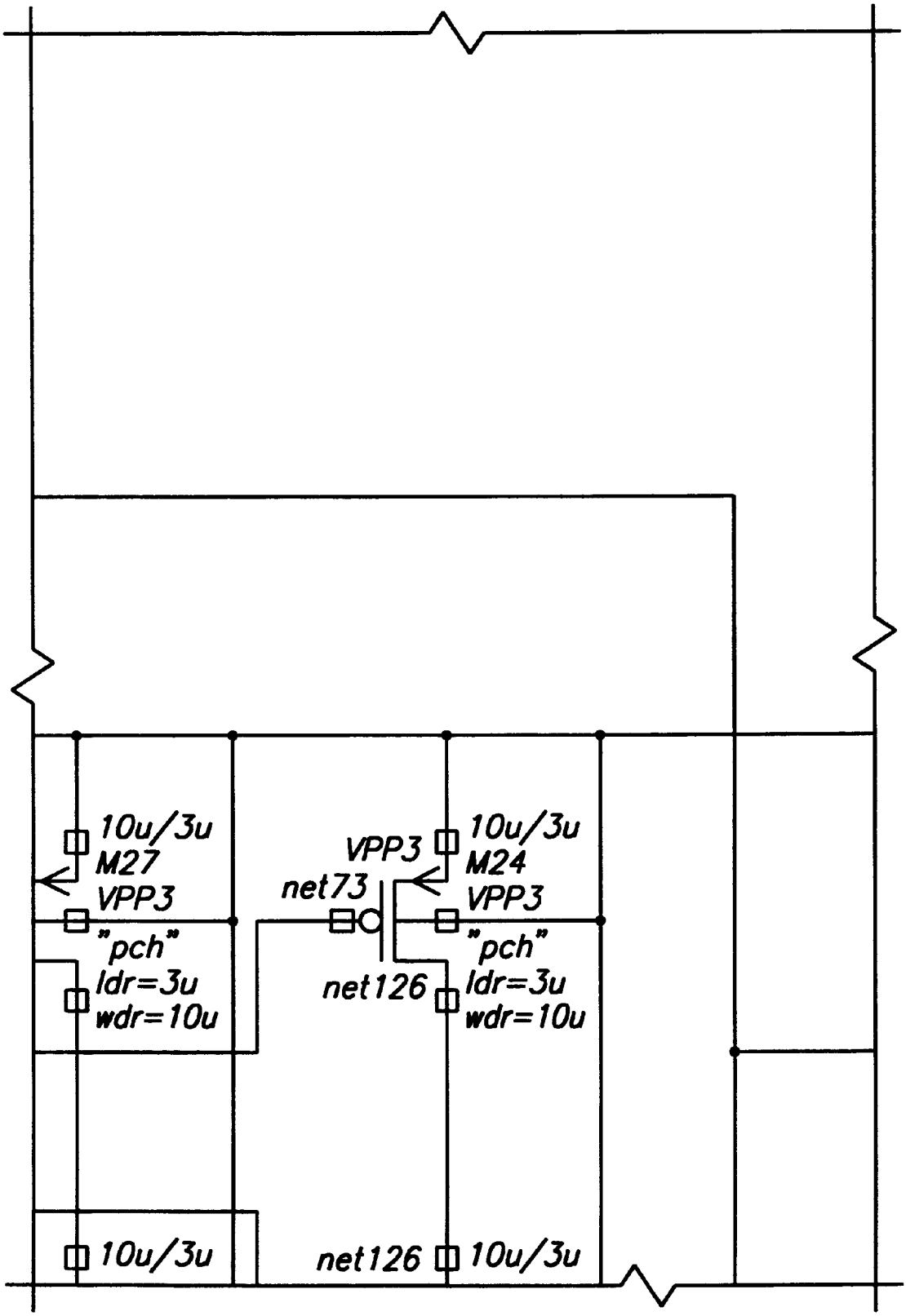

10u/3u
M27
VPP3
"pch"
ldr=3u
wdr=10u
VPP3
net73
net126
10u/3u
M24
VPP3
"pch"
ldr=3u
wdr=10u
10u/3u
net126
10u/3u

Fig 9,030,2BF

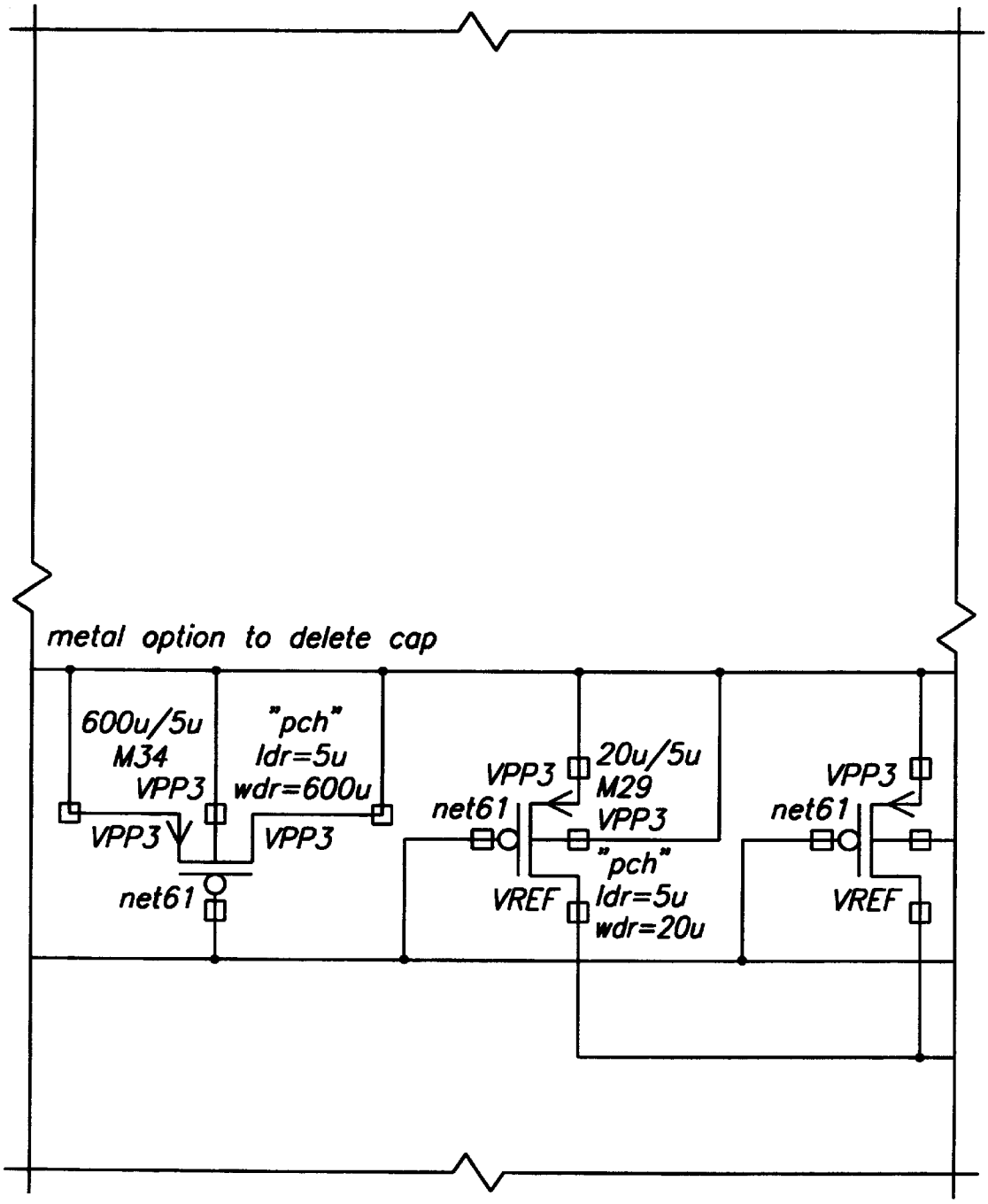


Fig 9.003028B6

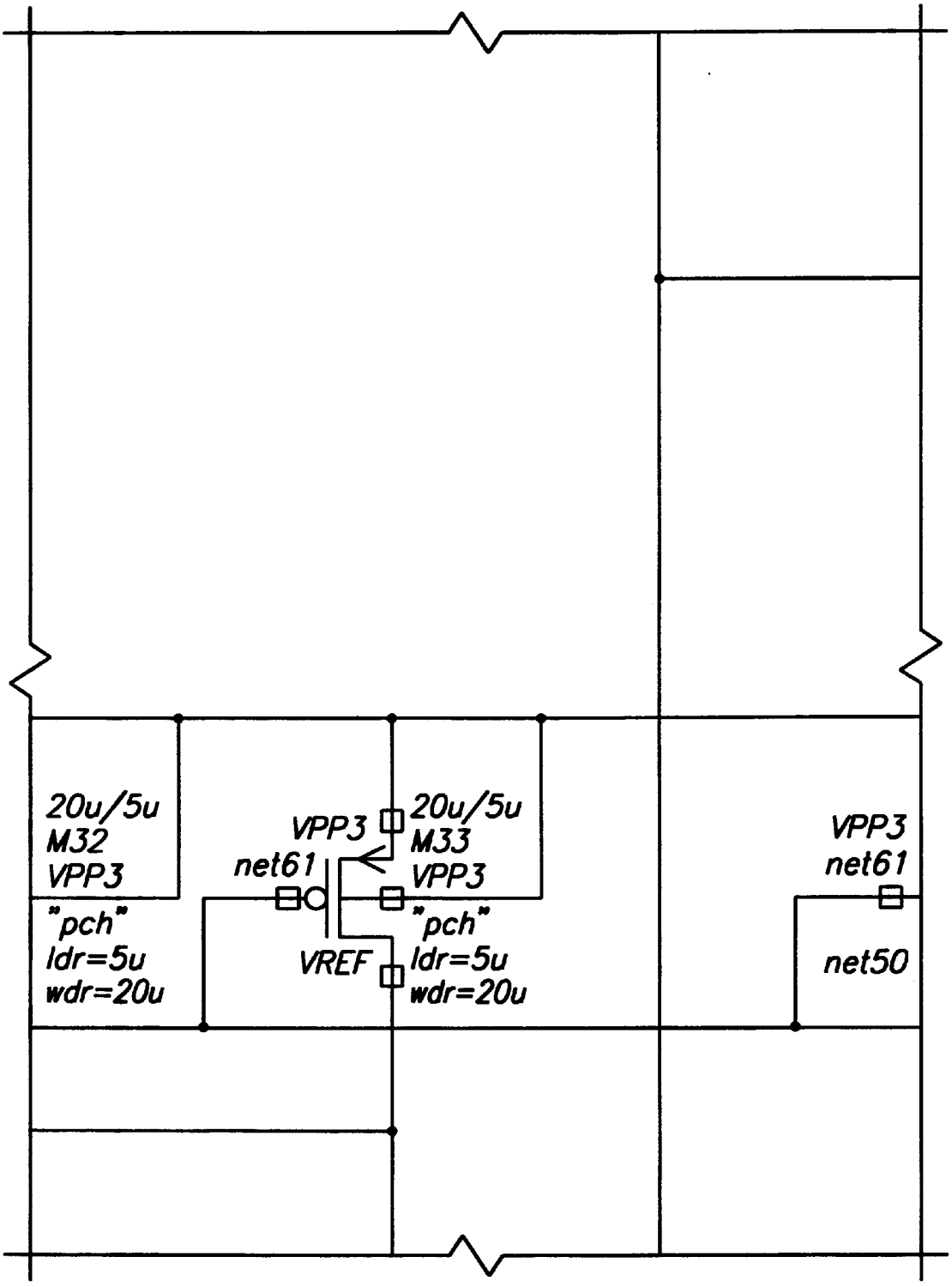


Fig 9.030208H

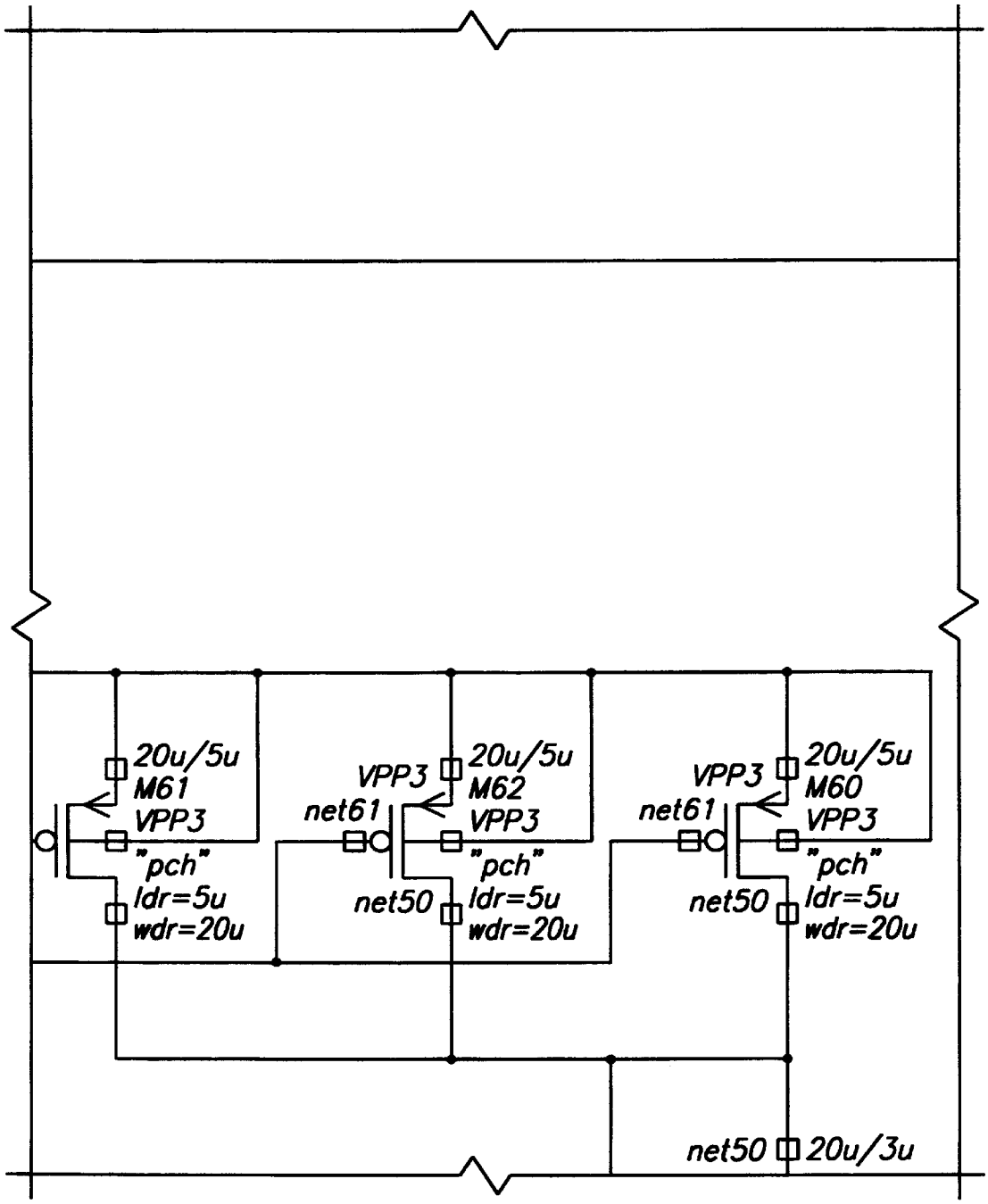

20u/5u
M61
VPP3
"pch"
ldr=5u
wdr=20u
VPP3
net61
20u/5u
M62
VPP3
"pch"
net50
ldr=5u
wdr=20u
VPP3
net61
20u/5u
M60
VPP3
"pch"
net50
ldr=5u
wdr=20u
net50
20u/3u

FIG 9.0302BI

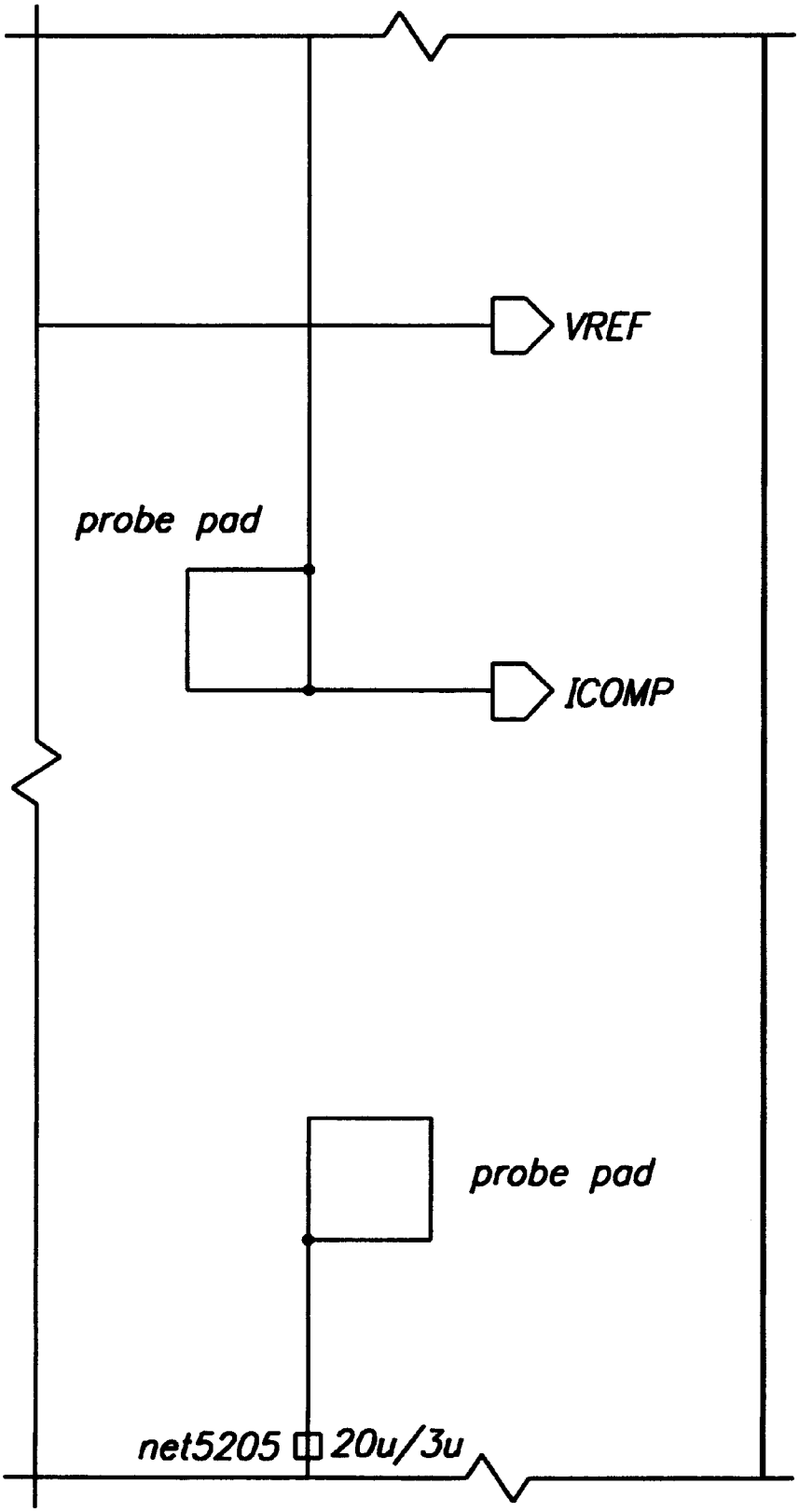


Fig 9.003028a

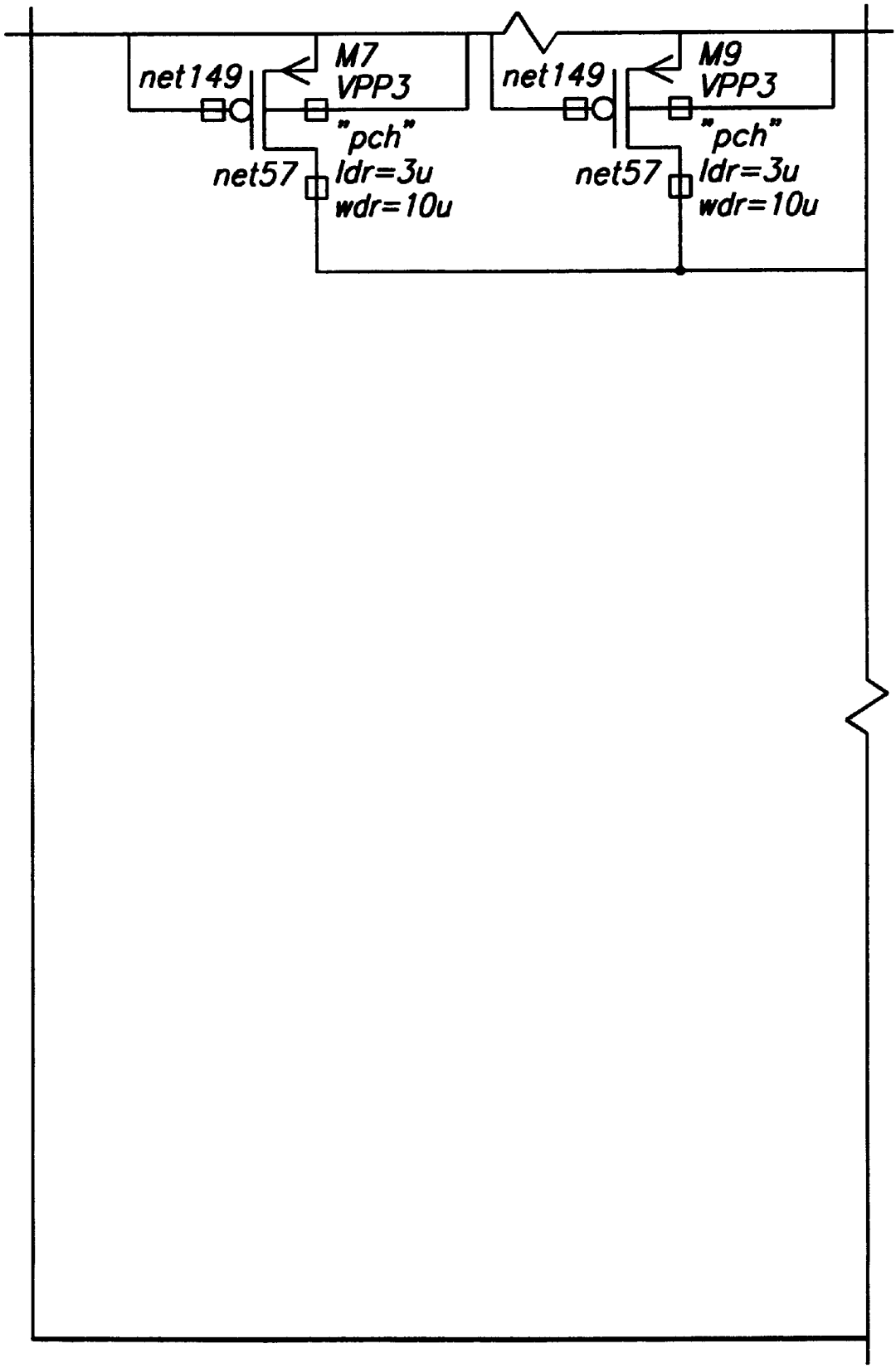

net149
M7
VPP3
"pch"
net57
ldr=3u
wdr=10u
net149
M9
VPP3
"pch"
net57
ldr=3u
wdr=10u

Fig 9.0302CC

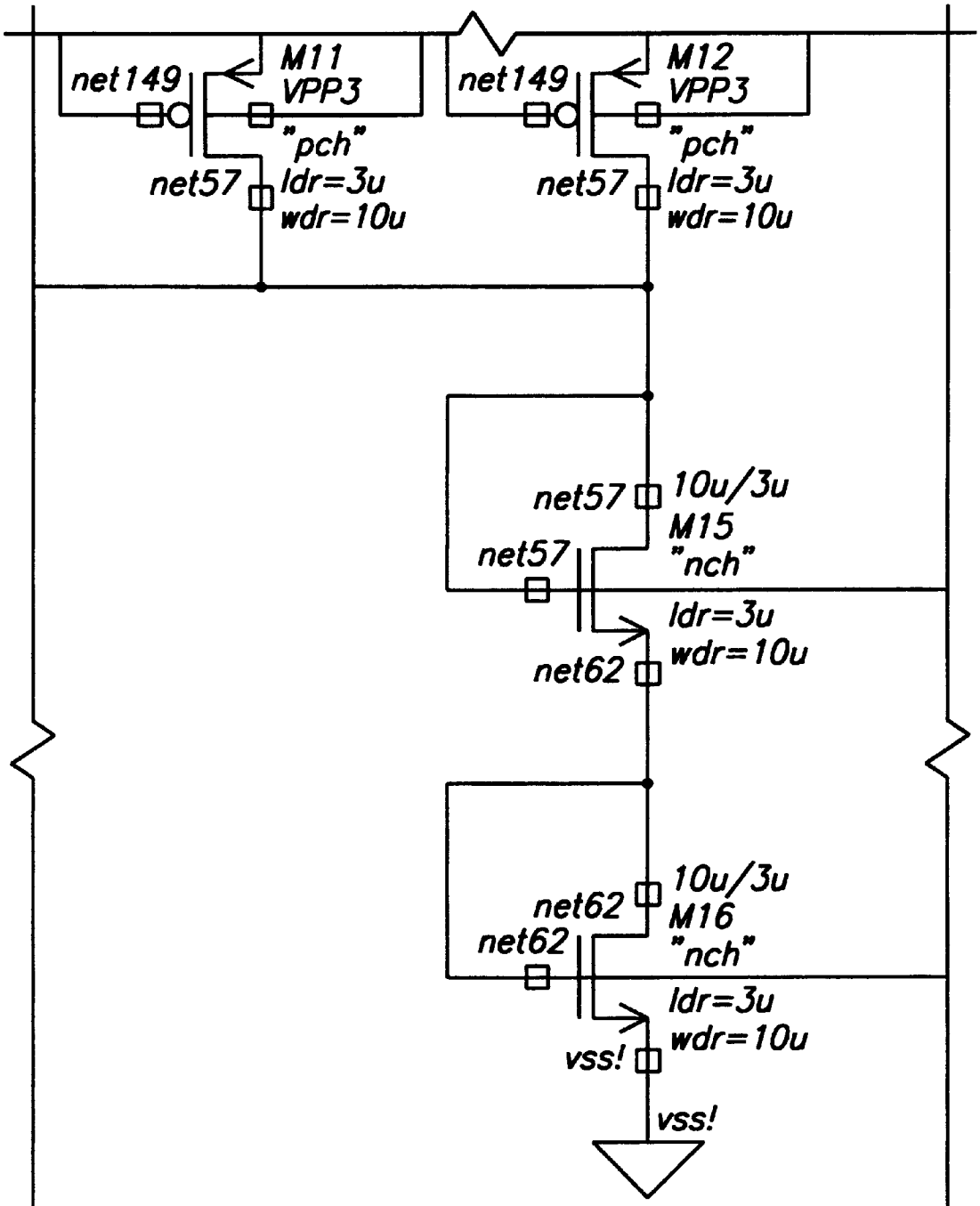

net149
M11
VPP3
"pch"
net57
ldr=3u
wdr=10u
net149
M12
VPP3
"pch"
net57
ldr=3u
wdr=10u
net57
10u/3u
M15
"nch"
net57
ldr=3u
wdr=10u
net62
10u/3u
M16
"nch"
net62
net62
ldr=3u
wdr=10u
vss!
vss!

Fig 9.0302CD

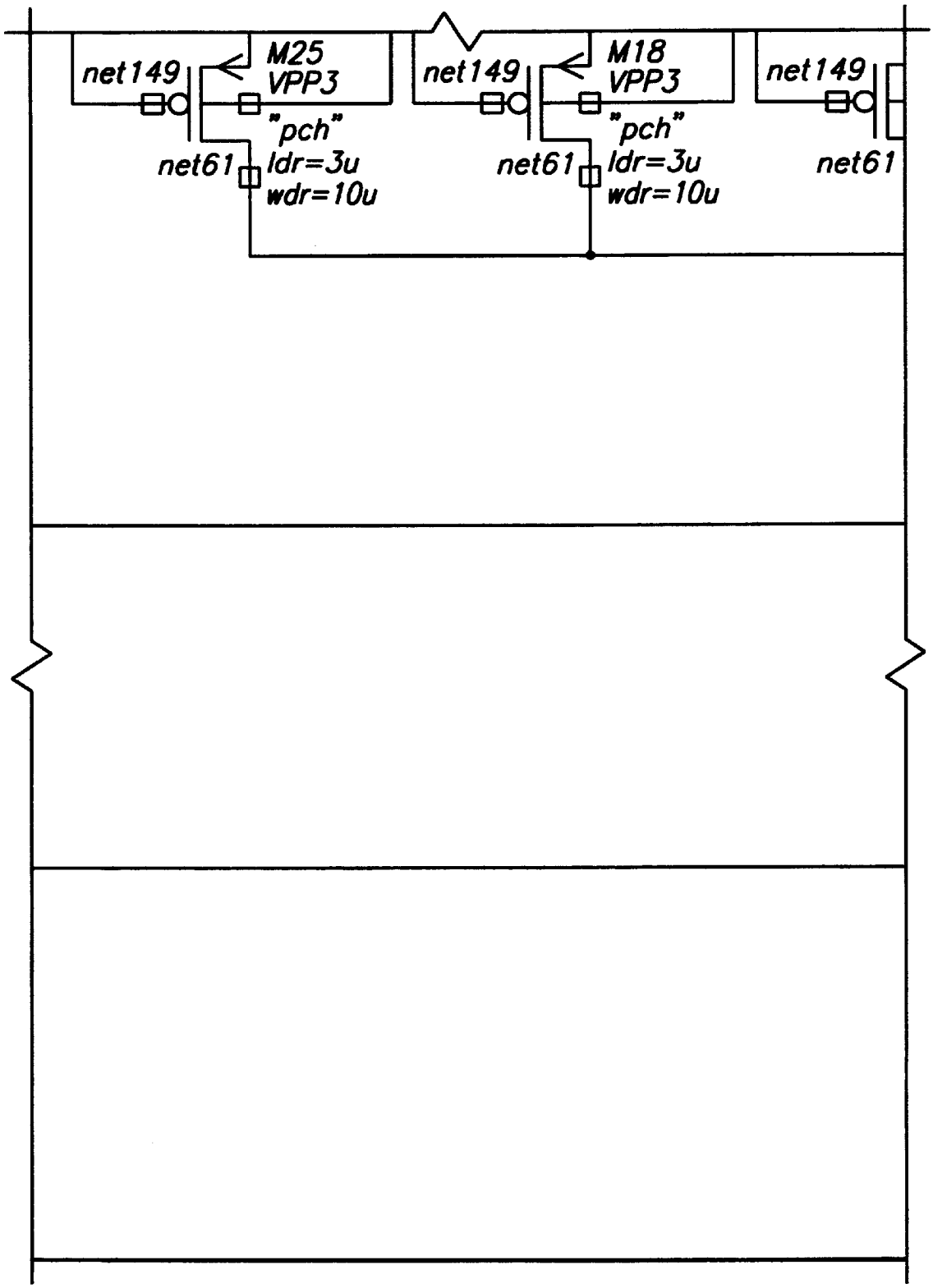

net149
M25
VPP3
"pch"
net61
ldr=3u
wdr=10u
net149
M18
VPP3
"pch"
net61
ldr=3u
wdr=10u
net149
net61

Fig 9.0302CE

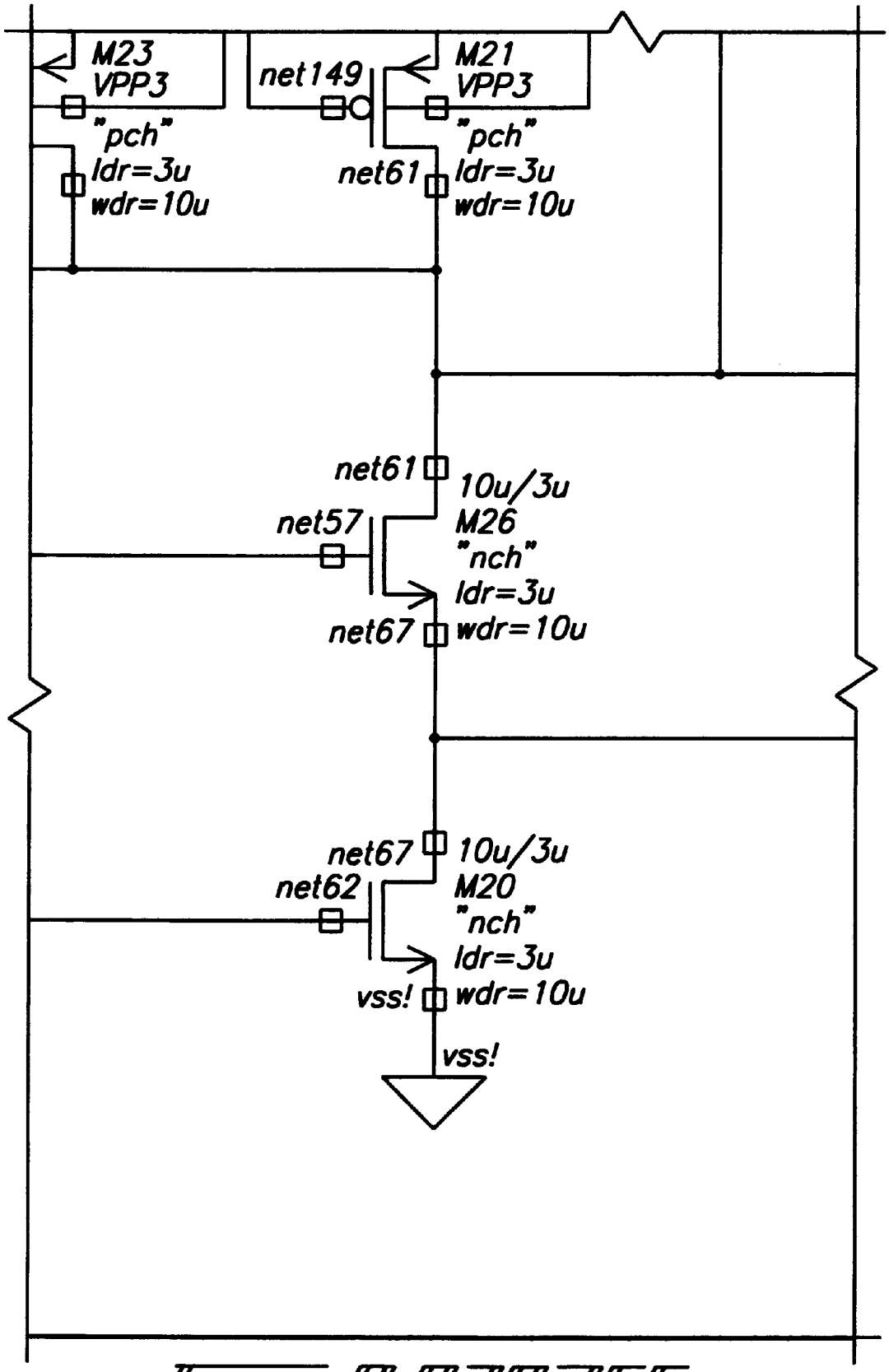

M23
VPP3
"pch"
ldr=3u
wdr=10u
net149
net61
M21
VPP3
"pch"
ldr=3u
wdr=10u
net61
10u/3u
net57
M26
"nch"
ldr=3u
net67
wdr=10u
net67
10u/3u
net62
M20
"nch"
ldr=3u
vss!
wdr=10u
vss!

Fig 9.0302CF

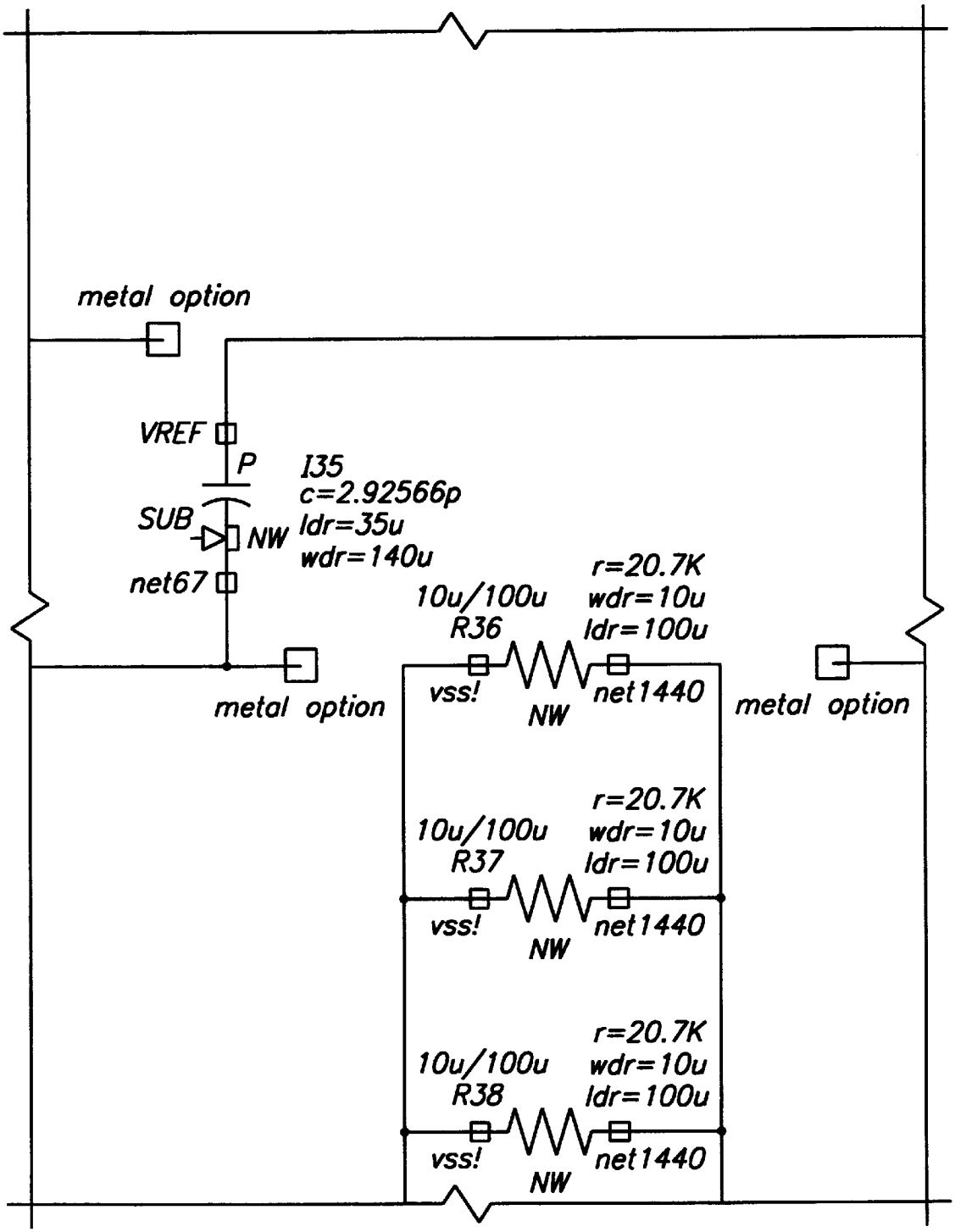

metal option
VREF
P
I35
c=2.92566p
SUB
NW
ldr=35u
wdr=140u
net67
10u/100u
R36
r=20.7K
wdr=10u
ldr=100u
vss!
NW
net1440
metal option
metal option
10u/100u
R37
r=20.7K
wdr=10u
ldr=100u
vss!
NW
net1440
10u/100u
R38
r=20.7K
wdr=10u
ldr=100u
vss!
NW
net1440

Fig 9.030206

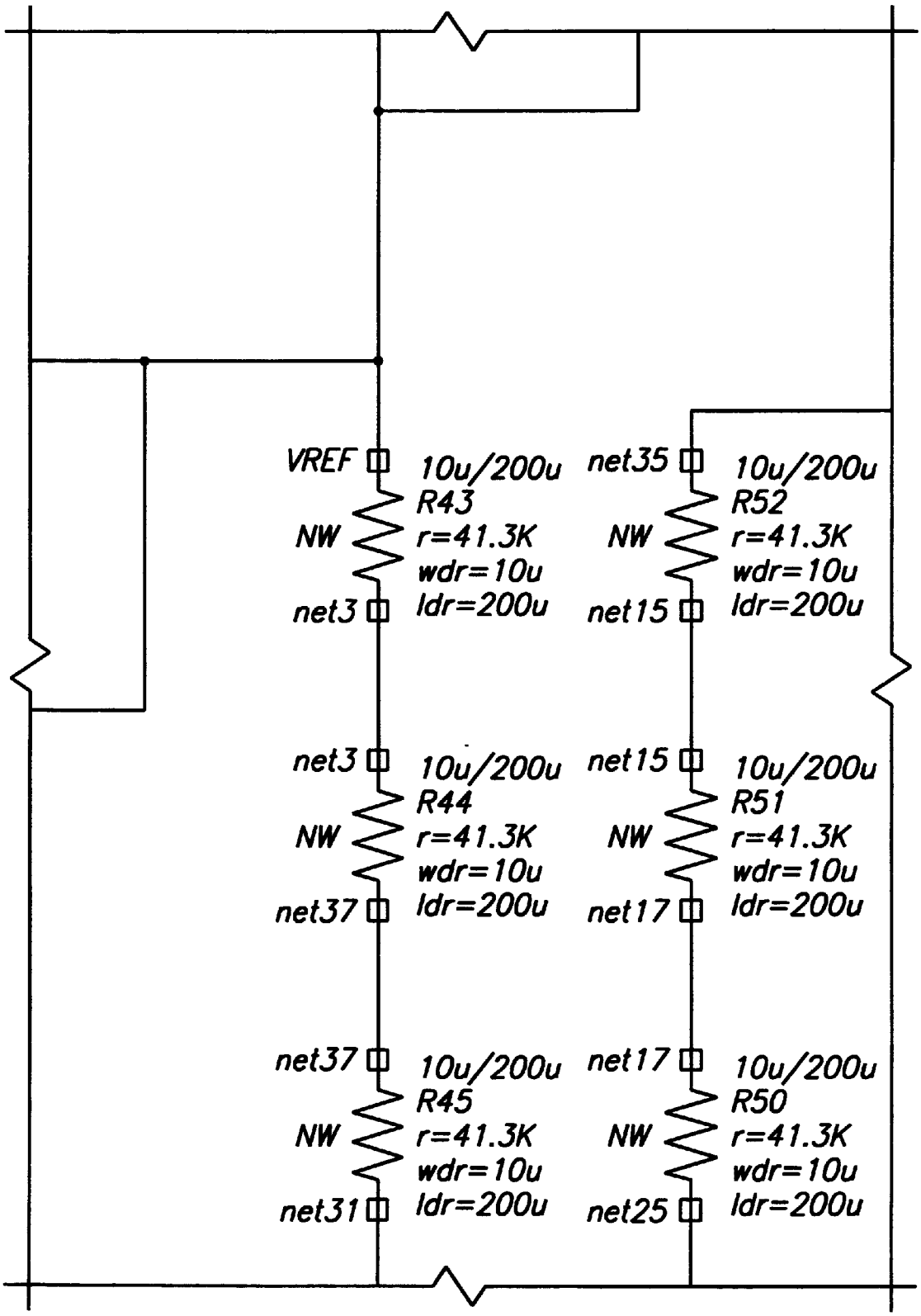

VREF
10u/200u
R43
NW
r=41.3K
wdr=10u
net3
ldr=200u
net35
10u/200u
R52
NW
r=41.3K
wdr=10u
net15
ldr=200u
net3
10u/200u
R44
NW
r=41.3K
wdr=10u
net37
ldr=200u
net15
10u/200u
R51
NW
r=41.3K
wdr=10u
net17
ldr=200u
net37
10u/200u
R45
NW
r=41.3K
wdr=10u
net31
ldr=200u
net17
10u/200u
R50
NW
r=41.3K
wdr=10u
net25
ldr=200u

Fig 9,030,2CH

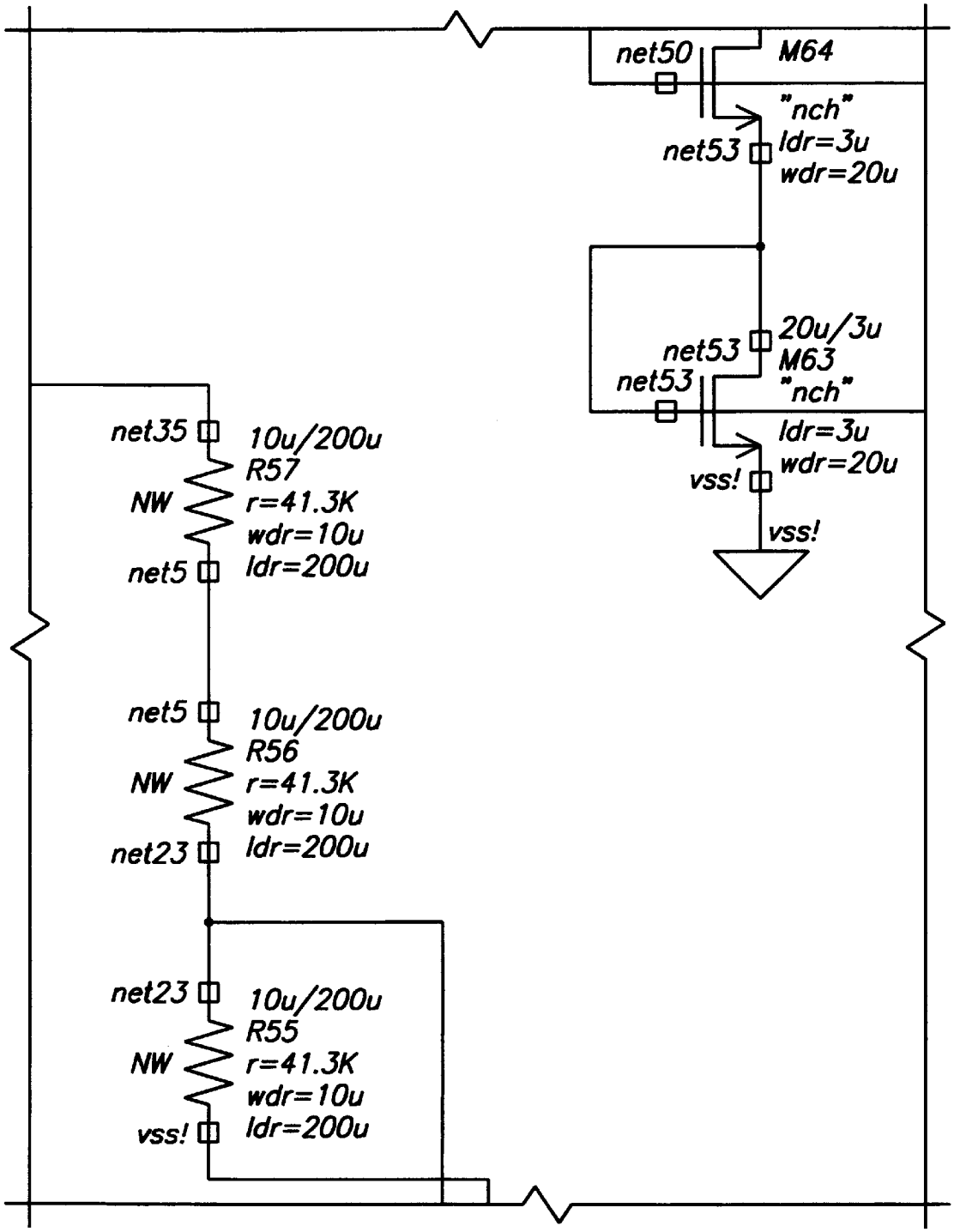

net50
M64
"nch"
net53
ldr=3u
wdr=20u
20u/3u
net53
M63
net53
"nch"
ldr=3u
wdr=20u
vss!
vss!
net35
10u/200u
R57
NW
r=41.3K
wdr=10u
net5
ldr=200u
net5
10u/200u
R56
NW
r=41.3K
wdr=10u
net23
ldr=200u
net23
10u/200u
R55
NW
r=41.3K
wdr=10u
vss!
ldr=200u

Fig 9,030,211

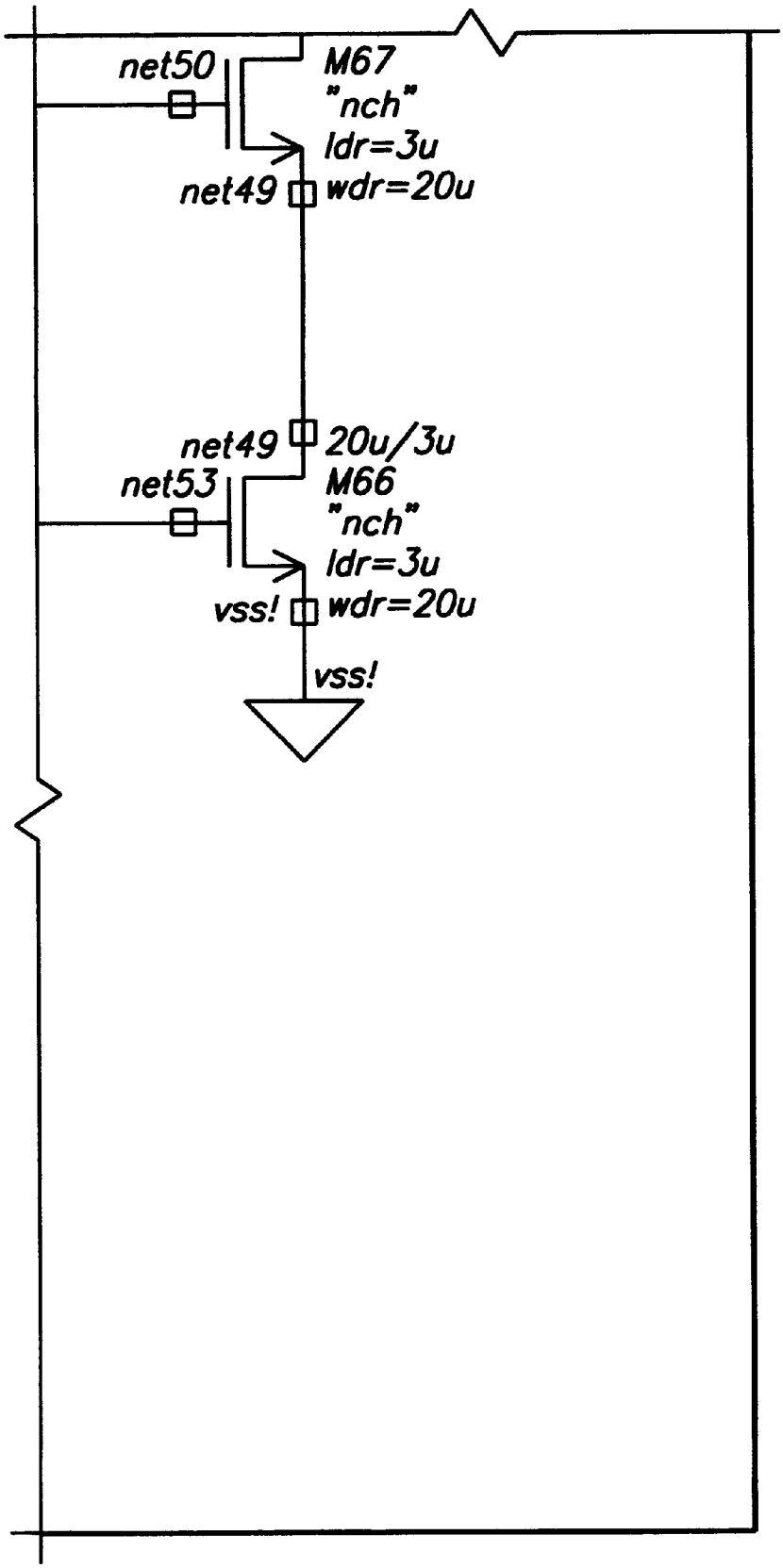


Fig 9.0302Cal

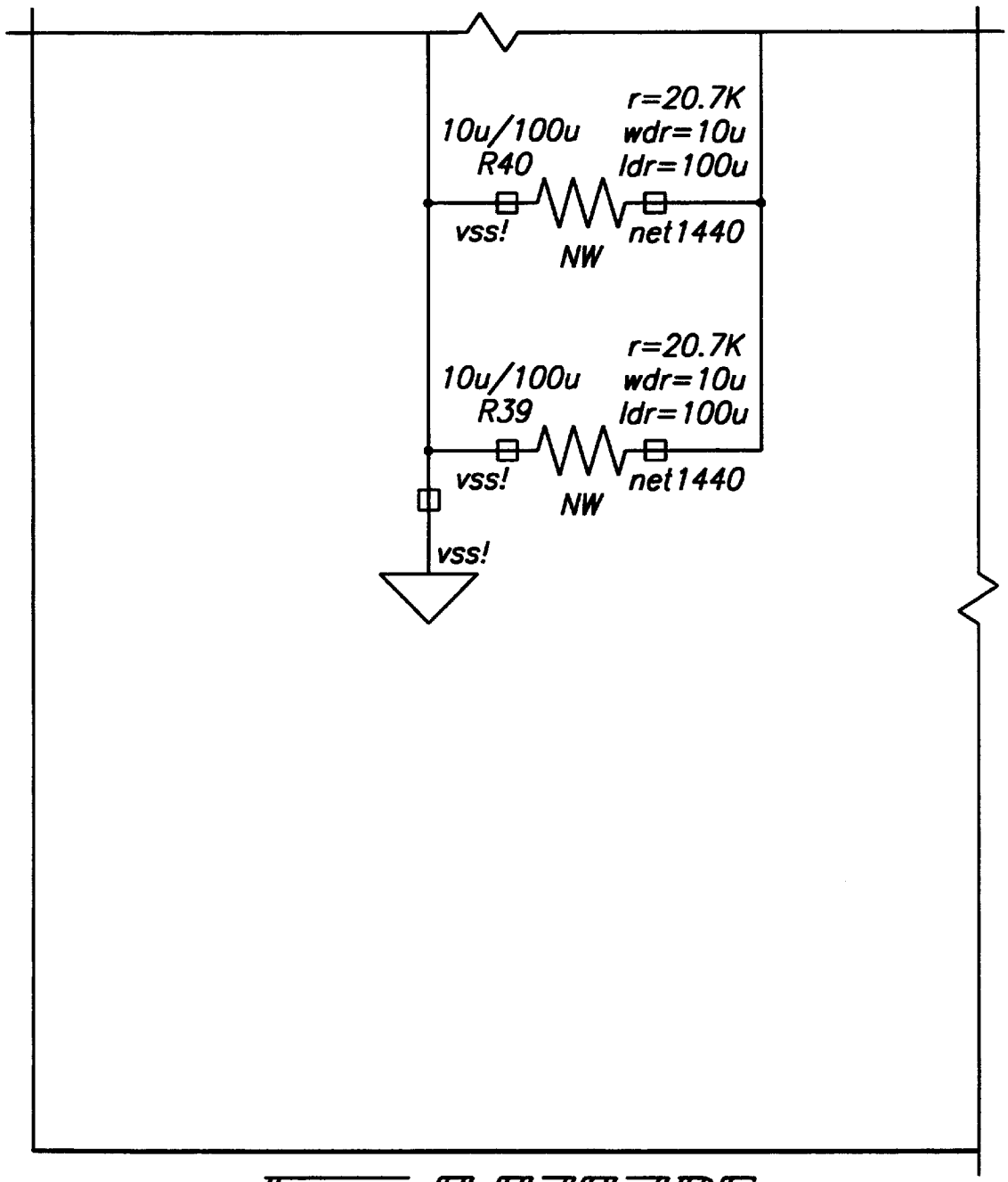

r=20.7K
10u/100u
wdr=10u
R40
ldr=100u
vss!
net1440
NW
r=20.7K
10u/100u
wdr=10u
R39
ldr=100u
vss!
net1440
NW
vss!

Fig 9.003206

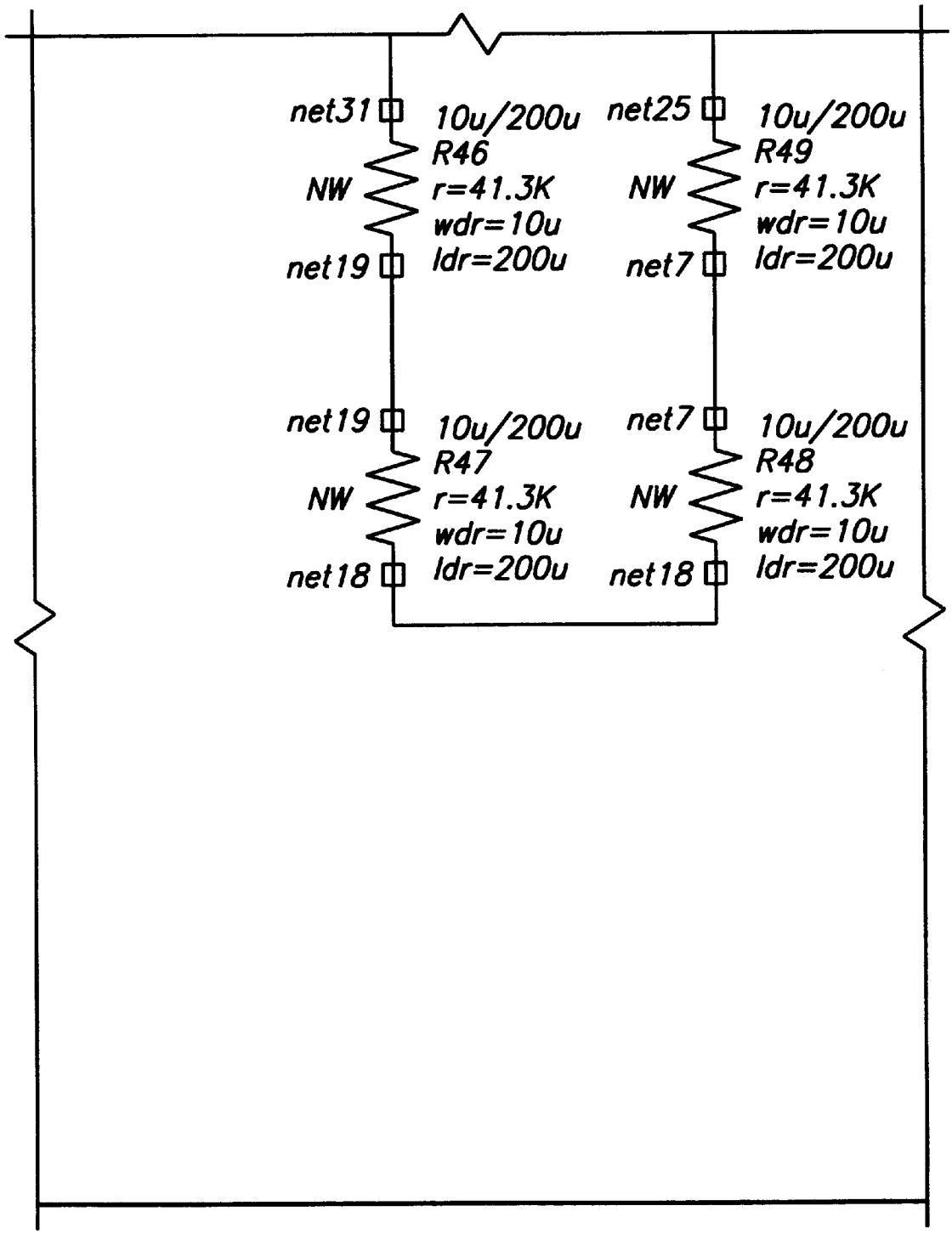

net31
10u/200u
R46
NW
r=41.3K
wdr=10u
net19
ldr=200u
net25
10u/200u
R49
NW
r=41.3K
wdr=10u
net7
ldr=200u
net19
10u/200u
R47
NW
r=41.3K
wdr=10u
net18
ldr=200u
net7
10u/200u
R48
NW
r=41.3K
wdr=10u
net18
ldr=200u

Fig 9.0302DH

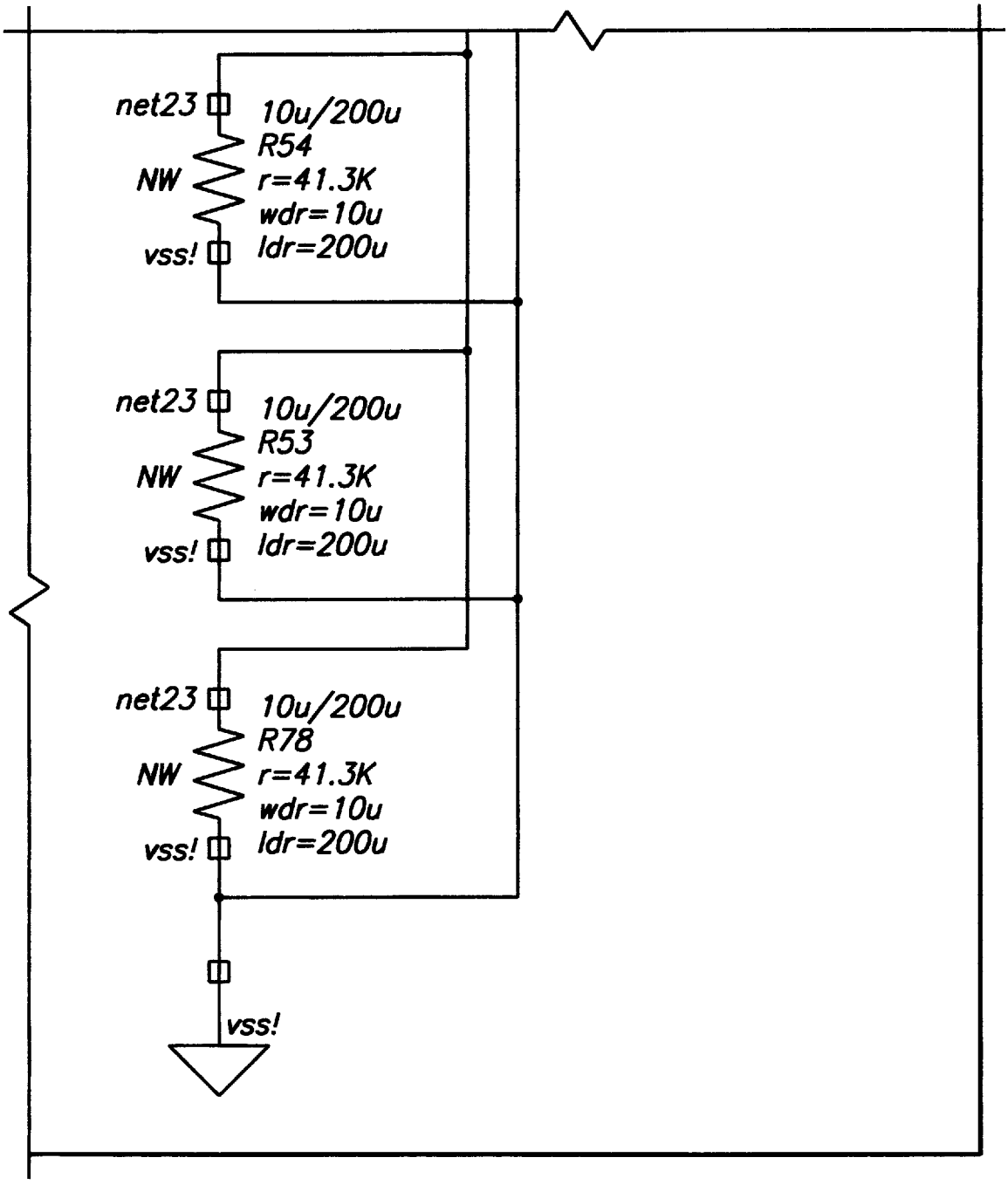

net23
10u/200u
R54
NW
r=41.3K
wdr=10u
vss!
ldr=200u
net23
10u/200u
R53
NW
r=41.3K
wdr=10u
vss!
ldr=200u
net23
10u/200u
R78
NW
r=41.3K
wdr=10u
vss!
ldr=200u
vss!

Fig 9.030201

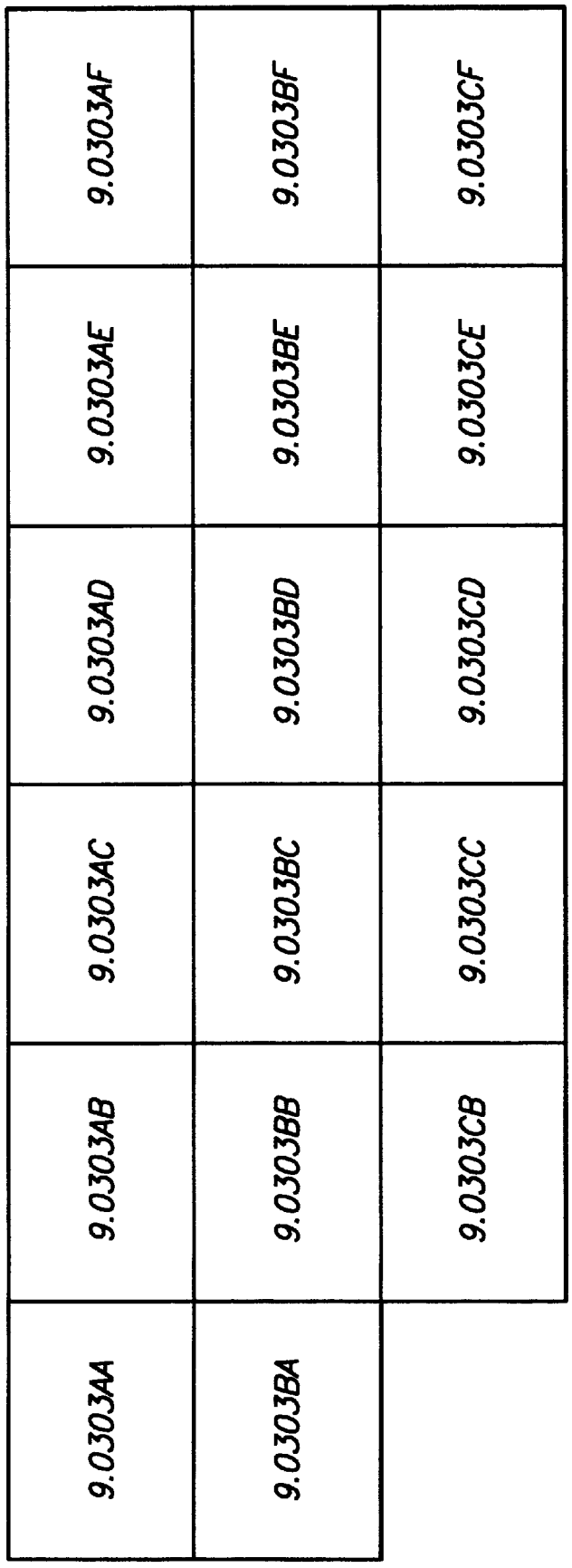

9.0303AA
9.0303AB
9.0303AC
9.0303AD
9.0303AE
9.0303AF
9.0303BA
9.0303BB
9.0303BC
9.0303BD
9.0303BE
9.0303BF
9.0303CB
9.0303CC
9.0303CD
9.0303CE
9.0303CF

FIG 9.0303E

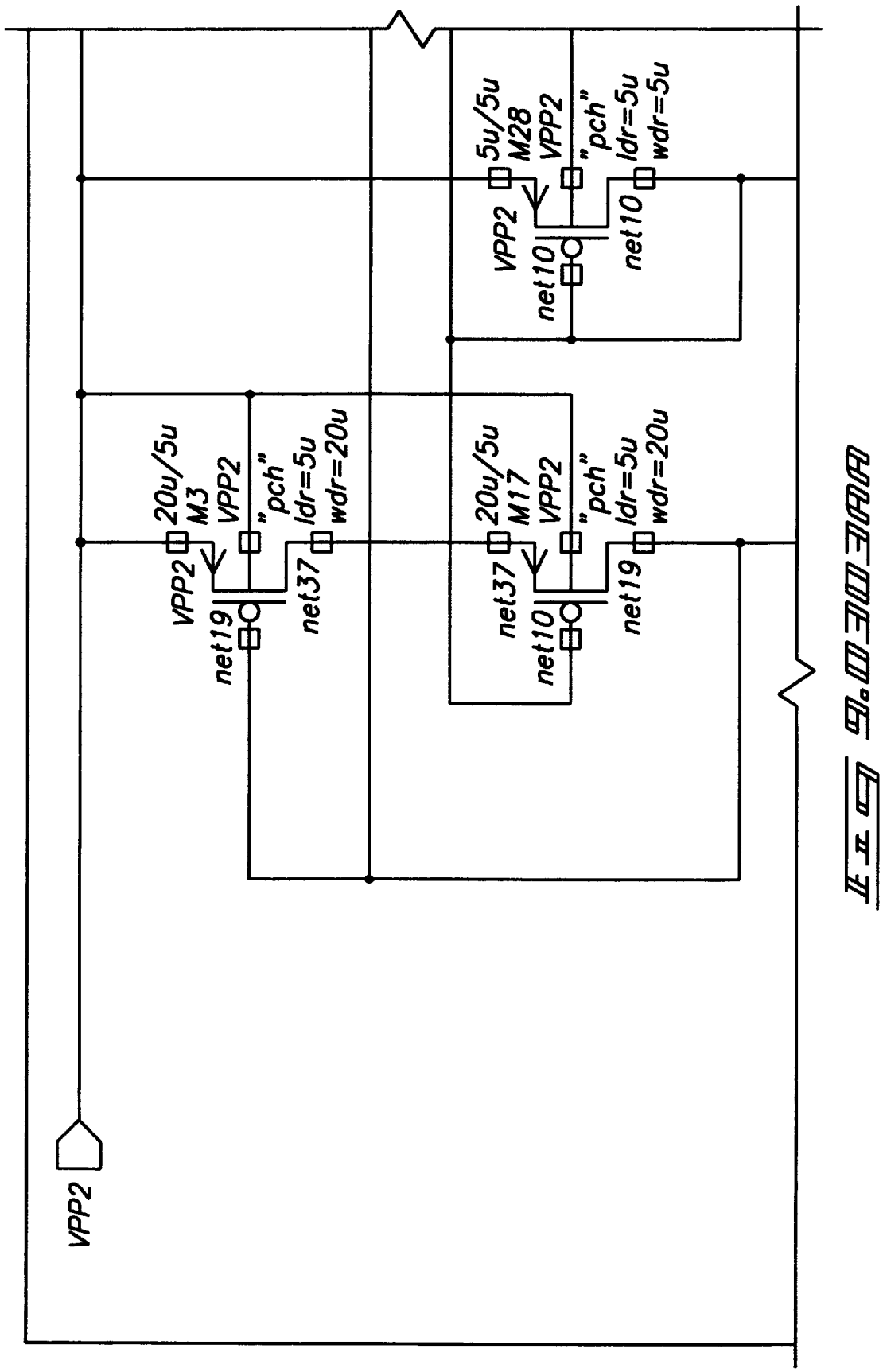

5u/5u
M28
VPP2
"pch"
ldr=5u
wdr=5u
VPP2
net10
net10
20u/5u
M3
VPP2
"pch"
ldr=5u
wdr=20u
VPP2
net19
net37
20u/5u
M17
VPP2
"pch"
ldr=5u
wdr=20u
net37
net10
net19
VPP2

FIG 9B

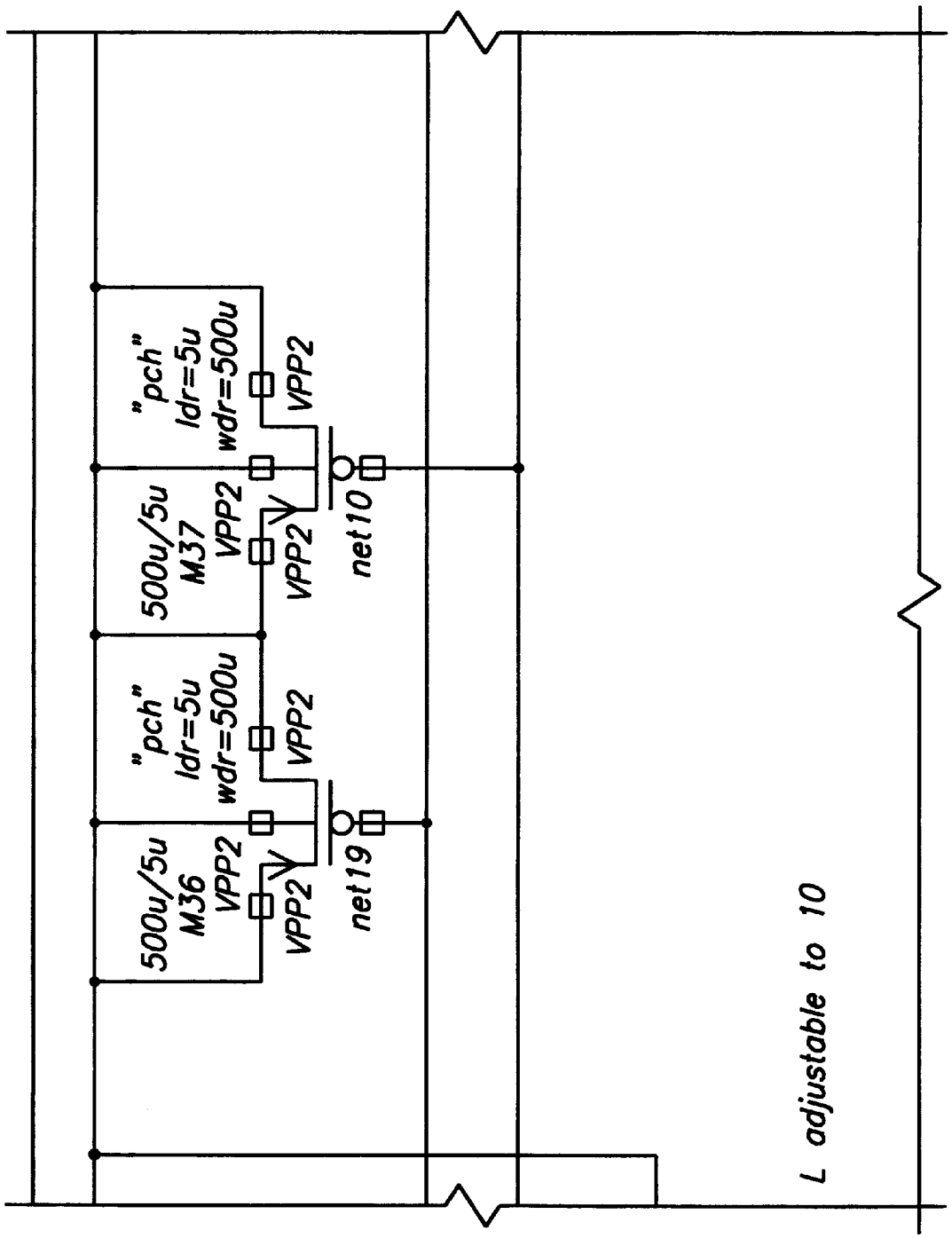

"pch"
ldr=5u
wdr=500u
VPP2
500u/5u
M37
VPP2
VPP2
net10
"pch"
ldr=5u
wdr=500u
VPP2
500u/5u
M36
VPP2
VPP2
net19
L adjustable to 10

FIG 31

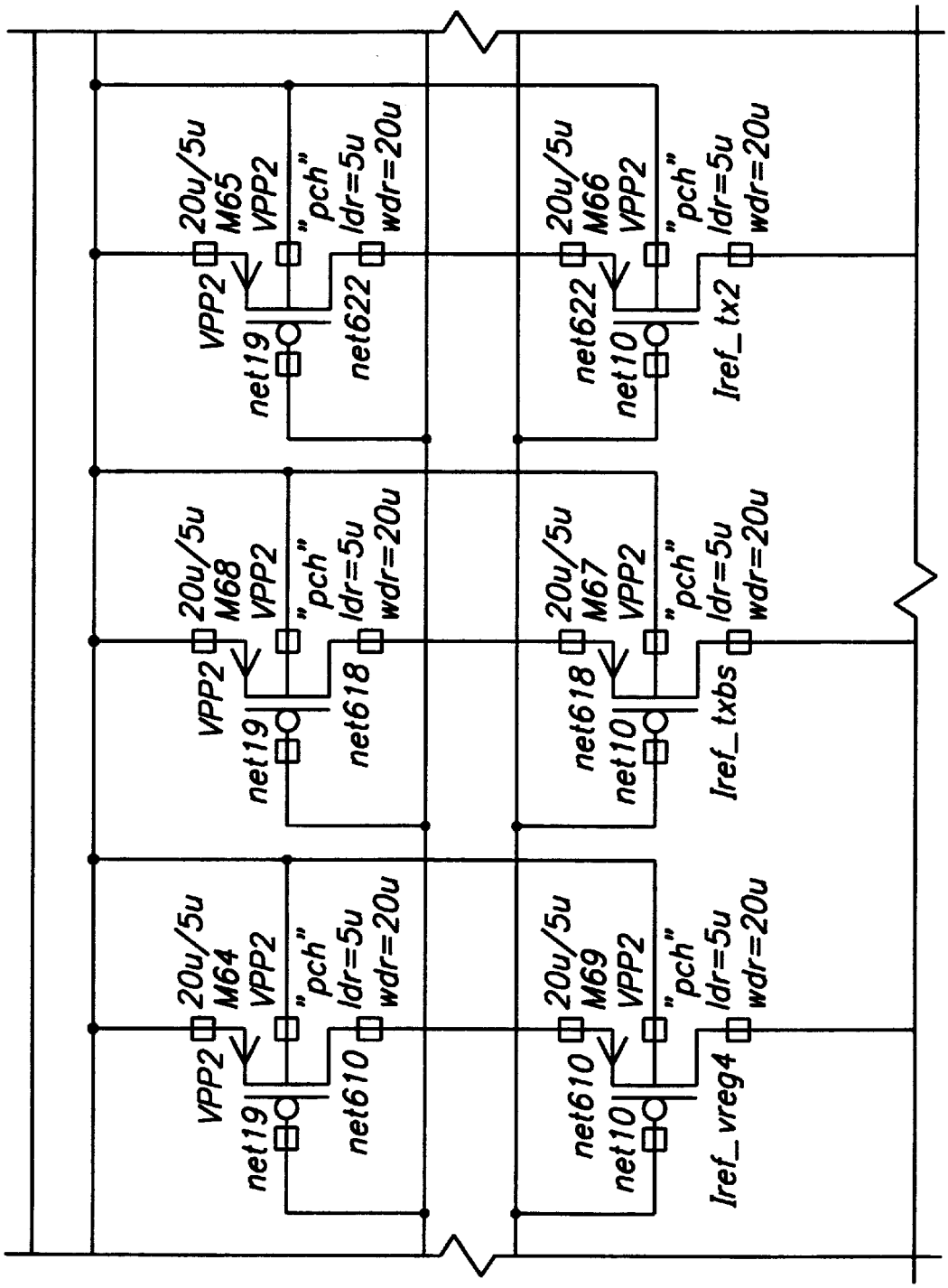

20u/5u
M65
VPP2
"pch"
ldr=5u
wdr=20u
VPP2
net19
net622
20u/5u
M66
VPP2
"pch"
ldr=5u
wdr=20u
net622
net10
Iref_tx2
20u/5u
M68
VPP2
"pch"
ldr=5u
wdr=20u
VPP2
net19
net618
20u/5u
M67
VPP2
"pch"
ldr=5u
wdr=20u
net618
net10
Iref_txbs
20u/5u
M64
VPP2
"pch"
ldr=5u
wdr=20u
VPP2
net19
net610
20u/5u
M69
VPP2
"pch"
ldr=5u
wdr=20u
net610
net10
Iref_vreg4

FIG. 615

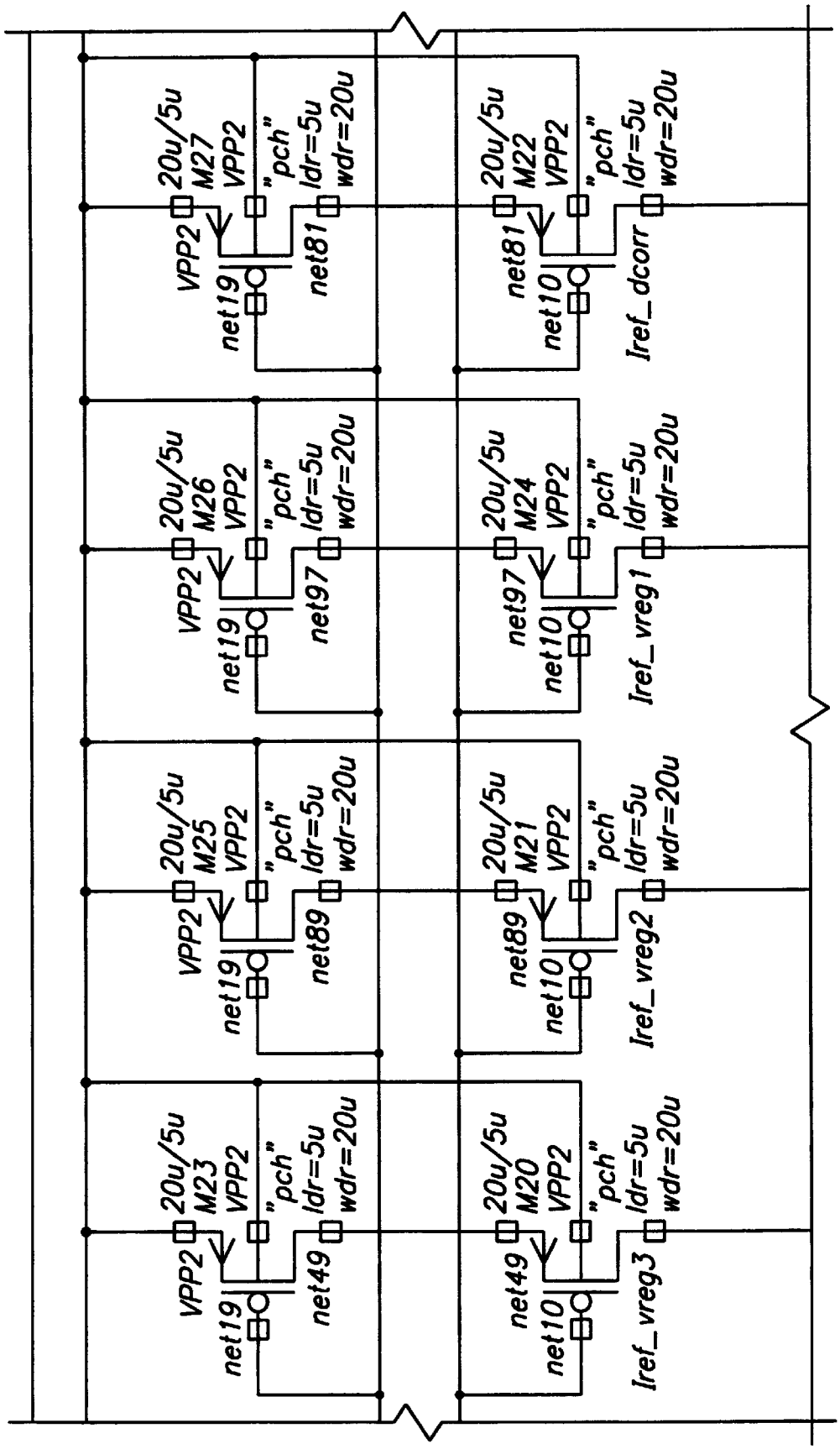


FIG. 69 DUMMY CELL

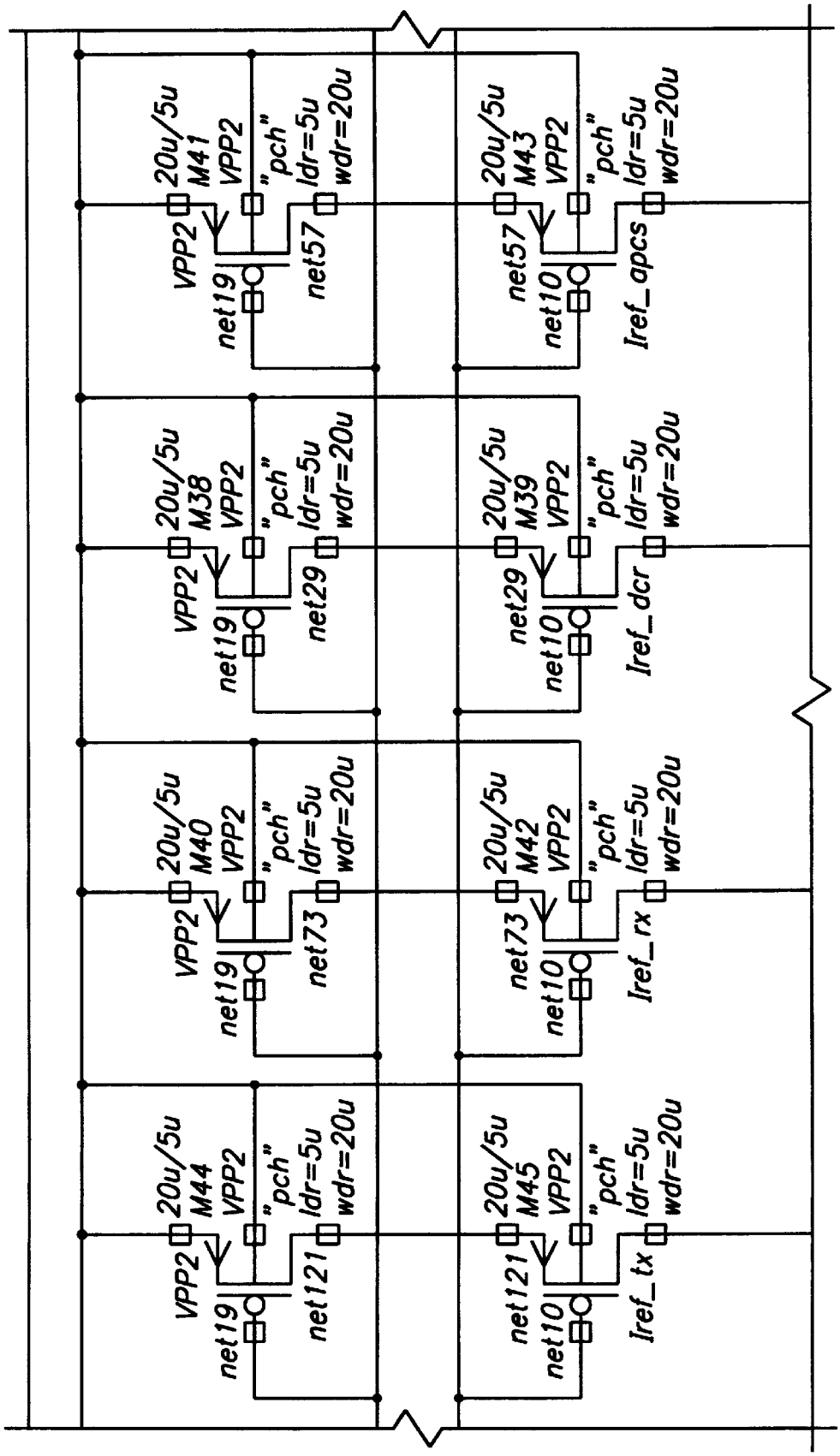
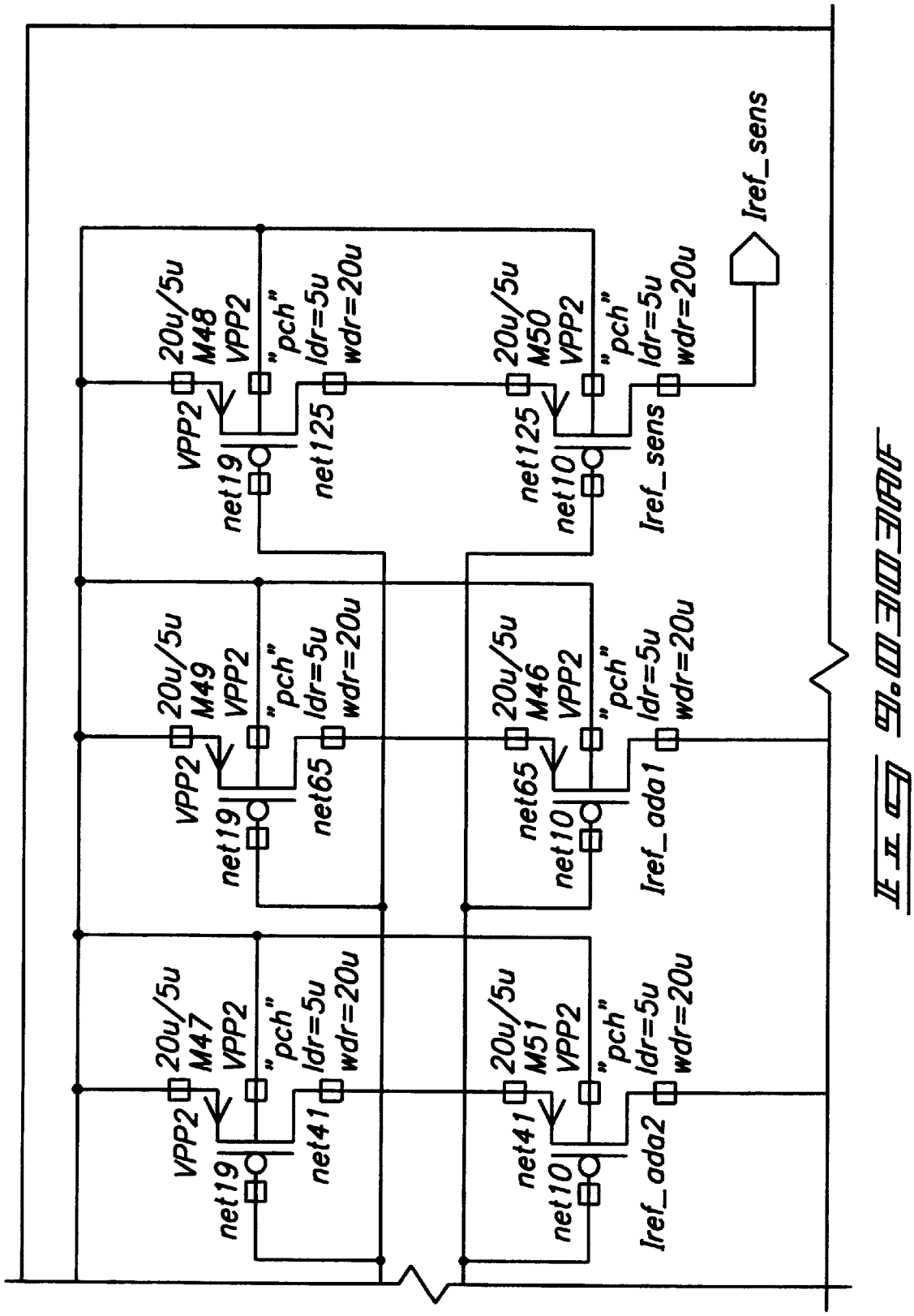
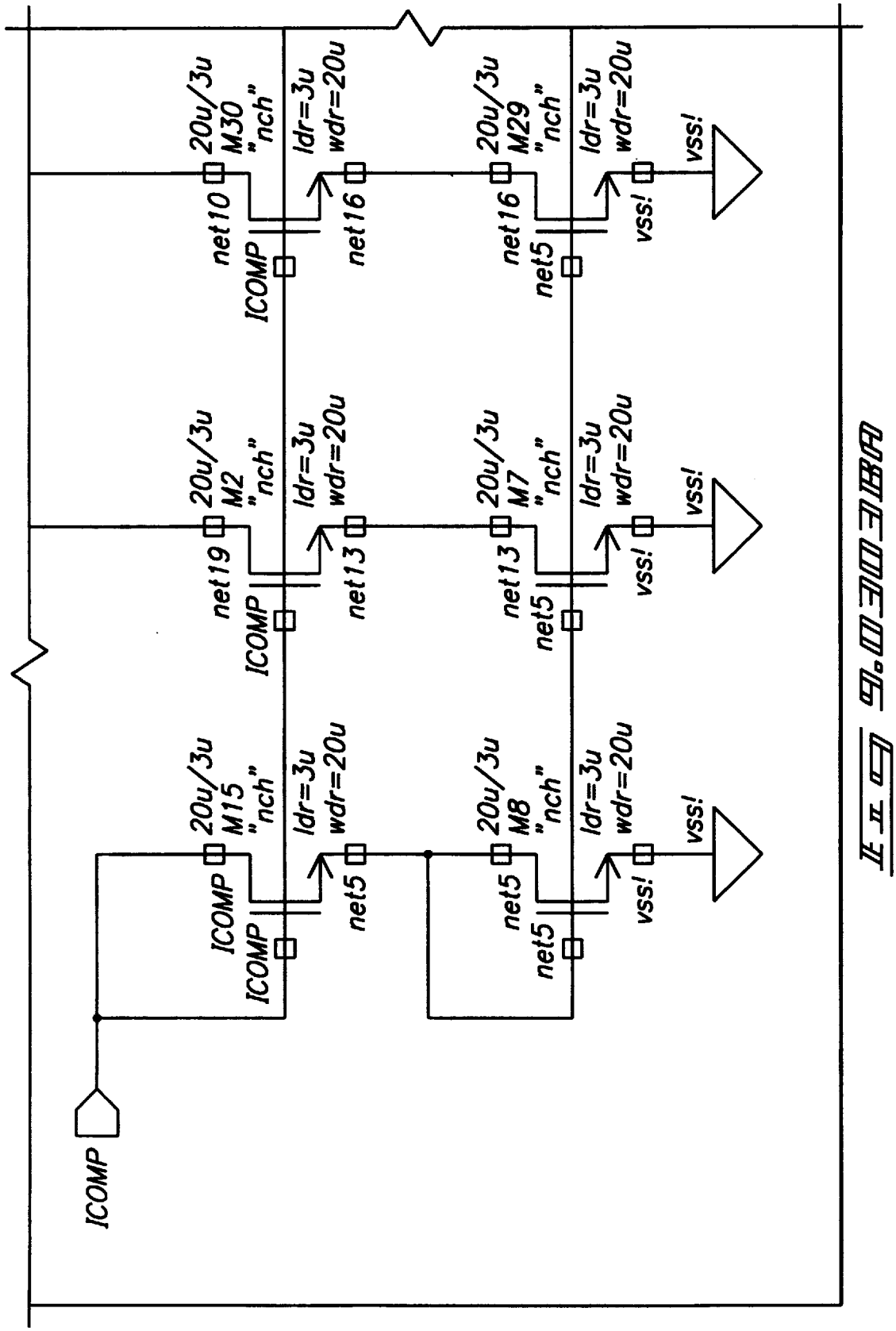

20u/5u M41 VPP2 "pch" ldr=5u wdr=20u
VPP2 net19 net57
20u/5u M43 VPP2 "pch" ldr=5u wdr=20u
net57 net10 Iref_apcs
20u/5u M38 VPP2 "pch" ldr=5u wdr=20u
VPP2 net19 net29
20u/5u M39 VPP2 "pch" ldr=5u wdr=20u
net29 net10 Iref_dcr
20u/5u M40 VPP2 "pch" ldr=5u wdr=20u
VPP2 net19 net73
20u/5u M42 VPP2 "pch" ldr=5u wdr=20u
net73 net10 Iref_rx
20u/5u M44 VPP2 "pch" ldr=5u wdr=20u
VPP2 net19 net121
20u/5u M45 VPP2 "pch" ldr=5u wdr=20u
net121 net10 Iref_tx

FIG. 95.0E3E


Iref_sens
20u/5u M48 VPP2 "pch" ldr=5u wdr=20u
20u/5u M50 VPP2 "pch" ldr=5u wdr=20u
20u/5u M49 VPP2 "pch" ldr=5u wdr=20u
20u/5u M46 VPP2 "pch" ldr=5u wdr=20u
20u/5u M47 VPP2 "pch" ldr=5u wdr=20u
20u/5u M51 VPP2 "pch" ldr=5u wdr=20u
VPP2
net19
net125
net10
Iref_sens
net65
Iref_ada1
net41
Iref_ada2


20u/3u
M30
"nch"
ldr=3u
wdr=20u
20u/3u
M29
"nch"
ldr=3u
wdr=20u
vss!
net10
ICOMP
net16
net16
net5
vss!
20u/3u
M2
"nch"
ldr=3u
wdr=20u
20u/3u
M7
"nch"
ldr=3u
wdr=20u
vss!
net19
ICOMP
net13
net13
net5
vss!
20u/3u
M15
"nch"
ldr=3u
wdr=20u
20u/3u
M8
"nch"
ldr=3u
wdr=20u
vss!
ICOMP
ICOMP
net5
net5
net5
vss!
ICOMP
GATE OUTPUT

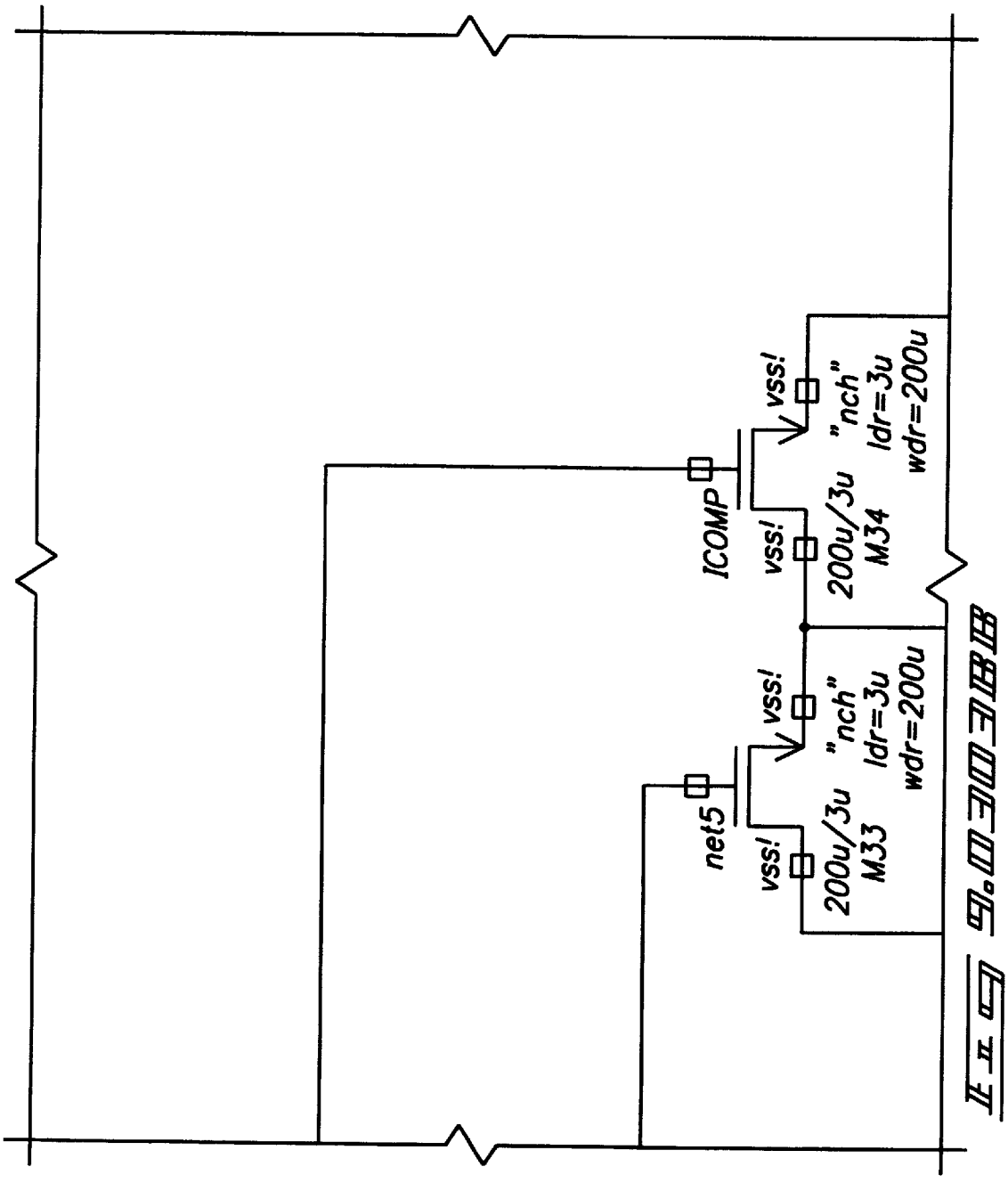
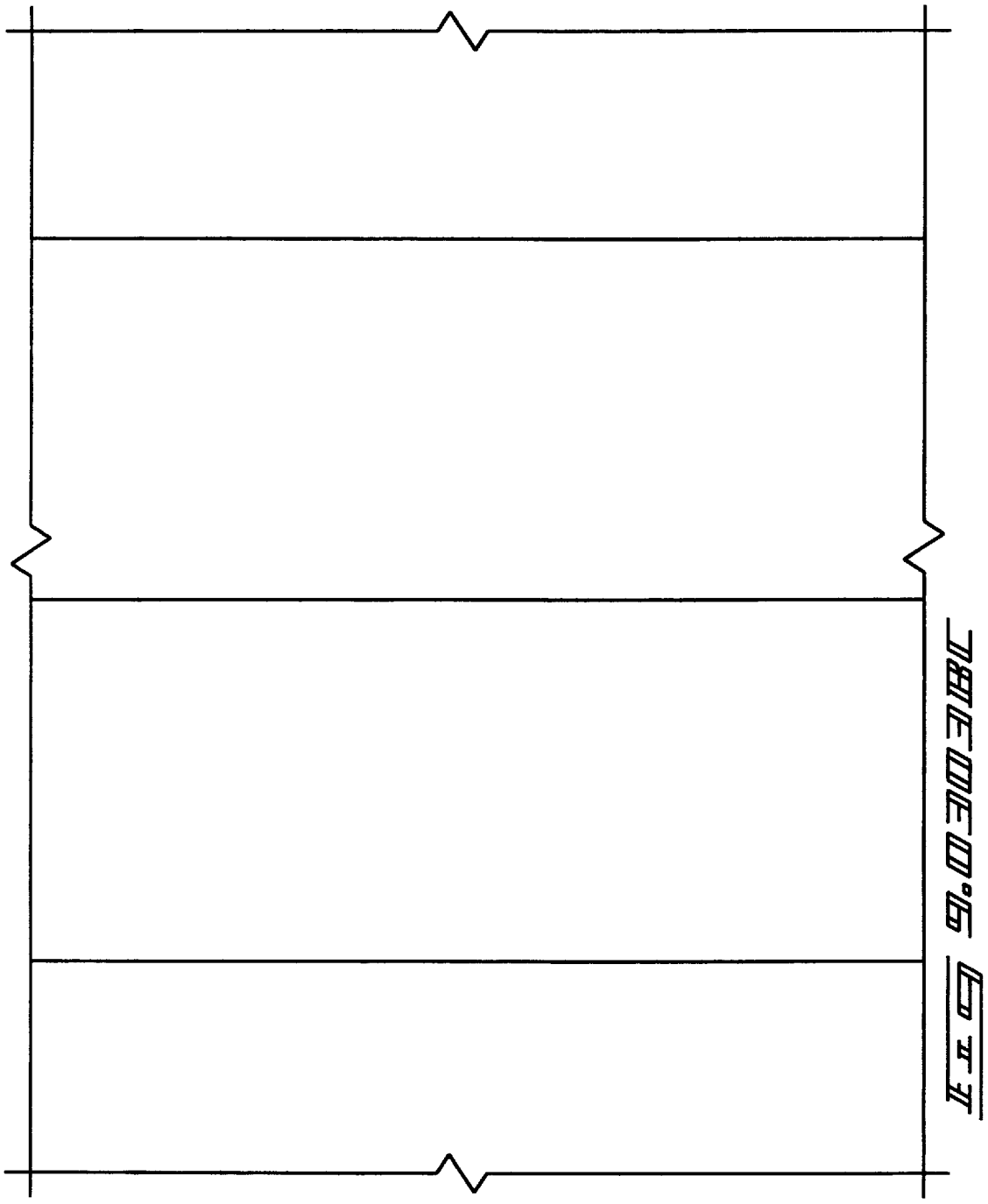

vss!
"nch"
ldr=3u
wdr=200u
ICOMP
vss!
200u/3u
M34
vss!
"nch"
ldr=3u
wdr=200u
net5
vss!
200u/3u
M33

FIG 6E



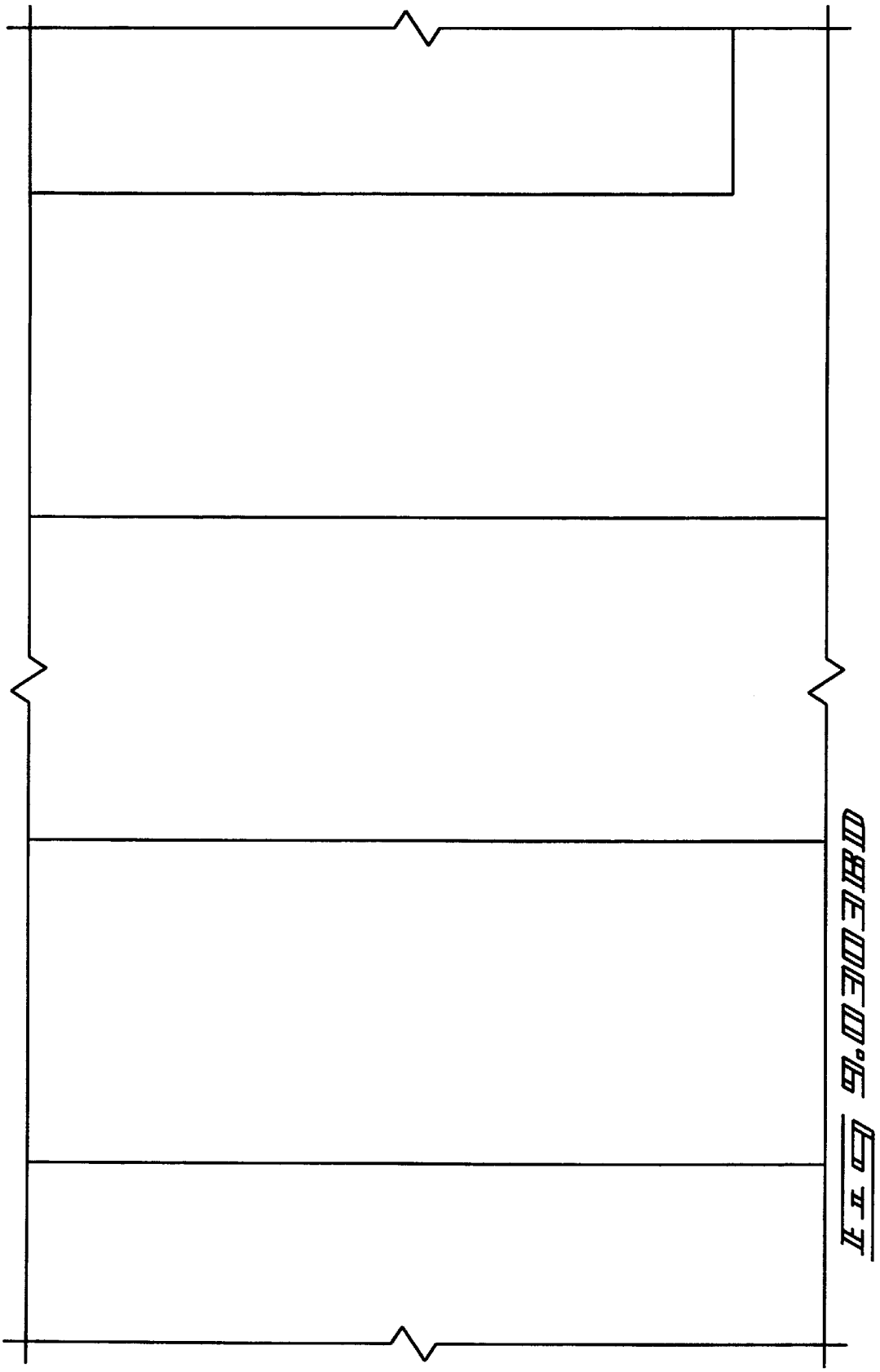


FIG. 5,060,000

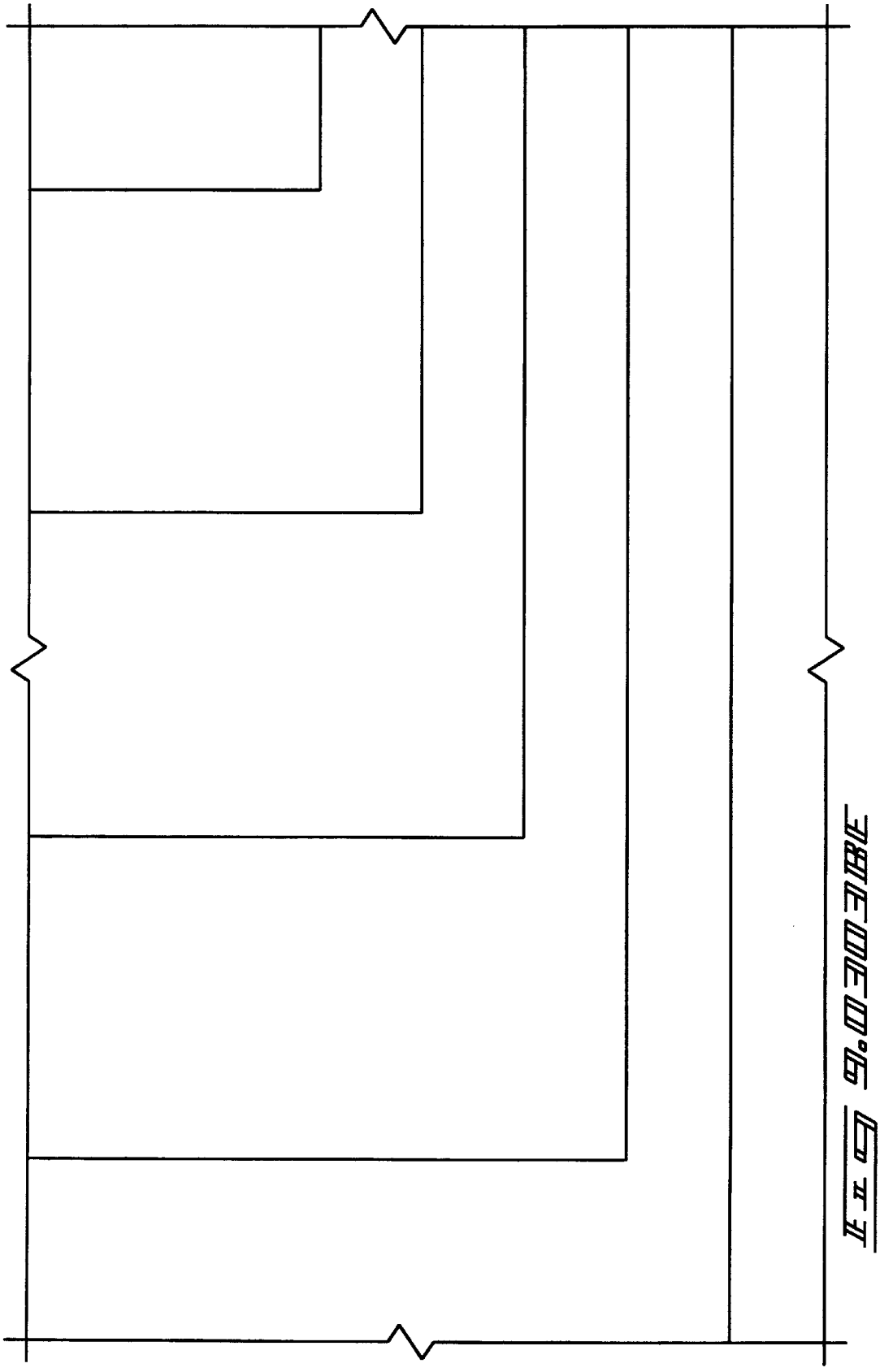
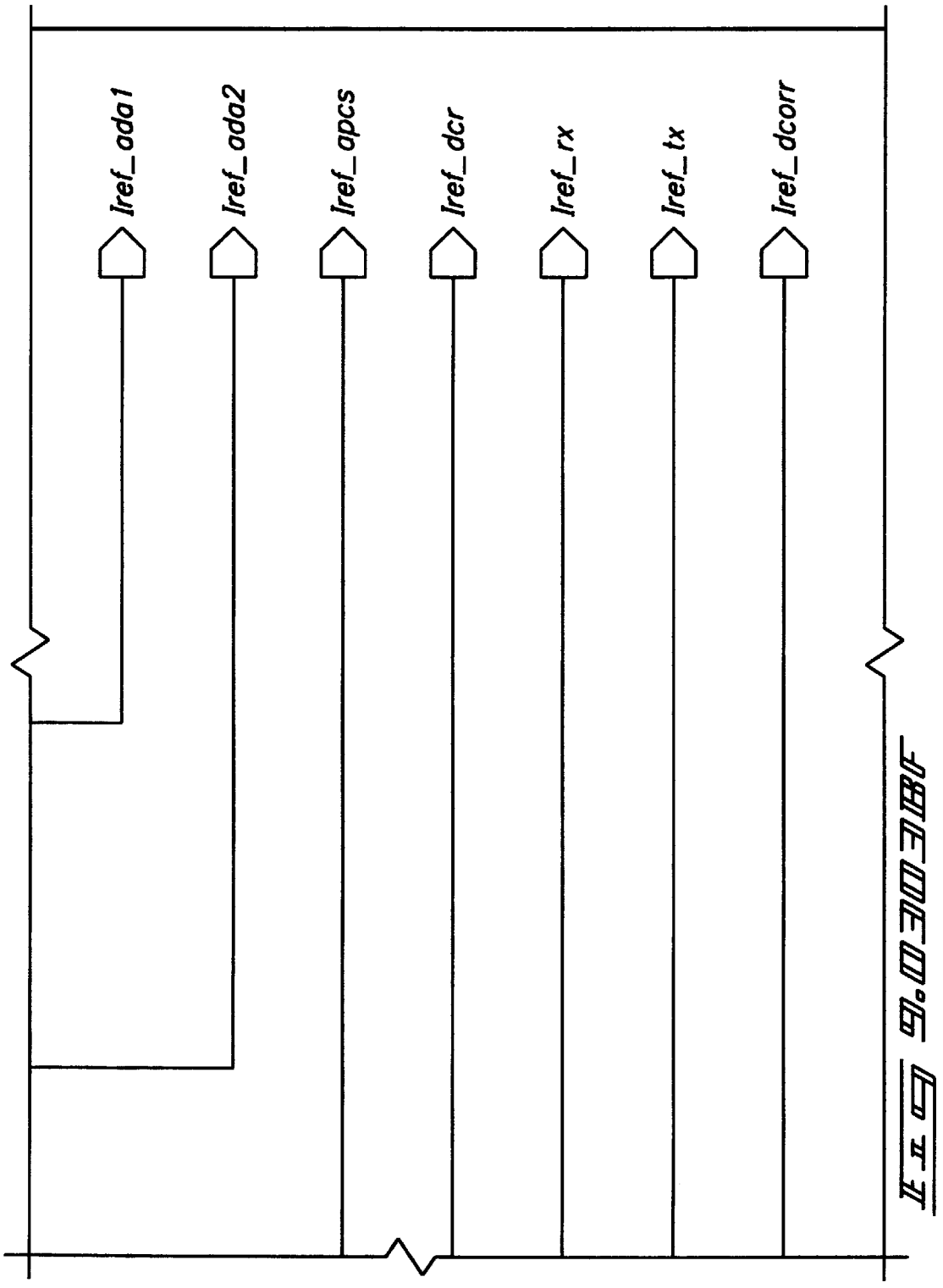


FIG. 96.0E+06


Iref_ada1
Iref_ada2
Iref_apcs
Iref_dcr
Iref_rx
Iref_tx
Iref_dcorr

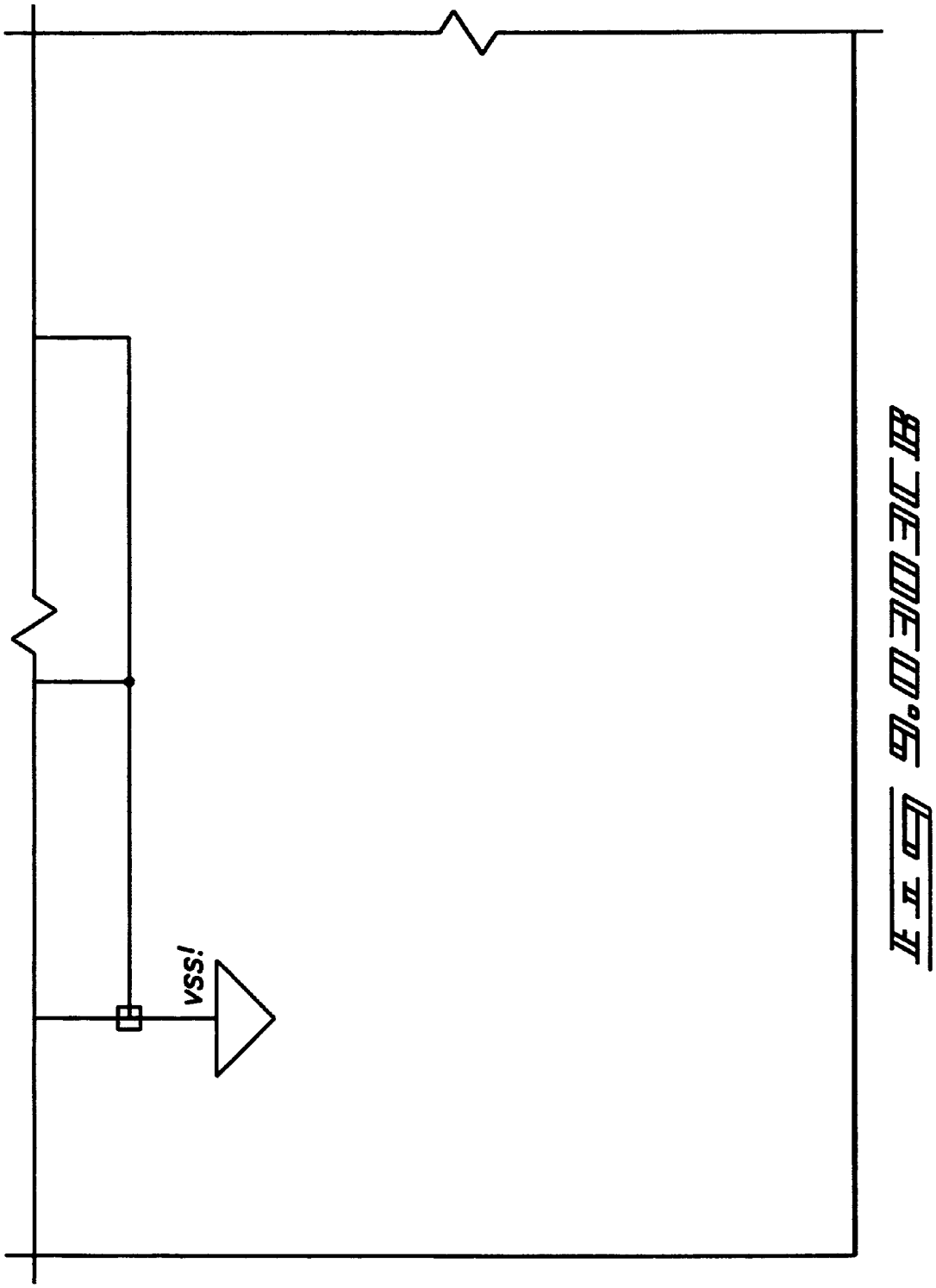


FIG 96,603

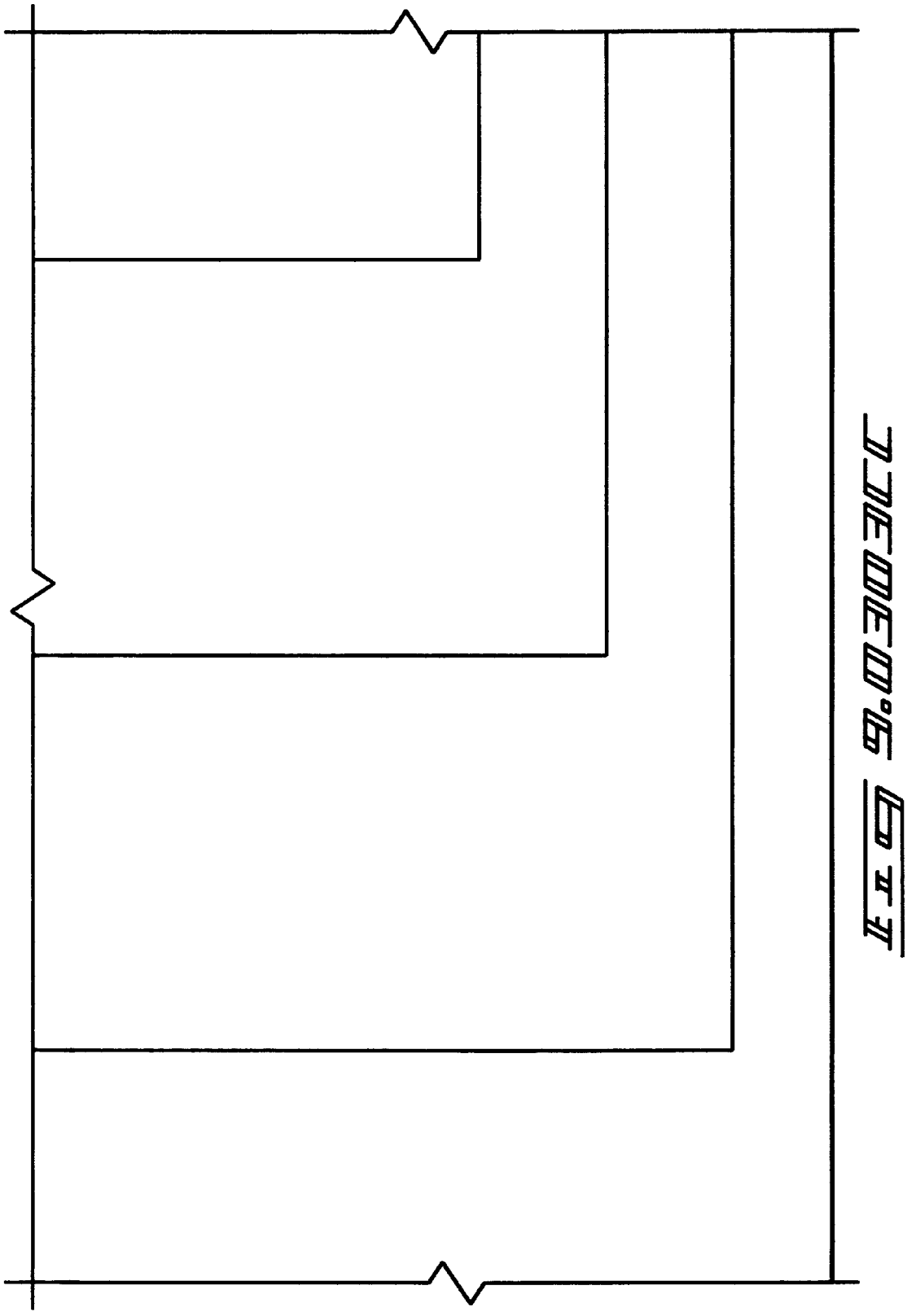
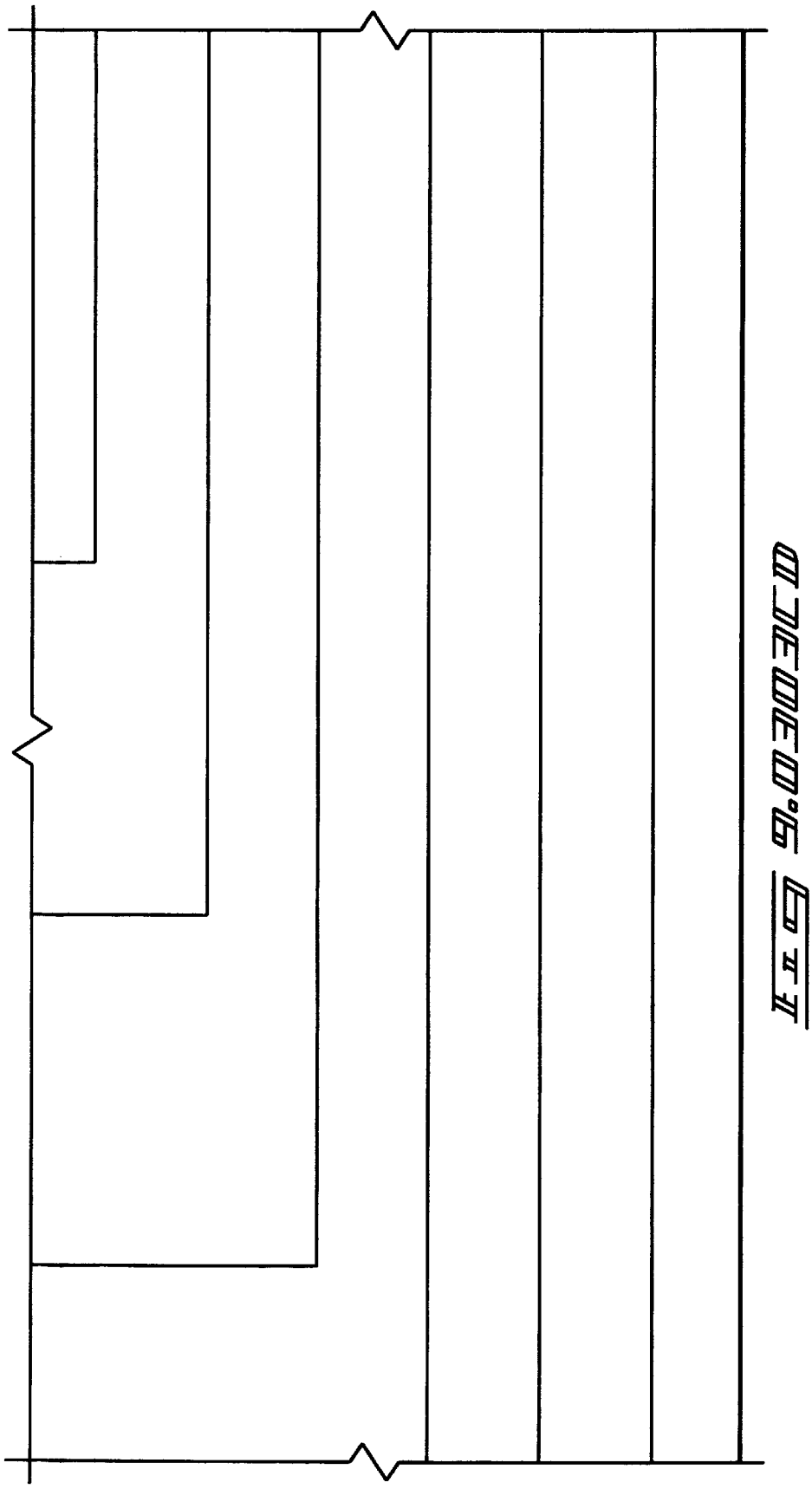


FIG. 96E



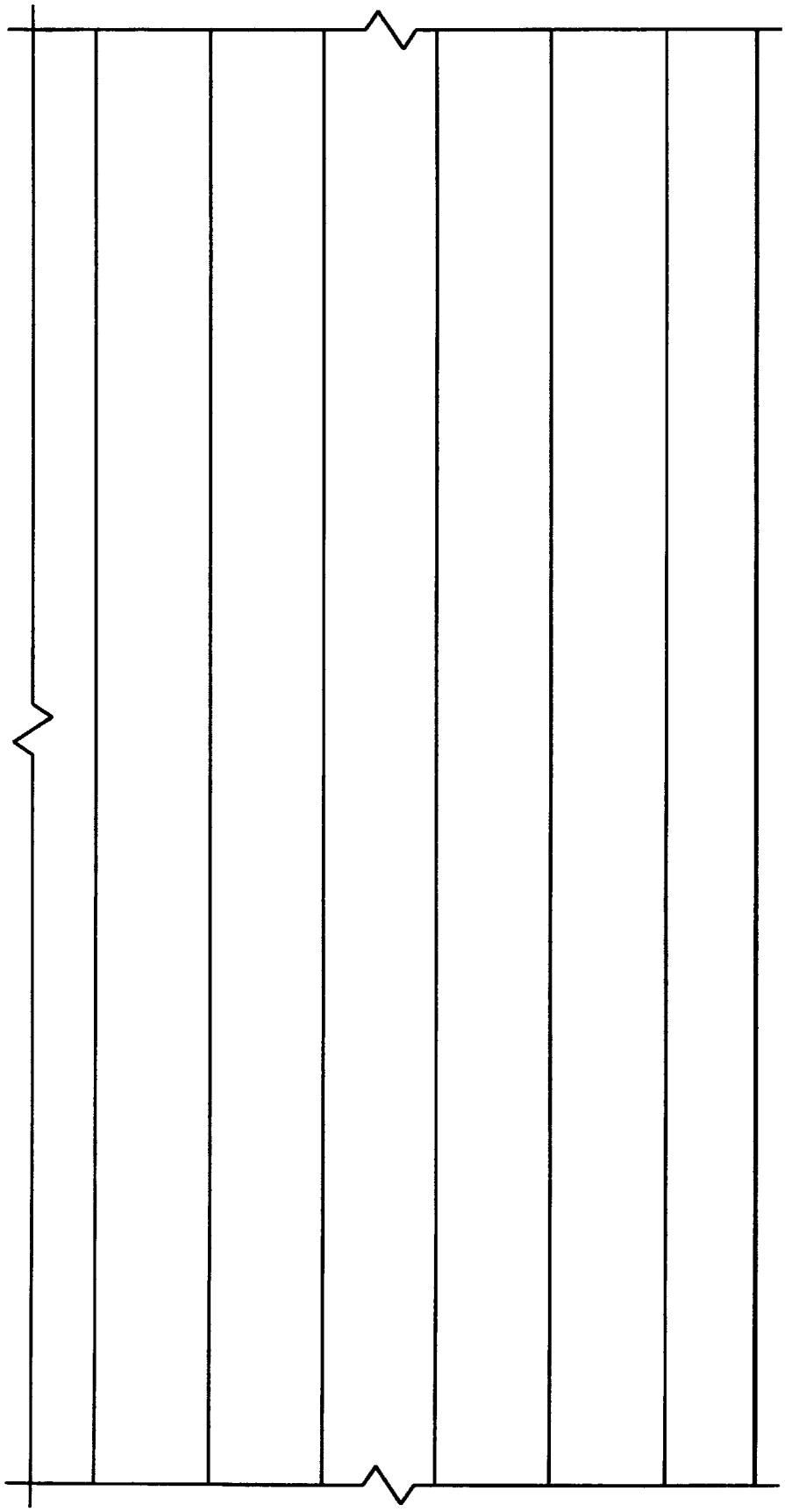


FIG 96,600

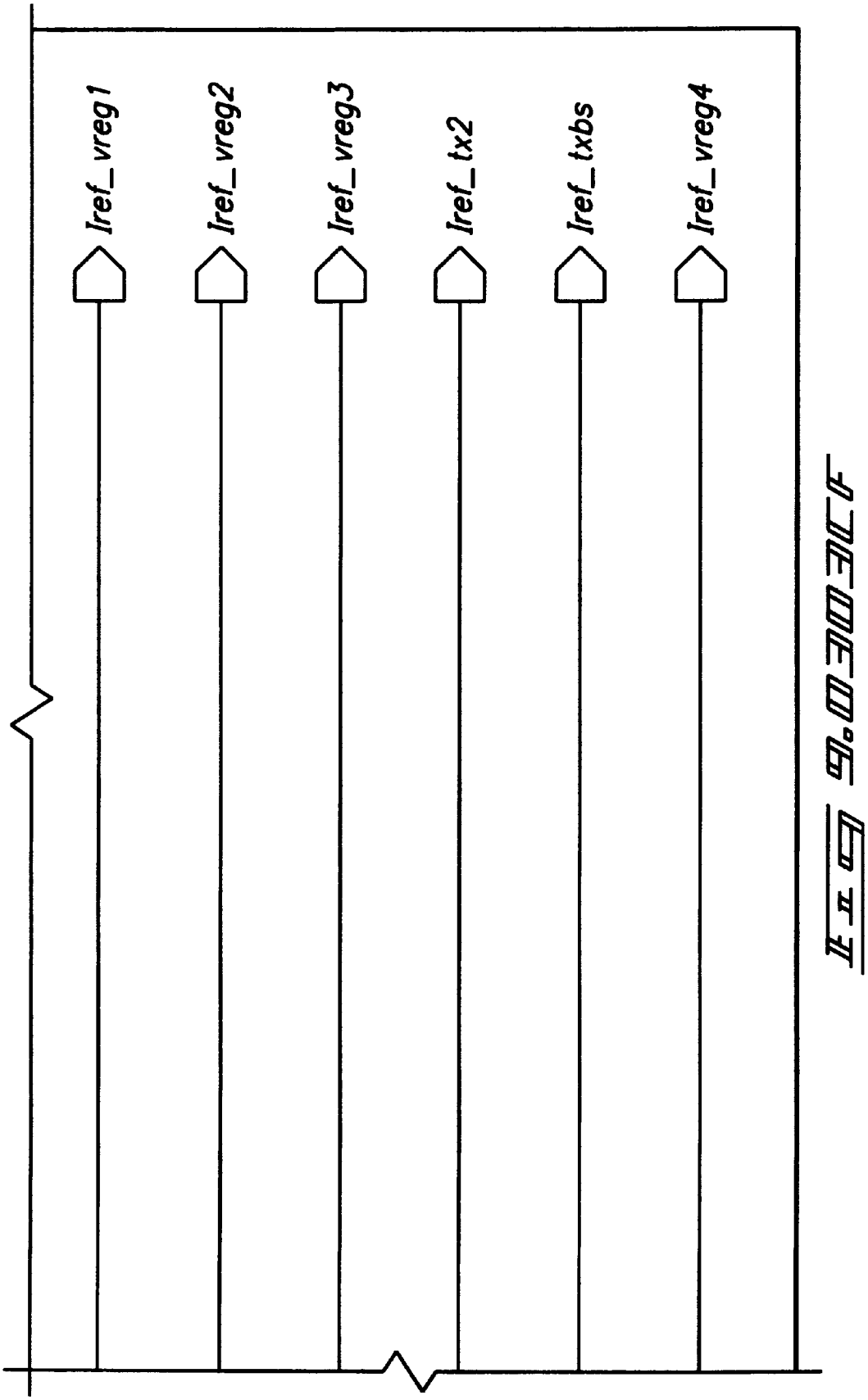

Iref_vreg1
Iref_vreg2
Iref_vreg3
Iref_tx2
Iref_txbs
Iref_vreg4

FIG 6b

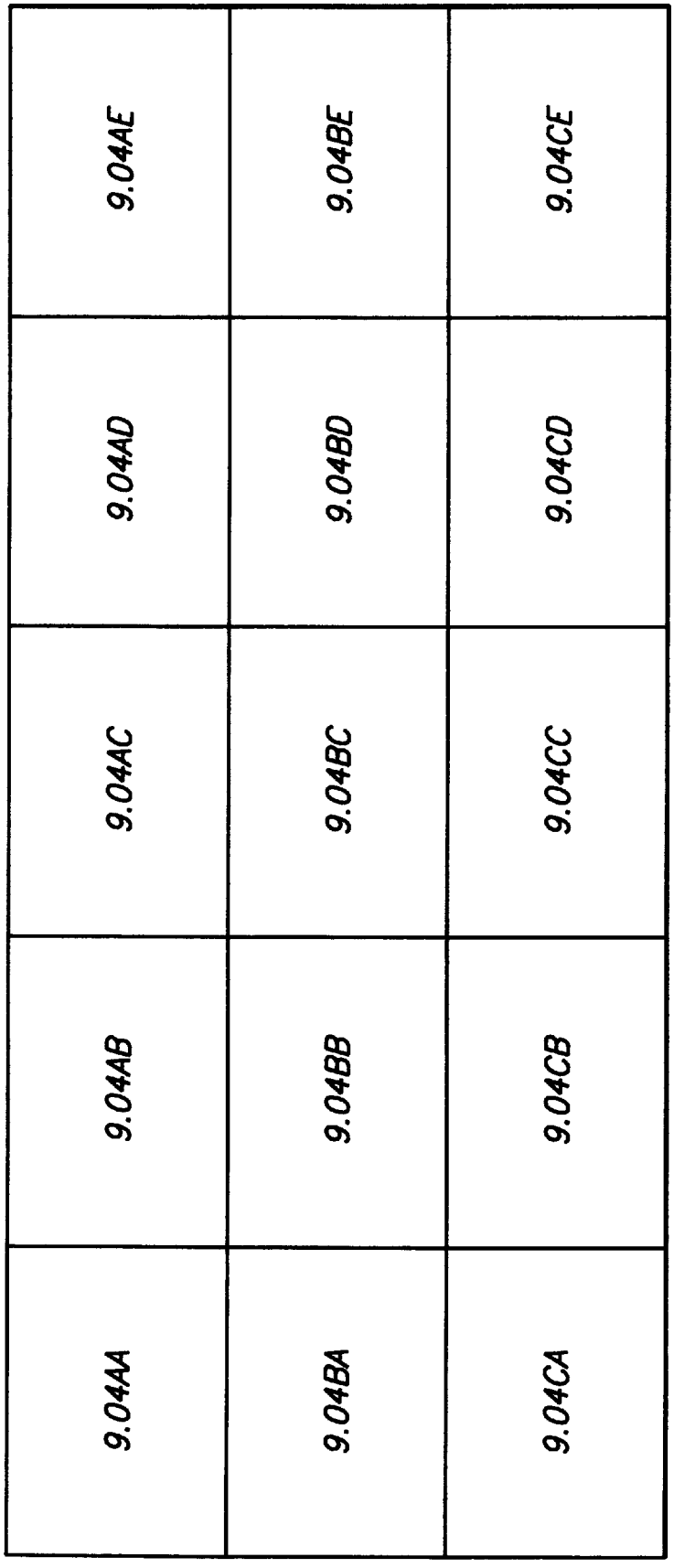
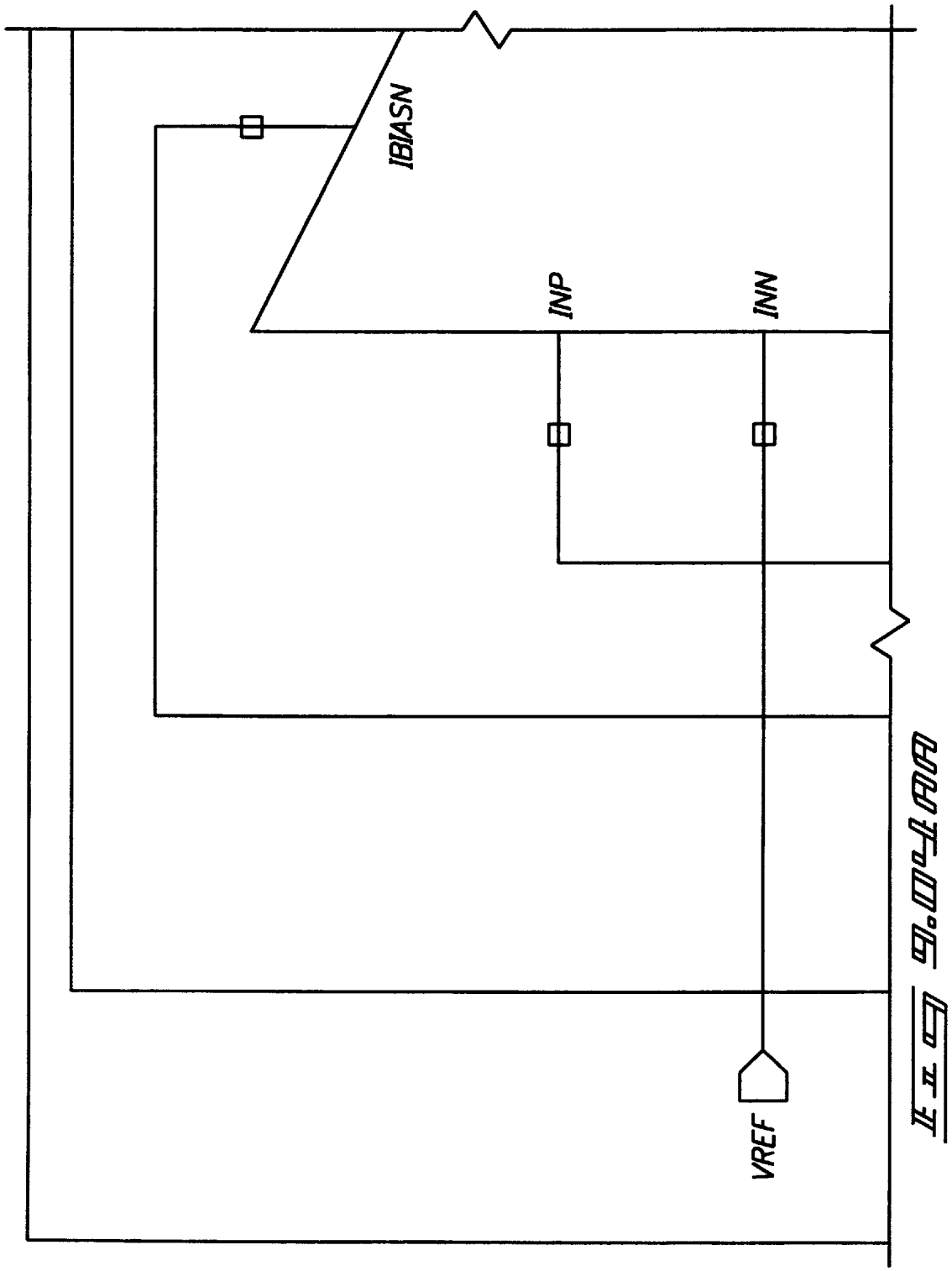
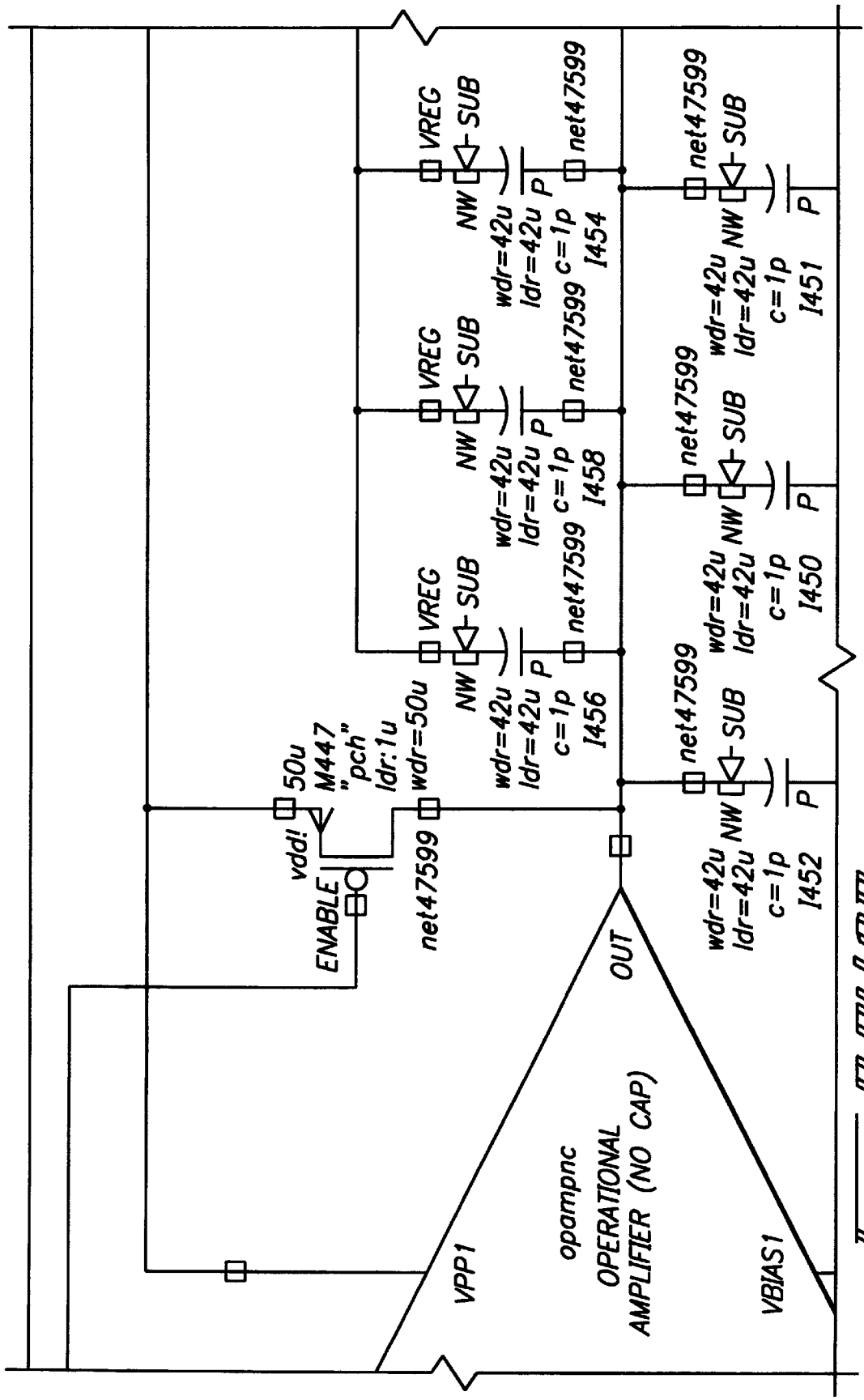

9.04AE
9.04BE
9.04CE
9.04AD
9.04BD
9.04CD
9.04AC
9.04BC
9.04CC
9.04AB
9.04BB
9.04CB
9.04AA
9.04BA
9.04CA

FIG. 9.04E


IBIASN
INP
INN
VREF
AV=100 GB=11 MHz


VREG
SUB
NW
P
net47599
wdr=42u
ldr=42u
c=1p
I454
I451
I458
I450
I456
I452
50u
M447
"pch"
ldr:1u
wdr=50u
vdd!
ENABLE
OUT
VPP1
VBIAS1
opampnc
OPERATIONAL
AMPLIFIER (NO CAP)

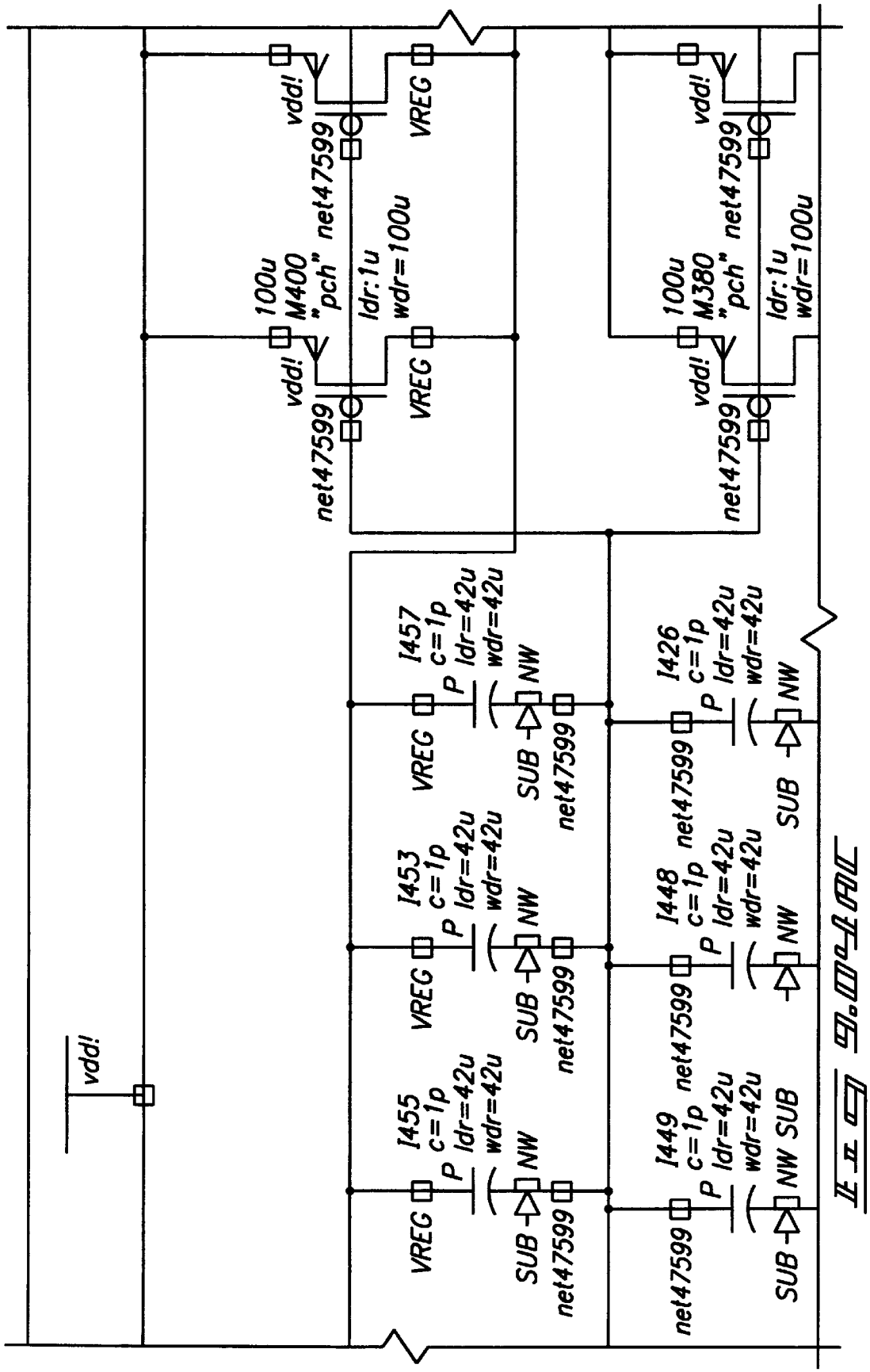

vdd!
VREG
net47599
100u
M400
"pch"
ldr:1u
wdr=100u
M380
I457
I453
I455
I426
I448
I449
c=1p
ldr=42u
wdr=42u
P
NW
SUB

FIG. 2550

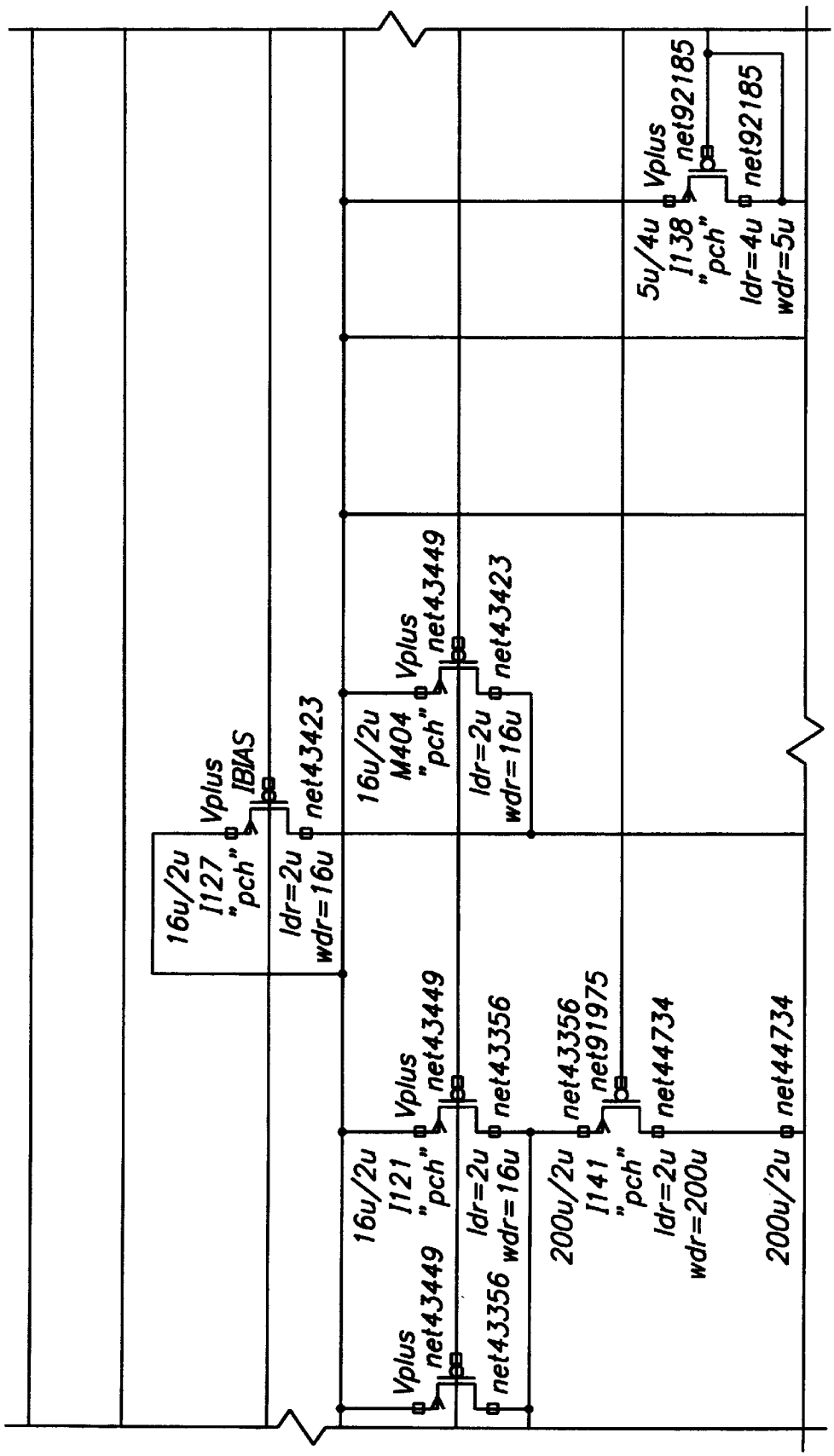

16u/2u
I127
"pch"
ldr=2u
wdr=16u
Vplus
IBIAS
net43423
16u/2u
M404
"pch"
ldr=2u
wdr=16u
Vplus
net43449
net43423
5u/4u
I138
"pch"
ldr=4u
wdr=5u
Vplus
net92185
net92185
16u/2u
I121
"pch"
ldr=2u
wdr=16u
Vplus
net43449
net43356
200u/2u
I141
"pch"
ldr=2u
wdr=200u
net43356
net91975
net44734
200u/2u
net44734
Vplus
net43449
net43356

FIG. 9.0111AM

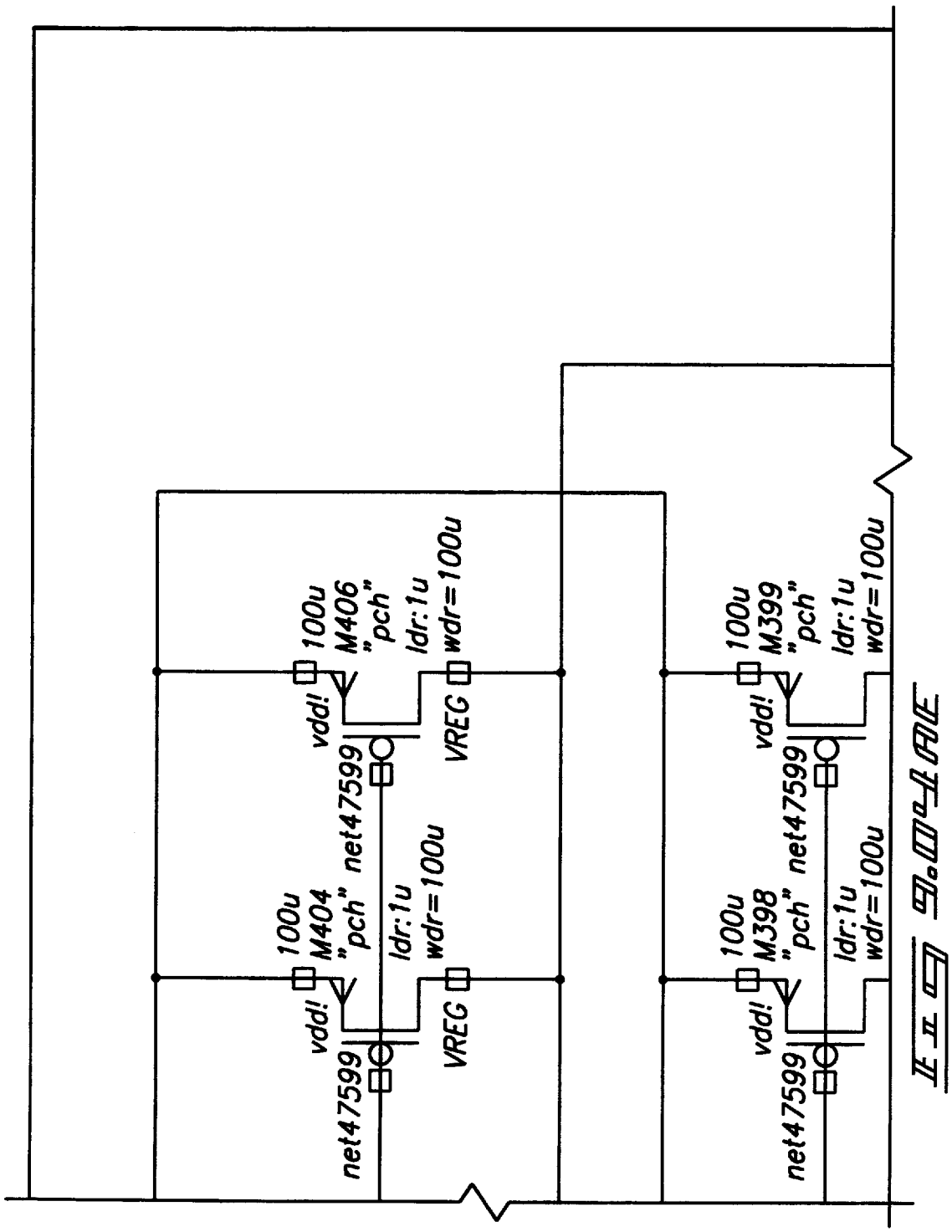
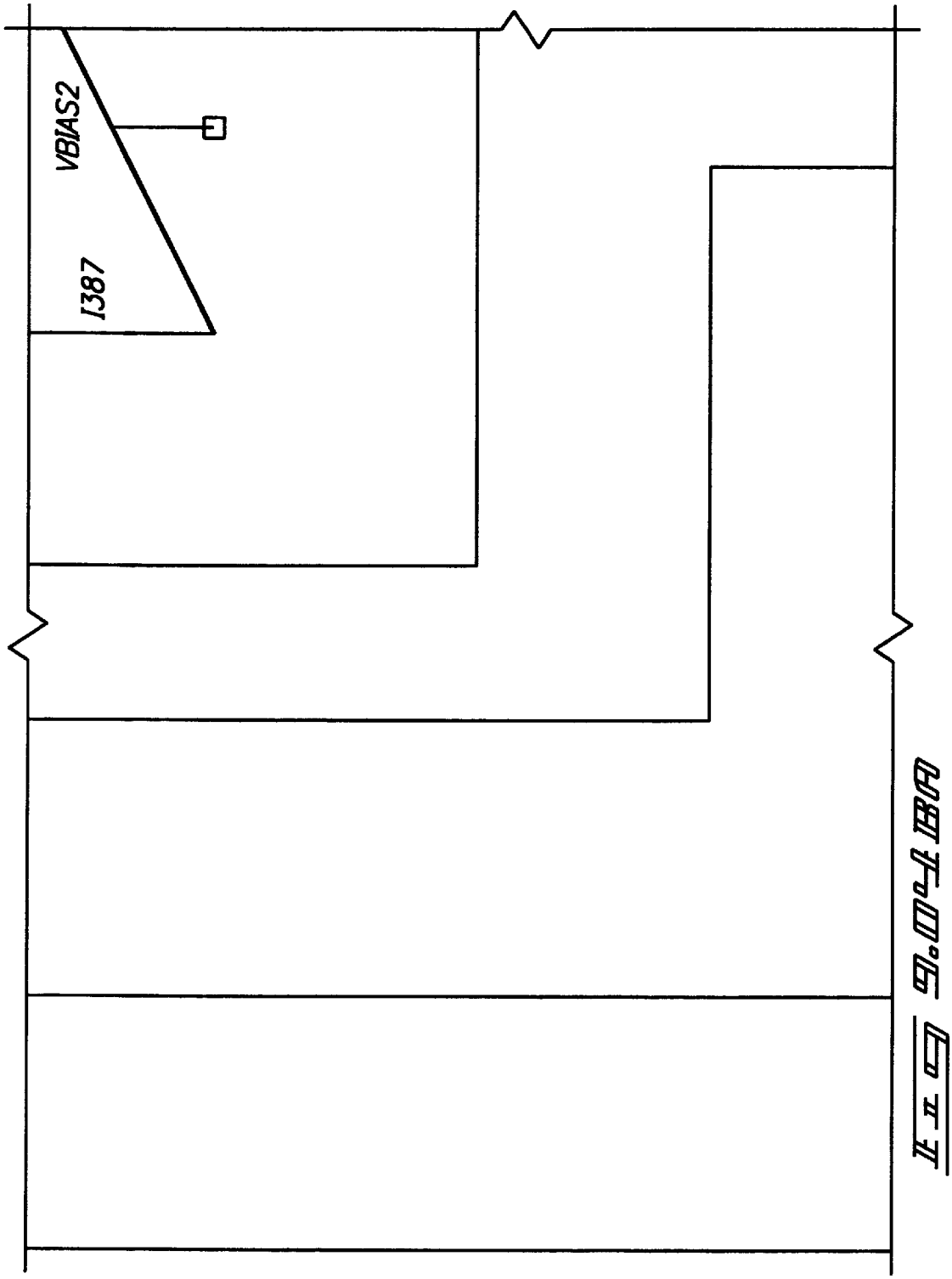
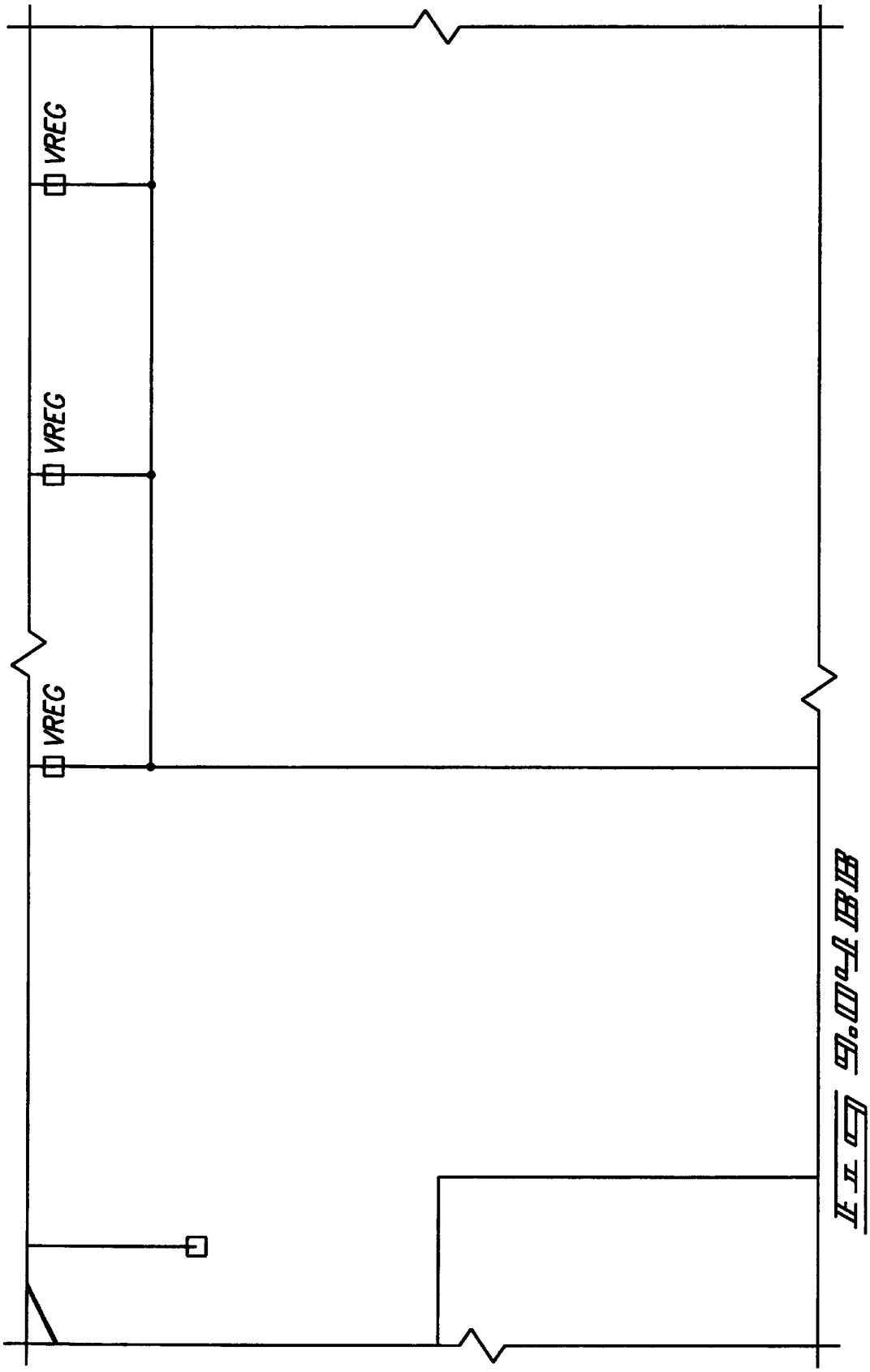
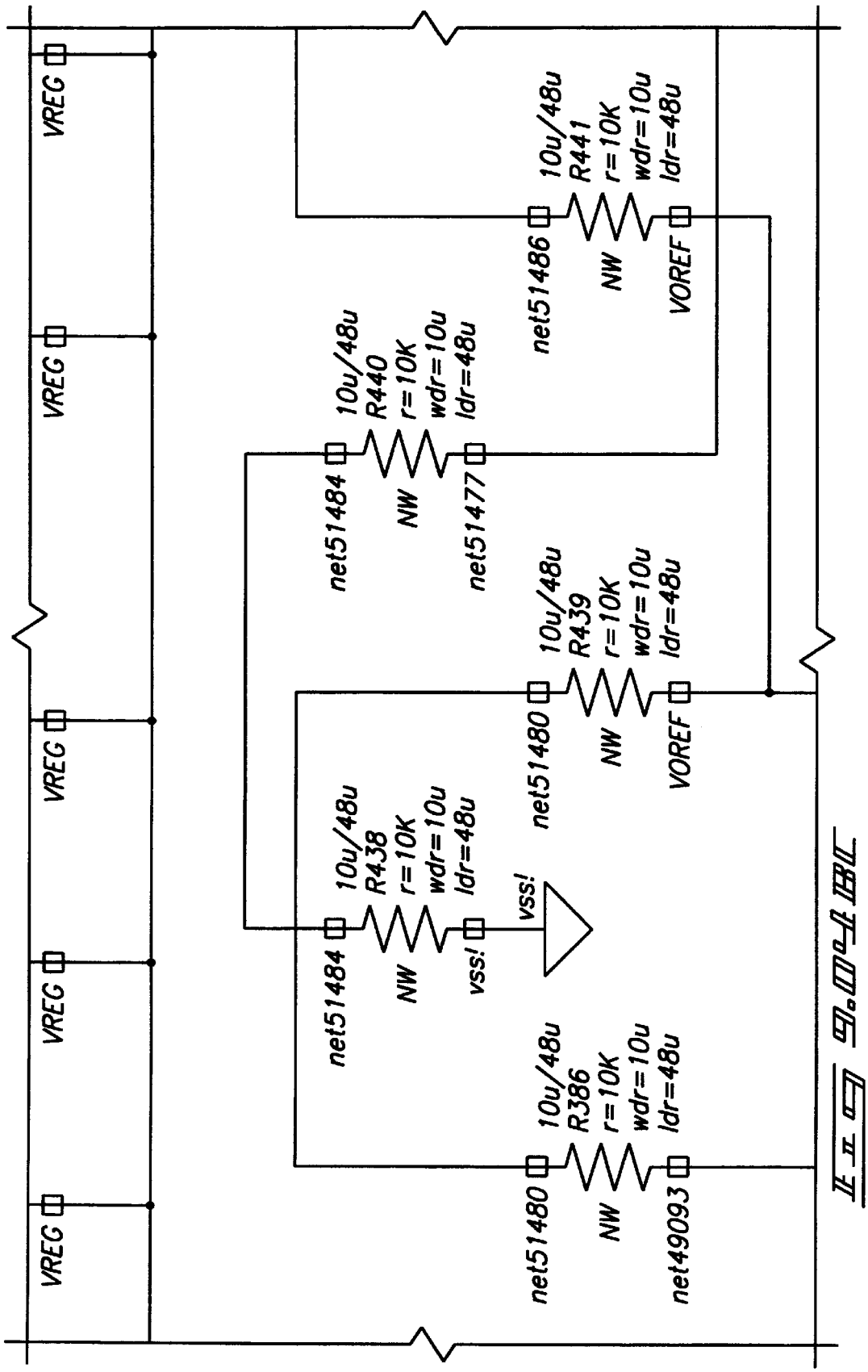

100u
M406
"pch"
ldr:1u
wdr=100u
vdd!
VREG
net47599
100u
M404
"pch"
ldr:1u
wdr=100u
vdd!
VREG
net47599
100u
M399
"pch"
ldr:1u
wdr=100u
vdd!
net47599
100u
M398
"pch"
ldr:1u
wdr=100u
vdd!
net47599

FIG. 90.0144E


VBIAS2
I387
FIG 96


VREG
VREG
VREG


VREG
VREG
VREG
VREG
VREG
10u/48u
R441
r=10K
wdr=10u
ldr=48u
net51486
NW
VOREF
10u/48u
R440
r=10K
wdr=10u
ldr=48u
net51484
NW
net51477
10u/48u
R439
r=10K
wdr=10u
ldr=48u
net51480
NW
VOREF
10u/48u
R438
r=10K
wdr=10u
ldr=48u
net51484
NW
vss!
vss!
10u/48u
R386
r=10K
wdr=10u
ldr=48u
net51480
NW
net49093

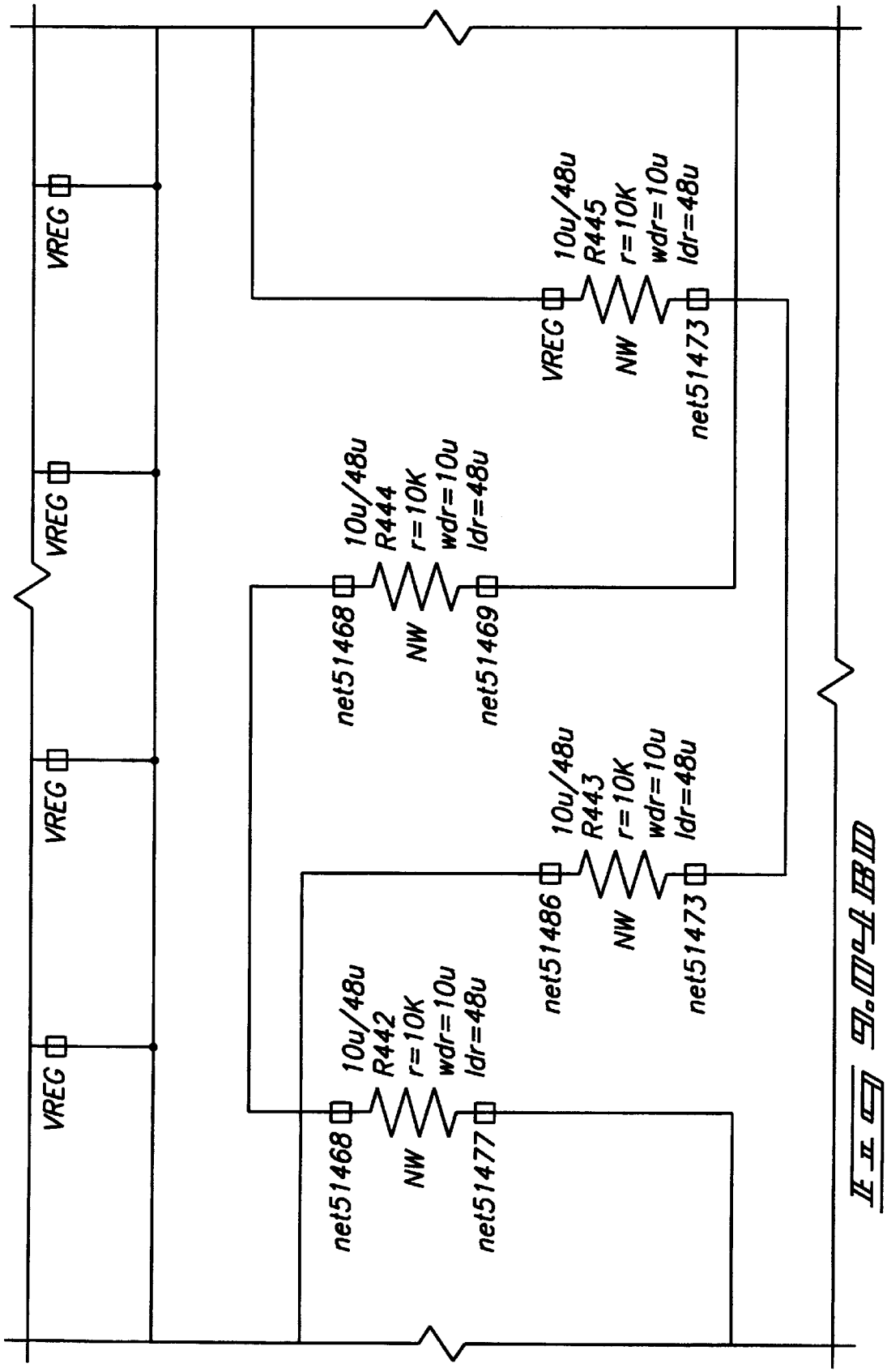

VREG
VREG
VREG
VREG
10u/48u
R445
r=10K
wdr=10u
ldr=48u
VREG
NW
net51473
10u/48u
R444
r=10K
wdr=10u
ldr=48u
net51468
NW
net51469
10u/48u
R443
r=10K
wdr=10u
ldr=48u
net51486
NW
net51473
10u/48u
R442
r=10K
wdr=10u
ldr=48u
net51468
NW
net51477

FIG. 6,004

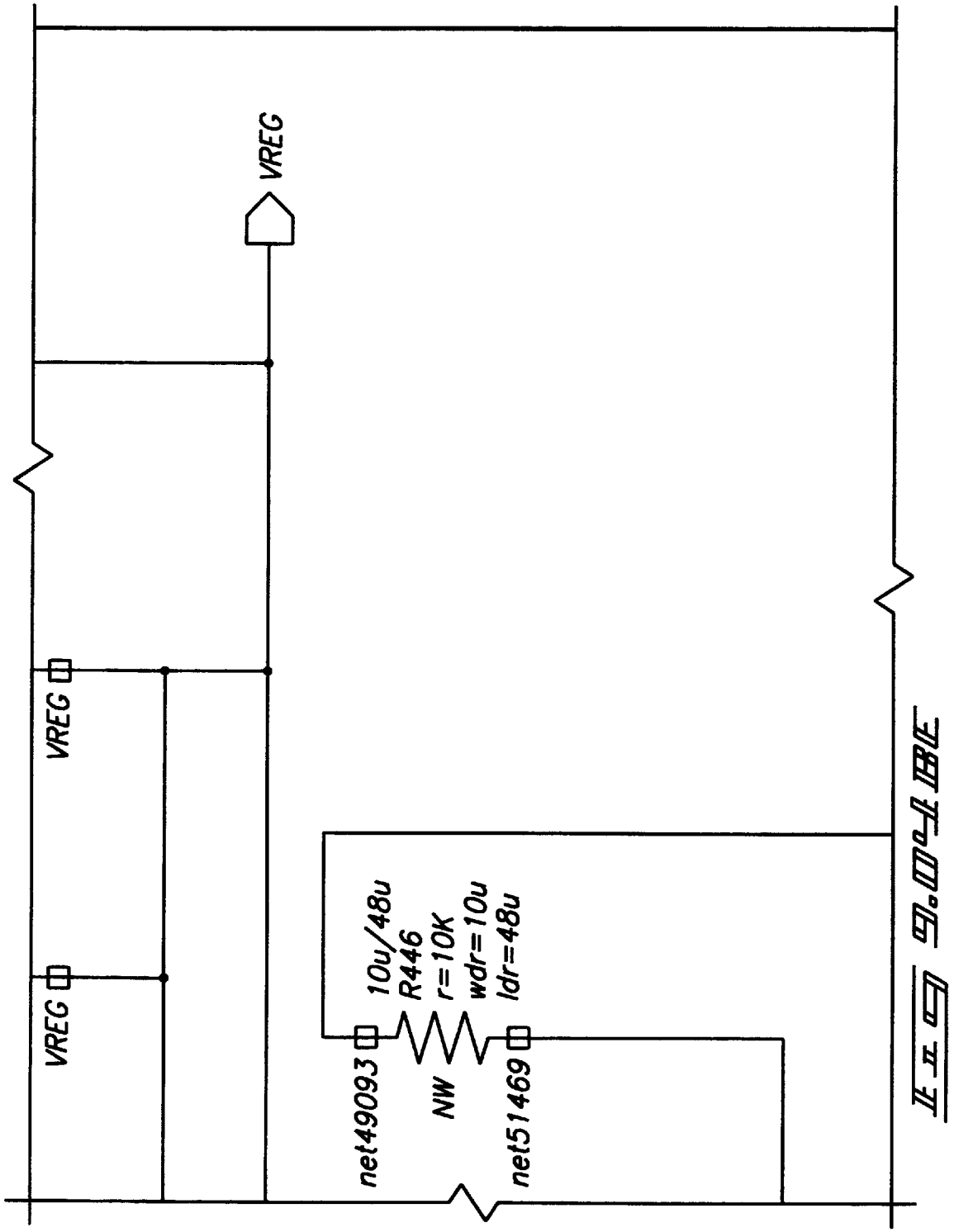

VREG
VREG
VREG
10u/48u
R446
r=10K
wdr=10u
ldr=48u
net49093
NW
net51469

FIG. 2557

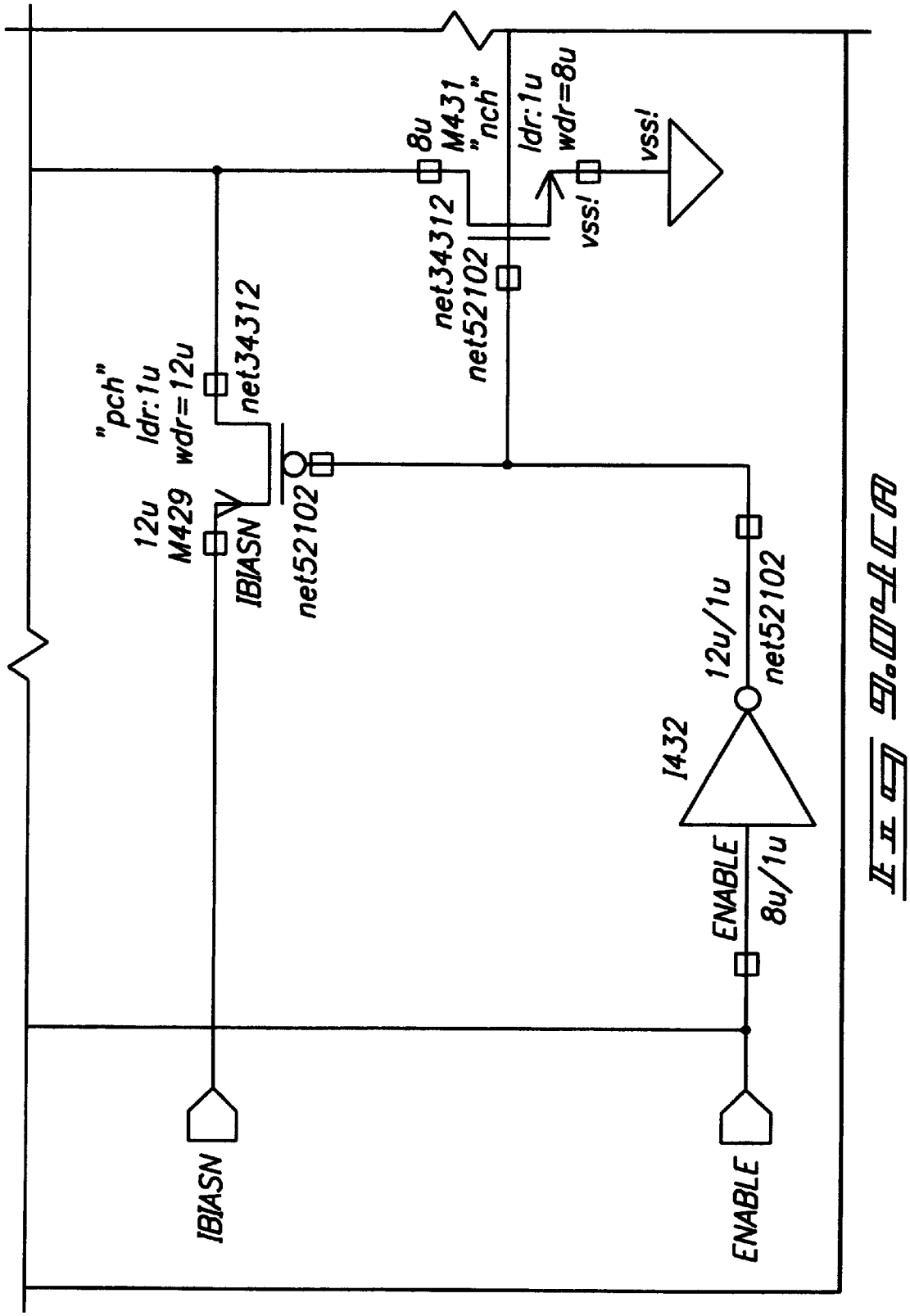

8u
M431
"nch"
ldr:1u
wdr=8u
vss!
net34312
net52102
vss!
"pch"
ldr:1u
wdr=12u
net34312
12u
M429
IBIASN
net52102
12u/1u
net52102
I432
ENABLE
8u/1u
IBIASN
ENABLE

FIG 9.00F31

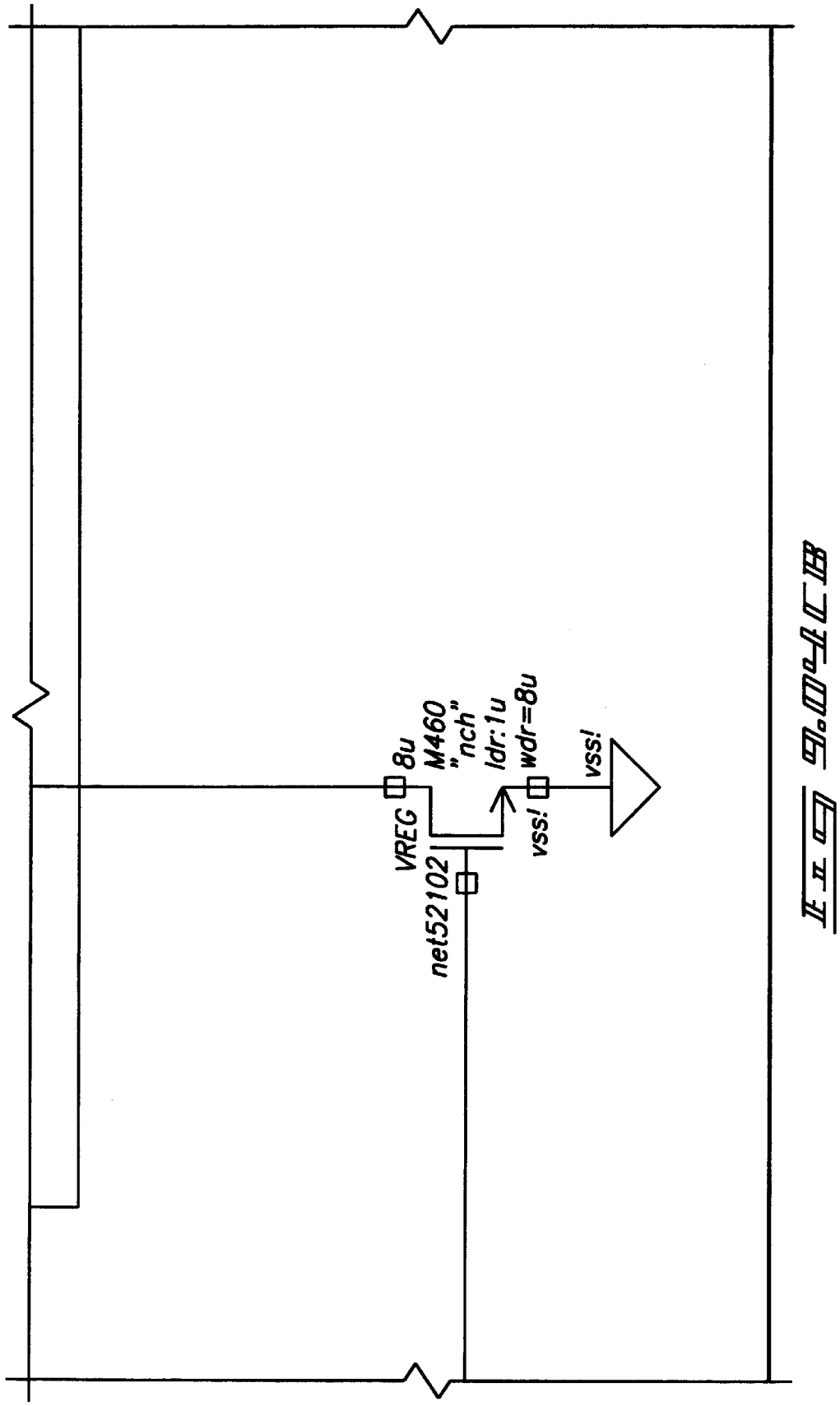


FIG 59.004

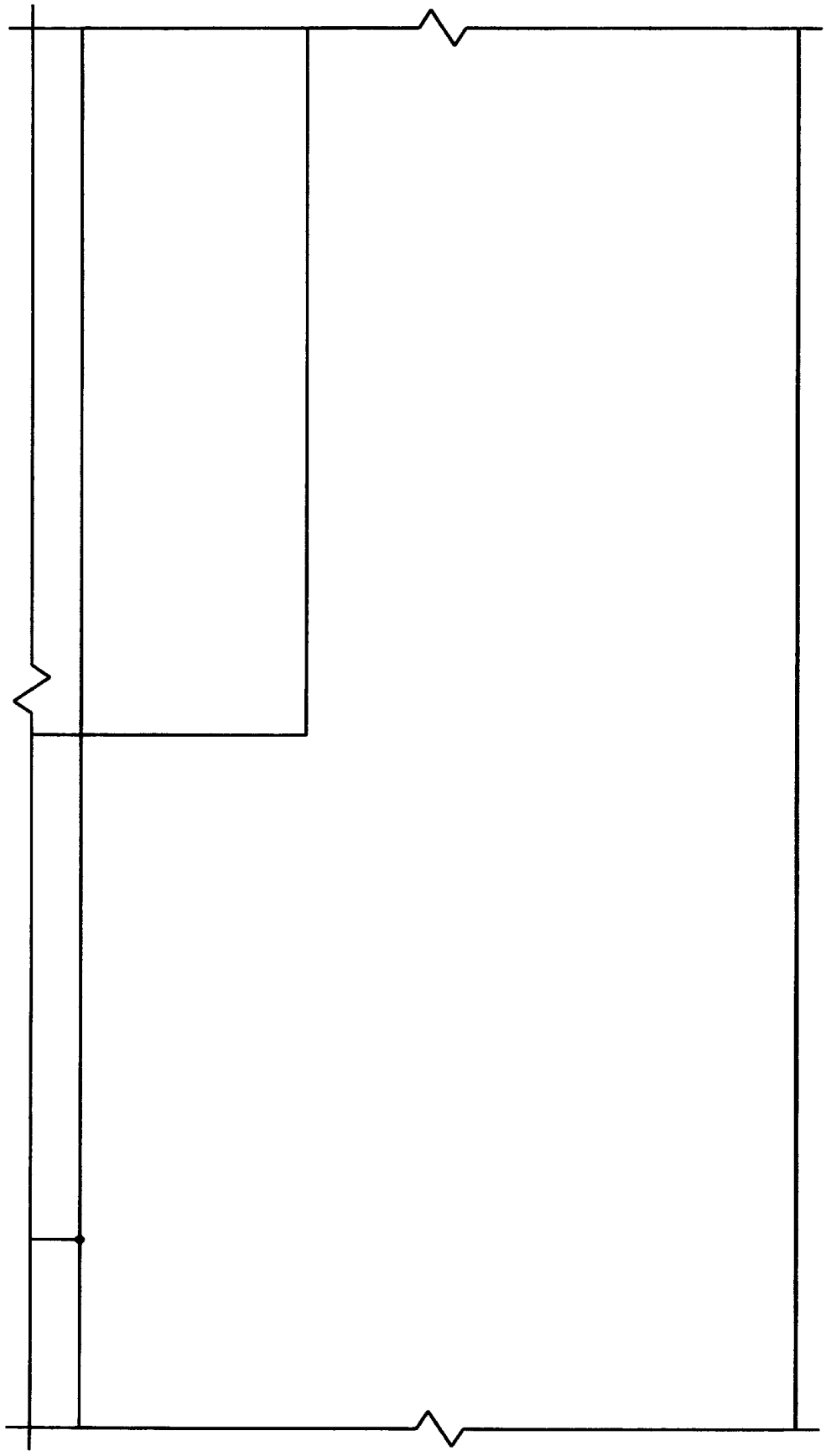


FIG 9,047C

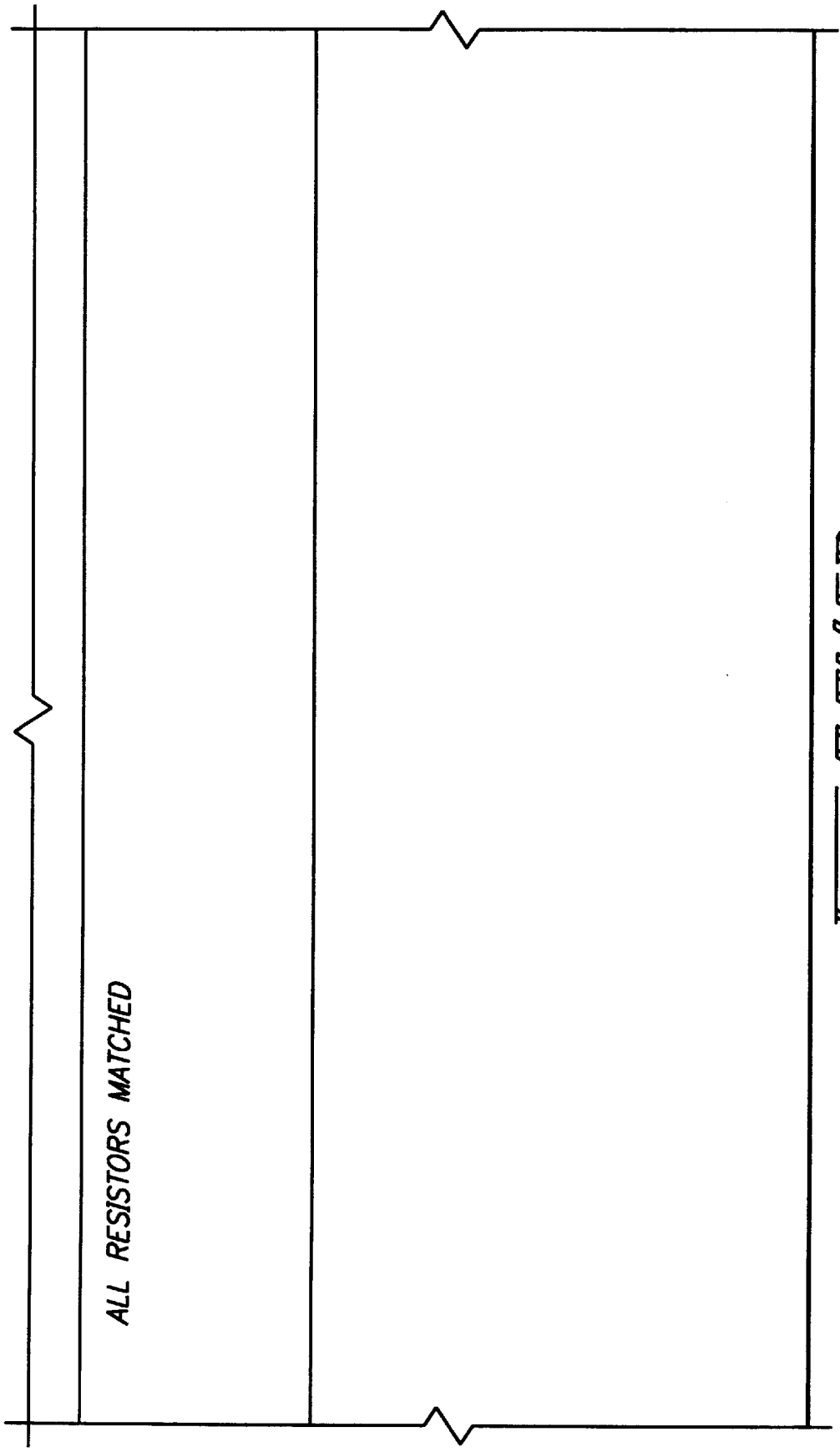
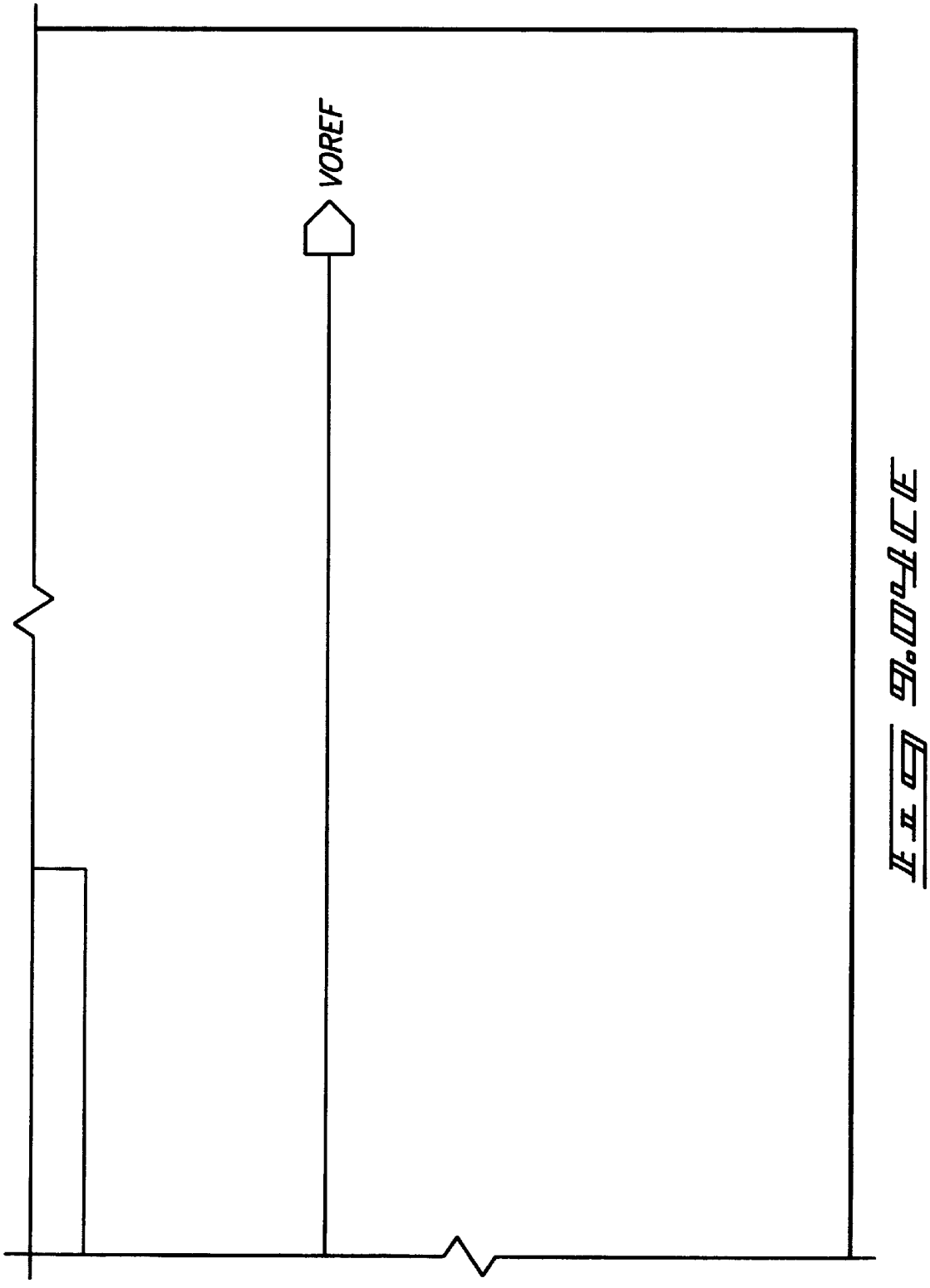


Fig 9,047D


VOREF
FIG 90.0475E

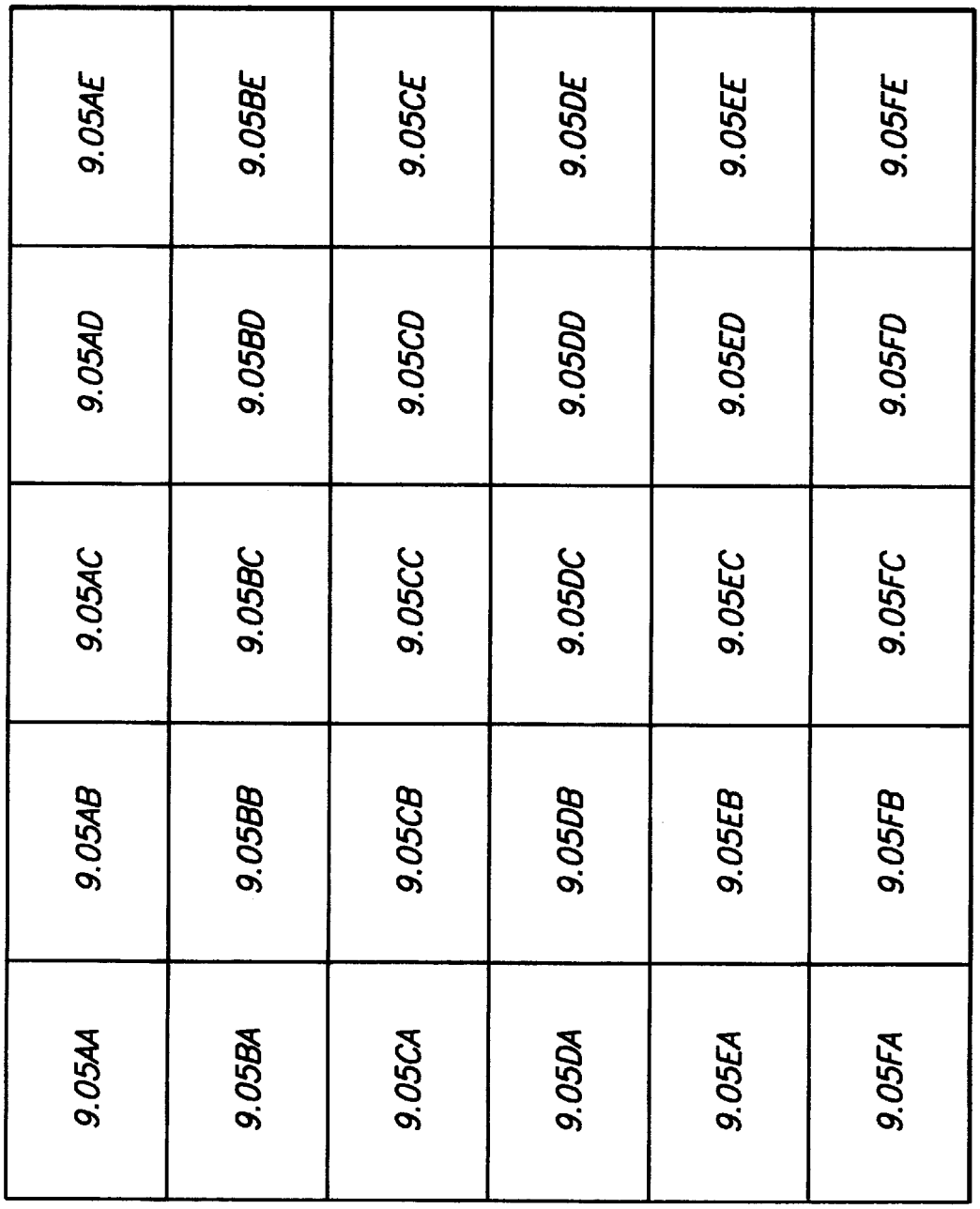

9.05AA
9.05AB
9.05AC
9.05AD
9.05AE
9.05BA
9.05BB
9.05BC
9.05BD
9.05BE
9.05CA
9.05CB
9.05CC
9.05CD
9.05CE
9.05DA
9.05DB
9.05DC
9.05DD
9.05DE
9.05EA
9.05EB
9.05EC
9.05ED
9.05EE
9.05FA
9.05FB
9.05FC
9.05FD
9.05FE

FIG. 9.05

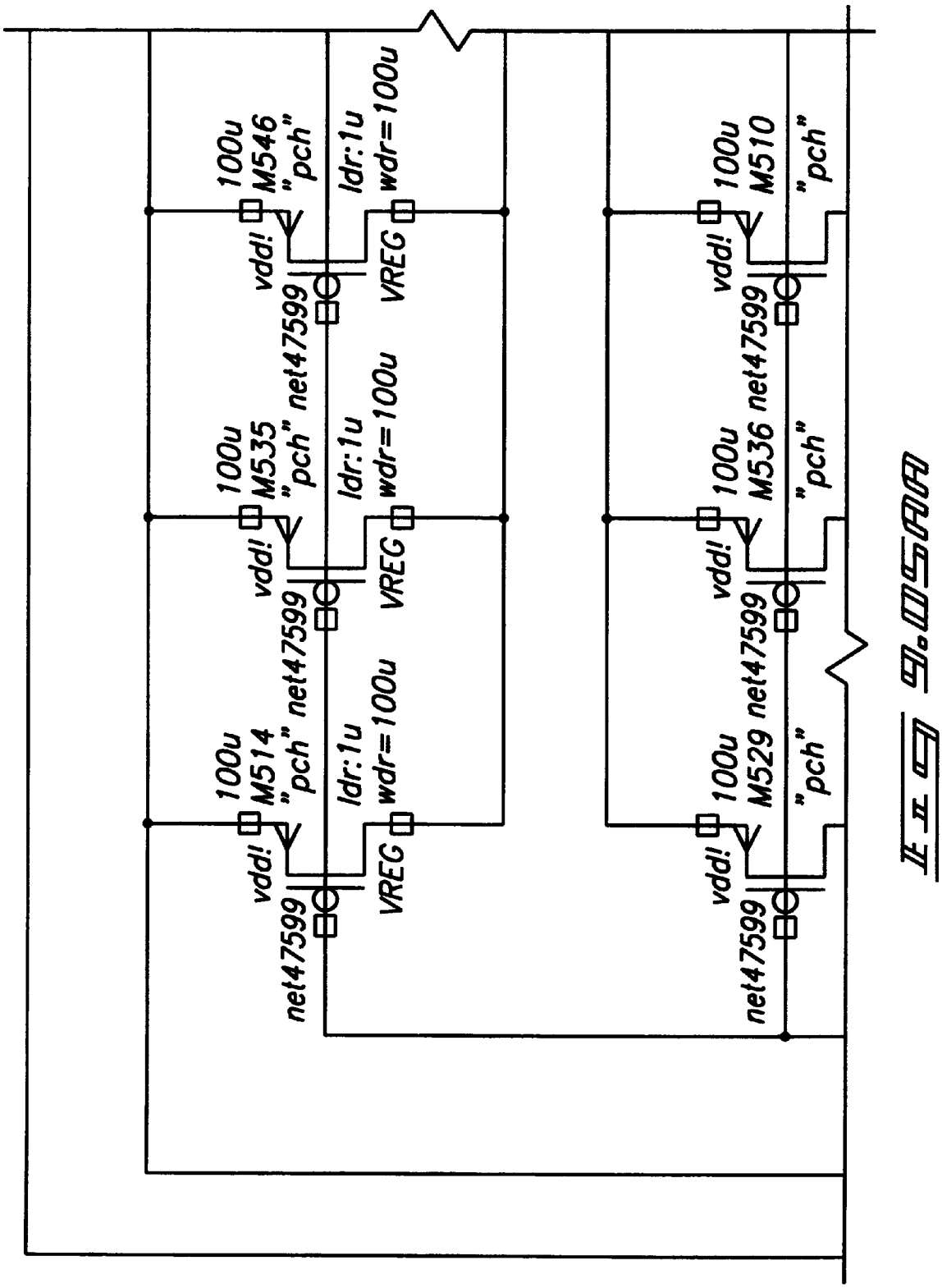

100u M546 "pch" ldr:1u wdr=100u
vdd! VREG
net47599
100u M535 "pch" net47599 ldr:1u wdr=100u
vdd! VREG
net47599
100u M514 "pch" net47599 ldr:1u wdr=100u
vdd! VREG
net47599
100u M510 "pch"
vdd!
net47599
100u M536 net47599 "pch"
vdd!
net47599
100u M529 net47599 "pch"
vdd!
net47599

FIG. 9.0564

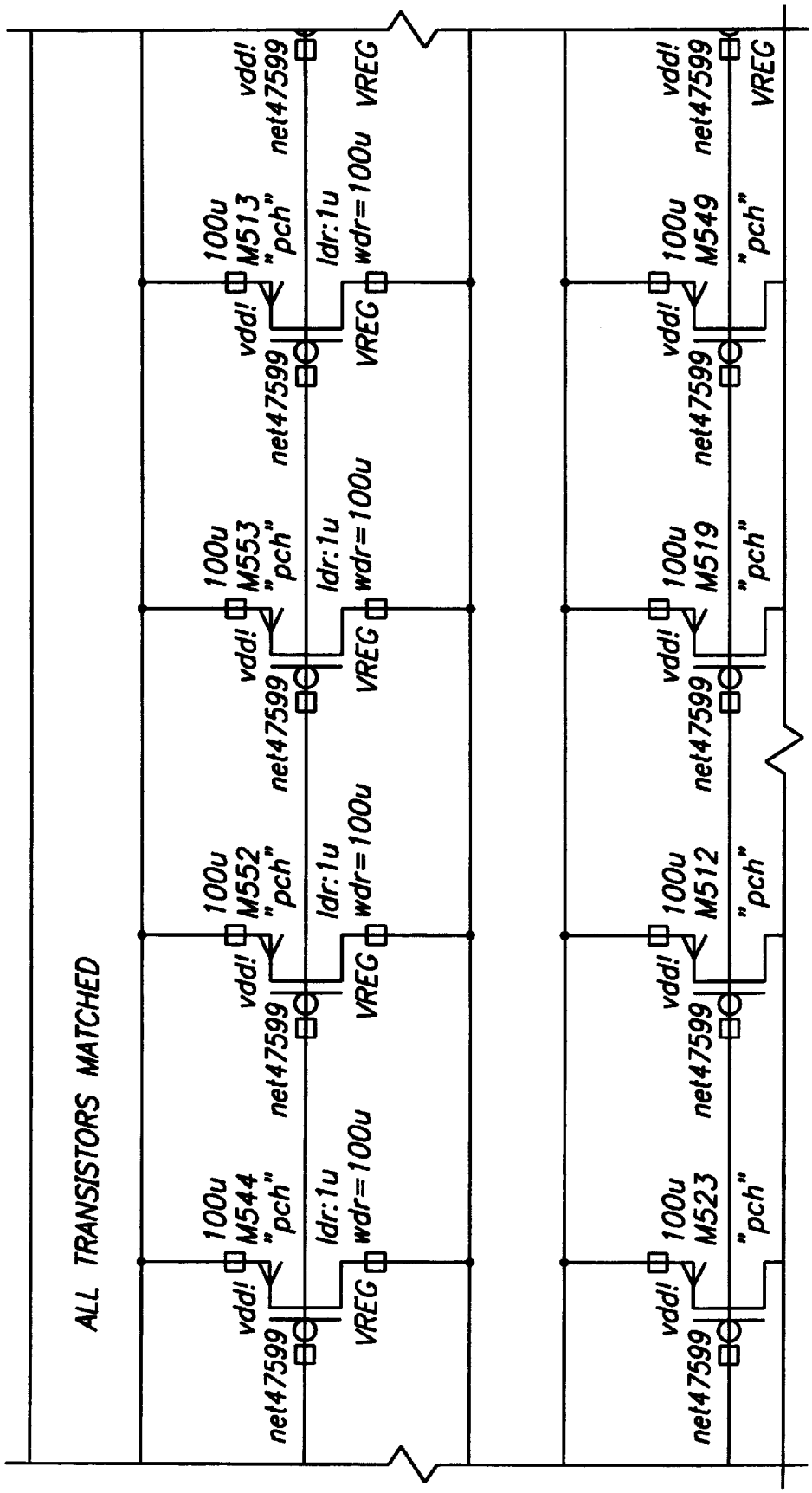

ALL TRANSISTORS MATCHED
100u M544 "pch" ldr:1u wdr=100u
100u M552 "pch" ldr:1u wdr=100u
100u M553 "pch" ldr:1u wdr=100u
100u M513 "pch" ldr:1u wdr=100u
100u M523 "pch"
100u M512 "pch"
100u M519 "pch"
100u M549 "pch"
vdd!
VREG
net47599

FIG. 459A

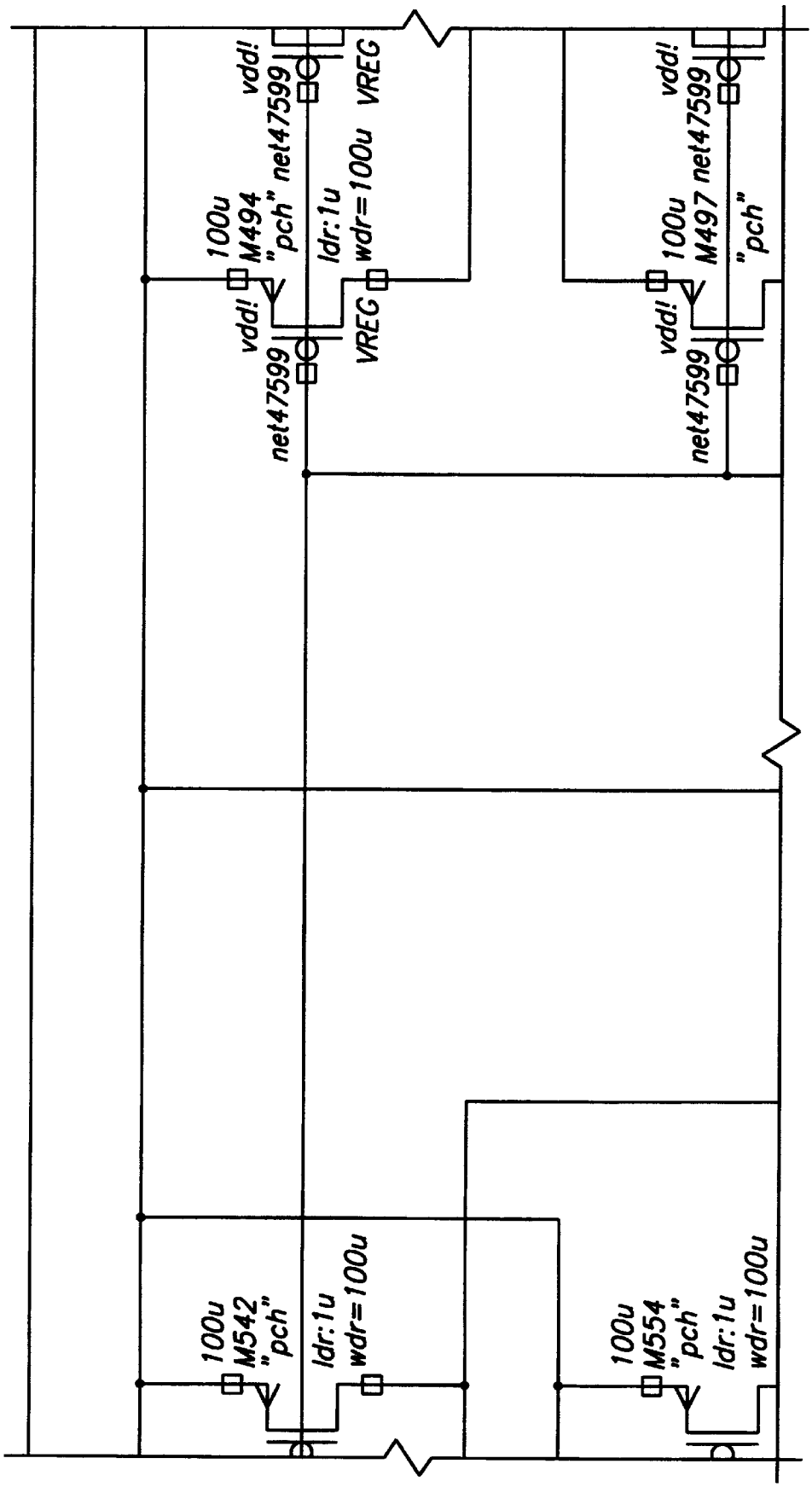

vdd!
net47599
100u
M494
"pch"
net47599
ldr:1u
wdr=100u
VREG
vdd!
net47599
VREG
vdd!
net47599
100u
M497
net47599
"pch"
vdd!
net47599
100u
M542
"pch"
ldr:1u
wdr=100u
100u
M554
"pch"
ldr:1u
wdr=100u

FIG 9,0SAC

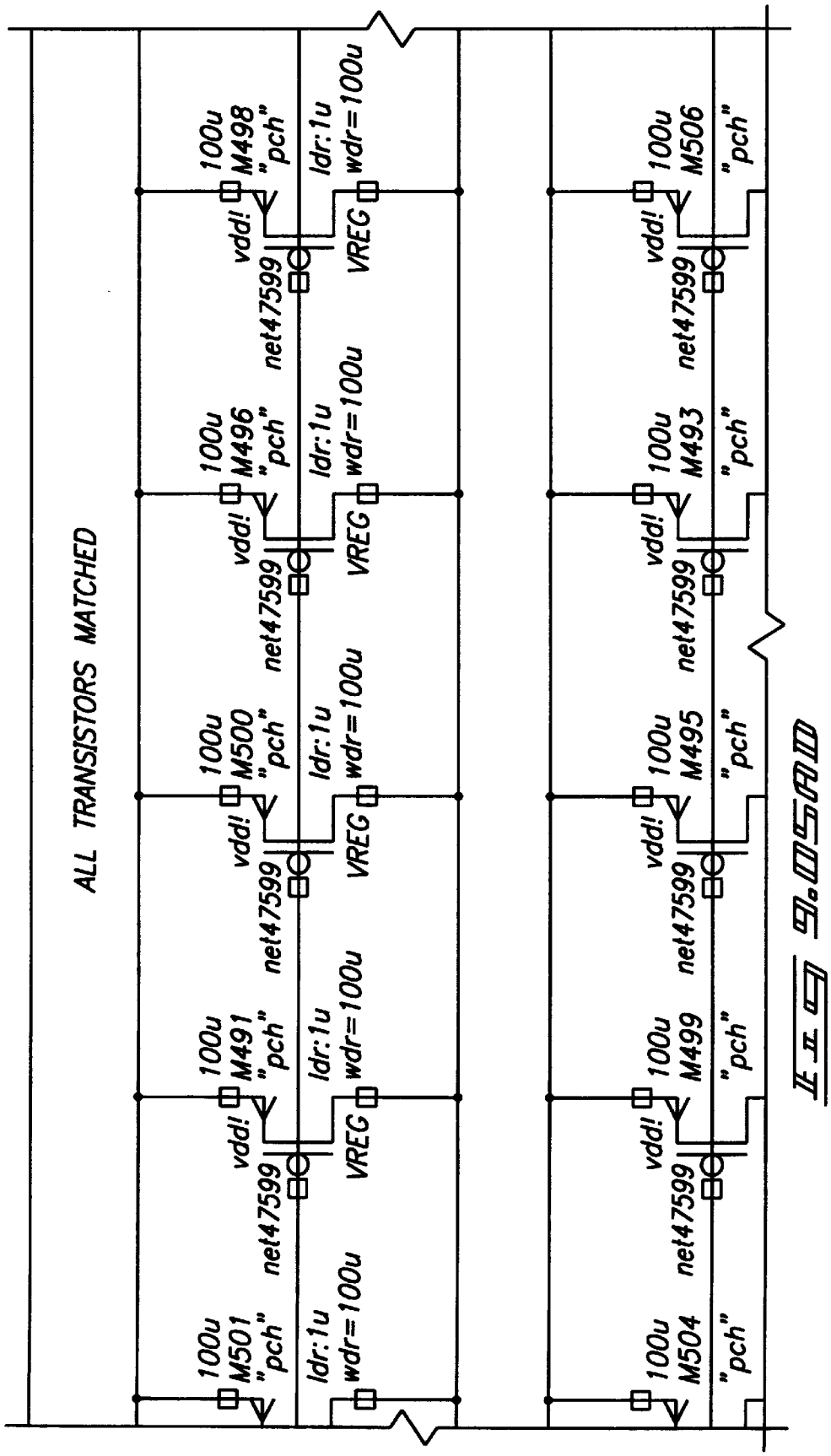

ALL TRANSISTORS MATCHED
100u M498 "pch"
100u M496 "pch"
100u M500 "pch"
100u M491 "pch"
100u M501 "pch"
100u M506 "pch"
100u M493 "pch"
100u M495 "pch"
100u M499 "pch"
100u M504 "pch"
vdd!
net47599
VREG
ldr:1u
wdr=100u

FIG 9,005,010

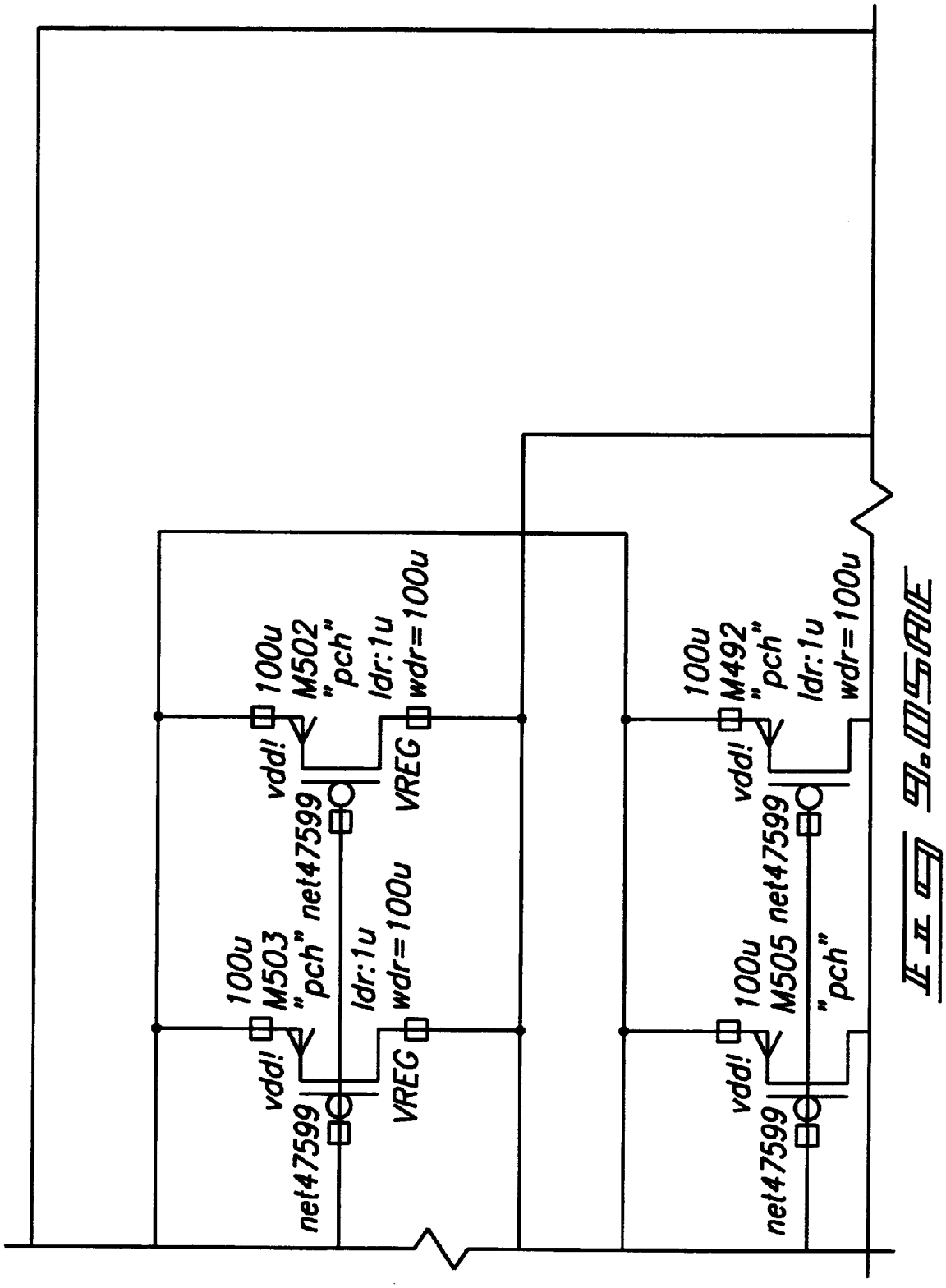


FIG 96 PRIOR ART

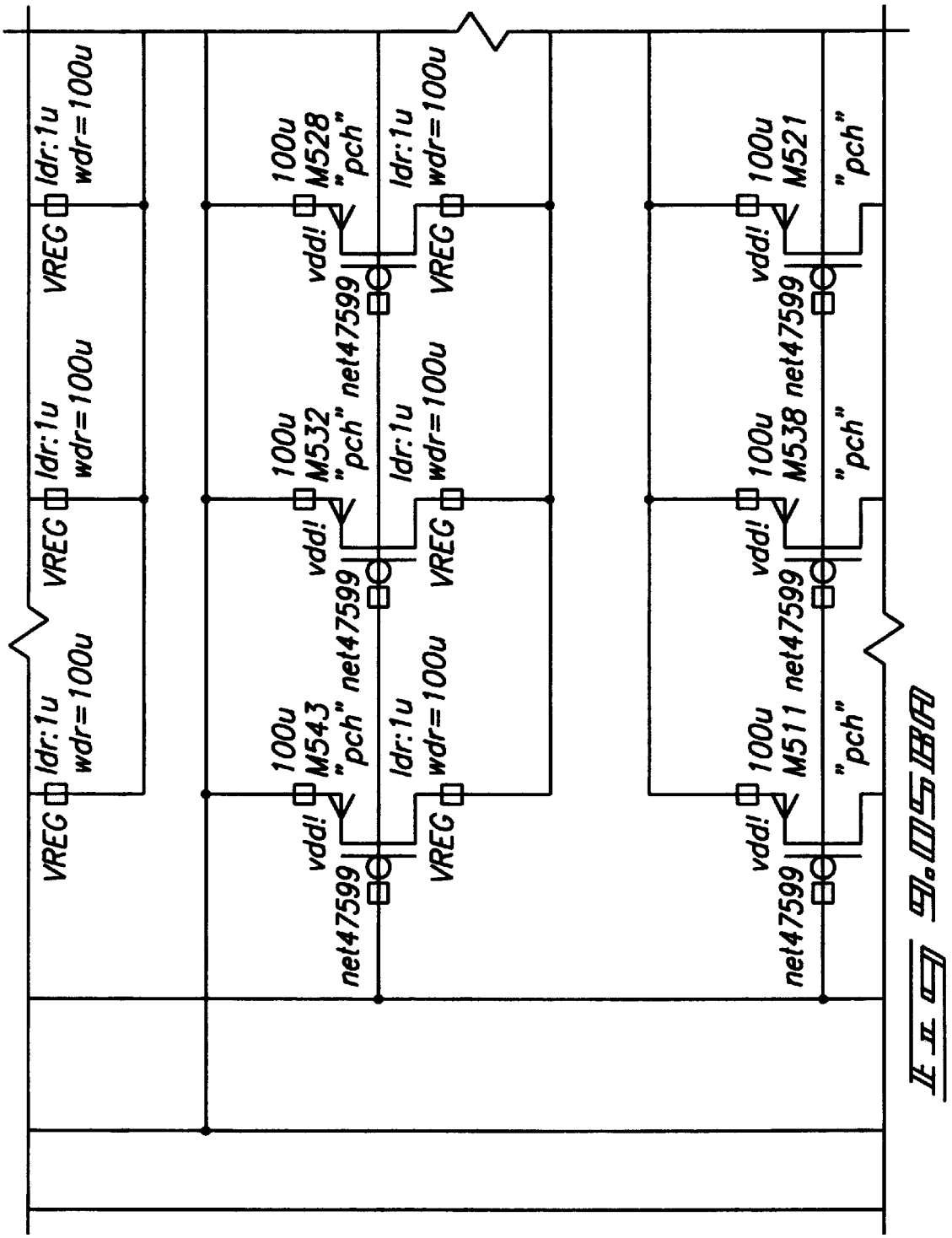
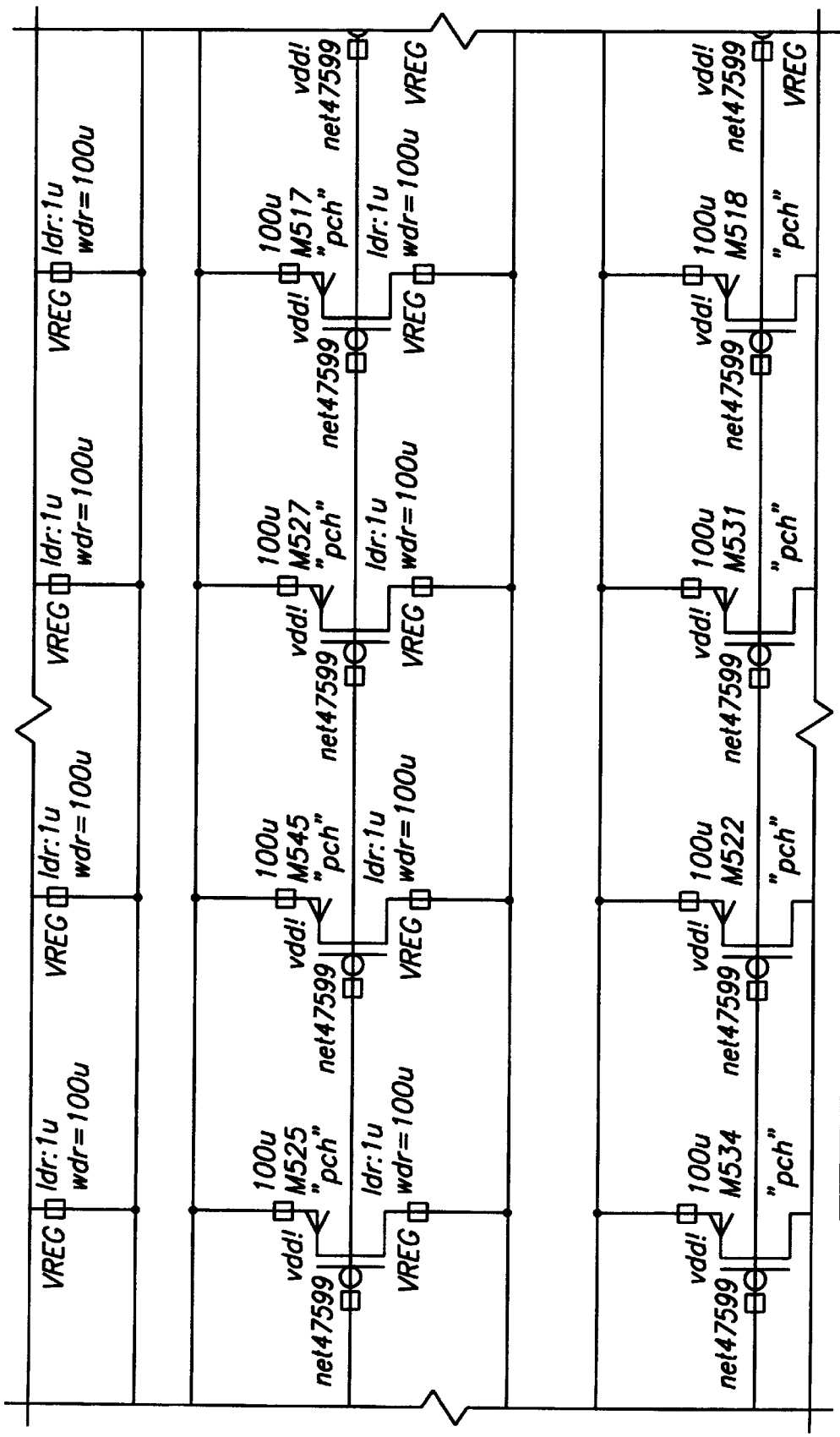

VREG
ldr:1u
wdr=100u
100u
M543
M532
M528
M521
M538
M511
"pch"
vdd!
net47599

FIG. 9.0SSBA


VREG
ldr:1u
wdr=100u
100u
M525
M534
M545
M522
M527
M531
M517
M518
"pch"
vdd!
net47599

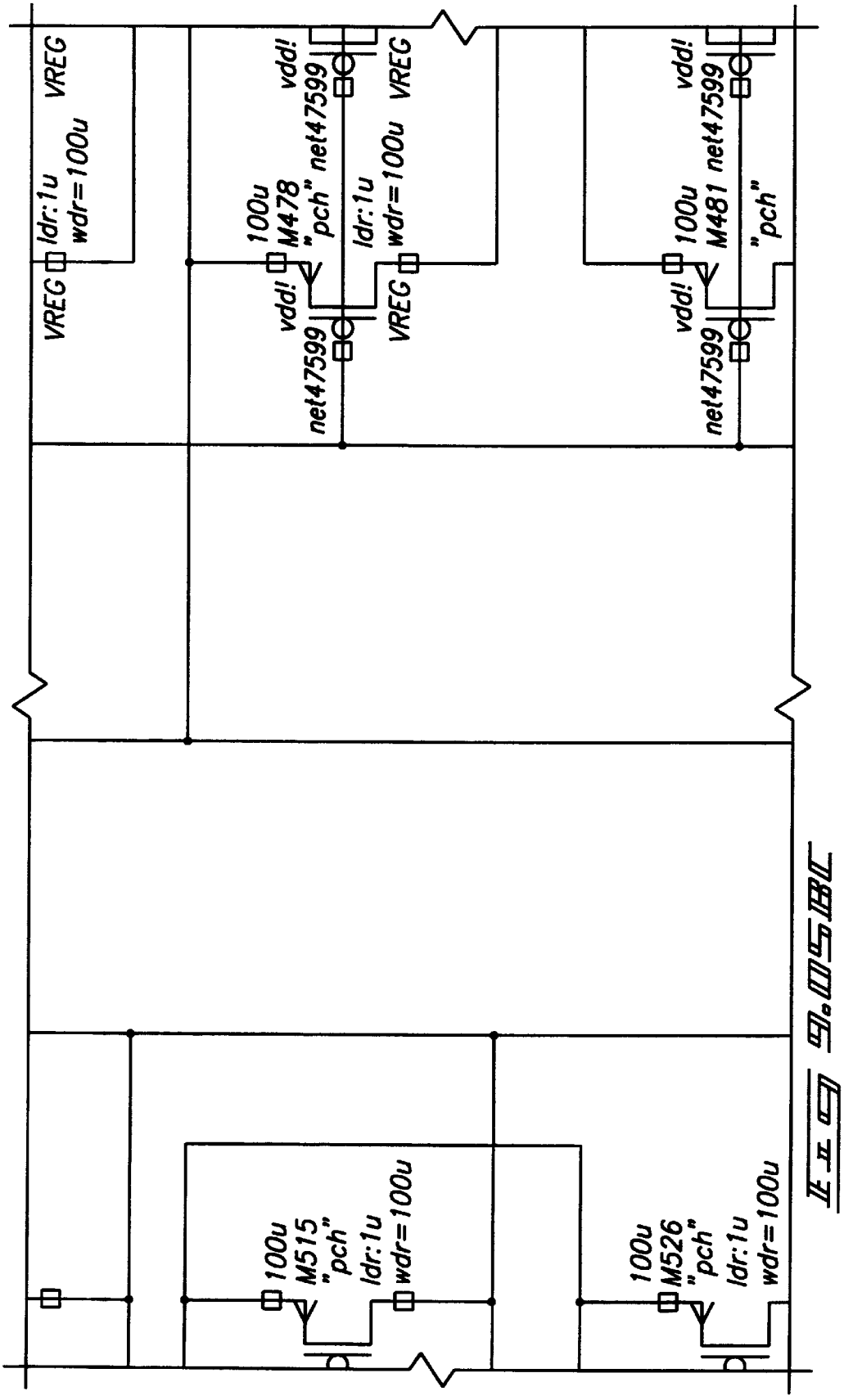


Fig 95,005,181

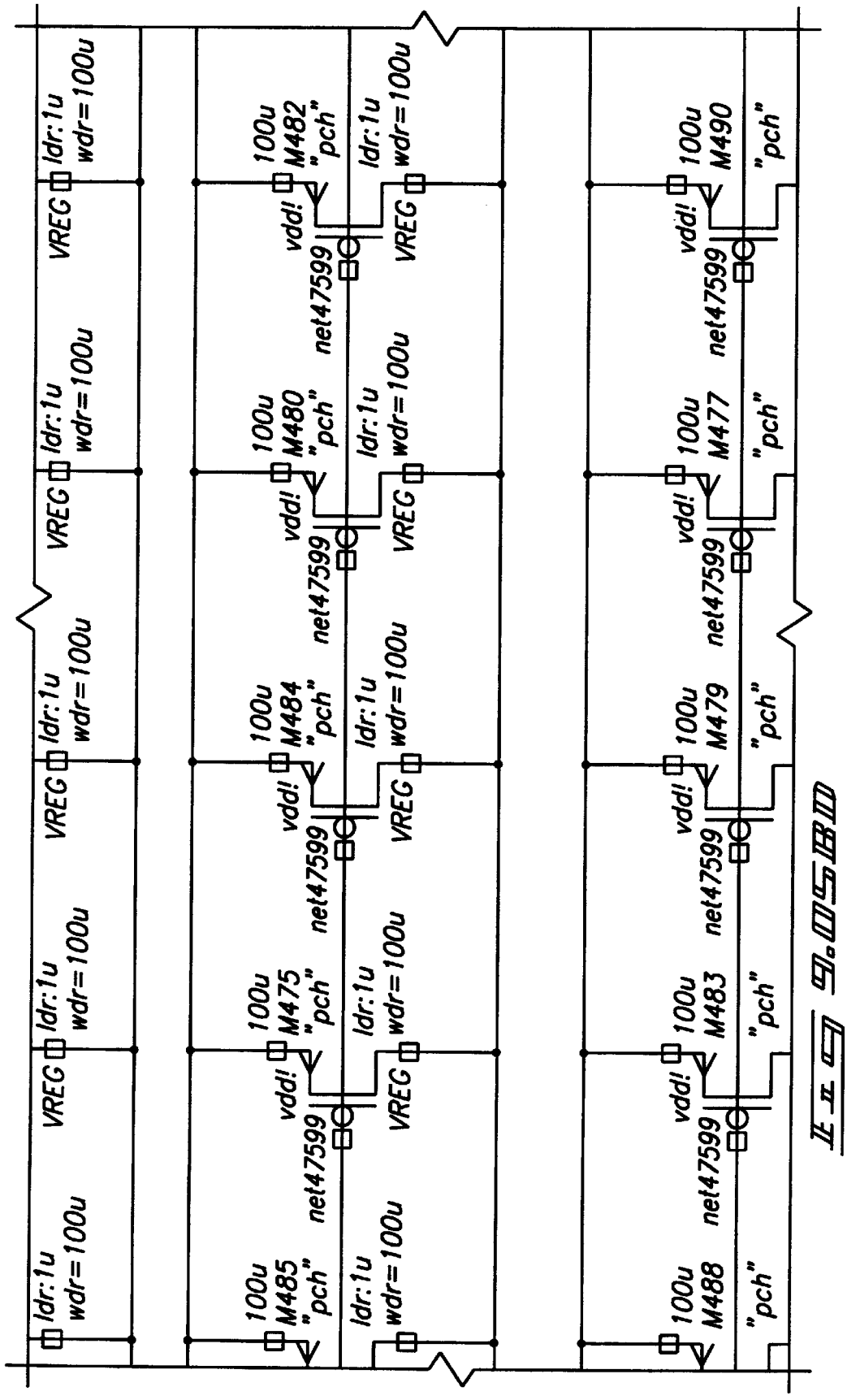
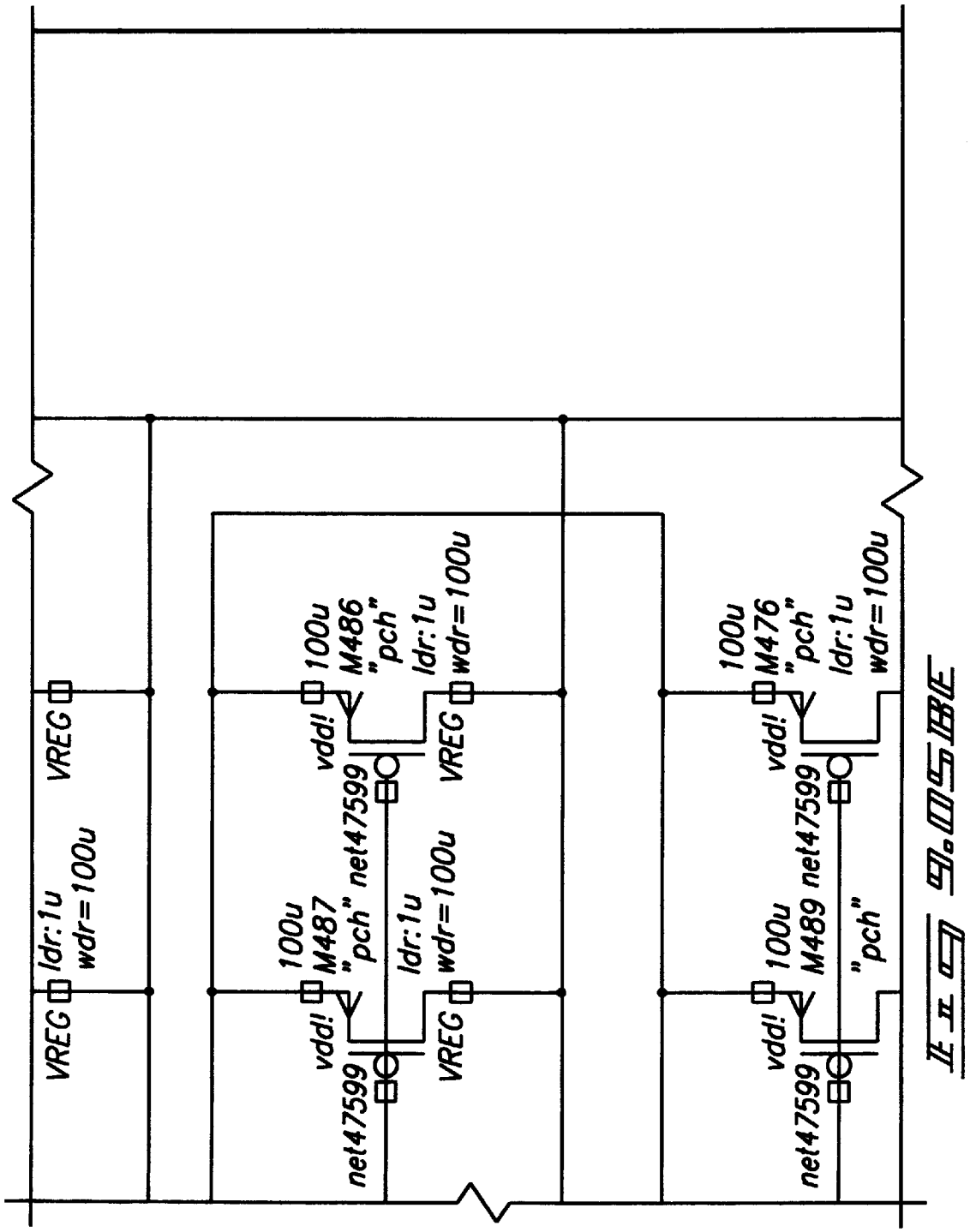

ldr:1u
wdr=100u
VREG
100u
M485
"pch"
M475
M484
M480
M482
M488
M483
M479
M477
M490
vdd!
net47599

FIG. 959B


VREG
ldr:1u
wdr=100u
100u
M487
"pch"
net47599
vdd!
100u
M486
"pch"
ldr:1u
wdr=100u
100u
M476
"pch"
100u
M489
net47599

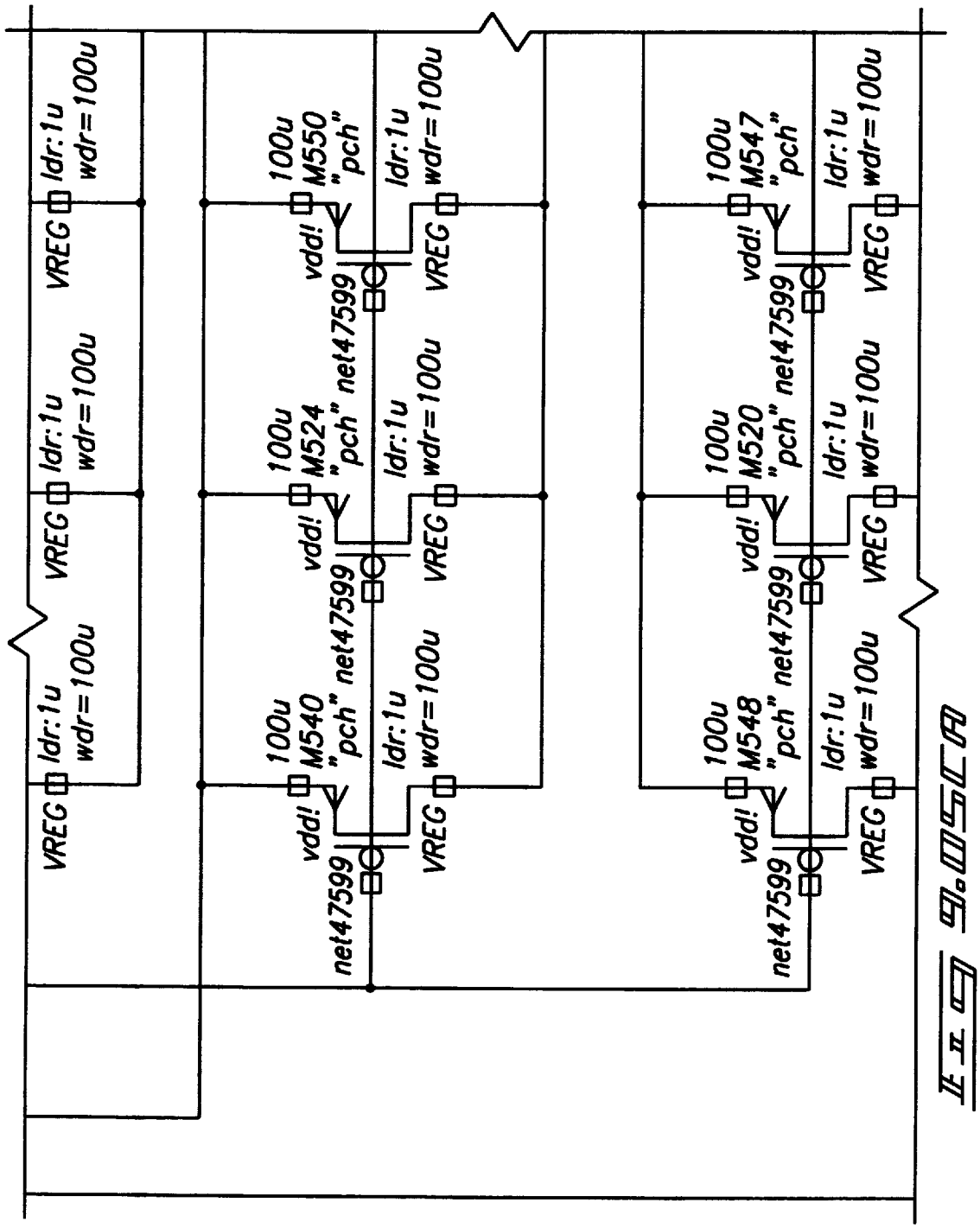

VREG
ldr:1u
wdr=100u
100u
M550
"pch"
M524
M540
M520
M548
M547
vdd!
net47599

FIG 15.005AA

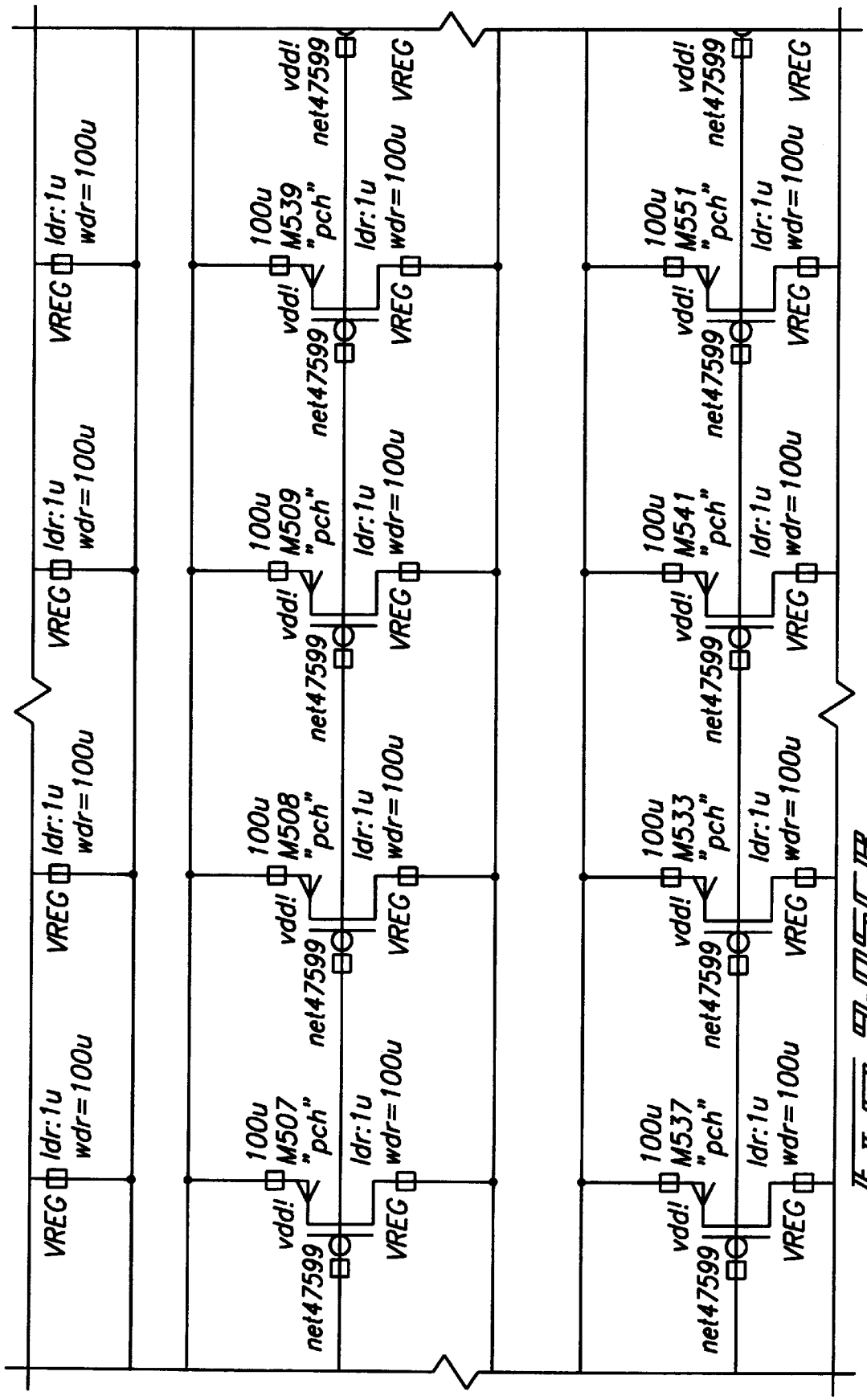

VREG
ldr:1u
wdr=100u
100u
M507
M508
M509
M533
M537
M539
M541
M551
"pch"
vdd!
net47599

FIG. 2575

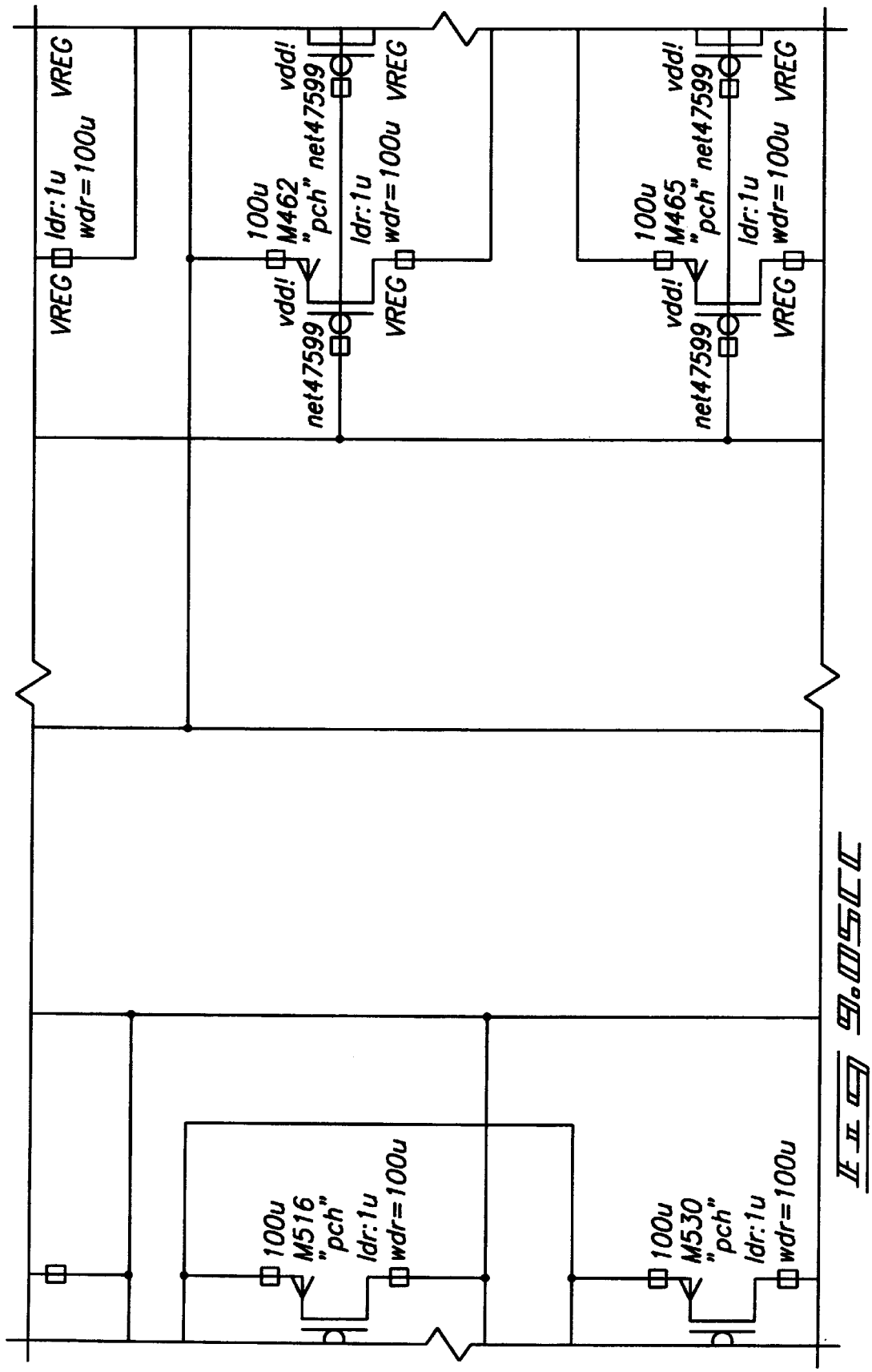

VREG
ldr:1u
wdr=100u
VREG
100u
M462
"pch"
net47599
vdd!
ldr:1u
wdr=100u
VREG
net47599
vdd!
100u
M465
"pch"
net47599
vdd!
ldr:1u
wdr=100u
VREG
net47599
vdd!
100u
M516
"pch"
ldr:1u
wdr=100u
100u
M530
"pch"
ldr:1u
wdr=100u

FIG 9.0SSW

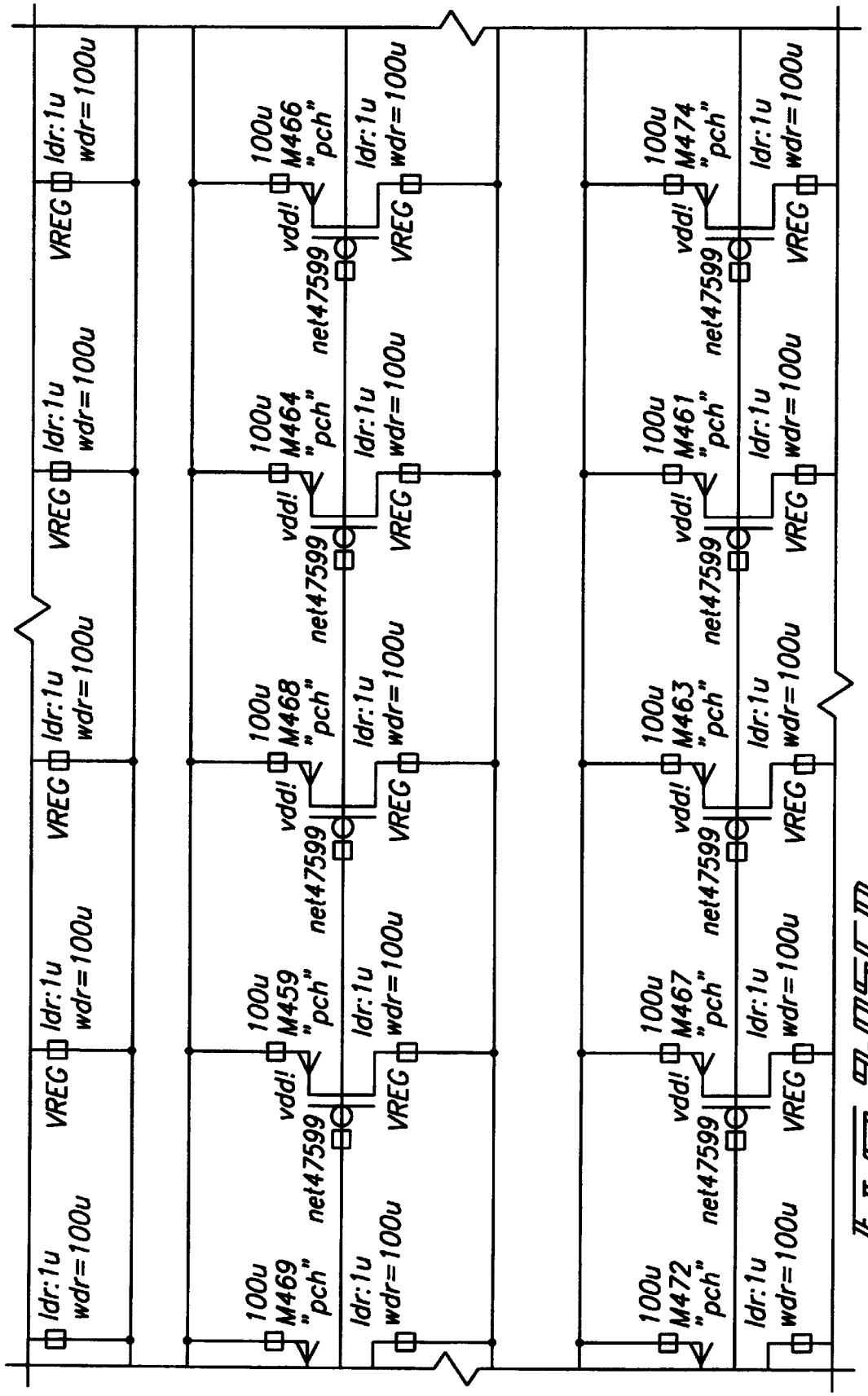

ldr:1u wdr=100u
VREG
100u M469 "pch"
100u M459 "pch"
100u M468 "pch"
100u M464 "pch"
100u M466 "pch"
100u M472 "pch"
100u M467 "pch"
100u M463 "pch"
100u M461 "pch"
100u M474 "pch"
vdd!
net47599

FIG. 2577

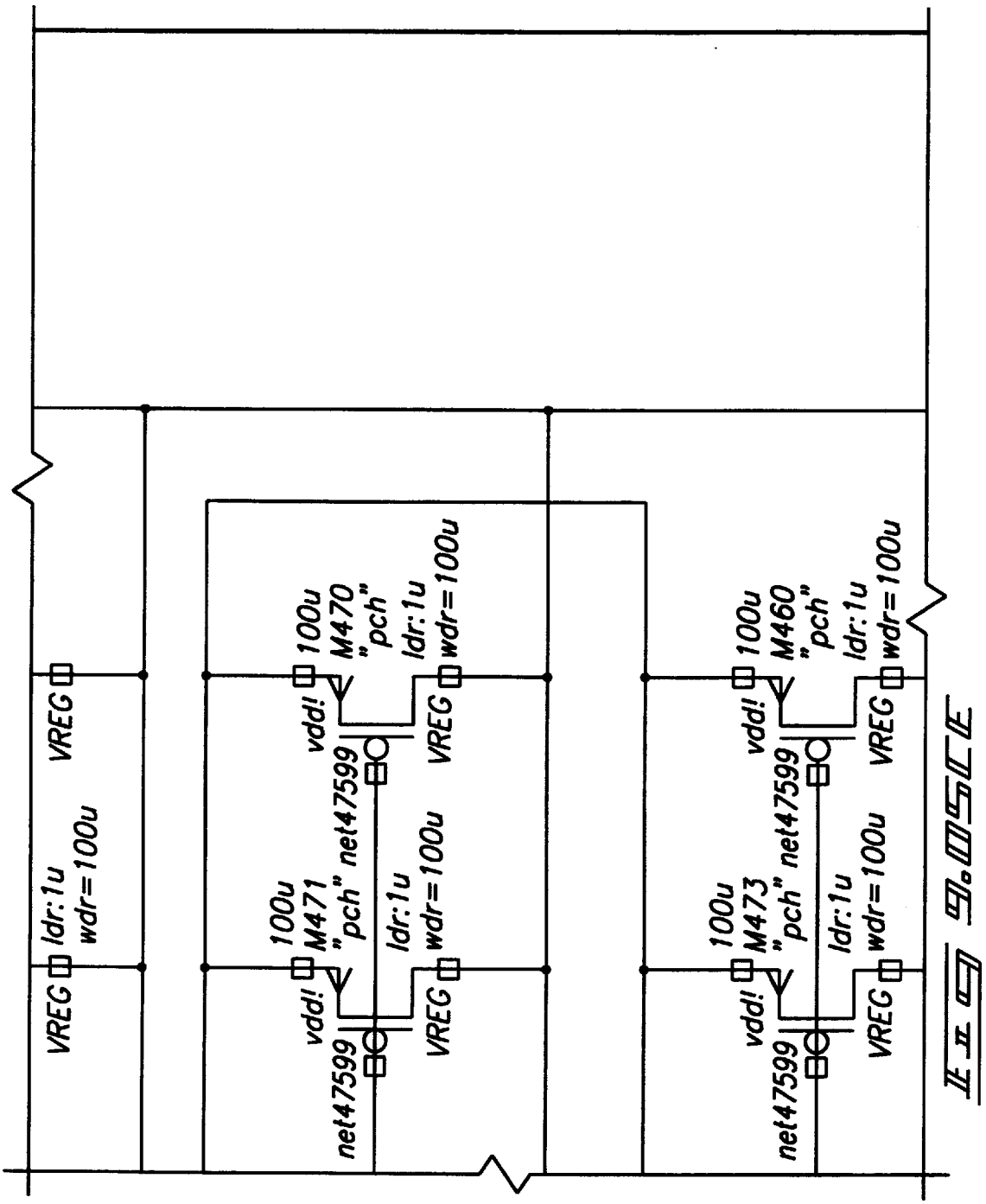
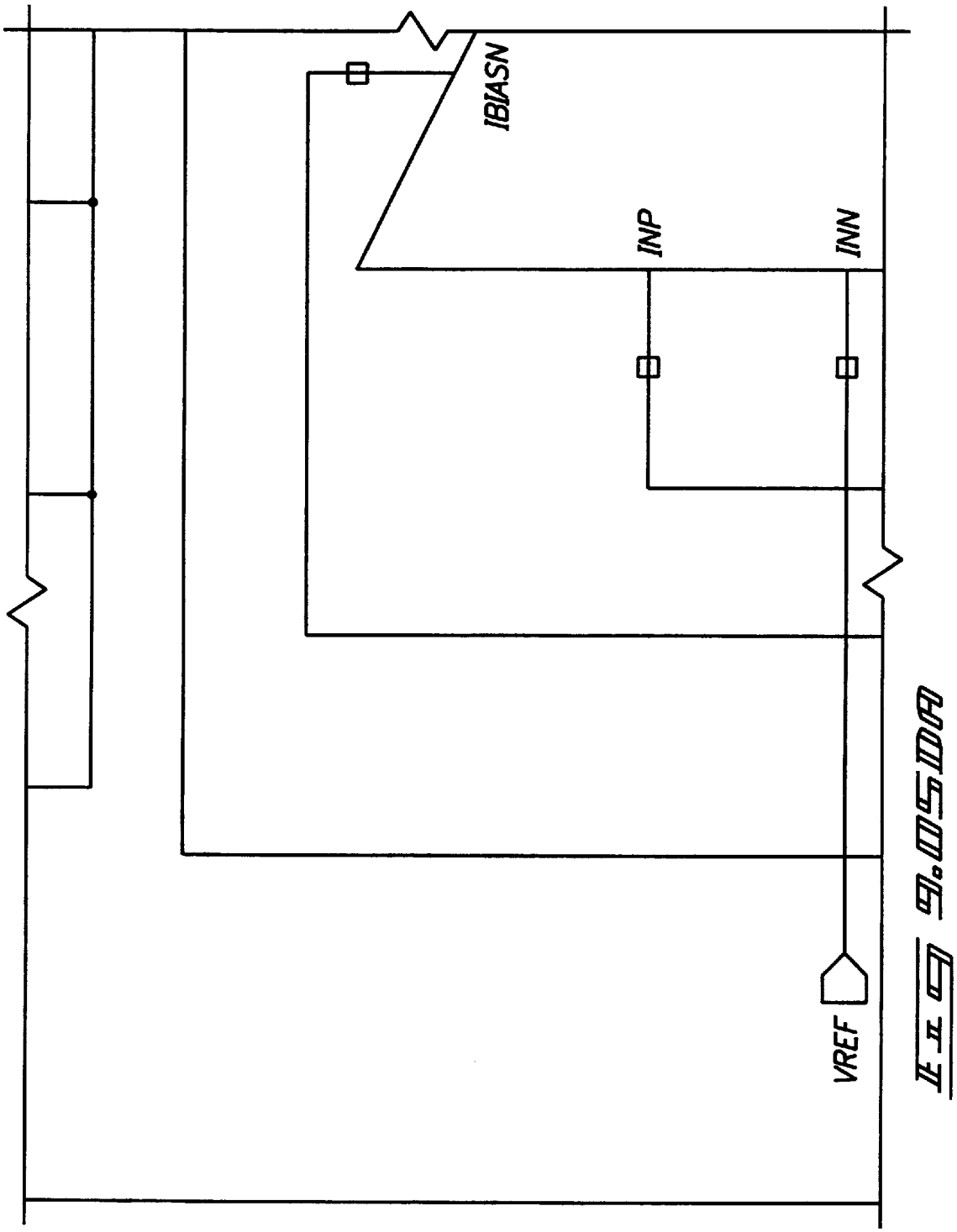

VREG
ldr:1u
wdr=100u
VREG
100u
M470
"pch"
ldr:1u
wdr=100u
vdd!
net47599
VREG
100u
M471
"pch"
net47599
ldr:1u
wdr=100u
vdd!
net47599
VREG
100u
M460
"pch"
ldr:1u
wdr=100u
vdd!
net47599
VREG
100u
M473
"pch"
net47599
ldr:1u
wdr=100u
vdd!
net47599
VREG

FIG. 4559


IBIASN
INP
INN
VREF
FIG. 9,005,016

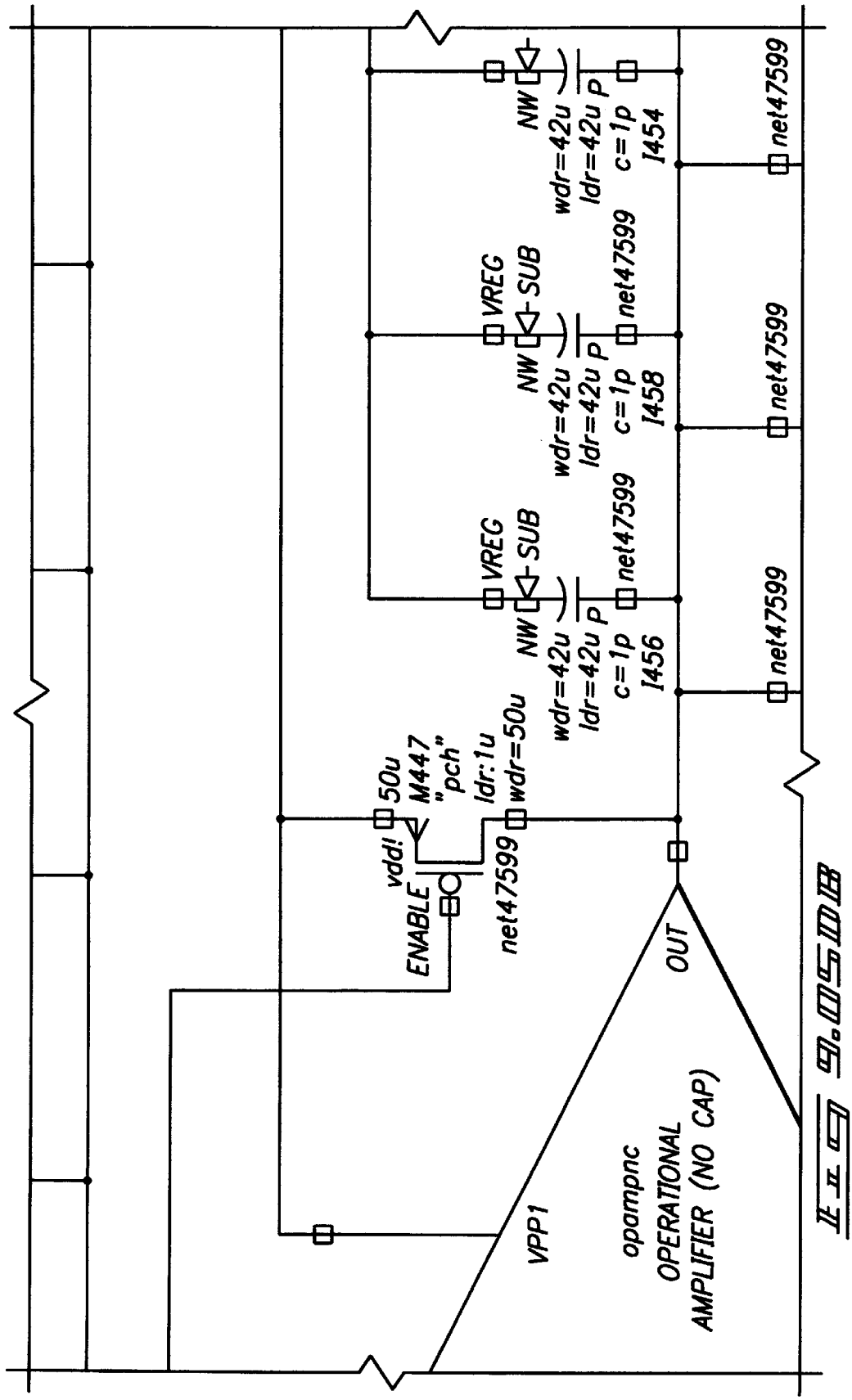

NW
wdr=42u
ldr=42u
P
c=1p
I454
net47599
VREG
SUB
I458
I456
50u
M447
"pch"
ldr:1u
wdr=50u
vdd!
ENABLE
OUT
VPP1
opampnc
OPERATIONAL
AMPLIFIER (NO CAP)

FIG. 59.0055

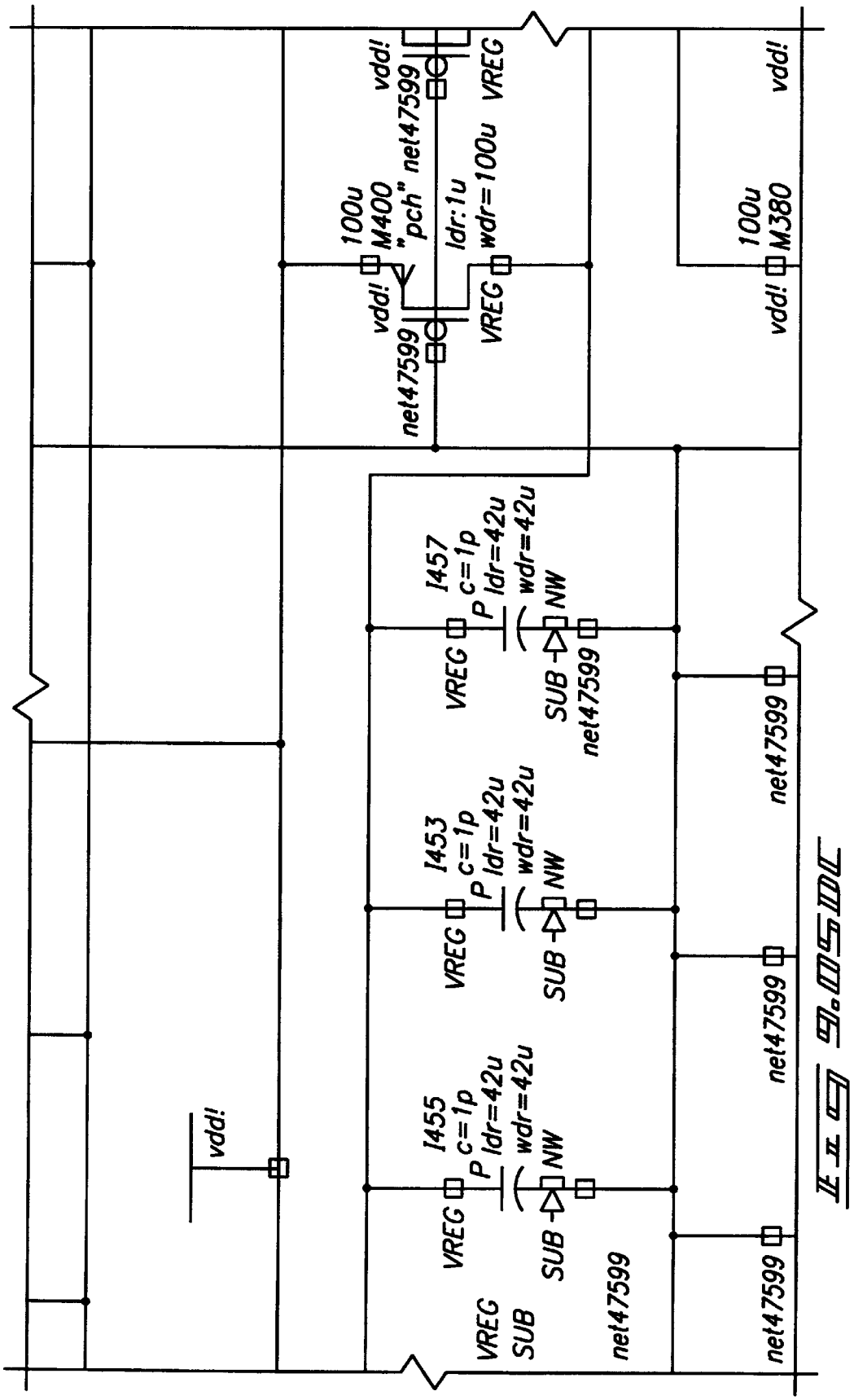

vdd!
net47599
VREG
100u
M400
"pch"
ldr:1u
wdr=100u
M380
I457
I453
I455
c=1p
P
ldr=42u
wdr=42u
NW
SUB

FIG 91.0SDC

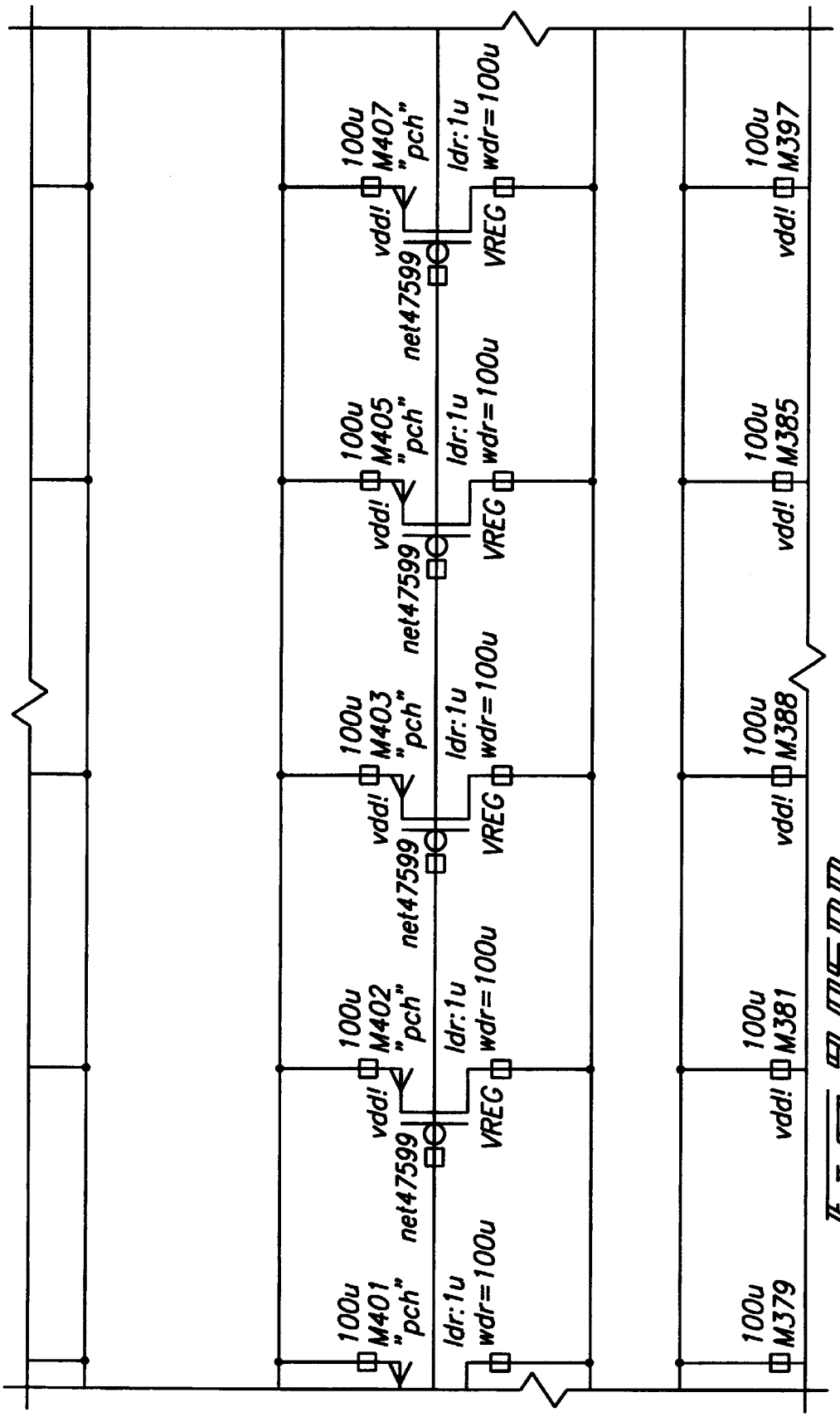

100u M407 "pch" ldr:1u wdr=100u
vdd! net47599 VREG
100u M405 "pch" ldr:1u wdr=100u
vdd! net47599 VREG
100u M403 "pch" ldr:1u wdr=100u
vdd! net47599 VREG
100u M402 "pch" ldr:1u wdr=100u
vdd! net47599 VREG
100u M401 "pch" ldr:1u wdr=100u
100u M397 vdd!
100u M385 vdd!
100u M388 vdd!
100u M381 vdd!
100u M379

FIG 59.0550

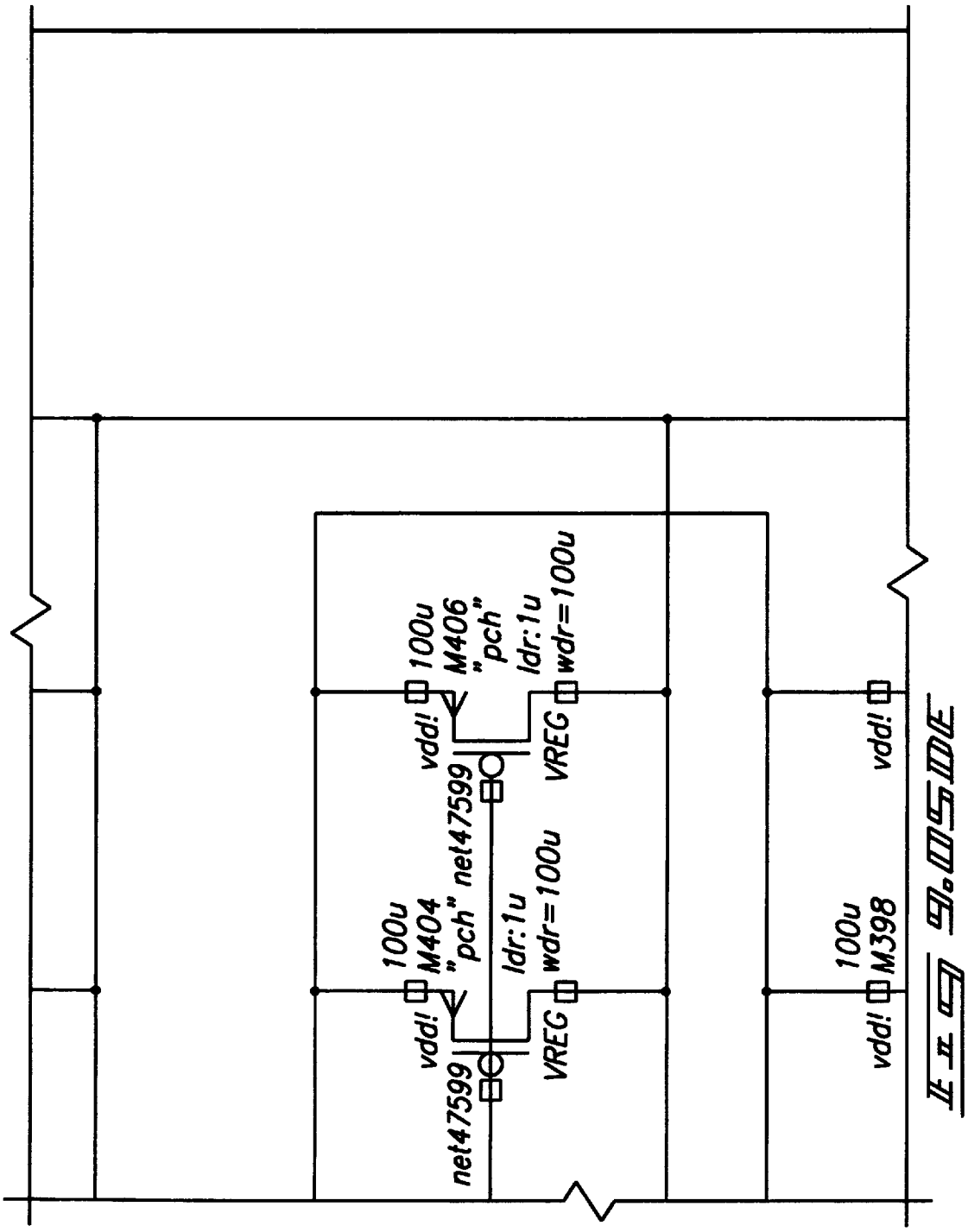
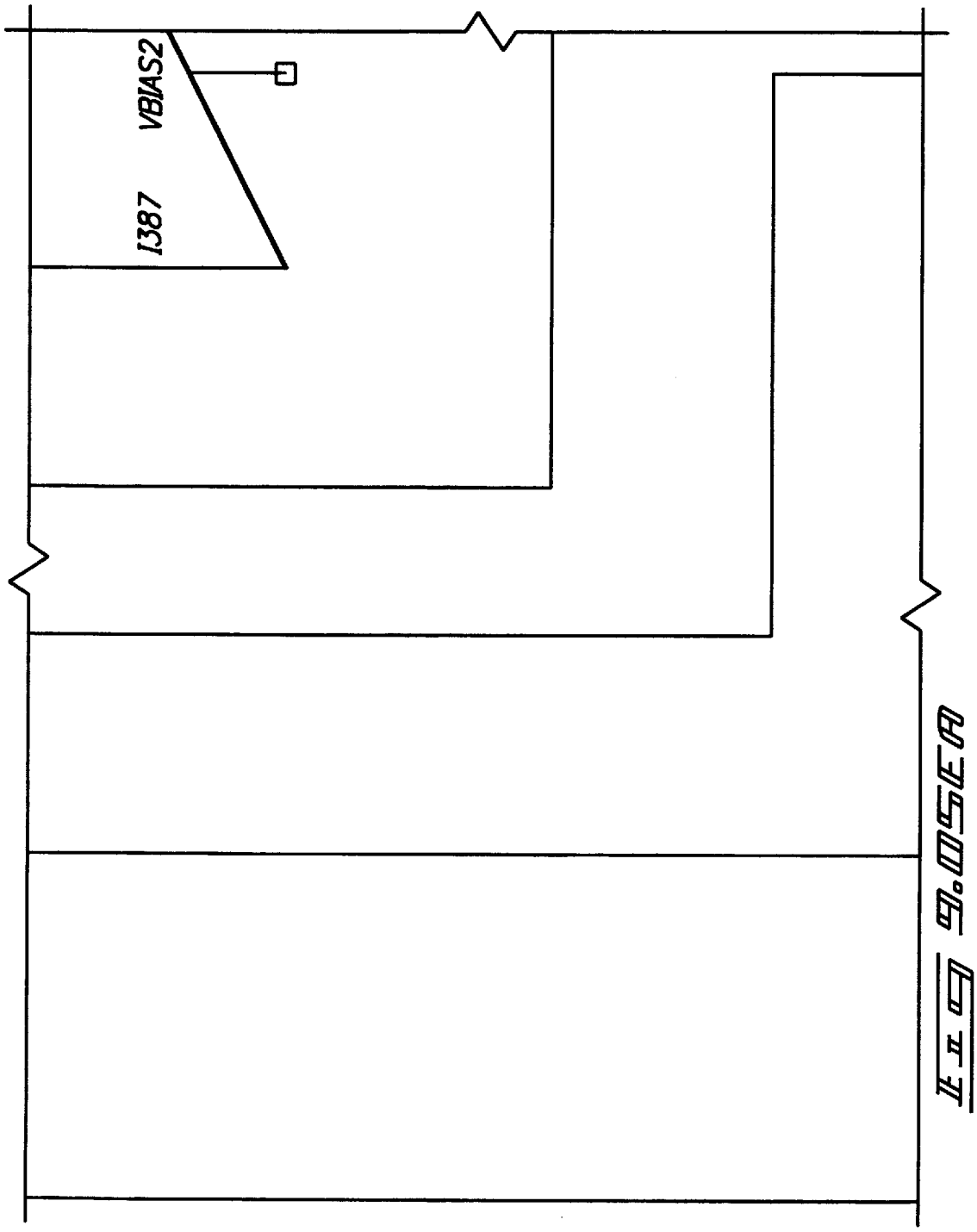
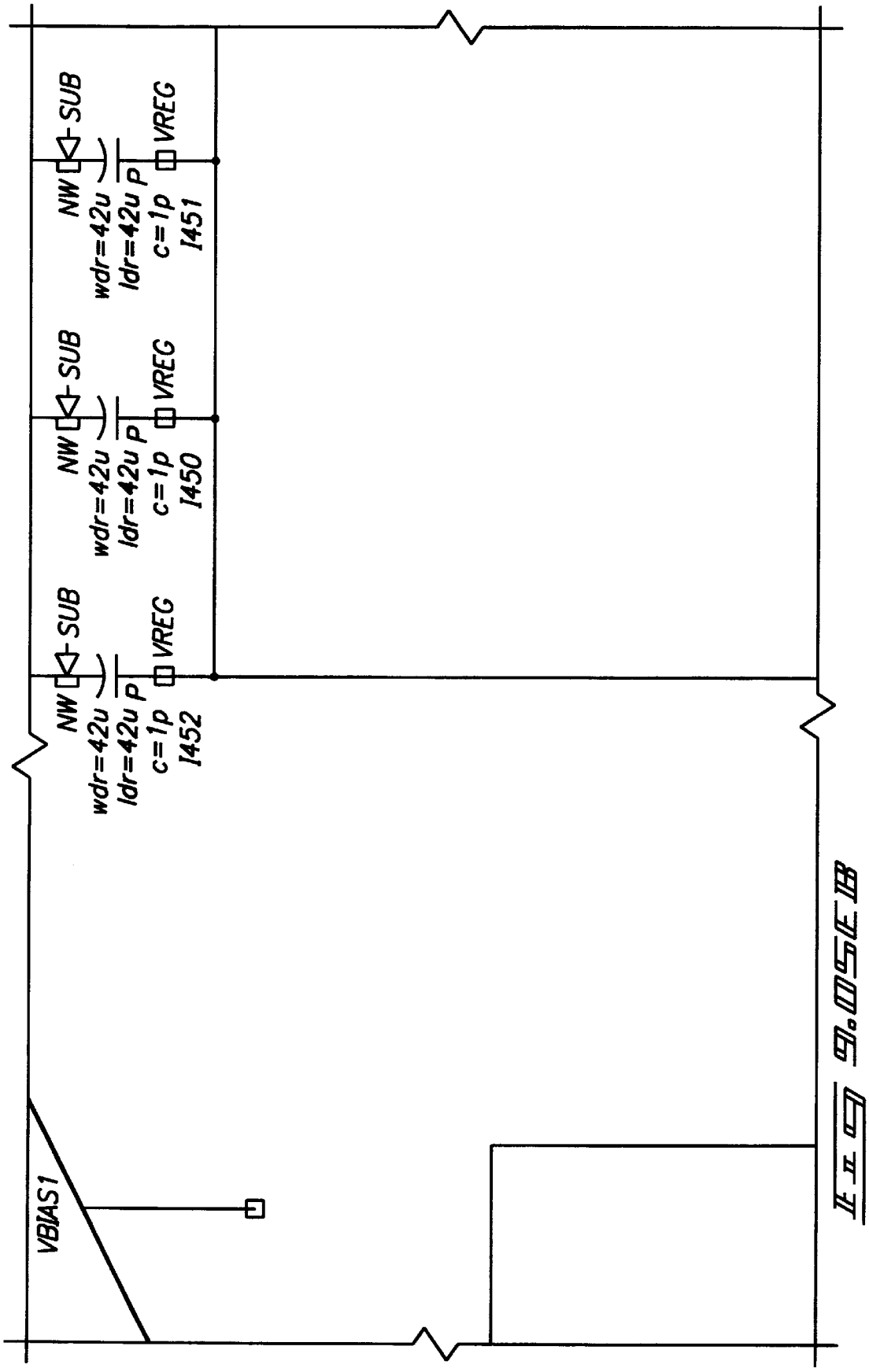
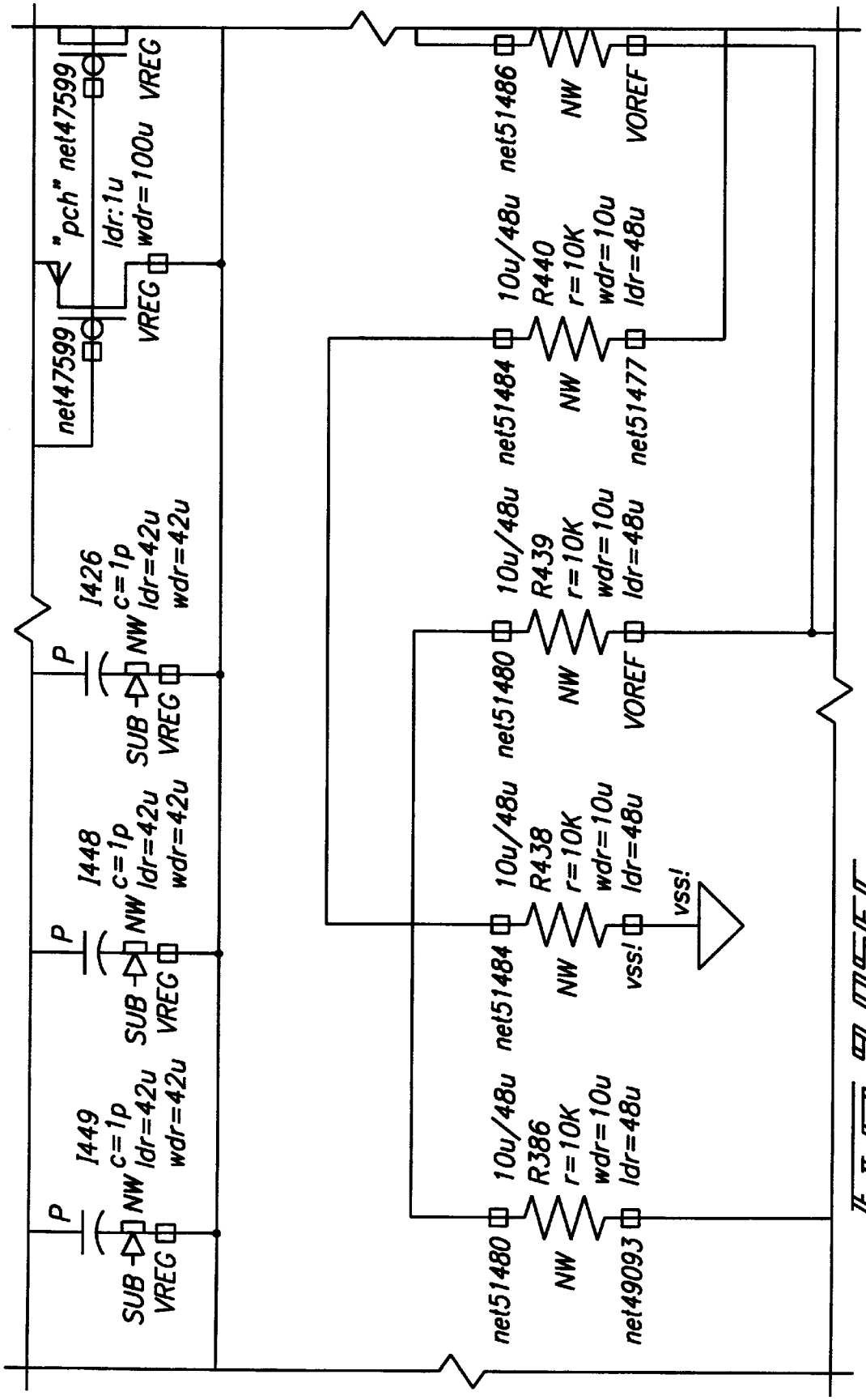

100u
M406
"pch"
ldr:1u
wdr=100u
vdd!
VREG
net47599
100u
M404
"pch"
ldr:1u
wdr=100u
vdd!
VREG
net47599
100u
M398
vdd!
vdd!

FIG. 959


VBIAS2
I387
FIG 95.0SEA


SUB
NW
wdr=42u
ldr=42u P
VREG
c=1p
I451
SUB
NW
wdr=42u
ldr=42u P
VREG
c=1p
I450
SUB
NW
wdr=42u
ldr=42u P
VREG
c=1p
I452
VBIAS1
FIG 9,056,18


"pch" net47599
ldr:1u
wdr=100u
VREG
net47599
VREG
I426
c=1p
ldr=42u
wdr=42u
P
NW
SUB
VREG
I448
c=1p
ldr=42u
wdr=42u
P
NW
SUB
VREG
I449
c=1p
ldr=42u
wdr=42u
P
NW
SUB
VREG
net51486
10u/48u
R440
r=10K
wdr=10u
ldr=48u
NW
VOREF
net51484
net51477
net51480
R439
VOREF
net51484
R438
vss!
net51480
R386
net49093
vss!

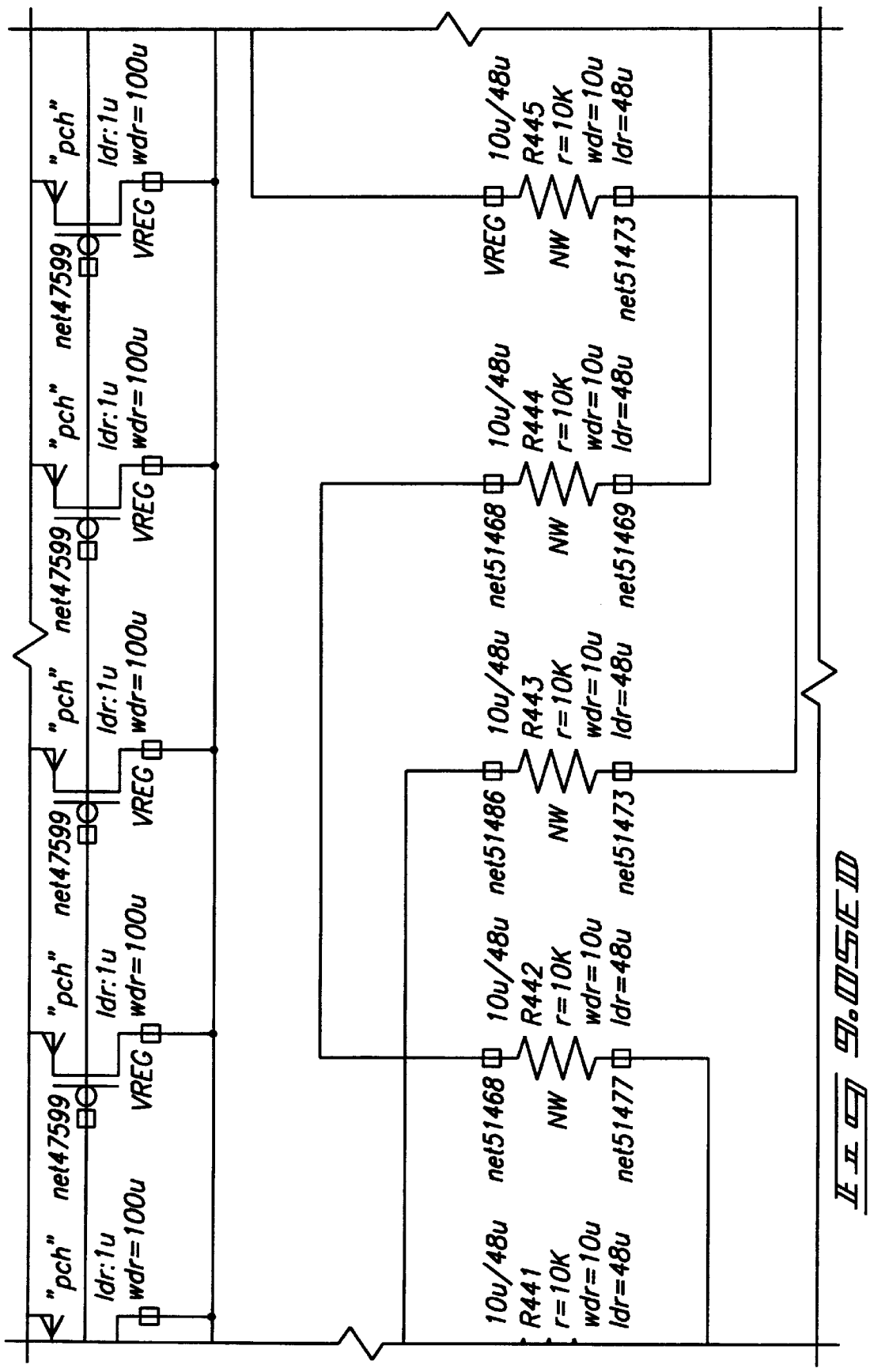
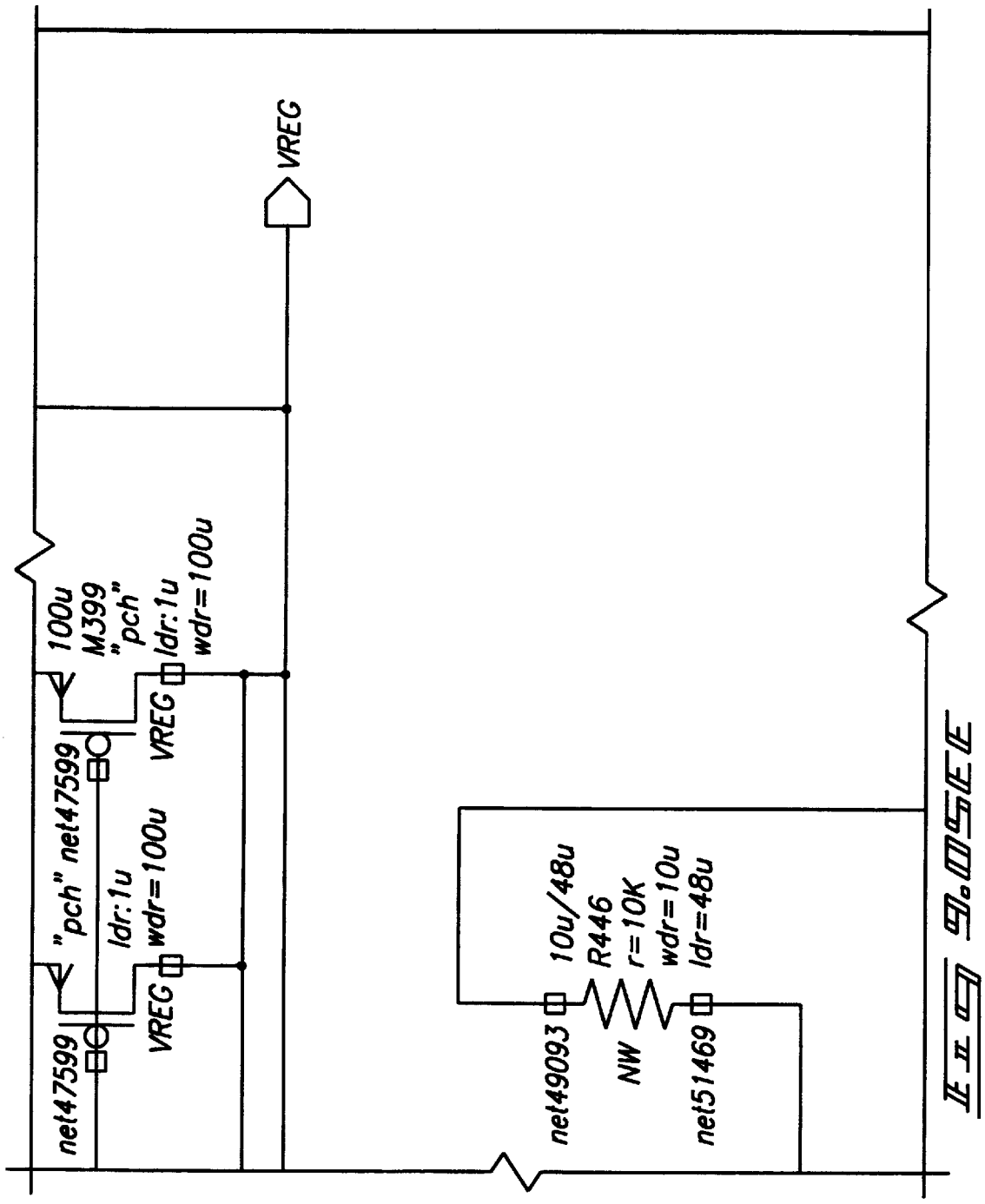

"pch" net47599 ldr:1u wdr=100u VREG
10u/48u R445 r=10K wdr=10u ldr=48u VREG NW net51473
10u/48u R444 r=10K wdr=10u ldr=48u net51468 NW net51469
10u/48u R443 r=10K wdr=10u ldr=48u net51486 NW net51473
10u/48u R442 r=10K wdr=10u ldr=48u net51468 NW net51477
10u/48u R441 r=10K wdr=10u ldr=48u

FIG. 2587


VREG
100u
M399
"pch"
ldr:1u
wdr=100u
VREG
"pch" net47599
ldr:1u
wdr=100u
VREG
net47599
10u/48u
R446
r=10K
wdr=10u
ldr=48u
net49093
NW
net51469
FIG. 9.0SEE

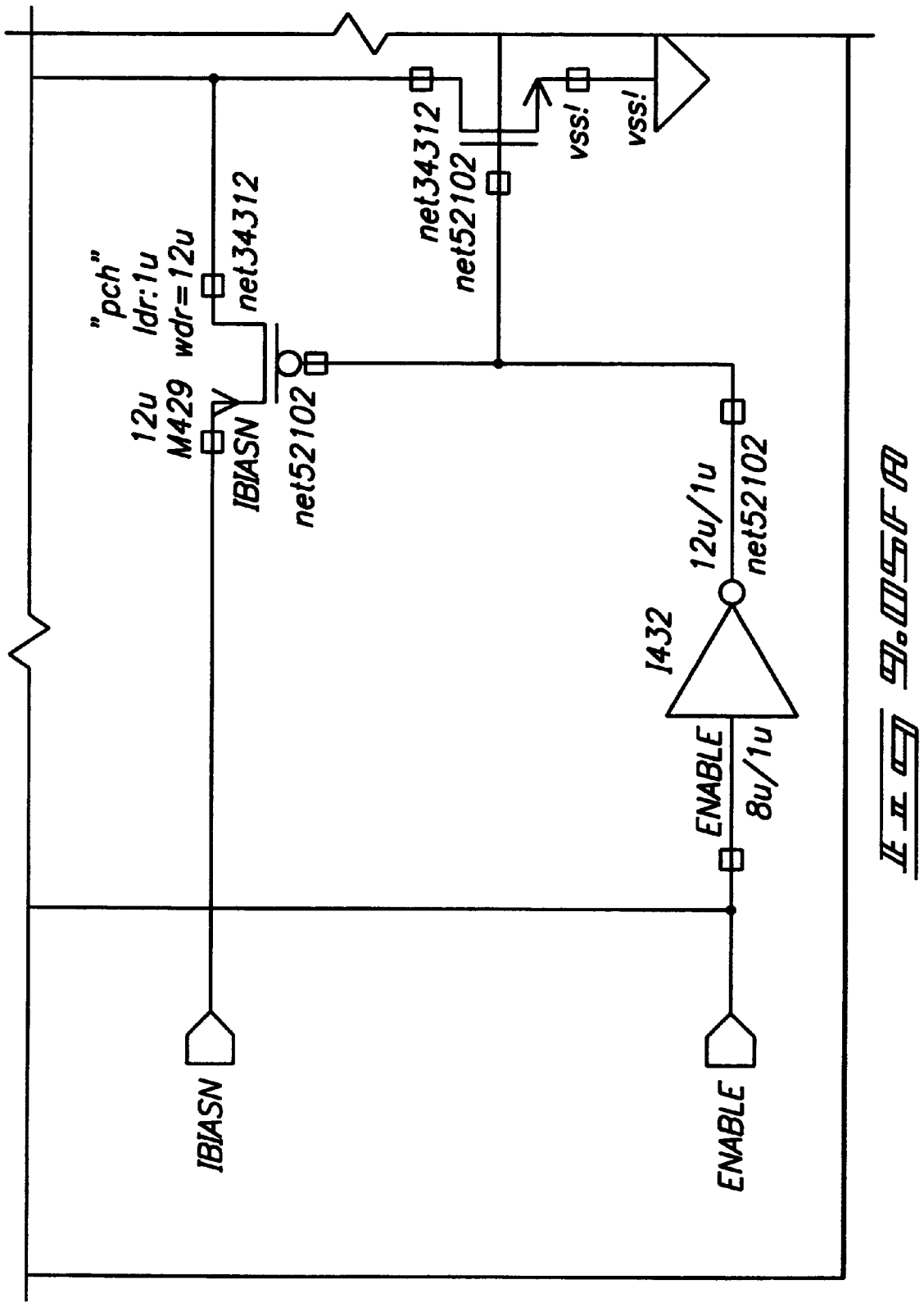
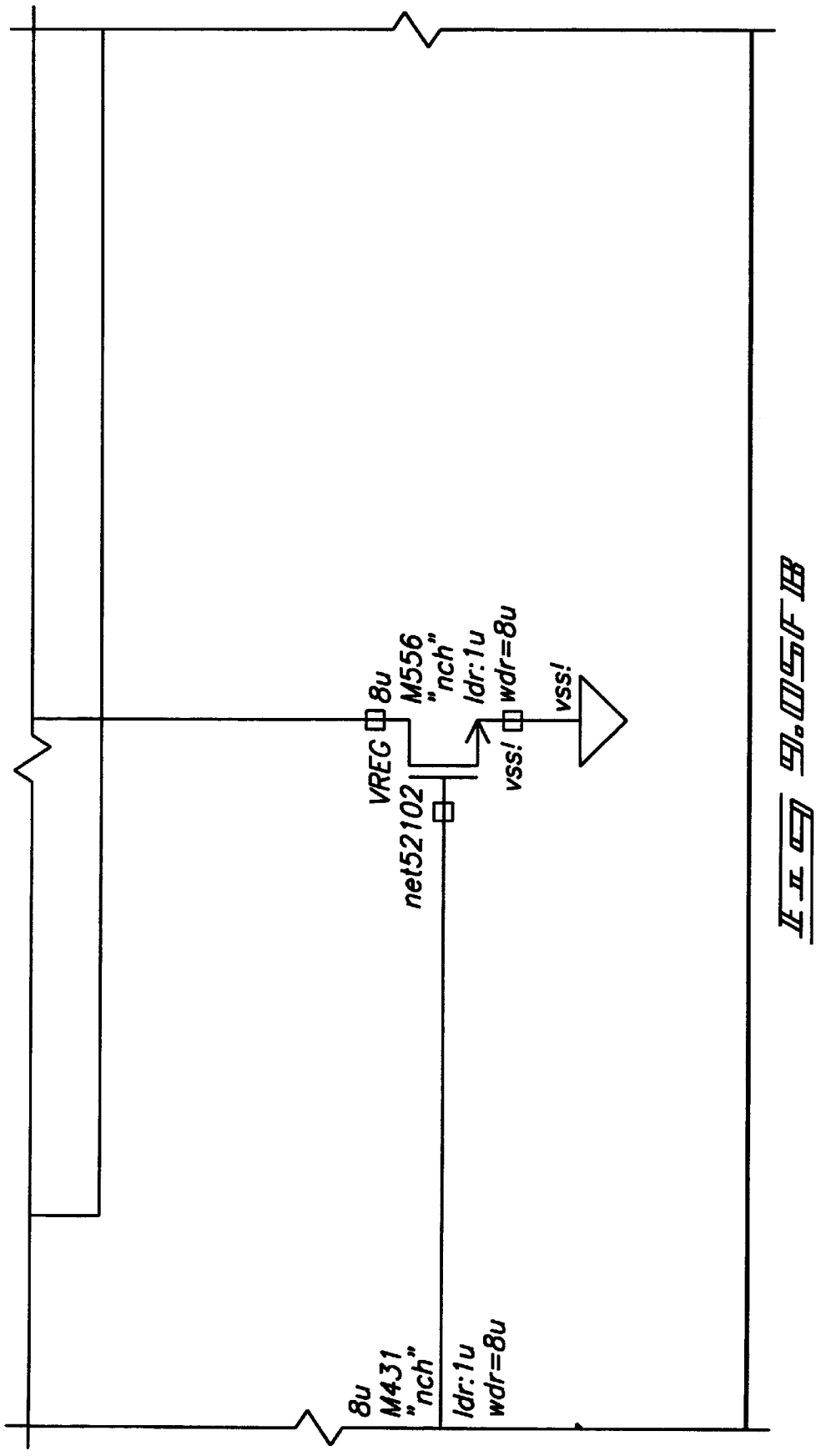

"pch"
ldr:1u
wdr=12u
net34312
12u
M429
IBIASN
net52102
net34312
net52102
vss!
vss!
12u/1u
net52102
I432
ENABLE
8u/1u
IBIASN
ENABLE

FIG. 2589


8u
M556
"nch"
ldr:1u
wdr=8u
VREG
vss!
vss!
net52102
8u
M431
"nch"
ldr:1u
wdr=8u

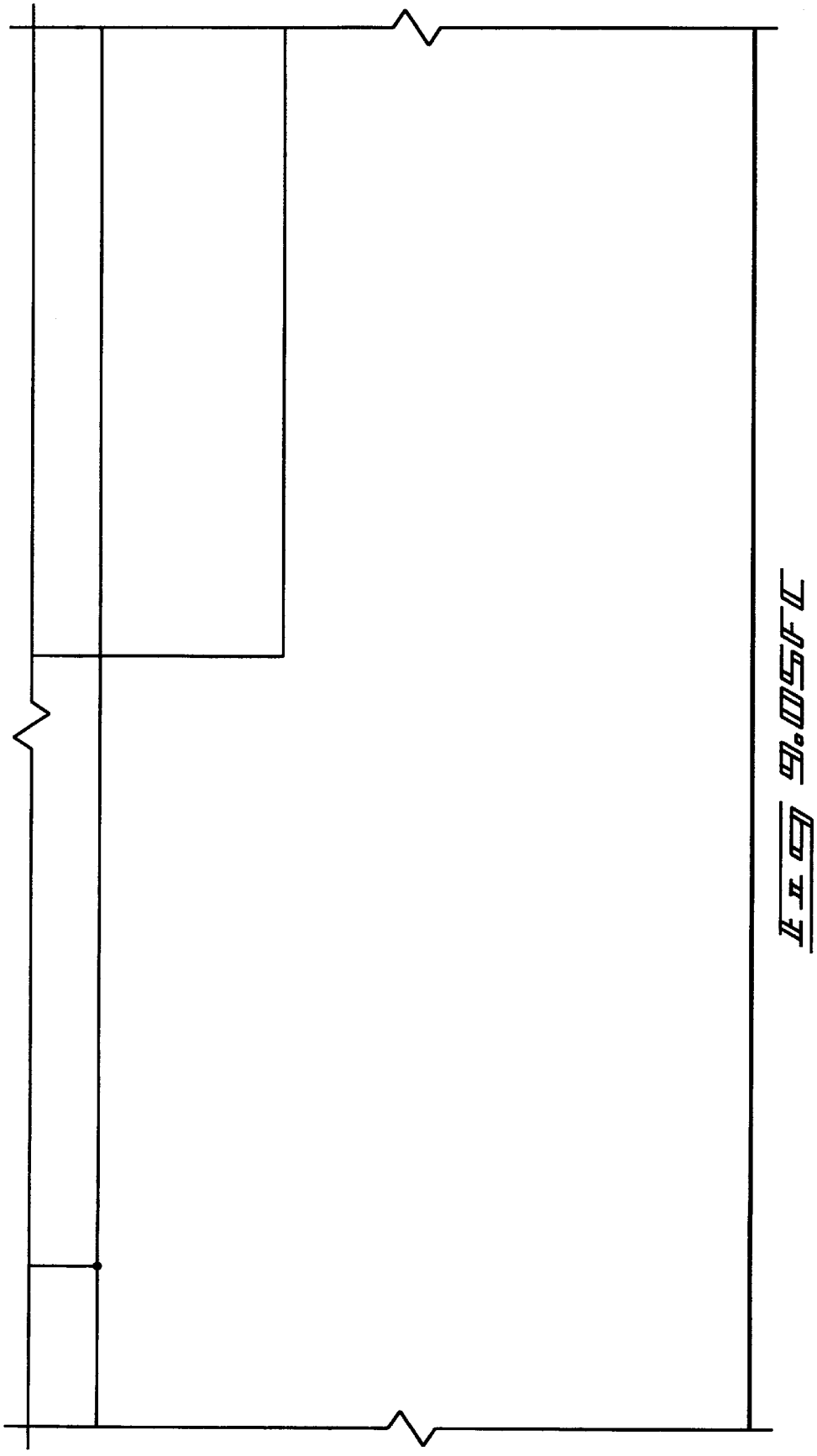
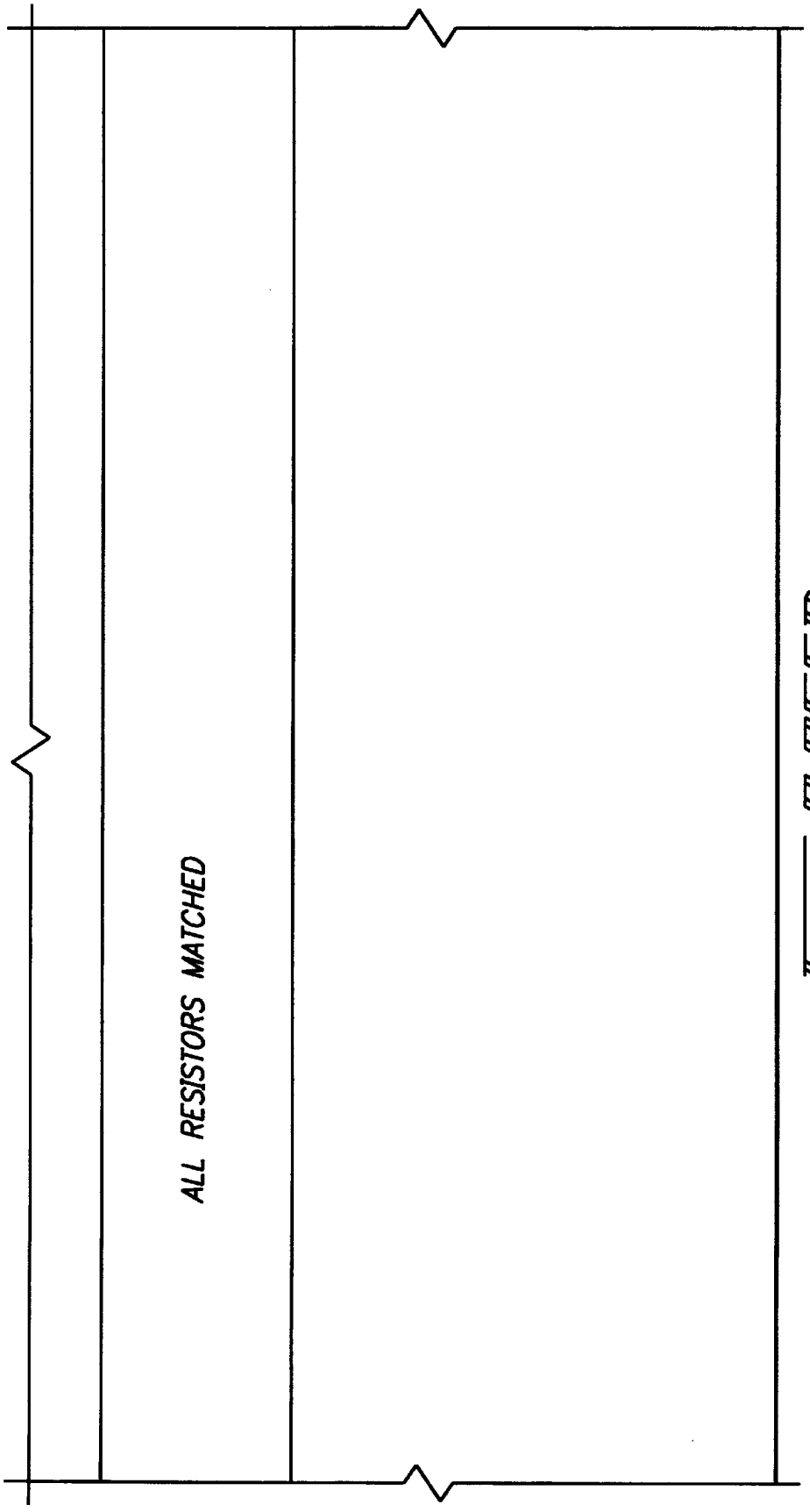
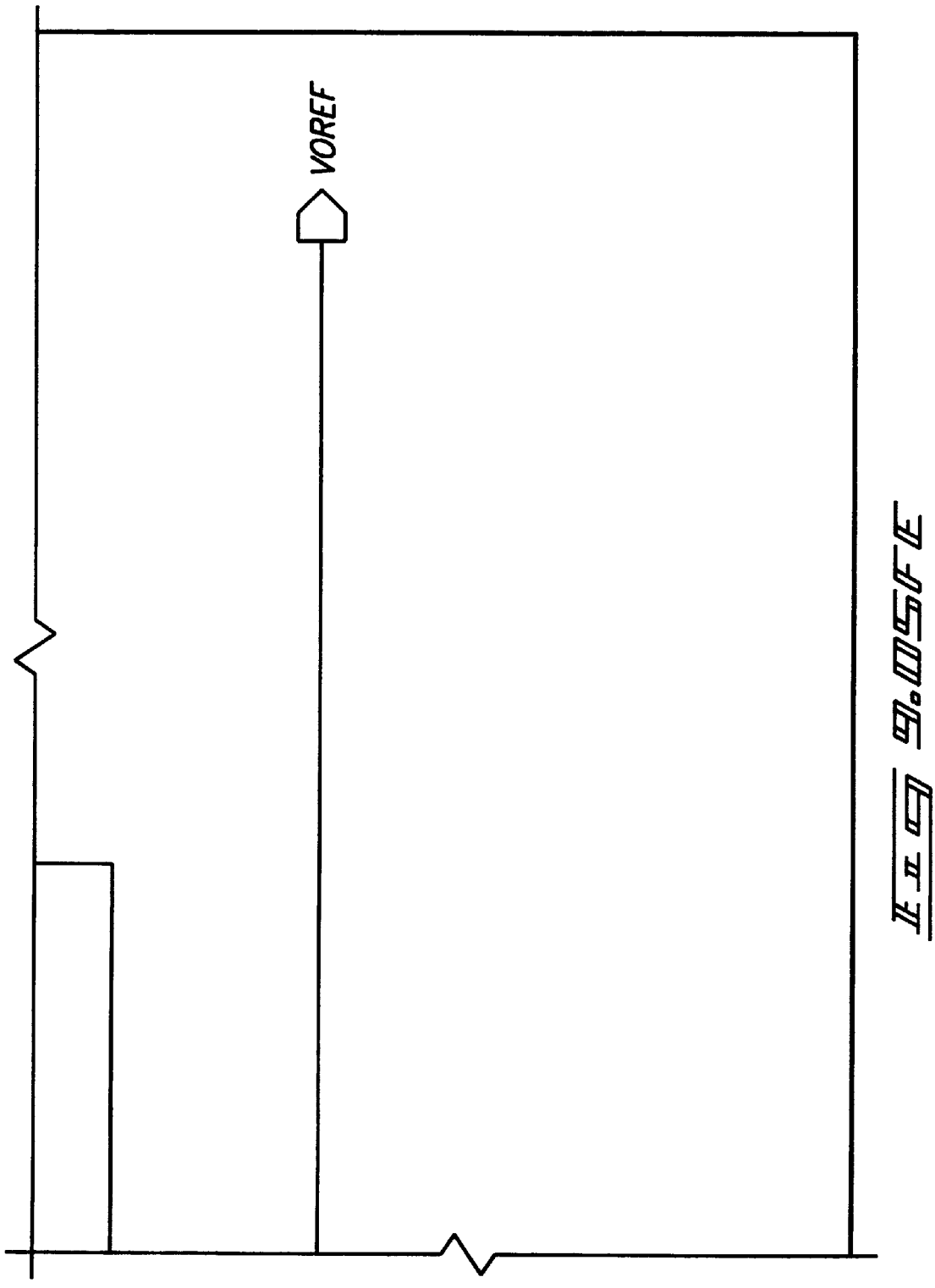


FIG 95,056


ALL RESISTORS MATCHED
FIG 91.05FD


VOREF
FIG 91.0SFE

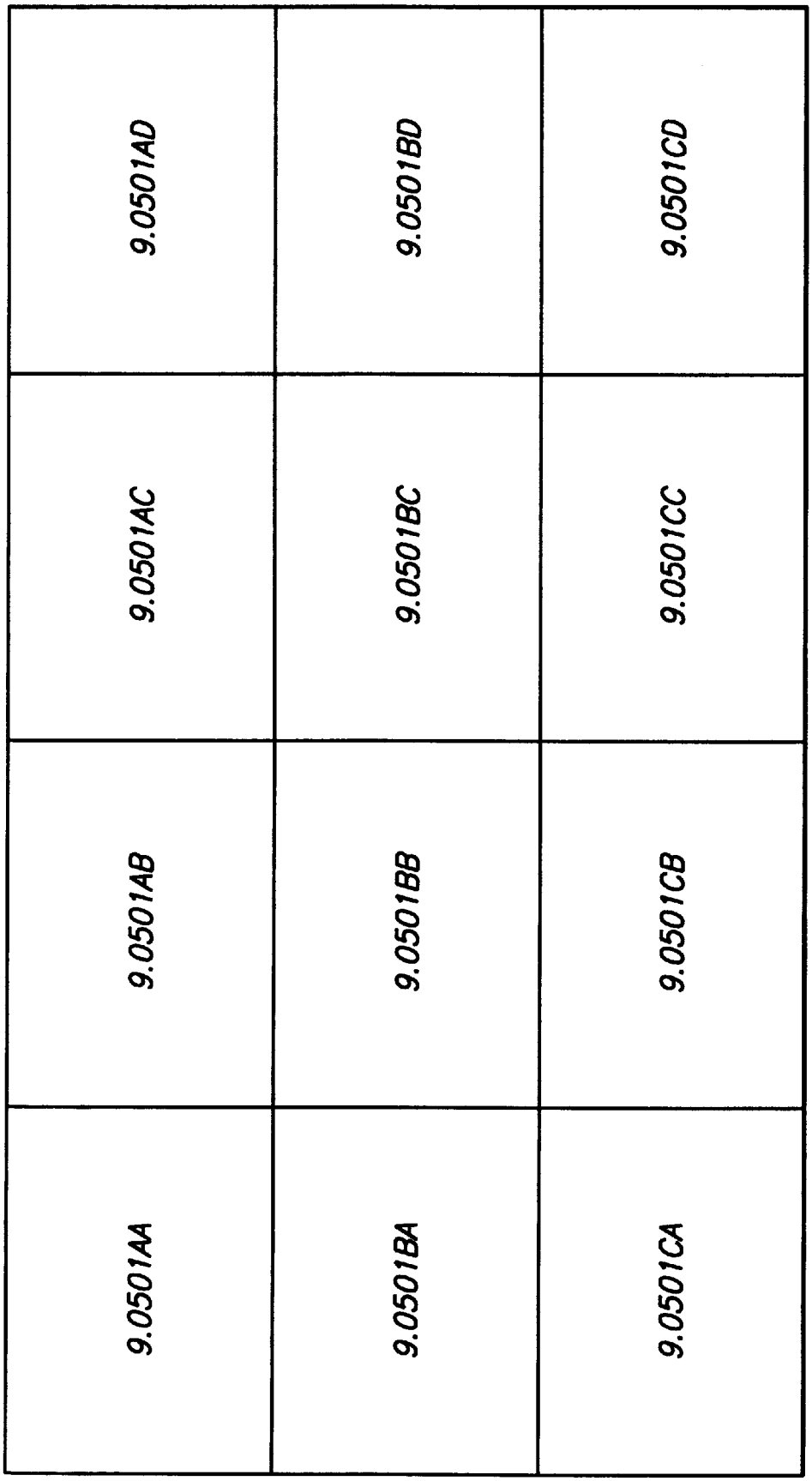

9.0501AD
9.0501BD
9.0501CD
9.0501AC
9.0501BC
9.0501CC
9.0501AB
9.0501BB
9.0501CB
9.0501AA
9.0501BA
9.0501CA

FIG. 9.0501

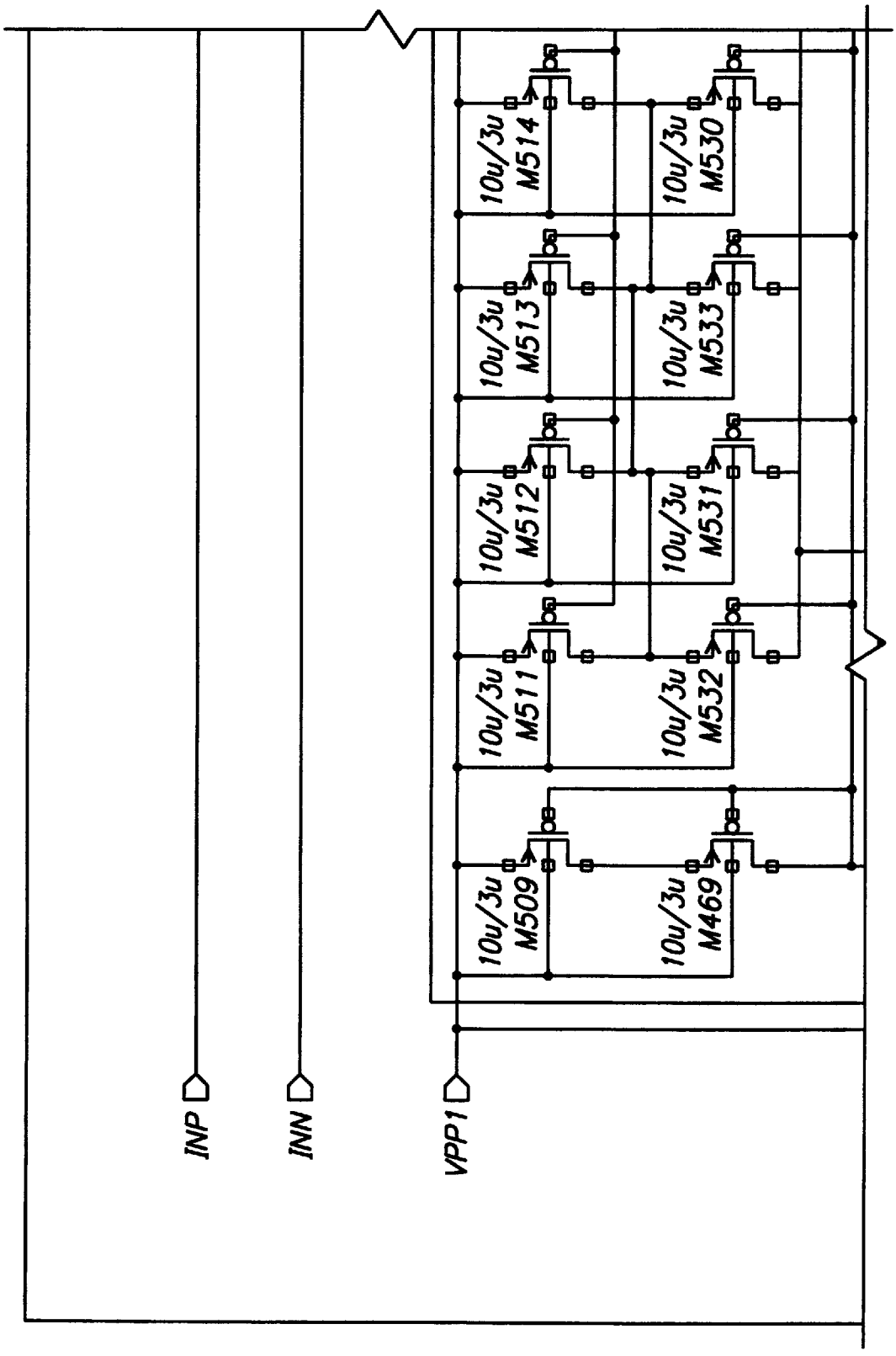


FIG 95.0501AA

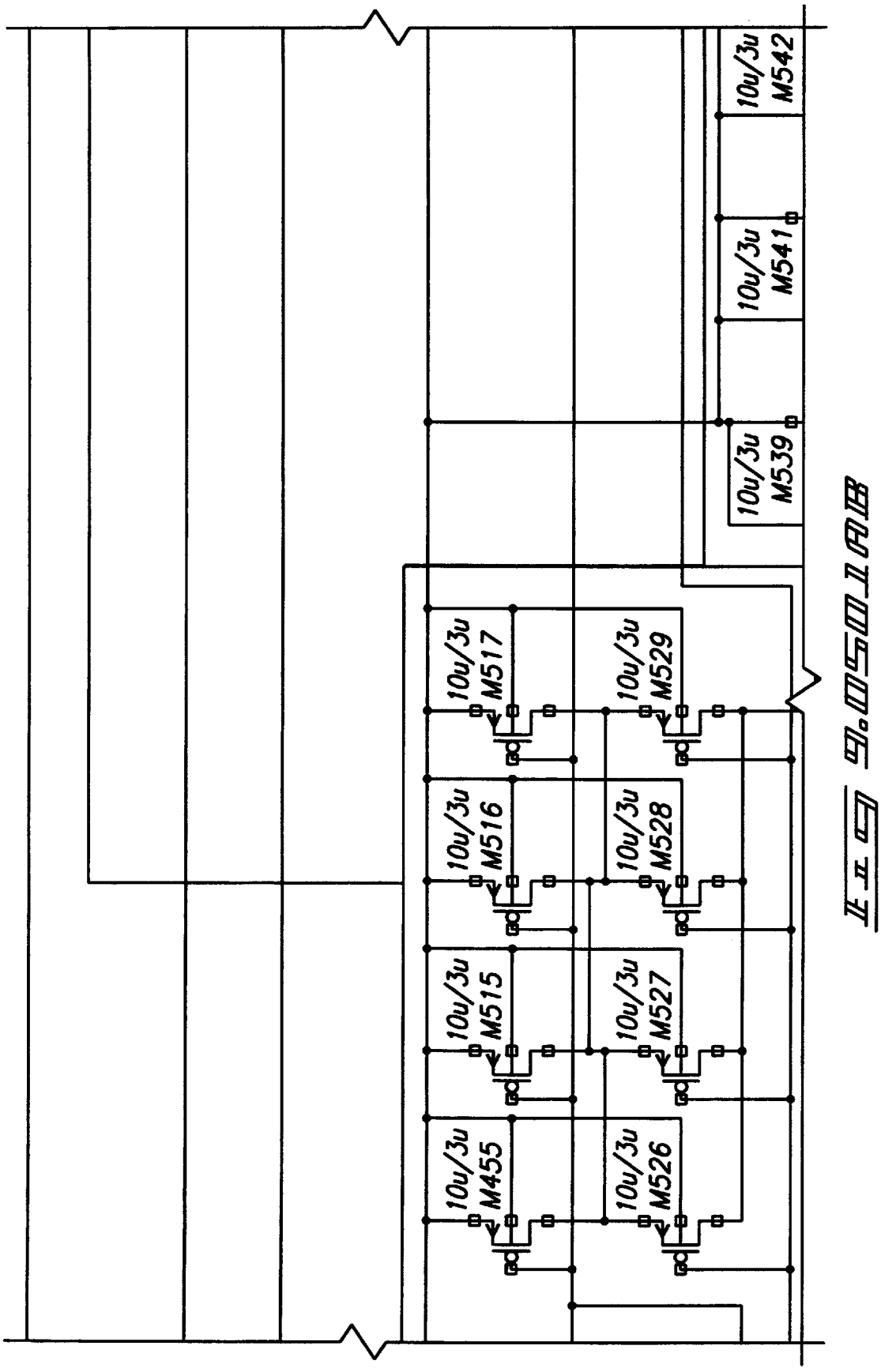

10u/3u M542
10u/3u M541
10u/3u M539
10u/3u M517
10u/3u M529
10u/3u M516
10u/3u M528
10u/3u M515
10u/3u M527
10u/3u M455
10u/3u M526

FIG. 596

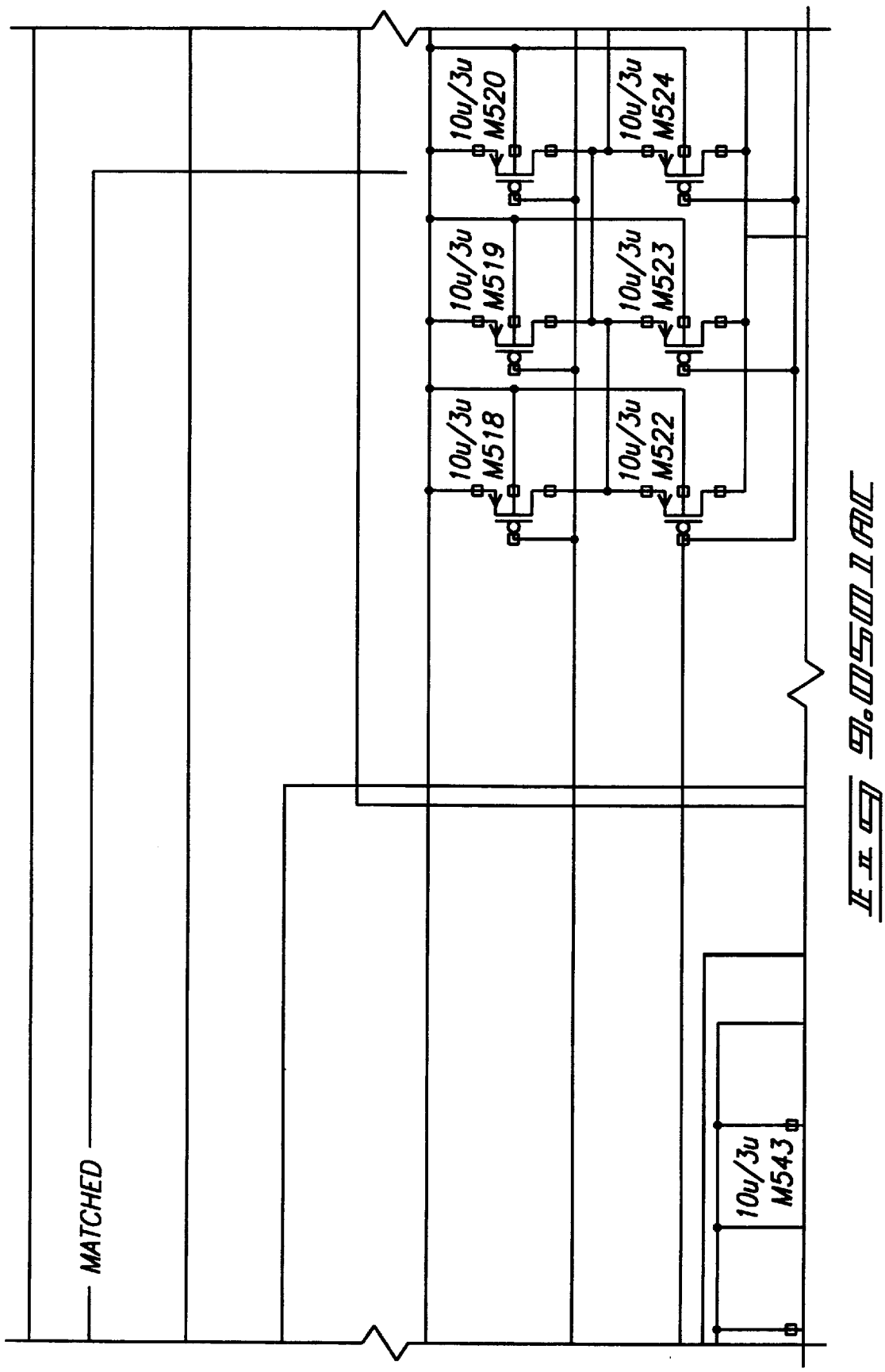

10u/3u M520
10u/3u M524
10u/3u M519
10u/3u M523
10u/3u M518
10u/3u M522
10u/3u M543
MATCHED

FIG 9.0511AC

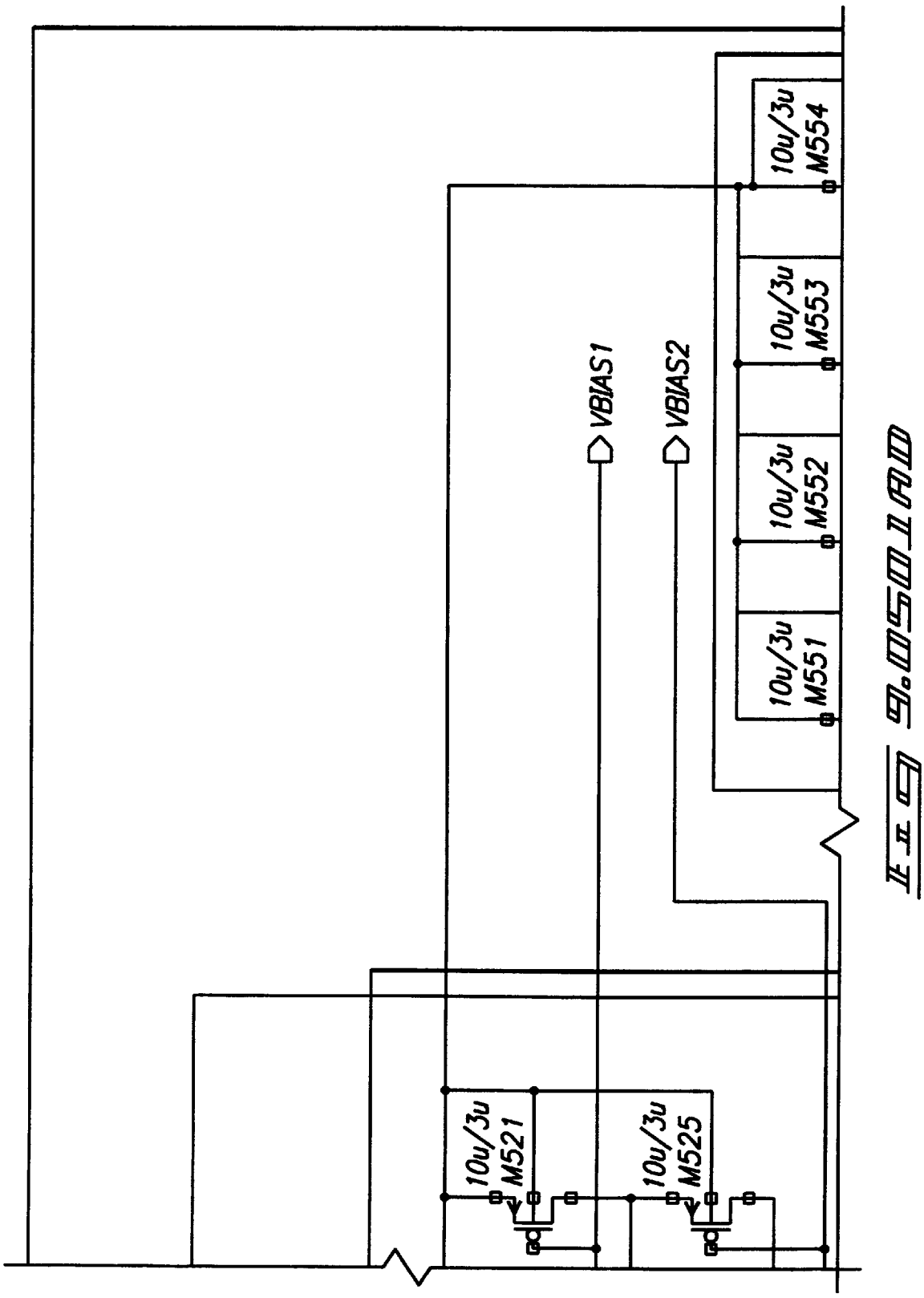
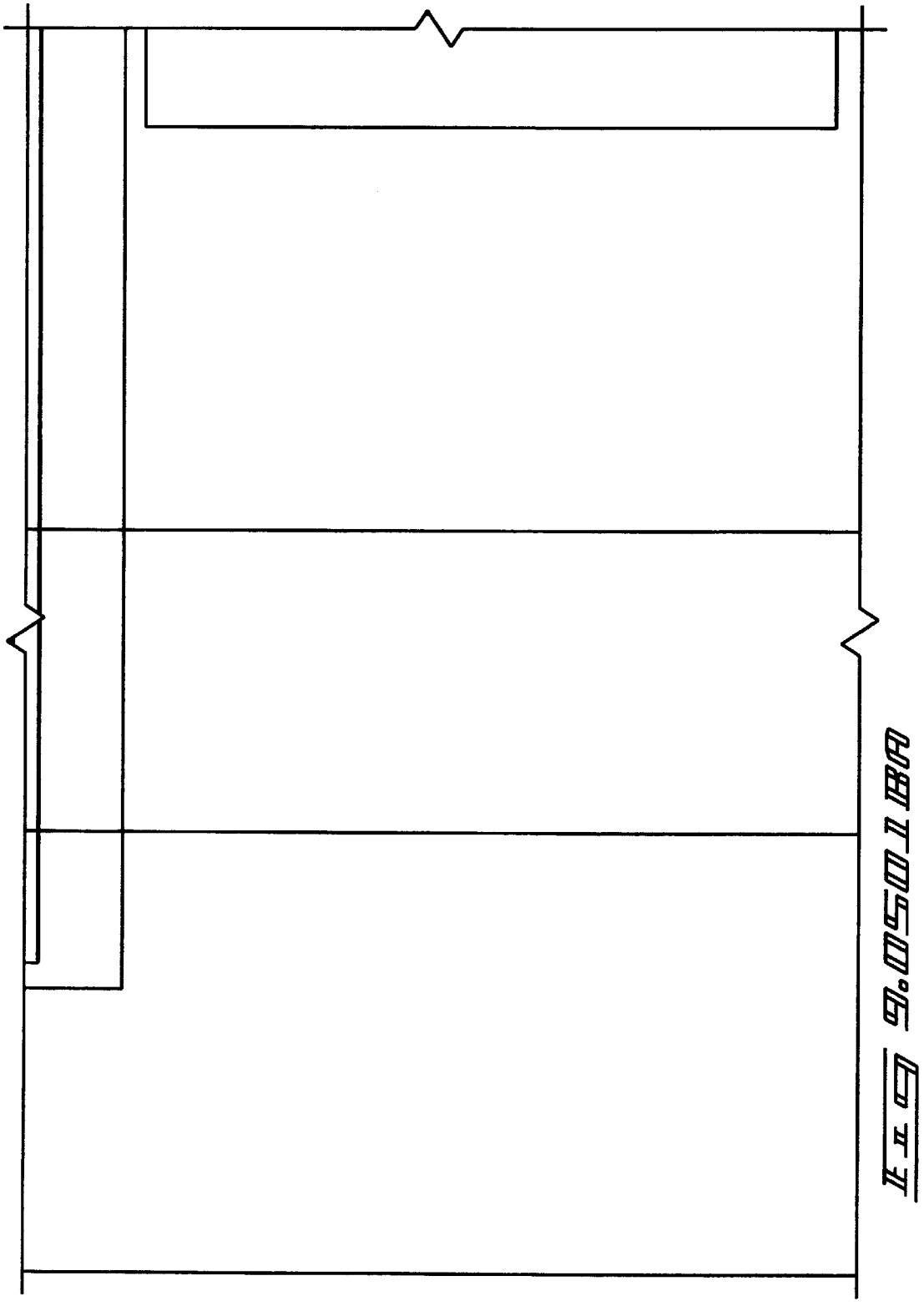

10u/3u
M554
10u/3u
M553
10u/3u
M552
10u/3u
M551
VBIAS1
VBIAS2
10u/3u
M521
10u/3u
M525

FIG 9.0501AD


WAT050.96 FIG 3T

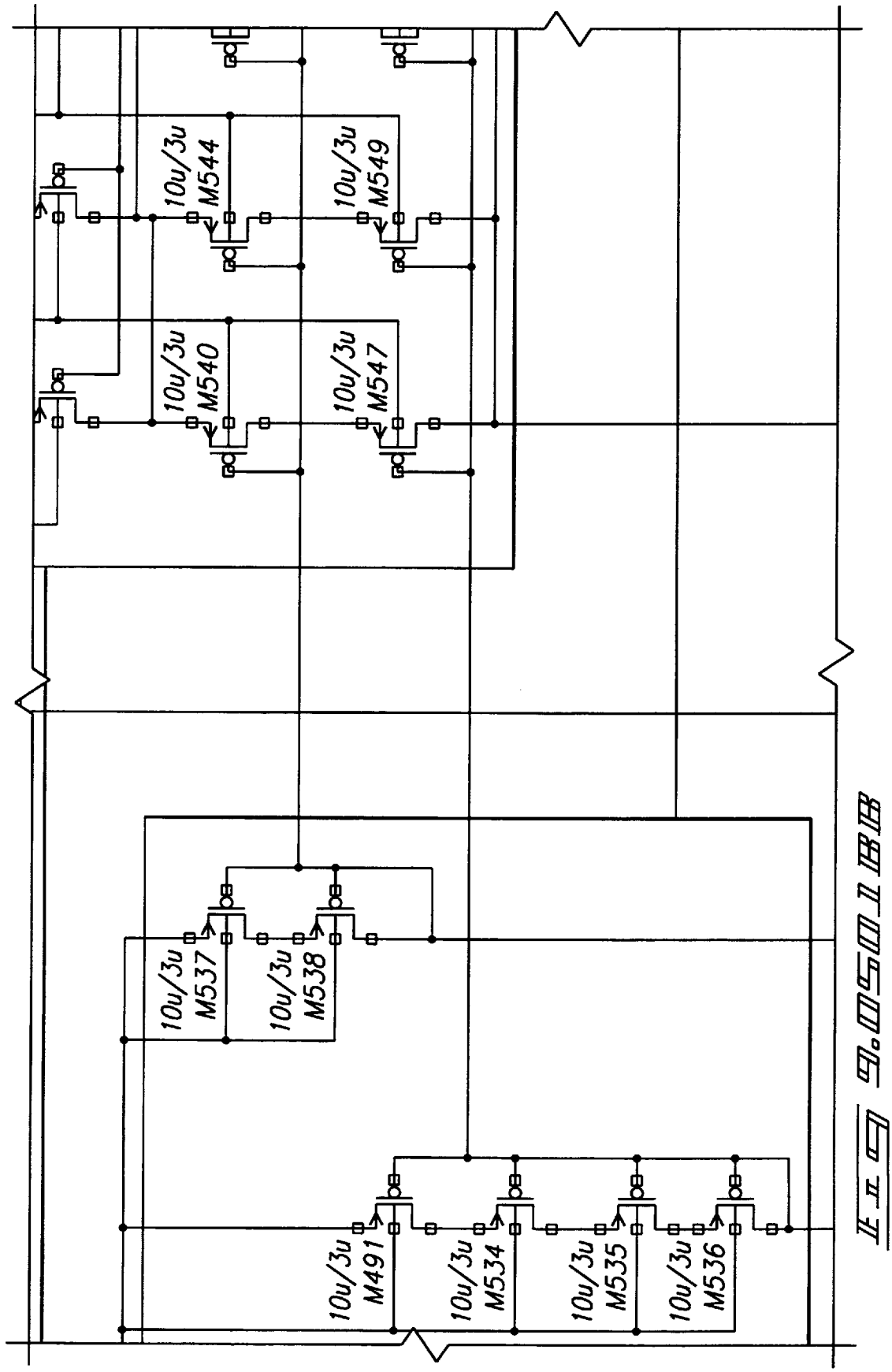

10u/3u M544
10u/3u M549
10u/3u M540
10u/3u M547
10u/3u M537
10u/3u M538
10u/3u M491
10u/3u M534
10u/3u M535
10u/3u M536

FIG 9.0501B

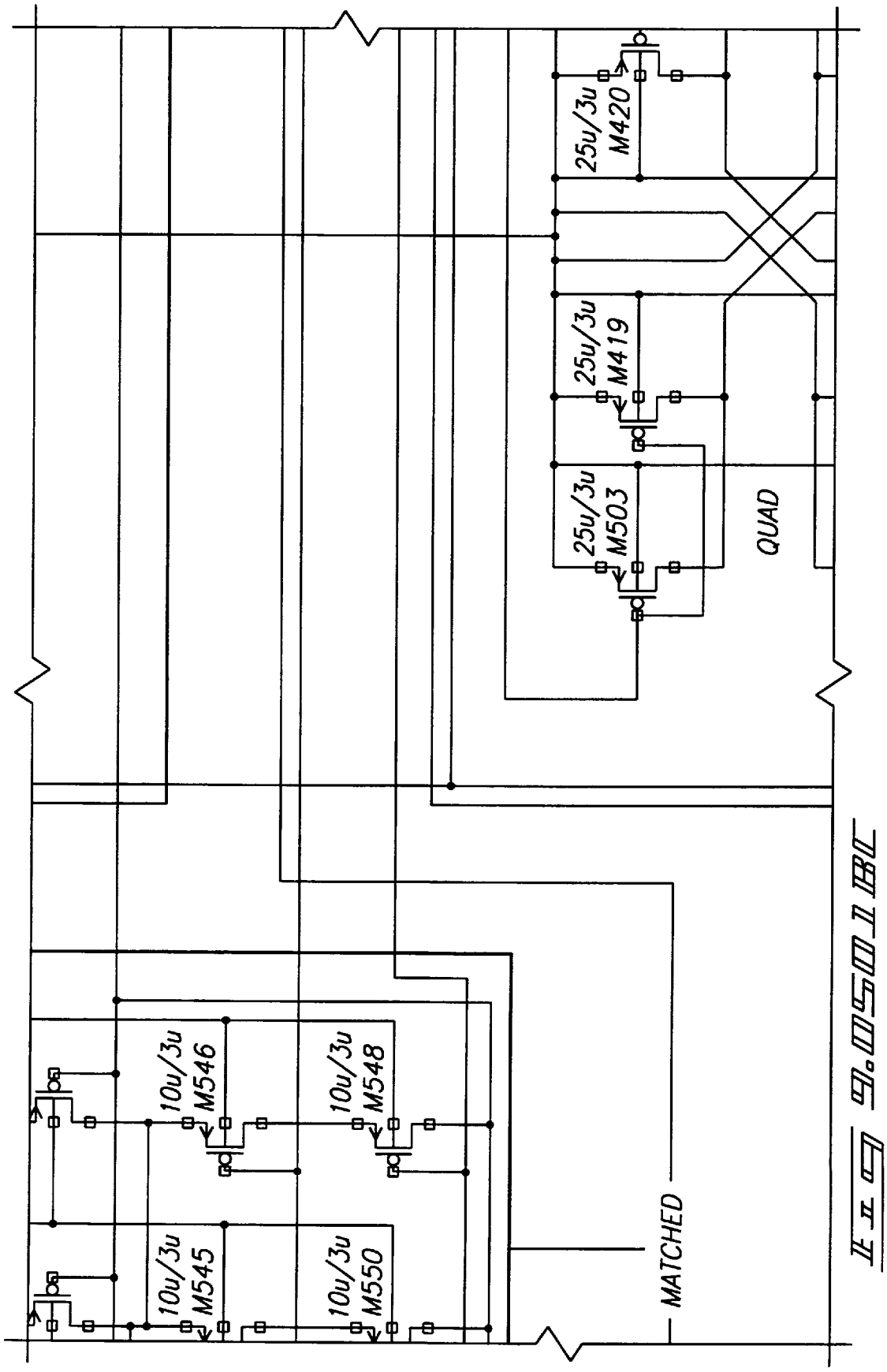


FIG 96.0501 IBC

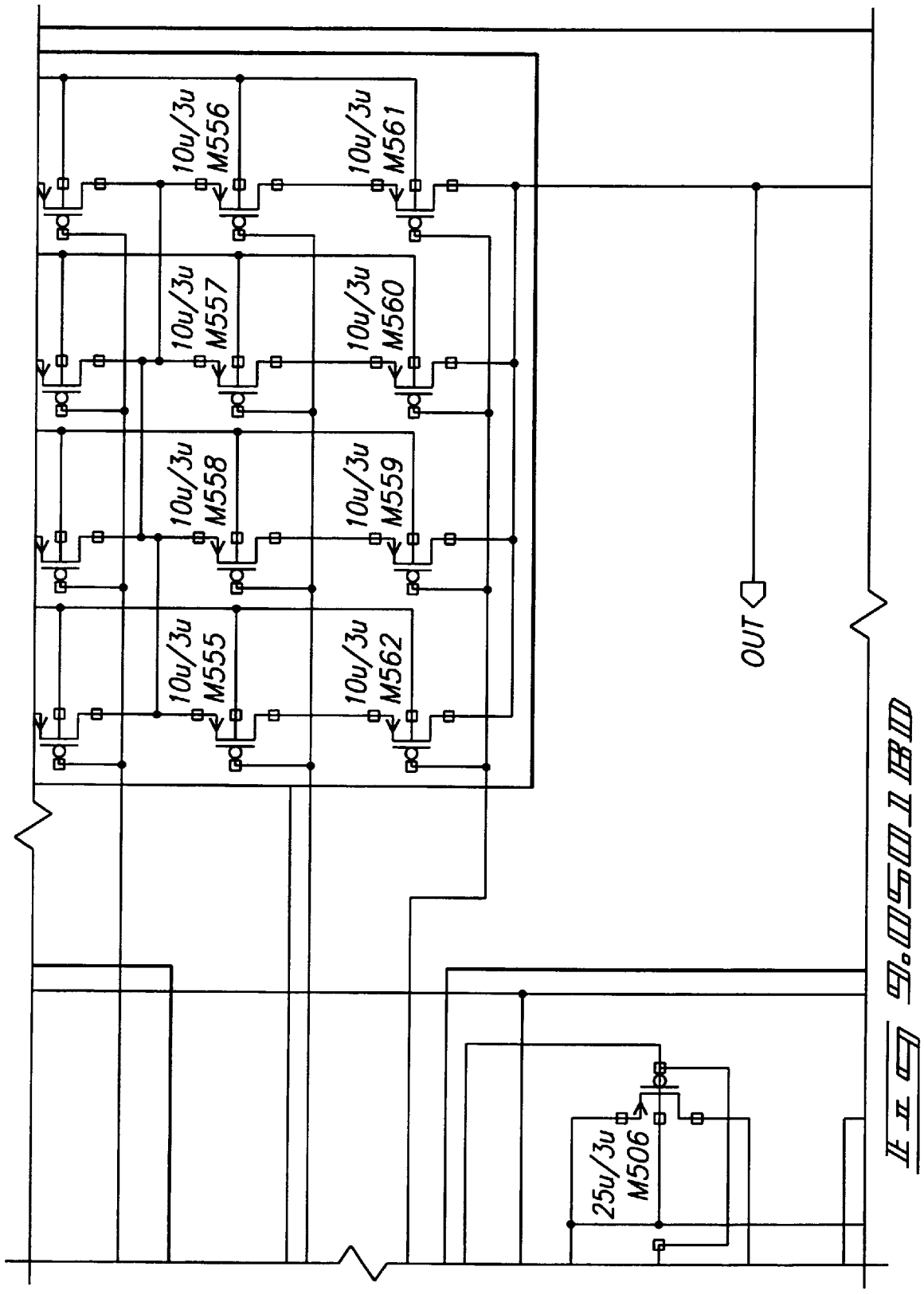

10u/3u M556
10u/3u M561
10u/3u M557
10u/3u M560
10u/3u M558
10u/3u M559
10u/3u M555
10u/3u M562
OUT
25u/3u M506

Fig 59

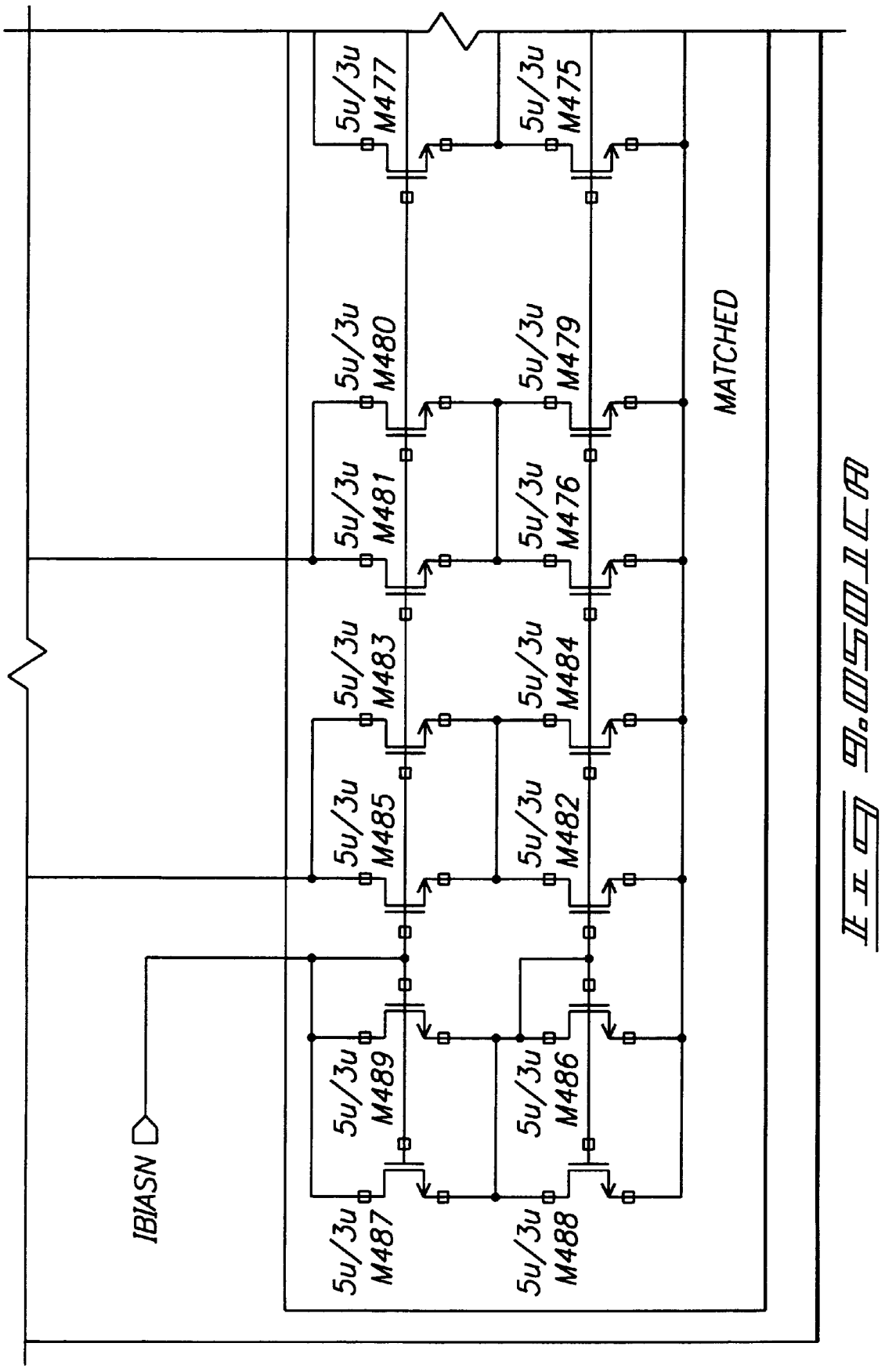

5u/3u M477
5u/3u M475
5u/3u M480
5u/3u M479
5u/3u M481
5u/3u M476
5u/3u M483
5u/3u M484
5u/3u M485
5u/3u M482
5u/3u M489
5u/3u M486
5u/3u M487
5u/3u M488
IBIASN
MATCHED

FIG. 9,005

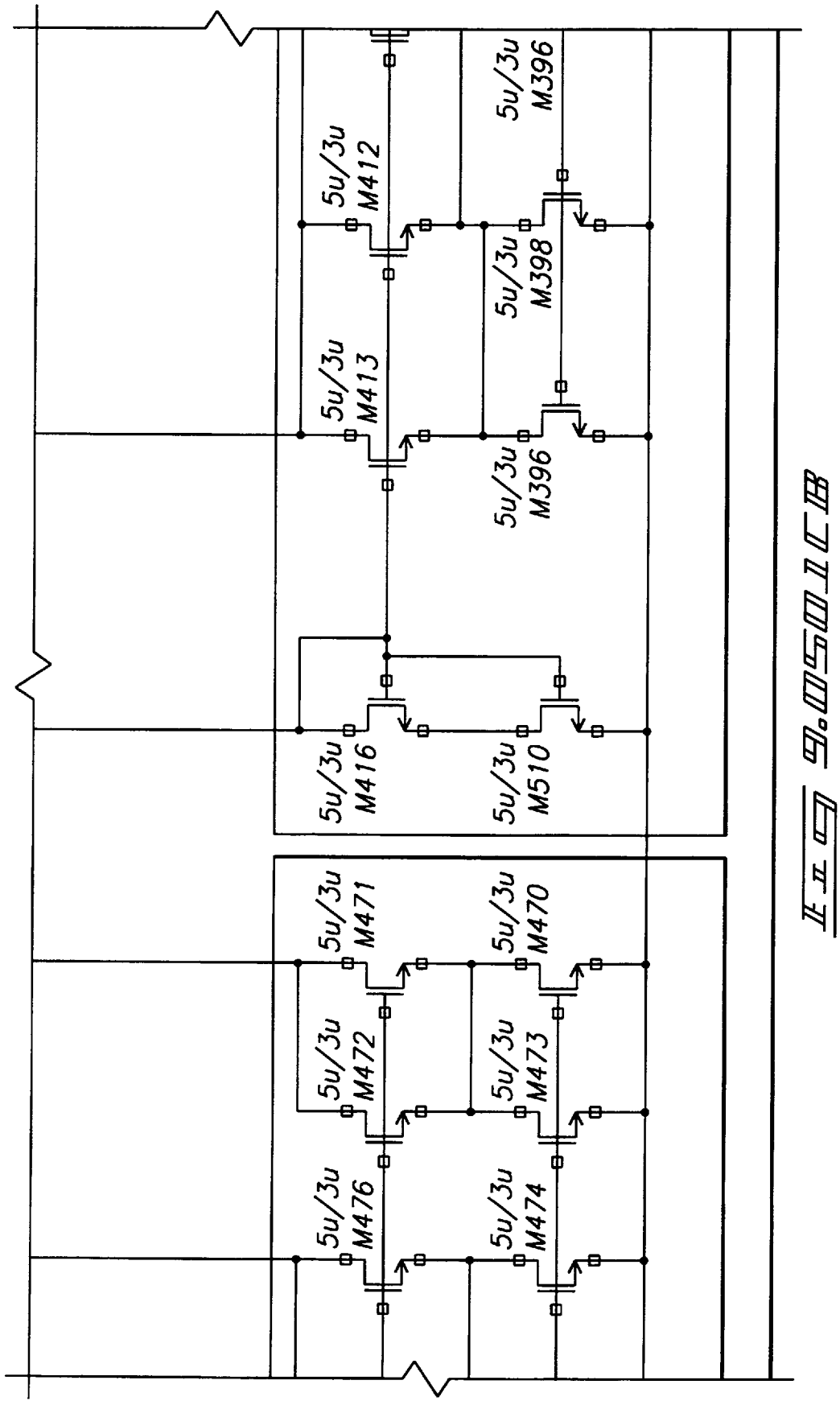

5u/3u M412
5u/3u M396
5u/3u M398
5u/3u M413
5u/3u M396
5u/3u M416
5u/3u M510
5u/3u M471
5u/3u M470
5u/3u M472
5u/3u M473
5u/3u M476
5u/3u M474

FIG. 6,050A

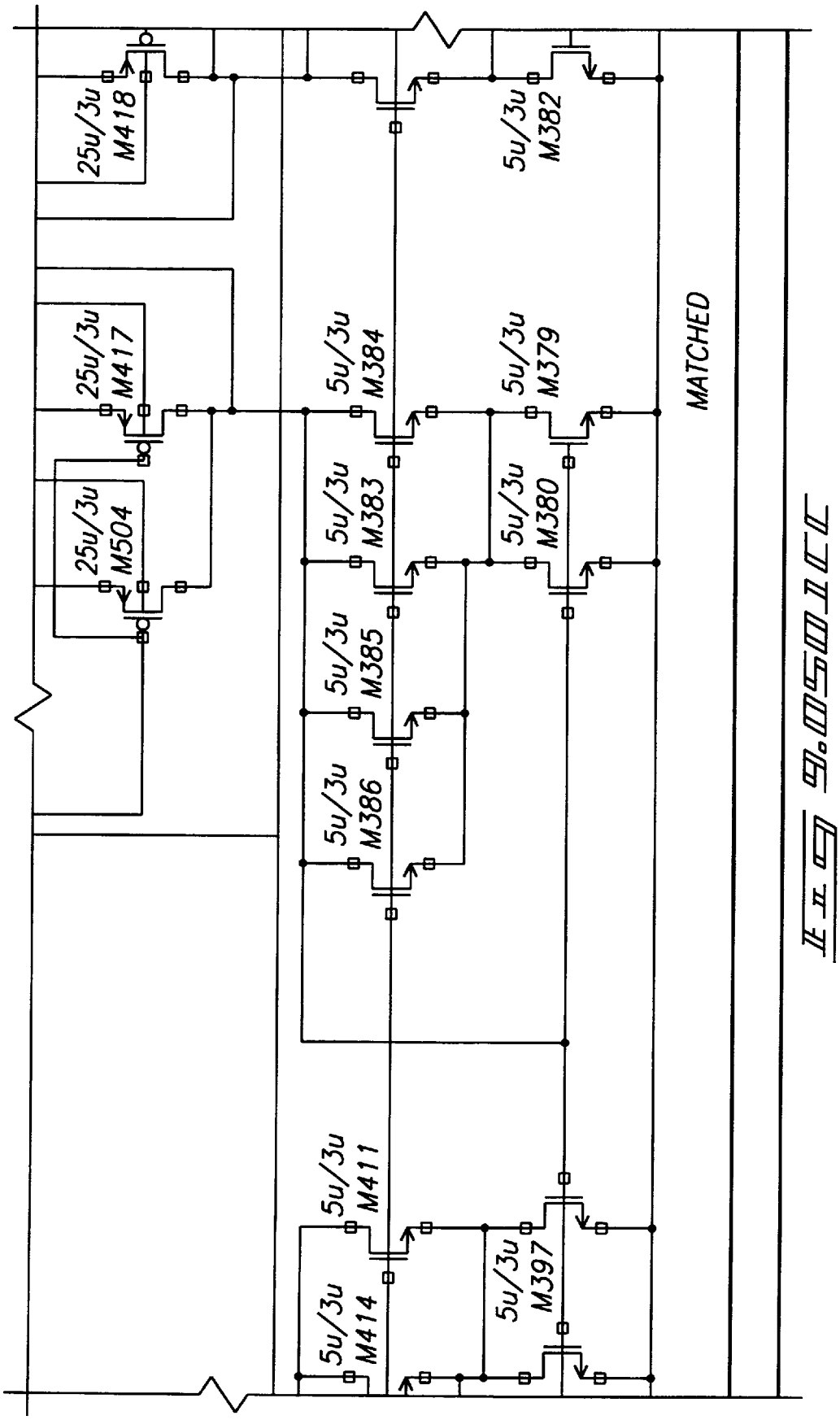

25u/3u M418
5u/3u M382
25u/3u M417
5u/3u M384
5u/3u M379
MATCHED
25u/3u M504
5u/3u M383
5u/3u M380
5u/3u M385
5u/3u M386
5u/3u M411
5u/3u M414
5u/3u M397

FIG 9.0501

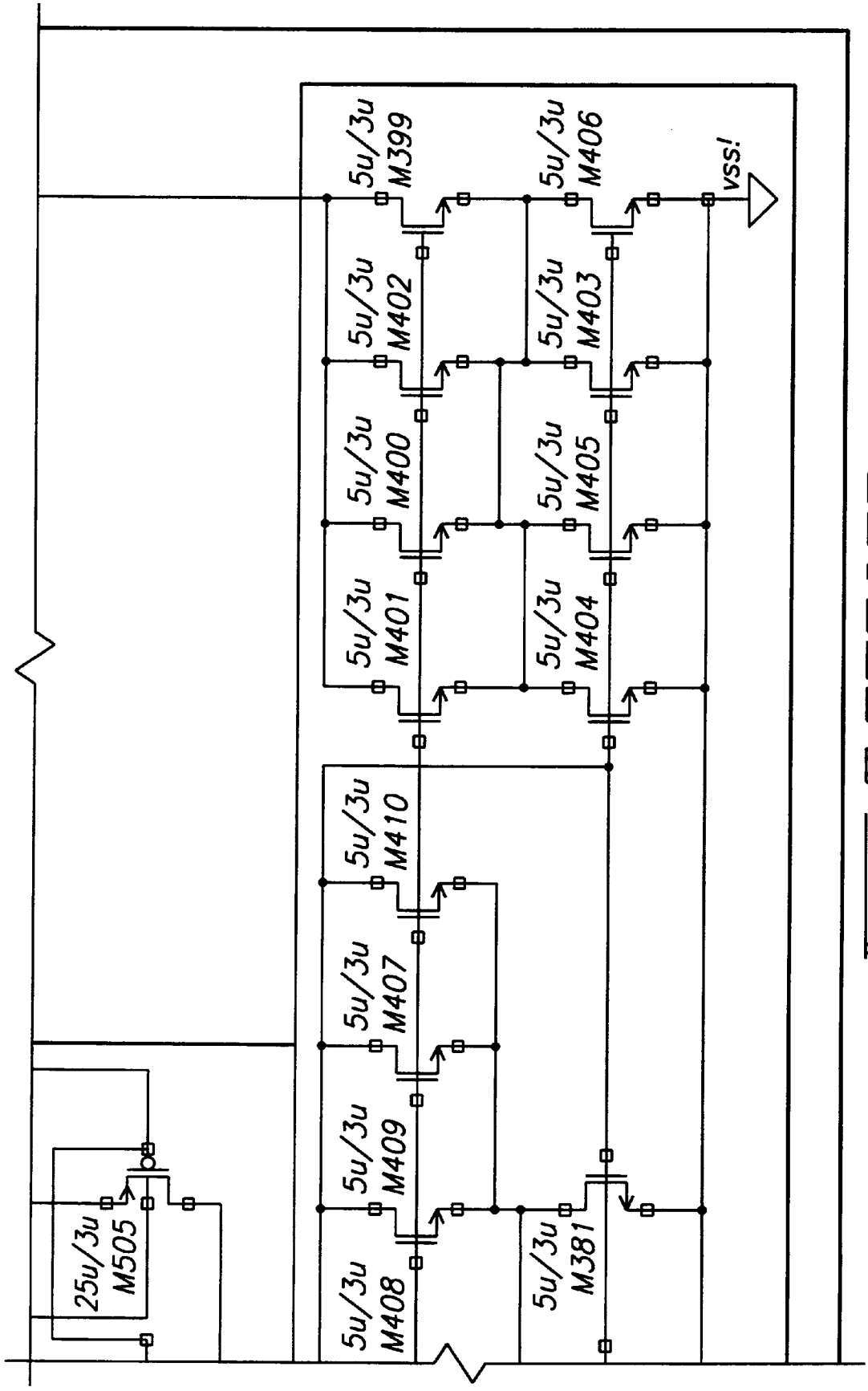

5u/3u M399
5u/3u M406
vss!
5u/3u M402
5u/3u M403
5u/3u M400
5u/3u M405
5u/3u M401
5u/3u M404
5u/3u M410
5u/3u M407
5u/3u M409
5u/3u M408
5u/3u M381
25u/3u M505

FIG 9,050

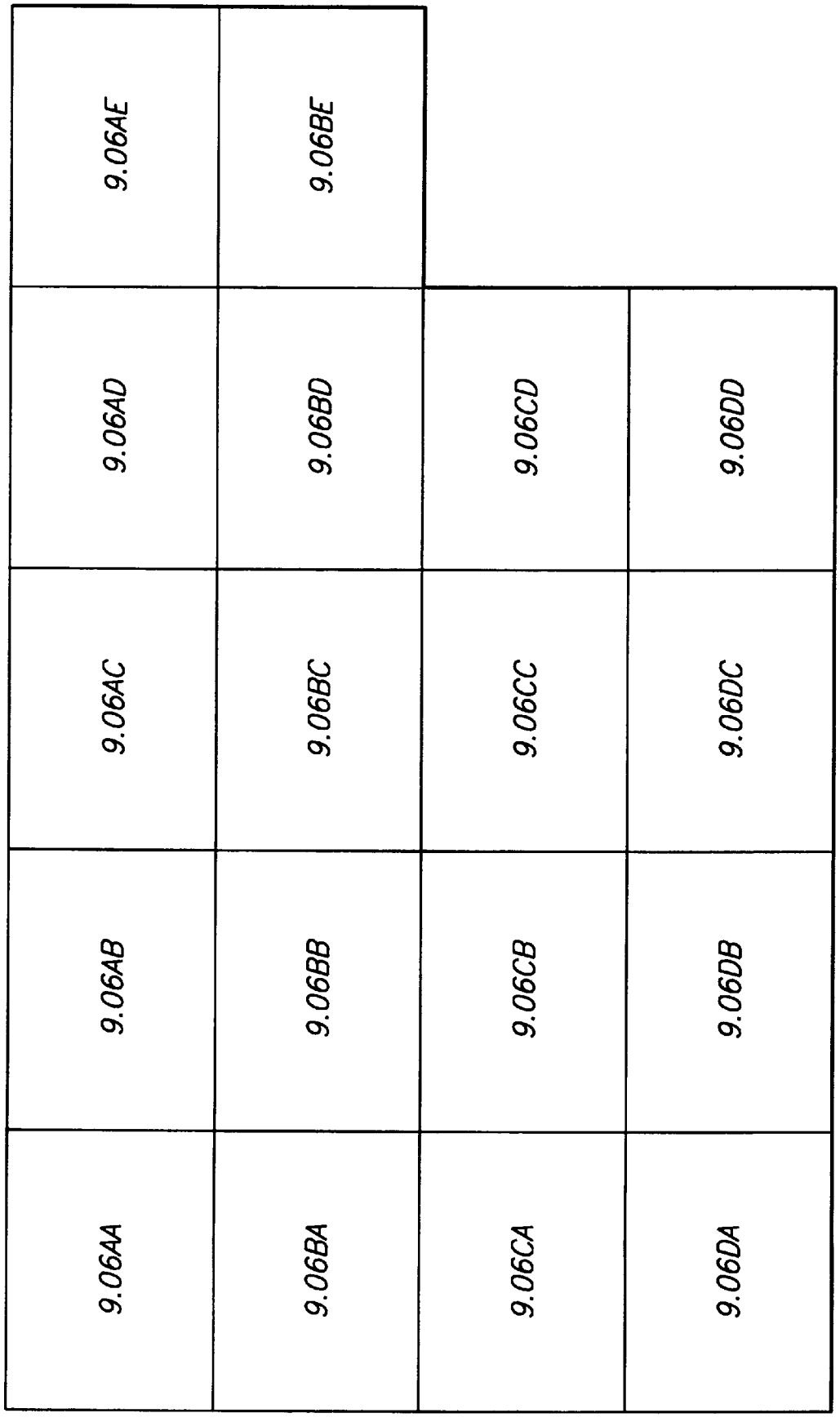

9.06AE
9.06BE
9.06AD
9.06BD
9.06CD
9.06DD
9.06AC
9.06BC
9.06CC
9.06DC
9.06AB
9.06BB
9.06CB
9.06DB
9.06AA
9.06BA
9.06CA
9.06DA

FIG. 9.605

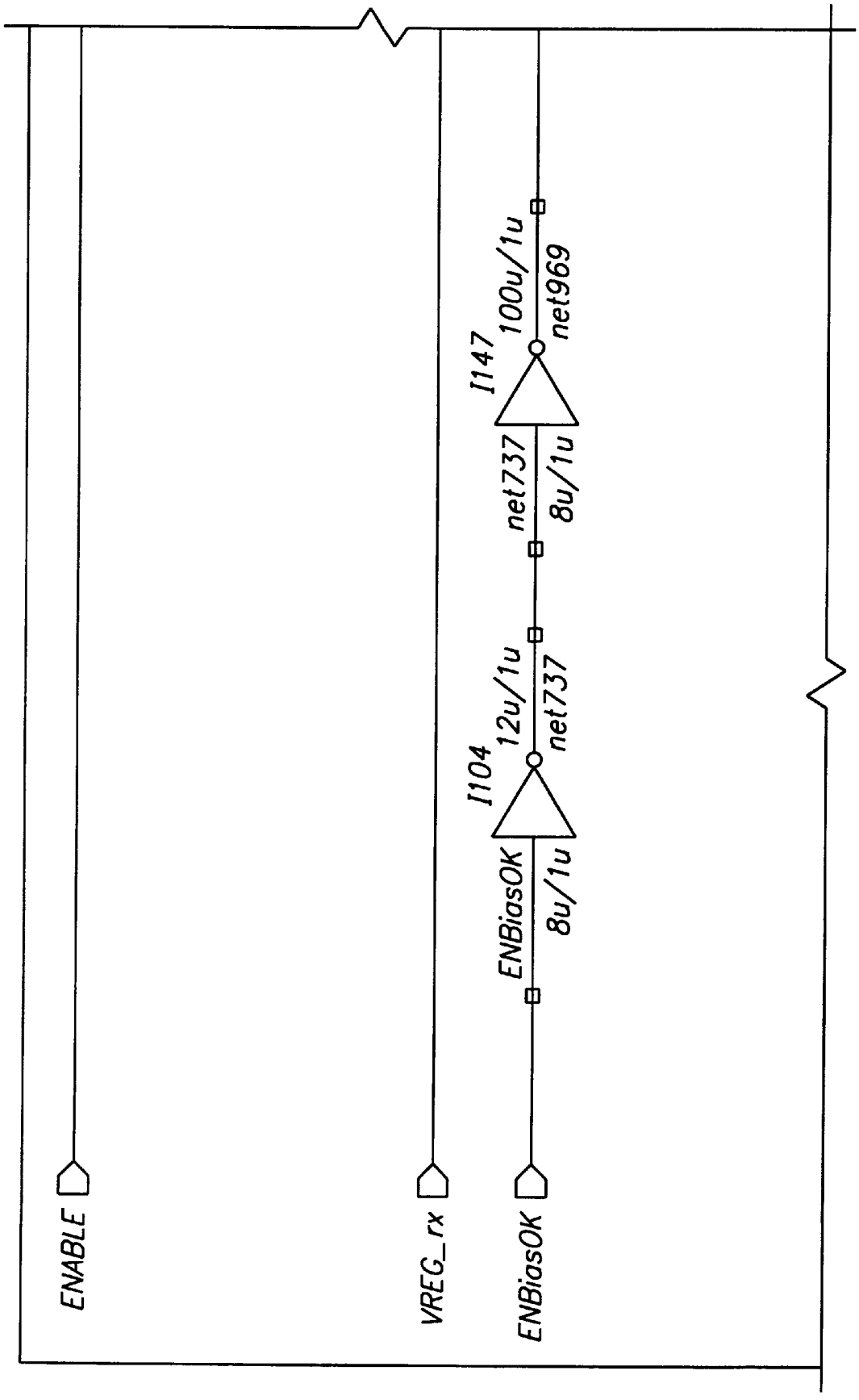

ENABLE
VREG_rx
ENBiasOK
ENBiasOK
I104
12u/1u
net737
8u/1u
I147
100u/1u
net969
net737
8u/1u

FIG 9.0GHA

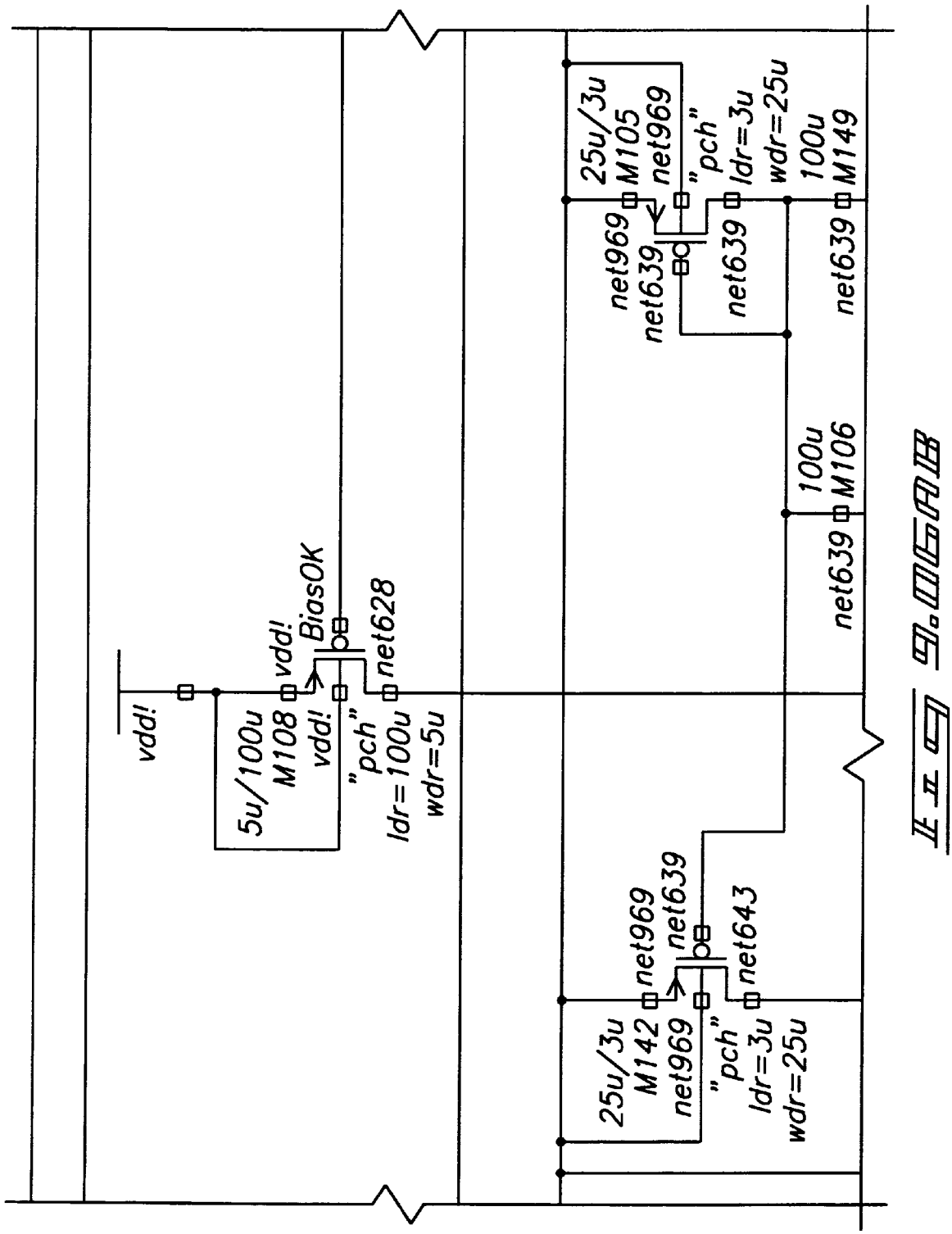
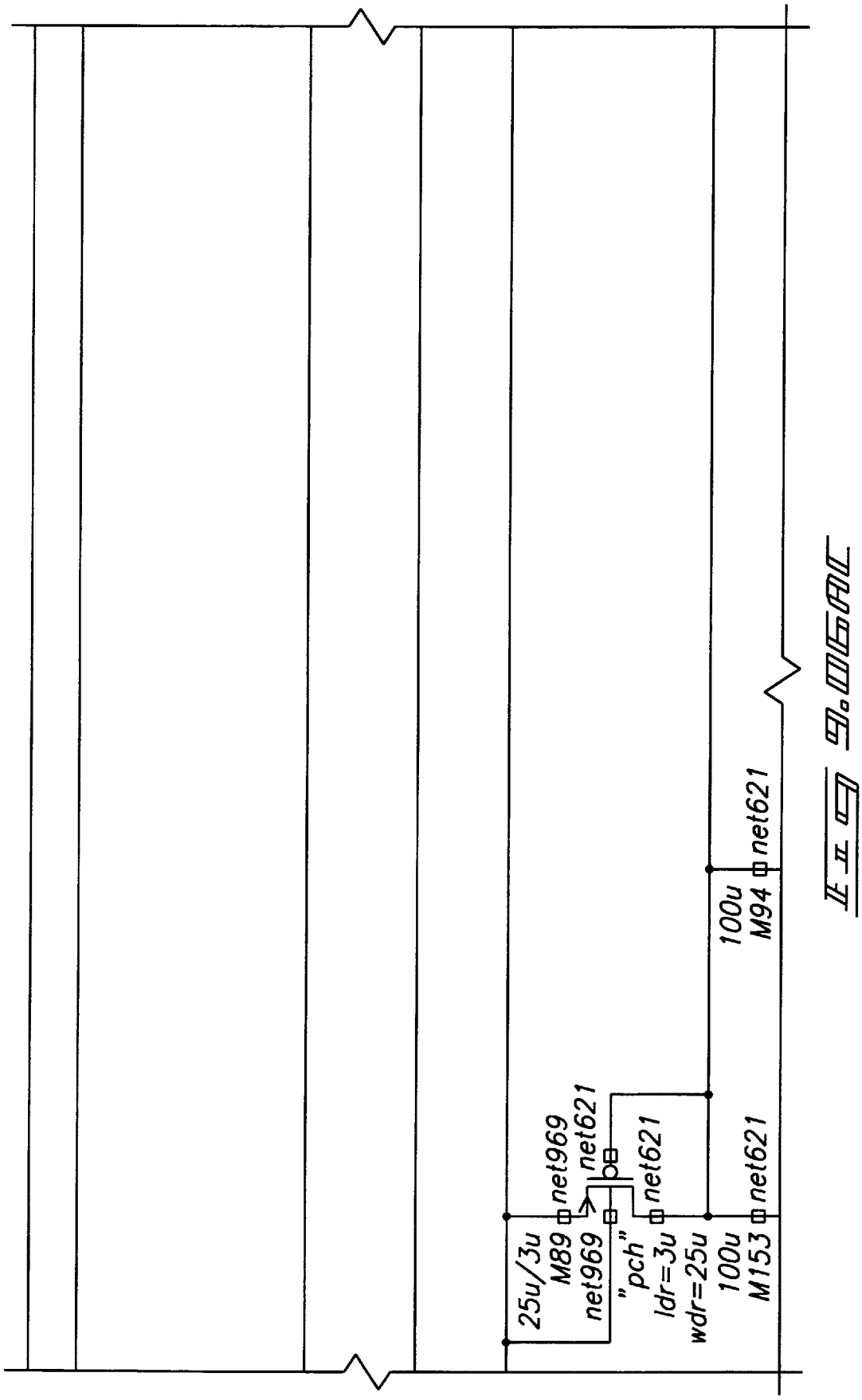

vdd!
5u/100u
M108
vdd!
"pch"
ldr=100u
wdr=5u
vdd!
BiasOK
net628
net969
net639
25u/3u
M142
net969
"pch"
ldr=3u
wdr=25u
net643
net639
100u
M106
net639
net969
net639
25u/3u
M105
net969
"pch"
ldr=3u
wdr=25u
100u
M149
net639

Fig. 9,085,AB


25u/3u
M89
net969
net969
"pch"
ldr=3u
wdr=25u
net621
net621
100u
M153
net621
100u
M94

Фиг 9.0548

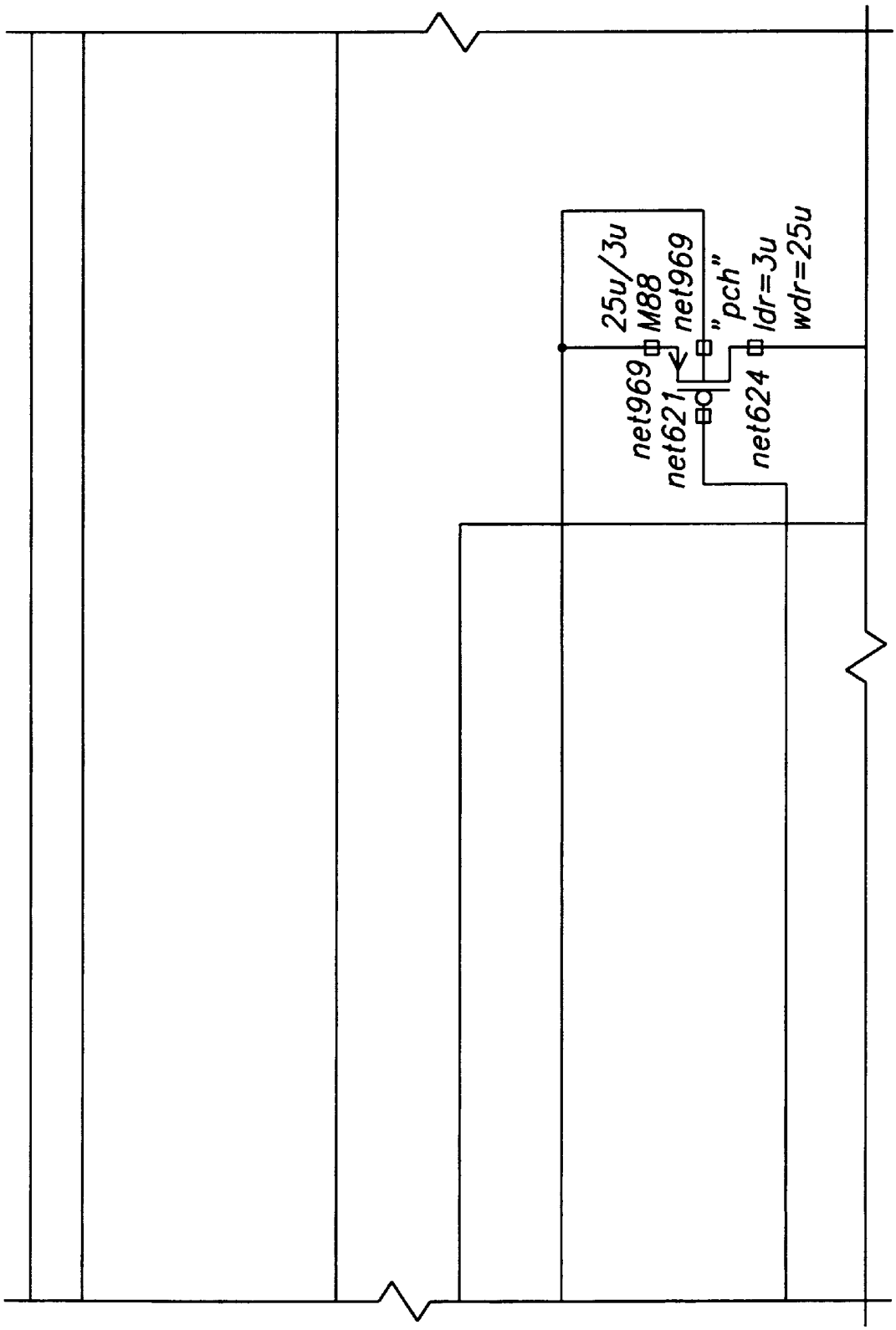


FIG 9,056,AD

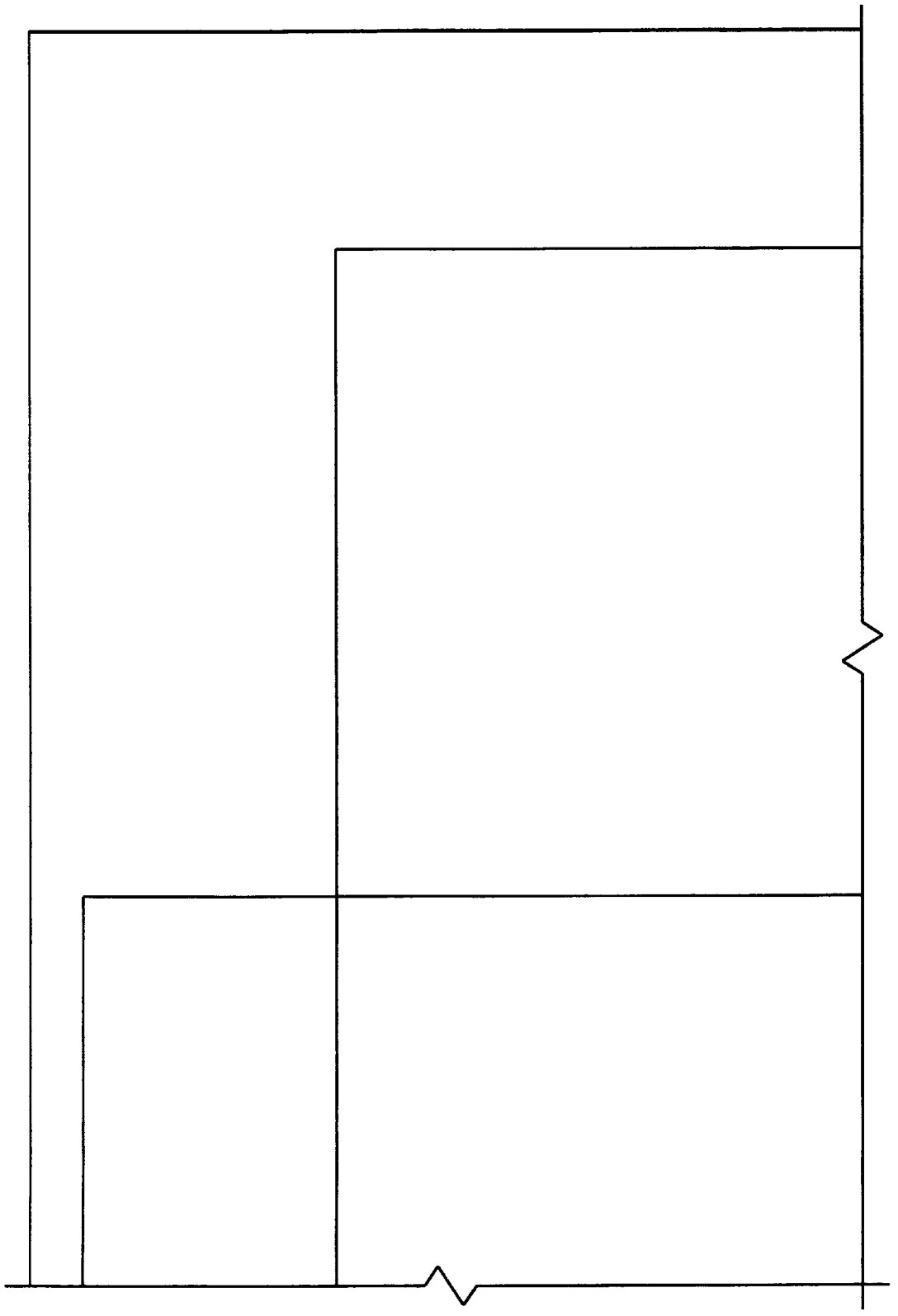
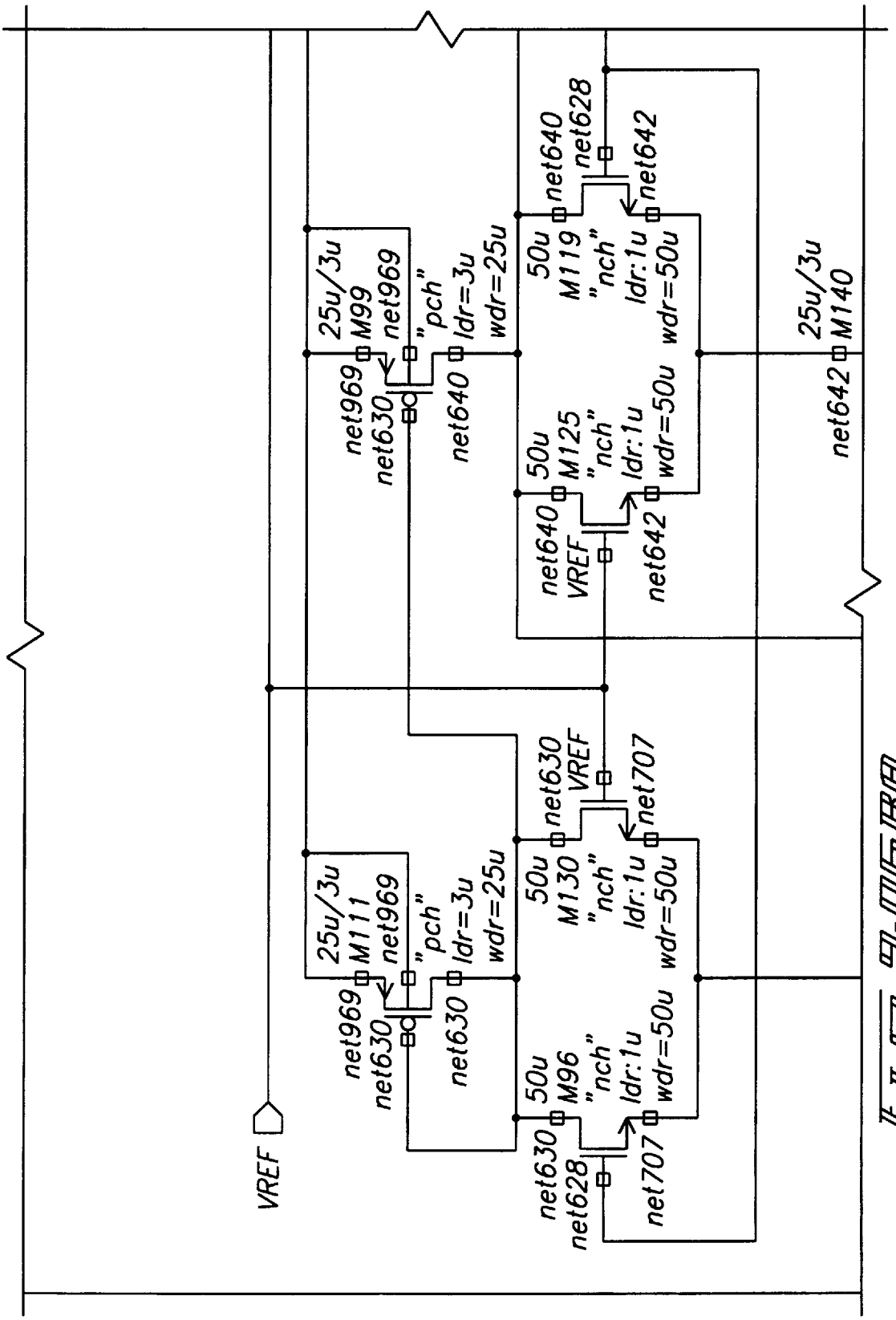


FIG 9.0GAE


VREF
net628
net640
net642
net630
net707
net969
net1630
25u/3u
M99
M111
M140
"pch"
"nch"
ldr=3u
ldr:1u
wdr=25u
wdr=50u
50u
M119
M125
M130
M96
VREF

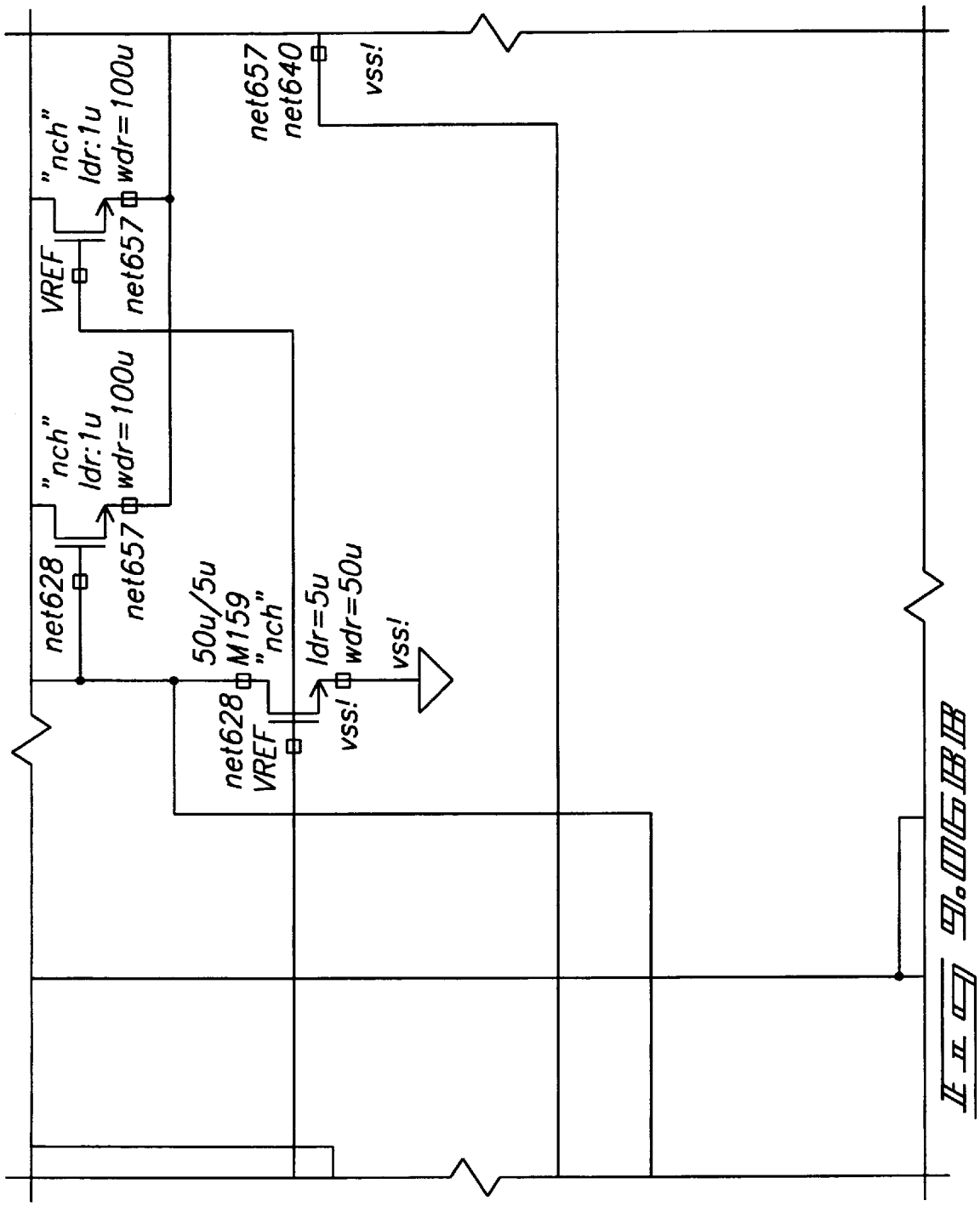

net657
net640
vss!
"nch"
ldr:1u
wdr=100u
VREF
net657
"nch"
ldr:1u
wdr=100u
net628
net657
50u/5u
M159
"nch"
ldr=5u
wdr=50u
vss!
net628
VREF
vss!

FIG. 59,008B

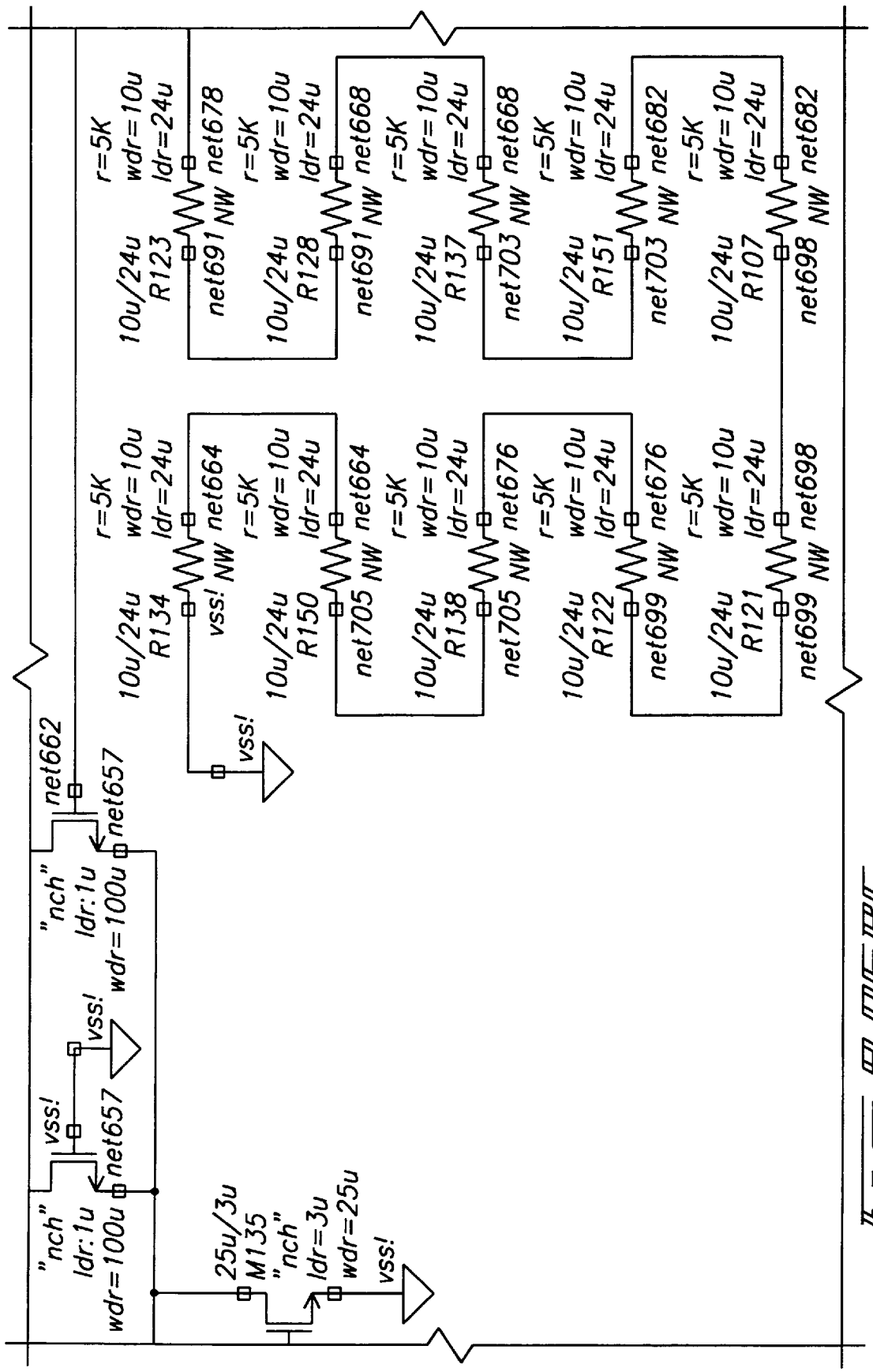


FIG. 91,006,IBIC

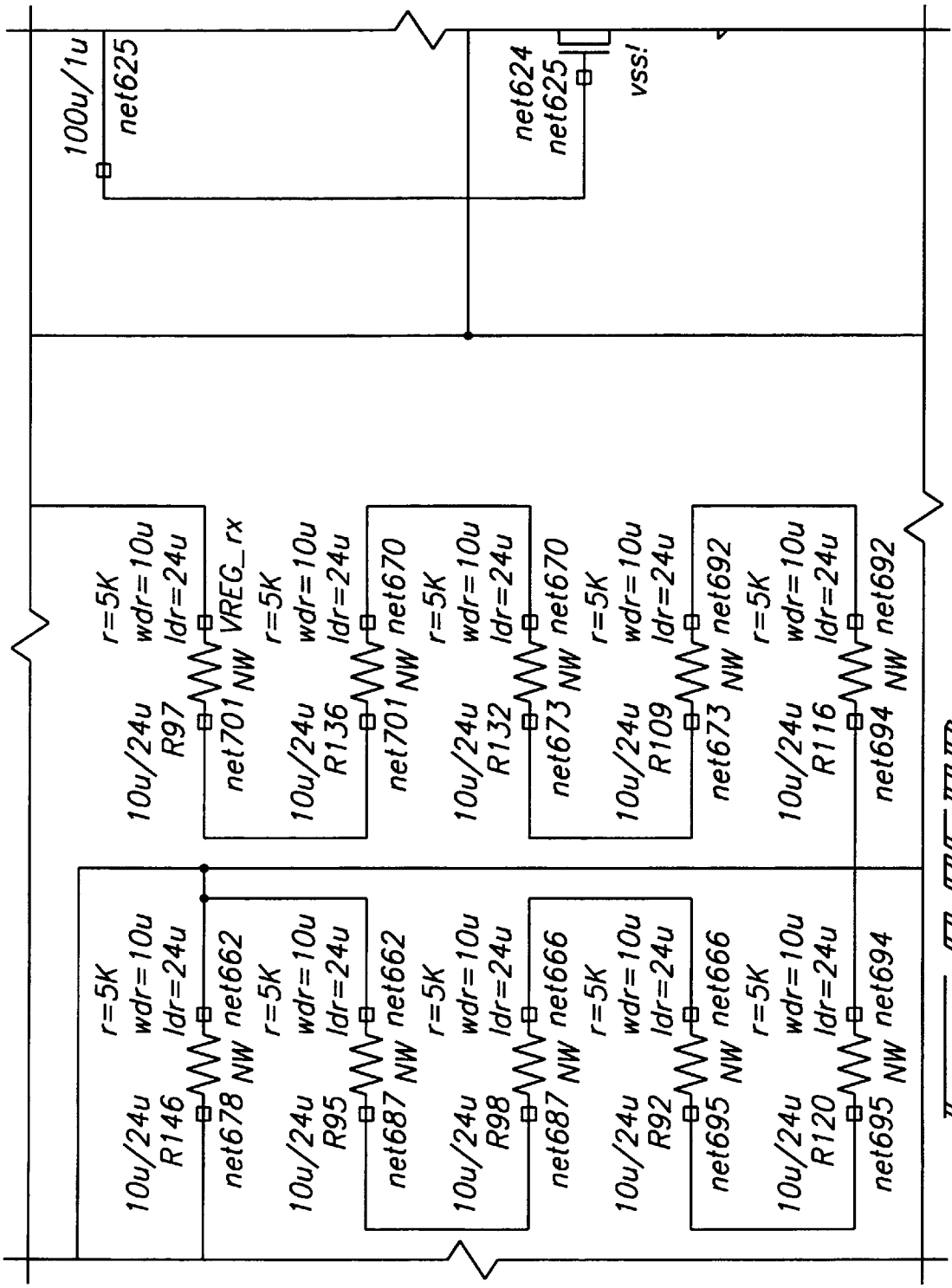

100u/1u
net625
net624
net625
vss!
10u/24u R97 net701 NW r=5K wdr=10u ldr=24u VREG_rx
10u/24u R136 net701 NW r=5K wdr=10u ldr=24u net670
10u/24u R132 net673 NW r=5K wdr=10u ldr=24u net670
10u/24u R109 net673 NW r=5K wdr=10u ldr=24u net692
10u/24u R116 net694 NW r=5K wdr=10u ldr=24u net692
10u/24u R146 net678 NW r=5K wdr=10u ldr=24u net662
10u/24u R95 net687 NW r=5K wdr=10u ldr=24u net662
10u/24u R98 net687 NW r=5K wdr=10u ldr=24u net666
10u/24u R92 net695 NW r=5K wdr=10u ldr=24u net666
10u/24u R120 net695 NW r=5K wdr=10u ldr=24u net694

FIG. 9,005,181

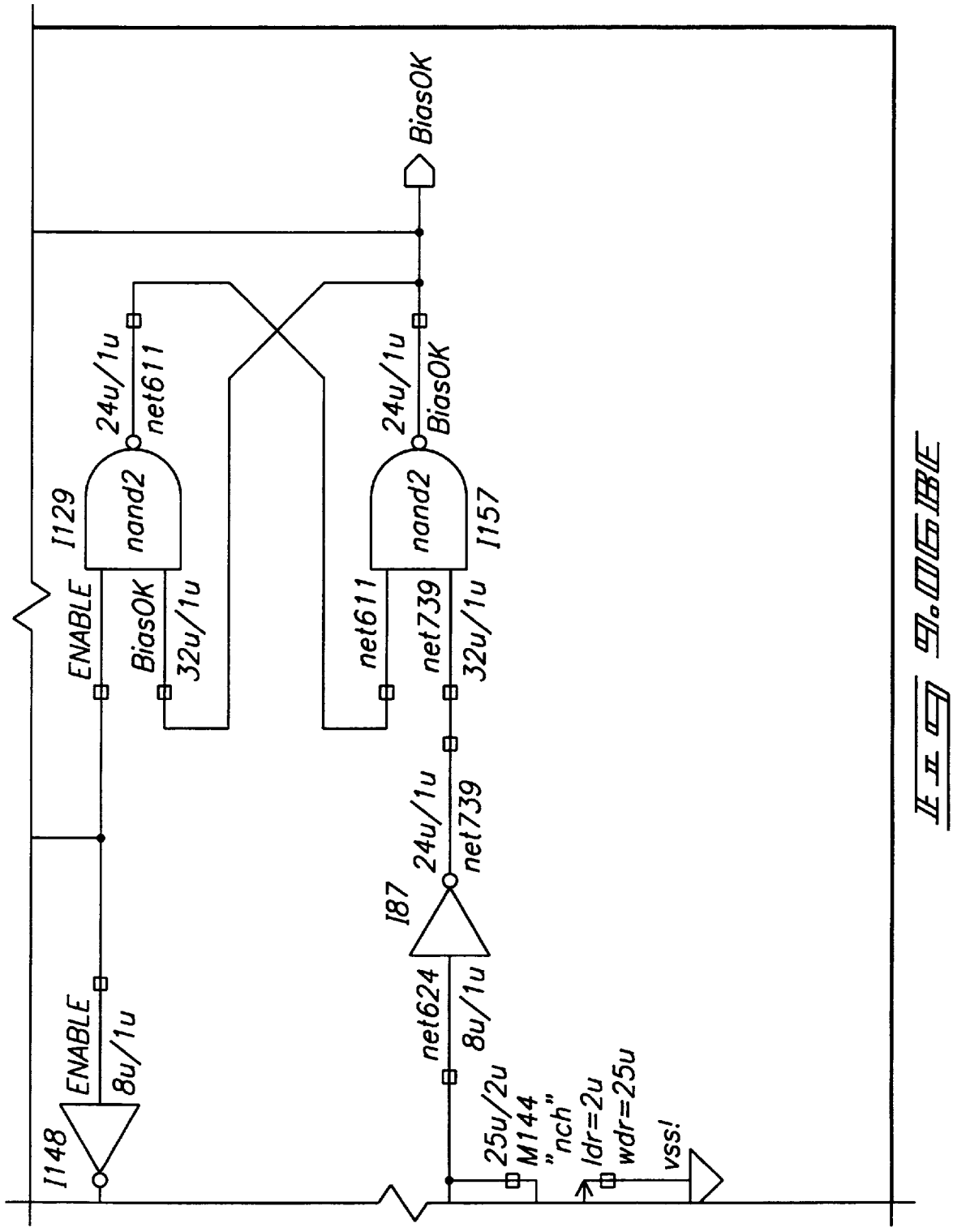
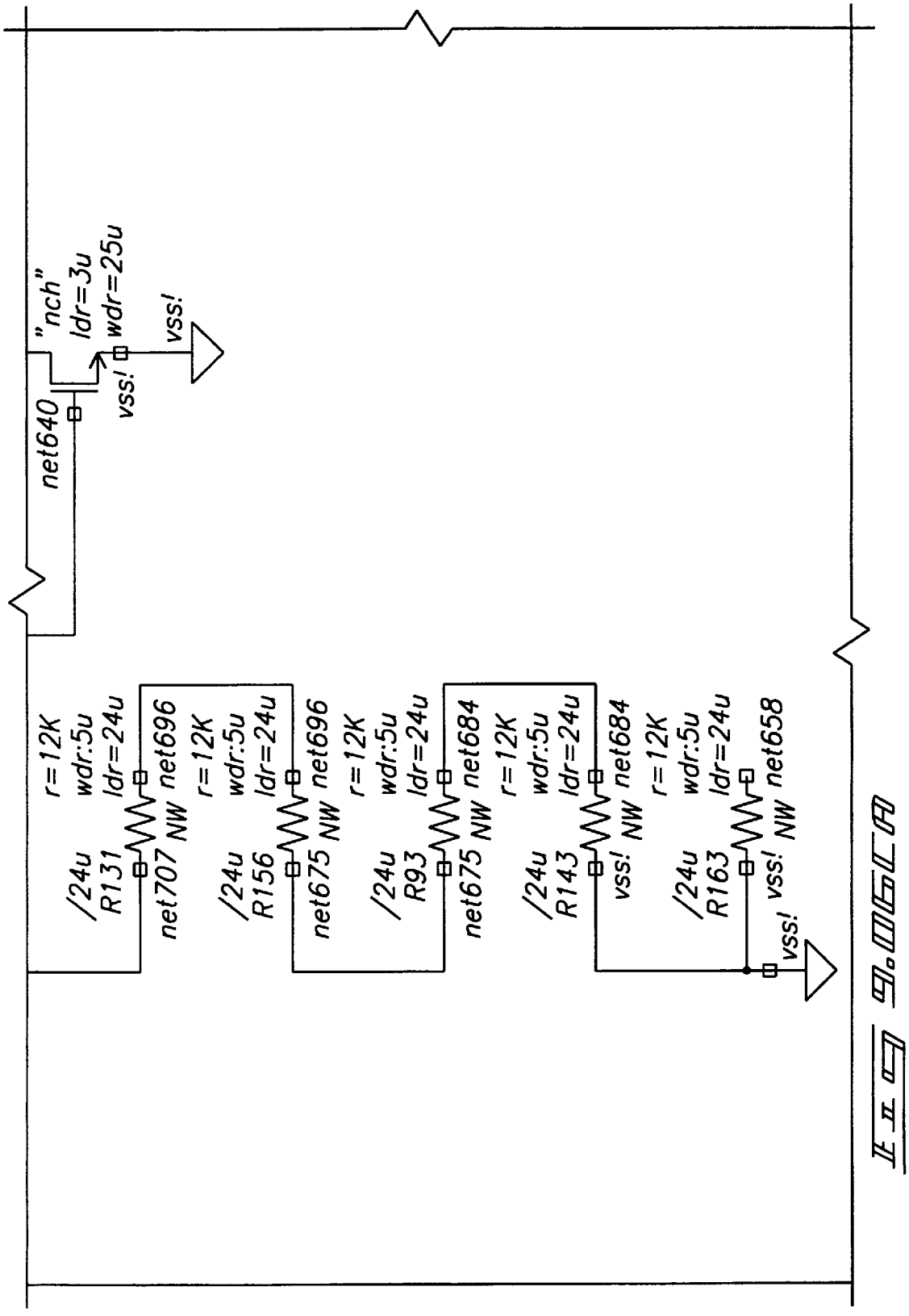

BiasOK
24u/1u
net611
I129
nand2
ENABLE
BiasOK
32u/1u
24u/1u
BiasOK
nand2
I157
net611
net739
32u/1u
24u/1u
net739
I87
net624
8u/1u
ENABLE
8u/1u
I148
25u/2u
M144
"nch"
ldr=2u
wdr=25u
vss!

FIG 9.0E5IBE


"nch"
ldr=3u
wdr=25u
vss!
vss!
net640
r=12K
wdr:5u
ldr=24u
/24u
R131
net707 NW
net696
r=12K
wdr:5u
ldr=24u
/24u
R156
net675 NW
net696
r=12K
wdr:5u
ldr=24u
/24u
R93
net675 NW
net684
r=12K
wdr:5u
ldr=24u
/24u
R143
vss! NW
net684
r=12K
wdr:5u
ldr=24u
/24u
R163
vss! NW
net658
vss!
FIG 9.0058A

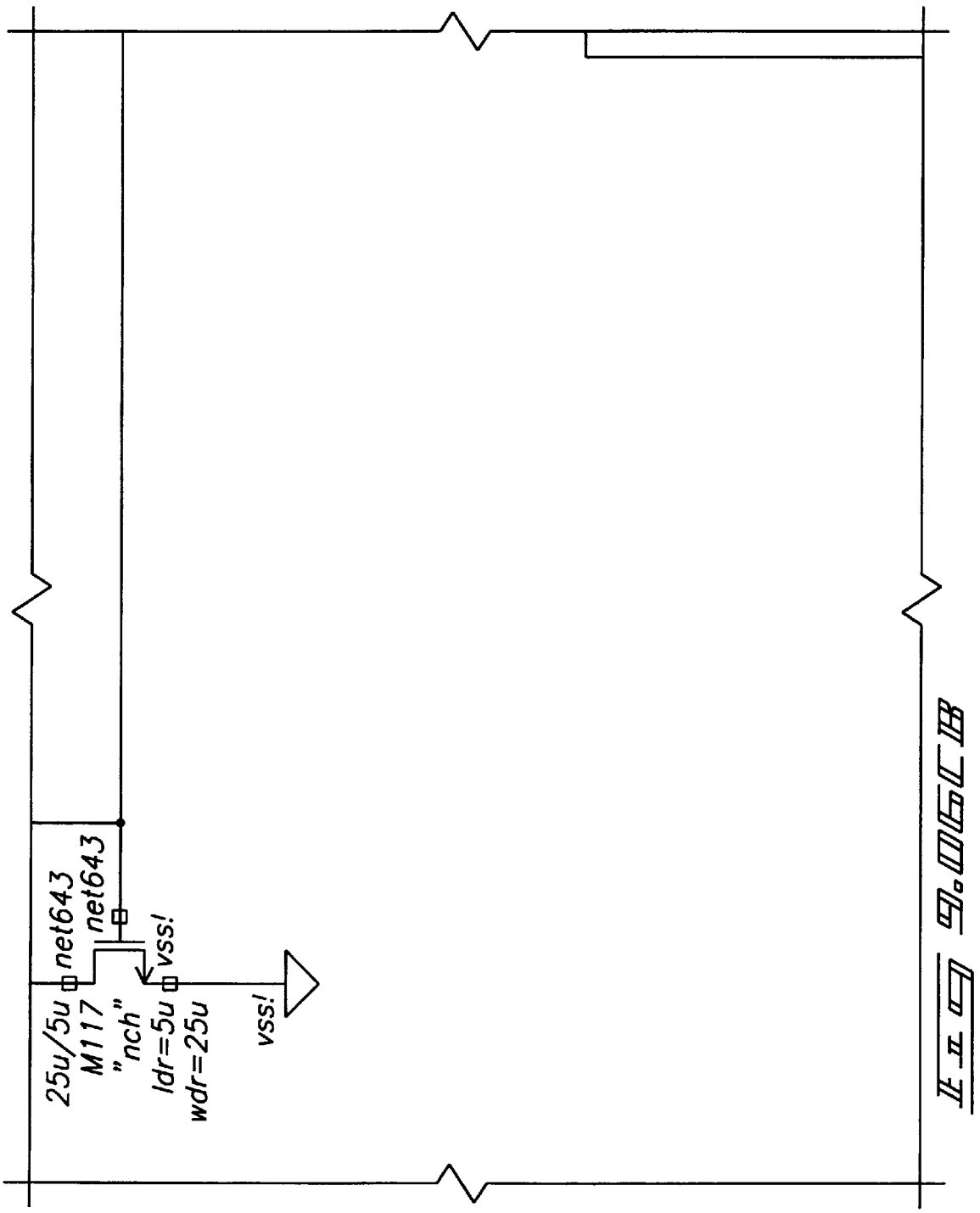


FIG. 9,059B

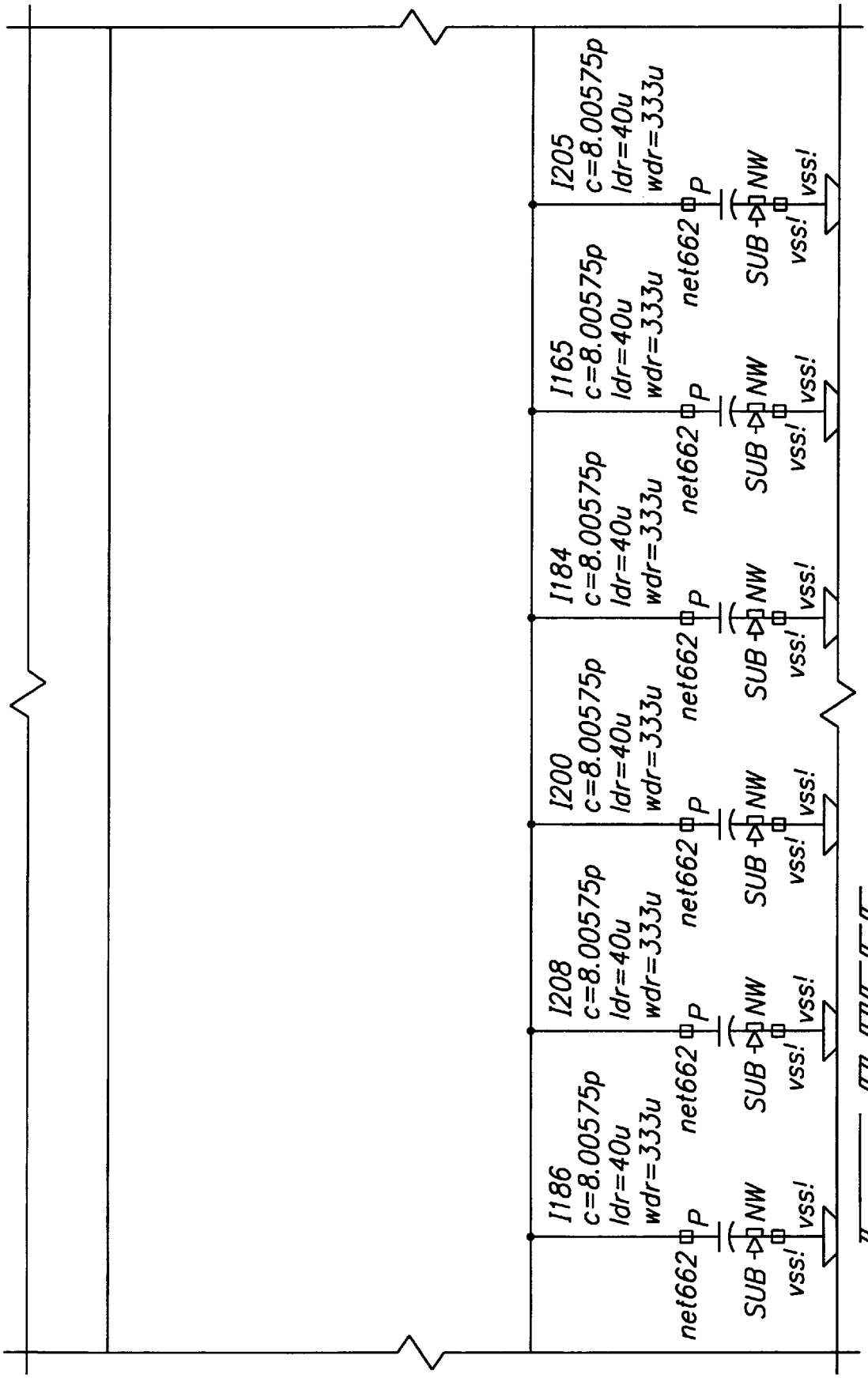

I186
c=8.00575p
ldr=40u
wdr=333u
net662
P
NW
SUB
vss!
I208
I200
I184
I165
I205

FIG. 9,005

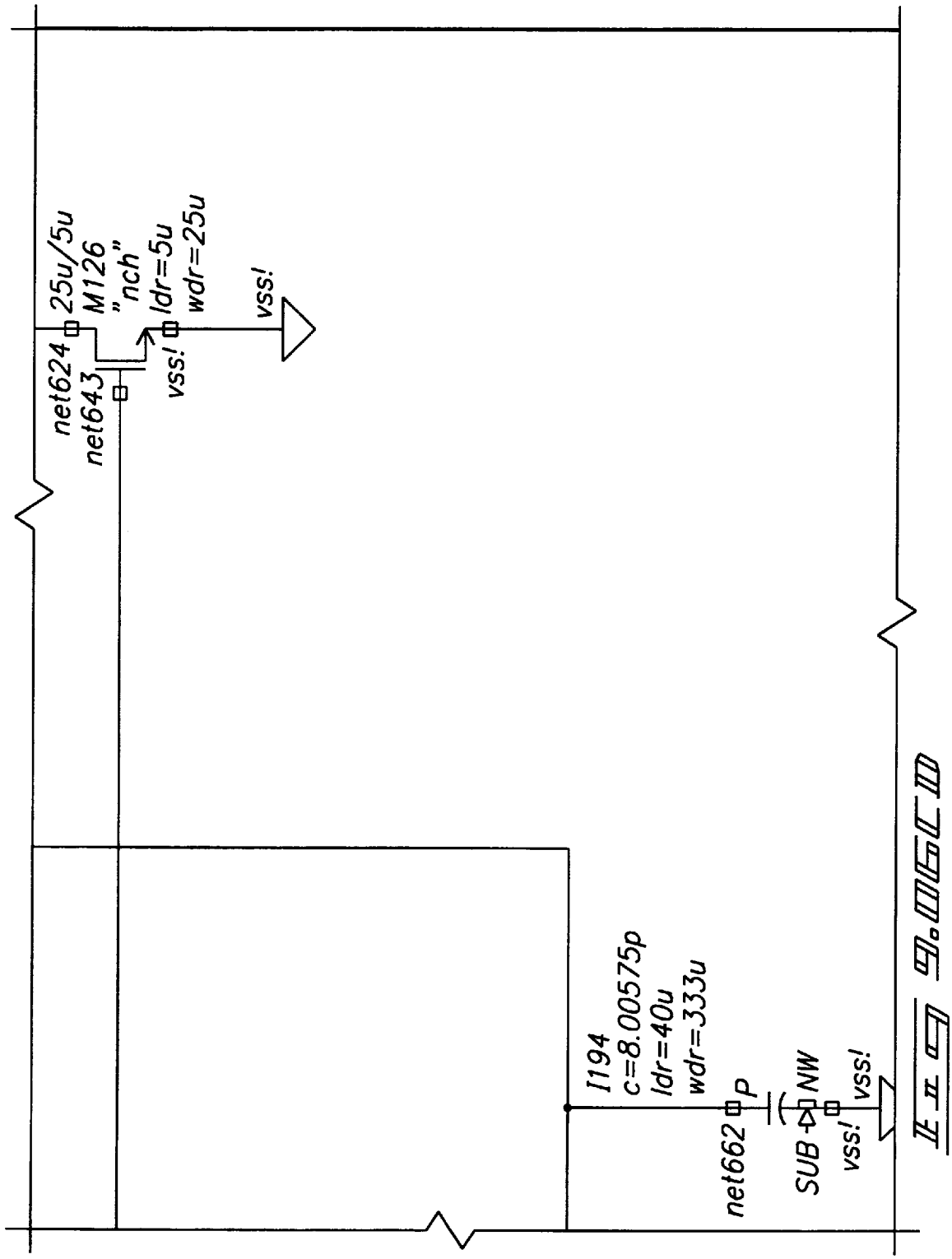
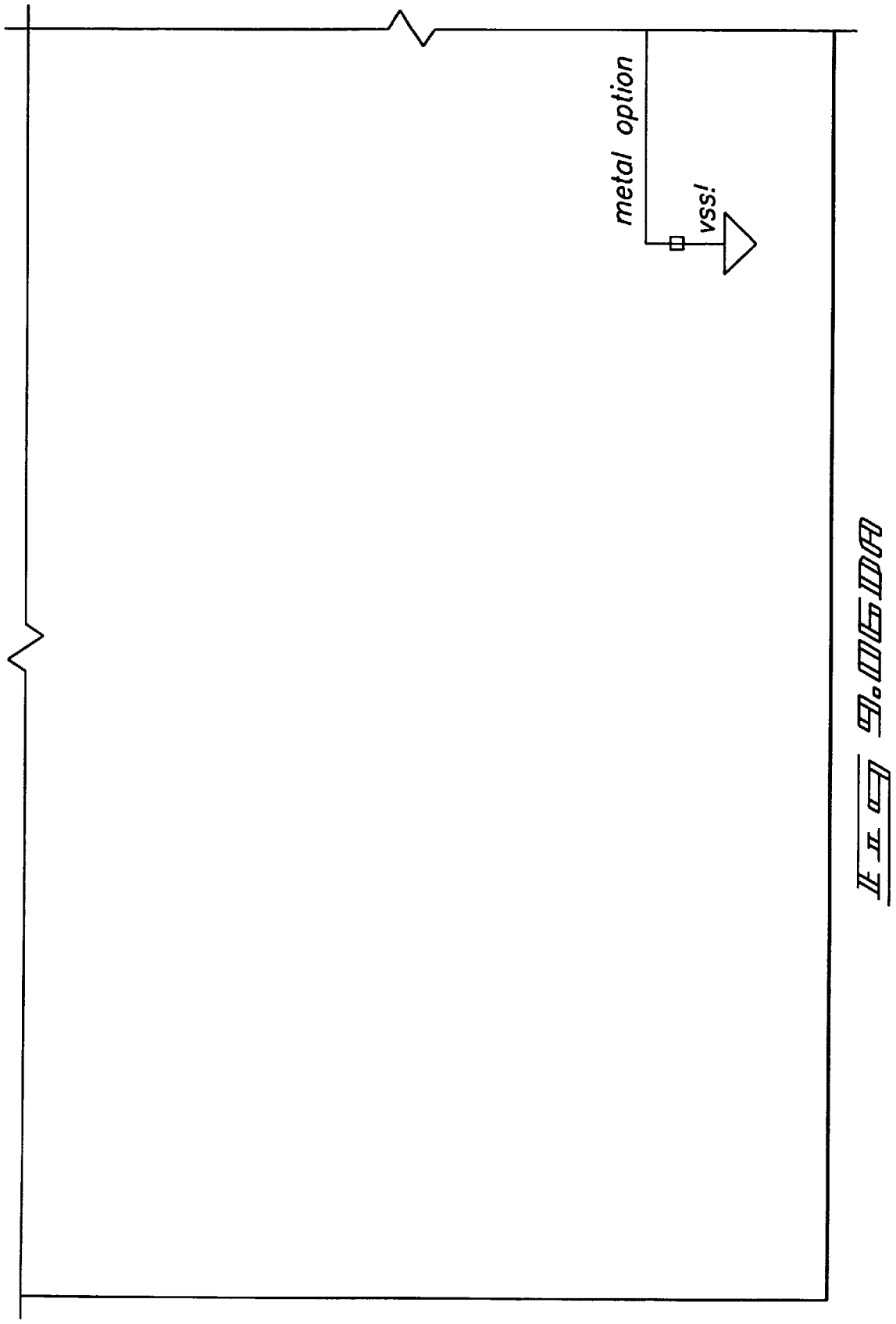

25u/5u
M126
"nch"
ldr=5u
wdr=25u
vss!
net624
net643
vss!
I194
c=8.00575p
ldr=40u
wdr=333u
net662
P
SUB
NW
vss!
vss!

FIG. 9,065,ID


metal option
vss!
FIG. 9,005

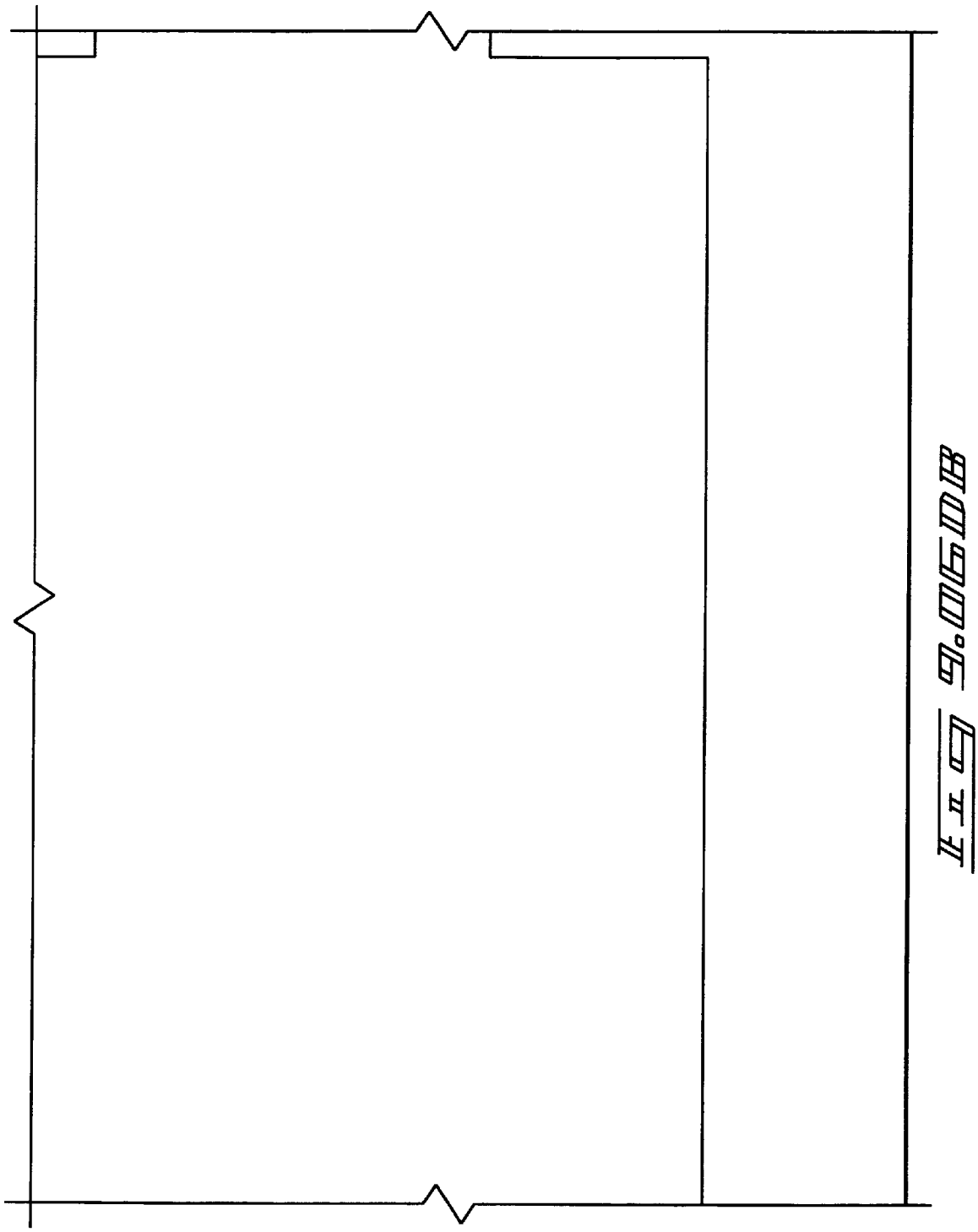


FIG 9,005B

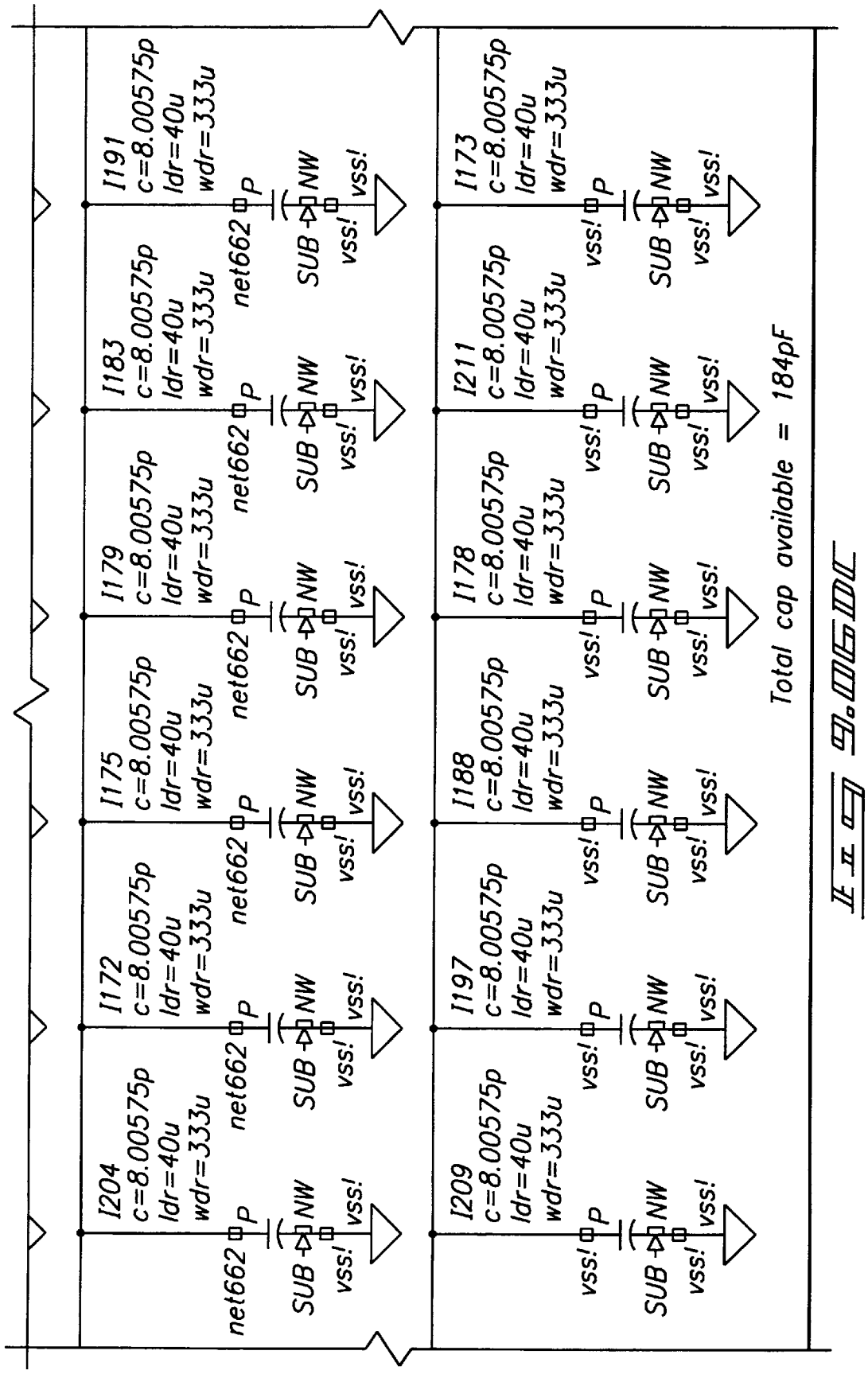

I204
c=8.00575p
ldr=40u
wdr=333u
net662
SUB
NW
P
vss!
I172
I175
I179
I183
I191
I197
I209
I188
I178
I211
I173
Total cap available = 184pF

FIG. 9.005

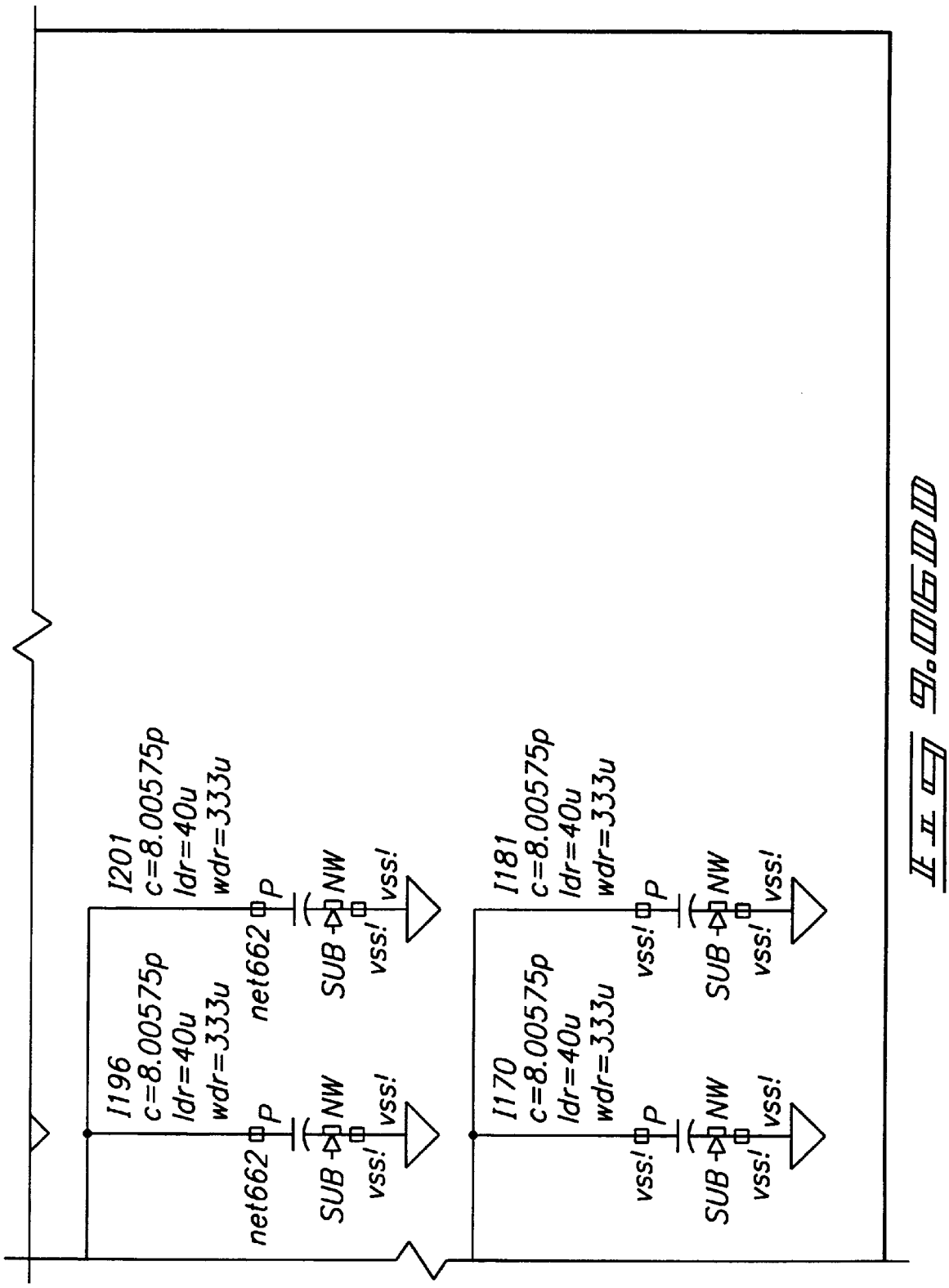

I201
c=8.00575p
ldr=40u
wdr=333u
I196
c=8.00575p
ldr=40u
wdr=333u
net662
P
NW
SUB
vss!
I181
c=8.00575p
ldr=40u
wdr=333u
I170
c=8.00575p
ldr=40u
wdr=333u

FIG 9,005,000

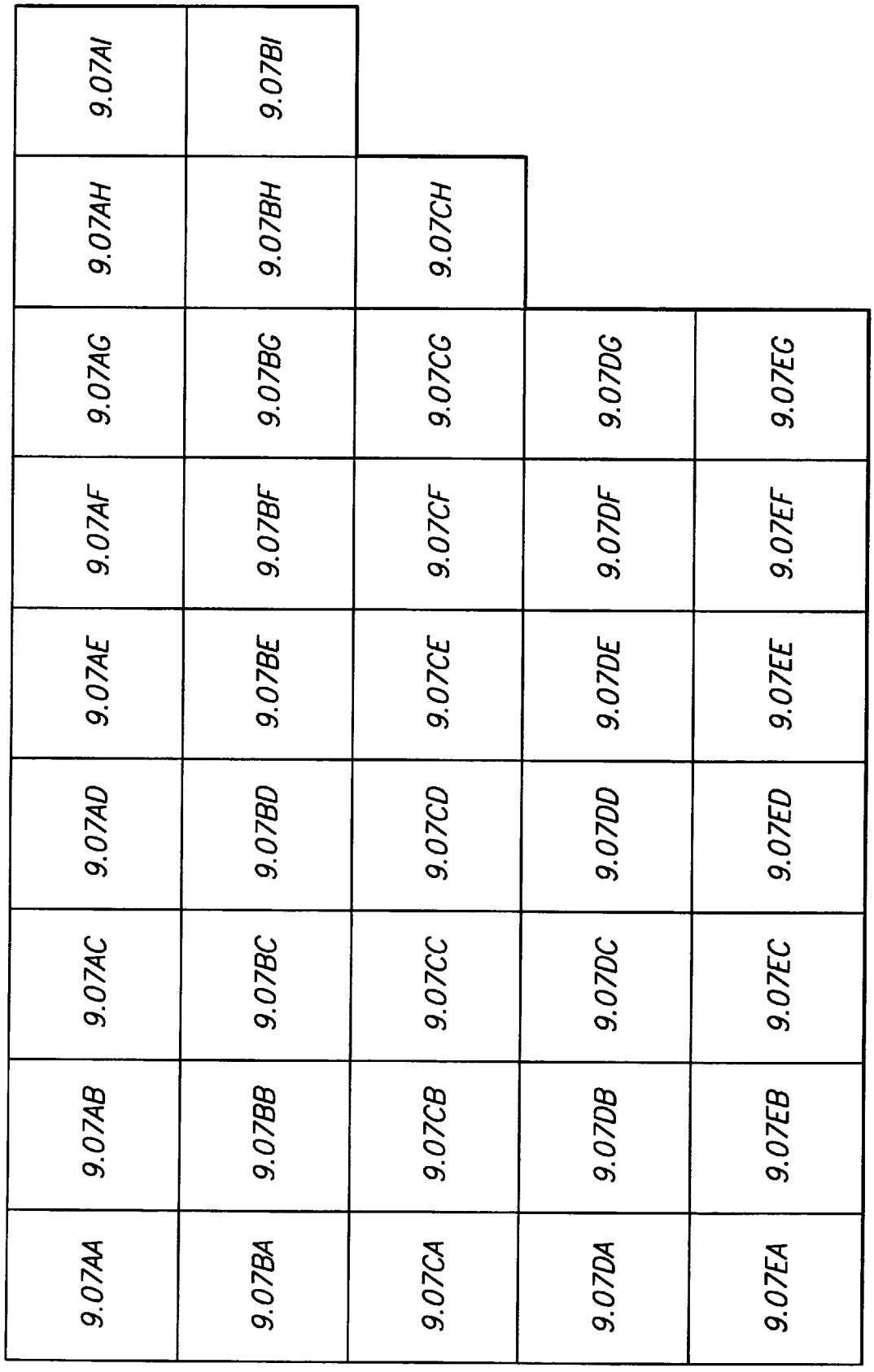
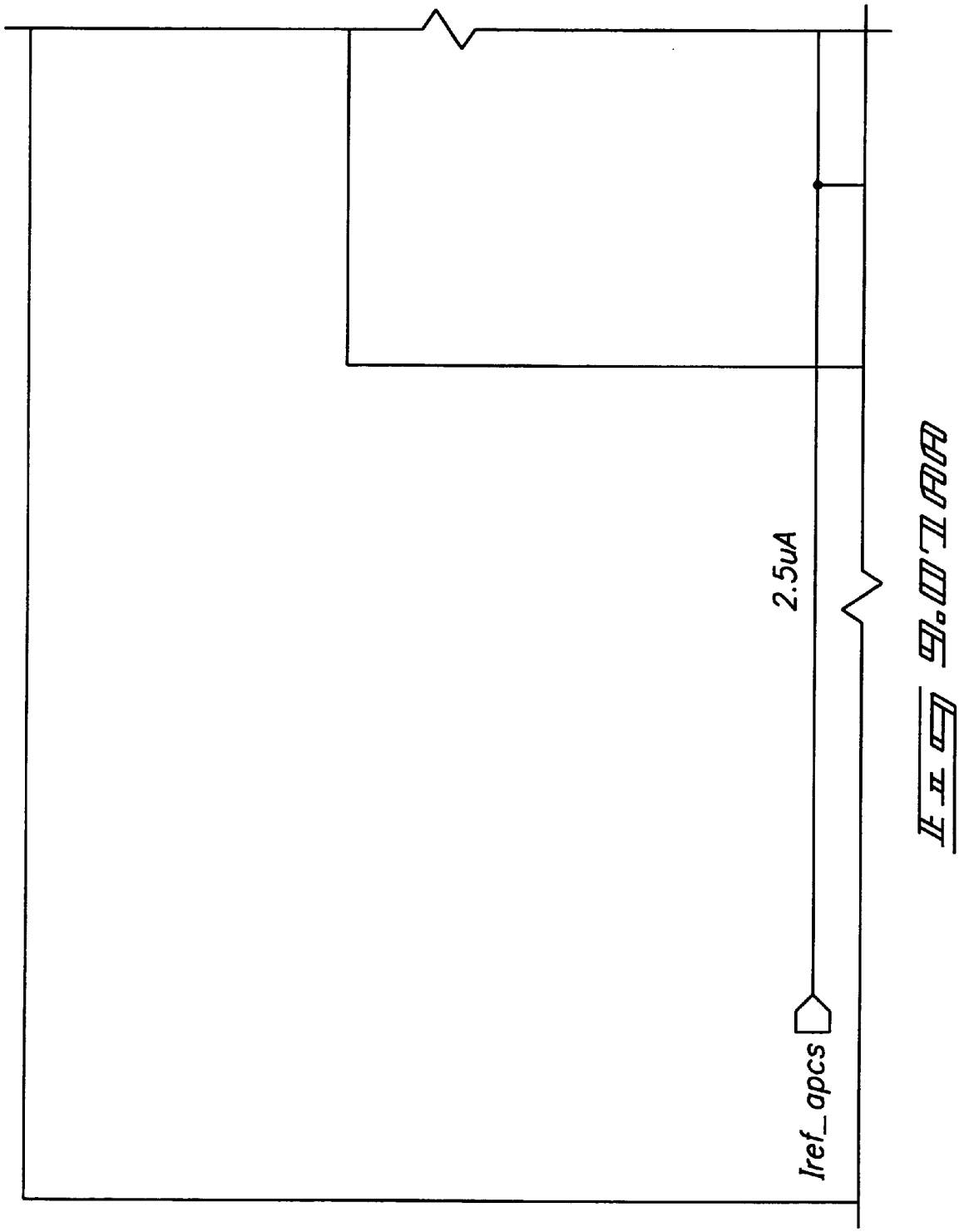

9.07AI
9.07BI
9.07AH
9.07BH
9.07CH
9.07AG
9.07BG
9.07CG
9.07DG
9.07EG
9.07AF
9.07BF
9.07CF
9.07DF
9.07EF
9.07AE
9.07BE
9.07CE
9.07DE
9.07EE
9.07AD
9.07BD
9.07CD
9.07DD
9.07ED
9.07AC
9.07BC
9.07CC
9.07DC
9.07EC
9.07AB
9.07BB
9.07CB
9.07DB
9.07EB
9.07AA
9.07BA
9.07CA
9.07DA
9.07EA

FIG. 9.07


2.5uA
Iref_apcs

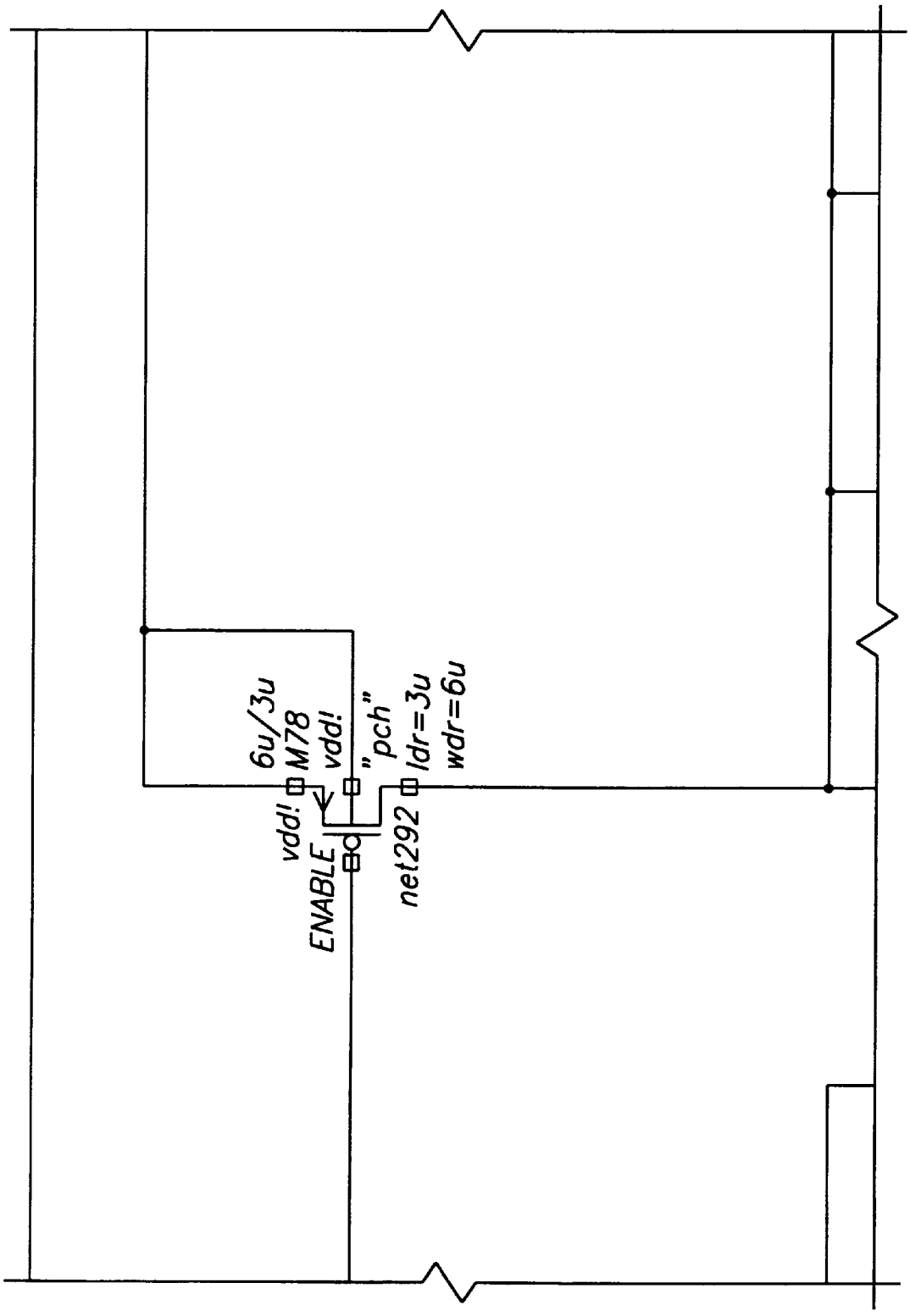


FIG 9.00AB

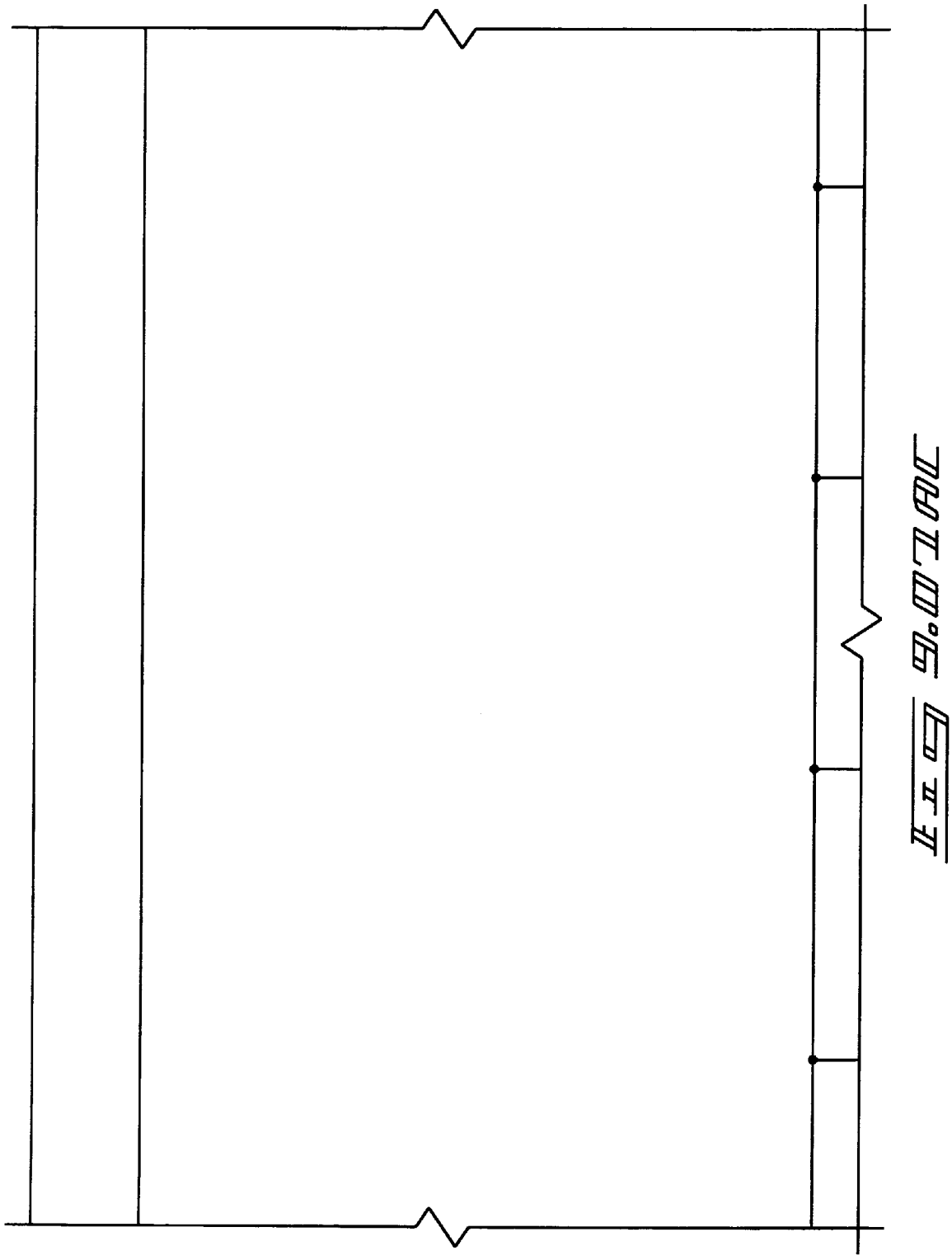


FIG 95,005

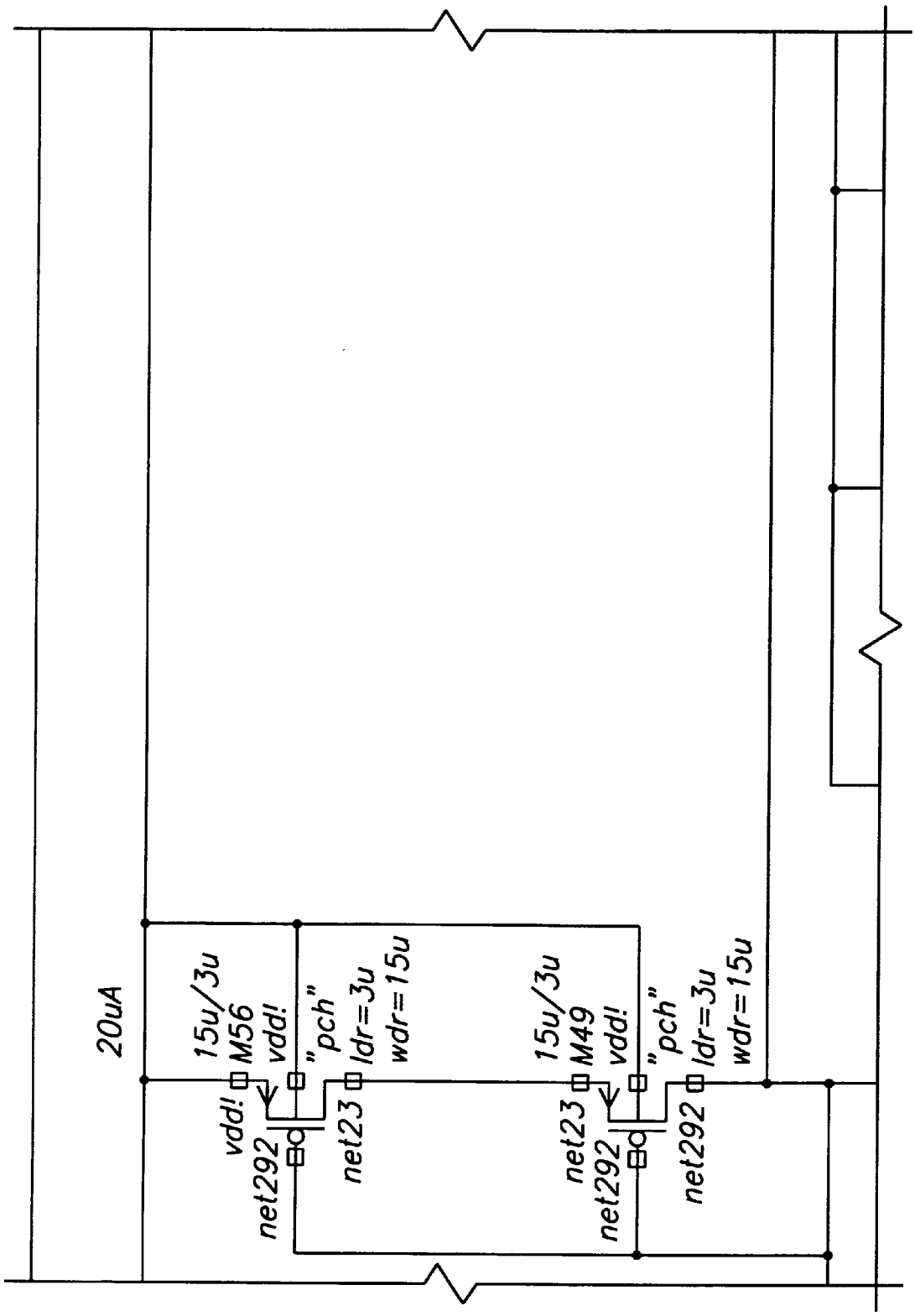

20uA
15u/3u
M56
vdd!
"pch"
ldr=3u
wdr=15u
vdd!
net292
net23
15u/3u
M49
vdd!
"pch"
ldr=3u
wdr=15u
net23
net292
net292

FIG. 69.0144

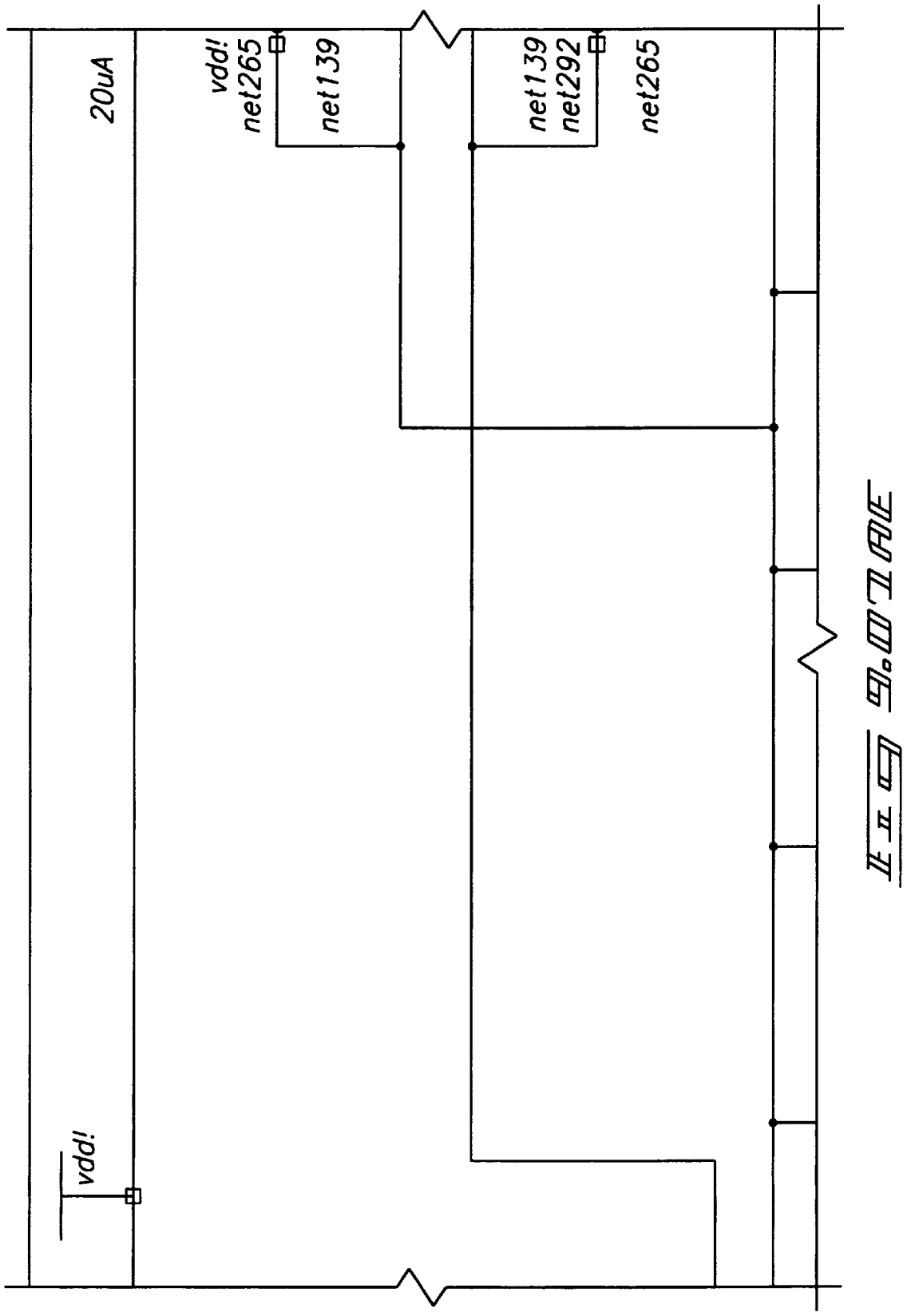


FIG 9.0TAE

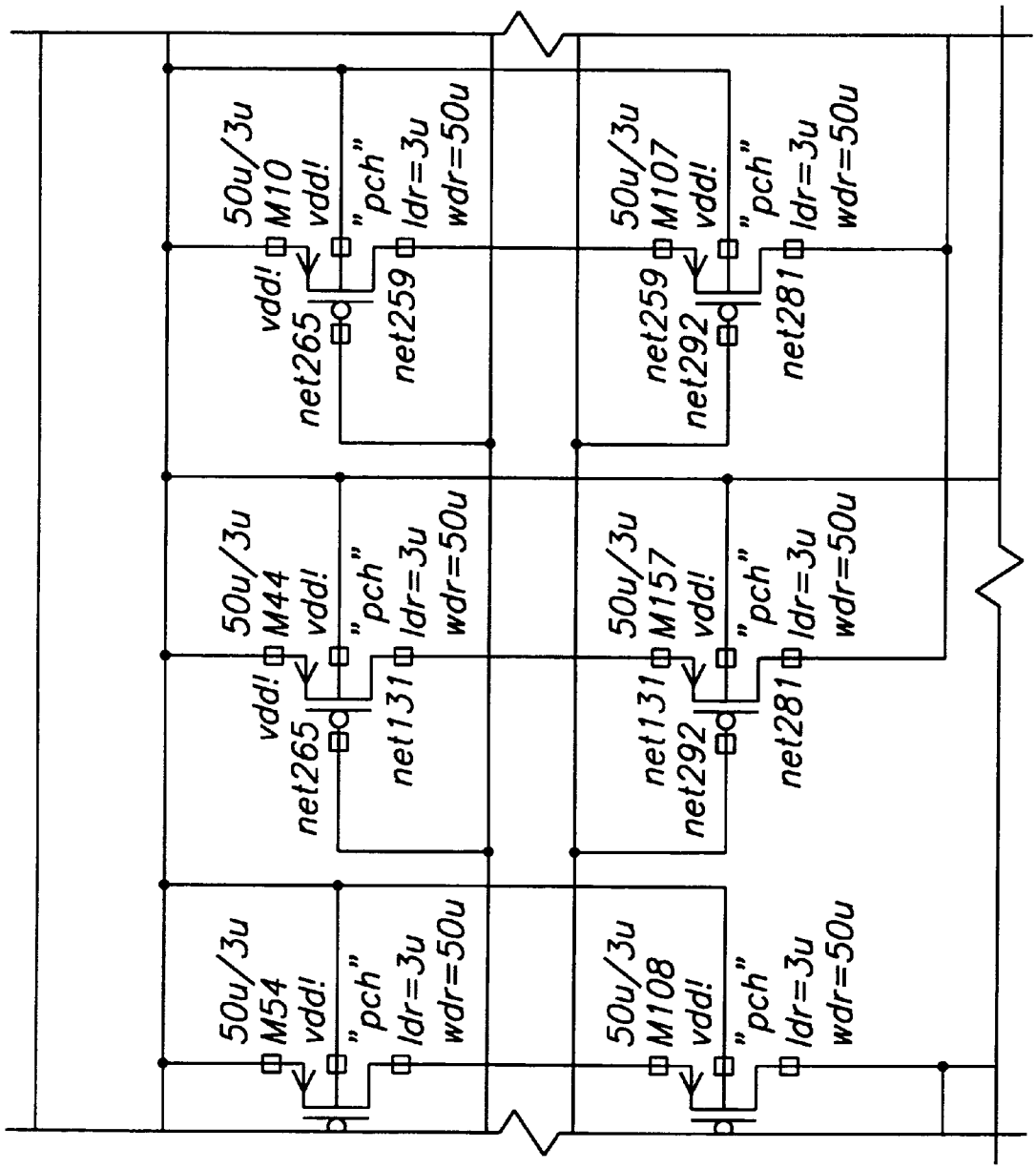

50u/3u
M10
vdd!
"pch"
ldr=3u
wdr=50u
vdd!
net265
net259
50u/3u
M107
vdd!
"pch"
ldr=3u
wdr=50u
net259
net292
net281
50u/3u
M44
vdd!
"pch"
ldr=3u
wdr=50u
vdd!
net265
net131
50u/3u
M157
vdd!
"pch"
ldr=3u
wdr=50u
net131
net292
net281
50u/3u
M54
vdd!
"pch"
ldr=3u
wdr=50u
50u/3u
M108
vdd!
"pch"
ldr=3u
wdr=50u

FIG. 9.0112AF

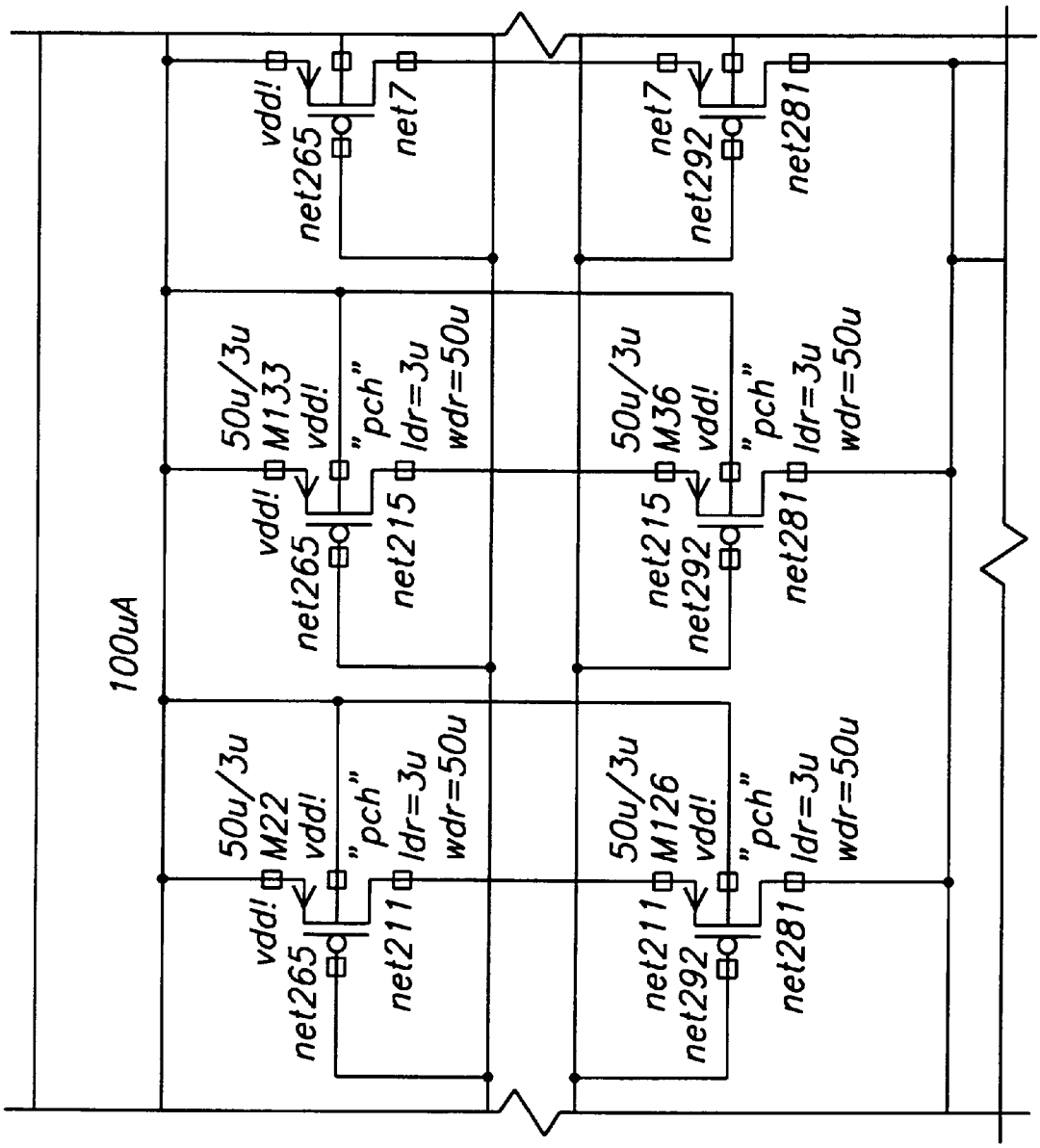

100uA
vdd!
net265
net7
net292
net281
50u/3u
M133
M36
M22
M126
"pch"
ldr=3u
wdr=50u
net215
net211

FIG 9.0112

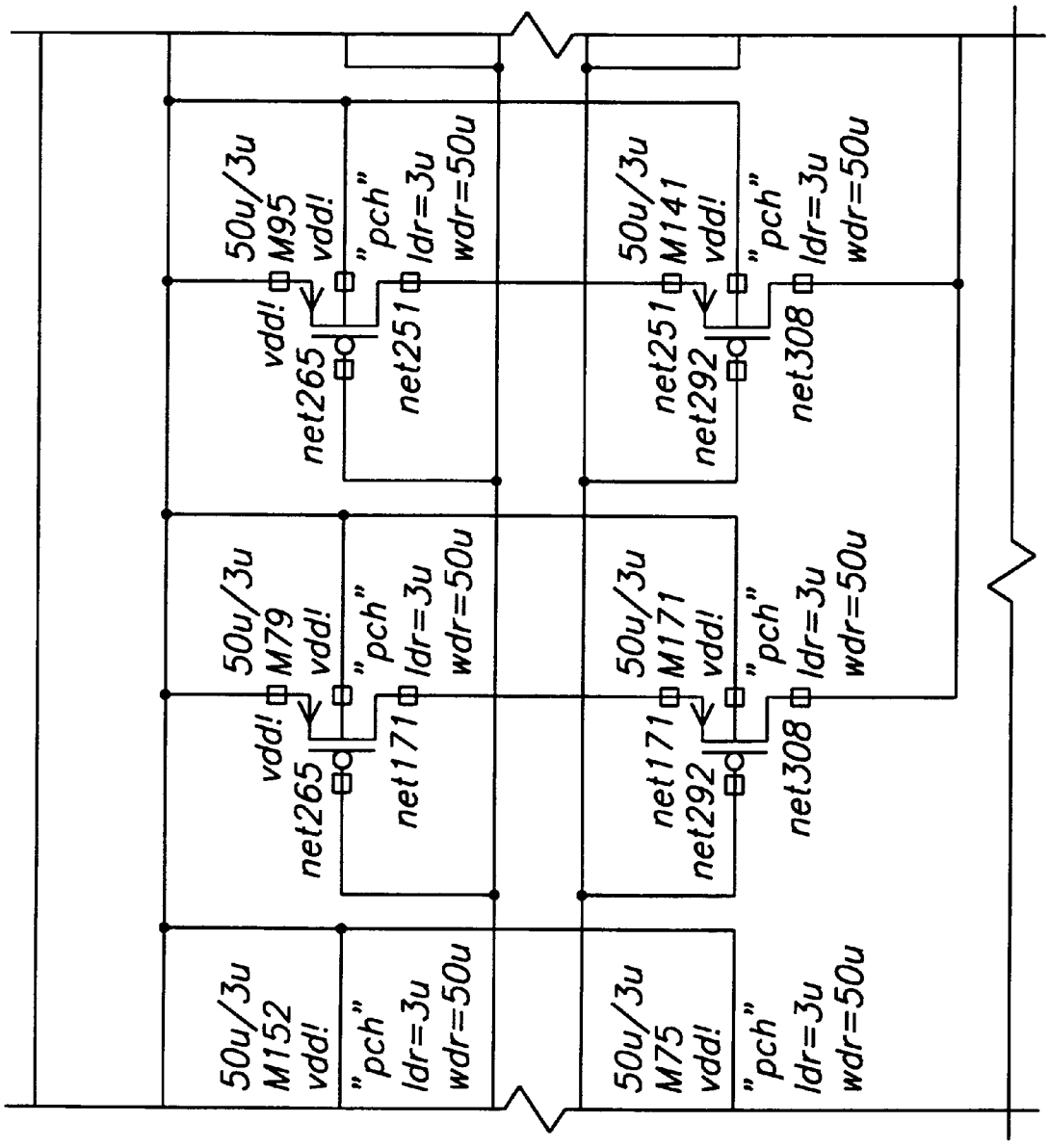


FIG. 99.0011 AH

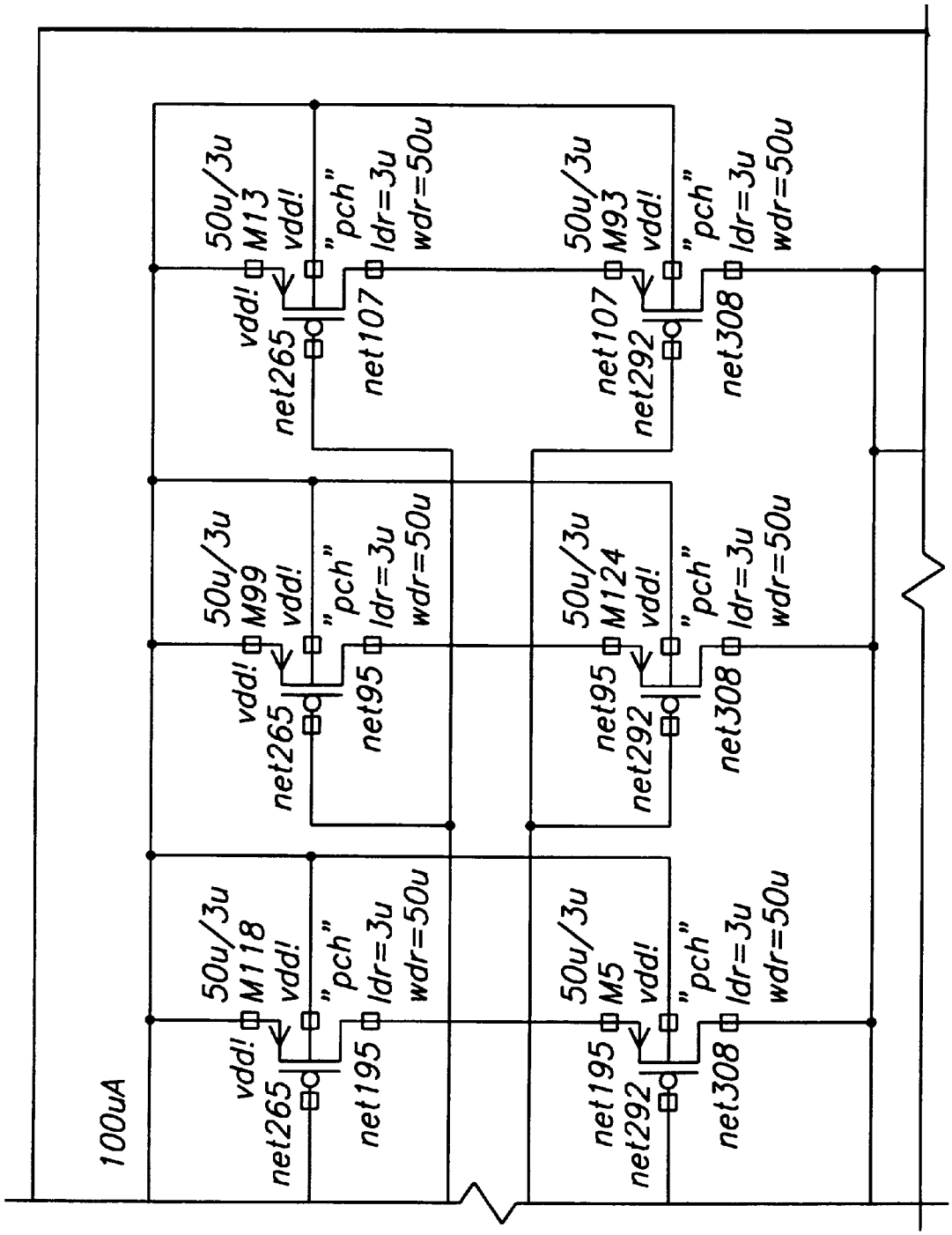

100uA
50u/3u M13 vdd! "pch" ldr=3u wdr=50u
50u/3u M93 vdd! "pch" ldr=3u wdr=50u
50u/3u M99 vdd! "pch" ldr=3u wdr=50u
50u/3u M124 vdd! "pch" ldr=3u wdr=50u
50u/3u M118 vdd! "pch" ldr=3u wdr=50u
50u/3u M5 vdd! "pch" ldr=3u wdr=50u
vdd! net265 net107 net292 net308 net95 net195

FIG. 2635

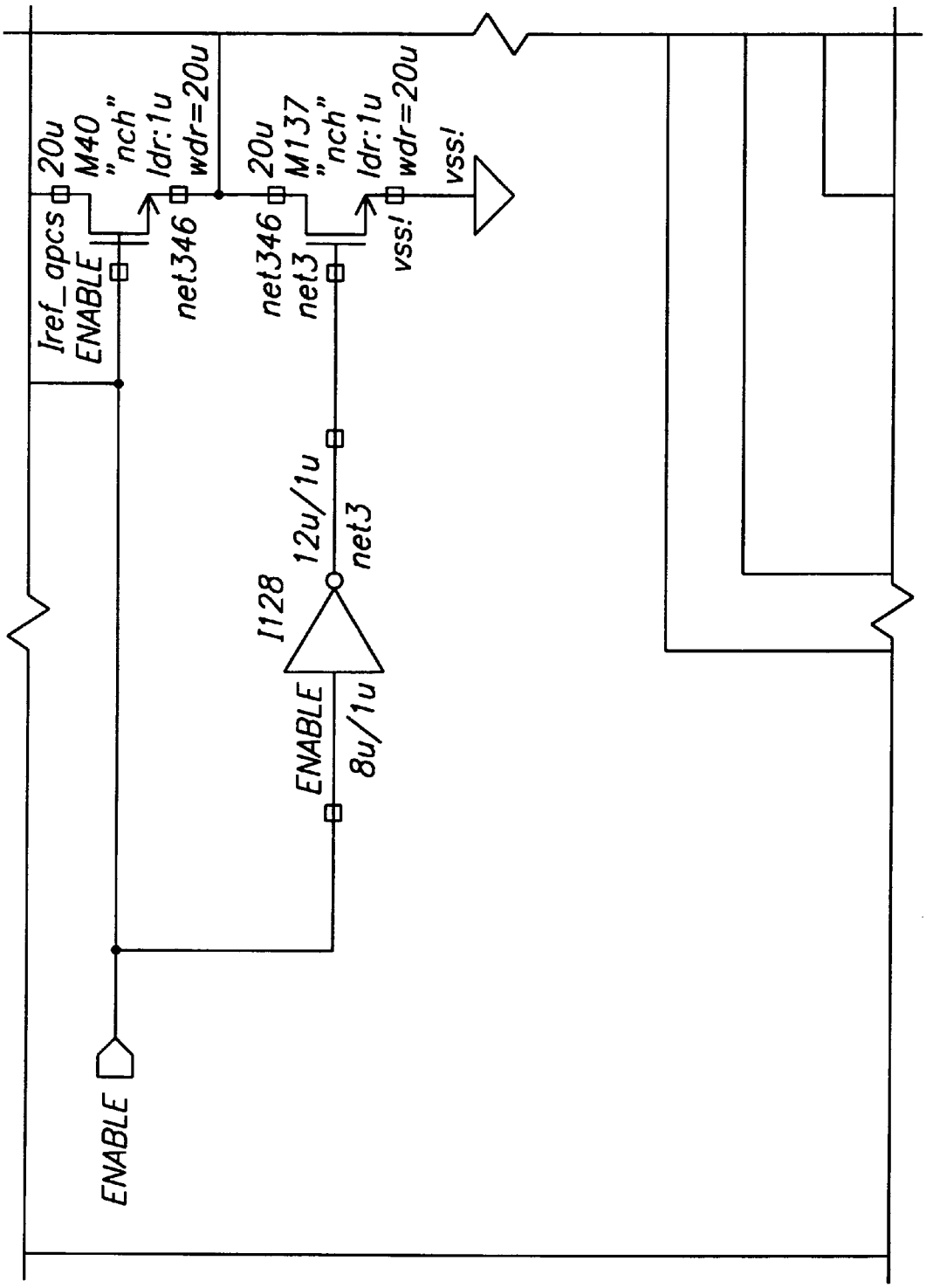

20u
M40
"nch"
ldr:1u
wdr=20u
20u
M137
"nch"
ldr:1u
wdr=20u
vss!
Iref_apcs
ENABLE
net346
net346
net3
vss!
I128
12u/1u
net3
ENABLE
8u/1u
ENABLE

FIG. 9.00 IBM

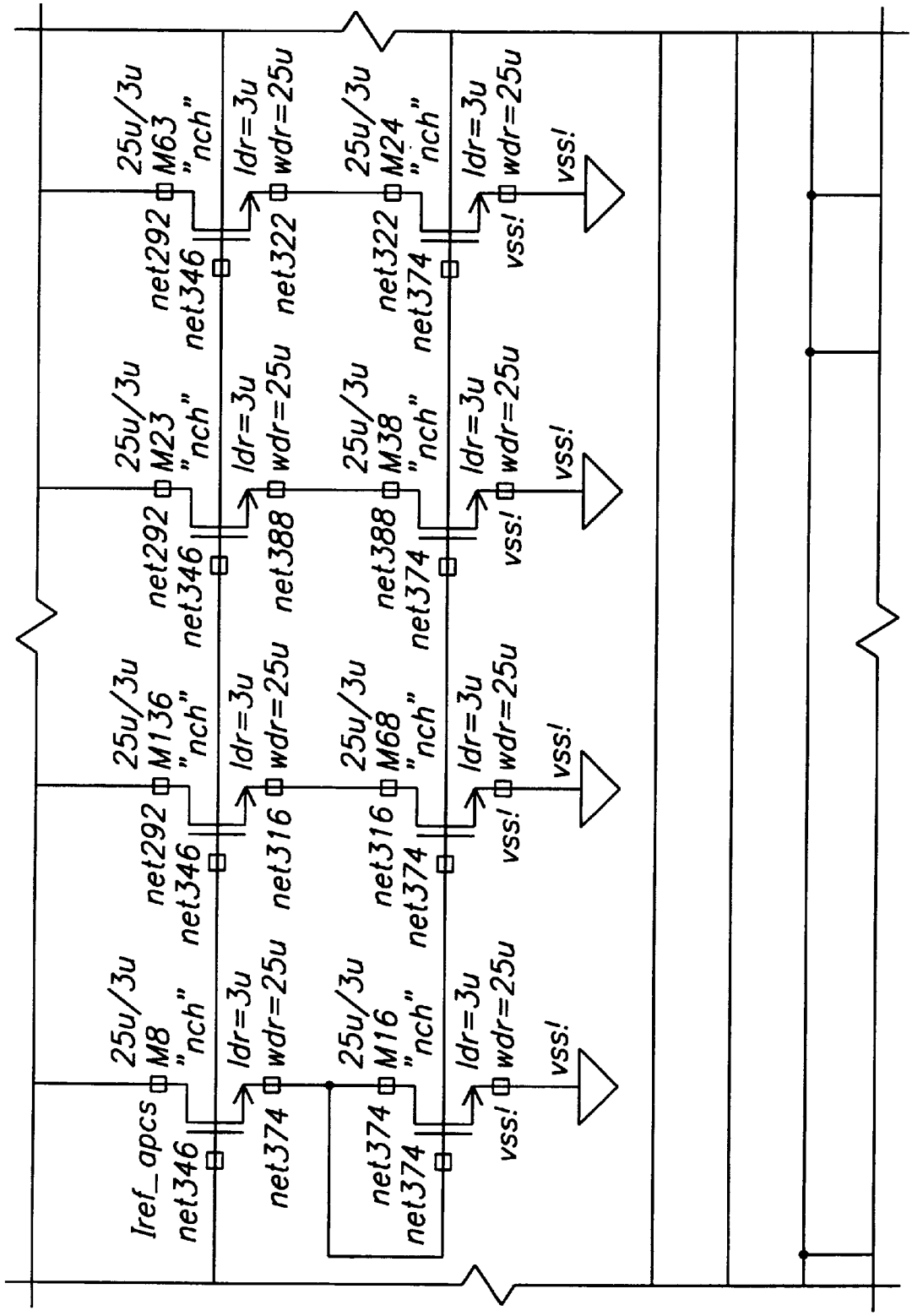

Iref_apcs
net346
25u/3u
M8
"nch"
ldr=3u
wdr=25u
net292
net346
net374
net374
net374
25u/3u
M16
"nch"
ldr=3u
wdr=25u
vss!
vss!
vss!
25u/3u
M136
"nch"
ldr=3u
wdr=25u
net292
net346
net316
net316
net374
25u/3u
M68
"nch"
ldr=3u
wdr=25u
vss!
vss!
vss!
25u/3u
M23
"nch"
ldr=3u
wdr=25u
net292
net346
net388
net388
net374
25u/3u
M38
"nch"
ldr=3u
wdr=25u
vss!
vss!
vss!
25u/3u
M63
"nch"
ldr=3u
wdr=25u
net292
net346
net322
net322
net374
25u/3u
M24
"nch"
ldr=3u
wdr=25u
vss!
vss!
vss!

FIG. 2637

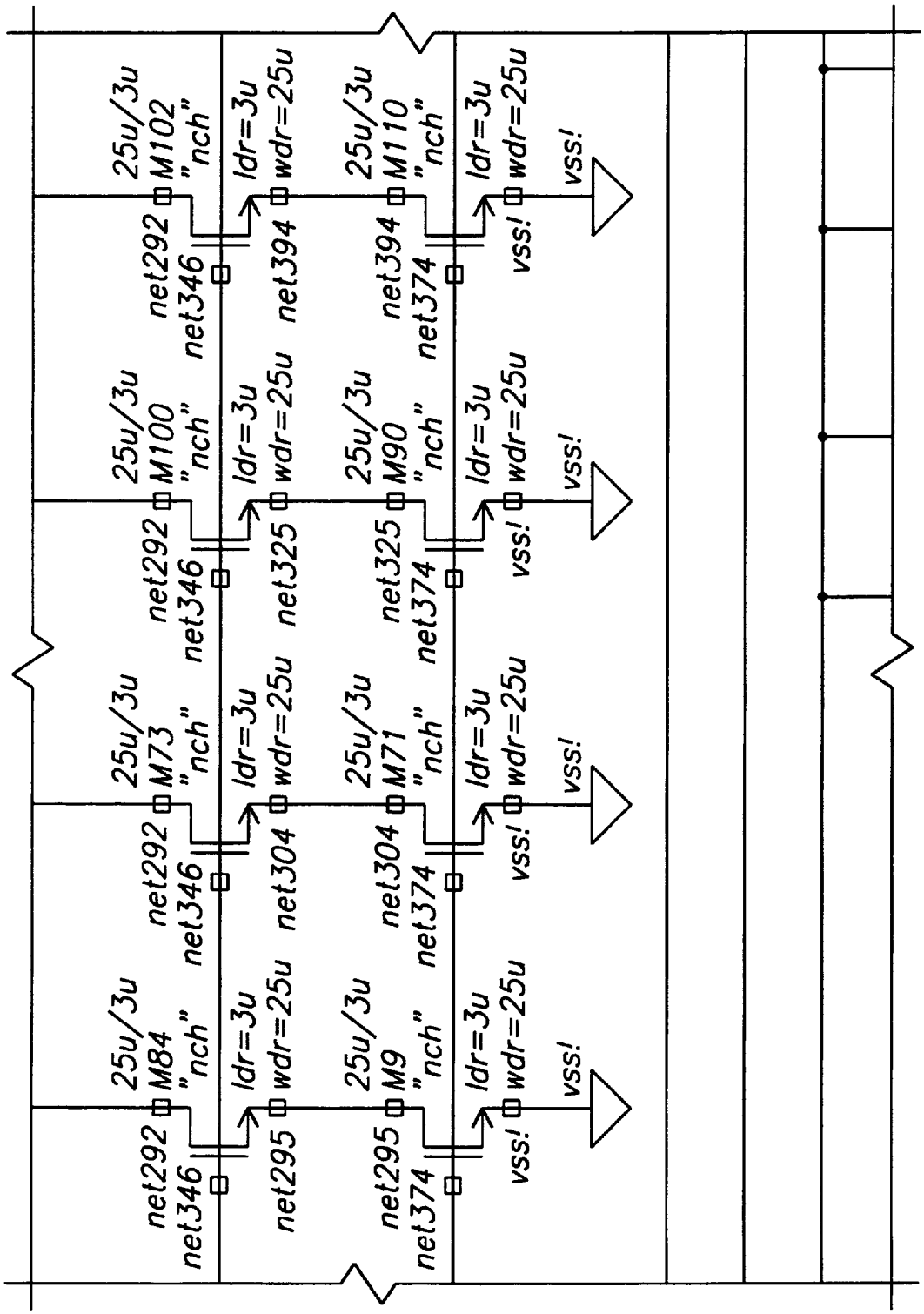

25u/3u
M84
"nch"
ldr=3u
wdr=25u
net292
net346
net295
vss!
25u/3u
M73
"nch"
ldr=3u
wdr=25u
net292
net346
net304
vss!
25u/3u
M100
"nch"
ldr=3u
wdr=25u
net292
net346
net325
vss!
25u/3u
M102
"nch"
ldr=3u
wdr=25u
net292
net346
net394
vss!
25u/3u
M9
"nch"
ldr=3u
wdr=25u
net295
net374
vss!
25u/3u
M71
"nch"
ldr=3u
wdr=25u
net304
net374
vss!
25u/3u
M90
"nch"
ldr=3u
wdr=25u
net325
net374
vss!
25u/3u
M110
"nch"
ldr=3u
wdr=25u
net394
net374
vss!

FIG. 9.00 IBM

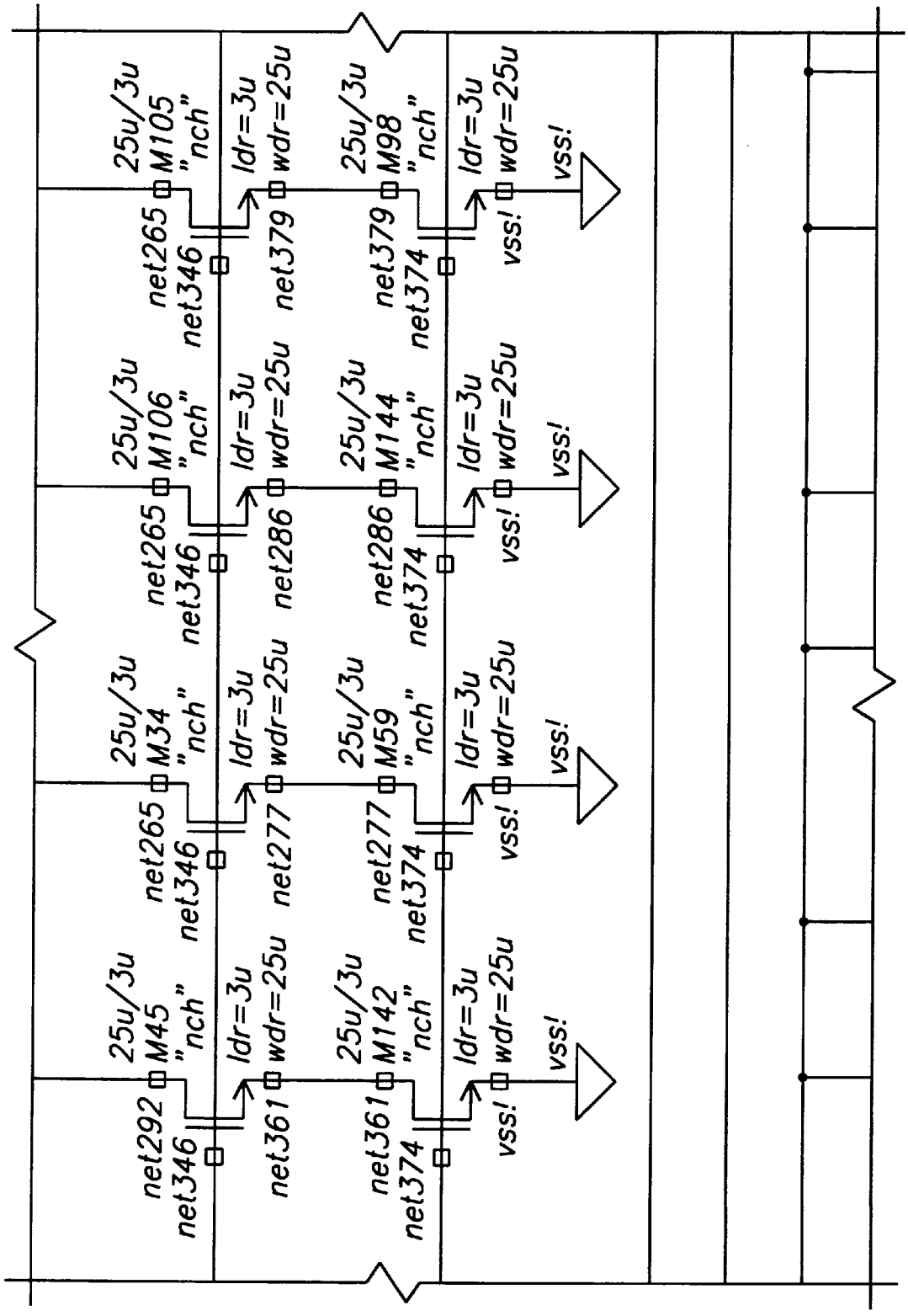

25u/3u
M105
"nch"
ldr=3u
wdr=25u
net265
net346
net379
M98
net374
vss!
M106
net286
M144
M34
net277
M59
M45
net292
net361
M142

FIG 9.00 IBM

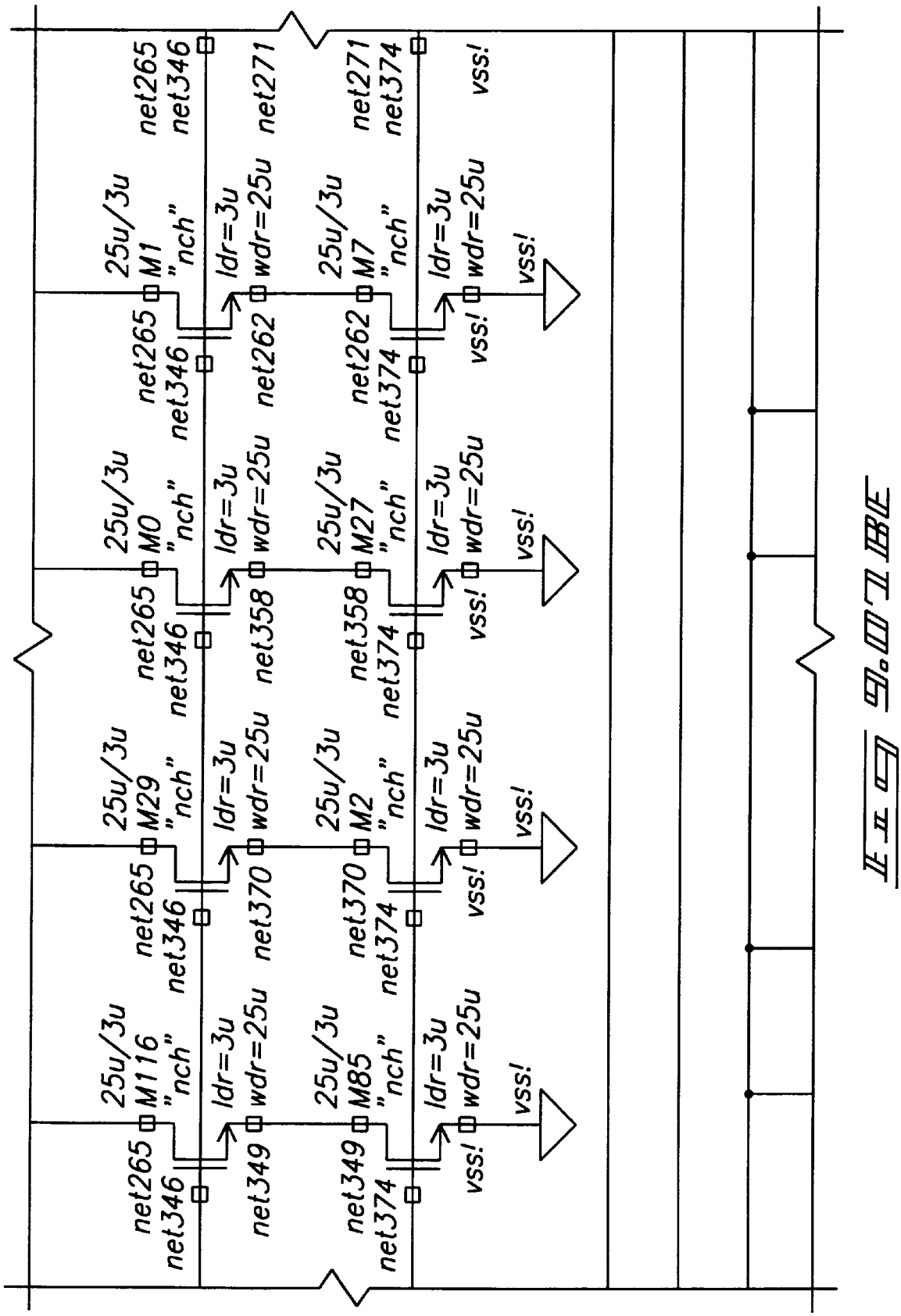

25u/3u
M116
"nch"
ldr=3u
wdr=25u
net265
net346
net349
net374
net370
net358
net262
net271
vss!
M85
M2
M27
M7
M29
M0
M1

FIG. 2640

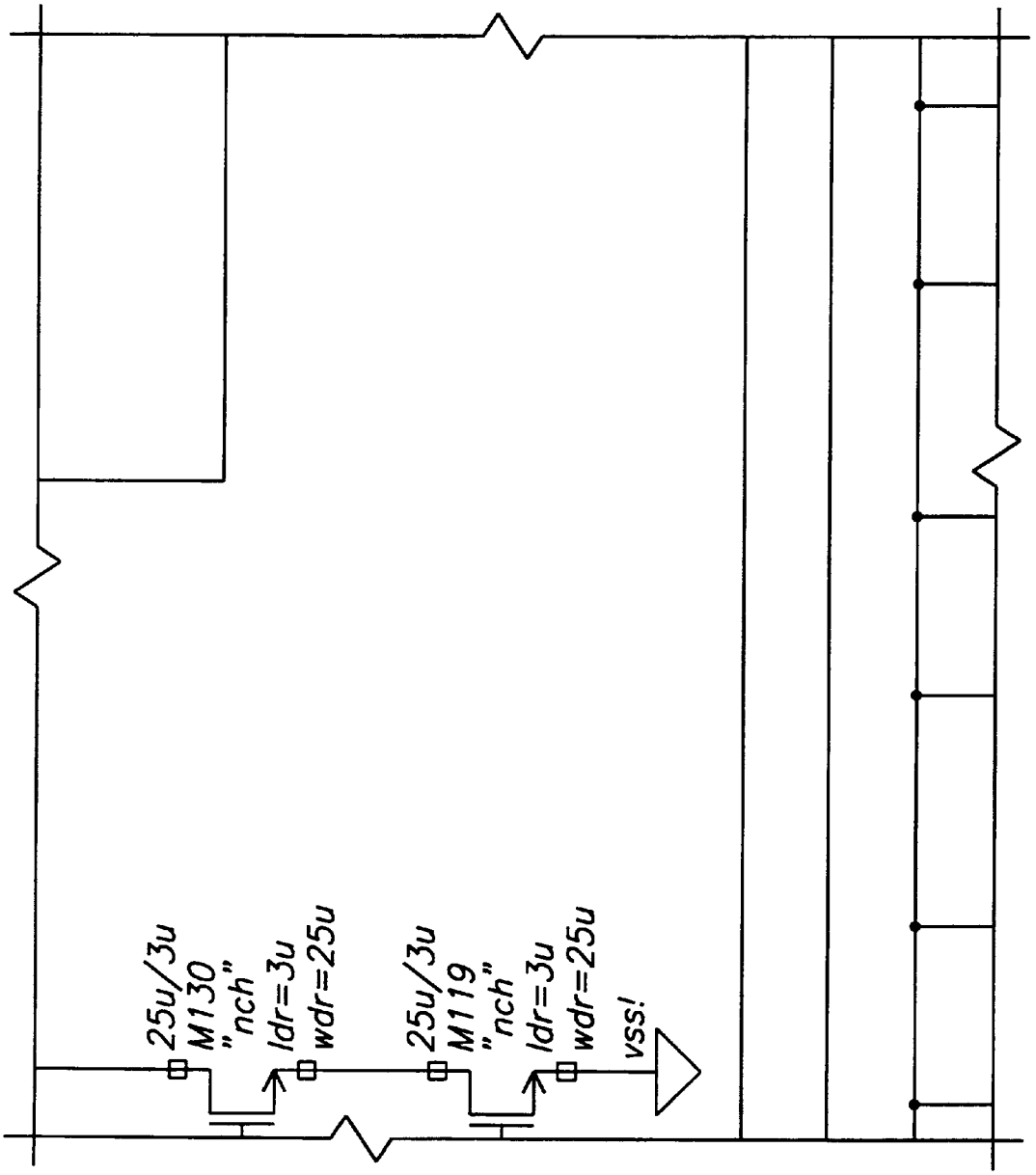


FIG 9.0118F

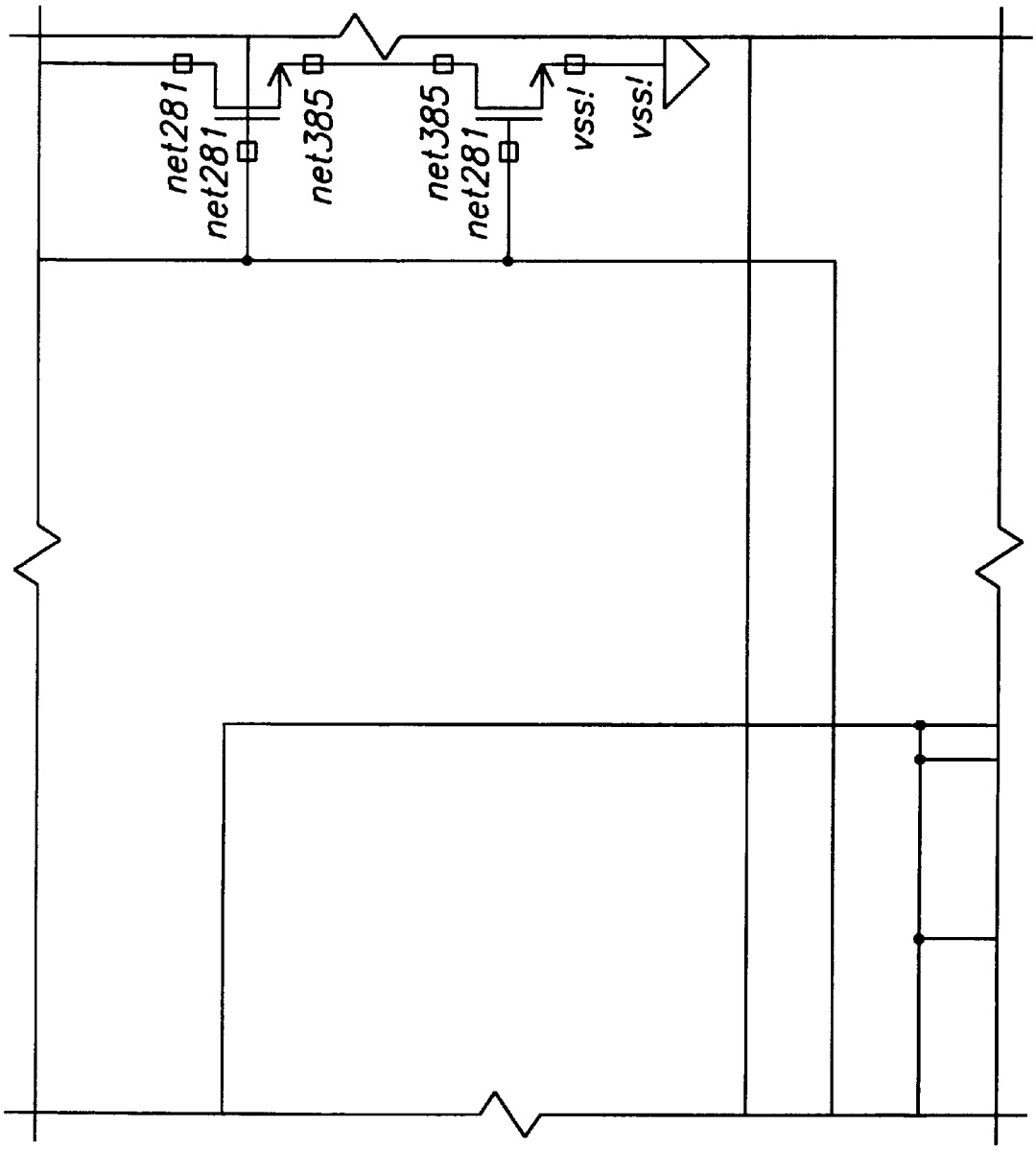


FIG 9,007 IBG

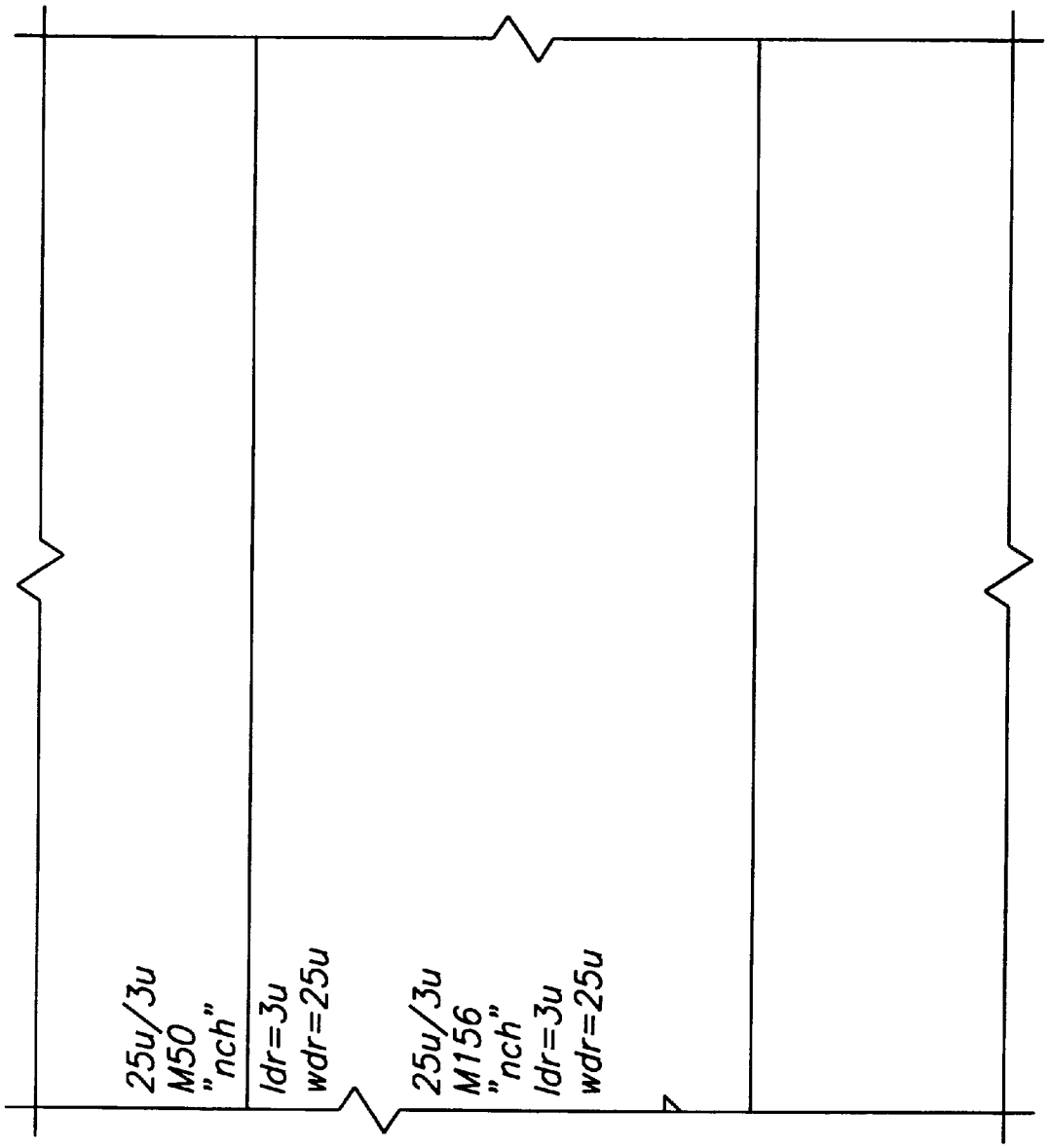


Fig. 90,005

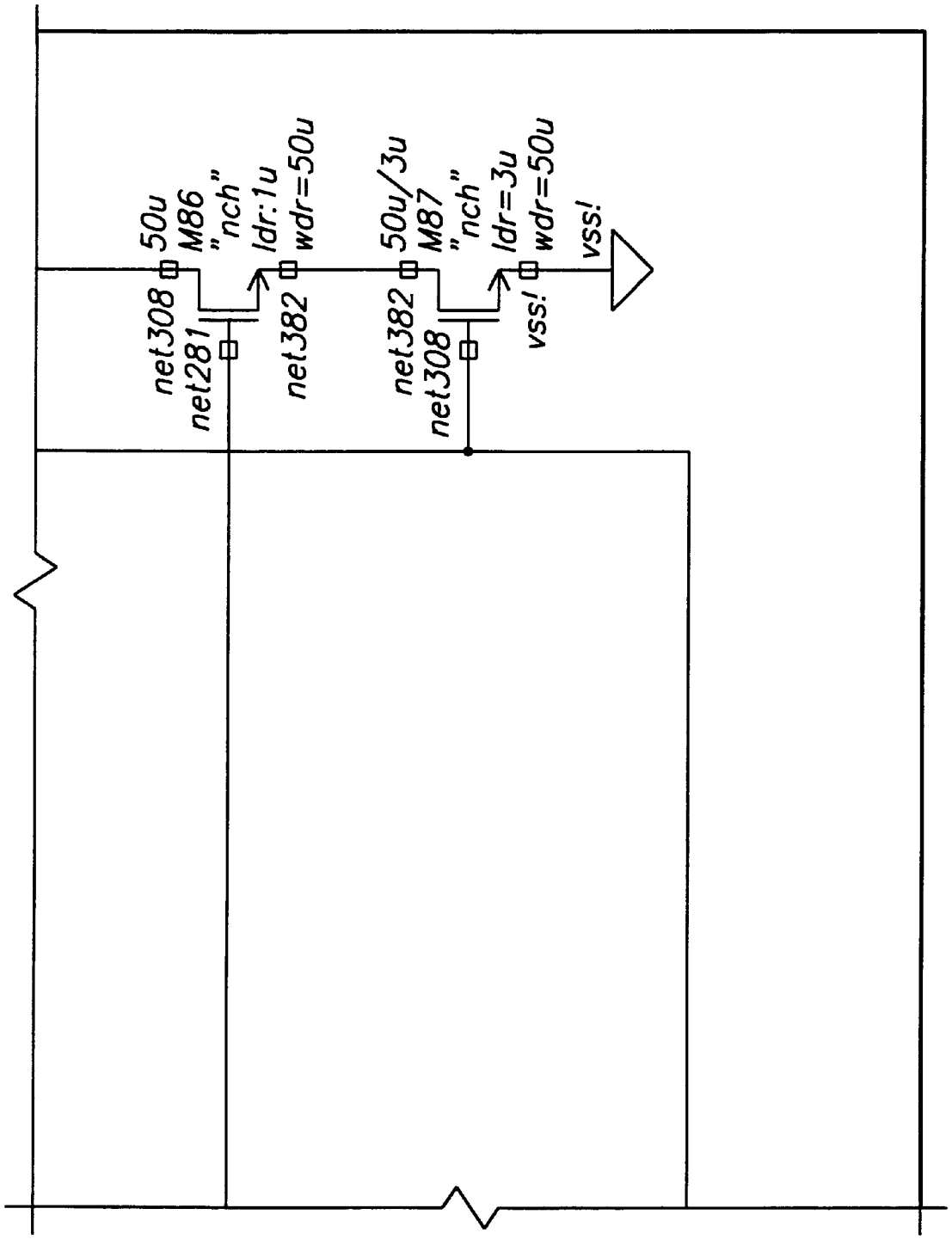
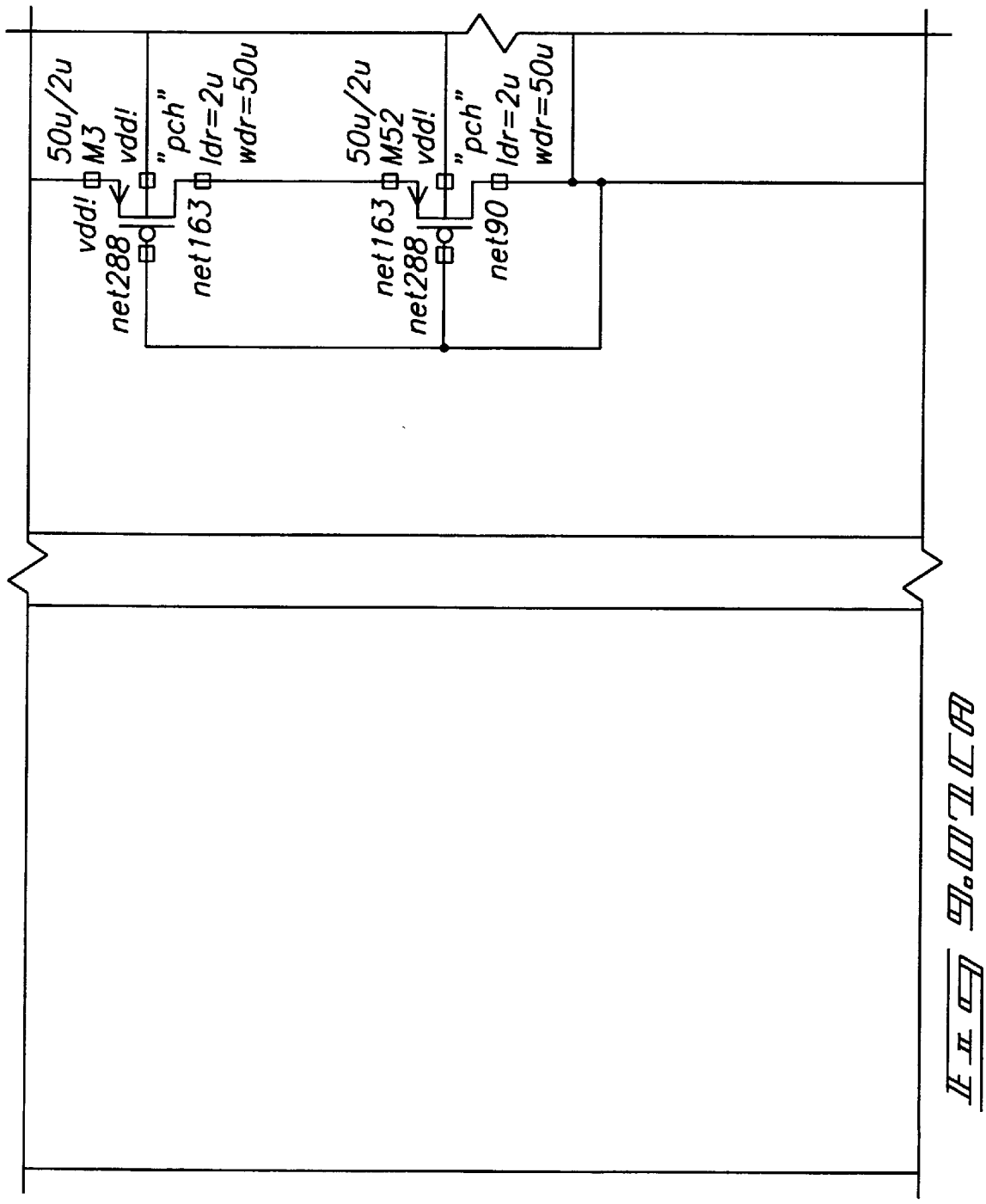

50u
M86
"nch"
ldr:1u
wdr=50u
50u/3u
M87
"nch"
ldr=3u
wdr=50u
vss!
net308
net281
net382
net382
net308
vss!

FIG 5,011 III


50u/2u
M3
vdd!
"pch"
ldr=2u
wdr=50u
vdd!
net288
net163
50u/2u
M52
vdd!
"pch"
ldr=2u
wdr=50u
net163
net288
net90

Фиг. 9.0114

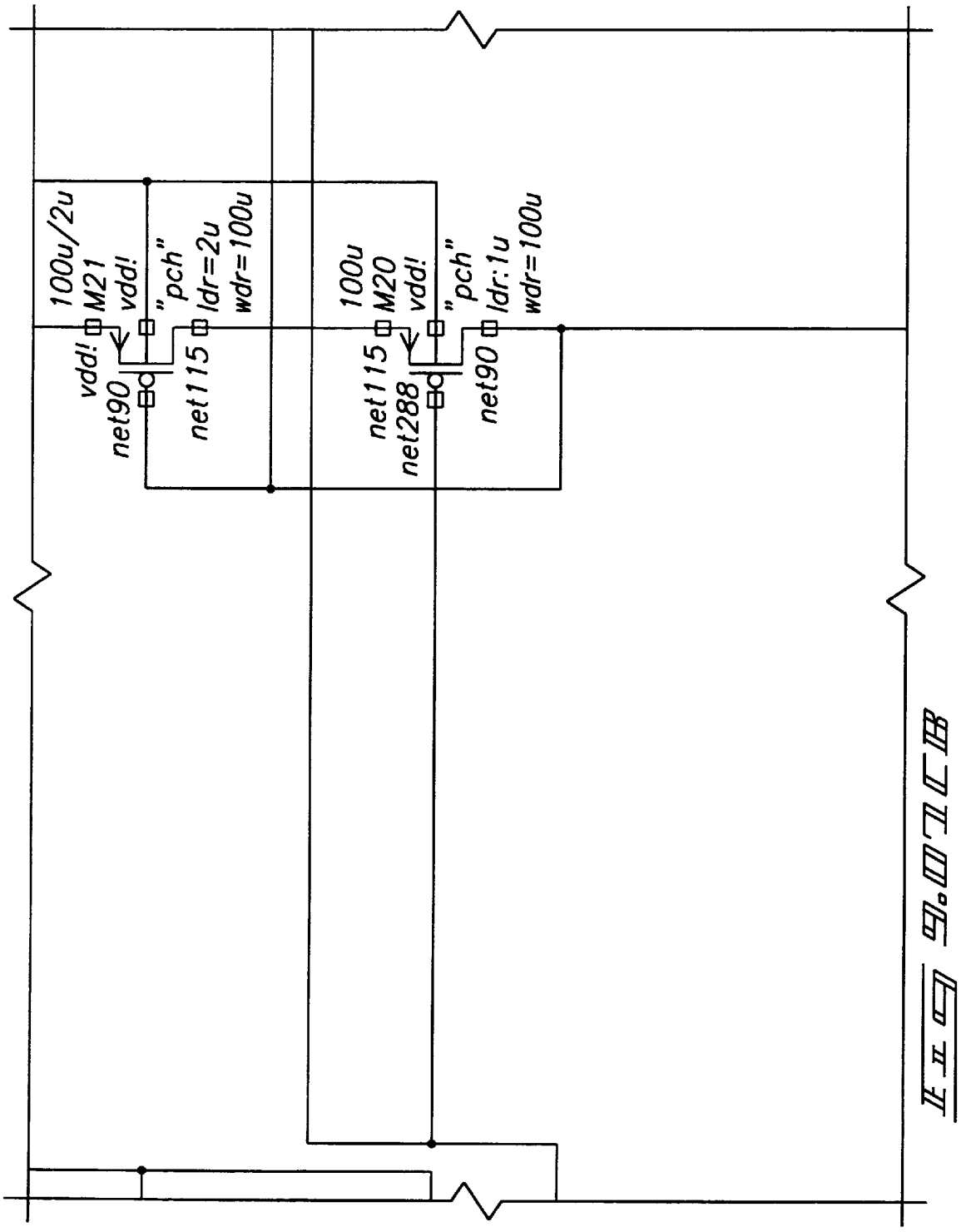

100u/2u
M21
vdd!
"pch"
ldr=2u
wdr=100u
vdd!
net90
net115
100u
M20
vdd!
"pch"
ldr:1u
wdr=100u
net115
net288
net90

FIG. 90,011

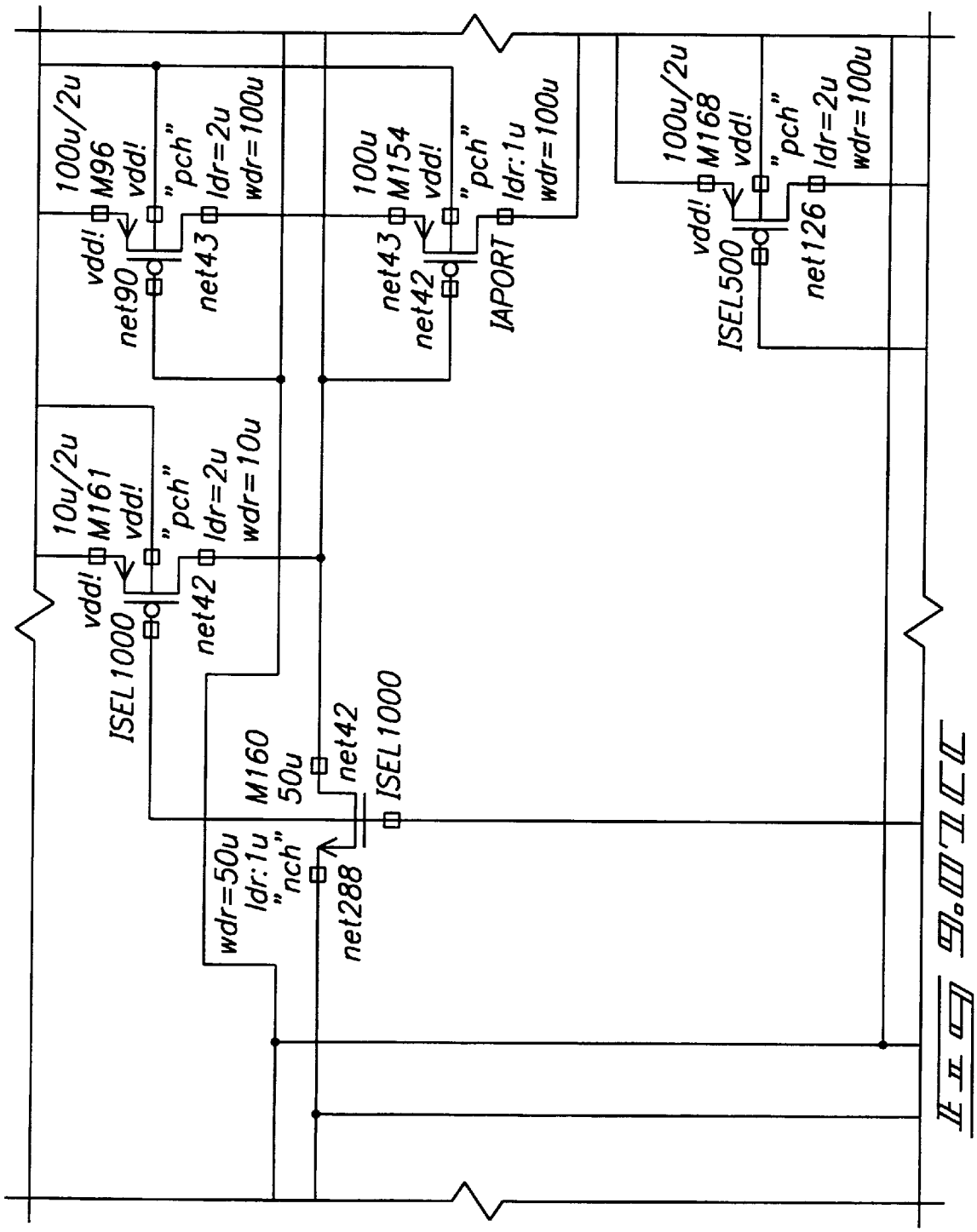

100u/2u
M96
vdd!
"pch"
ldr=2u
wdr=100u
vdd!
net90
net43
100u
M154
vdd!
"pch"
ldr:1u
wdr=100u
net43
net42
IAPORT
100u/2u
M168
vdd!
"pch"
ldr=2u
wdr=100u
vdd!
ISEL500
net126
10u/2u
M161
vdd!
"pch"
ldr=2u
wdr=10u
vdd!
ISEL1000
net42
M160
50u
net42
ISEL1000
wdr=50u
ldr:1u
"nch"
net288

Fig. 6,000,602

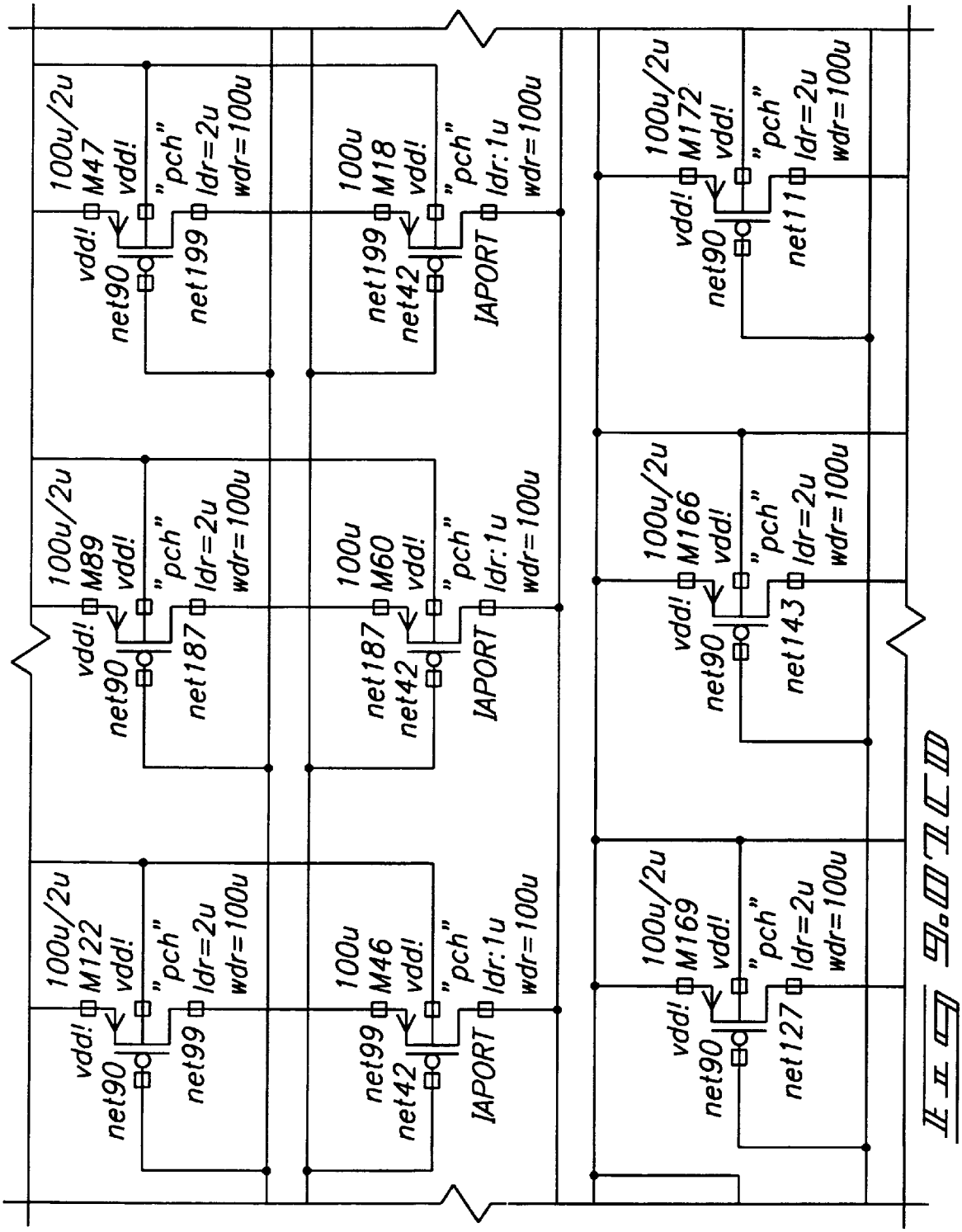

100u/2u
M47
vdd!
"pch"
ldr=2u
wdr=100u
net90
net199
100u
M18
net42
IAPORT
ldr:1u
M172
net11
M89
net187
M60
M166
net143
M122
net99
M46
M169
net127

FIG. 65

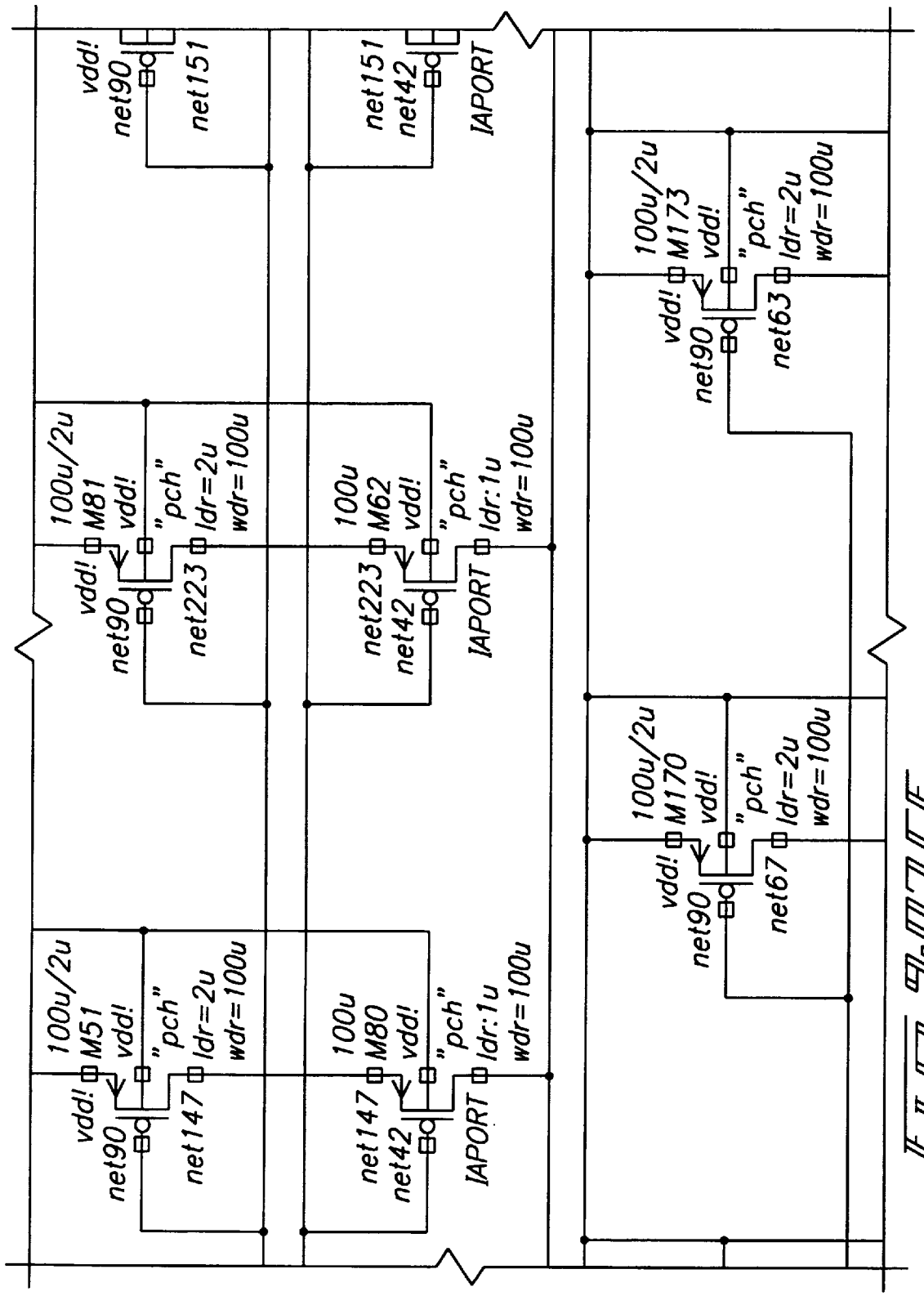

vdd!
net90
net151
net151
net42
IAPORT
100u/2u
M81
vdd!
"pch"
ldr=2u
wdr=100u
net223
100u
M62
ldr:1u
100u/2u
M173
net63
100u/2u
M170
net67
100u/2u
M51
net147
100u
M80
net147

FIG. 99.00LE

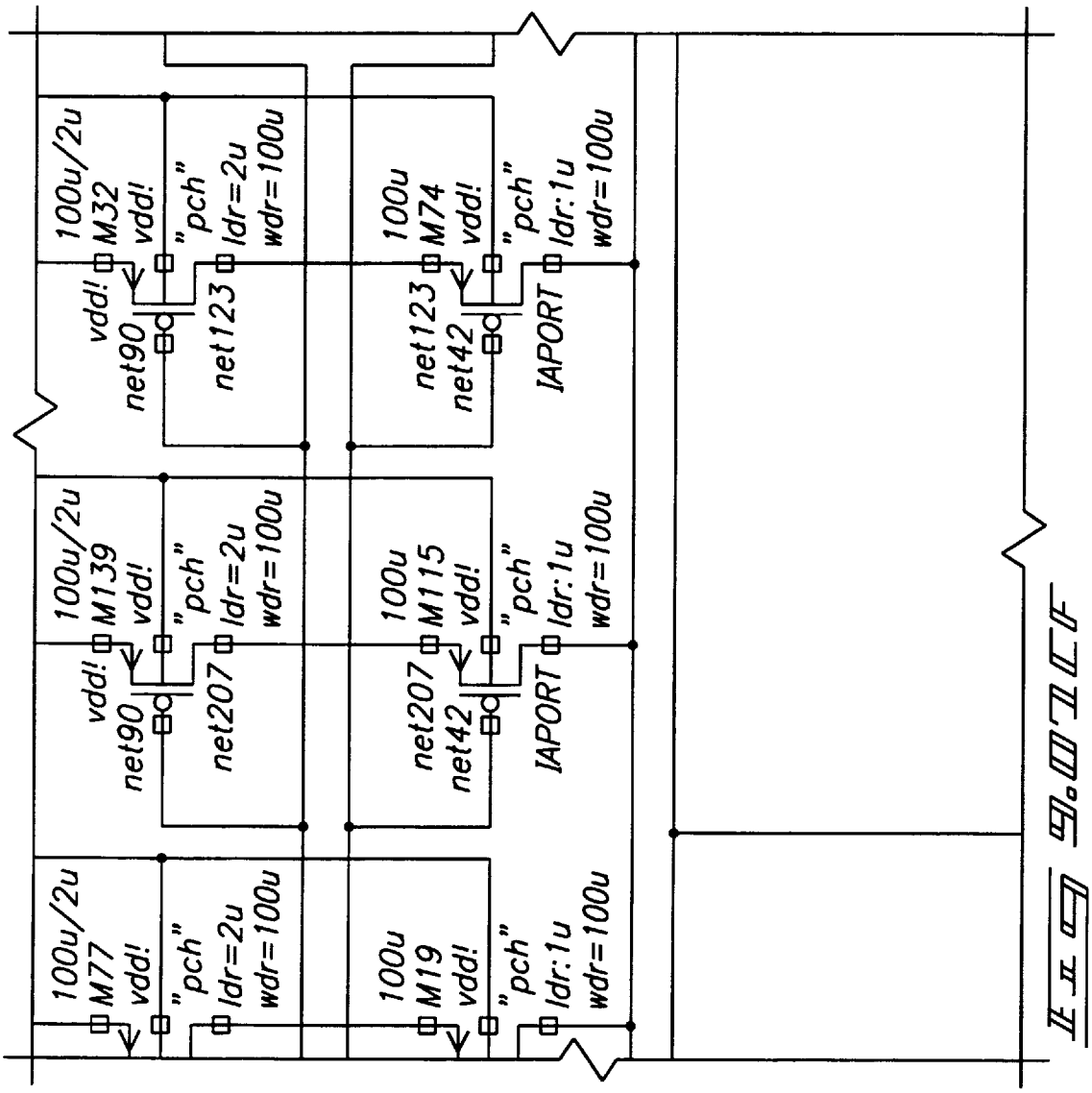
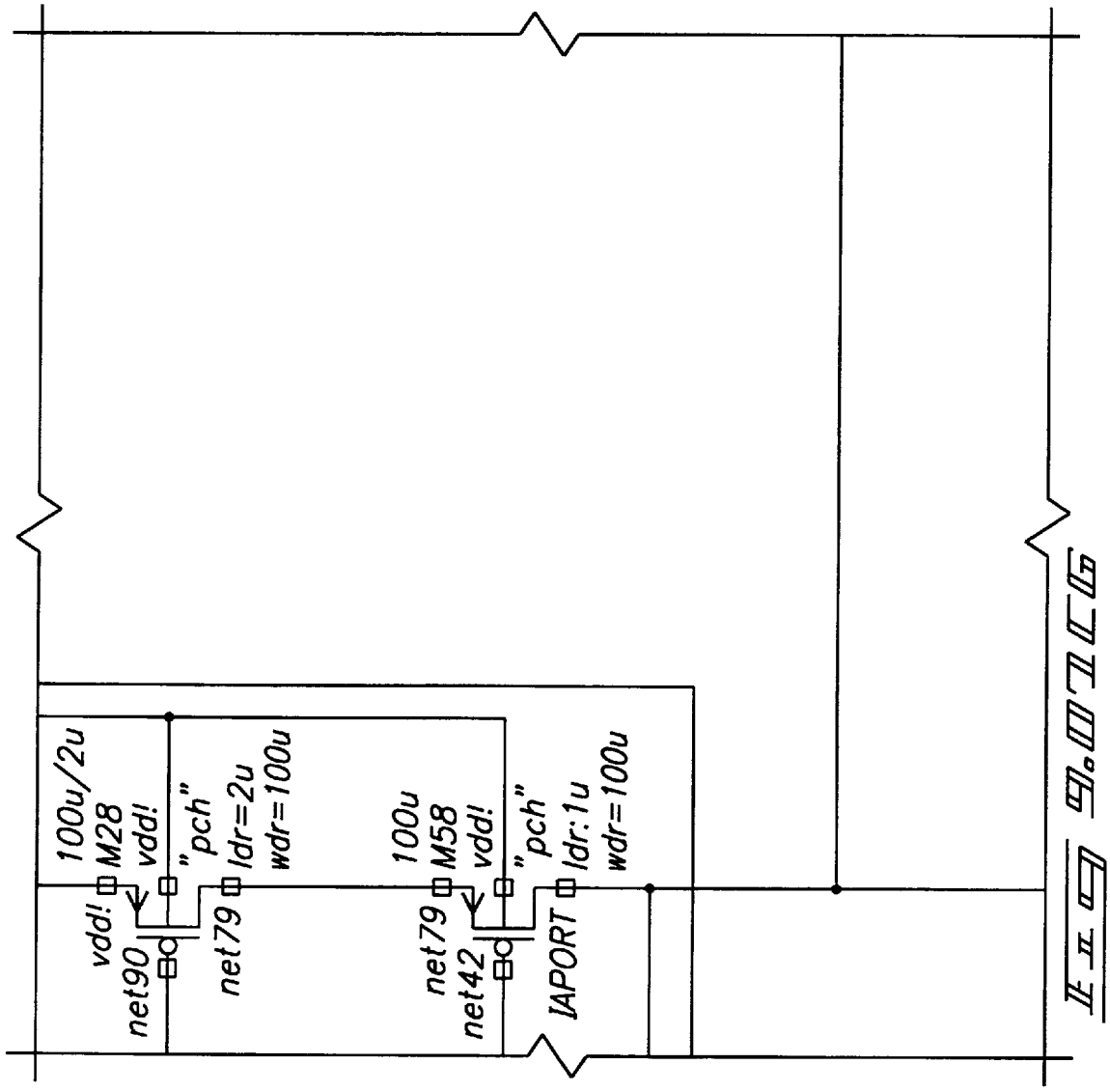
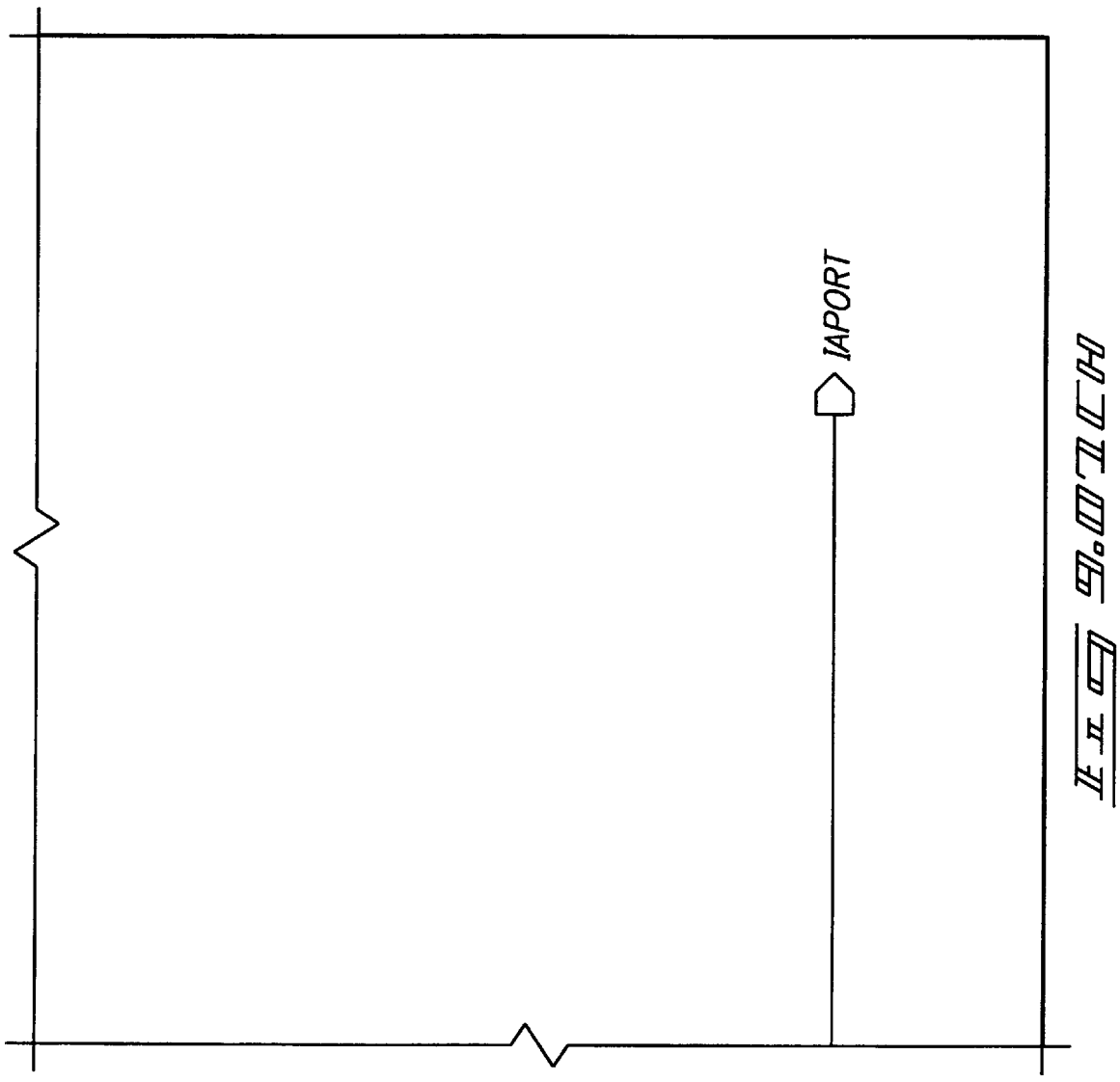

100u/2u
M32
vdd!
"pch"
ldr=2u
wdr=100u
vdd!
net90
net123
100u
M74
vdd!
"pch"
ldr:1u
wdr=100u
net123
net42
IAPORT
100u/2u
M139
vdd!
"pch"
ldr=2u
wdr=100u
vdd!
net90
net207
100u
M115
vdd!
"pch"
ldr:1u
wdr=100u
net207
net42
IAPORT
100u/2u
M77
vdd!
"pch"
ldr=2u
wdr=100u
100u
M19
vdd!
"pch"
ldr:1u
wdr=100u

FIG 9.0775


100u/2u
M28
vdd!
"pch"
ldr=2u
wdr=100u
vdd!
net90
net79
100u
M58
vdd!
"pch"
ldr:1u
wdr=100u
net79
net42
IAPORT


IAPORT
FIG. 95

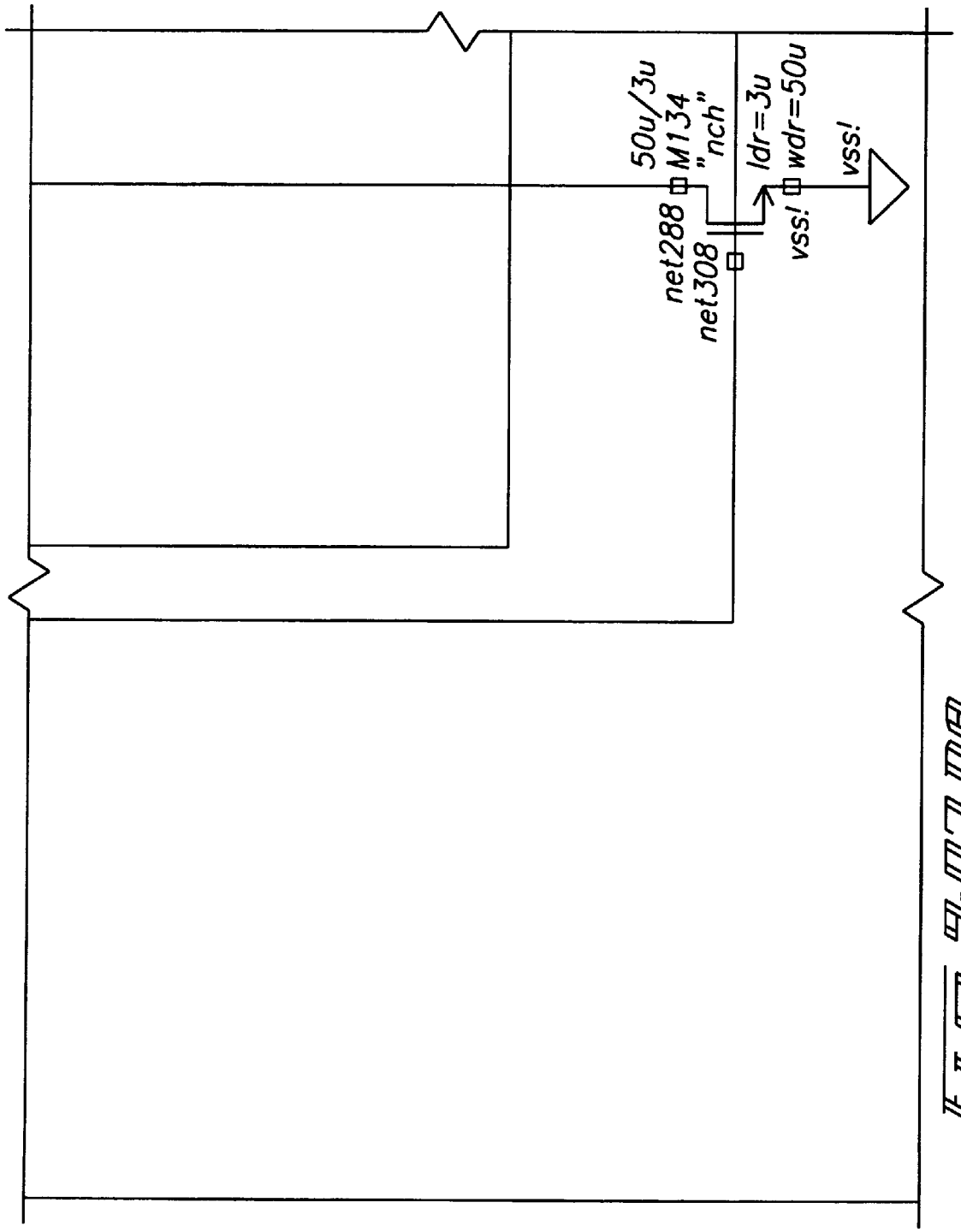


FIG. 9.0211A

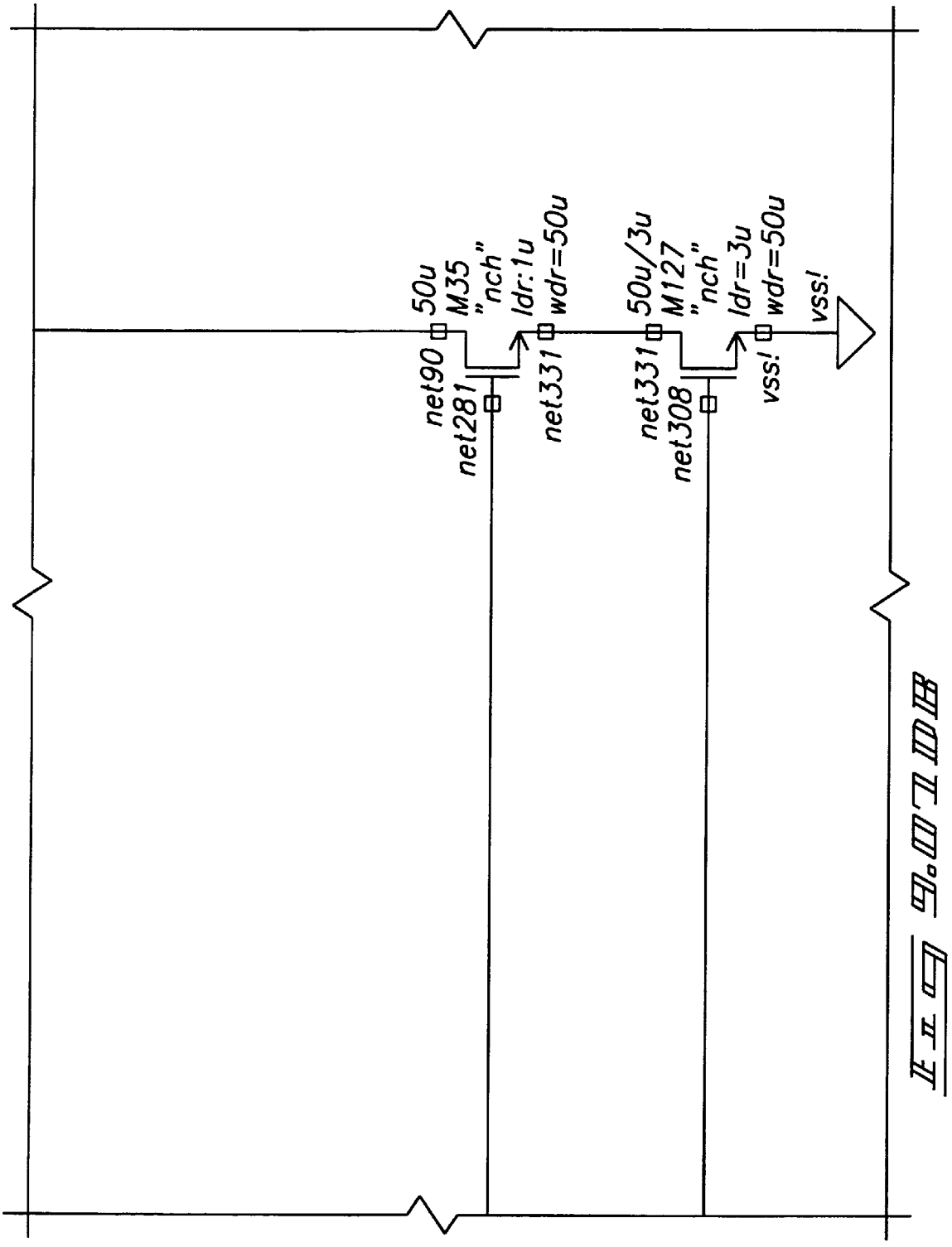
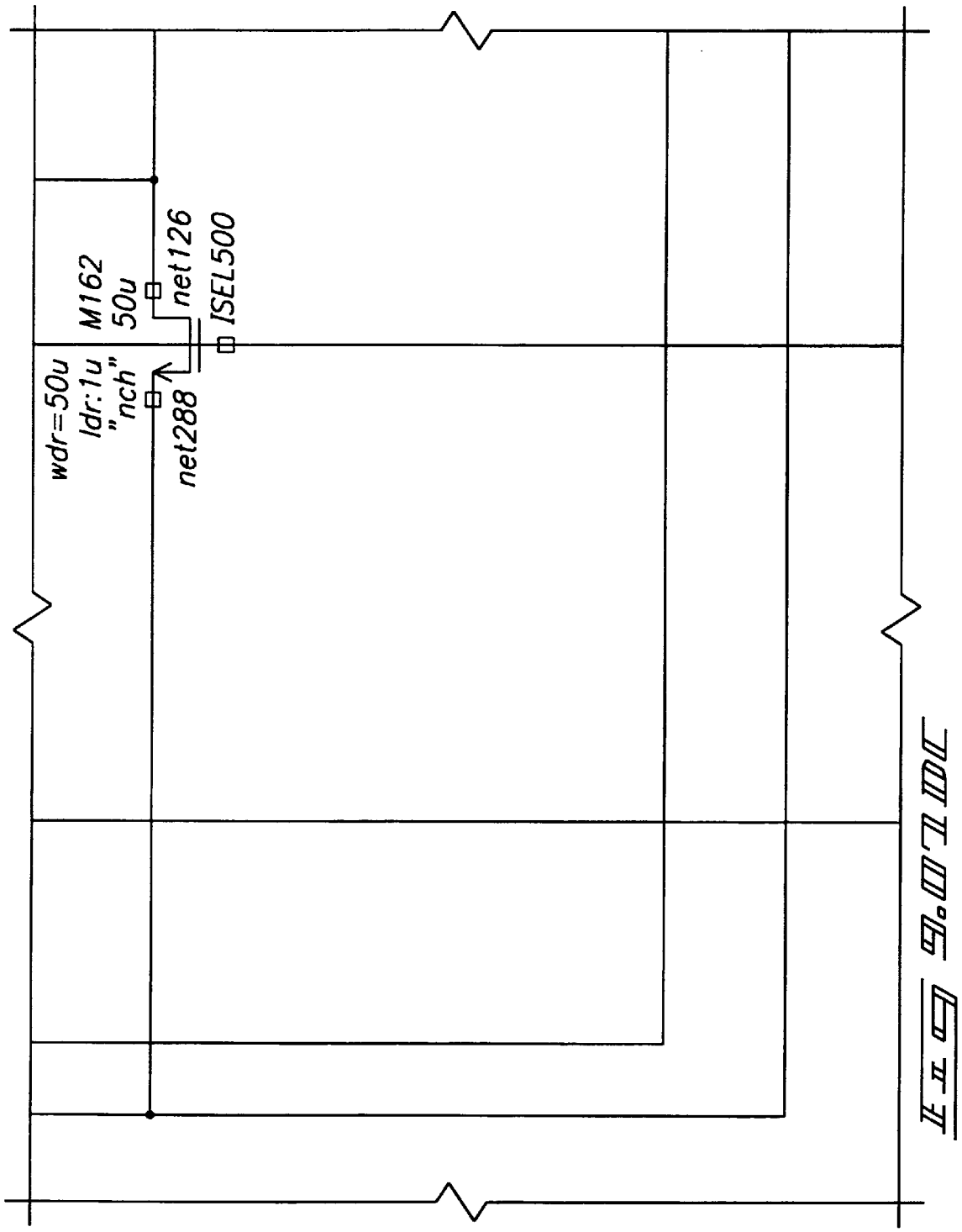
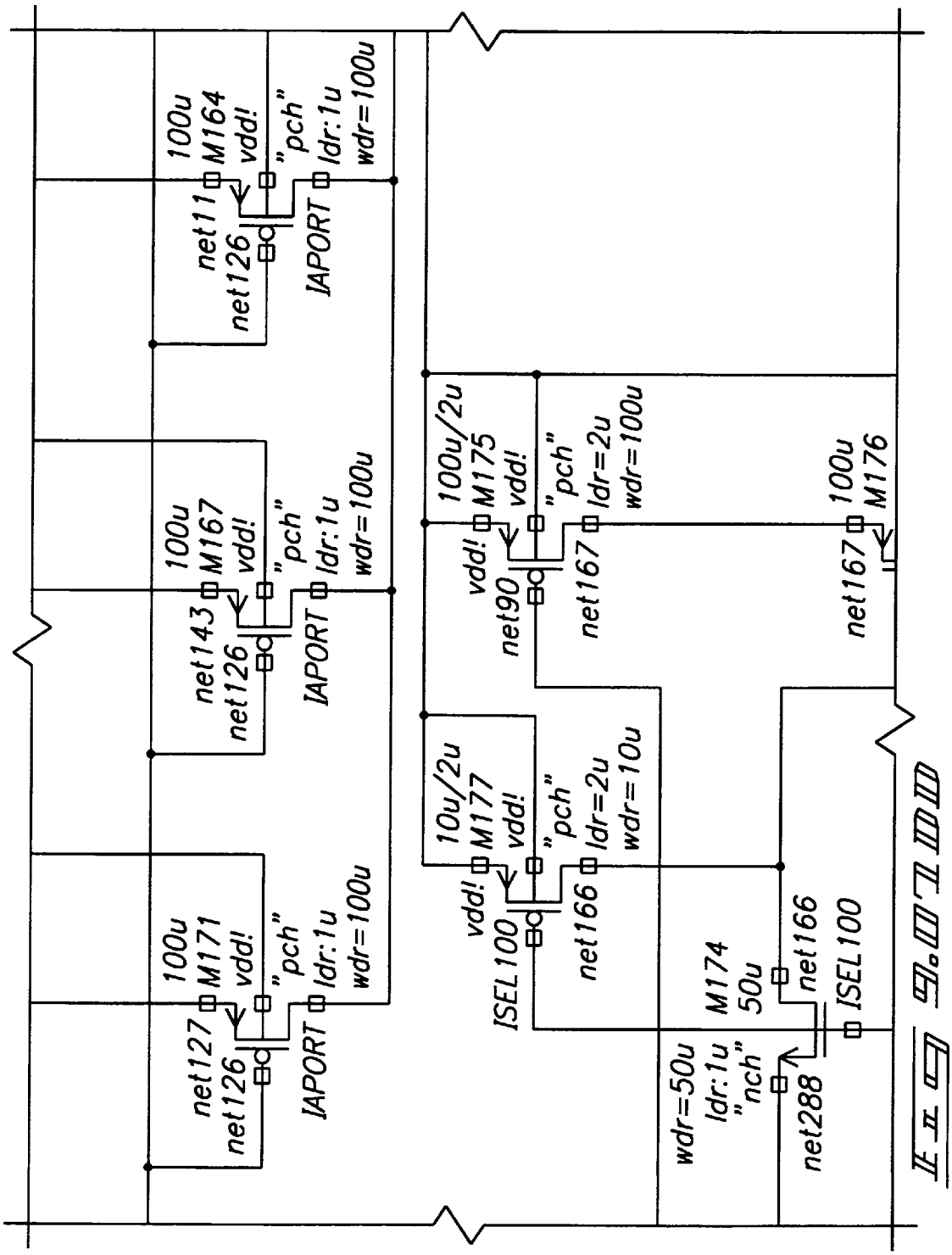

50u
M35
"nch"
ldr:1u
wdr=50u
50u/3u
M127
"nch"
ldr=3u
wdr=50u
vss!
net90
net281
net331
net331
net308
vss!

FIG. 5.6.0


M162
50u
net126
ISEL500
wdr=50u
ldr:1u
"nch"
net288
FIG. 95,005


100u
M164
vdd!
"pch"
ldr:1u
wdr=100u
net11
net126
IAPORT
100u
M167
vdd!
"pch"
ldr:1u
wdr=100u
net143
net126
IAPORT
100u
M171
vdd!
"pch"
ldr:1u
wdr=100u
net127
net126
IAPORT
100u/2u
M175
vdd!
"pch"
ldr=2u
wdr=100u
vdd!
net90
net167
100u
M176
net167
10u/2u
M177
vdd!
"pch"
ldr=2u
wdr=10u
vdd!
ISEL100
net166
wdr=50u
ldr:1u
"nch"
M174
50u
net166
ISEL100
net288

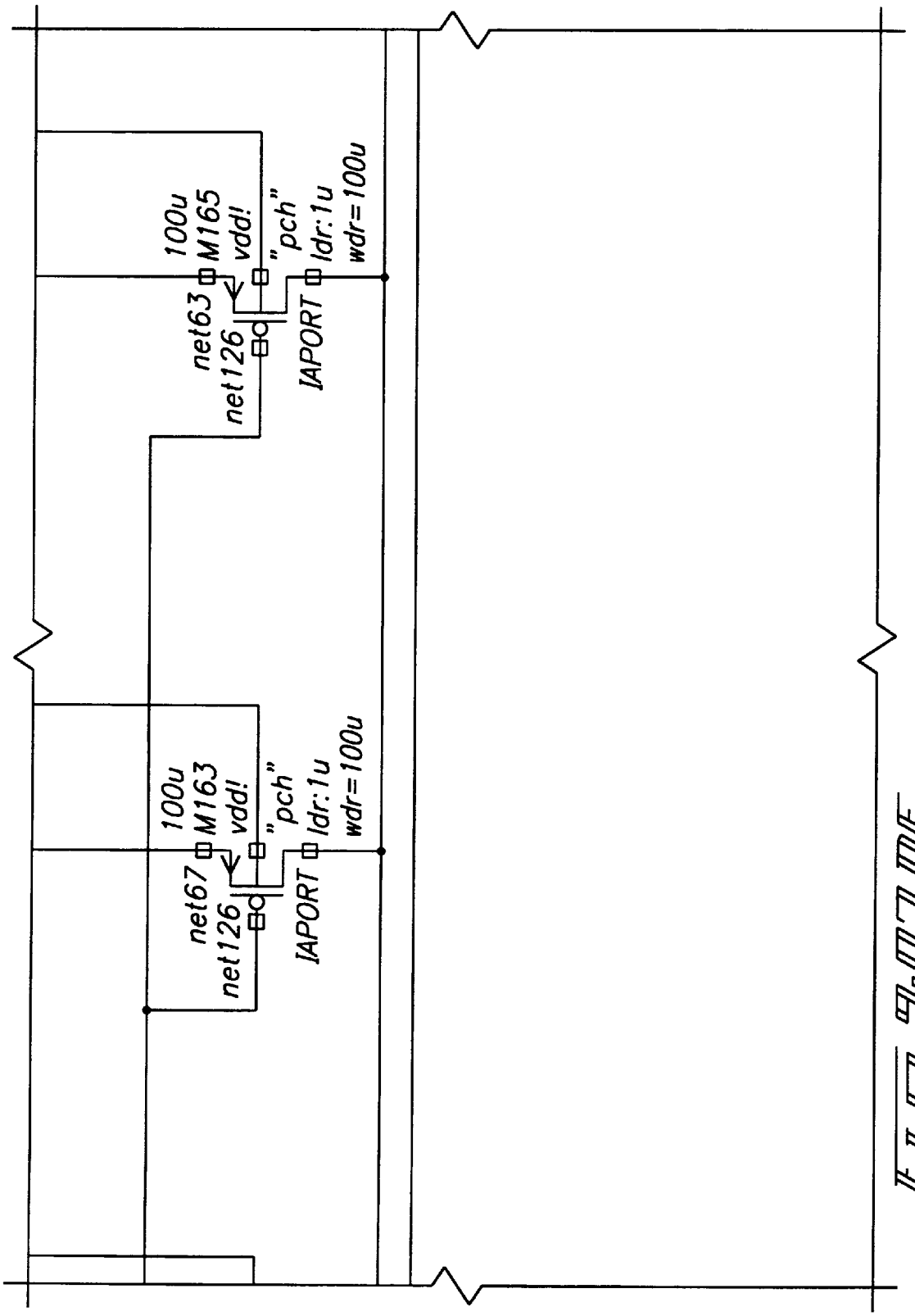

100u
M165
vdd!
"pch"
ldr:1u
wdr=100u
net63
net126
IAPORT
100u
M163
vdd!
"pch"
ldr:1u
wdr=100u
net67
net126
IAPORT

FIG. 9,001E

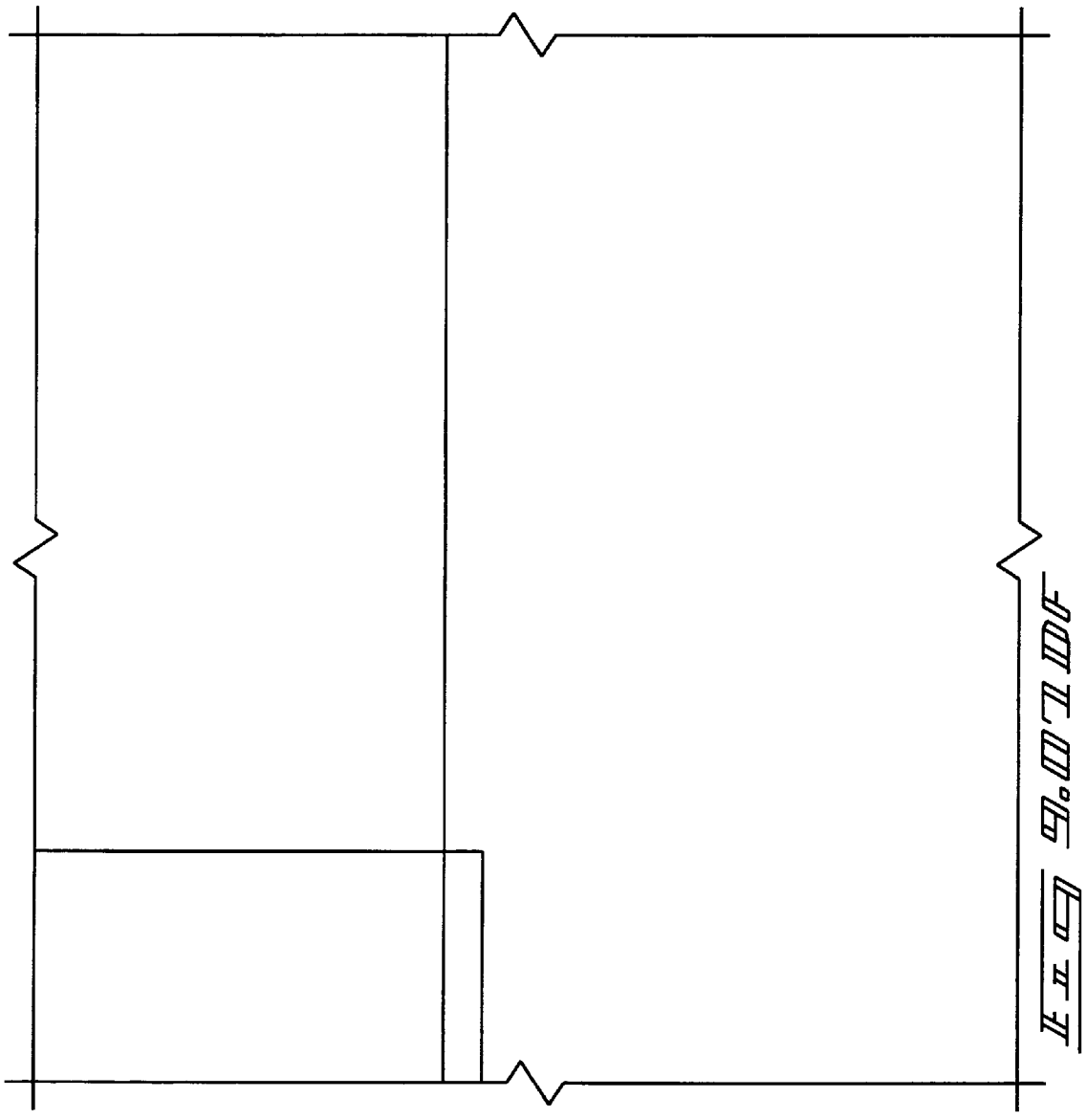


FIG 96

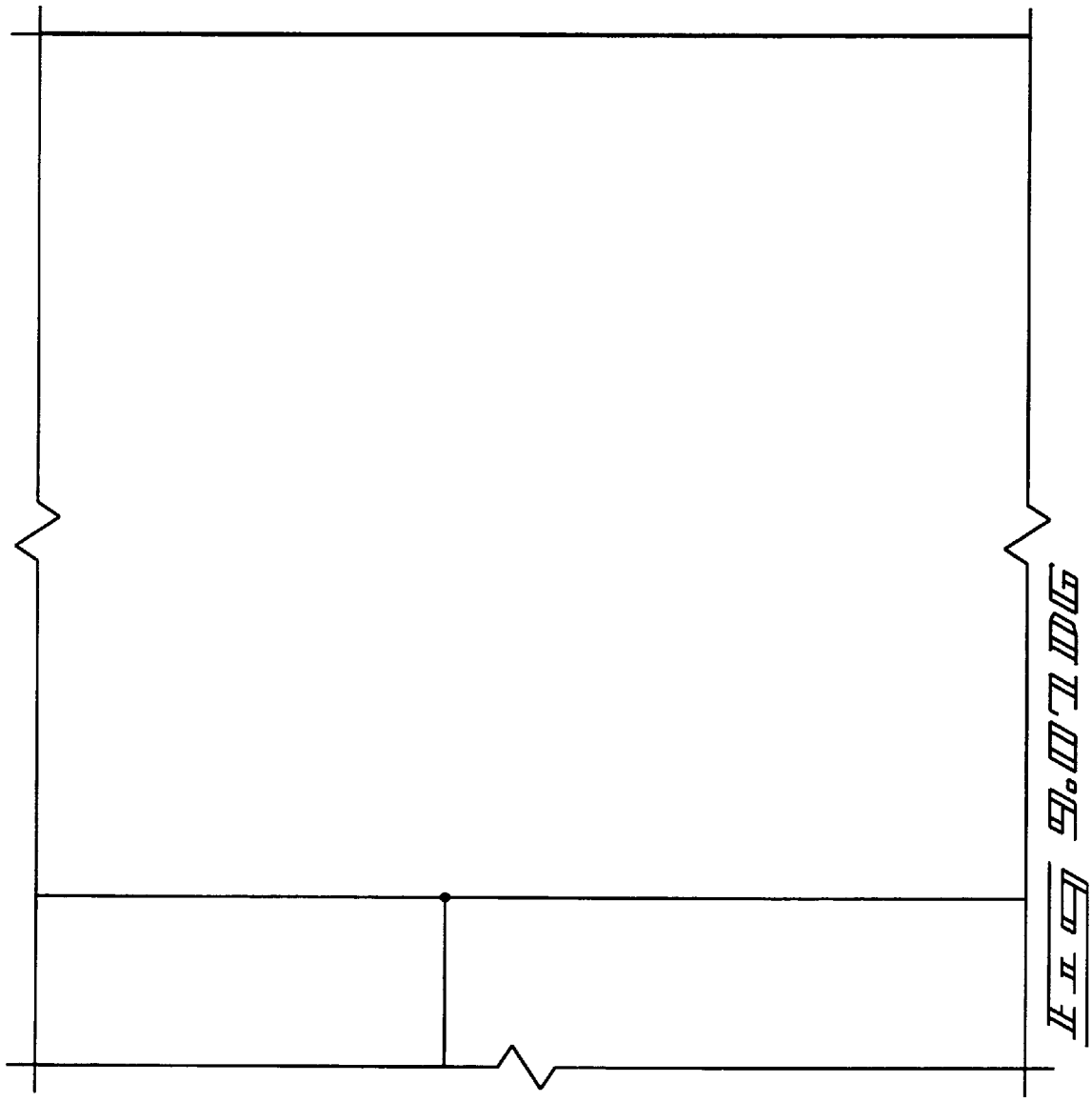


FIG 9,071,105

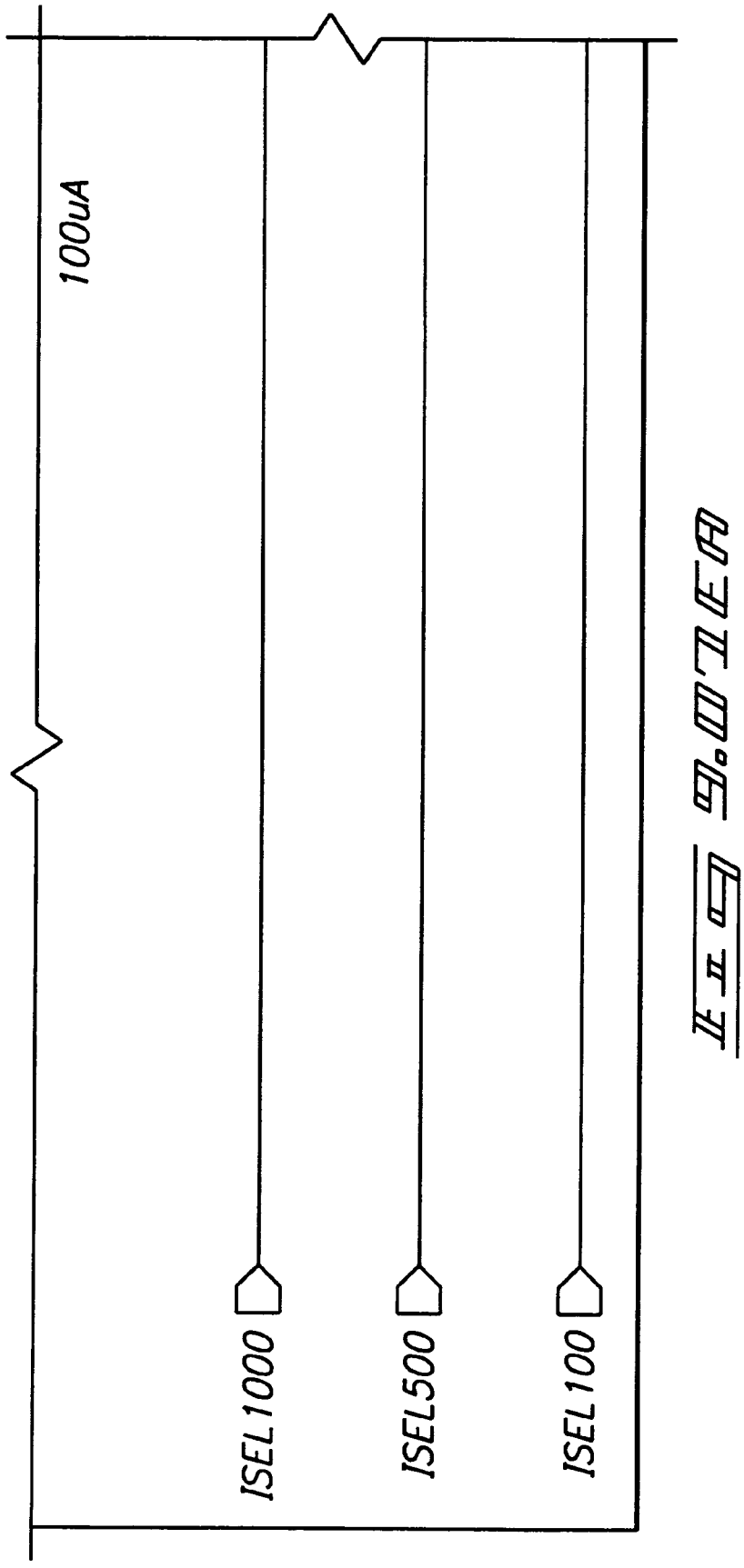
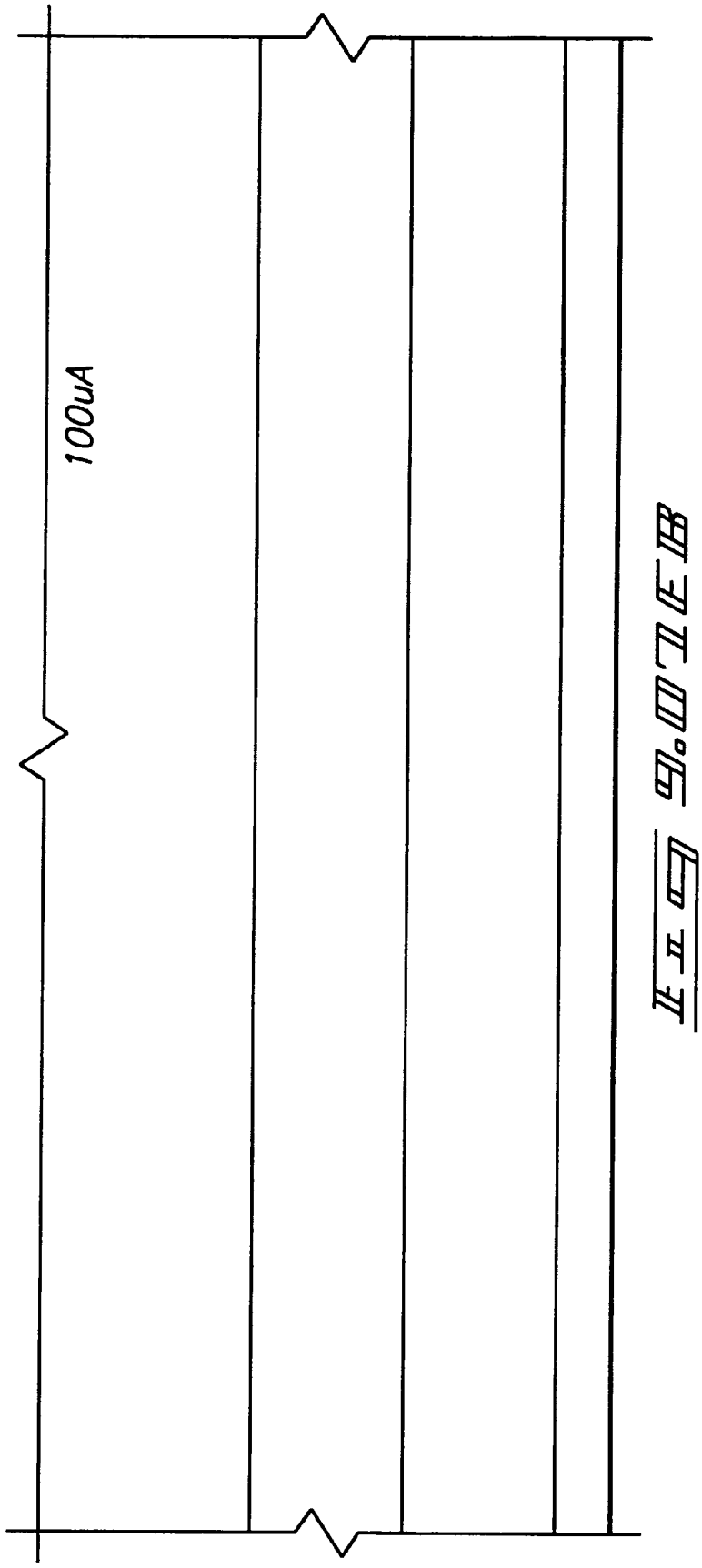


FIG 90.01EA


100uA
FIG 95.00

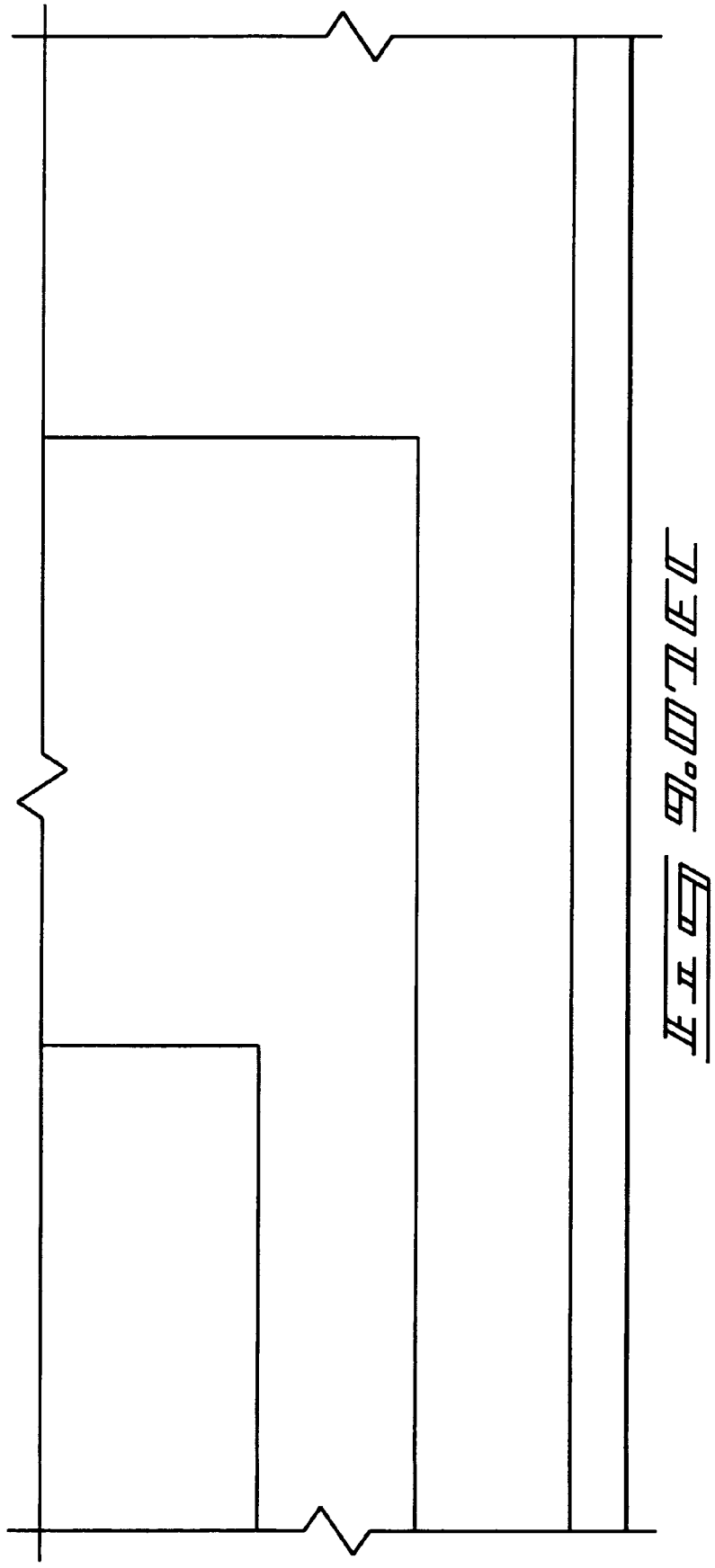


FIG. 9.00EE

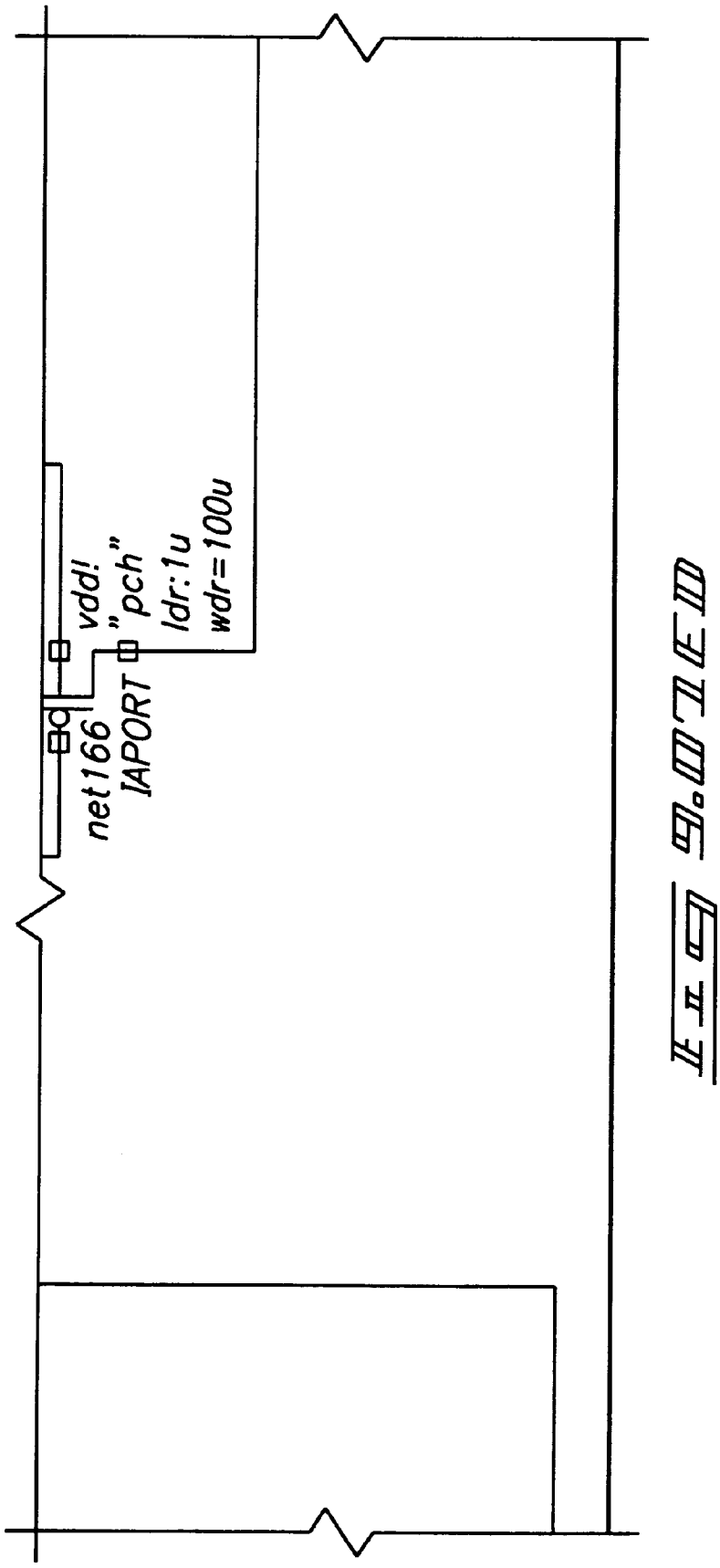


FIG. 59,077E

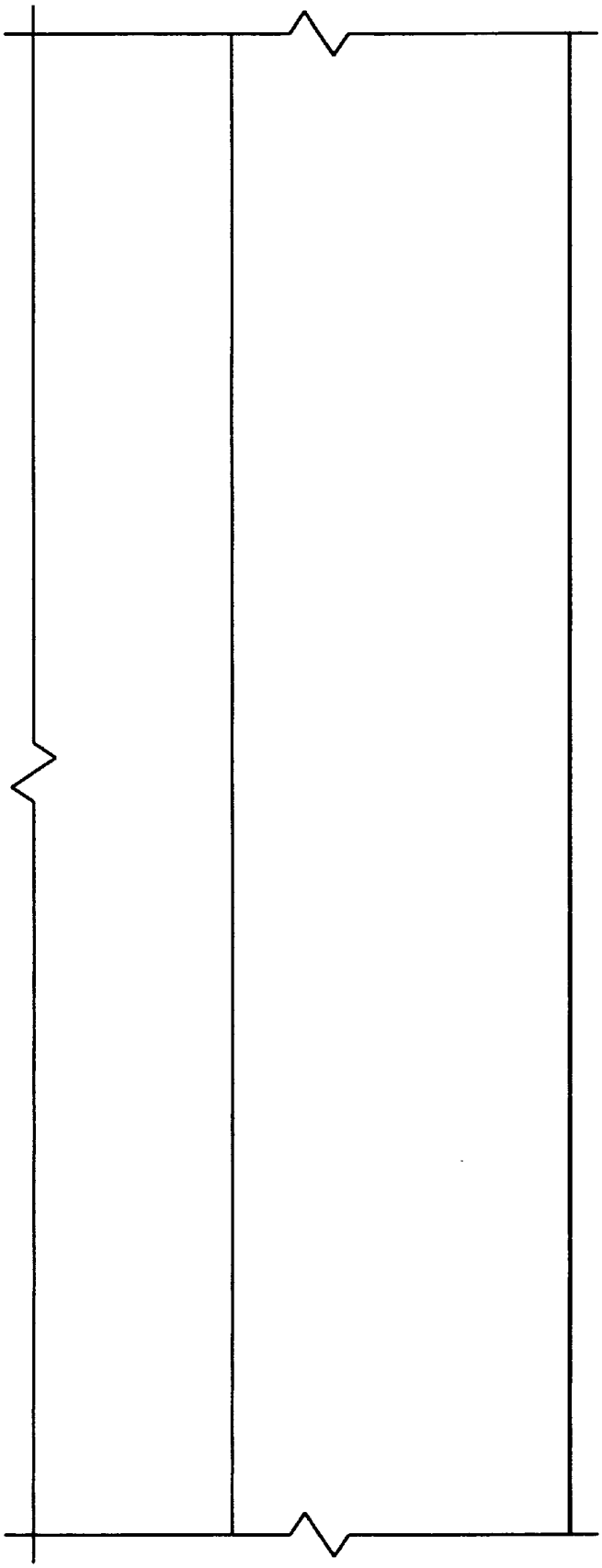


FIG. 90,011E

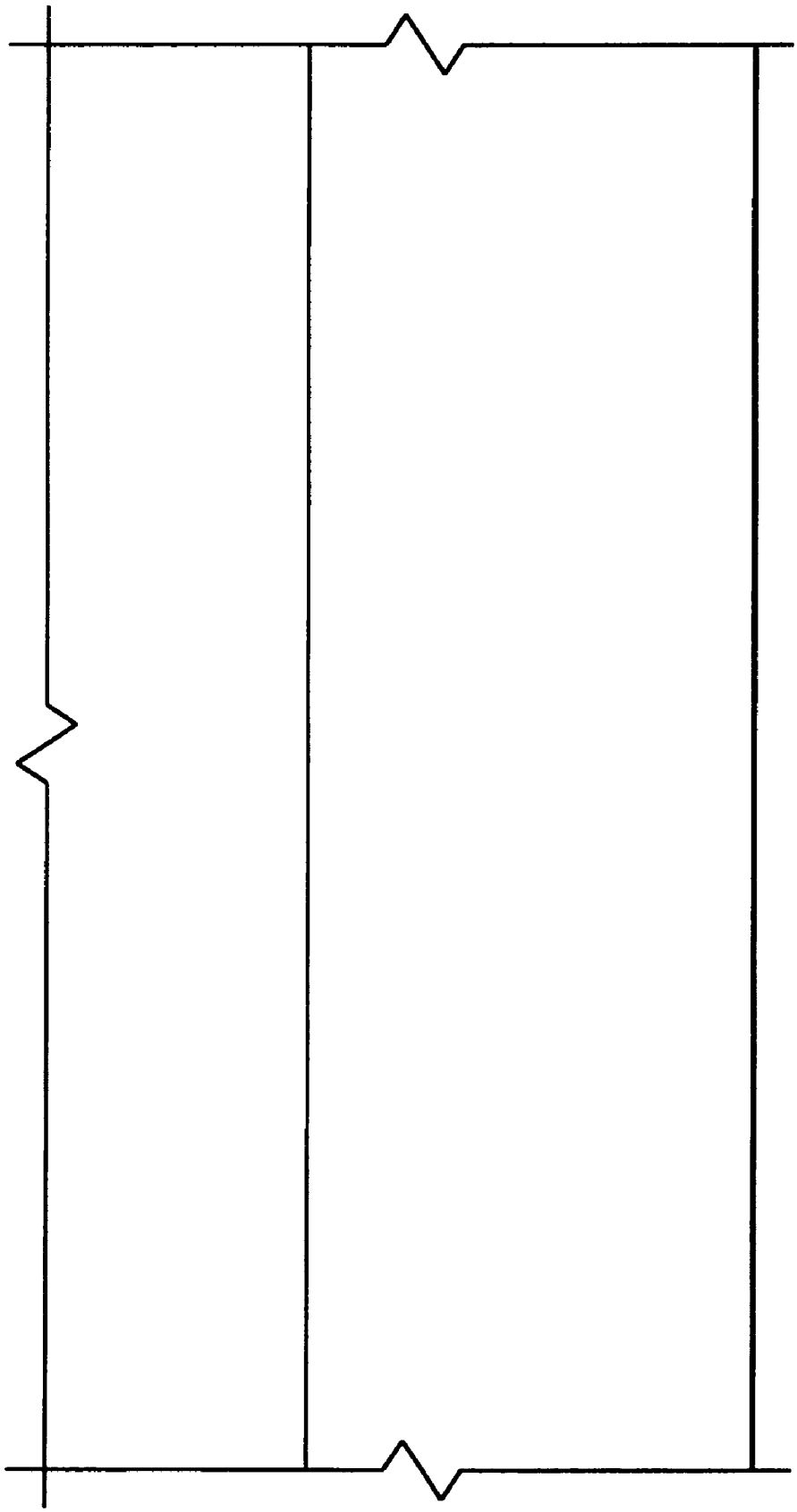


FIG 9,075F

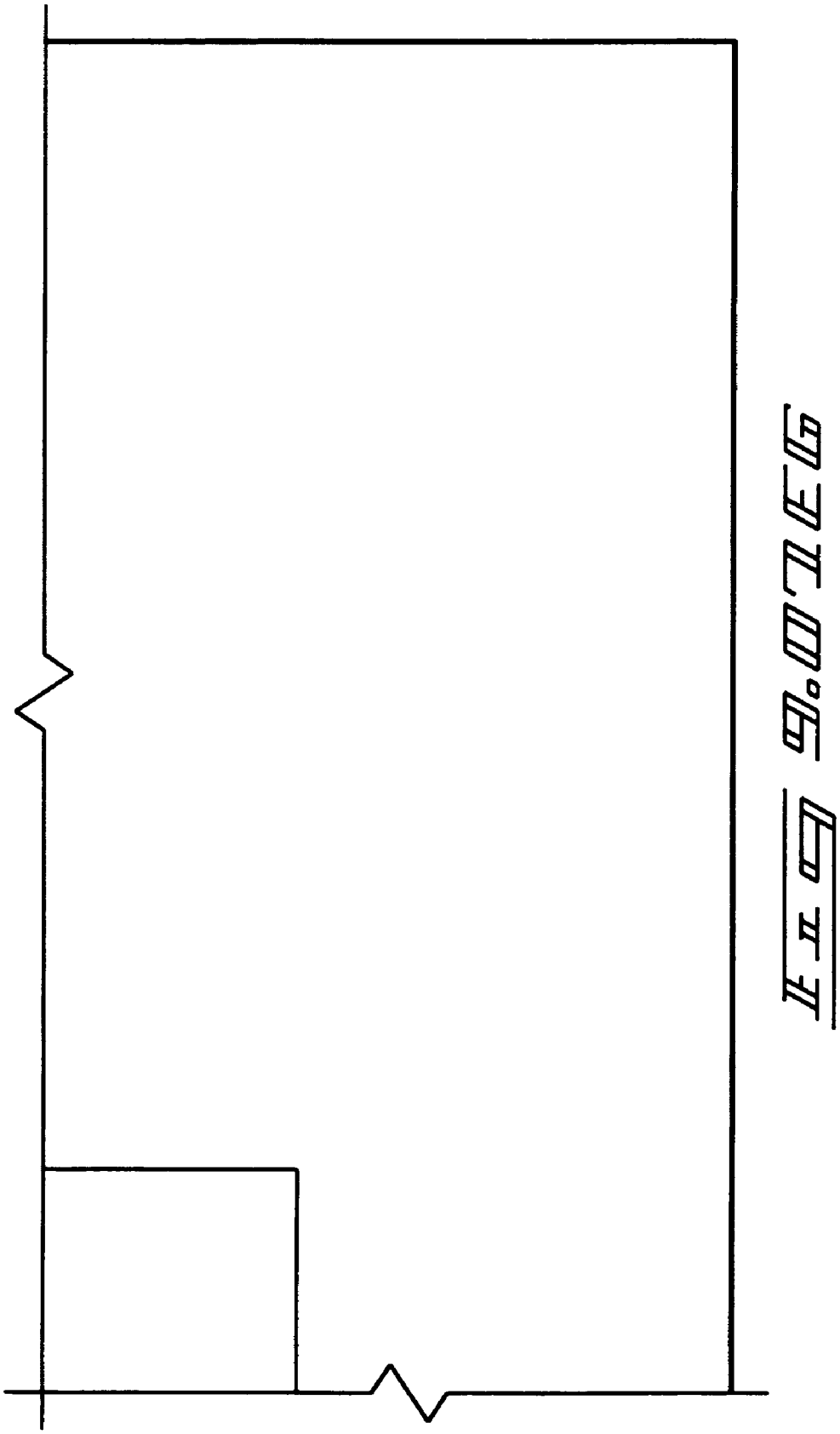


FIG 9,007E

9.08AA	9.08AB	9.08AC
9.08BA	9.08BB	9.08BC
9.08CA	9.08CB	9.08CC

Fig 9.08B

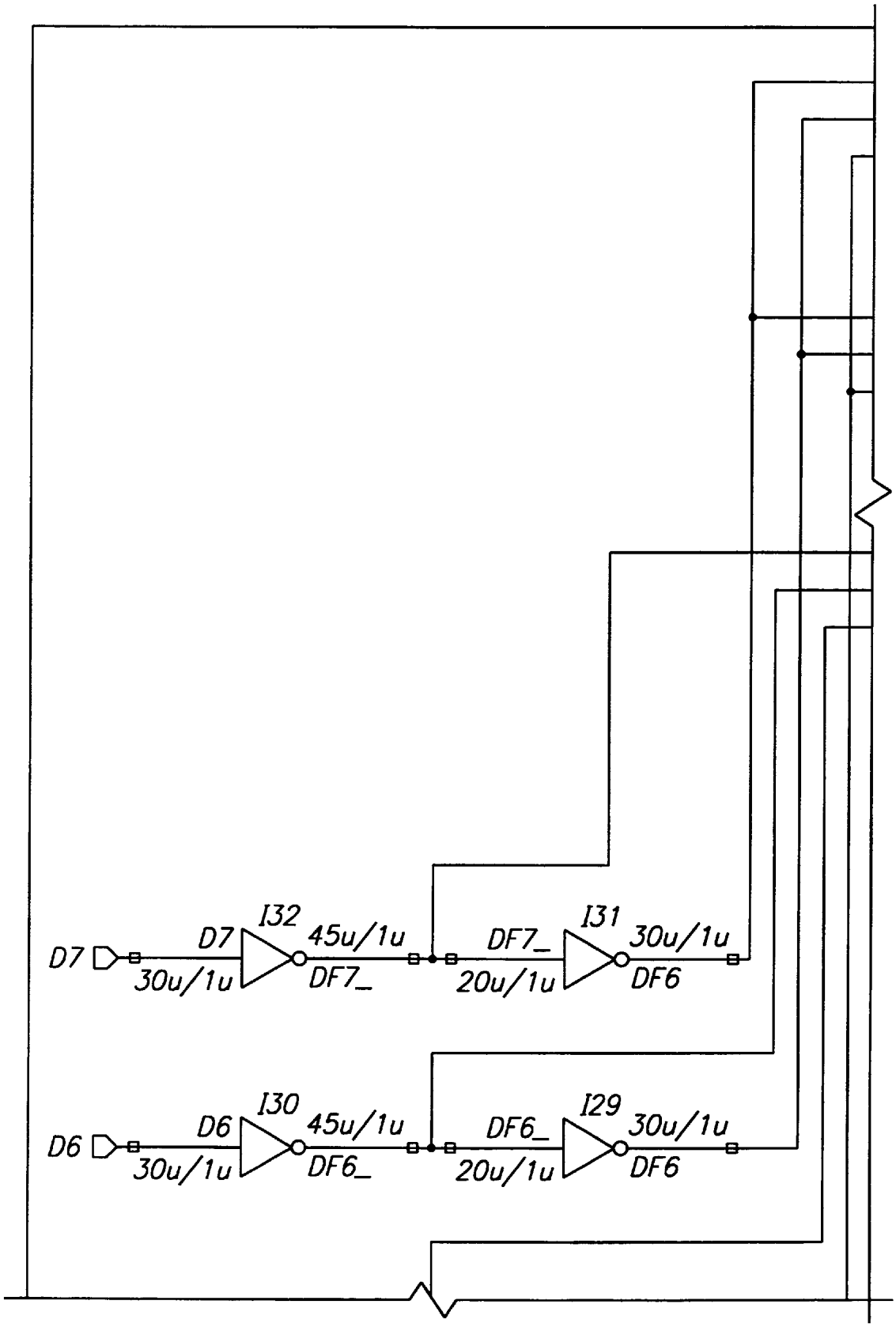
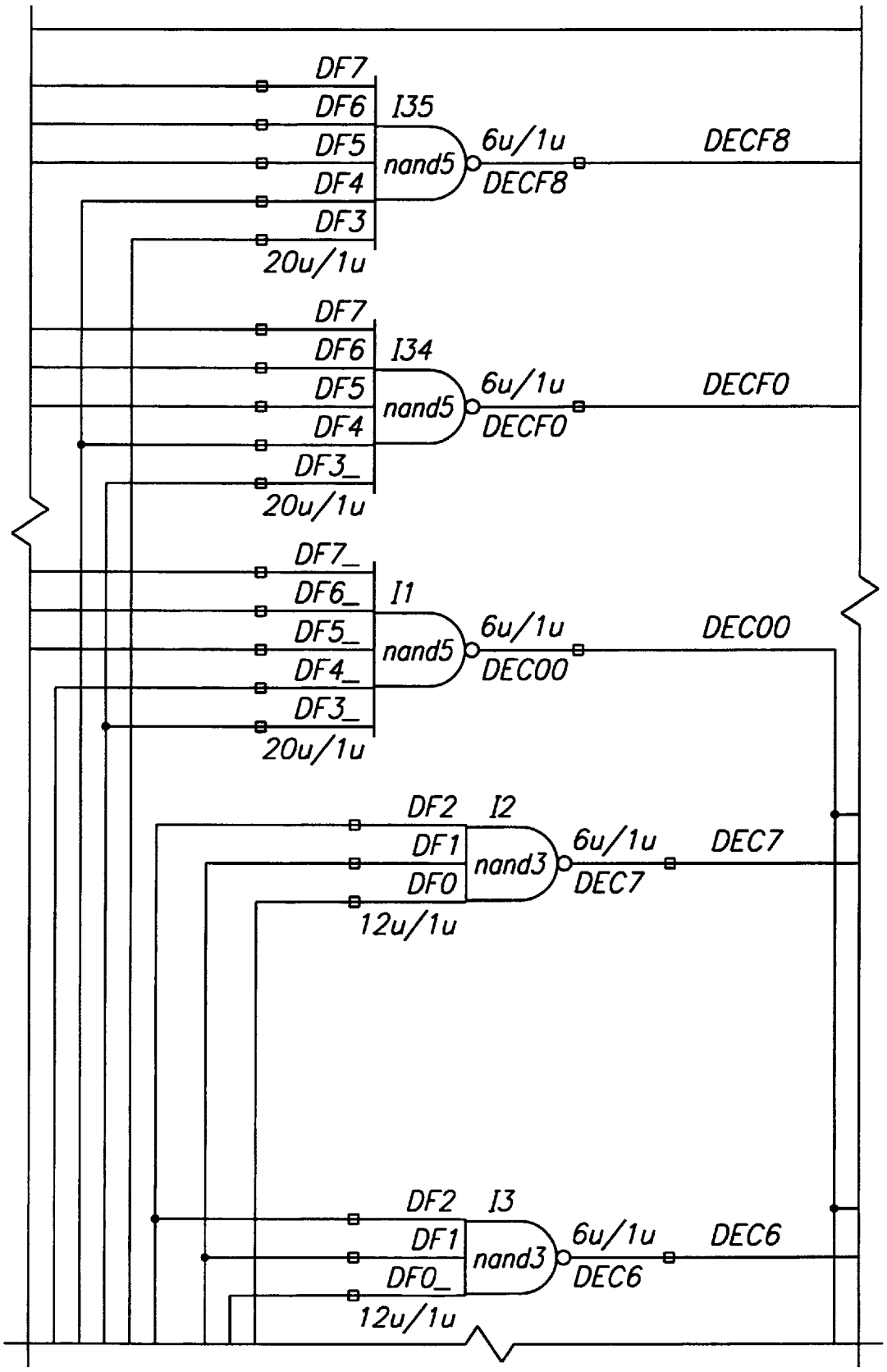

D7
30u/1u
D7
I32
45u/1u
DF7_
DF7_
20u/1u
I31
30u/1u
DF6
D6
30u/1u
D6
I30
45u/1u
DF6_
DF6_
20u/1u
I29
30u/1u
DF6

Fig 9.08AA


DF7
DF6
DF5
DF4
DF3
I35
nand5
6u/1u
20u/1u
DECF8
DF7
DF6
DF5
DF4
DF3_
I34
nand5
6u/1u
20u/1u
DECF0
DF7_
DF6_
DF5_
DF4_
DF3_
I1
nand5
6u/1u
20u/1u
DEC00
DF2
DF1
DF0
I2
nand3
6u/1u
12u/1u
DEC7
DF2
DF1
DF0_
I3
nand3
6u/1u
12u/1u
DEC6

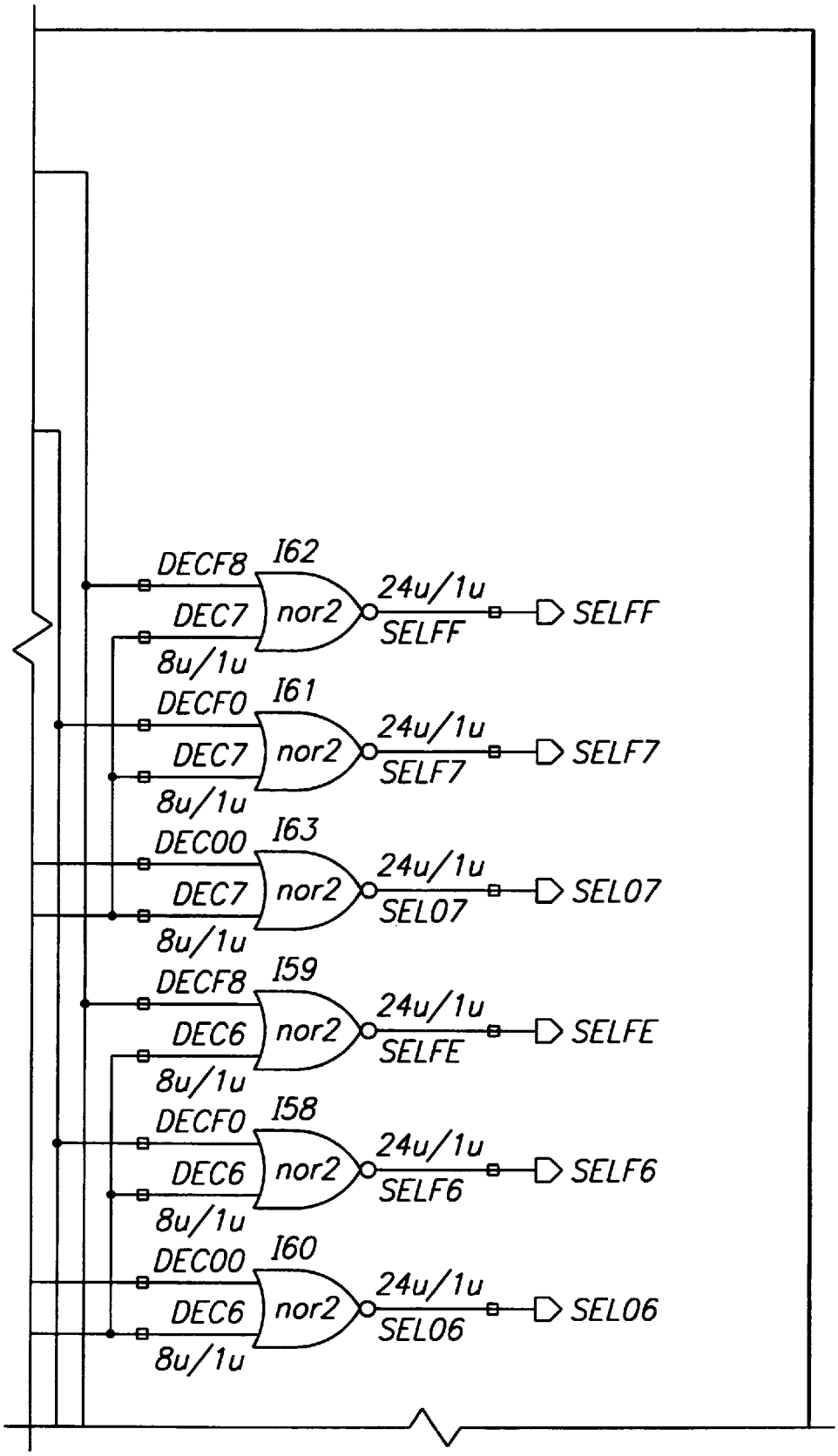

DECF8
DEC7
8u/1u
I62
nor2
24u/1u
SELFF
SELFF
DECF0
DEC7
8u/1u
I61
nor2
24u/1u
SELF7
SELF7
DEC00
DEC7
8u/1u
I63
nor2
24u/1u
SEL07
SEL07
DECF8
DEC6
8u/1u
I59
nor2
24u/1u
SELFE
SELFE
DECF0
DEC6
8u/1u
I58
nor2
24u/1u
SELF6
SELF6
DEC00
DEC6
8u/1u
I60
nor2
24u/1u
SEL06
SEL06

Fig 9.0880AC

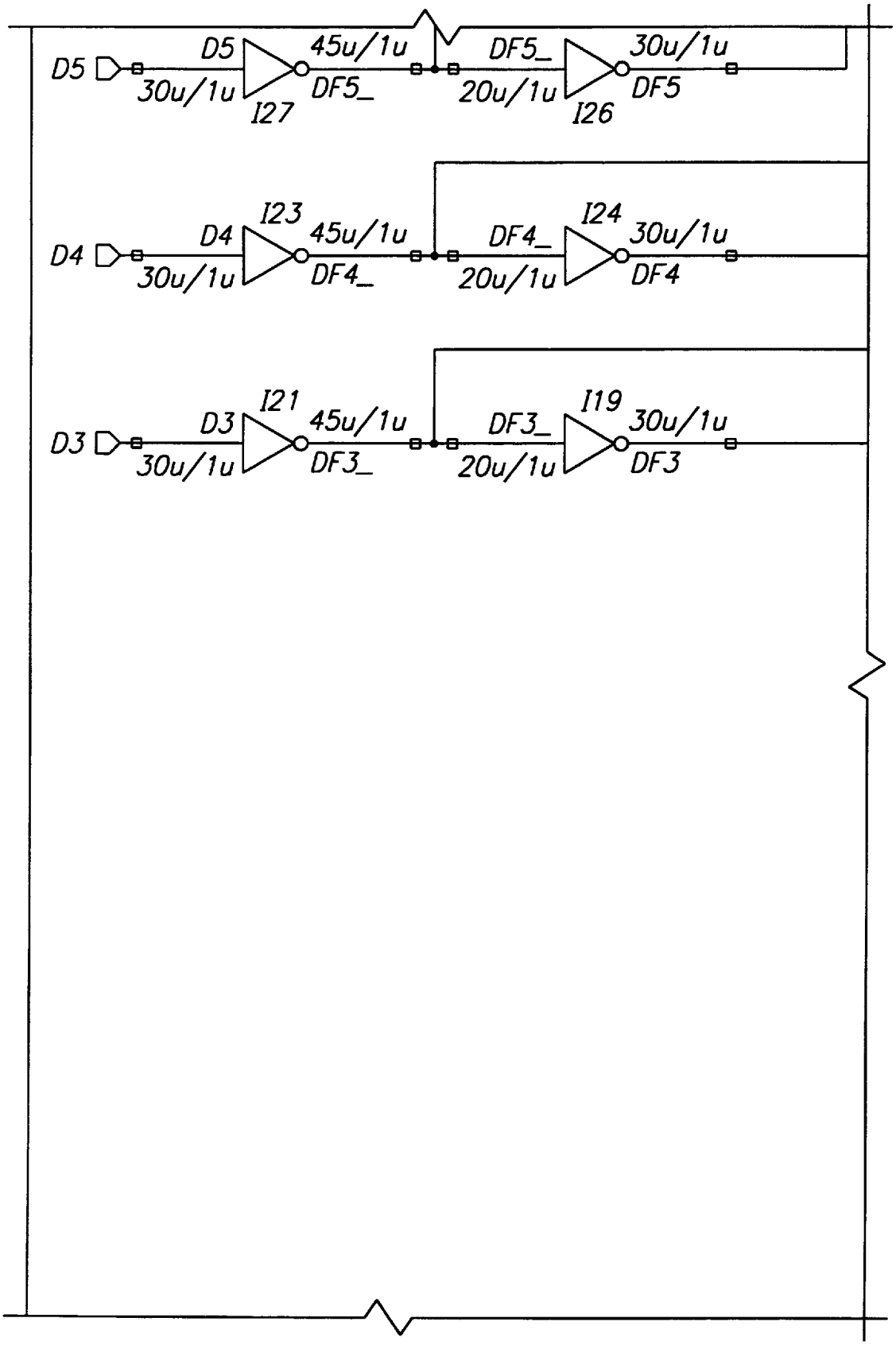

D5
D5
30u/1u
I27
45u/1u
DF5_
DF5_
20u/1u
I26
30u/1u
DF5
D4
D4
30u/1u
I23
45u/1u
DF4_
DF4_
20u/1u
I24
30u/1u
DF4
D3
D3
30u/1u
I21
45u/1u
DF3_
DF3_
20u/1u
I19
30u/1u
DF3

Fig 9.088A

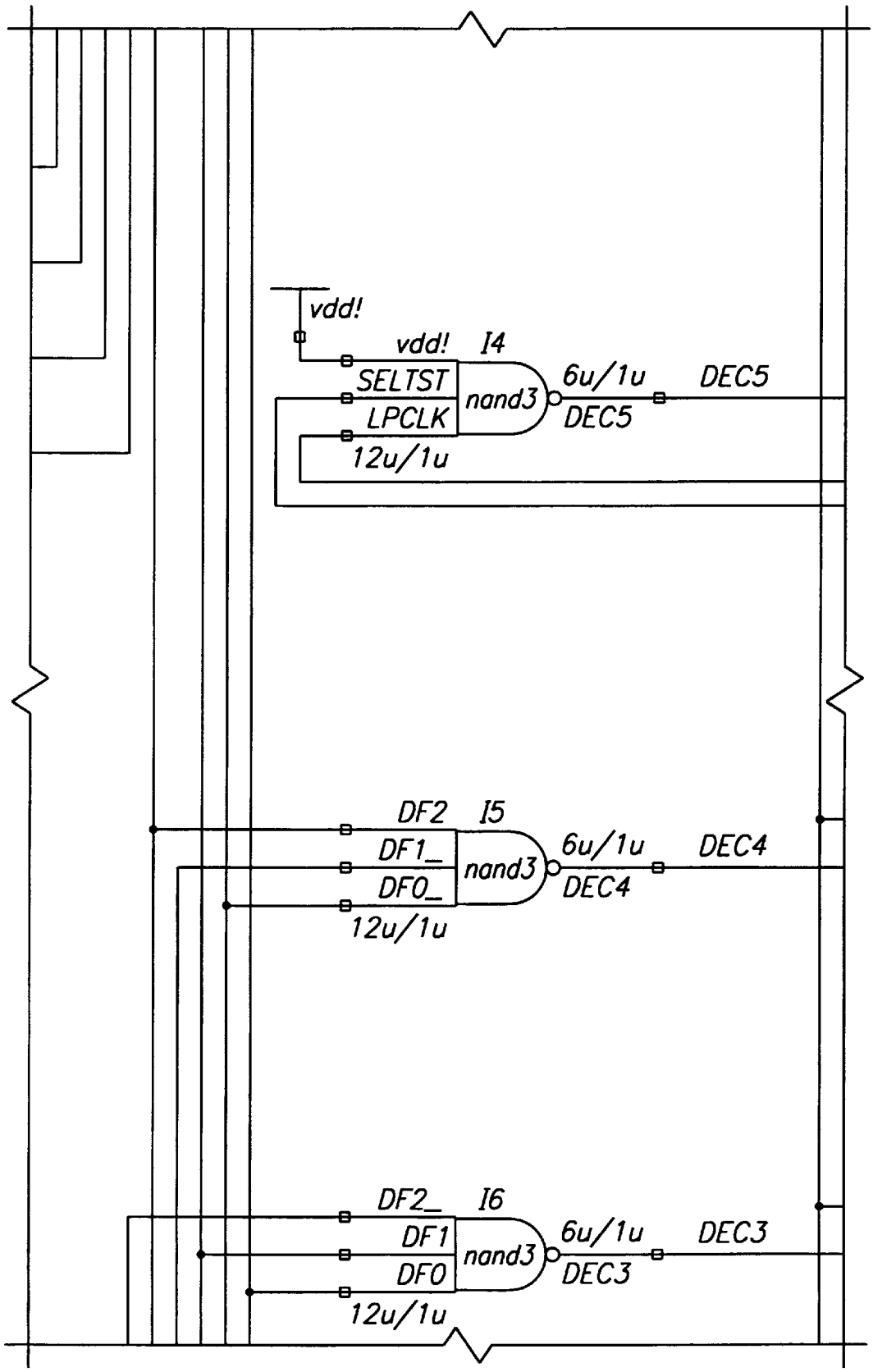

vdd!
vdd!
I4
SELTST
LPCLK
12u/1u
nand3
6u/1u
DEC5
DEC5
DF2
I5
DF1_
DF0_
12u/1u
nand3
6u/1u
DEC4
DEC4
DF2_
I6
DF1
DF0
12u/1u
nand3
6u/1u
DEC3
DEC3

Fig 9.0888

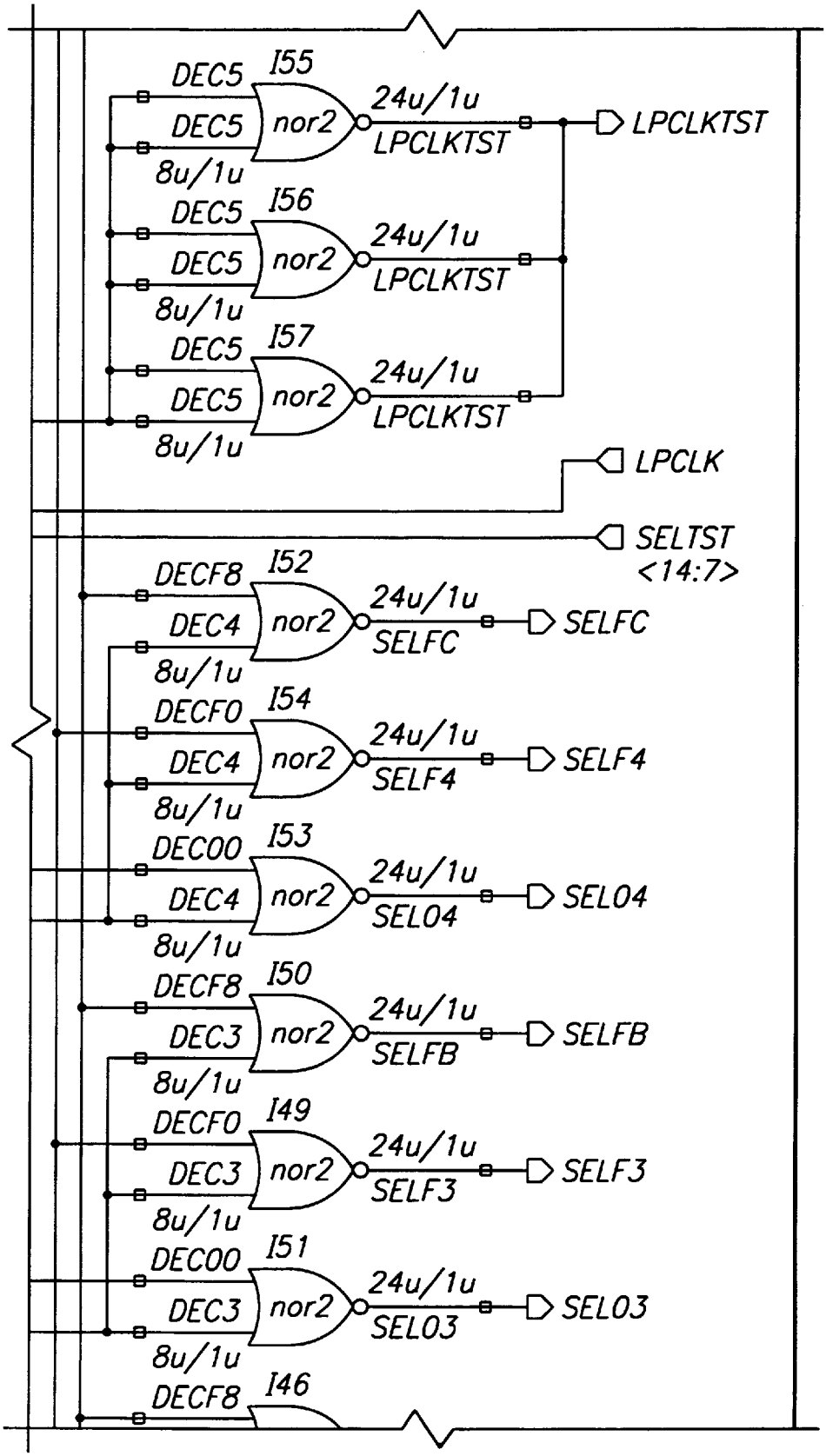

DEC5
I55
DEC5
nor2
24u/1u
LPCLKTST
LPCLKTST
8u/1u
DEC5
I56
DEC5
nor2
24u/1u
LPCLKTST
LPCLKTST
8u/1u
DEC5
I57
DEC5
nor2
24u/1u
LPCLKTST
LPCLKTST
8u/1u
LPCLK
SELTST
<14:7>
DECF8
I52
DEC4
nor2
24u/1u
SELFC
SELFC
8u/1u
DECF0
I54
DEC4
nor2
24u/1u
SELF4
SELF4
8u/1u
DEC00
I53
DEC4
nor2
24u/1u
SEL04
SEL04
8u/1u
DECF8
I50
DEC3
nor2
24u/1u
SELFB
SELFB
8u/1u
DECF0
I49
DEC3
nor2
24u/1u
SELF3
SELF3
8u/1u
DEC00
I51
DEC3
nor2
24u/1u
SEL03
SEL03
8u/1u
DECF8
I46

Fig 9.0888C

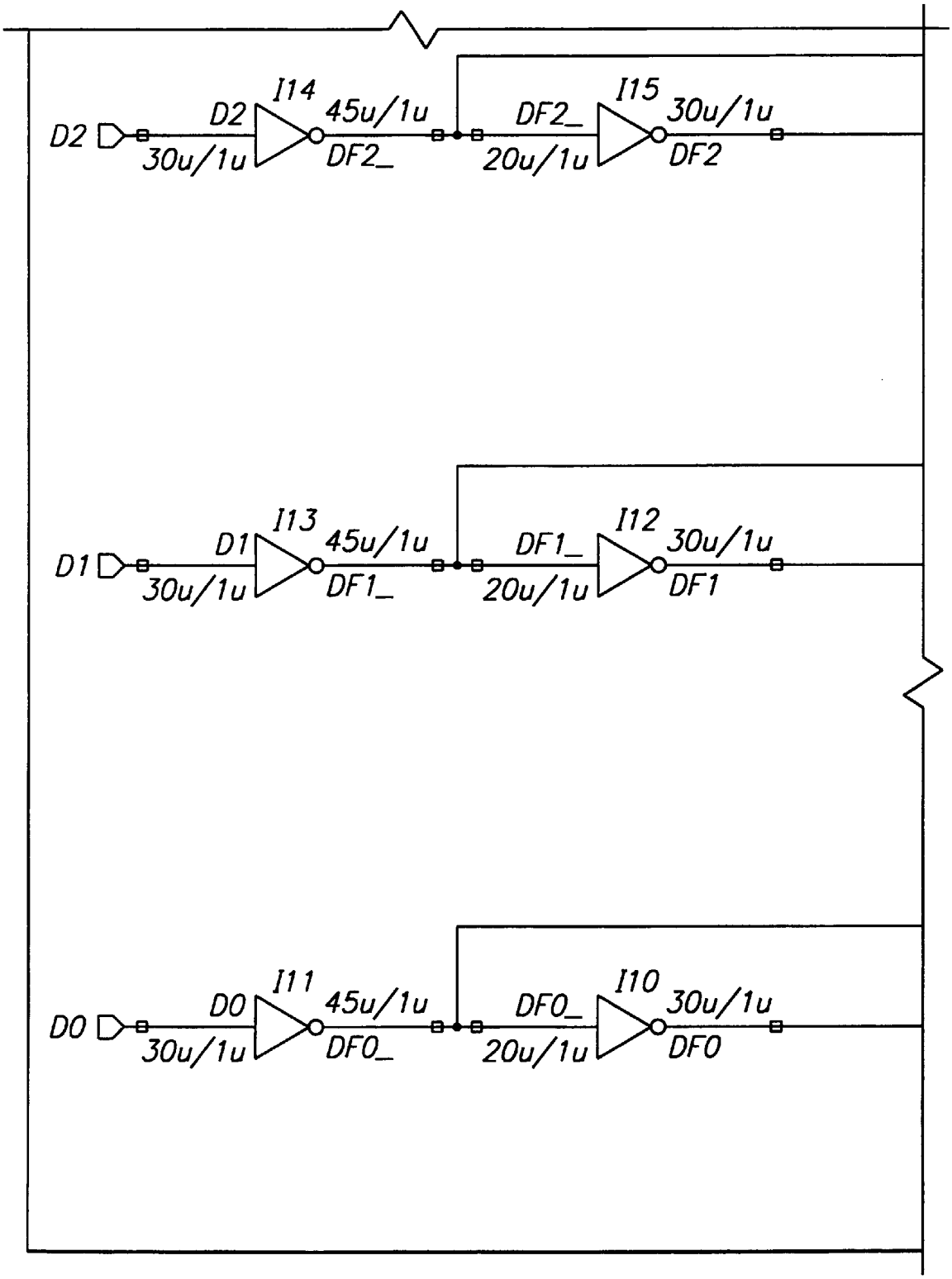

D2
30u/1u
D2
I14
45u/1u
DF2_
DF2_
20u/1u
I15
30u/1u
DF2
D1
30u/1u
D1
I13
45u/1u
DF1_
DF1_
20u/1u
I12
30u/1u
DF1
D0
30u/1u
D0
I11
45u/1u
DF0_
DF0_
20u/1u
I10
30u/1u
DF0

Fig 9.08CA

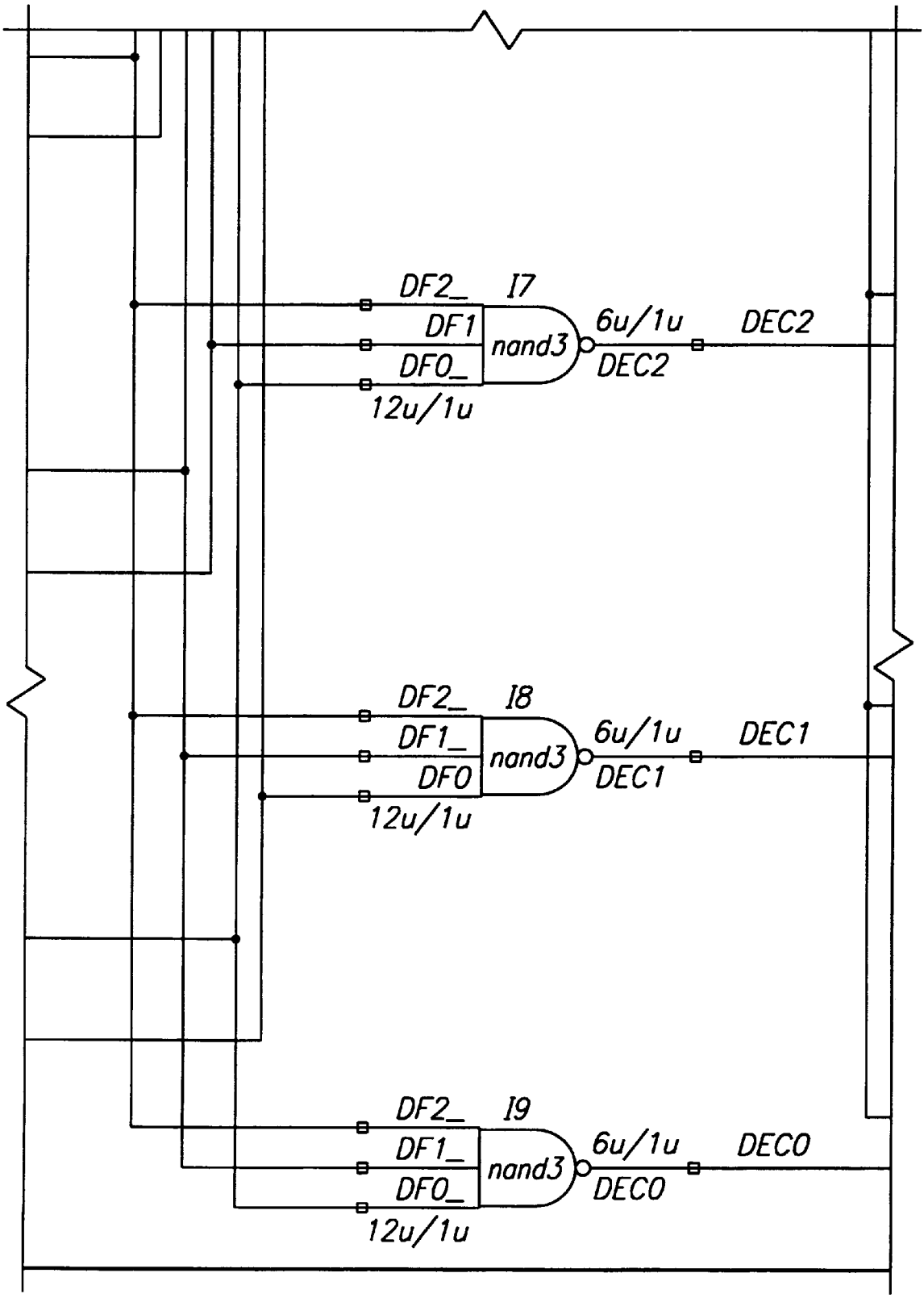


Fig 90.0088CIB

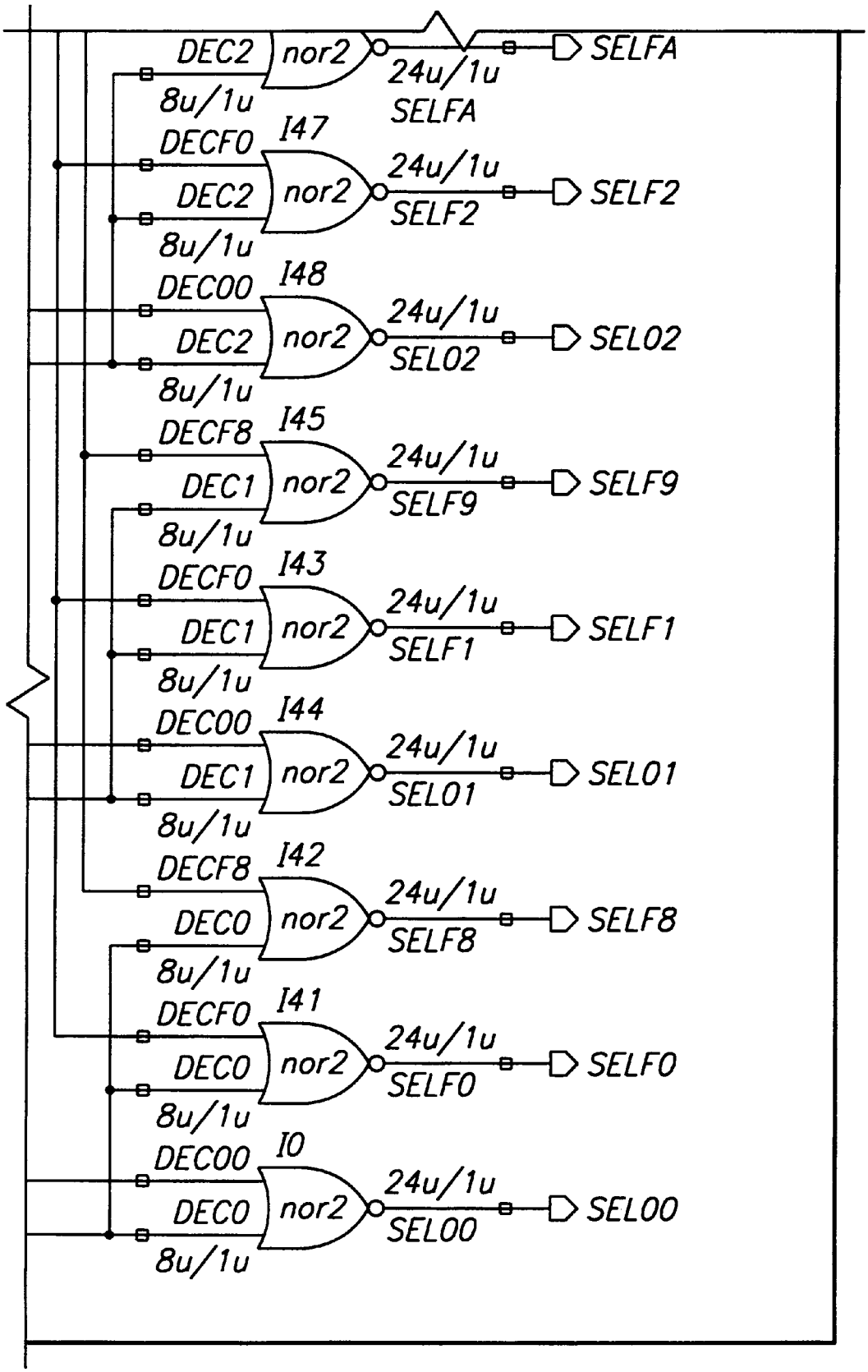

DEC2
nor2
24u/1u
SELFA
8u/1u
SELFA
I47
DECF0
DEC2
nor2
24u/1u
SELF2
8u/1u
SELF2
I48
DEC00
DEC2
nor2
24u/1u
SEL02
8u/1u
SEL02
I45
DECF8
DEC1
nor2
24u/1u
SELF9
8u/1u
SELF9
I43
DECF0
DEC1
nor2
24u/1u
SELF1
8u/1u
SELF1
I44
DEC00
DEC1
nor2
24u/1u
SEL01
8u/1u
SEL01
I42
DECF8
DEC0
nor2
24u/1u
SELF8
8u/1u
SELF8
I41
DECF0
DEC0
nor2
24u/1u
SELF0
8u/1u
SELF0
I0
DEC00
DEC0
nor2
24u/1u
SEL00
8u/1u
SEL00

Fig. 9.00BCC

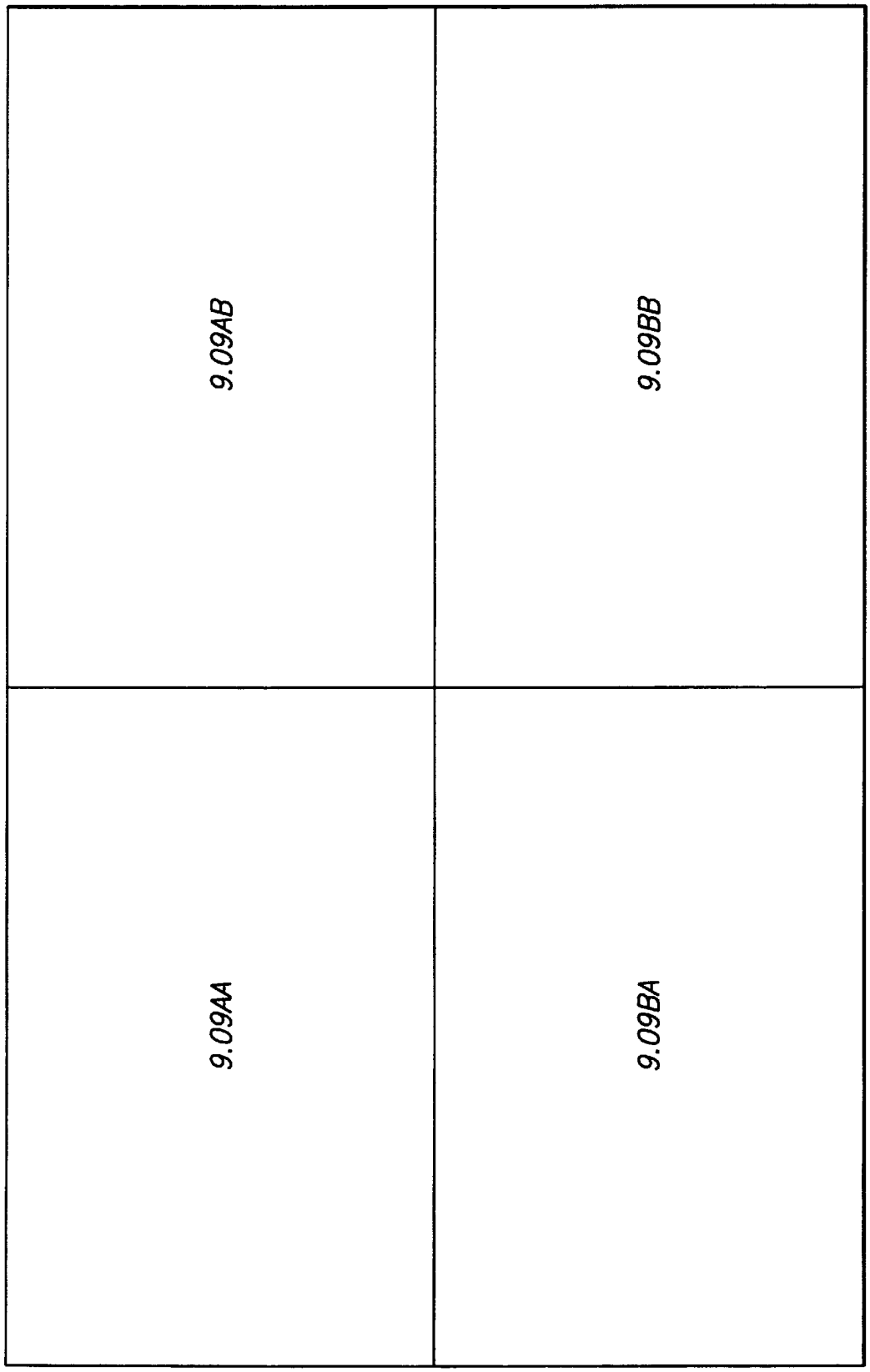


FIG. 9.09 (sheet)

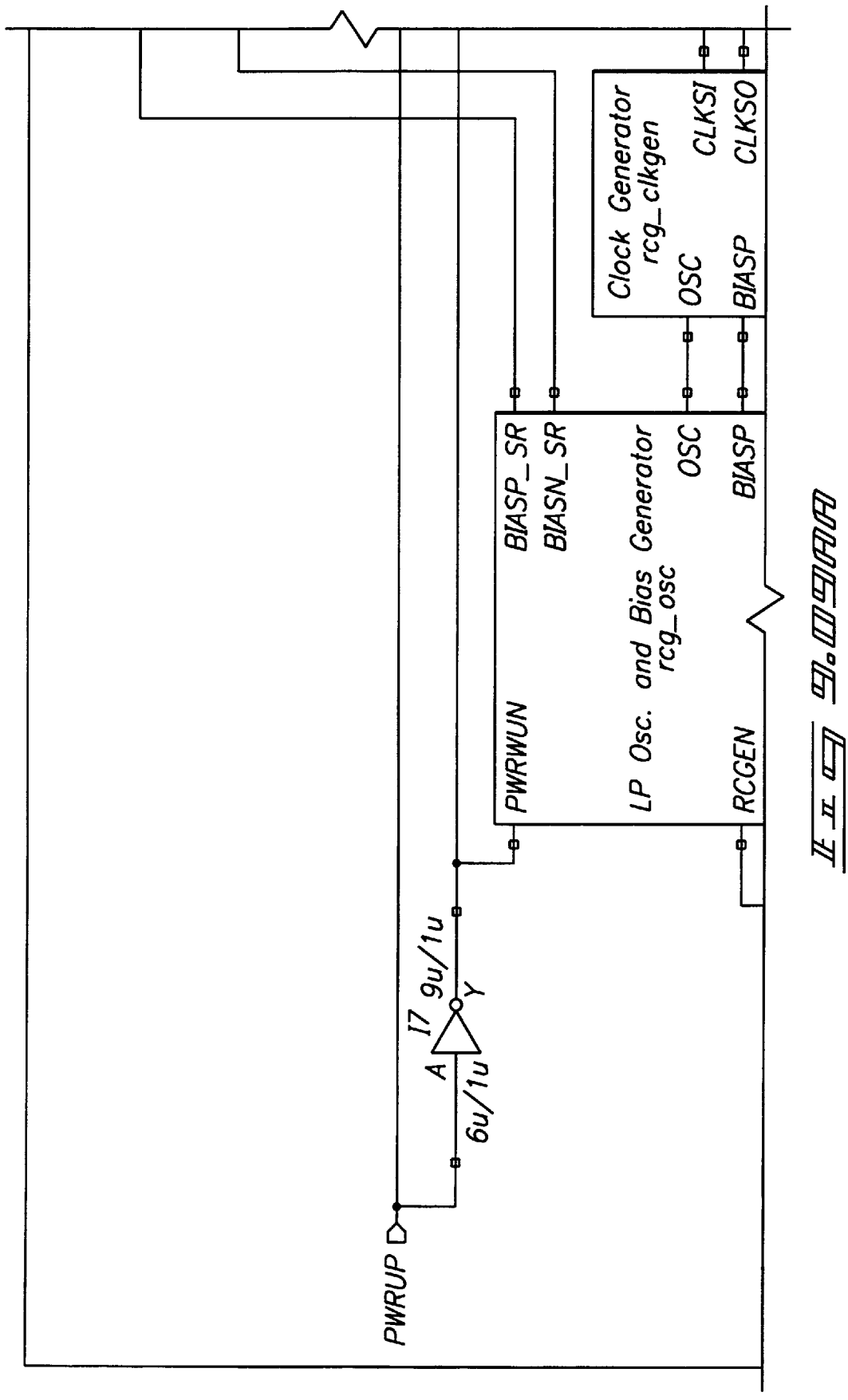

Clock Generator
rcg_clkgen
OSC
BIASP
CLKSI
CLKSO
LP Osc. and Bias Generator
rcg_osc
BIASP_SR
BIASN_SR
PWRWUN
RCGEN
OSC
BIASP
I7
9u/1u
6u/1u
A
Y
PWRUP

FIG. 9.0594A

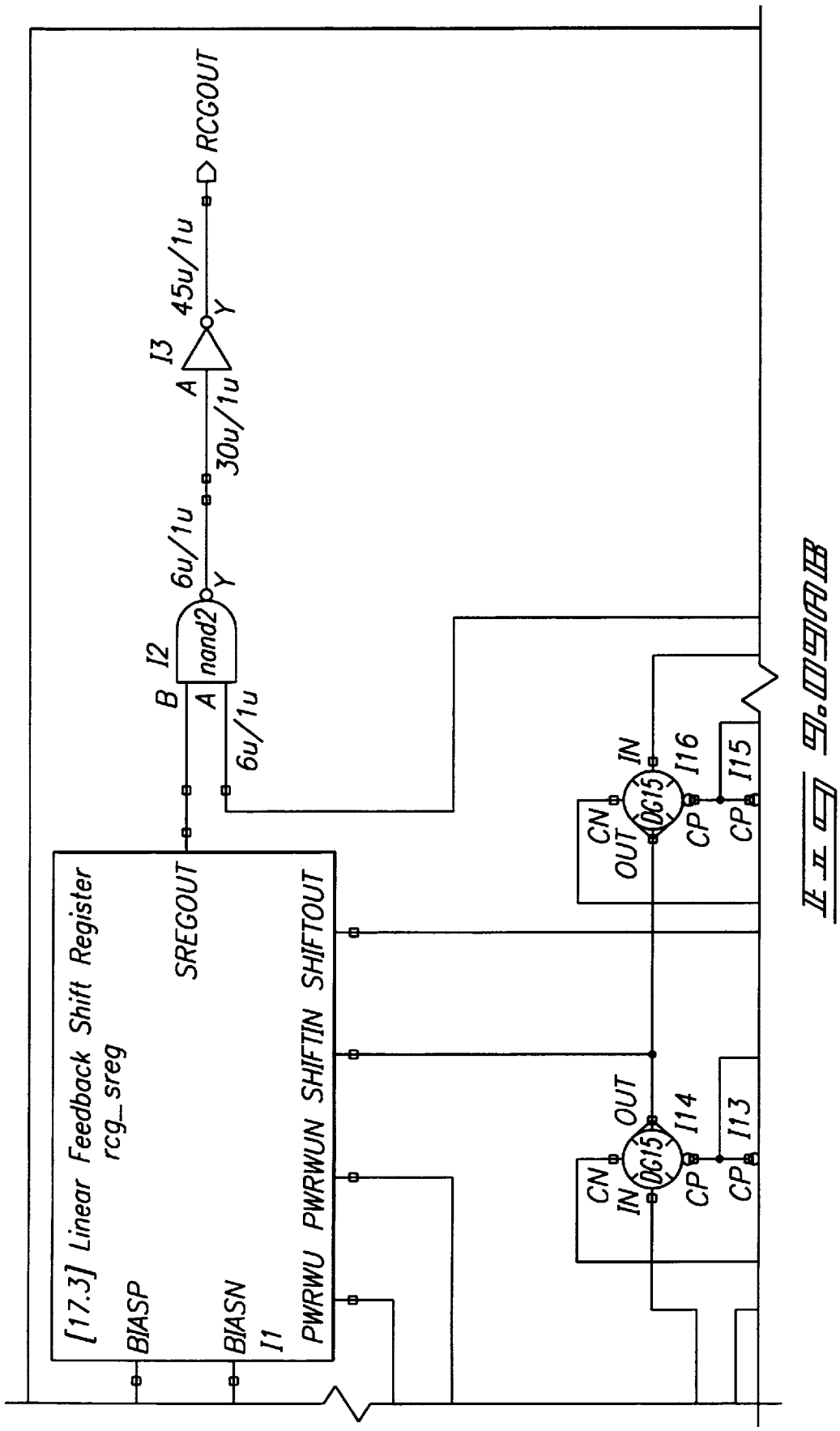

[17.3] Linear Feedback Shift Register
rcg_sreg
BIASP
BIASN
I1
SREGOUT
PWRWU
PWRWUN
SHIFTIN
SHIFTOUT
I2
nand2
B
A
Y
6u/1u
6u/1u
30u/1u
I3
45u/1u
A
Y
RCGOUT
I16
I15
I14
I13
DG15
CN
IN
OUT
CP

FIG 91.0594B

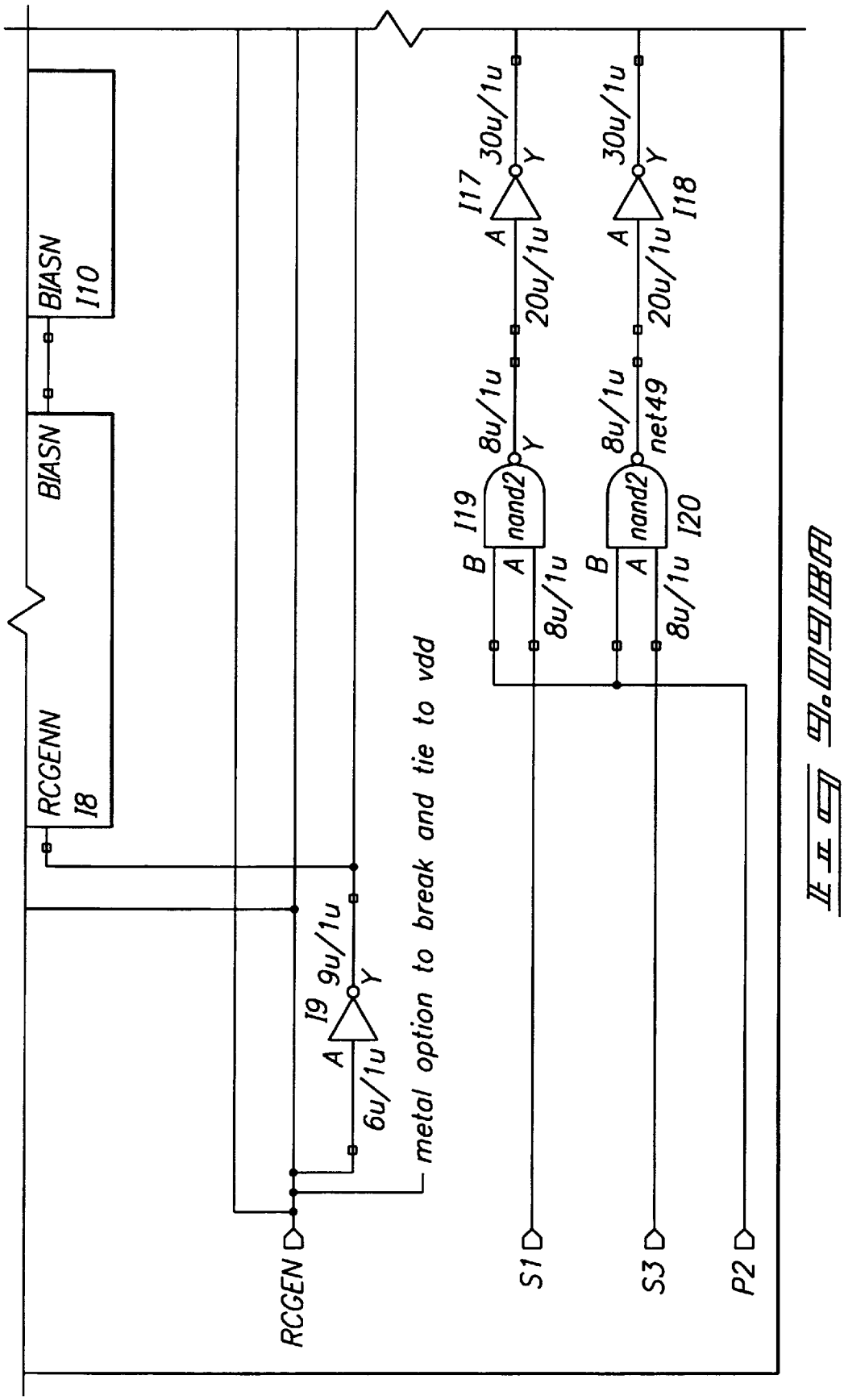

BIASN
I10
BIASN
RCGENN
I8
I19
9u/1u
A
Y
6u/1u
metal option to break and tie to vdd
RCGEN
I17
30u/1u
A
Y
20u/1u
8u/1u
Y
I119
B
nand2
A
8u/1u
I18
30u/1u
A
Y
20u/1u
8u/1u
net49
I120
B
nand2
A
8u/1u
S1
S3
P2

FIG. 6,130,602

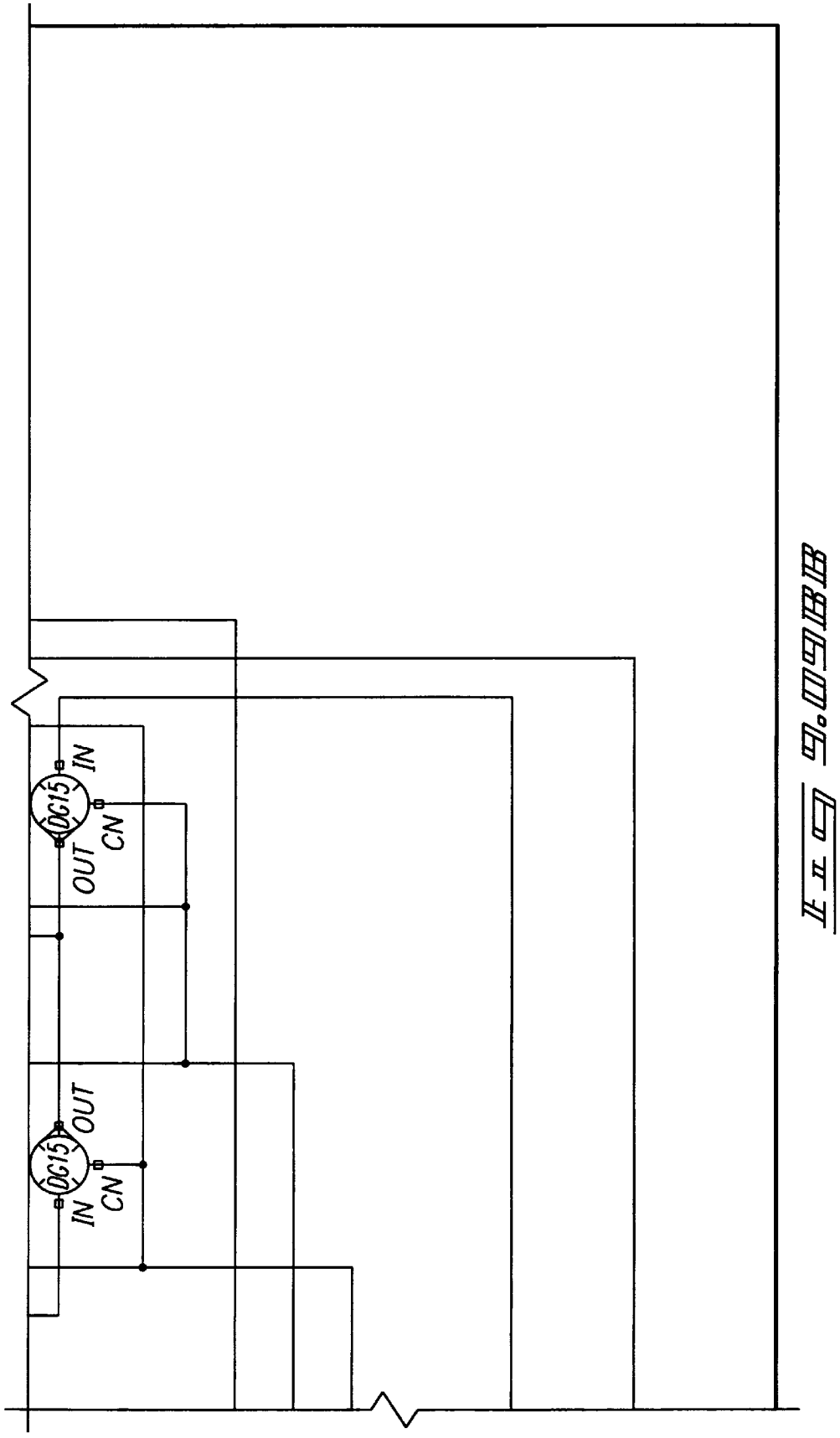


FIG 9,009,188

9.0901AA	9.0901AB	9.0901AC	9.0901AD	9.0901AE	9.0901AF	9.0901AG	9.0901AH
9.0901BA	9.0901BB	9.0901BC	9.0901BD	9.0901BE	9.0901BF	9.0901BG	9.0901BH
9.0901CA	9.0901CB	9.0901CC	9.0901CD	9.0901CE	9.0901CF	9.0901CG	9.0901CH

FIG. 9.0901

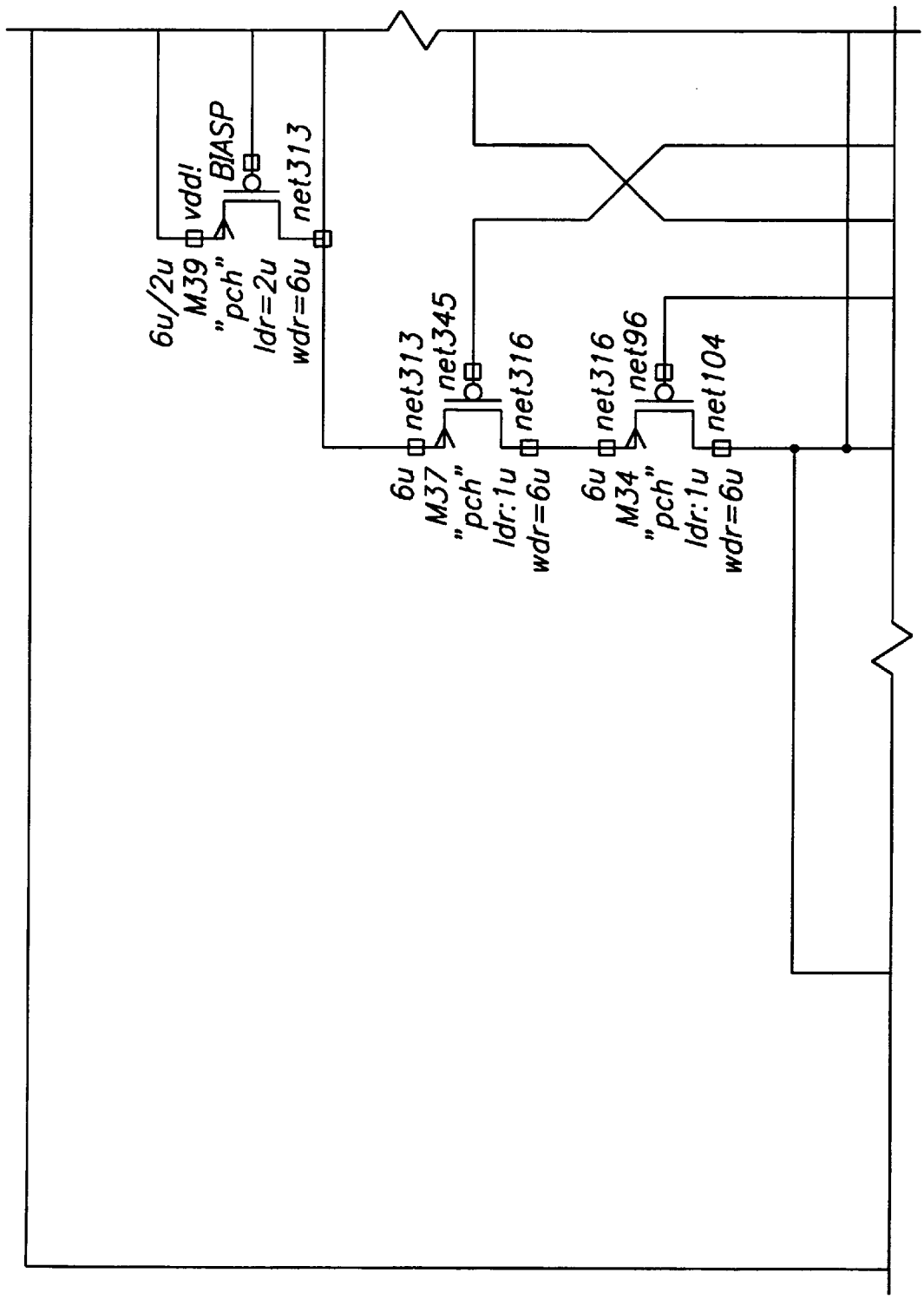

6u/2u
M39
"pch"
ldr=2u
wdr=6u
vdd!
BIASP
net313
6u
M37
"pch"
ldr:1u
wdr=6u
net313
net345
net316
6u
M34
"pch"
ldr:1u
wdr=6u
net316
net96
net104

FIG 9,090 IAA

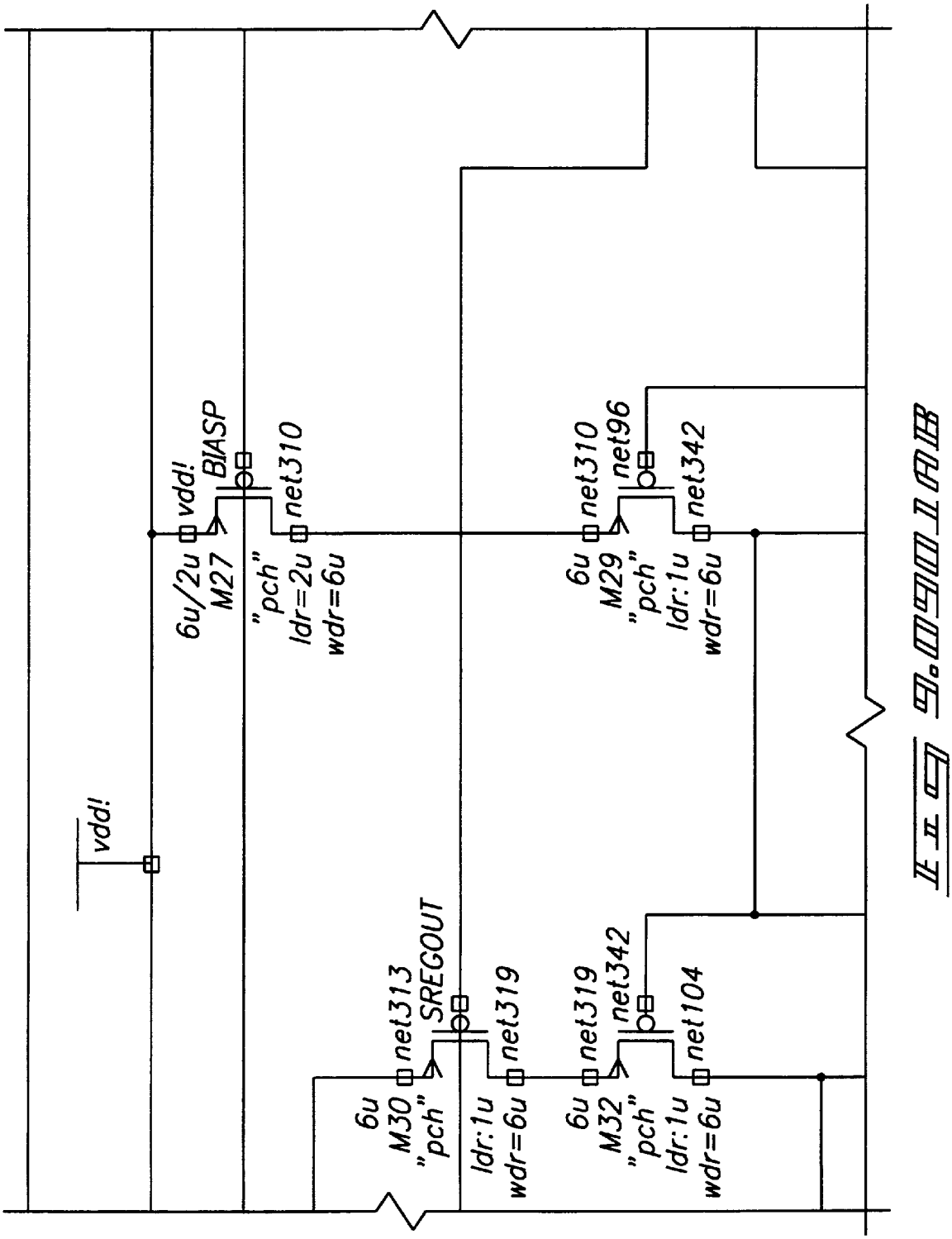

vdd!
6u/2u
M27
"pch"
ldr=2u
wdr=6u
vdd!
BIASP
net310
6u
M29
"pch"
ldr:1u
wdr=6u
net310
net96
net342
6u
M30
"pch"
ldr:1u
wdr=6u
net313
SREGOUT
net319
6u
M32
"pch"
ldr:1u
wdr=6u
net319
net342
net104

FIG 9.00511A

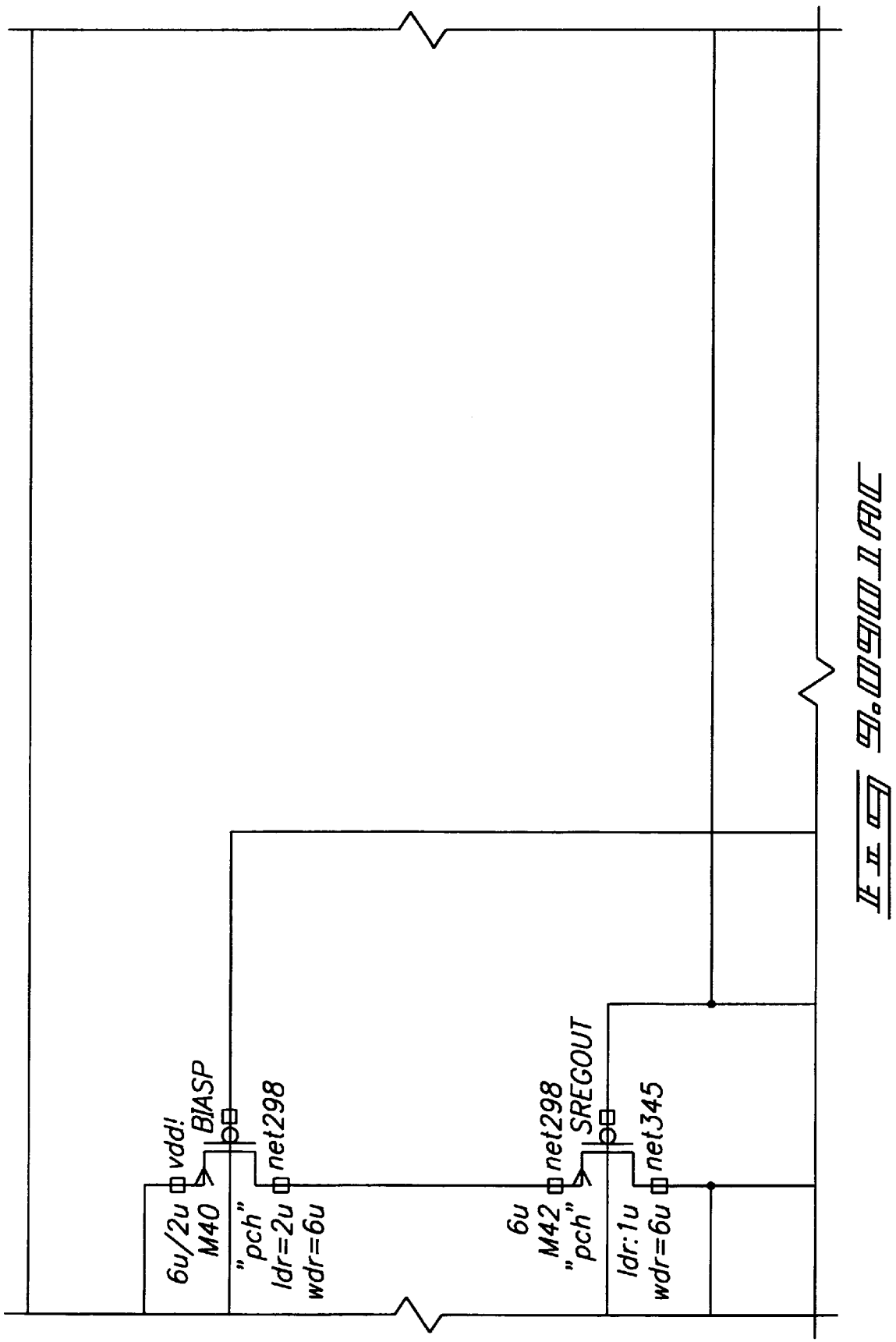


FIG. 9,060
vdd!
BIASP
net298
SREGOUT
net345
6u/2u
M40
"pch"
ldr=2u
wdr=6u
6u
M42
"pch"
ldr:1u
wdr=6u

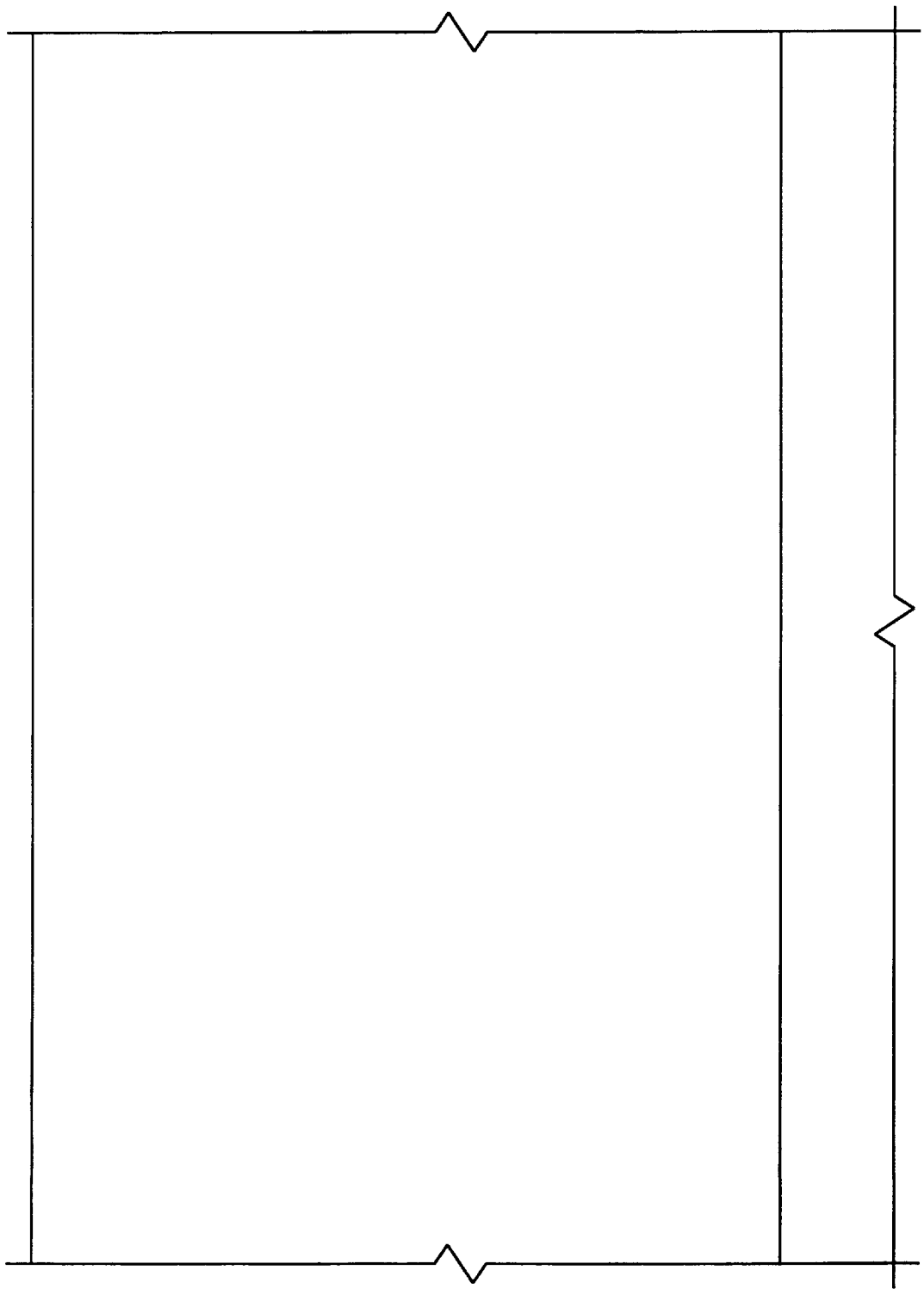


FIG 96,050A1AD

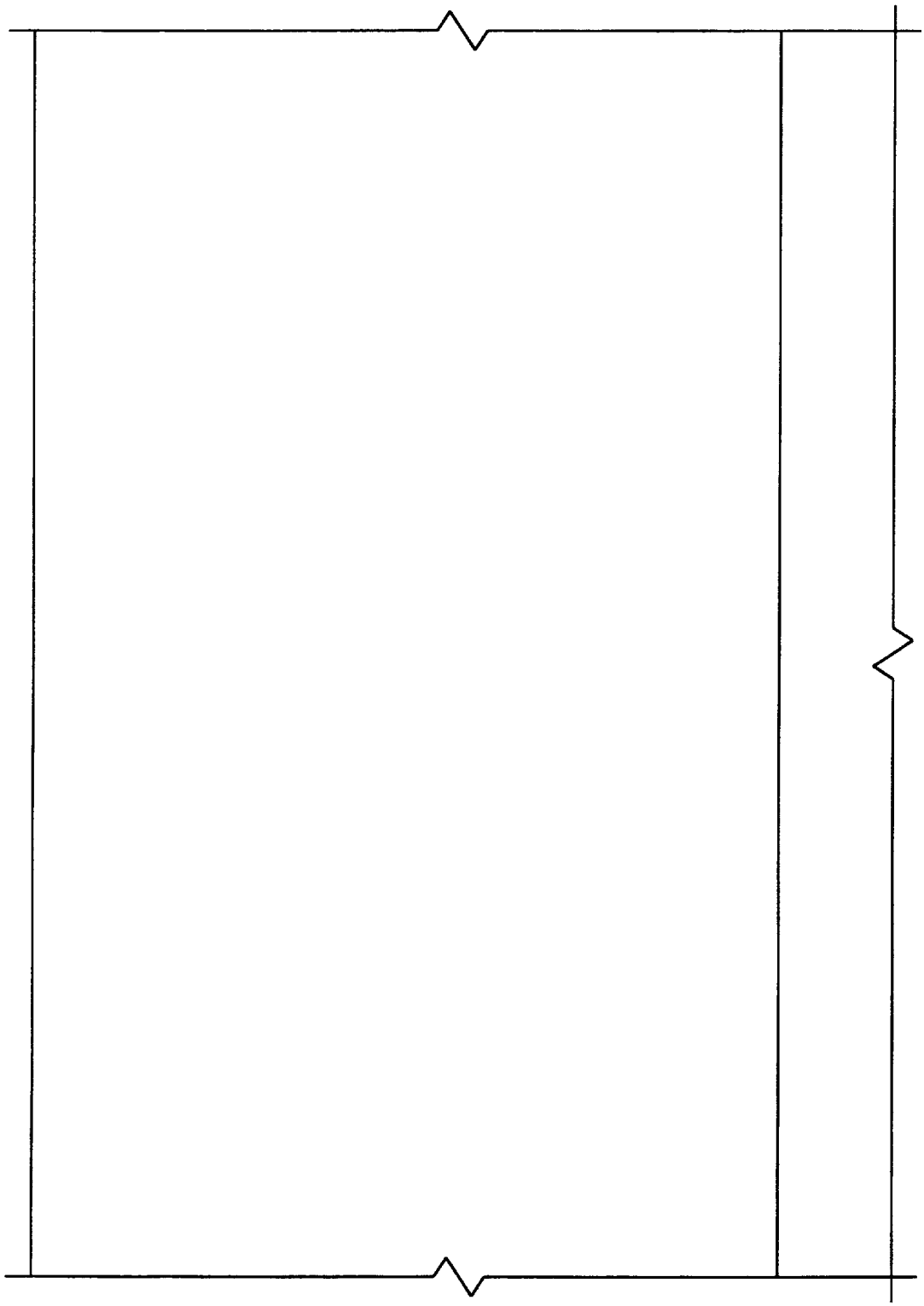


FIG 9,090 PAGE

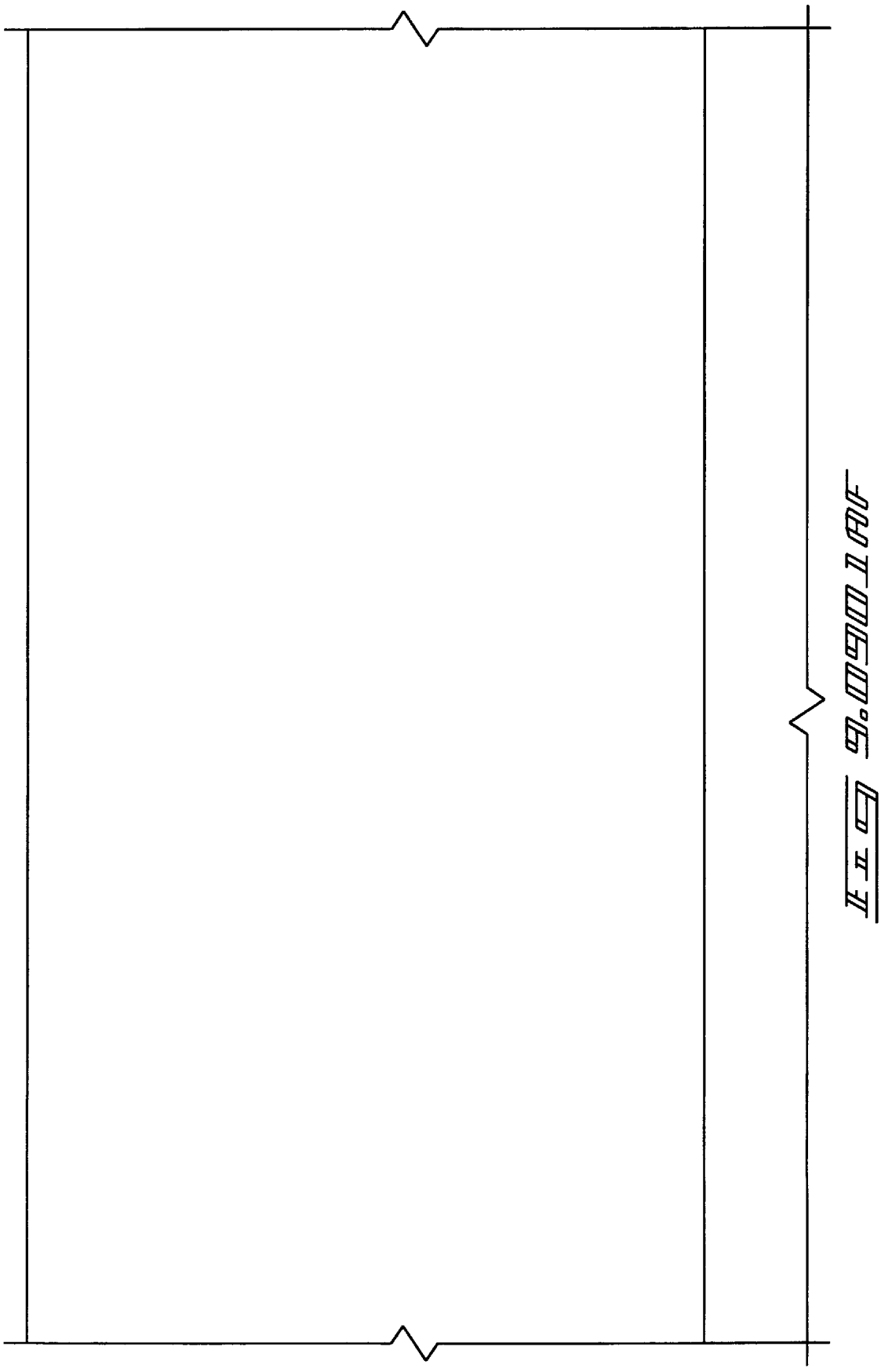


FIG. 96,005

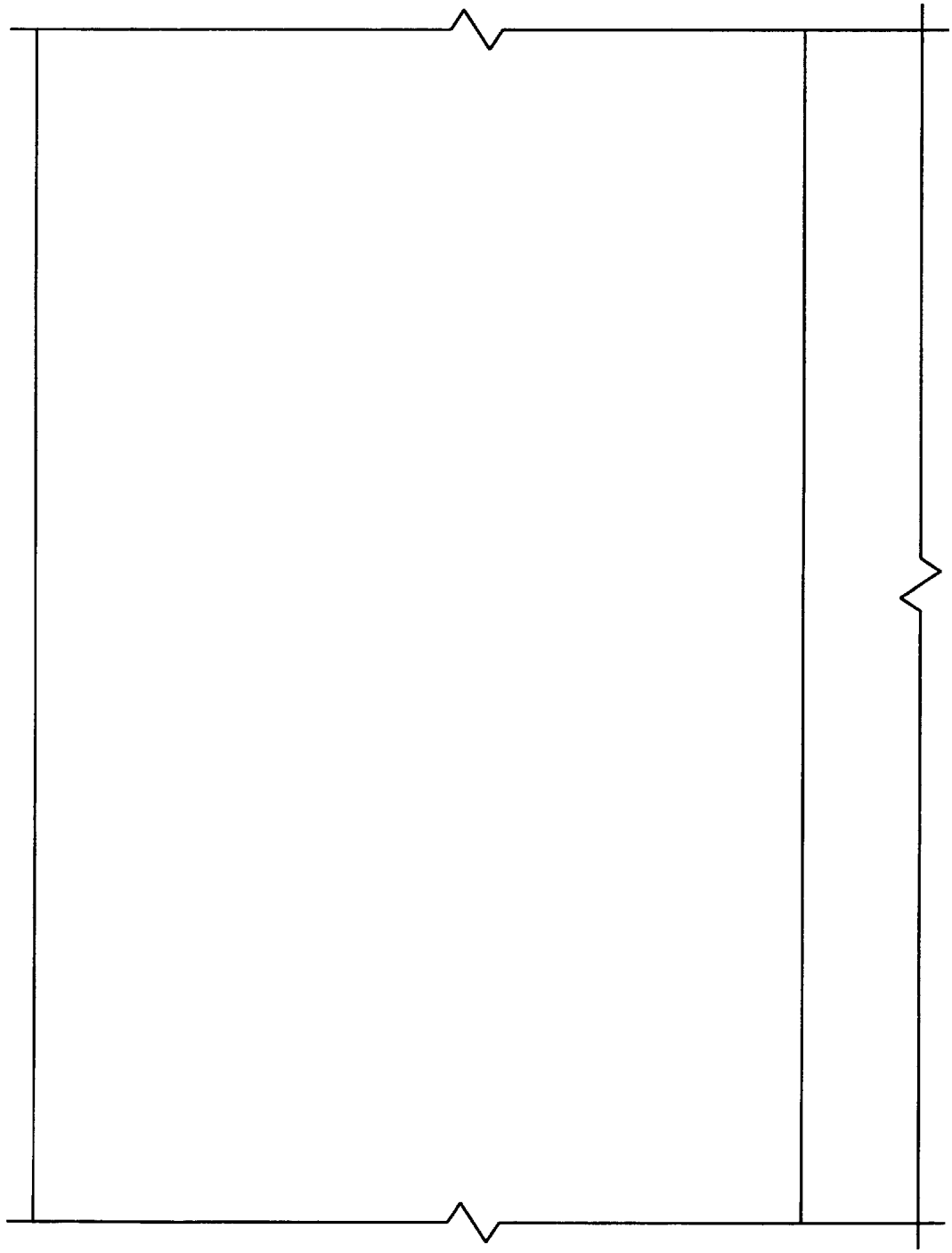


FIG 9,090,116

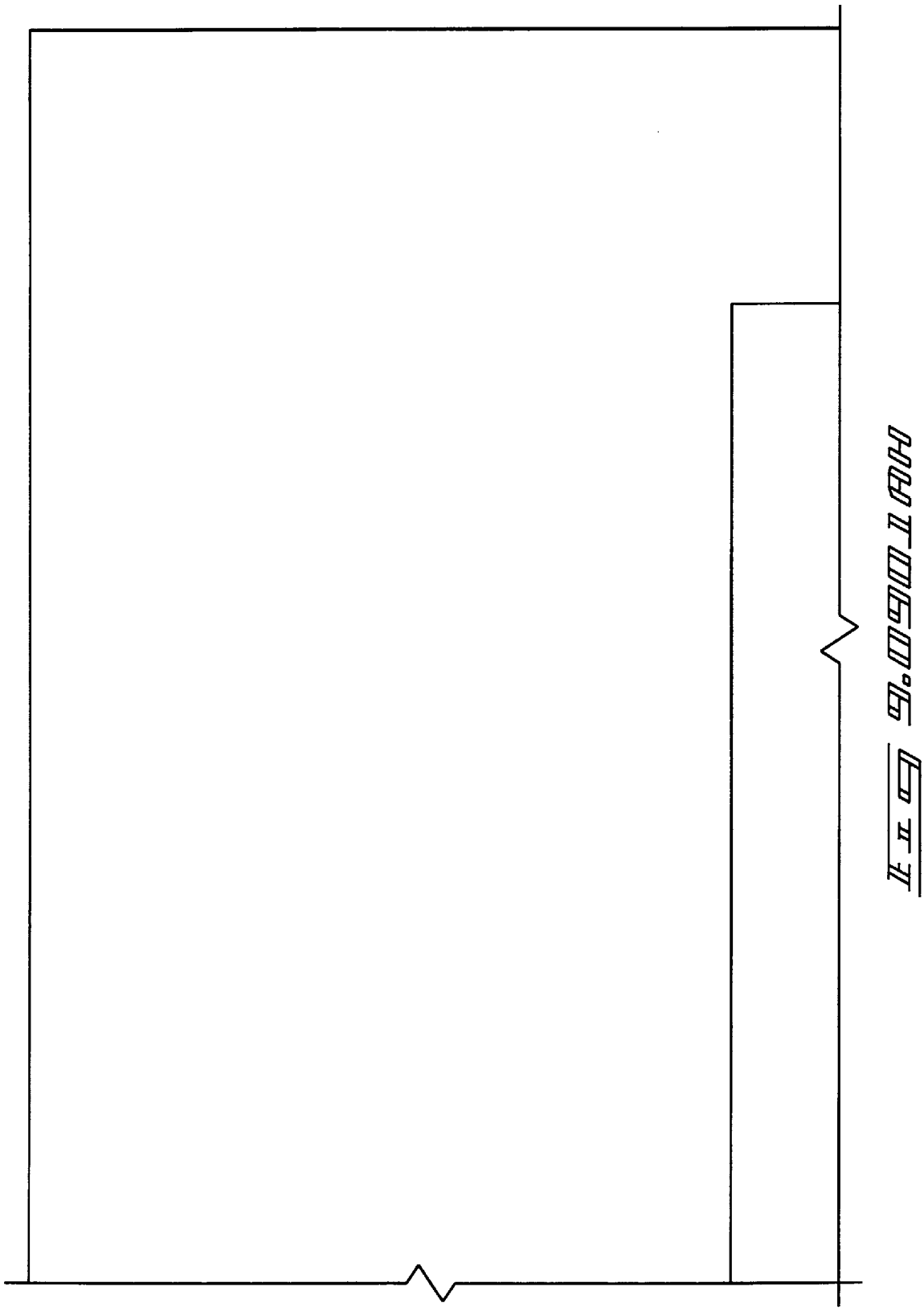


FIG 5,050,15 HAV

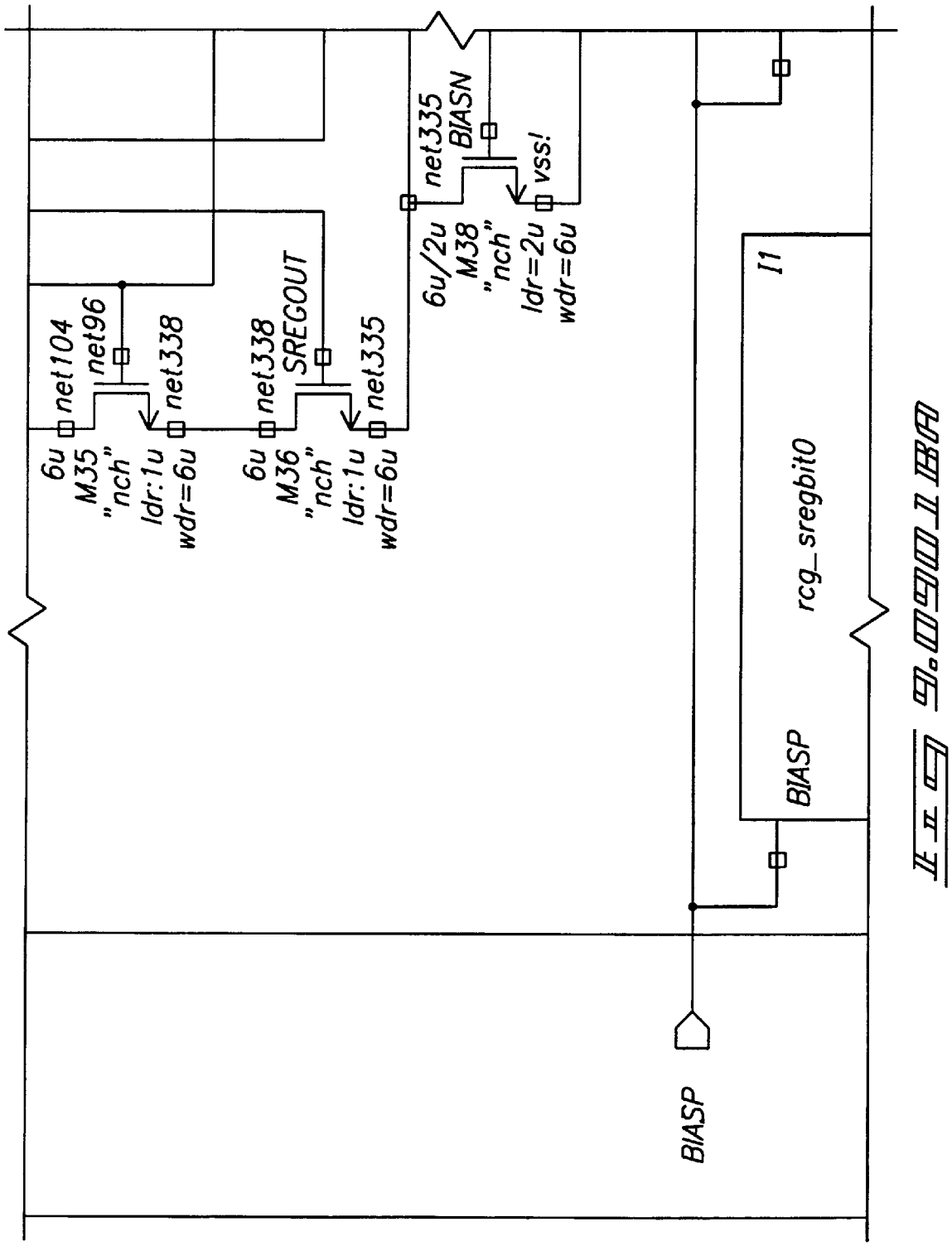

net104
net96
6u
M35
"nch"
ldr:1u
wdr=6u
net338
net338
SREGOUT
6u
M36
"nch"
ldr:1u
wdr=6u
net335
net335
BIASN
6u/2u
M38
"nch"
ldr=2u
wdr=6u
vss!
I1
rcg_sregbit0
BIASP
BIASP

FIG 6,000,118

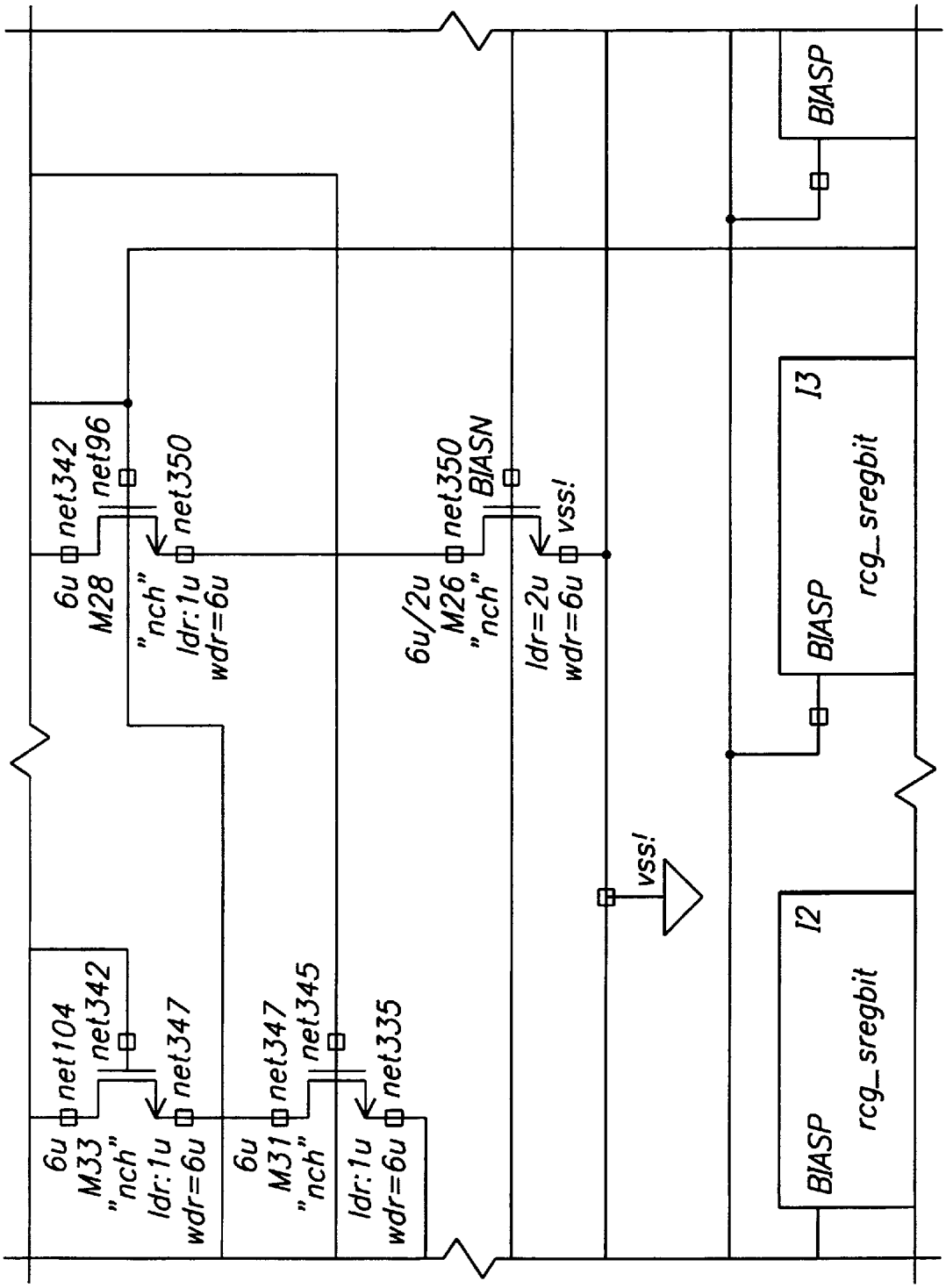
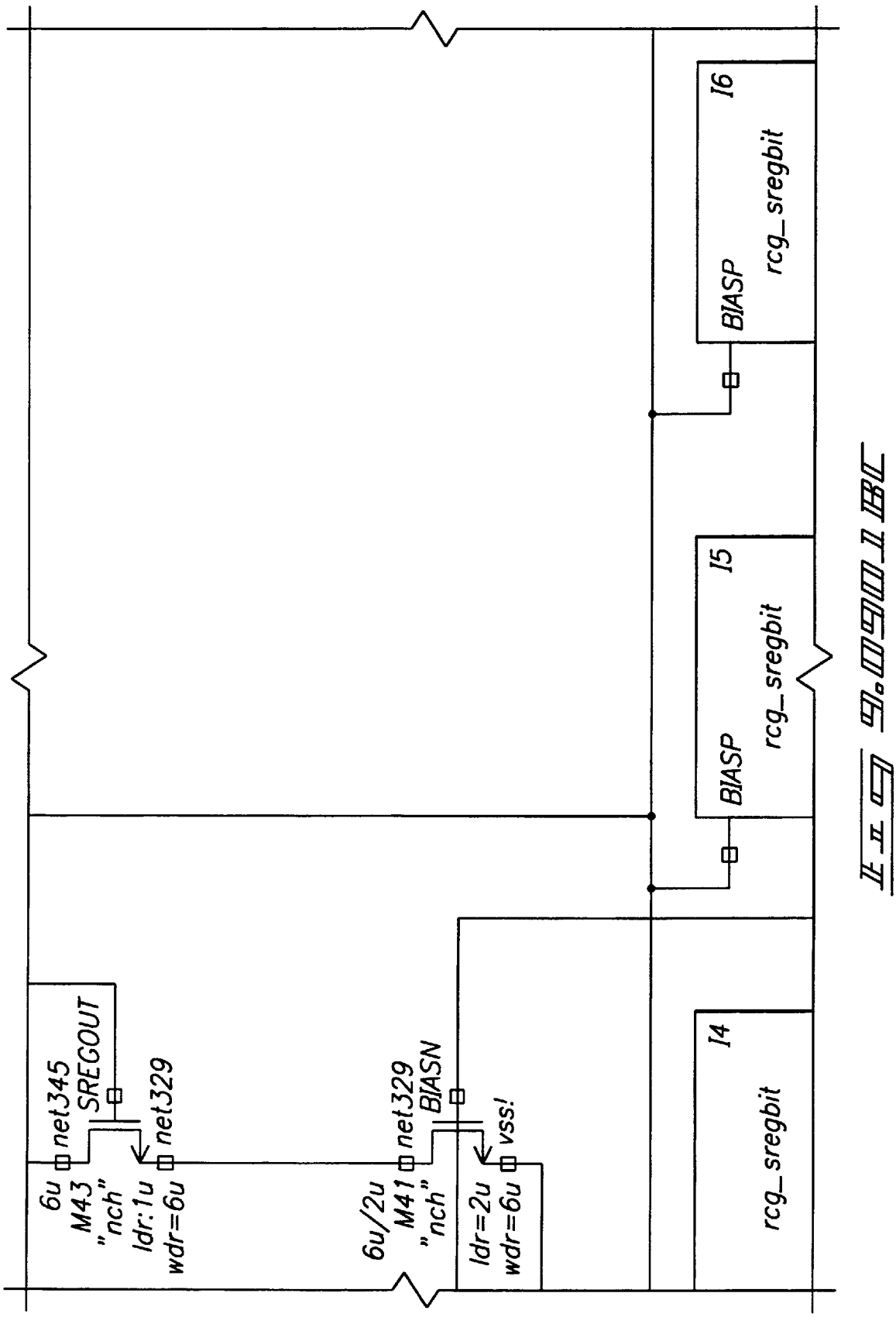


FIG. 9.00900 IIBB


I6
rcg_sregbit
BIASP
I5
rcg_sregbit
BIASP
I4
rcg_sregbit
6u
M43
"nch"
ldr:1u
wdr=6u
net345
SREGOUT
net329
6u/2u
M41
"nch"
ldr=2u
wdr=6u
net329
BIASN
vss!

Фиг 69.00516

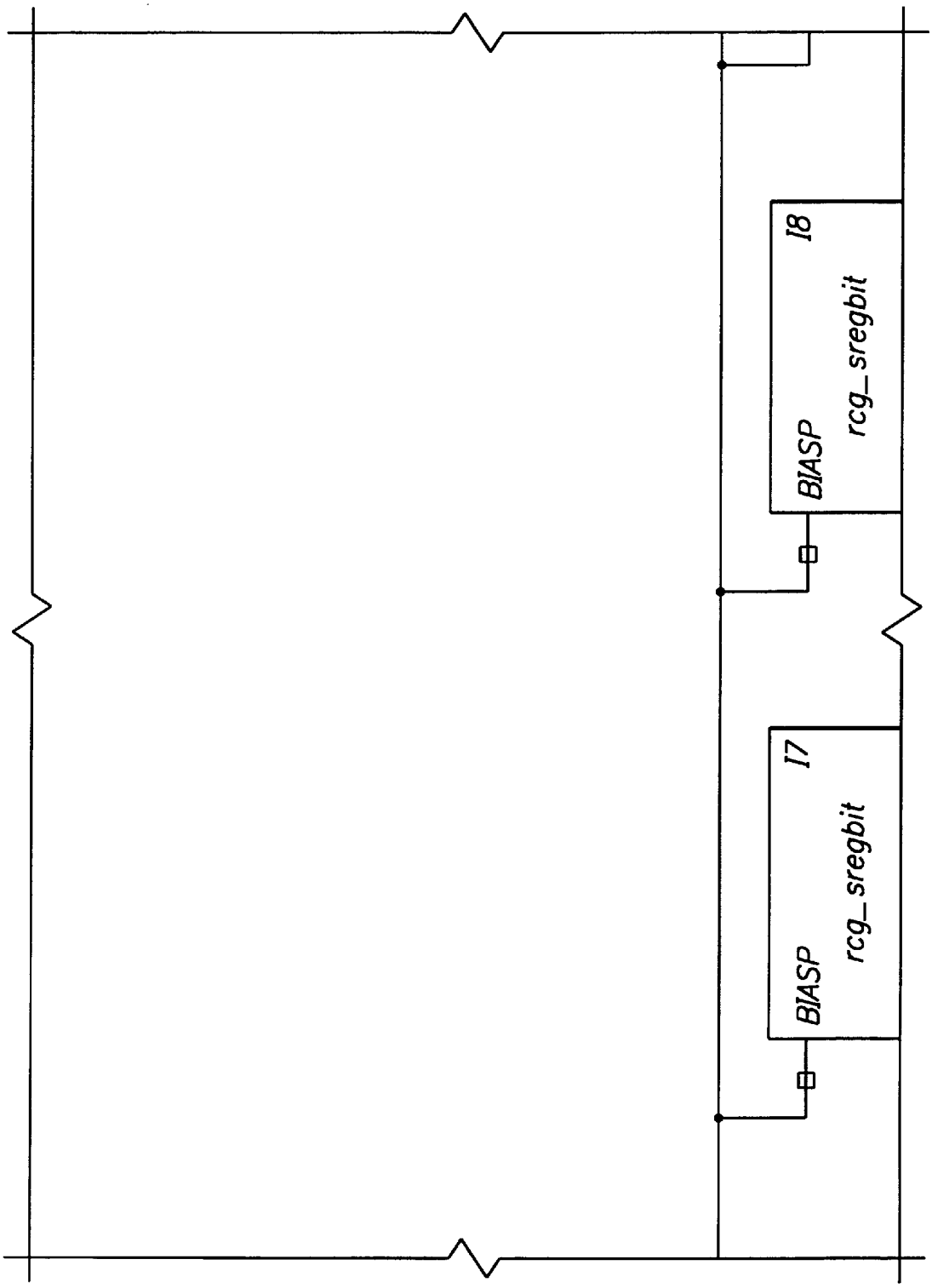


FIG 9,0900 II IBM

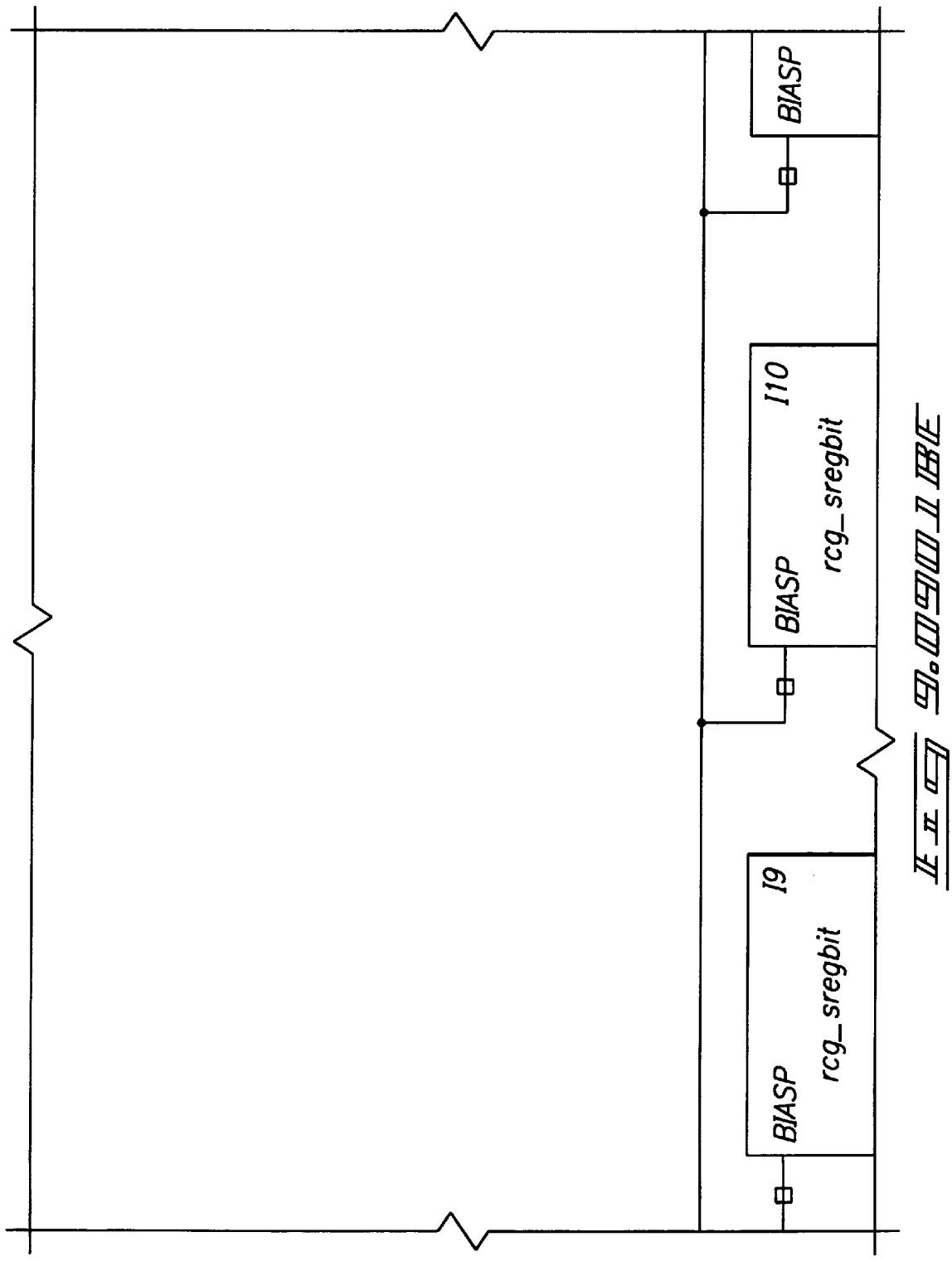


FIG. 69,011

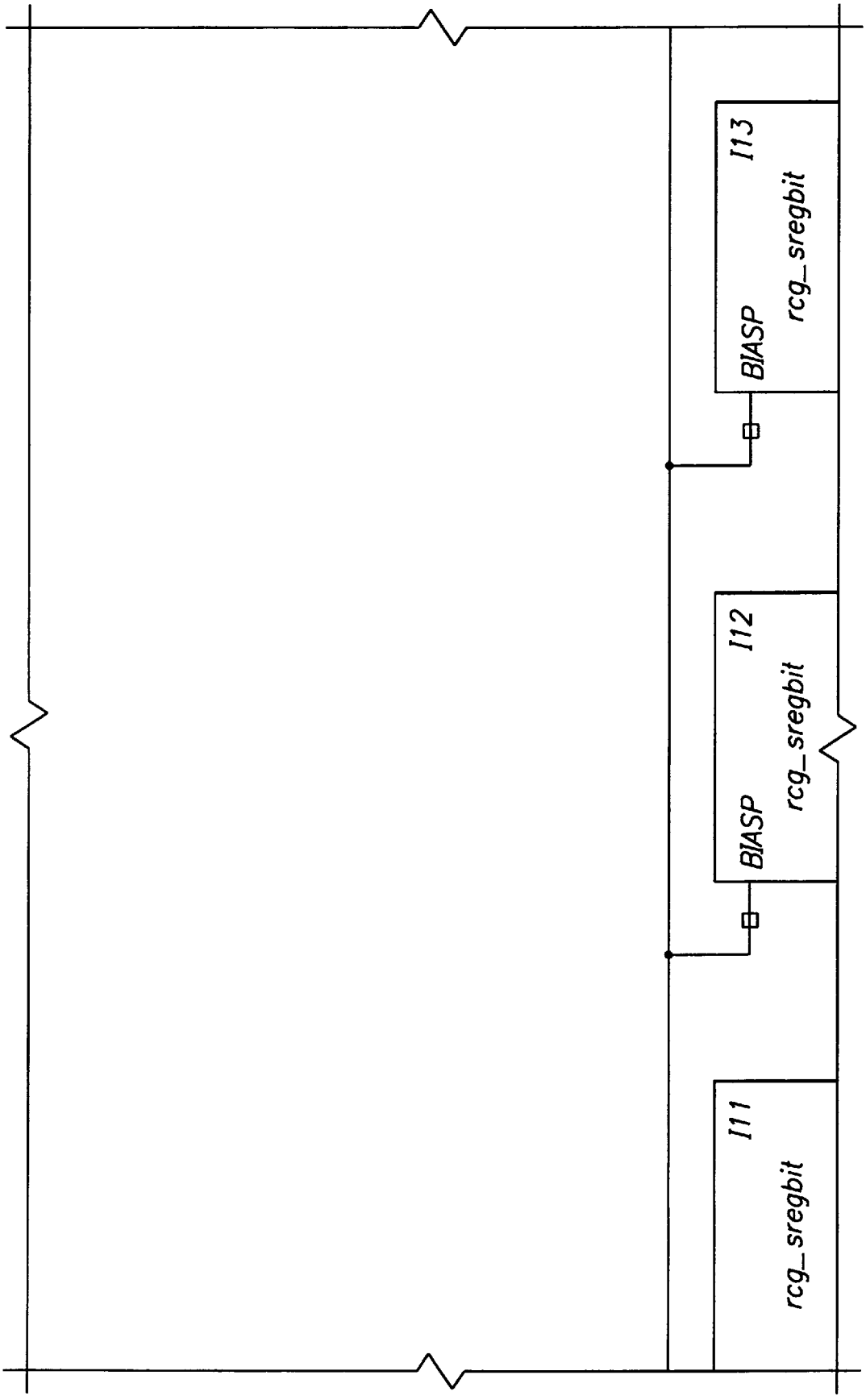


FIG. 2696

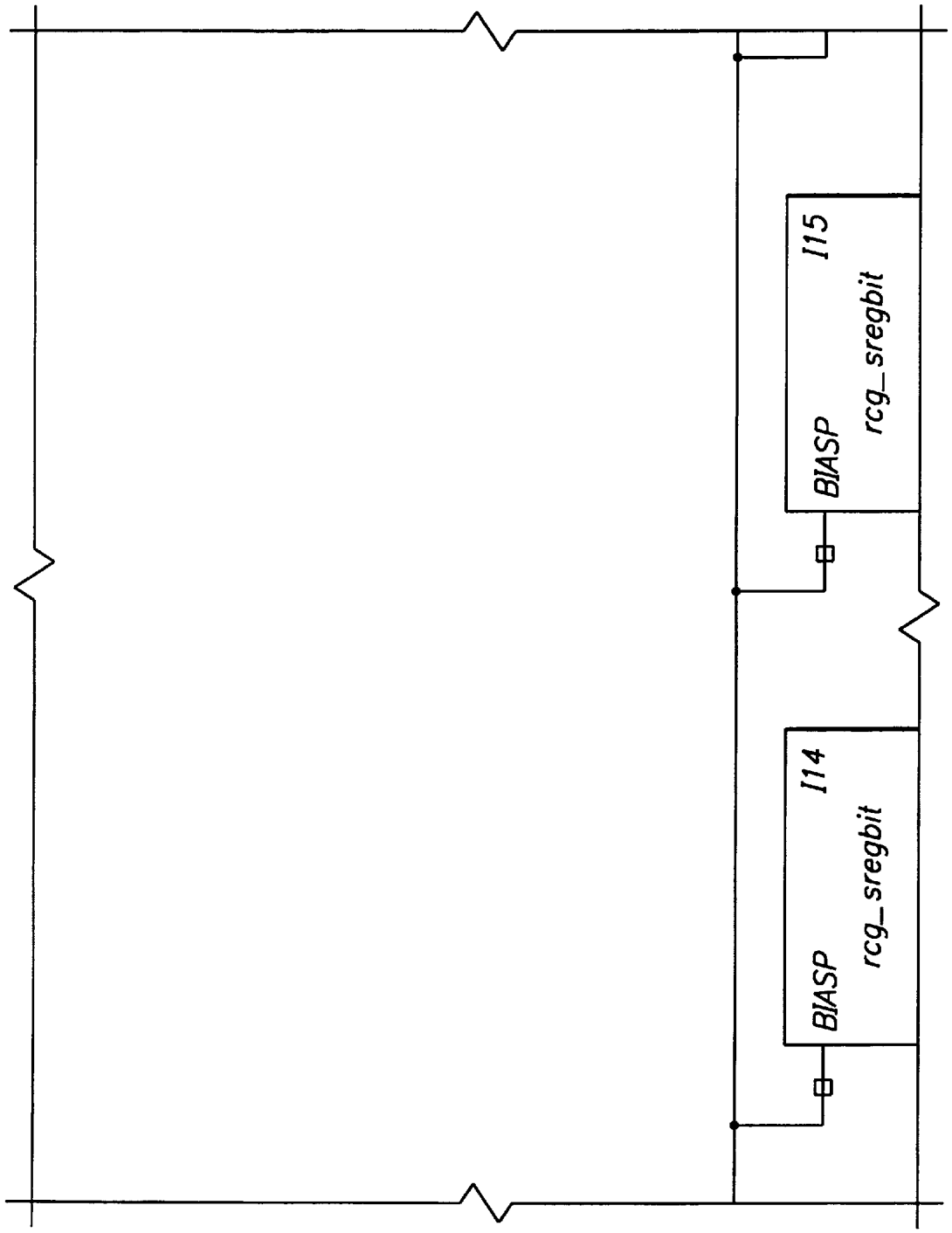


FIG. 9,009,11 BIG

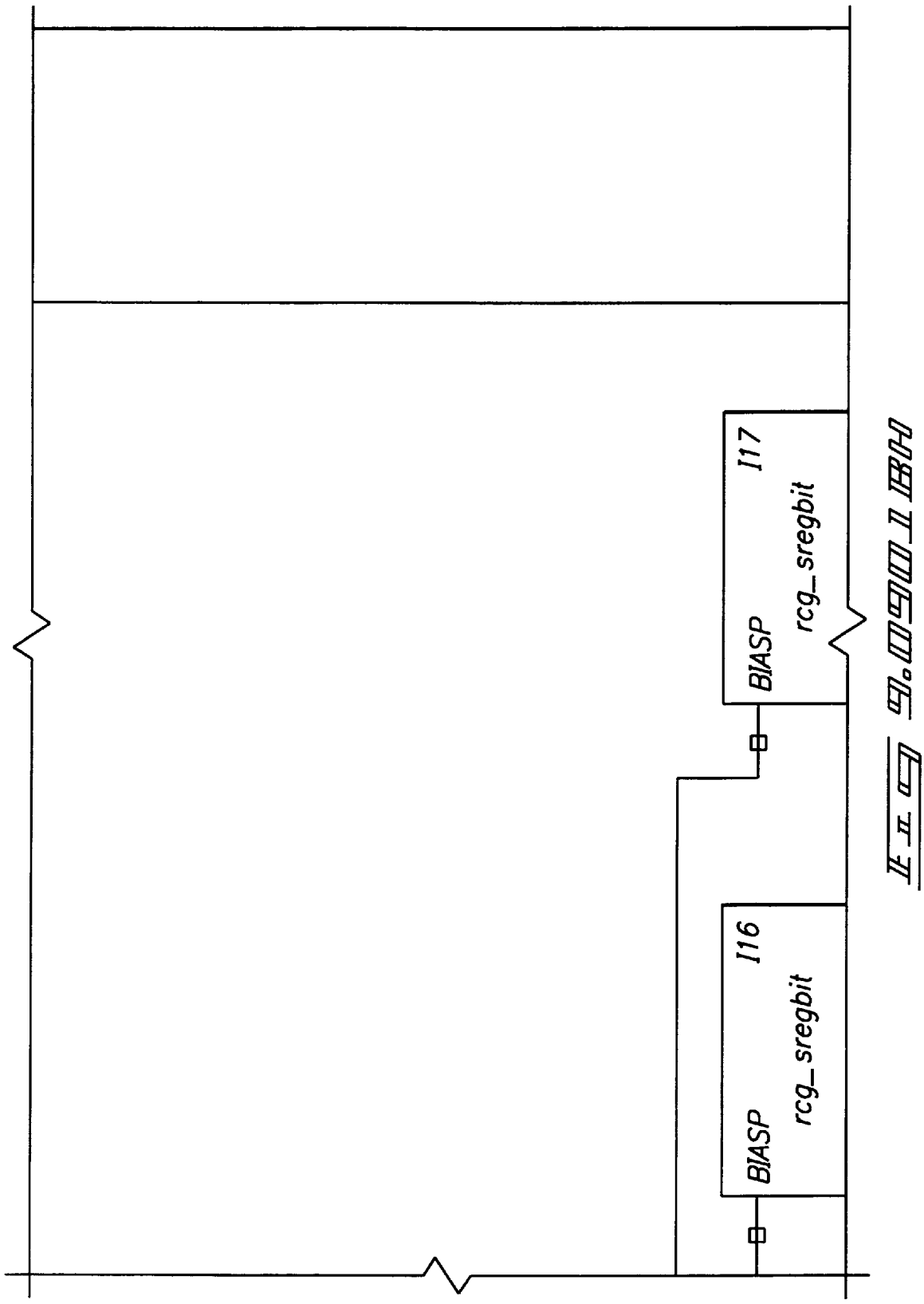


FIG 91,009 (PRIOR ART)

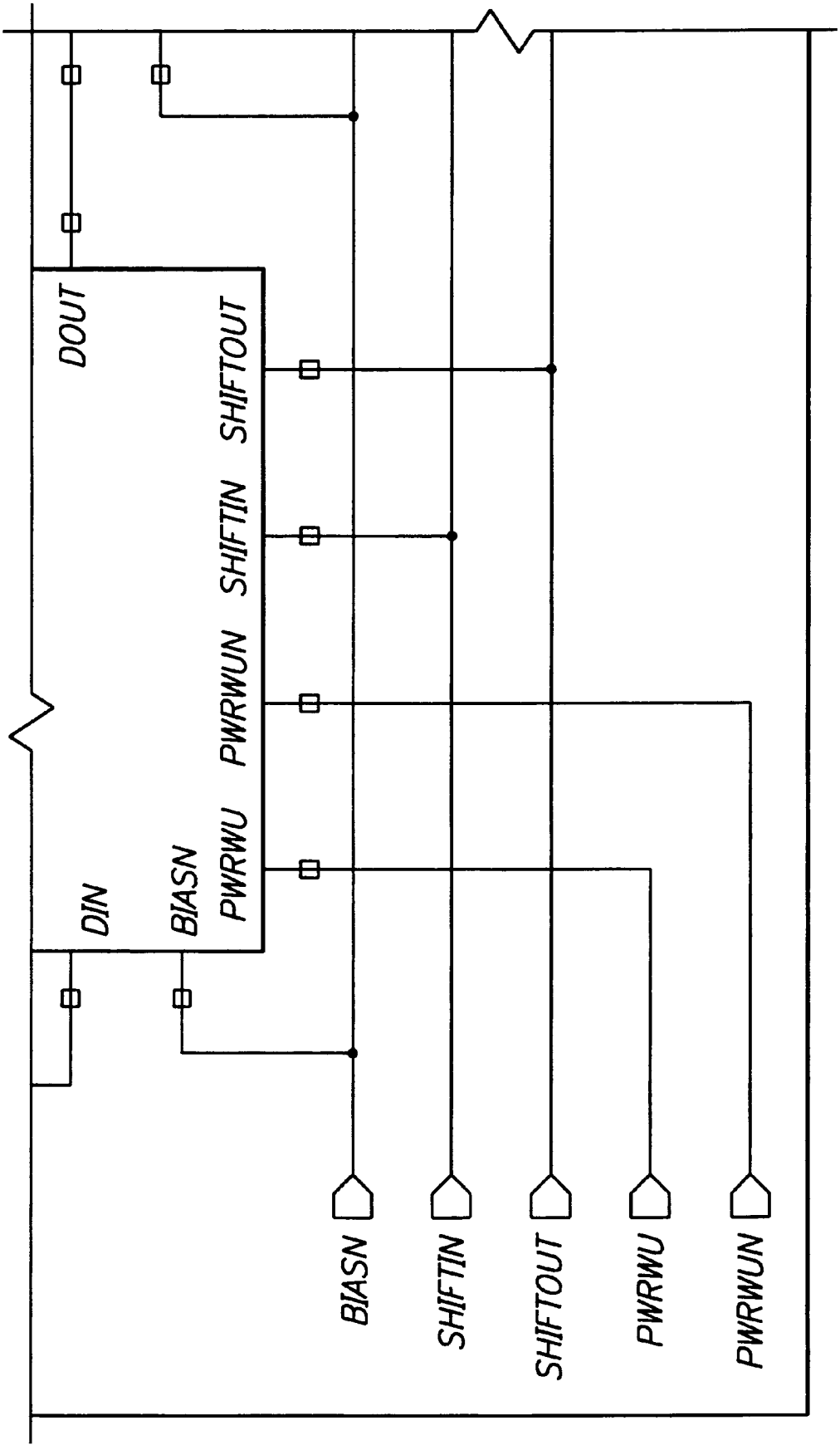


FIG 69.0900 ICA

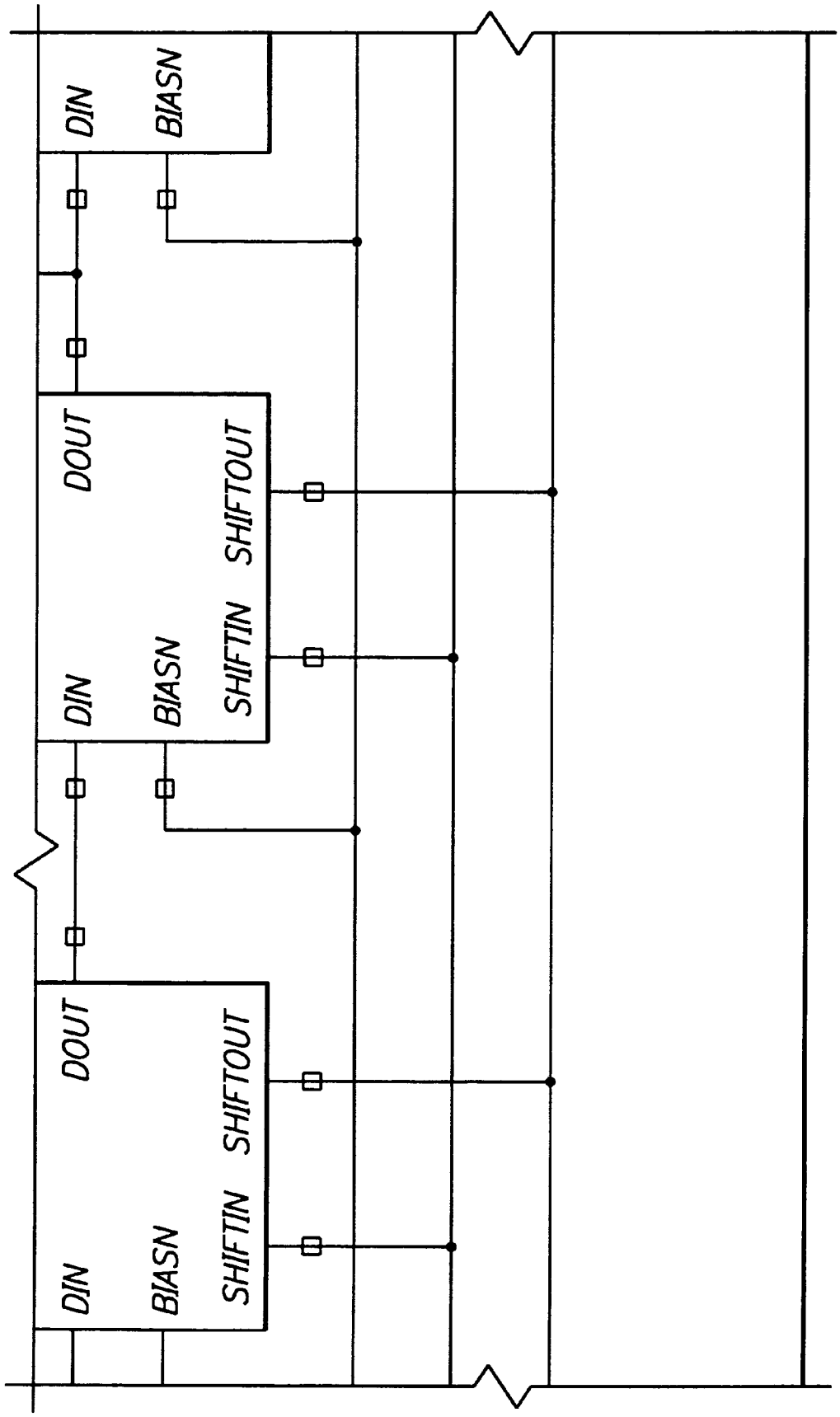

DIN
BIASN
DOUT
SHIFTOUT
SHIFTIN
DIN
BIASN
DOUT
SHIFTOUT
SHIFTIN
DIN
BIASN

FIG. 9,090,118

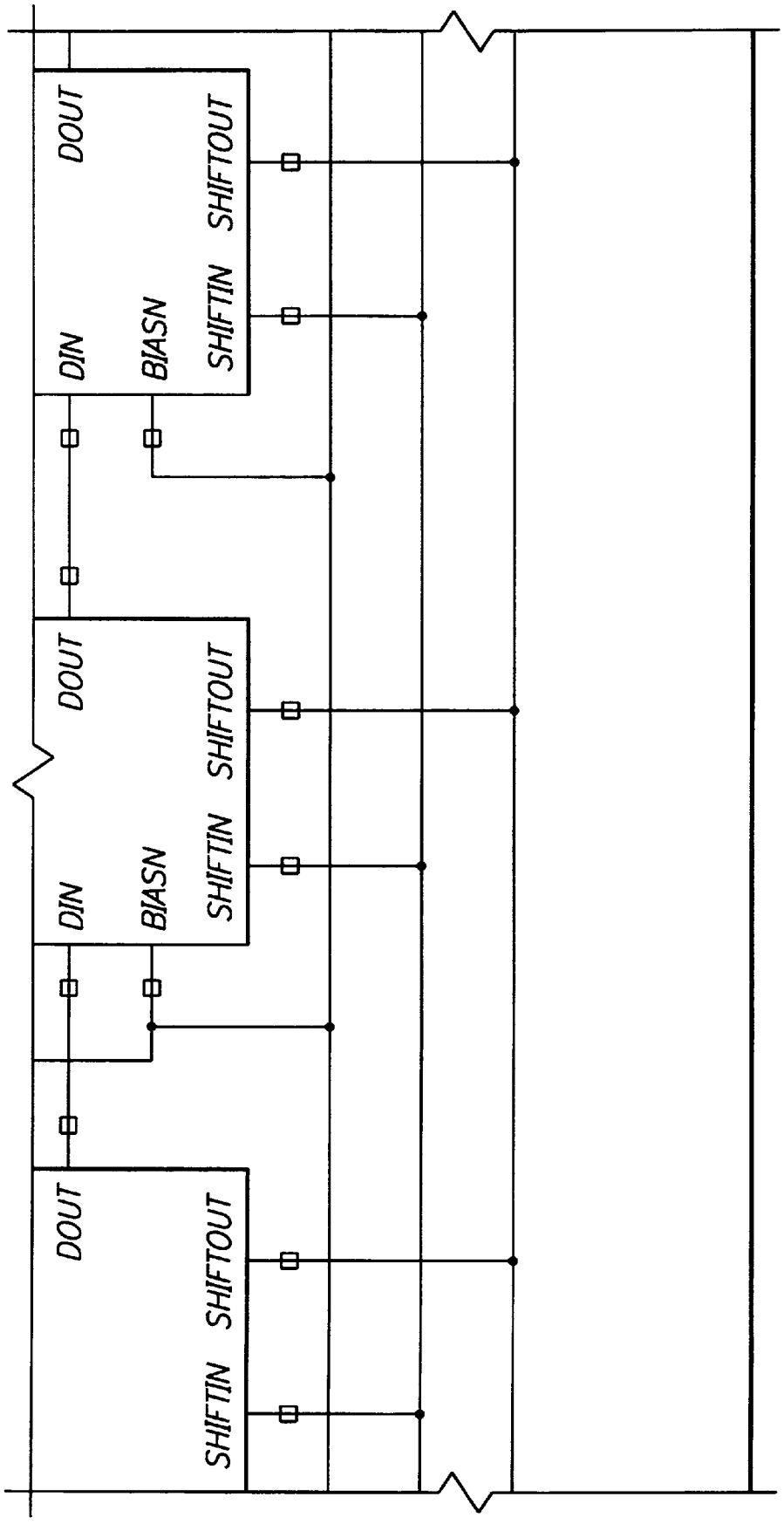

DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN
DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN
DOUT
SHIFTOUT
SHIFTIN

FIG. 9,090,116

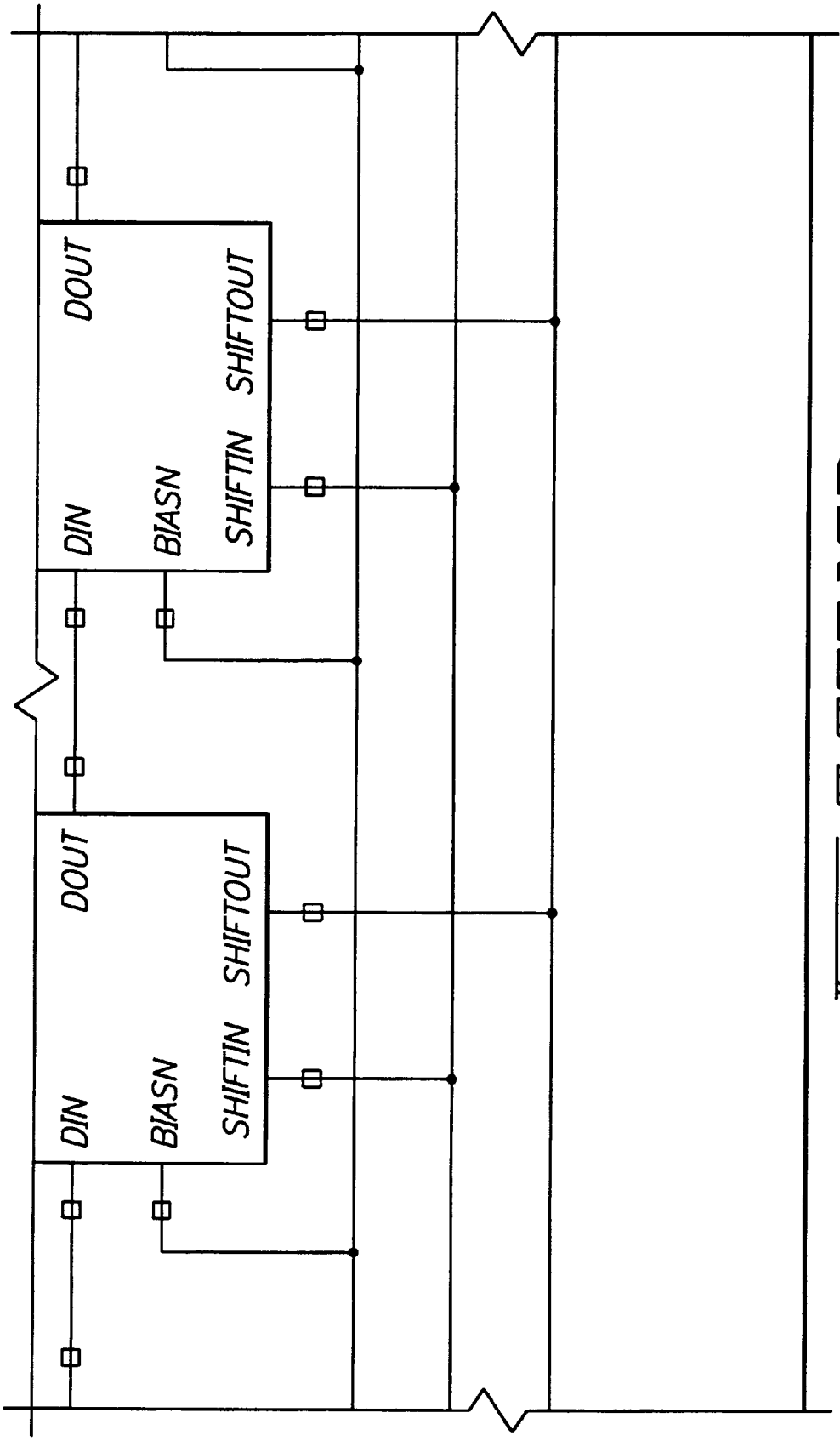

DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN
DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN

FIG 9,090,110

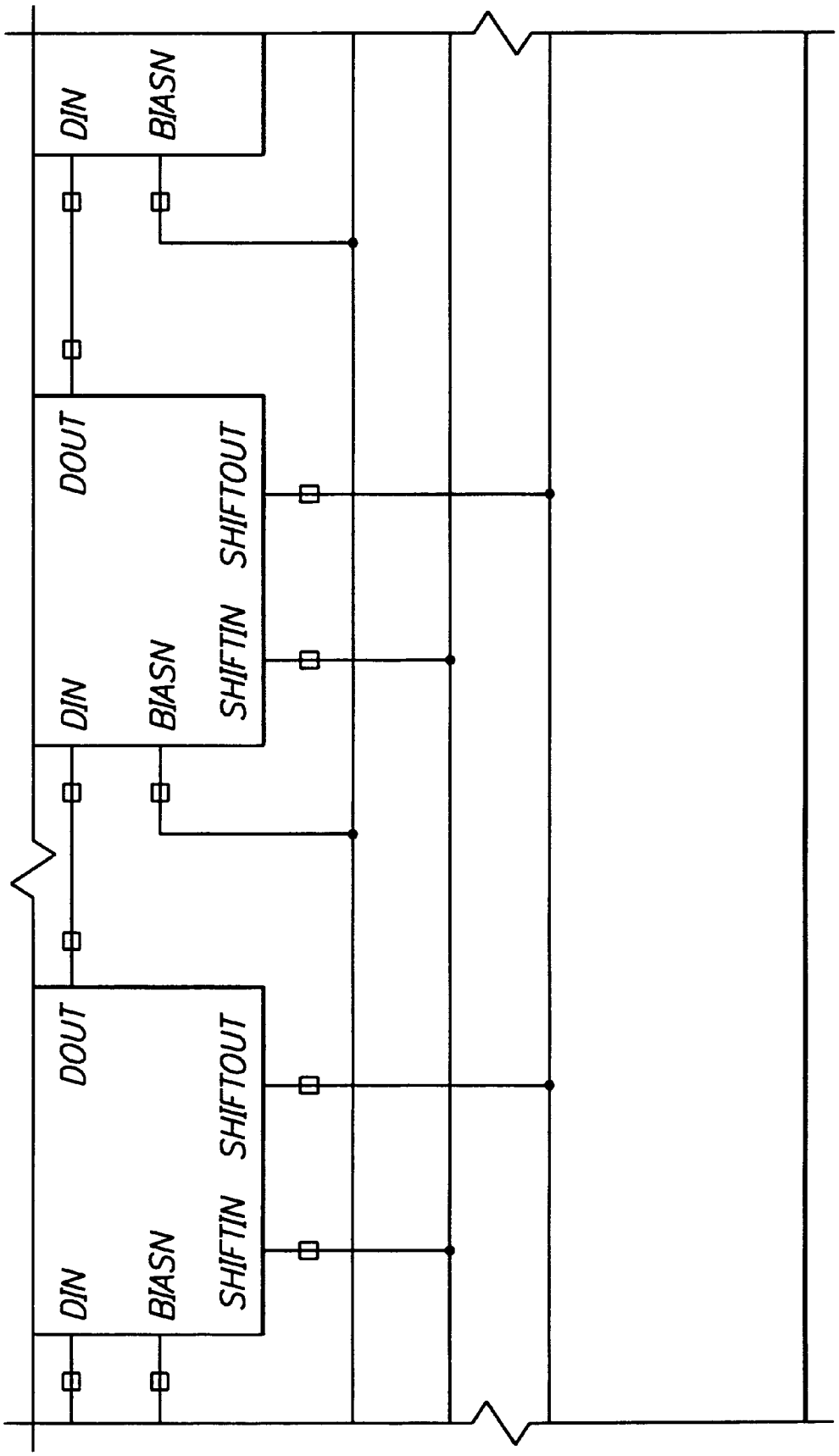


FIG 6,130,602 FIG 3H

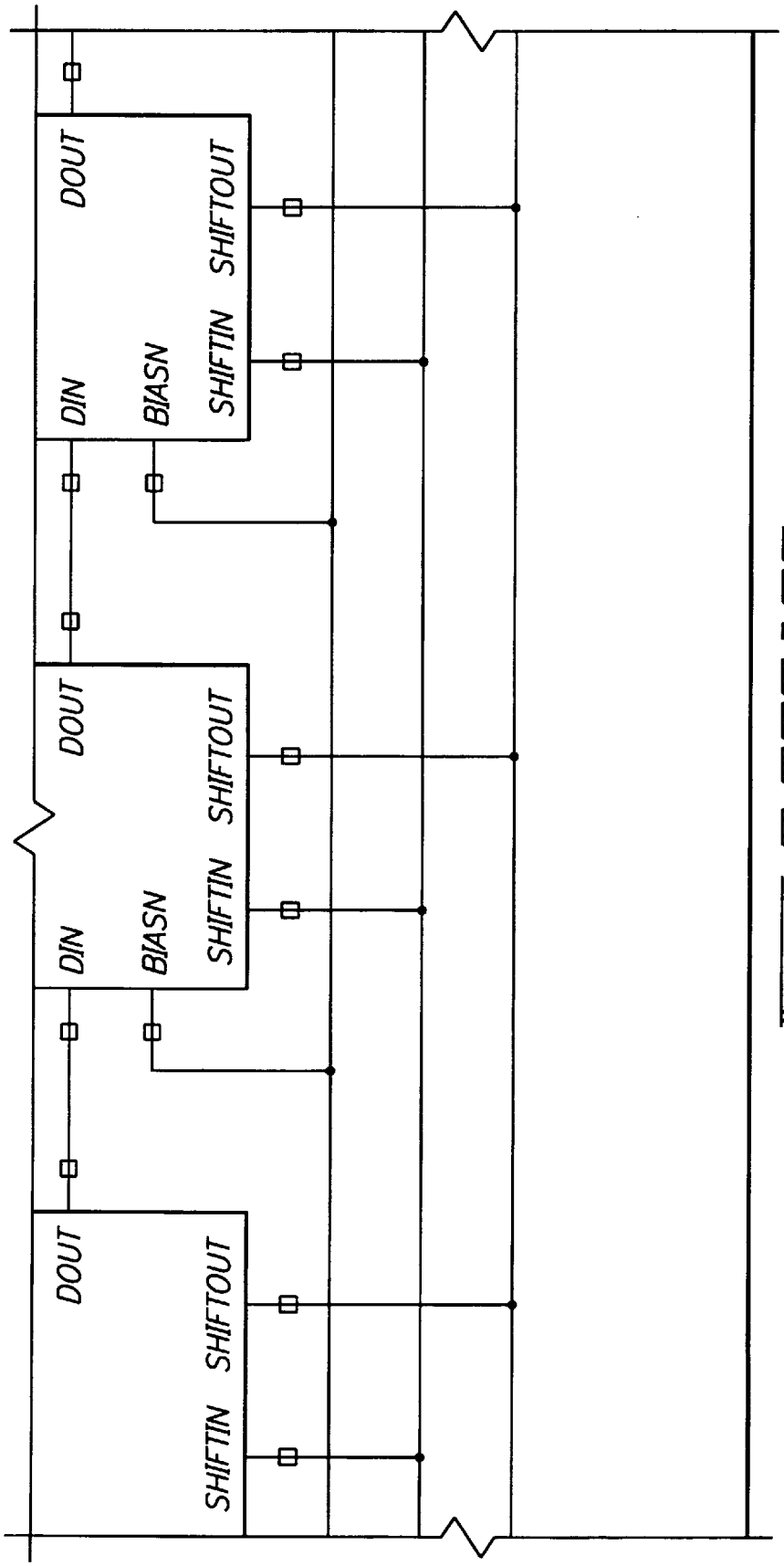


FIG 9,090,11CF

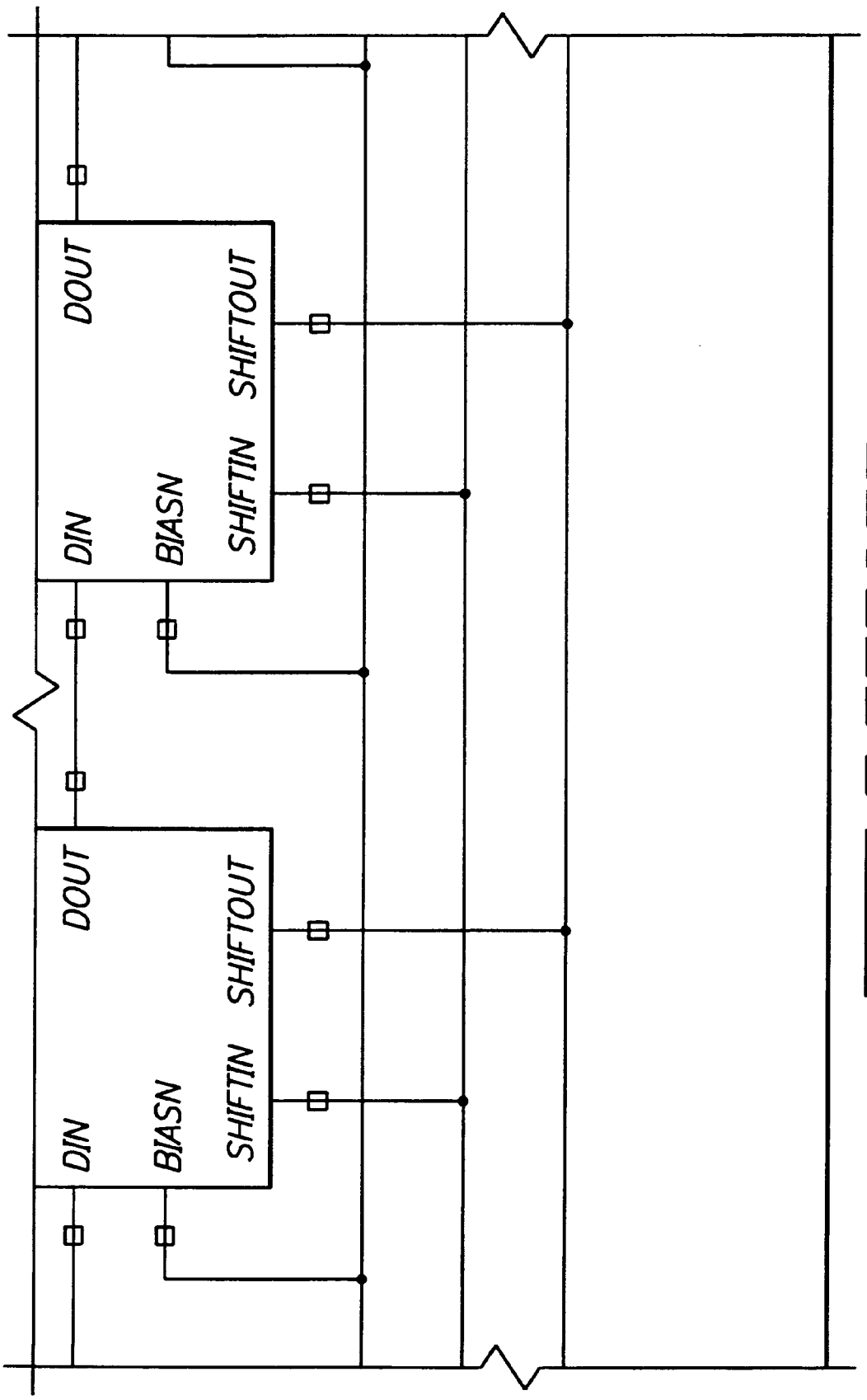

DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN
DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN

FIG 6,130,602

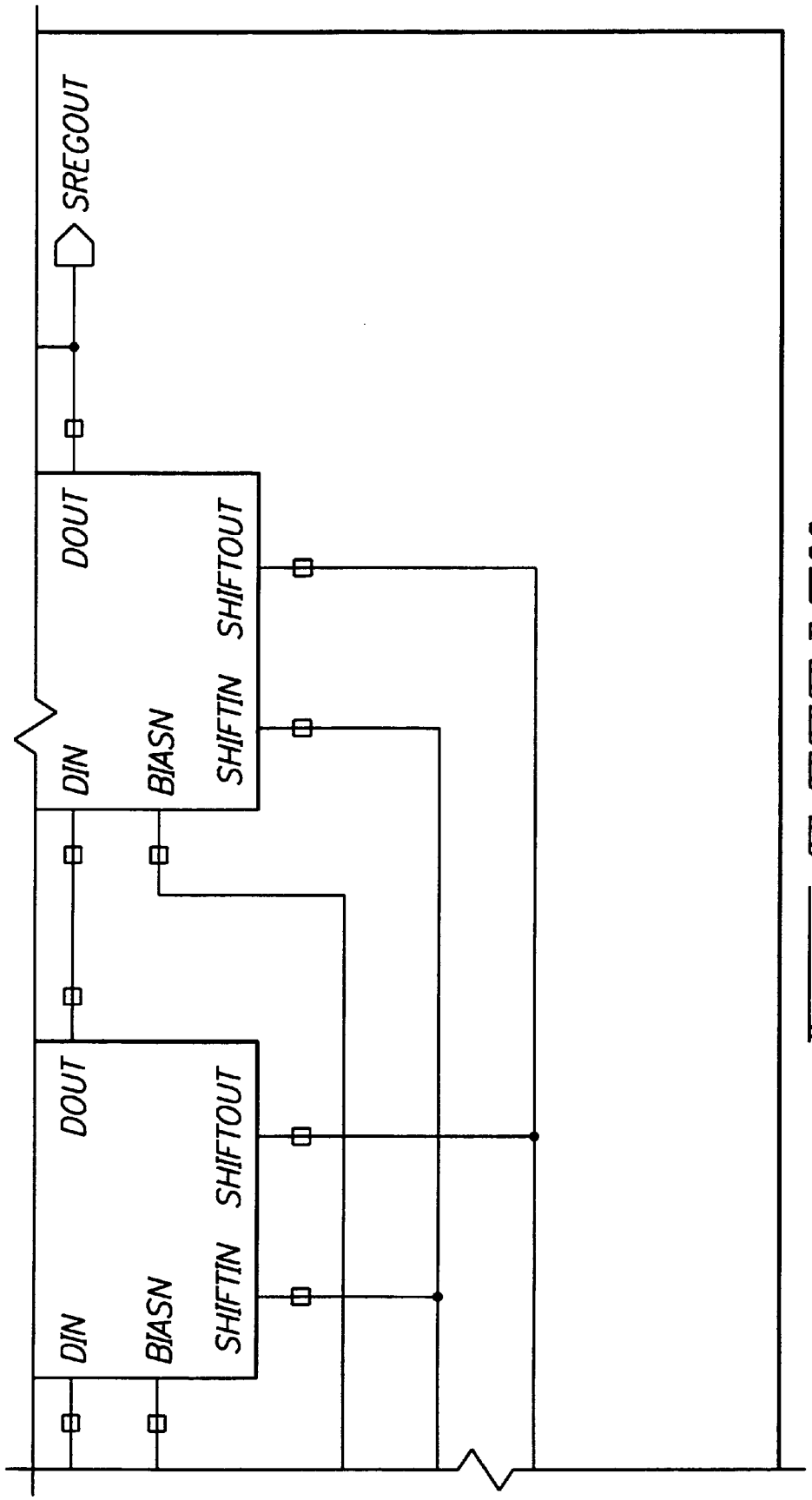

SREGOUT
DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN
DOUT
SHIFTOUT
DIN
BIASN
SHIFTIN

Fig. 96,001

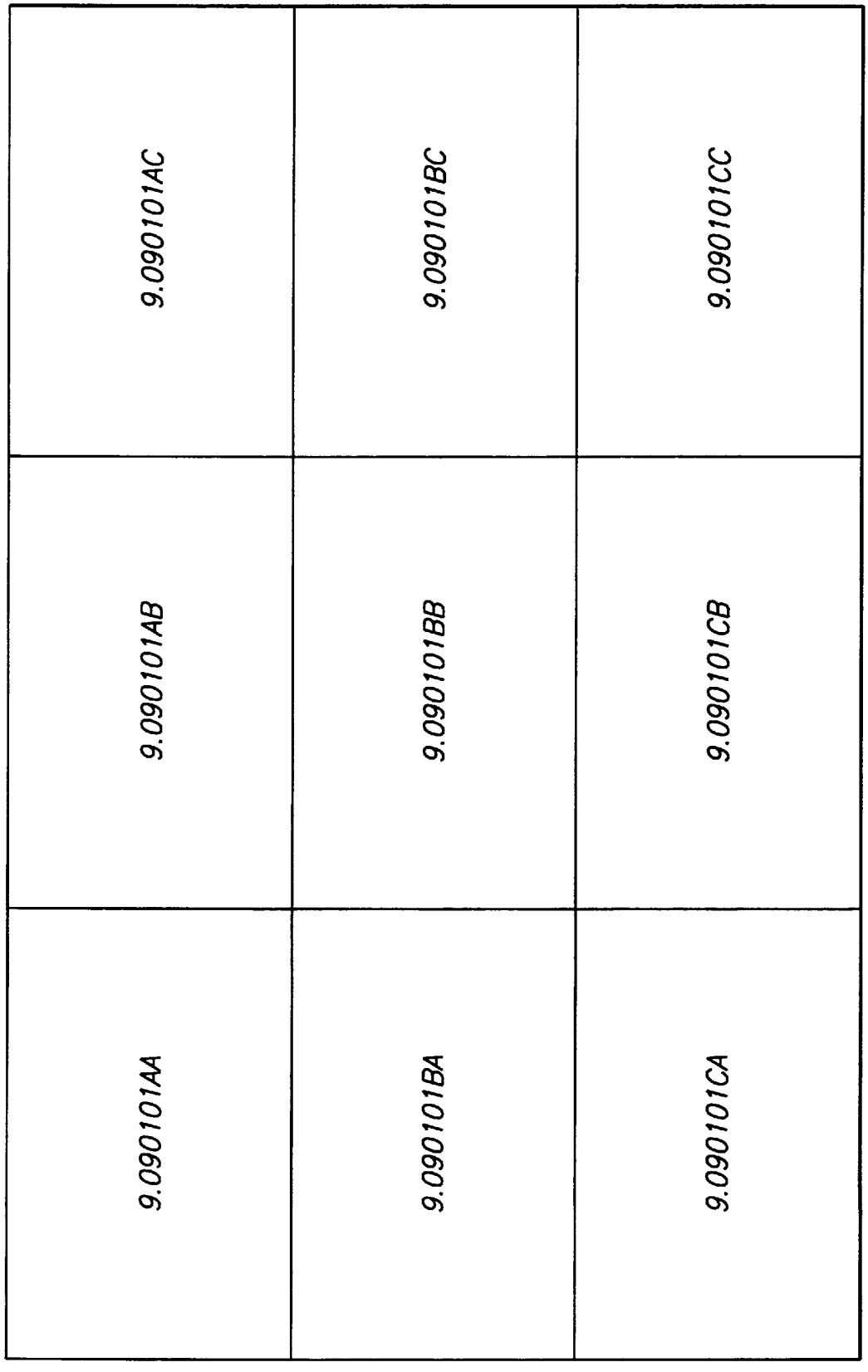
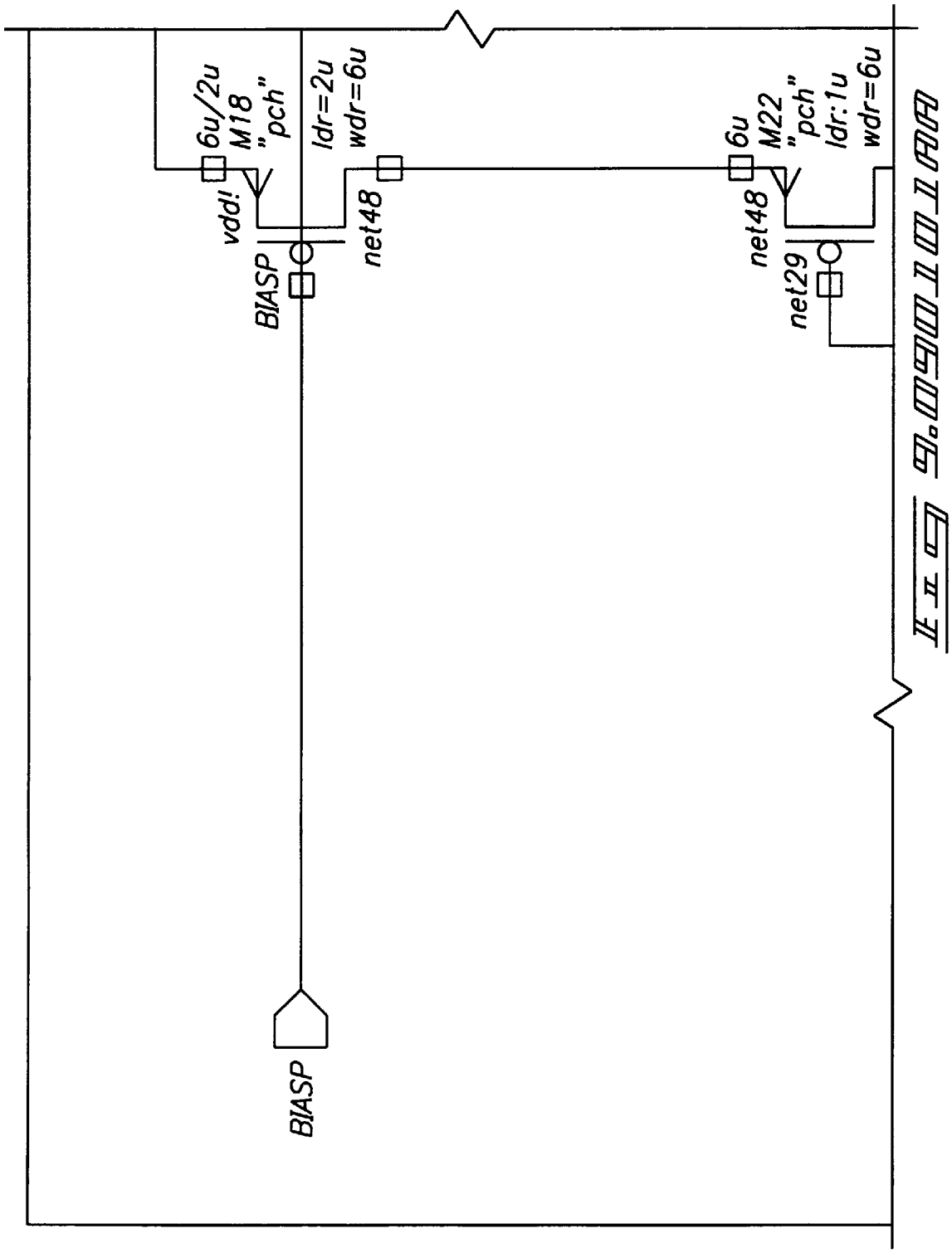

9.090101AC
9.090101BC
9.090101CC
9.090101AB
9.090101BB
9.090101CB
9.090101AA
9.090101BA
9.090101CA

FIG 9.090101


6u/2u
M18
"pch"
ldr=2u
wdr=6u
vdd!
BIASP
net48
6u
M22
"pch"
ldr:1u
wdr=6u
net48
net29
BIASP

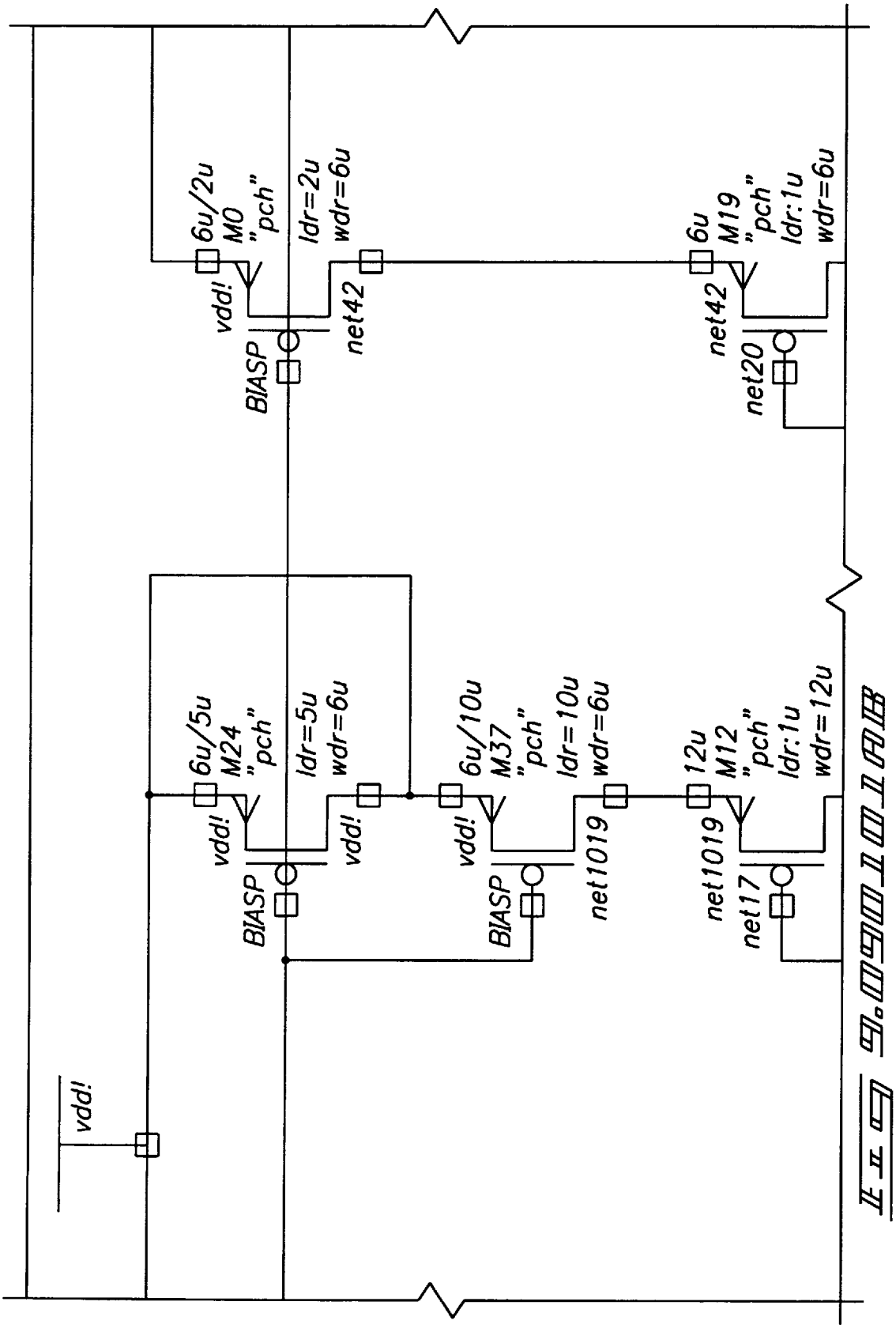
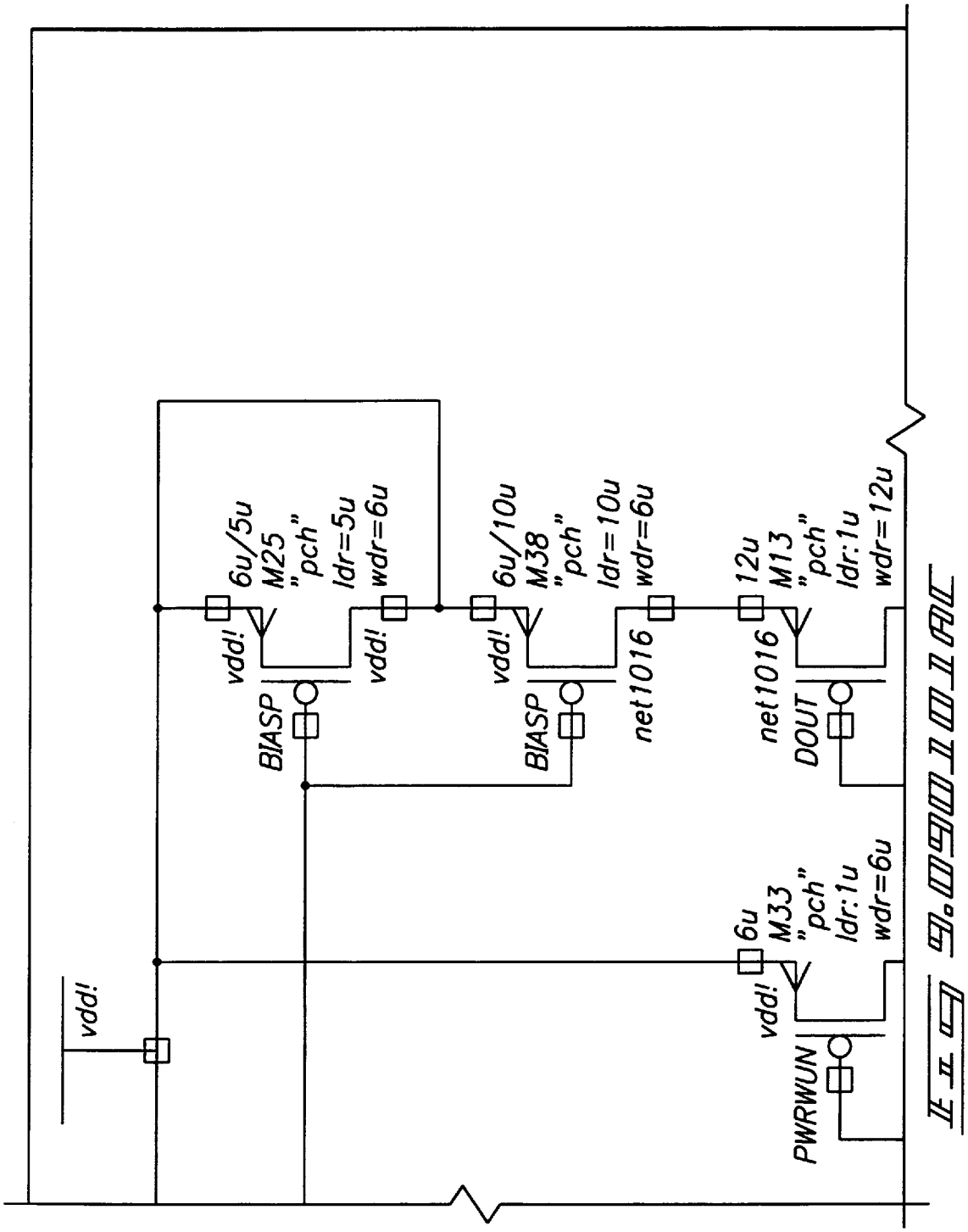
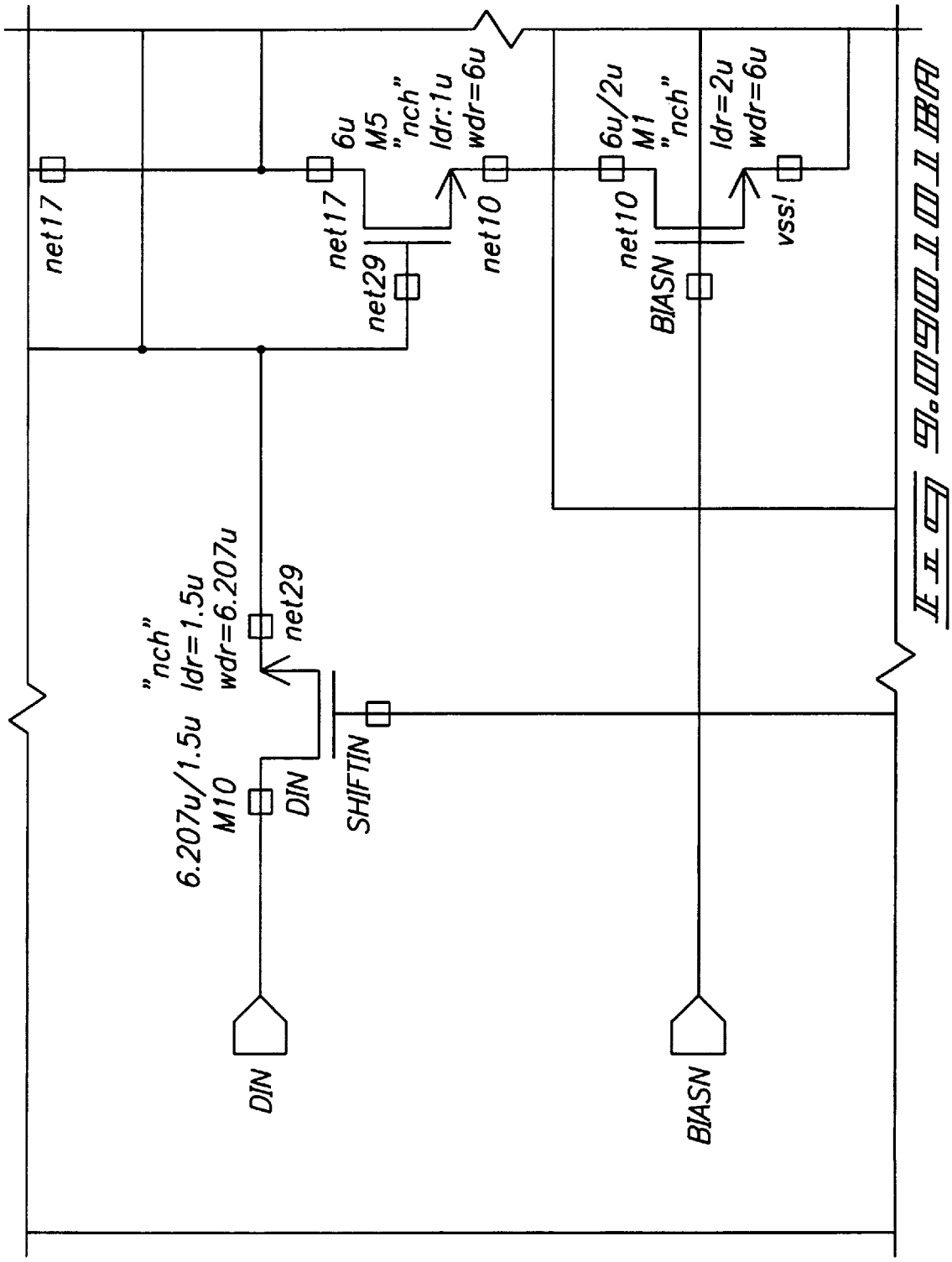
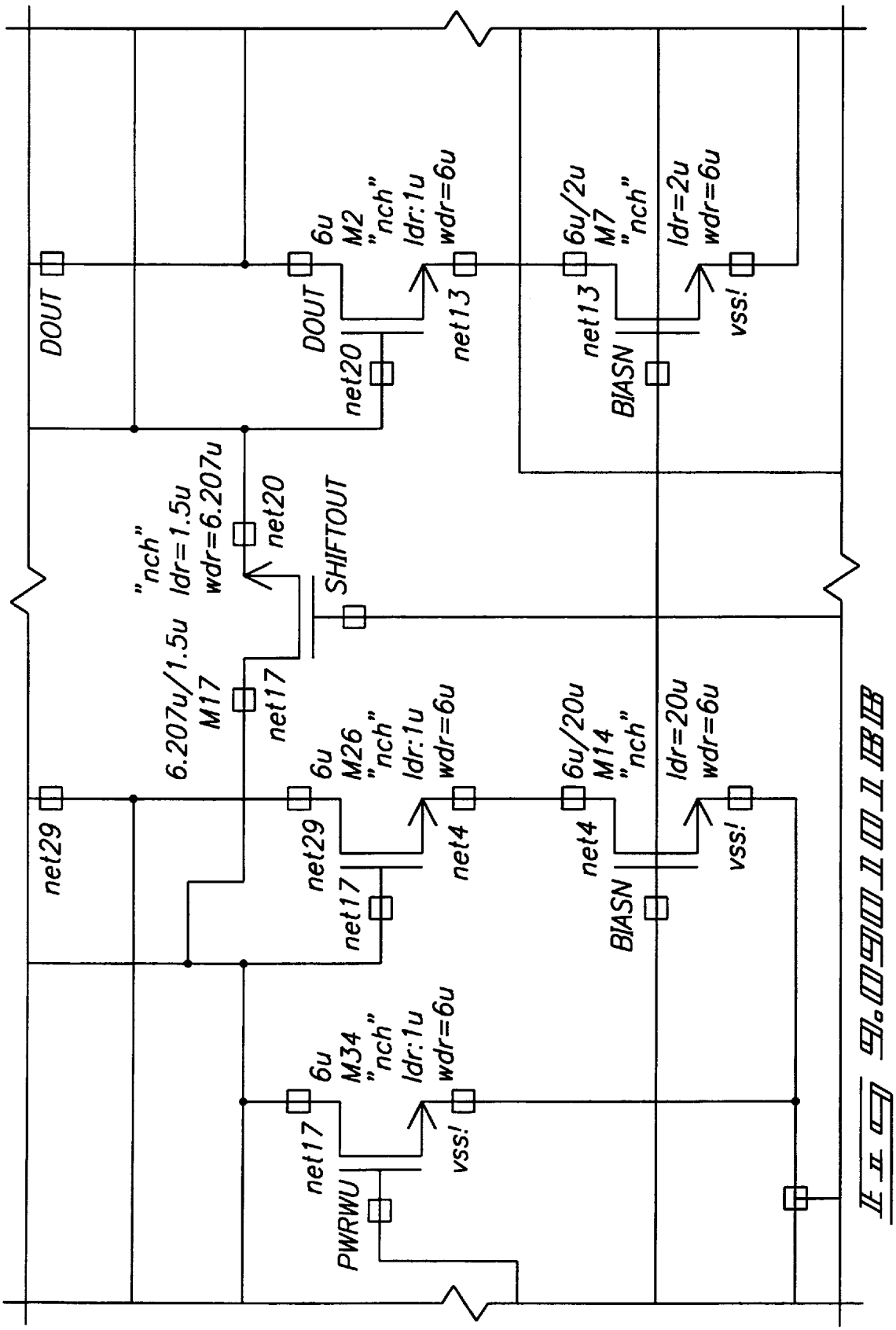


Fig. 9,090,110A/B


6u/5u
M25
"pch"
ldr=5u
wdr=6u
6u/10u
M38
"pch"
ldr=10u
wdr=6u
12u
M13
"pch"
ldr:1u
wdr=12u
6u
M33
"pch"
ldr:1u
wdr=6u
vdd!
BIASP
net1016
DOUT
PWRWUN


net17
6u
M5
"nch"
ldr:1u
wdr=6u
net17
net29
net10
6u/2u
M1
"nch"
ldr=2u
wdr=6u
net10
BIASN
vss!
"nch"
ldr=1.5u
wdr=6.207u
net29
6.207u/1.5u
M10
DIN
SHIFTIN
DIN
BIASN


DOUT
6u
M2
"nch"
ldr:1u
wdr=6u
DOUT
net20
net13
6u/2u
M7
"nch"
ldr=2u
wdr=6u
net13
BIASN
vss!
"nch"
ldr=1.5u
wdr=6.207u
net20
SHIFTOUT
6.207u/1.5u
M17
net17
net29
6u
M26
"nch"
ldr:1u
wdr=6u
6u/20u
M14
"nch"
ldr=20u
wdr=6u
net29
net17
net4
net4
BIASN
vss!
6u
M34
"nch"
ldr:1u
wdr=6u
net17
PWRWU
vss!

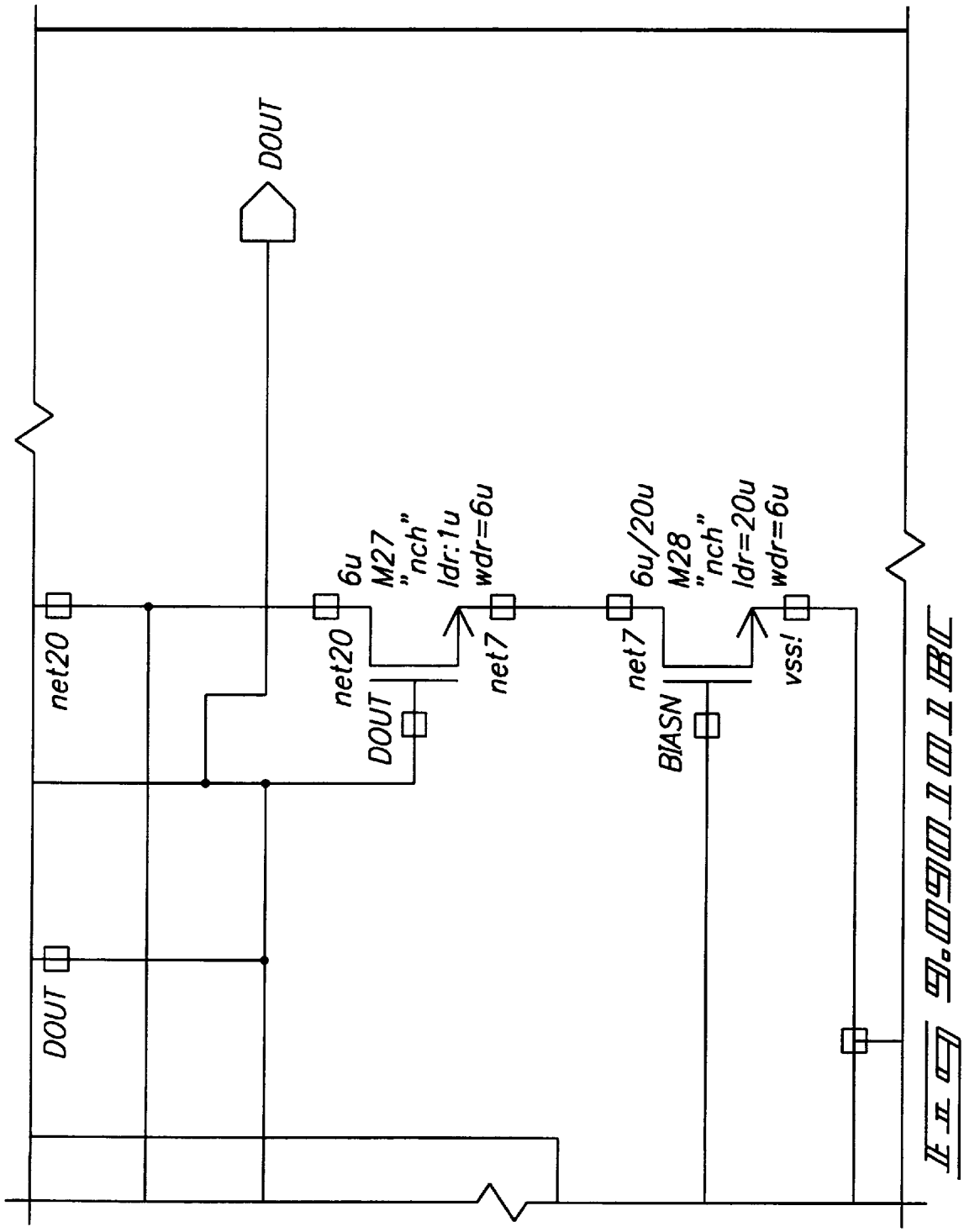


Fig. 9,090,110,181

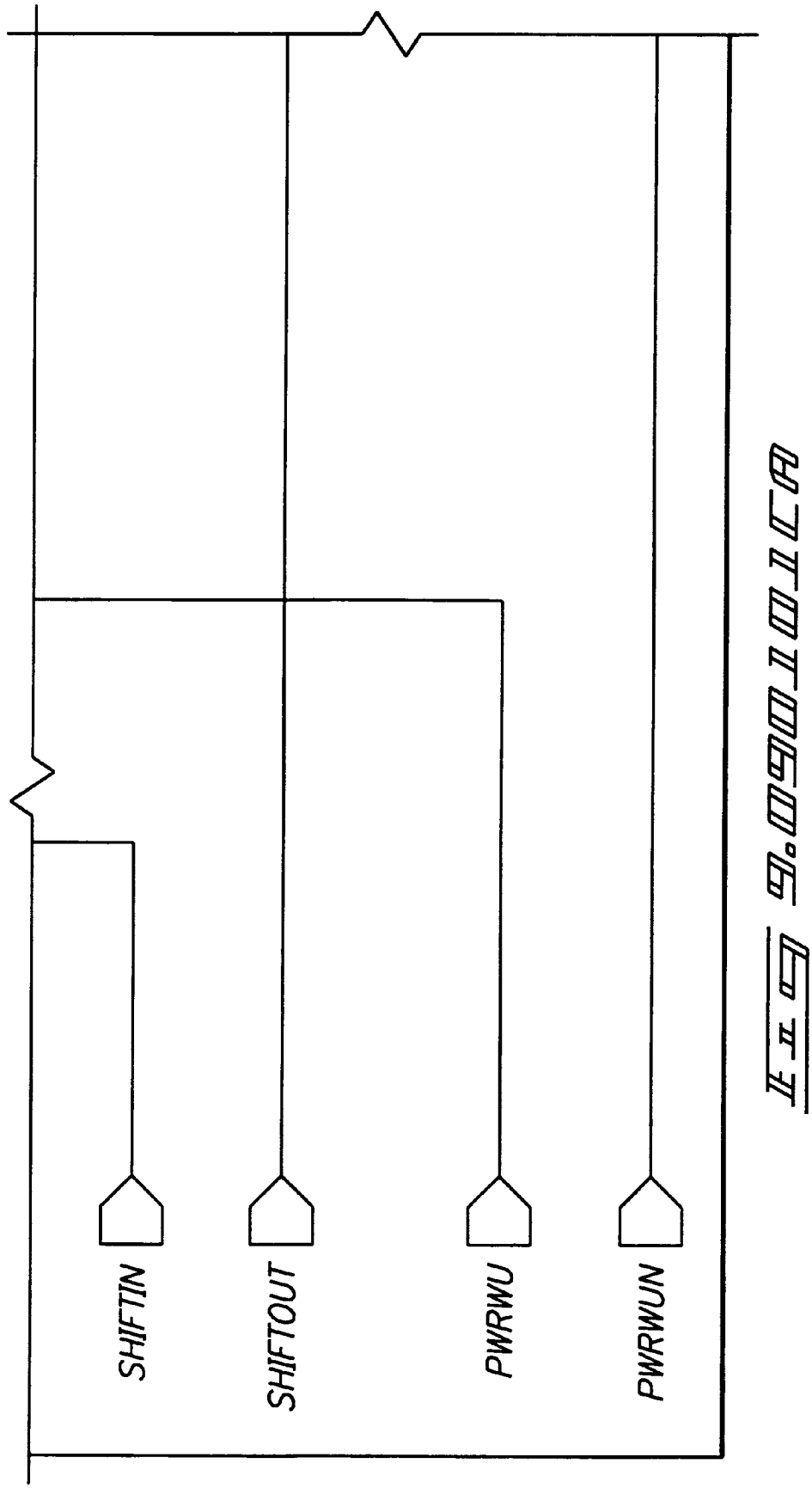


FIG 99,090,110 CA

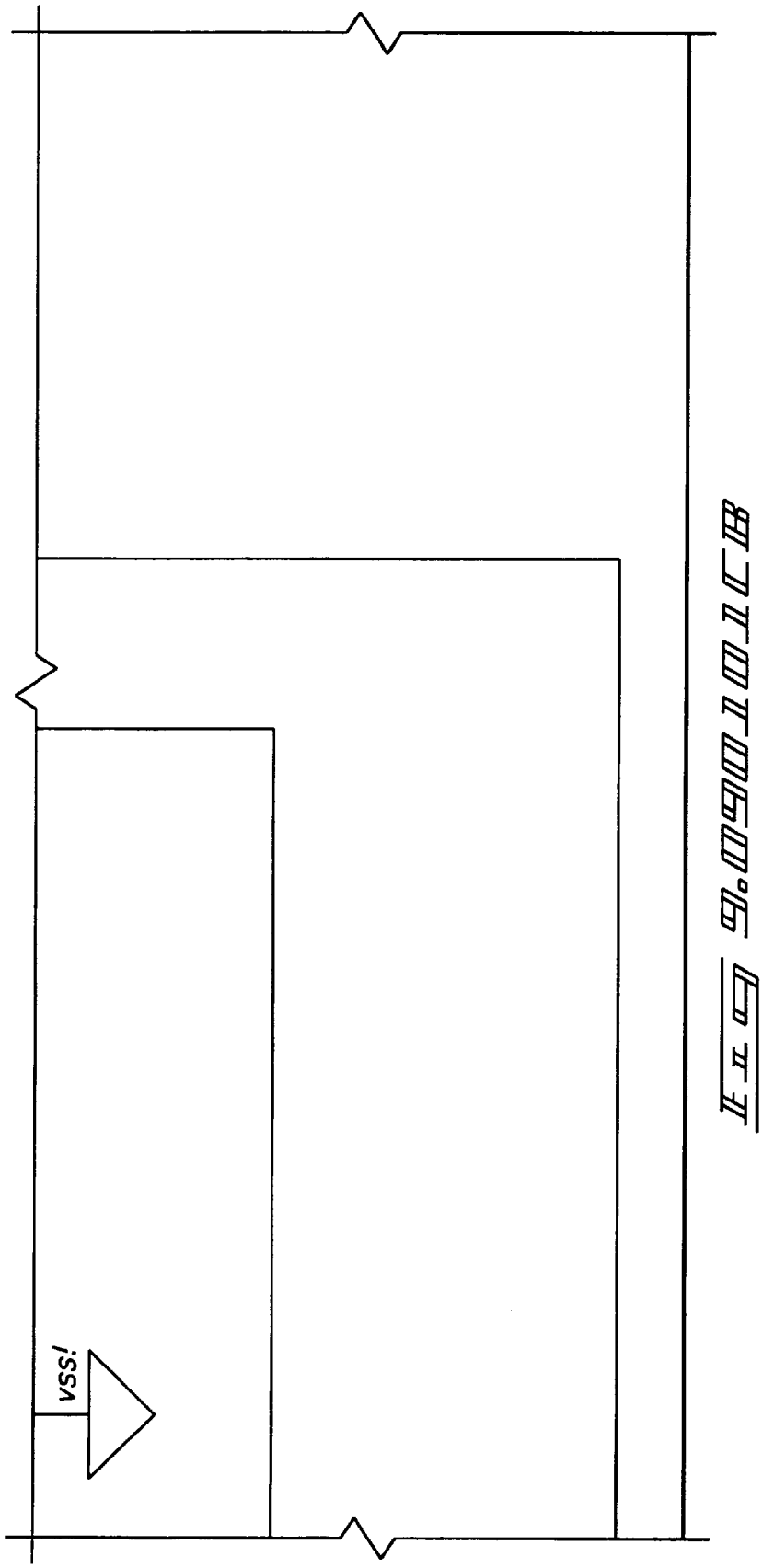


FIG. 9,090,110
VSS!

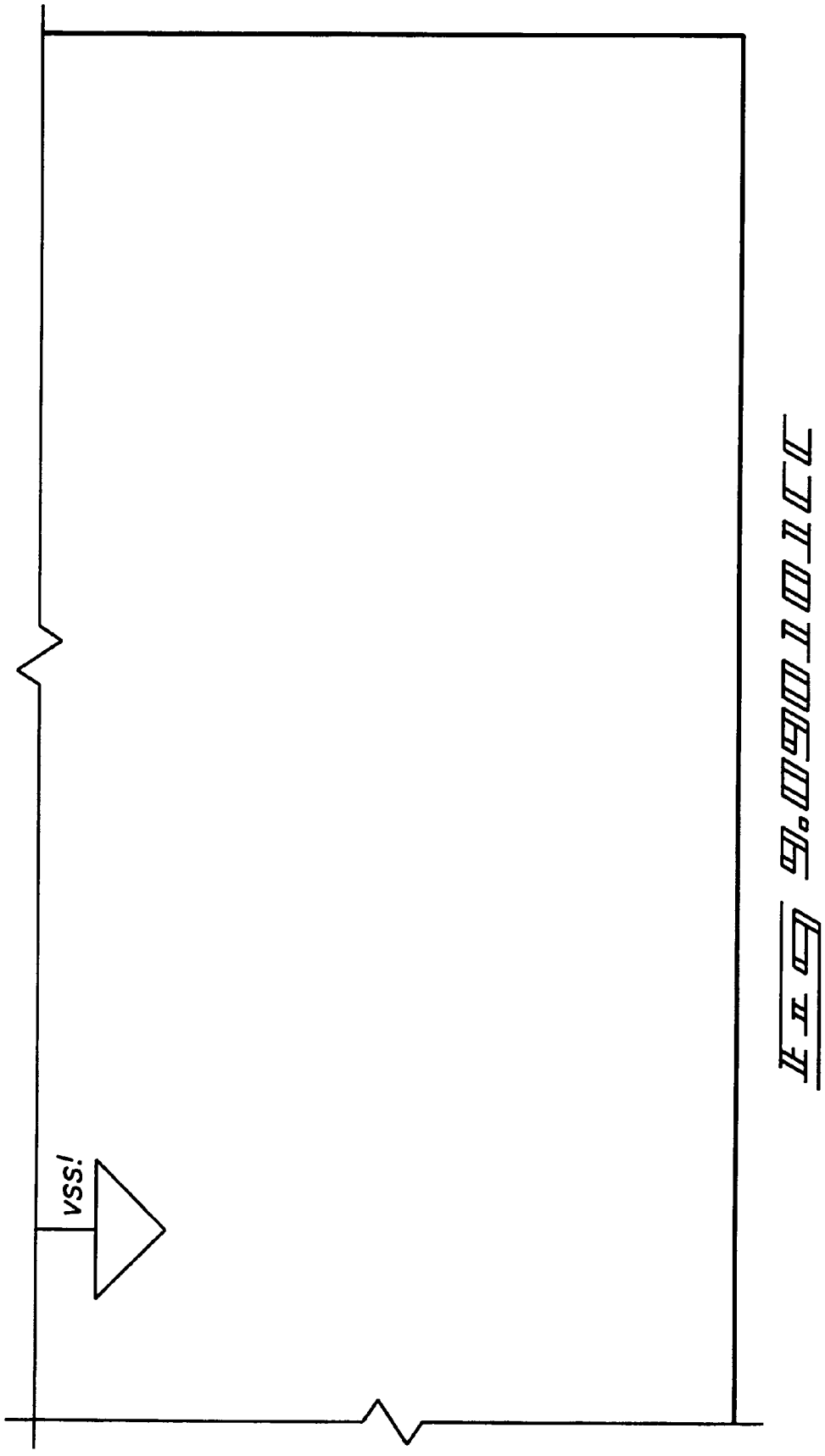


FIG 9,050,611

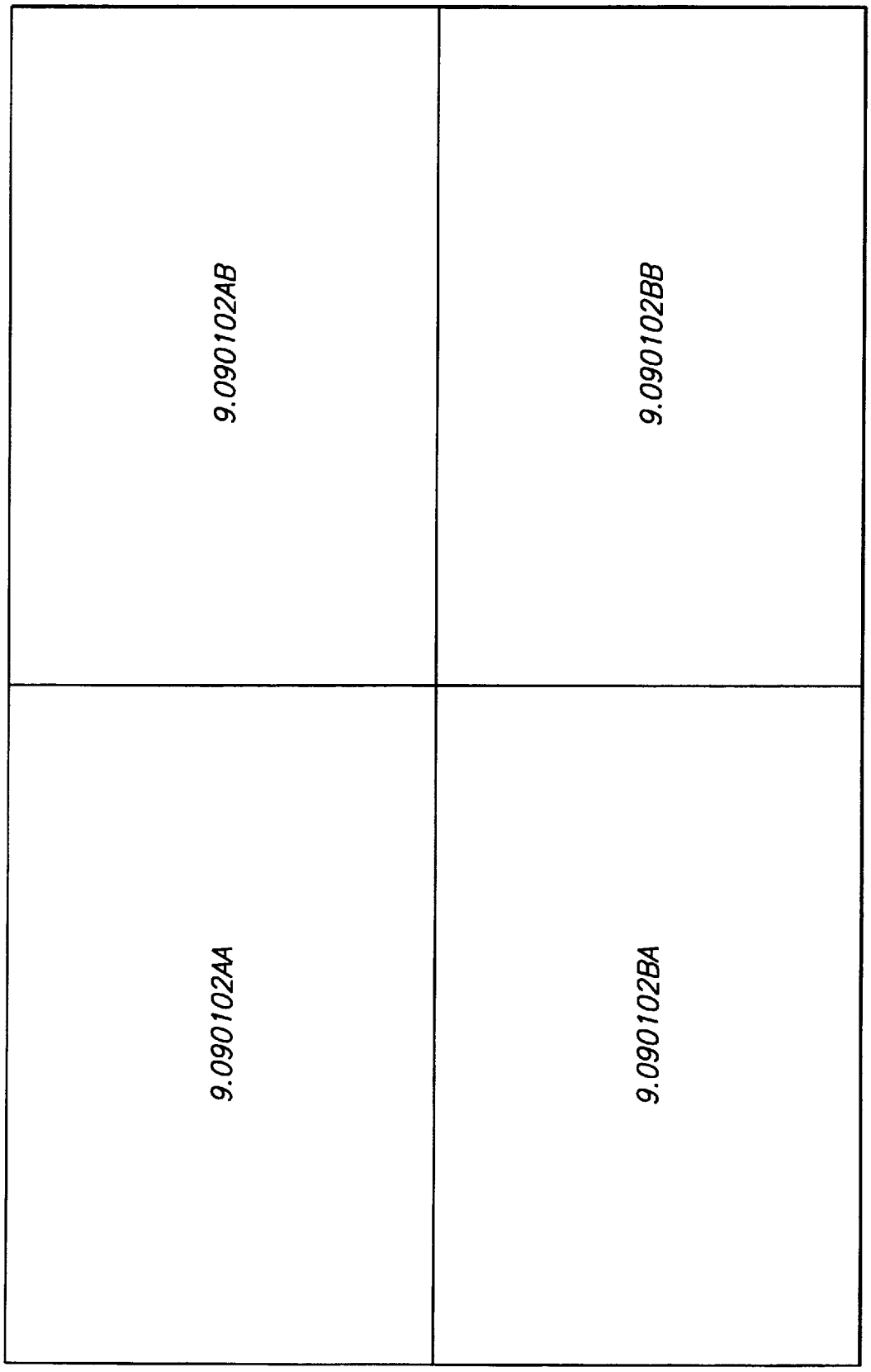


FIG 9.090102

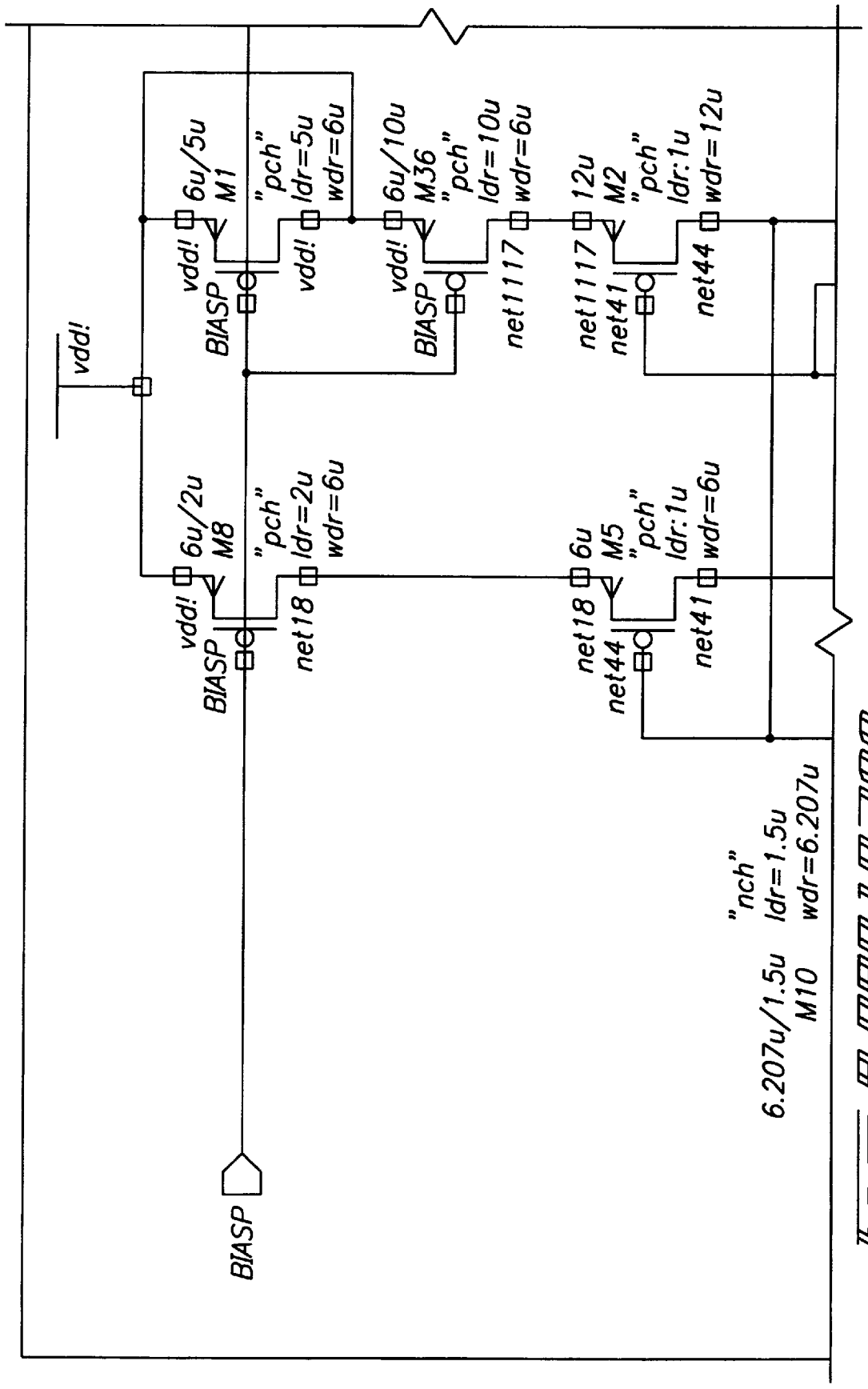
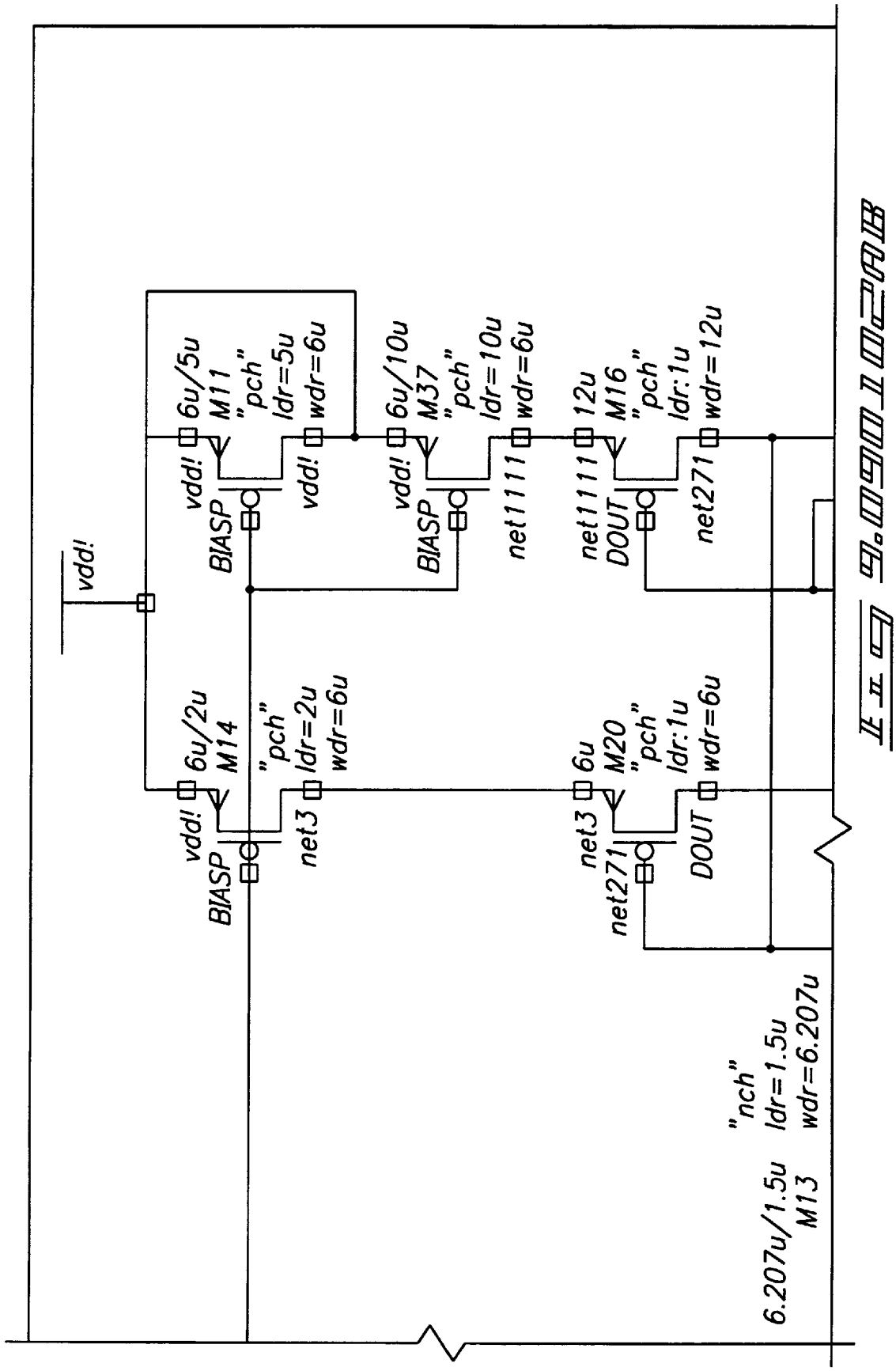


FIG. 9,090,II00ZAA


vdd!
6u/5u
M11
"pch"
ldr=5u
wdr=6u
vdd!
BIASP
vdd!
6u/10u
M37
"pch"
ldr=10u
wdr=6u
vdd!
BIASP
net1111
12u
M16
"pch"
ldr:1u
wdr=12u
net1111
DOUT
net271
6u/2u
M14
"pch"
ldr=2u
wdr=6u
vdd!
BIASP
net3
6u
M20
"pch"
ldr:1u
wdr=6u
net3
net271
DOUT
"nch"
ldr=1.5u
wdr=6.207u
6.207u/1.5u
M13

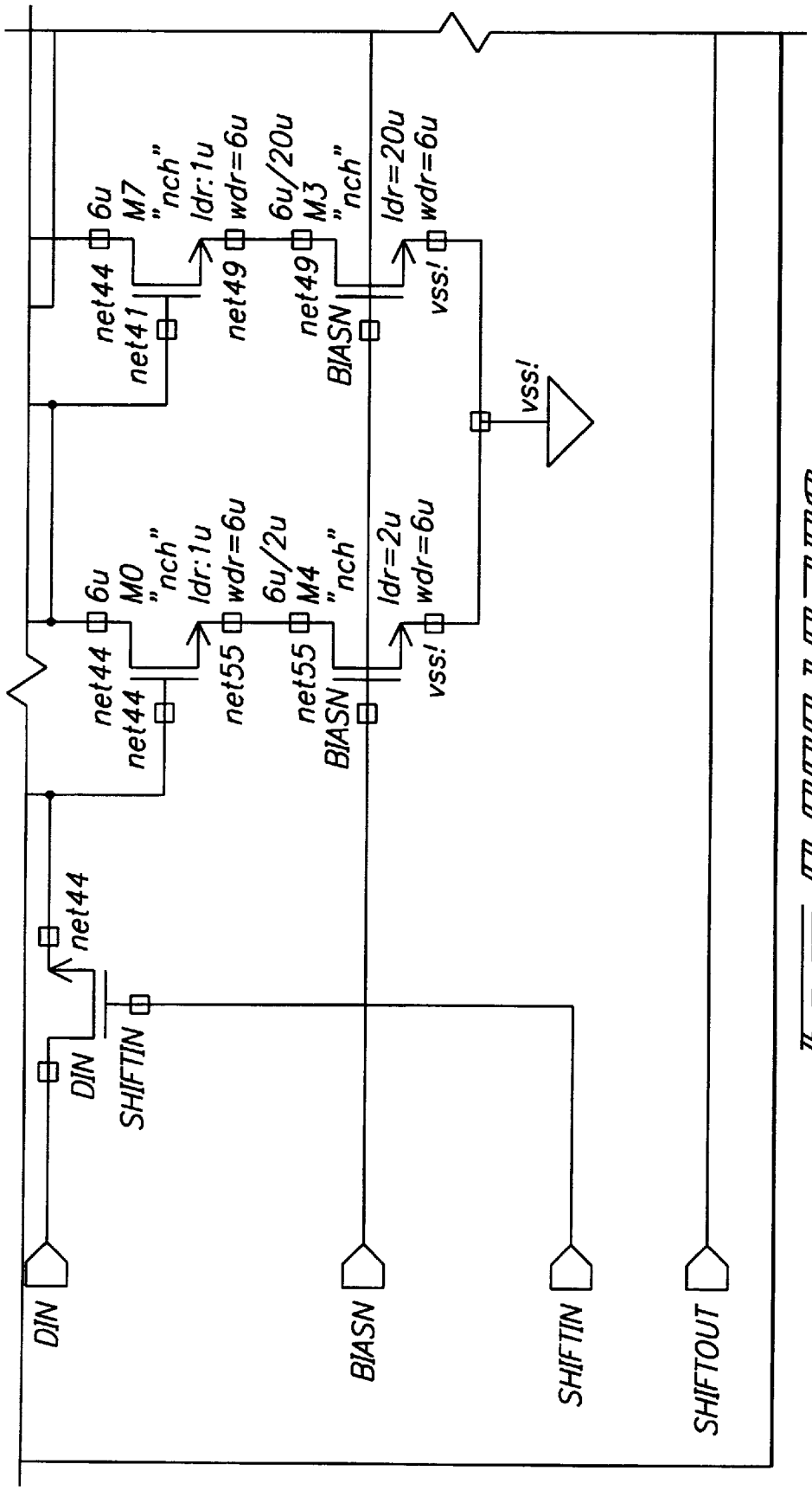


FIG 9,090,110,2BA

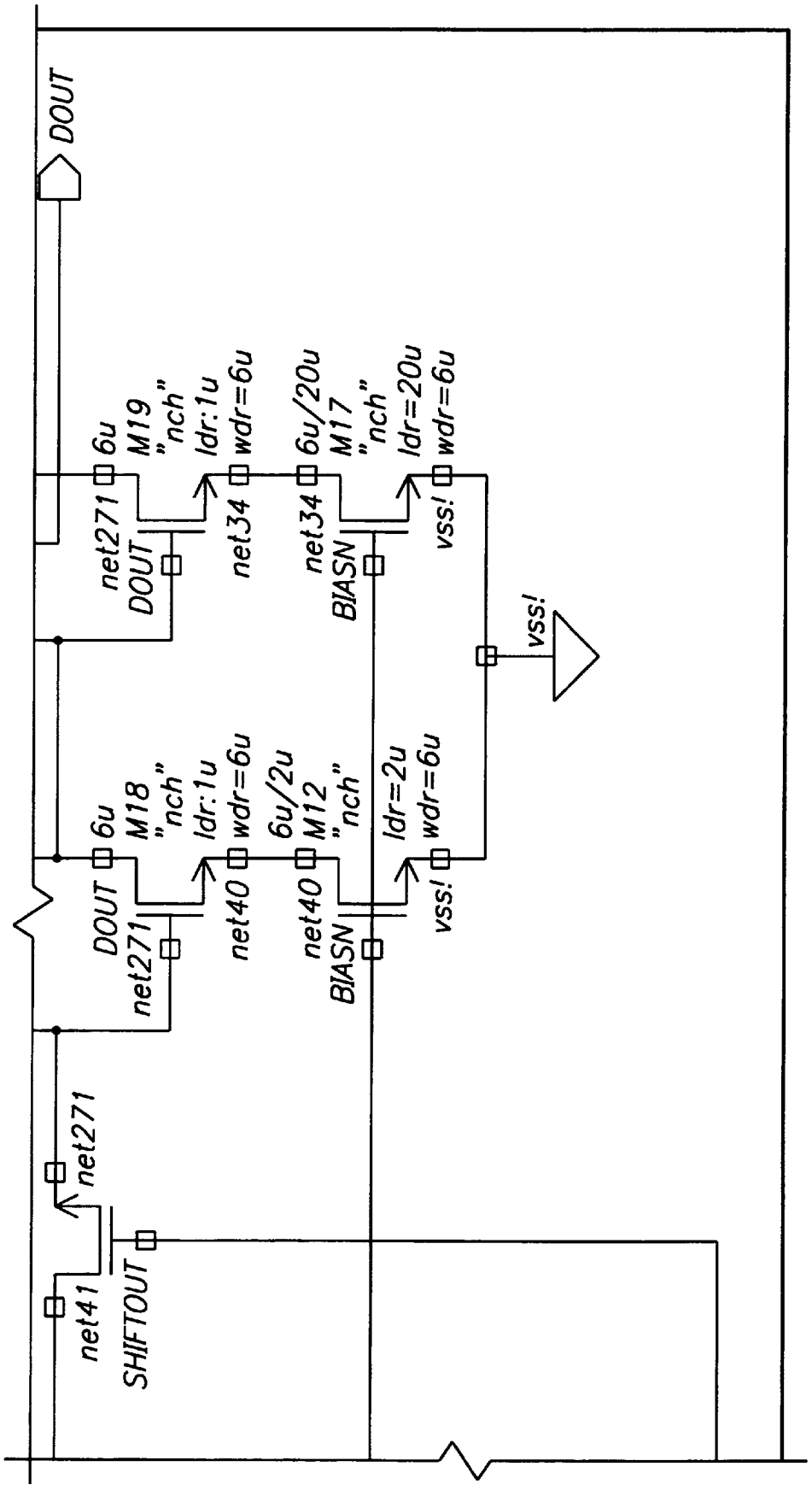

DOUT
6u
M19
"nch"
ldr:1u
wdr=6u
6u/20u
M17
"nch"
ldr=20u
wdr=6u
net271
DOUT
net34
net34
BIASN
vss!
vss!
6u
M18
"nch"
ldr:1u
wdr=6u
6u/2u
M12
"nch"
ldr=2u
wdr=6u
DOUT
net271
net40
net40
BIASN
vss!
net271
net41
SHIFTOUT

FIG 6,130,602

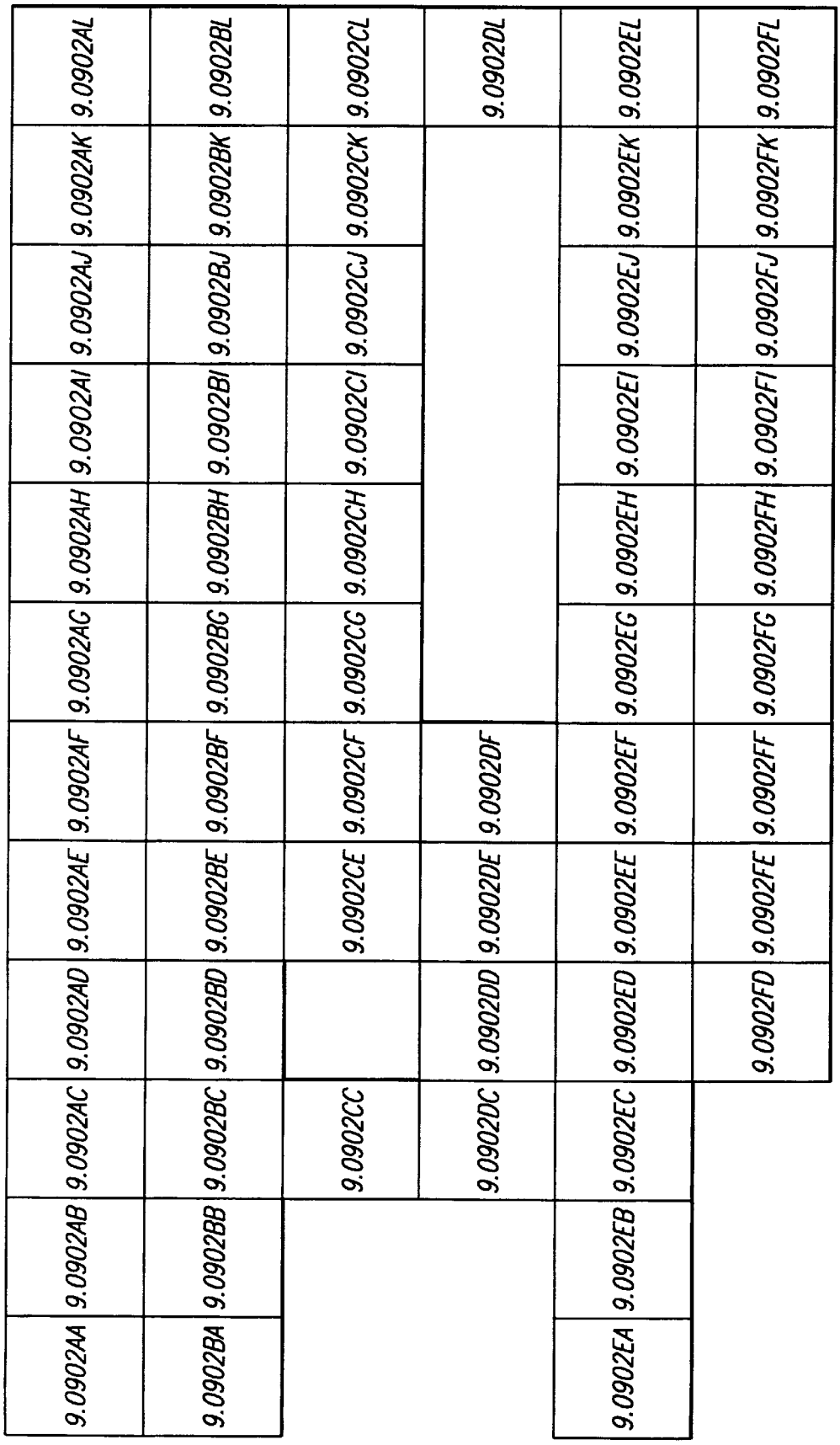
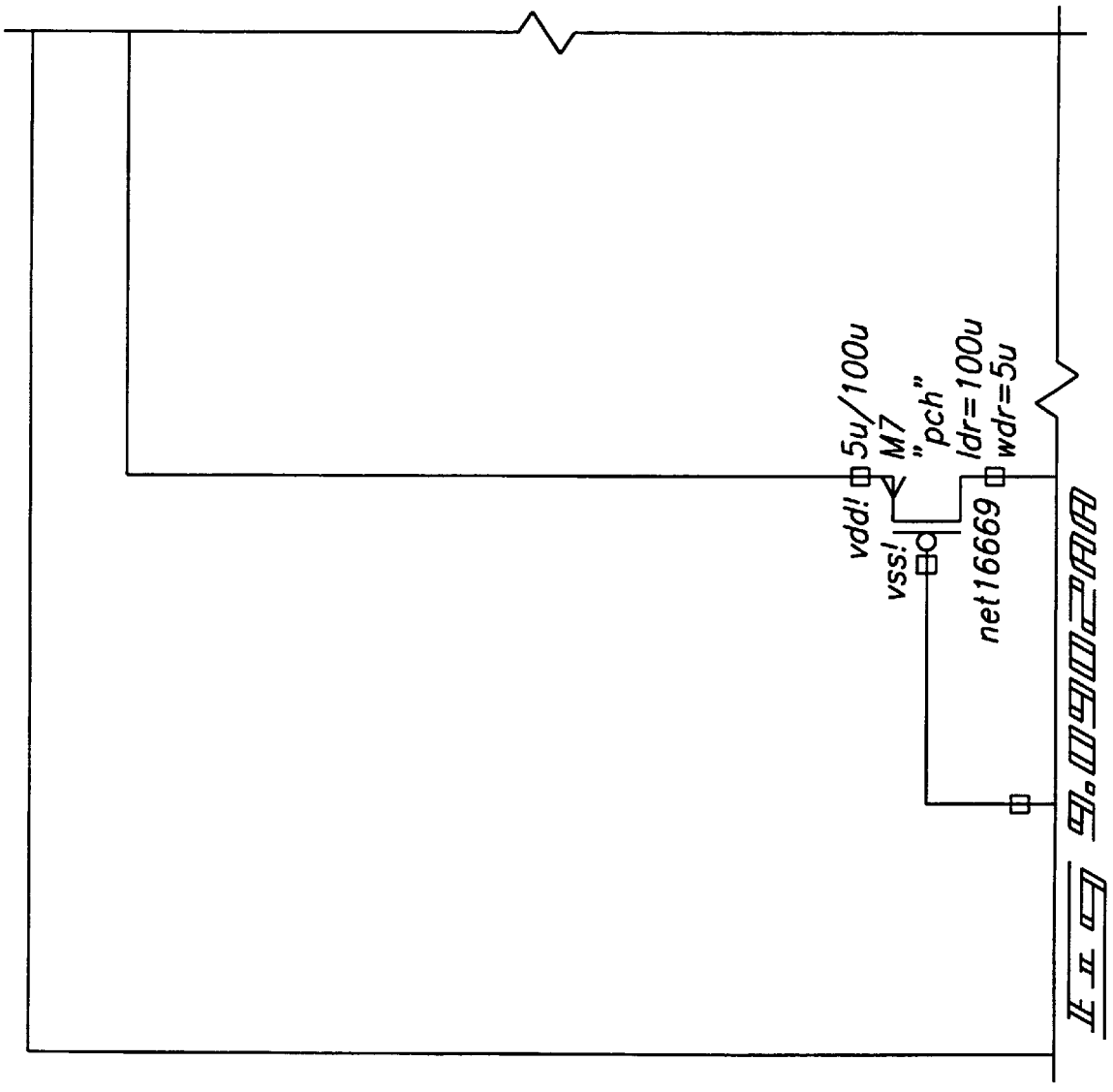

9.0902AA 9.0902AB 9.0902AC 9.0902AD 9.0902AE 9.0902AF 9.0902AG 9.0902AH 9.0902AI 9.0902AJ 9.0902AK 9.0902AL
9.0902BA 9.0902BB 9.0902BC 9.0902BD 9.0902BE 9.0902BF 9.0902BG 9.0902BH 9.0902BI 9.0902BJ 9.0902BK 9.0902BL
9.0902CC 9.0902CE 9.0902CF 9.0902CG 9.0902CH 9.0902CI 9.0902CJ 9.0902CK 9.0902CL
9.0902DC 9.0902DD 9.0902DE 9.0902DF 9.0902DL
9.0902EA 9.0902EB 9.0902EC 9.0902ED 9.0902EE 9.0902EF 9.0902EG 9.0902EH 9.0902EI 9.0902EJ 9.0902EK 9.0902EL
9.0902FD 9.0902FE 9.0902FF 9.0902FG 9.0902FH 9.0902FI 9.0902FJ 9.0902FK 9.0902FL

FIG. 9.0902


5u/100u
M7
"pch"
ldr=100u
wdr=5u
vdd!
vss!
net16669

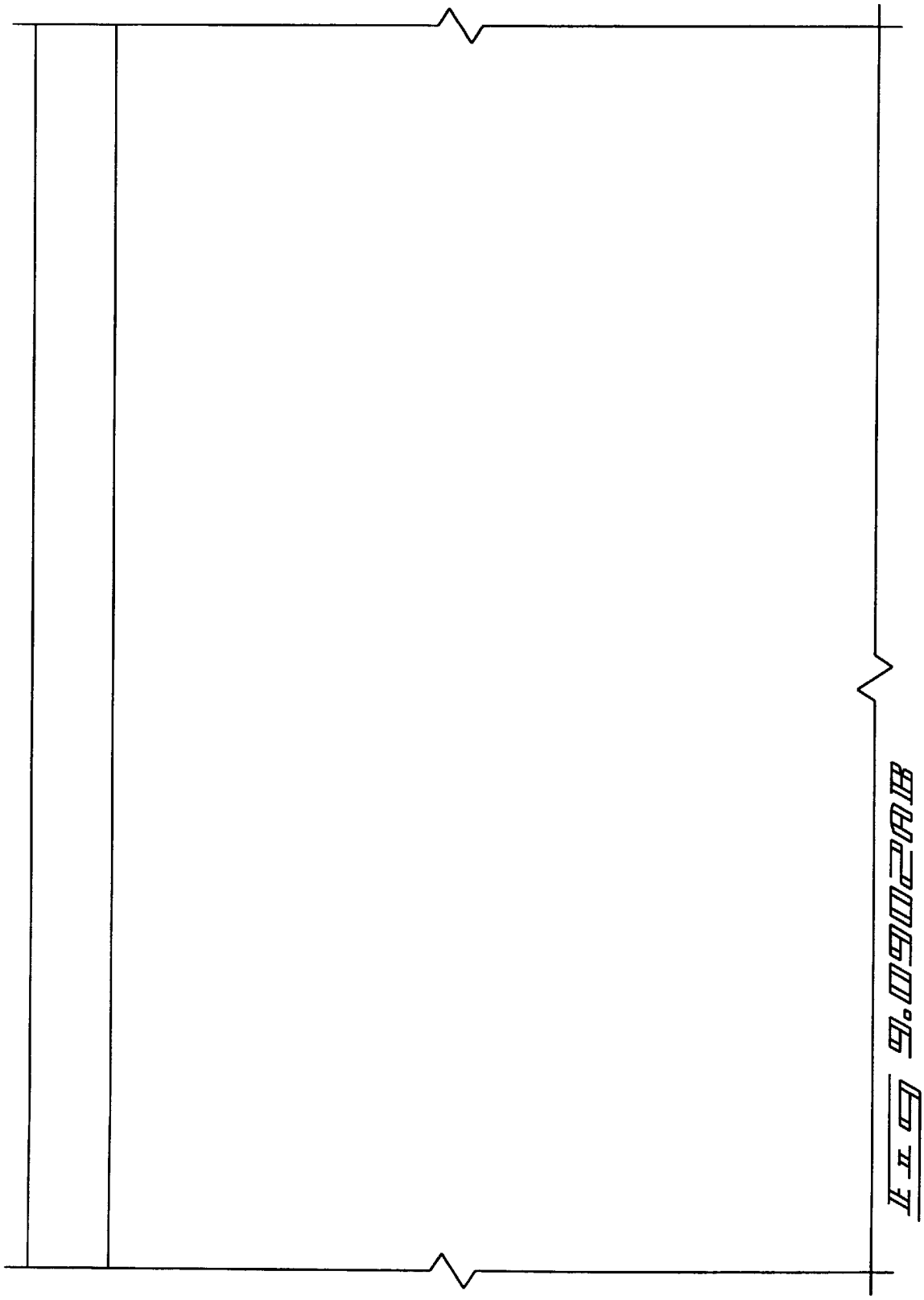


FIG. 6,130,602

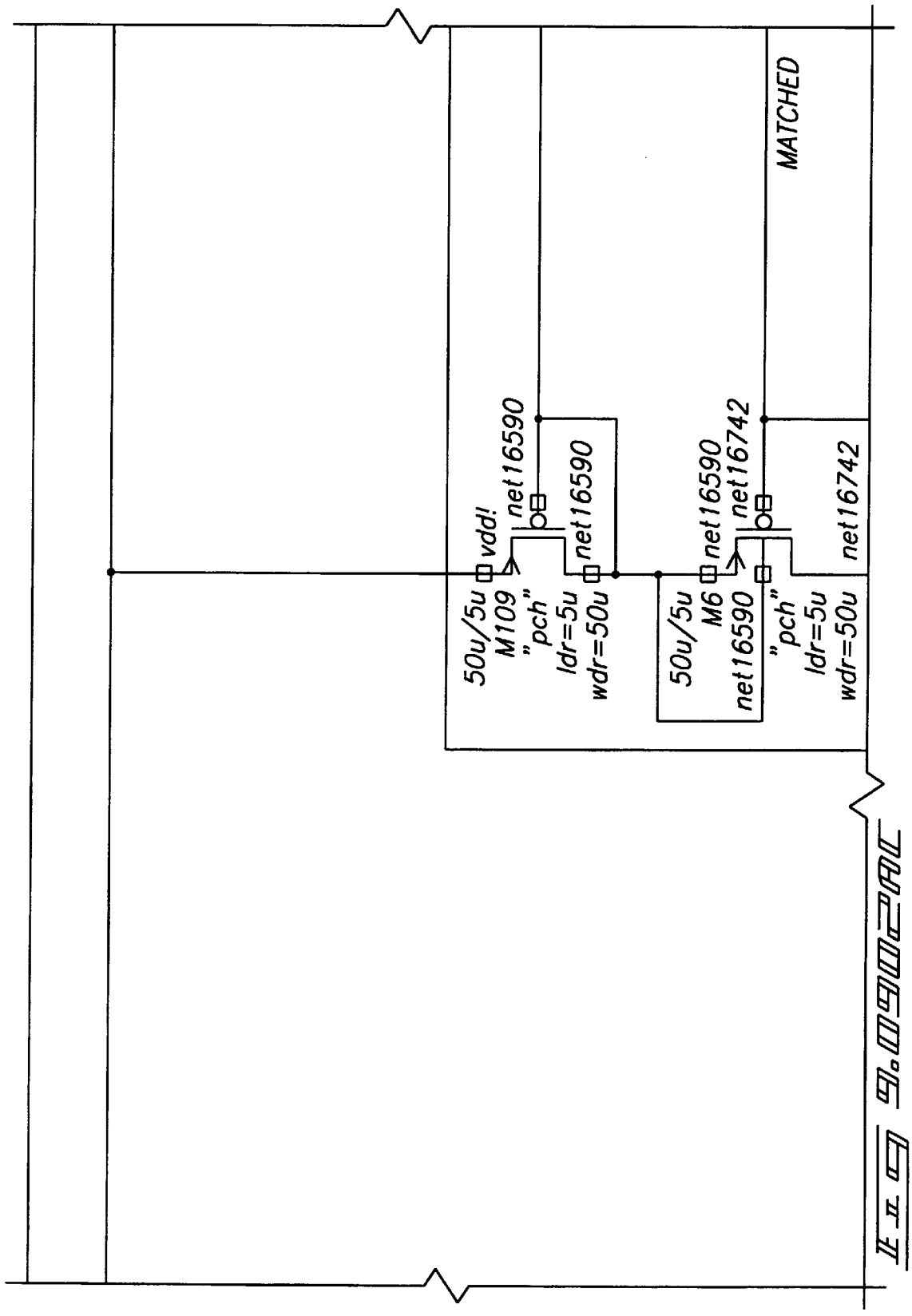

MATCHED
vdd!
net16590
net16590
50u/5u
M109
"pch"
ldr=5u
wdr=50u
net16590
net16742
net16590
50u/5u
M6
"pch"
ldr=5u
wdr=50u
net16742

FIG 6,130,602

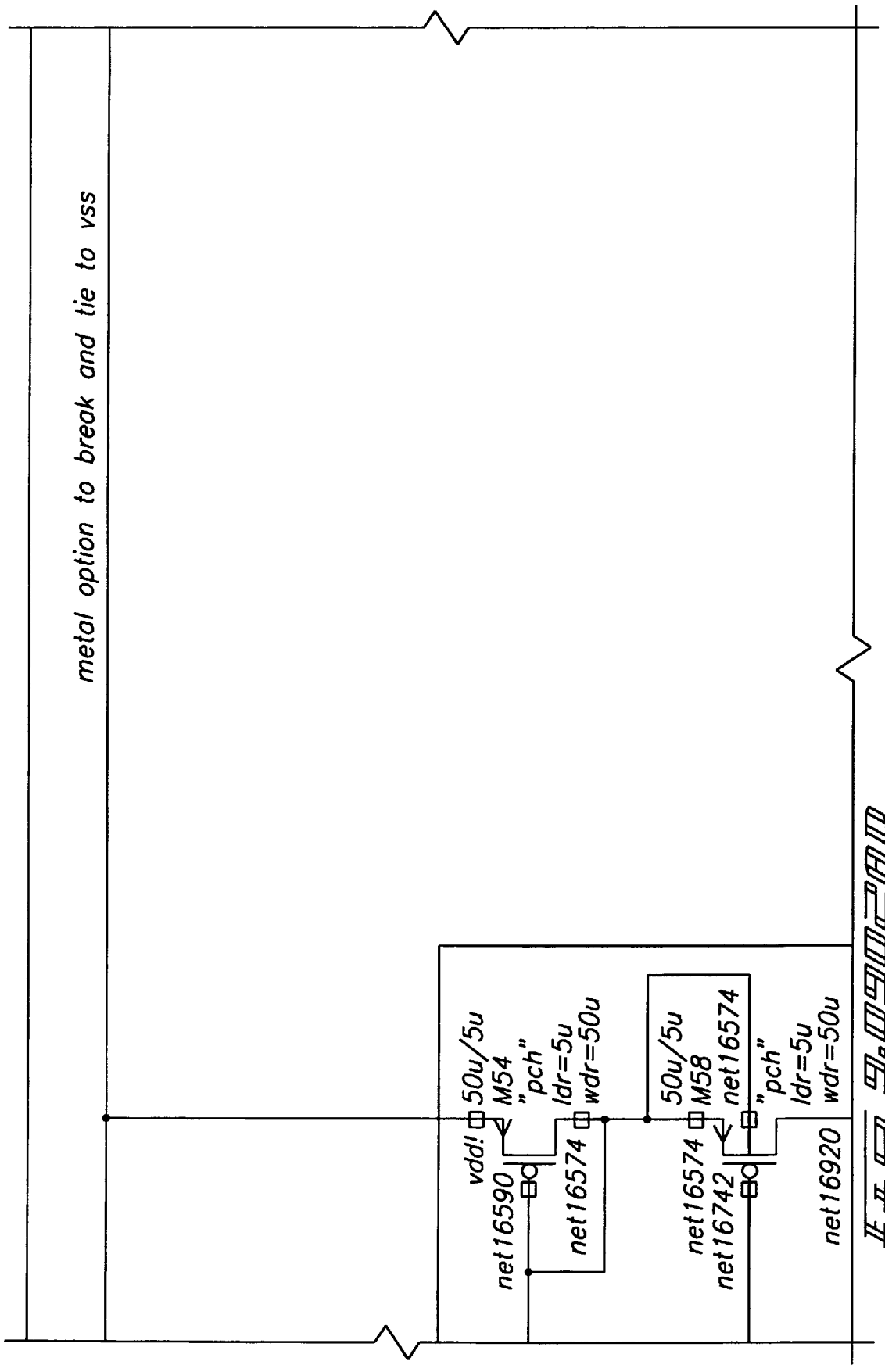

metal option to break and tie to vss
vdd!
net16590
50u/5u
M54
"pch"
ldr=5u
wdr=50u
net16574
net16574
net16742
50u/5u
M58
net16574
"pch"
ldr=5u
wdr=50u
net16920

FIG 9,009,249

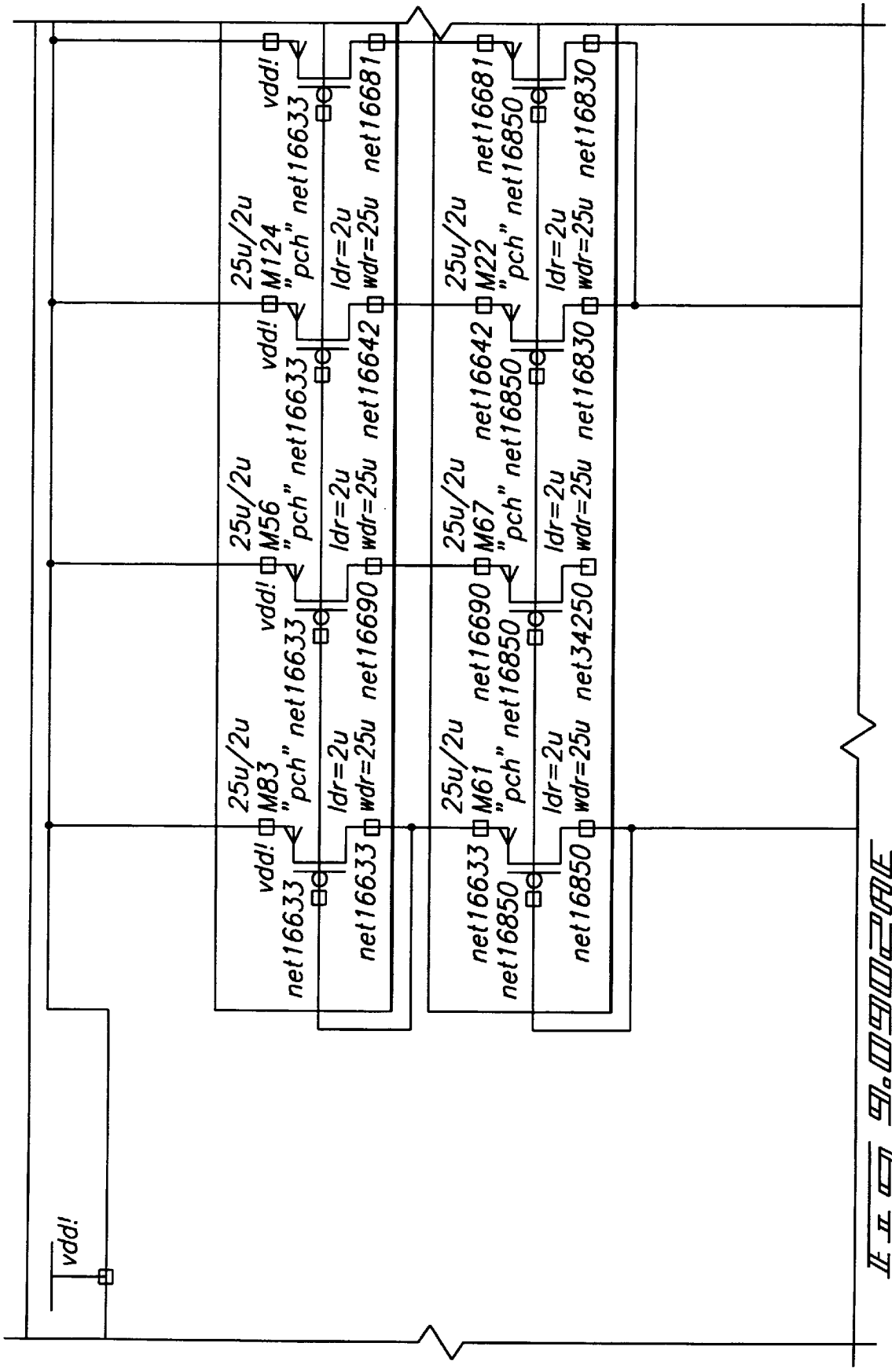

vdd!
net16633
net16850
net16633
net16850
net16633
net16850
net16633
net16850
25u/2u
M83
"pch"
ldr=2u
wdr=25u
net16633
net16690
25u/2u
M61
"pch"
ldr=2u
wdr=25u
net16690
net34250
25u/2u
M56
"pch"
ldr=2u
wdr=25u
net16633
net16642
25u/2u
M67
"pch"
ldr=2u
wdr=25u
net16642
net16830
25u/2u
M124
"pch"
ldr=2u
wdr=25u
net16633
net16681
25u/2u
M22
"pch"
ldr=2u
wdr=25u
net16681
net16830

FIG 9.0002AE

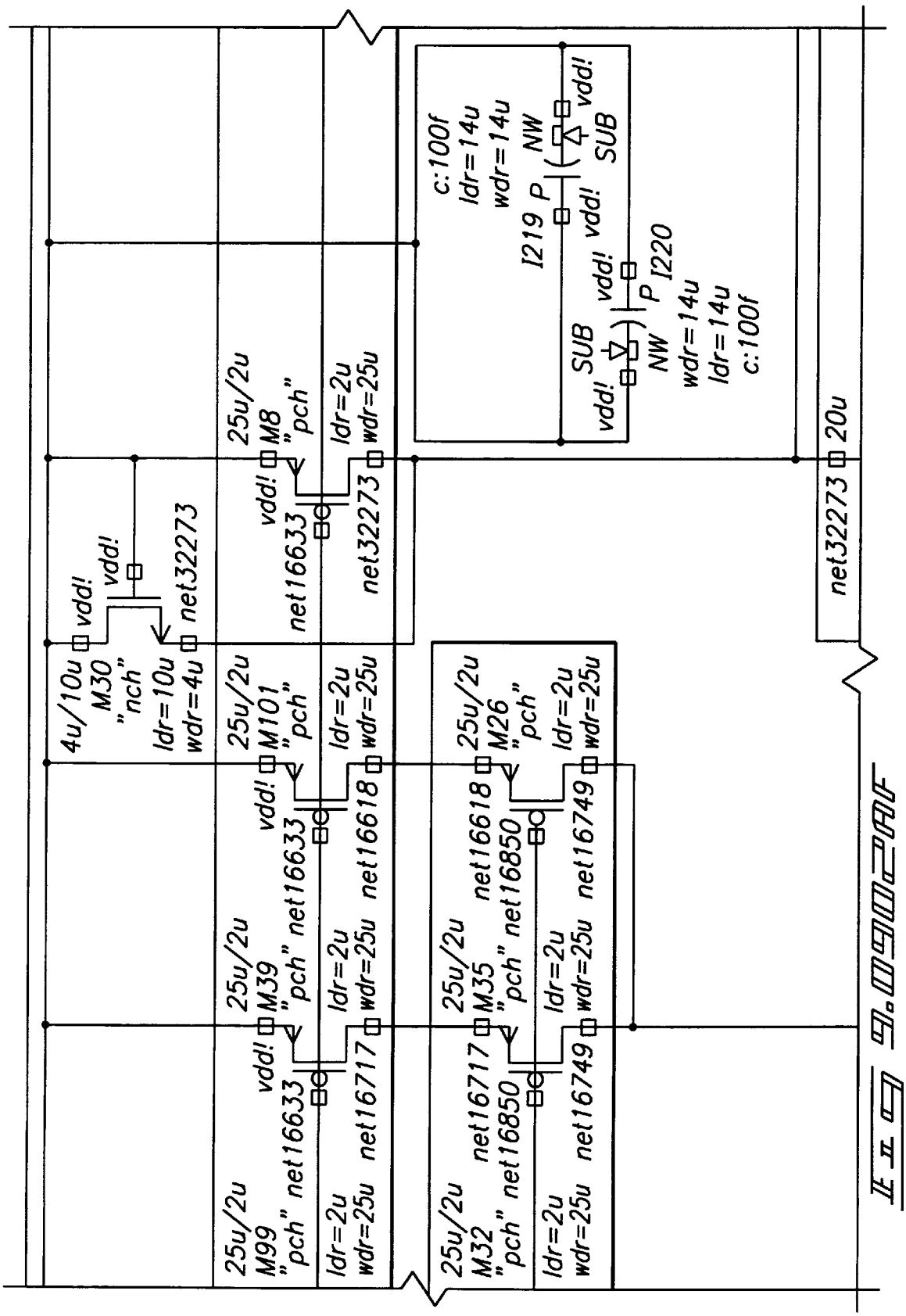
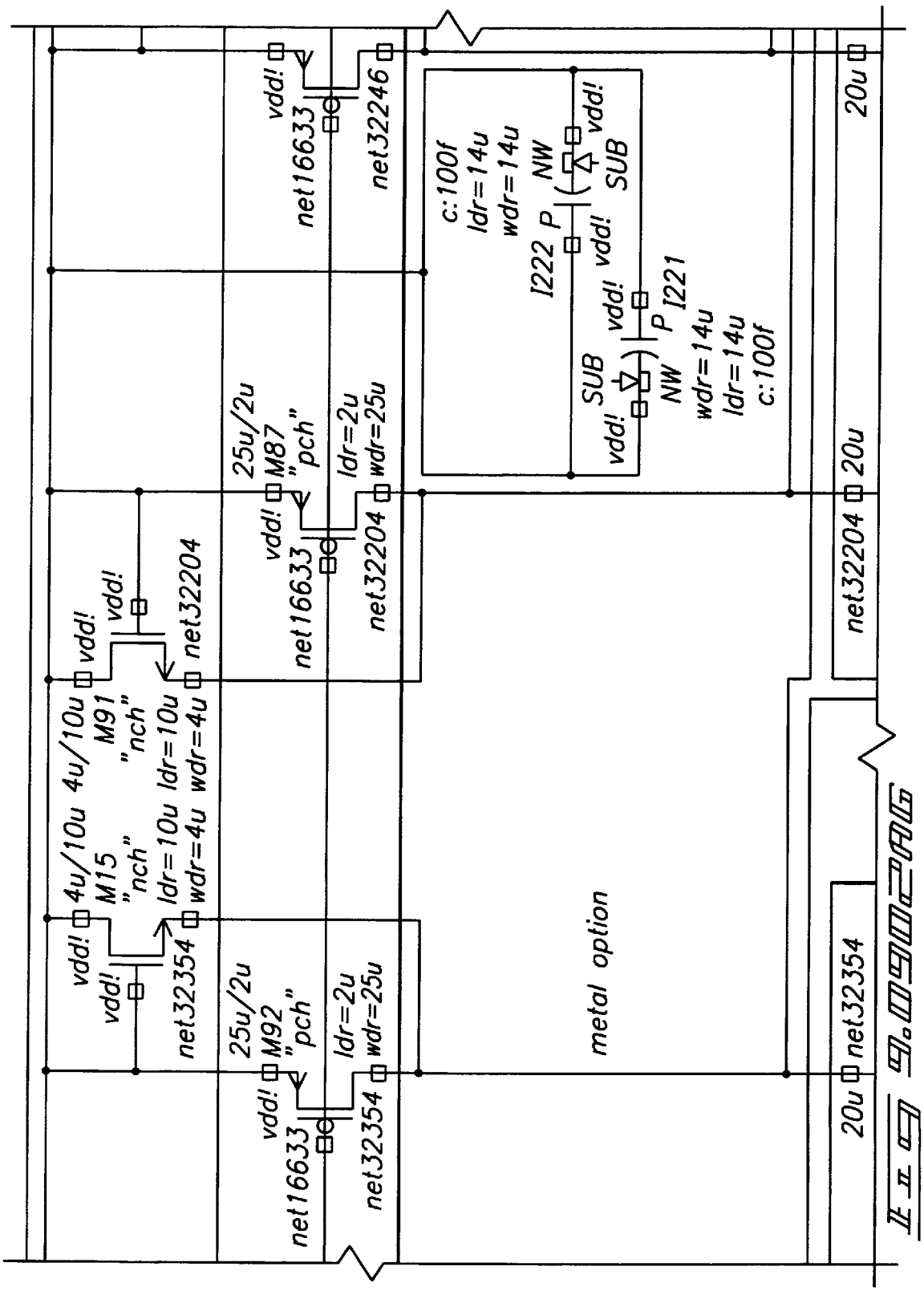

4u/10u
M30
"nch"
ldr=10u
wdr=4u
vdd!
net32273
25u/2u
M8
"pch"
ldr=2u
wdr=25u
net16633
net32273
25u/2u
M101
"pch"
ldr=2u
wdr=25u
net16618
25u/2u
M26
"pch"
ldr=2u
wdr=25u
net16749
25u/2u
M39
"pch"
ldr=2u
wdr=25u
net16717
25u/2u
M35
"pch"
ldr=2u
wdr=25u
net16850
25u/2u
M99
"pch"
ldr=2u
wdr=25u
25u/2u
M32
"pch"
ldr=2u
wdr=25u
c:100f
ldr=14u
wdr=14u
I219 P
NW
SUB
vdd!
I220
20u

Fig. 9.0902AF


vdd!
net16633
net32246
c:100f
ldr=14u
wdr=14u
I222 P
NW
SUB
vdd!
vdd!
SUB
NW
P I221
wdr=14u
ldr=14u
c:100f
20u
25u/2u
M87
"pch"
ldr=2u
wdr=25u
net32204
4u/10u
M91
"nch"
ldr=10u
wdr=4u
net32354
M15
M92
metal option
20u
net32354

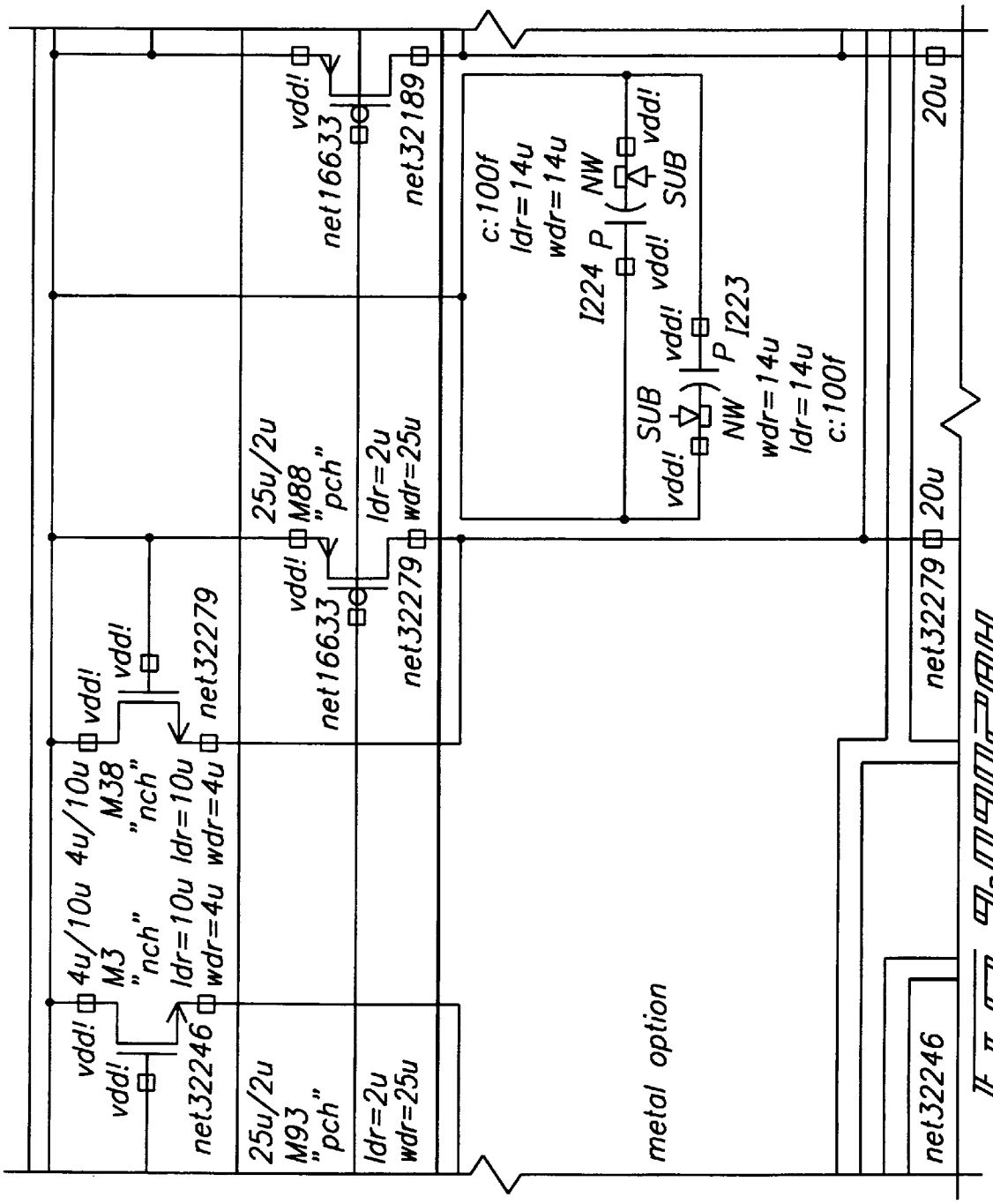

vdd!
net16633
net32189
c:100f
ldr=14u
wdr=14u
I224 P
NW
SUB
vdd!
vdd!
SUB
NW
P I223
wdr=14u
ldr=14u
c:100f
20u
25u/2u
M88
"pch"
ldr=2u
wdr=25u
net16633
net32279
net32279
20u
vdd!
vdd!
4u/10u
M38
"nch"
ldr=10u
wdr=4u
net32279
vdd!
vdd!
4u/10u
M3
"nch"
ldr=10u
wdr=4u
net32246
25u/2u
M93
"pch"
ldr=2u
wdr=25u
metal option
net32246

FIG 9.0000AH

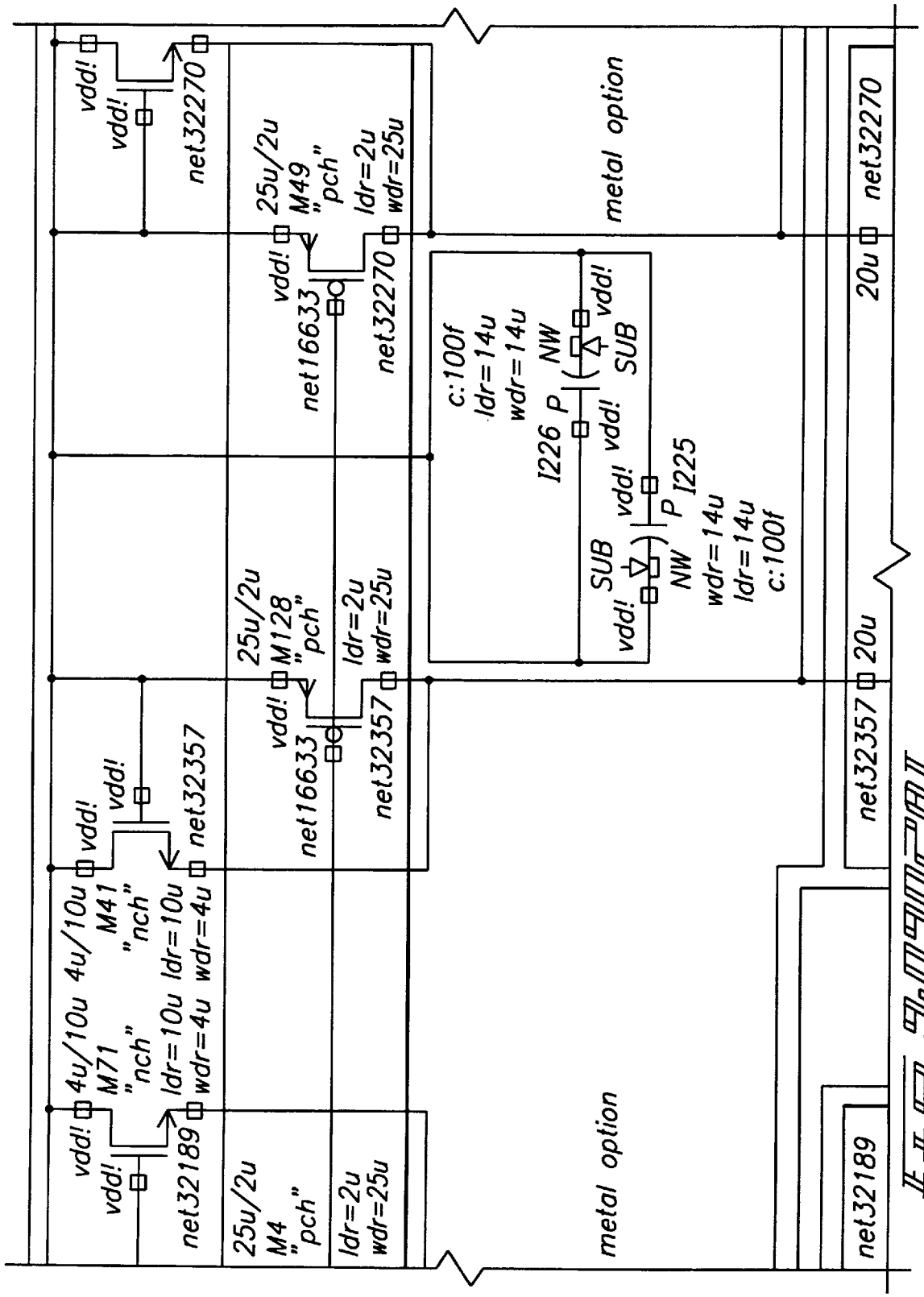

vdd!
vdd!
net32270
25u/2u
M49
"pch"
ldr=2u
wdr=25u
metal option
net16633
net32270
c:100f
ldr=14u
wdr=14u
I226 P
NW
SUB
vdd!
vdd!
P I225
wdr=14u
ldr=14u
c:100f
20u
net32270
4u/10u
M41
"nch"
ldr=10u
wdr=4u
net32357
25u/2u
M128
"pch"
ldr=2u
wdr=25u
net32357
20u
4u/10u
M71
"nch"
ldr=10u
wdr=4u
net32189
25u/2u
M4
"pch"
ldr=2u
wdr=25u
metal option
net32189

Fig. 9,009,AII

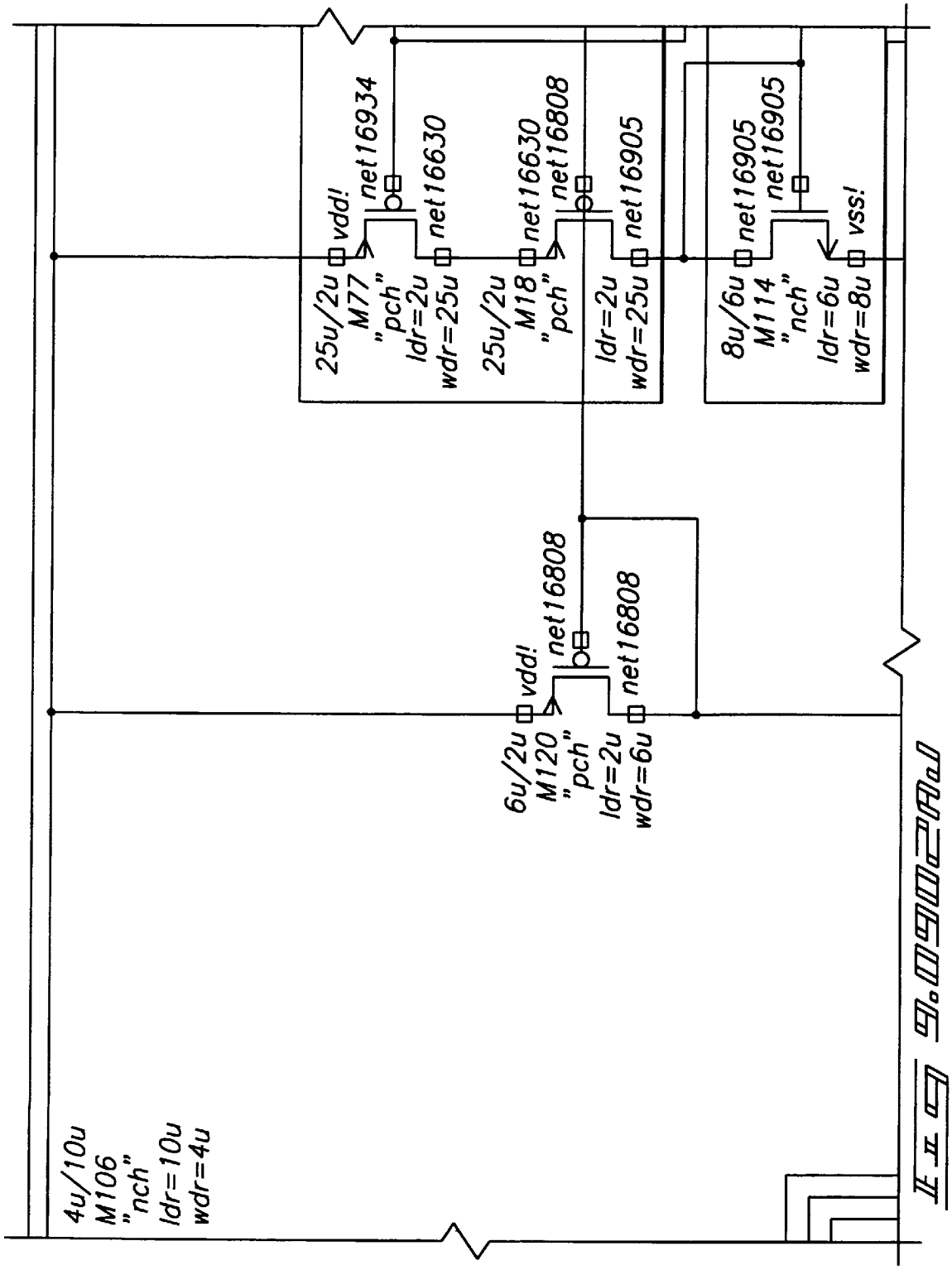

25u/2u
M77
"pch"
ldr=2u
wdr=25u
vdd!
net16934
net16630
25u/2u
M18
"pch"
ldr=2u
wdr=25u
net16630
net16808
net16905
8u/6u
M114
"nch"
ldr=6u
wdr=8u
net16905
net16905
vss!
6u/2u
M120
"pch"
ldr=2u
wdr=6u
vdd!
net16808
net16808
4u/10u
M106
"nch"
ldr=10u
wdr=4u

Fig. 6,130,602

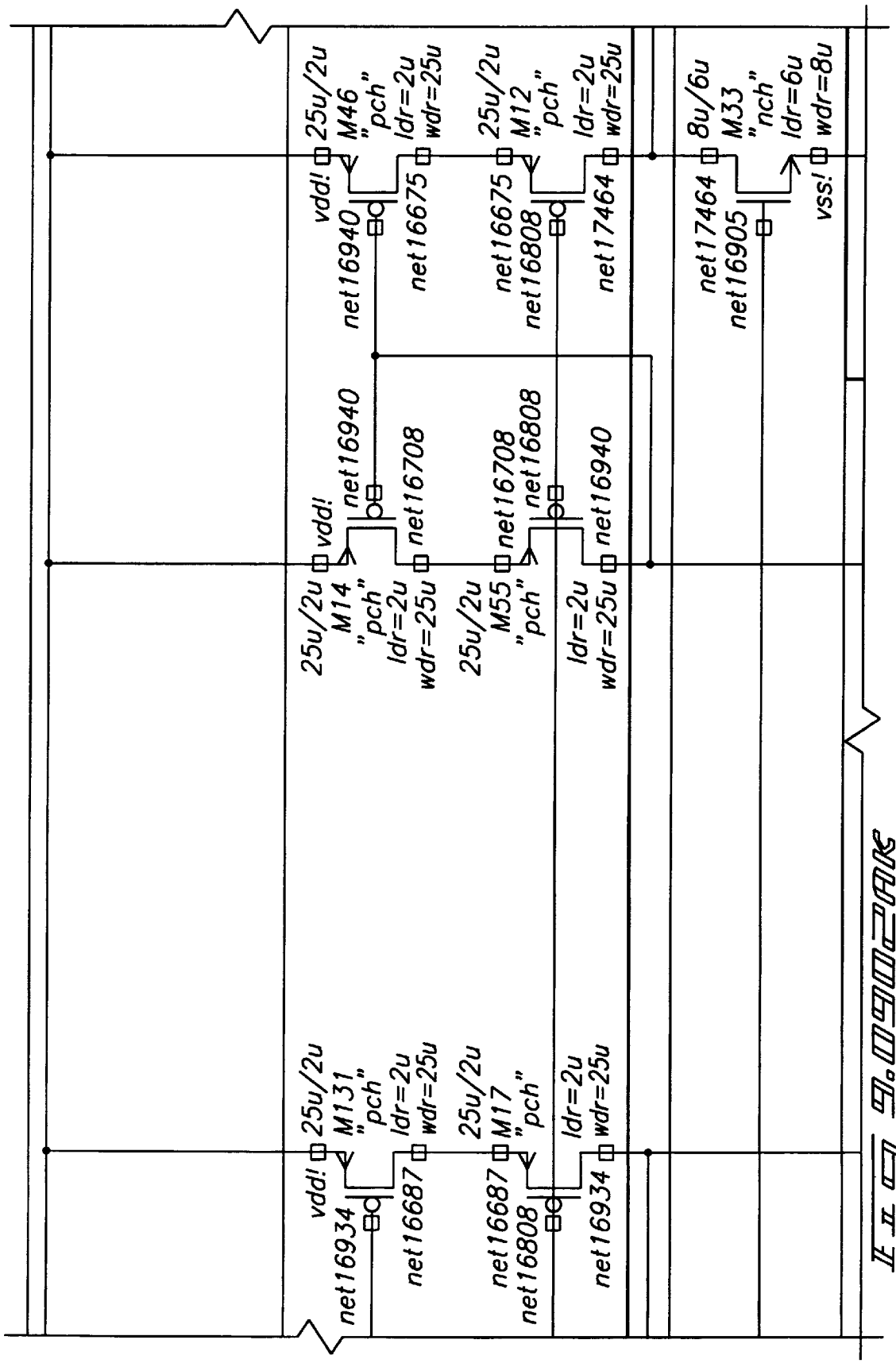
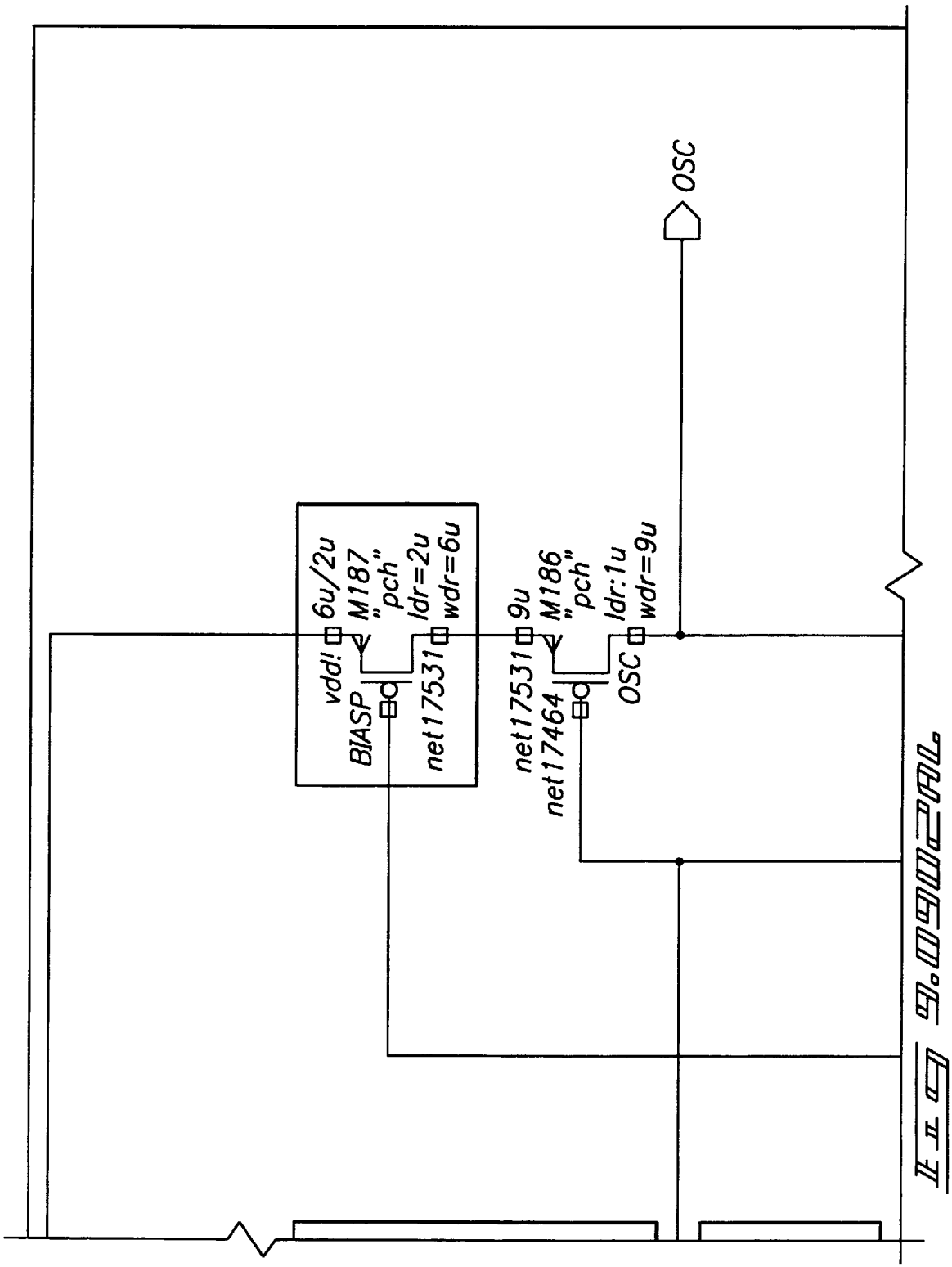

25u/2u
M46
"pch"
ldr=2u
wdr=25u
vdd!
net16940
net16675
25u/2u
M12
"pch"
ldr=2u
wdr=25u
net16675
net16808
net17464
8u/6u
M33
"nch"
ldr=6u
wdr=8u
net17464
net16905
vss!
25u/2u
M14
"pch"
ldr=2u
wdr=25u
vdd!
net16940
net16708
25u/2u
M55
"pch"
ldr=2u
wdr=25u
net16708
net16808
net16940
25u/2u
M131
"pch"
ldr=2u
wdr=25u
vdd!
net16934
net16687
25u/2u
M17
"pch"
ldr=2u
wdr=25u
net16687
net16808
net16934

FIG 9.0906AK


OSC
6u/2u
M187
"pch"
ldr=2u
wdr=6u
vdd!
BIASP
net17531
9u
M186
"pch"
ldr:1u
wdr=9u
net17531
net17464
OSC
FIG 9,090,291

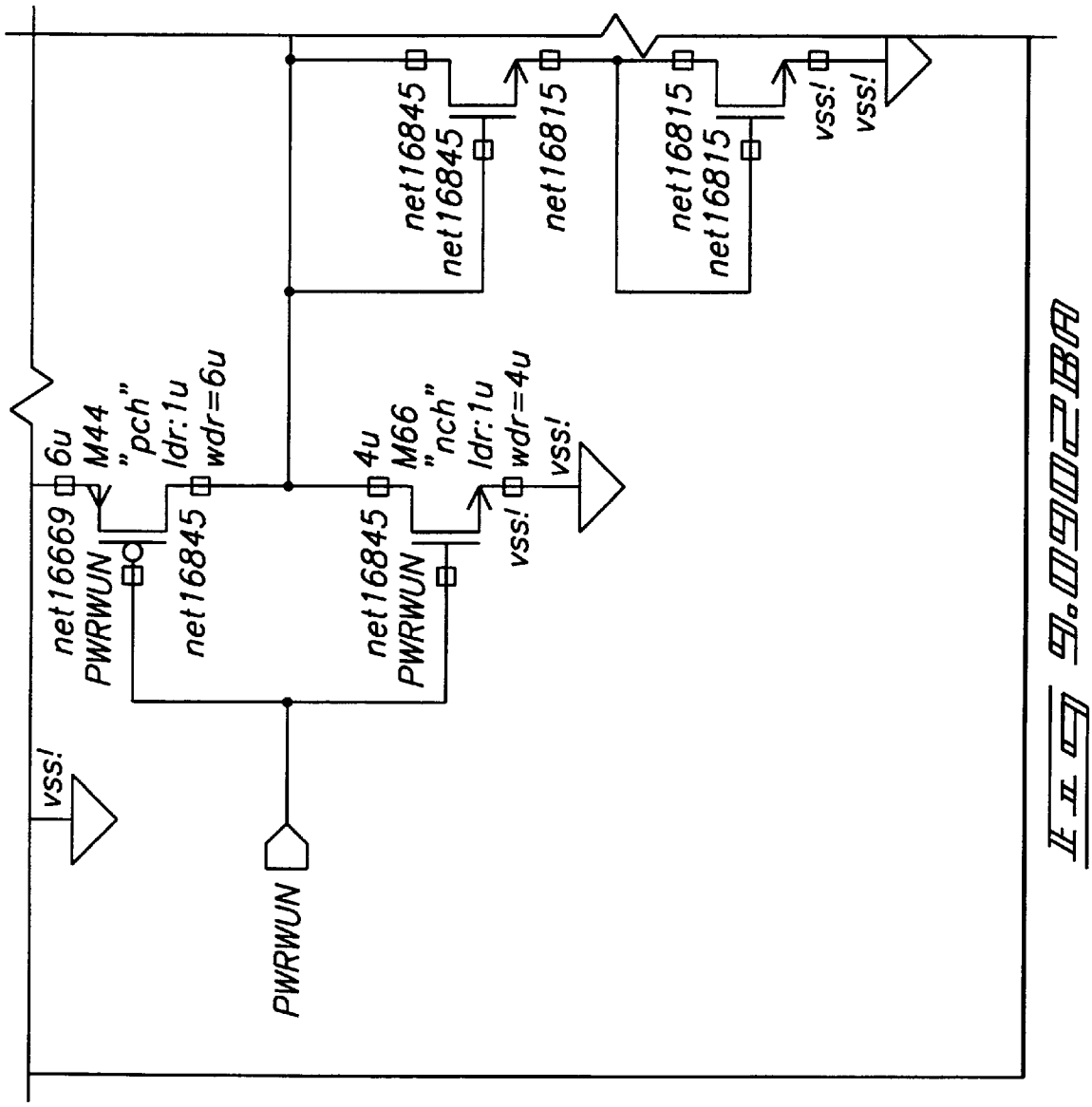


FIG 9,009,218A

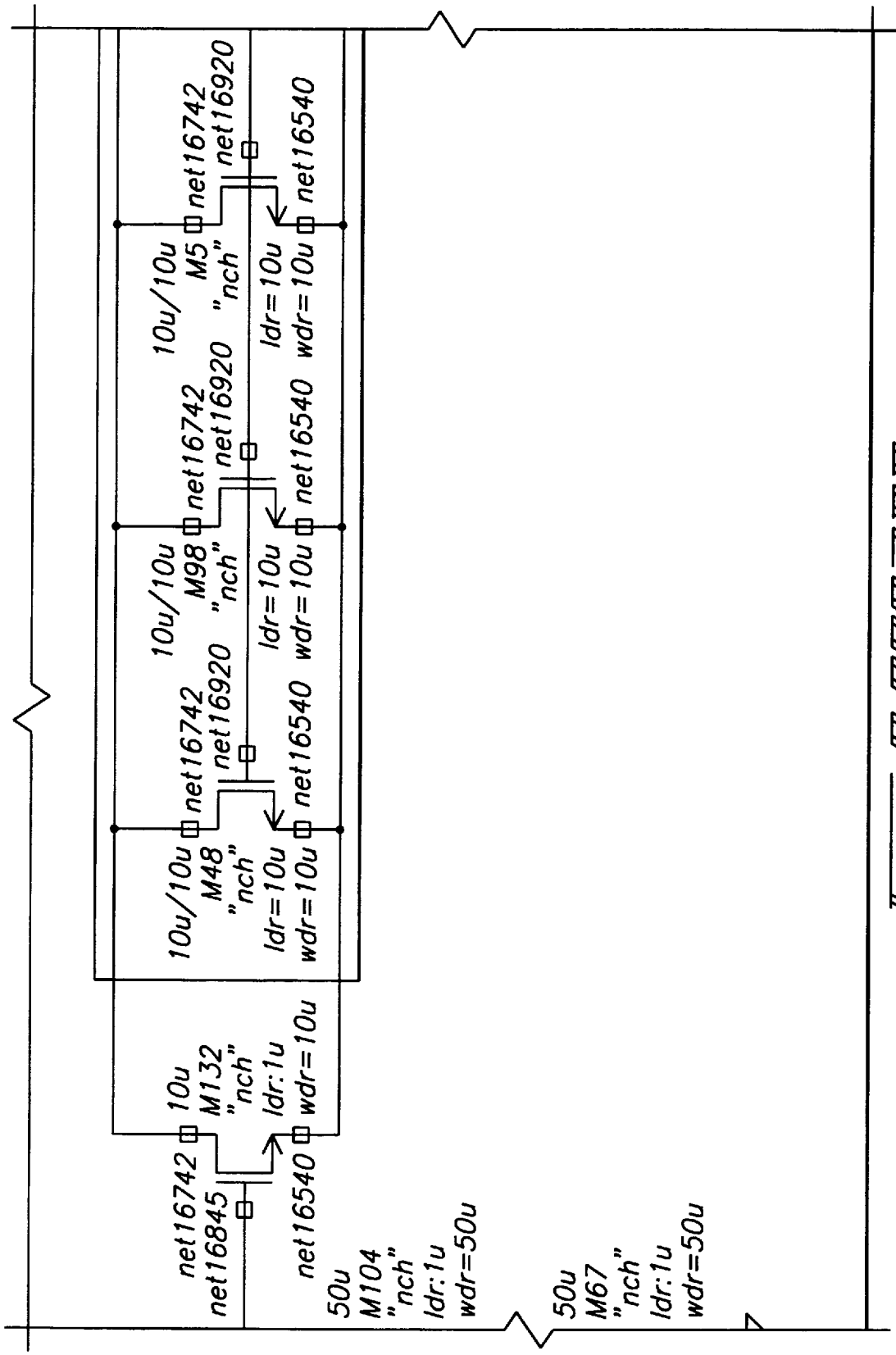

net16742
net16845
10u
M132
"nch"
ldr:1u
wdr=10u
net16540
50u
M104
"nch"
ldr:1u
wdr=50u
50u
M67
"nch"
ldr:1u
wdr=50u
10u/10u
M48
"nch"
ldr=10u
wdr=10u
net16742
net16920
10u/10u
M98
"nch"
ldr=10u
wdr=10u
net16540
net16742
net16920
10u/10u
M5
"nch"
ldr=10u
wdr=10u
net16540

FIG 6,130,602

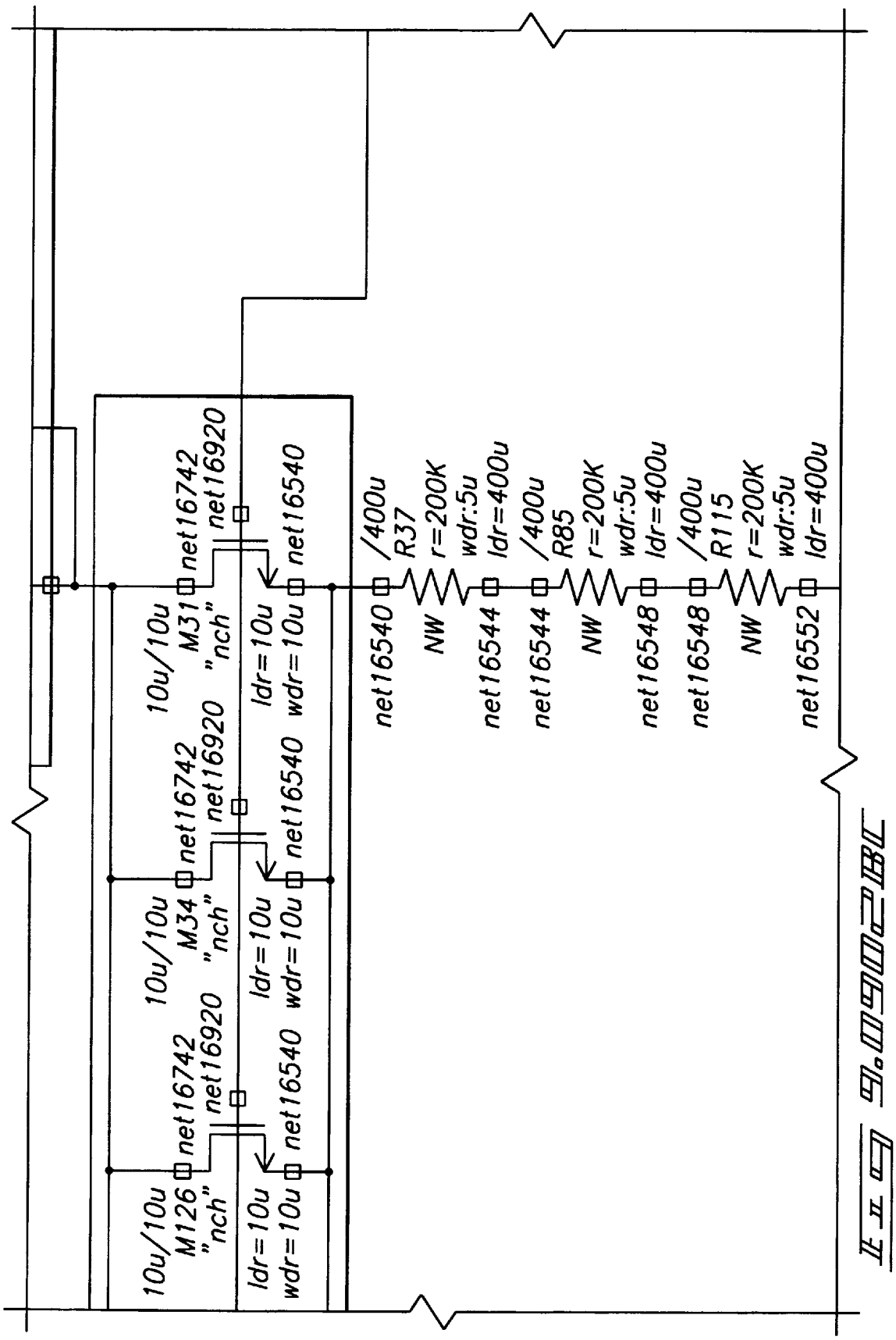
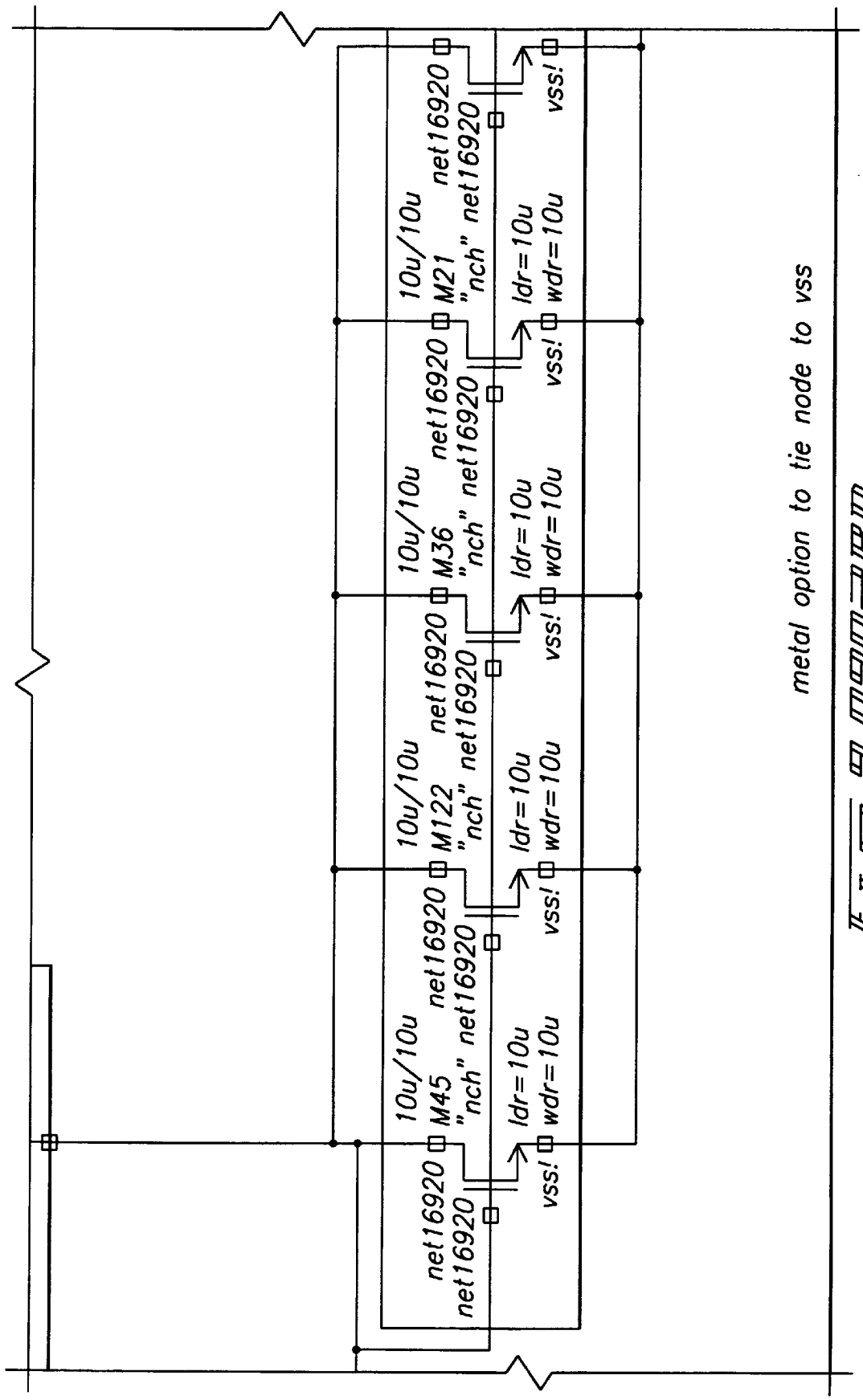

net16540
/400u
R37
r=200K
wdr:5u
ldr=400u
net16544
/400u
R85
r=200K
wdr:5u
ldr=400u
net16548
/400u
R115
r=200K
wdr:5u
ldr=400u
net16552
NW
net16742
net16920
10u/10u
M31
"nch"
ldr=10u
wdr=10u
net16540
net16742
net16920
10u/10u
M34
"nch"
ldr=10u
wdr=10u
net16540
net16742
net16920
10u/10u
M126
"nch"
ldr=10u
wdr=10u
net16540

FIG 6,130,602


metal option to tie node to vss
10u/10u
M45
"nch"
net16920
net16920
ldr=10u
wdr=10u
vss!
10u/10u
M122
"nch"
net16920
net16920
ldr=10u
wdr=10u
vss!
10u/10u
M36
"nch"
net16920
net16920
ldr=10u
wdr=10u
vss!
10u/10u
M21
"nch"
net16920
net16920
ldr=10u
wdr=10u
vss!

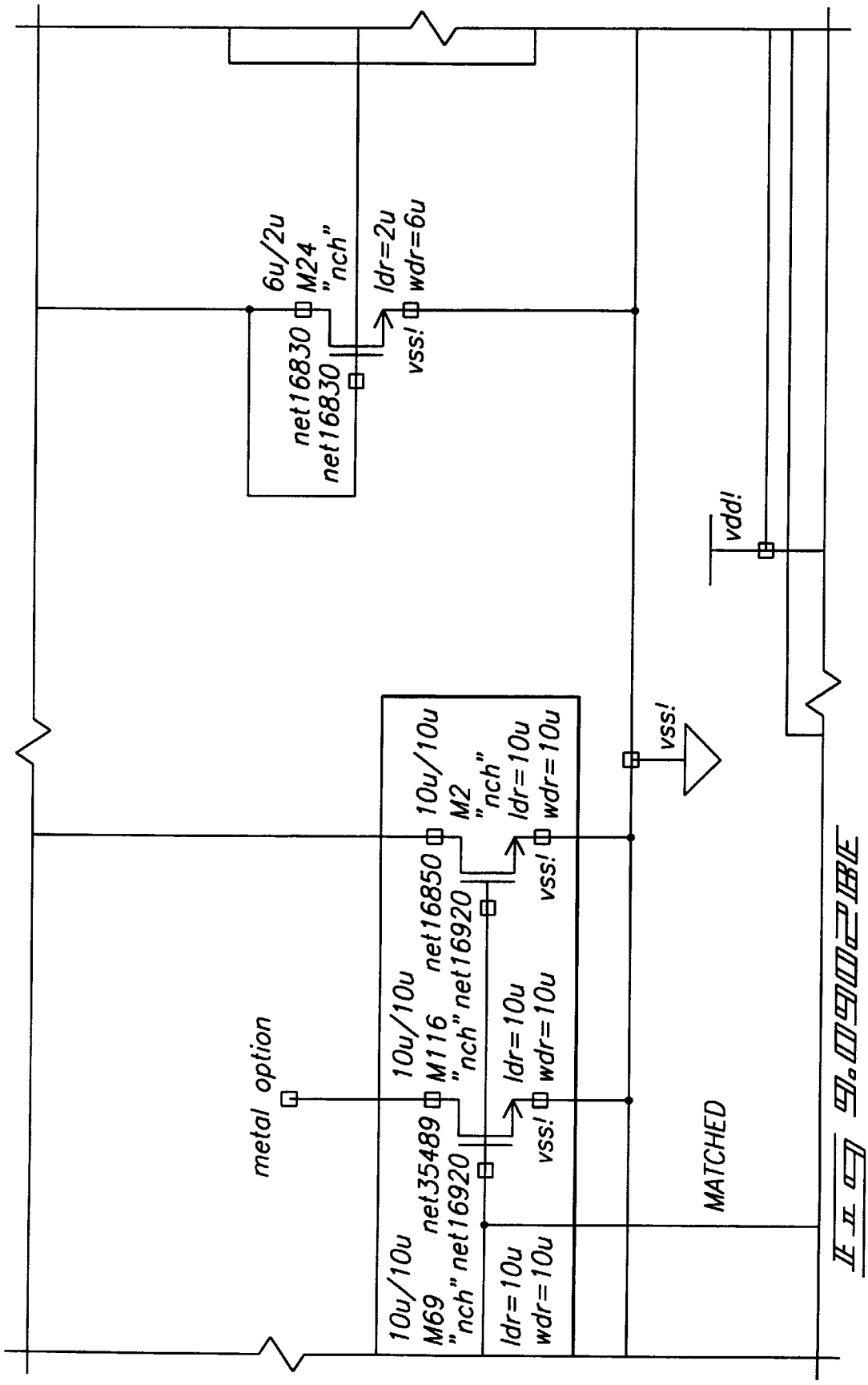
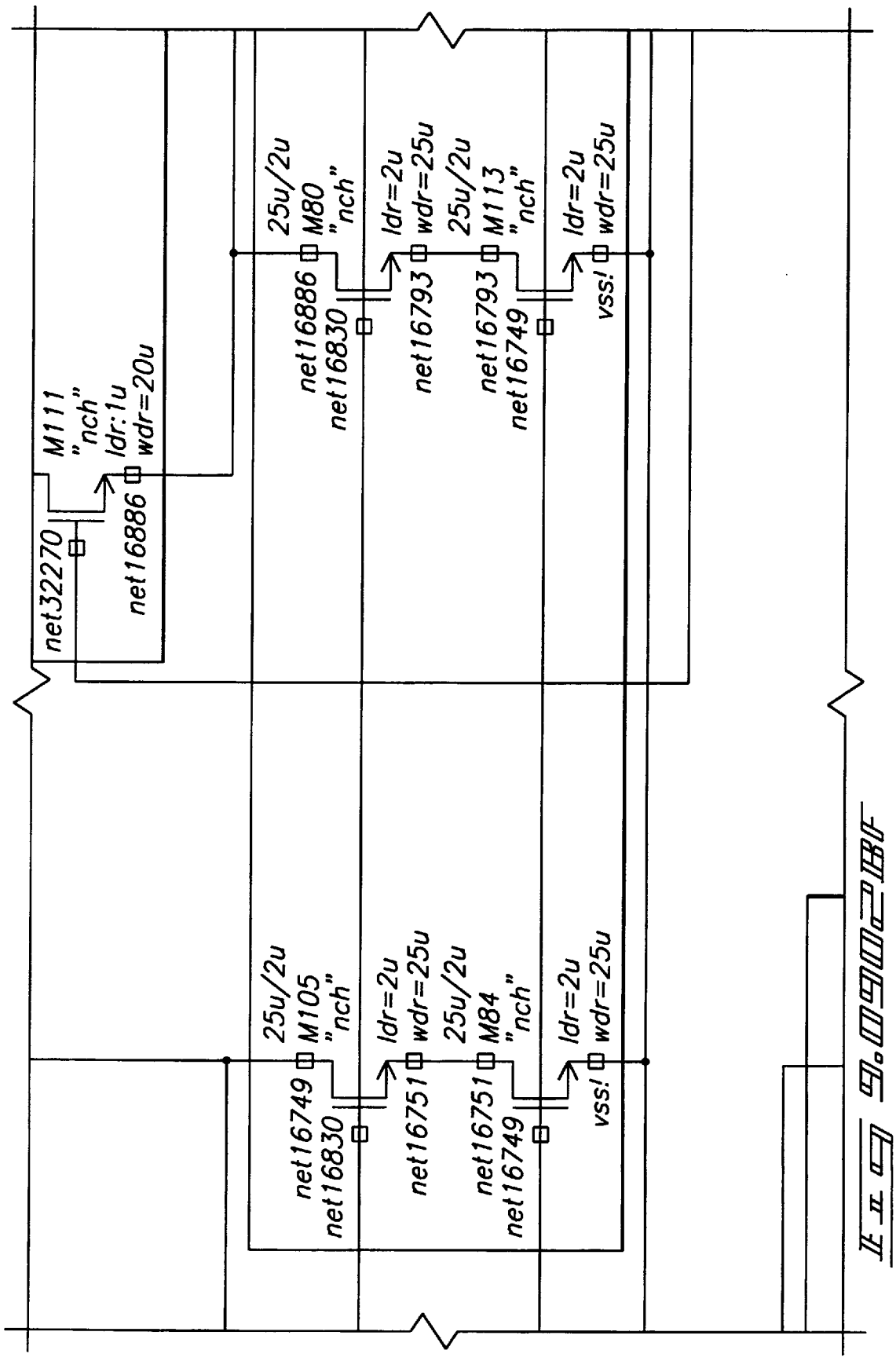

6u/2u
M24
"nch"
ldr=2u
wdr=6u
net16830
net16830
vss!
vdd!
vss!
10u/10u
M2
"nch"
ldr=10u
wdr=10u
net16850
net16920
vss!
metal option
10u/10u
M116
"nch"
net16920
ldr=10u
wdr=10u
net35489
vss!
MATCHED
10u/10u
M69
"nch"
net16920
ldr=10u
wdr=10u

FIG 69


M111
"nch"
ldr:1u
wdr=20u
net32270
net16886
25u/2u
M80
"nch"
ldr=2u
wdr=25u
net16886
net16830
net16793
25u/2u
M113
"nch"
ldr=2u
wdr=25u
net16793
net16749
vss!
25u/2u
M105
"nch"
ldr=2u
wdr=25u
net16749
net16830
net16751
25u/2u
M84
"nch"
ldr=2u
wdr=25u
net16751
net16749
vss!

Фиг. 6,130,602

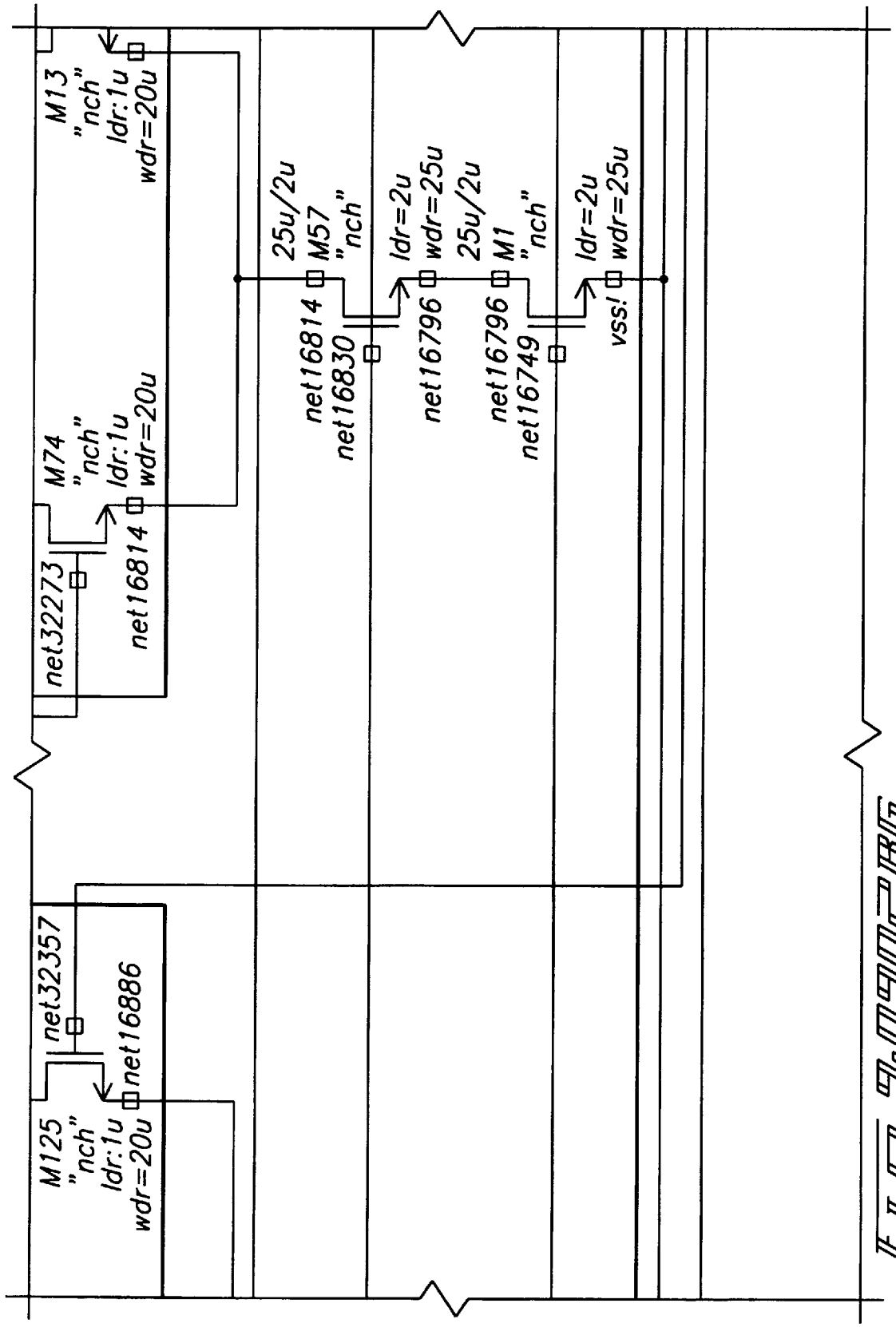
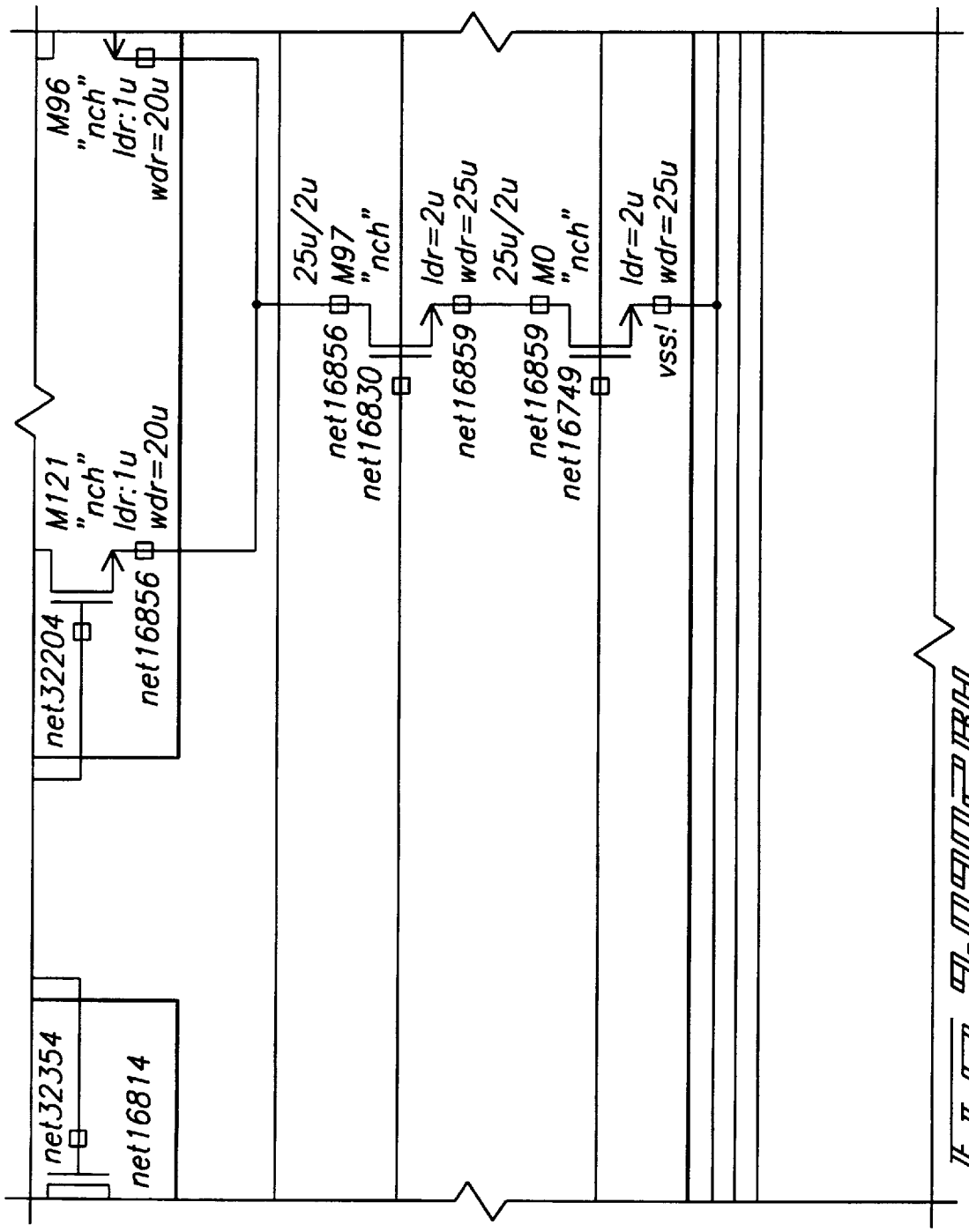

M13
"nch"
ldr:1u
wdr=20u
M74
"nch"
ldr:1u
wdr=20u
net32273
net16814
M125
"nch"
ldr:1u
wdr=20u
net32357
net16886
25u/2u
M57
"nch"
net16814
net16830
ldr=2u
wdr=25u
net16796
25u/2u
M1
"nch"
net16796
net16749
ldr=2u
wdr=25u
vss!

FIG 9.090286


net32354
net16814
net32204
net16856
M121
"nch"
ldr:1u
wdr=20u
M96
"nch"
ldr:1u
wdr=20u
net16856
net16830
25u/2u
M97
"nch"
ldr=2u
wdr=25u
net16859
net16749
25u/2u
M0
"nch"
ldr=2u
wdr=25u
vss!

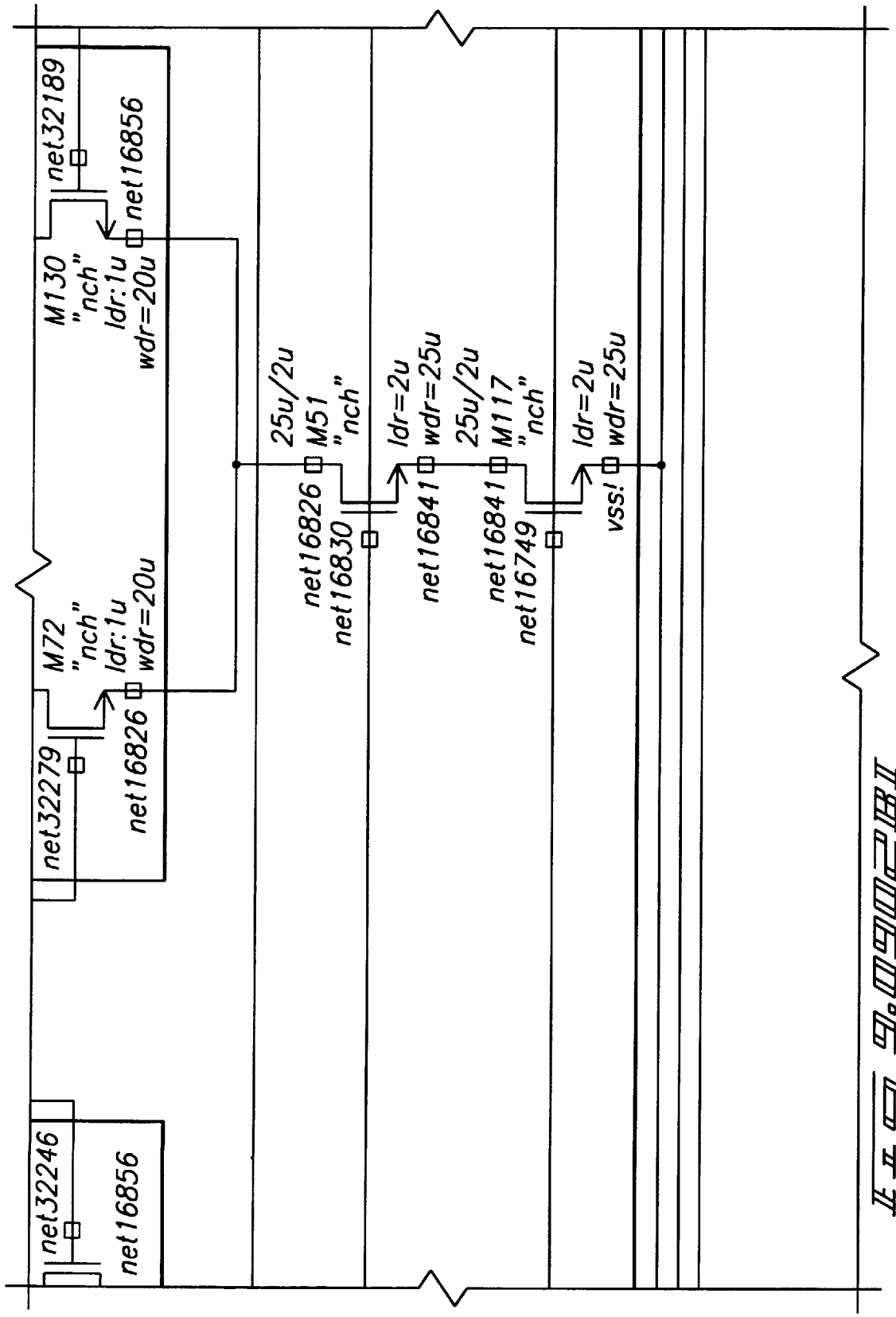
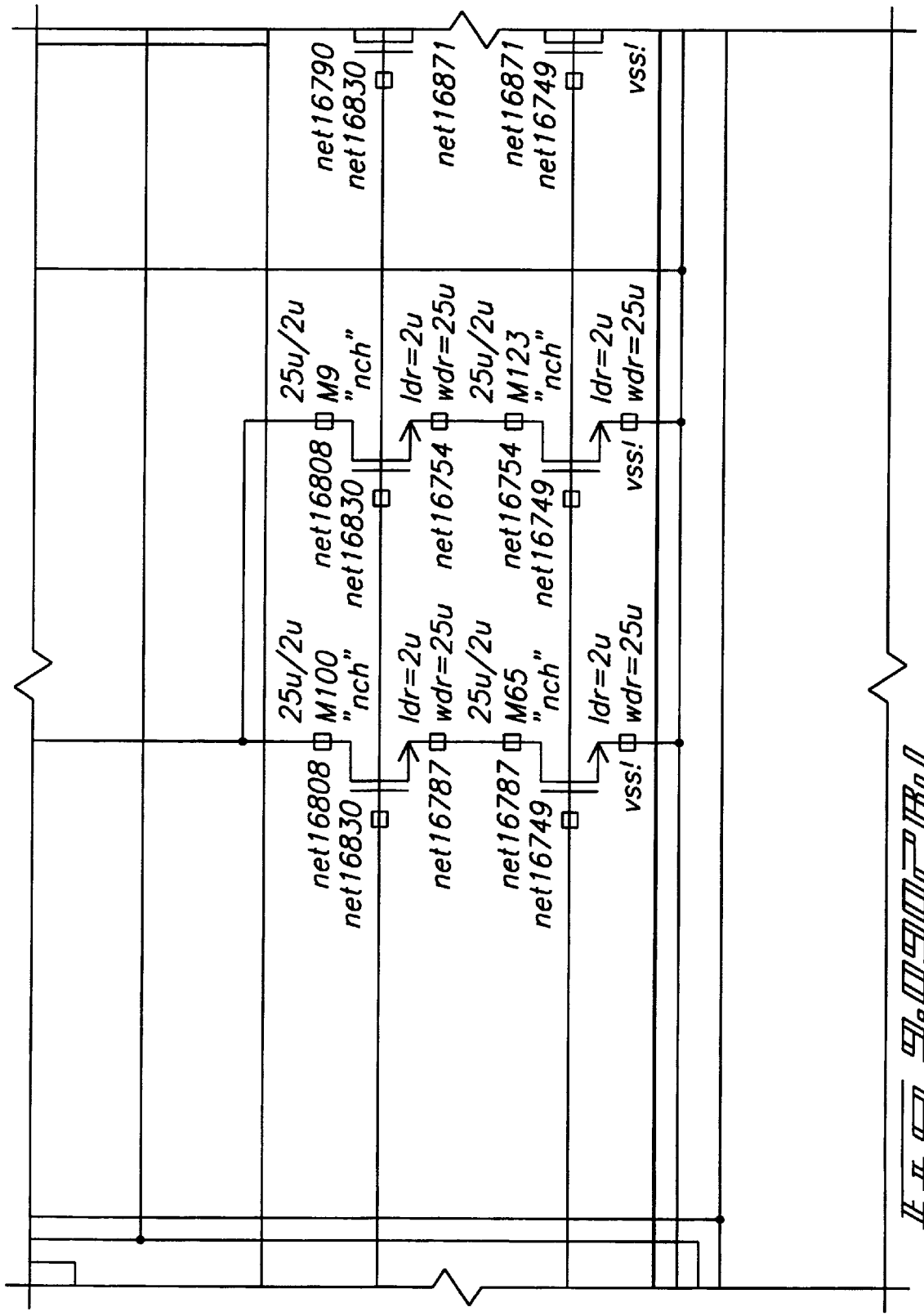

net32189
net16856
M130
"nch"
ldr:1u
wdr=20u
25u/2u
M51
"nch"
ldr=2u
wdr=25u
25u/2u
M117
"nch"
ldr=2u
wdr=25u
M72
"nch"
ldr:1u
wdr=20u
net16826
net16830
net16841
net16841
net16749
vss!
net32279
net16826
net32246
net16856

FIG 6,130,602


net16790
net16830
net16871
net16871
net16749
vss!
25u/2u
M9
"nch"
ldr=2u
wdr=25u
25u/2u
M123
"nch"
ldr=2u
wdr=25u
net16808
net16830
net16754
net16754
net16749
vss!
25u/2u
M100
"nch"
ldr=2u
wdr=25u
25u/2u
M65
"nch"
ldr=2u
wdr=25u
net16808
net16830
net16787
net16787
net16749
vss!
FIG 6,050,728

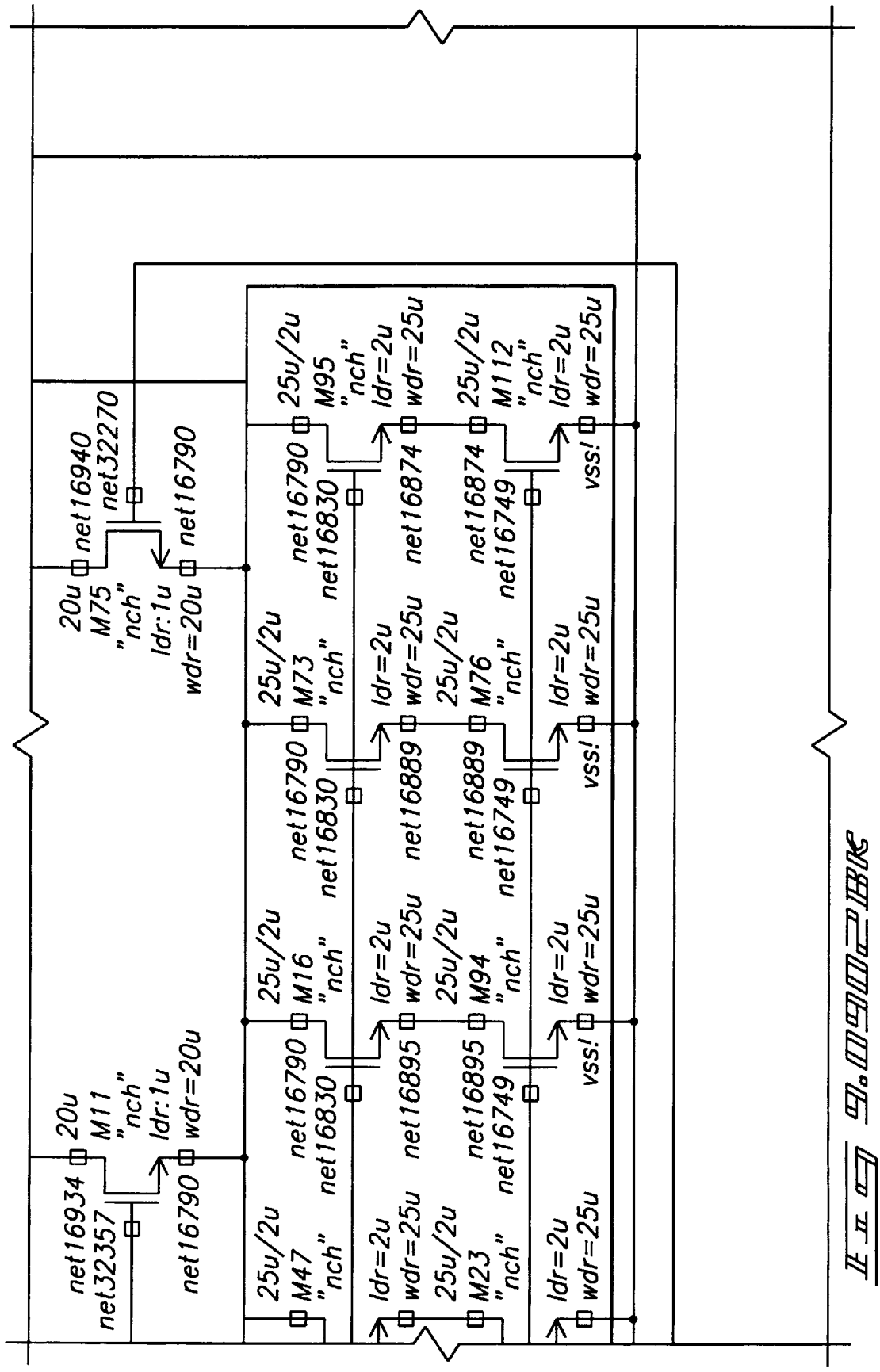

net16940
net32270
net16790
20u
M75
"nch"
ldr:1u
wdr=20u
25u/2u
M95
"nch"
ldr=2u
wdr=25u
M112
M73
M76
net16790
net16830
net16874
net16749
net16889
vss!
M16
M94
net16895
net32357
net16934
M11
M47
M23

FIG. 6,130,602

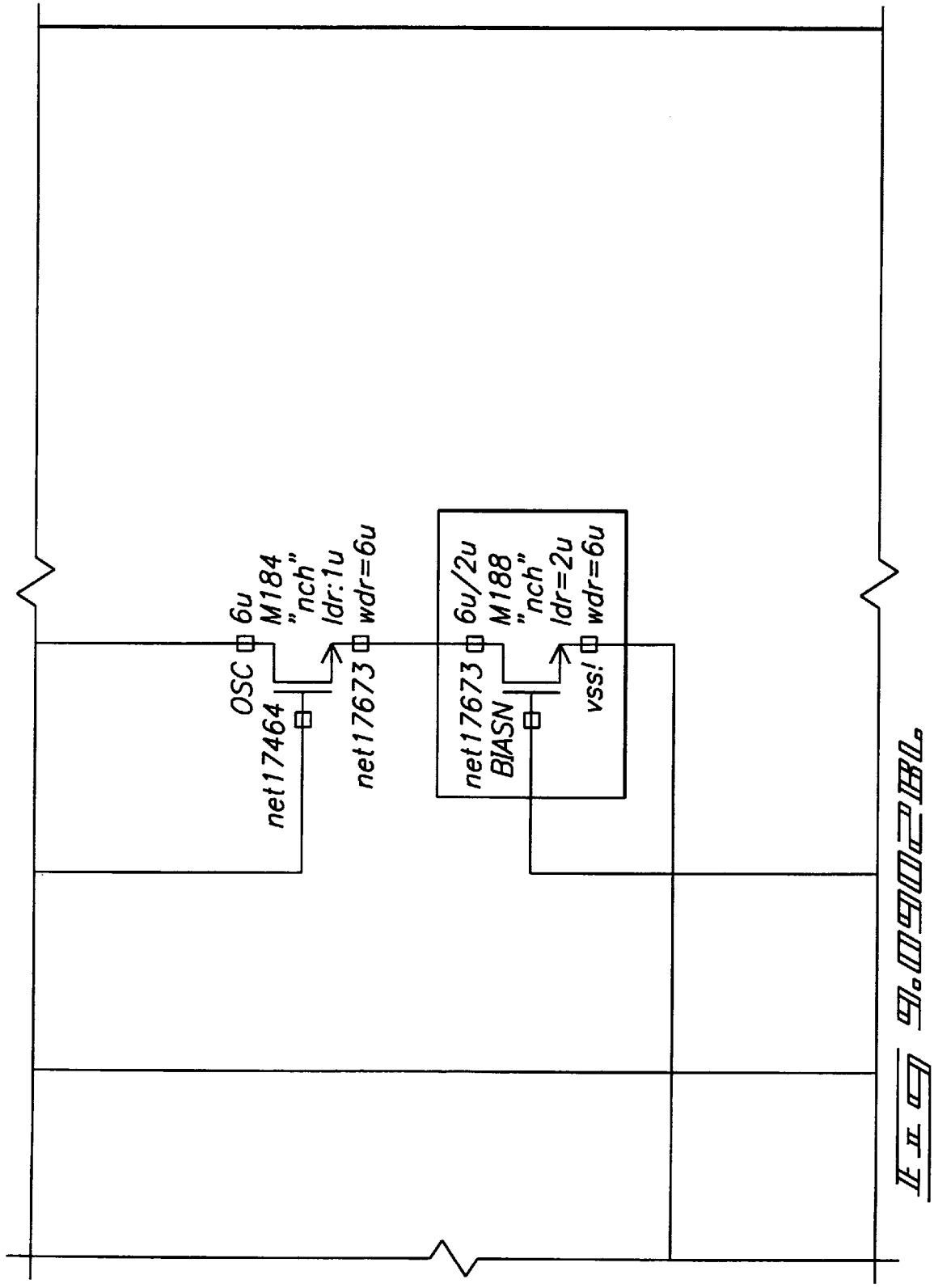


FIG 9,090,218L

net16652
/400u
R107
r=200K
wdr:5u
ldr=400u
NW
net16564
net16564
/400u
R102
r=200K
wdr:5u
ldr=400u
NW
net16560
net16560
/400u
R90
r=200K
wdr:5u
ldr=400u
NW
net16558
net16558
/400u
R27
r=200K
wdr:5u
ldr=400u
NW
net16542
net16542
/400u
R20
r=200K
wdr:5u
ldr=400u
NW
net16562
net16562
/400u
R103
r=200K
wdr:5u
ldr=400u
NW
net16568
net16568
/400u
R82
r=200K
wdr:5u
ldr=400u
NW
vss!
vss!
/400u
R43
r=200K
wdr:5u
ldr=400u
NW
net16550
metal option

Fig. 6,130,602

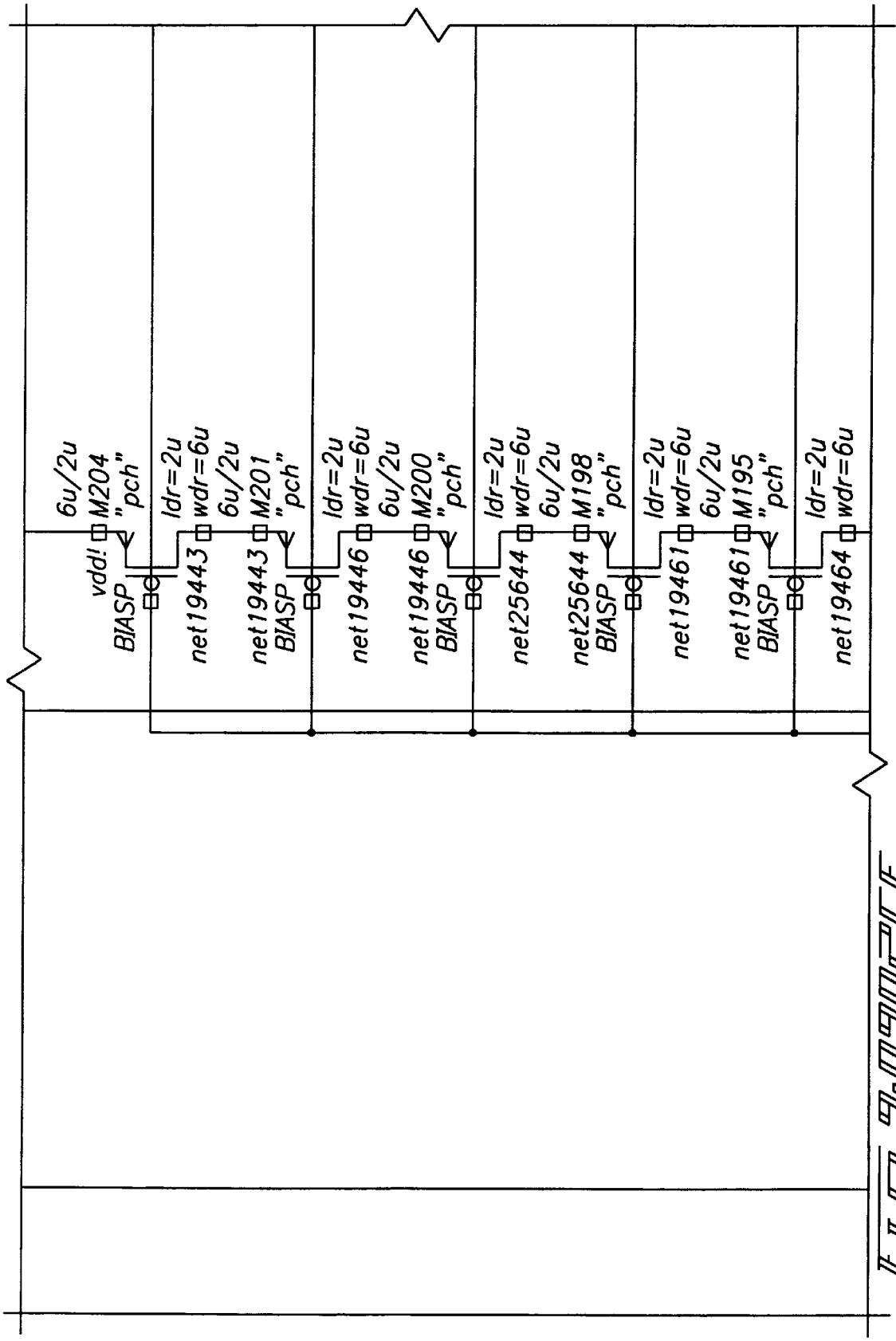
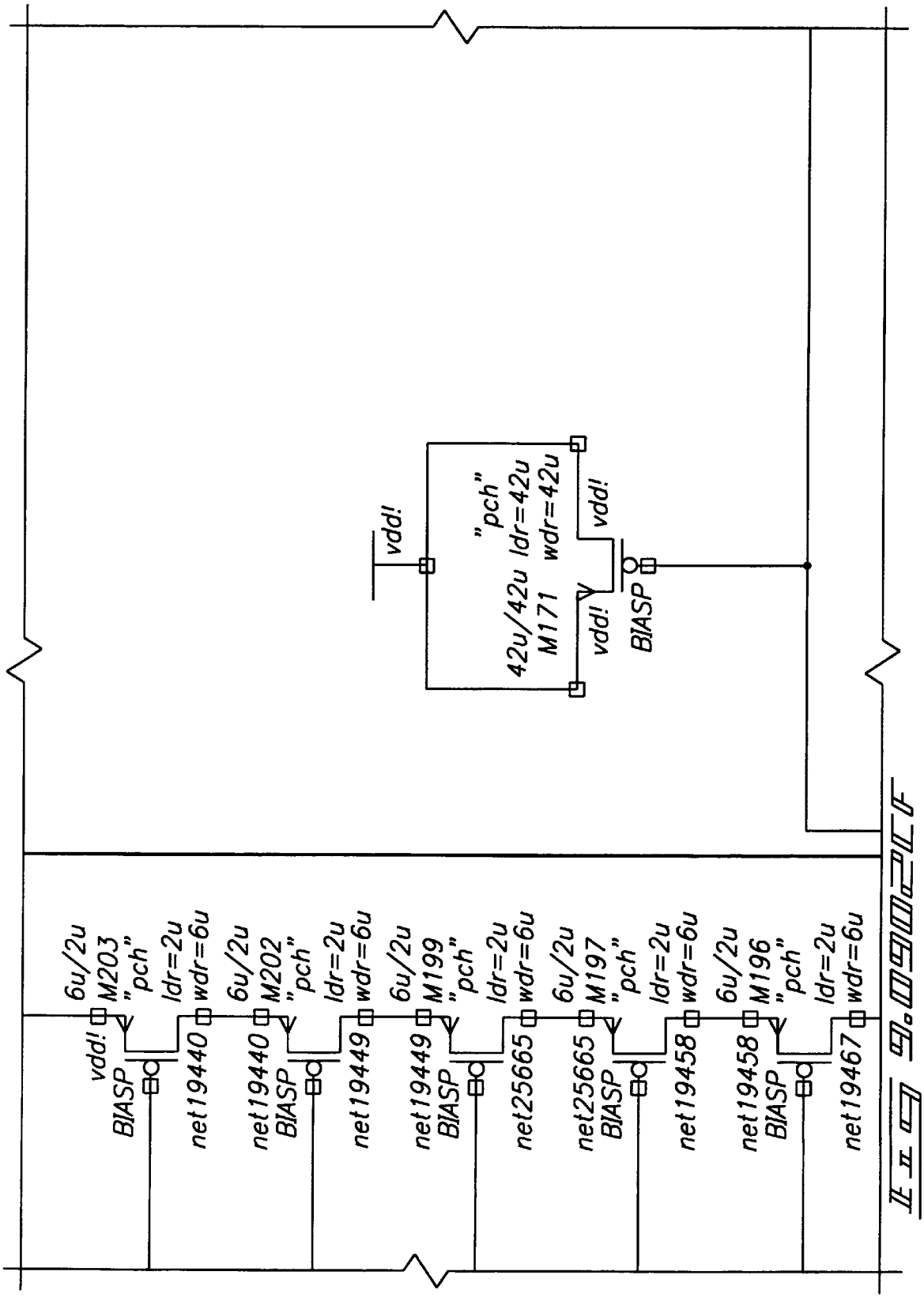

6u/2u
M204
"pch"
vdd!
BIASP
ldr=2u
wdr=6u
net19443
6u/2u
M201
"pch"
net19443
BIASP
ldr=2u
wdr=6u
net19446
6u/2u
M200
"pch"
net19446
BIASP
ldr=2u
wdr=6u
net25644
6u/2u
M198
"pch"
net25644
BIASP
ldr=2u
wdr=6u
net19461
6u/2u
M195
"pch"
net19461
BIASP
ldr=2u
wdr=6u
net19464

FIG 9,000,E


vdd!
"pch"
42u/42u ldr=42u
M171 wdr=42u
vdd!
vdd!
BIASP
6u/2u
M203
"pch"
ldr=2u
wdr=6u
vdd!
BIASP
net19440
6u/2u
M202
"pch"
ldr=2u
wdr=6u
net19440
BIASP
net19449
6u/2u
M199
"pch"
ldr=2u
wdr=6u
net19449
BIASP
net25665
6u/2u
M197
"pch"
ldr=2u
wdr=6u
net25665
BIASP
net19458
6u/2u
M196
"pch"
ldr=2u
wdr=6u
net19458
BIASP
net19467

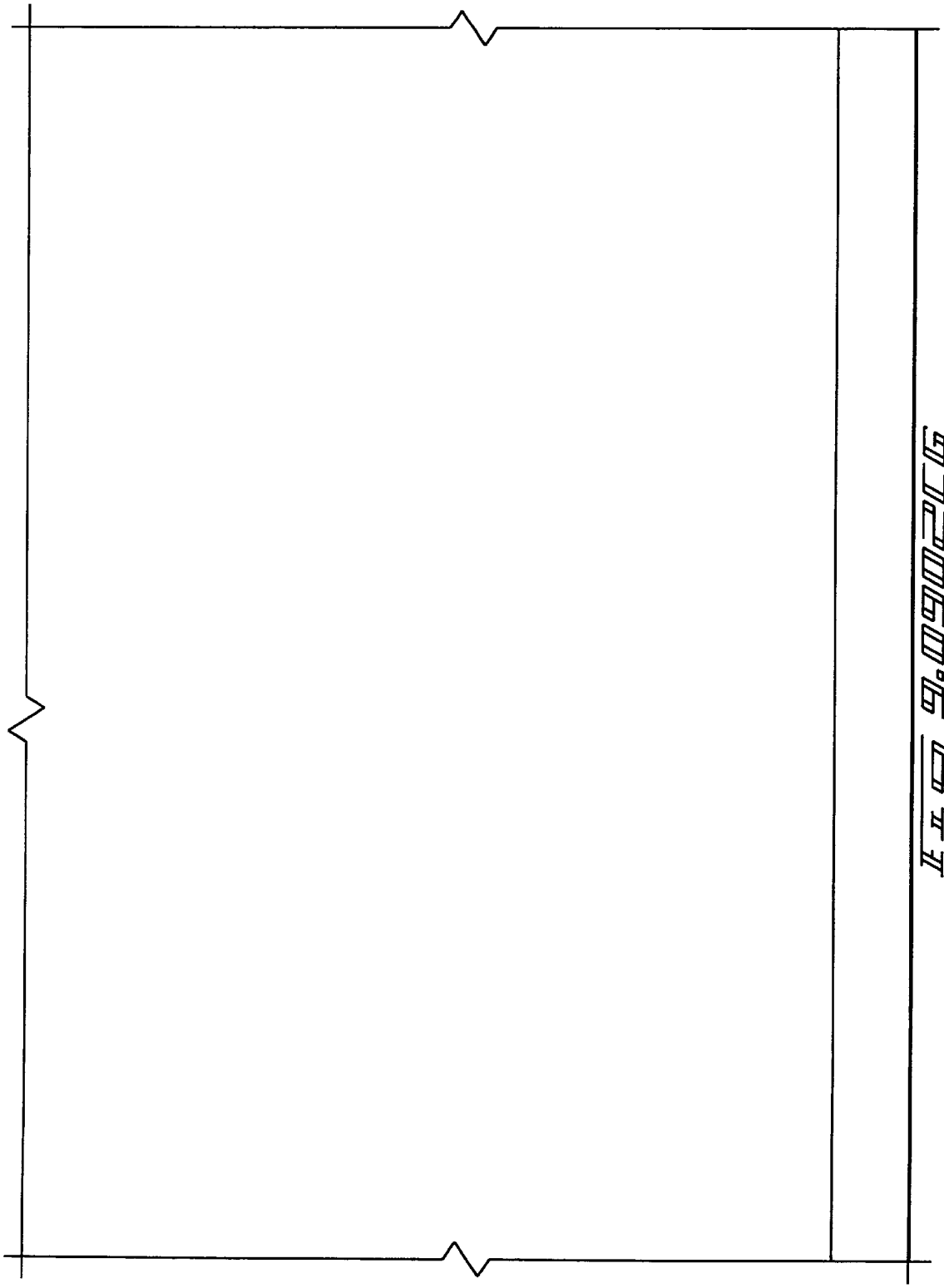


FIG. 9,760

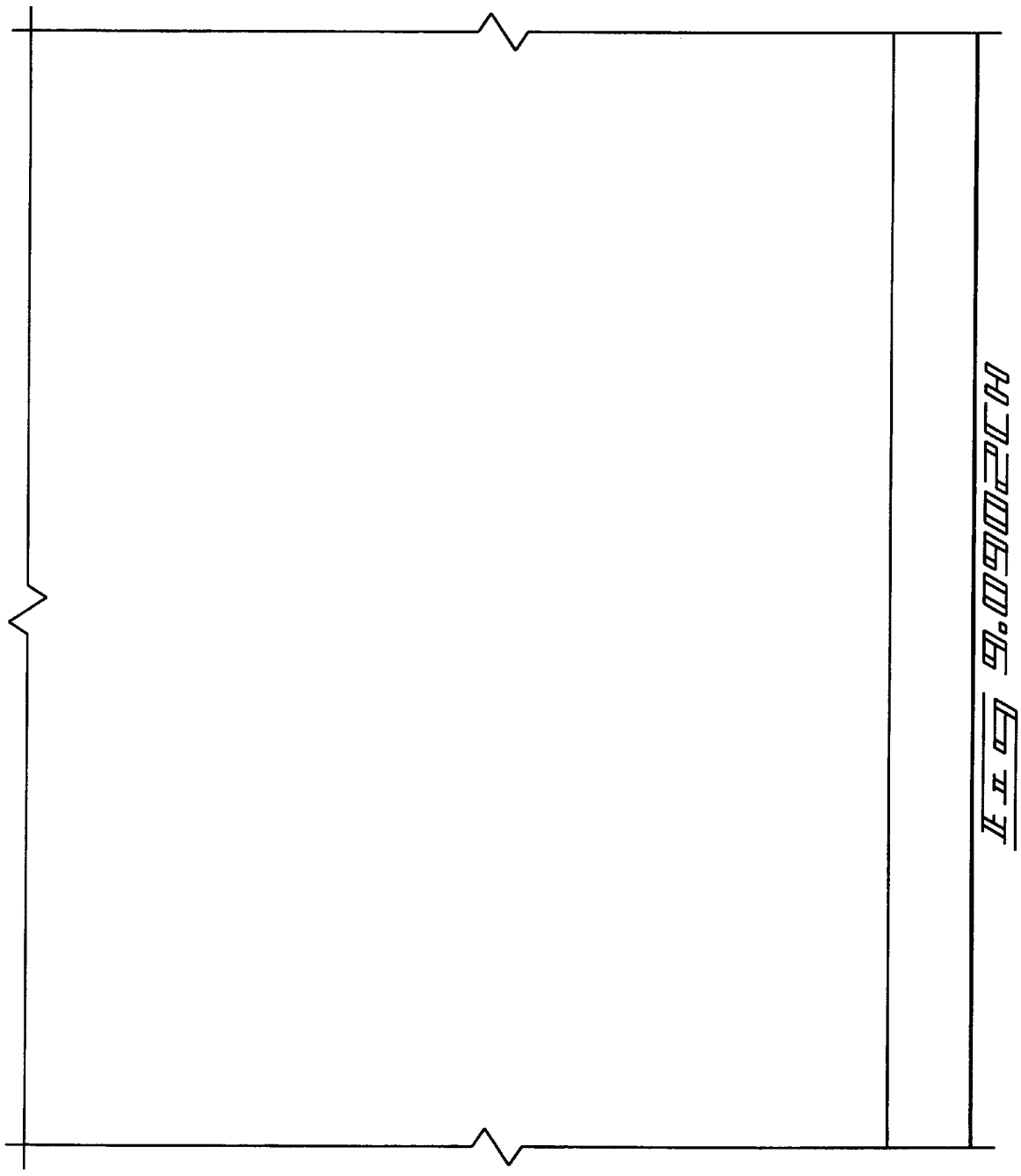


FIG 69

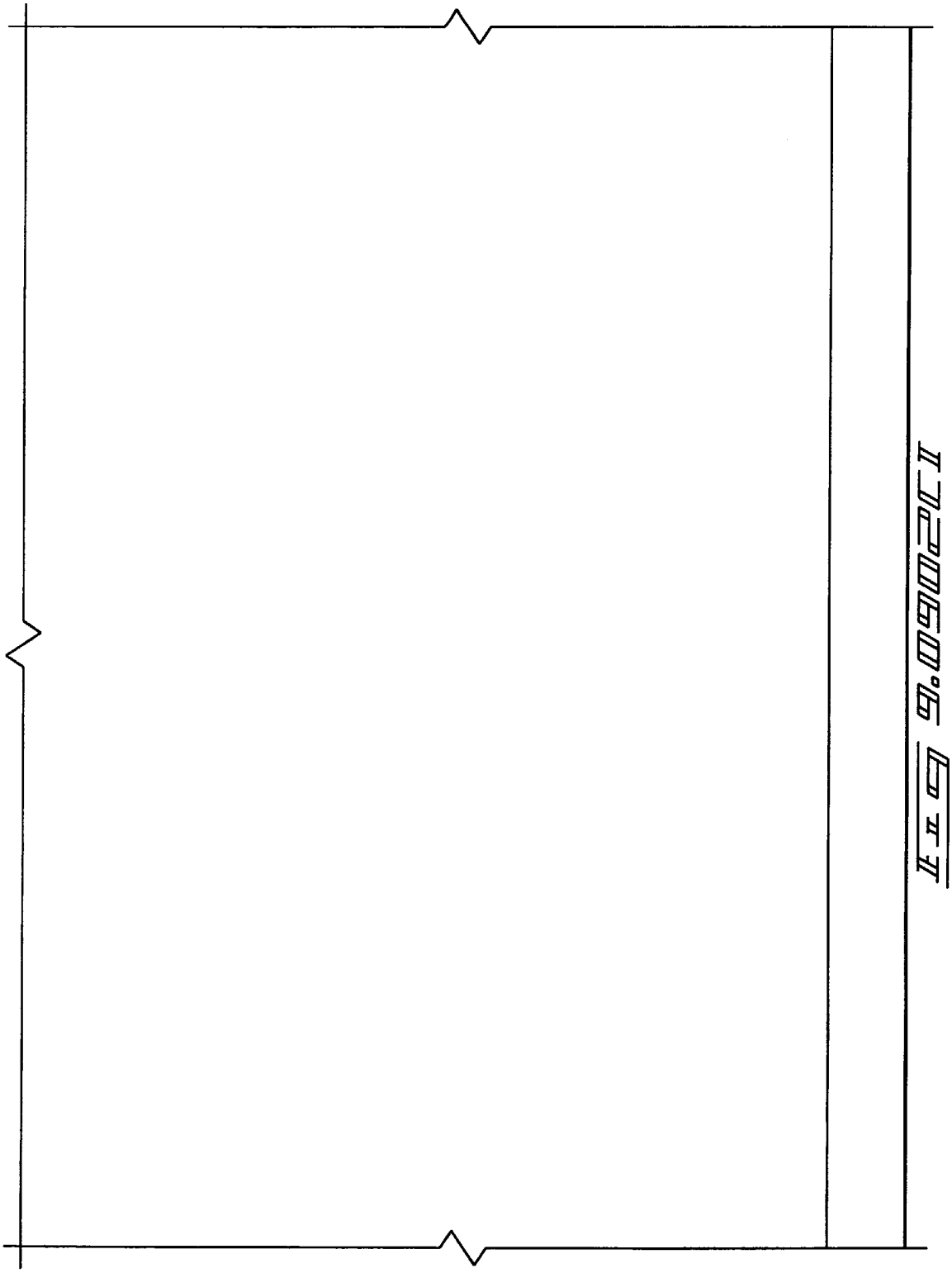


FIG. 9,090,272

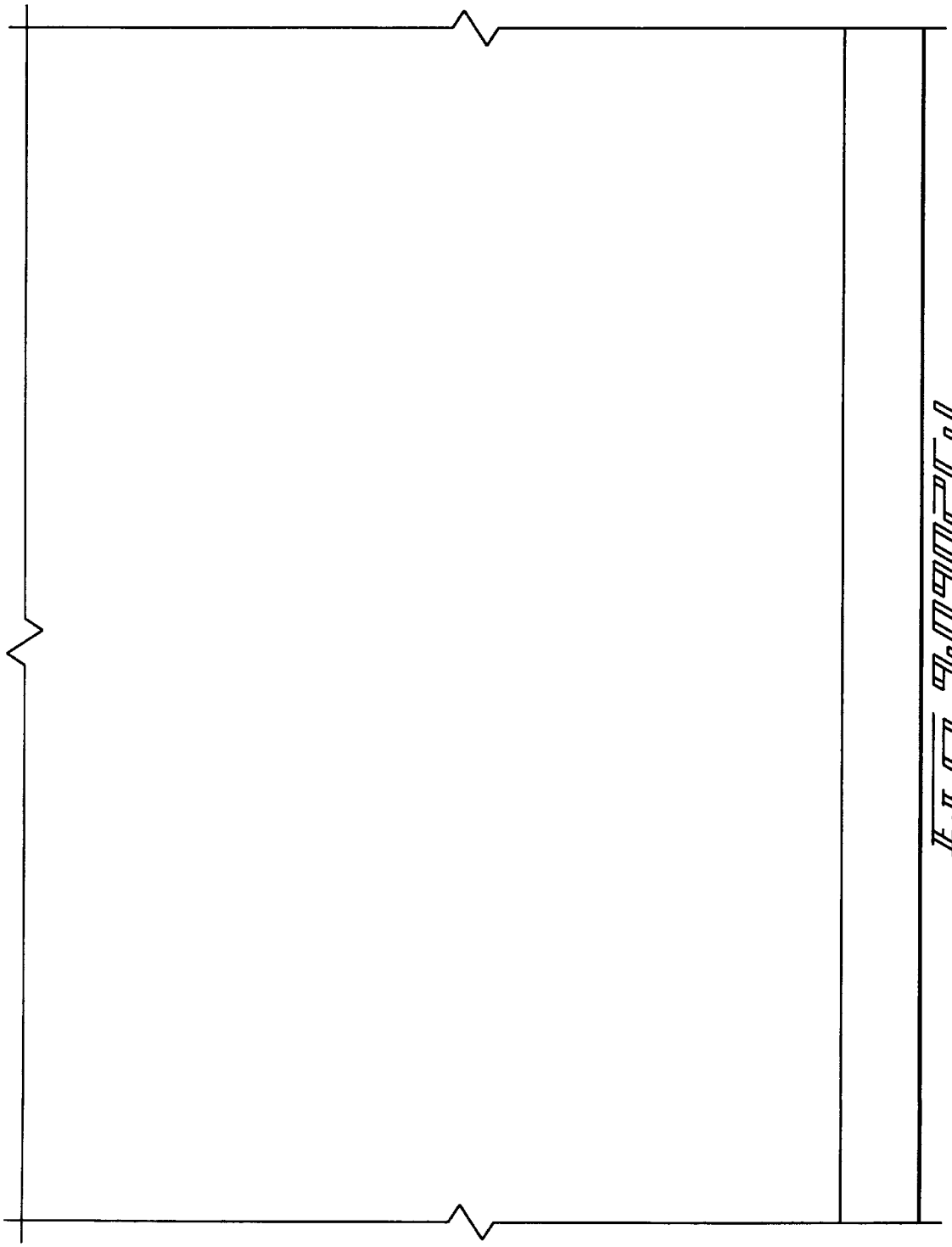


FIG 96

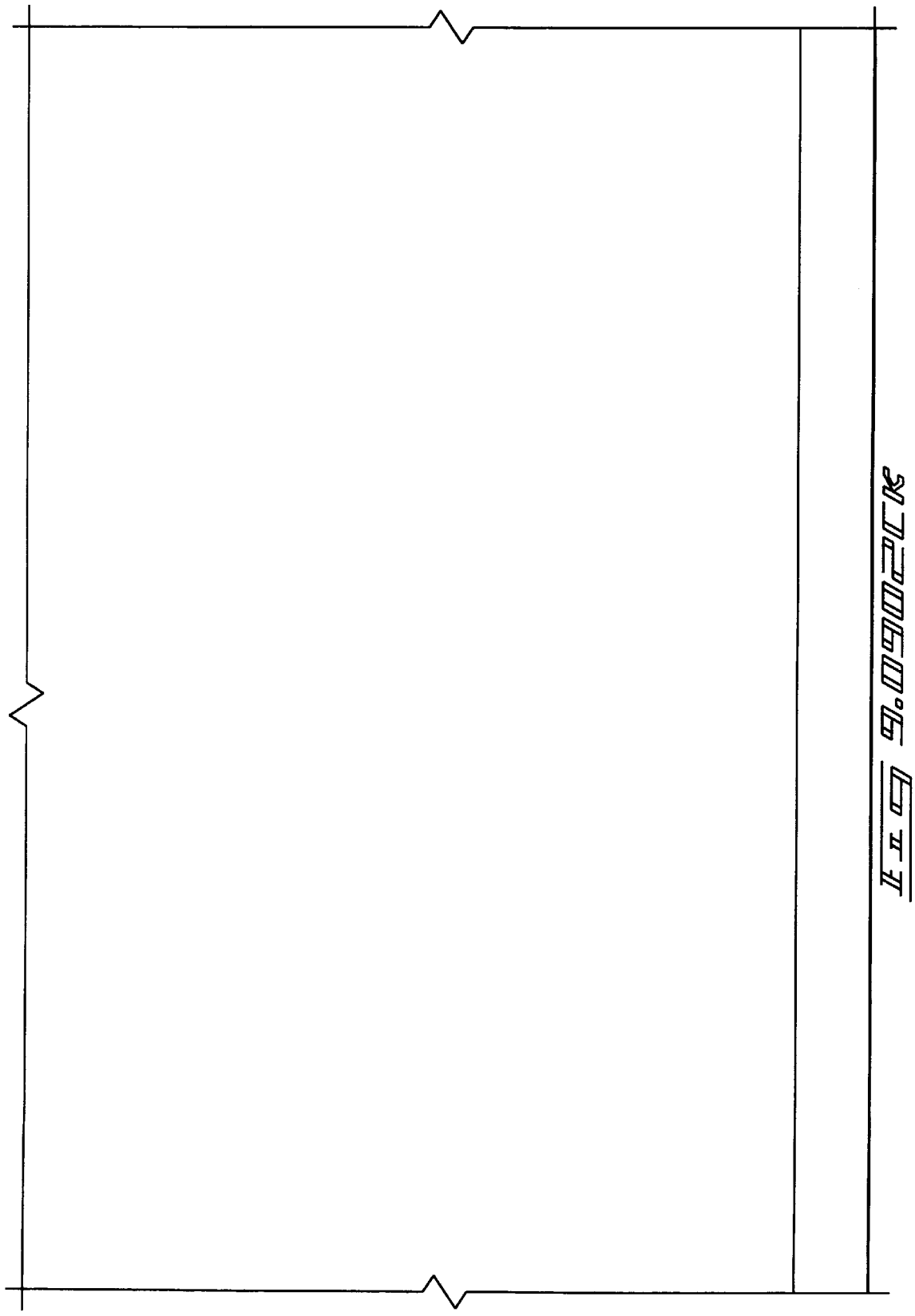
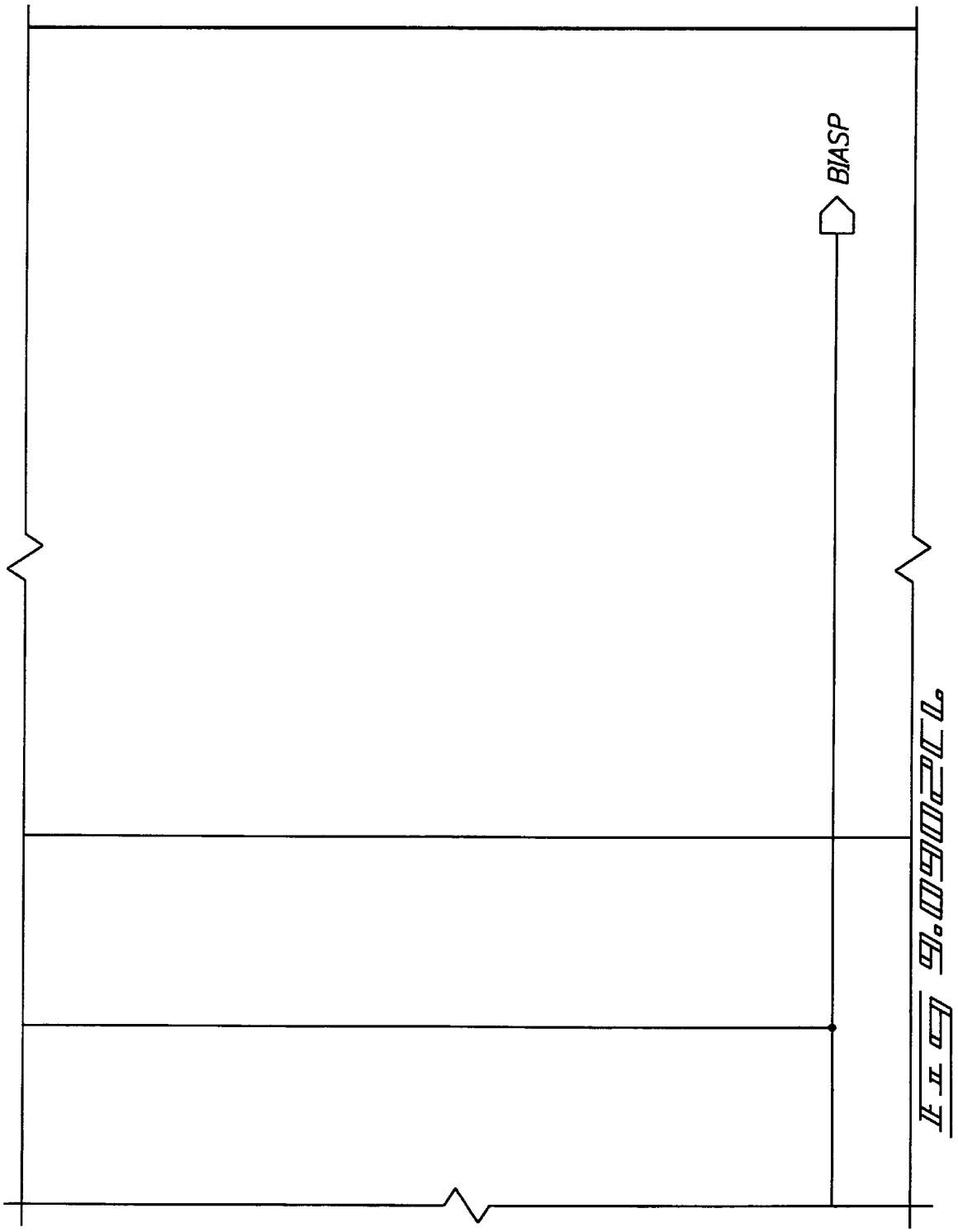


FIG 9,090,272


BIASP
FIG 91,091,276

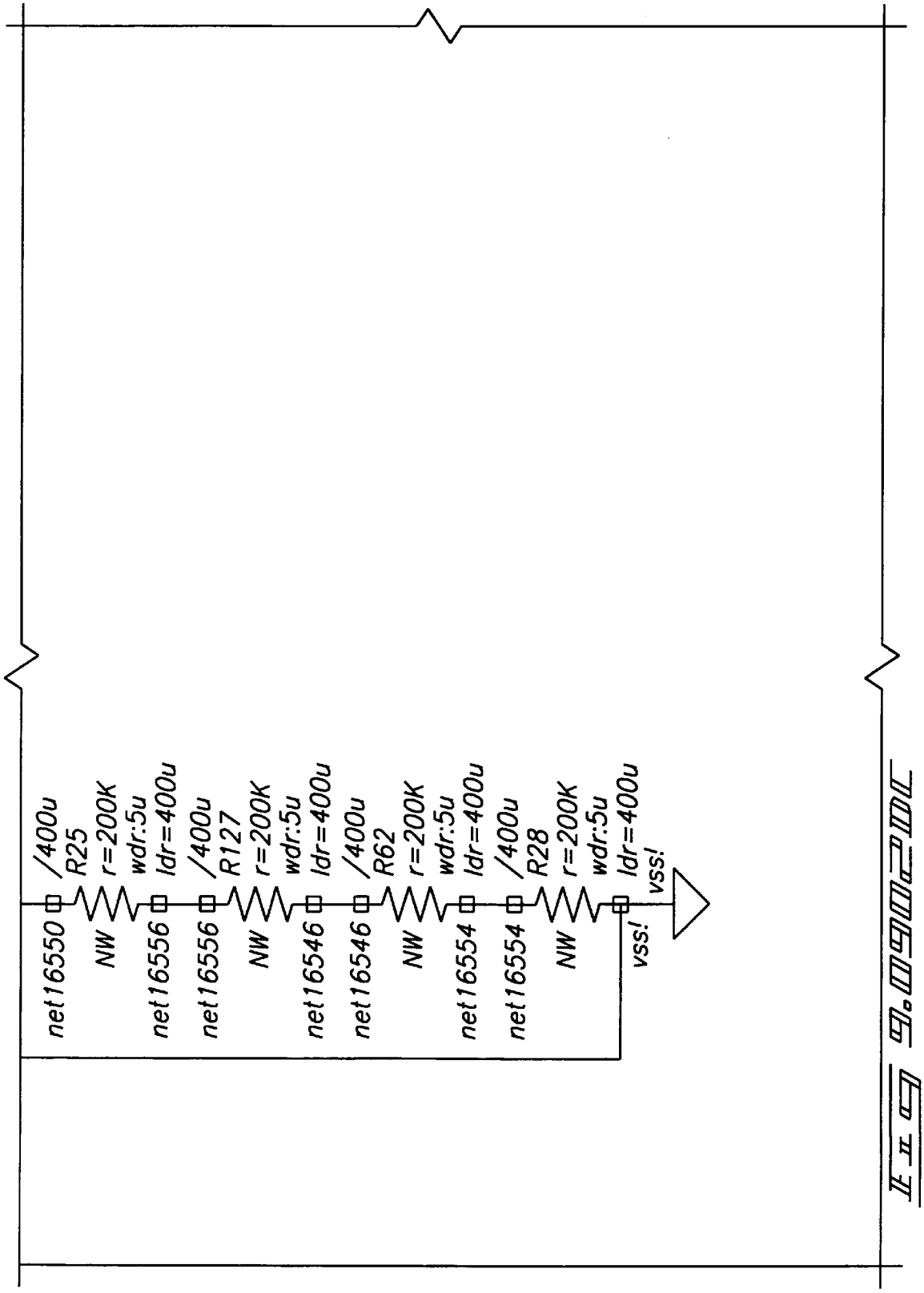

net16550
/400u
R25
r=200K
wdr:5u
ldr=400u
NW
net16556
/400u
R127
r=200K
wdr:5u
ldr=400u
NW
net16546
/400u
R62
r=200K
wdr:5u
ldr=400u
NW
net16554
/400u
R28
r=200K
wdr:5u
ldr=400u
NW
vss!
vss!

FIG 9,090,276

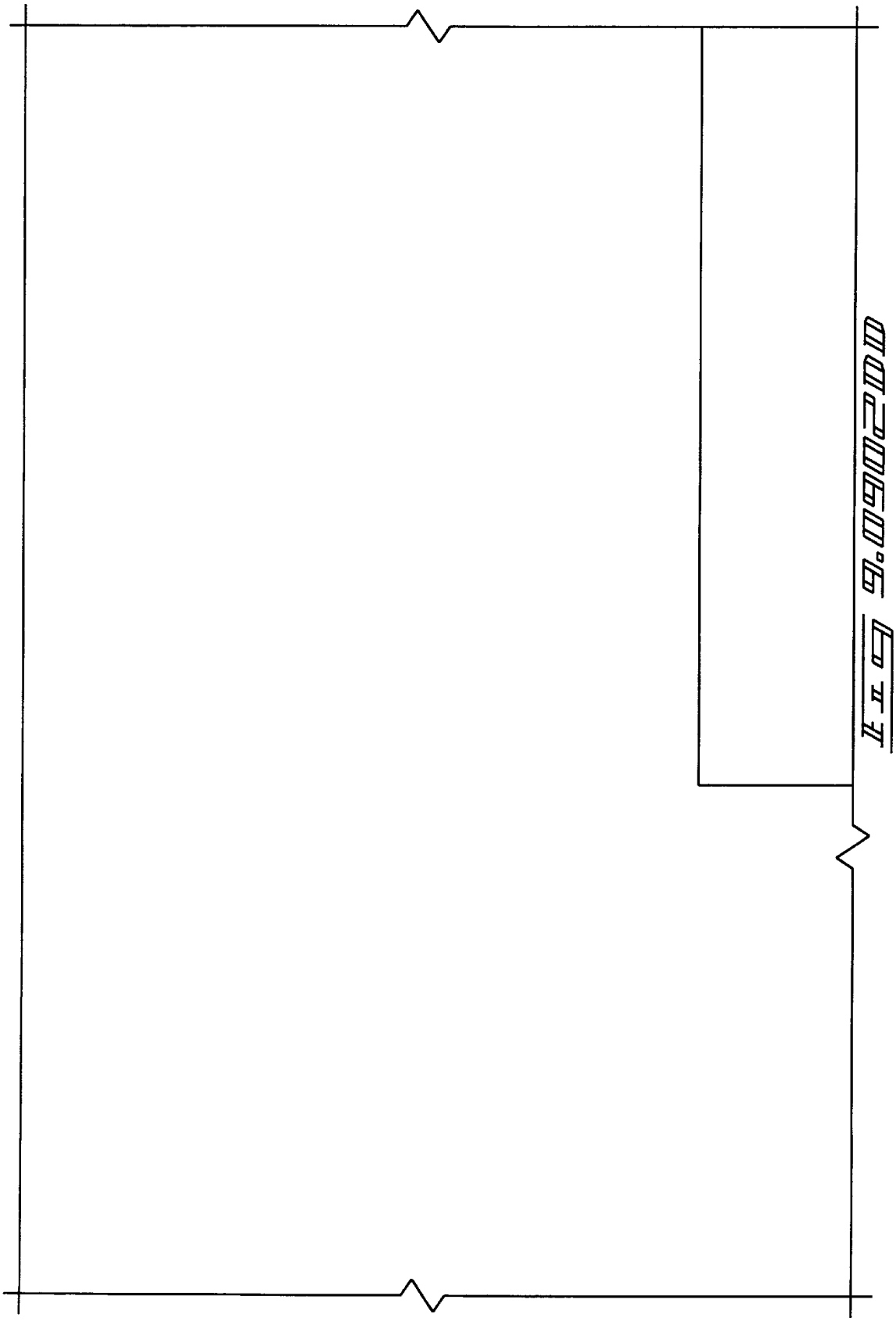


FIG. 9,000,000

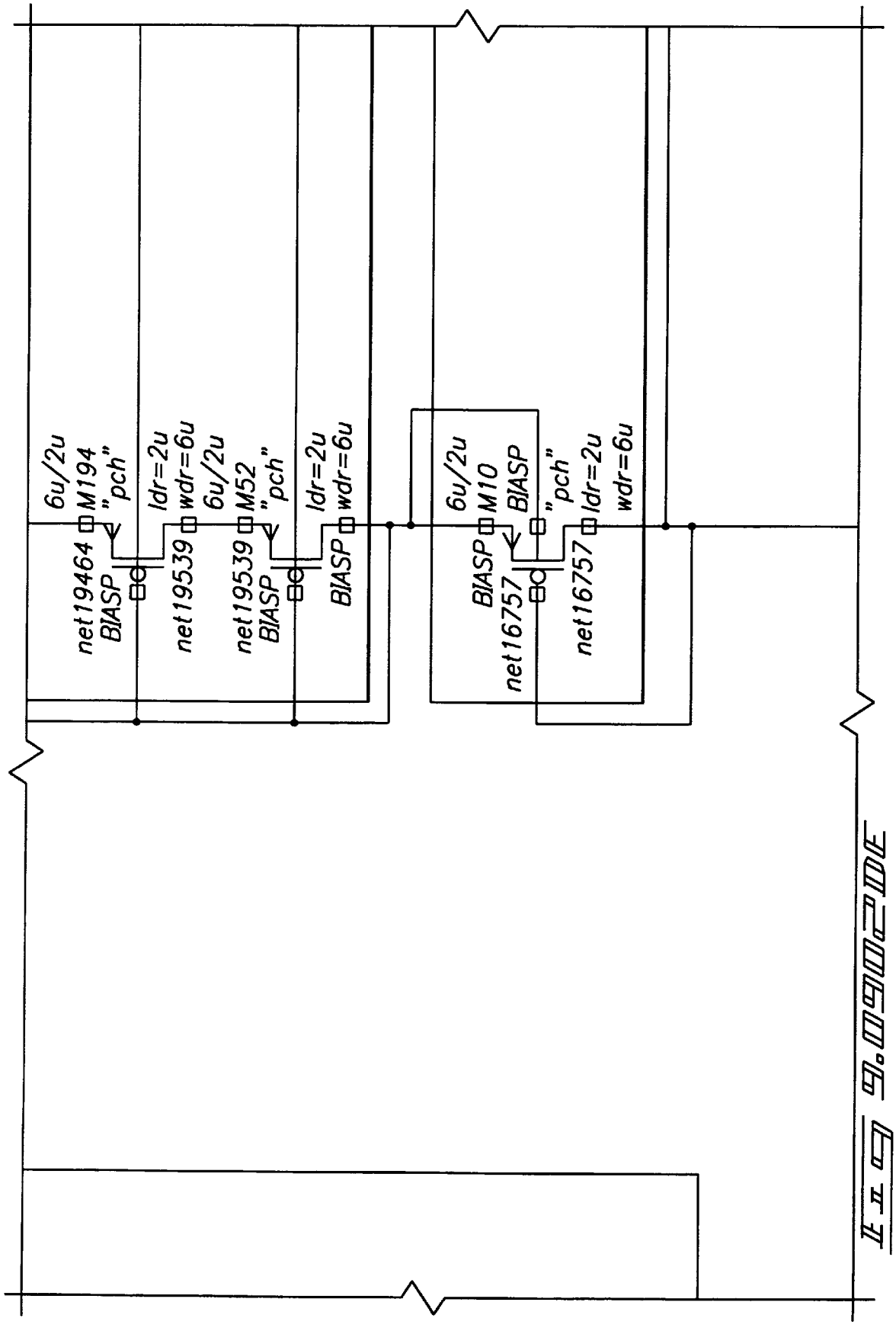


FIG 9,090,208E

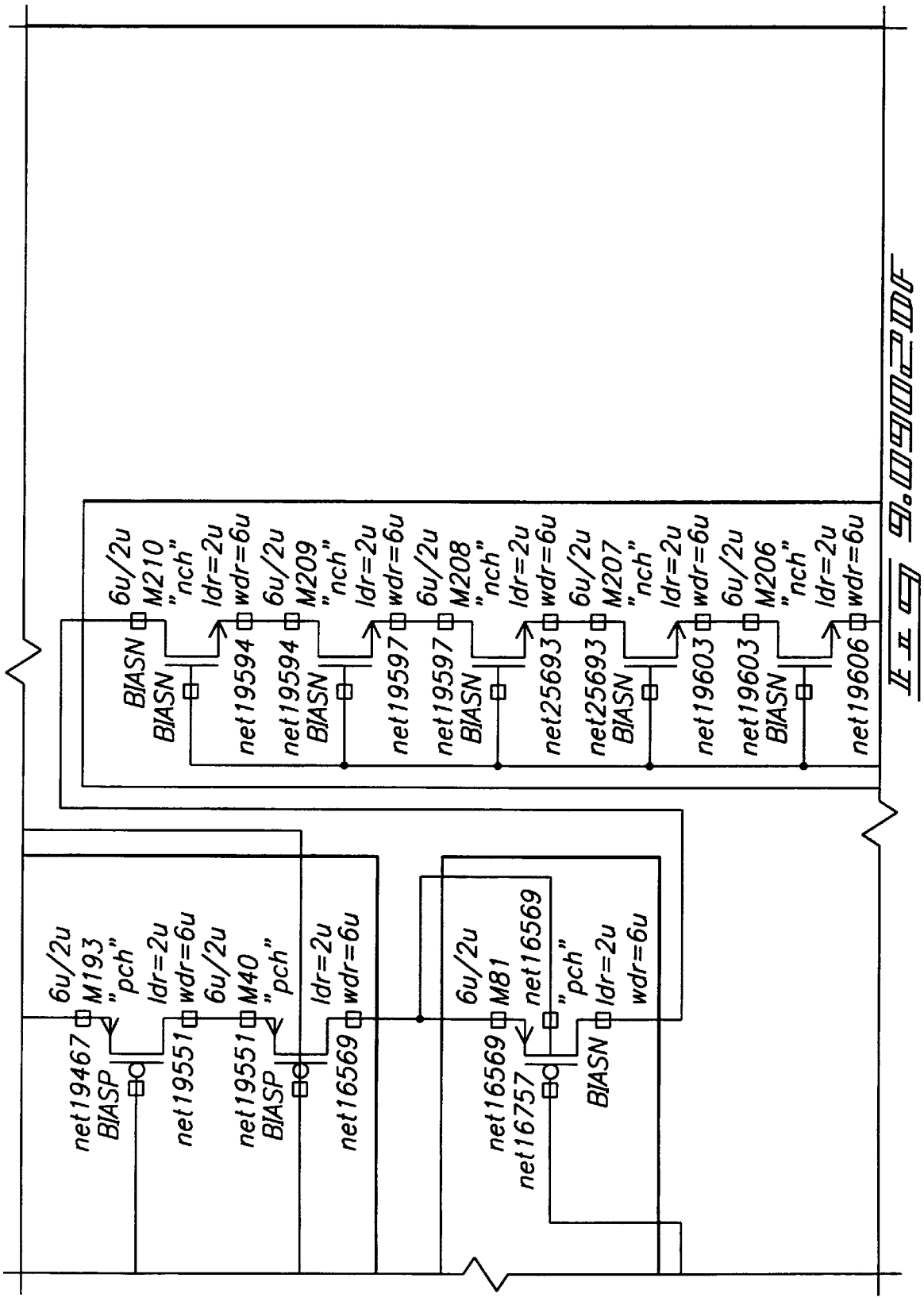
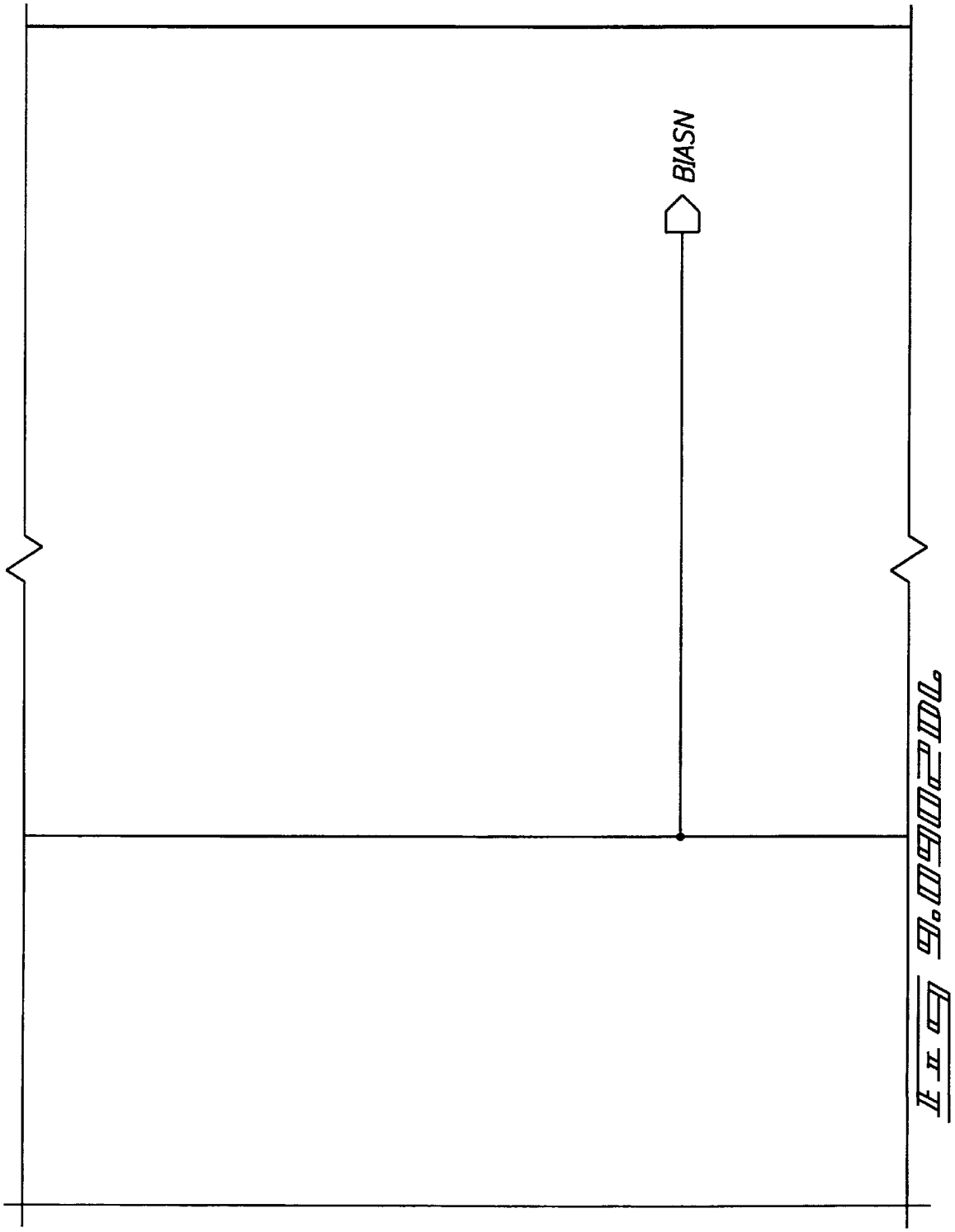
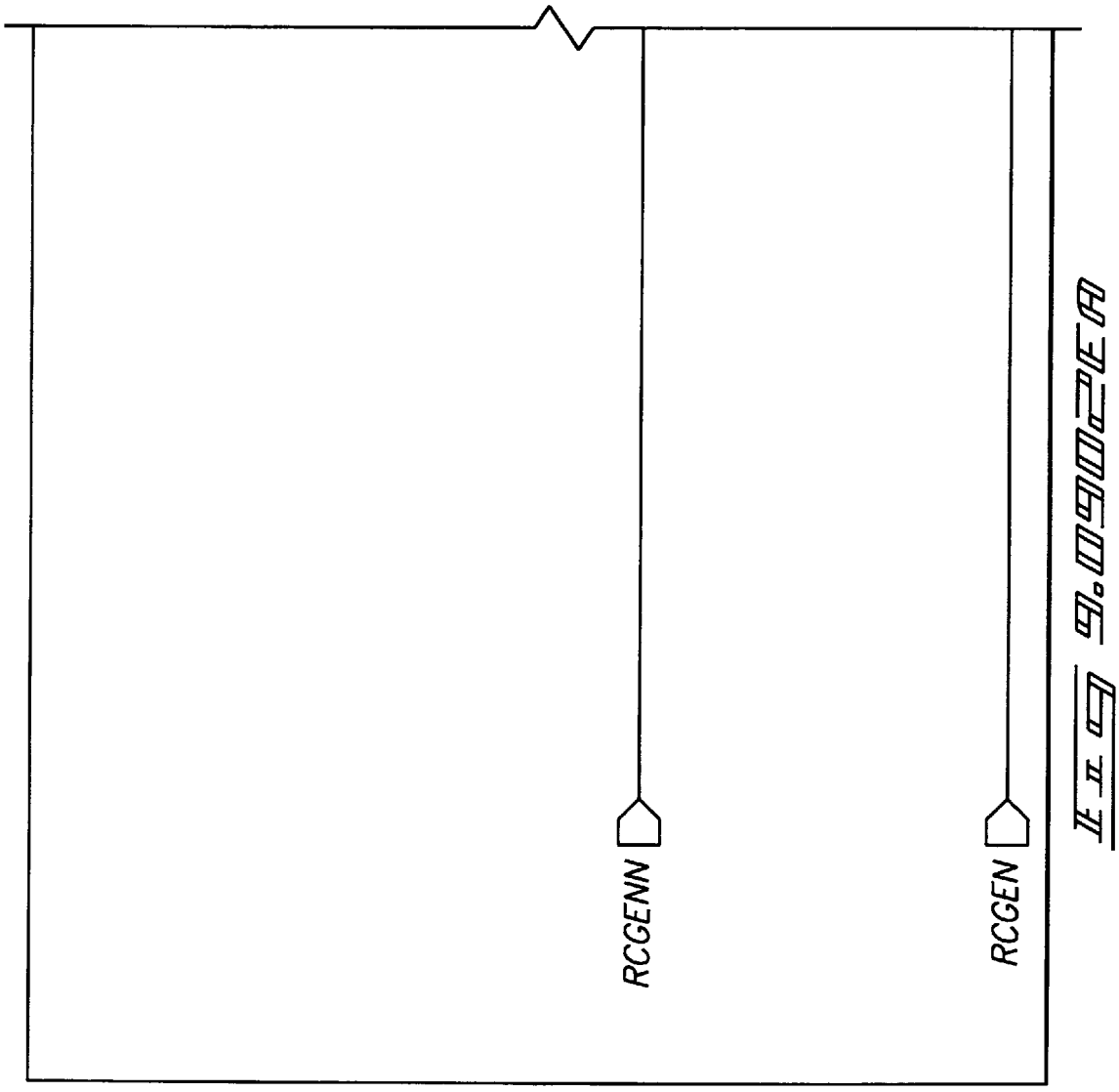

6u/2u
M210
"nch"
ldr=2u
wdr=6u
6u/2u
M209
"nch"
ldr=2u
wdr=6u
6u/2u
M208
"nch"
ldr=2u
wdr=6u
6u/2u
M207
"nch"
ldr=2u
wdr=6u
6u/2u
M206
"nch"
ldr=2u
wdr=6u
BIASN
net19594
net19597
net25693
net19603
net19606
6u/2u
M193
"pch"
ldr=2u
wdr=6u
6u/2u
M40
"pch"
ldr=2u
wdr=6u
6u/2u
M81
"pch"
ldr=2u
wdr=6u
BIASP
net19467
net19551
net16569
net16757

Fig 9,090,2DF


BIASN
FIG 9,090,704


RCGENN
RCGEN
FIG 9,090,264

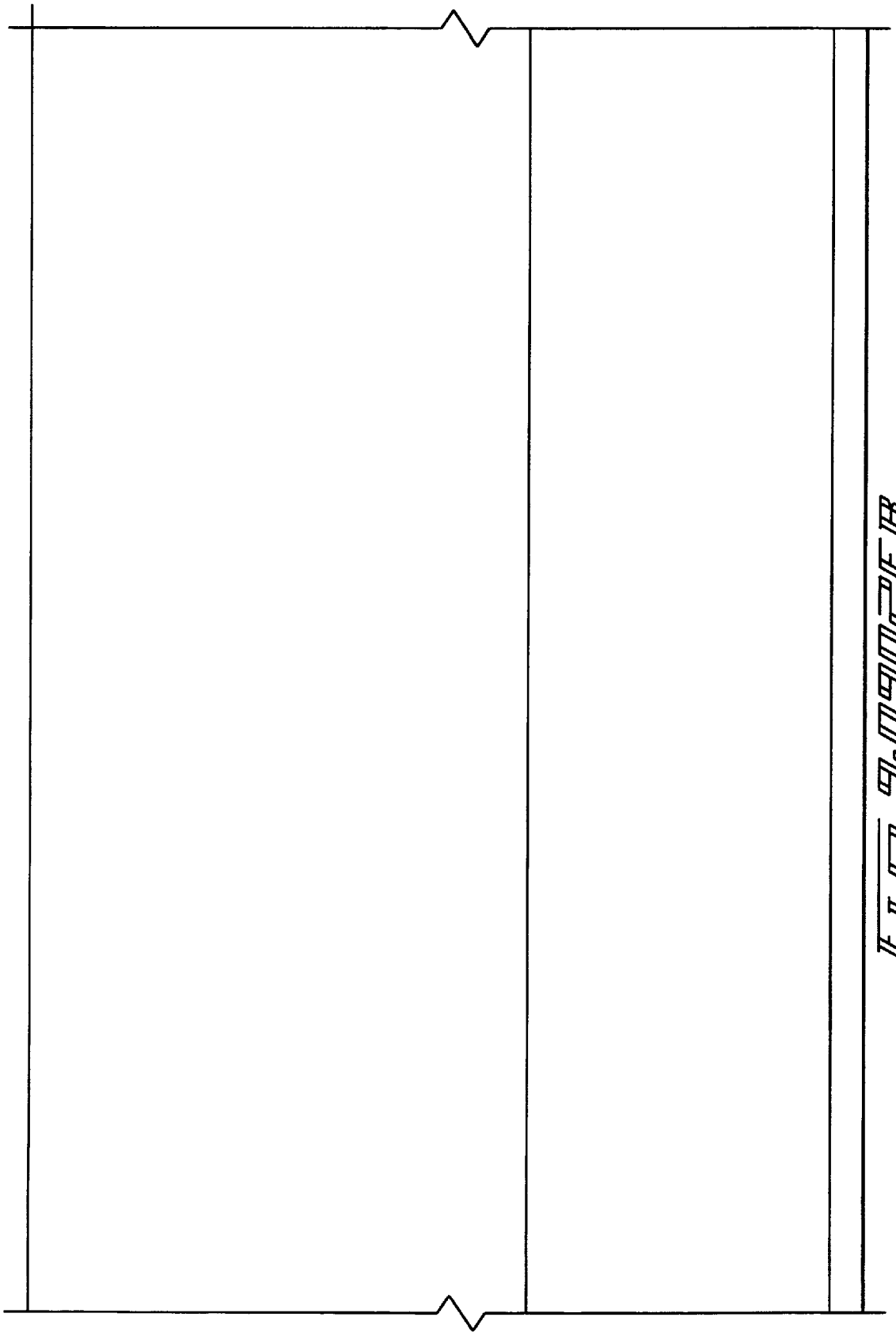


FIG. 6,130,602

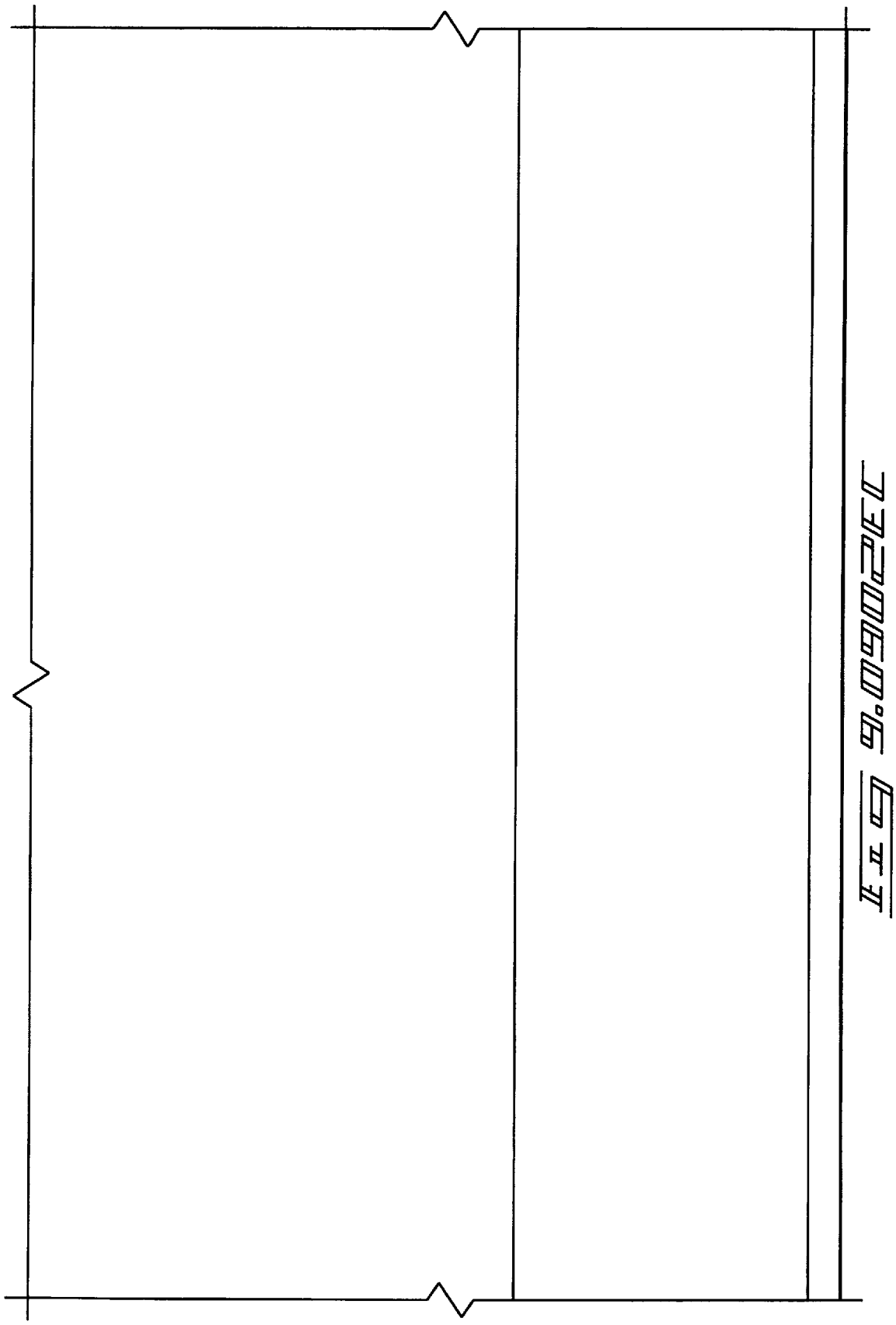
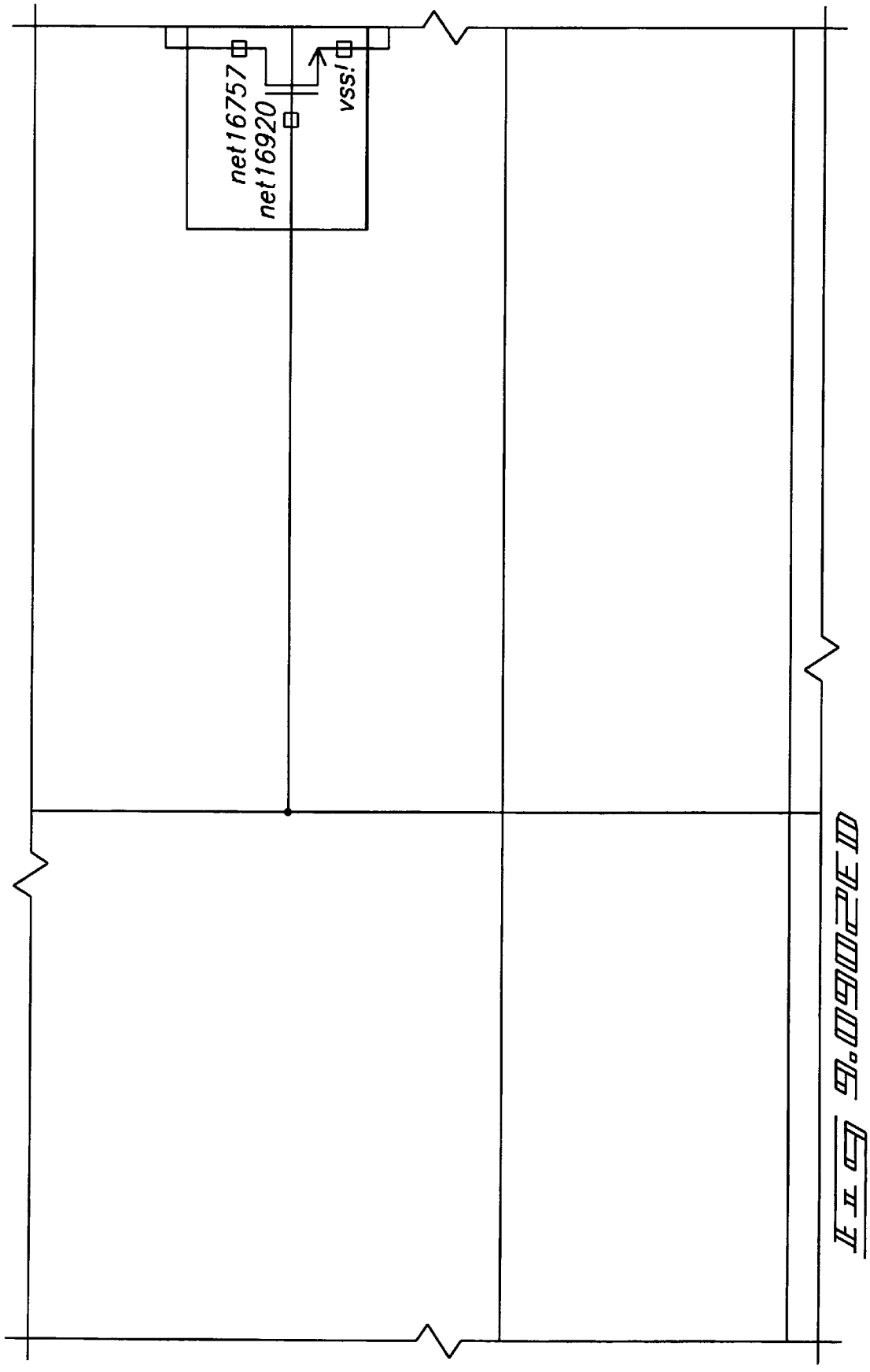


FIG. 6,130,602


net16757
net16920
vss!
FIG. 9,009,626

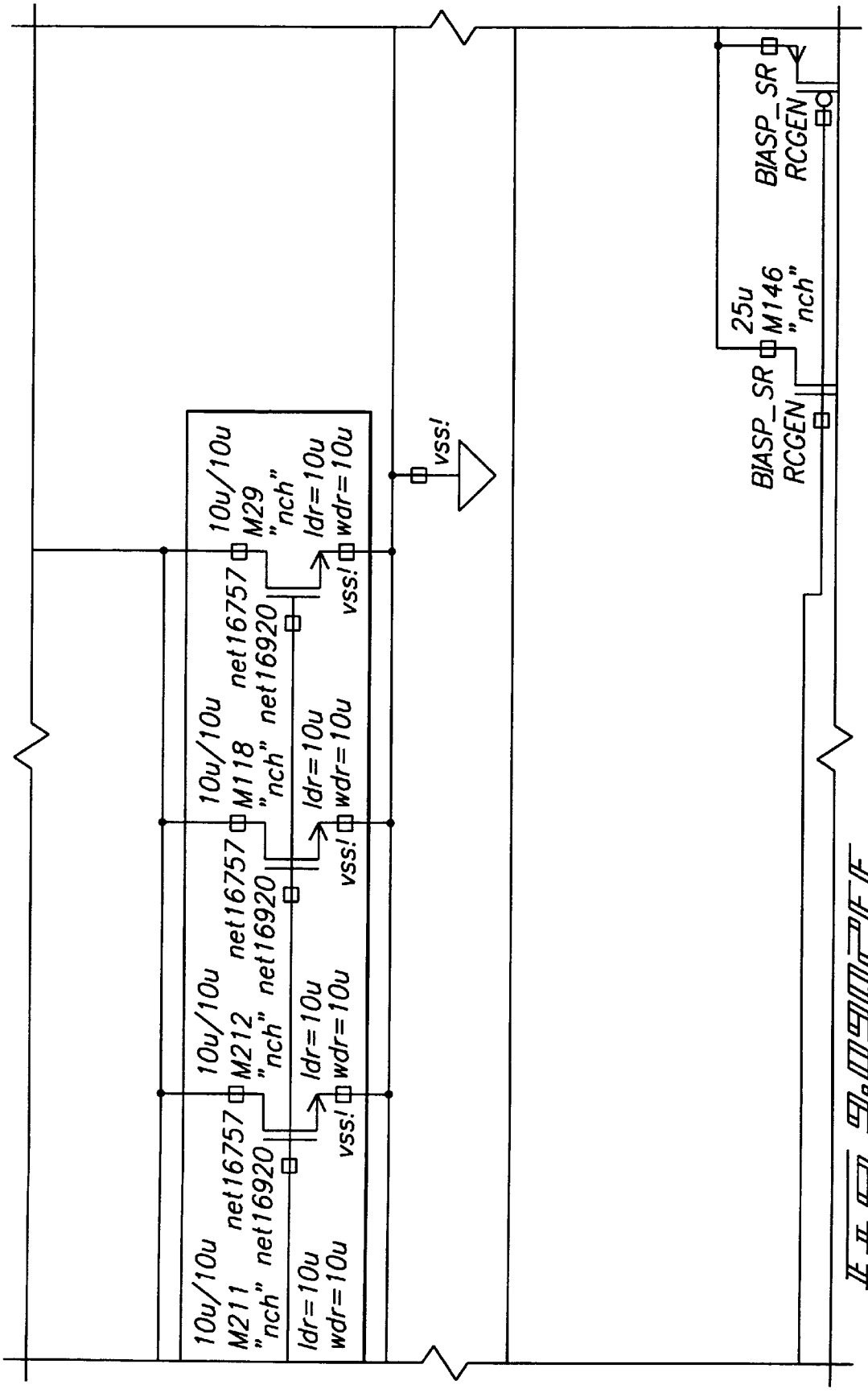

BIASP_SR
RCGEN
25u
M146
"nch"
BIASP_SR
RCGEN
vss!
10u/10u
M29
"nch"
ldr=10u
wdr=10u
net16757
net16920
vss!
10u/10u
M118
"nch"
ldr=10u
wdr=10u
net16757
net16920
vss!
10u/10u
M212
"nch"
ldr=10u
wdr=10u
net16757
net16920
vss!
10u/10u
M211
"nch"
ldr=10u
wdr=10u
net16757
net16920
vss!

FIG. 99,099

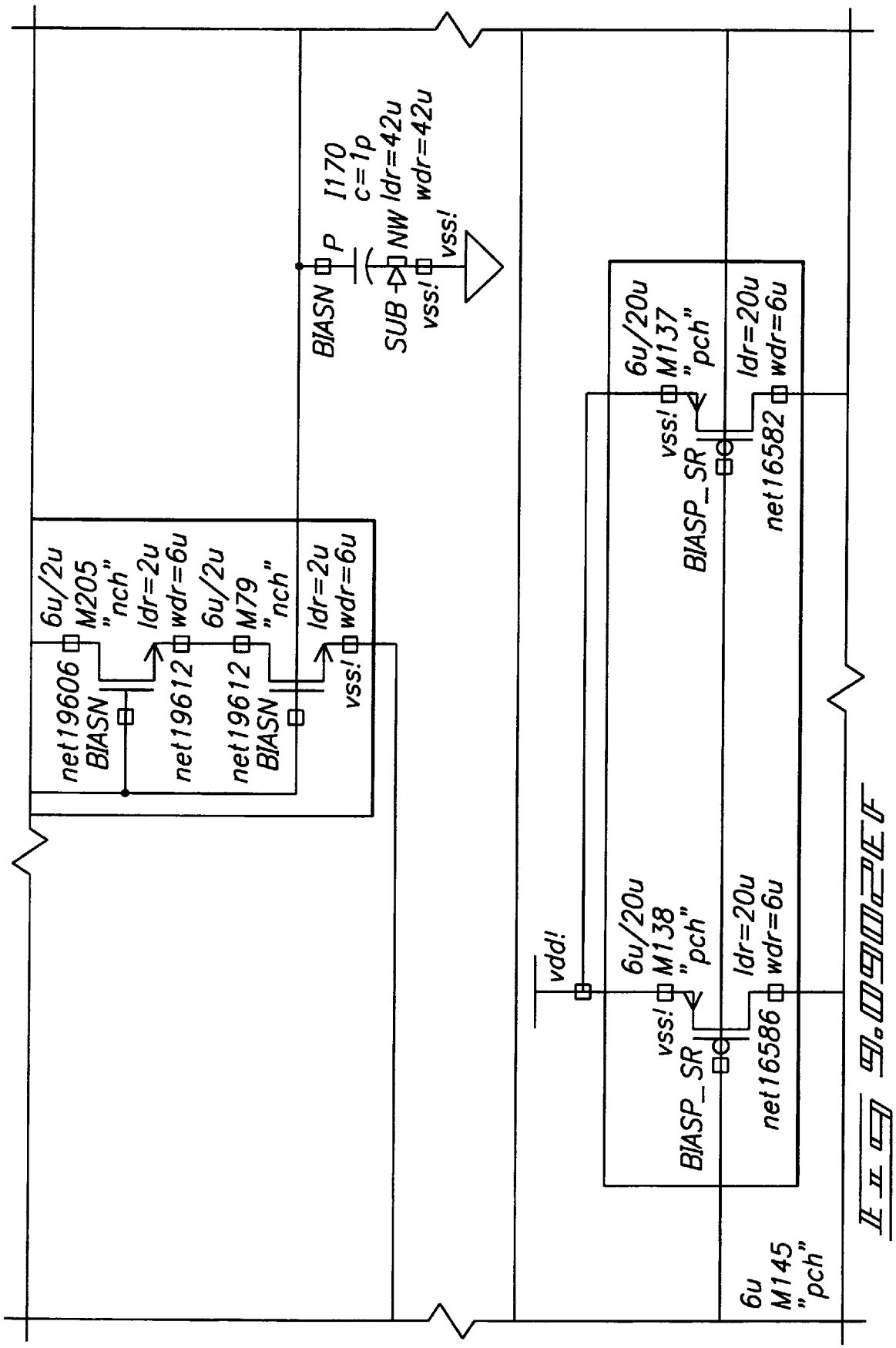
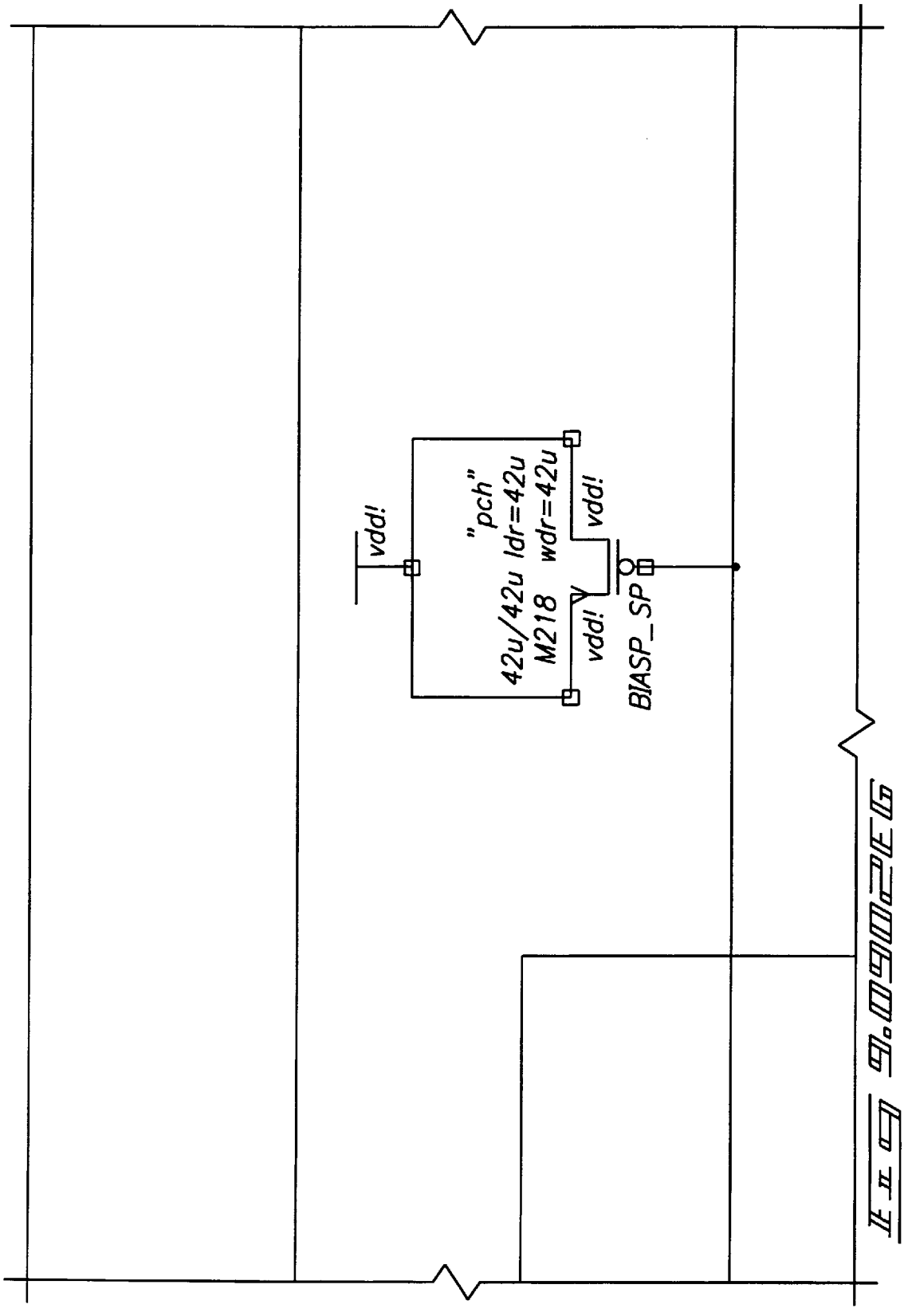

I170
c=1p
ldr=42u
wdr=42u
BIASN
P
SUB
NW
vss!
vss!
6u/2u
M205
"nch"
ldr=2u
wdr=6u
net19606
BIASN
net19612
6u/2u
M79
"nch"
ldr=2u
wdr=6u
net19612
BIASN
vss!
6u/20u
M137
"pch"
ldr=20u
wdr=6u
vss!
BIASP_SR
net16582
vdd!
6u/20u
M138
"pch"
ldr=20u
wdr=6u
vss!
BIASP_SR
net16586
6u
M145
"pch"

FIG 9.0906F


vdd!
"pch"
42u/42u ldr=42u
M218 wdr=42u
vdd!
vdd!
BIASP_SP
FIG. 2767

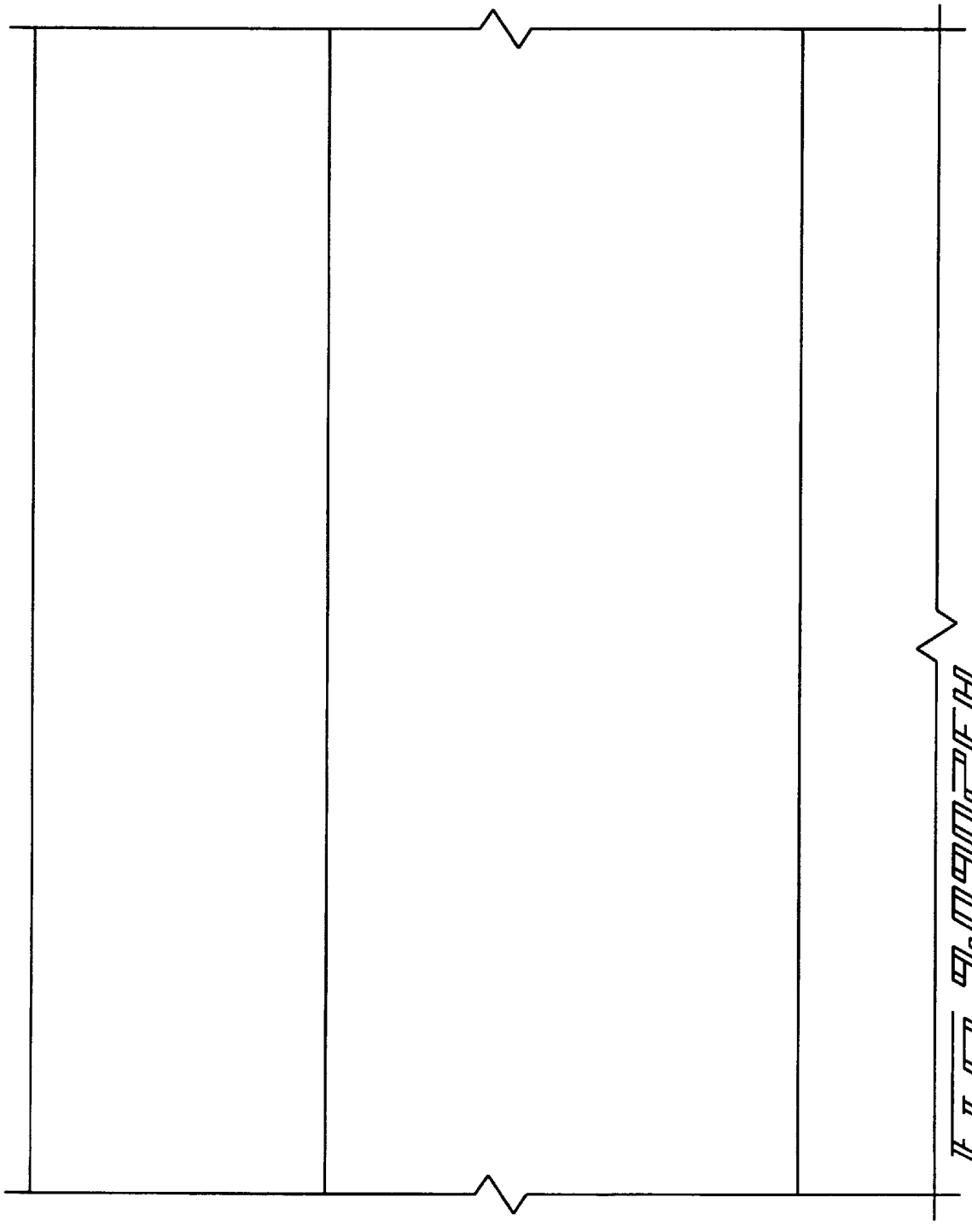


FIG 96,096,264

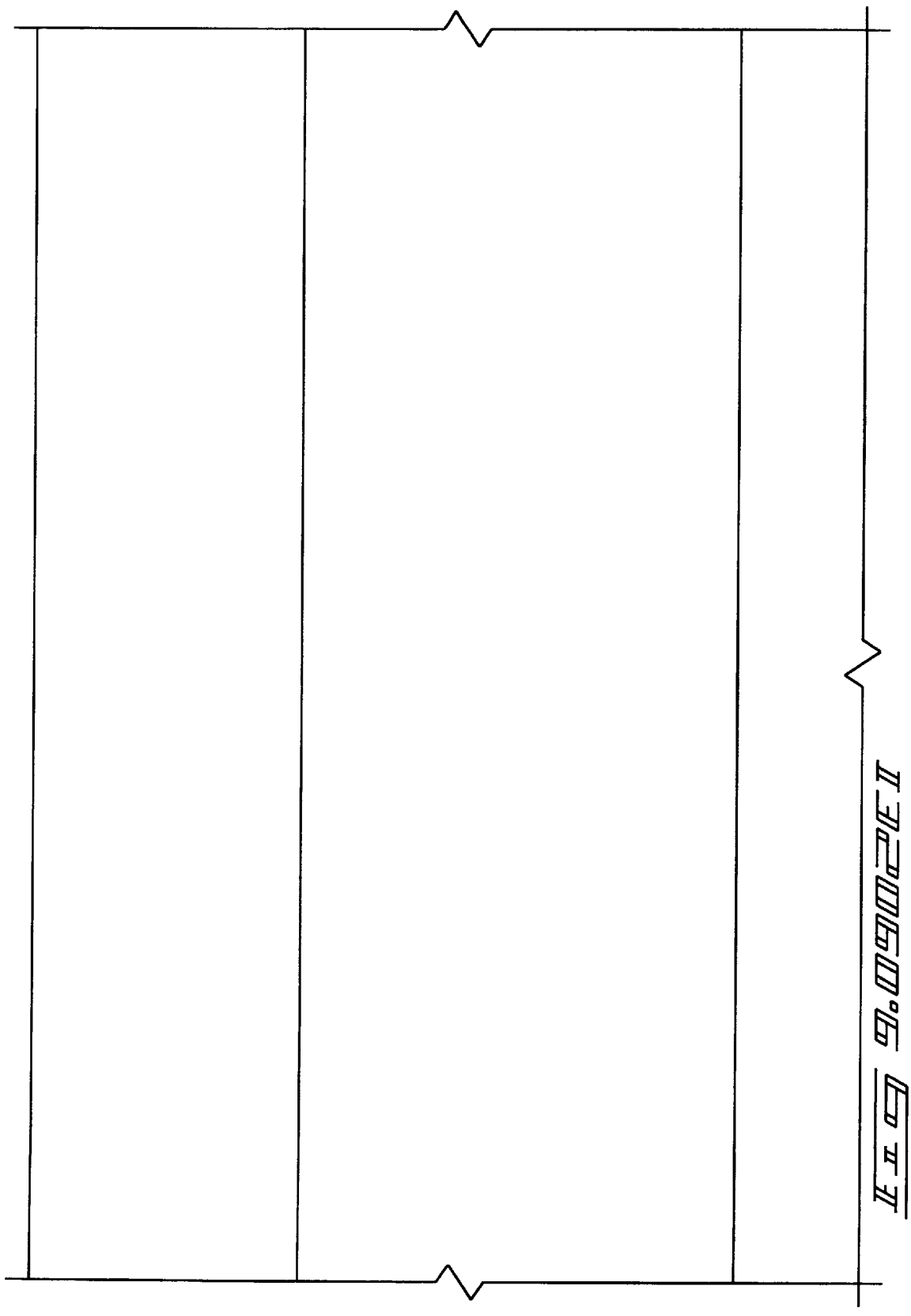


FIG 9,060,324

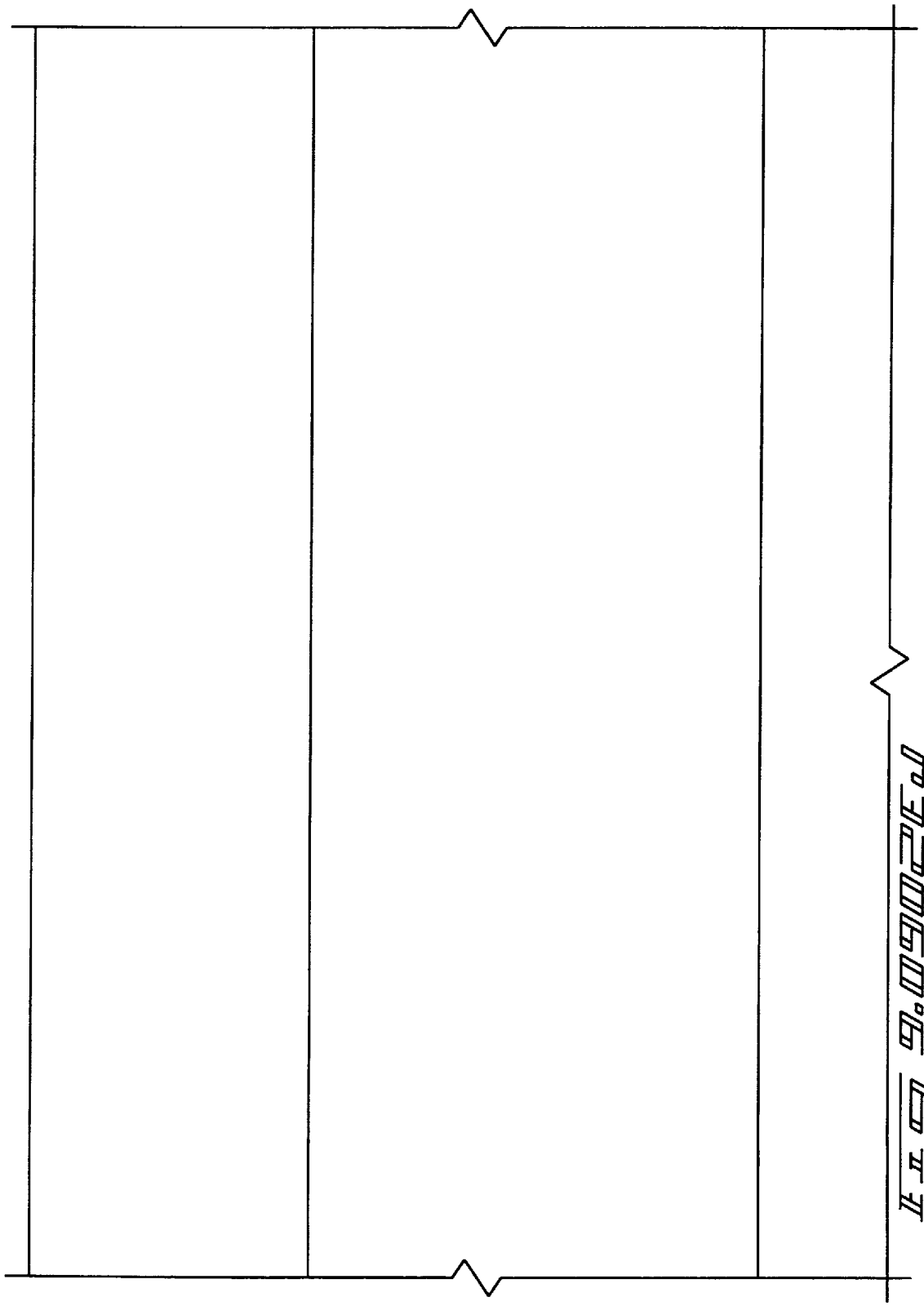


FIG. 96

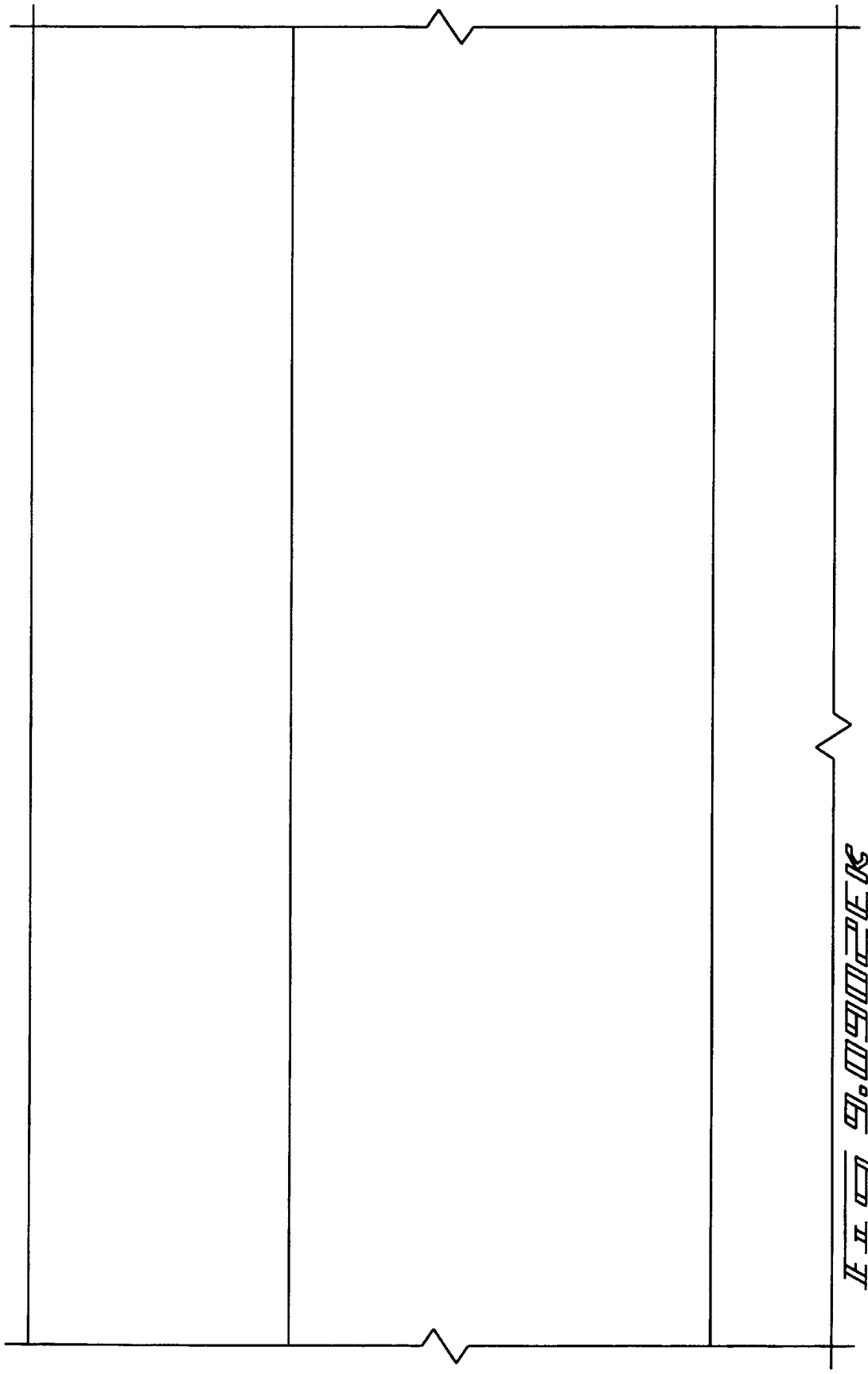
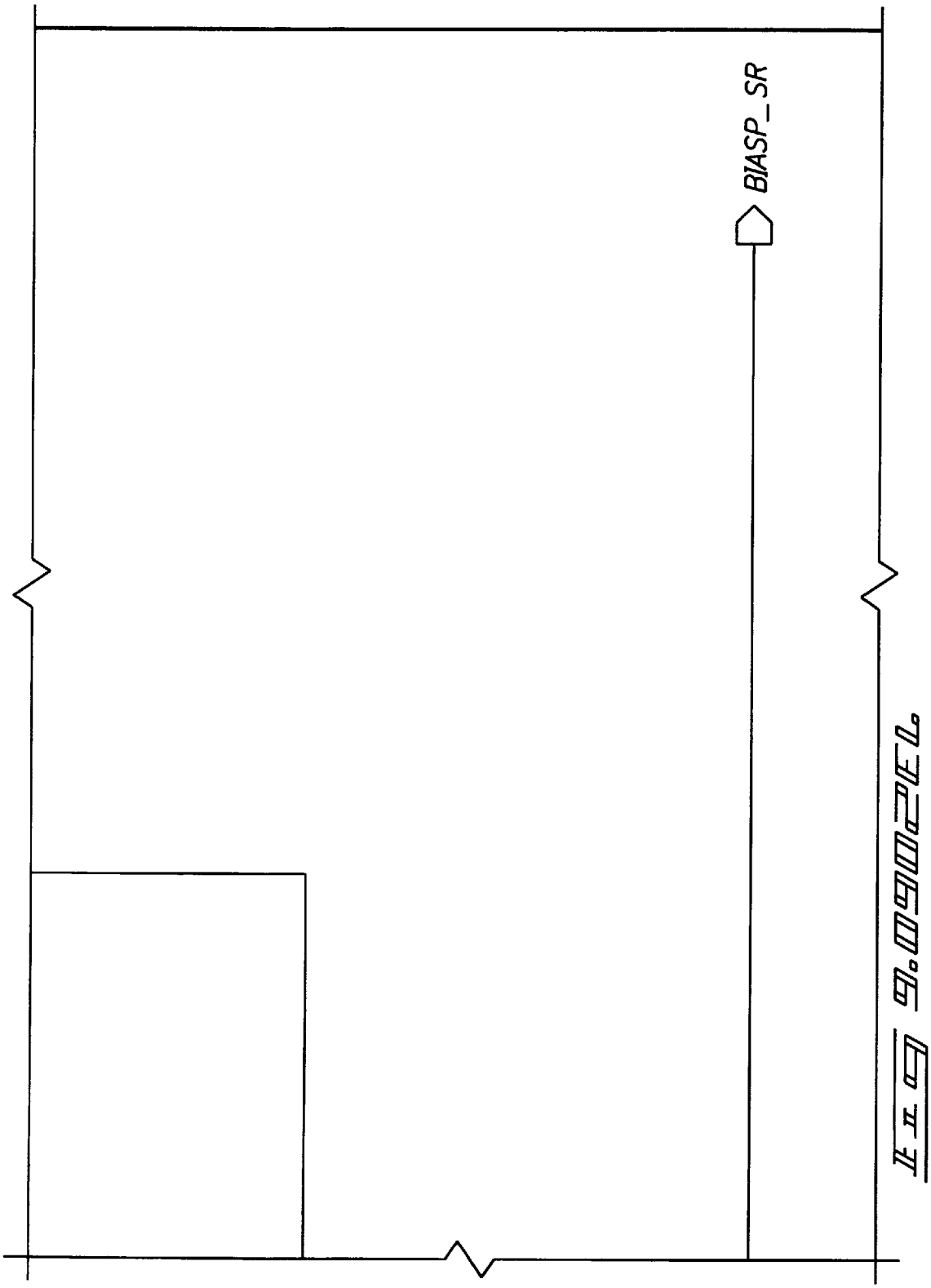


FIG 9,090,216


BIASP_SR
FIG. 9,090,261

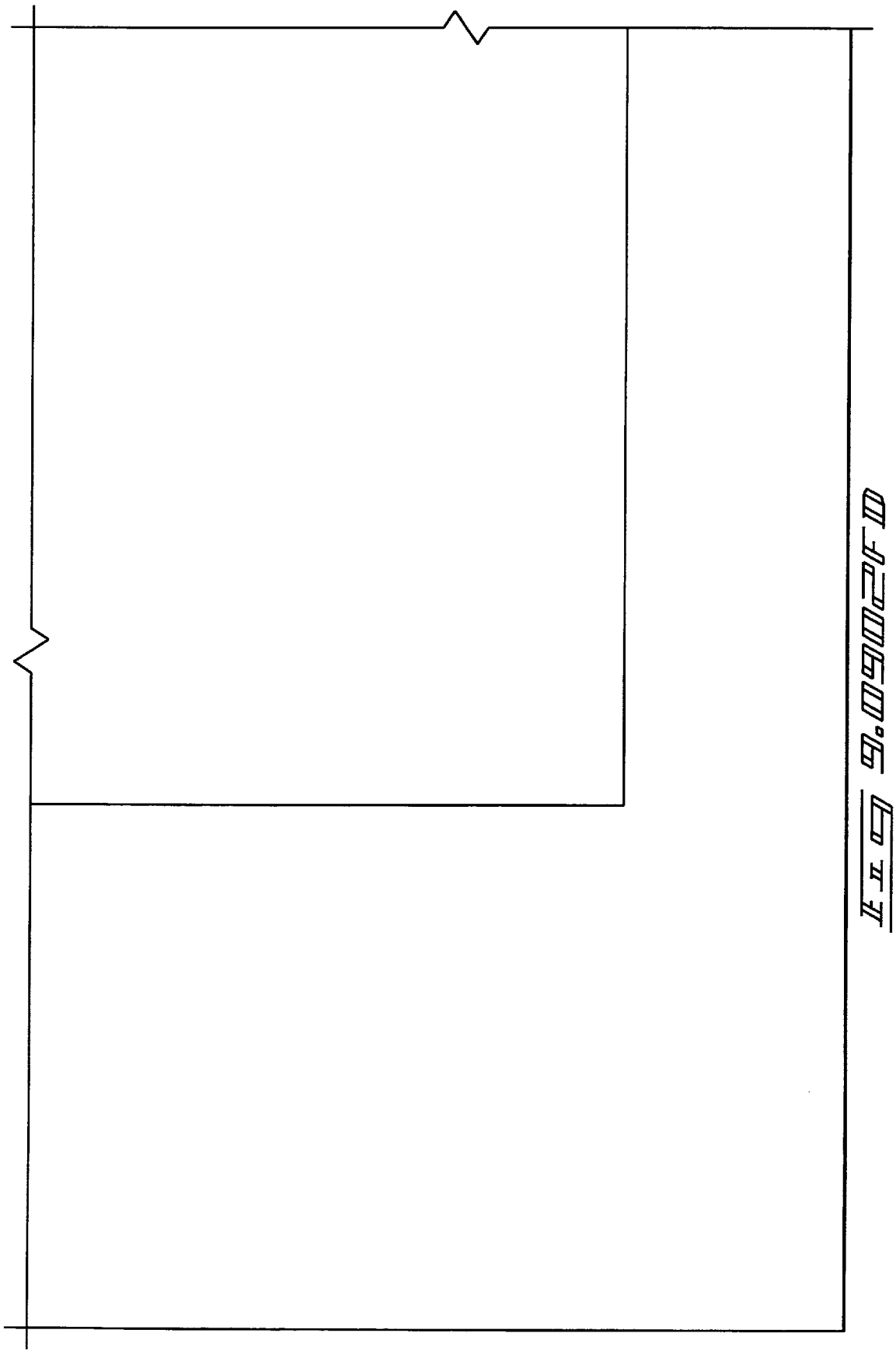


FIG. 6,130,602

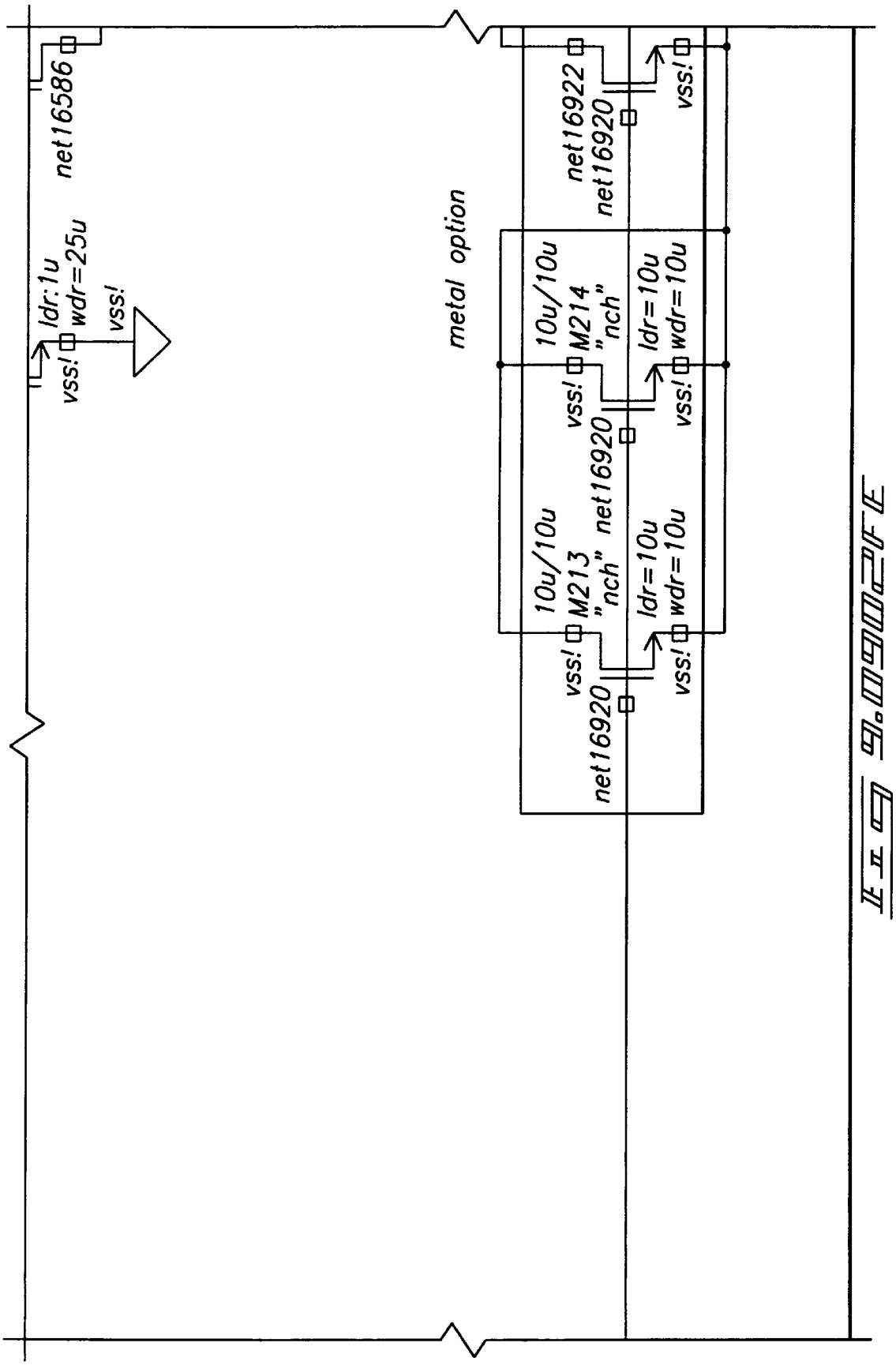
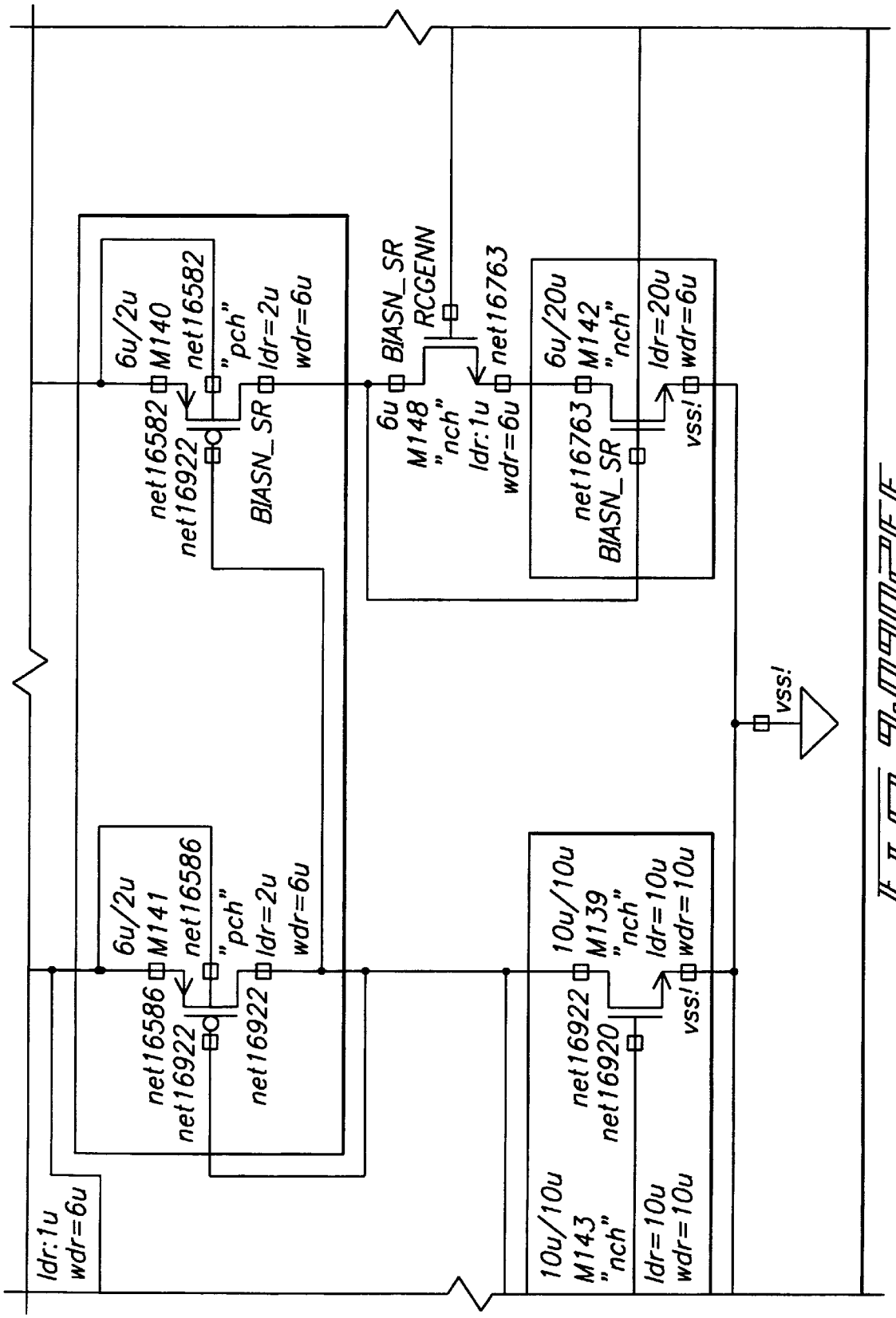

net16586
ldr:1u
wdr=25u
vss!
vss!
metal option
net16922
net16920
vss!
10u/10u
M214
"nch"
ldr=10u
wdr=10u
vss!
vss!
vss!
10u/10u
M213
"nch"
net16920
ldr=10u
wdr=10u
vss!
vss!
net16920

FIG 6


6u/2u
M140
net16582
"pch"
ldr=2u
wdr=6u
net16582
net16922
BIASN_SR
BIASN_SR
RCGENN
6u
M148
"nch"
ldr:1u
wdr=6u
net16763
6u/20u
M142
"nch"
ldr=20u
wdr=6u
net16763
BIASN_SR
vss!
6u/2u
M141
net16586
"pch"
ldr=2u
wdr=6u
net16586
net16922
net16922
10u/10u
M139
"nch"
ldr=10u
wdr=10u
net16920
vss!
vss!
ldr:1u
wdr=6u
10u/10u
M143
"nch"
ldr=10u
wdr=10u

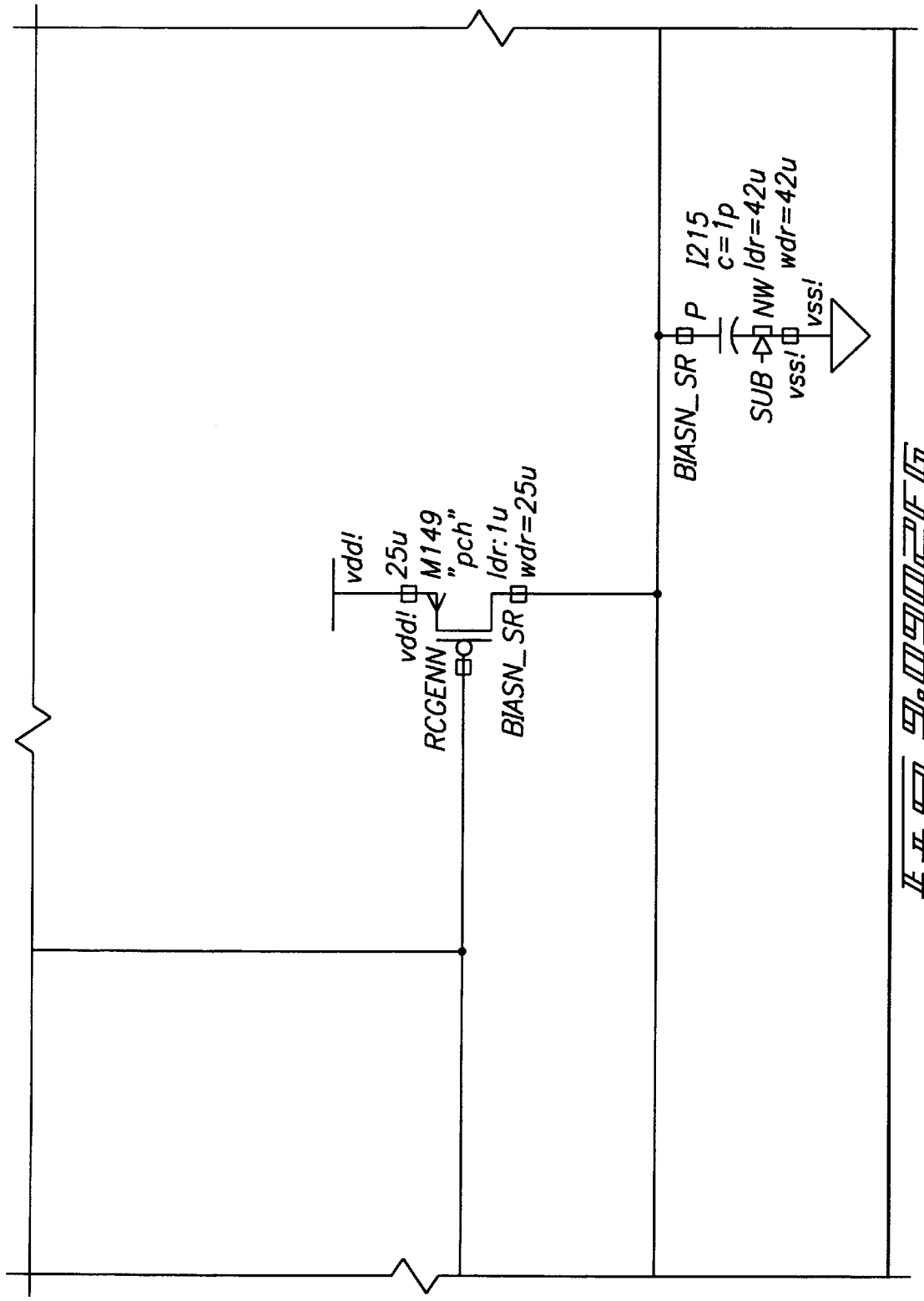


FIG 9.0900F 09

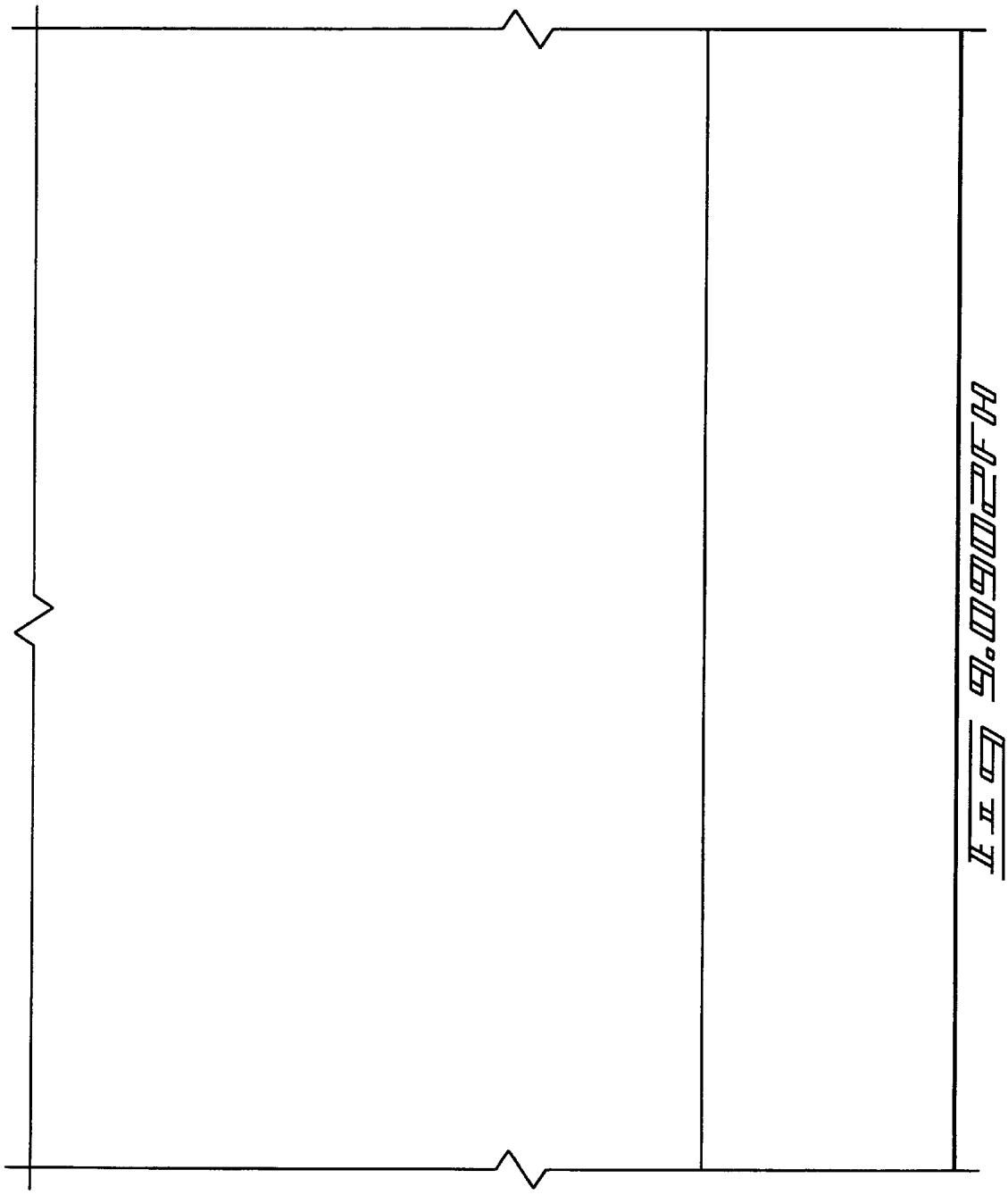


FIG 9606.6

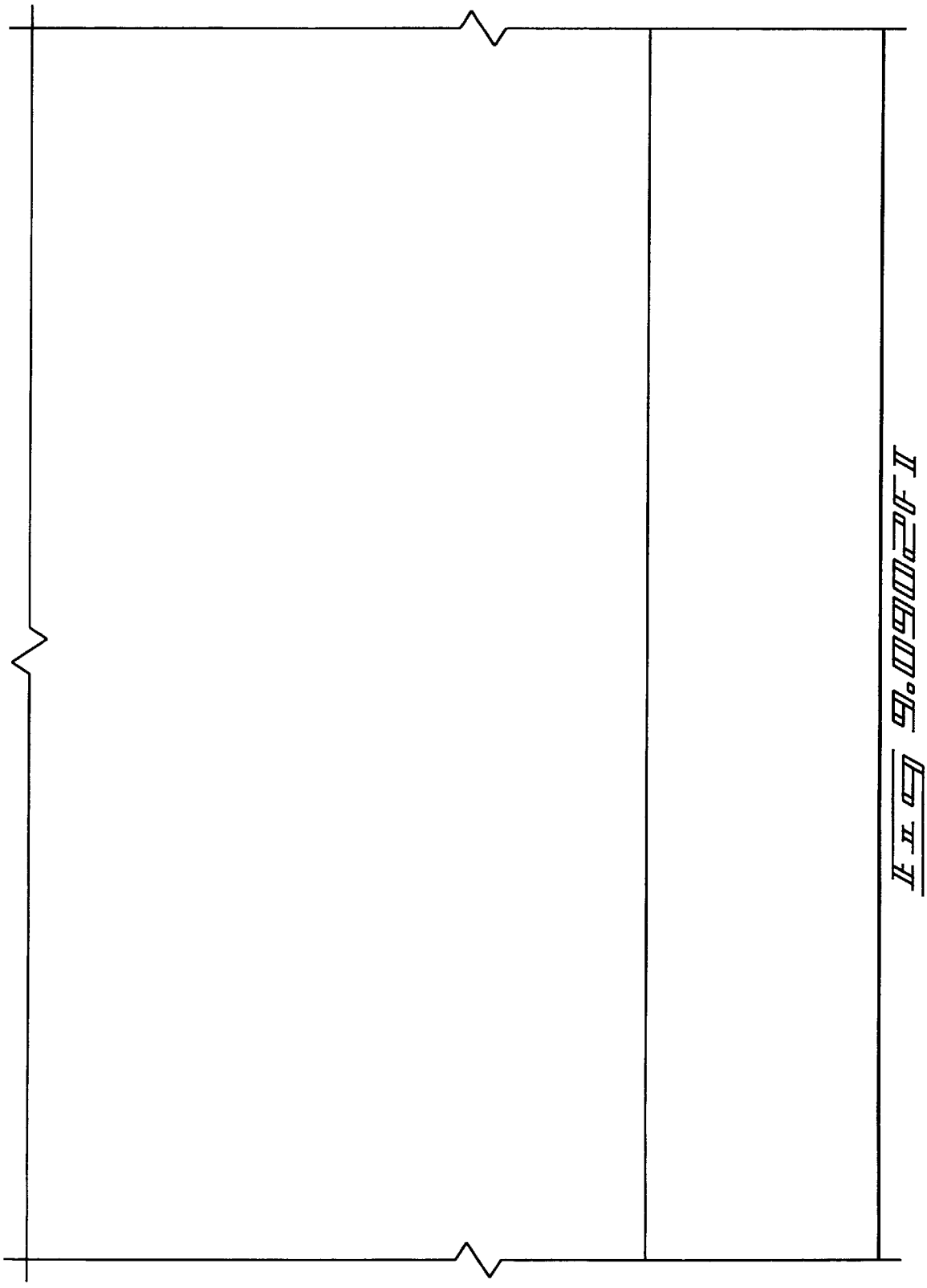


FIG 96

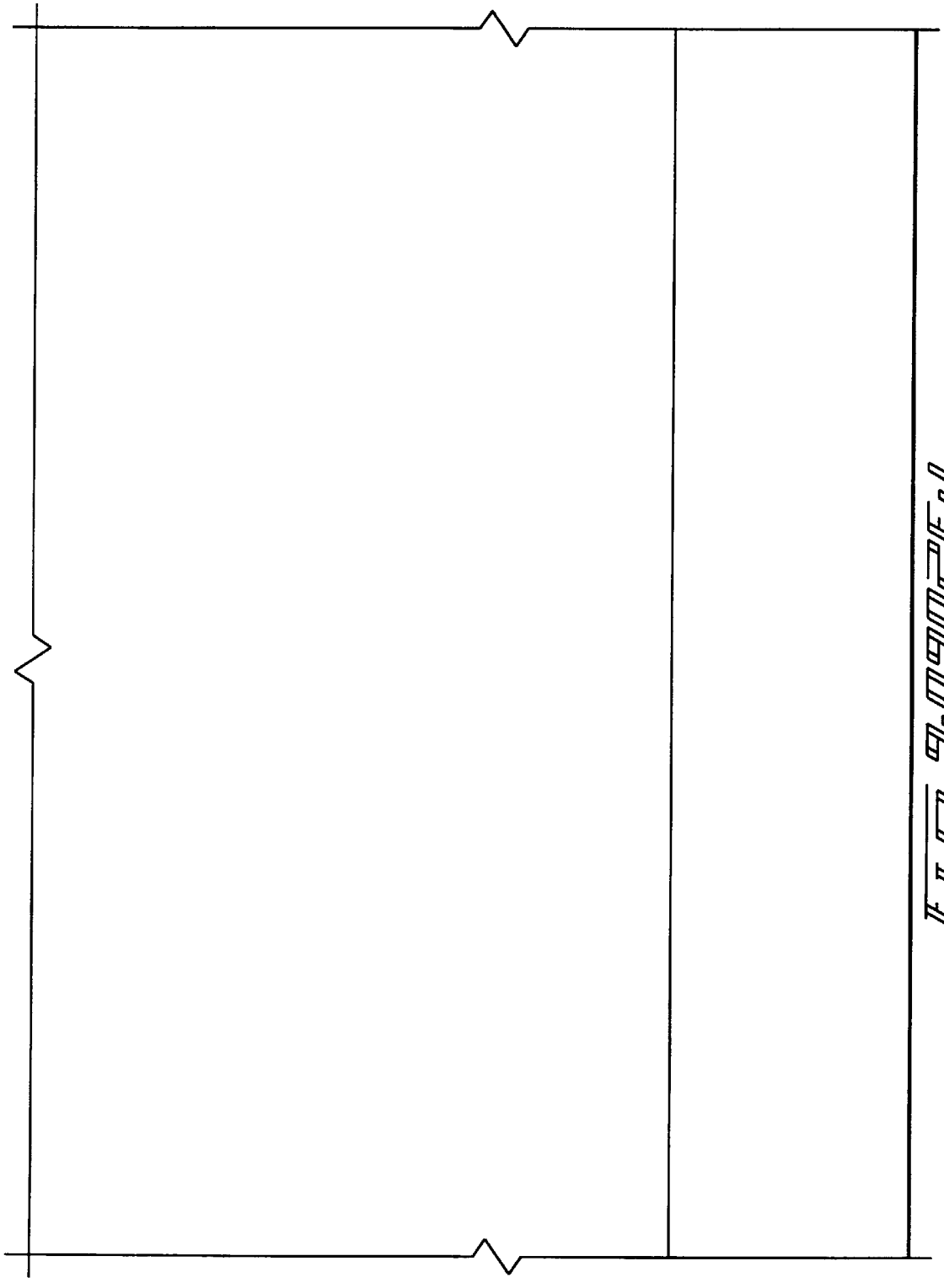


FIG 9,090,275

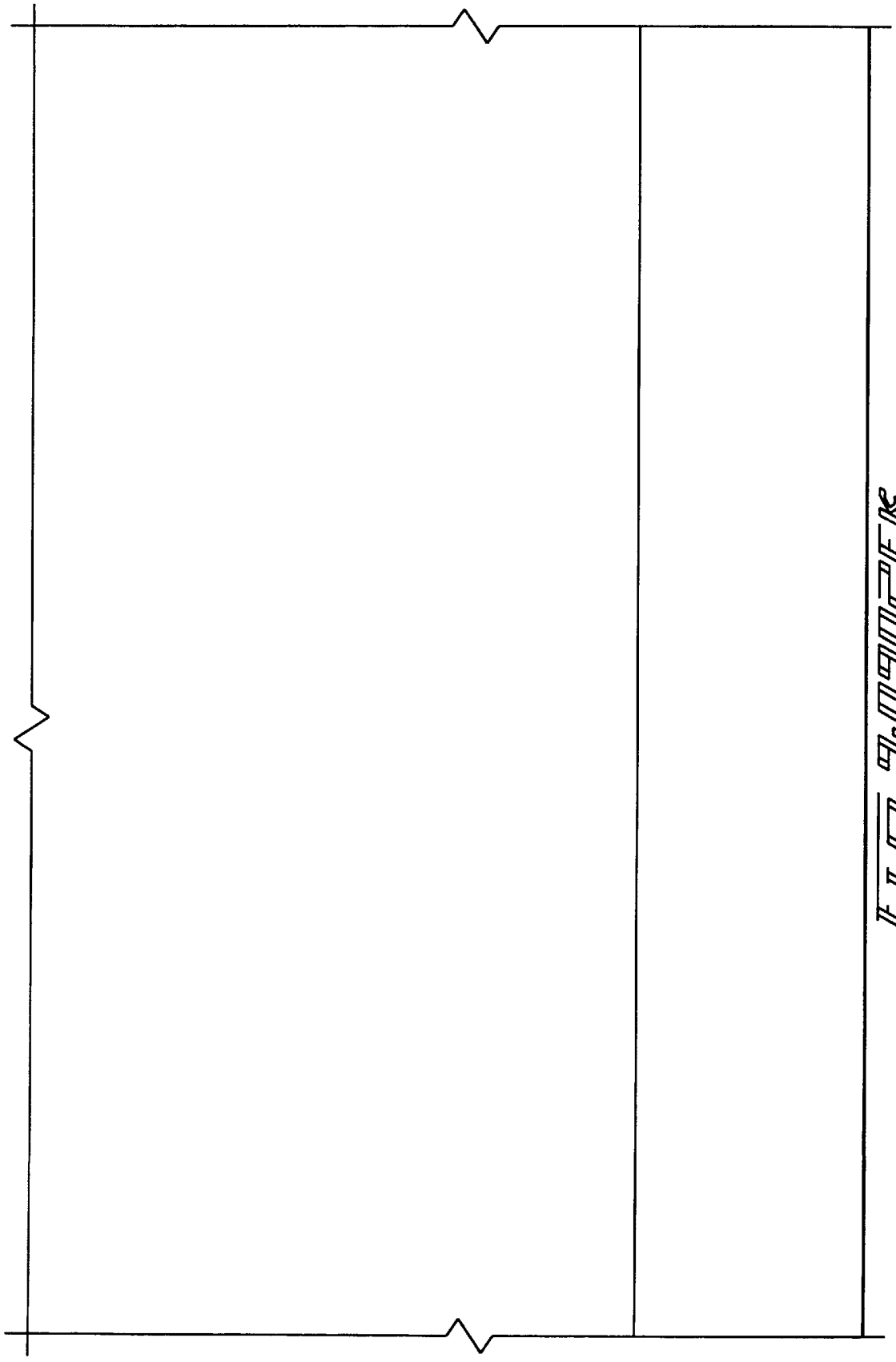
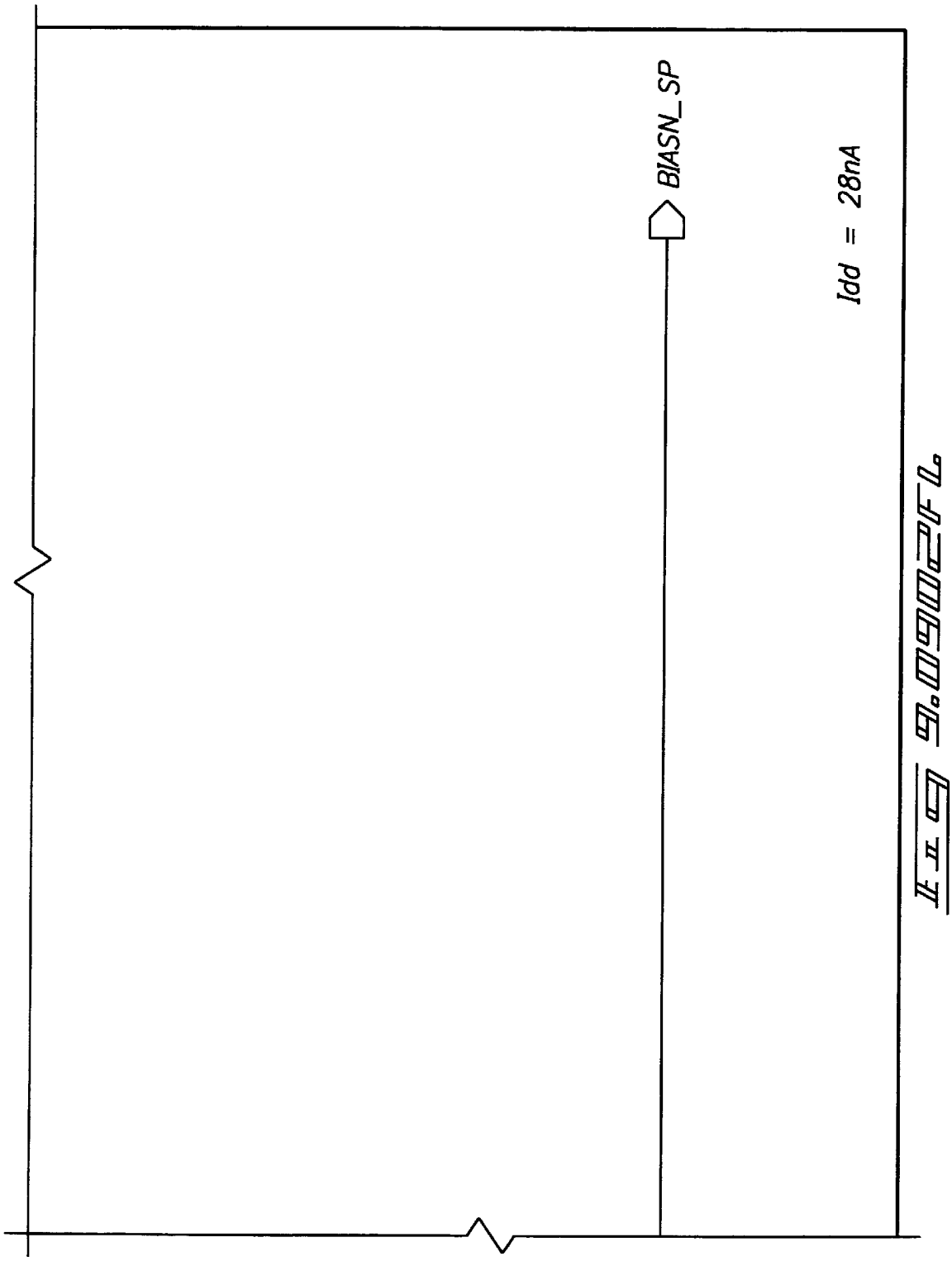


FIG 9,090,278


BIASN_SP
Idd = 28nA
FIG. 9,060

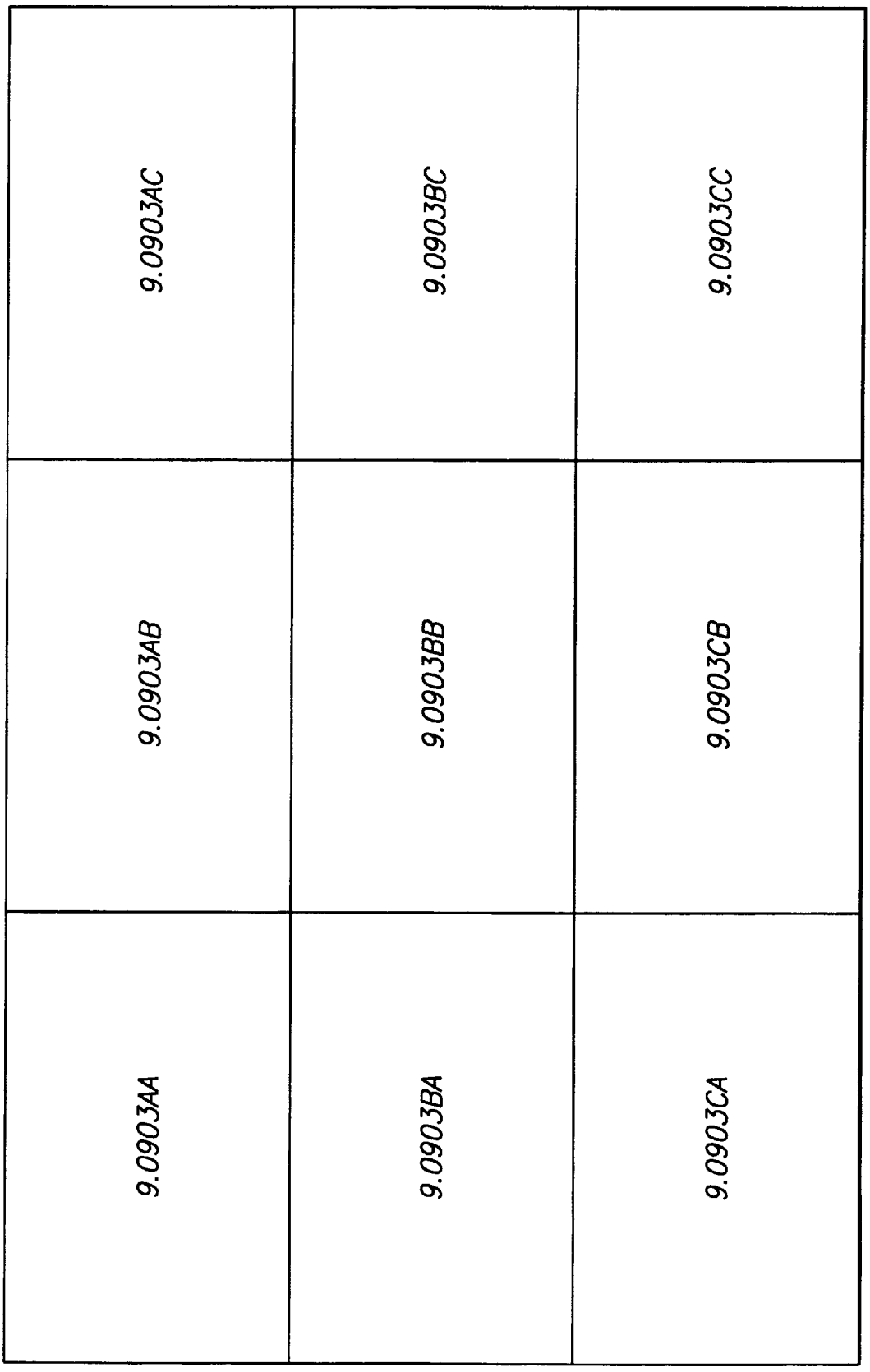
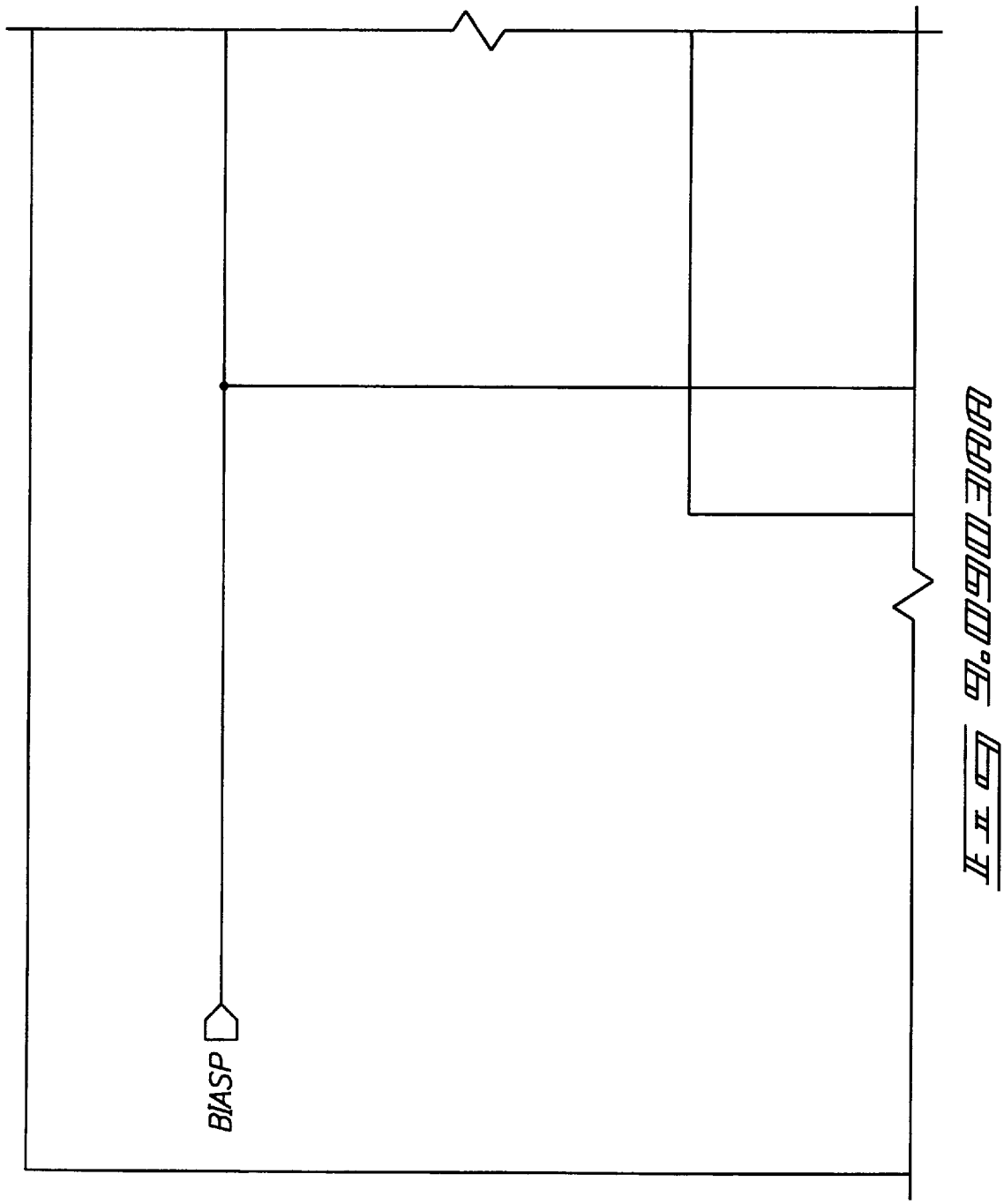

9.0903AC
9.0903BC
9.0903CC
9.0903AB
9.0903BB
9.0903CB
9.0903AA
9.0903BA
9.0903CA

FIG. 9.0903


BIASP
AGND_MGM96_EXT

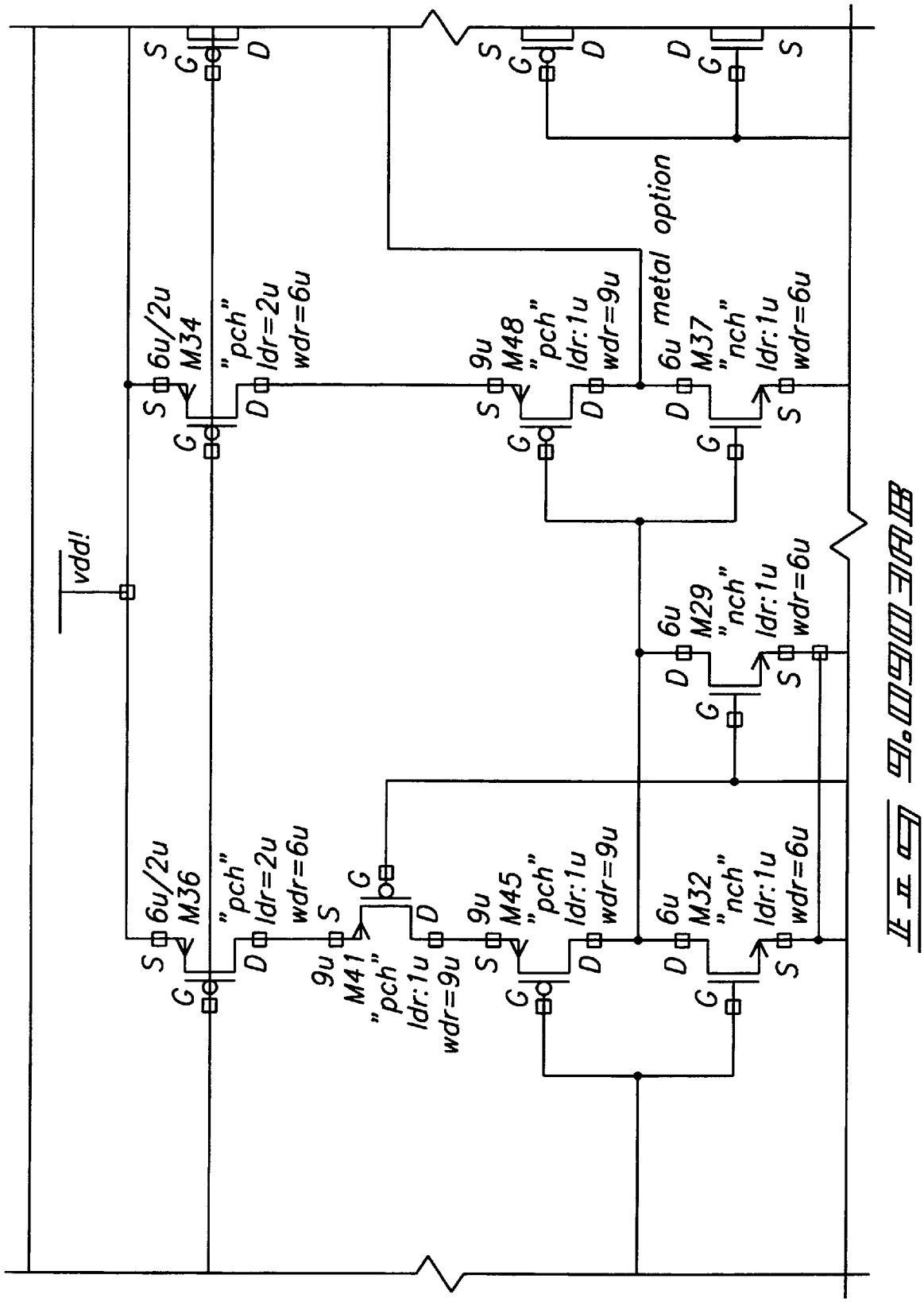
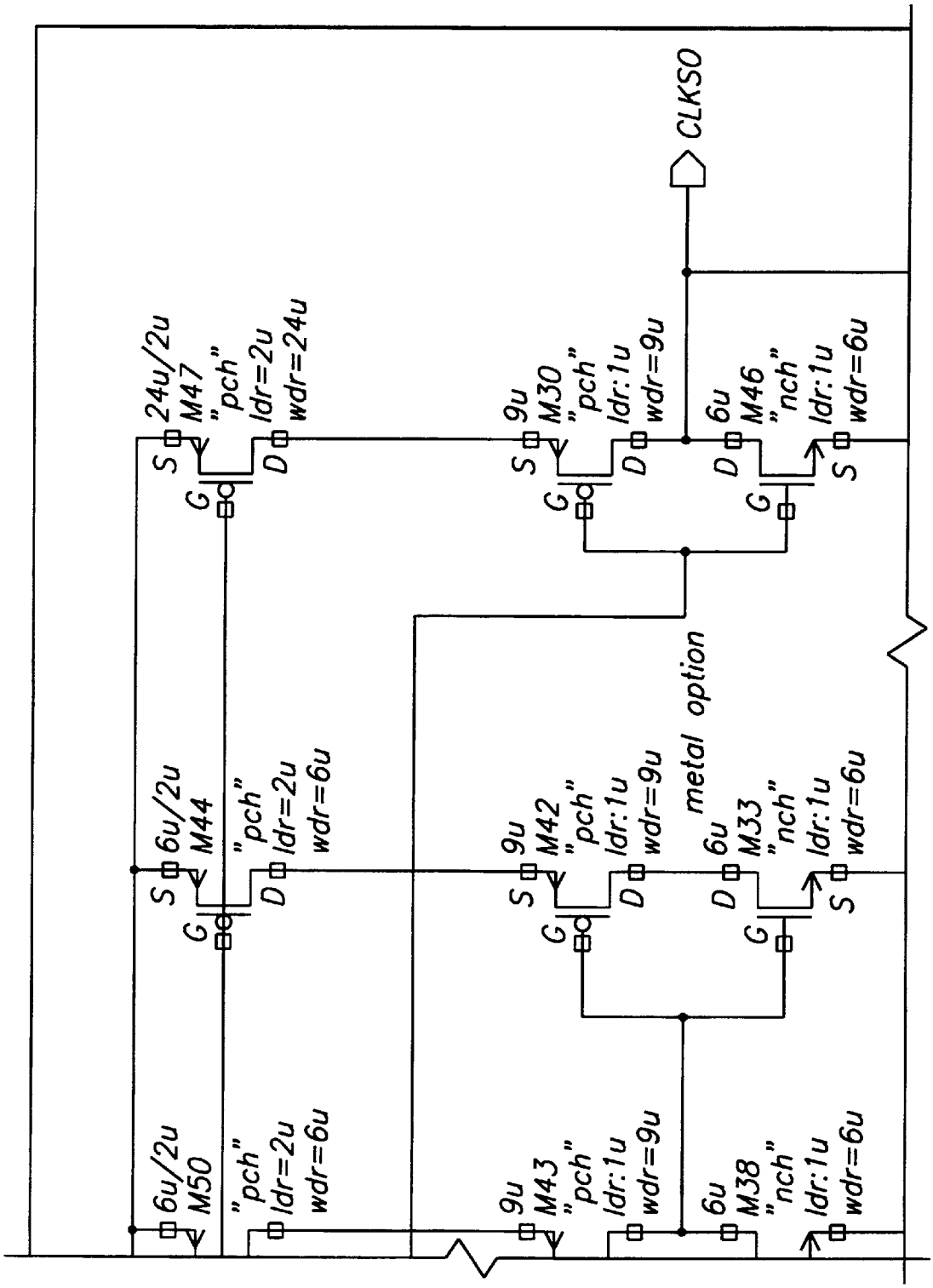

vdd!
6u/2u M34 "pch" ldr=2u wdr=6u
9u M48 "pch" ldr:1u wdr=9u
6u metal option
6u M37 "nch" ldr:1u wdr=6u
6u M29 "nch" ldr:1u wdr=6u
6u/2u M36 "pch" ldr=2u wdr=6u
9u M41 "pch" ldr:1u wdr=9u
9u M45 "pch" ldr:1u wdr=9u
6u M32 "nch" ldr:1u wdr=6u

FIG 2784


CLKSO
24u/2u M47 "pch" ldr=2u wdr=24u
9u M30 "pch" ldr:1u wdr=9u
6u M46 "nch" ldr:1u wdr=6u
6u/2u M44 "pch" ldr=2u wdr=6u
9u M42 "pch" ldr:1u wdr=9u
6u M33 "nch" ldr:1u wdr=6u
6u/2u M50 "pch" ldr=2u wdr=6u
9u M43 "pch" ldr:1u wdr=9u
6u M38 "nch" ldr:1u wdr=6u
metal option
S
D
G

Фиг 9.0506

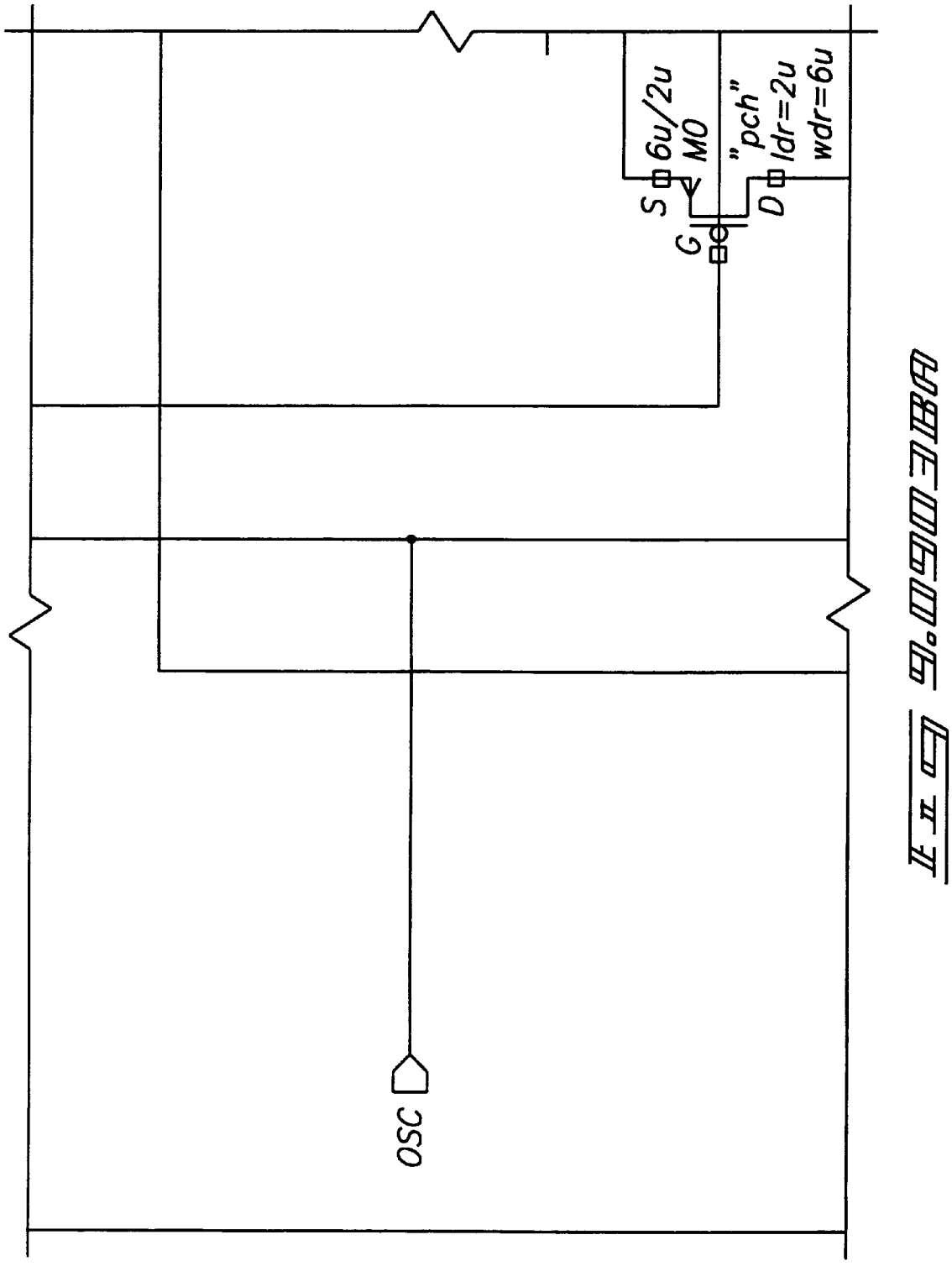


FIG 2786

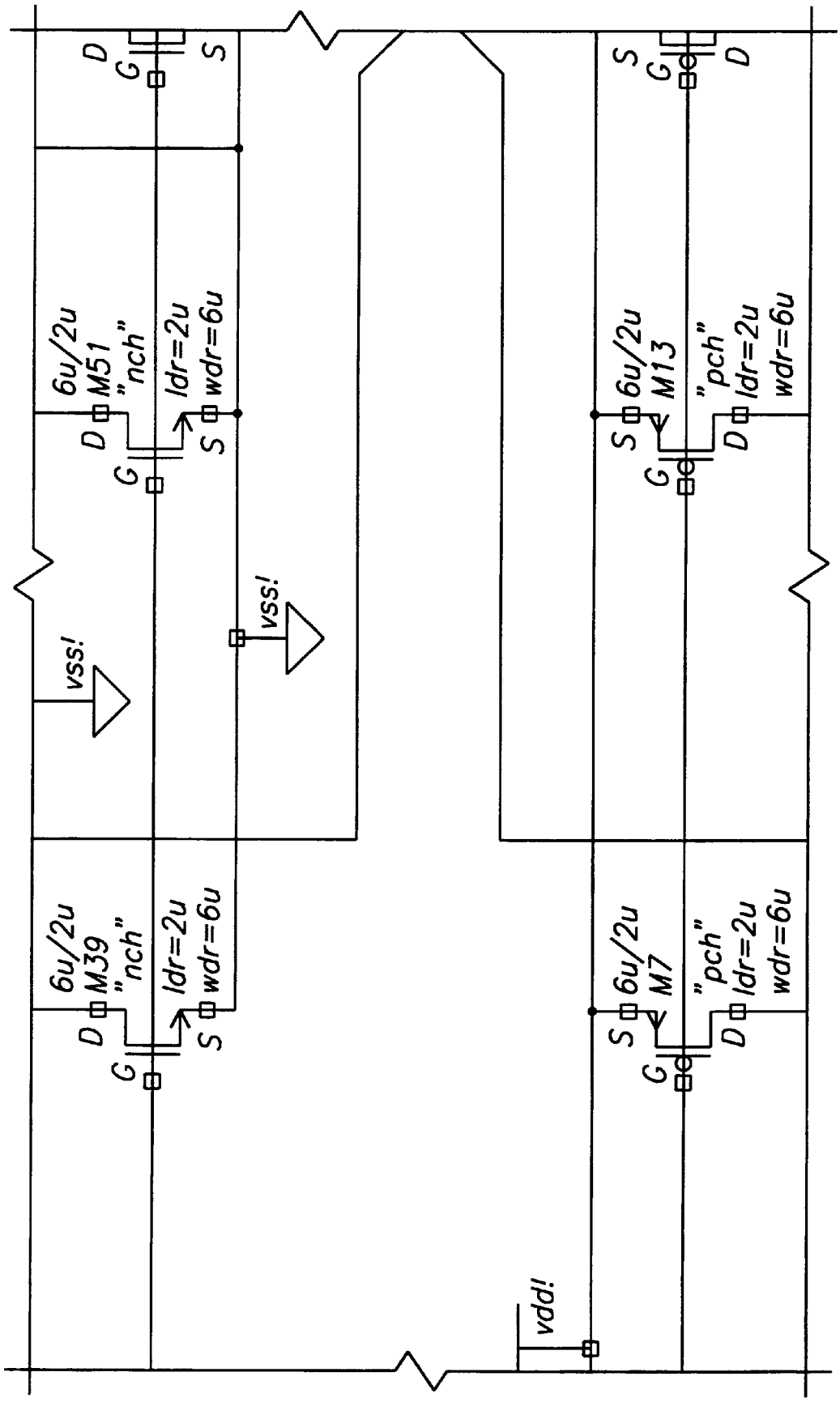
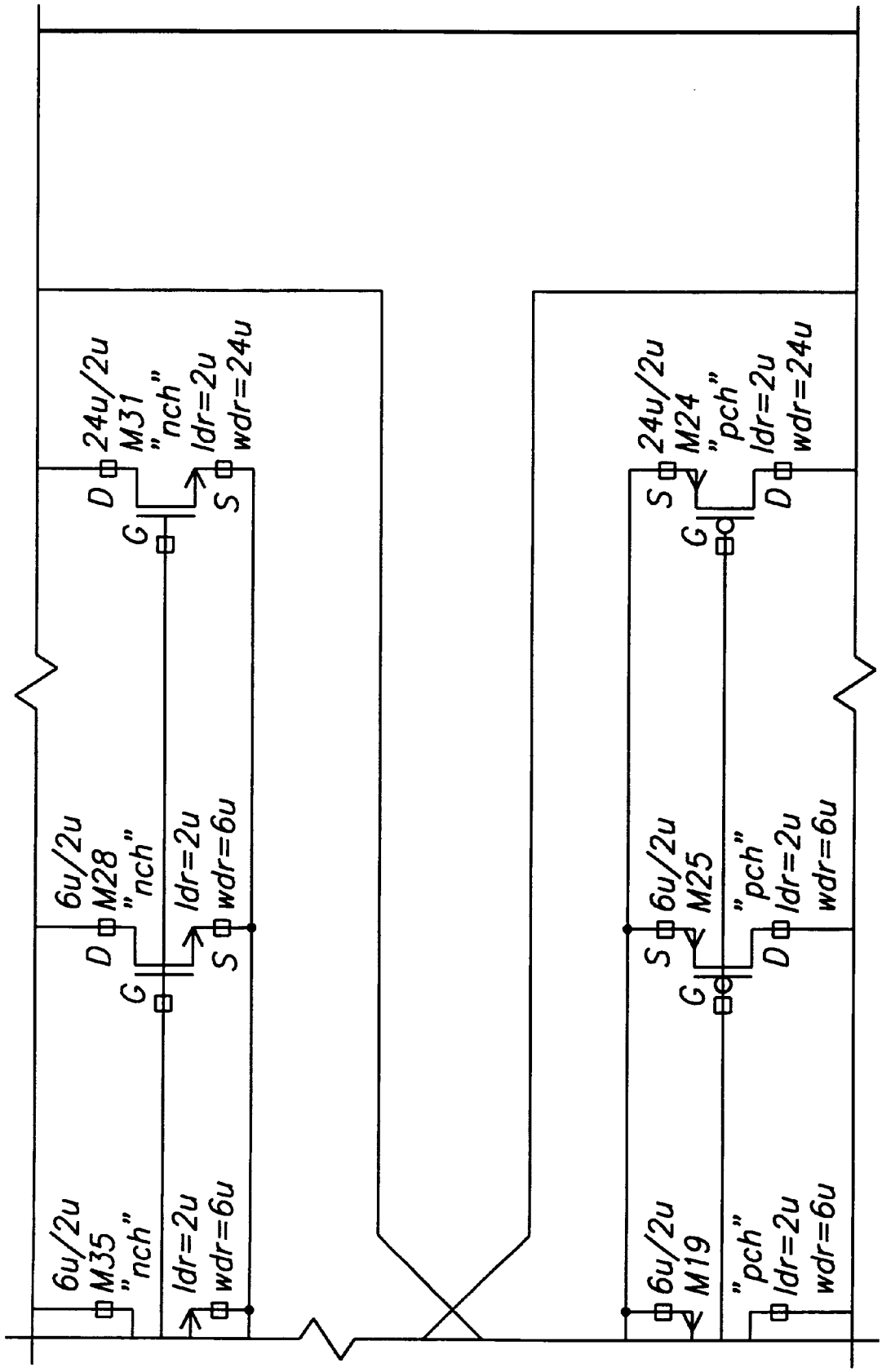

6u/2u
M51
"nch"
ldr=2u
wdr=6u
6u/2u
M13
"pch"
ldr=2u
wdr=6u
6u/2u
M39
"nch"
ldr=2u
wdr=6u
6u/2u
M7
"pch"
ldr=2u
wdr=6u
vss!
vss!
vdd!
D
G
S

FIG 2787


24u/2u
M31
"nch"
ldr=2u
wdr=24u
D
G
S
6u/2u
M28
"nch"
ldr=2u
wdr=6u
6u/2u
M35
"nch"
ldr=2u
wdr=6u
24u/2u
M24
"pch"
ldr=2u
wdr=24u
6u/2u
M25
"pch"
ldr=2u
wdr=6u
6u/2u
M19
"pch"
ldr=2u
wdr=6u

ФИГ. 2788

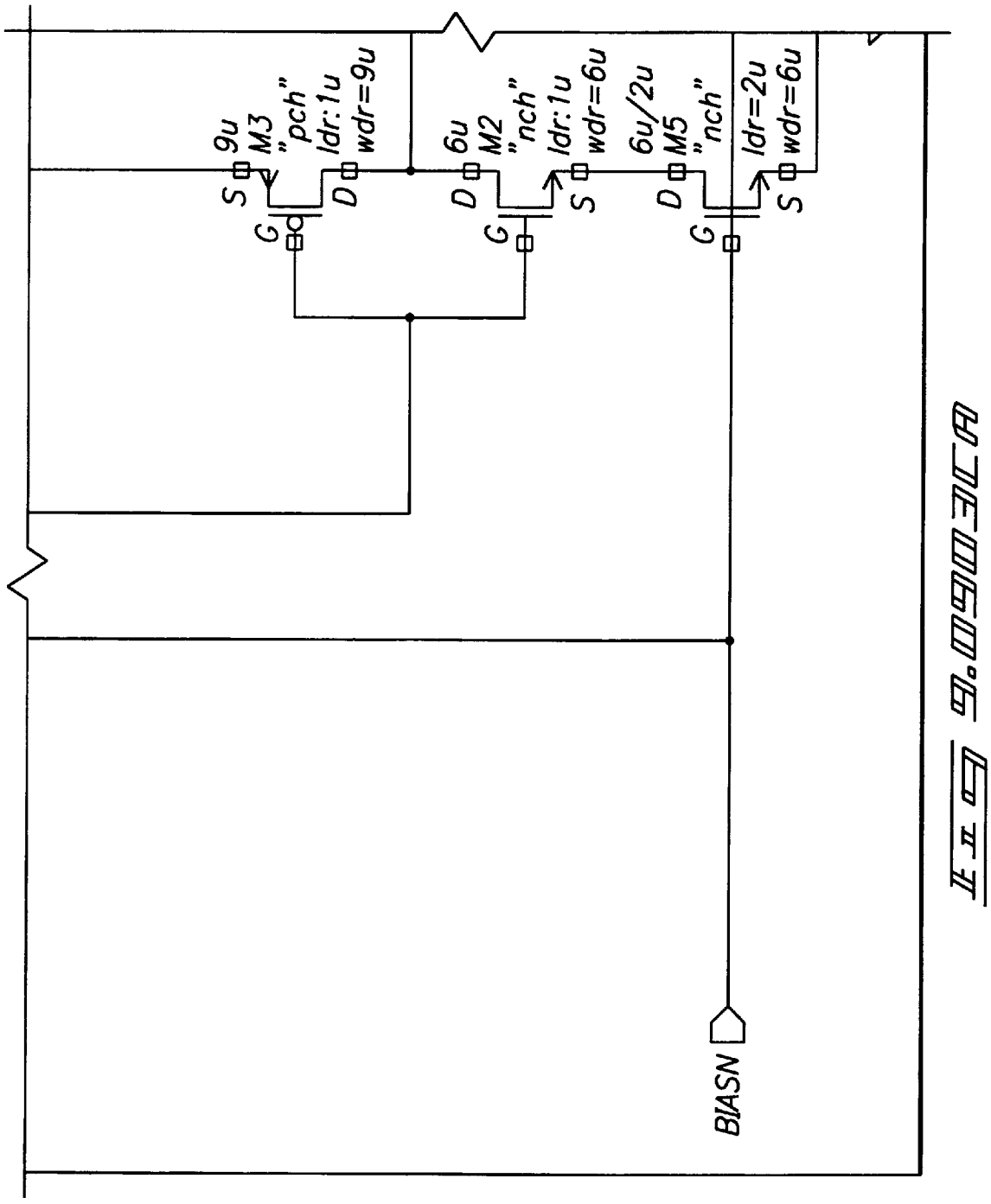

9u
M3
"pch"
ldr:1u
wdr=9u
6u
M2
"nch"
ldr:1u
wdr=6u
6u/2u
M5
"nch"
ldr=2u
wdr=6u
S
D
G
BIASN

FIG 9,130,602

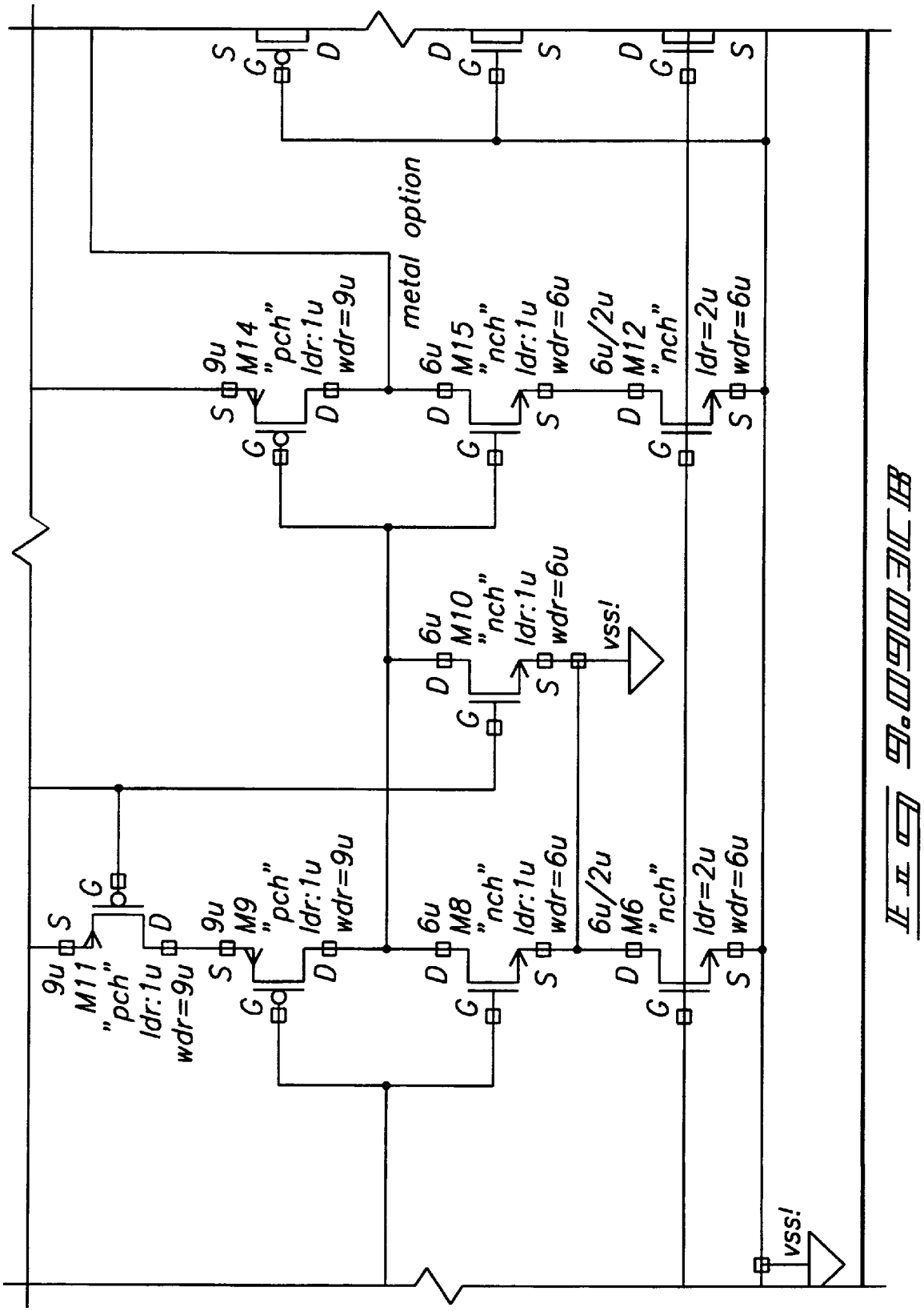

metal option
9u M14 "pch" ldr:1u wdr=9u
6u M15 "nch" ldr:1u wdr=6u
6u/2u M12 "nch" ldr=2u wdr=6u
6u M10 "nch" ldr:1u wdr=6u
vss!
9u M11 "pch" ldr:1u wdr=9u
9u M9 "pch" ldr:1u wdr=9u
6u M8 "nch" ldr:1u wdr=6u
6u/2u M6 "nch" ldr=2u wdr=6u
vss!

FIG 6,130,602

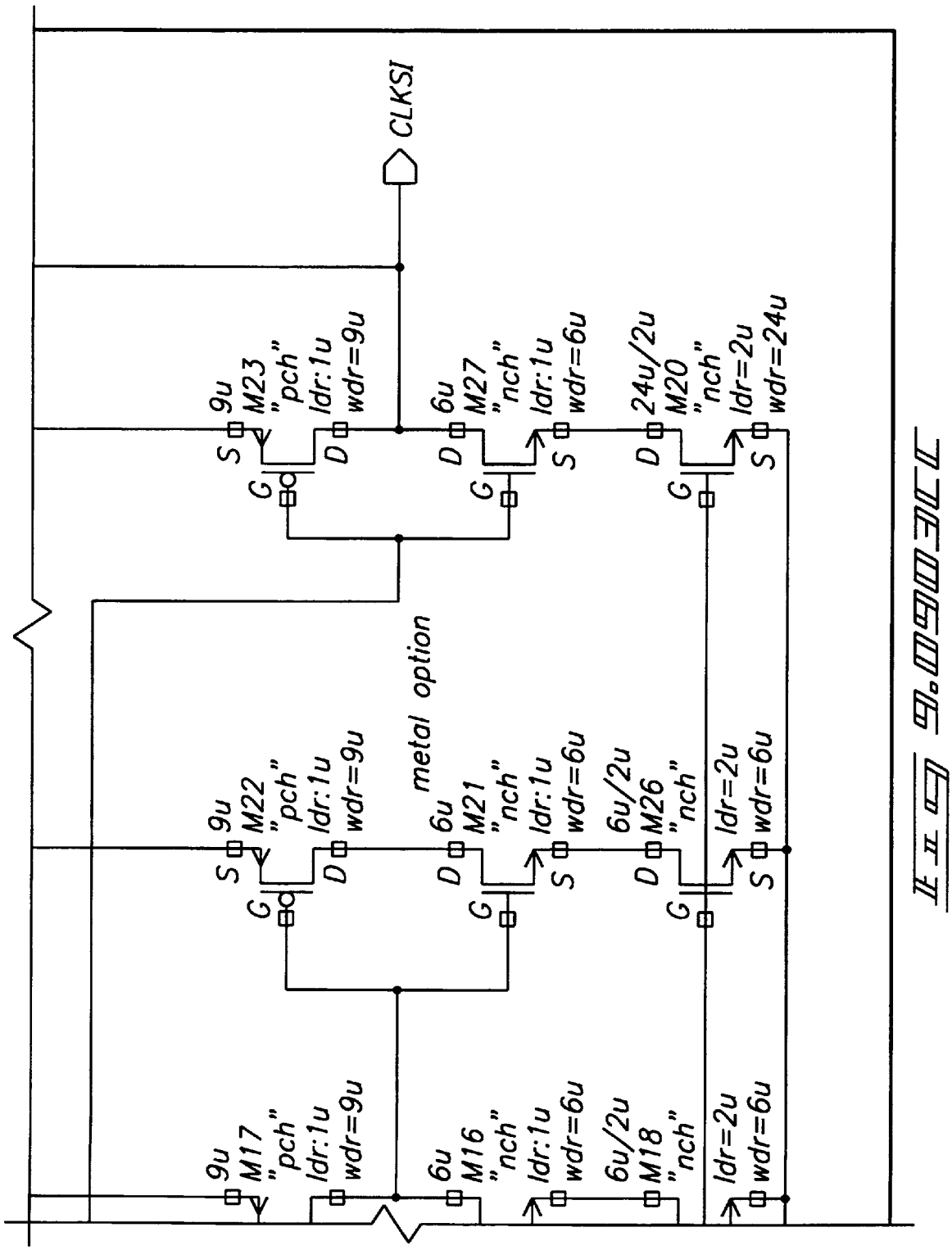

CLKSI
9u M23 "pch" ldr:1u wdr=9u
6u M27 "nch" ldr:1u wdr=6u
24u/2u M20 "nch" ldr=2u wdr=24u
metal option
9u M22 "pch" ldr:1u wdr=9u
6u M21 "nch" ldr:1u wdr=6u
6u/2u M26 "nch" ldr=2u wdr=6u
9u M17 "pch" ldr:1u wdr=9u
6u M16 "nch" ldr:1u wdr=6u
6u/2u M18 "nch" ldr=2u wdr=6u
S
D
G

FIG 9,060,16

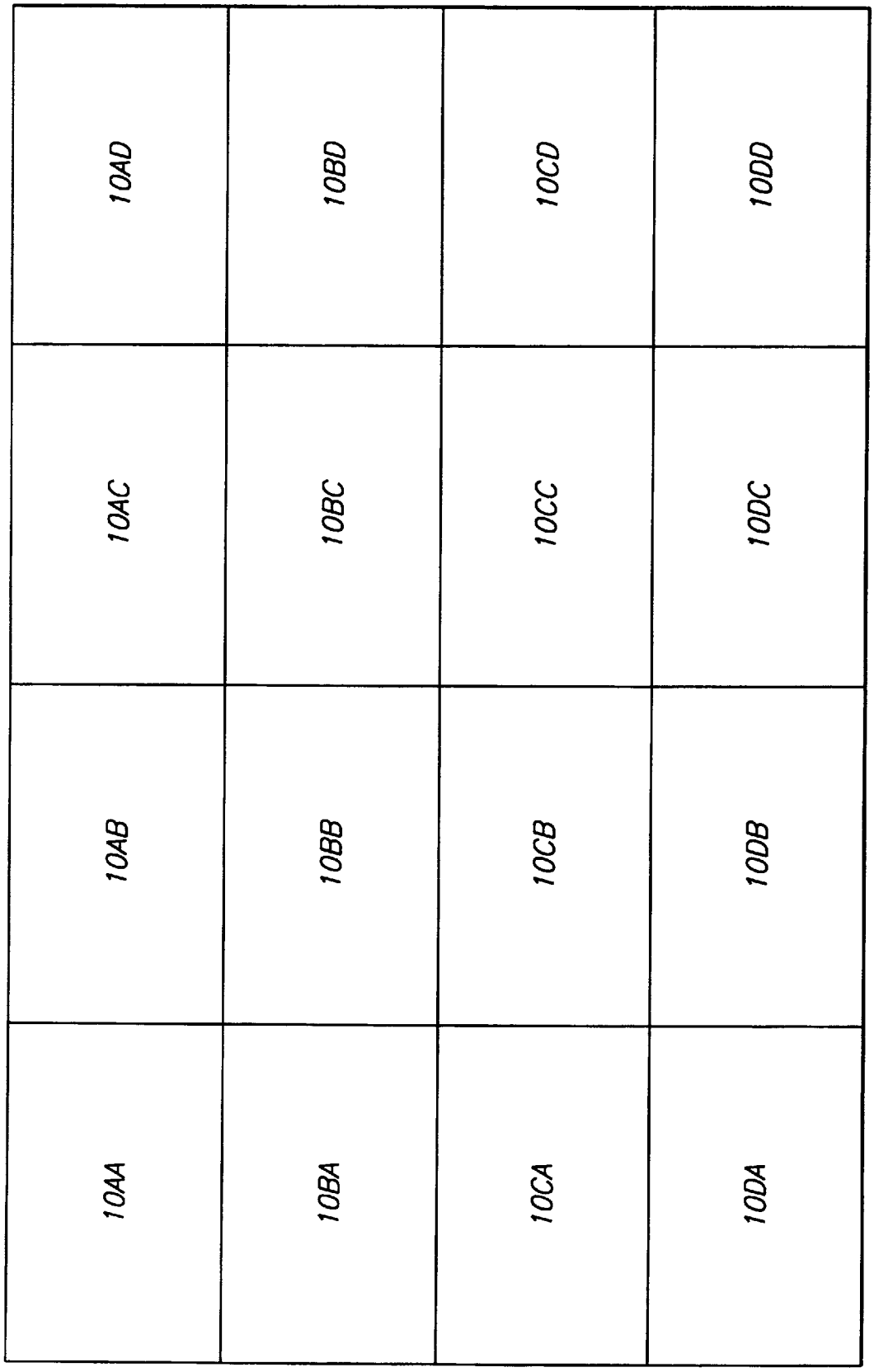
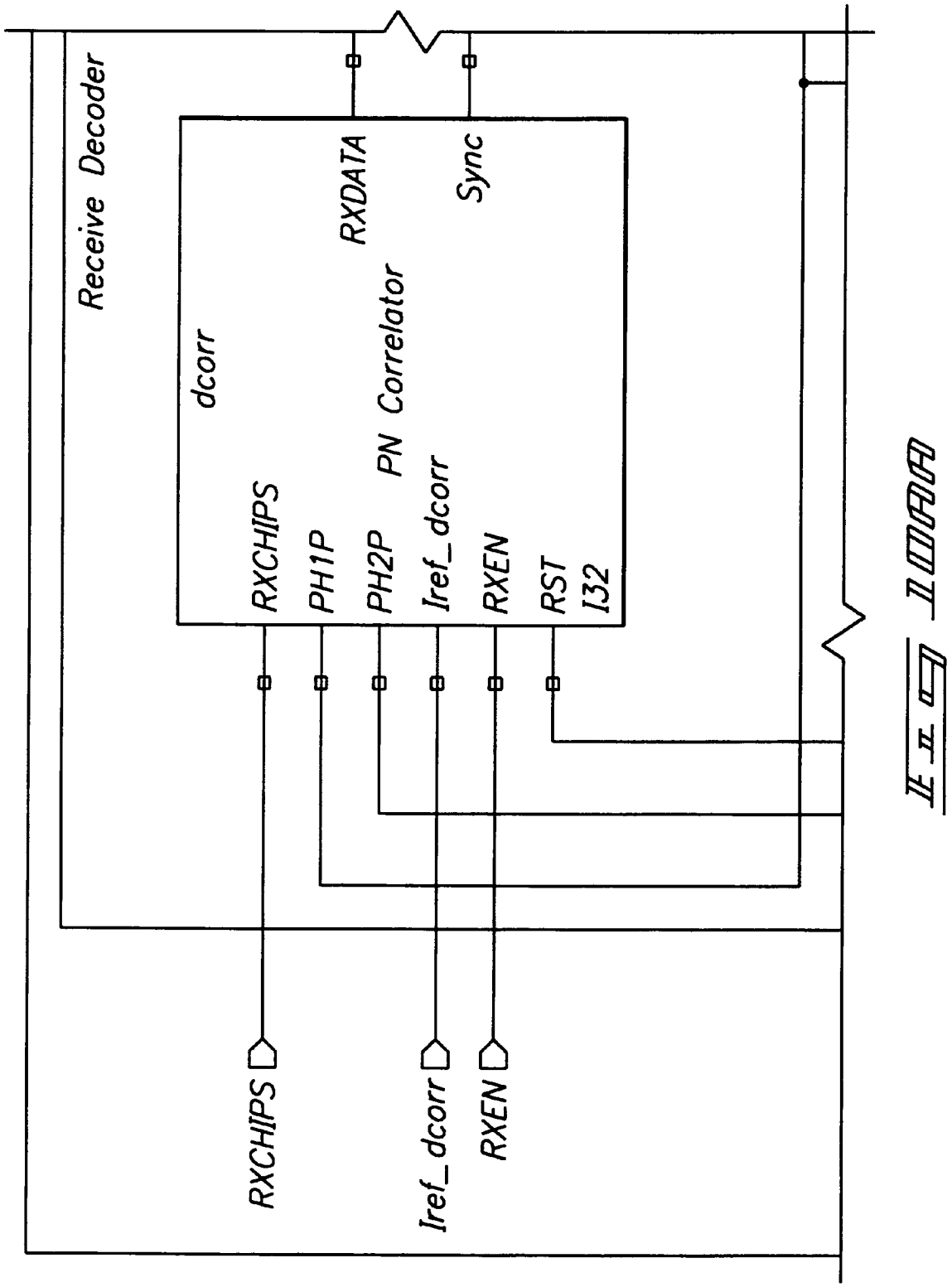

10AD
10BD
10CD
10DD
10AC
10BC
10CC
10DC
10AB
10BB
10CB
10DB
10AA
10BA
10CA
10DA

FIG 111


Receive Decoder
dcorr
PN Correlator
RXDATA
Sync
RXCHIPS
PH1P
PH2P
Iref_dcorr
RXEN
RST
I32
RXCHIPS
Iref_dcorr
RXEN

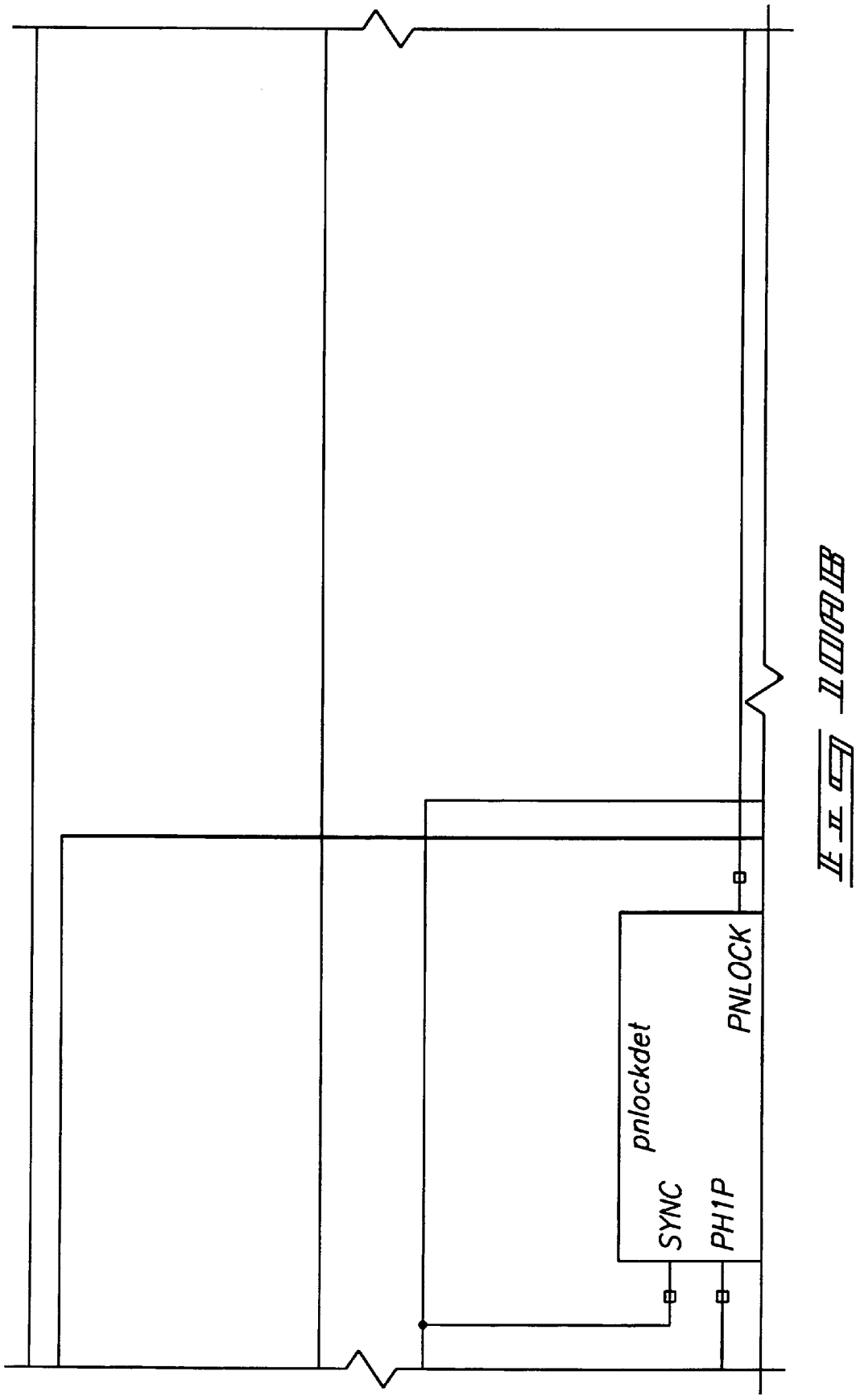


FIG 1008

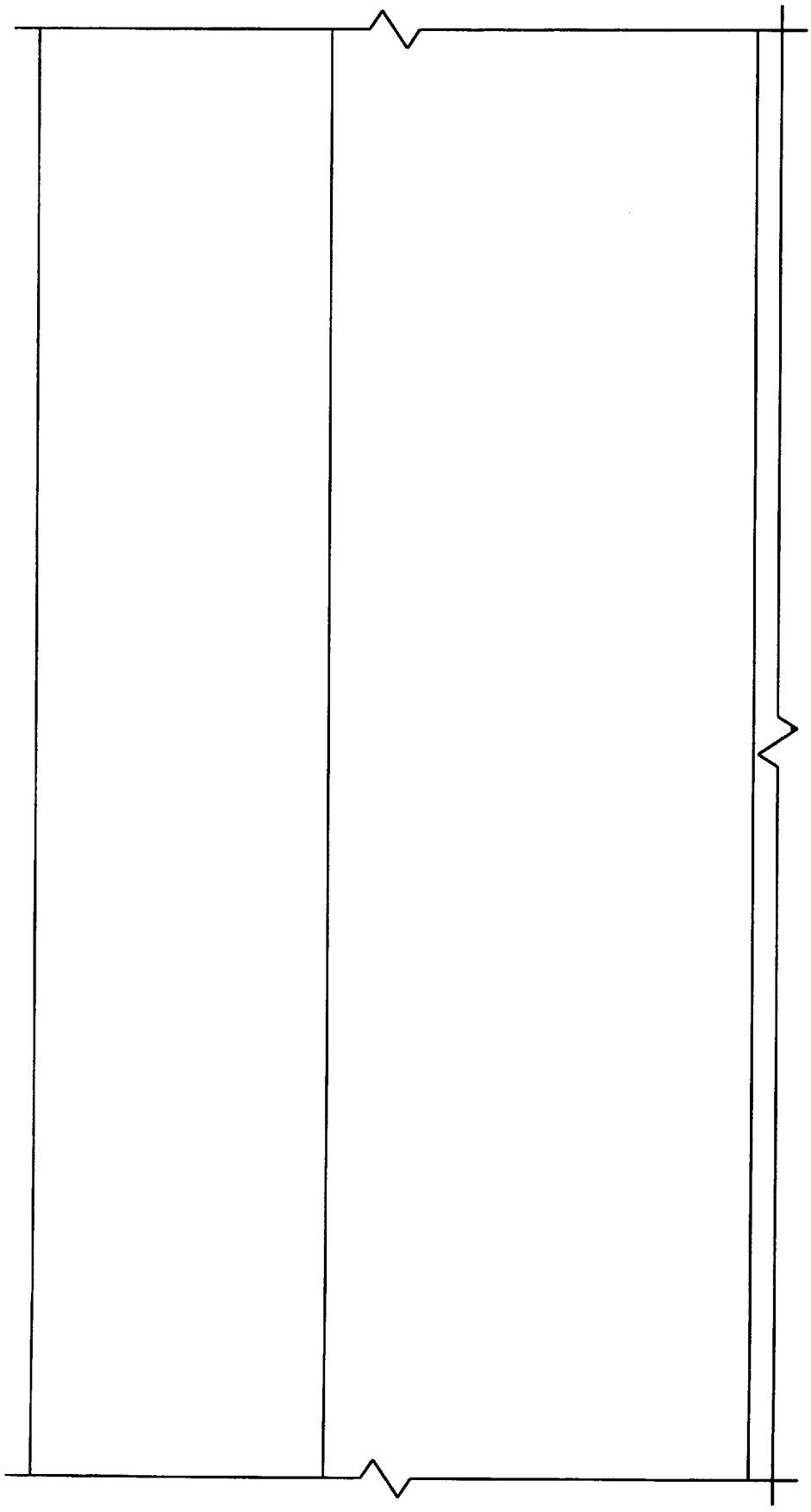
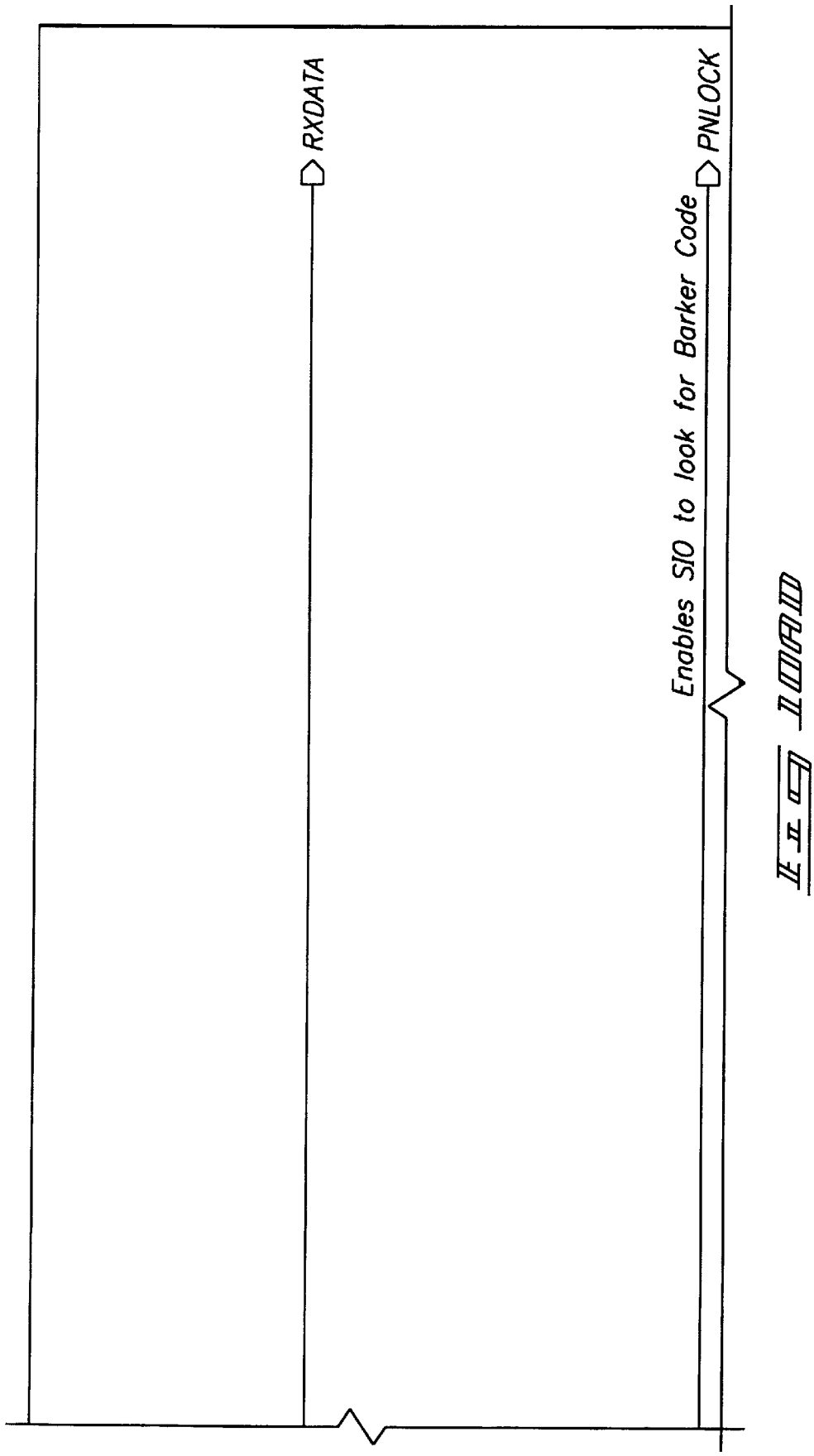
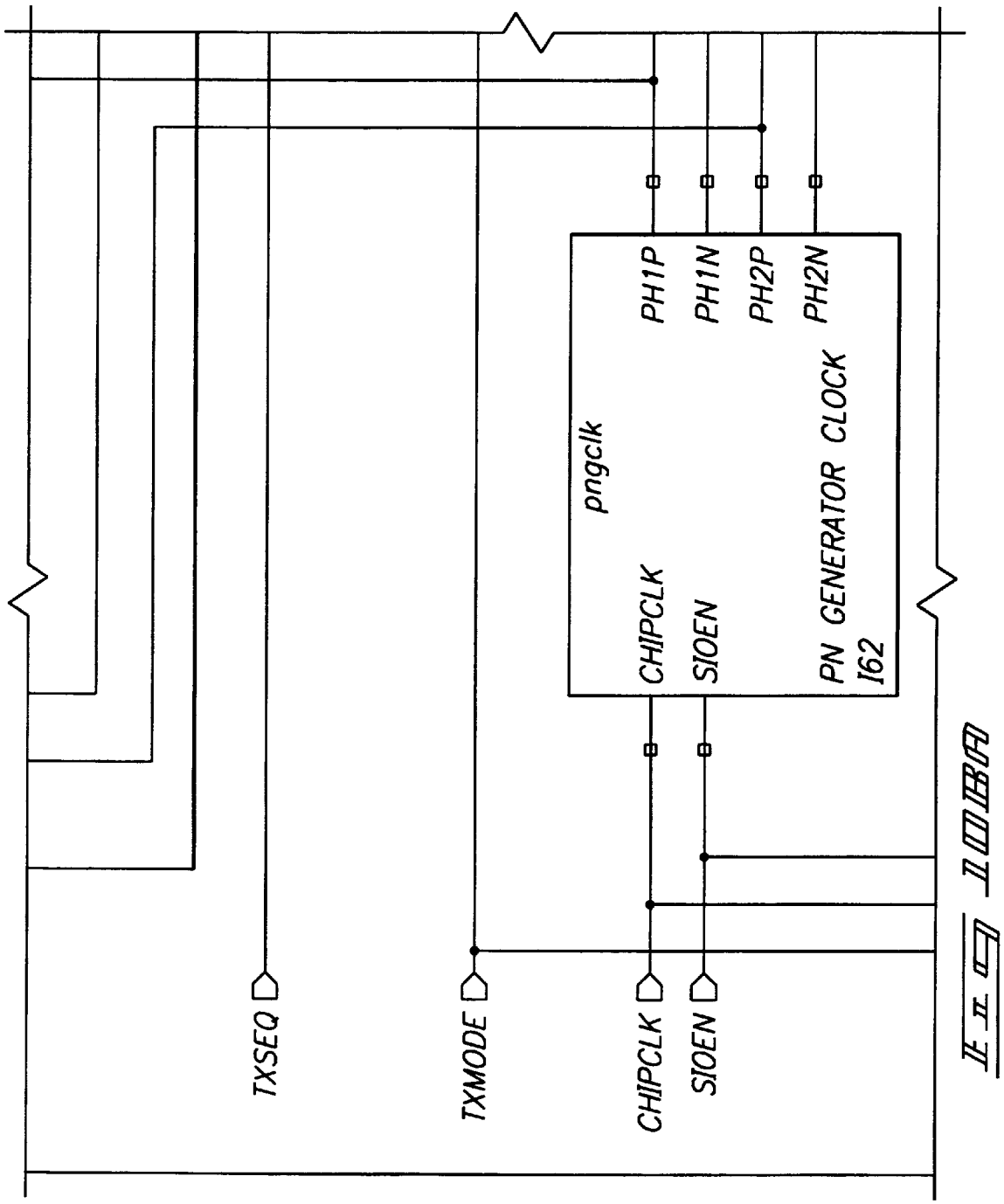


FIG 1004


RXDATA
PNLOCK
Enables SIO to look for Barker Code
FIG 1004


PH1P
PH1N
PH2P
PH2N
pngclk
CHIPCLK
SIOEN
PN GENERATOR CLOCK
I62
TXSEQ
TXMODE
CHIPCLK
SIOEN
FIG 1003A

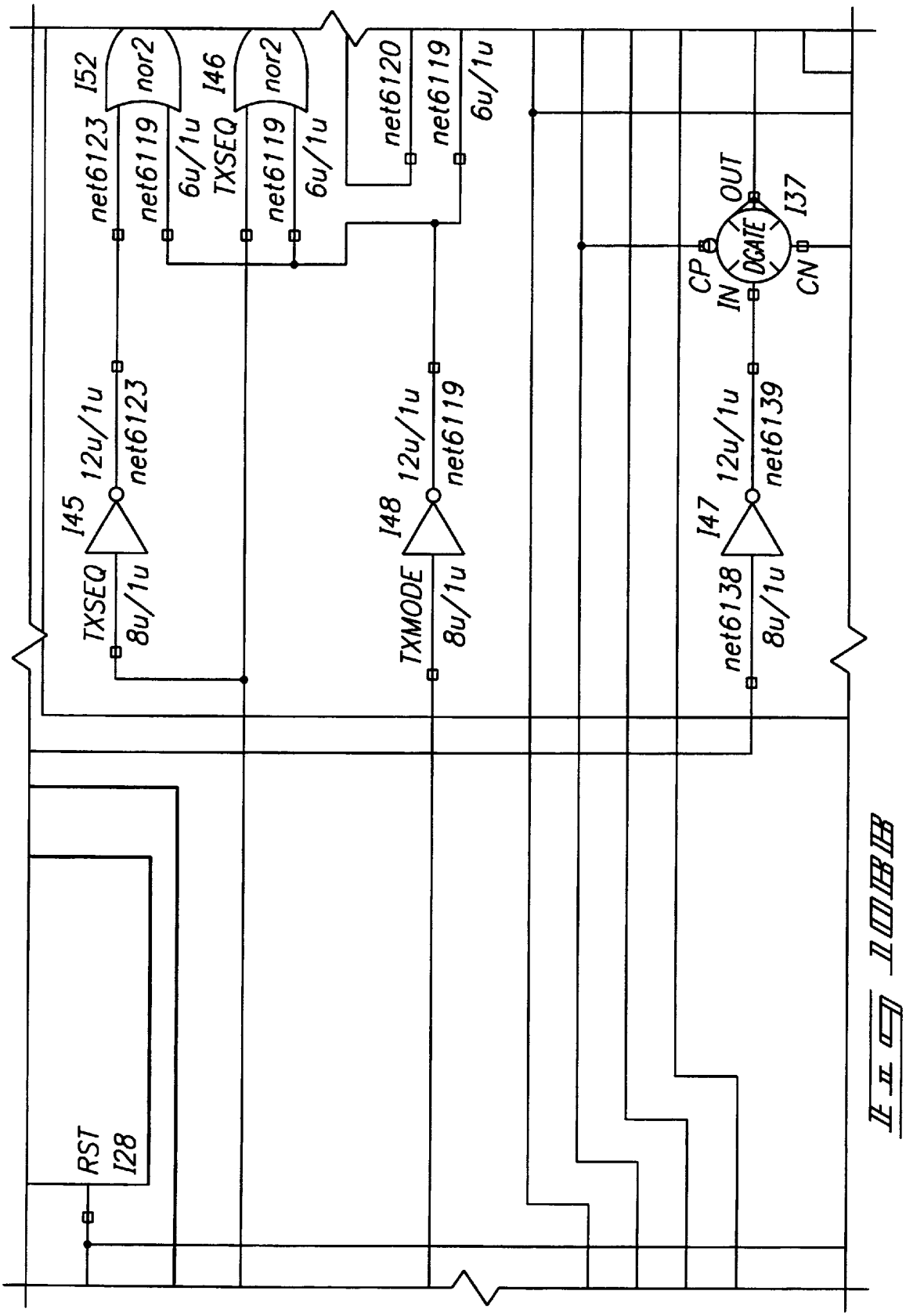
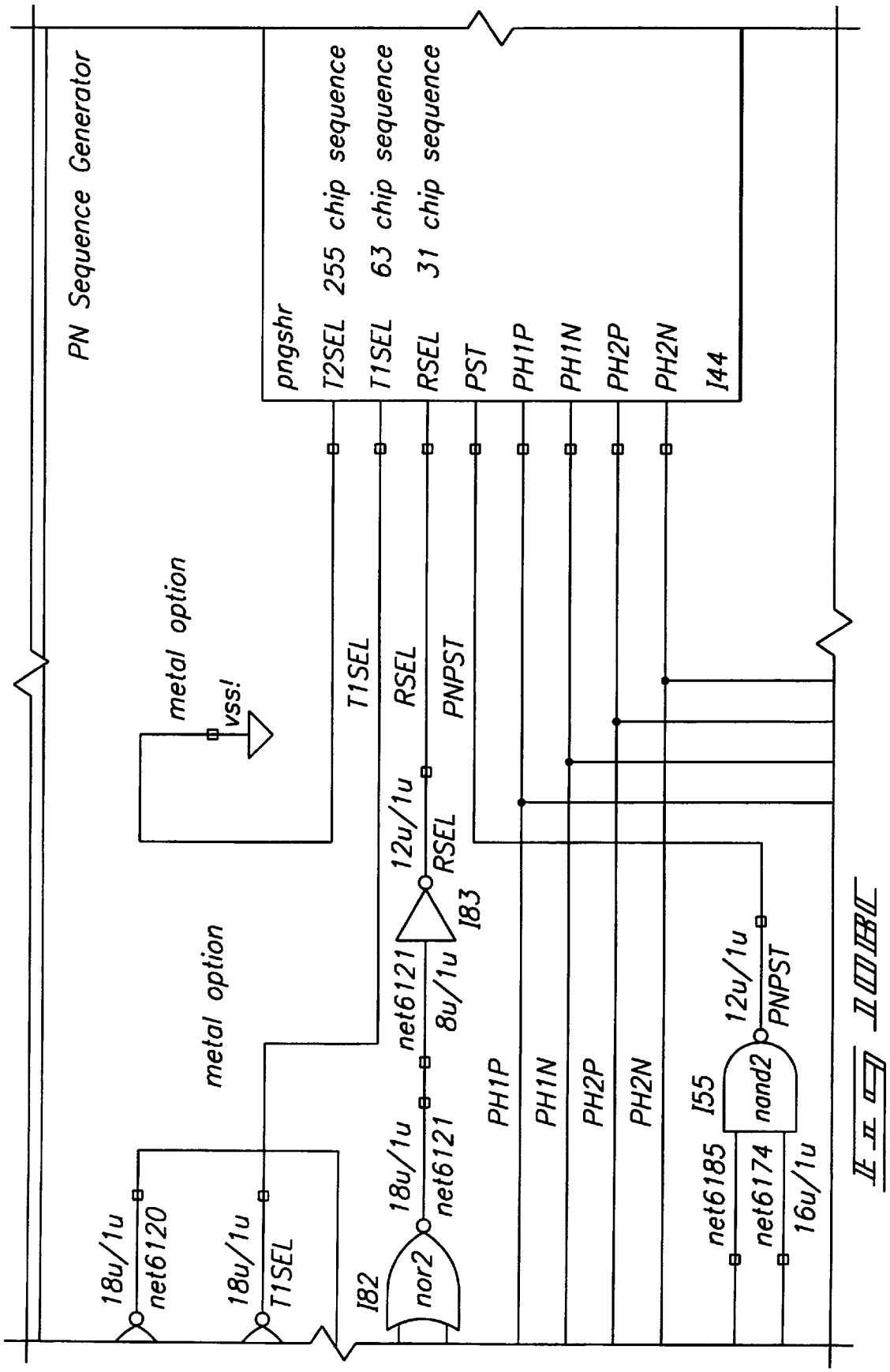

I52
nor2
net6123
net6119
6u/1u
I46
nor2
TXSEQ
net6119
6u/1u
net6120
net6119
6u/1u
OUT
I37
CP
IN
DGATE
CN
I45
12u/1u
net6123
TXSEQ
8u/1u
I48
12u/1u
net6119
TXMODE
8u/1u
I47
12u/1u
net6139
net6138
8u/1u
RST
I28

FIG 1008B


PN Sequence Generator
pngshr
T2SEL 255 chip sequence
T1SEL 63 chip sequence
RSEL 31 chip sequence
PST
PH1P
PH1N
PH2P
PH2N
I44
metal option
vss!
T1SEL
RSEL
PNPST
12u/1u
RSEL
I83
net6121
8u/1u
metal option
18u/1u
net6120
18u/1u
T1SEL
I82
nor2
18u/1u
net6121
PH1P
PH1N
PH2P
PH2N
I55
nand2
12u/1u
PNPST
net6185
net6174
16u/1u

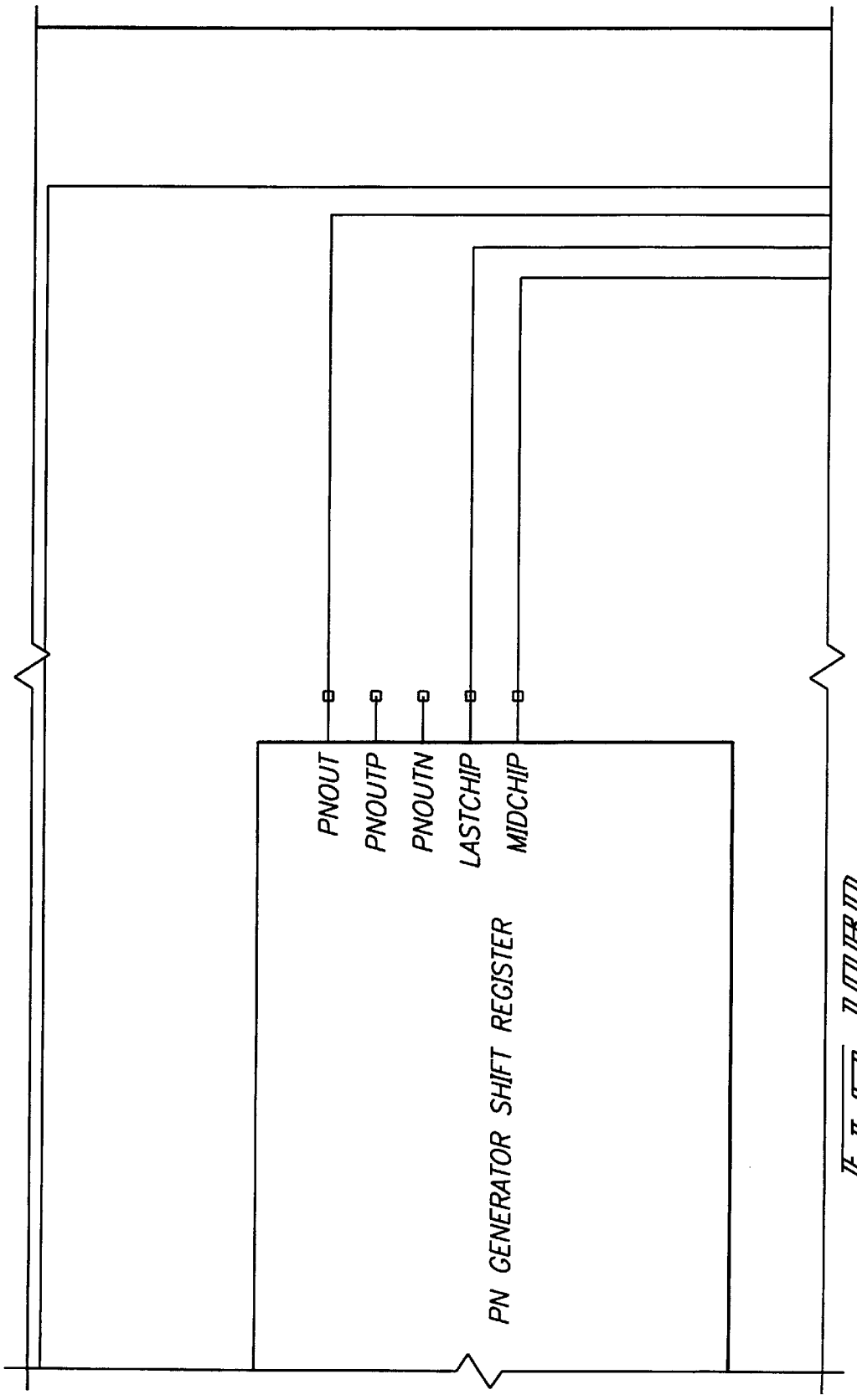

PNOUT
PNOUTP
PNOUTN
LASTCHIP
MIDCHIP
PN GENERATOR SHIFT REGISTER

FIG 1100B

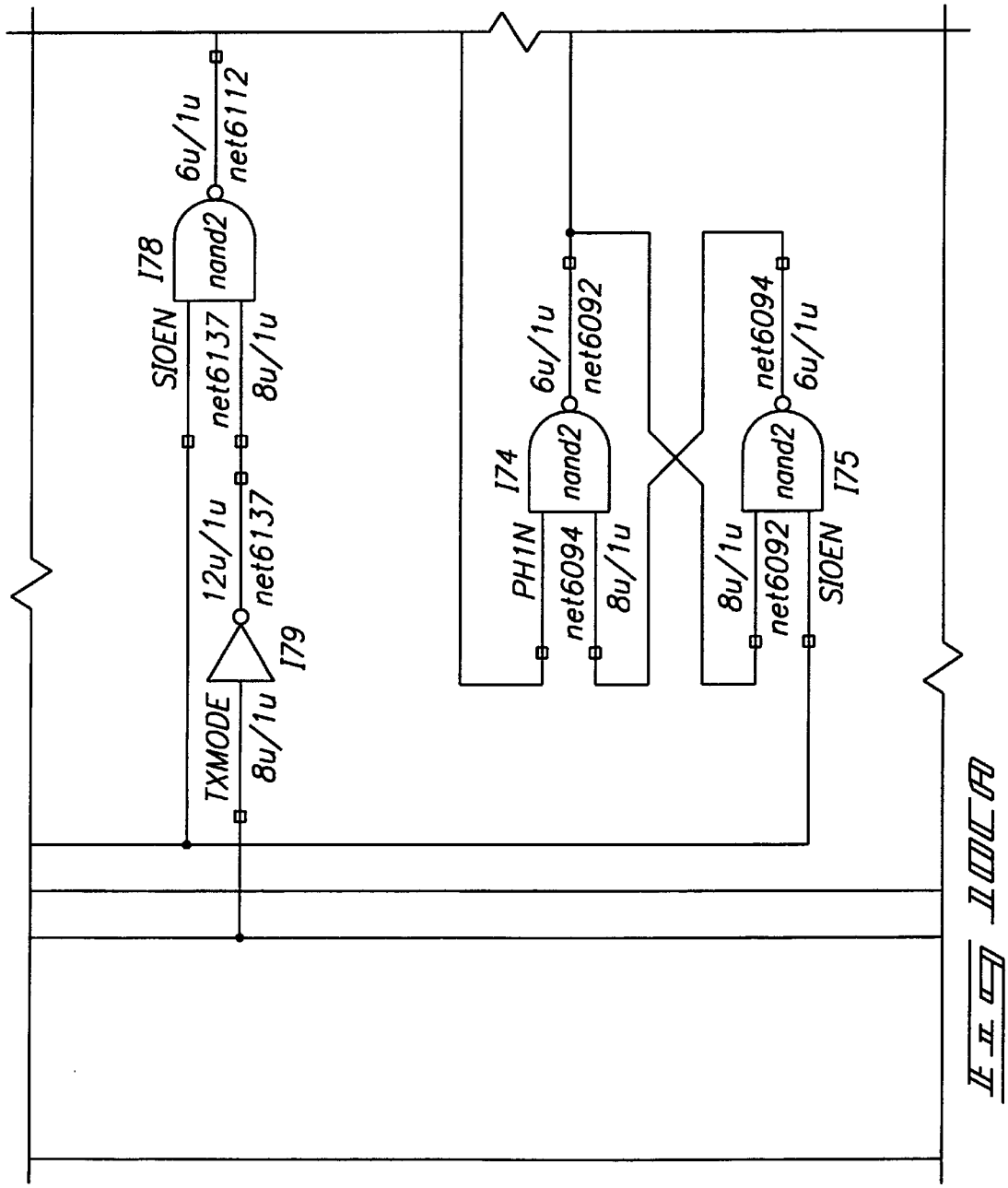
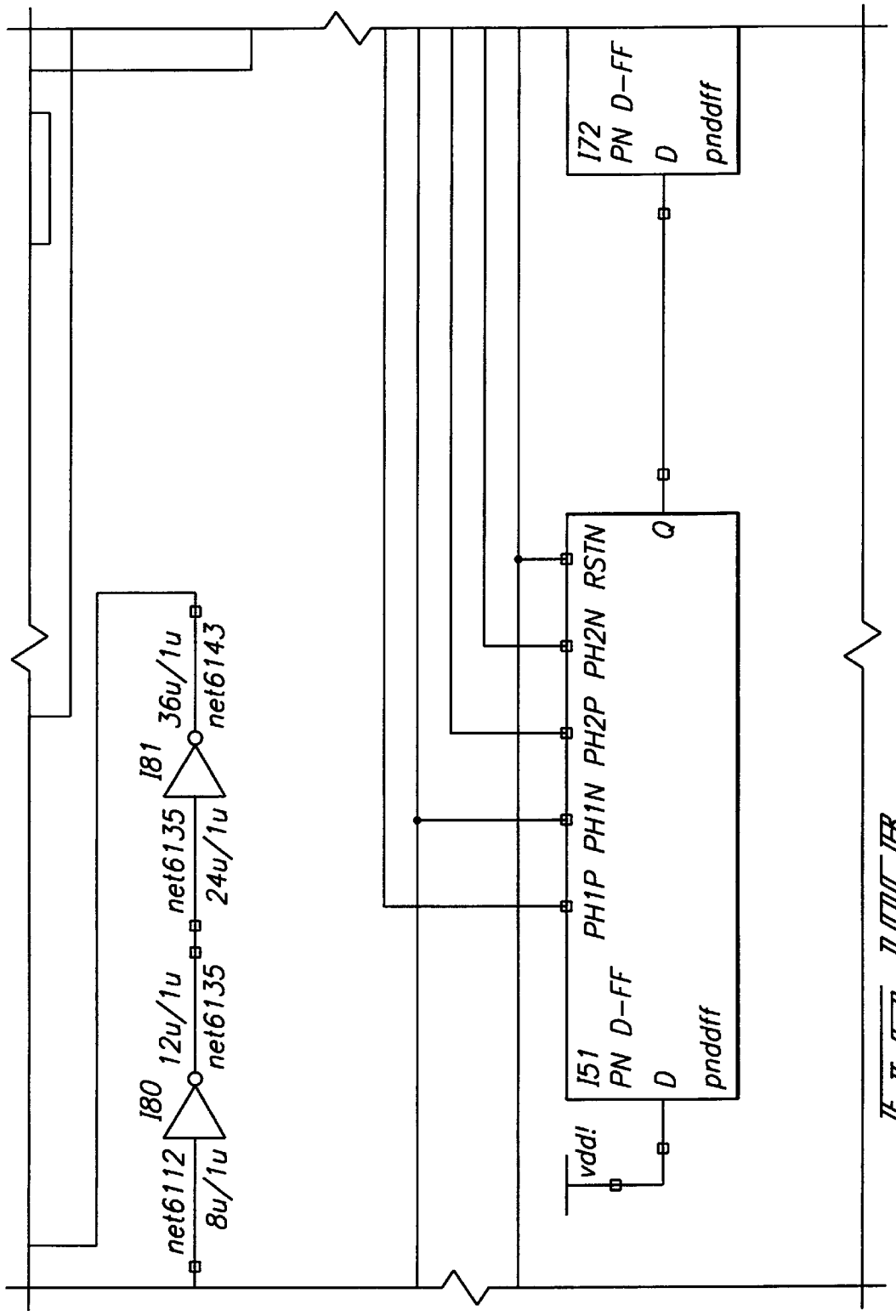

I78
nand2
6u/1u
net6112
SIOEN
net6137
8u/1u
12u/1u
net6137
I79
TXMODE
8u/1u
I74
nand2
6u/1u
net6092
PH1N
net6094
8u/1u
I75
nand2
net6094
6u/1u
8u/1u
net6092
SIOEN

FIG 100A


I72
PN D-FF
D
pnddff
Q
I51
PN D-FF
D
pnddff
PH1P PH1N PH2P PH2N RSTN
vdd!
I81
36u/1u
net6143
net6135
24u/1u
net6135
I80
12u/1u
net6112
8u/1u

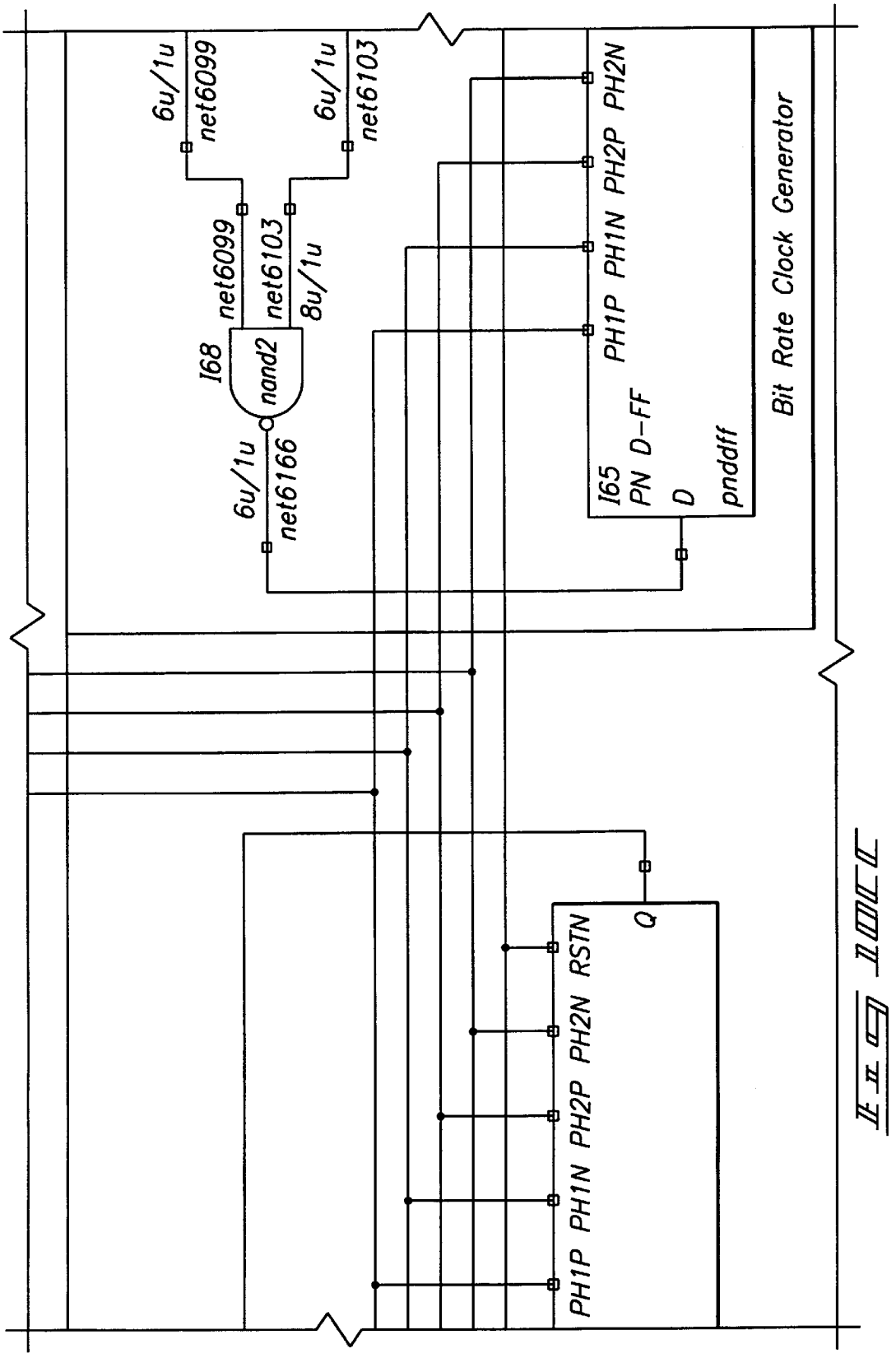

6u/1u
net6099
6u/1u
net6103
net6099
net6103
8u/1u
I68
nand2
6u/1u
net6166
I65
PN D-FF
D
pnddff
PH1P PH1N PH2P PH2N
Bit Rate Clock Generator
Q
PH1P PH1N PH2P PH2N RSTN

FIG 1003

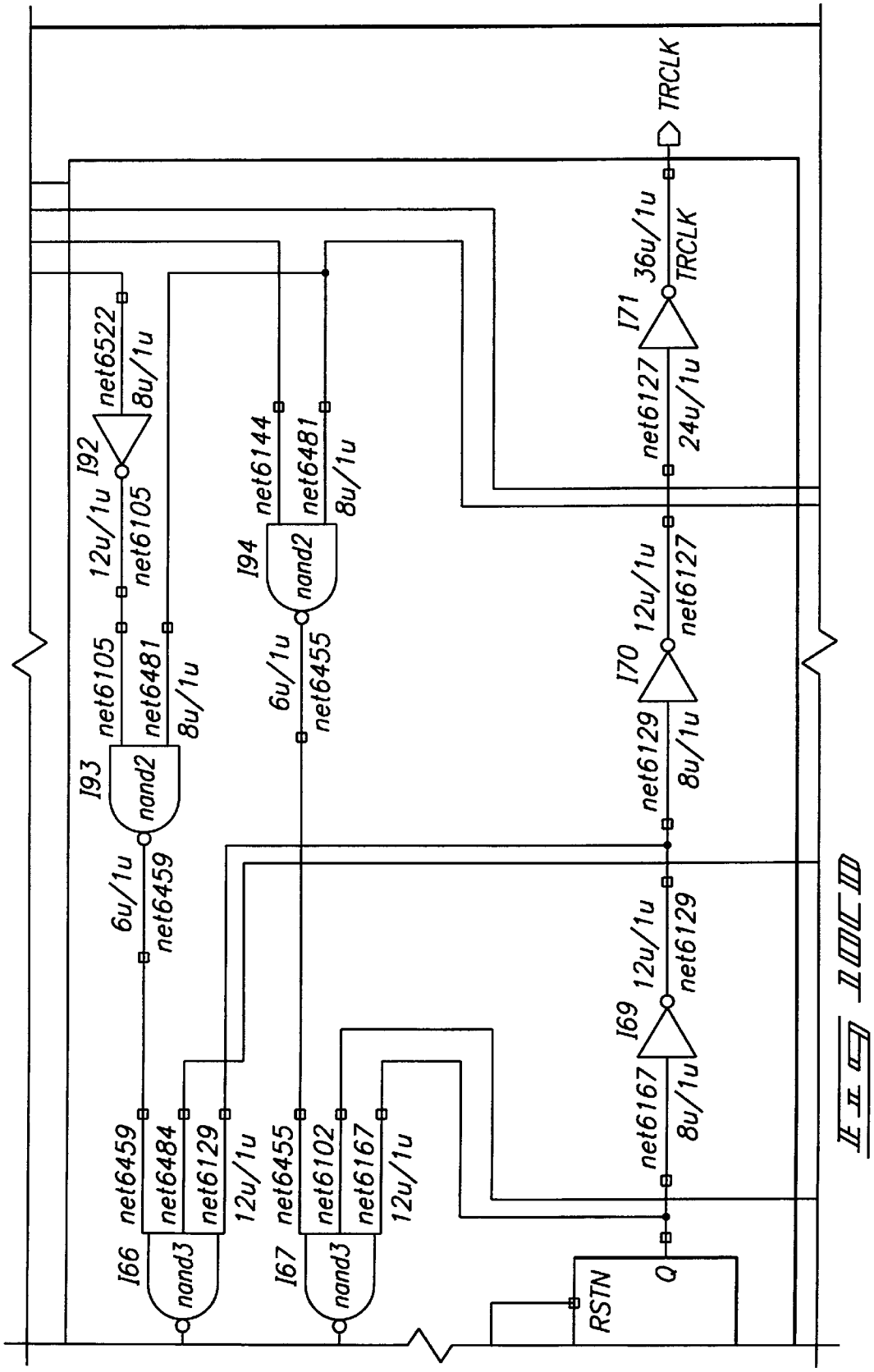

TRCLK
I71
36u/1u
TRCLK
net6127
24u/1u
I70
12u/1u
net6127
net6129
8u/1u
I69
12u/1u
net6129
net6167
8u/1u
I92
net6522
8u/1u
12u/1u
net6105
I94
net6144
net6481
8u/1u
nand2
6u/1u
net6455
I93
net6105
net6481
8u/1u
nand2
6u/1u
net6459
I66
net6459
net6484
net6129
12u/1u
nand3
I67
net6455
net6102
net6167
12u/1u
nand3
RSTN
Q

FIG 1001

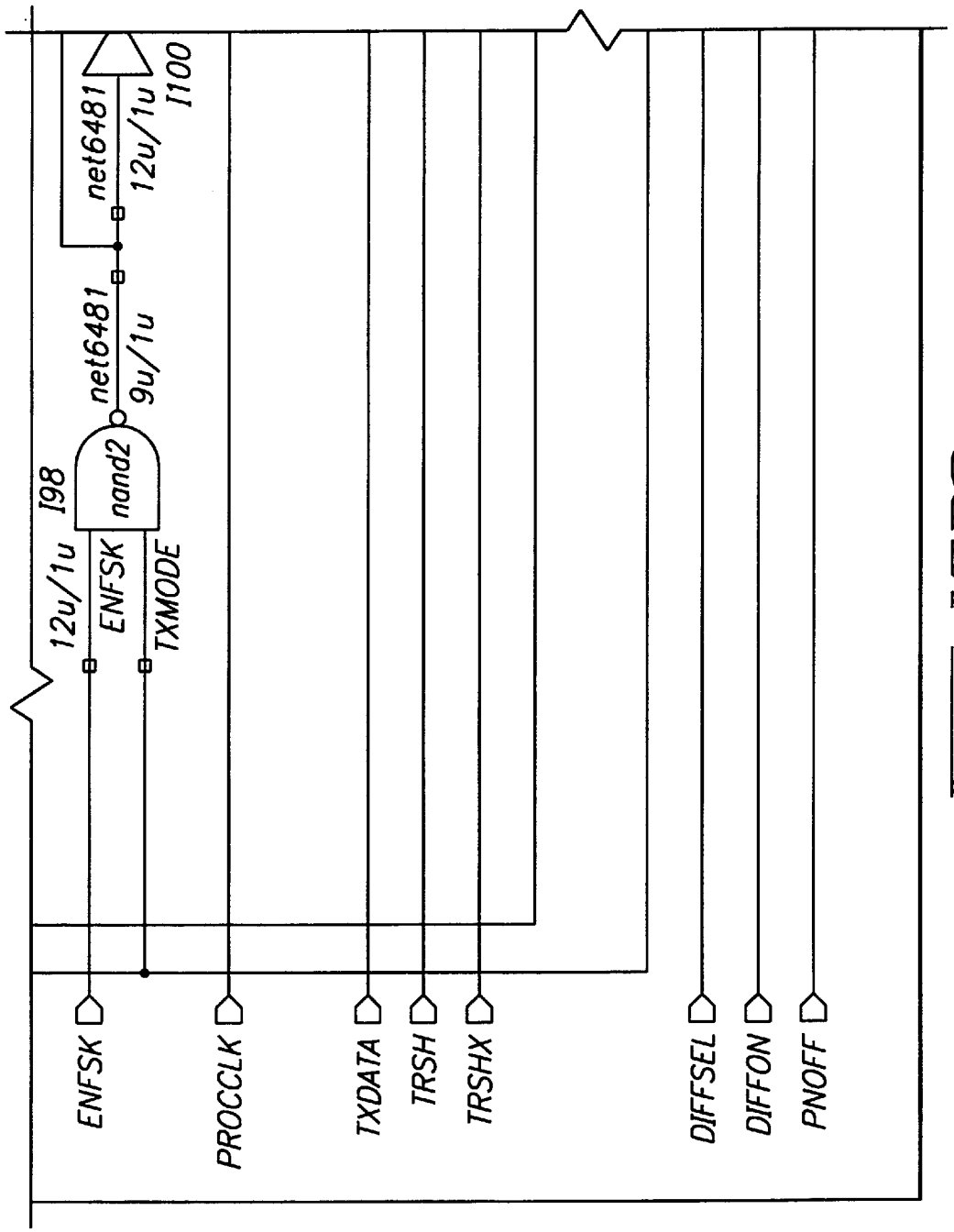

I100
net6481
12u/1u
net6481
9u/1u
I98
nand2
12u/1u
ENFSK
TXMODE
ENFSK
PROCCLK
TXDATA
TRSH
TRSHX
DIFFSEL
DIFFON
PNOFF

FIG 1100A

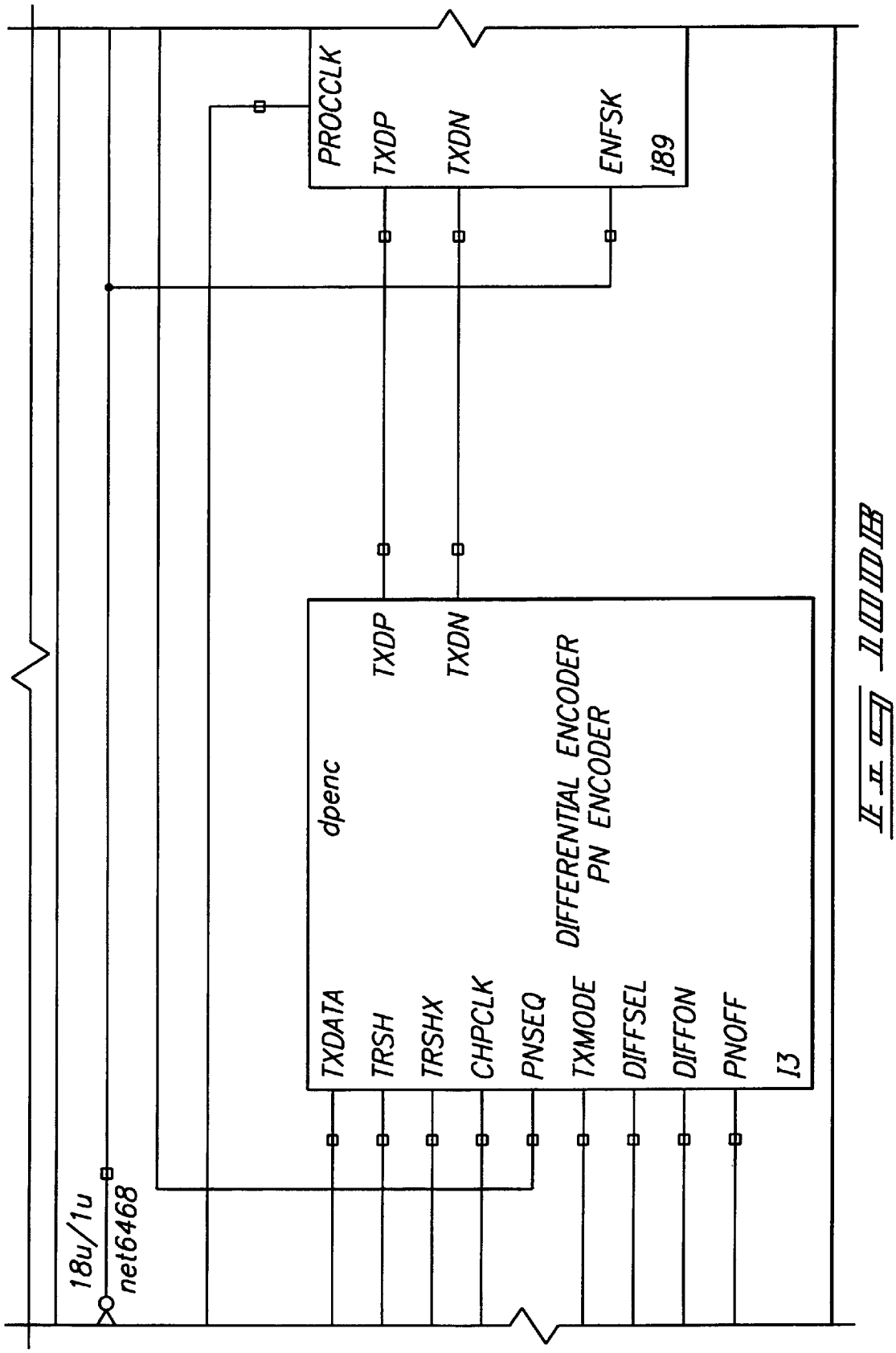

PROCCLK
TXDP
TXDN
ENFSK
I89
dpenc
TXDP
TXDN
DIFFERENTIAL ENCODER
PN ENCODER
TXDATA
TRSH
TRSHX
CHPCLK
PNSEQ
TXMODE
DIFFSEL
DIFFON
PNOFF
I3
18u/1u
net6468

Fig 1100

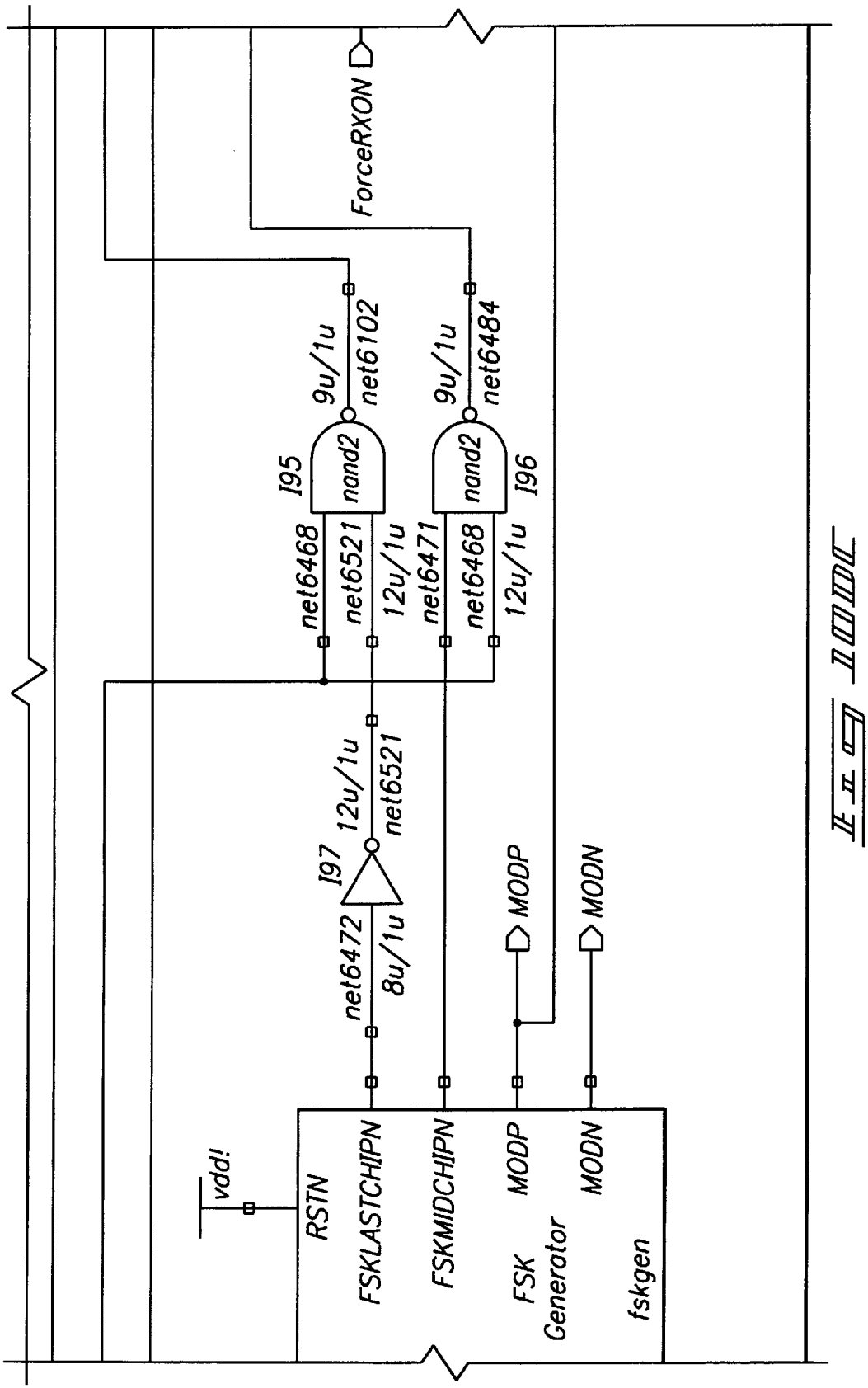

ForceRXON
9u/1u
net6102
9u/1u
net6484
I95
nand2
nand2
I96
net6468
net6521
12u/1u
net6471
net6468
12u/1u
12u/1u
net6521
I97
net6472
8u/1u
MODP
MODN
vdd!
RSTN
FSKLASTCHIPN
FSKMIDCHIPN
MODP
MODN
FSK
Generator
fskgen

FIG 1000

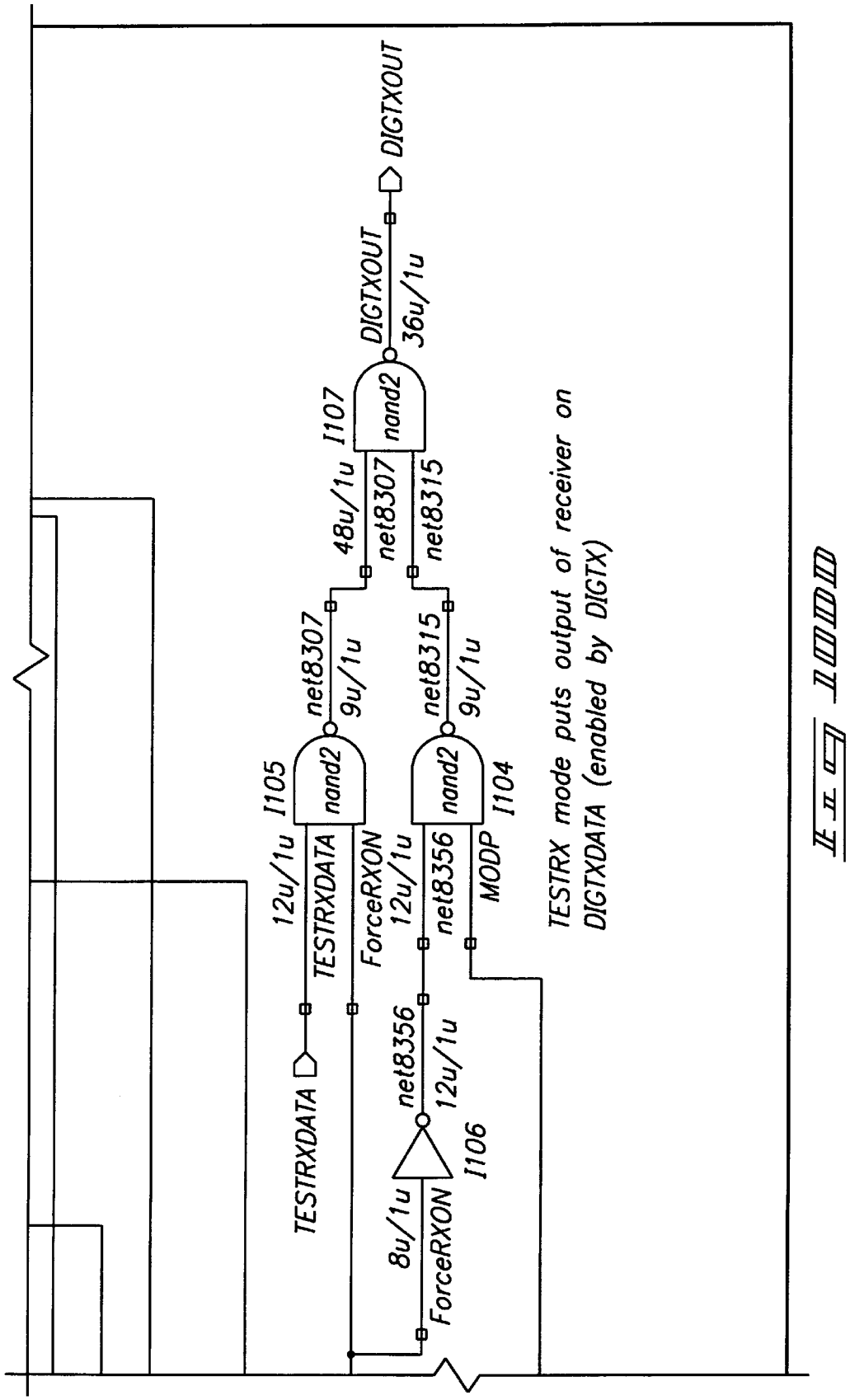

DIGTXOUT
DIGTXOUT
36u/1u
I107
nand2
48u/1u
net8307
net8315
net8307
9u/1u
net8315
9u/1u
I105
nand2
I104
nand2
12u/1u
TESTRXDATA
ForceRXON
12u/1u
net8356
MODP
TESTRX mode puts output of receiver on
DIGTXDATA (enabled by DIGTX)
TESTRXDATA
net8356
12u/1u
I106
8u/1u
ForceRXON

FIG 1000

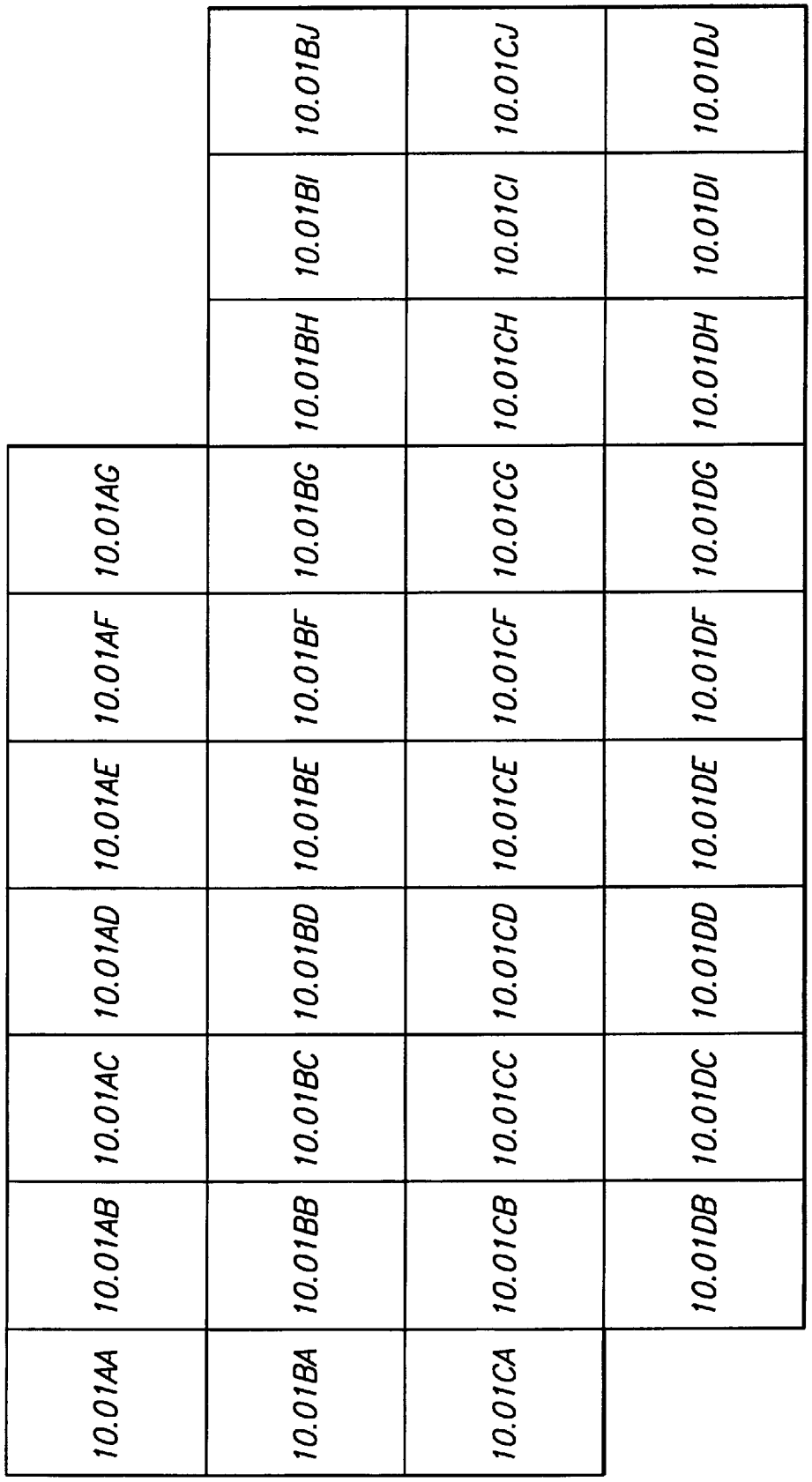

10.01AA
10.01AB
10.01AC
10.01AD
10.01AE
10.01AF
10.01AG
10.01BA
10.01BB
10.01BC
10.01BD
10.01BE
10.01BF
10.01BG
10.01BH
10.01BI
10.01BJ
10.01CA
10.01CB
10.01CC
10.01CD
10.01CE
10.01CF
10.01CG
10.01CH
10.01CI
10.01CJ
10.01DB
10.01DC
10.01DD
10.01DE
10.01DF
10.01DG
10.01DH
10.01DI
10.01DJ

FIG. 10,011

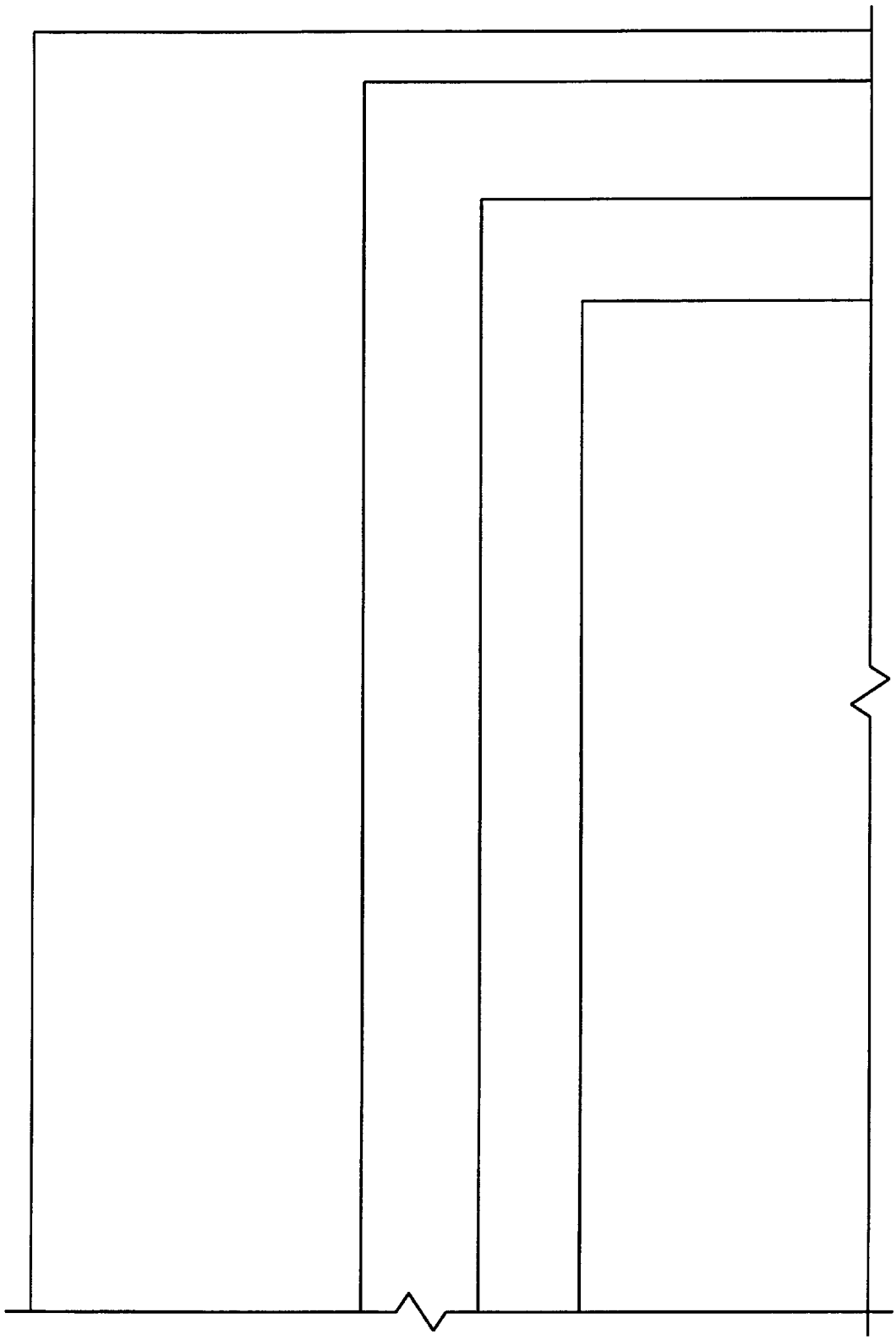


Fig 10.01AA

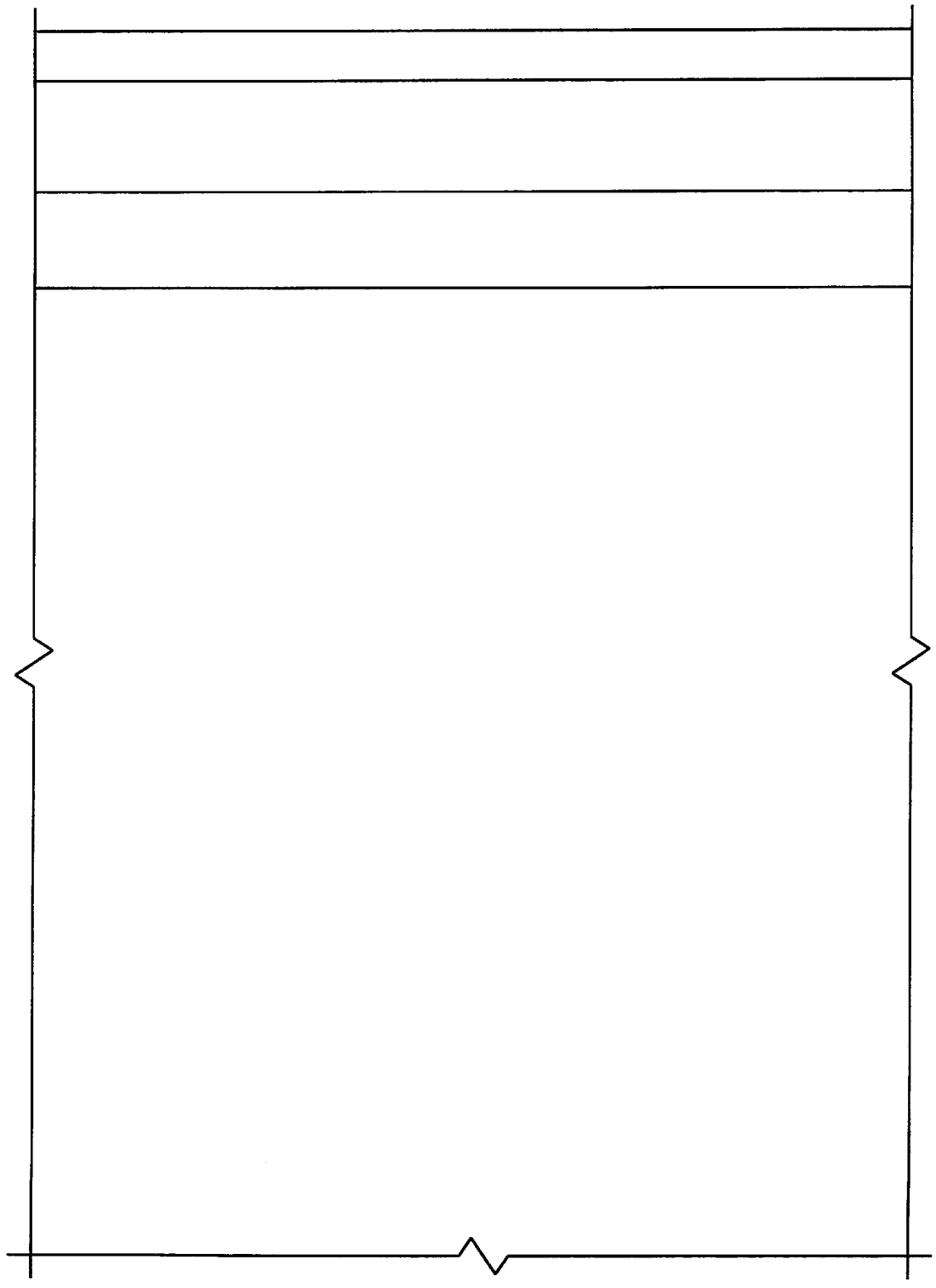


Fig 10.01AB

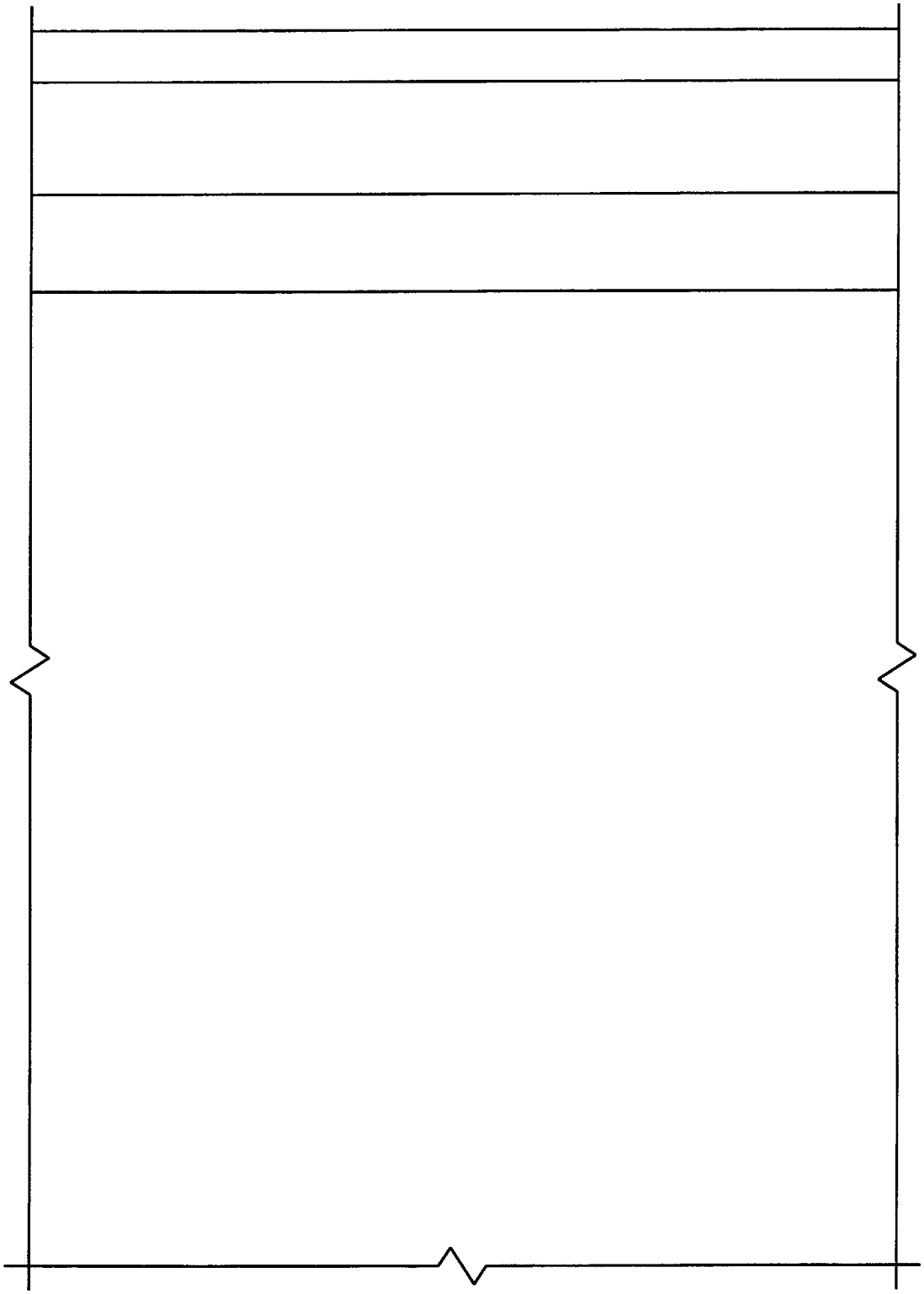


Fig 10.01AC

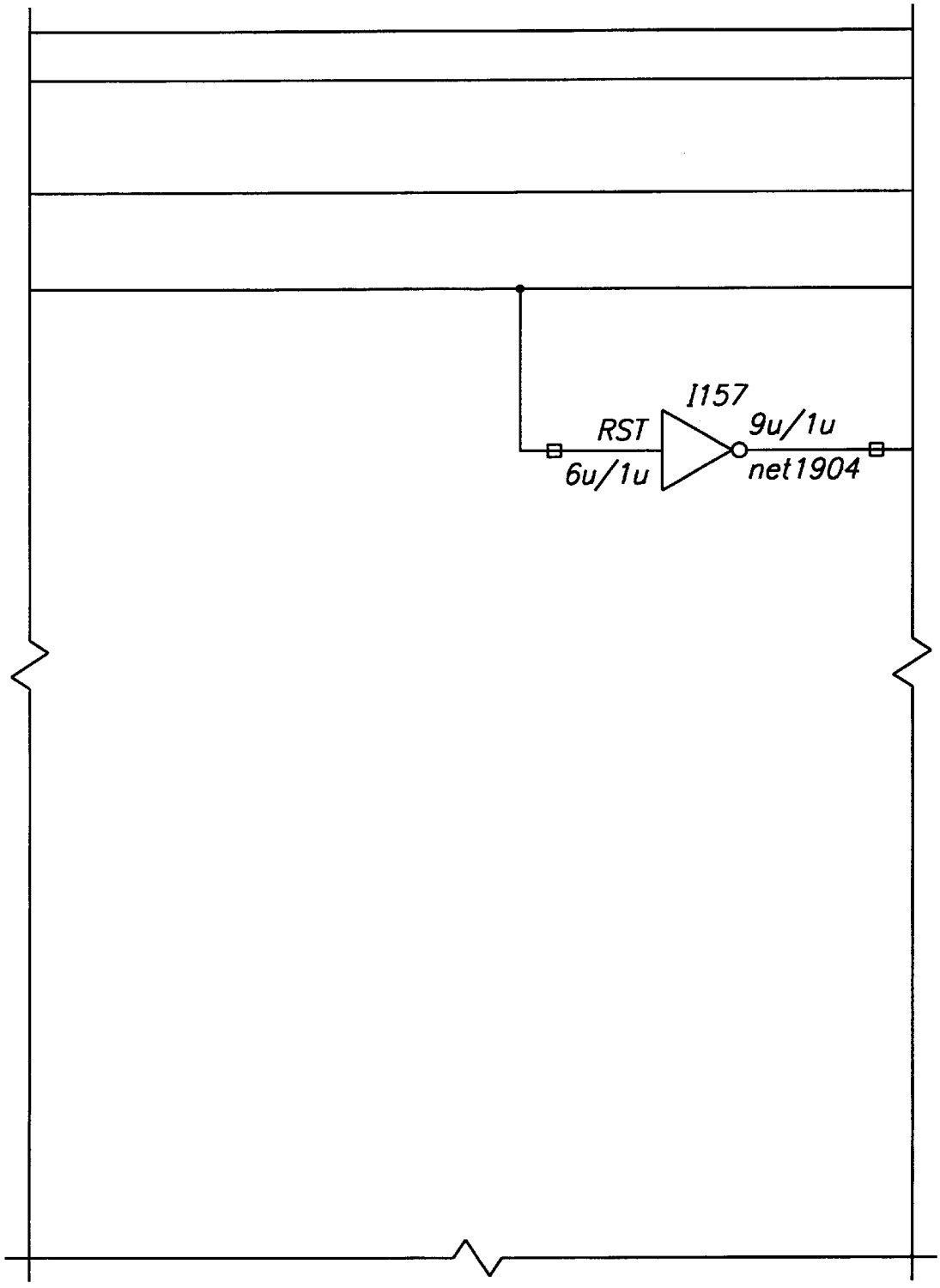
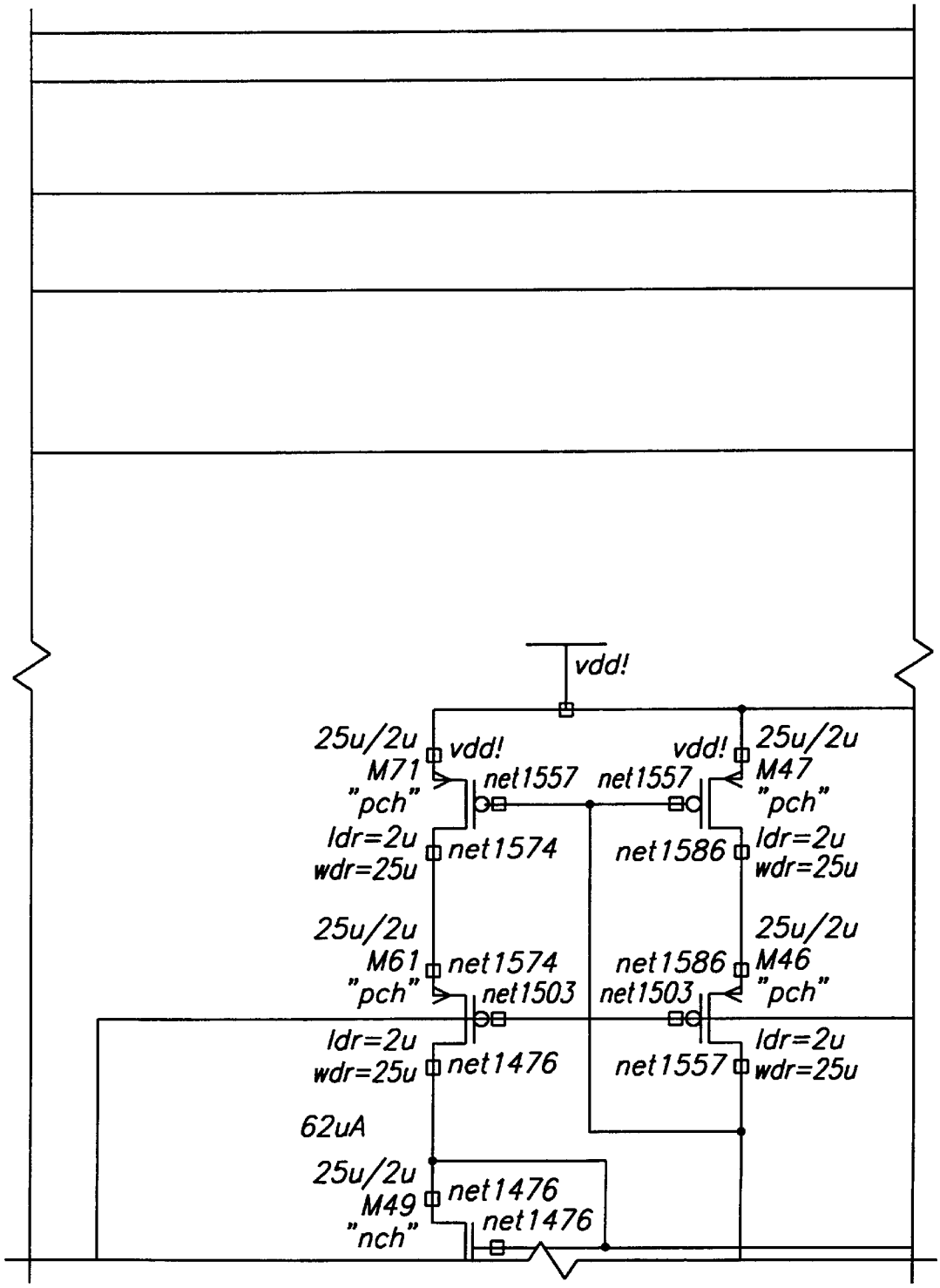


Fig 10.0140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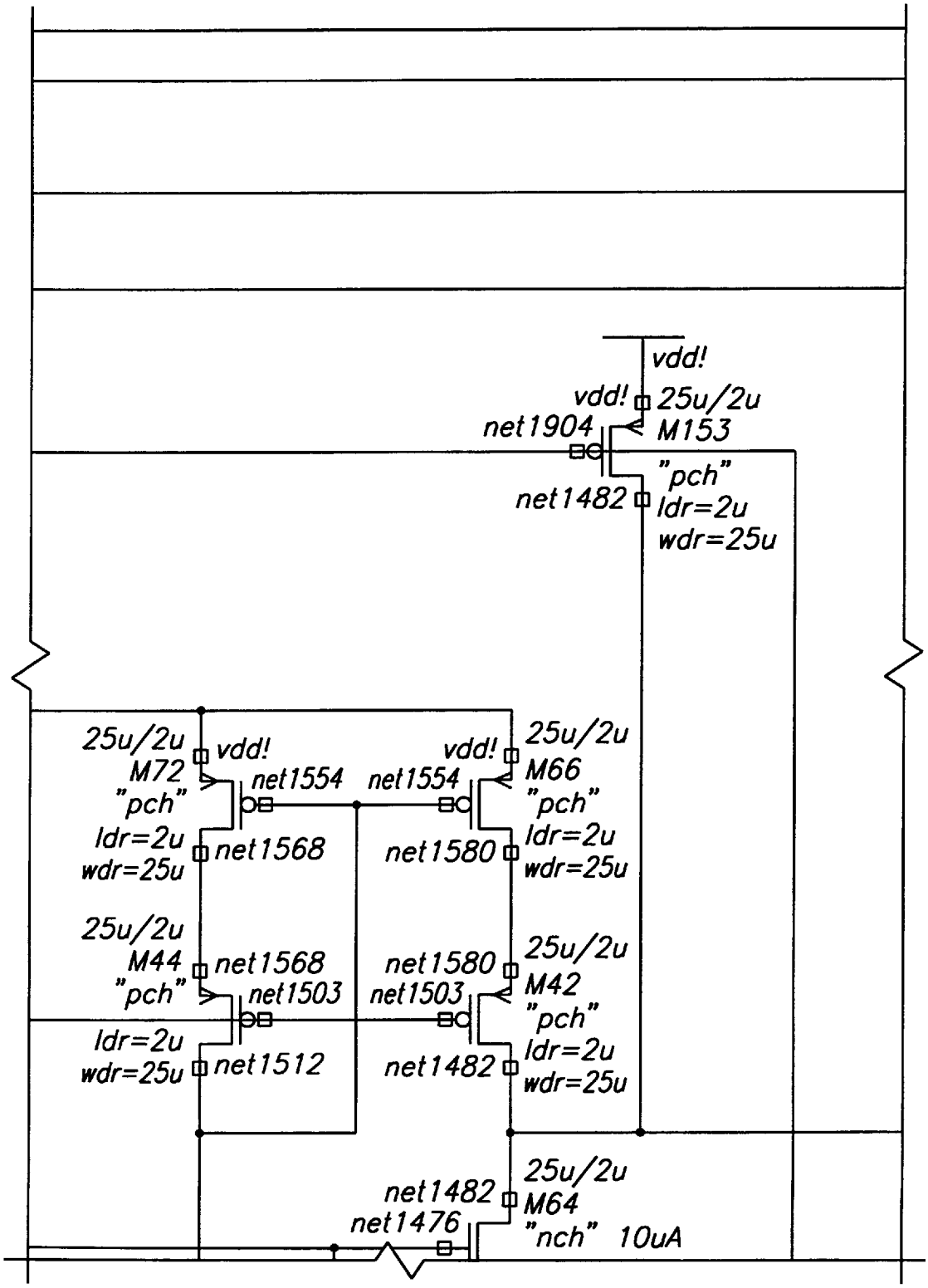
ldr=2u
wdr=25u
vdd!
net1557
net1574
25u/2u
M61
"pch"
net1574
net1503
ldr=2u
wdr=25u
net1476
62uA
25u/2u
M49
"nch"
net1476
net1476
vdd!
net1557
net1586
net1503
net1557
25u/2u
M47
"pch"
ldr=2u
wdr=25u
net1586
25u/2u
M46
"pch"
ldr=2u
wdr=25u

Fig 10.01AE


vdd!
vdd!
25u/2u
M153
net1904
"pch"
net1482
ldr=2u
wdr=25u
25u/2u
M72
"pch"
vdd!
net1554
ldr=2u
wdr=25u
net1568
net1554
vdd!
25u/2u
M66
"pch"
ldr=2u
net1580
wdr=25u
25u/2u
M44
"pch"
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ldr=2u
wdr=25u
net1512
net1580
net1503
25u/2u
M42
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net1476
"nch"
10uA

Fig 100.00 AF

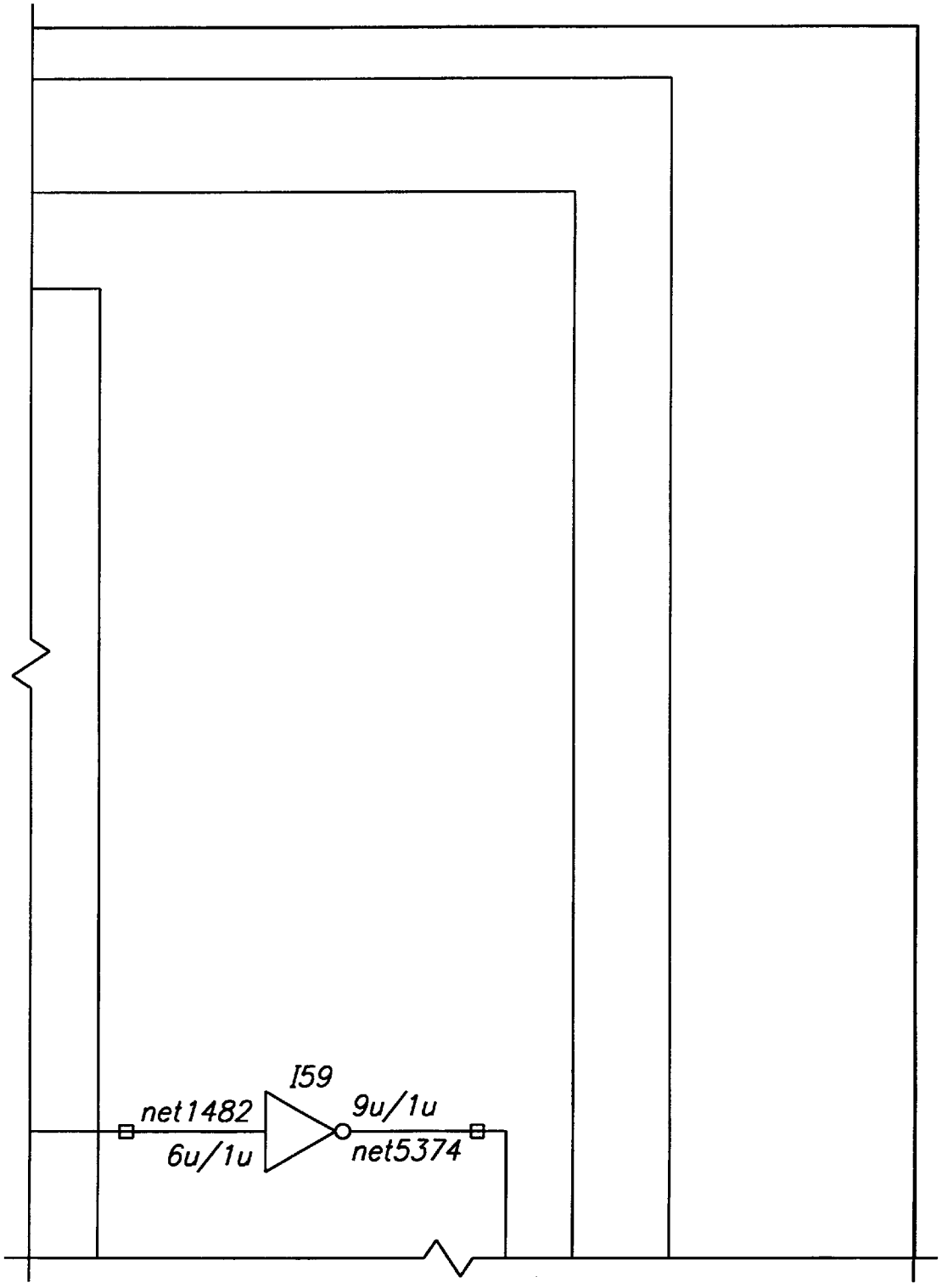


Fig 100,106

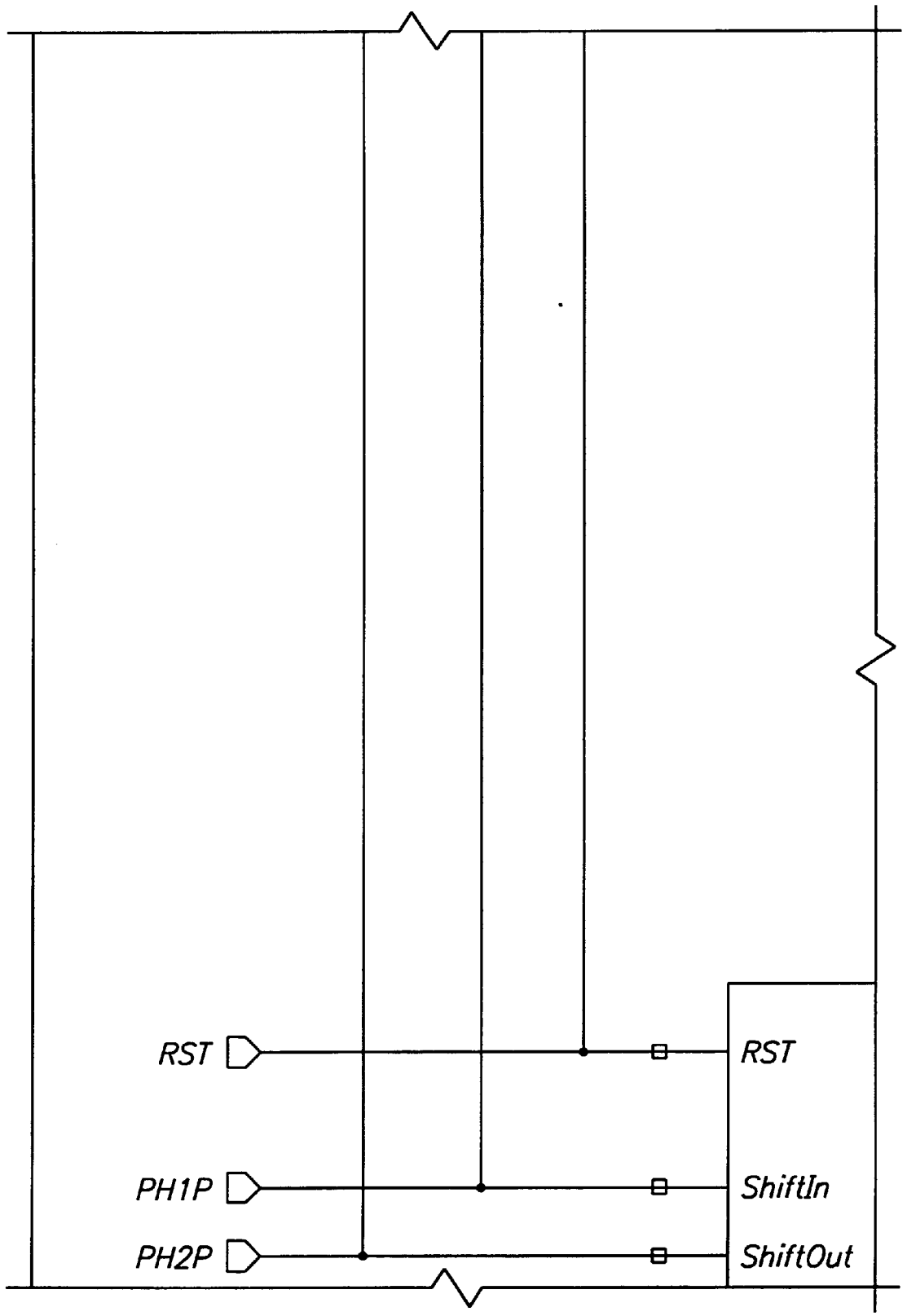


Fig. 100,118A

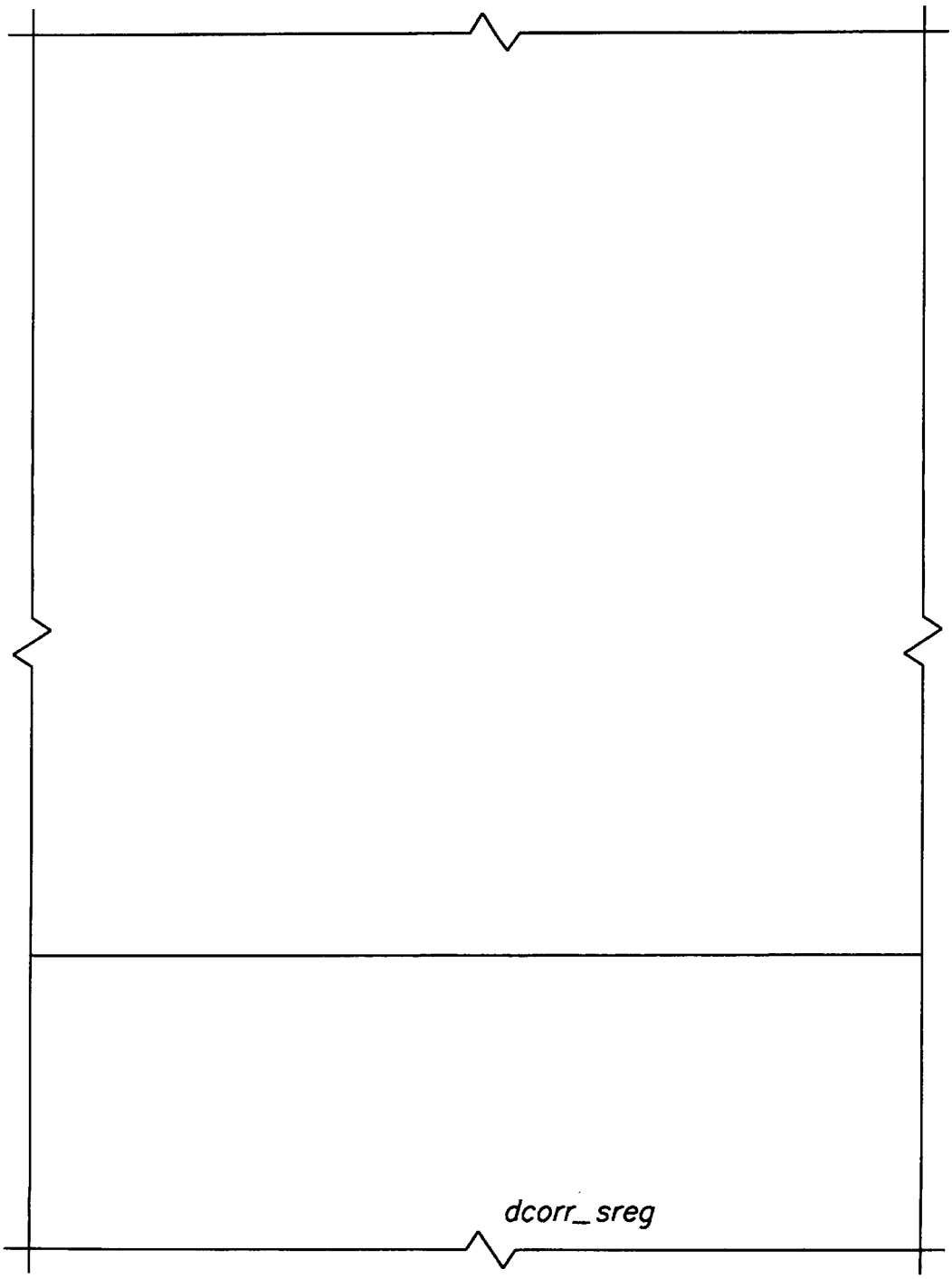


Fig 10.01BB

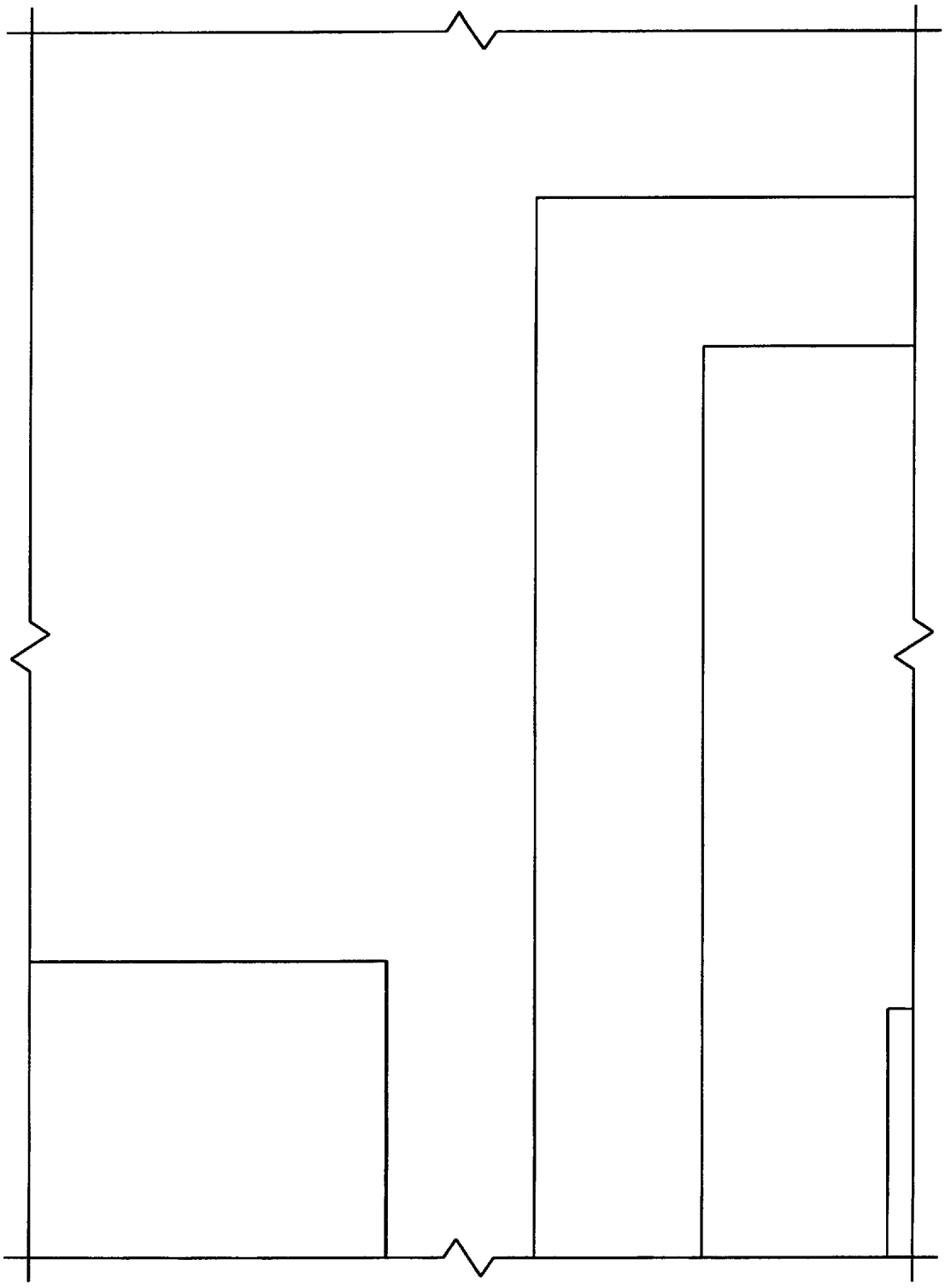
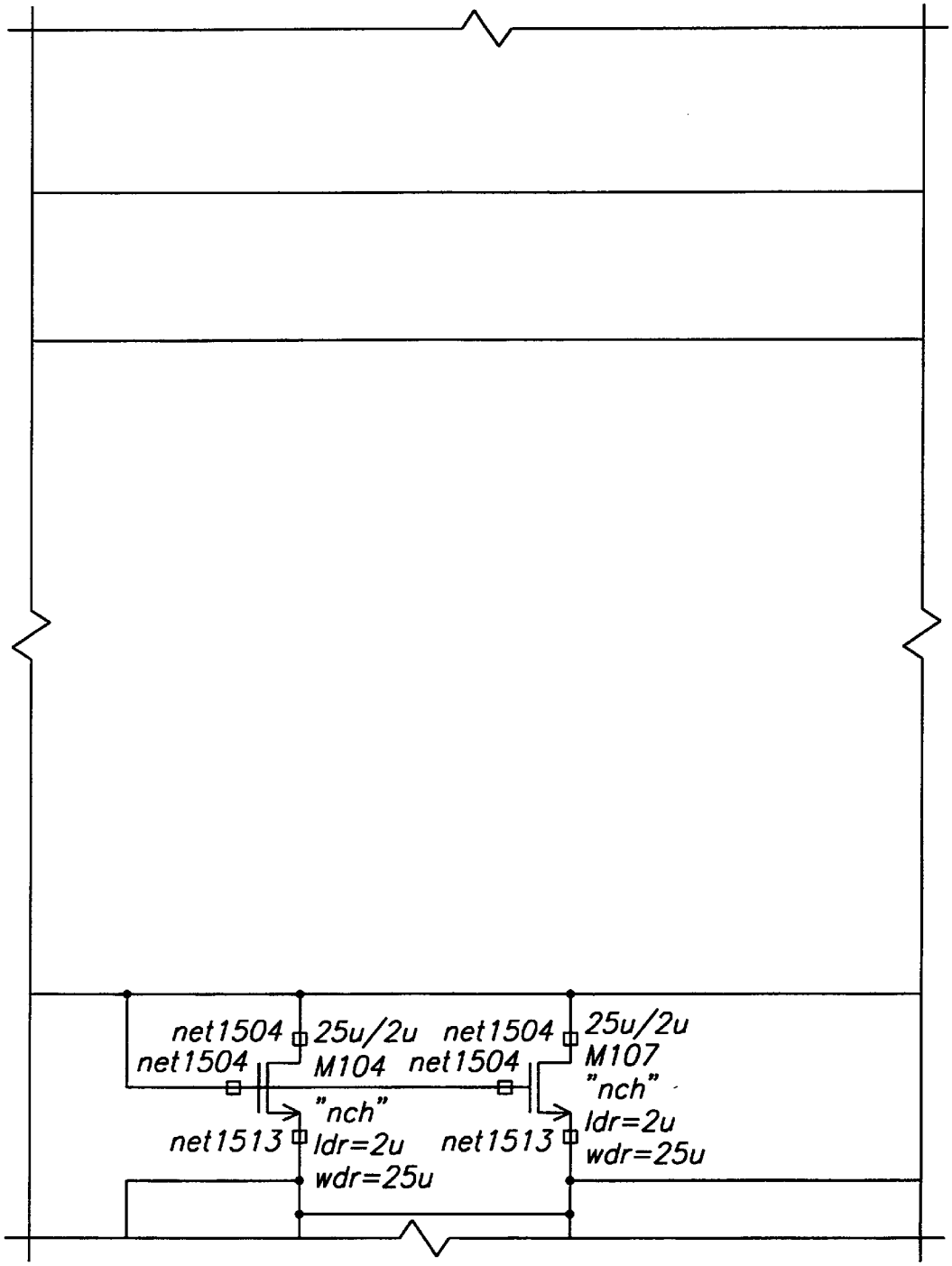


Fig 10.01BC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net1504
25u/2u
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net1504
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"nch"
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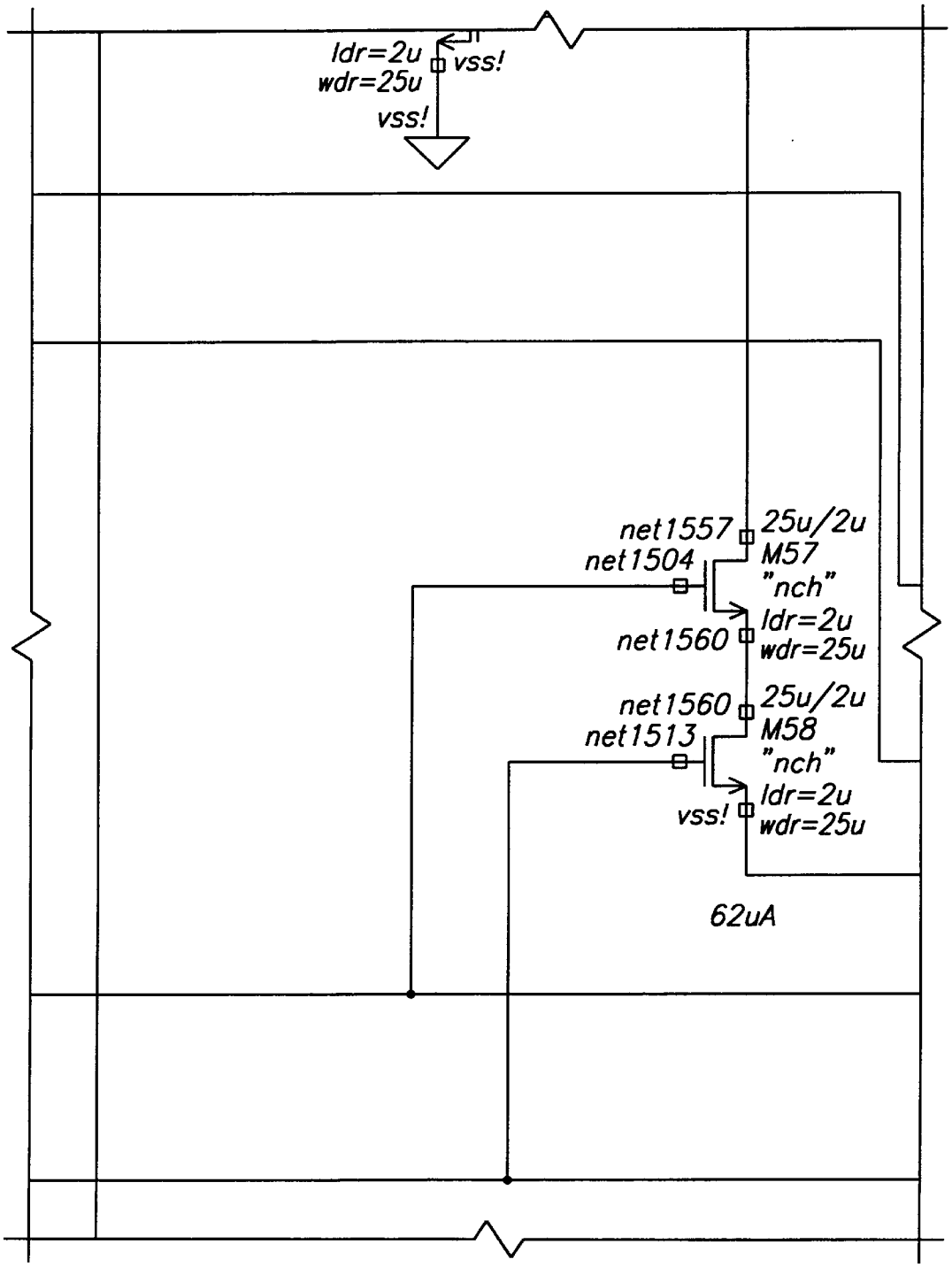
net1513
ldr=2u
wdr=25u
wdr=25u

Fig 1001BD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wdr=25u
vss!
vss!
net1557
net1504
25u/2u
M57
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ldr=2u
wdr=25u
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net1560
net1513
25u/2u
M58
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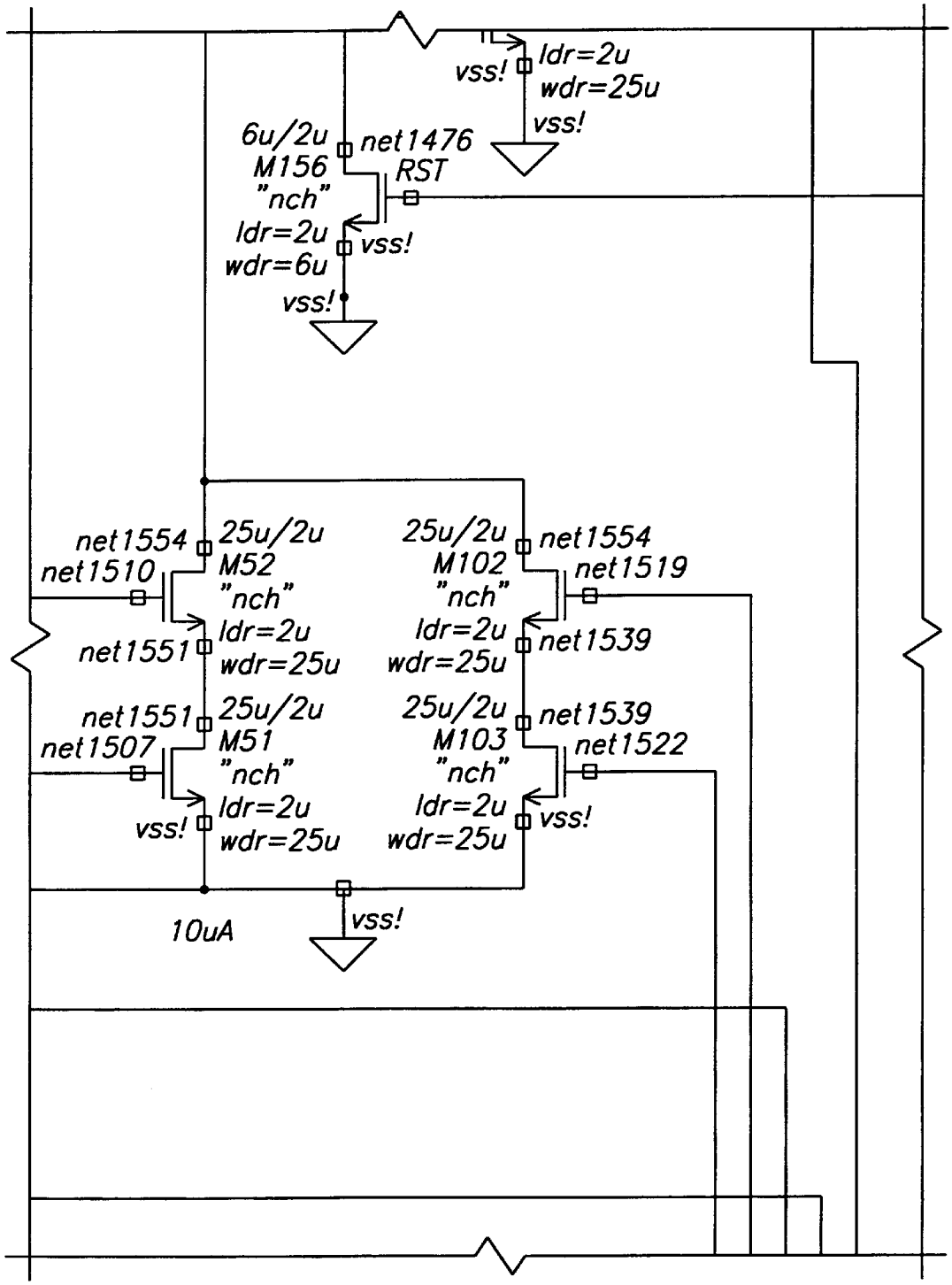
ldr=2u
wdr=25u
vss!
62uA

Fig 10.01BE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vss!
vss!
6u/2u
M156
"nch"
net1476
RST
ldr=2u
wdr=6u
vss!
vss!
net1554
net1510
25u/2u
M52
"nch"
ldr=2u
wdr=25u
net1551
25u/2u
M102
"nch"
ldr=2u
wdr=25u
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net1539
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net1507
25u/2u
M51
"nch"
ldr=2u
wdr=25u
vss!
25u/2u
M103
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wdr=25u
net1539
net1522
vss!
10uA
vss!

Fig 100.01BF

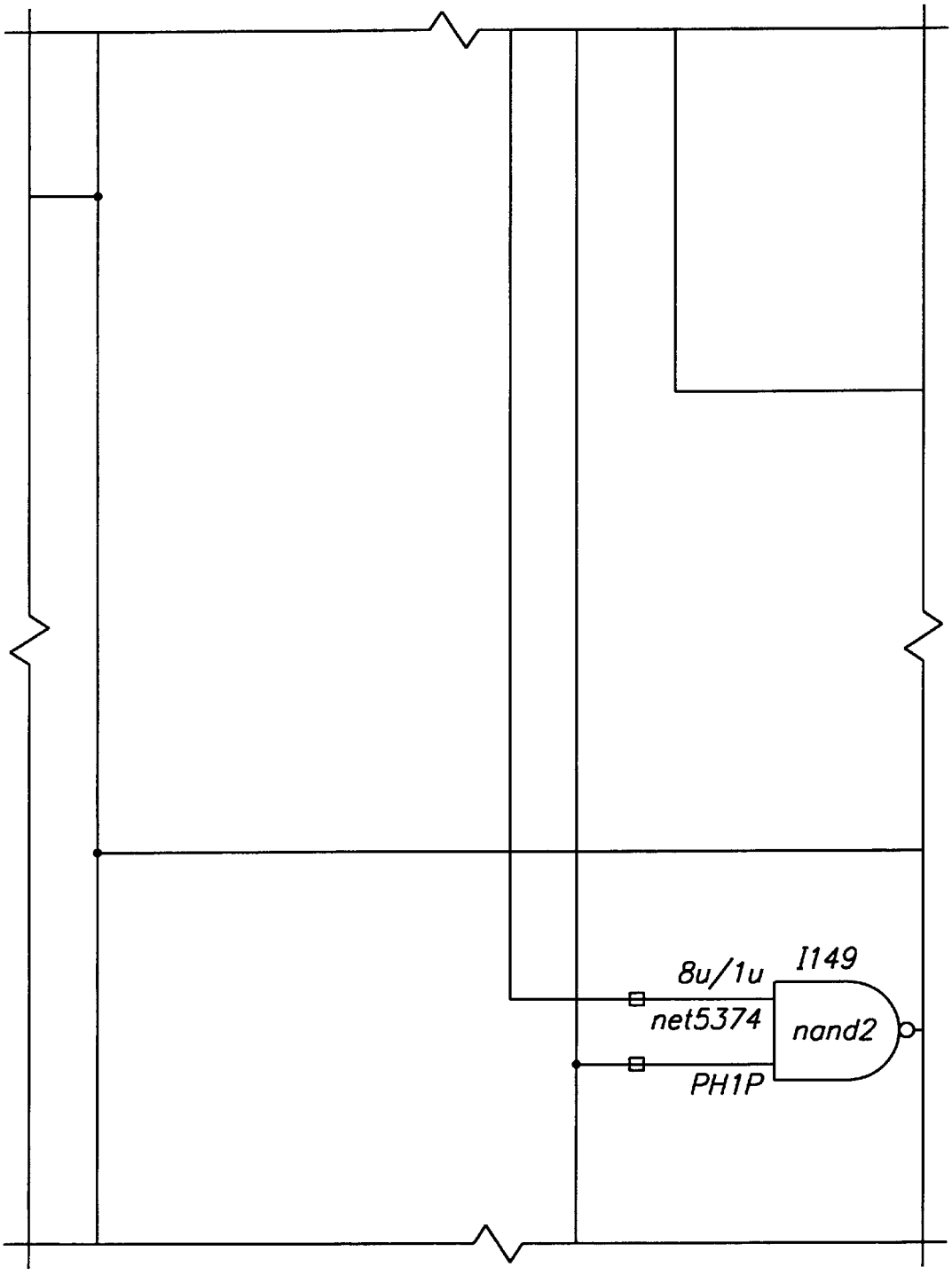
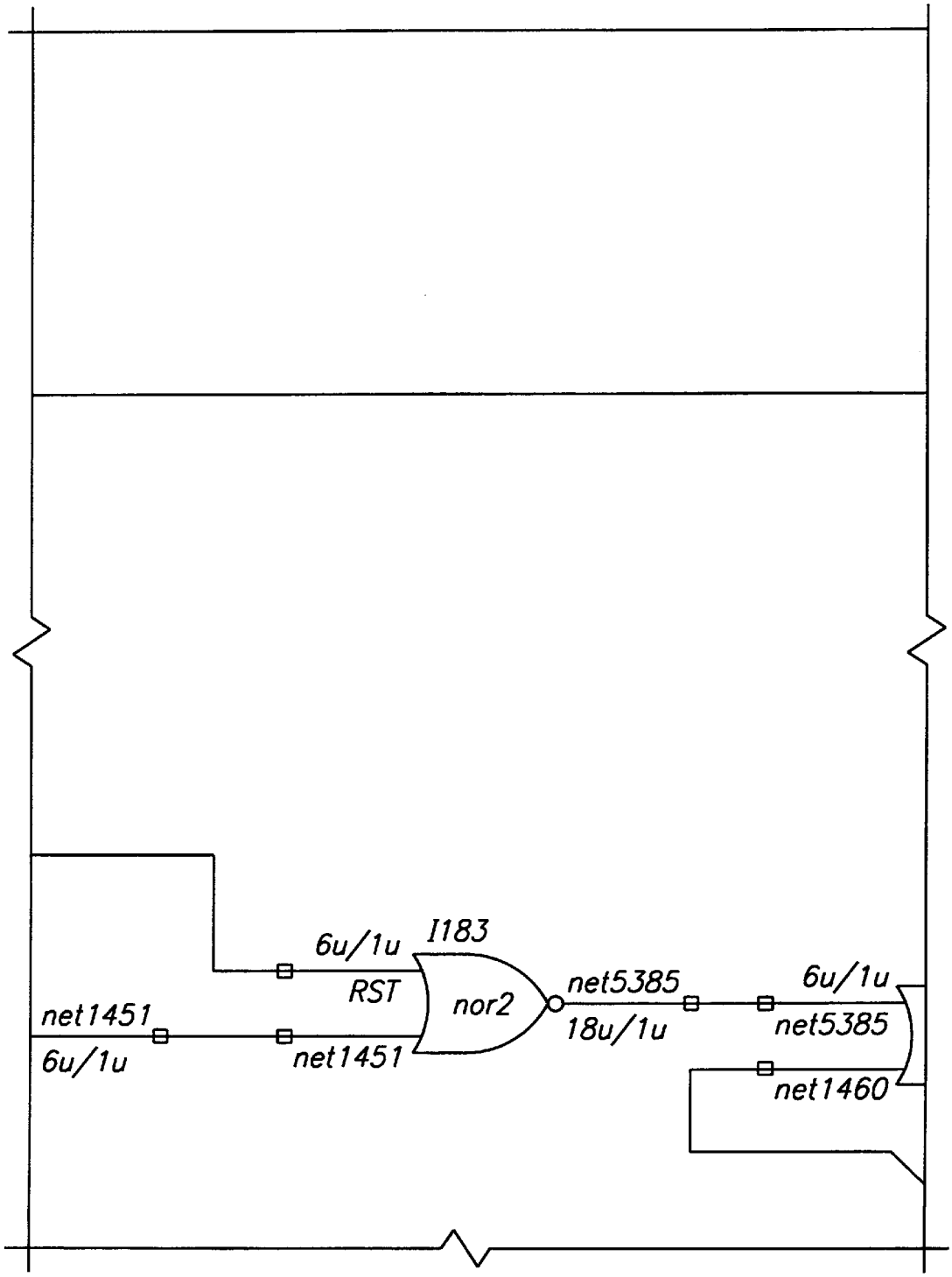


Fig 10.01B6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RST
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18u/1u
6u/1u
net5385
net1460
net1451
6u/1u
net1451

Fig 10.01BH

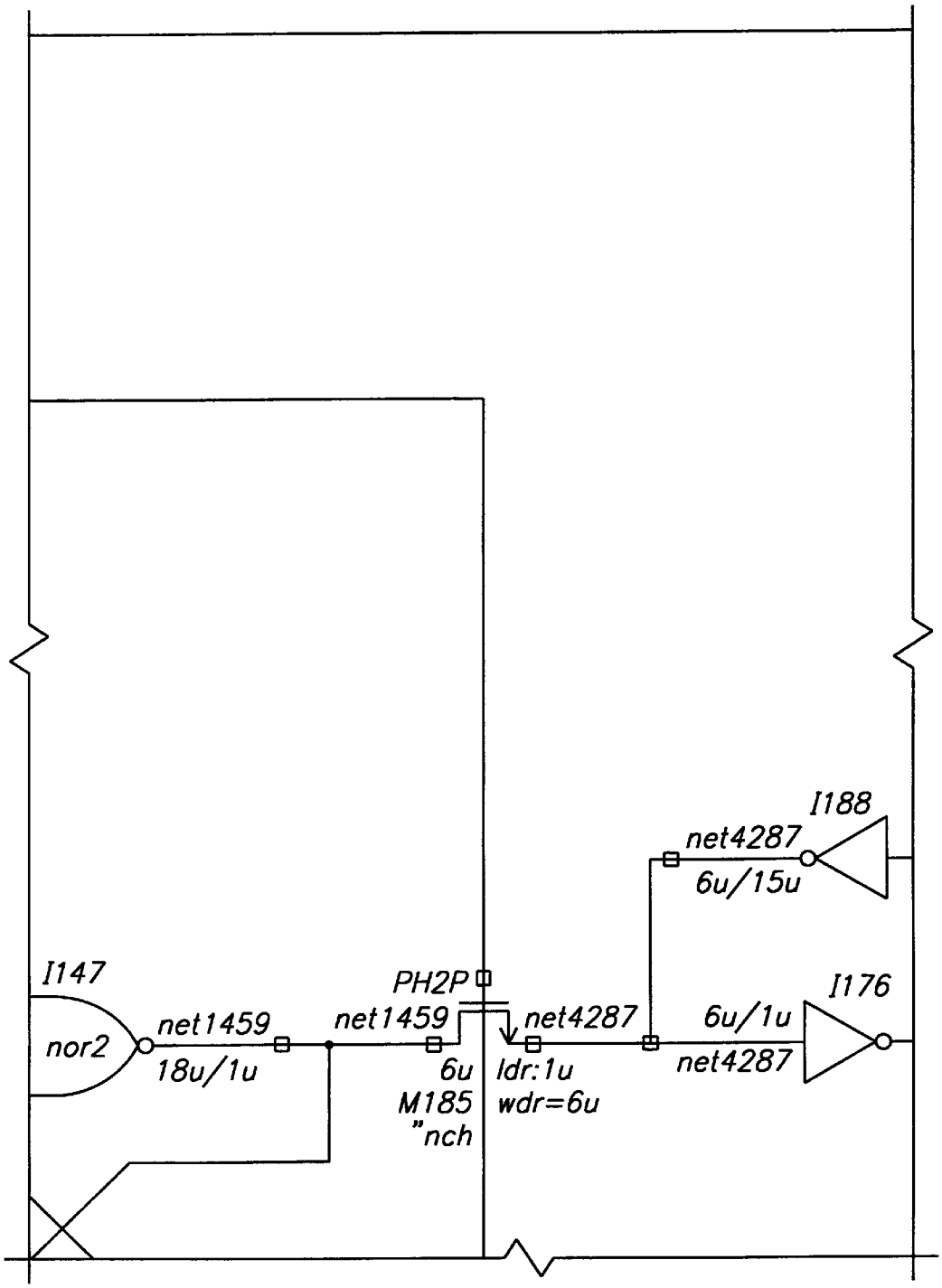


Fig 100,011B1

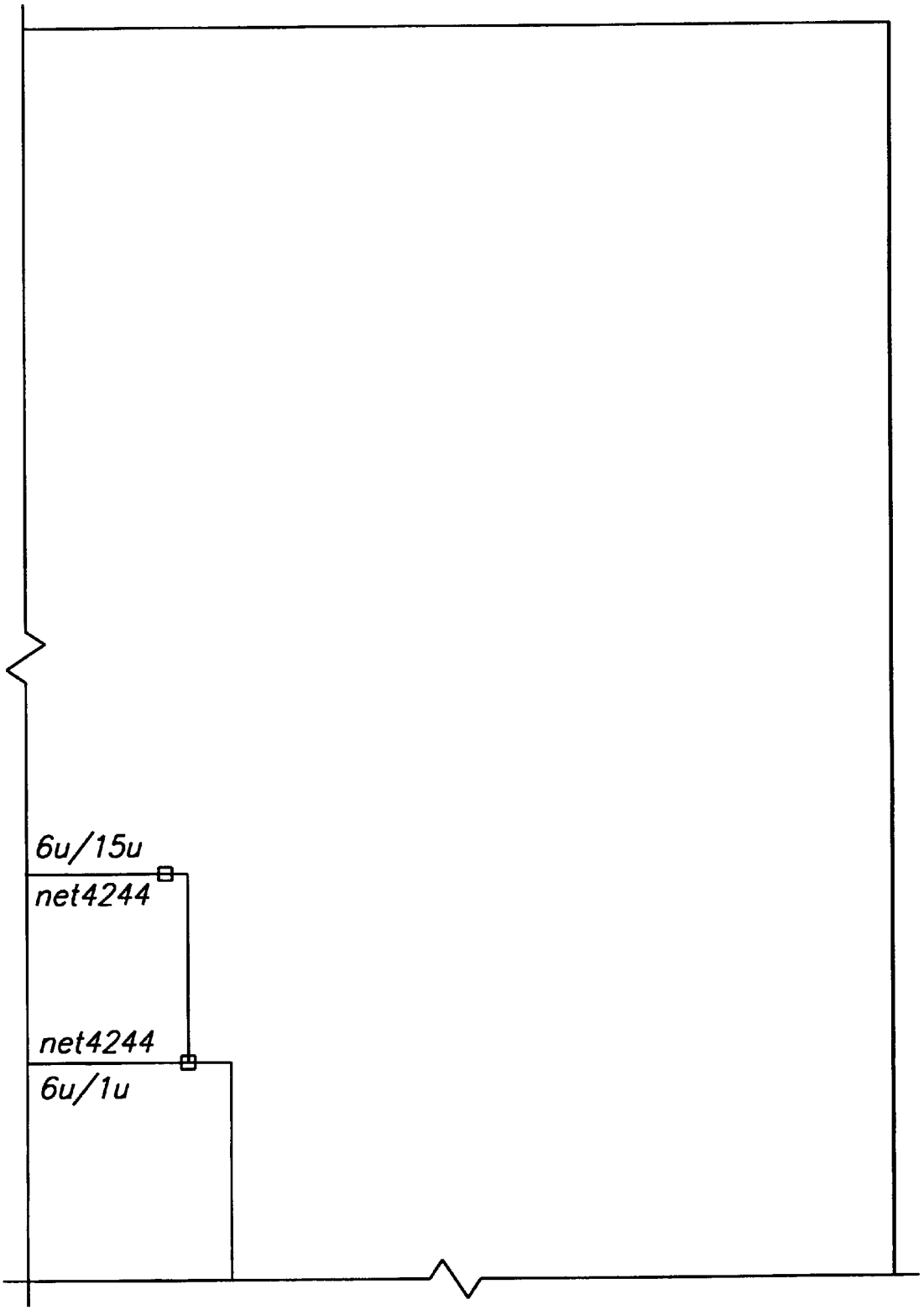
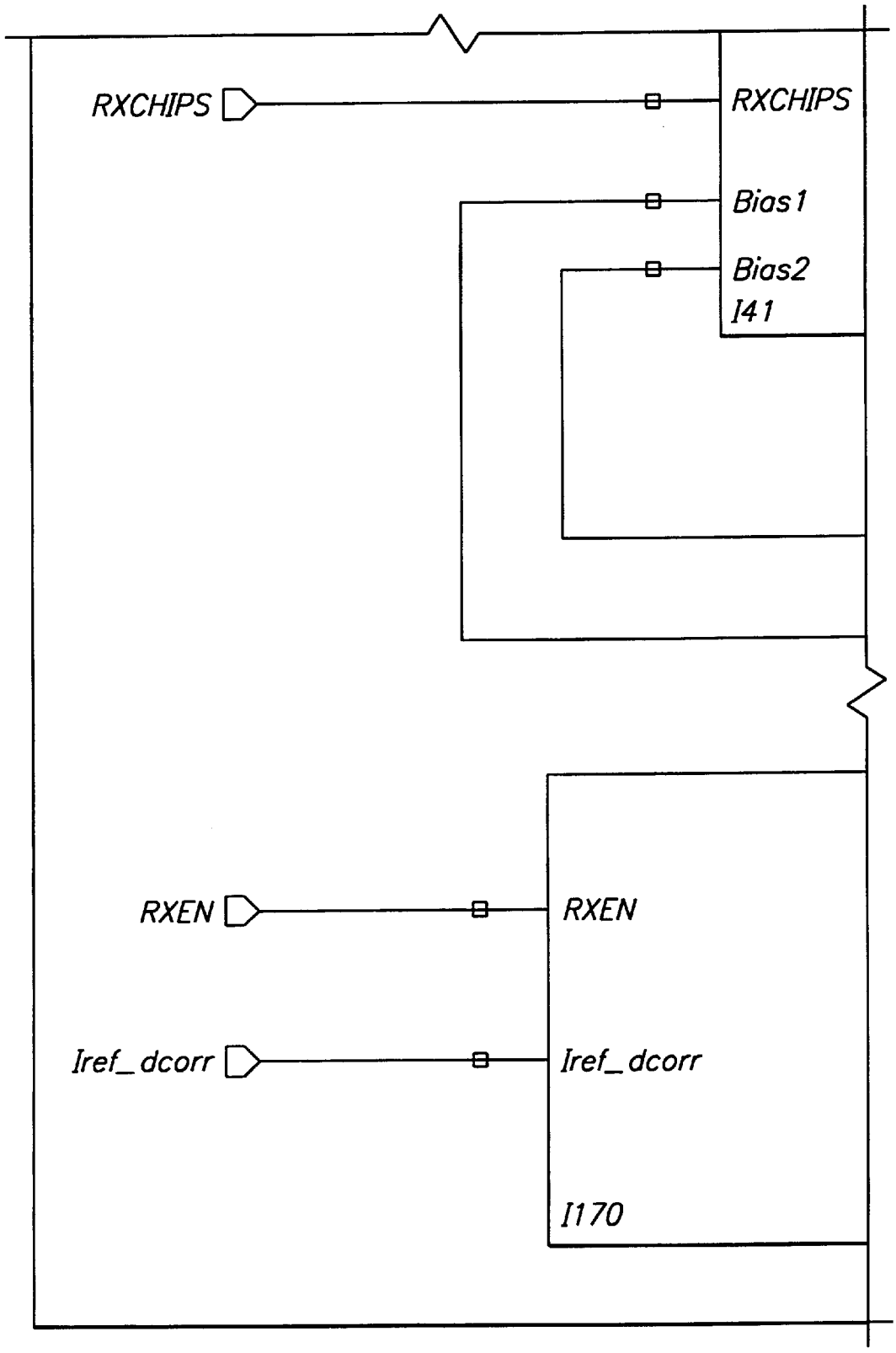


Fig 1001Bal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RXCHIPS
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Bias2
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RXEN
RXEN
Iref_dcorr
Iref_dcorr
I170

Fig 10.01CA

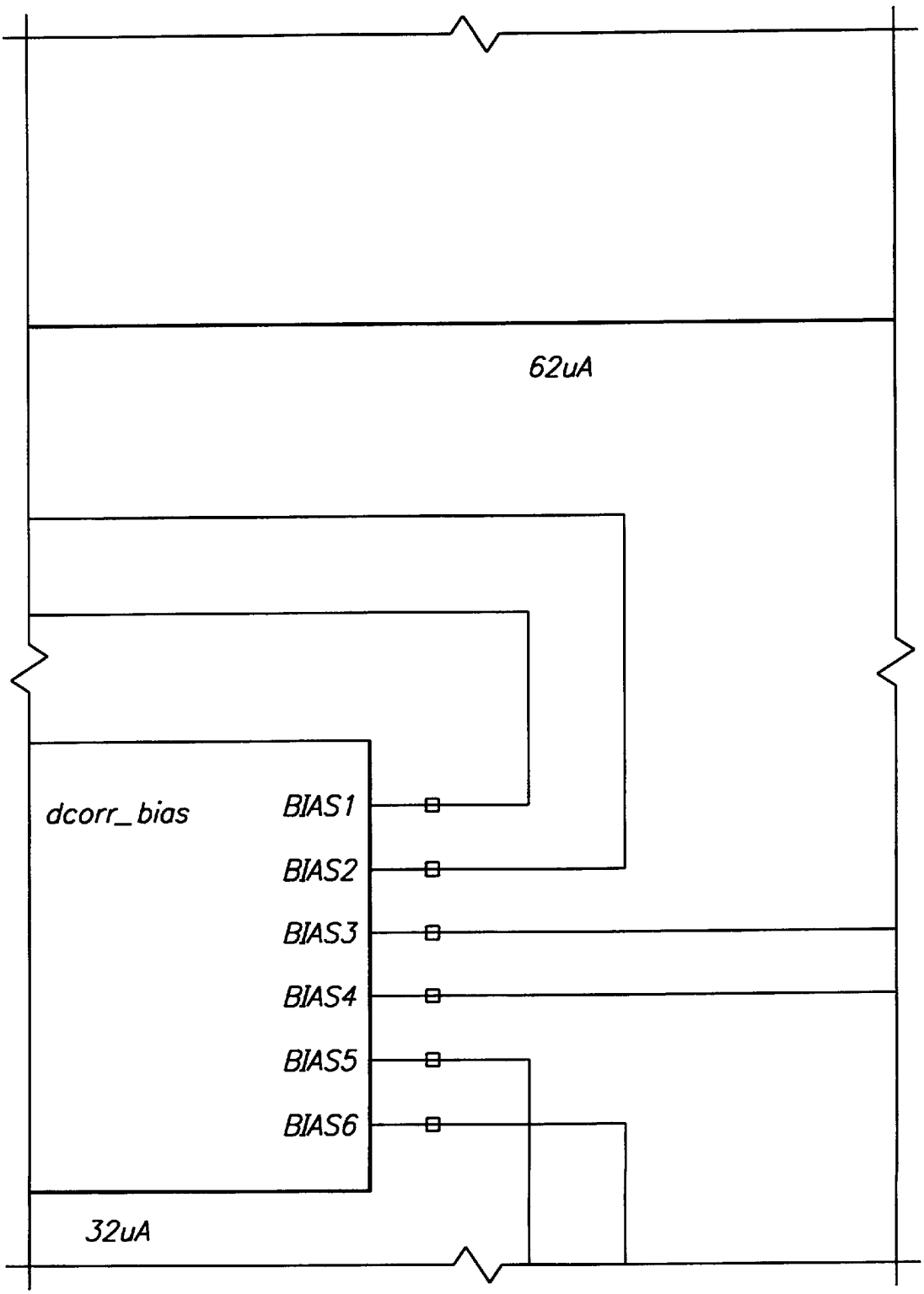


Fig 100.01CB

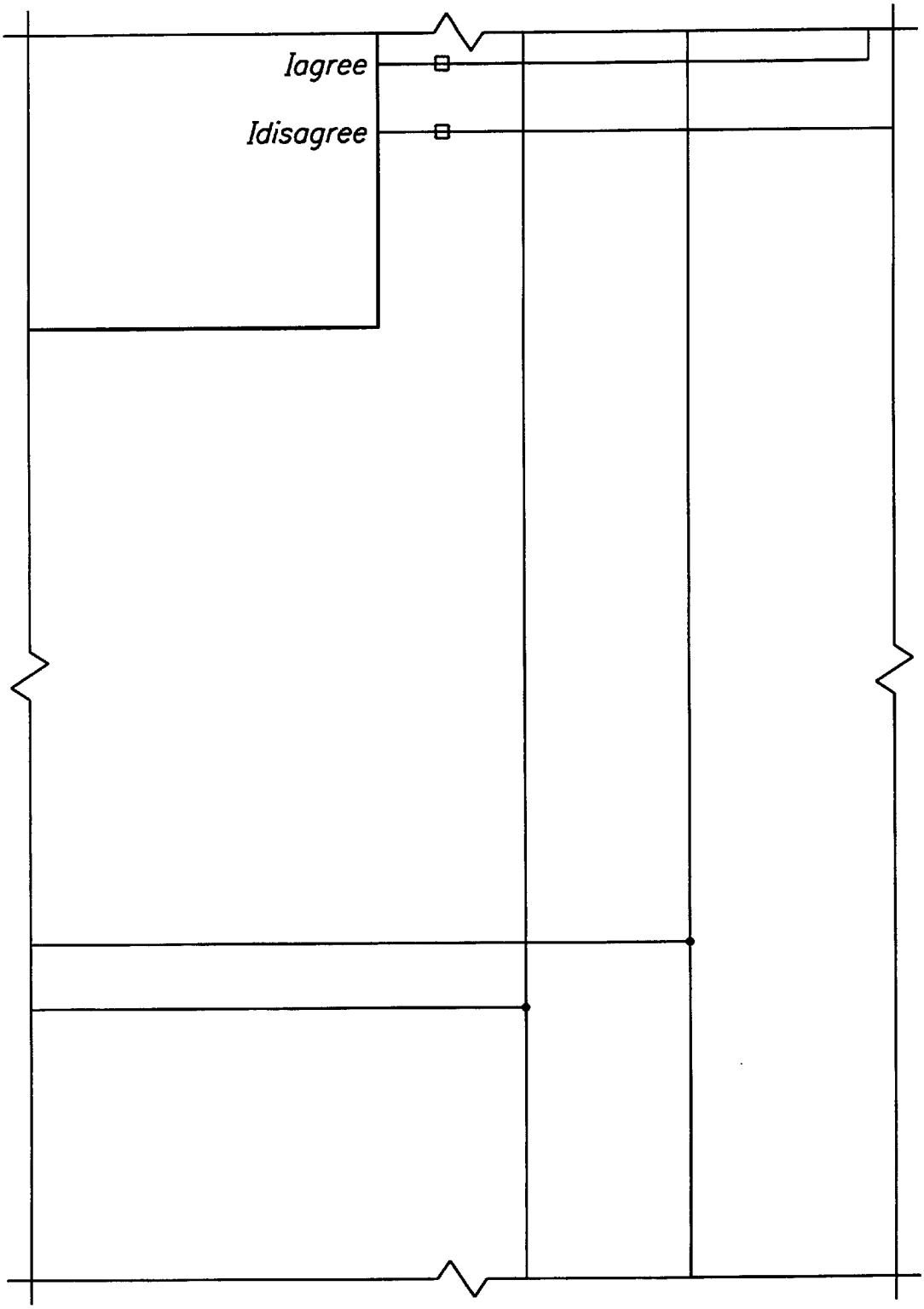
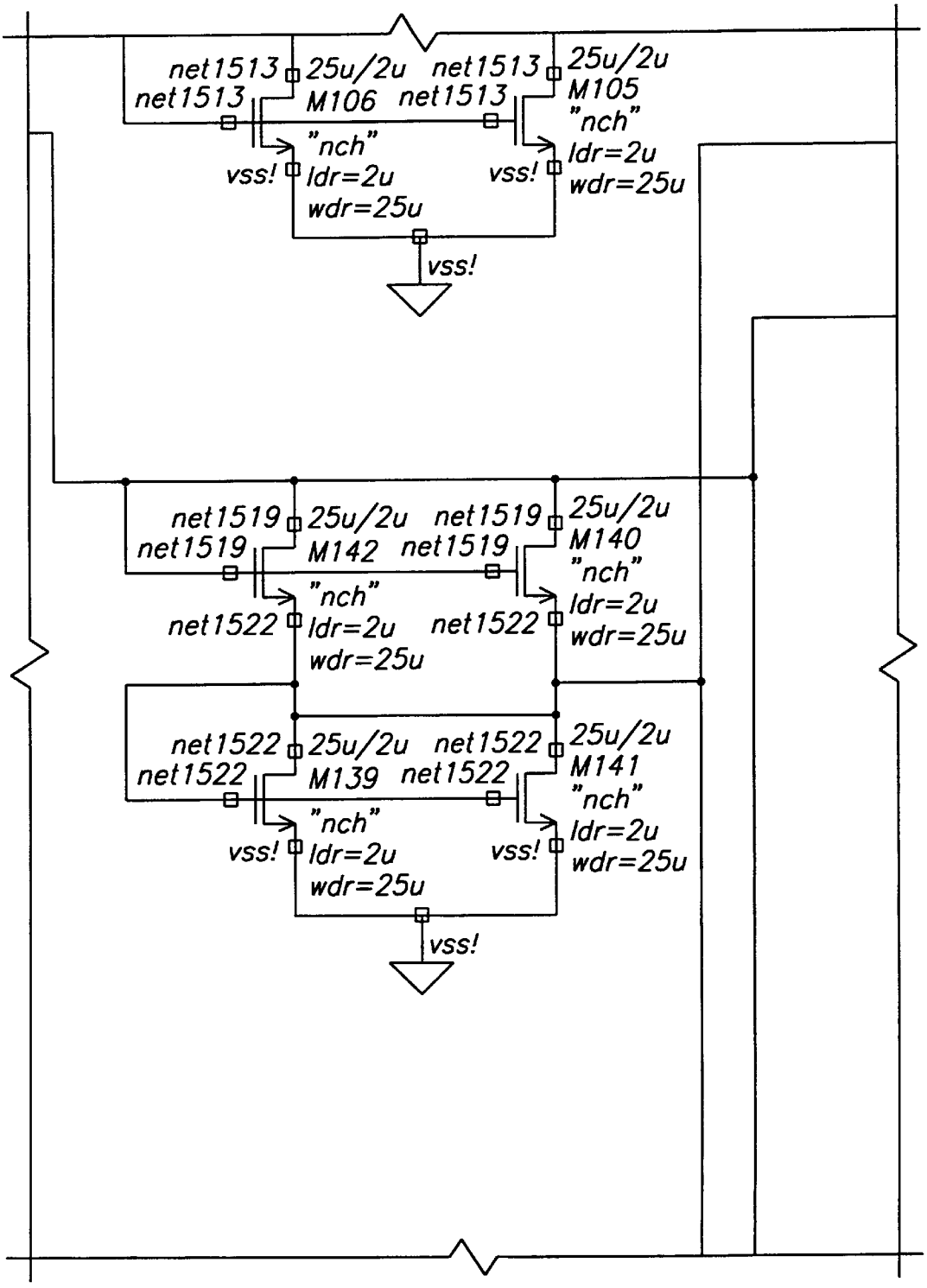


Fig 10,011C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ldr=2u
wdr=25u
vss!
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25u/2u
M105
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ldr=2u
wdr=25u
vss!
net1519
25u/2u
M142
"nch"
ldr=2u
wdr=25u
net1522
net1519
25u/2u
M140
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ldr=2u
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M139
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ldr=2u
wdr=25u
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net1522
25u/2u
M141
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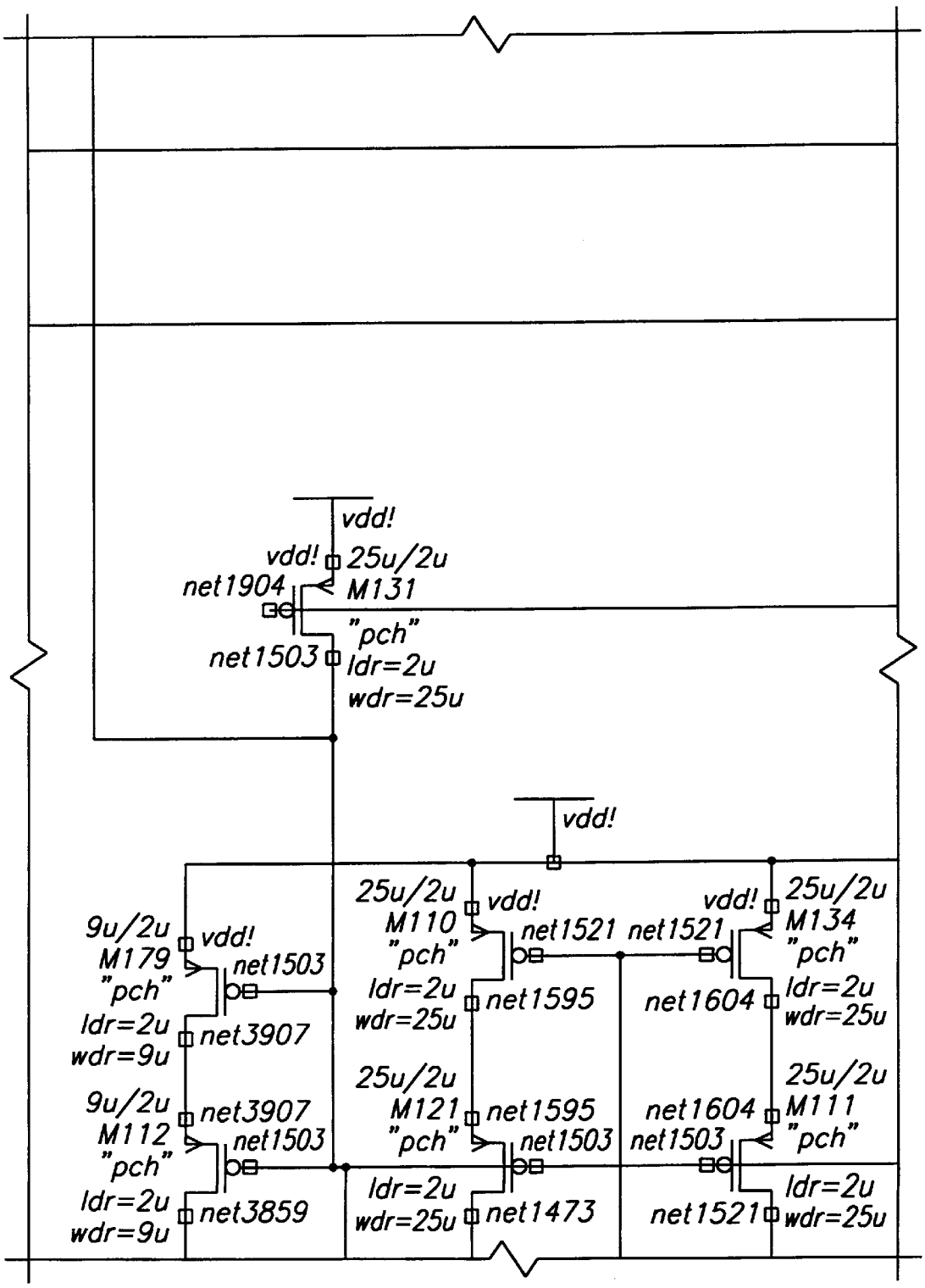
wdr=25u
vss!

Fig 100ICD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vdd!
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net1904
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ldr=2u
wdr=25u
vdd!
25u/2u
M110
"pch"
vdd!
net1521
net1521
vdd!
25u/2u
M134
"pch"
9u/2u
M179
"pch"
vdd!
net1503
ldr=2u
wdr=9u
net3907
ldr=2u
wdr=25u
net1595
net1604
ldr=2u
wdr=25u
25u/2u
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"pch"
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net1604
25u/2u
M111
"pch"
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M112
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net1503
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net1503
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ldr=2u
wdr=25u
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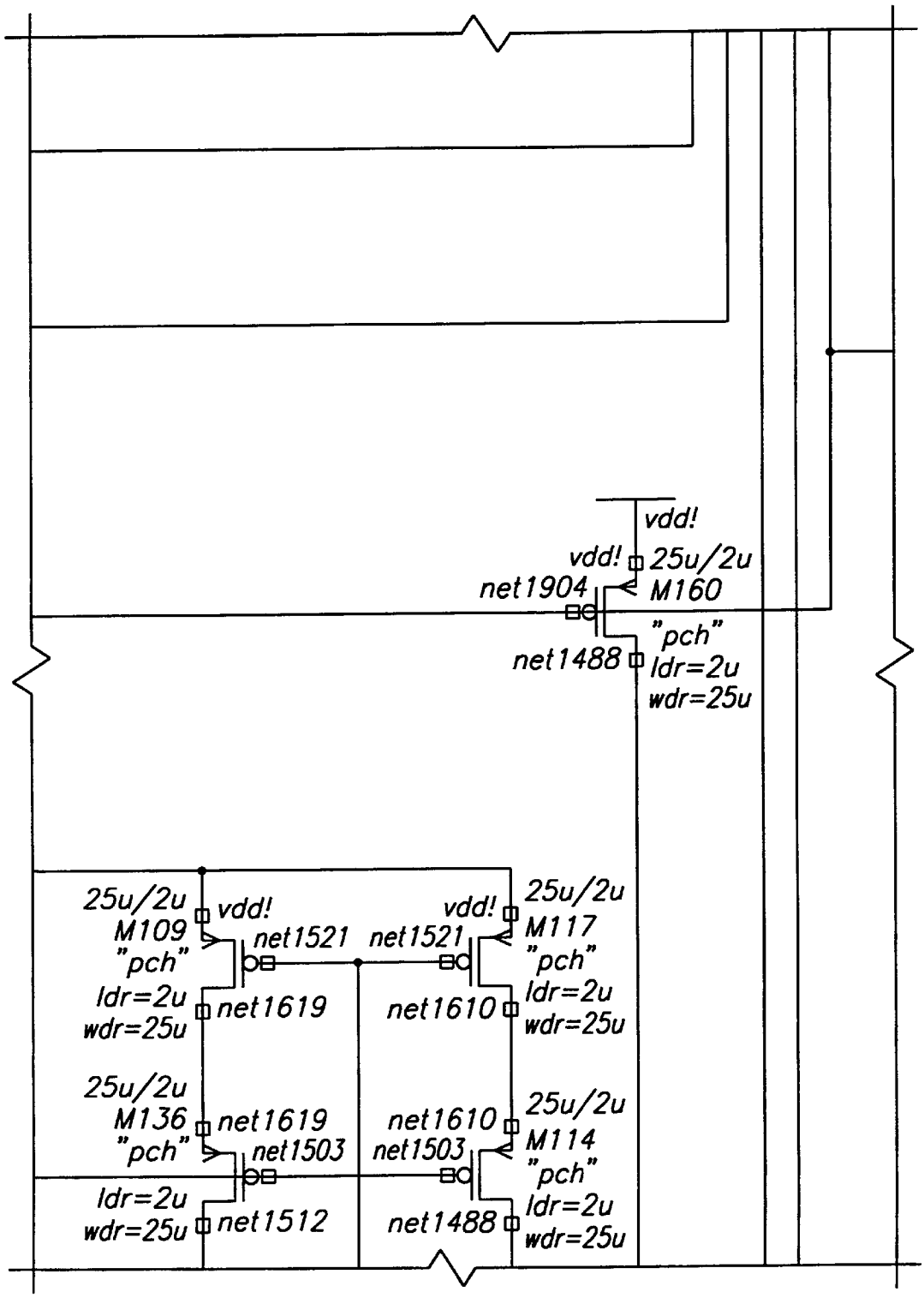
net1521
ldr=2u
wdr=25u

Fig 1003


vdd!
vdd!
25u/2u
M160
net1904
"pch"
net1488
ldr=2u
wdr=25u
25u/2u
M109
"pch"
vdd!
net1521
net1521
vdd!
25u/2u
M117
"pch"
ldr=2u
wdr=25u
net1619
net1610
ldr=2u
wdr=25u
25u/2u
M136
"pch"
net1619
net1503
net1610
net1503
25u/2u
M114
"pch"
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wdr=25u
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net1488
ldr=2u
wdr=25u

Fig 1001CF

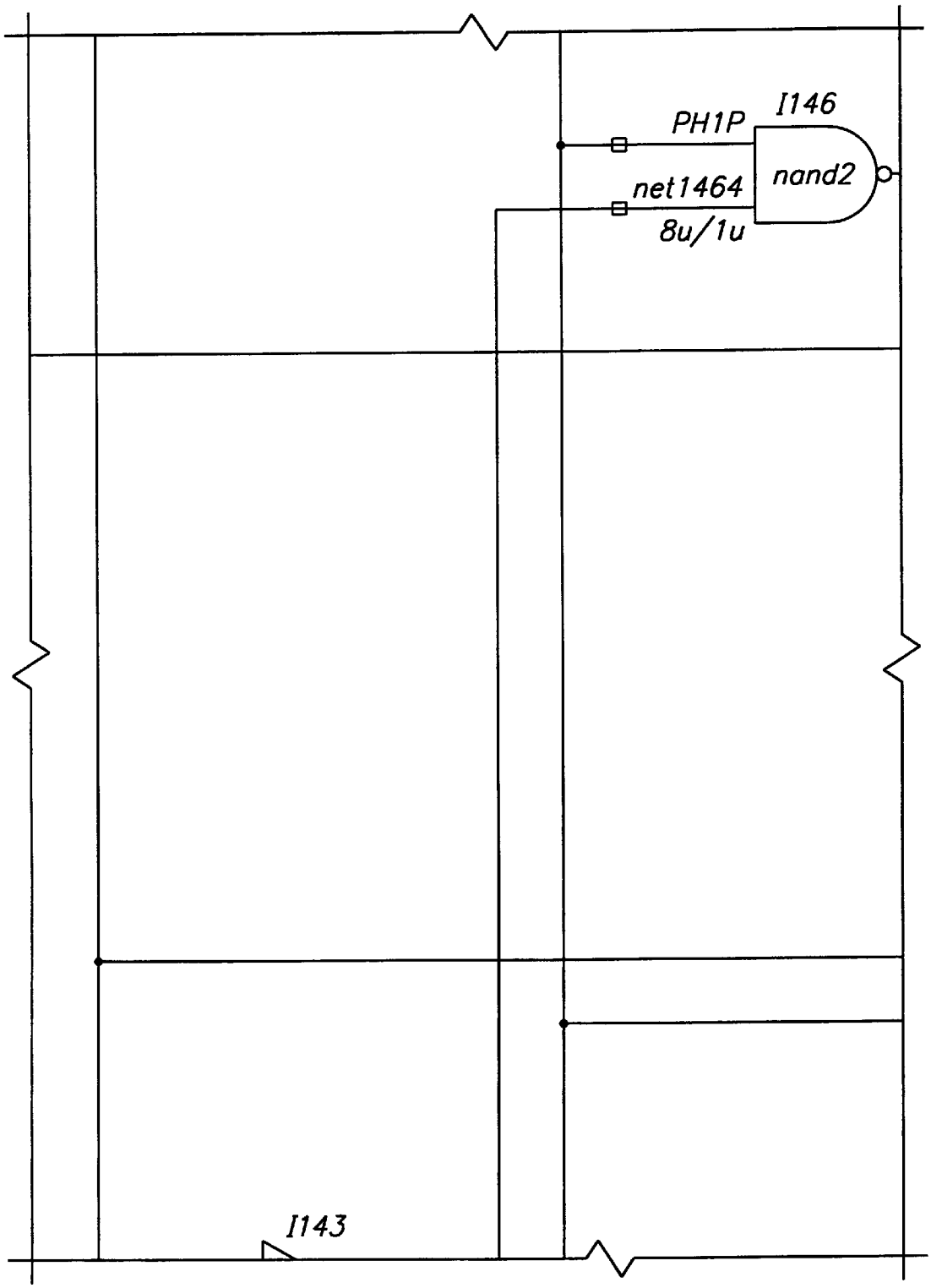
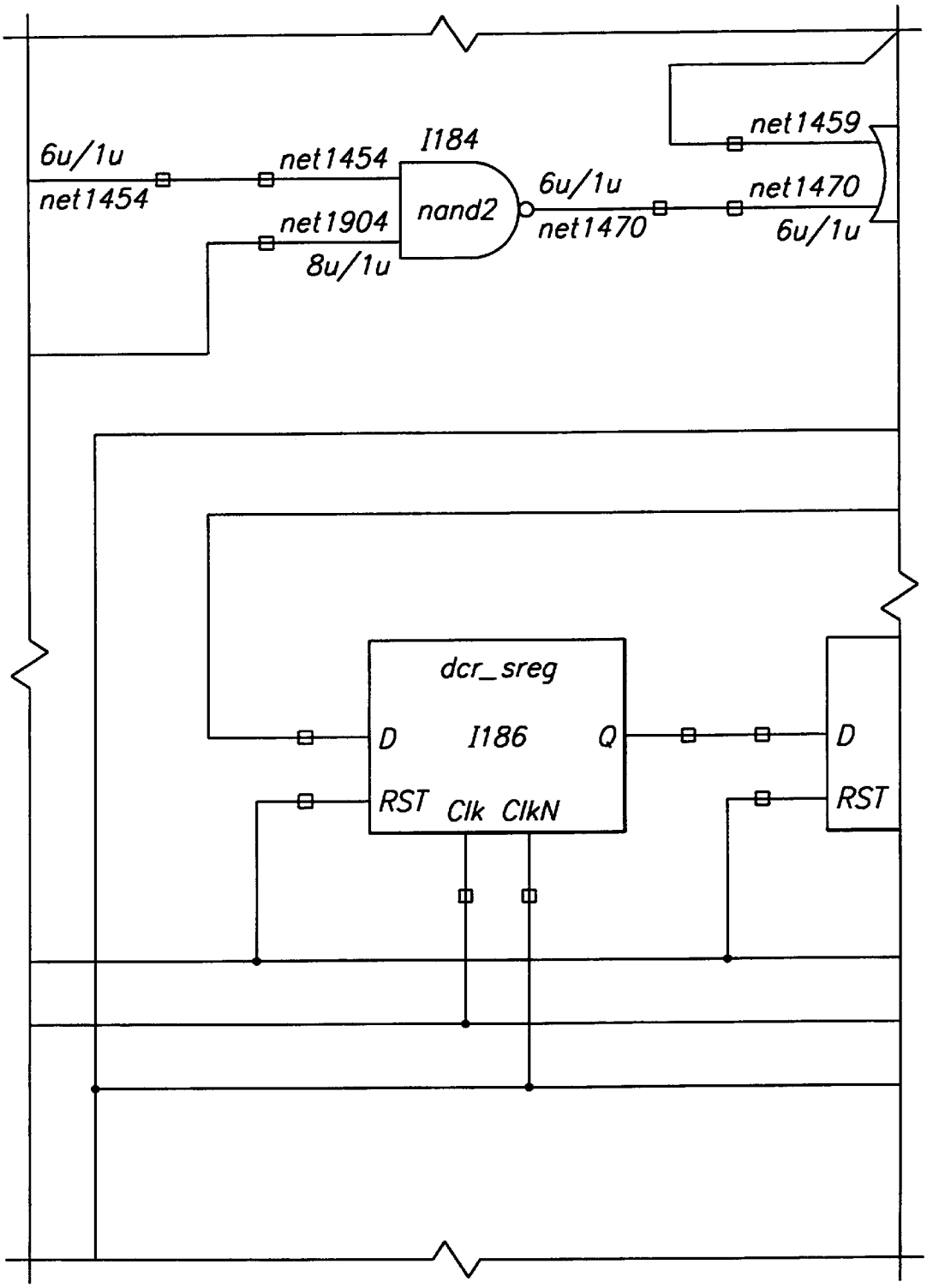


Fig 10.0116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net1454
I184
nand2
net1904
8u/1u
6u/1u
net1470
net1459
net1470
6u/1u
dcr_sreg
D
I186
Q
RST
Clk
ClkN
D
RST

Fig 10.01CH

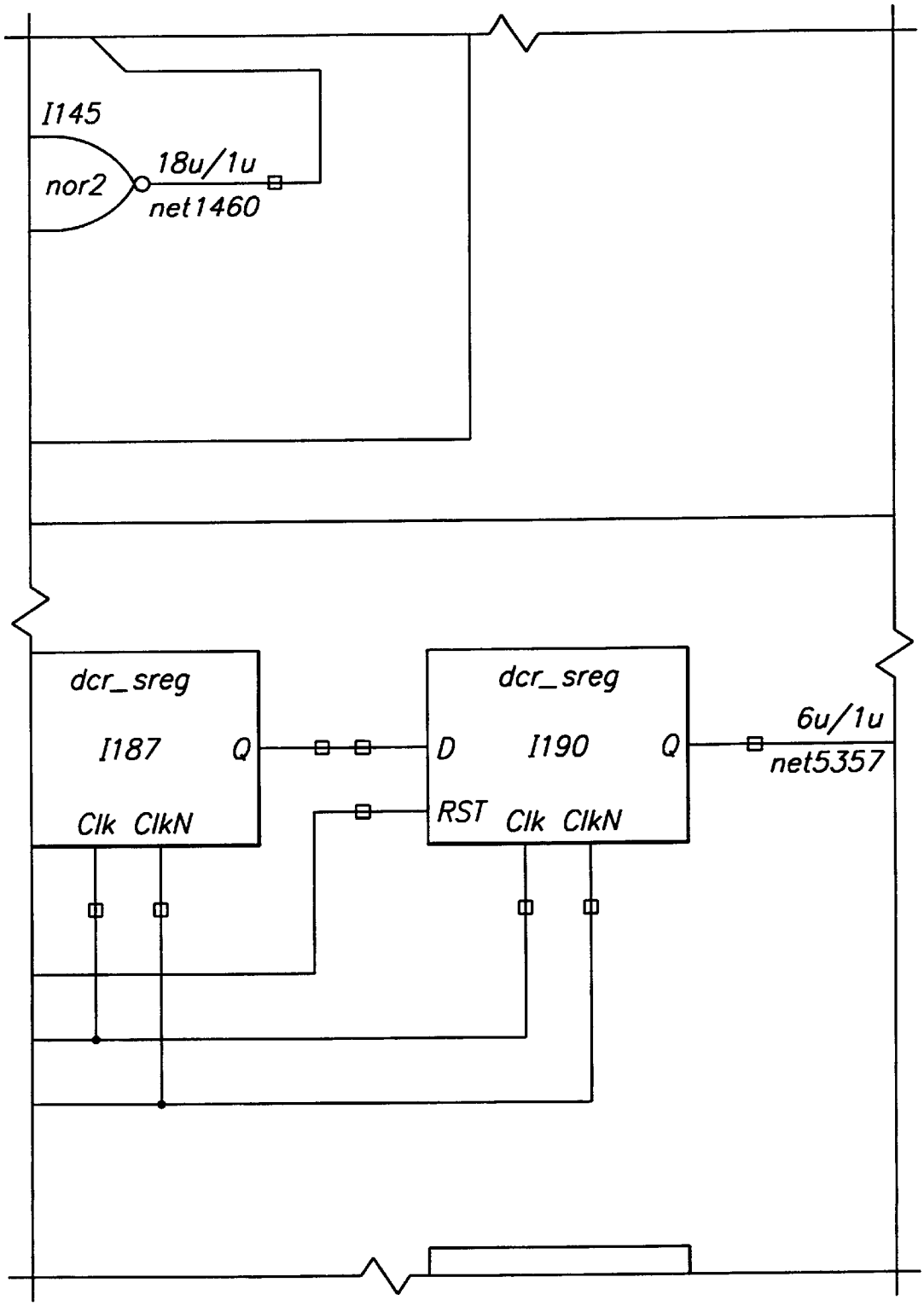

I145
nor2
18u/1u
net1460
dcr_sreg
I187
Q
Clk ClkN
dcr_sreg
D
I190
Q
RST Clk ClkN
6u/1u
net5357

Fig 100,101

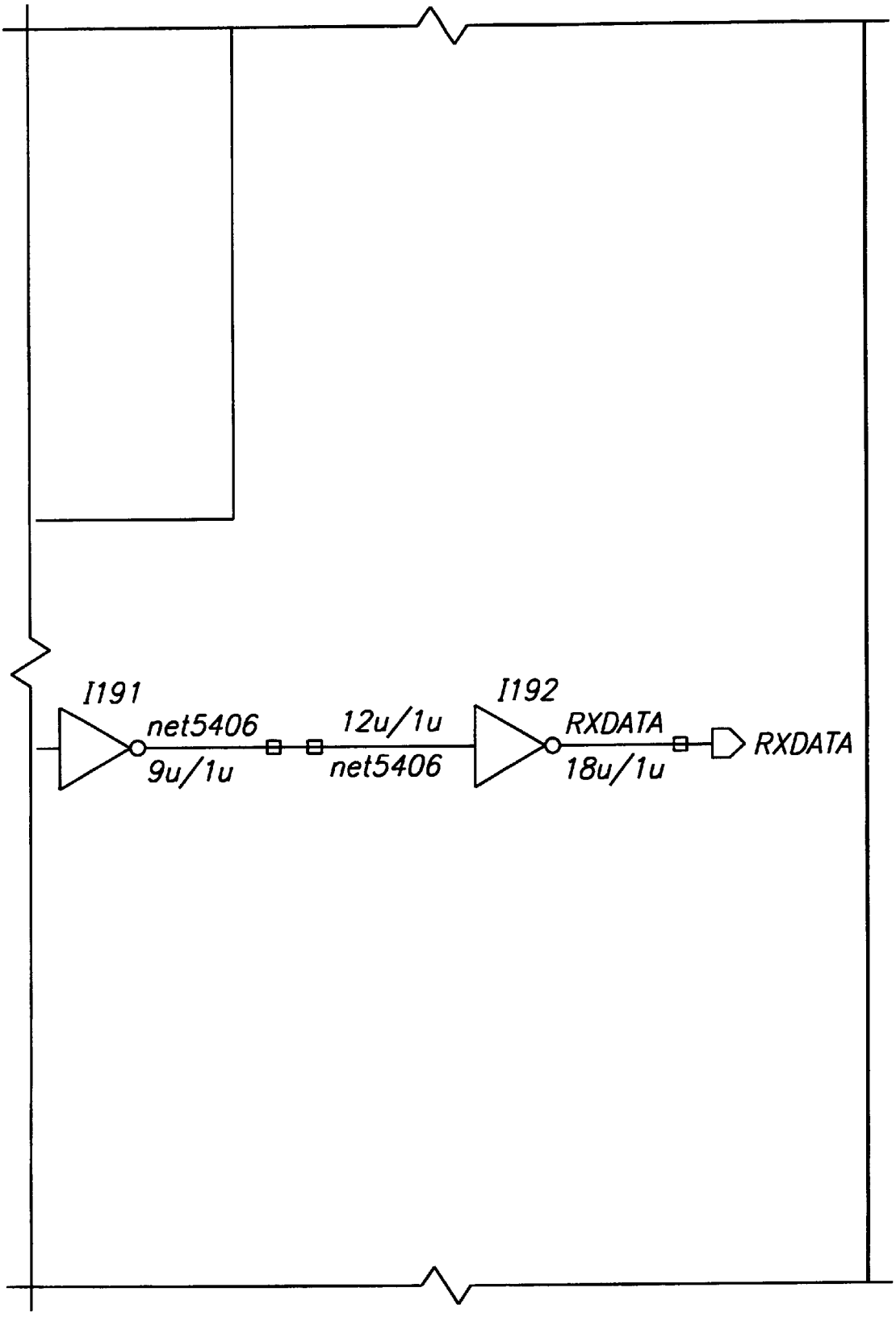


Fig 100.0110a

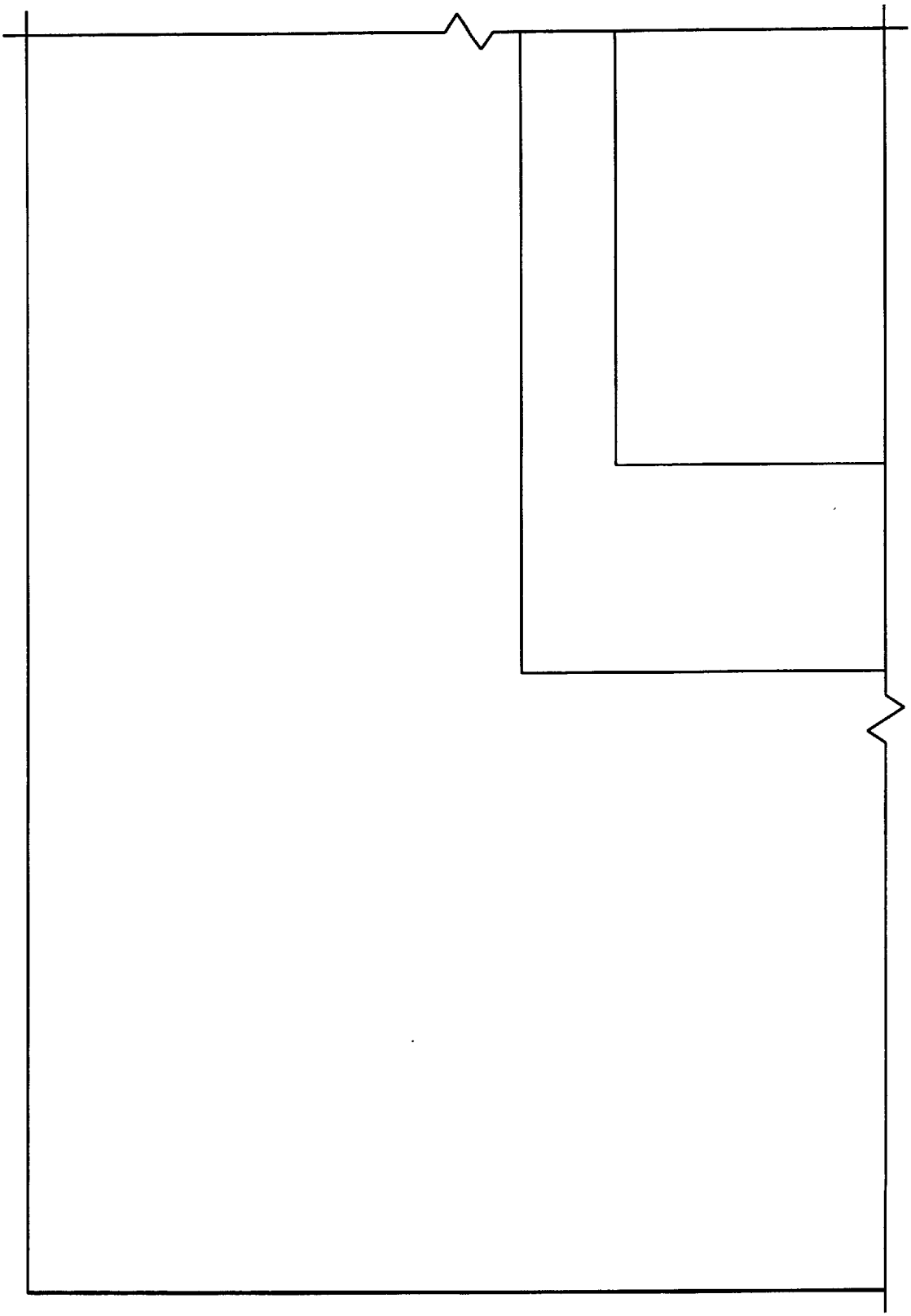


Fig 10.010B

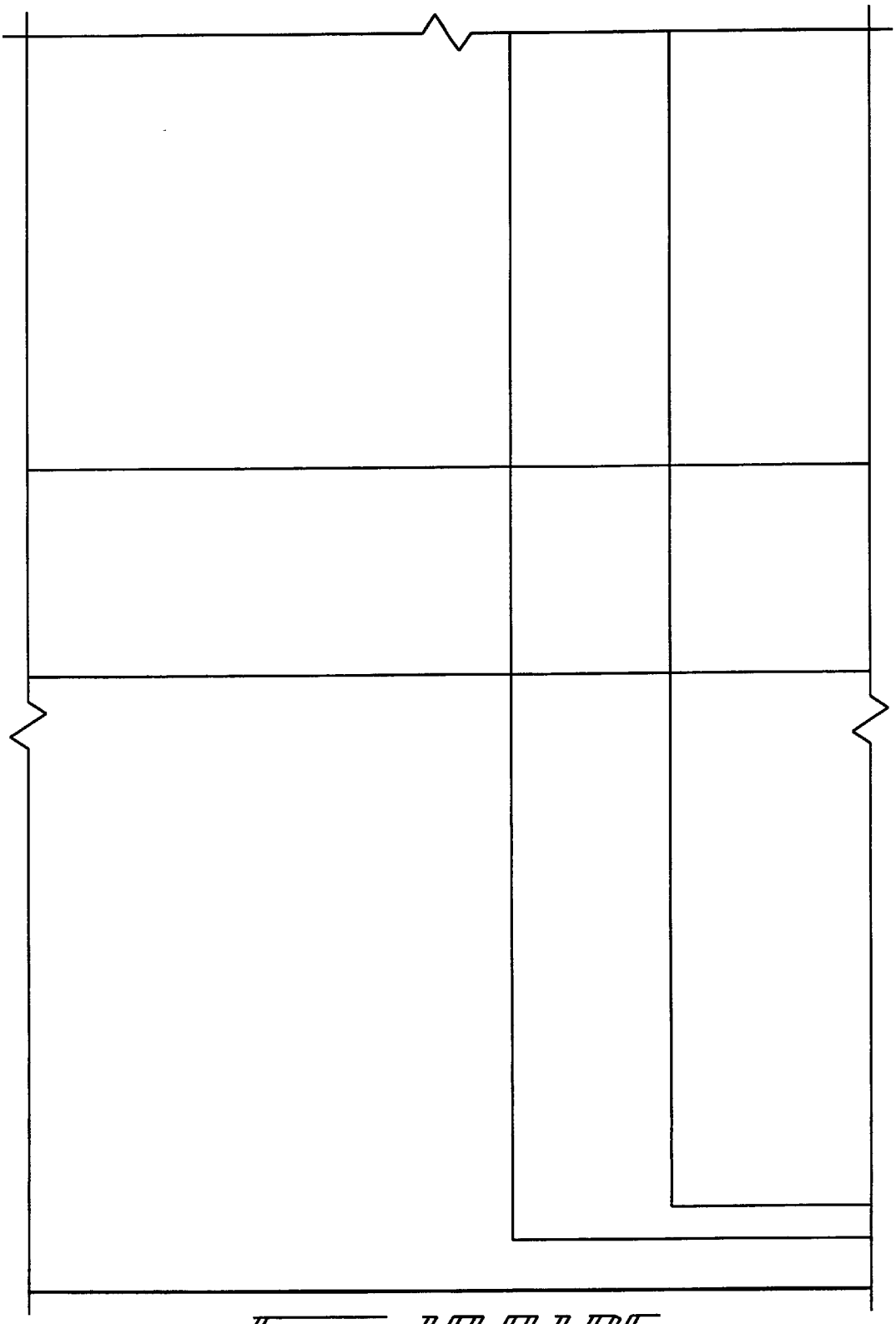


Fig 10.010C

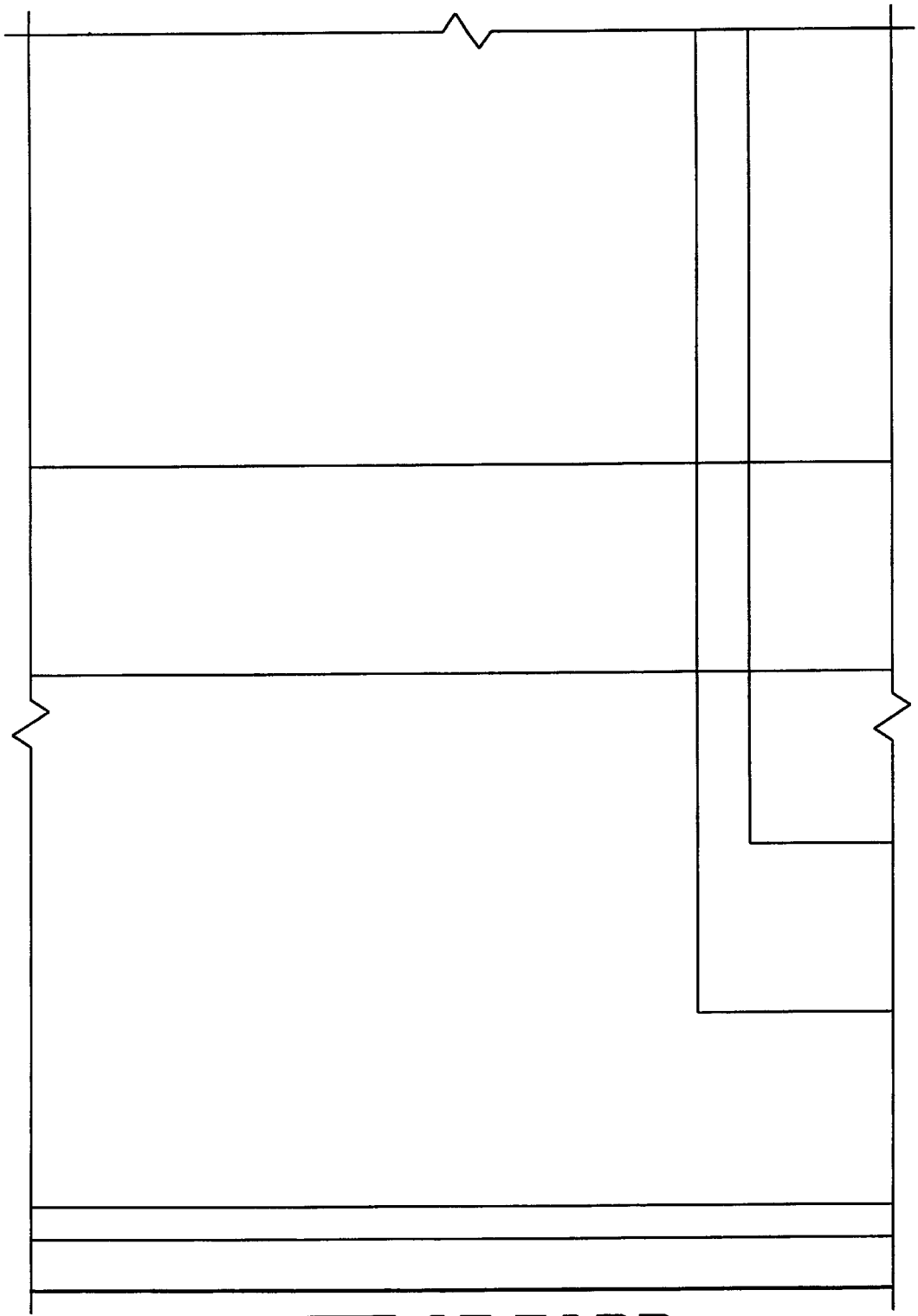
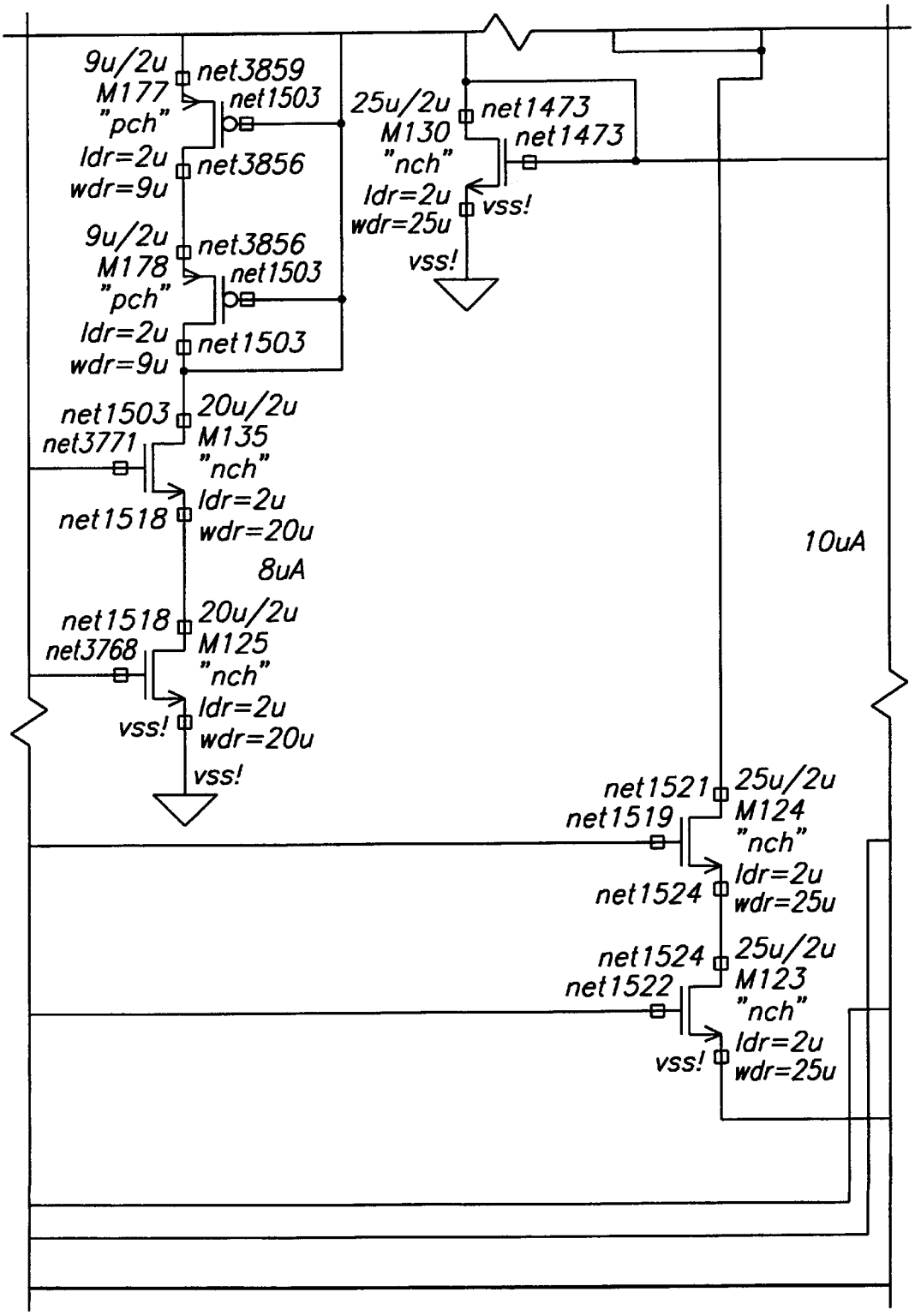


Fig 10.0100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net3856
9u/2u
M178
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net3856
net1503
net1503
25u/2u
M130
"nch"
ldr=2u
wdr=25u
net1473
net1473
vss!
vss!
net1503
net3771
net1518
20u/2u
M135
"nch"
ldr=2u
wdr=20u
8uA
net1518
net3768
vss!
20u/2u
M125
"nch"
ldr=2u
wdr=20u
vss!
10uA
net1521
net1519
25u/2u
M124
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ldr=2u
wdr=25u
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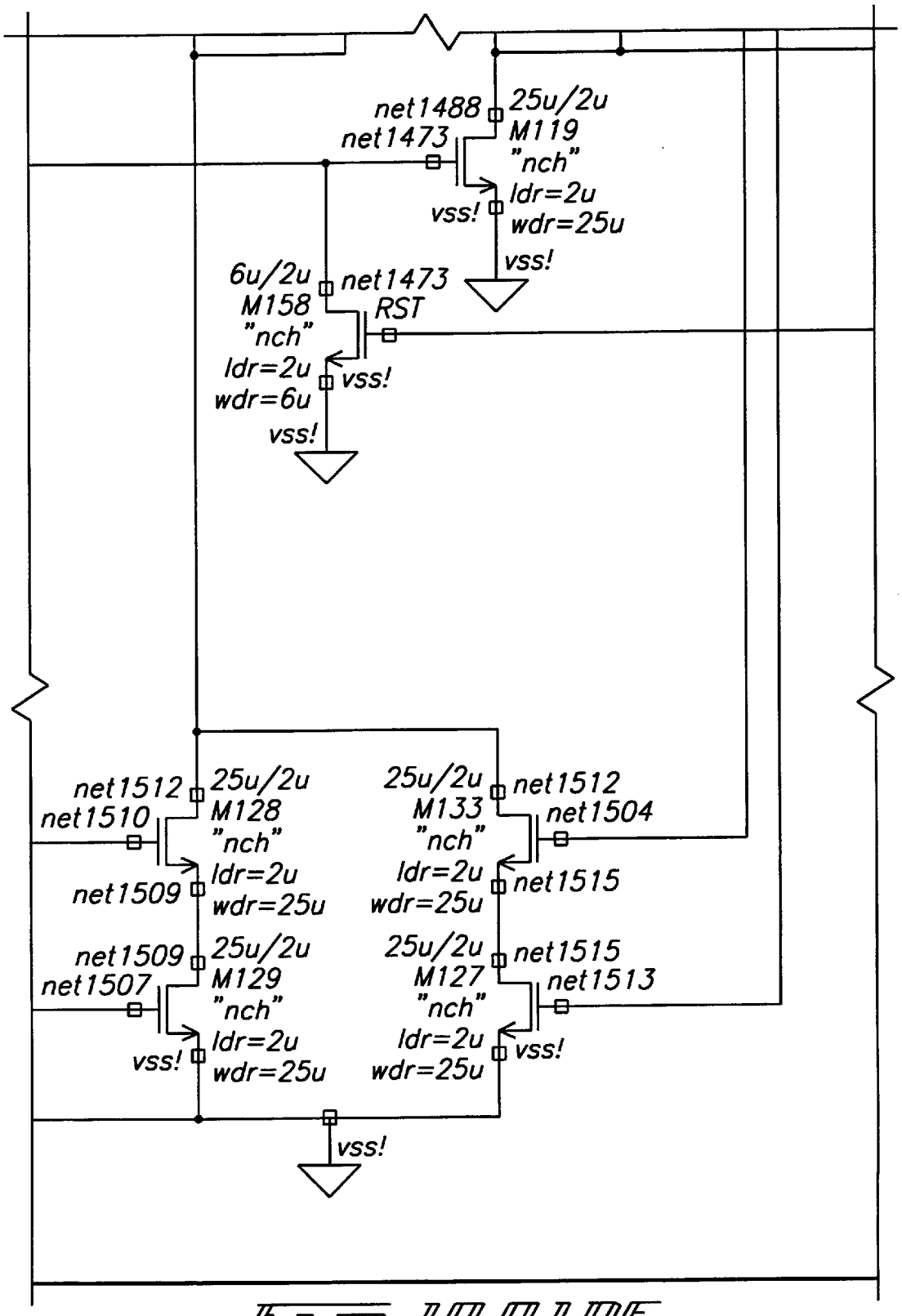
net1524
net1522
vss!
25u/2u
M123
"nch"
ldr=2u
wdr=25u

Fig 10.01DE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net1473
25u/2u
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ldr=2u
wdr=25u
vss!
vss!
6u/2u
M158
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ldr=2u
wdr=6u
net1473
RST
vss!
vss!
net1512
net1510
25u/2u
M128
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wdr=25u
net1509
net1509
net1507
25u/2u
M129
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wdr=25u
vss!
25u/2u
M133
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net1512
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M127
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net1513
vss!
vss!

Fig 100F

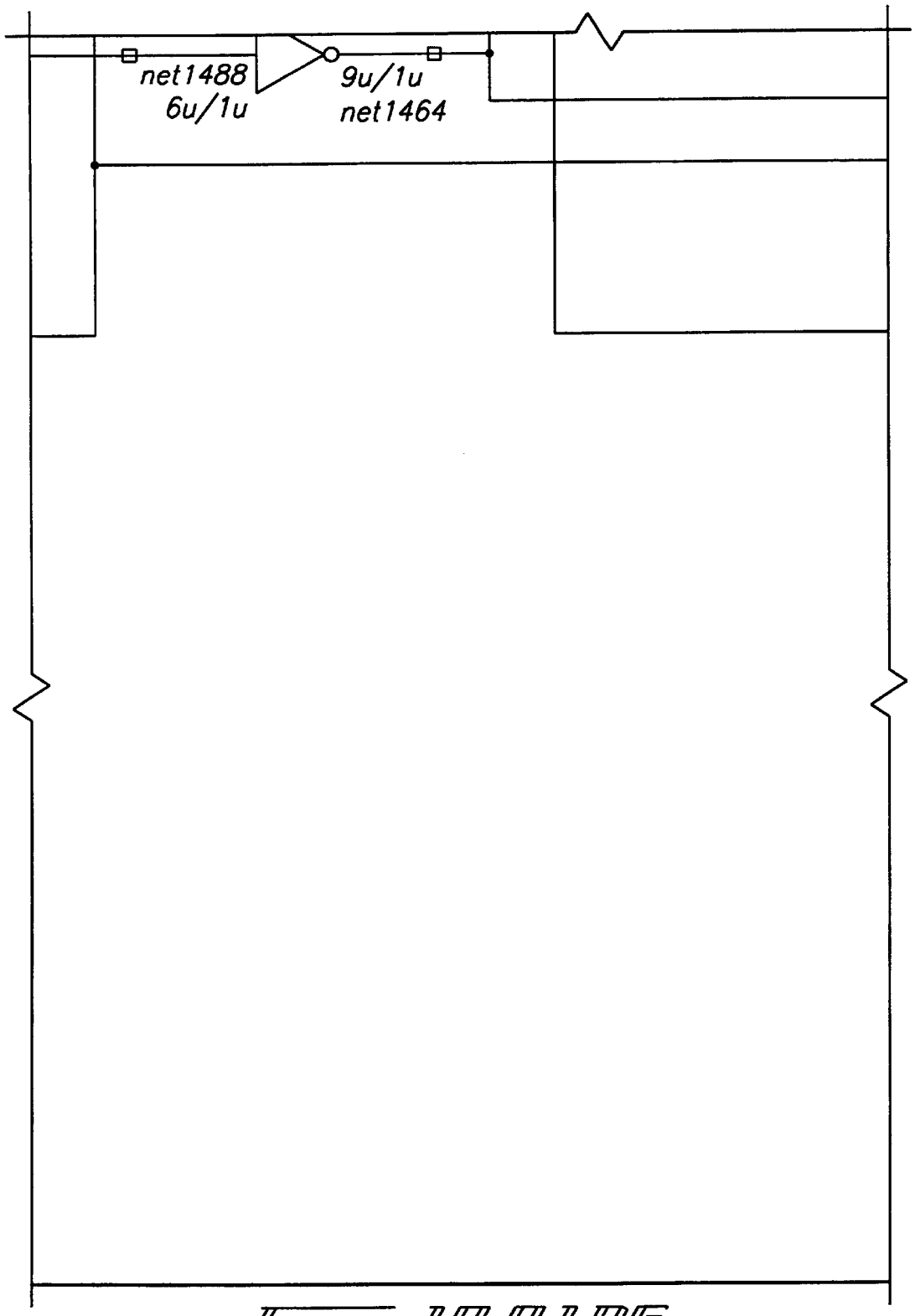


Fig 10.0106

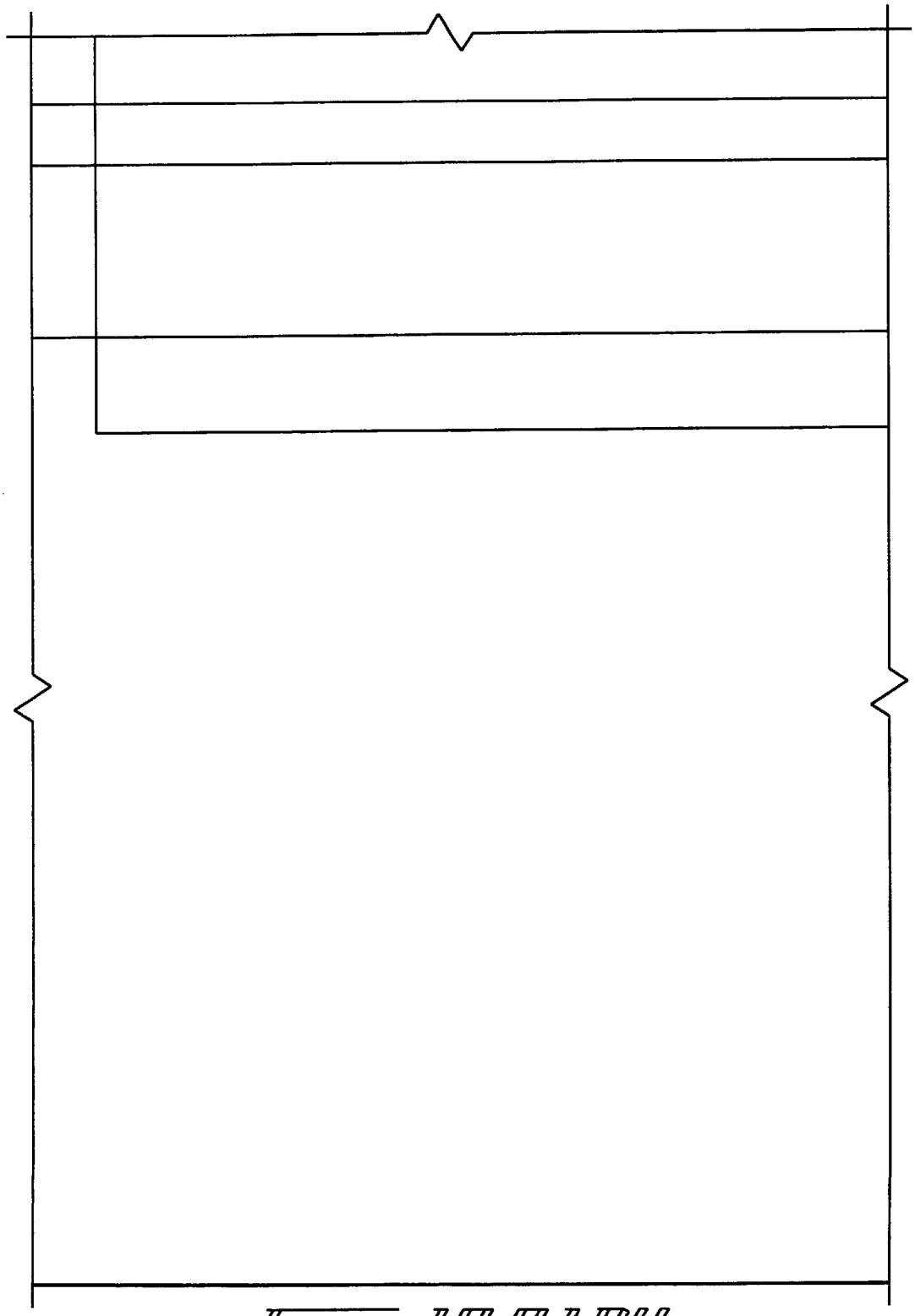


Fig 10.011H

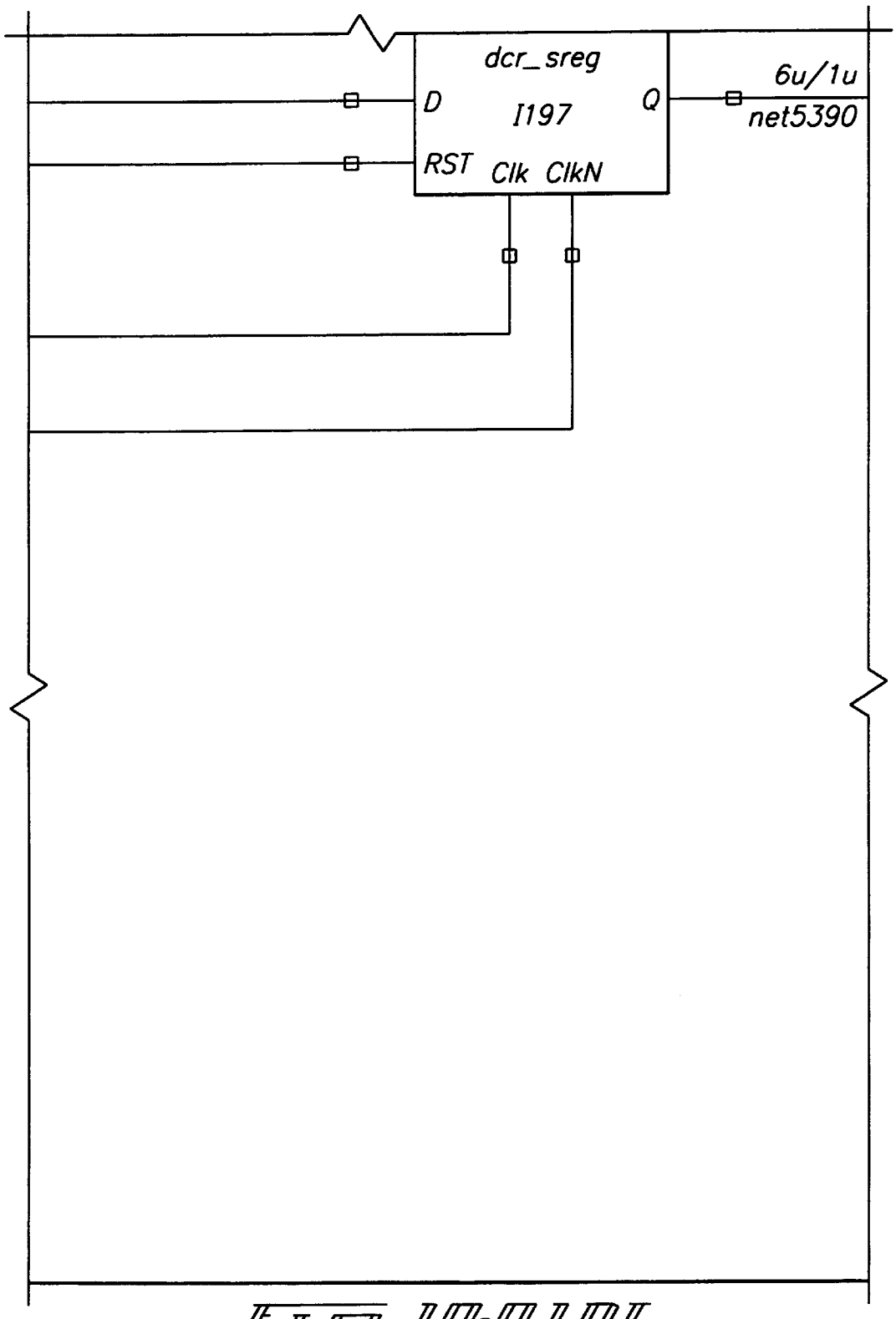


Fig 100,101

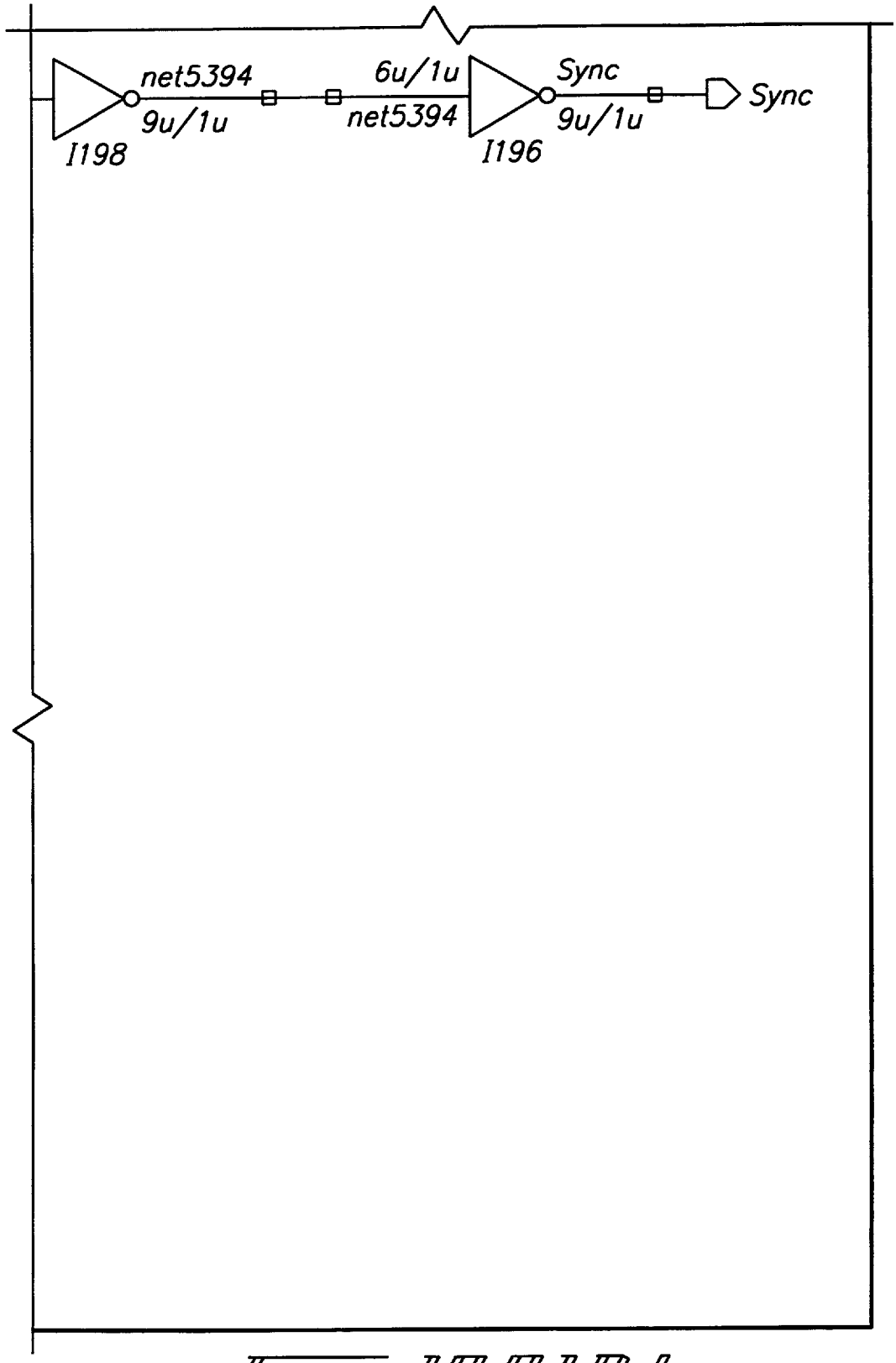
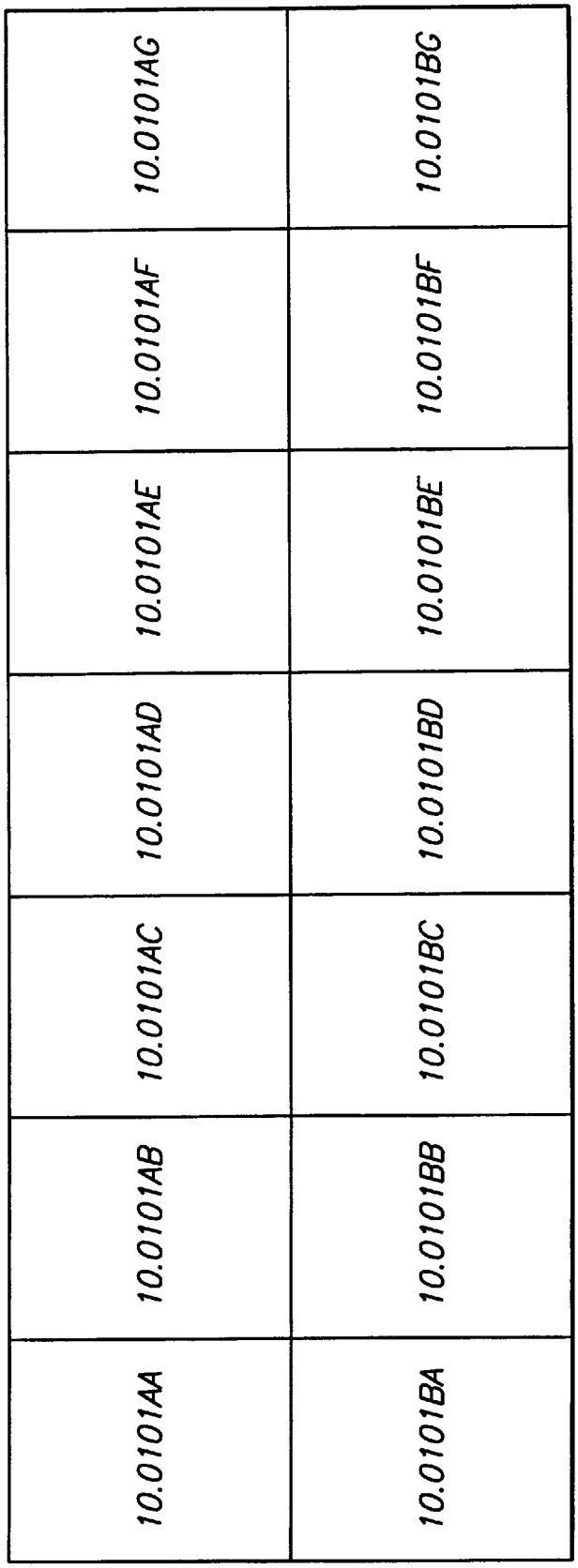


Fig 100,001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10.0101BC
10.0101BD
10.0101BE
10.0101BF
10.0101BG

FIG. 2846

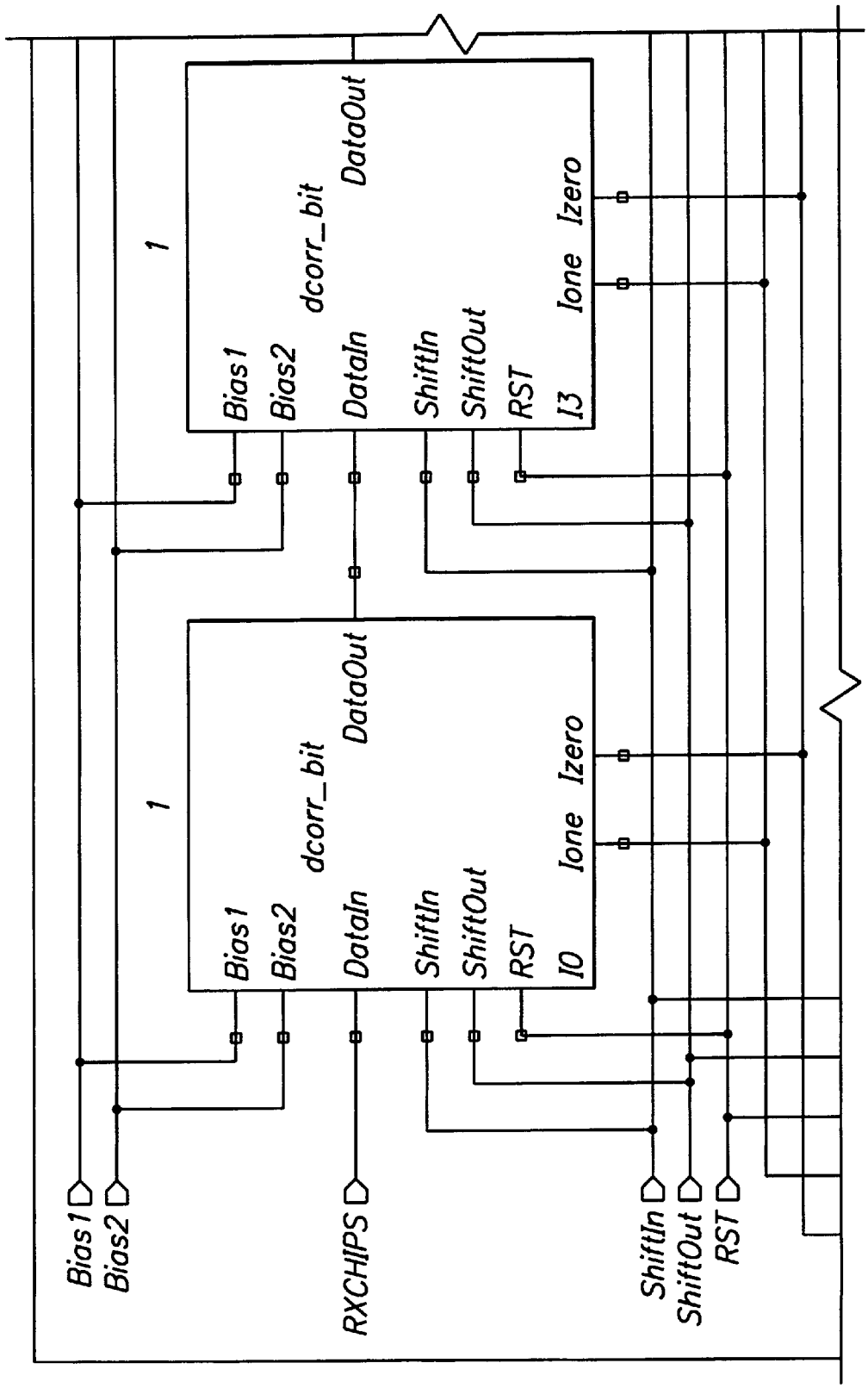


FIG. 1100.0011.1111

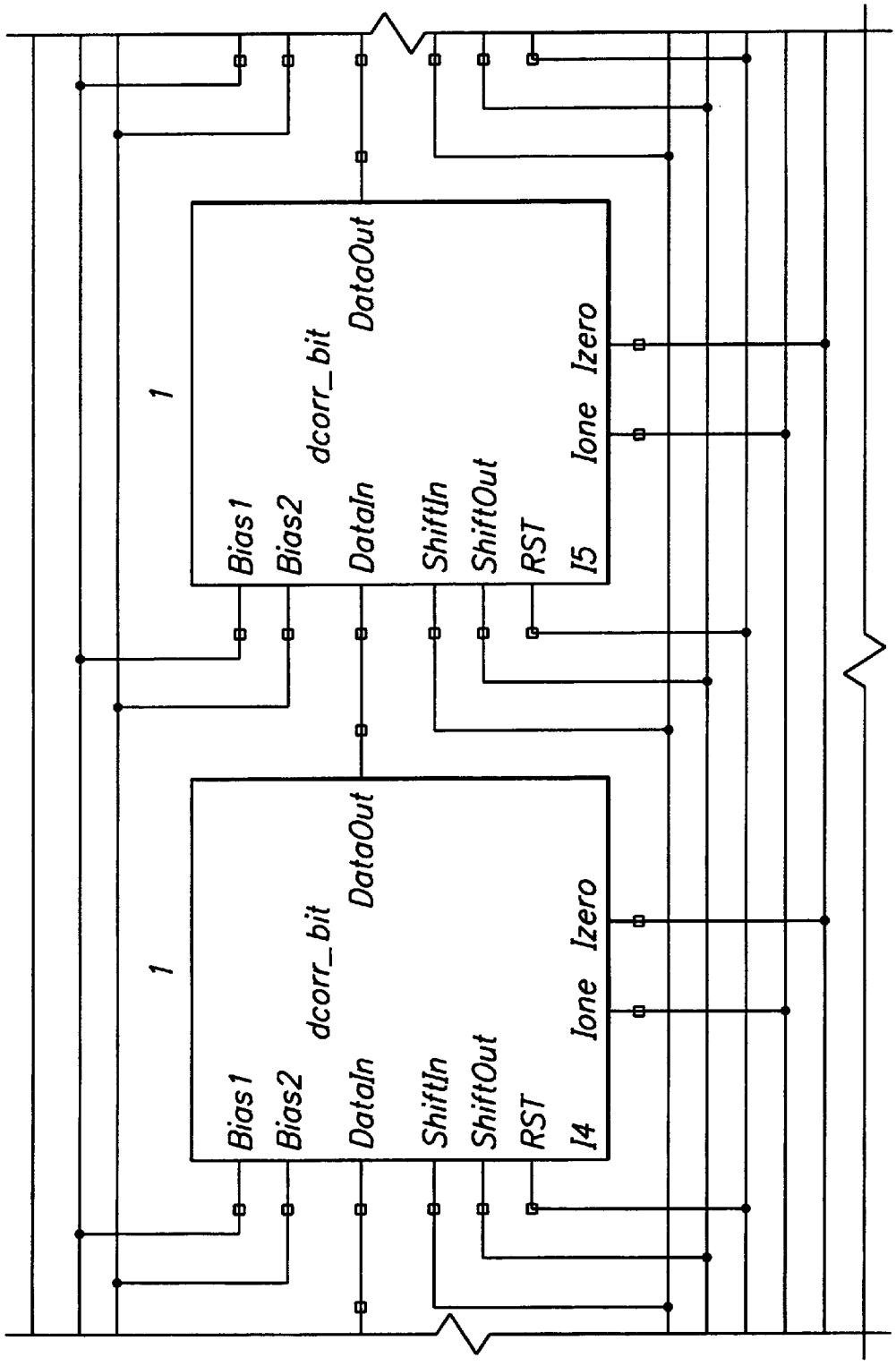


Fig 1100.0011A

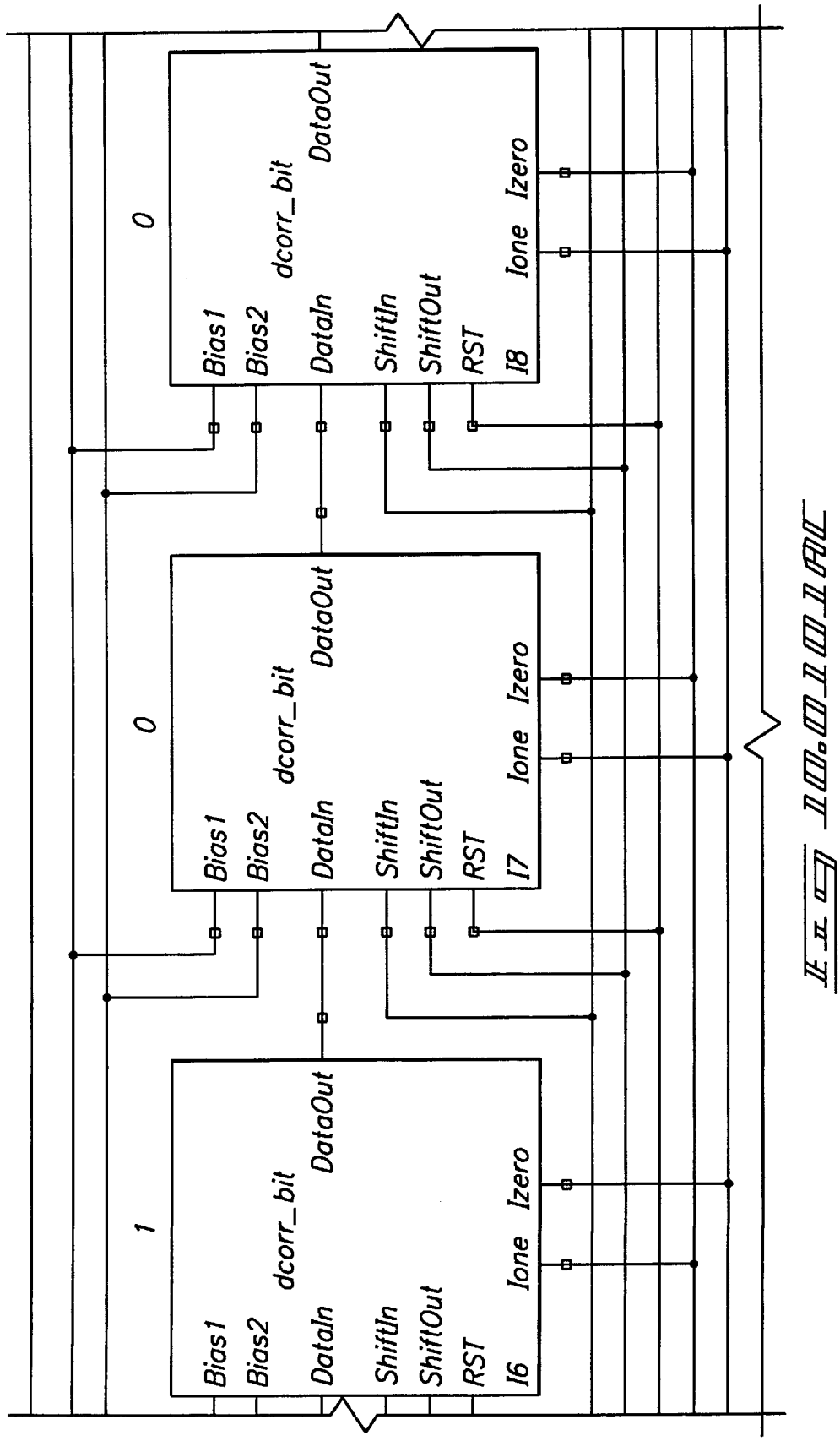

0
dcorr_bit
Bias1
Bias2
DataIn
ShiftIn
ShiftOut
RST
I8
DataOut
Ione
Izero
0
dcorr_bit
Bias1
Bias2
DataIn
ShiftIn
ShiftOut
RST
I7
DataOut
Ione
Izero
1
dcorr_bit
Bias1
Bias2
DataIn
ShiftIn
ShiftOut
RST
I6
DataOut
Ione
Izero

FIG. 100,001

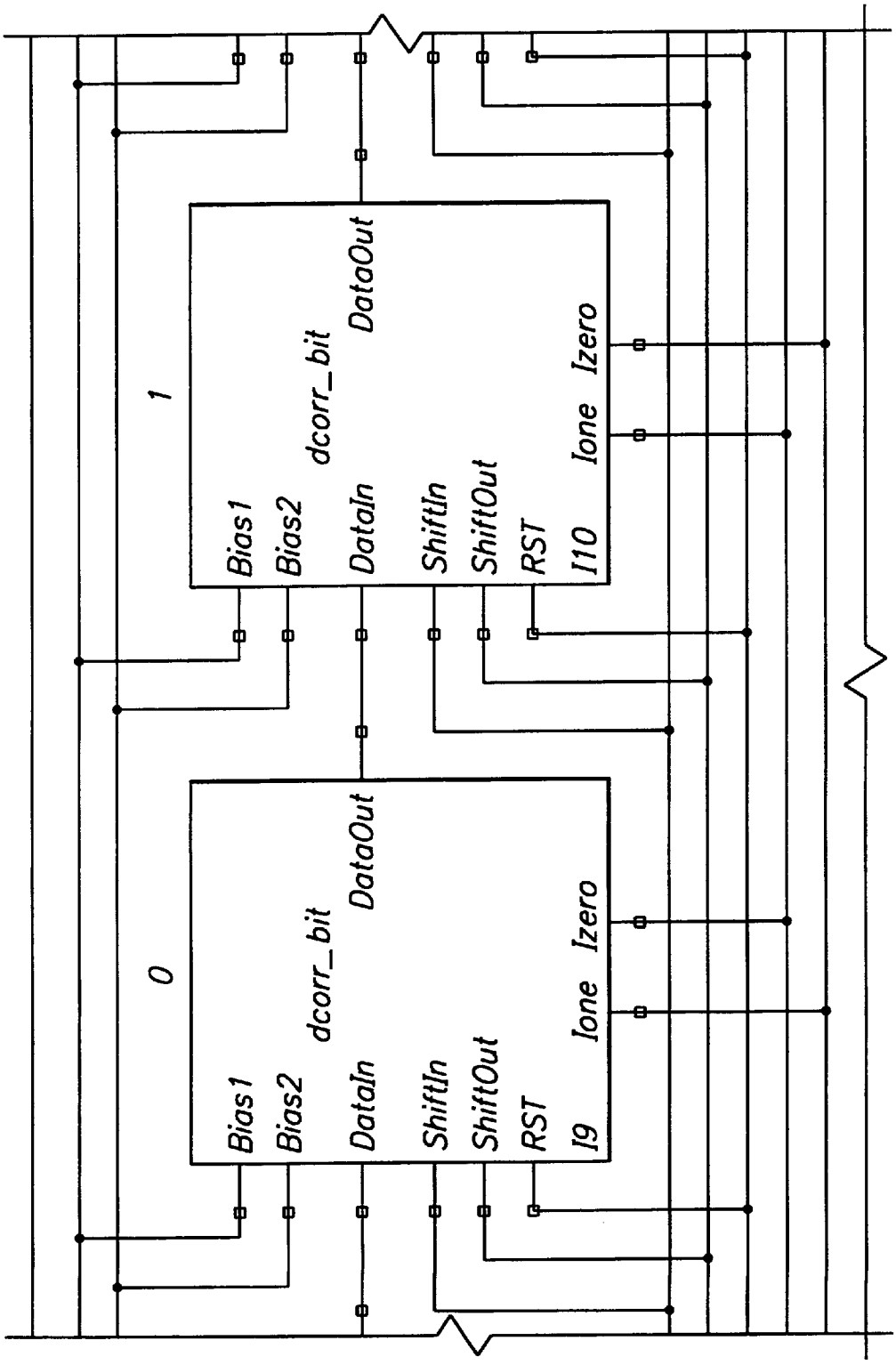


FIG. 100.0011.1010

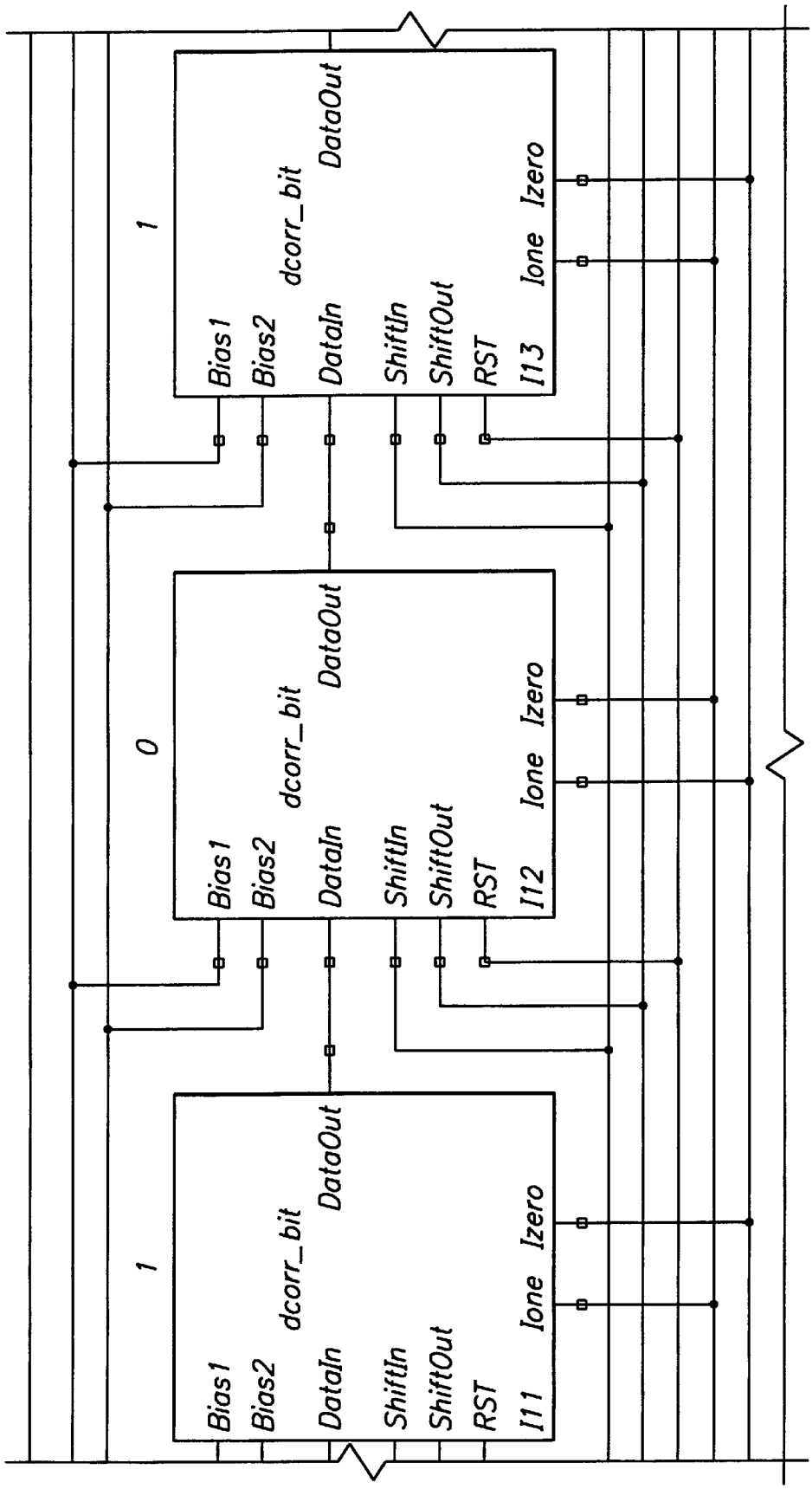


FIG 100.00110AE

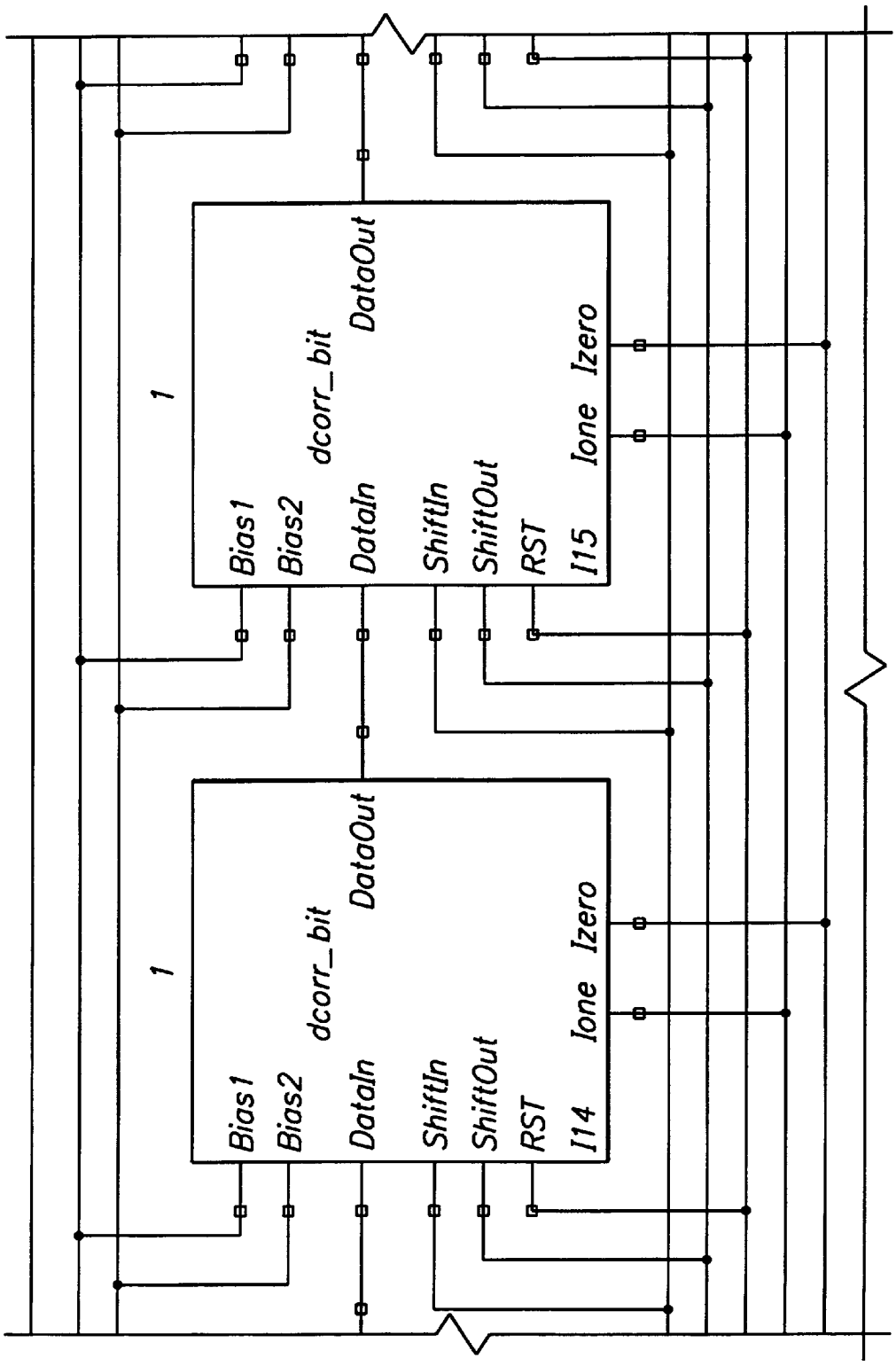


FIG. 1100,1001,1AF

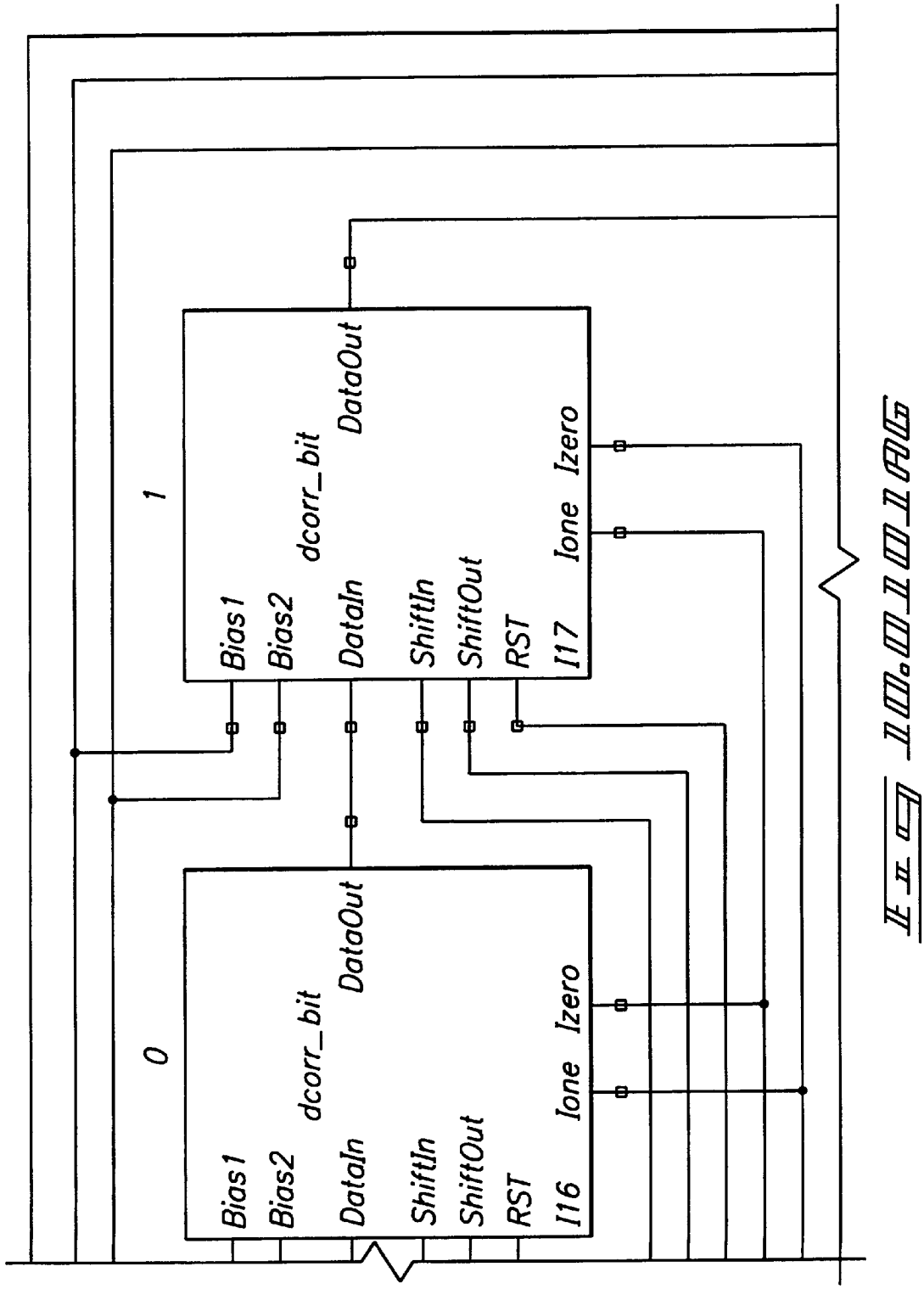


FIG 100.00110AG

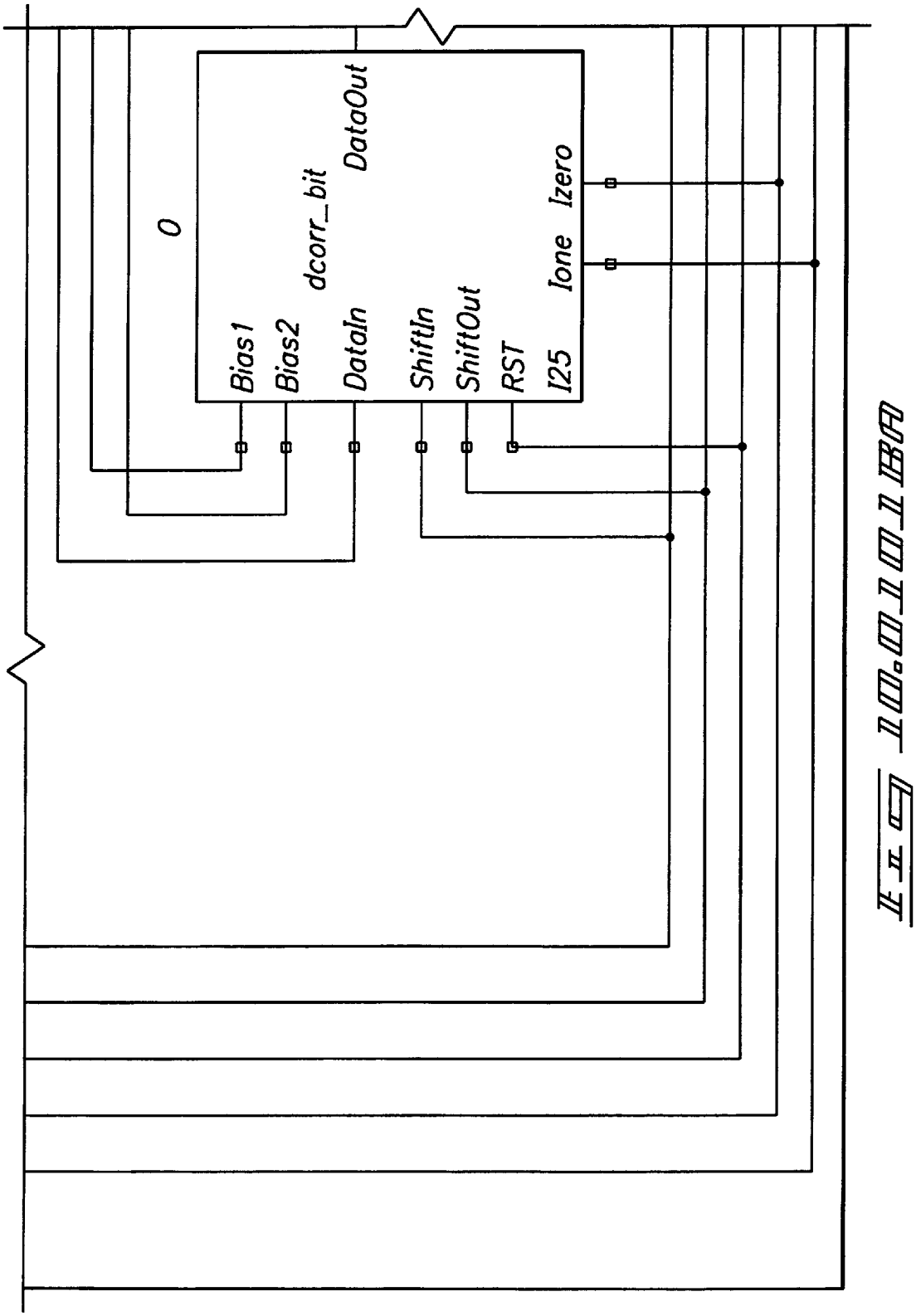
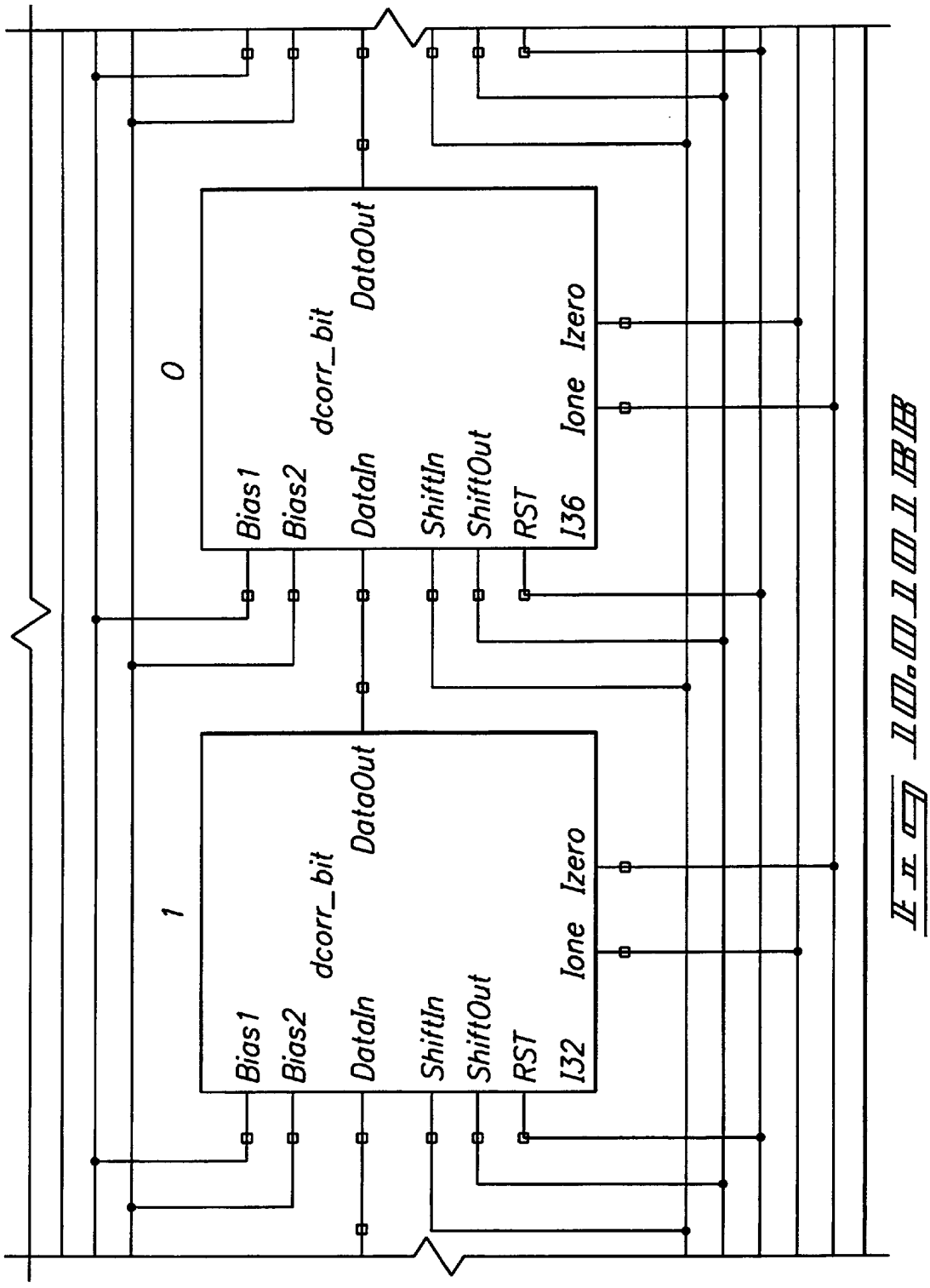


FIG 100.00110BA


0
dcorr_bit
DataOut
Bias1
Bias2
DataIn
ShiftIn
ShiftOut
RST
I36
Ione
Izero
1
dcorr_bit
DataOut
Bias1
Bias2
DataIn
ShiftIn
ShiftOut
RST
I32
Ione
Izero

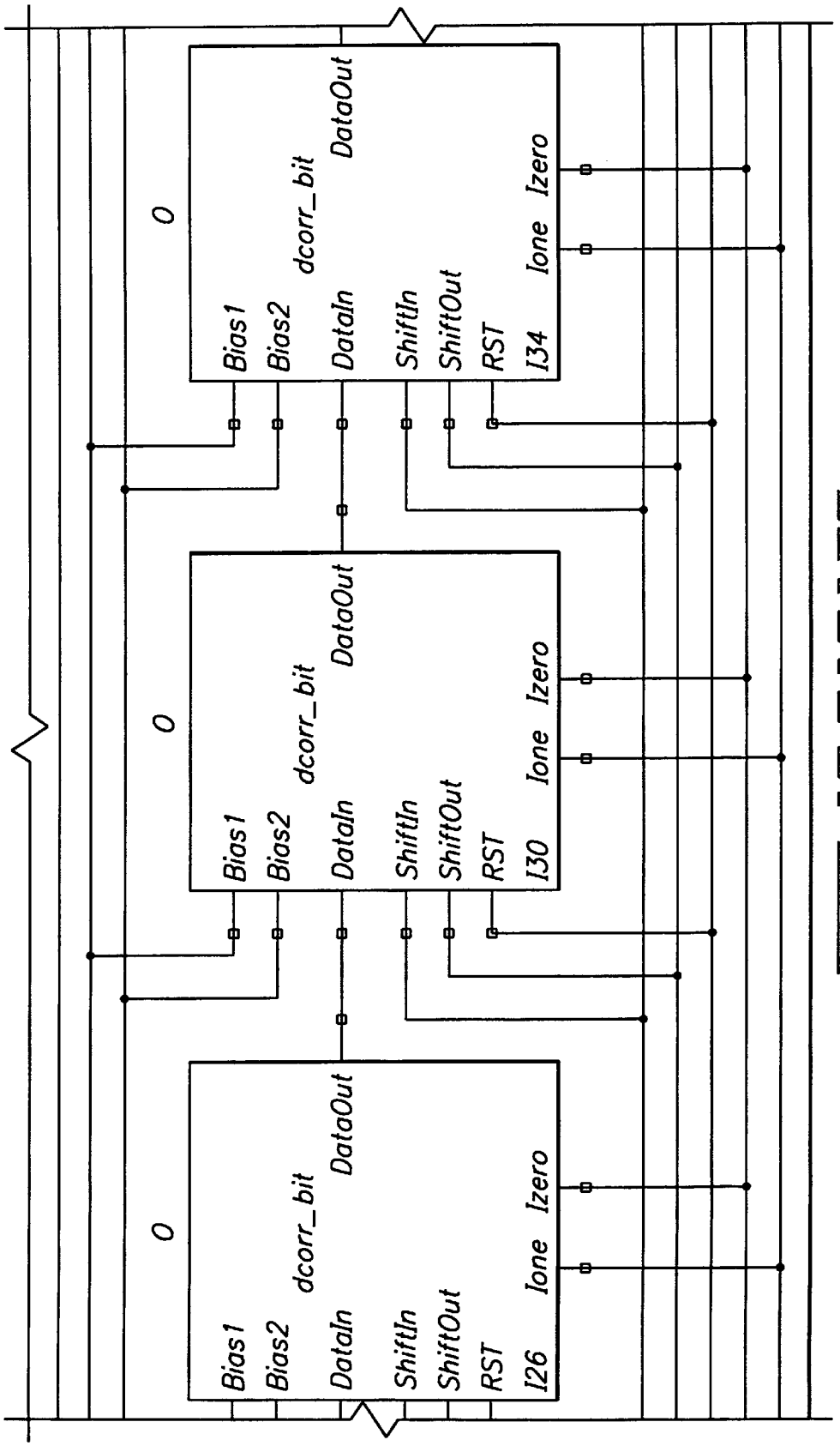


FIG. 1100.0011.1BIC

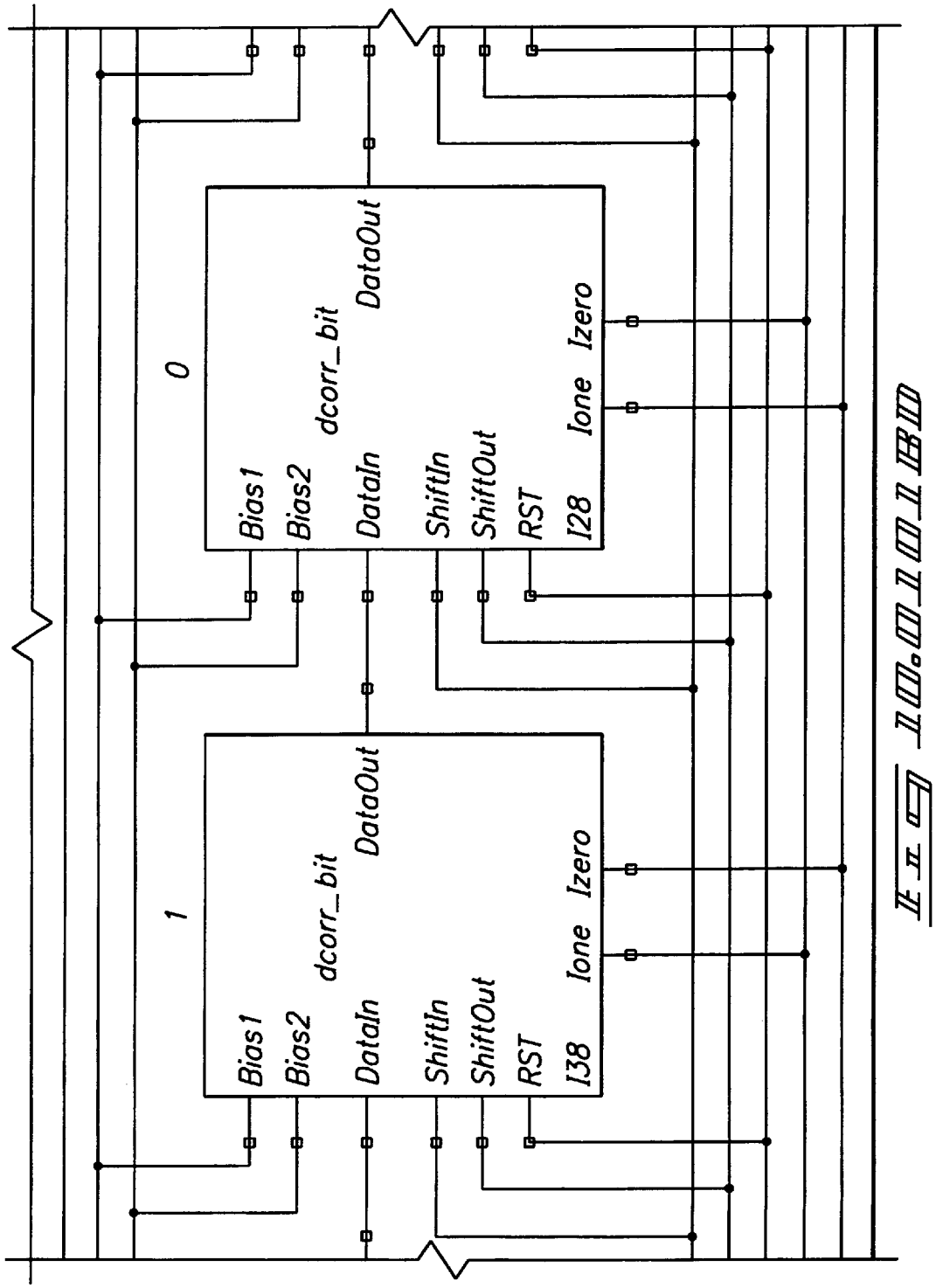


Fig 11.00.0011 IBM

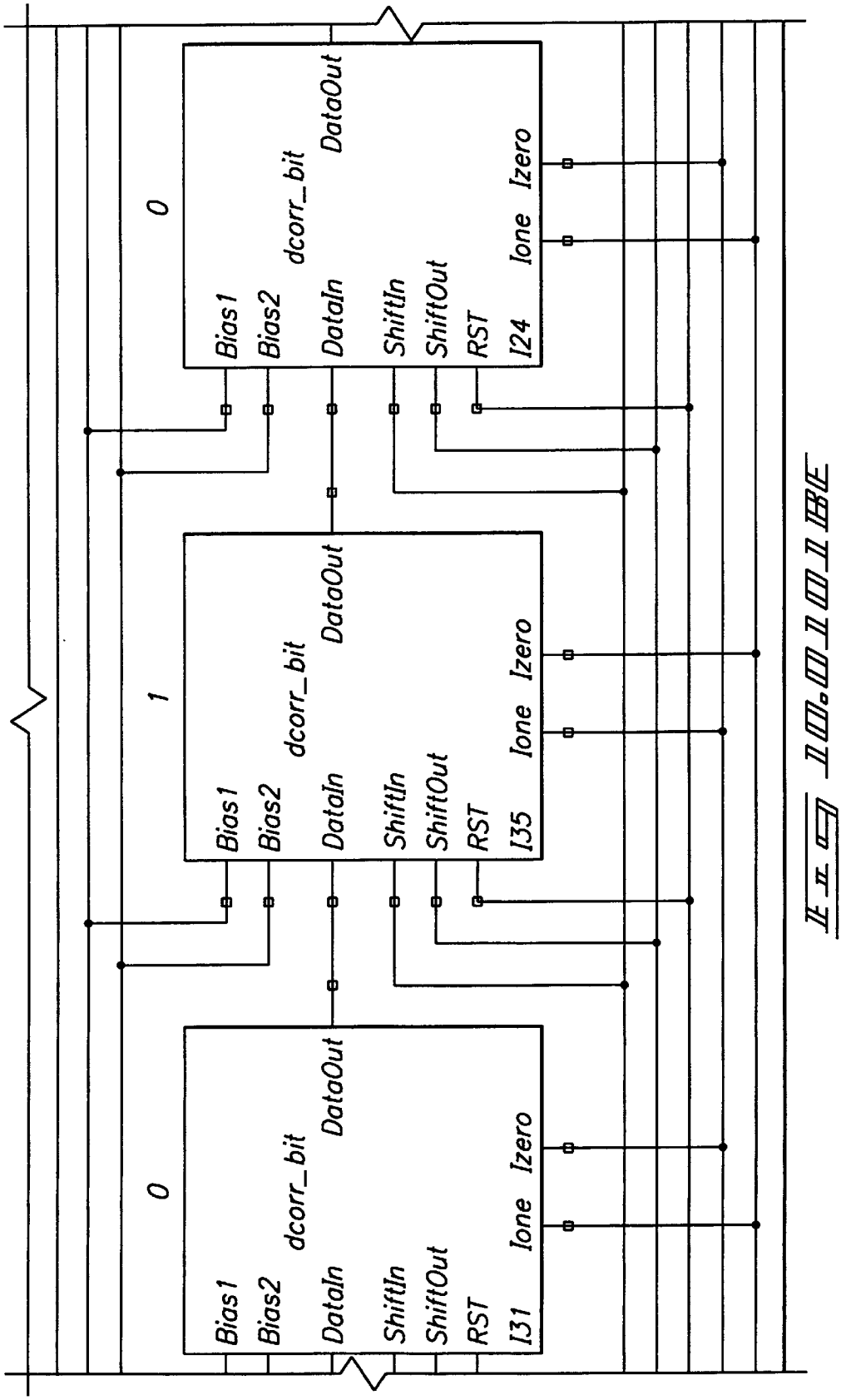
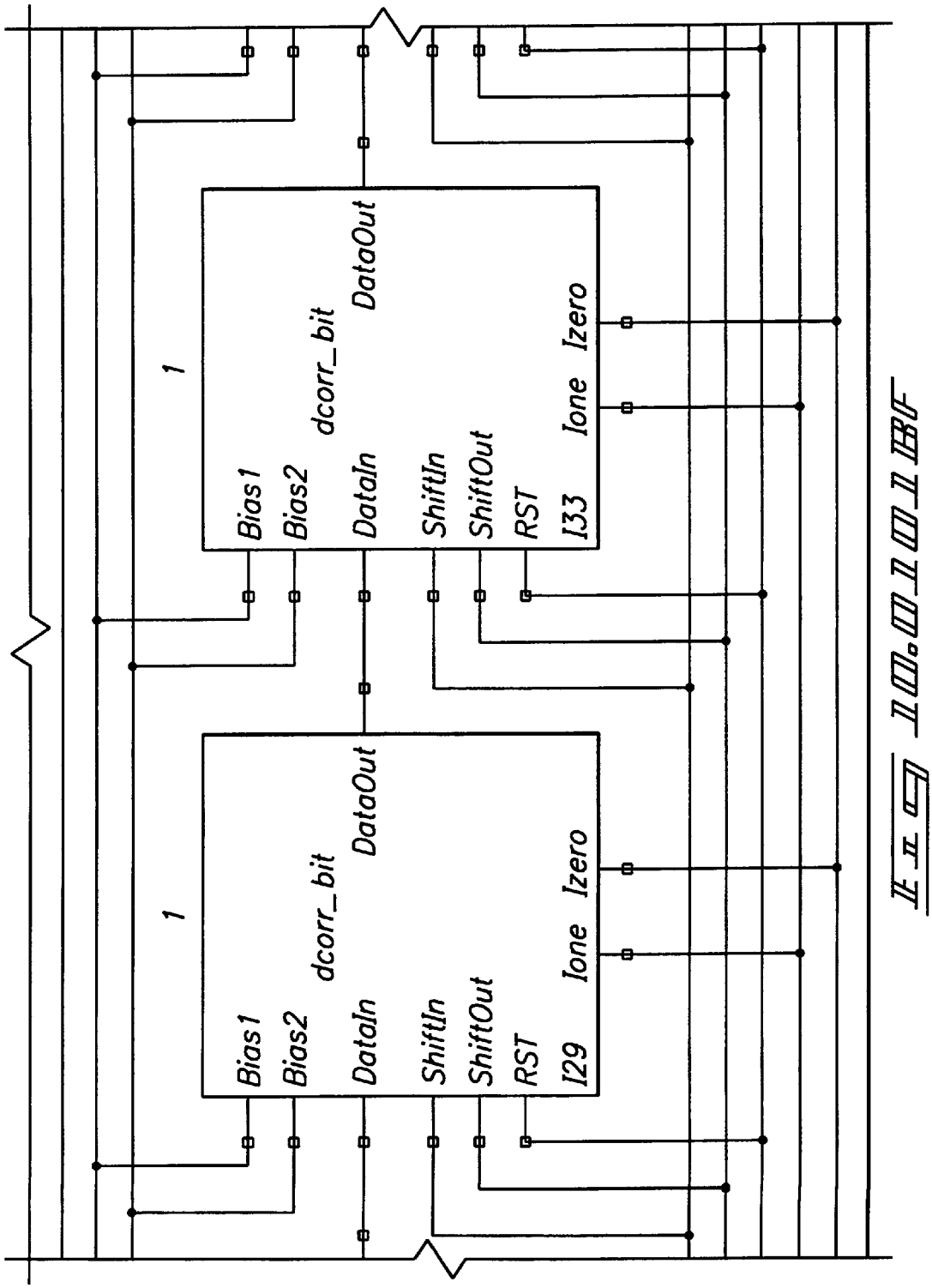


FIG 100,001,1BE


1
dcorr_bit
Bias1
Bias2
DataIn
ShiftIn
ShiftOut
RST
I33
Ione
Izero
DataOut
1
dcorr_bit
Bias1
Bias2
DataIn
ShiftIn
ShiftOut
RST
I29
Ione
Izero
DataOut

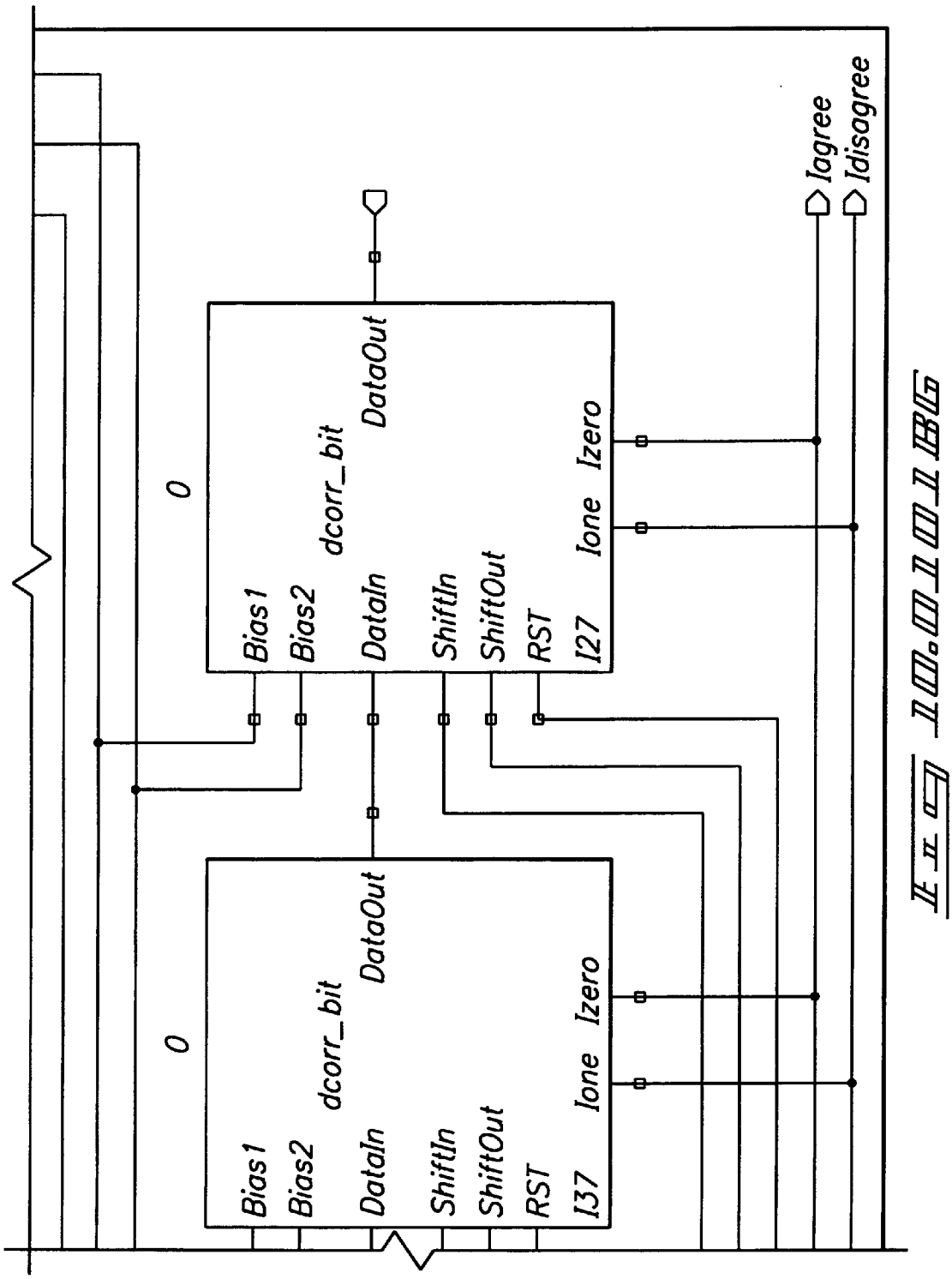


FIG 100.00110185

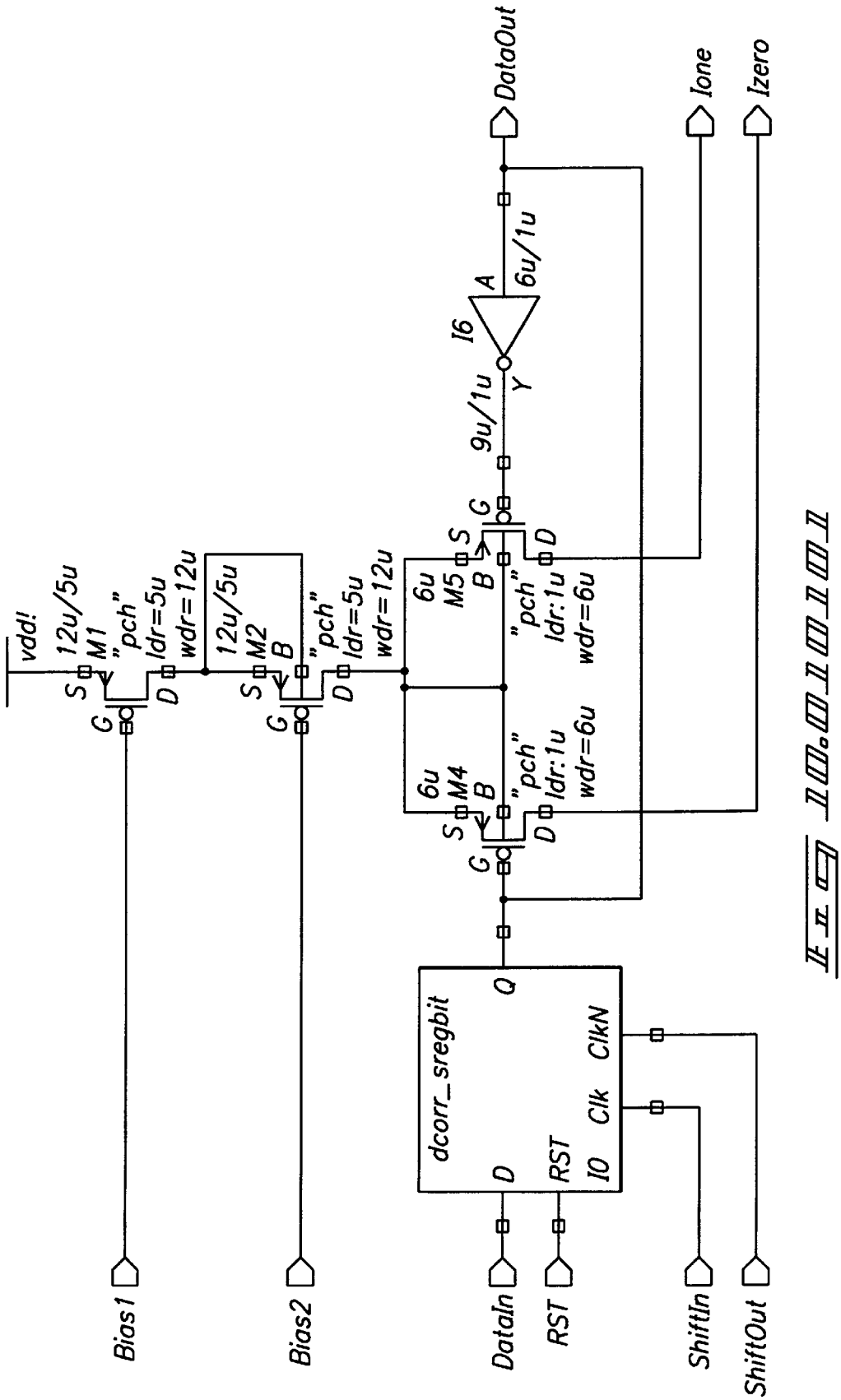

vdd!
12u/5u
M1
"pch"
ldr=5u
wdr=12u
12u/5u
M2
"pch"
ldr=5u
wdr=12u
6u
M5
"pch"
ldr:1u
wdr=6u
6u
M4
"pch"
ldr:1u
wdr=6u
9u/1u
I6
6u/1u
DataOut
Ione
Izero
dcorr_sregbit
D
RST
I0
Clk
ClkN
Q
Bias1
Bias2
DataIn
RST
ShiftIn
ShiftOut

FIG 11

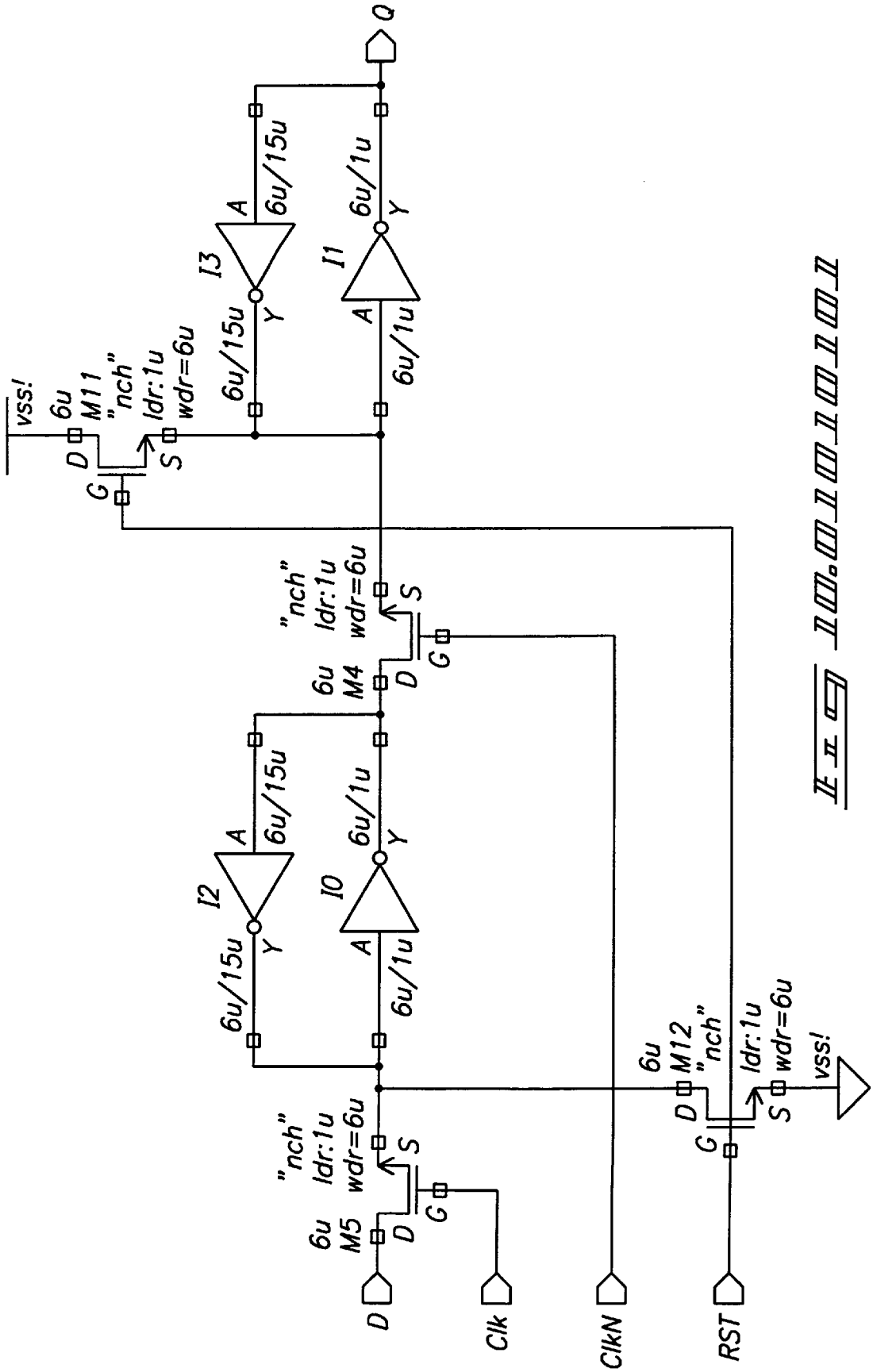


FIG 100.00110011001100

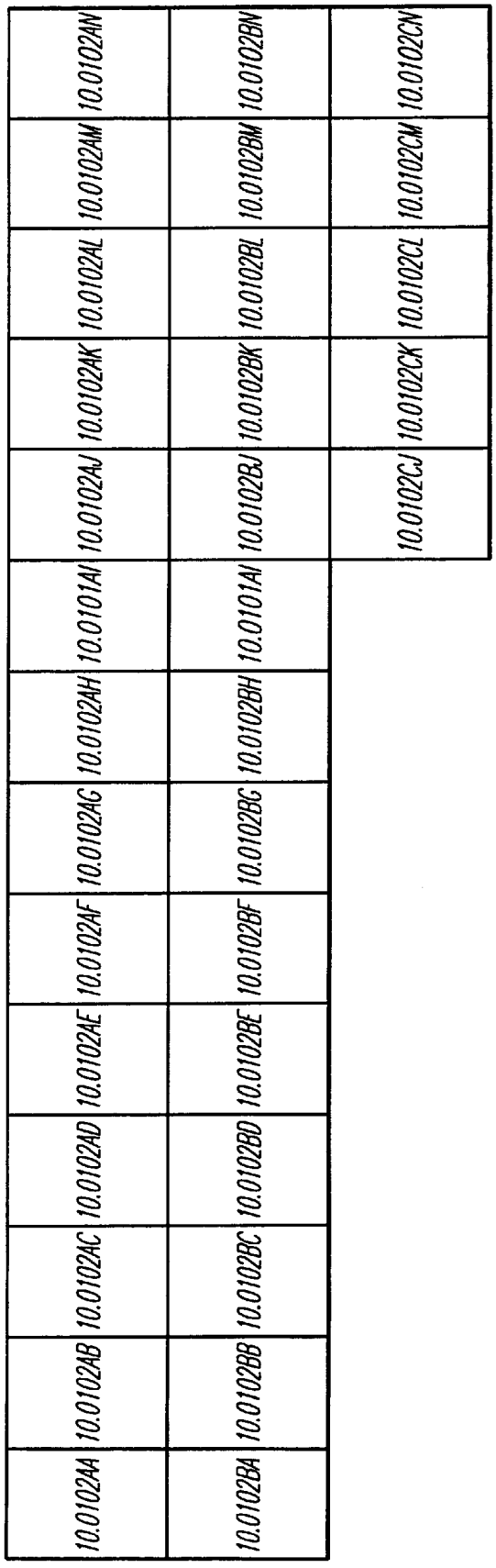

10.0102AA
10.0102AB
10.0102AC
10.0102AD
10.0102AE
10.0102AF
10.0102AG
10.0102AH
10.0101AI
10.0102AJ
10.0102AK
10.0102AL
10.0102AM
10.0102AN
10.0102BA
10.0102BB
10.0102BC
10.0102BD
10.0102BE
10.0102BF
10.0102BG
10.0102BH
10.0101AI
10.0102BJ
10.0102BK
10.0102BL
10.0102BM
10.0102BN
10.0102CJ
10.0102CK
10.0102CL
10.0102CM
10.0102CN

FIG. 10.0102

FIG 100.00112AA

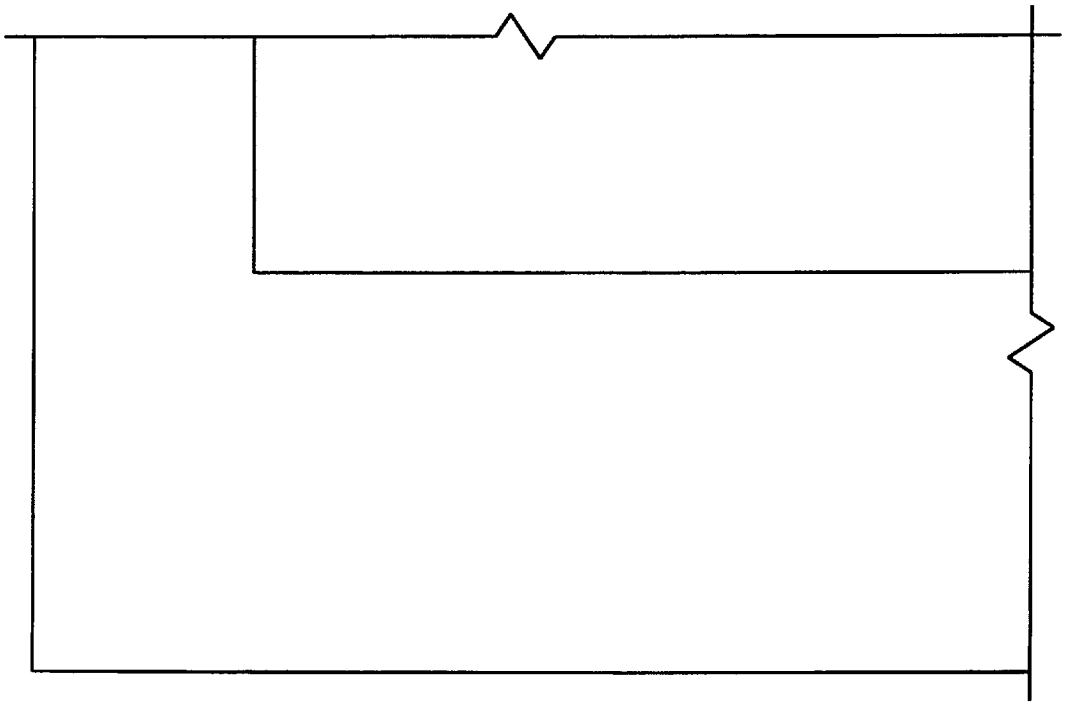
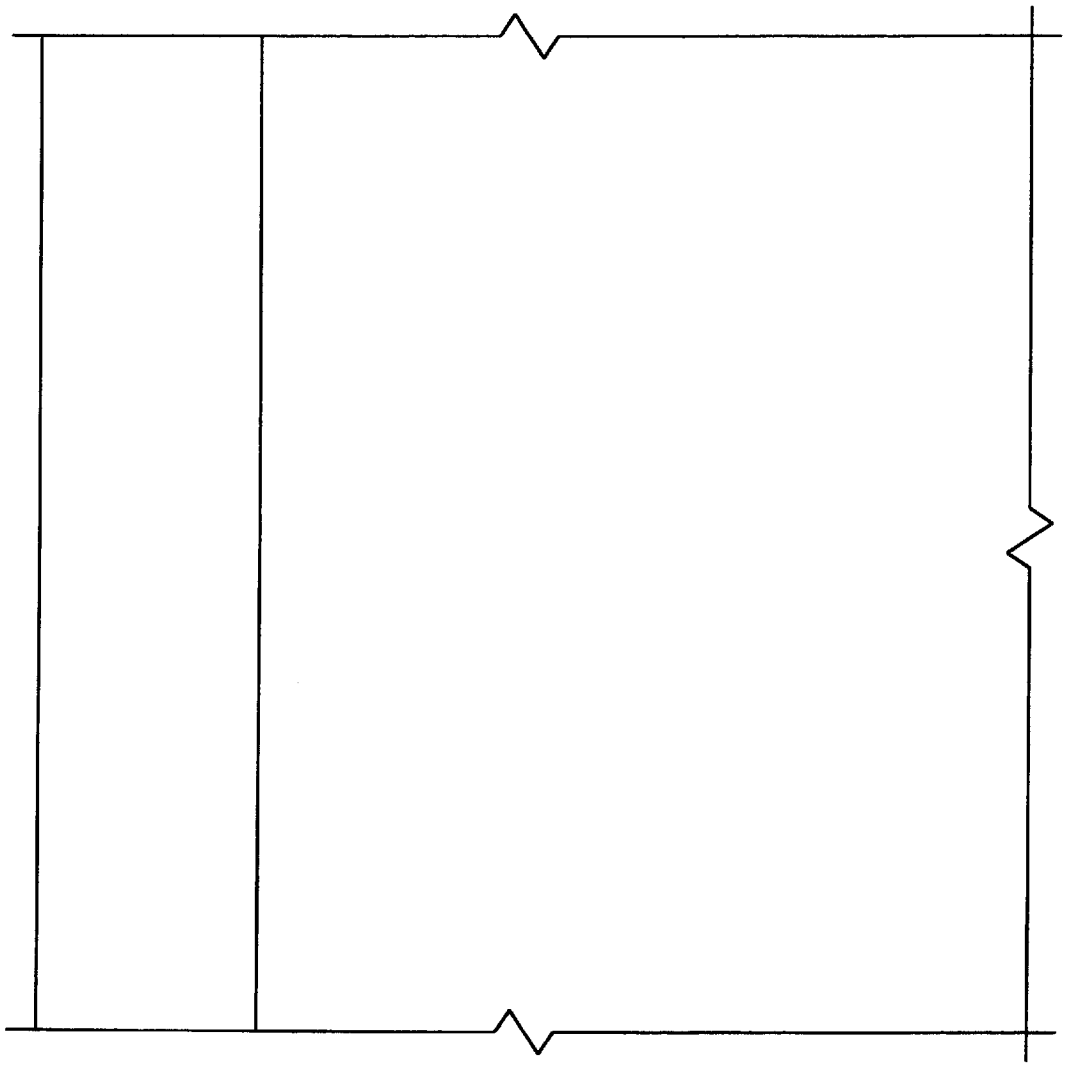


FIG 10,011,028



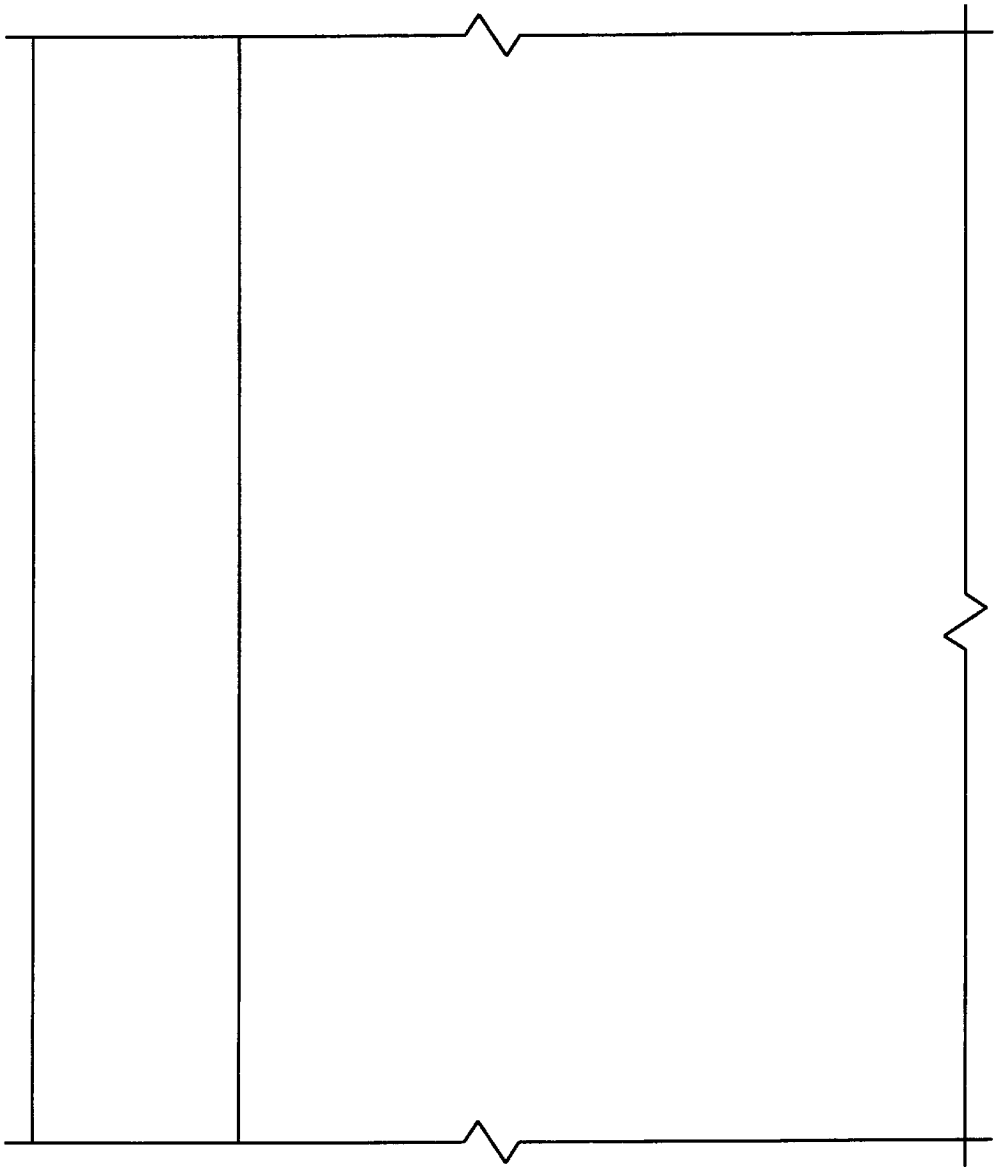


FIG 10.01ZAL

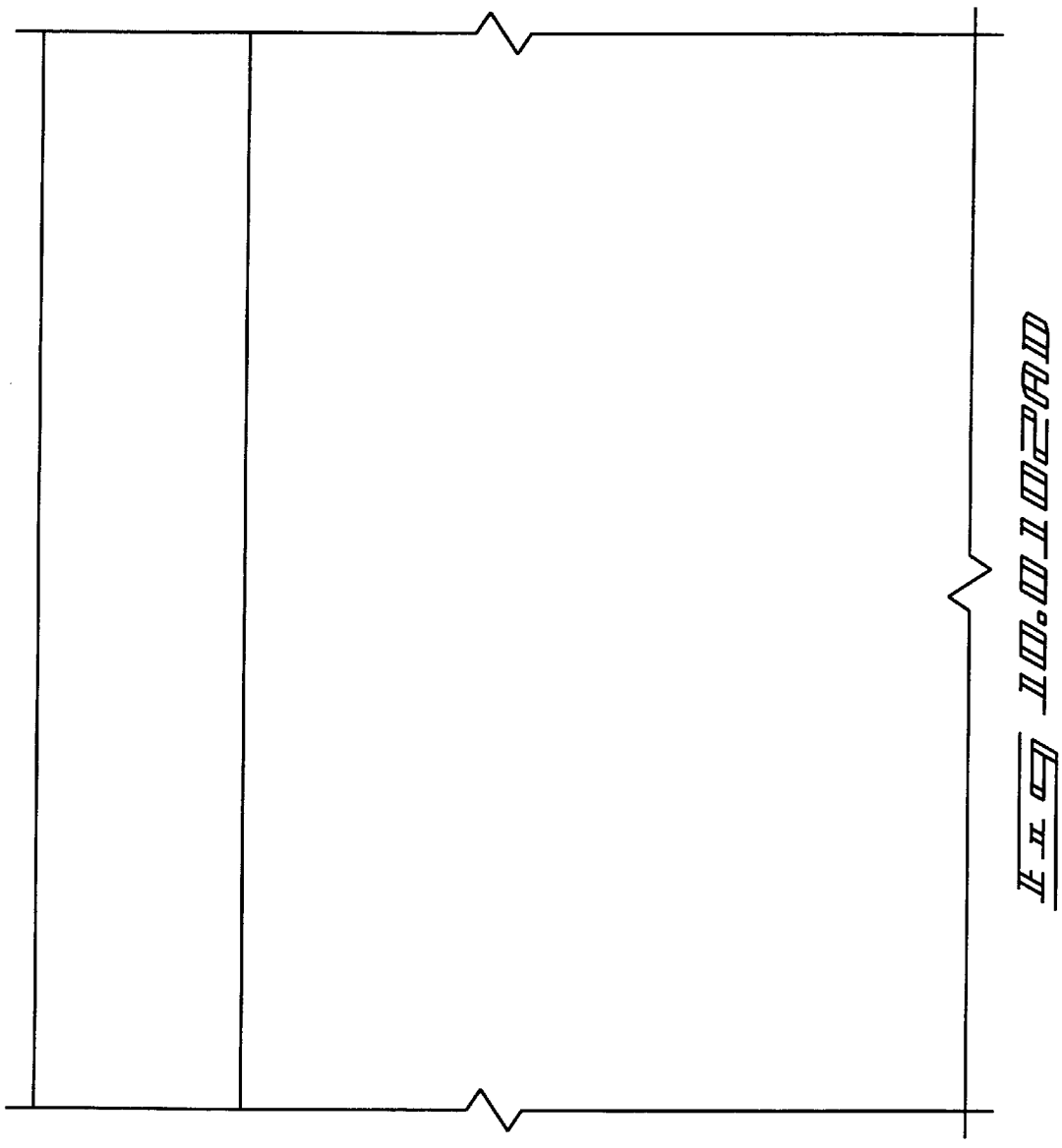
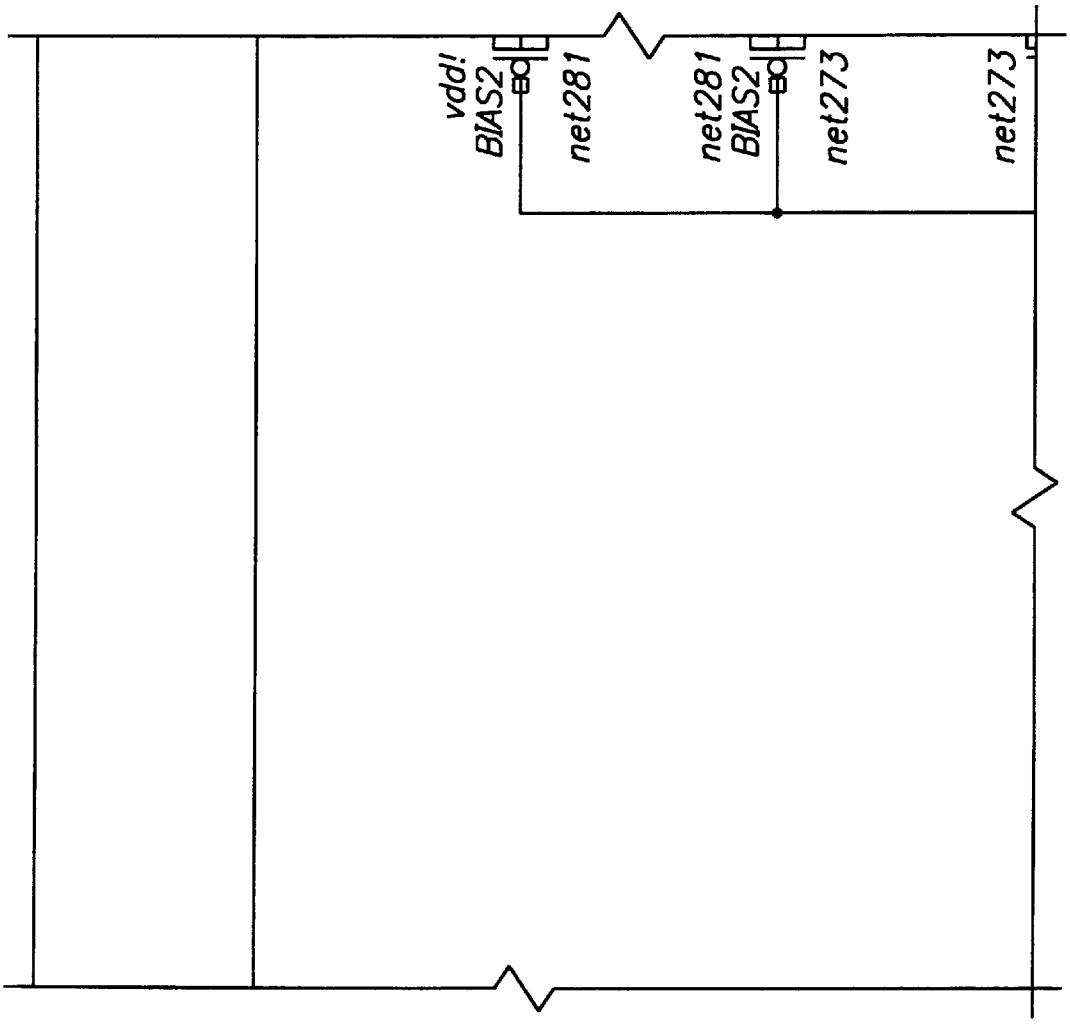


FIG 100,110,240

FIG 100.0110ZAE



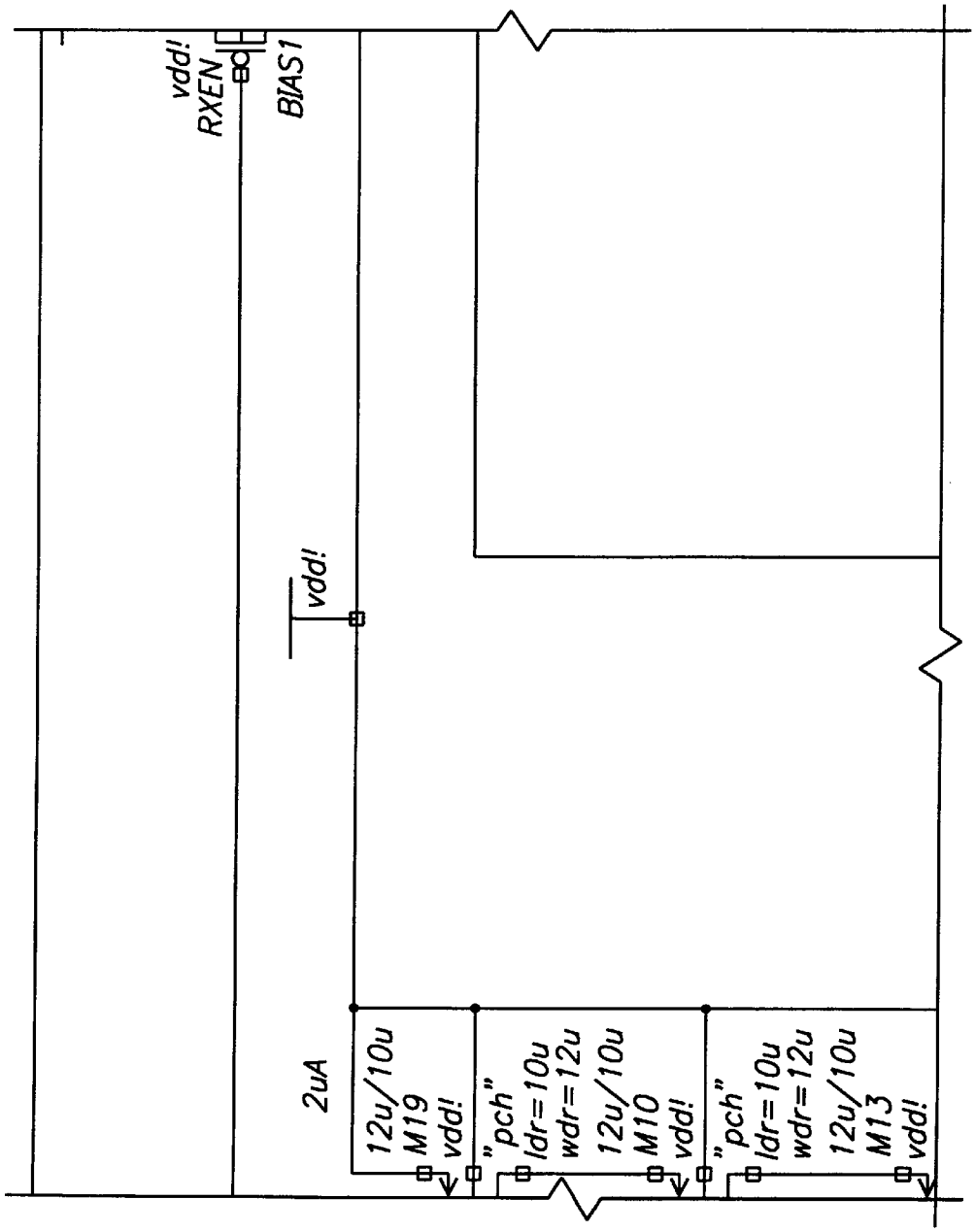


FIG 100,011,02AF

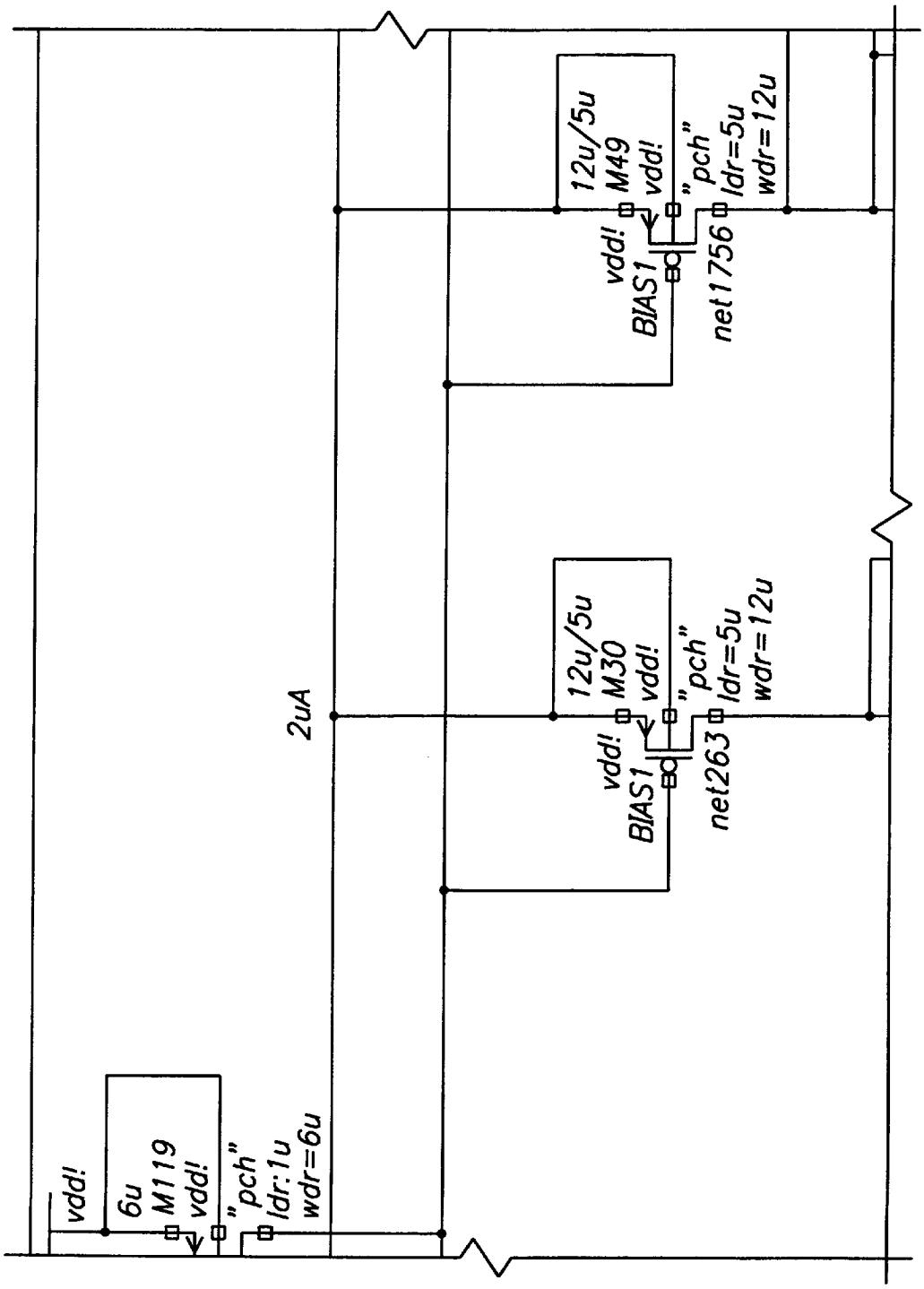


FIG 100125AS

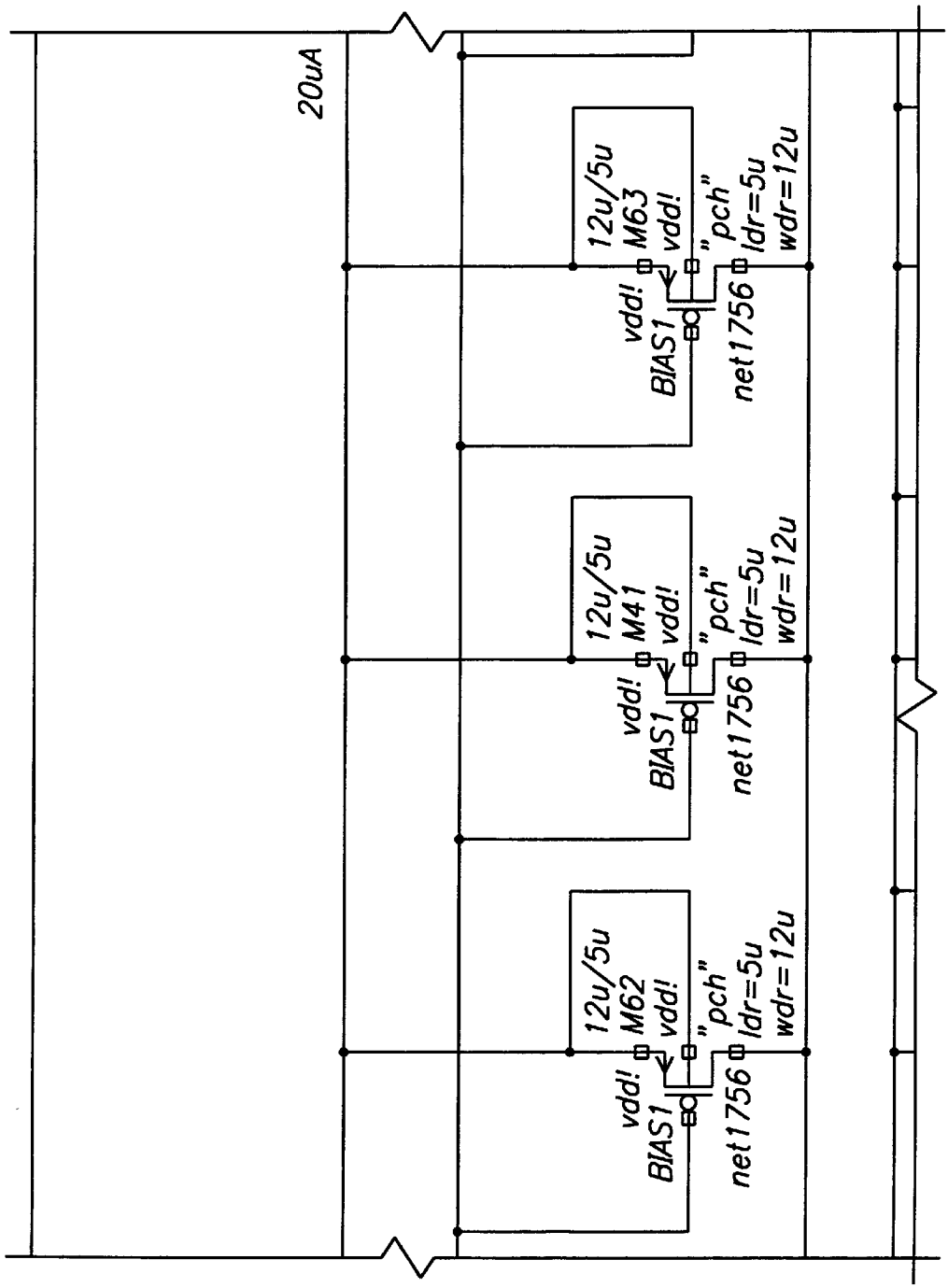

20uA
12u/5u
M63
vdd!
"pch"
ldr=5u
wdr=12u
vdd!
BIAS1
net1756
12u/5u
M41
vdd!
"pch"
ldr=5u
wdr=12u
vdd!
BIAS1
net1756
12u/5u
M62
vdd!
"pch"
ldr=5u
wdr=12u
vdd!
BIAS1
net1756

FIG 100,001

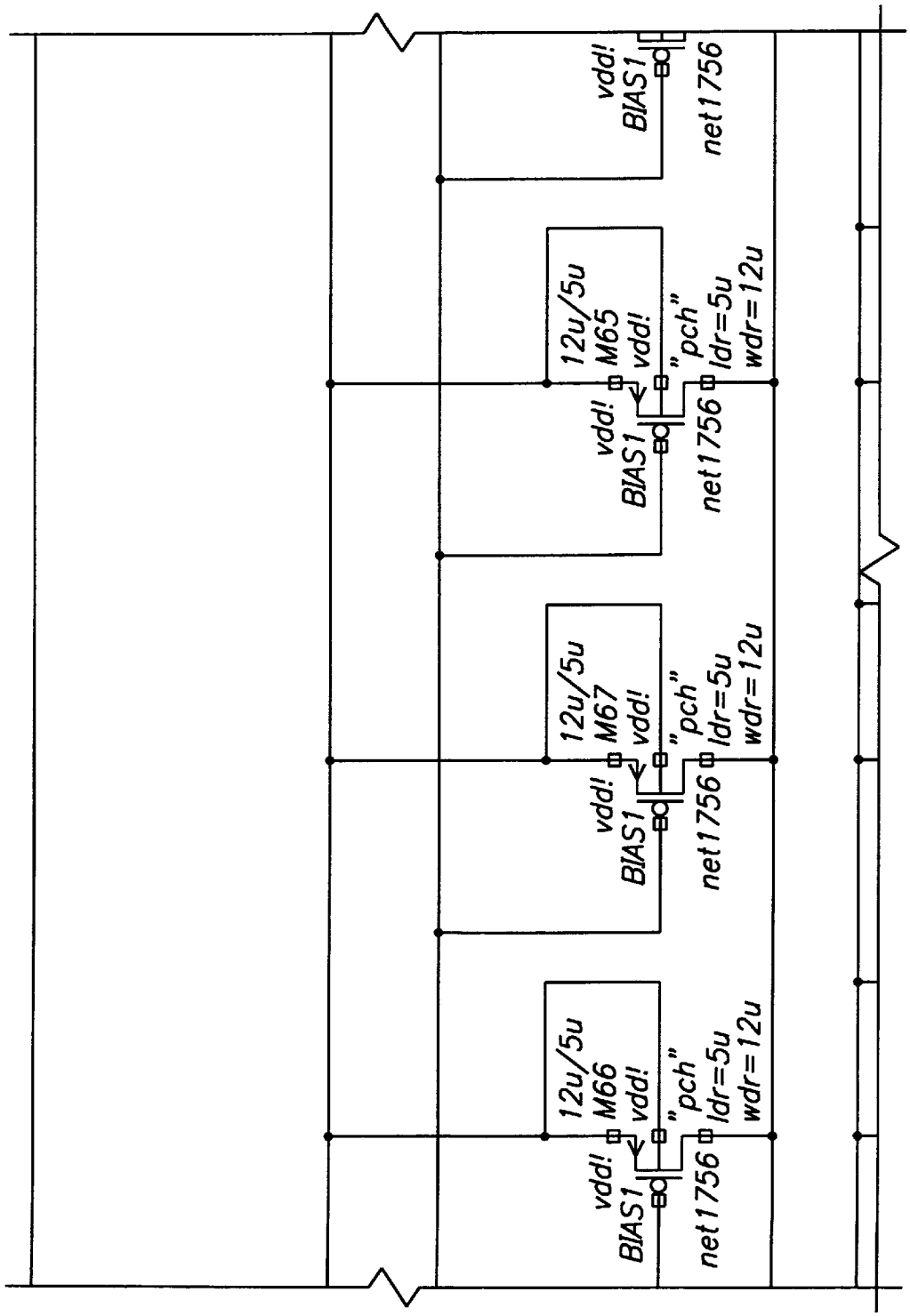


FIG 100,011

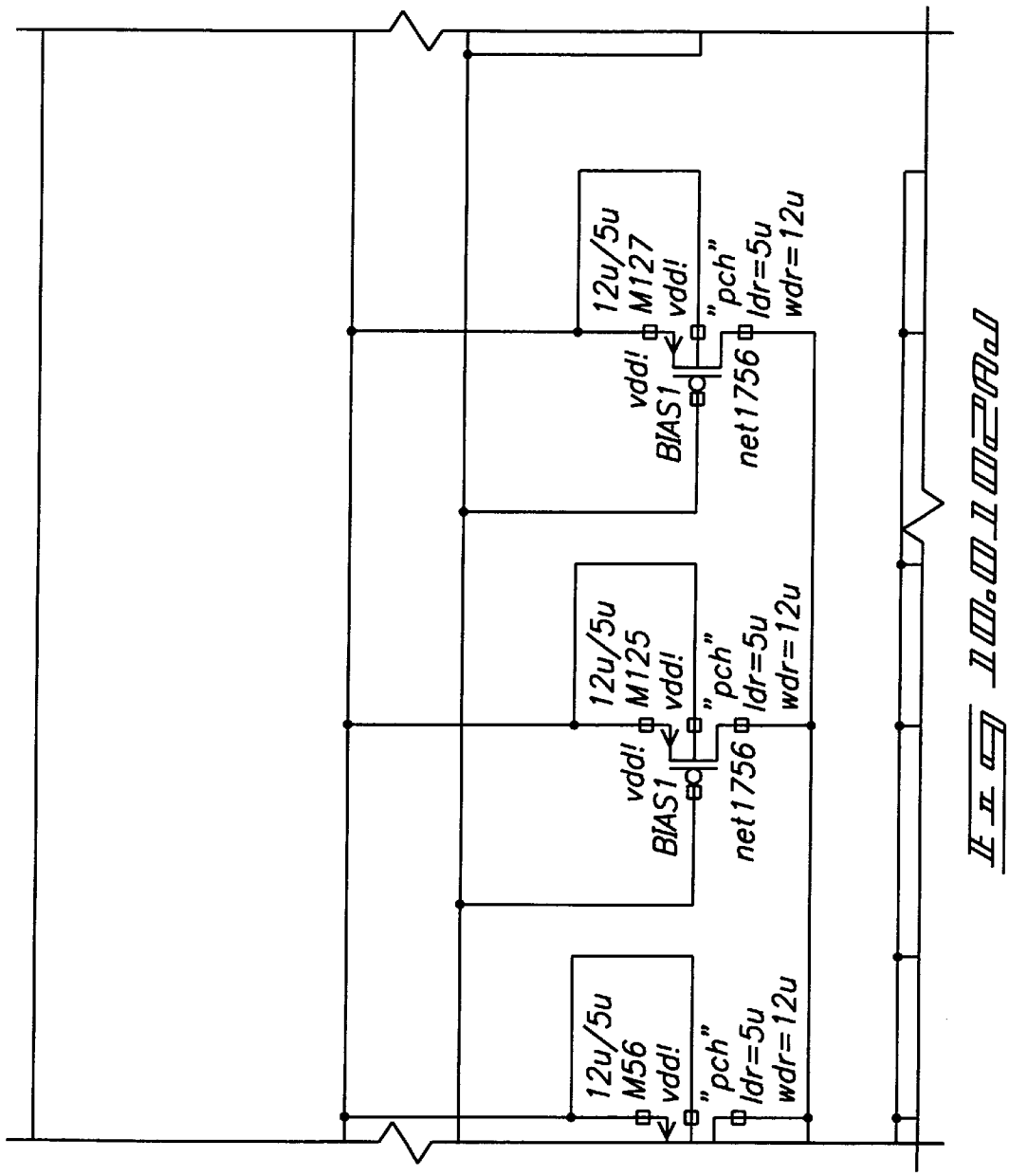


FIG 1100.0011.0024

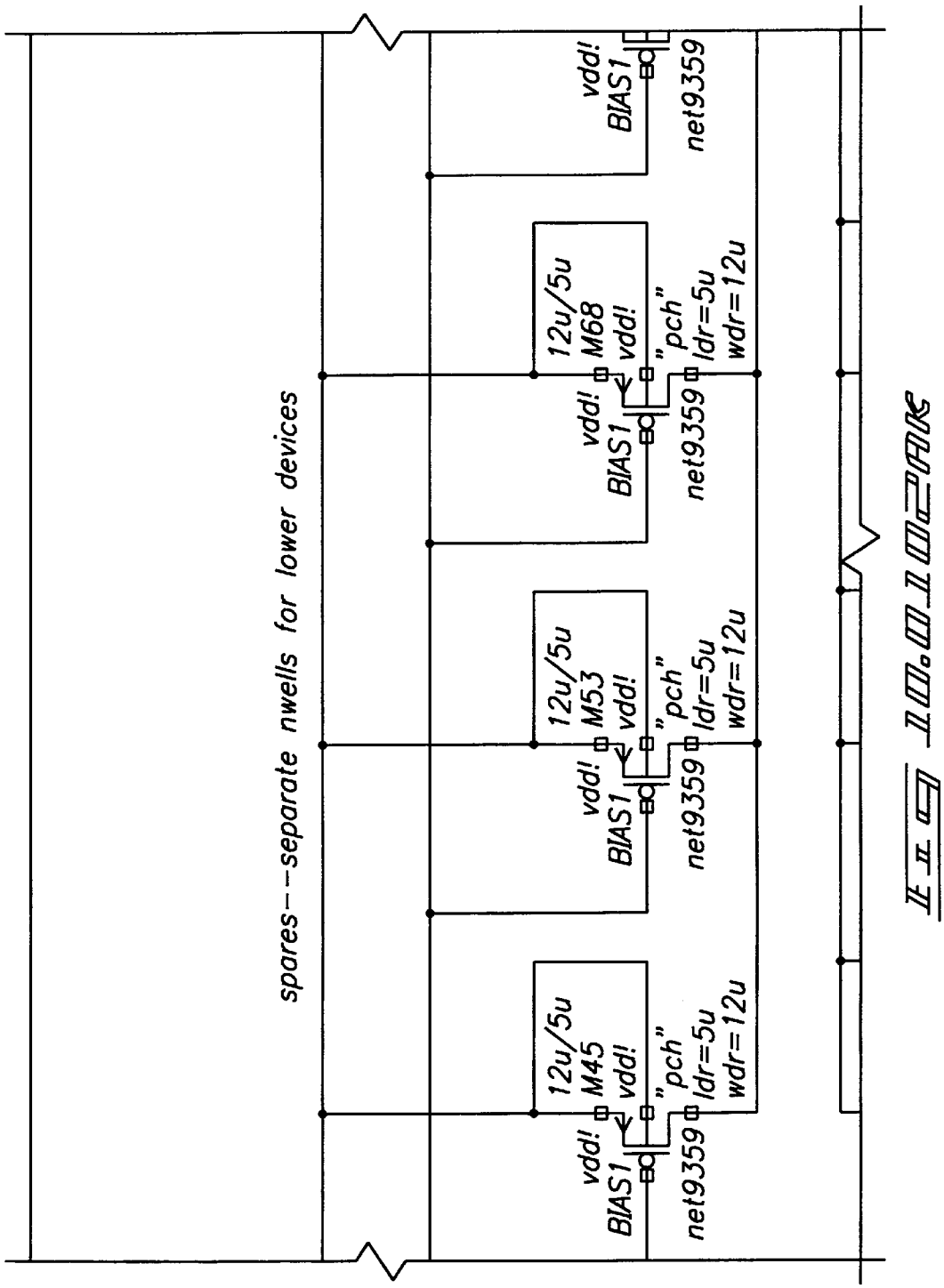


FIG 100.00.00ARR

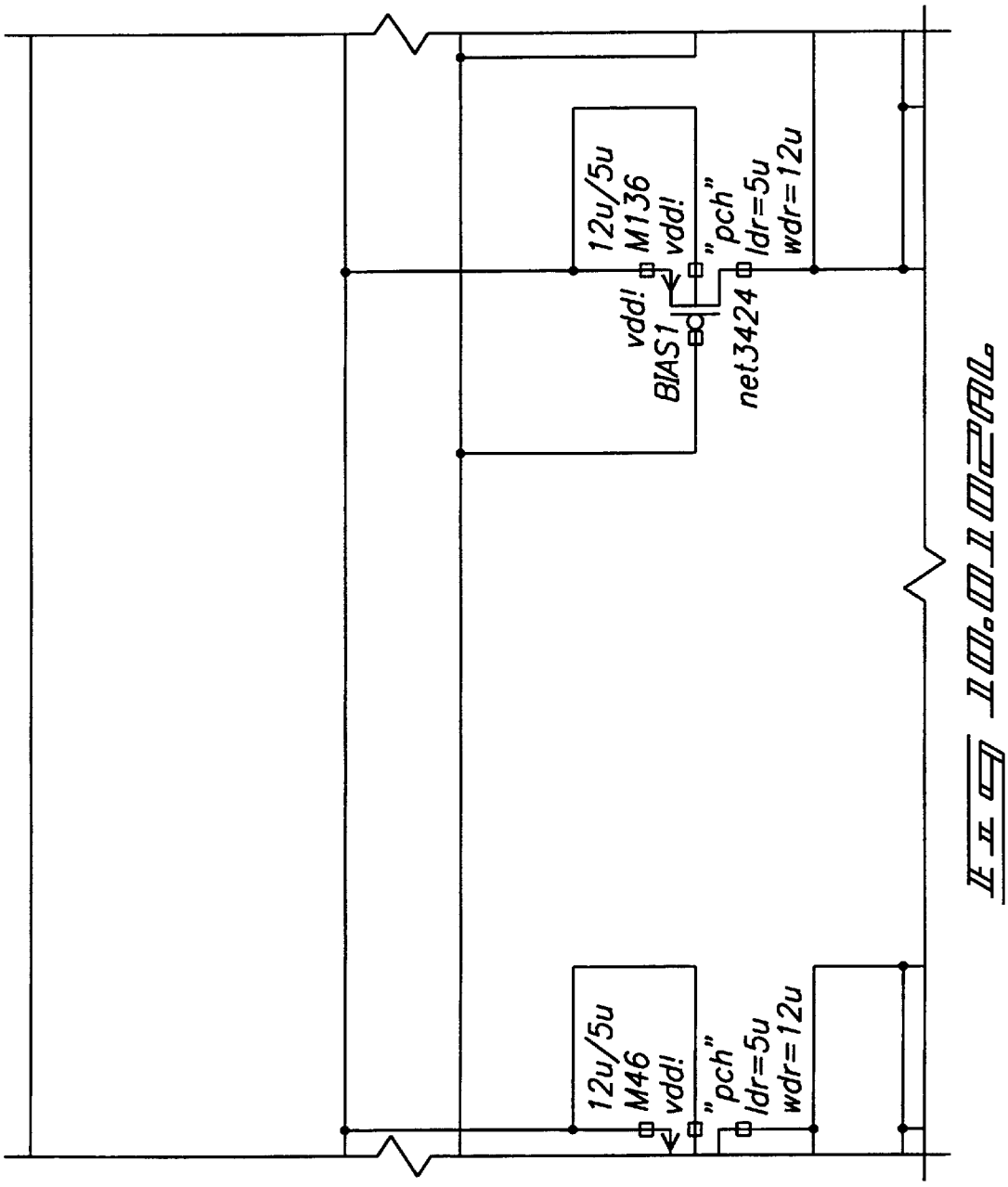


FIG 100,1002AL

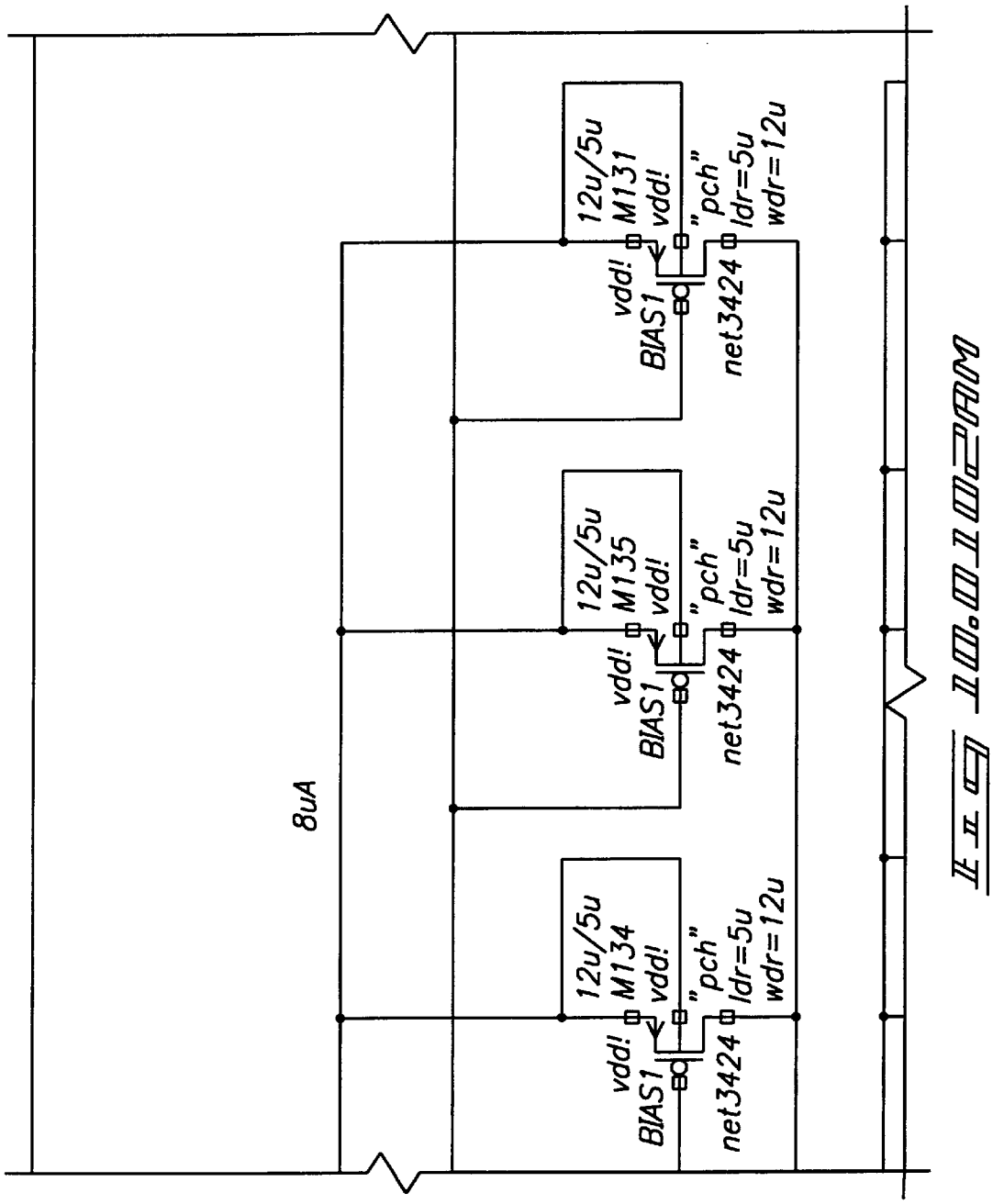

8uA
12u/5u
M131
vdd!
"pch"
ldr=5u
wdr=12u
vdd!
BIAS1
net3424
12u/5u
M135
vdd!
"pch"
ldr=5u
wdr=12u
vdd!
BIAS1
net3424
12u/5u
M134
vdd!
"pch"
ldr=5u
wdr=12u
vdd!
BIAS1
net3424

FIG 10,001

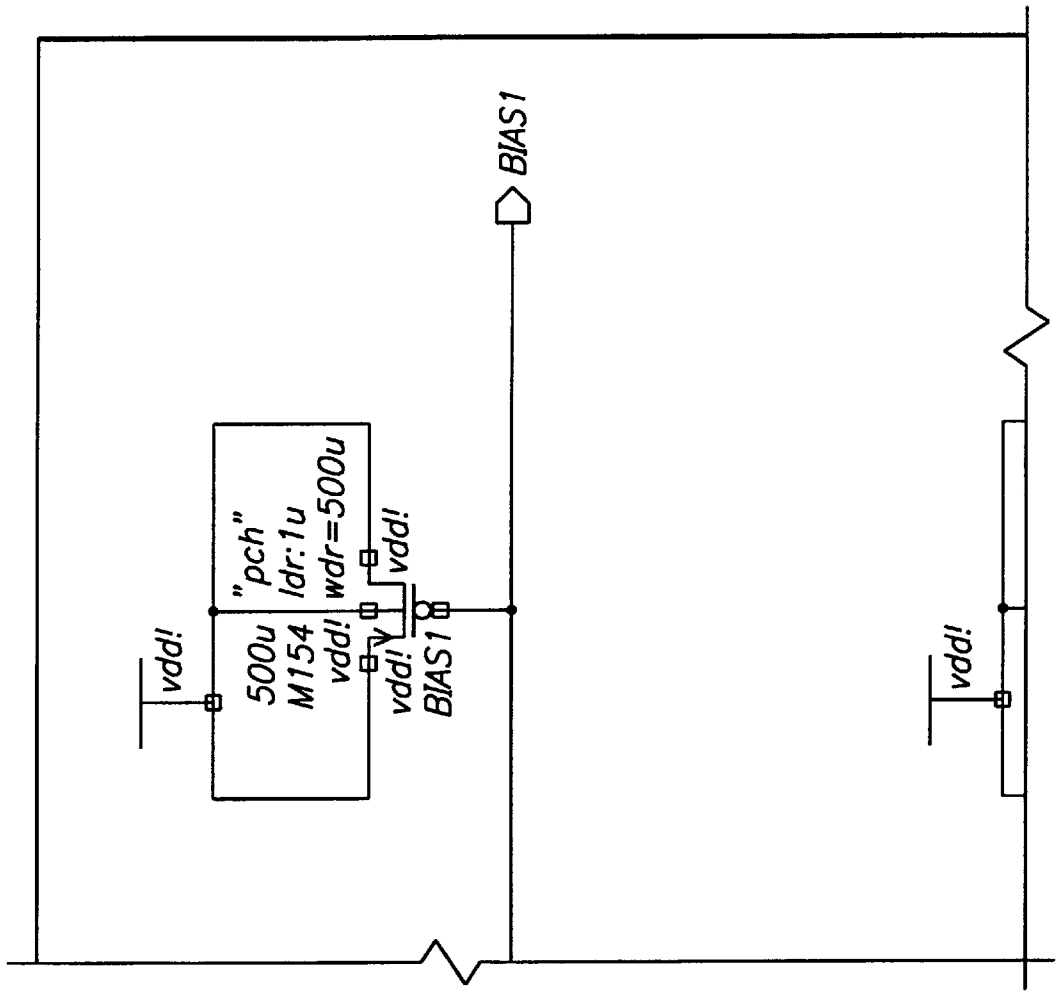


FIG 69

FIG 10.0128A

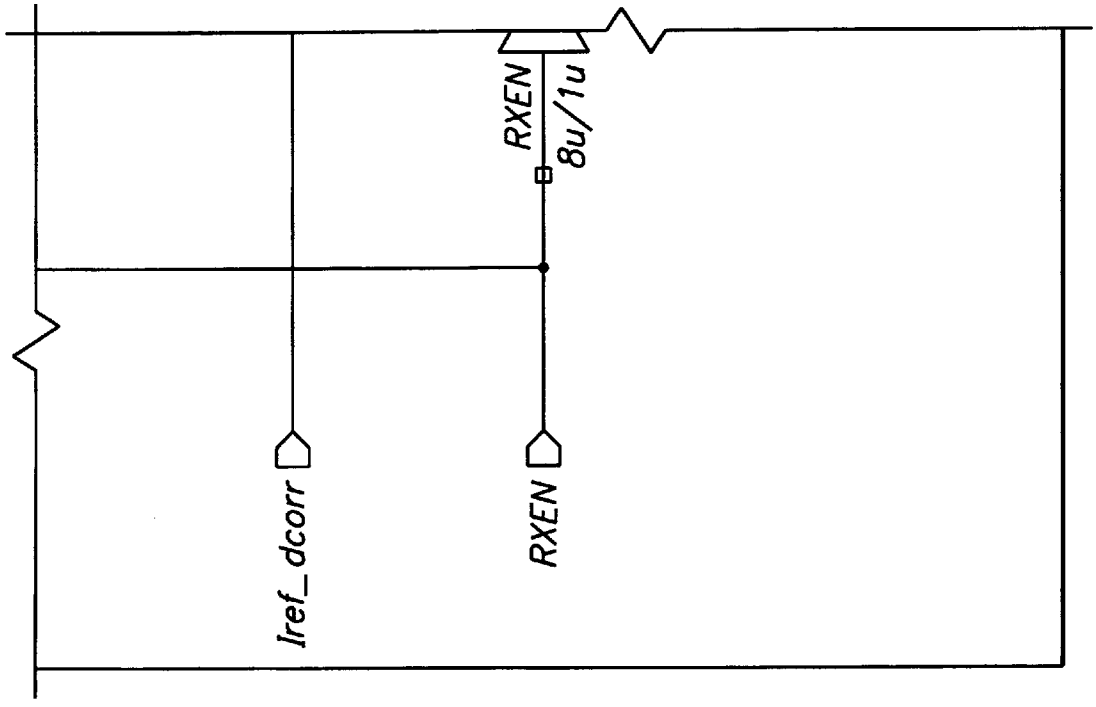
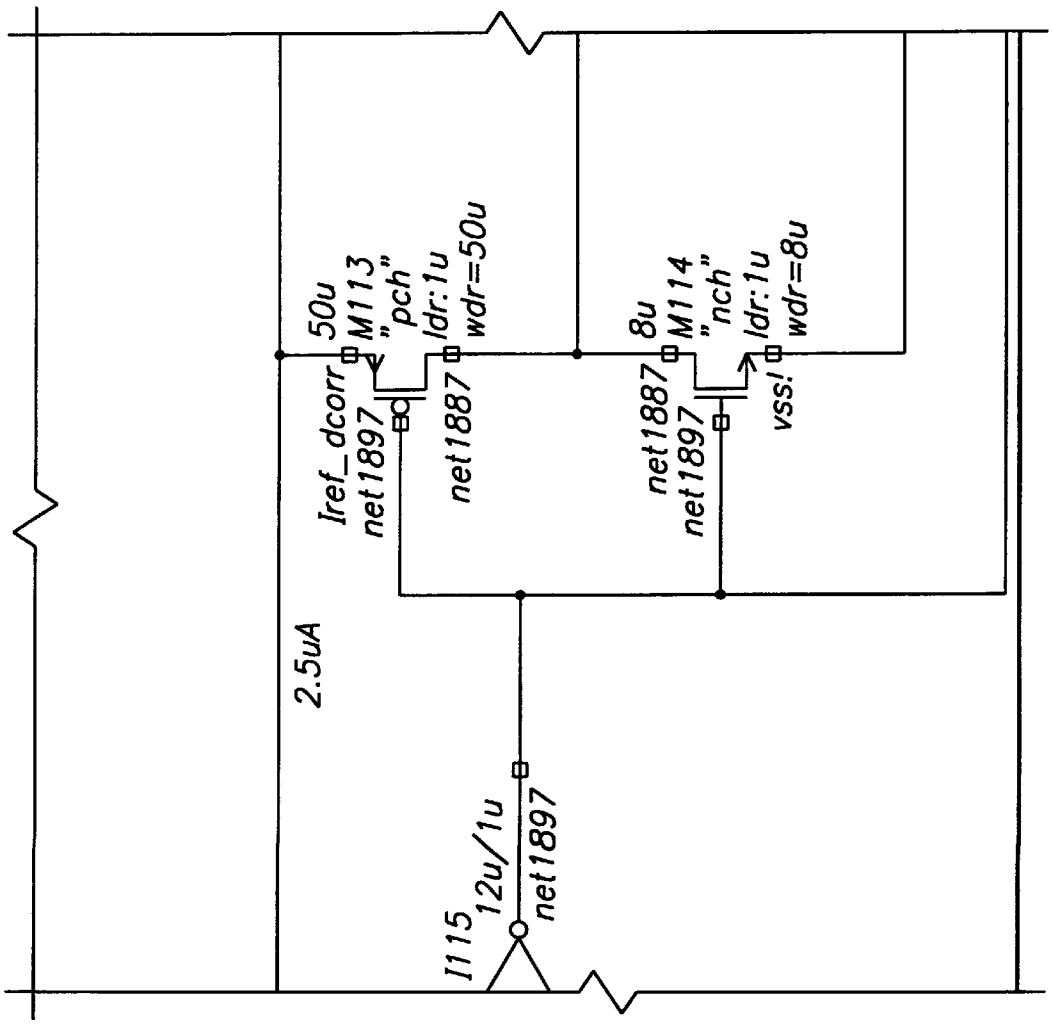


FIG 100,011,028



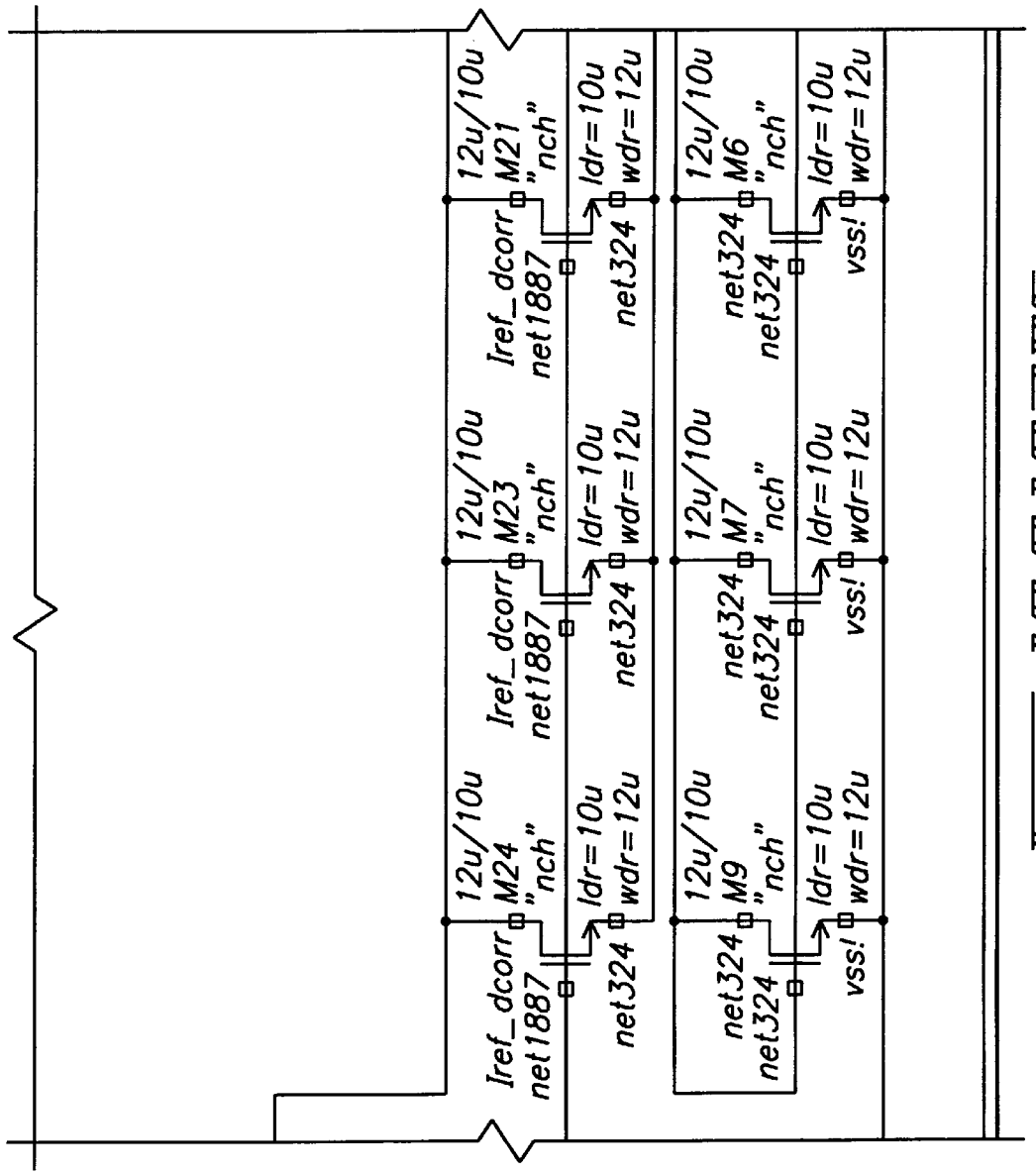


FIG 1100.0112

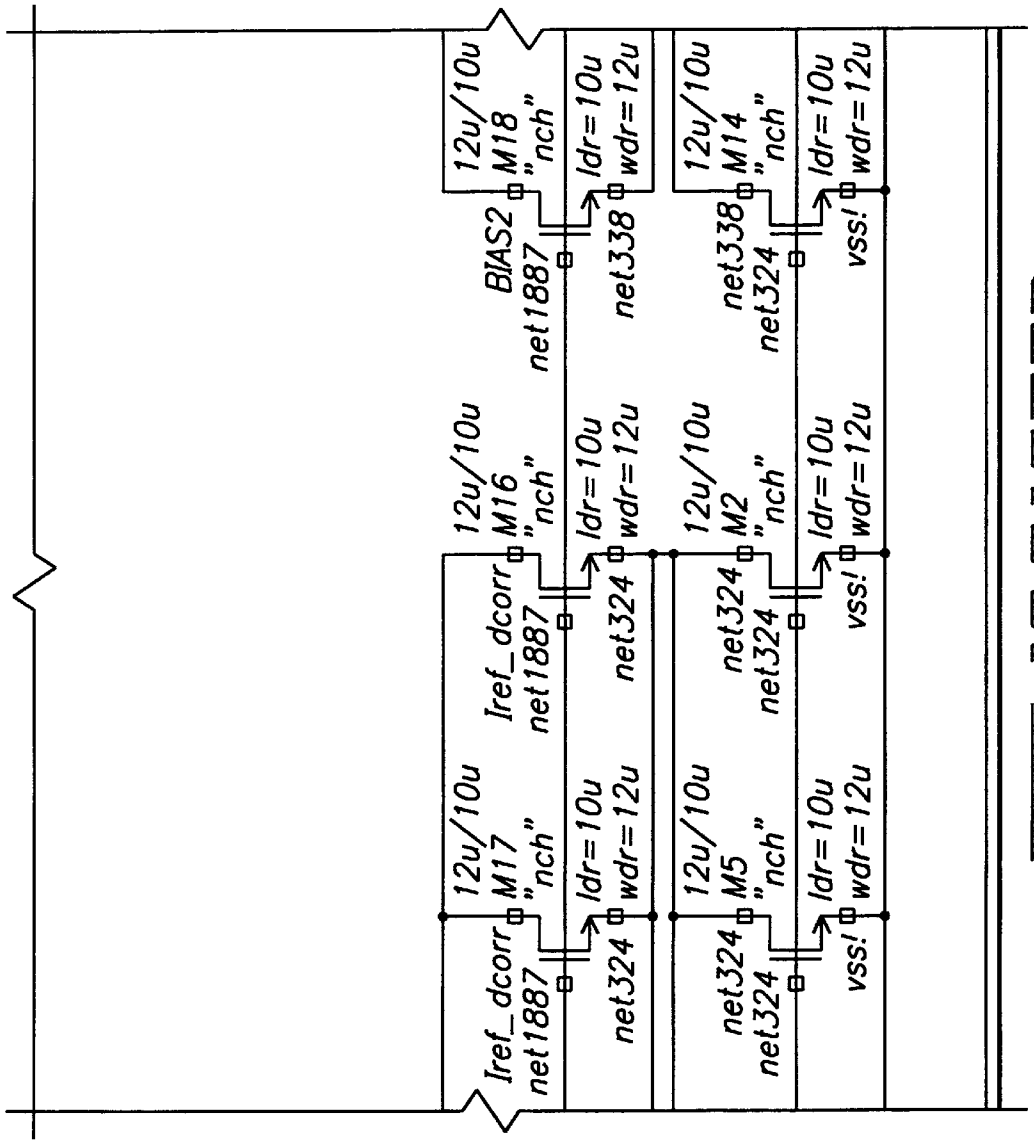
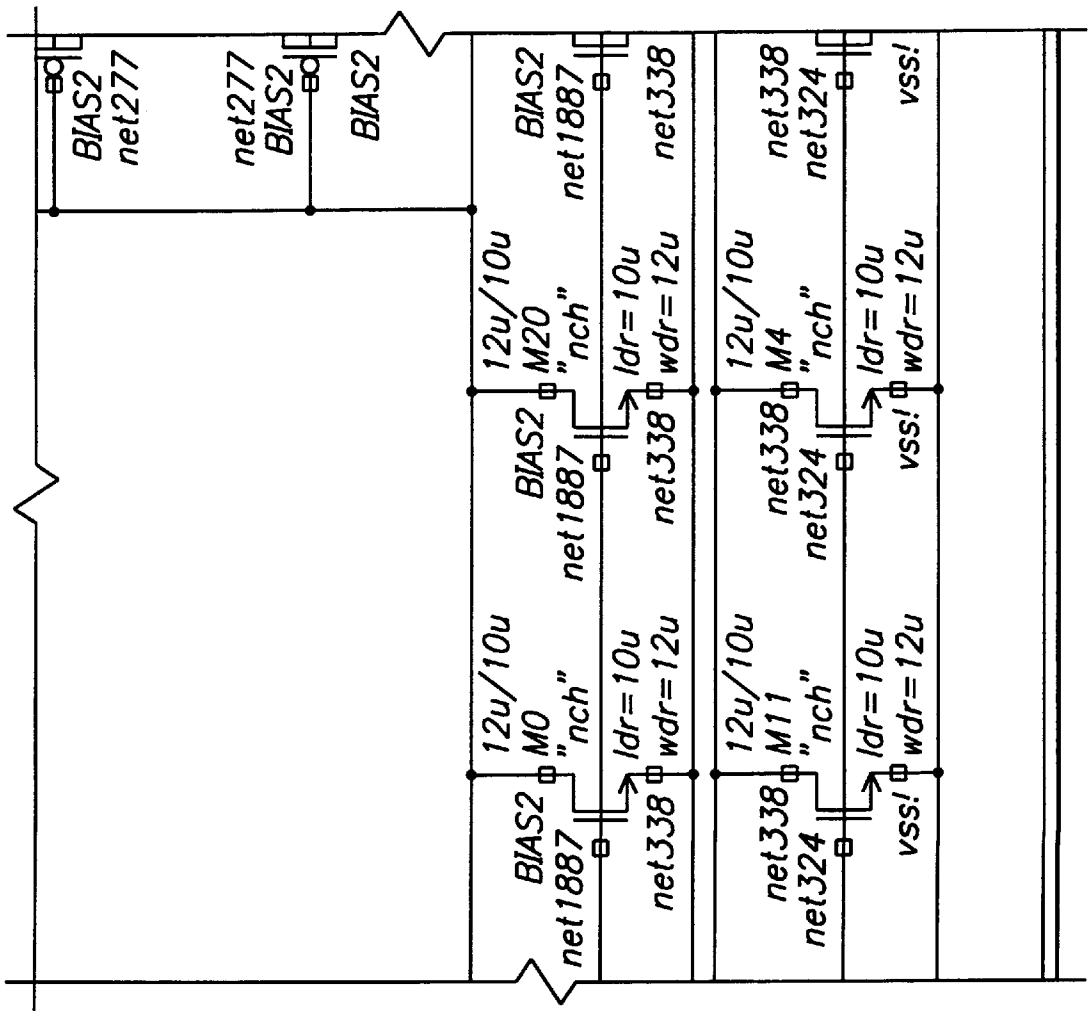

12u/10u
M18
"nch"
ldr=10u
wdr=12u
BIAS2
net1887
net338
12u/10u
M14
"nch"
ldr=10u
wdr=12u
net338
net324
vss!
12u/10u
M16
"nch"
ldr=10u
wdr=12u
Iref_dcorr
net1887
net324
12u/10u
M2
"nch"
ldr=10u
wdr=12u
net324
net324
vss!
12u/10u
M17
"nch"
ldr=10u
wdr=12u
Iref_dcorr
net1887
net324
12u/10u
M5
"nch"
ldr=10u
wdr=12u
net324
net324
vss!

FIG 1003

FIG 1100.001


BIAS2
net277
net277
BIAS2
BIAS2
12u/10u
M0
"nch"
ldr=10u
wdr=12u
BIAS2
net1887
net338
BIAS2
net1887
12u/10u
M20
"nch"
ldr=10u
wdr=12u
net338
net324
12u/10u
M11
"nch"
ldr=10u
wdr=12u
vss!
net338
net324
12u/10u
M4
"nch"
ldr=10u
wdr=12u
vss!

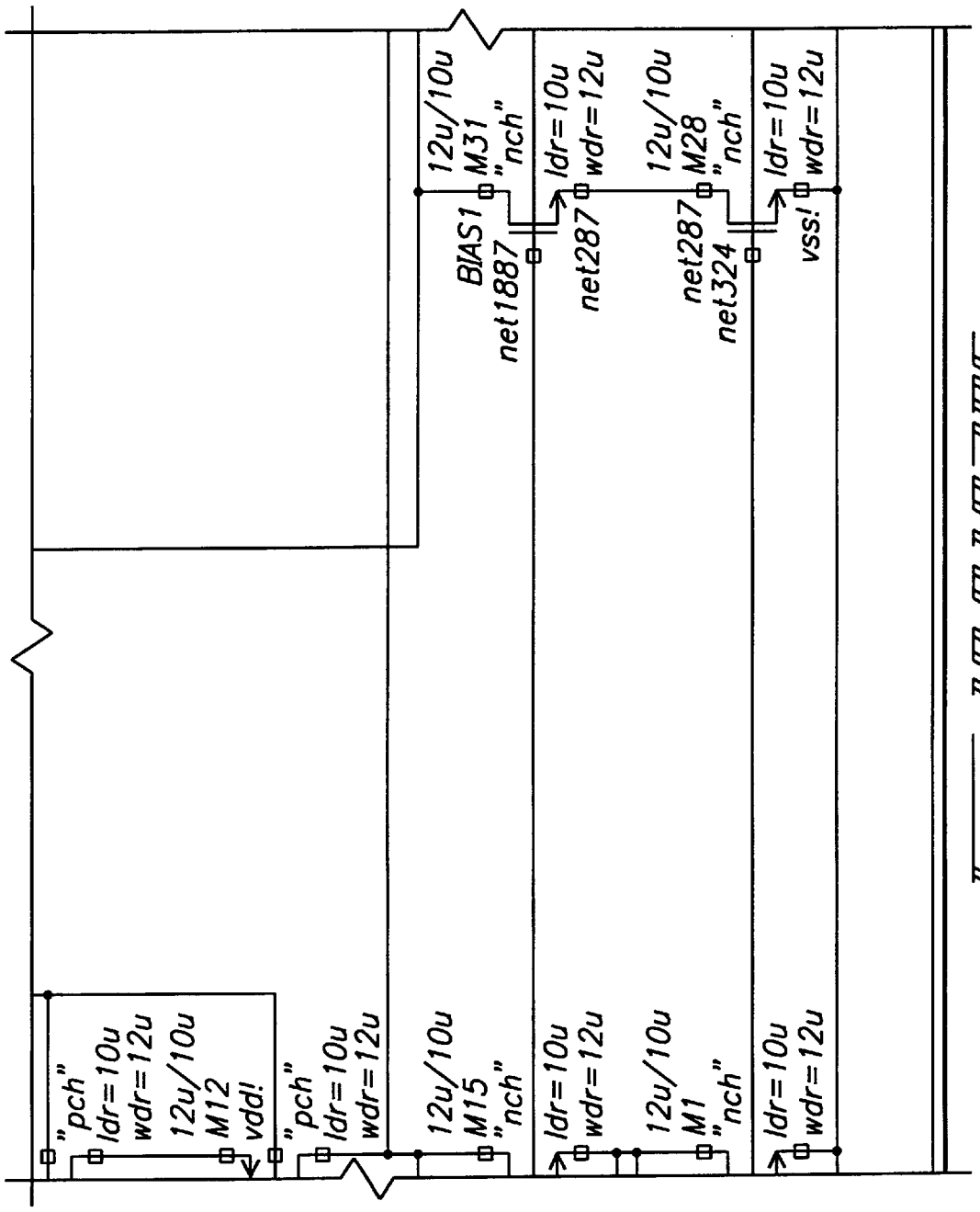

"pch"
ldr=10u
wdr=12u
12u/10u
M12
vdd!
"pch"
ldr=10u
wdr=12u
12u/10u
M15
"nch"
ldr=10u
wdr=12u
12u/10u
M1
"nch"
ldr=10u
wdr=12u
vss!
net324
net287
12u/10u
M28
"nch"
ldr=10u
wdr=12u
net287
net1887
BIAS1
12u/10u
M31
"nch"

FIG. 1100

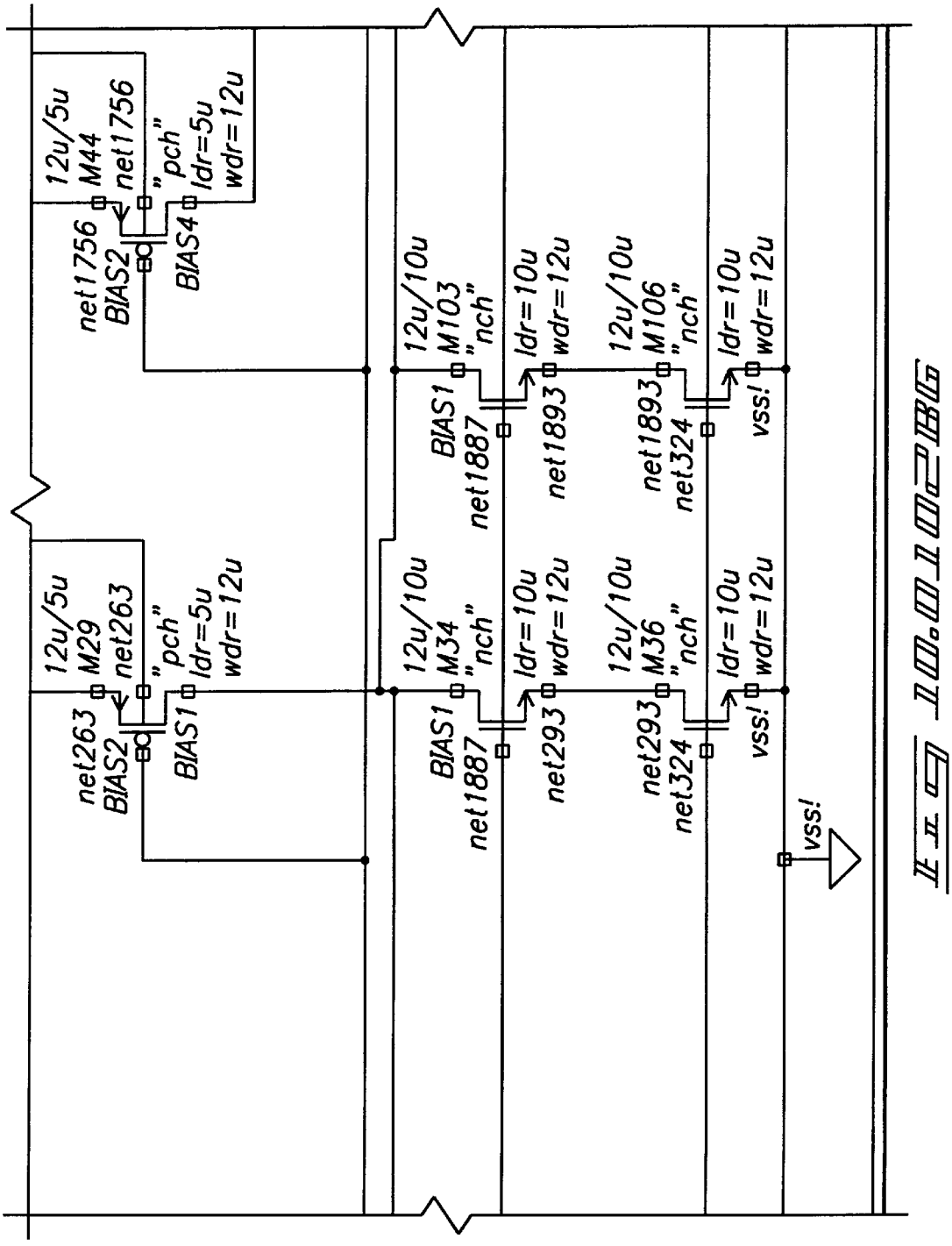

12u/5u
M44
net1756
"pch"
ldr=5u
wdr=12u
net1756
BIAS2
BIAS4
12u/10u
M103
"nch"
ldr=10u
wdr=12u
BIAS1
net1887
net1893
12u/10u
M106
"nch"
ldr=10u
wdr=12u
net1893
net324
vss!
12u/5u
M29
net263
"pch"
ldr=5u
wdr=12u
net263
BIAS2
BIAS1
12u/10u
M34
"nch"
ldr=10u
wdr=12u
BIAS1
net1887
net293
12u/10u
M36
"nch"
ldr=10u
wdr=12u
net293
net324
vss!
vss!

FIG 1001

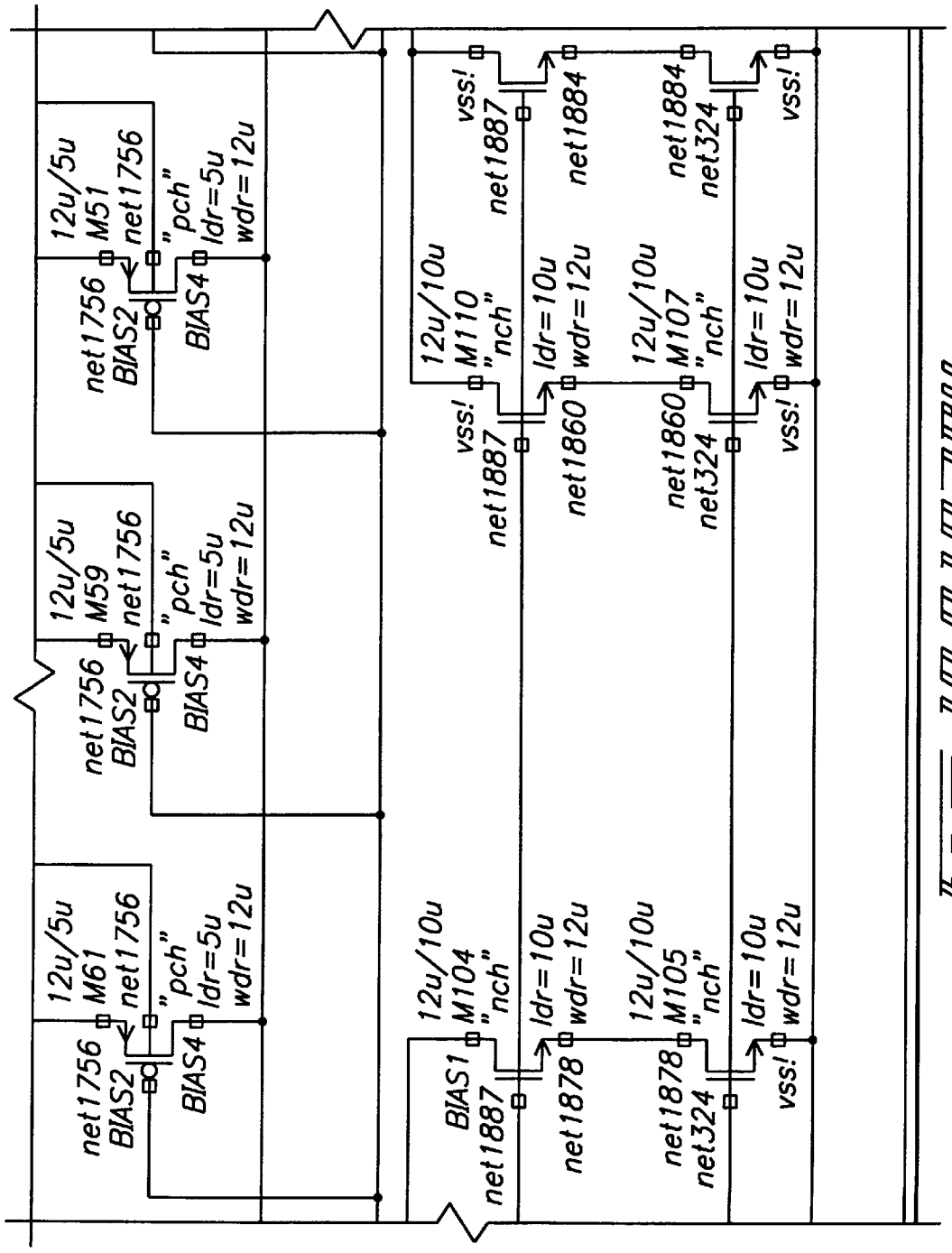

12u/5u
M61
net1756
"pch"
ldr=5u
wdr=12u
net1756
BIAS2
BIAS4
12u/5u
M59
net1756
"pch"
ldr=5u
wdr=12u
net1756
BIAS2
BIAS4
12u/5u
M51
net1756
"pch"
ldr=5u
wdr=12u
net1756
BIAS2
BIAS4
12u/10u
M104
"nch"
ldr=10u
wdr=12u
BIAS1
net1887
net1878
12u/10u
M105
"nch"
ldr=10u
wdr=12u
net1878
net324
vss!
12u/10u
M110
"nch"
ldr=10u
wdr=12u
vss!
net1887
net1860
12u/10u
M107
"nch"
ldr=10u
wdr=12u
net1860
net324
vss!
vss!
net1887
net1884
net1884
net324
vss!

FIG 100,001

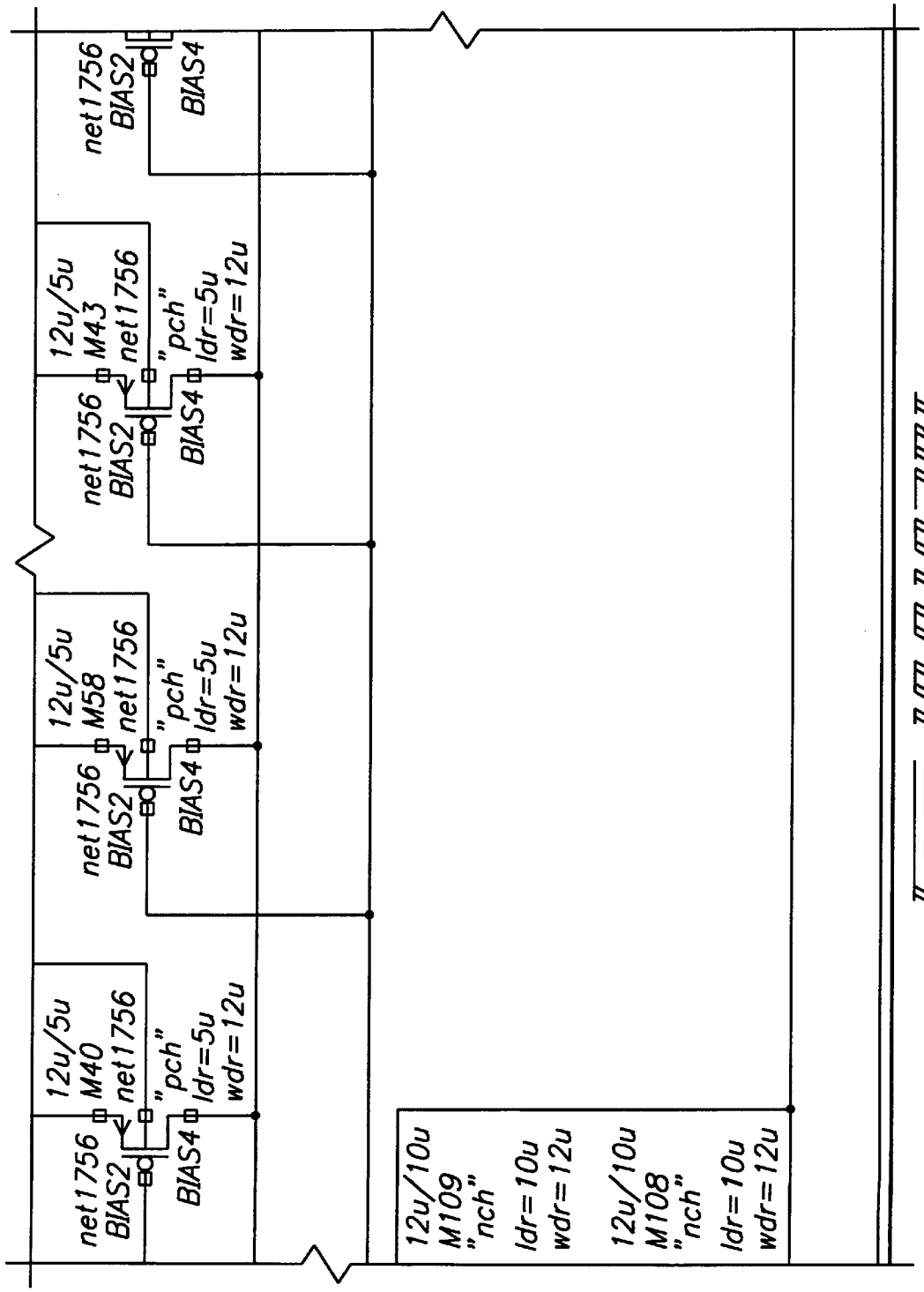

net1756
BIAS2
BIAS4
12u/5u
M43
net1756
"pch"
ldr=5u
wdr=12u
12u/5u
M58
net1756
"pch"
ldr=5u
wdr=12u
12u/5u
M40
net1756
"pch"
ldr=5u
wdr=12u
12u/10u
M109
"nch"
ldr=10u
wdr=12u
12u/10u
M108
"nch"
ldr=10u
wdr=12u

FIG 100

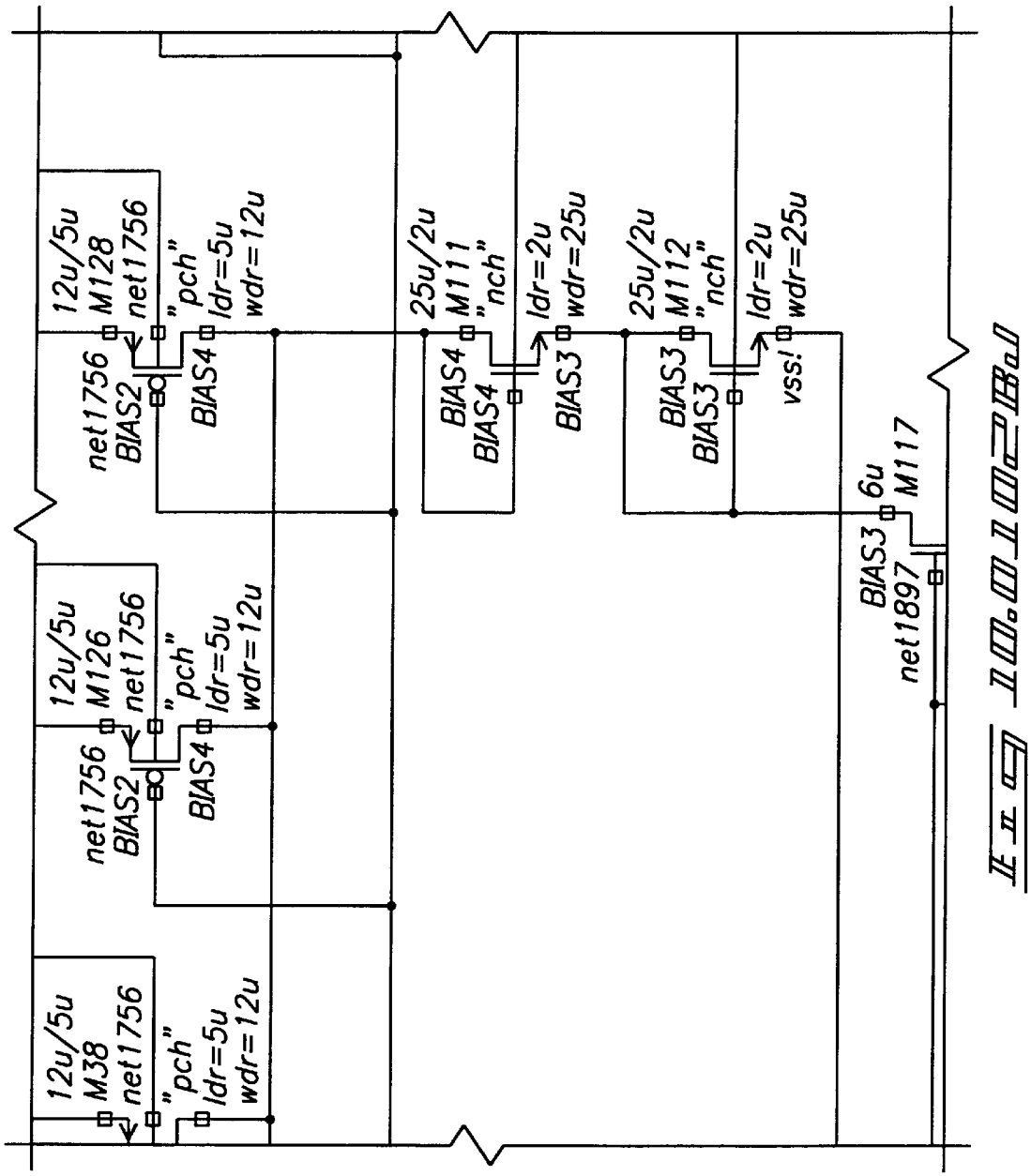

12u/5u
M128
net1756
"pch"
ldr=5u
wdr=12u
net1756
BIAS2
BIAS4
25u/2u
M111
"nch"
ldr=2u
wdr=25u
BIAS4
BIAS4
BIAS3
25u/2u
M112
"nch"
ldr=2u
wdr=25u
BIAS3
BIAS3
vss!
6u
M117
BIAS3
net1897
12u/5u
M126
net1756
"pch"
ldr=5u
wdr=12u
net1756
BIAS2
BIAS4
12u/5u
M38
net1756
"pch"
ldr=5u
wdr=12u

FIG 1100

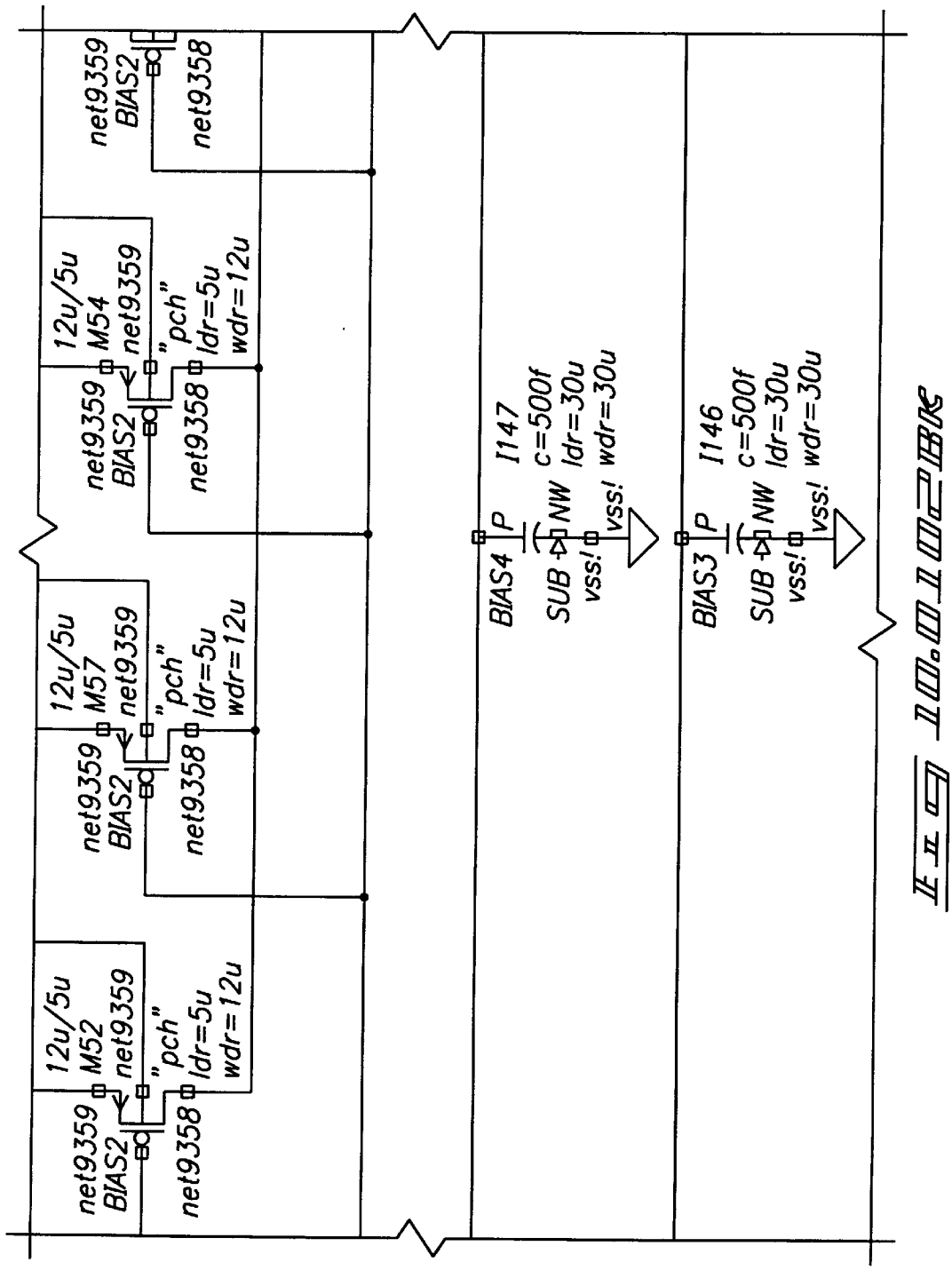

net9359
BIAS2
net9358
12u/5u
M54
net9359
"pch"
ldr=5u
wdr=12u
net9359
BIAS2
net9358
12u/5u
M57
net9359
"pch"
ldr=5u
wdr=12u
net9359
BIAS2
net9358
12u/5u
M52
net9359
"pch"
ldr=5u
wdr=12u
net9359
BIAS2
net9358
BIAS4
P
I147
c=500f
ldr=30u
wdr=30u
SUB
NW
vss!
vss!
BIAS3
P
I146
c=500f
ldr=30u
wdr=30u
SUB
NW
vss!
vss!

FIG 100,001B

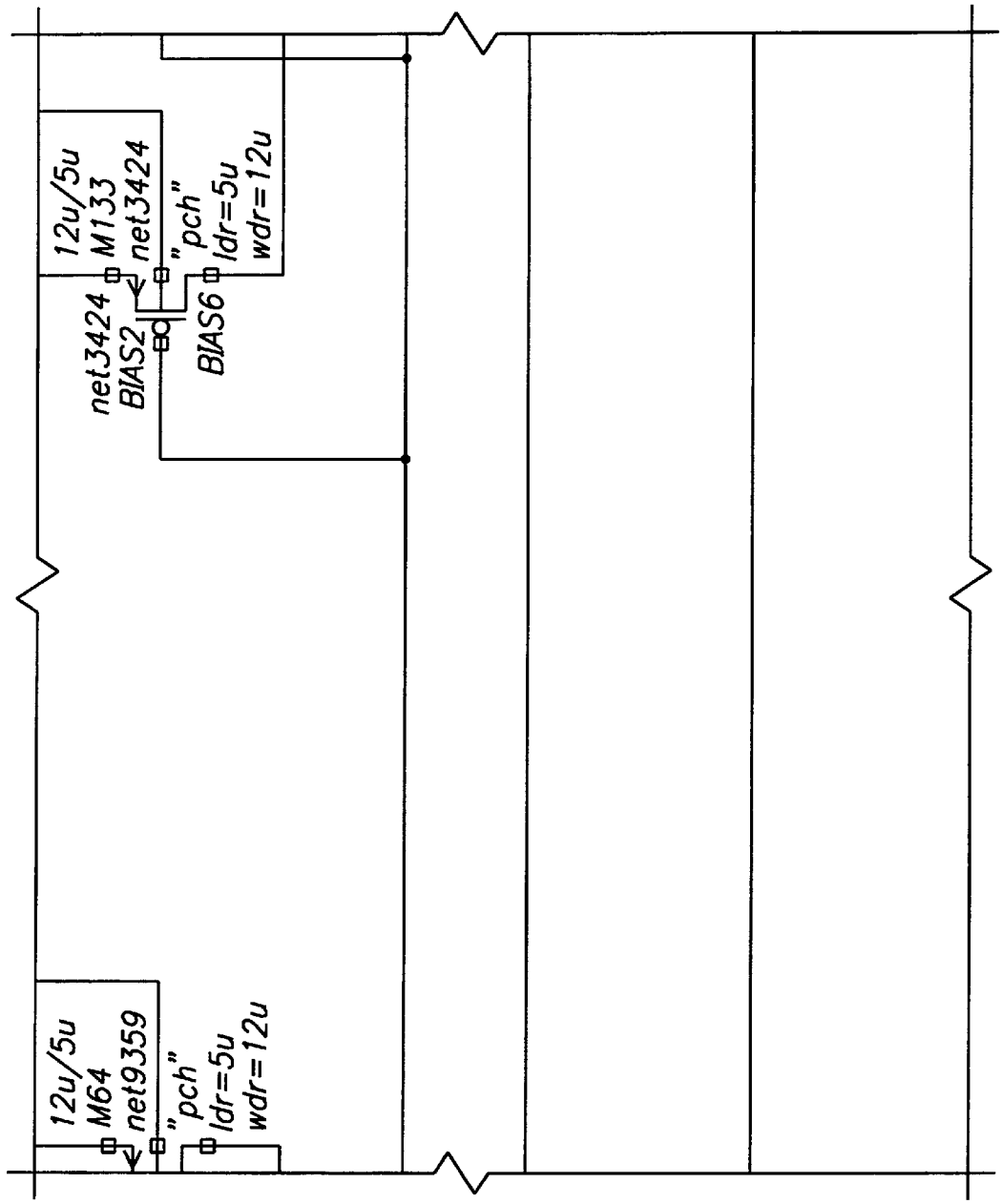


FIG 100,011,218

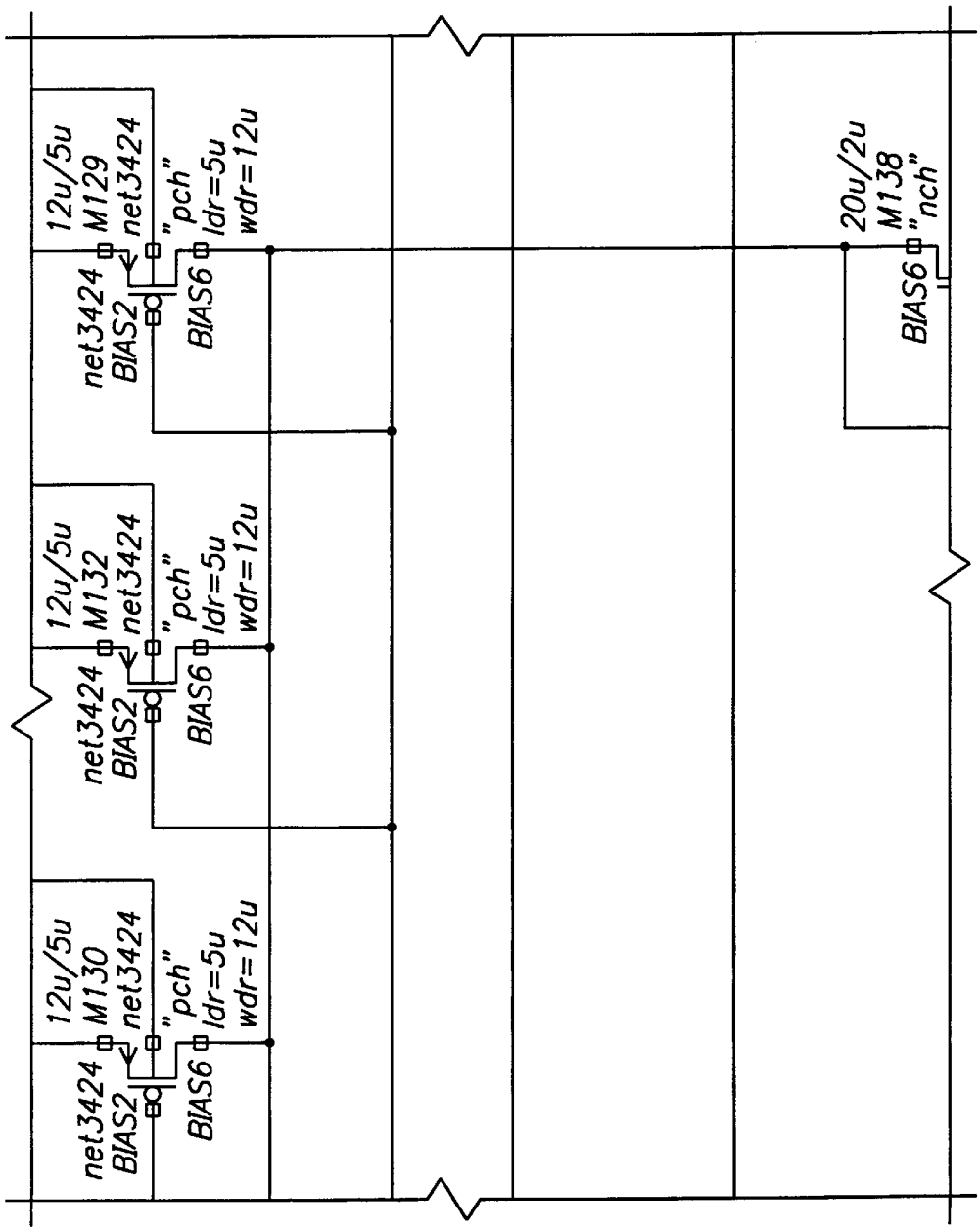


FIG 10.00120BM

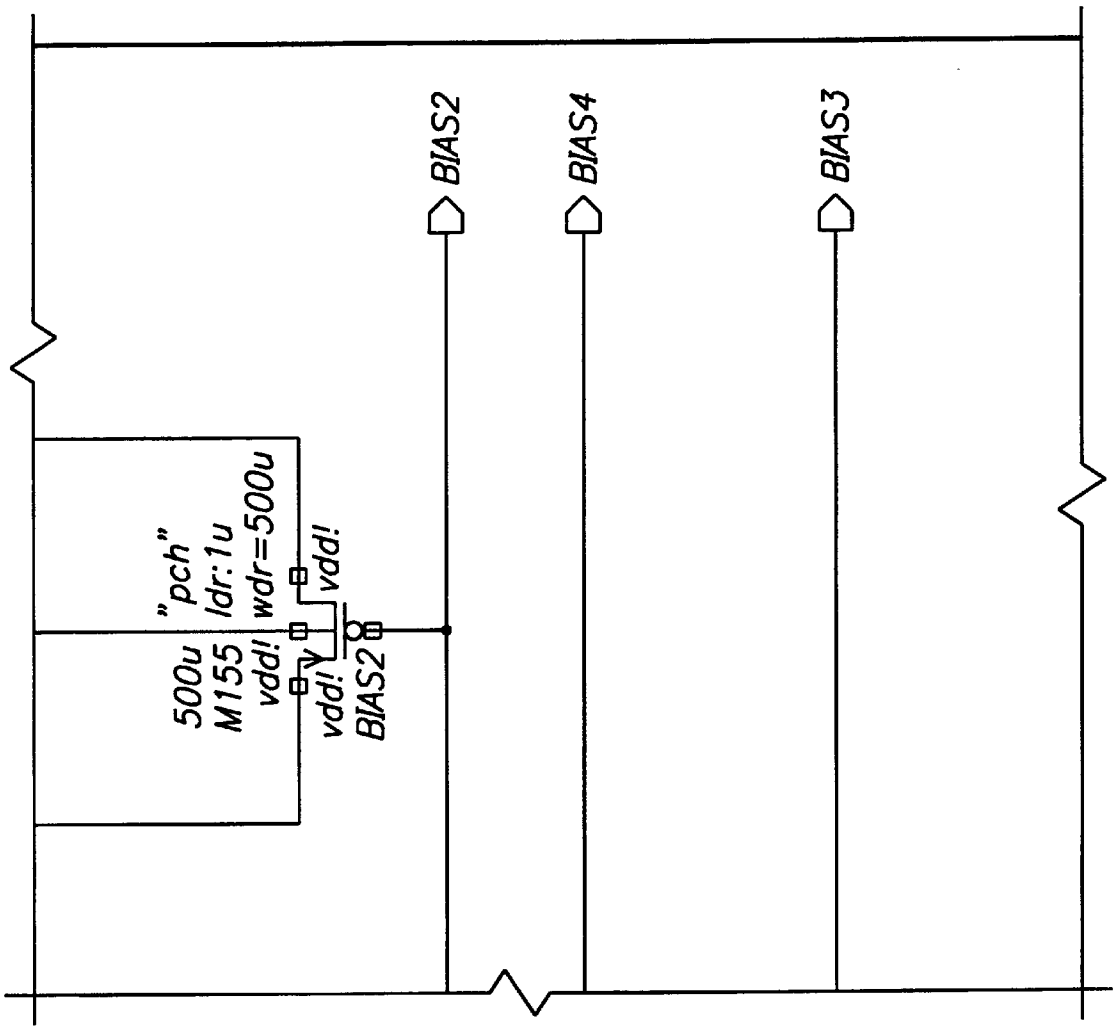


FIG 100,011,002,180N

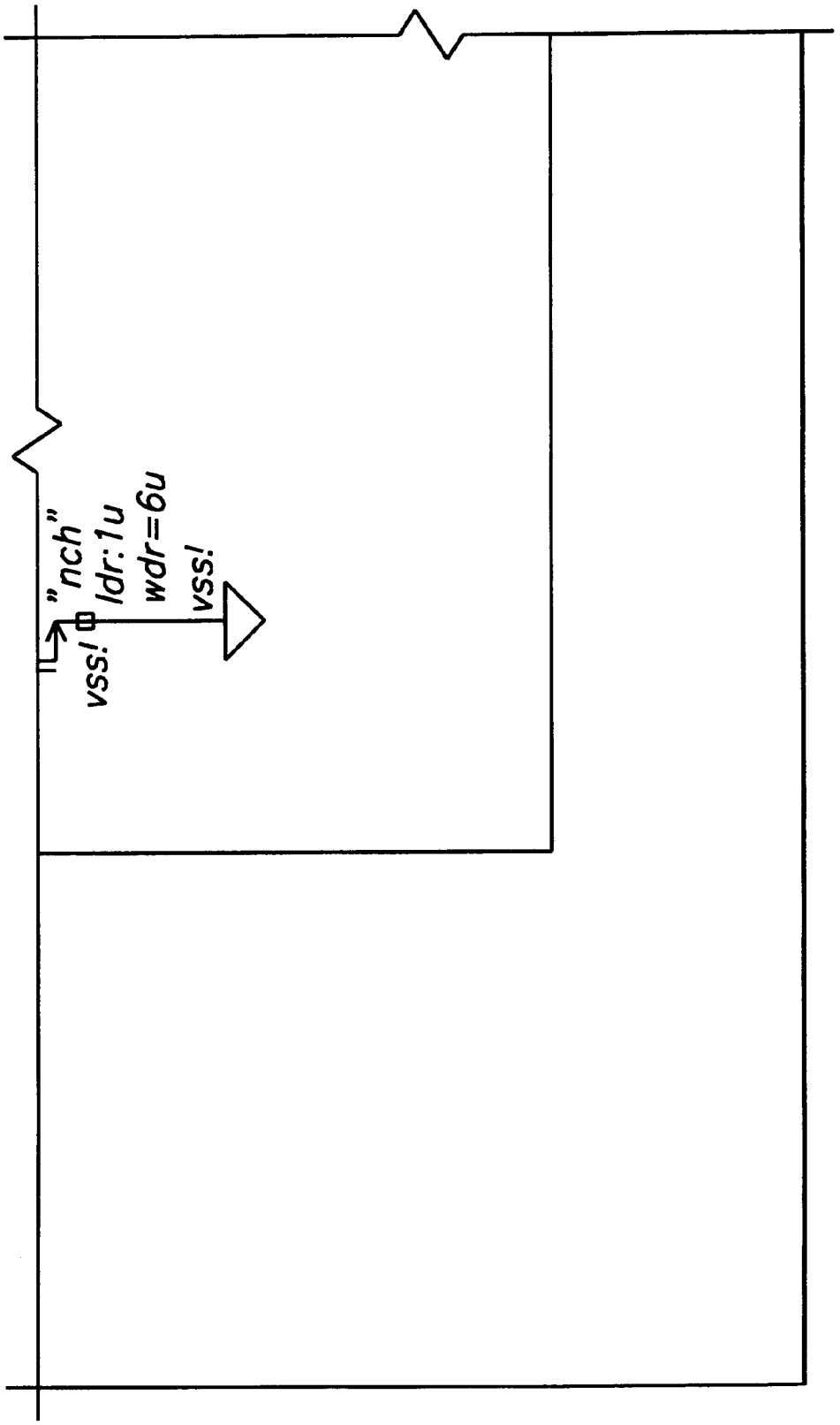


FIG 100,001

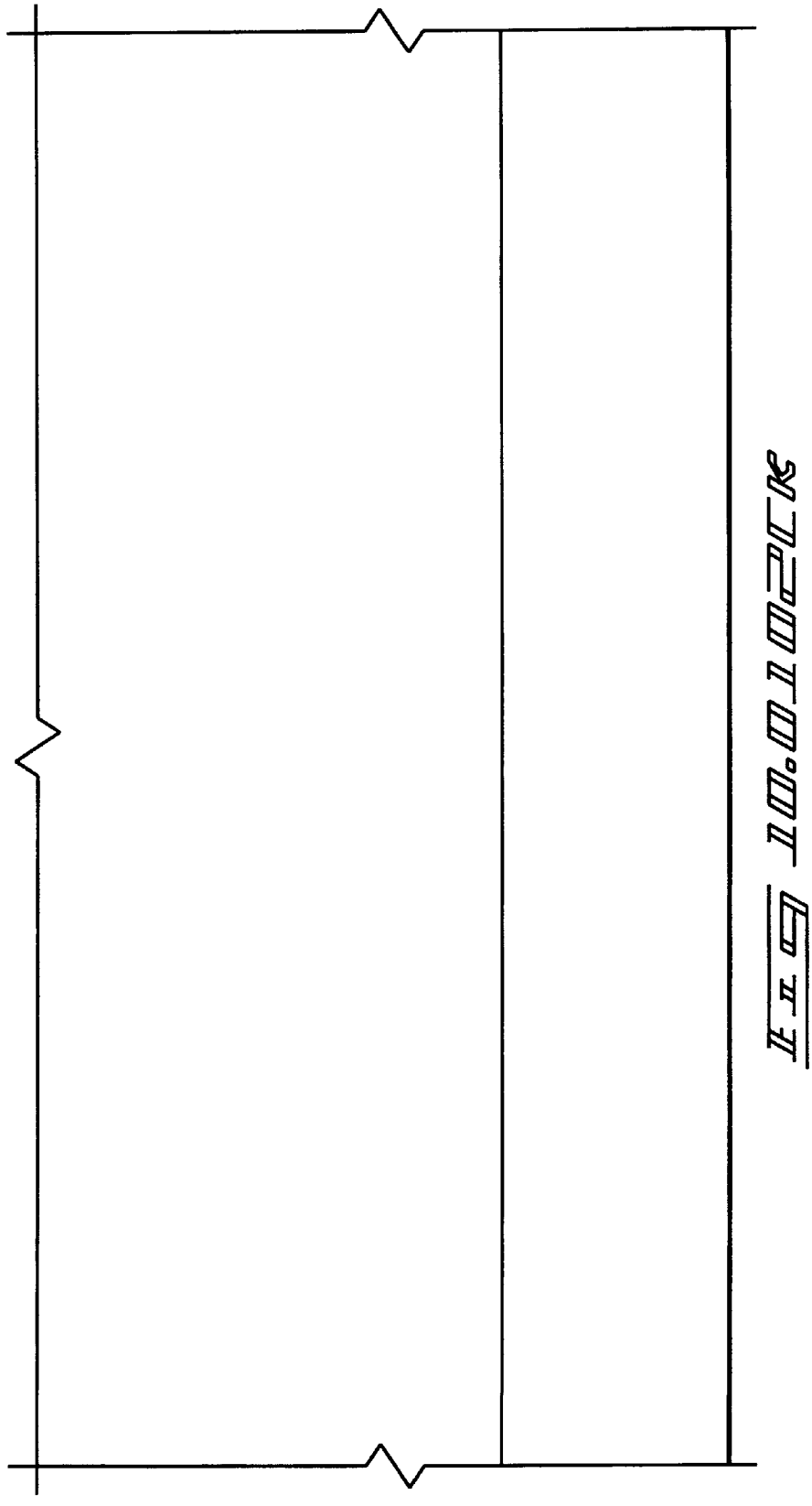


FIG 10,01127K

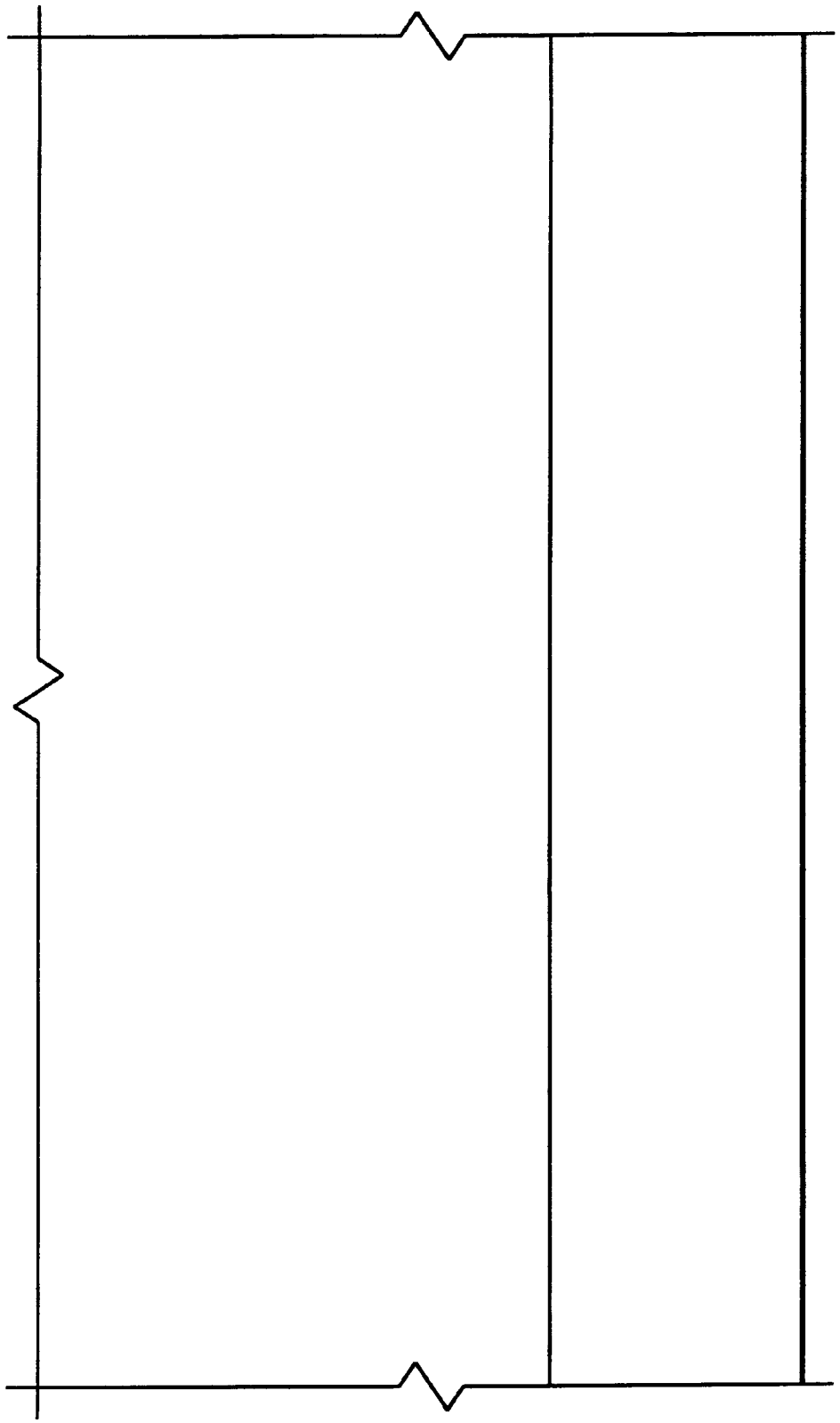


FIG 100,011,021.

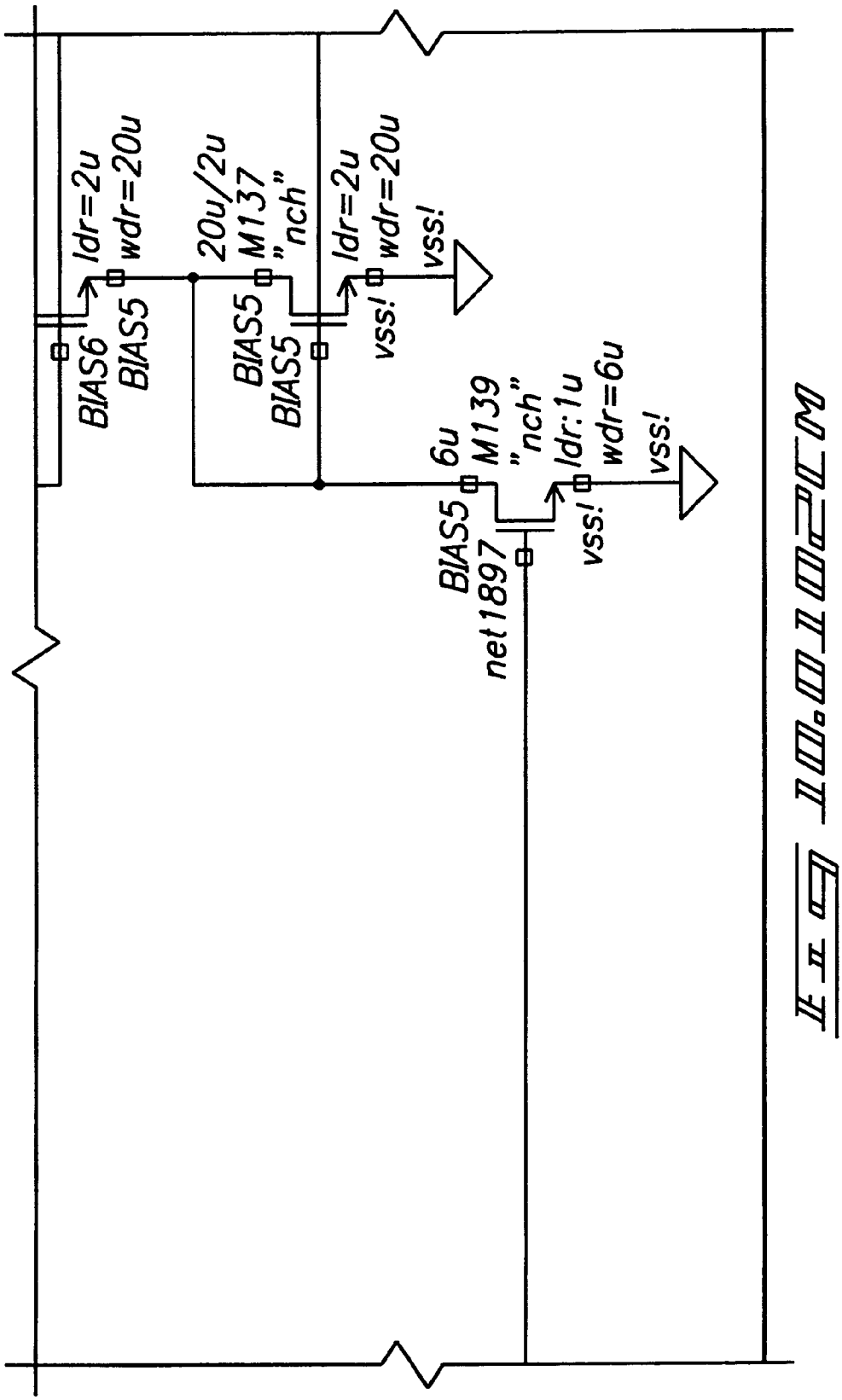

ldr=2u
wdr=20u
20u/2u
M137
"nch"
ldr=2u
wdr=20u
vss!
BIAS6
BIAS5
BIAS5
BIAS5
vss!
6u
M139
"nch"
ldr:1u
wdr=6u
vss!
BIAS5
net1897
vss!

FIG 11

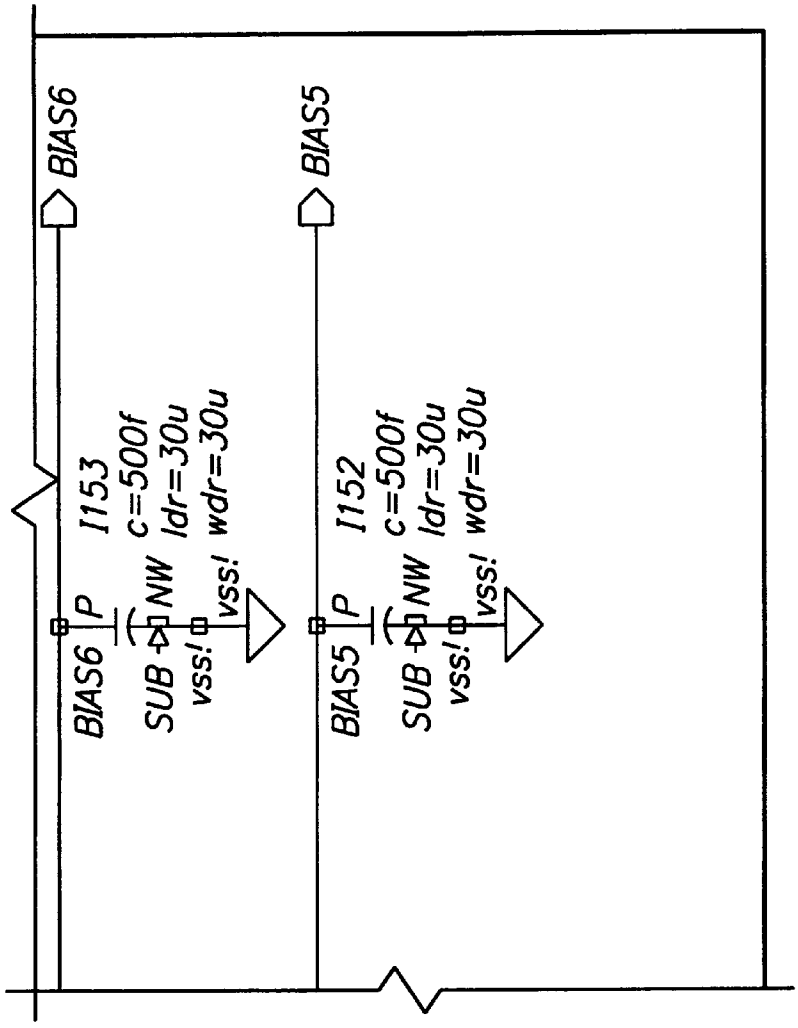

BIAS6
BIAS5
I153
c=500f
ldr=30u
wdr=30u
vss!
P
NW
SUB
I152
c=500f
ldr=30u
wdr=30u
vss!
P
NW
SUB

FIG 1100

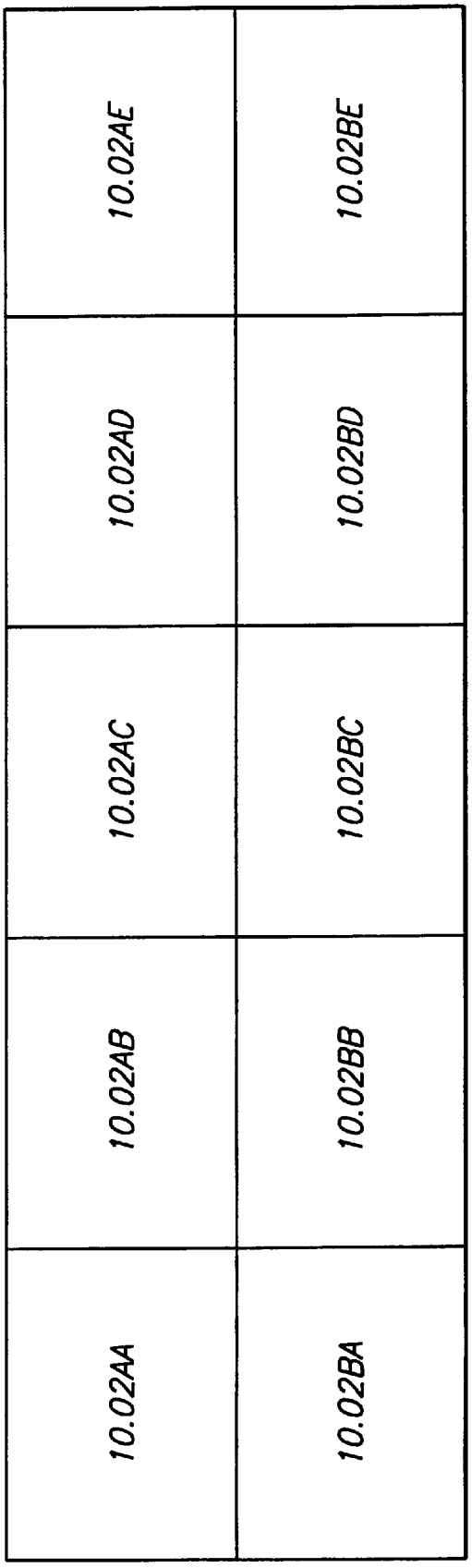

10.02AE
10.02BE
10.02AD
10.02BD
10.02AC
10.02BC
10.02AB
10.02BB
10.02AA
10.02BA

FIG 100.02

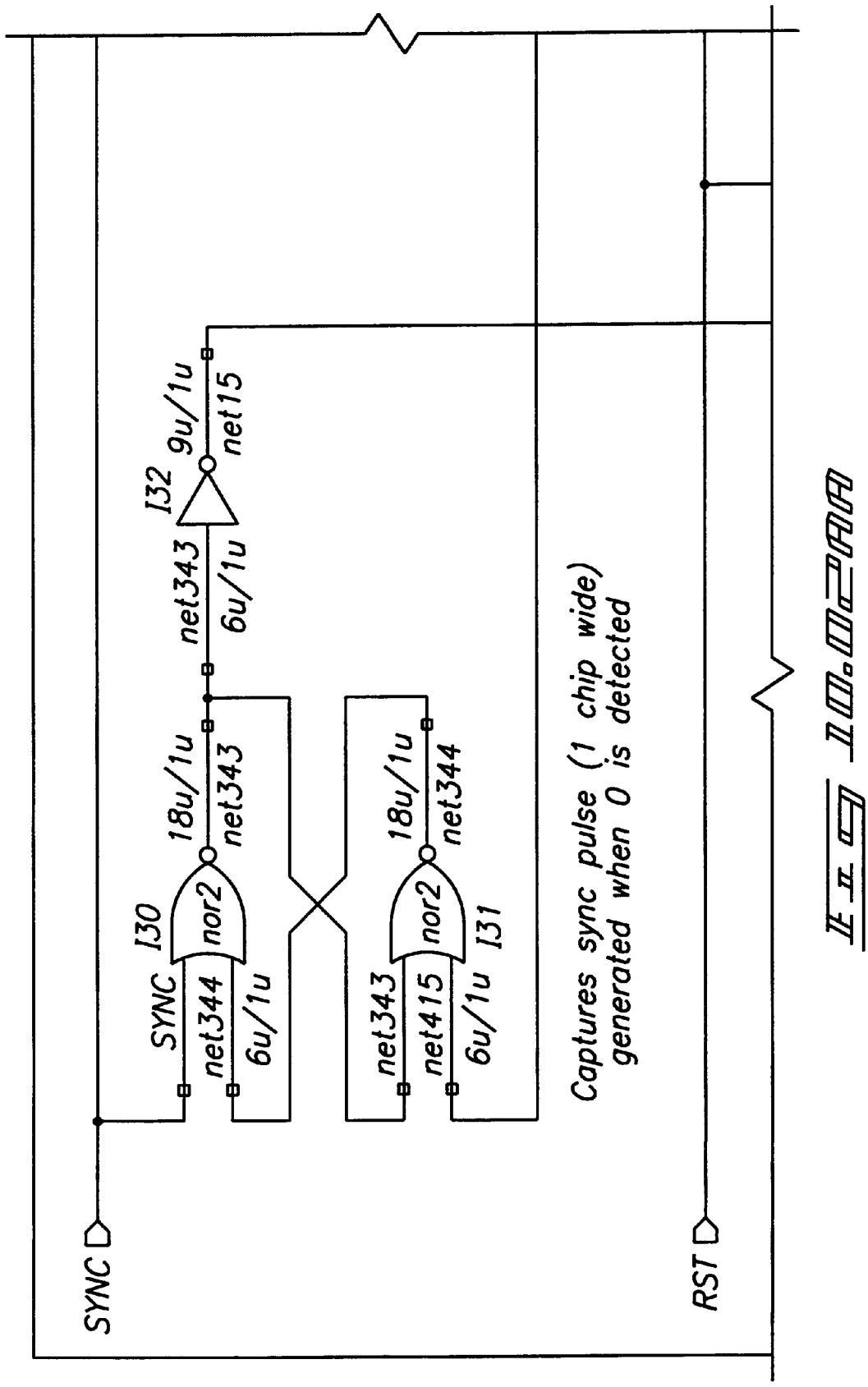

SYNC
RST
I30
nor2
SYNC
net344
6u/1u
18u/1u
net343
I31
nor2
net343
net415
6u/1u
18u/1u
net344
I32
9u/1u
net15
net343
6u/1u
Captures sync pulse (1 chip wide)
generated when 0 is detected

FIG 100.2AA

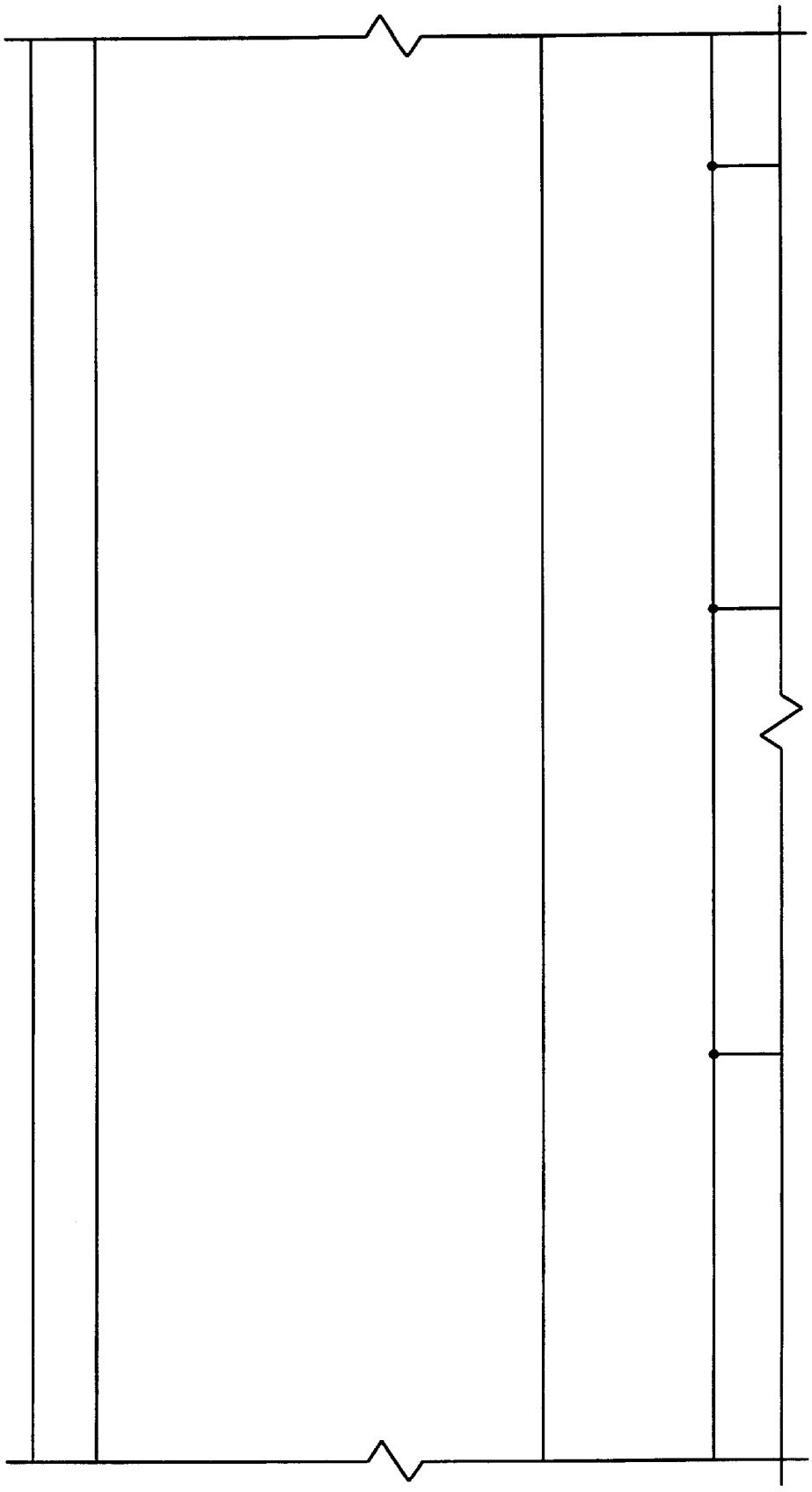


FIG 10,028B

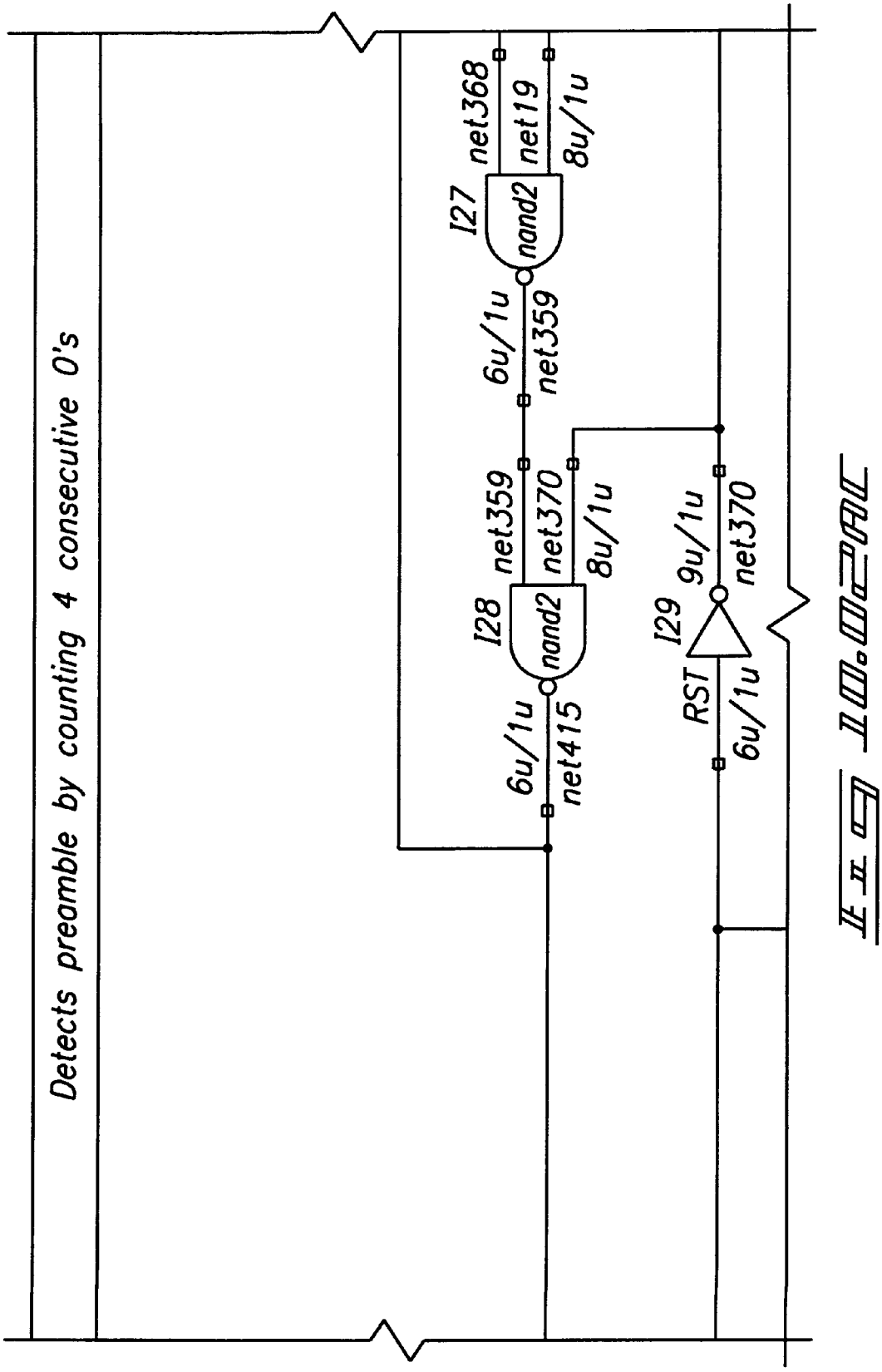
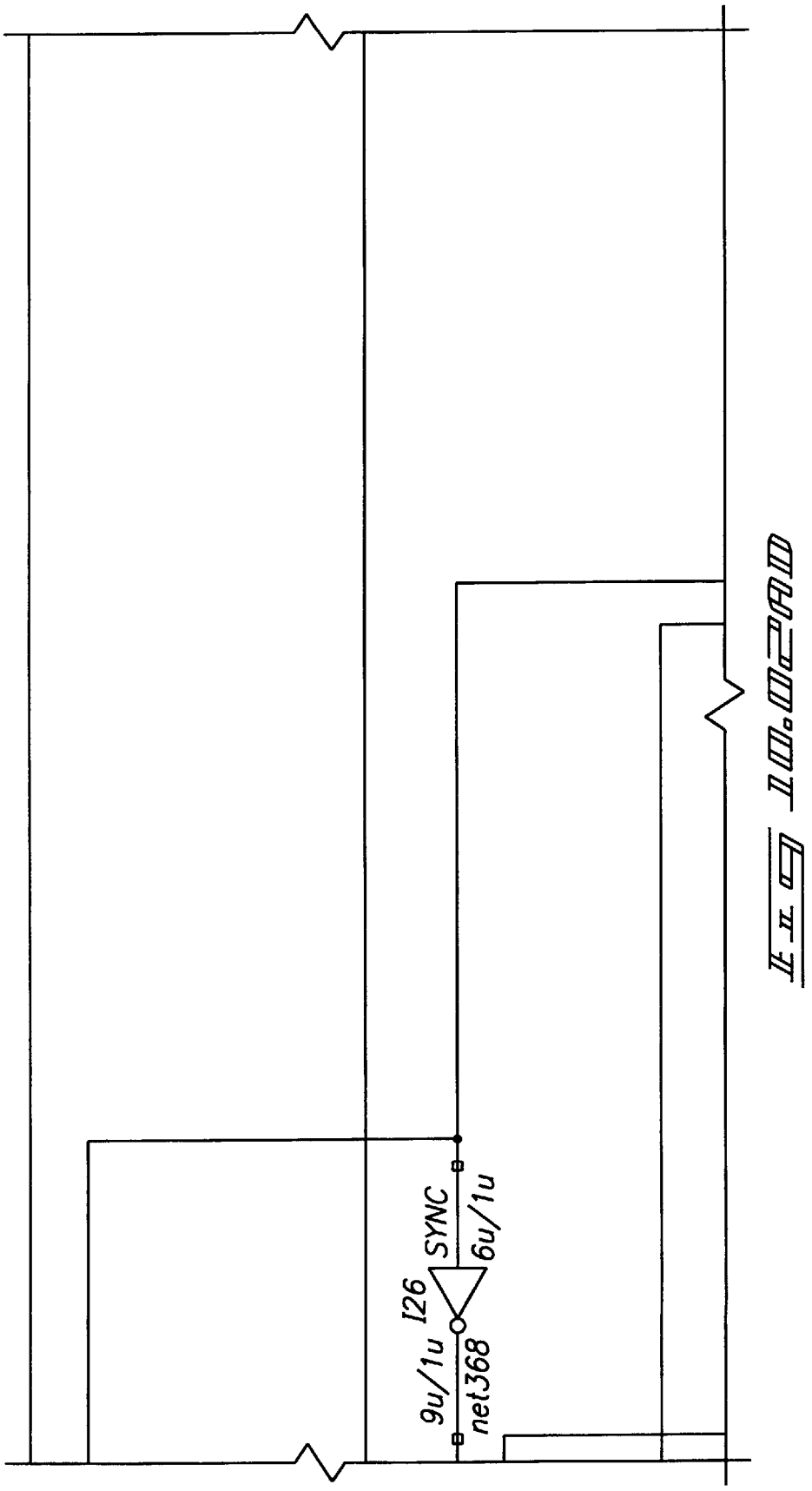


FIG 1100.0022


net368
9u/1u
I26
SYNC
6u/1u

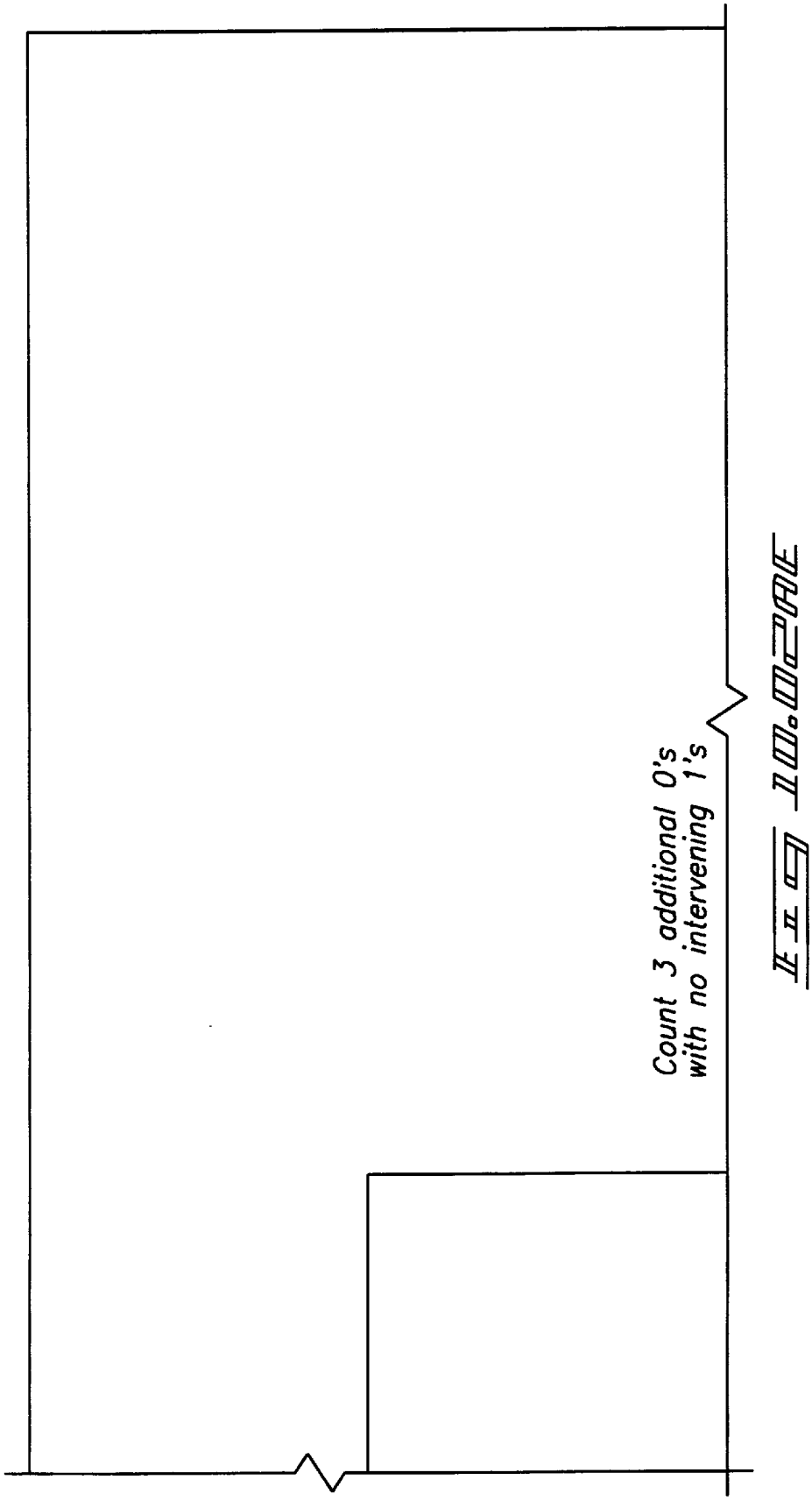


FIG 100,2AE
Count 3 additional 0's
with no intervening 1's

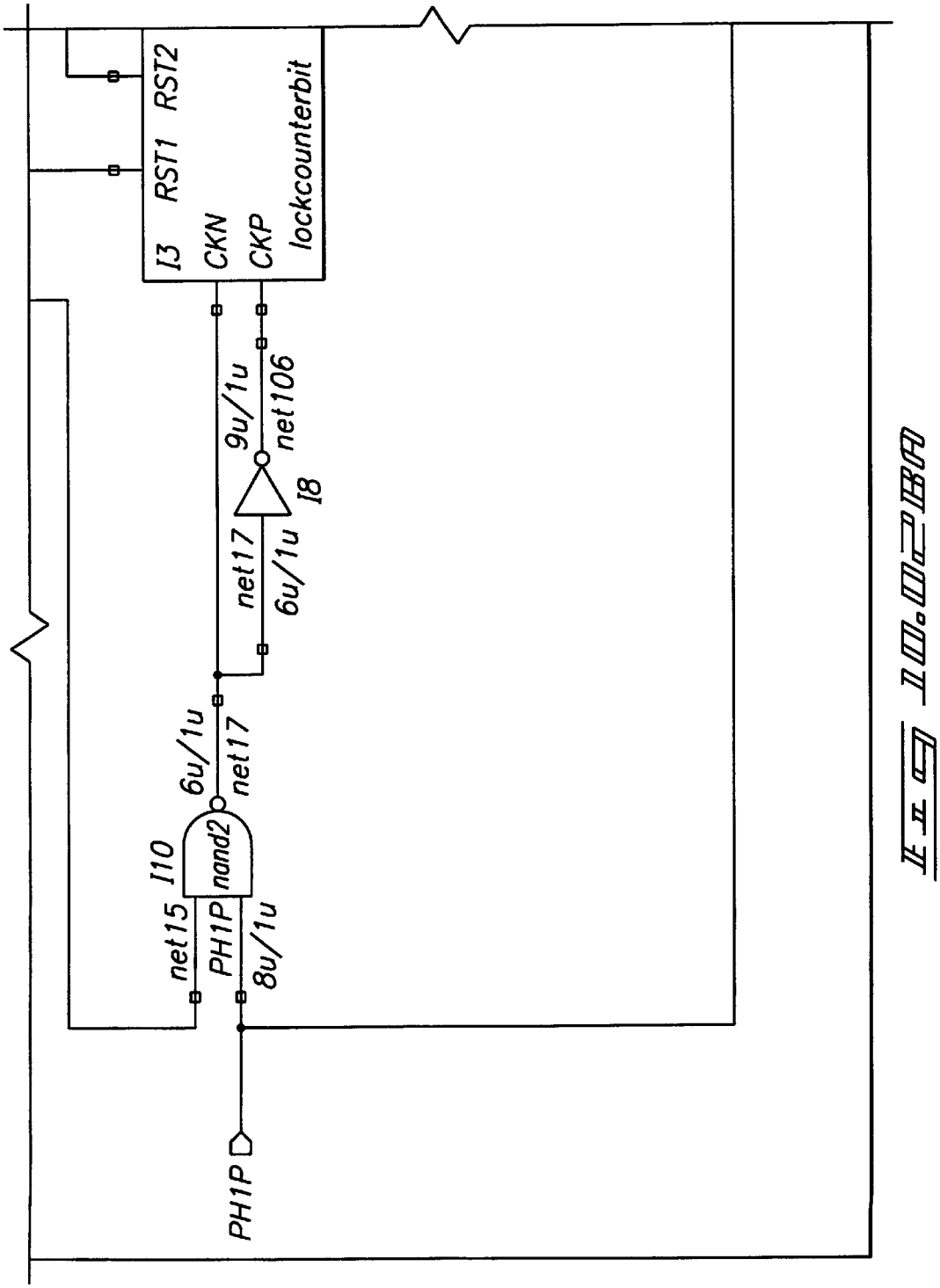

I3
RST1
RST2
CKN
CKP
lockcounterbit
9u/1u
net106
I8
net17
6u/1u
6u/1u
net17
I10
nand2
net15
PH1P
8u/1u
PH1P

FIG 100,2BA

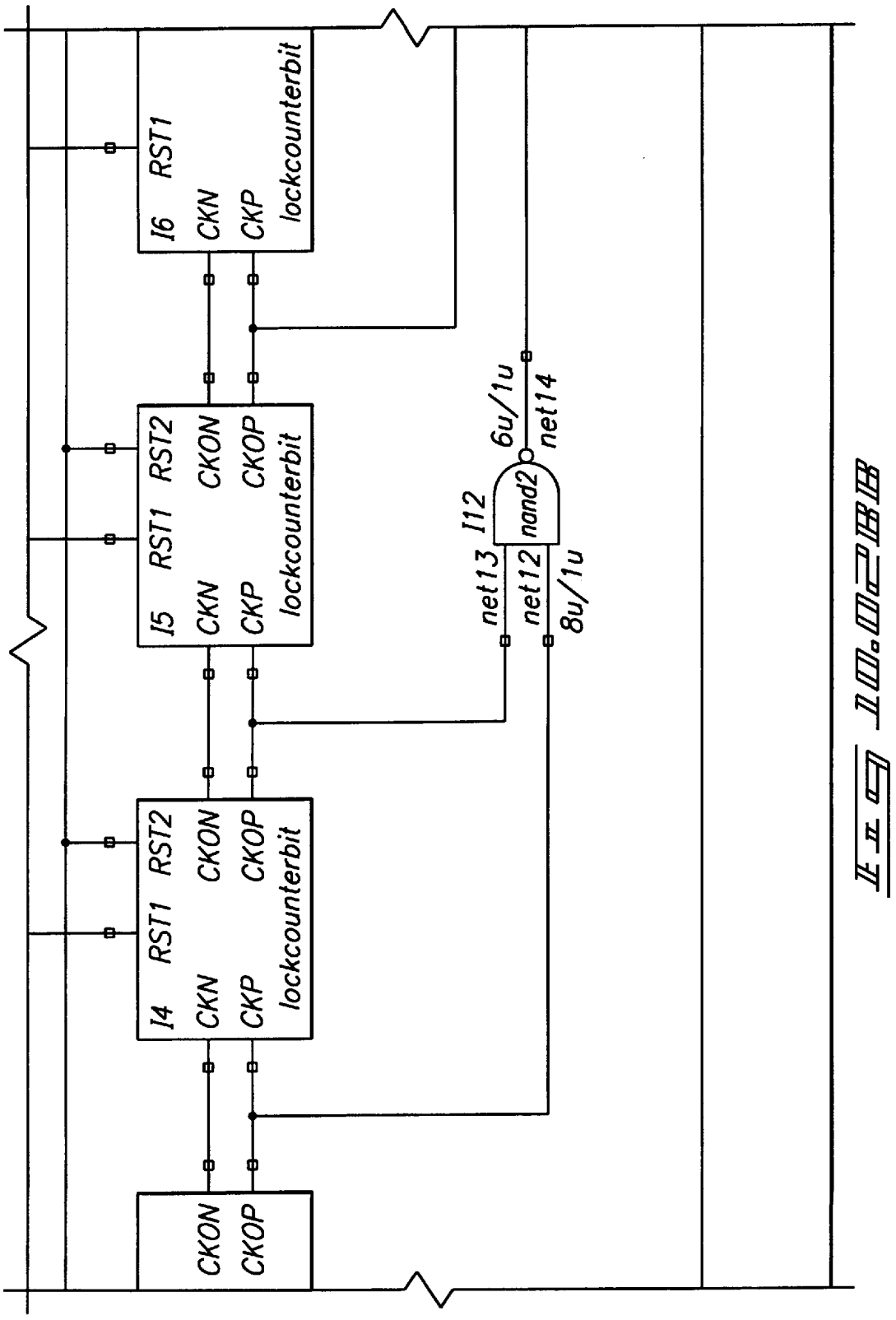

I6 RST1 CKN CKP lockcounterbit
I5 RST1 RST2 CKON CKOP CKN CKP lockcounterbit
I4 RST1 RST2 CKON CKOP CKN CKP lockcounterbit
CKON CKOP
I12 nand2
net13 net12
6u/1u net14
8u/1u

FIG 109,002

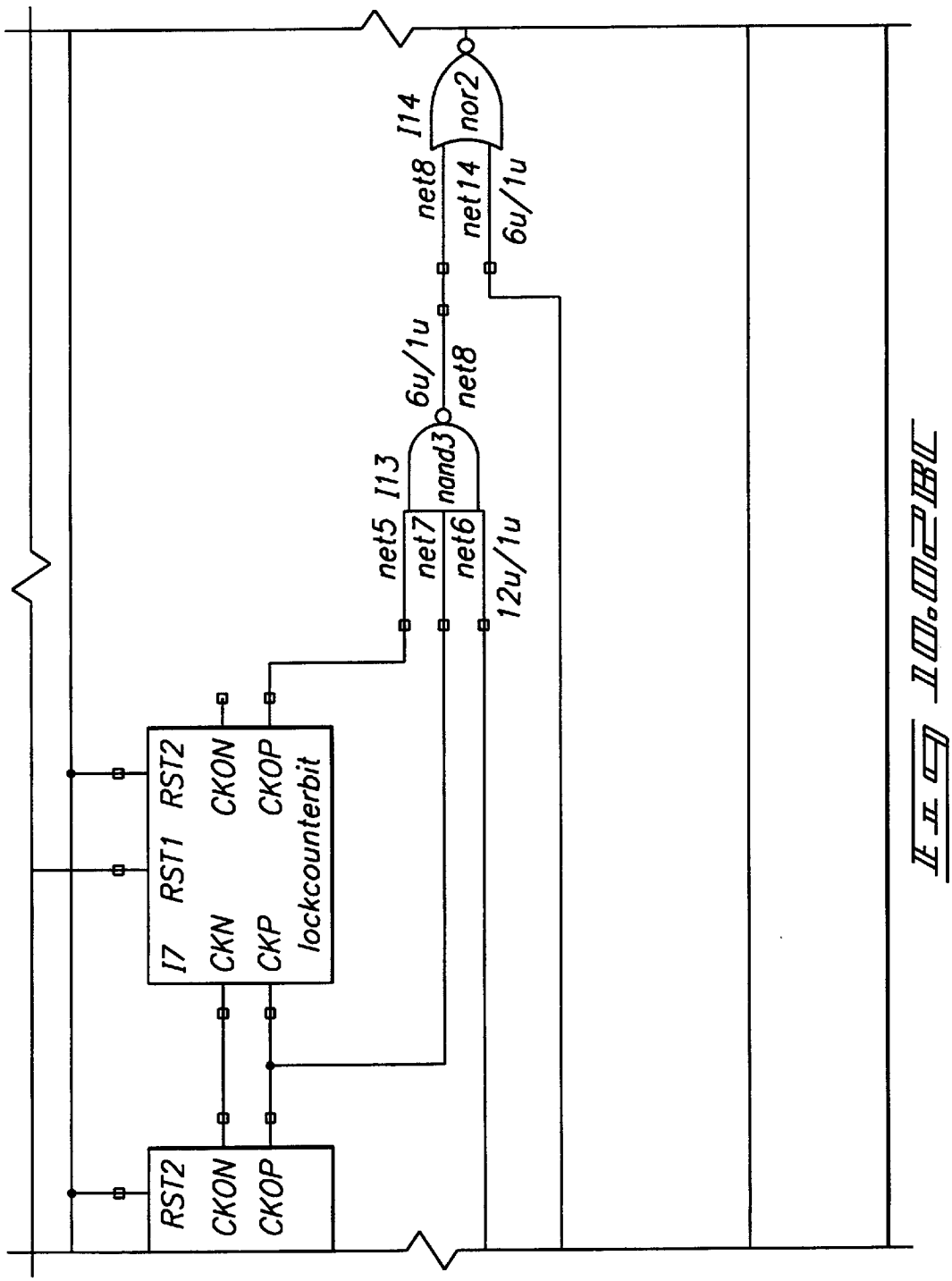
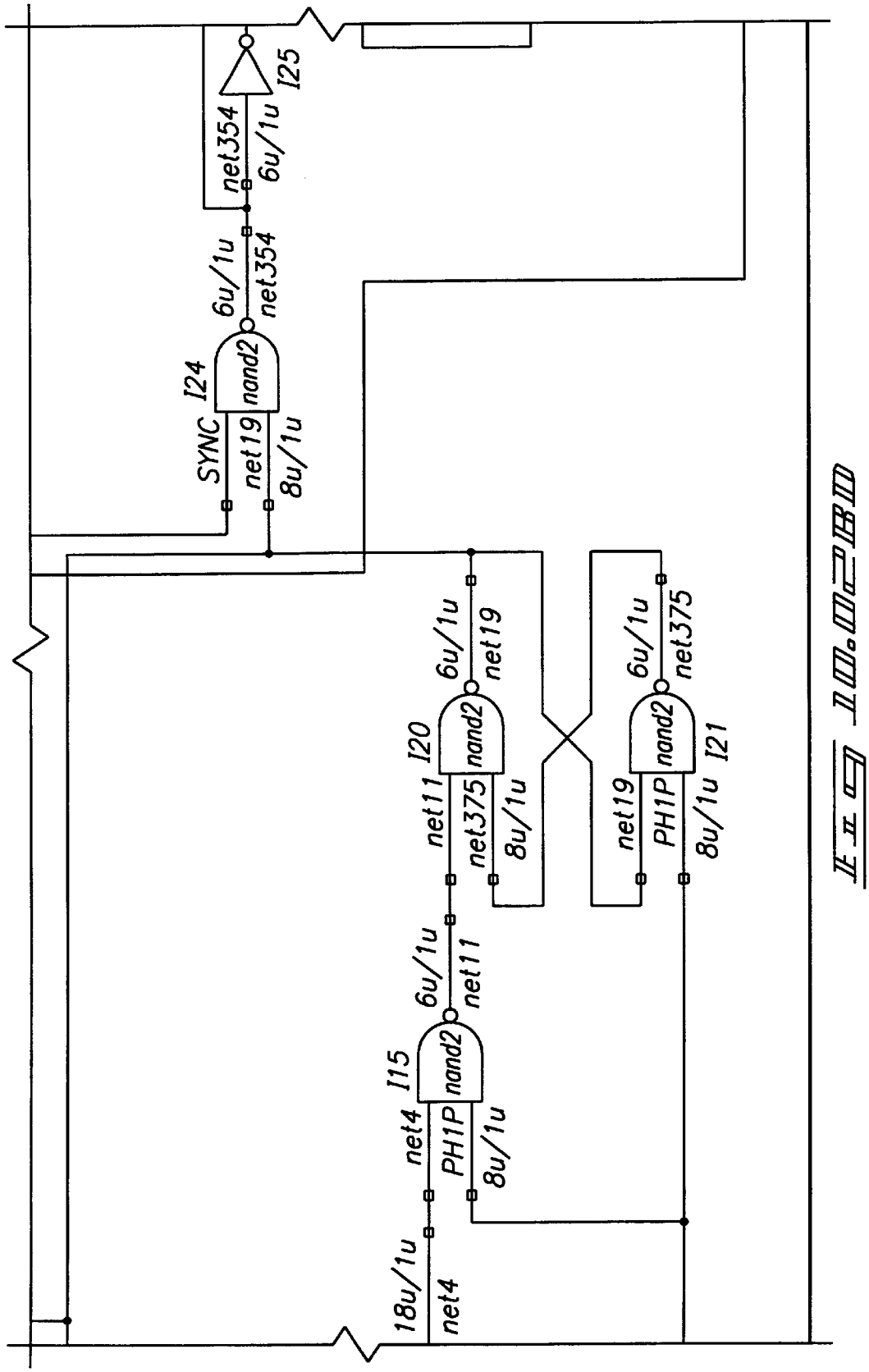

I14
nor2
net8
net14
6u/1u
6u/1u
net8
I13
nand3
net5
net7
net6
12u/1u
I7
RST1
RST2
CKN
CKP
CKON
CKOP
lockcounterbit
RST2
CKON
CKOP

FIG 100.02BC


I25
net354
6u/1u
6u/1u
net354
I24
nand2
SYNC
net19
8u/1u
6u/1u
net19
I20
nand2
net11
net375
8u/1u
6u/1u
net375
I21
nand2
net19
PH1P
8u/1u
6u/1u
net11
I15
nand2
net4
PH1P
8u/1u
18u/1u
net4

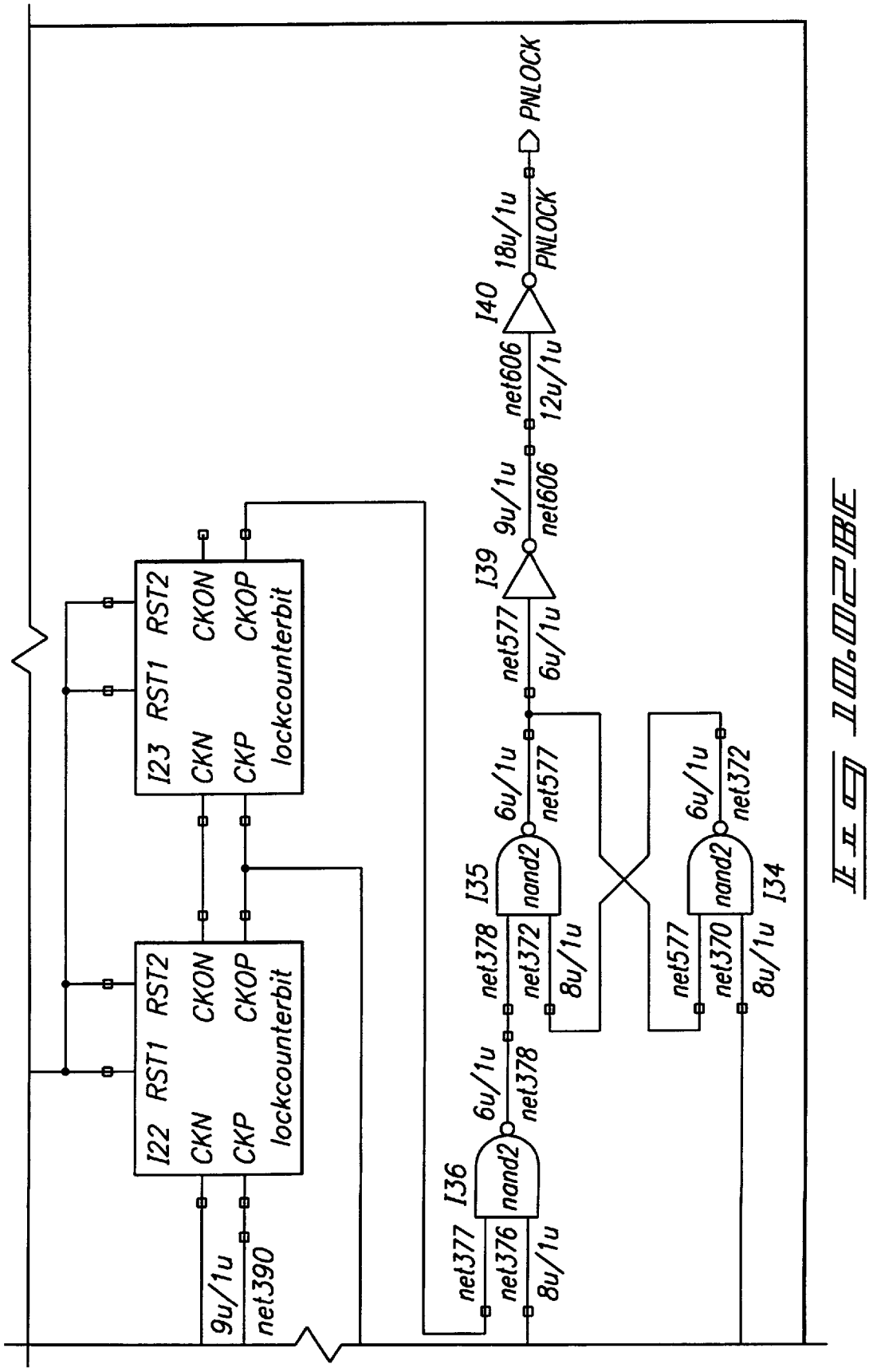


FIG. 1100.2186

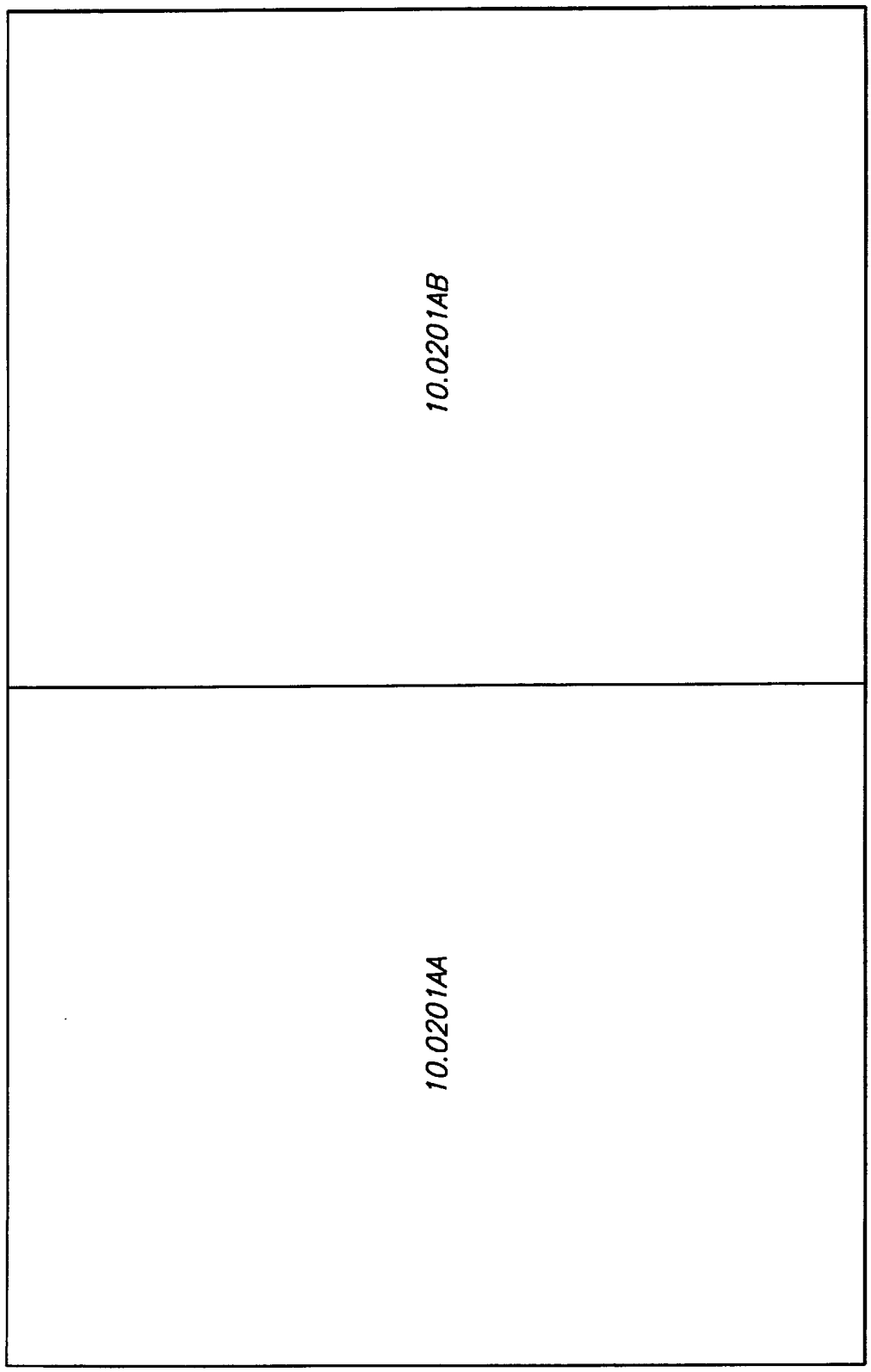


FIG 100.00211

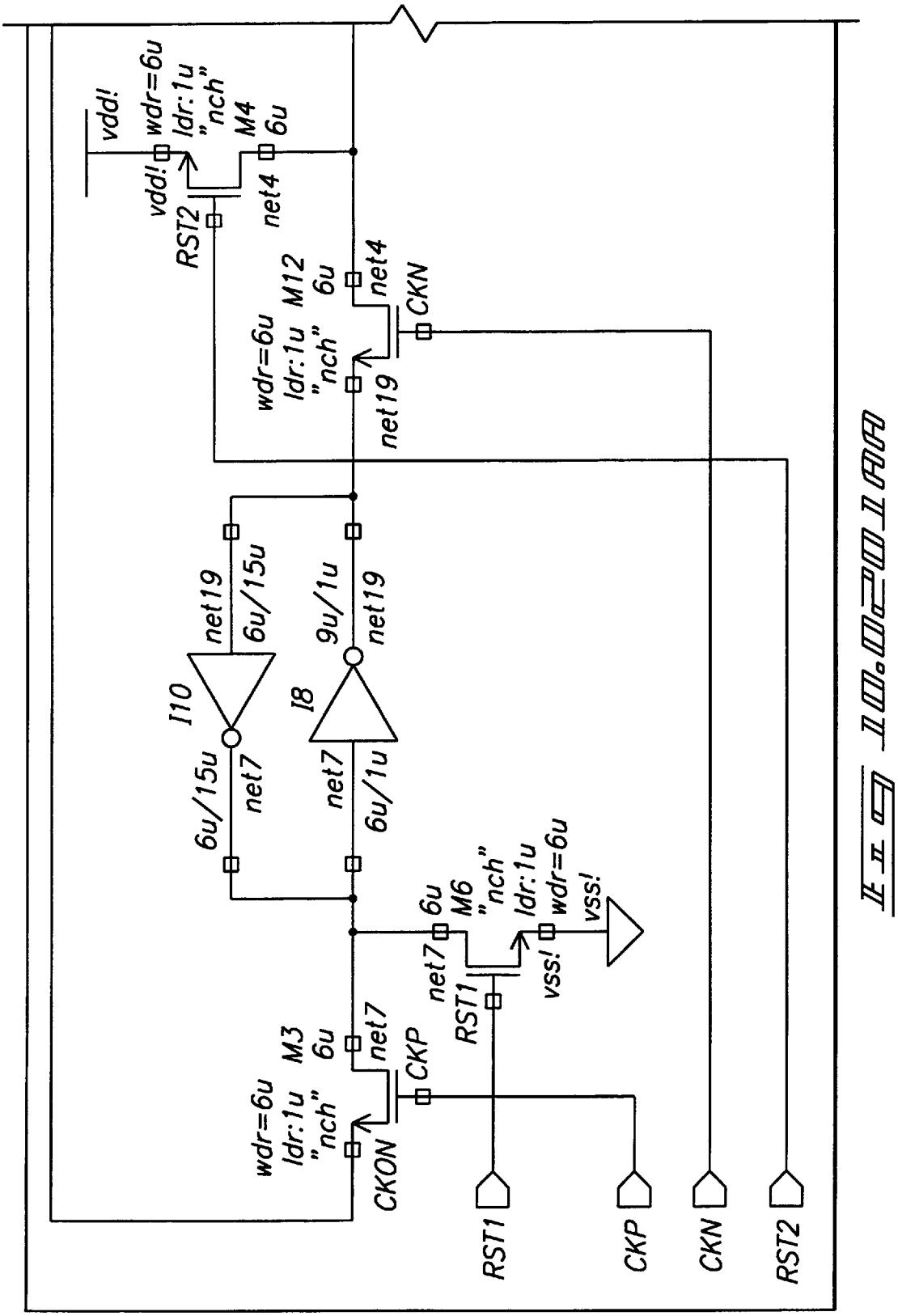

vdd!
wdr=6u
ldr:1u
"nch"
M4
6u
vdd!
RST2
net4
M12
6u
net4
CKN
wdr=6u
ldr:1u
"nch"
net19
net19
6u/15u
9u/1u
net19
I10
I8
6u/15u
net7
net7
6u/1u
6u
M6
"nch"
ldr:1u
wdr=6u
vss!
net7
RST1
vss!
M3
6u
net7
CKP
wdr=6u
ldr:1u
"nch"
CKON
RST1
CKP
CKN
RST2

FIG 109

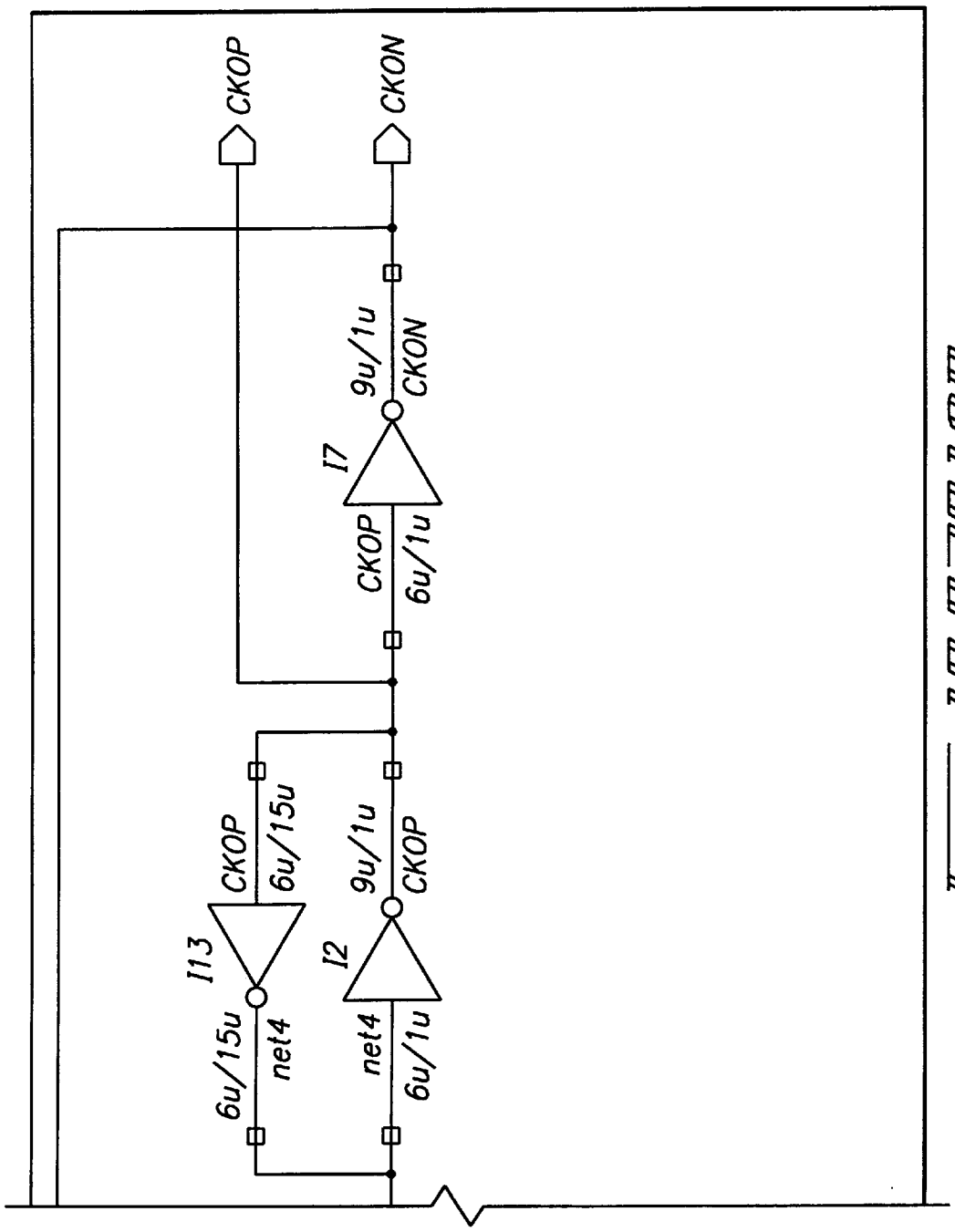
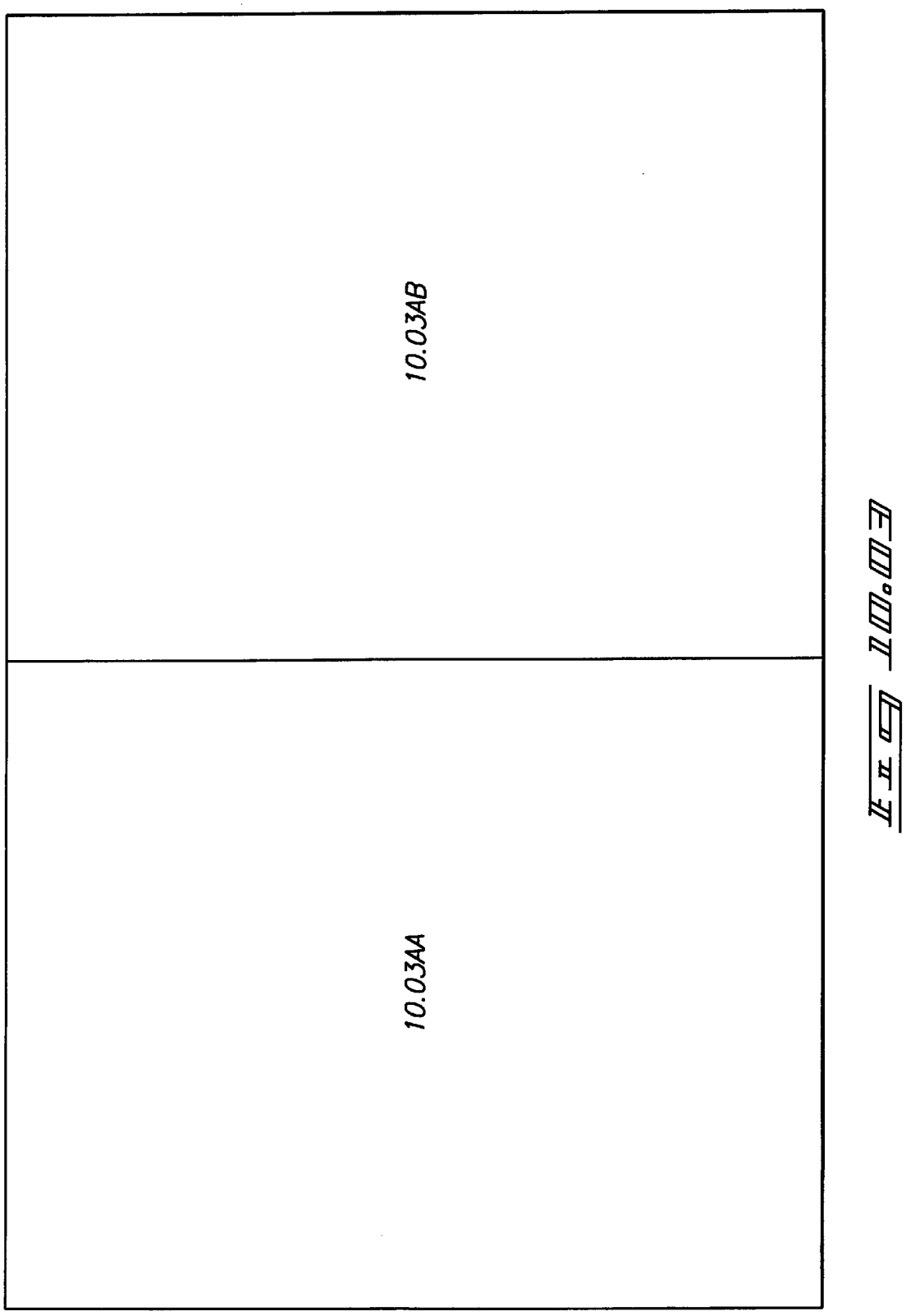


FIG 1007.01 AUTOZOOM


10.03AB
10.03AA
E 100.00 FT

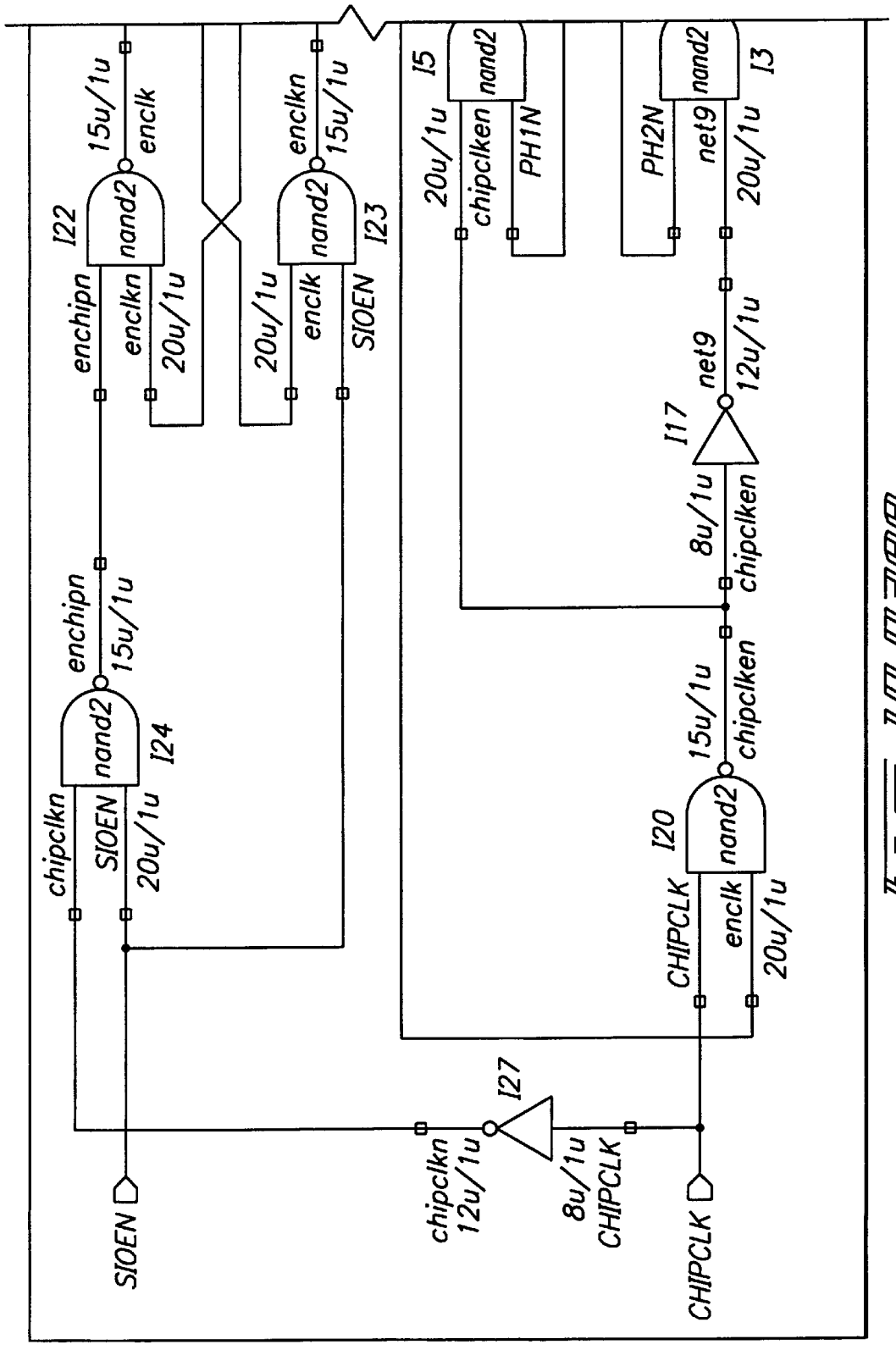


FIG. 1100.3AAA

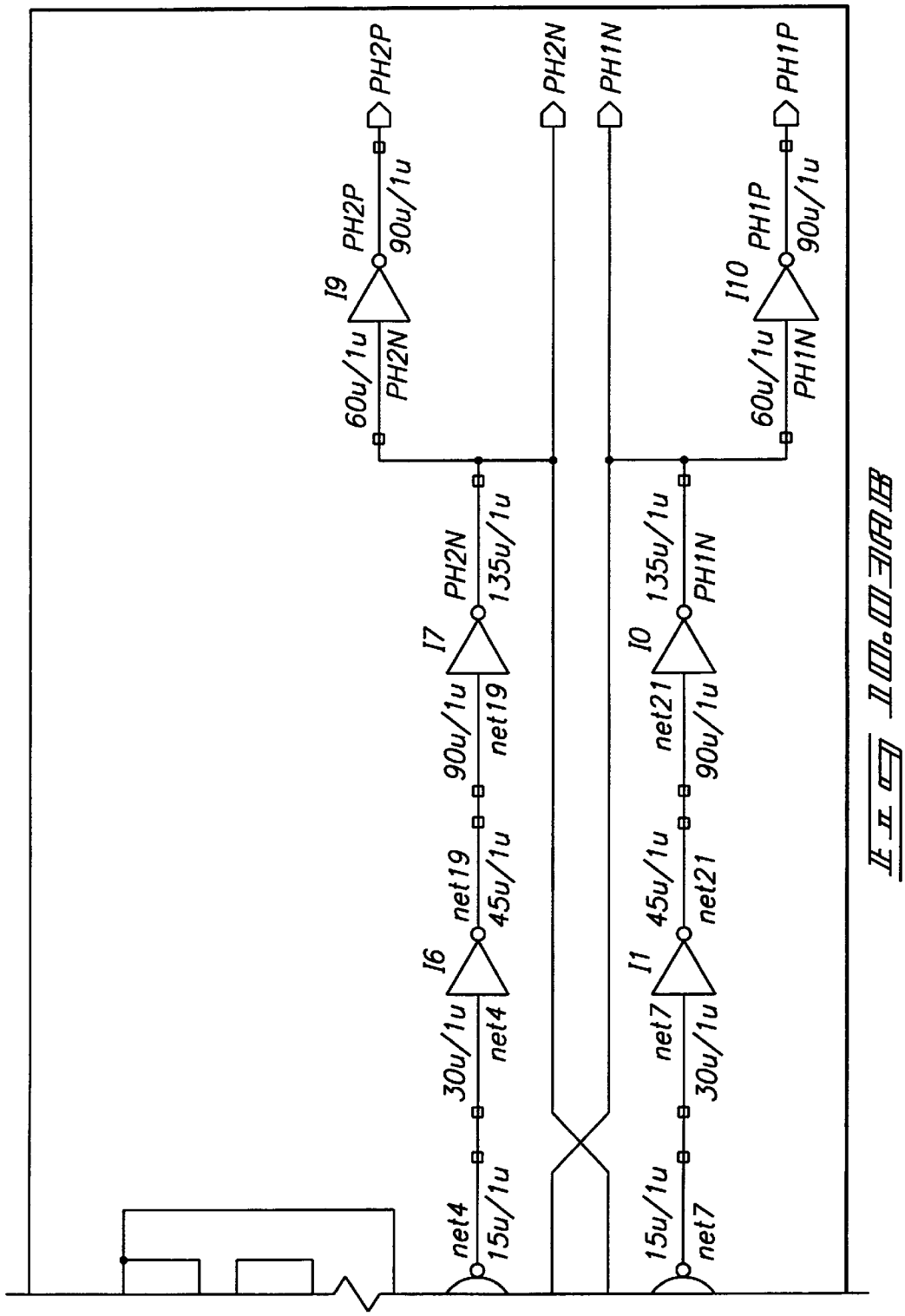


FIG. 1100.003A/B

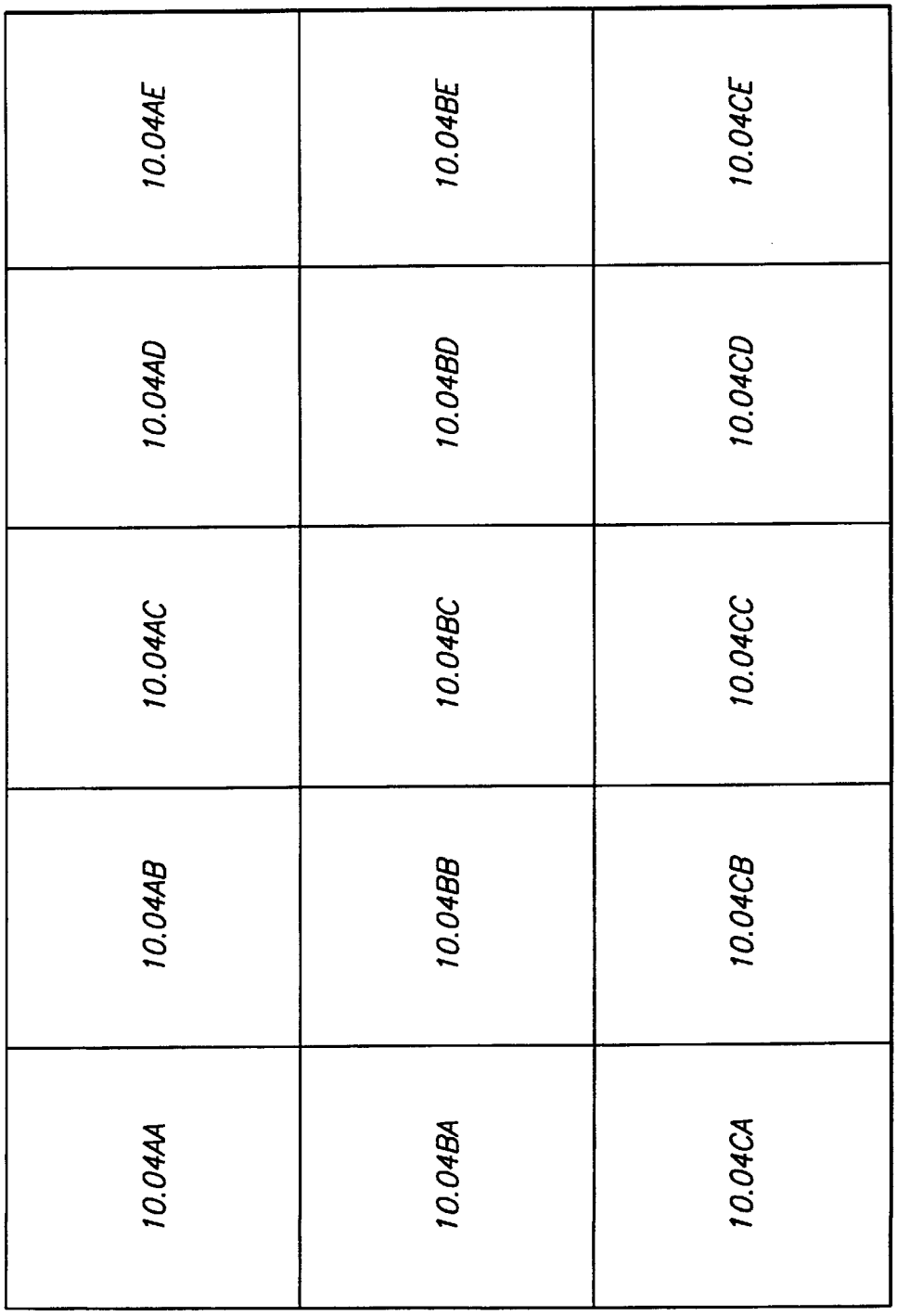

10.04AE
10.04BE
10.04CE
10.04AD
10.04BD
10.04CD
10.04AC
10.04BC
10.04CC
10.04AB
10.04BB
10.04CB
10.04AA
10.04BA
10.04CA

FIG 100.04

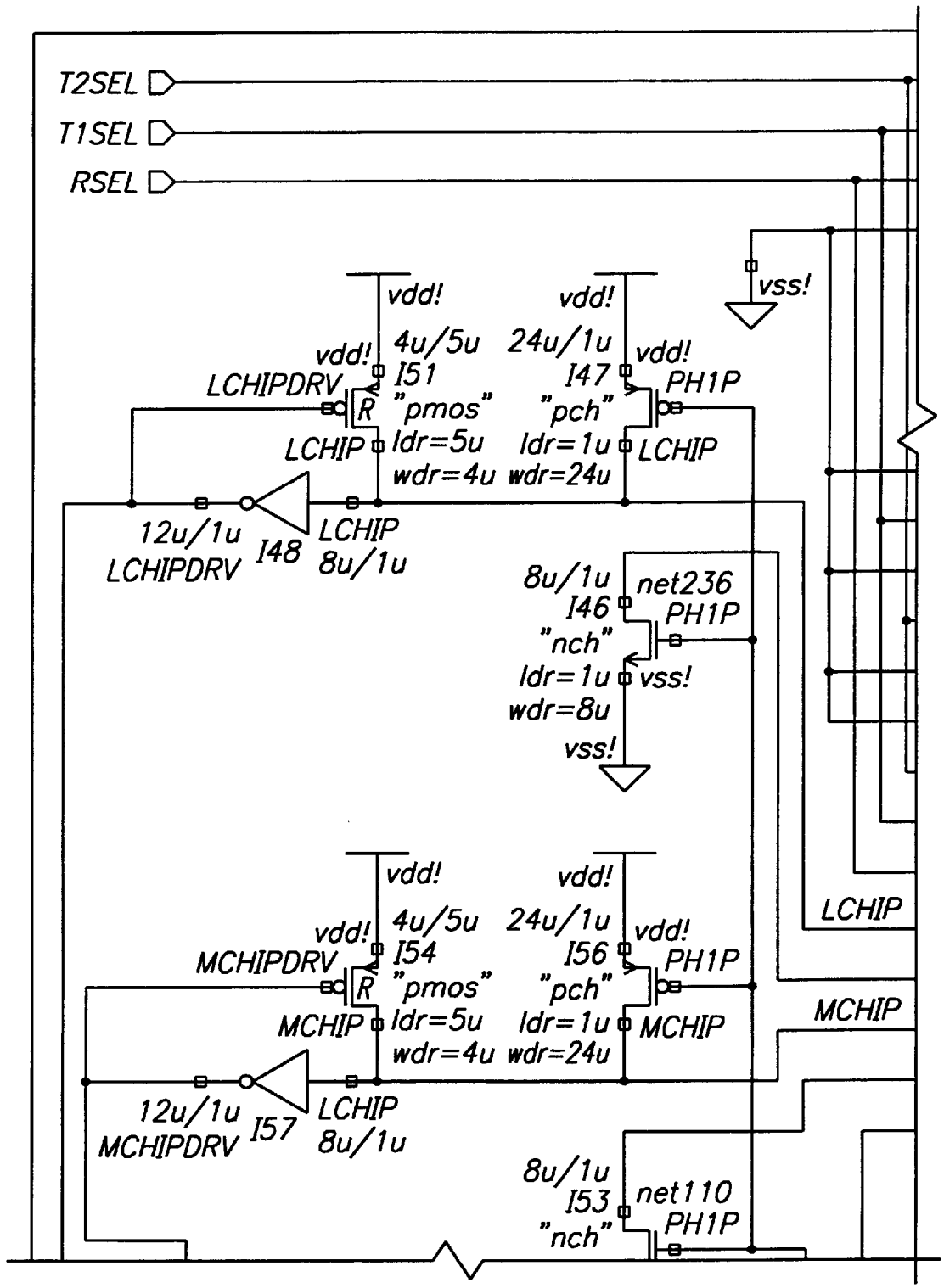

T2SEL
T1SEL
RSEL
vss!
vdd!
vdd!
4u/5u
24u/1u
vdd!
LCHIPDRV
I51
I47
PH1P
R
"pmos"
"pch"
LCHIP
ldr=5u
ldr=1u
LCHIP
wdr=4u
wdr=24u
12u/1u
LCHIPDRV
I48
LCHIP
8u/1u
8u/1u
net236
I46
PH1P
"nch"
ldr=1u
vss!
wdr=8u
vss!
LCHIP
MCHIPDRV
I54
I56
MCHIP
MCHIP
12u/1u
MCHIPDRV
I57
8u/1u
net110
I53
"nch"

Fig 10.04AA

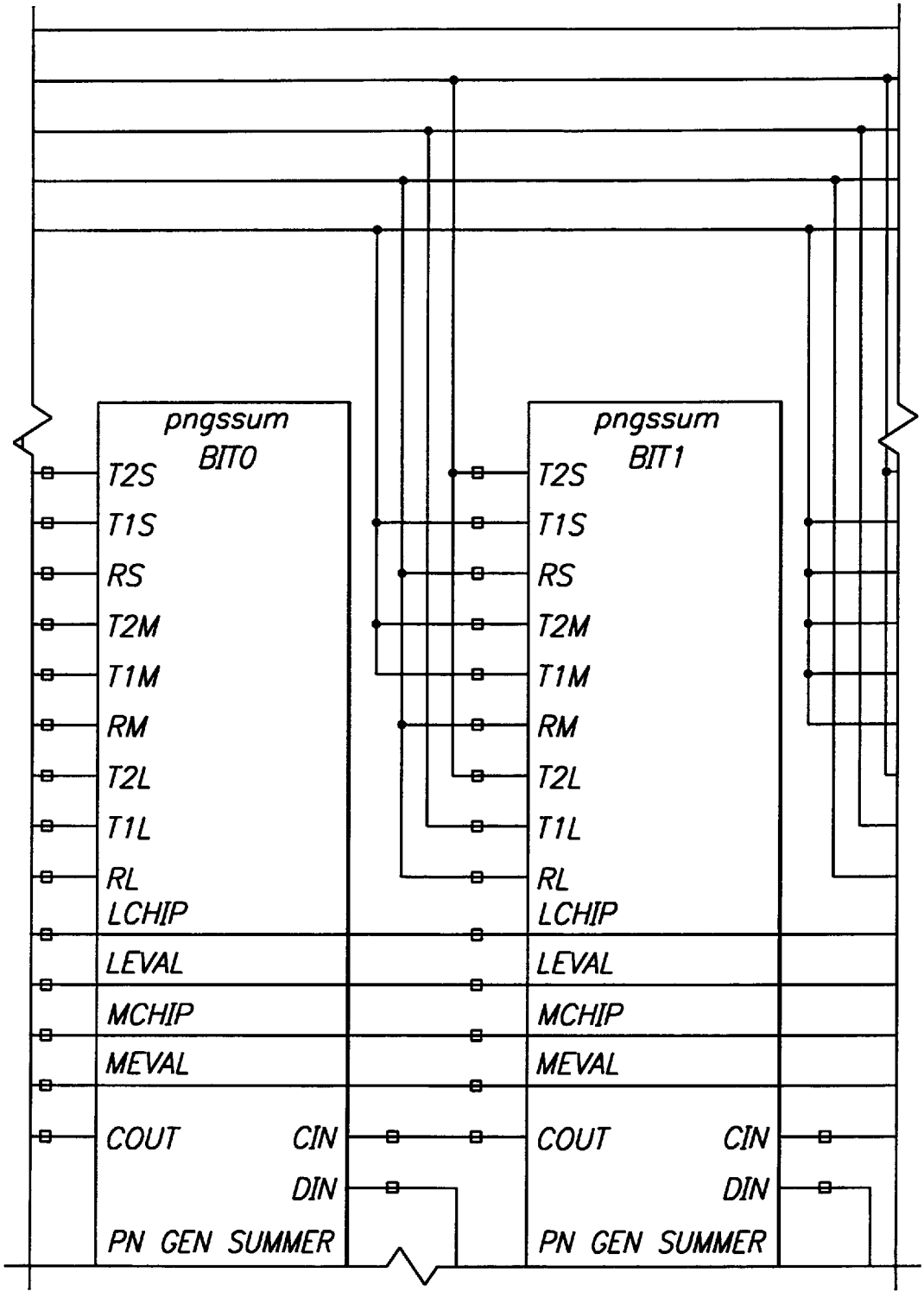

pngssum
BIT0
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER
pngssum
BIT1
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER

Fig 10.04AB

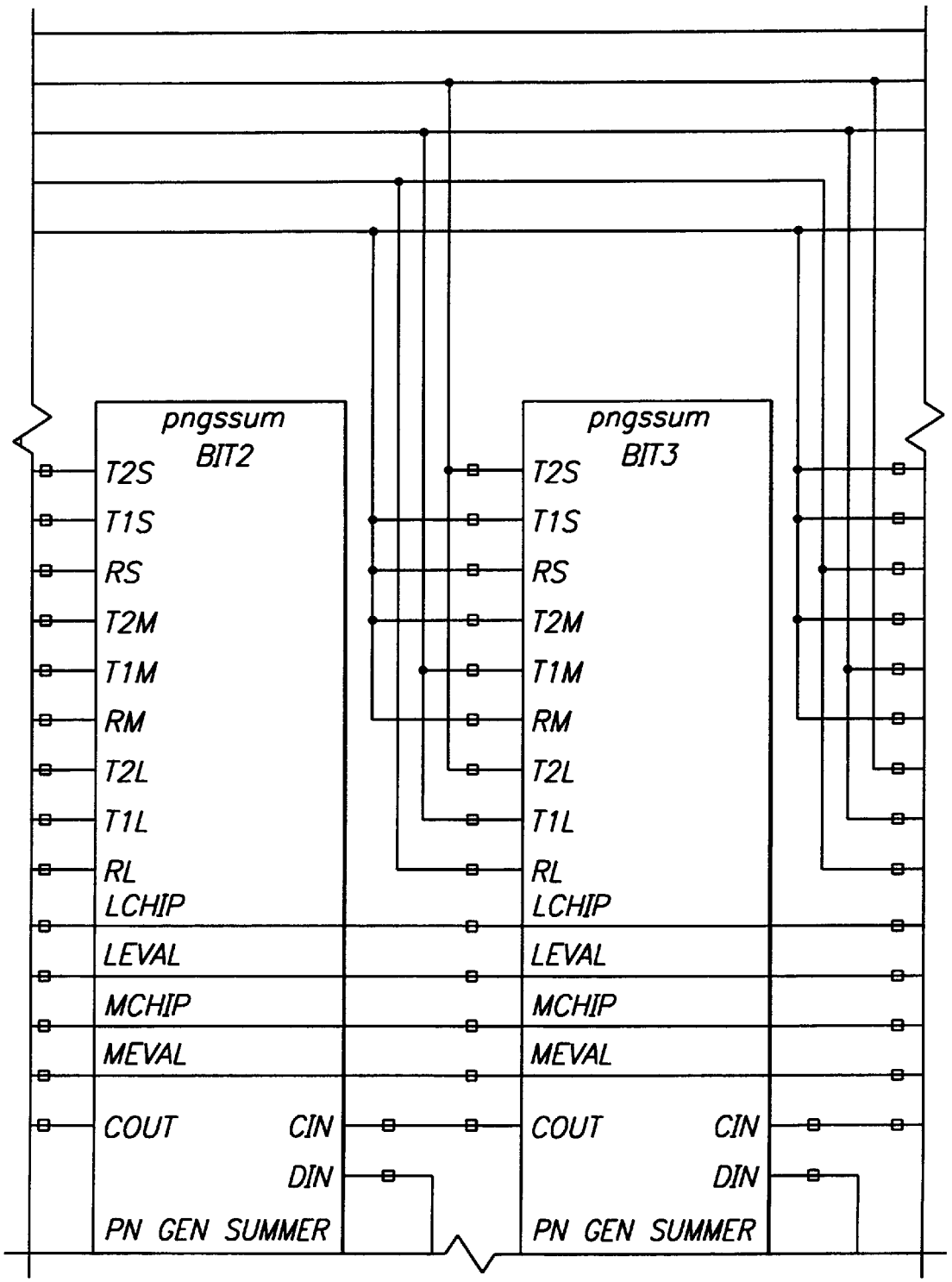

pngssum
BIT2
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER
pngssum
BIT3
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER

Fig 10.04AC

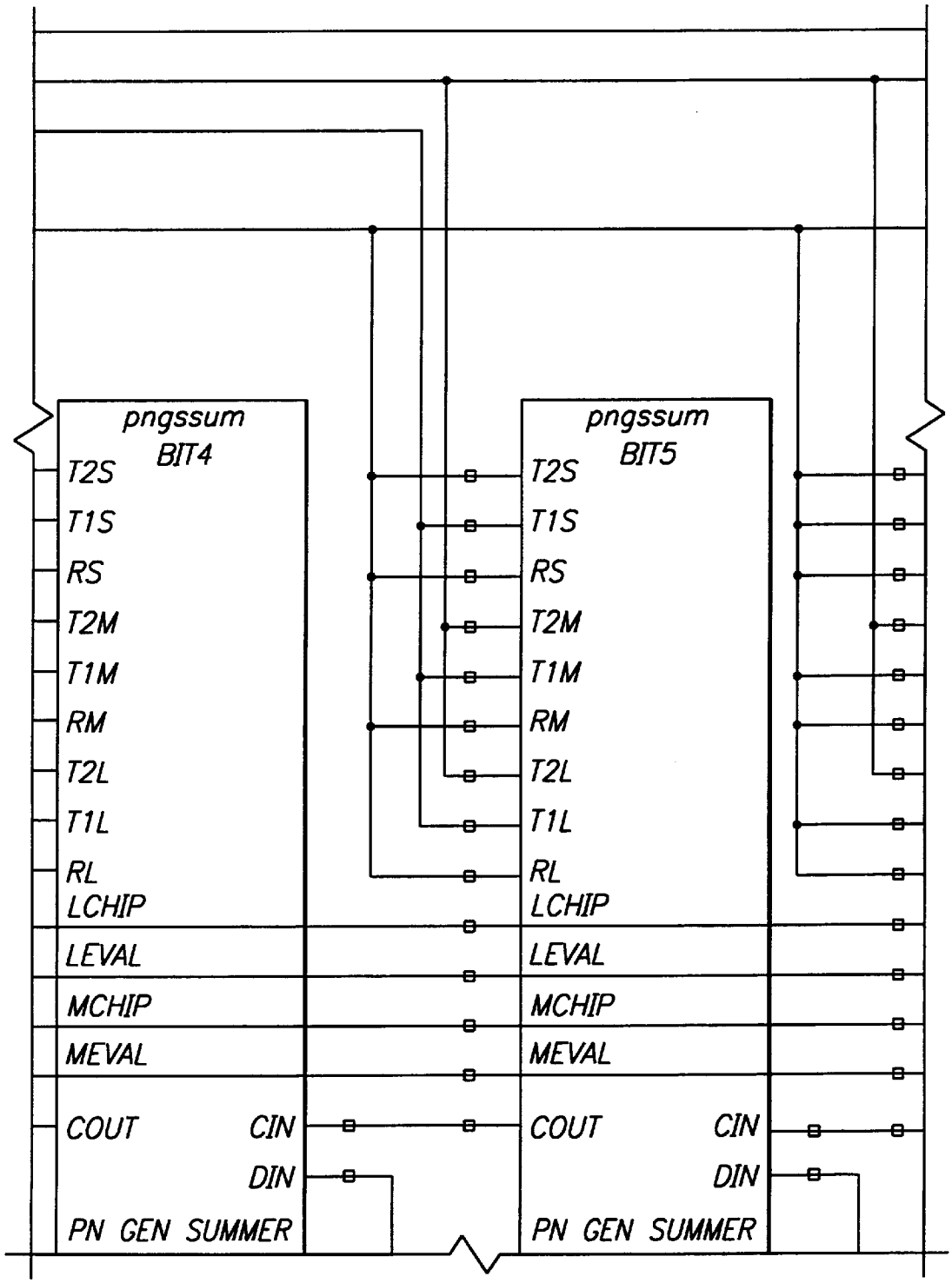

pngssum
BIT4
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER
pngssum
BIT5
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER

Fig 10.0+AD

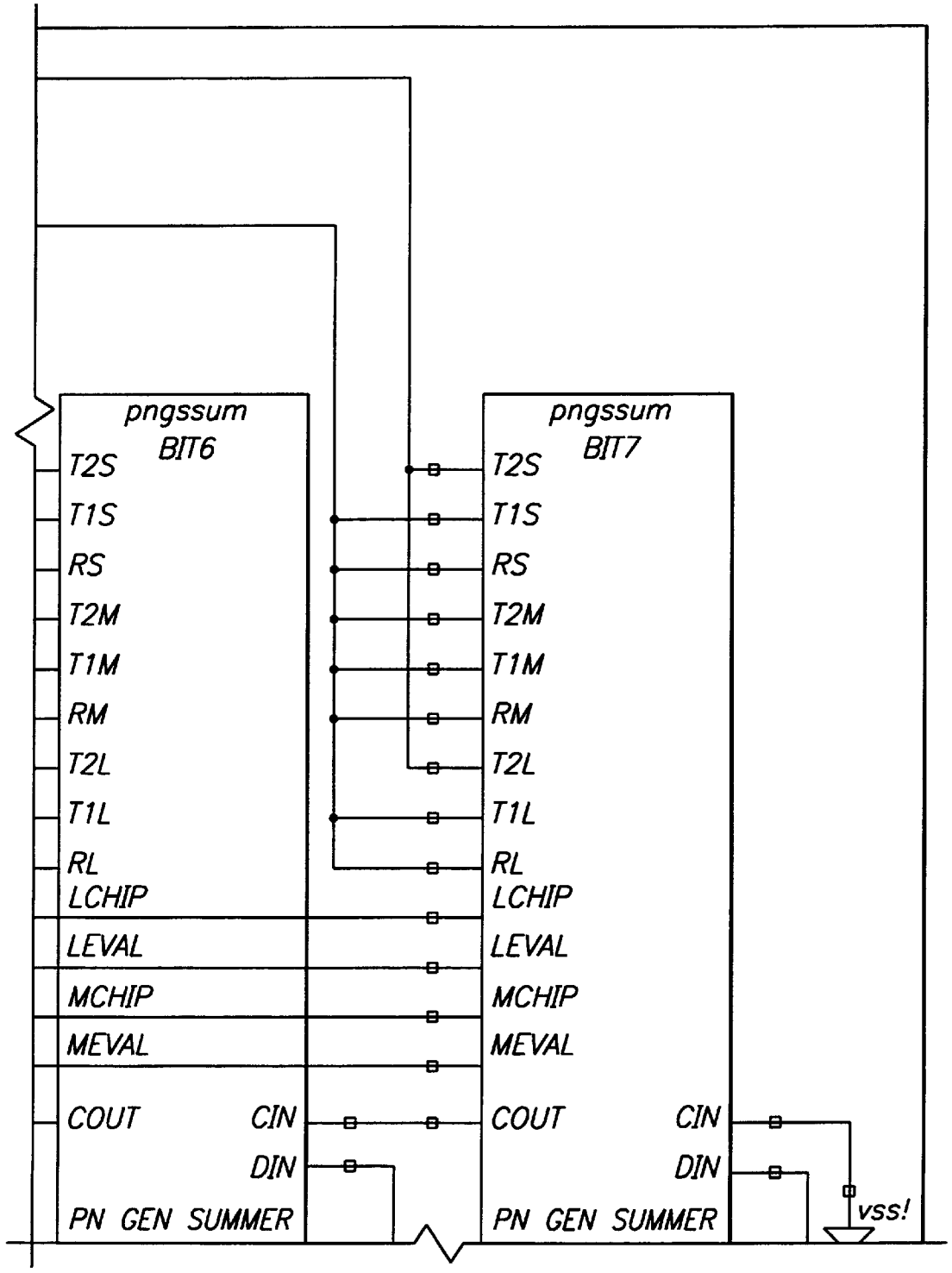

pngssum
BIT6
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER
pngssum
BIT7
T2S
T1S
RS
T2M
T1M
RM
T2L
T1L
RL
LCHIP
LEVAL
MCHIP
MEVAL
COUT
CIN
DIN
PN GEN SUMMER
vss!

Fig 1004AE

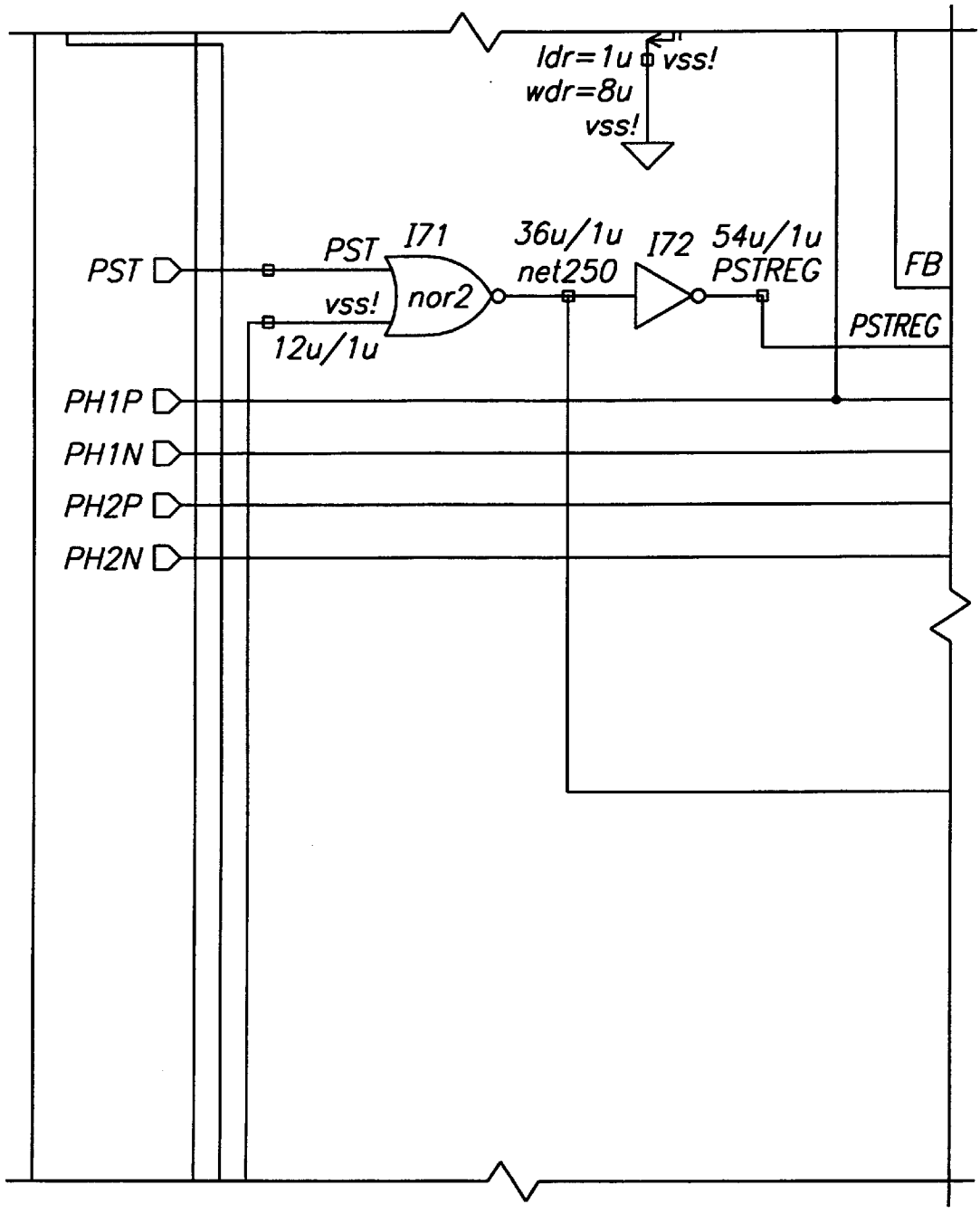

ldr=1u
wdr=8u
vss!
vss!
PST
PST
I71
vss!
nor2
12u/1u
36u/1u
net250
I72
54u/1u
PSTREG
FB
PSTREG
PH1P
PH1N
PH2P
PH2N

Fig 10.04BA

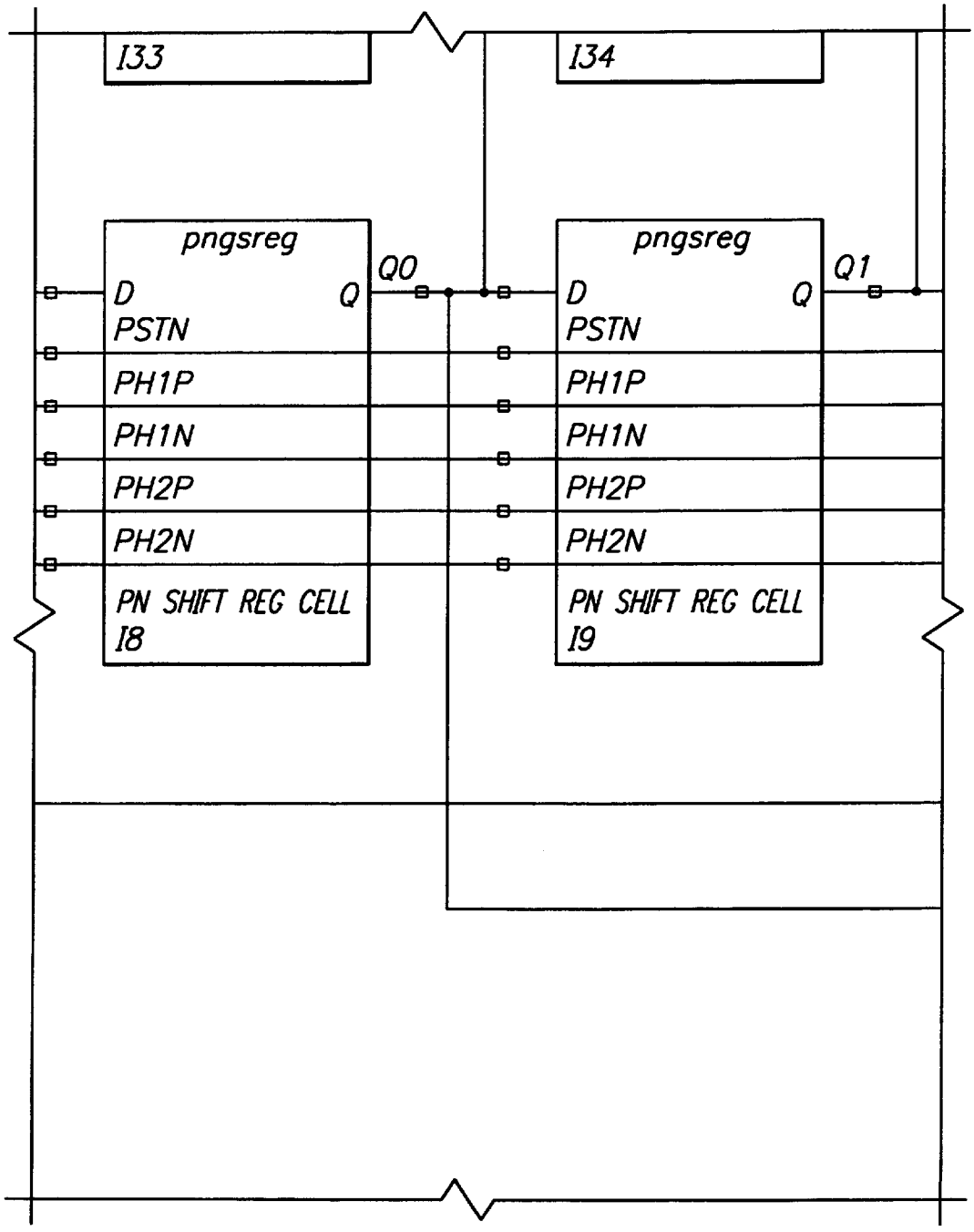


Fig 100.0418B

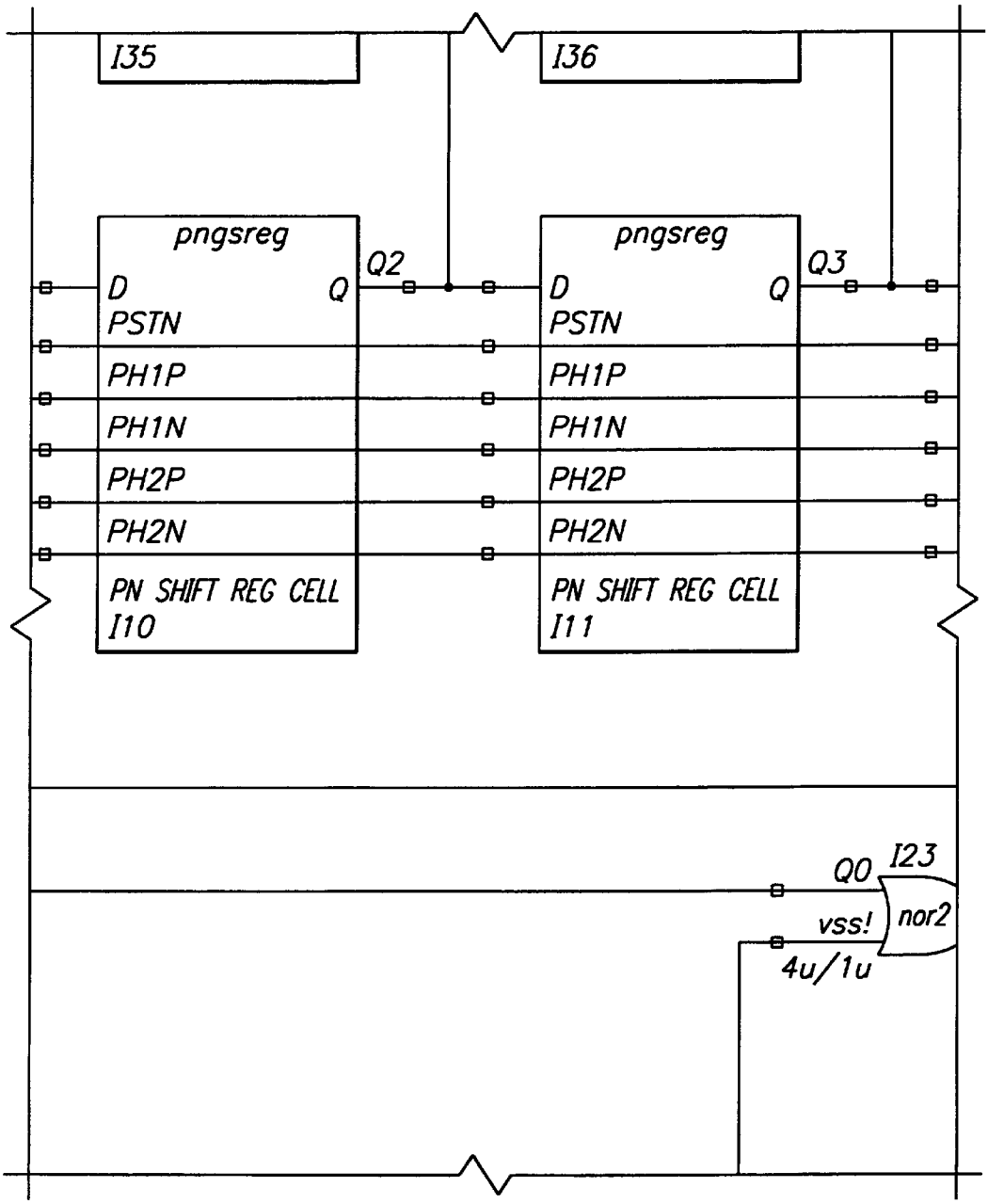

I35
I36
pngsreg
D
Q
Q2
PSTN
PH1P
PH1N
PH2P
PH2N
PN SHIFT REG CELL
I10
pngsreg
D
Q
Q3
PSTN
PH1P
PH1N
PH2P
PH2N
PN SHIFT REG CELL
I11
Q0
I23
vss!
nor2
4u/1u

Fig 10.04BC

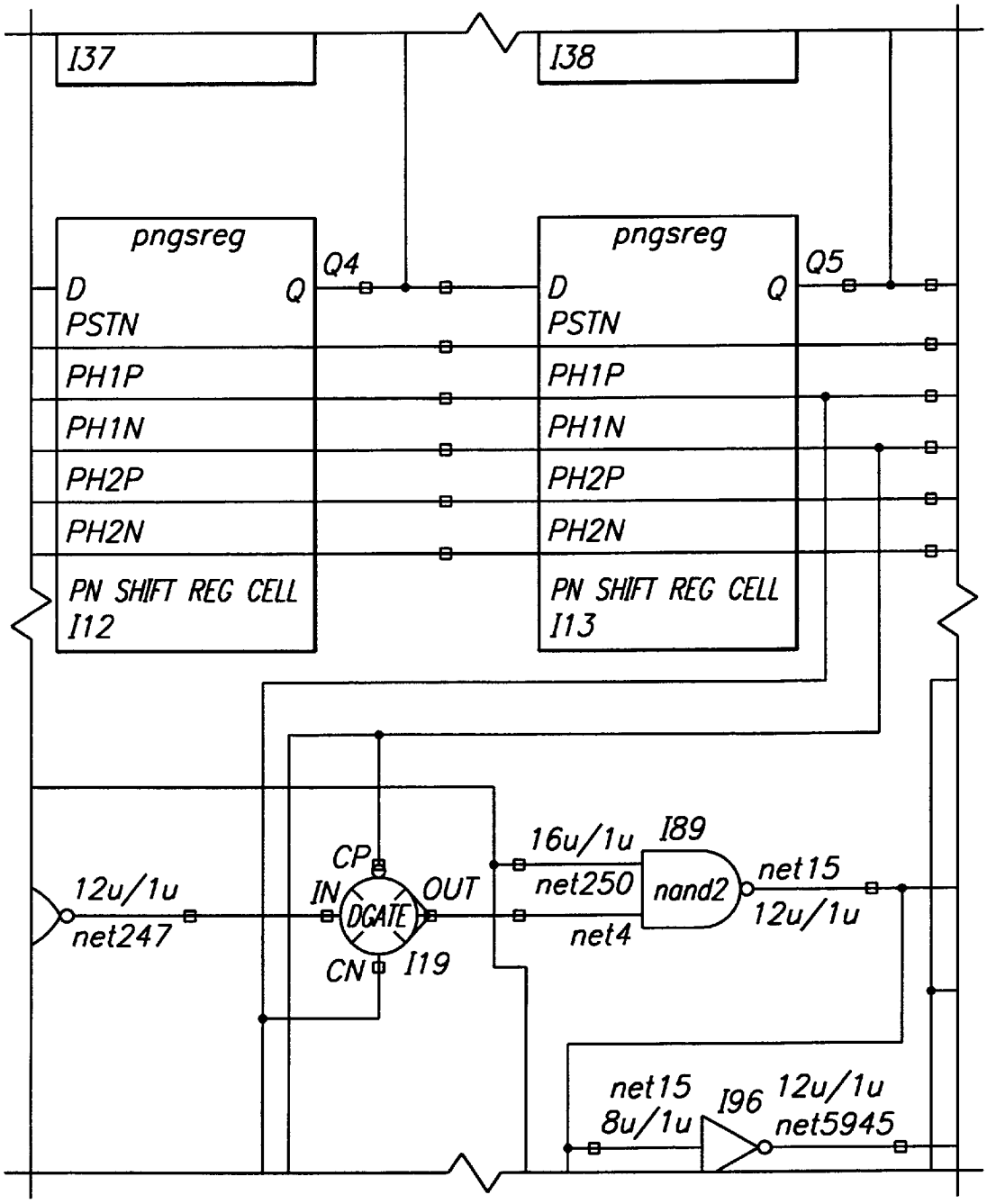


Fig 100.00-A1BD

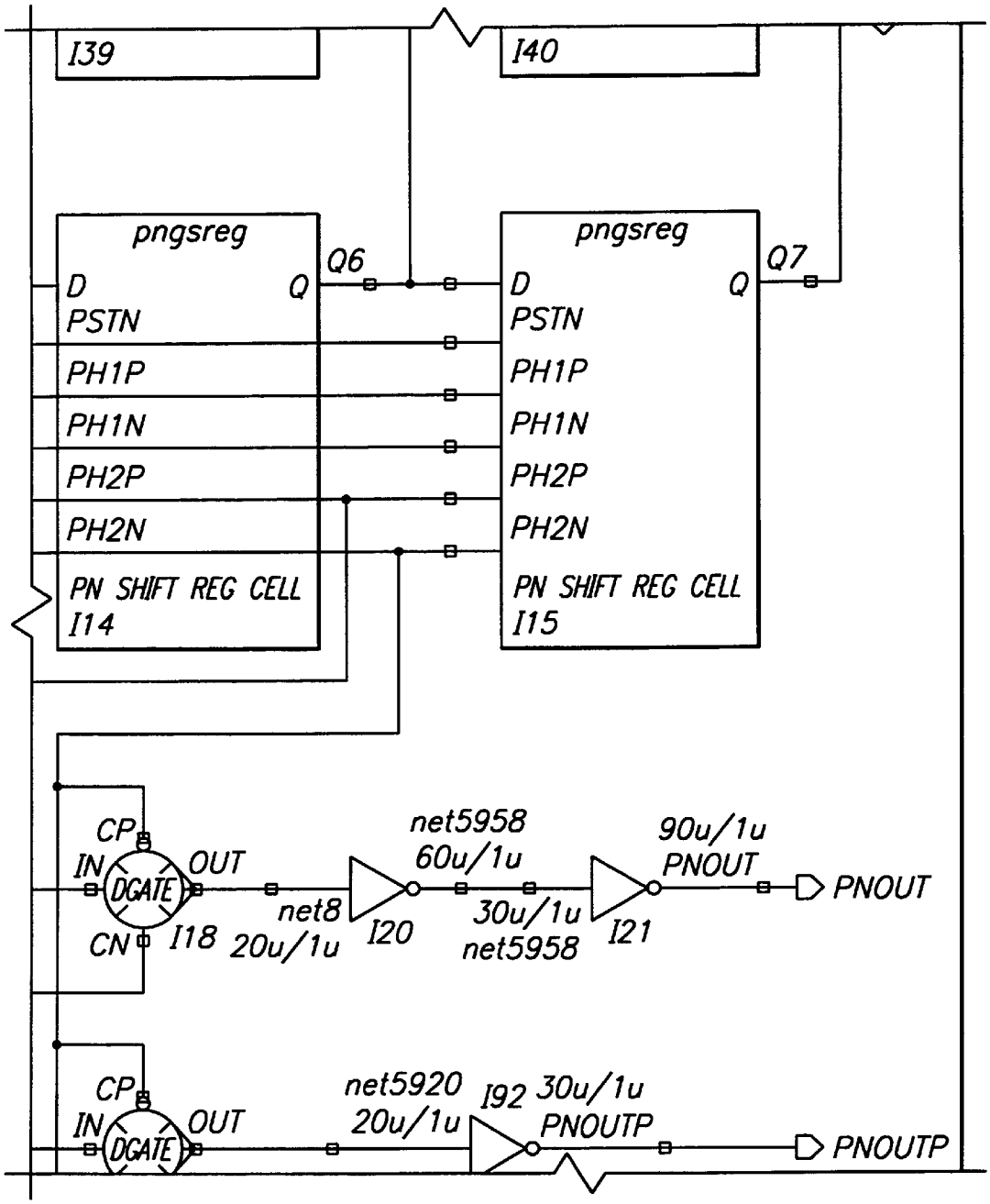

I39
I40
pngsreg
D
Q
PSTN
PH1P
PH1N
PH2P
PH2N
PN SHIFT REG CELL
I14
Q6
pngsreg
D
Q
PSTN
PH1P
PH1N
PH2P
PH2N
PN SHIFT REG CELL
I15
Q7
CP
IN
OUT
DGATE
CN
I18
net8
20u/1u
I20
net5958
60u/1u
30u/1u
net5958
I21
90u/1u
PNOUT
PNOUT
CP
IN
OUT
DGATE
net5920
20u/1u
I92
30u/1u
PNOUTP
PNOUTP

Fig 10.04BE

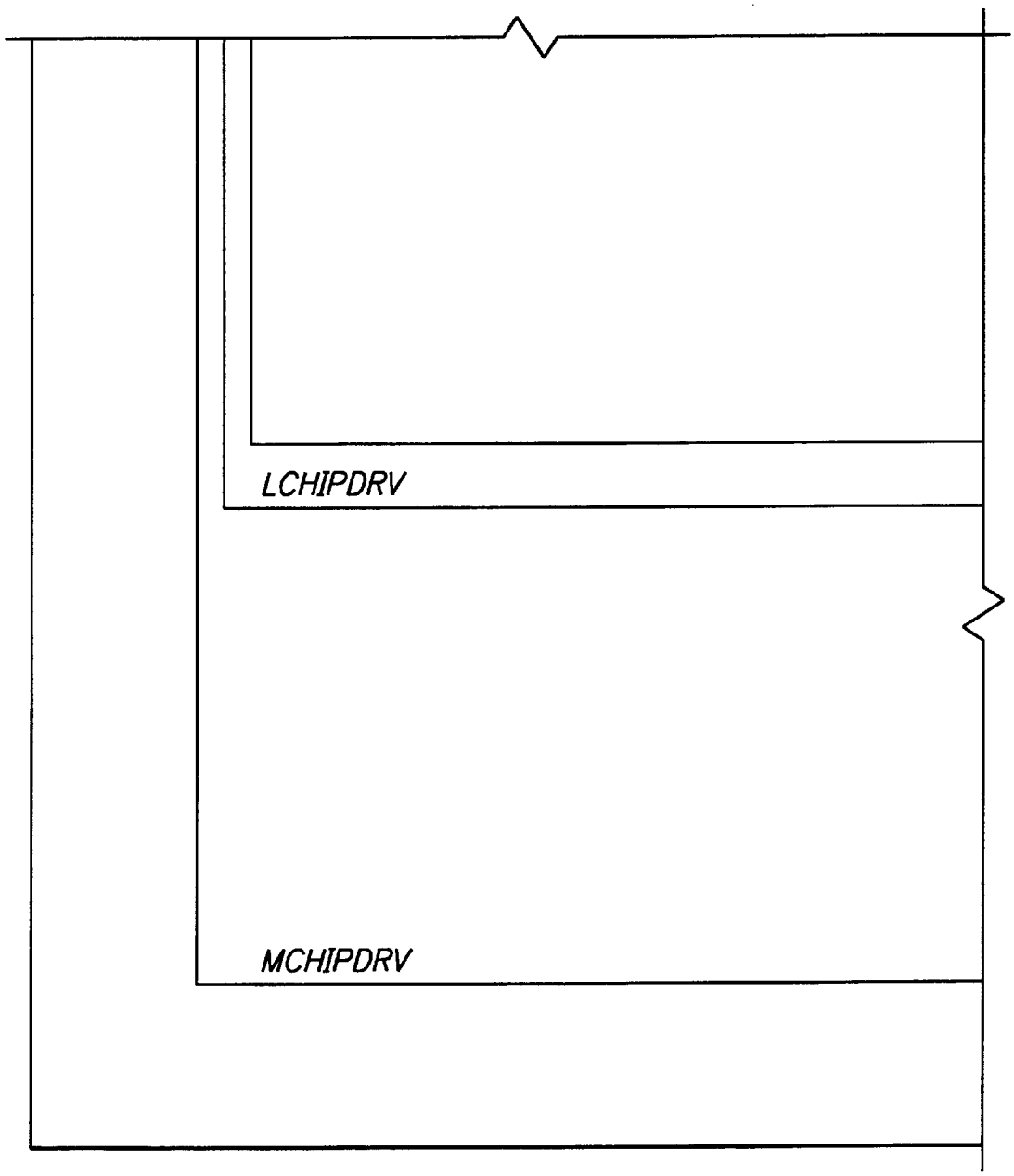


Fig 10.04CA

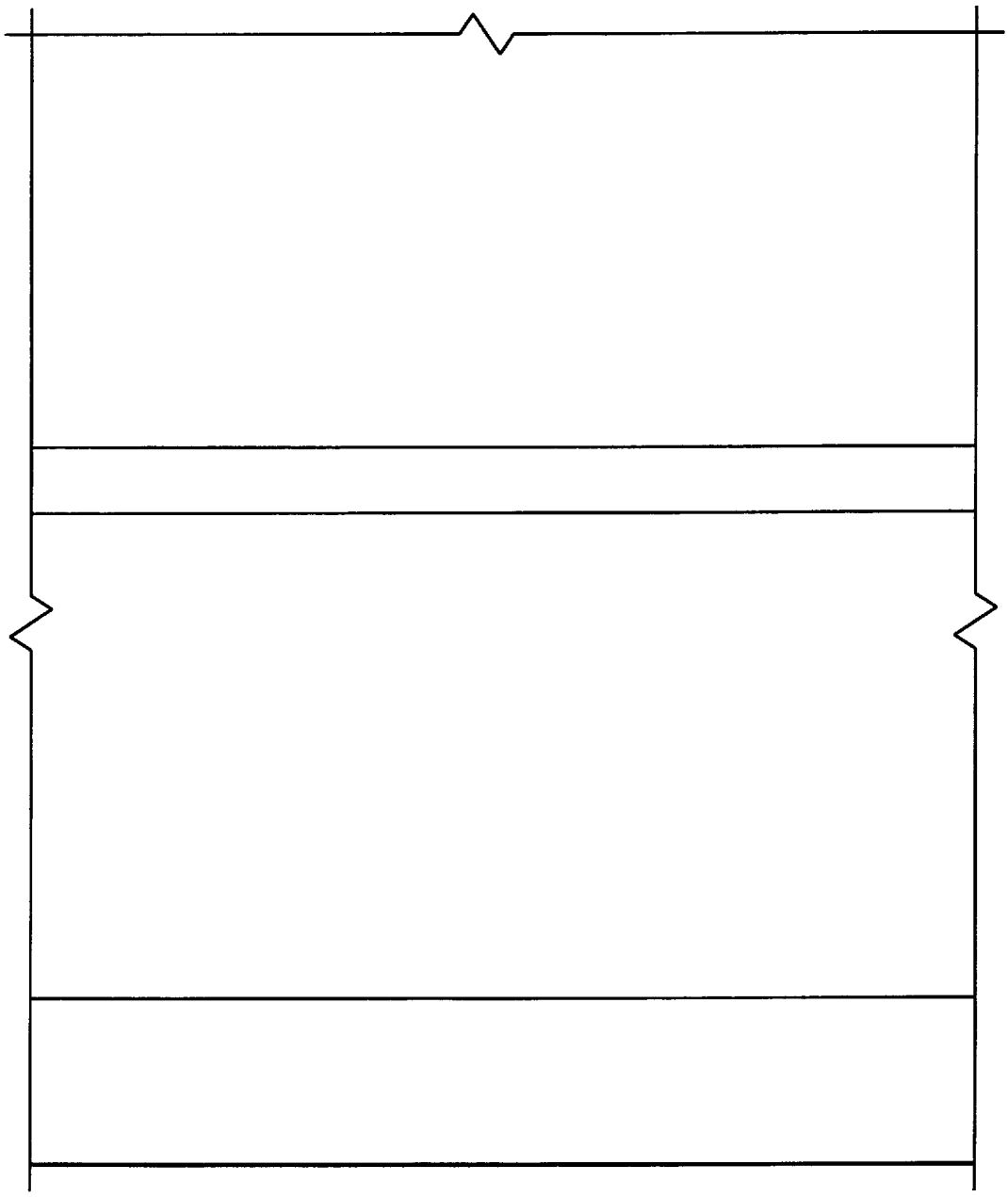


Fig 10.0454CB

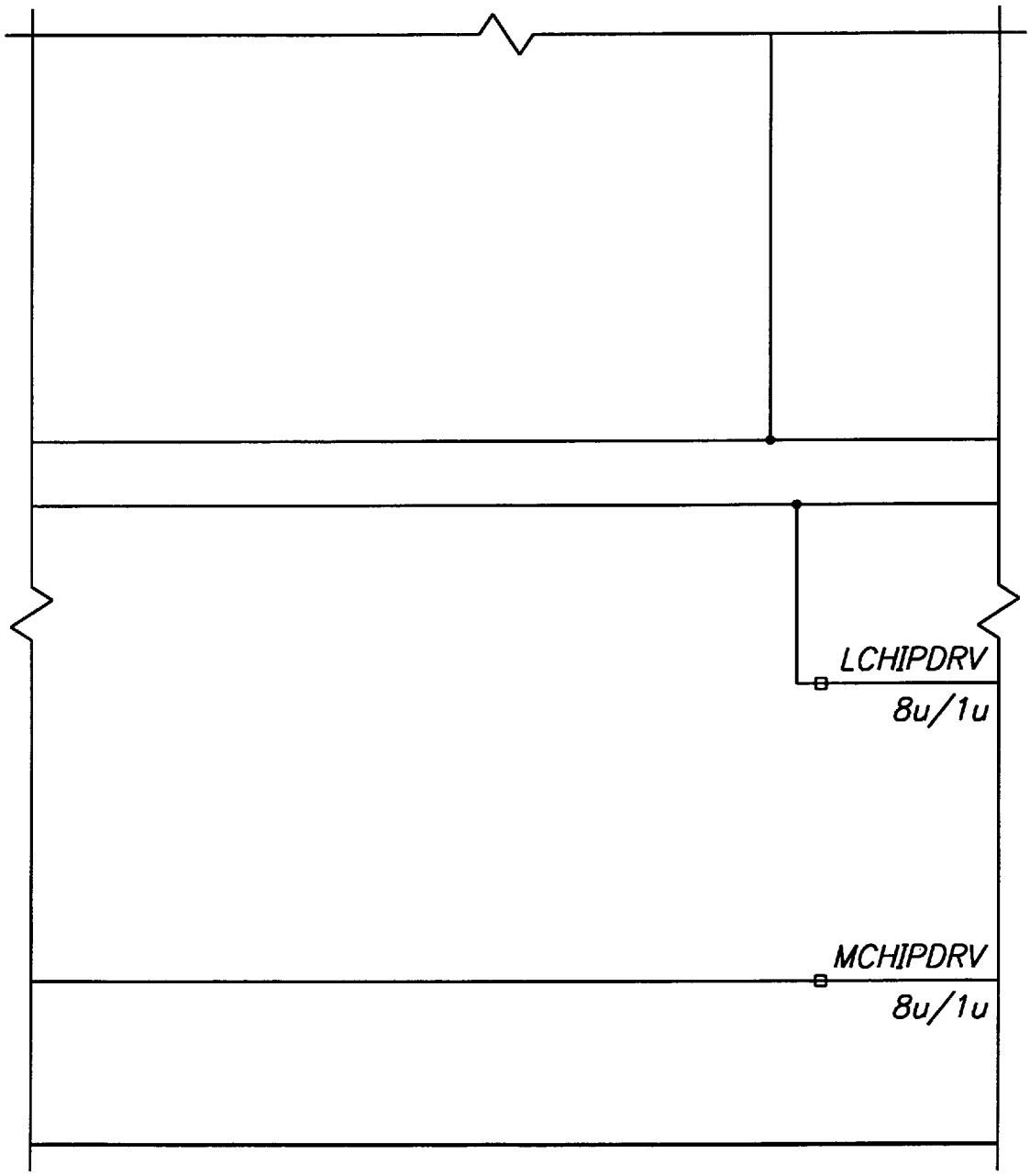


Fig 10.04CC

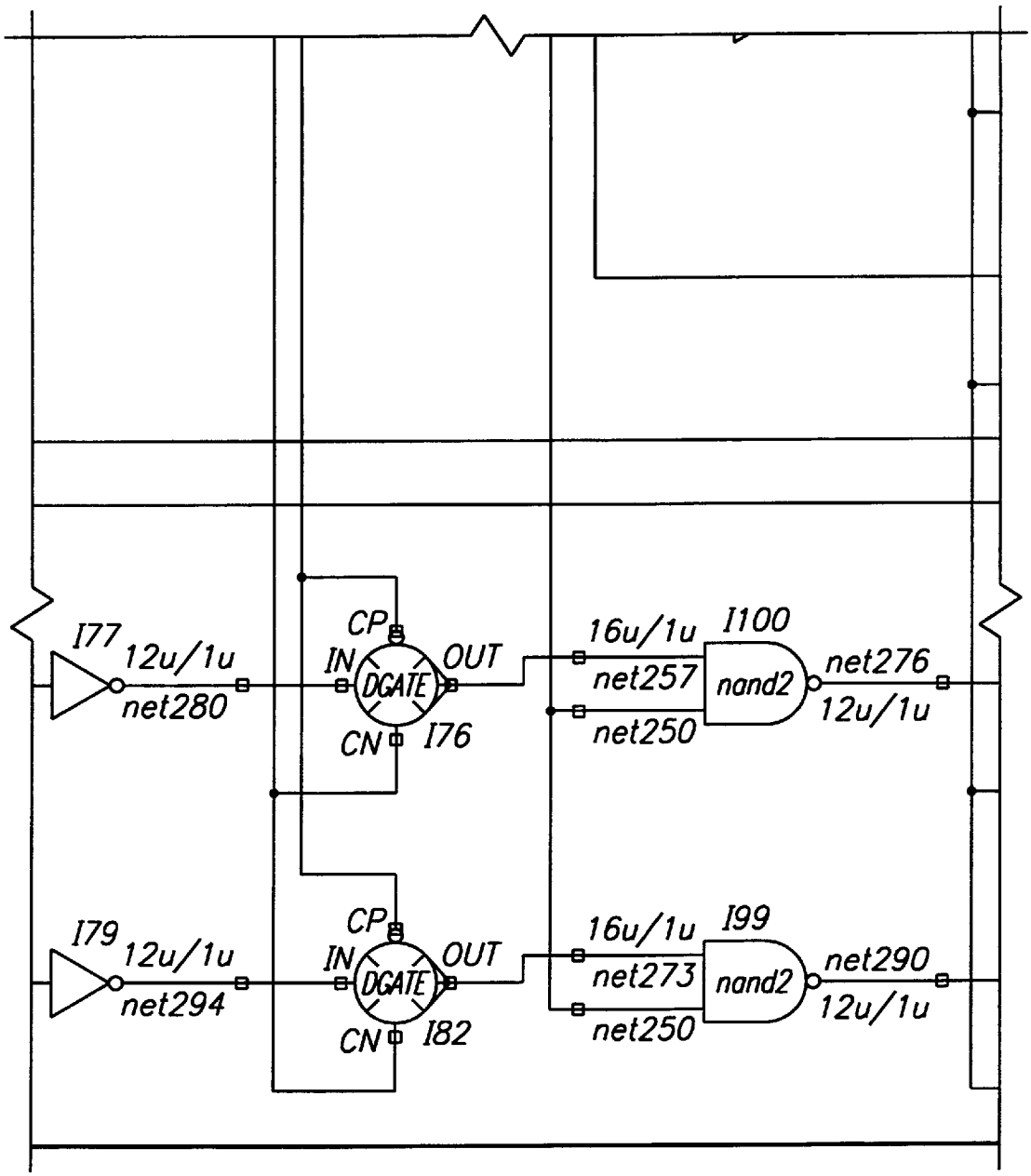


Fig 100.00-FIG

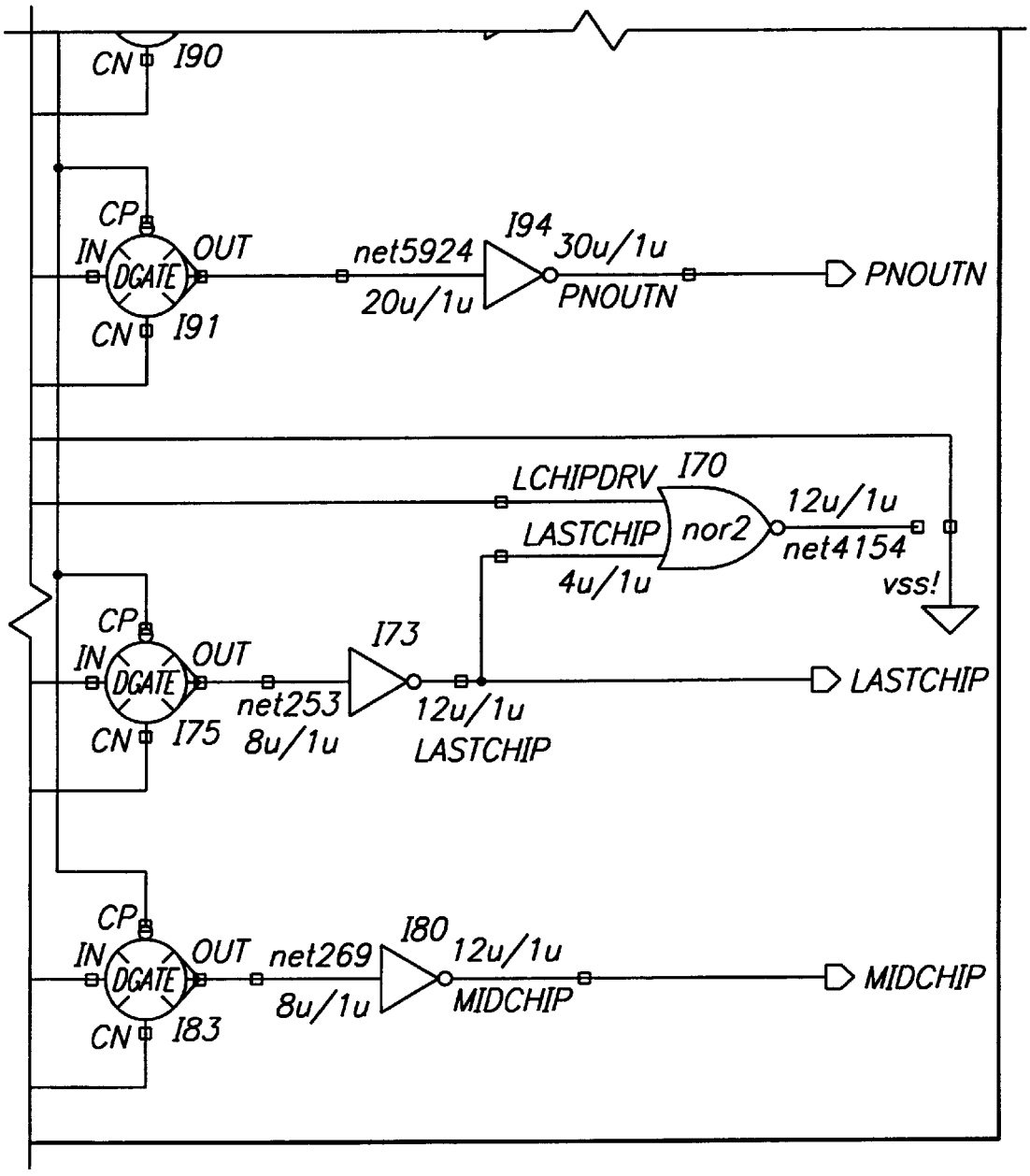


Fig 100.004CE

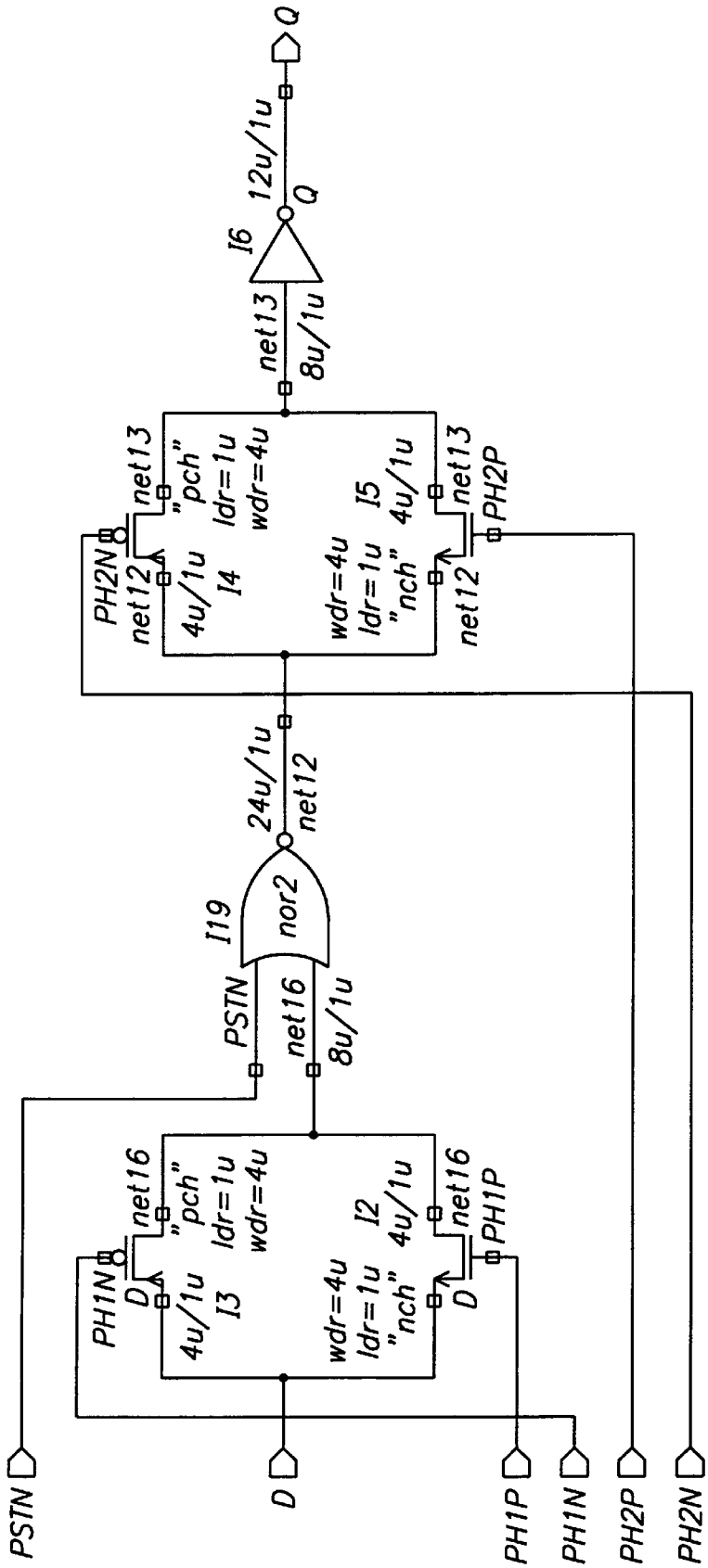

Q
12u/1u
I6
Q
net13
8u/1u
PH2N
net12
4u/1u
I4
net13
"pch"
ldr=1u
wdr=4u
wdr=4u
ldr=1u
"nch"
net12
I5
4u/1u
net13
PH2P
24u/1u
net12
I19
nor2
PSTN
net16
8u/1u
PH1N
D
4u/1u
I3
net16
"pch"
ldr=1u
wdr=4u
wdr=4u
ldr=1u
"nch"
D
I2
4u/1u
net16
PH1P
PSTN
D
PH1P
PH1N
PH2P
PH2N

FIG 11

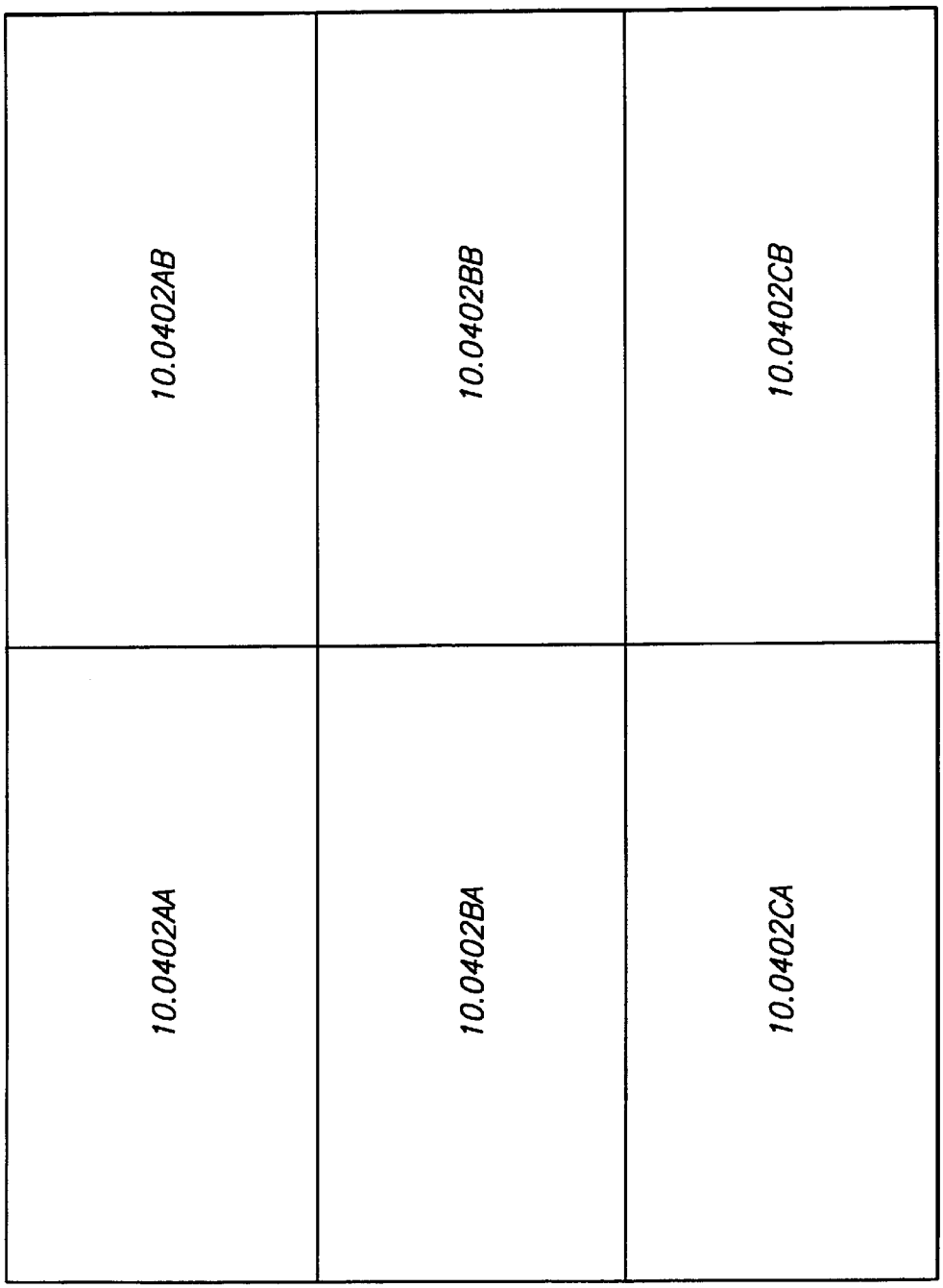


FIG 10,004,002

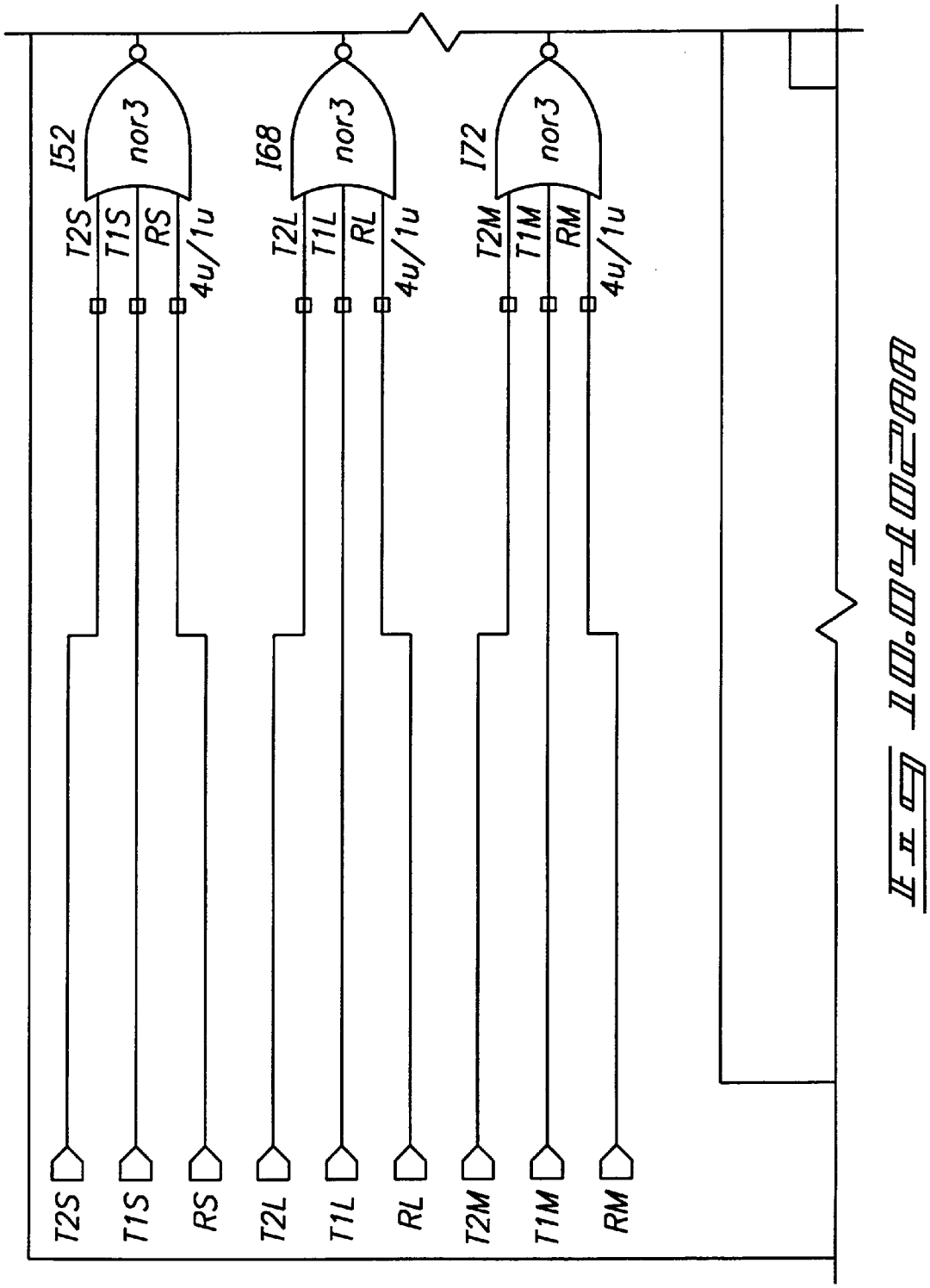

I52
nor3
T2S
T1S
RS
4u/1u
I68
nor3
T2L
T1L
RL
4u/1u
I72
nor3
T2M
T1M
RM
4u/1u
T2S
T1S
RS
T2L
T1L
RL
T2M
T1M
RM

FIG 1007

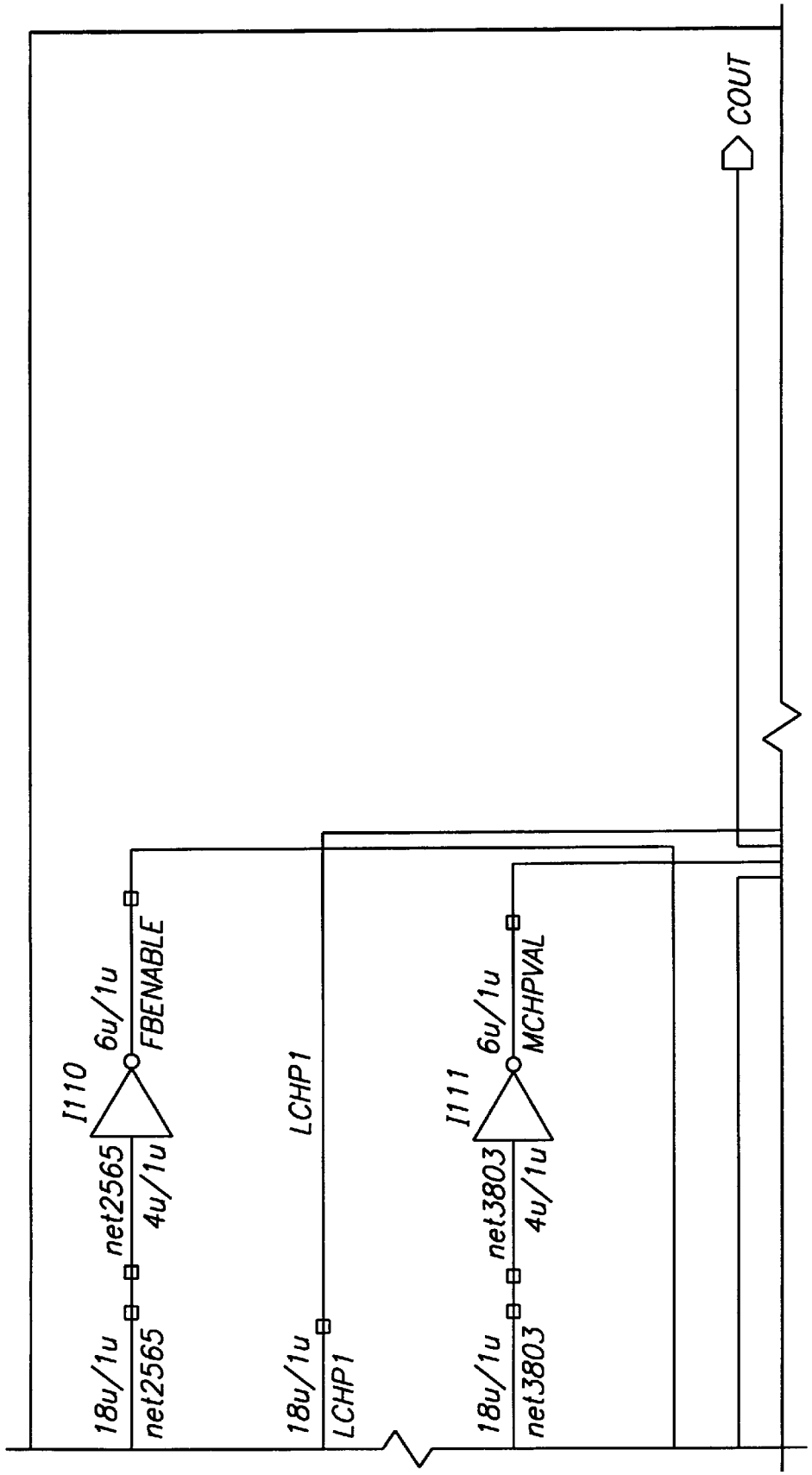


FIG 110,047,028

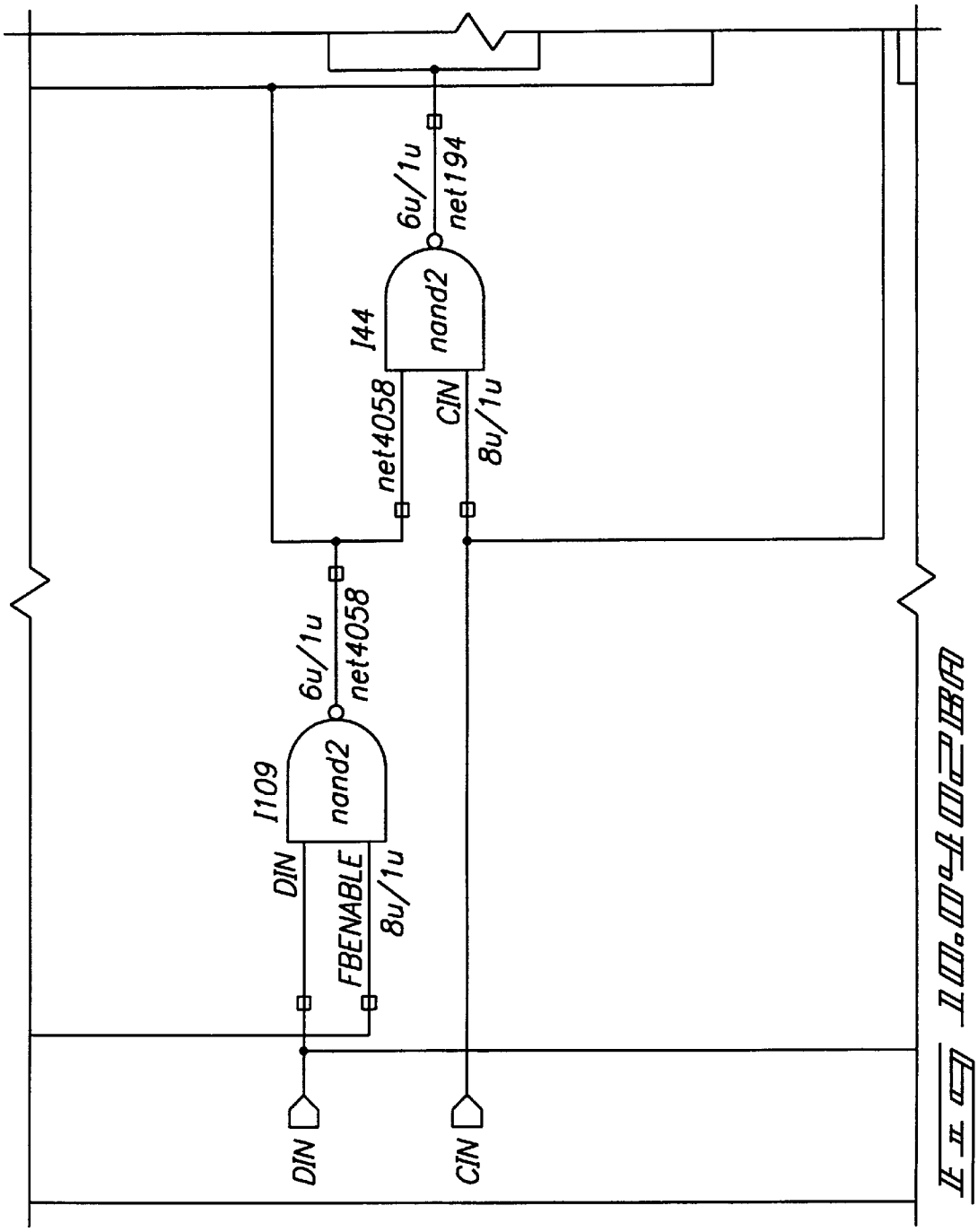
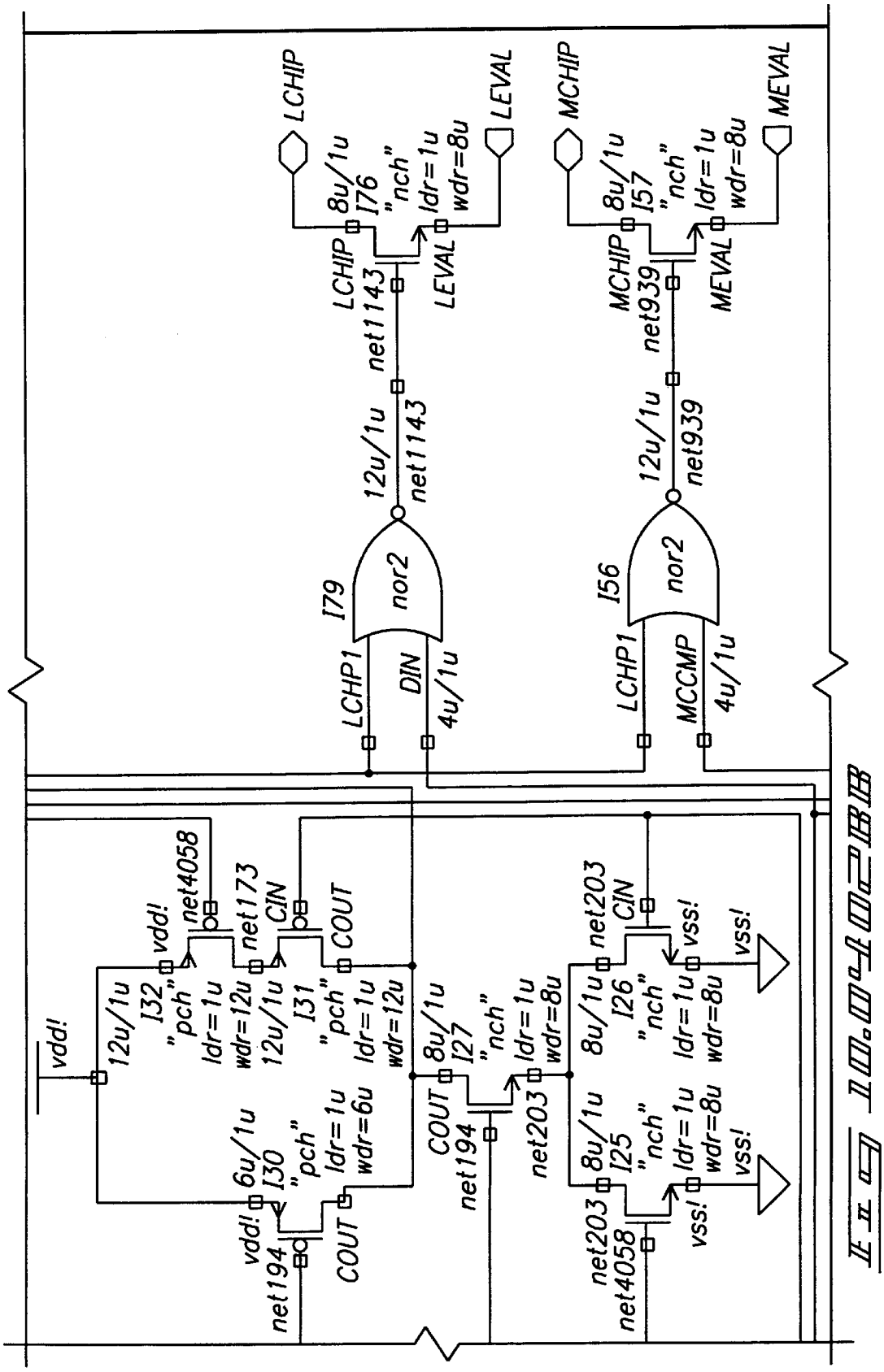
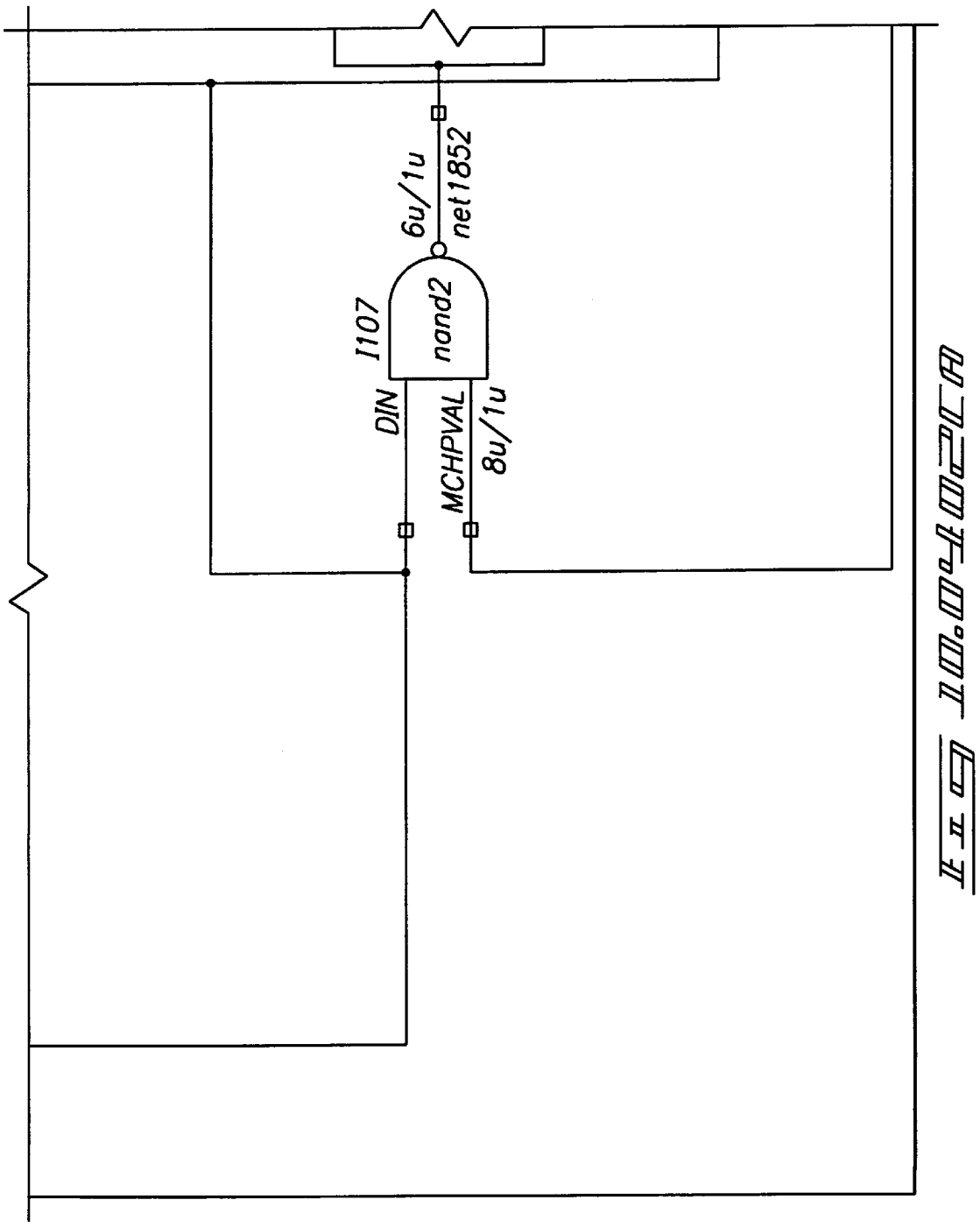


FIG 1100.0042BA


LCHIP
8u/1u
I76
"nch"
ldr=1u
wdr=8u
LEVAL
LCHIP
net1143
LEVAL
MCHIP
8u/1u
I57
"nch"
ldr=1u
wdr=8u
MEVAL
MCHIP
net939
MEVAL
12u/1u
net1143
12u/1u
net939
I79
nor2
I56
nor2
LCHP1
DIN
4u/1u
LCHP1
MCCMP
4u/1u
vdd!
12u/1u
I32
"pch"
ldr=1u
wdr=12u
vdd!
net4058
net173
CIN
12u/1u
I31
"pch"
ldr=1u
wdr=12u
COUT
6u/1u
I30
"pch"
ldr=1u
wdr=6u
vdd!
net194
COUT
8u/1u
I27
"nch"
ldr=1u
wdr=8u
COUT
net194
net203
8u/1u
I26
"nch"
ldr=1u
wdr=8u
net203
CIN
vss!
vss!
8u/1u
I25
"nch"
ldr=1u
wdr=8u
vss!
net203
net4058
vss!


6u/1u
net1852
I107
nand2
DIN
MCHPVAL
8u/1u
FIG 400.00T

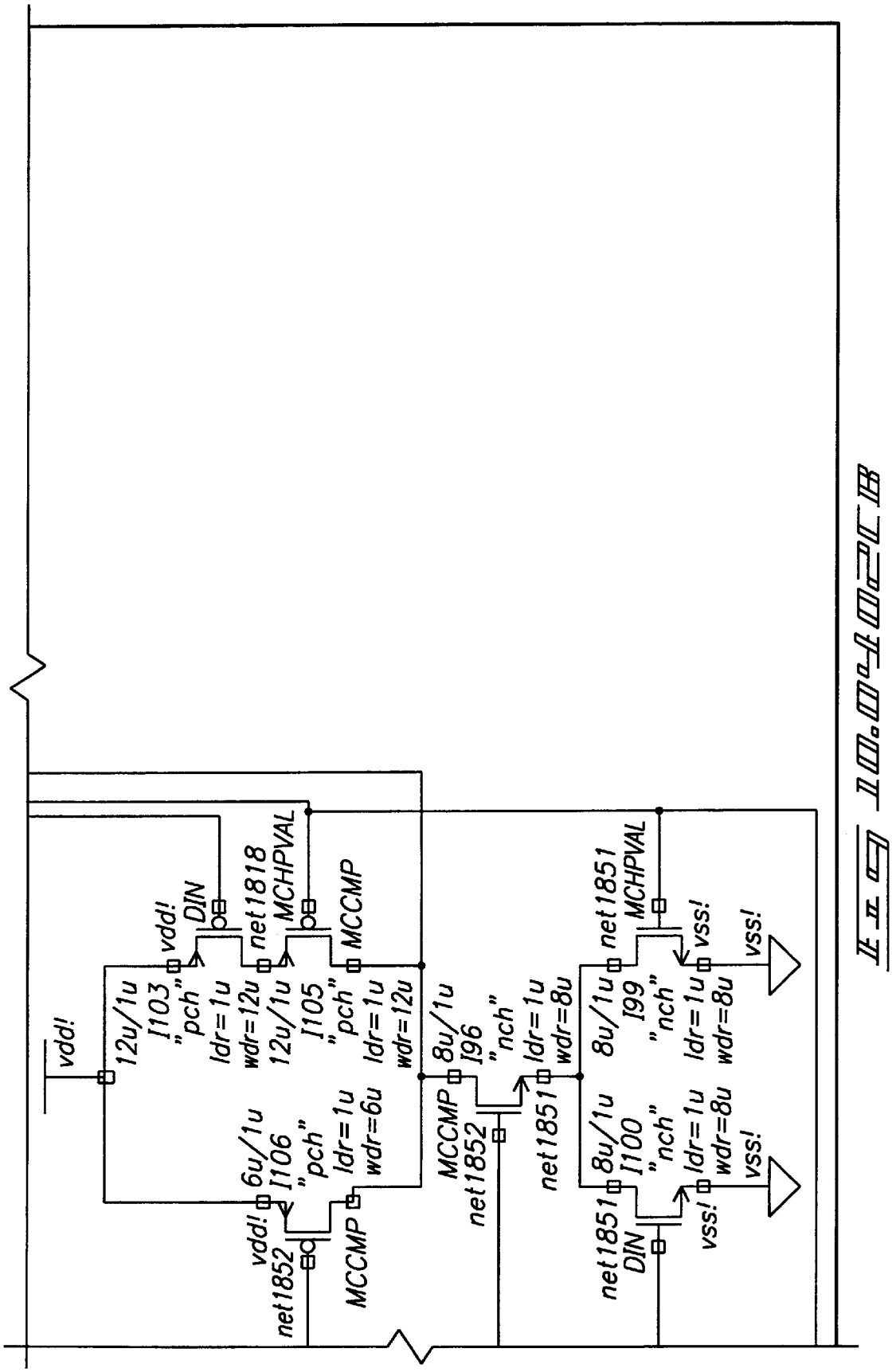

vdd!
12u/1u
I103
"pch"
ldr=1u
wdr=12u
vdd!
DIN
net1818
12u/1u
I105
"pch"
ldr=1u
wdr=12u
MCHPVAL
MCCMP
6u/1u
I106
"pch"
ldr=1u
wdr=6u
vdd!
net1852
MCCMP
MCCMP
net1852
8u/1u
I96
"nch"
ldr=1u
wdr=8u
net1851
8u/1u
I100
"nch"
ldr=1u
wdr=8u
net1851
DIN
vss!
8u/1u
I99
"nch"
ldr=1u
wdr=8u
net1851
MCHPVAL
vss!
vss!
vss!

FIG 100,004

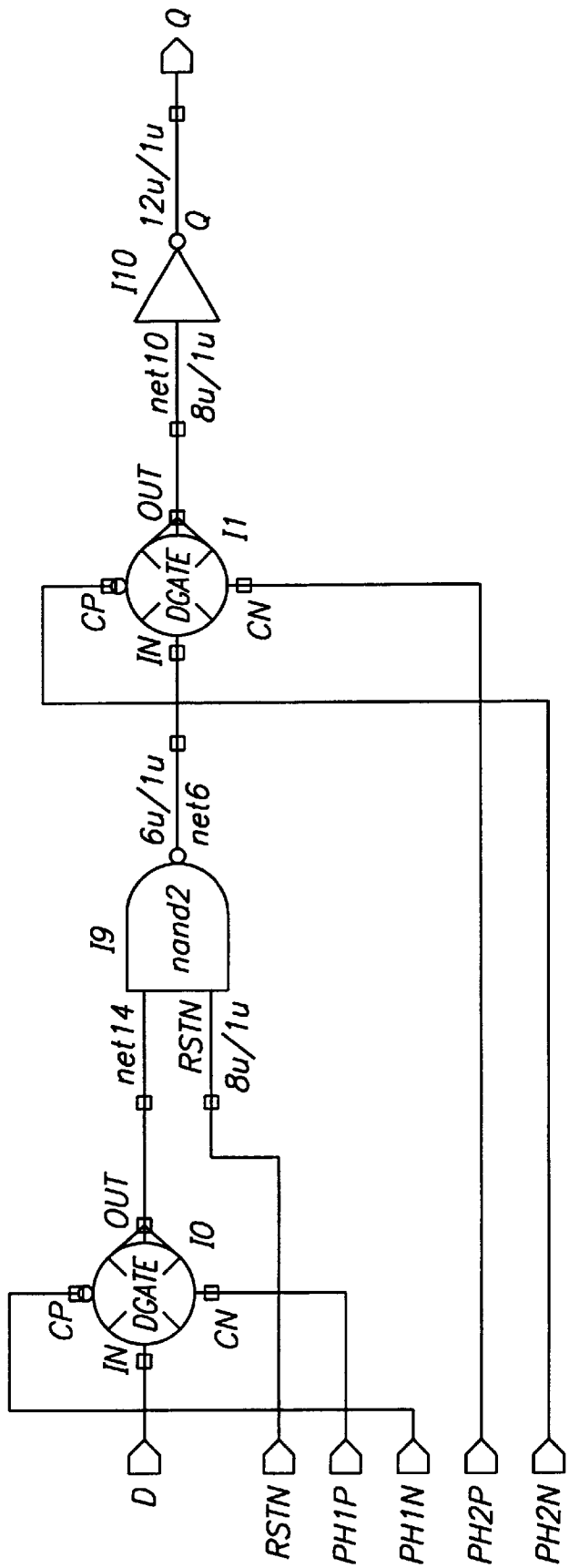

Q
12u/1u
Q
I10
net10
8u/1u
OUT
I1
CP
DGATE
CN
IN
6u/1u
net6
I9
nand2
net14
RSTN
8u/1u
OUT
I0
CP
DGATE
CN
IN
D
RSTN
PH1P
PH1N
PH2P
PH2N

FIG. 1100.005

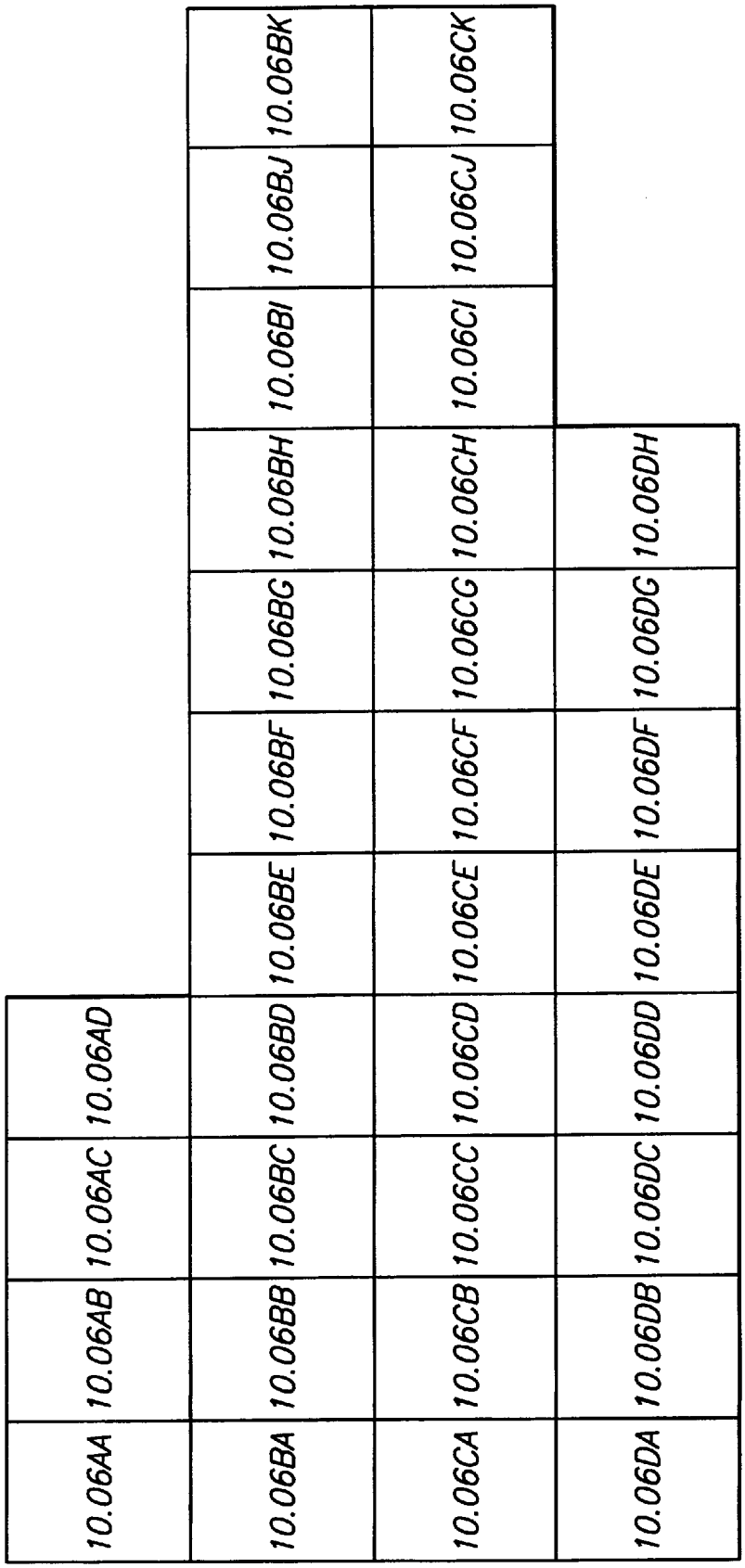

10.06AA
10.06AB
10.06AC
10.06AD
10.06BA
10.06BB
10.06BC
10.06BD
10.06BE
10.06BF
10.06BG
10.06BH
10.06BI
10.06BJ
10.06BK
10.06CA
10.06CB
10.06CC
10.06CD
10.06CE
10.06CF
10.06CG
10.06CH
10.06CI
10.06CJ
10.06CK
10.06DA
10.06DB
10.06DC
10.06DD
10.06DE
10.06DF
10.06DG
10.06DH

FIG 10.06

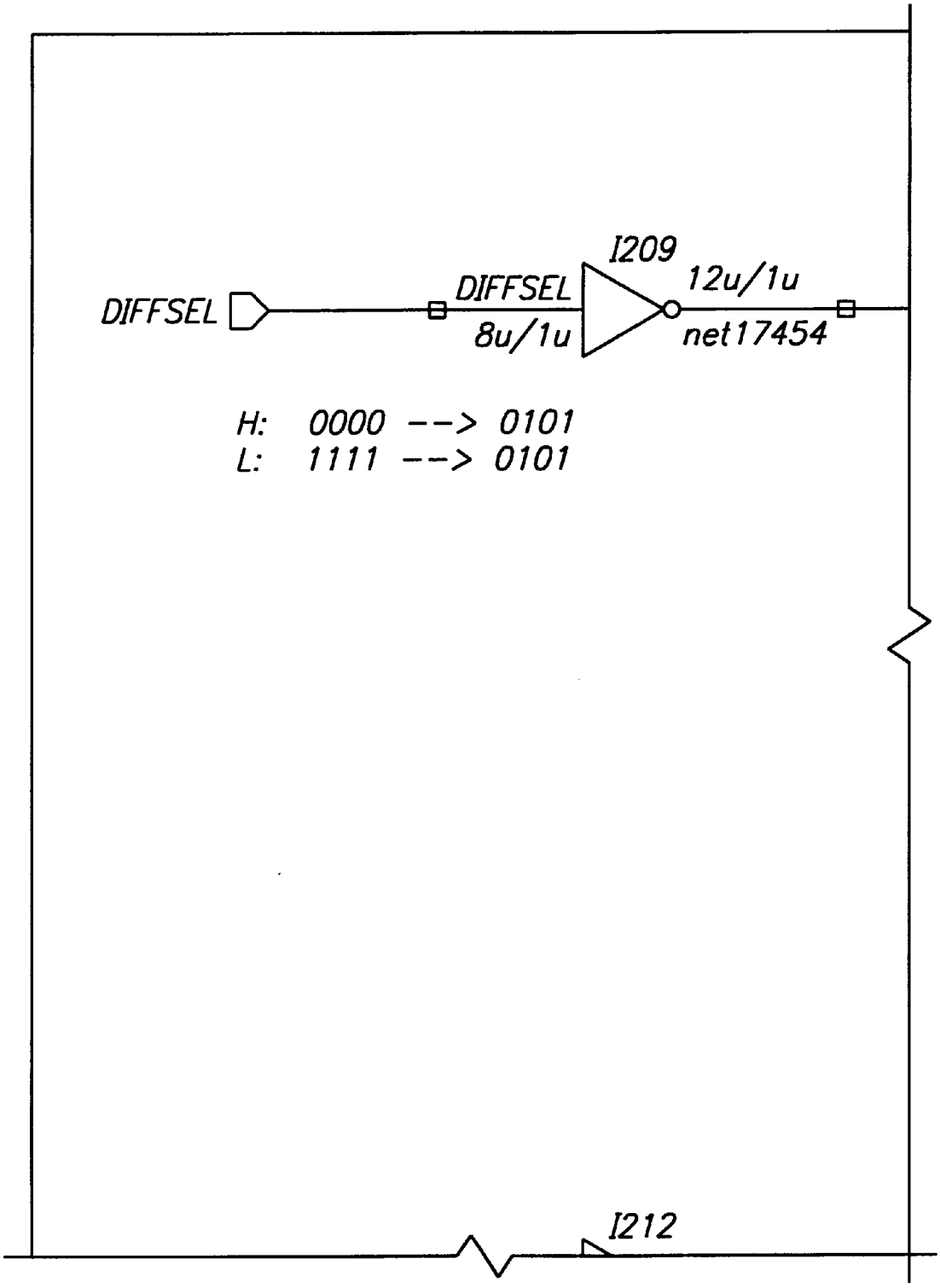

I209
DIFFSEL
DIFFSEL
12u/1u
8u/1u
net17454
H: 0000 --> 0101
L: 1111 --> 0101
I212

Fig 10.06AA

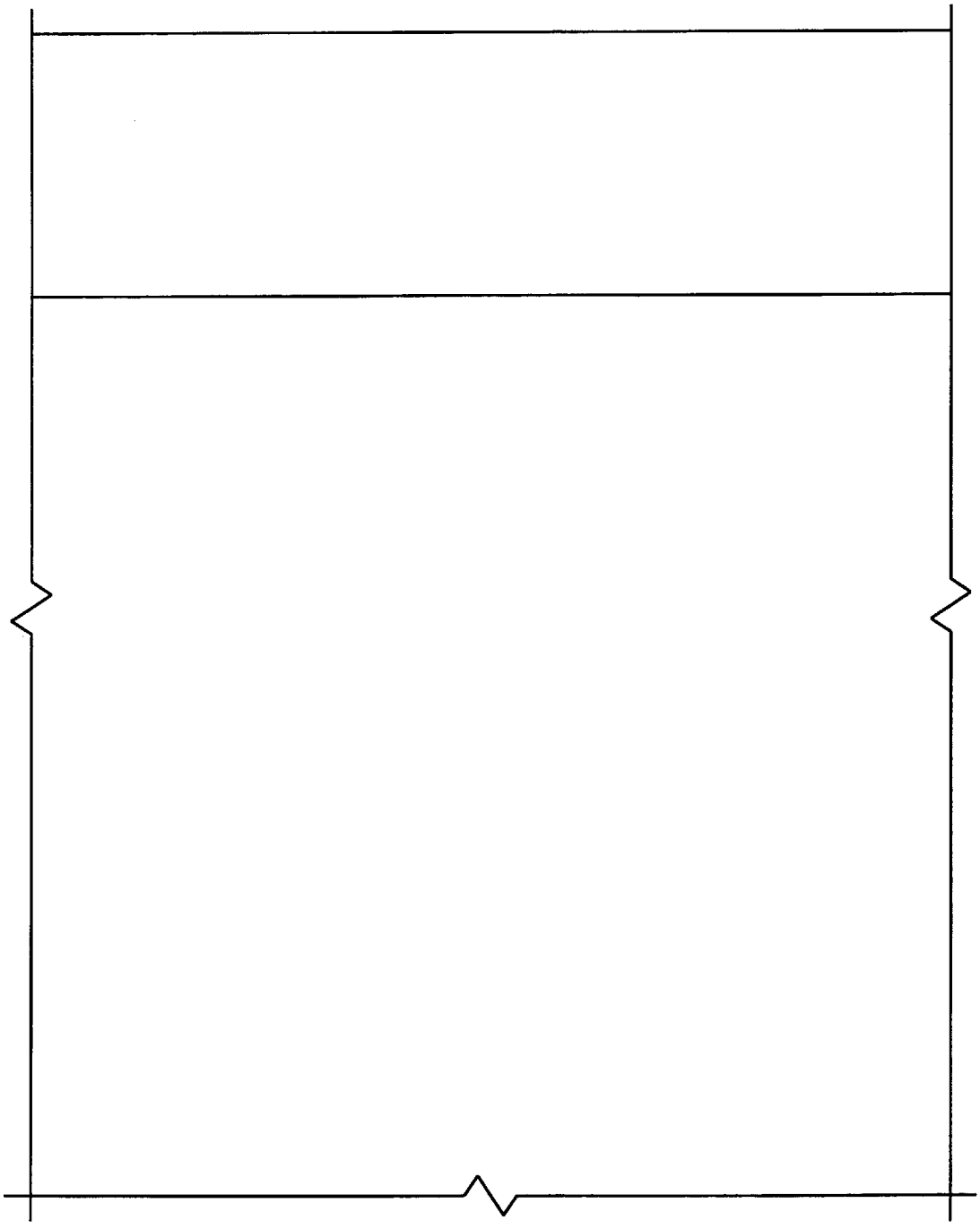


Fig 10.06AB

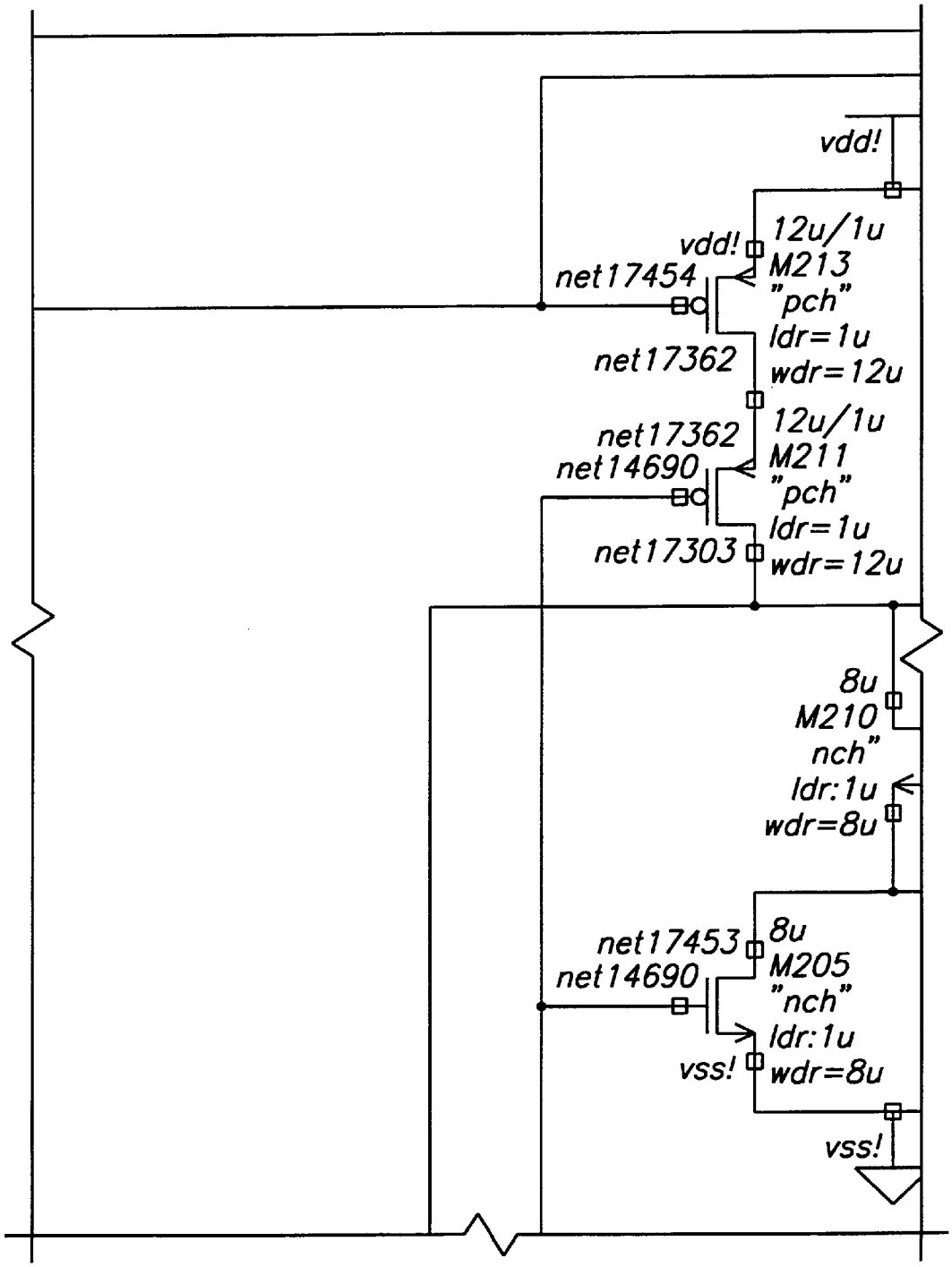

vdd!
vdd!
12u/1u
M213
"pch"
ldr=1u
wdr=12u
net17454
net17362
net17362
12u/1u
M211
"pch"
ldr=1u
wdr=12u
net14690
net17303
8u
M210
nch"
ldr:1u
wdr=8u
net17453
8u
M205
"nch"
ldr:1u
wdr=8u
net14690
vss!
vss!

Fig 10.06AC

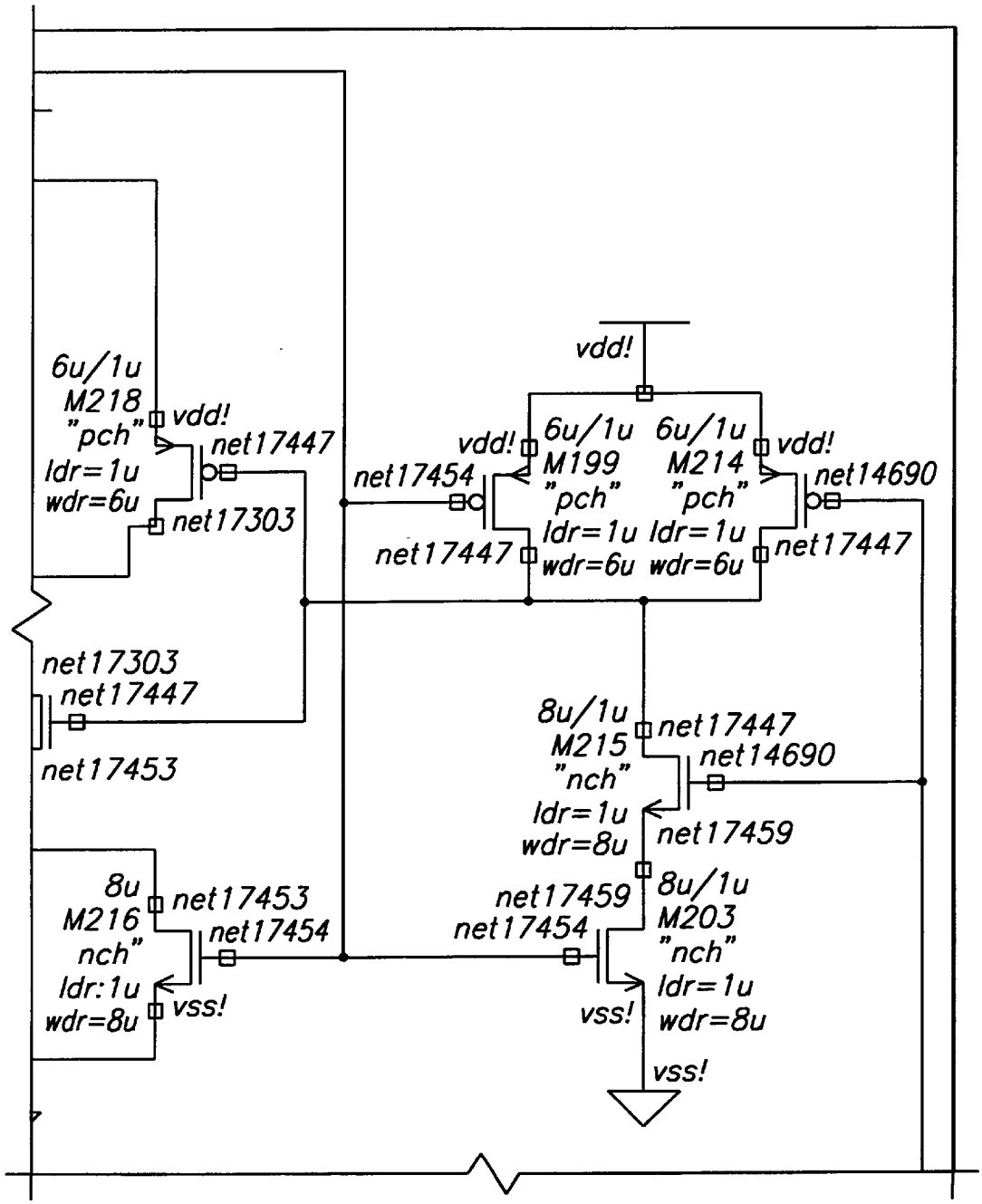

6u/1u
M218
"pch"
ldr=1u
wdr=6u
vdd!
net17447
net17303
net17454
vdd!
6u/1u
M199
"pch"
ldr=1u
wdr=6u
net17447
vdd!
6u/1u
M214
"pch"
ldr=1u
wdr=6u
vdd!
net14690
net17447
net17303
net17447
net17453
8u/1u
M215
"nch"
ldr=1u
wdr=8u
net17447
net14690
net17459
8u
M216
nch"
ldr:1u
wdr=8u
net17453
net17454
vss!
net17459
net17454
8u/1u
M203
"nch"
ldr=1u
wdr=8u
vss!
vss!

Fig 10.06AD

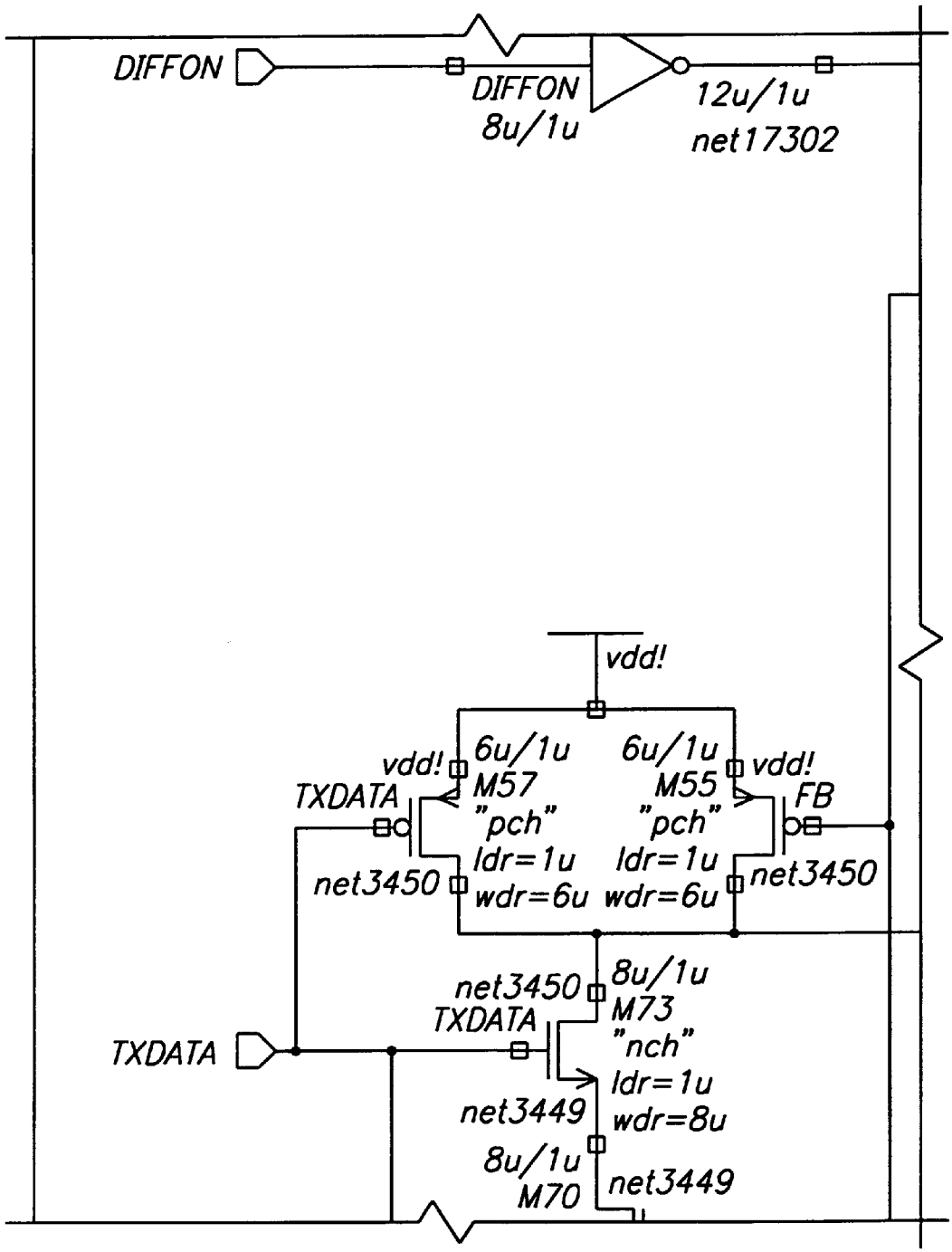

DIFFON
DIFFON
8u/1u
12u/1u
net17302
vdd!
vdd!
6u/1u
M57
"pch"
ldr=1u
wdr=6u
6u/1u
M55
"pch"
ldr=1u
wdr=6u
vdd!
TXDATA
FB
net3450
net3450
net3450
8u/1u
M73
"nch"
ldr=1u
wdr=8u
TXDATA
TXDATA
net3449
8u/1u
M70
net3449

Fig 10,068A

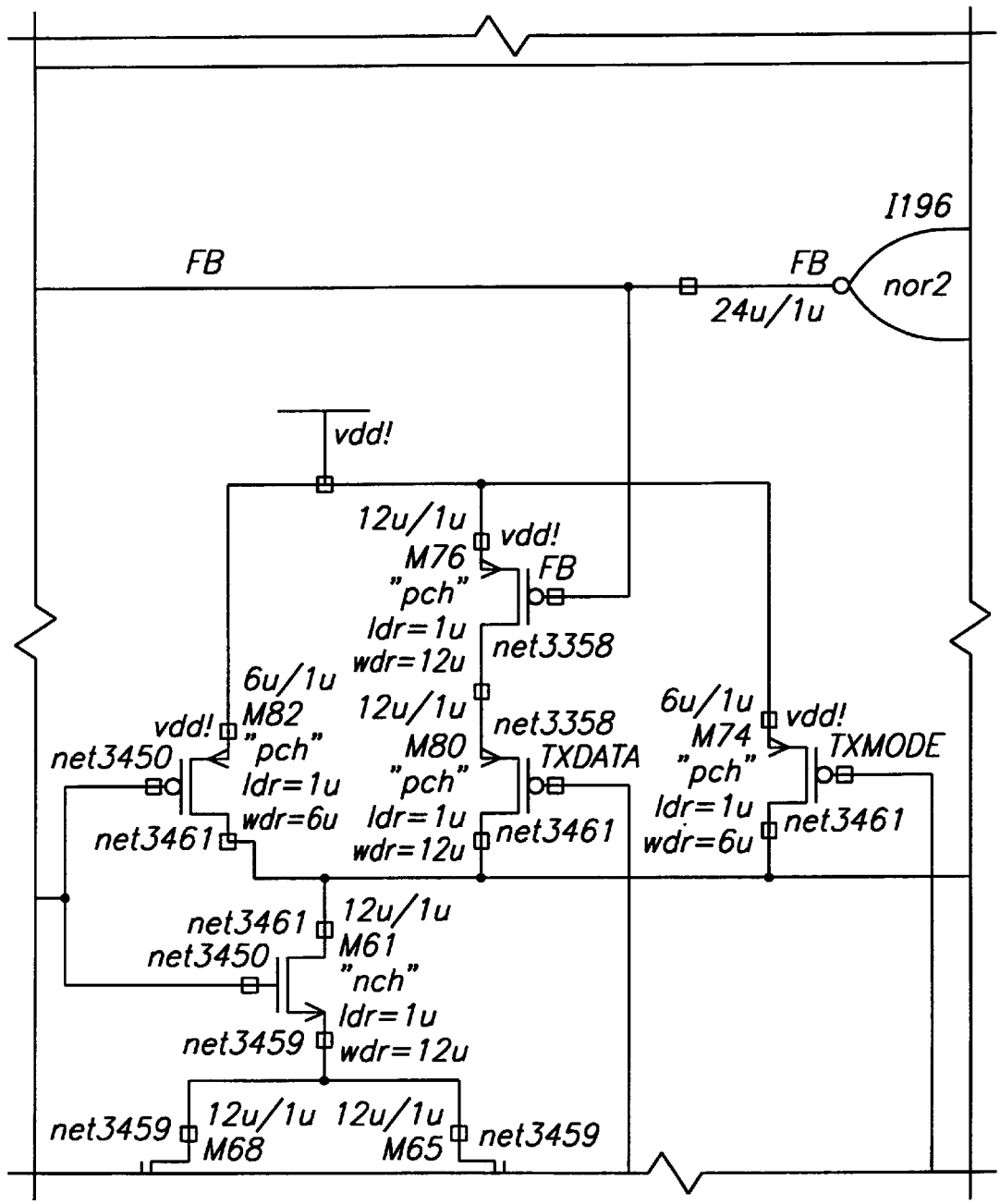

I196
FB
FB
nor2
24u/1u
vdd!
12u/1u
M76
"pch"
ldr=1u
wdr=12u
vdd!
FB
net3358
6u/1u
M82
"pch"
ldr=1u
wdr=6u
vdd!
net3450
net3461
12u/1u
M80
"pch"
ldr=1u
wdr=12u
net3358
TXDATA
net3461
6u/1u
M74
"pch"
ldr=1u
wdr=6u
vdd!
TXMODE
net3461
net3461
net3450
12u/1u
M61
"nch"
ldr=1u
wdr=12u
net3459
net3459
12u/1u
M68
12u/1u
M65
net3459

Fig 10.06BB

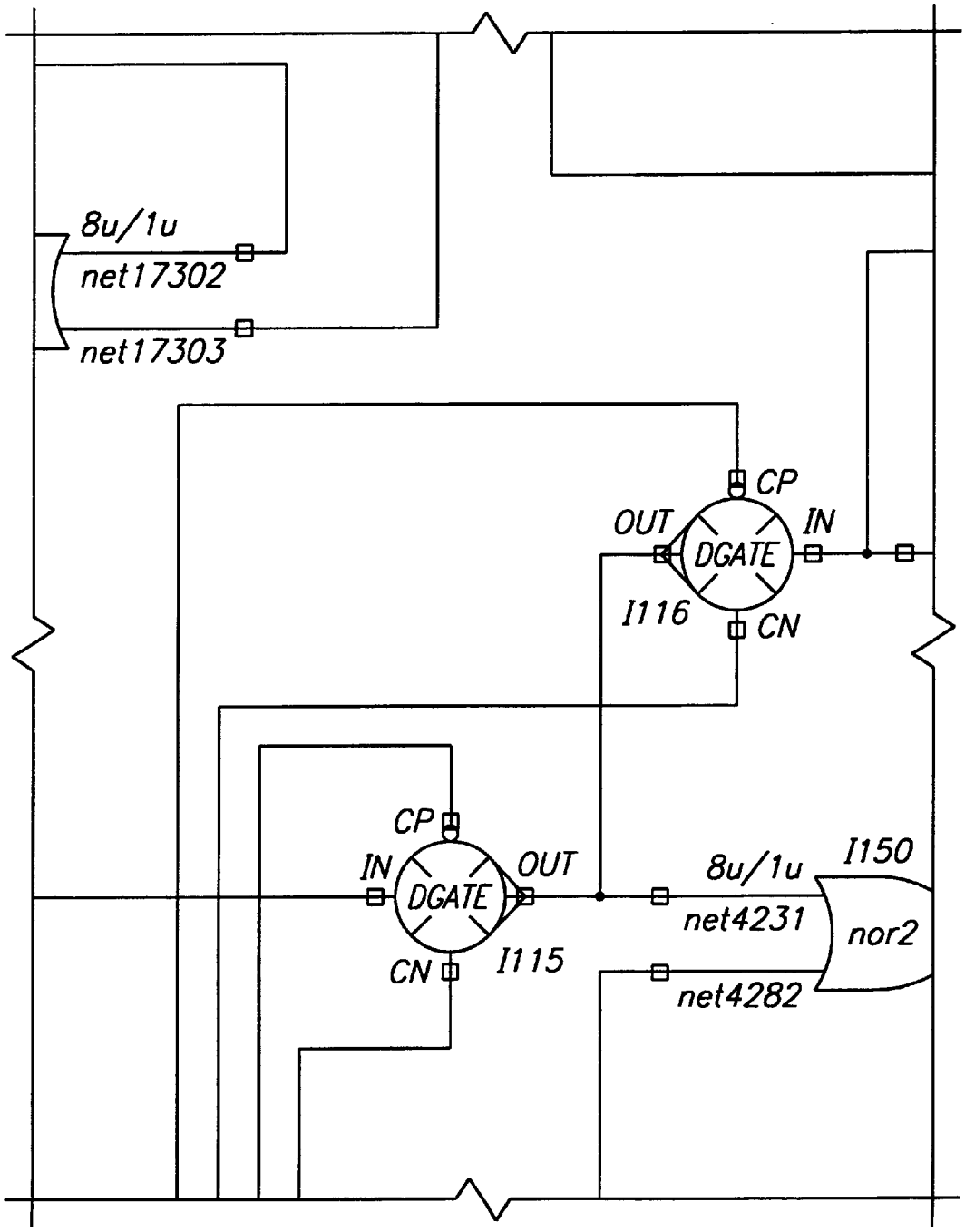

8u/1u
net17302
net17303
CP
OUT
IN
DGATE
I116
CN
CP
IN
OUT
DGATE
CN
I115
8u/1u
net4231
net4282
I150
nor2

Fig 10.06BC

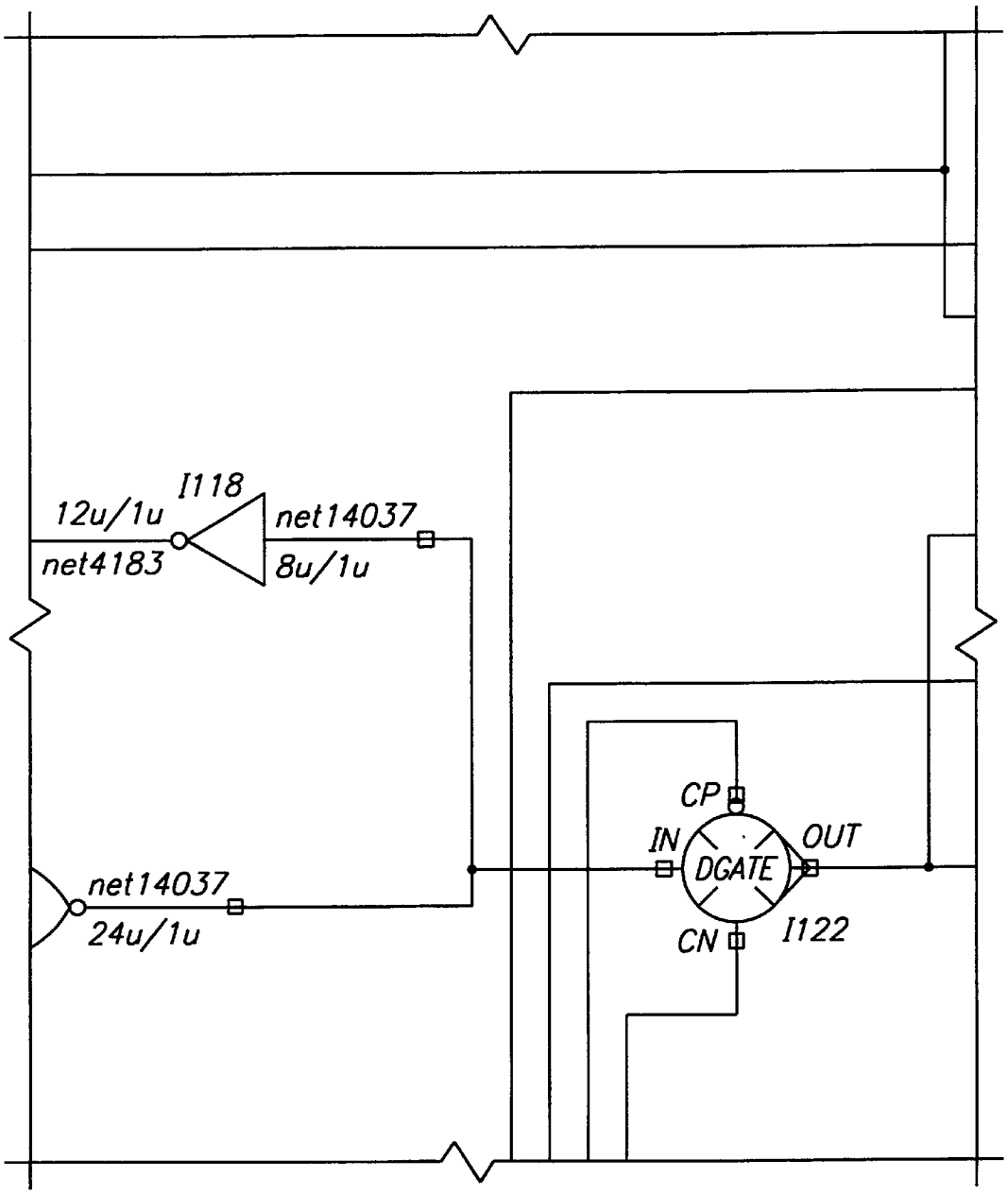

I118
12u/1u
net4183
net14037
8u/1u
net14037
24u/1u
CP
IN
DGATE
OUT
CN
I122

Fig 10.06BD

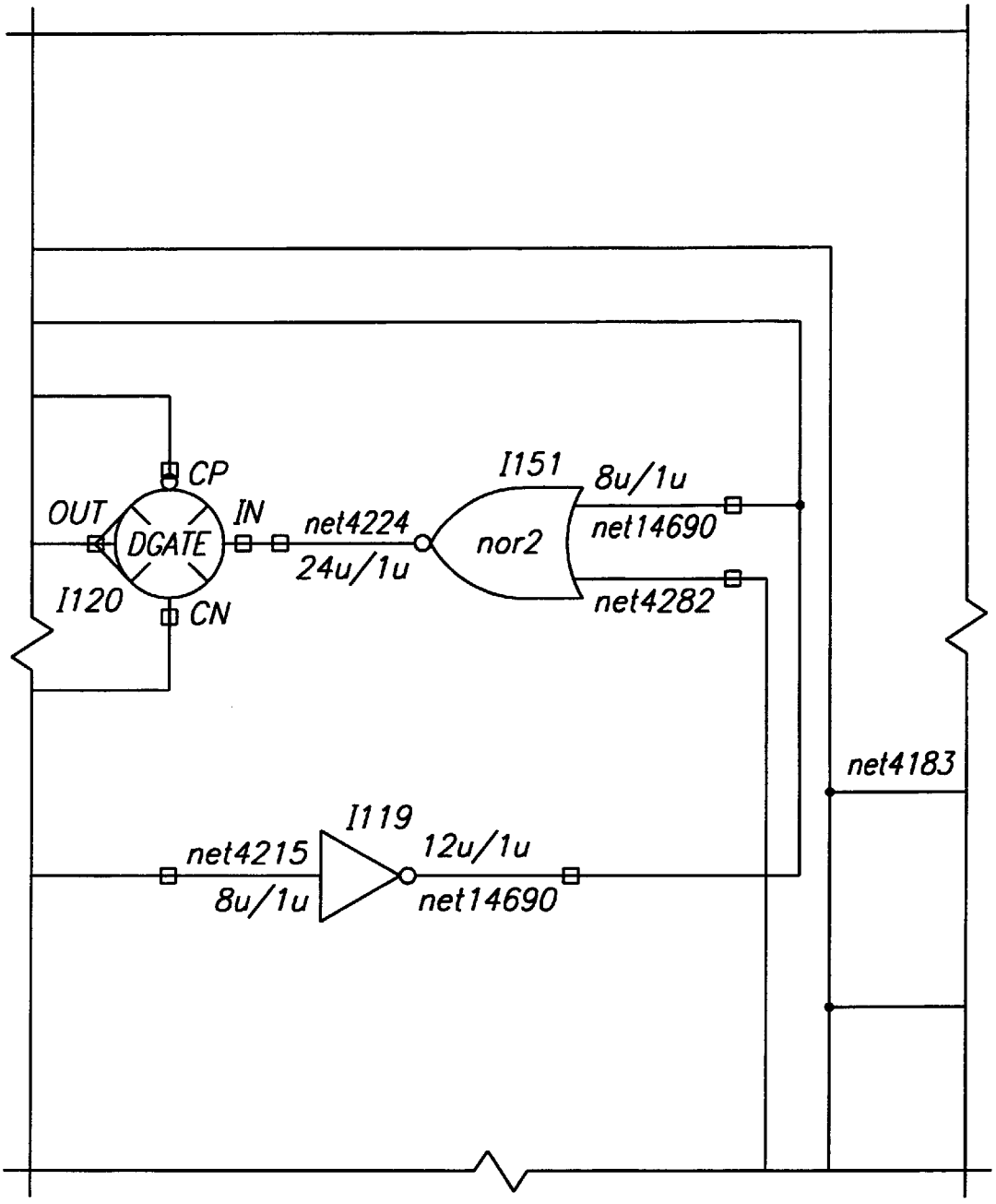

CP
OUT
DGATE
IN
net4224
24u/1u
I151
8u/1u
nor2
net14690
net4282
I120
CN
net4183
I119
net4215
8u/1u
12u/1u
net14690

Fig 10.06BE

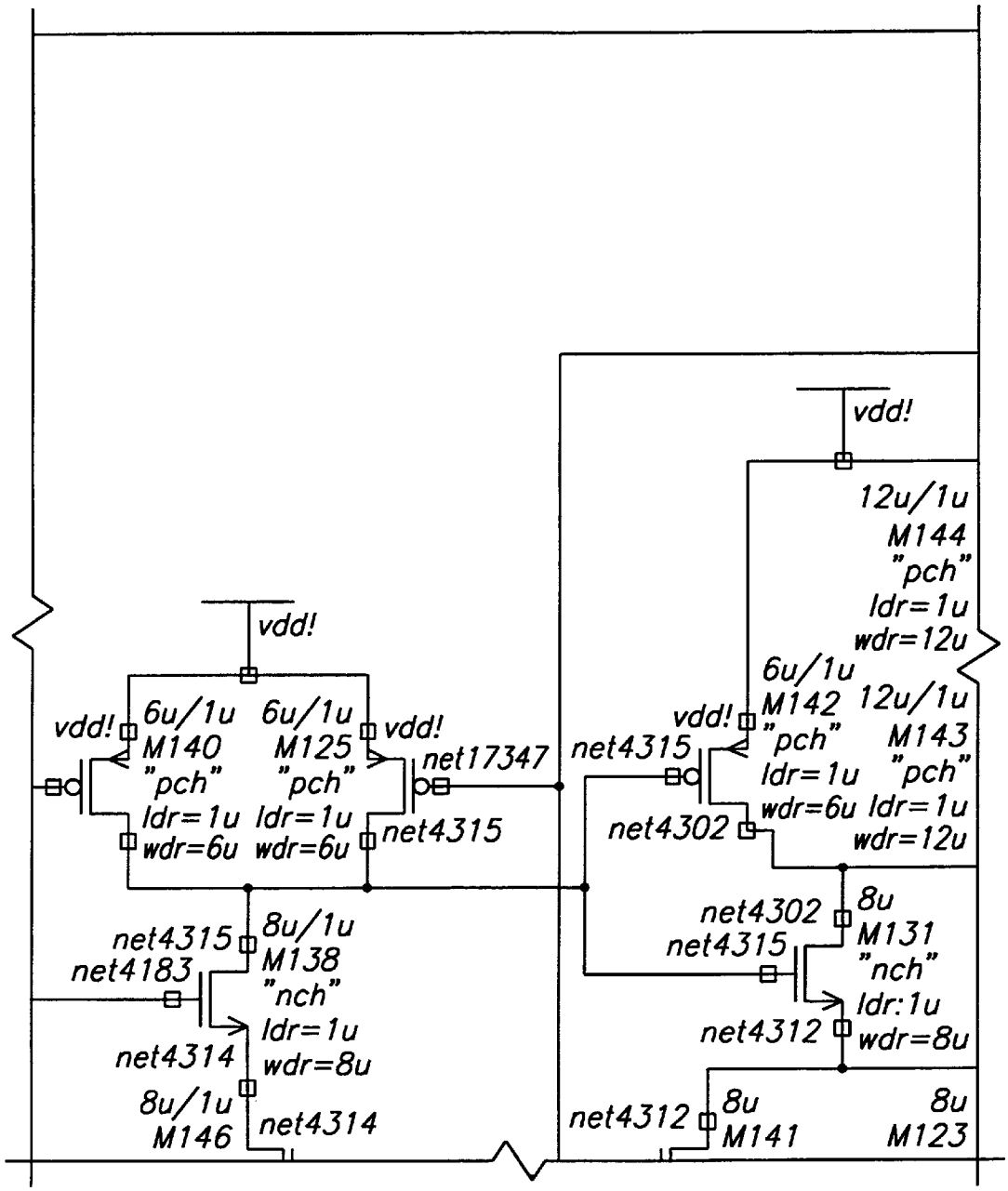

vdd!
12u/1u
M144
"pch"
ldr=1u
wdr=12u
6u/1u
M142
"pch"
ldr=1u
wdr=6u
12u/1u
M143
"pch"
ldr=1u
wdr=12u
vdd!
net4315
net4302
net4302
net4315
8u
M131
"nch"
ldr:1u
wdr=8u
net4312
net4312
8u
M141
8u
M123
vdd!
6u/1u
M140
"pch"
ldr=1u
wdr=6u
6u/1u
M125
"pch"
ldr=1u
wdr=6u
vdd!
vdd!
net17347
net4315
net4315
8u/1u
M138
"nch"
ldr=1u
wdr=8u
net4183
net4314
8u/1u
M146
net4314

Fig 10.06BF

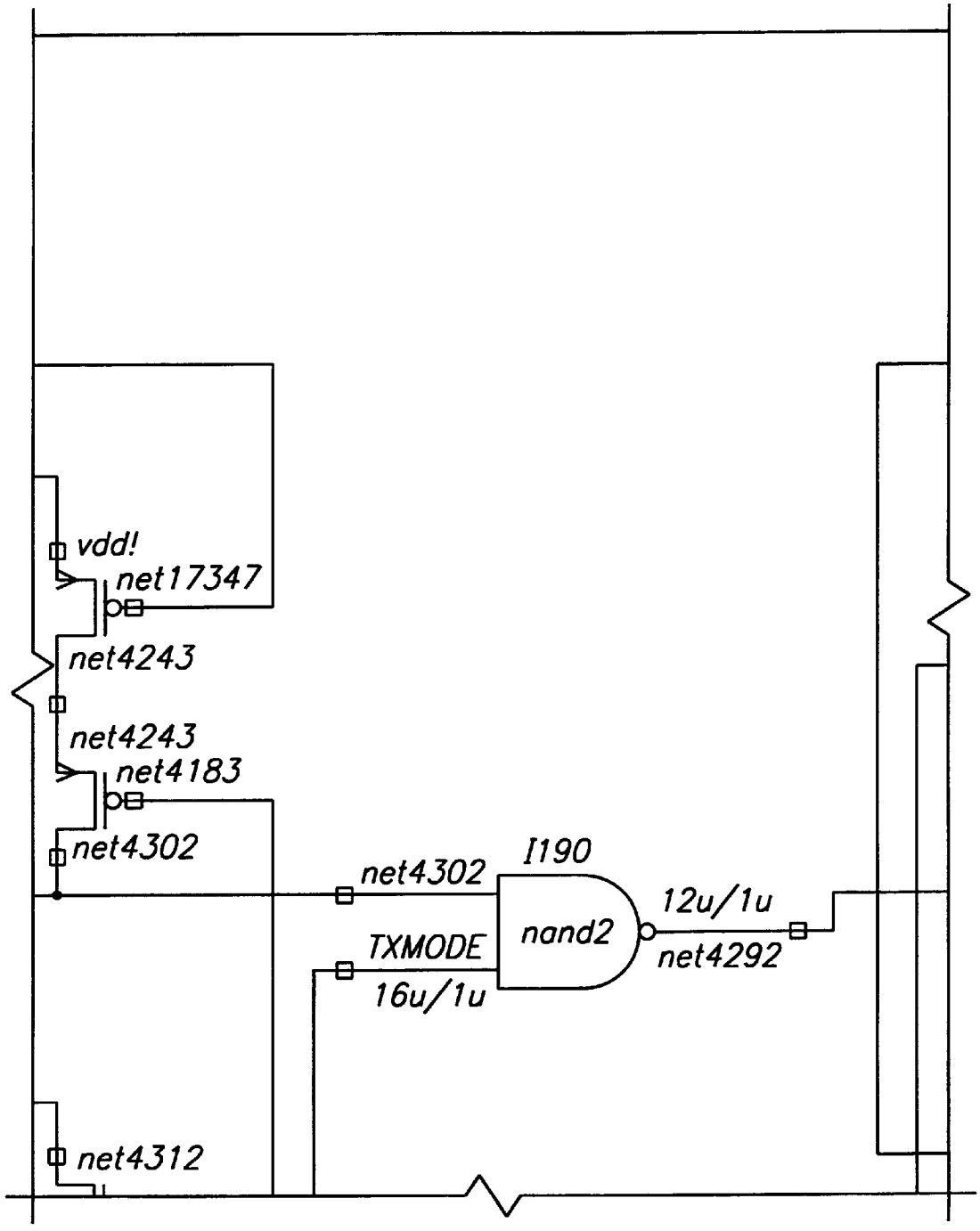

vdd!
net17347
net4243
net4243
net4183
net4302
net4302
I190
nand2
12u/1u
net4292
TXMODE
16u/1u
net4312

Fig 100,686

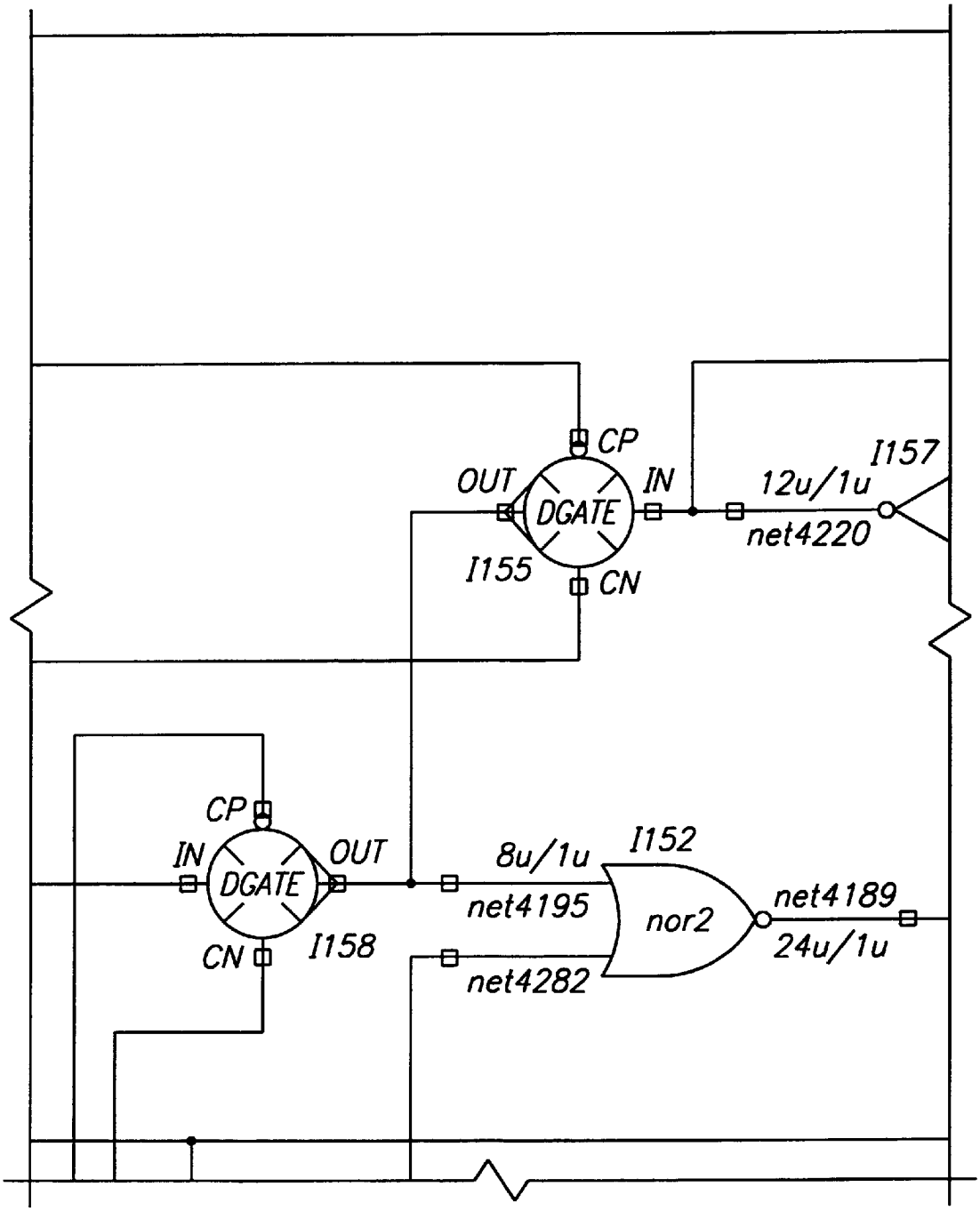

CP
OUT
DGATE
IN
I157
12u/1u
net4220
I155
CN
CP
IN
DGATE
OUT
8u/1u
I152
net4195
nor2
net4189
24u/1u
CN
I158
net4282

Fig 10.06BH

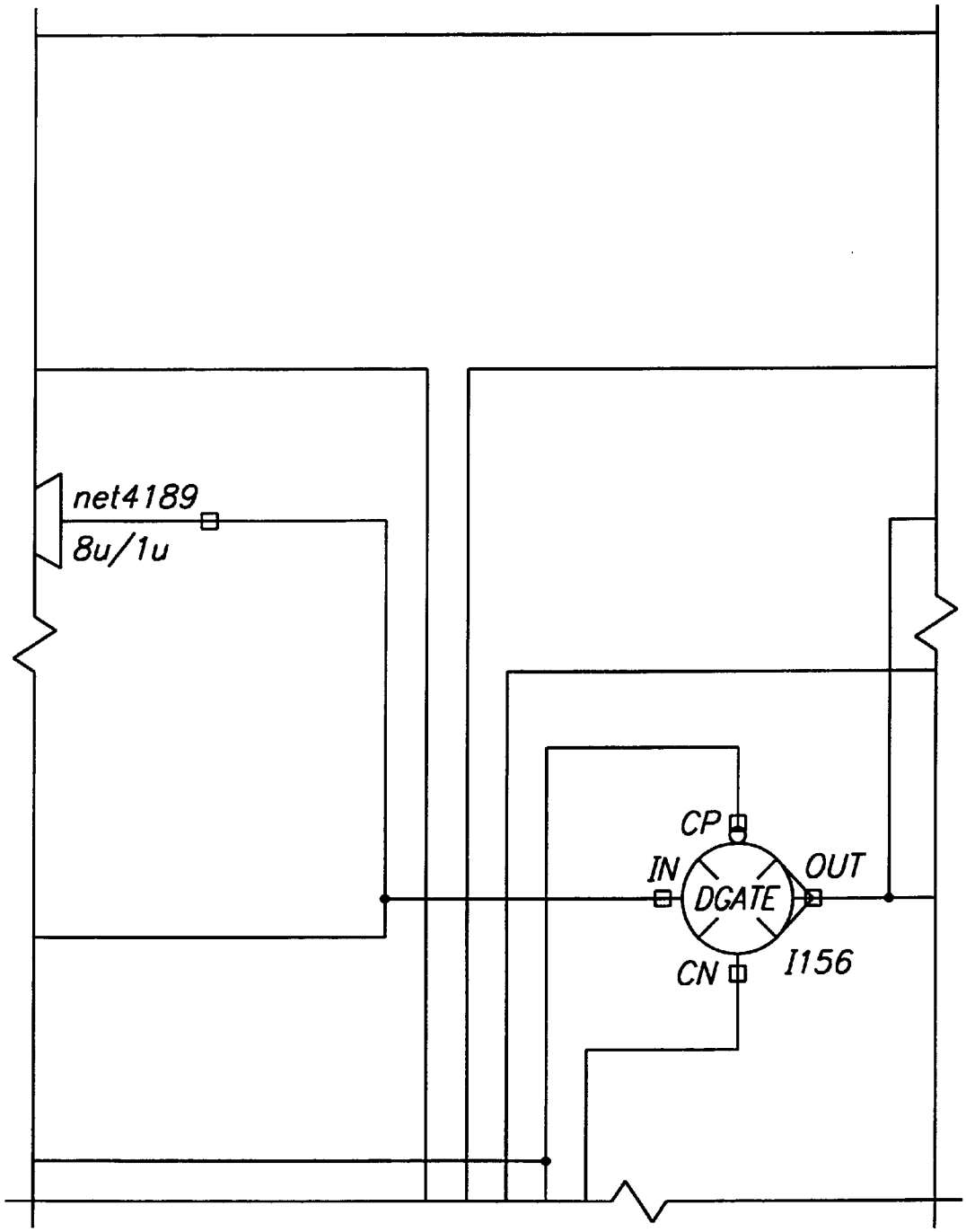


Fig 10.0681

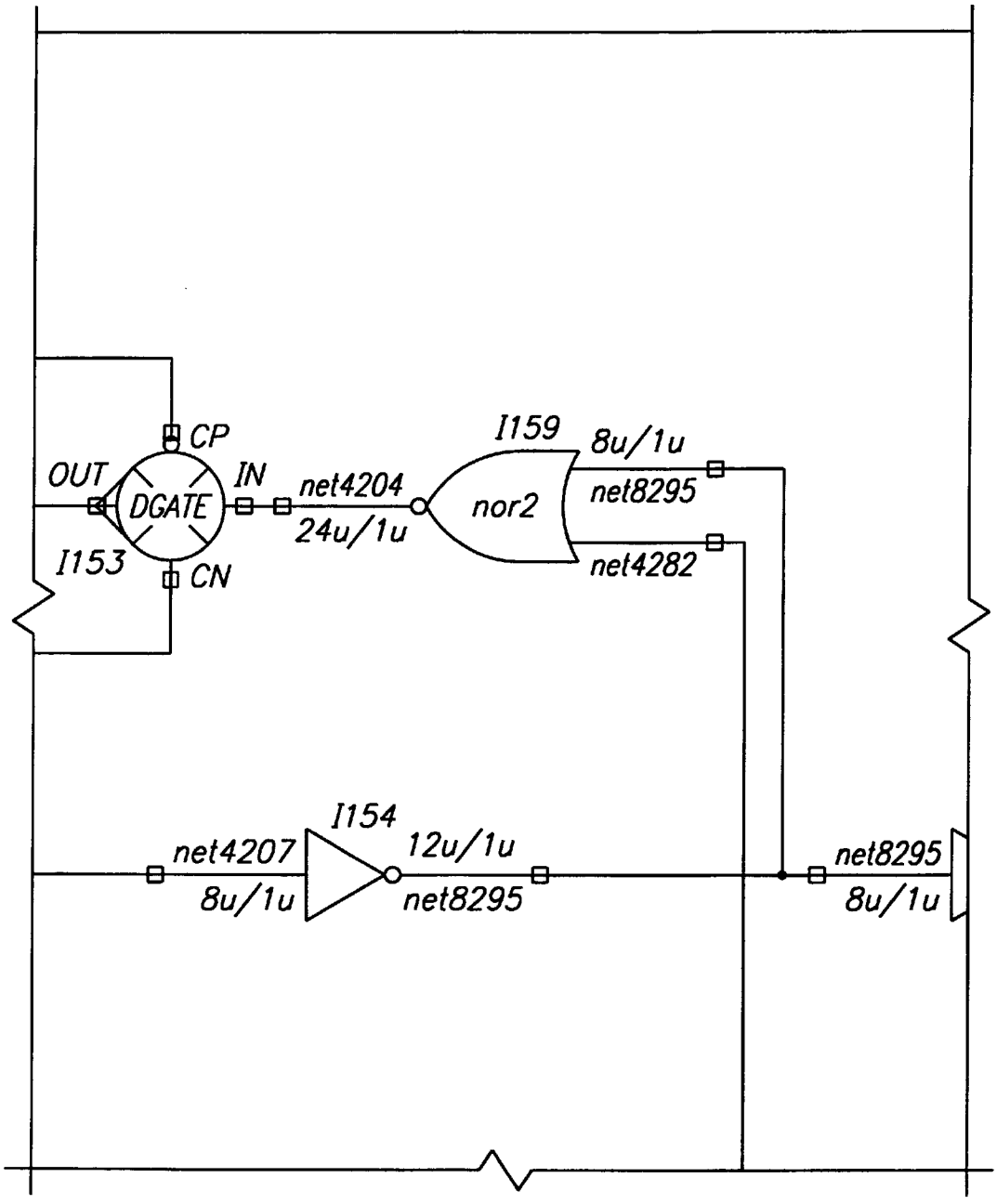

CP
OUT
DGATE
IN
net4204
24u/1u
I159
8u/1u
nor2
net8295
net4282
I153
CN
I154
net4207
8u/1u
12u/1u
net8295
net8295
8u/1u

Fig 10.06Bol

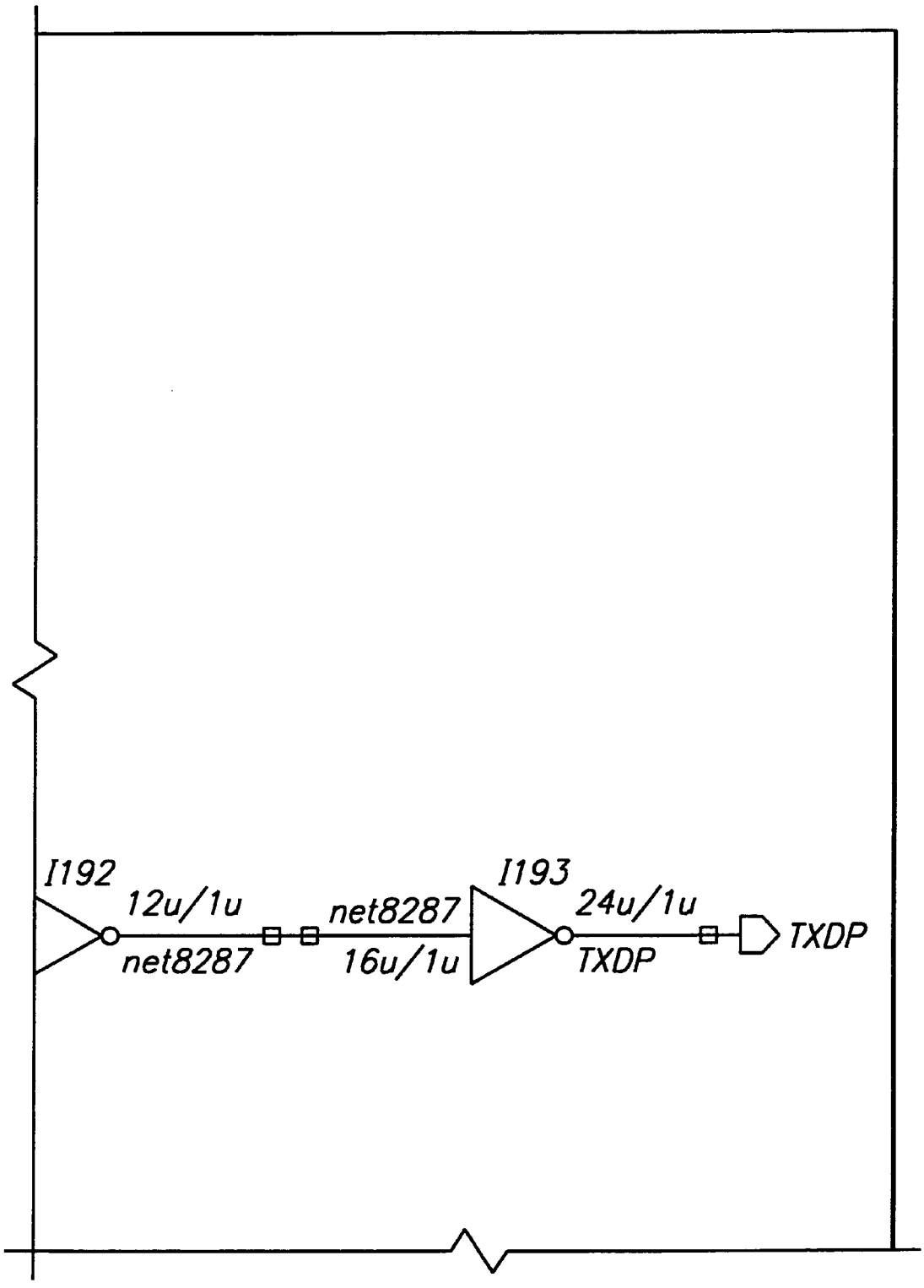


Fig 10.06BK

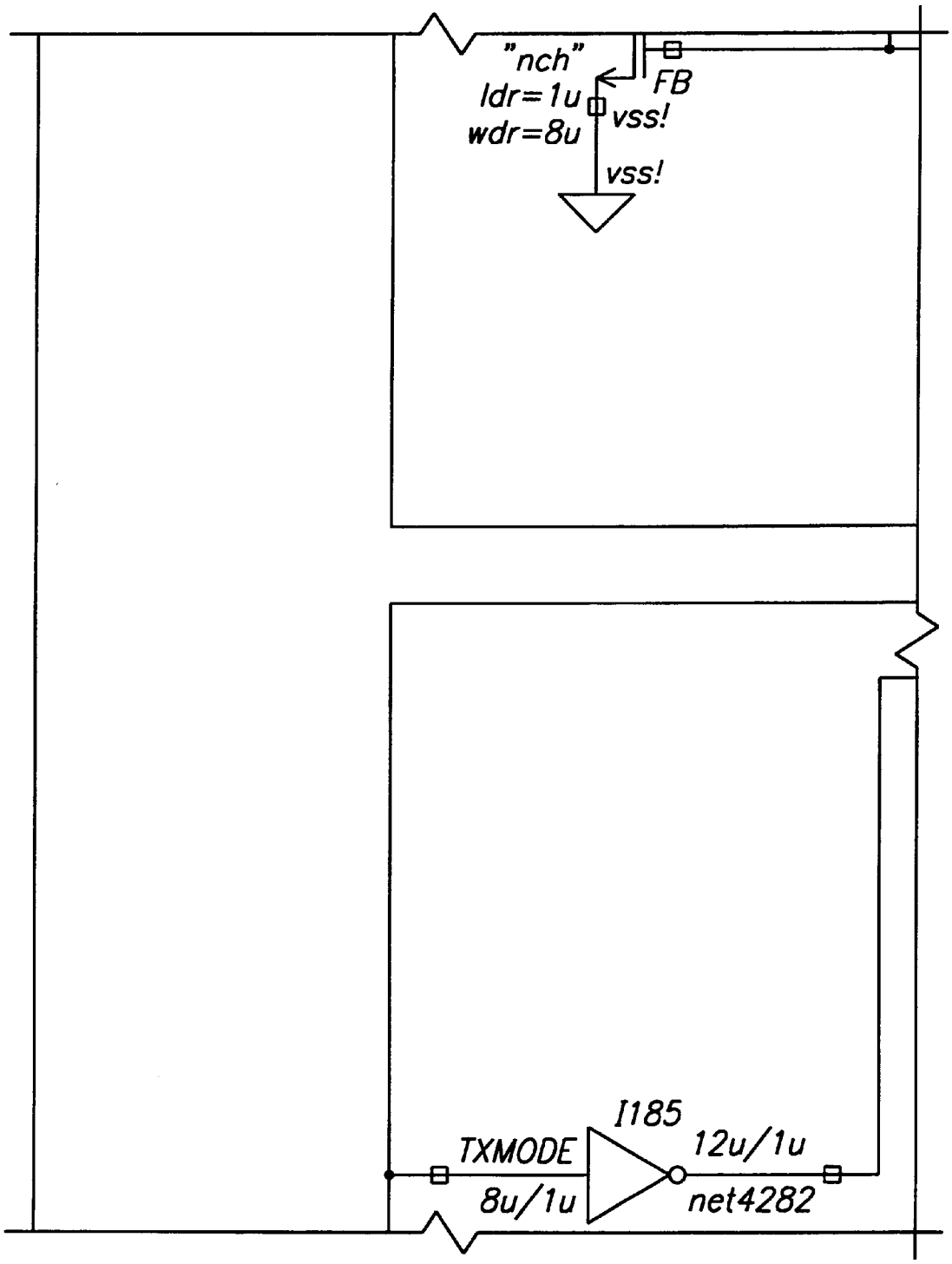


Fig 10.06CA

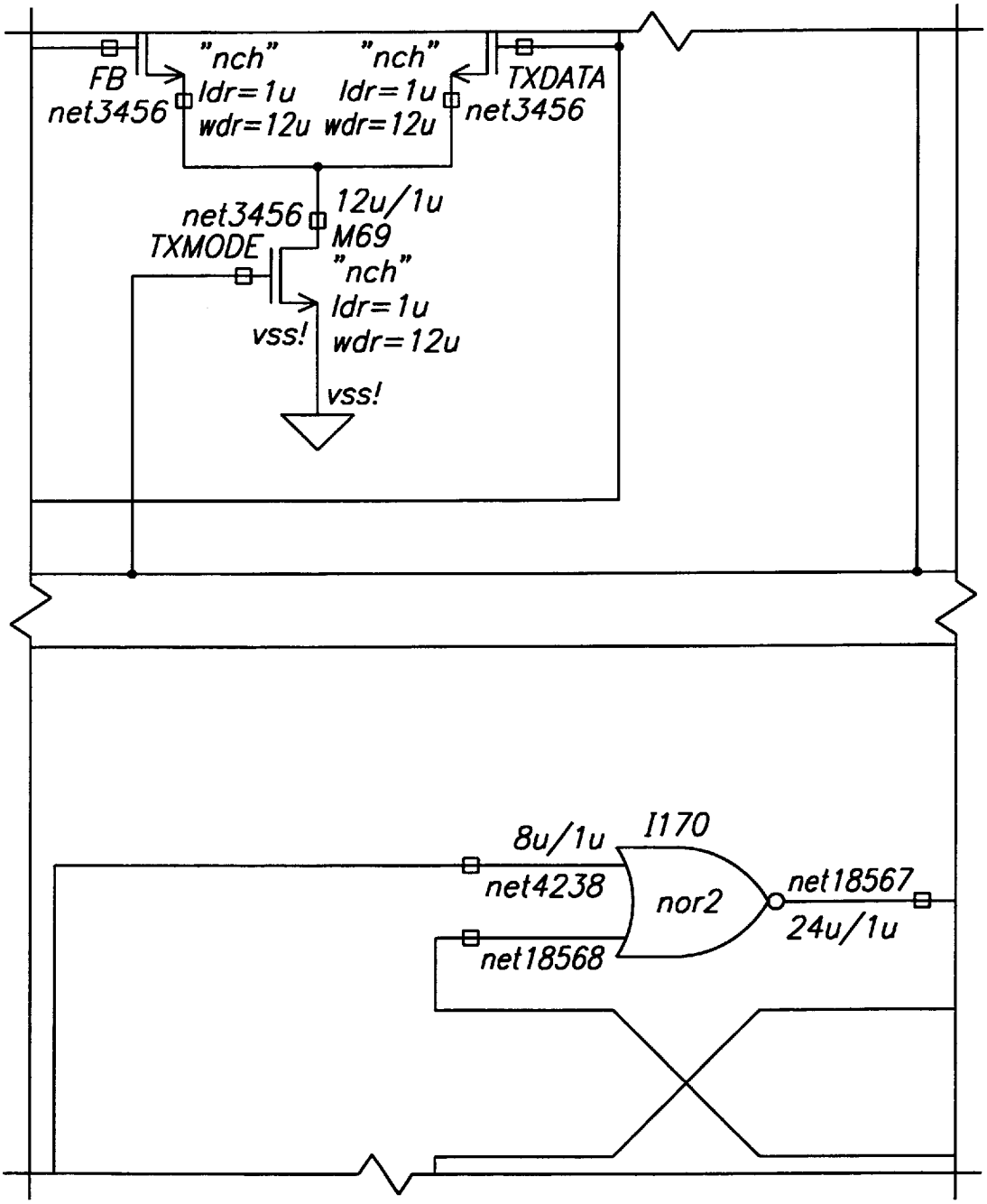

FB
net3456
"nch"
ldr=1u
wdr=12u
"nch"
ldr=1u
wdr=12u
TXDATA
net3456
net3456
TXMODE
12u/1u
M69
"nch"
ldr=1u
wdr=12u
vss!
vss!
8u/1u
net4238
I170
nor2
net18568
net18567
24u/1u

Fig 10.06CB

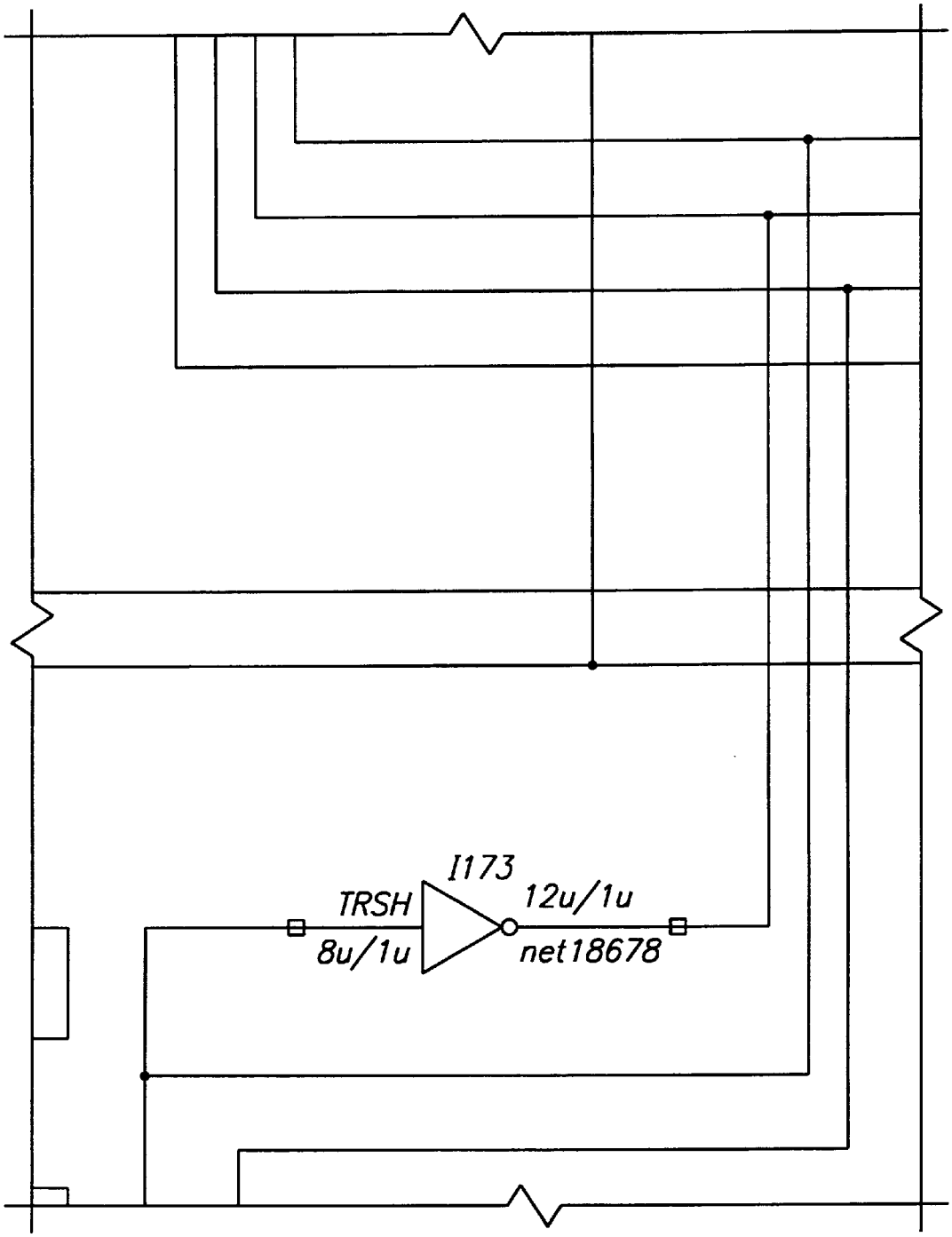


Fig 10.0660

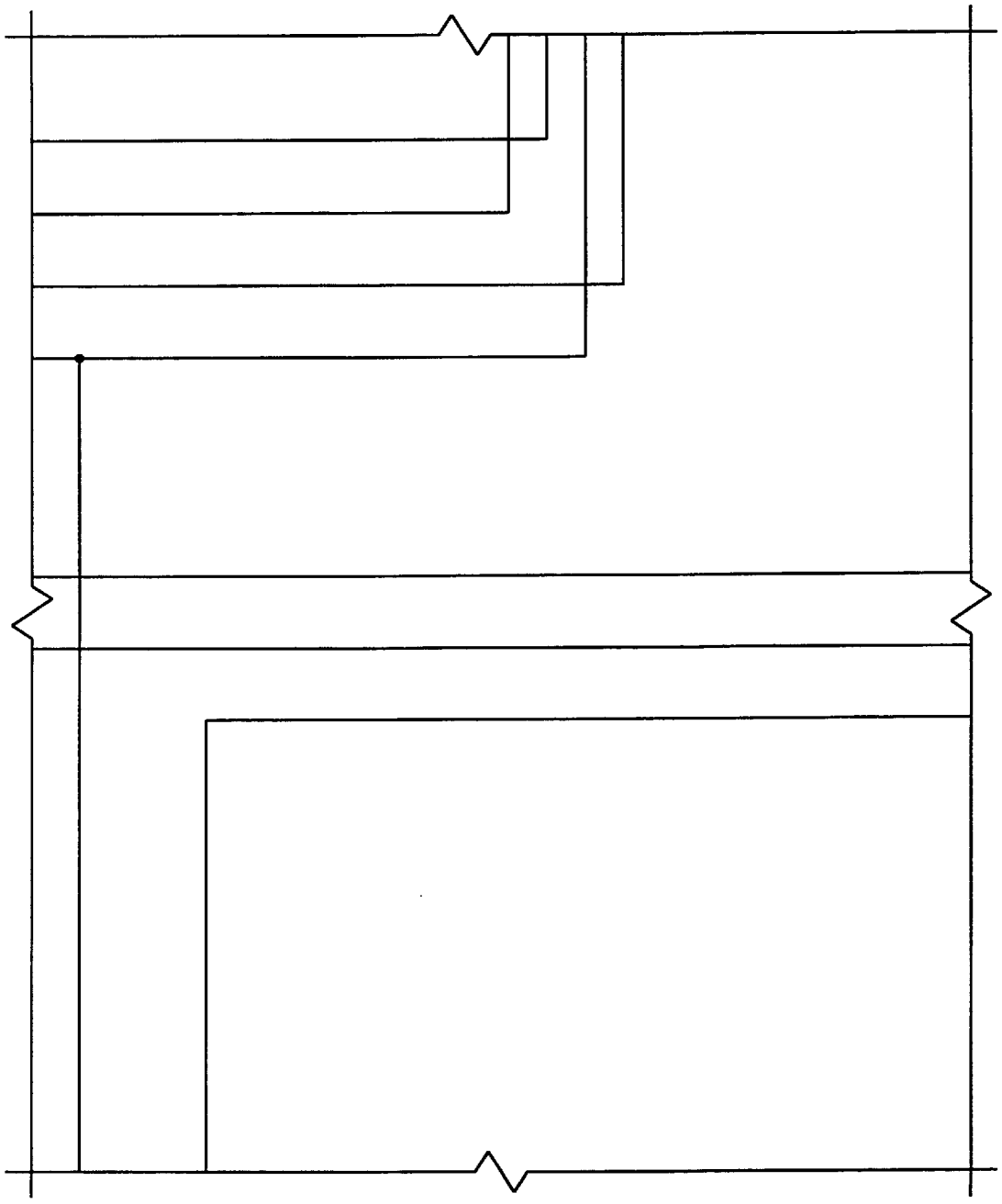


Fig 10.06CD

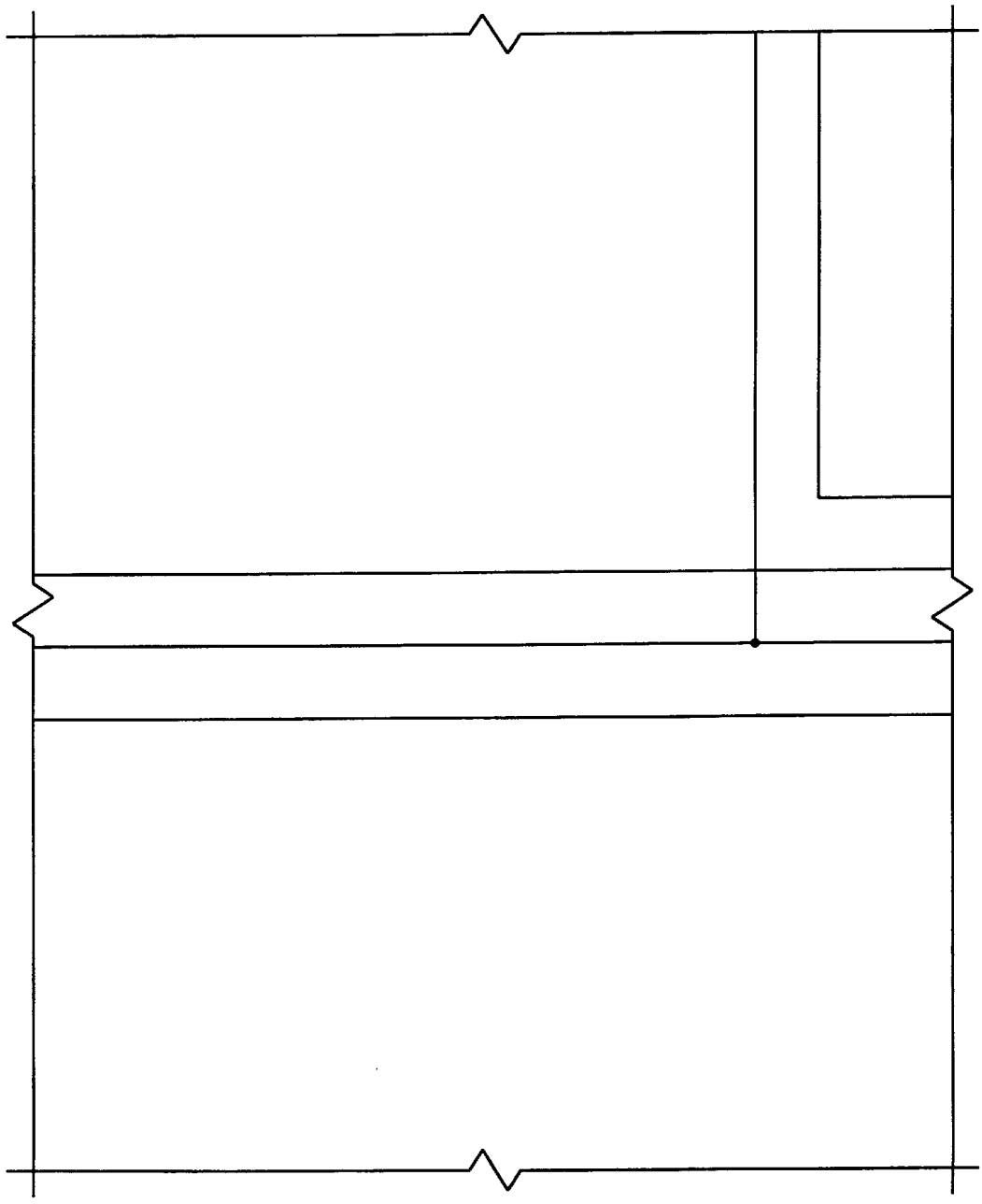


Fig 10.06CE

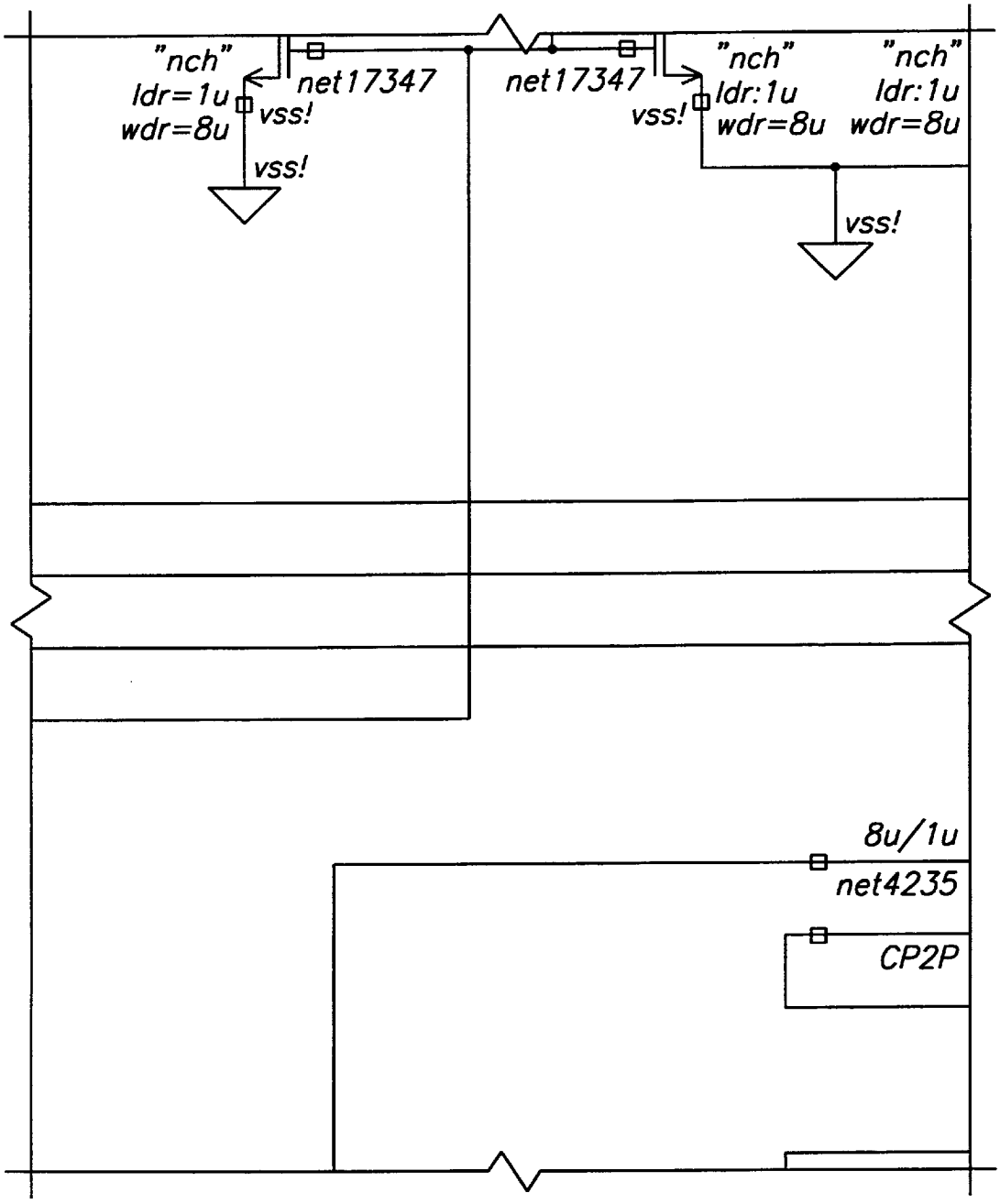

"nch"
ldr=1u
wdr=8u
vss!
net17347
vss!
net17347
"nch"
ldr:1u
wdr=8u
vss!
"nch"
ldr:1u
wdr=8u
vss!
8u/1u
net4235
CP2P

Fig 10.06CF

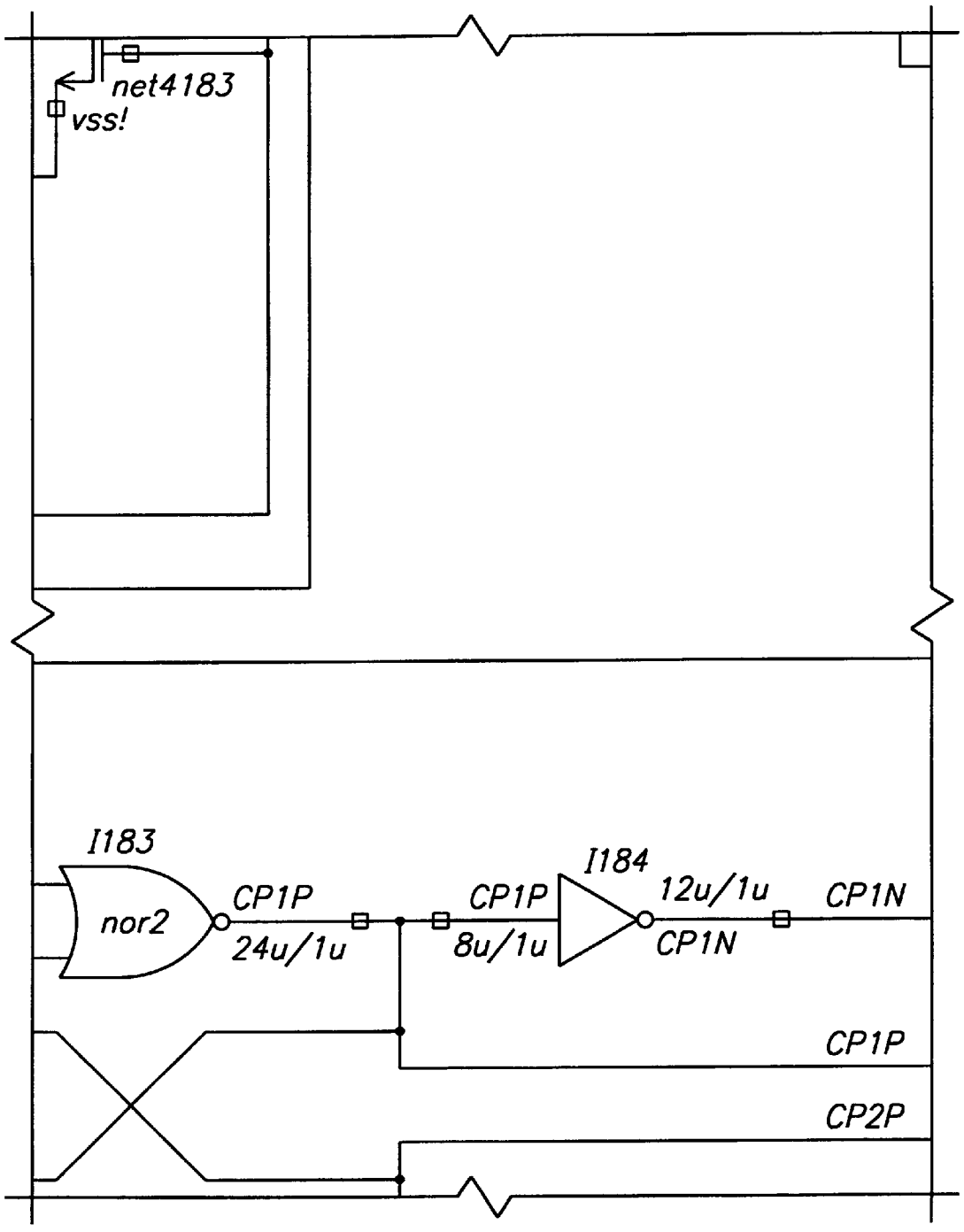

net4183
vss!
I183
nor2
CP1P
24u/1u
CP1P
8u/1u
I184
12u/1u
CP1N
CP1N
CP1P
CP2P

Fig 10.06C6

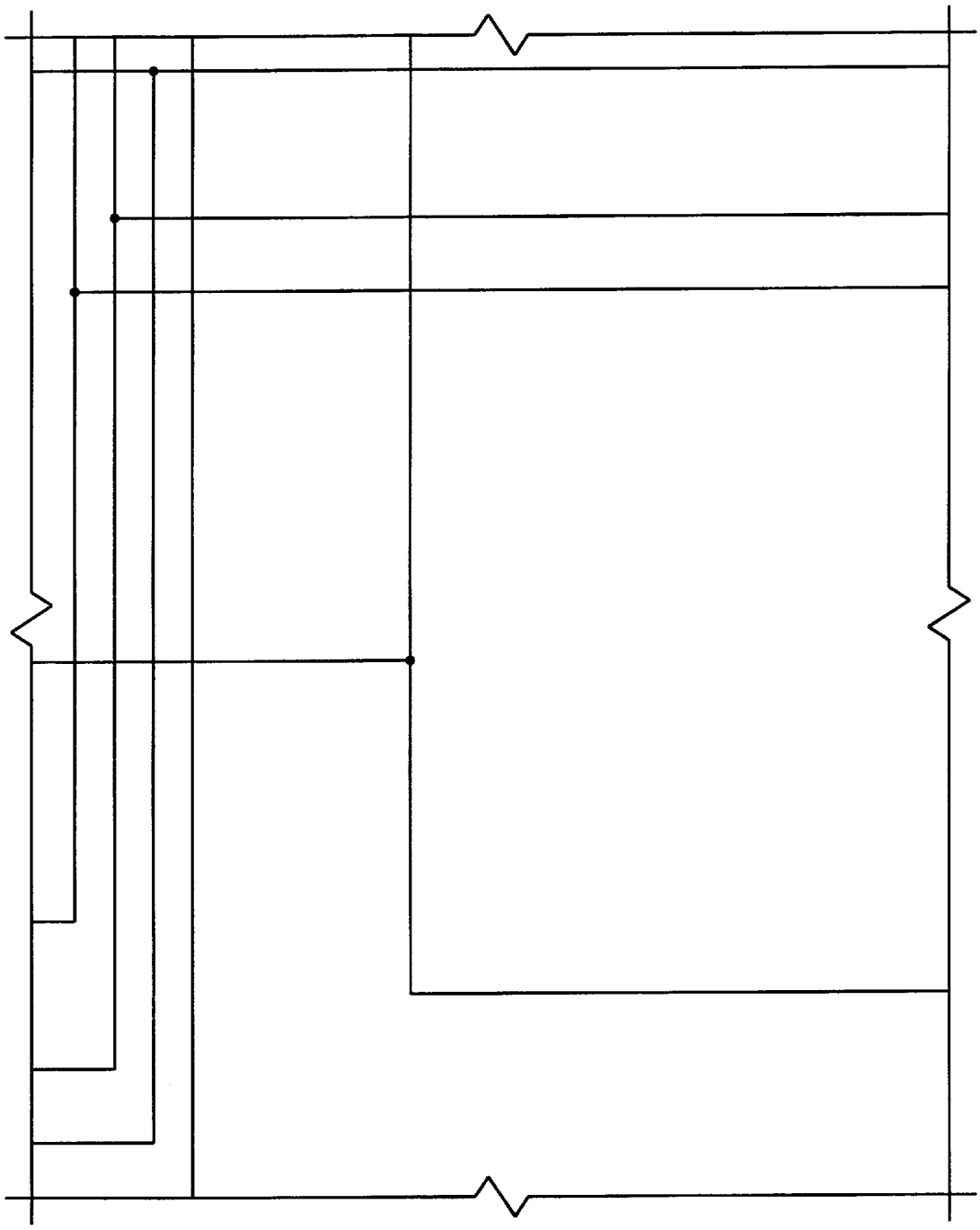


Fig 10.06CH

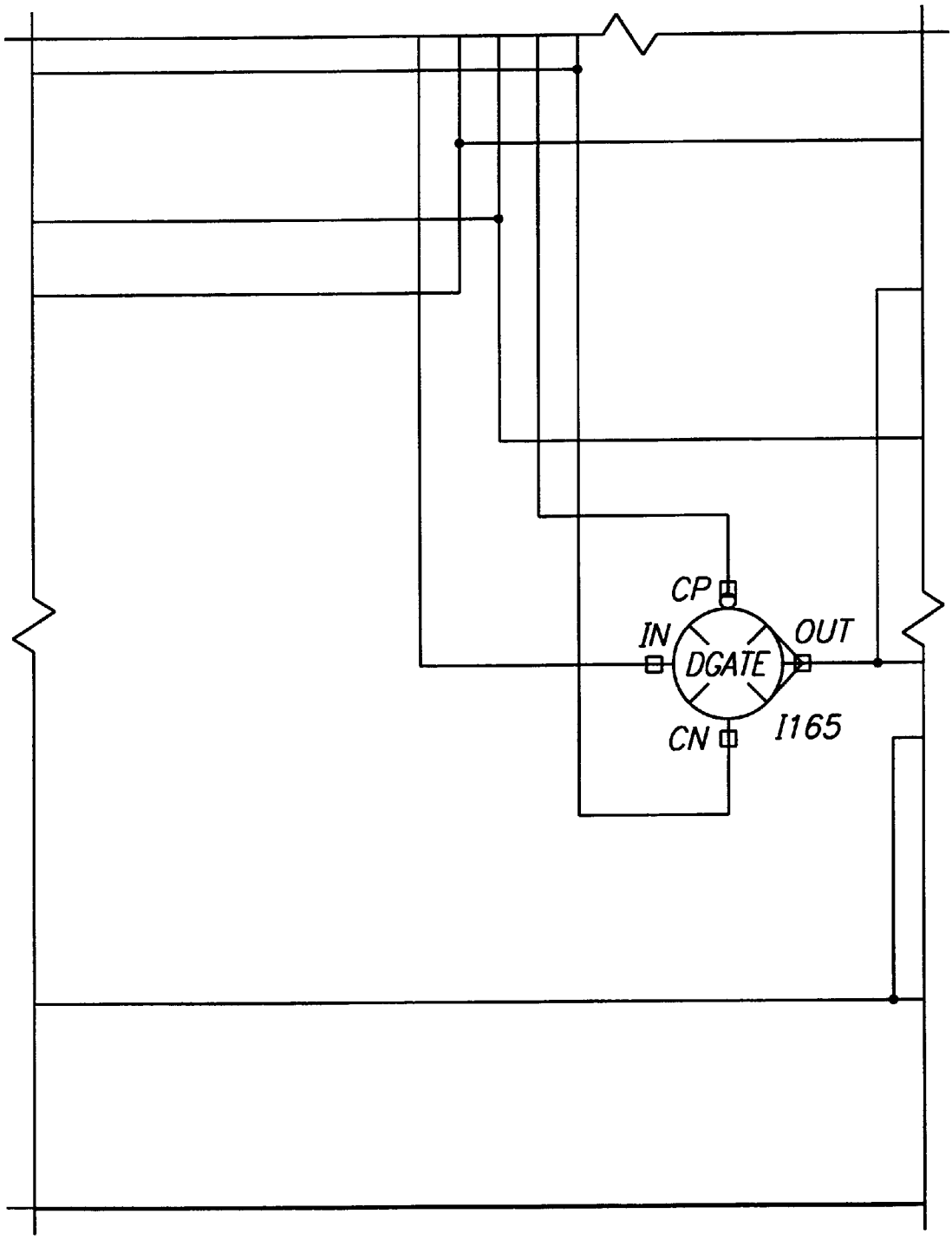


Fig 10.06CII

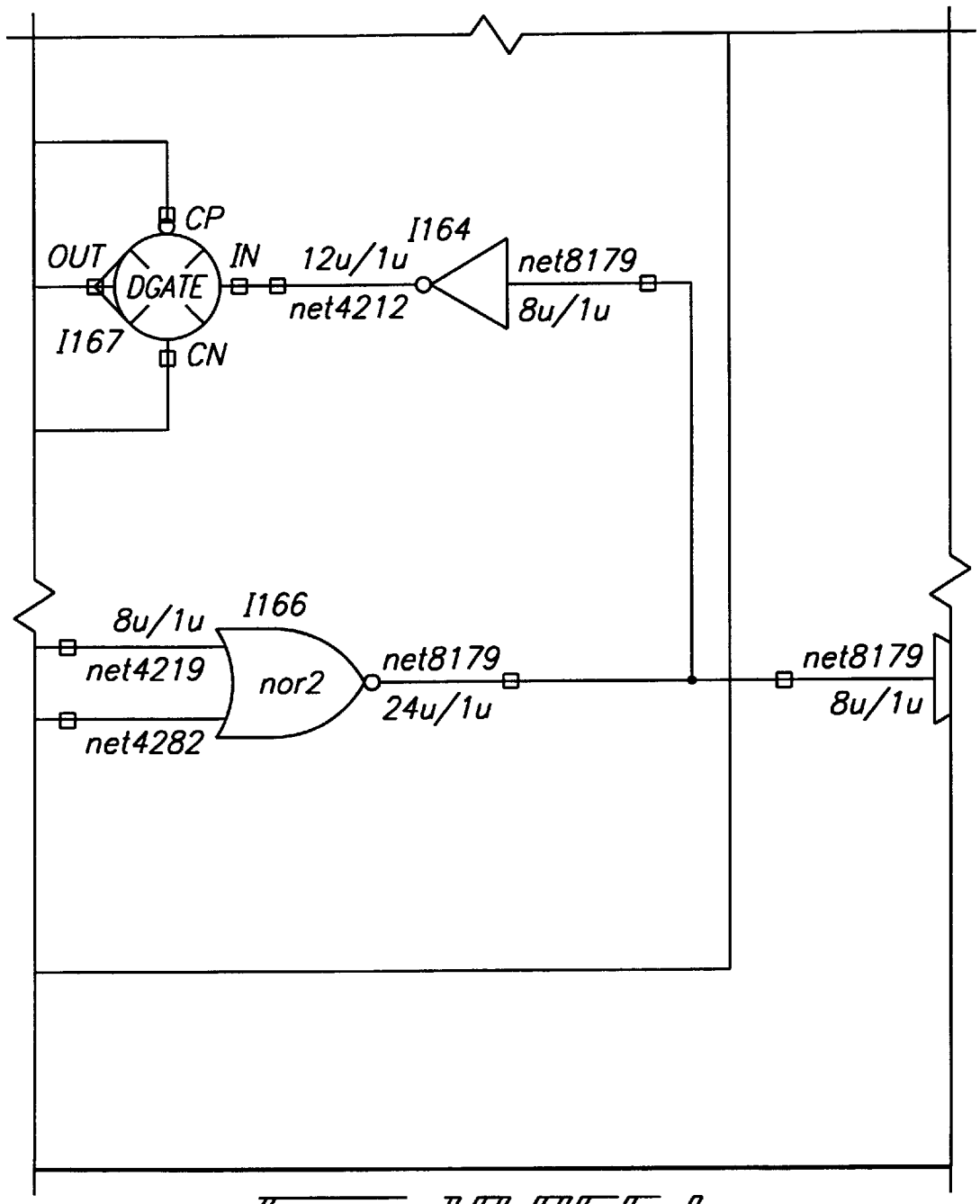

CP
OUT
DGATE
IN
I167
CN
12u/1u
net4212
I164
net8179
8u/1u
8u/1u
net4219
net4282
I166
nor2
net8179
24u/1u
net8179
8u/1u

Fig 10.06Cd

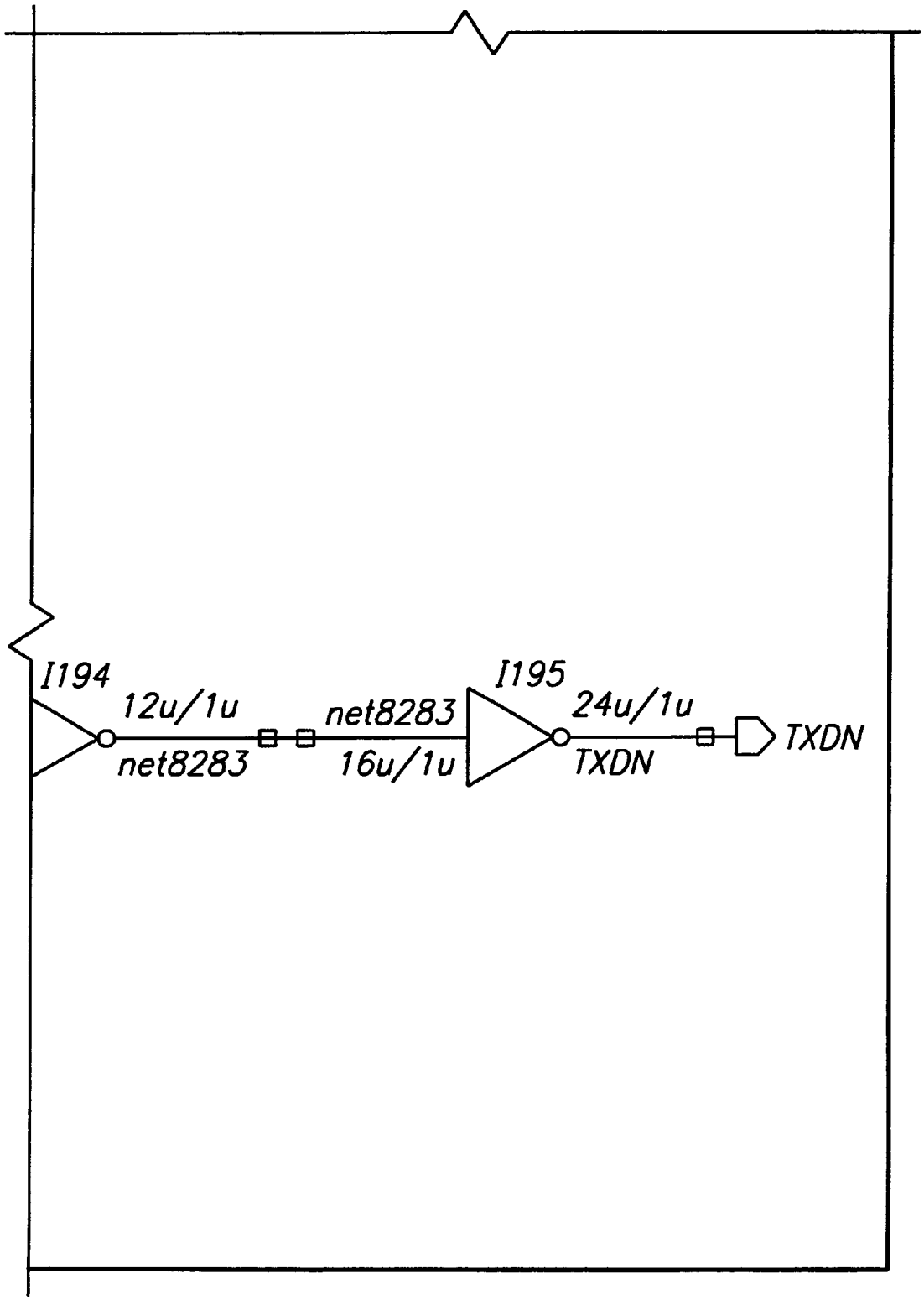


Fig 10.06CK

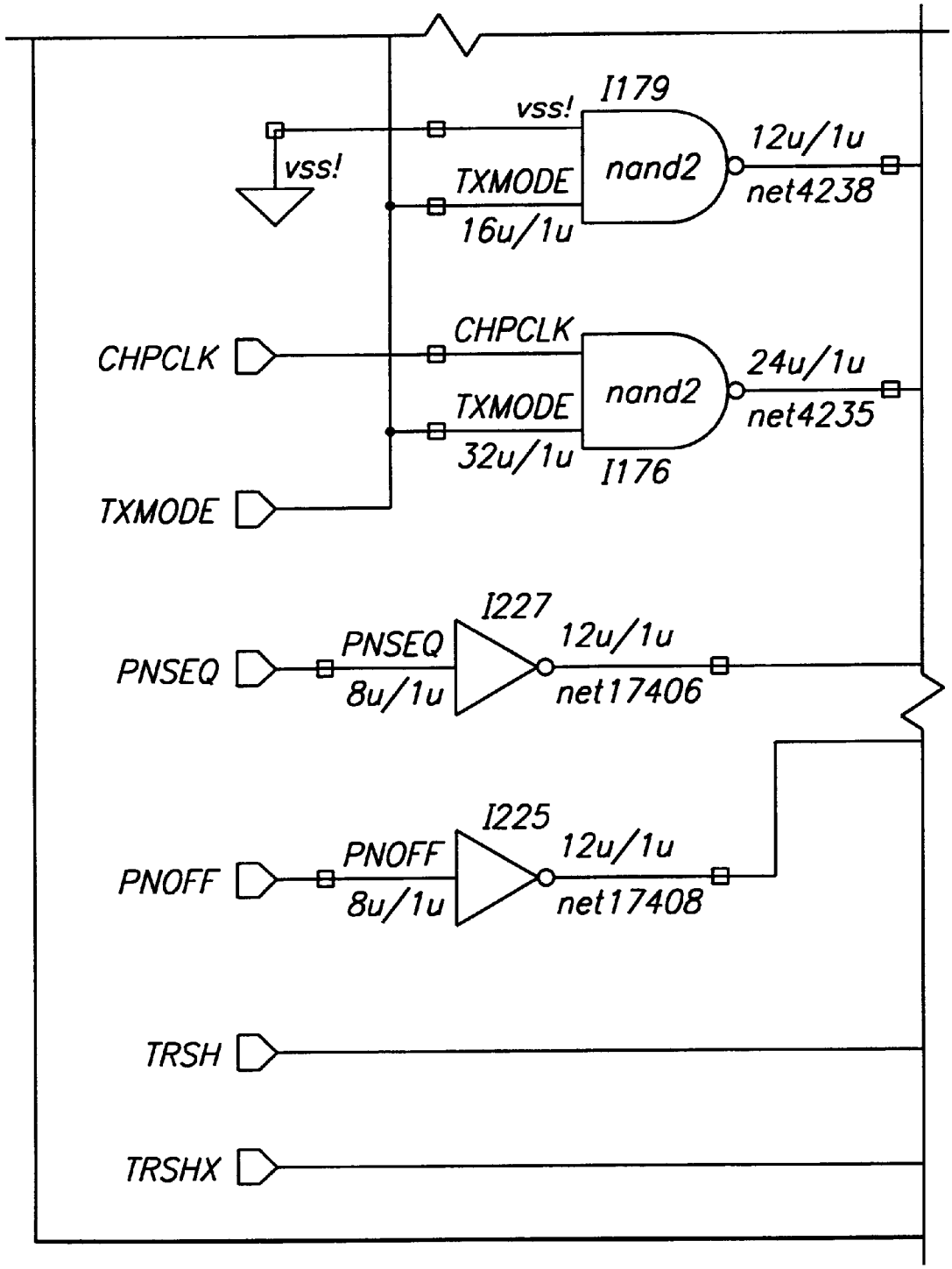

I179
vss!
vss!
12u/1u
TXMODE
nand2
net4238
16u/1u
CHPCLK
CHPCLK
24u/1u
TXMODE
nand2
net4235
32u/1u
I176
TXMODE
I227
PNSEQ
PNSEQ
12u/1u
8u/1u
net17406
I225
PNOFF
PNOFF
12u/1u
8u/1u
net17408
TRSH
TRSHX

Fig 10.0600A

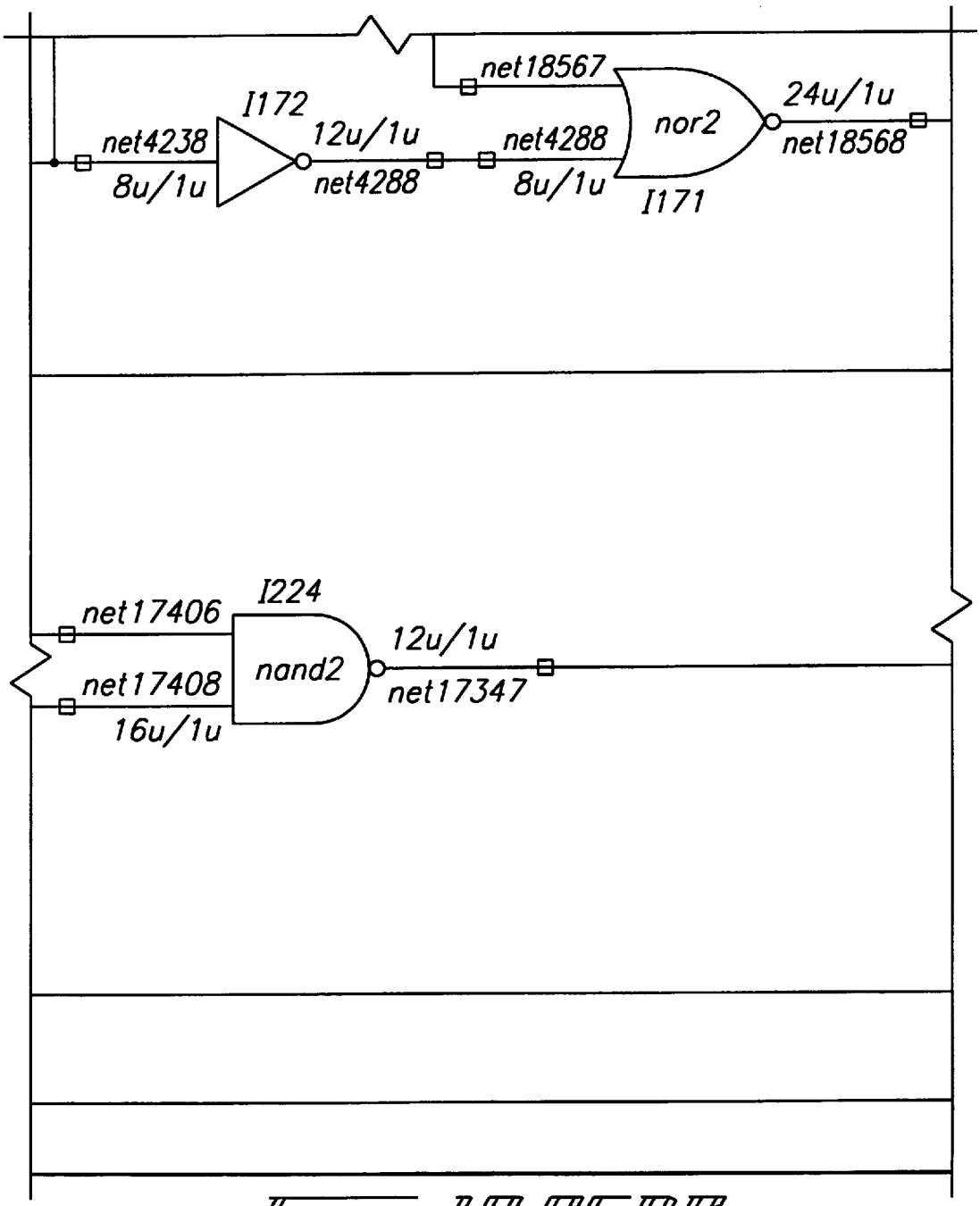

net18567
I172
net4238
8u/1u
12u/1u
net4288
net4288
8u/1u
nor2
I171
24u/1u
net18568
I224
net17406
net17408
16u/1u
nand2
12u/1u
net17347

Fig 10.0608

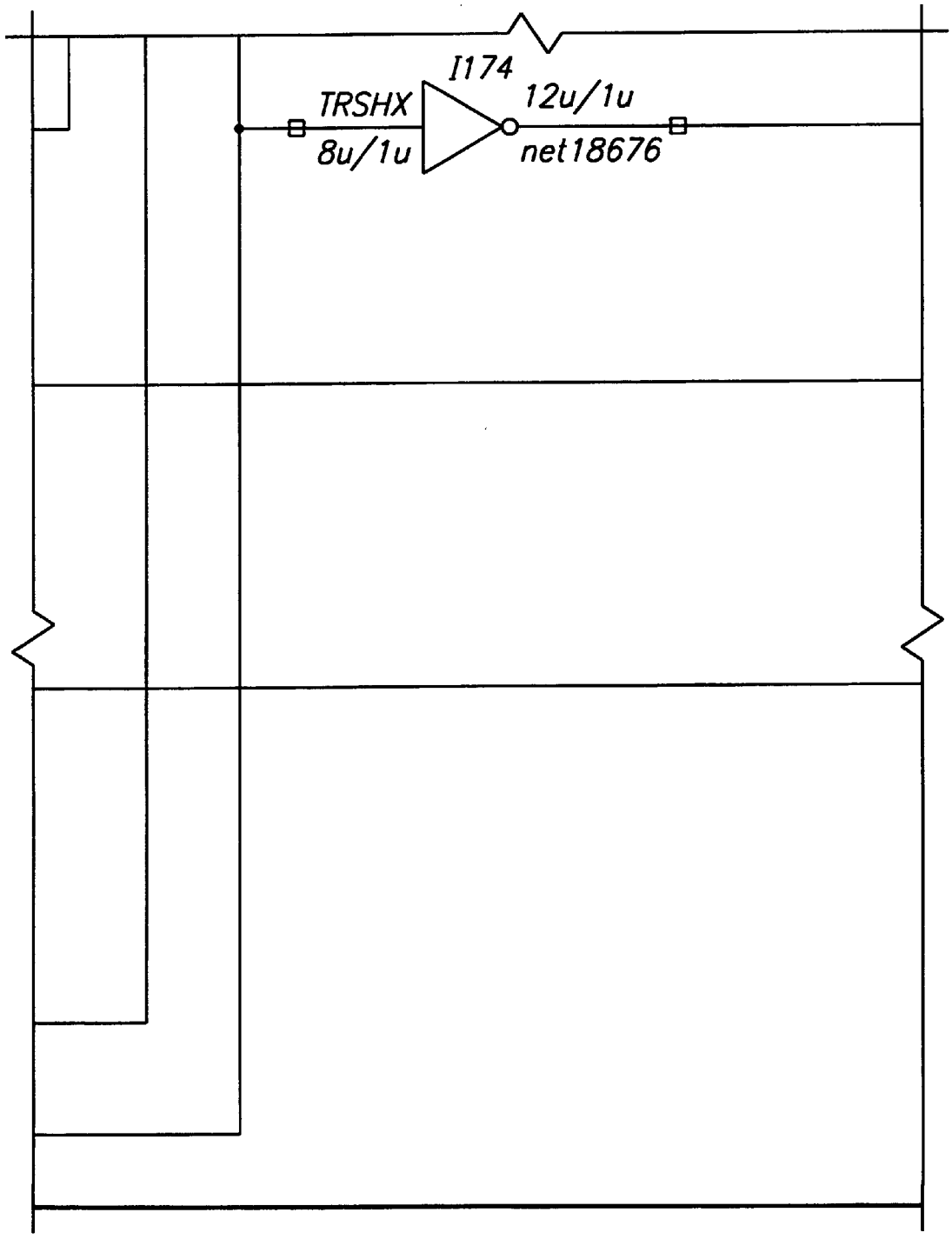


Fig 10.0600

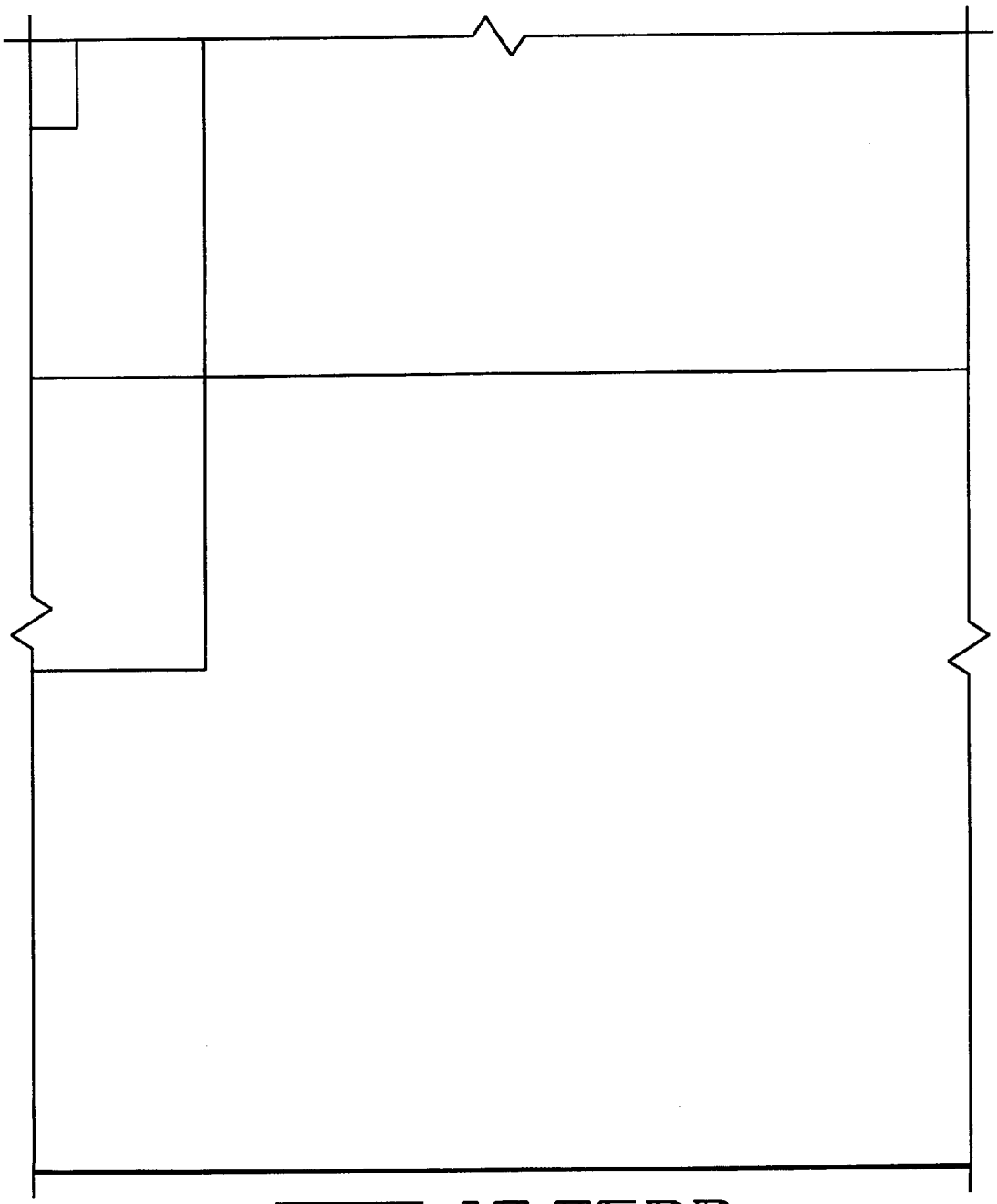


Fig 10.0600

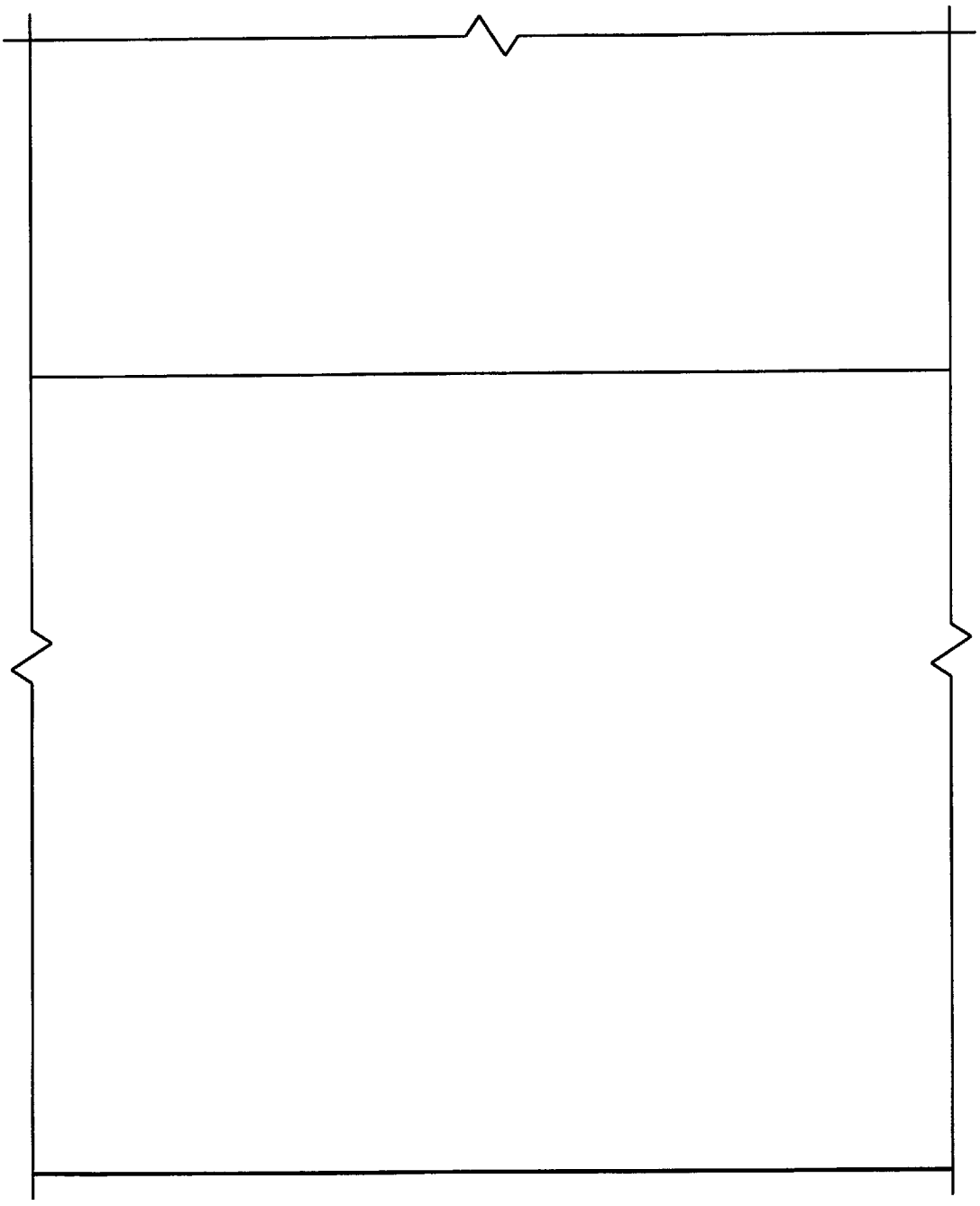


Fig 10.06DE

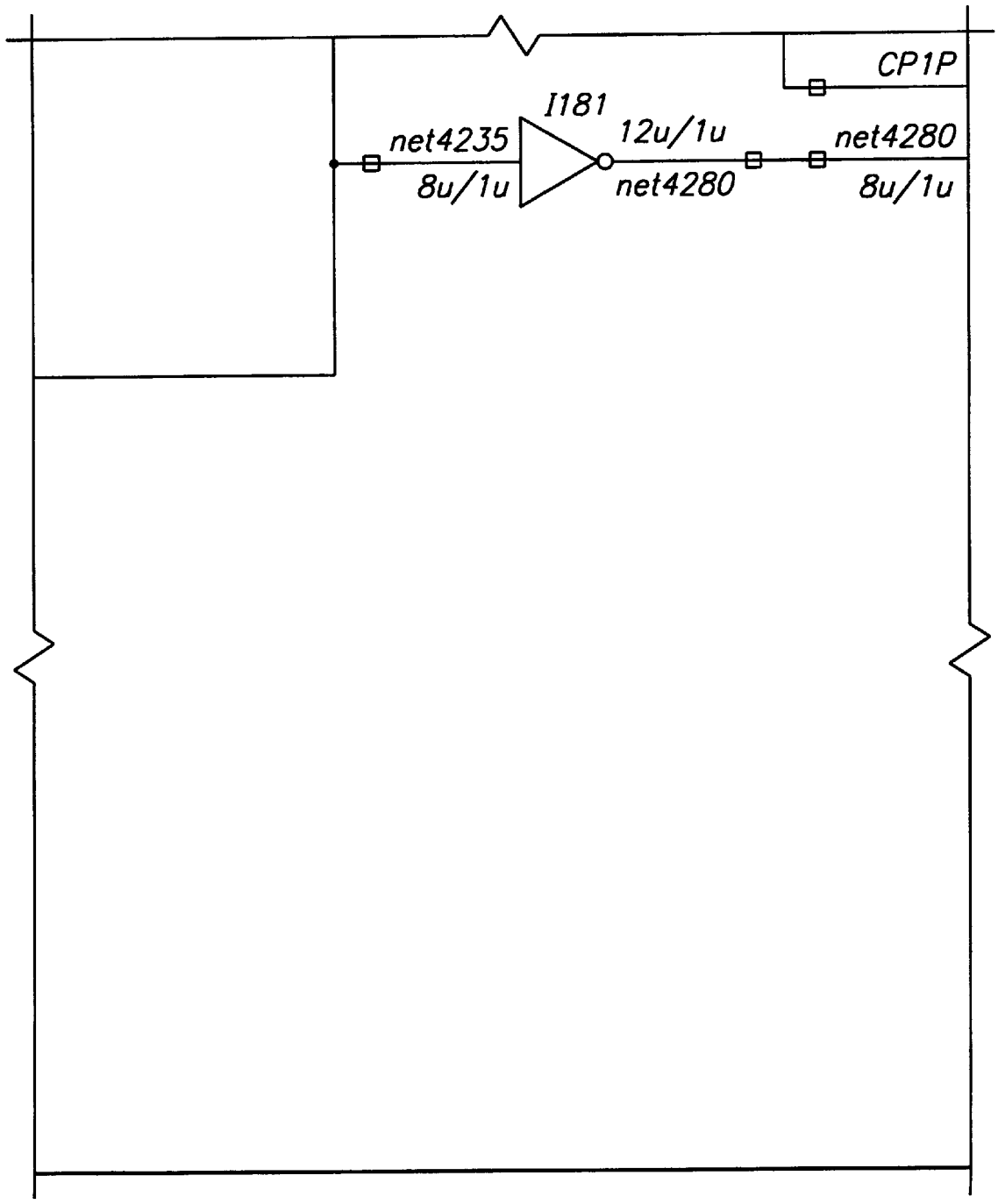


Fig 10.06DF

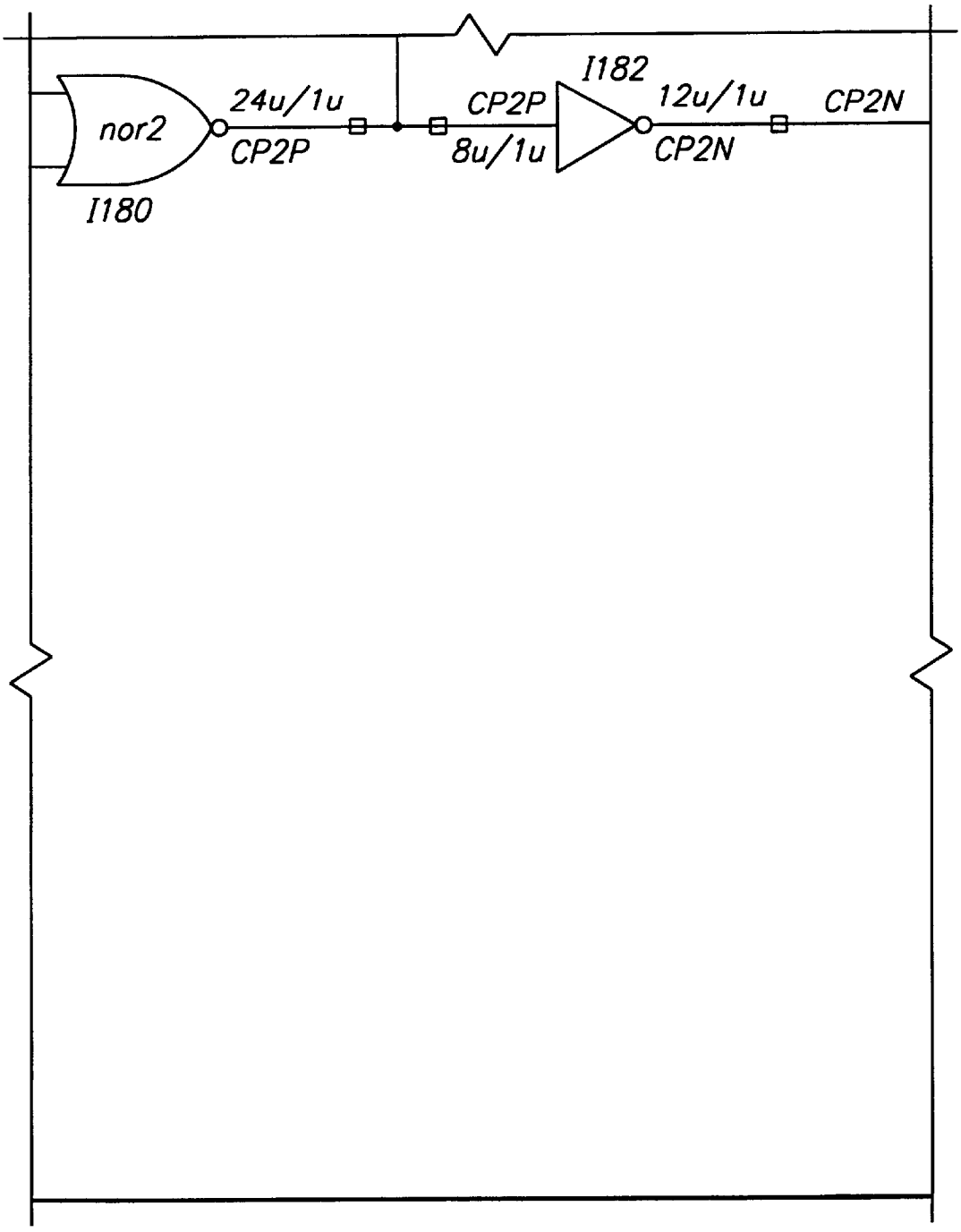


Fig 10.0606

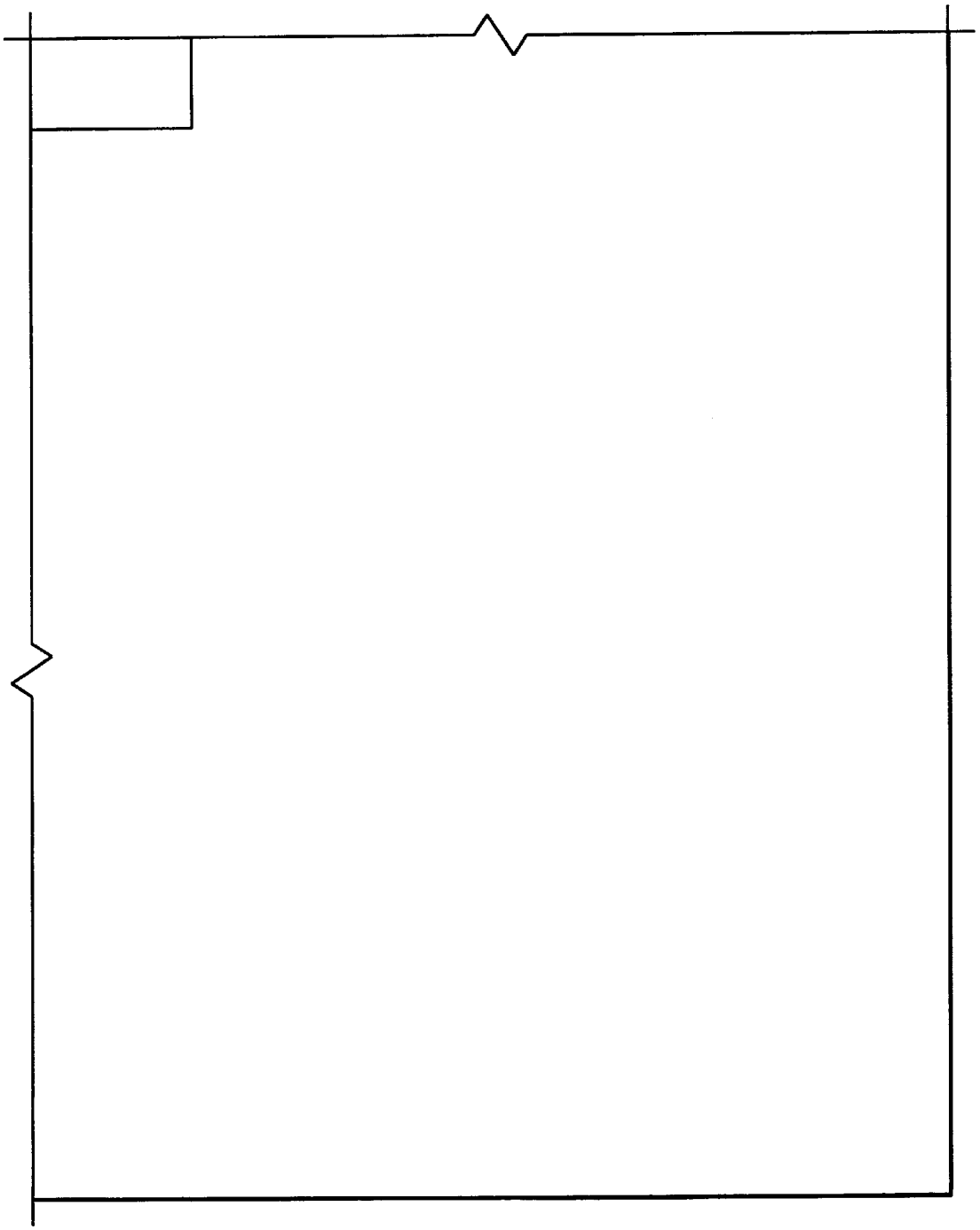


Fig 10.06DH

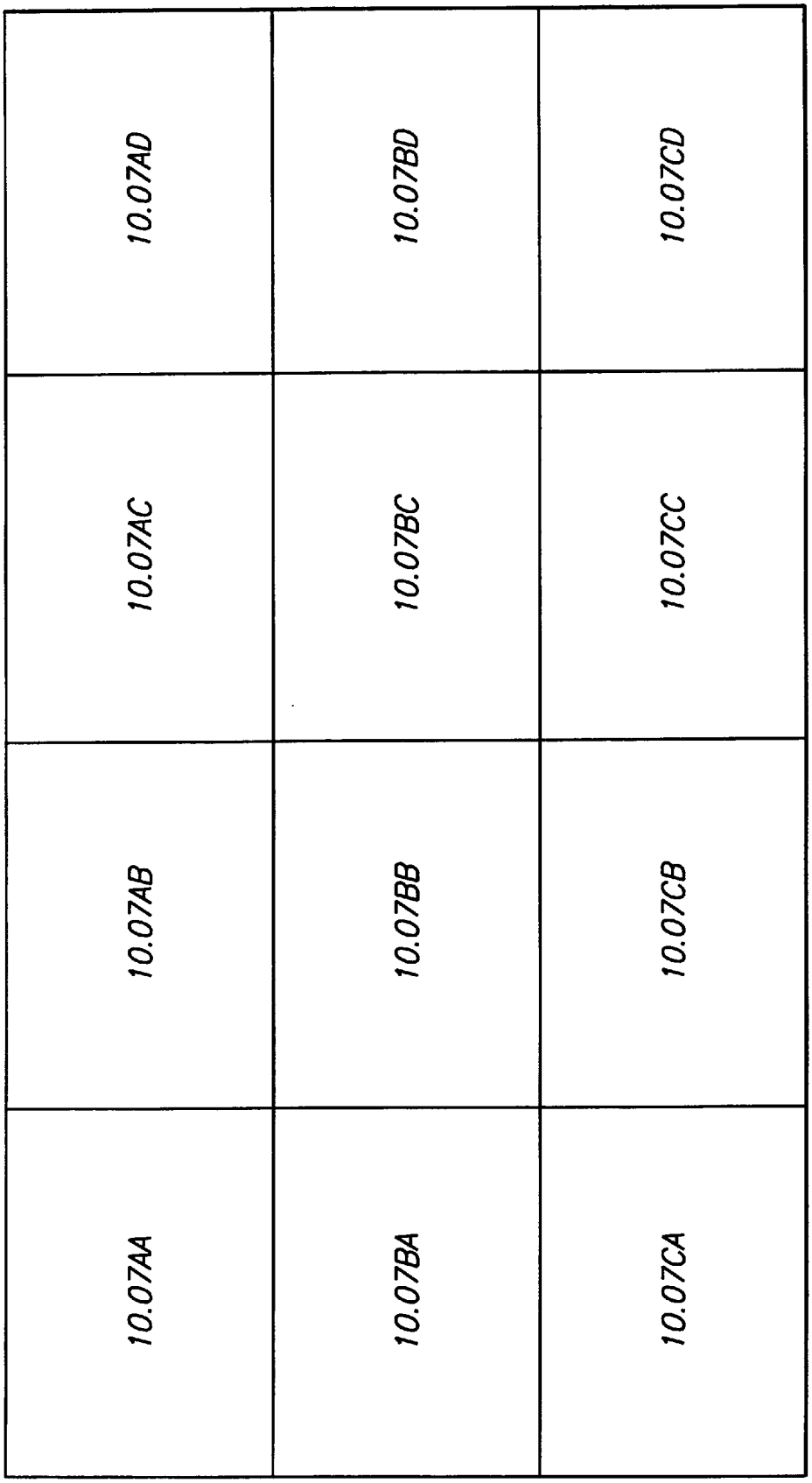

10.07AD
10.07BD
10.07CD
10.07AC
10.07BC
10.07CC
10.07AB
10.07BB
10.07CB
10.07AA
10.07BA
10.07CA

FIG. 10.07L

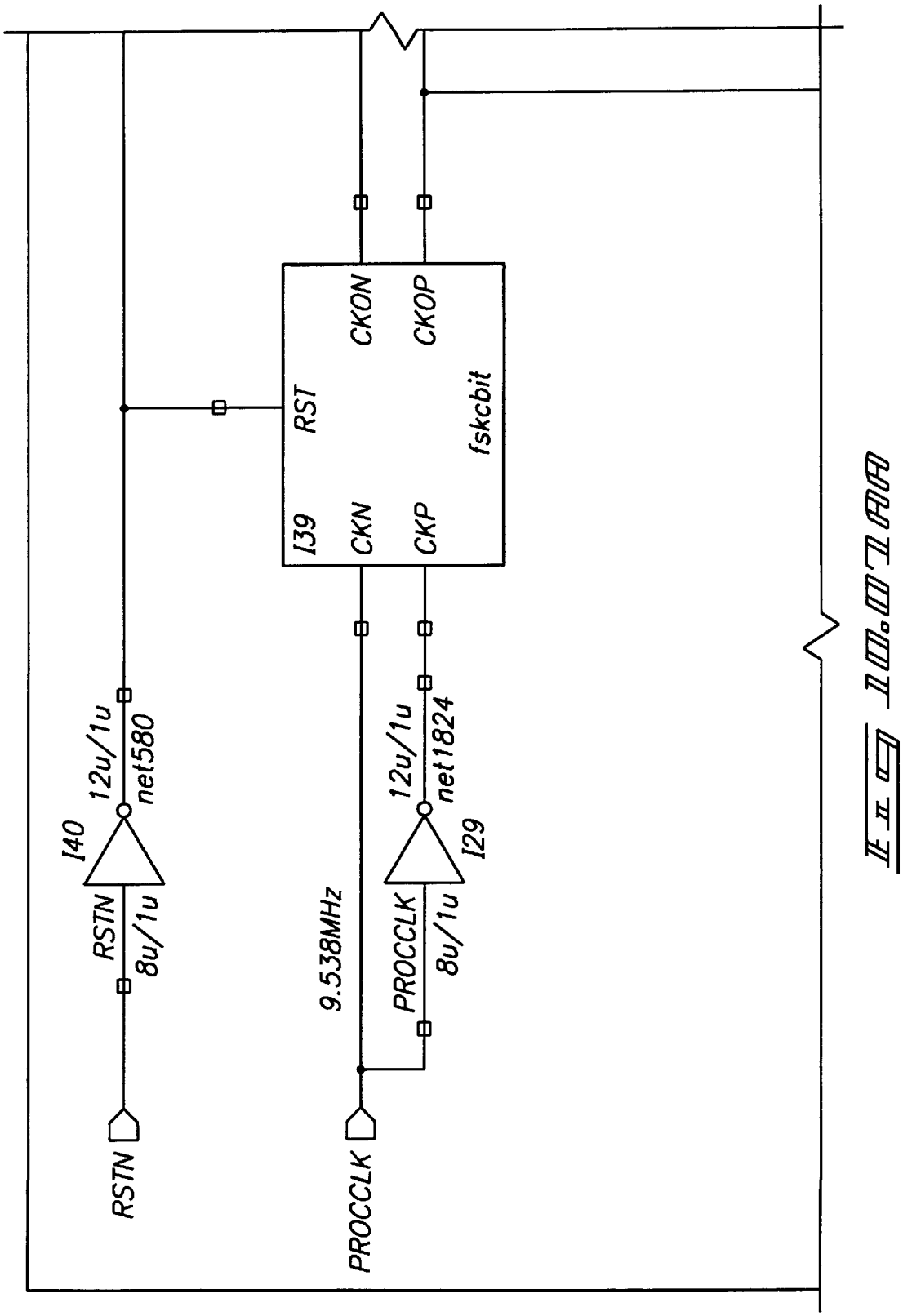


FIG. 100.001AA

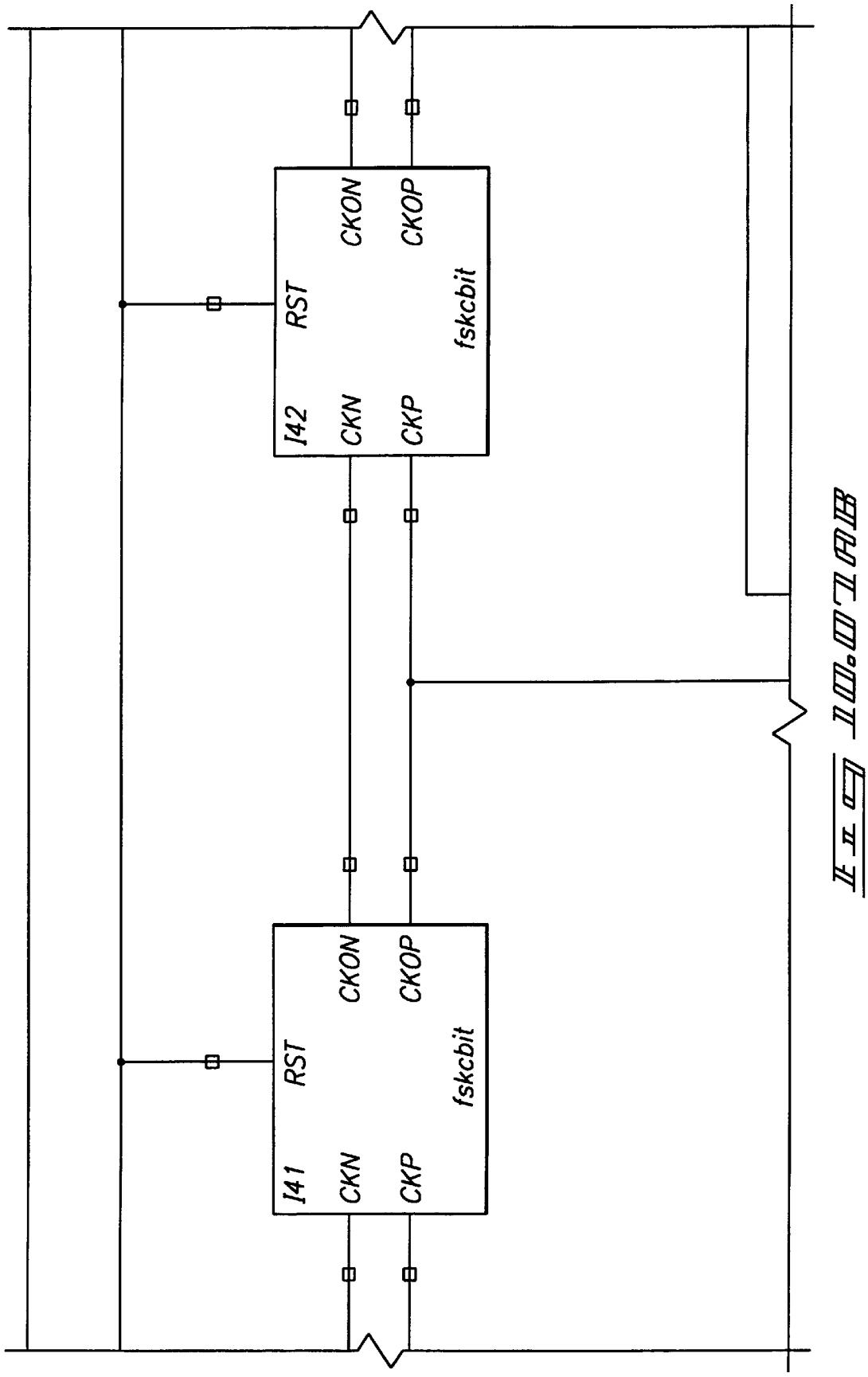
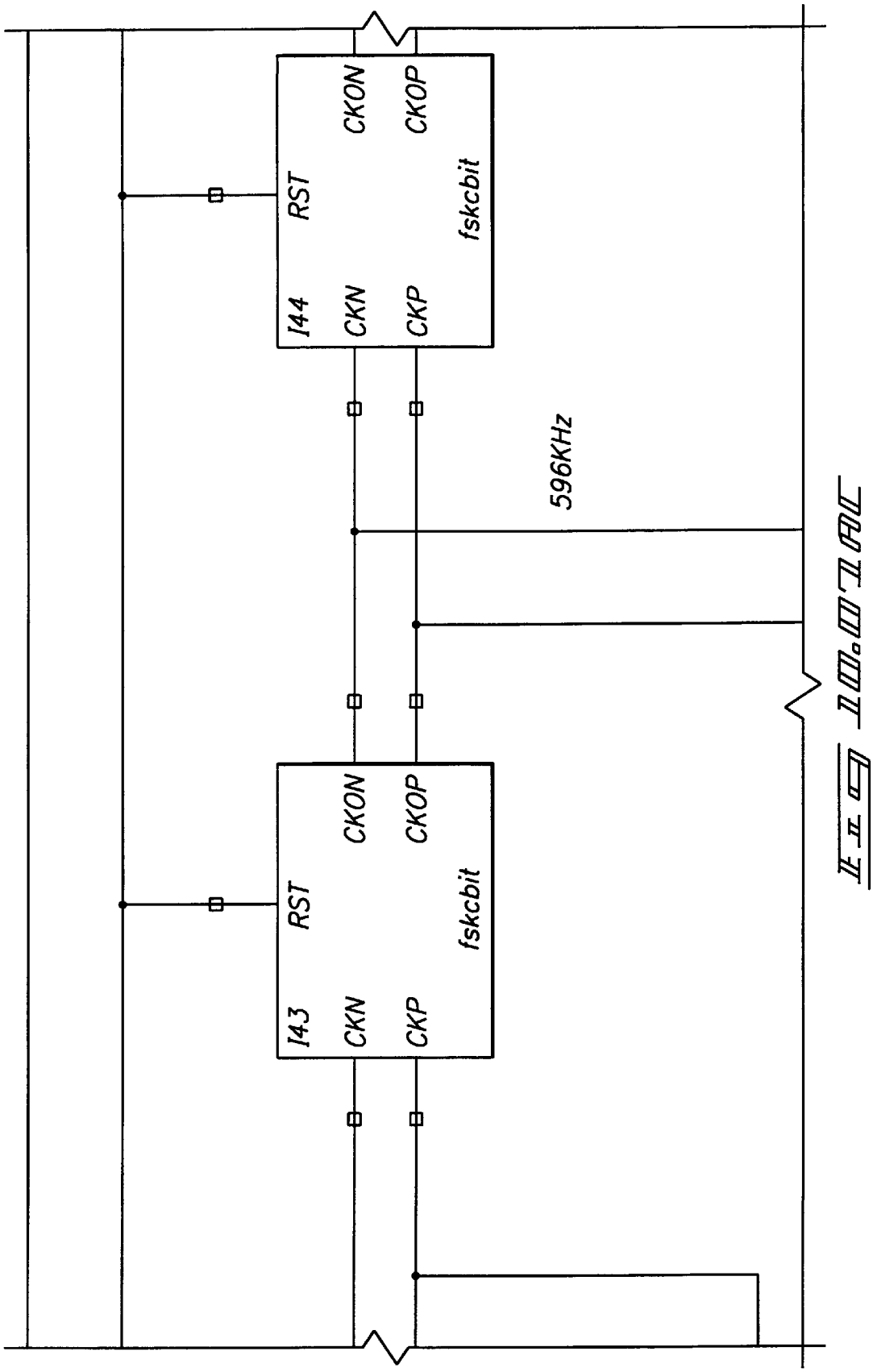
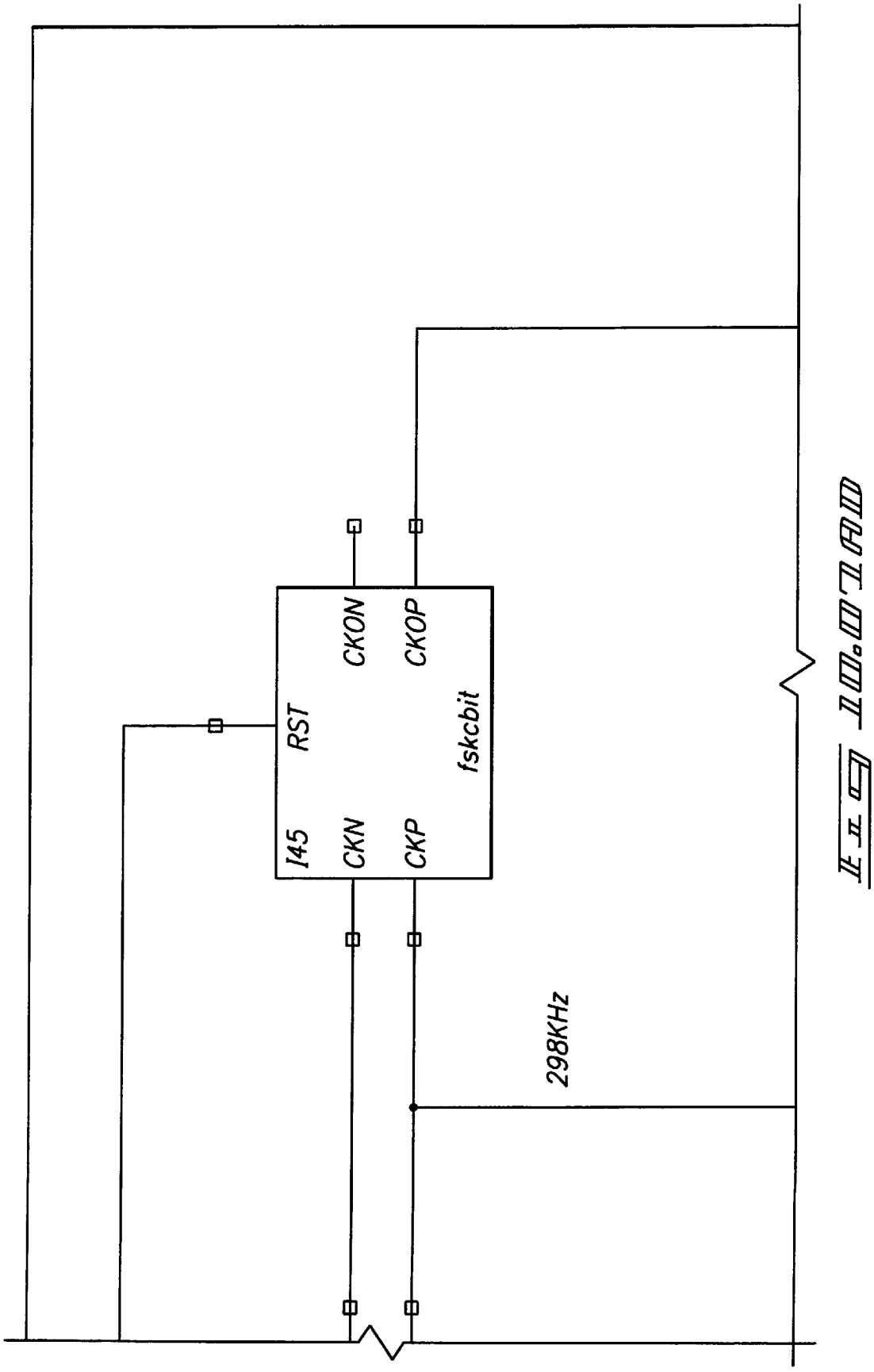

I42
RST
CKN
CKP
CKON
CKOP
fskcbit
I41
RST
CKN
CKP
CKON
CKOP
fskcbit

FIG 1,000,011


CKON
CKOP
RST
fskcbit
I44
CKN
CKP
596KHz
CKON
CKOP
RST
fskcbit
I43
CKN
CKP


CKON
CKOP
RST
fskcbit
I45
CKN
CKP
298KHz

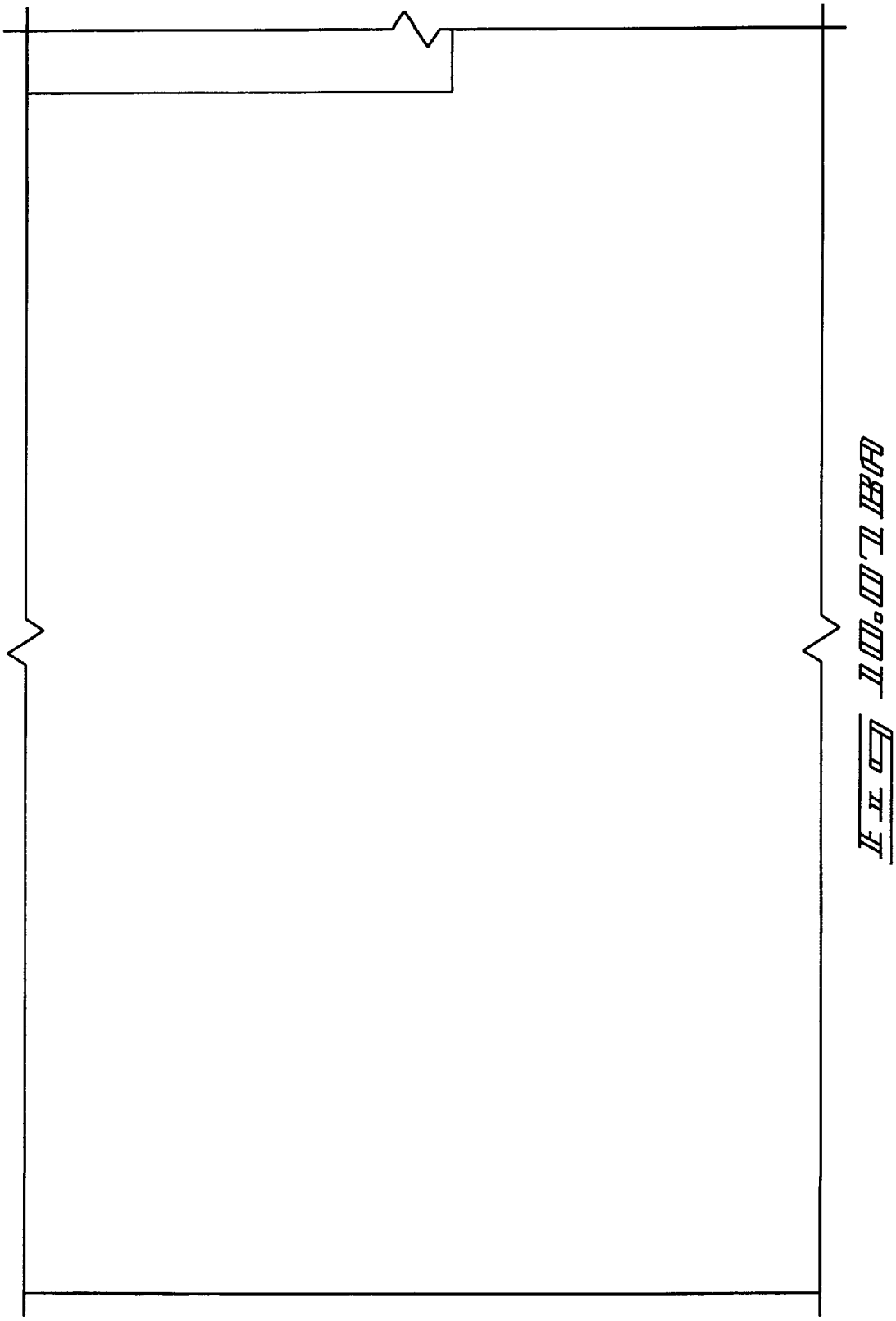


FIG 100,011

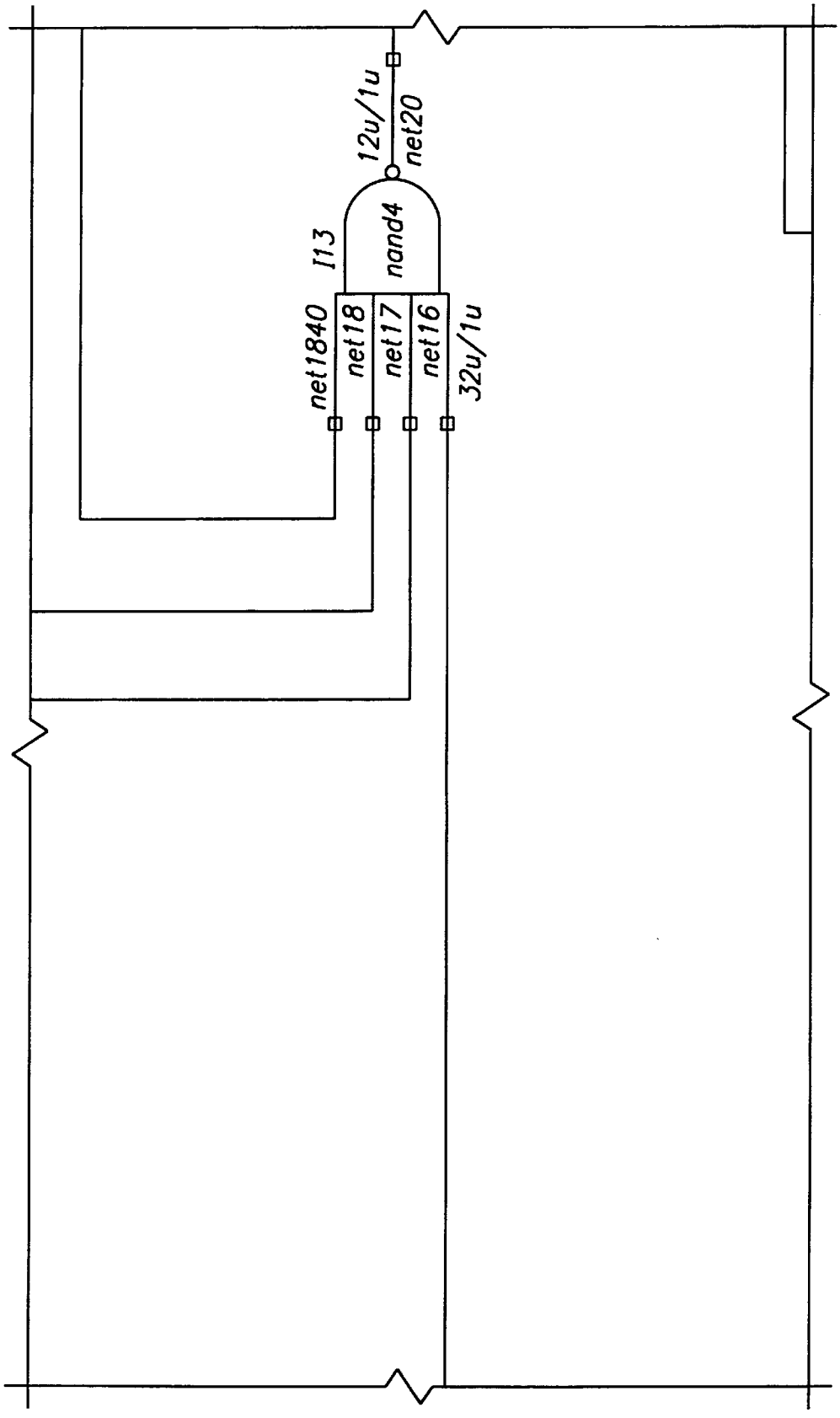


FIG 1100.001

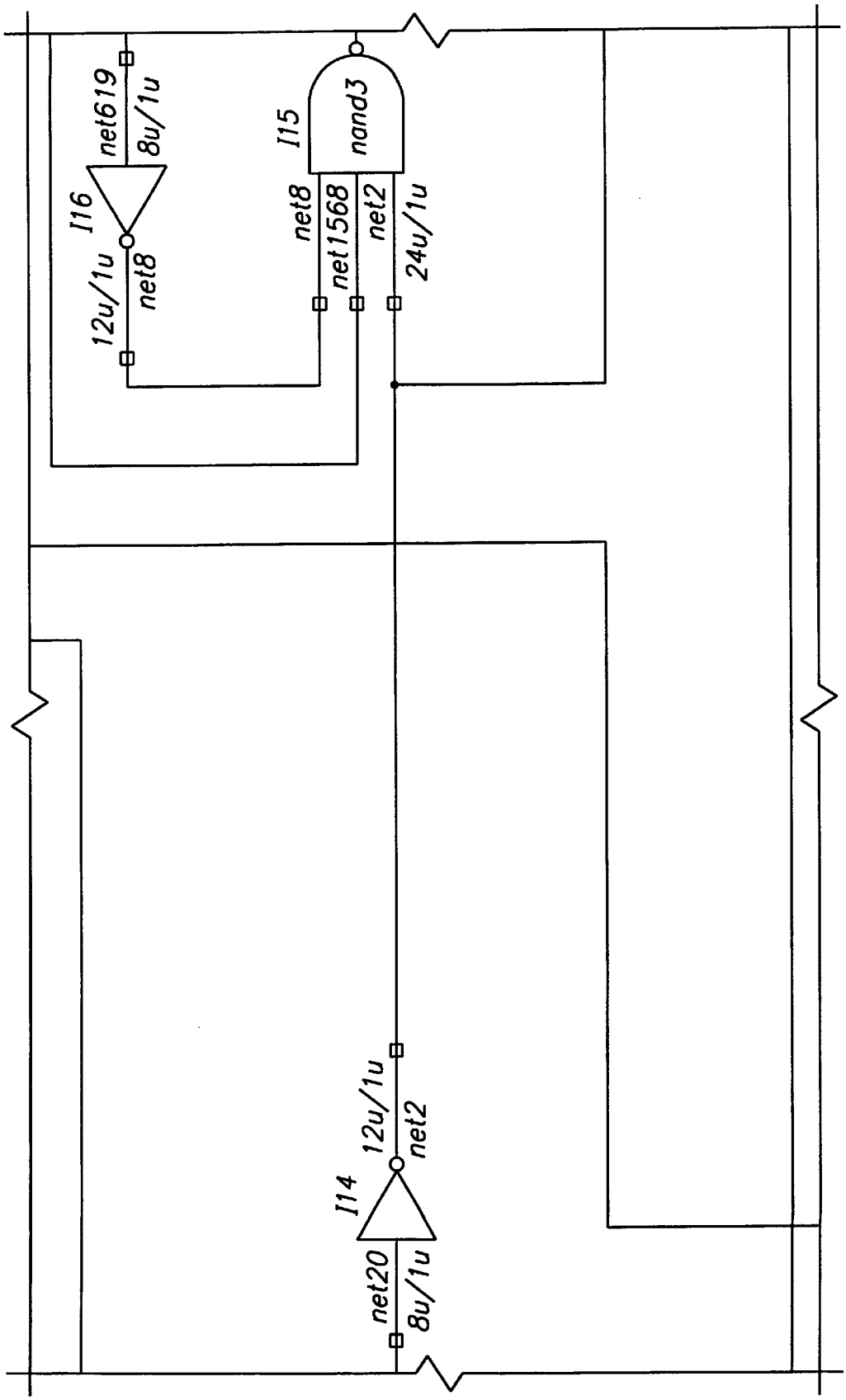

net619
8u/1u
I16
12u/1u
net8
I15
nand3
net8
net1568
net2
24u/1u
I14
12u/1u
net2
net20
8u/1u

FIG 100,001

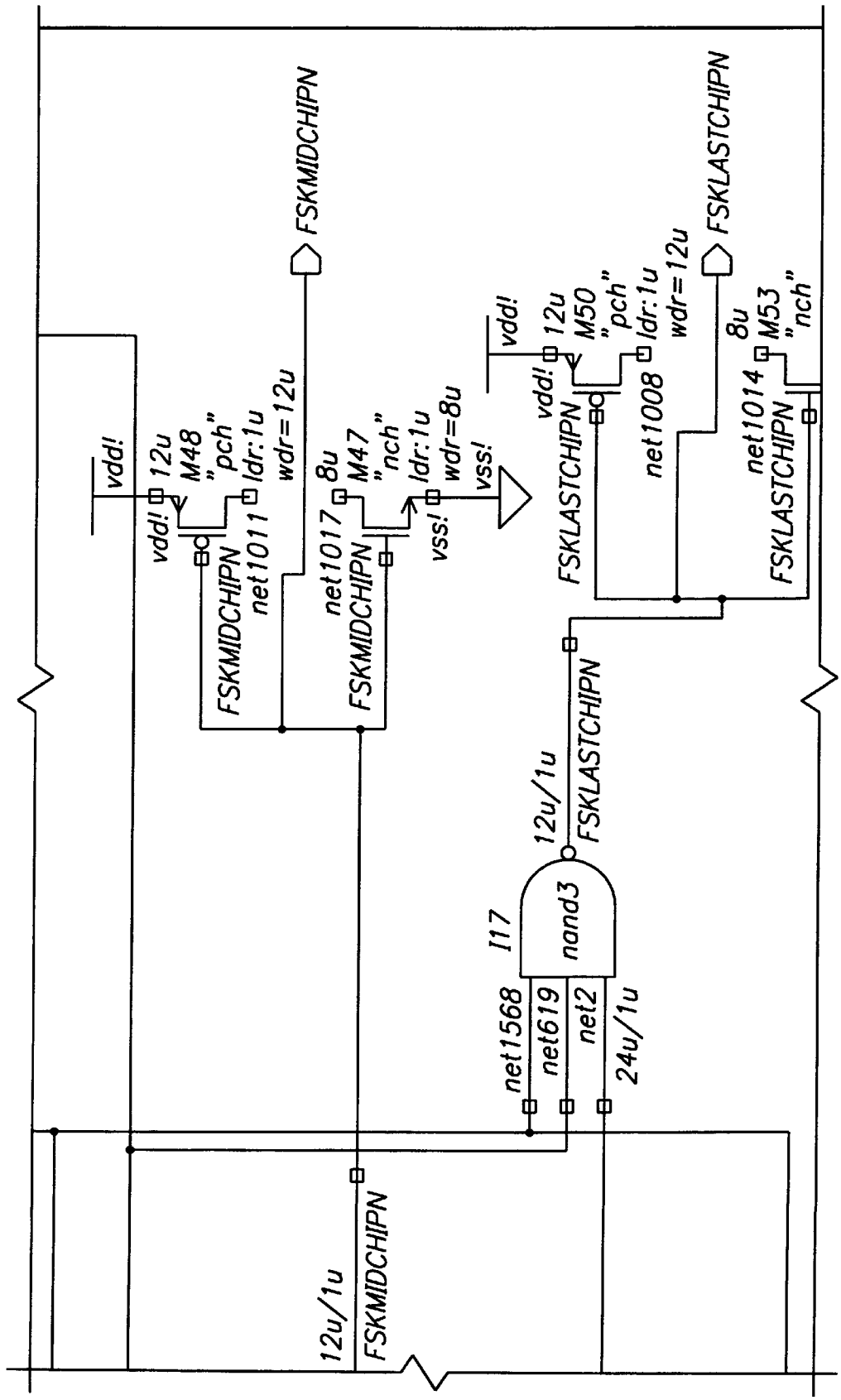
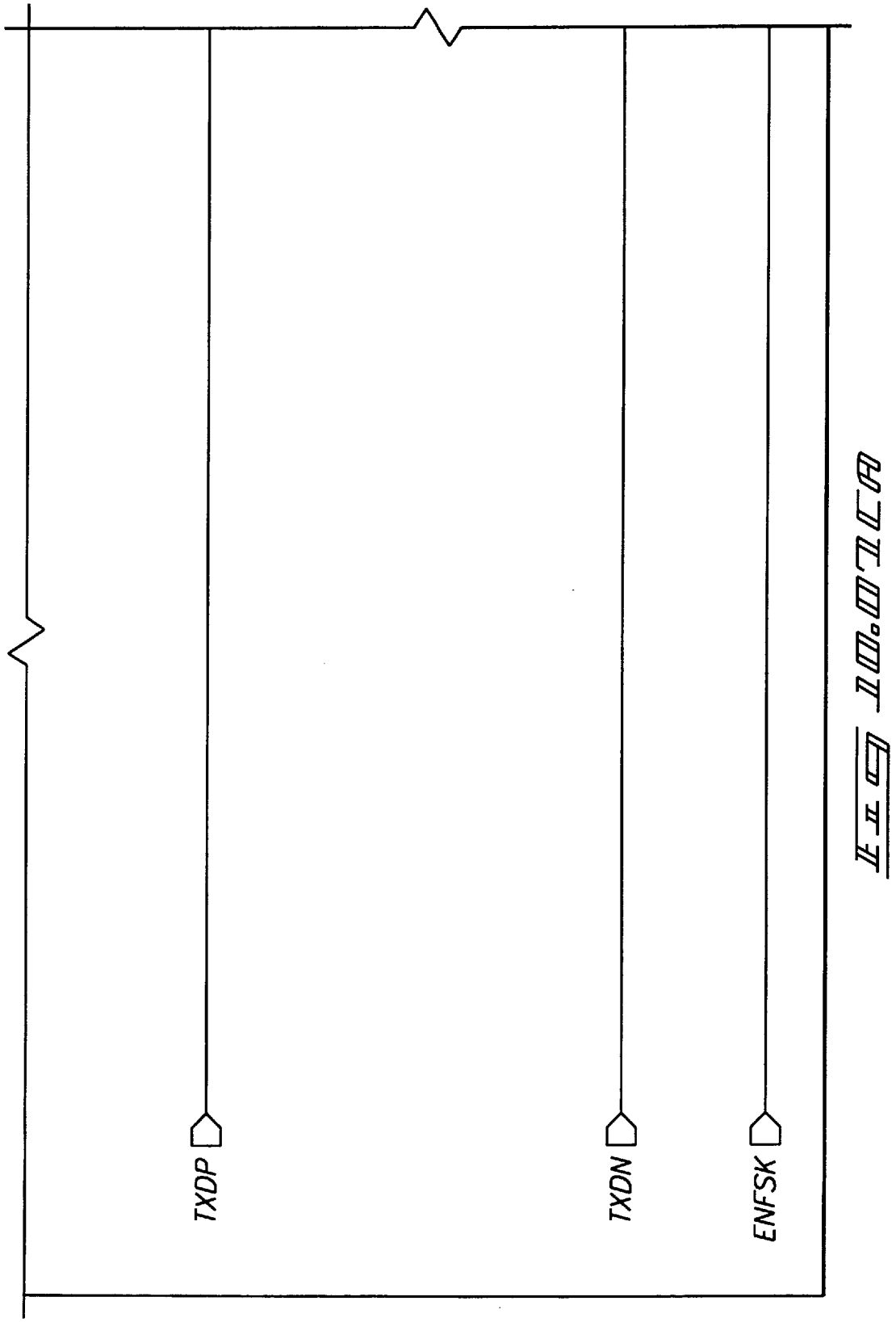
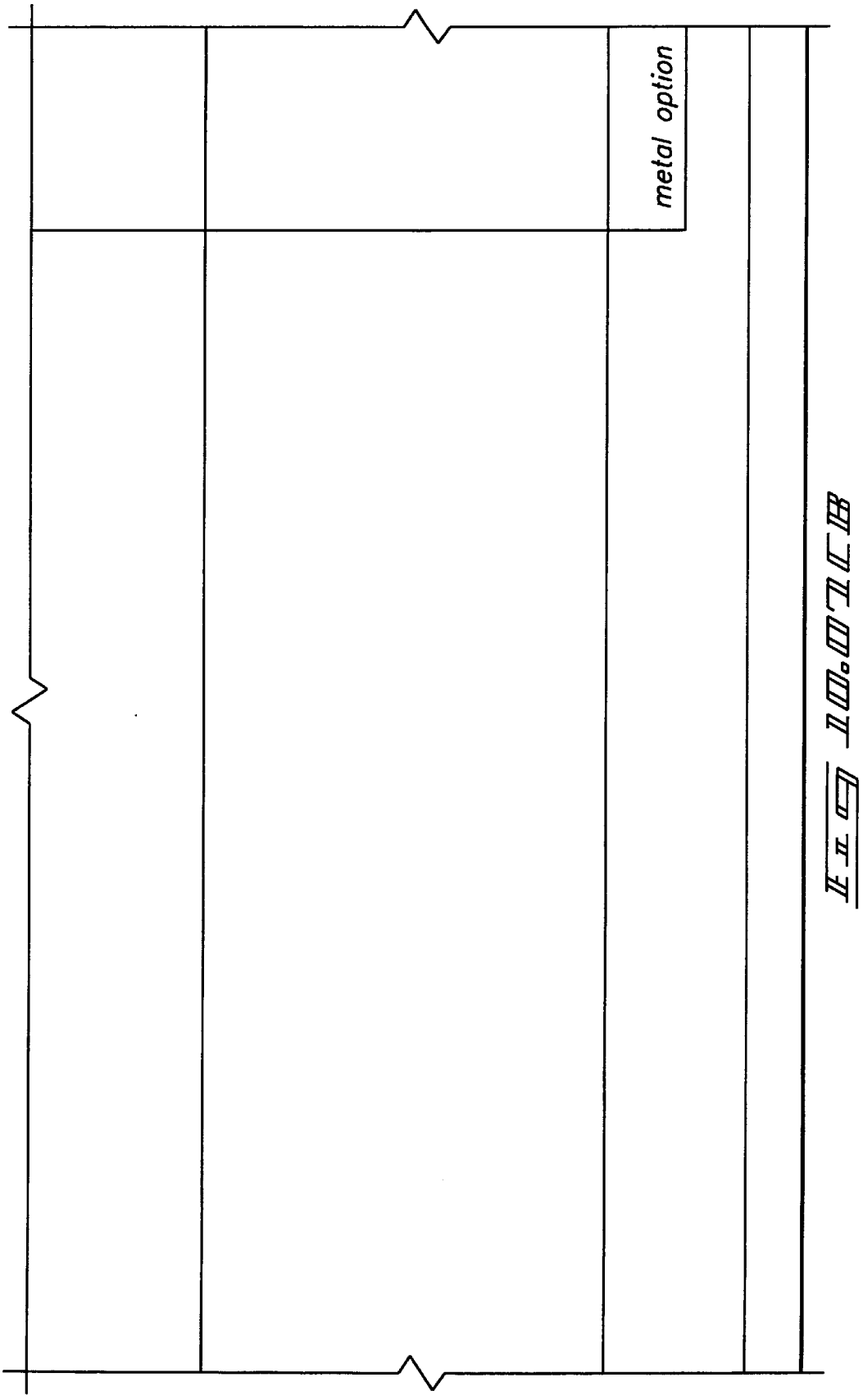


FIG. 100,011 IBM


TXDP
TXDN
ENFSK
FIG. 100,011


metal option
FIG. 100,611

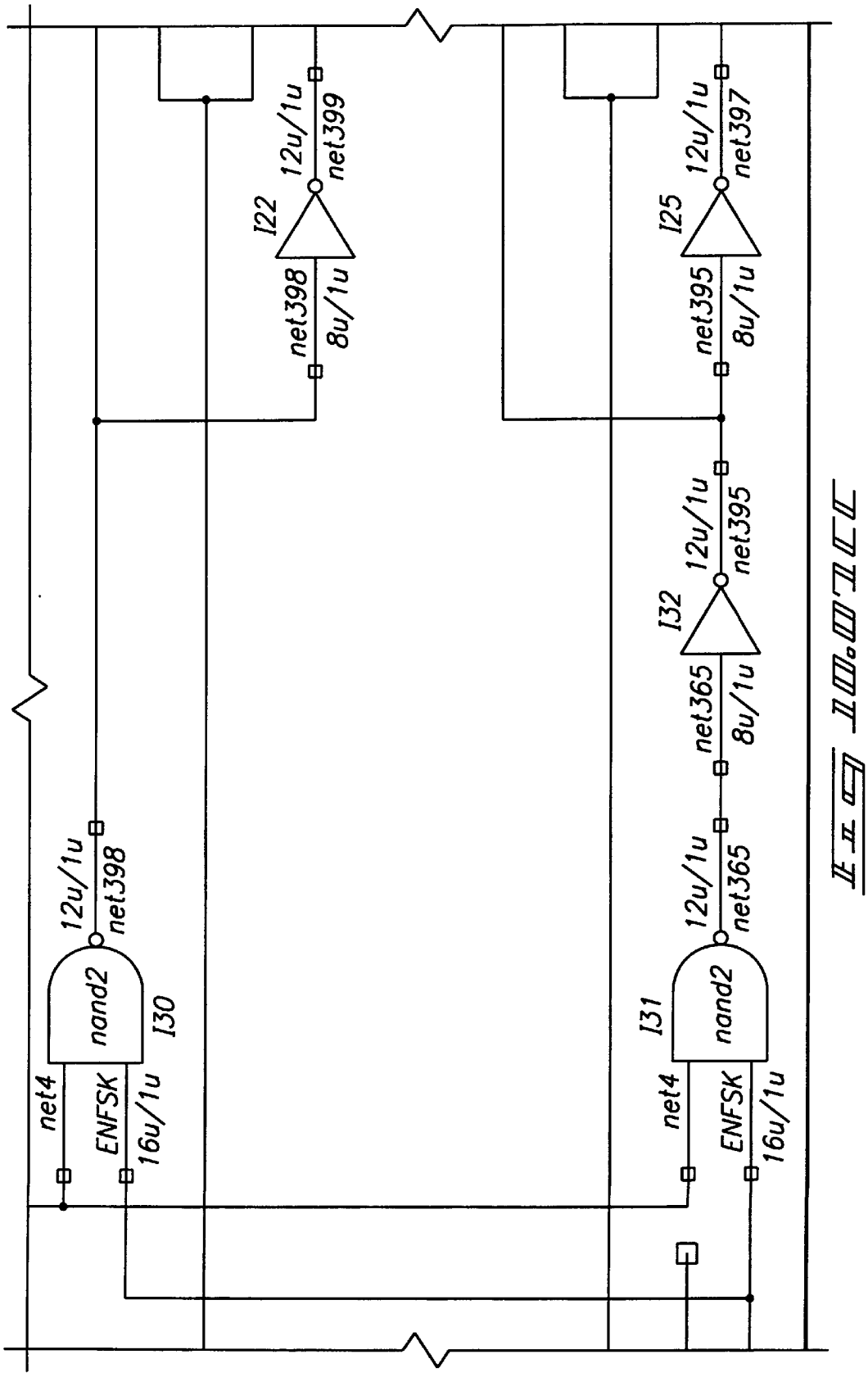

I30
nand2
12u/1u
net398
net4
ENFSK
16u/1u
I31
nand2
12u/1u
net365
net4
ENFSK
16u/1u
I22
12u/1u
net399
net398
8u/1u
I25
12u/1u
net397
net395
8u/1u
I32
12u/1u
net395
net365
8u/1u

FIG. 100,011

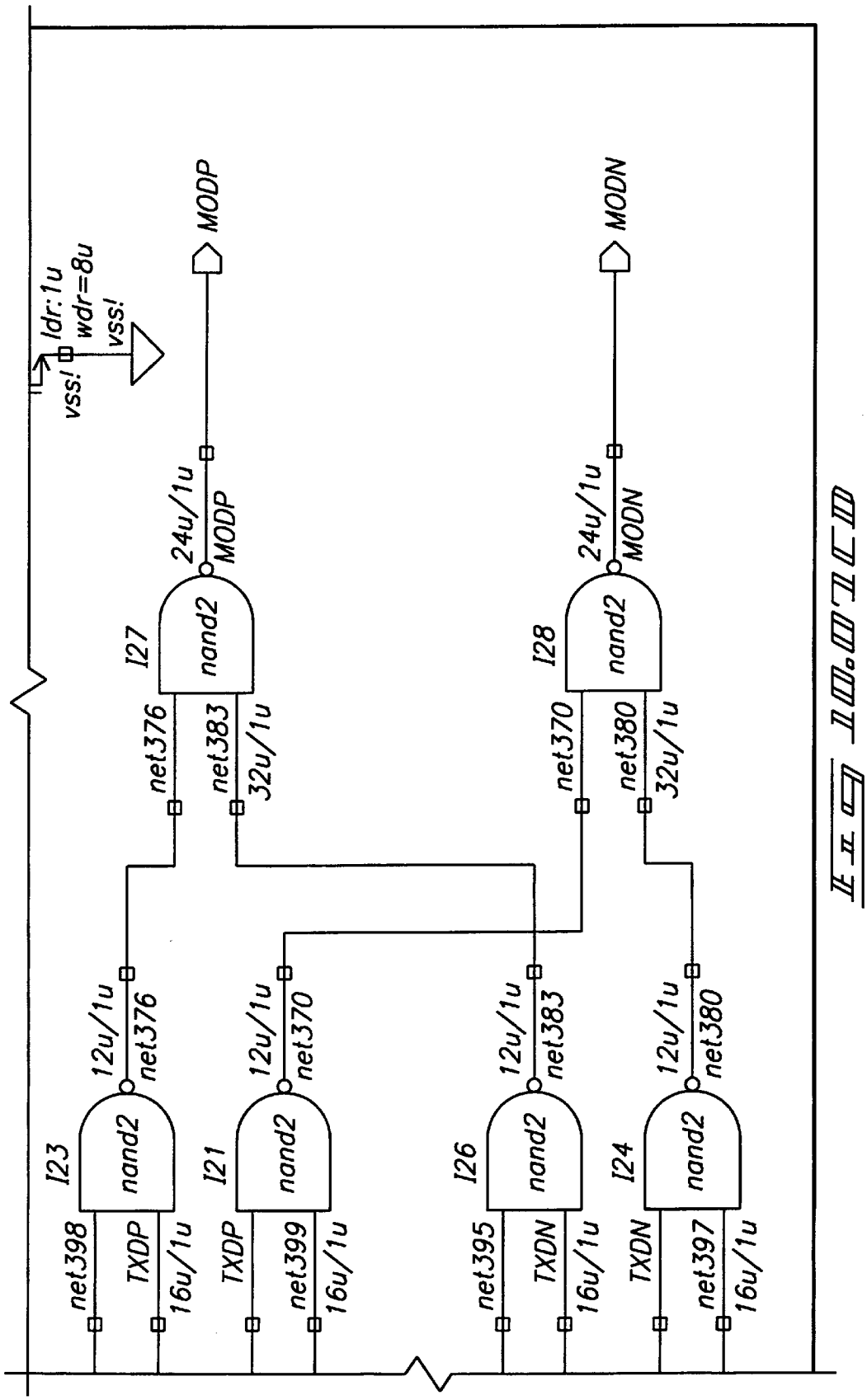
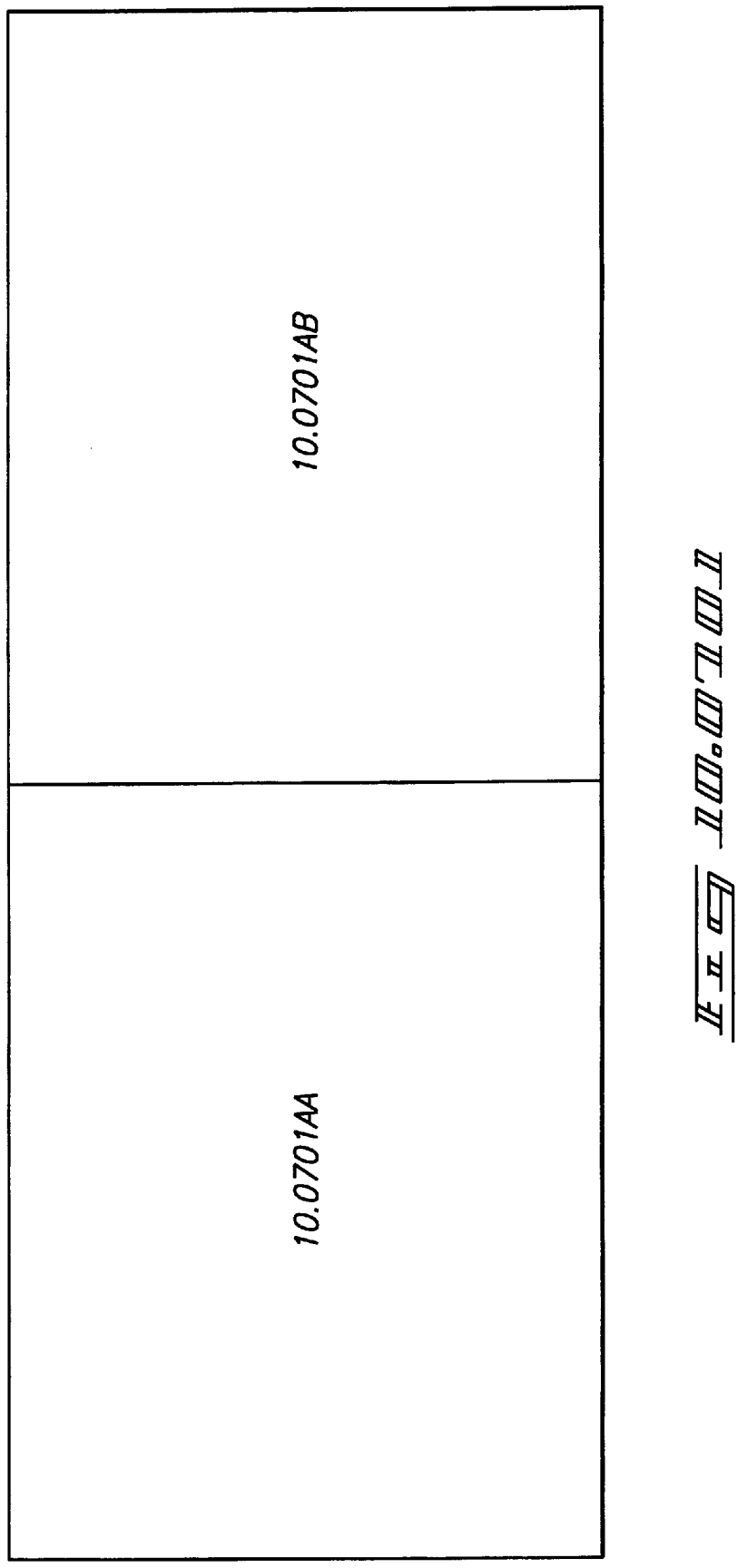

ldr:1u
wdr=8u
vss!
vss!
MODP
MODN
24u/1u
MODP
MODN
I27
I28
nand2
net376
net383
net370
net380
32u/1u
12u/1u
I23
I21
I26
I24
net398
net399
net395
net397
TXDP
TXDN
16u/1u

FIG 100


10.0701AB
10.0701AA
TO 100.01 FEET

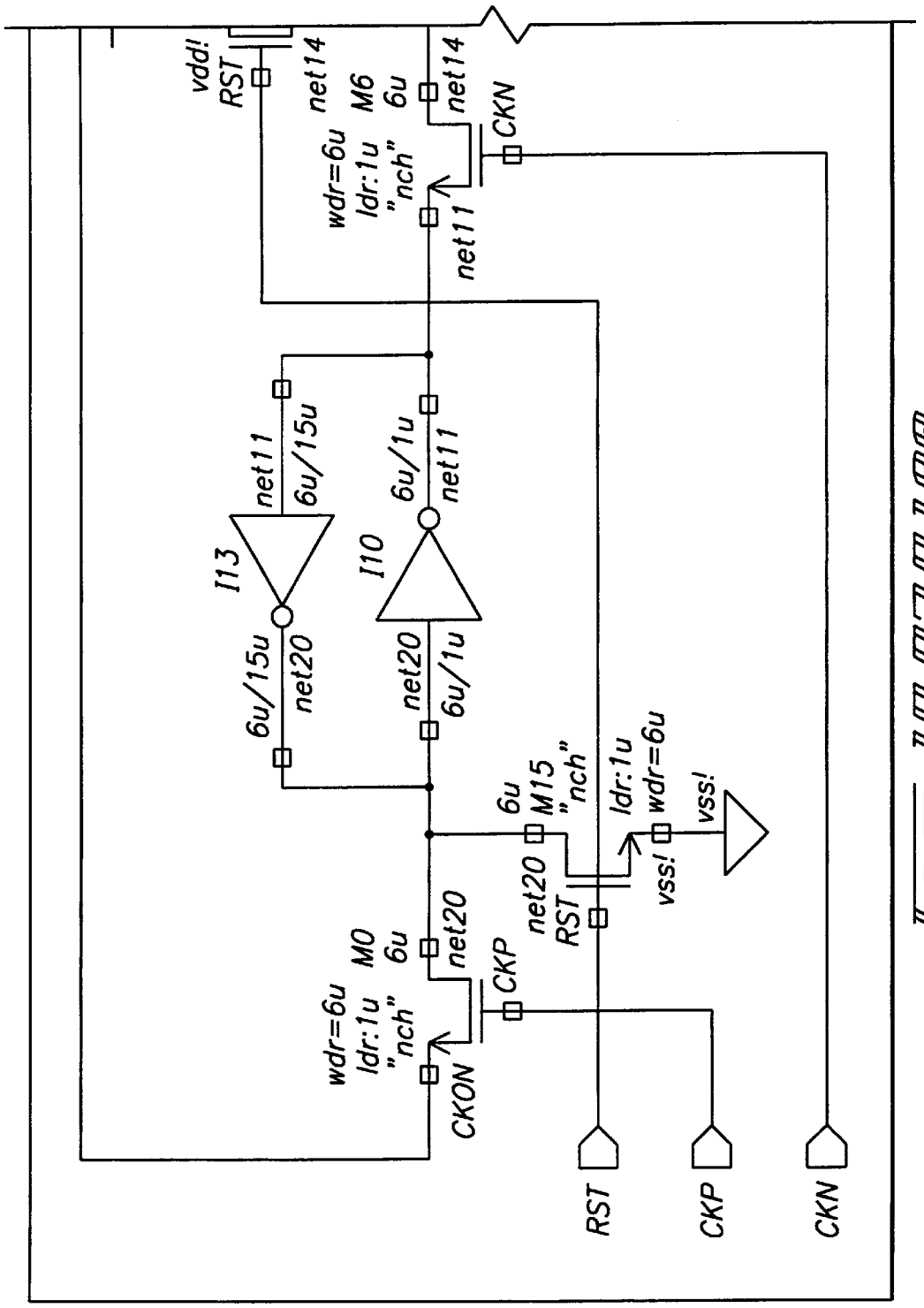
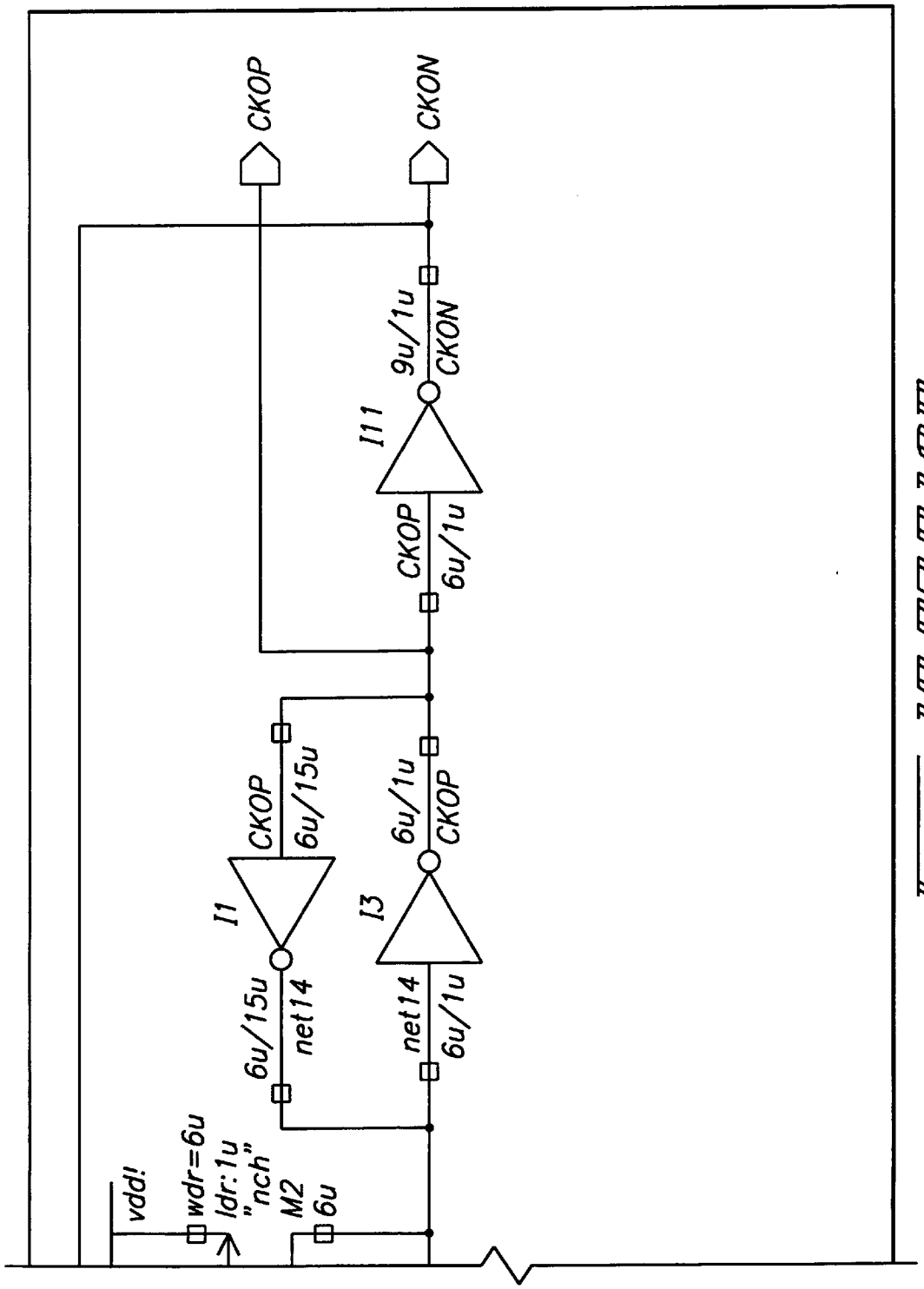


FIG 100,001AA



Фиг. 100.00111AIB

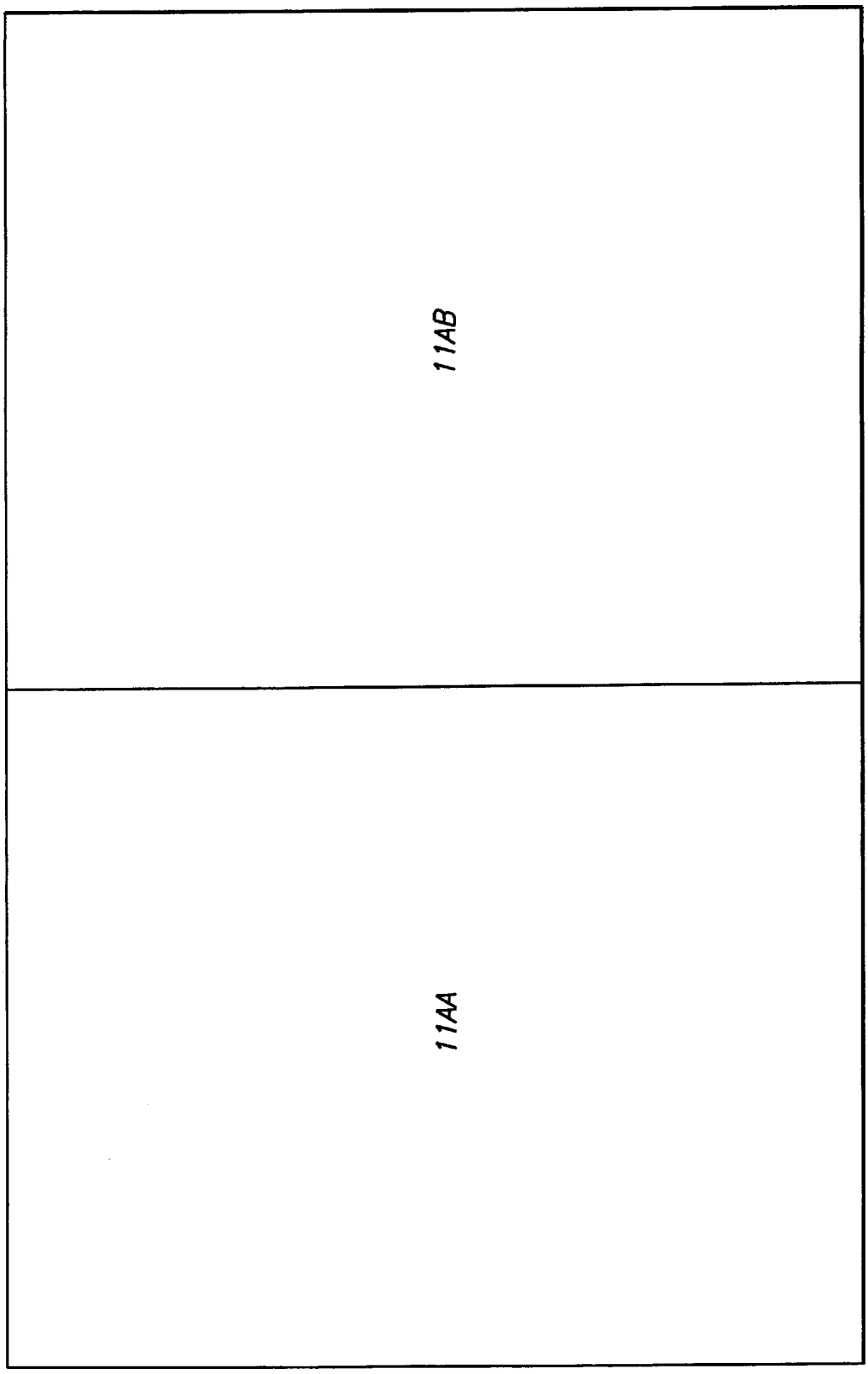


FIG 11

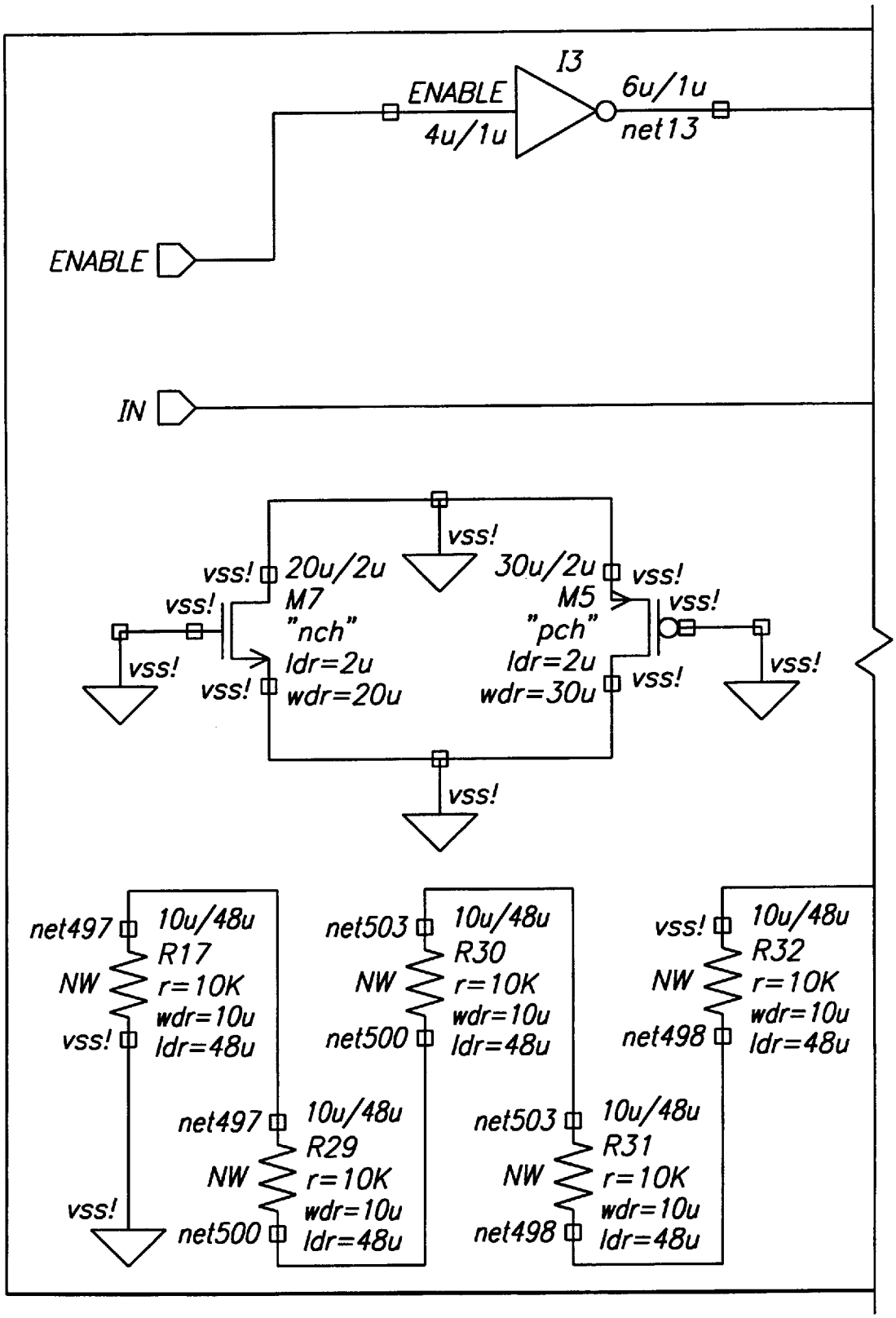

I3
ENABLE
4u/1u
6u/1u
net13
ENABLE
IN
vss!
vss!
20u/2u
M7
"nch"
ldr=2u
wdr=20u
vss!
vss!
30u/2u
M5
"pch"
ldr=2u
wdr=30u
vss!
vss!
vss!
vss!
vss!
net497
10u/48u
R17
NW
r=10K
wdr=10u
vss!
ldr=48u
net503
10u/48u
R30
NW
r=10K
wdr=10u
net500
ldr=48u
vss!
10u/48u
R32
NW
r=10K
wdr=10u
net498
ldr=48u
net497
10u/48u
R29
NW
r=10K
wdr=10u
vss!
net500
ldr=48u
net503
10u/48u
R31
NW
r=10K
wdr=10u
net498
ldr=48u

Fig 11AA

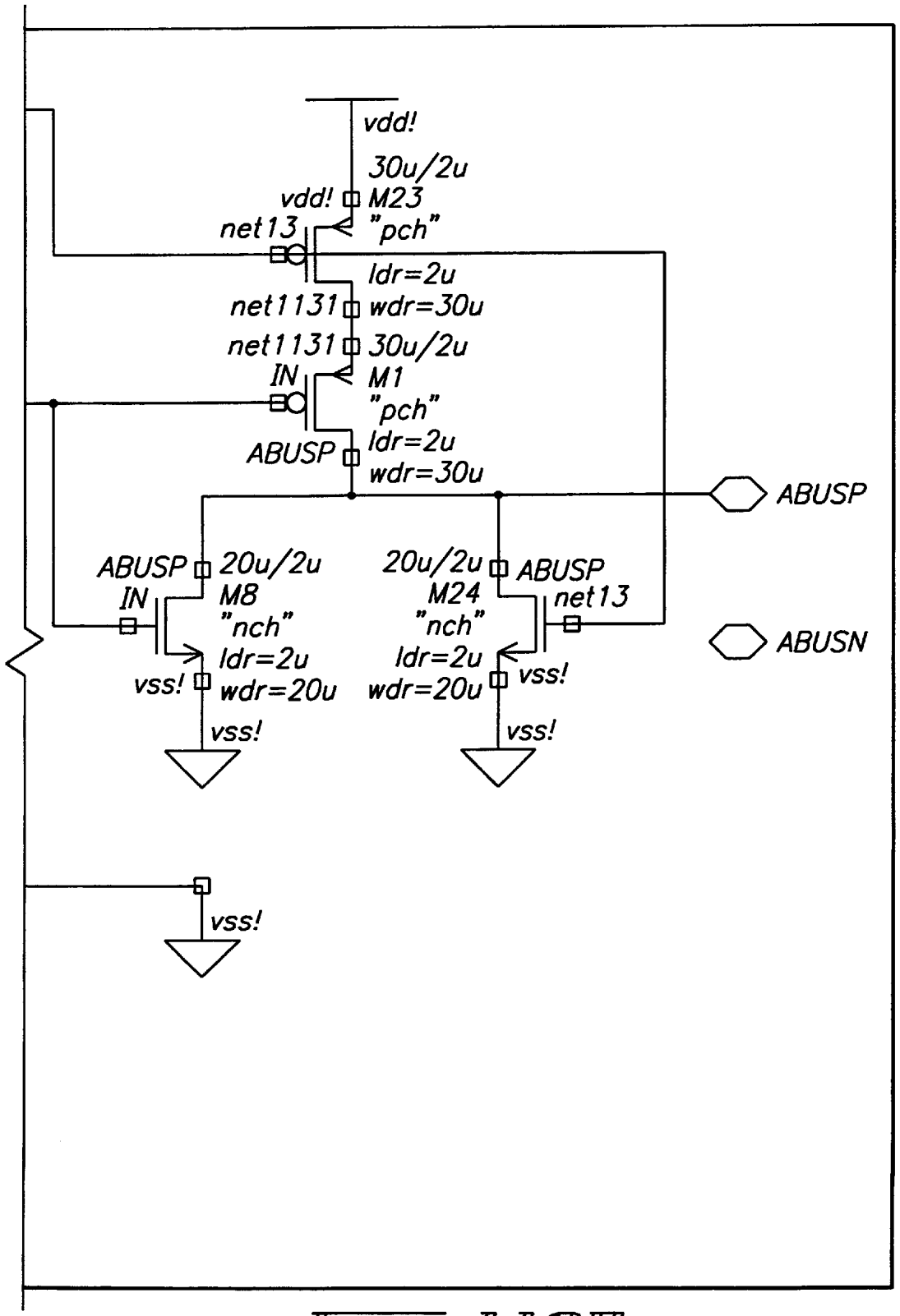

vdd!
30u/2u
vdd!
M23
net13
"pch"
ldr=2u
net1131
wdr=30u
net1131
30u/2u
IN
M1
"pch"
ldr=2u
ABUSP
wdr=30u
ABUSP
ABUSP
20u/2u
M8
IN
"nch"
ldr=2u
vss!
wdr=20u
vss!
20u/2u
M24
ABUSP
net13
"nch"
ldr=2u
wdr=20u
vss!
vss!
ABUSN
vss!

Fig 11AB

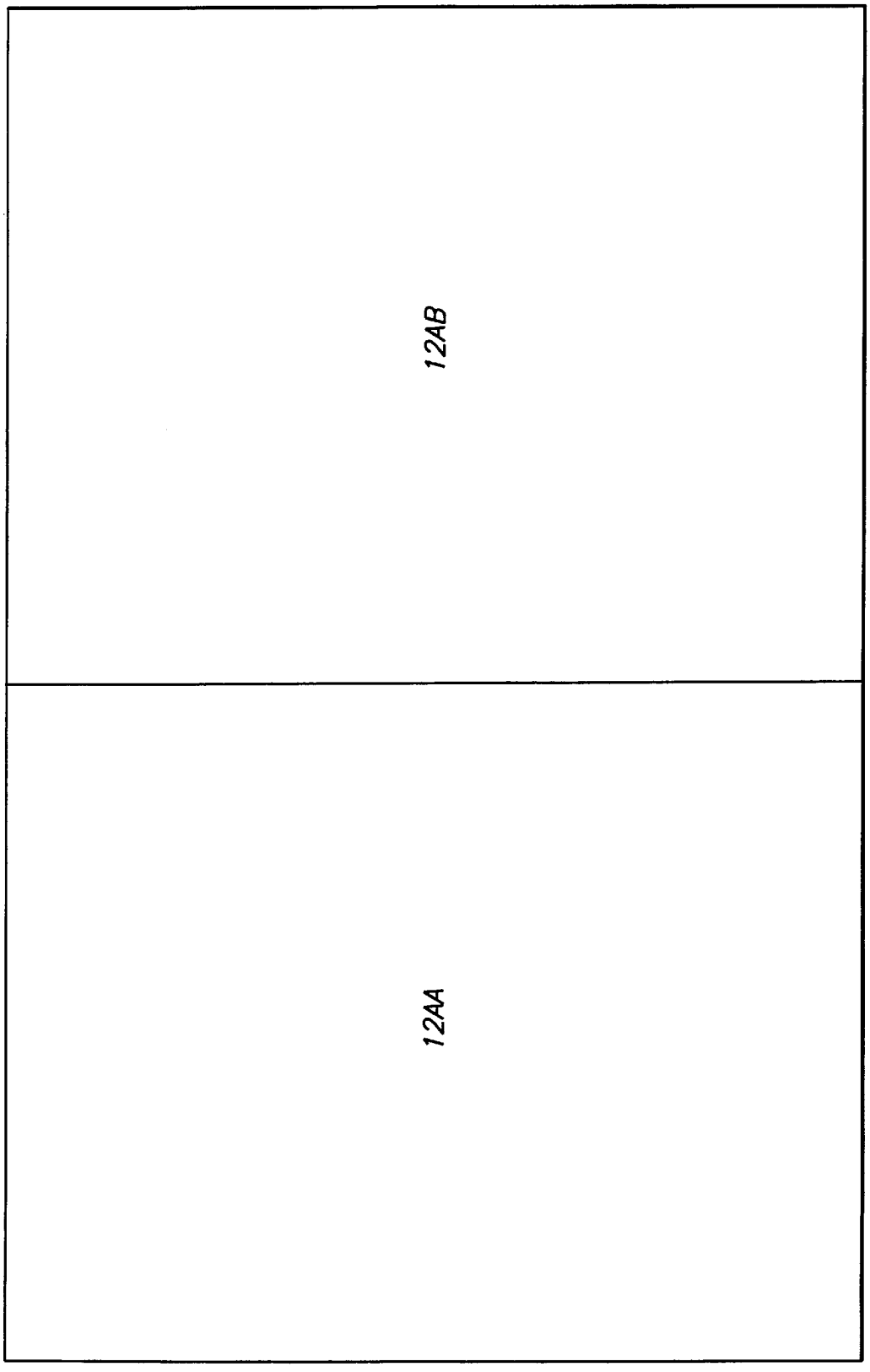


FIG 12

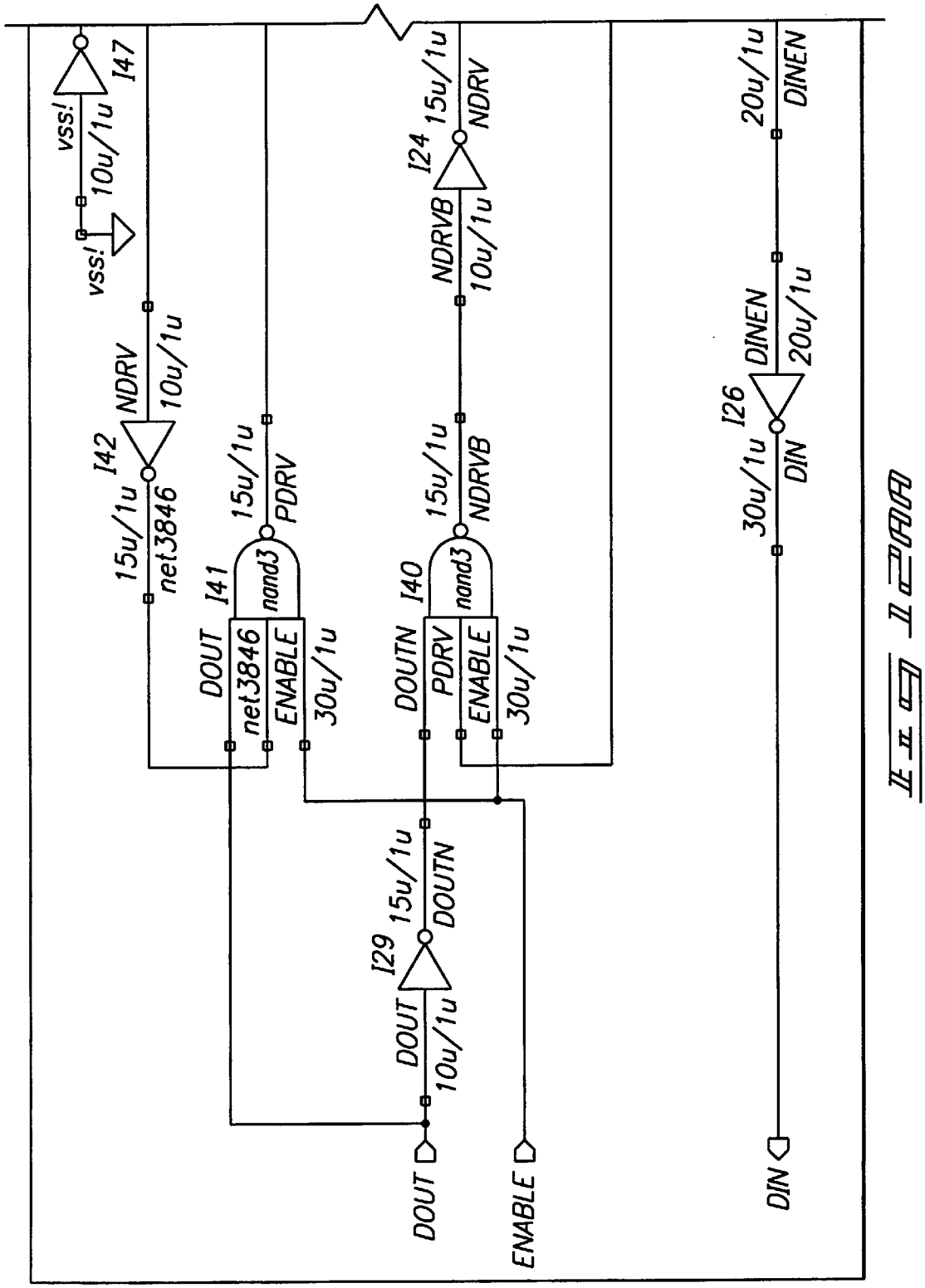

I47
vss!
10u/1u
vss!
NDRV
10u/1u
I42
15u/1u
net3846
15u/1u
PDRV
I41
nand3
DOUT
net3846
ENABLE
30u/1u
I24
15u/1u
NDRV
NDRVB
10u/1u
15u/1u
NDRVB
I40
nand3
DOUTN
PDRV
ENABLE
30u/1u
20u/1u
DINEN
DINEN
20u/1u
I26
30u/1u
DIN
I29
15u/1u
DOUTN
DOUT
10u/1u
DOUT
ENABLE
DIN

FIG 11AAA

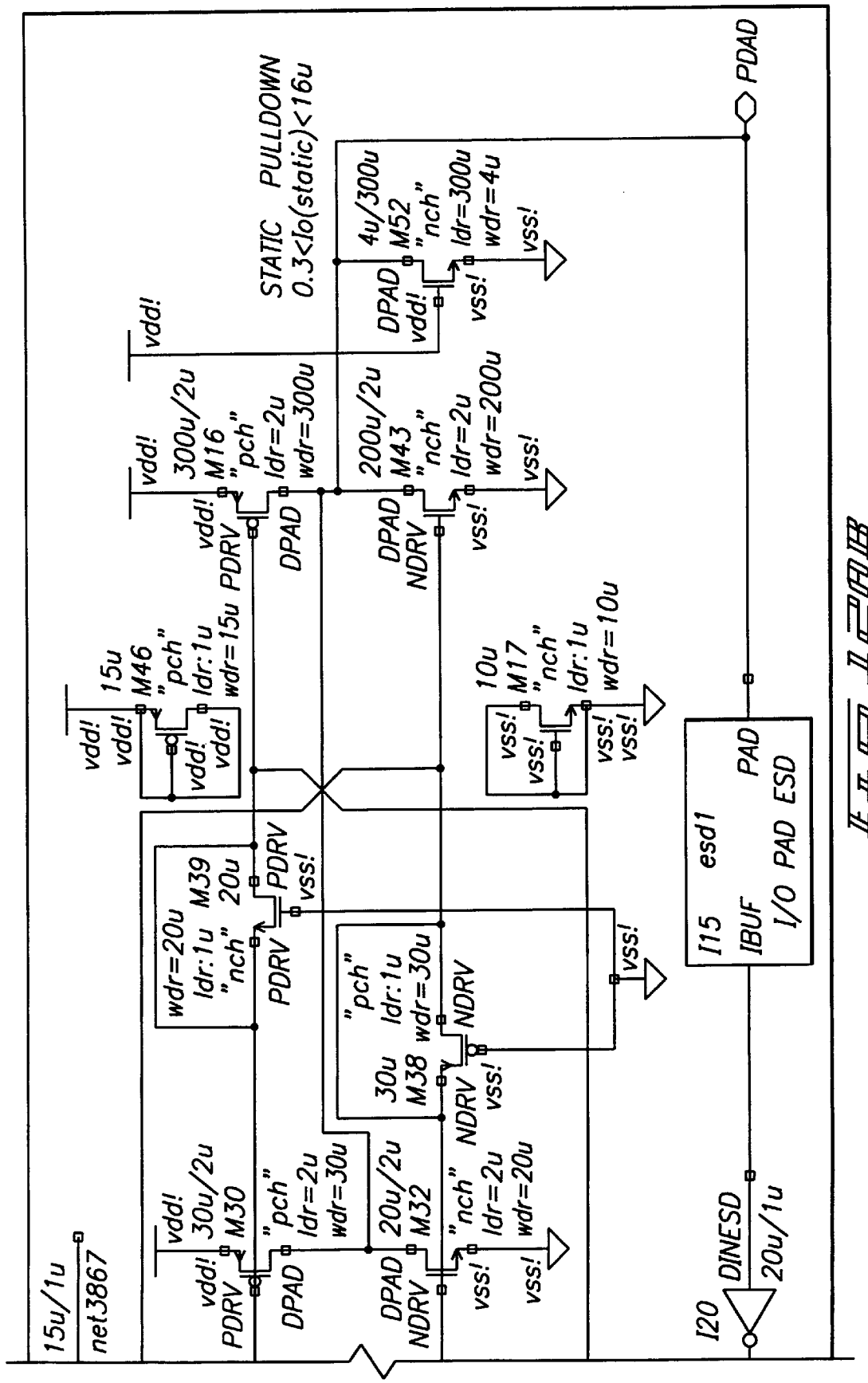
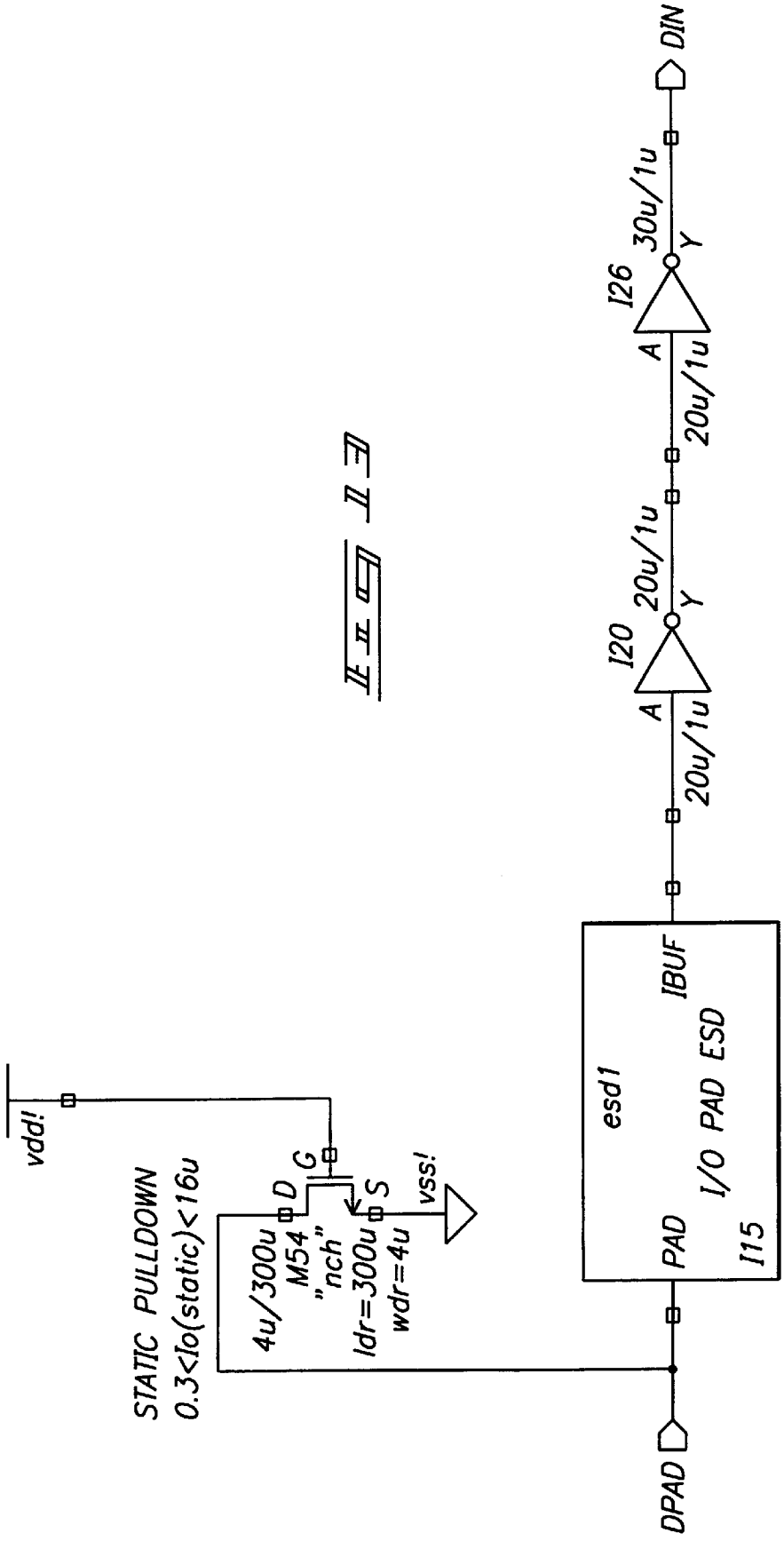

PDAD
STATIC PULLDOWN
0.3<Io(static)<16u
4u/300u
M52
"nch"
ldr=300u
wdr=4u
DPAD
vdd!
vss!
300u/2u
M16
"pch"
ldr=2u
wdr=300u
200u/2u
M43
"nch"
ldr=2u
wdr=200u
PDRV
NDRV
15u
M46
"pch"
ldr:1u
wdr=15u
10u
M17
"nch"
ldr:1u
wdr=10u
wdr=20u
ldr:1u
"nch"
M39
20u
"pch"
ldr:1u
wdr=30u
30u
M38
NDRV
30u/2u
M30
"pch"
ldr=2u
wdr=30u
20u/2u
M32
"nch"
ldr=2u
wdr=20u
I15
esd1
IBUF
I/O PAD ESD
PAD
I20
DINESD
20u/1u
15u/1u
net3867

FIG 11


DIN
I26
30u/1u
Y
A
20u/1u
20u/1u
Y
I20
A
20u/1u
IBUF
esd1
I/O PAD ESD
I15
PAD
DPAD
vdd!
STATIC PULLDOWN
0.3<Io(static)<16u
4u/300u
M54
"nch"
ldr=300u
wdr=4u
D
G
S
vss!

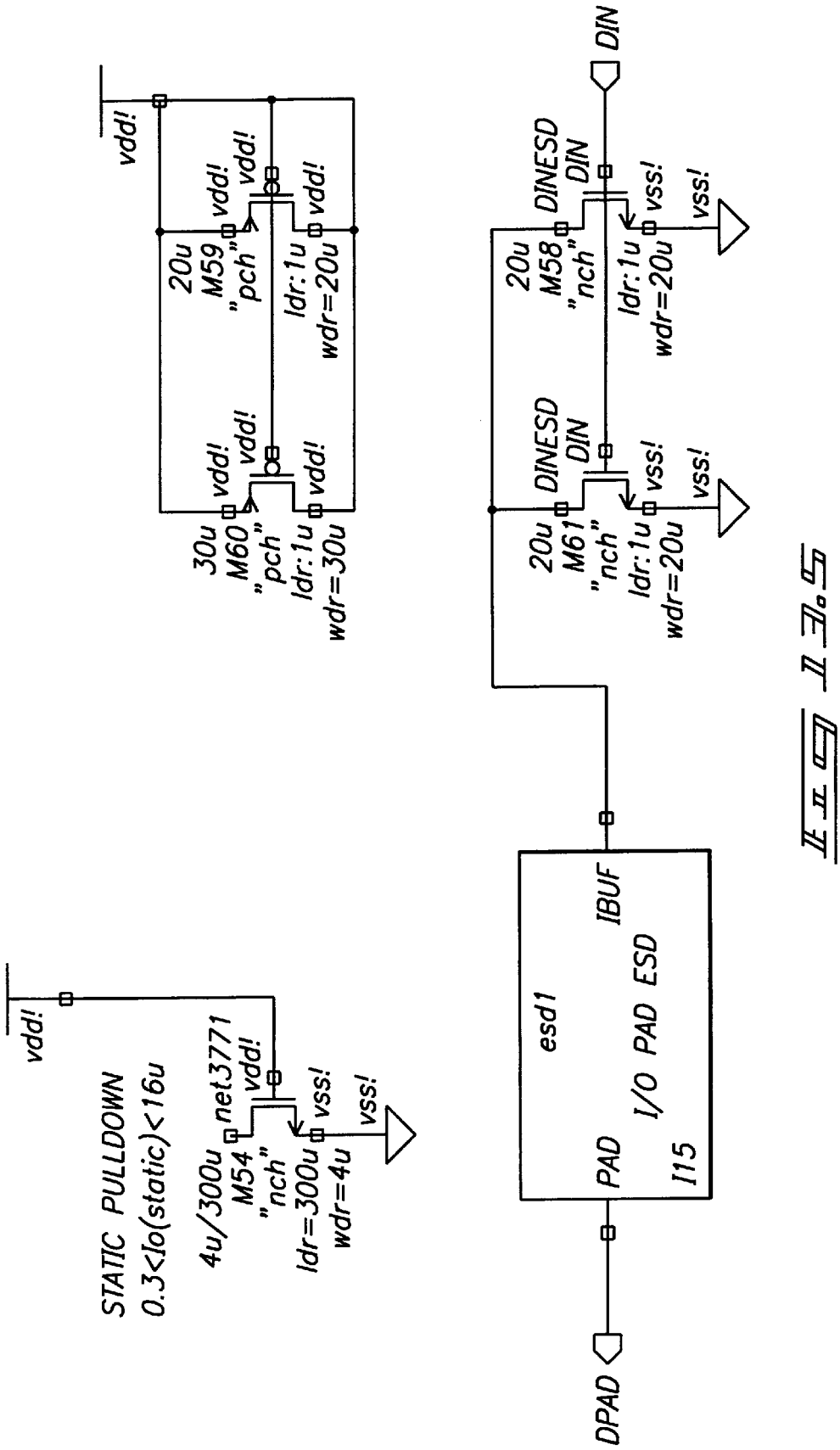

vdd!
20u
M59
"pch"
ldr:1u
wdr=20u
vdd!
vdd!
vdd!
30u
M60
"pch"
ldr:1u
wdr=30u
vdd!
vdd!
vdd!
DIN
DINESD
DIN
20u
M58
"nch"
ldr:1u
wdr=20u
vss!
vss!
DINESD
DIN
20u
M61
"nch"
ldr:1u
wdr=20u
vss!
vss!
vdd!
STATIC PULLDOWN
0.3<Io(static)<16u
4u/300u
net3771
M54
"nch"
ldr=300u
wdr=4u
vdd!
vss!
vss!
esd1
IBUF
I/O PAD ESD
I15
PAD
DPAD

FIG. 115

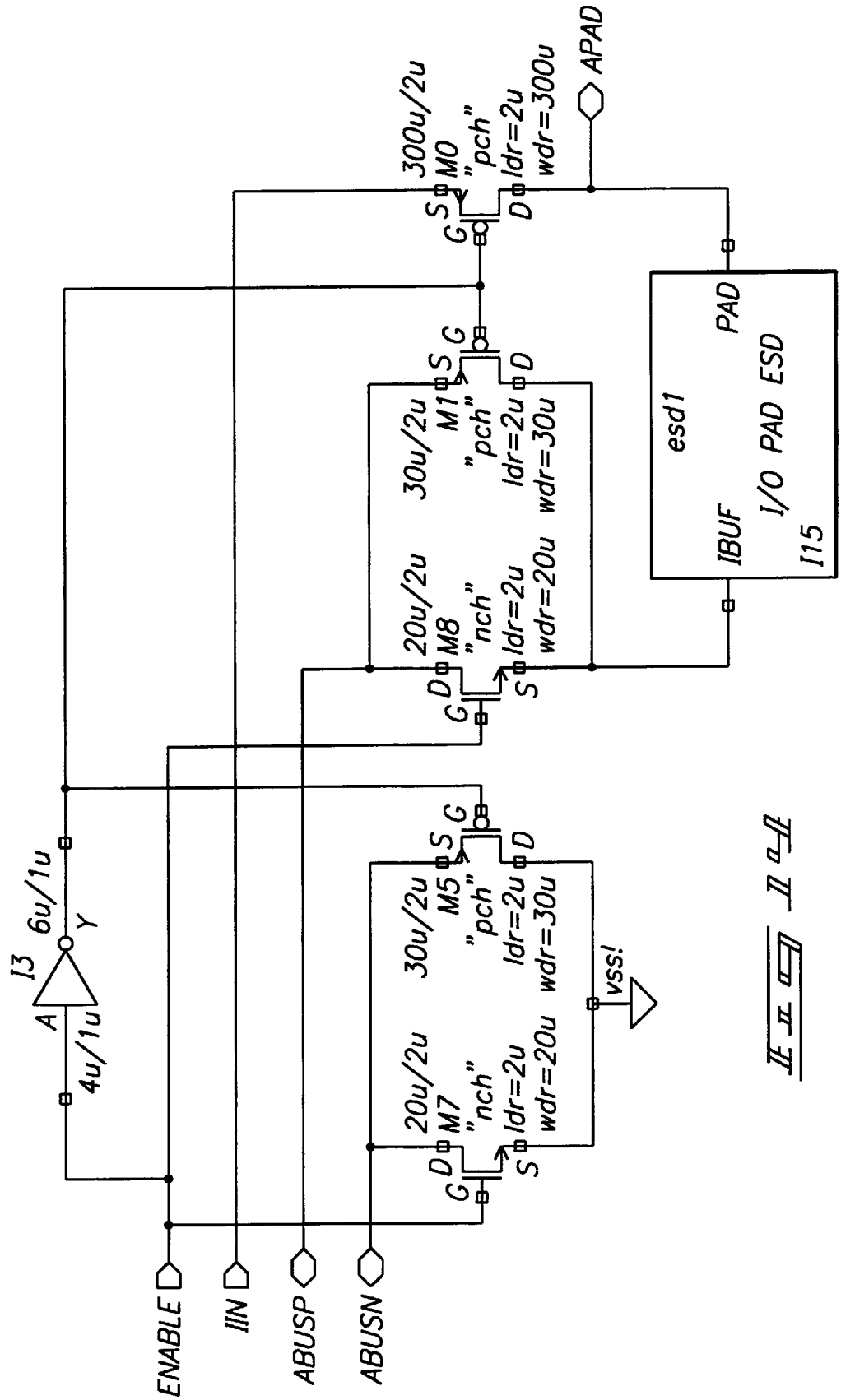

APAD
300u/2u
M0
"pch"
ldr=2u
wdr=300u
PAD
esd1
I/O PAD ESD
IBUF
I15
30u/2u
M1
"pch"
ldr=2u
wdr=30u
20u/2u
M8
"nch"
ldr=2u
wdr=20u
I3
6u/1u
Y
A
4u/1u
30u/2u
M5
"pch"
ldr=2u
wdr=30u
vss!
20u/2u
M7
"nch"
ldr=2u
wdr=20u
ENABLE
IIN
ABUSP
ABUSN

FIG 11

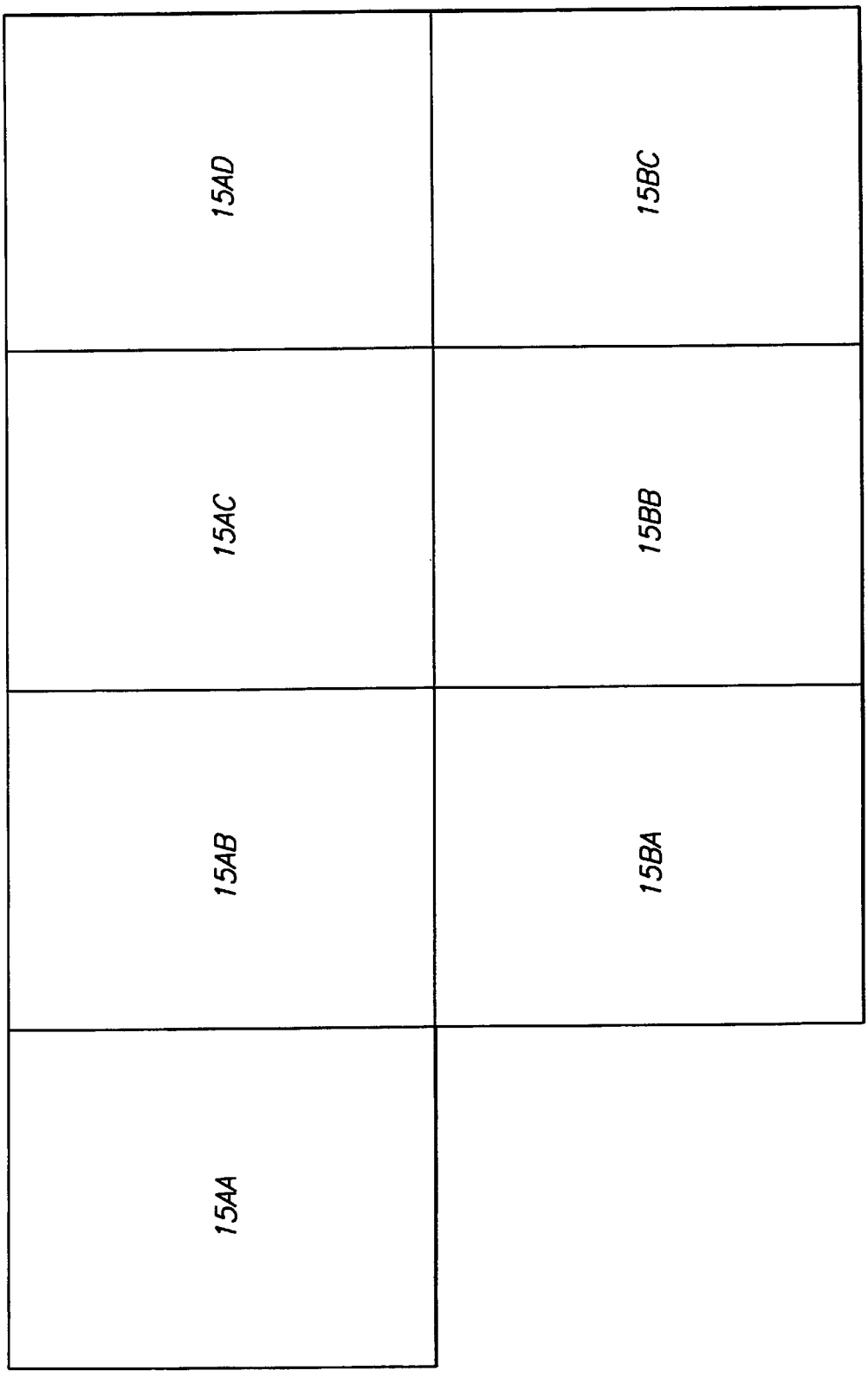


FIG 15

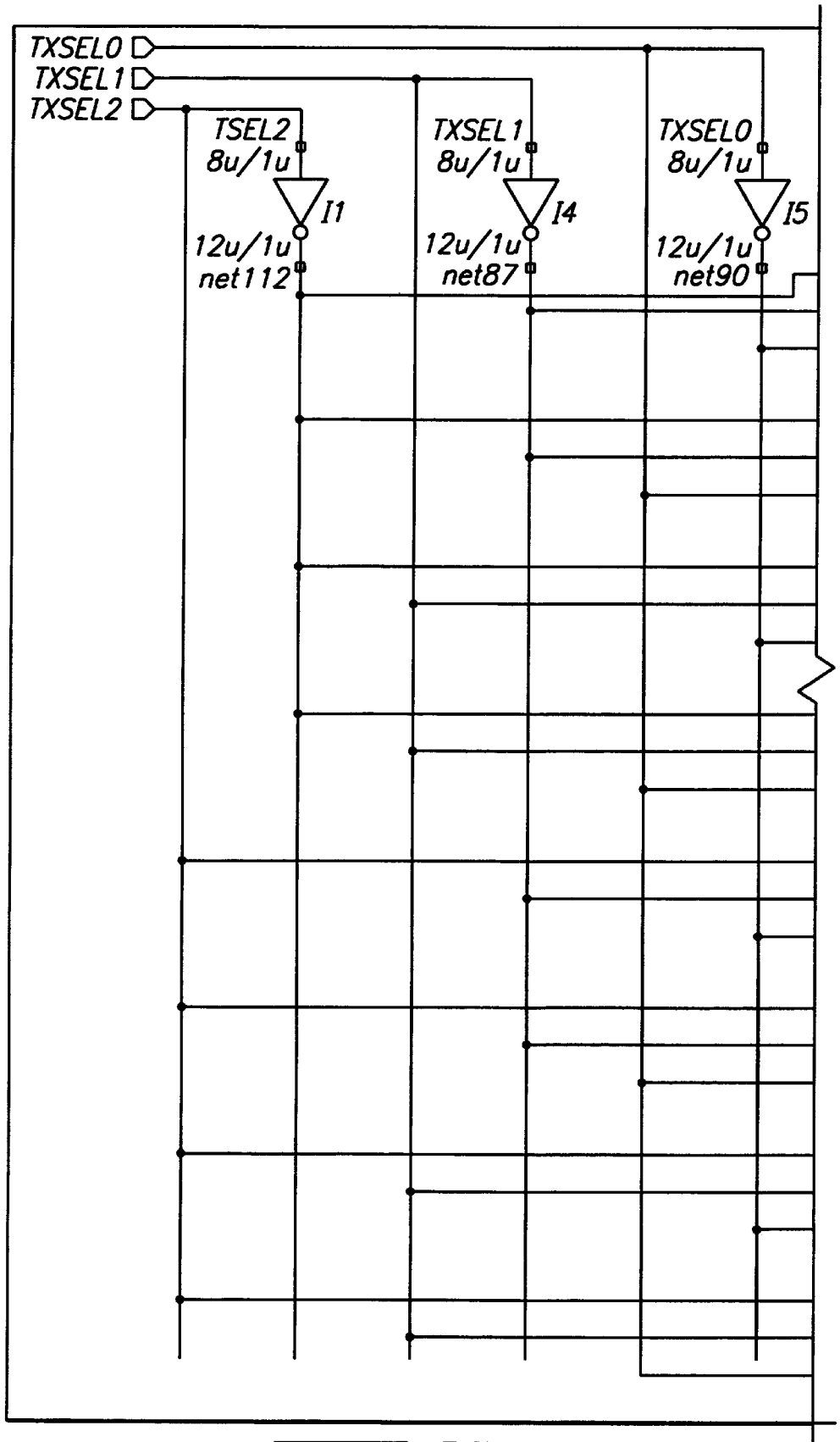
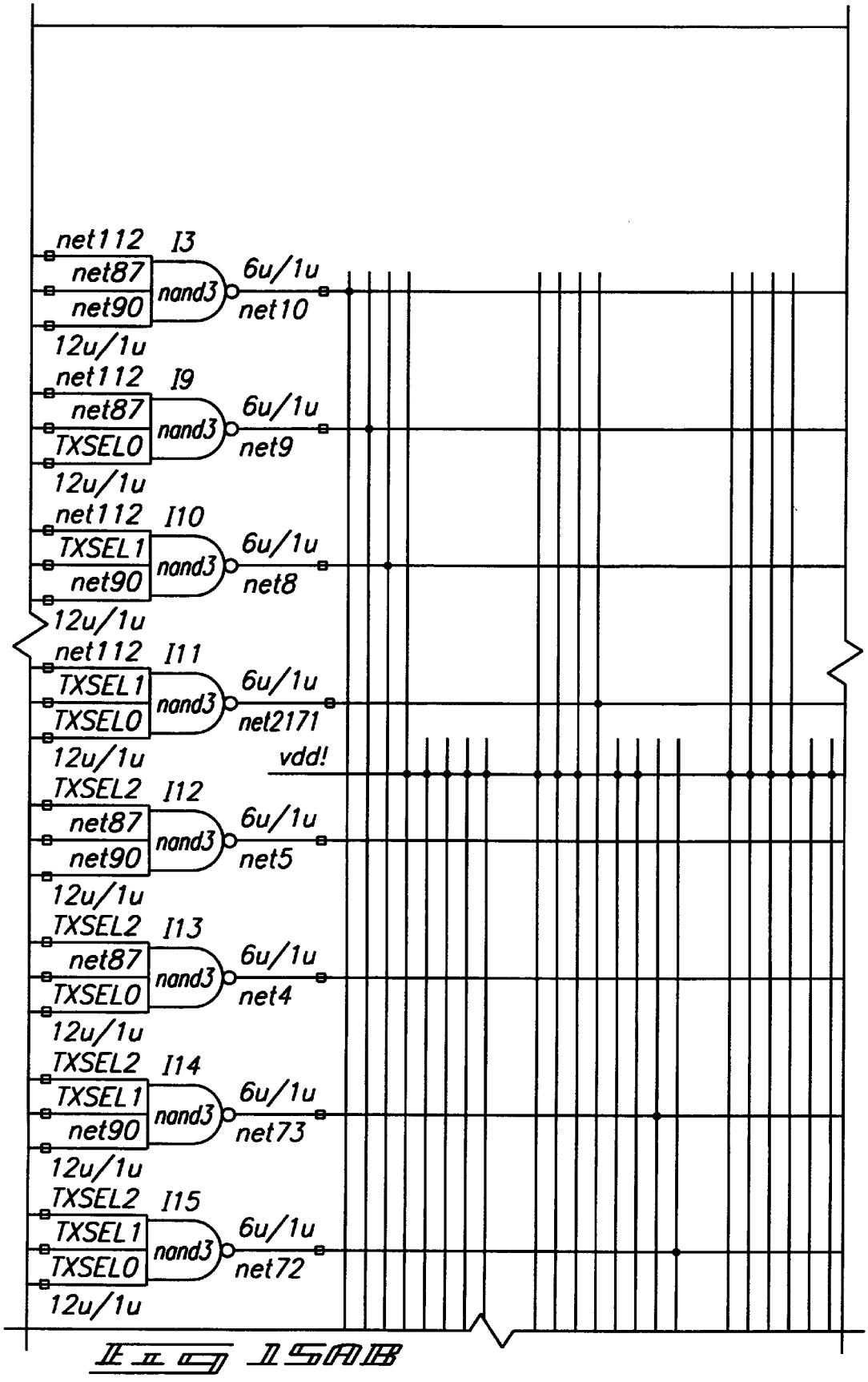

TXSEL0
TXSEL1
TXSEL2
TSEL2
8u/1u
I1
12u/1u
net112
TXSEL1
8u/1u
I4
12u/1u
net87
TXSEL0
8u/1u
I5
12u/1u
net90

Fig 15AA


net112
net87
net90
12u/1u
I3
nand3
6u/1u
net10
net112
net87
TXSEL0
12u/1u
I9
nand3
6u/1u
net9
net112
TXSEL1
net90
12u/1u
I10
nand3
6u/1u
net8
net112
TXSEL1
TXSEL0
12u/1u
I11
nand3
6u/1u
net2171
vdd!
TXSEL2
net87
net90
12u/1u
I12
nand3
6u/1u
net5
TXSEL2
net87
TXSEL0
12u/1u
I13
nand3
6u/1u
net4
TXSEL2
TXSEL1
net90
12u/1u
I14
nand3
6u/1u
net73
TXSEL2
TXSEL1
TXSEL0
12u/1u
I15
nand3
6u/1u
net72

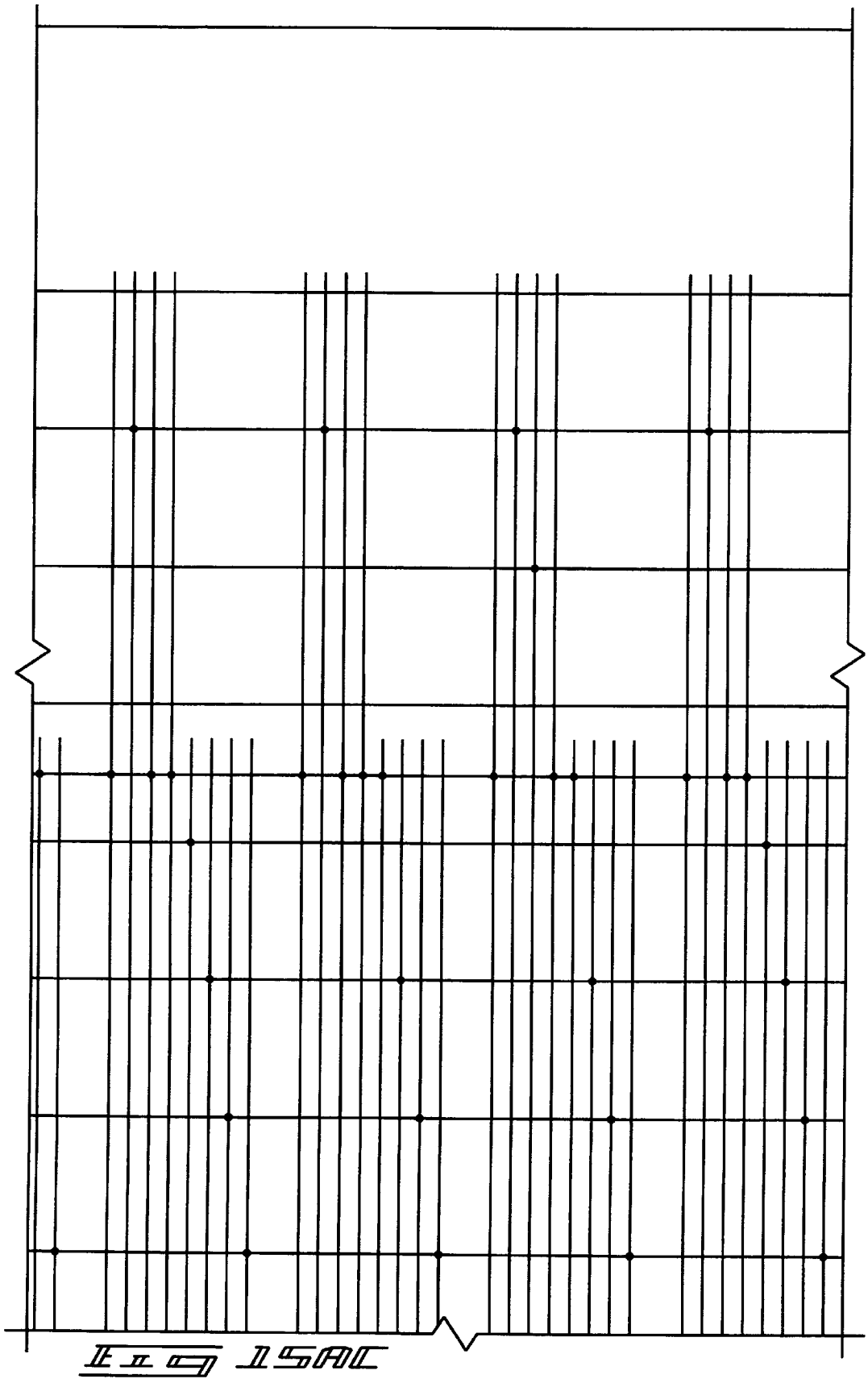
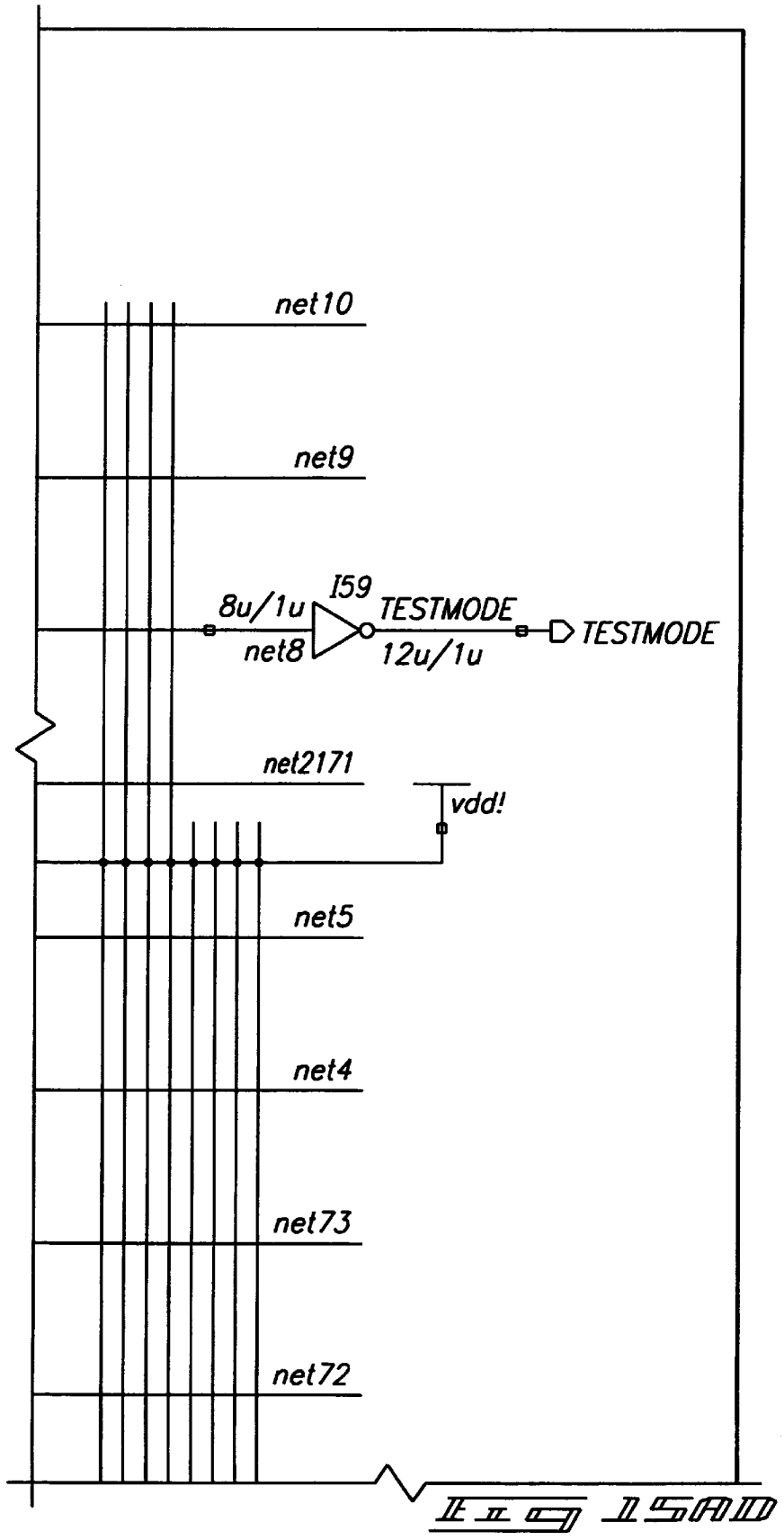


FIG 15AC


net10
net9
8u/1u
I59
TESTMODE
TESTMODE
net8
12u/1u
net2171
vdd!
net5
net4
net73
net72

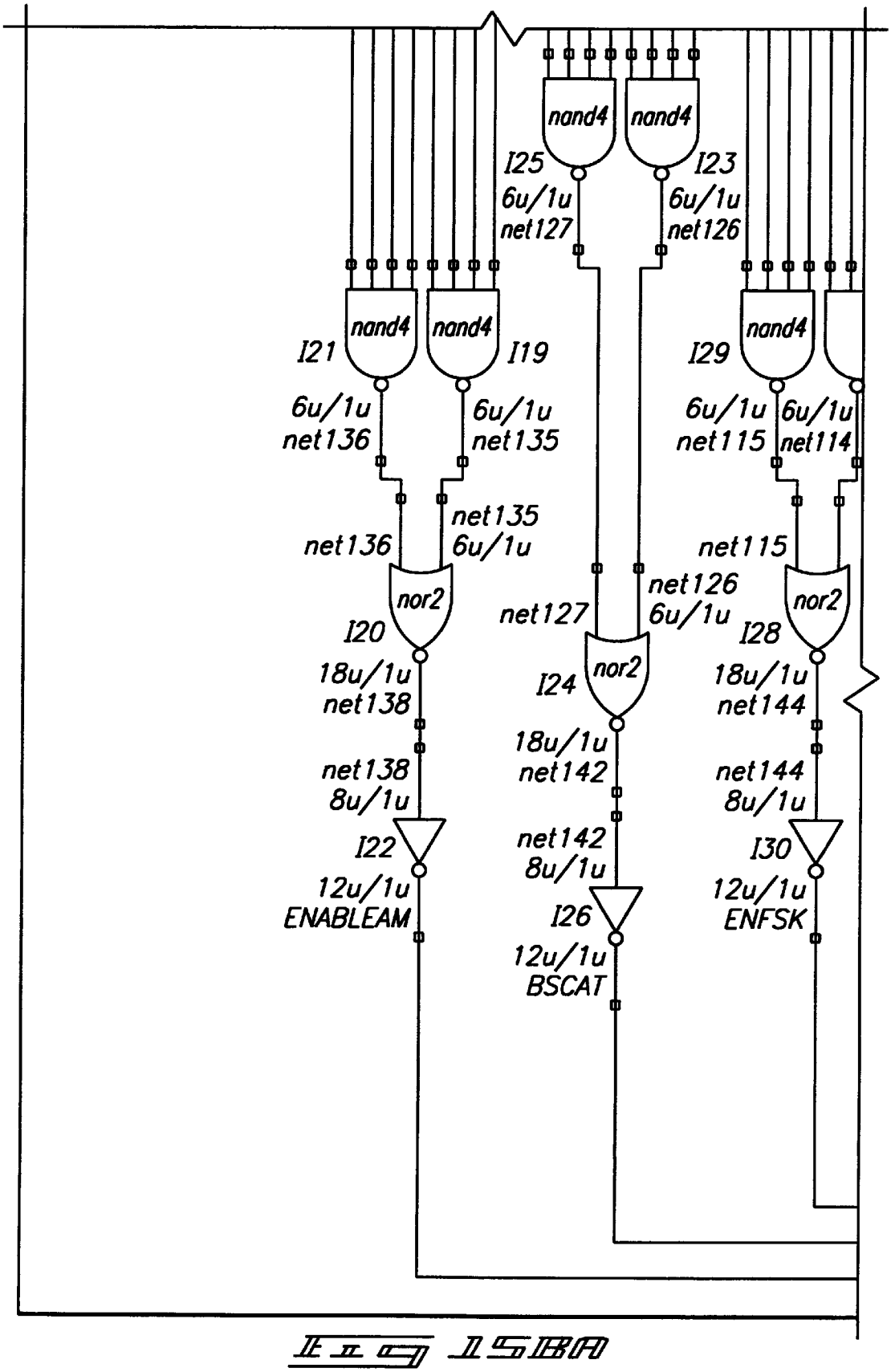

nand4
nand4
I25
6u/1u
net127
I23
6u/1u
net126
nand4
nand4
I21
I19
6u/1u
net136
6u/1u
net135
nand4
I29
6u/1u
net115
6u/1u
net114
net135
net136
6u/1u
net115
net126
net127
6u/1u
nor2
nor2
nor2
I20
I24
I28
18u/1u
net138
18u/1u
net142
18u/1u
net144
net138
8u/1u
net142
8u/1u
net144
8u/1u
I22
I26
I30
12u/1u
ENABLEAM
12u/1u
BSCAT
12u/1u
ENFSK

Fig 1SBA

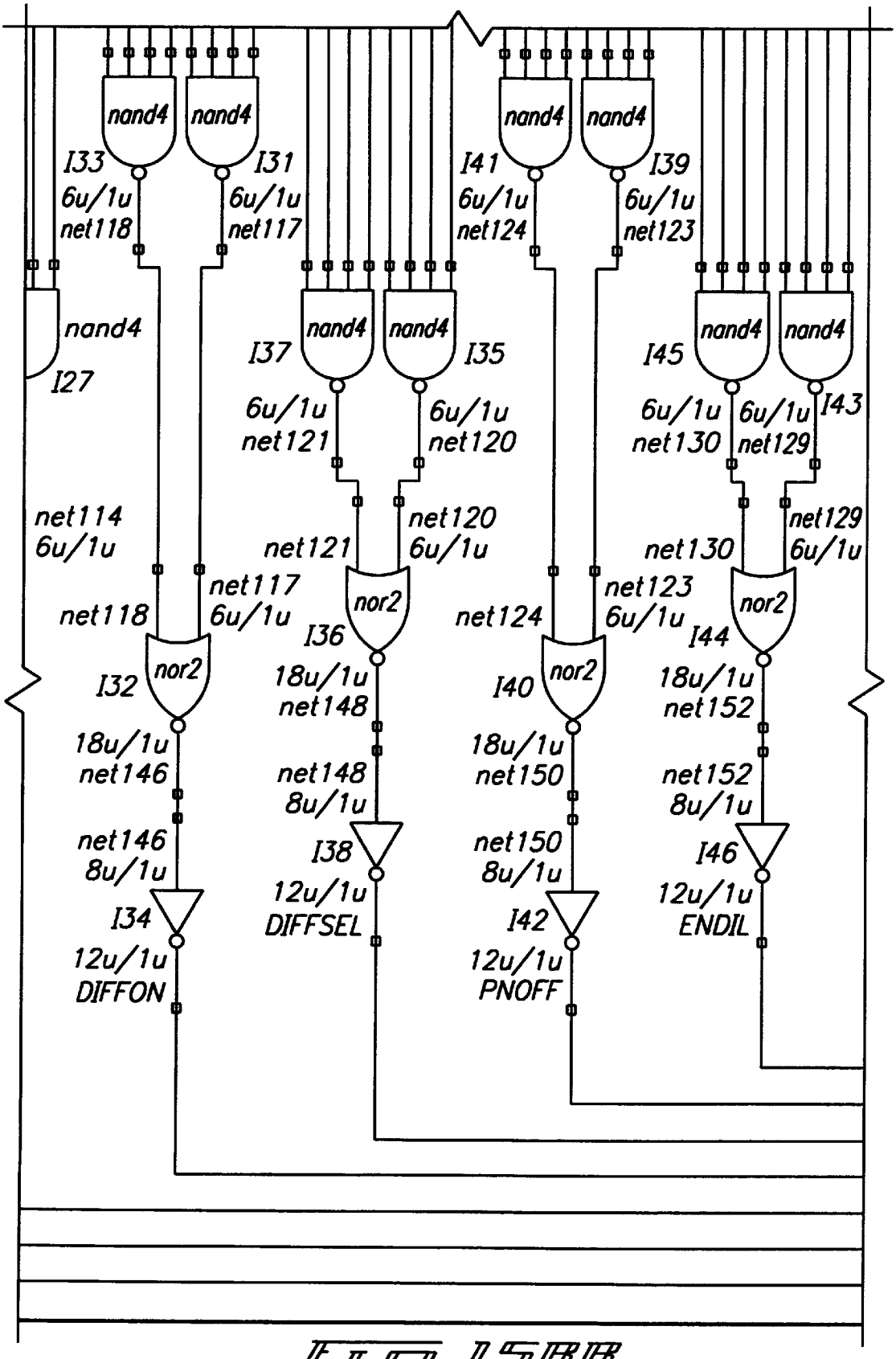

nand4
I33
6u/1u
net118
nand4
I31
6u/1u
net117
nand4
I41
6u/1u
net124
nand4
I39
6u/1u
net123
nand4
I27
nand4
I37
6u/1u
net121
nand4
I35
6u/1u
net120
nand4
I45
6u/1u
net130
nand4
I43
6u/1u
net129
net114
6u/1u
net118
net117
6u/1u
net121
net120
6u/1u
net130
net129
6u/1u
net123
6u/1u
net124
nor2
I32
nor2
I36
nor2
I40
nor2
I44
18u/1u
net146
18u/1u
net148
18u/1u
net150
18u/1u
net152
net146
8u/1u
net148
8u/1u
net150
8u/1u
net152
8u/1u
I34
12u/1u
DIFFON
I38
12u/1u
DIFFSEL
I42
12u/1u
PNOFF
I46
12u/1u
ENDIL

Fig 158B

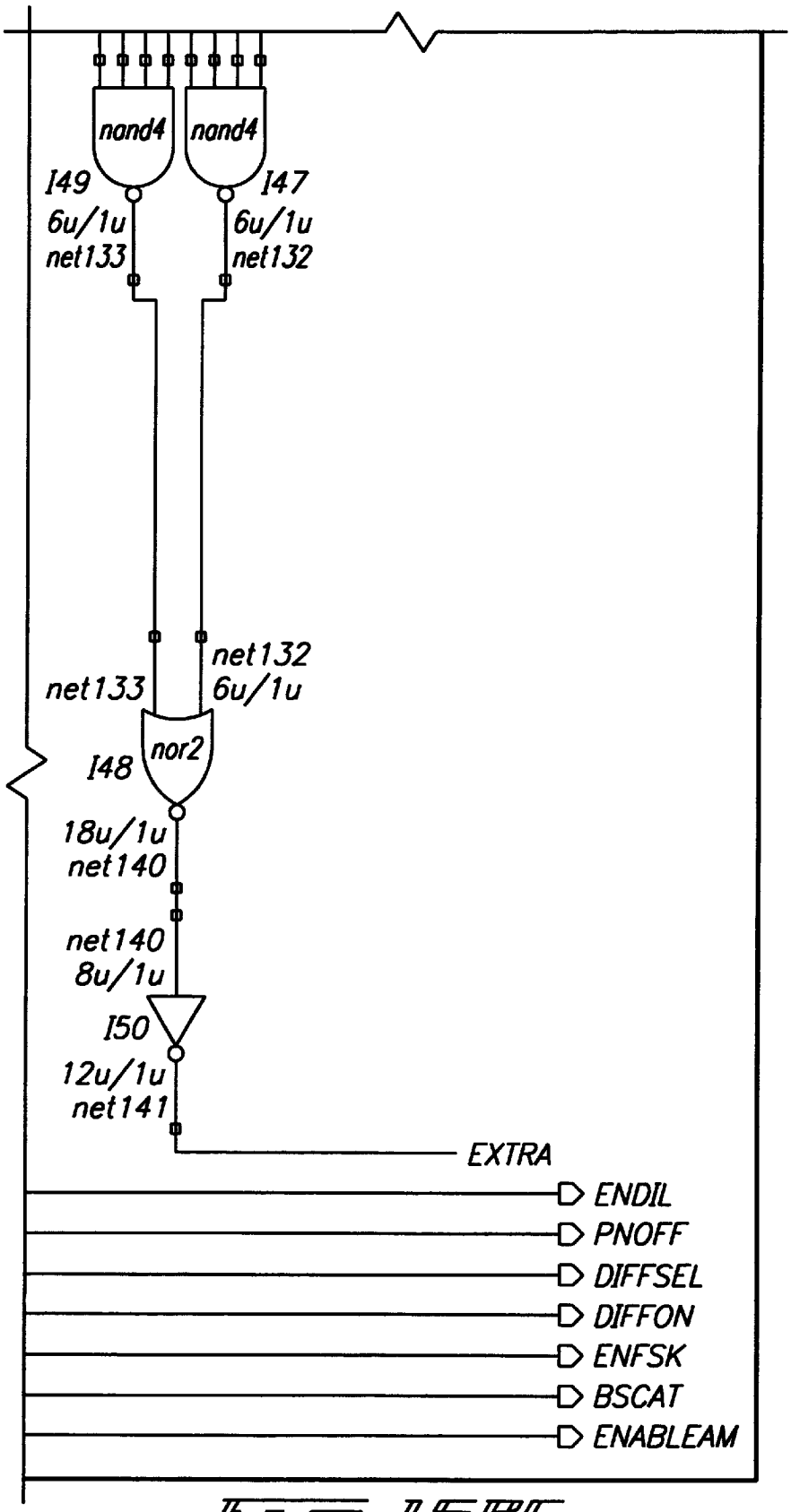

nand4
nand4
I49
6u/1u
net133
I47
6u/1u
net132
net133
net132
6u/1u
nor2
I48
18u/1u
net140
net140
8u/1u
I50
12u/1u
net141
EXTRA
ENDIL
PNOFF
DIFFSEL
DIFFON
ENFSK
BSCAT
ENABLEAM

Fig 1586

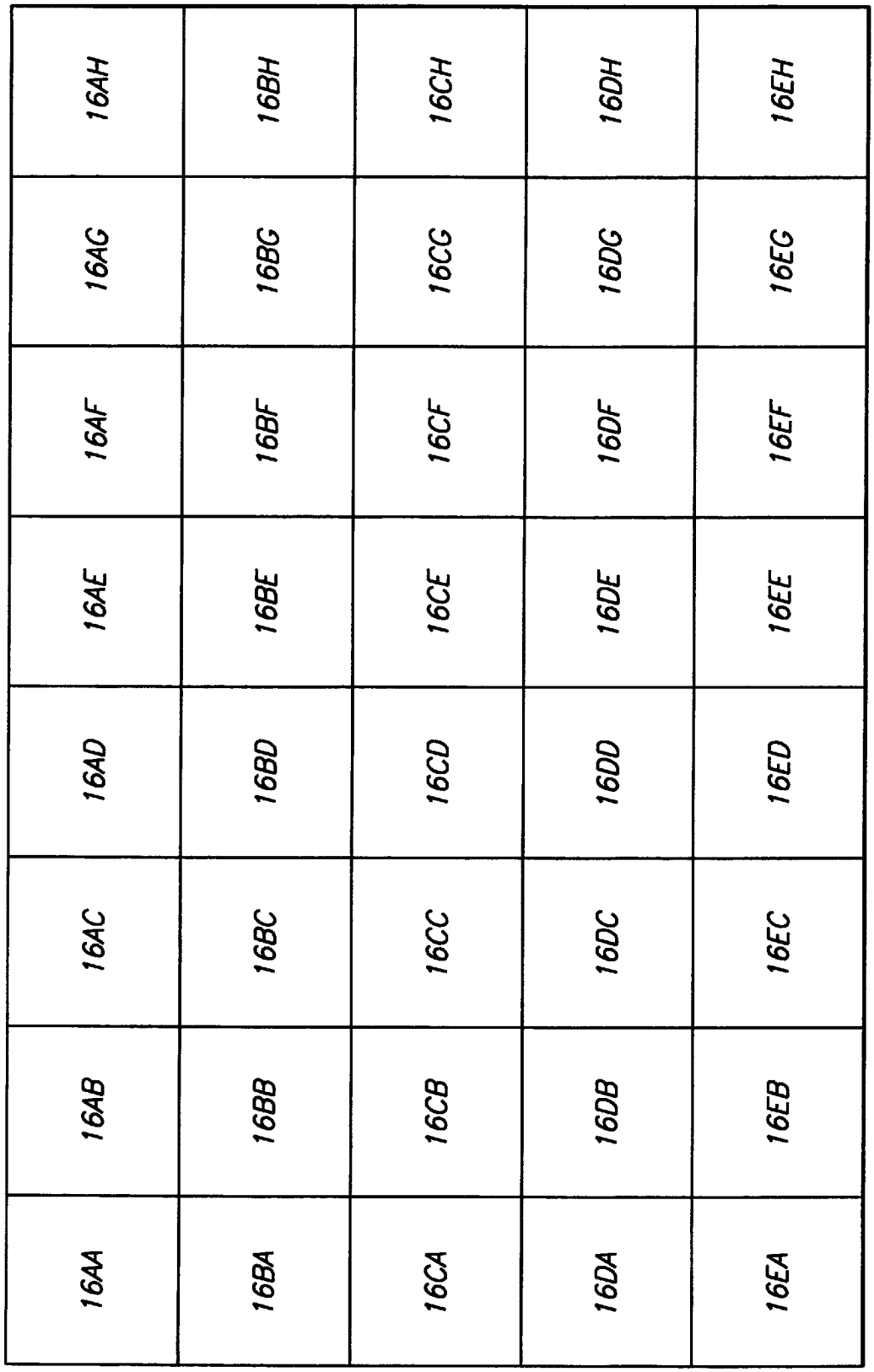

16AA 16AB 16AC 16AD 16AE 16AF 16AG 16AH
16BA 16BB 16BC 16BD 16BE 16BF 16BG 16BH
16CA 16CB 16CC 16CD 16CE 16CF 16CG 16CH
16DA 16DB 16DC 16DD 16DE 16DF 16DG 16DH
16EA 16EB 16EC 16ED 16EE 16EF 16EG 16EH

FIG 16

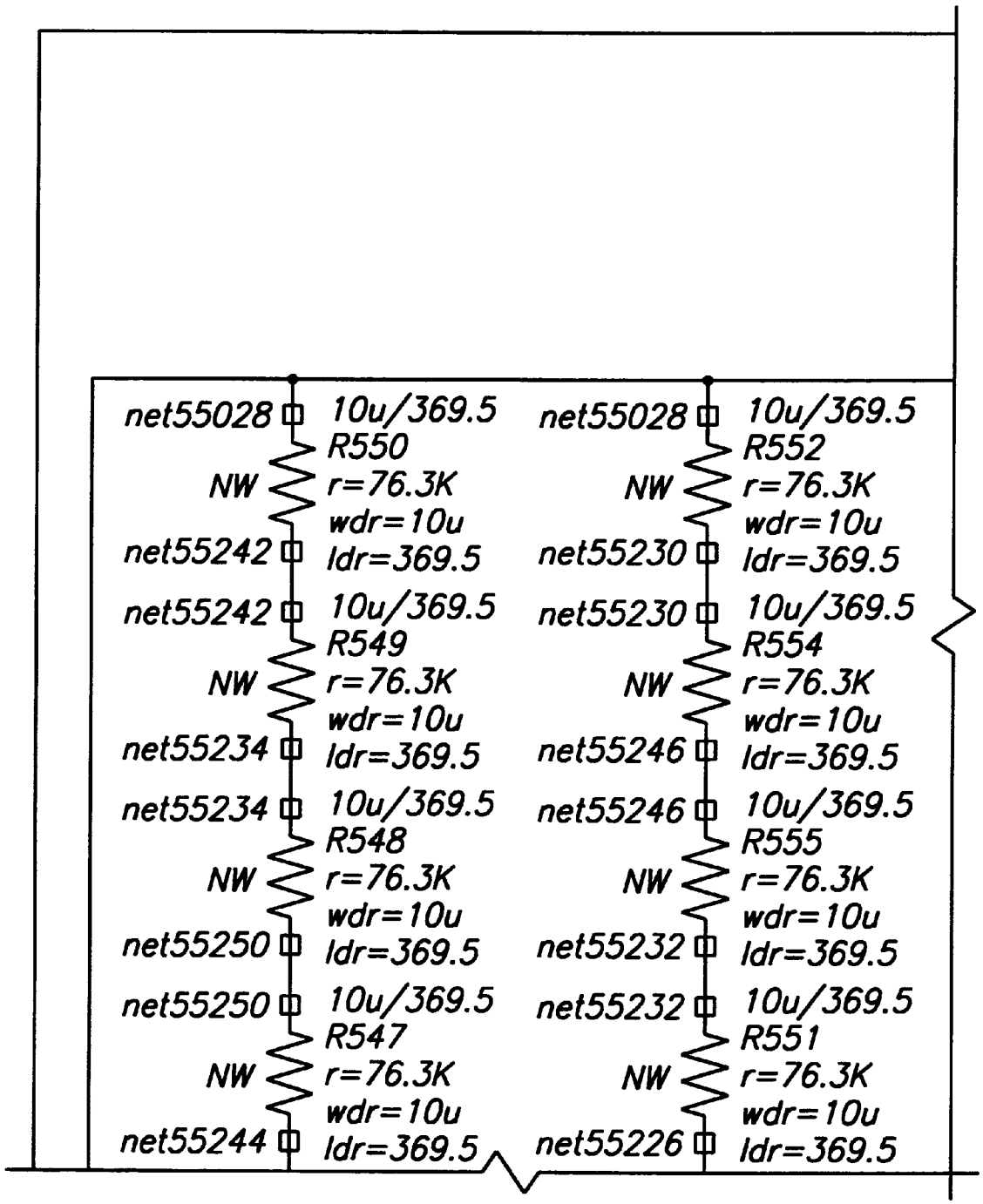

net55028
10u/369.5
R550
NW
r=76.3K
wdr=10u
net55242
ldr=369.5
net55242
10u/369.5
R549
NW
r=76.3K
wdr=10u
net55234
ldr=369.5
net55234
10u/369.5
R548
NW
r=76.3K
wdr=10u
net55250
ldr=369.5
net55250
10u/369.5
R547
NW
r=76.3K
wdr=10u
net55244
ldr=369.5
net55028
10u/369.5
R552
NW
r=76.3K
wdr=10u
net55230
ldr=369.5
net55230
10u/369.5
R554
NW
r=76.3K
wdr=10u
net55246
ldr=369.5
net55246
10u/369.5
R555
NW
r=76.3K
wdr=10u
net55232
ldr=369.5
net55232
10u/369.5
R551
NW
r=76.3K
wdr=10u
net55226
ldr=369.5

Fig 16AA

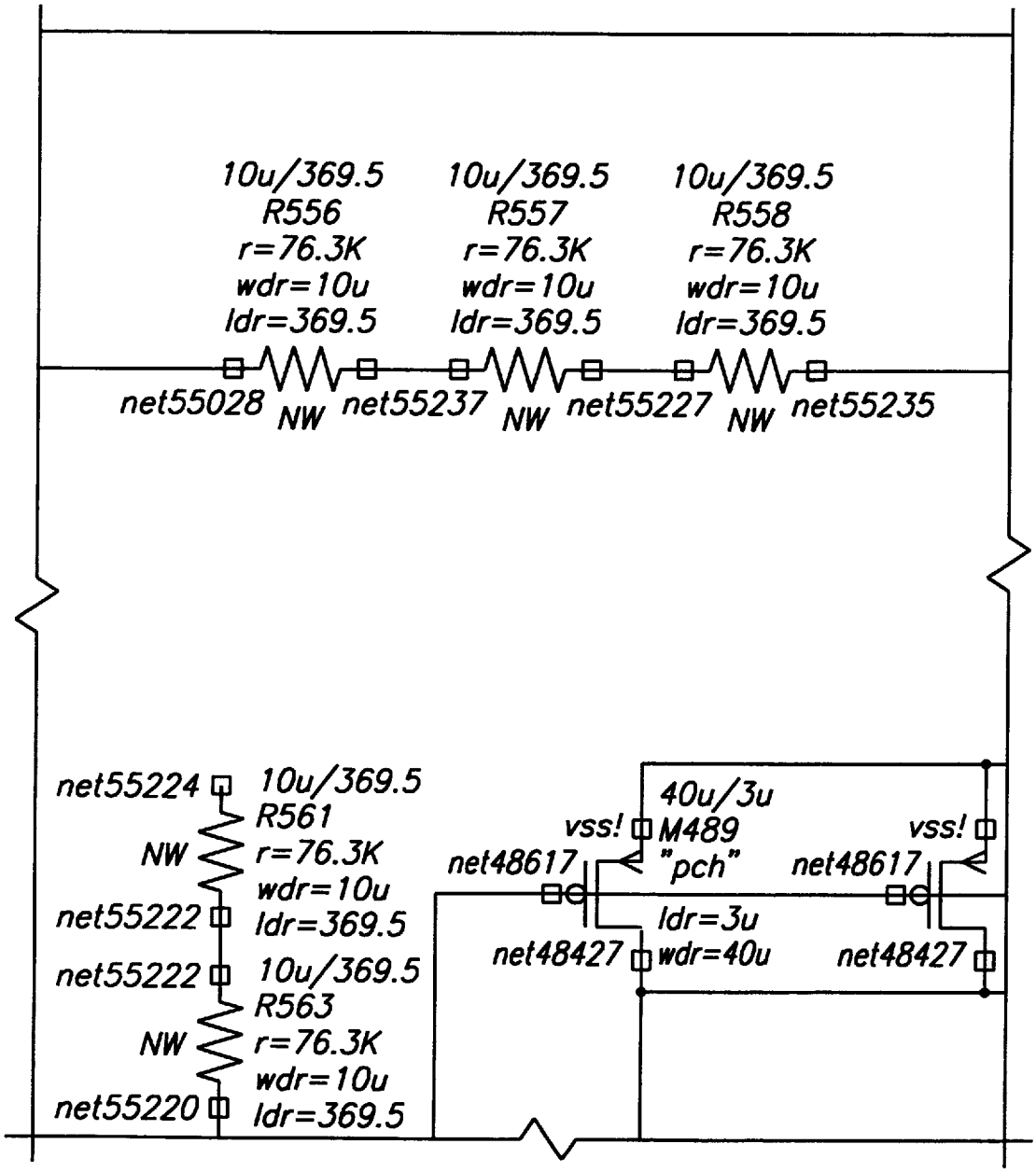

10u/369.5
R556
r=76.3K
wdr=10u
ldr=369.5
10u/369.5
R557
r=76.3K
wdr=10u
ldr=369.5
10u/369.5
R558
r=76.3K
wdr=10u
ldr=369.5
net55028
NW
net55237
NW
net55227
NW
net55235
net55224
10u/369.5
R561
NW
r=76.3K
wdr=10u
net55222
ldr=369.5
net55222
10u/369.5
R563
NW
r=76.3K
wdr=10u
net55220
ldr=369.5
40u/3u
vss!
M489
"pch"
net48617
ldr=3u
net48427
wdr=40u
vss!
net48617
net48427

Fig 16AB

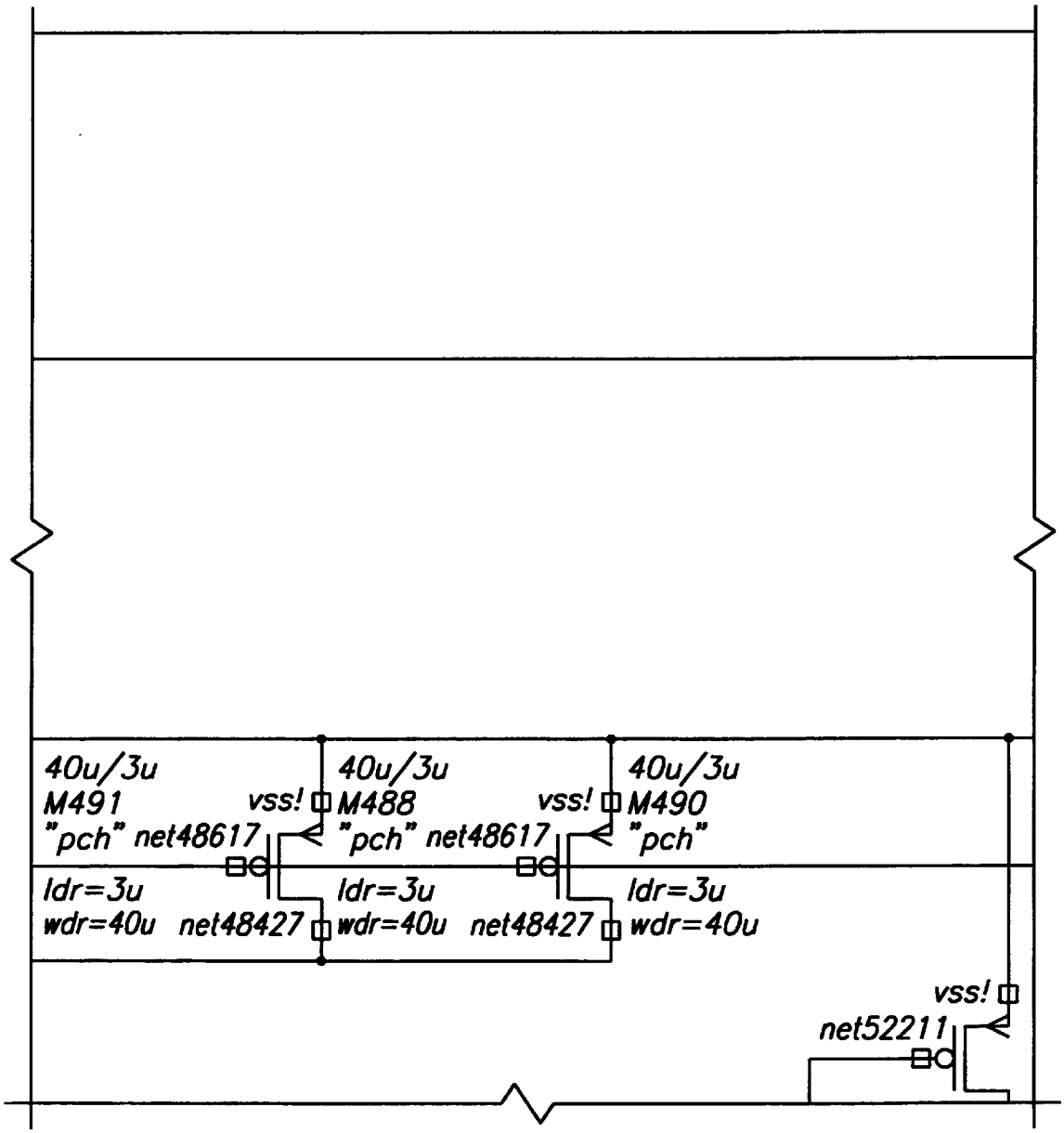

40u/3u
M491
"pch" net48617
ldr=3u
wdr=40u net48427
vss!
40u/3u
M488
"pch" net48617
ldr=3u
wdr=40u net48427
vss!
40u/3u
M490
"pch"
ldr=3u
wdr=40u
vss!
net52211

Fig 16AC

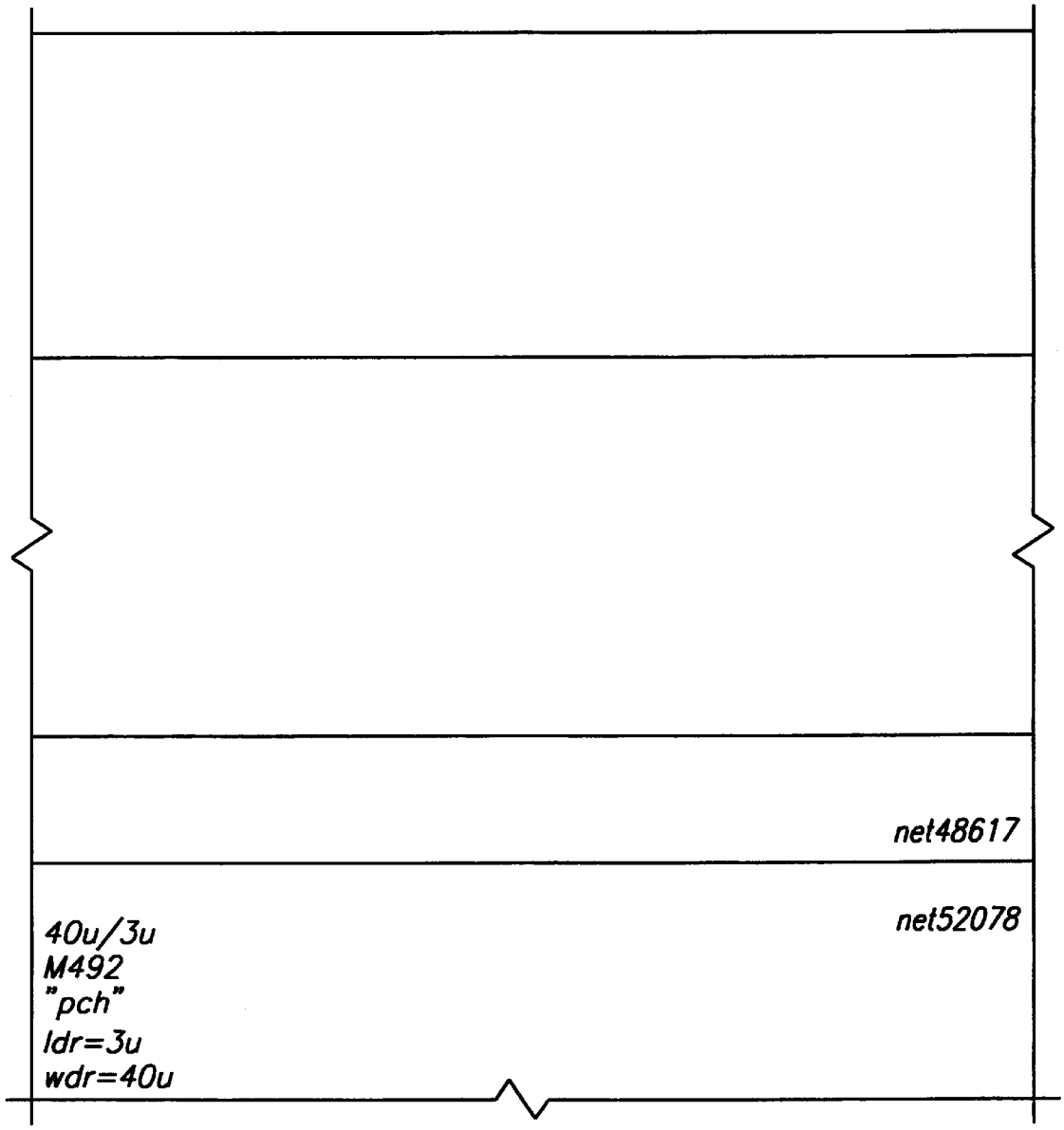


Fig 16AD

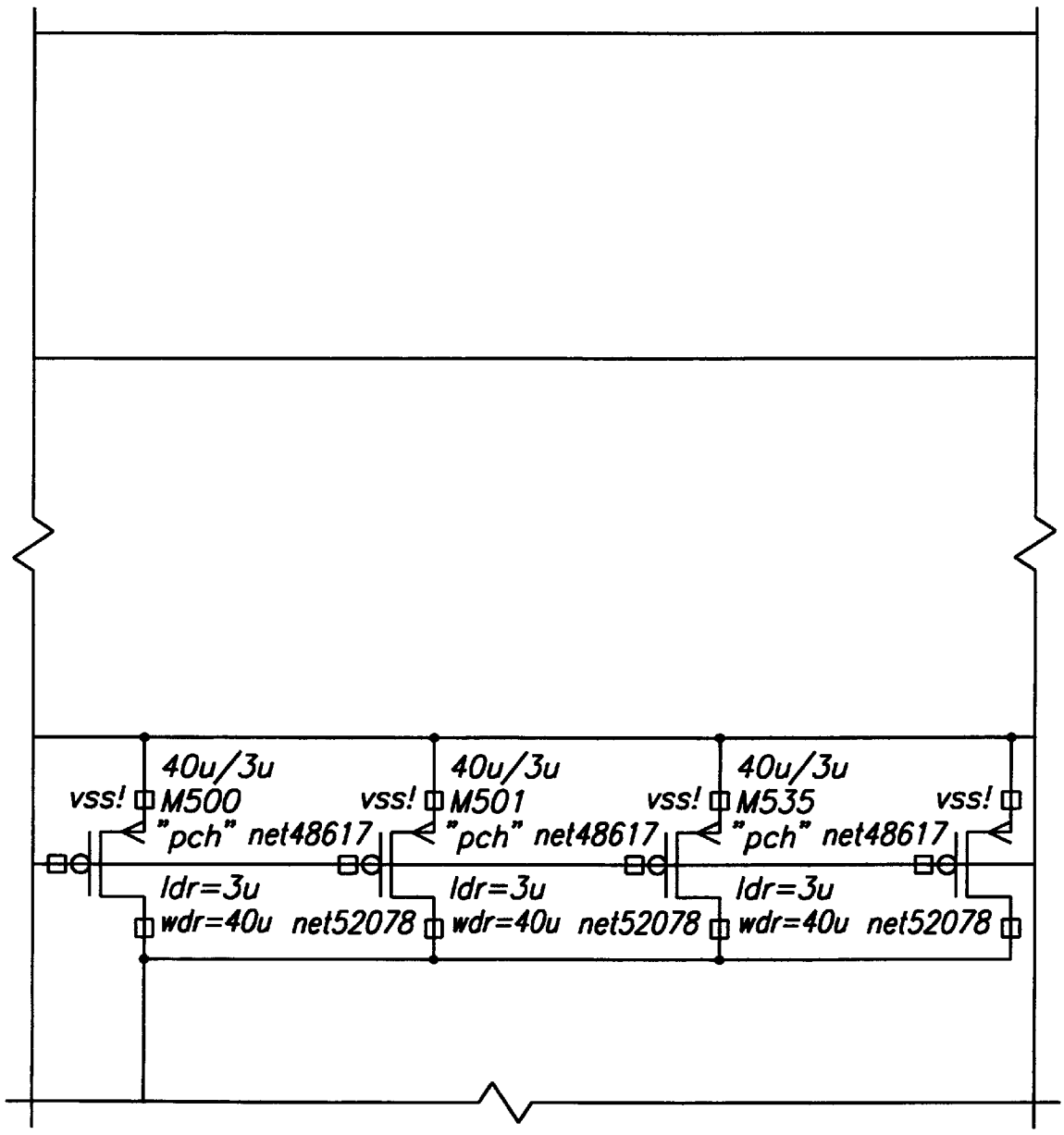

40u/3u
vss!
M500
"pch"
net48617
ldr=3u
wdr=40u
net52078
40u/3u
vss!
M501
"pch"
net48617
ldr=3u
wdr=40u
net52078
40u/3u
vss!
M535
"pch"
net48617
ldr=3u
wdr=40u
net52078
vss!

FIG 16AE

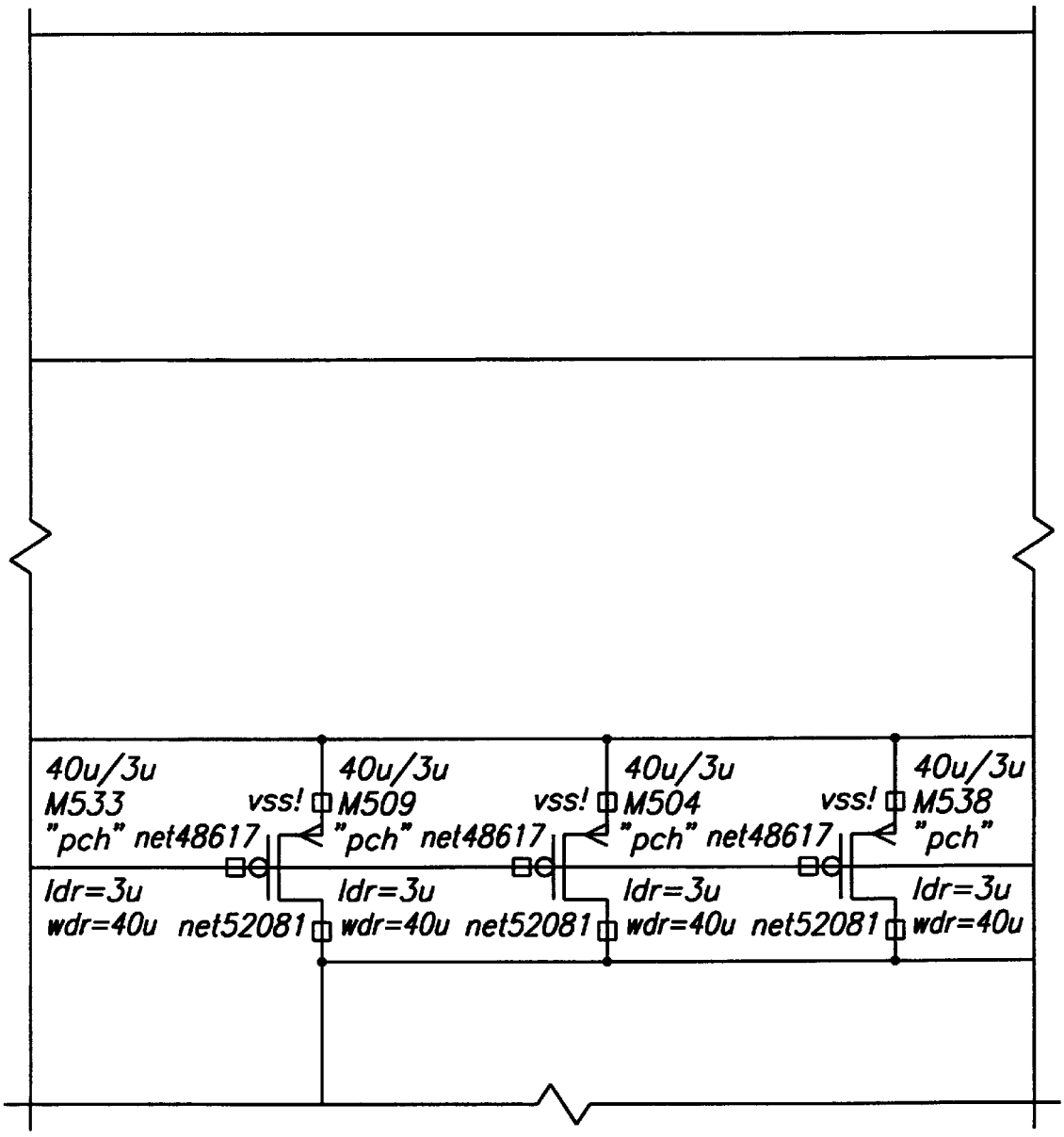

40u/3u
M533
"pch" net48617
vss!
ldr=3u
wdr=40u
net52081
40u/3u
M509
"pch" net48617
vss!
ldr=3u
wdr=40u
net52081
40u/3u
M504
"pch" net48617
vss!
ldr=3u
wdr=40u
net52081
40u/3u
M538
"pch"
ldr=3u
wdr=40u

Fig 16AF

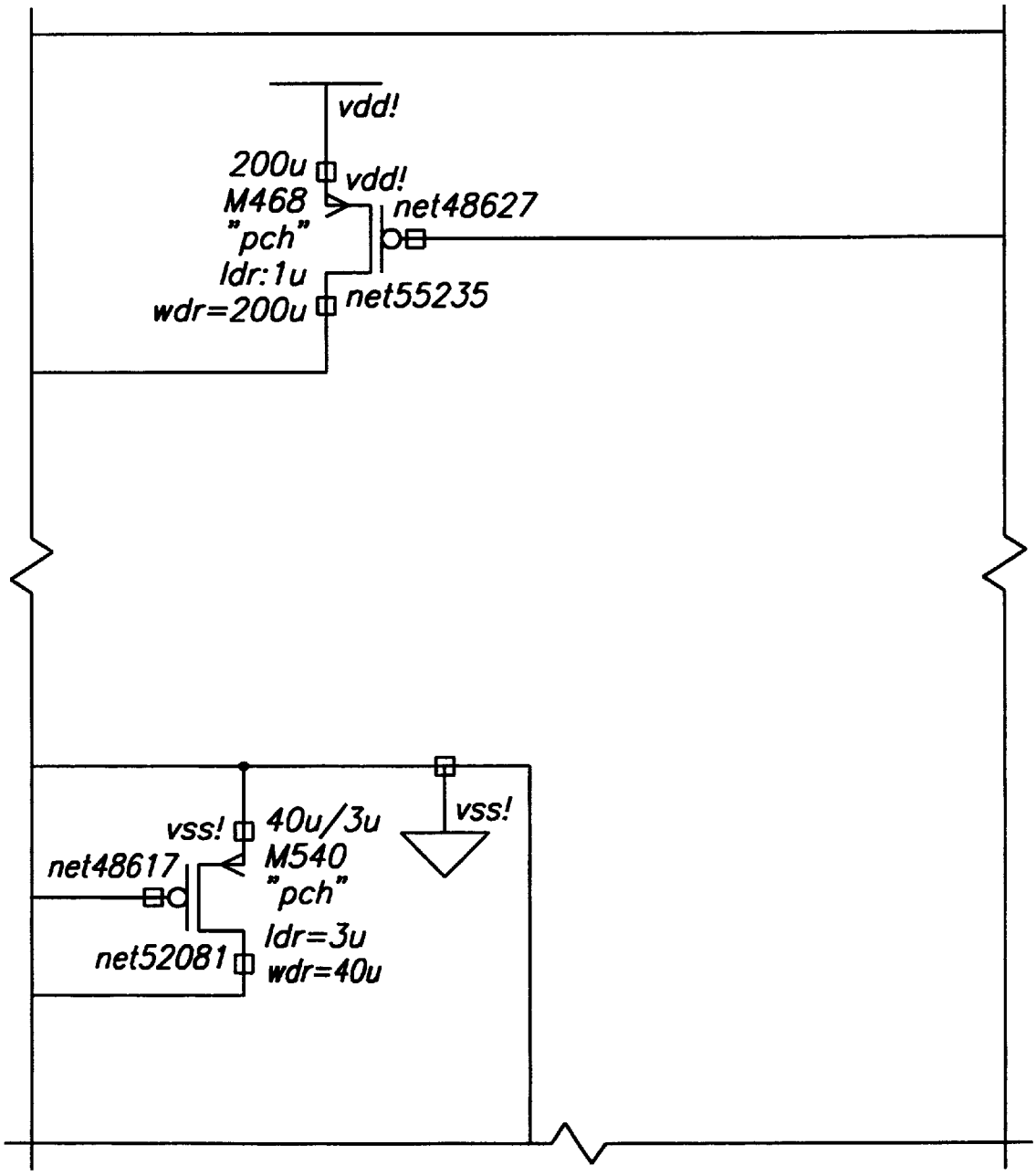

vdd!
200u
M468
"pch"
ldr:1u
wdr=200u
vdd!
net48627
net55235
vss!
net48617
net52081
40u/3u
M540
"pch"
ldr=3u
wdr=40u
vss!

Fig 1646

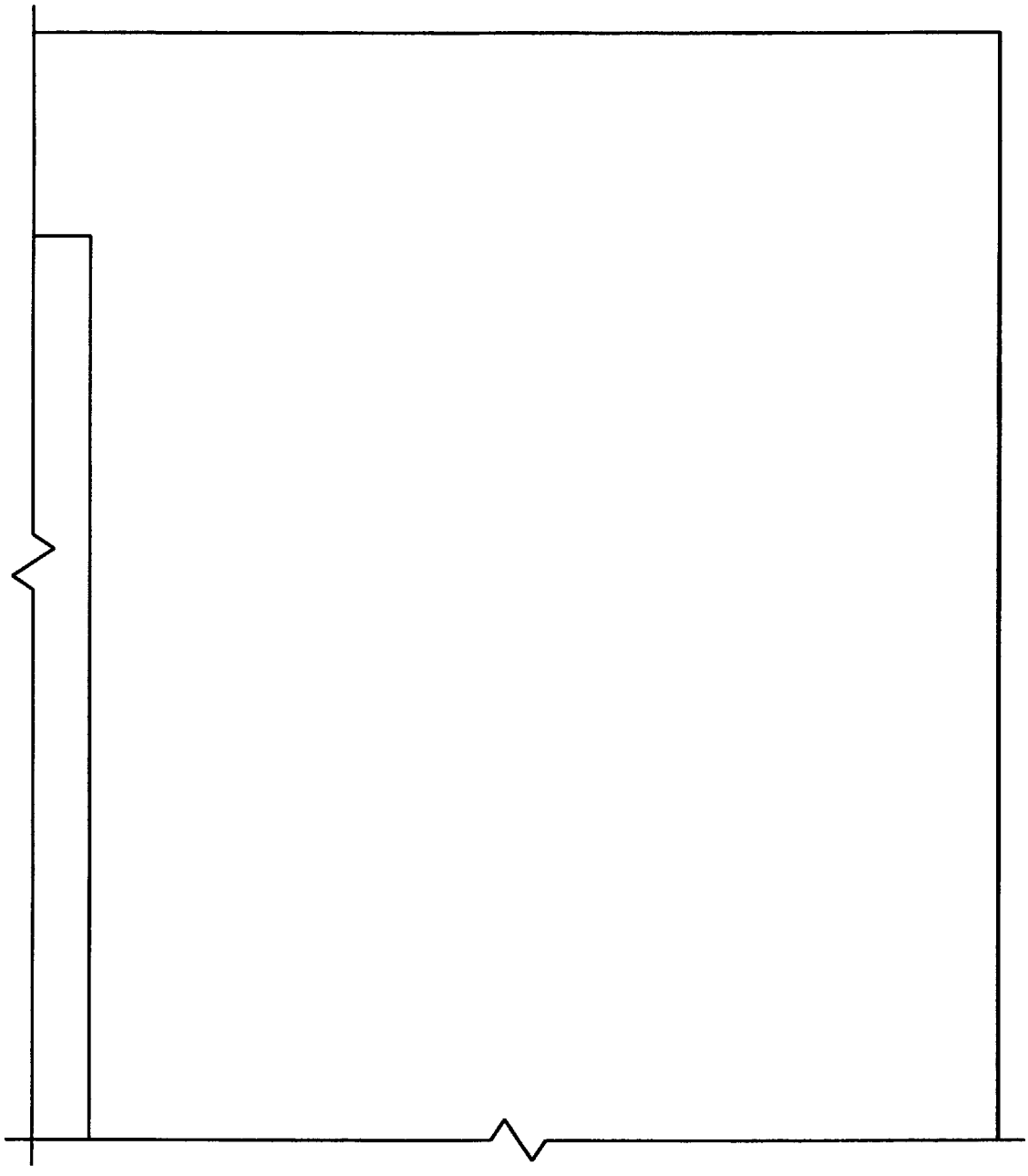


Fig 16AH

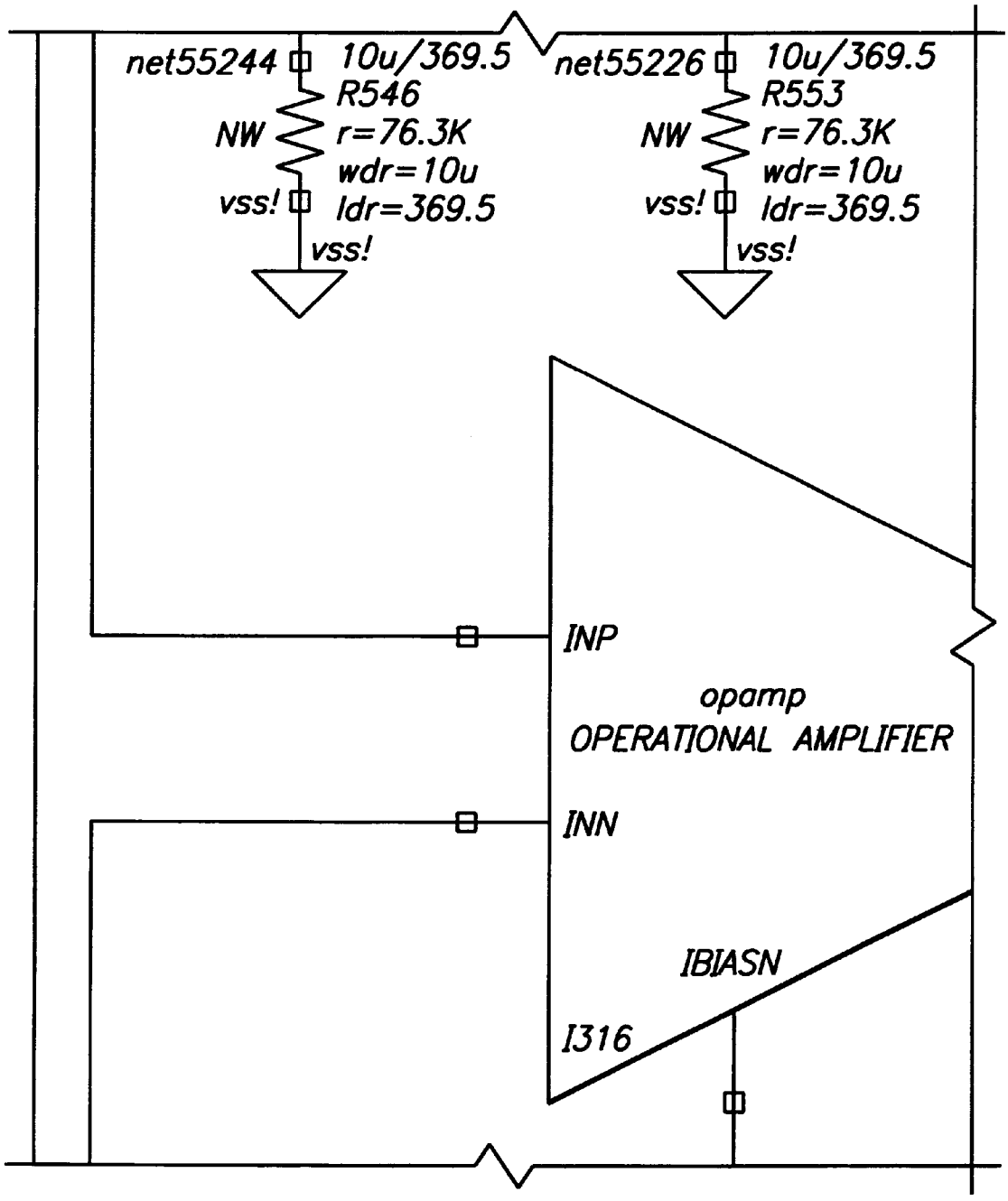

net55244
10u/369.5
R546
NW
r=76.3K
wdr=10u
vss!
ldr=369.5
vss!
net55226
10u/369.5
R553
NW
r=76.3K
wdr=10u
vss!
ldr=369.5
vss!
INP
opamp
OPERATIONAL AMPLIFIER
INN
IBIASN
I316

Fig 16BA

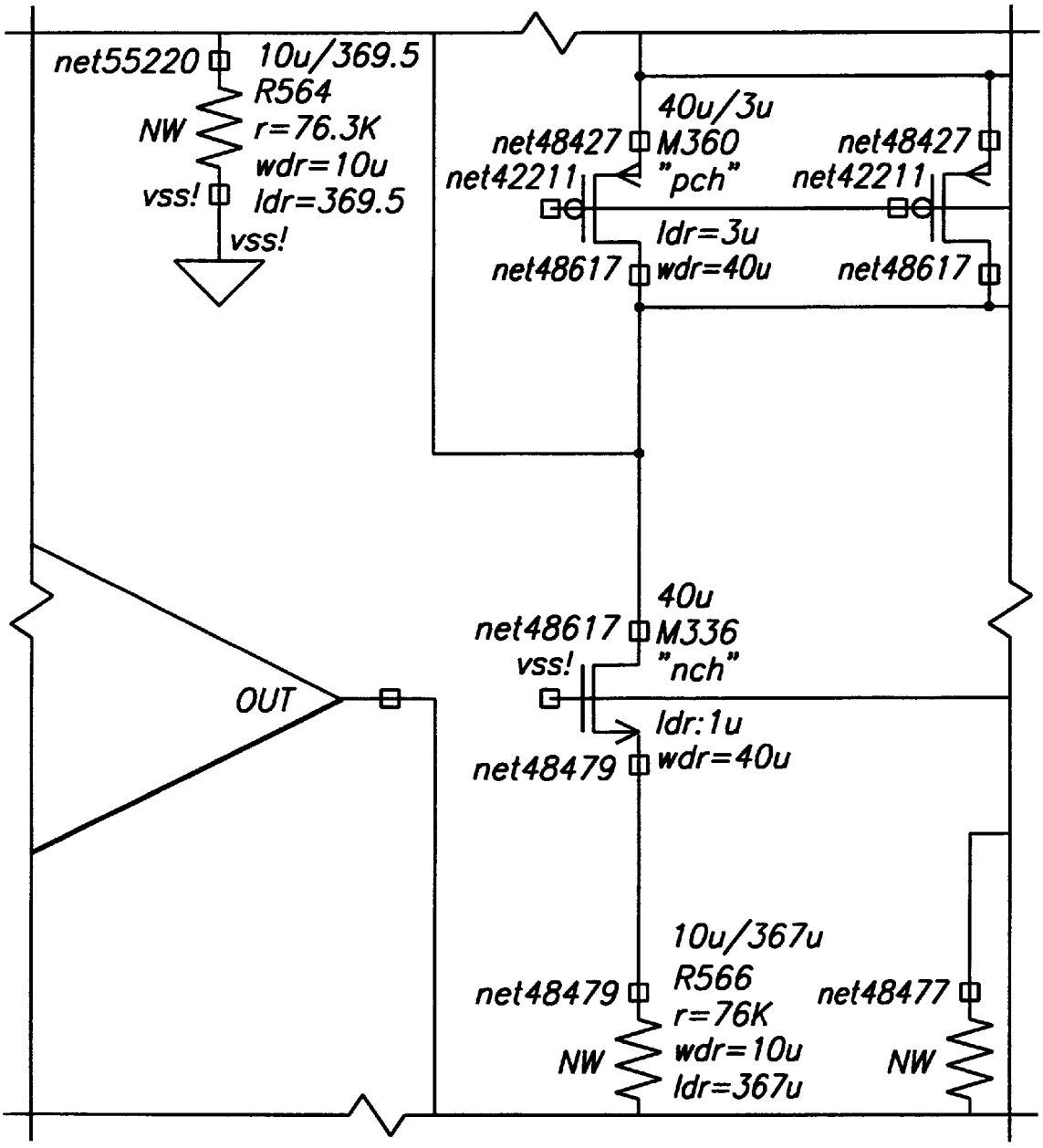

net55220
10u/369.5
R564
NW
r=76.3K
wdr=10u
vss!
ldr=369.5
vss!
40u/3u
net48427
M360
"pch"
net48427
net42211
net42211
ldr=3u
net48617
wdr=40u
net48617
40u
net48617
M336
"nch"
vss!
OUT
ldr:1u
net48479
wdr=40u
10u/367u
net48479
R566
r=76K
net48477
NW
wdr=10u
NW
ldr=367u

FIG 1088

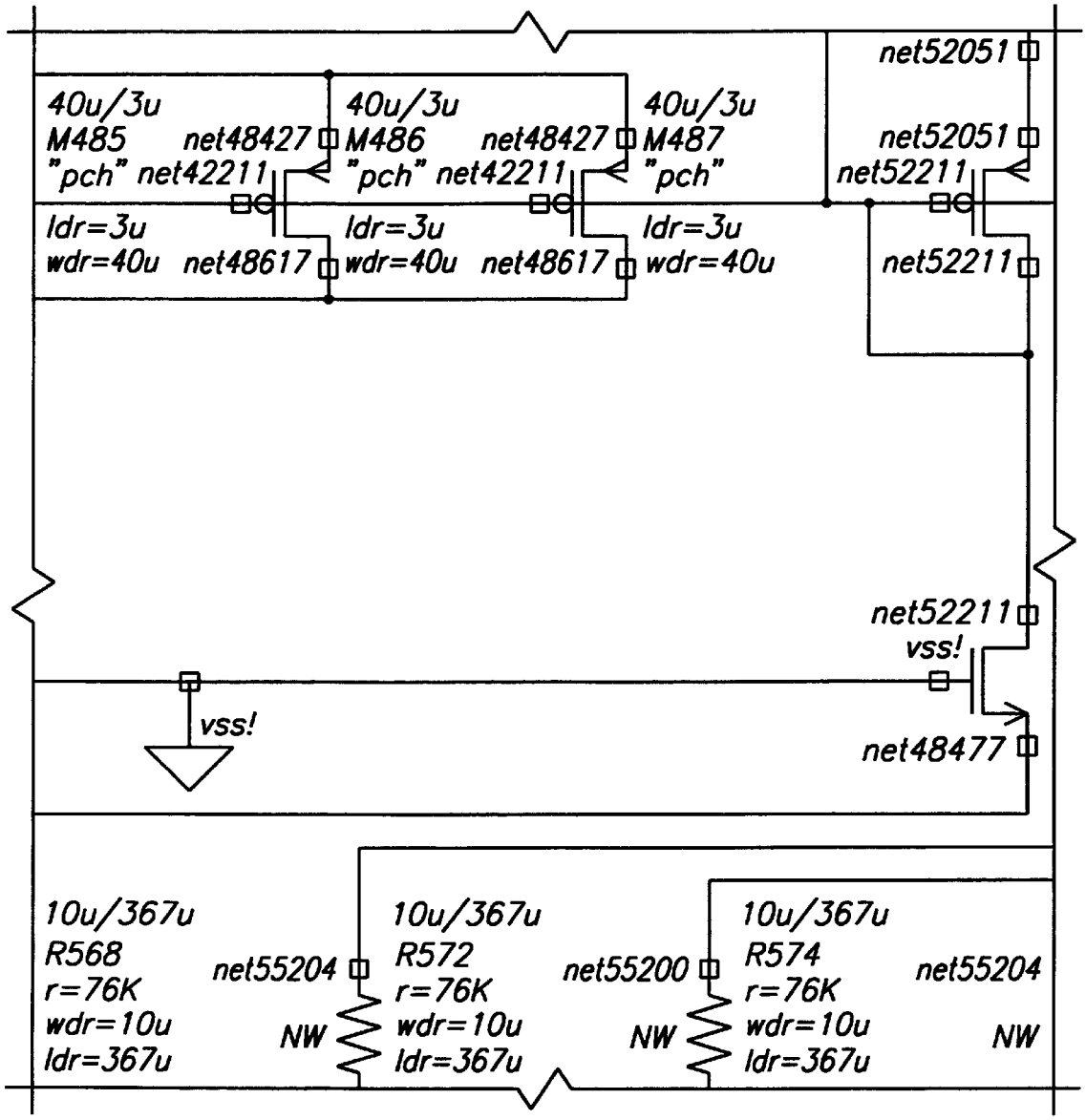

net52051
40u/3u
M485
"pch"
net48427
net42211
ldr=3u
wdr=40u
net48617
40u/3u
M486
"pch"
net48427
net42211
ldr=3u
wdr=40u
net48617
40u/3u
M487
"pch"
ldr=3u
wdr=40u
net52051
net52211
net52211
net52211
vss!
net48477
vss!
10u/367u
R568
r=76K
wdr=10u
ldr=367u
net55204
NW
10u/367u
R572
r=76K
wdr=10u
ldr=367u
net55200
NW
10u/367u
R574
r=76K
wdr=10u
ldr=367u
net55204
NW

FIG 16BC

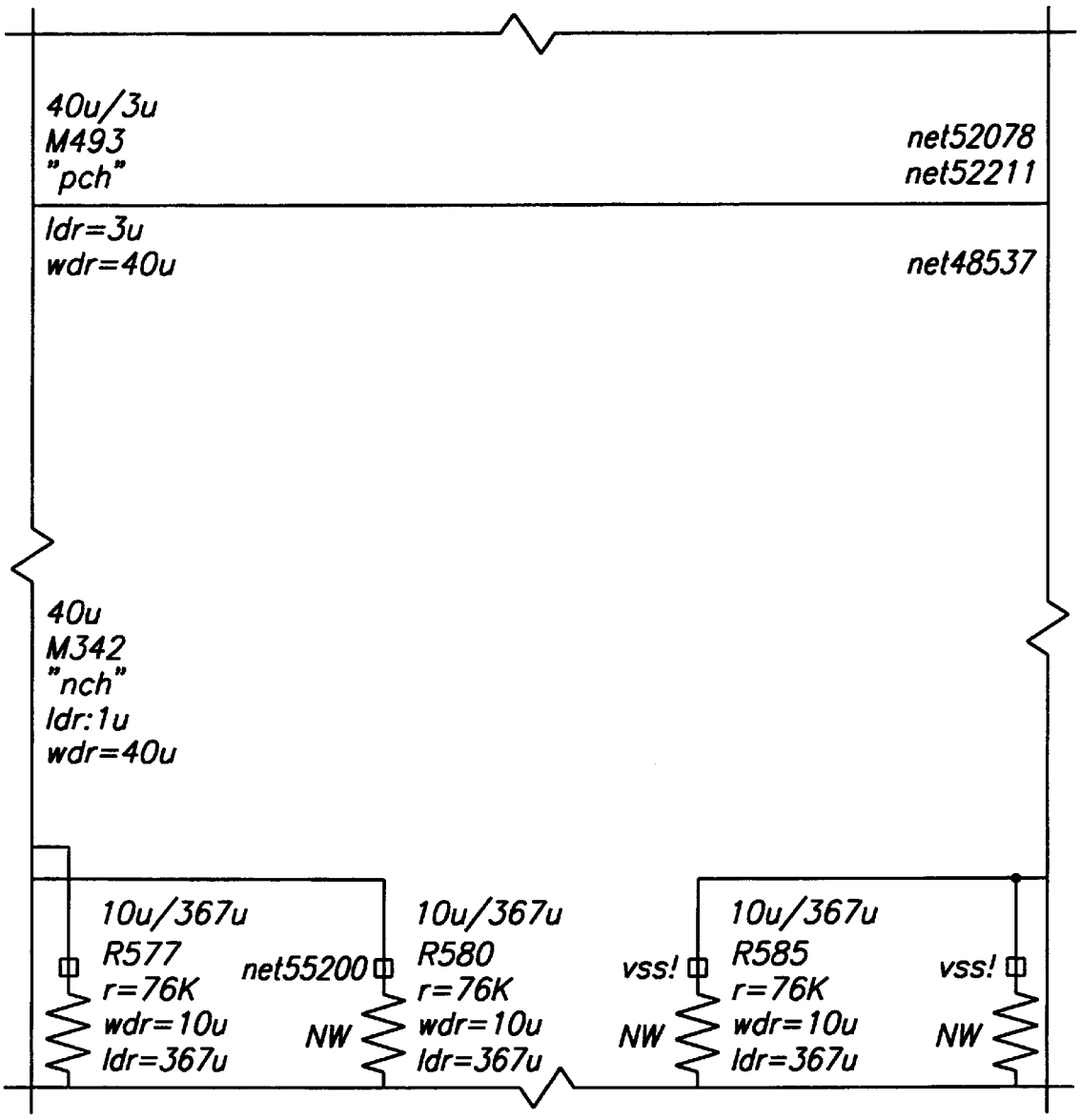

40u/3u
M493
"pch"
ldr=3u
wdr=40u
net52078
net52211
net48537
40u
M342
"nch"
ldr:1u
wdr=40u
10u/367u
R577
r=76K
wdr=10u
ldr=367u
net55200
NW
10u/367u
R580
r=76K
wdr=10u
ldr=367u
vss!
NW
10u/367u
R585
r=76K
wdr=10u
ldr=367u
vss!
NW

Fig 1680

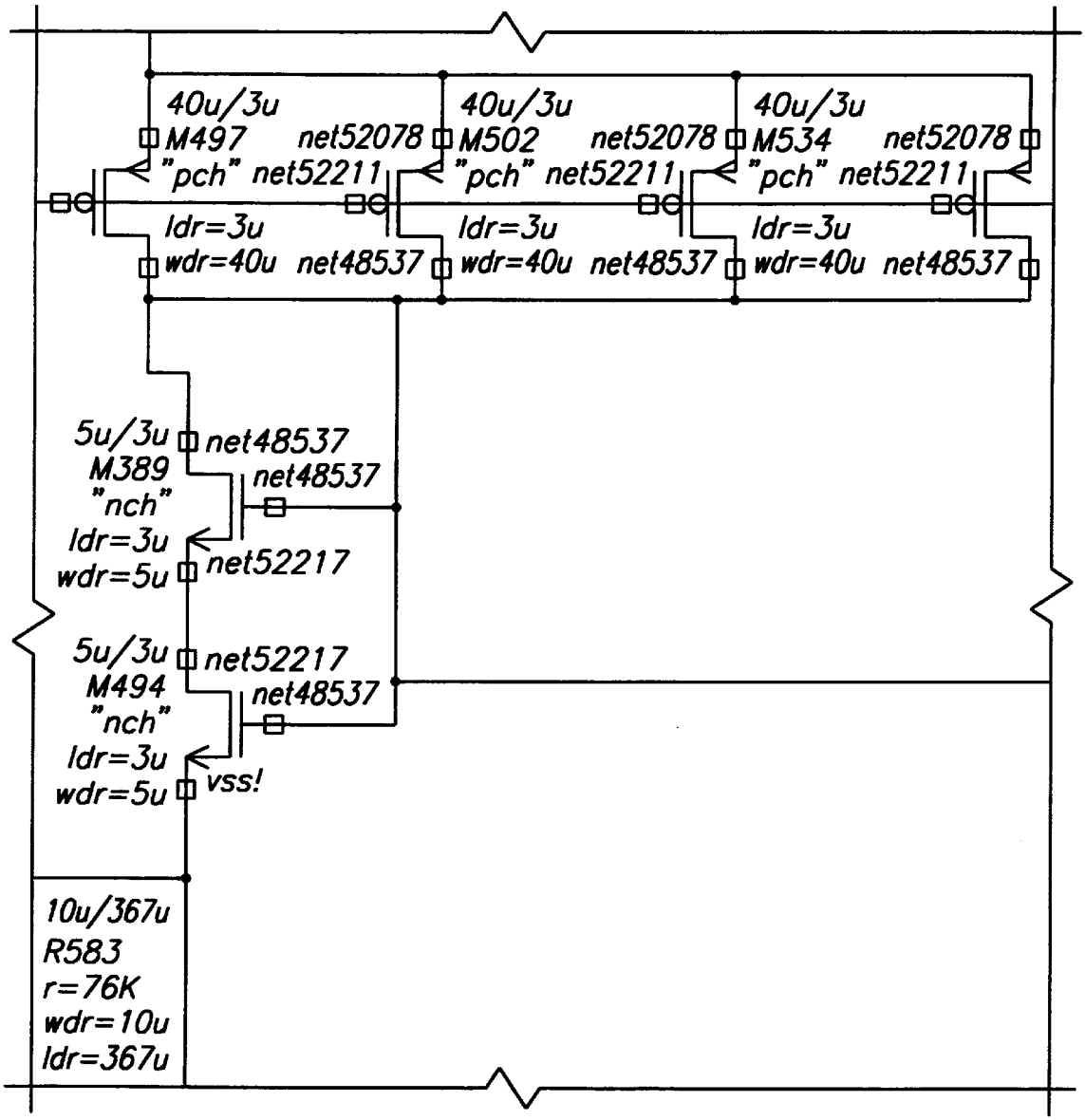

40u/3u
M497
"pch"
net52078
net52211
ldr=3u
wdr=40u
net48537
40u/3u
M502
"pch"
net52078
net52211
ldr=3u
wdr=40u
net48537
40u/3u
M534
"pch"
net52078
net52211
ldr=3u
wdr=40u
net48537
5u/3u
M389
"nch"
ldr=3u
wdr=5u
net48537
net48537
net52217
5u/3u
M494
"nch"
ldr=3u
wdr=5u
net52217
net48537
vss!
10u/367u
R583
r=76K
wdr=10u
ldr=367u

Fig 16BE

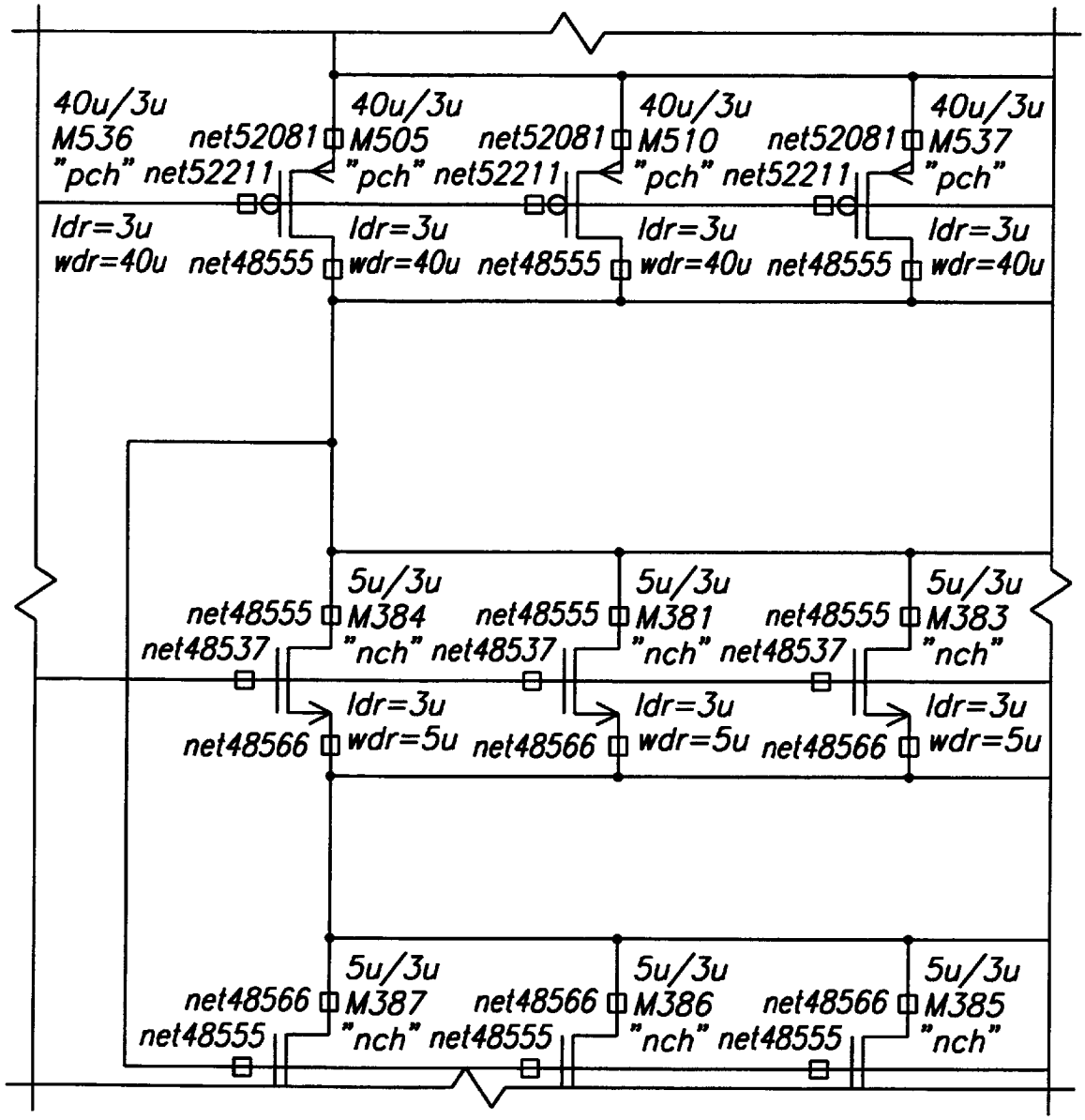

40u/3u
M536
"pch"
net52081
net52211
ldr=3u
wdr=40u
net48555
40u/3u
M505
"pch"
net52081
net52211
ldr=3u
wdr=40u
net48555
40u/3u
M510
"pch"
net52081
net52211
ldr=3u
wdr=40u
net48555
40u/3u
M537
"pch"
ldr=3u
wdr=40u
5u/3u
M384
"nch"
net48555
net48537
ldr=3u
wdr=5u
net48566
5u/3u
M381
"nch"
net48555
net48537
ldr=3u
wdr=5u
net48566
5u/3u
M383
"nch"
net48555
net48537
ldr=3u
wdr=5u
net48566
5u/3u
M387
"nch"
net48566
net48555
5u/3u
M386
"nch"
net48566
net48555
5u/3u
M385
"nch"
net48566
net48555

Fig 16BF

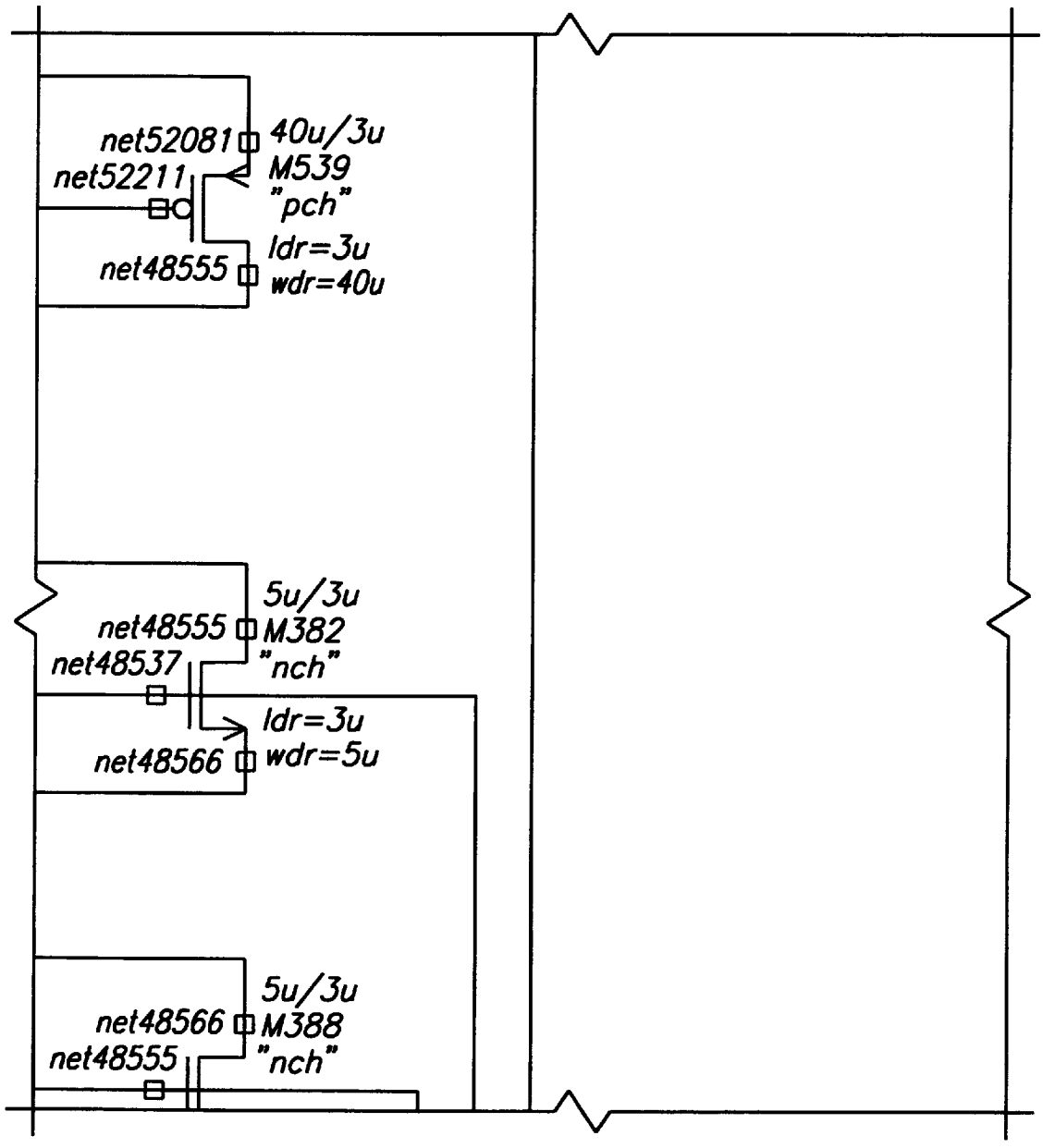

net52081
net52211
net48555
40u/3u
M539
"pch"
ldr=3u
wdr=40u
net48555
net48537
net48566
5u/3u
M382
"nch"
ldr=3u
wdr=5u
net48566
net48555
5u/3u
M388
"nch"

Fig 1686

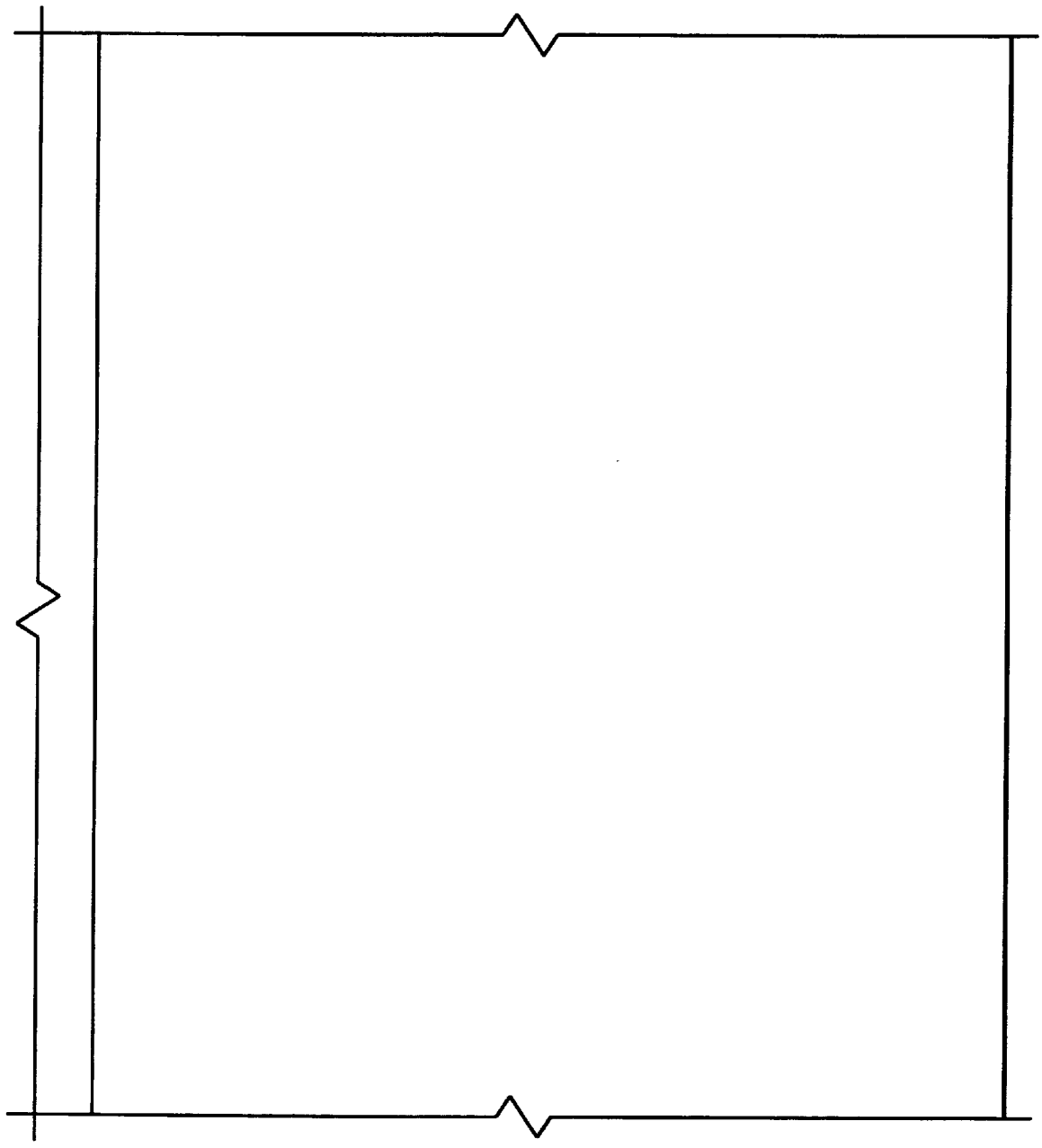


Fig 16BH

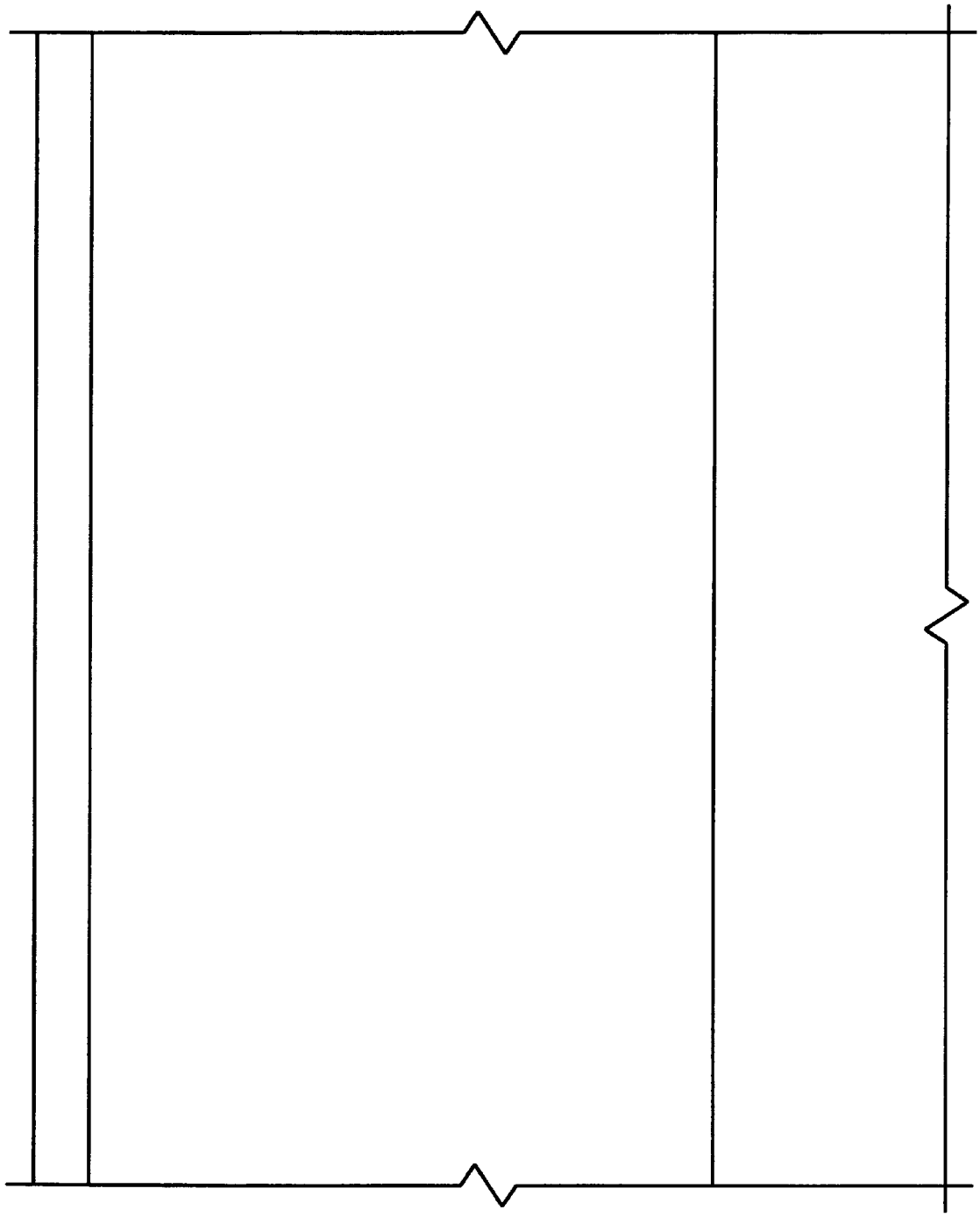


Fig 16CA

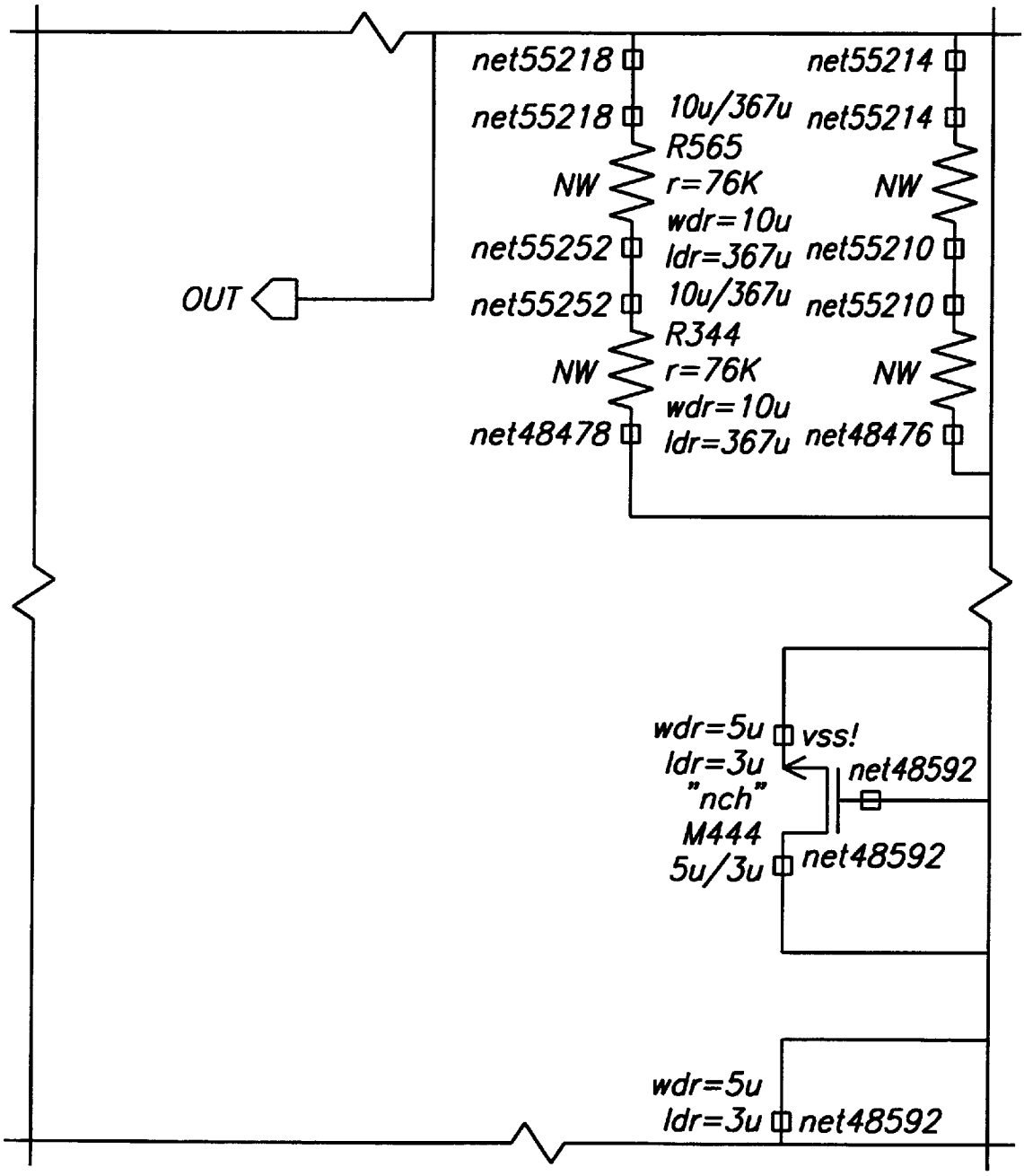

net55218
net55218
10u/367u
R565
NW
r=76K
wdr=10u
net55252
ldr=367u
OUT
net55252
10u/367u
R344
NW
r=76K
wdr=10u
net48478
ldr=367u
net55214
net55214
NW
net55210
net55210
NW
net48476
wdr=5u
ldr=3u
"nch"
M444
5u/3u
vss!
net48592
net48592
wdr=5u
ldr=3u
net48592

Fig 16CB

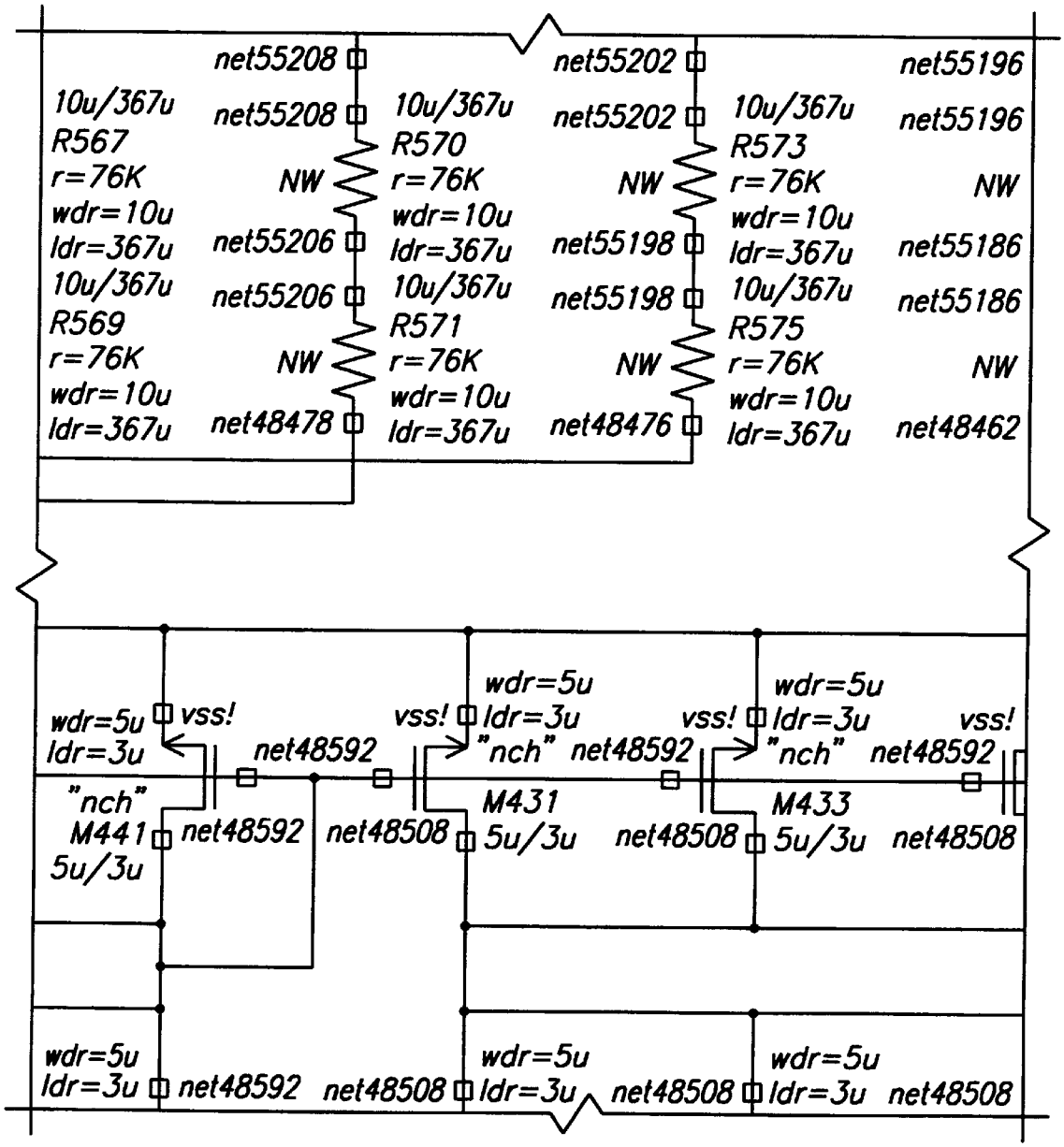

net55208
net55202
net55196
10u/367u
R567
r=76K
wdr=10u
ldr=367u
net55208
NW
net55206
10u/367u
R569
r=76K
wdr=10u
ldr=367u
net48478
10u/367u
R570
r=76K
wdr=10u
ldr=367u
10u/367u
R571
r=76K
wdr=10u
ldr=367u
net48476
net55202
NW
net55198
10u/367u
R573
r=76K
wdr=10u
ldr=367u
net55198
NW
10u/367u
R575
r=76K
wdr=10u
ldr=367u
net48462
net55196
NW
net55186
net55186
NW
wdr=5u
ldr=3u
vss!
net48592
"nch"
M441
5u/3u
net48592
net48508
M431
5u/3u
net48508
M433
5u/3u
net48508

Fig 16C

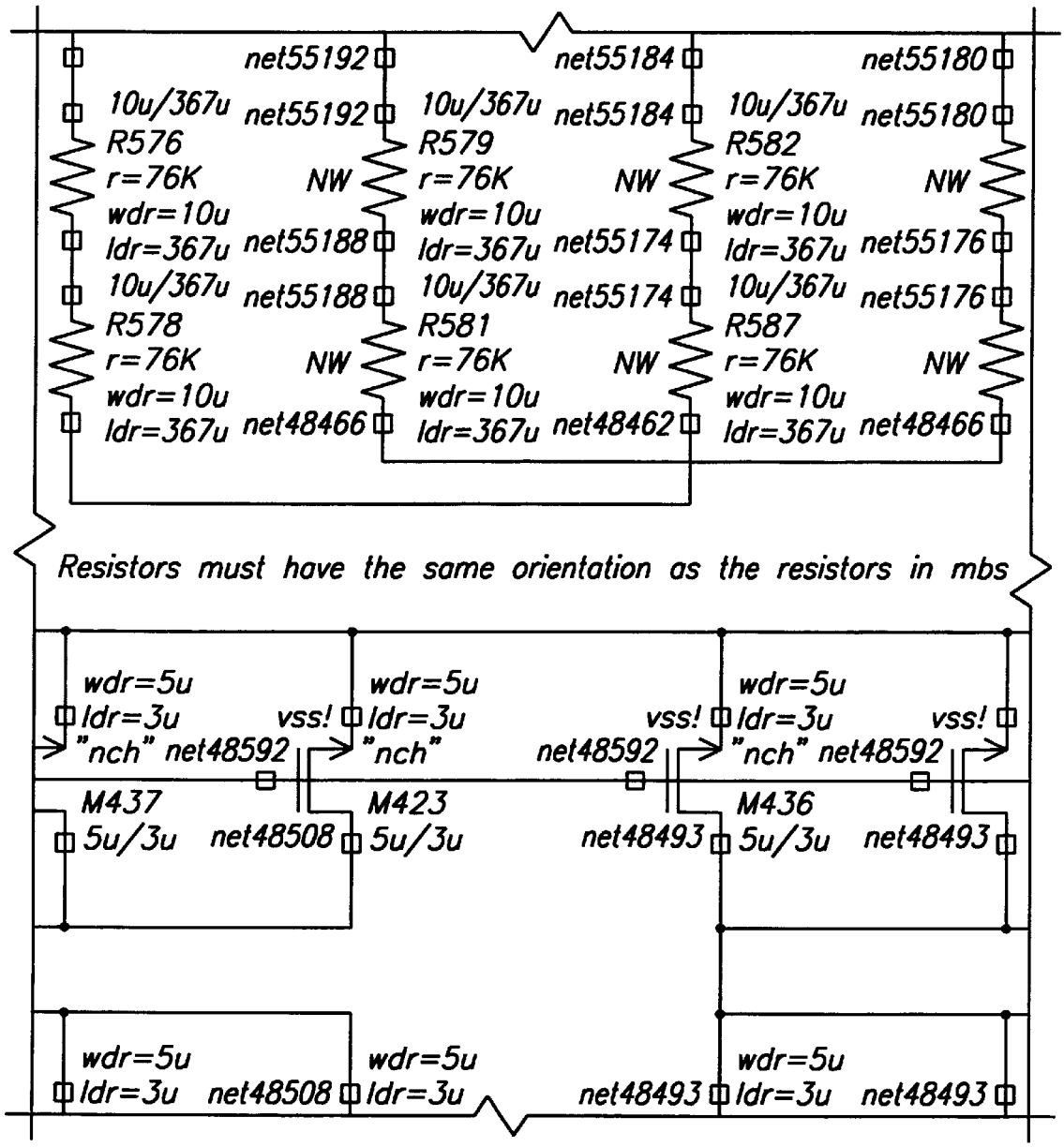

net55192
net55184
net55180
10u/367u
R576
r=76K
wdr=10u
ldr=367u
NW
net55188
10u/367u
R578
r=76K
wdr=10u
ldr=367u
net48466
10u/367u
R579
r=76K
wdr=10u
ldr=367u
net55174
10u/367u
R581
r=76K
wdr=10u
ldr=367u
net48462
10u/367u
R582
r=76K
wdr=10u
ldr=367u
net55176
10u/367u
R587
r=76K
wdr=10u
ldr=367u
Resistors must have the same orientation as the resistors in mbs
wdr=5u
ldr=3u
"nch"
net48592
vss!
M437
5u/3u
net48508
M423
5u/3u
M436
5u/3u
net48493

Fig 16CD

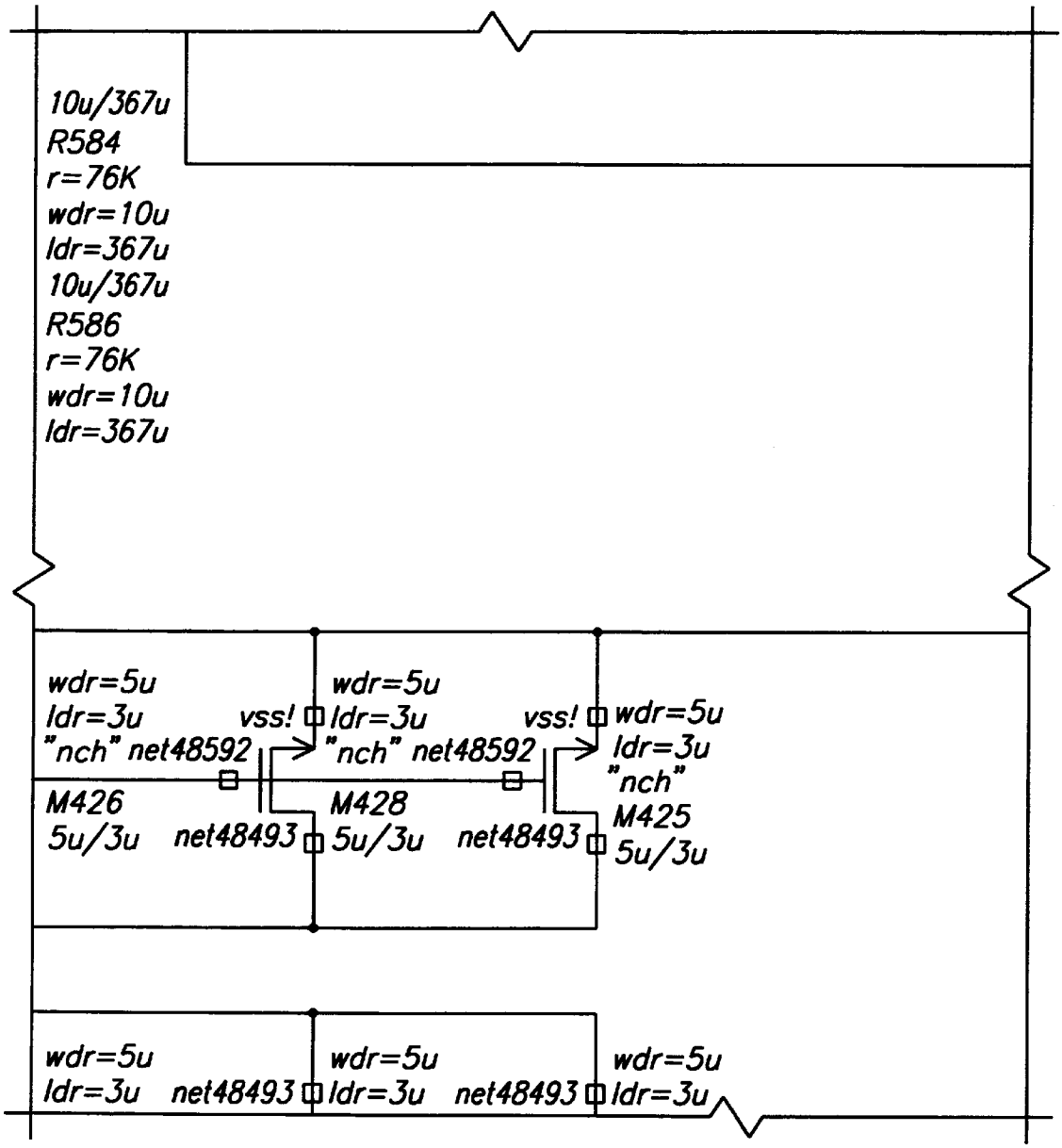

10u/367u
R584
r=76K
wdr=10u
ldr=367u
10u/367u
R586
r=76K
wdr=10u
ldr=367u
wdr=5u
ldr=3u
"nch"
M426
5u/3u
vss!
net48592
net48493
wdr=5u
ldr=3u
"nch"
M428
5u/3u
vss!
net48592
net48493
wdr=5u
ldr=3u
"nch"
M425
5u/3u
wdr=5u
ldr=3u
net48493
wdr=5u
ldr=3u
net48493
wdr=5u
ldr=3u

Fig 16CE

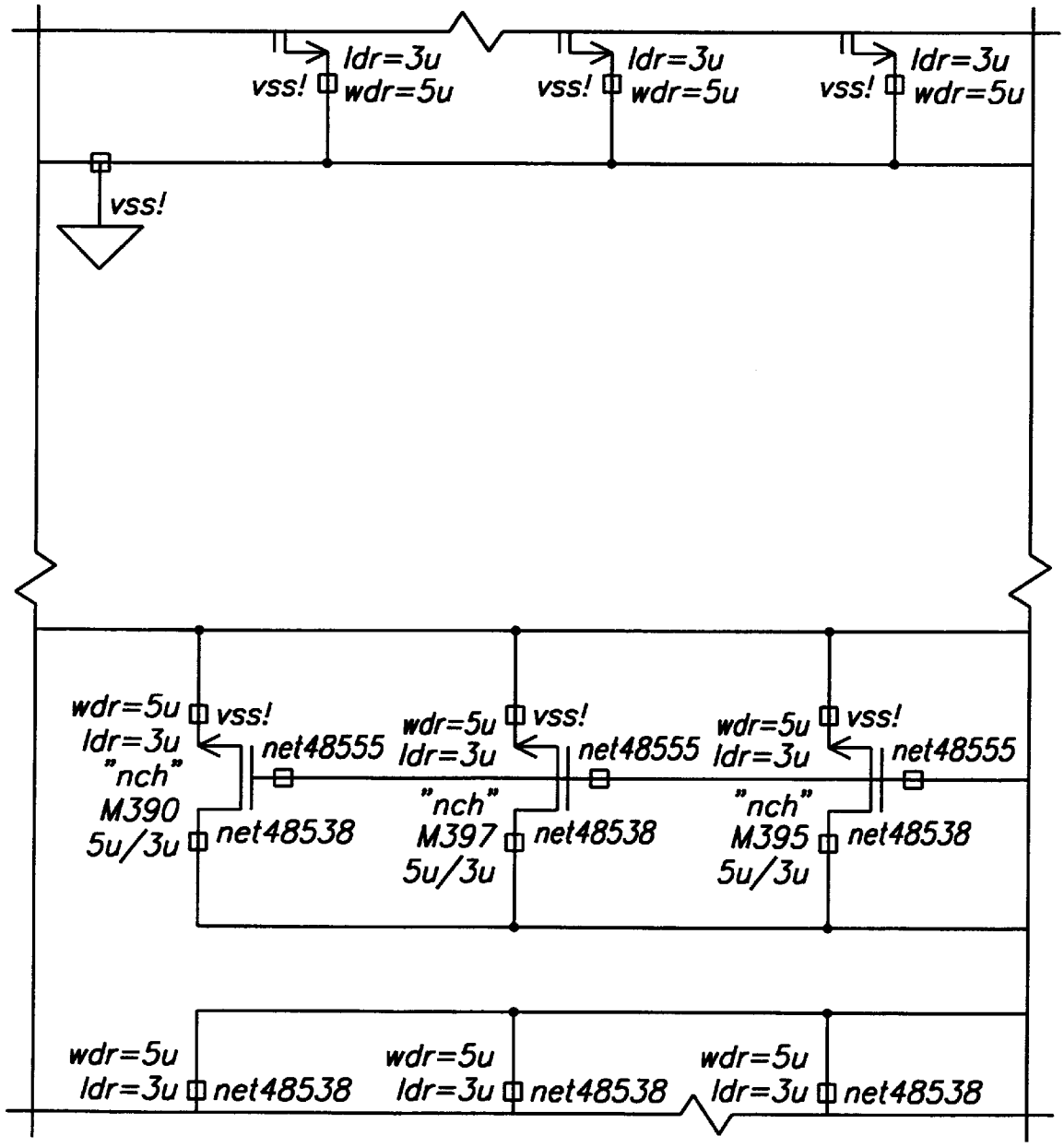

ldr=3u
wdr=5u
vss!
ldr=3u
wdr=5u
vss!
ldr=3u
wdr=5u
vss!
vss!
wdr=5u
ldr=3u
"nch"
M390
5u/3u
vss!
net48555
net48538
wdr=5u
ldr=3u
"nch"
M397
5u/3u
vss!
net48555
net48538
wdr=5u
ldr=3u
"nch"
M395
5u/3u
vss!
net48555
net48538
wdr=5u
ldr=3u
net48538
wdr=5u
ldr=3u
net48538
wdr=5u
ldr=3u
net48538

Fig 16CF

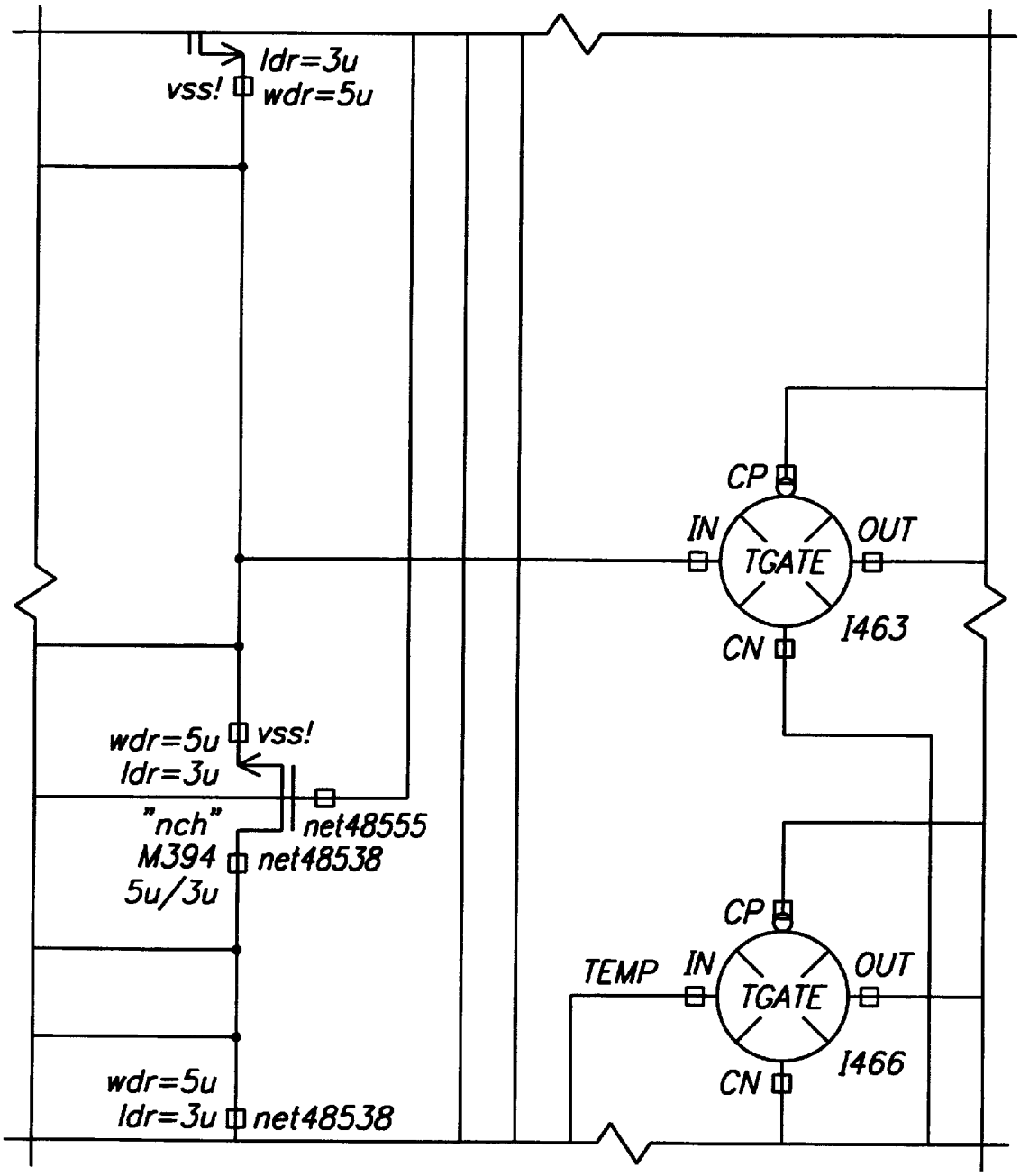

ldr=3u
vss!
wdr=5u
CP
IN
OUT
TGATE
I463
CN
wdr=5u
vss!
ldr=3u
"nch"
M394
5u/3u
net48555
net48538
CP
TEMP
IN
OUT
TGATE
I466
CN
wdr=5u
ldr=3u
net48538

Fig 166

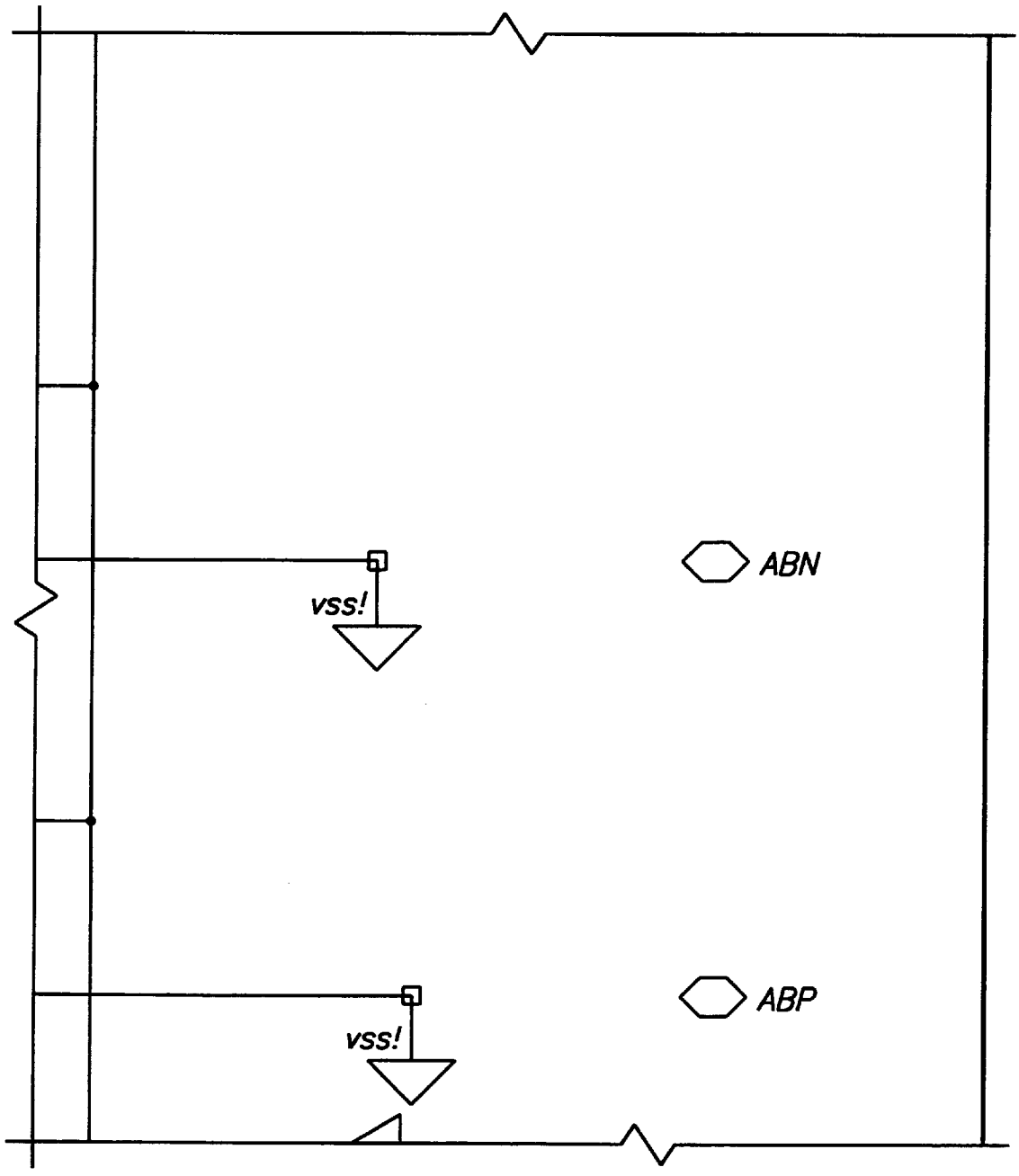


Fig 16CH

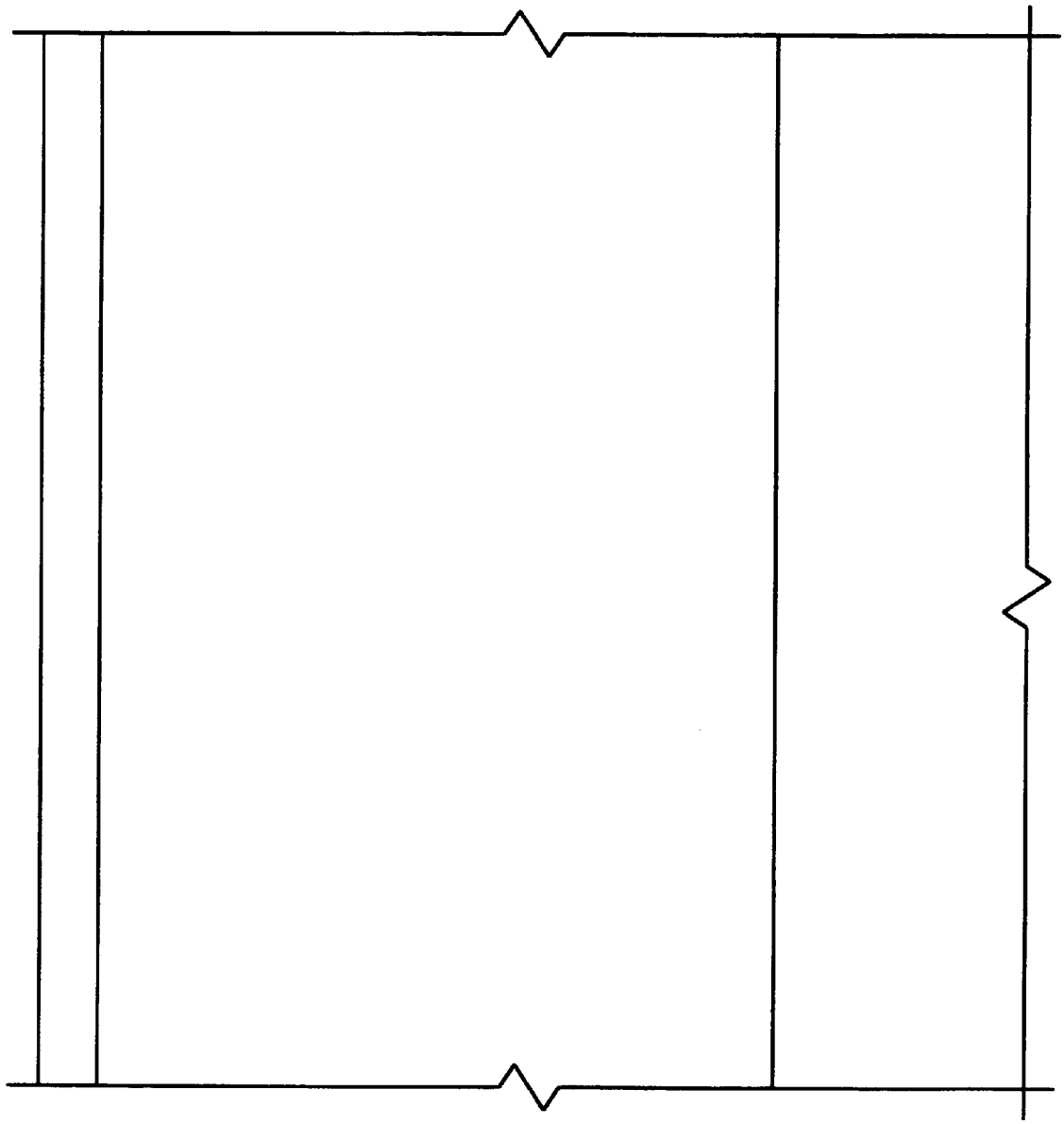


Fig 16DA

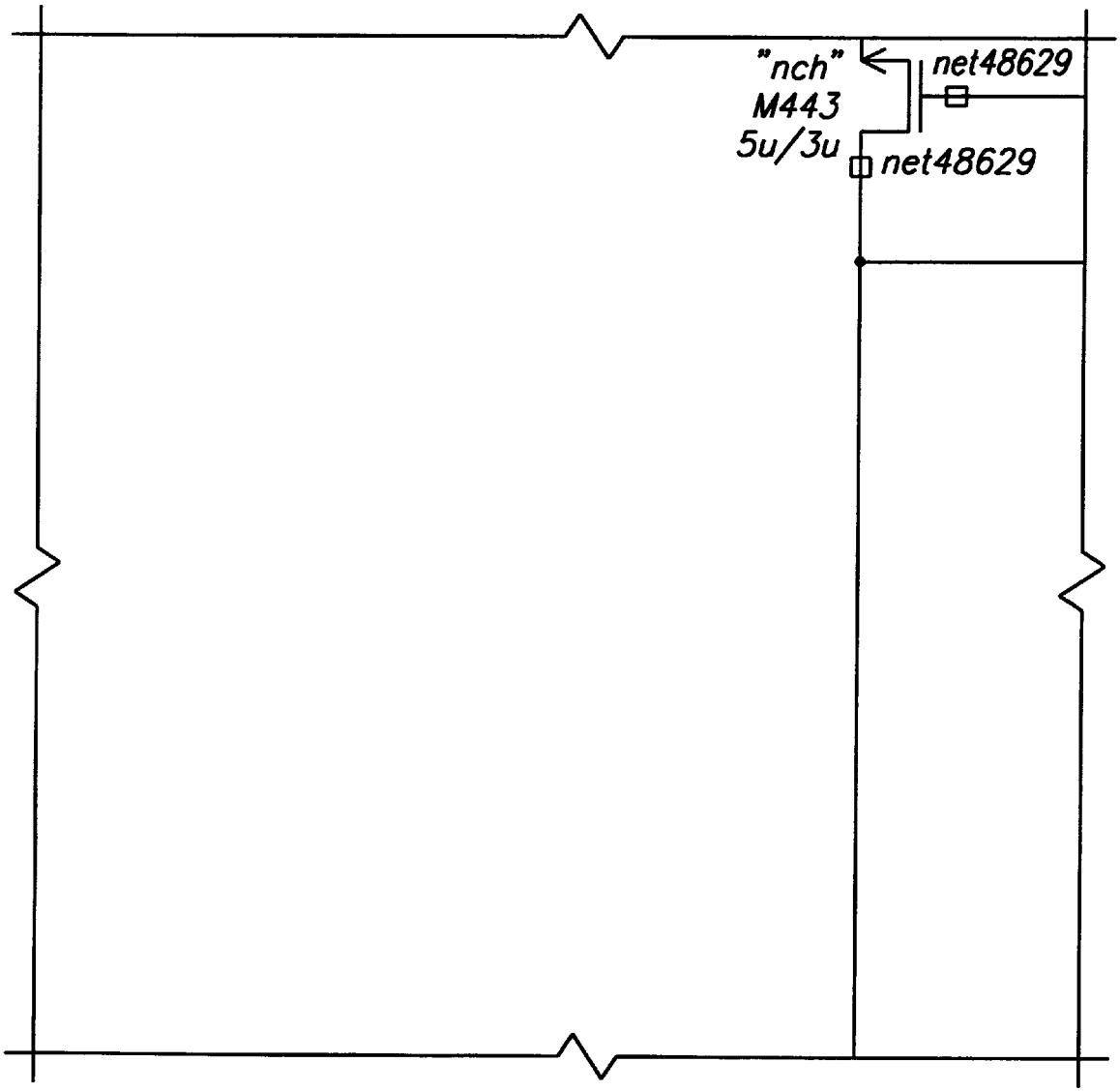


Fig 160B

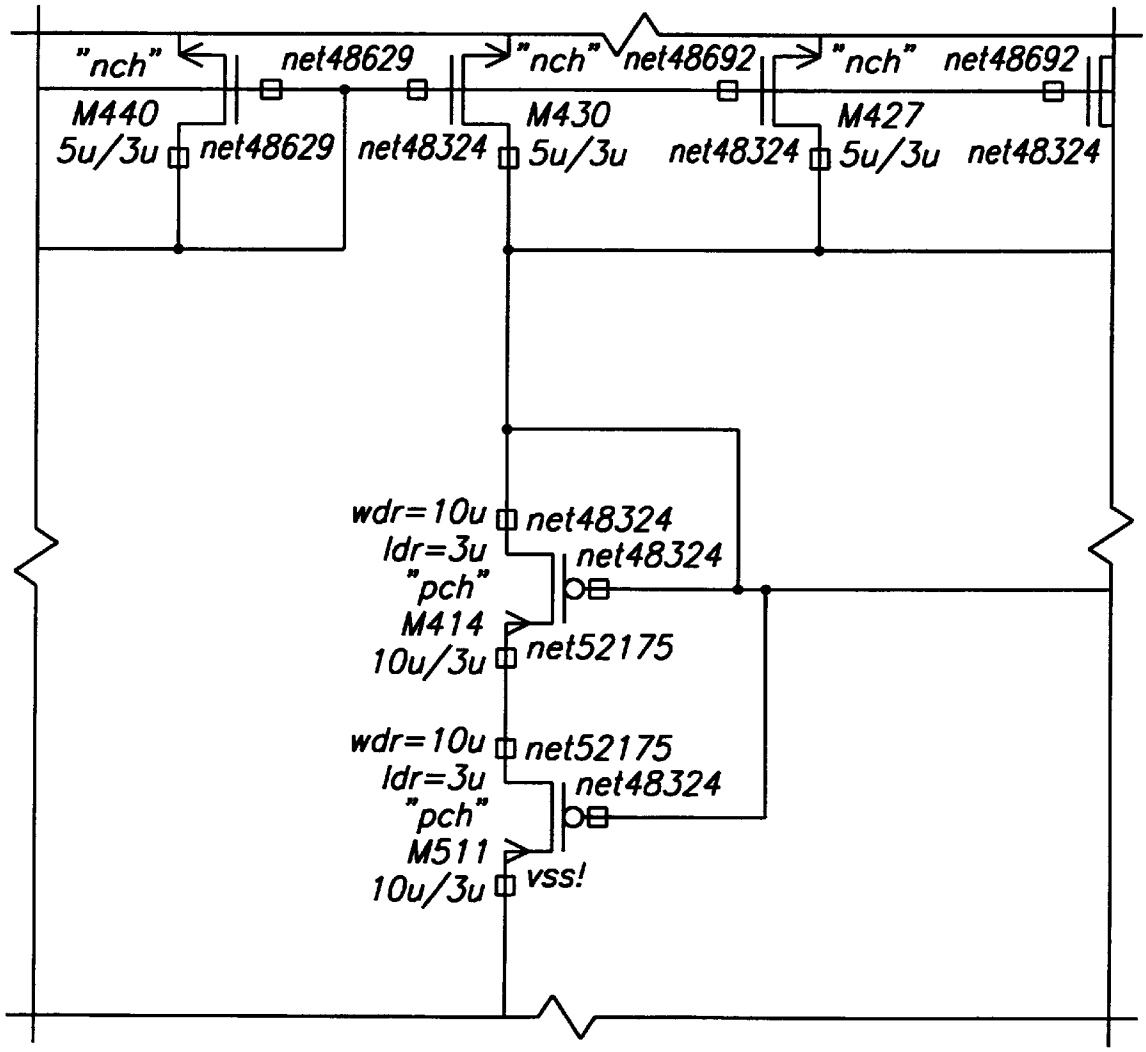

"nch"
net48629
"nch"
net48692
"nch"
net48692
M440
5u/3u
net48629
net48324
M430
5u/3u
net48324
M427
5u/3u
net48324
wdr=10u
ldr=3u
"pch"
M414
10u/3u
net48324
net52175
wdr=10u
ldr=3u
"pch"
M511
10u/3u
net52175
net48324
vss!

Fig 160C

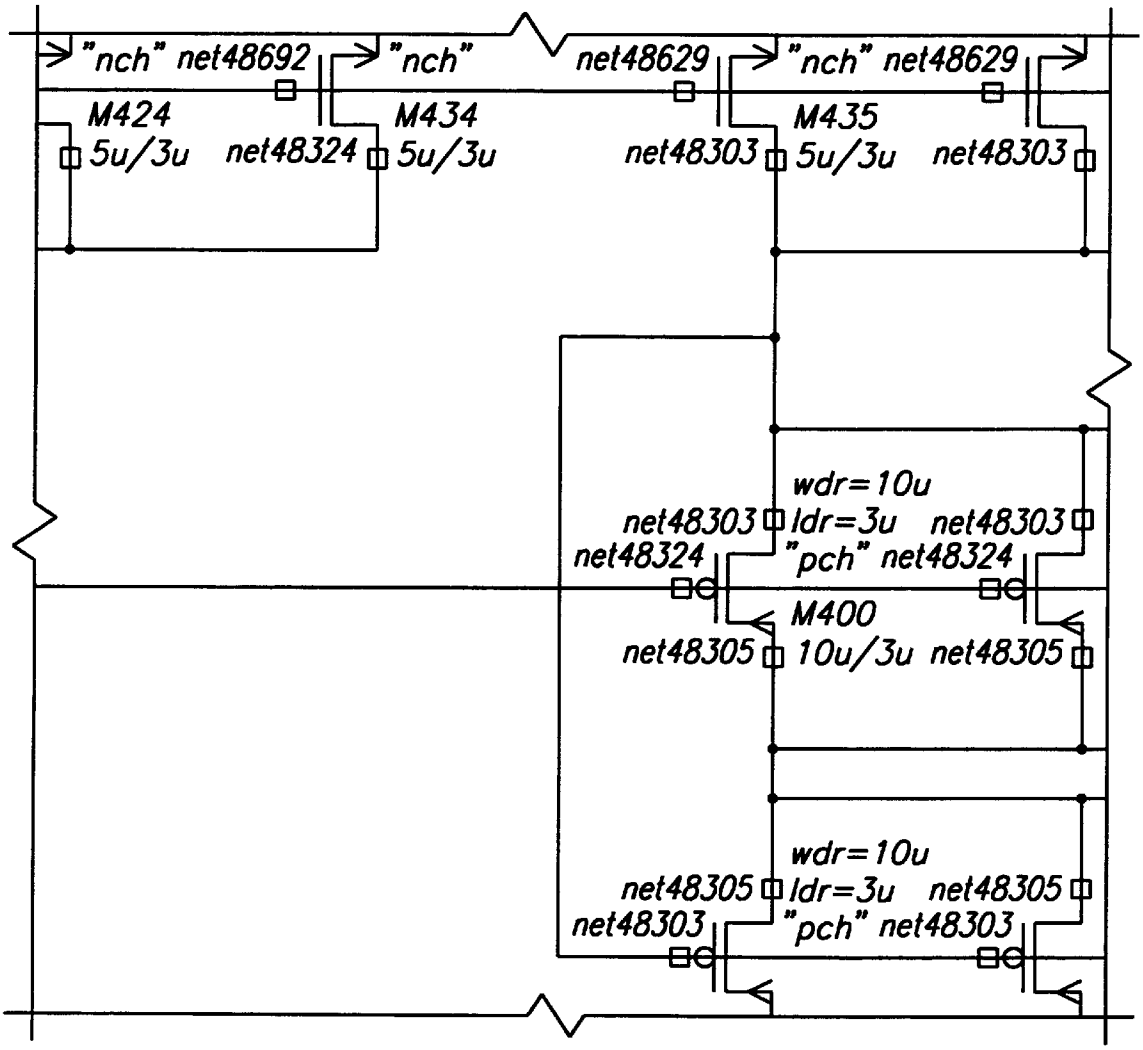

"nch" net48692
"nch"
net48629
"nch" net48629
M424
5u/3u
net48324
M434
5u/3u
net48303
M435
5u/3u
net48303
wdr=10u
net48303
ldr=3u
net48303
net48324
"pch" net48324
M400
net48305
10u/3u
net48305
wdr=10u
net48305
ldr=3u
net48305
net48303
"pch" net48303

Fig 1600

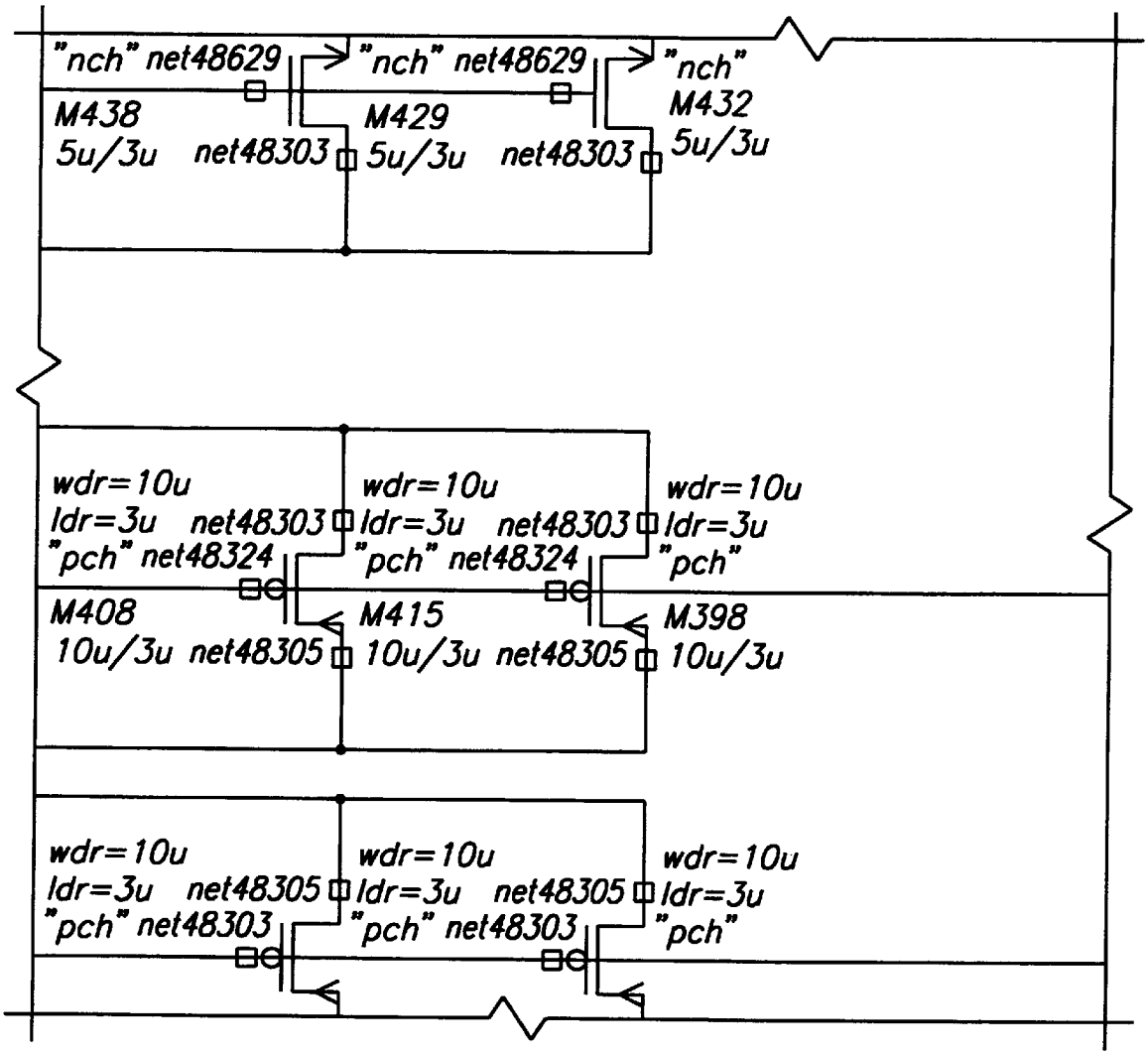

"nch" net48629
"nch" net48629
"nch"
M438
5u/3u
net48303
M429
5u/3u
net48303
M432
5u/3u
wdr=10u
ldr=3u
"pch"
net48303
net48324
wdr=10u
ldr=3u
"pch"
net48303
net48324
wdr=10u
ldr=3u
"pch"
M408
10u/3u
net48305
M415
10u/3u
net48305
M398
10u/3u
wdr=10u
ldr=3u
"pch"
net48305
net48303
wdr=10u
ldr=3u
"pch"
net48305
net48303
wdr=10u
ldr=3u
"pch"

Fig 16DE

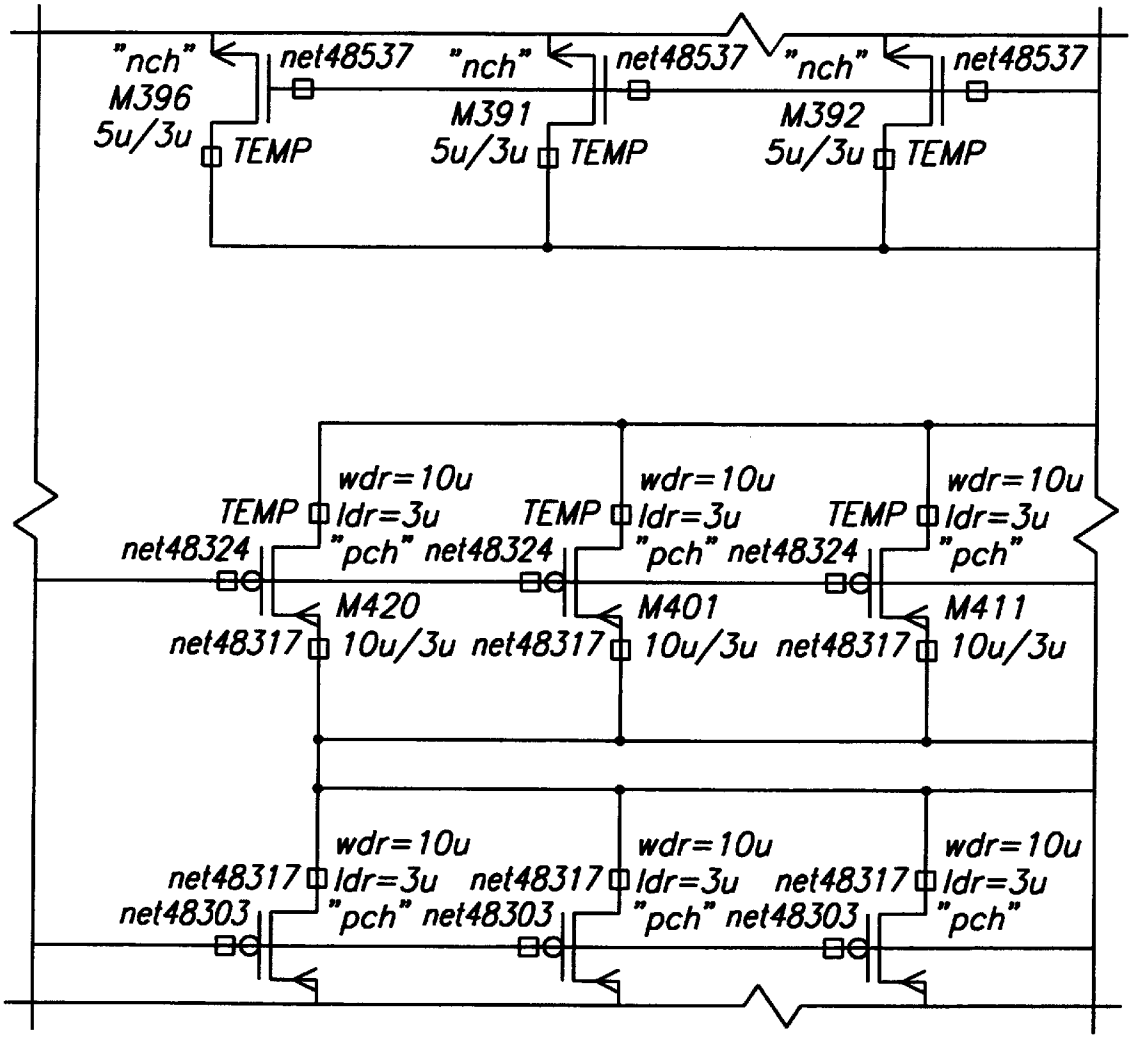

"nch"
M396
5u/3u
net48537
TEMP
"nch"
M391
5u/3u
net48537
TEMP
"nch"
M392
5u/3u
net48537
TEMP
wdr=10u
ldr=3u
"pch"
net48324
M420
10u/3u
net48317
wdr=10u
ldr=3u
"pch"
net48324
M401
10u/3u
net48317
wdr=10u
ldr=3u
"pch"
net48324
M411
10u/3u
net48317
wdr=10u
ldr=3u
"pch"
net48303
net48317
wdr=10u
ldr=3u
"pch"
net48303
net48317
wdr=10u
ldr=3u
"pch"
net48303
net48317

Fig 160F

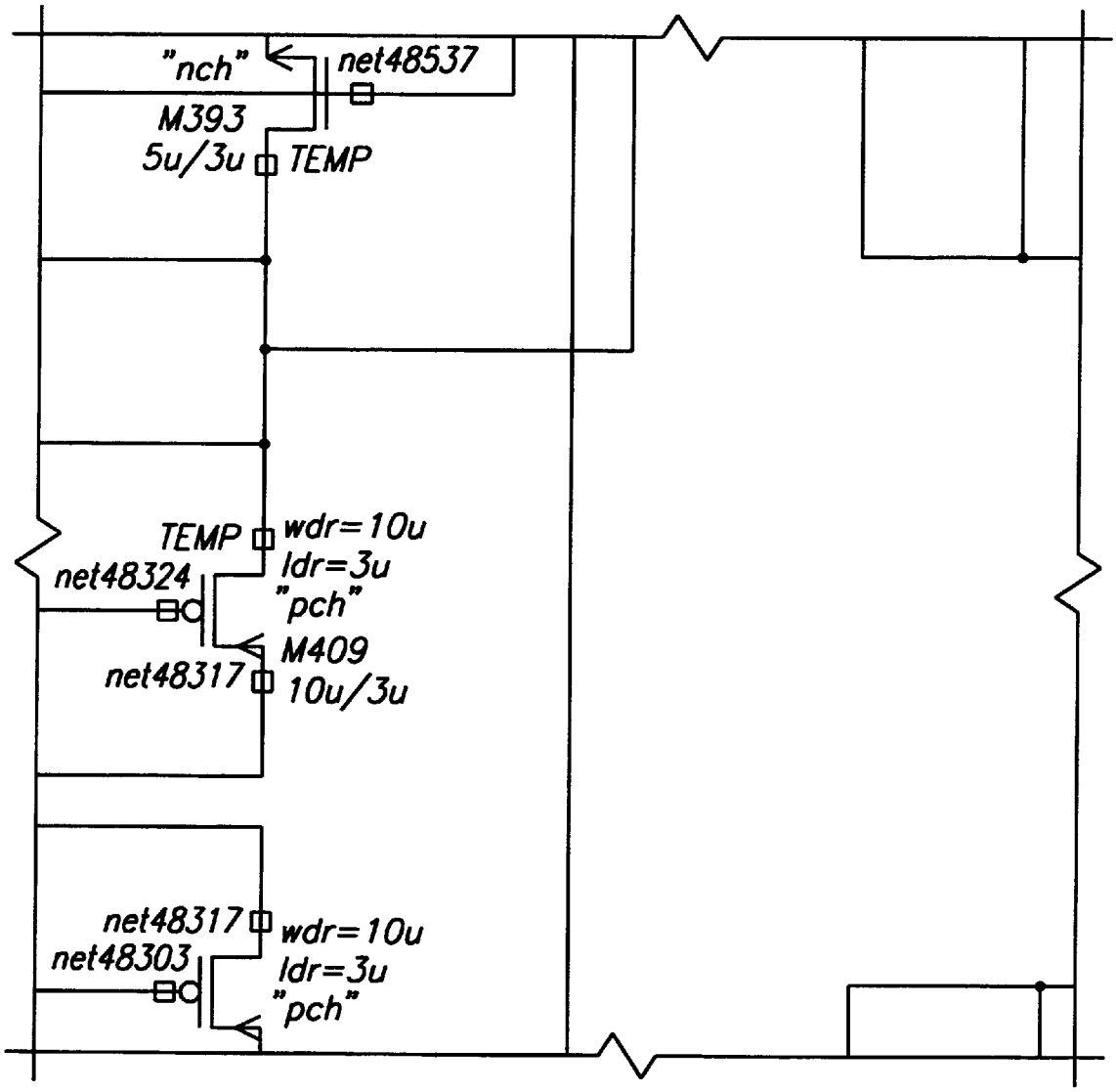

"nch"
net48537
M393
5u/3u
TEMP
TEMP
wdr=10u
ldr=3u
"pch"
net48324
M409
net48317
10u/3u
net48317
wdr=10u
net48303
ldr=3u
"pch"

Fig 1606

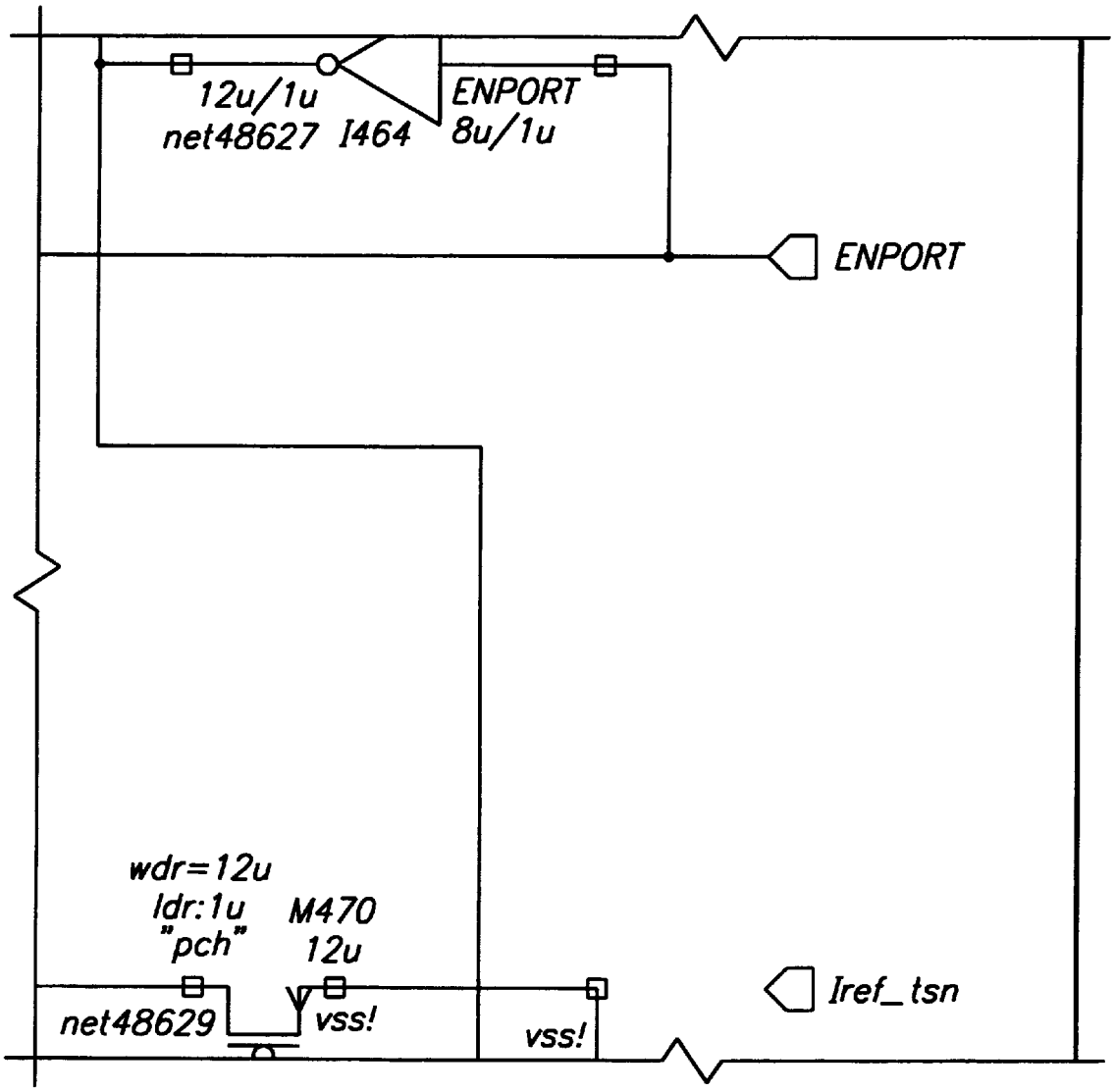

12u/1u
net48627
I464
ENPORT
8u/1u
ENPORT
wdr=12u
ldr:1u
"pch"
M470
12u
net48629
vss!
vss!
Iref_tsn

Fig 160H

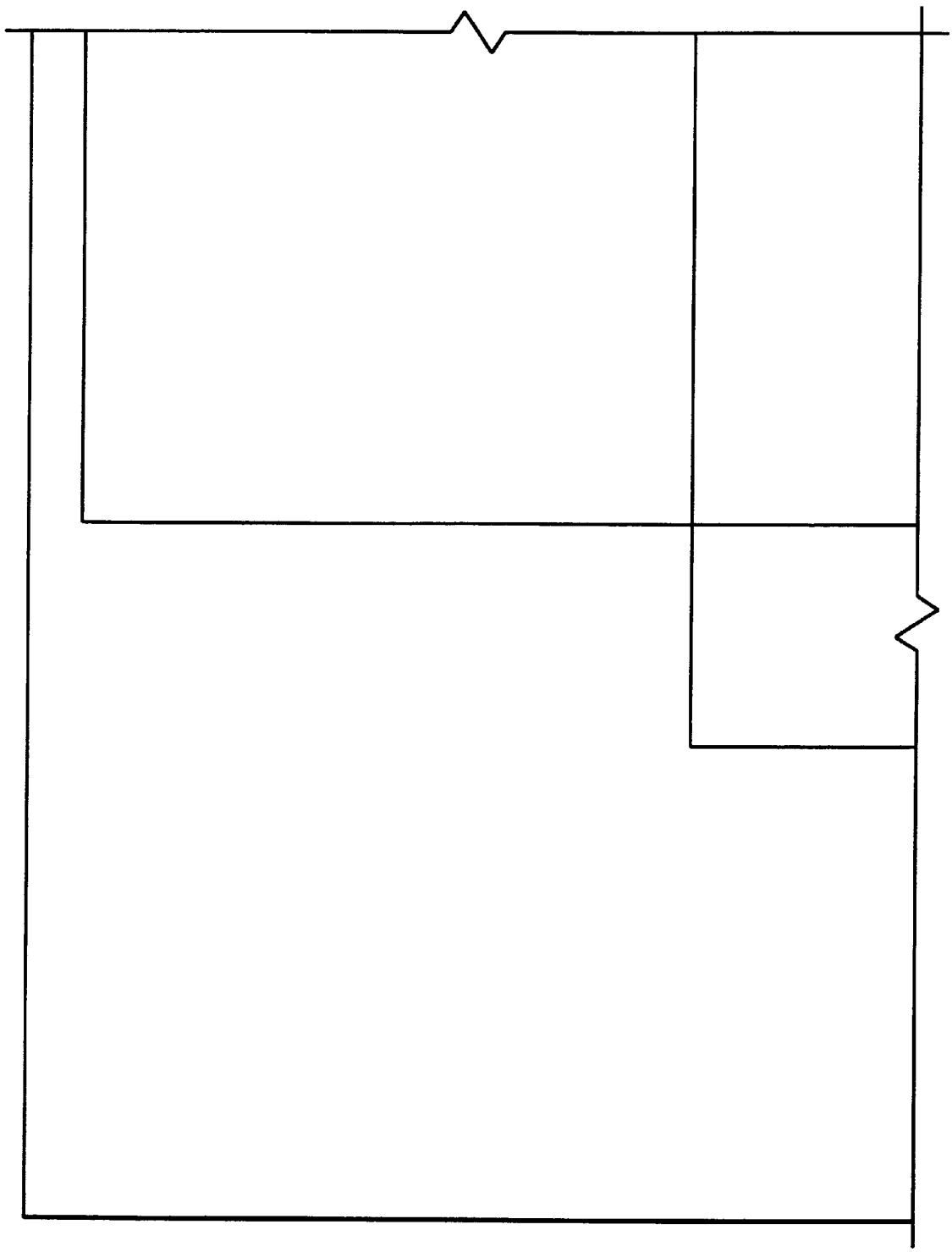


Fig 16EA

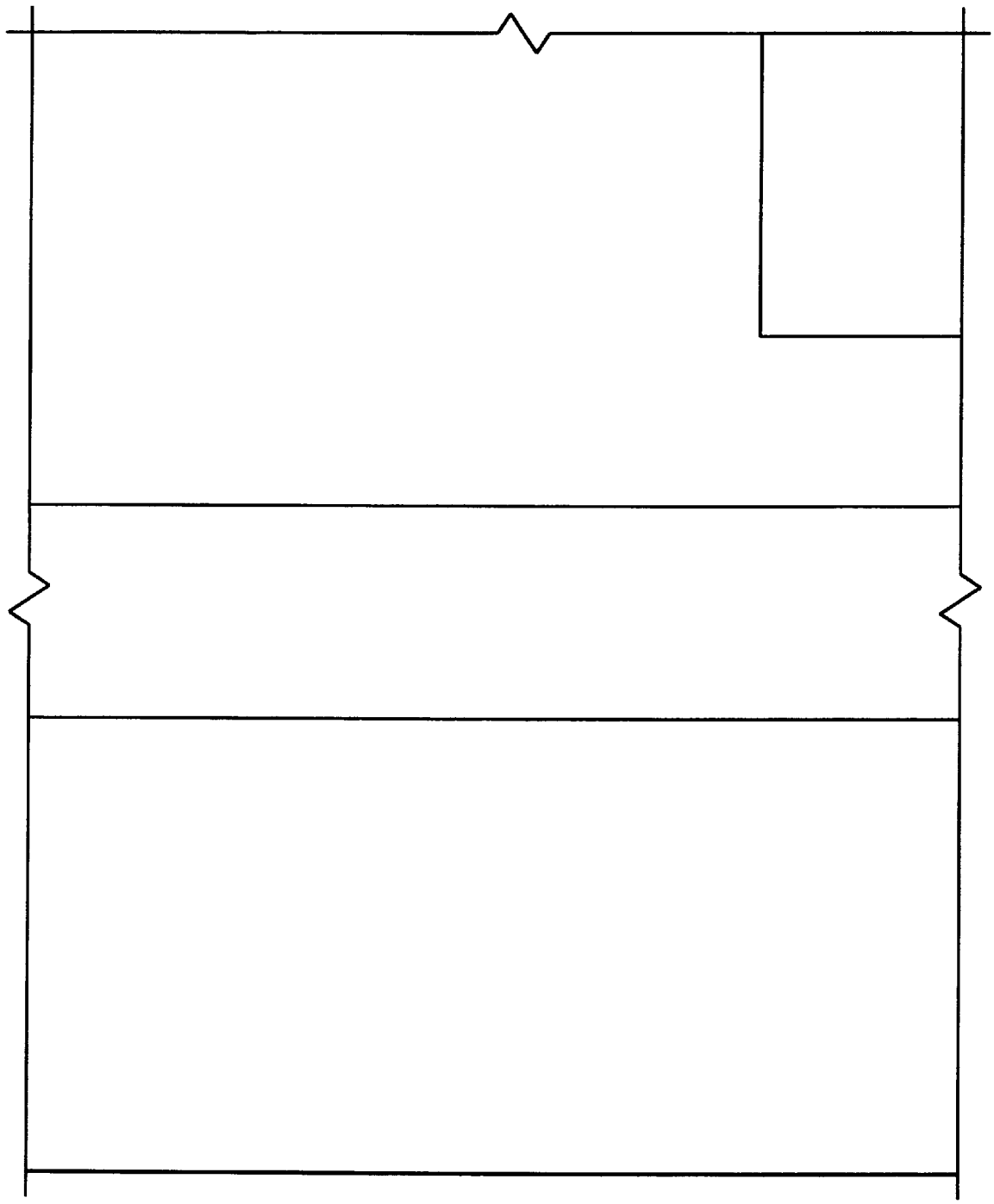


Fig 16EB

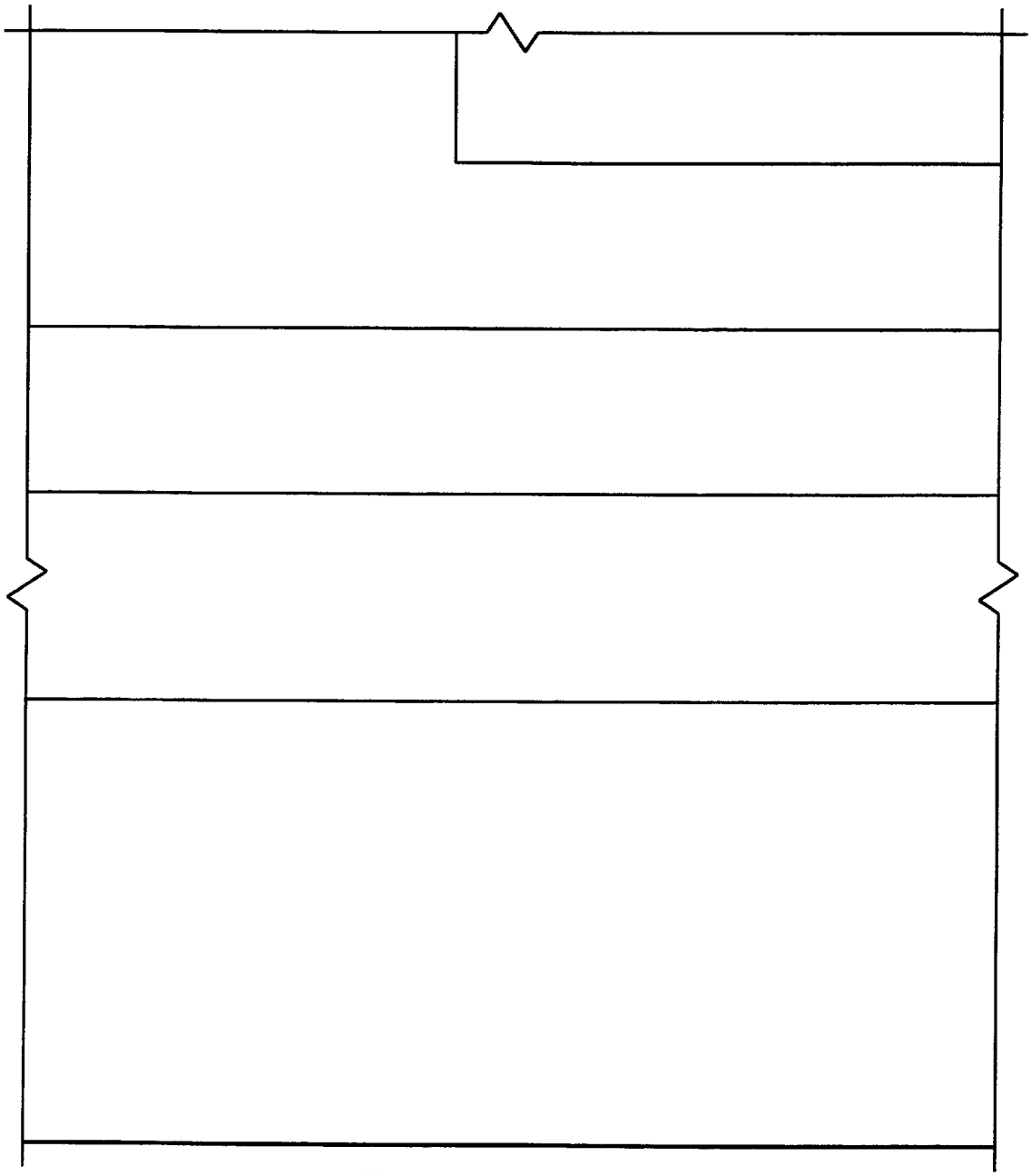


Fig 16EC

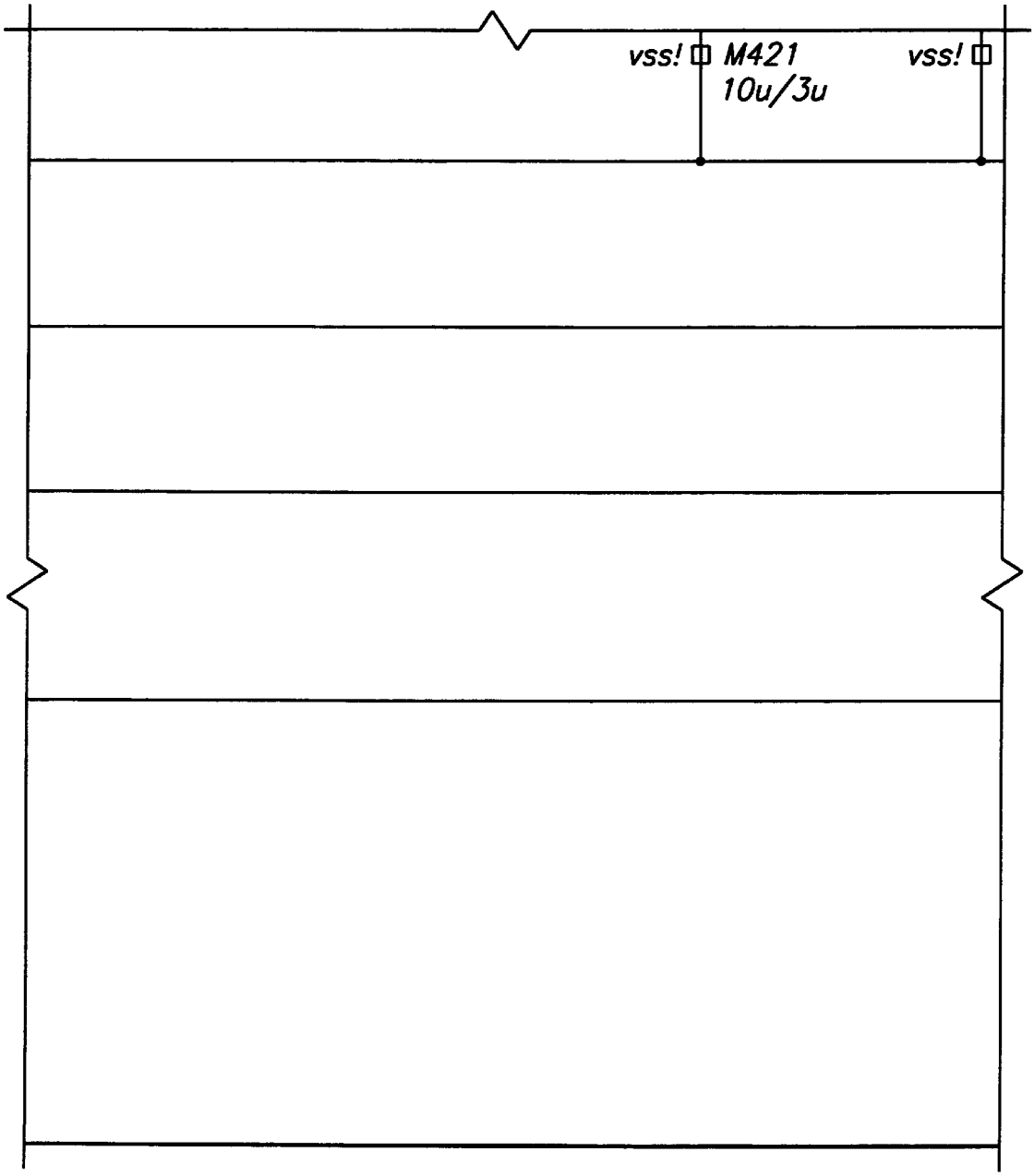


Fig 16ED

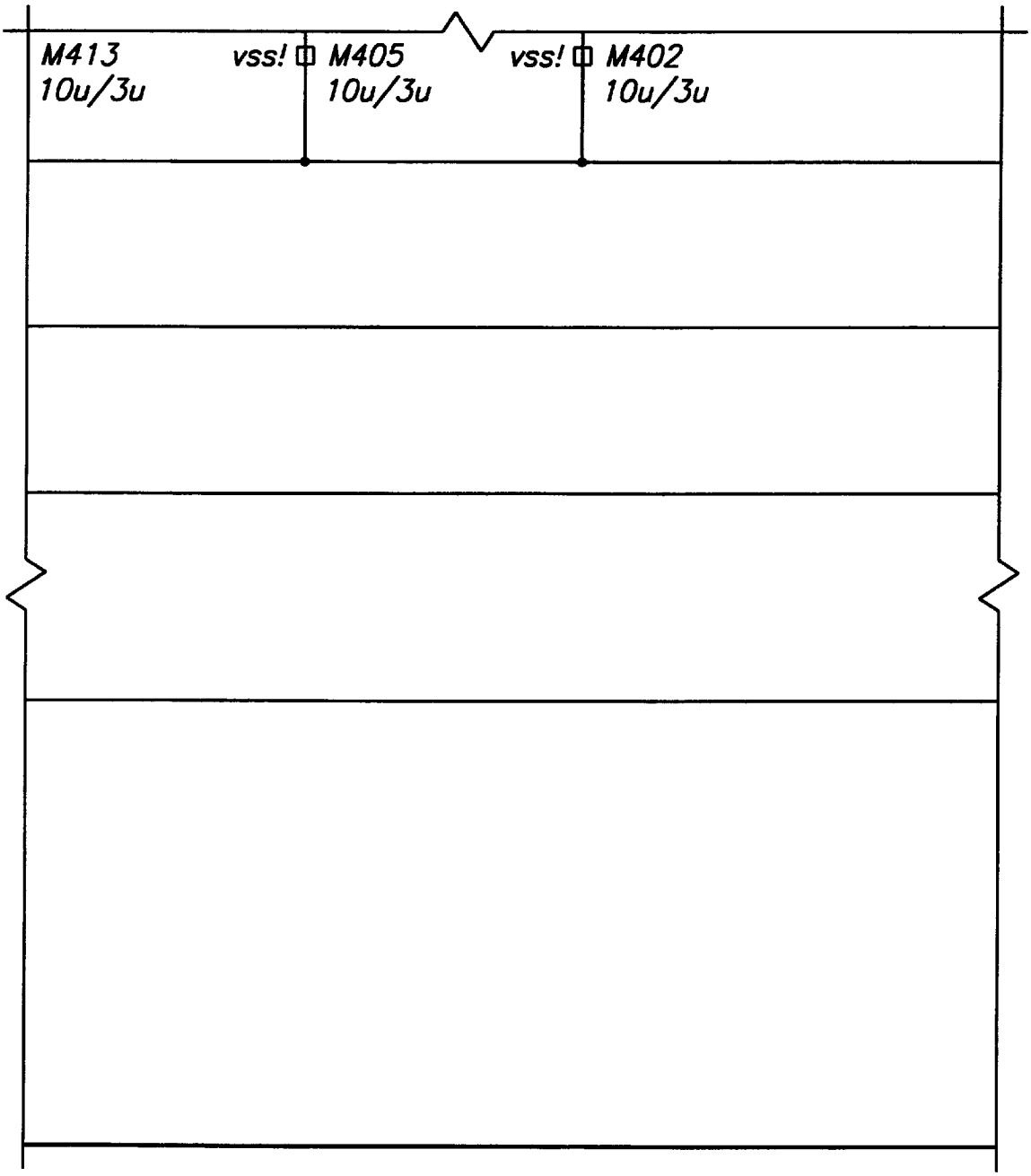


Fig 16EE

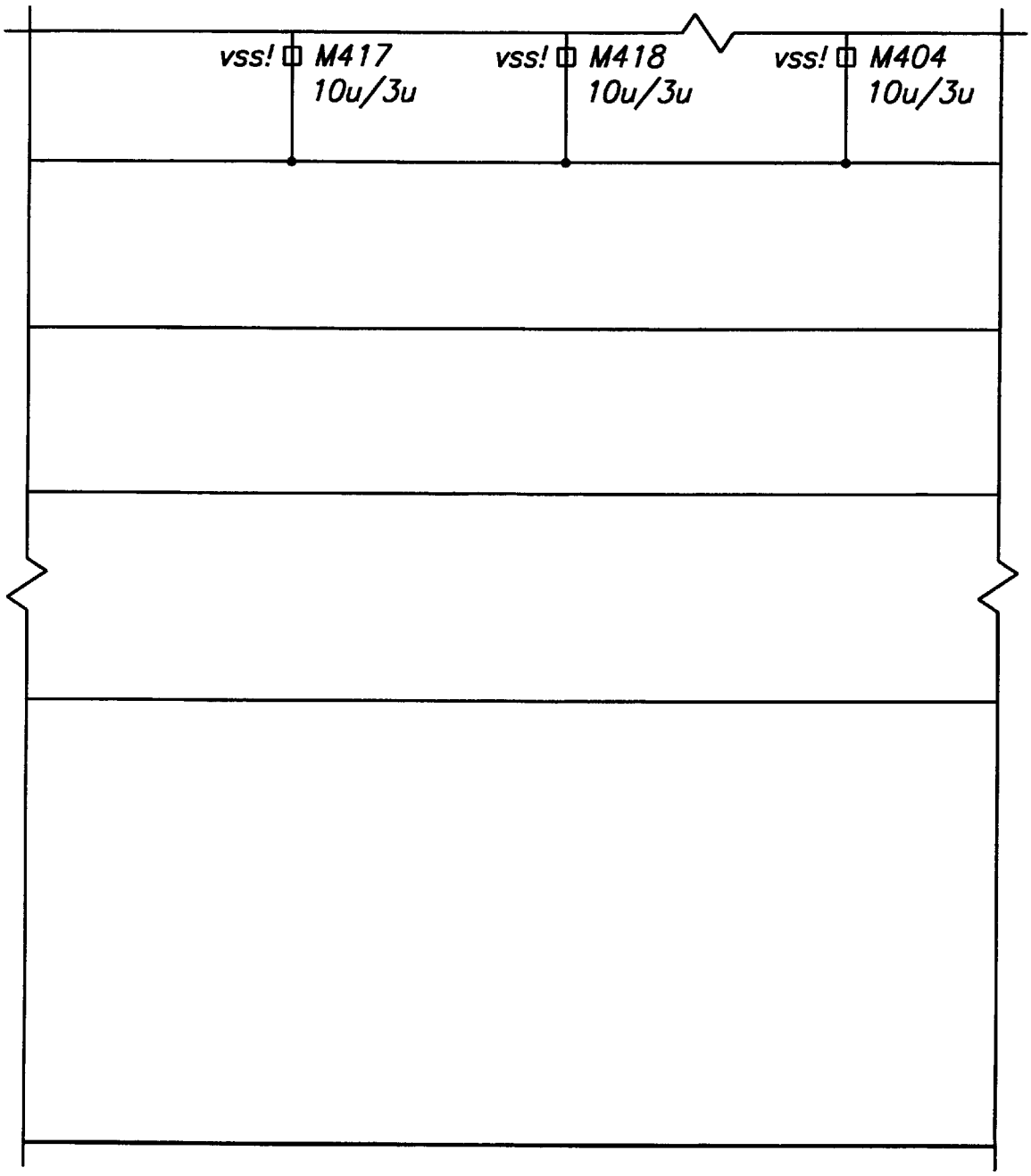


Fig 16EF

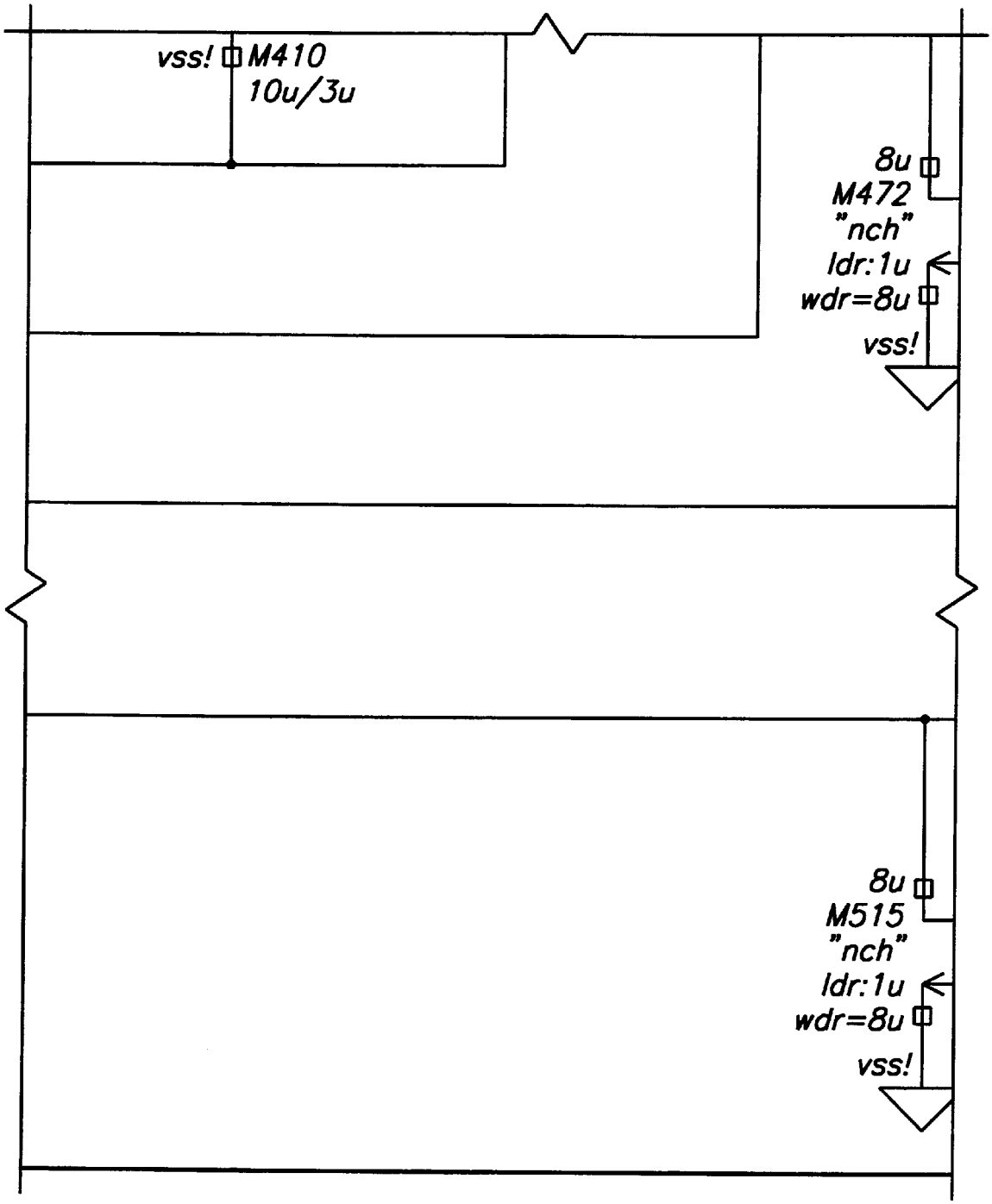

vss!
M410
10u/3u
8u
M472
"nch"
ldr:1u
wdr=8u
vss!
8u
M515
"nch"
ldr:1u
wdr=8u
vss!

Fig 1666

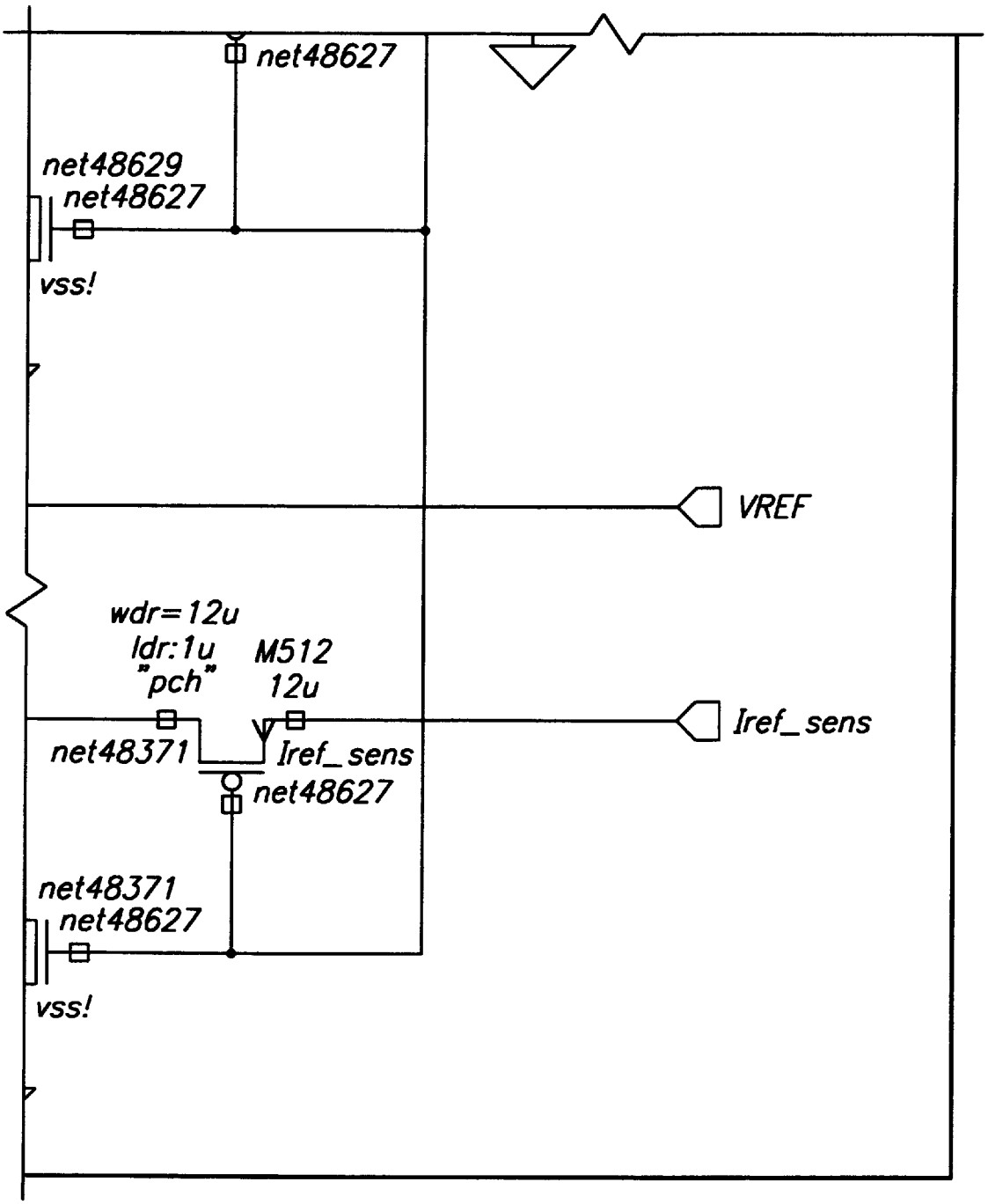

net48627
net48629
net48627
vss!
VREF
wdr=12u
ldr:1u
"pch"
M512
12u
Iref_sens
net48371
Iref_sens
net48627
net48371
net48627
vss!

Fig 16EH

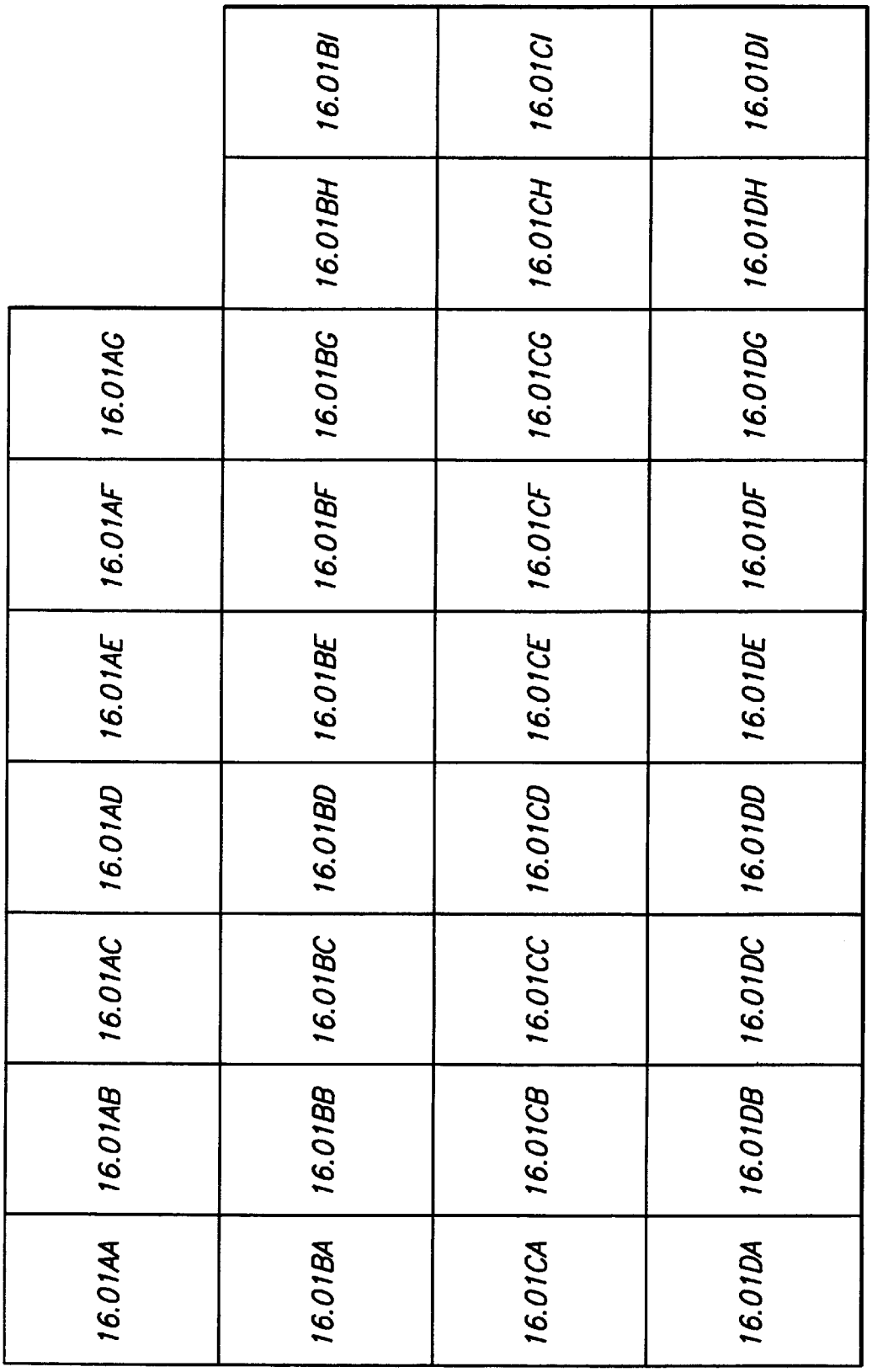

16.01AA
16.01AB
16.01AC
16.01AD
16.01AE
16.01AF
16.01AG
16.01BA
16.01BB
16.01BC
16.01BD
16.01BE
16.01BF
16.01BG
16.01BH
16.01BI
16.01CA
16.01CB
16.01CC
16.01CD
16.01CE
16.01CF
16.01CG
16.01CH
16.01CI
16.01DA
16.01DB
16.01DC
16.01DD
16.01DE
16.01DF
16.01DG
16.01DH
16.01DI

FIG. 16.01

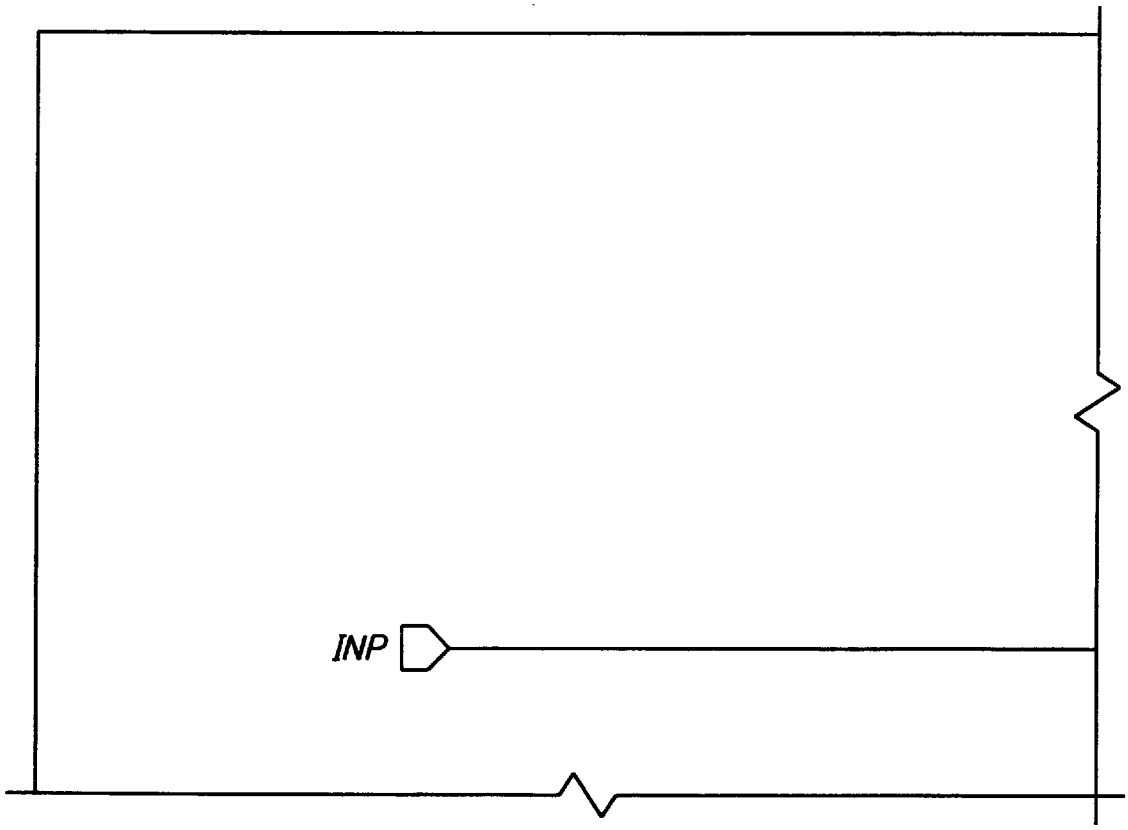


Fig 16.01AA

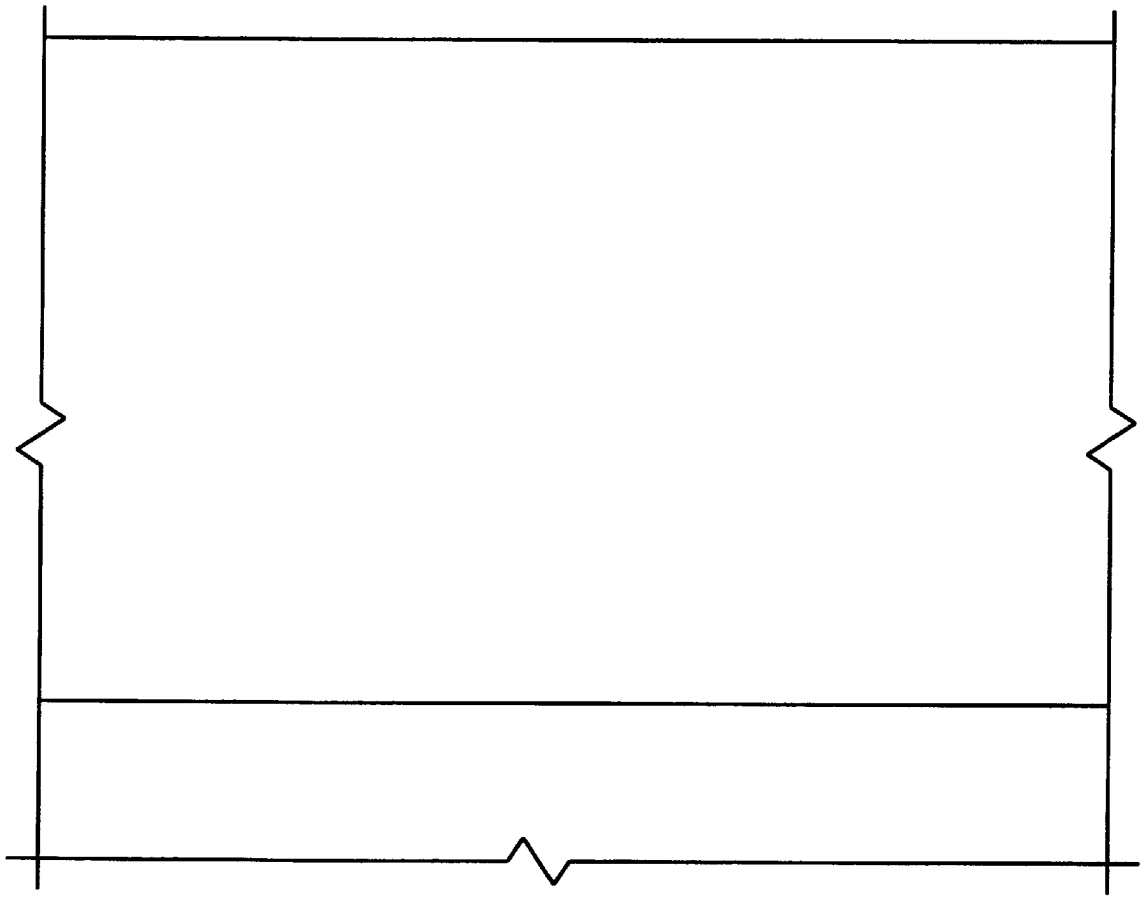


Fig 16.011AB

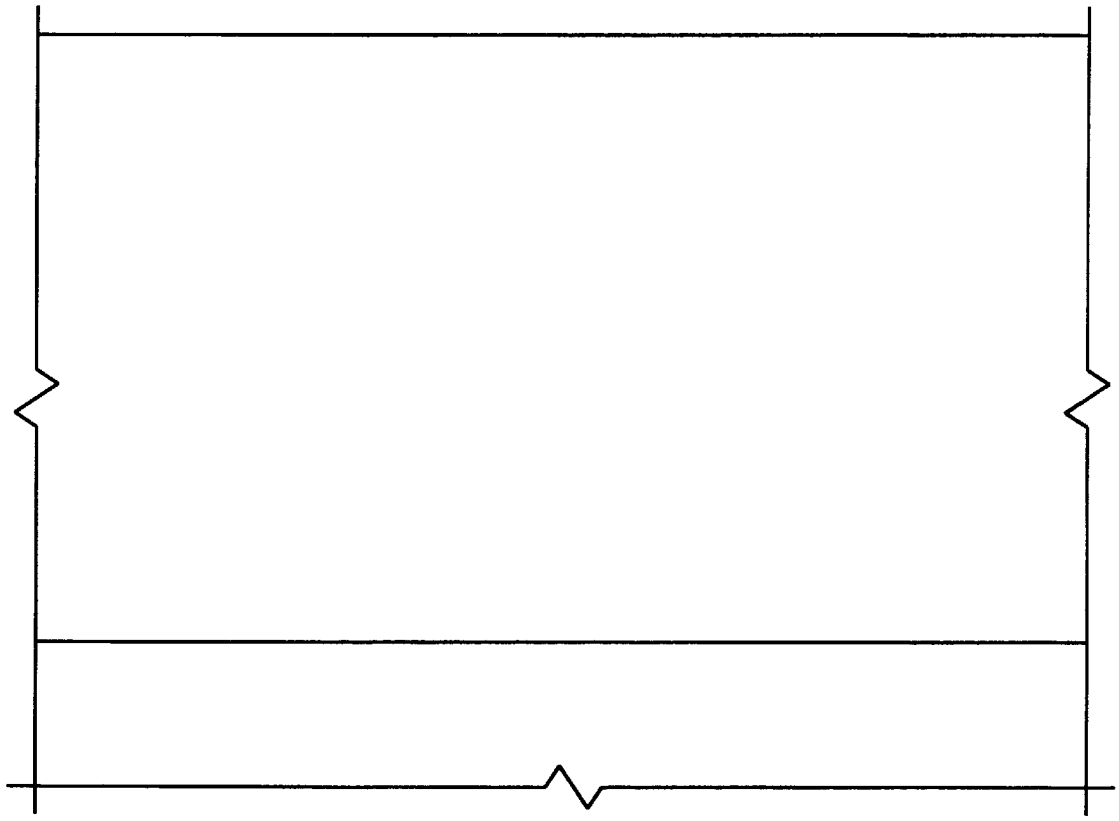


Fig 16.01AC

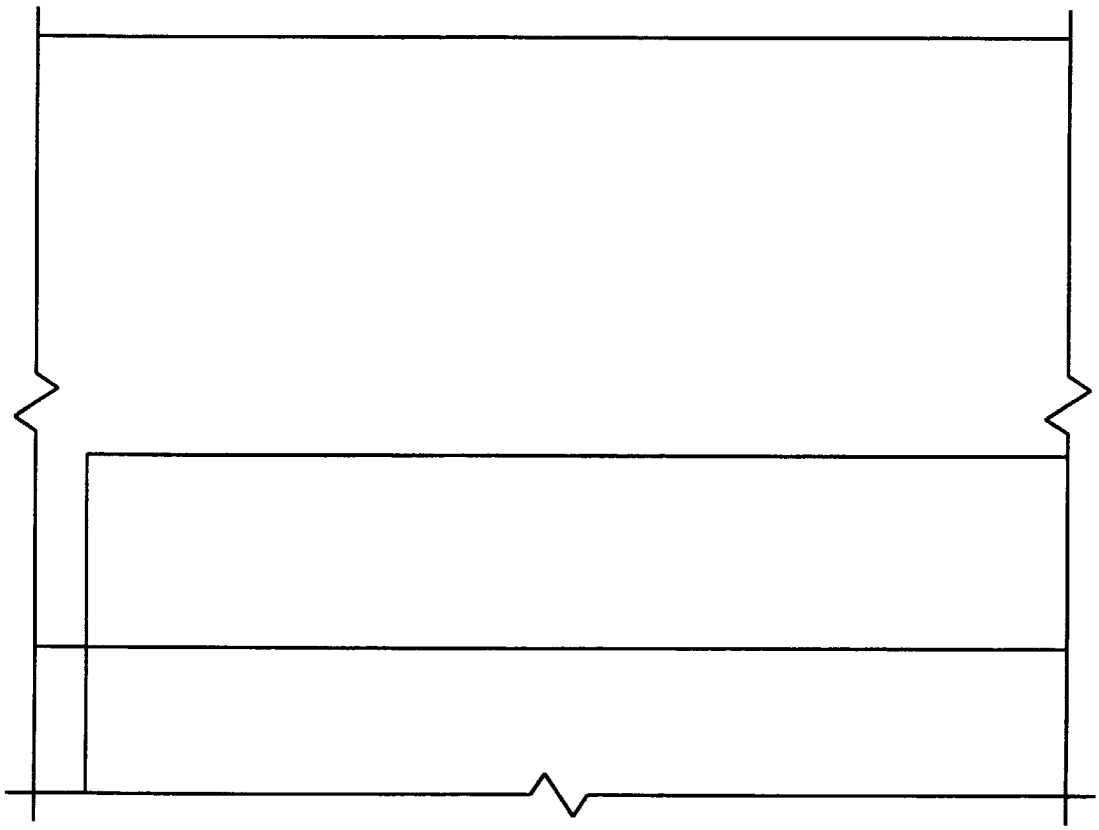


Fig 16.01AD

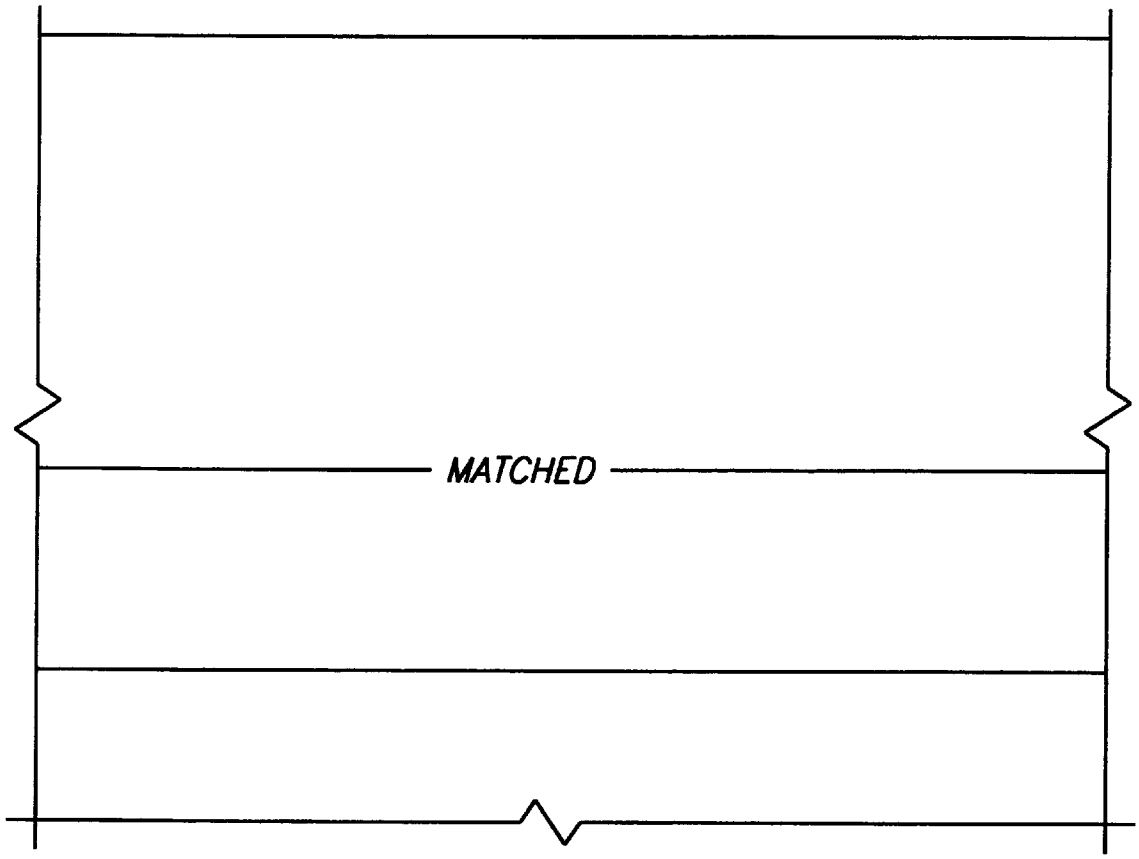


Fig 16.01AE

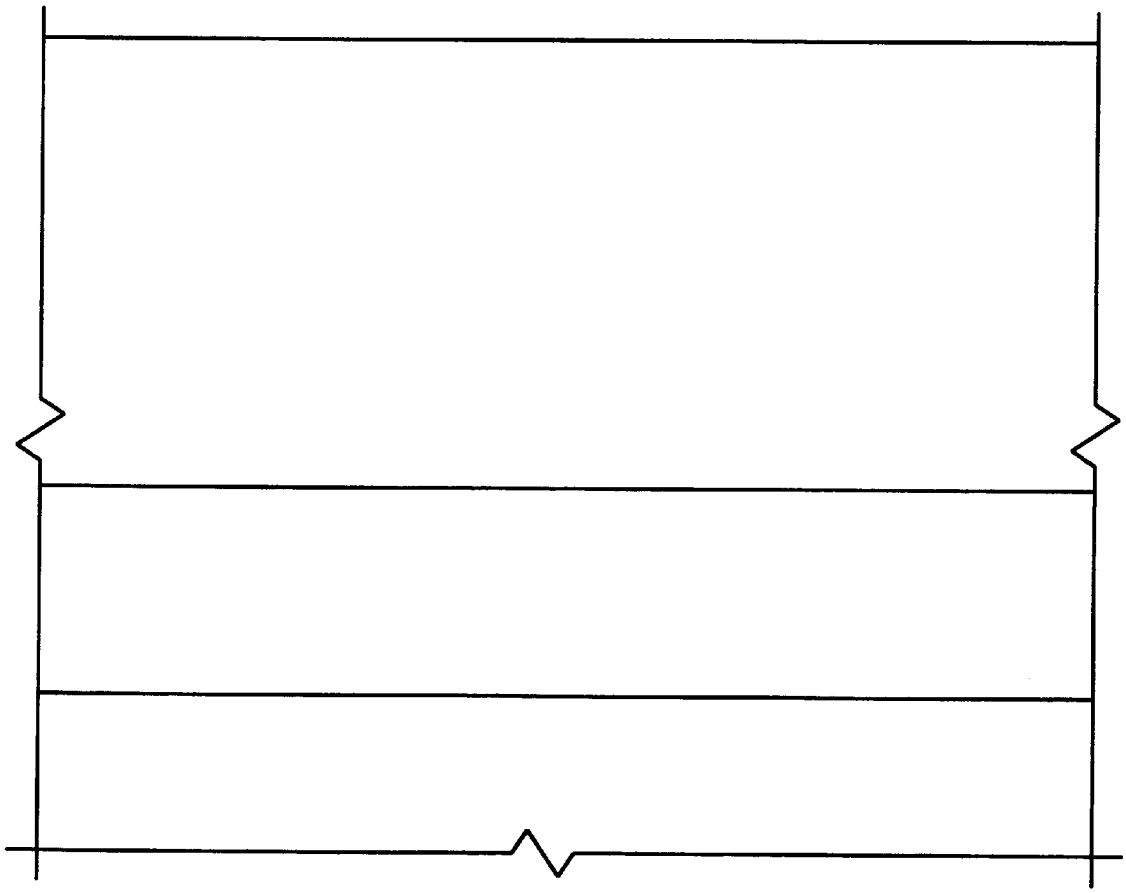


Fig 16.01AF

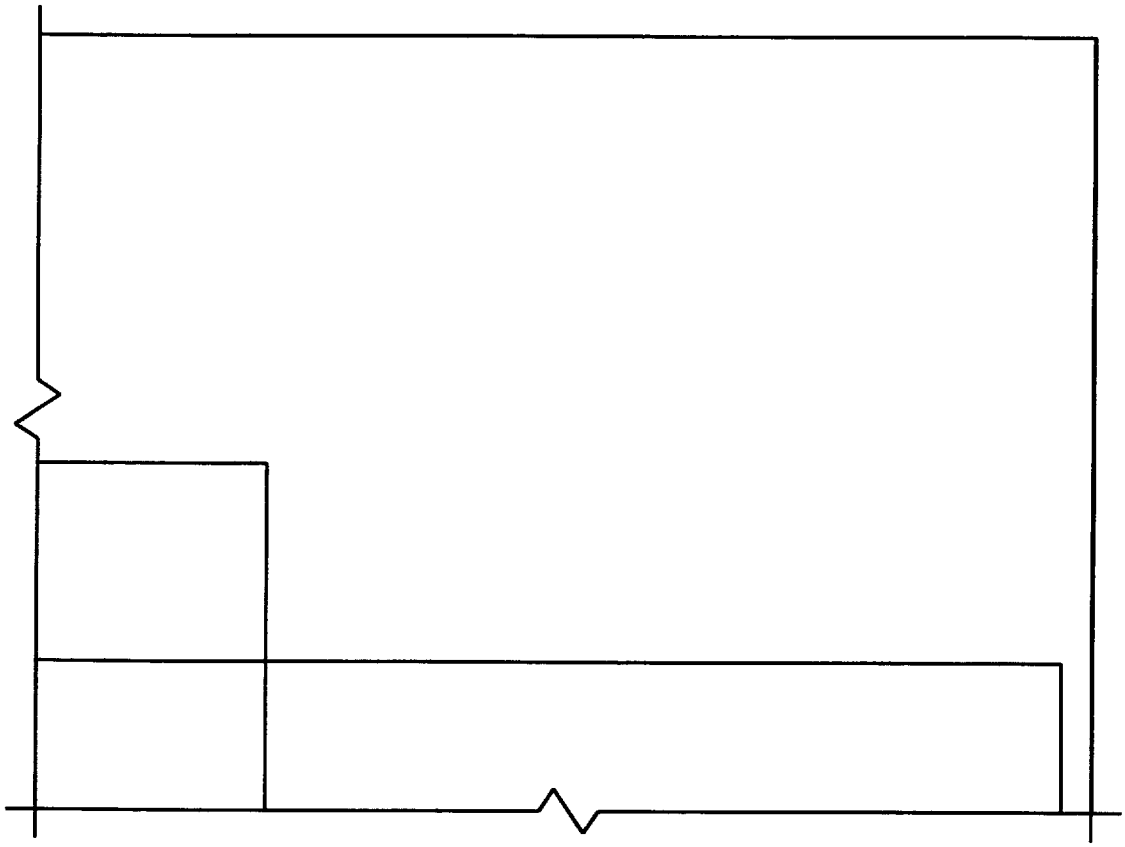


Fig 16.01A06

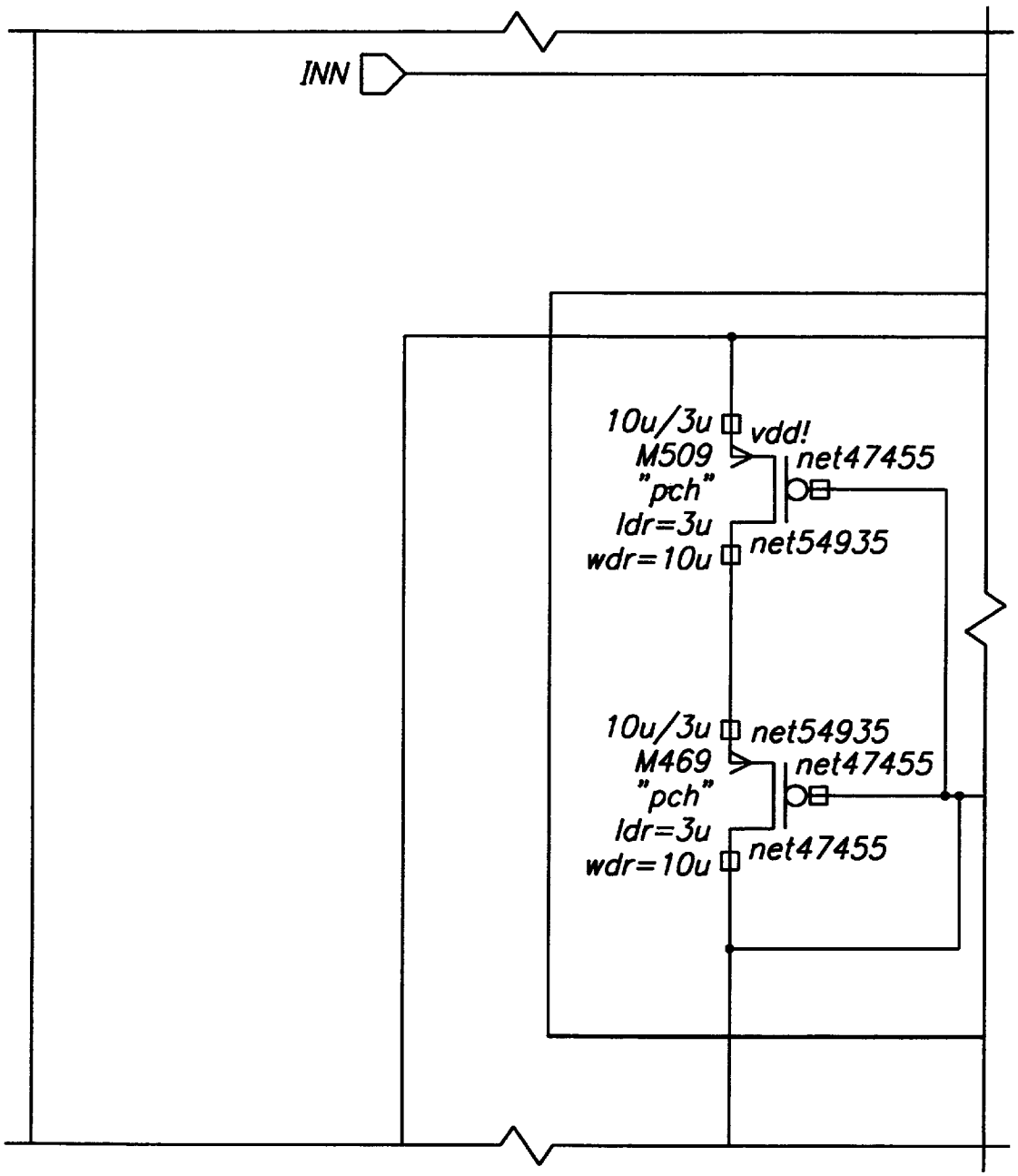

INN
10u/3u
M509
"pch"
ldr=3u
wdr=10u
vdd!
net47455
net54935
10u/3u
M469
"pch"
ldr=3u
wdr=10u
net54935
net47455
net47455

Fig 16.01BA

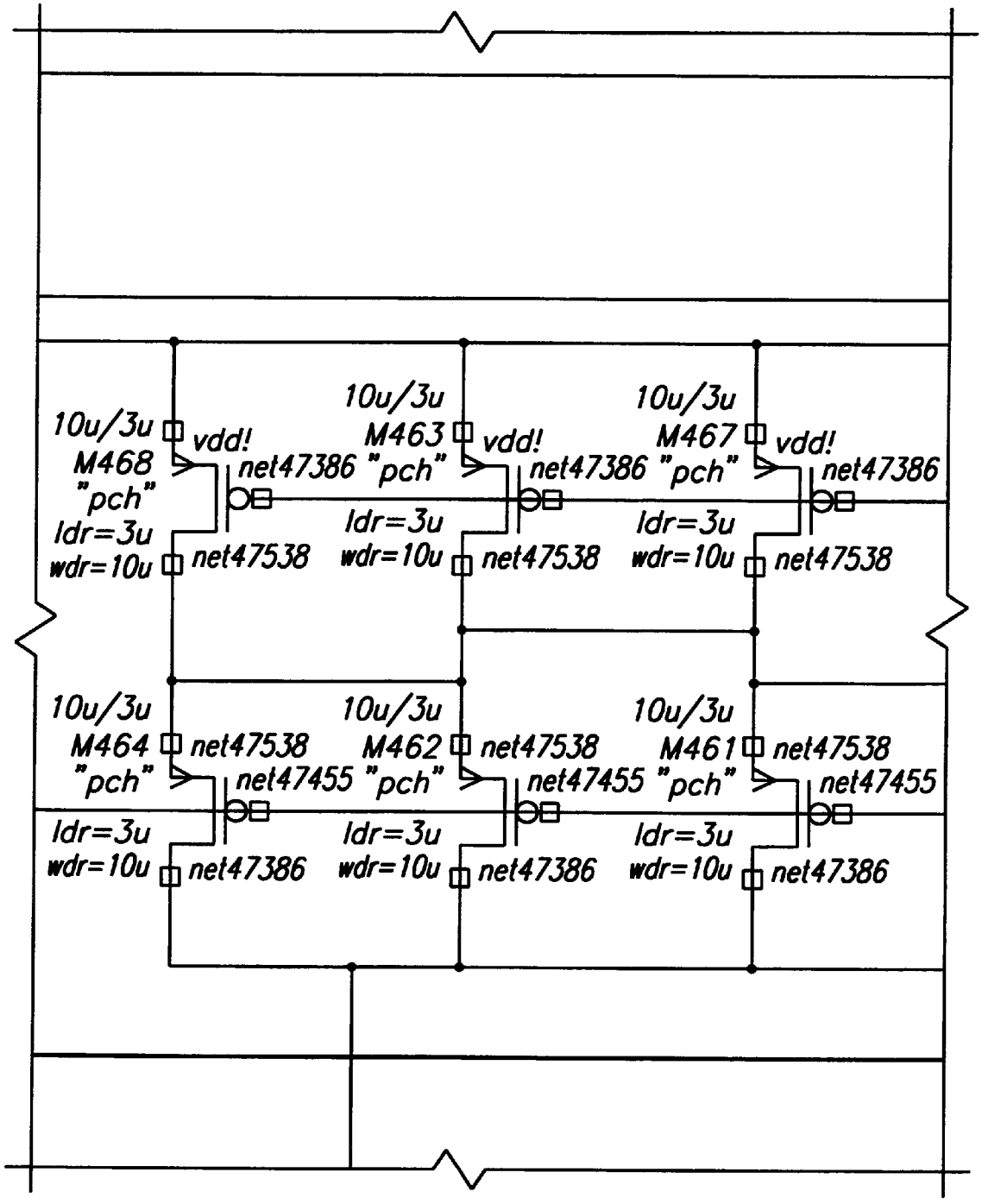

10u/3u
M468
"pch"
ldr=3u
wdr=10u
vdd!
net47386
net47538
10u/3u
M463
"pch"
ldr=3u
wdr=10u
vdd!
net47386
net47538
10u/3u
M467
"pch"
ldr=3u
wdr=10u
vdd!
net47386
net47538
10u/3u
M464
"pch"
ldr=3u
wdr=10u
net47538
net47455
net47386
10u/3u
M462
"pch"
ldr=3u
wdr=10u
net47538
net47455
net47386
10u/3u
M461
"pch"
ldr=3u
wdr=10u
net47538
net47455
net47386

Fig 16.01BB

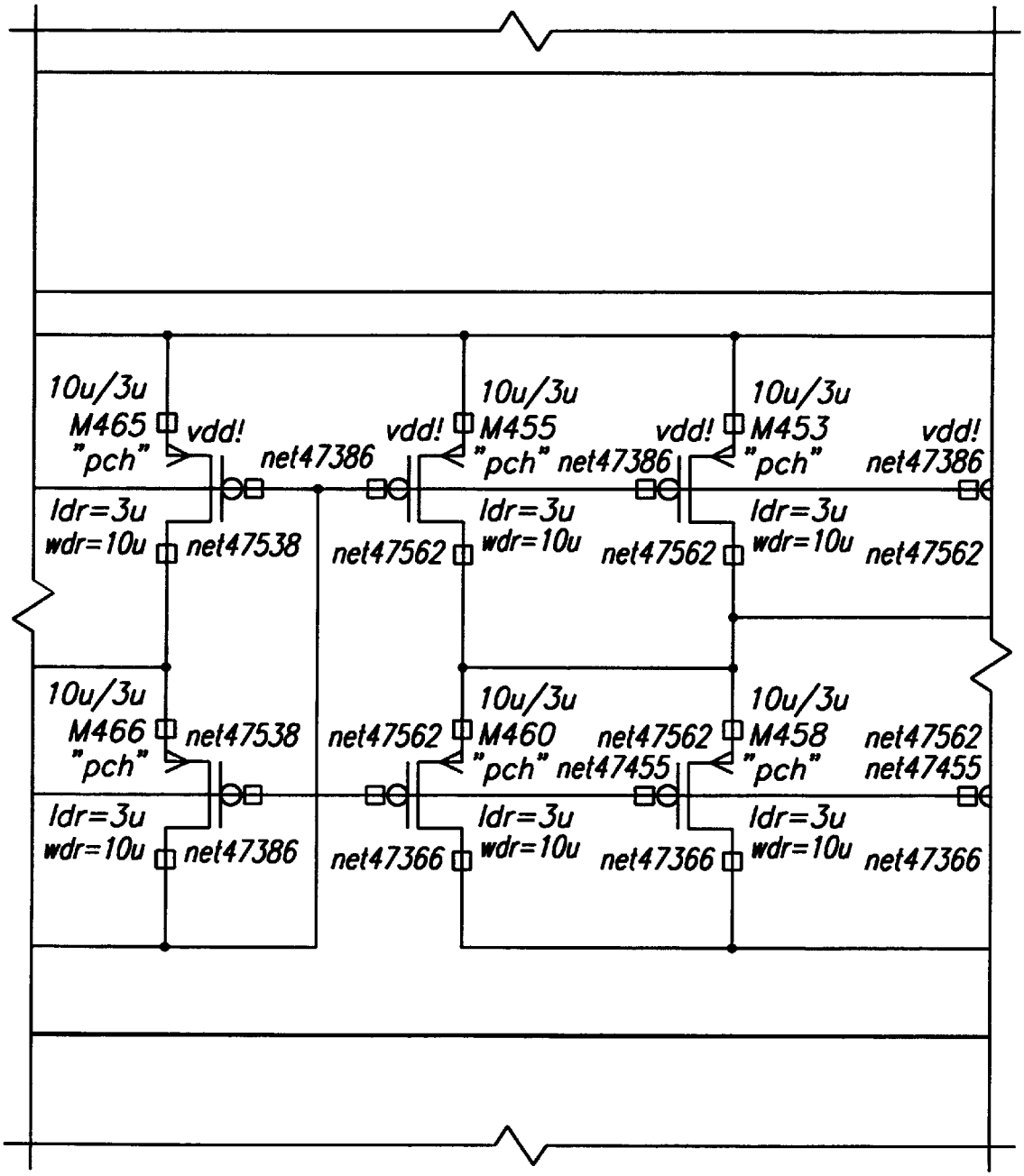

10u/3u
M465
"pch"
vdd!
net47386
ldr=3u
wdr=10u
net47538
10u/3u
M455
"pch"
vdd!
net47386
net47562
ldr=3u
wdr=10u
net47562
10u/3u
M453
"pch"
vdd!
net47386
ldr=3u
wdr=10u
net47562
10u/3u
M466
"pch"
net47538
ldr=3u
wdr=10u
net47386
10u/3u
M460
"pch"
net47562
net47455
ldr=3u
wdr=10u
net47366
10u/3u
M458
"pch"
net47562
net47455
ldr=3u
wdr=10u
net47366

Fig 16.01BC

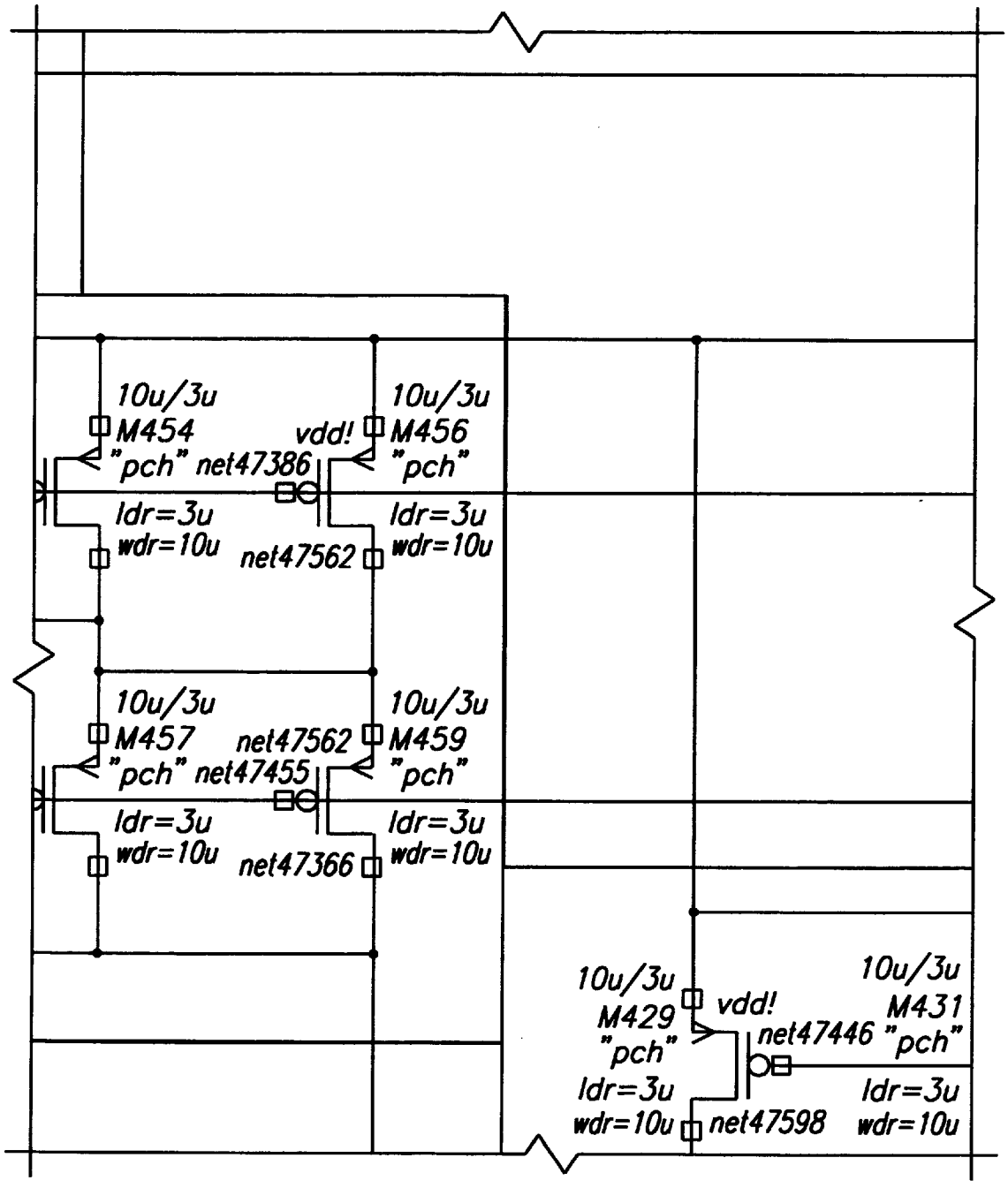

10u/3u
M454
"pch"
net47386
vdd!
10u/3u
M456
"pch"
ldr=3u
wdr=10u
net47562
ldr=3u
wdr=10u
10u/3u
M457
"pch"
net47562
net47455
10u/3u
M459
"pch"
ldr=3u
wdr=10u
net47366
ldr=3u
wdr=10u
10u/3u
M429
"pch"
vdd!
10u/3u
M431
"pch"
net47446
ldr=3u
wdr=10u
net47598
ldr=3u
wdr=10u

Fig 16.01BD

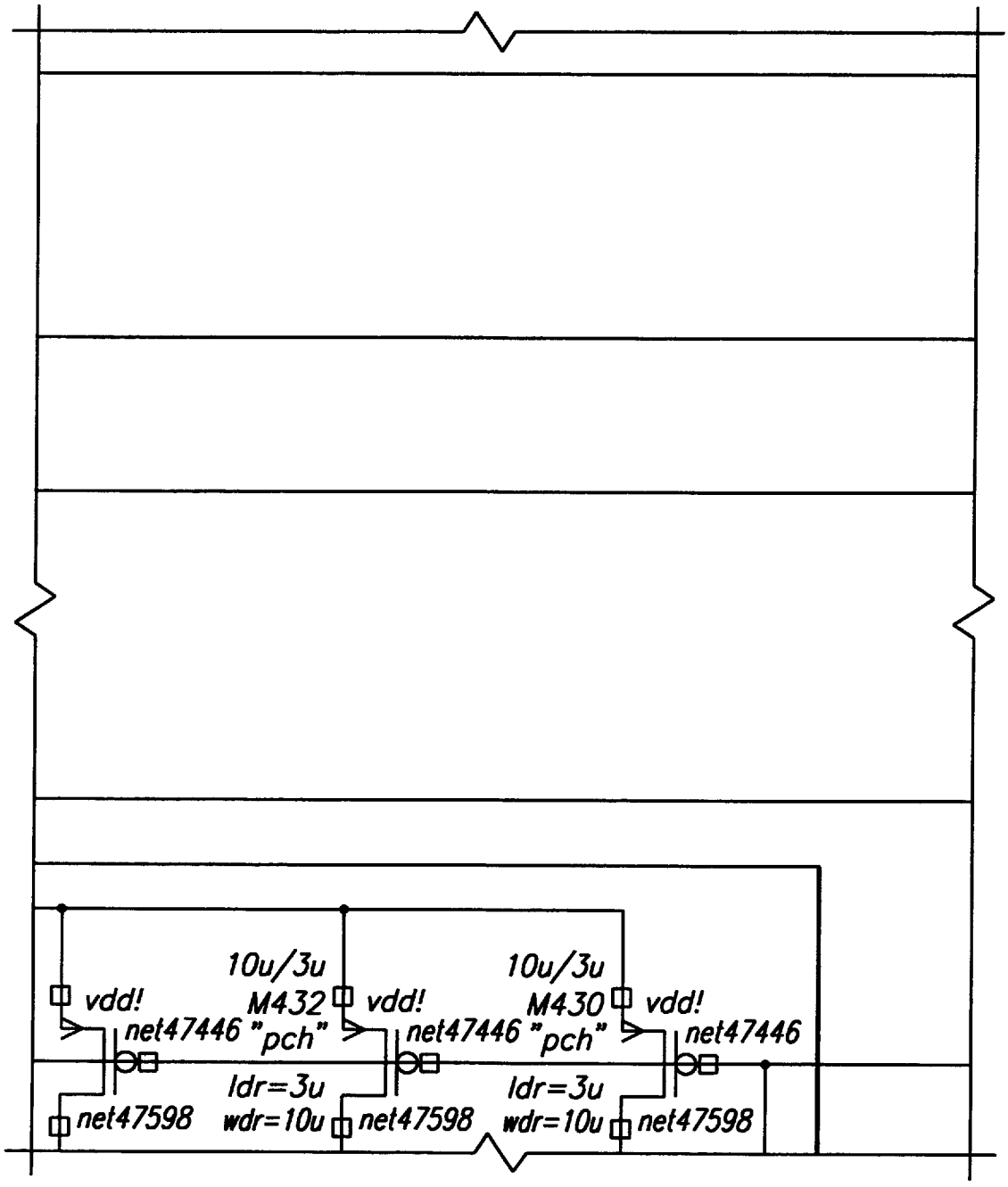


Fig 16.00188E

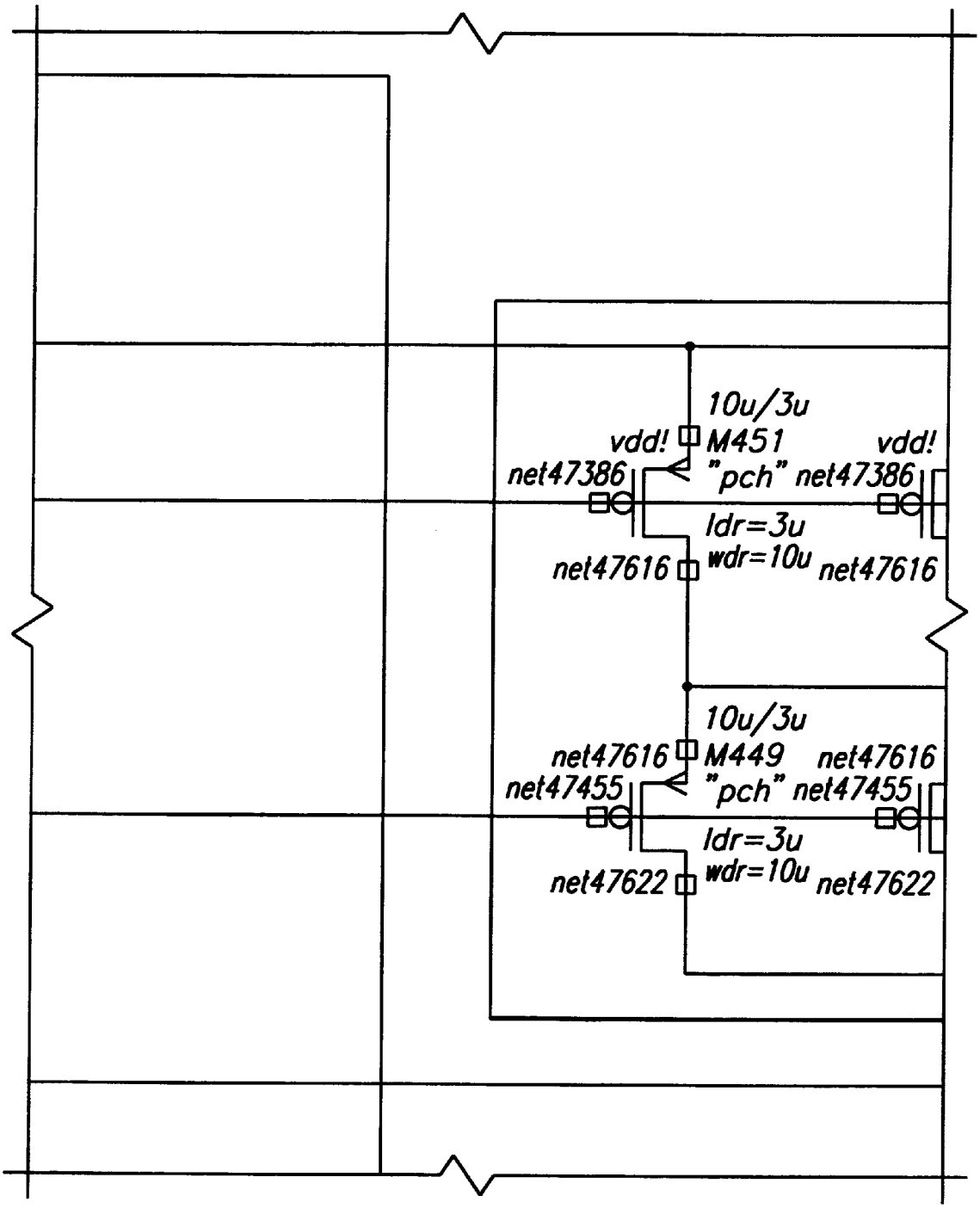

10u/3u
vdd!
M451
"pch"
vdd!
net47386
net47386
ldr=3u
wdr=10u
net47616
net47616
10u/3u
net47616
M449
"pch"
net47616
net47455
net47455
ldr=3u
wdr=10u
net47622
net47622

Fig 16.011BF

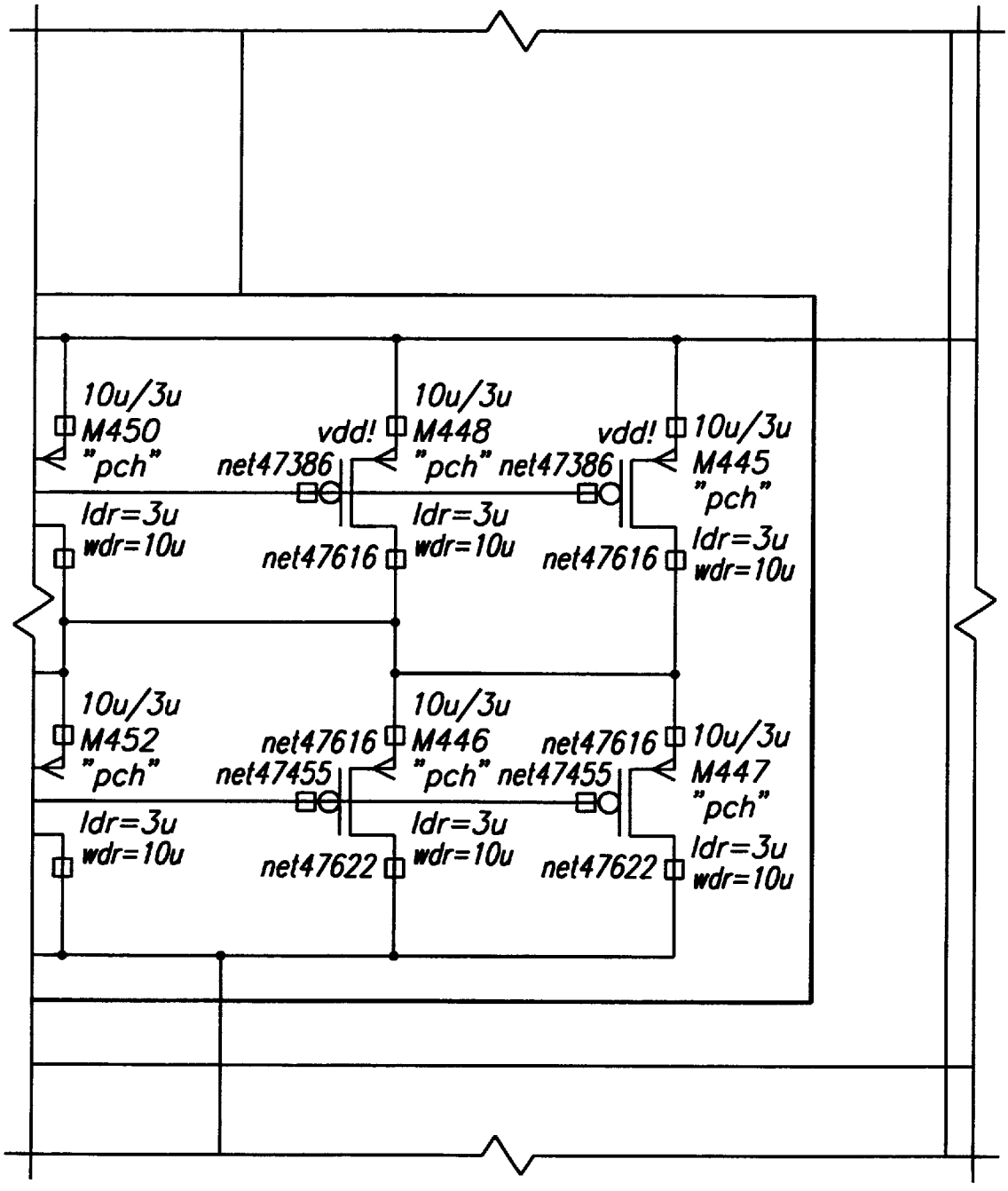

10u/3u
M450
"pch"
ldr=3u
wdr=10u
vdd!
10u/3u
M448
"pch"
net47386
ldr=3u
wdr=10u
net47616
vdd!
10u/3u
M445
"pch"
net47386
ldr=3u
wdr=10u
net47616
10u/3u
M452
"pch"
ldr=3u
wdr=10u
net47616
10u/3u
M446
"pch"
net47455
ldr=3u
wdr=10u
net47622
net47616
10u/3u
M447
"pch"
net47455
ldr=3u
wdr=10u
net47622

Fig 16.011B6

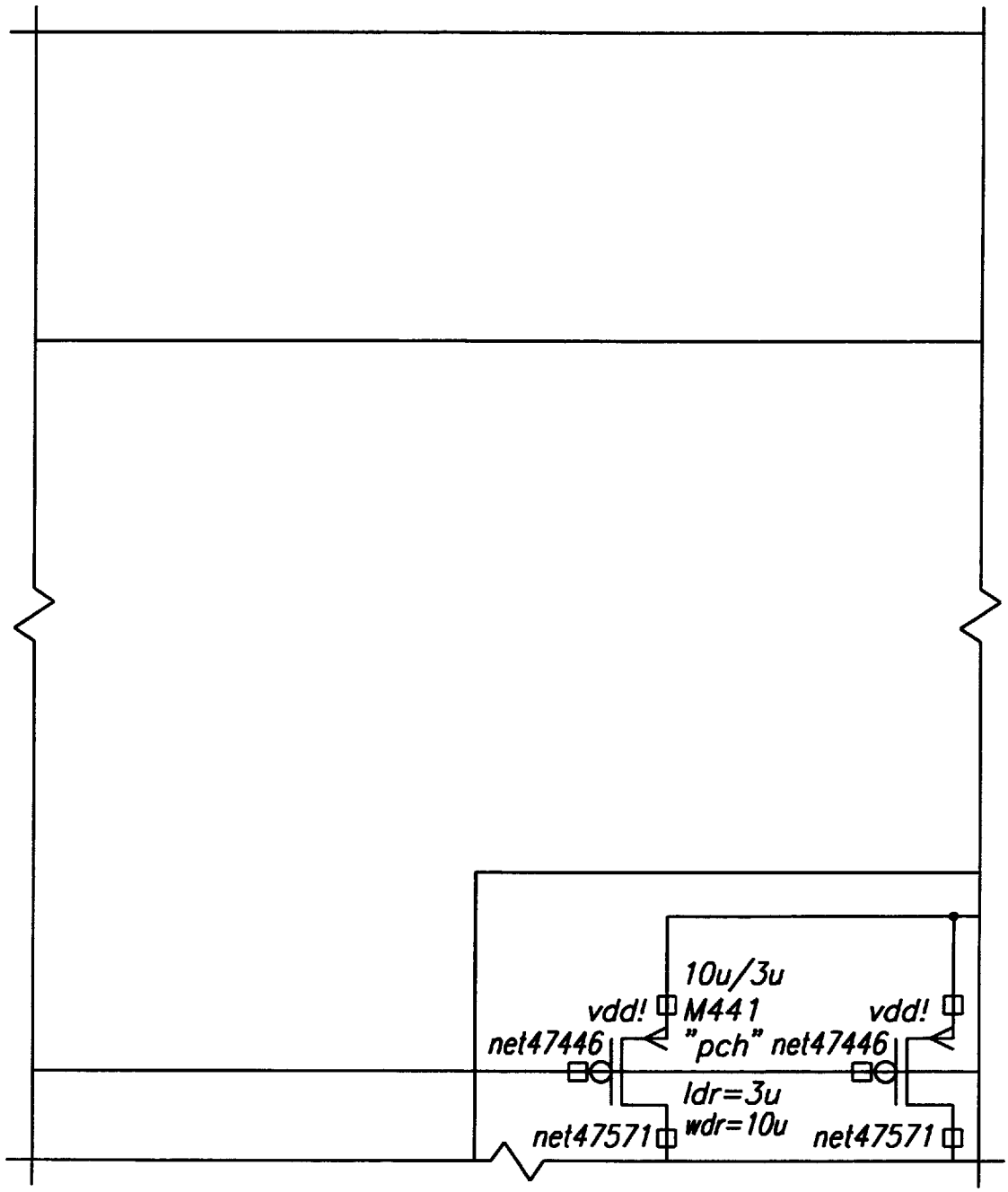

10u/3u
vdd!
M441
"pch"
vdd!
net47446
net47446
ldr=3u
wdr=10u
net47571
net47571

Fig 16.01BH

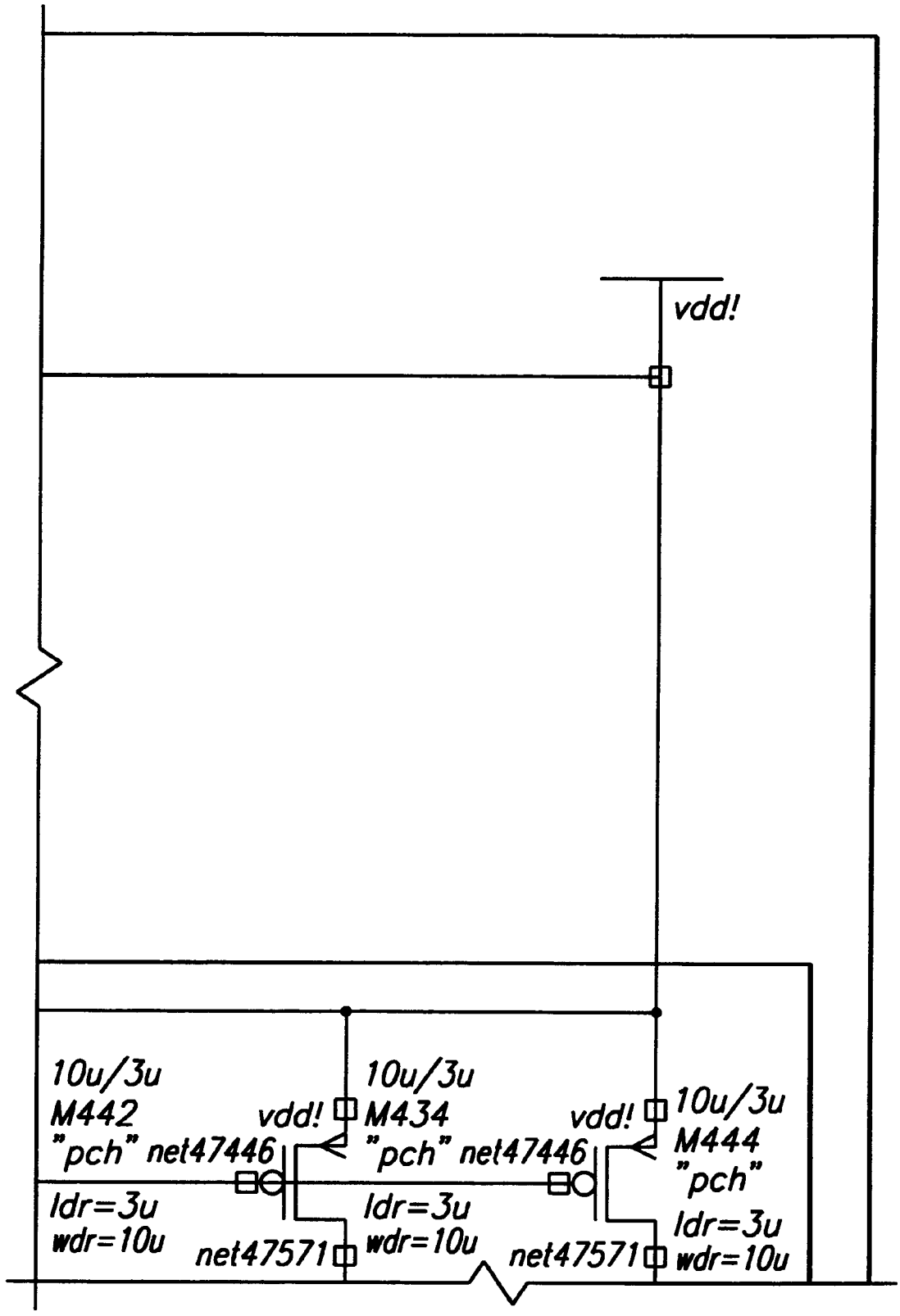

vdd!
10u/3u
M442
"pch"
net47446
ldr=3u
wdr=10u
net47571
vdd!
10u/3u
M434
"pch"
net47446
ldr=3u
wdr=10u
net47571
vdd!
10u/3u
M444
"pch"
ldr=3u
wdr=10u

Fig 16.01BII

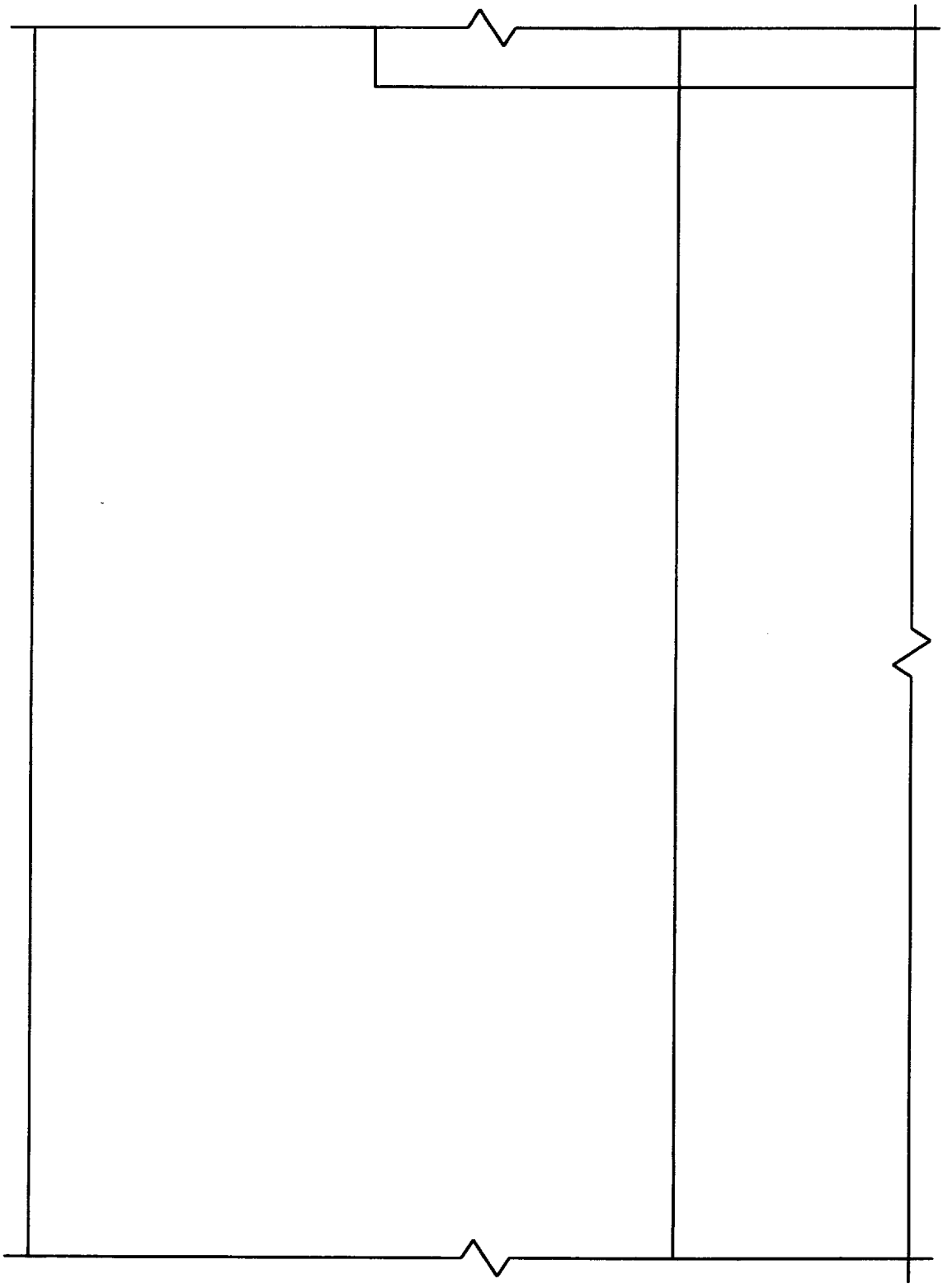


Fig 16.01CA

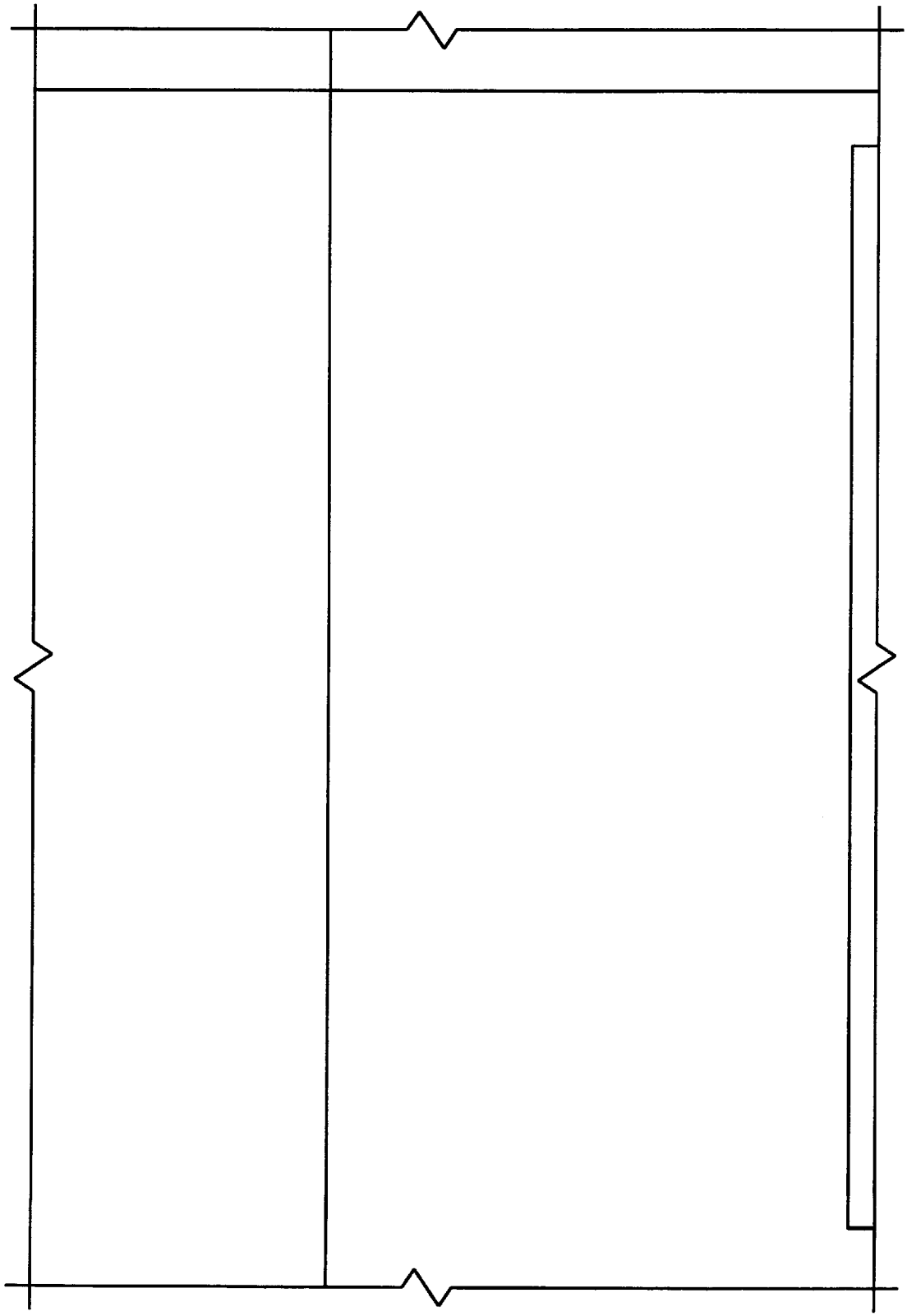


Fig 16.011CB

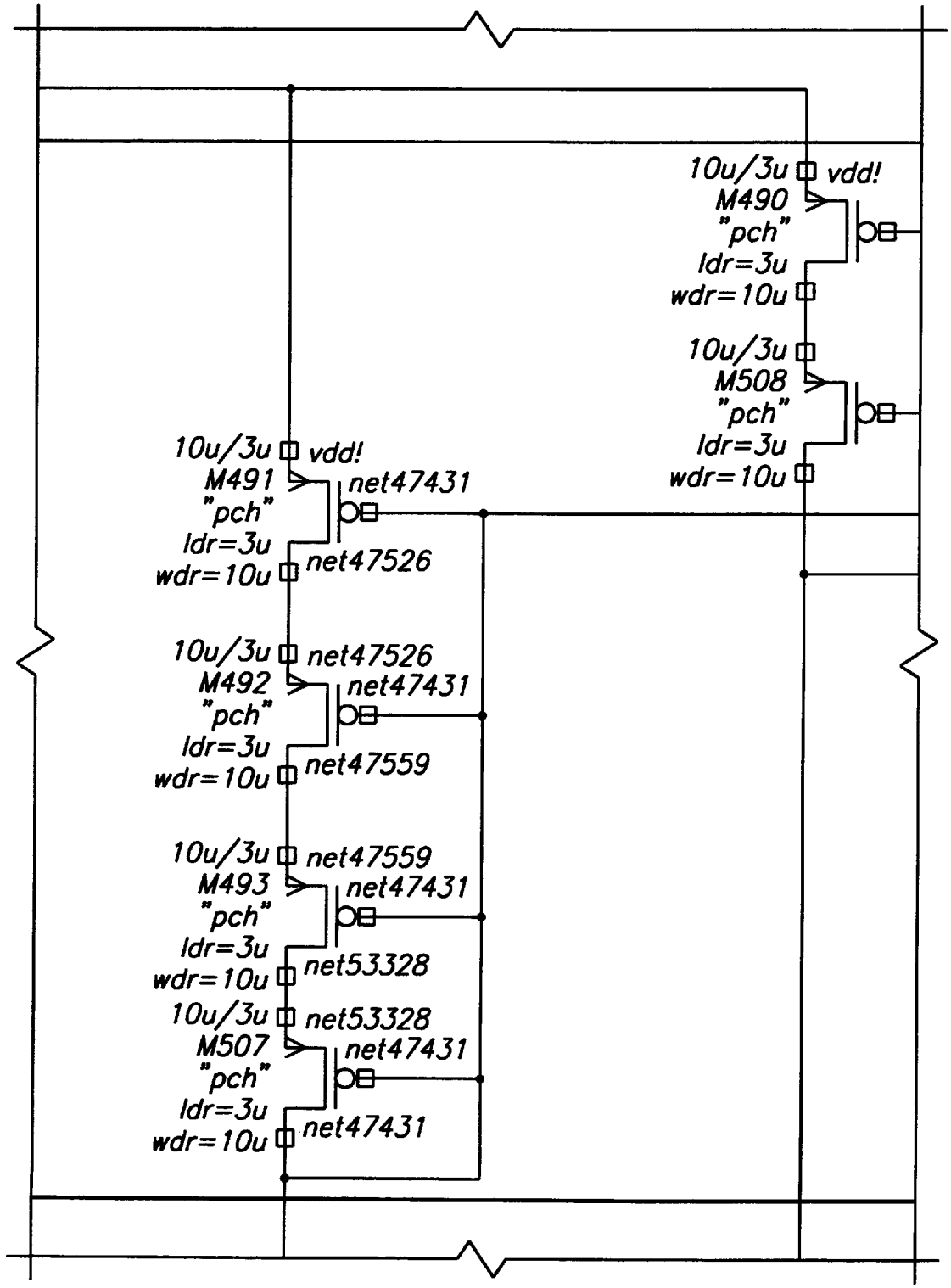

10u/3u
M490
"pch"
ldr=3u
wdr=10u
vdd!
10u/3u
M508
"pch"
ldr=3u
wdr=10u
10u/3u
M491
"pch"
ldr=3u
wdr=10u
vdd!
net47431
net47526
10u/3u
M492
"pch"
ldr=3u
wdr=10u
net47526
net47431
net47559
10u/3u
M493
"pch"
ldr=3u
wdr=10u
net47559
net47431
net53328
10u/3u
M507
"pch"
ldr=3u
wdr=10u
net53328
net47431
net47431

Fig 16.01CC

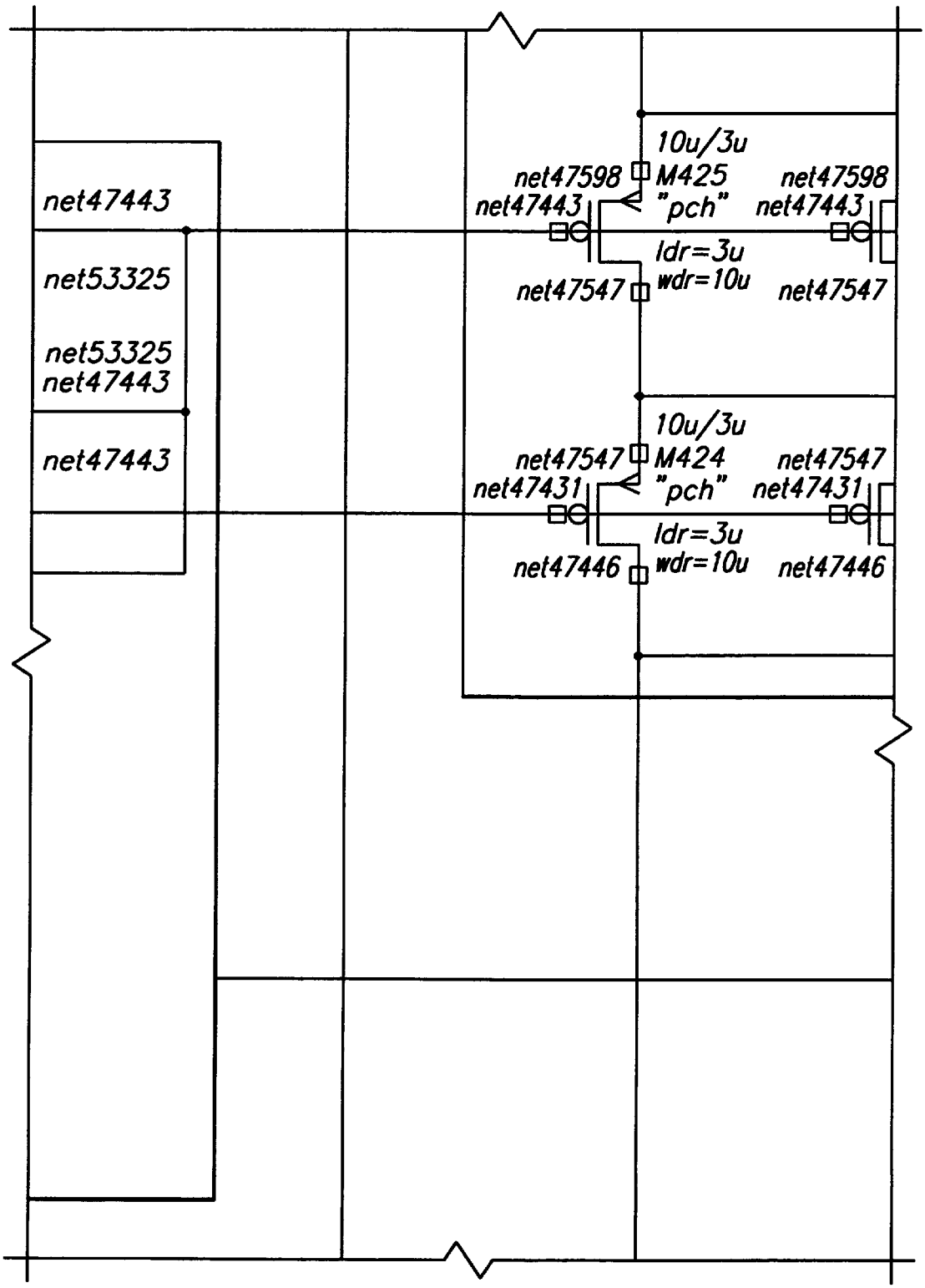

net47443
net53325
net53325
net47443
net47443
10u/3u
net47598
M425
"pch"
net47598
net47443
net47443
ldr=3u
wdr=10u
net47547
net47547
10u/3u
net47547
M424
"pch"
net47547
net47431
net47431
ldr=3u
wdr=10u
net47446
net47446

Fig 16.01CD

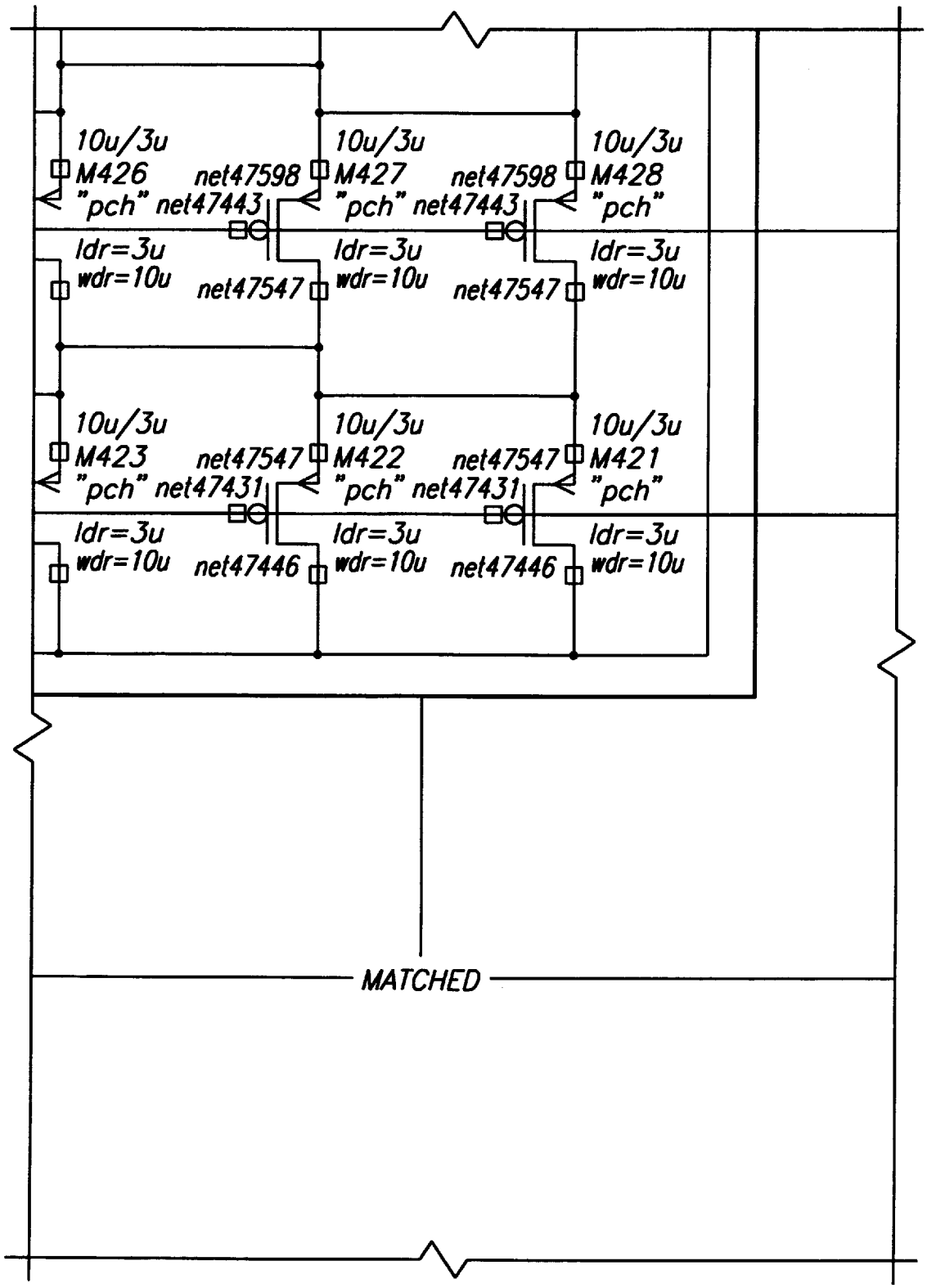

10u/3u
M426
"pch"
net47598
net47443
10u/3u
M427
"pch"
net47598
net47443
10u/3u
M428
"pch"
ldr=3u
wdr=10u
net47547
ldr=3u
wdr=10u
net47547
ldr=3u
wdr=10u
10u/3u
M423
"pch"
net47547
net47431
10u/3u
M422
"pch"
net47547
net47431
10u/3u
M421
"pch"
ldr=3u
wdr=10u
net47446
ldr=3u
wdr=10u
net47446
ldr=3u
wdr=10u
MATCHED

FIG 16.011CE

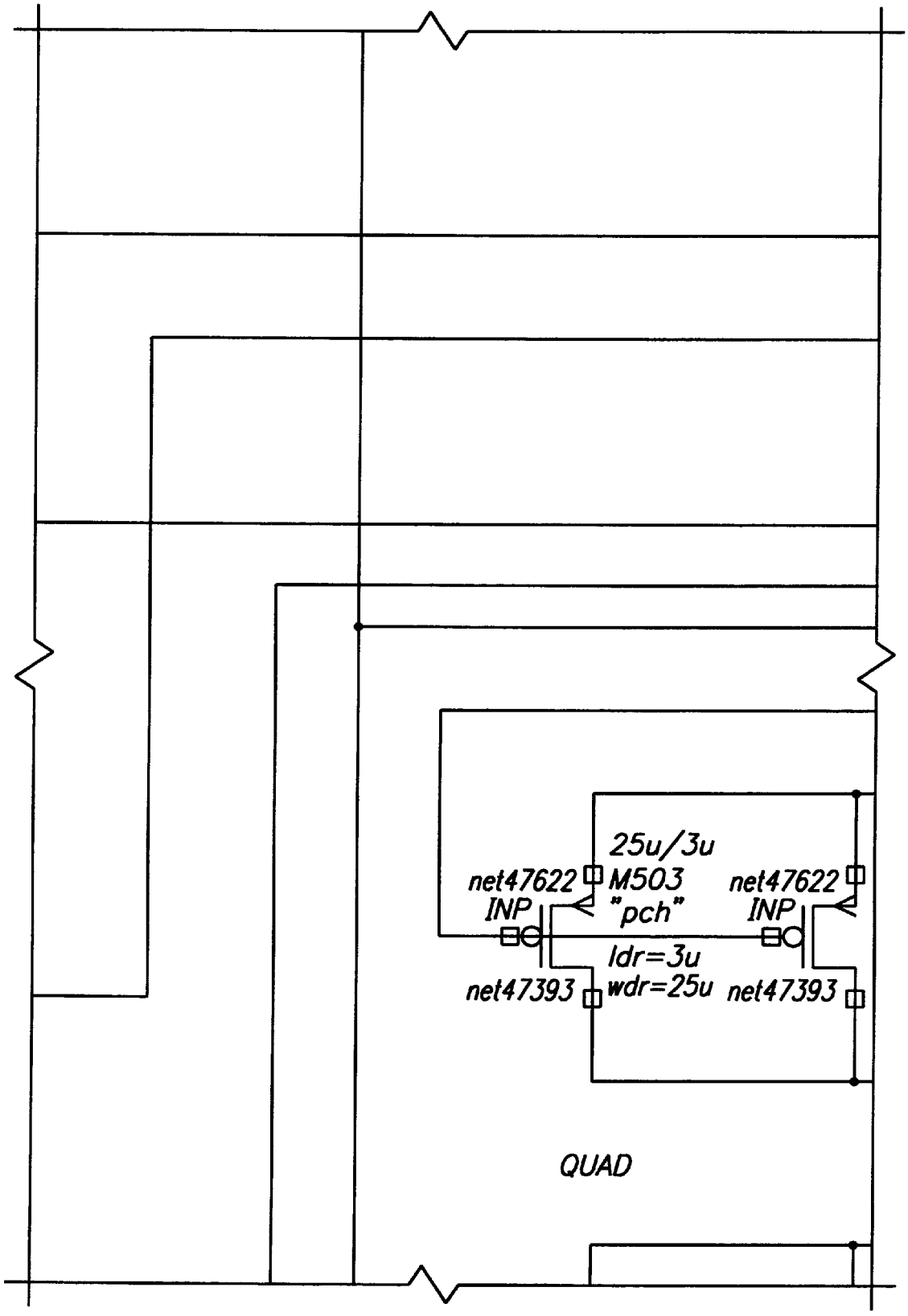

25u/3u
net47622
M503
"pch"
net47622
INP
INP
ldr=3u
net47393
wdr=25u
net47393
QUAD

Fig 16.011CF

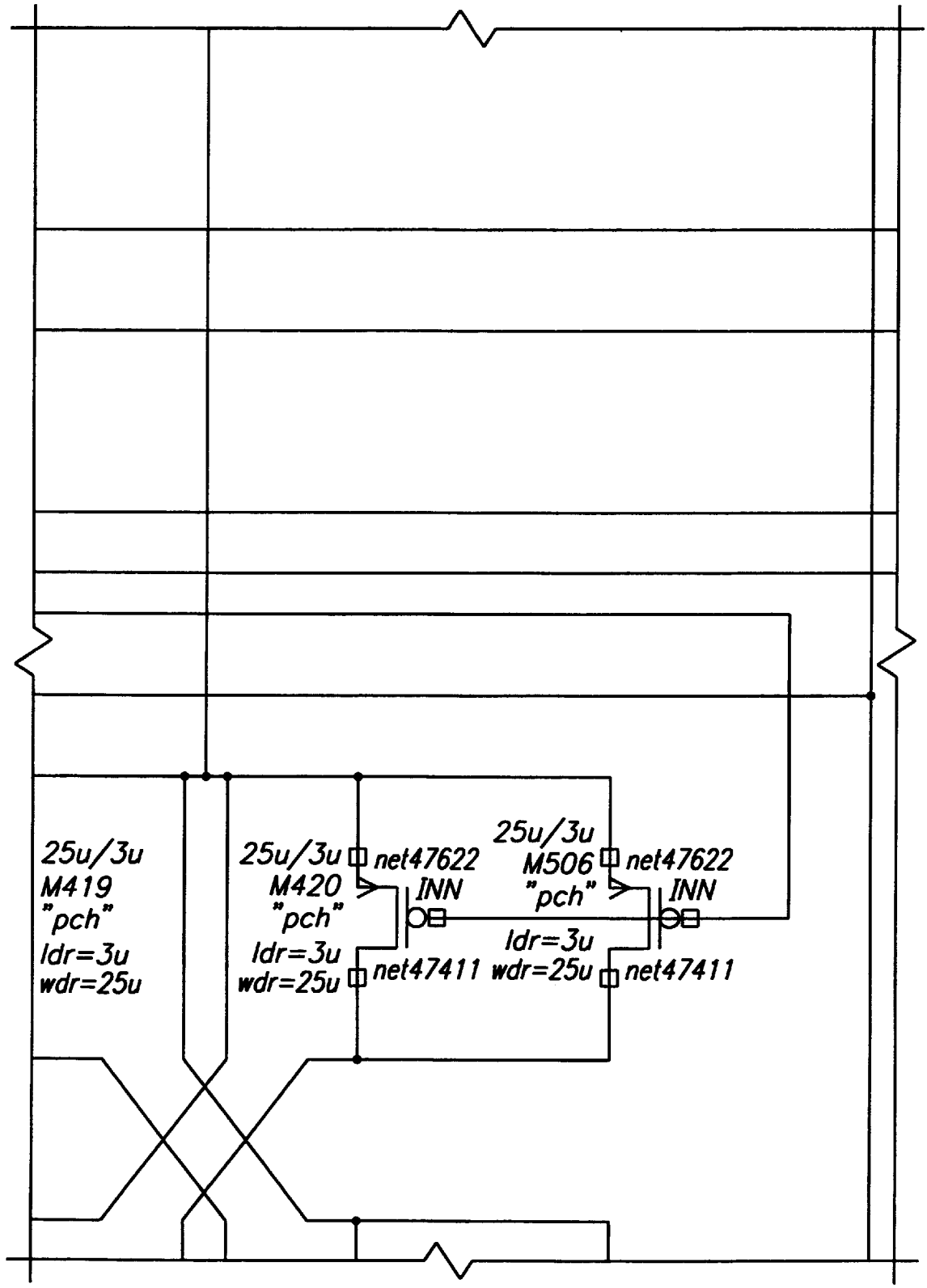

25u/3u
M419
"pch"
ldr=3u
wdr=25u
25u/3u
M420
"pch"
ldr=3u
wdr=25u
net47622
INN
net47411
25u/3u
M506
"pch"
ldr=3u
wdr=25u
net47622
INN
net47411

Fig 16.0116

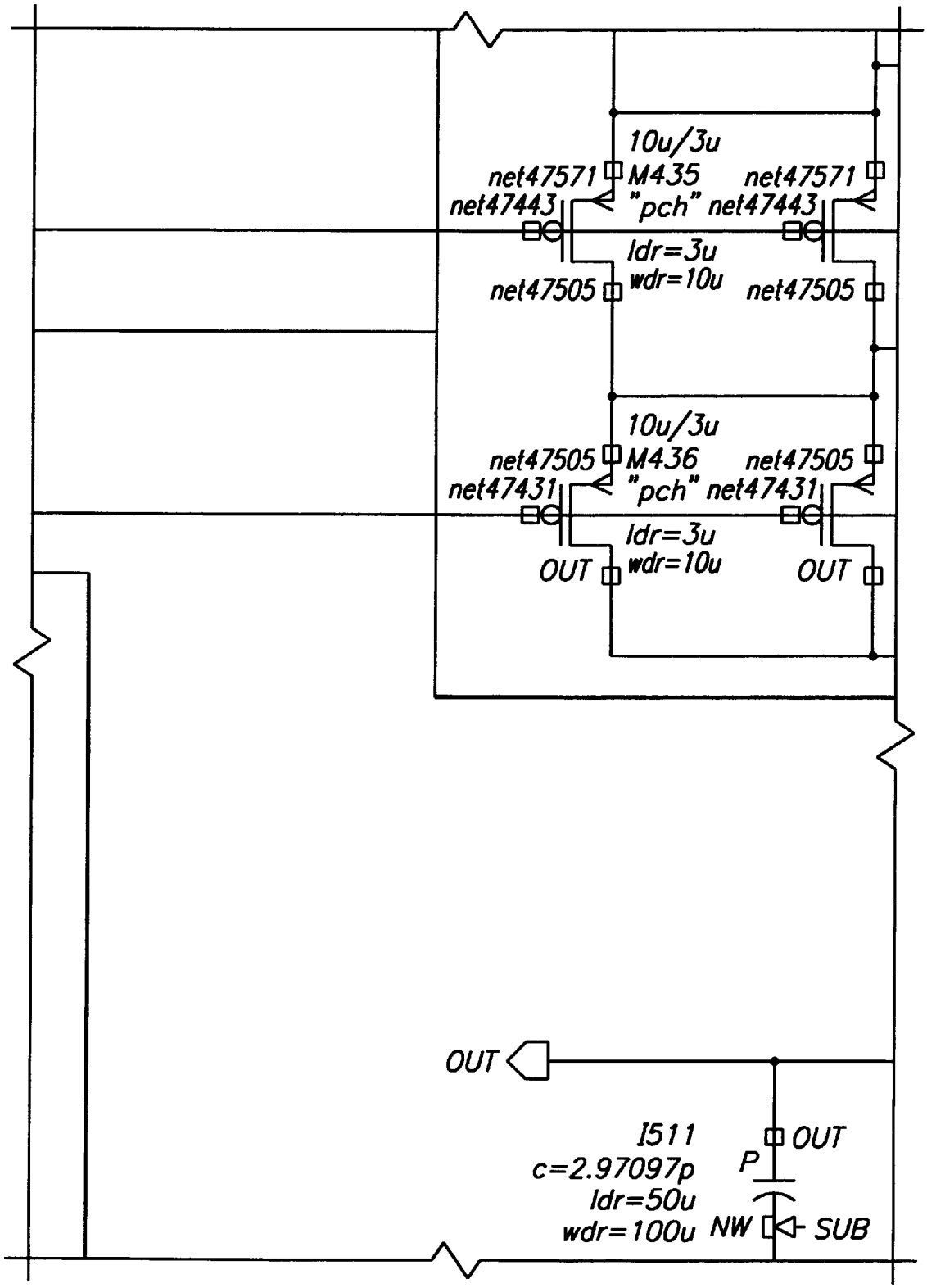

10u/3u
net47571
M435
net47571
net47443
"pch"
net47443
ldr=3u
wdr=10u
net47505
net47505
10u/3u
net47505
M436
net47505
net47431
"pch"
net47431
ldr=3u
wdr=10u
OUT
OUT
OUT
I511
c=2.97097p
ldr=50u
wdr=100u
OUT
P
NW
SUB

Fig 16.011CH

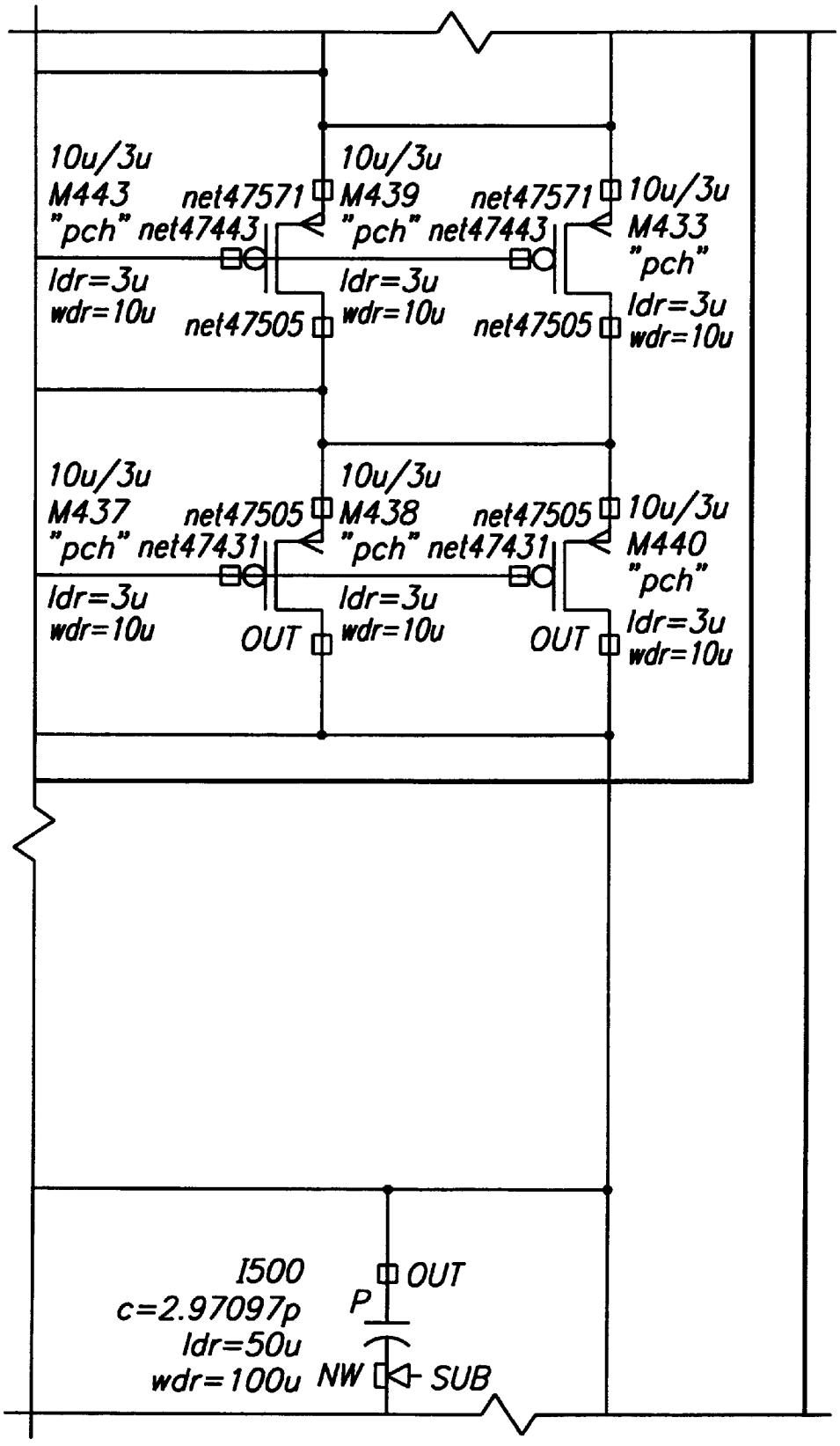


Fig 16.011C11

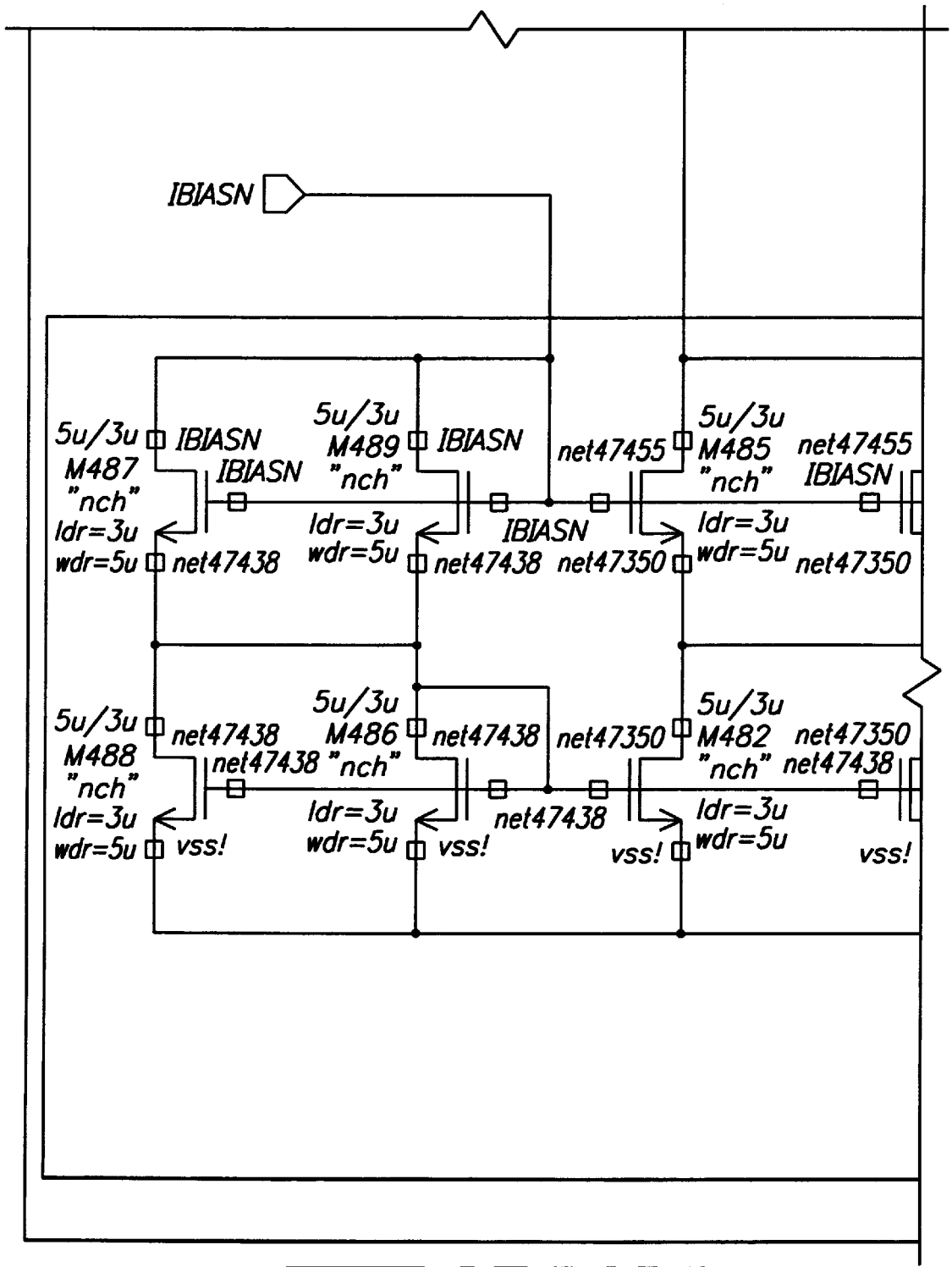

IBIASN
5u/3u
M487
"nch"
ldr=3u
wdr=5u
IBIASN
IBIASN
net47438
5u/3u
M489
"nch"
ldr=3u
wdr=5u
IBIASN
IBIASN
net47438
net47455
IBIASN
net47350
5u/3u
M485
"nch"
ldr=3u
wdr=5u
net47455
IBIASN
net47350
5u/3u
M488
"nch"
ldr=3u
wdr=5u
net47438
net47438
vss!
5u/3u
M486
"nch"
ldr=3u
wdr=5u
net47438
net47438
vss!
net47350
net47438
vss!
5u/3u
M482
"nch"
ldr=3u
wdr=5u
net47350
net47438
vss!

Fig 16.01DA

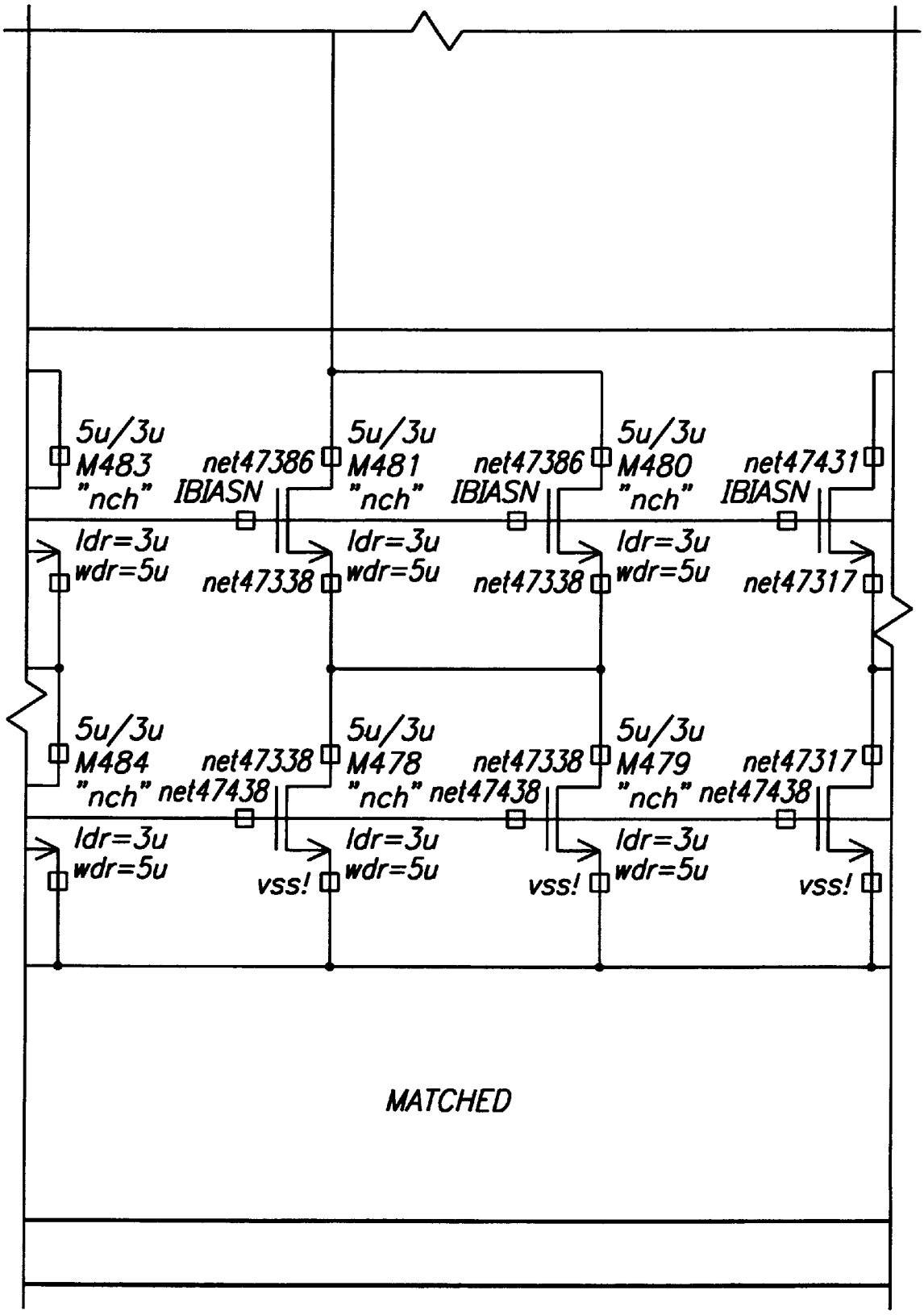


Fig 16.011.00B

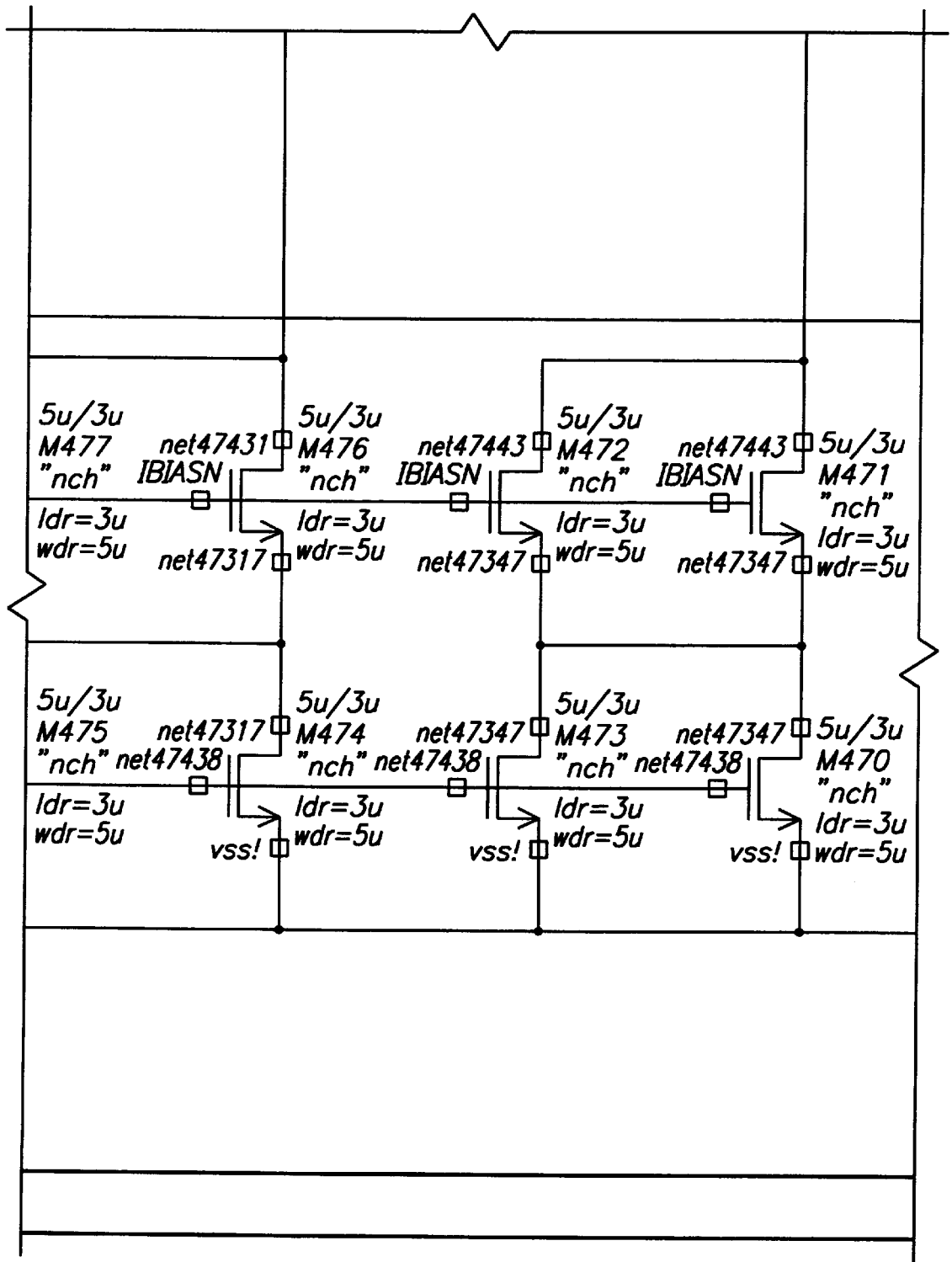

5u/3u
M477
"nch"
ldr=3u
wdr=5u
net47431
IBIASN
net47317
5u/3u
M476
"nch"
ldr=3u
wdr=5u
net47443
IBIASN
net47347
5u/3u
M472
"nch"
ldr=3u
wdr=5u
net47443
IBIASN
net47347
5u/3u
M471
"nch"
ldr=3u
wdr=5u
5u/3u
M475
"nch"
ldr=3u
wdr=5u
net47317
net47438
vss!
5u/3u
M474
"nch"
ldr=3u
wdr=5u
net47347
net47438
vss!
5u/3u
M473
"nch"
ldr=3u
wdr=5u
net47347
net47438
vss!
5u/3u
M470
"nch"
ldr=3u
wdr=5u

Fig 16.01DC

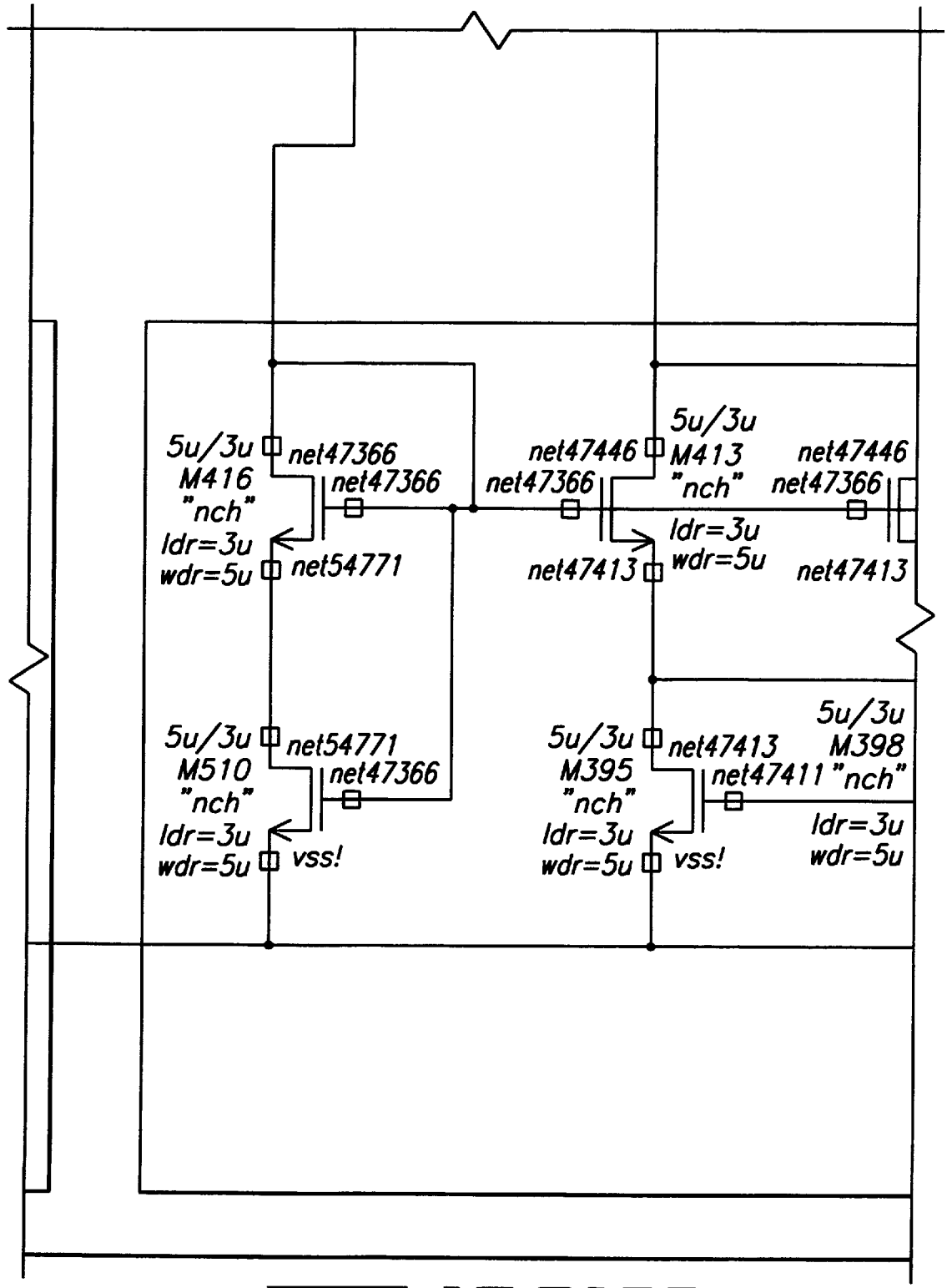
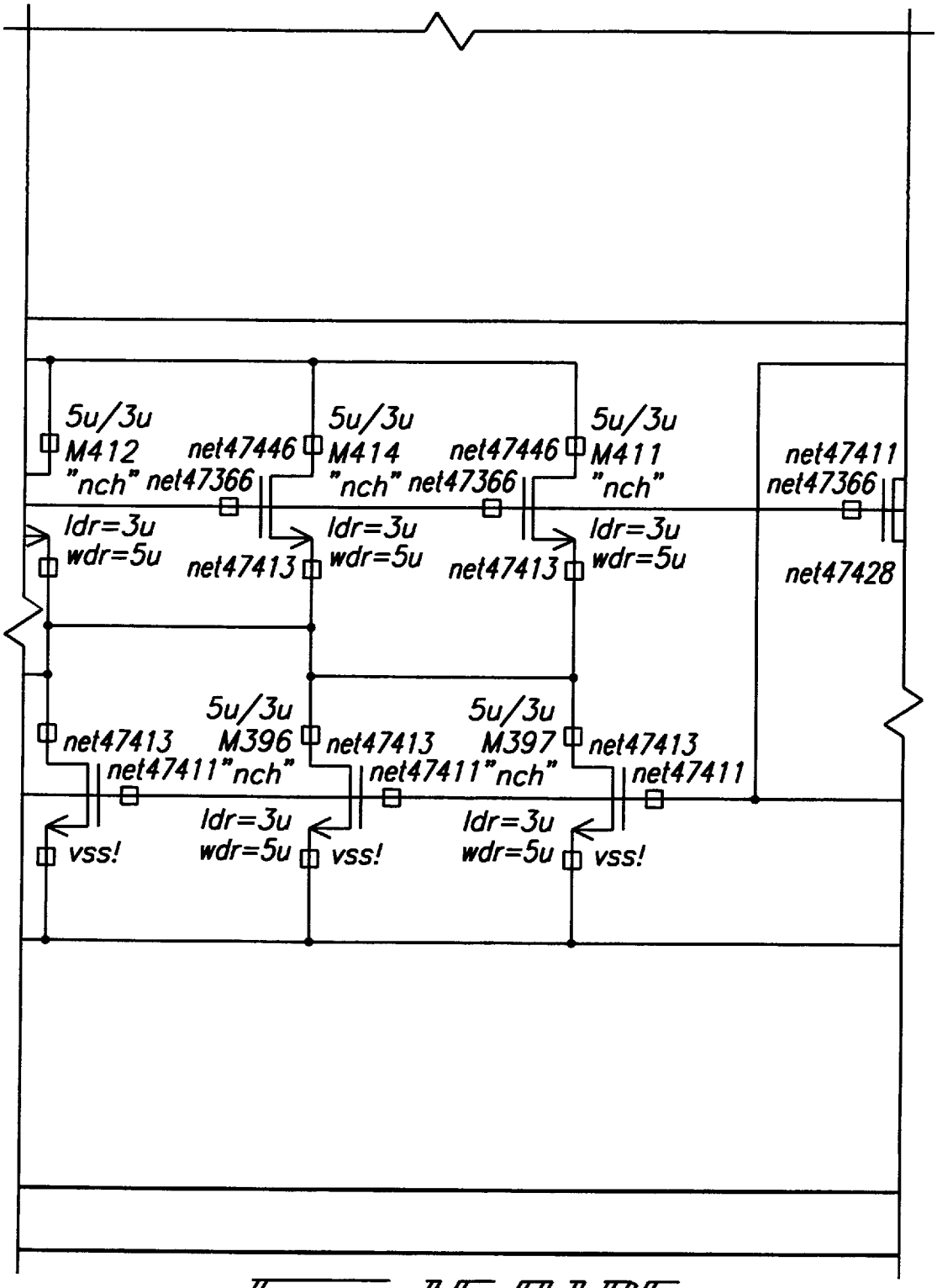

5u/3u
M416
"nch"
ldr=3u
wdr=5u
net47366
net47366
net54771
5u/3u
M510
"nch"
ldr=3u
wdr=5u
net54771
net47366
vss!
net47446
net47366
5u/3u
M413
"nch"
net47413
ldr=3u
wdr=5u
net47446
net47366
net47413
5u/3u
M395
"nch"
ldr=3u
wdr=5u
net47413
net47411
vss!
5u/3u
M398
"nch"
ldr=3u
wdr=5u

Fig 16.0110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M412
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net47446
net47366
5u/3u
M414
"nch"
net47446
net47366
5u/3u
M411
"nch"
net47411
net47366
net47428
ldr=3u
wdr=5u
net47413
ldr=3u
wdr=5u
net47413
ldr=3u
wdr=5u
5u/3u
M396
"nch"
5u/3u
M397
"nch"
net47413
net47411
net47413
net47411
net47413
net47411
ldr=3u
wdr=5u
vss!
ldr=3u
wdr=5u
vss!
ldr=3u
wdr=5u
vss!

Fig 16.01DE

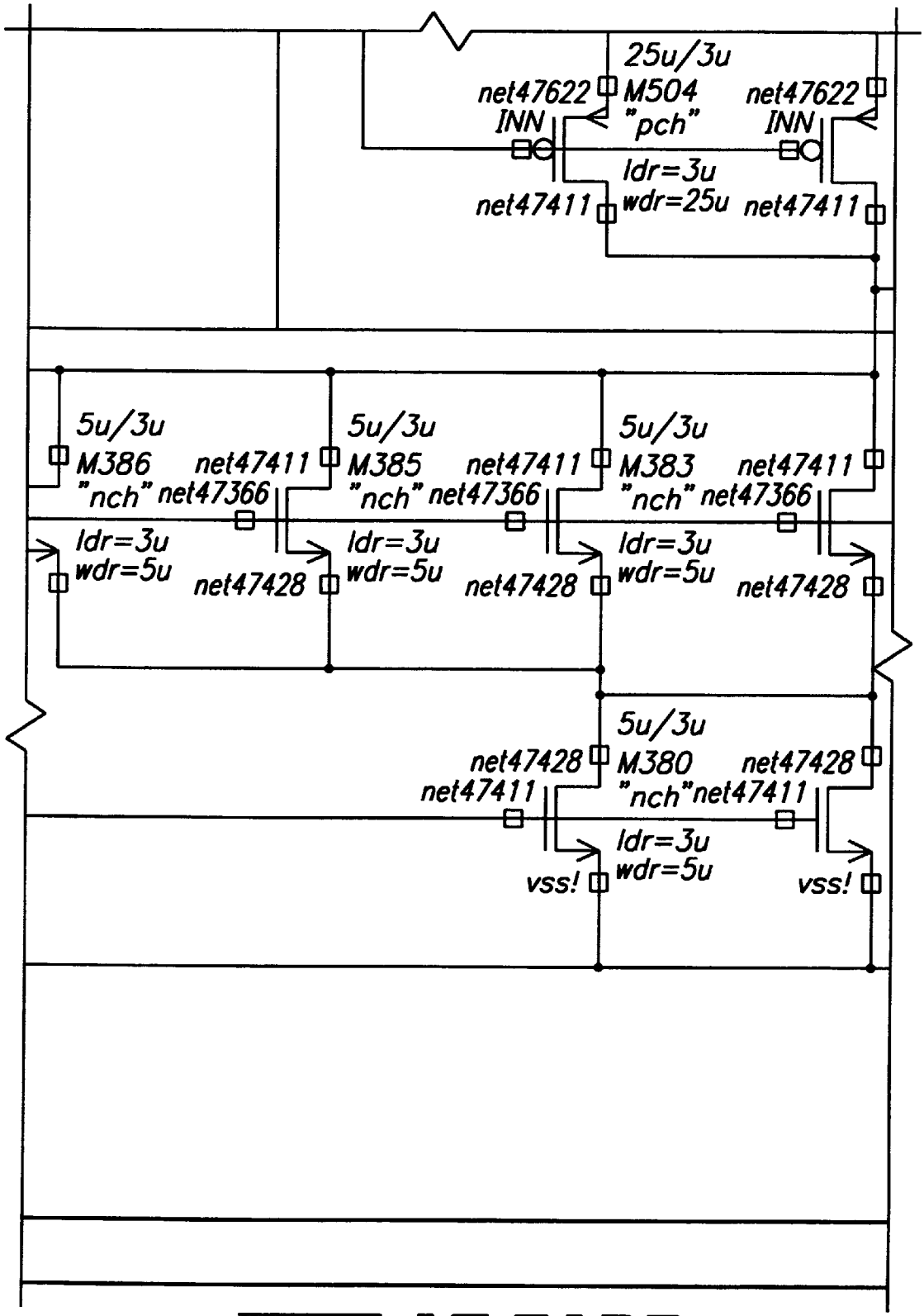
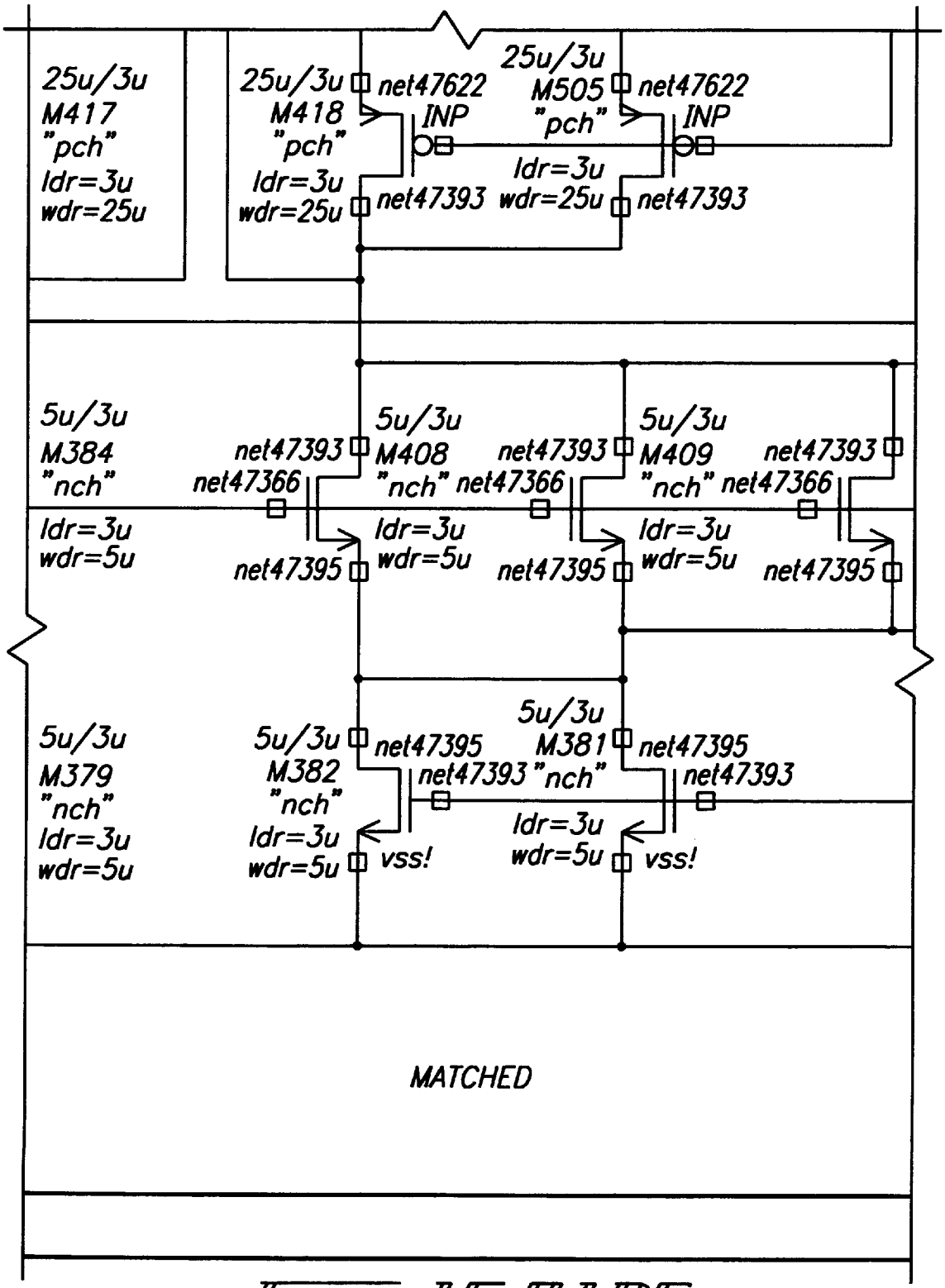

25u/3u
net47622
M504
"pch"
net47622
INN
INN
ldr=3u
net47411
wdr=25u
net47411
5u/3u
M386
net47411
5u/3u
M385
net47411
5u/3u
M383
net47411
"nch"
net47366
"nch"
net47366
"nch"
net47366
ldr=3u
wdr=5u
net47428
ldr=3u
wdr=5u
net47428
ldr=3u
wdr=5u
net47428
5u/3u
net47428
M380
net47428
net47411
"nch"net47411
ldr=3u
wdr=5u
vss!
vss!

Fig 16.011DF


25u/3u
M417
"pch"
ldr=3u
wdr=25u
25u/3u
M418
"pch"
ldr=3u
wdr=25u
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INP
net47393
25u/3u
M505
"pch"
ldr=3u
wdr=25u
net47622
INP
net47393
5u/3u
M384
"nch"
ldr=3u
wdr=5u
net47393
net47366
net47395
5u/3u
M408
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M409
"nch"
ldr=3u
wdr=5u
net47393
net47366
net47395
5u/3u
M379
"nch"
ldr=3u
wdr=5u
5u/3u
M382
"nch"
ldr=3u
wdr=5u
net47395
net47393
vss!
5u/3u
M381
"nch"
ldr=3u
wdr=5u
net47395
net47393
vss!
MATCHED

Fig 16.01DG

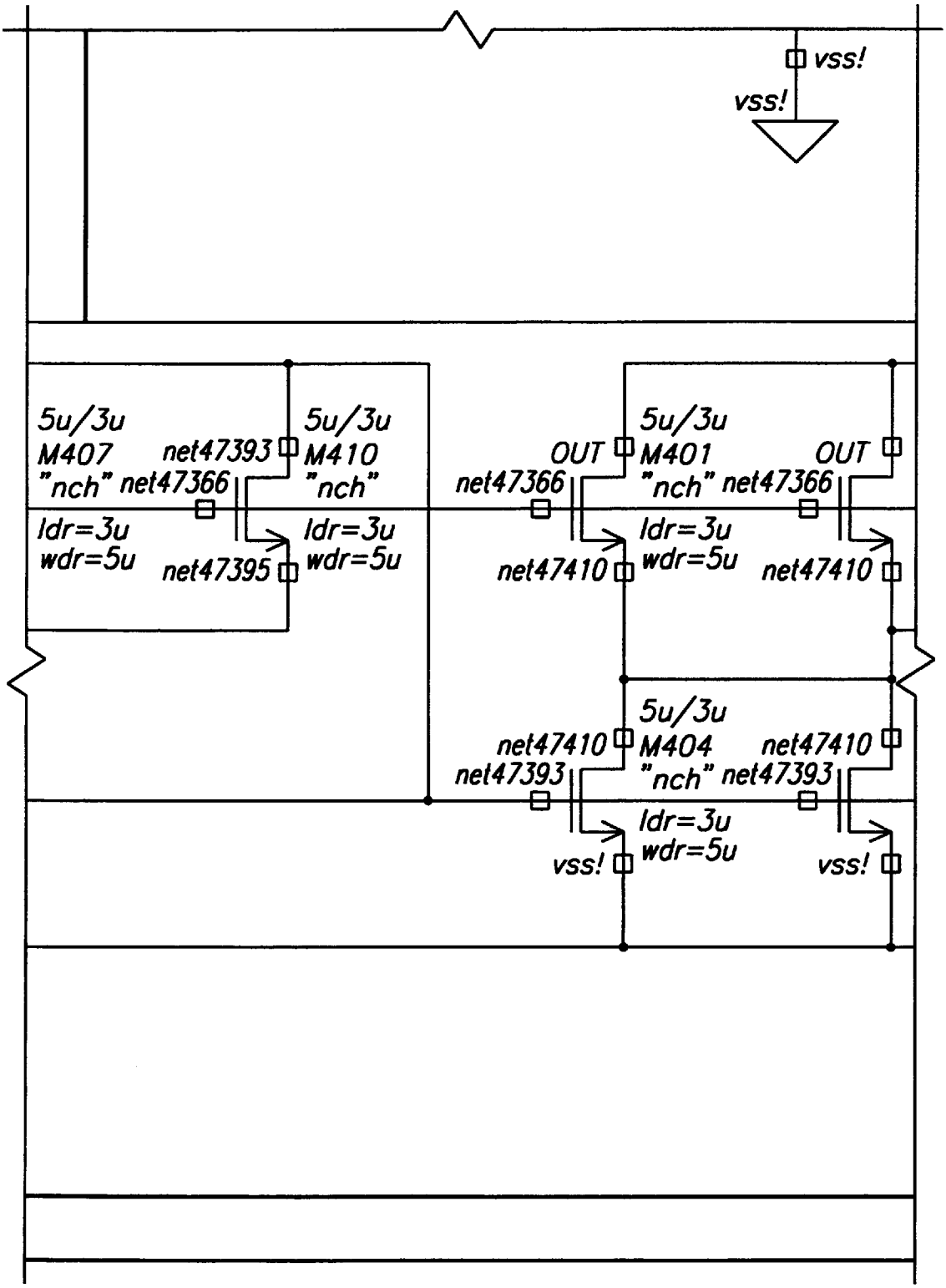

vss!
vss!
5u/3u
M407
"nch"
net47393
net47366
5u/3u
M410
"nch"
ldr=3u
wdr=5u
net47395
ldr=3u
wdr=5u
OUT
net47366
5u/3u
M401
"nch"
net47366
OUT
ldr=3u
wdr=5u
net47410
net47410
5u/3u
M404
"nch"
net47410
net47393
net47410
net47393
ldr=3u
wdr=5u
vss!
vss!

Fig 16.01DH

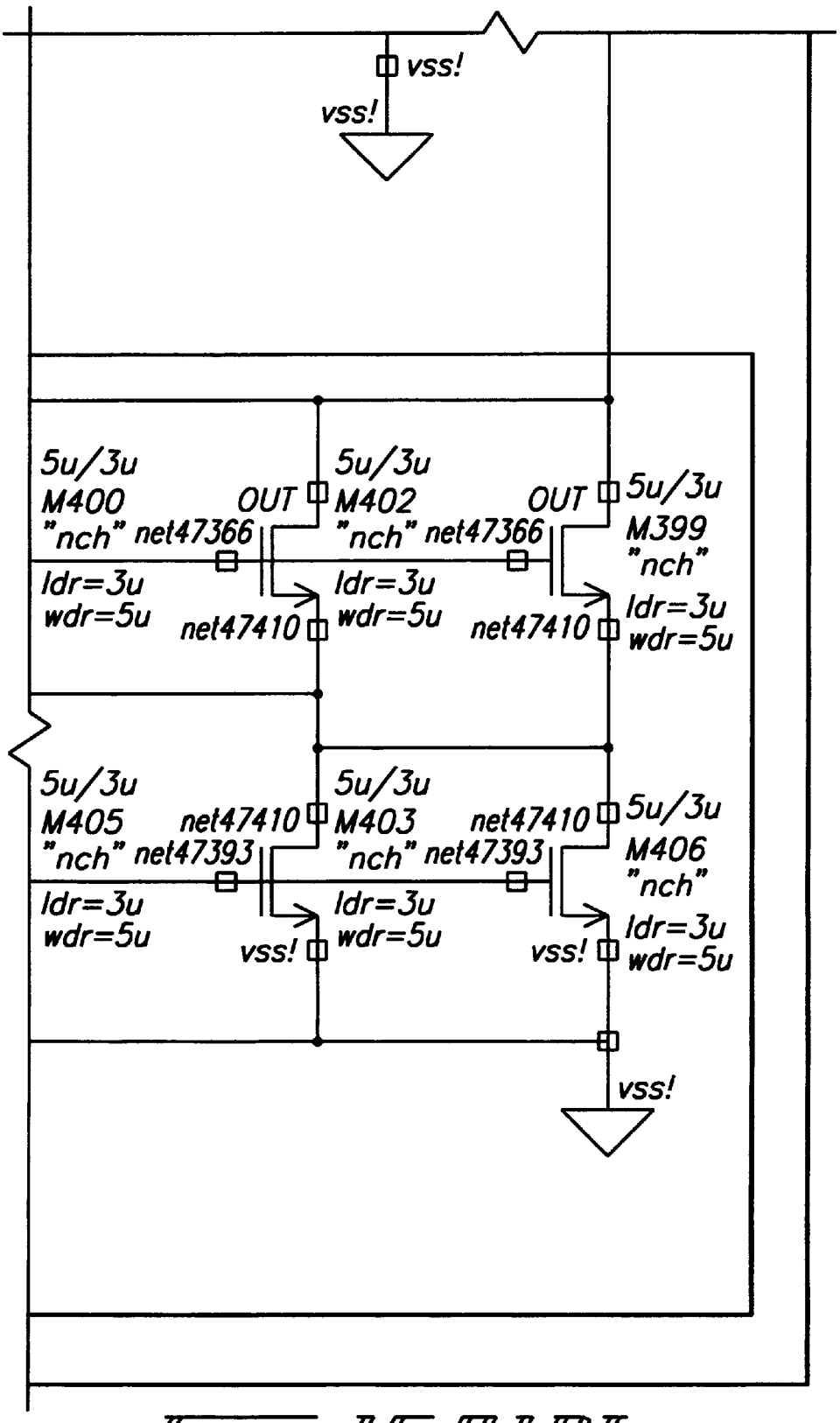

vss!
vss!
5u/3u
M400
"nch"
net47366
OUT
5u/3u
M402
"nch"
net47366
OUT
5u/3u
M399
"nch"
ldr=3u
wdr=5u
net47410
ldr=3u
wdr=5u
net47410
ldr=3u
wdr=5u
5u/3u
M405
"nch"
net47393
net47410
5u/3u
M403
"nch"
net47393
net47410
5u/3u
M406
"nch"
ldr=3u
wdr=5u
vss!
ldr=3u
wdr=5u
vss!
ldr=3u
wdr=5u
vss!

Fig 16.0110

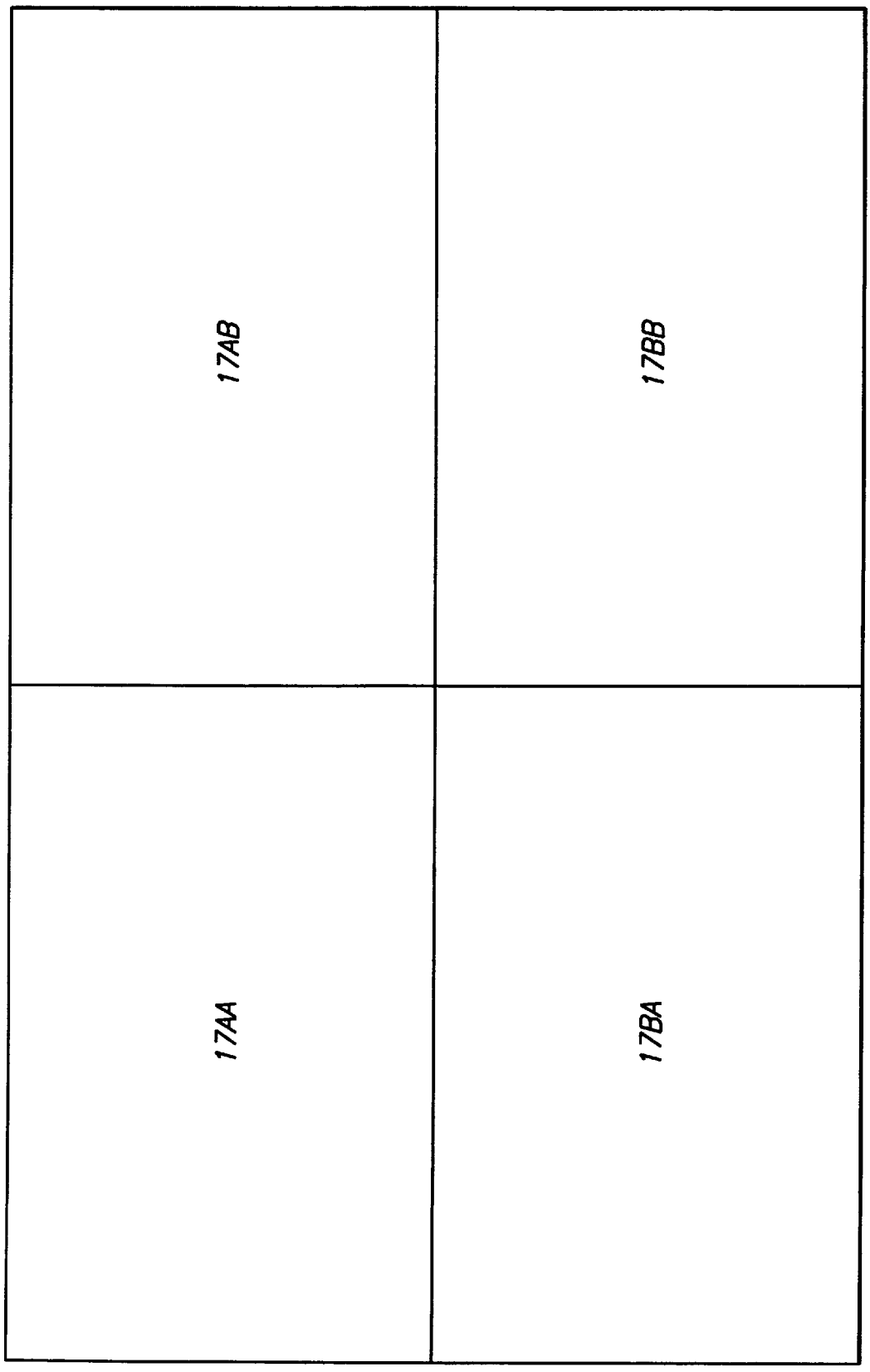
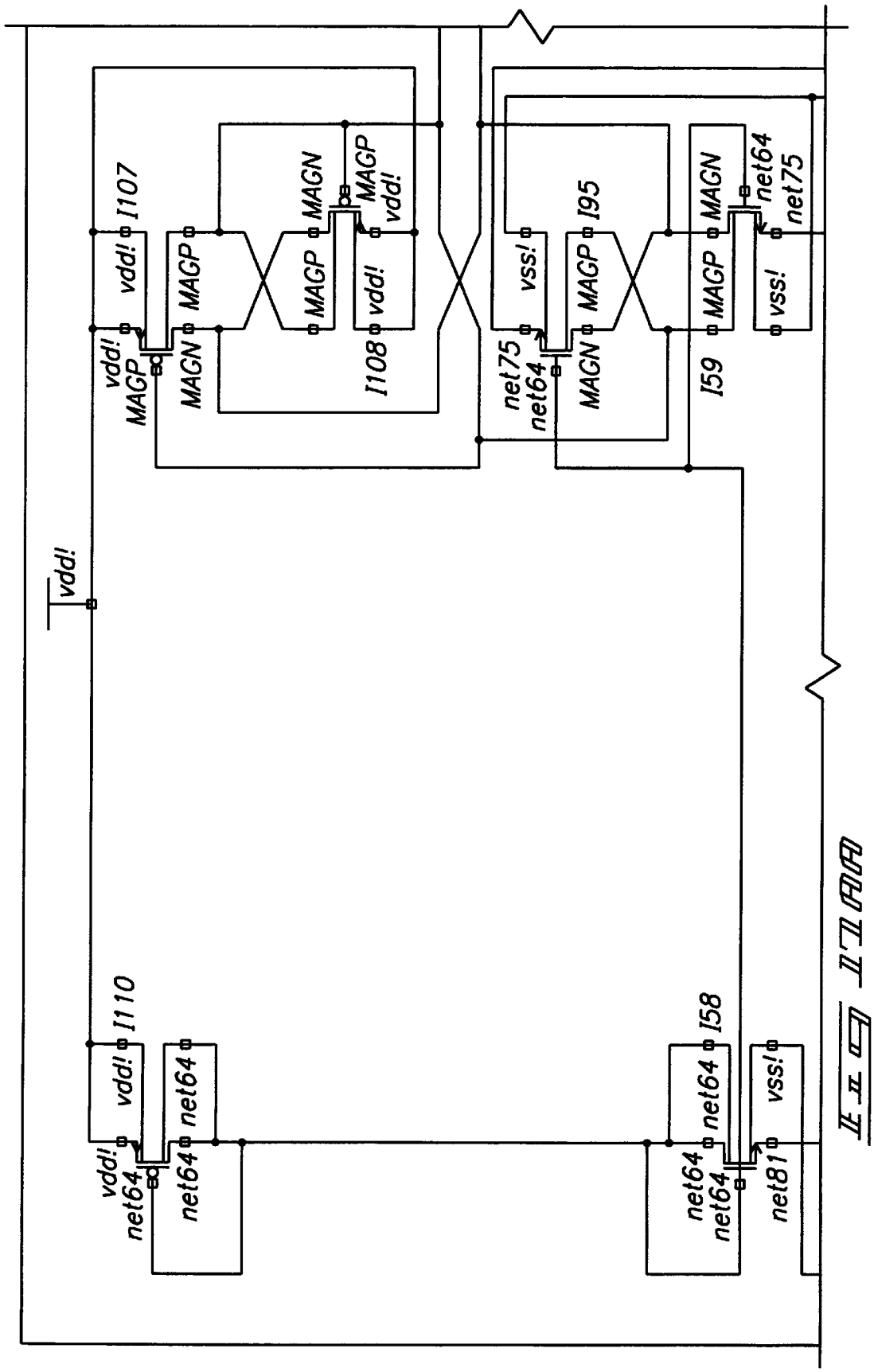
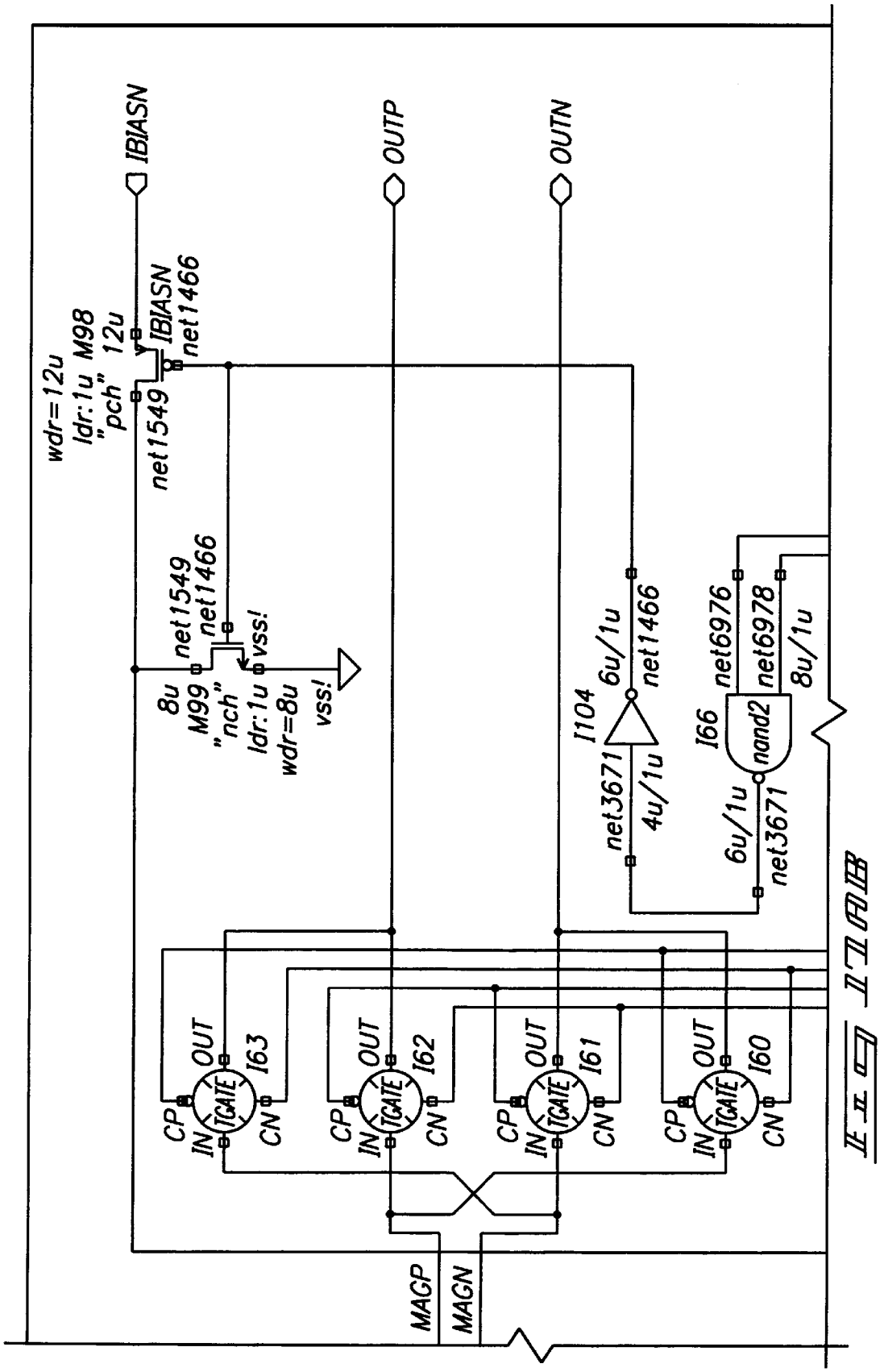


FIG 17


I107
vdd!
MAGP
MAGN
MAGN
MAGP
MAGP
vdd!
vdd!
I108
I95
vss!
MAGP
net75
net64
MAGN
MAGN
MAGP
net64
net75
vss!
I59
vdd!
I110
vdd!
net64
net64
net64
I58
net64
vss!
net64
net81
VDD LL


IBIASN
OUTP
OUTN
wdr=12u
ldr:1u M98
"pch" 12u
net1549
IBIASN net1466
net1549
net1466
8u
M99
"nch"
ldr:1u
wdr=8u
vss!
vss!
I104
6u/1u
net1466
net3671
4u/1u
I66
nand2
net6976
net6978
8u/1u
6u/1u
net3671
CP
IN
TGATE
CN
OUT
I63
I62
I61
I60
MAGP
MAGN

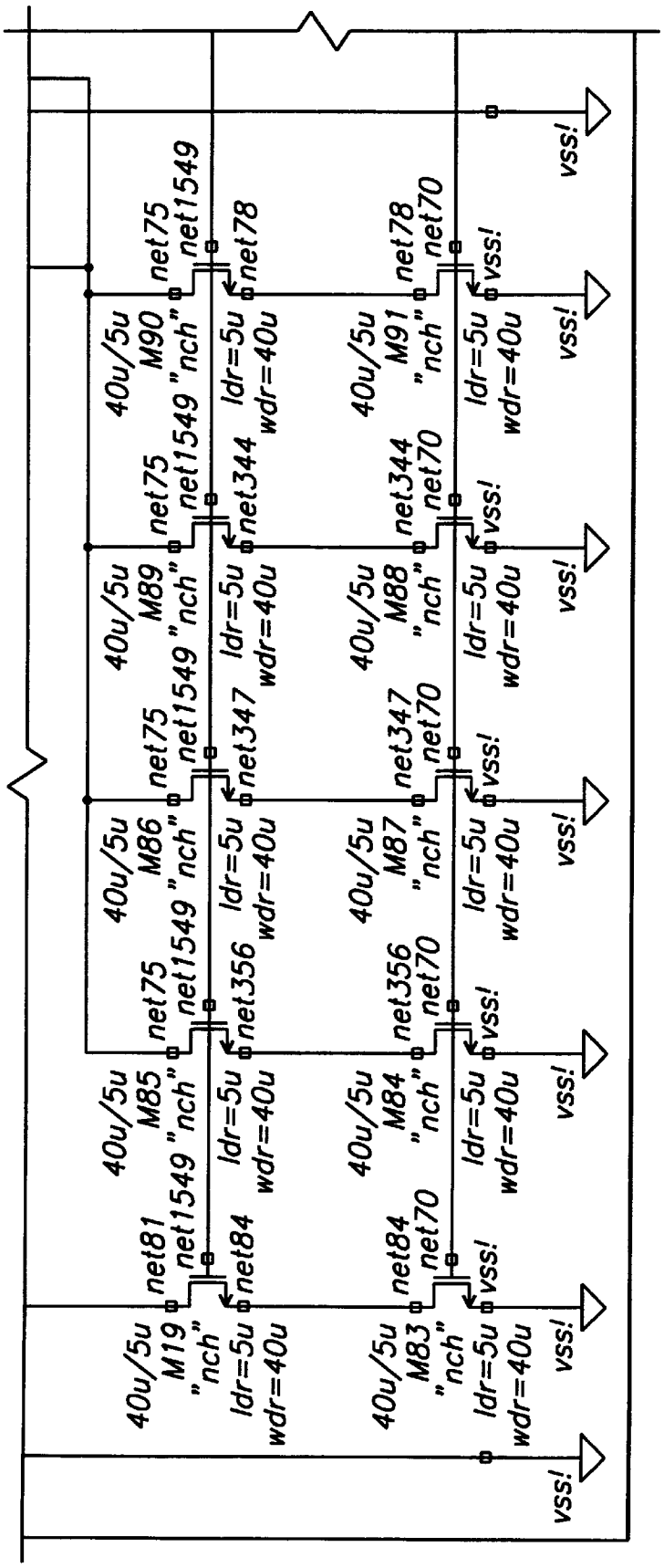
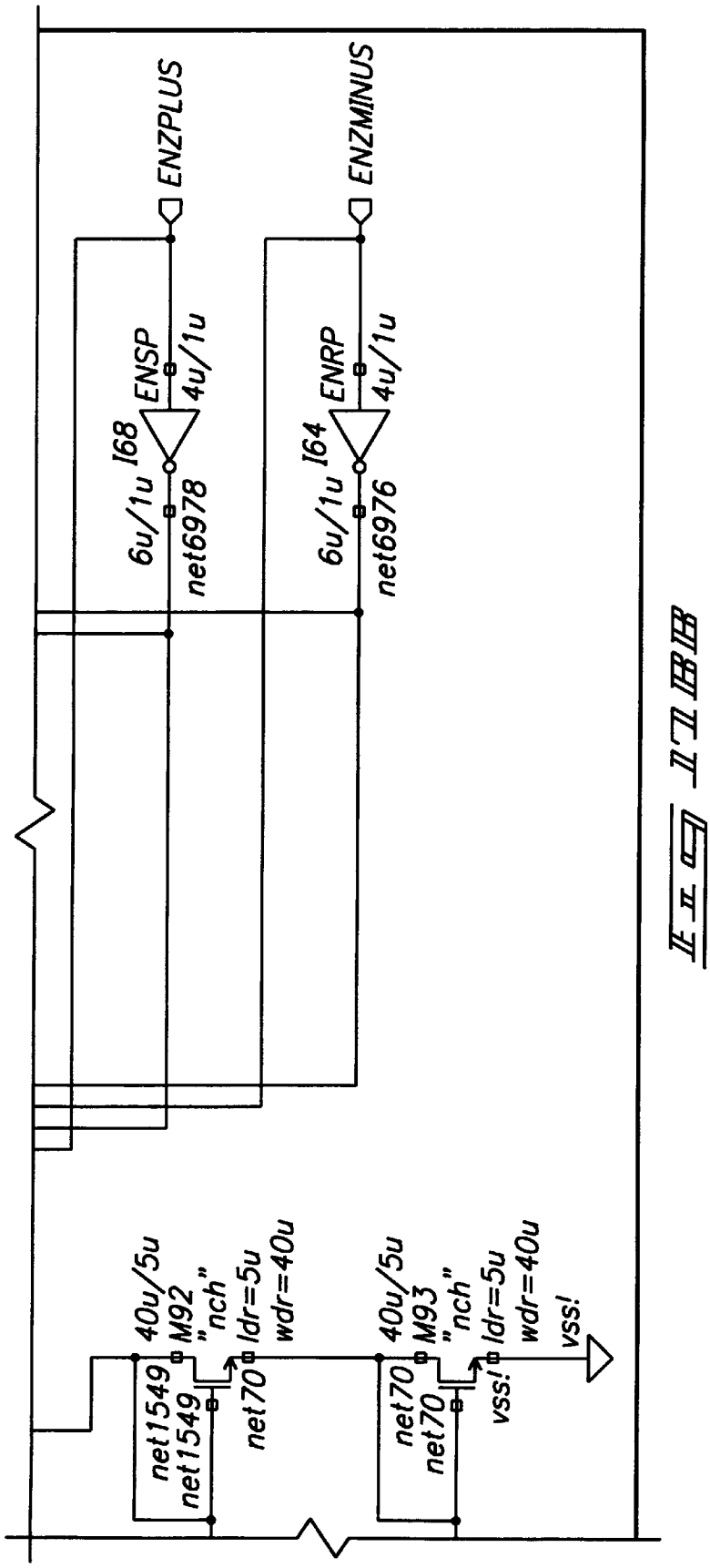
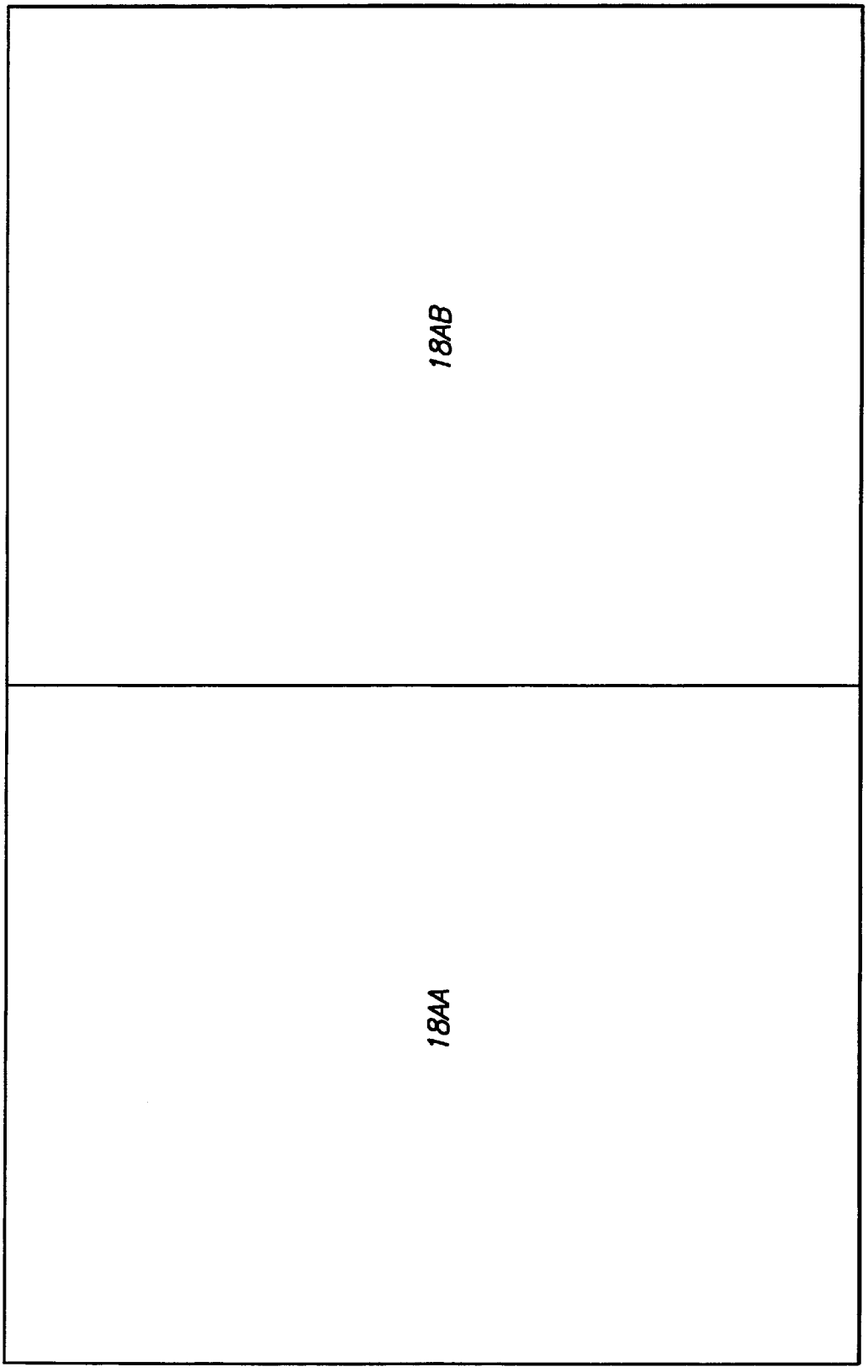

40u/5u
M19
"nch"
ldr=5u
wdr=40u
net81
net1549
net84
40u/5u
M83
"nch"
ldr=5u
wdr=40u
net84
net70
vss!
vss!
40u/5u
M85
"nch"
ldr=5u
wdr=40u
net75
net1549
net356
40u/5u
M84
"nch"
ldr=5u
wdr=40u
net356
net70
vss!
vss!
40u/5u
M86
"nch"
ldr=5u
wdr=40u
net75
net1549
net347
40u/5u
M87
"nch"
ldr=5u
wdr=40u
net347
net70
vss!
vss!
40u/5u
M89
"nch"
ldr=5u
wdr=40u
net75
net1549
net344
40u/5u
M88
"nch"
ldr=5u
wdr=40u
net344
net70
vss!
vss!
40u/5u
M90
"nch"
ldr=5u
wdr=40u
net75
net1549
net78
40u/5u
M91
"nch"
ldr=5u
wdr=40u
net78
net70
vss!
vss!
vss!
vss!

FIG. 1181A


ENZPLUS
ENZMINUS
ENSP
4u/1u
ENRP
4u/1u
I68
6u/1u
net6978
I64
6u/1u
net6976
40u/5u
M92
"nch"
ldr=5u
wdr=40u
net1549
net1549
net70
40u/5u
M93
"nch"
ldr=5u
wdr=40u
net70
net70
vss!
vss!


18AB
18AA
FIG. 18B

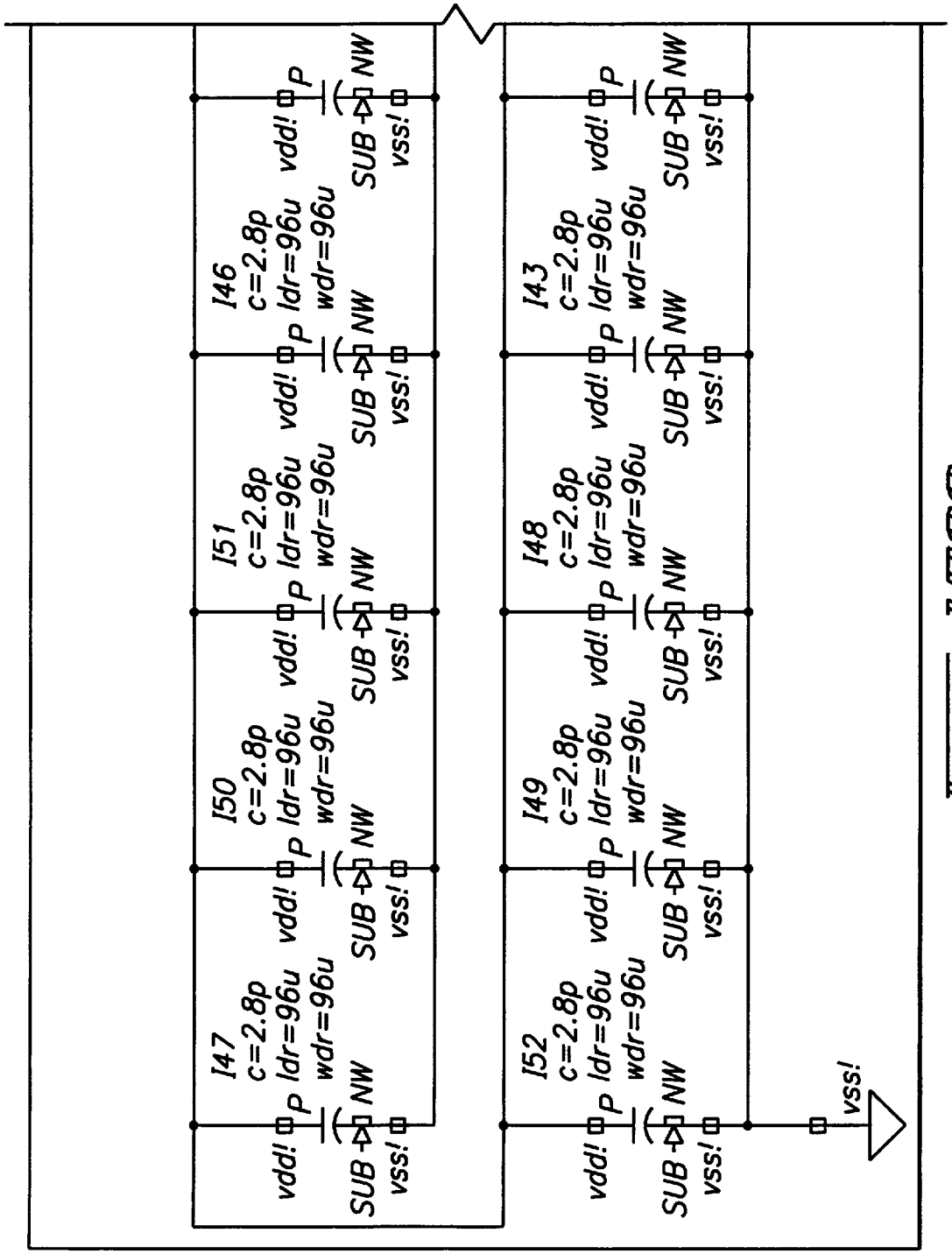

I47
c=2.8p
ldr=96u
wdr=96u
vdd!
P
NW
SUB
vss!
I50
I51
I46
I52
I49
I48
I43
vss!

FIG. 1183A

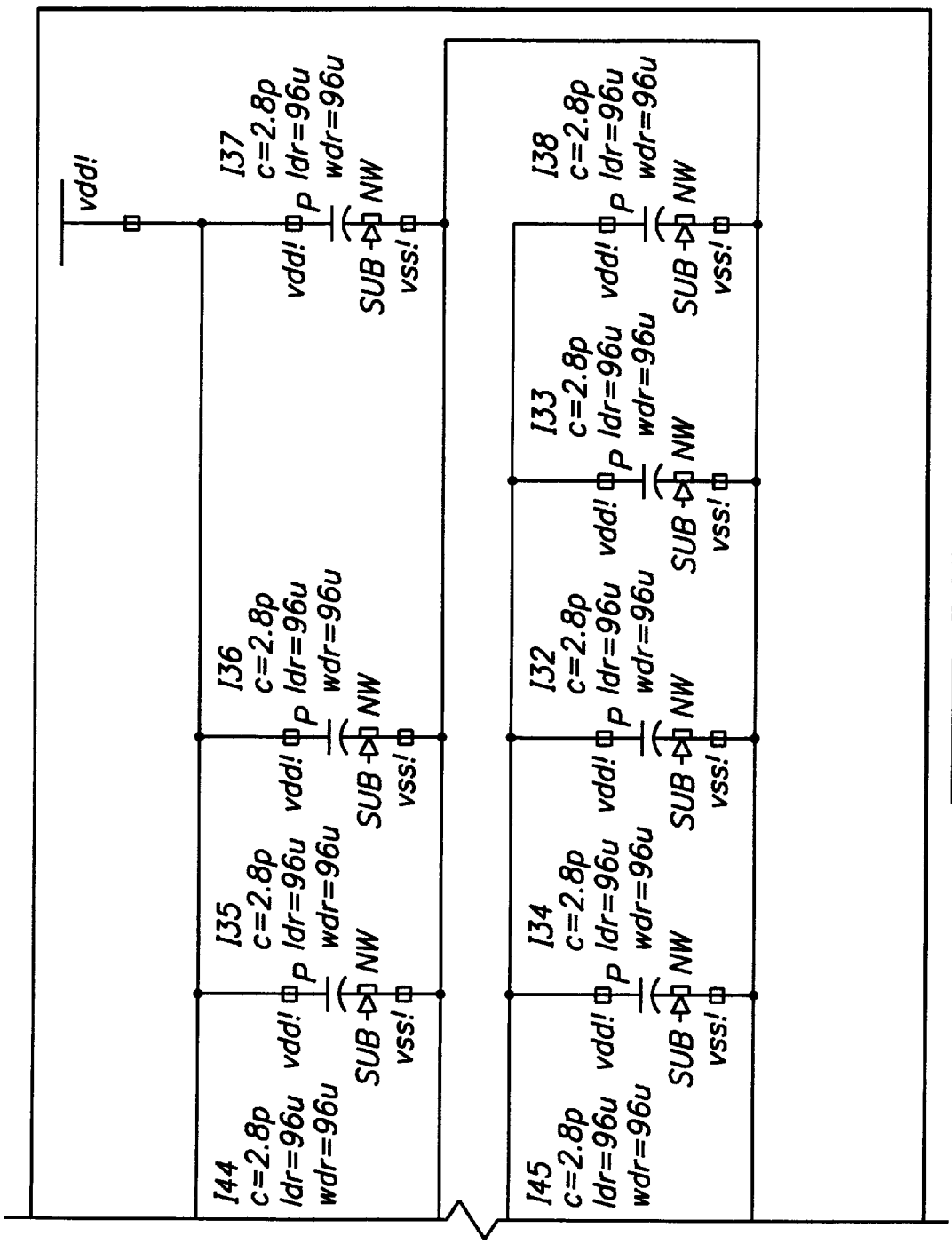

vdd!
I37 c=2.8p ldr=96u wdr=96u
I38 c=2.8p ldr=96u wdr=96u
I36 c=2.8p ldr=96u wdr=96u
I33 c=2.8p ldr=96u wdr=96u
I35 c=2.8p ldr=96u wdr=96u
I32 c=2.8p ldr=96u wdr=96u
I44 c=2.8p ldr=96u wdr=96u
I34 c=2.8p ldr=96u wdr=96u
I45 c=2.8p ldr=96u wdr=96u
P
NW
SUB
vdd!
vss!

FIG 11B

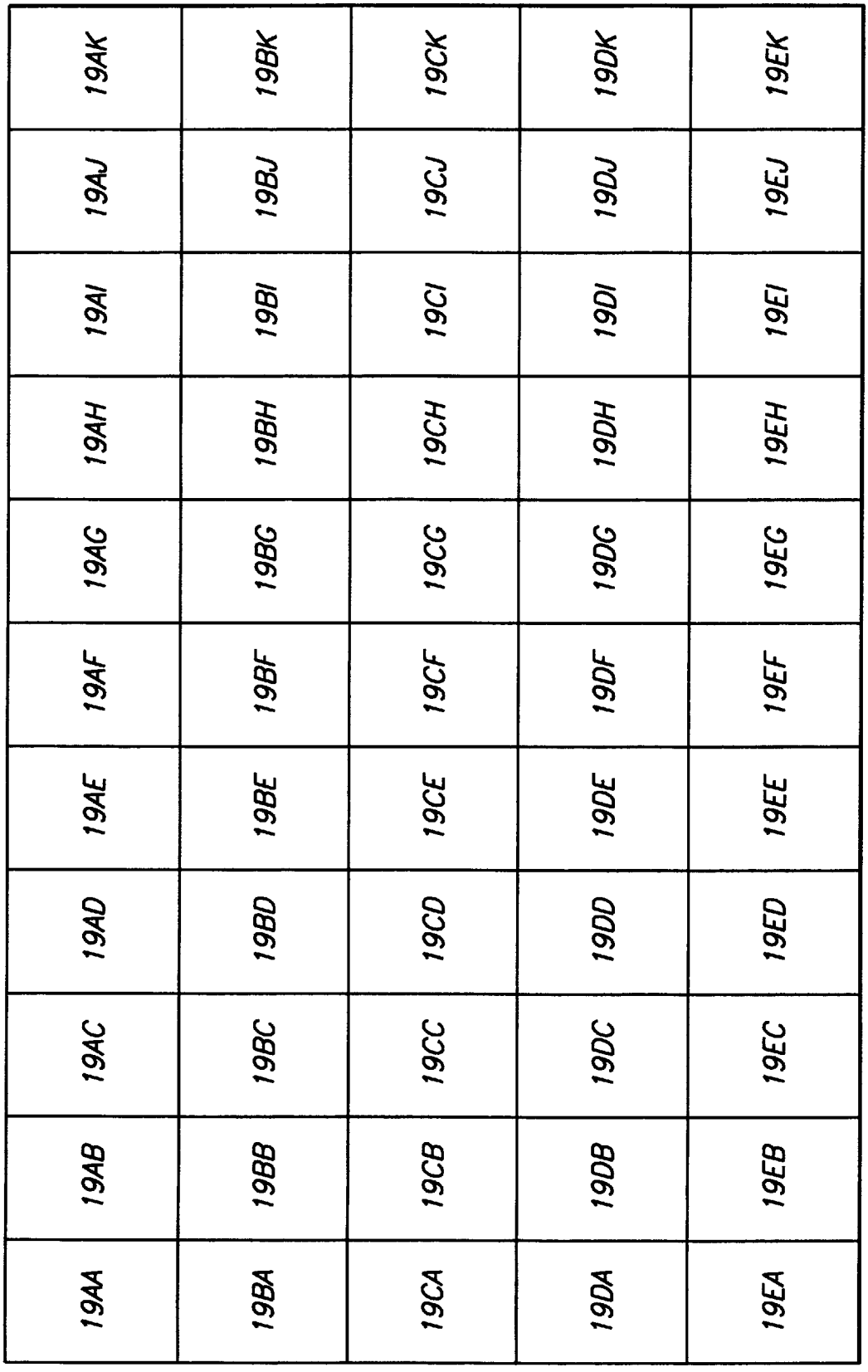

19AA 19AB 19AC 19AD 19AE 19AF 19AG 19AH 19AI 19AJ 19AK
19BA 19BB 19BC 19BD 19BE 19BF 19BG 19BH 19BI 19BJ 19BK
19CA 19CB 19CC 19CD 19CE 19CF 19CG 19CH 19CI 19CJ 19CK
19DA 19DB 19DC 19DD 19DE 19DF 19DG 19DH 19DI 19DJ 19DK
19EA 19EB 19EC 19ED 19EE 19EF 19EG 19EH 19EI 19EJ 19EK

FIG 19

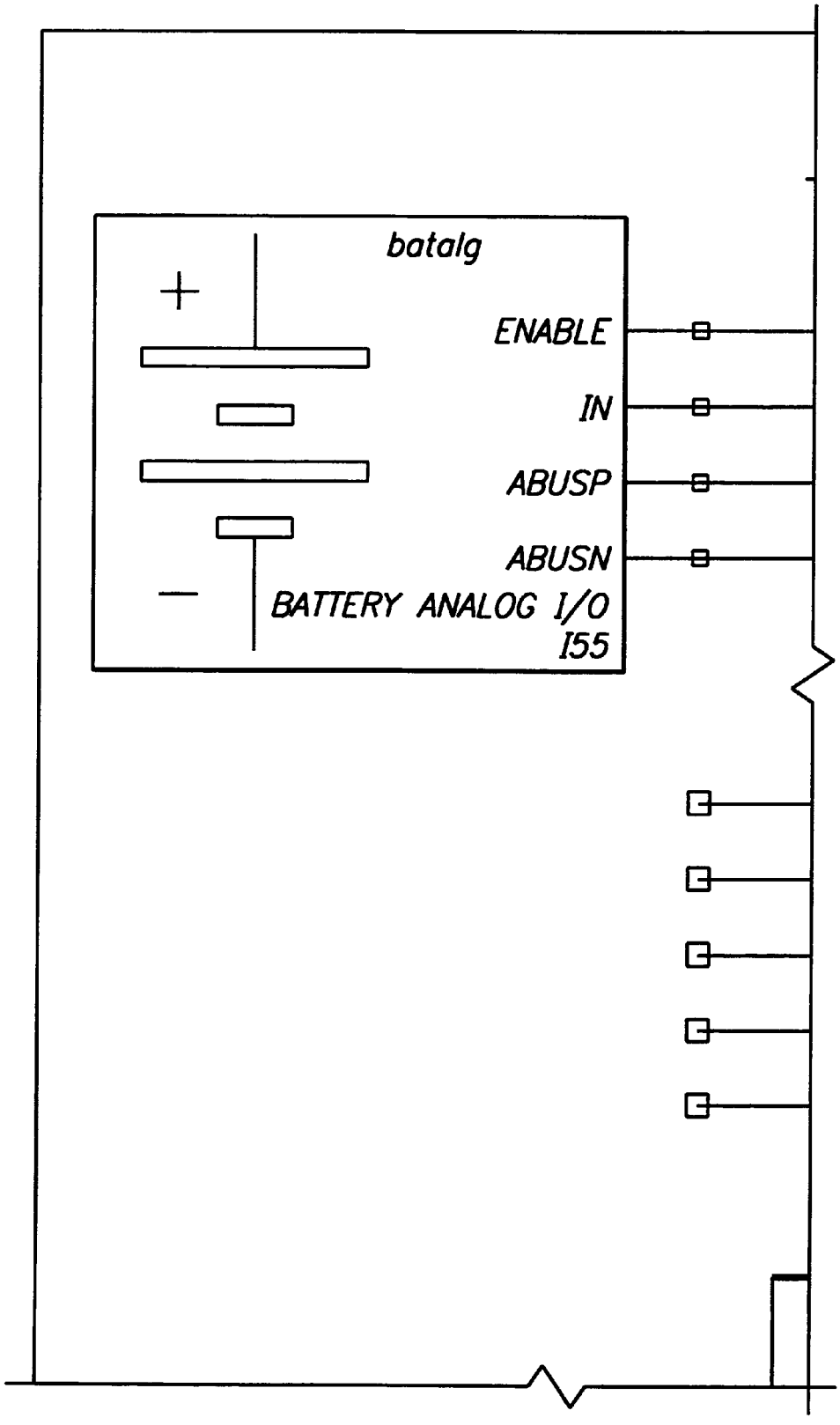


Fig 19AA

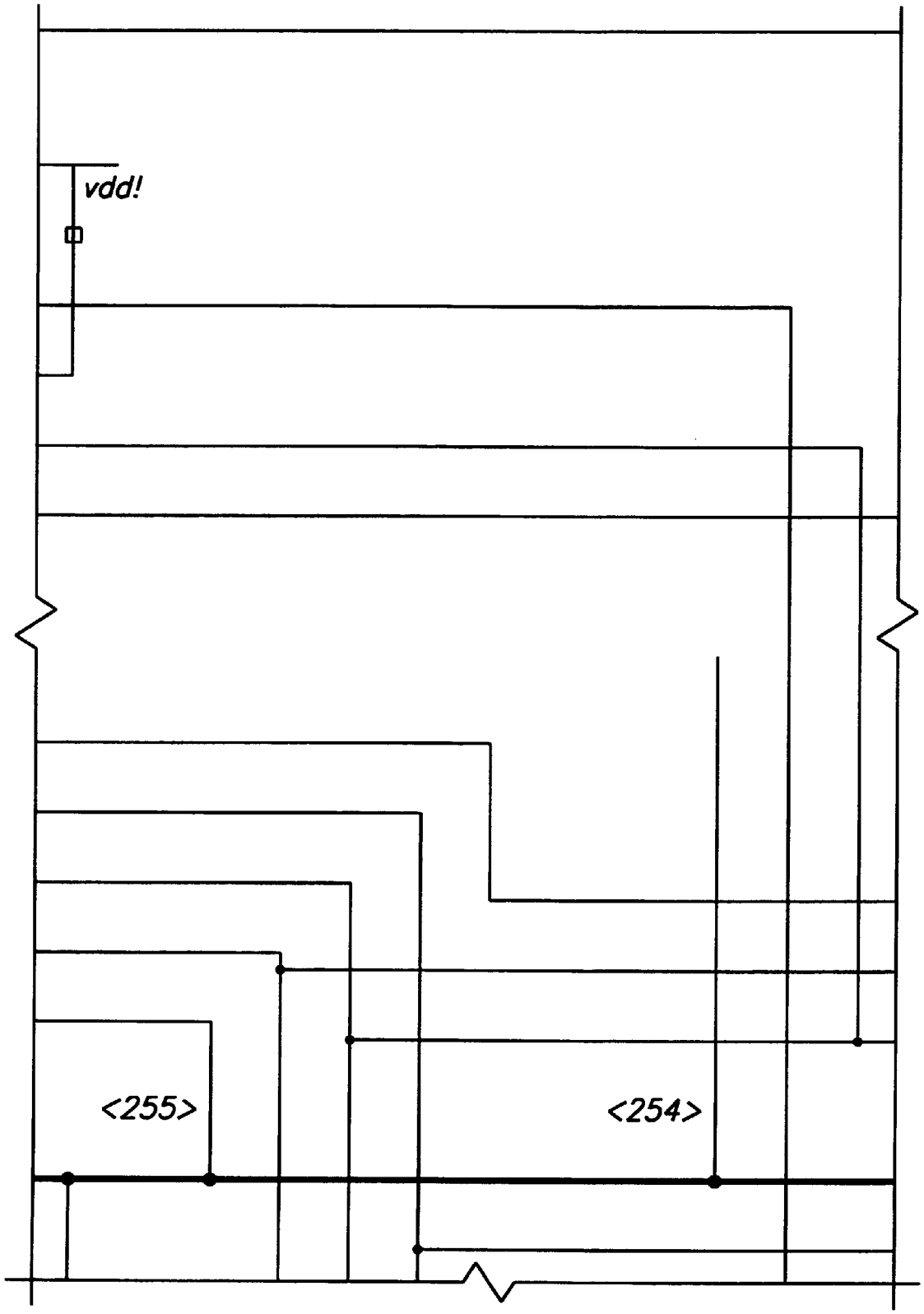


Fig 19AB

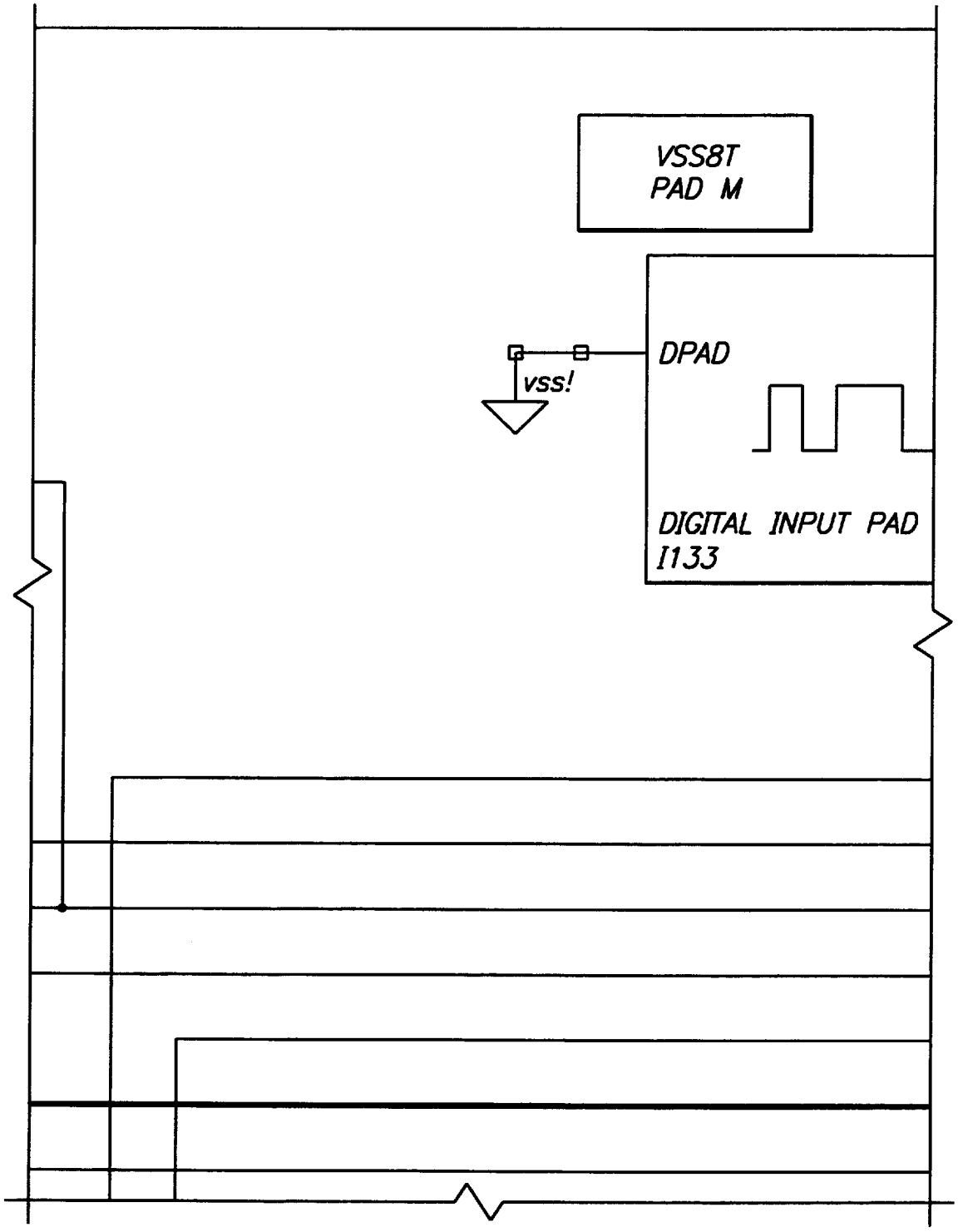


Fig 19AC

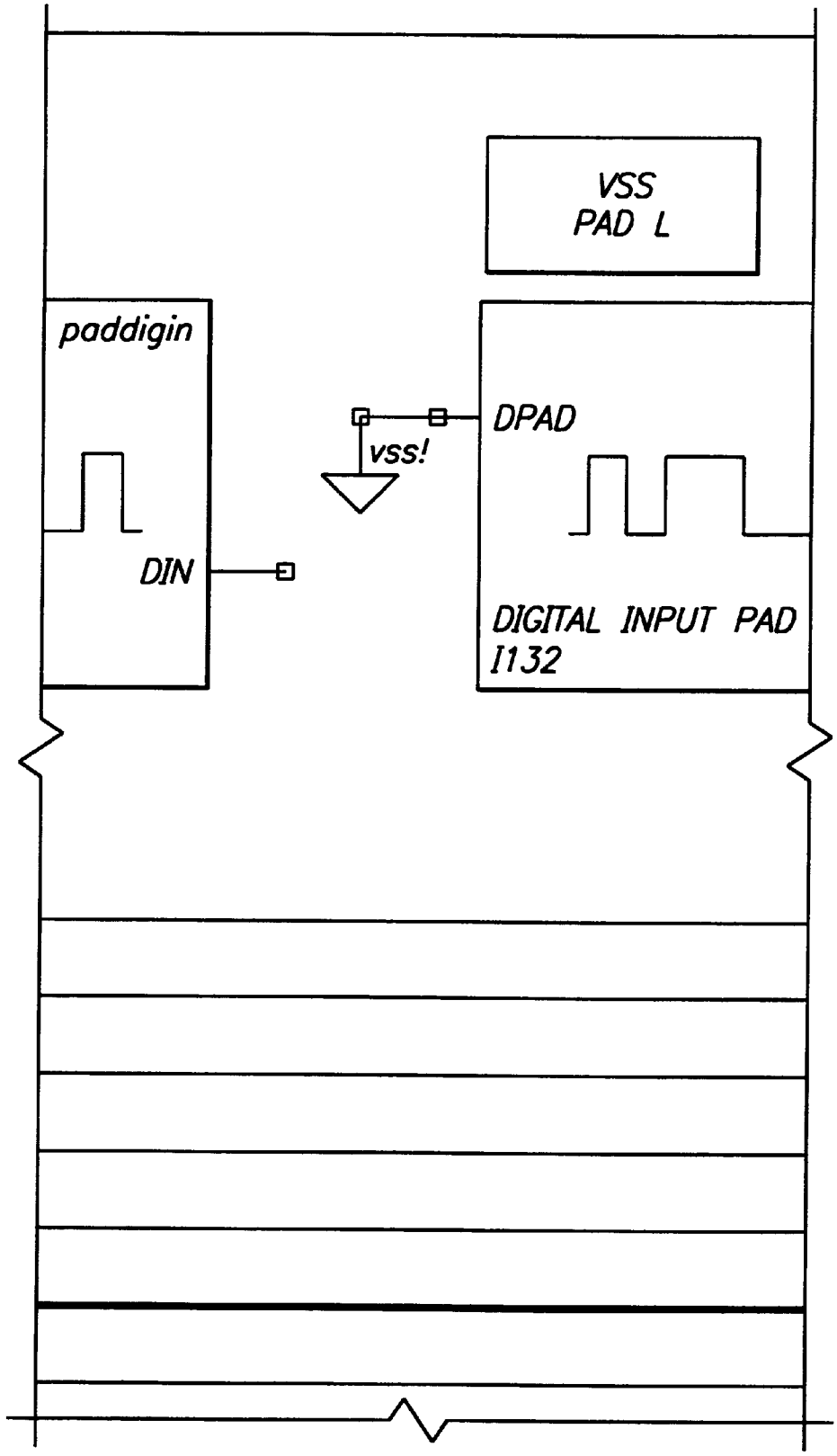


Fig 19AD

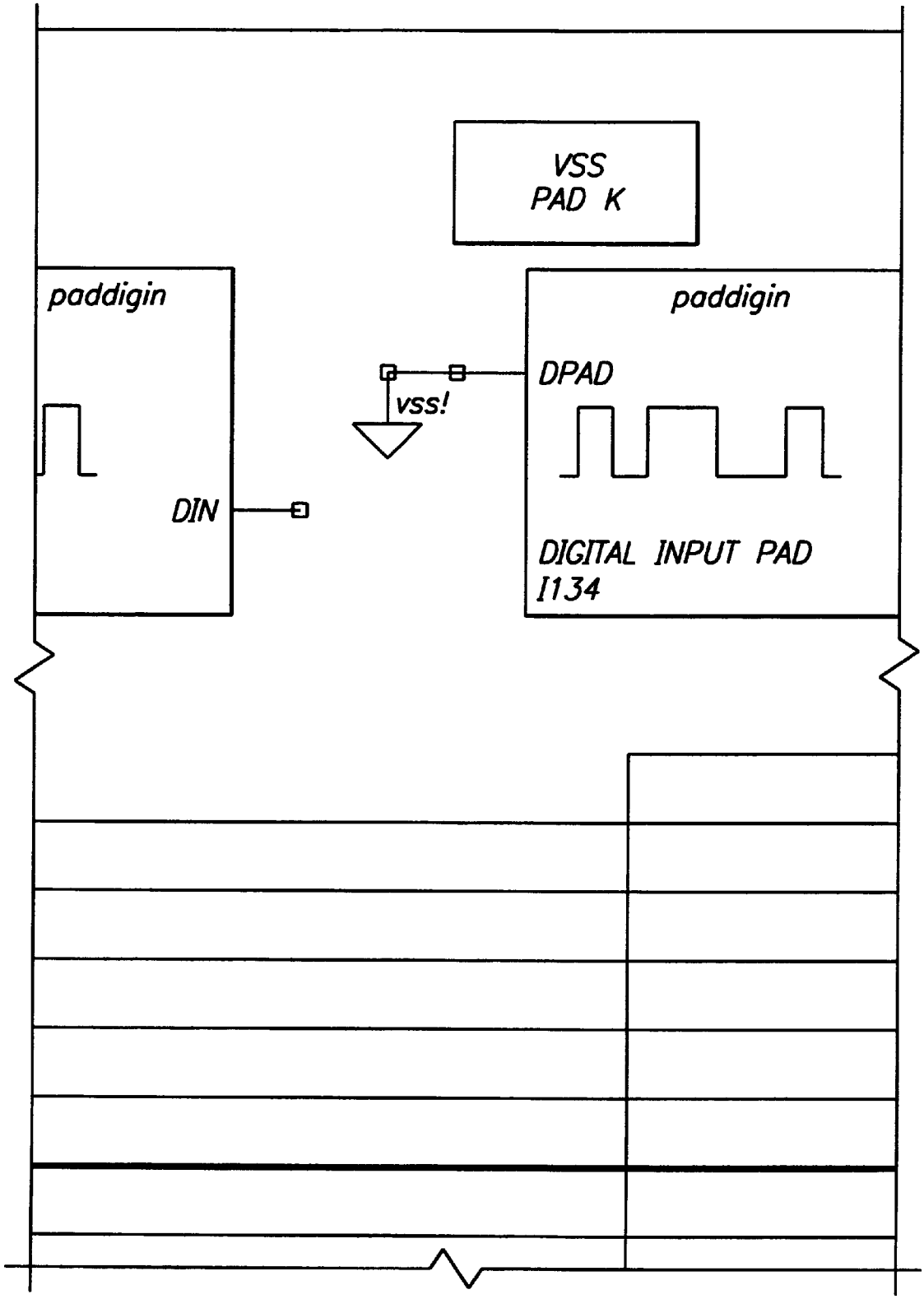

VSS
PAD K
paddigin
DIN
vss!
paddigin
DPAD
DIGITAL INPUT PAD
I134

Fig 19AE

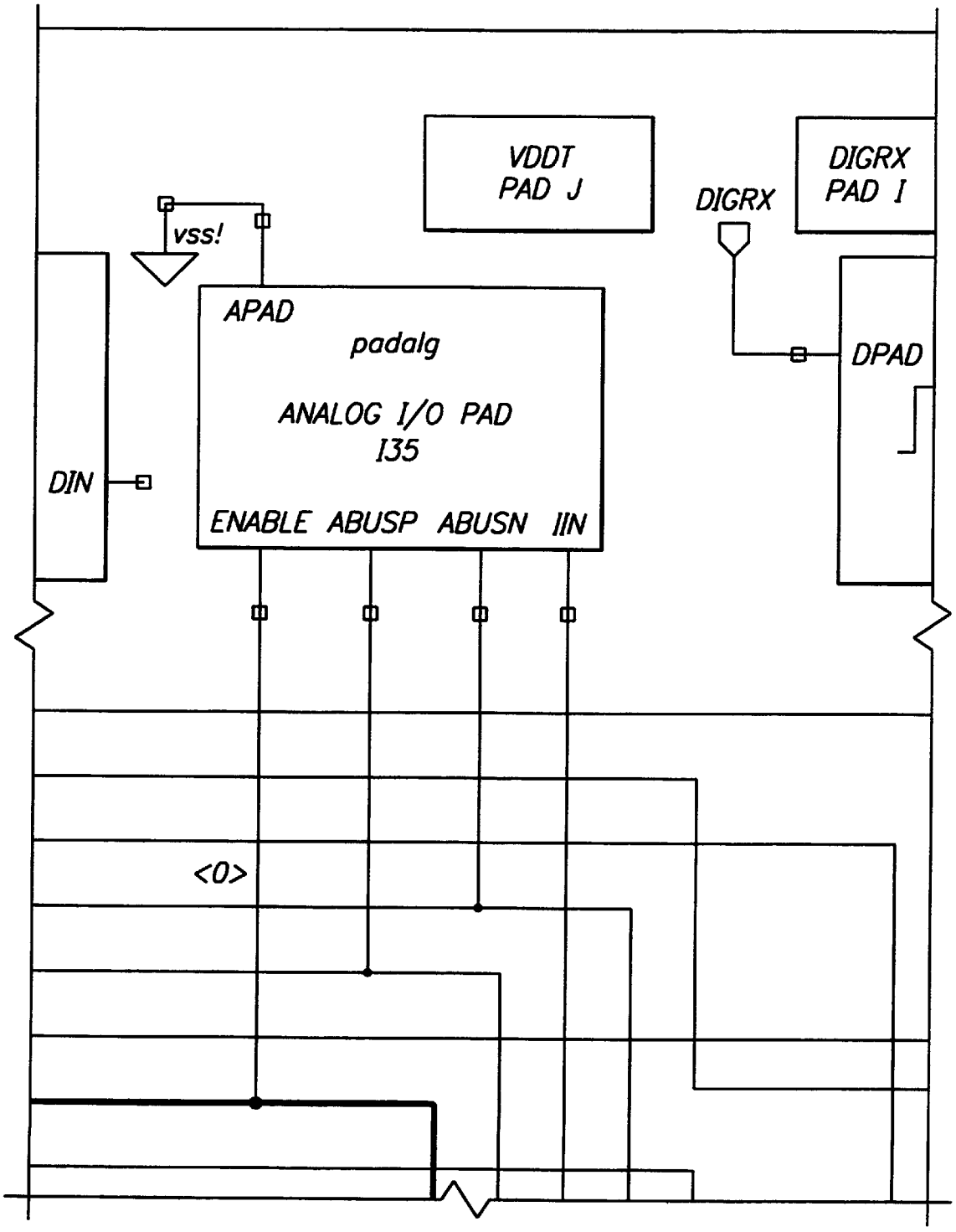

VDDT
PAD J
DIGRX
PAD I
DIGRX
vss!
APAD
padalg
ANALOG I/O PAD
I35
ENABLE ABUSP ABUSN IIN
DPAD
DIN
<0>

Fig 19AF

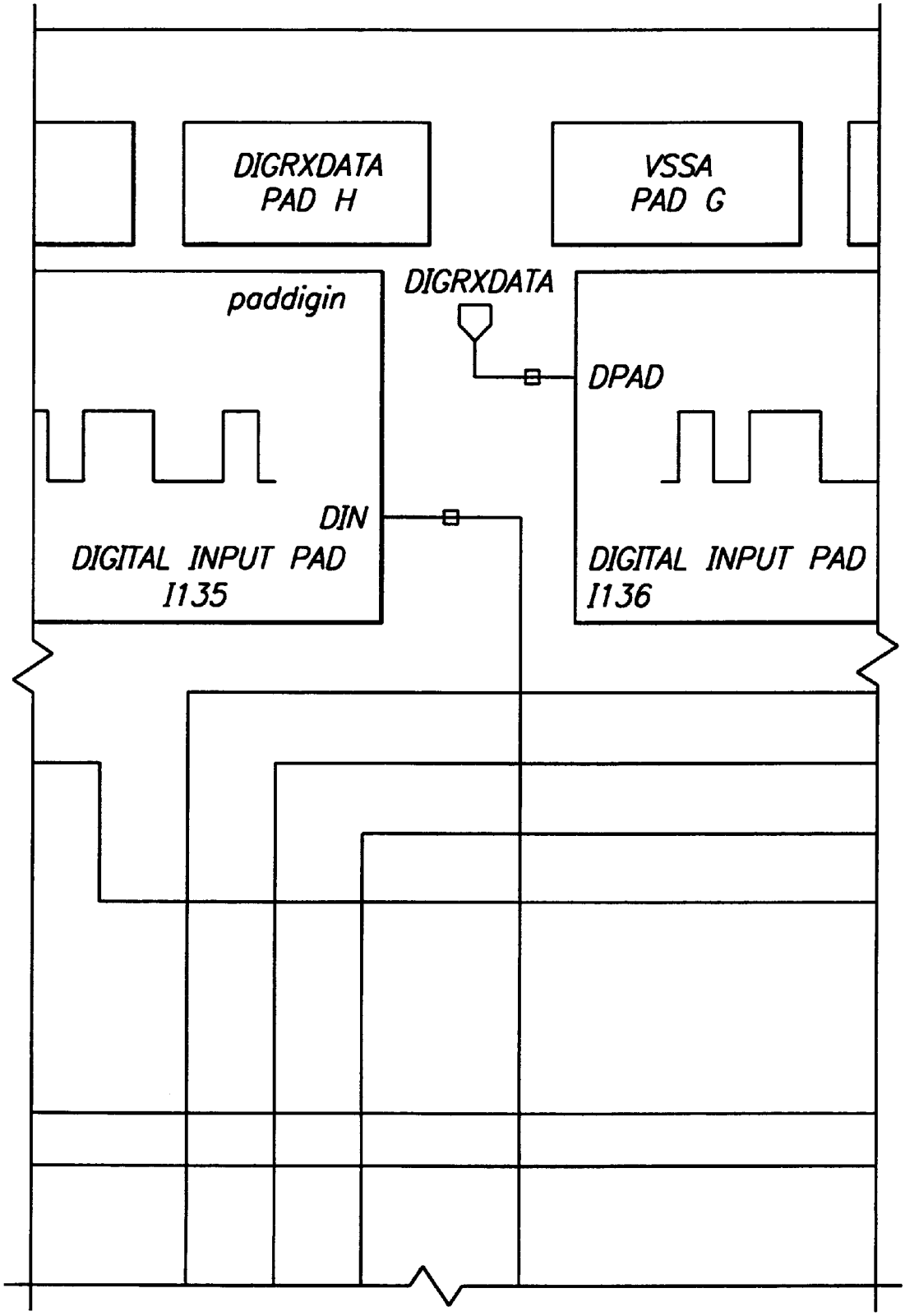

DIGRXDATA
PAD H
VSSA
PAD G
paddigin
DIGRXDATA
DPAD
DIN
DIGITAL INPUT PAD
I135
DIGITAL INPUT PAD
I136

Fig 19AG

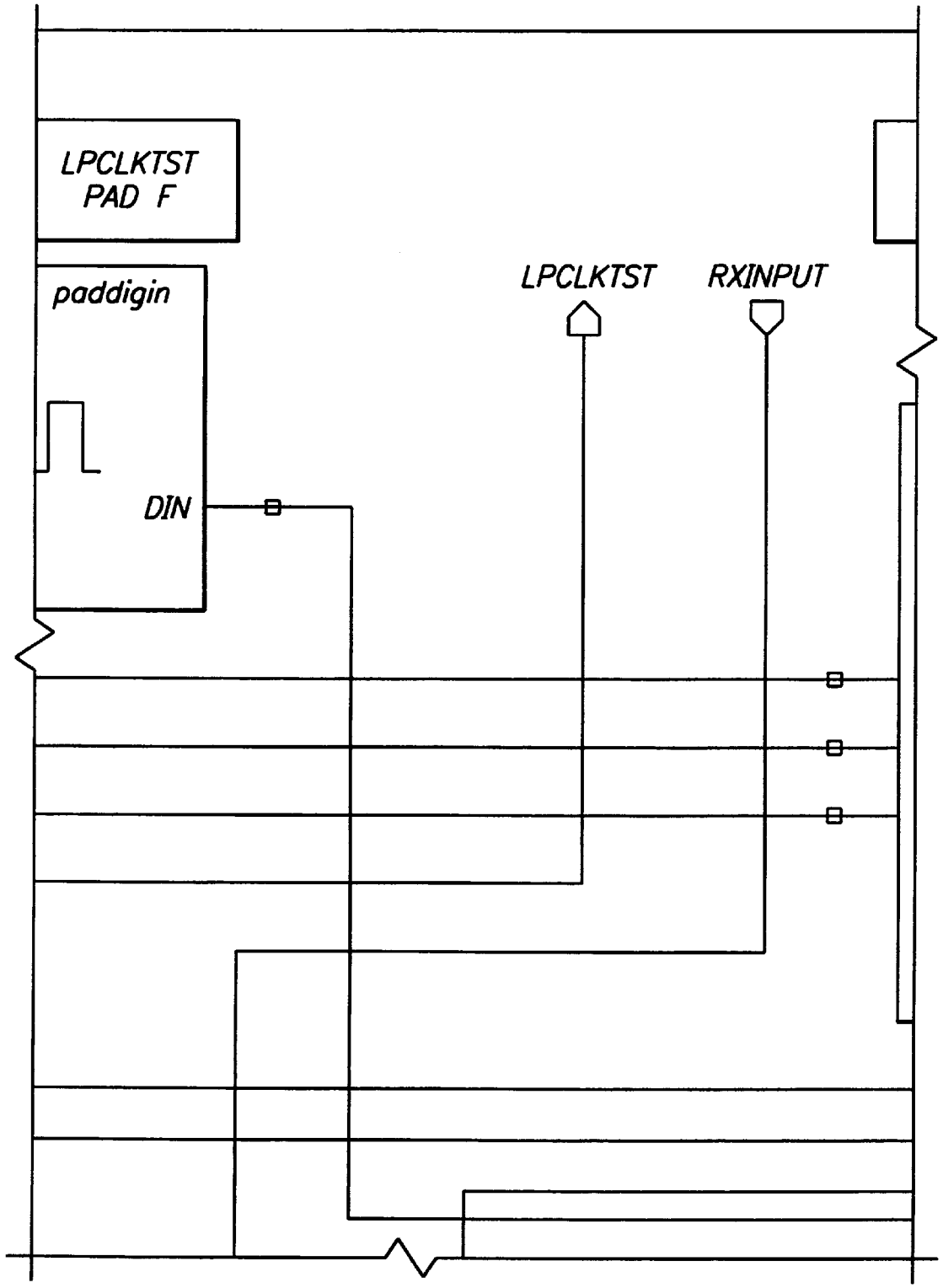


Fig 19AH

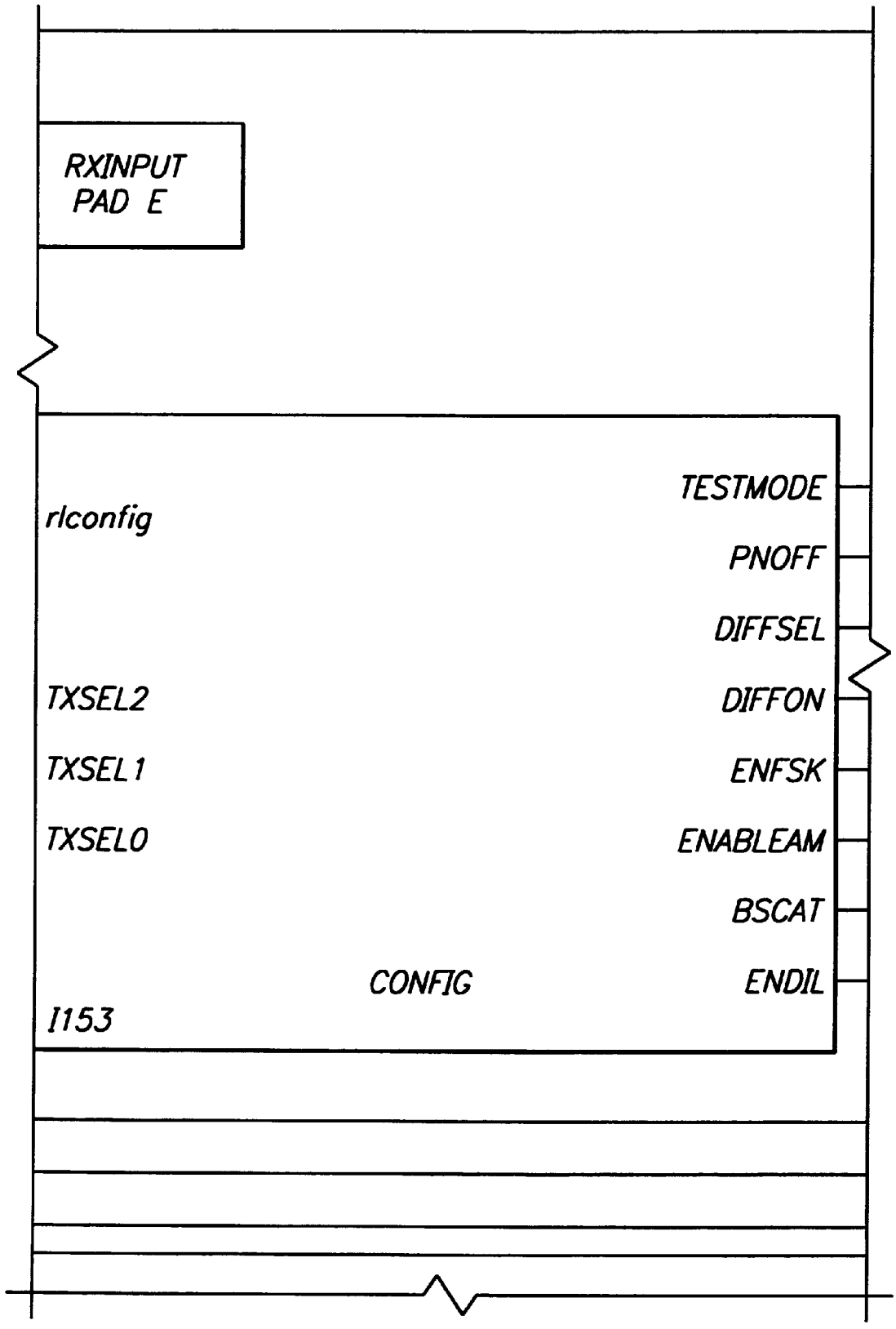

RXINPUT
PAD E
rlconfig
TXSEL2
TXSEL1
TXSEL0
TESTMODE
PNOFF
DIFFSEL
DIFFON
ENFSK
ENABLEAM
BSCAT
ENDIL
CONFIG
I153

Fig 1901

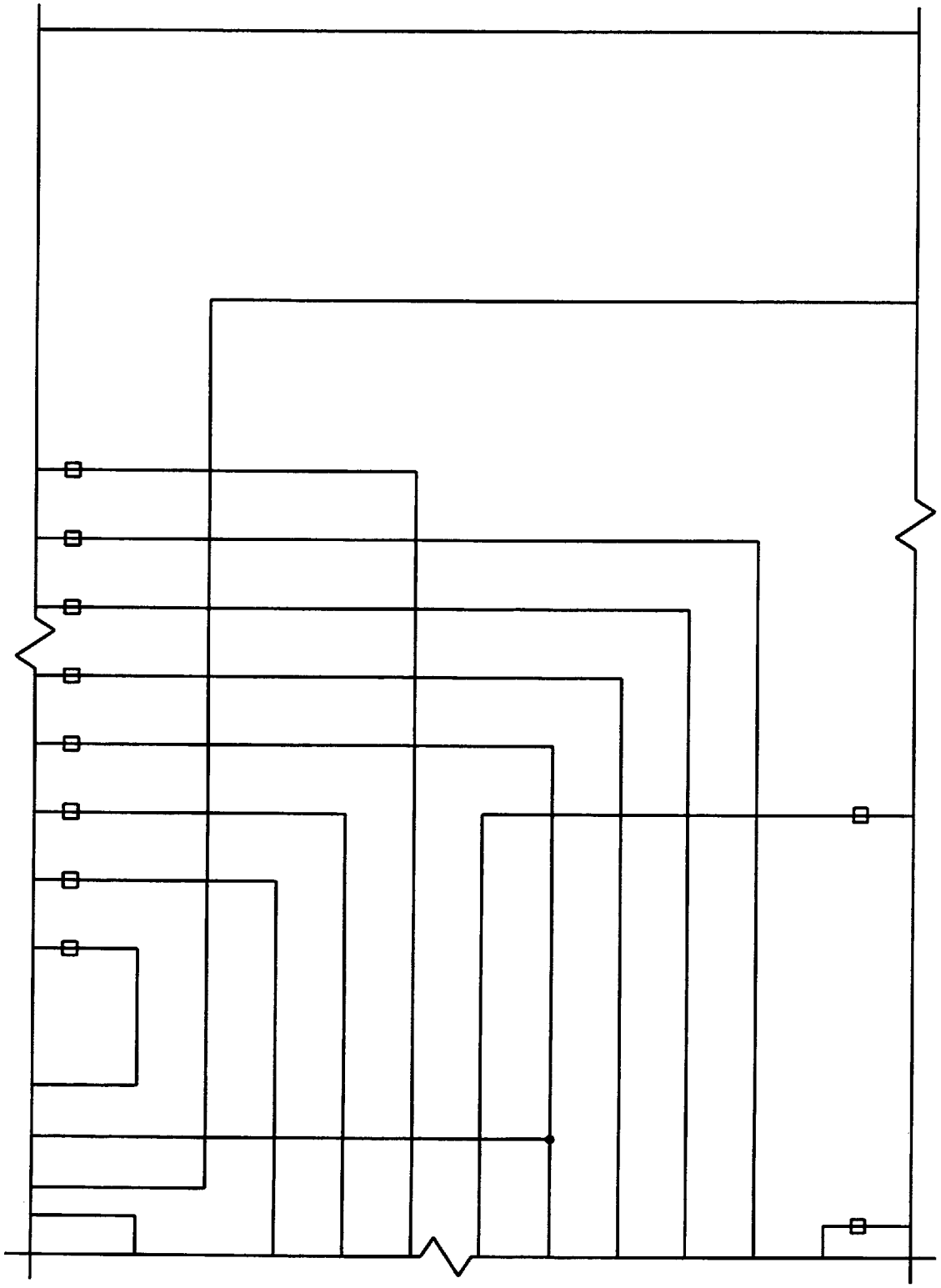


Fig 19Aal

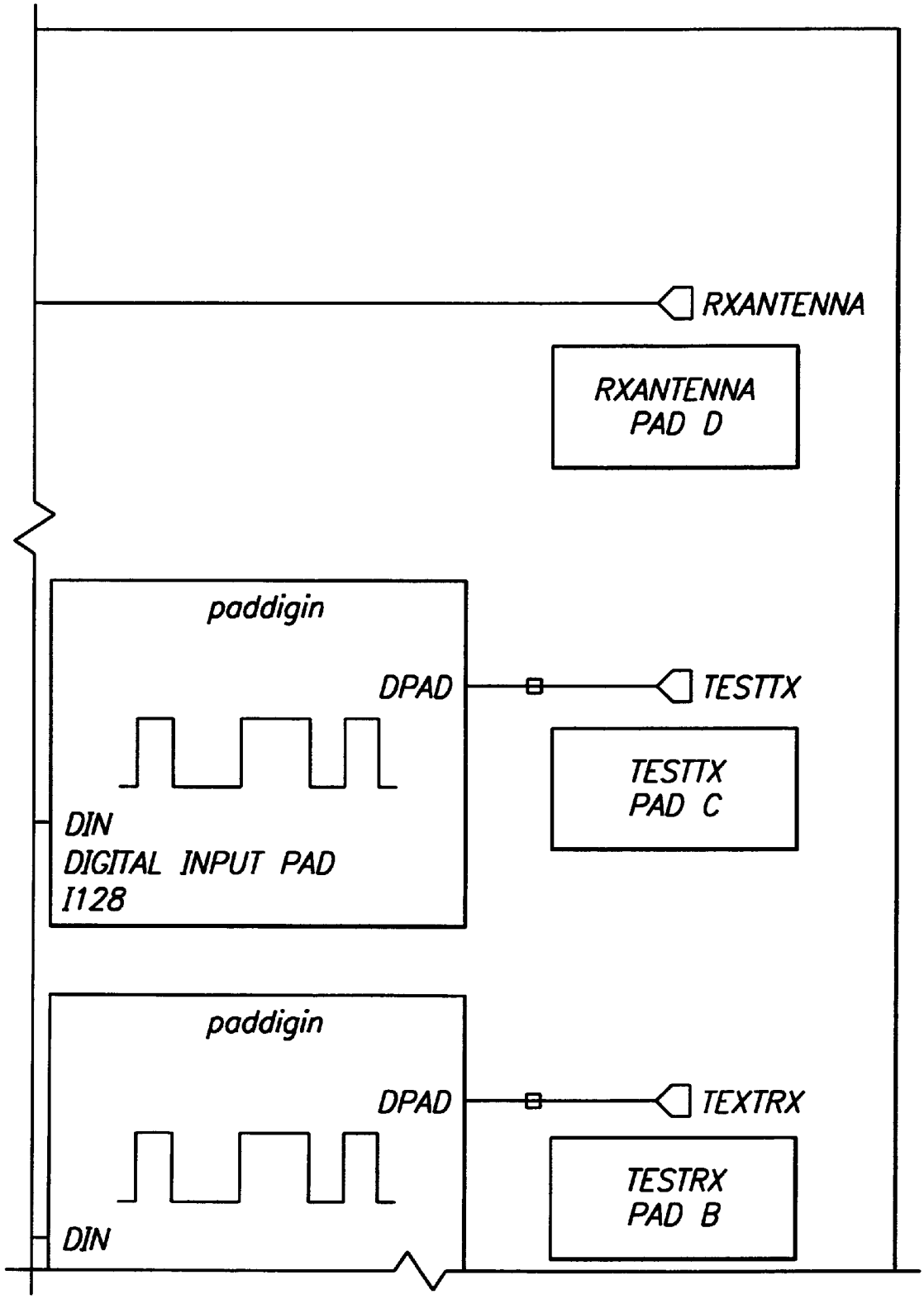

RXANTENNA
RXANTENNA
PAD D
paddigin
DPAD
TESTTX
TESTTX
PAD C
DIN
DIGITAL INPUT PAD
I128
paddigin
DPAD
TEXTRX
TESTRX
PAD B
DIN

Fig 19AK

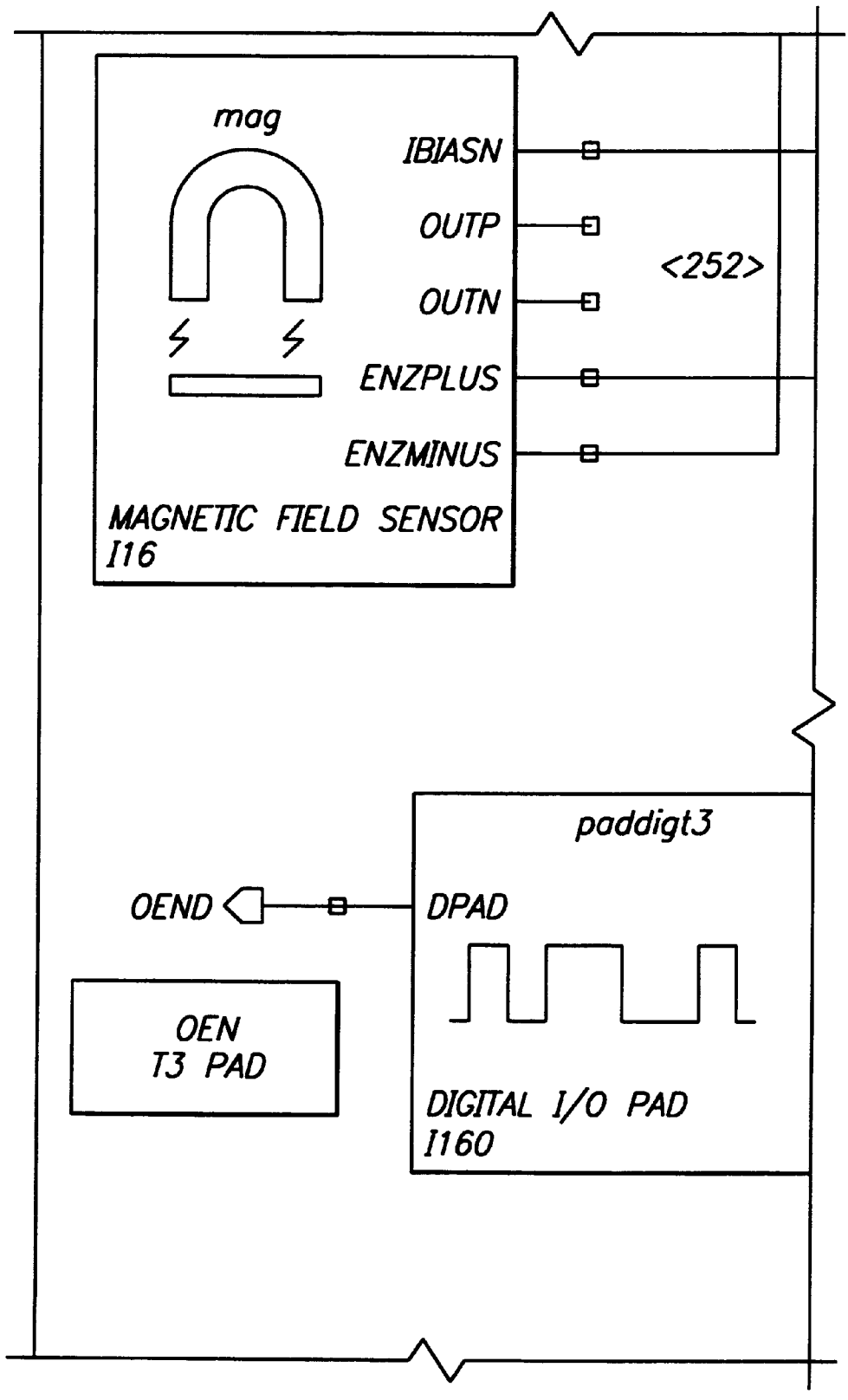

mag
IBIASN
OUTP
OUTN
ENZPLUS
ENZMINUS
<252>
MAGNETIC FIELD SENSOR
I16
paddigt3
OEND
DPAD
OEN
T3 PAD
DIGITAL I/O PAD
I160

Fig 19BA

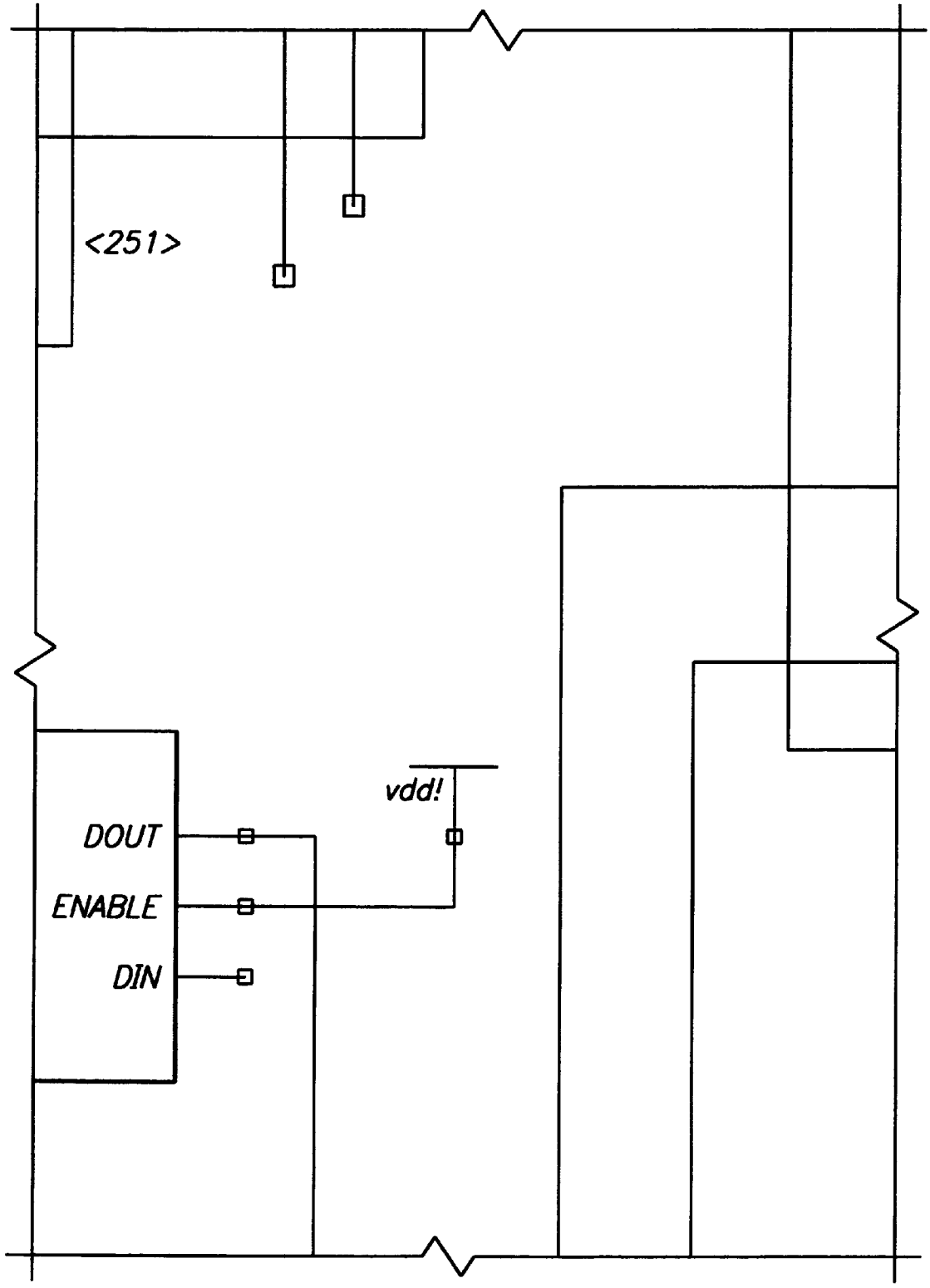


Fig 19BB

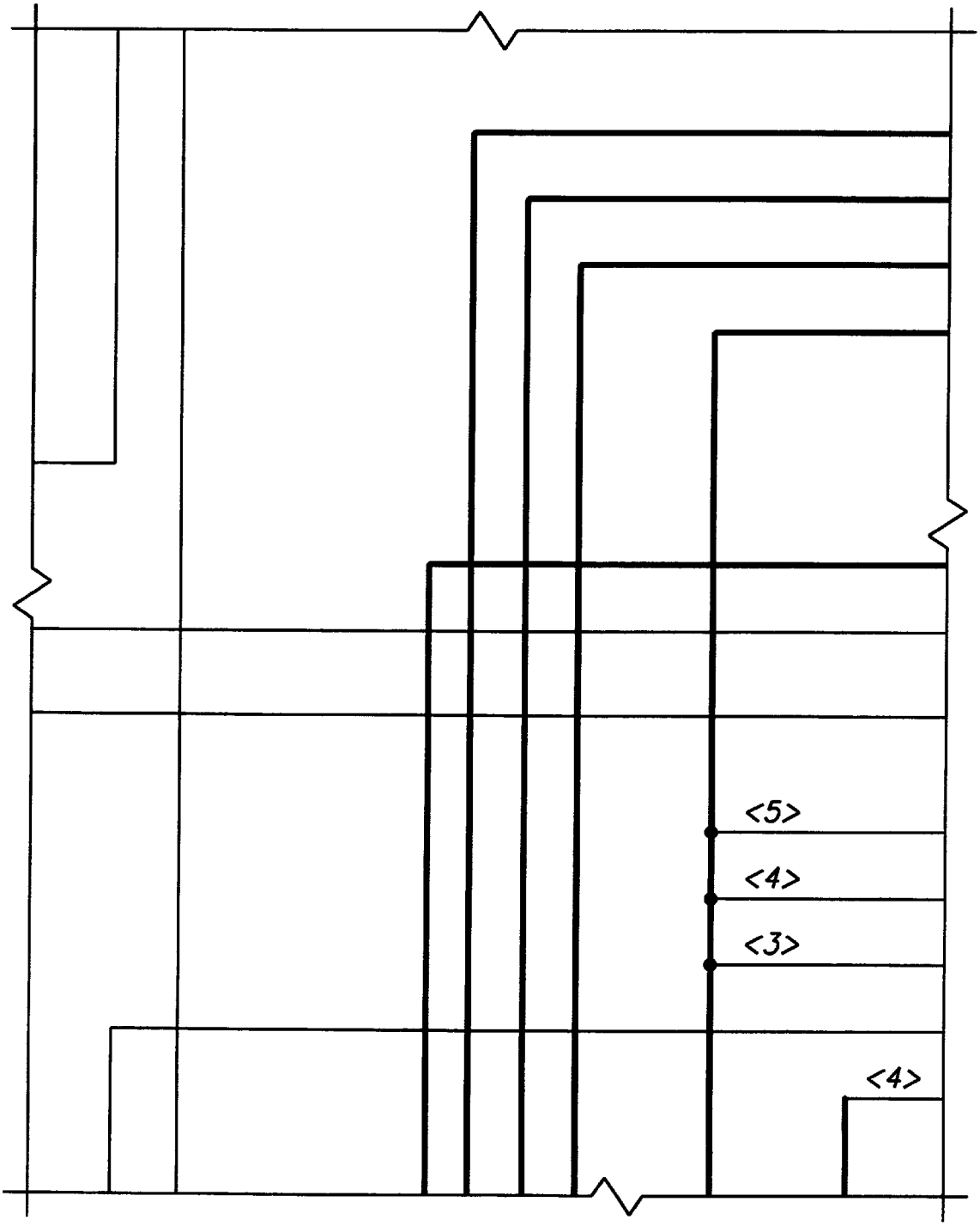


Fig 19BC

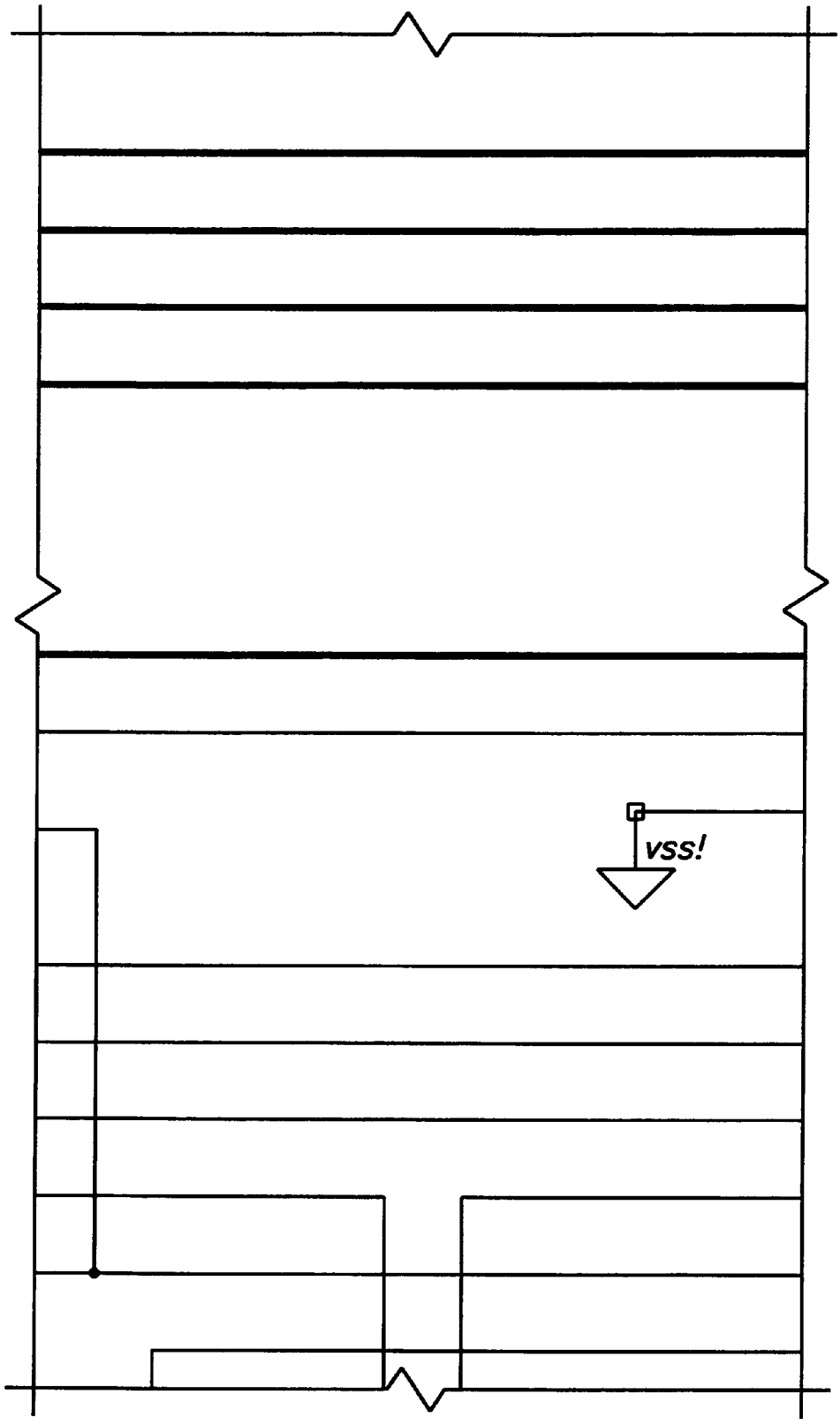


Fig 19BD

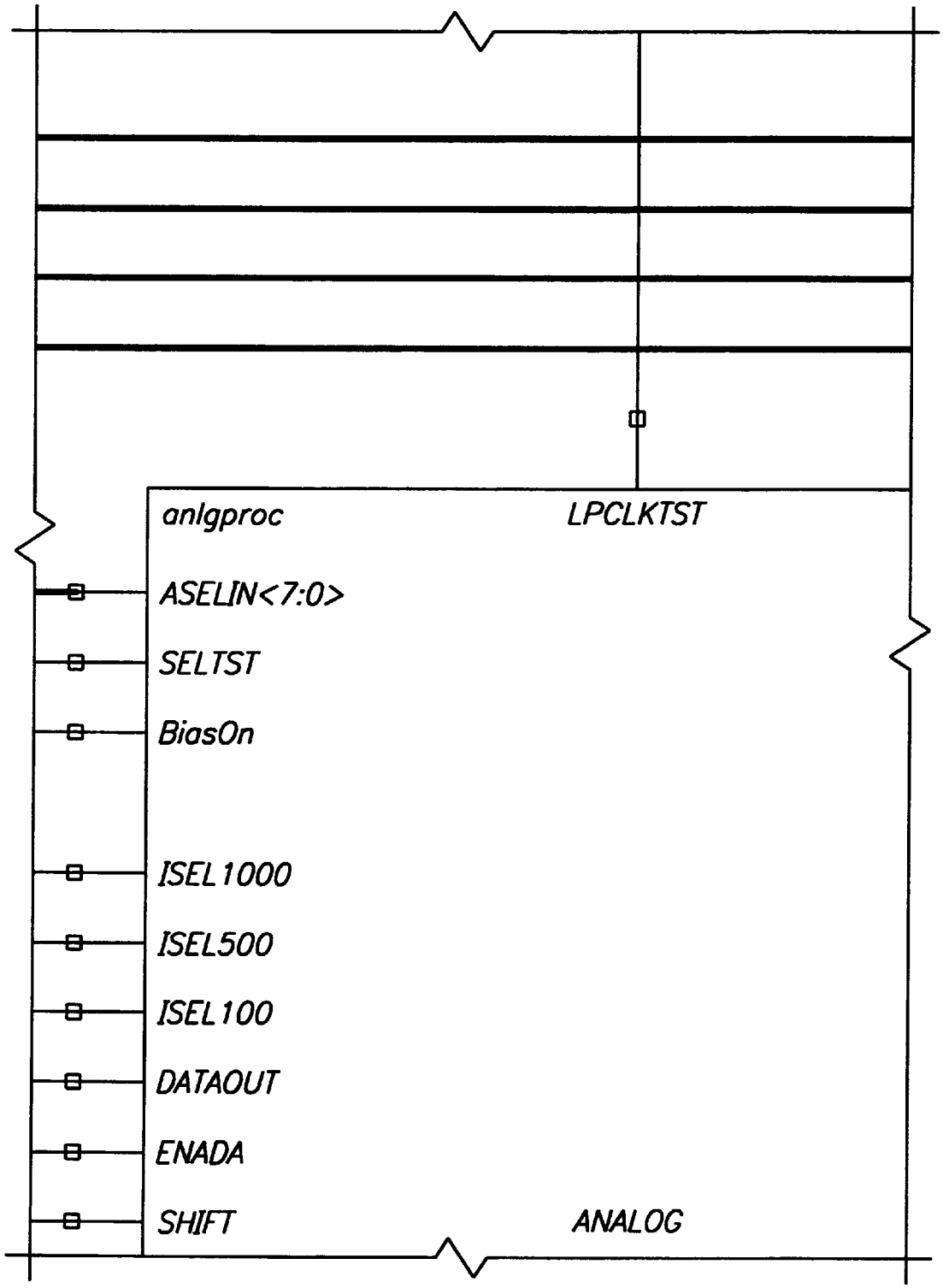

anlgproc
LPCLKTST
ASELIN<7:0>
SELTST
BiasOn
ISEL1000
ISEL500
ISEL100
DATAOUT
ENADA
SHIFT
ANALOG

Fig 19BE

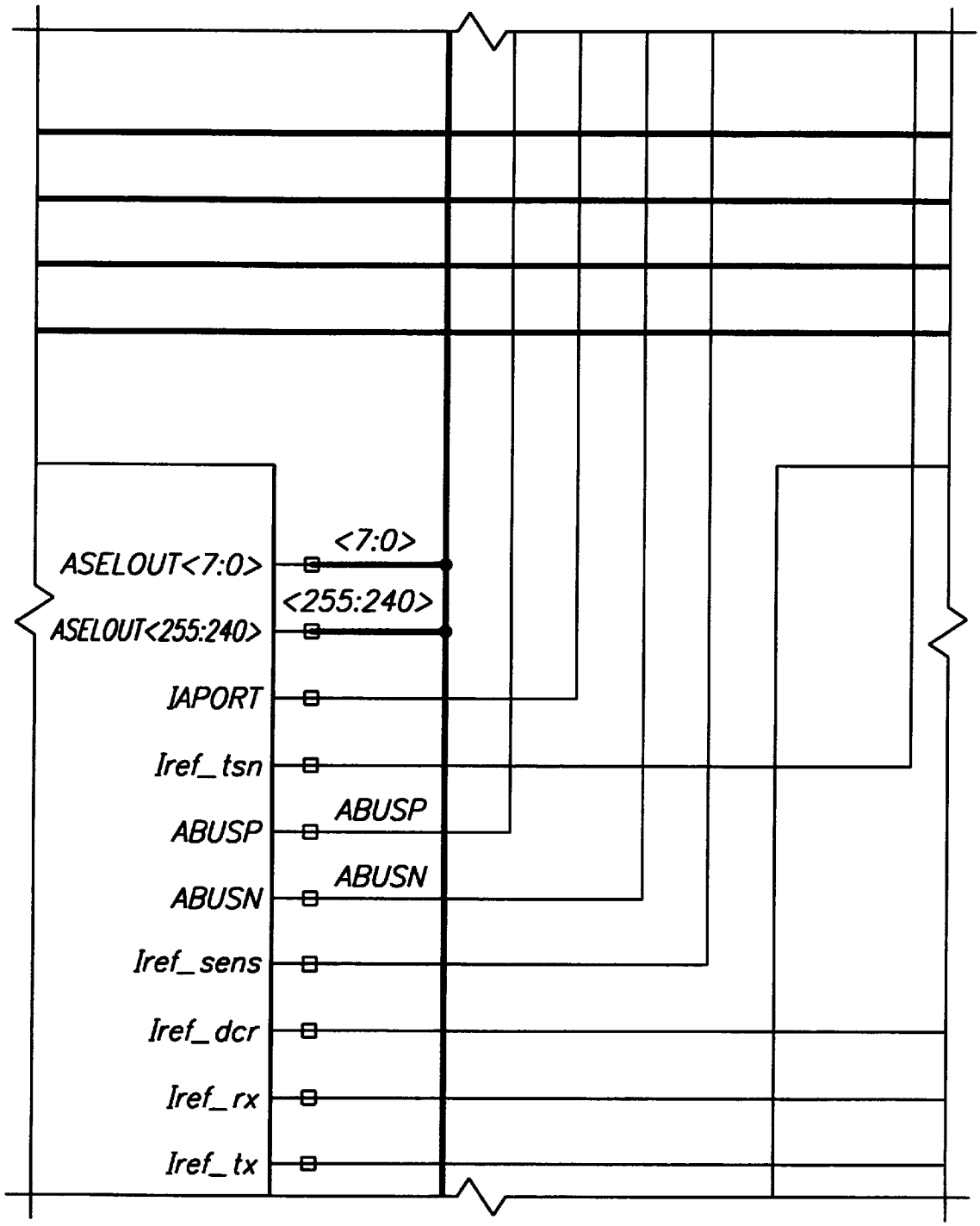

<7:0>
ASELOUT<7:0>
<255:240>
ASELOUT<255:240>
IAPORT
Iref_tsn
ABUSP
ABUSP
ABUSN
ABUSN
Iref_sens
Iref_dcr
Iref_rx
Iref_tx

Fig 198F

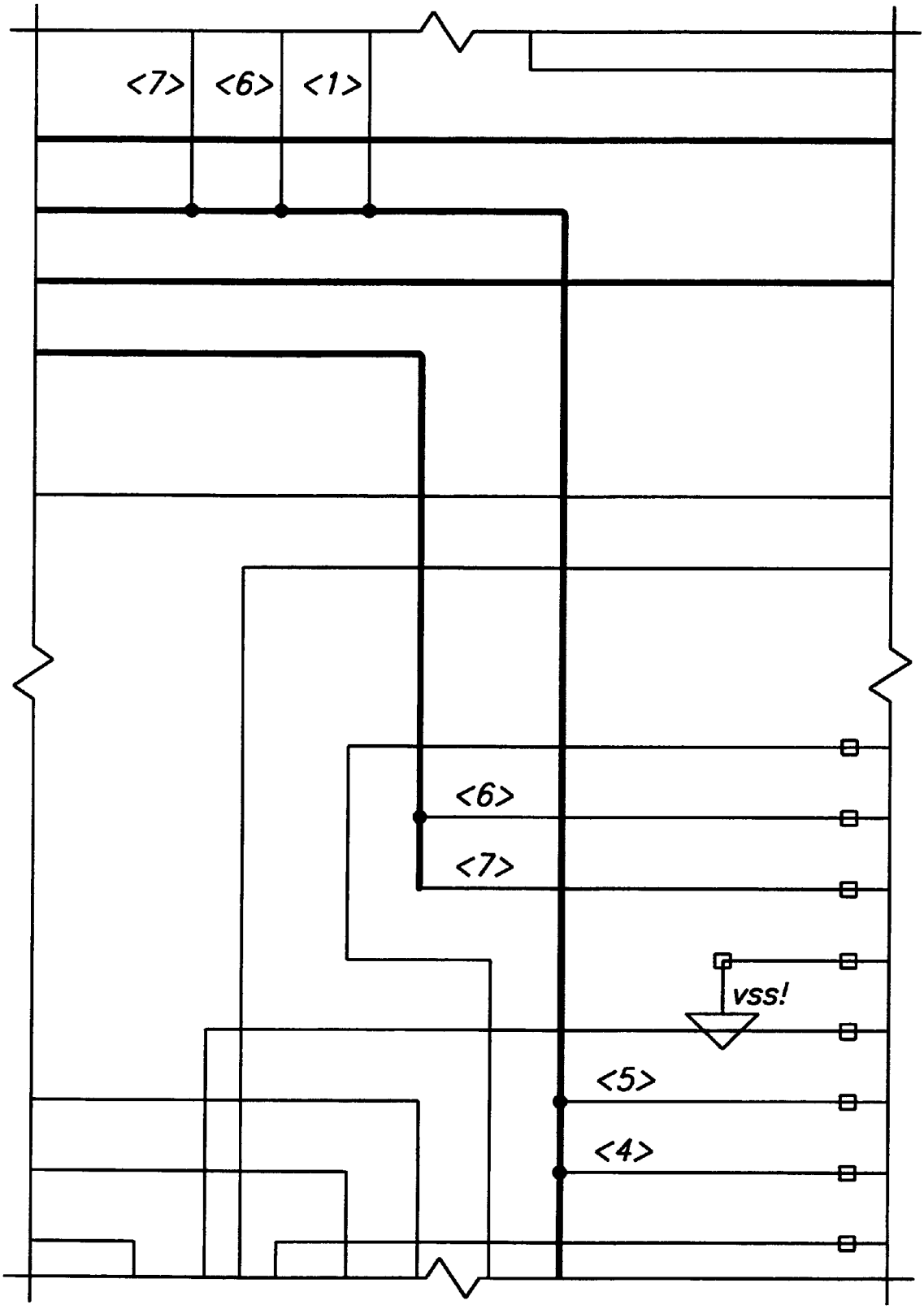


Fig 198G

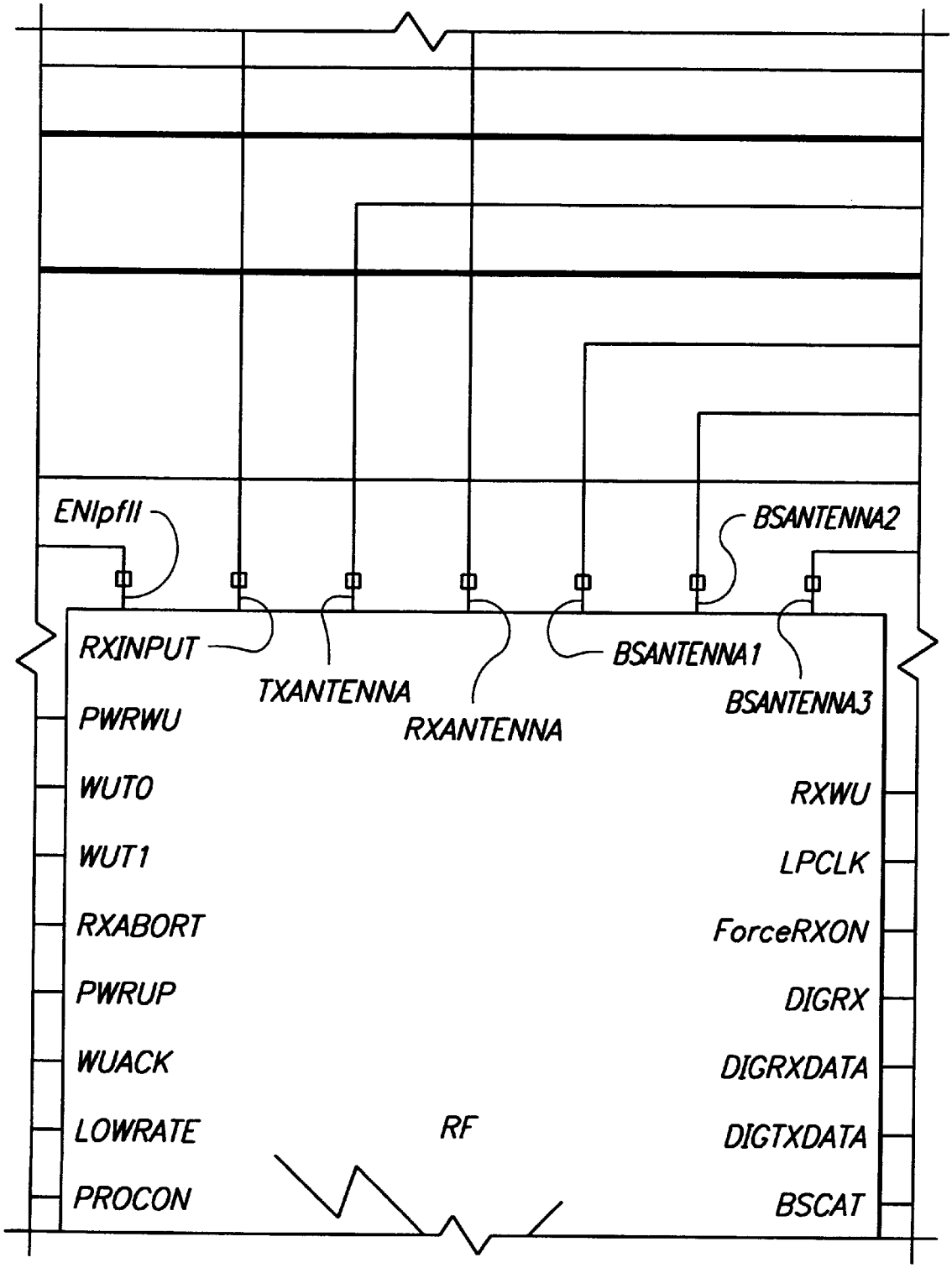

ENIpfII
BSANTENNA2
RXINPUT
TXANTENNA
RXANTENNA
BSANTENNA1
BSANTENNA3
PWRWU
WUT0
WUT1
RXABORT
PWRUP
WUACK
LOWRATE
PROCON
RF
RXWU
LPCLK
ForceRXON
DIGRX
DIGRXDATA
DIGTXDATA
BSCAT

Fig 19BH

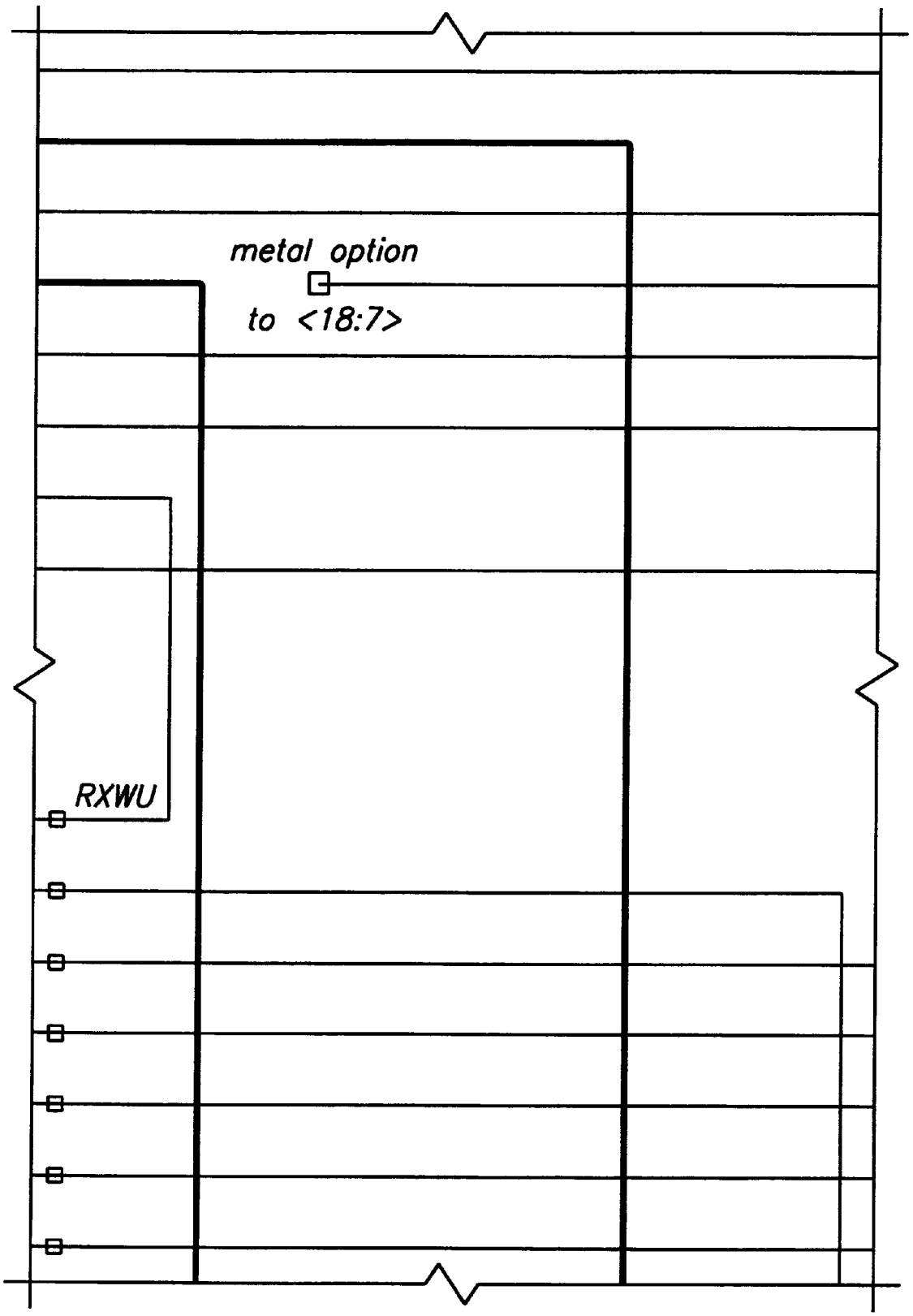


Fig 19BII

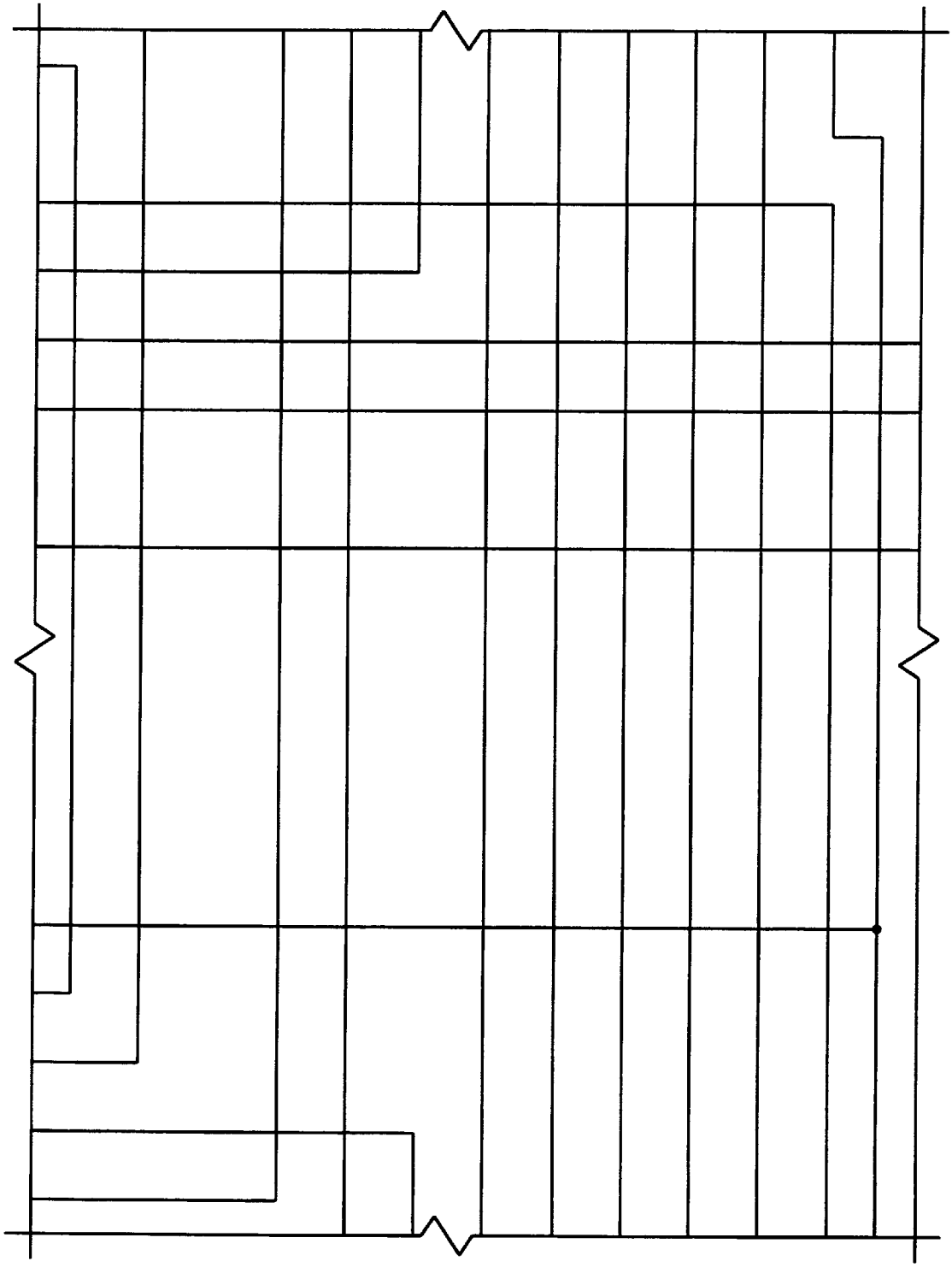


Fig 19Bal

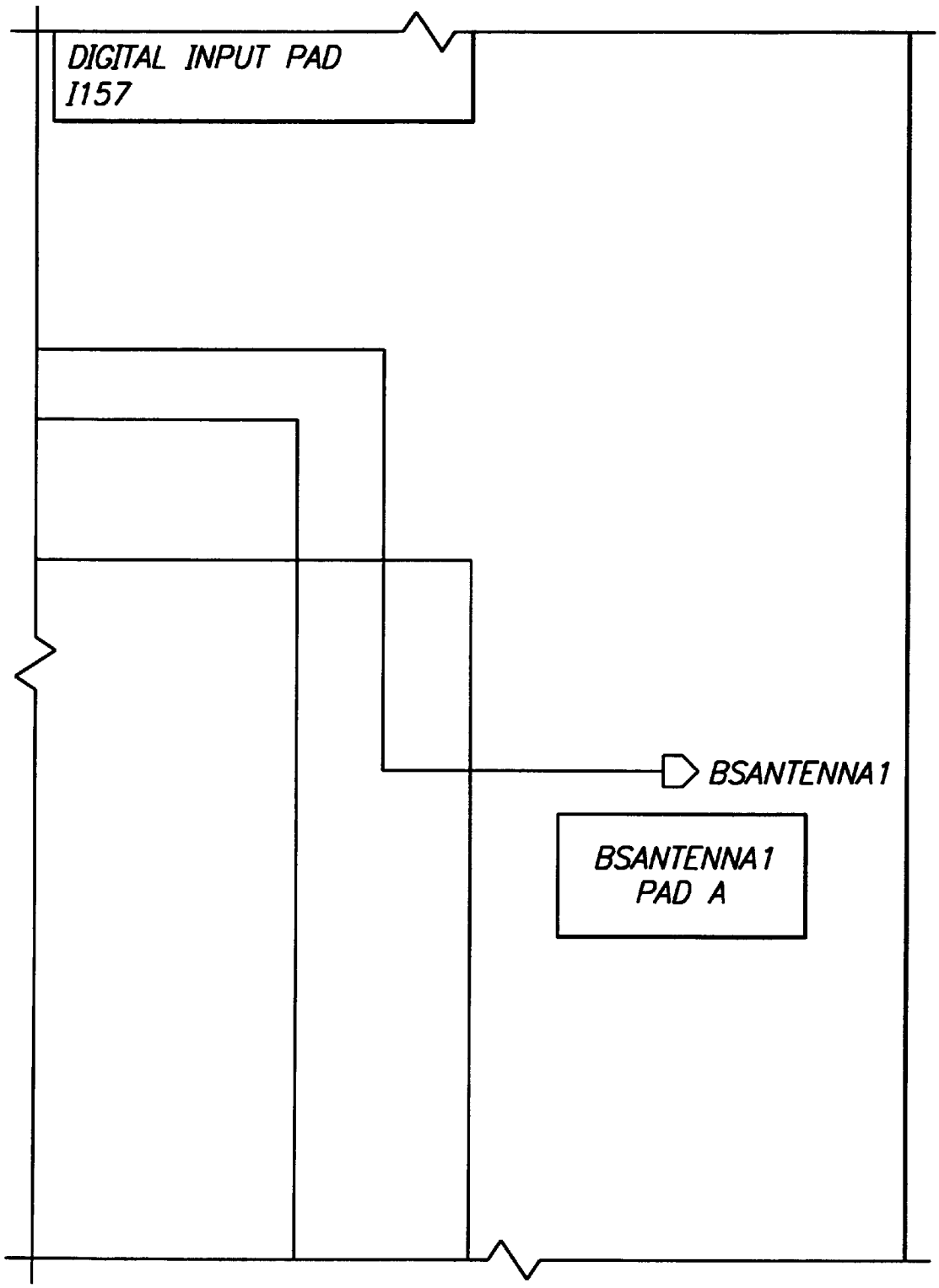


Fig 19BK

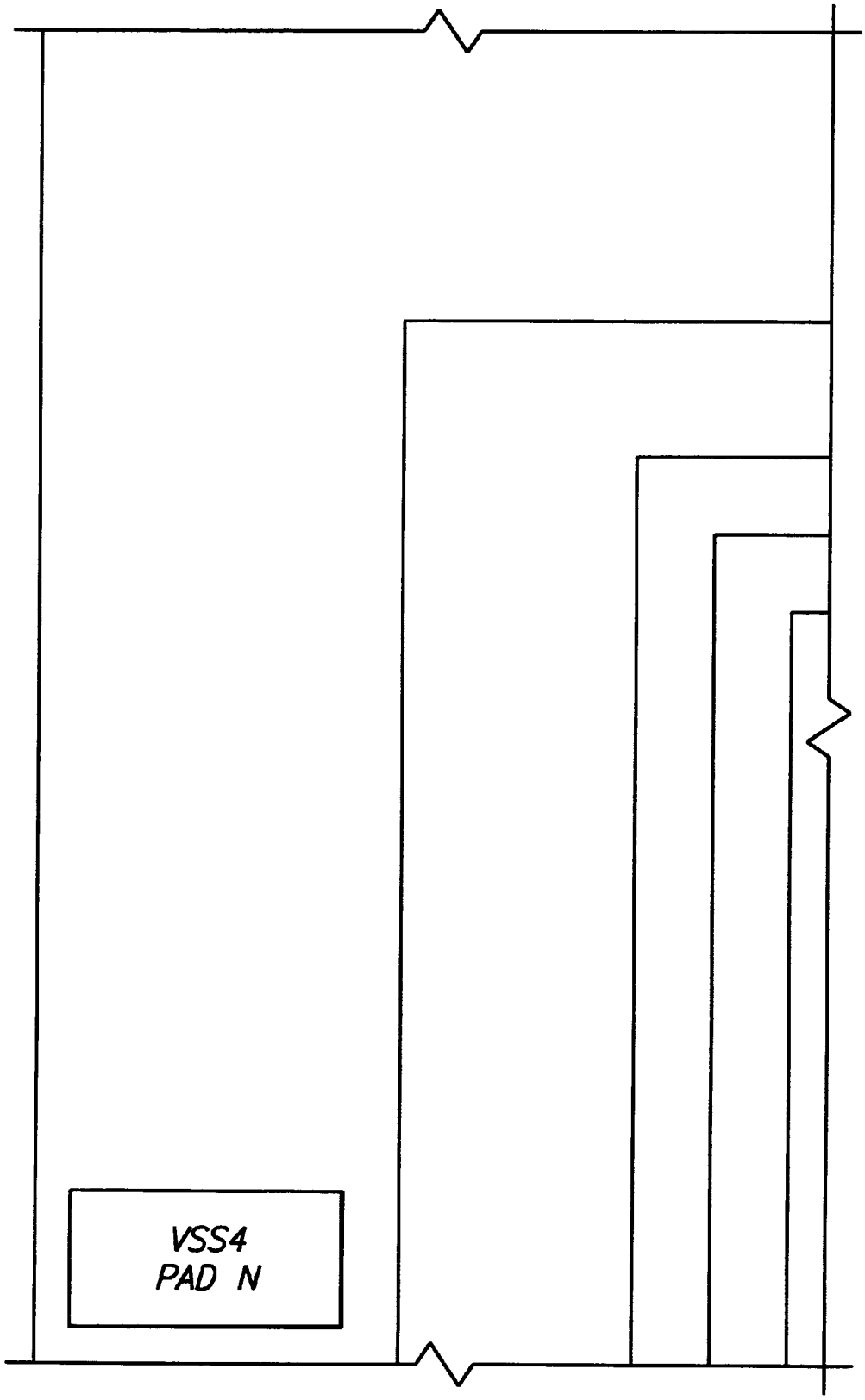


Fig 19CA

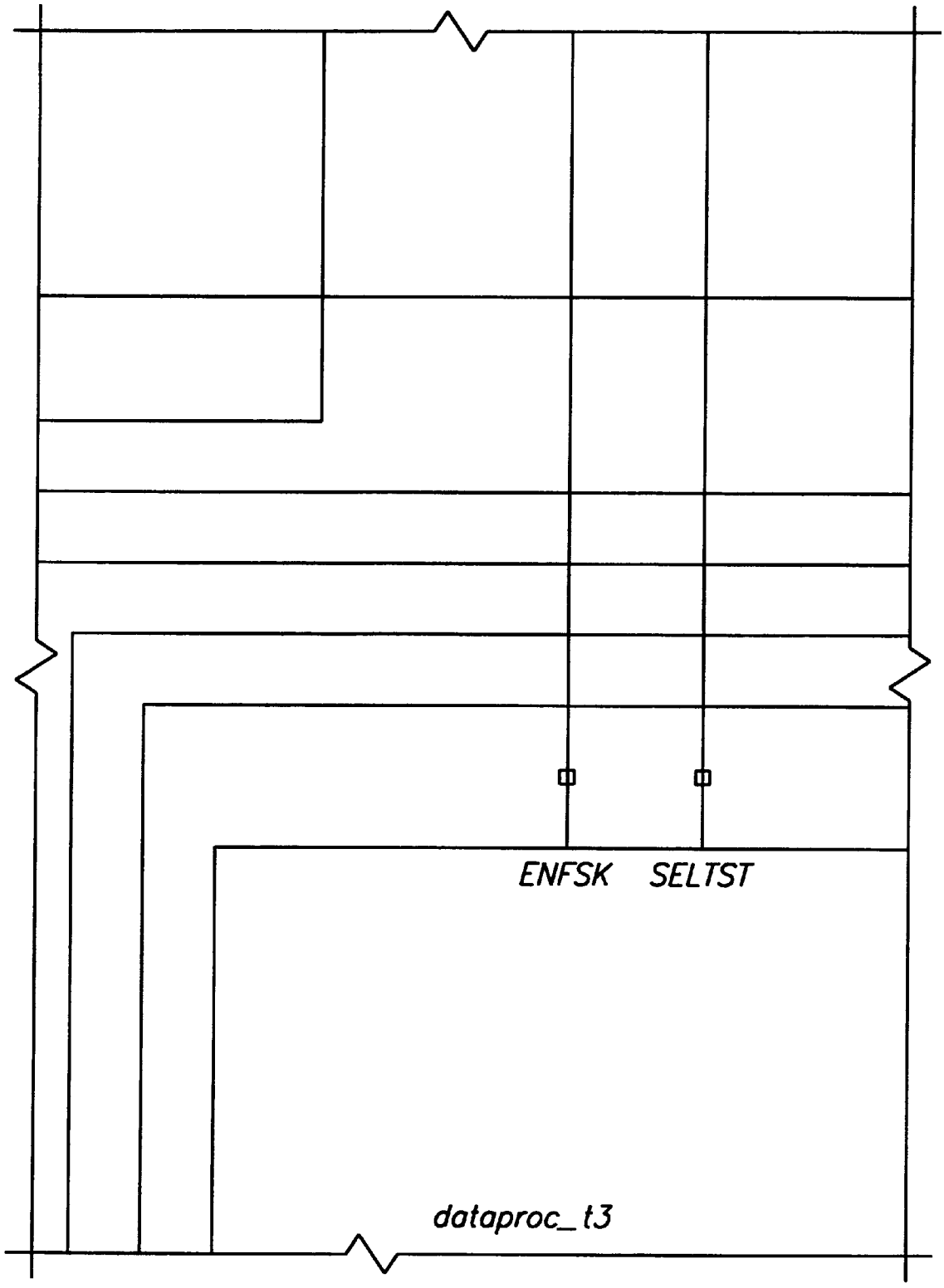


Fig 19CB

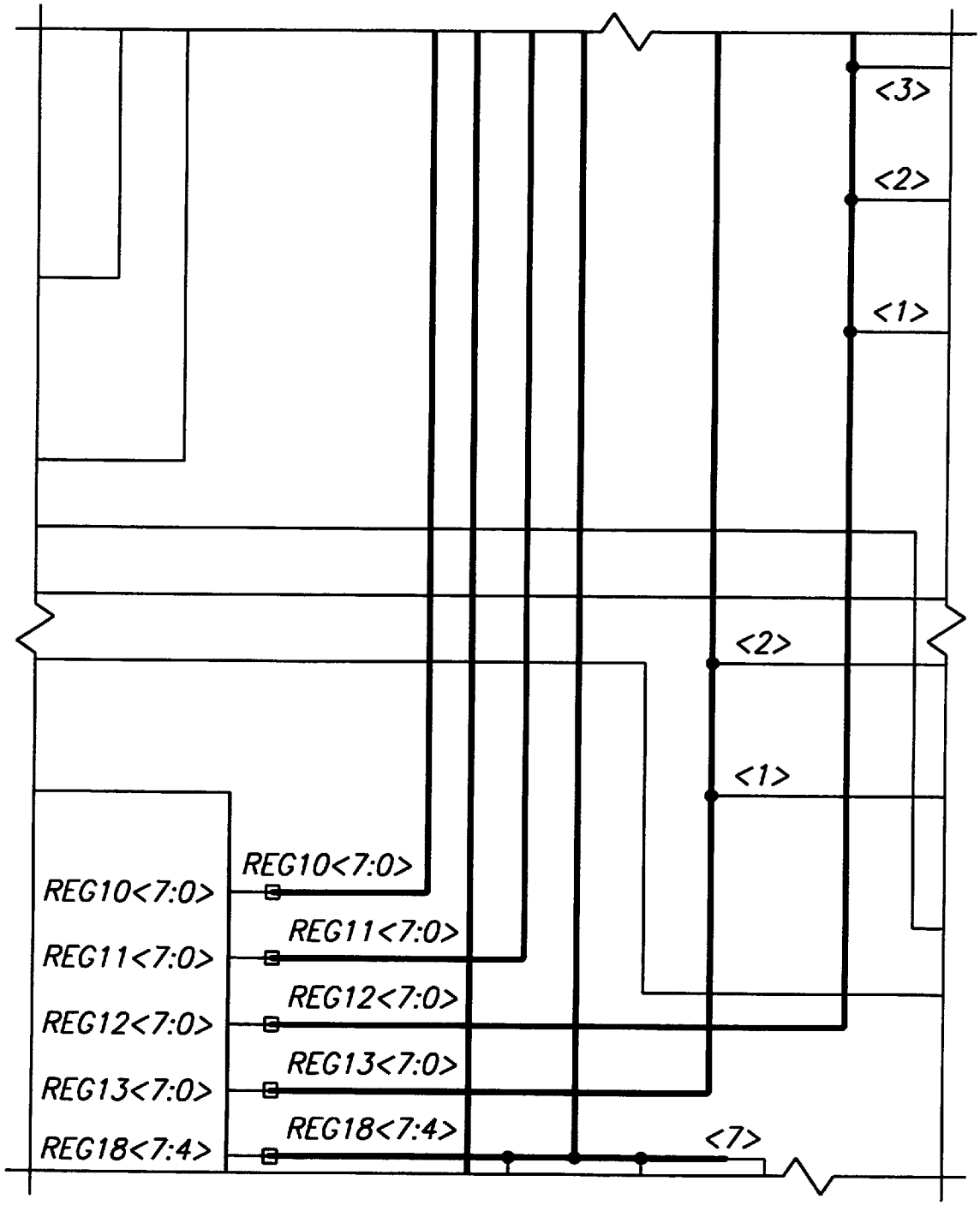

<3>
<2>
<1>
<2>
<1>
REG10<7:0>
REG10<7:0>
REG11<7:0>
REG11<7:0>
REG12<7:0>
REG12<7:0>
REG13<7:0>
REG13<7:0>
REG18<7:4>
REG18<7:4>
<7>

Fig 19CC

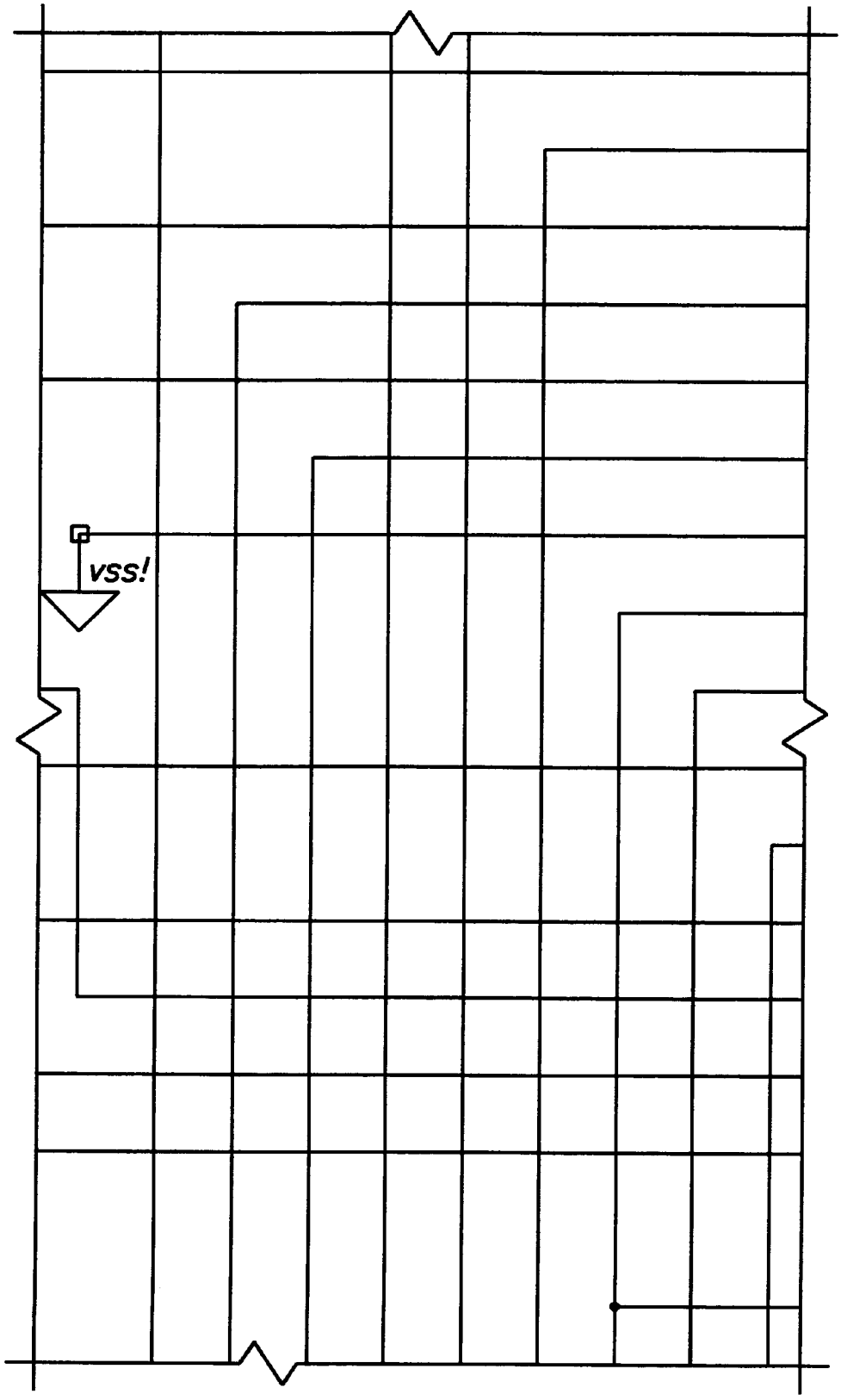


Fig 19CD

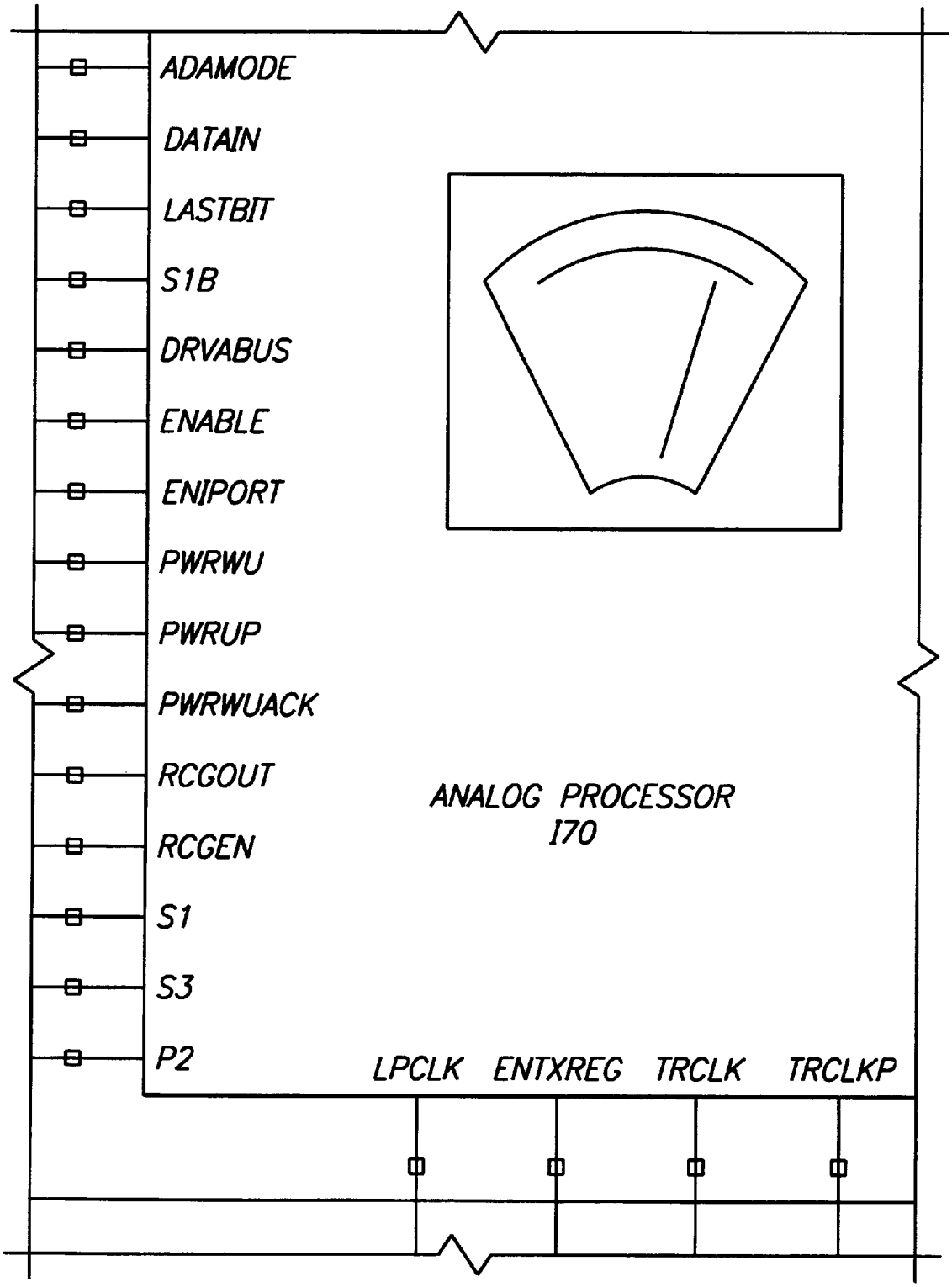

ADAMODE
DATAIN
LASTBIT
S1B
DRVABUS
ENABLE
ENIPORT
PWRWU
PWRUP
PWRWUACK
RCGOUT
RCGEN
S1
S3
P2
ANALOG PROCESSOR
I70
LPCLK
ENTXREG
TRCLK
TRCLKP

Fig 19CE

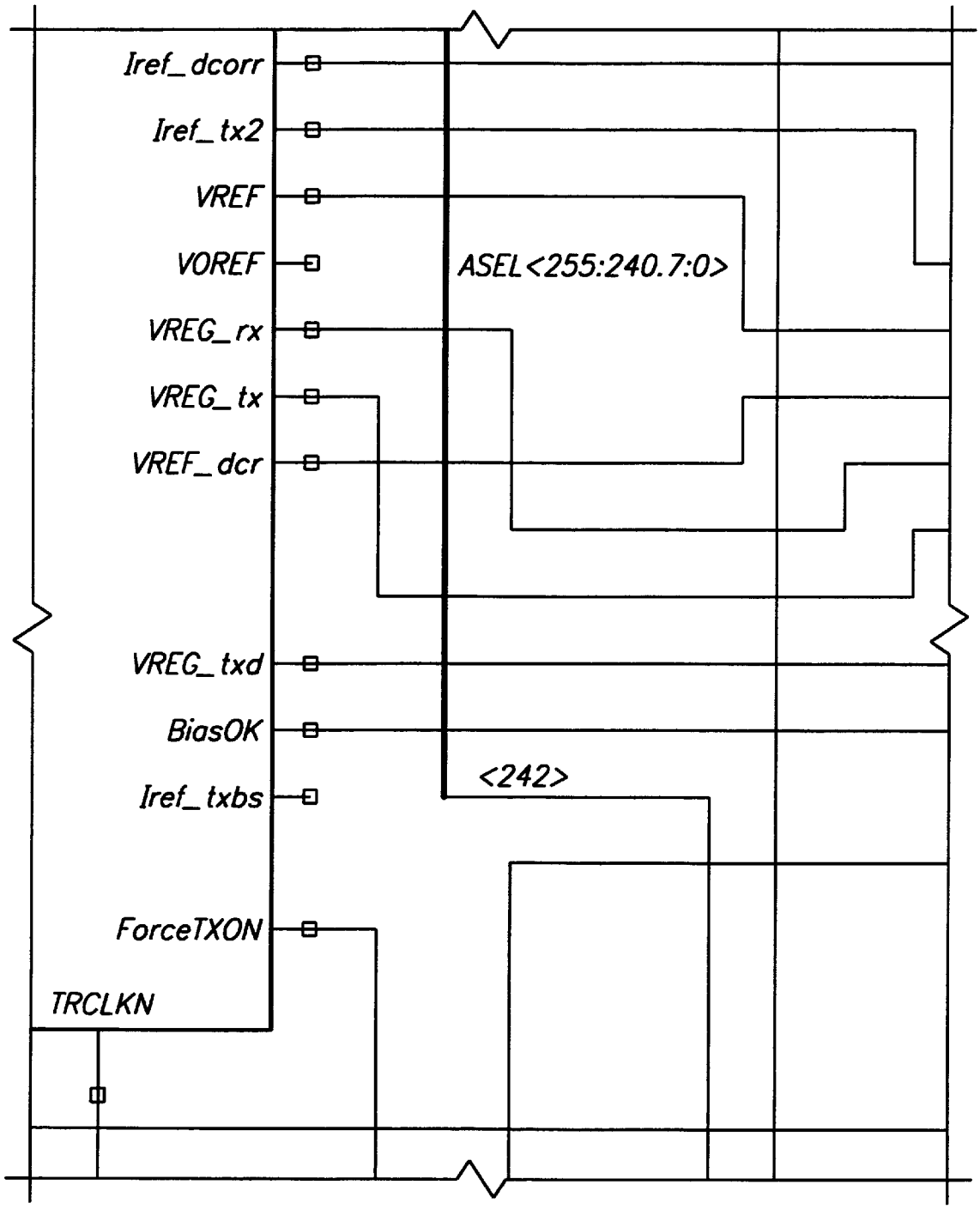

Iref_dcorr
Iref_tx2
VREF
VOREF
VREG_rx
VREG_tx
VREF_dcr
VREG_txd
BiasOK
Iref_txbs
ForceTXON
TRCLKN
ASEL<255:240.7:0>
<242>

Fig 19CF

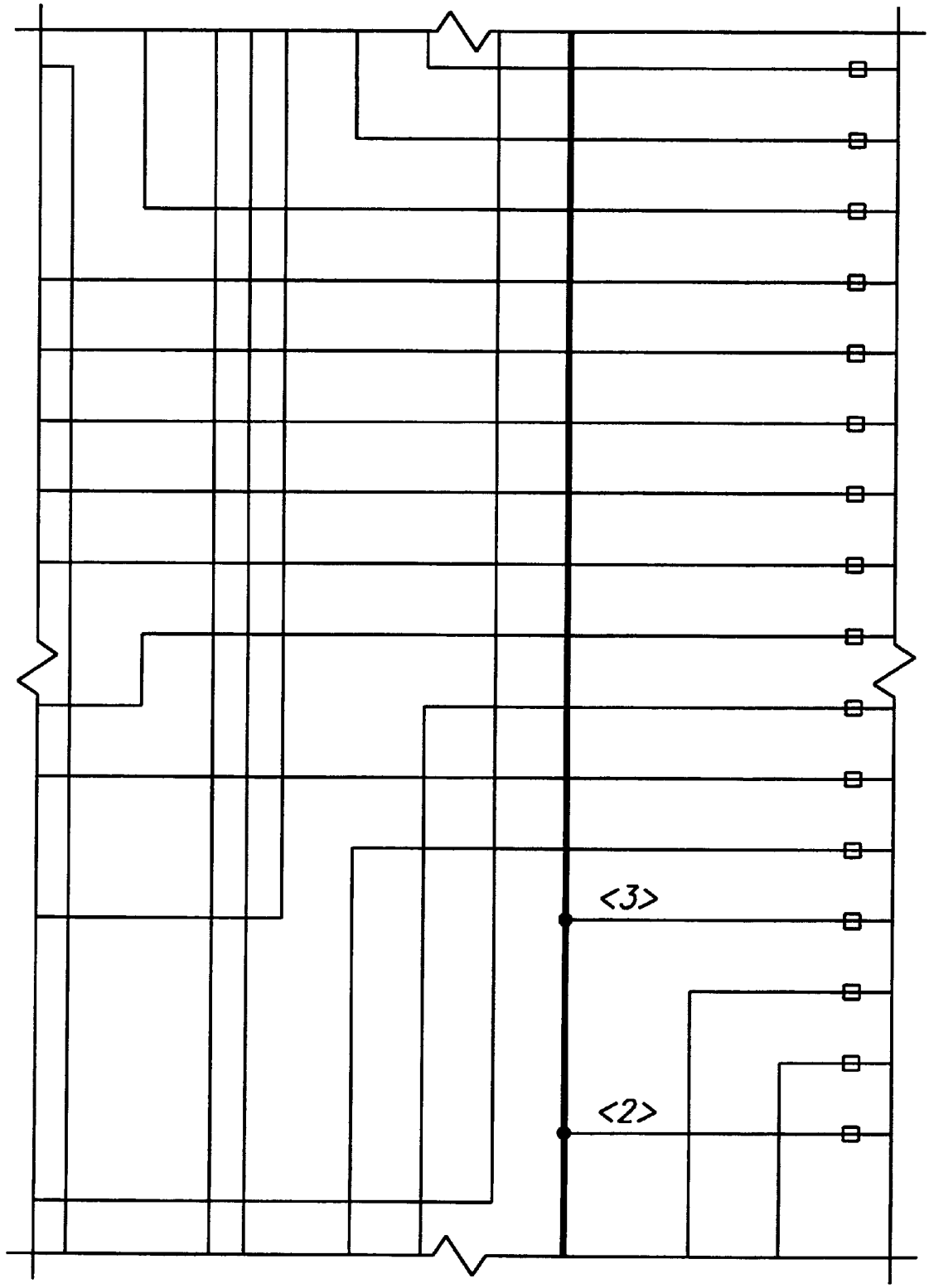


Fig 19CG

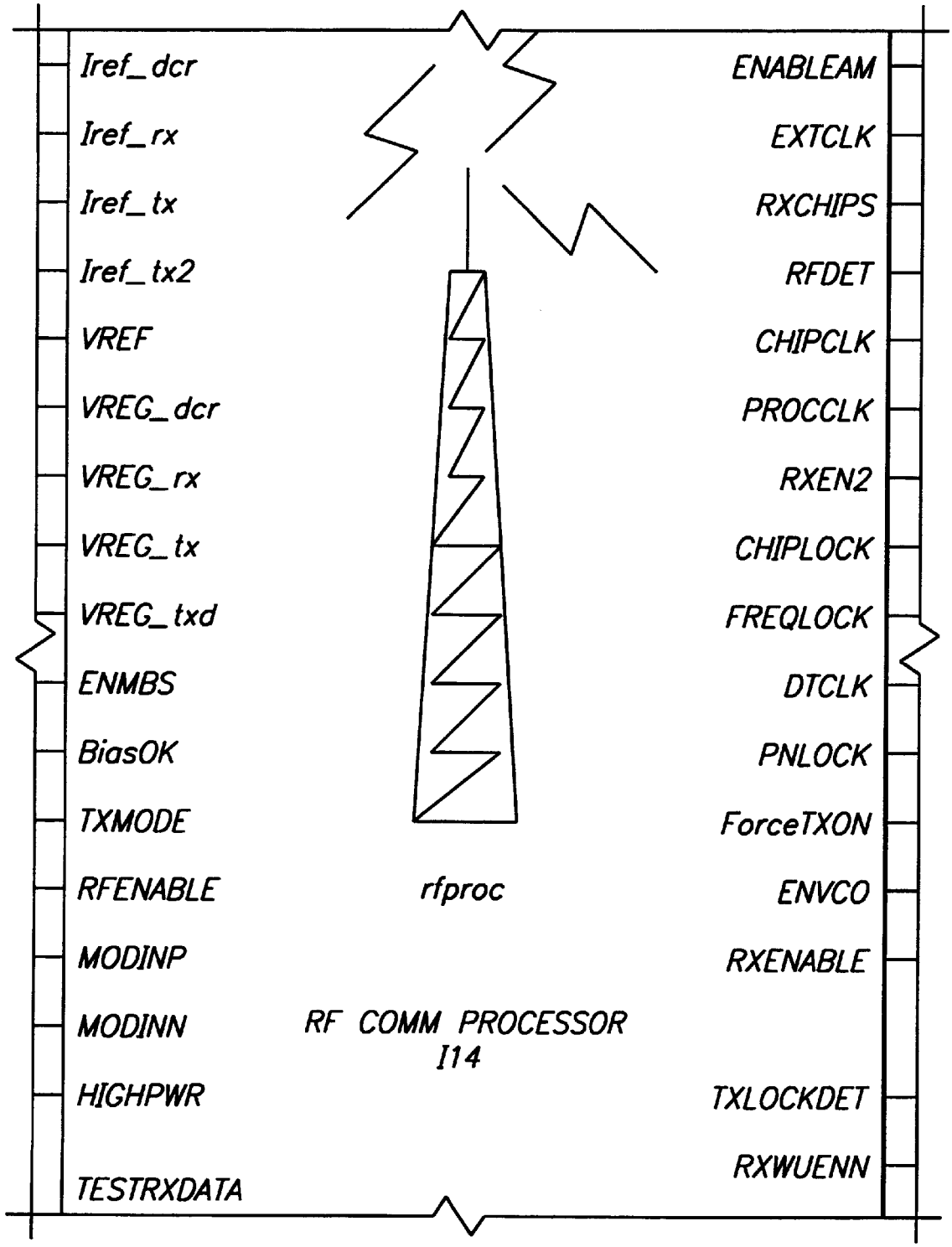

Iref_dcr
Iref_rx
Iref_tx
Iref_tx2
VREF
VREG_dcr
VREG_rx
VREG_tx
VREG_txd
ENMBS
BiasOK
TXMODE
RFENABLE
MODINP
MODINN
HIGHPWR
TESTRXDATA
ENABLEAM
EXTCLK
RXCHIPS
RFDET
CHIPCLK
PROCCLK
RXEN2
CHIPLOCK
FREQLOCK
DTCLK
PNLOCK
ForceTXON
ENVCO
RXENABLE
TXLOCKDET
RXWUENN
rfproc
RF COMM PROCESSOR
I14

Fig 19CH

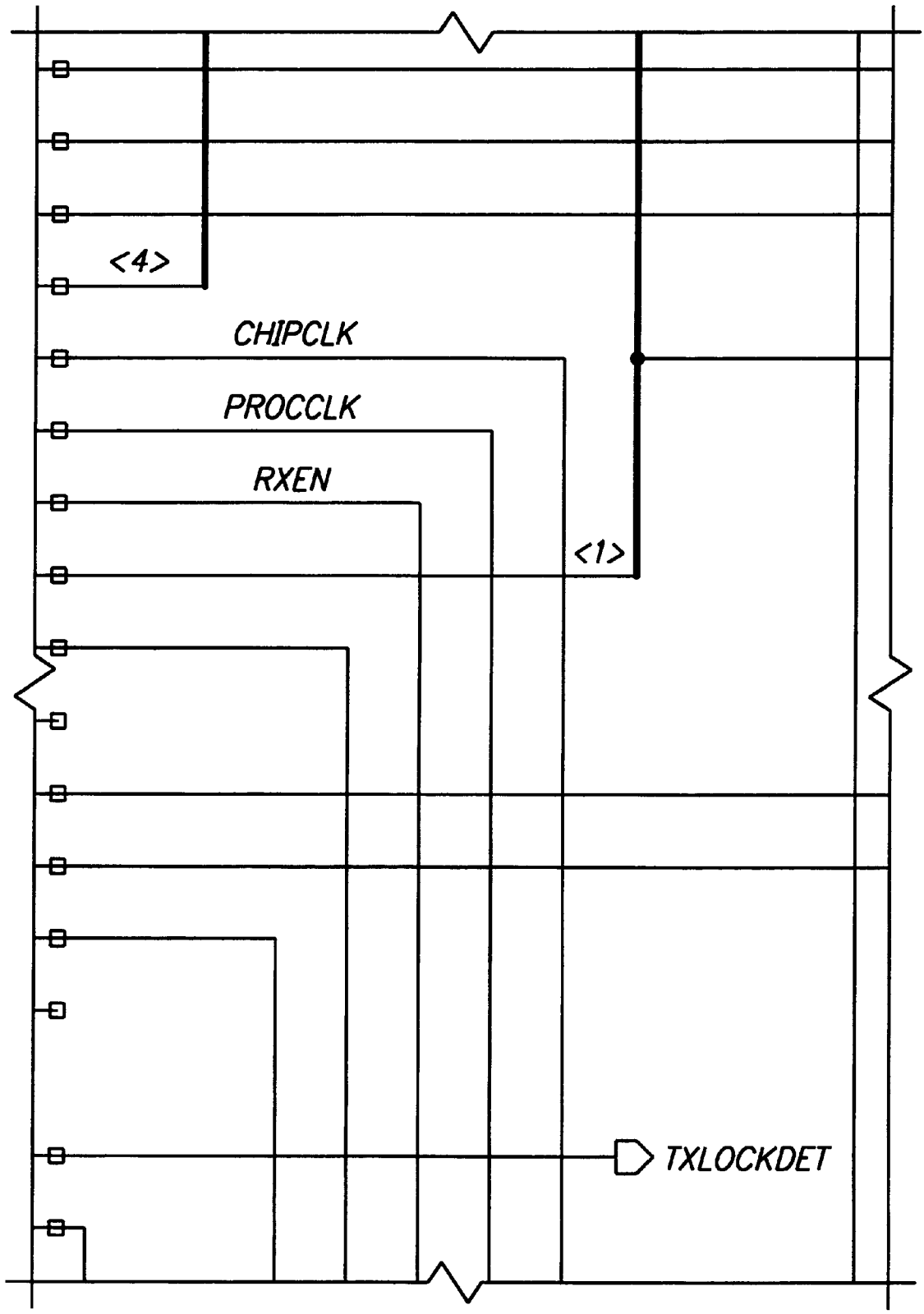


Fig 19CII

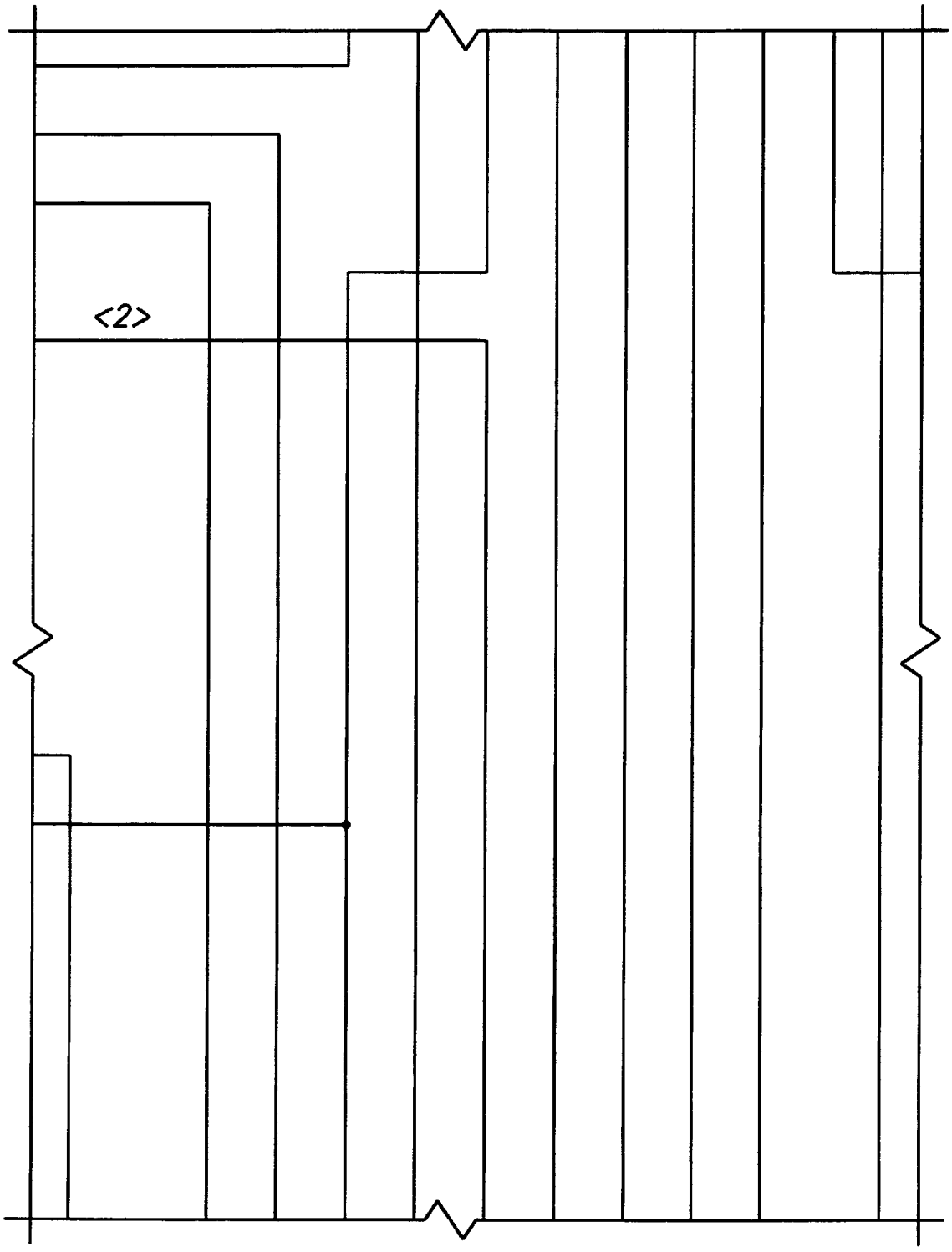


Fig 190a

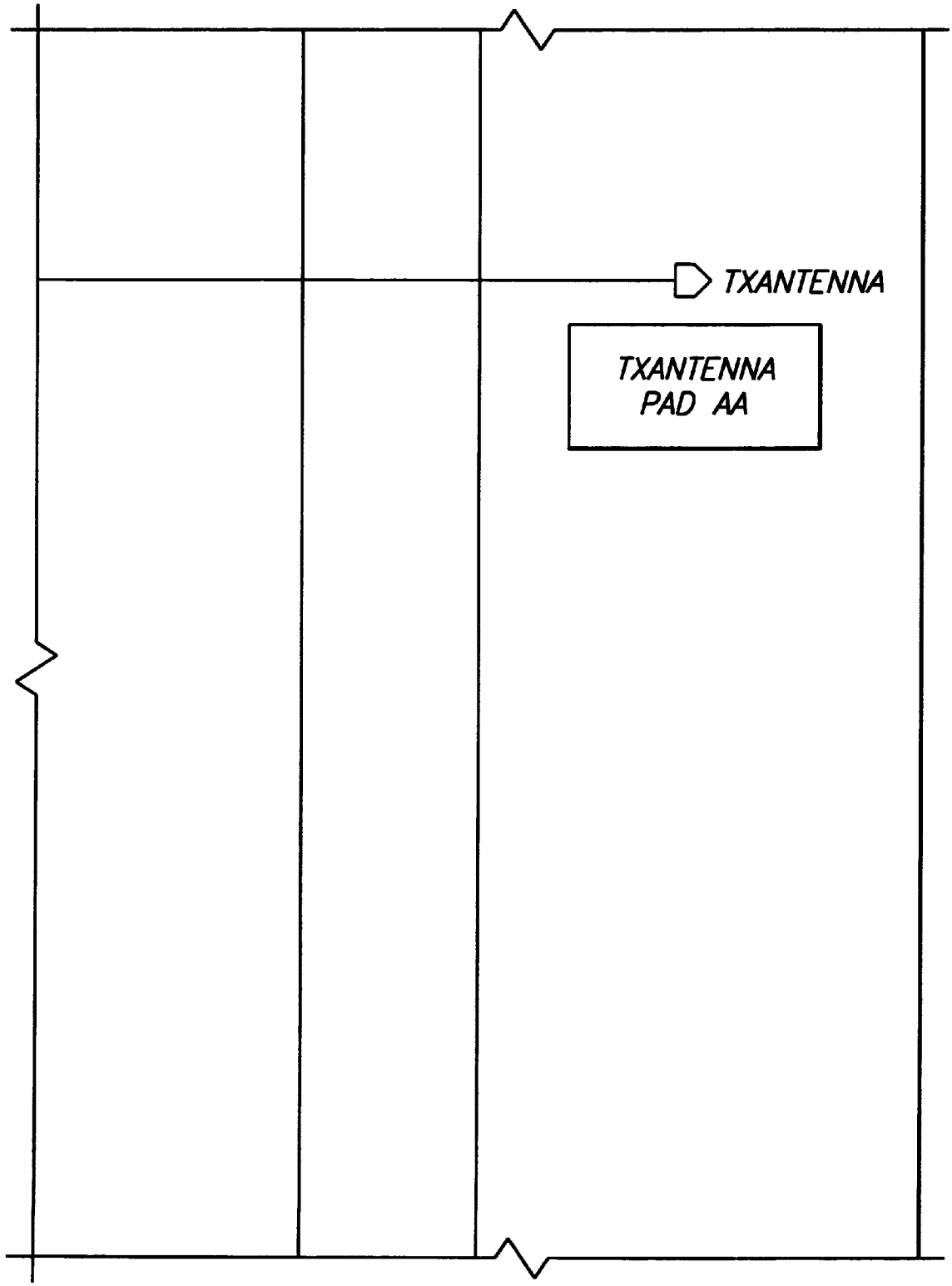


Fig 19CK

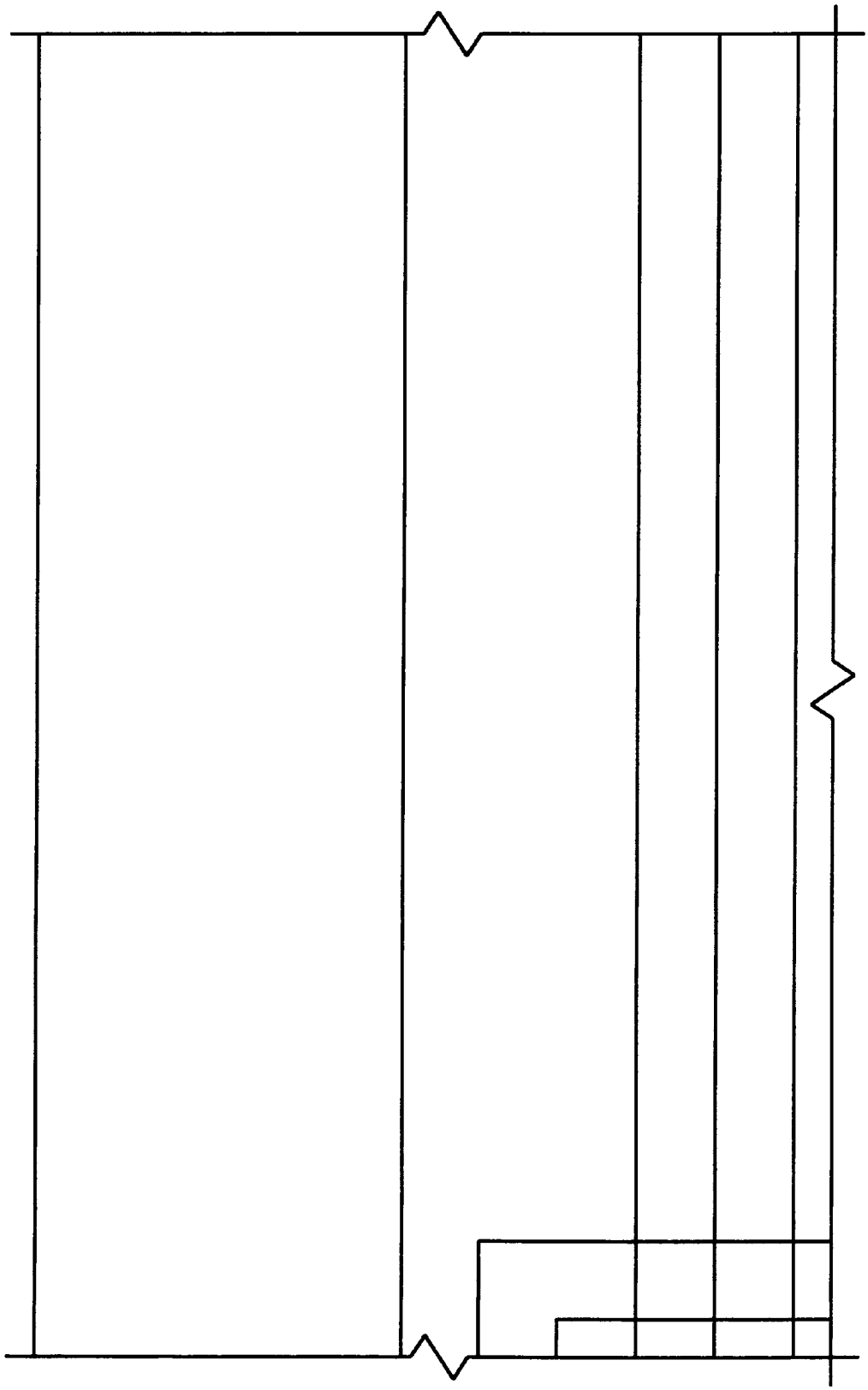


Fig 19DA

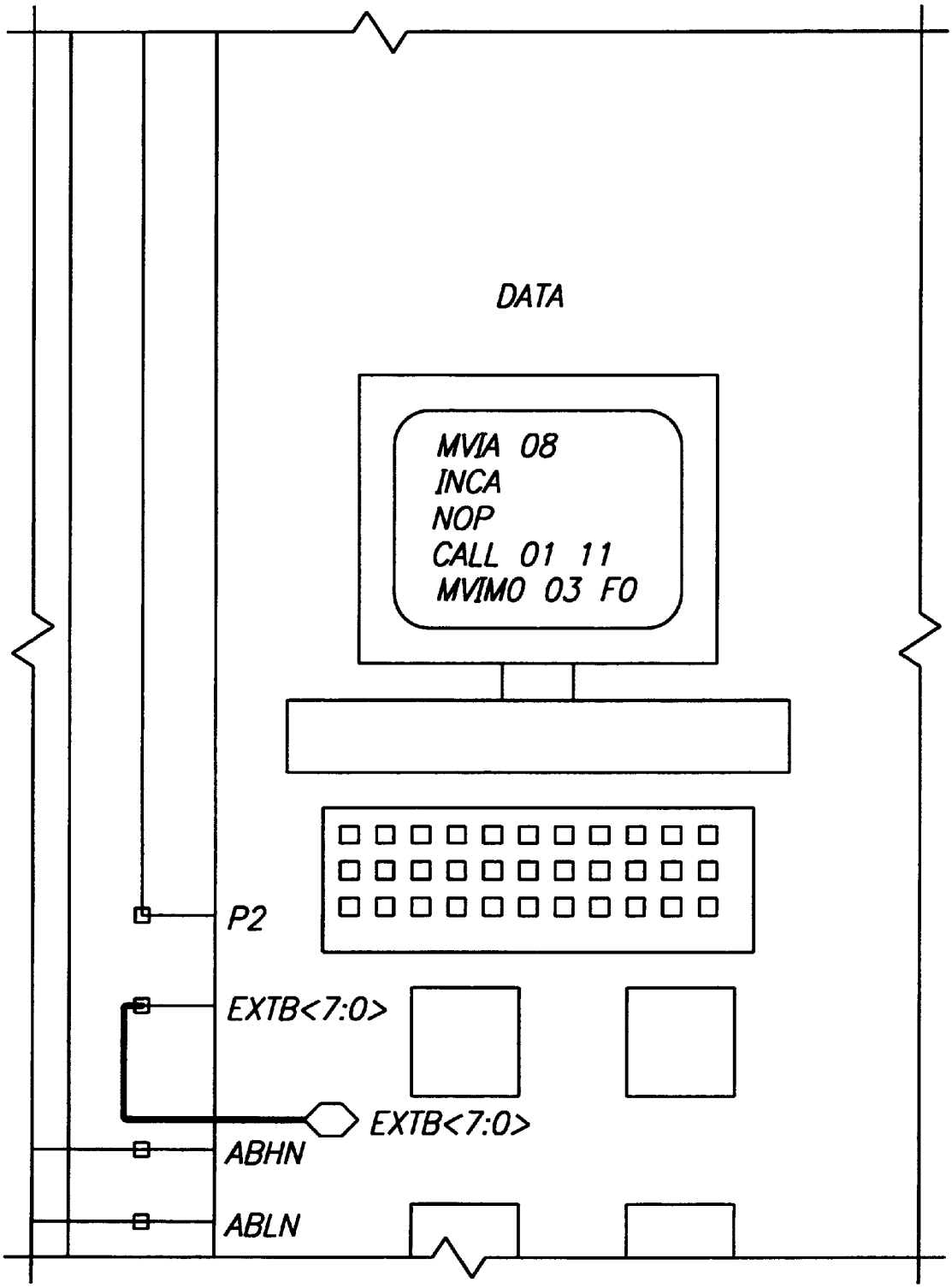

DATA
MVIA 08
INCA
NOP
CALL 01 11
MVIMO 03 F0
P2
EXTB<7:0>
EXTB<7:0>
ABHN
ABLN

Fig 190B

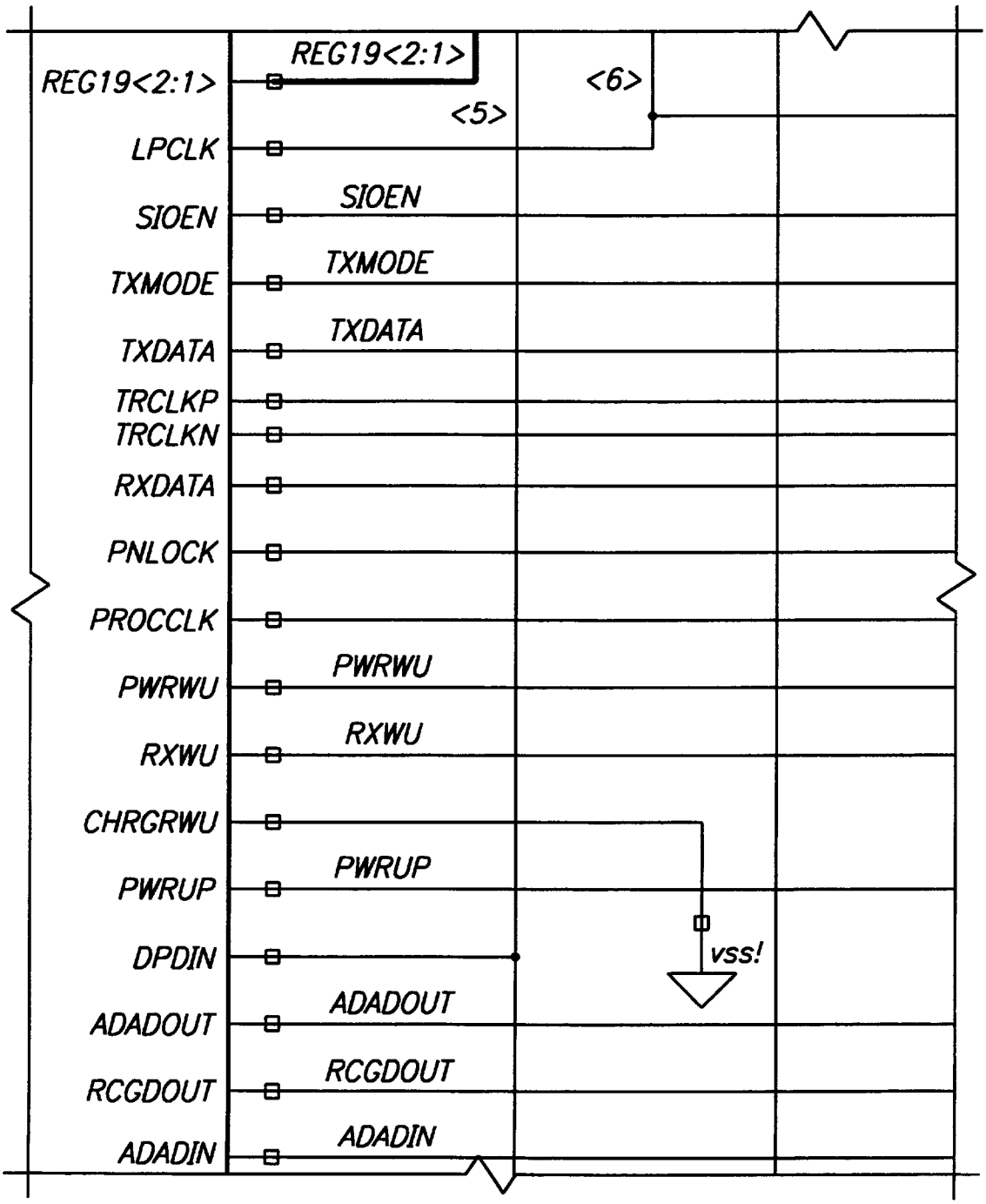

REG19<2:1>
REG19<2:1>
<6>
<5>
LPCLK
SIOEN
SIOEN
TXMODE
TXMODE
TXDATA
TXDATA
TRCLKP
TRCLKN
RXDATA
PNLOCK
PROCCLK
PWRWU
PWRWU
RXWU
RXWU
CHRGRWU
PWRUP
PWRUP
DPDIN
vss!
ADADOUT
ADADOUT
RCGDOUT
RCGDOUT
ADADIN
ADADIN

Fig 190C

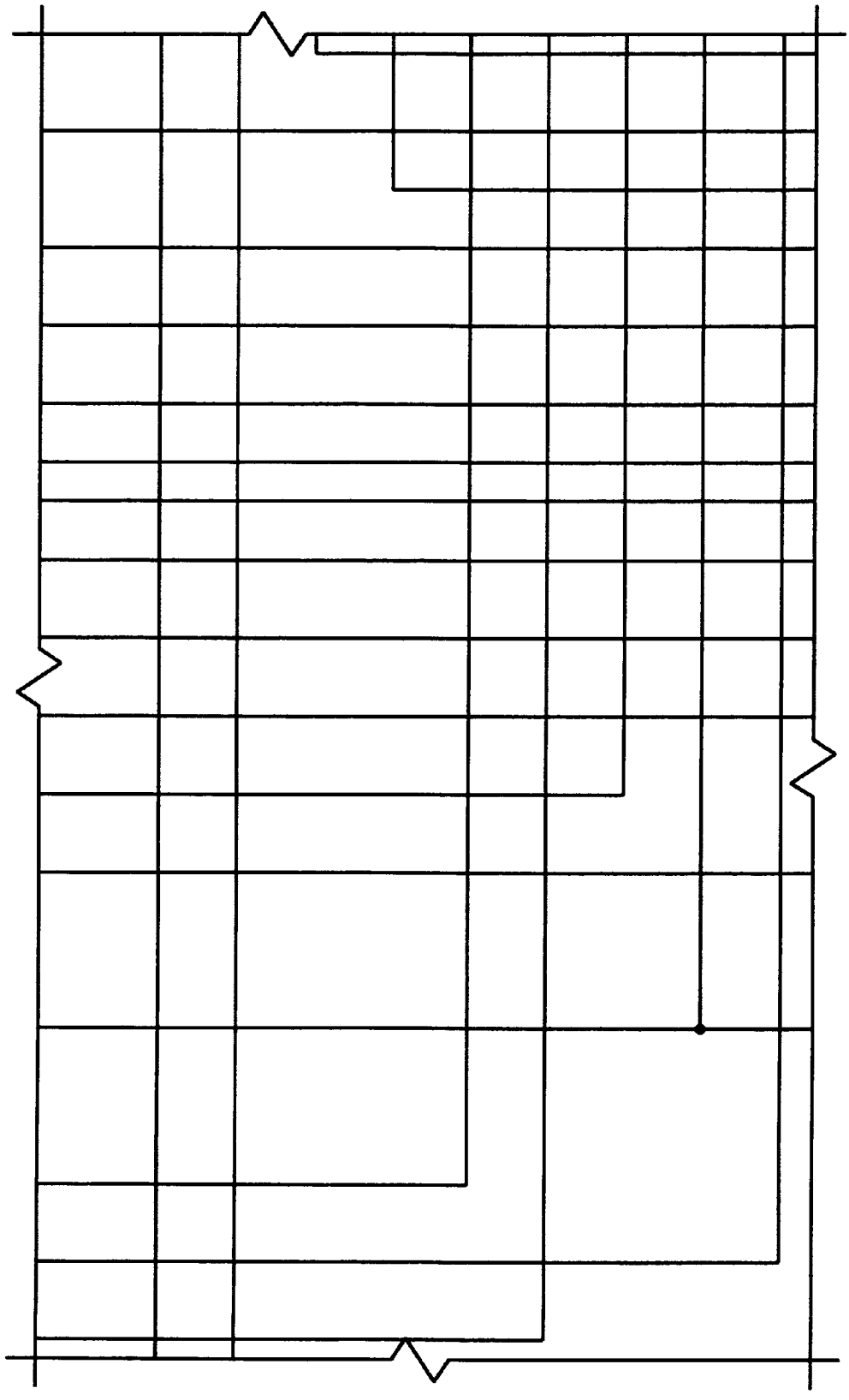


Fig 1900

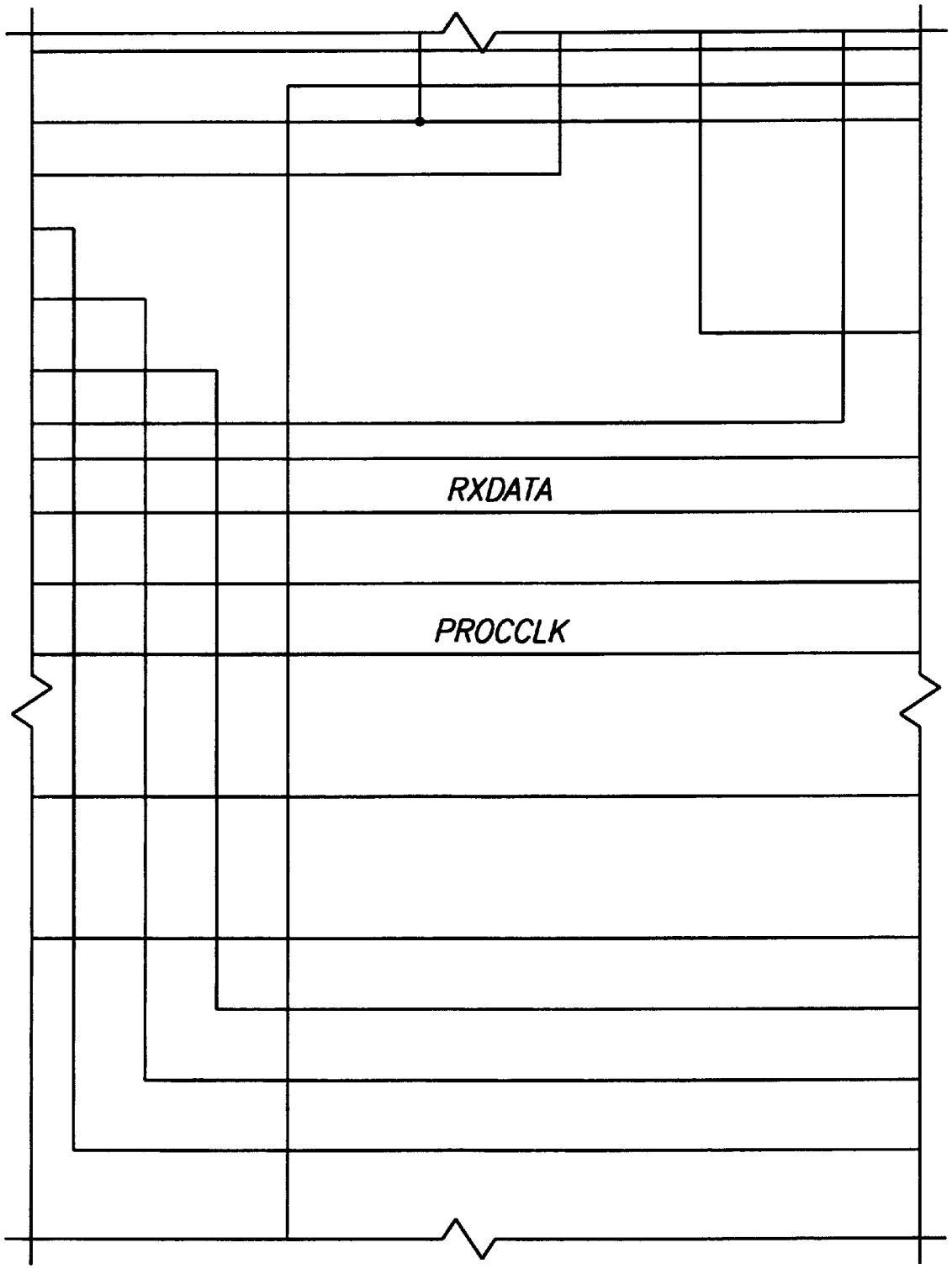


Fig 19DE

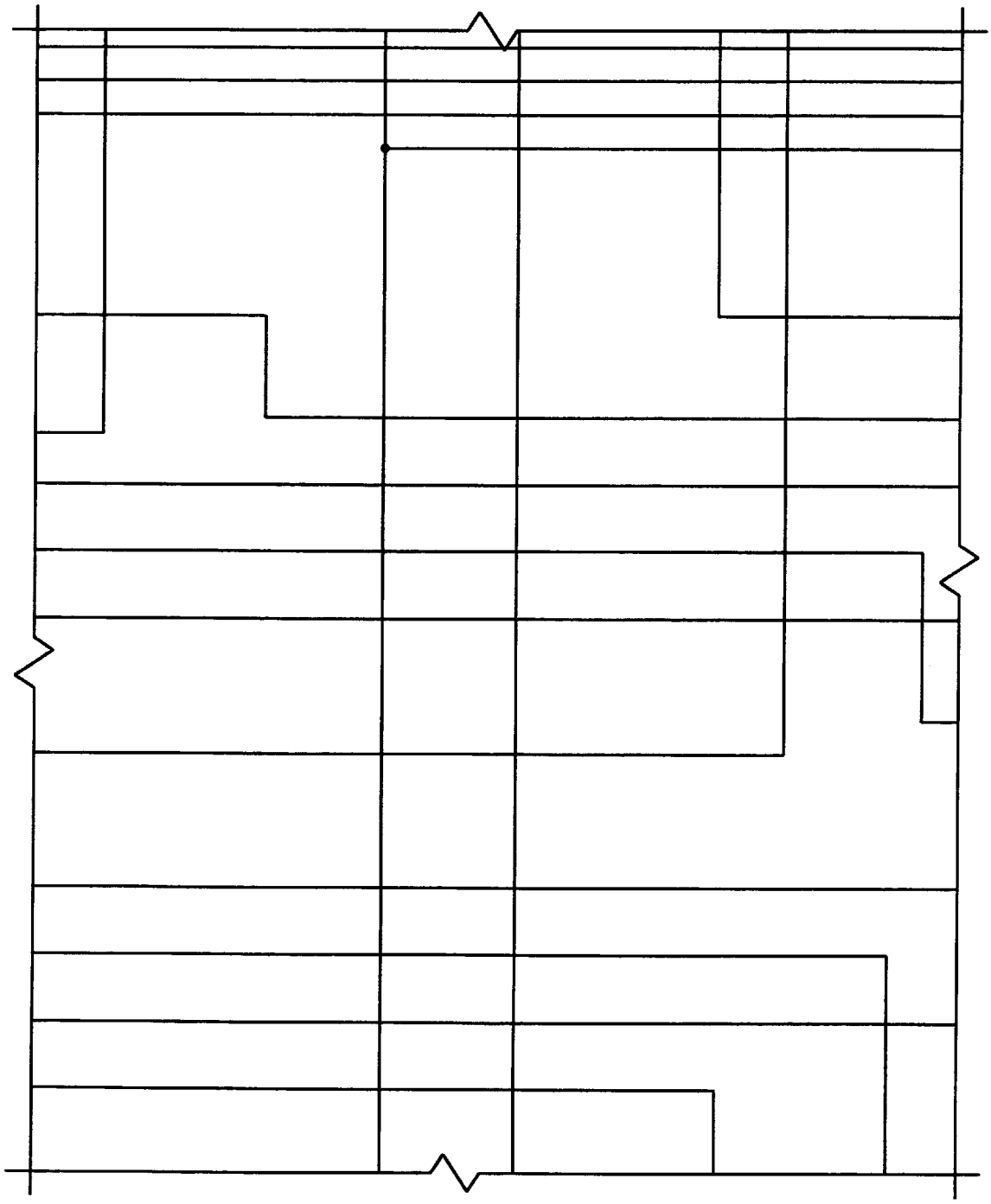


Fig 190F

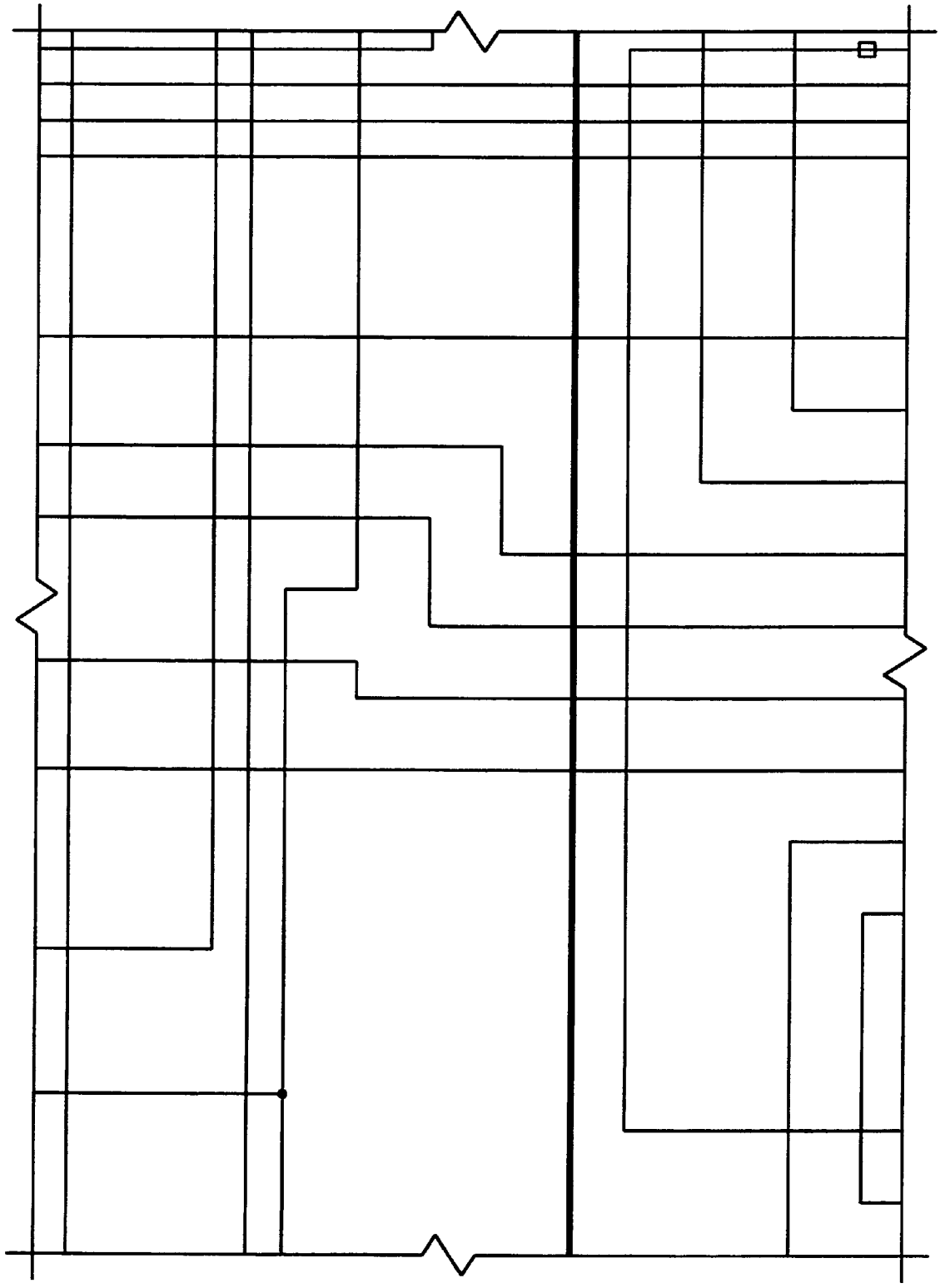


Fig 1906

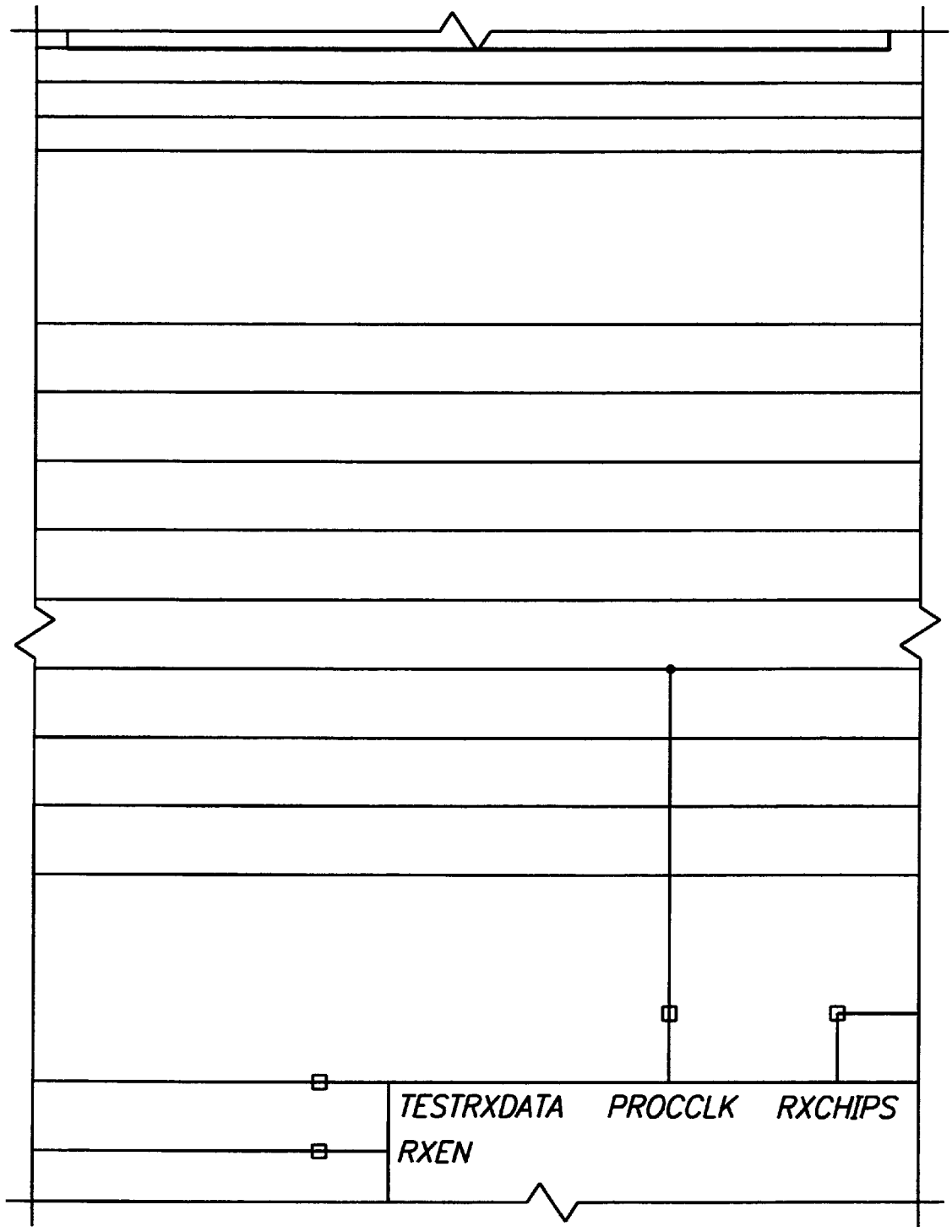


Fig 190H

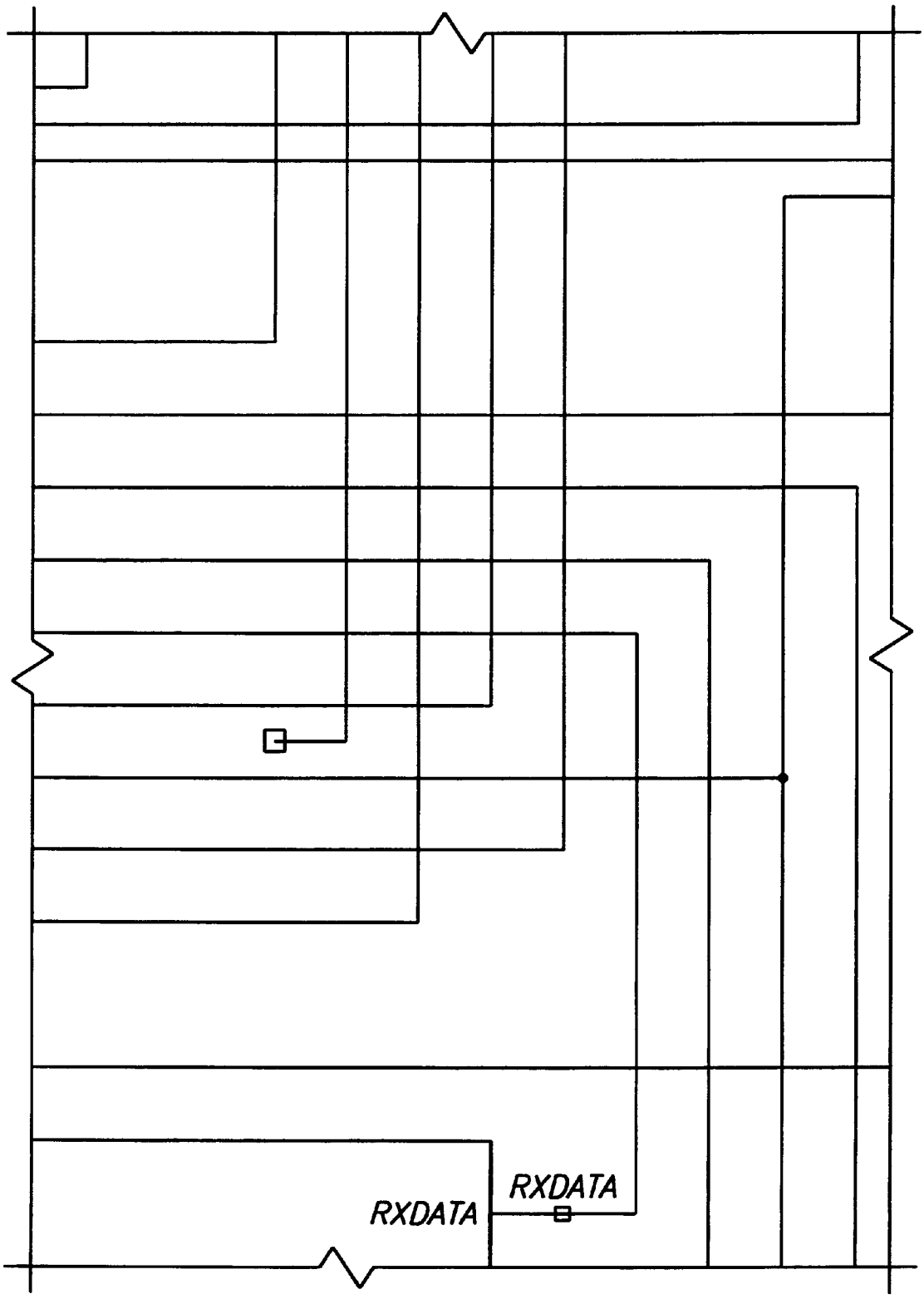


Fig 1901

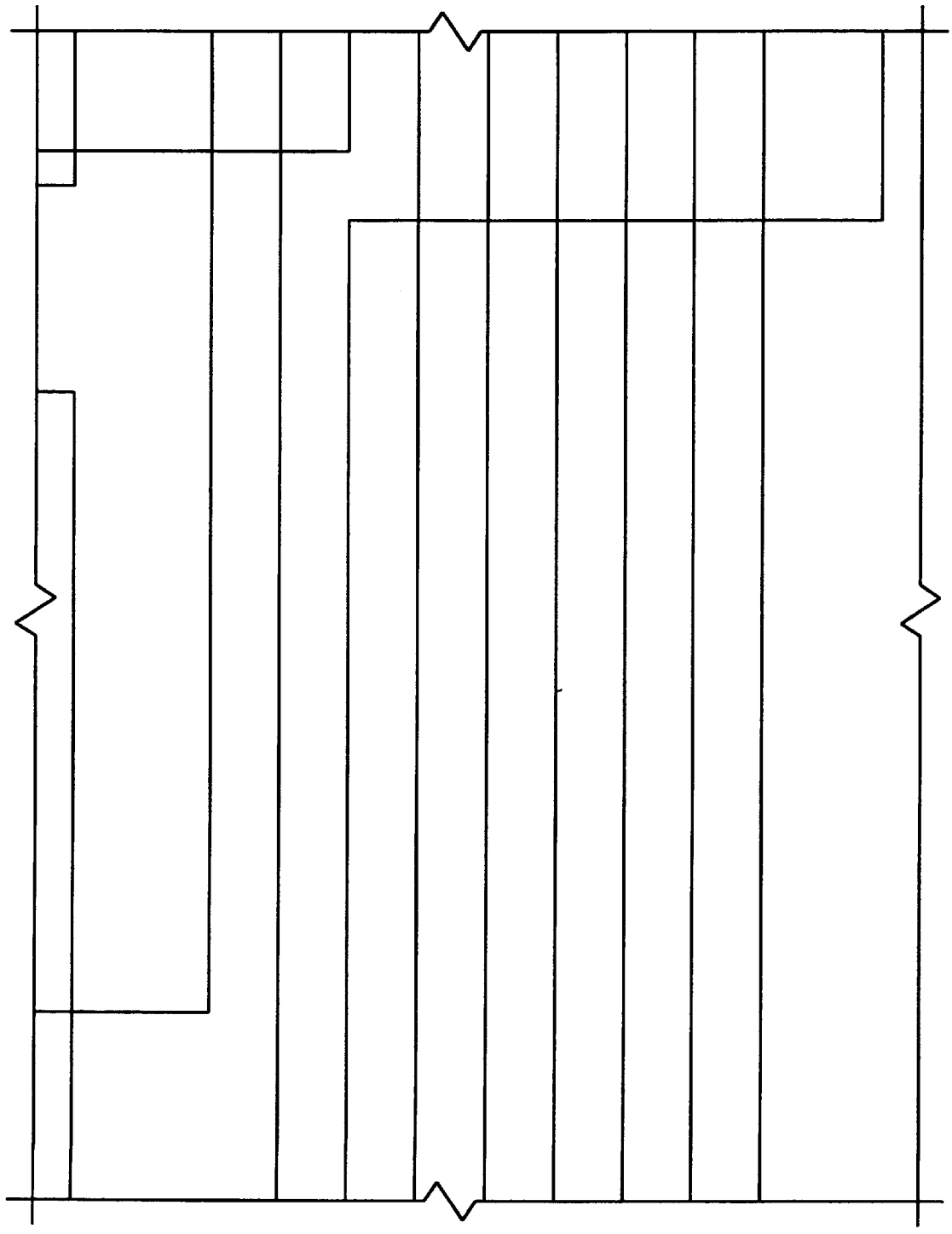


Fig 190al

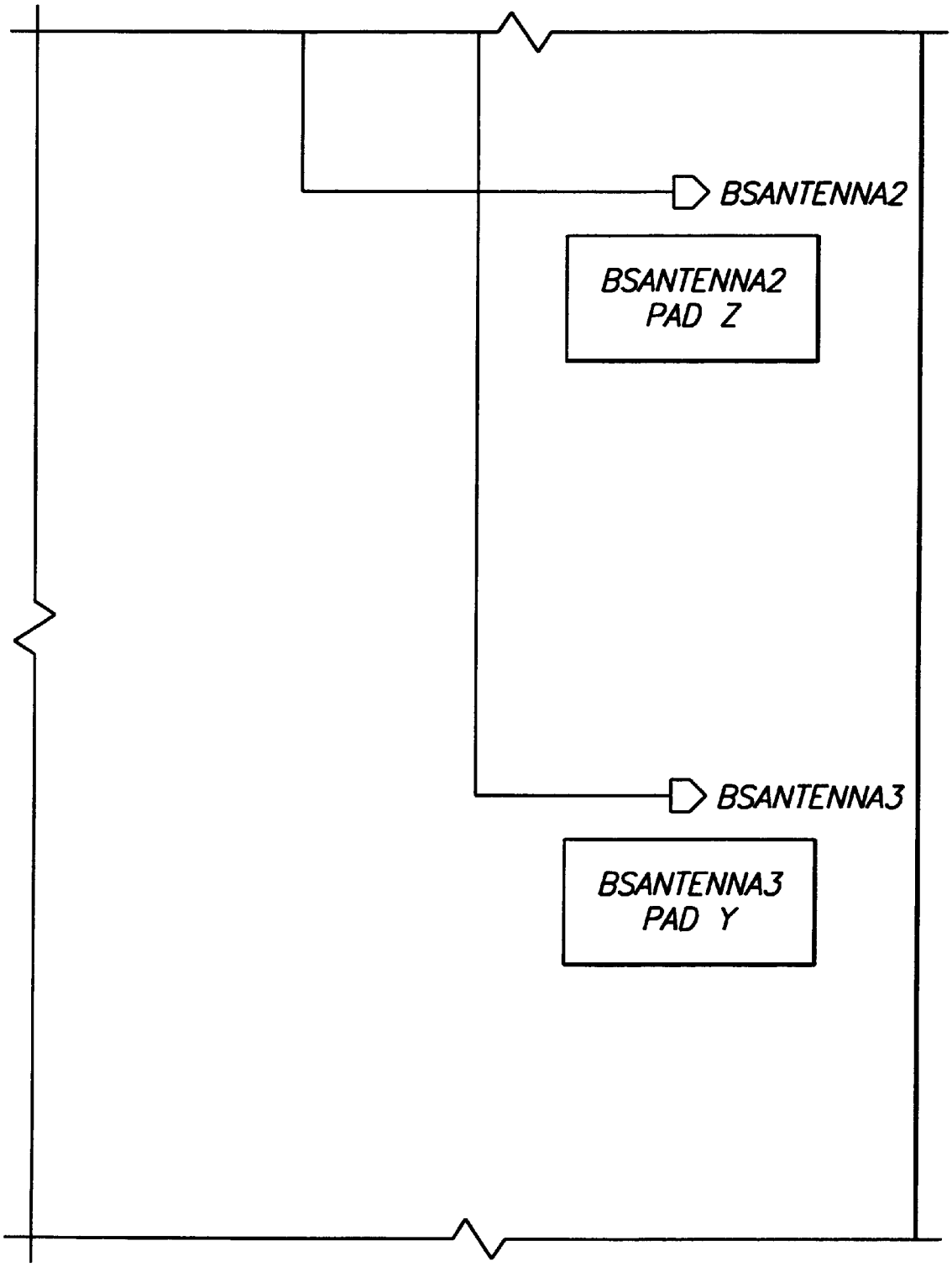


Fig 190K

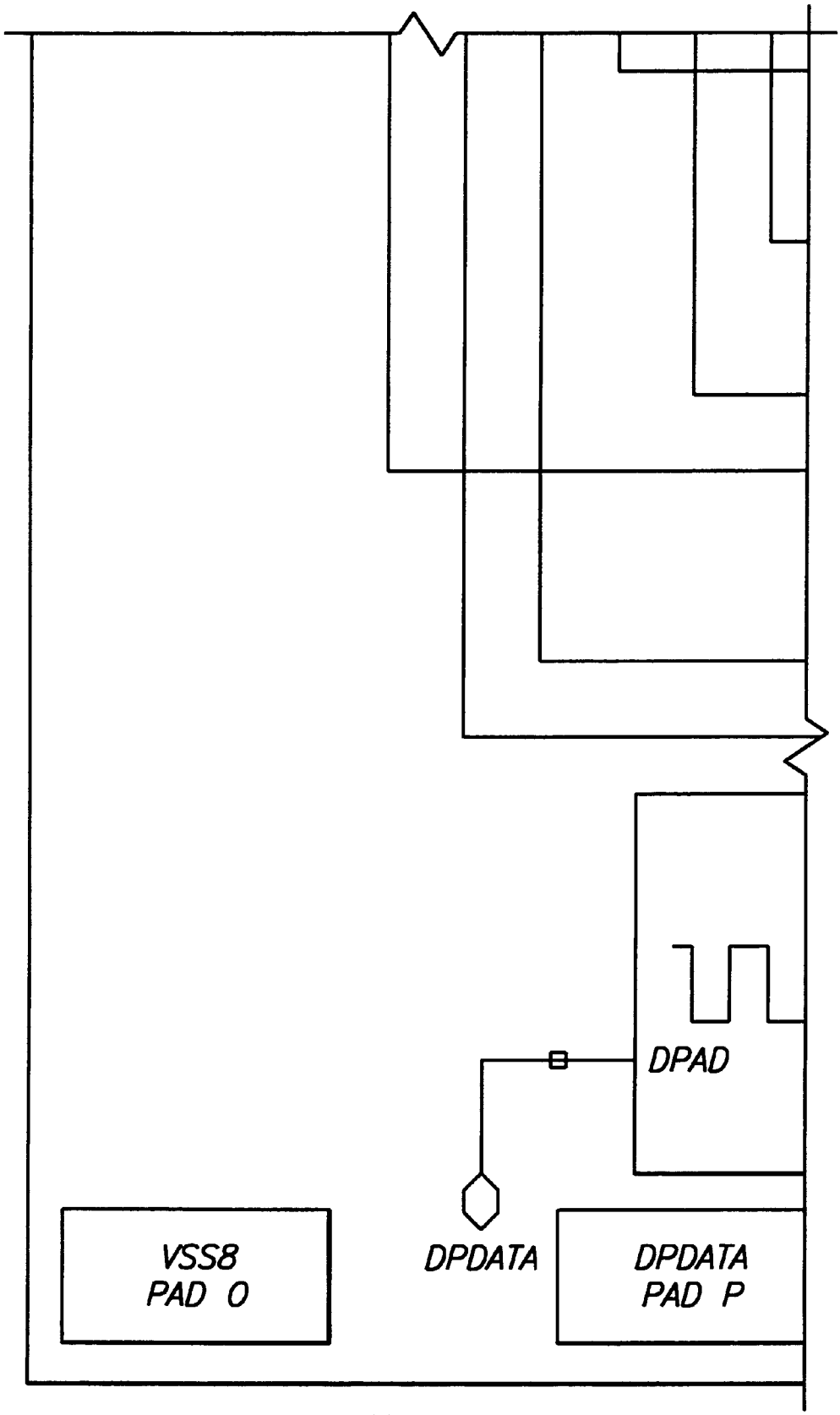


Fig 19EA

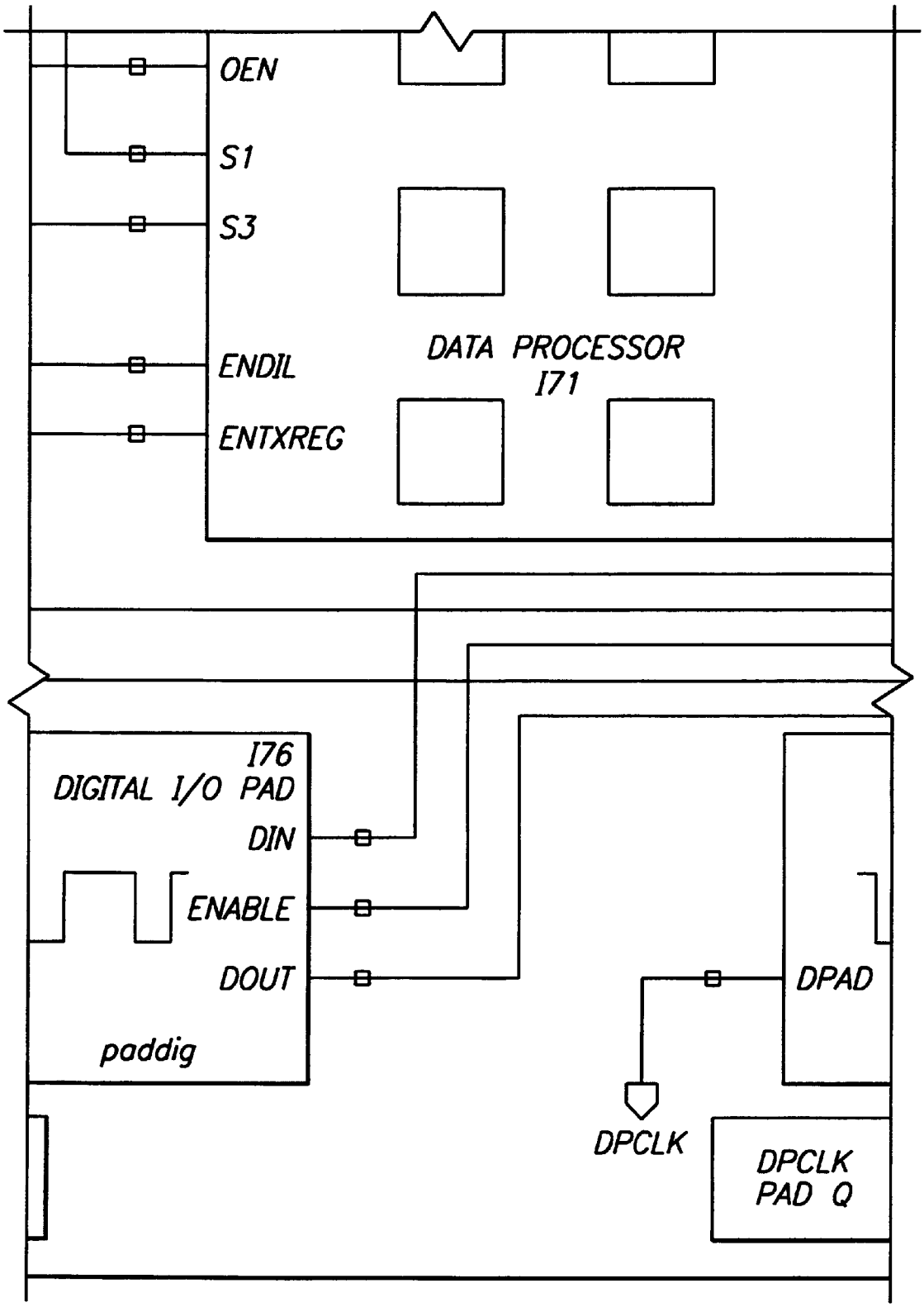

OEN
S1
S3
ENDIL
ENTXREG
DATA PROCESSOR
I71
I76
DIGITAL I/O PAD
DIN
ENABLE
DOUT
paddig
DPAD
DPCLK
DPCLK
PAD Q

Fig 19EB

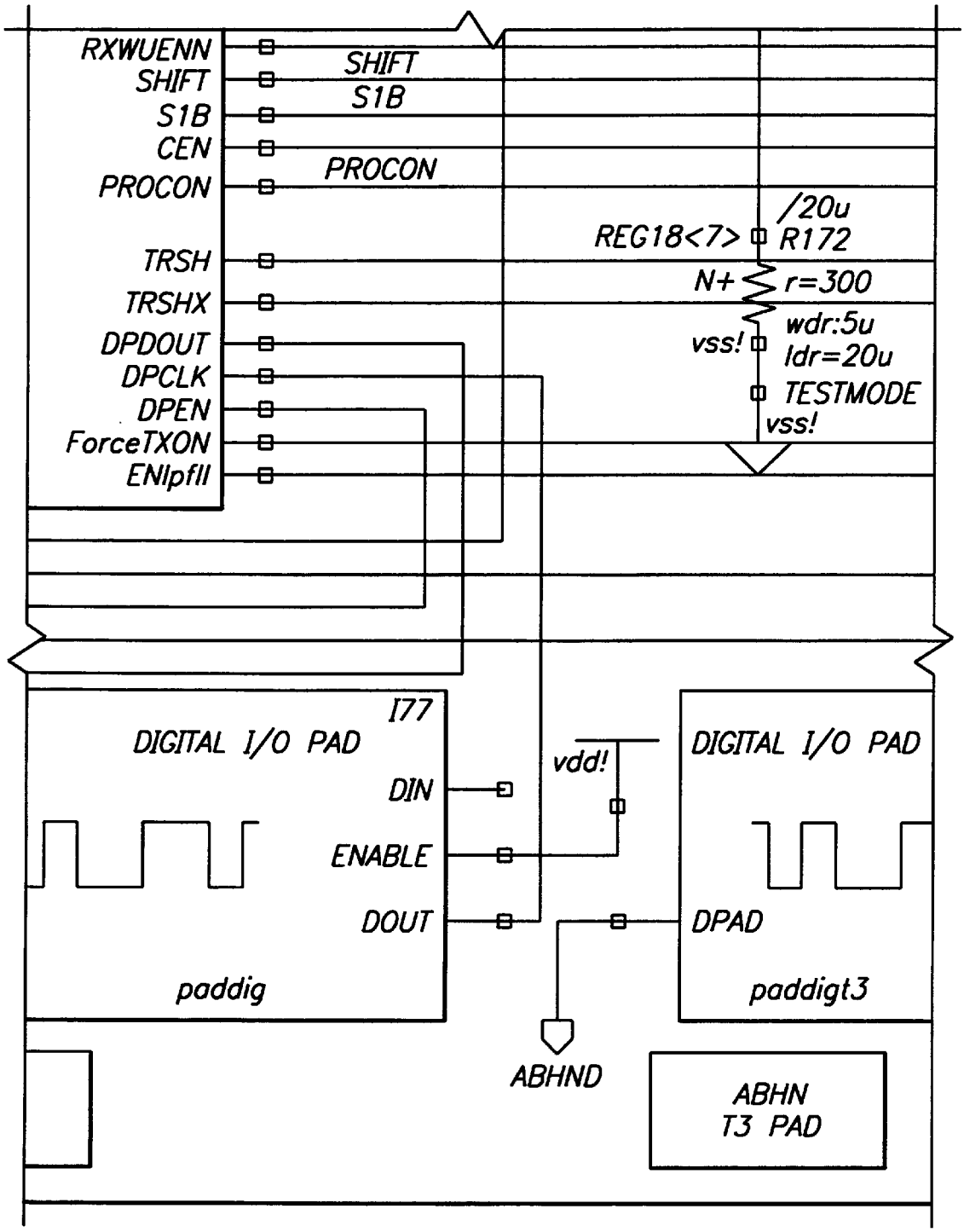

RXWUENN
SHIFT
S1B
CEN
PROCON
TRSH
TRSHX
DPDOUT
DPCLK
DPEN
ForceTXON
ENIpfII
SHIFT
S1B
PROCON
/20u
REG18<7>
R172
N+
r=300
wdr:5u
vss!
ldr=20u
TESTMODE
vss!
I77
DIGITAL I/O PAD
DIN
ENABLE
DOUT
paddig
vdd!
DIGITAL I/O PAD
DPAD
paddigt3
ABHND
ABHN
T3 PAD

Fig 19EC

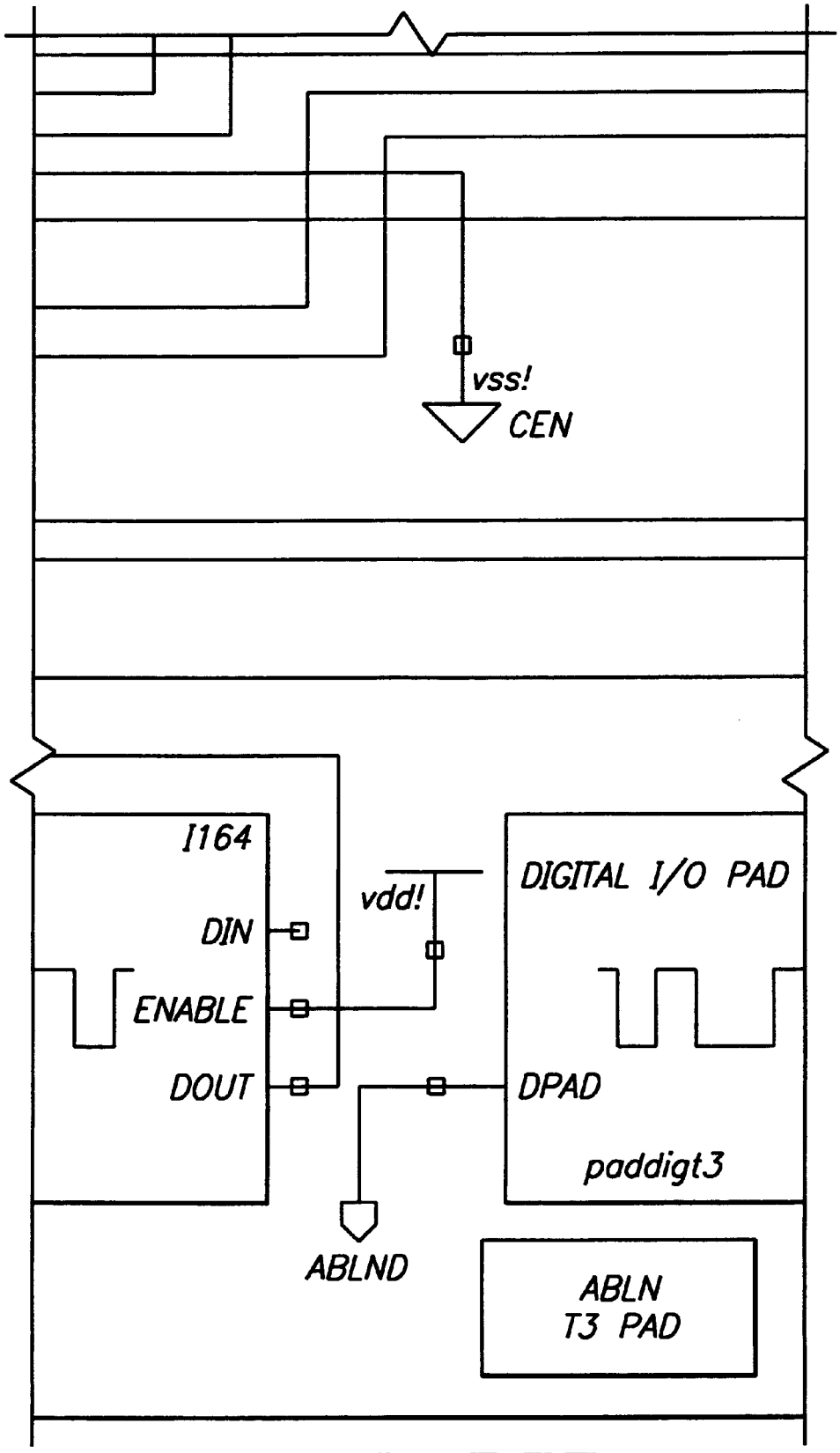

vss!
CEN
I164
DIN
ENABLE
DOUT
vdd!
DIGITAL I/O PAD
DPAD
paddigt3
ABLND
ABLN
T3 PAD

Fig 19ED

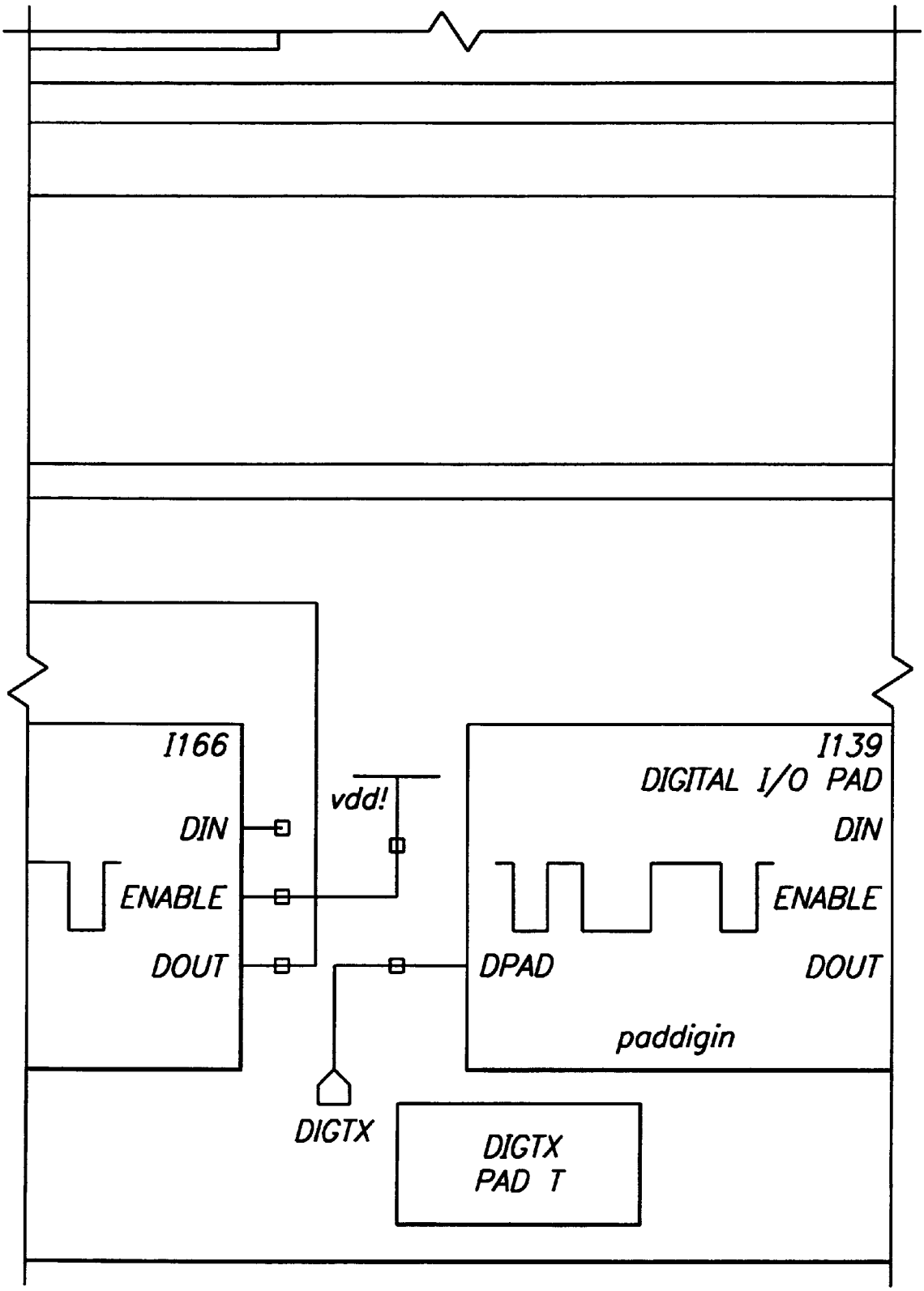

I166
DIN
ENABLE
DOUT
vdd!
I139
DIGITAL I/O PAD
DIN
ENABLE
DPAD
DOUT
paddigin
DIGTX
DIGTX
PAD T

Fig 19EE

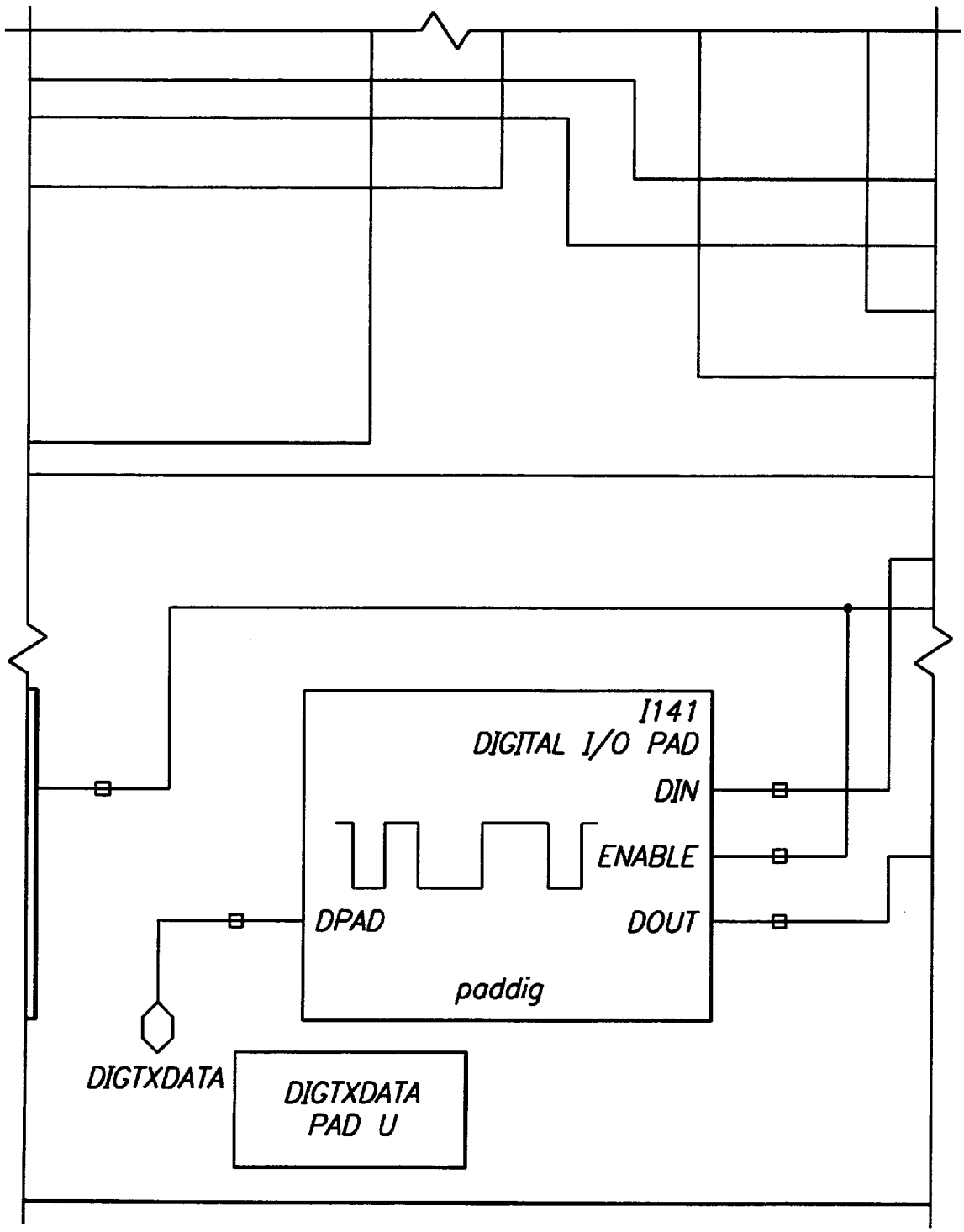

I141
DIGITAL I/O PAD
DIN
ENABLE
DPAD
DOUT
paddig
DIGTXDATA
DIGTXDATA
PAD U

Fig 19EF

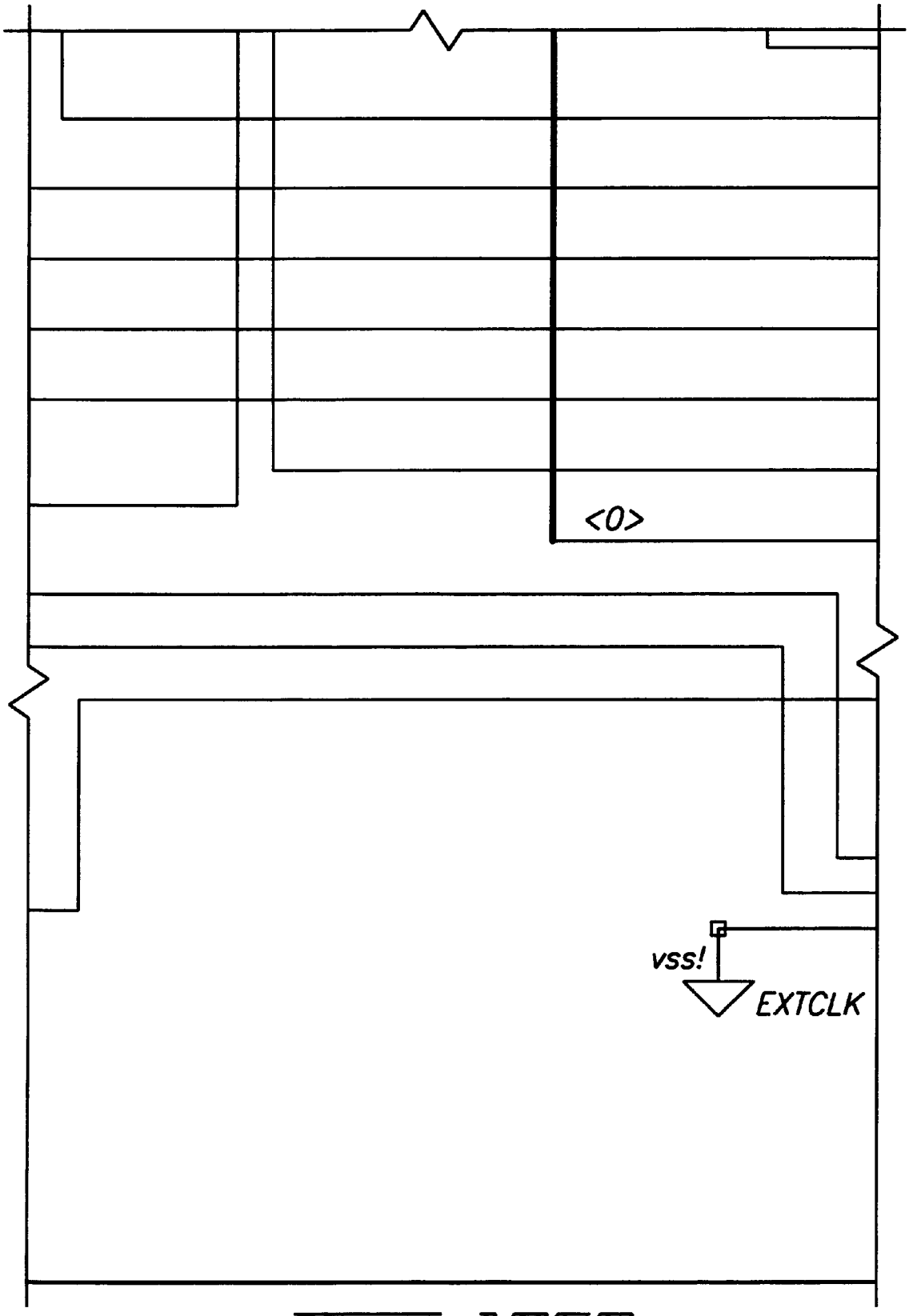


Fig 196

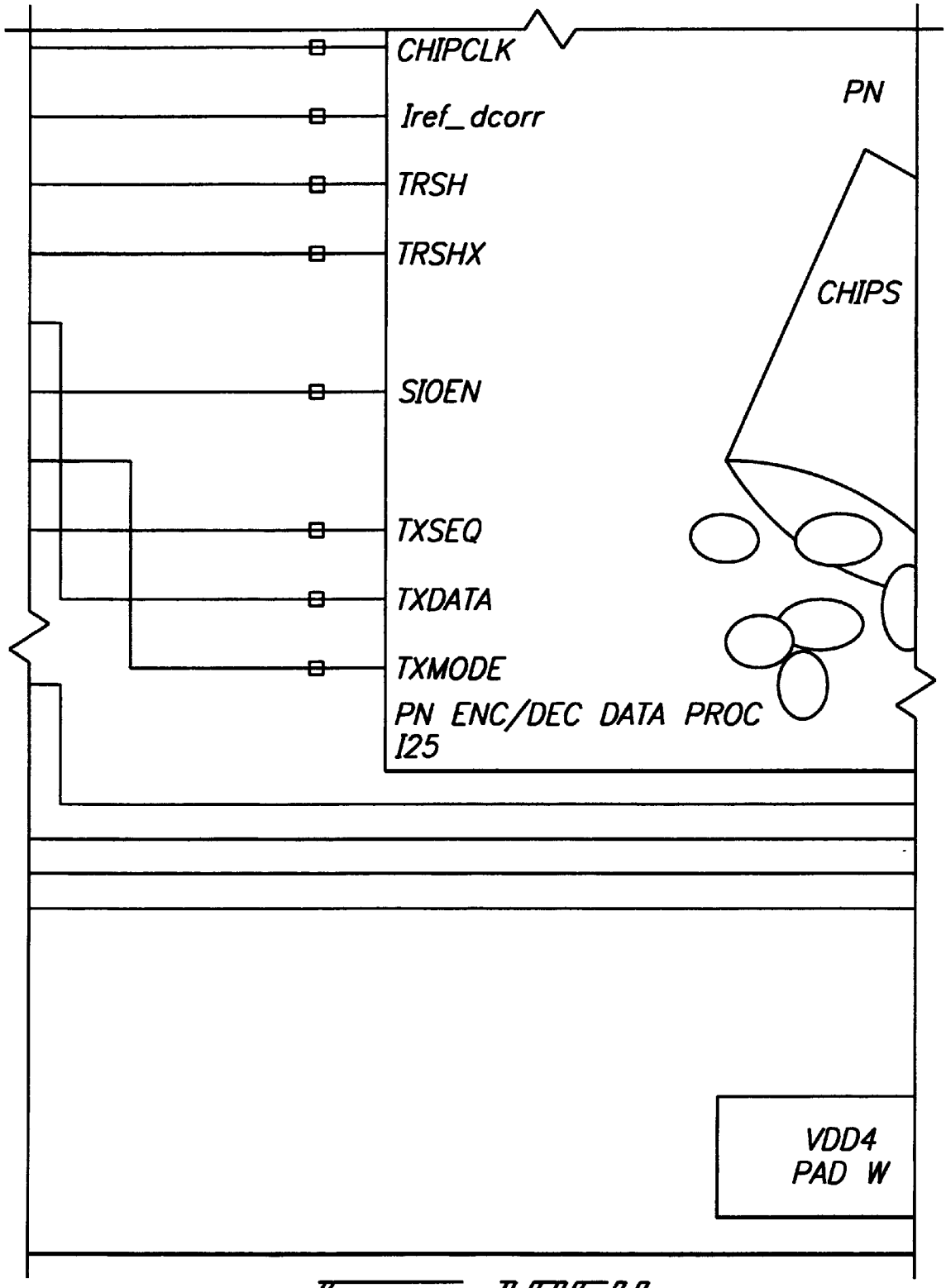

CHIPCLK
Iref_dcorr
TRSH
TRSHX
SIOEN
TXSEQ
TXDATA
TXMODE
PN ENC/DEC DATA PROC
I25
PN
CHIPS
VDD4
PAD W

Fig 19EH

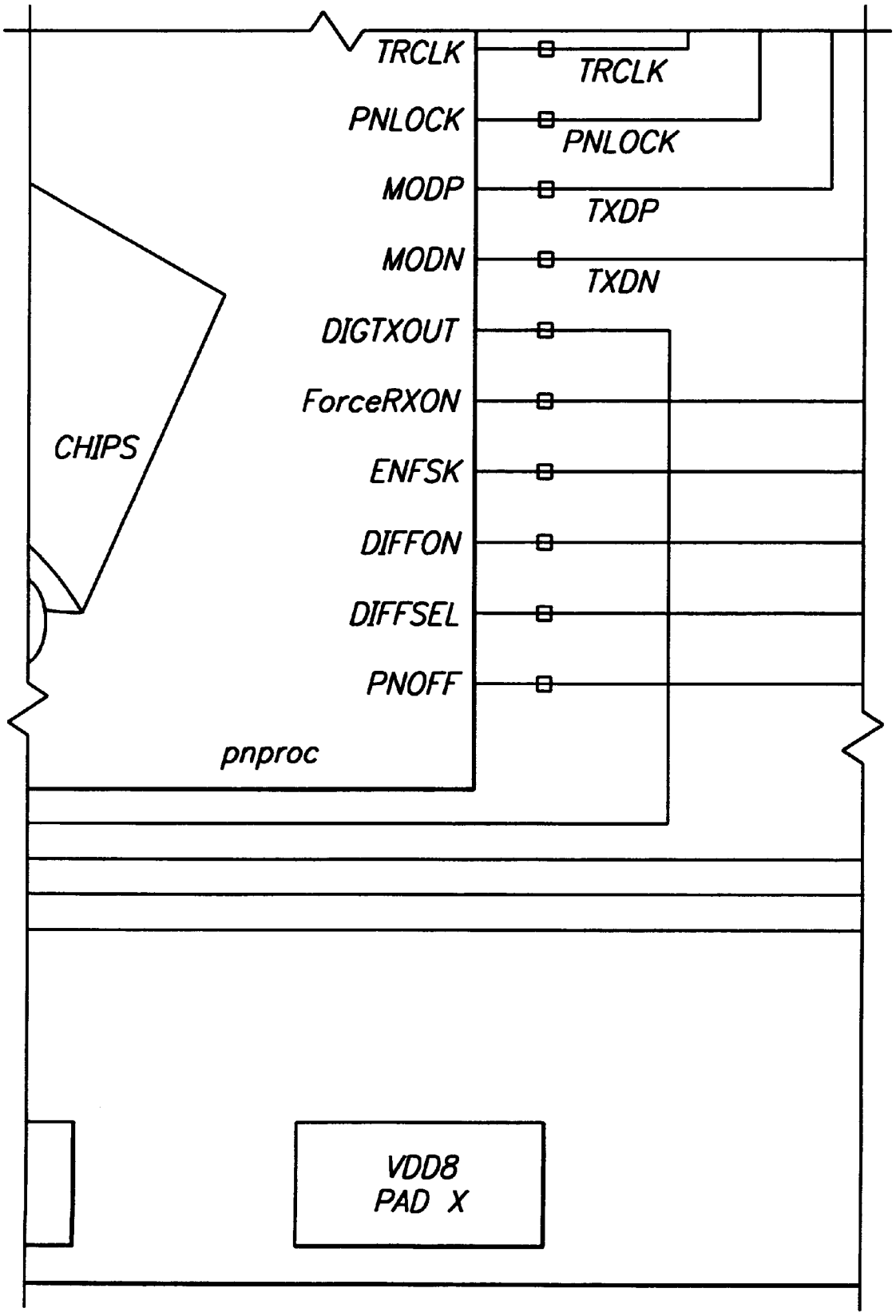

TRCLK
PNLOCK
MODP
MODN
DIGTXOUT
ForceRXON
ENFSK
DIFFON
DIFFSEL
PNOFF
pnproc
CHIPS
TRCLK
PNLOCK
TXDP
TXDN
VDD8
PAD X

Fig 19E

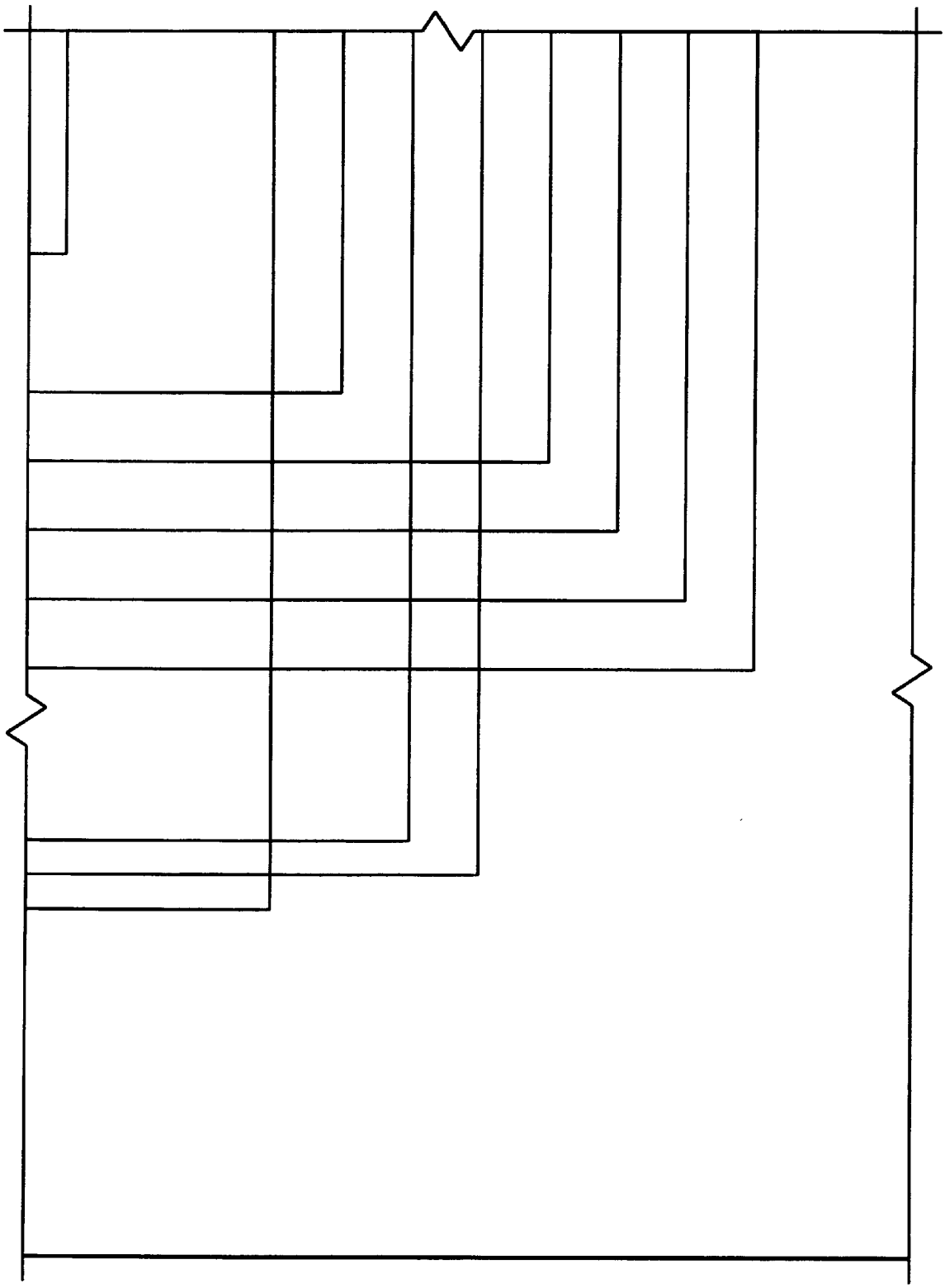


Fig 19Eal

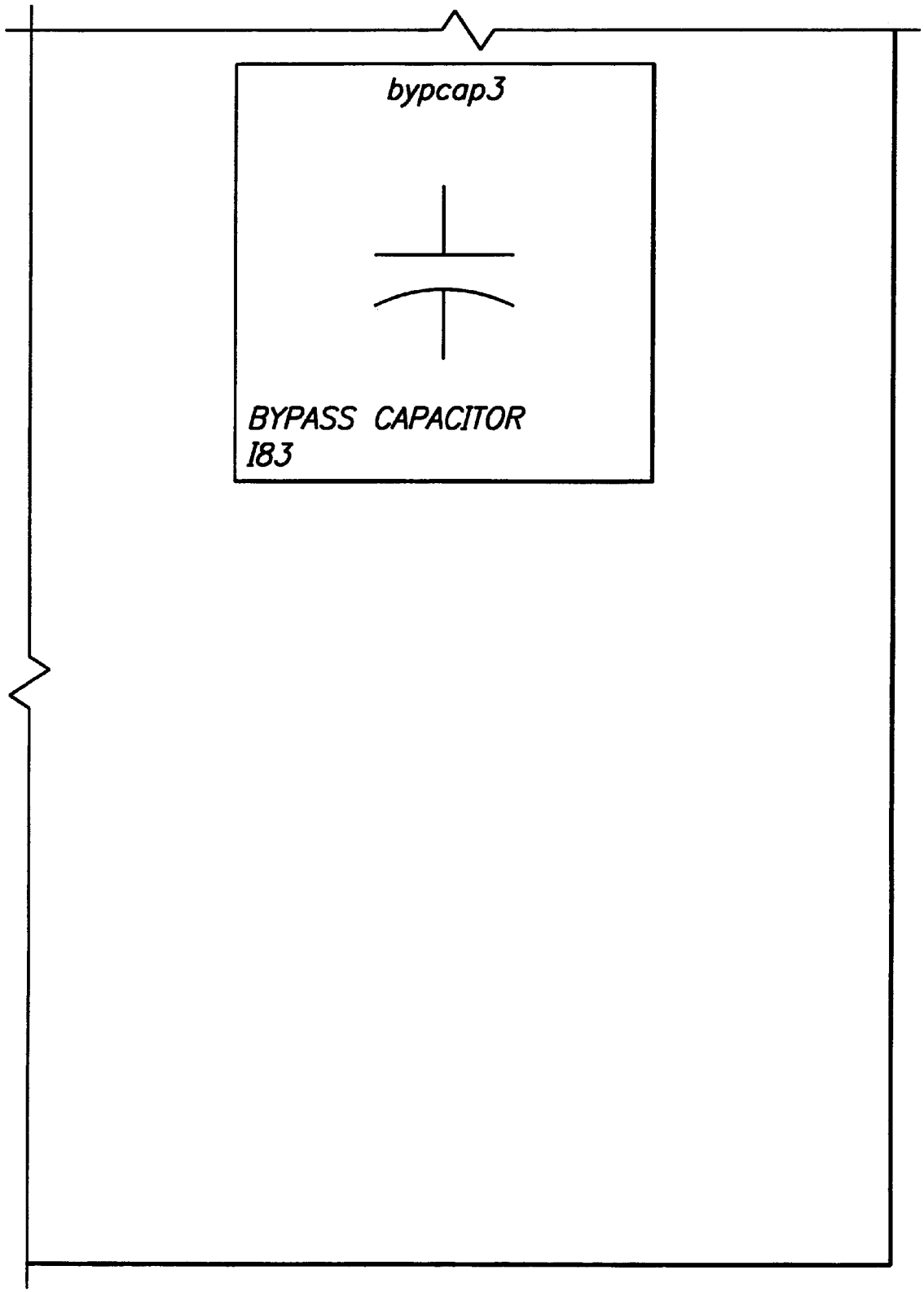
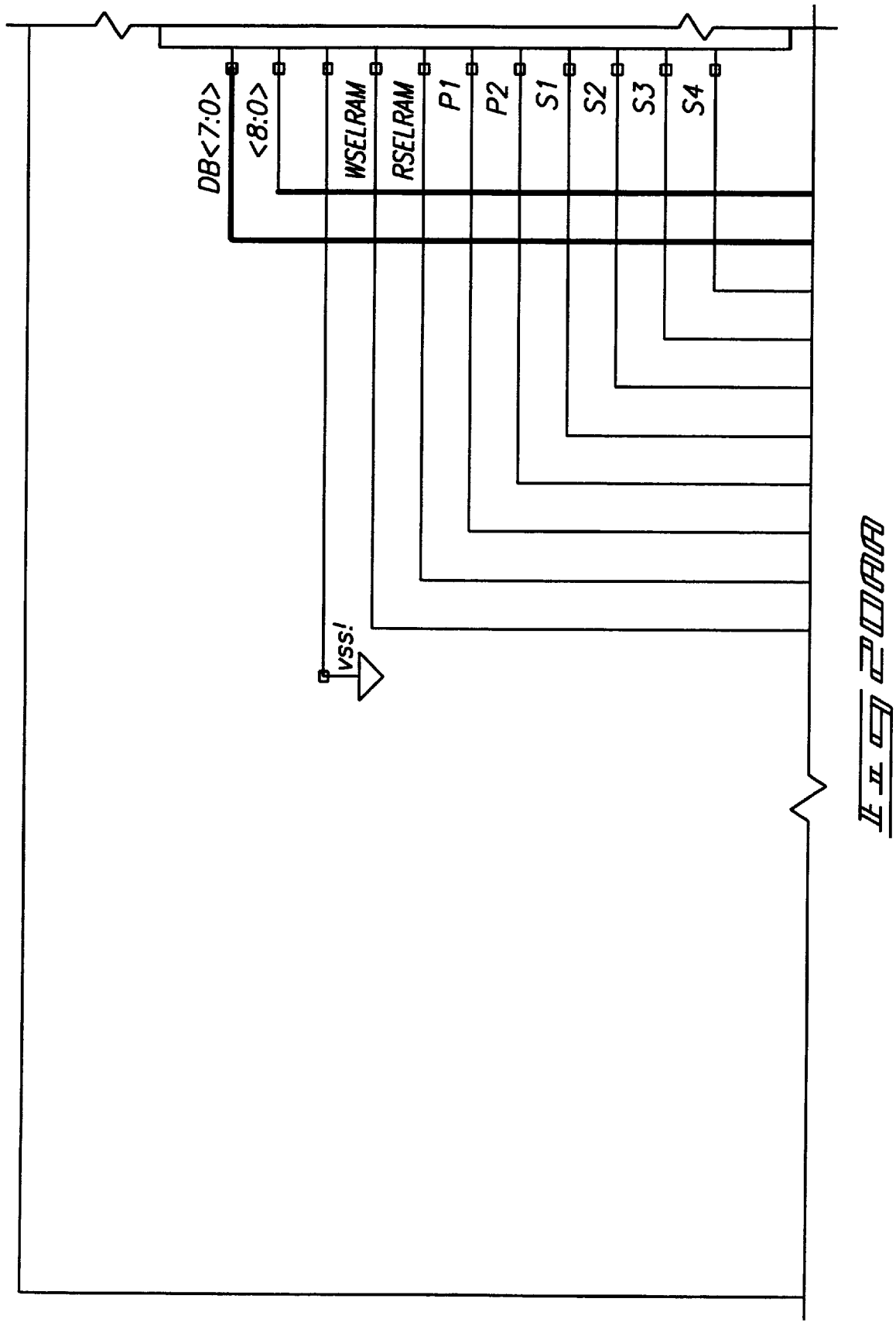


Fig 19EK

20AA	20AB								
20BA	20BB	20BC	20BD	20BE	20BF	20BG	20BH	20BI	20BJ
20CA	20CB	20CC	20CD	20CE	20CF	20CG	20CH	20CI	20CJ
20DA	20DB	20DC	20DD	20DE	20DF	20DG	20DH	20DI	20DJ
20EA	20EB	20EC	20ED	20EE	20EF	20EG	20EH	20EI	20EJ
20FA	20FB	20FC	20FD	20FE	20FF	20FG	20FH	20FI	20FJ
			20GD	20GE	20GF	20GG	20GH	20GI	20GJ
			20HD	20HE	20HF	20HG	20HH	20HI	20HJ

FIG 20


DB<7:0>
<8:0>
WSELRAM
RSELRAM
P1
P2
S1
S2
S3
S4
VSS!
FIG 2AAA

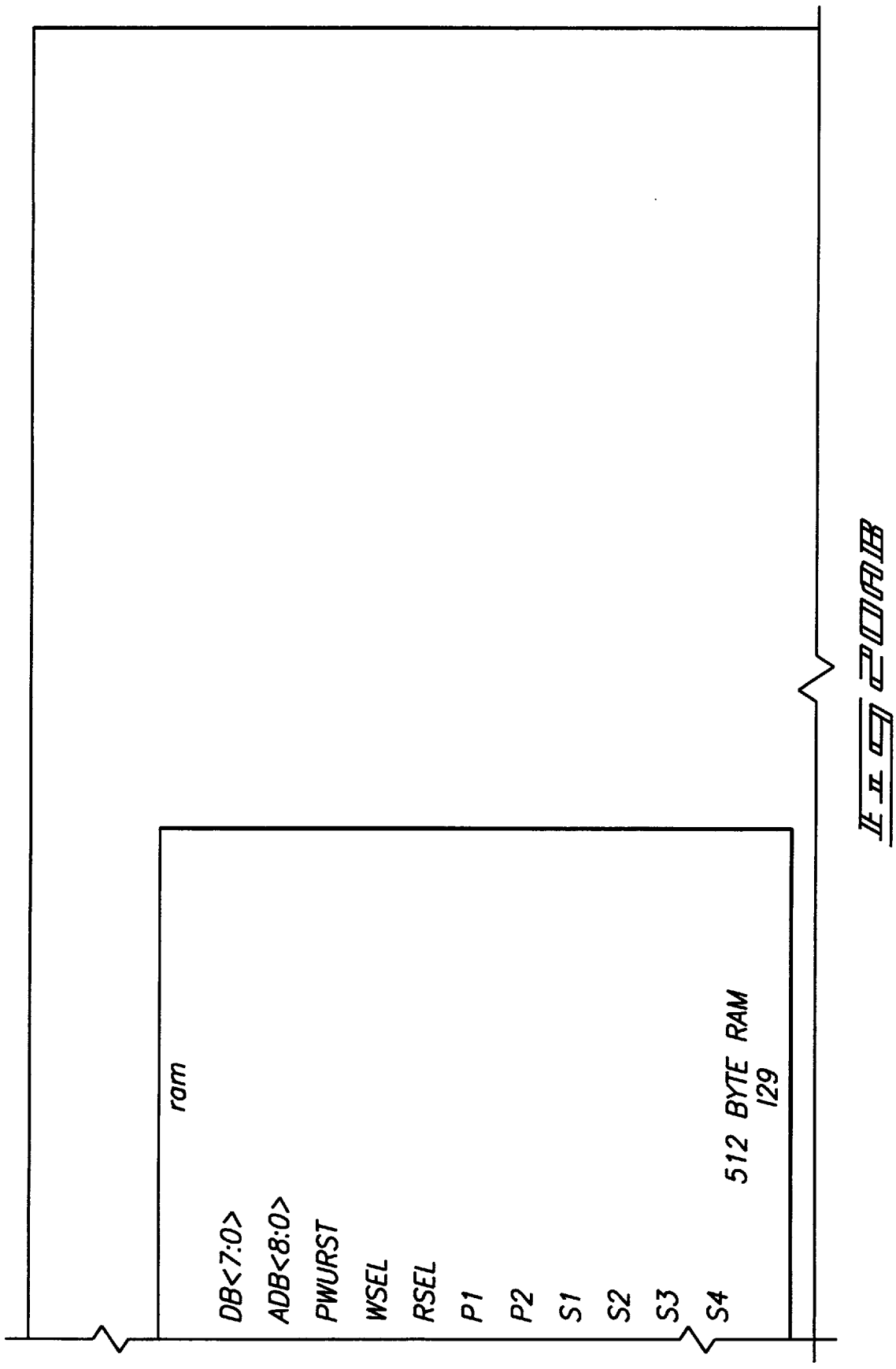
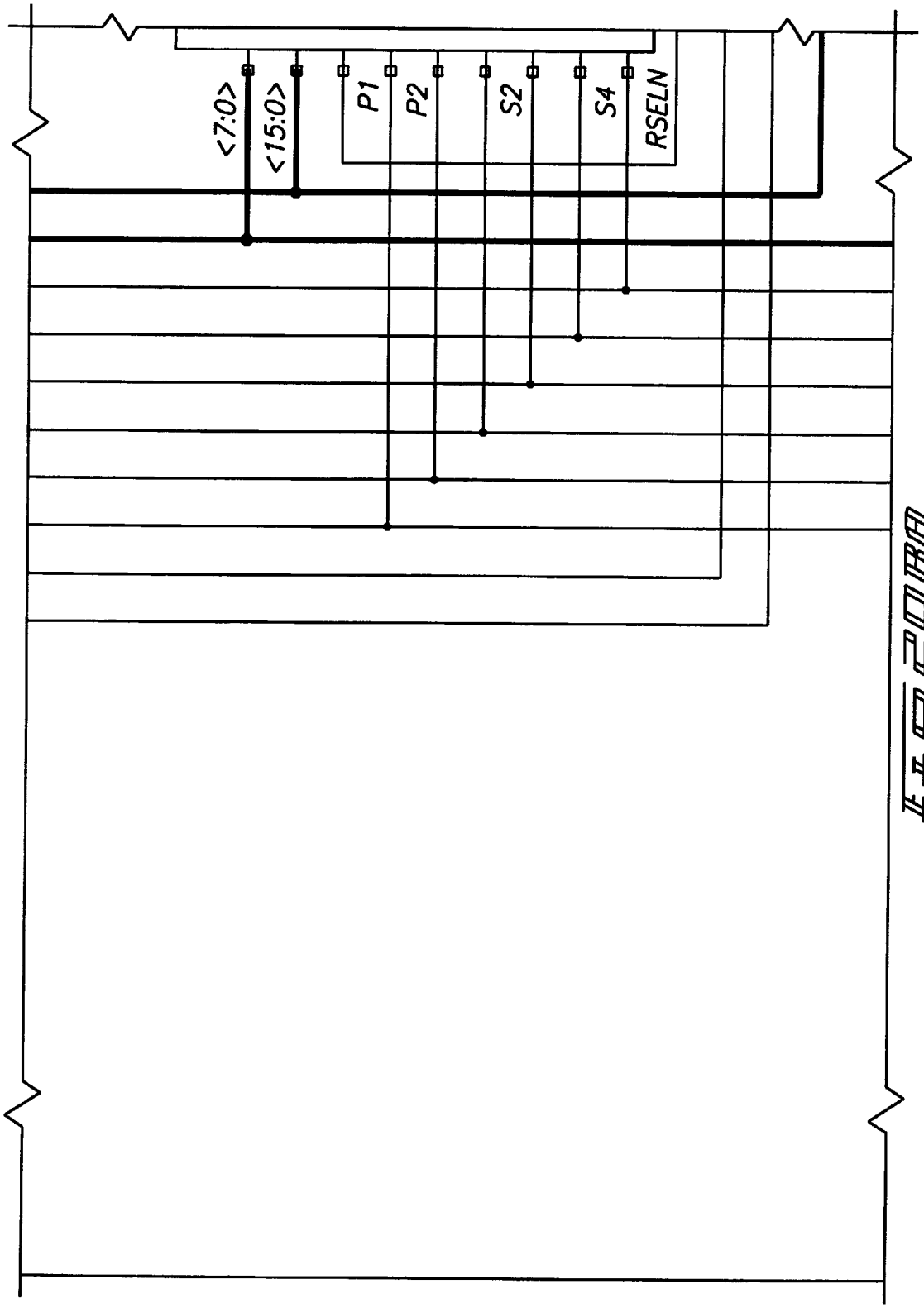


FIG 20AB
ram
DB<7:0>
ADB<8:0>
PWURST
WSEL
RSEL
P1
P2
S1
S2
S3
S4
512 BYTE RAM
129


<7:0>
<15:0>
P1
P2
S2
S4
RSELN
FIG 20BA

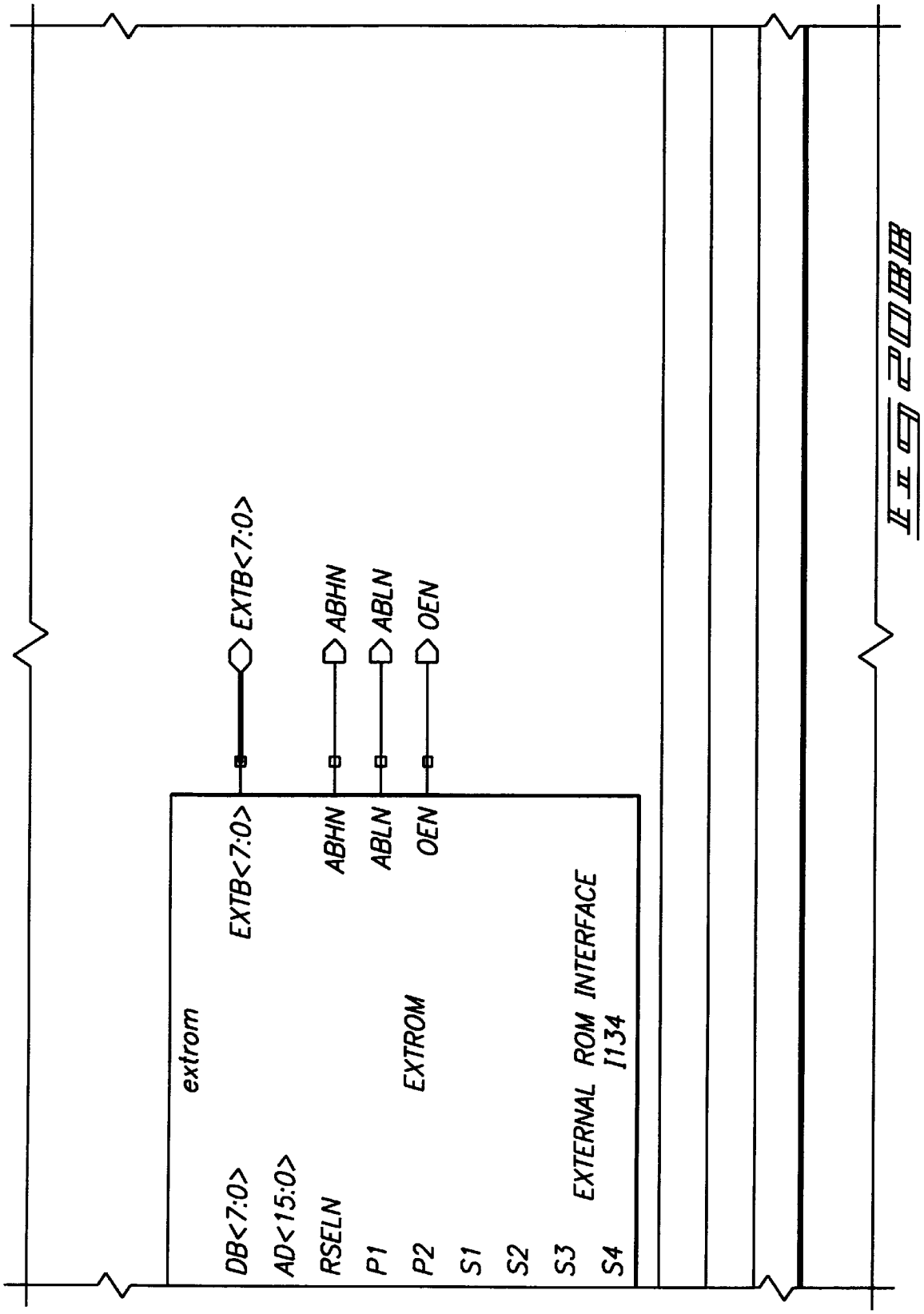

EXTB<7:0>
ABHN
ABLN
OEN
extrom
EXTB<7:0>
ABHN
ABLN
OEN
DB<7:0>
AD<15:0>
RSELN
P1
P2
S1
S2
S3
S4
EXTROM
EXTERNAL ROM INTERFACE
1134

FIG 2018

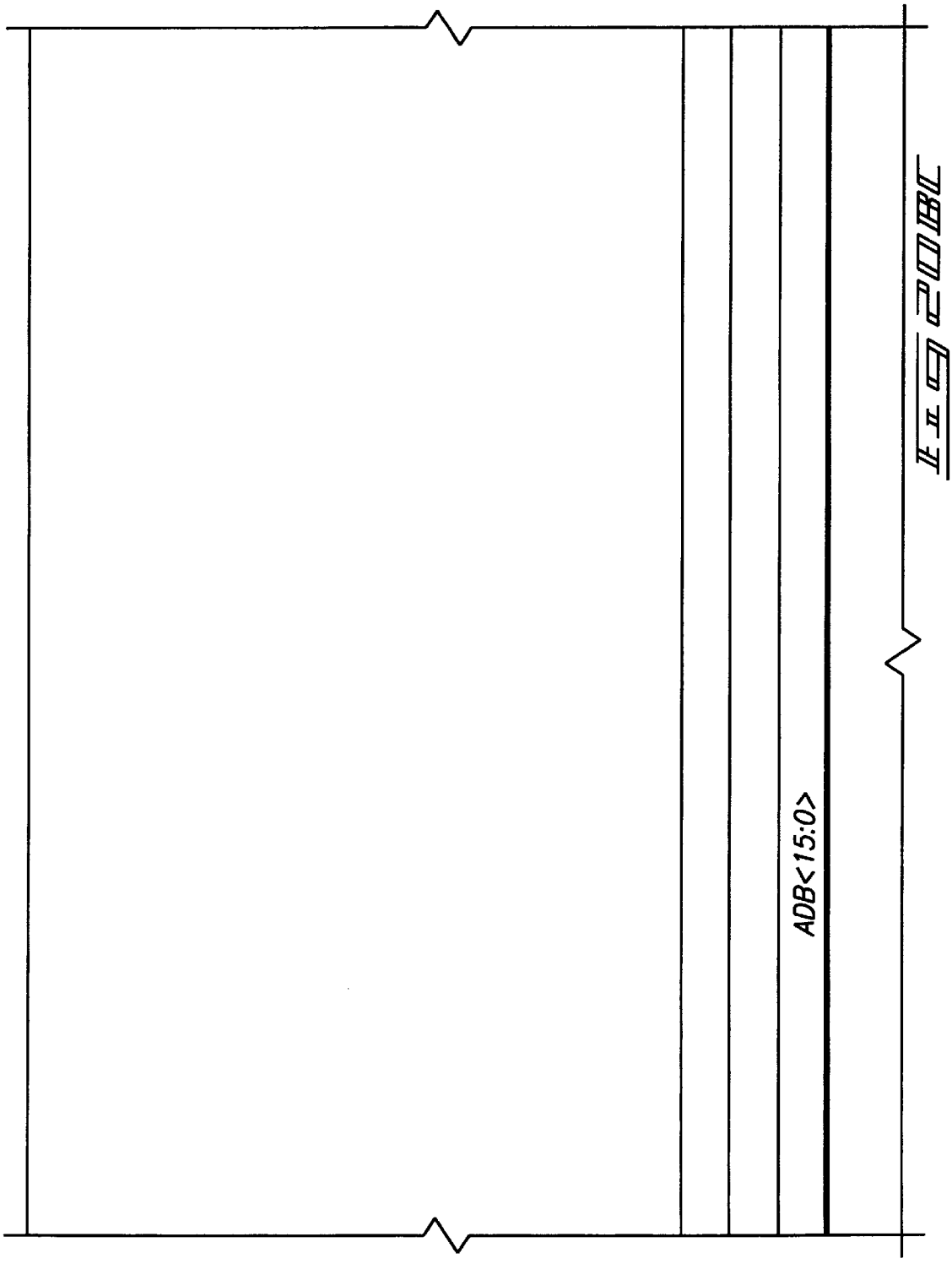


FIG 208C
ADB<15:0>

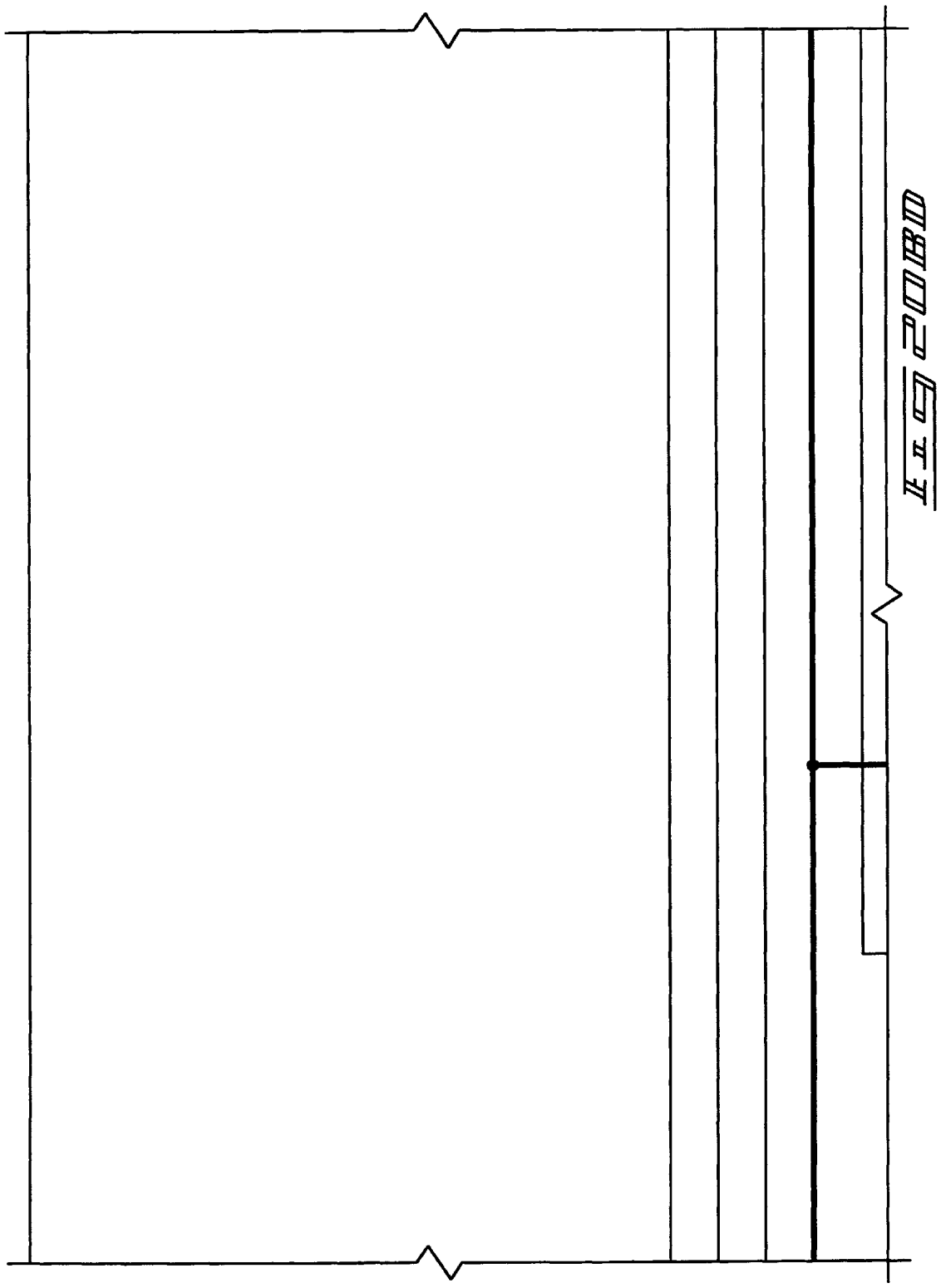
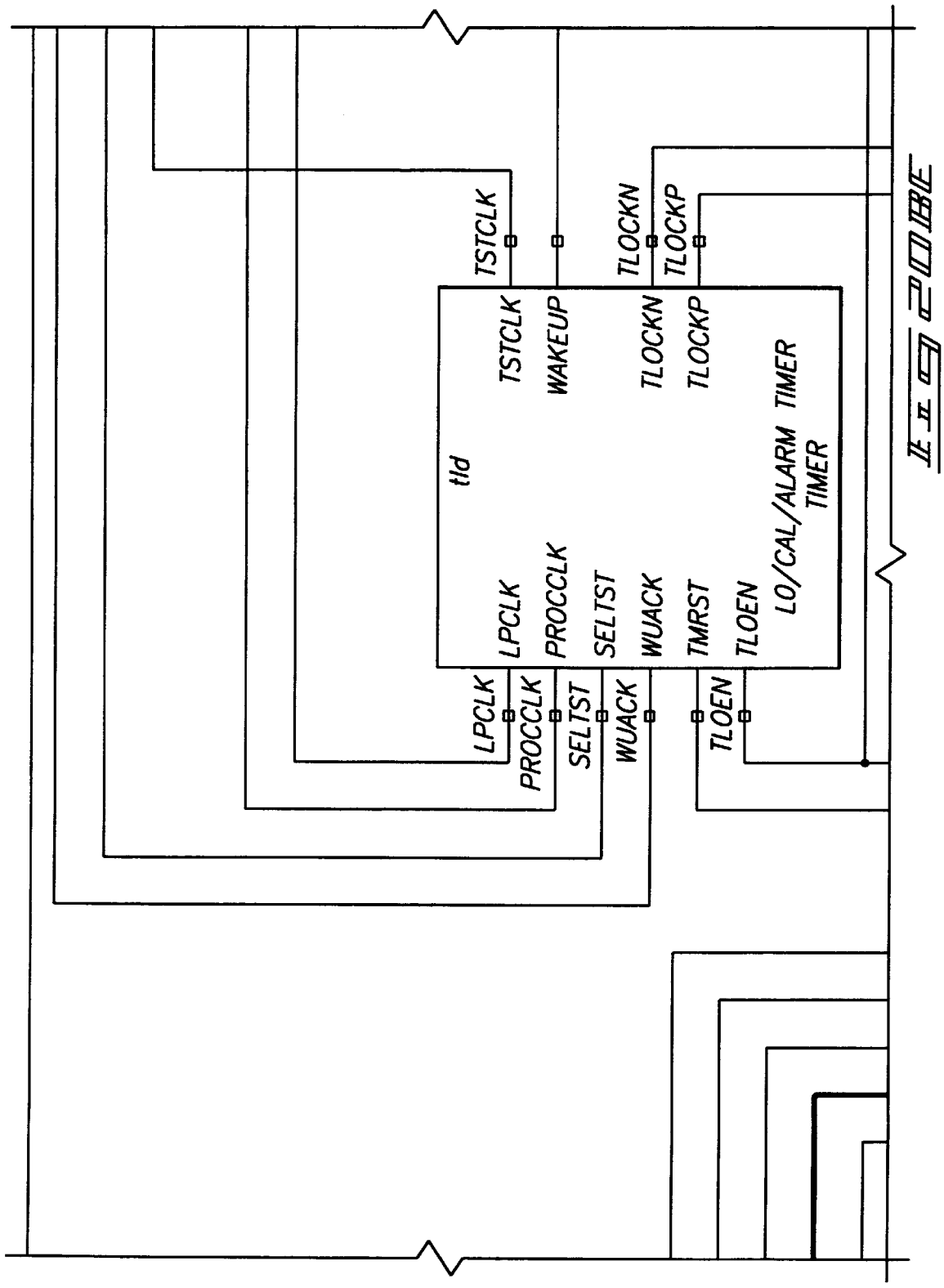


FIG 2080


TSTCLK
TLOCKN
TLOCKP
tld
TSTCLK
WAKEUP
TLOCKN
TLOCKP
TIMER
LO/CAL/ALARM
TIMER
LPCLK
PROCCLK
SELTST
WUACK
TMRST
TLOEN
LPCLK
PROCCLK
SELTST
WUACK
TLOEN

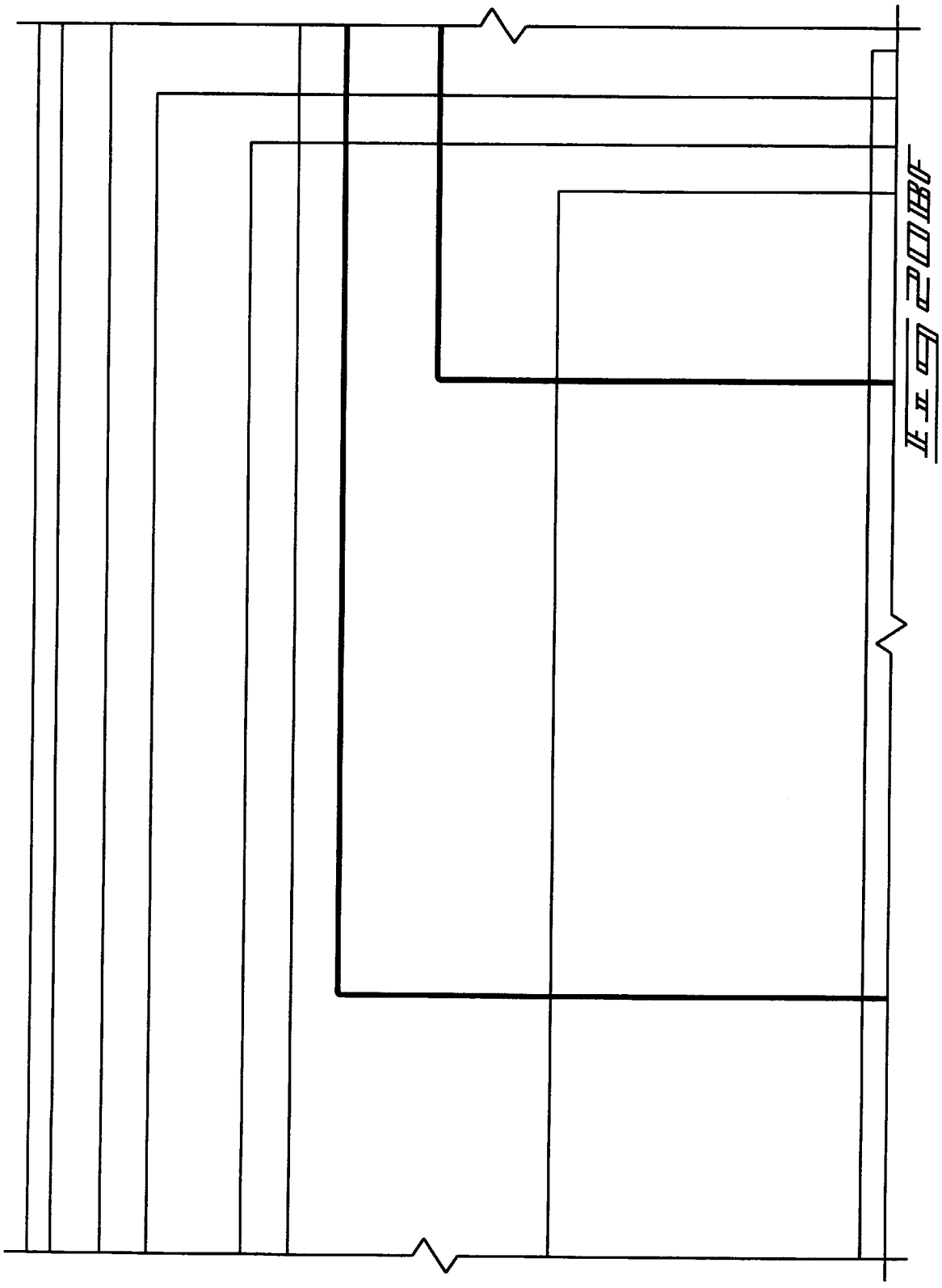


FIG 20BF

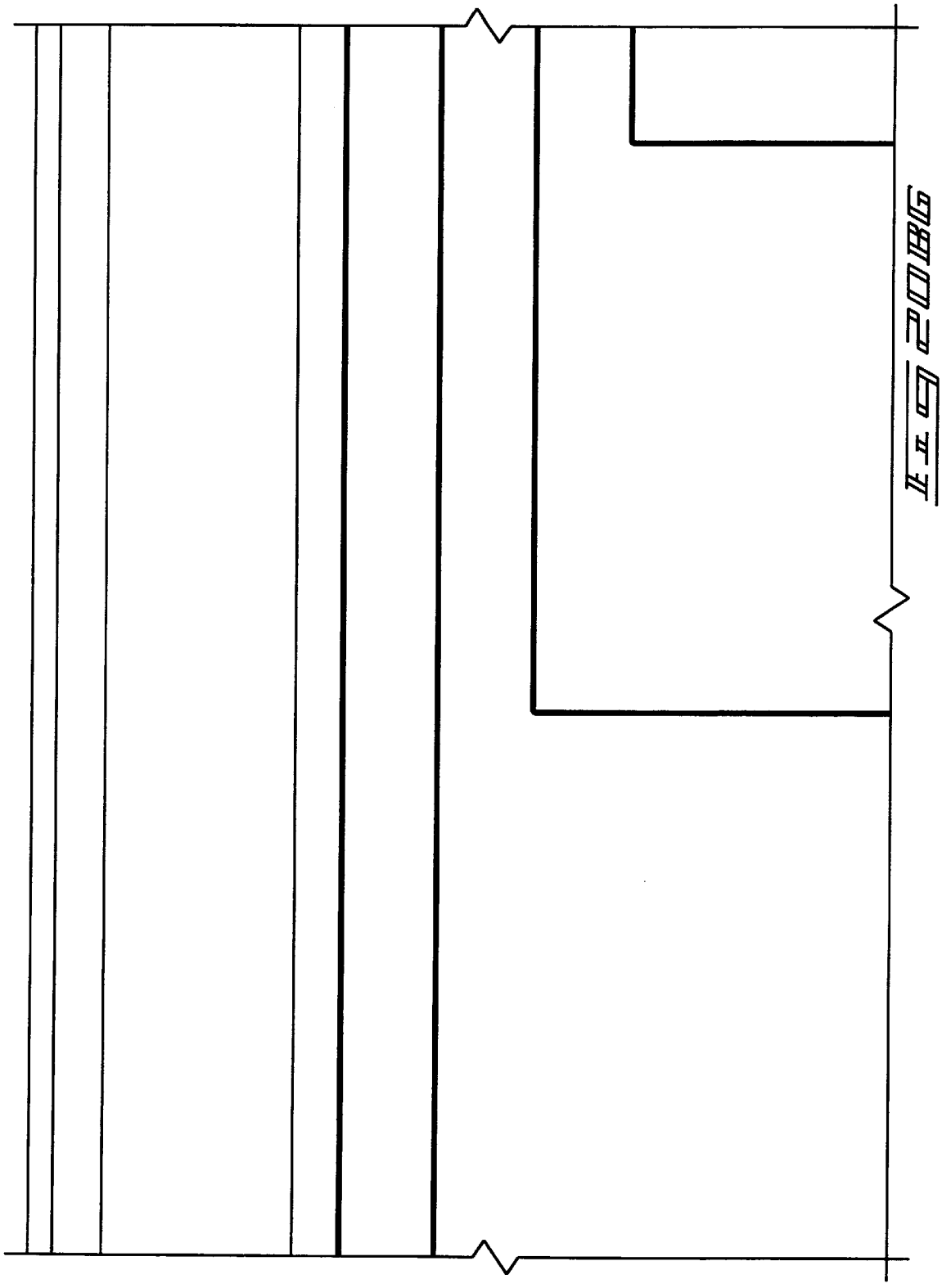


FIG 2086

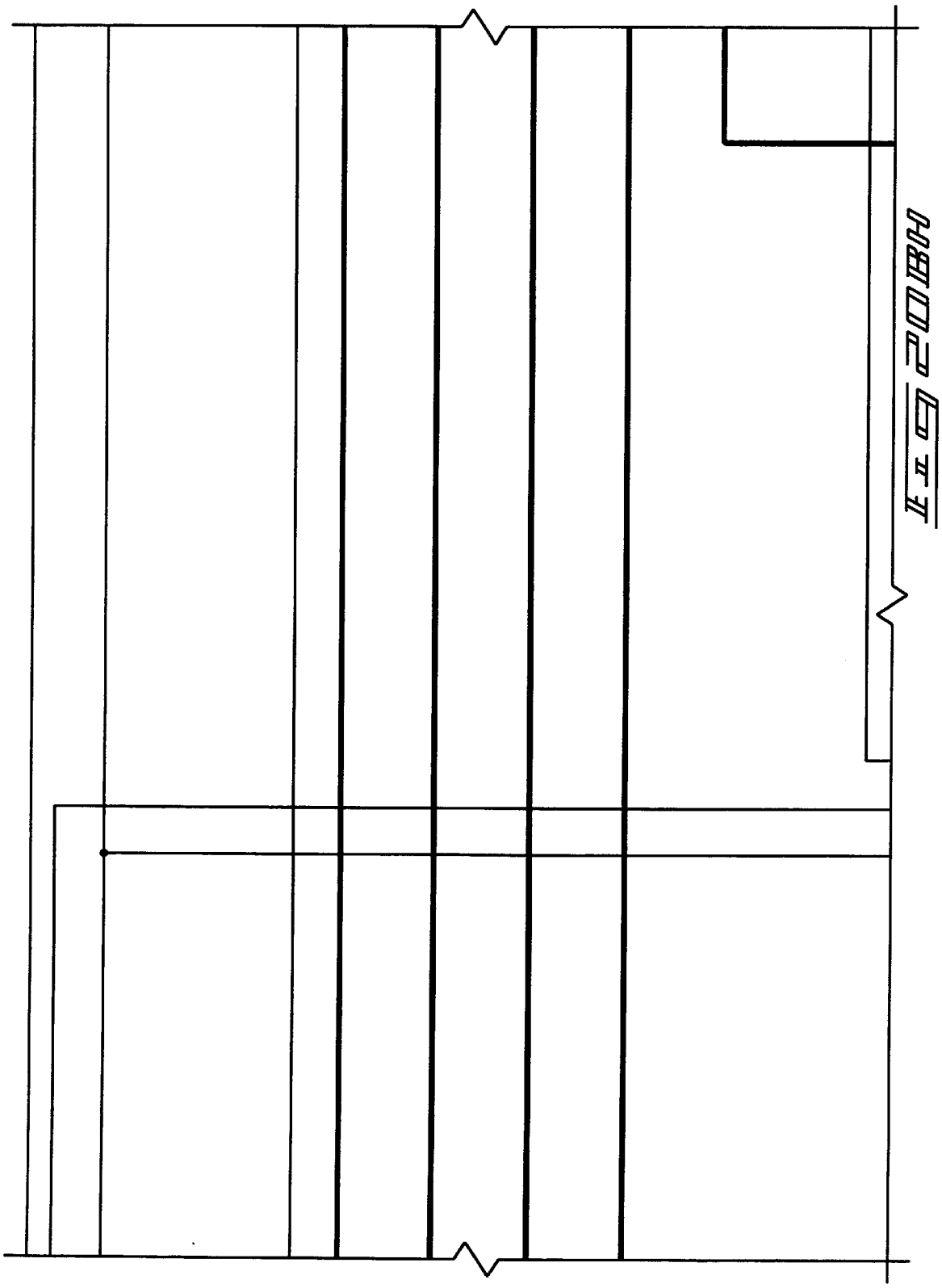


FIG 2800H

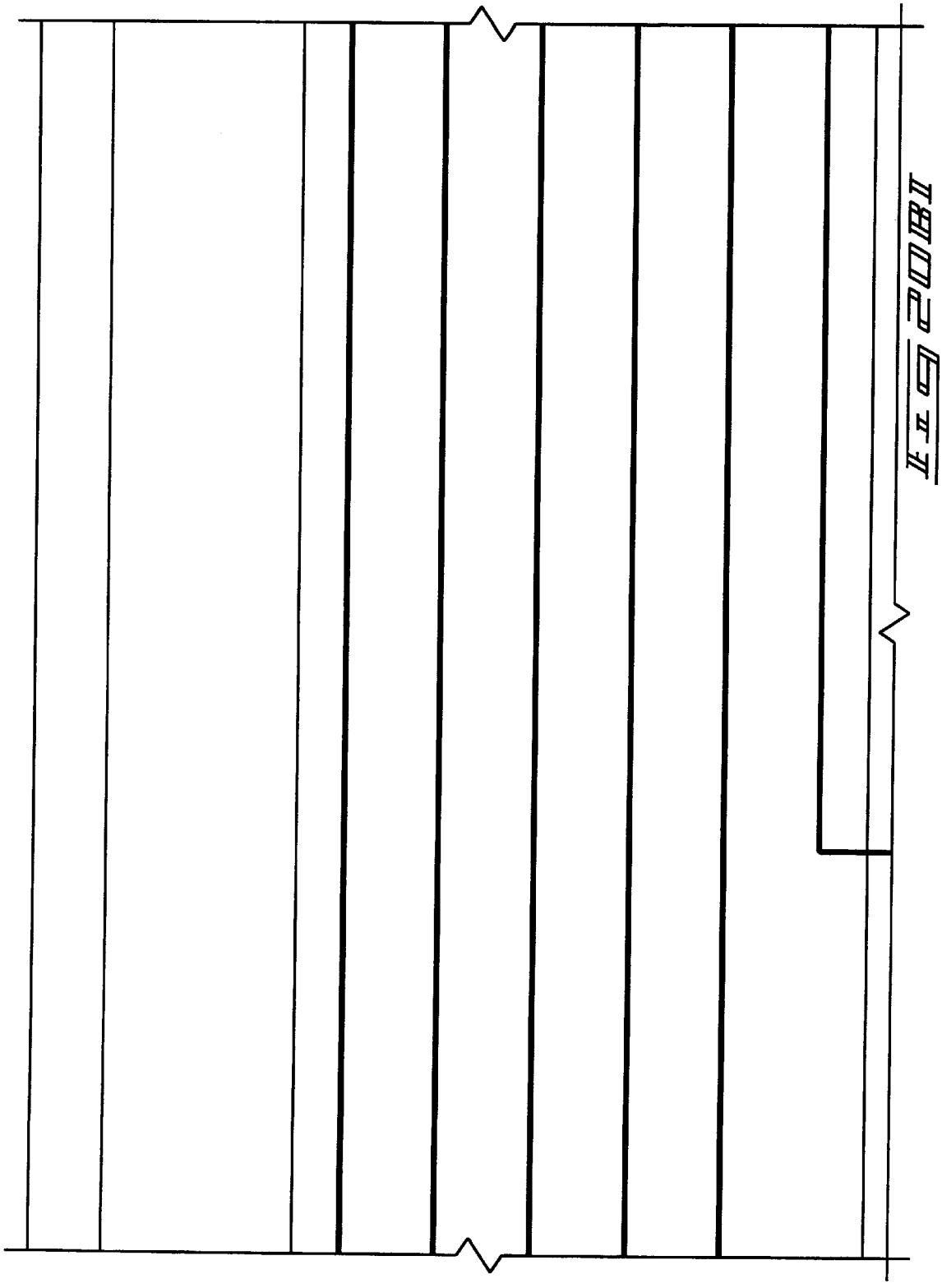


FIG 2802

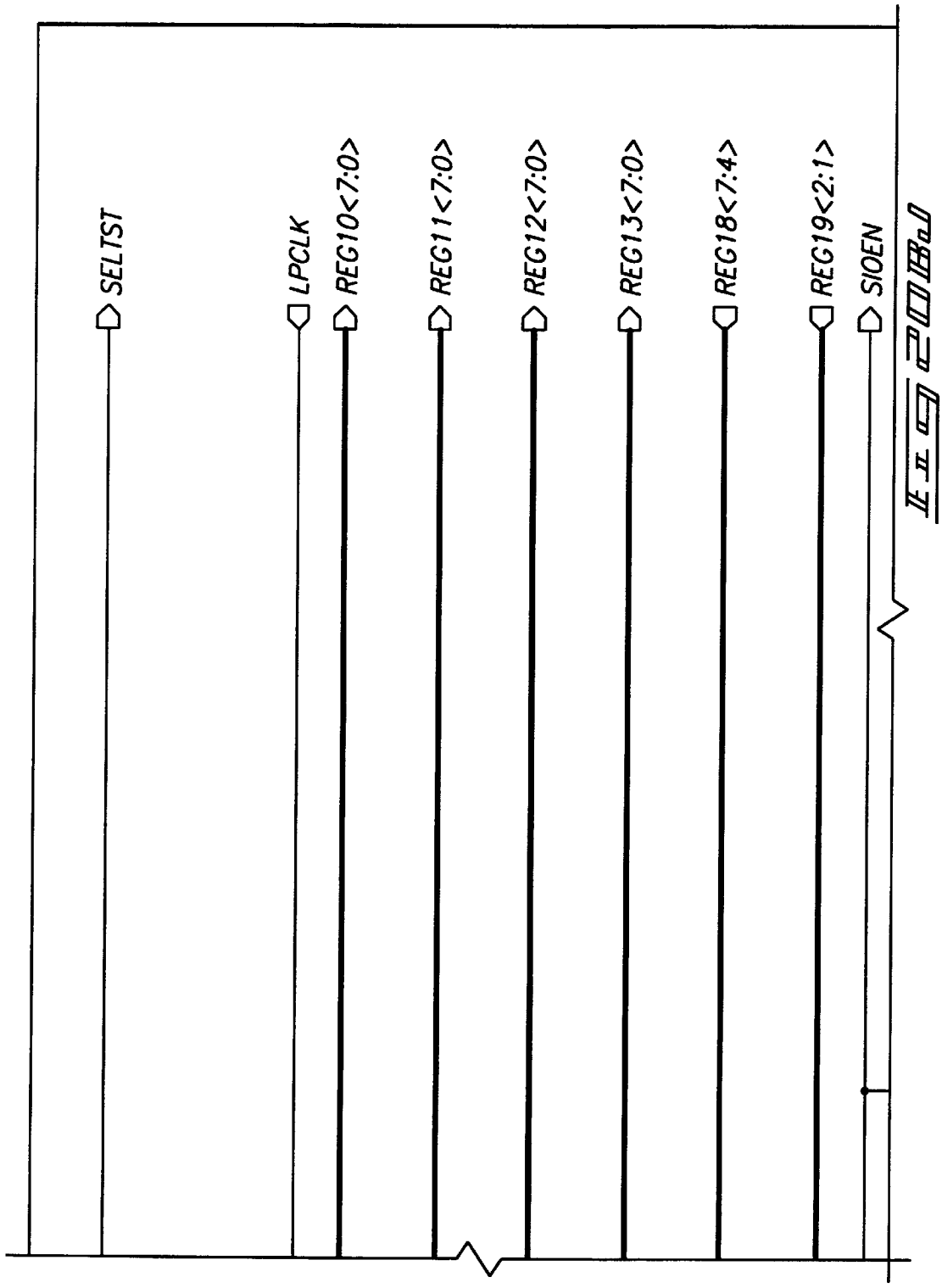
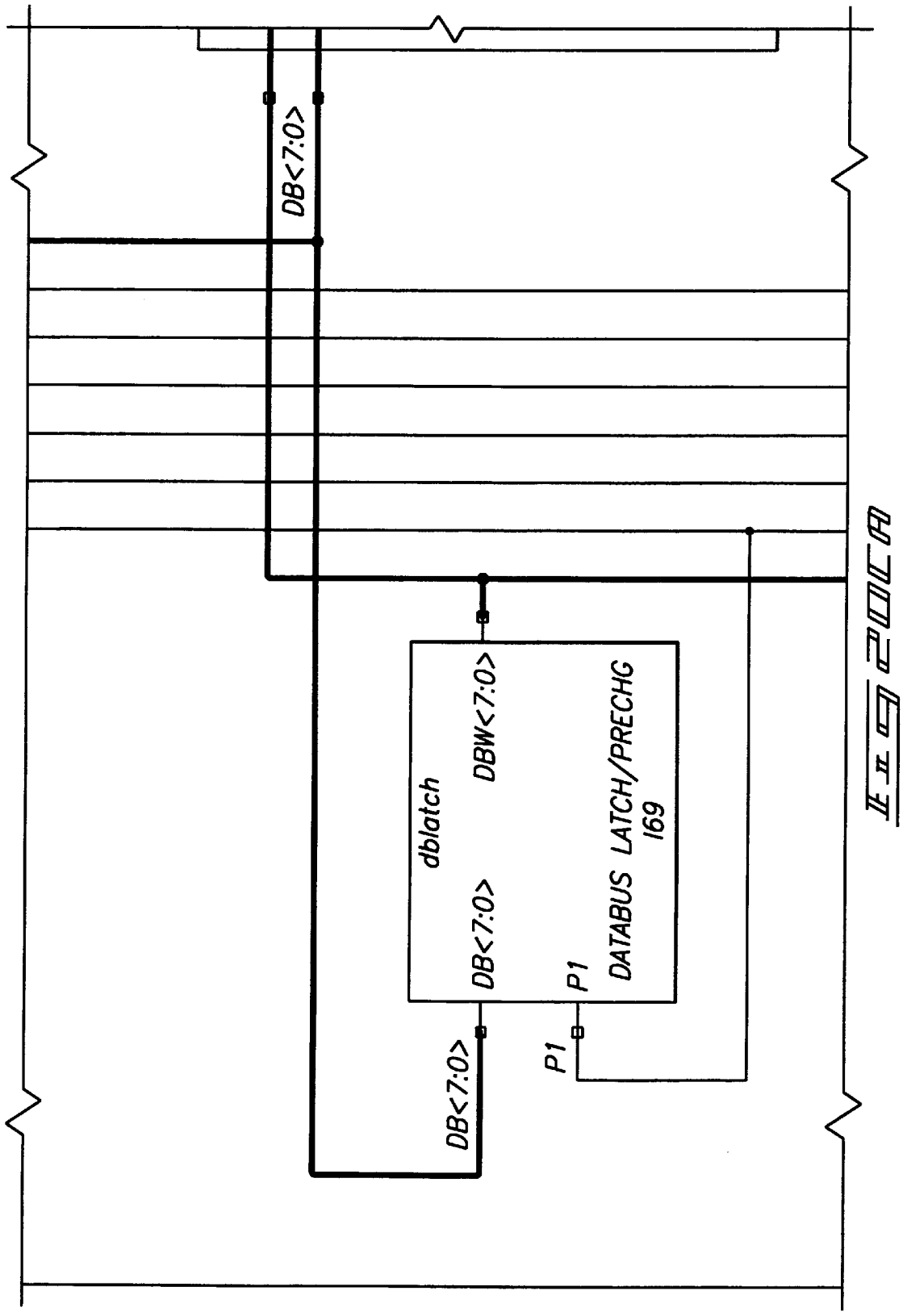
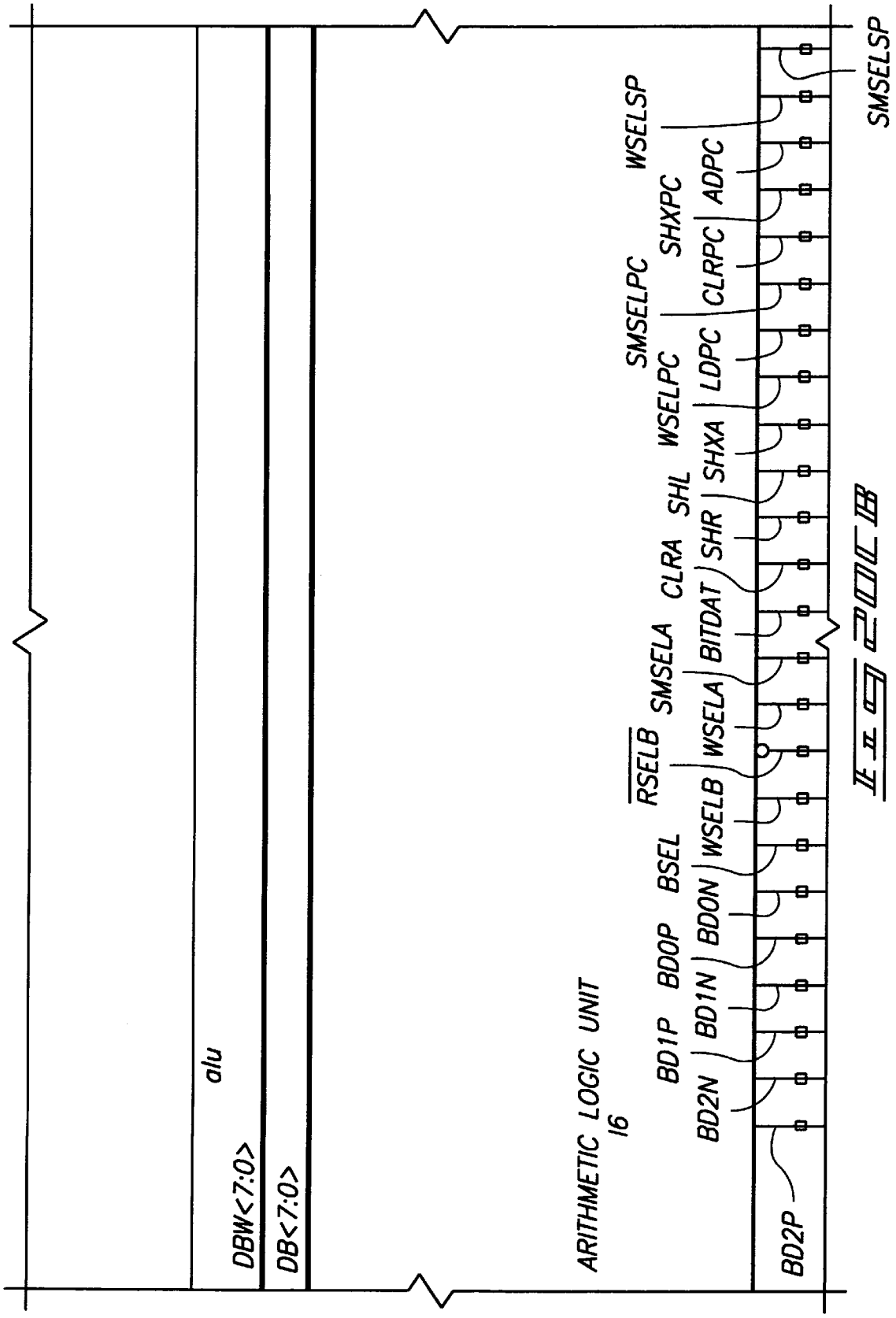
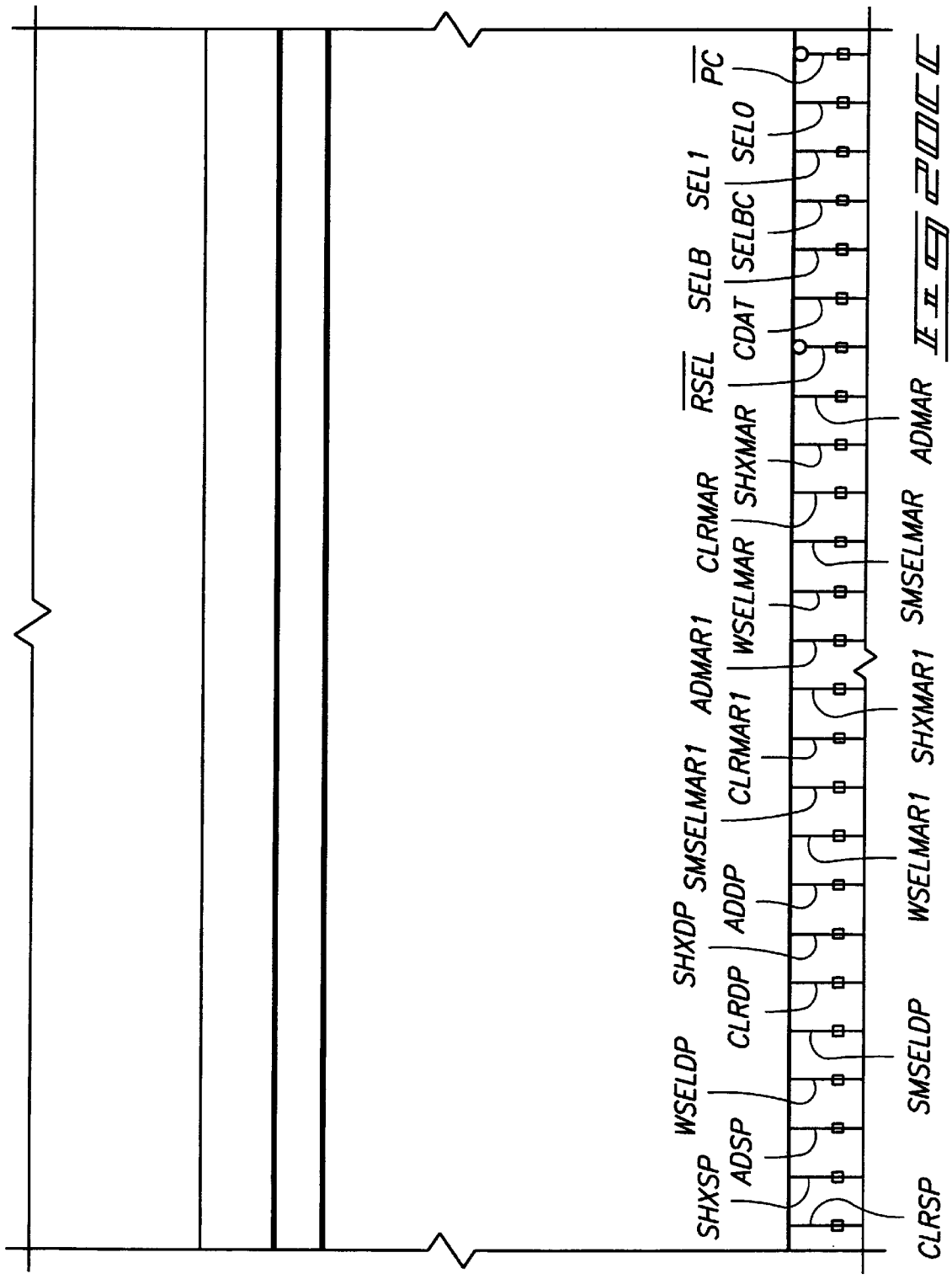
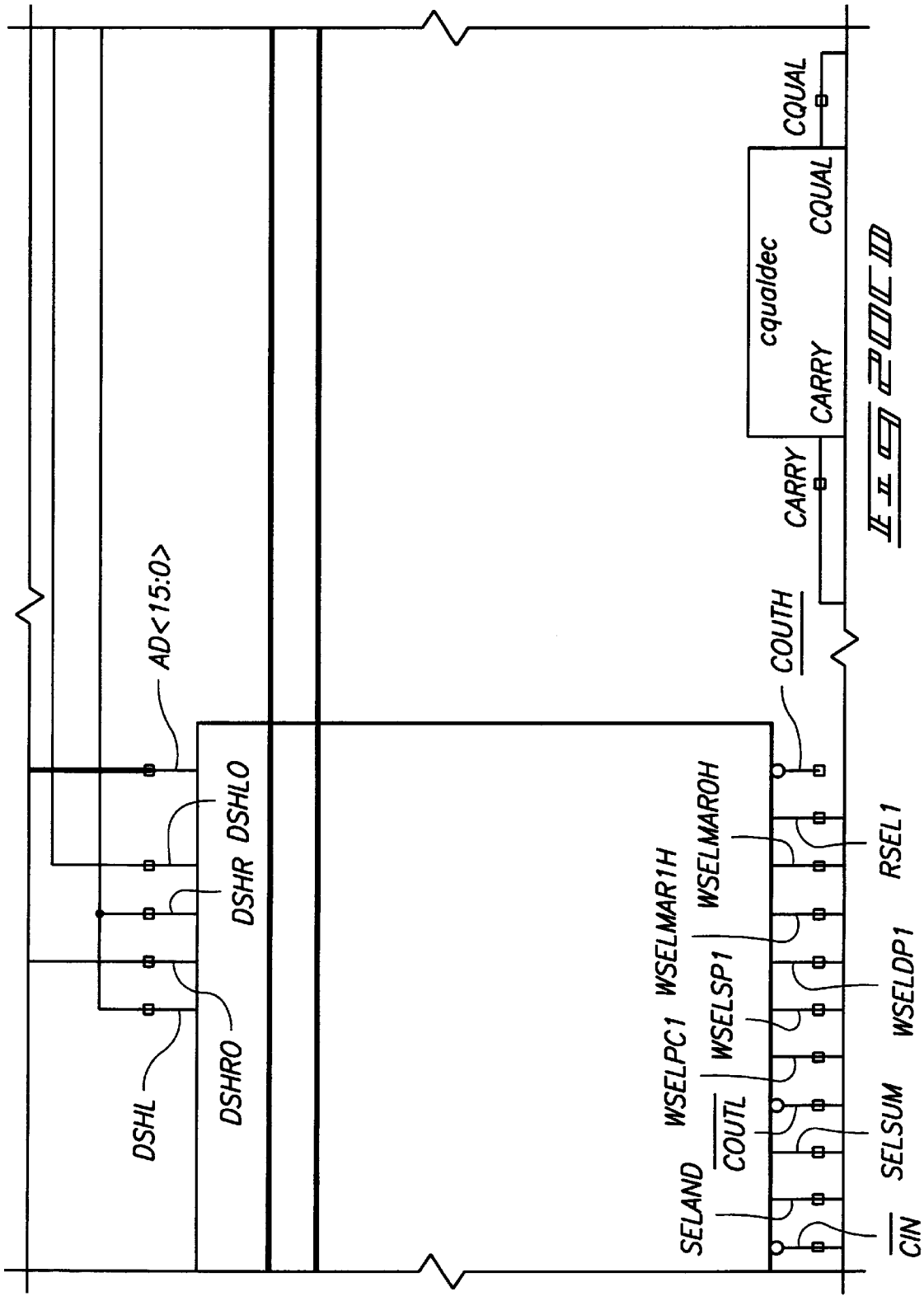

SELTST
LPCLK
REG10<7:0>
REG11<7:0>
REG12<7:0>
REG13<7:0>
REG18<7:4>
REG19<2:1>
SIOEN

FIG 2108


DB<7:0>
dblatch
DBW<7:0>
DB<7:0>
P1
DATABUS LATCH/PRECHG
169
P1
DB<7:0>
FIG 2005A


alu
DBW<7:0>
DB<7:0>
ARITHMETIC LOGIC UNIT
16
BD1P
BD2N
BD0P
BD1N
BSEL
BD0N
RSELB
WSELB
SMSELA
WSELA
CLRA
BITDAT
SHL
SHR
WSELPC
SHXA
SMSELPC
LDPC
SHXPC
CLRPC
WSELSP
ADPC
BD2P
SMSELSP


PC
SEL0
SEL1
SELBC
SELB
CDAT
RSEL
SHXMAR
CLRMAR
WSELMAR
ADMAR1
SMSELMAR1
CLRMAR1
ADDP
SHXDP
CLRDP
WSELDP
ADSP
SHXSP
ADMAR
SMSELMAR
SHXMAR1
WSELMAR1
SMSELDP
CLRSP


AD<15:0>
DSHL
DSHRO
DSHR
DSHLO
SELAND
COUTL
WSELPC1
WSELMAR1H
WSELSP1
WSELMAROH
WSELDP1
RSEL1
SELSUM
CIN
COUTH
CARRY
cqualdec
CARRY
CQUAL
CQUAL
FIG 2D1C 1D

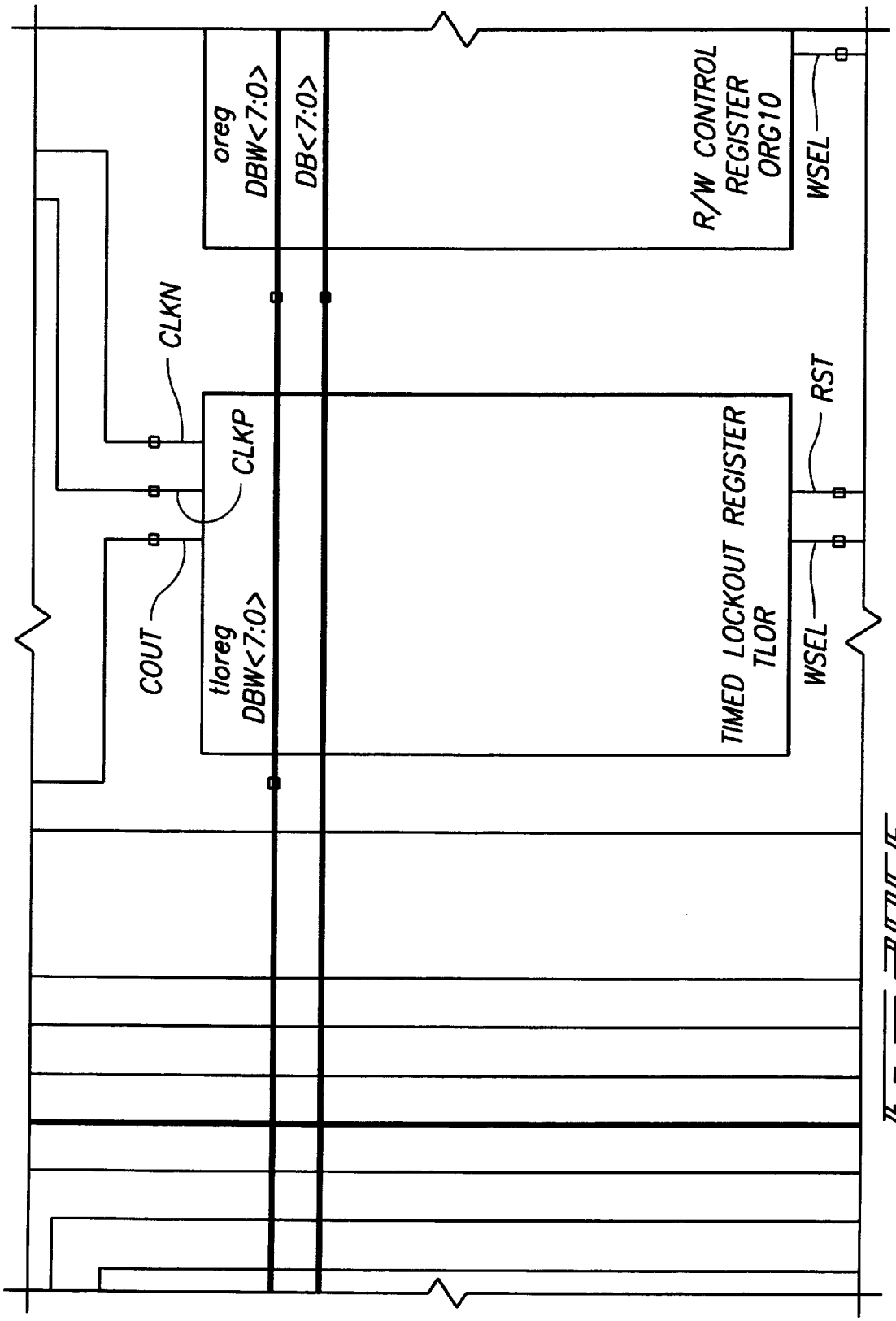

oreg
DBW<7:0>
DB<7:0>
R/W CONTROL
REGISTER
ORG10
WSEL
CLKN
CLKP
RST
COUT
tloreg
DBW<7:0>
TIMED LOCKOUT REGISTER
TLOR
WSEL

FIG 200E

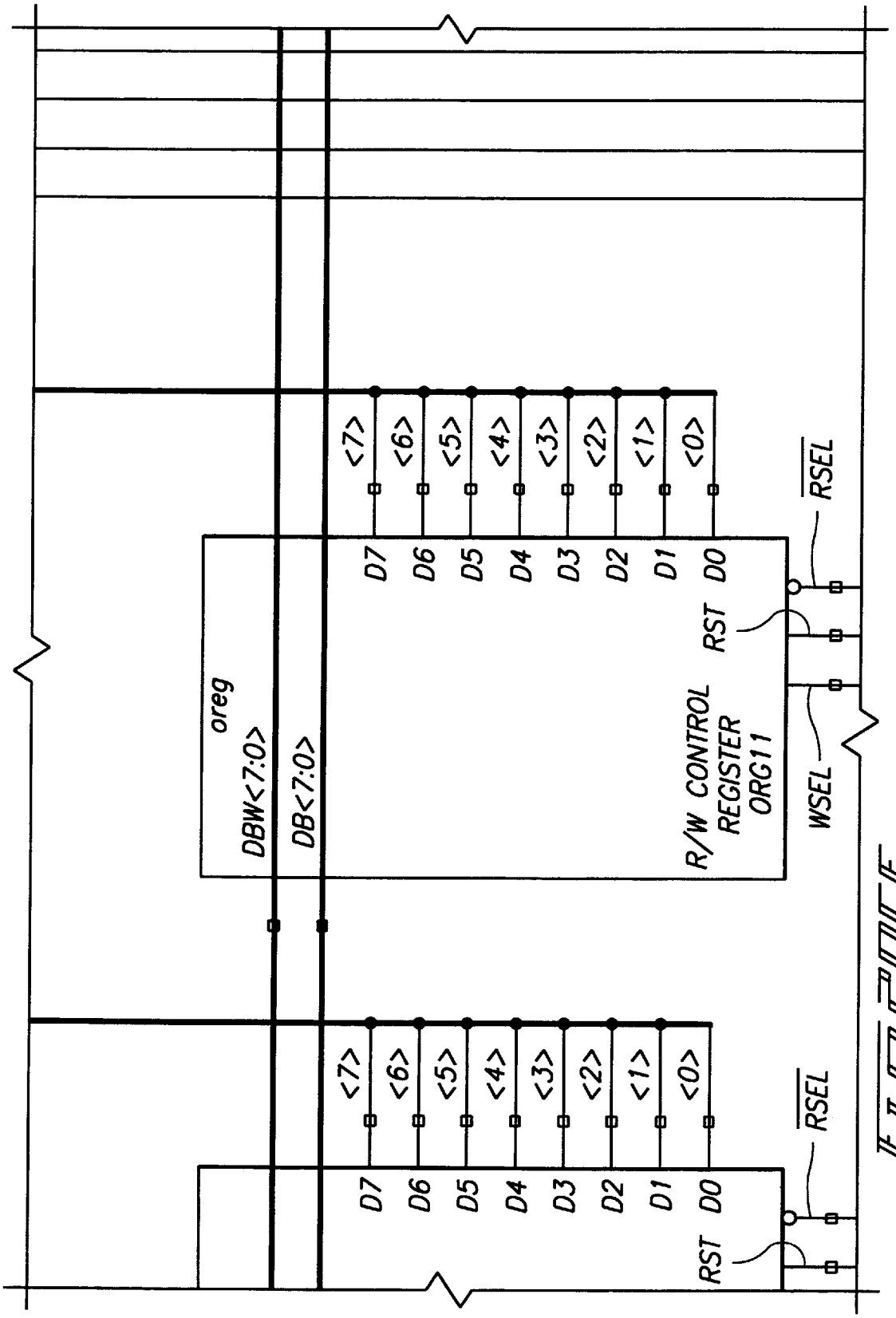

<7>
<6>
<5>
<4>
<3>
<2>
<1>
<0>
D7
D6
D5
D4
D3
D2
D1
D0
RSEL
RST
WSEL
R/W CONTROL REGISTER ORG11
oreg
DBW<7:0>
DB<7:0>

FIG 2100F

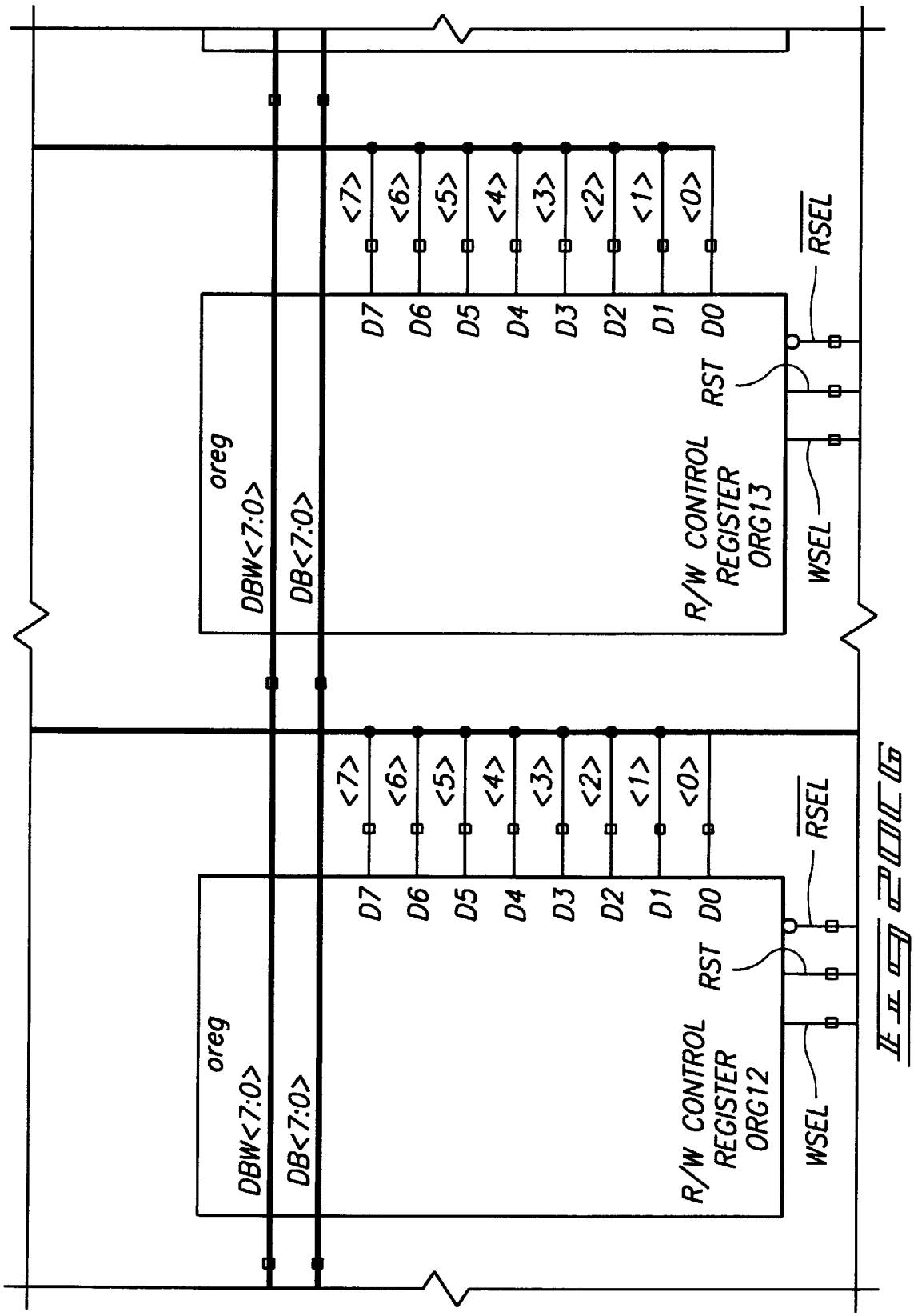

<7>
<6>
<5>
<4>
<3>
<2>
<1>
<0>
D7
D6
D5
D4
D3
D2
D1
D0
RSEL
RST
WSEL
oreg
DBW<7:0>
DB<7:0>
R/W CONTROL REGISTER ORG13
R/W CONTROL REGISTER ORG12

FIG 2006

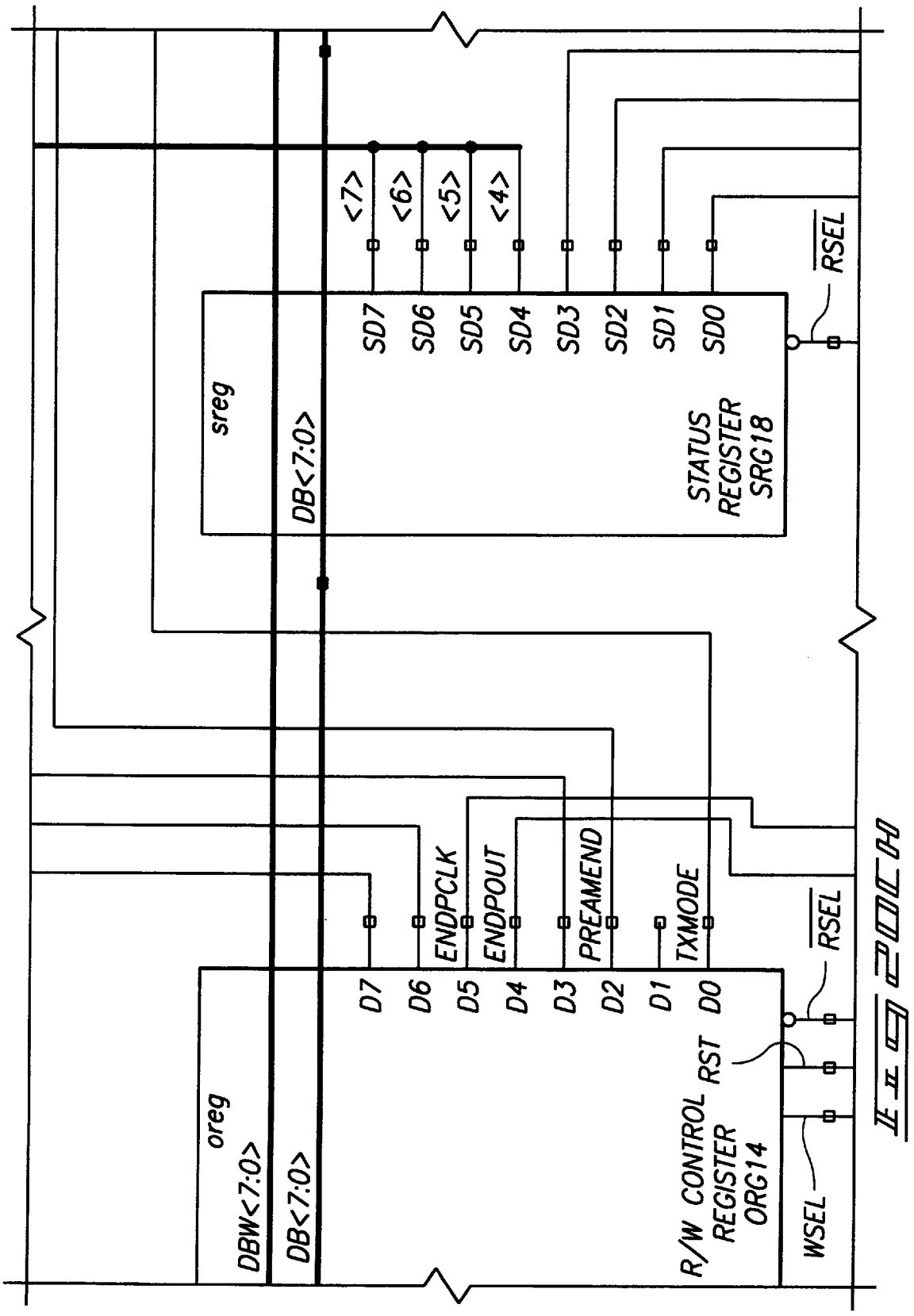

<7>
<6>
<5>
<4>
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
RSEL
sreg
DB<7:0>
STATUS REGISTER SRG18
D7
D6
D5
D4
D3
D2
D1
D0
ENDPCLK
ENDPOUT
PREAMEND
TXMODE
RSEL
RST
WSEL
oreg
DBW<7:0>
DB<7:0>
R/W CONTROL REGISTER ORG14

FIG 200H

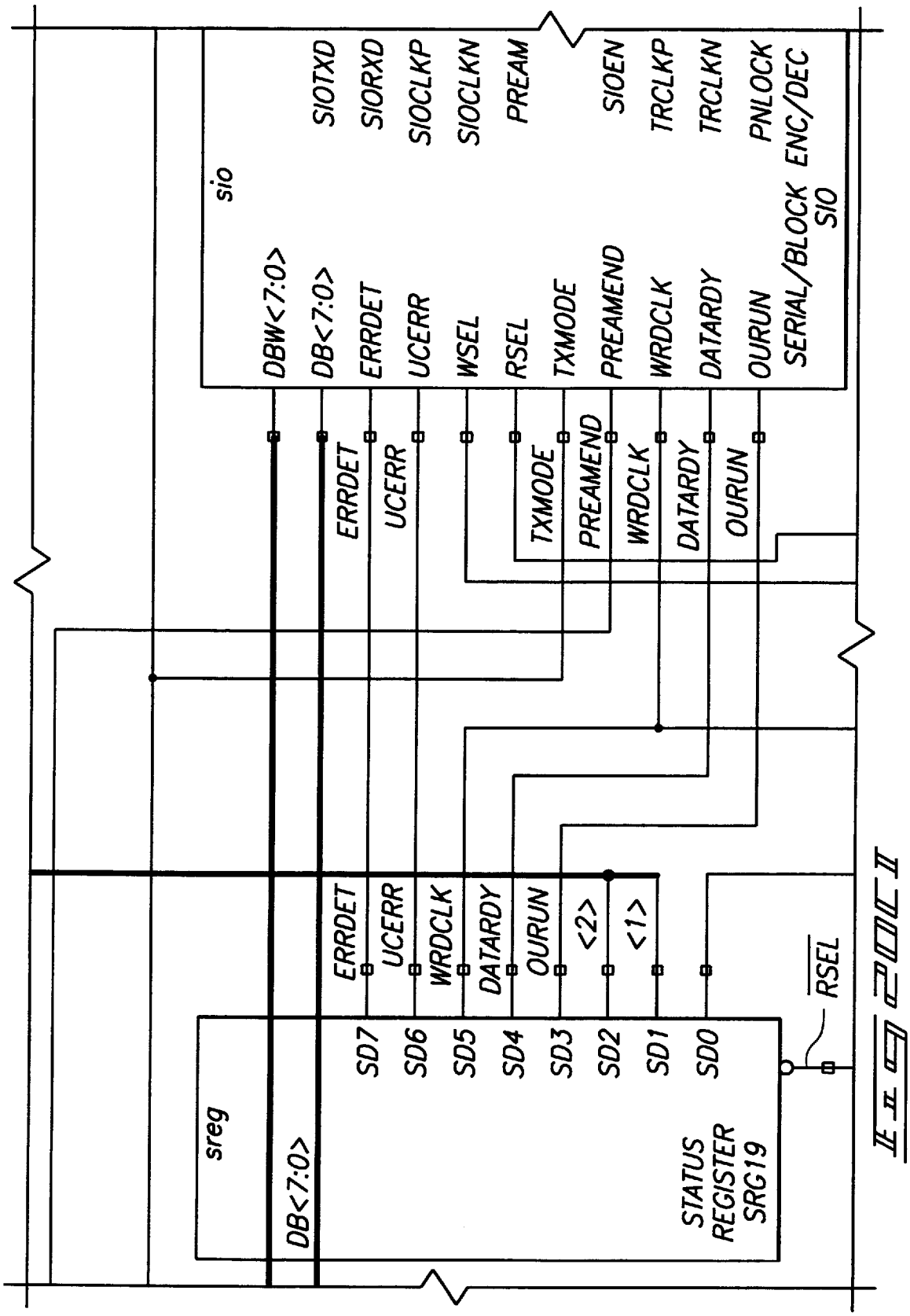

sio
SIOTXD
SIORXD
SIOCLKP
SIOCLKN
PREAM
SIOEN
TRCLKP
TRCLKN
PNLOCK
ENC/DEC
SIO
SERIAL/BLOCK
OURUN
DATARDY
WRDCLK
PREAMEND
TXMODE
RSEL
WSEL
UCERR
ERRDET
DB<7:0>
DBW<7:0>
sreg
STATUS REGISTER SRG19
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
<1>
<2>
RSEL

FIG 2

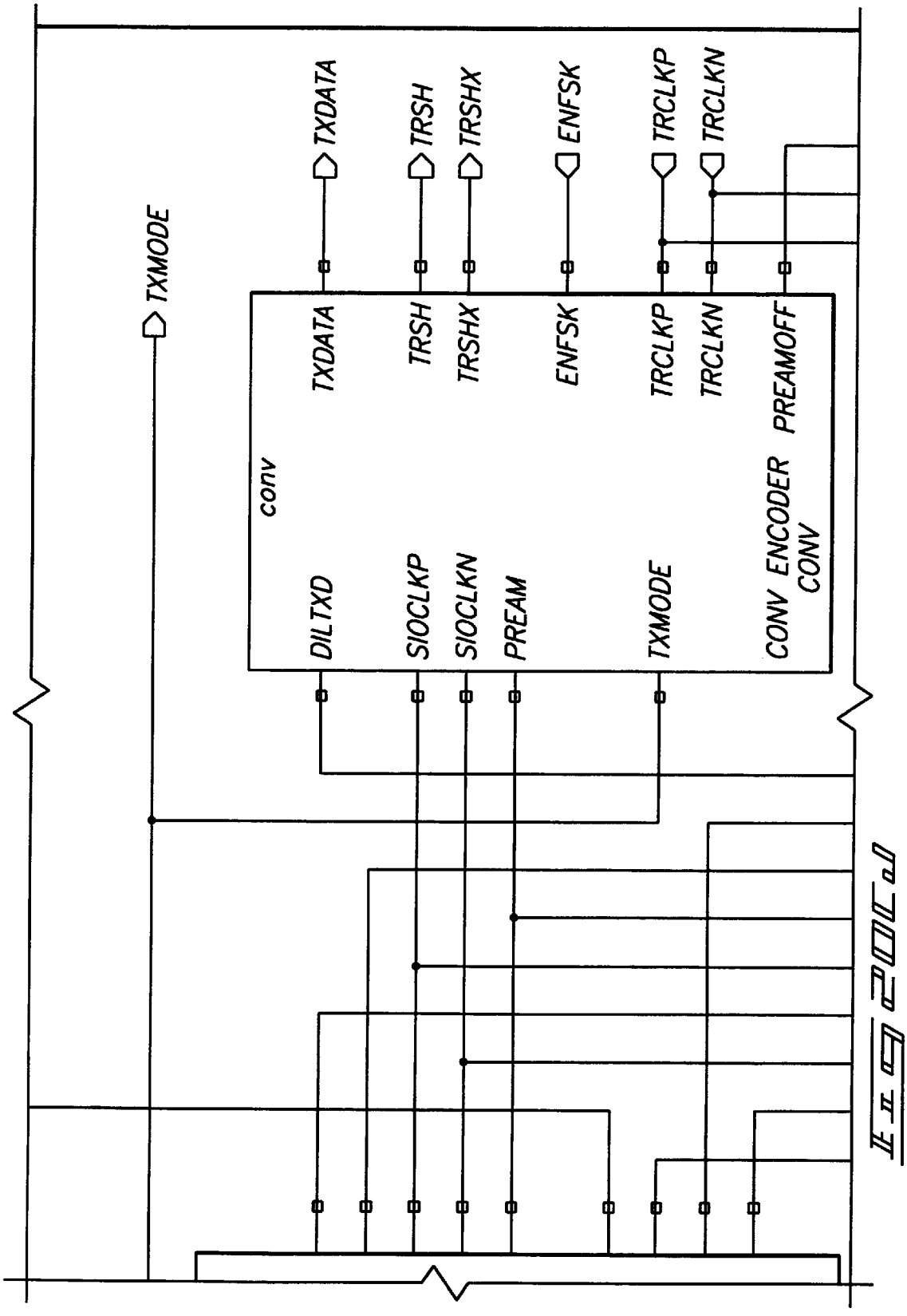

TXMODE
TXDATA
TRSH
TRSHX
ENFSK
TRCLKP
TRCLKN
conv
TXDATA
TRSH
TRSHX
ENFSK
TRCLKP
TRCLKN
PREAMOFF
DILTXD
SIOCLKP
SIOCLKN
PREAM
TXMODE
CONV ENCODER CONV

FIG 2003

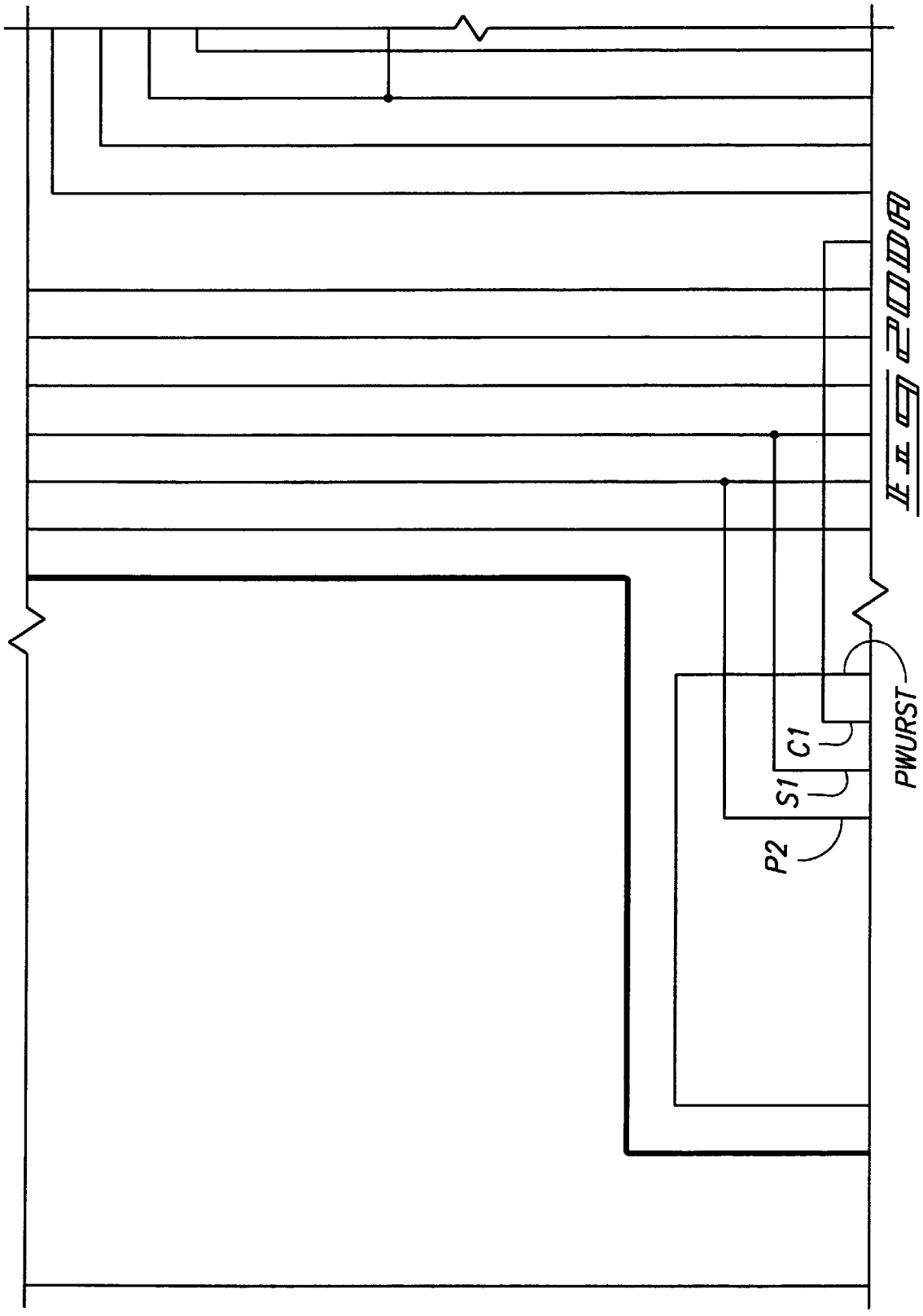


FIG 200A
PWURST
C1
S1
P2

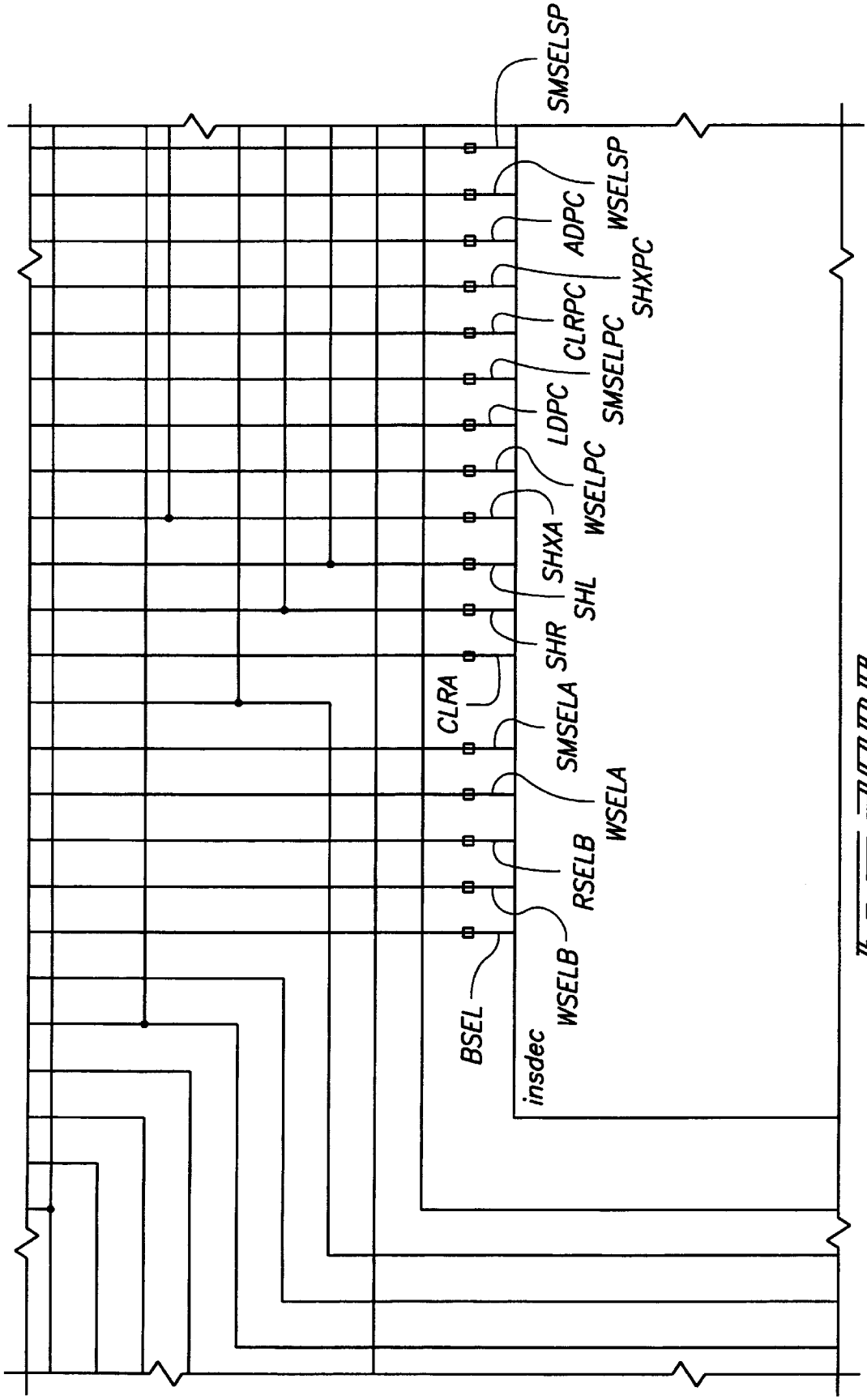

SMSELSP
WSELSP
ADPC
SHXPC
CLRPC
SMSELPC
LDPC
WSELPC
SHXA
SHL
SHR
SMSELA
CLRA
WSELA
RSELB
WSELB
BSEL
insdec

Fig 2008

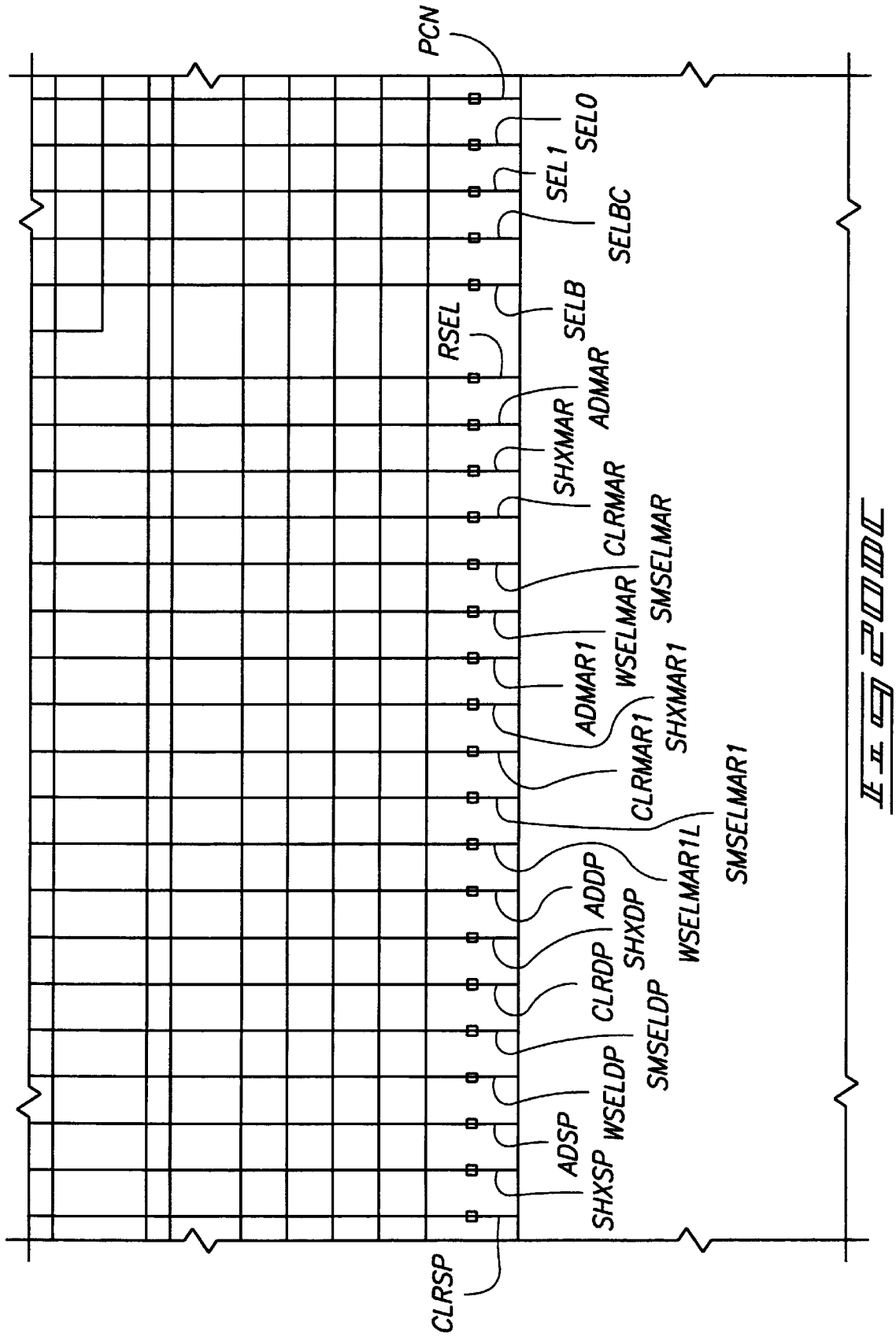
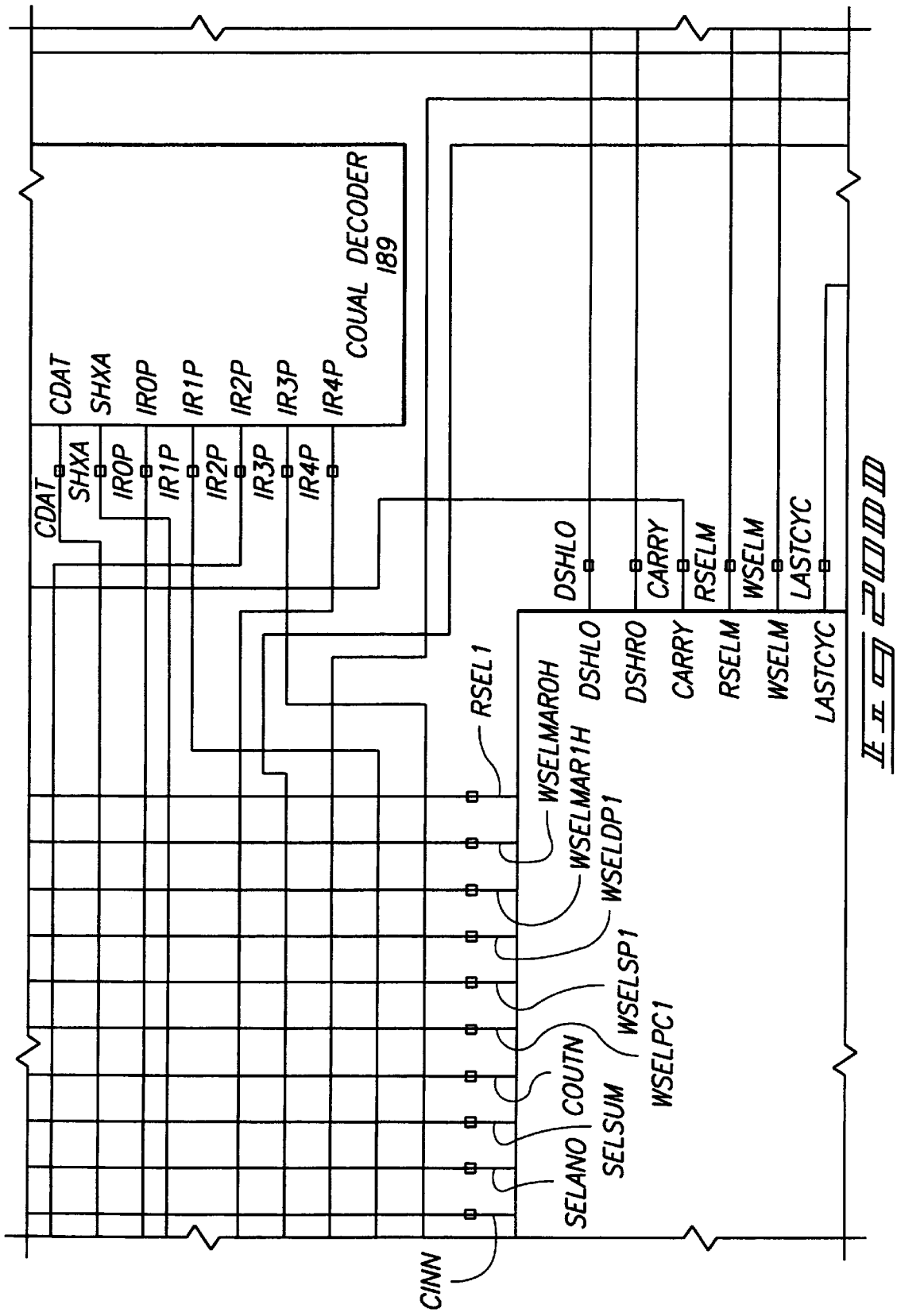
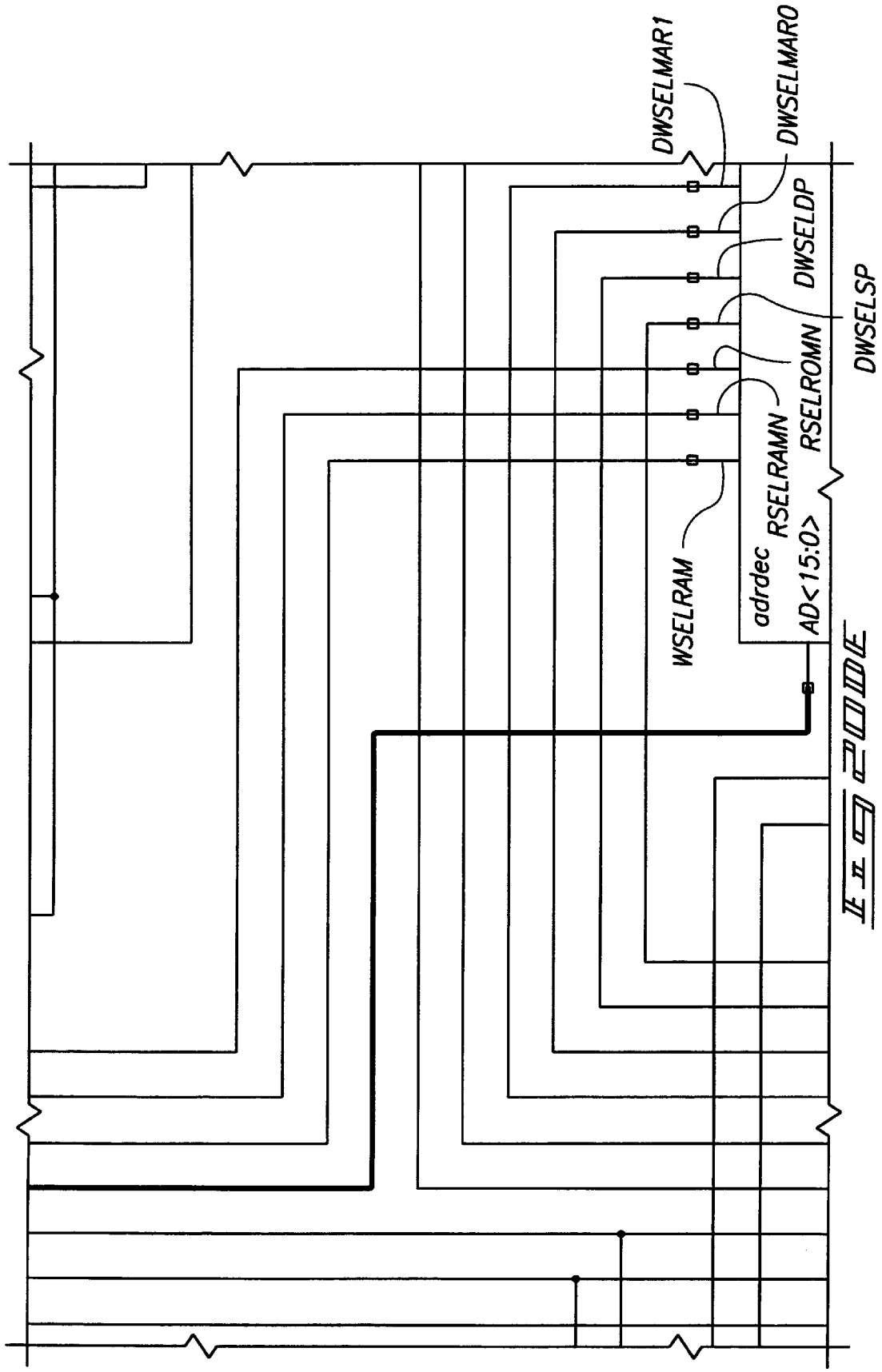

PCN
SEL0
SEL1
SELBC
SELB
RSEL
ADMAR
SHXMAR
CLRMAR
SMSELMAR
WSELMAR
ADMAR1
SHXMAR1
CLRMAR1
SMSELMAR1
WSELMAR1L
ADDP
SHXDP
CLRDP
SMSELDP
WSELDP
ADSP
SHXSP
CLRSP

FIG 2001


COUAL DECODER 189
CDAT
SHXA
IR0P
IR1P
IR2P
IR3P
IR4P
DSHLO
CARRY
RSELM
WSELM
LASTCYC
RSEL1
WSELMAR0H
WSELMAR1H
WSELDP1
WSELSP1
WSELPC1
COUTN
SELSUM
SELANO
CINN
FIG 2000


DWSELMAR1
DWSELMAR0
DWSELDP
DWSELSP
RSELROMN
RSELRAMN
adrdec
AD<15:0>
WSELRAM
FIG 2000E

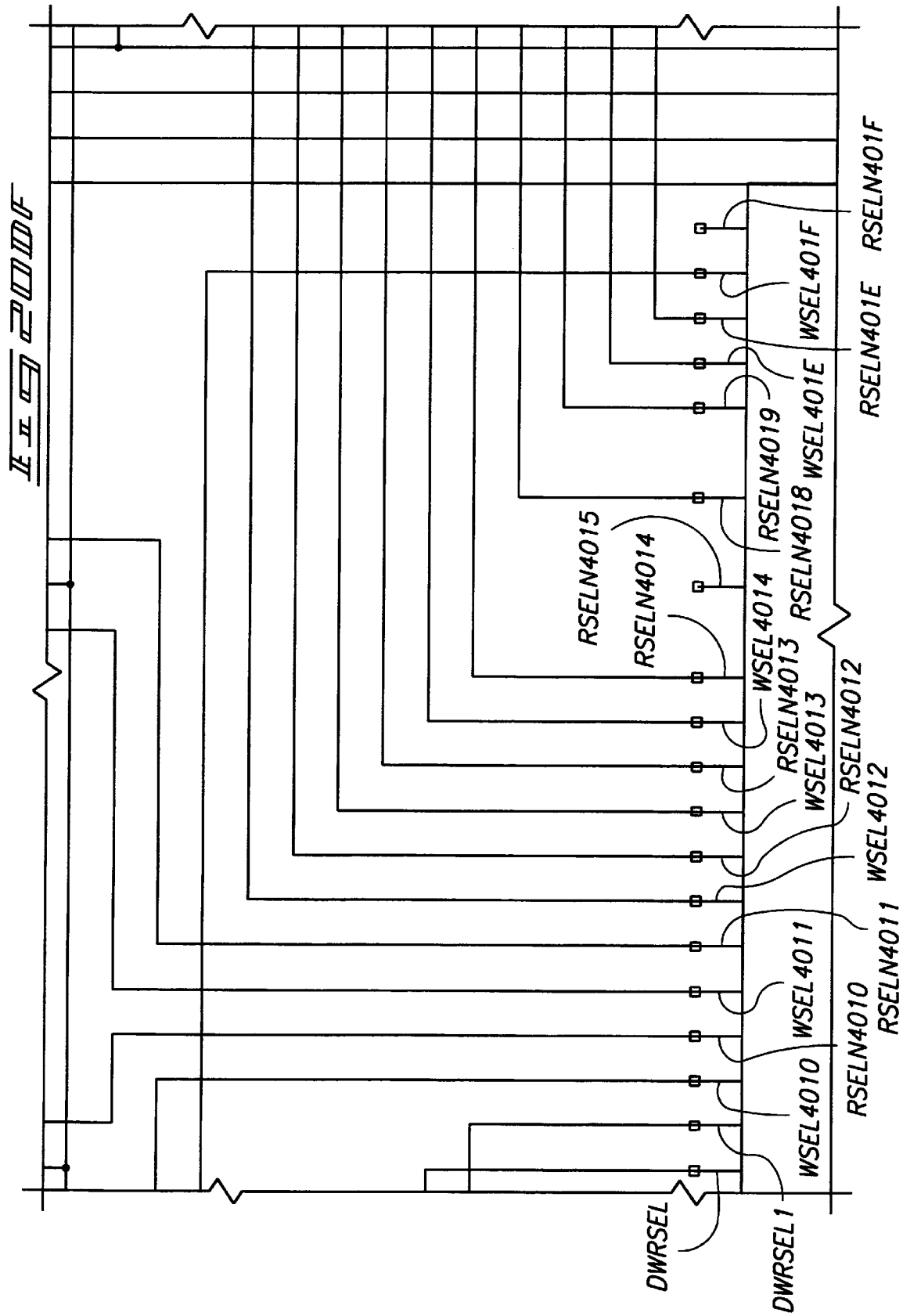


FIG 200F
RSELN401F
WSEL401F
RSELN401E
WSEL401E
RSELN4019
RSELN4018
RSELN4015
RSELN4014
WSEL4014
WSEL4013
RSELN4013
RSELN4012
WSEL4012
WSEL4011
RSELN4011
RSELN4010
WSEL4010
DWRSEL
DWRSEL1

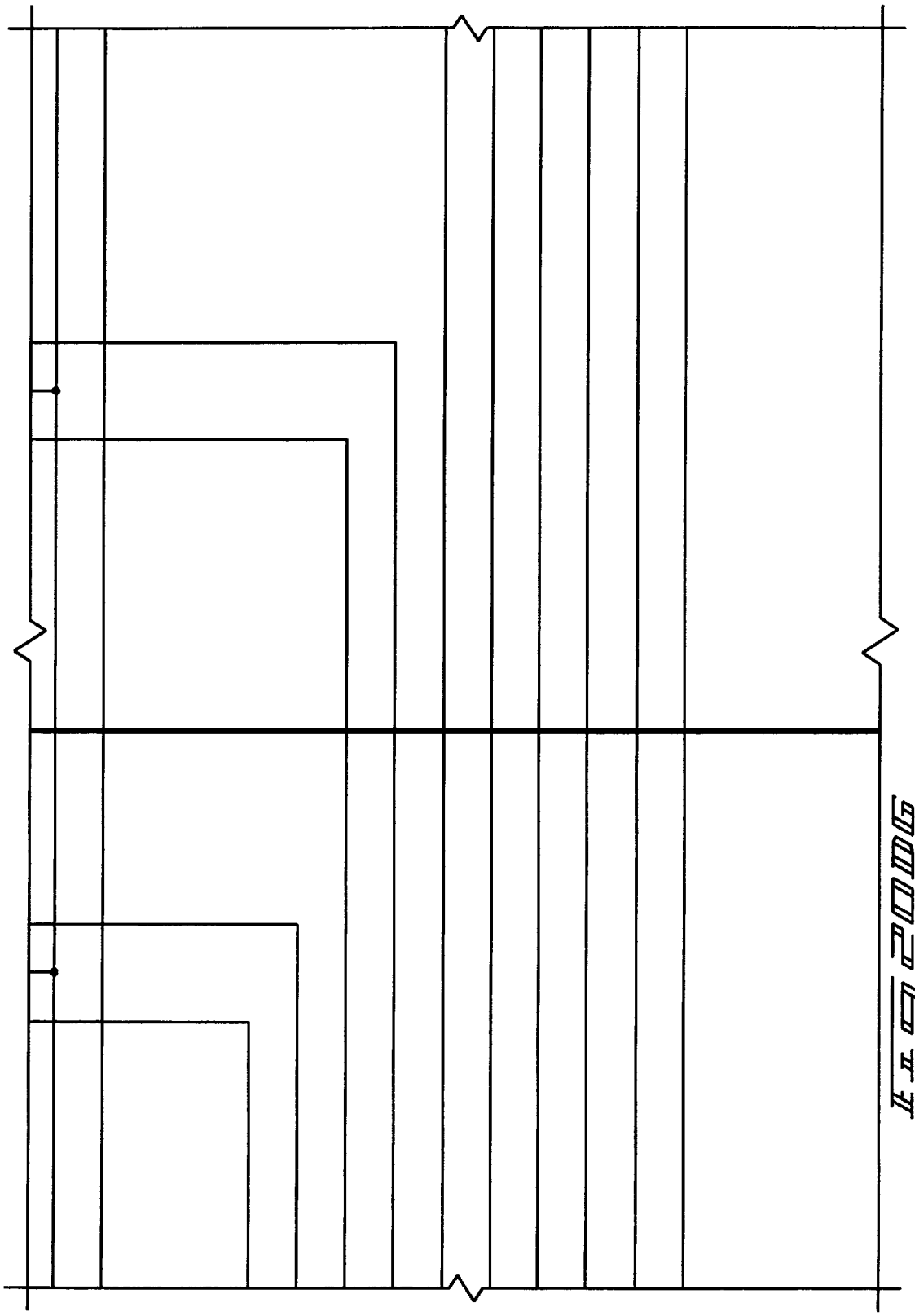


FIG 2005

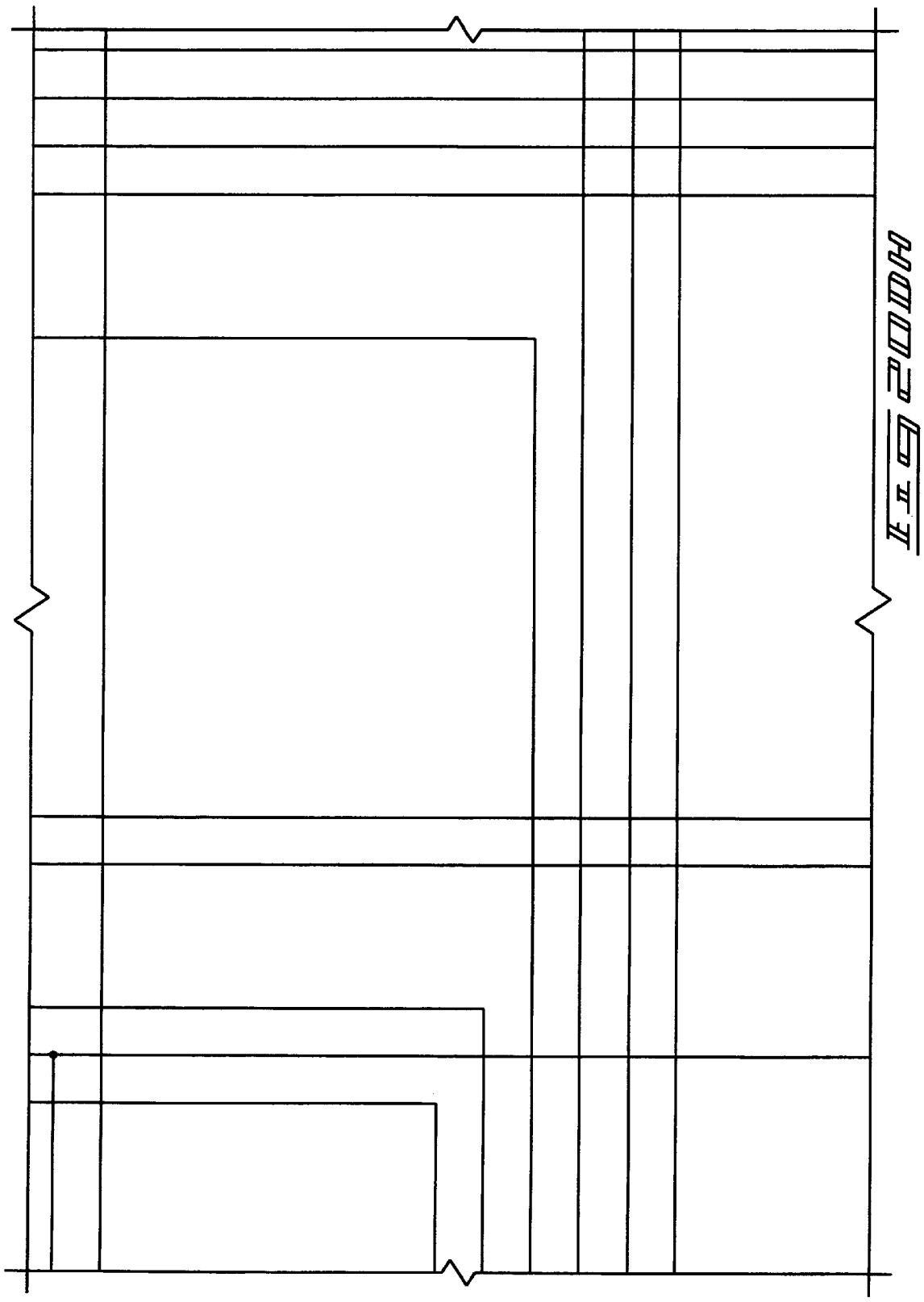


FIG 2004

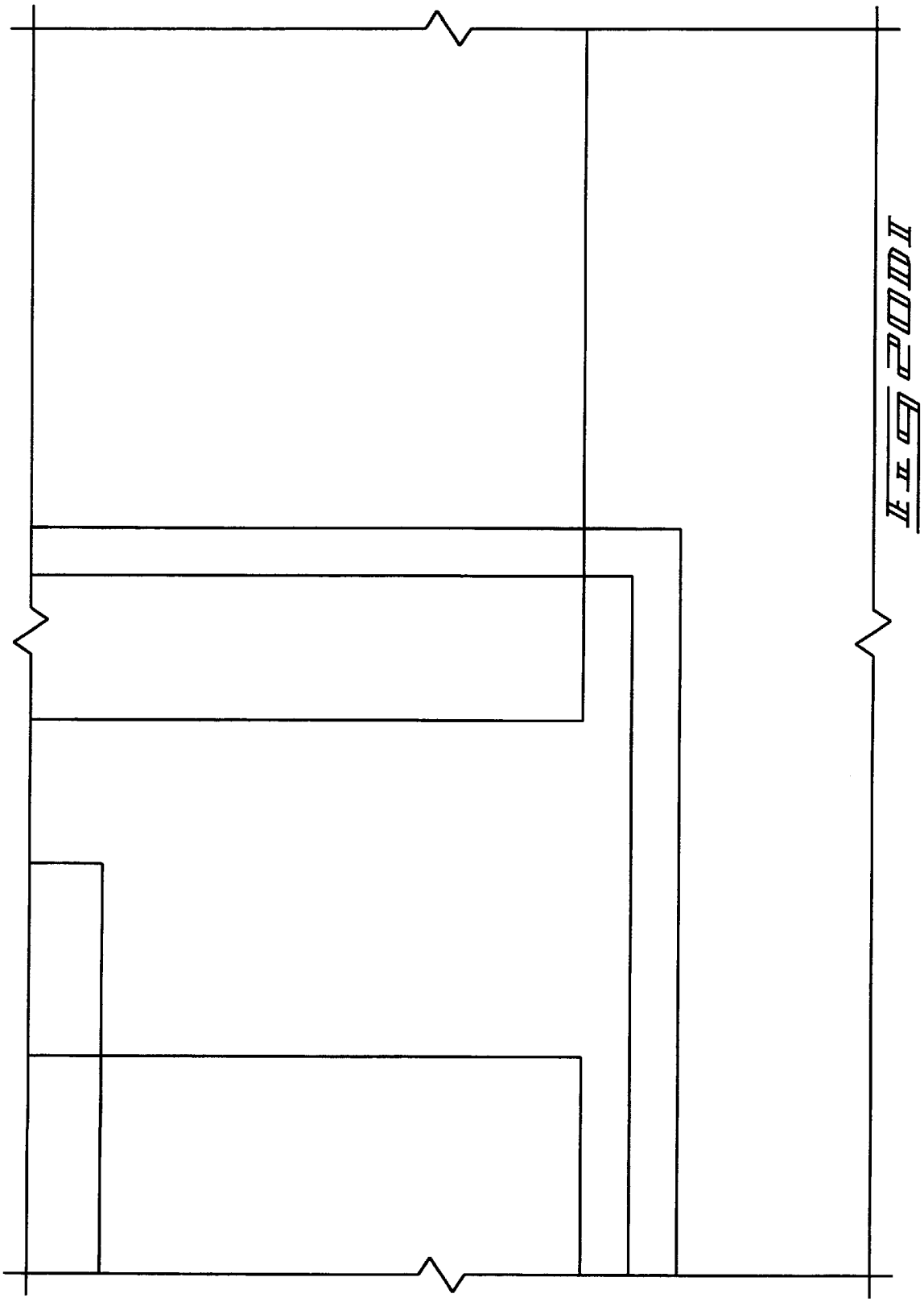
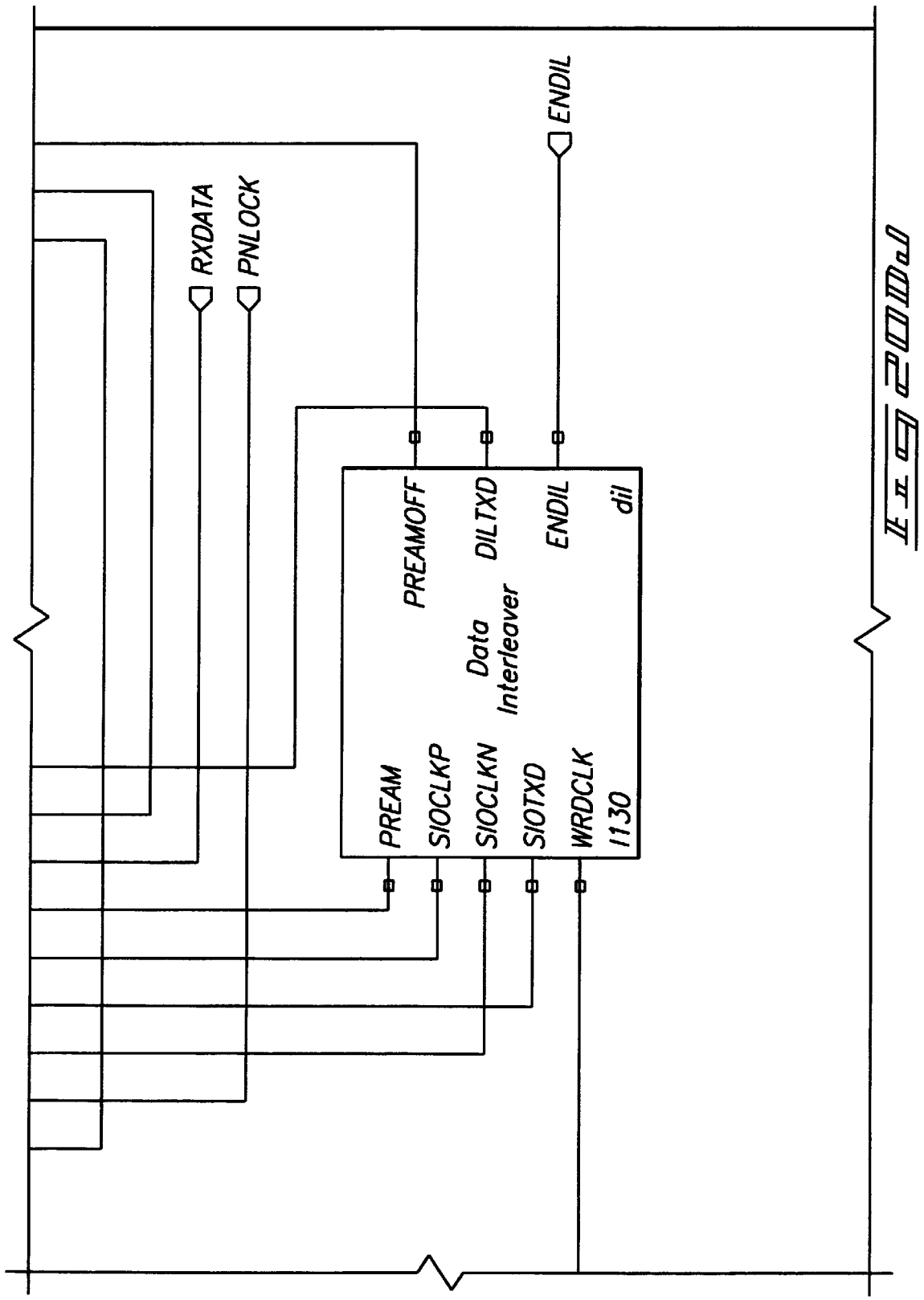


FIG 1002


ENDIL
RXDATA
PNLOCK
PREAMOFF
DILTXD
ENDIL
dil
Data Interleaver
PREAM
SIOCLKP
SIOCLKN
SIOTXD
WRDCLK
1130
FIG 2000

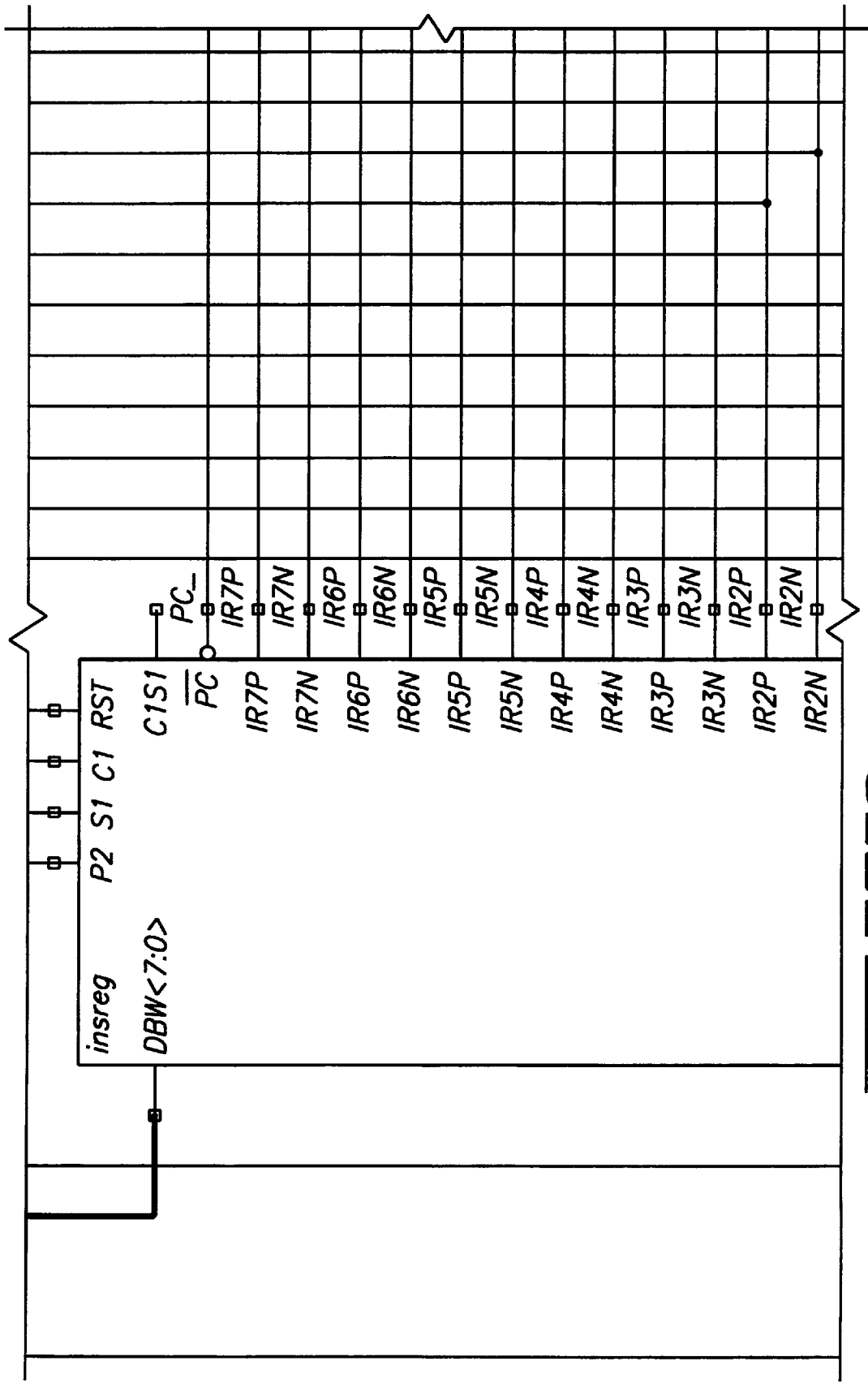

PC_
IR7P
IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
IR4N
IR3P
IR3N
IR2P
IR2N
C1S1
$\overline{PC}$
RST
C1
S1
P2
insreg
DBW<7:0>

Fig 2EA

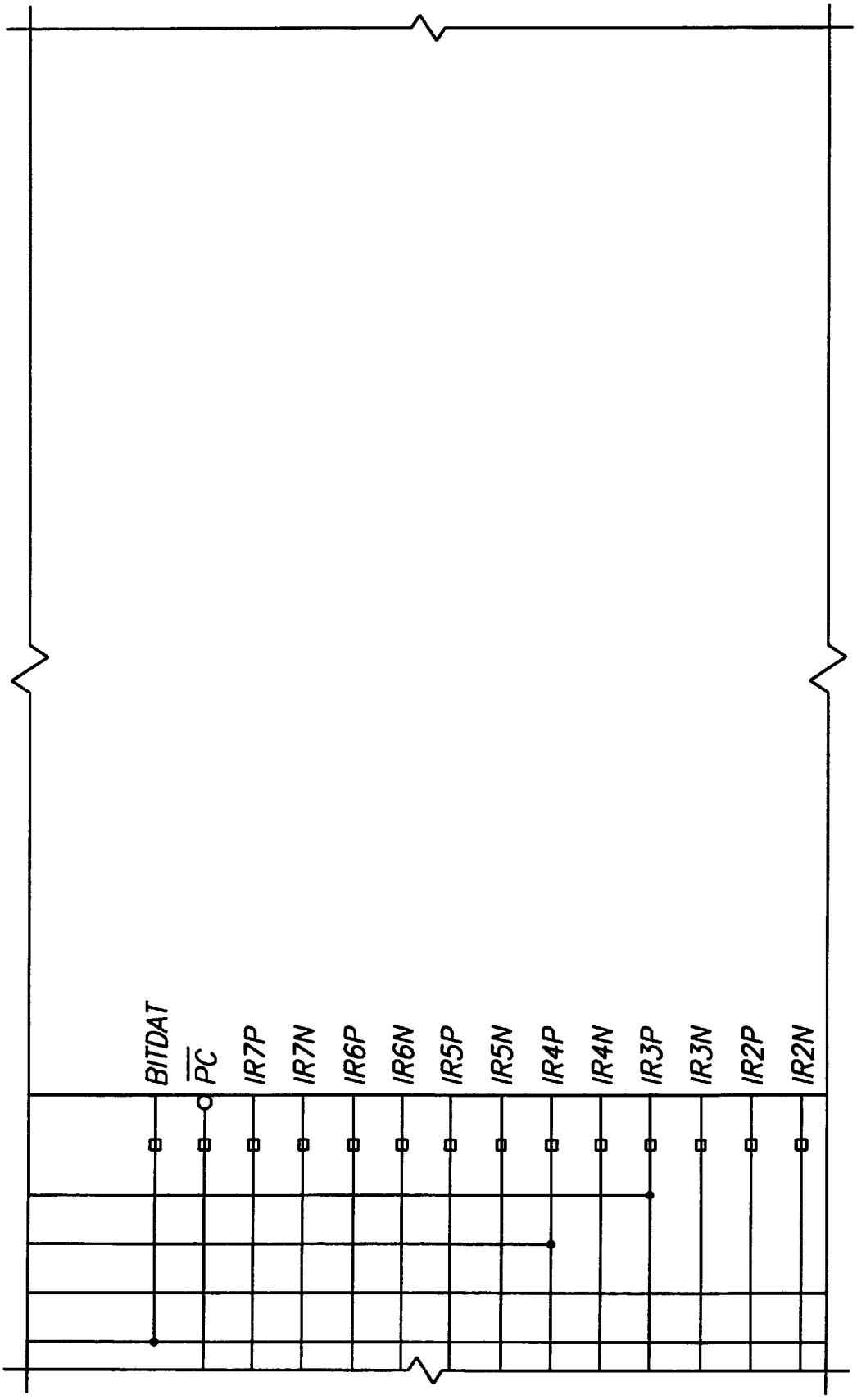

BITDAT
$\overline{PC}$
IR7P
IR7N
IR6P
IR6N
IR5P
IR5N
IR4P
IR4N
IR3P
IR3N
IR2P
IR2N

FIG 2081B

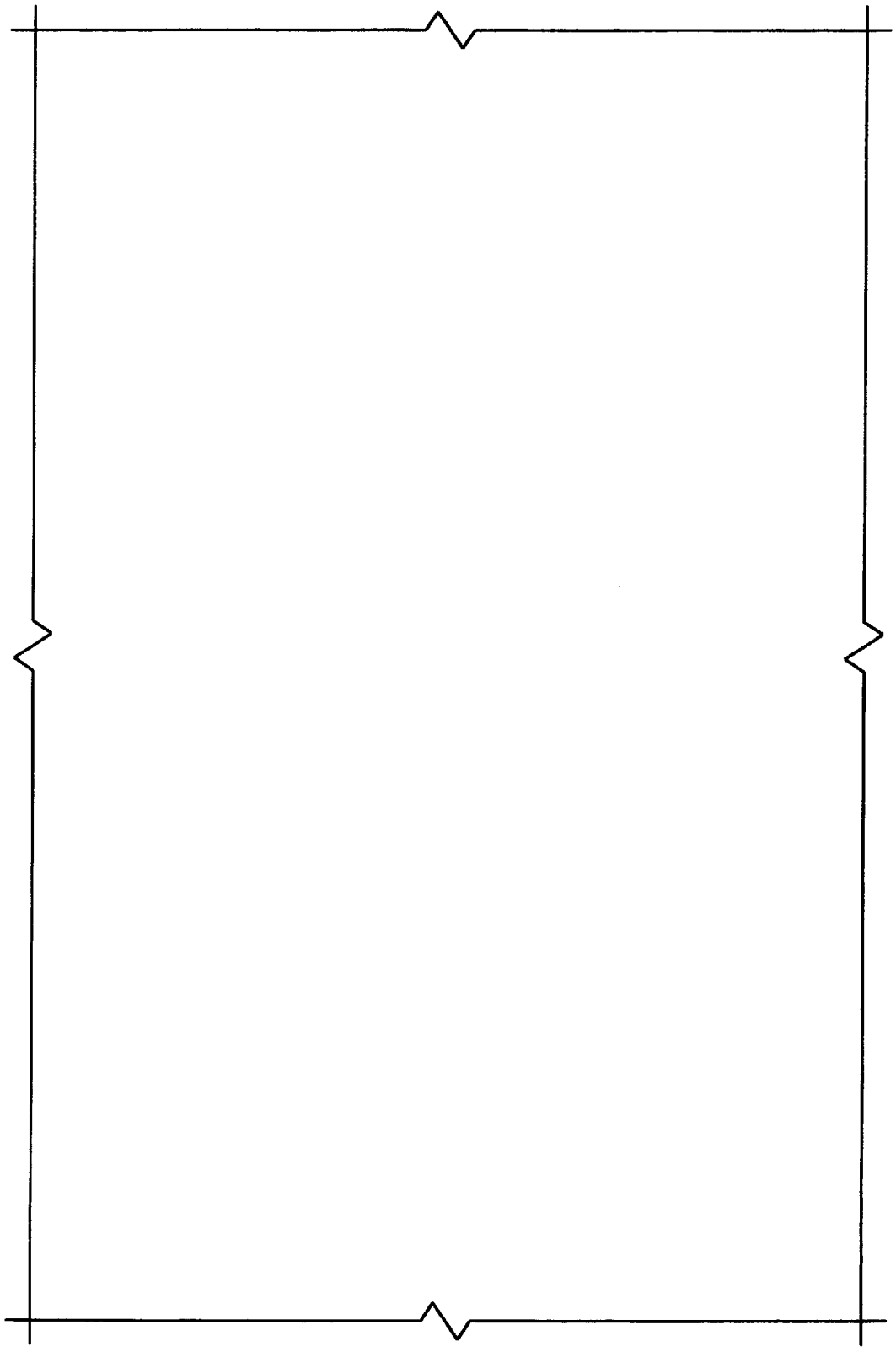


FIG. 3182

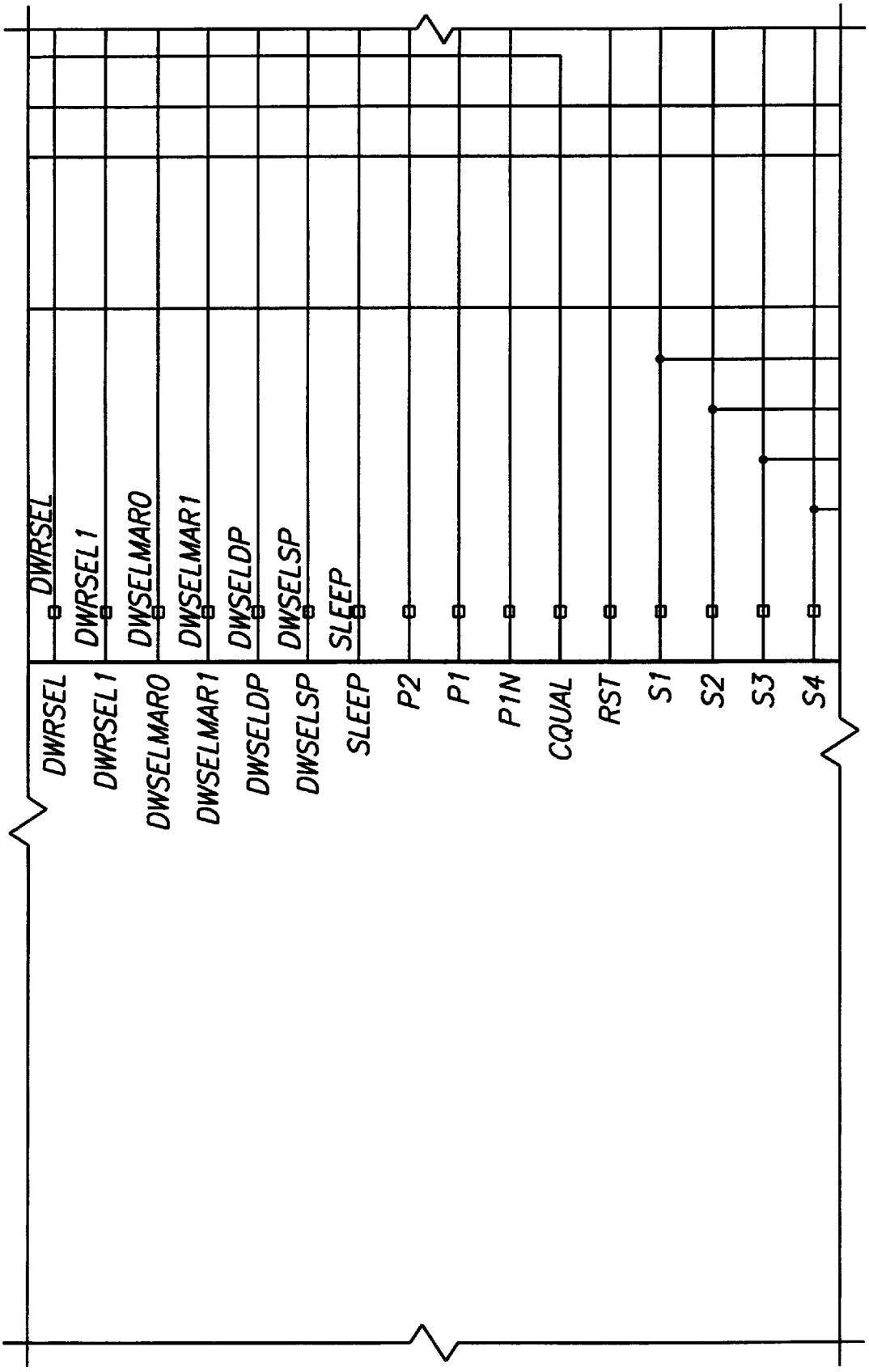

DWRSEL
DWRSEL1
DWSELMAR0
DWSELMAR1
DWSELDP
DWSELSP
SLEEP
P2
P1
P1N
CQUAL
RST
S1
S2
S3
S4

FIG 2DE III

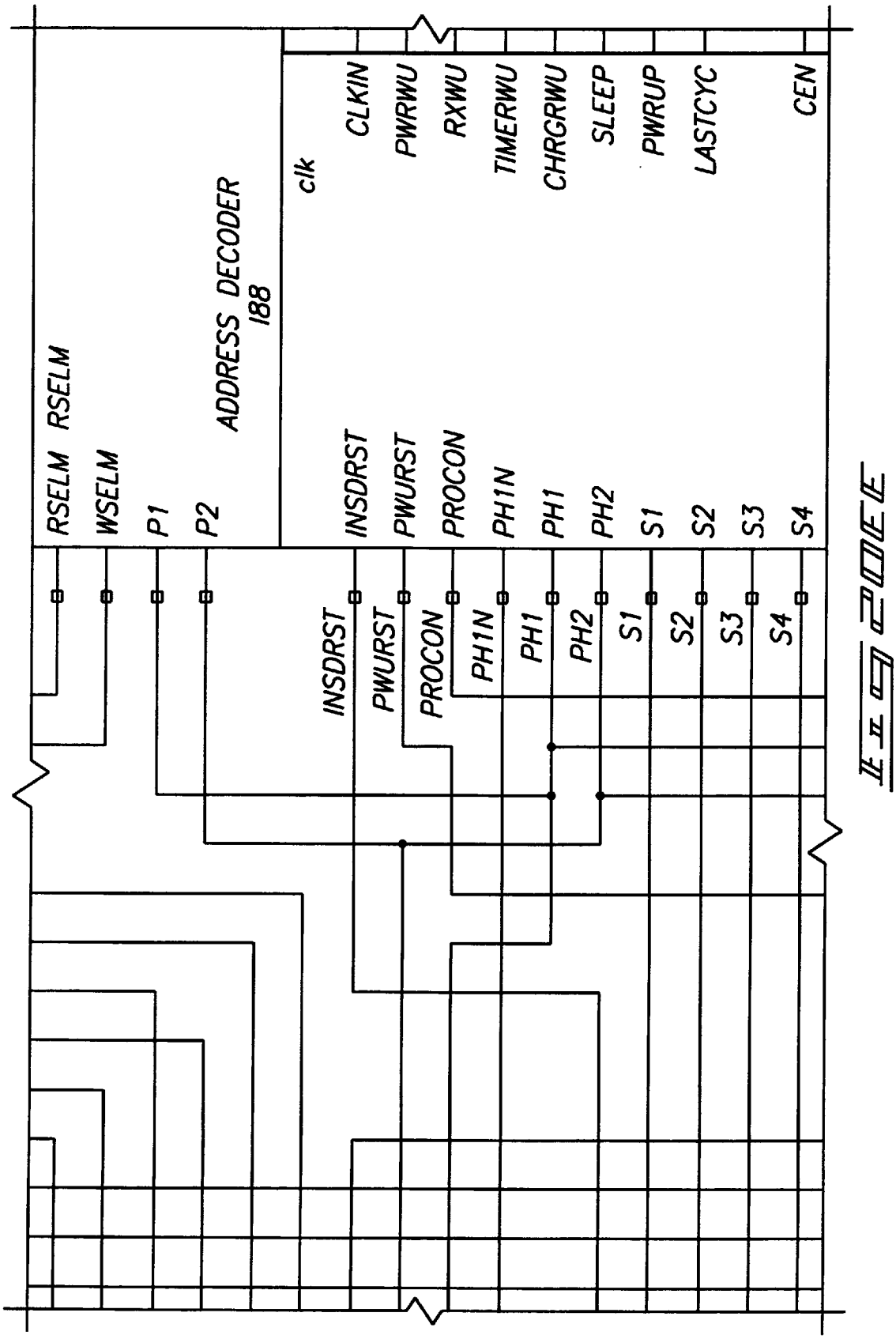
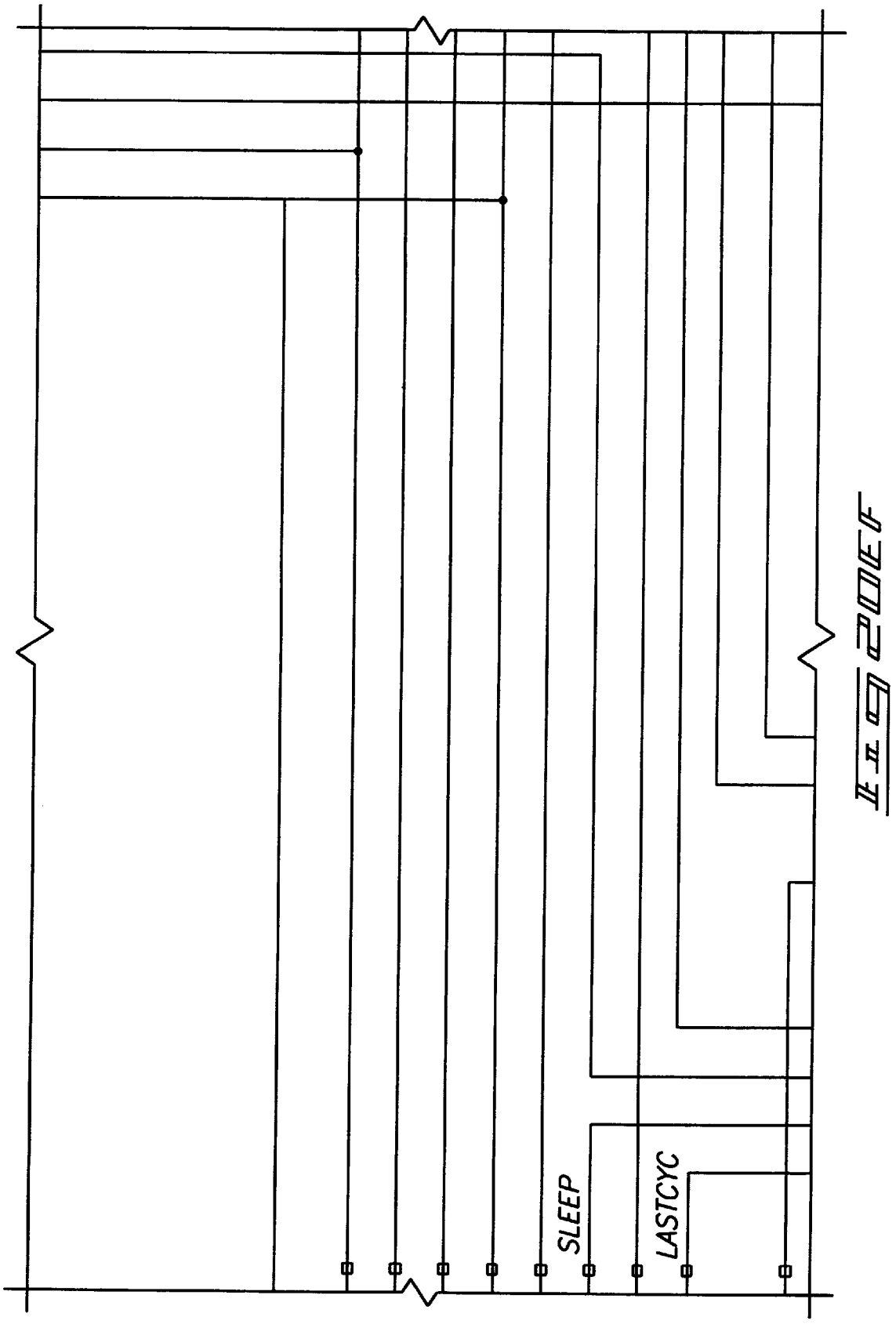

RSELM
WSELM
P1
P2
ADDRESS DECODER
188
clk
CLKIN
PWRWU
RXWU
TIMERWU
CHRGRWU
SLEEP
PWRUP
LASTCYC
CEN
INSDRST
PWURST
PROCON
PH1N
PH1
PH2
S1
S2
S3
S4

FIG 2DDE


SLEEP
LASTCYC
FIG 200E

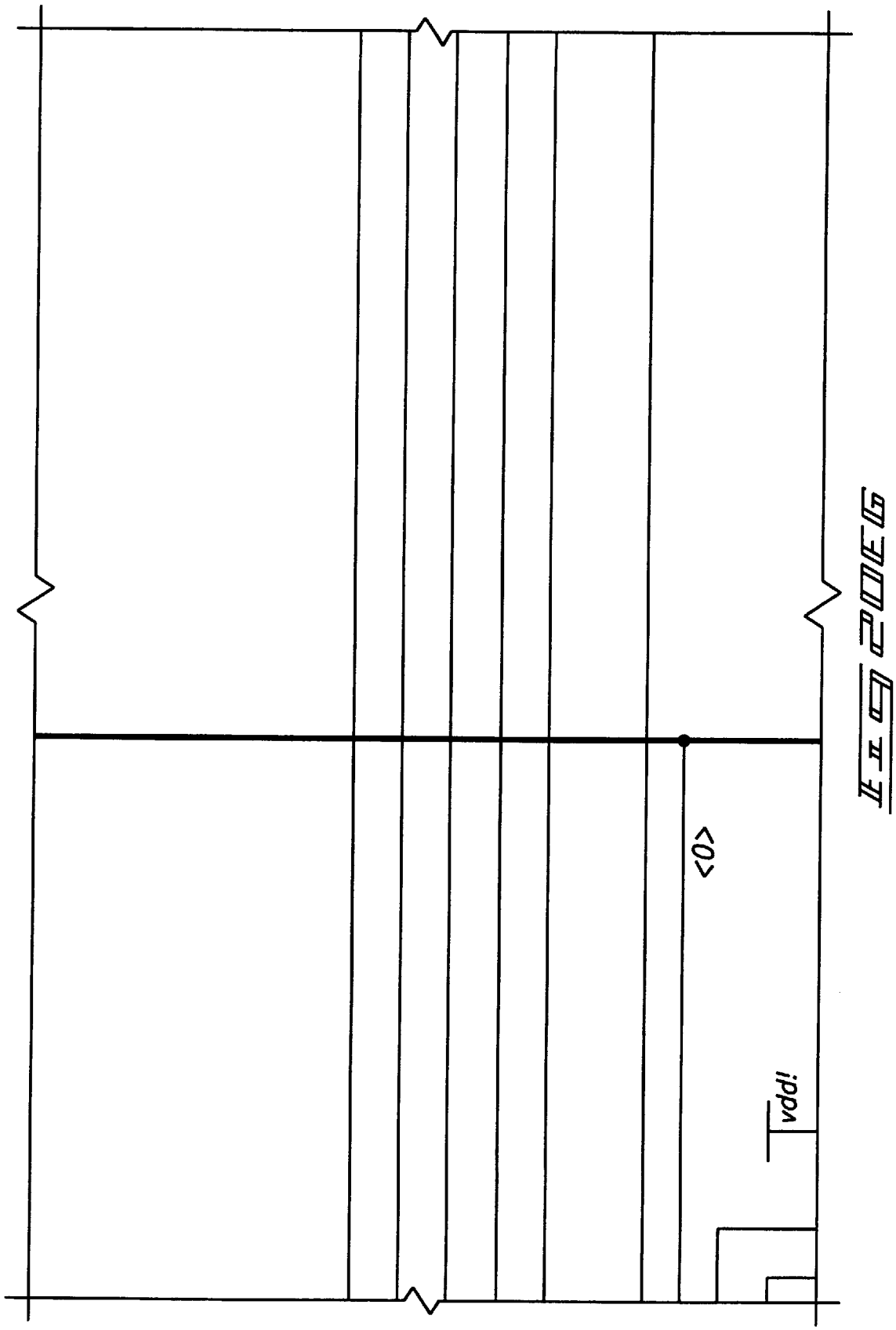


FIG 2065
<0>
vdd!

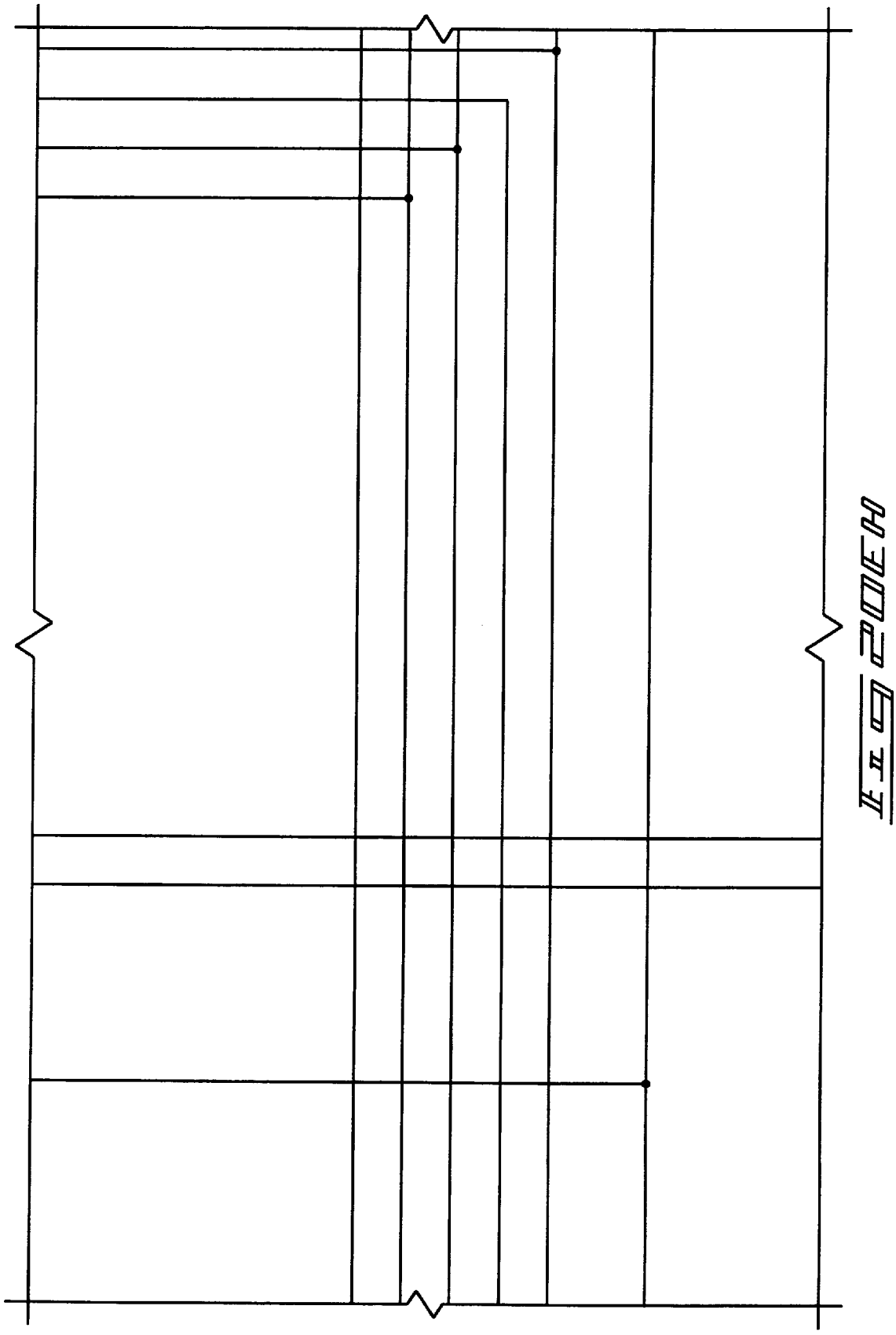


FIG 200H

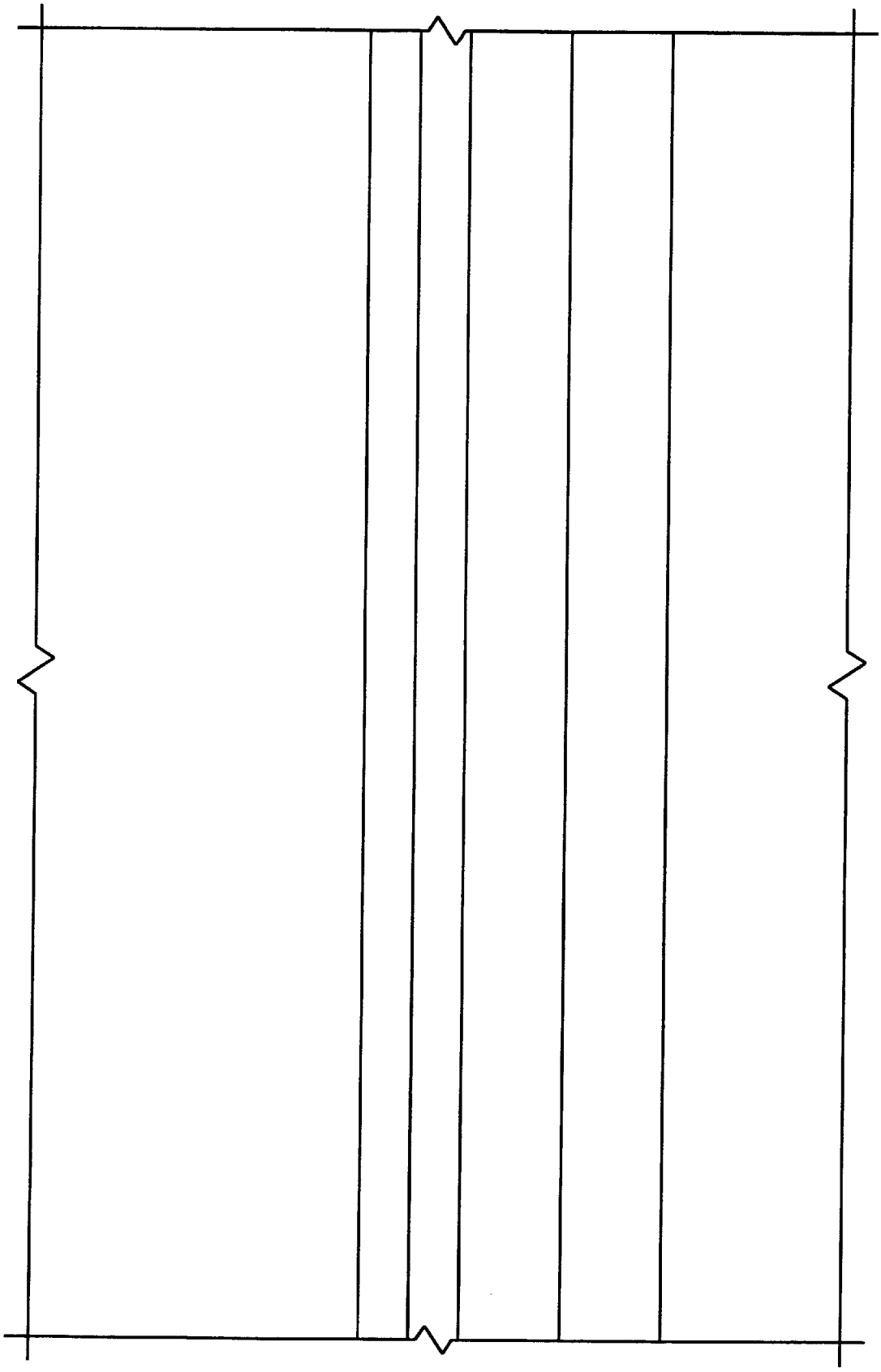


FIG 20EII

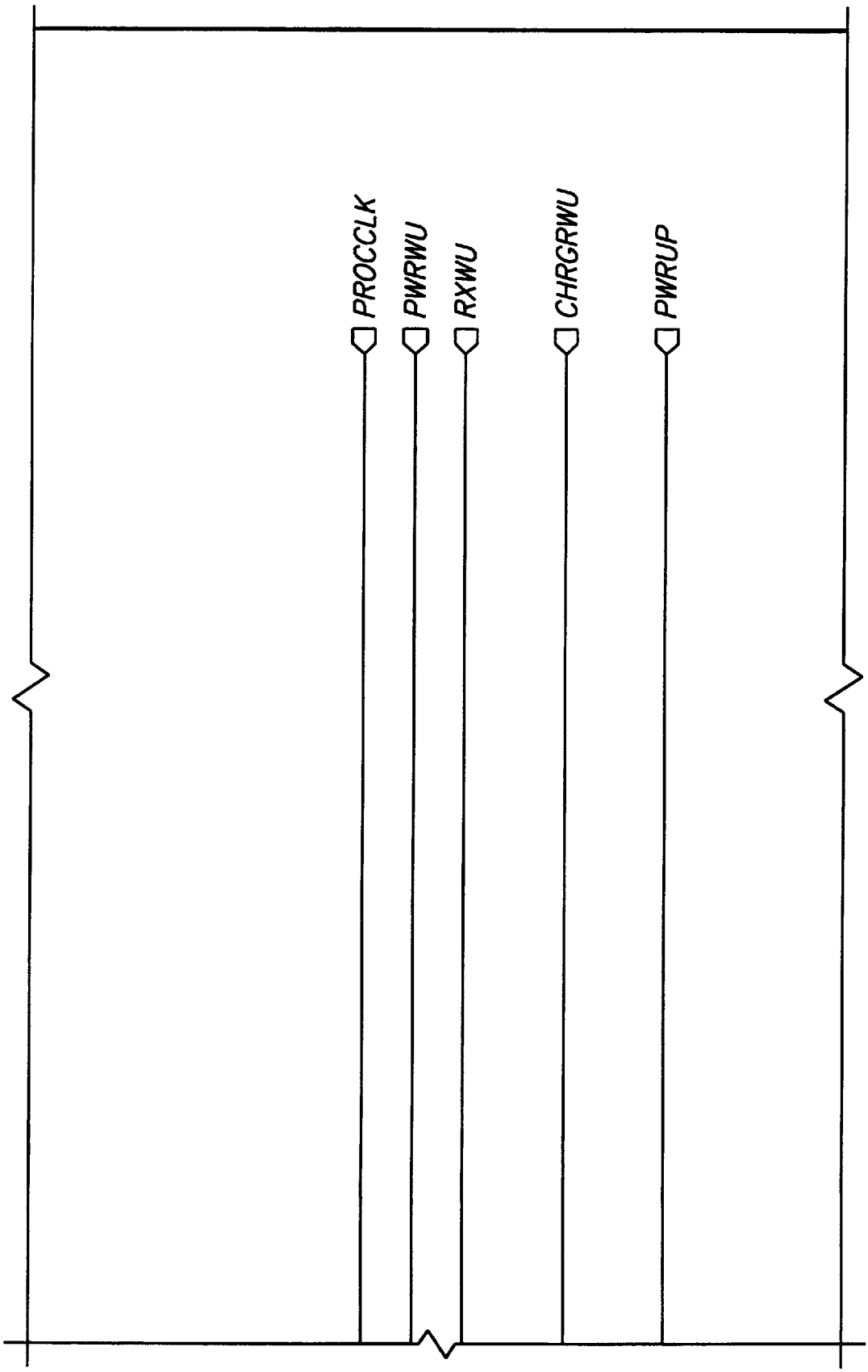


Fig 208d

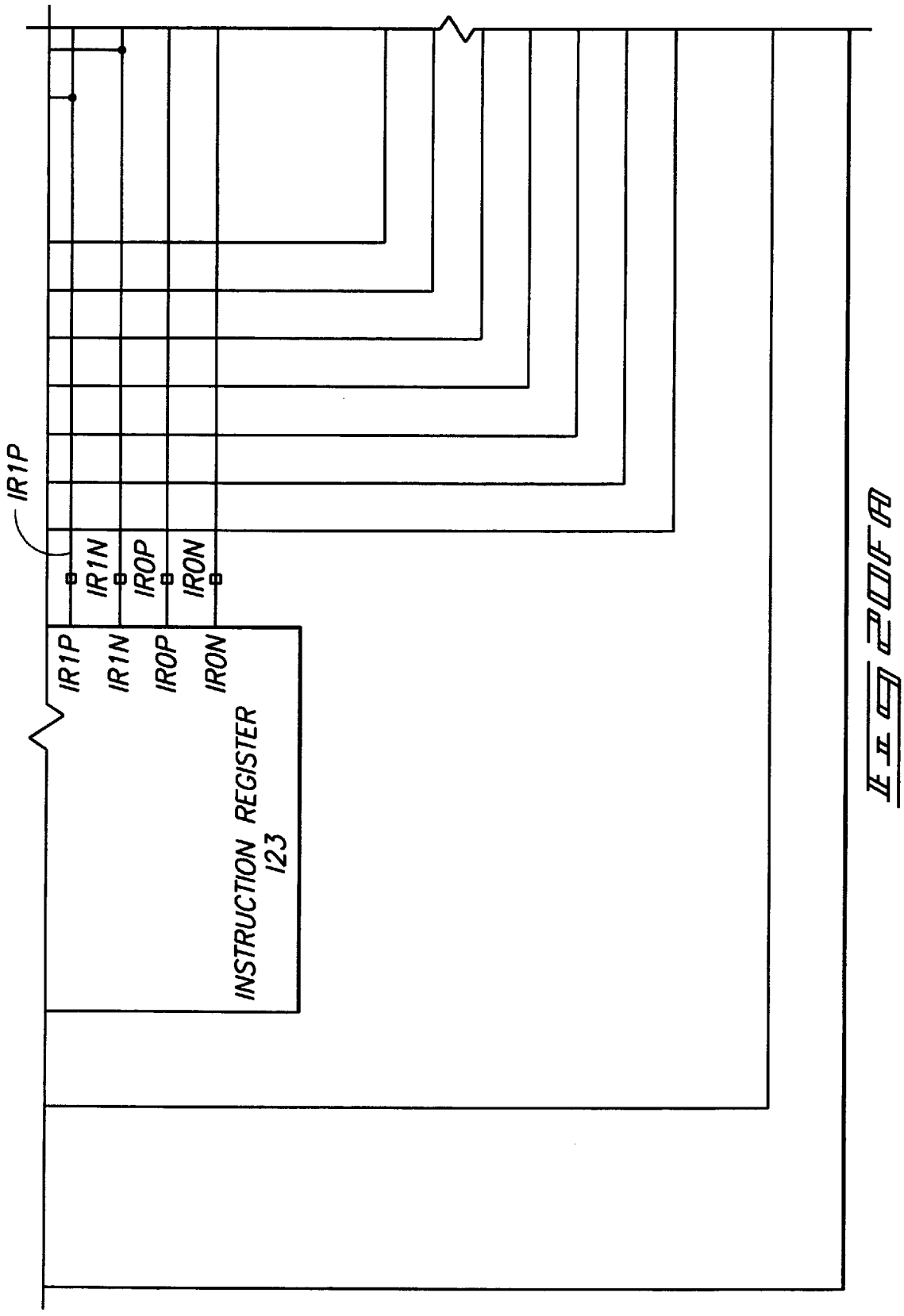

IR1P
IR1N
IR0P
IR0N
IR1P
IR1N
IR0P
IR0N
INSTRUCTION REGISTER
123

FIG 20FA

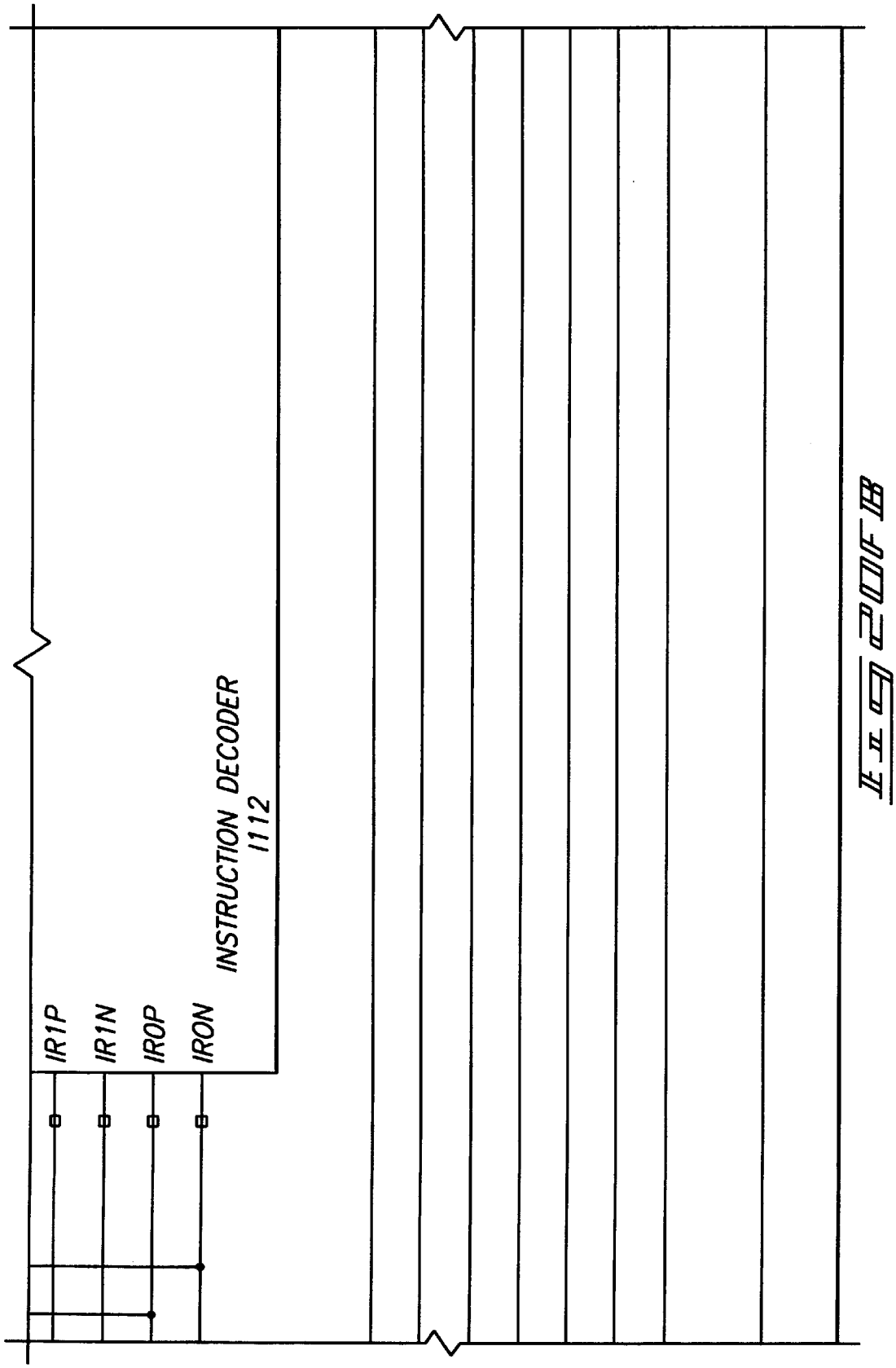


FIG 2OF 18
INSTRUCTION DECODER
1112
IR1P
IR1N
IR0P
IR0N

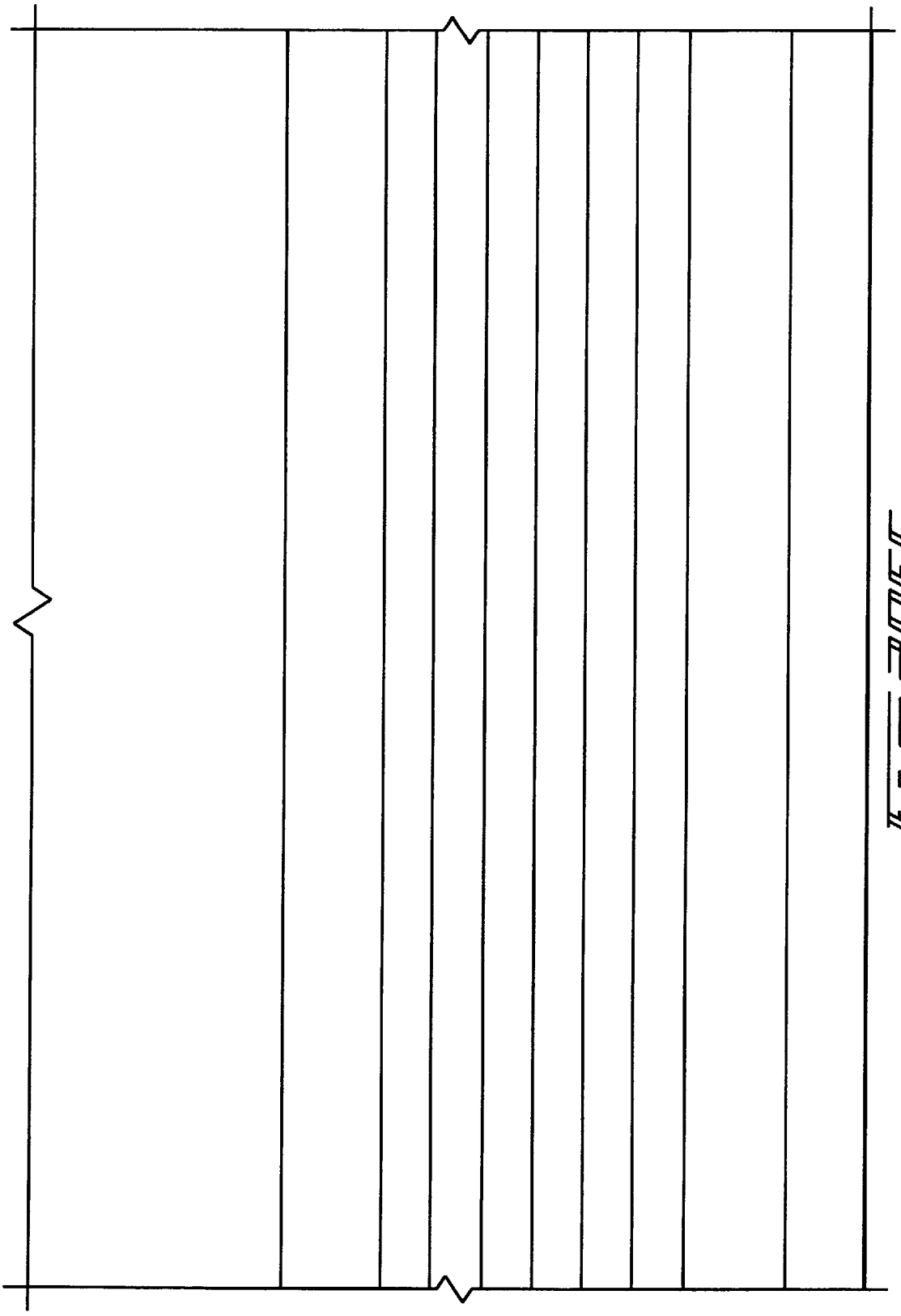


FIG 208F

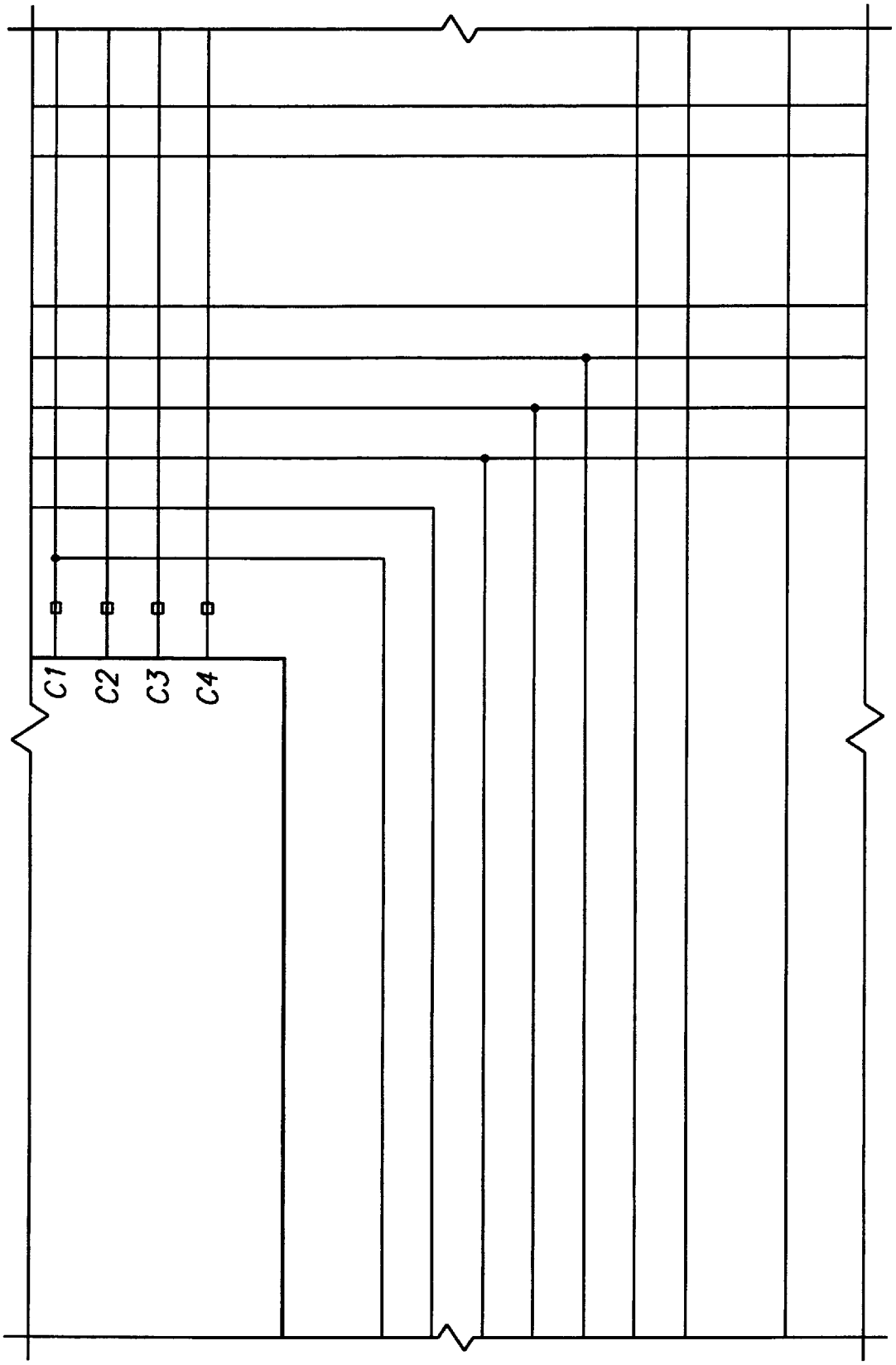


Fig 200 FD

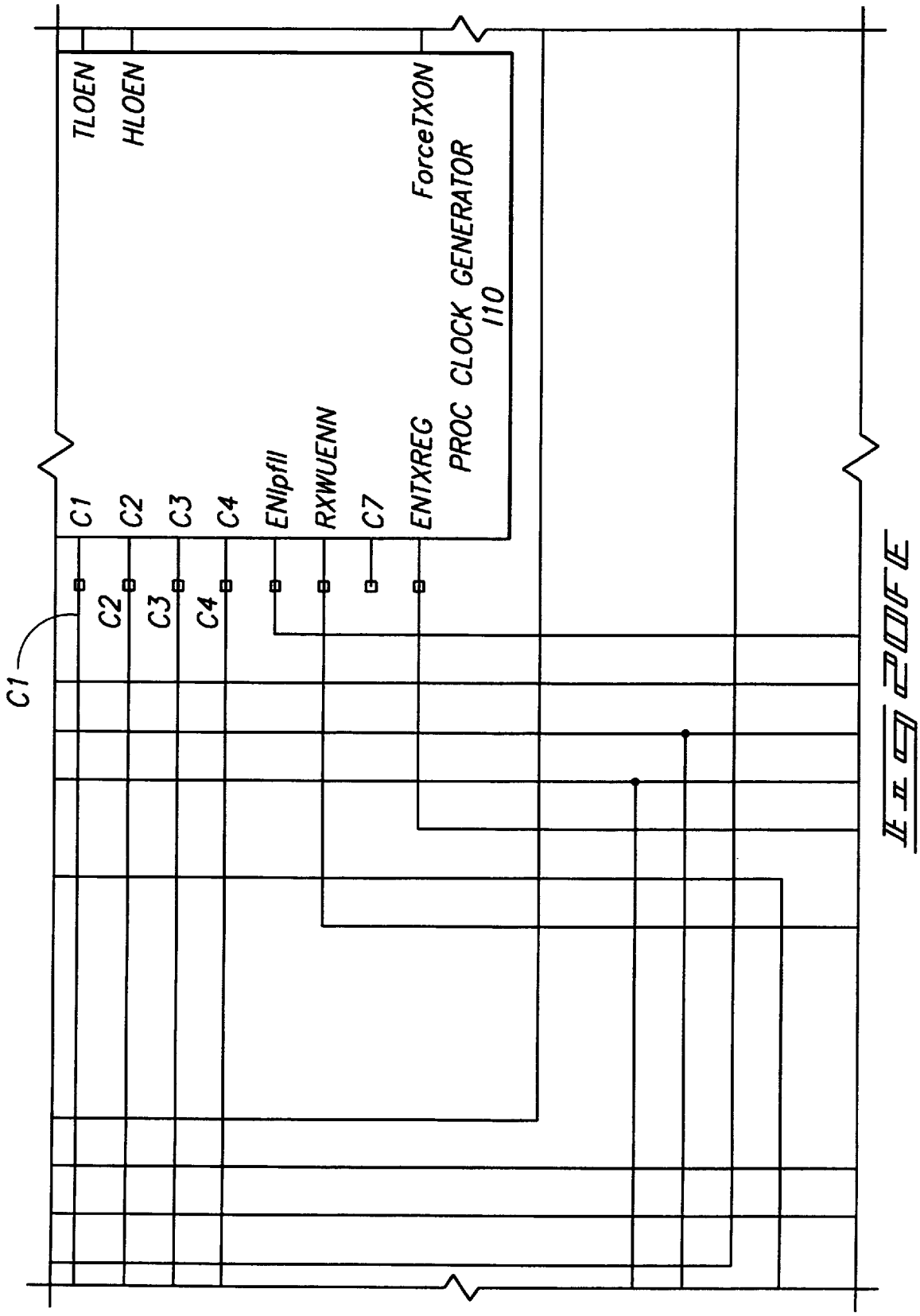

TLOEN
HLOEN
ForceTXON
PROC CLOCK GENERATOR
110
C1
C2
C3
C4
ENIpfII
RXWUENN
C7
ENTXREG
C1
C2
C3
C4

Fig 20fE

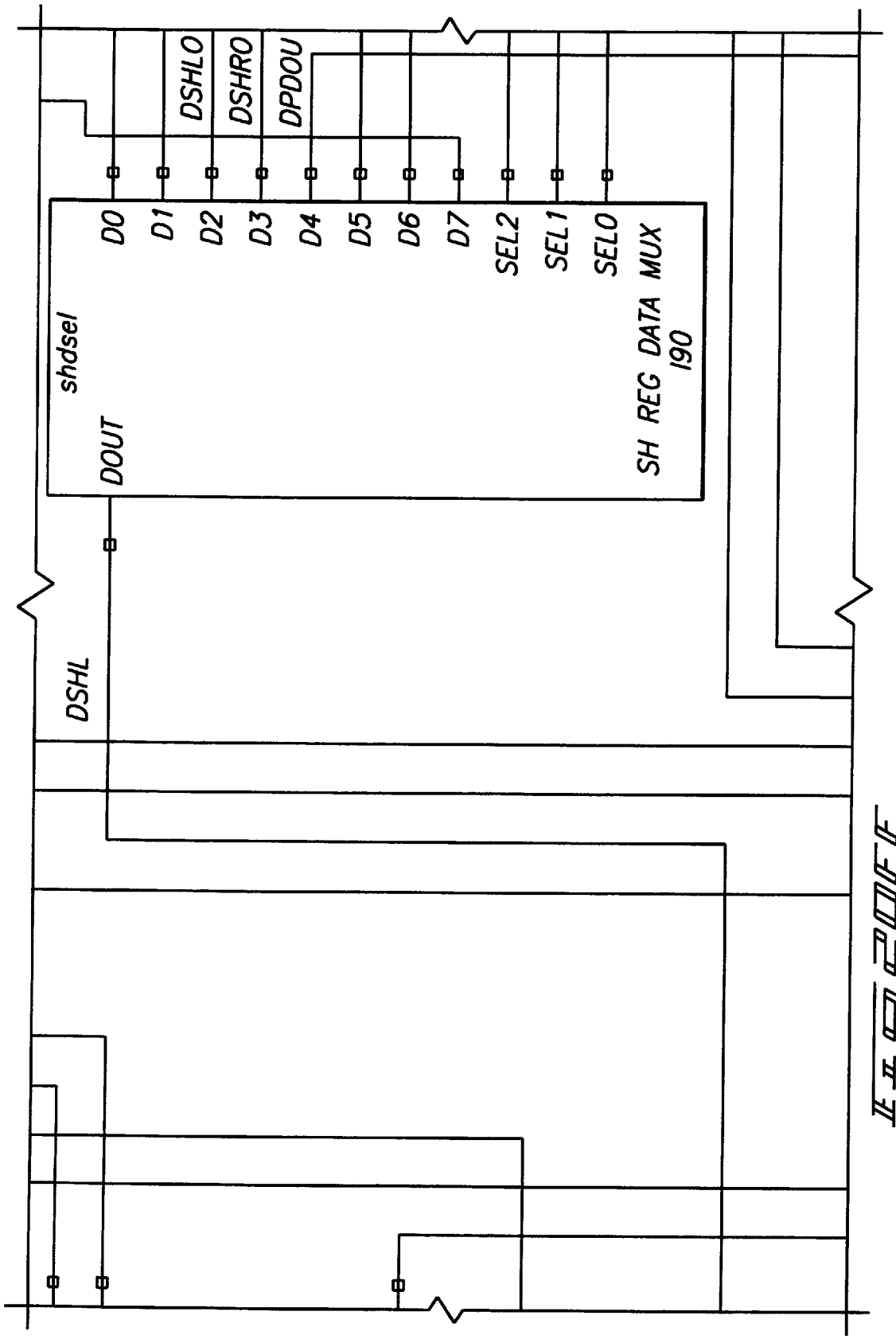

DSHLO
DSHRO
DPDOU
D0
D1
D2
D3
D4
D5
D6
D7
SEL2
SEL1
SEL0
MUX
DATA
REG
SH
shdsel
DOUT
DSHL

FIG 20F

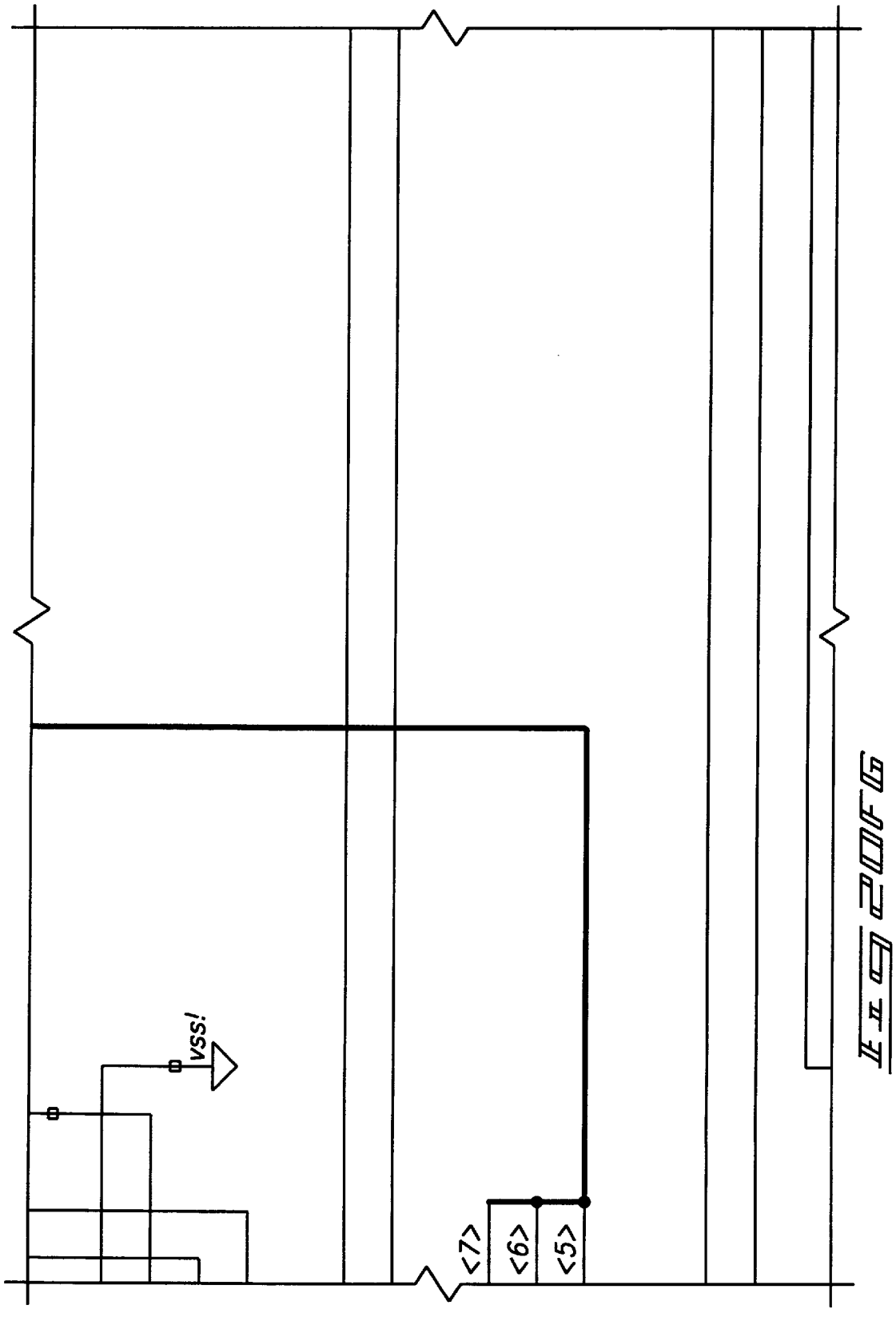


FIG 20F6

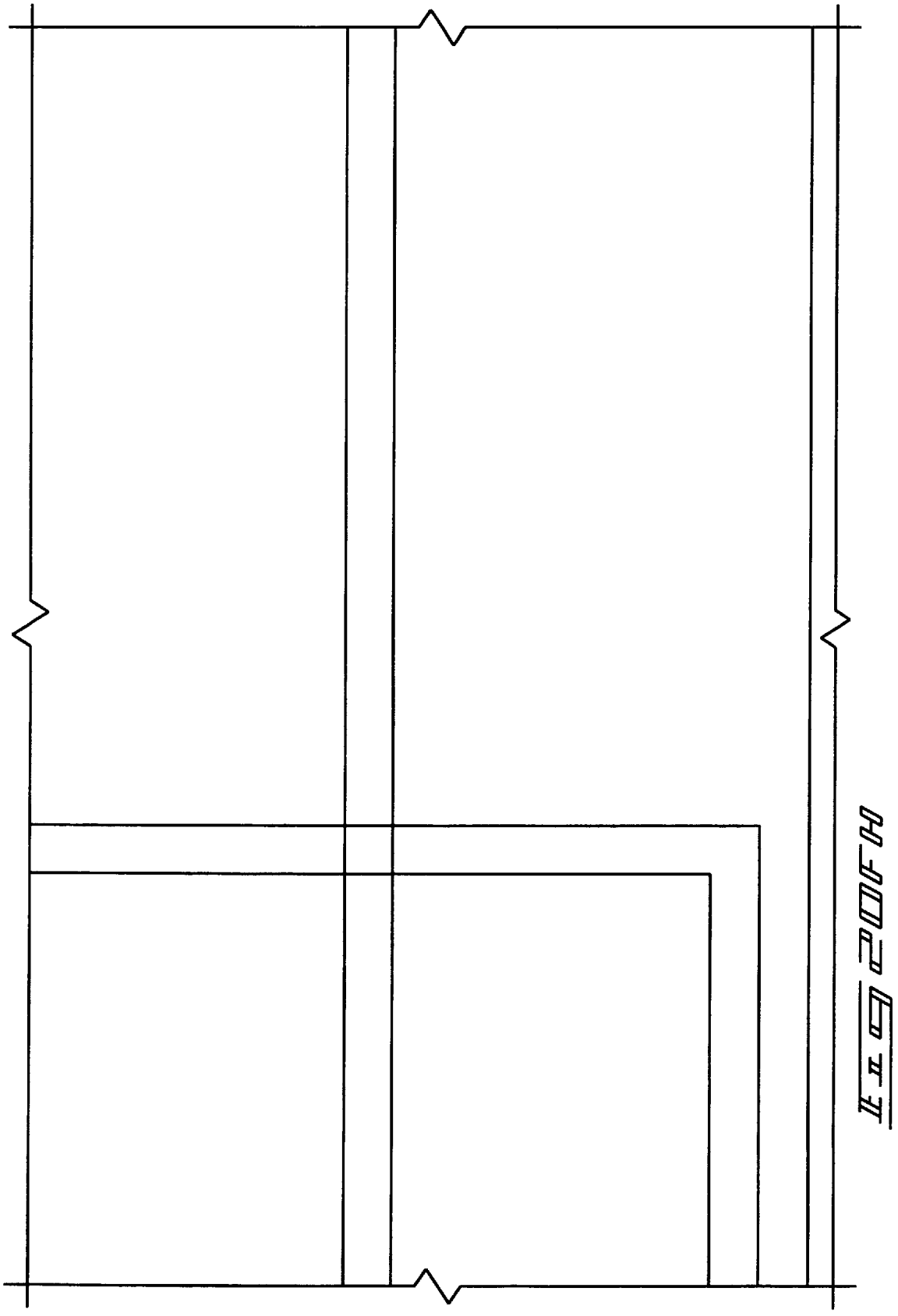


FIG 2054

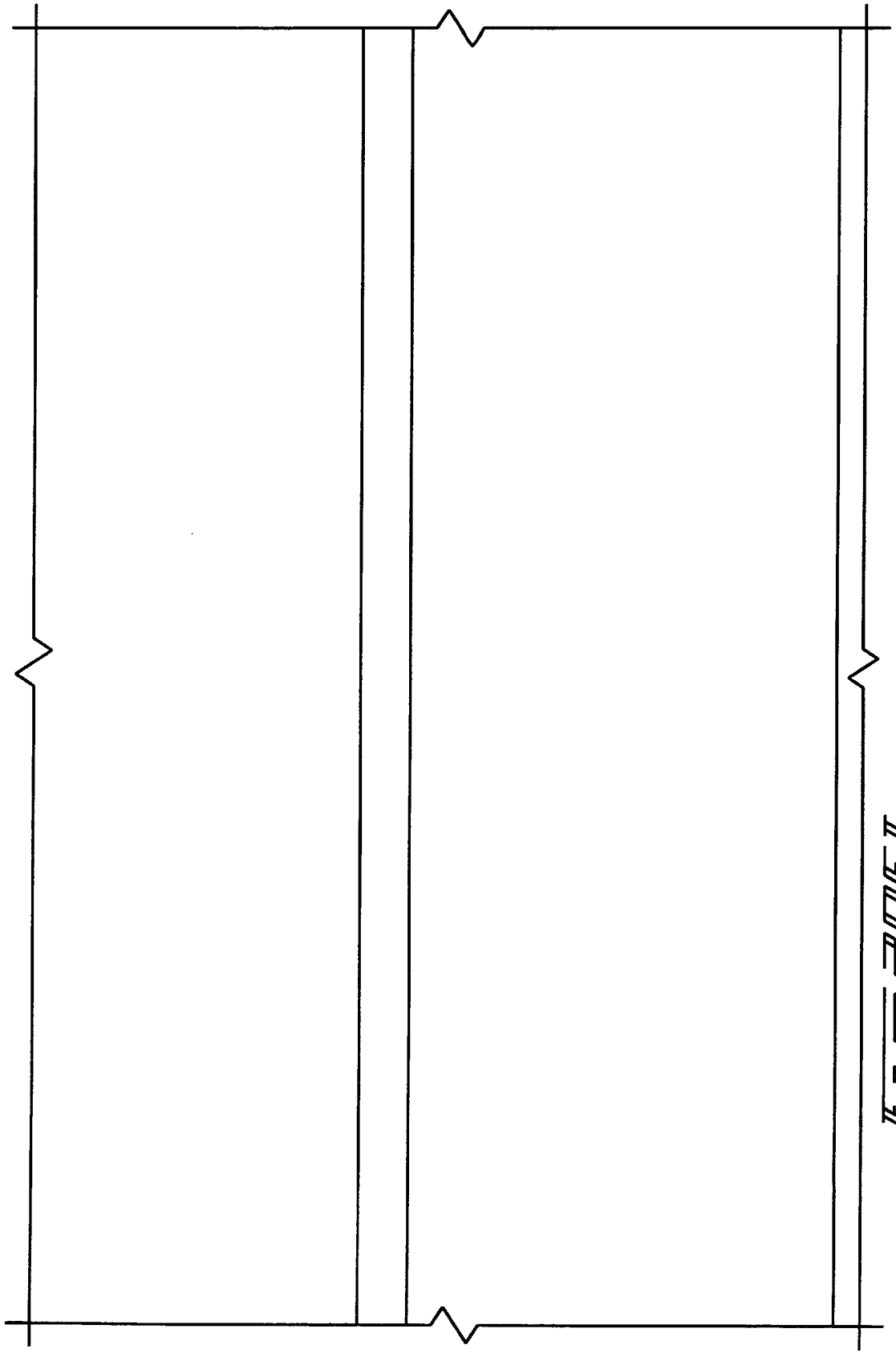


FIG 202 II

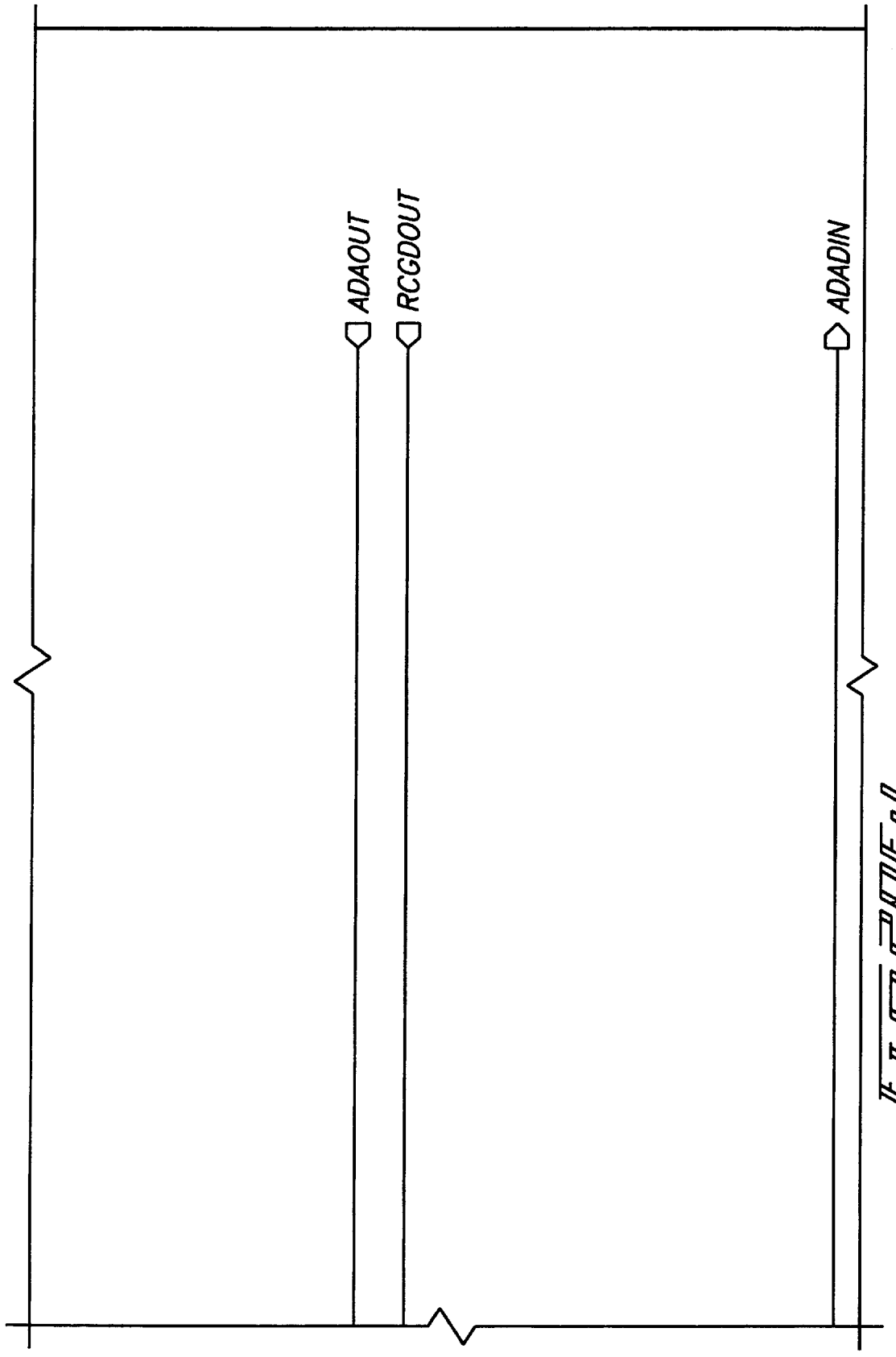


Fig 2007d

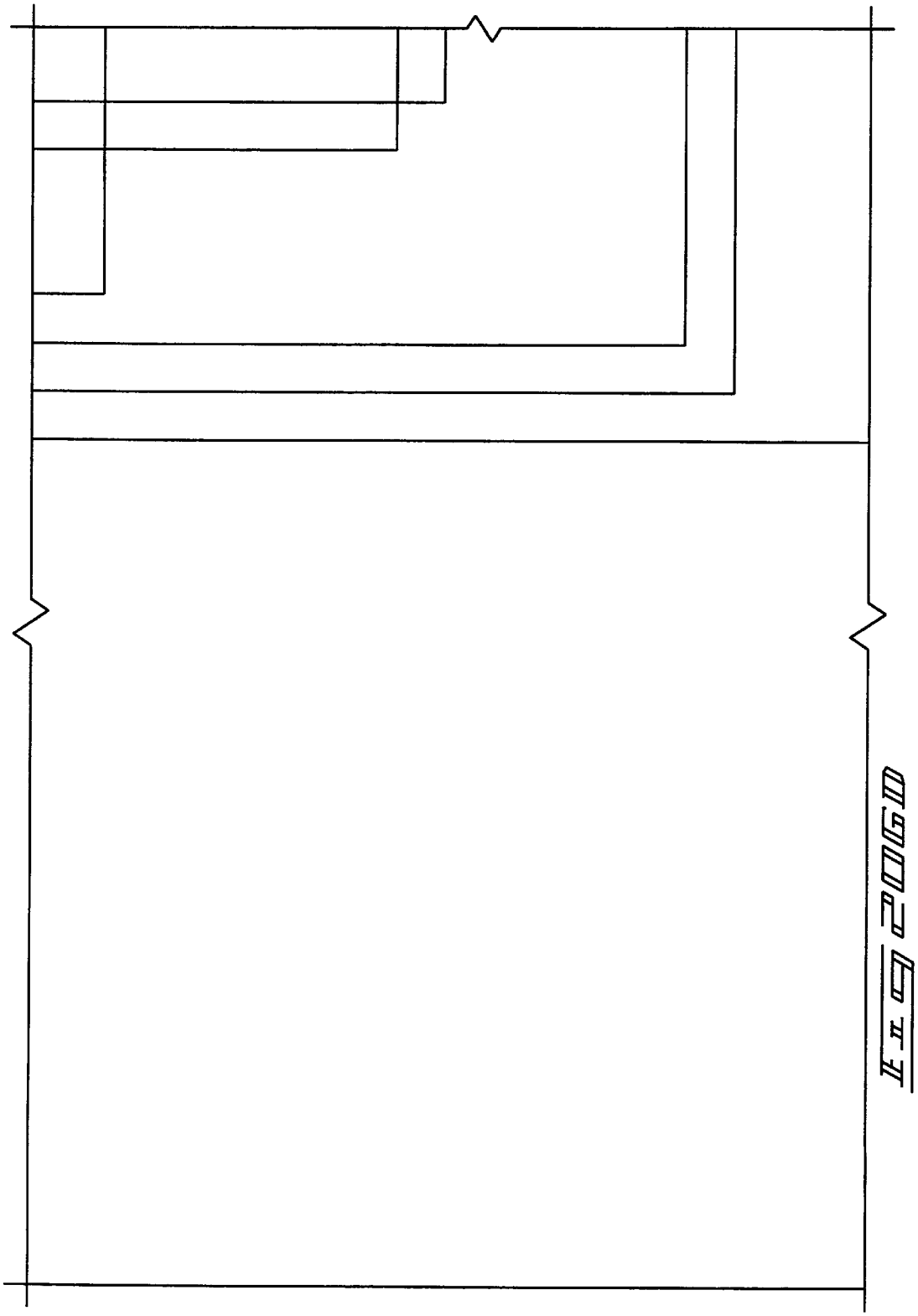


FIG 2900

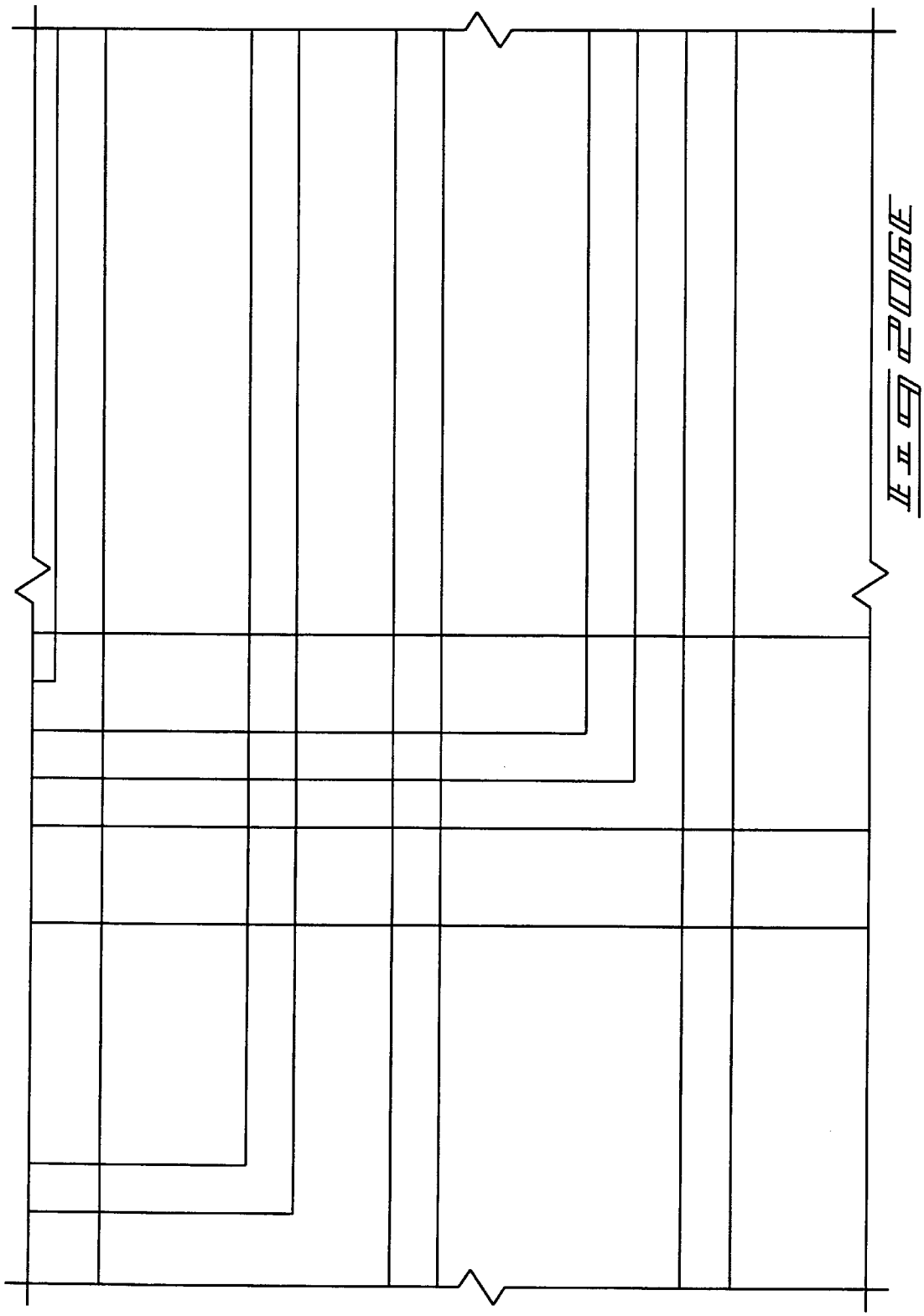


Fig 2056

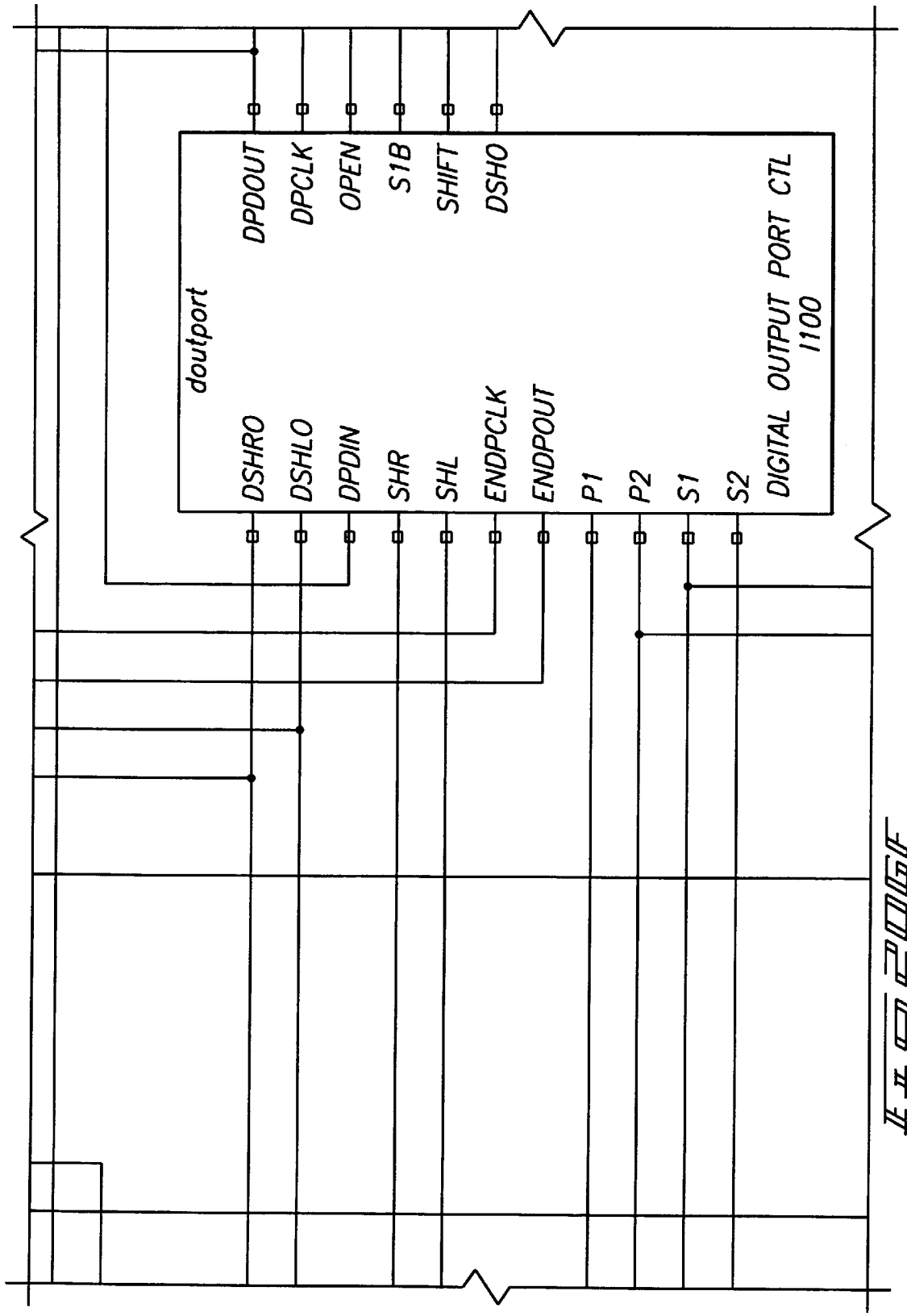

doutport
DPDOUT
DPCLK
OPEN
S1B
SHIFT
DSHO
DSHRO
DSHLO
DPDIN
SHR
SHL
ENDPCLK
ENDPOUT
P1
P2
S1
S2
DIGITAL OUTPUT PORT CTL
1100

FIG 2006F

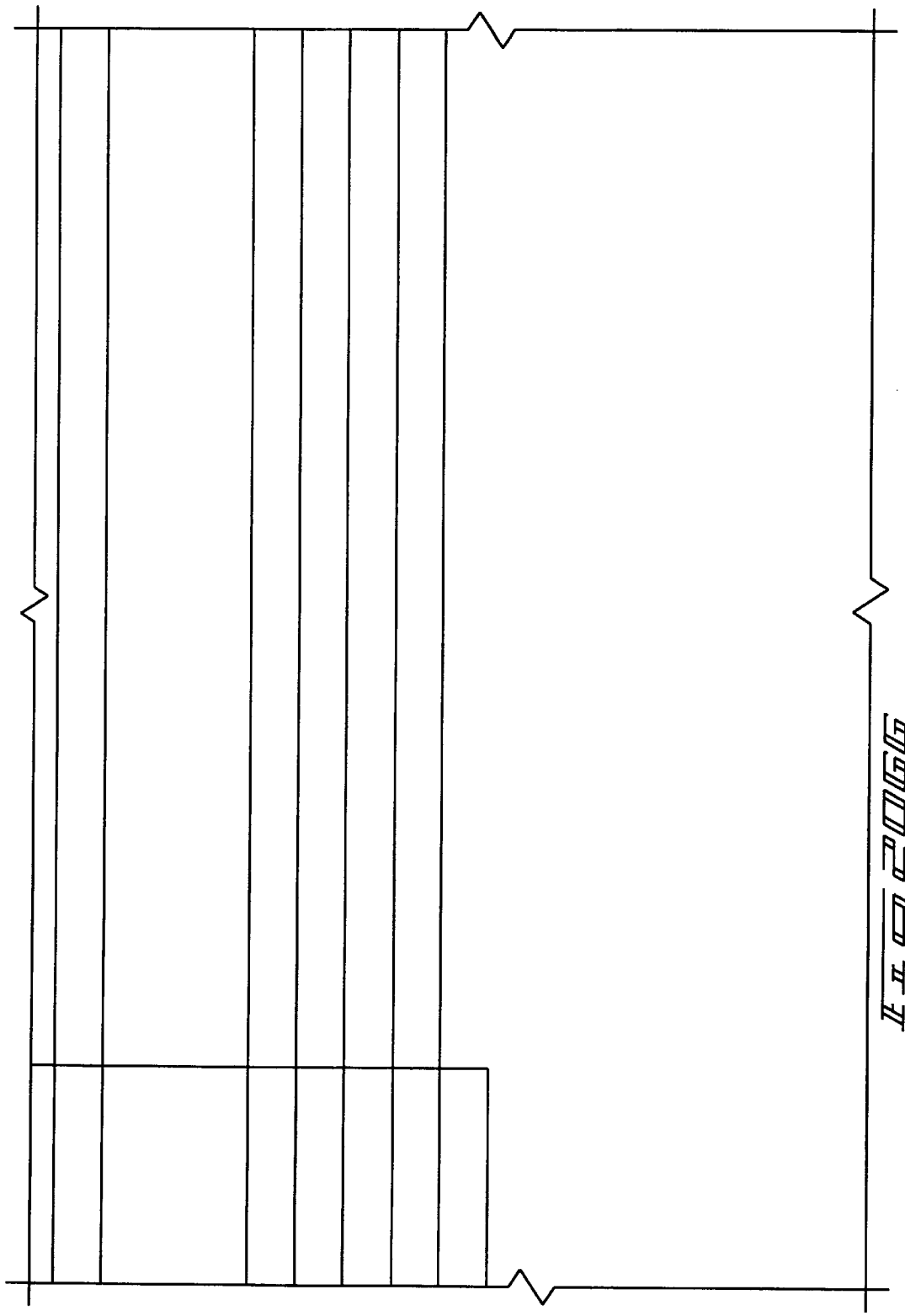


FIG 59202

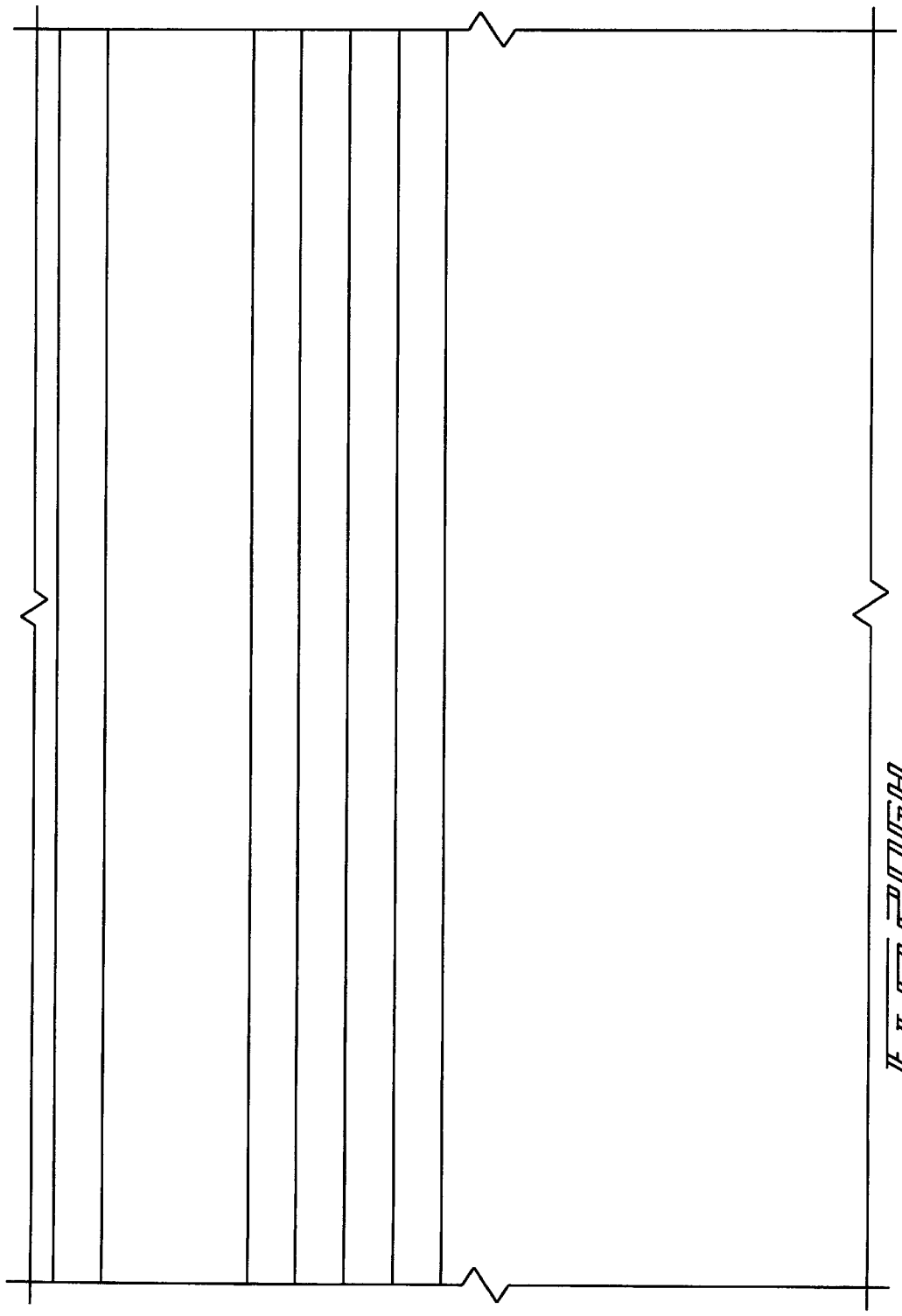


FIG 24900H

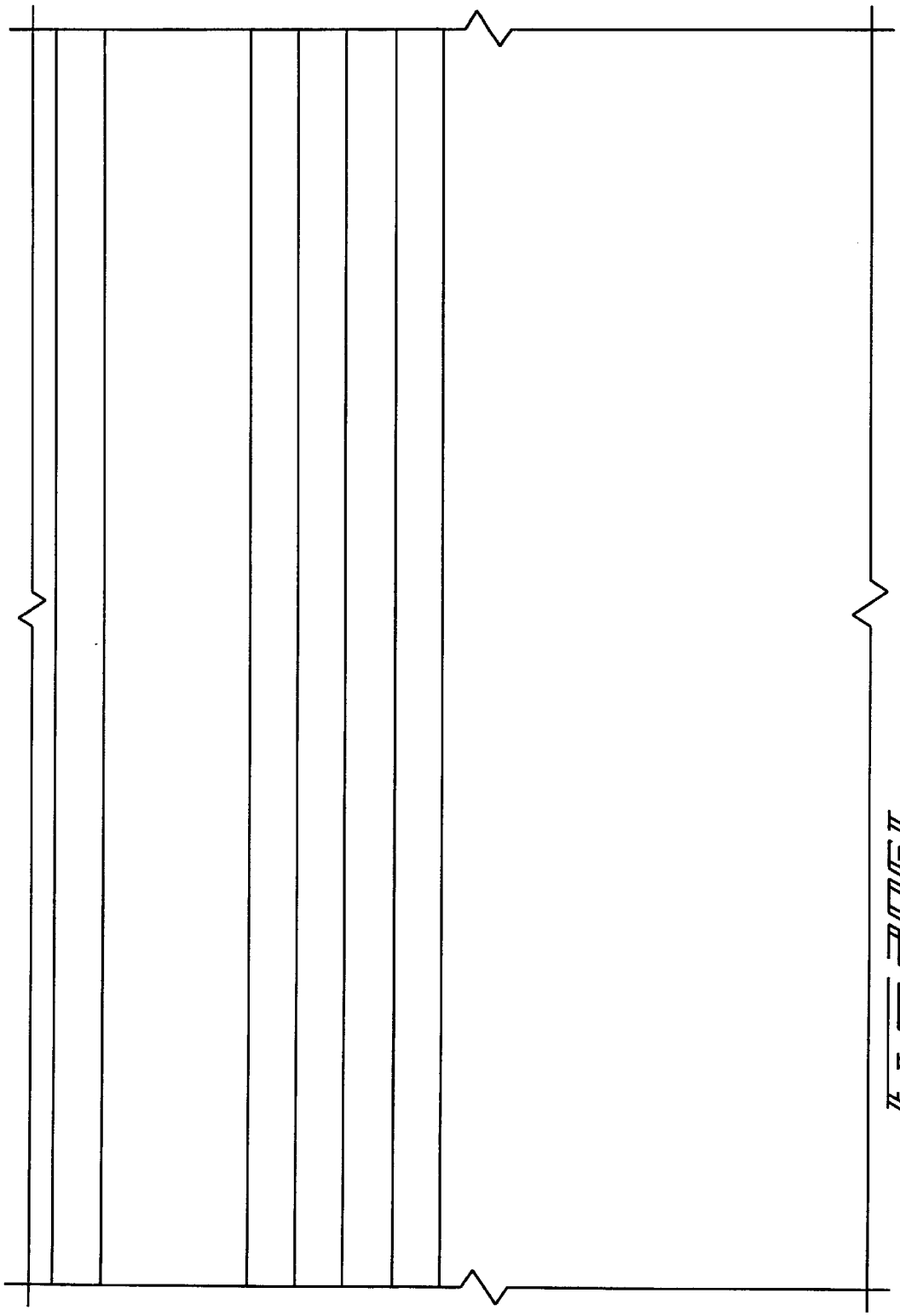


FIG 2001

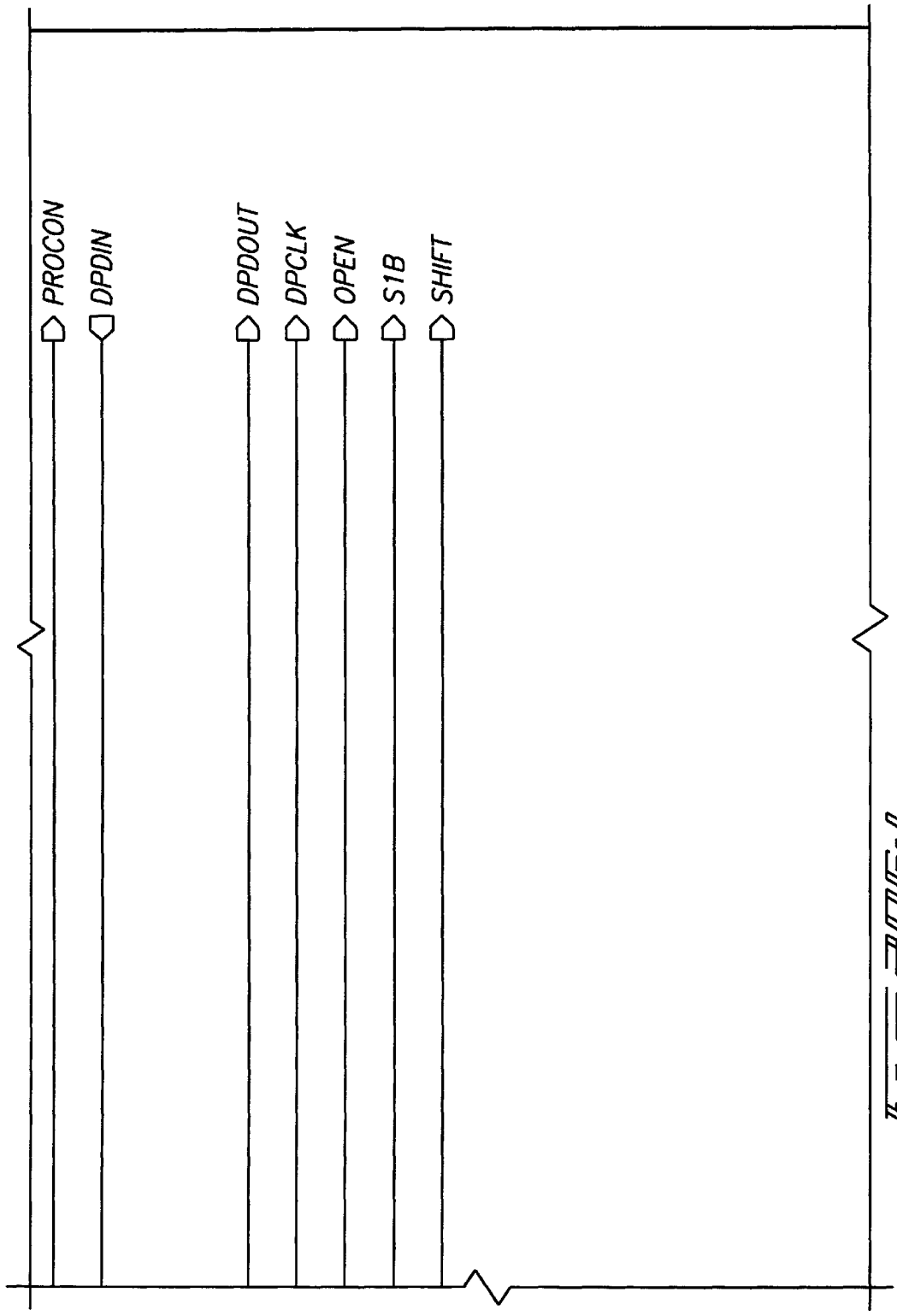


FIG 2090

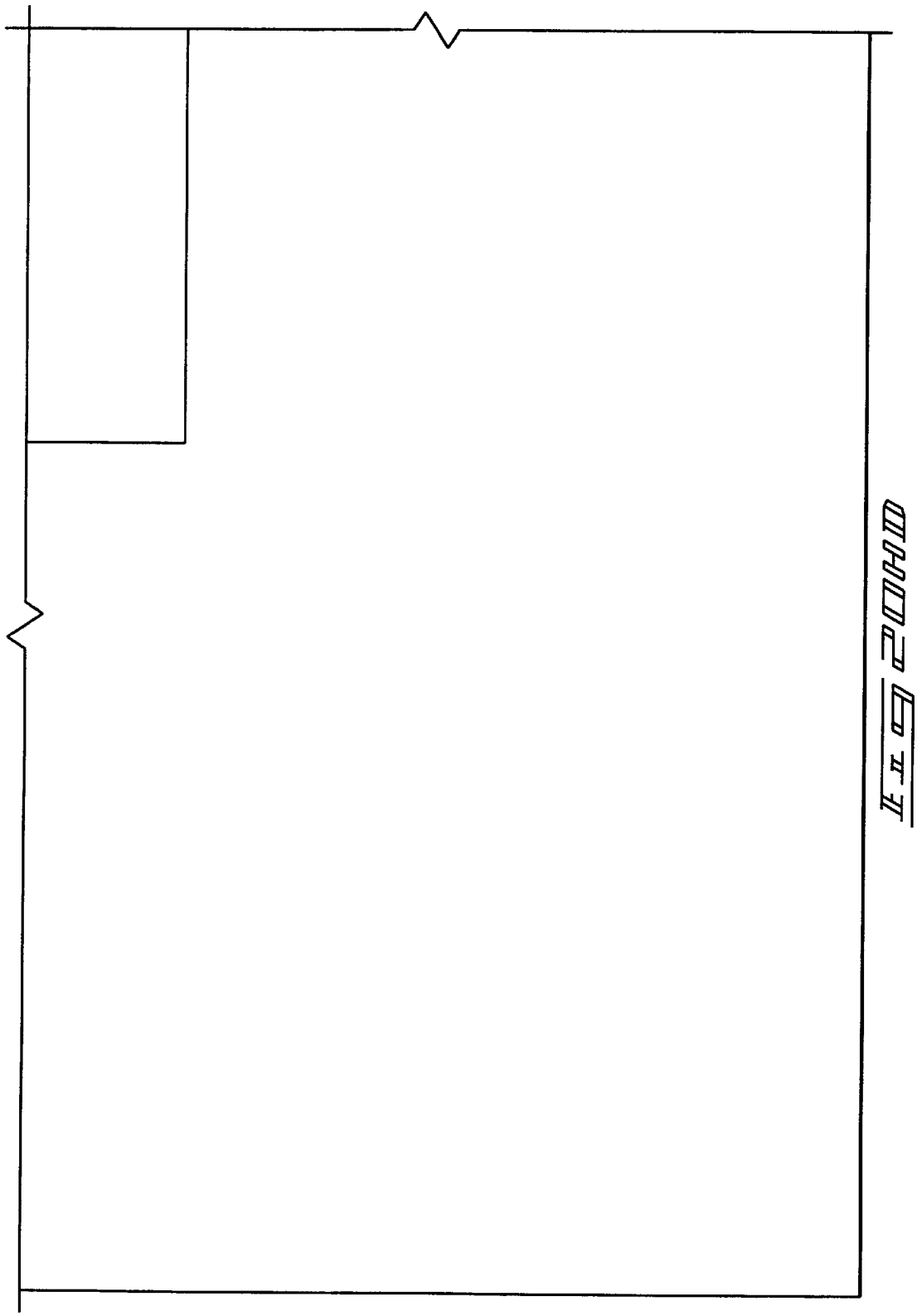


FIG 2040

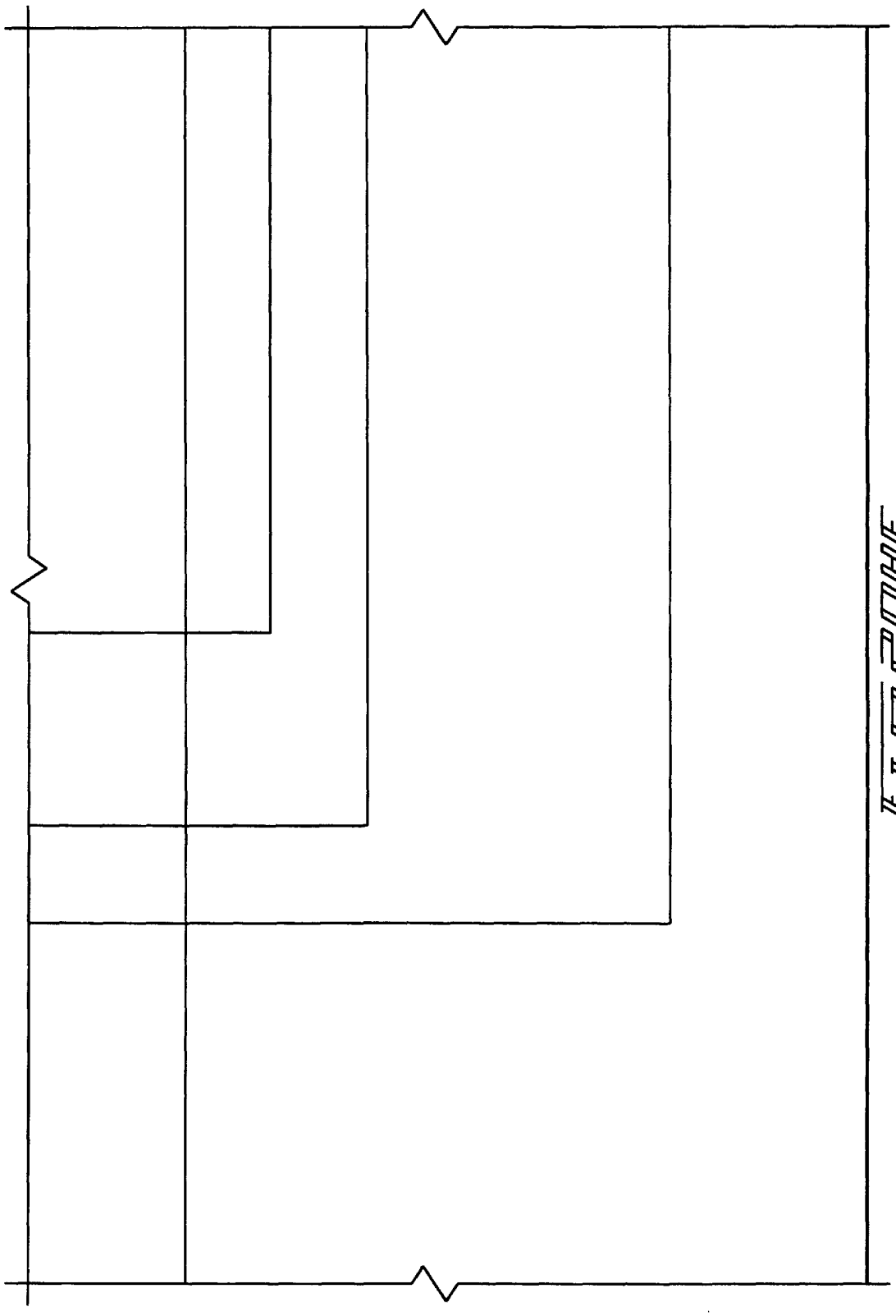


FIG 2DHE

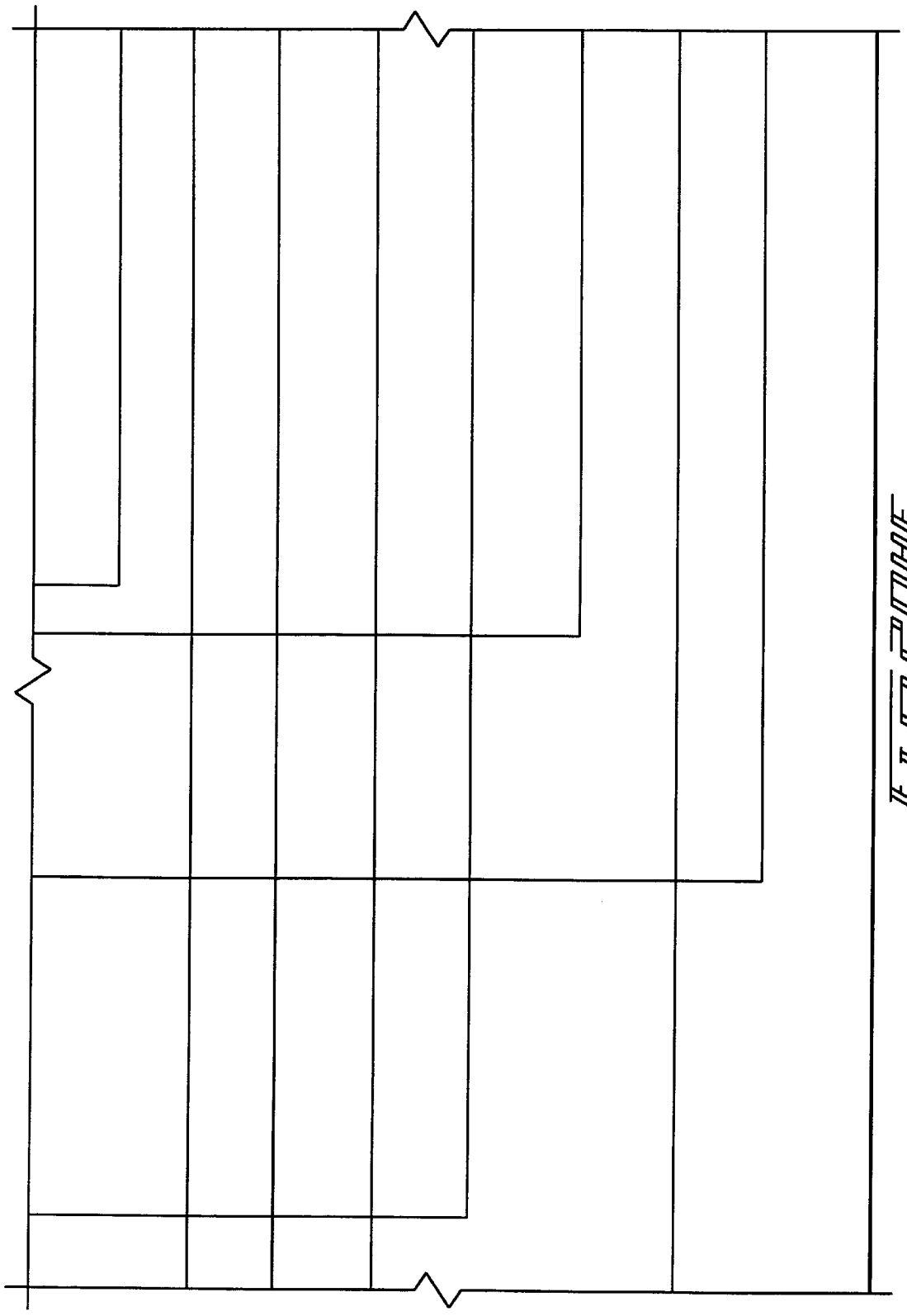


FIG 2044F

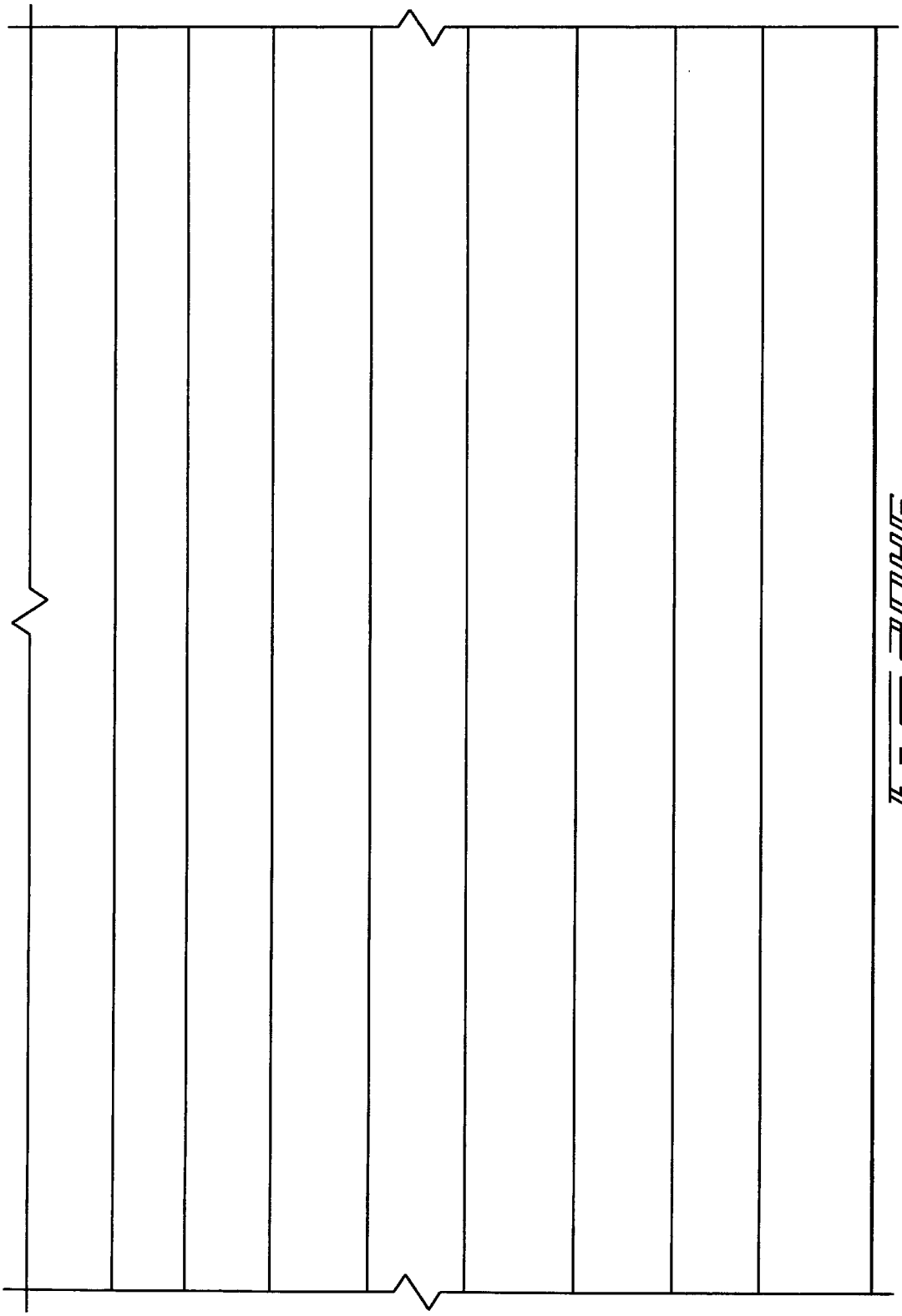


FIG 2002

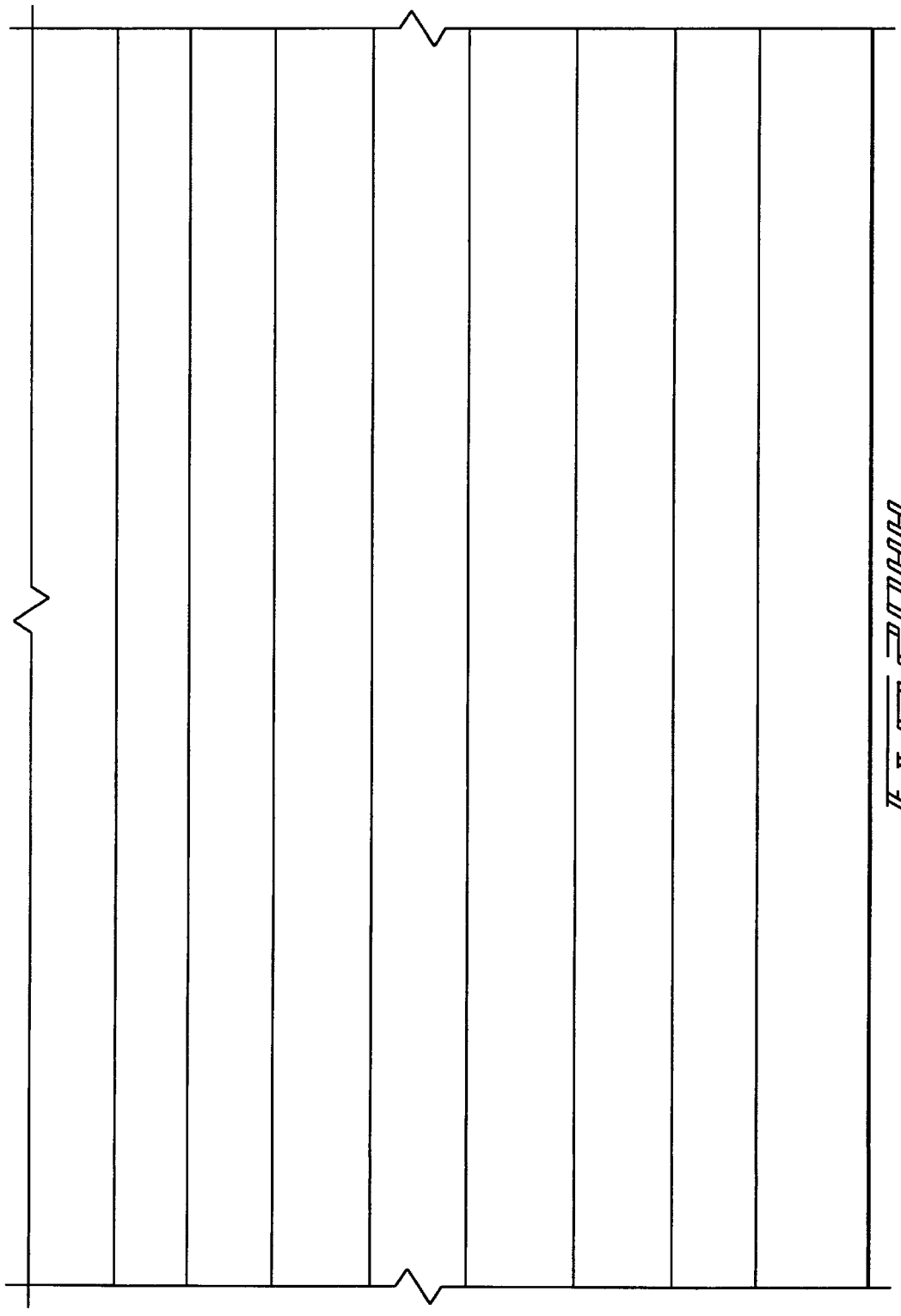


FIG 2004

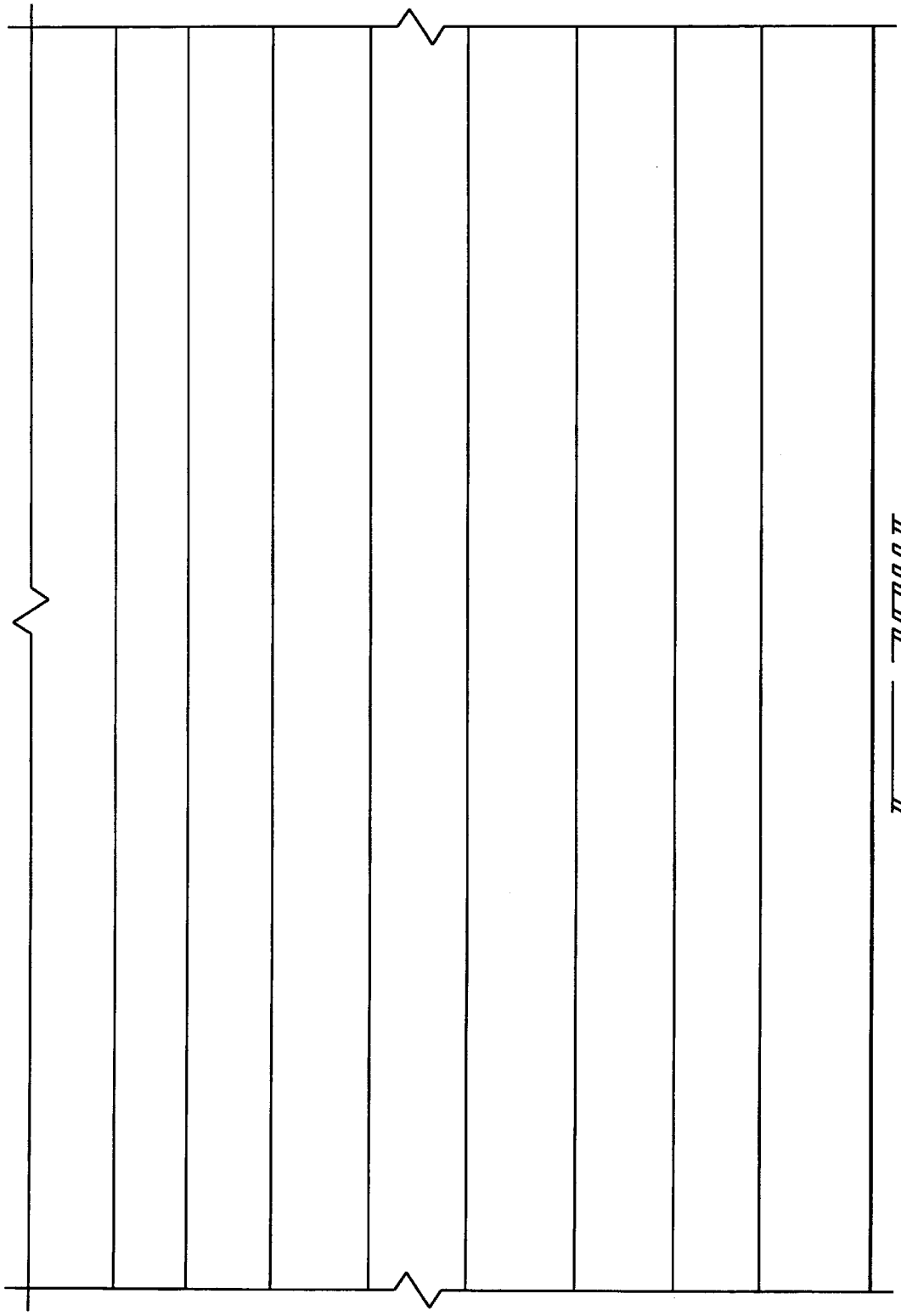


FIG 2602

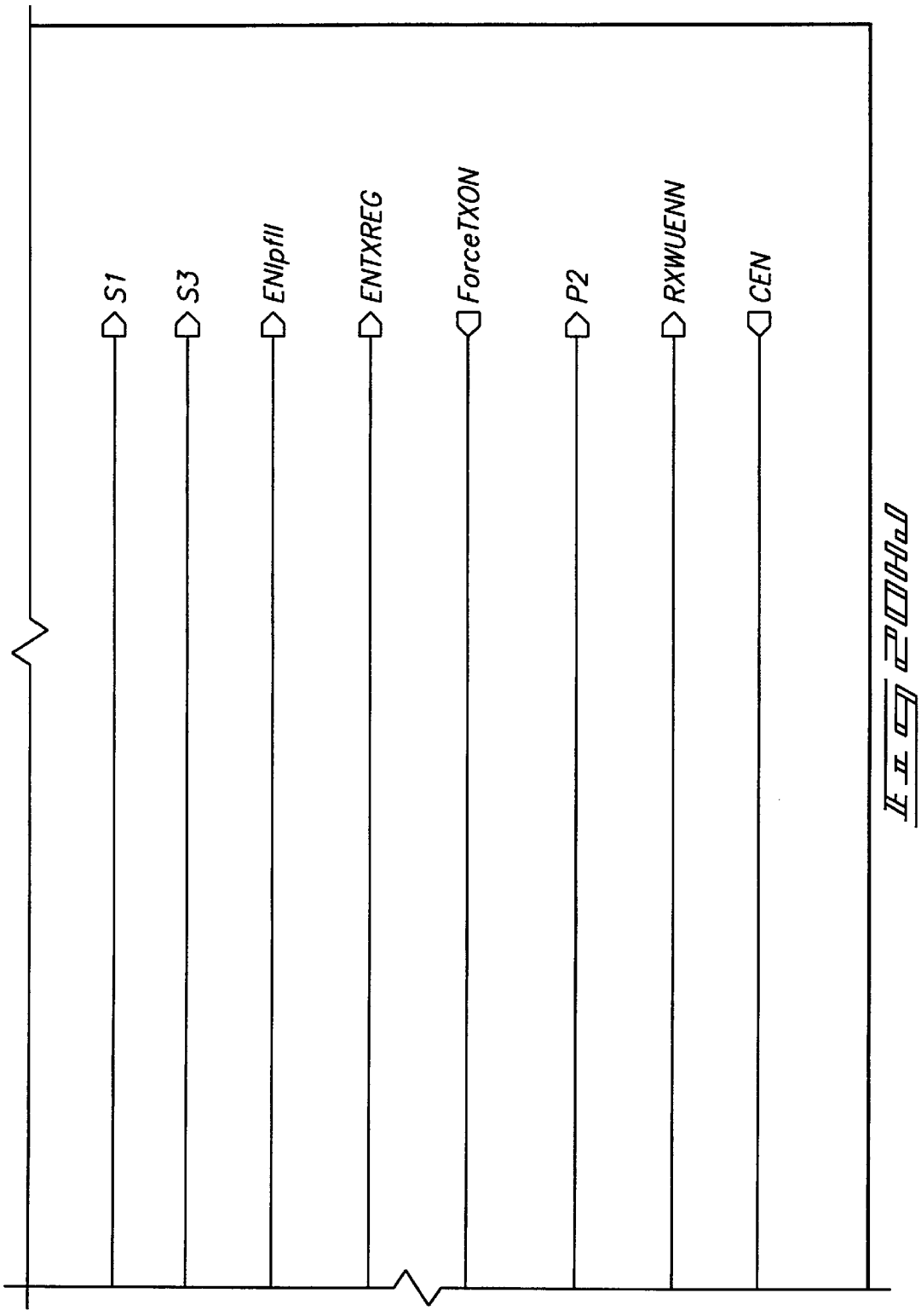


FIG 2004

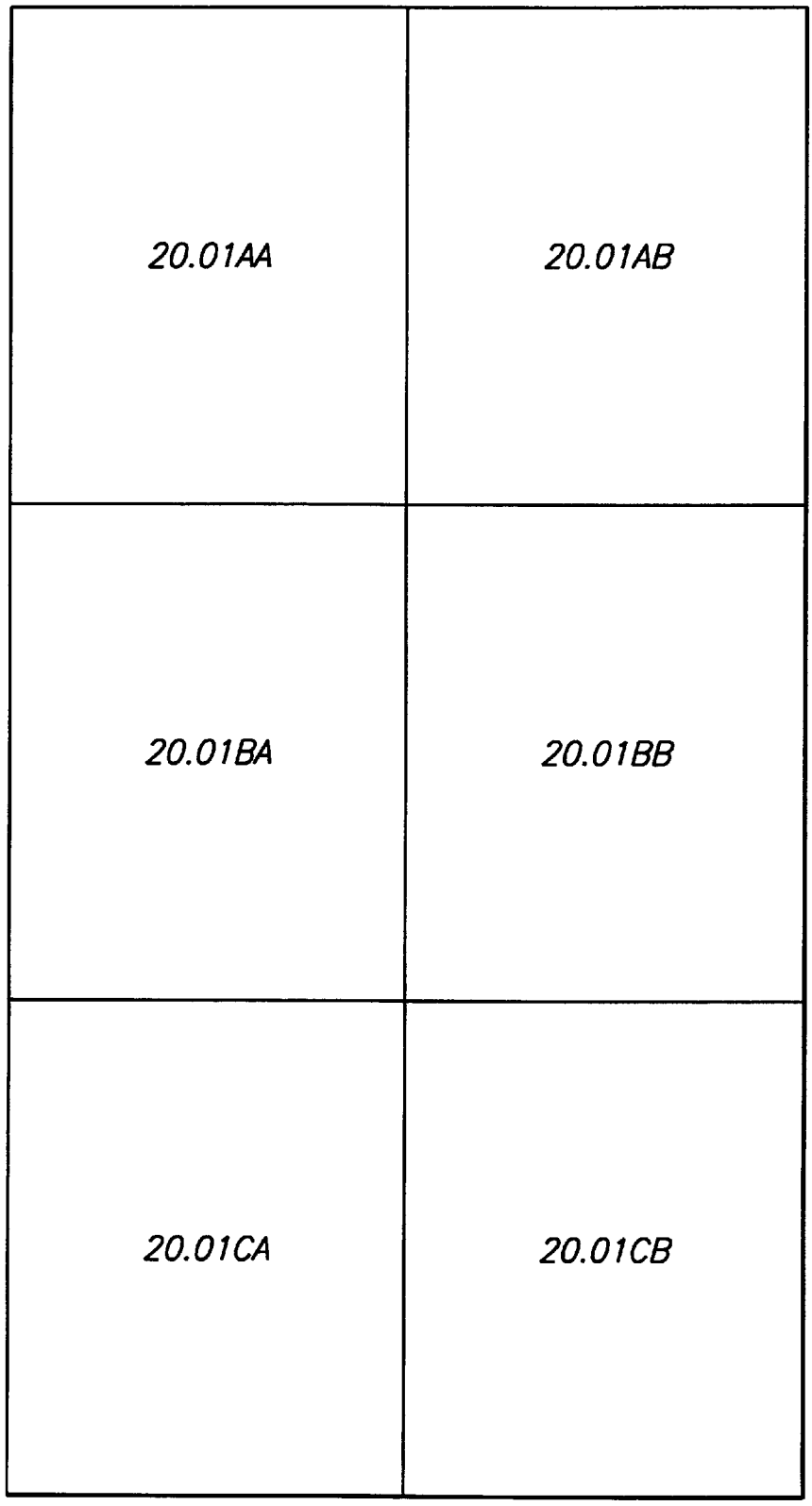


Fig 20.01

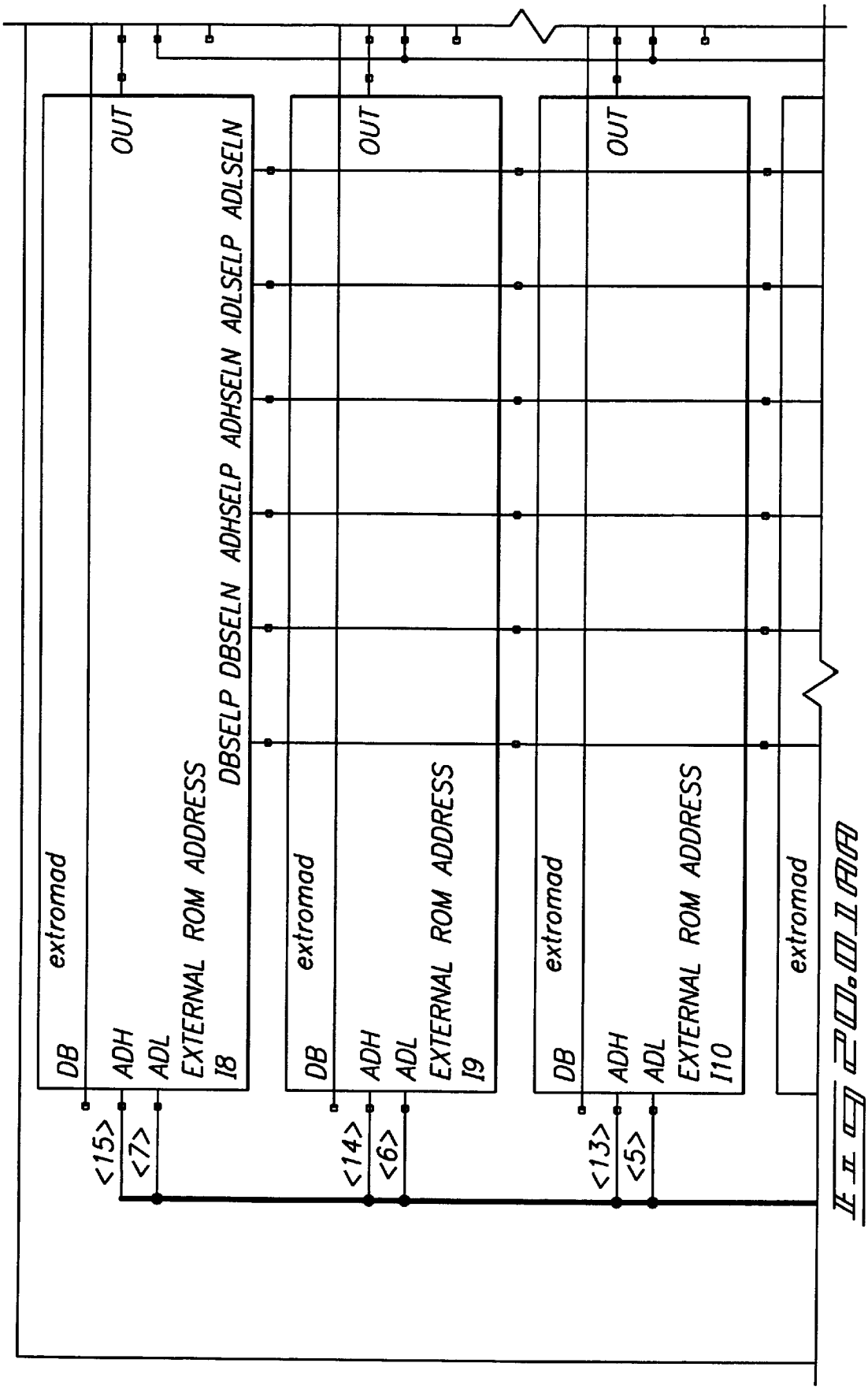

extromad
DB
ADH
ADL
EXTERNAL ROM ADDRESS
I8
DBSELP DBSELN ADHSELP ADHSELN ADLSELP ADLSELN
OUT
<15>
<7>
extromad
DB
ADH
ADL
EXTERNAL ROM ADDRESS
I9
OUT
<14>
<6>
extromad
DB
ADH
ADL
EXTERNAL ROM ADDRESS
I10
OUT
<13>
<5>
extromad

FIG 200.11AA

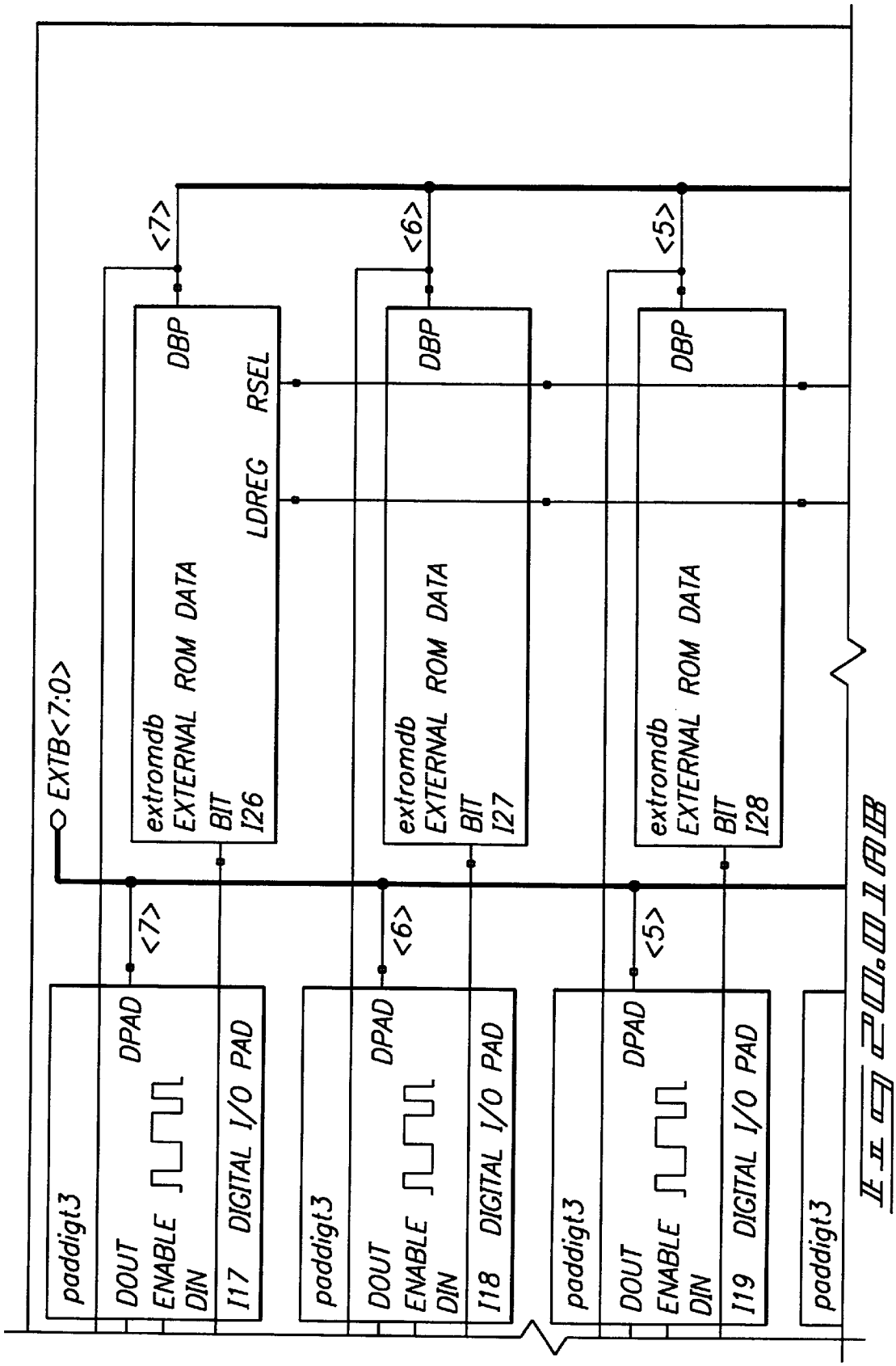

EXTB<7:0>
<7>
<6>
<5>
DBP
RSEL
LDREG
extromdb
EXTERNAL ROM DATA
BIT
I26
I27
I28
paddigt3
DOUT
ENABLE
DIN
DPAD
I17 DIGITAL I/O PAD
I18 DIGITAL I/O PAD
I19 DIGITAL I/O PAD

FIG 200.01AB

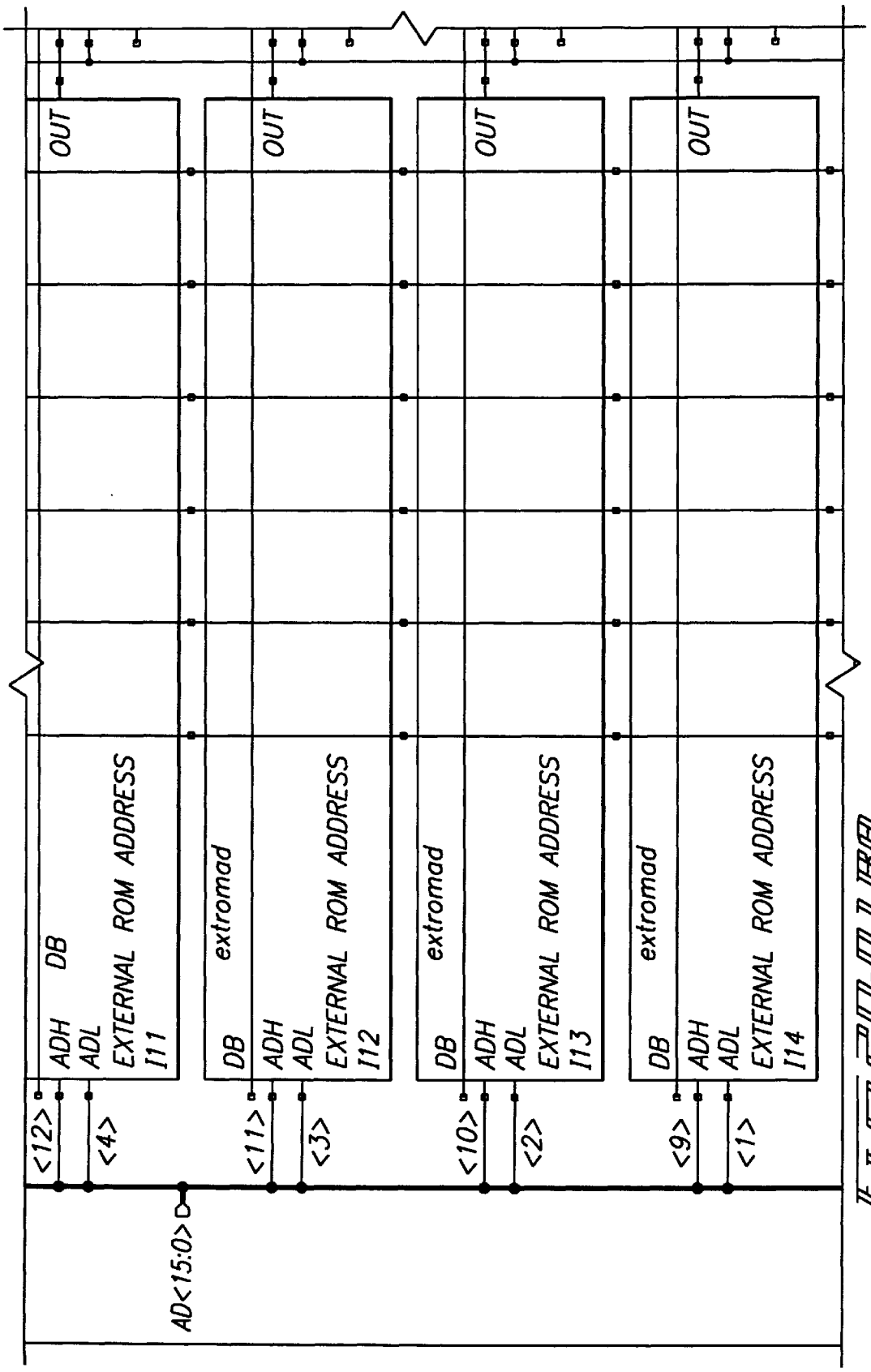

OUT
DB
ADH
ADL
EXTERNAL ROM ADDRESS
I11
extromad
I12
I13
I14
<12>
<4>
<11>
<3>
<10>
<2>
<9>
<1>
AD<15:0>

FIG 200.011B

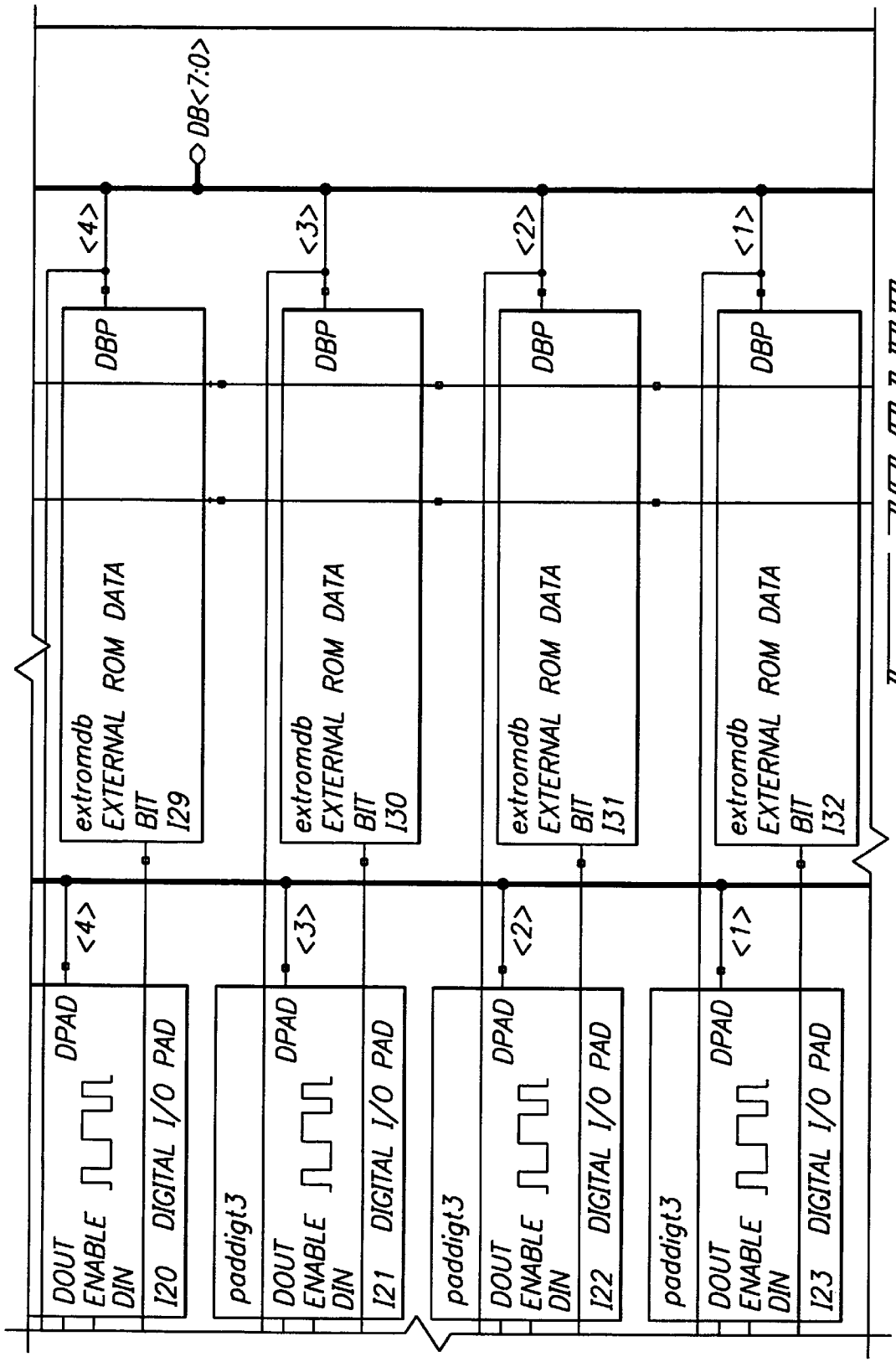

DB<7:0>
<4>
<3>
<2>
<1>
DBP
extromdb
EXTERNAL ROM DATA
BIT
I29
I30
I31
I32
DPAD
DOUT
ENABLE
DIN
I20 DIGITAL I/O PAD
I21 DIGITAL I/O PAD
I22 DIGITAL I/O PAD
I23 DIGITAL I/O PAD
paddigt3

FIG 2100.III

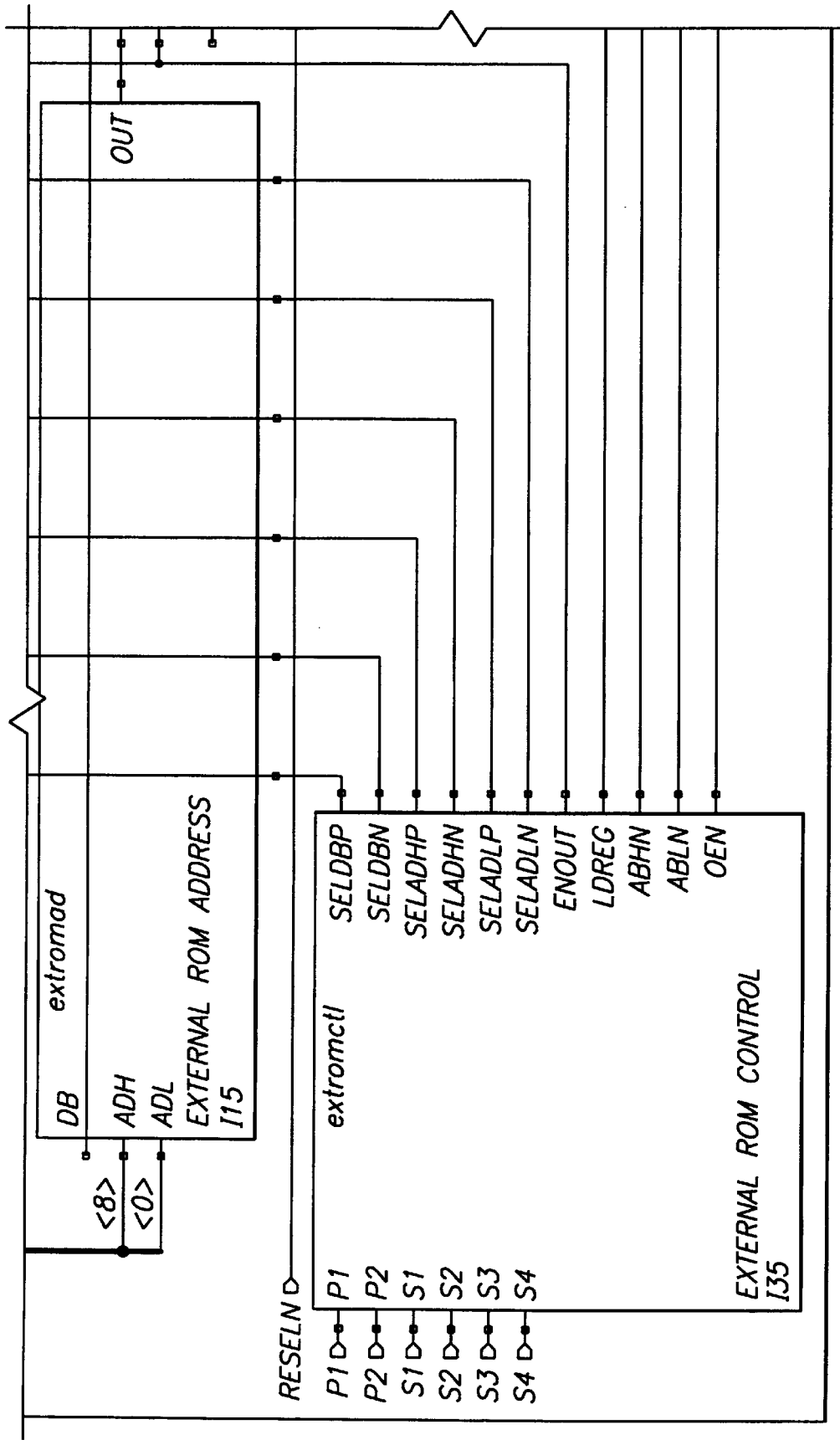


FIG 200.011CA

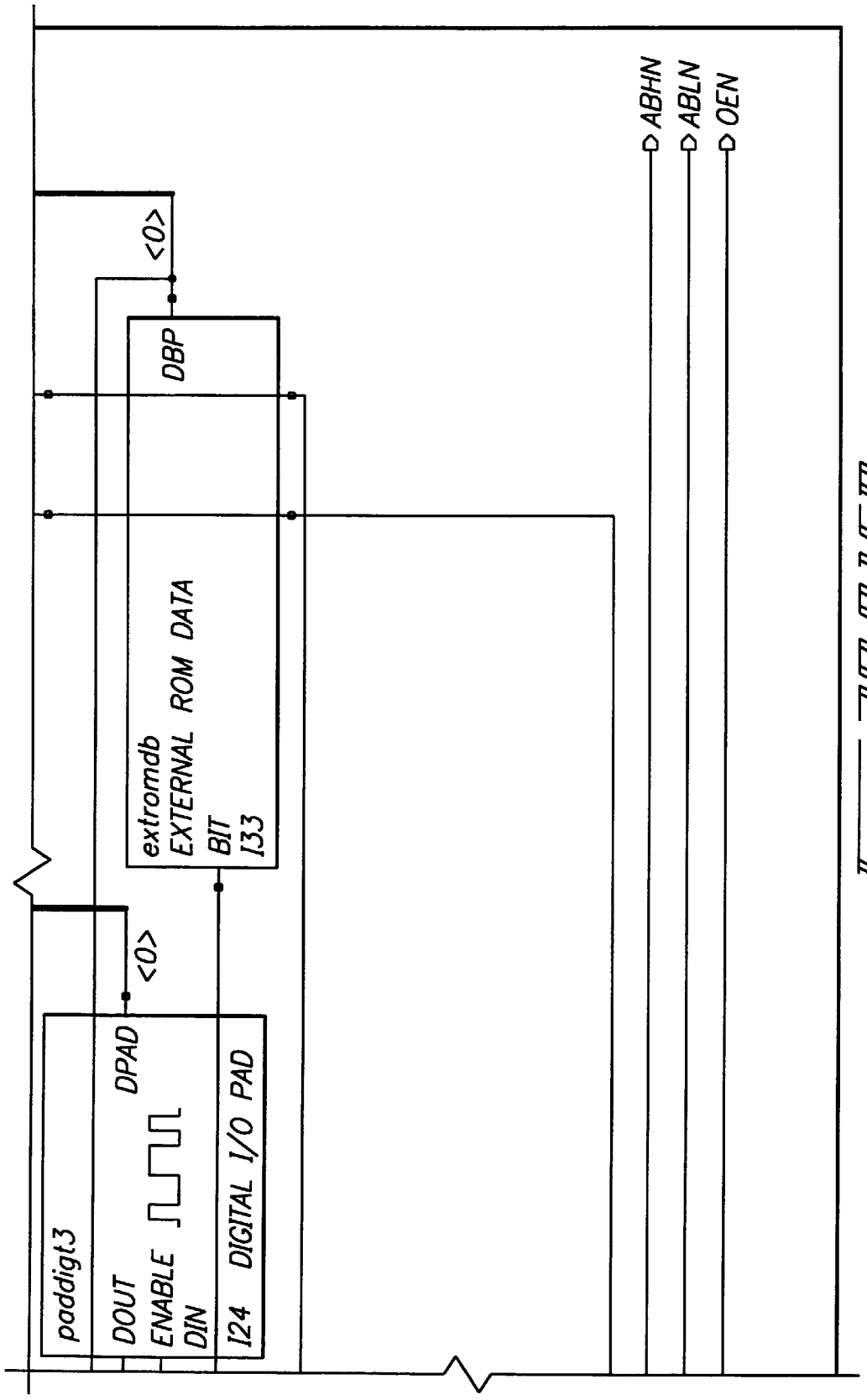

ABHN
ABLN
OEN
<0>
DBP
extromdb
EXTERNAL ROM DATA
BIT
133
<0>
DPAD
paddigt3
DOUT
ENABLE
DIN
124 DIGITAL I/O PAD

Fig 200,011B

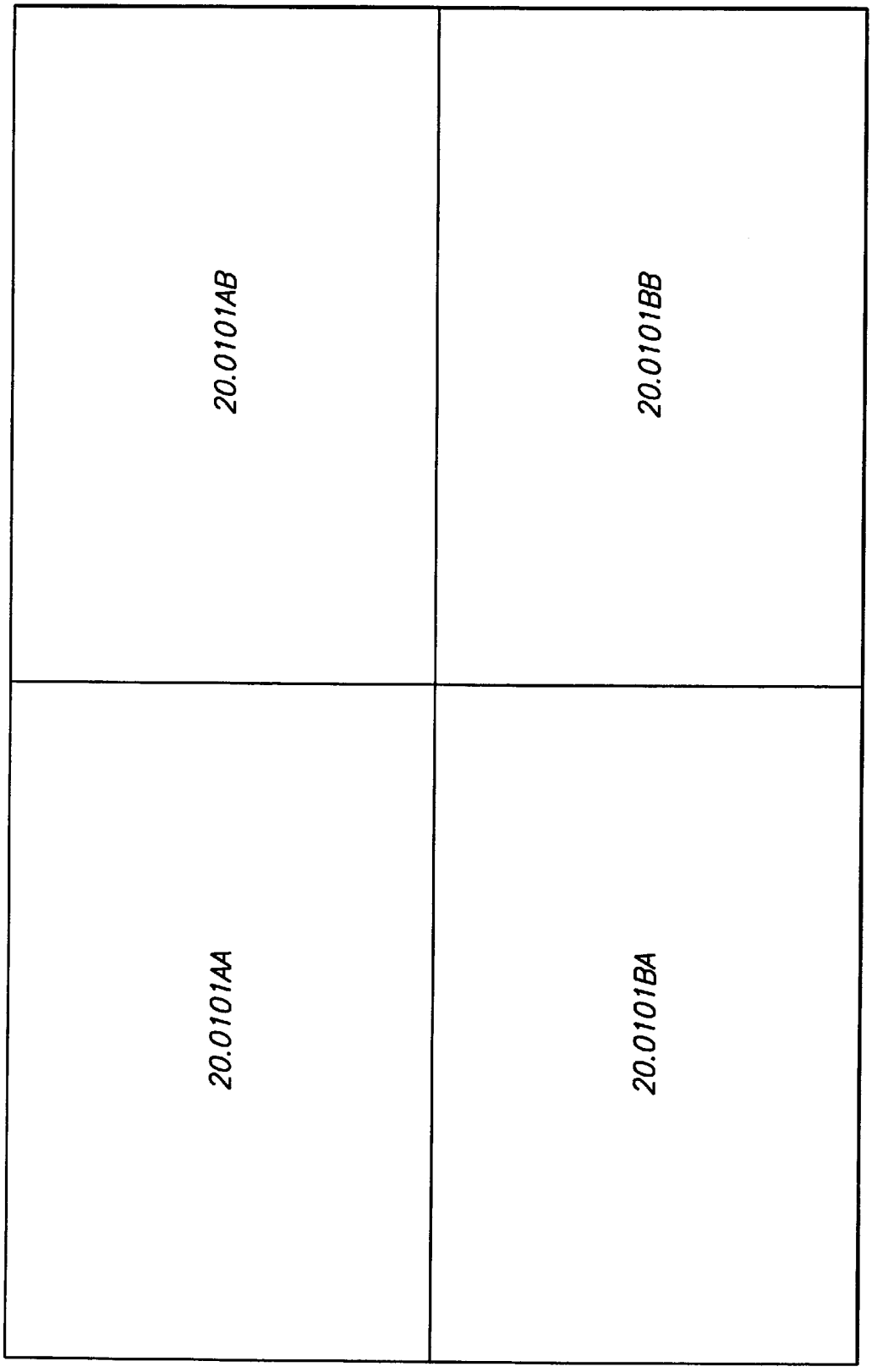


FIG 20.0101

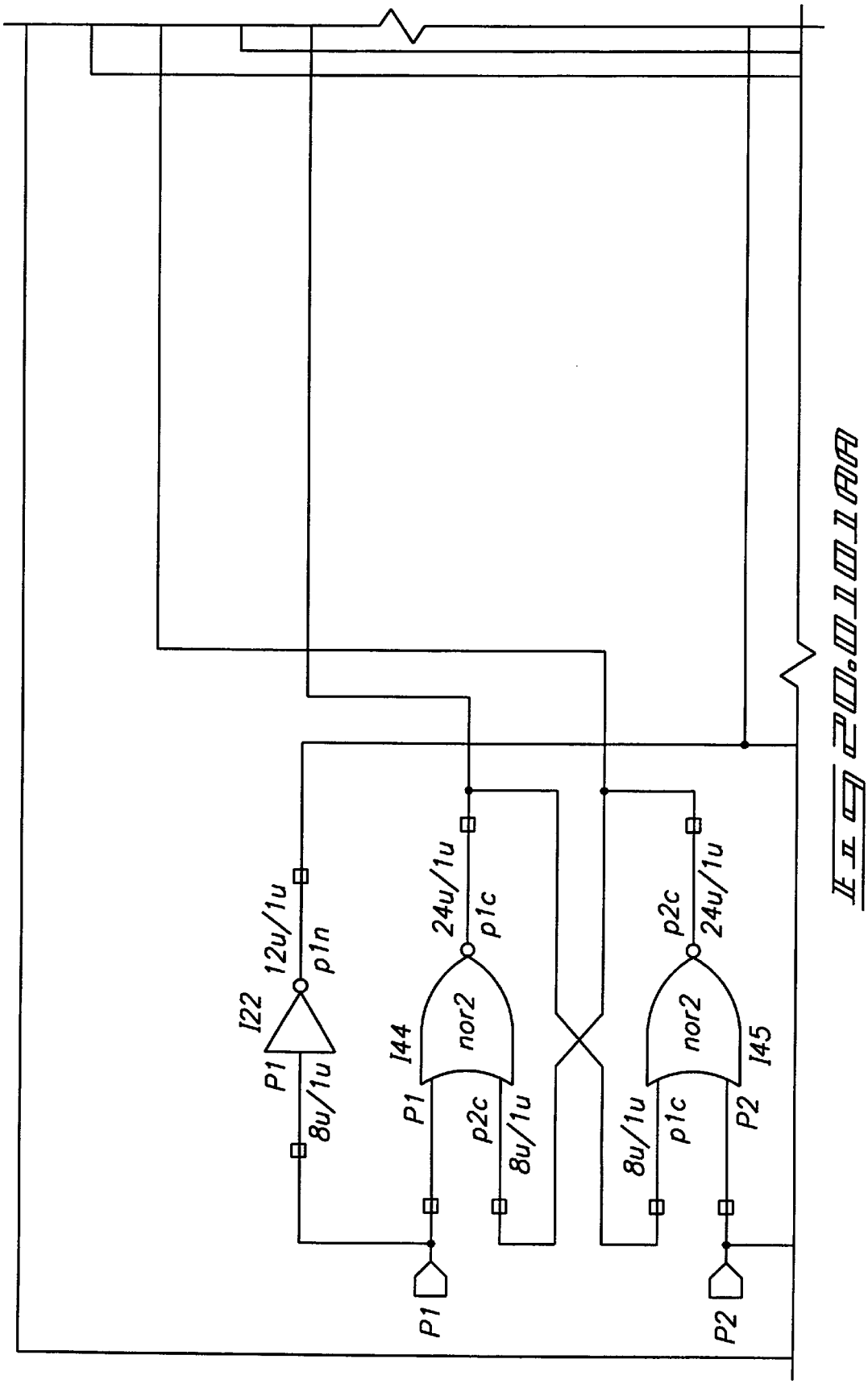


FIG 210.01011AA

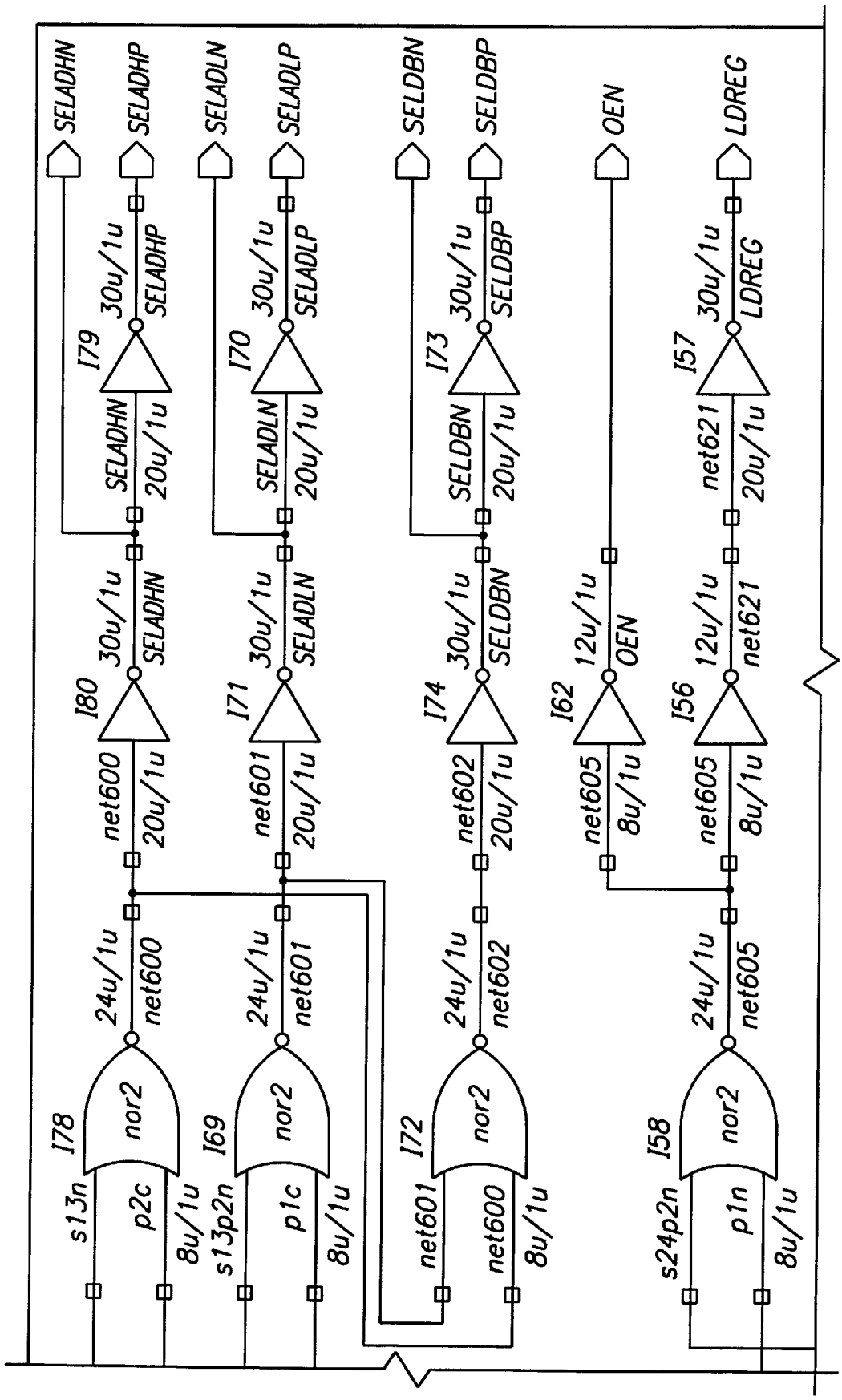


FIG 2000.III.II.AIB

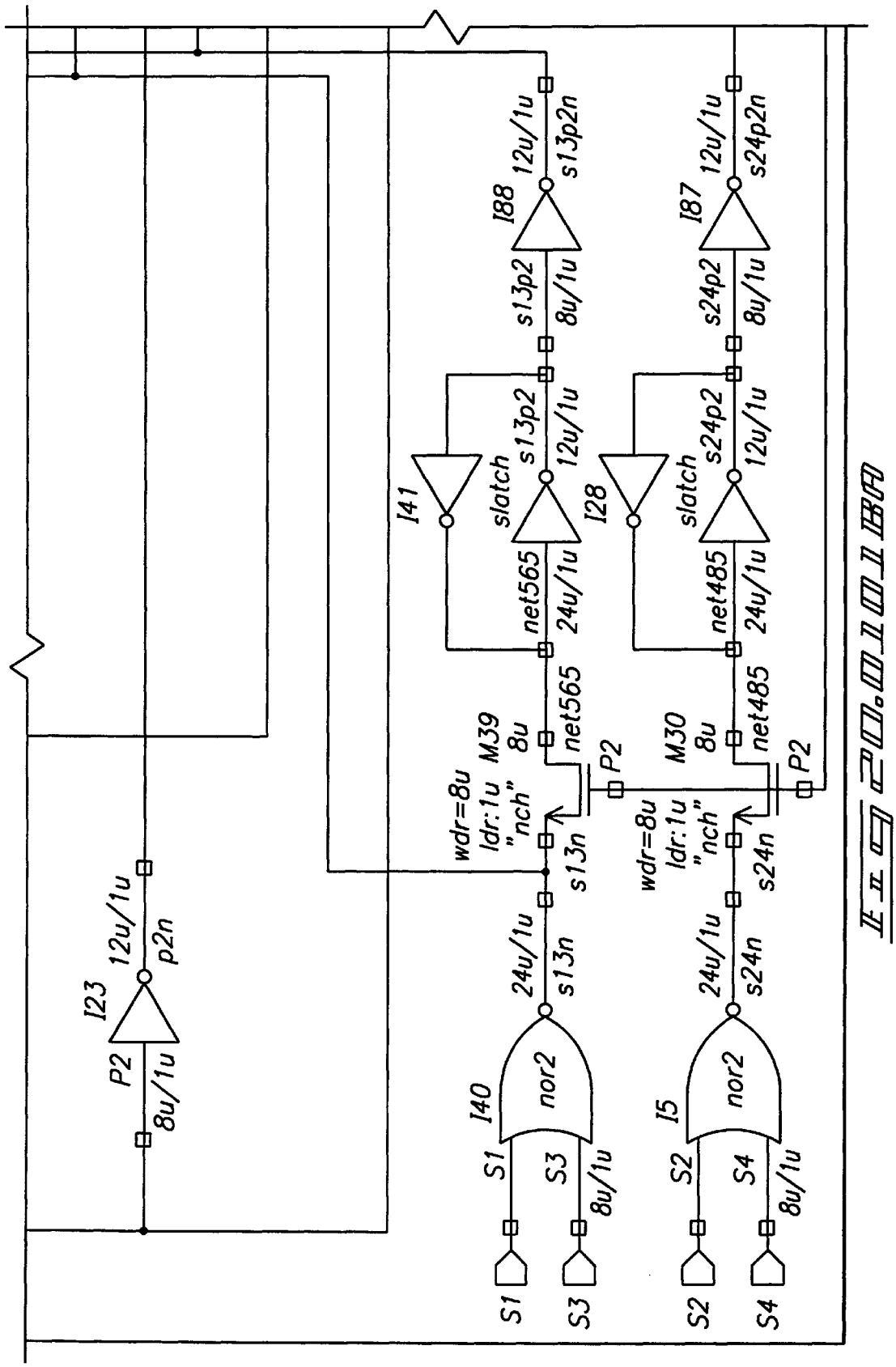


Fig 2003.III.IBM

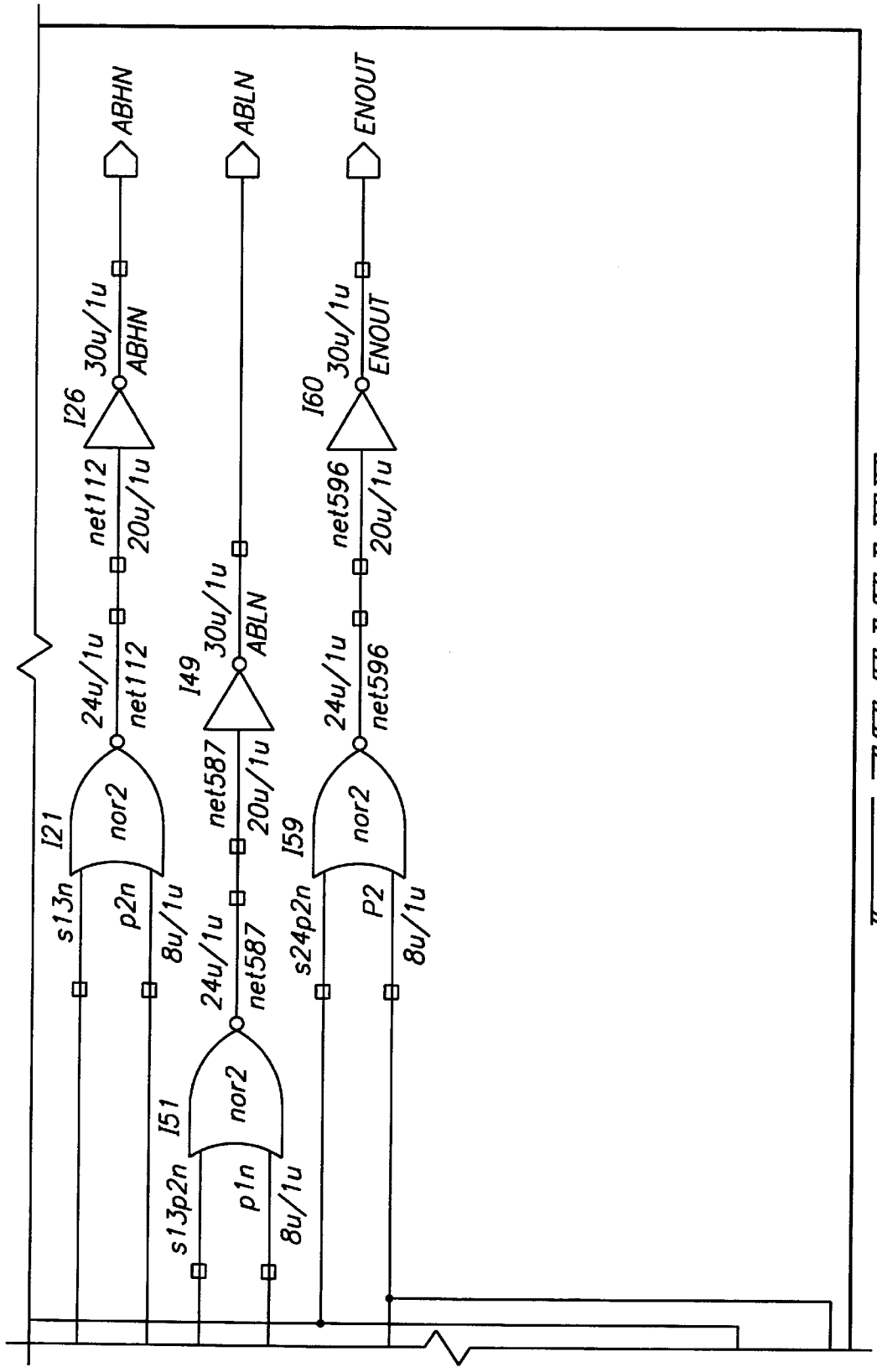


FIG 20.0011BB

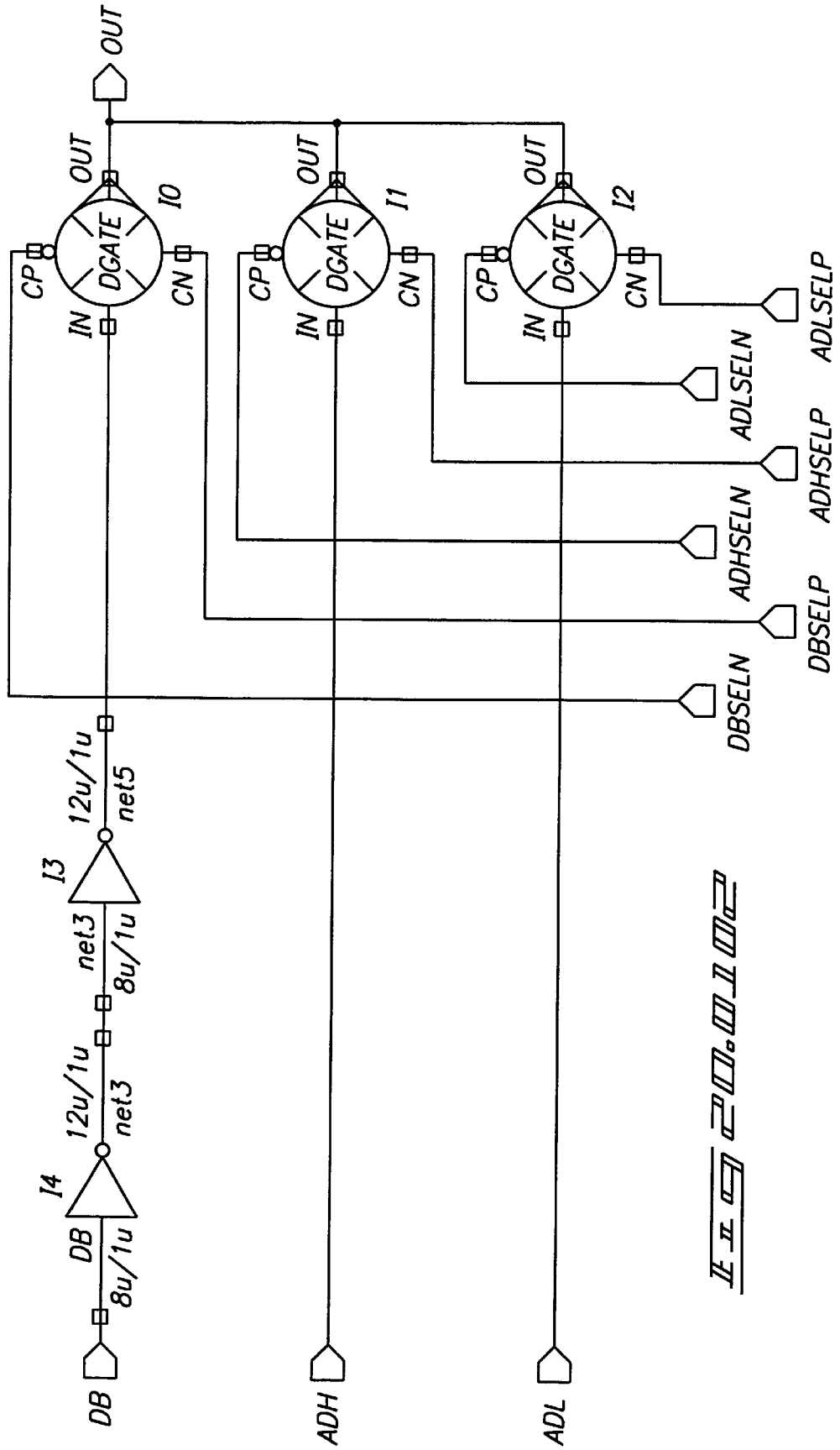
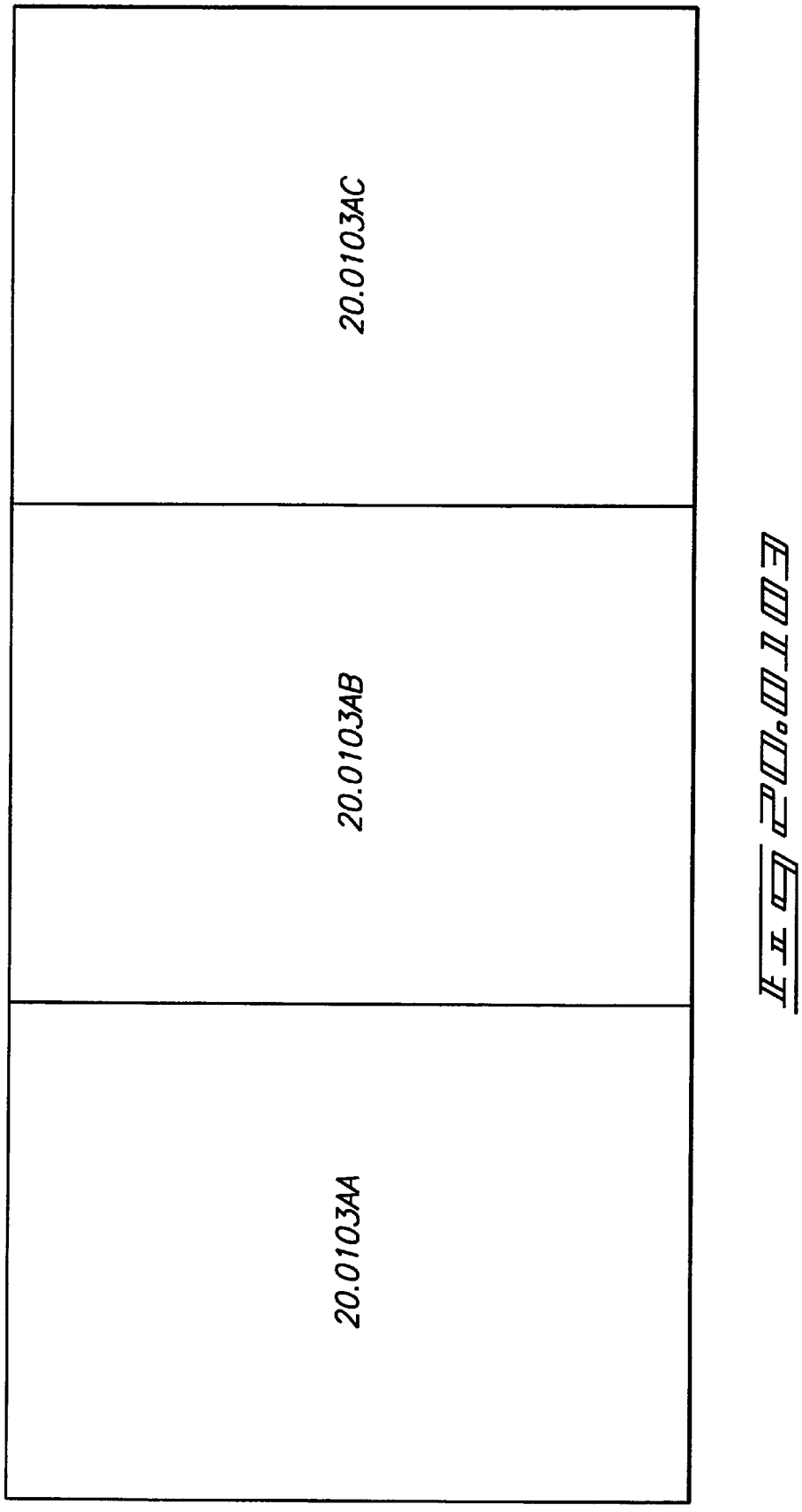

OUT
OUT
I0
DGATE
CP
IN
CN
OUT
I1
DGATE
CP
IN
CN
OUT
I2
DGATE
CP
IN
CN
ADLSELP
ADLSELN
ADHSELP
ADHSELN
DBSELP
DBSELN
12u/1u
net5
I3
net3
8u/1u
12u/1u
net3
I4
DB
8u/1u
DB
ADH
ADL

FIG 2001.002


20.0103AC
20.0103AB
20.0103AA
EAST 200.00'

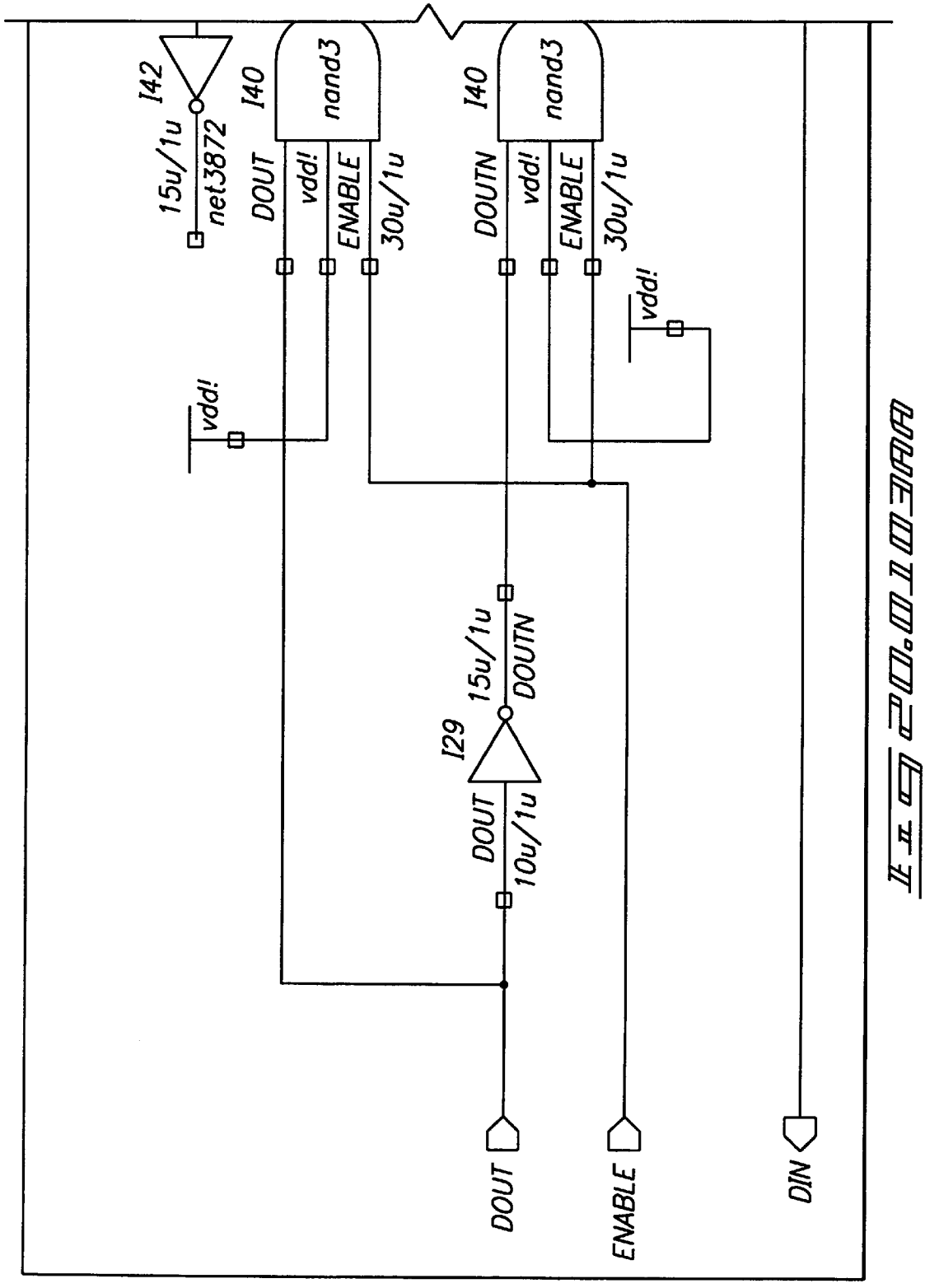

I42
15u/1u
net3872
I40
nand3
DOUT
vdd!
ENABLE
30u/1u
I40
nand3
DOUTN
vdd!
ENABLE
30u/1u
vdd!
vdd!
I29
15u/1u
DOUTN
DOUT
10u/1u
DOUT
ENABLE
DIN

FIG. 2002.00.0

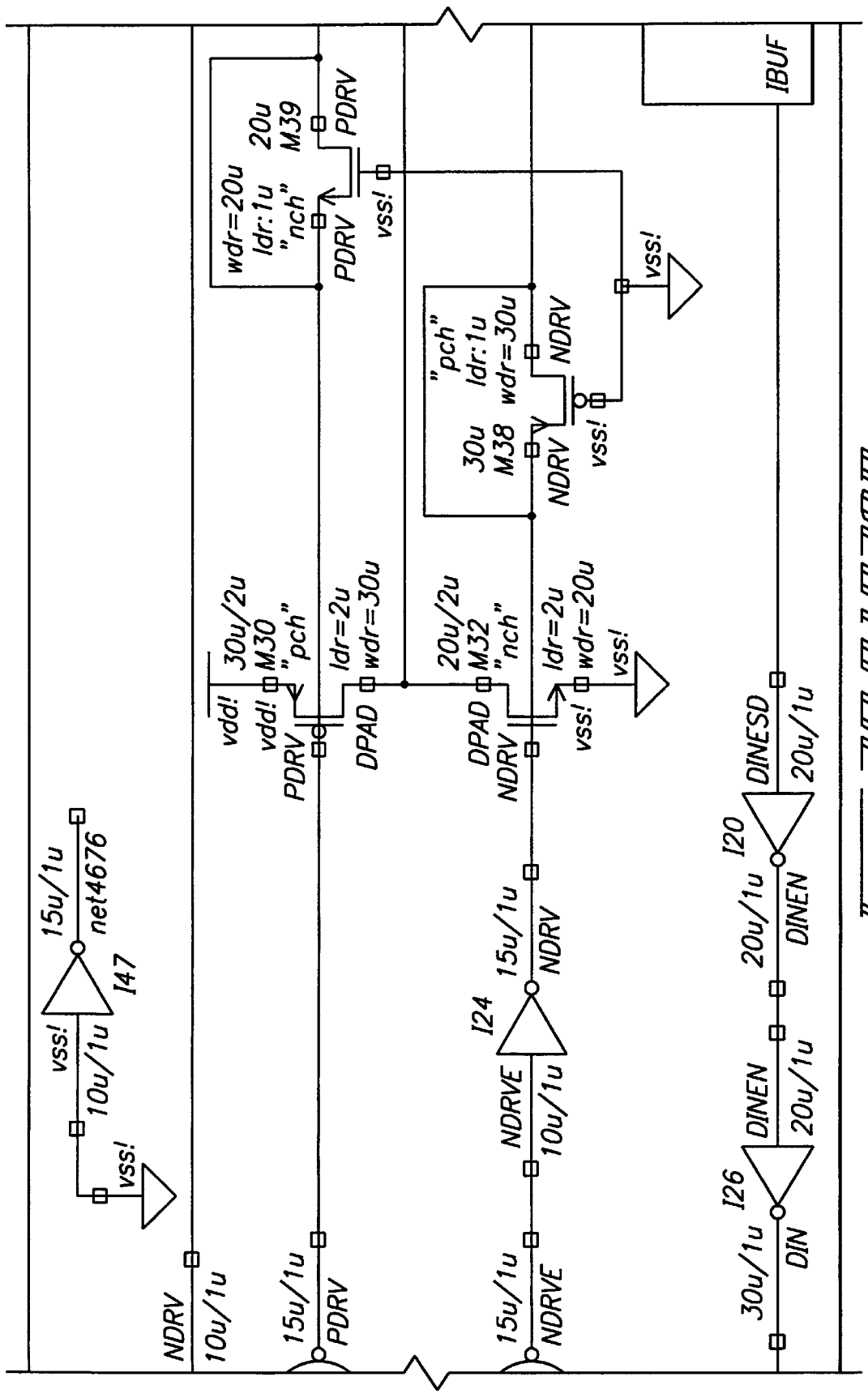


FIG 2.00.11.03AB

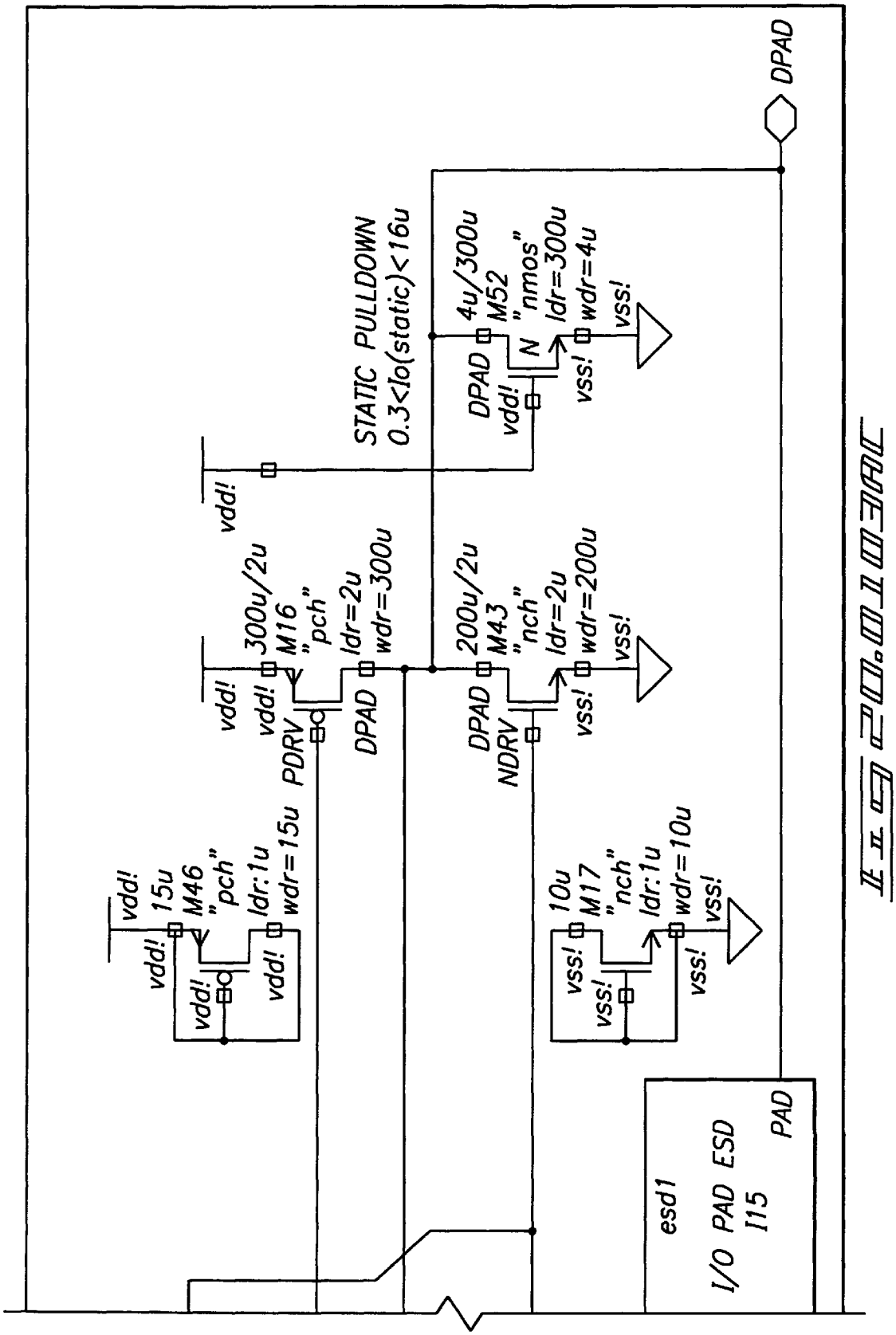


FIG 200.00 (PRIOR ART)

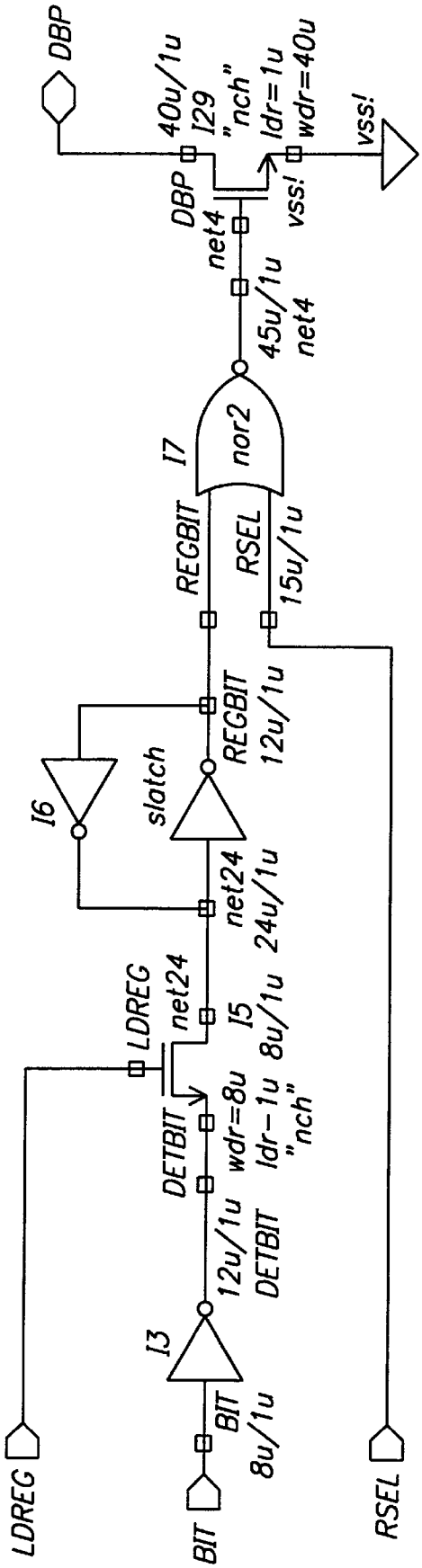

DBP
40u/1u
I29
"nch"
ldr=1u
wdr=40u
vss!
DBP
net4
vss!
45u/1u
net4
I7
nor2
REGBIT
RSEL
15u/1u
REGBIT
12u/1u
I6
slatch
net24
24u/1u
LDREG
net24
I5
8u/1u
DETBIT
wdr=8u
ldr=1u
"nch"
12u/1u
DETBIT
I3
BIT
8u/1u
LDREG
BIT
RSEL

FIG 2.0.0.1.0.4

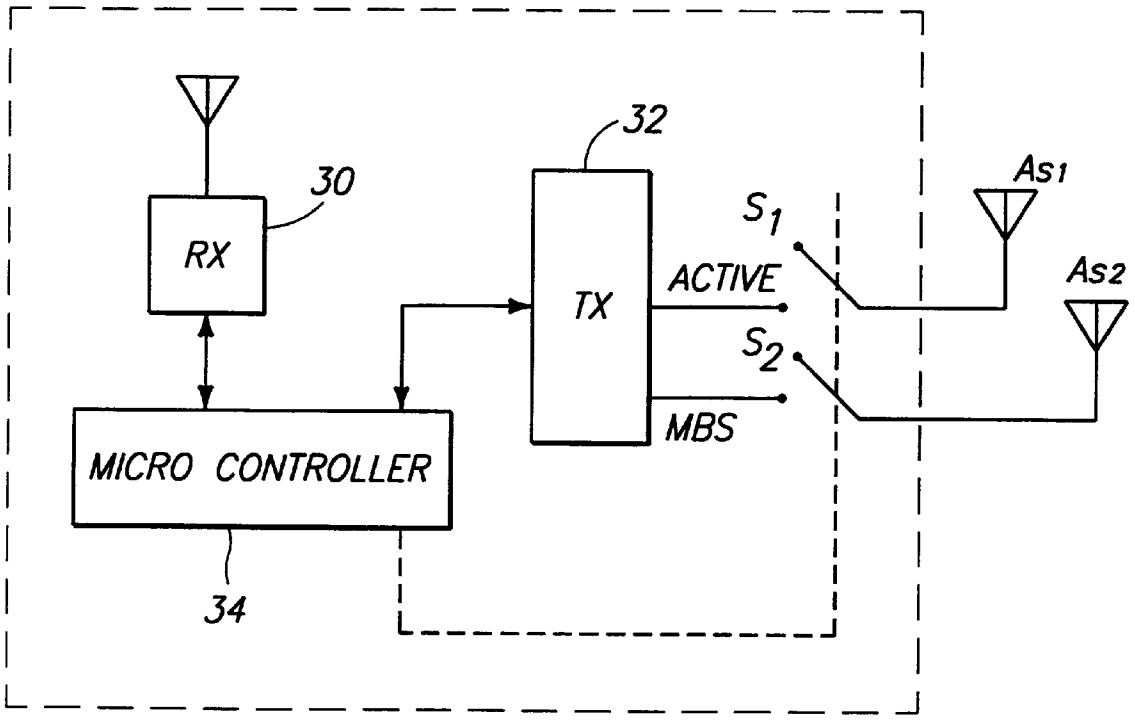

RX
30
32
TX
ACTIVE
MBS
S1
S2
As1
As2
MICRO CONTROLLER
34

Fig 21

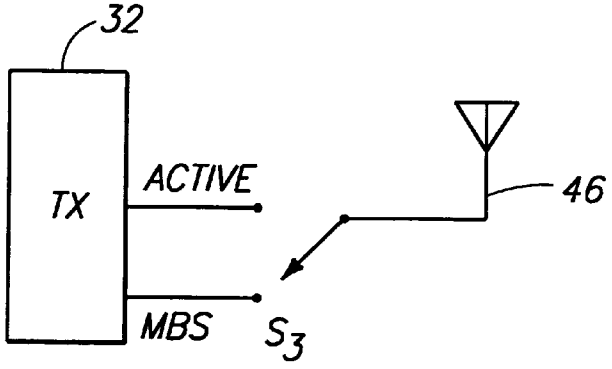
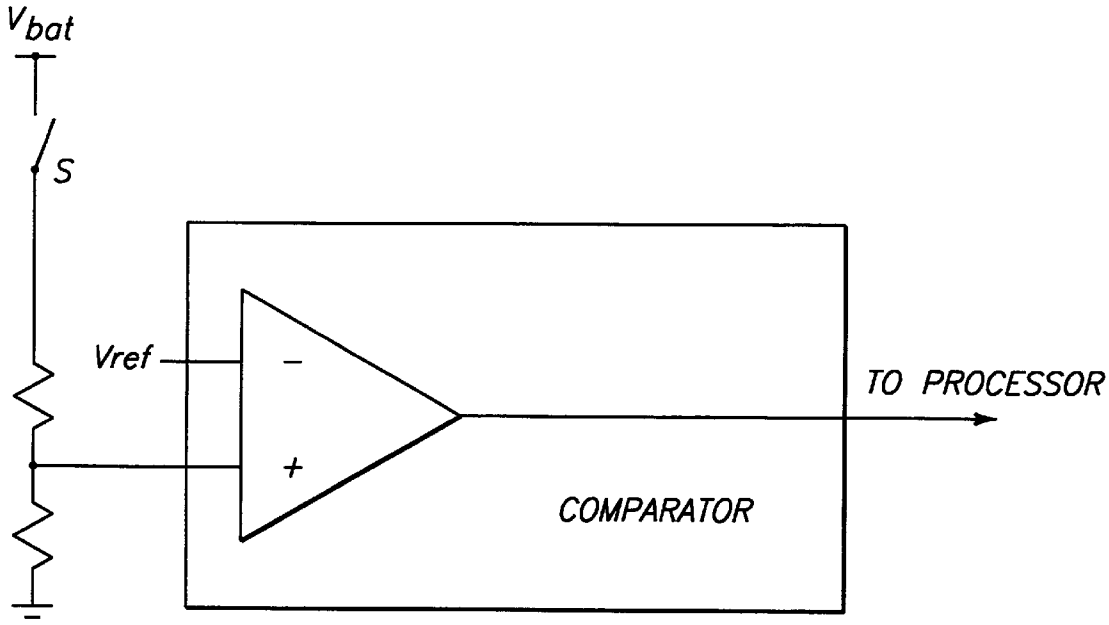

32
TX
ACTIVE
MBS
S3
46

Fig 22



V_{ref} = bandgap voltage ≈ 1.2 V for silicon

Fig 23

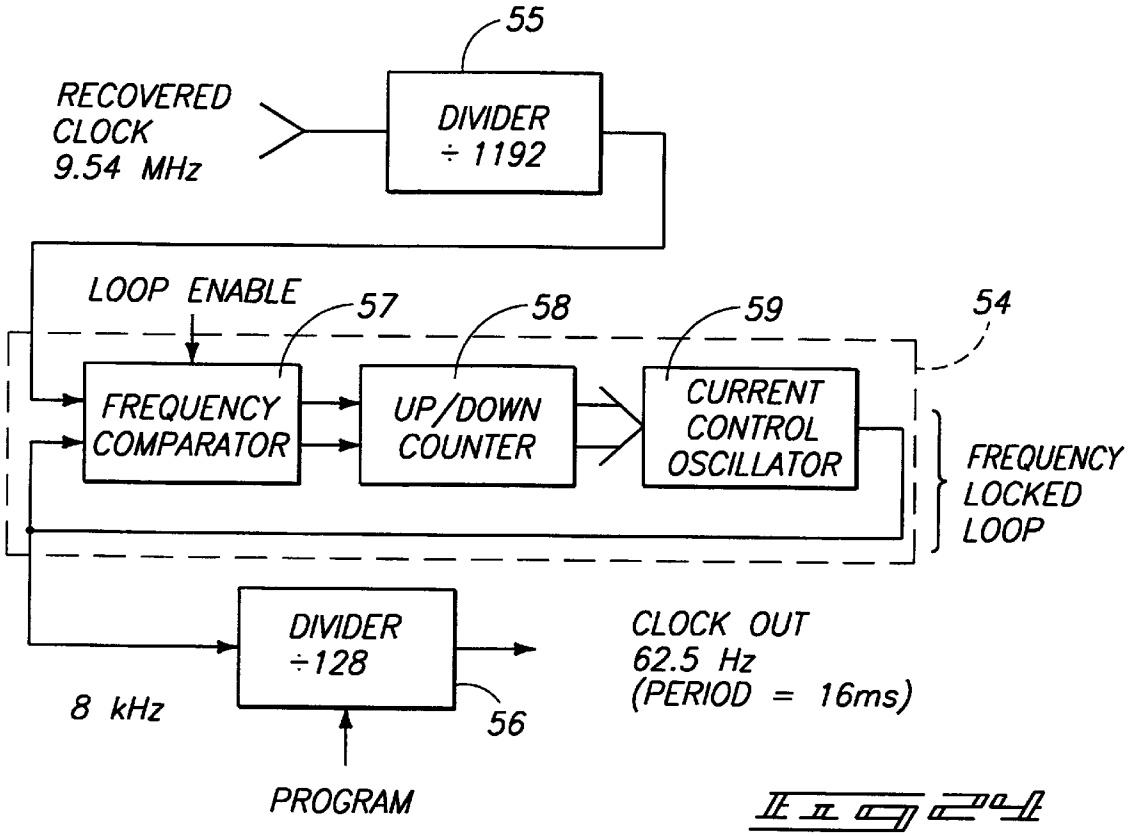


Fig 24

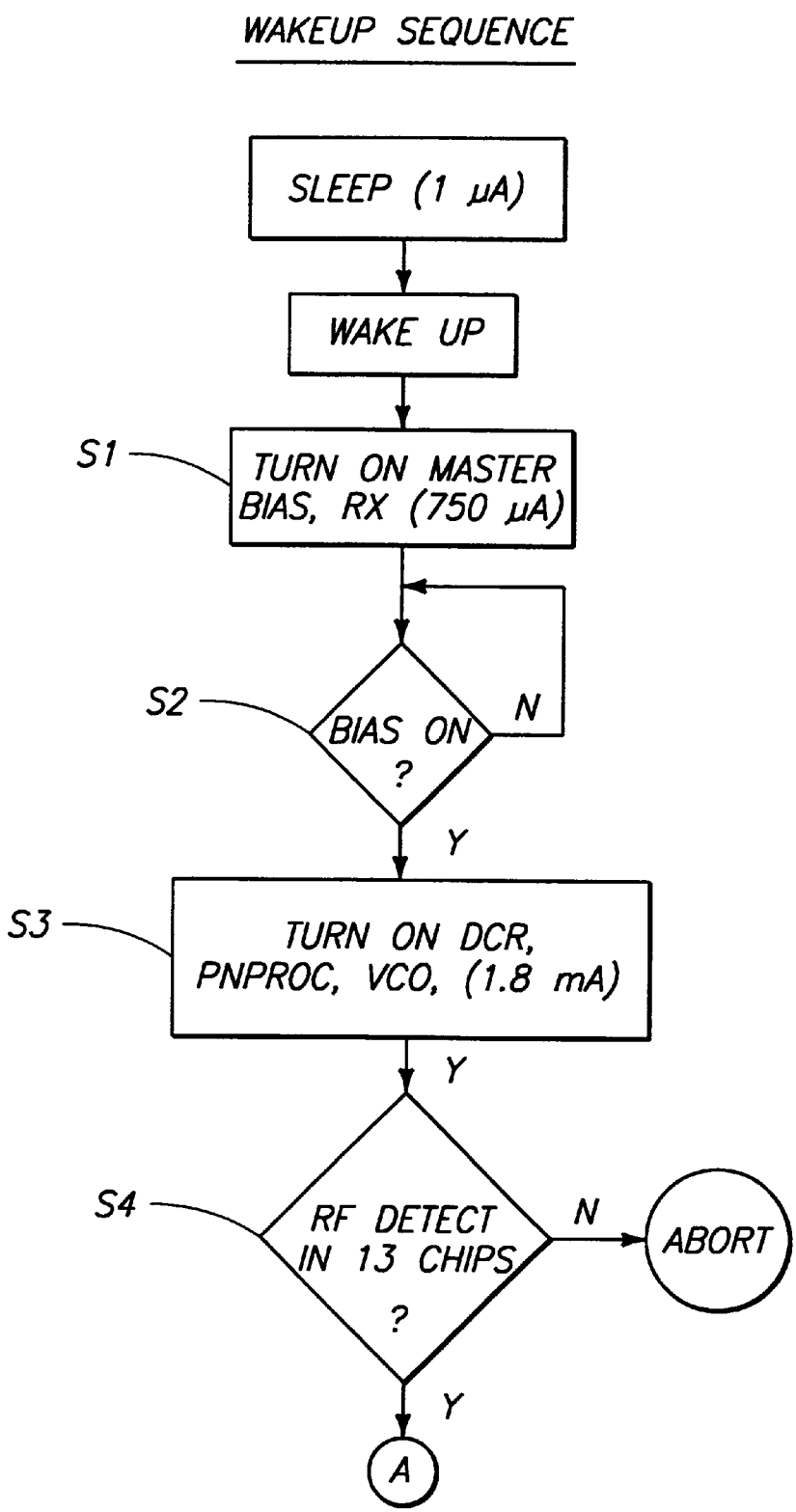

WAKEUP SEQUENCE
SLEEP (1 μA)
WAKE UP
S1
TURN ON MASTER BIAS, RX (750 μA)
S2
BIAS ON ?
N
Y
S3
TURN ON DCR, PNPROC, VCO, (1.8 mA)
Y
S4
RF DETECT IN 13 CHIPS ?
N
ABORT
Y
A

Fig 25

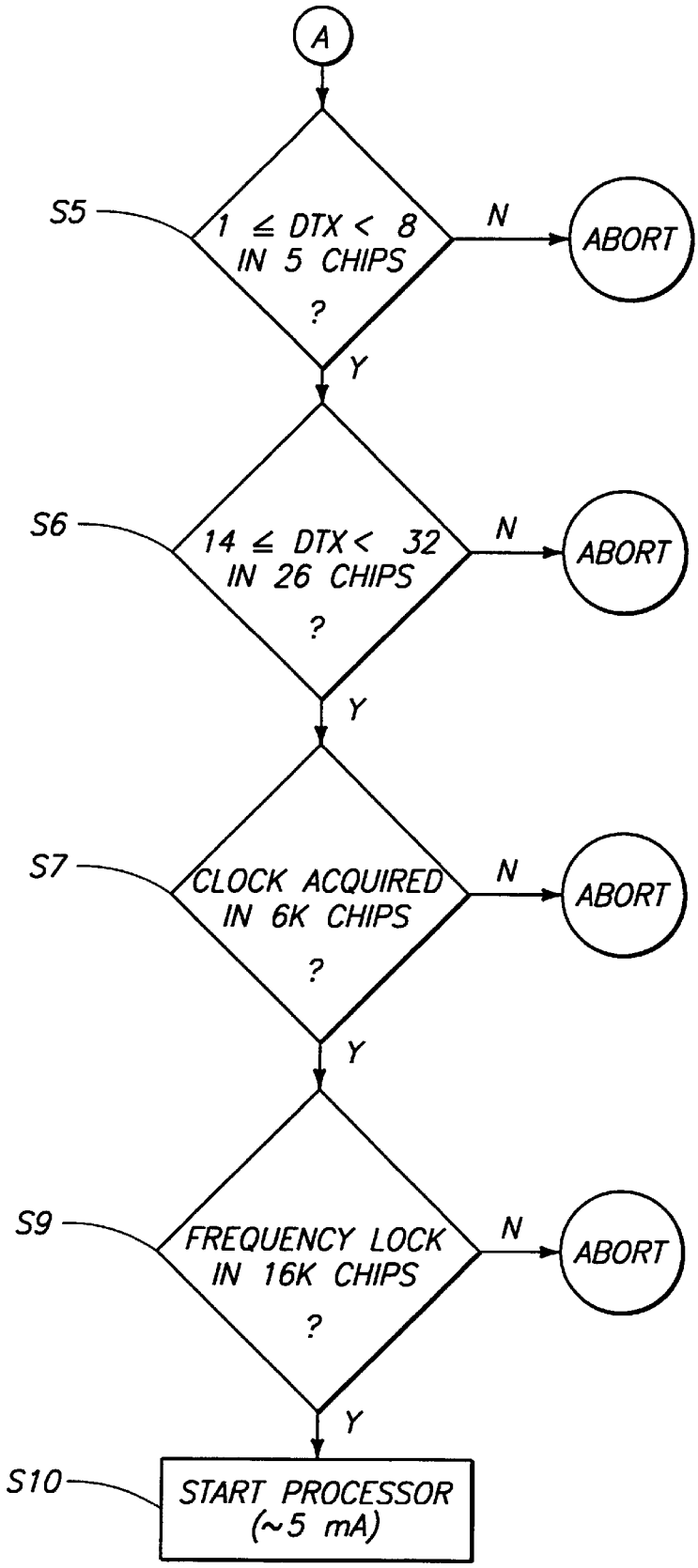
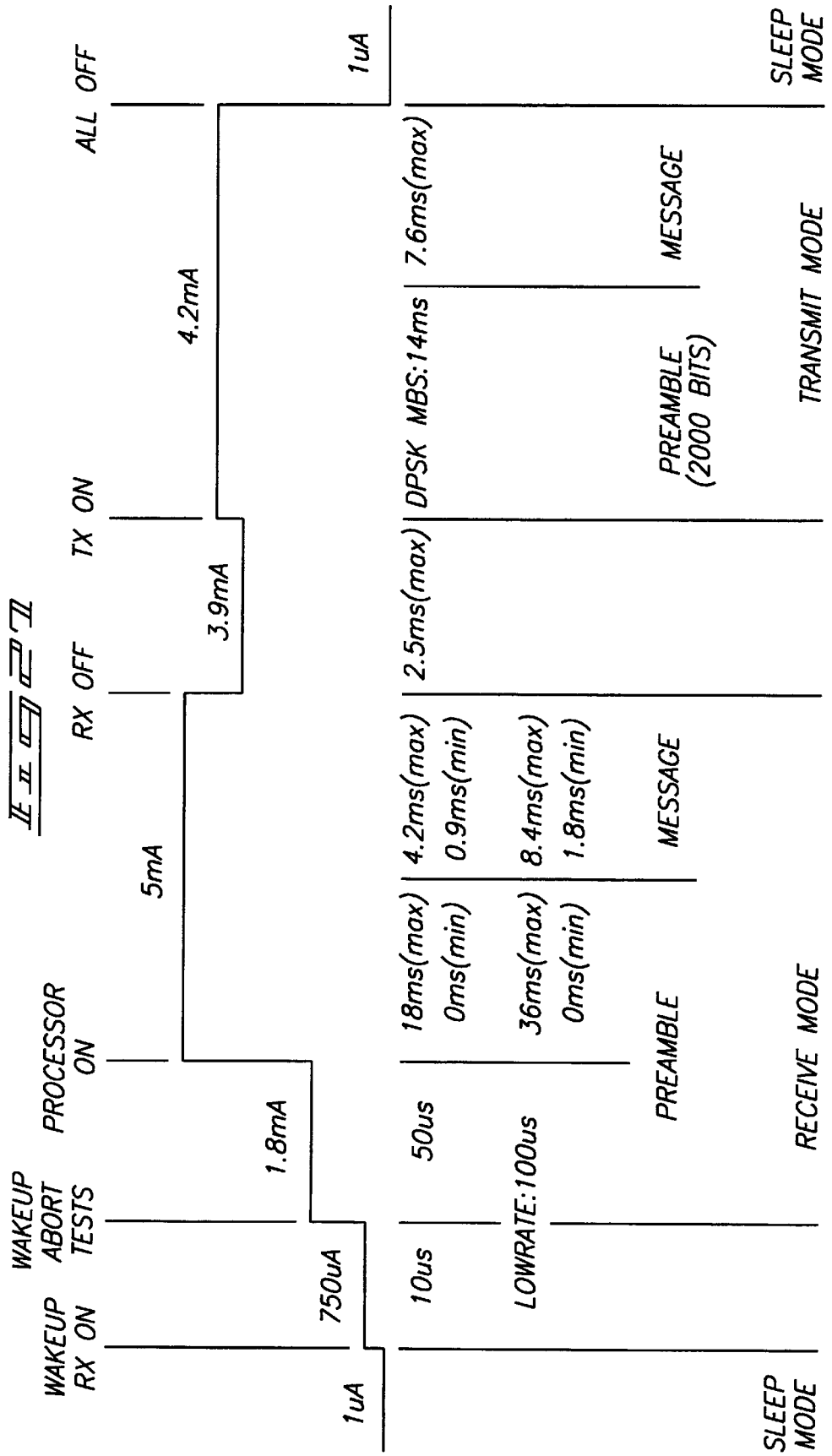

A
S5
1 ≤ DTX < 8
IN 5 CHIPS
?
N
ABORT
Y
S6
14 ≤ DTX < 32
IN 26 CHIPS
?
N
ABORT
Y
S7
CLOCK ACQUIRED
IN 6K CHIPS
?
N
ABORT
Y
S9
FREQUENCY LOCK
IN 16K CHIPS
?
N
ABORT
Y
S10
START PROCESSOR
(~5 mA)

FIG 26


WAKEUP RX ON
WAKEUP ABORT TESTS
PROCESSOR ON
RX OFF
TX ON
ALL OFF
1uA
750uA
1.8mA
5mA
3.9mA
4.2mA
1uA
10us
50us
18ms(max)
0ms(min)
4.2ms(max)
0.9ms(min)
2.5ms(max)
DPSK MBS:14ms
7.6ms(max)
LOWRATE:100us
36ms(max)
0ms(min)
8.4ms(max)
1.8ms(min)
PREAMBLE
MESSAGE
PREAMBLE (2000 BITS)
MESSAGE
SLEEP MODE
RECEIVE MODE
TRANSMIT MODE
SLEEP MODE

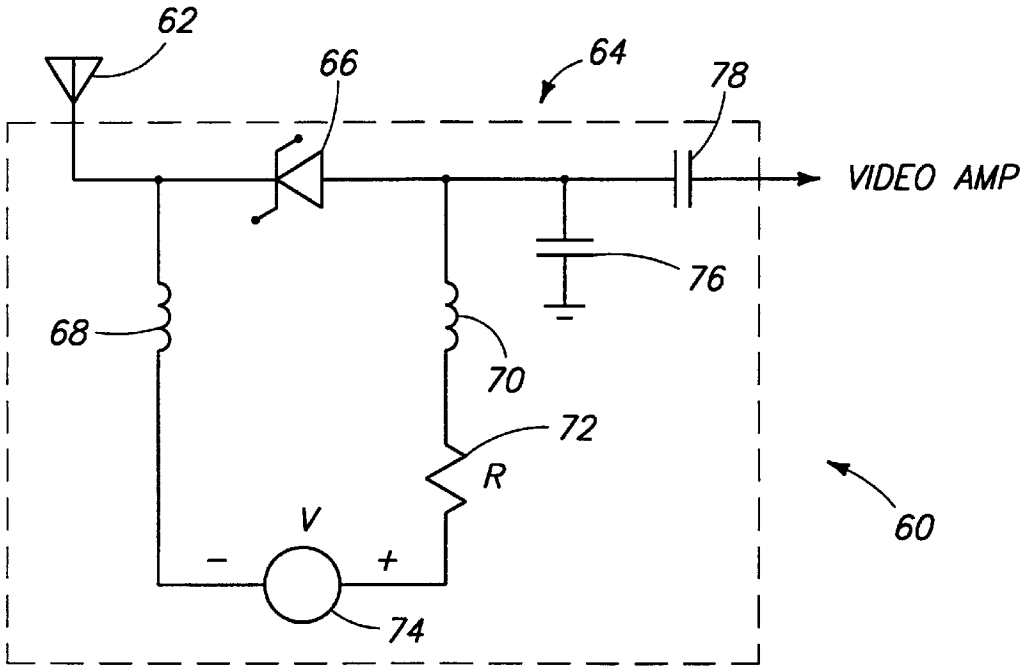


Fig 28B

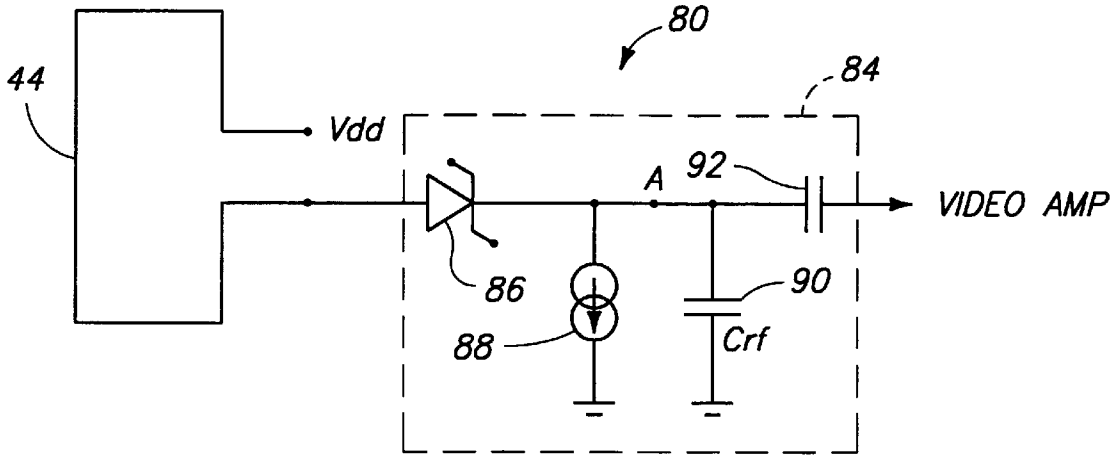


Fig 29

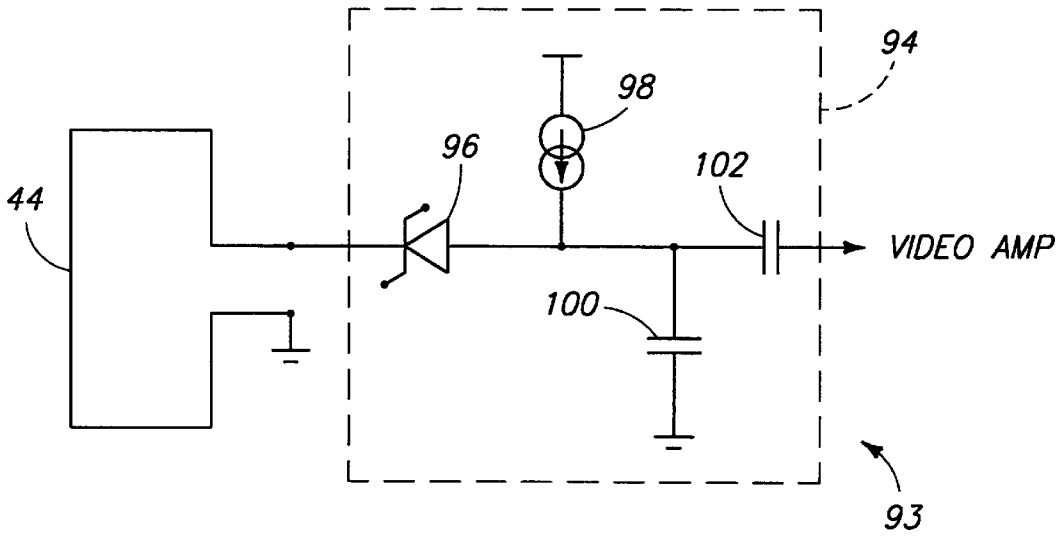

94
98
96
102
44
VIDEO AMP
100
93

Fig 30

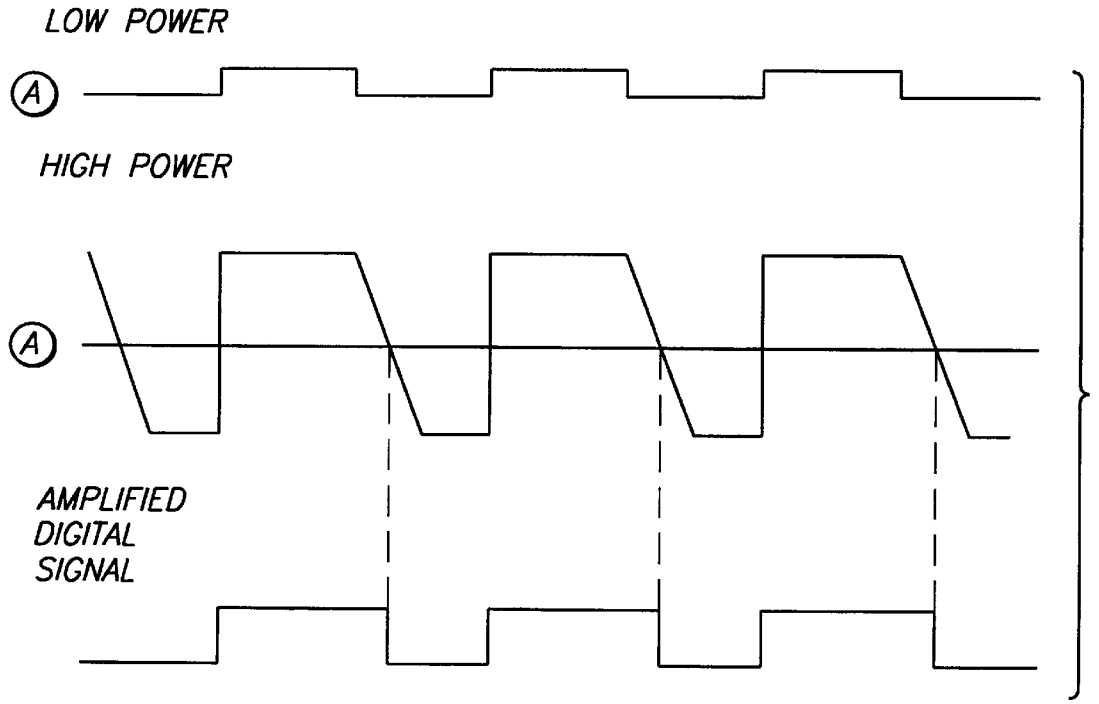

LOW POWER
A
HIGH POWER
A
AMPLIFIED
DIGITAL
SIGNAL

Fig 31

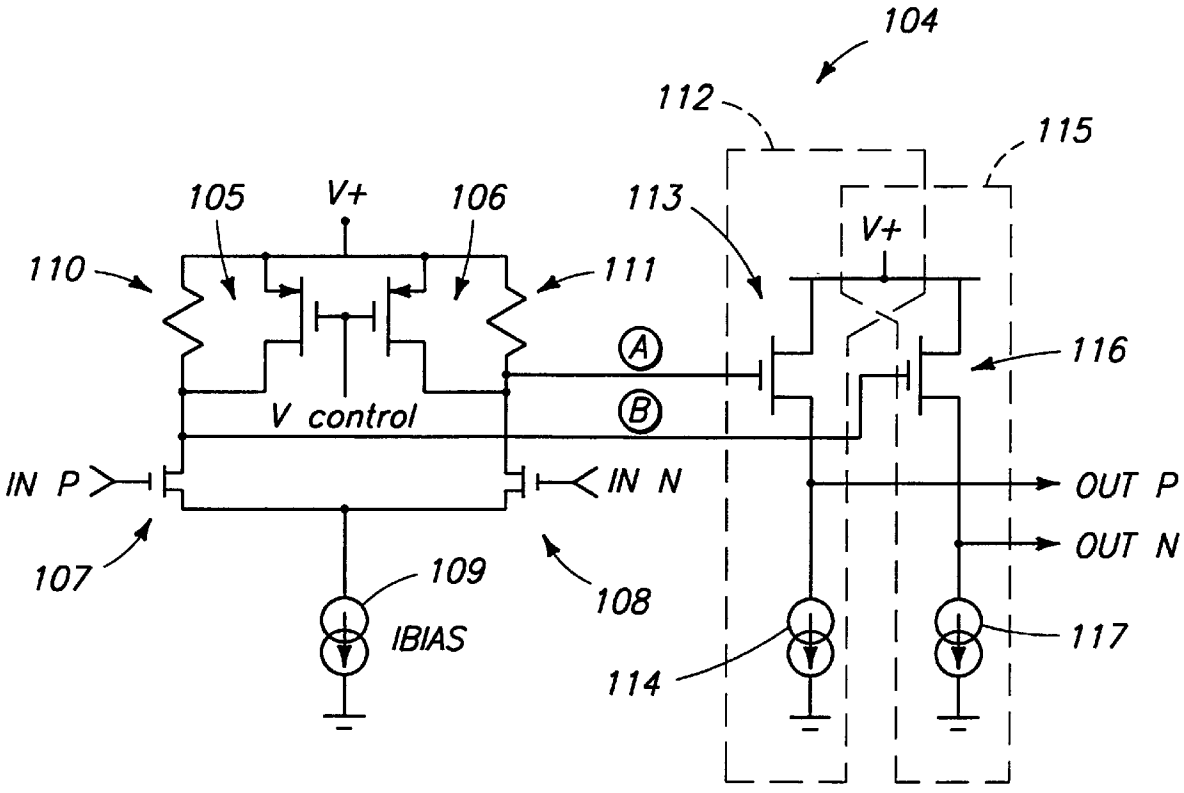

104
112
115
105
V+
106
113
V+
110
111
116
A
B
V control
IN P
IN N
OUT P
OUT N
107
109
108
IBIAS
114
117

Fig 32

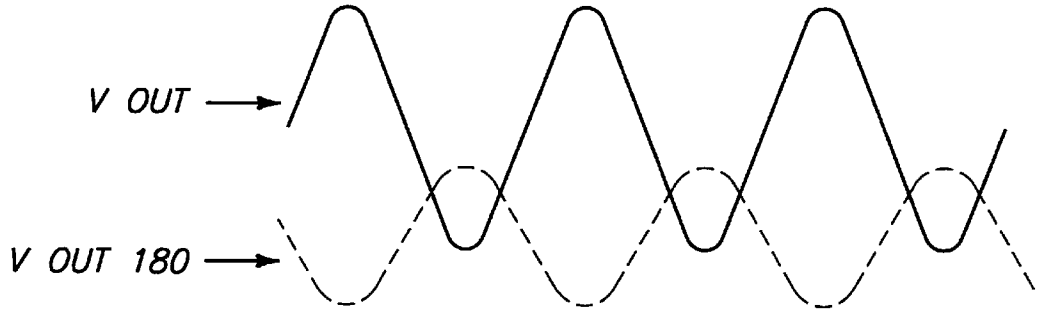

V OUT
V OUT 180

Fig 33

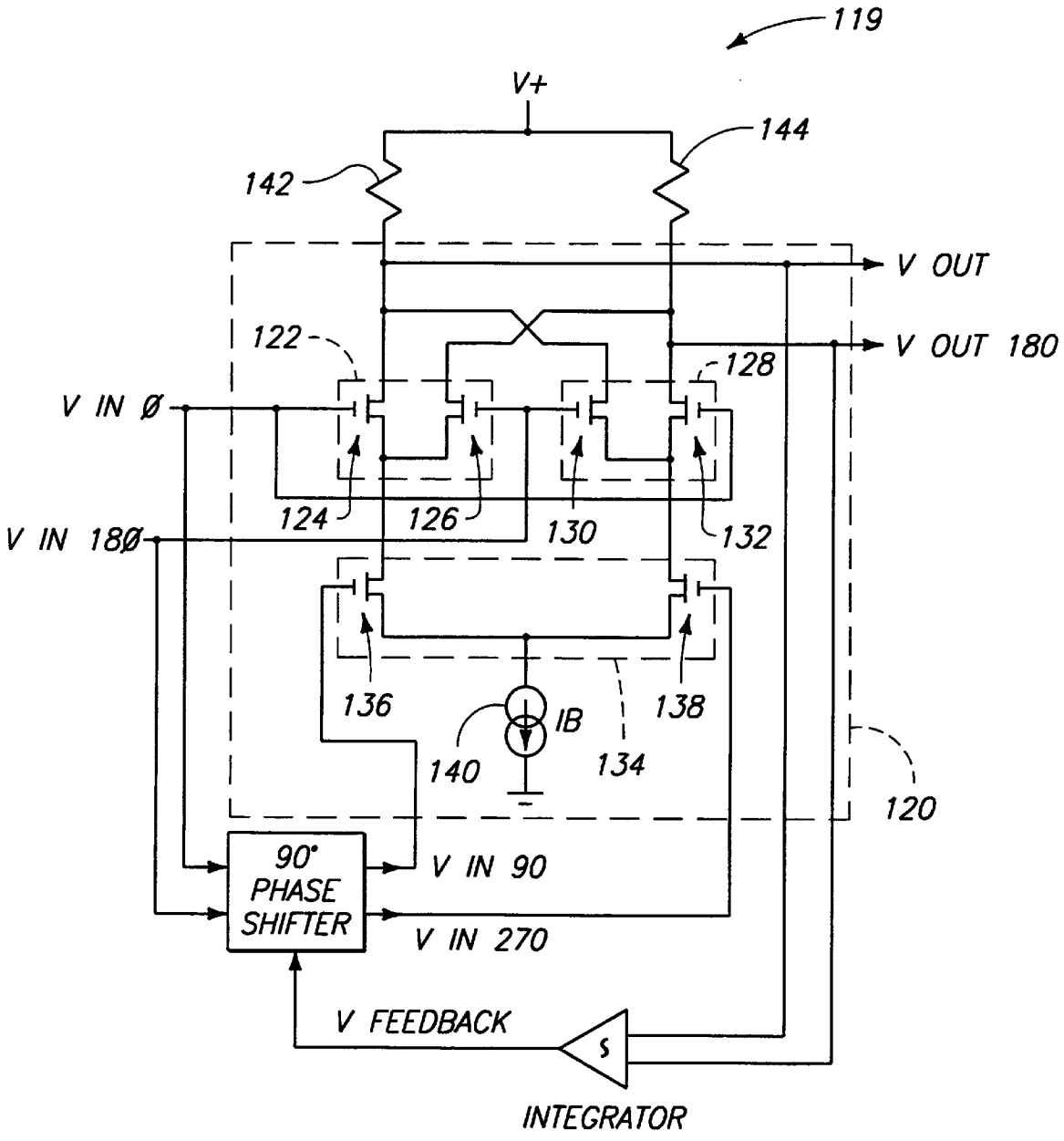

119
V+
144
142
V OUT
V OUT 180
122
128
V IN Ø
124
126
130
132
V IN 18Ø
136
IB
138
140
134
120
90°
PHASE
SHIFTER
V IN 90
V IN 270
V FEEDBACK
S
INTEGRATOR

Fig 34

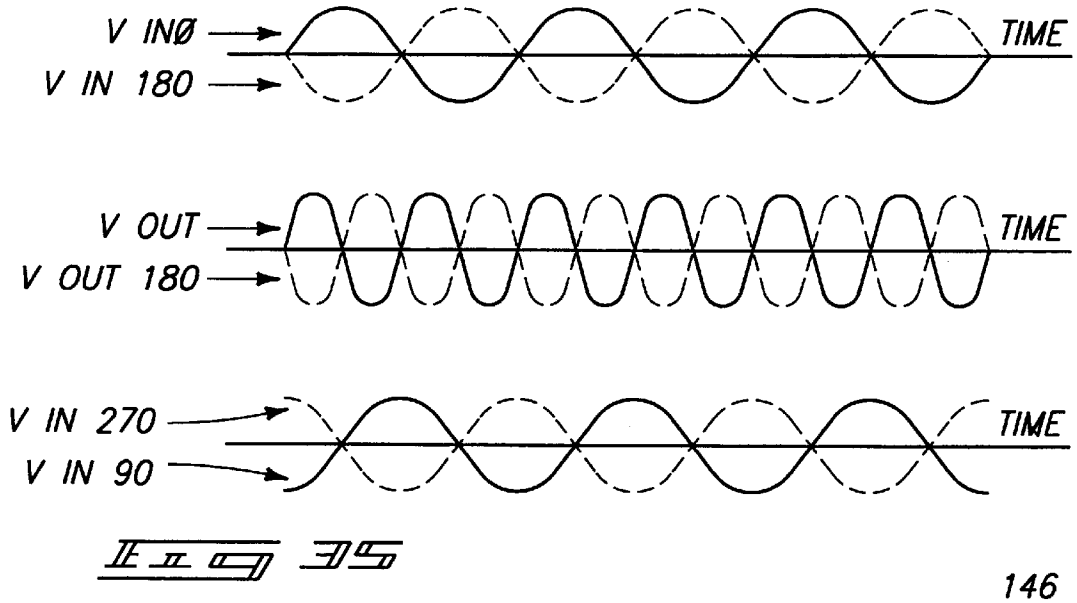

V INØ
V IN 180
TIME
V OUT
V OUT 180
TIME
V IN 270
V IN 90
TIME

Fig 35

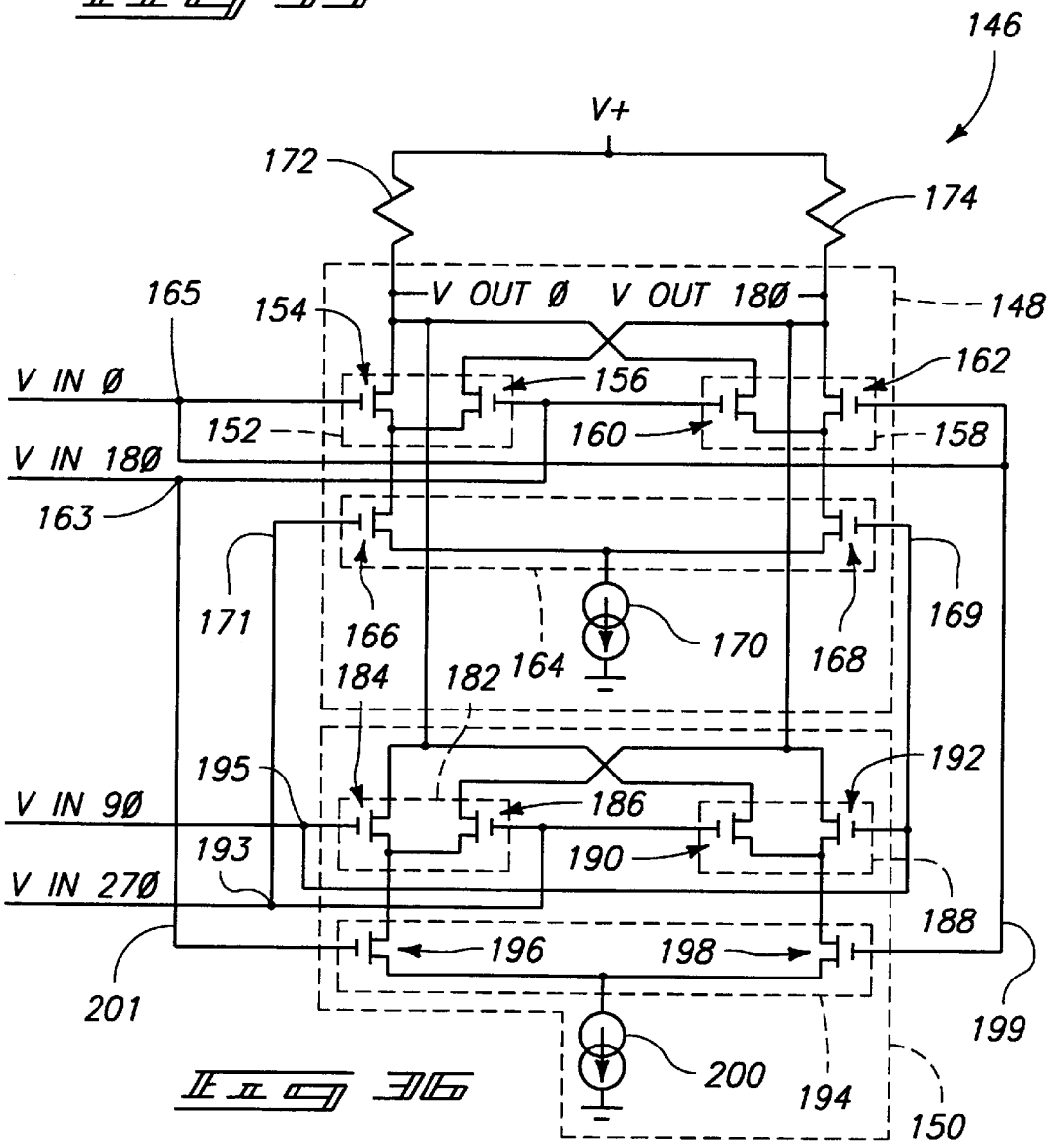

146
V+
172
174
165
154
V OUT Ø
V OUT 180Ø
148
V IN Ø
156
162
152
160
158
V IN 180Ø
163
171
166
184
182
164
170
168
169
195
192
V IN 9Ø
186
193
190
V IN 27Ø
188
196
198
201
199
200
194
150

Fig 36

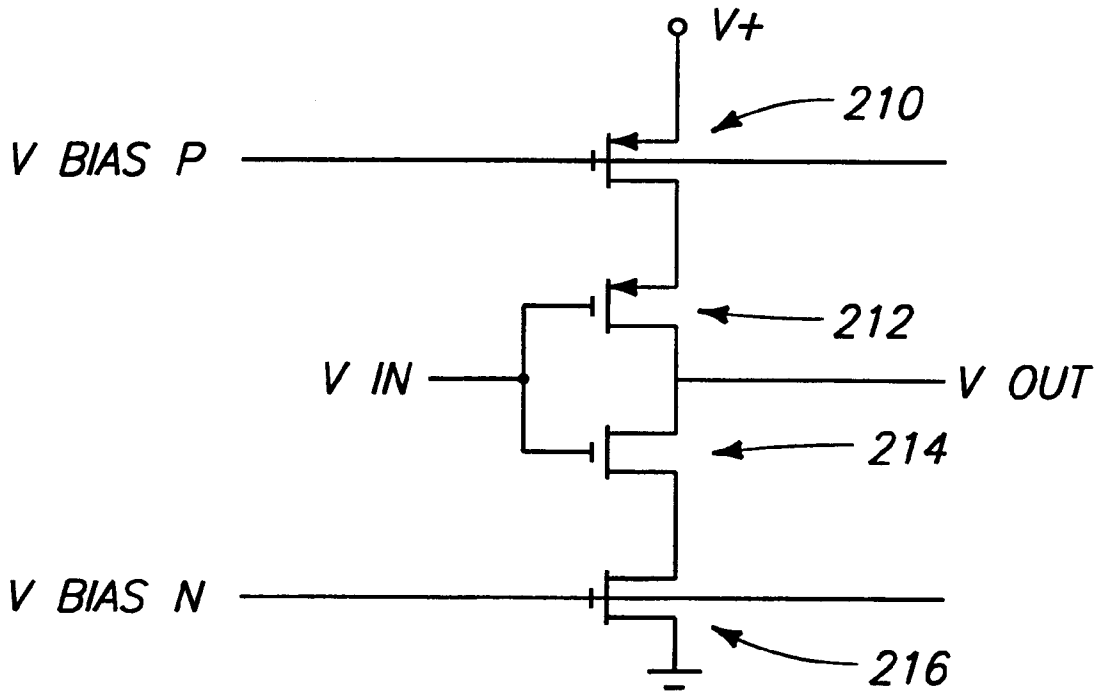


Fig 37

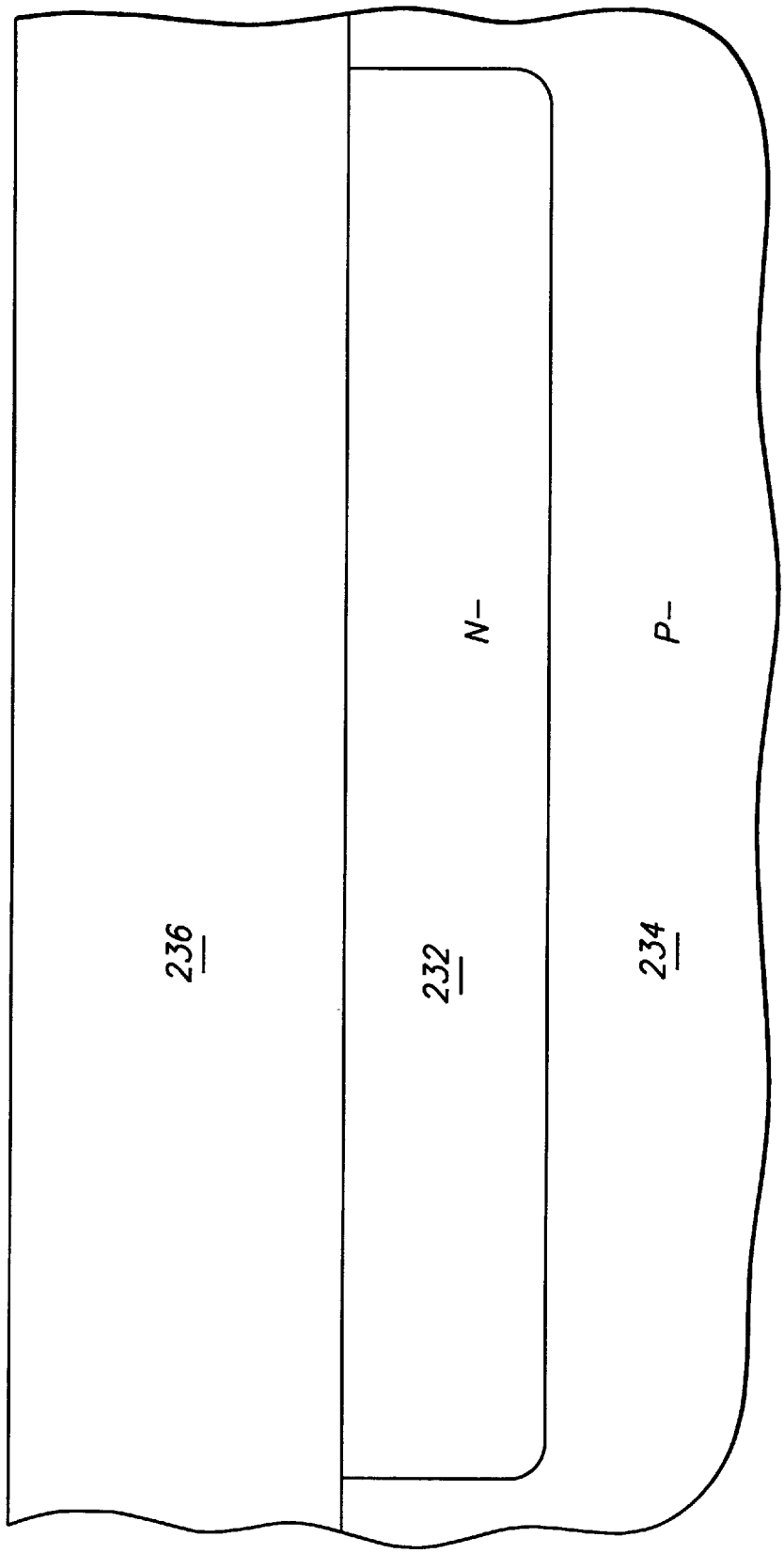


FIG 3BB

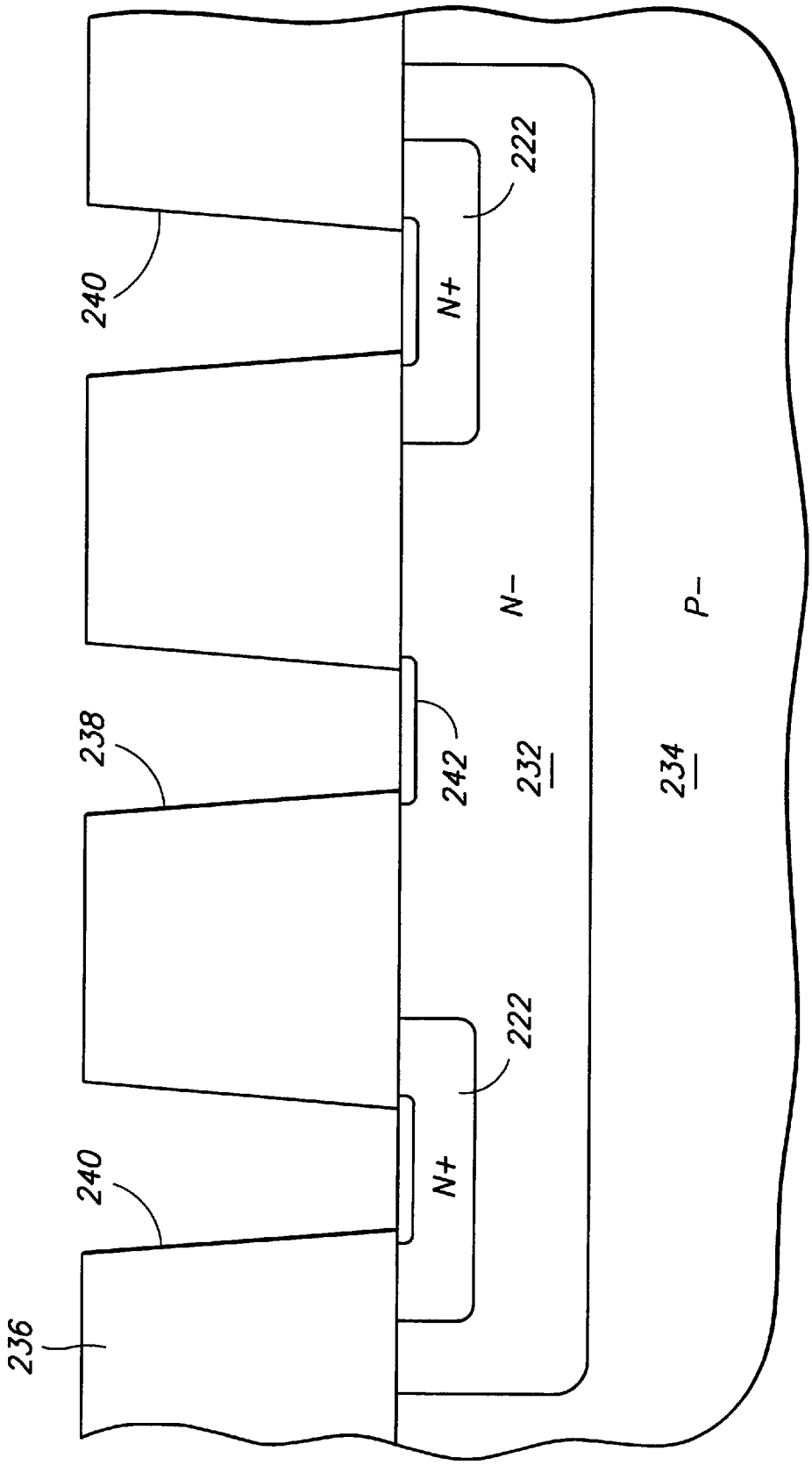


FIG 3E

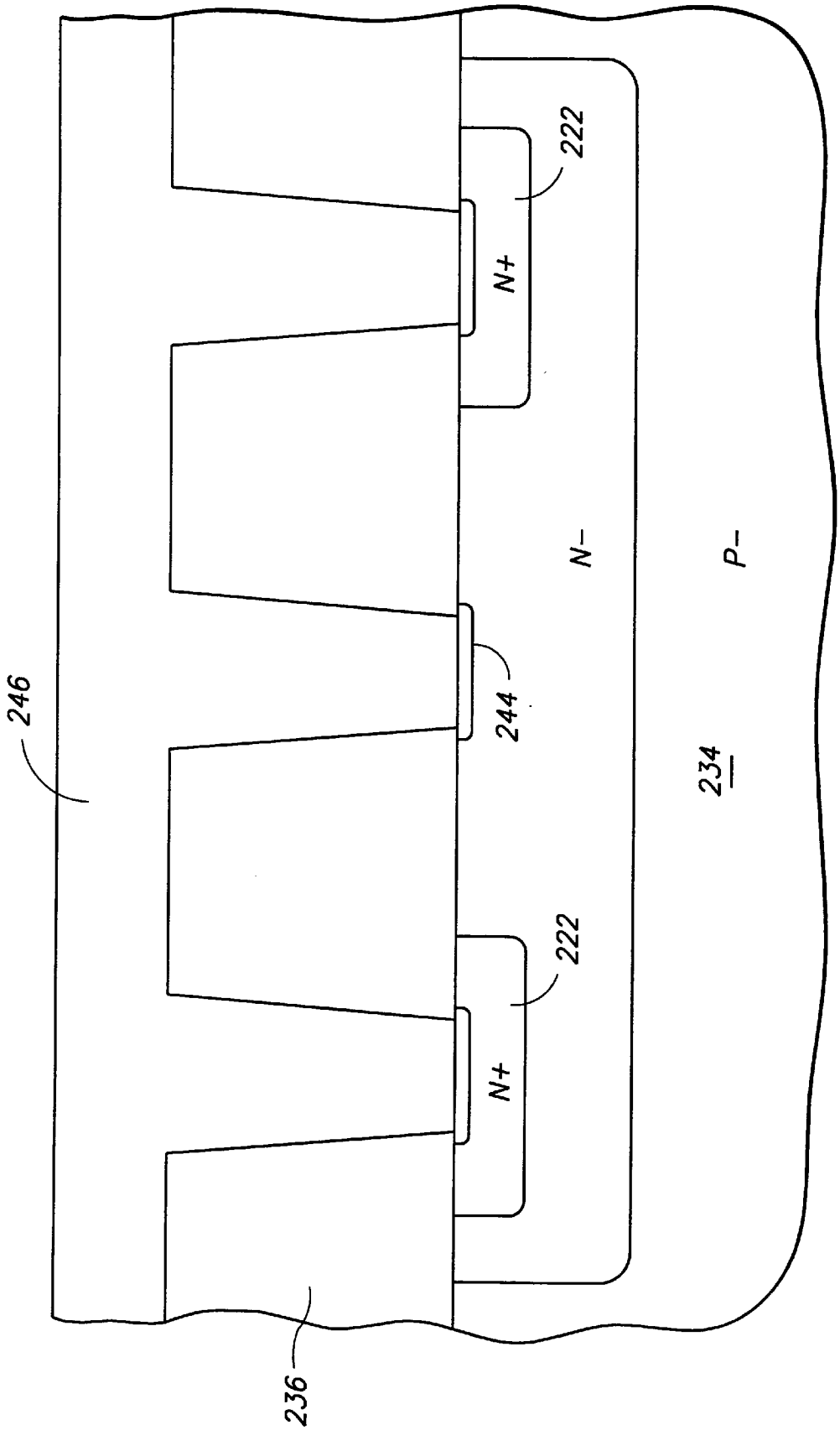


FIG 3II

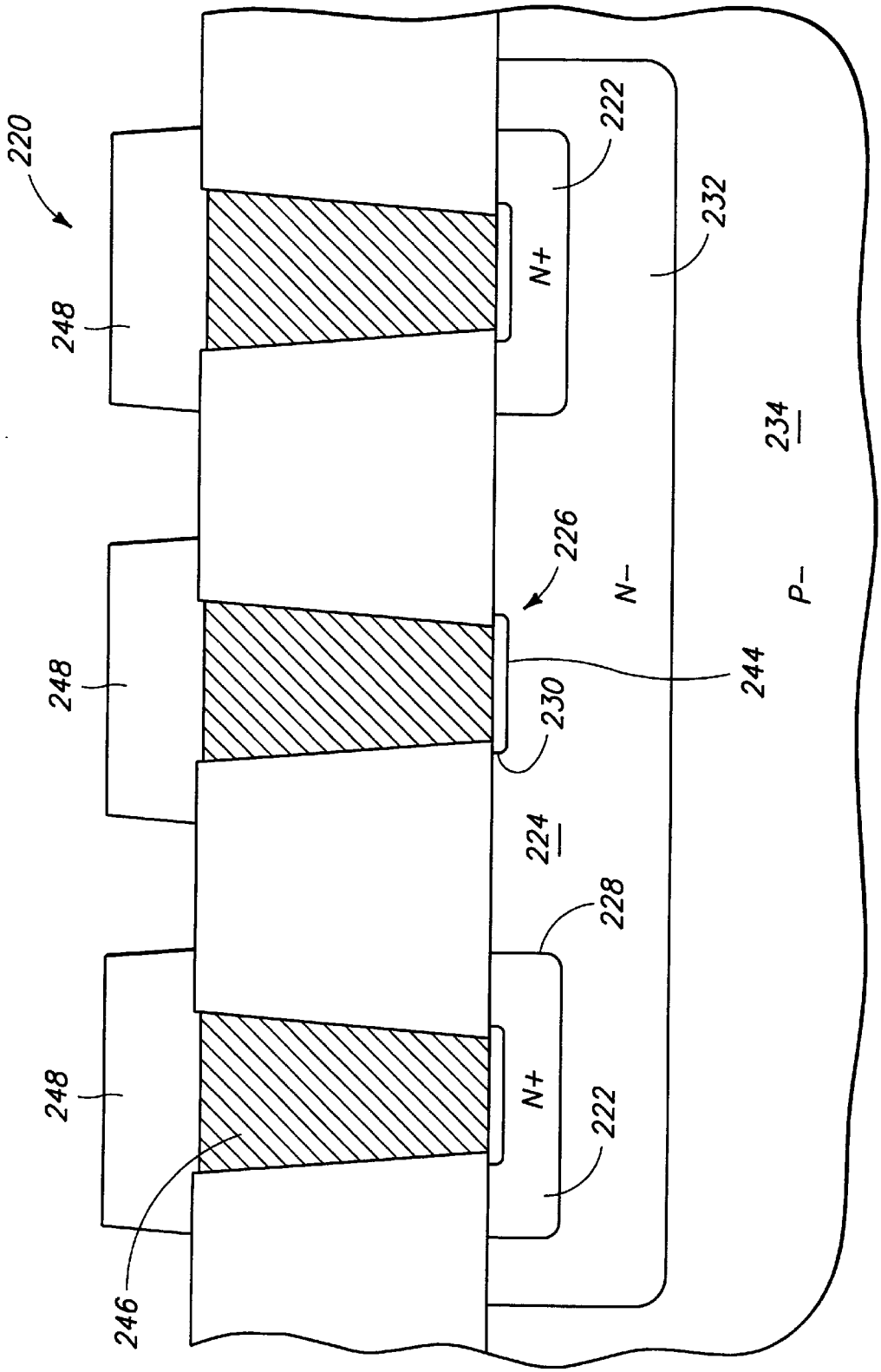


FIG 11

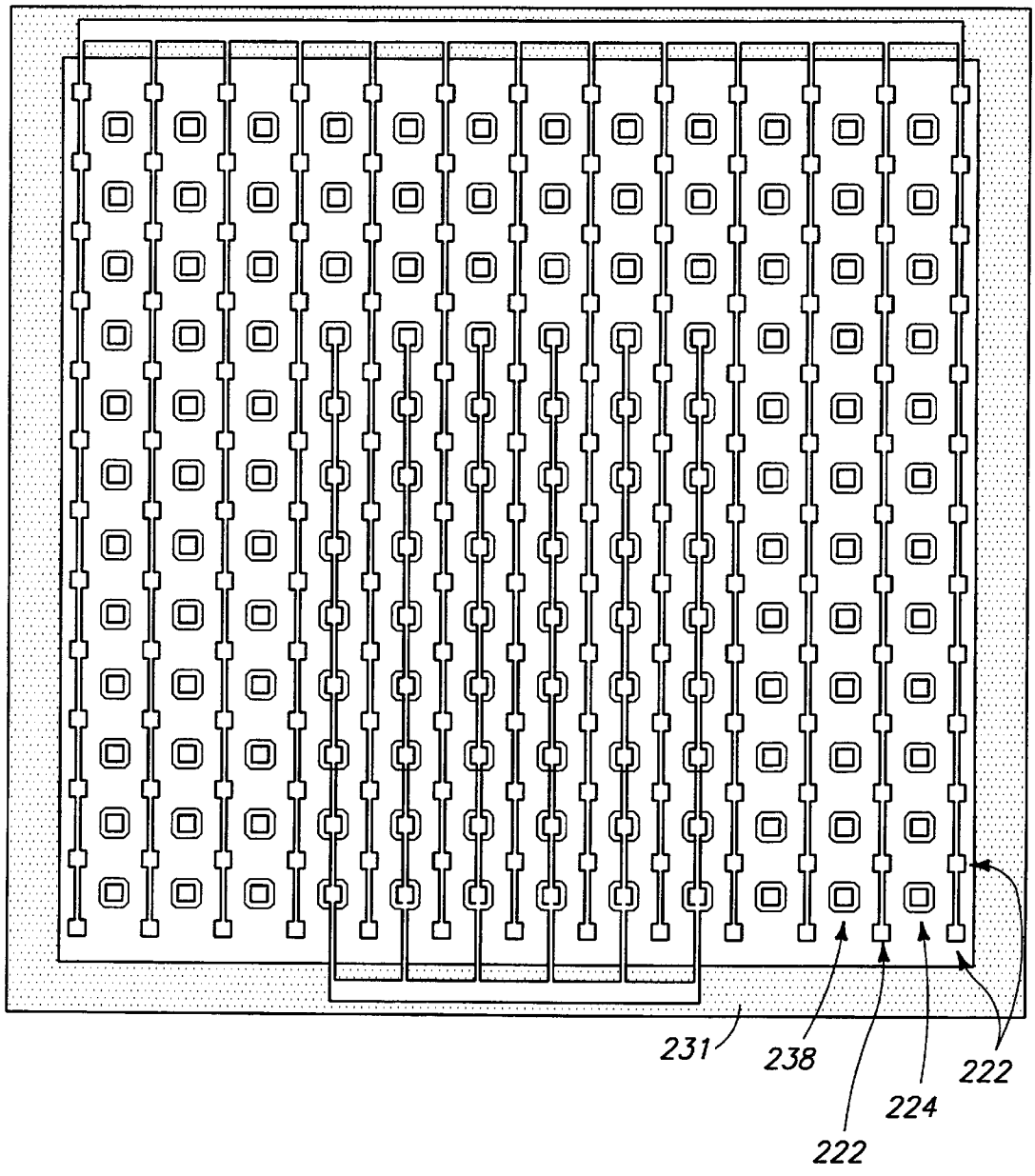


Fig 42

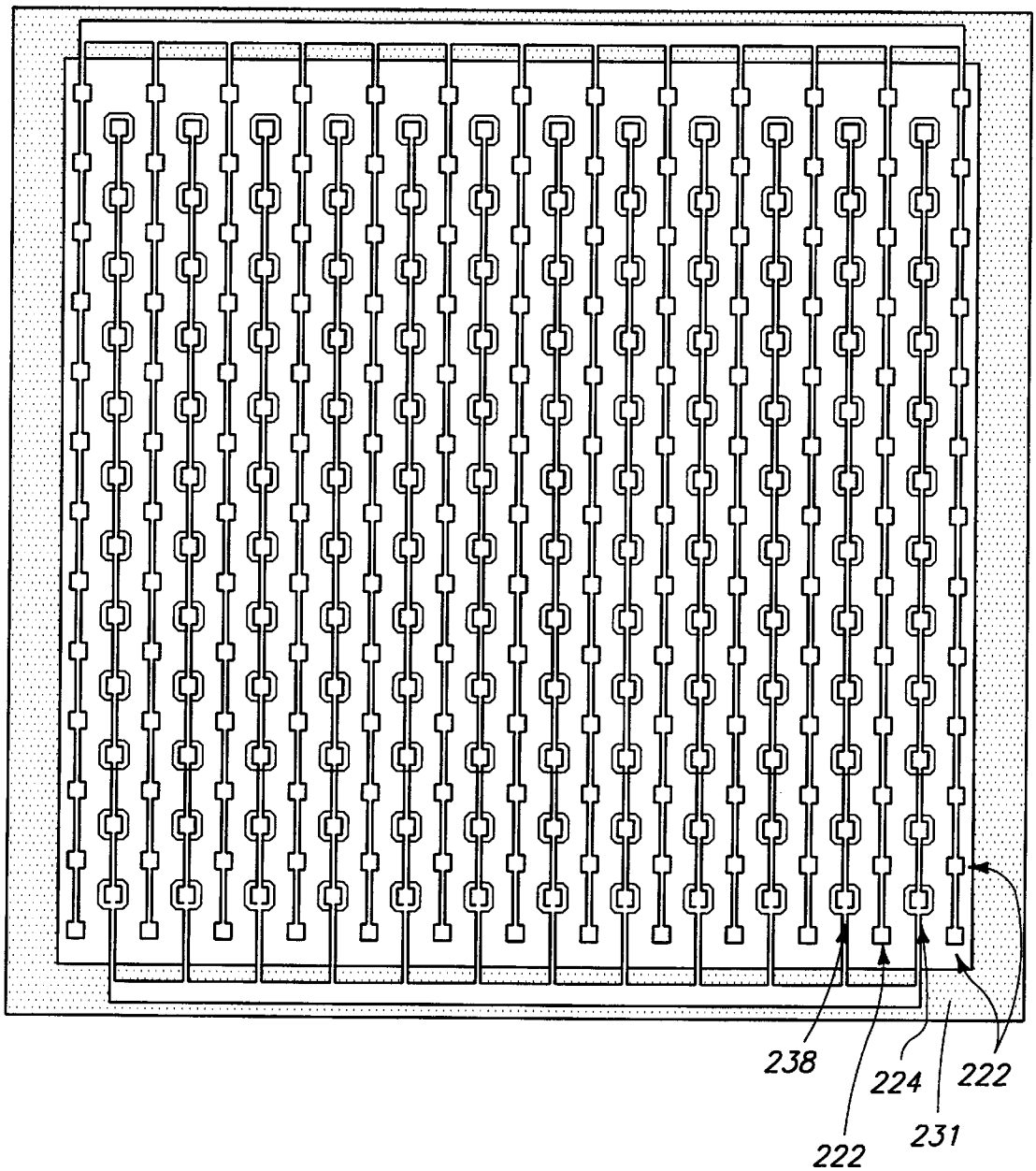


Fig 43

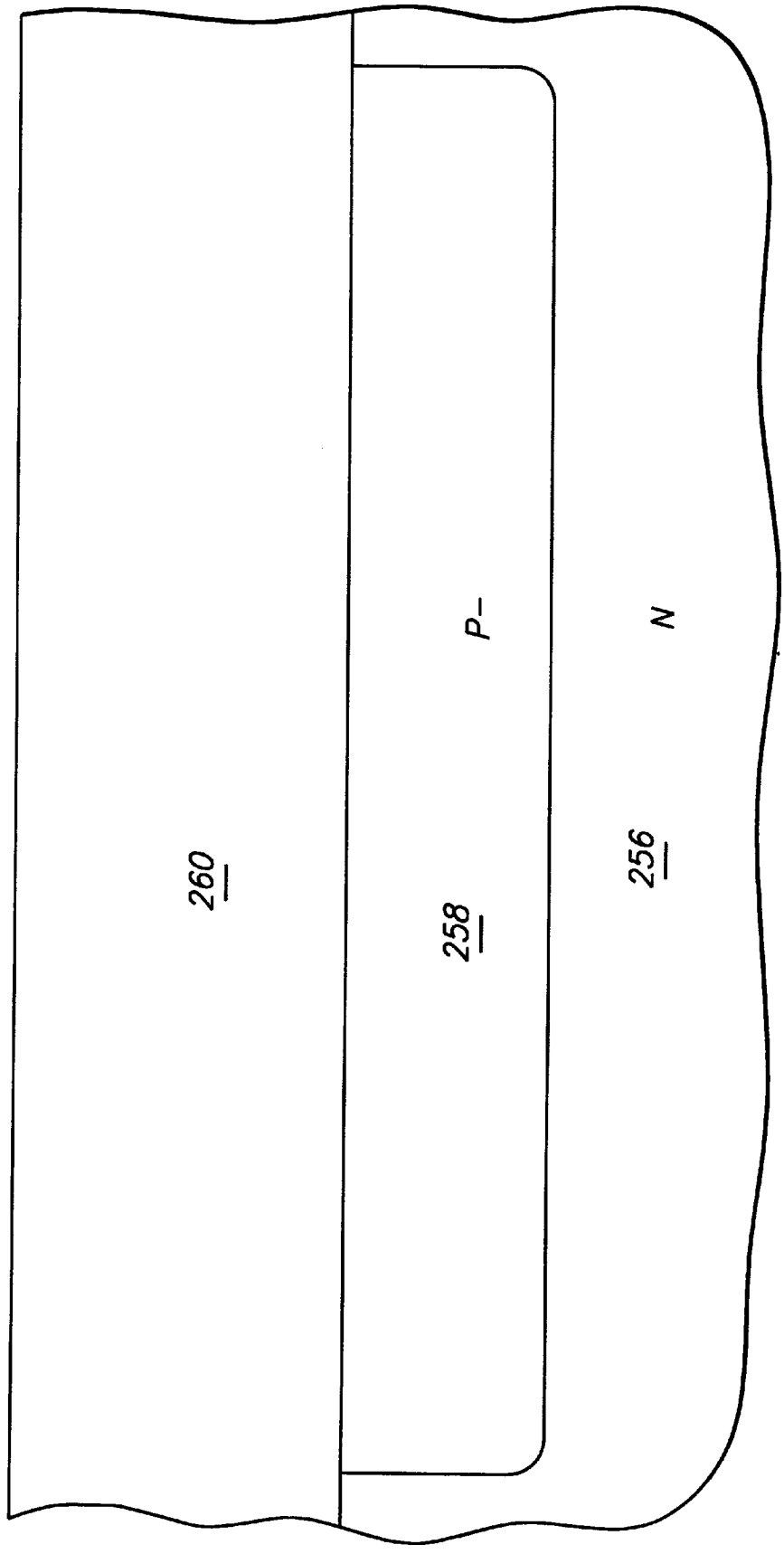


Fig. 5II

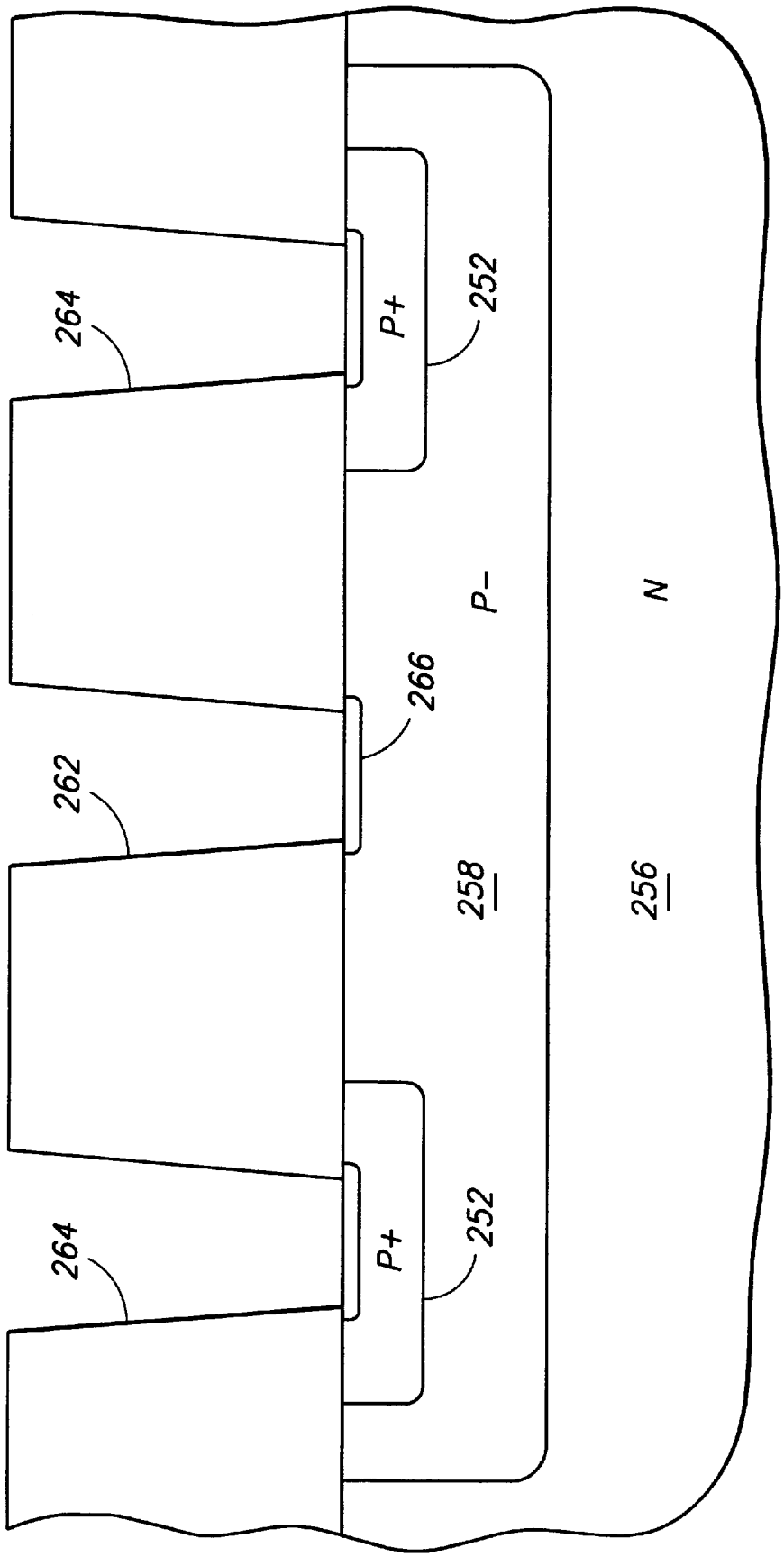


FIG 45

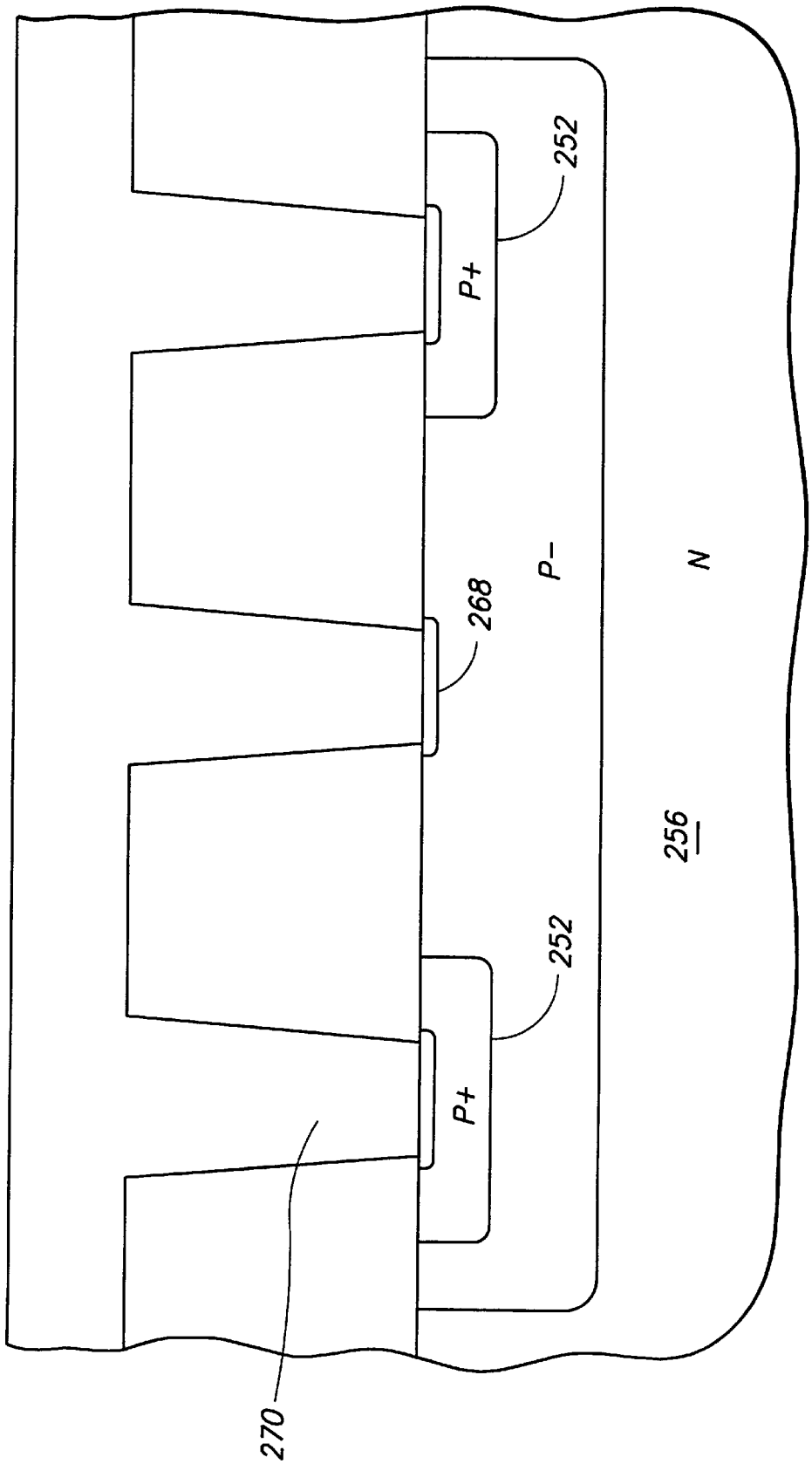


FIG 53F

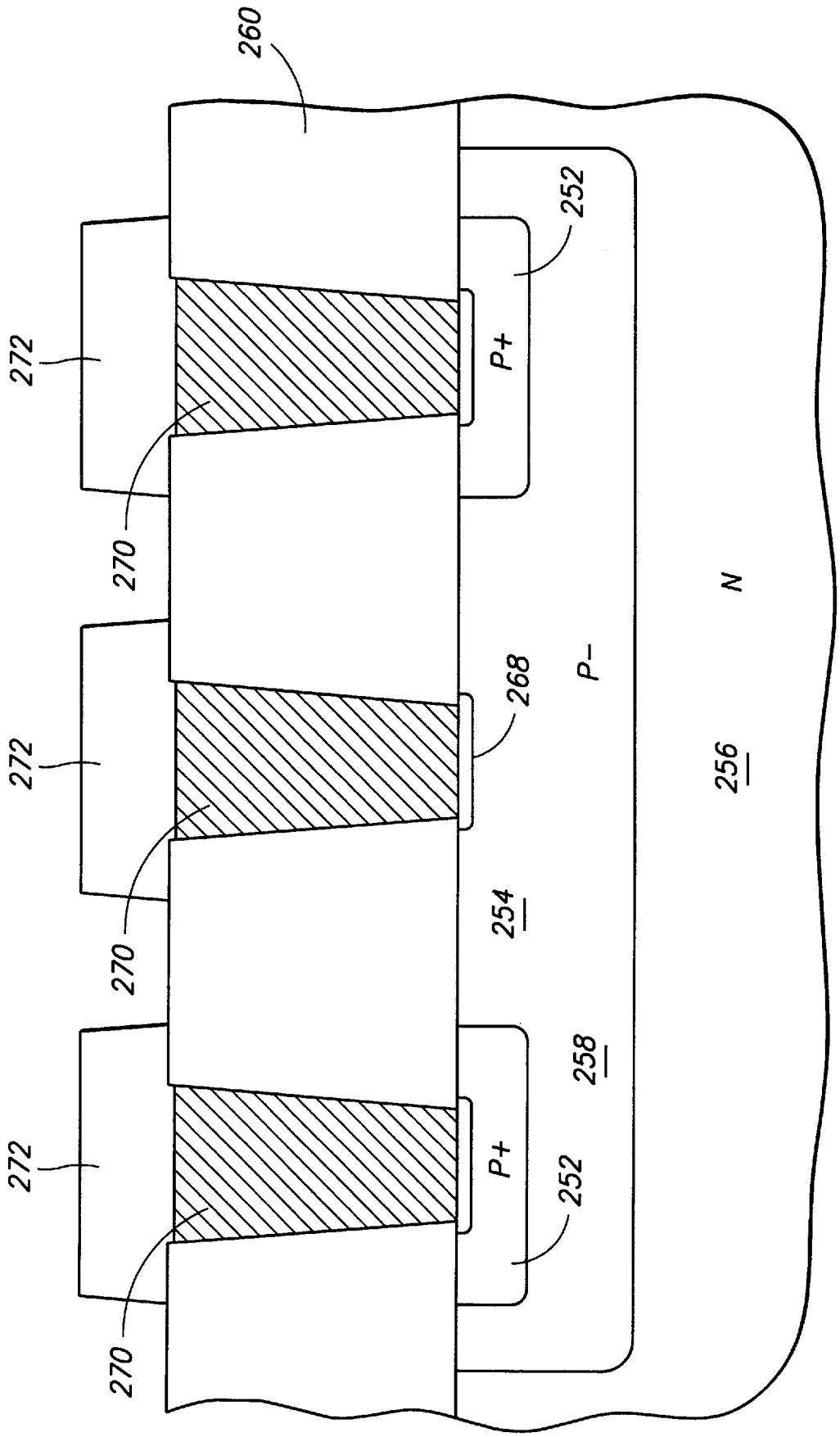


FIG 11

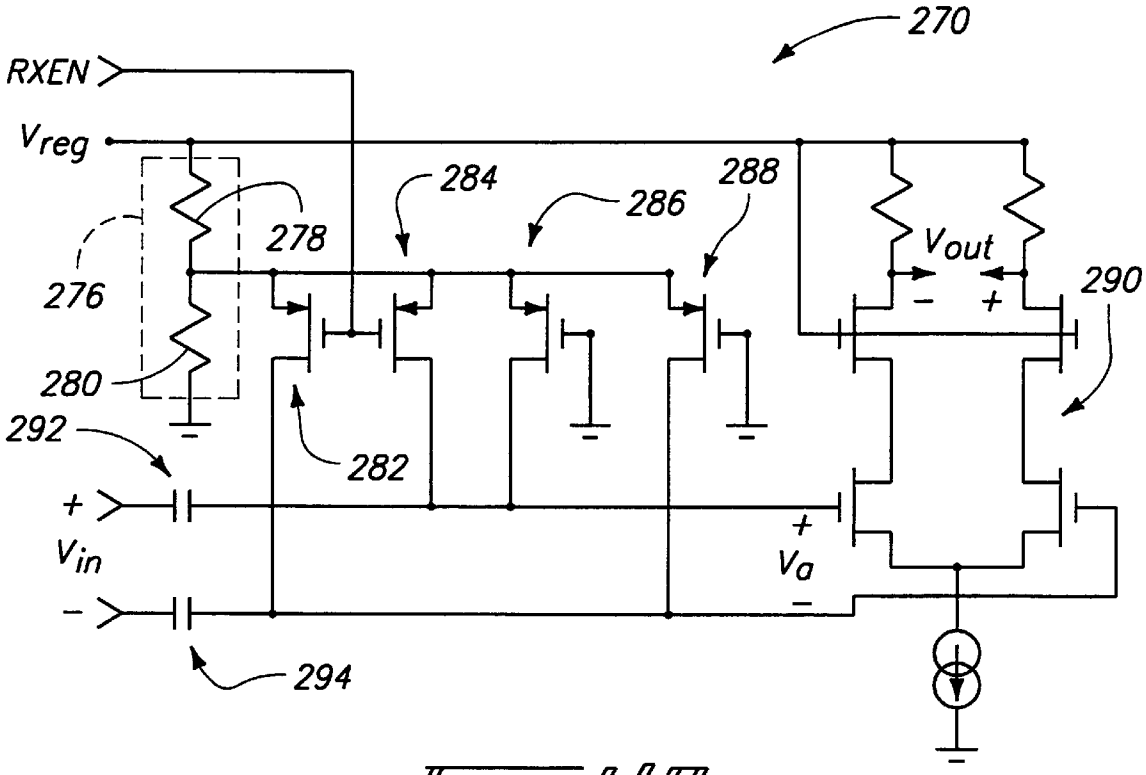


Fig 48B

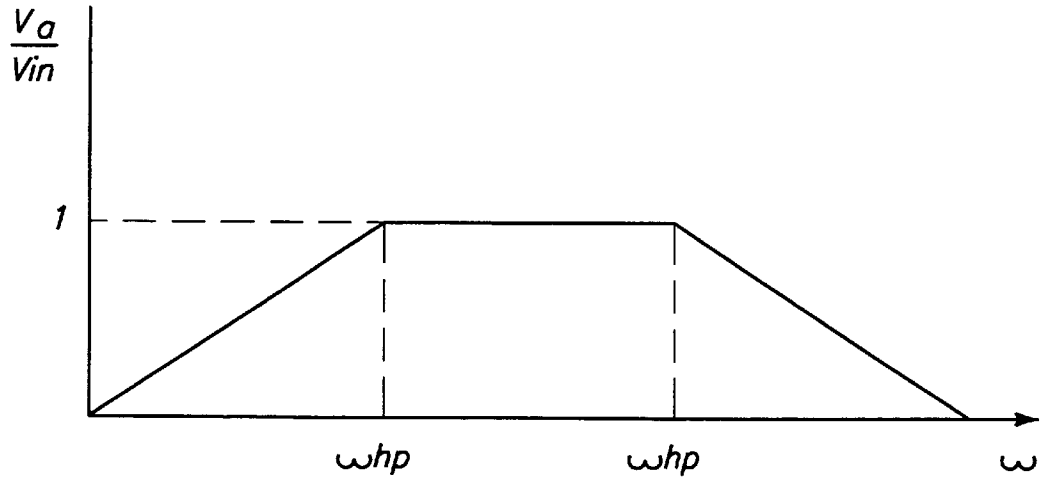


Fig 49

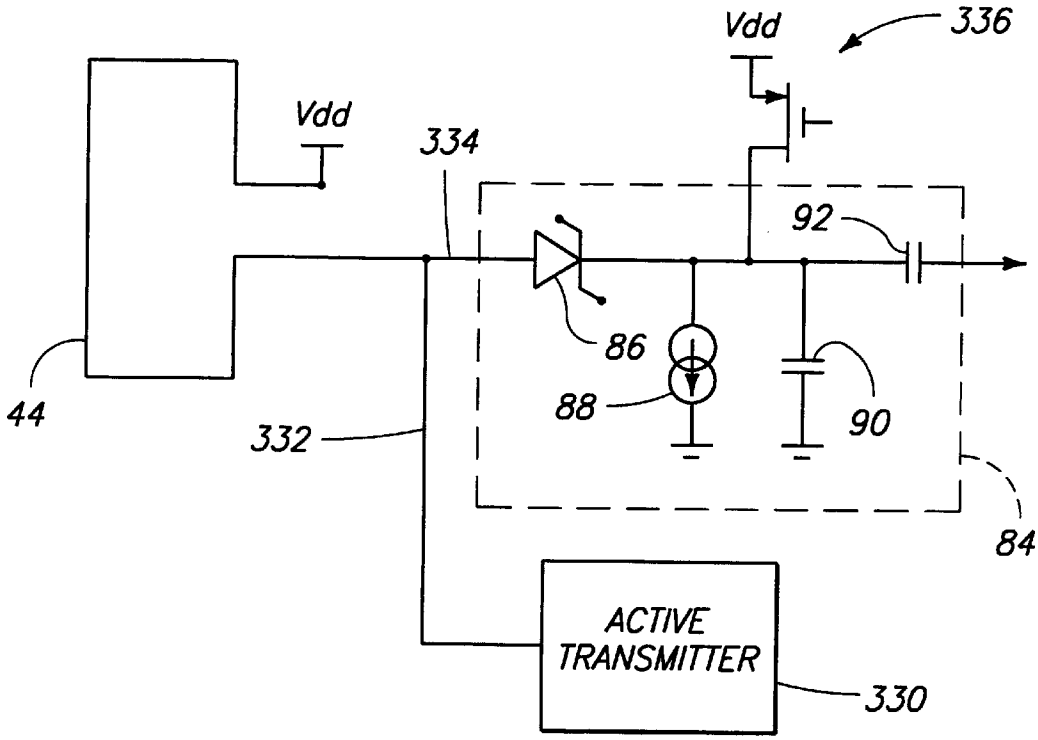

Vdd
336
Vdd
334
92
86
88
90
44
332
84
ACTIVE TRANSMITTER
330

FIG 50

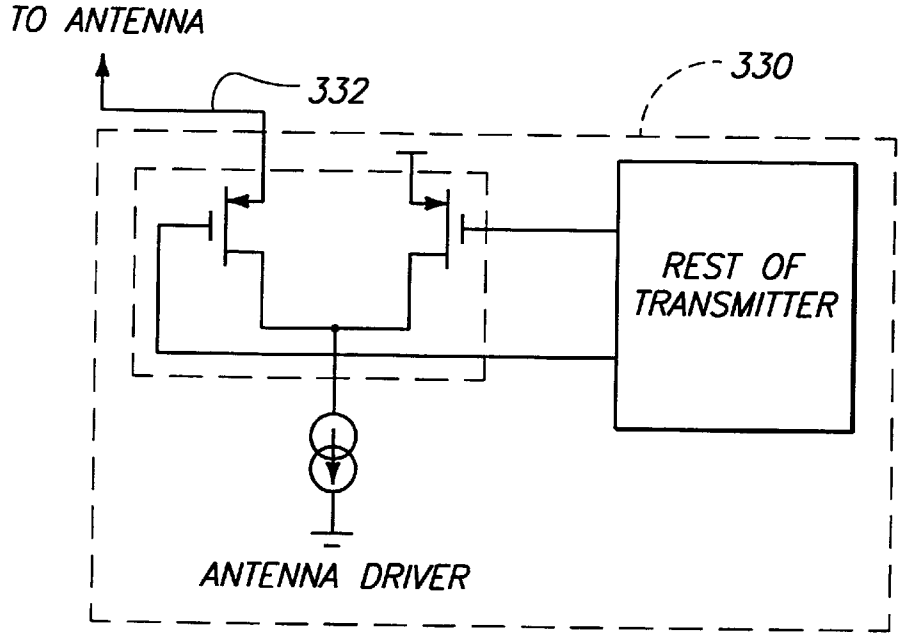

TO ANTENNA
332
330
REST OF TRANSMITTER
ANTENNA DRIVER

FIG 51

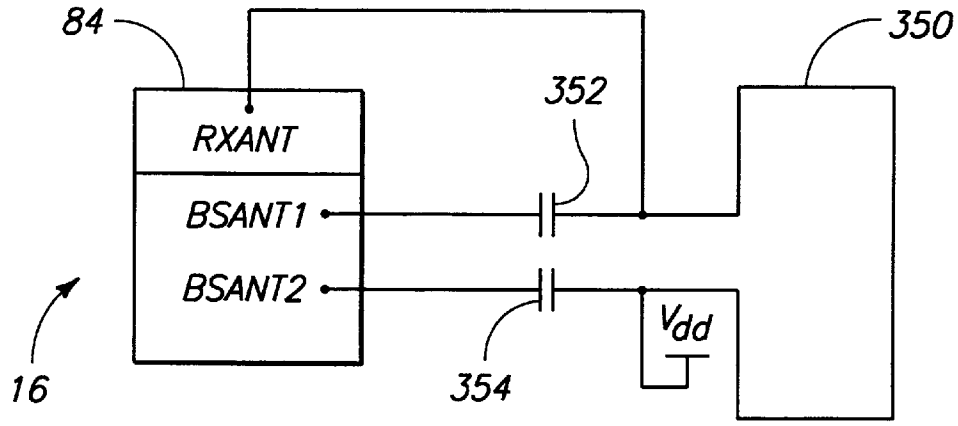

84
350
352
RXANT
BSANT1
BSANT2
16
354
Vdd

Fig 52

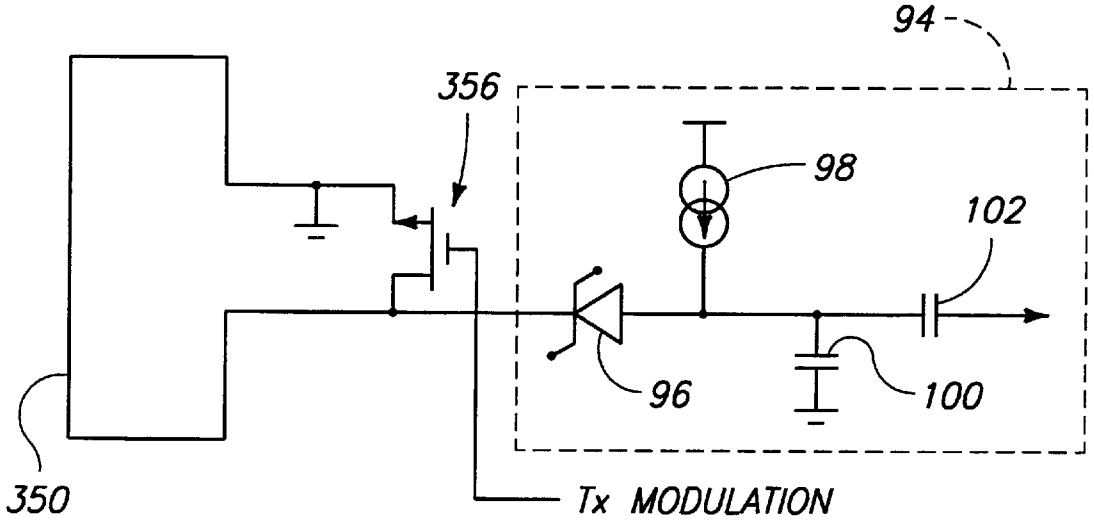

94
356
98
102
96
100
350
Tx MODULATION

Fig 53

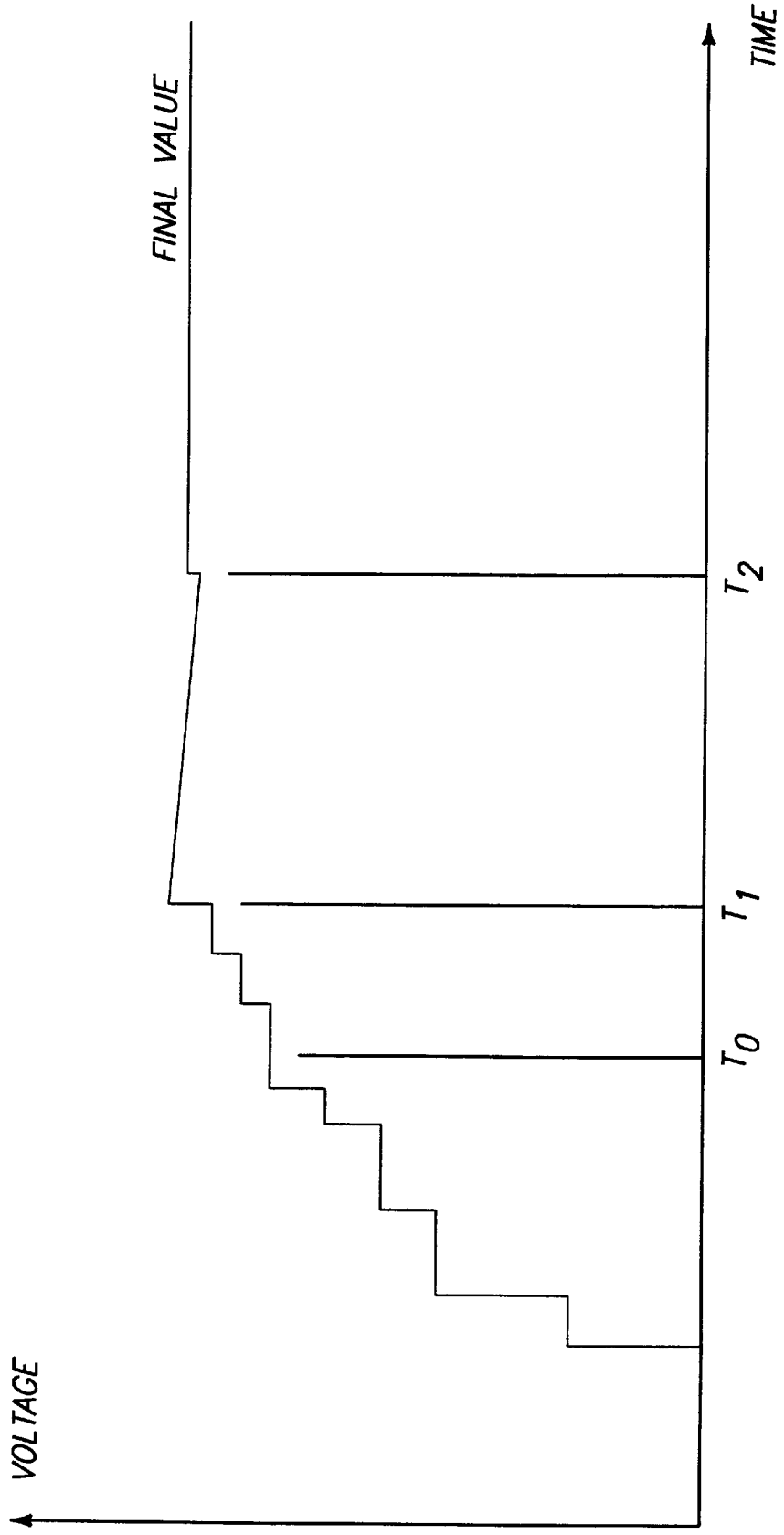


FIG 3F

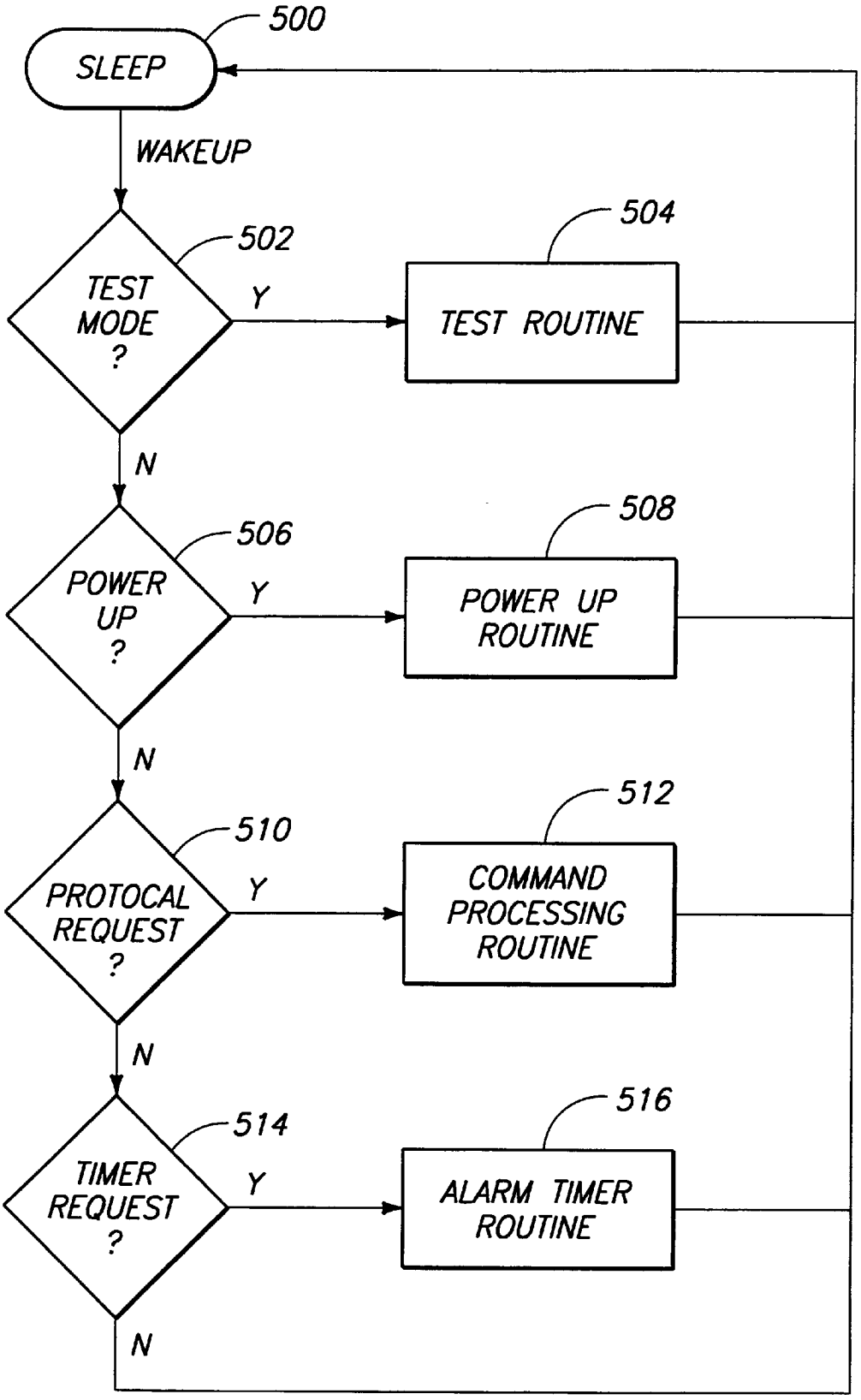

500
SLEEP
WAKEUP
502
TEST MODE ?
Y
504
TEST ROUTINE
N
506
POWER UP ?
Y
508
POWER UP ROUTINE
N
510
PROTOCAL REQUEST ?
Y
512
COMMAND PROCESSING ROUTINE
N
514
TIMER REQUEST ?
Y
516
ALARM TIMER ROUTINE
N

Fig 55

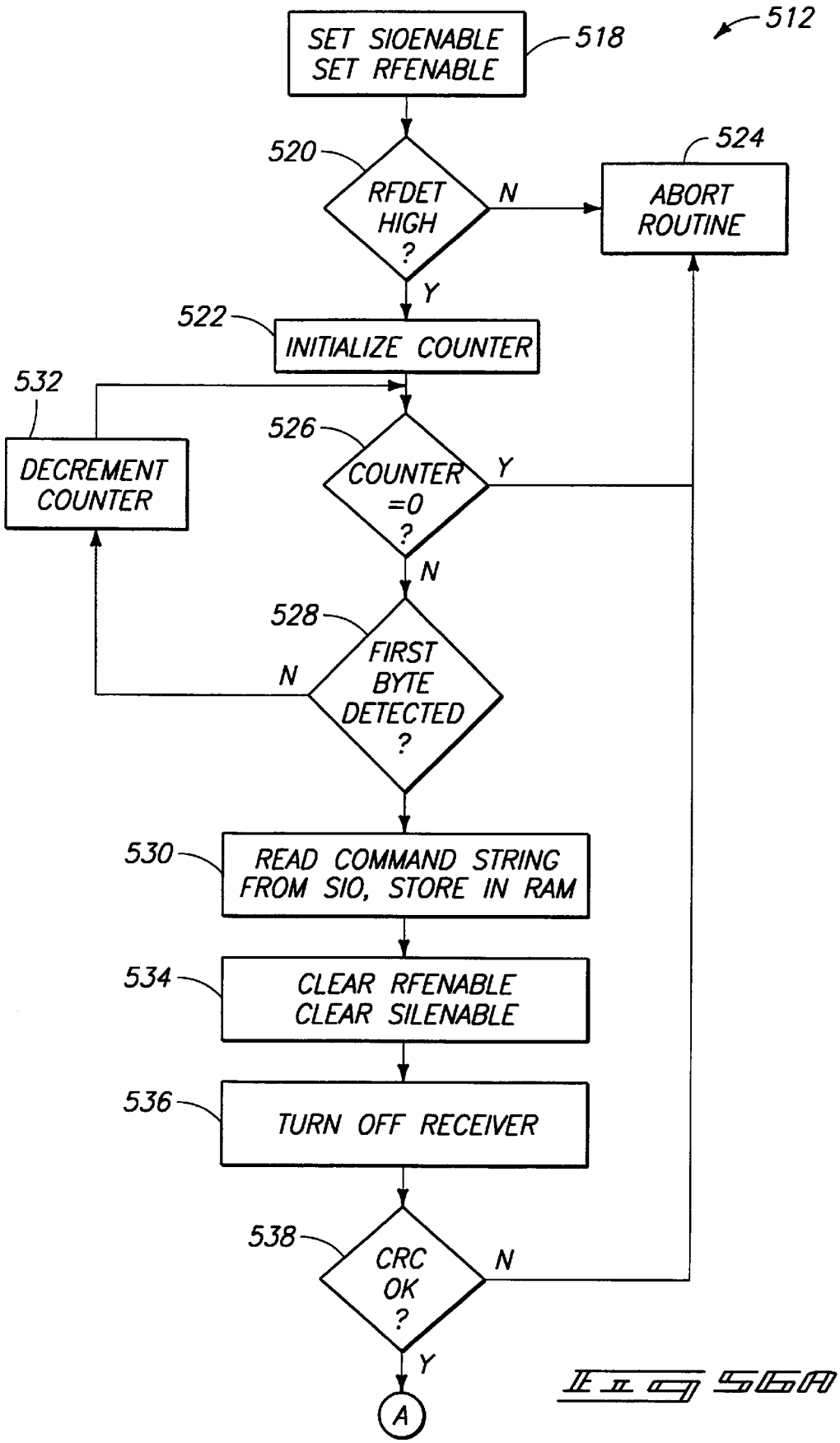

512
SET SIOENABLE
SET RFENABLE
518
520
RFDET HIGH ?
N
524
ABORT ROUTINE
Y
522
INITIALIZE COUNTER
532
DECREMENT COUNTER
526
COUNTER =0 ?
Y
N
528
FIRST BYTE DETECTED ?
N
530
READ COMMAND STRING FROM SIO, STORE IN RAM
534
CLEAR RFENABLE
CLEAR SILENABLE
536
TURN OFF RECEIVER
538
CRC OK ?
N
Y
A

Fig 56A

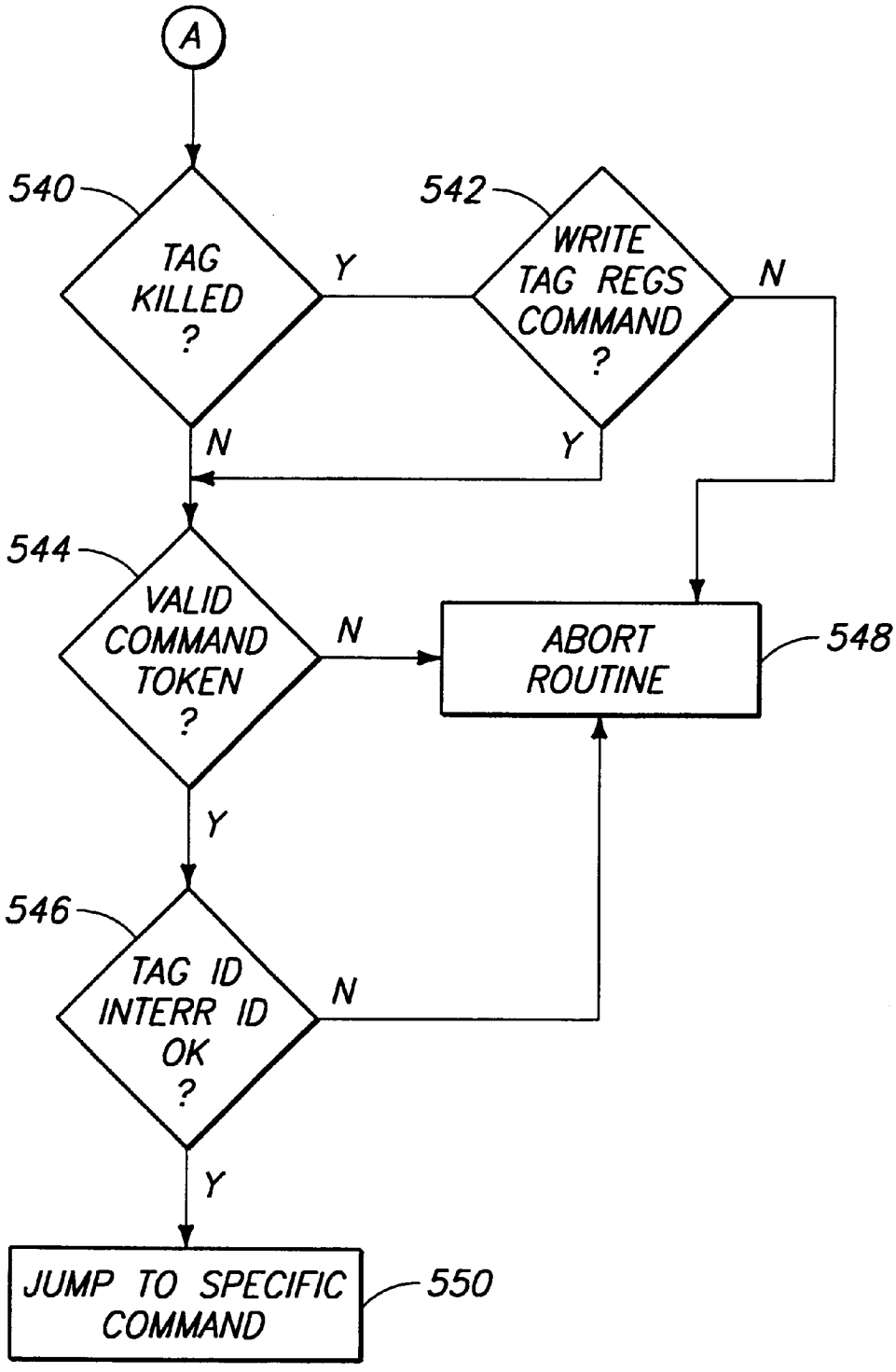

A
540
TAG KILLED ?
Y
542
WRITE TAG REGS COMMAND ?
N
N
Y
544
VALID COMMAND TOKEN ?
N
ABORT ROUTINE
548
Y
546
TAG ID INTERR ID OK ?
N
Y
JUMP TO SPECIFIC COMMAND
550

Fig 56B

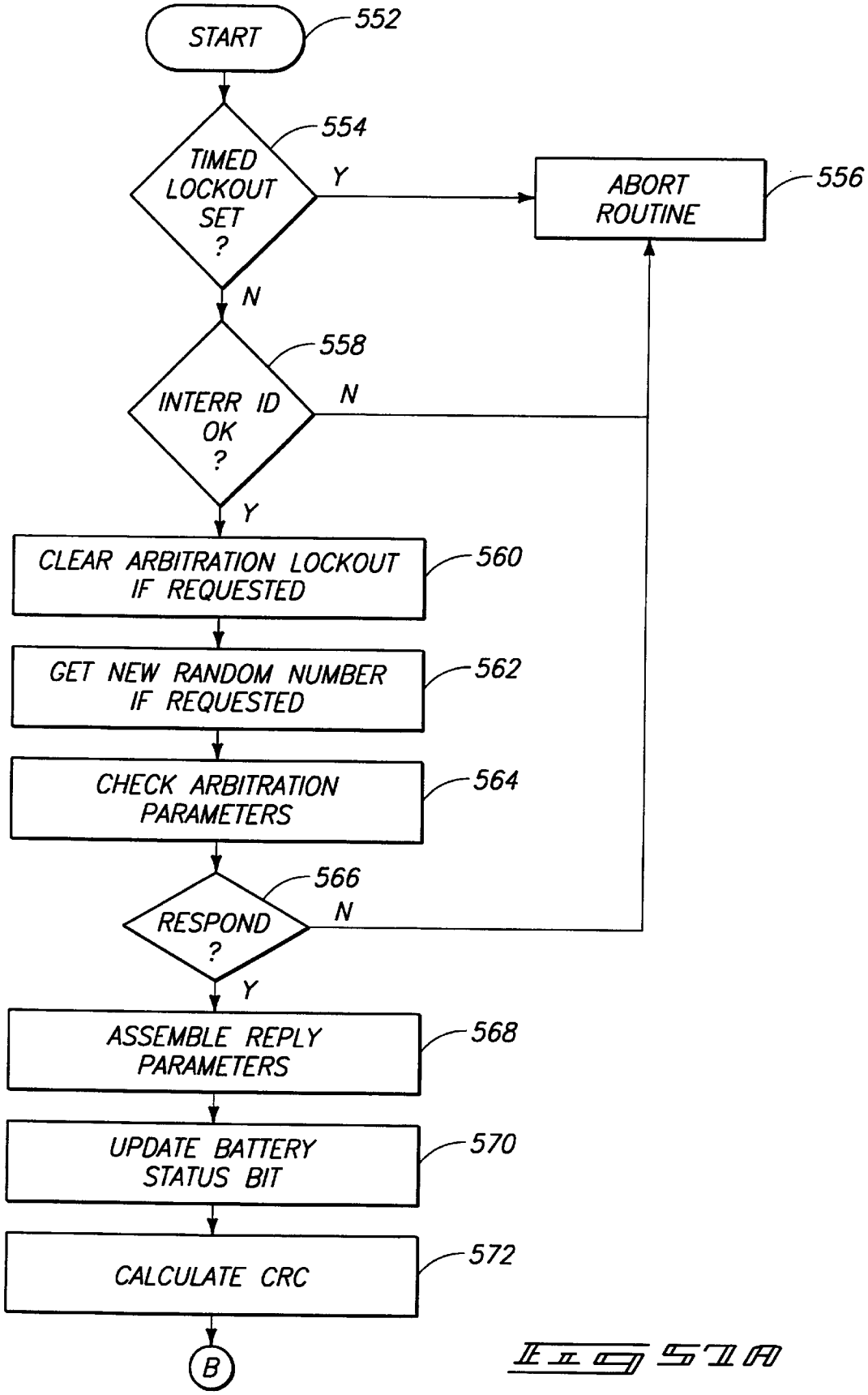

START
552
TIMED LOCKOUT SET ?
554
Y
ABORT ROUTINE
556
N
INTERR ID OK ?
558
N
Y
CLEAR ARBITRATION LOCKOUT IF REQUESTED
560
GET NEW RANDOM NUMBER IF REQUESTED
562
CHECK ARBITRATION PARAMETERS
564
RESPOND ?
566
N
Y
ASSEMBLE REPLY PARAMETERS
568
UPDATE BATTERY STATUS BIT
570
CALCULATE CRC
572
B

Fig 51A

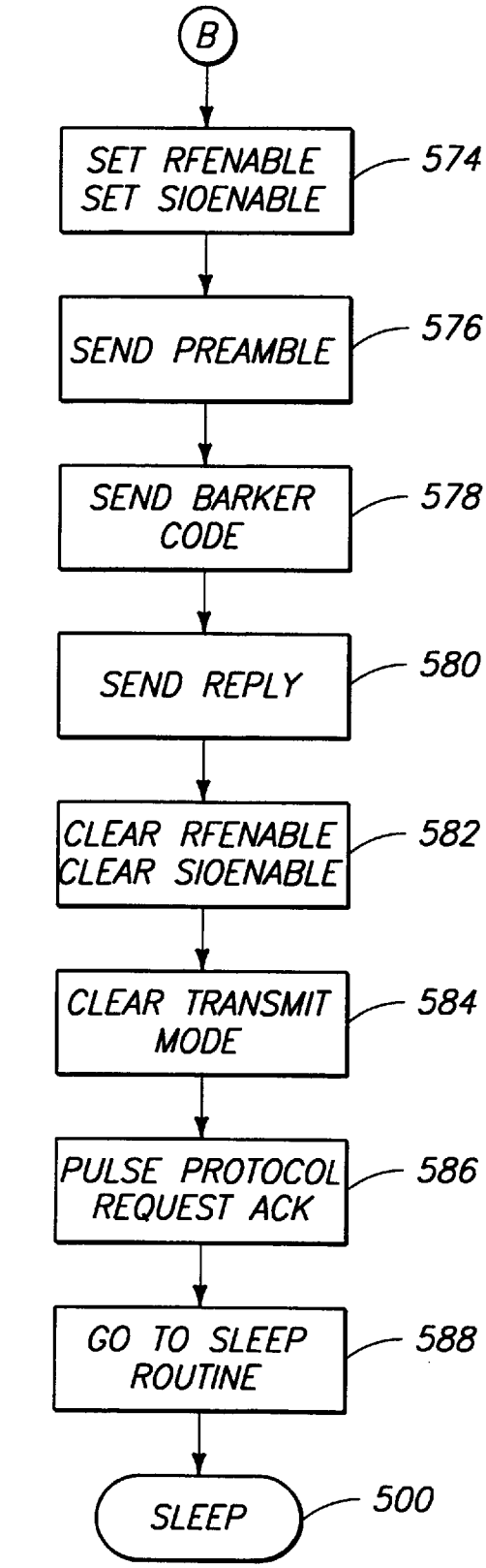

B
SET RFENABLE
SET SIOENABLE
574
SEND PREAMBLE
576
SEND BARKER CODE
578
SEND REPLY
580
CLEAR RFENABLE
CLEAR SIOENABLE
582
CLEAR TRANSMIT MODE
584
PULSE PROTOCOL REQUEST ACK
586
GO TO SLEEP ROUTINE
588
SLEEP
500

Fig 5IB

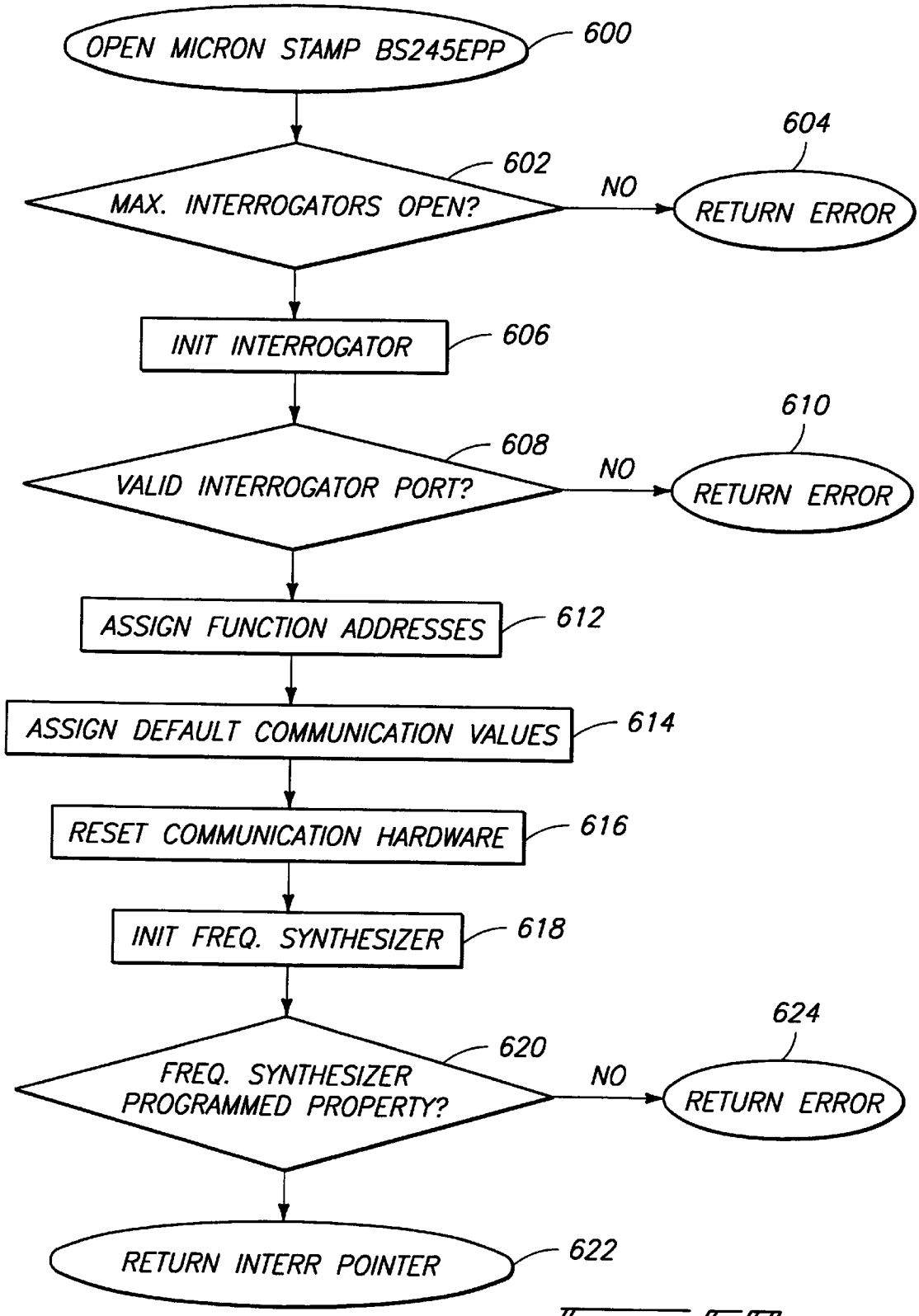

OPEN MICRON STAMP BS245EPP
600
MAX. INTERROGATORS OPEN?
602
NO
604
RETURN ERROR
INIT INTERROGATOR
606
VALID INTERROGATOR PORT?
608
NO
610
RETURN ERROR
ASSIGN FUNCTION ADDRESSES
612
ASSIGN DEFAULT COMMUNICATION VALUES
614
RESET COMMUNICATION HARDWARE
616
INIT FREQ. SYNTHESIZER
618
FREQ. SYNTHESIZER PROGRAMMED PROPERTY?
620
NO
624
RETURN ERROR
RETURN INTERR POINTER
622

Fig 58

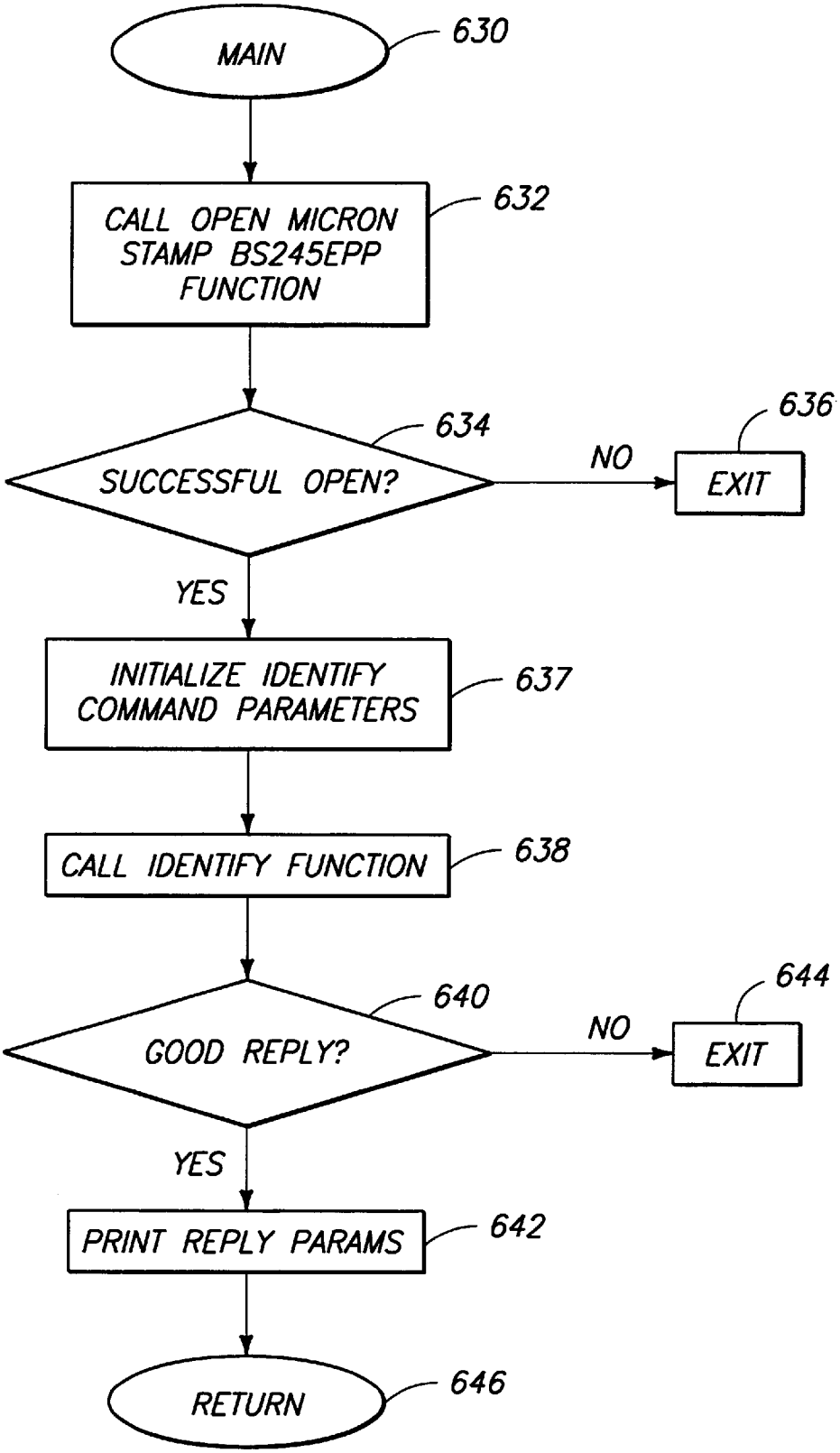

MAIN
630
CALL OPEN MICRON STAMP BS245EPP FUNCTION
632
SUCCESSFUL OPEN?
634
NO
EXIT
636
YES
INITIALIZE IDENTIFY COMMAND PARAMETERS
637
CALL IDENTIFY FUNCTION
638
GOOD REPLY?
640
NO
EXIT
644
YES
PRINT REPLY PARAMS
642
RETURN
646

Fig 59

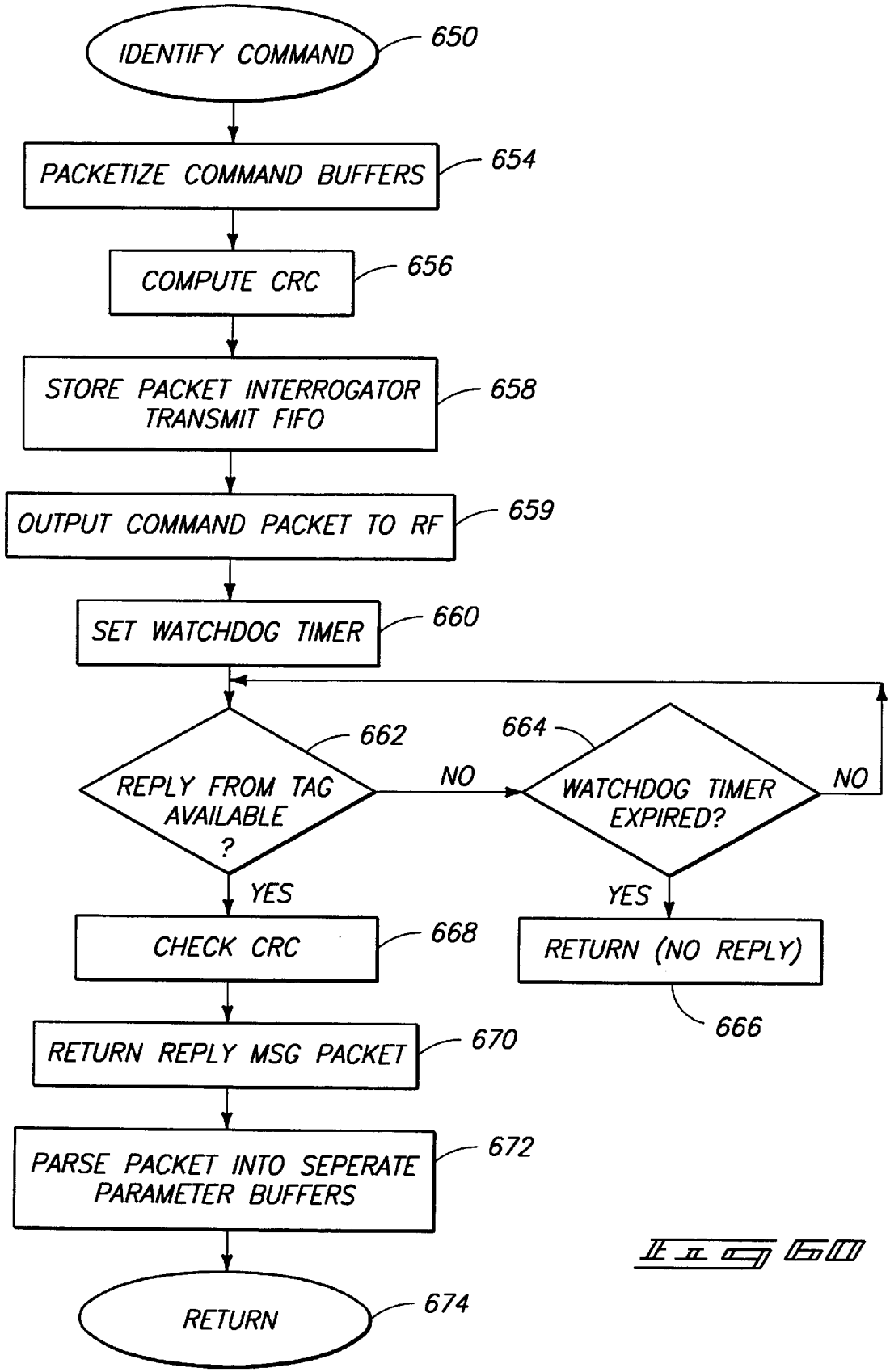

IDENTIFY COMMAND
650
PACKETIZE COMMAND BUFFERS
654
COMPUTE CRC
656
STORE PACKET INTERROGATOR TRANSMIT FIFO
658
OUTPUT COMMAND PACKET TO RF
659
SET WATCHDOG TIMER
660
REPLY FROM TAG AVAILABLE ?
662
NO
WATCHDOG TIMER EXPIRED?
664
NO
YES
YES
CHECK CRC
668
RETURN (NO REPLY)
666
RETURN REPLY MSG PACKET
670
PARSE PACKET INTO SEPERATE PARAMETER BUFFERS
672
RETURN
674

Fig 60

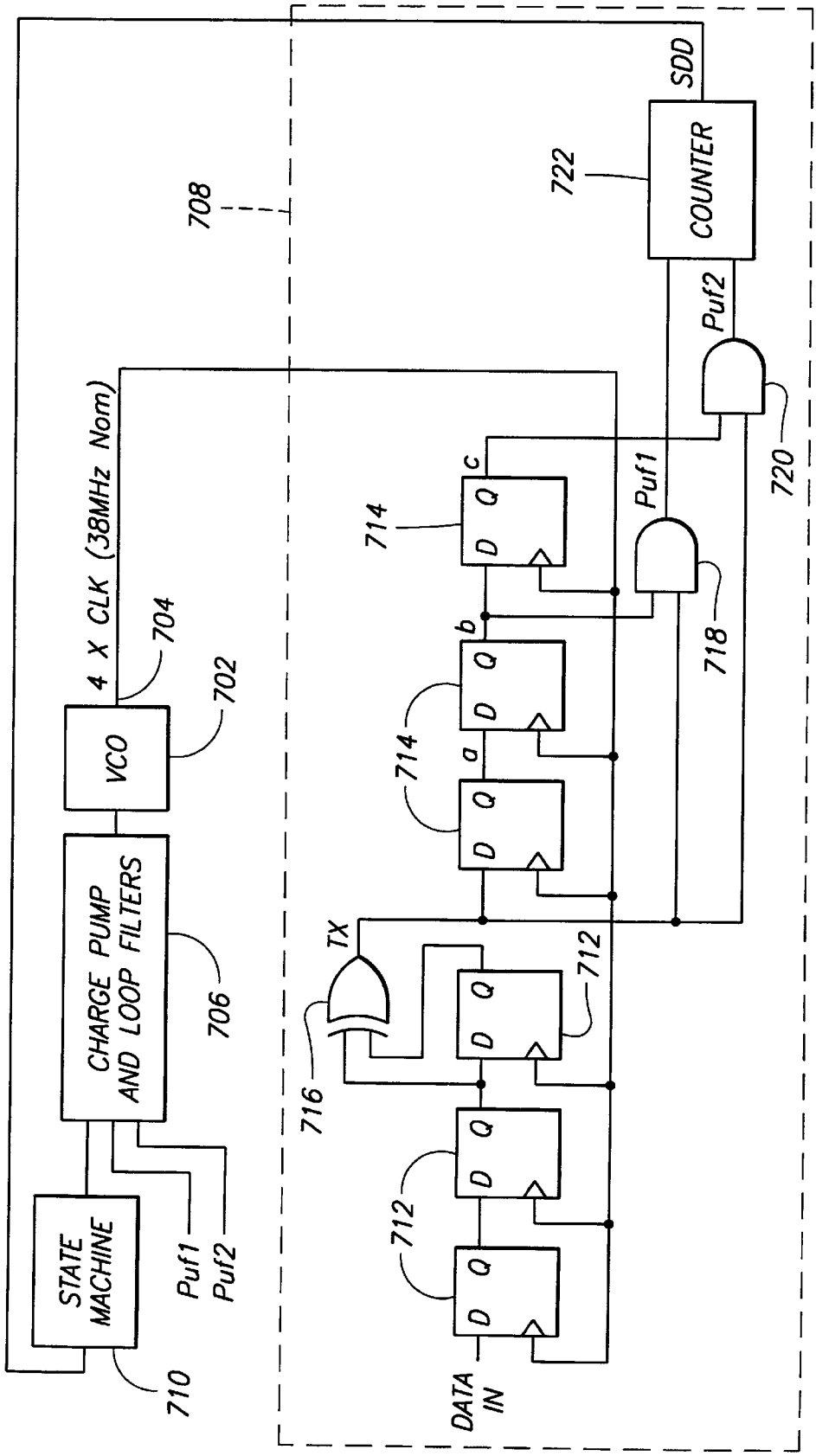

700
708
722
COUNTER
SDD
Puf2
720
Puf1
718
714
c
b
a
Q
D
714
712
712
TX
716
4 X CLK (38MHz Nom)
704
VCO
702
CHARGE PUMP AND LOOP FILTERS
706
STATE MACHINE
710
Puf1
Puf2
DATA IN

FIG. 11

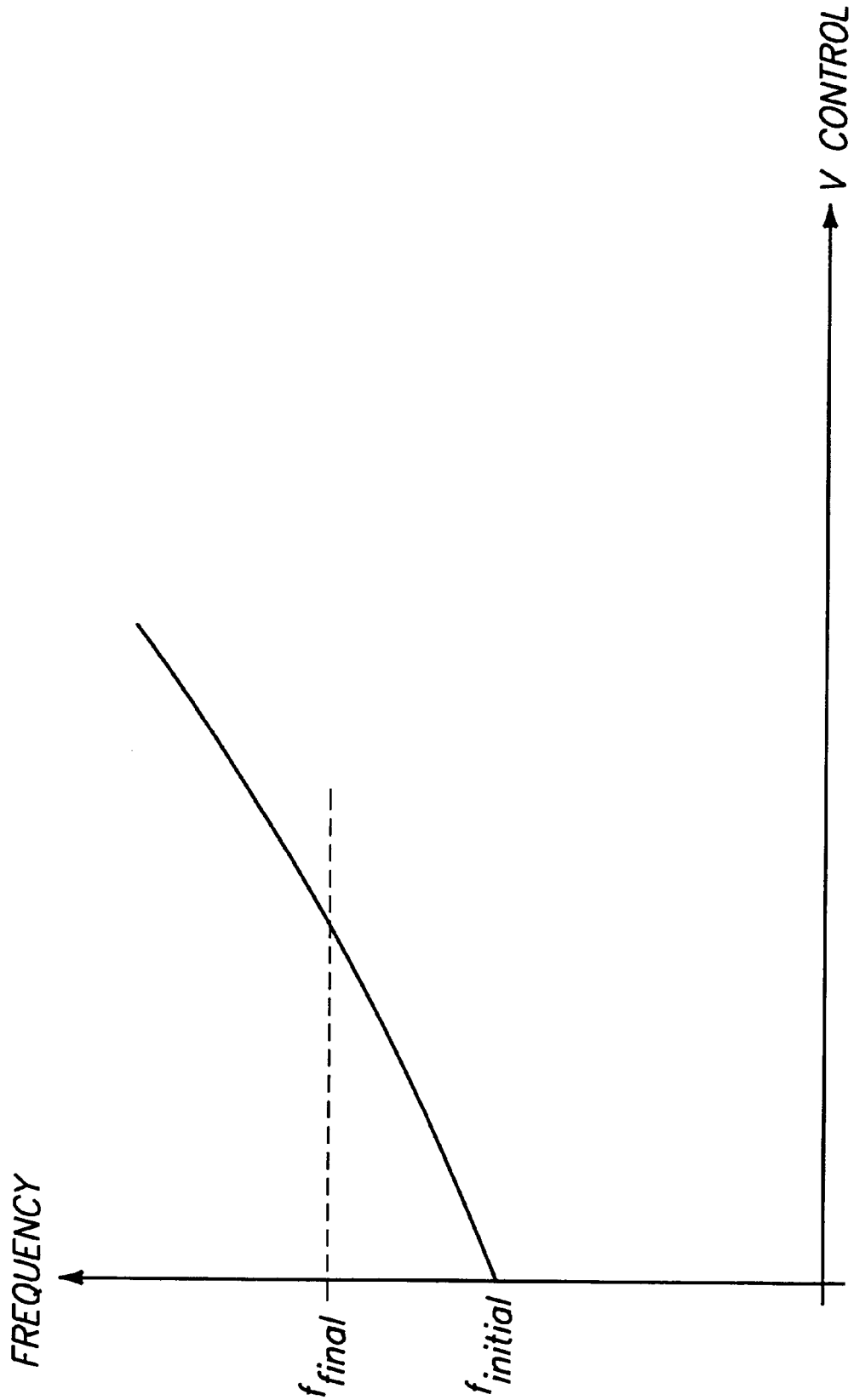


FIG 57H

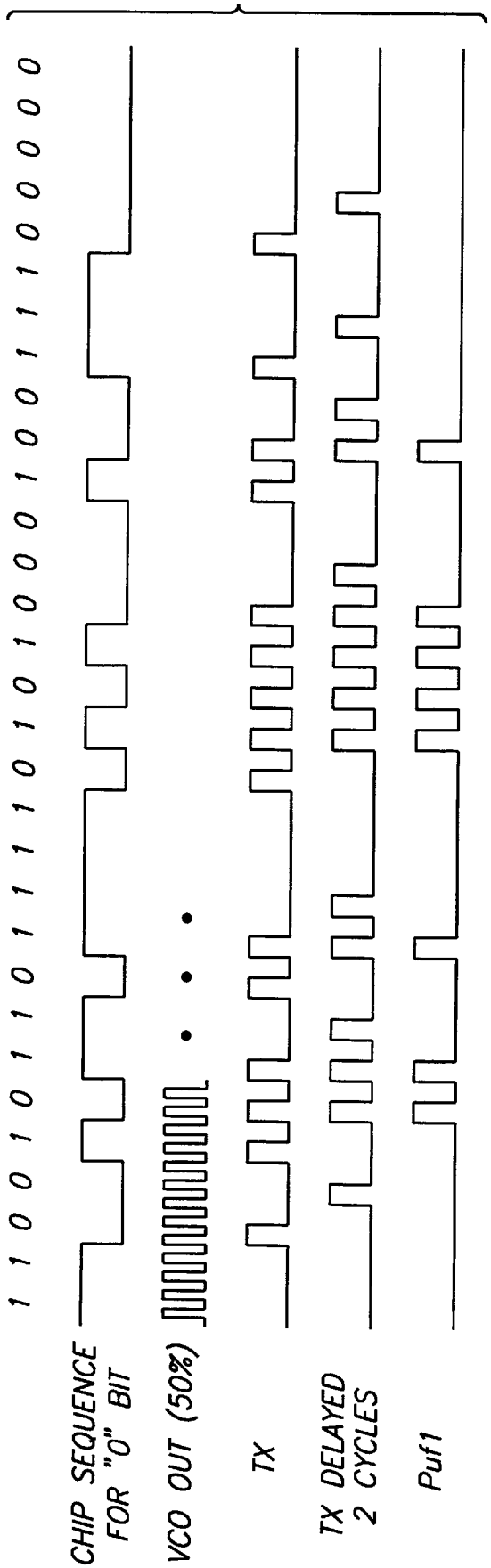

1 1 0 0 1 0 1 1 0 1 1 1 1 1 0 1 0 1 0 0 0 1 0 0 1 1 1 1 0 0 0 0 0
CHIP SEQUENCE FOR "0" BIT
VCO OUT (50%)
TX
TX DELAYED 2 CYCLES
Puf1

FIG 63

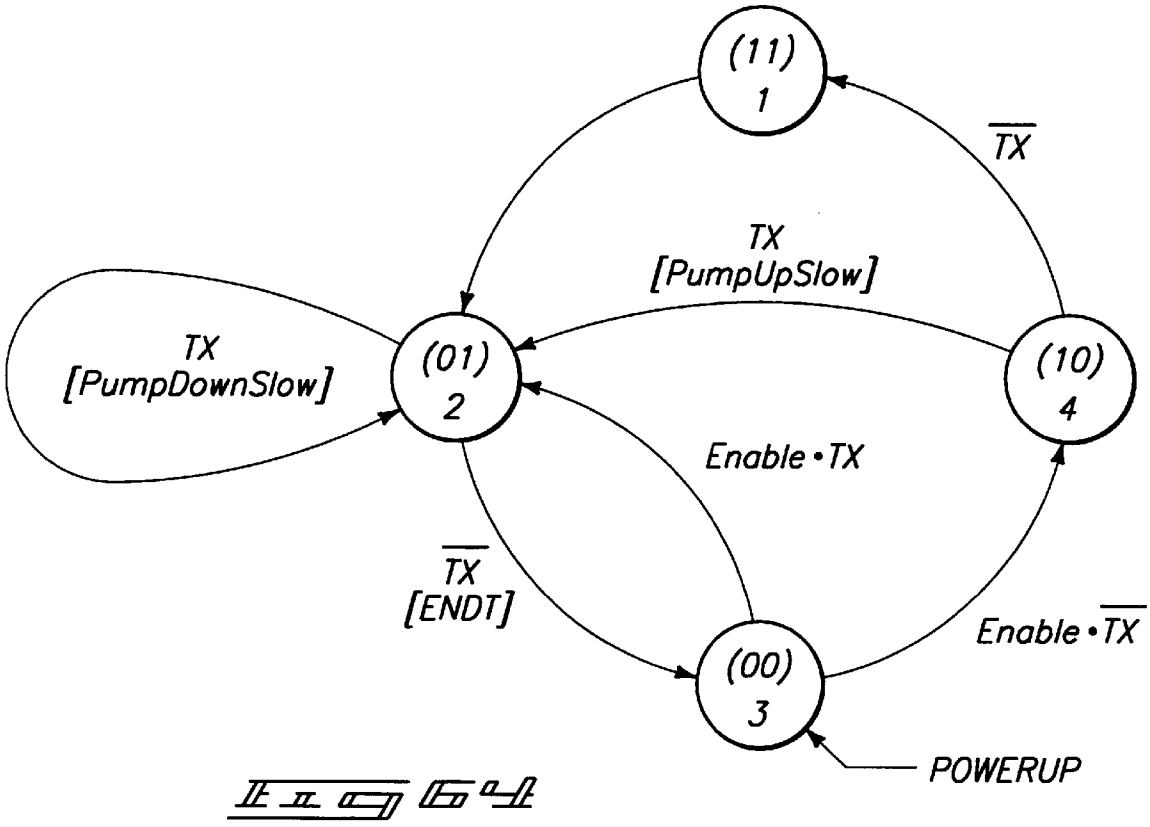

(11)
1
$\overline{TX}$
TX
[PumpUpSlow]
TX
[PumpDownSlow]
(01)
2
(10)
4
Enable • TX
$\overline{TX}$
[ENDT]
Enable • $\overline{TX}$
(00)
3
POWERUP

Fig 64

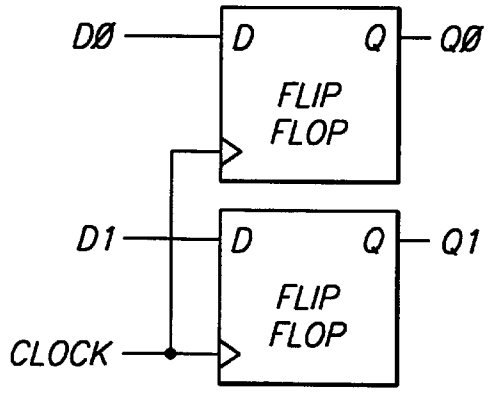

DØ
D
Q
QØ
FLIP
FLOP
D1
D
Q
Q1
FLIP
FLOP
CLOCK

Fig 65

ENABLE	TX	PRESENT STATE Q1	PRESENT STATE Q0	NEXT STATE D1	NEXT STATE D0
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	0	1	0
1	1	0	0	0	1
X	0	0	1	0	0
X	1	0	1	0	1
X	X	1	1	0	1
X	0	1	0	1	1
X	1	1	0	0	1

FIG 66

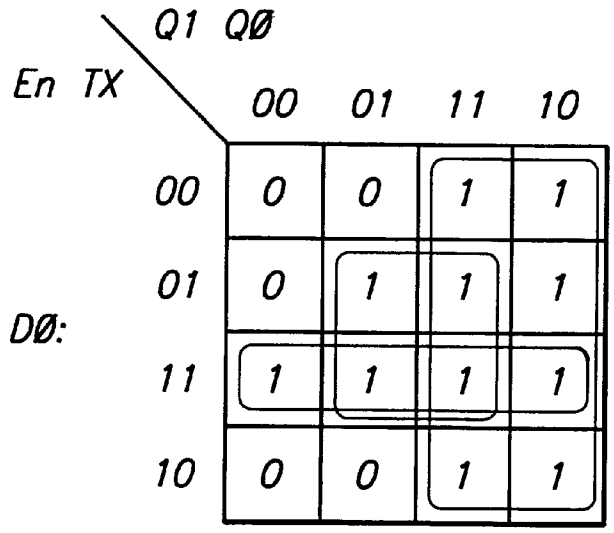

Q1 Q0
En TX
00 01 11 10
D0:
00 0 0 1 1
01 0 1 1 1
11 1 1 1 1
10 0 0 1 1

Fig 6A

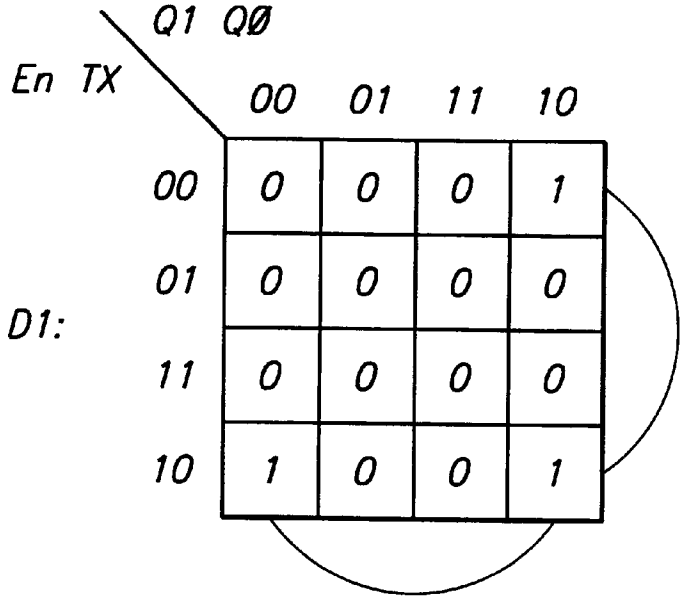

Q1 Q0
En TX
00 01 11 10
D1:
00 0 0 0 1
01 0 0 0 0
11 0 0 0 0
10 1 0 0 1

Fig 6B

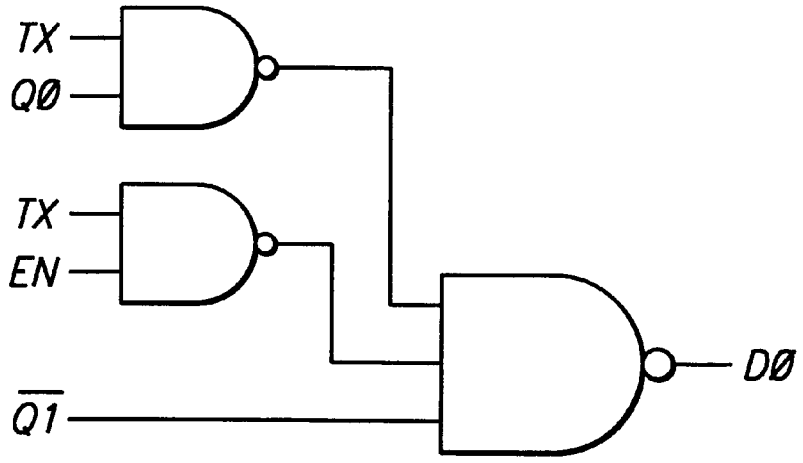


Fig 69

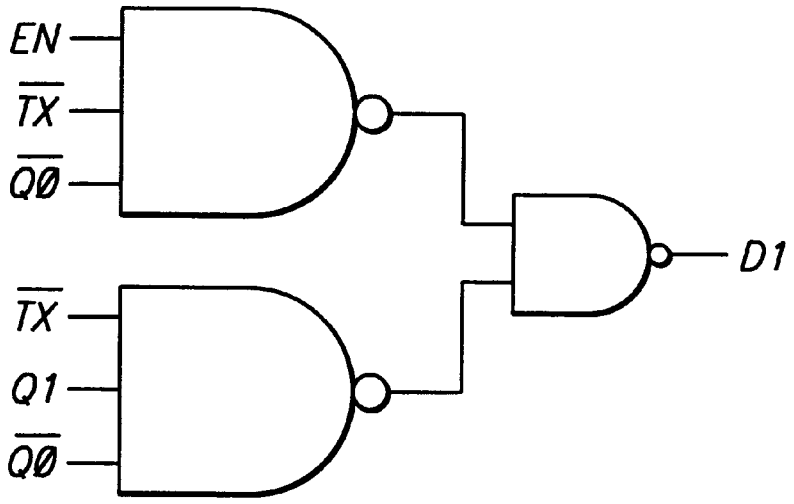


Fig 70

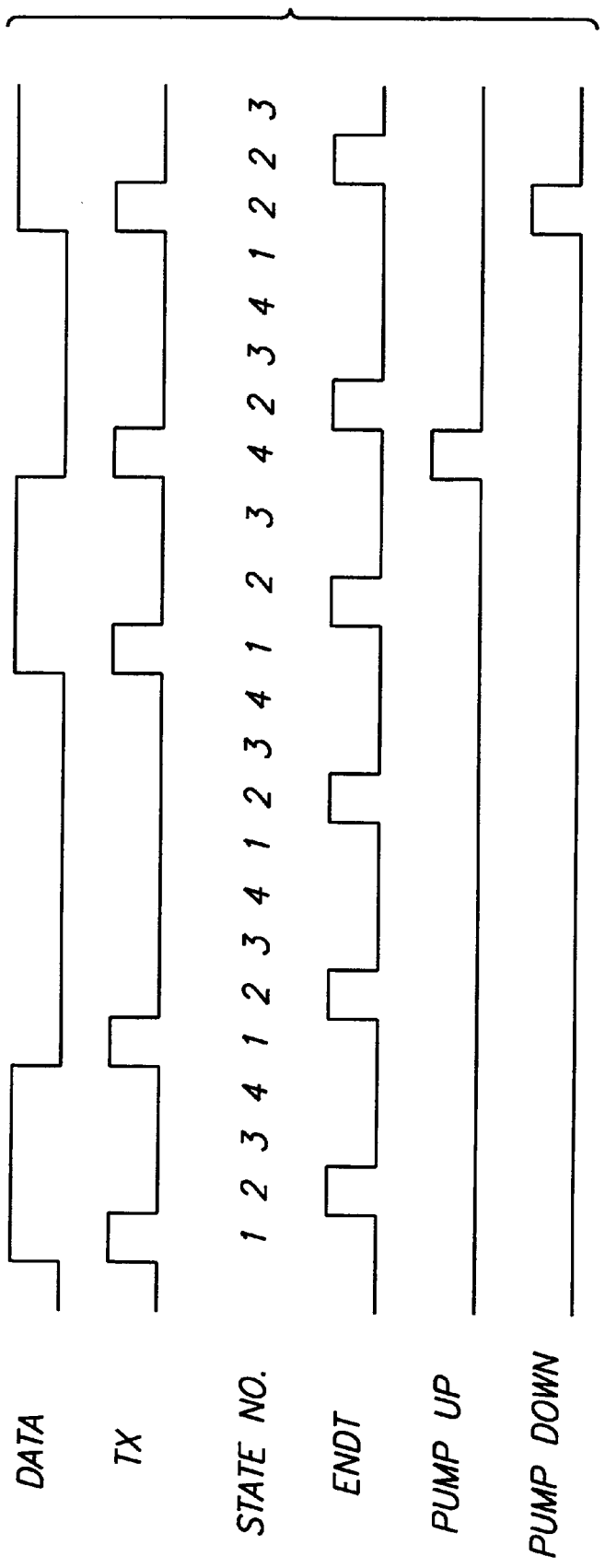

DATA
TX
STATE NO.
1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4 1 2 2 3
ENDT
PUMP UP
PUMP DOWN

FIG 11

NAME	CURRENT (μA)	ΔV (mV)	$\Delta V/V$ CONTROL(NOM) X 100
COARSE	40	160	13.3%
MEDIUM	10	40	3.3
MEDIUM FINE	1	2.6	0.22
FINE	0.1	0.26	0.022

FIG 22

RADIO FREQUENCY DATA COMMUNICATIONS DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S. Provisional Application 60/017,900, filed May 13, 1996, titled "Radio Frequency Data Communication Device."

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REFERENCE TO MICROFICHE

Appended hereto is a microfiche copy of a software guide entitled "Micron RFID Systems Developer's Guide," May 2, 1996. This appendix has 5 microfiche providing 266 total frames.

TECHNICAL FIELD

This invention relates to radio frequency communication devices. More particularly, the invention relates to radio frequency identification devices for inventory control, object monitoring, or for determining the existence, location or movement of objects.

BACKGROUND OF THE INVENTION

As large numbers of objects are moved in inventory, product manufacturing, and merchandising operations, there is a continuous challenge to accurately monitor the location and flow of objects. Additionally, there is a continuing goal to interrogate the location of objects in an inexpensive and streamlined manner. Furthermore, there is a need for tag devices suitably configured to mount to a variety of objects including goods, items, persons, or animals, or substantially any moving or stationary and animate or inanimate object. One way of tracking objects is with an electronic identification system.

One presently available electronic identification system utilizes a **1**s magnetic field modulation system to monitor tag devices. An interrogator creates a magnetic field that becomes detuned when the tag device is passed through the magnetic field. In some cases, the tag device may be provided with a unique identification code in order to distinguish between a number of different tags. Typically, the tag devices are entirely passive (have no power supply), which results in a small and portable package. However, this identification system is only capable of distinguishing a limited number of tag devices, over a relatively short range, limited by the size of a magnetic field used to supply power to the tags and to communicate with the tags.

Another electronic identification system utilizes an RF transponder device affixed to an object to be monitored, in which an interrogator transmits an interrogation signal to the device. The device receives the signal, then generates and transmits a responsive signal. The interrogation signal and the responsive signal are typically radio-frequency (RF) signals produced by an RF transmitter circuit. Since RF signals can be transmitted over greater distances than magnetic fields, RF-based transponder devices tend to be more suitable for applications requiring tracking of a tagged device that may not be in close proximity to an interrogator. For example, RF-based transponder devices tend to be more suitable for inventory control or tracking.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings. Like names for circuit blocks indicate like components. Where there are a plurality of identical circuit blocks, detailed drawings are provided for one such circuit block. Some circuit schematics have been numbered in a hierarchial manner to reflect the hierarchial nature of these drawings. Notwithstanding the order in which the figures are numbered, note that some detailed drawings provide details to blocks included in more than one higher level drawing. Some circuit schematics have been broken up into many portions due to size requirements for patent drawings.

FIG. **1** is a high level circuit schematic showing a circuit embodying the invention.

FIG. **2** is a front view of an employee badge according to but one embodiment the invention.

FIG. **3** is a front view of a radio frequency identification tag according to another embodiment of the invention.

FIG. **4** is a block diagram of an electronic identification system according to the invention and including an interrogator and the tag of FIG. **3**.

FIG. **5** is a high level circuit schematic of a monolithic semiconductor integrated circuit utilized in the devices of FIGS. **1**–**4**.

FIG. **6** is a graph illustrating how FIGS. **6**AA–EK are to be assembled. After such assembly, FIGS. **6**AA–EK provide a circuit drawing of another high level circuit schematic of the monolithic semiconductor integrated circuit of FIG. **5**, showing pads and other details.

FIG. **6.01** is a layout diagram illustrating the physical layout of various components on an integrated circuit die, in accordance with one embodiment of the invention. The physical locations and sizes of components relative to other components are shown. Boundaries between various blocks may be approximate in the sense that portions of certain blocks may extend into other blocks.

FIG. **7** is a graph illustrating how FIGS. **7**AA–HJ are to be assembled. After such assembly, FIGS. **7**AA–HJ provide a circuit drawing of a data processor "dataproc" included in the circuit of FIGS. **6**AA–EK.

FIG. **7.01** is a graph illustrating how FIGS. **7.01**AA–BB are to be assembled. After such assembly, FIGS. **7.01**AA–BB provide a circuit drawing of a processor clock generator "clk" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0101** is a graph illustrating how FIGS. **7.0101**AA–BB are to be assembled. After such assembly, FIGS. **7.0101**AA–BB provide a circuit drawing of a processor clock controller "clkctl" included in the circuit of FIGS. **7.01**AA–BB.

FIG. **7.0102** is a graph illustrating how FIGS. **7.0102**AE–DJ are to be assembled. After such assembly, FIGS. **7.0102**AE–DJ provide a circuit drawing of a phase generator "clkph" included in the circuit of FIGS. **7.01**AA–BB.

FIG. **7.0103** is a graph illustrating how FIGS. **7.0103**AA–BD are to be assembled. After such assembly, FIGS. **7.0103**AA–BD provide a circuit drawing of a state generator "clkst" included in the circuit of FIGS. **7.01**AA–BB.

FIG. **7.010301** is a graph illustrating how FIGS. **7.010301**AA–BB are to be assembled. After such assembly, FIGS. **7.010301**AA–BB provide a circuit drawing of a clock generator counter bit "clkcbit" included in the circuit of FIGS. **7.0103**AA–BD.

FIG. **7.02** is a graph illustrating how FIGS. **7.02**AA–BF are to be assembled. After such assembly, FIGS. **7.02**AA–BF provide a circuit drawing of an address decoder "adrdec" included in the circuit of FIGS. **7**AA–BF.

FIG. **7.03** is a graph illustrating how FIGS. **7.03**AA–EH are to be assembled. After such assembly, FIGS. **7.03**AA–EH provide a circuit drawing of a 512 byte RAM "ram" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0301** is a graph illustrating how FIGS. **7.0301**AA–BB are to be assembled. After such assembly, FIGS. **7.0301**AA–BB provide a circuit drawing of a RAM control circuit "ramctl" included in the circuit of FIGS. **7.03**AA–BB.

FIG. **7.0302** is a graph illustrating how FIGS. **7.0302**AA–AC are to be assembled. After such assembly, FIGS. **7.0302**AA–AC provide a circuit drawing of an 8×4 RAM array "ram8×4" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.030201** is a circuit drawing of a six transistor RAM cell "ramcell" included in the circuit of FIGS. **7.0302**AA–AC.

FIG. **7.0303** is a graph illustrating how FIGS. **7.0303**AA–AD are to be assembled. After such assembly, FIGS. **7.0303**AA–AD provide a circuit drawing of a RAM precharge circuit "rampch" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.0304** is a graph illustrating how FIGS. **7.0304**AA–AD are to be assembled. After such assembly, FIGS. **7.0304**AA–AD provide a circuit drawing of a second RAM precharge circuit "ramdch" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.0305** is a circuit drawing of a RAM address buffer "ramadb" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.0306** is a graph illustrating how FIGS. **7.0306**AA–BA are to be assembled. After such assembly, FIGS. **7.0306**AA–BA provide a circuit drawing of a RAM word line driver "ramwdr" included in the circuit of FIGS. **7.03**AA–EH. if FIG. **7.0307** is a graph illustrating how FIGS. **7.0307**AA–BB are to be assembled. After such assembly, FIGS. **7.0307**AA–BB provide a circuit drawing of a RAM word line decoder "ramwdec" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.0308** is a graph illustrating how FIGS. **7.0308**AA–BB are to be assembled. After such assembly, FIGS. **7.0308**AA–BB provide a circuit drawing of a RAM column select decode circuit "ramcdec" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.0309** is a graph illustrating how FIGS. **7.0309**AA–BG are to be assembled. After such assembly, FIGS. **7.0309**AA–BG provide a circuit drawing of a RAM column selector "ramcsel" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.0310** is a graph illustrating how FIGS. **7.0310**AA–BB are to be assembled. After such assembly, FIGS. **7.0310**AA–BB provide a circuit drawing of a RAM databus interface "ramdb" included in the circuit of FIGS. **7.03**AA–EH.

FIG. **7.04** is a graph illustrating how FIGS. **7.04**AA–HJ are to be assembled. After such assembly, FIGS. **7.04**AA–HJ provide a circuit drawing of a ROM "rom" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0401** is a graph illustrating how FIGS. **7.0401**AA–BB are to be assembled. After such assembly, FIGS. **7.0401**AA–BB provide a circuit drawing of a ROM control logic circuit "romctl" included in the circuit of FIGS. **7.04**AA–HJ.

FIG. **7.0402** is a graph illustrating how FIGS. **7.0402**AA–AB are to be assembled. After such assembly, FIGS. **7.0402**AA–AB provide a circuit drawing of a ROM bit line precharge circuit "rompch" included in the circuit of FIGS. **7.04**AA–HJ.

FIG. **7.0403** is a graph illustrating how FIGS. **7.0403**AA–BB are to be assembled. After such assembly, FIGS. **7.0403**AA–BB provide a circuit drawing of a ROM word line driver "romwdr" included in the circuit of FIGS. **7.04**AA–HJ.

FIG. **7.0404** is a graph illustrating how FIGS. **7.0404**AB–DC are to be assembled. After such assembly, FIGS. **7.0404**AA–DC provide a circuit drawing of a ROM word block decoder "romwdec_rev" included in the circuit of FIGS. **7.04**AA–HJ.

FIG. **7.0405** is a graph illustrating how FIGS. **7.0405**AA–BA are to be assembled. After such assembly, FIGS. **7.0405**AA–BA provide a circuit drawing of a ROM bit line address driver "rombldr" included in the circuit of FIGS. **7.04**AA–HJ.

FIG. **7.0406** is a graph illustrating how FIGS. **7.0406**AA–CK are to be assembled. After such assembly, FIGS. **7.0406**AA–CK provide a circuit drawing of a ROM bit line decoder "rombldec" included in the circuit of FIGS. **7.04**AA–HJ.

FIG. **7.0407** is a graph illustrating how FIGS. **7.0407**AA–AB are to be assembled. After such assembly, FIGS. **7.0407**AA–AB provide a circuit drawing of a ROM sense amplifier "romsns" included in the circuit of FIGS. **7.04**AA–HJ. **11** FIG. **7.05** is a graph illustrating how FIGS. **7.05**AA–CB are to be assembled. After such assembly, FIGS. **7.05**AA–CB provide a circuit drawing of an instruction register "insreg" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0501** is a graph illustrating how FIGS. **7.0501**AA–AB are to be assembled. After such assembly, FIGS. **7.0501**AA–AB provide a circuit drawing of an instruction register cell "insrcel" included in the circuit of FIGS. **7.05**AA–CB.

FIG. **7.06** is a graph illustrating how FIGS. **7.06**AA–CN are to be assembled. After such assembly, FIGS. **7.06**AA–CN provide a circuit drawing of an instruction decoder PLA "insdec" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0601** is a graph illustrating how FIGS. **7.0601**AA–HI are to be assembled. After such assembly, FIGS. **7.0601**AA–HI provide a circuit drawing of an instruction decoder "insdec**1**" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0602** is a graph illustrating how FIGS. **7.0602**AA–JH are to be assembled. After such assembly, FIGS. **7.0602**AA–JH provide a circuit drawing of an instruction decoder (second section) "insdec**2**" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0603** is a graph illustrating how FIGS. **7.0603**AA–JI are to be assembled. After such assembly, FIGS. **7.0603**AA–JI provide a circuit drawing of an instruction decoder (third section) "insdec**3**" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0604** is a graph illustrating how FIGS. **7.0604**AA–JI are to be assembled. After such assembly,

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FIGS. **7.0604**AA–JI provide a circuit drawing of an instruction decoder (fourth section) "insdec**4**" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.060401** is a circuit drawing of an instruction decoder ROM amp "insramp" included in the circuit of FIGS. **7.0604**AA–JI.

FIG. **7.060402** is a circuit drawing of an instruction decoder PLA amp "inspamp" included in the circuit of FIGS. **7.0604**AA–JI.

FIG. **7.060403** is a circuit drawing of an instruction decoder PLA latch "insplat" included in the circuit of FIGS. **7.0604**AA–JI.

FIG. **7.07** is a graph illustrating how FIGS. **7.07**AA–BB are to be assembled. After such assembly, FIGS. **7.07**AA–BB provide a circuit drawing of a conditional qualifier decoder "cqualdec" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.08** is a graph illustrating how FIGS. **7.08**AA–CA are to be assembled. After such assembly, FIGS. **7.08**AA–CA provide a circuit drawing of a databus latch/precharge circuit "dblatch" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.09** is a graph illustrating how FIGS. **7.09**AA–BF are to be assembled. After such assembly, FIGS. **7.09**AA–BF provide a circuit drawing of an arithmetic logic unit "alu" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.0901** is a graph illustrating how FIGS. **7.0901**AA–CE are to be assembled. After such assembly, FIGS. **7.0901**AA–CE provide a circuit drawing of an ALU low byte "alubyt**1**" included in the circuit of FIGS. **7.09**AA–BF.

FIG. **7.090101** is a graph illustrating how FIGS. **7.090101**AA–AD are to be assembled. After such assembly, FIGS. **7.090101**AA–AD provide a circuit drawing of a bit "alubitl" included in the circuit of FIGS. **7.0901**AA–CE.

FIG. **7.09010101** is a circuit drawing of an ALU bit decoder cell "alubdec" included in the circuit of FIGS. **7.090101**AA–AD.

FIG. **7.09010102** is a circuit drawing of an ALU B register cell "alubcell" included in the circuit of FIGS. **7.090101**AA–AD.

FIG. **7.09010103** is a graph illustrating how FIGS. **7.09010103**AA–AB are to be assembled. After such assembly, FIGS. **7.09010103**AA–AB provide a circuit drawing of an ALU A register cell "aluacell" included in the circuit of FIGS. **7.090101**AA–AD.

FIG. **7.09010104** is a graph illustrating how FIGS. **7.09010104**AA–AB are to be assembled. After such assembly, FIGS. **7.09010104**AA–AB provide a circuit drawing of an ALU register cell "alupc" included in the circuit of FIGS. **7.090101**AA–AD.

FIG. **7.09010105** is a circuit drawing of an ALU register cell "alurcell" included in the circuit of FIGS. **7.090101**AA–AD. Such register cells are used for a stack pointer and data pointer.

FIG. **7.09010106** is a graph illustrating how FIGS. **7.09010106**AA–AB are to be assembled. After such assembly, FIGS. **7.09010106**AA–AB provide a circuit drawing of an ALU memory address register "alumar" included in the circuit of FIGS. **7.090101**AA–AD.

FIG. **7.09010107** is a circuit drawing of an ALU slave cell "aluslave" included in the circuit of FIGS. **7.090101**AA–AD.

FIG. **7.09010108** is a graph illustrating how FIGS. **7.09010108**AA–BC are to be assembled. After such assembly, FIGS. **7.09010108**AA–BC provide a circuit drawing of an ALU adder "aluadd" included in the circuit of FIGS. **7.090101**AA–AD.

FIG. **7.0902** is a graph illustrating how FIGS. **7.0902**AA–BD are to be assembled. After such assembly, FIGS. **7.0902**AA–BD provide a circuit drawing of an ALU high byte "alubyth" included in the circuit of FIGS. **7.09**AA–BF.

FIG. **7.090201** is a graph illustrating how FIGS. **7.090201**AA–AC are to be assembled. After such assembly, FIGS. **7.090201**AA–AC provide a circuit drawing of a bit "alubith " included in the circuit of FIGS. **7.09**AA–BF.

FIG. **7.10** is a graph illustrating how FIGS. **7.10**AA–CC are to be assembled. After such assembly, FIGS. **7.10**AA–CC provide a circuit drawing of a timed lockout divider "tld" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.1001** is a circuit drawing of a timed lockout divider cell "tldcel" included in the circuit of FIGS. **7.10**AA–CC.

FIG. **7.11** is a graph illustrating how FIGS. **7.11**AA–AB are to be assembled. After such assembly, FIGS. **7.11**AA–AB provide a circuit drawing of a timed lockout register "tloreg" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.1101** is a graph illustrating how FIGS. **7.1101**AA–AC are to be assembled. After such assembly, FIGS. **7.1101**AA–AC provide a circuit drawing of a timed lockout register cell "tlorcel" included in the circuit of FIGS. **7.11**AA–AB.

FIG. **7.12** is a graph illustrating how FIGS. **7.12**AA–AC are to be assembled. After such assembly, FIGS. **7.12**AA–AC provide a circuit drawing of a R/W control register "oreg" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.1201** is a circuit drawing of a R/W control register cell "regcell" included in the circuit of FIGS. **7.12**AA–AC.

FIG. **7.13** is a graph illustrating how FIGS. **7.13**AA–BA are to be assembled. After such assembly, FIGS. **7.13**AA–BA provide a circuit drawing of a status register "sreg" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.1301** is a circuit drawing of a status register cell "sregcel" included in the circuit of FIGS. **7.13**AA–BA.

FIG. **7.14** is a graph illustrating how FIGS. **7.14**AA–AB are to be assembled. After such assembly, FIGS. **7.14**AA–AB provide a circuit drawing of a serial input/output block "sio" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.1401** is a graph illustrating how FIGS. **7.1401**AA–GF are to be assembled. After such assembly, FIGS. **7.1401**AA–GF provide a circuit drawing of a serial input/output data path "siodata" included in the circuit of FIGS. **7.14**AA–AB.

FIG. **7.140101** is a graph illustrating how FIGS. **7.140101**AA–AB are to be assembled. After such assembly, FIGS. **7.140101**AA–AB provide a circuit drawing of a serial input/output register cell "sioreg" included in the circuit of FIGS. **7.1401**AA–AB.

FIG. **7.140102** is a circuit drawing of a serial input/output XOR circuit "sioxor" included in the circuit of FIGS. **7.1401**AA–GF.

FIG. **7.140103** is a graph illustrating how FIGS. **7.140103**AA–AB are to be assembled. After such assembly, FIGS. **7.140103**AA–AB provide a circuit drawing of a bidirectional latch "siobdlat_inv" included in the circuit of FIGS. **7.1401**AA–GF.

FIG. **7.140104** is a graph illustrating how FIGS. **7.140104**AA–AB are to be assembled. After such assembly, FIGS. **7.140104**AA–AB provide a circuit drawing of a shift

register "sioshr" included in the circuit of FIGS. **7.1401**AA–GF.

FIG. **7.140105** is a graph illustrating how FIGS. **7.140105**AA–AB are to be assembled. After such assembly, FIGS. **7.140105**AA–AB provide a circuit drawing of a bidirectional latch "siobdlat" included in the circuit of FIGS. **7.1401**AA–GF.

FIG. **7.1402** is a graph illustrating how FIGS. **7.1402**BA–EI are to be assembled. After such assembly, FIGS. **7.1402**BA–EI provide a circuit drawing of serial input/output control logic "sioctl" included in the circuit of FIGS. **7.14**AA–AB.

FIG. **7.140201** is a graph illustrating how FIGS. **7.140201**AA–BB are to be assembled. After such assembly, FIGS. **7.140201**AA–BB provide a circuit drawing of a counter bit "siocbit" included in the circuit of FIGS. **7.1402**AA–AB

FIG. **7.15** is a graph illustrating how FIGS. **7.15**AA–EC are to be assembled. After such assembly, FIGS. **7.15**AA–EC provide a circuit drawing of a data interleaver (which interleaves two thirteen bit words) "dil" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.1501** is a graph illustrating how FIGS. **7.1501**AA–CA are to be assembled. After such assembly, FIGS. **7.1501**AA–CA provide a circuit drawing of a data interleaver shift register "dil_sreg" included in the circuit of FIGS. **7.15**AA–EC.

FIG. **7.1502** is a graph illustrating how FIGS. **7.1502**AA–CA are to be assembled. After such assembly, FIGS. **7.1502**AA–CA provide a circuit drawing of a data interleaver shift register with parallel load "dil_plsreg" included in the circuit of FIGS. **7.15**AA–EC.

FIG. **7.150201** is a circuit drawing of a data interleaver shift register bit "dil_sregbit" included in the circuit of FIGS. **7.1502**AA–CA.

FIG. **7.16** is a graph illustrating how FIGS. **7.16**AA–CD are to be assembled. After such assembly, FIGS. **7.16**AA–CD provide a circuit drawing of a convolutional encoder and preamble generator "conv" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.1601** is a circuit drawing of a shift register cell "convshr" included in the circuit of FIGS. **7.16**AA–CD.

FIG. **7.1602** is a circuit drawing of a summer "convsum" included in the circuit of FIGS. **7.16**AA–CD.

FIG. **7.17** is a graph illustrating how FIGS. **7.17**AA–BB are to be assembled. After such assembly, FIGS. **7.17**AA–BB provide a circuit drawing of a shift register input data MUX "shdcel" included in the circuit of FIGS. **7**AA–HJ.

FIG. **7.18** is a graph illustrating how FIGS. **7.18**AA–CC are to be assembled. After such assembly, FIGS. **7.18**AA–CC provide a circuit drawing of a digital port output controller "doutport" included in the circuit of FIGS. **7**AA–HJ.

FIG. **8** is a graph illustrating how FIGS. **8**AA–CB are to be assembled. After such assembly, FIGS. **8**AA–CB provide a circuit drawing of an RF processor "rfproc" included in the circuit of FIGS. **6**AA–EK.

FIG. **8.01** is a graph illustrating how FIGS. **8.01**AA–DE are to be assembled. After such assembly, FIGS. **8.01**AA–DE provide a circuit drawing of a receiver "rx" included in the circuit of FIGS. **8**AA–CB.

FIG. **8.0101** is a graph illustrating how FIGS. **8.0101**AA–CB are to be assembled. After such assembly, FIGS. **8.0101**AA–CB provide a circuit drawing of a Schottky diode detector "diodedet" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.0102** is a graph illustrating how FIGS. **8.0102**AA–BD are to be assembled. After such assembly, FIGS. **8.0102**AA–BD provide a circuit drawing of a CMOS square law detector "cmosdet" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.0103** is a graph illustrating how FIGS. **8.0103**AA–CF are to be assembled. After such assembly, FIGS. **8.0103**AA–CF provide a circuit drawing of a video amplifier "videoamp**1**" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.0104** is a graph illustrating how FIGS. **8.0104**AA–BC are to be assembled. After such assembly, FIGS. **8.0104**AA–BC provide a circuit drawing of a second video amplifier "videoamp**2**" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.0105** is a graph illustrating how FIGS. **8.0105**AA–ED are to be assembled. After such assembly, FIGS. **8.0105**AA–ED provide a circuit drawing of a comparator "comparator" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.0106** is a graph illustrating how FIGS. **8.0106**AA–CD are to be assembled. After such assembly, FIGS. **8.0106**AA–CD provide a circuit drawing of an RF detect circuit "rxdet" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.0107** is a graph illustrating how FIGS. **8.0107**AA–GN are to be assembled. After such assembly, FIGS. **8.0107**AA–GN provide a circuit drawing of a receiver bias generator "rxbias" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.0108** is a graph illustrating how FIGS. **8.0108**AA–AC are to be assembled. After such assembly, FIGS. **8.0108**AA–AC provide a circuit drawing of a data transition detector "datatx" included in the circuit of FIGS. **8.01**AA–DE.

FIG. **8.02** is a graph illustrating how FIGS. **8.02**AA–BC are to be assembled. After such assembly, FIGS. **8.02**A–BC provide a circuit drawing of a low power frequency locked loop "lpfll" included in the circuit of FIGS. **8**AA–CB.

FIG. **8.0201** is a graph illustrating how FIGS. **8.0201**AA–AB are to be assembled. After such assembly, FIGS. **8.0201**AA–AB provide a circuit drawing of a timed lockout divider cell "tldcel_bypass" included in the circuit of FIGS. **8.02**AA–BC.

FIG. **8.0202** is a graph illustrating how FIGS. **8.0202**AA–CD are to be assembled. After such assembly, FIGS. **11 8.0202**AA–CD provide a circuit drawing of a low power frequency locked loop frequency comparator "freqcomp" included in the circuit of FIGS. **8.02**AA–BC.

FIG. **8.0203** is a graph illustrating how FIGS. **8.0203**AA–BC are to be assembled. After such assembly, FIGS. **8.0203**AA–BC provide a circuit drawing of an up/down counter "udcounter" included in the circuit of FIGS. **8.02**AA–BC.

FIG. **8.020301** is a graph illustrating how FIGS. **8.020301**AA–BB are to be assembled. After such assembly, FIGS. **8.020301**AA–BB provide a circuit drawing of an adder "udcounter_adder" included in the circuit of FIGS. **8.0203**AA–BC.

FIG. **8.020302** is a graph illustrating how FIGS. **8.020302**AA–AB are to be assembled. After such assembly, FIGS. **8.020302**AA–AB provide a circuit drawing of a D

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type flip-flop "udcounter_dff" included in the circuit of FIGS. **8.0203**AA–BC.

FIG. **8.0204** is a graph illustrating how FIGS. **8.0204**AA–EJ are to be assembled. After such assembly, FIGS. **8.0204**AA–EJ provide a circuit drawing of a low power current controlled oscillator "lpcco" included in the circuit of FIGS. **8.02**AA–BC.

FIG. **8.0205** is a circuit drawing of a timed lockout divider cell "tldcel" included in the circuit of FIGS. **8.02**AA–BC.

FIG. **8.03** is a graph illustrating how FIGS. **8.03**AA–AB are to be assembled. After such assembly, FIGS. **8.03**AA–AB provide a circuit drawing of a counter bit "lpfll_cbit" included in the circuit of FIGS. **8**AA–CB.

FIG. **8.04** is a graph illustrating how FIGS. **8.04**AA–EE are to be assembled. After such assembly, FIGS. **8.04**AA–EE provide a circuit drawing of a receiver wake up controller "rxwu" included in the circuit of FIGS. **8**AA–CB.

FIG. **8.0401** is a graph illustrating how FIGS. **8.0401**AA–AB are to be assembled. After such assembly, FIGS. **8.0401**AA–AB provide a circuit drawing of wake up abort logic "wuabort" included in the circuit of FIGS. **8.04**AA–EE.

FIG. **8.040101** is a graph illustrating how FIGS. **8.040101**AA–AB are to be assembled. After such assembly, FIGS. **8.040101**AA–AB provide a circuit drawing of wake up abort logic counter bit "wuabort_cbit" included in the circuit of FIGS. **8.0401**AA–AB.

FIG. **8.0402** is a graph illustrating how FIGS. **8.0402**AA–AB are to be assembled. After such assembly, FIGS. **8.0402**AA–AB provide a circuit drawing of a timed lockout divider cell "tldcel" included in the circuit of FIGS. **8.04**AA–EE.

FIG. **8.05** is a graph illustrating how FIGS. **8.05**AA–DE are to be assembled. After such assembly, FIGS. **8.05**AA–DE provide a circuit drawing of a digital clock and data recovery circuit "dcr" included in the circuit of FIGS. **8**AA–CB.

FIG. **8.0501** is a graph illustrating how FIGS. **8.0501**AA–BE are to be assembled. After such assembly, FIGS. **8.0501**AA–BE provide a circuit drawing of a PLL start-up circuit "dcr_startup" included in the circuit of FIGS. **8.05**AA–DE.

FIG. **8.050101** is a graph illustrating how FIGS. **8.050101**AA–AB are to be assembled. After such assembly, FIGS. **8.050101**AA–AB provide a circuit drawing of a shift register cell "dcr_sreg" included in the circuit of FIGS. **8.0501**AA–BE.

FIG. **8.050102** is a graph illustrating how FIGS. **8.050102**AA–AB are to be assembled. After such assembly, FIGS. **8.050102**AA–AB provide a circuit drawing of a counter bit "dcr_counterbit" included in the circuit of FIGS. **8.0501**AA–BE.

FIG. **8.0502** is a graph illustrating how FIGS. **8.0502**AA–CD are to be assembled. After such assembly, FIGS. **8.0502**AA–CD provide a circuit drawing of a PLL state machine "dcr_statemachine" included in the circuit of FIGS. **8.05**AA–DE.

FIG. **8.0503** is a graph illustrating how FIGS. **8.0503**AA–FN are to be assembled. After such assembly, FIGS. **8.0503**AA–FN provide a circuit drawing of a DCR bias generator "dcr_bias" included in the circuit of FIGS. **8.05**AA–DE.

FIG. **8.0504** is a graph illustrating how FIGS. **8.0504**AA–EE are to be assembled. After such assembly, FIGS. **8.0504**AA–EE provide a circuit drawing of a VCO control voltage generator "dcr_vcocontrol" included in the circuit of FIGS. **8.05**AA–DE.

FIG. **8.050401** is a graph illustrating how FIGS. **8.050401**AA–CK are to be assembled. After such assembly, FIGS. **8.050401**AA–CK provide a circuit drawing of a coarse step generator "dcr_coarsestepgen" included in the circuit of FIGS. **8.0504**AA–EE.

FIG. **8.050402** is a graph illustrating how FIGS. **8.050402**AA–CJ are to be assembled. After such assembly, FIGS. **8.050402**AA–CJ provide a circuit drawing of a medium step generator "dcr_medstepgen" included in the circuit of FIGS. **8.0504**AA–EE.

FIG. **8.050403** is a graph illustrating how FIGS. **8.050403**AA–BI are to be assembled. After such assembly, FIGS. **8.050403**AA–BI provide a circuit drawing of a medium fine step generator "dcr_medfinestepgen" included in the circuit of FIGS. **8.0504**AA–EE.

FIG. **8.050404** is a graph illustrating how FIGS. **8.050404**AA–BB are to be assembled. After such assembly, FIGS. **8.050404**AA–BB provide a circuit drawing of a fine step controller "dcr_finestepctrl" included in the circuit of FIGS. **8.0504**AA–EE.

FIG. **8.050405** is a graph illustrating how FIGS. **8.050405**AA–EJ are to be assembled. After such assembly, FIGS. **8.050405**AA–EJ provide a circuit drawing of a fine step generator "dcr_finestepgen" included in the circuit of FIGS. **8.0504**AA–EE.

FIG. **8.0505** is a graph illustrating how FIGS. **8.0505**AA–EF are to be assembled. After such assembly, FIGS. **8.0505**AA–EF provide a circuit drawing of a receiver VCO "dcr_vco" included in the circuit of FIGS. **8.05**AA–DE.

FIG. **8.0506** is a graph illustrating how FIGS. **8.0506**AA–BB are to be assembled. After such assembly, FIGS. **8.0506**AA–BB provide a circuit drawing of an RX clock generator "dcr_rxclkgen" included in the circuit of FIGS. **8.05**AA–DE.

FIG. **8.050601** is a circuit drawing of an RX clock generator flip-flop "dcr_rxclkgenff" included in the circuit of FIGS. **8.0506**AA–BB.

FIG. **8.0507** is a graph illustrating how FIGS. **8.0507**AA–AB are to be assembled. After such assembly, FIGS. **8.0507**AA–AB provide a circuit drawing of a PLL non-overlapping clock generator "dcr_clkgen" included in the circuit of FIGS. **8.05**AA–DE.

FIG. **8.06** is a graph illustrating how FIGS. **8.06**AA–ED are to be assembled. After such assembly, FIGS. **8.06**AA–ED provide a circuit drawing of a BPSK/AM/Backscatter transmitter "tx" included in the circuit of FIGS. **8**AA–CB.

FIG. **8.0601** is a graph illustrating how FIGS. **8.0601**AA–BB are to be assembled. After such assembly, FIGS. **8.0601**AA–BB provide a circuit drawing of a transmitter PLL "txpllfsyn" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.060101** is a graph illustrating how FIGS. **8.060101**AA–CC are to be assembled. After such assembly, FIGS. **8.060101**AA–CC provide a circuit drawing of a TX phase/frequency detector "txpfdet" included in the circuit of FIGS. **8.0601**AA–BB.

FIG. **8.060102** is a graph illustrating how FIGS. **8.060102**AA–BB are to be assembled. After such assembly, FIGS. **8.060102**AA–BB provide a circuit drawing of a TX PLL charge pump "txchgpump" included in the circuit of FIGS. **8.0601**AA–BB.

FIG. **8.060103** is a graph illustrating how FIGS. **8.060103**AA–CB are to be assembled. After such assembly, FIGS. **8.060103**AA–CB provide a circuit drawing of a TX PLL loop filter "txloopfilter" included in the circuit of FIGS. **8.0601**AA–BB.

FIG. **8.060104** is a graph illustrating how FIGS. **8.060104**AA–DC are to be assembled. After such assembly, FIGS. **8.060104**AA–DC provide a circuit drawing of a TX VCO "txvco" included in the circuit of FIGS. **8.0601**AA–BB.

FIG. **8.06010401** is a graph illustrating how FIGS. **8.06010401**AA–BD are to be assembled. After such assembly, FIGS. **8.06010401**AA–BD provide a circuit drawing of a TX VCO stage "txvcostage" included in the circuit of FIGS. **8.060104**AA–DC.

FIG. **8.0601040101** is a graph illustrating how FIGS. **8.0601040101**AA–BC are to be assembled. After such assembly, FIGS. **8.0601040101**AA–BC provide a layout plot showing how the components of the VCO stage are laid out.

FIG. **8.060105** is a graph illustrating how FIGS. **8.060105**AA–DD are to be assembled. After such assembly, FIGS. **8.060105**AA–DD provide a circuit drawing of a divider "txdivider" included in the circuit of FIGS. **8.0601**AA–BB.

FIG. **8.06010501** is a graph illustrating how FIGS. **8.06010501**AA–AB are to be assembled. After such assembly, FIGS. **8.06010501**AA–AB provide a circuit drawing of a divider flip-flop "txdivtff" included in the circuit of FIGS. **8.060105**AA–DD.

FIG. **8.0602** is a graph illustrating how FIGS. **8.0602**AA–AB are to be assembled. After such assembly, FIGS. **8.0602**AA–AB provide a circuit drawing of a test mode data selector "txdatasel" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.0603** is a graph illustrating how FIGS. **8.0603**AA–AB are to be assembled. After such assembly, FIGS. **8.0603**AA–AB provide a circuit drawing of a BPSK modulation driver "txbpsk" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.0604** is a graph illustrating how FIGS. **8.0604**AA–AB are to be assembled. After such assembly, FIGS. **8.0604**AA–AB provide a circuit drawing of a frequency doubler "txdoubler" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.060401** is a graph illustrating how FIGS. **8.060401**AA–FE are to be assembled. After such assembly, FIGS. **8.060401**AA–FE provide a circuit drawing of a frequency doubler core "txfdbl" included in the circuit of FIGS. **8.0604**AA–ED.

FIG. **8.0605** is a graph illustrating how FIGS. **8.0605**AA–AB are to be assembled. After such assembly, FIGS. **8.0605**AA–AB provide a circuit drawing of a second frequency doubler "txdoubler**2**" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.060501** is a graph illustrating how FIGS. **8.060501**AA–CD are to be assembled. After such assembly, FIGS. **8.060501**AA–CD provide a circuit drawing of doubler driver amps "txfdbldrv" included in the circuit of FIGS. **8.0605**AA–CD.

FIG. **8.060502** is a graph illustrating how FIGS. **8.060502**AA–CD are to be assembled. After such assembly, FIGS. **8.060502**AA–CD provide a circuit drawing of second doubler driver amps "txfdbldrv**2**" included in the circuit of FIGS. **8.0605**AA–CD.

FIG. **8.060503** is a graph illustrating how FIGS. **8.060503**AA–FE are to be assembled. After such assembly, FIGS. **8.060503**AA–FE provide a circuit drawing of a frequency doubler core "txfdbl**2**" included in the circuit of FIGS. **8.0605**AA–CD.

FIG. **8.0606** is a graph illustrating how FIGS. **8.0606**AA–IE are to be assembled. After such assembly, FIGS.

8.0606AA–IE provide a circuit drawing of a transmitter power amp "txpoweramp" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.0607** is a graph illustrating how FIGS. **8.0607**AA–JJ are to be assembled. After such assembly, FIGS. **8.0607**AA–JJ provide a circuit drawing of a transmitter bias generator "txbias" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.0608** is a graph illustrating how FIGS. **8.0608**AA–BB are to be assembled. After such assembly, FIGS. **8.0608**AA–BB provide a circuit drawing of a modulated backscatter transmitter "txmbs" included in the circuit of FIGS. **8.06**AA–ED.

FIG. **8.07** is a graph illustrating how FIGS. **8.07**AA–BB are to be assembled. After such assembly, FIGS. **8.07**AA–BB provide a partial circuit drawing of a 915 MHZ transmitter "tx**915**" included in the circuit of FIGS. **8**AA–CB in place of the transmitter "tx" in an alternative embodiment of the invention.

FIG. **8.0701** is a graph illustrating how FIGS. **8.0701**AA–CB are to be assembled. After such assembly, FIGS. **8.0701**AA–CB provide a circuit drawing of a TX VCO stage "txvcostage**915**" for use with the 915 MHZ transmitter "tx**915**" of FIG. **8.07** in place of the TX VCO "txvco" of FIG. **8.060104**.

FIG. **9** is a graph illustrating how FIGS. **9**AA–CB are to be assembled. After such assembly, FIGS. **9**AA–CB provide a circuit drawing of an analog processor "anlgproc" included in the circuit of FIGS. **6**AA–EK.

FIG. **9.01** is a graph illustrating how FIGS. **9.01**AA–DH are to be assembled. After such assembly, FIGS. **9.01**AA–DH provide a circuit drawing of an algorithmic A/D converter with databus interface "ada new" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.0101** is a graph illustrating how FIGS. **9.0101**AA–CK are to be assembled. After such assembly, FIGS. **9.0101**AA–CK provide a circuit drawing of a differential I/O op-amp "dopamp" included in the circuit of FIGS. **9.01**AA–DH.

FIG. **9.0102** provides a circuit drawing of an analog divider (divide by two) "adaprescale" included in the circuit of FIGS. **9.01**AA–DH.

FIG. **9.0103** is a graph illustrating how FIGS. **9.0103**AJ–FP are to be assembled. After such assembly, FIGS. **9.0103**AJ–FP provide a circuit drawing of a control PLA "adactl_new" included in the circuit of FIGS. **9.01**AA–DH.

FIG. **9.010301** is a graph illustrating how FIGS. **9.010301**AA–CC are to be assembled. After such assembly, FIGS. **9.010301**AA–CC provide a circuit drawing of a clock generator "adacgen_new" included in the circuit of FIGS. **9.0103**AJ–FP.

FIG. **9.010302** is a graph illustrating how FIGS. **9.010302**AA–AB are to be assembled. After such assembly, FIGS. **9.010302**AA–AB provide a circuit drawing of a control output driver "adacdrv_new" included in the circuit of FIGS. **9.0103**AJ–FP.

FIG. **9.010303** is a graph illustrating how FIGS. **9.010303**AA–AB are to be assembled. After such assembly, FIGS. **9.010303**AA–AB provide a circuit drawing of a control output driver "adacdrvn_new" included in the circuit of FIGS. **9.0103**AJ–FP.

FIG. **9.010304** is a graph illustrating how FIGS. **9.010304**AA–BB are to be assembled. After such assembly, FIGS. **9.010304**AA–BB provide a circuit drawing of a data latch "adadlat_new" included in the circuit of FIGS. **9.0103**AJ–FP.

FIG. **9.0104** is a graph illustrating how FIGS. **9.0104**AA–DD are to be assembled. After such assembly, FIGS. **9.0104**AA–DD provide a circuit drawing of an analog bias circuit "adabias_new" included in the circuit of FIGS. **9.01**AA–DH.

FIG. **9.02** is a graph illustrating how FIGS. **9.02**AA–DK are to be assembled. After such assembly, FIGS. **9.02**AA–DK provide a circuit drawing of a Vdd power up detector "pup" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.03** is a graph illustrating how FIGS. **9.03**AA–BB are to be assembled. After such assembly, FIGS. **9.03**AA–BB provide a circuit drawing of a master bias source "mbs" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.0301** is a graph illustrating how FIGS. **9.0301**AA–DJ are to be assembled. After such assembly, FIGS. **9.0301**AA–DJ provide a circuit drawing of a band gap reference generator "mbs_bgr" included in the circuit of FIGS. **9.03**AA–BB.

FIG. **9.0302** is a graph illustrating how FIGS. **9.0302**AA–DI are to be assembled. After such assembly, FIGS. **9.0302**AA–DI provide a circuit drawing of a temperature compensated current generator "mbs_cur" included in the circuit of FIGS. **9.03**AA–BB.

FIG. **9.0303** is a graph illustrating how FIGS. **9.0303**AA–CF are to be assembled. After such assembly, FIGS. **9.0303**AA–CF provide a circuit drawing of a reference current generator "mbs_iref" included in the circuit of FIGS. **9.03**AA–BB.

FIG. **9.04** is a graph illustrating how FIGS. **9.04**AA–CE are to be assembled. After such assembly, FIGS. **9.04**AA–CE provide a circuit drawing of a voltage regulator "vrg" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.05** is a graph illustrating how FIGS. **9.05**AA–FE are to be assembled. After such assembly, FIGS. **9.05**AA–FE provide a circuit drawing of a voltage regulator "vrgtx" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.0501** is a graph illustrating how FIGS. **9.0501**AA–CD are to be assembled. After such assembly, FIGS. **9.0501**AA–CD provide a circuit drawing of an operational amplifier without compensation "opampnc" included in the circuit of FIGS. **9.05**AA–FE.

FIG. **9.06** is a graph illustrating how FIGS. **9.06**AA–DD are to be assembled. After such assembly, FIGS. **9.06**AA–DD provide a circuit drawing of a bias OK detector "biasok" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.07** is a graph illustrating how FIGS. **9.07**AA–EG are to be assembled. After such assembly, FIGS. **9.07**AA–EG provide a circuit drawing of an analog port current source "aportcs" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.08** is a graph illustrating how FIGS. **9.08**AA–CC are to be assembled. After such assembly, FIGS. **9.08**AA–CC provide a circuit drawing of an analog multiplexer decoder "asl" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.09** is a graph illustrating how FIGS. **9.09**AA–BB are to be assembled. After such assembly, FIGS. **9.09**AA–BB provide a circuit drawing of a random clock generator "rcg" included in the circuit of FIGS. **9**AA–CB.

FIG. **9.0901** is a graph illustrating how FIGS. **9.0901**AA–CH are to be assembled. After such assembly, FIGS. **9.0901**AA–CH provide a circuit drawing of a linear feedback shift register "rcg_sreg" included in the circuit of FIGS. **9.09**AA–CB.

FIG. **9.090101** is a graph illustrating how FIGS. **9.090101**AA–CC are to be assembled. After such assembly, FIGS. **9.090101**AA–CC provide a circuit drawing of a shift register bit "rcg sregbit**0**" included in the circuit of FIGS. **9.0901**AA–CH.

FIG. **9.090102** is a graph illustrating how FIGS. **9.090102**AA–BB are to be assembled. After such assembly, FIGS. **9.090102**AA–BB provide a circuit drawing of a shift register bit "rcg_sregbit" included in the circuit of FIGS. **9.0901**AA–CH.

FIG. **9.0902** is a graph illustrating how FIGS. **9.0902**AA–FL are to be assembled. After such assembly, FIGS. **9.0902**AA–FL provide a circuit drawing of a low power oscillator and bias generator "rcg_osc" included in the circuit of FIGS. **9.09**AA–CB.

FIG. **9.0903** is a graph illustrating how FIGS. **9.0903**AA–CC are to be assembled. After such assembly, FIGS. **9.0903**AA–CC provide a circuit drawing of a clock generator "rcg_clkgen" included in the circuit of FIGS. **9.09**AA–CB.

FIG. **10** is a graph illustrating how FIGS. **10**AA–DD are to be assembled. After such assembly, FIGS. **10**AA–DD provide a circuit drawing of a pn processor "pnproc" included in the circuit of FIGS. **6**AA–EK.

FIG. **10.01** is a graph illustrating how FIGS. **10.01**AA–DI are to be assembled. After such assembly, FIGS. **10.01**AA–DI provide a circuit drawing of a digital PN correlator "dcorr" included in the circuit of FIGS. **10**AA–DI.

FIG. **10.0101** is a graph illustrating how FIGS. **10.0101**AA–BG are to be assembled. After such assembly, FIGS. **10.0101**AA–BG provide a circuit drawing of a PN correlator shift register "dcorr_sreg" included in the circuit of FIGS. **10.01**AA–DI.

FIG. **10.010101** is a circuit drawing of a PN correlator bit "dcorr_bit" included in the circuit of FIGS. **10.0101**AA–BG.

FIG. **10.01010101** is a circuit drawing of a shift register cell "dcorr_sregbit" included in the circuit of FIG. **10.010101**.

FIG. **10.0102** is a graph illustrating how FIGS. **10.0102**AA–CN are to be assembled. After such assembly, FIGS. **10.0102**AA–CN provide a circuit drawing of a correlator bias generator "dcorr_bias" included in the circuit of FIGS. **10.01**AA–DI.

FIG. **10.02** is a graph illustrating how FIGS. **10.02**AA–BE are to be assembled. After such assembly, FIGS. **10.02**AA–BE provide a circuit drawing of a PN lock detector "pnlockdet" included in the circuit of FIGS. **10**AA–DD.

FIG. **10.0201** is a graph illustrating how FIGS. **10.0201**AA–AB are to be assembled. After such assembly, FIGS. **10.0201**AA–AB provide a circuit drawing of a counter bit "lockcounterbit" included in the circuit of FIGS. **10.02**AA–BE.

FIG. **10.03** is a graph illustrating how FIGS. **10.03**AA–AB are to be assembled. After such assembly,

FIGS. **10.03**AA–AB provide a circuit drawing of a PN generator clock "pngclk" included in the circuit of FIGS. **10**AA–DD.

FIG. **10.04** is a graph illustrating how FIGS. **10.04**AA–CE are to be assembled. After such assembly, FIGS. **10.04**AA–CE provide a circuit drawing of a PN generator shift register "pngshr" included in the circuit of FIGS. **10**AA–DD.

FIG. **10.0401** is a circuit drawing of a PN generator shift register cell "pngsreg" included in the circuit of FIGS. **10.04**AA–CE.

FIG. **10.0402** is a graph illustrating how FIGS. **10.0402**AA–CB are to be assembled. After such assembly, FIGS. **10.0402**AA–CB provide a circuit drawing of a PN generator shift register summer "pngssum" included in the circuit of FIGS. **10.04**AA–CE.

FIG. **10.05** is a circuit drawing of a PN controller D type flip-flop "pnddff" included in the circuit of FIGS. **10**AA–DD.

FIG. **10.06** is a graph illustrating how FIGS. **10.06**AA–DH are to be assembled. After such assembly, FIGS. **10.06**AA–DH provide a circuit drawing of differential and PN encoder "dpenc" included in the circuit of FIGS. **10**AA–DD.

FIG. **10.07** is a graph illustrating how FIGS. **10.07**AA–CD are to be assembled. After such assembly, FIGS. **10.07**AA–CD provide a circuit drawing of a PSK/FSK generator "fskgen" included in the circuit of FIGS. **10**AA–DD.

FIG. **10.0701** is a graph illustrating how FIGS. **10.0701**AA–AB are to be assembled. After such assembly, FIGS. **10.0701**AA–AB provide a circuit drawing of a FSK counter bit "fskcbit" included in the circuit of FIGS. **10**AA–DD.

FIG. **11** is a graph illustrating how FIGS. **11**AA–AB are to be assembled. After such assembly, FIGS. **11**AA–AB provide a circuit drawing of a battery I/O buffer "batalg" included in the circuit of FIGS. **6**AA–EK.

FIG. **12** is a graph illustrating how FIGS. **12**AA–AB are to be assembled. After such assembly, FIGS. **12**AA–AB provide a circuit drawing of a digital I/O pad buffer "paddig" included in the circuit of FIGS. **6**AA–EK.

FIG. **13** is a circuit drawing of a digital input pad buffer "paddigin" included in the circuit of FIGS. **6**AA–EK.

FIG. **13.5** is a circuit drawing of a digital input pad buffer "paddigin**2**" included in the circuit of FIGS. **6**AA–EK.

FIG. **14** is a circuit drawing of an analog I/O pad buffer "padalg" included in the circuit of FIGS. **6**AA–EK.

FIG. **15** is a graph illustrating how FIGS. **15**AA–BC are to be assembled. After such assembly, FIGS. **15**AA–BC provide a circuit drawing of return link configuration control logic "rlconfig" included in the circuit of FIGS. **6**AA–EK.

FIG. **16** is a graph illustrating how FIGS. **16**AA–EH are to be assembled. After such assembly, FIGS. **16**AA–EH provide a circuit drawing of a temperature sensor "tsn" included in the circuit of FIGS. **6**AA–EK.

FIG. **16.01** is a graph illustrating how FIGS. **16.01**AA–DI are to be assembled. After such assembly, FIGS. **16.01**AA–DI provide a circuit drawing of an operational amplifier "opamp" included in the circuit of FIGS. **16**AA–EH.

FIG. **17** is a graph illustrating how FIGS. **17**AA–BB are to be assembled. After such assembly, FIGS. **17**AA–BB provide a circuit drawing of a magnetic field sensor "mag" (a sensor for sensing magnetic fields) included in the circuit of FIGS. **6**AA–EK.

FIG. **18** is a graph illustrating how FIGS. **18**AA–AB are to be assembled. After such assembly, FIGS. **18**AA–AB provide a circuit drawing of a chip bypass capacitor "bypcap**3**" included in the circuit of FIGS. **6**AA–EK.

FIG. **19** is a graph illustrating how FIGS. **19**AA–EK are to be assembled. After such assembly, FIGS. **19**AA–EK provide a circuit drawing of a monolithic semiconductor integrated circuit "LO**3**BT**3**F" in accordance with an alternative embodiment of the invention. The integrated circuit of FIGS. **19**AA–EK is similar to the integrated circuit shown in FIGS. **6**AA–EK, like component names indicating like components, except that the integrated circuit of FIGS. **19**AA–EK has no ROM, and is adapted to be connected to external ROM "extrom". The embodiment of FIGS. **19**AA–EK is particularly useful for test purposes.

FIG. **20** is a graph illustrating how FIGS. **20**AA–DF are to be assembled. After such assembly, FIGS. **20**AA–DF provide a circuit drawing of a data processor "dataproc_t**3**" to be used in the integrated circuit of FIG. **19** in place of the data processor "dataproc" of FIG. **7**.

FIG. **20.01** is a graph illustrating how FIGS. **20.01**AA–CB are to be assembled. After such assembly, FIGS. **20.01**AA–CB provide a circuit drawing of an external ROM "extrom" shown in FIGS. **20**AA–CB.

FIG. **20.0101** is a graph illustrating how FIGS. **20.0111**AA–BB are to be assembled. After such assembly, FIGS. **20.0101**AA–BB provide a circuit drawing of external ROM control logic "extromctl" included in the circuit of FIGS. **20.01**AA–CB.

FIG. **20.0102** is a circuit drawing of an external ROM address interface "extromad" included in the circuit of FIGS. **20.01**AA–CB.

FIG. **20.0103** is a graph illustrating how FIGS. **20.0103**AA–AC are to be assembled. After such assembly, FIGS. **20.0103**AA–AC provide a circuit drawing of a digital I/O pad buffer "paddigt**3**" included in the circuit of FIGS. **20.01**AA–CB.

FIG. **20.0104** is a circuit drawing of an external ROM databus interface "extromdb" included in the circuit of FIGS. **20.01**AA–CB.

FIG. **21** is a circuit schematic illustrating a transmitter switchable between an active mode and a backscatter mode, and employing separate antennas for the active mode and the backscatter mode.

FIG. **22** is a circuit schematic illustrating a transmitter switchable between an active mode and a backscatter mode, and employing the same antenna for both the active mode and the backscatter mode.

FIG. **23** is a circuit schematic illustrating low battery detection circuitry.

FIG. **24** is a circuit schematic illustrating circuitry providing a low power wake up timer.

FIGS. **25–26** provide a flowchart illustrating logic employed for switching between a low power sleep mode, and higher power modes.

FIG. **27** is a diagram of current versus time illustrating switching between a low power sleep mode, and higher power modes.

FIG. **28** is a circuit schematic illustrating a Schottky diode detector.

FIG. **29** is a circuit schematic illustrating a Schottky diode detector in accordance with one embodiment of the invention.

FIG. **30** is a circuit schematic illustrating a Schottky diode detector in accordance with another embodiment of the invention.

FIG. **31** is a waveform diagram illustrating the effect of high power radio frequency input levels on Schottky detectors.

FIG. **32** is a circuit schematic illustrating a high frequency voltage controlled oscillator differential stage.

FIG. **33** is a waveform diagram illustrating the effect of errors in frequency doubler circuits that necessitates correction, such as by using an integrator and feedback.

FIG. **34** is a circuit schematic illustrating a frequency doubler circuit that employs an integrator and feedback to solve the problem illustrated in FIG. **33**.

FIG. **35** is a waveform diagram illustrating input and output waves created and employed by a frequency doubler circuit such as the one shown in FIG. **34**.

FIG. **36** is a circuit schematic illustrating a symmetric frequency doubler circuit that does not require an integrator and feedback to solve the problem illustrated in FIG. **33**. The frequency doubler circuit of FIG. **36** creates and employs waveforms such as those shown in FIG. **35**.

FIG. **37** is a circuit schematic of an inverter illustrating a power saving technique employed in a pseudo random number generator embodying one aspect of the invention.

FIG. **38** is a cross-sectional view illustrating a step of a process of manufacturing a Schottky diode.

FIG. **39** is a cross-sectional view illustrating a step subsequent to the step of FIG. **38**.

FIG. **40** is a cross-sectional view illustrating a step subsequent to the step of FIG. **39**.

FIG. **41** is a cross-sectional view illustrating a step subsequent to the step of FIG. **40**.

FIG. **42** is a top view illustrating a step subsequent to the step of FIG. **41** and showing parallel connection of some Schottky diodes of a plurality of Schottky diodes.

FIG. **43** is a top view illustrating a step subsequent to the step of FIG. **41** in accordance with an alternative embodiment of the invention and showing parallel connection of all Schottky diodes of a plurality of Schottky diodes.

FIG. **44** is a cross-sectional view illustrating a step of an alternative process of manufacturing a Schottky diode.

FIG. **45** is a cross-sectional view illustrating a step subsequent to the step of FIG. **44**.

FIG. **46** is a cross-sectional view illustrating a step subsequent to the step of FIG. **45**.

FIG. **47** is a cross-sectional view illustrating a step subsequent to the step of FIG. **46**.

FIG. **48** is a simplified circuit schematic of a quick bias AC-coupled video amplifier included in the integrated circuit.

FIG. **49** is a plot of voltage versus angular frequency illustrating selection of components to realize a desired high pass roll off frequency in the amplifier of FIG. **48**.

FIG. **50** is a simplified circuit schematic illustrating sharing of a single antenna by both a Schottky detector and an active transmitter.

FIG. **51** is a simplified circuit schematic illustrating circuitry included in the active transmitter of FIG. **50** in accordance with one aspect of the invention.

FIG. **52** is a simplified circuit schematic illustrating sharing of a single antenna by both a Schottky detector and a backscatter transmitter.

FIG. **53** is a simplified circuit schematic illustrating sharing of a single antenna by both a Schottky detector and a backscatter transmitter in accordance with an alternative embodiment of the invention.

FIG. **54** is a graph of voltage versus time illustrating a method of determining when frequency lock has occurred.

FIG. **55** is a flowchart illustrating a top level of code stored in ROM in the integrated circuit.

FIGS. **56**A and B define a flowchart illustrating a command processing routine performed by the integrated circuit.

FIGS. **57**A and B define a flowchart illustrating steps performed by the integrated circuit in response to an Identify command received from the interrogator in which the interrogator requests, via radio frequency command, identification of an integrated circuit.

FIG. **58** is a flowchart illustrating steps performed to initialize the interrogator.

FIG. **59** is a flowchart illustrating steps performed when the interrogator sends a command to the integrated circuit.

FIG. **60** is a flowchart illustrating steps performed by the interrogator in issuing an Identify command.

FIG. **61** is a simplified circuit diagram of a digital clock recovery loop including a start-up circuit including a counter, a voltage controlled oscillator, a charge pump and loop filter, and a state machine. The start-up circuit and counter determine when clock frequency is close to a desired value.

FIG. **62** is a plot of frequency produced by a voltage controlled oscillator versus control voltage applied to the voltage controlled oscillator.

FIG. **63** is a timing diagram showing when the start-up circuit of FIG. **61** issues pump up signals to increase the control voltage applied to the voltage controlled oscillator.

FIG. **64** is a state diagram illustrating the design of the state machine of FIG. **61**.

FIGS. **65–70** illustrate steps used in designing a state machine that implements the state diagram of FIG. **64**. FIG. **65** illustrates flip-flops having outputs representing in binary form the various states of the state diagrams and having inputs representing next state values. FIG. **66** is a state table. FIGS. **67** and **68** are Karnaugh maps used to derive minimum logic circuitry needed to derive circuit output functions and flip-flop input functions.

FIG. **71** is a simplified timing diagram illustrating operation of the state machine.

FIG. **72** is a table illustrating step sizes produced by the start-up circuit and the state machine.

SUMMARY OF THE INVENTION

The invention provides a radio frequency identification device comprising an integrated circuit including a receiver, a transmitter, and a microprocessor. The integrated circuit is preferably a monolithic single die integrated circuit including the receiver, the transmitter, and the microprocessor. Because the device includes an active transponder, instead of a transponder which relies on magnetic coupling for power, the device has a much greater range.

One aspect of the invention provides a radio frequency identification device comprising a monolithic integrated circuit including a receiver, a transmitter which can operate at frequencies above 400 MHz, and a microprocessor.

Another aspect of the invention provides a radio frequency identification device comprising a monolithic integrated circuit including a receiver, a transmitter which can operate at frequencies above 1 GHz, and a microprocessor.

Another aspect of the invention provides a radio frequency identification device comprising a monolithic integrated circuit including a transmitter, a microprocessor, and a receiver which can receive and interpret signals having frequencies above 400 MHz.

Another aspect of the invention provides a radio frequency identification device comprising a monolithic integrated circuit including a transmitter, a microprocessor, and a receiver which can receive and interpret signals having frequencies above 1 Ghz.

Another aspect of the invention provides a radio frequency identification device comprising a monolithic integrated circuit including a receiver, a microwave transmitter, and a microprocessor.

Another aspect of the invention provides a radio frequency identification device comprising a monolithic integrated circuit including a microwave receiver, a transmitter, and a microprocessor.

Another aspect of the invention provides a radio frequency identification device comprising a single die including a receiver, a transmitter, and a microprocessor, the die having a size less than 90,000 $mils^2$. In accordance with a more preferred embodiment of the invention, the die has a size less than 300×300 $mils^2$. In accordance with a more preferred embodiment of the invention, the die has a size less than 37,500 $mils^2$. In accordance with a more preferred embodiment of the invention, the die has a size of 209 by 116 $mils^2$.

Another aspect of the invention provides a radio frequency identification device comprising a single die integrated circuit including a receiver, a transmitter, and a microprocessor.

Another aspect of the invention provides a radio frequency identification device comprising a single die with a single metal layer including a receiver, a transmitter, and a microprocessor.

Another aspect of the invention provides a radio frequency identification device comprising a single die integrated circuit including a receiver, a transmitter, and a microprocessor formed using a single metal layer processing method.

Another aspect of the invention provides a radio frequency identification system comprising an integrated circuit including a receiver, and a transmitter; and an antenna coupled to the integrated circuit, the integrated circuit being responsive to radio frequency signals of multiple carrier frequencies.

Another aspect of the invention provides a radio frequency identification device comprising transponder circuitry formed in a monolithic integrated circuit comprising both transmitting and receiving circuits of the transponder circuitry; a power supply operably associated with the transponder circuitry; and an antenna operably associated with the transponder circuitry.

Another aspect of the invention provides a radio frequency identification device comprising a monolithic semiconductor integrated circuit including a receiver and a transmitter; means for applying a supply of power to the integrated circuit device from a battery; and means for configuring the integrated circuit to receive and transmit radio frequency signals.

Another aspect of the invention provides a method for producing a radio frequency identification device, the method comprising the following steps: providing a monolithic integrated circuit having a receiver and a transmitter; and providing a package configured to carry the integrated circuit.

Another aspect of the invention provides a method for adapting a radio frequency data communication device for use at a desired carrier frequency for use in a radio frequency identification (RFID) device, the method comprising the following steps: providing an integrated circuit having tunable circuitry, the integrated circuit comprising a receiver and a transmitter; configuring the integrated circuit for connection with a power supply to enable operation; configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation there between; and tuning the tunable circuitry and the antenna to realize a desired carrier frequency from a wide range of possible carrier frequencies. A method for adapting a radio frequency data communication device for use at a desired carrier frequency for use in a radio frequency identification device, the method comprising the following steps: providing an integrated circuit having tunable circuitry, the integrated circuit comprising a receiver and a transmitter; configuring the integrated circuit for connection with a power supply to enable operation; configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation there between; and tuning the antenna to realize a desired carrier frequency from a wide range of possible carrier frequencies.

Another aspect of the invention provides a radio frequency communications device comprising an integrated circuit including a transmitter and a receiver, the integrated circuit including a clock recovery circuit recovering a clock frequency from a signal received by the receiver, the clock recovery circuit having a phase lock loop including a voltage controlled oscillator, and a loop filter having a capacitor storing a voltage indicative of a frequency at which the voltage controlled oscillator is oscillating, the integrated circuit using the voltage stored on the capacitor to generate a clock frequency for the transmitter.

Another aspect of the invention provides a method of recovering a clock frequency from a received radio frequency signal, storing the clock frequency, and using the clock frequency for radio frequency transmission by a transmitter, the method comprising: providing a clock recovery circuit recovering a clock frequency from a signal received by the receiver, the clock recovery circuit having a phase lock loop including a voltage controlled oscillator, and a loop filter having a capacitor; using the clock recovery circuit to recover a clock frequency from a received radio frequency signal; storing on the capacitor a voltage indicative of frequency at which the voltage controlled oscillator is oscillating; using the voltage stored on the capacitor to generate a clock frequency for use by the transmitter.

Another aspect of the invention provides a method of recovering and storing a clock frequency from a received radio frequency signal in a radio frequency identification device including a transmitter and a receiver, the method comprising providing a clock recovery circuit recovering a clock frequency from a signal received by the receiver, the clock recovery circuit having a phase lock loop; using the clock recovery circuit to recover a clock frequency from a received radio frequency signal; storing in analog form a value indicative of frequency at which the voltage controlled oscillator is oscillating; and using the analog value to generate a clock frequency for use by the transmitter.

Another aspect of the invention provides a radio frequency communications device comprising an integrated circuit including a transmitter and a receiver, the transmitter being switchable between a backscatter mode, wherein a

carrier for the transmitter is derived from a carrier received from an interrogator spaced apart from the radio frequency communications device, and an active mode, wherein a carrier for the transmitter is generated by the integrated circuit itself.

Another aspect of the invention provides a radio frequency communications device comprising an integrated circuit including a transmitter and a receiver, the transmitter selectively transmitting a signal using a modulation scheme, the transmitter being switchable for transmission using different modulation schemes.

Another aspect of the invention provides a method for adapting modulation schemes of a radio frequency data communication device in a radio frequency identification device, the method comprising the following steps: providing an integrated circuit having switching circuitry, a receiver, a transmitter, and a processor; the integrated circuit having a plurality of transmitting circuits including a first transmitting circuit configured to realize an active transmitter scheme and a second transmitting circuit configured to realize a modulated backscatter scheme; configuring the integrated circuit for connection with a power supply to enable operation; configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation; and switching the switchable circuitry with respect to the antenna to enable one of the transmitting circuits to realize one of the modulation schemes.

Another aspect of the invention provides a method for adapting modulation schemes of a radio frequency data communication device in a radio frequency identification device, the method comprising the following steps: providing an integrated circuit having switching circuitry, a receiver, a transmitter, and a processor, the integrated circuit including a plurality of transmitting circuits, the plurality of transmitting circuits configured to selectively realize a plurality of modulated backscatter schemes; configuring the integrated circuit for connection with a power supply to enable operation; configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation; and switching the transmitting circuits with respect to the antenna to enable one of the transmitting circuits to realize one of the modulation schemes.

Another aspect of the invention provides a radio frequency identification device comprising: an integrated circuit including a transmitter and a receiver, the integrated circuit being adapted to be connected to a battery, and further including a comparator comparing the voltage of the battery with a predetermined voltage and generating a low battery signal if the voltage of the battery is less than the predetermined voltage.

Another aspect of the invention provides a method for detecting a low battery condition in a radio frequency data communication device for use in a radio frequency identification device, the method comprising the following steps: providing an integrated circuit having switching circuitry, a receiver, and a transmitter, the integrated circuit including a comparator configured to compare the battery voltage with a predetermined voltage and generate a low battery signal if the battery voltage is less than the predetermined voltage; configuring the integrated circuit for connection with the battery to enable operation; configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation there between; determining a predetermined voltage for the battery; comparing the voltage of the battery with the predetermined voltage; and generating a low battery signal if the voltage of the battery is less than the predetermined voltage.

Another aspect of the invention provides a radio frequency communications device comprising an integrated circuit including a transmitter and a receiver, the integrated circuit periodically checking if a radio frequency signal is being received by the receiver, the integrated circuit further including a timer setting a time period for the checking, the timer having a frequency lock loop.

Another aspect of the invention provides a radio frequency communications device comprising an integrated circuit including a transmitter and a receiver, the integrated circuit being configured to periodically check if a radio frequency signal is being received by the receiver, the integrated circuit further including a timer setting a time period for the checking, the timer having a phase lock loop.

Another aspect of the invention provides a method for calibrating a clock in a radio frequency data communication device for use in a radio frequency identification device, the method comprising the following steps: providing an integrated circuit having a receiver and a transmitter, the integrated circuit including a timer having a frequency lock loop configured to set a time period for periodically checking if a radio frequency signal is being received by the receiver; configuring the integrated circuit for connection with a battery to enable operation; configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation therebetween; and periodically checking whether a radio frequency signal is being received by the receiver.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein commands are received via the connection pin.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a digital input pin, the integrated circuit being switchable between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein commands are received digitally via the digital input pin.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein a modulation signal without a carrier is received via the connection pin.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an

integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein responses are transmitted via the connection pin.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a digital output pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein responses are transmitted digitally via the digital output pin.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein a modulation signal without a carrier is transmitted via the connection pin.

Another aspect of the invention provides a method comprising the following steps: providing an integrated circuit having a receiver, a transmitter, and a connection pin, the integrated circuit including a switchable circuit configured to switch between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein commands are received via the connection pin; configuring the integrated circuit for connection with a battery; configuring the integrated circuit to receive and transmit radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation; and switching to one of the radio frequency receive mode and the direct receive mode to enable receipt of radio frequency commands or commands received via the connection pin. Another aspect of the invention provides a method comprising the following steps: providing an integrated circuit having a receiver, a transmitter, and a connection pin, the integrated circuit including a switchable circuit configured to switch between a radio frequency transmit mode wherein the transmitter transmits information via radio frequency, and a direct transmit mode wherein data is transmitted via the connection pin; configuring the integrated circuit for connection with a battery; configuring the integrated circuit to receive and transmit radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation; and switching to one of the radio frequency transmit mode and the direct transmit mode to enable transmission of information via radio frequency or via the connection pin.

Another aspect of the invention provides an integrated circuit comprising a radio frequency receiver; a unique, non-alterable indicia identifying the integrated circuit; and a radio frequency transmitter configured to transmit a signal representative of the indicia in response to a command received by the receiver.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a receiver for receiving radio frequency commands from an interrogation device, and a transmitter for transmitting a signal identifying the device to the interrogator, the transmitter and receiver being formed on a die having a lot number, wafer number, and die number, the integrated circuit including non-alterable indicia identifying the lot number, wafer number, and die number, the transmitter being configured to transmit the non-alterable indicia in response to a manufacturer's command received by the receiver, the transmitted non-alterable indicia being different from the identifying signal.

Another aspect of the invention provides a method of tracing manufacturing process problems by tracing the origin of a defective radio frequency identification integrated circuit, the method comprising: forming a non-alterable indicia on a die for the integrated circuit, the indicia representing the wafer lot number, wafer number, and die number on the wafer, the indicia being not readily ascertainable by a user; and causing the integrated circuit to transmit the non-alterable indicia via radio frequency in response to a manufacturer's command.

Another aspect of the invention provides a method of tracing stolen property including a radio frequency identification integrated circuit, the method comprising: forming a non-alterable indicia on a die for the integrated circuit, the indicia representing the wafer lot number, wafer number, and die number on the wafer, the indicia being not readily ascertainable by a user; and causing the integrated circuit to transmit the non-alterable indicia via radio frequency in response to a manufacturer's command.

Another aspect of the invention provides a method of tracing manufacturing process problems in the manufacture of a radio frequency integrated circuit by tracing defect origin, the method comprising the following steps: providing a detectable signature on the integrated circuit, the signature indicative of one or more of the wafer lot number, wafer number, and die number of a die for the integrated circuit; and enabling the integrated circuit to transmit the signature via radio frequency responsive to an inquiry command.

Another aspect of the invention provides a radio frequency identification device comprising: an integrated circuit including a microprocessor, a receiver receiving radio frequency commands from an interrogation device, and a transmitter transmitting a signal identifying the device to the interrogator, the integrated circuit switching between a sleep mode, and a microprocessor on mode, in which more power is consumed than in the sleep mode, if the microprocessor determines that a signal received by the receiver is a radio frequency command from an interrogation device.

Another aspect of the invention provides a method for conserving power during operation of a radio frequency identification device, the method comprising the following steps: providing a receiver, a transmitter, microprocessor, and wake-up circuitry, the wake-up circuitry configured to selectively supply clock signals to the processor and thus control power consumption of the processor; configuring the receiver with an antenna to receive radio frequency signals from an interrogation device; configuring the transmitter to transmit a signal identifying the device to the interrogator; selectively enabling powered wake-up of the receiver to periodically check for presence of radio frequency signals; detecting whether a radio frequency signal is valid; and depending on whether a radio frequency signal is valid, supplying clock signals to the processor.

Another aspect of the invention provides a method for conserving power during operation of a radio frequency identification device, the method comprising the following steps: providing a receiver, a transmitter, microprocessor,

and wake-up circuitry, the wake-up circuitry configured to selectively supply power to the processor; configuring the receiver with an antenna to receive radio frequency signals from an interrogation device; configuring the transmitter to transmit a signal identifying the device to the interrogator; selectively enabling powered wake-up of the receiver to periodically check for presence of radio frequency signals; detecting whether a radio frequency signal is valid; and depending on whether a radio frequency signal is valid, supplying power signals to the processor.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit being switchable between a sleep mode, and a microprocessor on mode in which more power is consumed than in the sleep mode, the integrated circuit being switched from the sleep mode to the microprocessor on mode in response to a direct sequence spread spectrum modulated radio frequency signal, which has a predetermined number of transitions within a certain period of time, being received by the receiver.

Another aspect of the invention provides a method for conserving power in a radio frequency identification device, the method comprising periodically switching from a sleep mode to a receiver on mode and performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present: (a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode; and (b) determining if the radio frequency signal has a predetermined number of transitions per a predetermined time period of time and, if so, switching to the microprocessor on mode; and, if not, returning to the sleep mode.

Another aspect of the invention provides a radio frequency identification device switchable between a sleep mode and a mode in which more power is consumed than in the sleep mode, the radio frequency identification device comprising a transponder including a receiver and a transmitter; means for periodically checking whether any radio frequency signal is being received by the receiver; and means for determining if a radio frequency signal has a predetermined number of transitions within a predetermined period of time.

Another aspect of the invention provides a method for conserving power in a radio frequency identification device, the method comprising periodically switching from a sleep mode to a receiver on mode and performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present: (a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode; (b) determining if the radio frequency signal is modulated and has a predetermined number of transitions per a predetermined period of time and, if so, proceeding to step (c); and, if not, returning to the sleep mode; and (c) determining if the modulated radio frequency signal has a predetermined number of transitions per a predetermined period of time different from the predetermined time of step (b) and, if so, switching to the microprocessor on mode; and, if not, returning to the sleep mode.

Another aspect of the invention provides a method of forming an integrated circuit including a Schottky diode, the method comprising: providing a p-type substrate; defining an n-type region relative to the substrate; forming an insulator over the n-type region; removing an area of the insulator for definition of a contact hole, and removing an area encircling the contact hole; forming n+regions in the n-type regions encircling the contact hole; depositing a Schottky metal in the contact hole; and annealing the metal to form a silicide interface to the n-type region.

Another aspect of the invention provides a method of forming an integrated circuit including a Schottky diode, the method comprising: providing a substrate; defining a p-type region relative to the substrate; forming an insulator over the p-type region; removing an area of the insulator for definition of a contact hole, and removing an area encircling the contact hole; forming p+regions in the p-type regions encircling the contact hole; depositing a Schottky metal in the contact hole; and annealing the Schottky metal to form a silicide interface to the p-type region.

Another aspect of the invention provides a method of forming an integrated circuit including a Schottky diode, the method comprising: providing a p-type substrate; defining an n-well region relative to the substrate; forming a BPSG insulator over the n-well region; etching away an area of the BPSG for definition of a contact hole, and etching an area encircling the contact hole; forming n+regions in the n-well regions encircling the contact hole; depositing titanium in the contact hole; and annealing the titanium to form a silicide interface to the n-well region.

Another aspect of the invention provides a method of forming an integrated circuit including a Schottky diode, the method comprising: providing an n-type substrate; defining a p-well region relative to the substrate; forming a BPSG insulator over the p-well region; etching away an area of the BPSG for definition of a contact hole, and etching an area encircling the contact hole;

forming p+regions in the p-well regions encircling the contact hole; depositing titanium in the contact hole; and annealing the titanium to form a silicide interface to the p-well region.

Another aspect of the invention provides a radio frequency communications system comprising an antenna; an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode coupled to the antenna; and a current source connected to drive current through the antenna and the Schottky diode.

Another aspect of the invention provides an integrated circuit for radio frequency communications comprising an inductorless radio frequency detector.

Another aspect of the invention provides a system comprising an antenna; a transponder including a receiver having a Schottky diode detector including a Schottky diode having a first terminal coupled to the antenna and having a second terminal; and means for driving current through both the antenna and the Schottky diode in a direction from the first terminal to the second terminal.

Another aspect of the invention provides a system comprising an antenna; a transponder including a receiver having a Schottky diode detector including a Schottky diode having a first terminal coupled to the antenna and having a second terminal; and means for driving current through both the antenna and the Schottky diode in a direction from the second terminal to the first terminal. Another aspect of the invention provides a system comprising an antenna; a transponder including a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode; and means for driving current through both the antenna and the Schottky diode in a direction from the anode to the cathode.

Another aspect of the invention provides a radio frequency communications system comprising: an antenna; an

integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode, the Schottky diode detector further including a capacitor connected between the cathode and ground, and including a capacitor having a first contact connected to the cathode and having a second contact defining an output of the Schottky diode detector; a current source connected to the cathode to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

Another aspect of the invention provides a radio frequency communications system comprising an antenna; an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode, the Schottky diode detector further including a capacitor connected between the anode and ground, and including a capacitor having a first contact connected to the anode and having a second contact defining an output of the Schottky diode detector; and a current source connected to the anode to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

Another aspect of the invention provides a system comprising an antenna; a transponder including a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode; and means for driving current through both the antenna and the Schottky diode in a direction from the anode to the cathode.

Another aspect of the invention provides a method for realizing an improved radio frequency detector for use in a radio frequency identification device, the method comprising the following steps: providing an integrated circuit and an antenna, the integrated circuit having a receiver and a transmitter, the integrated circuit further having a Schottky diode and a current source, with the Schottky diode in operation being coupled to the antenna and the current source, the Schottky diode and antenna cooperating there between to form an inductorless radio frequency detector; applying a supply of power to the integrated circuit device from a battery; and applying a desired current across the Schottky diode to impart a desired impedance there across relative to the impedance of the antenna.

Another aspect of the invention provides a frequency lock loop comprising a current controlled oscillator including a plurality of selectively engageable current mirrors, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the current mirrors including transistors operating in a subthreshold mode.

Another aspect of the invention provides an integrated circuit comprising a receiver, a transmitter, and a frequency lock loop including a current source having a thermal voltage generator, a current controlled oscillator having a plurality of selectively engageable current mirrors multiplying up the current of the current source, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the current mirrors including transistors operating in a subthreshold mode.

Another aspect of the invention provides a timing oscillator that consumes less than one milliAmp.

Another aspect of the invention provides a method of constructing a frequency lock loop including a current controlled oscillator having a plurality of selectively engageable current mirrors, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the method comprising selecting current mirrors to vary frequency of operation, and operating transistors in the current mirrors in subthreshold mode.

Another aspect of the invention provides a method of operating an integrated circuit including a receiver, a transmitter, and a frequency lock loop including a current source having a thermal voltage generator, a current controlled oscillator having a plurality of selectively engageable current mirrors multiplying up the current of the current source, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the method comprising engaging selected current mirrors and operating transistors in the current mirrors in a subthreshold mode.

Another aspect of the invention provides an amplifier powered by a selectively engageable voltage source, the amplifier comprising first and second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors; a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output; selectively engageable resistances between the voltage source and respective inputs of the differential amplifier and defining, with the coupling capacitors, the high pass characteristics of the circuit; and second selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller values that the first mentioned resistances, the second resistances being engaged then disengaged in response to the voltage source being engaged.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a microprocessor, a receiver receiving radio frequency commands from an interrogation device, and a transmitter transmitting a signal identifying the device to the interrogator, the integrated circuit switching between a sleep mode, and a microprocessor on mode, in which more power is consumed than in the sleep mode, if the microprocessor determines that a signal received by the receiver is a radio frequency command from an interrogation device, the integrated circuit further including an amplifier powered by a selectively engageable voltage source engaged in the microprocessor on mode but not in the sleep mode, the amplifier including first and second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors, a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output, selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, second selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller values that the first mentioned resistances, the second resistances being engaged then disengaged in response to the integrated circuit switching from the sleep mode to the microprocessor on mode. Another aspect of the invention provides a method of speeding power up of an amplifier stage powered by a selectively voltage source and including first and second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors; a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output; and selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the method comprising: shorting around the selectively engageable resistances for a predetermined amount of time in response to the voltage source being engaged.

Another aspect of the invention provides a radio frequency communications system comprising an antenna; an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode, the Schottky diode detector further including a capacitor connected between the cathode and ground, and including a capacitor having a first contact connected to the cathode and having a second contact defining an output of the Schottky diode detector, the integrated circuit further including a clock recovery circuit recovering a clock from rising edges only of a signal at the output of the Schottky diode detector; and a current source connected to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

Another aspect of the invention provides a radio frequency communications system comprising an antenna; an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode, the Schottky diode detector further including a capacitor connected between the anode and ground, and including a capacitor having a first contact connected to the anode and having a second contact defining an output of the Schottky diode detector, the integrated circuit further including a clock recovery circuit recovering a clock from falling edges only of a signal at the output of the Schottky diode detector; and a current source connected to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

Another aspect of the invention provides a method of recovering a clock in a radio frequency communications system, the method comprising: providing an antenna; providing a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode, the Schottky diode detector further including a capacitor connected between the cathode and ground, and including a capacitor having a first contact connected to the cathode and having a second contact defining an output of the Schottky diode detector; driving current through the antenna and the Schottky diode in a direction from the anode to the cathode; and recovering a clock from rising edges only of a signal at the output of the Schottky diode detector.

Another aspect of the invention provides a method of recovering a clock in a radio frequency communications system, the method comprising: providing an antenna; providing a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode, the Schottky diode detector further including a capacitor connected between the anode and ground, and including a capacitor having a first contact connected to the anode and having a second contact defining an output of the Schottky diode detector; driving current through the antenna and the Schottky diode in a direction from the anode to the cathode; and recovering a clock from falling edges only of a signal at the output of the Schottky diode detector.

Another aspect of the invention provides a stage for a voltage controlled oscillator, the stage comprising a first transistor having a control electrode defining a first input, and having first and second power electrodes, the first power electrode defining a first node; a second transistor having a control electrode defining a second input, and having first and second power electrodes, the first power electrode of the second transistor defining a second node; a current source connected to the second power electrodes of the first and second transistors and directing current away from the second power electrodes of the first and second transistors; and means defining a variable resistance connecting the first and second nodes to a supply voltage.

Another aspect of the invention provides a stage for a voltage controlled oscillator, the stage comprising a first p-channel transistor having a gate defining a control node, having a source adapted to be connected to a supply voltage, and having a drain; a second p-channel transistor having a gate connected to the control node, having a source connected to the supply voltage, and having a drain; a first n-channel transistor having a gate defining a first input, having a drain connected to the drain of the first p-channel transistor and defining a first node, and having a source; a second n-channel transistor having a gate defining a second input, having a drain connected to the drain of the second p-channel transistor and defining a second node, and having a source; a current source connected to the sources of the first and second n-channel transistors directing current from the sources of the first and second n-channel transistors; a first resistor connected between the supply voltage and the drain of the first n-type transistor; a second resistor connected between the supply voltage and drain of the second n-type transistor; a first source follower having an input connected to the first node and having an output defining a first output of the stage; and a second source follower having an input connected to the second node and having an output defining a second output of the stage.

Another aspect of the invention provides a transmitter including a ring oscillator having a chain of stages, each stage comprising a first p-channel transistor having a gate defining a control node, having a source adapted to be connected to a supply voltage, and having a drain; a second p-channel transistor having a gate connected to the control node, having a source connected to the supply voltage, and having a drain; a first n-channel transistor having a gate defining a first input, having a drain connected to the drain of the first p-channel transistor and defining a first node, and having a source; a second n-channel transistor having a gate defining a second input, having a drain connected to the drain of the second p-channel transistor and defining a second node, and having a source; a current source connected to the sources of the first and second n-channel transistors directing current from the sources of the first and second n-channel transistors; a first resistor connected between the supply voltage and the drain of the first n-type transistor; a second resistor connected between the supply voltage and drain of the second n-type transistor; a first source follower having an input connected to the first node and having an output defining a first output of the stage; and a second source follower having an input connected to the second node and having an output defining a second output of the stage.

Another aspect of the invention provides a method of varying frequency in a stage of a voltage controlled oscillator having two input transistors having gates defining input nodes and having drain to source paths adapted to be connected between a supply voltage and a current source, the method comprising providing an impedance between the input transistors and the supply voltage, and varying the impedance.

Another aspect of the invention provides a frequency doubler comprising a first Gilbert cell; a second Gilbert cell coupled to the first Gilbert cell; a frequency generator configured to apply a first sinusoidal wave to the first Gilbert cell; and a phase shifter applying a sinusoidal wave shifted from the first sinusoidal wave to the second Gilbert cell.

Another aspect of the invention provides a frequency doubler comprising a first Gilbert cell including a first pair

of transistors having sources that are connected together, a second pair of transistors having sources that are connected together, a first one of the transistors of the first pair having a gate defining a first input node and a first one of the transistors of the second pair having a gate connected to the first input node, a second one of the transistors of the first pair having a gate defining a second input node and a second one of the transistors of the second pair having a gate connected to the second input node, the first transistor of the first pair having a drain, and the second transistor of the second pair having a drain connected to the drain of the first transistor of the first pair, the second transistor of the first pair having a drain, and the first transistor of the second pair having a drain connected to the drain of the second transistor of the first pair, a third pair including first and second transistors having sources coupled together, the first transistor of the third pair having a drain connected to the source of the second transistor of the first pair, the second transistor of the third pair having a drain connected to the source of the second transistor of the second pair, and a current source connected to the sources of the third pair and forward biasing the third pair, the second transistor of the third pair having a gate defining a third input node, and the first transistor of the third pair having a gate defining a fourth input node; and a second Gilbert cell including a first pair of transistors having sources that are connected together, a second pair of transistors having sources that are connected together, a first one of the transistors of the first pair of the second cell having a gate defining a first input node and a first one of the transistors of the second pair of the second cell having a gate connected to the first input node of the second cell, a second one of the transistors of the first pair of the second cell having a gate defining a second input node of the second cell and a second one of the transistors of the second pair of the second cell having a gate connected to the second input node of the second cell, the first transistor of the first pair of the second cell having a drain, and the second transistor of the second pair of the second cell having a drain connected to the drain of the first transistor of the first pair of the second cell, the second transistor of the first pair of the second cell having a drain, and the first transistor of the second pair of the second cell having a drain connected to the drain of the second transistor of the first pair of the second cell, a third pair including first and second transistors having sources coupled together, the first transistor of the third pair of the second cell having a drain connected to the source of the second transistor of the first pair of the second cell, the second transistor of the third pair of the second cell having a drain connected to the source of the second transistor of the second pair of the second cell, and a current source connected to the sources of the third pair of the second cell and forward biasing the third pair of the second cell, the second transistor of the third pair of the second cell having a gate defining a third input node of the second cell, and the first transistor of the third pair of the second cell having a gate defining a fourth input node of the second cell; the drain of the second transistor of the first pair of the second cell being connected to the drain of the second transistor of the first pair of the first cell, the drain of the second transistor of the second pair of the second cell being connected to the drain of the second transistor of the second pair of the second cell, the first input node of the second cell being connected to the fourth input node of the first cell, the third input node of the second cell being connected to the second input node of the first cell, and the fourth input node of the second cell being connected to the first input node of the first cell.

Another aspect of the invention provides a method of doubling frequency without using a feedback loop, the method comprising: providing a first Gilbert cell; providing a second Gilbert cell coupled to the first Gilbert cell; applying a first sinusoidal wave to the first Gilbert cell; and applying a sinusoidal wave shifted from the first sinusoidal wave to the second Gilbert cell.

Another aspect of the invention provides a pseudo random number generator comprising a linear feedback shift register switchably operable in a first mode, and in a second mode wherein the shift register consumes more power than in the first mode.

Another aspect of the invention provides a method of generating a pseudo random number, the method comprising providing a linear feedback shift register; providing an oscillator which generates clock signals used by the linear feedback shift register for shifting; and providing a first power level to the oscillator when a pseudo random number is required, and providing a second power level, lower than the first power level, to the oscillator at other times. Another aspect of the invention provides a method of generating a pseudo random number, the method comprising: providing a linear feedback shift register; providing an oscillator which generates clock signals used by the linear feedback shift register for shifting; and operating the oscillator at a first frequency in response to a request for a pseudo random number, and operating the oscillator at a second frequency lower than the first frequency after the pseudo random number is generated.

Another aspect of the invention provides a system comprising a microprocessor operating at a frequency; a linear feedback shift register operable in a low power mode, wherein the shift register operates at a frequency below the frequency of the microprocessor, and a high power mode wherein the shift register consumes more power than in the low power mode, operates at the frequency of the microprocessor, and shifts data into the microprocessor.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a receiver, a transmitter, a thermal voltage generator, a microprocessor operating at a frequency, a linear feedback shift register operable in a low power mode, wherein the shift register operates at a frequency below the frequency of the microprocessor, and a high power mode wherein the shift register consumes more power than in the low power mode, operates at the frequency of the microprocessor, and shifts data into the microprocessor, an oscillator supplying clock signals to the shift register, and current mirrors supplying current to each stage of the shift register, the current mirrors being referenced to the thermal voltage generator when the shift register is in the low power mode, and, when the shift register is in the high power mode, connected to a supply voltage potential greater than the potential provided by the thermal voltage generator.

Another aspect of the invention provides a method of generating a pseudo random number, the method comprising: providing a thermal voltage generator, a linear feedback shift register, an oscillator supplying clock signals to the shift register, and current mirrors supplying current to each stage of the shift register; referencing the current mirrors to the thermal voltage generator when no pseudo random number is required; and connecting the current mirrors to a supply voltage potential greater than the potential provided by the thermal voltage generator when a pseudo random number is required.

Another aspect of the invention provides an integrated circuit comprising a receiver and a transmitter sharing a common antenna.

Another aspect of the invention provides a method of using an integrated circuit including a receiver and a transmitter, the method comprising connecting the receiver and transmitter to a common antenna.

Another aspect of the invention provides an integrated circuit comprising:

a die including a transmitter having an antenna output and a detector having an antenna input; a package housing the die; a first contact connected to the antenna output and accessible from outside the package; a second contact connected to the antenna input and accessible from outside the package; and a short electrically connecting the first contact to the second contact outside the package.

Another aspect of the invention provides a method of using an integrated circuit including a die having a transmitter including an antenna output and a detector including an antenna output, the integrated circuit further including a package housing the die, a first contact connected to the antenna output and accessible from outside the package, and a second contact connected to the antenna input and accessible from outside the package, the method comprising: electrically shorting the first contact to the second contact outside the package.

Another aspect of the invention provides a transceiver comprising an antenna having a first end connected to a bias voltage, and having a second end; a detector including a Schottky diode having an anode connected to the second end of the antenna; and a transmitter having an output connected to the second end of the antenna.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including both a receiver and a transmitter; a first antenna connected to the receiver; and a second antenna connected to the transmitter.

Another aspect of the invention provides a transceiver comprising a loop antenna having a first end connected to a bias voltage, and having a second end; a second antenna; a detector including a Schottky diode having an anode connected to the second end of the antenna; and a transmitter having an output connected to the second antenna.

Another aspect of the invention provides a transceiver comprising an antenna having a first end connected to a bias voltage, and having a second end; a detector including a Schottky diode having an anode connected to the second end of the antenna; and an active transmitter having an output connected to the second end of the antenna.

Another aspect of the invention provides a transceiver comprising an antenna having a first end, and having a second end; a detector including a Schottky diode having a cathode connected to the second end of the antenna and defining a potential at the second end of the antenna, the first end of the antenna being connected to a potential lower than the potential of the second end of the antenna; and a backscatter transmitter including a transistor having a first power electrode connected to the first end of the antenna, a second power electrode connected to the second end of the antenna, and a control electrode adapted to have a modulation signal applied thereto.

Another aspect of the invention provides a transceiver in accordance with claim and further comprising a current source directing current in the direction from the anode to the cathode.

Another aspect of the invention provides a transceiver comprising a loop antenna having a first end connected to a bias voltage, and having a second end; a detector including a Schottky diode having an anode connected to the second end of the antenna; a backscatter transmitter having a first output and having a second output; a capacitor connected between the first output and the first end of the antenna; and a capacitor connected between the second output and the second end of the antenna.

Another aspect of the invention provides a method of configuring a transceiver including a backscatter transmitter having first and second outputs, and a detector having a Schottky diode including an anode, the method comprising: applying a bias voltage to a first end of an antenna; connecting a second end of the antenna to the anode; connecting a capacitor between the first output and the first end of the antenna; and connecting a capacitor between the second output and the second end of the antenna.

Another aspect of the invention provides a method of arranging a transceiver including a backscatter transmitter and a detector having a Schottky diode including a cathode, the method comprising: connecting a first end of an antenna to a ground potential; connecting a second end of the antenna to the cathode; and connecting a first power electrode of a transistor to the first end of the antenna; connecting a second power electrode connected to the second end of the antenna; and connecting a control electrode of the transistor to a modulation signal.

Another aspect of the invention provides a method of determining when a phase lock loop achieves frequency lock relative to a desired frequency, the phase lock loop including a voltage controlled oscillator having a control node and oscillating at a frequency responsive to the voltage applied to the control node, the method comprising: crossing the voltage that would result in the phase lock loop tracking the desired frequency in a first direction; crossing the voltage that would result in the phase lock loop tracking the desired frequency in a second direction opposite the first direction; and indicating that frequency lock has been achieved.

Another aspect of the invention provides a method of determining when frequency lock occurs relative to a desired frequency, the method comprising:

providing a phase lock loop including a voltage controlled oscillator that oscillates at a frequency responsive to voltage applied to the voltage controlled oscillator; applying a voltage to the voltage controlled oscillator to produce a frequency of oscillation less than the desired frequency; increasing the voltage applied to the voltage controlled oscillator using one or more steps of a first size; increasing the voltage applied to the voltage controlled oscillator using one or more steps of a second size smaller than the first size; decreasing the voltage applied to the voltage controlled oscillator using one or more steps of a third size smaller than the second size; increasing the voltage applied to the voltage controlled oscillator using a step of the third size; and indicating that lock has occurred in response to the increase of the step of the third size.

Another aspect of the invention provides a method of determining when a phase lock loop achieves frequency lock relative to a desired frequency, the phase lock loop including a voltage controlled oscillator having a control node and oscillating at a frequency responsive to the voltage applied to the control node, the method comprising: increasing the voltage applied to the control node to a voltage above the voltage that would result in the phase lock loop tracking the desired frequency; decreasing the voltage applied to the control node to a voltage below the voltage that would result in the phase lock loop tracking the desired frequency; and increasing the voltage applied to the control node and indicating that frequency lock has been achieved.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit

including a microprocessor, a transmitter, and a receiver, the integrated circuit periodically switching between a sleep mode, and a receiver-on mode in which more power is consumed than in the sleep mode, and further including a selectively engageable timer preventing switching from the sleep mode to the receiver-on mode for a predetermined amount of time.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit periodically switching between a sleep mode, and a receiver-on mode in which more power is consumed than in the sleep mode, and further including means for selectively preventing switching from the sleep mode to the receiver-on mode for a predetermined amount of time.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit being switchable between a sleep mode, and a mode in which more power is consumed than in the sleep mode, the integrated circuit being switched from the sleep mode to the mode in which more power is consumed in response to a direct sequence spread spectrum modulated radio frequency signal being received by the receiver which has a predetermined number of transitions within a certain period of time, the integrated circuit further including a selectively engageable timer which prevents switching from the sleep mode for a period of time regardless of whether a signal is subsequently received by the receiver which has the predetermined number of transitions within a certain period of time.

Another aspect of the invention provides a method for conserving power in a radio frequency identification device, the method comprising: periodically switching from a sleep mode to a receiver on mode and performing tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present; and selectively disabling the periodic switching from the sleep mode for a predetermined amount of time.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Overview of Device

FIG. **1** illustrates a radio frequency data communication device **12** embodying the invention. The radio frequency data communication device **12** includes an integrated circuit **16**, a power source **18** connected to the integrated circuit **16** to supply power to the integrated circuit **16**, and at least one antenna **14** connected to the integrated circuit **16** for radio frequency transmission and reception by the integrated circuit **16**. For purposes of this disclosure, including the appended claims, the term "integrated circuit" shall be defined as a combination of interconnected circuit elements inseparably associated on or within a continuous substrate. For purposes of this disclosure, including the appended claims, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). For purposes of this disclosure, including the appended claims, the term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. In the illustrated embodiment, the integrated circuit **16** is a monolithic integrated circuit. For purposes of this disclosure, including the appended claims, the term "monolithic integrated circuit" shall be defined as an integrated circuit wherein all circuit components are manufactured into or on top of a single chip of silicon. The integrated circuit **16** will be described in greater detail below. The power source **18** is a battery or other suitable power source.

Housing

The radio frequency data communication device **12** can be included in any appropriate housing or packaging.

FIG. **2** shows but one example in the form of an employee identification badge **10** including the radio frequency data communication device **12**, and a card **11** made of plastic or other suitable material. In one embodiment, the radio frequency data communication device **12** is laminated to the back face of the plastic card **11**, and the card forms the visible portion of the badge. In another embodiment, the radio frequency data communication device **12** is bonded to the back face of the card by embedding it within a thin bond line of epoxy-based material. Alternatively, the radio frequency data communication device **12** is embedded into the plastic card **11**. In one embodiment, the front face of the badge **10** has visual identification features including an employee photograph as well as identifying text.

FIG. **3** illustrates but one alternative housing supporting the device **12**. More particularly, FIG. **3** shows a miniature housing **20** encasing the device **12** to define a tag which can be supported by an object (e.g., hung from an object, affixed to an object, etc.). The housing **20** preferably has the general shape and size, in plan view, of a postage stamp. The embodiment of FIG. **3** also includes a card **21** supporting the device **12** in the housing **20**. The card **21** is formed of plastic or other suitable material having a thickness of about 0.040 inches, a width of about 1.25 inches, and a height of about 1.25 inches. In one embodiment, the device **12** is bonded to a back face of the card **21** with a thin layer of non-conductive epoxy material that cooperates with the card to define the housing **20**.

Although two particular types of housings have been disclosed, the device **12** can be included in any appropriate housing. The device **12** is of a small size that lends itself to applications employing small housings, such as cards, miniature tags, etc. Larger housings can also be employed. The device **12**, housed in any appropriate housing, can be supported from or attached to an object in any desired manner; for example using double sided tape, glue, lanyards, leash, nails, staples, rivets, or any other fastener. The housing can be sewn on to an object, hung from an object, implanted in an object (hidden), etc.

Antenna

Various configurations are possible for the antenna **14**. The integrated circuit **16** includes a receiver **30** and a transmitter **32** (FIG. **5**). In one embodiment, separate antennas **44** and **46** are provided for receiver and transmitter of the integrated circuit **16**. In another embodiment (FIG. **1**), a single antenna is shared by the receiver and transmitter sections. In one embodiment, the antenna is defined by conductive epoxy screened onto a card or housing. In the illustrated embodiment, the antenna is conductively bonded to the integrated circuit via bonding pads.

In an embodiment where a single antenna is employed, that single antenna preferably comprises a folded dipole antenna defining a continuous conductive path, or loop, of

microstrip. Alternatively, the antenna can be constructed as a continuous loop antenna.

Battery

If the power source **18** is a battery, the battery can take any suitable form. Preferably, the battery type will be selected depending on weight, size, and life requirements for a particular application. In one embodiment, the battery **18** is a thin profile button-type cell forming a small, thin energy cell more commonly utilized in watches and small electronic devices requiring a thin profile. A conventional button-type cell has a pair of electrodes, an anode formed by one face and a cathode formed by an opposite face. Exemplary button-type cells are disclosed in several pending U.S. patent applications including U.S. patent application Ser. No. 08/205,957, "Button-Type Battery Having Bendable Construction and Angled Button-Type Battery," listing Mark E. Tuttle and Peter M. Blonsky as inventors; now U.S. Pat. No. 5,432,027; U.S. patent application Ser. No. 08/321,251, "Button-Type Batteries and Method of Forming Button-Type Batteries," listing Mark E. Tuttle as inventor; now U.S. Pat. No. 5,494,495; and U.S. patent application Ser. No. 08/348,543, "Method of Forming Button-Type Batteries and a Button-Type Battery Insulating and Sealing Gasket," listing Mark E. Tuttle as inventor now U.S. Pat. No. 5,662,718. These patent applications and resulting patents are hereby incorporated by reference. In an alternative embodiment, the battery **18** comprises a series connected pair of button type cells. Instead of using a battery, any suitable power source can be employed.

Overview of Communication System

FIG. **4** illustrates a radio frequency communication system **24** including the device **12** and a radio frequency interrogator unit (hereinafter "interrogator") **26**. The device **12** transmits and receives radio frequency communications to and from the interrogator **26**. Preferably, the interrogator unit **26** includes an antenna **28**, as well as dedicated transmitting and receiving circuitry, similar to that implemented on the integrated circuit **16**. The system **24** further includes a host computer **48** in communication with the interrogator **26**. The host computer **48** acts as a master in a master-slave relationship with the interrogator **26**. The host computer **48** includes an applications program for controlling the interrogator **26** and interpreting responses, and a library ("MRL") of radio frequency identification device applications or functions. Most of the functions communicate with the interrogator **26**. These functions effect radio frequency communication between the interrogator **26** and the device **12**. These functions are described below in a section titled "Protocol."

One example of an interrogator implemented in combination with a transponder unit is disclosed in U.S. Pat. No. 4,857,893, hereby incorporated by reference. Generally, the interrogator **26** includes an antenna **28**, and transmits an interrogation signal or command **27** ("forward link") via the antenna **28**. The device **12** receives the incoming interrogation signal via its antenna **14**. Upon receiving the signal **27**, the device **12** responds by generating and transmitting a responsive signal or reply **29** ("return link"). Preferably, the responsive signal **29** is encoded with information that uniquely identifies, or labels the particular device **12** that is transmitting, so as to identify any object or person with which the device **12** is associated.

In the illustrated embodiment in FIG. **4**, there is no communication between devices **12**. Instead, the devices **12** communicate with the interrogator **26**. FIG. **4** illustrates the device **12** as being in the housing **20** of FIG. **3**. The system **24** would operate in a similar manner if the device **12** is provided in a housing such as the housing **10** of FIG. **2**, or any other appropriate housing. Multiple devices **12** can be used in the same field of an interrogator **26** (i.e., within communications range of an interrogator **26**). Similarly, multiple interrogators **26** can be in proximity to one or more of the devices **12**.

Various U.S. patent applications, which are incorporated herein by reference, disclose features that are employed in various alternative embodiments of the invention: Ser. No. 08/092,147, filed Jul. 15, 1993, "Wake Up Device for a Communications System" now abandoned, and continuation application Ser. No. 08/424,827, filed Apr. 19, 1995, "Wake Up Device for a Communications System"; now U.S. Pat. No. 5,790,946; Ser. No. 08/281,384, filed Jul. 27, 1994, "Communication System Having Transmitter Frequency Control"; now U.S. Pat. No. 5,539,775, Ser. No. 07/990,918, filed Dec. 15, 1992, now U.S. Pat. No. 5,365,551, "Data Communication Transceiver Using Identification Protocol"; Ser. No. 07/899,777, filed Jun. 17, 1992, "Radio Frequency Identification Device (RFID) and Method of Manufacture, Including an Electrical Operating System and Method," now abandoned; Ser. No. 07/921,037, filed Jul. 24, 1992, "Anti-Theft Method for Detecting The Unauthorized Opening of Containers and Baggage," now abandoned; Ser. No. 07/928,899, filed Aug. 12, 1992, "Electrically Powered Postage Stamp or Mailing or Shipping Label Operative with Radio Frequency (RF) Communications," now abandoned; and Ser. No. 08/032,384, filed on Mar. 17, 1993, "Modulated Spread Spectrum in RF Identification Systems Method," now allowed.

The above described system **24** is advantageous over prior art devices that utilize magnetic field effect systems because, with the system **24**, a greater range can be achieved, and more information can be obtained (instead of just an identification number).

As a result, such a system **24** can be used, for example, to monitor large warehouse inventories having many unique products needing individual discrimination to determine the presence of particular items within a large lot of tagged products. The system can also be used to counteract terrorism to monitor luggage entering a plane to ensure that each item of luggage that enters the plane is owned by a passenger who actually boards the plane. Such a technique assumes that a terrorist will not board a plane that he or she is planning to bomb. The system **24** is useful whenever RF transmission over a large range is desirable, such as for inventory control. In one embodiment, the sensitivity of the devices **12** is adjustable so that only devices within a certain range of the interrogator **26** will respond. In another if embodiment, the power of the interrogator **26** is adjustable so that only devices within a certain range of the interrogator **26** will respond.

However, a power conservation problem is posed by such implementations where batteries are used to supply power to the integrated circuits **16**. If the integrated circuit **16** operates continuously at full power, battery life will be short, and device **12** will have to be frequently replaced. If the battery **18** is permanently sealed in a housing, replacement of the battery will be difficult or impossible. For example, one reason for sealing the battery with the integrated circuit **16** and antenna **14** in a housing is to simplify the design and construction, to reduce the cost of production, and protect the electrical interconnections between devices. Another reason is protection of the battery and integrated circuit **16** from moisture and contaminants. A third reason is to enhance the cosmetic appeal of the device **12** by eliminating the need for an access port or door otherwise necessary to

insert and remove the battery. When the battery is discharged, the entire badge or stamp is then discarded. It is therefore desirable in this and other applications to incorporate power conservation techniques into the integrated circuit **16** in order to extend useful life.

In one embodiment, the devices **12** switch between a "sleep" mode of operation, and higher power modes to conserve energy and extend battery life during periods of time where no interrogation signal **27** is received by the device **12**. These power conservation techniques are described in greater detail below.

In one embodiment of the invention, in order to further extend the life of the battery **18**, the receiver sensitivity of the device **12** is tuned over a range of tuned and detuned states in order to modify the ability of the device to detect signal **27**, and therefore adjust the tendency for the device to wake up. One way to adjust the receiver sensitivity is by adjusting the sensitivity, or impedance of the antenna. Another way is by controlling the gain of amplifiers included in the receiver. Another way is to adjust or switch in different circuit elements in the device **12**, thereby realizing different circuit configurations. Additionally, the transmitting sensitivity for the device **12** can be adjusted. For example, transmitting range can be adjusted by controlling interrogator continuous wave power if the transmitter is operating in backscatter mode, and by controlling output power if the transmitter is in active mode.

Overview of Integrated Circuit

FIG. **5** is a high level circuit schematic of the integrated circuit **16** utilized in the devices of FIGS. **1–4**. In the embodiment shown in FIG. **5**, the integrated circuit **16** is a monolithic integrated circuit. More particularly, in the illustrated embodiment, the integrated circuit **16** comprises a single die, having a size of 209×116 mils^2, including the receiver **30**, the transmitter **32**, a micro controller or microprocessor **34**, a wake up timer and logic circuit **36**, a clock recovery and data recovery circuit **38**, and a bias voltage and current generator **42**.

In one embodiment, a spread spectrum processing circuit **40** is also included in the integrated circuit **16** and formed relative to the single die. In this embodiment, signals received by the receiver **30** are modulated spread spectrum signals. Spread spectrum modulation is described below. In the illustrated embodiment, the modulation scheme for replies sent by the transmitter **32** is selectable. One of the available selections for replies sent by the transmitter **32** is modulated spread spectrum.

Spread Spectrum Modulation

Many modulation techniques minimize required transmission bandwidth. However, the spread spectrum modulation technique employed in the illustrated embodiment requires a transmission bandwidth that is up to several orders of magnitude greater than the minimum required signal bandwidth. Although spread spectrum modulation techniques are bandwidth inefficient in single user applications, they are advantageous where there are multiple users, as is the case with the instant radio frequency identification system **24**. The spread spectrum modulation technique of the illustrated embodiment is advantageous because the interrogator signal can be distinguished from other signals (e.g., radar, microwave ovens, etc.) operating at the same frequency. The spread spectrum signals transmitted by the device **12** and by the interrogator **26** (FIG. **4**) are pseudo random and have noise-like properties when compared with the digital command or reply. The spreading waveform is controlled by a pseudo-noise or pseudo random number (PN) sequence or code (described below). The PN code is a binary sequence that appears random but can be reproduced in a predetermined manner by the device **12**. More particularly, incoming spread spectrum signals are demodulated by the device **12** through cross correlation with a version of the pseudo random carrier that is generated by the device **12** itself. Cross correlation with the correct PN sequence unspreads the spread spectrum signal and restores the modulated message in the same narrow band as the original data.

A pseudo-noise or pseudo random sequence (PN sequence) is a binary sequence with an autocorrelation that resembles, over a period, the autocorrelation of a random binary sequence. The autocorrelation of a pseudo-noise sequence also roughly resembles the autocorrelation of band-limited white noise. A pseudo-noise sequence has many characteristics that are similar to those of random binary sequences. For example, a pseudo-noise sequence has a nearly equal number of zeros and ones, very low correlation between shifted versions of the sequence, and very low cross correlation between any two sequences. A pseudo-noise sequence is usually generated using sequential logic circuits. For example, a pseudo-noise sequence can be generated using a feedback shift register.

A feedback shift register comprises consecutive stages of two state memory devices, and feedback logic. Binary sequences are shifted through the shift registers in response to clock pulses, and the output of the various stages are logically combined and fed back as the input to the first stage. The initial contents of the memory stages and the feedback logic circuit determine the successive contents of the memory.

The illustrated embodiment employs direct sequence spread spectrum modulation. A direct sequence spread spectrum (DSSS) system spreads the baseband data by directly multiplying the baseband data pulses with a pseudo-noise sequence that is produced by a pseudo-noise generator. A single pulse or symbol of the PN waveform is called a "chip." Synchronized data symbols, which may be information bits or binary channel code symbols, are added in modulo-2 fashion to the chips before being modulated. The receiver performs demodulation. For example, in one embodiment the data is phase modulated, and the receiver performs coherent or differentially coherent phase-shift keying (PSK) demodulation. In another embodiment, the data is amplitude modulated. Assuming that code synchronization has been achieved at the receiver, the received signal passes through a wideband filter and is multiplied by a local replica of the PN code sequence. This multiplication yields the unspread signal.

A pseudo-noise sequence is usually an odd number of chips long. In the illustrated embodiment, one bit of data is represented by a thirty-one chip sequence. A zero bit of data is represented by inverting the pseudo-noise sequence.

Spread spectrum techniques are also disclosed in the following patent applications and patent, which are incorporated herein by reference: U.S. patent application Ser. No. 08/092,147; U.S. patent application Ser. No. 08/424,827, filed Apr. 19, 1995; and U.S. Pat. No. 5,121,407 to Partyka et al. They are also disclosed, for example, in "Spread Spectrum Systems," by R. C. Dixon, published by John Wiley and Sons, Inc.

The system disclosed in U.S. patent application Ser. No. 08/092,147 includes two receivers, a low power receiver for detecting a wake up signal from an interrogator, and a high power receiver for receiving commands from an interrogator. On the other hand, the integrated circuit **16** of the illustrated embodiment employs a single receiver for both wake up and receiving commands from an interrogator.

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Another difference is that in the system **12** of the illustrated embodiment the receiver, not the interrogator, controls wake up. In the system **24** of the illustrated embodiment, the integrated circuit **16** includes a timer that causes the receiver and support circuitry to be powered on periodically. This is described in greater detail elsewhere.

Backscatter and Frequency Hopping

The interrogator sends out a command that is spread around a certain center frequency (e.g, 2.44 GHz). After the interrogator transmits the command, and is expecting a response, the interrogator switches to a CW mode (continuous wave mode). In the continuous wave mode, the interrogator does not transmit any information. Instead, the interrogator just transmits 2.44 GHz radiation. In other words, the signal transmitted by the interrogator is not modulated. After the device **12** receives the command from the interrogator, the device **12** processes the command. If the device **12** is in a backscatter mode it alternately reflects or does not reflect the signal from the interrogator to send its reply. For example, in the illustrated embodiment, two halves of a dipole antenna are either shorted together or isolated from each other, as described below in greater detail. In the illustrated embodiment, frequency hopping does not occur when the interrogator transmits a command, but occurs when the interrogator is in the continuous wave mode. The interrogator, in the continuous wave mode, hops between various frequencies close to the 2.44 GHz frequency. These various frequencies are sufficiently close to the 2.44 GHz frequency that backscatter antenna reflection characteristics of the device **12** are not appreciably altered. Because the interrogator is hopping between frequencies, the interrogator knows what frequency backscatter reflections to expect back from the device **12**. By hopping between various frequencies, the amount of time the interrogator continuously uses a single frequency is reduced. This is advantageous in view of FCC regulatory requirements.

In the illustrated embodiment, no attempt is made to frequency hop at the interrogator to a pseudo-random sequence and then correlate to that at the receiver. However, in alternative embodiments, such correlation takes place.

CMOS Process

The integrated circuit **16** is formed according to semiconductor wafer processing steps, such as CMOS semiconductor wafer processing steps used to form static random access memories. In the preferred embodiment, the integrated circuit **16** is a single metal integrated circuit. In other words, the integrated circuit **16** is formed using a single metal layer processing method. More particularly, only one layer of metal (e.g., aluminum) is employed. This is advantageous in that it results in a lower cost of production.

In this processing method, a p-type wafer is employed. The processing method employed provides n-well areas used to define p-channel transistors; an active area which is used to define p+ and n+ diffused regions inside the p-type wafer or inside the n-well areas. Next, a layer is provided that helps prevent leakage between adjacent devices. Then, transistor are defined by forming n-type and p-type polysilicon. Then, a contact layer is defined for connecting desired intersections of polysilicon with metal (aluminum) that is subsequently formed. The contact layer is also used, in some instances, for connecting desired intersections of the metal that is subsequently formed with active area. Then the metal layer is formed. The contact layer provides a means for connecting metal with layers below the metal. Then, a passivation step is performed. Passivation means that the die is covered with a protective layer and holes are cut around the edge of the die so that electrical connection can be made to the bond pads.

In some processing, after the metal layer is formed, an insulating layer is provided, and another layer of aluminum is formed above the insulating layer. Holes are provided at selected locations to interconnect the top layer of aluminum with lower layers. An advantage of using multiple layers of metal is that it provides greater flexibility in how functional blocks are laid out and in how power is bused to various areas. However, multiple metal layers add processing steps. This results in added cost and complexity.

The process of the preferred embodiment employs only one layer of metal, and is therefore a relatively simple, inexpensive process.

The following U.S. patents, which are incorporated herein by reference, disclose CMOS processing techniques that are employed in various alternative embodiments of the invention: U.S. Pat. Nos. 5,489,546 to Ahmad et al.; 5,272,367 to Dennison et al.; and 5,134,085 to Gilgen et al.

Various other processing methods can be employed in alternative embodiments.

Transmitter and Receiver

The receiver **30** is a radio frequency receiver included in the integrated circuit **16**, and the transmitter **32** is a radio frequency transmitter included in the integrated circuit **16**. In one embodiment, the receiver **30** includes a Schottky diode detector. Various forms of Schottky diode detectors are described in a paper titled "Designing Detectors for RF/ID Tags," by Raymond W. Waugh of Hewlett-Packard Company, submitted for presentation at the RF Expo, San Diego, Feb. 1, 1995, and incorporated herein by reference.

The receiver **30** of the illustrated embodiment makes use of the rate or frequency of data included in incoming signals, but does not make use of the carrier frequency of the incoming signal. In other words, operation of the receiver **30** is independent of the frequency of the carrier of the incoming signal over a wide range of carrier frequencies.

Therefore, the device **12** can operate over a wide range of carrier frequencies. For example, the device **12** can operate with carriers of 915–5800 MHZ. In a more particular embodiment, the device **12** can operate with carrier frequencies in the 915, 2450, or 5800 MHZ bands. In the illustrated embodiment, the antennas are half wave antennas, and frequency selectivity of the device **12** is achieved based on selection of the antenna external to the integrated circuit **16**. Capacitors employed in the Schottky diode detector are also selected based on the carrier frequency that will be employed.

In one embodiment, the transmitter **32** is switchable between operating in a modulated backscatter transmitter mode, and operating in an active mode. The transmitter **32** switches between the backscatter mode and the active mode in response to a radio frequency command, instructing the transmitter to switch, sent by the interrogator **26** and received by the receiver **30**. In the active mode, a carrier for the transmitter is extracted from a signal received by the receiver **30**. Active transmitters are known in the art. See, for example, U.S. patent application Ser. No. 08/281,384. U.S. patent application Ser. No. 08/281,384 also discloses how transmit frequency for the transmitter **32** is recovered from a message received via radio frequency from the interrogator **26**. The device **12** differs from the device disclosed in U.S. patent application Ser. No. 08/281,384 in that a VCO control voltage is stored as an analog voltage level on a capacitor instead of as a digital number in a register. Further, in the illustrated embodiment, the recovered frequency is also used by the integrated circuit **16** to generate a DPSK subcarrier for modulated backscatter transmission.

The transmitter is capable of transmitting using different modulation schemes, and the modulation scheme is selectable by the interrogator. More particularly, if it is desired to change the modulation scheme, the interrogator sends an appropriate command via radio frequency. The transmitter can switch between multiple available modulation schemes such as Binary Phase Shift Keying (BPSK), Direct Sequence Spread Spectrum, On-Off Keying (OOK), and Modulated Backscatter (MBS).

Wake Up Timer and Logic Circuit

The integrated circuit **16** includes the wake up timer and logic circuit **36** for conserving battery power. More particularly, the integrated circuit **16** normally operates in a sleep mode wherein most circuitry is inactive and there is a very low current draw on the battery **18**. One circuit that is active during the sleep mode is a timer for waking up the integrated circuit at predetermined intervals. In the illustrated embodiment, the interval is 16 milliseconds; however, various other intervals can be selected by radio frequency by sending a message from the interrogator **26** to the device **12**. For example, in the illustrated embodiment, the interval is selectable as being 0.5, 16, 64 or 256 milliseconds.

Assuming the selected interval is 16 milliseconds, after every sleep period of 16 milliseconds the wake up timer and logic circuit **36** activates the receiver **30**, the clock recovery and data recovery circuit **38**, and all the bias currents and voltages associated with the receiver **30**. This is a receiver on mode, illustrated by a vertical line marked WAKEUP RX ON in FIG. **27**. Such bias currents and voltages are generated by the bias voltage and current generator **42**. The receiver **30** then determines if there is a radio frequency signal present.

If there is no radio frequency signal present, the wake up timer and logic circuit **36** deactivates the receiver **30** and clock recovery and data recovery circuit **38**. The receiver then goes back to sleep in the low current mode until another **16** milliseconds pass (or whatever sleep period is selected).

If there is a radio frequency signal present, the receiver will unspread the spread spectrum signal for processing. It is possible that while the receiver is on, it may detect a radio frequency signal from a source other than the interrogator **26**. For example, other radio frequency transmitting devices may be operating in the area. In the illustrated embodiment, the receiver is set to receive microwave frequency signals, so that a small antenna can be used. Therefore, the wake up timer and logic circuit **36** performs tests to determine if a radio frequency signal received on wake up is valid. This is a wake up abort test mode, illustrated by a vertical line marked WAKEUP ABORT TESTS in FIG. **27**. If the wake up timer and logic circuit **36** determines that the incoming signal is not valid, the integrated circuit **16** returns to the sleep mode. The illustrated integrated circuit **16** consumes approximately one micro amp in the sleep mode, and the battery **18** is expected to last up to 10 years with a current drain of that order, depending on how often radio frequency signals are present and on the capacity of the battery.

If a radio frequency signal is detected upon wake up, the wake up timer and logic compares the incoming signal to known characteristics of expected spread spectrum encoded data. In the illustrated embodiment, a valid incoming radio frequency signal will be a spread spectrum signal having a thirty-one chip code representing a single data bit. To represent a digital one ("1") the thirty-one chip code is sent as is. To represent a digital zero ("0") the thirty-one chip code is inverted. The wake up timer and logic circuit **36** knows how many transitions there are in a valid thirty-one chip sequence, and knows the time period within which all those transitions are expected (or the frequency of the transitions). After the incoming radio frequency signal is amplified and converted to baseband, it is tested against known characteristics of a valid signal.

If the incoming signal does not pass these tests, the integrated circuit **16** returns to the sleep mode. If the incoming signal does pass these tests, then the wake up timer and logic circuit determines whether the clock recovery and data recovery circuit **38** locks on to the clock frequency contained in the chip rate of the incoming signal within a predetermined time period. If frequency lock is obtained, the microprocessor is turned on for processing of the received command. this is a processor on mode illustrated by a vertical line marked "PROCESSOR ON" in FIG. **27**.

If frequency lock is not obtained within the predetermined time, the integrated circuit **16** returns to the sleep mode.

Other appropriate tests can be performed in embodiments where spread spectrum is not employed. In these embodiments, knowing how valid data is encoded, the wake up timer and logic still compares the number of transitions received in a given amount of time with an expected number of transitions for a valid signal.

In summary, various tests are performed, and the order in which they are performed is preferably selected to most quickly identify invalid signals. U.S. patent application Ser. No. 08/424,827, filed Apr. 19, 1995 and U.S. patent application Ser. No. 08/092,147, which are incorporated herein by reference, disclose tests that could be employed in various alternative embodiments of the invention.

After the wake up timer and logic circuit **36** determines that a received signal is valid, the integrated circuit **16** then performs clock recovery. To save space and cost, the preferred device **12** does not include a crystal timing element (clock). Instead, all timing for the device **12** is extracted from valid incoming signals received by the receiver **30**.

In one embodiment, a valid incoming radio frequency signal is digital, and starts with a preamble, which is followed by a start code (or Barker code), which is followed by data (e.g., a command). For example, in the illustrated embodiment, the preamble is a long (e.g., eighteen milliseconds) string of zeros; i.e., the thirty-one chip sequence is inverted, and sent repeatedly for approximately 18 milliseconds. In the illustrated embodiment the data or command after the Barker code is shorter than the preamble, and is approximately 4 milliseconds long.

Clock Recovery and Data Recovery Circuit

The clock for the entire integrated circuit **16** is extracted from the incoming message itself. In one embodiment, the transmitter **32** is selectable as being operable in an active transmission mode, or a backscatter mode. If the transmitter **32** is operating in an active mode, the extracted clock is multiplied up to the carrier frequency of the transmitter **32**. For example, in one embodiment, the transmitter carrier frequency is 2.44 GHz. The choice of chip rate is a function of the carrier frequency and the carrier frequency has to be divisible by a power of two to give the chip rate on the input.

If the transmitter **32** is operating in a backscatter mode, the clock that has been recovered from the incoming signal received by the receiver **30** is divided to make it slower and is then used for frequency shift key or phase shift key modulated backscatter.

In summary, a clock is recovered from the incoming message, and used for timing for the micro controller **34** and all the other clock circuitry on the chip, and also for deriving the transmitter carrier or the subcarrier, depending on whether the transmitter is operating in active mode or backscatter mode.

Note that there are disadvantages to generating a transmit frequency in this fashion. In an alternative embodiment (not shown), a crystal is employed to generate a clock. A crystal provides a more stable, reliable clock to generate the transmit frequency, but also increases cost and size of the device **12**.

In addition to recovering a clock, the clock recovery and data recovery circuit **38** also performs data recovery on valid incoming signals. The valid spread spectrum incoming signal is passed through the spread spectrum processing circuit **40**, and the spread spectrum processing circuit **40** extracts the actual ones and zeros of data from the incoming signal. More particularly, the spread spectrum processing circuit **40** takes the chips from the spread spectrum signal, and reduces each thirty-one chip section down to a bit of one or zero, which is passed to the micro controller **34**.

Micro Controller

The micro controller **34** includes a serial processor, or I/O facility that received the bits from the spread spectrum processing circuit **40**. The micro controller **34** performs further error correction. More particularly, a modified hamming code is employed, where each eight bits of data is accompanied by five check bits used by the micro controller **34** for error correction. The micro controller **34** further includes a memory, and after performing the data correction, the micro controller **34** stores bytes of the data bits in memory. These bytes contain a command sent by the interrogator **26**. The micro controller **34** responds to the command.

For example, the interrogator **26** may send a command requesting that any device **12** in the field respond with the device's identification number. Status information is also returned to the interrogator **26** from the device **12** when the device **12** responds.

Unalterable Identification

In one embodiment, the integrated circuit **16** includes unalterable indicia (a signature), different from the device's identification number discussed above. The unalterable indicia is burned into programmable read only memory or formed using a laser operating on fusible links. The unalterable indicia is indicative of the history of the particular die used to manufacture the integrated circuit **16**. For example, in the illustrated embodiment, the unalterable indicia includes a lot number, wafer number, and die number of the die used to manufacture the integrated circuit **16**. This information is transmitted by the transmitter in response to a manufacturer's command received by the receiver. In one embodiment, the manufacturer's command is a controlled access, or secret command that is not readily ascertainable by the public or purchaser/user of the device. This unalterable indicia can be used to trace manufacturing problems in defective devices **12**, or to locate stolen products carrying a device **12**.

Arbitration

If the interrogator **26** sends out a command requesting that all devices **12** within range identify themselves, and gets a large number of simultaneous replies, the interrogator **26** may not able to interpret any of these replies. Further, there may be multiple interrogators in an area trying to interrogate the same device **12**.

Therefore, arbitration schemes are provided. With the more common scenario of multiple devices **12** trying to respond to an interrogator, the interrogator **26** sends a command causing each device **12** of a potentially large number of responding devices **12** to select a random number from a known range and use it as that device's arbitration number. By transmitting requests for identification to various subsets of the full range of arbitration numbers, and checking for an error-free response, the interrogator **26** determines the arbitration number of every responder station capable of communicating at the same time. Therefore, the interrogator **26** is able to conduct subsequent uninterrupted communication with devices **12**, one at a time, by addressing only one device **12**.

If the interrogator **26** has prior knowledge of the identification number of a device **12** which the interrogator **26** is looking for, it can specify that a response is requested only from the device **12** with that identification number.

Arbitration schemes are discussed below, in greater detail, in connection with protocols.

U.S. Pat. No. 5,365,551 to Snodgrass et al., which is incorporated by reference, discloses arbitration schemes that could be employed in various alternative embodiments of the invention.

Reply

After the micro controller processes a command from the interrogator **26**, the micro controller formats the reply as specified in the protocol and the formatted reply leaves the micro controller via a serial data port of the micro controller. If desired, the formatted reply is spread spectrum encoded by the spread spectrum processing circuit **40**. The reply is then modulated by the transmitter **32**. The transmitter **32** is capable of transmitting using different modulation schemes, and the modulation scheme is selectable by the interrogator **26**. More particularly, if it is desired to change the modulation scheme, the interrogator **26** sends an appropriate command via radio frequency.

The transmitted replies have a format similar to the format of incoming messages. More particularly, a reply starts with a preamble (e.g., all zeros in active mode, or alternating double zeros and double ones in backscatter mode), followed by a Barker or start code which is thirteen bits long, followed by actual data.

No stop bits are included in the incoming message or reply, in the preferred embodiment. Instead, part of the incoming message describes how many bytes are included, so the integrated circuit **16** knows how much information is included. Similarly, part of the outgoing reply describes how many bytes are included, so the interrogator **12** knows how much information is included. The incoming message and outgoing reply preferably also include a check sum or redundancy code so that the integrated circuit **16** or the interrogator **12** can confirm receipt of the entire message or reply.

After the reply is sent, the integrated circuit **16** returns to the sleep mode, and the wake up timer and logic circuit **36** starts timing again for the next wake up (e.g., in 16 milliseconds, or whatever period is selected).

Detailed Circuit Schematics

FIG. **6** is a graph illustrating how FIGS. **6**AA–EK are to be assembled.

FIGS. **6**AA–EK include circuitry partitioned in blocks in a manner that is somewhat different from the way the blocks are partitioned in FIG. **5**. In some ways FIGS. **6**AA–EK shows less detail than in FIG. **5**, and in some ways they show more detail.

The integrated circuit **16** is shown as including an analog processor "anlgproc," an RF processor "rfproc," a PN (pseudo random number) processor "pnproc," a data processor "dataproc," and return link configuration logic "rlconfig."

The data processor "dataproc" shown in FIGS. **6**AA–EK is the micro controller or microprocessor **34** of FIG. **5**. The data processor "dataproc" is shown in greater detail in FIG.

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7. In the illustrated embodiment, the data processor "dataproc" is an eight bit processor, and includes a ROM "rom," a RAM "ram," a serial I/O block "sio," an eight bit ALU (arithmetic logic unit) "alu," an instruction decoder programmable logic array "insdec," and address decoder "adrdec," a clock generator "clk," a conditional qualifier decoder "cqualdec," a databus latch/precharge circuit "dblatch," a timed lockout divider "tld," a data interleaver (which interleaves two thirteen bit words) "dil," a convolutional encoder and preamble generator "conv," a digital port output controller "doutport," a shift register input data multiplexer "shdel" and a series of registers. In the illustrated embodiment, the registers include a timed lockout register "tloreg," a plurality of status registers "sreg," a plurality of read/write control registers "oreg," and an instruction register "insreg."

The registers are used to drive control lines to various different circuits to allow the data processor to have control over those circuits. The "sio" block (described below) is the data path for data received and for the data to be transmitted.

FIG. **6.01** is a layout diagram illustrating the physical layout of various components on an integrated circuit die, in accordance with one embodiment of the invention. The physical locations and sizes of components relative to other components are shown. Boundaries between various blocks may be approximate in the sense that portions of certain blocks may extend into other blocks. The layout diagram illustrates that separate analog and digital ground returns are provided. In the illustrated embodiment, the ground return for the receiver and transmitter is spaced apart from the receiver and transmitter. However, in an alternative embodiment, locating the ground return for the receiver and transmitter proximate the receiver and transmitter may provide improved results. In the preferred embodiment, the transmitter and receiver circuitry is physically located on the die close to an edge, proximate to the bond pads. More particularly, the microwave outputs of the transmitter **32** are arranged on the die so as to be next to (in close physical proximity to) the appropriate bond pads. Also shown in FIG. **6.01** are small squares adjacent the receiver and active transmitter pads, respectively. These are ground pads for microwave probing, in the exemplary embodiment. In an alternative embodiment, these microwave probing ground pads can be employed as functional ground pads instead of using the illustrated common analog ground pad.

FIGS. **7.01**AA–BB provide a circuit drawing of a processor clock generator "clk." The processor clock generator provides clock circuitry that generates all the various clocks that are used by the processor.

FIGS. **7.0101**AA–BB provide a circuit drawing of a processor clock controller "clkctl." The clock controller "clkctl" determines when the clocks are running. As described elsewhere, the processor is not always on. The clock controller uses enabling signals from wake up so that it knows when to turn on. Thus, some of the inputs to the clock controller are power wake up, receive wake up, timer wake up. The clock controller also synchronizes shut down of the clocks when the processor has completed its task.

FIGS. **7.0102**AE–DJ provide a circuit drawing of a processor phase generator "clkph." The processor phase generator "clkph" generates master clocks—phase one "PH1" and phase two "PH2"—which are non-overlapping clocks.

FIGS. **7.0103**AA–BD provide a circuit drawing of a clock state generator "clkst." The clock state generator "clkst" generates some derivative clocks. Processor instruction cycles are divided. There are cycles and there are states. Within each cycle, which is a certain time period, there are four states—**S1** through **S4**. The states are all non-overlapping, and each state has a high time that is one quarter of the cycle time. As a processor instruction executes, the instruction is taken from the rom "rom," and loaded into the instruction register. The instruction can be, for example, a 1, 2 or 3 cycle instruction, depending on how complex the function is that is performed by that instruction. These are micro instructions for running the processor on chip. They should not be confused with the commands that are sent by radio frequency, which are a much higher level commands. The commands sent by radio frequency require many of these micro instructions for the processor to carry them out. During clock cycle one, line **C1** in FIGS. **7.0103**AA–BD is high, during clock cycle two, line **C2** is high, etc. Within each one of those clock cycles, state one is high for a certain time period and then goes low, and state two goes high for a certain time period then goes low, and so on up through state four. Within each of these states, there is one phase one high time, and one phase two high time.

FIGS. **7.02**AA–BF provide a circuit drawing of an address decoder "adrdec." In executing instructions, the processor has the need to move bytes of data between registers and ram "ram" and possibly to the serial IO controller "sio." The address decoder "adrdec" generates enable lines to those various different blocks (the registers, ram, and sio, as appropriate) when their address appears on the address bus. The primary input to the address decoder is the address bus. This decoder decides which circuit block is being addressed and issues an enable for either a write or a read, whichever is appropriate, to that particular block.

FIGS. **7.03**AA–EH provide a circuit drawing of random access memory "ram." The ram has 512 bytes of storage available. 256 of those bytes are available to the user of the device **12**, and the other 256 bites are used to do calculations required by the processor. Most of the drawing is taken up by blocks of RAM arrays "ram8×4."

FIGS. **7.0301**AA–BB provide a circuit drawing of a ram control circuit "ramctl." The ram control circuit issues word line select enable signals, a read command, a write command, and some precharge signals. The ram control circuit generates the signals to control access to and from the random access memory "ram."

FIGS. **7.0302**AA–AC provide a circuit drawing of a RAM array C"ram 8×4." Each RAM array is made up of four rows and eight columns of RAM cells.

FIG. **7.030201** provides a circuit drawing of a single RAM cell. In the illustrated embodiment, the RAM cell is a six transistor RAM cell. Four transistor RAM cells are employed in alternative embodiments.

FIGS. **7.0303**AA–AD provide a circuit drawing of a RAM precharge circuit "rampch." FIGS. **7.0304**AA–AD provide a circuit drawing of a RAM precharge circuit "ramdch." In the illustrated embodiment, this circuit has been disabled as is shown in the figure. The RAM precharge circuits provides precharge signals to speed up writing to and reading from RAM cells.

FIG. **7.0305** provides a circuit drawing of a RAM address buffer "ramadb." The RAM address buffer isolates the capacitive load presented by the RAM circuits from the address bus.

FIGS. **7.0306**AA–BA provide a circuit drawing of a RAM word line driver "ramwdr." The RAM wordline driver is a predecoder. It takes two address inputs and generates four possible select lines "**P0**–**P3**" which are used in a row decoder (discussed below) for the RAM.

FIGS. **7.0307**AA–BB provide a circuit drawing of a RAM word line decoder "ramwdec." The RAM word line decoder

receives the select lines from the RAM wordline driver in conjunction with four other addresses "AD**0**–AD**3**" to select a unique word line. A word line is a row of RAM cells within the RAM.

FIGS. **7.0308**AA–BB provide a circuit drawing of a RAM column select decode circuit "ramcdec." The RAM column select decode circuit uses three address lines "AD**5**–AD**7**" to generate eight select lines "CSEL**0**–CSEL**7**."

FIGS. **7.0309**AA–BG provide a circuit drawing of a RAM column selector multiplexor "ramcsel." The RAM column selector multiplexor uses the output select lines "CSEL**0**–CSEL**7**" from the RAM column select decode circuit "ramcdec" to connect one pair of bit or column lines out of eight pairs "BIT**0**N/P"–"BIT**7**N/P" onto a bus. The bus goes to a sense amp or to a write driver, depending on whether a RAM cell is being read or written. There are eight of these RAM column selectors side by side, functioning in the same manner. With any one selection, one of eight pairs are selected on FIGS. **7.0309**AA–BG, but there are seven more similar selections taking place so an entire byte of RAM is selected at one time.

FIGS. **7.0310**AA–BB provide a circuit drawing of a RAM databus interface "ramdb." The RAM databus interface includes a sense amp and write driver for the RAM. The RAM databus interface receives the output/input lines "BIT**0**N/P"–"BIT**7**N/P" from the RAM column selector "ramcsel." Selected RAM cells can either be sensed or written.

FIGS. **7.04**AA–HJ provide a circuit drawing of a ROM "rom." The ROM has 4096 bytes of contact programmable memory. ROMs of multiple integrated circuits **16** are simultaneously mass programmed. In the third to the last mask step, each particular cell of ROM is programmed with a zero or a one. The ROM does not include the information about the lot number, wafer number and die number discussed elsewhere herein. The ROM is programmed at the time of manufacture, whereas the information about the lot number and wafer number and die location is stored after the manufacture of the wafer using an electrically programmable or laser fuse programmable, or electrical fuse programmable structure.

FIGS. **7.0401**AA–BB provide a circuit drawing of a ROM control logic circuit "romctl." The ROM control logic circuit provides signals to allow the contents of eight memory cells of the ROM, one byte to be read out at a time.

FIGS. **7.0402**AA–AB provide a circuit drawing of a ROM bit line precharge circuit "ROMPCH." The ROM bit line precharge circuit precharges bit lines of the ROM. Bit lines are the vertical lines in the array of ROM cells on which the voltage that is sensed appears after selected ROM cells are accessed.

FIGS. **7.0403**AA–BB provide a circuit drawing of a ROM word line driver "romwdr." The ROM word line driver (or row driver) takes address inputs "A**7**–A**9**" and generates enable signals "WDR**0**–WDR**7**" to select row lines of the ROM.

FIGS. **7.0404**AA–DC provide a circuit drawing of a ROM word block decoder "romwdec_rev." The ROM word block decoder has as inputs the enable signals "WDR**0**–WDR**7**" from the ROM word line driver "romwdr" plus other addresses to generate actual word line signals themselves. A word line signal selects a row of ROM cells.

FIGS. **7.0405**AA–BA provide a circuit drawing of a ROM bit line address driver "rombldr." The ROM bit line address driver buffers some of the addresses so they are capable of driving a large decoder structure "rombldec" (described below).

FIGS. **7.0406**AA–CK provide a circuit drawing of a ROM bit line decoder "rombldec." The ROM bit line decoder provides a decoder structure for selecting a particular ROM bit line out of thirty-two bit lines. There are eight such "rombldec" circuits, allowing simultaneous selection of eight bit lines.

FIGS. **7.0407**AA–AB provide a circuit drawing of a ROM sense amplifier "romsns." The ROM sense amplifier is the sense amp used for determining the state of a particular ROM bit being accessed. Eight ROM bit sense amplifiers are used.

FIGS. **7.05**AA–CB provide a circuit drawing of an instruction register "insreg." The code or program that controls the operation of the processor is stored in the ROM. The instructions stored in the ROM are transferred one at a time to this instruction register "insreg" so that they can be interpreted and the processor can carry out the operations required by that instruction. After the integrated circuit wakes up, its operation is controlled by the wake up and clock recovery circuits. After the integrated circuit locks on to the clock and a valid start (Barker) code is received, the processor turns on and the program stored in the ROM takes over from that point. The program performs functions such as determining if the integrated circuit **16** is in a power up cycle. If the device **12** is in a power up cycle, the processor performs various tasks relevant to power up. If the integrated circuit **16** is receiving a command from an interrogator, the program will determine which command and then go through a sequence of required steps in order to respond appropriately to that command. Then the program allows the integrated circuit **16** to go back to sleep.

FIGS. **7.0501**AA–BB provide a circuit drawing of an instruction register "insrcel" included in the instruction register "insreg."

FIGS. **7.06**AA–CN provide a circuit drawing of an instruction decoder PLA "insdec." The instruction decoder PLA interprets what is in the instruction register "insreg" and issues all the enable signals necessary to effect performance of the functions called for in that instruction. Details of the instruction decoder PLA are shown in FIGS. **7.0601**AA–HI; **7.0602**AA–JH; **7.0603**AA–JI; and **7.0604**AA–JI.

FIGS. **7.0601**AA–HI provide a circuit drawing of an instruction decoder (first section) "insdec**1**."

FIGS. **7.0602**AA–JH provide a circuit drawing of an instruction decoder (second section) "insdec**2**."

FIGS. **7.0603**AA–JI provide a circuit drawing of an instruction decoder (third section) "insdec**3**."

FIGS. **7.0604**AA–JI provide a circuit drawing of an instruction decoder (fourth section) "insdec**4**." FIG. **7.060401** provides a circuit drawing of an instruction decoder ROM amp "insramp" included in the circuit of FIGS. **7.0604**AA–JI, **7.0601**AA–HI, **7.0602**AA–JH, and **7.0603**AA–JI. FIG. **7.060402** is a circuit drawing of an instruction decoder PLA amp "inspamp" included in the circuit of FIGS. **7.0604**AA–JI, **7.0601**AA–HI, **7.0602**AA–JH, and **7.0603**AA–JI. FIG. **7.060403** is a circuit drawing of an instruction decoder PLA latch "insplat" included in the circuit of FIGS. **7.0604**AA–JI, **7.0601**AA–HI, **7.0602**AA–JH, and **7.0603**AA–JI.

FIGS. **7.07**AA–BB provide a circuit drawing of a conditional qualifier decoder "cqualdec." Certain instructions behave differently depending on certain conditions (e.g., whether a carry bit is set), and the conditional qualifier decoder looks for these conditions.

FIGS. **7.08**AA–CA provide a circuit drawing of a databus latch and precharge circuit "dblatch." Data is bused around

in eight bit bytes, and the databus latch and precharge circuit drives the databus. The data bus is in a precharge high state when the data bus is not being used. Whichever source of data is selected to put its information on the bus will then drive selected bits low if appropriate.

FIGS. **7.09**AA–BF provide a circuit drawing of an arithmetic logic unit "alu." The arithmetic logic unit "alu" is a basic arithmetic logic unit that provides enough flexibility to perform the functions that are needed for the RFID task. Details of the arithmetic logic unit are provided in drawings below.

FIGS. **7.0901**AA–CE provide a circuit drawing of an ALU low byte "alubyt**1**". There are eight bits within the ALU low byte that are all processed simultaneously.

FIGS. **7.090101**AA–AD provide a circuit drawing of a ALU bit "alubit**1**" included in the ALU low byte "alubyt**1**." FIGS. **7.090101**AA–AD show the registers contained within each bit of the ALU. The registers include an A cell "aluacell" and a B cell "alubcell" which are the primary registers. The data on which arithmetic or logical operations are to be performed reside typically in the A cell "aluacell" or the B cell "alubcell." The registers further include a program counter "alupc," a stack pointer "alurcell," a data pointer "alurcell," and a memory address register "alumar" that provides for indirect addressing. The ALU bit "alubit**1**" further includes an adder "aluadd" and a slave register "aluslave" to the adder.

FIG. **7.09010101** is a circuit drawing showing details of construction of an ALU bit decoder cell "alubdec" included in the ALU bit.

FIG. **7.09010102** is a circuit drawing showing details of construction of the ALU B register cell "alubcell" included in the ALU bit.

FIG. **7.09010103** is a circuit drawing showing details of construction of the ALU A register cell "alubacell" included in the ALU bit.

FIG. **7.09010104** is a circuit drawing showing details of construction of the ALU program counter "alupc" included in the ALU bit. FIG. **7.09010105** is a circuit drawing showing details of construction of the ALU register cell "alurcell." Such cells are used for a stack pointer, data pointer, etc.

FIG. **7.09010106** is a circuit drawing showing details of construction of the ALU memory address register "alumar" included in the ALU bit.

FIG. **7.09010107** is a circuit drawing showing details of construction of the ALU slave cell "aluslave" for the ALU adder "aluadd."

FIG. **7.09010108** is a circuit drawing showing details of construction of the ALU adder "aluadd" included in the ALU bit.

FIGS. **7.0902**AA–BD provide a circuit drawing for an ALU high byte "alubyth" which functions similarly to the ALU low byte "alubyt**1**." Two ALU bytes are provided so that sixteen bit commands can be processed.

FIGS. **7.090201**AA–AC provide a circuit drawing of a bit "alubith" included in the ALU high byte "alubyth."

Details of Low Power Dormant Mode

It is sometimes desirable to prevent the integrated circuit **16** from responding to commands from an interrogator. For example, after communication with a particular device **12**, it is sometimes desirable to prevent that particular device **12** from responding to a subsequent interrogation that is intended for a different device **12**. If, for example, the device **12** is used in connection with an access gate, after an interrogator has read a badge containing the device **12** as a controlled access point is passed, the interrogator no longer has a need to communicate with that badge. The interrogator instead would want to pick up subsequent badges passing through the access gate. In addition, when the interrogator no longer has a need to communicate with a particular device **12**, it is desirable that the device **12** stay in the sleep mode to conserve battery power.

In one embodiment, the device **12** is put into an unresponsive state by using a counter which is set to a desired time via a radio frequency command. The device will then not respond to Identify commands (described below in greater detail) used by an interrogator to request information from a device **12**. In this embodiment, the unresponsive state can be cancelled by a radio frequency command. However, this embodiment is disadvantageous in that the device must wake up to process incoming commands and abort if the command is an Identify command. This consumes battery capacity.

In a preferred embodiment, the device **12** can be placed in a dormant mode via a radio frequency command. The dormant mode cannot be cancelled. When in the dormant mode, the device **12** does not wake up to look for incoming commands.

FIGS. **7.10**AA–CC provide a circuit drawing of a timed lock out divider "tld." The timed lock out divider takes as an input the low power clock which is the same clock that sets the wake up interval for the integrated circuit **16**. The timed lock out divider provides two functions. The timed lockout divider provides an alarm timer function, and provides a timed lockout function which is used for the dormant mode function and for the timed lockout of Identify commands.

The alarm timer is set to go off in intervals, such as about every one minute. As an alarm timer, the timed lock out divider causes the integrated circuit **16** to wake up and check for threshold violations in alarm mode. Such threshold violations would be triggered by analog sensors such as temperature sensors, magnetic sensors, etc.

The timed lock out divider also allows, by RF command from an interrogator, a user to disable a device **12** to make it not respond for a prescribed period of time (i.e., allows the user to place the device **12** in the dormant mode). The prescribed period of time can be set in various increments. For example, in the illustrated embodiment, the increments are one second increments from one up to 255 seconds.

When in the dormant mode, the device **12** does not periodically switch to the receiver on mode to check for the presence of radio frequency commands. Therefore, power is conserved.

This dormant mode function is useful for the same reasons that the cancellable timed disabling is useful. If, for example, the device **12** is used in connection with an access gate, after an interrogator has read a badge containing the device **12** as a controlled access point is passed, the interrogator no longer has a need to communicate with that badge. The interrogator instead would want to pick up subsequent badges. Therefore, the interrogator can instruct the device **12** to not respond for a certain time, so as to prevent an unwanted response of a device **12**, after having communicated with that device **12**, but with increased power savings over the cancellable timed disabling. Because wake ups are disabled, current consumed by the device **12** is very low; e.g., 1 μA.

FIG. **7.1001** provides a circuit drawing showing details of construction of a timed lock out divider cell "tldcel" included in the timed lockout divider "tld."

FIGS. **7.11**AA–AB provide a circuit drawing of a timed lock out register "tloreg." This register acts as a down counter and is selectively set with the desired lockout time, from 1 to 255 seconds.

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FIGS. **7.1101**AA–AC provide a circuit drawing of a timed lock out register cell "tlorcel" included in the timed lockout register.

FIGS. **7.12**AA–AC provide a circuit drawing of an read/write control register or output register "oreg." There are a number of these output registers. The output registers allow the processor to send control signals out to various peripheral circuits to cause them to function when required.

FIG. **7.1201** provides construction details of a control register cell "regcell" included in the output register "oreg."

FIGS. **7.13**AA–BA provide a circuit drawing of a status register "sreg." The processor uses the status register to monitor the status of lines supplied from various blocks of circuitry.

FIGS. **7.1301**AA–AB provide a circuit drawing of a status register cell "sregcel" included in the status register.

FIGS. **7.14**AA–AB provide a circuit drawing of a serial input output block "sio." The serial input output circuitry is the data path for data received and for the data to be transmitted. This circuit controls the transfer of the serial stream of data received from the receiver into the processor. The circuit also controls the transfer of the transmit serial data stream from the processor out to the transmitter. The serial input output circuitry comprises two blocks: a block "siodata" that processes data, and a controller "sioctl" that runs the block that processes data.

FIGS. **7.1401**AA–AB provide a circuit drawing of a serial input output data path "siodata." When the integrated circuit **16** is in a transmit mode, data enters the bit registers "sioreg" from the top of the figure, and the data is transferred down to the registers "siobdlat" and "siobdlat_inv" which are the row of blocks second up from the bottom of the figure. The intermediate stages "sioxor" are all exclusive or gates that are used to generate check bits according to the previously mentioned modified Hamming code. The extra five bits "**P0**–**P4**" appended to the eight data bits "**D0**–**D7**" are generated by the exclusive-or gates, and then all thirteen bits are transferred to the registers "sioshr" which are the row of blocks at the bottom of the figure. The thirteen bits are serially shifted out to the right of the figure.

When the integrated circuit **16** is in a receive mode, a reverse sequence takes place. Data is shifted into the thirteen bit registers "sioshr" shown on the bottom of the figure, then transferred up to the registers "siodblat" immediately above the shift registers "sioshr" in the figure. Then the exclusive or circuitry "sioxor" uses the data and the check bits to determine whether there are any errors. If there are any correctable errors, they are corrected at that point. The serial input output data path "siodata" can also detect double bit errors which are not correctable. If a double bit error is detected, a signal is provided at the upper left of the figure to the processor that an uncorrectable error has occurred. Assuming that there is no uncorrectable error, the eight corrected bits are now present as inputs to the top row of registers "sioreg." The eight corrected bits are then transferred in to the top row of registers. From the top row of registers "sioreg," the corrected bits are transferred in parallel to the processor.

FIGS. **7.140101**AA–AB provide construction details of the serial input output register cell "sioreg" included in the serial input output data path "siodata."

FIGS. **7.140102**AA–GF provide construction details of the serial input output exclusive or circuit "sioxor" included in the serial input output data path "siodata."

FIGS. **7.140103**AA–AB provide construction details of the bidirectional latch "siobdlat_inv" included in the serial input output data path "siodata."

FIGS. **7.140104**AA–BB provide construction details of the shift register "sioshr" included in the serial input output data path "siodata."

FIGS. **7.140105**AA–AB provide construction details of the bidirectional latch "siobdlat" included in the serial input output data path "siodata."

FIGS. **7.1402**BA–EI provide a circuit drawing of the previously mentioned control logic "sioctl." The control logic "sioctl" generates all the clocking and the signals that control when data is transferred from register to register.

FIGS. **7.140201**AA–BB provide a circuit drawing showing construction details of the counter bit "siocbit" included in the control logic "sioctl."

FIGS. **7.15**AA–EC provide a circuit drawing of a data interleaver "dil." In a number of modulation schemes used or selectively used by the integrated circuit **16**, differential encoding is employed. Use of differential encoding in the integrated circuit **16** makes possible a simpler receiver in the interrogator. However, if an error occurs in the process of differential encoding, it necessarily corrupts two adjacent bits. The modified Hamming code cannot correct errors where two adjacent bits are in error. This problem is solved by interleaving two bytes. Bit by bit, the first bit of one byte is shuffled next to the first bit of another byte and so on through all thirteen bits. This way, when differential encoding is performed, which may possibly create two adjacent errors, the two bytes are deinterleaved and separated at the receiver so that the bytes are in separate error corrective words. The errors can then be fixed.

The data interleaver works by shifting data in from a data input "SIOTXD" (on the upper left of FIGS. **7.15**AA–EC). Twenty-six bits are shifted into the registers "dil_sreg" shown along the top of FIGS. **7.15**AA–EC, then all twenty-six bits are simultaneously shifted to the lower registers "dil_plsreg" and scrambled in order simultaneously by wiring interconnections between the registers "dil_sreg" and the registers "dil_plsreg" shown in FIGS. **7.15**AA–CC. Thus, a new interleave order is generated on transfer from the registers "dil_sreg" to the registers "dil_plsreg." Then, the contents of the registers "dil_plsreg" are shifted out (to the right in the view of FIGS. **7.15**AA–EC) in a serial, bit by bit fashion, through line "DILTXD."

FIGS. **7.1501**AA–CA provide a circuit drawing showing construction details of the shift register "dil_sreg" included in the data interleaver "dil."

FIGS. **7.1502**AA–CA provide a circuit drawing showing construction details of the parallel load shift register "dil_plsreg" included in the data interleaver "dil."

FIG. **7.150201** provides a circuit drawing showing construction details of a shift register bit "dil_sregbit" included in the parallel load shift register "dil_sregbit" and in the shift register "dil_sreg."

FIGS. **7.16**AA–CD provide a circuit drawing of a convolutional encoder "conv." In the illustrated embodiment, convolutional encoding is disabled. However, in one embodiment, convolution encoding is provided. The circuitry of FIGS. **7.16**AA–CD performs more functions than just convolutional encoding. The circuitry of FIGS. **7.16**AA–CD also includes a preamble generator. In one embodiment, a series of zeros are generated as a preamble. However, in the illustrated embodiment, a pattern of alternating zeros and ones (0101) is generated for DPSK backscatter. The circuitry of FIGS. **7.16**AA–CD also includes a clock for the SIO "sio."

FIG. **7.1601** provides a circuit drawing showing construction details of a shift register cell "convshr" included in the convolutional encoder "conv."

FIG. **7.1602** provides a circuit drawing showing construction details of a summer "convsum" included in the convolutional encoder "conv."

FIGS. **7.17**AA–BB provide a circuit drawing of a shift register data multiplexor "shdcel." The shift register data multiplexor provides a port into the processor. It does a selection among eight sources on the integrated circuit **16**, and connects only one of them for shifting of data for transfer into the A register.

FIGS. **7.18**AA–CC provide a circuit drawing of a digital port output controller "doutport." The device selectively reads data via a digital port in response to a radio frequency command, instead of by radio frequency reception, and the device selectively writes data via a digital port in response to a radio frequency command, instead of by radio frequency. The digital port output controller circuit controls these functions. The digital port output controller circuit also includes a clock in order to synchronize the transfer of the data in either direction (input or output).

The RF processor "rfproc" shown in FIGS. **6**AA–EK contains the receiver **30**, the transmitter **32**, the clock recovery and data recovery circuit **38**, and the wake up timer and logic circuit **36**. The RF processor "rfproc" is shown in greater detail in FIGS. **8**AA–CB.

FIGS. **8**AA–CB provide a circuit drawing of a RF processor "rfproc." The RF processor "rfproc" includes a receiver "rx" (which is the receiver **30** of FIGS. **6**AA–EK), a transmitter "tx" (which is the transmitter **32** of FIGS. **6**AA–EK), a low power frequency locked loop "lpfll," a counter bit "lpfll_cbit," a receiver wake up controller "rxwu" (which is the wake up timer and logic circuit **36** of FIGS. **6**AA–EK), and a digital clock and data recovery circuit "dcr" (which is the clock and data recovery circuit **38** of FIGS. **6**AA–EK). Thus, RF processor "rfproc" includes the clock that sets the wake up interval, as well as logic that performs tests on the incoming signal to see whether the incoming signal is a valid signal such that the integrated circuit **16** should stay awake.

FIGS. **8.01**AA–DE provide a circuit drawing of the receiver "rx" included in the RF processor. In the illustrated embodiment, the receiver "rx" includes a Schottky diode detector "diodedet." In the illustrated embodiment, the Schottky diode detector "diodet" is an inductorless Schottky diode detector. Instead of employing inductors in the diode detector to supply bias current to the diode, the diode detector includes a current source which drives current through both an antenna and a Schottky diode included in the detector. The inductorless Schottky diode detector is described in more detail below. FIGS. **8.01**AA–DE also illustrate a CMOS detector "cmosdet" that is used in accordance with an alternative embodiment, but which is not used in the illustrated embodiment. The output of the Schottky diode detector is applied through a series of AC coupled amplifiers. More particularly, in the illustrated embodiment, the Schottky diode detector is applied through amplifiers "videoamp**1**," "videoamp**2**" replicated four times, and then into a comparator. The function of the comparator is to put out a full digital signal. The output of the comparator is a base band digital representation of the command that was sent by the interrogator.

A base band signal is a signal without a carrier frequency present. The output of the comparator is a signal that is the equivalent of the signal that was used to modulate the carrier back at the interrogator.

The receiver "rx" includes a RF detect circuit "rxdetect." The RF detect circuit determines when a modulated radio frequency signal is present at the receiver and the output of the receiver is switching between high and low states. The receiver "rx" includes a bias block "rxbias" that provides currents to the various amplifiers "videoamp**1**," "videoamp**2**," etc. The receiver "rx" further includes logic that bypasses the receiver when a user selects not to use RF for an input, but rather to provide a base band input signal directly in digital form. The user may make the selection to bypass the receiver, for example, for testing or exercising the integrated circuit **16**. The user may also make the selection in applications where the receiver portion of the chip is not required, but the integrated circuit **16** is used to transmit information (e.g., for periodic transmissions).

Schottky Diode RFID Detector

Overview

For purposes of realizing a cost effective and low power radio frequency receiver on an RFID tag, a simple Schottky diode receiver is utilized. The receiver is formed from a Schottky diode detector, an amplifier, and the receiving antenna "rxantenna". With the implementation of a single integrated circuit **16** RFID tag, an easy and low cost technique for configuring the frequency of operation on a tag is needed. Receiver frequency characteristics can be tailored by selecting an appropriately sized antenna to be coupled to the integrated circuit **16** that supports the Schottky diode detector. Furthermore, adjustment of bias current across the Schottky diode can be used to realize a desired resistance there across, enabling tuning or detuning of the receiver.

For purposes of enabling simplified representation, FIG. **29** illustrates a simplified circuit schematic for one embodiment of a receiver **80** having a Schottky diode detector **84** and antenna **44**.

The detector **84** includes a Schottky diode **86** having an anode connected to the antenna **44** and having a cathode.

The exemplary antenna **44** is formed from a loop or folded dipole construction. The antenna **44** performs band pass filtering.

The detector **84** further includes an ideal current source **88** connected to the cathode of the Schottky diode **86** and driving current through the antenna and Schottky diode **86** in the direction from the anode to the cathode. The current source **88** is an ideal current source, and is configured to forward bias the Schottky diode **86**, realizing a desired resistance (or impedance) in the process.

The detector **84** further includes a capacitor **90** connected between the cathode of the Schottky diode **86** and ground. The capacitor **90** provides a radio frequency short to ground so that all radio frequency voltage appears across the Schottky diode **86**. This maximizes a base band signal produced by the Schottky diode **86**.

The detector **84** further includes a capacitor **92** having a first terminal connected to the cathode and having a second terminal defining an output of the detector **84**. The capacitor **92** provides an AC short to video frequency, and defines the output of the detector **84**. The capacitor **92** allows different bias levels in the detector and at the input of a video amplifier connected to the output of the detector **84**. Details of the actual circuit implementation on integrated circuit **16** (of FIG. **5**) will be discussed below with reference to FIGS. **5**, **8**AA–CB, **8.01**AA–DE, **8.0101**AA–CB, **28**, **29**, and **30**.

Antenna Implementation

Preferably, the antenna "rxantenna" is constructed and arranged to form a folded dipole antenna, consisting of a continuous conductive path, or loop of microstrip. The terminal ends of the antenna **44** loop each form a conductive lead that electrically interconnects with the integrated circuit **16** of FIG. **5**. According to the actual circuit layout of FIG. **6**, antenna "rxantenna" is connected to the integrated circuit

16 via the exposed conductive bonding pad labeled "rxantenna—Pad D". Alternatively, the antenna can be constructed as a continuous loop antenna. In this case, the antenna is constructed from a continuous piece of conductive microstrip configured in the shape of a square or circle to form a loop antenna.

In assembly, antenna **44** (as well as antenna **46**) is depicted in electrically conductive and bonded relationship with "rxantenna—Pad D," shown on the integrated circuit **16** of FIG. **6**. Similarly, antenna **46** is bonded to "txantenna—Pad AA". The preferred assembly technique, discussed below, involves a flip-chip epoxy bonding technique wherein the antennas **44** and **46** of FIG. **5** are actually printed onto the back face of the plastic card or carrier (e.g. card **11** of FIG. **2** and stamp **20** of FIG. **3**), after which the integrated circuit **16** is bonded to the antenna, as well as to the battery, using a conductive epoxy.

Preferably, the antennas **44** and **46** are printed onto the back side of the card or stamp, forming each microstrip loop antenna thereon. For example, the antenna can be silk screened onto the card with a conductive polymer thick film. Alternatively, a conductive silver filled epoxy can be used. Alternatively, the antenna can be formed from a separate piece of conductive material, for example, from a piece of wire or conductive ribbon that is glued to the back of the card.

One exemplary technique for assembling the postage stamp **20** of FIG. **4** is provided here below. The same technique can be used to assemble the badge **10** of FIG. **2**, or any other similarly constructed tag having a rigid support or substrate similar to plastic cards **11** and **21**. First, antennas **44** and **46** (of FIG. **5**) are mounted to a back face of the card. Preferably, the above elements are simultaneously printed onto the back of a large sheet of plastic with a conductive silver printed thick film, after which the cards are individually separated, or cut from the sheet. Pads on the integrated circuit **16** form enlarged connection points for electrically bonding each antenna **44** and **46** to "rxantenna—Pad D" and "txantenna—Pad AA" of FIG. **6** and for connections to a power supply. Next, the card is positioned front face down onto a rigid support plate. Then integrated circuit **16** (of FIG. **4**) is mounted to the pads with conductive beads of epoxy. Finally, the battery **18** is bonded along its bottom face with a bead of conductive epoxy, after which conductive epoxy is used to electrically connect the opposite terminal or top of the battery with a corresponding conductive die pad.

Subsequently, a metal dam sized to conform generally to the outer peripheral shape of the card **20** is placed over the back of the card. The dam functions as an outer template while a thin layer of non-conductive epoxy (not shown) is applied to the back of the card **20**, preferably hermetically sealing in the integrated circuit **16**, antenna and battery. Preferably, the thin coat of epoxy consists of a coating, barely thick enough to cover over the components forming the device. One benefit provided by this construction technique is the elimination of any visible bumps in the tag which can result when constructing the tag by heat sealing two or more pieces of plastic card together to trap the device **12** therein. However, a lesser preferred construction of this invention envisions forming the tag, e.g. badge **10**, stamp **20**, or some other tag, with such a heat sealed sandwich of plastic cards.

Preferably, the above technique for mounting integrated circuit **16** to card **20** (of FIG. **4**) consists of a flip-chip mounting technique. One example of a flip-chip mounting technique is disclosed in pending U.S. patent application Ser. No. 08/166,747, "Process of Manufacturing an Electrical Bonding Interconnect Having a Metal Bond Pad Portion and Having a Conductive Epoxy Portion Comprising an Oxide Reducing Agent," listing Rick Lake and Mark E. Tuttle as inventors, now U.S. Pat. No. 5,480,834 and incorporated herein by reference.

Integrated Circuit Implementation

According to FIG. **8**, the Schottky diode detector "diodet" is configured within receiver "rx" to receive radio frequency signals via receiving antenna "rxantenna". One exemplary receiving antenna configuration is depicted in FIG. **5**, denoted generally by reference numeral **44**. In operation, the Schottky diode detector and the receiving antenna cooperate to form a tunable receiving circuit. Signals detected by the Schottky diode detector are input to a five stage amplifier, then a comparator, for further signal conditioning. The output of the comparator is a digital representation of the received baseband signal.

As shown in FIG. **8**, receiver "rx" is an Amplitude Shift Keying (ASK) receiver. This is also known as an AM receiver. The illustrated embodiment employs On Off keying (OOK) wherein a digital one ("1") is represented by the presence of the RF carrier, and wherein a digital zero ("0") is represented by the absence of the carrier.

FIGS. **8.01**AA–DE illustrate in greater detail the circuit implementation of receiver "rx". According to this embodiment, Schottky diode detector "diodedet" receives input signals via an input "rxantenna," and bias voltages for the current source via a pair of inputs "bias**1**" and "bias**2**". A pair of output signals "OUTN" and "OUTP" leave "diodedet" for input to a serially connected chain of amplifiers, and a comparator. The array of amplifiers comprise five video amplifiers, labeled "videoamp**1**" and "videoamp**2**". Bias voltages are applied to "bias**1**" and "bias**2**" via "rxbias," a bias circuit which generates all bias voltages required by the receiver.

A circuit "rxdet" shown in FIGS. **8.01**AA–DE receives the output signal from the comparator, via combinational logic, with "digrxdata" and "digrx". The output signal "RFDET" is driven high if there is a signal at the output of the comparator. The resulting signal input into "rxdet" is received via "dataIn." Additional inputs to "rxdet" include "lowrate," "Vref," "Vbias**1**," "Vbias**2**," "Vreg," and "enable." Further details of "rxdet" are disclosed below with reference to FIGS. **8.0106**AA–CD, entitled "RF Detect".

FIGS. **8.0101**AA–CB illustrate one embodiment for realizing the Schottky diode detector "diodedet" of FIGS. **8.01**AA–DE. Namely, a Schottky diode is forward biased from receiving antenna, coupled at "ANT," to a detector output "OUTP." A second Schottky diode is forward biased from Vdd to a detector output "OUTN." Two current sources are formed by four transistors, and are driven by bias voltages at "bias**1**" and "bias**2**." A capacitor is coupled to Vss, between each Schottky diode and associated output, "OUTP" and "OUTN," respectively. Furthermore, an array of parallel capacitors are provided in series between each Schottky diode and associated output, "OUTP" and "OUTN," respectively. The array of parallel capacitors acts as a single capacitor. Each Schottky diode is formed from an array of Schottky diodes. In order to use standard contact hole sizes, each Schottky diode is formed from an array of Schottky diodes connected together in parallel to act as a single Schottky diode.

According to FIGS. **8.01**AA–DE, "OUTP" and "OUTN" are input into a multiple (e.g., five) stage amplifier and into a comparator. In order to avoid amplification of substrate noise, a differential amplifier is employed for each stage of the multiple stage amplifier. Noise appears equally on both

inputs of each differential amplifier, and, the common mode rejection of the differential amplifiers impedes transmission of substrate noise. The differential amplifiers amplify a received baseband signal up to a digital level. A dummy Schottky diode (the lower Schottky diode in the figures) is connected to the second input of the first differential amplifier.

Details of Realization of Wide Carrier Frequency Bandwidth

In order to meet the wide range of intended applications, it is desirable to construct the integrated circuit for an RFID tag to realize operation of a wide range of carrier frequencies. For example, several desirable carrier frequencies for the device disclosed in FIGS. **5** and **6** are 915, 2450, and 5800 MegaHertz bands. Frequency selectivity is realized in the device of FIGS. **5** and **6** by appropriately configuring external antennas and internal circuit components of the integrated circuit. For the case of a single integrated circuit with an active on-board transmitter, it is necessary to design circuit components into the integrated circuitry prior to mounting and encapsulation of the integrated circuit with an antenna inside of a package. Hence, the circuit components needed to facilitate tailoring of the carrier frequency must be "designed in" the integrated circuit. In the case of a backscatter transmitter, components included in the integrated circuit can be selected so as to allow operation over a wide range of carrier frequencies, the selection being made by choice of antenna.

According to FIGS. **8**.**01**AA–DE, the number of amplifiers that need to be implemented via "videoamp**1**" and "videoamp**2**" is determined based upon the magnitude of the minimum detected signal and the required signal to noise (S/N) ratio. Amplification is sufficient to produce full digital levels at the output of the comparator.

The capacitor configured to ground in the video receiver circuit of FIG. **29** (and FIGS. **8**.**0101**AA–CB) is used to separate the radio frequency (RF) from the "VIDEO AMP" side of the video receiver circuit. The capacitor is sized to impart an effective short circuit to ground at radio frequency, thereby ensuring that all of the radio frequency (RF) voltage appears across the Schottky diode terminals. Additionally, the capacitor should be sized small enough at video frequencies, so that the capacitor does not load down the video amp circuit.

The capacitor configured in series in the video receiver circuit of FIG. **29** (and FIGS. **8**.**0101**AA–CB) is used to block out the DC component of a voltage to "VIDEO AMP" while retaining the AC component. In this manner, the series capacitor forms a "blocking" capacitor or "coupling" capacitor.

Details of Inductorless RF Detector

A second desirable feature for the integrated circuit of an RFID tag is to eliminate the need to use inductors when constructing the Schottky diode detector. One technique for providing a bias current to a Schottky diode is disclosed in FIG. **28**. FIG. **28** illustrates a receiver **60** including an antenna **62** and a Schottky diode detector **64**. The receiver **60** includes inductors **68** and **70** used to provide the bias current via voltage source **74** with this implementation. A capacitor **76** is shunted to ground, and a second capacitor **78** is placed in series, providing AC coupling to the video amplifier. Several variations of such inductor-based bias current implementations are described in a paper entitled "Designing Detectors for RF/ID Tags," by Raymond W. Waugh of Hewlett-Packard Company, submitted for presentation at the RF Expo, San Diego, Feb. 1, 1995, and which is already incorporated by reference. Inductors are required in all of these constructions, but their implementation on an integrated circuit proves difficult because of problems inherent in forming inductors in an integrated circuit. The circuit in FIG. **29** eliminates the inductors by biasing the Schottky diode with a high impedance current source. A current sink is provided by connecting the far end of the antenna to Vdd.

Details of Elimination of Overdrive Problem

The Schottky diode detector circuit implementation of FIGS. **8**.**0101**AA–CB realizes a technique for negating the effect of high power radio frequency (RF) input levels on the Schottky diode detector. More particularly, when high level radio frequency (RF) power is present at the antenna "rxantenna," e.g. when the RFID tag antenna is close to the transmitting antenna of an interrogator, the signal present on node "A" of FIG. **29** becomes large. For example, the signal on node "A" could be several hundreds of millivolts. The rising and falling edges of the detected signal are controlled by two separate time constants which are very different, as shown in FIG. **31**. As shown by the high power signal of FIG. **31**, the high power signal has a rising edge which is fast, or has a very steep, nearly vertical slope. The nearly vertical slope of the rising edge results because the rising edge is controlled by the effective resistance of the Schottky diode (about 1 kOhm) multiplied by the capacitance of capacitor **90** (Crf) (about 1–10 pF). Hence, the resulting time constant is about 1 to 10 nanoseconds.

In contrast, the falling edge of the detected signal in FIG. **31** is controlled by the current source **88** as it discharges capacitor **90** (Crf), which takes approximately 100 nanoseconds. As a result, the voltage waveform at node "A" is distorted. According to the amplified digital version of the signal, shown in FIG. **31**, the signal in the high power case is distorted by the unequal rise and fall times. The onset of each fall for the digital version is triggered at the cross-over point, which deviates substantially from that of the low power signal. Such a distortion poses a serious problem for implementing clock recovery schemes, which rely on accurate edge-to-edge timing.

To overcome the above-mentioned problem, the integrated circuit **16** of FIG. **6** uses only rising edges for clock recovery. Hence, the distorted falling edges are avoided altogether. As becomes apparent from viewing the amplified digital signal of FIG. **31**, rising edge to rising edge timing is not affected by the slow falling edges. Therefore, the clock can be accurately recovered.

FIG. **30** illustrates a circuit **93** including a Schottky diode detector **94**, and an antenna **44** connected to the Schottky diode detector **94**. More particularly, in the illustrated embodiment, the Schottky diode detector **94** includes a Schottky diode **96** having a cathode connected to the antenna **44** and an anode. The Schottky diode detector **94** further includes a current source **98** driving current in the direction from the anode to the cathode of the Schottky diode **96** and through the antenna **44**. The Schottky diode detector **94** further includes a capacitor **100** connected between the anode of the Schottky diode **96** and ground; and a capacitor **102** connected between the anode of the Schottky diode **96** and an output of the diode detector **94** which is connected to an amplification circuit. The same technique used with respect to FIG. **29** can also be implemented for the Schottky diode detector circuit of FIG. **30**. However, for this case, only the rising edges are significantly distorted, since the Schottky diode is reversed in direction. Therefore, only the falling edges are used in clock recovery.

Details of Method of Forming an IC Schottky Structure

A method of forming a Schottky structure that can be employed to manufacture the Schottky diode detector will now be described. A Schottky diode is a diode in which a

metal and a semiconductor form a pn junction. Electrons injected into the metal have a higher energy level than the charge carriers in a semiconductor, and energy storage at the junction is low because current flow is not accompanied by hole movement.

One embodiment of the invention comprises a Schottky diode **220** including an n+ region **222** generally encircling or surrounding an n-well region **224** (FIG. **41**). In the illustrated embodiment, the n+ region **222** is heavily doped; e.g., 1×10^{18} atoms/cm^3 or greater of n-type material, and the n-well region **224** is lightly doped; e.g., 1×10^{17} atoms/cm^3 or lower of n-type material. The n-well region **224** defines a contact area **226**, and the n+ region **222** provides a low resistance interconnect to the Schottky diode **220**. The n+ region **222** has a diffused edge **228**, and the n-well region has a contact edge **230**. The distance from the n+ region diffused edge **228** to the n-well region contact edge **230** is minimized. In one embodiment, the distance from the n+ region diffused edge **228** to the n-well region contact edge **230** is less than twenty micrometers. In a more preferred embodiment, the distance from the n+ region diffused edge **228** to the n-well region contact edge **230** is about two micrometers.

More particularly, the integrated circuit **16** includes a grid pattern of n+ regions **222**. Each region **222** generally encircles or surrounds isolated n-well regions **224** of a large common n-well region **232** under the n+ regions **222** (FIGS. **41** and **42**). This provides for parallel connection of a selectable number of Schottky diodes **220**. As described elsewhere, the parallel connection of Schottky diodes **220** acts a single Schottky diode, and allows use of standard sized contact holes. The number of Schottky diodes **220** connected together is selectable to tailor resistance, parasitic capacitance, and electrostatic discharge sensitivity for a specific application.

To form the grid of Schottky diodes **220**, the following process steps are performed.

First, a p– substrate **234** is provided (FIG. **38**). Next, n-well region **232** is defined relative the substrate **234**. Next, an insulator **236** is formed over the n-well region. In one embodiment, the insulator **236** is borophosphosilicate glass (BPSG).

Next, a removal or etching step is performed to remove areas of the insulator **236** for definition of contact holes **238**, and areas **240** generally encircling or surrounding the contact holes **238** (FIG. **39**). The contact holes **238** are not necessarily circular in cross-section; any cross-sectional shape is possible. Similarly, any cross-sectional shape is possible for the areas **240** surrounding the contact holes **238**. In a preferred embodiment, the contact holes **238** all have the same diameter (or peripheral extent) to facilitate subsequent filling of the contact holes **238** (described below in greater detail). In an alternative embodiment, different contact holes **238** have different sizes. In the process of the illustrated embodiment, the contact holes **238** do not need to be completely filled with a conductor, and all contact holes therefore do not need to be the same size.

In the illustrated embodiment, the n+ regions **222** are formed in the n-well region **232** by diffusion after the etching has been performed, via the openings **240** surrounding the contact holes **238**. The n+ regions **222** can be formed by other processes or in other sequences. For example, the n+ regions **222** can be formed before the insulator **236** is formed over the n-well region **232**.

Next, a Schottky forming metal **242** such as titanium is formed in the contact hole openings. In the illustrated embodiment, the Schottky forming metal is deposited on the surface of n-well regions **224** via the contact hole openings **238**. In one embodiment, the thickness of the deposited metal is about 200 Å. The metal is annealed to form a stable silicide interface to the n-well silicon.

If it is desired to fill the contact holes, a material such as tungsten **246** may be deposited into the contact holes (FIG. **40**). The tungsten is then planarized to form final contact structures (FIG. **41**).

Then, an interconnect metallization step is performed (FIG. **42**). For example, copper doped aluminum **248** is deposited (e.g. sputtered) over the wafer, then the wafer is masked and etched to remove unwanted areas. The mask defines a pattern to interconnect the contacts as desired.

A variable number of Schottky diodes may be connected in parallel by simply changing the metal masks and interconnecting only the number of Schottky diodes required by a particular circuit application. In one illustrated embodiment, an array of twelve by twelve Schottky diodes (144 total Schottky diodes) is provided (FIG. **43**). In another embodiment (FIG. **42**), less than all available Schottky diodes are connected together. In one embodiment, only a six by six array (36 Schottky diodes) is connected together in parallel.

In one alternative embodiment, aluminum is employed instead of tungsten and silicide. In another alternative embodiment, tungsten is employed instead of aluminum to interconnect contacts, and the step of forming tungsten plugs is omitted.

In an alternative embodiment (FIG. **47**), each Schottky diode includes a p+ region **252** encircling a "p–" p-well region **254** and is formed by a method substantially identical to the method described above except with p-type material substituted for n-type material and vice versa. More particularly, in this alternative embodiment, the following steps are performed.

First, an n-type substrate **256** is provided (FIG. **44**). Next, a common p-well region **258** is defined relative the substrate **256**. The common p-well region **258** defines the p-well regions **254** for each of the Schottky diodes. Next, an insulator **260** such as borophosphosilicate glass (BPSG) is formed over the p-well region **258**. Next, an etching step is performed to etch away regions of the insulator for definition of contact holes, and areas **264** generally encircling or surrounding the contact holes (FIG. **45**). In a preferred embodiment, the contact holes **262** all have the same diameter (or peripheral extent) to facilitate subsequent filling of the contact holes **262** with Tungsten or another conductor. In an alternative embodiment, different contact holes **262** have different diameters. In the process of the illustrated embodiment, the contact holes do not need to be completely filled, and all contact holes therefore do not need to be the same size.

In the illustrated embodiment, the p+regions **252** are formed in the p-well regions by diffusion after the etching has been performed, via the openings **264** encircling the contact holes. The p+regions **252** can be formed by other processes or at other times. For example, the p+regions **252** can be formed before the insulator is formed over the p-well region **258**.

Next, a Schottky forming metal **266** such as Titanium is formed in the contact hole openings **262**. In the illustrated embodiment, the Schottky forming metal **266** is deposited on the surface of the p-well region **258** via the contact hole openings **262**. In one embodiment, the thickness of the deposited metal is about 200 Å. The metal **266** is annealed to form a stable silicide interface **268** to the p-well region **258**.

If it is desired to fill the contact holes **262**, a metal such as tungsten **270** is deposited into the contact holes (FIG. **46**). The tungsten **270** is then planarized to form final contact structures.

Then, an interconnect metallization step is performed (FIG. **47**). For example, copper doped aluminum **272** is deposited (e.g. sputtered) over the wafer, then the wafer is masked and etched to remove unwanted areas. The mask defines a pattern to interconnect the contacts as desired.

The above described processes for forming a Schottky diode are preferred over a process wherein, after the contact holes a etched, ion implantation of phosphorus into the holes is performed. In such a process, the implant would be a two step process, with a low energy implant (e.g., 35 keV of 4×10^{12} ions/cm^2) followed by a high energy implant (e.g., 120 keV of 4×10^{12} ions/cm^2). Such implants cause a high doping level at the bottom of the contact hole, which prevents formation of a low leakage Schottky diode. The preferred processes described above eliminates these two contact implants, and allows for formation of a good quality Schottky diode.

FIGS. **8.0101**AA–CB provide a circuit drawing of the Schottky diode detector "diodedet." FIGS. **8.0101**AA–CB actually show two Schottky diode detectors. The lower Schottky diode detector shown in FIGS. **8.0101**AA–CB is a replicated or dummy detector which generates a signal for the compliment side of the differential amplifier "videoamp**1**." The structure of the dummy Schottky diode detector is similar to the real Schottky diode detector so that any noise coupled through ground or possibly through Vdd is replicated on both sides of the differential amplifier "videoamp**1**" and so that the common mode rejection of the amplifier will result in little noise making it through the amplifier chain. Bias current to the Schottky diode detector is provided by the current source transistors having gates connected to "BIAS**1**" and "BIAS**2**" respectively. A path for that current is through the antenna. Thus, the antenna is biased to a high potential Vdd. The array of capacitors in FIGS. **8.0101**AA–CB is a series capacitance that couples the output of the Schottky detector to the input of the video amp "videoamp**1**" and allows an independent bias level to be set at the input of the video amp "videoamp**1**." The value of that capacitor in conjunction with the effective resistance seen looking into the amplifier "videoamp**1**" determines the high pass response of the amplifier "videoamp**1**." The values of the capacitor and effective resistance determine the lowest frequency at which the amplifiers can respond, and that frequency is selected to be low enough so that none of the information contained in the base band signal is lost.

FIGS. **8.0102**AA–BD provide a circuit drawing of the CMOS detector "cmosdet" which is employed in an alternative embodiment.

Details of Quick Bias AC-Coupled Video Amplifier

FIG. **48** provides a simplified circuit schematic of a quick bias AC-coupled video amplifier **270**. The video amplifier goes from a power down (unbiased) state to a fully biased state quickly despite a large value effective resistance and capacitor used to bias and couple the amplifier.

The video amplifier **270** has an input adapted to be connected to V_{in} and includes coupling capacitors **292** and **294** at the input.

The video amplifier includes a voltage divider **276** including two resistors **278** and **280** in series, and four transistors **282**, **284**, **286**, and **288** shown to the right of a voltage divider in FIG. **48**. Transistors **286** and **288**, the rightmost two of the four transistors, are long L (length), narrow W (width) p-channel devices operated in linear mode to provide very high effective resistance R_{EFF}. Transistors **286** and **288** are used instead of resistors because it is hard to provide high resistances using resistors without generating undesirable parasitic capacitance and without taking up more space on an integrated circuit die. The video amplifier **270** includes a differential amplifier **290**. The voltage divider **276** sets a bias voltage at the inputs of the differential amplifier **290**. The effective resistance R_{EFF}, in conjunction with the value of coupling capacitor **292** or **294**, sets the angular high pass roll off frequency for the amplifier according to a relationship of $\omega_{HP}=1/((R_{EFF}+R1\|R2)C1)$ where ω is angular frequency (2π times frequency), R1 and R2 are the values of the resistors **278** and **280** included in the voltage divider **276**, and C1 is the value of one of the coupling capacitors. The values of R_{EFF}, and the coupling capacitors are adjusted to achieve the desired high pass roll off frequency ω_{HP} as illustrated in FIG. **49**. The high pass roll off frequency determines what frequencies will be amplified or attenuated. The high pass roll off frequency is set low enough so that important data is not excluded.

In many applications, the values of these components are high. For example, in the integrated circuit **16**, REFF is approximately two MegaOhms, and the capacitance of each of the coupling capacitors **292** and **294** is approximately one picoFarad, which gives an angular high pass frequency of approximately 1/((2 MegaOhms)(1 pF))=500 kiloradians/second, or a high pass frequency of $500/2\pi$=79.6 kHz.

In a powered down state, input Vreg is zero. Upon power up, there is a delay before the inputs reach the desired bias voltage, according to a relationship $V_{BIAS}=R1/(R1+R2)V_{reg}$. The time constant equals $R_{EFF}C1$ which is approximately equal to two microseconds.

If it is decided to wait five time constants, this requires about ten microseconds.

In accordance with the invention, transistors **282** and **284** are added (the two leftmost transistors of the four). These are short L (length) wide W (width) devices which allow the bias voltage to be established in much less time by shorting around the high resistance of the right two transistors **286** and **288**. The time constant is thereby reduced. This shorting occurs when an input RXEN is low. Before using the circuit as an amplifier, RXEN is taken high (after bias voltage is achieved). This restores the desired frequency behavior.

FIGS. **8.0103**AA–CF provide a circuit drawing of the video amp "videoamp**1**." The video amp "videoamp**1**" is a differential amplifier with a cascode device isolating a resistor load from differential transistors of the amplifier. This lowers capacitance and improves the frequency response of the amplifier. Bias is provided by a resistor divider shown on the upper left of FIGS. **8.0103**AA–CF, which resistor divider provides a potential to two p-channel transistors found almost in the center of the FIGS. **8.0103**AA–CF. Each of these p-channel transistors defines a very large resistance, effectively on the order of one to two megaOhms connecting to the nodes of the amplifier to provide the bias. The remaining p-channel devices shown left of center in FIGS. **8.0103**AA–CF are shorting devices which short out the two p-channel transistors during the period when the receiver is being powered on out of the sleep mode. The function of these remaining p-channel devices is to cause the inputs to the receiver to come up to the bias level as quickly as possible. They are then shut off in order to leave the circuit with only the high resistance p-channel devices providing the bias. This is necessary from a frequency response standpoint.

FIGS. **8.0104**AA–BC provide a circuit drawing of the video amp "videoamp**2**." The video amp "videoamp**2**" operates in a manner similar to operation of the video amp "videoamp**1**." The video amp "videoamp**1**" has a higher bias current than the video amp "videoamp**2**." The reason for this is to minimize the noise generated in the amplifier.

FIGS. **8.0105**AA–EE provide a circuit drawing of the comparator "comparator." The comparator has biasing considerations similar to the biasing considerations for the video amps, and has a biasing network shown at the left in FIGS. **8.0105**AA–EE, at the inputs, which is similar to the biasing networks in the video amps. The function of the comparator "comparator" is to ensure an output at a full digital level.

FIGS. **8.0106**AA–CD provide a circuit drawing of an RF detect circuit "rxdet." This circuit generates an RF detect signal. The circuit includes an input switch that is either high or low, and a capacitor. If the input switch is high for a sufficient percentage of the time, the input switch will charge up the capacitor. The capacitor has a continual discharge leakage current. As long as the input switch is high sufficiently frequently, the input switch will overcome the capacitor leakage current, and the circuit "rxdet" will put out an RF detect signal.

FIGS. **8.0107**AA–GN provide a circuit drawing showing construction details of the receiver bias generator "rxbias." The receiver bias generator includes a series of current mirrors to produce bias currents for various stages of the receiver.

FIGS. **8.0108**AA–AC provide a circuit drawing showing construction details of a data transition detector "datatx." The data transition detector has an input connected to the digital level output of the comparator "comparator" of the receiver "rx" in FIGS. **8.01**AA–DE. The data transition detector generates a high going pulse every time there is a transition from high to low or from low to high in the data output by the comparator "comparator." These transitions are tested by other circuitry, described below, to determine whether or not a valid signal is being received.

Details of Low Power Frequency Locked Loop

As previously discussed, the integrated circuit **16** periodically checks if a radio frequency signal is being received by the receiver. The integrated circuit **16** includes a timer setting the period for the checking, the timer comprising a frequency locked loop "ipfll."

The low power frequency locked loop "lpfll" is shown in greater detail in FIGS. **8.02**AA–BC. This is also shown in a simplified schematic in FIG. **24**. In the embodiment shown in FIG. **24**, the device **12** includes a frequency locked loop (or phase locked loop) **54**, a divider **55** coupled to the input of the loop **54**, and a divider **56** coupled to the output of the loop **54**. A clock (e.g. 9.54 MHz) that is recovered from an incoming radio frequency command from the interrogator **26** is supplied to the frequency locked loop (or phase locked loop) **54** after being passed through the divider **55**. The terms "phase locked loop" or "frequency locked loop" as used herein are meant to describe physical structure, not a state of operation. The term "locked" does not imply that the circuitry is operating, or functioning in a locked condition. Thus, as used herein, "locked" is a term for assisting definition of a particular circuit configuration and is not meant to imply a required state of operation for the circuit. To avoid ambiguity, the appended claims use the terms "phase lock loop" or "frequency lock loop" instead of "phase locked loop" or "frequency locked loop" to indicate that state of operation is not being claimed.

Phase locked loops and frequency locked loops are similar to one another, except that a phase locked loop tracks phase as well as frequency. A phase locked loop includes a phase detector having a first input receiving the incoming message, having a second input, and having an output; a loop filter having an input coupled to the output of the phase detector and having an output; a voltage controlled oscillator having an input coupled to the output of the loop filter, and having an output defining an output of the phase locked loop; and a divider having an input coupled to the output of the voltage controlled oscillator and having an output connected to the second input of the phase detector. The phase detector produces an output voltage proportional to the phase difference of two input signals. The loop filter is used to control the dynamics of the phase locked loop. The voltage controlled oscillator produces an AC output having a frequency proportional to input control voltage. The divider produces an output signal having a frequency that is an integer division of the input signal. The loop filter includes a capacitor on a control node of the voltage controlled oscillator.

The frequency locked loop **54** includes a frequency comparator **57** receiving the divided recovered clock, an up/down counter **58** connected to the output of the frequency comparator, and a current controlled oscillator **59** connected to the output of the up/down counter. The output of the current controlled oscillator **59** is fed back to the frequency comparator **57**, and to the divider **56**. The divider **56** is programmable (in response to a radio frequency command from the interrogator **26**) in one embodiment of the invention. To conserve power, the loop **54** is enabled only during processing of a command from the interrogator **26**, during which time a recovered clock reference signal is available. In the illustrated embodiment, the current controlled oscillator **59** is a low power current controlled oscillator "lpcco" shown in FIGS. **8.0204**AA–EJ.

FIGS. **8.02**AA–BC provide a circuit drawing of the low power frequency locked loop "lpfll." This circuit generates a clock which is used in multiple places to time the interval between wake ups. The clock is used as a reference for the timed lock out function, and for the alarm timer wake up function. In a preferred embodiment, the low power frequency locked loop "lpfll" generates a 8 kHz clock. The low power frequency locked loop includes a current controlled oscillator "lpcco" that consumes very little current and that runs continuously from the time power is first supplied to the integrated circuit **16** ("power up") until power is removed from the integrated circuit **16**. During power up, the low power frequency locked loop "lpfll" attempts to synchronize to the main clock recovery oscillator "dcr" (described below). However, that oscillator is not calibrated to anything yet because it has just been powered on. Still, an initial frequency is set for the low power frequency locked loop "lpfll." On the first successful communication with an interrogator, the low power frequency locked loop "lpfll" is actually calibrated to a known clock frequency and set to a desired frequency (8 kHz in the illustrated embodiment).

The low power frequency locked loop includes a divider shown at the top of FIGS. **8.02**AA–CB. The divider divides down an input clock signal. In the illustrated embodiment, the input clock signal is a 9.5 MHz clock signal. The input clock signal is divided down by a desired factor to get a reference clock for the actual loop shown at the bottom of FIGS. **8.02**AA–CB. In the preferred embodiment, the reference clock for the loop shown in FIGS. **8.02**AA–CB runs at 8 kHz. The loop receives a loop enable signal "LoopEN", shown at the lower left of FIGS. **8.02**AA–CB. The loop enable signal "LoopEN" enables this frequency locked loop to operate in a loop configuration. The loop enable signal "LoopEN" is asserted when a valid message has been certified and on power up. Those are the only two times the loop enable signal is asserted.

The frequency of the current controlled oscillator "lpcco" is determined by current input into the current controlled oscillator "lpcco." A selection of the number of current steps

for controlling the oscillator is made by the outputs of the up/down counter "udcounter." The up/down counter has outputs select 1 "Sel1," select 2 "Sel2," select 4 "Sel4," and select 8 "Sel8." The outputs of the up/down counter are labelled according to their binary weights, and that is also how currents are rated within the current controlled oscillator. When the loop is disabled, at the end of processing of a valid command, the count on the output of the up/down counter is frozen so that the select 1 through select 8 lines remain constant and they keep that same frequency in the low power frequency locked loop "lpfll" until the next valid command is processed. At the time when the next valid command is processed, if the clock frequency of the low power frequency locked loop has drifted, the loop sets the frequency back to the desired frequency (e.g., 8 kHz).

FIGS. **8.0201**AA–AB provide a circuit drawing showing construction details of a timed lockout divider cell "tldcel_bypass" included in the circuit of FIGS. **8.02**AA–BC.

FIGS. **8.0202**AA–CD provide a circuit drawing of a frequency comparator "freqcomp" of the frequency locked loop "lpfll." The frequency comparator counts a certain number of cycles of the reference clock and also counts how many cycles of the low power clock occurred within that number of cycles. The frequency comparator thus determines whether the low power clock "lpfll" is running too fast, too slow, or on time. If the clock is running too fast or too slow, the frequency comparator makes an adjustment by causing the counter "udcounter" to either count up or count down. If no adjustment is necessary, the frequency comparator makes no adjustment to the counter.

FIGS. **8.0203**AA–BC provide a circuit drawing showing construction details of the up/down counter "udcounter" included in the low power frequency locked loop "lpfll." The counter has some logic on the counter's output so that if the counter counts all the way down to zero, the counter does not wrap around and go to all ones. Instead, the counter stops at zero (until a signal requesting an up count is received). Similarly, if the counter counts all the way up to all ones, the counter does not wrap around to all zeros. Instead, the counter stops at all ones (until a signal requesting a down count is received).

FIGS. **8.020301**AA–BB provide a circuit drawing showing construction details of an adder "udcounter_adder" included in the up/down counter.

FIGS. **8.020302**AA–AB provide a circuit drawing showing construction details of a D type flip-flop "udcounter_dff" included in the up/down counter.

Details of Low Power Current Controlled Oscillator

The integrated circuit **16** includes the low power current controlled oscillator "lpcco." The oscillator consumes very little current (e.g., less than 100 nA). The oscillator "lpcco" includes digital input lines, and oscillates at a frequency controlled by the digital input lines. The circuit includes a thermal generator, a digitally controlled current mirror, an oscillator, and an output driver.

FIGS. **8.0204**AA–EJ provide a circuit drawing of the low power current controlled oscillator "lpcco." The low power current controlled oscillator "lpcco" includes a thermal voltage generator, including a string of resistors, shown in FIGS. **8.0204**AA–EJ in the upper left corner. The thermal voltage generator generates a small voltage proportional to kT/q across the string of resistors where k is Boltzmann's constant, 1.38×10^{-23} Joules per degree Kelvin, T is temperature in degrees Kelvin, and q is the electron charge in Coulombs. The voltage kT/q is approximately equal to 26 mV at room temperature. That small voltage divided by the resistor value sets the current in the circuit. This current is approximately equal to (kT/qR) ln ((W/L)Q1)/(W/L)Q2). In the illustrated embodiment, the current is set to a low value (e.g., approximately three nano-amps).

Thermal generators are known in the art. See for example, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation" by Eric Vittoz and Jean Fellrath, IEEE Journal of Solid-State Circuits, Vol. SC-12, No. 3, June 1977. See particularly FIG. **8** of this article, and the associated description.

The low power current controlled oscillator "lpcco" also includes a wake up circuit shown to the far left of the thermal voltage generator that causes a much higher current to flow initially to turn on the feedback loop. The wake up circuit then shuts off and leaves the low value (nano-amp) current flowing. Thus, initialization occurs on power up and the wake up circuit is off after that unless power is removed and reapplied. The outputs of the up/down counter "udcounter," select 1 "Sel1," select 2 "Sel2," select 4 "Sel4," and select 8 "Sel8" come into the low power current controlled oscillator as shown on the left edge of FIGS. **8.0204**AA–EJ. The low power current controlled oscillator further includes control circuitry shown on the bottom strip of FIGS. **8.0204**AA–EJ. These outputs of the up/down counter control the number of currents that are mirrored into this control circuitry by a current mirror. The current mirror is digitally controlled and weightings are binary in the illustrated embodiment; however, any weighting scheme can be used. The current mirror includes transistors operating in the subthreshold, or weak inversion mode, due to the extremely low current level.

More particularly, referring to FIGS. **8.0204**AA–EJ, there are five transistors to the right of the string of resistors, mirrored down to one about the center of the page providing a divide by five. Current is then mirrored through all the p-channel devices. The block shown in the upper right of FIGS. **8.0204**AA–EJ is a selectable current mirror. The first stage generates one current equal to the reference current and that is always flowing into the n-channel diode down at the bottom of that stack. Shown to the right of the n-channel diode are the selectable groups of p-channels. The first one has one, the next two, the next four, the next eight in a binary sequence. The transistors shown below the p-channels transistors are select devices and they are controlled by the digital signals select 1 "Sel1," select 2 "Sel2," select 4 "Sel4," and select 8 "Sel8." Thus, the number of currents can be selected and however many are selected are added into the one that is always flowing in the diode.

The current from groups of p-channel transistors that are not selected is diverted over to a separate or second diode shown on the far right of FIGS. **8.0204**AA–EJ. This is so that when a block of transistors is not selected, their drain nodes do not get pulled up to V_{DD}. By sinking the current in this second diode, the voltage at the drain node of an unselected block of transistors is kept down near the voltage at which it will operate when and if it is actually connected over to the first diode. This is so that, upon switching a select line, a capacitance doesn't have to be charged from V_{DD} down to the proper operating voltage. In any case, the selected number of currents are added together into the first diode, and then that voltage is carried on the line shown in FIGS.**8.0204**AA–EJ as going down the right side of page, which line has a capacitor tied to it. That capacitor is a filter capacitor so that the voltage on that node does not change abruptly when the select lines change or when some unrelated signal nearby switches. Since all of these transistors are operating in a sub-threshold or weak inversion mode, a small change in the voltage on their gate will otherwise result in

a rather large impact on the operation of the circuit. That line is the input for the circuitry shown across the bottom of FIGS. **8.0204**AA–EJ. There is a current mirror situation there, so that the sum of all the selected currents plus the one default current flowing in the diode above is mirrored and flows through the p-channel devices of this circuitry. There is then another mirror to generate bias voltages for the n-channel current source devices for the VCO ring oscillator. The p-channel gate voltages are used in mirroring into the p-channel load devices of the same ring oscillator. The frequency of this ring oscillator is controlled by the current mirrored to them.

The low power current controlled oscillator includes a four stage ring oscillator. The frequency of oscillation is approximately proportional to the amount of current flowing. The frequency of oscillation of the four stage ring oscillator is directly proportional to its bias current over a wide range of frequencies. For example, frequency is directly proportional to bias current for frequencies between approximately 100 Hz and tens of MHZ (e.g. to twenty MHZ).

The low power current controlled oscillator further includes an output driver. In the illustrated embodiment, the output driver includes a comparator circuit receiving the output of the fourth stage ring. The purpose for this comparator is to convert the small output signal of the oscillator to full digital levels. In the illustrated embodiment, full digital levels are zero volts and V_{DD}. In the illustrated embodiment, V_{DD} is 3.3 Volts±0.3 Volts. In an alternative embodiment, V_{DD} is 5 Volts±10 or 20%. Another other suitable values can be employed for V_{DD} and the digital levels.

Circuitry is included to eliminate the crossover current in the n and p channel devices in the first few invertors. This is because, when operated at very low current levels, the rise and fall times are long and could allow substantial current to flow in the n and p channel devices during switching.

The digital levels are buffered and amplified up by the comparator to provide an output signal from the low power frequency locked loop "lpfll." The output of the low power current controlled oscillator is shown on the right edge of FIGS. **8.0204**AA–EJ. In the illustrated embodiment, the low power current controlled oscillator operates at eight kHz. However, if desired for alternative embodiments, the low power current controlled oscillator is capable of running at a frequency from approximately 100 Hz to 20 kHz. In an alternative embodiment, the low power current controlled oscillator is capable of running at a frequency from approximately 100 Hz to 30 kHz.

The low power current controlled oscillator consumes very little power. For example, in the illustrated embodiment, the low power current controlled oscillator consumes less than a milliAmp. More particularly, in the illustrated embodiment, the low power current controlled oscillator consumes approximately 100 nanoAmps.

In an alternative embodiment, instead of using a thermal voltage generator, a transistor is biased in the subthreshold region in order to define the current source and to generate a small current. However, in this embodiment, the voltage on the gate of the transistor is updated periodically as it leaks away.

Although the low power current controlled oscillator has been described in connection with a radio frequency identification device, the low power current controlled oscillator can be advantageously employed in any battery powered electronic product which must keep track in time.

FIGS. **8.03**AA–AB provide a circuit drawing showing construction details of a counter bit "lpfll_cbit" included in the receiver "rx."

FIGS. **8.04**AA–EE provide a circuit drawing of the wake up controller "rxwu." An input to the wake up controller is a clock signal "LPCLK" from the low power frequency locked loop "lpfll." This clock signal input is shown in the upper left of FIGS. **8.04**AA–EE. The clock signal "LPCLK" is further divided down to provide certain time intervals available for selection. These are the time intervals at which the integrated circuit **16** will wake up and look for a radio frequency signal. In the illustrated embodiment, these time intervals are set at 0.5, 16, 64 and 256 milliseconds. The selection of one of these multiple available time intervals is accomplished via radio frequency command from the interrogator.

The wake up controller includes wake up abort logic shown in the lower left of FIGS. **8.04**AA–EE. The wake up abort logic performs a number of tests (described elsewhere herein) to determine whether the received signal is a valid signal and, if all tests are passed, then the wake up controller asserts a signal on line "RXWU" shown on the right of FIGS. **8.04**AA–EE. This signal wakes up the processor, and the processor then processes the command contained in the message.

Details of Wake Up Tests

FIGS. **8.0401**AA–AB provide a circuit drawing of a wake up abort logic circuit "wuabort." The wake up abort logic circuit provides for conservation of battery power. If what is received is not a valid message, the wake up abort logic circuit determines this quickly and the device returns to the sleep mode so that the battery is not drained on invalid messages or spurious communication. The wake up abort logic circuit works by counting clock cycles. The wake up abort logic circuit has as an input a clock signal "CHIPCLK" that is the output of the clock recovery oscillator "dcr" (described below). This clock signal is divided down by a factor of four, which results in a value approximately equal to the spread spectrum chip rate. After the clock is actually acquired from a message from the interrogator, the resulting value will be equal to the chip rate.

Initially though, when these wake up tests are performed, a clock has not yet been acquired from a message. The wake up abort logic includes an RF Detect Timer, shown on the top, left of FIGS. **8.0401**AA–EE, which performs a first test. The RF Detect Timer counts a predetermined number of cycles of the clock (e.g., 13 cycles) and, if the RF detect signal from the receiver is not asserted, the wake up is aborted. On the other hand, if the RF detect signal is asserted within those cycles, the wake up abort logic starts the next series of tests without waiting for the end of the predetermined number of cycles.

The next series of tests are timed by a counter shown across the center of the page in FIGS. **8.0401**AA–EE. For the next tests, transitions in the incoming data stream are counted within a certain time interval and the number of transitions must fall within a certain range in order to pass the test. Transitions are counted by the counter shown at the bottom in FIGS. **8.0401**AA–EE. The range limits are set by knowing the number of transitions that should occur in the data within the amount of time allowed. This is known because each data bit is encoded as a thirty-one chip sequence as described elsewhere herein. The reason there is a range is because the clock has not yet been acquired accurately so there is a range of clock frequencies that must be considered. In the illustrated embodiment, one test checks whether, after five counts of the clock, there has been between greater than or equal to one, and less than eight transitions in the data. If not, the wake up is aborted and the device goes back to sleep. If yes, then the next test is performed.

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The next test checks whether, after twenty-six clock counts, there are greater than or equal to fourteen and less than thirty-two transitions in the data. If not, wake up is aborted and the chip goes back to the sleep mode. If this test is passed, the wake up abort logic circuit performs tests relating to signals generated by the clock recovery nodes. One such test is a test for chip lock. Chip lock is an indication that clock recovery is proceeding and has actually gotten within a few percent of the desired clock frequency. The final check is whether frequency lock has occurred. Again, these tests are timed. If one of the signals is not asserted by the time the timer signal goes high, then the wake up will be aborted and the device goes back to sleep and will try again after another wake up interval. Frequency lock will come into the logic in the center of the page in FIGS. **8.04**AA–CB, and that is what causes the RXWU signal to be asserted, thus waking up the processor.

Another function of the wake up abort logic shown in FIGS. **8.0401**AA–EE is to discriminate between high rate and low rate. The wake up abort logic measures time while these tests are performed to determine when the interrogator is in high rate, but the chip is in low rate or vice versa and abort out of wake up (return to the sleep mode).

These tests will now be described in connection with flowcharts illustrated in FIGS. **25–27**.

The wake up controller "rxwu" was described above in connection with FIGS. **8.04**AA–EE. The wake up tests performed by the wake up controller are illustrated in flow chart form in FIGS. **25–26**.

When the integrated circuit **16** first wakes up, bias generators and the receiver "rx" are powered on (step Si in FIG. **25**). After ensuring that the bias is on (step S**2** in FIG. **25**), the master clock "dcr" is started. By design, the master clock "dcr" starts at a frequency below the final frequency it will achieve after the clock recovery circuit "lpfll" extracts the clock frequency from the incoming signal. More particularly, in the illustrated embodiment, the master clock starts at a start frequency above half of the final frequency it will achieve after the clock recovery circuit "lpfll" extracts the clock frequency from the incoming signal. Still more particularly, in the illustrated embodiment, the master clock starts at a start frequency between half and three quarters of the final frequency the master clock will achieve after the clock recovery circuit "lpfll" extracts the clock frequency from the incoming signal. In the illustrated embodiment, the final frequency is 38.15 MHZ, and the start frequency is between 20 and 30 MHZ. The master clock includes a frequency locked loop including a voltage controlled oscillator. An offset is applied to the oscillator to make sure that the clock starts at least as fast as 20 MHZ. Then, the frequency locked loop adjusts the frequency to 38.15 MHZ.

Because the clock has not yet been acquired from the incoming signal, the clock is a free running oscillator when providing the start frequency. Initial wake up tests are performed at this lower start frequency. The receiver "rx," digital clock and data recovery circuit "dcr," pseudo random number processor "pnproc," and voltage controlled oscillator "vco" are turned on (step S**3** in FIG. **25**).

The input radio frequency signal received from the interrogator **26** is a direct sequence spread spectrum input signal in the illustrated embodiment. Spread spectrum techniques are described above. In one embodiment, incoming radio frequency commands are included in packets that contain, in order of transmission, a preamble, a Barker code, and the command. In one embodiment, each bit of the incoming radio frequency command sent by the interrogator is modulated using a pseudo noise (PN) sequence for direct sequence spread spectrum communication.

After the clock is running, the device **12** is in a receiver on mode illustrated in FIG. **27** by a vertical line marked "WAKEUP RX ON." After the clock is running, the device **12** performs wake up tests so (at the lower or start frequency).

A first test is whether the receiver "rx" detects any radio frequency signal within a predetermined number of clock cycles (step S**4** in FIG. **25**). In the illustrated embodiment, this predetermined number of clock cycles is 13. If no radio frequency signal is detected by the receiver "rx" within 13 clock cycles, the device **12** returns to the sleep mode. If a radio frequency signal is detected by the receiver "rx" within 13 clock cycles, the device **12** switches to a wake up abort test mode illustrated in FIG. **27** by a vertical line marked "WAKEUP ABORT TESTS," and a second test is performed.

In the second test, a determination is made as to whether a predetermined number of data transition pulses occur within a predetermined number of clock pulses for the radio frequency signal detected by the receiver "rx" (step S**5** in FIG. **25**). More particularly, the device **12** includes a long counter shown in FIGS. **8.0401**AA–EE driven by a clock signal "CHIPCLK." The device **12** further includes a circuit "datatx" which detects transitions in the signal received by the receiver "rx" and generates a pulse ("DTX" in FIG. **26**) at each transition. The device **12** further includes another counter circuit shown in FIGS. **8.0401**AA–EE which counts these pulses. Because a valid incoming signal is modulated with a known PN sequence, the number of transitions in a given time for a valid incoming signal is known. The device **12** includes logic "wuabort" that tests whether the proper number of data transition pulses occur within a certain number of clock pulses. More particularly, in the illustrated embodiment, the logic tests whether more than or equal to one and less than eight such data transition pulses occur within five chips. If not, the device returns to the sleep mode. If so, a third test is performed.

In the third test, a determination is made as to whether a predetermined number of data transition pulses occur within a predetermined number of clock pulses for the radio frequency signal detected by the receiver "rx" (step S**5** in FIG. **26**). The third test is similar to the second test, except that the number of data transition pulses is tested against a number of clock pulses that is different from the number in the second test. More particularly, in the illustrated embodiment, the logic tests whether more than or equal to fourteen and less than thirty-two such data transition pulses occur within thirty-one chips. If not, the device **12** returns to the sleep mode.

If the above transition tests are passed, the device **12** checks to see if the clock recovery circuit locks onto the incoming clock rate. More particularly, in the illustrated embodiment, a determination is made as to whether a clock is acquired from the incoming signal within 6 k chips (step S**7** in FIG. **26**). A determination is then made as to whether frequency lock is achieved within 16 k chips (step S**9** in FIG. **26**). The device **12** returns to the sleep mode if any of these tests fail. If these tests are passed, then the device **12** enters a processor on mode illustrated in FIG. **27** by a vertical line marked "PROCESSOR ON." Power is supplied to the processor (step S**10** in FIG. **26**) and the device **12** waits for the preamble of the incoming message to end and the command to begin.

In one embodiment, the tests of FIG. **26** are employed to distinguish between incoming signals with different possible valid chipping rates.

More particularly, in the illustrated embodiment, it is known how long each of the various tests should take for

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valid low chipping rate or high chipping rate signals, and this information can be tested to determine whether the incoming signal is a high rate or low rate signal.

Other appropriate tests can be performed in embodiments where spread spectrum is not employed. In these embodiments, knowing how valid data is encoded, the wake up timer and logic still compares the number of transitions received in a given amount of time with an expected number of transitions for a valid signal.

FIGS. **8.040101**AA–AB provide a circuit drawing showing construction details of a counter bit "wuabort-cbit" included in the wake up abort logic.

FIGS. **8.0402**AA–AB provide a circuit drawing showing construction details of a timed lockout divider cell "tldcel" included in the receiver wake up controller.

Details of Lock Detection in a Digital Clock Recovery Loop

In many communications systems, it is necessary to recover a clock signal from the received data. A phase locked loop is one way of recovering such a clock signal. In the illustrated embodiment, such a recovered clock is used as a master clock.

The integrated circuit **16** includes the digital clock and data recovery circuit "dcr" which includes a phase locked loop. The phase locked loop includes a voltage controlled oscillator "dcr_vco." The frequency of the voltage controlled oscillator always starts low, at between 50% and 75% of the final desired value. When the voltage controlled oscillator starts running, large steps are taken (FIG. **54**). As the frequency approaches the final value, increasingly smaller steps are taken to achieve greater accuracy. The illustrated embodiment employs four step sizes: large, medium, medium-fine, and fine. For example, in the illustrated embodiment, large steps up are employed between 50% to 75% of the final desired value, and medium steps up are then taken above 75% until pump up commands are not issued for a predetermined number of transitions, then medium-fine steps up are employed until the final value is overshot, then fine steps down are employed.

A method is needed to determine when the frequency of the voltage controlled oscillator matches the desired frequencies contained in the received data.

The voltage controlled oscillator includes a control node having a voltage indicative of the frequency of the voltage controlled oscillator. The behavior of this node is used to determine when frequency lock has occurred.

After the phase locked loop has run long enough to get within a few percent of the final value (at a time illustrated as To in FIG. **54**), a signal "SDD" (start data decoding) is generated. This signal "SDD" disables the large and medium steps and enables lock detect circuitry for determining if frequency lock has occurred. A latch "KILLSU" (kill start up) detects when the first fine step pump down occurs (at T_1 in FIG. **54**). This enables a latch "FREQLOCK." The latch "FREQLOCK" is set when the first fine step pump up occurs (at a time illustrated as T_2 in FIG. **54**). A signal "FREQLOCK" is then indicative that the phase locked loop has reached its final value.

In other words, large, medium, then medium-fine steps up are followed by fine steps down. The final value is overshot, and a frequency lock signal is provided upon occurrence of the first subsequent fine step up.

In the illustrated embodiment, the final value of the voltage on the control node of the voltage controlled oscillator, where frequency lock is expected, is approximately 1.2 Volts. In one embodiment, each large step is approximately several hundred milliVolts, each medium step has a size approximately in the tens of milliVolts (e.g., 25 millivolts), each medium-fine step has a size of approximately a few milliVolts (e.g. two milliVolts), and each fine step has a size approximately in the tenths of milliVolts. Various other relative sizes or numbers of steps are employed in alternative embodiments.

The sizes of steps is set using current sources of different values that are turned on for a fixed period of time to drive to the capacitor on the control node of the voltage controlled oscillator.

In the illustrated embodiment, the fine step generator is not disabled before time T_0 so there is a possibility that a combination of fine steps with larger steps can take place before time T_0. In an alternative embodiment, however, the fine step generator is disabled before time T_0.

FIGS. **8.05**AA–CB provide a circuit drawing of the digital clock and data recovery circuit "dcr." The digital clock and data recovery circuit includes a phase locked loop of a digital design, and a state machine "dcr_statemachine" that drives the phase locked loop. The phase locked loop includes a voltage controlled oscillator "dcr_vco" and control circuitry "dcr_vcocontrol" for the voltage controlled oscillator. The voltage controlled oscillator "dcr_vco" includes a control node ("OUTN" and "OUTP" shown in FIGS. **8.0504**AA–EE and described below in greater detail) and produces an oscillation at a rate dependent on the value of a voltage applied to the control node. In the illustrated embodiment, the state machine has four states. The phase locked loop produces an output pulse on a line "OUTC" (later labeled "FMASTER"). The digital clock and data recovery circuit attempts to place four pulses of the output clock within one chip time.

The state machine "dcr_statemachine" determines when that is not the case and, if not, whether to cause the oscillator to run faster or to run slower. The state machine "dcr_statemachine" then issues appropriate pump up or pump down signals to drive a control node of the oscillator. The voltage controlled oscillator "dcr_vco" starts out at a minimum frequency as determined by an offset current which is present regardless of the loop. This ensures that the oscillator will start up and run at greater than 50% of the final value so that the phase locked loop will converge on the proper frequency. The digital clock and data recovery circuit also includes a PLL start-up circuit "dcr_startup." The acquisition of the clock frequency happens in stages and, initially, the control node moves in large increments towards its final value. The start-up circuit "dcr_startup" provides large increments for controlling the loop. However, as the digital clock and data recovery circuit gets closer to acquisition of clock frequency, control switches from that start up circuit "dcr_startup" over to the state machine "dcr_statemachine." The state machine provides very fine steps as the final convergence is done with very fine steps. The data stream is fed into the circuitry on the upper right. Then the data is sampled during one of the states of the state machine after it has been determined that the data is valid. The data stream is recreated and called "RXCHIPS."

FIGS. **8.0501**AA–BE provide a circuit drawing of the start up circuit "dcr_startup" included in the digital clock and data recovery circuit. In the illustrated embodiment, the start up circuit provides either very large or fairly large steps dependent upon how far from frequency the oscillator is running. The start up circuit also has a counter (shown along the bottom in FIGS. **8.0501**AA–BE) that determines when there have been no pump up commands issued for a given count of transitions. In the illustrated embodiment, the counter determines when there have been no pump up commands during sixteen transitions. If the given count of

transitions are detected in the data and there has been no pump up command (e.g., no pump up medium or pump up fast command) then a signal is asserted on a line "SDD." SDD stands for Start Data Decode and is an indication that the control voltage has converged to within a few percent.

FIGS. **8.050101**AA–BE provide a circuit drawing showing construction details of a shift register cell "dcr_sreg" included in the PLL start up circuit. FIGS. **8.050102**AA–AB provide a circuit drawing showing construction details of a counter bit "dcr_counterbit" included in the PLL start up circuit.

FIGS. **8.0502**AA–CD provide a circuit drawing of the state machine "dcr_statemachine." In the illustrated embodiment, the state machine has four states. The state machine includes two flip-flops with feedback signals providing the four states. This circuit generates pump up slow, and pump down slow commands for adjusting voltage on a control node of the voltage controlled oscillator.

This circuit also has the circuitry that turns off the start up circuit and generates the frequency lock signal. When trying to acquire frequency lock, there will be large and medium pump ups, without any pump downs, until the final desired value is overshot. At this point, there will be a first pump down slow pulse. When the first pump down slow command is issued, the start up circuitry "dcr_startup" is turned off, which leaves only fine step capability for adjustment in the control voltage. It takes time for the fine steps to bring down the control node voltage to the proper value and the voltage on the control node will overshoot the desired voltage in the negative direction. The state machine will detect that it has gone too far and it will step the voltage back up towards the final value and that first fine step up will be detected and at that point the frequency lock signal is asserted.

FIGS. **8.0503**AA–BB provide a circuit drawing of a bias generator "dcr_bias." The bias generator includes current mirrors that generate the appropriate bias values for the various circuits in the digital clock and data recovery block.

The digital clock and data recovery circuit "dcr" includes a VCO control voltage generator "dcr_vcocontrol" which is shown in greater detail in FIGS. **8.0504**AA–EE.

The digital clock and data recovery circuit "dcr" employs a phase locked loop to recover the clock frequency from an incoming radio frequency message. Phase locked loops use feedback to maintain an output signal in a predetermined phase relationship with a reference signal.

Details of Digital Clock Recovery Loop

Operation and design of the digital clock and data recovery circuit "dcr" will now be further described with reference to FIGS. **61–72**

In many communications systems it is necessary to recover a clock signal from the received digital data stream. In the device **12**, this clock signal is used as the master timing reference to eliminate the need for an external crystal-based timing reference. Typically, a phase locked loop of some type is used to extract the clock.

There are many requirements on the phase locked loop used to recover a clock signal from the received digital data stream. Several important ones for this application are that the phase locked loop must acquire the desired frequency without locking to a multiple or sub-multiple of the desired frequency; the phase locked loop must lock to the desired frequency within a certain time of interest; and the phase locked loop must yield consistent performance despite wide variation in device parameters which is inherent in integrated circuit processing. The phase locked loop employed in the illustrated embodiment, embodied in the digital clock recovery circuitry "dcr," satisfies all of these requirements.

In the illustrated embodiment, the forward link baseband data is encoded for direct sequence spread spectrum. In the illustrated embodiment, a data bit "1" is represented by a thirty-one chip sequence and a data bit "0" is represented by the logical inversion of the same thirty-one chip sequence.

The mode of operation of the device **12** is as follows. The chip periodically awakens from a low-current sleep mode in order to detect whether an incoming RF message is present. The clock recovery loop "dcr" is inactive in the low-current sleep mode. If a message is present, the message is tested to make sure it is a valid message from an interrogator. If the incoming signal passes these tests, the clock recovery loop is enabled, the clock is acquired, the message is processed, and a reply is sent. The device **12** then returns to sleep mode.

The digital clock recovery loop is illustrated by reference numeral **700** in FIG. **61**. The digital clock recovery loop **700** comprises several sub-circuits. The digital clock recovery loop **700** includes a voltage controlled oscillator **702**. The voltage controlled oscillator **702** has an output **704**, and produces a square wave at output **704** having a frequency controlled by the voltage on an input control node. When the voltage on the control node is zero, the frequency at output **704** is at least one half of the final recovered frequency and not greater than the final recovered frequency. The output frequency rises monotonically, nearly linearly, as the control node voltage is increased. This is shown in FIG. **62**. More particularly, FIG. **62** illustrates the frequency produced at the output **704** of the voltage controlled oscillator **702** relative to a voltage at the input control node.

The digital clock recovery loop **700** further includes a charge pump and loop filters which control the rate of change of the voltage on the control node of the voltage controlled oscillator. The charge pump and loop filters are designated in FIG. **61** with reference numeral **706**.

The digital clock recovery loop **700** further includes a start-up circuit **708** which performs frequency detection when the voltage controlled oscillator first starts up and, in conjunction with the charge pump and loop filters **706**, causes the voltage on the control node of the voltage controlled oscillator to change rapidly.

The digital clock recovery loop **700** further includes a state machine **710** which performs phase detection when the frequency of the voltage controlled oscillator is within a few percent of its final value and, in conjunction with the charge pump and loop filters, causes the voltage on the control node of the voltage controlled oscillator **702** to change slowly.

The only analog blocks are the voltage controlled oscillator **702** and the charge pump. The rest of the circuits of the digital clock recovery loop are digital circuits which are easy to build at high yield in integrated circuit processes.

In the preferred embodiment, the voltage controlled oscillator **702** is the voltage controlled oscillator "dcr_vco" shown in the detailed schematic drawings, and has control nodes "OUTN" and "OUTP"; the state machine **710** is the state machine "dcr_statemachine" shown in the detailed schematic drawings; and the start-up circuit **708** is the start-up circuit "dcr_startup" shown in the detailed schematic drawings.

The digital clock recovery loop causes the frequency at the output of the voltage controlled oscillator to vary until a predetermined number of this clock fit within the time interval of an identifiable discrete segment of the incoming data. More particularly, in the illustrated embodiment, the digital clock recovery loop causes the frequency at the output of the voltage controlled oscillator to increase until exactly four cycles of the clock fit within the time interval of a single chip. In alternative embodiments, other integer

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numbers could be used. In the illustrated embodiment, a state machine having four states is employed to cause the frequency at the output of the voltage controlled oscillator to increase until exactly four cycles of the clock fit within the time interval of a single chip. A general description of the behavior of the control node voltage can be found above in the section titled Details of Lock Detection in a Digital Clock Recovery Loop.

What follows is a discussion of the operation of each block of the digital clock recovery loop. The start-up circuit **708** is show in FIG. **61**. Although it may be simplified from the circuitry shown in the detailed schematics including "dcr_startup" shown in FIGS. **8.0501**AA–BE, the theory of operation is the same.

The start-up circuit **708** includes a plurality of flip-flops **712** chained together, a plurality of flip-flops **714** chained together, and an exclusive-or gate **716**. The exclusive-or gate **716** has an output connected to the input of the first of the flip-flops **714**, has an input connected to the output of the last of the flip-flops **712**, and has another input connected to the input of the same flip-flop **712**. More particularly, in the illustrated embodiment, each flip-flop **712** and **714** is a D-type flip-flop and has a D input, a clock input, and a Q output. The D input of flip-flops **712** other than the first flip-flop is connected to the Q output of a previous flip-flop **712**. The first flip-flop **712** is connected to the input data "Data In." The D input of flip-flops **714** other than the first flip-flop **714** is connected to the Q output of a previous flip-flop **714**. The first flip-flop **714** is connected to the output of the exclusive-or gate **716**. The clock inputs of the flip-flops **712** and **714** are all tied to the output **704** of the voltage controlled oscillator **702**. Data is shifted from the D input of each flip-flop to the Q output of the same flip-flop on each clock pulse. Thus, the flip-flops **712** as a group define a shift register, and the flip-flops **714** as a group define a shift register.

The start-up circuit **708** further includes an AND gate **718** that has one input that is the output of the exclusive-or gate **716**, has a second input that is the output of the second of the flip-flops **714**, and defines an output "Puf**1**" (a first pump up fast output). The start-up circuit **708** further includes an AND gate **720** that has one input that is the output of the exclusive-or gate **716**, has a second input that is the output of the third of the flip-flops **714**, and defines an output "Puf**2**" (a second pump up fast output).

The start-up circuit **708** further includes a counter **722** that receives as inputs "Puf**1**" and "Puf**2**" and generates an output "SDD" (start data decode) when the output of the voltage controlled oscillator **702** is close to its final value.

The exclusive-or gate **716** in the center of the page generates a high output whenever there is a transition in the data as sampled by If the clock signal output by the voltage controlled oscillator **702** output clock. Assume for discussion that data is latched into all flip-flops **712** and **714** on the falling edge of the clock. Puf**2** goes high when three falling edges of the clock occur within one chip because the inputs of the AND gate are spaced apart by three flip-flops. Three falling edges of the clock occur within one chip when the frequency is between 75% and 100% of the final value. Puf**1** goes high when two falling edges of the clock occur within one chip because the inputs of the AND gate are spaced apart by two flip-flops. Two falling edges of the clock occur within one chip when the clock frequency is 50% to 75% of its final value. This is shown on the waveform diagram of FIG. **63** for the case when the frequency is exactly 50%. Puf**1** could be used to pump up the control node of the voltage controlled oscillator **702** rapidly. Puf**2** could be used to pump up the control node of the voltage controlled oscillator **702** at a rate equal to that for Puf**1** (as is shown in FIG. **61**) or it could pump at a slower rate (as is done in the circuitry shown in the detailed schematics). As the clock frequency approaches 75% of final in the Puf**1** case or 100% of final in the Puf**2** case, pump up signals occur infrequently as error must accumulate over a long time to cause the appropriate number of clock edges to shift within a chip. This is used to detect when the clock frequency is close to its final value.

The counter **722** counts transition pulses until it is cleared by a Puf**1** or Puf**2** signal. If a predetermined large number of transitions are counted before a pump up occurs, a signal is asserted on a line SDD (start data decode). In the illustrated embodiment, if sixteen transitions are counted before a pump up occurs, a signal is asserted on line SDD. This indicates that the voltage on the control node of the voltage controlled oscillator is within a few percent of its final value, allowing data to be accurately recovered.

In the illustrated embodiment, the state machine **710** issues finer pump-up signals than the start-up circuit **708**, and can also issue pump-down signals. In the illustrated embodiment, the start-up circuit **708** only issues pump up signals. The state machine **710** has as many states as the number of clock cycles which fit within one chip time. In the illustrated embodiment, the state machine has four states. The state machine **710** counts clock pulses and expects the data to transition at a count of one every time there is a transition. If the transition actually occurs at a count of four then the clock is too slow and a pump up is issued. If the transition actually occurs at a count of two then the clock is too fast and a pump down is issued. If the transition actually occurs at a count of three, it is not known whether the clock is fast or slow so no adjustment is made to the voltage controlled oscillator. A state diagram is shown in FIG. **64**.

Design of a clocked sequential circuit is known in the art. See, for example, chapter 6 of Digital Logic and Computer Design by M. Morris Mano, 1979, Prentice-Hall, Inc. A typical design procedure involves describing circuit behavior using a state diagram (see FIG. **64**), obtaining a state table (see FIG. **66**), assigning binary values to each state (see FIG. **64**), determining the number of flip-flops needed (see FIG. **65**), choosing the type of flip-flops to be used (see FIG. **65**), using Karnaugh maps or other simplification methods, deriving circuit output functions and flip-flop input functions (see FIGS. **67** and **68**), and drawing the logic diagram. The numbers in parentheses in FIG. **64** are the binary state numbers. ENDT enables the sampling of the data (always at state two when no transition occurred). There are several ways to implement a circuit to perform functions of a state diagram. Assume that Q1 and Q0 are the binary state numbers in parentheses above (Q1 on the left, Q0 on the right), and that D1 and D0 are the next state values of Q1 and Q0, respectively. This is illustrated in FIG. **65**. The flip-flop outputs Q0 and Q1 are the states. Then, a state table can be derived. This is shown in FIG. **66**. Using Karnaugh maps (see FIGS. **67** and **68**), minimum logic to perform the desired function can be derived. It should be noted, of course, that minimum logic need not be employed—logic involving an increased number of logic gates but performing the same desired function can also be employed. From the Karnaugh map shown in FIG. **67**, the following equation can be derived:

$$D0=Q1+TX\cdot Q0+En\cdot TX$$

which can also be written as:

$$D0=[Q1'\cdot(TX\cdot Q0)'\cdot(En\cdot TX)']'$$

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where the symbol "+" represents a logical OR, the symbol "·" represents a logical AND, and the symbol "'" represents a logical NOT.

From the Karnaugh map shown in FIG. **68**, the following equation can be derived:

$$D1=TX'\cdot Q1\cdot Q0'+En\cdot TX'\cdot Q0'$$

which can also be written as:

$$D1=[(TX'\cdot Q1\cdot Q0')'\cdot(En\cdot TX'\cdot Q0')']'$$

where the symbol "+" represents a logical OR, the symbol "·" represents a logical AND, and the symbol "'" represents a logical NOT.

Logic to implement these equations is shown in FIGS. **69** and **70**.

Paths shown in FIG. **64** are defined as follows:

ENDT=Q1'·Q0·TX'

PumpUpSlow=Q1·Q0'·TX; and

PumpDownSlow=Q1'·Q0·TX

Logic used to implement the state machine, in accordance with one embodiment of the invention, is shown in FIGS. **8.0502**AA–CD.

A simplified timing diagram showing operation of the state machine is shown in FIG. **71**. The crowding and separation of states in FIG. **71** is exaggerated to show the various modes of operation in a compact form. More particularly, it is highly unlikely that a pump down signal would be necessary so soon after a pump up signal as is depicted in FIG. **71**.

The state machine is trying to fit four cycles of the output of the voltage controlled oscillator in one chip width. Referring simultaneously to FIGS. **71** and **64**, starting at the first occurrence of state **3** in FIG. **71**, there is no transition, so the state machine will proceed to state **4** on the next clock. At state **4**, there is no transition, so the state machine will proceed to state **1** at the next clock. At state **1**, there is a transition in the waveform. The state machine always proceeds to state **2** from state **1**. At state **2**, there is no transition. From state **2**, the state machine proceeds to state **3**. This cycle is repeated and these paths are followed unless the clock recovery loop drifts off frequency.

If the clock recovery loop drifts off frequency, other paths of the state diagram of FIG. **64** are followed. For example, if a transition is seen at state **4**, the voltage controlled oscillator is oscillating too slowly, and a PumpUpSlow is issued. The state machine skips state **1** and goes to state **2**.

If, after going from state **1** to state **2**, a transition is seen, the voltage controlled oscillator is oscillating too fast. The state machine will go from state **2** to state **2** so that state **2** is now in the proper position.

If a transition is seen at state **3**, the voltage controlled oscillator may either be oscillating too fast or too slowly, so no pump up or pump down signals are issued. Instead, the state machine proceeds to state **2**.

The control functions performed by the start-up circuit and state machines can be used to control the frequency of any voltage controlled oscillator. The particular voltage controlled oscillator **702** that is employed in the illustrated embodiment is shown in FIGS. **8.0505**AA–EF.

In the illustrated embodiment, the voltage controlled oscillator **702** includes a current controlled four-stage ring oscillator shown in the center of FIGS. **8.0505**AA–EF. The frequency of oscillation is very much linearly proportional to the bias current flowing in each stage.

The voltage controlled oscillator **702** further includes an Operational Transconductance Amplifier shown on the left side of FIGS. **8.0505**AA–EF. This Operational Transconductance Amplifier converts a voltage difference at its inputs to a current difference at its outputs. This Operational Transconductance Amplifier has a characteristic that is linear over a range of input voltage.

The composite circuit is a voltage controlled oscillator **702** with nearly linear operation about the operating point of 38.15 MHz. The circuit shown to the right in FIGS. **8.0505**AA–EF converts the small signal output of the oscillator to full digital levels.

The input reference voltage is generated by a bandgap regulator and has a value of about 1.2 volts. The circuit is designed so that at nominal conditions the control node needs to pump to about equal to the reference voltage to oscillate at 38.15 MHz.

The start-up circuit requires that the oscillator start at greater than half frequency (approximately 19 MHz) and less than full frequency over all operating conditions and for all process variations. This oscillator start frequency is set by providing an offset current to the bias of the oscillator which is not controlled by the input voltage. In the illustrated embodiment, the range of allowed offset currents is 7.437 μA to 9.763 μA. A value of 8.2 μA was chosen. Thus, the oscillator start frequency will vary from about 20 MHz to 34 MHz.

The charge pump and loop filters **706** are shown in greater detail in FIGS. **8.0504**AA–EE. The filter capacitors are shown on the right side of FIGS. **8.0504**AA–EE. In the illustrated embodiment, the filter capacitors include a first group of ten capacitors, defining a total capacitance of 10 pF, and an second group of ten capacitors, defining a total capacitance of 10 pF. In FIGS. **8.0504**AA–EE, the first group of ten capacitors is shown above the second group of ten capacitors. Other values or numbers are possible. In the illustrated embodiment, the lower group of capacitors is connected to the reference voltage input to the voltage controlled oscillator **702**. The upper group of capacitors is connected to the control node input of the voltage controlled oscillator **702**. The control node always starts at 0 Volts and is pumped up. The other (reference) side is always at the bandgap voltage.

The charge pump is shown in the center of FIGS. **8.0504**AA–EE. In the illustrated embodiment, there are actually four charge pumps. If The method employed is to steer a current to charge or discharge the 10 pF capacitor for a prescribed period of time (one cycle of the recovered clock, in the illustrated embodiment). The change in control voltage for a single pump is:

$$\Delta V=(I/C)\Delta t$$

The lower three of the illustrated charge pumps are controlled by the start-up circuit **708** and can only pump up. The upper pump is controlled by the state machine **710** and can pump up or down in fine steps. The step sizes are controlled by the current value which is set accurately using a bandgap regulator to generate a reference current and using current mirrors to set the pump current. The step sizes used in the illustrated embodiment are shown in FIG. **72**. Of course, other step sizes can be employed, as desired, and various numbers of different sized steps can be employed.

The time used for the calculations for the coarse and medium cases is 40 ns, a typical value for the starting period of the oscillator. 26.2 ns is used for the medium fine and fine cases because these steps occur when the oscillator is close to its final frequency.

The course and medium steps are controlled by the Puf**1** and Puf**2** outputs of the start-up circuit. More particularly, in

the illustrated embodiment, the course steps are controlled by the PumpUpFast output of the start-up circuit "dcr_startup" shown in the detailed schematic drawings, and the medium step is controlled by the PumpUpMed output of the start-up circuit "dcr_startup" shown in the detailed schematic drawings. The medium fine step is also controlled by the PumpUpMed signal but the step size is reduced when the SDD (start data decode) signal is asserted indicating the oscillator is within a few percent of its final value. The fine step is controlled by the state machine and is used to "close in" on the final value.

While this charge pump and loop filter configuration is advantageous for implementation on an integrated circuit, other configuration are possible. For example, simple RC filters can be employed.

Details of Transmit Frequency Derivation from Incoming Data

The illustrated embodiment has a loop filter including capacitors on respective control nodes "OUTN" and "OUTP" (shown in FIGS. **8**.**0504**AA–EE) of the voltage controlled oscillator "vco." In the illustrated embodiment, the loop filter capacitor on the control node "OUTP" is defined by a plurality of capacitors in parallel, and the loop filter capacitor on the control node "OUTN" is defined by a plurality of capacitors in parallel. The voltage on the respective control nodes is indicative of the frequency at which the voltage controlled oscillator "vco" is oscillating. After an entire incoming message has been received by the receiver "rx," the control nodes and the capacitors on the control nodes are isolated from driving circuitry. The control voltage is thus stored in analog form on the capacitors, and the voltage controlled oscillator "vco" continues to oscillate at the recovered frequency. The length of time that the voltage stored on the capacitors is valid depends on leakage currents that can charge or discharge the capacitors over time.

In the illustrated embodiment, such leakage currents are minimized by minimizing n+ and p+ active areas on the control node, and by minimizing drain to source voltages on devices connected to the control nodes. The values for the respective capacitors are chosen, in conjunction with loop filter requirements, to hold the control voltages for as long as possible as required before the device **12** transmits a reply to the received radio frequency command. This amount of time is approximately several hundred milliseconds in the illustrated embodiment.

The output frequency of the voltage controlled oscillator can be multiplied up to generate a carrier frequency for the transmitter, as described elsewhere, or can be divided down to generate tones for FSK (frequency shift keyed) transmission or DPSK (differential phase shift keyed) transmission depending on what form of transmission is selected for the transmitter "tx."

In one embodiment, only one control node is employed; however, in the illustrated embodiment, a differential control node scheme is employed involving two control nodes "OUTN" and "OUTP." Therefore, in the illustrated embodiment, a capacitor is provided on each control node, and control voltages are stored in analog form on these two capacitors.

FIGS. **8**.**0504**AA–EE provide a circuit drawing of the control voltage generator "dcr_vcocontrol." The control voltage generator shows the control nodes for the voltage controlled oscillator. The control voltage generator is a differential circuit. The control nodes are shown on the right edge of FIGS. **8**.**0504**AA–EE as "OUTP" and "OUTN," where "OUTN" is actually tied to the band gap voltage, which is approximately 1.2 Volts. "OUTP" is the node that is pumped up to adjust frequency. The control voltage generator includes step size generators shown on the left half of FIGS. **8**.**0504**AA–EE. The steps are achieved by conducting a current to the capacitor on the control node for a prescribed length of time. For a large step, a large current is applied to this capacitor. For a small step, a smaller current is applied to this capacitor. The capacitor on the control node "OUTP" is defined by ten capacitors in parallel in the illustrated embodiment.

A similar capacitor, defined by ten capacitors in parallel, is provided on the other control node "OUTN."

Four different size currents are generated by fine, medium fine, medium, and coarse step generators "dcr_finestepgen," "dcr_medfinestepgen," "dcr_medstepgen," and "dcr_coarsestepgen" respectively. The currents are either steered to the control capacitor on the control node or away from the capacitor, depending on whether there is a pump up or pump down command.

FIGS. **8**.**050401**AA–CK provide a circuit drawing showing construction details of the coarse step generator "dcr_coarsestepgen." The coarse step generator includes a plurality of current mirrors.

FIGS. **8**.**050402**AA–CJ provide a circuit drawing showing construction details of the medium step generator "dcr_medstepgen." The medium step generator includes a plurality of current mirrors.

FIGS. **8**.**050403**AA–BI provide a circuit drawing showing construction details of the medium fine step generator "dcr_medfinestepgen." The medium fine step generator includes a plurality of current mirrors.

FIGS. **8**.**050404**AA–BB provide a circuit drawing showing construction details of a fine step controller "dcr_finestepctrl."

FIGS. **8**.**050405**AA–EJ provide a circuit drawing showing construction details of the fine step generator "dcr_finestepgen."

FIGS. **8**.**0505**AA–EF provide a circuit drawing of the voltage controlled oscillator "dcr_vco." The voltage controlled oscillator "dcr_vco" is a four stage ring oscillator with differential stages. The voltage controlled oscillator includes an OTA (operational transconductance amplifier) shown on the left side of FIGS. **8**.**0505**AA–DE. The OTA gives a linear relationship between the voltage differential at its inputs and the current at its output. The voltage controlled oscillator further includes current mirrors which mirror the current at the output of the OTA to drive the voltage controlled oscillator to change its frequency. The previously discussed control nodes ("OUTN" and "OUTP" of FIGS. **8**.**0504**AA–EE) are shown coming in on the left side FIGS. **8**.**0505**AA–DE, labelled as "INN" and "INP." The voltage controlled oscillator further includes, at its output, a comparator type circuit that provides digital levels for the output of the voltage controlled oscillator "dcr_vco."

FIGS. **8**.**0506**AA–AB provide a circuit drawing of a clock generator "dcr_rxclkgen." Different frequencies are needed for different functions. The clock generator provides outputs at different frequencies. For example, the clock generator provides an output "PROCCLK" (for the processor), an output "CHIPCLK" (chip clock); and outputs "PLLCLKP" and "PLLCLKN" for the clock that drives the state machine. The clock generator "dcr_rxclkgen" has an input "LOWRATE" for low rate which is a signal indicative that the chip is in low rate and can expect data to come in at a chip rate of one-half the normal chip rate. The loop is adjusted in a manner such that the frequency of "FMASTER" does not change regardless of whether the chip is in high rate or low rate. However, the clock "CHIPCLK" for the integrated

circuit **16** is half as fast in low rate, and it takes twice as long to get data in as it would to get the same amount of data in at the high rate.

FIG. **8.050601** provides a circuit drawing showing construction details of a flip-flop "dcr_rxclkgenff" included in the clock generator.

FIGS. **8.0507**AA–AB provide a circuit drawing of a non-overlapping clock generator "dcr_clkgen." The non-overlapping clock generator receives as inputs true and compliment clock signals "ClkInP" and "ClkInN" and provides buffered true and compliment clock signals "ClkOut" and "ClkOutN." The non-overlapping clock generator buffers the true and compliment clock signals "ClkInP" and "ClkInN" in such a way that before "ClkOut" can go high, "ClkOutN" must be low, and then at the end of that cycle, before "ClkOutN" can go high, "ClkOut" must be low. Any overlap between the two clocks occurs when they are both low. They are never both high at the same time. This is quite commonly required in many circuits throughout the integrated circuit **16** where shift register type techniques are used, and one stage passes information to another. Non-overlapping clocks are required for such functions.

The circuit of FIGS. **6**AA–EK further includes a transmitter "tx." The transmitter "tx" is capable of transmitting using different modulation schemes, and the modulation scheme is selectable by the interrogator. More particularly, if it is desired to change the modulation scheme, the interrogator sends an appropriate command via radio frequency. The transmitter can switch between multiple available modulation schemes such as Frequency Shift Keying (FSK), Binary Phase Shift Keying (BPSK), Direct Sequence Spread Spectrum, On-Off Keying (OOK), Amplitude Modulation (AM), and Modulated Backscatter (MBS).

The output responses are included in packets that contain, in order of transmission, a preamble, a Barker code, and the reply data.

In one embodiment, each bit of the radio frequency reply sent by the device **12** is modulated using a pseudo noise (PN) sequence for direct sequence spread spectrum communication. The sequence is generated in part by a linear feedback shift register "pngshr" having a plurality of registers "pngsreg." In one embodiment, the linear feedback shift register is in the form [**5**,**2**] which means that the input to the first register is the result of combining the output of the fifth register by the exclusive-OR with the output of the second register. This produces thirty-one states. In one embodiment, the linear feedback shift register is in the form [**6**,**1**] for a sixty-three chip sequence. In another embodiment, the linear feedback shift register is in the form [**8**,**4**,**3**,**2**] for a two hundred and fifty-five chip sequence. In a preferred embodiment, the shift register is selectable between multiple of the above forms. In the form [**6**,**1**], the input to the first of six registers is the result of combining the output of the sixth register by exclusive-OR with the output of the first register. In the form [**8**,**4**,**3**,**2**], the input to the first of eight registers is the result of combining the outputs of registers eight, four, three, and two by exclusive-OR. The sixty-three chip output sequence requires less time for signal synchronization than the two hundred and fifty-five chip sequence. However, the two hundred and fifty-five chip output sequence provides better performance in systems having poor signal to noise ratio.

FIGS. **8.06**AA–ED provide a circuit drawing of the transmitter "tx." FIGS. **8.06**AA–ED show a transmitter PLL "txpllfsyn," a test mode data selector "txdatasel," a BPSK modulation driver "txbpsk," a frequency doubler "txdoubler," a second frequency doubler "txdoubler**2**," a transmitter power amp "txpoweramp," a transmitter bias generator "txbias," and a modulated backscatter transmitter "txmbs." FIGS. **8.06**AA–ED actually shows two different transmitters. Much of FIGS. **8.06**AA–ED illustrates circuitry employed for an active transmitter which is used in accordance with an alternative embodiment of the invention, but not in accordance with the preferred embodiment. FIGS. **8.06**AA–ED also illustrate the modulated backscatter transmitter "txmbs" that is employed in a preferred embodiment. The active transmitter will be discussed first.

In embodiment where the active transmitter is employed, the active transmitter operates by taking the "FMASTER" clock that was recovered from the incoming data stream and using a phase locked loop "txpllfsyn" (an analog phase locked loop in the illustrated embodiment) to multiply up the frequency. In the illustrated embodiment, the frequency is multiplied up by a factor of sixteen from 38 MHZ to 610 MHZ. The phase locked loop includes an oscillator that generates eight phases which are 45° out of phase with respect to each other. The eight phases generated by the oscillator are applied to first doubler circuits "txdoubler" and "txdoubler**2**" in order to generate the proper phased outputs at double the frequency that then again serve as inputs to the other doubler circuit. The active transmitter further includes a transmitter power amp "txpoweramp." The transmitter power amp includes the other doubler that receives the outputs of the first doubler circuits "txdoubler" and "txdoubler**2**." Capability for several different modulation techniques is provided for the active transmitter. One such modulation technique is BPSK where the phase of the carrier (2.44 GHz in the illustrated embodiment) is inverted to indicate a bit change. Another such modulation technique is amplitude modulation (AM). In the illustrated embodiment, 100% modulation, or on/off keying, is employed with the amplitude modulation.

FIGS. **8.0601**AA–BB provide a circuit drawing of the transmitter phase locked loop "txpllfsyn." The phase locked loop "txpllfsyn" includes a voltage controlled oscillator "txvco" that receives an analog tune voltage and provides an output frequency in accordance with the analog tune voltage. The phase locked loop further includes a divider "txdivider" which receives the output signal of the voltage controlled oscillator "txvco" and divides the frequency of the output of the oscillator "txvco" by a factor of sixteen. It will be understood that this division ratio of sixteen is for an exemplary embodiment, and the scope of the present invention encompasses other division ratios. The phase locked loop "txpllfsyn" includes a phase/frequency detector "txpfdet." At the phase/frequency detector "txpfdet," the output of the divider "txdivider" is compared to the signal received at the reference input of the detector, which reference input, in accordance with one embodiment, is the signal "FMASTER" recovered from the incoming data stream. The phase/frequency detector "txpfdet" compares the fed back signal (i.e., having a frequency of the voltage controlled oscillator "txvco" divided by sixteen) with the signal received at the reference input and puts out a pump up signal "PU" or pump down signal "PD" in accordance with phase and frequency difference therebetween. The phase locked loop "txpllfsyn" further includes a charge pump "txchgpump." The pump up signal "PU" or pump down signal "PD" put out by the phase/frequency detector "txpfdet" drive the charge pump "txchgpump." The phase locked loop "txpllfsyn" further includes a loop filter "txloopfilter" that receives an output signal from the charge pump "txchgpump" and filters this output signal for providing the tune voltage for controlling the voltage controlled oscillator "txvco." The filter "txloop-

filter" removes transients and establishes loop dynamics, i.e. responsiveness, of the resulting phase locked loop.

Again, the voltage controlled oscillator provides an output signal having a frequency proportional to the tune voltage received at its input. When the phase locked loop is locked, the frequency and phase of the signal fed back to the phase/frequency detector is equal to the frequency and phase of the reference input signal. Therefore, the output frequency of the voltage controlled oscillator "txvco" is equal to times the frequency of the reference signal, where N is equal to the division factor of the divider. For the exemplary embodiment described above, N is equal to sixteen and the output frequency of the voltage controlled oscillator "txvco" is equal to sixteen times the frequency of the reference signal, e.g. 16×38.15 MHZ=610.45 MHZ. By providing various output taps distributed along a ring topology of the voltage controlled oscillator "txvco," output signals of different phase relationships (but of equal frequency) are obtained from the voltage controlled oscillator "txvco." In a preferred embodiment, eight separate output taps from the voltage controlled oscillator "txvco" provide eight different output signals having substantially 45° differences in phase therebetween, e.g., 0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°. Thus, in the illustrated embodiment, the voltage controlled oscillator "txvco" generates eight phases spaced 45°.

FIGS. **8.060101**AA–BB provide a circuit drawing showing construction details of the phase/frequency detector "txpfdet." The phase/frequency detector puts out a pump up signal "PU" or pump down signal "PD", and drives the charge pump.

FIGS. **8.060102**AA–BB provide a circuit drawing showing construction details of the charge pump "txchgpump." The charge pump drives the loop filter.

FIGS. **8.060103**AA–CB provide a circuit drawing showing construction details of the loop filter "txloopfilter."

FIGS. **8.060104**AA–DC provide a circuit drawing showing construction details of the transmitter voltage controlled oscillator "txvco." The voltage controlled oscillator "txvco" generates eight phases spaced 45°.

Details of CMOS High Frequency VCO Stage

The voltage controlled oscillator "txvco" comprises a ring oscillator having four stages. FIG. **32** is a simplified schematic illustrating one stage **104**. Four such stages are connected in a chain, with the outputs of the chain connected to the inputs of the chain, to define the ring oscillator. The stage **104** includes a p-channel transistor **105** having a gate defining a control node "V control," having a source connected to a supply voltage "V+," and having a drain; and a p-channel transistor **106** having a gate connected to the control node "V control," having a source connected to the supply voltage "V+," and having a drain. The stage **104** further includes an n-channel transistor **107** having a gate defining an input "IN P," a drain connected to the drain of the transistor **105** and defining a node "B," and a source; and an n-channel transistor **108** having a gate defining an input "IN N," a drain connected to the drain of the transistor **106** and defining a node "A," and a source. The stage **104** further includes an ideal current source **109** connected to the sources of the transistors **107** and **108** and directing current from the sources of the transistors **107** and **108** to ground. The stage **104** further includes a resistor **110** connected between the voltage "V+" and the drain of the transistor **107**, and a resistor **111** connected between the voltage "V+" and drain of the transistor **108**. The stage **104** further includes a source follower **112** including an n-channel transistor **113** having a gate connected to the node "A," having a drain connected to a supply voltage "V+," and having a source defining an output "OUT P"; and an ideal current source **114** connected to the source of the transistor **113** and directing current from the source of the transistor **113** to ground. The stage **104** further includes a source follower **115** including an n-channel transistor **116** having a gate connected to the node "B," having a drain connected to the supply voltage "V+," and having a source defining an output "OUT N"; and an ideal current source **117** connected to the source of the transistor **116**. A source follower is a circuit where the signal at the source terminal of a transistor is approximately equal to the signal at the gate of the transistor. The source followers **112** and **115** are provided in the stage **104** to provide the necessary drive for the outputs "OUT P" and "OUT N" to drive a load. More particularly, the outputs "OUT P" and "OUT N" drive amplifiers that drive frequency doublers described elsewhere herein. Nodes "A" and B" are connected to another stage in the chain (e.g., by connecting the nodes "A" and "B" to inputs "IN P" and "IN N" of a subsequent stage).

The ideal current source **109** drives a current "IBIAS," and the values of the resistors **110** and **111** and of "IBIAS" are chosen such that transistors **107** and **108** are in saturation. More particularly, the values of the resistor **110** and the current "IBIAS" are chosen such that the value of the resistance of resistor **110** multiplied by the current "IBIAS" is less than a maximum voltage (e.g. 800 mV) to cause saturation of transistor **107**. In the illustrated embodiment, resistors **110** and **111** have the same resistance value. The resistors **110** and **111** are made from n-well, n+, p+, or polysilicon depending on the process used to manufacture the integrated circuit **16**. Parasitic capacitance on nodes A and B is minimized by compact arrangement of the components of the stage **104**. Computer software, such as from Cadence, can also be employed to reduce parasitic capacitance.

The stage **104** provides a differential amplifier capable of switching at a very high frequency. The switching frequency is adjustable by adjusting the voltage at control node "V control." More particularly, as the voltage at the control node "V control" decreases, the p-channel transistors **105** and **106** become more conductive, and there is less impedance between the supply voltage "V+," and the drains of the transistors **107** and **108**. This provides for a faster switching rate. There is a linear change in frequency versus the voltage at the control node "V control" for at least some range of voltages.

FIGS. **8.06010401**AA–DC provide a circuit drawing showing construction details of a stage "txvcostage" included in the transmitter voltage controlled oscillator. FIG. **8.0601040101** is a layout plot showing how the components of the stage **104** of FIG. **32** are laid out. More particularly, FIG. **8.0601040101** actually shows four stages. FIG. **8.0601040101** shows locations **400** defining resistors; a line **402** providing VREG (V+ of FIG. **32**); locations **404** defining source followers of FIG. **32**; a location **406** defining input "IN P" of FIG. **32**; a location **408** defining input "IN N" of FIG. **32**; locations **410** defining the n-channel differential pair and the current source of FIG. **32**; locations **412** defining the p-channel devices of FIG. **32**; a line **414** providing the control voltage "V control" of FIG. **32**; and 915 MHZ option capacitors **416**.

FIGS. **8.060105**AA–DD provide a circuit drawing showing construction details of the divider "txdivider."

FIGS. **8.06010501**AA–AB provide a circuit drawing showing construction details of a flip-flop "txdivtff" included in the divider.

FIGS. **8.0602**AA–AB provide a circuit drawing showing construction details of a test mode data selector "txdatasel."

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FIGS. **8.0603**AA–AB provide a circuit drawing showing construction details of a BPSK modulation driver "txbpsk."

Details of Frequency Doubler

Analog multipliers are known in the art. An analog multiplier includes two inputs, and includes an output providing a signal that is representative of a multiplication of one of the inputs with the other of the inputs. One known analog multiplier is known as a Gilbert multiplier cell. For a detailed discussion of Gilbert cells, see *Four Quadrant Multiplier,* B. Gilbert, IEEE Journal of Solid State Circuits, 1968, pp. 365–373. Such Gilbert multiplier cells are also described in detail in *Analysis and Design of Analog Integrated Circuits*, Paul R. Gray and Robert G. Meyer, Third Edition, 1993, John Wiley & Sons, Inc., pp. 667–681. Such Gilbert multiplier cells include two cross-coupled, emitter-coupled pairs of bipolar junction transistors in series with an emitter coupled pair of bipolar junction transistors. A Gilbert multiplier cell employing bipolar junction transistors produces an output that is the hyperbolic tangent of two input voltages. This is because a characteristic of bipolar junction transistors is exponential non-linearity. If the input voltages are sufficiently low, the hyperbolic tangent function can be approximated as linear, and the circuit behaves as a multiplier which multiplies together the two input voltages.

The multiplier cell originally developed by Gilbert employed bipolar junction transistors. It is also known to employ MOS transistors to produce a Gilbert multiplier cell. See, for example, *Analog Integrated Circuits for Communication, Principles, Simulation and Design,* Donald O. Pederson and Kartikeya Mayaram, Kuwer Academic Publishers, Third Printing, 1994, pp. 431–433.

FIG. **34** illustrates a frequency doubler circuit **119** that includes a Gilbert cell **120**. The Gilbert cell **120** includes a pair **122** defined by transistors **124** and **126**. The Gilbert cell **120** further includes a pair **128** defined by transistors **130** and **132**. The transistors **124** and **126** have sources that are connected together. Thus, the pair **122** is a source coupled pair. The transistors **130** and **132** have sources that are connected together. Thus, the pair **128** is a source coupled pair.

The transistors **126** and **130** have gates that are connected together to define a first input node. The transistors **124** and **132** have gates that are connected together to define a second input node. The transistors **124** and **130** have drains that are connected together, and the transistors **126** and **132** have drains that are connected together (shown as a criss-cross pattern in FIG. **34**).

The Gilbert cell **120** further includes another pair **134** including transistors **136** and **138** having sources coupled together. Thus, the pair **134** is a source coupled pair. The pair **134** is in series with the pairs **122** and **128**. More particularly, the transistor **136** has a drain connected to the sources of the transistors **124** and **126**, and the transistor **138** has a drain connected to the sources of the transistors **130** and **132**. The transistor **138** has a gate defining a third input node, and the transistor **136** has a gate defining a fourth input node.

The Gilbert cell **120** further includes an ideal current source **140** driving current from the sources of the transistors **136** and **138** to ground. The frequency doubler **119** further includes a resistor **142** connected between the drain of the transistor **124** and a voltage, and a resistor **144** connected between the drain of the transistor **132** and the voltage. The resistors **142** and **144** define loads for current steering that produces output voltage swings.

For low amplitude signals, the Gilbert cell **120** provides an output between the drain of the transistor **124** and the drain of the transistor **132** that is an analog multiplication of a first input signal applied between the first and second input nodes, by a second input signal applied between the third and fourth input nodes.

It is known to use a Gilbert cell to multiply together sine waves of different phases to produce a doubled frequency (FIGS. **34** and **35**). This is based on a known trigonometric relationship:

$$\sin 2\theta = 2 \sin \theta \cos \theta$$

Signals that are 180° apart are applied to the first and second input nodes, and a phase shifter produces 90° shifted signals that are applied to the third and fourth input nodes. However, in such embodiments, an integrator is required, and the phase shifter is required to be feedback controlled, because slight errors in the required 90° phase shift would otherwise cause the output signals to have different average values and different amplitudes as shown in FIG. **33**. FIG. **33** is a waveform diagram illustrating the effect of errors in frequency doubler circuits that necessitates correction, such as by using an integrator and feedback. FIG. **34** is a circuit schematic illustrating a frequency doubler circuit that employs an integrator and feedback to solve the problem illustrated in FIG. **33**. FIG. **35** is a waveform diagram illustrating input and output waves created and employed by a frequency doubler circuit such as the one shown in FIG. **34**.

It is desirable to avoid the need for feedback. Frequency multiplier circuits employing feedback are susceptible to being disturbed. For example, if substrate noise or an adjacent line switches and causes a shift at the integrator, the output will be distorted from the desired output until the integrator has a chance to recover. The integrator can take a long time to recover. Therefore, it is desirable to eliminate feedback loops from a frequency multiplier.

FIG. **36** is a circuit schematic illustrating a symmetric frequency doubler circuit **146** that does not require an integrator and feedback to solve the problem illustrated in FIG. **33**. The frequency doubler circuit of FIG. **36** creates and employs waveforms such as those shown in FIG. **35**.

The frequency doubler circuit **146** includes a first Gilbert cell **148**, and a second Gilbert cell **150** coupled to the first Gilbert cell **148**.

The first Gilbert cell **148** includes a pair **152** defined by transistors **154** and **156**. The transistors **154** and **156** have sources that are connected together. Thus, the pair **152** is a source coupled pair. The Gilbert cell **148** further includes a pair **158** defined by transistors **160** and **162**. The transistors **160** and **162** have sources that are connected together. Thus, the pair **158** is a source coupled pair.

The transistors **156** and **160** have gates that are connected together to define a first input node **163**. The transistors **154** and **162** have gates that are connected together to define a second input node **165**. The transistors **154** and **160** have drains that are connected together, and the transistors **156** and **162** have drains that are connected together (shown as a criss-cross pattern in FIG. **36**).

The Gilbert cell **148** further includes another pair **164** including transistors **166** and **168** having sources coupled together. Thus, the pair **164** is a source coupled pair. The pair **164** is in series with the pairs **152** and **158**. More particularly, the transistor **166** has a drain connected to the sources of the transistors **154** and **156**, and the transistor **168** has a drain connected to the sources of the transistors **160** and **162**. The transistor **168** has a gate defining a third input node **169**, and the transistor **166** has a gate defining a fourth input node **171**.

The Gilbert cell **148** further includes an ideal current source **170** driving current from the sources of the transistors **166** and **168** to ground. The frequency doubler **146** further includes a resistor **172** connected between the drain of the transistor **154** and a voltage, and a resistor **174** connected between the drain of the transistor **162** and the voltage. The resistors **172** and **174** define loads for current steering that produces output voltage swings.

The second Gilbert cell **150** includes a pair **182** defined by transistors **184** and **186**. The transistors **184** and **186** have sources that are connected together. Thus, the pair **182** is a source coupled pair. The Gilbert cell **150** further includes a pair **188** defined by transistors **190** and **192**. The transistors **190** and **192** have sources that are connected together. Thus, the pair **188** is a source coupled pair.

The transistors **186** and **190** have gates that are connected together to define a first input node **193** of the second Gilbert cell **150**. The transistors **184** and **192** have gates that are connected together to define a second input node **195** of the second Gilbert cell **150**. The transistors **184** and **190** have drains that are connected together, and the transistors **186** and **192** have drains that are connected together (shown as a criss-cross pattern in FIG. **36**).

The Gilbert cell **150** further includes another pair **194** including transistors **196** and **198** having sources coupled together. Thus, the pair **194** is a source coupled pair. The pair **194** is in series with the pairs **182** and **188**. More particularly, the transistor **196** has a drain connected to the sources of the transistors **184** and **186**, and the transistor **198** has a drain connected to the sources of the transistors **190** and **192**. The transistor **198** has a gate defining a third input node **199**, and the transistor **196** has a gate defining a fourth input node **201**.

The Gilbert cell **150** further includes an ideal current source **200** driving current from the sources of the transistors **196** and **198** to ground.

The outputs of the second Gilbert cell are connected to the outputs of the first Gilbert cell. More particularly, the drain of the transistor **184** is connected to the drain of the transistor **154** and the drain of the transistor **192** is connected to the drain of the transistor **162**.

The first input node **193** of the second Gilbert cell **150** is connected to the fourth input node **171** of the first Gilbert cell **148**. The third input node **199** of the second Gilbert cell **150** is connected to the second input node **165** of the first Gilbert cell **148**. The fourth input node **201** of the second Gilbert cell **150** is connected to the first input node **163** of the first Gilbert cell **148**.

In operation, a first sinusoidal signal is applied to the second input node **165** of the first Gilbert cell **148**. A second sinusoidal signal, 180° out of phase with the first sinusoidal signal, is applied to the first input node **163** of the first Gilbert cell **148** (and to the fourth input node of the second Gilbert cell **150**). A third sinusoidal signal, 90° out of phase with the first sinusoidal signal, is applied to the second input node **195** of the second Gilbert cell **150**. A fourth sinusoidal signal, 270° out of phase with the first sinusoidal signal, is applied to the first input node of the second Gilbert cell **150**. This relationship of phases on the inputs to the first and second Gilbert cells causes the output to be symmetrical so that the problem of FIG. **33** is avoided without the need for feedback. Even with slight errors in phases between the input signals, a symmetrical output is produced.

Generally speaking, each Gilbert cell adds current from bottom transistors to top transistors through the resistor loads to form output voltages. In the illustrated embodiment, a phase arrangement applied to the upper Gilbert cell is generally reversed for the bottom Gilbert cell so undesirable offsets cancel each other.

In one embodiment, the second, third, and fourth input sinusoidal signals are derived from the first input sinusoidal signal using a simple four stage differential oscillator.

A doubled frequency is thus obtained at the outputs, which are defined at the drain of the transistor **154** and the drain of the transistor **162**, without the need for an integrator and feedback.

FIGS. **8.0604**AA–AB provide a circuit drawing of the frequency doubler "txdoubler." The frequency doubler circuit "txdoubler" includes a doubler core "txfdbl" having two tiers of transistors. The two tiers of transistors are shown in FIGS. **8.060401**AA–FE as being a top tier and a bottom tier. The frequency doubler requires different levels depending on whether the top tier of transistors or bottom tier of transistors are driven by a particular phase. The frequency doubler "txdoubler" therefore includes driver amplifiers "txfdbldrv" which provide that level shifting. There is no intended phase shift introduced by the driver amplifiers.

FIGS. **8.060401**AA–FE provide a circuit drawing of the frequency doubler core "txfdbl." The frequency doubler core "txfdbl" includes level shifting circuitry. The level shift is a little level shift, and is accomplished by a resistor and capacitor shown at the top of the right stack (FIG. **8.060401**AD). The level shift is performed in order to adjust output levels down in voltage because this frequency doubler core drives another frequency doubler.

FIGS. **8.0605**AA–AB provide a circuit drawing of the frequency doubler "txdoubler**2**." The frequency doubler "txdoubler**2**" is substantially similar to the first frequency doubler "txdoubler." The main difference has to do with the bias arrangements for the driver amps and for the doubler core. In an alternative embodiment, the first and second frequency doublers "txdoubler" and "txdoubler**2**" are identical.

FIGS. **8.060501**AA–CD provide a circuit drawing showing construction details of the doubler driver amplifier "txfdbldrv."

FIGS. **8.060502**AA–CD provide a circuit drawing showing construction details of a second doubler driver amplifier "txfdbldrv**2**" included in the frequency doubler "txdoubler**2**." The second doubler driver amplifier "txfdbldrv**2**" include a bias diode. The doubler driver amplifier "txfdbldrv**2**" includes circuitry (the criss-cross configuration in FIGS. **8.060502**AA–CD) where bi-phase (binary phase shift keying) modulation is performed. This is where a phase can be switched from one side to another by the state of two inputs "BPMODINP" and s"PMODINN." Thus, a phase reversal can be accomplished in this circuit.

FIGS. **8.060503**AA–FE provide a circuit drawing of a frequency doubler core "txfdbl**2**." The frequency doubler core "txfdbl**2**" is substantially identical to the frequency doubler core "txfdbl" except for the biasing transistors.

Details of Single Antenna Receiver and Active Transmitter

FIG. **50** provides a simplified circuit schematic showing the antenna **44** being shared by the active transmitter and the Schottky diode detector **84**. The Schottky diode detector **84** was described above in detail in connection with FIG. **29**, like reference numerals indicating like components.

The detector **84** includes a Schottky diode **86** having an anode connected to the antenna **44** and having a cathode. The detector **84** further includes an ideal current source **88** connected to the cathode of the Schottky diode **86** and driving current through the antenna and Schottky diode **86** in the direction from the anode to the cathode. The detector **84** further includes a capacitor **90** connected between the

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cathode of the Schottky diode **86** and ground and providing a radio frequency short to ground. The detector **84** further includes a capacitor **92** having a first terminal connected to the cathode, having a second terminal defining an output of the detector **84**, providing an AC short to video frequency, and defining the output of the detector **84**.

The active transmitter is described elsewhere herein, and is illustrated as a block **330** in FIG. **50**.

The antenna is a loop antenna and has one end connected to a bias voltage (Vdd) and has another end connected to the anode of the Schottky diode **86**.

The transmitter has an antenna output (or RF output) **332**, and the detector **84** has an antenna input (or RF input) **334**. In the illustrated embodiment, the integrated circuit **16** having the transmitter **330** and detector **84** includes a contact connected to the antenna output **332** and accessible from outside the IC package; and a contact connected to the antenna input **334** and accessible from outside the IC package. These contacts are connected together by a short outside the package. This provides for flexibility in that different antenna configurations are possible, separate antennas can be used for the detector **84** and transmitter **330**, if desired, an external amplifier can be used to amplify the output of the transmitter **330**, etc.

The detector and transmitter do not operate simultaneously.

In one embodiment, the integrated circuit **16** further includes a pull up transistor **336** connected to the cathode of the Schottky diode **86** and configured to connect the cathode to the bias voltage (Vdd) when the transmitter is operating. The pull up transistor **336** can be included if necessary so the detector does not interfere with the transmitter **330** while the transmitter **330** is transmitting.

By using a common antenna for the active transmitter and the Schottky diode detector, space savings are achieved.

The active transmitter **330** is shown in greater detail in FIG. **51**. The active transmitter includes a differential pair **338** of transistors driven by the frequency doubler. The function of the differential pair **338** is to steer current to the antenna **44** or away from the antenna **44**. If bi-phase modulation is employed, the differential pair **338** steers one phase or the other phase to the antenna **44**. More particularly, if bi-phase modulation is employed, then a signal on line "ENABLEAM" (see FIGS. **8.06**AA–ED, and **8.0605**AA–AB to **8.0608**AA–BB) is low and the leftmost of three current steering transistors (sources connected to the current source) is off because its gate is low. Current is then steered to the antenna by the transistor shown on the right. Its phase is determined in an earlier stage. The other phase is present in the middle transistor. When data is reversed the current phases switch sides in response to the earlier stage. If amplitude modulation is employed, the differential pair either sends current to the antenna **44**, or is sends none to provide on/off keying. More particularly, in the amplitude modulation mode, a signal on line "ENABLEAM" is high and current is steered to the antenna by the transistor shown to the right if a signal on line "AMDATA" is high, and the current is steered to Vdd (not to the antenna) if the signal on line "AMDATA" is low.

FIGS. **8.0606**AA–IE provide a circuit drawing of a transmitter power amplifier "txpoweramp." The transmitter power amplifier includes a frequency doubler, shown in the left half of FIGS. **8.0606**AA–IE. In the illustrated embodiment, the frequency doubler receives inputs at 1.22 GHz, and provides outputs at 2.44 GHz. The transmitter power amplifier includes the differential pair of transistors, shown on the right side of FIGS. **8.0606**AA–IE, driven by the frequency doubler. The differential pair steers current to the antenna or away from the antenna, as described above. If bi-phase modulation is employed, the differential pair steers one phase or the other phase to the antenna. If amplitude modulation is employed, the differential pair either sends current to the antenna, or it sends none to provide on/off keying.

FIGS. **8.0607**AA–JJ provide a circuit drawing of a transmitter bias generator "txbias." The transmitter bias generator includes various current mirrors in order to provide the proper bias currents to the various blocks of the transmitter "tx."

Details of Single Antenna Receiver and Backscatter Transmitter

FIG. **52** provides a simplified circuit schematic showing an antenna **350** being shared by the backscatter transmitter and the Schottky diode detector **84**, in a manner similar to the antenna sharing possibility described in connection with FIGS. **50–51**. The Schottky diode detector **84** was described above in detail in connection with FIG. **29**, like reference numerals indicating like components.

In the illustrated embodiment, the antenna **350** is a loop antenna and has one end connected to a bias voltage (Vdd) and has another end connected to the detector **84** via a detector input illustrated as RXANT in FIG. **52**. For antenna sharing with a backscatter transmitter, capacitors **352** and **354** external of the integrated circuit **16** are employed, as illustrated in FIG. **52**, to isolate the antenna from the backscatter antenna driver when the detector is using the antenna.

The detector and transmitter do not operate simultaneously.

By using a common antenna for the backscatter transmitter and the Schottky diode detector, space savings are achieved.

In an alternative embodiment shown in FIG. **53**, a single antenna **350** is shared by the detector **94** (shown in FIG. **30** and described elsewhere herein) and a backscatter transmitter. An n-channel transistor **356** is provided having power electrodes connected to opposite ends of the antenna, and having a control electrode connecting to transmitter modulation circuitry. The control electrode is held low when the antenna is being used by the receiver.

FIGS. **8.0608**AA–BB provide a circuit drawing of a modulated backscatter transmitter "txmbs." The modulated backscatter transmitter "txmbs" includes circuitry that creates non-overlapping drive signals. The modulated backscatter transmitter "txmbs" includes primary antenna ports "BS1" and "BS2." Each of these antenna ports is intended to be connected to one-half of a dipole antenna having a length appropriate for the transmission frequency. In the illustrated embodiment, the halves of the dipole antenna have respective sizes appropriate for 2.44 Ghz. The halves of the dipole antenna are not included on the integrated circuit **16**, in the illustrated embodiment, but are instead provided "off chip." Other antenna arrangements are possible.

The modulated backscatter transmitter "txmbs" further includes an n-channel transistor marked 900 micron in FIGS. **8.0608**AA–BB, and two n-channel pull-up transistors marked 100 micron and respectively connected between a voltage vdd! and the 900 micron transistor. When the gate of the transistor marked 900 micron is high, then the two dipole halves are shorted together with a fairly low impedance (e.g., on the order of 15 Ohms, plus any bond wire impedance that might be present depending on how the device is packaged). The antenna becomes substantially similar to a

single half-wavelength antenna. In a backscatter mode, when the two halves of the antenna are shorted together, the antenna reflects a portion of the power being transmitted by the interrogator. In the other state, the gate of the 900 micron transistor is low. The 900 micron transistor is then off, but the two 100 micron transistors that pull up the voltage vdd! are on, lifting antenna ports "BS1" and "BS2" both up to a voltage of vdd! minus an n-channel Vt. The two antenna ports "BS1" and "BS2" are then isolated from each other by an open circuit. This isolation changes the radar cross-section of the dipole antenna dramatically from when the two halves are shorted together. The antenna becomes substantially similar to two quarter wavelength antennas. In a Backscatter mode, when the two halves of the antenna are isolated, the antenna reflects very little of the power transmitted by the interrogator.

The modulated backscatter transmitter "txmbs" further includes cross-coupled circuitry shown near the middle in FIGS. **8**.**0608**AA–BB. The cross-coupled circuitry is provided to make sure that both the pull up transistors and the shorting device are not on at the same time.

The modulated backscatter transmitter "txmbs" further includes another antenna port "BS3" that is intended to be used when the integrated circuit **16** is packaged in the standard SOIC package. The antenna port "BS3" provides another option for configuring a backscatter antenna. The antenna port "BS3" supplies a one milliamp current and can drive an external PIN diode that would be situated between the two halves of the dipole antenna or any other suitable antenna. The other side of that external PIN diode can be returned to either the antenna port "BS1" or "BS2." Because PIN diodes are good shorting and opening devices for backscatter applications, the transmission range of a device **12** built with the integrated circuit **16** can be extended over the range that is obtained using only the internal circuitry of the integrated circuit **16**. This is at the expense of the need for an external component and an accompanying increase in cost of the device **12**.

FIGS. **8**.**07**AA–BB provide a partial circuit drawing illustrating a 915 MHZ transmitter "tx**915**" that can be included instead of the active transmitter described above. The transmitter "tx**915**" has one less stage of doubling. The chip rate also changes.

FIGS. **8**.**0701**AA–CB provide a circuit drawing of a VCO stage modified for use with the 915 MHZ transmitter "tx**915**" by adding capacitors to the output. The modified VCO stage is manufactured by making a metal mask adjustment employed in an alternative embodiment of the invention.

FIGS. **9**AA–CB provide a circuit drawing of the analog processor "analgproc." The analog processor "analgproc" includes a master bias source "mbs," voltage regulators "vrg" and "vrgtx," a bias OK circuit "biasok," an analog port current source "aportcs," an analog multiplexor decoder "asl," a random number clock generator "rcg" for the pseudo random number generator, a power up detector "pup," and an analog to digital (A/D) converter "ada_new." The analog multiplexor decoder "asl" is an address selector used, in one embodiment, to choose from among various possible inputs to the analog to digital converter. The power up detector "pup" puts out a master reset pulse upon power up. The power up detector also puts out another pulse that lasts throughout a power up cycle in which the processor performs operations appropriate upon power up, the last operation being to reset the wake up pulse. The random number clock generator "rcg" generates random numbers for use in arbitration schemes and generates a pseudo-random sequence. The master bias source "mbs" includes a band gap regulator. The voltage regulators "vrg" and "vrgtx" generate supply voltages for various blocks of circuitry. The bias OK circuit "biasok" determines when the regulator voltage has reached a final level, and then enables the circuitry that is driven by the regulator.

Details of Low Battery Detection

The integrated circuit **16** includes a differential I/O op-amp or comparator comparing the voltage of the battery with a predetermined voltage (e.g., with band gap voltage). A low battery signal is generated if the voltage of the battery is less than the predetermined voltage. More particularly, one of the status registers is a battery status register and has a value indicating if the voltage of the battery is less than the predetermined voltage. The transmitter "tx" transmits the value of this battery status register via radio frequency when responding to commands from the interrogator. In the illustrated embodiment, a battery voltage detector is shown in FIGS. **16** (and in FIGS. **11** and **9**.**010304**AA–BB); however, the battery voltage detector can be provided in a different location of the integrated circuit **16**.

FIGS. **9**.**01**AA–DH provide a circuit drawing of the analog to digital converter "ada_new." In the illustrated embodiment, the analog to digital converter is substantially disabled and is used only to provide a latch circuit for reading the low battery voltage detector. In a preferred embodiment, the analog to digital converter is used in connection with analog sensors and to provide alarm signals when thresholds are exceeded.

FIGS. **9**.**0101**AA–CK provide a circuit drawing showing construction details of the differential I/O op-amp "dopamp" included in the analog to digital converter.

FIGS. **9**.**0102**AA–DH provide a circuit drawing showing construction details of an analog divider (divide by two) "adaprescale" included in the analog to digital converter.

FIGS. **9**.**0103**AJ–FP provide a circuit drawing showing construction details of a control PLA "adactl_new" included in the analog to digital converter circuit of FIGS. **9**.**01**AA–DH.

FIGS. **9**.**010301**AA–CC provide a circuit drawing showing construction details of a clock generator "adacgen_new" included in the control PLA.

FIGS. **9**.**010302**AA–AB provide a circuit drawing showing construction details of a control output driver "adacdrv_new" included in the control PLA.

FIGS. **9**.**010303**AA–AB provide a circuit drawing showing construction details of a control output driver "adacdrvn_new" included in the control PLA.

FIGS. **9**.**010304**AA–BB provide a circuit drawing showing construction details of a data latch "adadlat_new" which is included in the control PLA and which is presently used as part of the battery voltage detector.

FIGS. **9**.**0104**AA–DD provide a circuit drawing showing construction details of the analog bias circuit "adabias_new" included in the analog to digital converter.

FIGS. **9**.**02**AA–DK provide a circuit drawing of a Vdd power up detector "pup" included in the analog processor. The power up detector puts out a master reset pulse upon power up. The power up detector also puts out another pulse that extends throughout a power up cycle while the processor performs a number of operation, the last one of which is to reset the wake up pulse. The power up detector uses a thermal voltage generator, which is a circuit such as is used for the low power current controlled oscillator, described above. The thermal voltage generator generates a small current. The power up circuit "pup" further includes current mirrors, and a capacitor illustrated near the top center of

FIGS. **9.02**AA–DK. The current mirrors mirror the small current generated by the thermal voltage generator. The mirrored current holds down one side of the capacitor illustrated near the top center of FIGS. **9.02**AA–DK. When the power supply first rises from zero to its final value, whatever that might be (e.g., 3 Volts or 5 Volts), the capacitor couples up the bottom plate causing a signal to rise on a line "PWRUP." The small mirrored current then slowly discharges the bottom plate until "PWRUP" switches back low. A signal from before the final inverter producing "PWRUP" goes down to circuitry shown on the lower right of FIGS. **9.02**AA–DK. That circuitry provides a hard pull down on the bottom of the capacitor to impede any switching back and forth. After the "PWRUP" pulse, the circuitry switches the bottom of the capacitor back down to ground much more rapidly than the small mirrored currents could. The circuitry then resets so that the only thing left holding the bottom of the capacitor low is the small current mirrored from the thermal voltage generator. The power up detector also generates another pulse on a line "WAKEUP" shown on the right of FIGS. **9.02**AA–DK. This pulse goes high at the same time as the pulse on line "PWRUP" but does not come down at the same time. Instead, the pulse on the line "WAKEUP" does not come down until the processor issues a wake up acknowledge signal on line "WUACK." The processor does not issue the wake up acknowledge signal until completion of running of a wake up program stored in the ROM.

FIGS. **9.03**AA–BB provide a circuit drawing of a master bias source "mbs" included in the analog processor. The master bias source "mbs" includes a band gap reference generator "mbs_bgr" to generate bias voltages for various circuits of the integrated circuit **16**. The master bias generator includes a temperature compensated current generator "mbs_cur" that is employed in one embodiment of the invention, but is disconnected in the illustrated embodiment. The master bias source further includes a reference current generator "mbs_iref" that comprises current mirrors to replicate a reference current (e.g., 2.5 microAmps).

FIGS. **9.0301**AA–DJ provide a circuit drawing showing construction details of a band gap reference generator "mbs_bgr" included in the master bias source. Band gap reference generators produce a reference voltage, and are known in the art. See, for example, *Analysis and Design of Analog Integrated Circuits,* Paul R. Gray and Robert G. Meyer, John Wiley & Sons. The reference voltage produced is approximately equal to the band gap voltage of silicon, which is approximately 1.2 Volts. A band gap reference generator generates a voltage output that is independent of power supply and temperature.

FIGS. **9.0302**AA–DI provide a circuit drawing showing construction details of a temperature compensated current generator "mbs_cur" included in the master bias source.

FIGS. **9.0303**AA–CF provide a circuit drawing of the reference current generator "mbs_iref" included in the master bias source. The reference current generator "mbs_iref" biases various circuits of the integrated circuit **16**. The reference current generator "mbs_iref" includes current mirrors that replicate incoming current so that the reference current generator can supply the same value current to a number of different circuit blocks.

FIGS. **9.04**AA–CE provide a circuit drawing of the voltage regulator "vrg" included in the analog processor. The voltage regulator includes an op-amp having an input receiving a reference voltage "VREF" (which is approximately 1.2 Volts). The voltage regulator further includes a large p-channel device driven by the output of the op-amp. In the illustrated embodiment, the p-channel device is made up of a plurality of p-channel devices connected together in parallel. The voltage regulator further includes an output node "VREG" driven by the plurality of p-channel devices. The voltage regulator further includes a resistor divider, shown along the middle of the right side of FIGS. **9.04**AA–CE, connected to the output "VREG." The resistor divider includes a fifty percent point (having a voltage of half of the voltage at the output node "VREG") that is fed back to another input of the op-amp so that the voltage at the output node "VREG" is required to be two times the input voltage "VREF" to complete the feedback. In the illustrated embodiment, a number of individual regulators are employed in order to isolate power supplies to different areas of the circuit. However, in alternative embodiments, a reduced number of voltage regulators are employed.

FIGS. **9.05**AA–FE provide a circuit drawing of the voltage regulator "vrgtx" included in the analog processor. The voltage regulators "vrg" and "vrgtx" generate supply voltages approximately equal to two times band gap voltage (about 2.4 Volts) for various blocks of circuitry. The voltage regulator "vrgtx" provides substantially the same output voltage as the voltage regulator "vrg"; however, it has a bigger drive capability. The voltage regulator "vrgtx" is connected to the active transmitter which requires a lot of current.

FIGS. **9.0501**AA–CD provide a circuit drawing showing construction details of an operational amplifier without compensation "opampnc" included in the voltage regulator.

FIGS. **9.06**AA–DD provide a circuit drawing of a bias OK detector "biasok" included in the analog processor. The bias OK detector puts out a signal indicating that regulator voltage going to the receiver is at or near full level. The bias OK detector includes a voltage detector. A delay is built in so that adequate time is allowed. The bias OK detector allows biases to stabilize before releasing the clock recovery circuit and the wake up test logic.

FIGS. **9.07**AA–EG provide a circuit drawing showing construction details of an analog port current source "aportcs" included in the analog processor. The analog port current source "aportcs" provides a current which can be used to bias sensors external to the integrated circuit **16**. The value of the current supplied by the analog port current source "aportcs" is selected from several available values by a radio frequency command. In the illustrated embodiment, the analog port is not employed. However, in alternative embodiments, an analog port is used.

FIGS. **9.08**AA–CC provide a circuit drawing showing construction details of an analog multiplexer decoder "asl" included in the analog processor. The analog multiplexer decoder "asl" is an address selector. More particularly, in a preferred embodiment, the analog multiplexer decoder "asl" is used to choose from among various possible analog inputs to the analog to digital converter.

The random number clock generator "rcg" for the pseudo random number generator is shown in greater detail in FIGS. **9.09**AA–BB. The random clock generator generates random numbers for use in the arbitration scheme of the protocol to sort between multiple responding devices **12**.

Details of Low Power Pseudo Random Number Generator

The device includes a random clock generator "rcg" including a linear feedback shift register "rcg_osc" that has a plurality of stages and that generates a pseudo-random sequence. The random clock generator "rcg" includes an oscillator "rcg_osc" that supplies clock signals to the linear feedback shift register. The device includes a low current generator, such as a thermal voltage generator, to drive the

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oscillator that supplies clock signals to the linear feedback shift register. The shift register has two modes of operation; namely, a low power mode, and a high power mode. The random clock generator includes current mirrors referenced to the low current generator. In the low power mode, the current to each stage of the shift register is limited by the current mirrors. In the high power mode, the current mirror device gates are driven to full supply voltages. This allows the shift register to operate at a higher frequency appropriate for shifting the random number into the processor.

This technique is illustrated, with reference to an inverter, in a simplified schematic in FIG. **37**. FIG. **37** shows a circuit including series connected p-type transistors **210** and **212**, and series connected n-type transistors **214** and **216** which are connected in series with the p-type transistors **210** and **212**. The transistors **210**, **212**, **214**, and **216** are connected between a positive voltage "V+" and ground. The transistor **210** has a gate connected to a voltage "V BIAS P" and the transistor **216** has a gate connected to a voltage "V BIAS N."

When "V BIAS N" and "V BIAS P" are controlled by a low current current mirror (low power mode), the turn-on voltages of transistors **210** and **216** are small and current through inverter transistors **212** and **214** is limited. When "V BIAS N" is pulled to "V+" and "V BIAS P" is pulled to ground, the inverter operates at full speed.

FIGS. **9.09**AA–BB provide a circuit drawing showing construction details of the random clock generator "rcg" included in the analog processor. The random clock generator "rcg" includes a low power oscillator and bias generator "rcg_osc." The random clock generator "rcg" further includes the linear feedback shift register "rcg_sreg." The random clock generator "rcg" further includes a clock generator "rcg_clkgen" which generates non-overlapping versions of the clock which drives the linear feedback shift register "rcg_osc." The linear feedback shift register "rcg_osc" generates the pseudo-random sequence. The random clock generator further includes circuitry (shown below the linear feedback shift register in FIGS. **9.09**AA–BB) for switching between clock schemes. This circuitry includes an n-channel device and a p-channel device (shown as circles with x's through them in FIGS. **9.09**AA–BB) allowing connection or blocking connection between the input and the output of the devices. The alternate clock sources are state one "**S1**," state three "**S3**," and phase two "**P2**" from the processor clock. The shift register is operable in a high power mode and in a very low power mode. When the processor wants a random number from the shift register "rcg_osc," these clocks are used and the shift register is operated in the high power mode to shift eight bits at a time in serial fashion into the processor. A total of sixteen bits are transferred, so two transfers of eight bits each take place. At other times, the shift register is in the very low power mode and is driven by the clock generated by the low power oscillator. In this manner, the shift register "rcg_osc" sequences through its pseudo-random sequence continuously in the background until the shift register is called upon to provide a number.

FIGS. **9.0901**AA–CH provide a circuit drawing showing construction details of the linear feedback shift register "rcg_sreg" included in the random clock generator. In the illustrated embodiment, the linear feedback shift register "rcg_sreg" is a [**17,3**] shift register having an output in register seventeen. The input to the first register is the exclusive-or of registers seventeen and three. The linear feedback shift register "rcg_sreg" includes seventeen stages, so it produces a sequence of $2^{17}-1$. Therefore, the odds of two devices **12** being at the same place in the sequence are low.

FIGS. **9.090101**AA–CC provide a circuit drawing showing construction details of a shift register zero bit "rcg_sregbit**0**" included in the linear feedback shift register. This bit is different from others so that it can power up in a particular state. The shift register will function to deliver a sequence of pseudo-random numbers as long as all registers are not allowed to go to zero. Therefore, the zero bit "rcg_sregbit**0**" of the shift register is altered to guarantee that it will be a one on power up. The shift register bit "rcg_sregbit**0**" shown in FIGS. **9.090101**AA–CC also includes a series of n-channel and p-channel devices to limit current in the logic gates. When the random clock generator is in the low power mode, the bias voltages on these series devices allow only very small currents; however, when the random clock generator is operating in the high power mode (when the processor is shifting in a random number) then these nodes are driven to full supply. A line "BIASN" will be driven to Vdd, and a line "BIASP" will be driven to ground. Then the logic of the random clock generator operates in a normal mode.

FIGS. **9.090102**AA–BB provide a circuit drawing showing construction details of a shift register bit "rcg_sregbit" included in the linear feedback shift register.

FIGS. **9.0902**AA–FL provide a circuit drawing showing construction details of the low power oscillator and bias generator "rcg_osc" included in the random clock generator. The low power oscillator includes a thermal generator, as in previously described circuitry. The low power oscillator and bias generator "rcg_osc" further includes bias voltage generators shown in the middle and at the bottom in FIGS. **9.0902**AA–FL. The bias voltage generator shown at the bottom in FIGS. **9.0902**AA–FL includes extra transistors to allow switching between high and low power states.

FIGS. **9.0903**AA–CC provide a circuit drawing showing construction details of a clock generator "rcg_clkgen" included in the random clock generator.

The PN processor "pnproc" shown in FIGS. **6**AA–EK is the spread spectrum processing circuit **40** shown in FIG. **5**. The PN processor "pnproc" performs spread spectrum processing. Spread spectrum modulation is described elsewhere. The PN processor "pnproc" is shown in greater detail in FIGS. **10**AA–DD.

The PN processor "pnproc" shown in FIGS. **10**AA–DD includes a digital PN correlator "dcorr." The correlator receives a data stream on line "RXCHIPS" that comes from the receiver. The correlator has a thirty-one chip register and performs a comparison of the chip pattern of the incoming data stream with the expected thirty-one chip pattern. When there is a total or near match, the correlator "dcorr" puts out a high signal (a one) on line "RXDATA." When there is a nearly total mismatch, the correlator "dcorr" puts out a low signal (a zero) on line "RXDATA." Every thirty-one chips, "RXDATA" either changes state or does not change state, depending on whether the PN sequence was inverted or not inverted (i.e., depending on whether a zero or one was defined by the thirty-one chip sequence). The output of the correlator "dcorr" on line "RXDATA" is a sequence of true, non-encoded, data bits of ones and zeros.

The PN processor further includes a PN lock detector "pnlockdet." The lock detector is a circuit that determines whether a preamble is present. In the illustrated embodiment, the preamble is all zeros. Therefore, the lock detector "pnlockdet" determines whether or not a certain length of zeros have occurred in a row. In the illustrated embodiment, the lock detector "pnlockdet" determines whether or not four zeros occurred in a row. The lock detector "pnlockdet" has an output that is connected to the

serial input output circuit "sio" in the processor, and enables the processor to look for the Barker or start code.

The PN processor further includes a clock "pngclk." The clock "pngclk" is a clock generator that is based on a clock signal "CHIPCLK" produced by the digital clock and data recovery circuit "dcr." The clock "pngclk" puts out non-overlapping true and compliment versions of the clock and these are used to drive circuitry in the PN processor.

The PN processor further includes a shift register "pngshr." The shift register is a block of logic that can be used to generate a thirty-one chip sequence, a sixty-three chip sequence, and a two hundred and fifty-five chip sequence. A thirty-one chip sequence is always used for receiving, but for transmitting multiple selections are available. In the illustrated embodiment, the integrated circuit **16** is wired to allow a selection between thirty-one and sixty-three chips. In alternative embodiments, it can be wired to allow a selection between thirty-one and two hundred and fifty-five chips, or between thirty-one and sixty-three chips. In the receive mode, the PN sequence is not used explicitly, except that the middle chip and the last chip in the sequence are detected, and those signals are used by circuitry labelled "Bit Rate Clock Generator" in FIGS. **10**AA–DI to generate a bit rate clock for the transmitter and receiver. Thus, the output of this shift register "pngshr" is used to generate a bit rate clock, on line "TRCLK." In the transmit mode, if a modulation scheme has been selected that uses spread spectrum encoding, the output of this shift register is used to encode the data.

The PN processor further includes a differential and PN encoder "dpenc." The differential encoder performs differential encoding and PN encoding. The differential encoder includes an input connected to a line "TXDATA." The data on line "TXDATA" is differential encoded by the differential encoder, if differential encoding is selected. Both polarities of differential encoding are provided for and are selected depending on the desired modulation scheme. The differential and PN encoder can also impress the PN code on the data "TXDATA" if this is selected.

The PN processor further includes a PSK/FSK generator "fskgen." In the illustrated embodiment, PSK (phase shift keying) is performed by the PSK/FSK generator "fskgen." In an alternative embodiment, FSK (frequency shift keying) is performed by the PSK/FSK generator "fskgen." The generator "fskgen" has both a last chip complement output "FSKLASTCHIP" and a mid chip complement output "FSKMIDCHIP." These outputs are connected to the bit rate clock generator and override the outputs from the PN generator shift register "pngshr". The bit rate clock generator then generates the appropriate bit rate clock.

The PN processor further includes D type flip-flops "pnddff," one of which is included in the bit rate clock generator.

The PN processor further includes circuitry shown on the lower right in FIGS. **10**AA–DD that provides for test modes. This circuitry provides a way to bring a modulating signal for the transmitter out to a digital pad "DIGTXOUT" depending on whether an enable signal is placed on an enable pin "DIGTX." The enable signal on enable pin "DIGTX" is also used, in connection with a signal on line "ForceRXON" to force the receiver to receive in a continuous fashion. The output of the receiver is routed to a line "TESTRXDATA" and that signal is routed to a digital output pad (the digital pad "DIGTXOUT" in the illustrated embodiment).

FIGS. **10.01**AA–DJ provide a circuit drawing showing construction details of the digital PN correlator "dcorr" included in the PN processor. The correlator "dcorr" includes a bias generator "dcor_bias" that generates bias currents for other circuitry included in the correlator. The correlator "dcorr" further includes a shift register "dcorr_sreg." The shift register "dcorr_sreg" performs a chip by chip comparison between the incoming data stream and the expected thirty-one chip PN sequence. For each chip that agrees, the shift register "dcorr_sreg" puts out a current on a line "Iagree." For each chip that is in disagreement, the shift register "dcorr_sreg" puts out a current on a line "Idisagree." Currents are added for each of the thirty-one chips on these lines "Iagree" and "Idisagree." The PN correlator "dcorr" further includes two comparator structures shown in the middle of FIGS. **10.01**AA–DJ as an upper comparator and a lower comparator. The upper comparator has current biasing defining a threshold, and the lower comparator has current biasing defining a threshold. When a sufficient number of currents flow from the shift register "dcorr_sreg" into the "Iagree" line to overcome the threshold set by the current biasing in the upper comparator, a one is detected, and the circuit puts out a digital one. If, on the other hand, the currents in the "Idisagree" line are high enough to overcome the threshold set by the current biasing in the lower comparator, a zero is detected, and the circuit puts out a digital zero. In other cases, the output does not change. The correlator further includes circuitry shown on the right of FIGS. **10.01**AA–DJ that synchronizes the data stream out of the correlator and into other information processing circuitry.

FIGS. **10.0101**AA–BG provide a circuit drawing showing construction details of the PN correlator shift register "dcorr_sreg" included in the PN correlator. The shift register "dcorr_sreg" performs a chip by chip comparison between the incoming data stream and the expected thirty-one chip PN sequence. For each chip that agrees, the shift register "dcorr_sreg" puts out a current on a line "Iagree." For each chip that is in disagreement, the shift register "dcorr_sreg" puts out a current on a line "Idisagree."

FIG. **10.010101** provides a circuit drawing showing construction details of a PN correlator bit "dcorr_bit" included in the PN correlator shift register.

FIG. **10.01010101** provides a circuit drawing showing construction details of a shift register cell "dcorr_sregbit" included in the PN correlator bit.

FIGS. **10.0102**AA–CN provide a circuit drawing showing construction details of a correlator bias generator "$dcorr_{13}$ bias" included in the PN correlator.

FIGS. **10.02**AA–BE provide a circuit drawing showing construction details of a PN lock detector "pnlockdet" included in the PN processor. The PN lock detector "pnlockdet" detects the preamble by counting. For example, in the illustrated embodiment, the PN lock detector "pnlockdet" determines that a preamble has been received if the lock detector counts four consecutive zeros in a row. If the PN lock detector does not achieve the four consecutive zeros, it resets and starts counting again.

FIGS. **10.0201**AA–AB provide a circuit drawing showing construction details of a counter bit "lockcounterbit" included in the PN lock detector.

FIGS. **10.03**AA–AB provide a circuit drawing showing construction details of the PN generator clock "pngclk" included in the PN processor. The PN generator clock is a non-overlapping clock generator.

FIGS. **10.04**AA–CE provide a circuit drawing showing construction details of a PN generator shift register "pngshr" included in the PN processor. The PN generator shift register has select lines so that various sized PN sequences can be

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generated (e.g. thirty-one, sixty-three, or two hundred and fifty-five chip sequences). The PN generator shift register also includes circuitry for generating mid chip and last chip signals "MIDCHIP" and "LASTCHIP" which are used for generating the bit rate clock.

FIG. **10**.**0401** provides a circuit drawing showing construction details of a PN generator shift register cell "pngsreg" included in the PN processor.

FIGS. **10**.**0402**AA–CB provide a circuit drawing showing construction details of a PN generator shift register summer "pngssum" included in the PN generator shift register.

FIG. **10**.**05** is a circuit drawing showing construction details of a PN controller D type flip-flop "pnddff" included in the PN processor.

FIGS. **10**.**06**AA–DH provide a circuit drawing showing construction details of differential and PN encoder "dpenc" included in the PN processor. The differential and PN encoder includes circuitry shown on the left in FIGS. **10**.**06**AA–DH which performs differential encoding. The circuitry encodes data such that zeros in the incoming data cause the output to transition from either zero to one or one to zero, and ones in the incoming data cause the output not to transition. Other forms of differential encoding can be performed. For example, the circuitry can encode data such that ones in the incoming data cause the output to transition from either zero to one or one to zero, and zeros in the incoming data cause the output not to transition. A selection of one of these two forms of differential encoding is performed by placing a high or low signal on a selection line "DIFFSEL." Whether or not differential encoding takes place at all is also selectable. The differential and PN encoder further includes circuitry shown on the right in FIGS. **10**.**06**AA–DH which PN encodes the data, if spread spectrum modulation is selected.

FIGS. **10**.**07**AA–CD provide a circuit drawing showing construction details of a PSK/FSK generator "fskgen" included in the PN processor. The PSK/FSK generator "fskgen" takes as its input a clock which runs at the chip rate (9.538 MHz in the illustrated embodiment). The PSK/FSK generator "fskgen" generates a tone for phase shift keying (e.g., 596 kHz in the illustrated embodiment). The PSK/FSK generator "fskgen" further includes circuitry shown at the bottom in FIGS. **10**.**07**AA–CD which switches phase according to the input data. In other words, this circuitry compliments ones to zeros, and zeros to ones according to input data. If PSK or FSK is not selected, data passes through the PSK/FSK generator unaltered.

FIGS. **10**.**0701**AA–AB provide a circuit drawing showing construction details of a FSK counter bit "fskcbit" included in the PSK/FSK generator.

FIGS. **11**AA–AB provide a circuit drawing of a battery I/O buffer "batalg" included in the integrated circuit **16**. In one embodiment, battery voltage is compared to band gap voltage (produced by the band gap reference generator) using an op-amp. In one embodiment, the battery I/O buffer "batalg" is used to connect a voltage to the analog to digital converter; however, in the illustrated embodiment, this function is performed by a circuit "tsn." The circuit "tsn" includes an enable line, and includes a resistor divider. When an enable signal is placed on the enable line, the resistor divider is tapped, and the output of the resistor divider goes to an op-amp for comparison with band gap voltage.

In order to detect a low battery voltage, circuitry is provided which defines what is a low voltage. The lowest possible value at which an indication is given that the battery voltage is low is the value at which the integrated circuit **16** begins to fail to operate properly. However, in a preferred embodiment, an extra margin is provided so that there is time to replace the battery or replace the device before the integrated circuit **16** fails. For example, in one embodiment, the margin is 0.1 Volts. The circuitry "tsn" is therefore set up with a voltage divider having a tap compared to the band gap voltage. The voltage divider has resistor values selected so that when battery voltage is at the margin (e.g. 0.1 Volts) above the lowest possible value, the tap in the voltage divider has a voltage slightly below the band gap voltage (e.g., 1.2 Volts).

FIGS. **12**AA–AB provide a circuit drawing of a digital I/O pad buffer "paddig" included in the integrated circuit **16**. The digital I/O pad buffer is both an input and output buffer. The I/O pad buffer "paddig" has an input "DPAD" which is connected to a bond pad of the integrated circuit **16**. Data entering the pad buffer "paddig" from the input "DPAD" passes through an ESD protection device "esdl" and then passes on to whatever circuit for which it is an input (there are many such pad buffers "paddig" in the illustrated embodiment). Data to be output via the pad buffer "paddig" comes into the pad buffer "paddig" via a line "DOUT" along with an enable on line "ENABLE." The pad buffer "paddig" includes a static pull down device shown on the far right in FIGS. **12**AA–AB. The pad buffer "paddig" further includes n-channel and p-channel transistors shown in the right in FIGS. **12**AA–AB proximate the static pulldown device. If an enable signal is present on line "ENABLE" and "DOUT" is high, the two p-channel devices will turn on and pull the output pad "DPAD" high. If "DOUT" is low, the two n-channel devices will turn on and pull the output pad "DPAD" low. The pad buffer "paddig" further includes circuitry providing for gradual pulling high or pulling low to reduce transient currents. This is because a user may connect the pad to drive a heavy load.

FIG. **13** provides a circuit drawing of a digital input pad buffer "padigin" included in the integrated circuit **16**. FIG. **13** shows the input portion only of the pad buffer "paddig."

FIG. **14** provides a circuit drawing of an analog I/O pad buffer "padalg" included in the integrated circuit **16**. In one embodiment, the analog I/O pad buffer is used to connect an external sensor to the analog to digital converter.

Details of RF Selectable Return Link

The return link configuration logic "rlconfig" provides for user customization of operation of the transmitter "tx." Various customizations are possible. For example, the transmitter "tx" is selectable as operating in a backscatter transmit mode, or an active transmit mode in response to a command from the interrogator **26**. This is shown in FIGS. **21** and **22**. FIG. **21** is a simplified circuit schematic illustrating a transmitter "tx" switchable between an active mode and a backscatter mode, and employing separate antennas As**1** and As**2** for the active mode and the backscatter mode, respectively. If the active mode is selected, the micro controller connects the antenna As**1** to transmit the output of the transmitter, using switch S**1**. If the backscatter mode is selected, the micro controller **34** connects the antenna As**2** to transmit the output of the transmitter, using switch S**2**. In an alternative embodiment, shown in FIG. **22**, the transmitter "tx" is still switchable between an active mode and a backscatter mode, but employs the same antenna **46** for both the active mode and the backscatter mode.

If the backscatter mode is selected, the interrogator **26** sends a continuous unmodulated RF signal while the transmitter "tx" transmits a response to a command from the interrogator **26**. The clock recovered from the incoming message is used to derive a subcarrier for the transmitter "tx." In the illustrated embodiment, the subcarrier for the

transmitter "tx" is a square wave subcarrier. The response to the interrogator is modulated onto the square wave subcarrier by the device **12** using a selected modulation scheme. For example, the response can be modulated onto the subcarrier using Frequency Shift Keying (FSK), or Binary Phase Shift Keying (BPSK).

If the active transmit mode is selected, the transmitter **32** is selectable as using amplitude modulation, or bi-phase (Binary Phase Shift Keying) modulation. The transmitter **32** is selectable as using differential coding, and/or spread spectrum coding. There are various combinations of options that can be selected through the commands that are sent to the integrated circuit **16** by the interrogator **26**. The transmitter **32** is selectable as using the thirty-one chip spread spectrum sequence, or a narrow band.

These options provide for a wide range of possible applications or uses for the integrated circuit **16**, and provide for the possibility of using different schemes in an application for different purposes. For example, an active transmit can be selected for certain purposes, while a backscatter transmit can be selected for different purposes.

FIGS. **15**AA–BC provide a circuit drawing of return link configuration control logic "rlconfig." The return link configuration control logic "rlconfig" has inputs "TXSEL**0**," "TXSEL**1**," and "TXSEL**2**." The values on these inputs are defined by a radio frequency command sent by the interrogator. These inputs "TXSEL**0**," "TXSEL**1**," and "TXSEL**2**" are connected to the outputs of an output register "oreg" included in the processor. The return link configuration logic takes each possible combination of inputs "TXSEL**0**," "TXSEL**1**," and "TXSEL**2**" (there are a total of 2×2×2=8 possible combinations) and asserts appropriate control signals to enable the desired return link configuration. The signals being controlled by the return link configuration control logic "rlconfig" are: "ENDIL" for enabling the data interleaver; "PNOFF" for selecting whether or not PN encoding is employed for data transmitted by the device **12**; "DIFFSEL" for selecting which polarity of differential encoding is used for transmitted data; "DIFFON" for selecting whether or not differential encoding is employed for transmitted data; and "ENFSK" for selecting FSK (or PSK in an alternative embodiment) for transmitted data; "BSCAT" for enabling backscatter for transmitted data; and "ENABLEAM" enables amplitude modulation.

The integrated circuit **16** further includes a number of sensors, such as sensors "batalg," "tsn," and "mag," in the embodiments where an A/D converter is included in the analog processor "anlgproc." The sensor "batalg" is a battery voltage detector, the sensor "tsn" is a temperature sensor, and the sensor "mag" is a magnetic sensor. These sensors will be connected to the A/D converter in the analog processor "anlgproc" in one embodiment of the invention. In one embodiment, one or more of these sensors are not included or not used.

Using such sensors, the device **12** can monitor things such as its own battery voltage, its temperature and detect the presence of a magnetic field. There are various possible uses for information sensed by such sensors. For example, events can be counted so that, depending on the user's application, the user can determine whether or how many times a certain item was exposed to temperature above or below a certain value (e.g., to determine likelihood of spoilage or damage). Alternatively, the user can determine whether or how many times a certain item was exposed to a magnetic field of a certain value (e.g., when passing a certain location).

FIGS. **16**AA–EH provide a circuit drawing showing construction details of the temperature sensor "tsn." The temperature sensor "tsn" was designed to put out a voltage that is linearly proportional to temperature. In the illustrated embodiment, the circuit "tsn" has been reconfigured for use as a low battery voltage detector.

FIGS. **16.01**AA–DI provide a circuit drawing showing construction details of an operational amplifier "opamp" included in the temperature sensor "tsn."

FIGS. **17**AA–BB provide a circuit drawing of a magnetic field sensor "mag." The magnetic field sensor senses magnetic fields.

FIGS. **18**AA–AB provide a circuit drawing showing a chip bypass capacitor "bypcap**3**." The capacitor "bypcap**3**" is a integrated circuit decoupling capacitor between Vdd and ground.

FIG. **19**AA–EK provide a circuit drawing of a semiconductor integrated circuit in accordance with an alternative embodiment of the invention. The integrated circuit of FIGS. **19**AA–EK is similar to the integrated circuit shown in FIGS. **6**AA–EK, like components having like component names, except that the integrated circuit of FIGS. **19**AA–EK has no ROM, and is intended to be connected to an external ROM. This is useful for test purposes.

FIGS. **20**AA–DF provide a circuit drawing of a data processor "dataproc_t**3**" to be used in the integrated circuit of FIG. **19** in place of the data processor "dataproc." The data processor "dataproc_t**3**" has an interface to external ROM.

FIGS. **20.01**AA–CB provide a circuit drawing of an interface "extrom" to an external ROM.

FIGS. **20.0101**AA–BB provide a circuit drawing of external ROM control logic "extromctl" included in the interface "extrom."

FIG. **20.0102** is a circuit drawing of an external ROM address interface "extromad" included in the interface "extrom."

FIGS. **20.0103**AA–AC provide a circuit drawing of a digital I/O pad buffer "paddigt**3**" included in the interface "extrom." The digital I/O pad buffer "paddigt**3**" is the pad driver for the external ROM.

FIG. **20.0104** is a circuit drawing of an external ROM databus interface "extromdb" included in the interface "extrom."

FIGS. **6**AA–EK also illustrate bonding pads "PAD AA," and "PAD A," "PAD B," "PAD C," "PAD D," "PAD E," "PAD F," "PAD G," "PAD H," "PAD I," "PAD J," "PAD K," "PAD L," "PAD M," "PAD N," "PAD O," "PAD P," "PAD Q," "PAD R," "PAD S," "PAD T," "PAD U," "PAD V," "PAD W," "PAD X," "PAD Y," and "PAD Z," which are provided around the edge of the die of integrated circuit **16**. In the illustrated embodiment, the integrated circuit **16** includes a standard **20** lead SOIC package; however, any appropriate integrated circuit package can be employed.

Connections to these pads are brought out of the package and are accessible to the user. In this way, the user can somewhat tailor the function of the integrated circuit **16** to their application. In one embodiment, however, the entire device **12** is encapsulated in a housing such as that shown in FIG. **3**.

The pads P and Q are digital port data and clock pads, and work together to provide a serial input or output, or a digital connection outside the integrated circuit. For example, if desired, data can be transmitted to the integrated circuit **16** via radio frequency, and a response can be put out on the digital port data pad, or vice versa.

The pad R is a chip enable pad, and prevents wake up to look for an incoming radio frequency signal. There are some applications or uses where the user knows that there will be

certain periods of time when no valid radio frequency signals will be presented to the integrated circuit **16**. The user will want to prevent the integrated circuit **16** from leaving the sleep mode so that power can be saved, and the life of the battery **18** can be extended.

The pad S is a test mode pad for testing. When the integrated circuit **16** is powered on (i.e., when power is first applied), if that pad is held high then the micro controller **34** goes into a self-test mode. After the self-test, if the pad S is no longer held high, the integrated circuit **16** goes to the sleep mode, and periodically awakens to look for valid radio frequency signals, as it normally would. This pad S is useful to the manufacturer of the integrated circuit **16**, such as for testing prior to packaging the die of the integrated circuit **16** in the housing of the integrated circuit **16**.

The pad T is a digital transmit pad, and the pad U is a digital transmit data pad. These pads are useful for testing. They allow the integrated circuit **16** to operate in its intended manner, except that, if the pad T is held high, data from the integrated circuit **16** is brought out as a digital signal on the pad U instead of being transmitted via radio frequency using transmitter "tx."

If the pad I is held high, data to the integrated circuit **16** is brought in as a digital signal on the pad H instead of being received via radio frequency using receiver "rx". Details of the logic associated with this function are included in the FIG. **8.01** in connection with lines "DIGRX" (associated with pad I) and "DIGRXDATAY" (associated with pad H). This logic includes the NAND gates and invertors shown leading from the lines "DIGRX" and "DIGRXDATA" to a line "DataIn."

These pads T, U, I, and H provide for testing of most functions of the integrated circuit **16** without the need to use high frequency radio signals. High frequency radio signals may not always be convenient in a testing lab. The pads T and U do not provide for testing of some functions relating to radio frequency transmission, and the pads I and H do not provide for testing of some functions relating to radio frequency reception (e.g., operation of the Schottky detector). These pads T, U, V, and H do provide for testing of the spread spectrum processing circuit **40**, and for processing of protocol commands described in the appended microfiche. This allows everything but operation of radio frequency transmitter **32** and receiver **30** to be checked prior to proceeding with that radio frequency testing. It also provides a function for the user, in that the integrated circuit **16** does not necessarily need to be used as a radio frequency identification device. The integrated circuit **16** has a receiver, and a transmitter, and it can be used for various purposes, such as an actuator or beacon. If it is not necessary to have a radio transmission or reception of data, either one or both form of data can be passed directly through the pads in digital form.

Note that there are separate enables T and I associated with transmitting or receiving digital data. For example, if the digital transmit pad T is taken high, then the transmitter "tx" will not cause a radio frequency signal to travel to antenna **46** but instead outgoing responses will come out on the pad U. However, the receiver "rx" will operate normally unless the digital receive pad I is taken high.

The pad V is a TX clock pad, or transmit clock pad. Pad V was intended to be an external input that could be used for a clock for the transmitter **32** instead of the clock recovered from the incoming signal. In some applications, it may be necessary to have a clock that is more stable than the recovered clock, and the pad V provides a way for the user to supply such a clock. For example, the user may connect a crystal oscillator, external to the integrated circuit **16**, and that way achieve a very stable carrier frequency for the transmitter "tx." In the illustrated embodiment, pad V has been reconnected to provide a signal which can be used to activate an external, high performance radio.

The pads Y, Z, AA, A, and D are antenna pads for connecting the receiver **30** and transmitter **32** to the shared antenna **14** or the multiple antennas **44** and **46**. In the preferred embodiment, circuitry that interfaces these pads is physically located on the die next to these pads. More particularly, the microwave outputs of the transmitter **32** are arranged on the die so as to be next to (in close physical proximity to) the appropriate bond pads.

The pad B is a test RX or test receive pad, and the pad C is a test TX or test transmit pad. Because the integrated circuit **16** is usually in the sleep mode, but wakes up briefly to look for a valid incoming radio frequency signal, and then goes back to sleep, it can be difficult to test the receiver "rx" and the transmitter "tx." Therefore the pads B and C provide for forcing on the receiver "rx" and transmitter "tx," respectively, such as for testing. If a high signal is applied to the pad B, this forces the receiver "rx" to remain on. Similarly, if a high signal is applied to the pad C, this forces the transmitter "tx" to remain on.

If the pad B is used to force the receiver on in order to exercise the circuitry, such as through clock recovery, an input radio frequency signal is required at the appropriate frequency (e.g., 2.45 GHz) modulated with the spread spectrum code.

The pad E is a RX input or receive input pad. This pad is connected to a side of the Schottky detector where the base band signal is available. This pad is provided for test purposes and to allow the use of a high-performance Schottky diode external to the integrated circuit **16**.

The pad G is a VSS A pad, or analog VSS pad. The pad G is a connection to a ground bus that only goes to the analog circuitry.

Other pads J, K, L, M, N, O, and W are voltage supply or voltage drain pads (Vss or Vdd).

Protocol

A description of a protocol which can be employed by the device **12** for the commands, replies, and status information is contained is in a manual titled "Micron RFID Systems Developer's Guide." This manual relates to a device for use with an "AMBIT" (TM) brand tracking system as well as to the device **12**. Also relevant is U.S. Pat. No. 5,500,650 to Snodgrass et al., titled "Data Communication Method Using Identification Protocol," incorporated by reference.

Examples of commands that can be sent from the interrogator **26** to the device **12** are as follow:

Identify

An Identify function is used when attempting to determine the identification of one or more of the devices **12**. Each device **12** has its own identification number TagId. It is possible that the interrogator will receive a garbled reply if more than one tag responds with a reply. If replies from multiple tags are received, an arbitration scheme, discussed below, is used to isolate a single device **12**.

ReadAnalogPort

In one embodiment, a ReadAnalogPort function is provided which returns the voltage (eight-bit value) of a selected analog port on a device **12**.

ReadDigitalPort

A ReadDigitalPort function returns data read from a serial port of a device **12**.

ReadTagMemory

A ReadTagMemory function returns data from a user accessible portion of memory included in a device **12**.

ReadTagStatus

A ReadTagStatus function returns system information about a specified device **12**. For example, in response to this command, the device **12** will transmit a confirmation of its TagId, a tag revision number, the low battery status bit, and other information.

SetAlarmMode

In one embodiment, a SetAlarmMode function is provided which is used to determine if a set point has been exceeded on an analog port of the device **12** (e.g., if a sensor senses a condition exceeding a predetermined threshold). There are three alarm modes: SET_HIGH_BAND_ON_ALARM, SET_LOW_BAND_ON_ALARM, and SET_STATUS_REG_ON_ALARM.

The SET_HIGH_BAND_ON_ALARM mode sets a device **12** to a low data band, and clears a bit in the device's status register indicative of an alarm threshold being exceeded. When a set point (threshold) is violated, the device **12** will switch from the low data band to a high data band.

The SET_LOW_BAND_ON_ALARM mode sets a device **12** to a high data band, and clears a bit in the device's status register indicative of an alarm threshold being exceeded. When a set point (threshold) is violated, the device **12** will switch from the high data band to the low data band.

The SET_STATUS_REG_ON_ALARM mode does not change data bands, but will result in a bit ALARM_THRESHOLD_EXCEEDED in the status register being set if the set point is violated.

SetMemoryPartition

A SetMemoryPartition function defines (initializes) a block of user memory in a device **12** for memory partition. After being initialized, a partition may be used to store data using a function WriteTagMemory. Data may be read from the partition using a function ReadTagMemory. The number of partitions available on a device **12** can be determined using the ReadTagStatus function.

WriteAccessId

A WriteAccessId function is used to update an access identification AccessId for one of the memory partitions.

WriteDigitalPort

A WriteDigitalPort function is used to write data to the synchronous serial port of a device **12**.

WriteTagId

A WriteTagId function is used to update the TagId of a device **12**.

WriteTagMemory

A WriteTagMemory function is used to write to the user memory space UserMemory of a device **12**.

WriteTagsRegs

A WriteTagsRegs function is used to update selected or all registers of a device **12** including registers TagControlReg, LswTagId, TagStoredInterrId, TimedLockoutCounter, and DormantCounter for a range of RandomValueIds. This command can be used, for example, to disable a device **12**. If desired, the transmitter of a device **12** can be disabled while the receiver of that device **12** is left functional. This is accomplished using bits KILL_TAG_**0** and KILL_TAG_**1** in a register TagControlReg.

WriteTagRegsRandIdRange and WriteTagRegsTagIdRange

WriteTagRegsRandIdRange and WriteTagRegsTagIdRange functions are used to update registers of a group of devices **12**. The WriteTagRegsTagIdRange function updates selected or all registers, including registers TagControlReg, LswTagId, TagStoredInterrid, TimedLockoutCounter, and DormantCounter, for a range of TagIds.

Examples of interrogator commands are as follows:

GetCrntAntenna

A GetCrntAntenna function returns the current antenna set used to communicate with a device **12**.

GetCrntRetries

A GetCrntRetries function returns the number of times a command was re-transmitted during the last tag-specific command.

GetInterrStats

A GetInterrStats function returns record-keeping parameters if the interrogator performs this function.

GetReplyStats

A GetReplyStats function returns values that are specific to the last tag-specific reply if the interrogator processes this information.

SetInterrReps

A SetInterrRegs function is used to set various communication parameters on an interrogator. Not all of the parameters are used on all interrogators.

SetInterrTest

A SetInterrTest function is used during testing. This function should not be called in normal operation.

SetTimeouts

A SetTimeouts function is used to set the system watchdog timers.

A convenience command is described as follows:

IdentifyAll

An IdentifyAll function returns the number of devices **12** found within the system's communication range. The IdentifyAll reply parameters include the TagId and RandomValueId for each device **12** that is identified.

The sequence of steps performed by a device **12** upon receipt of an Identify command from an interrogator will now be provided, reference being made to FIGS. **55**–**57**.

FIG. **55** illustrates top level steps, held in ROM, performed by the data processor of the device **12** upon wake up (upon leaving a sleep mode **500**) for any reason. The sleep mode is described above.

At step **502**, a determination is made as to whether the device **12** is in a test mode. Test mode is enabled by holding a special pin high at power up time. If so, the data processor proceeds to step **504**; if not, the data processor proceeds to step **506**.

At step **504**, a test routine is performed. The current test routine checks the Rom, RAM, processor registers, and the timed lockout timer. After performing step **504**, the data processor proceeds to step **500** (the device **12** returns to the sleep mode).

At step **506**, a determination is made as to whether the device **12** is being powered up according to the status of a signal provided by a power up detector circuit. If so, the data processor proceeds to step **508**; if not, the data processor proceeds to step **510**.

At step **508**, a power up routine is performed which initializes the wakeup timer, sets up the control register, and clears the RAM. After performing step **508**, the data processor proceeds to step **500** (the device **12** returns to the sleep mode).

At step **510**, a determination is made as to whether a protocol request has been issued. If so, the data processor proceeds to step **512**; if not, the data processor proceeds to step **514**.

At step **512**, the data processor executes a command processing routine. The command processing routine is described in greater detail below, in connection with FIGS. **56**A–B. After performing step **512**, the data processor proceeds to step **500** (the device **12** returns to the sleep mode).

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At step **514**, a determination is made as to whether an alarm timer request has been issued. This occurs once each minute. If so, the data processor proceeds to step **516**; if not, the data processor proceeds to step **500** (the device **12** returns to the sleep mode).

At step **516**, the data processor performs an alarm timer routine, which in one embodiment allows a selected analog input to be compared against a threshold. The results of the comparison can be used to set a bit and optionally cause the chip to change data bands.

The command processing routine **512** is illustrated in greater detail in FIG. **56**.

At step **518**, high signals are placed on lines SIOENABLE and RFENABLE to enable the serial input output block "sio" and to enable radio frequency communications. After performing step **518**, the data processor proceeds to step **520**.

At step **520**, a determination is made as to whether RFDET is high indicating that an RF signal is still present at the receiver input. If so, the data processor proceeds to step **522**; if not, the data processor proceeds to step **524**.

At step **524**, the command processing routine is aborted, and the device **12** returns to the sleep mode.

Steps **522**, **526**, **528**, and **532** are used to determine whether a first byte of a command is received within a predetermined amount of time after the chip wakes up and successfully acquires the clock signal from the incoming preamble.

At step **522**, a counter is initialized according to the wakeup interval selected. After performing step **522**, the data processor proceeds to step **526**.

At step **526**, a determination is made as to whether the counter has counted down to zero. If so, the data processor proceeds to step **524**; if not, the processor proceeds to step **528**.

At step **528**, a determination is made as to whether the first byte of a valid incoming radio frequency signal has been detected. If so, the processor proceeds to step **530**; if not, the processor proceeds to step **532**.

At step **532**, the counter is decremented. After performing step **532**, the data processor proceeds to step **526**.

At step **530**, the data processor reads in a command string from the serial input output block "sio" and stores the command string in random access memory. The serial input output block "sio" controls transfer of an incoming radio frequency message from the receiver to the data processor. After performing step **530**, the data processor proceeds to step **534**.

At step **534**, the high signals on lines RFENABLE and SIOENABLE are cleared. After performing step **534**, the data processor proceeds to step **536**.

At step **536**, the receiver is turned off in order to conserve power. After performing step **536**, the data processor proceeds to step **538**.

At step **538**, a determination is made using CRC as to whether transmission occurred without errors. If so, the data processor proceeds to step **540**; if not, the data processor proceeds to step **524**. CRC is cyclic redundancy checking, a technique known in the art used to detect errors in transmission of data by the affirmation of error codes by both the sending and receiving devices. In one embodiment, a check sum is used in place of a CRC.

At step **540**, a determination is made as to whether the device **12** was killed by a previous command. If so, the data processor proceeds to step **542**; if not, the data processor proceeds to step **544**.

At step **542**, a determination is made as to whether the received command is a WriteTagRegs command which can reset the kill bits in the control register. If so, the data processor proceeds to step **544**; if not, the data processor proceeds to step **548**, which is identical to step **524** on the previous page of the diagram.

At step **544**, a determination is made as to whether a valid command token exists for the received command. If so, the data processor proceeds to step **546**; if not, the data processor proceeds to step **548**.

At step **546**, a determination is made as to whether variables TagID and InterrID transmitted to the device **12** correctly correspond to the identification number for the particular device **12** and the identification number for the interrogator with which the particular device **12** is to correspond. If so, the data processor proceeds to step **550**; if not, the data processor proceeds to step **548**.

At step **548**, the command processing routine is aborted, and the device **12** returns to the sleep mode.

At step **550**, the data processor jumps to code for the specific command that was received by radio frequency. If the command is an Identify command, the data processor will jump to step **552**, which is the start of an Identify command routine.

The Identify command routine is illustrated in FIGS. **57**A–B.

At step **554**, a determination is made as to whether a timed lockout has been set by a previously received command. If so, the data processor proceeds to step **556**; if not, the data processor proceeds to step **558**.

At step **556**, the Identify command routine is aborted, and the device **12** returns to the sleep mode.

At step **558**, a determination is made as to whether a variable "InterrID" transmitted to the device **12** correctly corresponds to the identification number for the interrogator with which the particular device **12** is to correspond. If so, the data processor proceeds to step **560**; if not, the data processor proceeds to step **556**.

At step **560**, Arbitration Lockout is cleared if this is requested. After performing step **560**, the data processor proceeds to step **562**.

At step **562**, a new random number is obtained if this is requested. After performing step **562**, the data processor proceeds to step **564**.

At step **564**, arbitration parameters are checked. After performing step **564**, the data processor proceeds to step **566**.

At step **566**, a determination is made as to whether the particular device **12** should respond. If so, the data processor proceeds to step **568**; if not, the data processor proceeds to step **556**.

At step **568**, reply parameters are assembled and stored in the RAM. After performing step **568**, the data processor proceeds to step **570**.

At step **570**, a battery status bit is updated to indicate whether the battery voltage is below a threshold value. This information is included in the reply to the Identify command that is sent to the interrogator. After performing step **570**, the data processor proceeds to step **572**.

At step **572**, CRC is calculated. After performing step **572**, the data processor proceeds to step **574**.

At step **574**, high signals are set on lines RFENABLE and SIOENABLE to enable radio frequency transmission and to enable the serial input output block which transfers the data to be transmitted (i.e., the reply parameters) from the processor to the transmit circuitry. After performing step **574**, the data processor proceeds to step **576**.

At step **576**, the device **12** sends a preamble, consisting of 2000 bits of alternating pairs of ones and zeros, to the

interrogator via radio frequency. After performing step **576**, the data processor proceeds to step **578**.

At step **578**, the device **12** sends the 13 bit start code to the interrogator via radio frequency. After performing step **578**, the data processor proceeds to step **580**.

At step **580**, the data processor sends a reply to the Identify command to the interrogator via radio frequency. After performing step **580**, the data processor proceeds to step **582**.

At step **582**, the high signals on lines RFENABLE and SIOENABLE are cleared. After performing step **582**, the data processor proceeds to step **584**.

At step **584**, transmit mode is cleared. After performing step **584**, the data processor proceeds to step **586**.

At step **586**, the processor pulses the Protocol Request Acknowledge signal which terminates the wakeup condition that initiated this entire routine. After performing step **586**, the data processor proceeds to step **588**.

At step **588**, the data processor returns certain control register bits to their proper states in preparation for sleep mode.

The processor then proceeds to step **500** and returns to sleep mode.

The sequence of steps performed by an interrogator to issue an Identify command will now be provided, reference being made to FIGS. **58–60**.

FIG. **58** illustrates steps performed by a host processor of the interrogator upon initialization. Initialization is started in step **600** by calling a function.

At step **602**, a determination is made as to whether an attempt is being made to open more than a maximum number of interrogators. If so, the host processor proceeds to step **604**; if not, the host processor proceeds to step **606**.

At step **604**, an appropriate error message is returned by setting the parameter RFID ErrorNum to the appropriate value, and a null value is returned to the calling function.

At step **606**, interrogator parameters are initialized. This includes initializing timeout values, interrogator types and ports. After performing step **606**, the host processor proceeds to step **608**.

At step **608**, a determination is made as to whether a valid interrogator IO port has been selected. If so, the host processor proceeds to step **612**; if not, the host processor proceeds to step **610**.

At step **610**, an appropriate error message is returned. The parameter RFID ErrorNum is set to the appropriate value and a null is returned to the calling function.

At step **612**, function addresses are assigned. This includes the function to compute CRCs or checksums and the input and output routines. After performing step **612**, the host processor proceeds to step **614**.

At step **614**, default communication values are assigned. This includes default selections for diversity and communication retries. After performing step **614**, the host processor proceeds to step **616**.

At step **616**, communication hardware is reset. This initializes the interrogator into a known state by resetting the hardware and clearing the I/O FIFO's. After performing step **616**, the host processor proceeds to step **618**.

At step **618**, a frequency synthesizer is initialized. This function programs the frequency synthesizer to the desired frequency. After performing step **618**, the host processor proceeds to step **620**.

At step **620**, a determination is made as to whether the frequency synthesizer is programmed properly. This function is used to abort the initialization process if the frequency synthesizer cannot be programmed, thereby preventing subsequent communications to occur on inappropriate frequencies. If so, the host processor proceeds to step **622**; if not, the host processor proceeds to step **624**.

At step **622**, an host memory pointer is returned that points to a structure that contains the initialized parameters. After performing step **622**, program control is returned to the Host Application Code.

At step **624**, an appropriate error message is returned in the RFID ErrorNum parameter and a null is returned to the calling function.

FIG. **59** illustrates an example of a software application, starting at step **630**, that calls the Identify function and causes the interrogator to transmit an Identify command via radio frequency.

At step **632**, the function shown and described above in connection with FIG. **58** is called. After a successful call to the open functions (step **632**) the host computer proceeds to step **634**.

At step **634**, a determination is made as to whether the function shown and described in connection with FIG. **58** was successfully opened. If so, the system proceeds to step **638**; if not, the system proceeds to step **636**.

At step **636**, the host processor exits the application (or takes whatever steps are appropriate within the intended application).

At step **637**, the parameters are initialized for an Identify Command.

At step **638**, an Identify function (described below in connection with FIG. **60**) is called. After performing step **638**, the host library function proceeds to step **640**.

At step **640**, a determination is made as to whether a good reply was received from the device **12**. If so, the host computer proceeds to step **642**; if not, the host processor proceeds to step **644**.

At step **642**, reply parameters received from the device **12** are printed, displayed, or otherwise used or processed. After performing step **642**, the host computer proceeds to step **646** where the application returns results and ends.

At step **644**, the host processor exits the application or takes whatever steps are appropriate for a given application.

FIG. **60** illustrates the sequence of steps performed by the host library function at the starting at step **650**, when an Identify command is issued to the device **12**.

At step **654**, the command buffer is packetized, using the host application initialized parameters. After performing step **654**, the host computer proceeds to step **656**.

At step **656**, the packet CRC is computed and stored at the end of the packet.

At step **658**, the packet including the CRC is stored in an interrogator transmit queue that operates in a first in, first out fashion. After performing step **658**, the host computer proceeds to step **659**.

At step **659**, the interrogator is commanded to output the packet to the RF.

At step **660**, a watchdog timer is set. After performing step **660**, the host computer proceeds to step **662**.

At step **662**, a determination is made as to whether a reply is available from the device **12**. If so, the host computer proceeds to step **668**; if not, the host computer proceeds to step **664**.

At step **664**, a determination is made as to whether the watchdog timer set in step **660** has expired. If so, the host computer proceeds to step **666**; if not, the host computer proceeds to step **662**.

At step **666**, the host computer returns no reply and terminates processing for the Identify command.

At step **668**, CRC is checked to ensure error free transmission from the device **12** to the interrogator. After performing step **668**, the host computer proceeds to step **670**.

At step **670**, the reply packet is read from the reply FIFO. After performing step **670**, the library routine proceeds to step **672**.

At step **672**, the reply packet is parsed into separate parameter buffers. After performing step **672**, the host library returns program control to the host application (step **674**), where processing for the Identify command terminates and the host application software continues.

Details of Arbitration

The arbitration of multiple interrogators per device **12** is a detection method based upon each interrogator using a unique interrogator ID (InterrId). The InterrId is sent to a device **12** in a command. The device **12** also stores an interrogator ID TagStoredInterrId. The TagStoredInterrId is only updated by a WriteTagRegsXXX command. A RcvdInterrId is included in replies from a device **12**. If a TagStoredInterrId does not match the RcvdInterrId then the tag will not respond with a reply.

The arbitration of more than one tag per interrogator **26** is accomplished by using an ArbitrationValue and an ArbitrationMask during an Identify command. Contained within each device **12** is a random value ID (RandomValueId) and an arbitration lockout (IDENTIFY_LOCKOUT) bit. The RandomValueId is set to a "random" binary number upon command by an interrogator. It may also be set by an Identify command setting a SELECT_RANDOM_VALUE bit in SubCmnd.

The following examples use a 1-byte ArbitrationValue for simplicity. If an interrogator **26** transmits an Identify command with its ArbitrationMask set to 0000 0000 (binary), all devices **12** in the receiving range will respond. If there is only one device **12**, communications may proceed between the interrogator **26** and device **12**. If there are multiple devices **12** responding, the interrogator **26** will detect a collision and will start the arbitration sequence. To start the arbitration sequence among multiple tags, the interrogator **26** instructs the tags to clear their IDENTIFY_LOCKOUT bit and (possibly) re-randomize their RandomValuId values. The ArbitrationValue 0000 0000 and ArbitratioMask 0000 0001 are then treansmitted to all devices **12** in range. The devices **12** perform a logical ANDing (masking) of th ArbitrationMask and the RandomValueId. If the result matches the ArbitrationValue sent by the interrogator **26**, the device or devices **12** will reply to the Identify command. If not, the interrogator **26** will increment the ArbitrationValue to 0000 0001 and try again.

The interrogator **26** then checks each of the possible binary numbers (0000 0000 and 0000 0001 in this case) in the expanded mask (0000 0001) for a response by a device **12**. If a single device **12** responds to one of these values, the interrogator **26** will reply by commanding it to set its lockout bit. If any collisions are detected at this mask level, the mask would be widened again by one bit, and so on through the eight bit wide mask (256 numbers). If no collisions are detected for a particular ArbitrationValue and ArbitrationMask combination, the TagId returned in the reply is used for direct communication with that particular device **12**. During the arbitration sequence with up to about one hundred devices **12**, the mask will eventually grow large enough such that all devices **12** can respond without collision. After the mask widens to four or five bits, more devices **12** have unique random numbers and single tag replies are received. Thus with each expansion of the ArbitrationMask, there are fewer and fewer tags left to Identify.

With a large number of tags in range, it is possible that several devices **12** will choose the same value for their RandomValueId. In this case, the complete mask will be used. Collisions will still occur and the remaining tags will be instructed to select a new Random ValueId. If an application dictates, for example, that one hundred tags will usually be present in range of the interrogator **26**, it would be advantageous to start with the mask set to eight bit wide (11111111) and count up through 256 instead of starting with the mask set at 0000 0000, followed by 0000 0001, 0000 0011, etc. Other arbitration schemes can be implemented by the user.

Applications

There are a large number of possible applications for devices such as the device **12**. Because the device **12** includes an active transponder, instead of a transponder which relies on magnetic coupling for power, the device **12** has a much greater range.

One application for devices **12** is inventory control to determine the presence of particular items within a large lot of products.

Another application for devices **12** is electronic article surveillance (EAS). The devices **12** can be attached to retail items in a store having an interrogator **26** at the exits, for detection of unauthorized removal of retail items. The merchant can deactivate or remove devices **12** from retail items for which proper payment has been made.

Another application for devices **12** is to track migration of animals.

Another application for devices **12** is to counteract terrorism by monitoring luggage entering a plane to ensure that each item of luggage that enters the plane is owned by a passenger who actually boards the plane. The devices **12** can also be used to monitor luggage to locate lost luggage.

The device **12** can be use to track packages, such as courier packages.

The device **12** can be used to track hazardous chemicals or waste to ensure that it safely reaches a proper disposal site.

The device **12** can be used for security purposes, to track personnel within a building. The device **12** can also be used for access control.

The device **12** can be used to monitor and manage freight transit. For example, interrogators **26** can be placed at the entrance and exit of a terminal (e.g., a rail or truck terminal), to monitor incoming and outgoing shipments of vehicles bearing the devices **12**.

The device **12** can be used to impede car theft. A European anti-theft directive (74/61/EEC) provides that all new car models sold after January 1997 must be fitted with electronic immobilizers and approved alarm systems. The devices **12** can be provided on keychains or within car keys, and interrogators **26** placed in cars, so that the vehicle will be inoperable unless the specified device **12** for a specific car is used. The interrogator **26** can control the door locks of a car, or the ignition of the car, or both. Because the device **12** includes memory, the interrogator **26** in the car can periodically automatically change values in the device **12** (like changing a password).

Devices **12** can be placed in cars and used in connection with electronic toll collections systems. Because the devices **12** can be used to identify the respective cars in which they are placed, interrogators **26** in toll plazas can charge appropriate accounts based on which cars have passed the, toll plaza.

Devices **12** can be placed in cars and used in connection with parking systems. Because the devices **12** can be used to identify the respective cars in which they are placed, interrogators **26** in parking areas can determine when a vehicle arrives and leaves a parking area.

The devices **12** can be used for inventory control of rental equipment.

The devices **12** can be used where bar code labels will not properly work because of harsh environmental conditions (e.g., grease, dirt, paint).

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

We claim:

1. A method for conserving power in a radio frequency identification device defined by a single integrated circuit including a microprocessor and receiver, the method comprising in the single integrated circuit periodically switching from a sleep mode to a receiver-on mode and performing the following tests to determine whether to further switch to a microprocessor-on mode, in which more power is consumed than in the receiver-on mode, because a valid radio frequency signal is present:

(a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode;

(b) determining if the radio frequency signal is modulated and has a predetermined number of transitions per a predetermined period of time and, if so, proceeding to step (c); and, if not, returning to the sleep mode; and

(c) determining if the modulated radio frequency signal has a predetermined number of transitions per a predetermined period of time different from the predetermined time of step (b) and, if so, switching from the receiver-on mode to the microprocessor on mode; and, if not, returning to the sleep mode.

2. A method in accordance with claim **1** wherein the radio frequency identification device further comprises a clock recovery circuit configured to recover a clock from the incoming radio frequency signals, the clock recovery circuit including a phase lock loop and wherein the tests further comprise:

determining whether frequency lock is achieved on the incoming radio frequency signal within a predetermined amount of time;

switching from the receiver-on mode to the microprocessor-on mode when the phase lock loop has achieved frequency lock within the predetermined time; and

returning to the sleep mode when the phase lock loop has not achieved frequency lock within the predetermined time.

3. A radio frequency communications device comprising:

a single integrated circuit including a transmitter and a receiver, the integrated circuit being configured to periodically check if a radio frequency signal is being received by the receiver, the integrated circuit further including a timer configured to set a time period for the checking, the timer having a frequency lock loop, the frequency lock loop including a current controlled oscillator, the integrated circuit being configured to recover a clock frequency from the received signal, the transmitter being configured to use the recovered clock frequency, the integrated circuit being configured to switch between a sleep mode, a receiver-on power mode in which more power is consumed than in the sleep mode and in which the checking takes place, and a microprocessor-on power mode in which more power is consumed than in the receiver-on power mode, the integrated circuit further including a variable value divider coupled to the output of the frequency lock loop, the value of the divider being programmable in response to a radio frequency command received by the receiver which contains data representing the desired value of the divider, so as to permit remote programming of the time period of the checking.

4. A radio frequency communications device in accordance with claim **3** and further comprising a selectively engageable countdown timer configured to prevent switching from the sleep mode to the receiver-on mode for a predetermined amount of time set by a radio frequency command, received by the receiver, containing data representing the desired amount of time.

5. A radio frequency communications device in accordance with claim **3** wherein the device is configured to receive and process commands from an interrogator transmitting a radio frequency signal and to enable the frequency lock loop only during processing of a command, to calibrate the timer to a clock frequency recovered from a received command.

6. A method for conserving power in a radio frequency identification device of a type including a single integrated circuit having a microprocessor, a transmitter, a receiver, and circuitry for performing the following:

periodically switching from a sleep mode to a receiver-on mode and performing tests to determine whether to further switch to a microprocessor-on mode, in which more power is consumed than in the receiver-on mode, because a valid radio frequency signal is present, the tests including counting transitions in spread spectrum data to determine if the number of transitions within a predetermined time period fall within a predetermined range and, if so, determining if chip lock has occurred and, if not, returning to the sleep mode;

if chip lock has occurred, determining if frequency lock has occurred and, if so, switching to a microprocessor-on mode and, if not, returning to the sleep mode; and

selectively disabling the periodic switching from the sleep mode for a predetermined amount of time, the selective disabling being performed in response to a radio frequency command, wherein the selective disabling cannot be cancelled by a subsequent radio frequency command, the selective disabling comprising setting a countdown timer, the length of the predetermined amount of time being a variable amount and being selectable from a number of predetermined selectable amounts of time via a radio frequency command.

7. A method of operating a radio frequency identification device comprising:

determining when a predetermined timer interval has elapsed;

providing, after determining that the predetermined timer interval has elapsed, a receiver wake-up signal;

asserting a bias control signal in response to the receiver wake-up signal to turn on a master receiver bias to provide electrical power to a radio receiver;

testing to verify presence of the master receiver bias;

repeating asserting the bias control signal when the testing determines that the master receiver bias is not present;

determining, when the testing determines that the master receiver bias is present, when a radio frequency signal

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is being received by the radio receiver and returning the radio receiver to the sleep mode when the radio frequency signal is not present;

determining when a first number of spread spectrum transitions of the radio frequency signal falls within in a predetermined first range of numbers and occurs during a first predetermined interval, and, when the first number of transitions within the predetermined first range of numbers does not occur during the first predetermined interval, returning the radio receiver circuit to the sleep mode;

determining when a second number of spread spectrum transitions of the radio frequency signal falls within a predetermined second range of numbers and occurs during a second predetermined interval, and, when the second number of transitions does not occur during the second predetermined interval, returning the radio receiver circuit to the sleep mode; and

providing a microprocessor wake-up signal to a microprocessor that is co-integrated in a single integrated circuit with the radio receiver circuit when the first number of transitions occurs during the first predetermined interval and the second number of transitions occurs during the second predetermined interval.

8. A method as claimed in claim **7** wherein the radio frequency identification device includes a wake-up controller circuit, wherein the determining when a predetermined time interval has elapsed is performed by the wake-up controller circuit, and returning the radio receiver to the sleep mode comprises:

turning off the master receiver bias; and

restarting a timer in the wake-up controller.

9. A method as claimed in claim **8**, further comprising:

receiving by the receiver and decoding by the microprocessor a wake-up timer interval reset signal for setting a new wake-up interval in a wake-up interval timer in the wake-up controller; and

resetting the wake-up interval in the wake-up timer in response to the wake-up timer interval reset signal.

10. A method as claimed in claim **7**, wherein asserting a bias control signal comprises turning on a bias control signal to turn on a master receiver bias to provide electrical power to a clock and data recovery circuit and a voltage controlled oscillator, the method further comprising, prior to providing a microprocessor wake-up signal and after determining when a second number of spread spectrum transitions of the radio frequency signal occurs during the second predetermined interval:

determining, during an interval of predetermined length, presence or absence of clock signal acquisition from the radio frequency signal by the clock and data recovery circuit, and, when absence of clock signal acquisition is determined, returning the radio receiver circuit to the sleep mode; and

determining, during an interval of predetermined length, when the voltage controlled oscillator and clock and data recovery circuit have acquired frequency lock, and, when absence of frequency lock is determined, returning the radio receiver to the sleep mode.

11. A method of operating a radio frequency identification device comprising:

determining, in a wake-up controller circuit, that a predetermined timer interval has elapsed, while the radio frequency identification devices is in a sleep mode requiring a first power level;

providing, when the predetermined interval has elapsed, a receiver wake-up signal to set the radio frequency identification device to a receiver on mode requiring a second power level greater than the first power level;

determining, when testing determines that the master receiver bias is present, when a radio frequency signal is being received by the radio receiver;

returning the radio receiver to the sleep mode when the radio frequency signal is not present;

enabling a master receiver bias when the radio frequency signal is present to set the radio frequency identification device to a test mode requiring a third power level greater than the second power level, the master receiver bias providing electrical power to a radio receiver, a clock and data recovery circuit and a voltage controlled oscillator;

initiating the voltage controlled oscillator to oscillate at a first frequency;

determining, by the wake-up controller, when a first number of spread spectrum transitions of the radio frequency signal occurs during a first predetermined interval, and, when the first number of transitions does not occur during the first predetermined interval, returning the radio receiver circuit to the sleep mode;

determining, by the wake-up controller, when a second number of spread spectrum transitions of the radio frequency signal occurs during a second predetermined interval, and, when the second number of transitions does not occur during the second predetermined interval, returning the radio receiver circuit to the sleep mode;

determining, during an interval of predetermined length, presence or absence of voltage controlled oscillator signal acquisition from the radio frequency signal by the clock and data recovery circuit, and, when absence of clock signal acquisition is determined, returning the radio receiver to the sleep mode; and

providing a microprocessor wake-up signal from the wake-up controller to a microprocessor that is co-integrated in a single integrated circuit with the radio receiver circuit and the wake-up controller when the first number of transitions occurs during the first predetermined interval and the second number of transitions occurs during the second predetermined interval, the microprocessor wake-up signal setting the radio frequency identification device to a processor-on mode requiring a fourth power level that is greater than the third power level.

12. The method of claim **11**, further comprising, prior to providing a microprocessor wake-up signal, determining, during a frequency lock interval of predetermined length, when the voltage controlled oscillator and clock and data recovery circuit have acquired frequency lock, and, when absence of frequency lock is determined, returning the radio receiver to the sleep mode.

13. A method of operating a radio frequency identification device comprising:

changing a state of the identification device from a sleep mode requiring a first power level to a second mode by turning a radio receiver in the identification device on in response to a first criterion, the radio receiver requiring a second power level greater than the first power level;

changing the state of the identification device from the second mode to a third mode when a second criterion

is met, the third mode requiring a third power level greater than the second power level, and, when the second criterion is not met, changing the state from the second mode to the sleep mode; and

changing the state of the identification device from the third mode to a fourth mode when a third criterion is met, the fourth mode requiring a fourth power level greater than the third mode, and, when the third criterion is not met, changing the state from the third mode to the sleep mode.

14. A method as claimed in claim **13** wherein changing the state to a fourth mode when a third criterion is met includes providing a microprocessor wake-up signal when a variable frequency oscillator achieves frequency lock with a received RF signal.

15. A radio frequency identification device comprising:

a radio receiver having an output;

a wake-up timer circuit providing a receiver wake-up signal to the radio receiver at predetermined intervals to change a state of the radio frequency identification device from a sleep mode requiring a first power level to a second mode requiring a second power level greater than the first power level;

a radio frequency signal detection circuit having an input coupled to the radio receiver output, the radio frequency detection circuit providing an output signal returning the radio frequency identification device to the sleep mode when no radio frequency signal is detected, the radio frequency signal detection circuit setting the radio frequency detection device to a third mode requiring more power than the second mode when a radio frequency circuit is detected;

a wake-up controller circuit having an input coupled to the radio receiver output, the wake-up controller circuit first testing the radio frequency signal to determine when a first number of spread spectrum transitions of the radio frequency signal occurs during a first predetermined interval, the wake-up controller circuit providing an output signal returning the radio frequency identification device to the sleep mode when the wake-up controller circuit determines that the first number of transitions does not occur during the first predetermined interval, the wake-up controller circuit then testing the radio frequency signal to determine when a second number of spread spectrum transitions of the radio frequency signal occurs during a second predetermined interval and providing an output signal returning the radio frequency identification device to the sleep mode when the wake-up controller circuit determines that the second number of transitions does not occur during the second predetermined interval;

a clock and data recovery circuit including a phase-locked loop, the clock and data recovery circuit having an input coupled to the radio receiver output, the clock and data recovery circuit determining, during an interval of predetermined length, presence or absence of voltage controlled oscillator signal acquisition from the radio frequency signal and returning the radio receiver to the sleep mode when absence of clock signal acquisition is determined; and

a microprocessor having a data input coupled to the radio receiver output and a control input coupled to the wake-up controller circuit, the wake-up controller circuit providing a microprocessor wake-up signal to the microprocessor when the first number of transitions occurs during the first predetermined interval, the second number of transitions occurs during the second predetermined interval and the wake-up controller determines presence of voltage controlled oscillator signal acquisition from the radio frequency signal, the microprocessor wake-up signal setting the radio frequency identification device to a processor-on mode requiring a fourth power level that is greater than the third power level.

16. A radio frequency identification device comprising:

a radio receiver having an output and a control input;

a microprocessor having a data input coupled to the radio receiver output and having a control input;

a timer having an output coupled to the control input of the radio receiver, the timer providing an output signal to the radio receiver control input changing a state of the identification device from a sleep mode requiring a first power level to a second mode by turning the radio receiver in the identification device on in response to a first criterion, the radio receiver requiring a second power level greater than the first power level; and

a wake-up controller circuit including an output coupled to the microprocessor control input, the wake-up controller circuit changing the state of the identification device from the second mode to a third mode when a second criterion is met, the third mode requiring a third power level greater than the second power level, and, when the second criterion is not met, changing the state from the second mode to the sleep mode, the wake up controller circuit providing an output signal to the microprocessor control input changing the state of the identification device from the third mode to a fourth mode when a third criterion is met, the fourth mode requiring a fourth power level greater than the third mode, and, when the third criterion is not met, changing the state from the third mode to the sleep mode.

17. The identification device as claimed in claim **16** wherein changing the state to a fourth mode when a third criterion is met includes providing a microprocessor wake-up signal when a variable frequency oscillator achieves frequency lock with a received RF signal.

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