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Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is the nonprovisional patent application

For (Title): ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

By (Inventors): Yojiro MATSUEDA; Hayato NAKANISHI

☒ Formal drawings (Figs. 1-6F; 5 sheets) are attached.
☐ Use Figure _____ for front page of Publication.
☐ A Declaration and Power of Attorney is filed herewith.
☐ This application claims benefit of Provisional Application No. _____ filed _____.
(A Preliminary Amendment is attached to reflect this claim in the Specification if not already present.)
☒ This patent application is assigned to SEIKO EPSON CORPORATION.
☐ The executed Assignment is filed herewith.
☐ An Information Disclosure Statement is filed herewith.
☐ Entitlement to small entity status is hereby asserted.
☐ A Preliminary Amendment is filed herewith.
☒ Priority of foreign application No. 2002-293696 filed October 7, 2002 in JAPAN is claimed (35 U.S.C. §119).
☐ A certified copy of the above corresponding foreign application is filed herewith.
☐ This application is NOT to be published under 35 U.S.C. 112(b). The undersigned attorney or agent hereby certifies that the invention disclosed in this application has not been and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.
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| BASIC FEE | | | | $ 385 | OR | | $ 770 |
| TOTAL CLAIMS | 12 - 20 | = 0 | x 9 = | $ | OR | x 18 | $ |
| INDEP CLAIMS | 6 - 3 | = 3 | x 43 = | $ | OR | x 86 | $ 258 |
| ☐ MULTIPLE DEPENDENT CLAIMS PRESENTED | | | + 145 = | $ | OR | + 290 | $ |
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# ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

## BACKGROUND OF THE INVENTION

1. Field of Invention

**[0001]** The present invention relates to a wiring layout suitable for an electro-optical device including electro-optical devices.

2. Description of Related Art

**[0002]** Organic EL devices are current-driven self-light-emitting devices, and accordingly, there are an advantage of no need to provide a backlight, as well as other advantages such as low power consumption, a wide range of vision, and a high contrast ratio, so there is high expectation for development of flat panel displays employing EL devices. The organic EL device is an electro-optical device including a light-emission layer introduced between an anode and a cathode, wherein, upon supplying forward bias current between both the electrodes, self-light-emission is effected due to the recombination energy at the time of recombination of a hole injected from the anode and an electron injected from the cathode. Accordingly, a supply of electric power from an external circuit is required in order to cause the organic EL device to emit light.

**[0003]** With conventional color-display active-matrix-driven display panels, an M number each of electric power lines and data lines are disposed in the column direction on a pixel matrix with an N number of columns and an M number of rows formed on a pixel region, as well as an N number of selection lines being disposed in the row direction on the aforementioned matrix. With a given pixel of such a wiring layout, a data line is disposed between the given pixel and the left-adjacent pixel, and an electric power line is disposed between the given pixel and the right-adjacent pixel. That is to say, with the lines disposed between adjacent pixels in the column direction, a layout is formed so that one data line and one electric line make up one pair. With the above-described configuration, disposed at an intersection of a scan line and a data line are: a switching transistor, a holding capacitance, a driving transistor, and an organic EL device for emitting light in one color of the RGB three primary colors, and these devices make up a pixel.

## SUMMARY OF THE INVENTION

**[0004]** With the conventional arrangements, a light-emission layer is formed of a material corresponding to each color of the RGB three primary colors, and accordingly, the organic EL device is operated with greatly different power consumption corresponding to

each color, so the optimal width of the electric power line is greatly different for each color. Accordingly, with the above-described wiring layout, while there is the need to determine the pixel pitch according to the maximal width for disposing the electric power lines, there is the need to form a pixel matrix with the same pixel pitch due to the restriction from the manufacturing process for a display, and accordingly, there is the need to determine the pixel layout at the sacrifice of the aperture ratio. On the other hand, in the event of reducing the aperture ratio, there is the need to increase the amount of electric current supplied to the organic EL device for obtaining predetermined luminance, and accordingly, there is the need to form the electric power line with a greater width, leading to further reduction of the aperture ratio from the above-described reason.

**[0005]** As described above, with the conventional wiring layout, the width of the electric line and the aperture ratio of the pixel are in the relation of trade off each other, and it is difficult to maintain a large aperture ratio while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.

**[0006]** Accordingly, it is an object of the present invention to provide a wiring method for electric power lines, wherein the aperture ratio of the pixel can be increased while maintaining a pixel matrix with the same pixel pitch.

**[0007]** In order to solve the above-described problems, an electro-optical device according to the present invention comprises multiple pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from an electric power supply circuit, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein the line forming regions are formed with generally the same width. With such a configuration, a the pixel pitch can be made the same.

**[0008]** Here, "electro-optical device" means a general electronic device for changing the optical state of light by using electric effects, and include, besides self-light-emitting devices such as electro-luminescence devices, electronic devices for displaying grayscale by adjusting the state of the polarized light, similarly to liquid crystal devices. With the present invention, the electro-luminescence devices are preferably employed. With the present invention, the electro-luminescence devices are employed, whereby current-driven self-light-emission devices can be obtained.

**[0009]** Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein at least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

**[0010]** Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein both at least one electric power line of the multiple electric power lines and at least one scan line of the multiple scan lines are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

**[0011]** Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein both at least one electric power line of the multiple electric power lines

and at least one data line of the multiple data lines are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

**[0012]** The aforementioned line forming regions are preferably formed with generally the same width. With the present invention, the line forming regions are formed with generally the same width, whereby the pixel matrix can be formed with the same pixel pitch.

**[0013]** The aforementioned electro-optical device preferably includes electro-optical devices which are operated with different driving voltages, wherein the electric power lines for supplying voltage to the electro-optical devices are formed with different widths corresponding to the driving voltage. Even with such a configuration wherein the electric power lines are formed with different widths, the wiring layout is designed as described above, whereby the pixel matrix can be formed with the same pixel pitch while improving the aperture ratio.

**[0014]** The aforementioned electro-optical device preferably is a light-emission device, wherein the electric power lines are formed with each different width corresponding to the emission light color of the light-emission device. With the present invention, the optimal width of the electric power line is determined corresponding to the properties of the electro-optical device, thereby facilitating design of devices.

**[0015]** The color of the light which is to be emitted is preferably red, green, or blue. This enables full-color display.

**[0016]** The electro-optical device preferably is an electro-luminescence device. With the electro-luminescence device, the grayscale due to light emission can be controlled by current control.

**[0017]** An electronic apparatus according to the present invention comprises an electro-optical device according to the present invention. The electronic apparatus is not particularly restricted so long as it includes a display device, and can be applied to, for example, cellular phones, video cameras, personal computers, head mount displays, projectors, facsimiles, digital cameras, portable TVs, DSP devices, PDAs, palmtops, and the like.

**[0018]** A matrix substrate according to the present invention comprises multiple pixel electrodes disposed in the form of a matrix, wherein the multiple pixel electrodes make

up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups, and wherein the line forming regions are formed with generally the same width. With such a configuration, the pixel pitch can be made the same.

**[0019]** Another matrix substrate according to the present invention comprises multiple scan lines, multiple data lines, multiple pixel electrodes disposed at portions corresponding to the intersections of the scan lines and the data lines, and multiple electric power lines for supplying voltage to the multiple pixel electrodes, wherein the multiple pixel electrodes make up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups, and wherein at least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, the pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio, while forming the electric power lines with the optimal width.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** Fig. 1 is a plan view of an organic EL display panel according to the present invention.

**[0021]** Fig. 2 is a principal circuit configuration diagram of a pixel.

**[0022]** Fig. 3 is an explanatory diagram for describing a wiring layout according to a first embodiment.

**[0023]** Fig. 4 is an explanatory diagram for describing a wiring layout according to a second embodiment.

**[0024]** Fig. 5 is an explanatory diagram for describing a wiring layout according to a third embodiment.

**[0025]** Fig. 6(a) through Fig. 6(f) are explanatory diagrams for describing application examples employing the organic EL display according to the present invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

**[0026]** The present embodiment will now be described with reference to the drawings.

**[0027]** Fig. 1 is an overall configuration diagram which illustrates an active-matrix organic-EL display panel 100 according to the present embodiment. As shown in the drawing, the display panel 100 comprises a display region 11 including multiple pixels 10 disposed in the form of a matrix with an N number of columns and an M number of rows, a scan line driver 12 for outputting scan signals to scan lines arrayed in the row direction which are connected to a group of pixels 10, a data line driver 13 for supplying data signals and electric power to data lines and electric power lines arrayed in the column direction which are connected to a group of pixels 10, wherein these components are disposed on a substrate 16. An organic EL device is formed on each pixel 10 for emitting light in a color of the RGB three primary colors. A cathode 14 is formed in the form of a film as a common electrode on the entire face of the display region 11, and is connected to an external circuit through cathode output electrode 15.

**[0028]** Note that while the organic EL display panel 100 shown in the drawing is a so-called "top-emission configuration display panel" which emits light from the side of the substrate 16, the present invention is not restricted to this arrangement, but rather, the present invention can also be applied to a bottom-emission configuration display panel which emits light from a transparent cathode.

**[0029]** Fig. 2 is a principal circuit configuration diagram of the pixel 10. The pixel 10 comprises a switching transistor Tr1, a driving transistor Tr2, holding capacitance C, a light-emission portion OLED, and is driven with the dual transistor method. The switching transistor Tr1 comprises an n-channel FET, wherein the gate terminal thereof is connected to the scan line $V_{sel}$, and the drain terminal thereof is connected to the data line $I_{dat}$. The driving transistor Tr2 comprises a p-channel FET, wherein the gate terminal is connected to the source terminal of the switching transistor Tr1. Furthermore, the source terminal of the transistor Tr2 is connected to the electric power line $V_{dd}$, and the drain terminal thereof is connected to the light-emission portion OLED. Furthermore, holding capacitance is formed between the gate and the source of the transistor Tr2. With the above-described configuration, upon outputting a selection signal to the scan line $V_{sel}$, and opening the transistor Tr1, the data signals supplied through the data line $I_{dat}$ are written to the holding capacitance C as a voltage value. Subsequently, the holding voltage written to the holding capacitance C is held during one frame period, and the conductance of the driving transistor Tr2 is determined according to the holding voltage in an analog manner, whereby forward

bias current corresponding to light-emission level is supplied to the light-emission portion OLED.

**[0030]** Fig. 3 is a diagram for describing a wiring layout in the pixel region. In the drawing, in order to simplify description, a wiring layout for six pixels disposed with the two rows and the three columns is shown. In the drawing, reference characters R, G, and B denote the pixels 10 for emitting light in red, green, and blue, respectively, and the RGB pixels are disposed in the column direction. Furthermore, reference character $V_{dd\text{-}R}$ denotes an electric line for a red pixel, $V_{dd\text{-}G}$ denotes an electric line for a green pixel, $V_{dd\text{-}B}$ denotes an electric line for a blue pixel, and 17 denotes a pixel electrode (anode) of an organic EL device. Detailed description regarding other components described above will be omitted. Furthermore, reference numeral 31 denotes a line forming region in the form of a line which is formed between a pixel group of the (m-1) column and a pixel group of the m column, and is extending in the column direction over generally the same length as the pixel array length in the column direction. In the same way, reference numeral 32 denotes a line forming region formed between pixel groups of the m column and the (m + 1) column, 33 denotes a line forming region formed between pixel groups of the (m + 1) column and (m + 2) column, and 34 denotes a line forming region formed between pixel groups of the (m + 2) column and the (m + 3) column. For convenience of description, a pixel group of the (m - 1) column and a pixel group of the (m + 3) column are not shown in the drawing. With the present embodiment, in order to determine the line forming regions 31 through 34 with the width as same as possible, two or more lines, disposed on the aforementioned line forming regions, are determined with the same total width. While the electric power line $V_{dd}$ is formed with a width corresponding to a material of the emission layer of the organic EL device, now, for convenience of description, let us make an assumption that the width of the electric power lines increases in the order of green, red, and blue. That is to say, let us assume that the relation: width of $V_{dd\text{-}G}$ > width of $V_{dd\text{-}R}$ > width of $V_{dd\text{-}B}$, holds.

**[0031]** With the above-described assumption, in order to form the line forming regions 31 through 34 with the width as same as possible, a combination is determined such that the total width of the electric power line $V_{dd}$ and the data line $I_{dd}$ is approximately the same. For example, making an assumption that: the total width of $V_{dd\text{-}G}$ which has the maximal width and $V_{dd\text{-}B}$ of the minimal width; the total width of $V_{dd\text{-}R}$ of an intermediate width and the data line $I_{dat}$ of an intermediate width; and the total width of the two data lines $I_{dat}$; are determined to be generally the same value, the combinations of these electric power lines $V_{dd}$ and the data line $I_{dat}$ are formed in the line forming regions 31 through 34. With the

arrangement shown in the drawing, a combination of $V_{dd\text{-}G}$ with the maximal width and $V_{dd\text{-}B}$ with the minimal width is formed on the line forming region 33, a combination of $V_{dd\text{-}R}$ with the intermediate width and the data line $I_{dat}$ with the intermediate width is formed in the line forming regions 31 and 34, and a combination of the two data lines $I_{dat}$ is formed on the line forming region 32. Note that with the line forming region 31, only the electric power line $V_{dd\text{-}R}$ is shown in the drawing, and with the line forming region 34, only the data line $I_{dat}$ is shown in the drawing. On the other hand, a scan line $V_{sel}$ is disposed on each line forming region in the form of a line, between pixel groups arrayed in the row direction, with generally the same length as the pixel array length of the pixel group. The wiring layout shown in the drawing corresponds to one unit of a periodically repeating wiring pattern, and any portion of the wiring layout of the RGB pixels 10 randomly selected has the same pattern as shown in the drawing. Accordingly, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other.

**[0032]** With the present embodiment, the same kind of electric power line, extending in the column direction of the pixel matrix, is formed with generally the same array pitch in the row direction, and accordingly, the pixels can be formed with the same pixel pitch, thereby facilitating design of a layout for a device, wherein power consumption is different for each color, such as an organic EL display. In particular, in the event of forming light-emission layers using the ink-jet method, the pixels are preferably formed with the same pixel pitch, and accordingly, an arrangement according to the present embodiment has the great advantage of facilitating the manufacturing process. Furthermore, with the present embodiment, the electric power line can be formed with a width suitable for each color, thereby reducing power consumption while maintaining the high aperture ratio and the optimal color balance.

**[0033]** Note that the above-described arrangement is only an example of the present invention, and the present invention is not restricted to the above-described arrangement. For example, three combinations of two electric power lines selected from the three RGB lines $V_{dd}$ can be made, and accordingly, with the present embodiment, three wiring layout patterns can be made. Furthermore, while description has been made regarding a configuration wherein a scan line $V_{sel}$ is disposed on each line forming region in the row direction, and any two lines selected from the three electric power lines $V_{dd}$ and the three data line $I_{dat}$ are disposed on the line forming regions 31, 32, and 33 in the column direction, the present

invention is not restricted to this arrangement. Description will be made below regarding various modifications.

Second Embodiment

**[0034]** Fig. 4 is an explanatory diagram for describing a wiring layout according to a second embodiment of the present invention.

**[0035]** The present embodiment has a configuration wherein, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ make up a combination, and are disposed in the row direction on a line forming region 41 between the pixel group of the (n - 1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines $V_{sel}$ make up a combination, and are disposed in the row direction in a line forming region 42 between the pixel groups of the n row and the (n + 1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration wherein the combination of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the combination of the two scan lines $V_{sel}$ are disposed periodically and repeatedly. Accordingly, a line forming region 43 between the pixel groups of the (n + 1) row and the (n + 2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 41.

**[0036]** On the other hand, one electric power line $V_{dd}$ and one data line $I_{dat}$ make up a combination, and are disposed in the column direction and are disposed on a line forming region between pixel groups arranged in the column direction. With an arrangement shown in the drawing, the electric power line $V_{dd\text{-}R}$ and the data line $I_{dat}$ make up a combination, and are disposed on a line forming region 51 between the R-pixel group of the m column and the G-pixel group of the (m + 1) column, which are arrayed in the column direction. In the same way, the electric power line $V_{dd\text{-}G}$ and the data line $I_{dat}$ make up a combination, and are disposed on a line forming region between the G-pixel group of the (m + 1) column and the B-pixel group (not shown) of the (m + 2) column, which are arrayed in the column direction, wherein only the electric power line $V_{dd\text{-}G}$ is shown in the drawing for convenience of description. Furthermore, the electric power lines $V_{dd\text{-}R}$ disposed in the row and column directions are formed in different layers, and are electrically connected with each other

through contact holes h1 formed in an inter-layer insulating film. The electric power lines $V_{dd\text{-}G}$ are electrically connected with each other through contact holes h2 in the same way.

**[0037]** With the present embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same array pitch, and accordingly, the present embodiment has the same advantages as with the first embodiment, and furthermore, the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, cross-talk can be reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present embodiment is particularly advantageous.

Third Embodiment

**[0038]** Fig. 5 is an explanatory diagram for describing a wiring layout according to a third embodiment of the present invention.

**[0039]** The present embodiment has a configuration wherein, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction and the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ make up a combination, and are disposed in the row direction on a line forming region 61 between the pixel group (not shown) of the (n - 1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines $V_{sel}$ make up a combination, and are disposed in the row direction in a line forming region 62 between the pixel groups of the n row and the (n + 1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration wherein the combination of the three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the combination of the two scan lines $V_{sel}$ are disposed periodically and repeatedly. Accordingly, a line forming region 63 between the pixel groups of the (n + 1) row and the (n + 2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 61.

**[0040]** On the other hand, three combinations of two lines selected from the three electric power lines $V_{dd\text{-}C}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the three data lines $I_{dat}$ are formed between

the pixel groups arrayed in the column direction. With an arrangement shown in the drawing, the electric power line (not shown) and the data line $I_{dat}$ make up a combination, and are disposed in a line forming region 71 between the B-pixel group (not shown) of the (m - 1) column and the R-pixel group of the m column, which are arrayed in the column direction, and the two electric power lines $V_{dd\text{-}G}$ and $V_{dd\text{-}R}$ make up a combination, and are disposed on a line forming region 72 between the R-pixel group of the m column and the G-pixel group of the (m + 1) column, which are arrayed in the column direction. Furthermore, the two data lines $I_{dat}$ make up a combination, and are disposed on a line forming region 73 between the G-pixel group of the (m + 1) column and the B-pixel group of (m + 2) column, which are arrayed in the column direction, and the electric power line $V_{dd\text{-}G}$ and the data line $I_{dat}$ make up a combination, and are formed on a line forming region 74 between the B-pixel group of the (m + 2) column and the R-pixel group (not shown) of the (m + 3) column, which are arrayed in the column direction.

**[0041]** The electric power lines disposed in the column and row directions are formed in different layers, and are electrically connected with each other through the contact holes h1 formed on an inter-layer insulating film. In the same way, the electric power lines $V_{dd\text{-}G}$ in the column and row directions, and the electric power lines $V_{dd\text{-}B}$ in the column and row directions, are formed in different layers, and the electric power lines in the column and row directions are electrically connected with each other through the contact holes h2 and h3. With the present embodiment, a plurality of each of the contact holes h1, h2, and h3 are formed, whereby the present embodiment has the advantage of preventing wiring breakage, and furthermore has the advantage of reducing the wiring resistance.

**[0042]** With the present embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same array pitch, the same kind of electric power line extending in the column direction of the pixel matrix is formed in the row direction with generally the same array pitch, and accordingly, the present embodiment has the same advantages as with the first embodiment, and furthermore, the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, the occurrence of cross-talk can be

reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present embodiment is particularly advantageous.

Fourth Embodiment

**[0043]** Fig. 6(a) through Fig. 6(f) are diagrams which illustrate examples of electronic apparatuses to which the electric-optical device according to the present invention can be applied. Fig. 6(a) shows an example of application to a cellular phone, wherein the cellular phone 230 comprises an antenna unit 231, an audio output unit 232, an audio input unit 233, an operating unit 234, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 according to the present invention can be employed as a display unit of the cellular phone 230. Fig. 6(b) shows an application example to a video camera, wherein the video camera 240 comprises a TV-camera unit 241, an operating unit 242, an audio input unit 243, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a viewfinder or a display unit. Fig. 6(c) shows an application example to a portable personal computer, wherein the computer 250 comprises a camera unit 251, an operation unit 252, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a display device.

**[0044]** Fig. 6(d) shows an application example to a head mount display, wherein the head mount display 260 comprises a belt 261, an optical system storage unit 262, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as an image display unit. Fig. 6(e) shows an application example to a rear projector, wherein the projector 270 comprises a casing 271, a light source 272, a synthesizing optical system 273, mirrors 274 and 275, a screen 276, and the organic EL display panel 100 according to the present invention. Fig. 6(f) shows an application example to a front projector, wherein the projector 280 comprises a casing 282, an optical system 281, and the organic EL display panel 100 according to the present invention, wherein an image can be displayed on a screen 283. As described above, the organic EL display panel 100 can be employed as an image display unit.

WHAT IS CLAIMED IS:

1. An electro-optical device comprising a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from an electric power supply circuit;

wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction;

and wherein line forming regions are formed between adjacent pixel groups of said plurality of pixel groups;

and wherein said line forming regions are formed with generally the same width.

2. An electro-optical device comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of said scan lines and said data lines, including electro-optical devices; and

a plurality of electric power lines for supplying driving voltage to said electro-optical devices;

wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction;

and wherein a plurality of line forming regions are formed between adjacent pixel groups of said plurality of pixel groups;

and wherein at least two lines selected from at least one electric power line of said plurality of electric power lines, at least one scan line of said plurality of scan lines, and at least one data line of said plurality of data lines, are formed in at least one line forming region of said plurality of line forming regions.

3. An electro-optical device comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of said scan lines and said data lines, including electro-optical devices; and

a plurality of electric power lines for supplying driving voltage to said electro-optical devices;

wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction;

and wherein a plurality of line forming regions are formed between adjacent pixel groups of said plurality of pixel groups;

and wherein both at least one electric power line of said plurality of electric power lines and at least one scan line of said plurality of scan lines are formed in at least one line forming region of said plurality of line forming regions.

4. An electro-optical device comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of said scan lines and said data lines, including electro-optical devices; and

a plurality of electric power lines for supplying driving voltage to said electro-optical devices;

wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction;

and wherein a plurality of line forming regions are formed between adjacent pixel groups of said plurality of pixel groups;

and wherein both at least one electric power line of said plurality of electric power lines and at least one data line of said plurality of data lines are formed in at least one line forming region of said plurality of line forming regions.

5. An electro-optical device according to Claim 2, wherein said line forming regions are formed with generally the same width.

6. An electro-optical device according to Claim 1, wherein said electro-optical devices are operated with each different driving voltages;

and wherein said electric power lines for supplying voltage to said electro-optical devices are formed with different widths corresponding to said driving voltage.

7. An electro-optical device according to Claim 6, wherein said electro-optical device is a light-emission device;

and wherein said electric power lines are formed with different widths corresponding to the emission light color of said light-emission device.

8. An electro-optical device according to Claim 7, wherein said color of the light which is to be emitted is red, green, or blue.

9. An electro-optical device according to Claim 1, wherein said electro-optical device is an electro-luminescence device.

10. An electronic apparatus comprising an electro-optical device according to Claim 1.

11. A matrix substrate comprising a plurality of pixel electrodes disposed in the form of a matrix;

wherein said plurality of pixel electrodes make up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction;

and wherein a plurality of line forming regions are formed between adjacent pixel electrode groups of said plurality of pixel electrode groups;

and wherein said line forming regions are formed with generally the same width.

12. A matrix substrate comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel electrodes disposed at portions corresponding to intersections of said scan lines and said data lines; and

a plurality of electric power lines for supplying voltage to said plurality of pixel electrodes;

wherein said plurality of pixel electrodes make up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction;

and wherein a plurality of line forming regions are formed between adjacent pixel electrode groups of said plurality of pixel electrode groups;

and wherein at least two lines selected from at least one electric power line of said plurality of electric power lines, at least one scan line of said plurality of scan lines, and at least one data line of said plurality of data lines, are formed in at least one line forming region of said plurality of line forming regions.

## ABSTRACT OF THE DISCLOSURE

To provide a wiring layout of electric power lines, which improves the aperture ratio of the pixel while forming pixels with the same pixel pitch. An electric-optical apparatus according to the present invention comprises multiple pixels (10) arranged in matrix including electro-optical devices driven by receiving electric power from an electric power supply circuit, wherein the aforementioned multiple pixels (10) make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and any of line forming regions (31, 32, 33, 34) is disposed between adjacent pixel groups of the aforementioned pixel groups, wherein the aforementioned line forming regions (31, 32, 33, 34) are formed with generally the same width.

Fig. 1

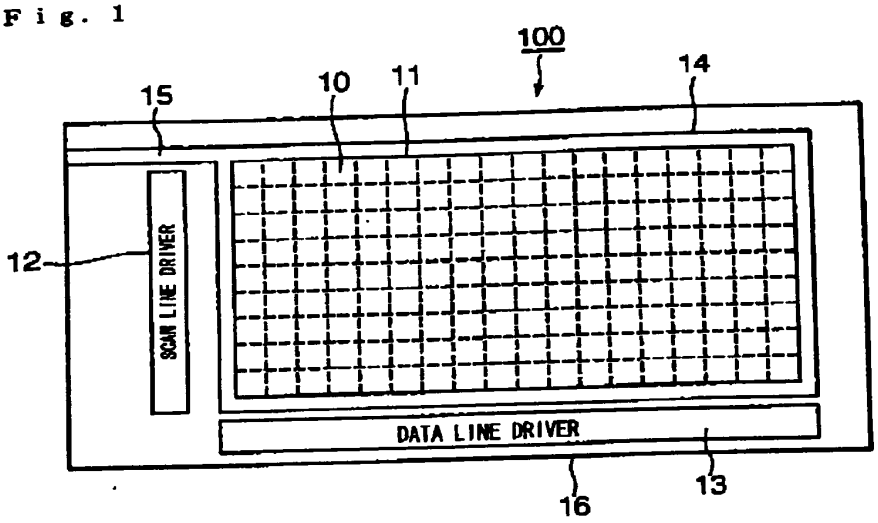

100
15
10
11
14
12
SCAN LINE DRIVER
DATA LINE DRIVER
16
13

Fig. 2

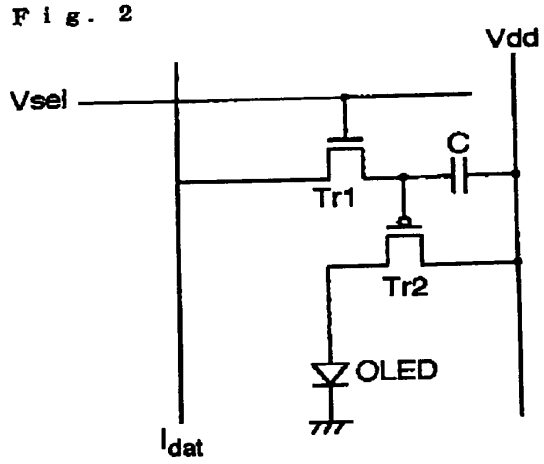

Vdd
Vsel
C
Tr1
Tr2
OLED
Idat

Fig. 3

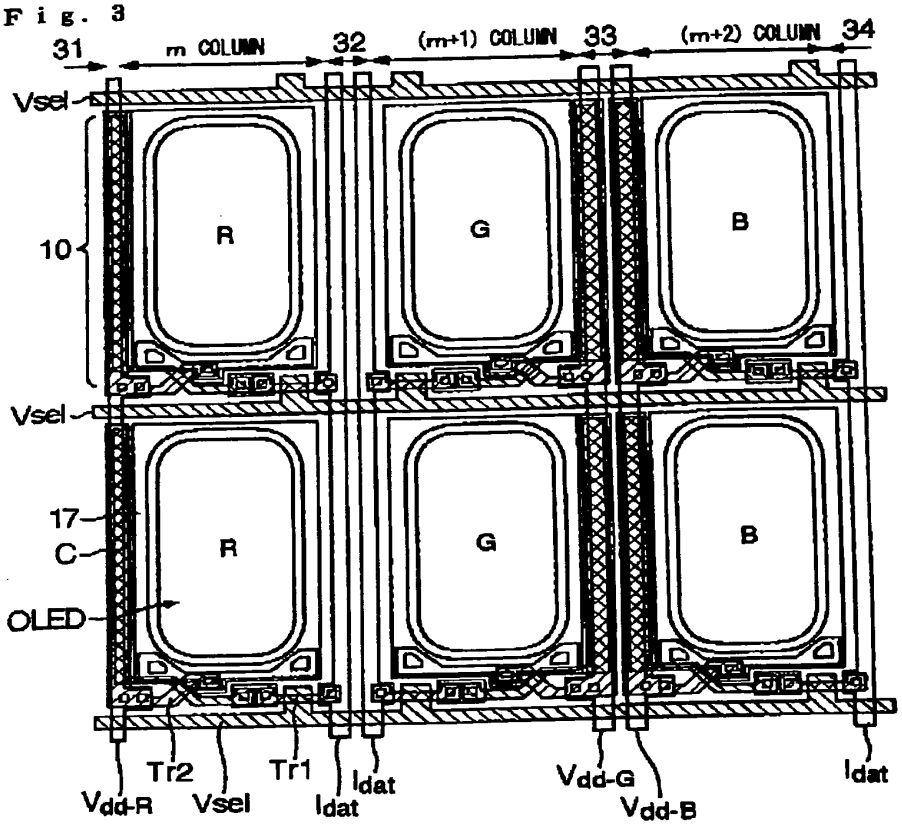

31
m COLUMN
32
(m+1) COLUMN
33
(m+2) COLUMN
34
Vsel
10
R
G
B
Vsel
17
C
OLED
R
G
B
Vdd-R
Tr2
Vsel
Tr1
Idat
Idat
Vdd-G
Vdd-B
Idat

Fig. 4

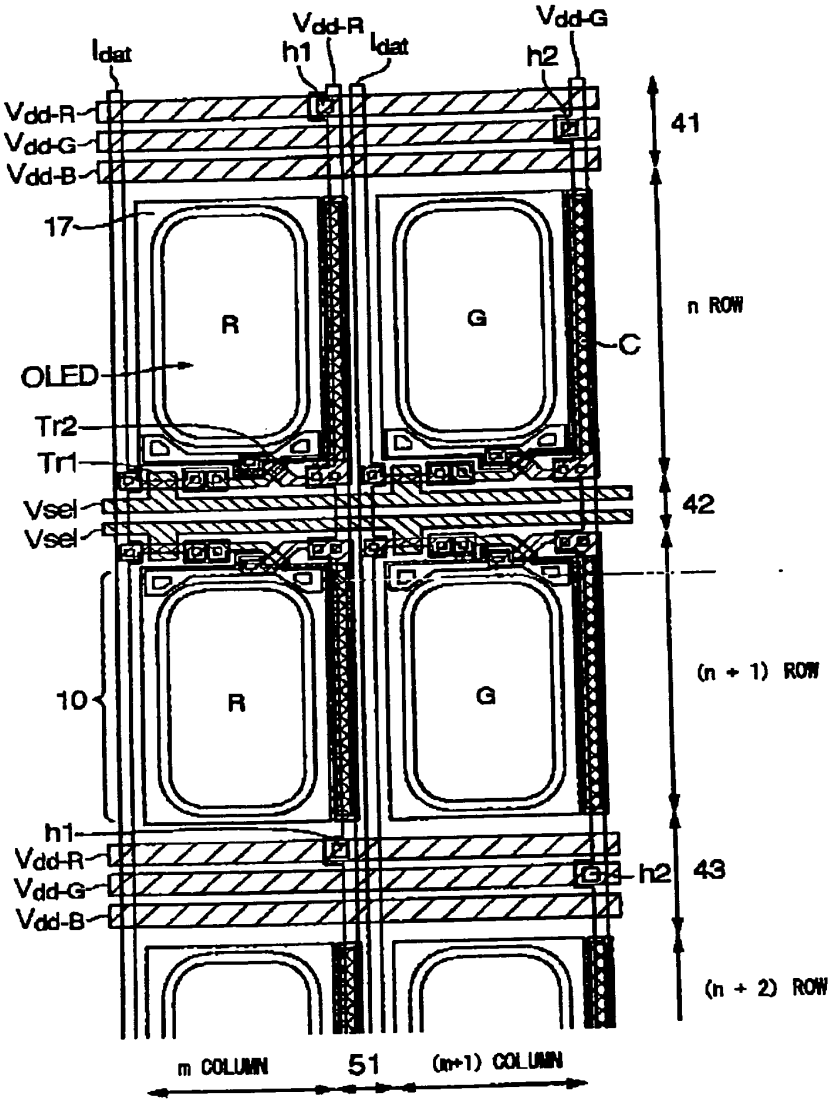
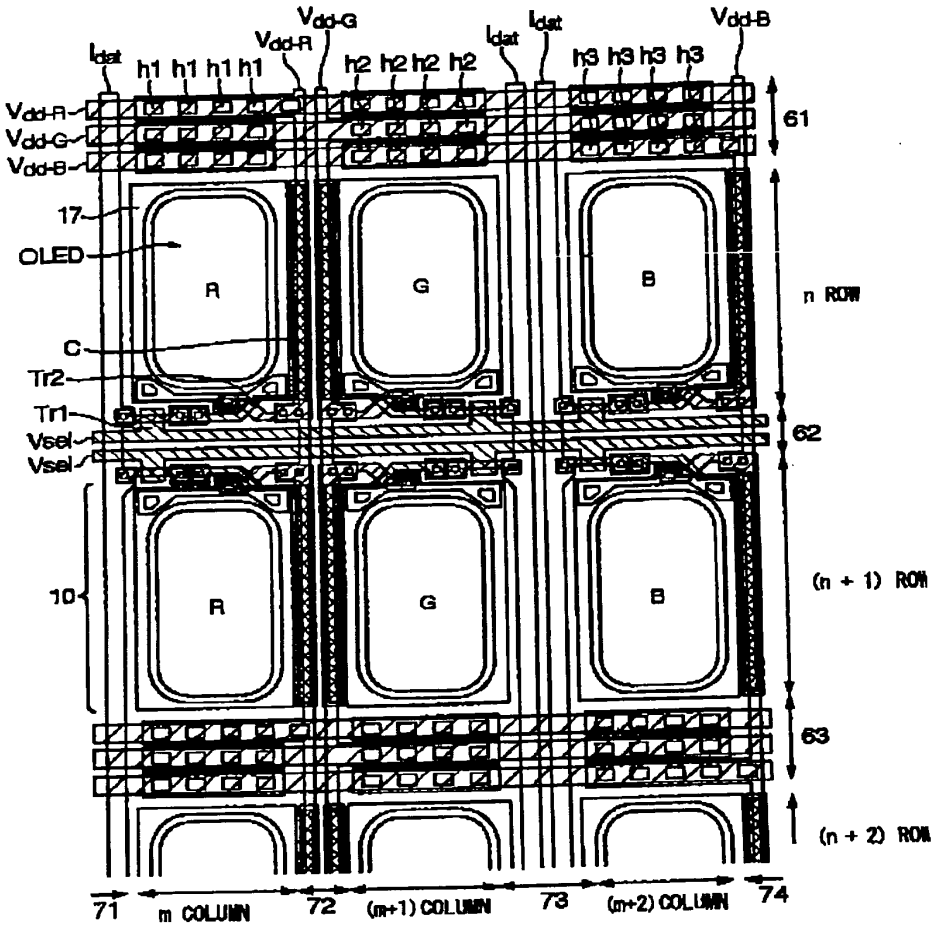

Idat
Vdd-R
h1
Idat
Vdd-G
h2
Vdd-R
Vdd-G
Vdd-B
17
R
G
C
OLED
Tr2
Tr1
Vsel
Vsel
10
R
G
h1
Vdd-R
Vdd-G
Vdd-B
h2
41
n ROW
42
(n + 1) ROW
43
(n + 2) ROW
m COLUMN
51
(n+1) COLUMN

Fig. 5


Idat
h1 h1 h1 h1
Vdd-R
Vdd-G
h2 h2 h2 h2
Idat
Idat
h3 h3 h3 h3
Vdd-B
Vdd-R
Vdd-G
Vdd-B
61
17
OLED
R
G
B
n ROW
C
Tr2
Tr1
Vsel
Vsel
62
10
R
G
B
(n + 1) ROW
63
(n + 2) ROW
71
m COLUMN
72
(m+1) COLUMN
73
(m+2) COLUMN
74

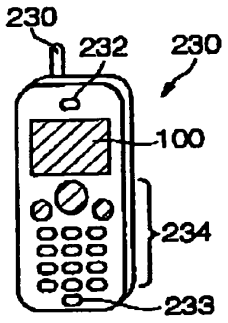



Fig. 6A

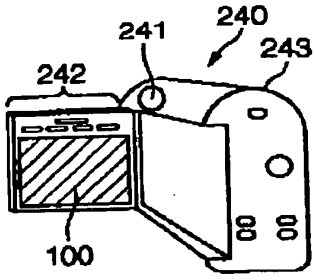



Fig. 6B

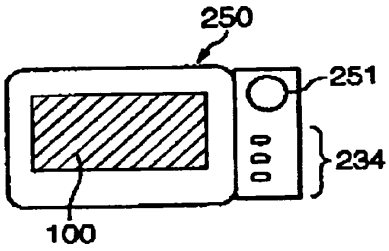



Fig. 6C

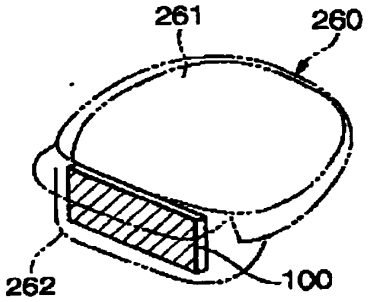



Fig. 6D

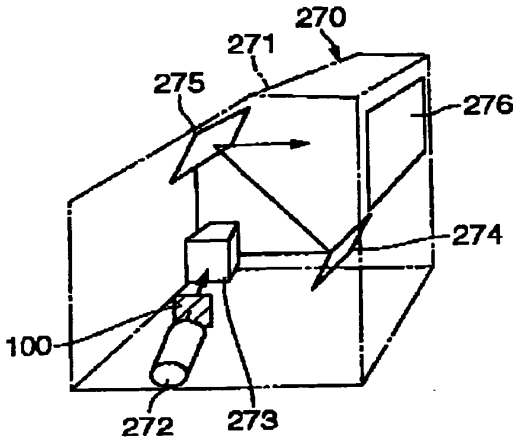



Fig. 6E

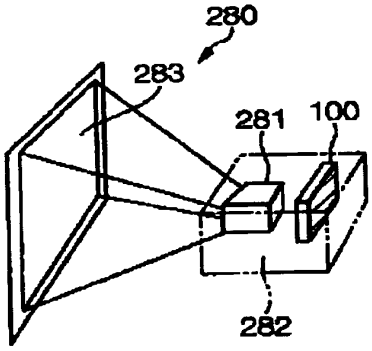



Fig. 6F

## Application Data Sheet

### Application Information

| | |
|---|---|
| Application Type:: | Regular |
| Subject Matter:: | Utility |
| CD-ROM or CD-R: | None |
| Title:: | ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS |
| Attorney Docket Number:: | 117390 |
| Suggested Drawing Figure:: | |
| Total Drawing Sheets:: | 5 |
| Small Entity:: | No |

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| Country of Residence:: | JAPAN |

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| Country of Residence:: | JAPAN |

**Correspondence Information**

Correspondence Customer Number:: 25944

| **Foreign Priority Information** | | | |
|---|---|---|---|
| | | | |
| Country:: | Application Number:: | Filing Date:: | Priority Claimed:: |
| | | | |
| JAPAN | 2002-293696 | 10/7/2002 | Yes |
| | | | |

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| Country of mailing address:: | JAPAN |
| Postal or Zip Code of mailing address:: | 163-0811 |
| | |

## PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 117390

### CLAIMS AS FILED - PART I

| | (Column 1) | (Column 2) |
|---|---|---|
| TOTAL CLAIMS | 12 | |
| FOR | NUMBER FILED | NUMBER EXTRA |
| TOTAL CHARGEABLE CLAIMS | 12 minus 20= | * 0 |
| INDEPENDENT CLAIMS | 6 minus 3 = | * 3 |
| MULTIPLE DEPENDENT CLAIM PRESENT | | ☐ |

* If the difference in column 1 is less than zero, enter "0" in column 2

| SMALL ENTITY TYPE ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|
| RATE | FEE | | RATE | FEE |
| BASIC FEE | 385.00 | OR | BASIC FEE | 770.00 |
| X$ 9= | | OR | X$18= | 0 |
| X43= | | OR | X86= | 258 |
| +145= | | OR | +290= | 0 |
| TOTAL | | OR | TOTAL | 1028 |

### CLAIMS AS AMENDED - PART II

**AMENDMENT A**

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|
| Total | * | Minus | ** | = |
| Independent | * | Minus | *** | = |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | ☐ |

| SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|
| RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
| X$ 9= | | OR | X$18= | |
| X43= | | OR | X86= | |
| +145= | | OR | +290= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

**AMENDMENT B**

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|
| Total | * | Minus | ** | = |
| Independent | * | Minus | *** | = |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | ☐ |

| RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
|---|---|---|---|---|
| X$ 9= | | OR | X$18= | |
| X43= | | OR | X86= | |
| +145= | | OR | +290= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

**AMENDMENT C**

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|
| Total | * | Minus | ** | = |
| Independent | * | Minus | *** | = |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | ☐ |

| RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
|---|---|---|---|---|
| X$ 9= | | OR | X$18= | |
| X43= | | OR | X86= | |
| +145= | | OR | +290= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

OIPE
OCT 2 3 2003
PATENT & TRADEMARK OFFICE

[redacted]

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al.

Application No.: 10/676,067

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

**CLAIM FOR PRIORITY**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The benefit of the filing date of the following prior foreign application filed in the following foreign country is hereby requested for the above-identified patent application and the priority provided in 35 U.S.C. §119 is hereby claimed:

Japanese Patent Application No. 2002-293696, filed October 7, 2002.

In support of this claim, a certified copy of said original foreign application:

__X__ is filed herewith.

_____ was filed on _____ in Parent Application No. _____ filed _____.

_____ will be filed at a later date.

It is requested that the file of this application be marked to indicate that the requirements of 35 U.S.C. §119 have been fulfilled and that the Patent and Trademark Office kindly acknowledge receipt of this document.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
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JAO:EDM/gam

Date: October 23, 2003

**OLIFF & BERRIDGE, PLC**
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**Alexandria, Virginia 22320**
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# 日本国特許庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。
This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日
Date of Application: ２００２年１０月　７日

出願番号
Application Number: 特願２００２－２９３６９６
[ST. 10/C]: [ＪＰ２００２－２９３６９６]

出願人
Applicant(s): セイコーエプソン株式会社

２００３年　９月１１日

特許庁長官
Commissioner,
Japan Patent Office 今井康夫

出証番号　出証特２００３－３０７４６５６

【書類名】　特許願
【整理番号】　J0091837
【あて先】　特許庁長官殿
【国際特許分類】　H05B 33/04
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【選任した代理人】
【識別番号】　100093861
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出証特２００３－３０７４６５６

【手数料の表示】

【予納台帳番号】　011903

【納付金額】　21,000円

【提出物件の目録】

【物件名】　明細書　1

【物件名】　図面　1

【物件名】　要約書　1

【包括委任状番号】　9808570

【プルーフの要否】　要

【書類名】　明細書

【発明の名称】　電気光学装置、マトリクス基板、及び電子機器

【特許請求の範囲】

【請求項１】　電源回路から電源供給を受けて駆動される電気光学素子を含む、マトリクス状に配置された複数の画素を備えた電気光学装置であって、

前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる複数の画素群を構成しており、

前記複数の画素群の各々の画素群の間に配線形成領域が設けられ、

前記配線形成領域の幅は略等しい、

ことを特徴とする、電気光学装置。

【請求項２】　複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された各々に電気光学素子を備えた複数の画素と、を含む電気光学装置であって、

前記電気光学素子に駆動電圧を供給する複数の電源線を含み、

前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素群を構成し、

前記複数の画素群の各々の画素群の間に複数の配線形成領域が設けられ、

前記複数の配線形成領域のうち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線、前記複数の走査線のうち少なくとも一つの走査線、及び前記複数のデータ線のうち少なくとも一つのデータ線から選ばれた少なくとも二つの配線が形成されている、

ことを特徴とする、電気光学装置。

【請求項３】　複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された各々に電気光学素子を備えた複数の画素と、を含む電気光学装置であって、

前記電気光学素子に駆動電圧を供給する複数の電源線を含み、

前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素群を構成し、

前記複数の画素群の各々の画素群の間に複数の配線形成領域が設けられ、

前記複数の配線形成領域のうち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線と、前記複数の走査線のうち少なくとも一つの走査線がともに形成されている、

ことを特徴とする、電気光学装置。

【請求項４】　複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された各々に電気光学素子を備えた複数の画素と、を含む電気光学装置であって、

前記電気光学素子に駆動電圧を供給する複数の電源線を含み、

前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素群を構成し、

前記複数の画素群の各々の画素群の間に複数の配線形成領域が設けられ、

前記複数の配線形成領域のうち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線と、前記複数のデータ線のうち少なくとも一つのデータ線がともに形成されている、

ことを特徴とする、電気光学装置。

【請求項５】　請求項２乃至請求項４のうち何れか１項に記載の電気光学装置であって、前記配線形成領域の幅は略等しいことを特徴とする電気光学装置。

【請求項６】　前記電気光学素子には、駆動電圧が異なる電気光学素子を含み、前記駆動電圧に応じて前記電気光学素子へ電圧を供給する電源線の幅が異なることを特徴とする請求項１乃至請求項５のうち何れか１項に記載の電気光学装置。

【請求項７】　前記電気光学素子は発光素子であり、前記電源線は前記発光素子の発光色に対応して幅が異なることを特徴とする請求項６に記載の電気光学装置。

【請求項８】　前記発光色は、赤、緑、又は青であることを特徴とする請求項７に記載の電気光学装置。

【請求項９】　前記電気光学素子はエレクトロルミネセンス素子であることを特徴とする請求項１乃至請求項８のうち何れか１項に記載の電気光学装置。

【請求項１０】　請求項１乃至請求項９のうち何れか１項に記載の電気光学

装置を備える電子機器。

【請求項１１】　マトリクス状に配置された複数の画素電極を備えたマトリクス基板であって、

前記複数の画素電極は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素電極からなる複数の画素電極群を構成しており、

前記複数の画素電極群の各々の画素電極群の間に配線形成領域が設けられ、

前記配線形成領域の幅は略等しい、

ことを特徴とする、マトリクス基板。

【請求項１２】　複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された複数の画素電極と、を含むマトリクス基板であって、

前記複数の画素電極に電圧を供給するための複数の電源線を含み、

前記複数の画素電極は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素電極群を構成し、

前記複数の画素電極群の各々の画素電極群の間に複数の配線形成領域が設けられ、

前記複数の配線形成領域のうち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線、前記複数の走査線のうち少なくとも一つの走査線、及び前記複数のデータ線のうち少なくとも一つのデータ線から選ばれた少なくとも二つの配線が形成されている、

ことを特徴とする、マトリクス基板。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】

本発明は電気光学素子を備えた電気光学装に好適な配線レイアウトに関する。

【０００２】

【従来の技術】

有機ＥＬ素子は電流駆動型の自発光素子であるため、バックライトが不要となる上に、低消費電力、高視野角、高コントラスト比が得られるメリットがあり、

フラットパネルディスプレイの開発において期待されている。有機ＥＬ素子は陽極と陰極との間に介在する発光層を備えた電気光学素子であり、両電極間に順バイアス電流を供給することで、陽極から注入された正孔と陰極から注入された電子とが再結合する際の再結合エネルギーにより自発光する。このため、有機ＥＬ素子を発光させるためには、外部回路からの電源供給が必要となる。

【０００３】

従来のカラー表示用のアクティブマトリクス駆動型ディスプレイパネルにおいては、例えば、画素領域内にＮ行Ｍ列のマトリクス状に配された画素マトリクスの列方向に各々Ｍ本の電源線とデータ線を敷設する一方で、同マトリクスの行方向にＮ本の選択線を敷設している。このような配線レイアウトでは、ある特定の画素に着目したとき、例えば、当該特定の画素に対して左に隣接する画素との間にデータ線を敷設する一方、右に隣接する画素との間に電源線を敷設している。つまり、相互に隣接する画素間に敷設されている列方向のラインに着目すると、当該ラインには１本のデータ線と１本の電源線が１組となってレイアウトされている。上記の構成において、走査線とデータ線の交差点には、スイッチングトランジスタと、保持容量と、駆動トランジスタと、ＲＧＢ三原色で発光する有機ＥＬ素子とが配され、これらの素子により画素を構成している。

【０００４】

【発明が解決しようとする課題】

しかし、ＲＧＢ三原色の各色毎に発光層の材料が異なるため、各色の有機ＥＬ素子における消費電力も大きく異なり、結果として、電源線の最適な幅も色毎に大きく異なることとなる。上記の配線レイアウトで電源線を敷設すると、最大幅にあわせて画素ピッチを選定しなければならないところ、ディスプレイの製造プロセス上、画素ピッチを等間隔に設定する要請があるため、開口率を犠牲にして画素レイアウトを決定しなければならない。その一方で、開口率を小さくすると、所定の輝度を得るために有機ＥＬ素子に供給される電流量を大きくする必要があり、その結果、電源線の幅をさらに広くしなければならず、上記の理由によりさらに開口率を小さくする必要がある。

【０００５】

このように、従来の配線レイアウトでは電源線の幅と画素の開口率はトレードオフの関係にあり、画素ピッチを等間隔にするという条件下で、各色に好適な電源線の幅を確保しつつ、開口率を大きく確保することは困難であった。

【０００６】

そこで、本発明は画素の配列ピッチを等間隔に設定しつつ、画素の開口率を高めることができる電源線の配線技術を提案することを課題とする。

【０００７】

【課題を解決するための手段】

上記の課題を解決するため、本発明の電気光学装置は、電源回路から電源供給を受けて駆動される電気光学素子を含む、マトリクス状に配置された複数の画素を備えた電気光学装置であって、前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる複数の画素群を構成しており、前記複数の画素群の各々の画素群の間に配線形成領域が設けられ、前記配線形成領域の幅は略等しい、ことを特徴とする。かかる構成により、画素ピッチを等間隔に設定できる。

【０００８】

ここで、「電気光学素子」とは、電気的作用により光の光学的状態を変化させる電子素子一般をいい、エレクトロルミネセンス素子などの自発光素子の他に、液晶素子のように光の偏向状態を変化させることで階調表示する電子素子を含む。本発明ではエレクトロルミネセンス素子が好適である。エレクトロルミネセンス素子を用いることで、電流駆動により自発光する電流駆動型発光素子を得ることができる。

【０００９】

本発明の電気光学装置は、複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された各々に電気光学素子を備えた複数の画素と、を含む電気光学装置であって、前記電気光学素子に駆動電圧を供給する複数の電源線を含み、前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素群を構成し、前記複数の画素群の各々の画素群の間に複数の配線形成領域が設けられ、前記複数の配線形成領域のう

ち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線、前記複数の走査線のうち少なくとも一つの走査線、及び前記複数のデータ線のうち少なくとも一つのデータ線から選ばれた少なくとも二つの配線が形成されている、ことを特徴とする。かかる構成により、画素ピッチを等間隔に設定することができる上に、最適な電源幅を選択しつつ、画素の高開口率を得ることができる。

【００１０】

本発明の電気光学装置は、複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された各々に電気光学素子を備えた複数の画素と、を含む電気光学装置であって、前記電気光学素子に駆動電圧を供給する複数の電源線を含み、前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素群を構成し、前記複数の画素群の各々の画素群の間に複数の配線形成領域が設けられ、前記複数の配線形成領域のうち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線と、前記複数の走査線のうち少なくとも一つの走査線がともに形成されている、ことを特徴とする。かかる構成により、画素ピッチを等間隔に設定することができる上に、最適な電源幅を選択しつつ、画素の高開口率を得ることができる。

【００１１】

本発明の電気光学装置は、複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された各々に電気光学素子を備えた複数の画素と、を含む電気光学装置であって、前記電気光学素子に駆動電圧を供給する複数の電源線を含み、前記複数の画素は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素群を構成し、前記複数の画素群の各々の画素群の間に複数の配線形成領域が設けられ、前記複数の配線形成領域のうち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線と、前記複数のデータ線のうち少なくとも一つのデータ線がともに形成されている、ことを特徴とする。かかる構成により、画素ピッチを等間隔に設定することができる上に、最適な電源幅を選択しつつ、画素の高開口率を得るこ

とができる。

【００１２】

好ましくは、前記配線形成領域の幅を略等しくする。配線形成領域の幅を略等しくすることで、画素ピッチを等間隔に設定できる。

【００１３】

好ましくは、前記電気光学素子には、駆動電圧が異なる電気光学素子を含み、前記駆動電圧に応じて前記電気光学素子へ電圧を供給する電源線の幅が異なる。電源線の幅が異なる場合であっても、上述のように配線レイアウトを工夫することで、開口率を高めつつ、画素ピッチを等間隔にできる。

【００１４】

好ましくは、前記電気光学素子は発光素子であり、前記電源線は前記発光素子の発光色に対応して幅が異なる。電気光学素子の特性に応じた最適な電源幅を選択することにより、デバイス設計の自由度を高めることができる。

【００１５】

好ましくは、前記発光色は、赤、緑、又は青である。これにより、フルカラー表示が可能となる。

【００１６】

好ましくは、前記電気光学素子はエレクトロルミネセンス素子である。エレクトロルミネセンス素子によれば、電流制御により発光階調を制御できる。

【００１７】

本発明の電子機器は、本発明の電気光学装置を備える。電子機器としては、表示装置を備えるものであれば特に限定はなく、例えば、携帯電話、ビデオカメラ、パーソナルコンピュータ、ヘッドマウントディスプレイ、プロジェクタ、ファックス装置、デジタルカメラ、携帯型ＴＶ、ＤＳＰ装置、ＰＤＡ、電子手帳などに適用できる。

【００１８】

本発明のマトリクス基板は、マトリクス状に配置された複数の画素電極を備えたマトリクス基板であって、前記複数の画素電極は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素電極からなる複数の画素電極群を構成し

ており、前記複数の画素電極群の各々の画素電極群の間に配線形成領域が設けられ、前記配線形成領域の幅は略等しい、ことを特徴とする。かかる構成により、画素ピッチを等間隔に設定できる。

【００１９】

本発明のマトリクス基板は、複数の走査線と、複数のデータ線と、前記走査線と前記データ線との交差部に対応して配置された複数の画素電極と、を含むマトリクス基板であって、前記複数の画素電極に電圧を供給するための複数の電源線を含み、前記複数の画素電極は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる画素電極群を構成し、前記複数の画素電極群の各々の画素電極群の間に複数の配線形成領域が設けられ、前記複数の配線形成領域のうち、少なくとも１つの配線形成領域には、前記複数の電源線のうち少なくとも一つの電源線、前記複数の走査線のうち少なくとも一つの走査線、及び前記複数のデータ線のうち少なくとも一つのデータ線から選ばれた少なくとも二つの配線が形成されている、ことを特徴とする。かかる構成により、画素ピッチを等間隔に設定することができる上に、最適な電源幅を選択しつつ、画素の高開口率を得ることができる。

【００２０】

【発明の実施の形態】

発明の実施の形態１．

以下、各図を参照して本実施形態について説明する。

【００２１】

図１は本実施形態のアクティブマトリクス型有機ＥＬディスプレイパネル１００の全体構成図である。同図に示すように、ディスプレイパネル１００は基板１６上にてＮ行Ｍ列のマトリクス状に配列された複数の画素１０を備える表示領域１１と、行方向に並ぶ一群の画素１０に接続する走査線に走査信号を出力する走査線ドライバ１２と、列方向に並ぶ一群の画素１０に接続するデータ線及び電源線にデータ信号及び電源電圧を供給するデータ線ドライバ１３とを備えて構成されている。各々の画素１０には、ＲＧＢ三原色で発光する有機ＥＬ素子が形成されている。表示領域１１の全面には共通電極としての陰極１４が被覆成膜されて

おり、陰極取り出し電極１５を介して外部回路と接続している。

【００２２】

尚、同図に示す有機ＥＬディスプレイパネル１００は、基板１６側から光を射出するいわゆるトップエミッション構造のタイプであるが、本発明はこれに限らず、透明陰極から光を射出するいわゆるボトムエミッション構造のタイプでもよい。

【００２３】

図２は画素１０の主要回路構成図である。画素１０は、スイッチングトランジスタＴｒ１と、駆動トランジスタＴｒ２と、保持容量Ｃと、発光部ＯＬＥＤとを備えて構成されており、２トランジスタ方式により駆動制御される。スイッチングトランジスタＴｒ１はｎチャネル型ＦＥＴであり、そのゲート端子には走査線$V_{sel}$が接続されており、ドレイン端子にはデータ線$I_{dat}$が接続している。駆動トランジスタＴｒ２はｐチャネル型ＦＥＴであり、そのゲート端子はスイッチングトランジスタＴｒ１のソース端子に接続されている。また、同トランジスタのソース端子は電源線$V_{dd}$に接続されており、ドレイン端子は発光部ＯＬＥＤに接続している。さらに、同トランジスタのゲート／ソース間には保持容量が形成されている。上記の構成において、走査線$V_{sel}$に選択信号を出力し、スイッチングトランジスタＴｒ１を開状態にすると、データ線$I_{dat}$を介して供給されたデータ信号は電圧値として保持容量Ｃに書き込まれる。すると、保持容量Ｃに書き込まれた保持電圧は１フレーム期間を通じて保持され、当該保持電圧によって、駆動トランジスタＴｒ２のコンダクタンスがアナログ的に変化し、発光諧調に対応した順バイアス電流を発光部ＯＬＥＤに供給する。

【００２４】

図３は画素領域内における配線レイアウトを説明するための図である。同図においては、説明を簡略化するため、２行３列に配列する６画素分の配線レイアウトを図示している。図中、Ｒ，Ｇ，Ｂとあるのは、それぞれ赤、緑、青で発光する画素１０であることを意味しており、ＲＧＢの画素群が列方向に配列している。また、$V_{dd-R}$は赤の画素の電源線、$V_{dd-G}$は緑の画素の電源線、$V_{dd-B}$は青の画素の電源線、１７は有機ＥＬ素子の画素電極（陽極）である。その他の符号の

うち上述したものについては詳細な説明を省略する。また、３１は（ｍ－１）列の画素群とｍ列の画素群の間に形成されるライン状の配線形成領域であり、列方向の画素配列長とほぼ同程度の長さにわたって、列方向に延在している。同様に、３２はｍ列と（ｍ＋１）列の画素群の間、３３は（ｍ＋１）列と（ｍ＋２）列の画素群の間、３４は（ｍ＋２）列と（ｍ＋３）列の画素群の間に形成される配線形成領域である。説明の便宜上、（ｍ－１）列の画素群と（ｍ＋３）列の画素群は図示されていない。本実施形態においては、配線形成領域３１～３４の幅をできるだけ均一に設定するため、これらの配線形成領域にレイアウトされる２以上の配幅の合計を各々等しくする。電源線$V_{dd}$の幅は有機ＥＬ素子の発光層の材料によって異なるが、ここでは説明の便宜上、緑、赤、青の順に電源線の幅が太くなるものとする。つまり、$V_{dd-G}$の幅＞$V_{dd-R}$の幅＞$V_{dd-B}$の幅と仮定する。

【００２５】

上記の仮定の下では、配線形成領域３１～３４の幅をできるだけ均一にするため、電源線$V_{dd}$とデータ線$I_{dat}$の幅の合計値がほぼ等しくなるような組み合わせを選択する。例えば、最大幅を有する$V_{dd-G}$と最小幅を有する$V_{dd-B}$との幅の合計値と、中間幅を有する$V_{dd-R}$とデータ線$I_{dat}$の幅の合計値と、データ線$I_{dat}$２本の幅の合計値とがそれぞれほぼ等しいものとすると、これらの電源線$V_{dd}$とデータ線$I_{dat}$の組み合わせを各配線形成領域３１～３４上にレイアウトする。同図に示す例では、最大幅を有する$V_{dd-G}$と最小幅を有する$V_{dd-B}$とを一組にして、配線形成領域３３上にレイアウトし、中間幅を有する$V_{dd-R}$とデータ線$I_{dat}$とを一組にして、配線形成領域３１及び３４上にレイアウトし、データ線$I_{dat}$２本を一組にして、配線形成領域３２上にレイアウトしている。但し、配線形成領域３１については、電源線$V_{dd-R}$のみを図示し、配線形成領域３４についてはデータ線$I_{dat}$のみを図示している。一方、走査線$V_{sel}$については、行方向に並ぶ画素群同士の間において、当該画素群の画素配列長とほぼ同程度の長さを有するライン状の配線形成領域につき、１本づつレイアウトされている。同図に示す配線レイアウトは周期的に繰り返す配線パターンの１単位を示すものであり、任意に選んだＲＧＢの画素１０における配線レイアウトは全て同図に示すパターンに設定されている。このため、本実施形態においては、画素の列方向に沿って

形成される配線形成領域の配置レイアウトを規定するレイアウト図を仮想的に想定して、複数の配線形成領域のうち特定の配線形成領域に着目し、当該配線形成領域を中心として前記レイアウト図を仮想的に折り返したとき、同種類の配線の組み合わせを有する配線形成領域同士が重なるようになっている。

【００２６】

本実施形態によれば、画素マトリクスの列方向に延在する同種の電源線が行方向に対して略等間隔の配列ピッチで形成されているため、画素ピッチを等間隔に設定することができ、有機ＥＬディスプレイのように色毎に消費電流の異なるデバイスにおいて設計の自由度を高めることができる。特に、インクジェット方式を利用して発光層を成膜するには、画素ピッチは等間隔であることが望ましいため、製造プロセス上のメリットが大きい。また、色毎に最適な電源線の幅を選択できるため、高開口率を維持したまま、最適な色バランスを確保しつつ、さらに消費電力を低減することができる。

【００２７】

但し、上記に示した例は一例であり、上述した例に限られるものではない。例えば、ＲＧＢ３本の電源線$V_{dd}$のうち何れか２本の電源配線を選択する組み合わせは全部で３通りあるため、本実施形態に示す配線レイアウトのパターンは全部で３通りとなる。また、本実施形態においては、行方向の配線形成領域に走査線$V_{sel}$を１本づつレイアウトし、列方向の配線形成領域３１，３２，及び３３に３本の電源配線$V_{dd}$と３本のデータ線$I_{dat}$の中から何れか２本の組み合わせを選択してレイアウトする構成を示したが、本発明はこれに限られるものではない。以下に各種の変形例について説明する。

【００２８】

発明の実施の形態２．

図４は本発明の第２の形態における配線レイアウトの説明図である。

【００２９】

本実施形態においては、画素の行方向に沿って形成される配線形成領域の配置レイアウトを規定するレイアウト図を仮想的に想定して、複数の配線形成領域の

うち特定の配線形成領域に着目し、当該配線形成領域を中心として前記レイアウト図を仮想的に折り返したとき、同種類の配線の組み合わせを有する配線形成領域同士が重なるように構成されている。（ｎ－１）行目の行方向に並ぶ画素群（図示せず）とｎ行目の行方向に並ぶ画素群との間の配線形成領域４１には３本の電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$が一組となって行方向にレイアウトされており、ｎ行目の行方向に配列する画素群と（ｎ＋１）行目の行方向に配列する画素群との間の配線形成領域４２には２本の走査線$V_{sel}$が一組となって行方向にレイアウトされている。行方向における配線レイアウトの基本的なパターンは３本の電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$と２本の走査線$V_{sel}$をそれぞれ一組としてレイアウトし、この基本パターンを周期的に繰り返しレイアウトする構成となっている。従って、（ｎ＋１）行目の行方向に配列する画素群と（ｎ＋２）行目の行方向に配列する画素群との間の配線形成領域４３における配線レイアウトは配線形成領域４１における配線レイアウトと同じである。

【００３０】

一方、列方向に配列する画素群同士の間の配線形成領域には、１本の電源線$V_{dd}$と１本のデータ線$I_{dat}$とが一組となって列方向にレイアウトされている。同図に示す例では、ｍ列目の列方向に配列するＲの画素群と（ｍ＋１）列目の列方向に配列するＧの画素群との間の配線形成領域５１に電源線$V_{dd-R}$とデータ線$I_{dat}$とが一組となってレイアウトされている。同様に、（ｍ＋１）列目の列方向に配列するＧの画素群と（ｍ＋２）列目の列方向に配列するＢの画素群（図示せず）との間の配線形成領域には電源線$V_{dd-G}$とデータ線$I_{dat}$とが一組となってレイアウトされているが、説明の便宜上、電源線$V_{dd-G}$のみ図示してある。また、行方向及び列方向にレイアウトされている電源線$V_{dd-R}$は各々異なるレイヤに敷設されており、層間絶縁膜に開口するコンタクトホールｈ１を介して導通している。電源線$V_{dd-G}$についても同様にコンタクトホールｈ２を介して導通している。

【００３１】

本実施形態によれば、画素マトリクスの行方向に延在する同種の電源線が列方向に対して略等間隔の配列ピッチで形成されているため、実施形態１と同様の効

果が得られる他、電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$が画素領域内においてマトリクス状に行方向及び列方向にレイアウトされているため、電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$の配線抵抗を低減させることができ、有機ＥＬ素子への電流供給を十分に行うことができる。このため、特定の電源線だけが電流供給不十分になることによる輝度ムラの発生を抑止することができ、クロストークの発生を低減できる。特に、大画面ディスプレイにおいては、画面内に十分な電流を均一に供給する必要があるため、特に効果がある。

【００３２】

発明の実施の形態３．

図５は本発明の第３の形態における配線レイアウトの説明図である。

【００３３】

本実施形態においては、画素の行方向及び列方向に沿って形成される配線形成領域の配置レイアウトを規定するレイアウト図を仮想的に想定して、複数の配線形成領域のうち特定の配線形成領域に着目し、当該配線形成領域を中心として前記レイアウト図を仮想的に折り返したとき、同種類の配線の組み合わせを有する配線形成領域同士が重なるように構成されている。（ｎ－１）行目の行方向に並ぶ画素群（図示せず）とｎ行目の行方向に並ぶ画素群との間の配線形成領域６１には３本の電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$が一組となって行方向にレイアウトされており、ｎ行目の行方向に配列する画素群と（ｎ＋１）行目の行方向に配列する画素群との間の配線形成領域６２には２本の走査線$V_{sel}$が一組となって行方向にレイアウトされている。行方向における配線レイアウトの基本的なパターンは３本の電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$と２本の走査線$V_{sel}$をそれぞれ一組としてレイアウトし、この基本パターンを周期的に繰り返しレイアウトする構成となっている。従って、（ｎ＋１）行目の行方向に配列する画素群と（ｎ＋２）行目の行方向に配列する画素群との間の配線形成領域６３における配線レイアウトは配線形成領域６１における配線レイアウトと同じである。

【００３４】

一方、列方向に配列する画素群同士の間には３本の電源線$V_{dd-G}$，$V_{dd-R}$，及

び$V_{dd-B}$が３本のデータ線$I_{dat}$の中から選ばれた２本一組からなる３通りの組み合わせでレイアウトされている。同図に示す例では、（ｍ－１）列目の列方向に配列するＢの画素群（図示せず）とｍ列目の列方向に配列するＲの画素群との間の配線形成領域７１に電源線$V_{dd-G}$（図示せず）とデータ線$I_{dat}$とが一組となってレイアウトされており、ｍ列目の列方向に配列するＲの画素群と（ｍ＋１）列目の列方向に配列するＧの画素群との配線形成領域７２には２本の電源線$V_{dd-G}$，$V_{dd-R}$が一組となってレイアウトされている。また、（ｍ＋１）列目の列方向に配列するＧの画素群と（ｍ＋２）列目の列方向に配列するＢの画素群との間の配線形成領域７３に２本のデータ線$I_{dat}$が一組となってレイアウトされており、（ｍ＋２）列目の列方向に配列するＢの画素群と（ｍ＋３）列目の列方向に配列するＲの画素群（図示せず）との間の配線形成領域７４には電源線$V_{dd-G}$とデータ線$I_{dat}$とが一組となってレイアウトされている。

【００３５】

行方向及び列方向にレイアウトされている電源線$V_{dd-R}$は各々異なるレイヤに敷設されており、層間絶縁膜に開口するコンタクトホールｈ１を介して導通している。電源線$V_{dd-G}$及び電源線$V_{dd-B}$ついても同様に行方向及び列方向に対して異なるレイヤに敷設されており、コンタクトホールｈ２及びｈ３を介してそれぞれ導通している。これらのコンタクトホールｈ１，ｈ２，及びｈ３は複数形成することで、配線の断線対策に効果があり、さらに配線の低抵抗化を図ることができるメリットがある。

【００３６】

本実施形態によれば、画素マトリクスの行方向に延在する同種の電源線が列方向に対して略等間隔の配列ピッチで形成され、かつ、画素マトリクスの列方向に延在する同種の電源線が行方向に対して略等間隔の配列ピッチで形成されるため、実施形態１と同様の効果が得られる他、電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$が画素領域内においてマトリクス状に行方向及び列方向にレイアウトされているため、電源線$V_{dd-G}$，$V_{dd-R}$，及び$V_{dd-B}$の配線抵抗を低減させることができ、有機ＥＬ素子への電流供給を十分に行うことができる。このため、特定の電源線だけが電流供給不十分になることによる輝度ムラの発生を抑止することができ、ク

ロストークの発生を低減できる。特に、大画面ディスプレイにおいては、画面内に十分な電流を均一に供給する必要があるため、特に効果がある。

【００３７】

発明の実施の形態４．

図６は本発明の電気光学装置を適用可能な電子機器の例を示す図である。同図（ａ）は携帯電話への適用例であり、携帯電話２３０は、アンテナ部２３１、音声出力部２３２、音声入力部２３３、操作部２３４、及び本発明の有機ＥＬディスプレイパネル１００を備えている。このように本発明の有機ＥＬディスプレイパネル１００を携帯電話２３０の表示部として利用可能である。同図（ｂ）はビデオカメラへの適用例であり、ビデオカメラ２４０は、受像部２４１、操作部２４２、音声入力部２４３、及び本発明の有機ＥＬディスプレイパネル１００を備えている。このように本発明の有機ＥＬディスプレイパネル１００は、ファインダーや表示部として利用可能である。同図（ｃ）は携帯型パーソナルコンピュータへの適用例であり、コンピュータ２５０は、カメラ部２５１、操作部２５２、及び本発明の有機ＥＬディスプレイパネル１００を備えている。このように本発明の有機ＥＬディスプレイパネル１００は、表示装置として利用可能である。

【００３８】

同図（ｄ）はヘッドマウントディスプレイへの適用例であり、ヘッドマウントディスプレイ２６０は、バンド２６１、光学系収納部２６２及び本発明の有機ＥＬディスプレイパネル１００を備えている。このように本発明の有機ＥＬディスプレイパネル１００は画像表示源として利用可能である。同図（ｅ）はリア型プロジェクターへの適用例であり、プロジェクター２７０は、筐体２７１に、光源２７２、合成光学系２７３、ミラー２７４、ミラー２７５、スクリーン２７６、及び本発明の有機ＥＬディスプレイパネル１００を備えている。同図（ｆ）はフロント型プロジェクターへの適用例であり、プロジェクター２８０は、筐体２８２に光学系２８１及び本発明の有機ＥＬディスプレイパネル１００を備え、画像をスクリーン２８３に表示可能になっている。このように本発明の有機ＥＬディスプレイパネル１００は画像表示源として利用可能である。

【図面の簡単な説明】

【図１】　本発明の有機ＥＬディスプレイパネルの平面図である。

【図２】　画素の主要回路構成図である。

【図３】　第１の実施形態における配線レイアウトの説明図である。

【図４】　第２の実施形態における配線レイアウトの説明図である。

【図５】　第３の実施形態における配線レイアウトの平面図である。

【図６】　本発明の有機ＥＬディスプレイの応用例の説明図である。

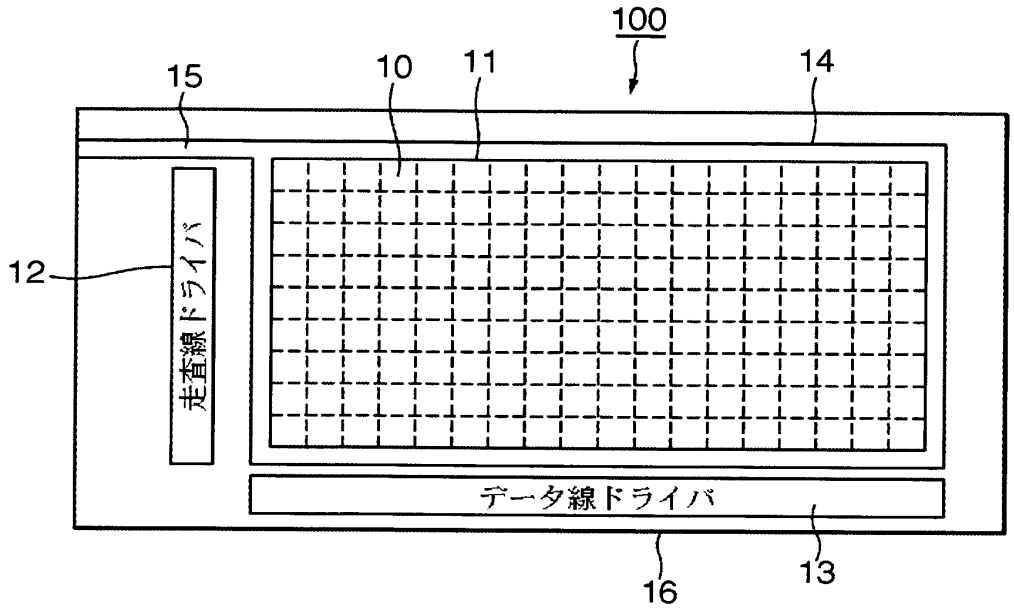
【符号の説明】

１０…画素　１１…画素領域　１２…走査線ドライバ　１３…データ線ドライバ　１４…陰極　１５…陰極取出電極　１６…基板　１７…画素電極　$V_{dd}$…電源線　$V_{sel}$…走査線　$I_{dat}$…データ線　Ｔｒ１…スイッチングトランジスタ　Ｔｒ２…駆動トランジスタ　Ｃ…保持容量　ＯＬＥＤ…発光部

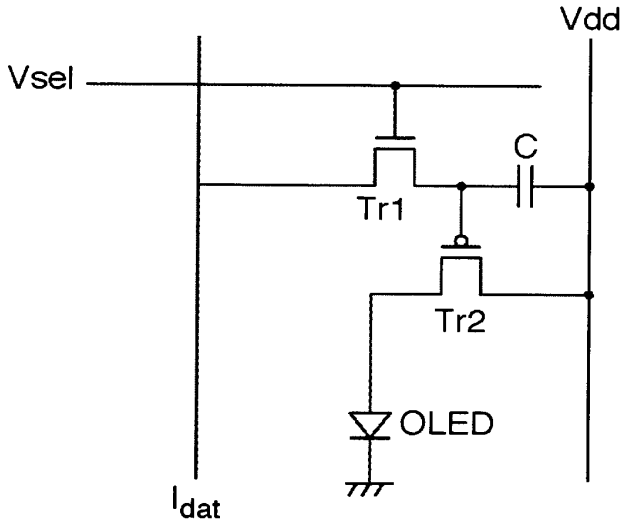
出証特２００３－３０７４６５６

【書類名】　図面

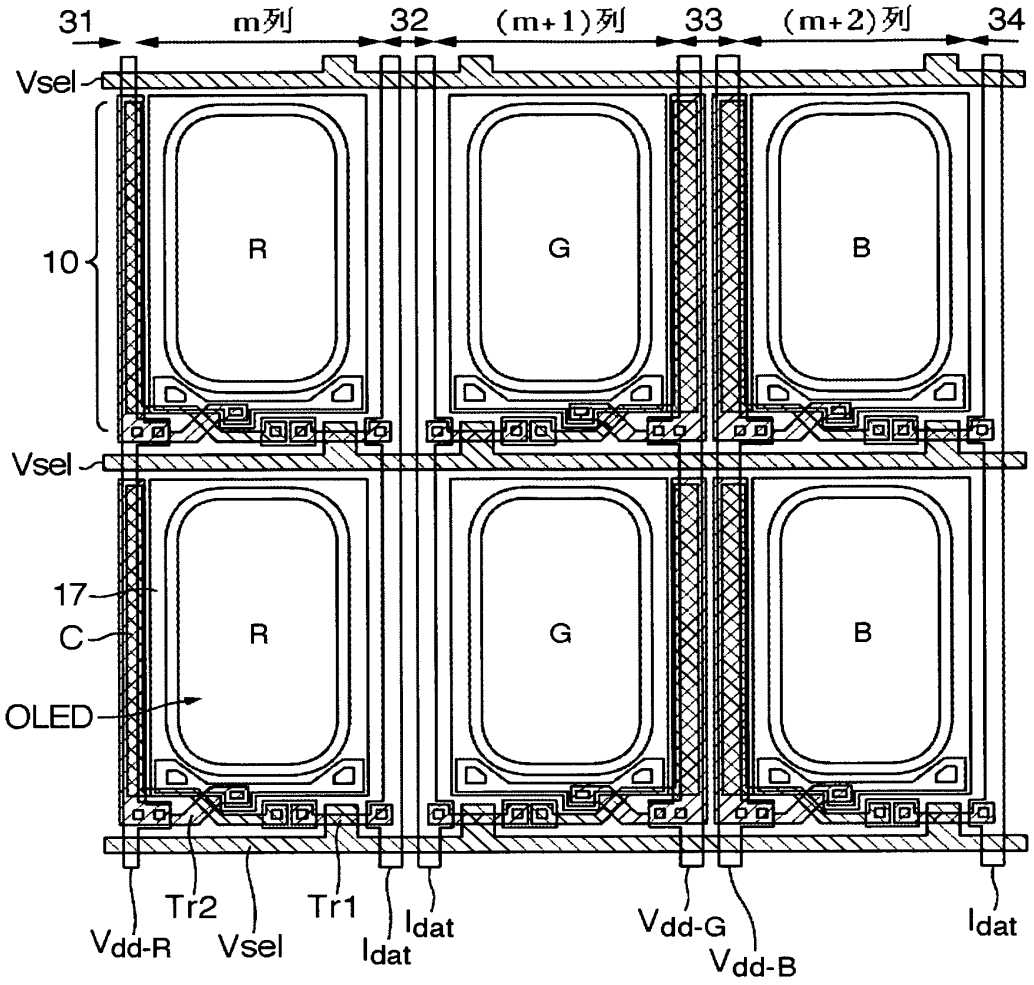
【図１】


100
15
10
11
14
12
走査線ドライバ
データ線ドライバ
16
13

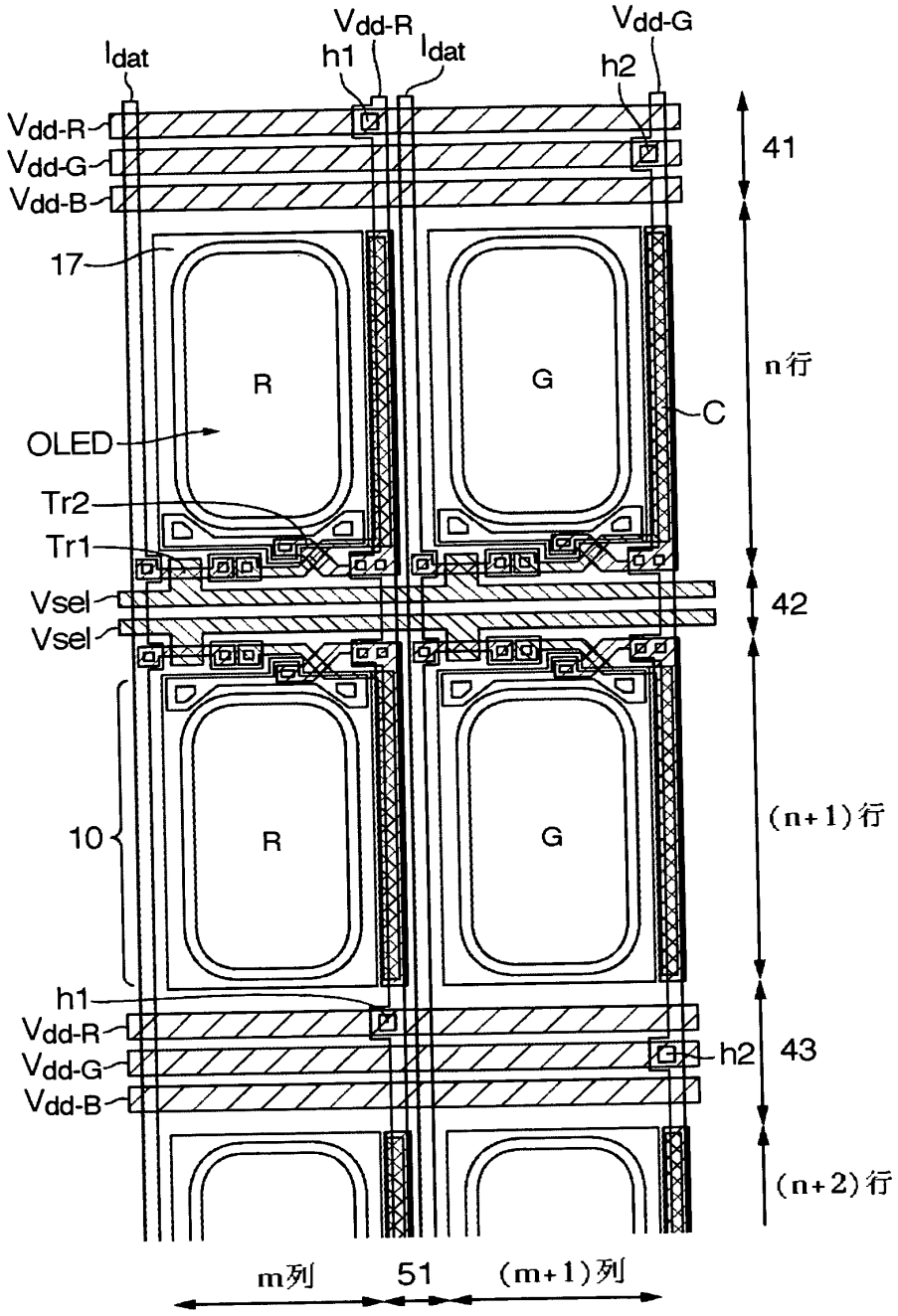
【図２】


Vdd
Vsel
C
Tr1
Tr2
OLED
Idat

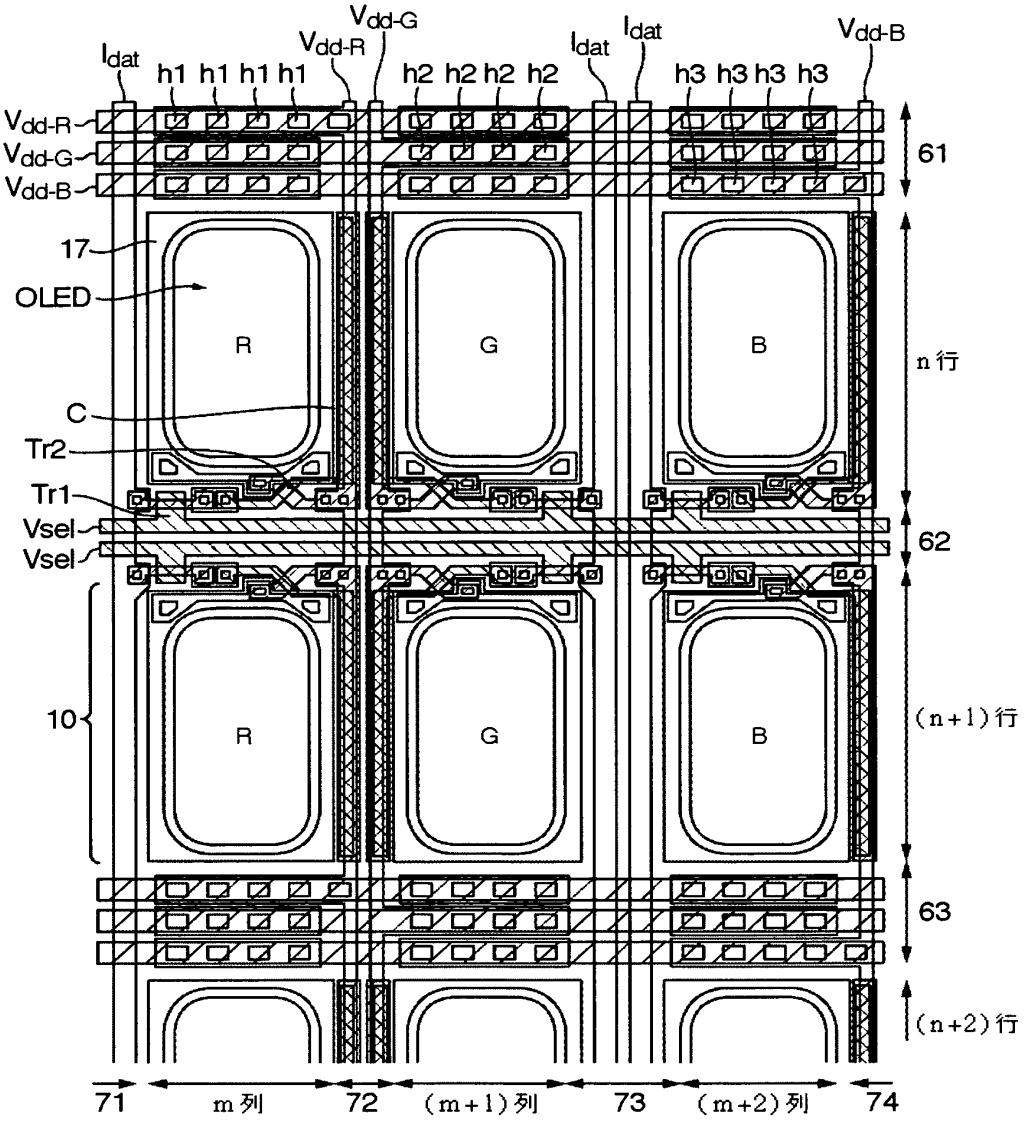
【図３】


31
m列
32
(m+1)列
33
(m+2)列
34
Vsel
10
R
G
B
Vsel
17
C
OLED
R
G
B
Vdd-R
Tr2
Vsel
Tr1
Idat
Idat
Vdd-G
Vdd-B
Idat

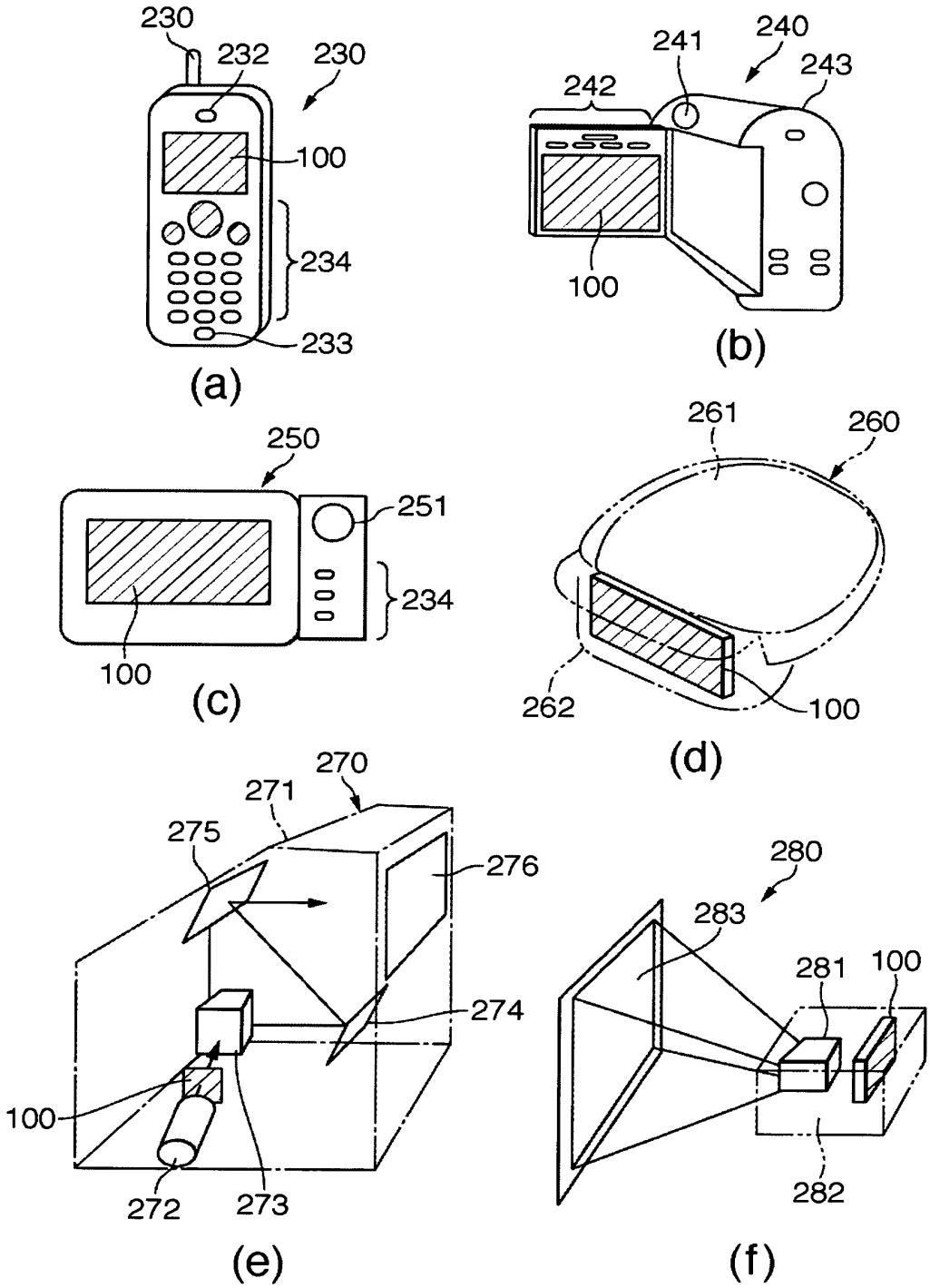
【図４】


Idat
Vdd-R
h1
Idat
Vdd-G
h2
Vdd-R
Vdd-G
Vdd-B
17
R
G
C
OLED
Tr2
Tr1
Vsel
Vsel
10
R
G
h1
Vdd-R
Vdd-G
Vdd-B
h2
41
n行
42
(n+1)行
43
(n+2)行
m列
51
(m+1)列

【図５】


Idat
h1 h1 h1 h1
Vdd-R
Vdd-G
h2 h2 h2 h2
Idat
Idat
h3 h3 h3 h3
Vdd-B
Vdd-R
Vdd-G
Vdd-B
61
17
OLED
R
G
B
n行
C
Tr2
Tr1
Vsel
Vsel
62
10
R
G
B
(n+1)行
63
(n+2)行
71
m列
72
(m+1)列
73
(m+2)列
74

【図６】




出証特２００３－３０７４６５６

【書類名】　要約書

【要約】

【課題】　画素の配列ピッチを等間隔に設定しつつ、画素の開口率を高めることができる電源線の配線レイアウトを提案する。

【解決手段】　本発明の電気光学装置は、電源回路から電源供給を受けて駆動される電気光学素子を含む、マトリクス状に配置された複数の画素（１０）を備えた電気光学装置であって、前記複数の画素（１０）は、行方向又は列方向のうち少なくとも何れか一方向に並ぶ一連の画素からなる複数の画素群を構成しており、前記複数の画素群の各々の画素群の間に配線形成領域（３１，３２，３３，３４）が設けられ、前記配線形成領域（３１，３２，３３，３４）の幅は略等しいことを特徴とする。

【選択図】　図３

出証特２００３－３０７４６５６

# 認定・付加情報

| | |
|---|---|
| 特許出願の番号 | 特願２００２－２９３６９６ |
| 受付番号 | ５０２０１５０６７９０ |
| 書類名 | 特許願 |
| 担当官 | 第四担当上席　００９３ |
| 作成日 | 平成１４年１０月　８日 |

＜認定情報・付加情報＞

【提出日】　平成14年10月 7日

次頁無

出証特２００３－３０７４６５６

特願２００２－２９３６９６

出　願　人　履　歴　情　報

識別番号　　［０００００２３６９］

１．変更年月日　　１９９０年　８月２０日
［変更理由］　　新規登録
住　所　　東京都新宿区西新宿２丁目４番１号
氏　名　　セイコーエプソン株式会社

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[redacted]

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al.

Application No.: 10/676,067

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

**LETTER TO THE OFFICIAL DRAFTSPERSON**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please substitute the attached 5 sheets of formal drawings depicting Figures 1-6F for the corresponding drawings filed with the application. The attached drawings correspond to the facsimile copies of the drawings filed on October 2, 2003.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Date: October 23, 2003

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

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Fig. 1

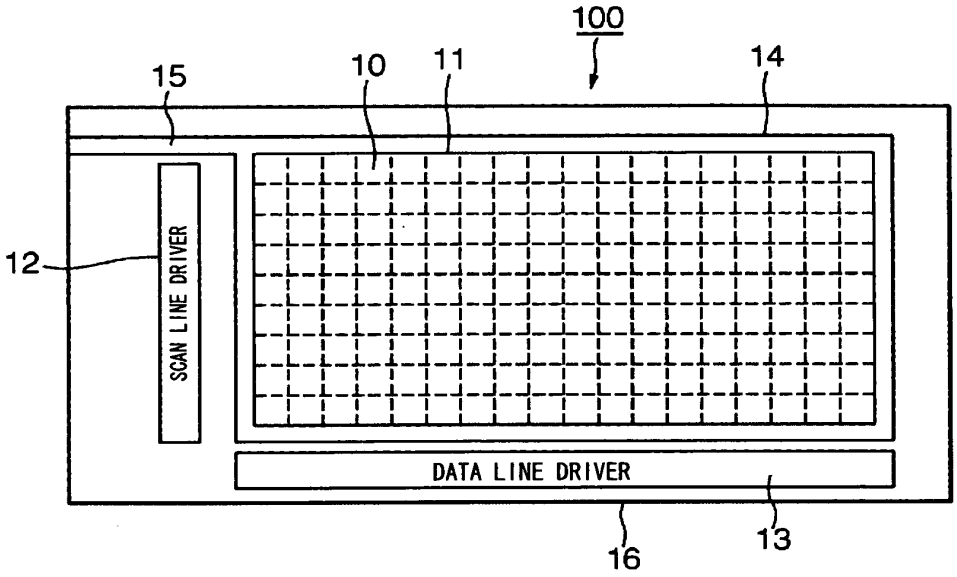
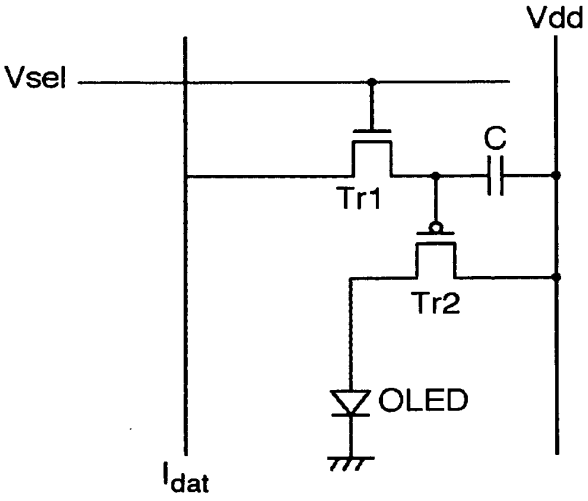
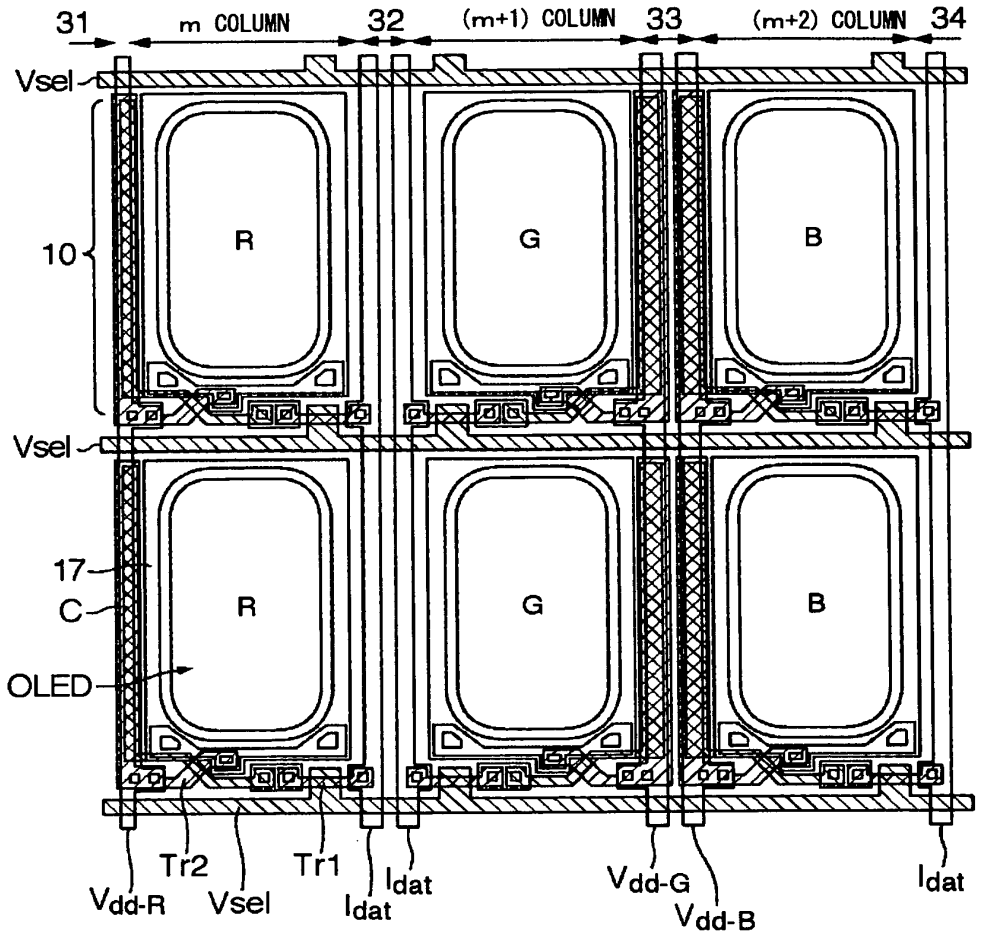



Fig. 2



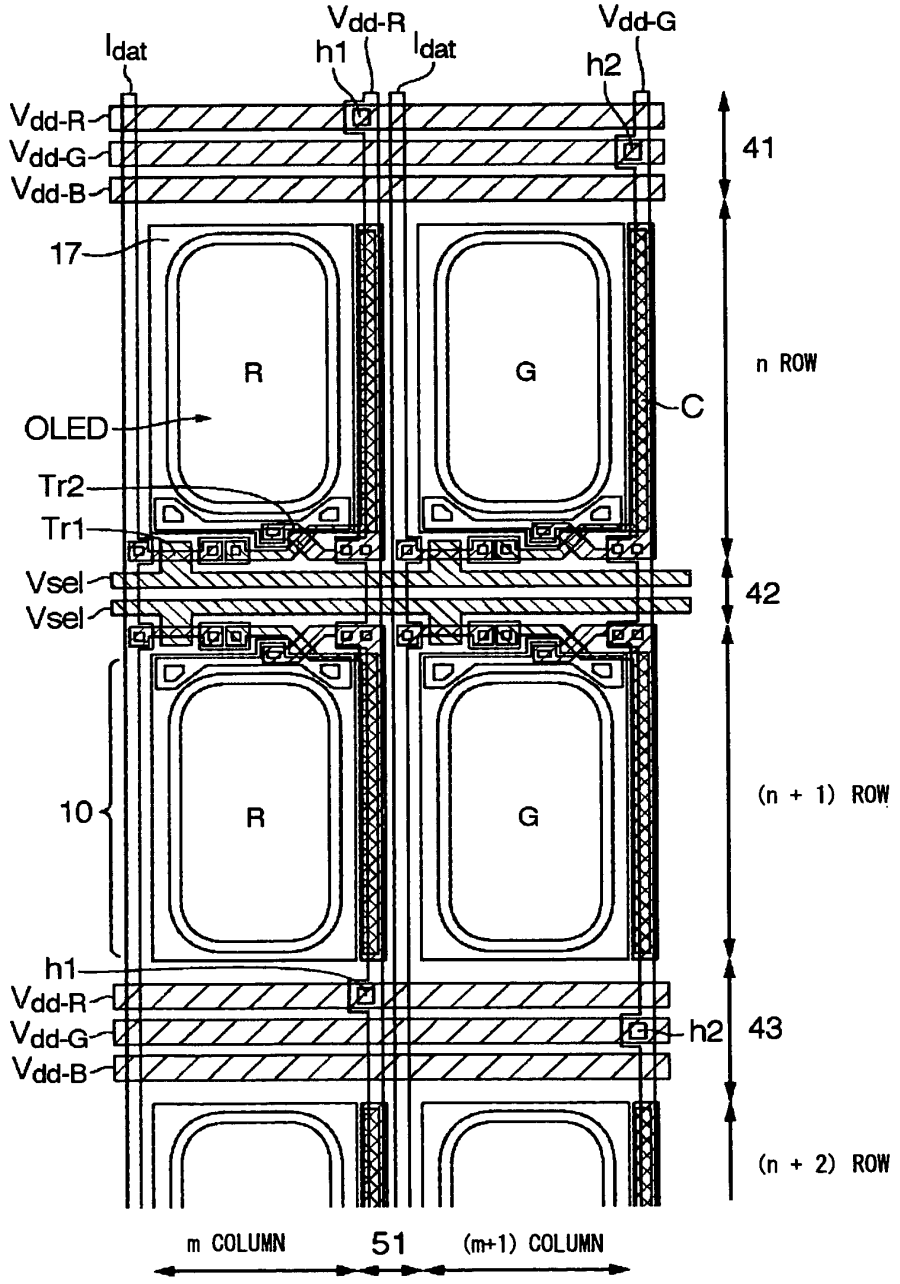
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Fig. 3



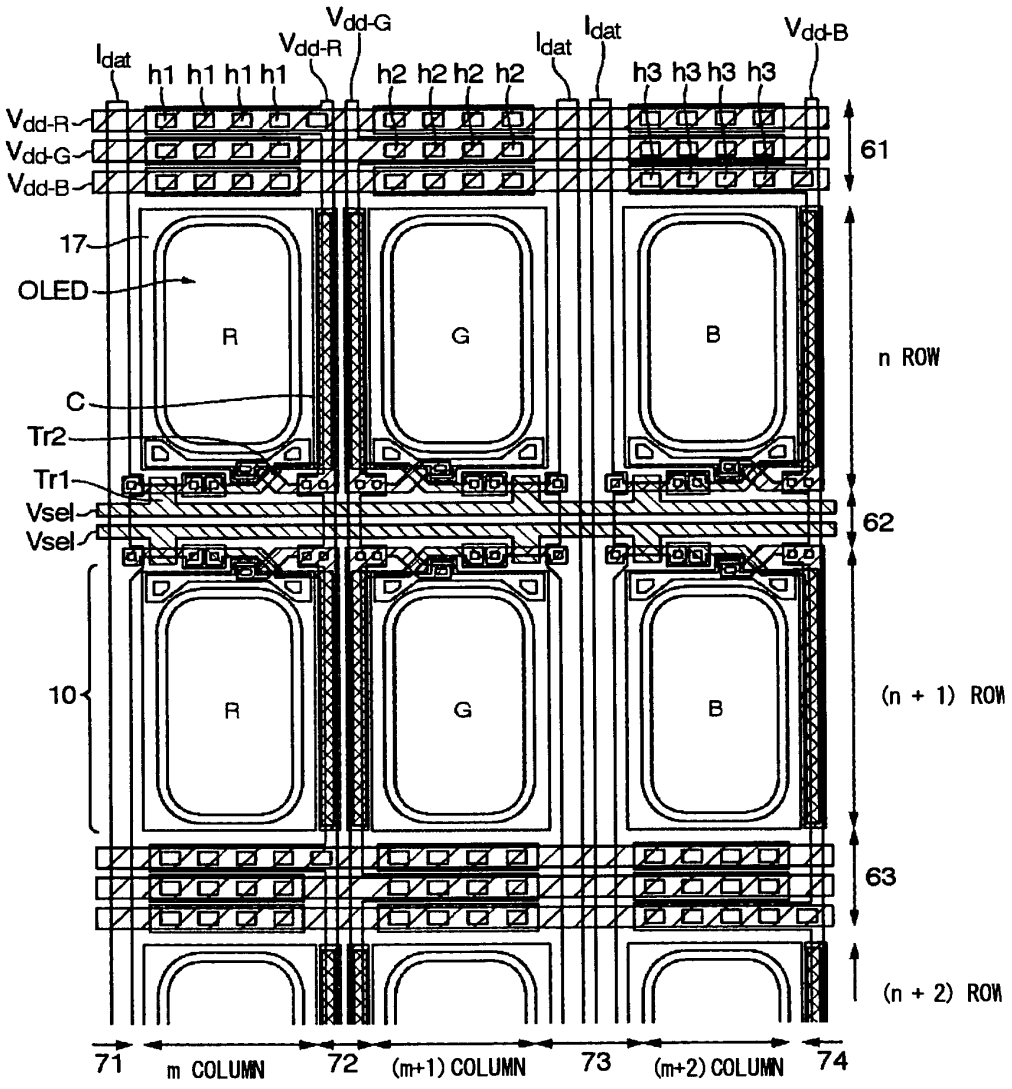
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Fig. 4



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Fig. 5



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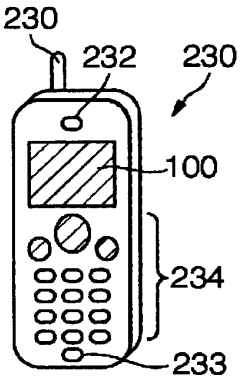



Fig. 6A

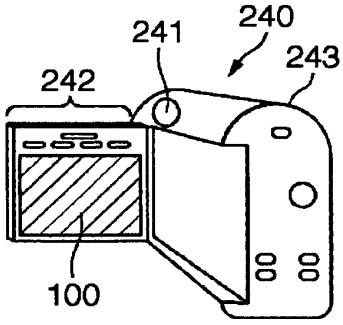



Fig. 6B

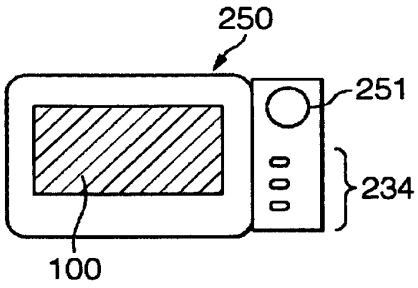



Fig. 6C

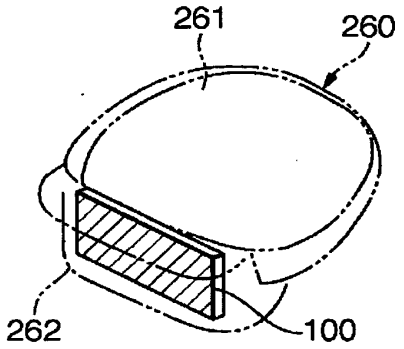



Fig. 6D

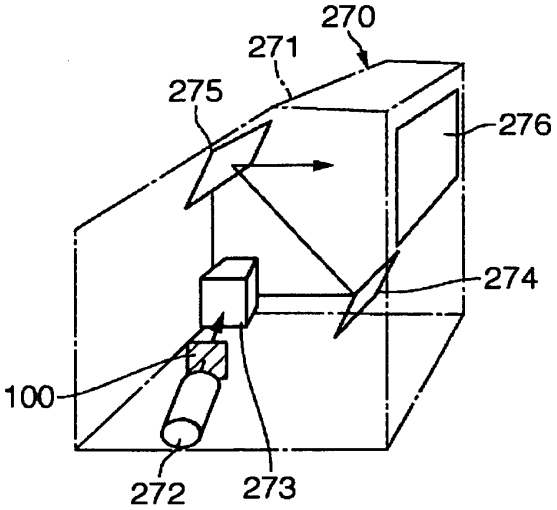



Fig. 6E

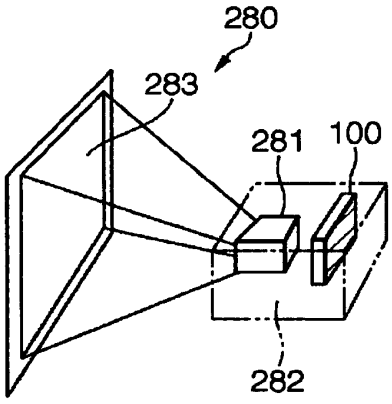



Fig. 6F

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**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al.

Application No.: 10/676,067

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

**PRELIMINARY AMENDMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please consider the following:

**Amendments to the Specification**;

**Amendments to the Claims** as reflected in the listing of claims; and

**Remarks**.

**Amendments to the Specification**

Attached are a marked-up copy of the originally filed specification and a clean substitute specification in accordance with 37 C.F.R. §§1.121(b)(3) and 1.125(c). The substitute specification contains no new matter.

Please replace the Abstract with the attached amended Abstract.

**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical ~~device~~ device, comprising:

an electric power supply circuit; and

a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from ~~an~~ the electric power supply circuit, ;

~~wherein said~~ the plurality of pixels ~~make~~ making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, ;

~~and wherein~~ line forming regions ~~are~~ being formed between adjacent pixel groups of ~~said~~ the plurality of pixel groups, ;

and ~~wherein said~~the line forming regions ~~are~~ being formed with generally the same width.

2. (Currently Amended) An electro-optical ~~device~~ device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of ~~said~~ the scan lines and ~~said~~ the data lines, including electro-optical devices; and

a plurality of electric power lines ~~for supplying~~to supply driving voltage to ~~said~~ the electro-optical devices;

~~wherein said~~the plurality of pixels ~~make~~ making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, ;

~~and wherein~~ a plurality of line forming regions ~~are~~ being formed between adjacent pixel groups of said plurality of pixel groups, ;

and ~~wherein~~ at least two lines selected from at least one electric power line of ~~said~~ the plurality of electric power lines, at least one scan line of ~~said~~ the plurality of scan lines, and at least one data line of ~~said~~ the plurality of data lines, ~~are~~ being formed in at least one line forming region of ~~said~~ the plurality of line forming regions.

3. (Currently Amended) An electro-optical ~~device~~ device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of ~~said~~ the scan lines and ~~said~~ the data lines, including electro-optical devices; and

a plurality of electric power lines ~~for supplying~~to supply driving voltage to ~~said~~ the electro-optical devices;

~~wherein said~~the plurality of pixels ~~make~~ making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, ;

~~and wherein~~ a plurality of line forming regions ~~are~~ being formed between adjacent pixel groups of ~~said~~ the plurality of pixel groups, ;

and ~~wherein~~ both at least one electric power line of ~~said~~ the plurality of electric power lines and at least one scan line of ~~said~~ the plurality of scan lines ~~are~~ being formed in at least one line forming region of ~~said~~ the plurality of line forming regions.

4. (Currently Amended) An electro-optical ~~device~~ device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of ~~said~~ the scan lines and ~~said~~ the data lines, including electro-optical devices; and

a plurality of electric power lines ~~for supplying~~to supply driving voltage to ~~said~~ the electro-optical devices;

~~wherein said~~the plurality of pixels ~~make~~ making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction~~,~~;

~~and wherein~~ a plurality of line forming regions ~~are~~ being formed between adjacent pixel groups of said plurality of pixel groups~~,~~;

and ~~wherein~~ both at least one electric power line of ~~said~~ the plurality of electric power lines and at least one data line of ~~said~~ the plurality of data lines ~~are~~ being formed in at least one line forming region of ~~said~~ the plurality of line forming regions.

5. (Currently Amended) ~~An~~ The electro-optical device according to Claim 2, ~~wherein said~~the line forming regions ~~are~~ being formed with generally the same width.

6. (Currently Amended) ~~An~~ The electro-optical device according to Claim 1, ~~wherein said~~the electro-optical devices ~~are~~ being operated with each different driving voltages;

and ~~wherein said~~the electric power lines ~~for supplying~~to supply voltage to ~~said~~ the electro-optical devices ~~are~~ being formed with different widths corresponding to said driving voltage.

7. (Currently Amended) ~~An~~ The electro-optical device according to Claim 6, ~~wherein said~~the electro-optical device ~~is~~ being a light-emission device;

and ~~wherein said~~the electric power lines ~~are~~ being formed with different widths corresponding to the emission light color of said light-emission device.

8. (Currently Amended) ~~An~~ The electro-optical device according to Claim 7, the color of the light which is to be emitted ~~is~~ being at least one of red, green, ~~or~~ and blue.

9. (Currently Amended) ~~An~~ The electro-optical device according to Claim 1, ~~wherein said~~the electro-optical device ~~is~~ being an electro-luminescence device.

10. (Currently Amended) An electronic ~~apparatus~~ apparatus, comprising:

~~an~~ the electro-optical device according to Claim 1.

11. (Currently Amended) A matrix ~~substrate~~ substrate, comprising:

a plurality of pixel electrodes disposed in the form of a matrix, ;

~~wherein said~~ the plurality of pixel electrodes ~~make~~ making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, ;

~~and wherein~~ a plurality of line forming regions ~~are~~ being formed between adjacent pixel electrode groups of ~~said~~ the plurality of pixel electrode groups, ;

and ~~wherein said~~ the line forming regions ~~are~~ being formed with generally the same width.

12. (Currently Amended) A matrix ~~substrate~~ substrate, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel electrodes disposed at portions corresponding to intersections of ~~said~~ the scan lines and ~~said~~ the data lines; and

a plurality of electric power lines ~~for supplying~~to supply voltage to ~~said~~ the plurality of pixel electrodes;

~~wherein said~~the plurality of pixel electrodes ~~make~~ making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, ;

~~and wherein~~ a plurality of line forming regions ~~are~~ being formed between adjacent pixel electrode groups of ~~said~~ the plurality of pixel electrode groups, ~~;~~

~~and wherein~~ at least two lines selected from at least one electric power line of ~~said~~ the plurality of electric power lines, at least one scan line of ~~said~~ the plurality of scan lines, and at least one data line of ~~said~~ the plurality of data lines, ~~are~~ being formed in at least one line forming region of ~~said~~ the plurality of line forming regions.

## REMARKS

Claims 1-12 are pending. By this Preliminary Amendment, the Abstract and specification are replaced with an amended Abstract and substitute specification, and claims 1-12 are amended.

Prompt and favorable examination on the merits is respectfully requested.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Attachments:
Amendment Abstract
Substitute Specification
Marked-up Copy of Specification

Date: November 10, 2003

**OLIFF & BERRIDGE, PLC**
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## ABSTRACT OF THE DISCLOSURE

~~To provide~~The invention provides a wiring layout of electric power lines, which ~~improves~~ enhances the aperture ratio of the pixel while forming pixels with the same pixel pitch. An electric-optical apparatus according to the present invention ~~comprises~~ includes multiple pixels ~~(10)~~ arranged in matrix including electro-optical devices driven by receiving electric power from an electric power supply circuit. ~~, wherein the~~The aforementioned multiple pixels ~~(10)~~ make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and any of line forming regions ~~(31, 32, 33, 34)~~ is disposed between adjacent pixel groups of the aforementioned pixel groups. ~~, wherein the~~The aforementioned line forming regions ~~(31, 32, 33, 34)~~ are formed with generally the same width.

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# ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

## BACKGROUND OF THE INVENTION

1. Field of Invention

**[0001]** The present invention relates to a wiring layout suitable for an electro-optical device including electro-optical devices.

2. Description of Related Art

**[0002]** Organic EL devices are current-driven self-light-emitting devices, and accordingly provide the advantage of not needing a backlight. These devices provide other advantages, such as low power consumption, a wide range of vision, and a high contrast ratio. Thus, the related art is developing flat panel displays employing EL devices. The organic EL device is an electro-optical device including a light-emission layer introduced between an anode and a cathode. Upon supplying forward bias current between both the electrodes, self-light-emission is effected due to the recombination energy at the time of recombination of a hole injected from the anode and an electron injected from the cathode. Accordingly, a supply of electric power from an external circuit is required in order to cause the organic EL device to emit light.

**[0003]** With related art color-display active-matrix-driven display panels, an M number each of electric power lines and data lines are disposed in the column direction on a pixel matrix with an N number of columns and an M number of rows formed on a pixel region, as well as an N number of selection lines being disposed in the row direction on the aforementioned matrix. With a given pixel of such a wiring layout, a data line is disposed between the given pixel and the left-adjacent pixel, and an electric power line is disposed between the given pixel and the right-adjacent pixel. That is to say, with the lines disposed between adjacent pixels in the column direction, a layout is formed so that one data line and one electric line make up one pair. With the above-described configuration, the following elements are disposed at an intersection of a scan line and a data line: a switching transistor, a holding capacitance, a driving transistor, and an organic EL device for emitting light in one color of the RGB three primary colors, and these devices make up a pixel.

## SUMMARY OF THE INVENTION

**[0004]** With the related art arrangements, a light-emission layer is formed of a material corresponding to each color of the RGB three primary colors, and accordingly the organic EL device is operated with greatly different power consumption corresponding to

each color, so the optimal width of the electric power line is greatly different for each color. Accordingly, with the above-described wiring layout, while there is the need to determine the pixel pitch according to the maximal width for disposing the electric power lines, there is the need to form a pixel matrix with the same pixel pitch due to the restriction from the manufacturing process for a display, and accordingly there is the need to determine the pixel layout at the sacrifice of the aperture ratio. On the other hand, in the event of reducing the aperture ratio, there is the need to increase the amount of electric current supplied to the organic EL device to obtain predetermined luminance, and accordingly there is the need to form the electric power line with a greater width, leading to further reduction of the aperture ratio from the above-described reason.

**[0005]** As described above, with the related art wiring layout, the width of the electric line and the aperture ratio of the pixel are in the relation of trade off each other, and it is difficult to maintain a large aperture ratio while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.

**[0006]** Accordingly, the present invention provides a wiring method for electric power lines. The aperture ratio of the pixel can be increased while maintaining a pixel matrix with the same pixel pitch.

**[0007]** In order to address or solve the above, an electro-optical device according to the present invention includes multiple pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from an electric power supply circuit. The multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction. Line forming regions are formed between adjacent pixel groups of the multiple pixel groups. The line forming regions are formed with generally the same width. With such a configuration, a the pixel pitch can be made the same.

**[0008]** Here, "electro-optical device" means a general electronic device for changing the optical state of light by using electric effects, and include, besides self-light-emitting devices, such as electro-luminescence devices, electronic devices to display grayscale by adjusting the state of the polarized light, similarly to liquid crystal devices. With the present invention, the electro-luminescence devices are preferably employed. With the present invention, the electro-luminescence devices are employed, whereby current-driven self-light-emission devices can be obtained.

[0009] Another electro-optical device according to the present invention includes multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines to supply driving voltage to the electro-optical devices. The multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction. Multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups. At least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with an enhanced or the optimal width.

[0010] Another electro-optical device according to the present invention includes multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines to supply driving voltage to the electro-optical devices. The multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction. Multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups. Both at least one electric power line of the multiple electric power lines and at least one scan line of the multiple scan lines are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with an enhanced or the optimal width.

[0011] Another electro-optical device according to the present invention includes multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines to supply driving voltage to the electro-optical devices. The multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction. Multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups. At least one electric power line of the multiple electric power lines and at least one data line of the multiple data lines are formed in at least one line forming region of the multiple line forming regions. With

such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with an enhanced or the optimal width.

**[0012]** The aforementioned line forming regions are preferably formed with generally the same width. With the present invention, the line forming regions are formed with generally the same width, whereby the pixel matrix can be formed with the same pixel pitch.

**[0013]** The aforementioned electro-optical device preferably includes electro-optical devices which are operated with different driving voltages. The electric power lines to supply voltage to the electro-optical devices are formed with different widths corresponding to the driving voltage. Even with such a configuration where the electric power lines are formed with different widths, the wiring layout is designed as described above, whereby the pixel matrix can be formed with the same pixel pitch while enhancing the aperture ratio.

**[0014]** The aforementioned electro-optical device preferably is a light-emission device. The electric power lines are formed with each different width corresponding to the emission light color of the light-emission device. With the present invention, an enhanced or the optimal width of the electric power line is determined corresponding to the properties of the electro-optical device, thereby facilitating design of devices.

**[0015]** The color of the light which is to be emitted is preferably red, green, or blue. This enables full-color display.

**[0016]** The electro-optical device preferably is an electro-luminescence device. With the electro-luminescence device, the grayscale due to light emission can be controlled by current control.

**[0017]** An electronic apparatus according to the present invention includes an electro-optical device according to the present invention. The electronic apparatus is not particularly restricted so long as it includes a display device, and can be applied to, for example, cellular phones, video cameras, personal computers, head mount displays, projectors, facsimiles, digital cameras, portable TVs, DSP devices, PDAs, palmtops, and the like.

**[0018]** A matrix substrate according to the present invention includes multiple pixel electrodes disposed in the form of a matrix. The multiple pixel electrodes make up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction. Multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups. The line

forming regions are formed with generally the same width. With such a configuration, the pixel pitch can be made the same.

**[0019]** Another matrix substrate according to the present invention includes multiple scan lines, multiple data lines, multiple pixel electrodes disposed at portions corresponding to the intersections of the scan lines and the data lines, and multiple electric power lines to supply voltage to the multiple pixel electrodes. The multiple pixel electrodes make up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction. Multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups. At least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, the pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio, while forming the electric power lines with the optimal width.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** Fig. 1 is a plan view of an organic EL display panel according to the present invention;

**[0021]** Fig. 2 is a schematic of a principal circuit configuration diagram of a pixel;

**[0022]** Fig. 3 is a schematic describing a wiring layout according to a first exemplary embodiment;

**[0023]** Fig. 4 is a schematic describing a wiring layout according to a second exemplary embodiment;

**[0024]** Fig. 5 is a schematic describing a wiring layout according to a third exemplary embodiment;

**[0025]** Fig. 6(A) through Fig. 6(F) are schematics describing application examples employing the organic EL display according to the present invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

**[0026]** An exemplary embodiment is described below with reference to the drawings.

**[0027]** Fig. 1 is a schematic showing an overall configuration of an active-matrix organic-EL display panel 100 according to an exemplary embodiment. As shown in the drawing, the display panel 100 includes a display region 11 including multiple pixels 10

disposed in the form of a matrix with an N number of columns and an M number of rows, a scan line driver 12 to output scan signals to scan lines arrayed in the row direction which are connected to a group of pixels 10, a data line driver 13 to supply data signals and electric power to data lines and electric power lines arrayed in the column direction which are connected to a group of pixels 10. These components are disposed on a substrate 16. An organic EL device is formed on each pixel 10 to emit light in a color of the RGB three primary colors. A cathode 14 is formed in the form of a film as a common electrode on the entire face of the display region 11, and is connected to an external circuit through cathode output electrode 15.

**[0028]** While the organic EL display panel 100 shown in the drawing is a so-called "top-emission configuration display panel" which emits light from the side of the substrate 16, the present invention is not restricted to this arrangement, but rather, the present invention can also be applied to a bottom-emission configuration display panel which emits light from a transparent cathode.

**[0029]** Fig. 2 is a schematic of a principal circuit of the pixel 10. The pixel 10 includes a switching transistor Tr1, a driving transistor Tr2, holding capacitance C, a light-emission portion OLED, and is driven with the dual transistor method. The switching transistor Tr1 includes an n-channel FET. The gate terminal thereof is connected to the scan line $V_{sel}$, and the drain terminal thereof is connected to the data line $I_{dat}$. The driving transistor Tr2 includes a p-channel FET. The gate terminal is connected to the source terminal of the switching transistor Tr1. Furthermore, the source terminal of the transistor Tr2 is connected to the electric power line $V_{dd}$, and the drain terminal thereof is connected to the light-emission portion OLED. Furthermore, holding capacitance is formed between the gate and the source of the transistor Tr2. With the above-described configuration, upon outputting a selection signal to the scan line $V_{sel}$, and opening the transistor Tr1, the data signals supplied through the data line $I_{dat}$ are written to the holding capacitance C as a voltage value. Subsequently, the holding voltage written to the holding capacitance C is held during one frame period, and the conductance of the driving transistor Tr2 is determined according to the holding voltage in an analog manner, whereby forward bias current corresponding to light-emission level is supplied to the light-emission portion OLED.

**[0030]** Fig. 3 is a schematic describing a wiring layout in the pixel region. In the drawing, in order to simplify description, a wiring layout for six pixels disposed with the two rows and the three columns is shown. In the drawing, reference characters R, G, and B

denote the pixels 10 to emit light in red, green, and blue, respectively, and the RGB pixels are disposed in the column direction. Furthermore, reference character $V_{dd\text{-}R}$ denotes an electric line for a red pixel, $V_{dd\text{-}G}$ denotes an electric line for a green pixel, $V_{dd\text{-}B}$ denotes an electric line for a blue pixel, and 17 denotes a pixel electrode (anode) of an organic EL device. Detailed description regarding other components described above is omitted. Furthermore, reference numeral 31 denotes a line forming region in the form of a line which is formed between a pixel group of the (m-1) column and a pixel group of the m column, and is extending in the column direction over generally the same length as the pixel array length in the column direction. In the same way, reference numeral 32 denotes a line forming region formed between pixel groups of the m column and the (m + 1) column, 33 denotes a line forming region formed between pixel groups of the (m + 1) column and (m + 2) column, and 34 denotes a line forming region formed between pixel groups of the (m + 2) column and the (m + 3) column. For convenience of description, a pixel group of the (m - 1) column and a pixel group of the (m + 3) column are not shown in the drawing. With the present exemplary embodiment, in order to determine the line forming regions 31 through 34 with the width as same as possible, two or more lines, disposed on the aforementioned line forming regions, are determined with the same total width. While the electric power line $V_{dd}$ is formed with a width corresponding to a material of the emission layer of the organic EL device, now, for convenience of description, let us make an assumption that the width of the electric power lines increases in the order of green, red, and blue. That is to say, let us assume that the relation: width of $V_{dd\text{-}G}$ > width of $V_{dd\text{-}R}$ > width of $V_{dd\text{-}B}$, holds.

**[0031]** With the above-described assumption, in order to form the line forming regions 31 through 34 with the width as same as possible, a combination is determined such that the total width of the electric power line $V_{dd}$ and the data line $I_{dd}$ is approximately the same. For example, making an assumption that: the total width of $V_{dd\text{-}G}$ which has the maximal width and $V_{dd\text{-}B}$ of the minimal width; the total width of $V_{dd\text{-}R}$ of an intermediate width and the data line $I_{dat}$ of an intermediate width; and the total width of the two data lines $I_{dat}$; are determined to be generally the same value, the combinations of these electric power lines $V_{dd}$ and the data line $I_{dat}$ are formed in the line forming regions 31 through 34. With the arrangement shown in the drawing, a combination of $V_{dd\text{-}G}$ with the maximal width and $V_{dd\text{-}B}$ with the minimal width is formed on the line forming region 33, a combination of $V_{dd\text{-}R}$ with the intermediate width and the data line $I_{dat}$ with the intermediate width is formed in the line forming regions 31 and 34, and a combination of the two data lines $I_{dat}$ is formed on the line forming region 32. With the line forming region 31, only the electric power line $V_{dd\text{-}R}$ is

shown in the drawing, and with the line forming region 34, only the data line $I_{dat}$ is shown in the drawing. On the other hand, a scan line $V_{sel}$ is disposed on each line forming region in the form of a line, between pixel groups arrayed in the row direction, with generally the same length as the pixel array length of the pixel group. The wiring layout shown in the drawing corresponds to one unit of a periodically repeating wiring pattern, and any portion of the wiring layout of the RGB pixels 10 randomly selected has the same pattern as shown in the drawing. Accordingly, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other.

**[0032]** With the present exemplary embodiment, the same kind of electric power line, extending in the column direction of the pixel matrix, is formed with generally the same array pitch in the row direction, and accordingly, the pixels can be formed with the same pixel pitch, thereby facilitating design of a layout for a device, wherein power consumption is different for each color, such as an organic EL display. In particular, in the event of forming light-emission layers using the ink-jet method, the pixels are preferably formed with the same pixel pitch, and accordingly, an arrangement according to the present exemplary embodiment has the great advantage of facilitating the manufacturing process. Furthermore, with the present exemplary embodiment, the electric power line can be formed with a width suitable for each color, thereby reducing power consumption while maintaining the high aperture ratio and the optimal color balance.

**[0033]** The above-described arrangement is only an example of the present invention, and the present invention is not restricted to the above-described arrangement. For example, three combinations of two electric power lines selected from the three RGB lines $V_{dd}$ can be made, and accordingly, with the present exemplary embodiment, three wiring layout patterns can be made. Furthermore, while description has been made regarding a configuration where a scan line $V_{sel}$ is disposed on each line forming region in the row direction, and any two lines selected from the three electric power lines $V_{dd}$ and the three data line $I_{dat}$ are disposed on the line forming regions 31, 32, and 33 in the column direction, the present invention is not restricted to this arrangement. Description is made below regarding various exemplary modifications.

Second Exemplary Embodiment

**[0034]** Fig. 4 is a schematic describing a wiring layout according to a second exemplary embodiment of the present invention.

**[0035]** The present exemplary embodiment has a configuration wherein, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ make up a combination, and are disposed in the row direction on a line forming region 41 between the pixel group of the (n - 1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines $V_{sel}$ make up a combination, and are disposed in the row direction in a line forming region 42 between the pixel groups of the n row and the (n + 1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration where the combination of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the combination of the two scan lines $V_{sel}$ are disposed periodically and repeatedly. Accordingly, a line forming region 43 between the pixel groups of the (n + 1) row and the (n + 2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 41.

**[0036]** On the other hand, one electric power line $V_{dd}$ and one data line $I_{dat}$ make up a combination, and are disposed in the column direction and are disposed on a line forming region between pixel groups arranged in the column direction. With an arrangement shown in the drawing, the electric power line $V_{dd\text{-}R}$ and the data line $I_{dat}$ make up a combination, and are disposed on a line forming region 51 between the R-pixel group of the m column and the G-pixel group of the (m + 1) column, which are arrayed in the column direction. In the same way, the electric power line $V_{dd\text{-}G}$ and the data line $I_{dat}$ make up a combination, and are disposed on a line forming region between the G-pixel group of the (m + 1) column and the B-pixel group (not shown) of the (m + 2) column, which are arrayed in the column direction. Only the electric power line $V_{dd\text{-}G}$ is shown in the drawing for convenience of description. Furthermore, the electric power lines $V_{dd\text{-}R}$ disposed in the row and column directions are formed in different layers, and are electrically connected with each other through contact holes h1 formed in an inter-layer insulating film. The electric power lines $V_{dd\text{-}G}$ are electrically connected with each other through contact holes h2 in the same way.

**[0037]** With the present exemplary embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same array pitch, and accordingly, the present exemplary embodiment has the same advantages as with the first exemplary embodiment, and furthermore, the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, cross-talk can be reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present exemplary embodiment is particularly advantageous.

Third Exemplary Embodiment

**[0038]** Fig. 5 is a schematic describing a wiring layout according to a third exemplary embodiment of the present invention.

**[0039]** The present exemplary embodiment has a configuration where, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction and the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ make up a combination, and are disposed in the row direction on a line forming region 61 between the pixel group (not shown) of the (n - 1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines $V_{sel}$ make up a combination, and are disposed in the row direction in a line forming region 62 between the pixel groups of the n row and the (n + 1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration where the combination of the three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the combination of the two scan lines $V_{sel}$ are disposed periodically and repeatedly. Accordingly, a line forming region 63 between the pixel groups of the (n + 1) row and the (n + 2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 61.

**[0040]** On the other hand, three combinations of two lines selected from the three electric power lines $V_{dd\text{-}C}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the three data lines $I_{dat}$ are formed between

the pixel groups arrayed in the column direction. With an arrangement shown in the drawing, the electric power line (not shown) and the data line $I_{dat}$ make up a combination, and are disposed in a line forming region 71 between the B-pixel group (not shown) of the (m - 1) column and the R-pixel group of the m column, which are arrayed in the column direction, and the two electric power lines $V_{dd\text{-}G}$ and $V_{dd\text{-}R}$ make up a combination, and are disposed on a line forming region 72 between the R-pixel group of the m column and the G-pixel group of the (m + 1) column, which are arrayed in the column direction. Furthermore, the two data lines $I_{dat}$ make up a combination, and are disposed on a line forming region 73 between the G-pixel group of the (m + 1) column and the B-pixel group of (m + 2) column, which are arrayed in the column direction, and the electric power line $V_{dd\text{-}G}$ and the data line $I_{dat}$ make up a combination, and are formed on a line forming region 74 between the B-pixel group of the (m + 2) column and the R-pixel group (not shown) of the (m + 3) column, which are arrayed in the column direction.

**[0041]** The electric power lines disposed in the column and row directions are formed in different layers, and are electrically connected with each other through the contact holes h1 formed on an inter-layer insulating film. In the same way, the electric power lines $V_{dd\text{-}G}$ in the column and row directions, and the electric power lines $V_{dd\text{-}B}$ in the column and row directions, are formed in different layers, and the electric power lines in the column and row directions are electrically connected with each other through the contact holes h2 and h3. With the present exemplary embodiment, a plurality of each of the contact holes h1, h2, and h3 are formed, whereby the present exemplary embodiment has the advantage of reducing or preventing wiring breakage, and furthermore has the advantage of reducing the wiring resistance.

**[0042]** With the present exemplary embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same array pitch, the same kind of electric power line extending in the column direction of the pixel matrix is formed in the row direction with generally the same array pitch, and accordingly, the present exemplary embodiment has the same advantages as with the first exemplary embodiment, and furthermore, the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, the occurrence of cross-

talk can be reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present exemplary embodiment is particularly advantageous.

Fourth Exemplary Embodiment

**[0043]** Fig. 6(A) through Fig. 6(F) are schematics which illustrate examples of electronic apparatuses to which the electric-optical device according to the present invention can be applied. Fig. 6(A) shows an example of application to a cellular phone, where the cellular phone 230 includes an antenna unit 231, an audio output unit 232, an audio input unit 233, an operating unit 234, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 according to the present invention can be employed as a display unit of the cellular phone 230. Fig. 6(B) shows an application example to a video camera, where the video camera 240 includes a TV-camera unit 241, an operating unit 242, an audio input unit 243, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a viewfinder or a display unit. Fig. 6(C) shows an application example to a portable personal computer, where the computer 250 comprises a camera unit 251, an operation unit 252, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a display device.

**[0044]** Fig. 6(D) shows an application example to a head mount display, where the head mount display 260 includes a belt 261, an optical system storage unit 262, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as an image display unit. Fig. 6(E) shows an application example to a rear projector, where the projector 270 includes a casing 271, a light source 272, a synthesizing optical system 273, mirrors 274 and 275, a screen 276, and the organic EL display panel 100 according to the present invention. Fig. 6(F) shows an application example to a front projector, where the projector 280 comprises a casing 282, an optical system 281, and the organic EL display panel 100 according to the present invention, where an image can be displayed on a screen 283. As described above, the organic EL display panel 100 can be employed as an image display unit.

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# ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

## BACKGROUND OF THE INVENTION

1. Field of Invention

**[0001]** The present invention relates to a wiring layout suitable for an electro-optical device including electro-optical devices.

2. Description of Related Art

**[0002]** Organic EL devices are current-driven self-light-emitting devices, and accordingly, ~~there are an advantage of no need to~~ provide a backlight, ~~as well as~~ other advantages such as low power consumption, a wide range of vision, and a high contrast ratio, ~~so there is high expectation for development of~~ flat panel displays employing EL devices. The organic EL device is an electro-optical device including a light-emission layer introduced between an anode and a cathode, ~~wherein,~~ upon supplying forward bias current between both the electrodes, self-light-emission is effected due to the recombination energy at the time of recombination of a hole injected from the anode and an electron injected from the cathode. Accordingly, a supply of electric power from an external circuit is required in order to cause the organic EL device to emit light.

**[0003]** With ~~conventional~~ color-display active-matrix-driven display panels, an M number each of electric power lines and data lines are disposed in the column direction on a pixel matrix with an N number of columns and an M number of rows formed on a pixel region, as well as an N number of selection lines being disposed in the row direction on the aforementioned matrix. With a given pixel of such a wiring layout, a data line is disposed between the given pixel and the left-adjacent pixel, and an electric power line is disposed between the given pixel and the right-adjacent pixel. That is to say, with the lines disposed between adjacent pixels in the column direction, a layout is formed so that one data line and one electric line make up one pair. With the above-described configuration, disposed at an intersection of a scan line and a data line ~~are~~: a switching transistor, a holding capacitance, a driving transistor, and an organic EL device for emitting light in one color of the RGB three primary colors, and these devices make up a pixel.

## SUMMARY OF THE INVENTION

**[0004]** With the ~~conventional~~ arrangements, a light-emission layer is formed of a material corresponding to each color of the RGB three primary colors, and accordingly, the organic EL device is operated with greatly different power consumption corresponding to

each color, so the optimal width of the electric power line is greatly different for each color. Accordingly, with the above-described wiring layout, while there is the need to determine the pixel pitch according to the maximal width for disposing the electric power lines, there is the need to form a pixel matrix with the same pixel pitch due to the restriction from the manufacturing process for a display, and accordingly, there is the need to determine the pixel layout at the sacrifice of the aperture ratio. On the other hand, in the event of reducing the aperture ratio, there is the need to increase the amount of electric current supplied to the organic EL device for obtaining predetermined luminance, and accordingly, there is the need to form the electric power line with a greater width, leading to further reduction of the aperture ratio from the above-described reason.

**[0005]** As described above, with the ~~conventional~~ wiring layout, the width of the electric line and the aperture ratio of the pixel are in the relation of trade off each other, and it is difficult to maintain a large aperture ratio while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.

**[0006]** Accordingly, ~~it is an object of~~ the present invention to provide a wiring method for electric power lines, ~~wherein~~ the aperture ratio of the pixel can be increased while maintaining a pixel matrix with the same pixel pitch.

**[0007]** In order to solve the above ~~described problems~~, an electro-optical device according to the present invention ~~comprises~~ multiple pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from an electric power supply circuit, ~~wherein~~ the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, ~~and wherein~~ line forming regions are formed between adjacent pixel groups of the multiple pixel groups, ~~and wherein~~ the line forming regions are formed with generally the same width. With such a configuration, a the pixel pitch can be made the same.

**[0008]** Here, "electro-optical device" means a general electronic device for changing the optical state of light by using electric effects, and include, besides self-light-emitting devices such as electro-luminescence devices, electronic devices for displaying grayscale by adjusting the state of the polarized light, similarly to liquid crystal devices. With the present invention, the electro-luminescence devices are preferably employed. With the present invention, the electro-luminescence devices are employed, whereby current-driven self-light-emission devices can be obtained.

[0009] Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein at least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

[0010] Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein both at least one electric power line of the multiple electric power lines and at least one scan line of the multiple scan lines are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

[0011] Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein both at least one electric power line of the multiple electric power lines

and at least one data line of the multiple data lines are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with an enhanced or the optimal width.

**[0012]** The aforementioned line forming regions are preferably formed with generally the same width. With the present invention, the line forming regions are formed with generally the same width, whereby the pixel matrix can be formed with the same pixel pitch.

**[0013]** The aforementioned electro-optical device preferably includes electro-optical devices which are operated with different driving voltages, ~~wherein~~ the electric power lines for supplying voltage to the electro-optical devices are formed with different widths corresponding to the driving voltage. Even with such a configuration wherein the electric power lines are formed with different widths, the wiring layout is designed as described above, whereby the pixel matrix can be formed with the same pixel pitch while ~~improving~~ enhancing the aperture ratio.

**[0014]** The aforementioned electro-optical device preferably is a light-emission device, ~~wherein~~ the electric power lines are formed with each different width corresponding to the emission light color of the light-emission device. With the present invention, an enhanced or the optimal width of the electric power line is determined corresponding to the properties of the electro-optical device, thereby facilitating design of devices.

**[0015]** The color of the light which is to be emitted is preferably red, green, or blue. This enables full-color display.

**[0016]** The electro-optical device preferably is an electro-luminescence device. With the electro-luminescence device, the grayscale due to light emission can be controlled by current control.

**[0017]** An electronic apparatus according to the present invention ~~comprises~~ includes an electro-optical device according to the present invention. The electronic apparatus is not particularly restricted so long as it includes a display device, and can be applied to, for example, cellular phones, video cameras, personal computers, head mount displays, projectors, facsimiles, digital cameras, portable TVs, DSP devices, PDAs, palmtops, and the like.

**[0018]** A matrix substrate according to the present invention ~~comprises~~ includes multiple pixel electrodes disposed in the form of a matrix, ~~wherein~~ the multiple pixel electrodes make

up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, ~~and wherein~~ multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups, ~~and wherein~~ the line forming regions are formed with generally the same width. With such a configuration, the pixel pitch can be made the same.

**[0019]** Another matrix substrate according to the present invention ~~comprises~~ includes multiple scan lines, multiple data lines, multiple pixel electrodes disposed at portions corresponding to the intersections of the scan lines and the data lines, and multiple electric power lines ~~for~~ supplying voltage to the multiple pixel electrodes, ~~wherein~~ the multiple pixel electrodes make up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, ~~and wherein~~ multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups, ~~and wherein~~ at least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, the pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio, while forming the electric power lines with the optimal width.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** Fig. 1 is a plan view of an organic EL display panel according to the present invention;

**[0021]** Fig. 2 is a principal circuit configuration diagram of a pixel;

**[0022]** Fig. 3 is ~~an explanatory diagram for~~ describing a wiring layout according to a first embodiment;

**[0023]** Fig. 4 is ~~an explanatory diagram for~~ describing a wiring layout according to a second embodiment;

**[0024]** Fig. 5 is ~~an explanatory diagram for~~ describing a wiring layout according to a third embodiment;

**[0025]** Fig. 6~~(A)~~ through Fig. 6~~(F)~~ are ~~explanatory diagrams for~~ describing application examples employing the organic EL display according to the present invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

**[0026]** ~~The present~~ embodiment ~~will now be~~ described with reference to the drawings.

[0027] Fig. 1 is an overall configuration ~~diagram which illustrates~~ an active-matrix organic-EL display panel 100 according to the ~~present~~ embodiment. As shown in the drawing, the display panel 100 ~~comprises~~ a display region 11 including multiple pixels 10 disposed in the form of a matrix with an N number of columns and an M number of rows, a scan line driver 12 ~~for~~ outputting scan signals to scan lines arrayed in the row direction which are connected to a group of pixels 10, a data line driver 13 ~~for~~ supplying data signals and electric power to data lines and electric power lines arrayed in the column direction which are connected to a group of pixels 10, ~~wherein~~ these components are disposed on a substrate 16. An organic EL device is formed on each pixel 10 ~~for~~ emitting light in a color of the RGB three primary colors. A cathode 14 is formed in the form of a film as a common electrode on the entire face of the display region 11, and is connected to an external circuit through cathode output electrode 15.

[0028] ~~Note that~~ while the organic EL display panel 100 shown in the drawing is a so-called "top-emission configuration display panel" which emits light from the side of the substrate 16, the present invention is not restricted to this arrangement, but rather, the present invention can also be applied to a bottom-emission configuration display panel which emits light from a transparent cathode.

[0029] Fig. 2 is a principal circuit ~~configuration diagram~~ of the pixel 10. The pixel 10 ~~comprises~~ a switching transistor Tr1, a driving transistor Tr2, holding capacitance C, a light-emission portion OLED, and is driven with the dual transistor method. The switching transistor Tr1 ~~comprises~~ an n-channel FET, ~~wherein~~ the gate terminal thereof is connected to the scan line $V_{sel}$, and the drain terminal thereof is connected to the data line $I_{dat}$. The driving transistor Tr2 ~~comprises~~ a p-channel FET, ~~wherein~~ the gate terminal is connected to the source terminal of the switching transistor Tr1. Furthermore, the source terminal of the transistor Tr2 is connected to the electric power line $V_{dd}$, and the drain terminal thereof is connected to the light-emission portion OLED. Furthermore, holding capacitance is formed between the gate and the source of the transistor Tr2. With the above-described configuration, upon outputting a selection signal to the scan line $V_{sel}$, and opening the transistor Tr1, the data signals supplied through the data line $I_{dat}$ are written to the holding capacitance C as a voltage value. Subsequently, the holding voltage written to the holding capacitance C is held during one frame period, and the conductance of the driving transistor Tr2 is determined according to the holding voltage in an analog manner, whereby forward

bias current corresponding to light-emission level is supplied to the light-emission portion OLED.

**[0030]** Fig. 3 is a ~~diagram for~~ schematic describing a wiring layout in the pixel region. In the drawing, in order to simplify description, a wiring layout for six pixels disposed with the two rows and the three columns is shown. In the drawing, reference characters R, G, and B denote the pixels 10 ~~for~~ emitting light in red, green, and blue, respectively, and the RGB pixels are disposed in the column direction. Furthermore, reference character $V_{dd\text{-}R}$ denotes an electric line for a red pixel, $V_{dd\text{-}G}$ denotes an electric line for a green pixel, $V_{dd\text{-}B}$ denotes an electric line for a blue pixel, and 17 denotes a pixel electrode (anode) of an organic EL device. Detailed description regarding other components described above ~~will be~~ omitted. Furthermore, reference numeral 31 denotes a line forming region in the form of a line which is formed between a pixel group of the (m-1) column and a pixel group of the m column, and is extending in the column direction over generally the same length as the pixel array length in the column direction. In the same way, reference numeral 32 denotes a line forming region formed between pixel groups of the m column and the (m + 1) column, 33 denotes a line forming region formed between pixel groups of the (m + 1) column and (m + 2) column, and 34 denotes a line forming region formed between pixel groups of the (m + 2) column and the (m + 3) column. For convenience of description, a pixel group of the (m - 1) column and a pixel group of the (m + 3) column are not shown in the drawing. With the present exemplary embodiment, in order to determine the line forming regions 31 through 34 with the width as same as possible, two or more lines, disposed on the aforementioned line forming regions, are determined with the same total width. While the electric power line $V_{dd}$ is formed with a width corresponding to a material of the emission layer of the organic EL device, now, for convenience of description, let us make an assumption that the width of the electric power lines increases in the order of green, red, and blue. That is to say, let us assume that the relation: width of $V_{dd\text{-}G}$ > width of $V_{dd\text{-}R}$ > width of $V_{dd\text{-}B}$, holds.

**[0031]** With the above-described assumption, in order to form the line forming regions 31 through 34 with the width as same as possible, a combination is determined such that the total width of the electric power line $V_{dd}$ and the data line $I_{dd}$ is approximately the same. For example, making an assumption that: the total width of $V_{dd\text{-}G}$ which has the maximal width and $V_{dd\text{-}B}$ of the minimal width; the total width of $V_{dd\text{-}R}$ of an intermediate width and the data line $I_{dat}$ of an intermediate width; and the total width of the two data lines $I_{dat}$; are determined to be generally the same value, the combinations of these electric power lines $V_{dd}$ and the data line $I_{dat}$ are formed in the line forming regions 31 through 34. With the

arrangement shown in the drawing, a combination of $V_{dd-G}$ with the maximal width and $V_{dd-B}$ with the minimal width is formed on the line forming region 33, a combination of $V_{dd-R}$ with the intermediate width and the data line $I_{dat}$ with the intermediate width is formed in the line forming regions 31 and 34, and a combination of the two data lines $I_{dat}$ is formed on the line forming region 32. ~~Note that~~ with the line forming region 31, only the electric power line $V_{dd-R}$ is shown in the drawing, and with the line forming region 34, only the data line $I_{dat}$ is shown in the drawing. On the other hand, a scan line $V_{sel}$ is disposed on each line forming region in the form of a line, between pixel groups arrayed in the row direction, with generally the same length as the pixel array length of the pixel group. The wiring layout shown in the drawing corresponds to one unit of a periodically repeating wiring pattern, and any portion of the wiring layout of the RGB pixels 10 randomly selected has the same pattern as shown in the drawing. Accordingly, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other.

**[0032]** With the present exemplary embodiment, the same kind of electric power line, extending in the column direction of the pixel matrix, is formed with generally the same array pitch in the row direction, and accordingly, the pixels can be formed with the same pixel pitch, thereby facilitating design of a layout for a device, wherein power consumption is different for each color, such as an organic EL display. In particular, in the event of forming light-emission layers using the ink-jet method, the pixels are preferably formed with the same pixel pitch, and accordingly, an arrangement according to the present exemplary embodiment has the great advantage of facilitating the manufacturing process. Furthermore, with the present exemplary embodiment, the electric power line can be formed with a width suitable for each color, thereby reducing power consumption while maintaining the high aperture ratio and the optimal color balance.

**[0033]** ~~Note that~~ the above-described arrangement is only an example of the present invention, and the present invention is not restricted to the above-described arrangement. For example, three combinations of two electric power lines selected from the three RGB lines $V_{dd}$ can be made, and accordingly, with the present exemplary embodiment, three wiring layout patterns can be made. Furthermore, while description has been made regarding a configuration wherein a scan line $V_{sel}$ is disposed on each line forming region in the row direction, and any ~~two lines~~ selected from the three electric power lines $V_{dd}$ and the three data line $I_{dat}$ are disposed on the line forming regions 31, 32, and 33 in the column direction, the present

invention is not restricted to this arrangement. Description ~~will be~~ is made below regarding various modifications.

Second Embodiment

**[0034]** Fig. 4 is ~~an explanatory diagram for~~ a schematic describing a wiring layout according to a second embodiment of the present invention.

**[0035]** The present embodiment has a configuration wherein, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ make up a combination, and are disposed in the row direction on a line forming region 41 between the pixel group of the (n - 1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines $V_{sel}$ make up a combination, and are disposed in the row direction in a line forming region 42 between the pixel groups of the n row and the (n + 1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration wherein the combination of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the combination of the two scan lines $V_{sel}$ are disposed periodically and repeatedly. Accordingly, a line forming region 43 between the pixel groups of the (n + 1) row and the (n + 2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 41.

**[0036]** On the other hand, one electric power line $V_{dd}$ and one data line $I_{dat}$ make up a combination, and are disposed in the column direction and are disposed on a line forming region between pixel groups arranged in the column direction. With an arrangement shown in the drawing, the electric power line $V_{dd\text{-}R}$ and the data line $I_{dat}$ make up a combination, and are disposed on a line forming region 51 between the R-pixel group of the m column and the G-pixel group of the (m + 1) column, which are arrayed in the column direction. In the same way, the electric power line $V_{dd\text{-}G}$ and the data line $I_{dat}$ make up a combination, and are disposed on a line forming region between the G-pixel group of the (m + 1) column and the B-pixel group (not shown) of the (m + 2) column, which are arrayed in the column direction, wherein only the electric power line $V_{dd\text{-}G}$ is shown in the drawing for convenience of description. Furthermore, the electric power lines $V_{dd\text{-}R}$ disposed in the row and column directions are formed in different layers, and are electrically connected with each other

through contact holes h1 formed in an inter-layer insulating film. The electric power lines $V_{dd\text{-}G}$ are electrically connected with each other through contact holes h2 in the same way.

**[0037]** With the present embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same array pitch, and accordingly, the present embodiment has the same advantages as with the first embodiment, and furthermore, the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, cross-talk can be reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present embodiment is particularly advantageous.

Third Embodiment

**[0038]** Fig. 5 is ~~an explanatory diagram for~~ describing a wiring layout according to a third embodiment of the present invention.

**[0039]** The present embodiment has a configuration wherein, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction and the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ make up a combination, and are disposed in the row direction on a line forming region 61 between the pixel group (not shown) of the (n - 1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines $V_{sel}$ make up a combination, and are disposed in the row direction in a line forming region 62 between the pixel groups of the n row and the (n + 1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration wherein the combination of the three electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the combination of the two scan lines $V_{sel}$ are disposed periodically and repeatedly. Accordingly, a line forming region 63 between the pixel groups of the (n + 1) row and the (n + 2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 61.

**[0040]** On the other hand, three combinations of two lines selected from the three electric power lines $V_{dd\text{-}C}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$, and the three data lines $I_{dat}$ are formed between

the pixel groups arrayed in the column direction. With an arrangement shown in the drawing, the electric power line (not shown) and the data line $I_{dat}$ make up a combination, and are disposed in a line forming region 71 between the B-pixel group (not shown) of the (m - 1) column and the R-pixel group of the m column, which are arrayed in the column direction, and the two electric power lines $V_{dd\text{-}G}$ and $V_{dd\text{-}R}$ make up a combination, and are disposed on a line forming region 72 between the R-pixel group of the m column and the G-pixel group of the (m + 1) column, which are arrayed in the column direction. Furthermore, the two data lines $I_{dat}$ make up a combination, and are disposed on a line forming region 73 between the G-pixel group of the (m + 1) column and the B-pixel group of (m + 2) column, which are arrayed in the column direction, and the electric power line $V_{dd\text{-}G}$ and the data line $I_{dat}$ make up a combination, and are formed on a line forming region 74 between the B-pixel group of the (m + 2) column and the R-pixel group (not shown) of the (m + 3) column, which are arrayed in the column direction.

**[0041]** The electric power lines disposed in the column and row directions are formed in different layers, and are electrically connected with each other through the contact holes h1 formed on an inter-layer insulating film. In the same way, the electric power lines $V_{dd\text{-}G}$ in the column and row directions, and the electric power lines $V_{dd\text{-}B}$ in the column and row directions, are formed in different layers, and the electric power lines in the column and row directions are electrically connected with each other through the contact holes h2 and h3. With the present embodiment, a plurality of each of the contact holes h1, h2, and h3 are formed, whereby the present embodiment has the advantage of preventing wiring breakage, and furthermore has the advantage of reducing the wiring resistance.

**[0042]** With the present embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same array pitch, the same kind of electric power line extending in the column direction of the pixel matrix is formed in the row direction with generally the same array pitch, and accordingly, the present embodiment has the same advantages as with the first embodiment, and furthermore, the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines $V_{dd\text{-}G}$, $V_{dd\text{-}R}$, and $V_{dd\text{-}B}$ can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, the occurrence of cross-talk can be

reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present embodiment is particularly advantageous.

Fourth Embodiment

**[0043]** Fig. 6(A) through Fig. 6(F) are ~~diagrams~~ which illustrate examples of electronic apparatuses to which the electric-optical device according to the present invention can be applied. Fig. 6(A) shows an example of application to a cellular phone, wherein the cellular phone 230 ~~comprises~~ includes an antenna unit 231, an audio output unit 232, an audio input unit 233, an operating unit 234, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 according to the present invention can be employed as a display unit of the cellular phone 230. Fig. 6(B) shows an application example to a video camera, wherein the video camera 240 ~~comprises~~ includes a TV-camera unit 241, an operating unit 242, an audio input unit 243, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a viewfinder or a display unit. Fig. 6(C) shows an application example to a portable personal computer, wherein the computer 250 comprises a camera unit 251, an operation unit 252, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a display device.

**[0044]** Fig. 6(D) shows an application example to a head mount display, wherein the head mount display 260 ~~comprises~~ includes a belt 261, an optical system storage unit 262, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as an image display unit. Fig. 6(E) shows an application example to a rear projector, wherein the projector 270 ~~comprises~~ includes a casing 271, a light source 272, a synthesizing optical system 273, mirrors 274 and 275, a screen 276, and the organic EL display panel 100 according to the present invention. Fig. 6(F) shows an application example to a front projector, wherein the projector 280 comprises a casing 282, an optical system 281, and the organic EL display panel 100 according to the present invention, wherein an image can be displayed on a screen 283. As described above, the organic EL display panel 100 can be employed as an image display unit.

| TRANSMITTAL FORM *(to be used for all correspondence after initial filing)* | | Application Number | 10/676,067 |
|---|---|---|---|
| | | Filing Date | September 30, 2003 |
| | | First Named Inventor | Hao Pan, et. al. |
| | | Group Art Unit | |
| | | Examiner Name | |
| Total Number of Pages in this Submission | | Attorney Docket Number | KLR:7146.0167 |

PTO/SB/21 JC42 Rec'd PCT/PTO 10 NOV 2003 PATENT & TRADEMARK OFFICE

| ENCLOSURES (check all that apply) | | |
|---|---|---|
| ☐ Fee transmittal<br>☐ Fee attached form | ☐ Assignment Papers (for an application) | ☐ After Allowance Communication to Group |
| ☐ Amendment<br>☐ After Final/ Response | ☐ Drawing(s) | ☐ Appeal Communication to Board of Appeals and Interferences |
| ☐ Affidavits/Declaration(s) | ☐ Licensing Related Papers | ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) |
| ☐ Extension of Time Request | ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition | ☐ Proprietary Information |
| ☐ Express Abandonment Request | ☐ Petition to Convert to a Provisional Application | ☐ Status Letter |
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| ☐ Response to Missing Parts Under 37 CFR 1.52 or 1.53 | ☐ Request for Refund | |
| | Remarks: ***Commissioner is authorized to charge any additional fee, or credit any overpayment, to Deposit Account No. 03-1550. A duplicate copy of this Transmittal Form is enclosed for purposes of use with Deposit Account No. 03-1550 as stated herein.*** | |

| SIGNATURE OF APPLICANT, ATTORNEY OR AGENT | |
|---|---|
| Firm or Individual Name | Kevin L. Russell of CHERNOFF, VILHAUER, Mc CLUNG & STENZEL, LLP |
| Signature | |
| Date | November 7 2003 |

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November 7, 2003 (3:36PM)

PTO/SB/06 (08-03)
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## PATENT APPLICATION FEE DETERMINATION RECORD
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Application or Docket Number: 10016069

### CLAIMS AS FILED – PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY RATE | SMALL ENTITY FEE | OR | OTHER THAN SMALL ENTITY RATE | OTHER THAN SMALL ENTITY FEE |
|---|---|---|---|---|---|---|---|
| BASIC FEE (37 CFR 1.16(a)) | | | | $____ | OR | | $770 |
| TOTAL CLAIMS (37 CFR 1.16(c)) | 12 minus 20 = | * | X $____ = | | OR | X $18 = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(b)) | 6 minus 3 = | * 3 | X $____ = | | OR | X $86 = | 258 |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d)) | | | + $____ = | | OR | + $____ = | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | OR | TOTAL | 1028 |

### CLAIMS AS AMENDED – PART II

AMENDMENT A

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE | SMALL ENTITY ADDITIONAL FEE | OR | OTHER THAN SMALL ENTITY RATE | OTHER THAN SMALL ENTITY ADDITIONAL FEE |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(c)) | * 12 | Minus | ** 20 | = 1 | X $____ = | | OR | X $____ = | |
| Independent (37 CFR 1.16(b)) | * 6 | Minus | *** 6 | = | X $____ = | | OR | X $____ = | 0 |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d)) | | | | | + $____ = | | OR | + $____ = | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

AMENDMENT B

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE | SMALL ENTITY ADDITIONAL FEE | OR | OTHER THAN SMALL ENTITY RATE | OTHER THAN SMALL ENTITY ADDITIONAL FEE |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(c)) | * | Minus | ** | = | X $____ = | | OR | X $____ = | |
| Independent (37 CFR 1.16(b)) | * | Minus | *** | = | X $____ = | | OR | X $____ = | |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d)) | | | | | + $____ = | | OR | + $____ = | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

AMENDMENT C

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE | SMALL ENTITY ADDITIONAL FEE | OR | OTHER THAN SMALL ENTITY RATE | OTHER THAN SMALL ENTITY ADDITIONAL FEE |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(c)) | * | Minus | ** | = | X $____ = | | OR | X $____ = | |
| Independent (37 CFR 1.16(b)) | * | Minus | *** | = | X $____ = | | OR | X $____ = | |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d)) | | | | | + $____ = | | OR | + $____ = | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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| APPLICATION NUMBER | FILING OR 371 (c) DATE | FIRST NAMED APPLICANT | ATTORNEY DOCKET NUMBER |
|---|---|---|---|
| 10/676,067 | 10/02/2003 | Yojiro Matsueda | 117390 |

**CONFIRMATION NO. 7780**

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

**FORMALITIES LETTER**

*OC000000011750477*

Date Mailed: 01/26/2004

## NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

**FILED UNDER 37 CFR 1.53(b)**

***Filing Date Granted***

**Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

**SUMMARY OF FEES DUE:**

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

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| APPL NO. | FILING OR 371 (c) DATE | ART UNIT | FIL FEE REC'D | ATTY.DOCKET NO | DRAWINGS | TOT CLMS | IND CLMS |
|---|---|---|---|---|---|---|---|
| 10/676,067 | 10/02/2003 | 2673 | 1028 | 117390 | 5 | 12 | 6 |

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Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

**Applicant(s)**

Yojiro Matsueda, Chino-shi, ~~Suwa-shi~~, JAPAN;
Hayato Nakanishi, ~~Suwa-shi~~ Toyama-shi, JAPAN;

**Assignment For Published Patent Application**

SEIKO EPSON CORPORATION, Tokyo, JAPAN;

**Domestic Priority data as claimed by applicant**

**Foreign Applications**

JAPAN 2002-293696 10/07/2002

**If Required, Foreign Filing License Granted:** 01/22/2004

**Projected Publication Date:** To Be Determined - pending completion of Missing Parts

**Non-Publication Request:** No

**Early Publication Request:** No

**Title**

Electro-optical device, matrix substrate, and electronic apparatus

OIPE JC59
FEB 06 2004
PATENT & TRADEMARK OFFICE

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Attn: OIPE

Yojiro MATSUEDA et al.

Application No.: 10/676,067

Docket No.: 117390

Filed: October 2, 2003

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

**REQUEST FOR CORRECTION OF PALM RECORDS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is a photocopy of the original filing receipt on which errors have been corrected in red. These errors are being brought to the attention of the Patent and Trademark Office so that it may correct its records. A Supplemental Application Data Sheet is attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Date: February 6, 2004

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

FEB 0 6 2004
PATENT & TRADEMARK OFFICE

OLIFF & BERRIDGE, PLC
ATTORNEYS AT LAW

## Supplemental Application Data Sheet

### Application Information

| | |
|---|---|
| Application Type:: | **Regular** |
| Subject Matter:: | **Utility** |
| CD-ROM or CD-R: | **None** |
| Title:: | **ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS** |
| Attorney Docket Number:: | **117390** |
| Total Drawing Sheets:: | **5** |
| Small Entity:: | **No** |

### Applicant Information

| | |
|---|---|
| Applicant Authority type:: | **Inventor** |
| Primary Citizenship Country:: | **Japan** |
| Status:: | **Full Capacity** |
| Given Name:: | **Yojiro** |
| Family Name:: | **MATSUEDA** |
| City of Residence:: | **Chino-shi** |
| State or Province of Residence:: | **Nagano-ken** |
| Country of Residence:: | **JAPAN** |

| | |
|---|---|
| Applicant Authority type:: | **Inventor** |
| Primary Citizenship Country:: | **Japan** |
| Status:: | **Full Capacity** |
| Given Name:: | **Hayato** |
| Family Name:: | **NAKANISHI** |
| City of Residence:: | **Toyama-shi** |
| State or Province of Residence:: | **Toyama-ken** |
| Country of Residence:: | **JAPAN** |

**Correspondence Information**

Correspondence Customer Number:: **25944**

| **Foreign Priority Information** | | | |
|---|---|---|---|
| | | | |
| Country:: | Application Number:: | Filing Date:: | Priority Claimed:: |
| | | | |
| **JAPAN** | **2002-293696** | **10/07/2002** | **Yes** |
| | | | |

| **Assignee Information** | |
|---|---|
| | |
| Assignee Name:: | **Seiko Epson Corporation** |
| Street of mailing address:: | **4-1, Nishi-shinjuku 2-chome, Shinjuku-ku** |
| City of mailing address:: | **Tokyo** |
| Country of mailing address:: | **JAPAN** |
| Postal or Zip Code of mailing address:: | **163-0811** |

OIPE JC59
FEB 0 6 2004
PATENT & TRADEMARK OFFICE

PTO/SB/106 (8-96)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Seiko Epson Ref. No.: F008847US00 | Attorney's Ref. No.: 117390

# Declaration and Power of Attorney For Patent Application

## 特許出願宣言書及び委任状

## Japanese Language Declaration

## 日本語宣言書

| | |
|---|---|
| 下記の氏名の発明者として、私は以下の通り宣言します。 | As a below named inventor, I hereby declare that: |
| 私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。 | My residence, post office address and citizenship are as stated next to my name. |
| 下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。 | I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled |
| 電気光学装置、マトリクス基板、及び電子機器 | ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS |
| 上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、 | the specification of which is attached hereto unless the following box is checked: |
| ☒ 2003年10月2日に提出され、米国出願番号または特許協定条約 国際出願番号を 10/676,067 とし、（該当する場合） _____ に訂正されました。 | ☒ was filed on October 2, 2003 as United States Application Number or PCT International Application Number 10/676,067 and was amended on _____ (if applicable). |
| 私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。 | I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. |
| 私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。 | I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. |



Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office. Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks, Washington, DC 20231.

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# Japanese Language Declaration
## (日本語宣言書)

私は、米国法典第３５編１１９条（ａ）-（ｄ）項又は３６５条（ｂ）項に基き下記の、米国以外の国の少なくとも１ヶ国を指定している特許協力条約３６５条（ａ）項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

| (Number) (番号) | (Country) (国名) | (Day/Month/Year Filed) (出願年月日) | |
|---|---|---|---|
| 2002-293696 | Japan | 07/October/2002 | ☐ |
| | | | ☐ |

私は、第３５編米国法典１１９条（ｅ）項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

| (Application No.) (出願番号) | (Filing Date) (出願日) | (Application No.) (出願番号) | (Filing Date) (出願日) |
|---|---|---|---|
| | | | |

私は下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条（ｃ）に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１章５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

| (Application No.) (出願番号) | (Filing Date) (出願日) | (Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済) |
|---|---|---|
| | | |
| | | |

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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# Japanese Language Declaration
## (日本語宣言書)

委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

書類送付先：
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Alexandria, Virginia 22320

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唯一または第一発明者名
松枝 洋二郎 Y.M. Oct. 29, 2003

Full name of sole or first inventor
Yojiro MATSUEDA

発明者の署名 日付 10月29日
松枝洋二郎 2003年~~11月29日~~

Inventor's signature Date
Yojiro Matsueda ~~Nov. 29~~ Oct. 29, 2003

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Residence
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国籍
日本

Citizenship
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中西 早人

Full name of second joint inventor, if any
Hayato NAKANISHI

第二共同発明者の署名 日付
中西 早人 2003年11月15日

Second inventor's signature Date
Hayato NAKANISHI Nov. 15, 2003

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Post Office Address
c/o Seiko Epson Corporation
3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502 Japan

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)




IPW

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al.

Group Art Unit: 2674

Application No.: 10/676,067

Examiner: Patrick Edouard

Filed: October 2, 2003

Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

**STATUS INQUIRY LETTER**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please telephone Eric D. Morehouse at 703-836-6400 with the status of the above-identified patent application, including an indication as to when the next communication can be expected.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Date: April 4, 2005

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

OIPE IAP13 JAN 27 2006 PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al.

Group Art Unit: 2674

Application No.: 10/676,067

Examiner: P. EDOUARD

Filed: October 2, 2003

Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Kurt P. Goudy
Registration No. 52,954

JAO:KPG/tbm

Date: January 27, 2006

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

DEPOSIT ACCOUNT USE AUTHORIZATION
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OIPE IAP13
JAN 27 2006
PATENT & TRADEMARK OFFICE



| Form PTO-1449 (REV. 1/06) | US Dept. of Commerce PATENT & TRADEMARK OFFICE | ATTY DOCKET NO. 117390 | APPLICATION NO. 10/676,067 |
|---|---|---|---|
| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | | APPLICANT(S) Yojiro MATSUEDA et al. | |
| | | FILING DATE October 2, 2003 | GROUP 2674 |

U.S. PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Name |
|---|---|---|---|---|
| | 1 | US 2002/0140644 A1 | 10-3-2002 | Sato et al. |
| | 2 | US 5,159,476 | 10-27-1992 | Hayashi |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

FOREIGN PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Country | With English Abstract | With English Translation |
|---|---|---|---|---|---|---|
| | | | | | | |
| | | | | | | |
| | | | | | | |
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| | | | | | | |

OTHER DOCUMENTS

| Examiner Initials | Cite No. | (Including Author, Title, Date, Pertinent Pages, etc.) |
|---|---|---|
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

| EXAMINER | DATE CONSIDERED |
|---|---|

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 27, 2006

# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S1 | 1529149 | (electro$1optic$3 electrooptical LED OLED EL ELD OEL OELD) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/21 08:03 |
| S2 | 842147 | (scan$4 select$4 gate$1 address$4) near3 (line$1 electr$4) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/20 08:04 |
| S3 | 662615 | (data signal) near3 line$1 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/20 08:04 |
| S4 | 352331 | (power voltage) near3 line$1 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/20 08:05 |
| S5 | 16433 | S1 and S2 and S3 and S4 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/20 08:05 |
| S6 | 2862 | 315/169.3,169.2.ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/20 08:05 |
| S7 | 611 | S5 and S6 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/20 10:45 |
| S10 | 328 | S7 and width | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/20 09:40 |
| S41 | 473029 | (power voltage current electric) near3 line | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/21 15:05 |
| S42 | 2541 | S41 with width with (differen$3 sam$1 decreas$4 increas$4 $2equal $3similar vary$3 vari$3 alter$3) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/21 15:08 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| S43 | 38 | S20 and S42 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/11/21 15:39 |

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/676,067 | 10/02/2003 | Yojiro Matsueda | 117390 | 7780 |

25944 7590 12/01/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

| EXAMINER | |
|---|---|
| DUONG, DIEU HIEN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2821 | |

DATE MAILED: 12/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | Dieu Hien T. Duong | 2821 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ~~*11/10/03*~~*01/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

The Preliminary Amendment filed November 10, 2003 is acknowledged.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al (US 6,825,820).

Regarding claim 1, Figures 14A and 14B of Yamazaki disclose an electro-optical device comprising an electric power supply circuit 904; and a plurality of pixels 906 disposed in the form of a matrix including electro-optical devices driven by receiving electric power from the electric power supply circuit; the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and line forming regions 914r, 912g, 913 being formed between adjacent pixel groups of the plurality of pixel groups, and line forming regions being formed with generally the same width.

Regarding claim 2, Figures 14A and 14B of Yamazaki disclose an electro-optical device comprising a plurality of scan lines 913; a plurality of data lines 914r, 912g, 912b;

a plurality of pixels 906, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and a plurality of electric power lines 914r, 914g, 914b to supply driving voltage to the electro-optical devices; the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions 914r, 912g being formed between adjacent pixel groups of said plurality of groups, and at least two lines selected from at least one electric power line 914r of the plurality of electric power lines, at least one scan line 913 of the plurality of scan lines, and at least one data line 912g of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions.

Claims 3-4 are rejected for similar subject matter to claim 2.

Regarding claim 5, as applied to claim 2, Figure 14A and 14B of Yamazaki disclose the line forming regions being formed with generally the same width.

Regarding claim 6, as applied to claim 1, Figure 1B and page 6, lines 5-15 of Yamazaki discloses the electro-optical devices being operated with each different driving voltages; and the electric power lines to supply voltage to the electro-optical devices being formed with different widths corresponding to the driving voltage.

Regarding claim 7, as applied to claim 6, Figure 1B of Yamazaki discloses the electro-optical device being a light-emission device; and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

Regarding claim 8, as applied to claim 7, Figure 1B of Yamazaki discloses the color of the light which is to be emitted being at least one of red, green, and blue.

Regarding claim 9, as applied to claim 1, Yamazaki (col. 23, lines 21-35) discloses the electro-optical device being an electro-luminescence device.

Regarding claim 10, as applied to claim 1, Figure 12 of Yamazaki discloses an electronic apparatus comprising the electro-optical device according to claim 1.

Regarding claim 11, Figures 14A and 14B of Yamazaki disclose a matrix substrate comprising a plurality of pixel electrodes 906 disposed in the form of a matrix, the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, and a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups and the line forming regions being formed with generally the same width.

Regarding claim 12, Figures 14A and 14B of Yamazaki disclose a matrix substrate comprising a plurality of scan lines 913; a plurality of data lines 914r, 912g, 912b; a plurality of pixel electrodes 906 disposed at portions corresponding to intersections of the scan lines and the data lines; and a plurality of electric power lines 914r, 914g, 914b to supply voltage to the plurality of pixel electrodes; the plurality of pixel electrodes make-making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions are formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and at least two lines selected from at

least one electric power line 914r of the plurality of electric power lines, at least one scan line 913 of the plurality of scan lines, and at least one data line 912g of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions.

***Conclusion***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu Hien T. Duong whose telephone number is 571-272-8980. The examiner can normally be reached on Monday - Friday, from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit 2821
DD

HOANG V. NGUYEN
PRIMARY EXAMINER

| Notice of References Cited | Application/Control No. 10/676,067 | Applicant(s)/Patent Under Reexamination MATSUEDA ET AL. | |
|---|---|---|---|
| | Examiner Dieu Hien T. Duong | Art Unit 2821 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| * | A | US-6,825,820 | 11-2004 | Yamazaki et al. | 345/76 |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

OIPE IAP13 JAN 27 2006 PATENT & TRADEMARK OFFICE



| Form PTO-1449 (REV. 1/06) | US Dept. of Commerce PATENT & TRADEMARK OFFICE | ATTY DOCKET NO. 117390 | APPLICATION NO. 10/676,067 |
|---|---|---|---|
| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | | APPLICANT(S) Yojiro MATSUEDA et al. | |
| | | FILING DATE October 2, 2003 | GROUP ~~2674~~ 2821 |

U.S. PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Name |
|---|---|---|---|---|
| DD | 1 | US 2002/0140644 A1 | 10-3-2002 | Sato et al. |
| DD | 2 | US 5,159,476 | 10-27-1992 | Hayashi |
| | | | | |
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FOREIGN PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Country | With English Abstract | With English Translation |
|---|---|---|---|---|---|---|
| | | | | | | |
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OTHER DOCUMENTS

| Examiner Initials | Cite No. | (Including Author, Title, Date, Pertinent Pages, etc.) |
|---|---|---|
| | | |
| | | |
| | | |
| | | |

| EXAMINER | /Dieu Duong/ | DATE CONSIDERED 11/26/2006 |
|---|---|---|

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 27, 2006

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | Examiner | Art Unit |
| | Duong, Dieu Hien T | 2821 |

| SEARCHED | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| 315 | 169.2,169.3 | 11/20/06 | dd |

| SEARCH NOTES | | |
|---|---|---|
| Search Notes | Date | Examiner |
| Please See East Search History | 11/20/06 | dd |

| INTERFERENCE SEARCH | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| | | | |

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | Examiner | Art Unit |
| | Duong, Dieu Hien T | 2821 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 11/26/2006 | | | | | | | | |
| | 1 | ✓ | | | | | | | | |
| | 2 | ✓ | | | | | | | | |
| | 3 | ✓ | | | | | | | | |
| | 4 | ✓ | | | | | | | | |
| | 5 | ✓ | | | | | | | | |
| | 6 | ✓ | | | | | | | | |
| | 7 | ✓ | | | | | | | | |
| | 8 | ✓ | | | | | | | | |
| | 9 | ✓ | | | | | | | | |
| | 10 | ✓ | | | | | | | | |
| | 11 | ✓ | | | | | | | | |
| | 12 | ✓ | | | | | | | | |

| Interview Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | Dieu Hien T. Duong | 2821 | |

All participants (applicant, applicant's representative, PTO personnel):

(1) *Dieu Hien T. Duong*. (3) *John Radi*.

(2) *Thuy Tran*. (4)_____.

Date of Interview: *02/07/07*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☐ No.
If Yes, brief description: _____.

Claim(s) discussed: *1*.

Identification of prior art discussed: *6,825,820 B2*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *The proposed claim 1 was discussed. Both examiner and attorney agreed to make clear about the formation of the line regions in the display device. The proposed claim overcomes 102 rejection but not 103(a). A further addition of new limitation for a proper characterization of claim invention is suggested by examiner*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

OIPE IAP17 FEB 15 2007 PATENT & TRADEMARK OFFICE

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al. Group Art Unit: 2821

Application No.: 10/676,067 Examiner: D. DUONG

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

**AMENDMENT UNDER 37 C.F.R. §1.111**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the December 1, 2006 Office Action and the February 7, 2007 personal interview, please consider the following:

**Amendments to the Claims** as reflected in the listing of claims; and

**Remarks**.

**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device, comprising:

an electric power supply circuit; ~~and~~

a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit, the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and the line forming regions being formed with generally the same width; and

a combination being determined such that a sum of widths of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

2. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and at least two lines selected from at least one electric power line of the

plurality of electric power lines, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and

a combination being determined such that a sum of widths of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

3. (Previously Presented) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and both at least one electric power line of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions.

4. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and both at least one electric power line of the plurality of electric power lines and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions; and

a combination being determined such that a sum of widths of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

5. (Previously Presented) The electro-optical device according to Claim 2, the line forming regions being formed with generally the same width.

6. (Previously Presented) The electro-optical device according to Claim 1, the electro-optical devices being operated with each different driving voltages;

and the electric power lines to supply voltage to the electro-optical devices being formed with different widths corresponding to said driving voltage.

7. (Previously Presented) The electro-optical device according to Claim 6, the electro-optical device being a light-emission device;

and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

8. (Previously Presented) The electro-optical device according to Claim 7, the color of the light which is to be emitted being at least one of red, green, and blue.

9. (Previously Presented) The electro-optical device according to Claim 1, the electro-optical device being an electro-luminescence device.

10. (Previously Presented) An electronic apparatus, comprising:

the electro-optical device according to Claim 1.

11. (Currently Amended) A matrix substrate, comprising:

a plurality of pixel electrodes disposed in the form of a matrix, the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and the line forming regions being formed with generally the same width; and

a combination being determined such that a sum of widths of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

12. (Currently Amended) A matrix substrate, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel electrodes disposed at portions corresponding to intersections of the scan lines and the data lines; ~~and~~

a plurality of electric power lines to supply voltage to the plurality of pixel electrodes;

the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and at least two lines selected from at least one electric power line of the plurality of electric power lines, at least one scan line of

the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and

a combination being determined such that the sum of the widths of a plurality of lines formed in one line forming region is approximately the same as that of the sum of the widths of a plurality of lines formed in another line forming region.

13. (New) The electro-optical device according to claim 1, each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pitch.

14. (New) The electro-optical device according to claim 1, the combination of the plurality of lines being disposed periodically and repeatedly in at least one direction of the row direction and the column direction.

## REMARKS

Claims 1-14 are pending in this application. By this Amendment, claims 1, 2, 4, 11 and 12 are amended, and claims 13 and 14 are added. Support for amended claims 1, 2, 4, 11 and 12 and new claims 13 and 14 can be found, for example, in Fig. 3 and paragraphs [0030], [0031], and [0037].

The courtesies extended to Applicants representative by Examiners Duong and Tran at the interview held February 7, 2007, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicants' record of the interview.

Claims 1-12 were rejected under 35 U.S.C. §102(e) over Yamazaki et al (U.S. Patent No. 6,825,820). The rejection is respectfully traversed.

With respect to claim 1 and for similarly recited features in claims 2, 4, 11 and 12, and as agreed during the personal interview, Fig. 14B of Yamazaki only discloses a schematic view of the wiring diagram without a disclosure as to the relative widths of the lines in any of the line forming regions. Thus, Yamazaki does not teach nor make it possible to infer that the sum of the widths of a plurality of lines formed in one line forming region is approximately the same as the sum of the widths of a plurality of lines formed in another line forming region.

With respect to claim 3, Yamazaki does not teach at least one power line and at least one scan line being formed in at least one line forming region of the plurality of line forming regions.

As can be seen in Fig. 14B of Yamazaki, Yamazaki teaches power lines (power source feed lines 914) and data lines (source signal lines 912) being formed in the vertical line feeding regions and only scan lines (source signal lines 913) being formed in the horizontal line feeding regions. Therefore, because the scan lines run perpendicular to the power lines,

Yamazaki does not teach at least one power line and at least one scan line being formed in at least one line forming region of the plurality of line forming regions, as recited in claim 3.

Applicants respectfully request the rejection be withdrawn.

The Examiner should note, as discussed in the specification, for example at paragraphs [0030] to [0033], and in particular at the end of paragraph [0033], the voltage requirements of pixels of different colors are not the same. Thus, because the voltage requirements of differing colored pixels are different, the width of the voltage lines to pixels of different colors is varied accordingly. Therefore, it would not have been obvious to one skilled in the art to ensure that the sum of the widths of a plurality of lines formed in one line forming region is approximately the same as the sum of the widths of a plurality of lines formed in another line forming region, as recited in amended claims 1, 2, 4, 11 and 12.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

John A. Radi
Registration No. 59,345

JAO:JAR/tbm

Date: February 15, 2007

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

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Charge any fee due to our Deposit Account No. 15-0461

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

| Application or Docket Number | Filing Date | ☐ To be Mailed |
|---|---|---|
| 10/676,067 | 10/02/2003 | |

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| | | (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 02/15/2007 | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| AMENDMENT | Total (37 CFR 1.16(i)) | * 14 | Minus | ** 20 | = 0 | X $ = | | OR | X $50= | 0 |
| | Independent (37 CFR 1.16(h)) | * 6 | Minus | ***6 | = 0 | X $ = | | OR | X $200= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

| | | (Column 1) | | (Column 2) | (Column 3) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| AMENDMENT | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

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Legal Instrument Examiner:
Rosalind Ball

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al.

Group Art Unit: 2821

Application No.: 10/676,067

Examiner: D. DUONG

Filed: October 2, 2003

Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☒ 2. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

☒ 3. An English language Abstract of one or more non-English language reference is attached hereto. See References 2 and 3.

☒ 4. A computer-generated English language translation of one or more Japanese Patent Publication cited herein has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See References 2 and 3.

☒ 5. Reference 1 corresponds to reference 4.

Respectfully submitted,

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Date: March 19, 2007

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| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | | APPLICANTS Yojiro MATSUEDA et al. | |
| | | FILING DATE October 2, 2003 | GROUP 2821 |

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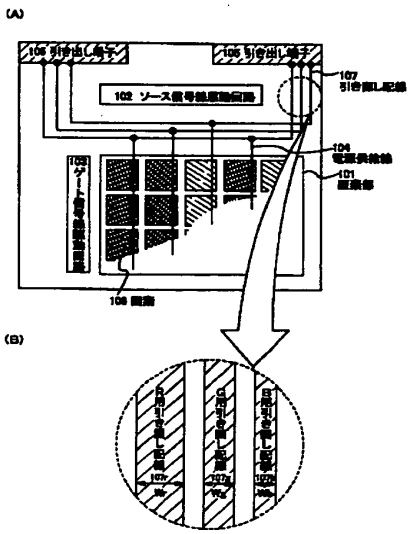
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最終頁に続く

(54)【発明の名称】　表示装置及び電子機器

(57)【要約】
【課題】　ＥＬ素子の色のバランスが良く、なおかつ発光輝度のバランスが良い、色鮮やかな画像を表示することが可能な表示装置を提供する。
【解決手段】　ＥＬ素子に流す電流を大きくしたい画素ほど、該画素のＥＬ素子に電圧または電流を供給する引き回し配線の幅を大きくした。これによって、ＥＬ素子に流す電流を大きくしたい画素ほど、該画素のＥＬ素子に電圧または電流を供給する引き回し配線の配線抵抗が小さくなる。配線抵抗が小さくなると、引き回し配線における電位降下が小さくなり、ＥＬ素子に流す電流を大きくすることが可能になる。なお実際のパネルでは、引き回し配線を配置するスペースは限られているので、各色における引き回し配線の幅の比を変えることで、各色のＥＬ素子に流れる電流の大きさのバランスを取ることが可能である。



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【特許請求の範囲】

【請求項１】複数のＥＬ素子と、複数の電源供給線と、複数の引き回し配線と、外部接続端子とを有する表示装置であって、

前記外部接続端子と前記複数の電源供給線とは前記複数の引き回し配線を介して電気的に接続されており、

前記複数の電源供給線は、前記複数のＥＬ素子が有する画素電極に電気的に接続されており、

前記複数のＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記複数の電源供給線にそれぞれ接続されている前記複数の引き回し配線の幅が大きいことを特徴とする表示装置。

【請求項２】請求項１において、前記複数のＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記複数の電源供給線の幅が大きいことを特徴とする表示装置。

【請求項３】複数の画素と、複数の電源供給線と、複数の引き回し配線と、外部接続端子とを有する表示装置であって、

前記複数の画素は、前記複数の電源供給線のいずれか１つと、ＥＬ素子と、スイッチング用ＴＦＴと、ＥＬ駆動用ＴＦＴとを有しており、

前記スイッチング用ＴＦＴは前記ＥＬ駆動用ＴＦＴのスイッチングを制御しており、

前記ＥＬ駆動用ＴＦＴによって、前記複数の電源供給線のいずれか１つの電位が、前記ＥＬ素子が有する画素電極に与えられ、

前記外部接続端子と前記複数の電源供給線とは前記複数の引き回し配線を介して電気的に接続されており、

前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記複数の電源供給線にそれぞれ接続されている前記複数の引き回し配線の幅が大きいことを特徴とする表示装置。

【請求項４】請求項３において、前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記ＥＬ駆動用ＴＦＴが有するチャネル形成領域のチャネル幅が大きいことを特徴とする表示装置。

【請求項５】請求項３または請求項４において、前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記ＥＬ駆動用ＴＦＴが有するＬＤＤ領域の長さが長いことを特徴とする表示装置。

【請求項６】請求項３乃至請求項５のいずれか１項において、前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記複数の電源供給線の幅が大きいことを特徴とする表示装置。

【請求項７】複数のＥＬ素子と、複数の電源供給線と、複数の引き回し配線と、外部接続端子とを有する表示装置であって、

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前記複数のＥＬ素子は画素電極と、対向電極と、前記画素電極と前記対向電極の間に設けられたＥＬ層とをそれぞれ有し、

前記外部接続端子と前記複数の電源供給線とは前記複数の引き回し配線を介して電気的に接続されており、

前記複数の電源供給線は、前記複数のＥＬ素子がそれぞれ有する前記画素電極に電気的に接続されており、

前記複数のＥＬ素子を駆動させるときにおける、前記複数のＥＬ素子がそれぞれ有する前記ＥＬ層の電流密度が大きいほど、前記複数の電源供給線にそれぞれ接続されている前記複数の引き回し配線の幅が大きいことを特徴とする表示装置。

【請求項８】請求項７において、前記複数のＥＬ素子を駆動させるときにおける、前記複数のＥＬ素子がそれぞれ有する前記ＥＬ層の電流密度が大きいほど、前記複数の電源供給線の幅が大きいことを特徴とする表示装置。

【請求項９】複数の画素と、複数の電源供給線と、複数の引き回し配線と、外部接続端子とを有する表示装置であって、

前記複数の画素は、前記複数の電源供給線のいずれか１つと、ＥＬ素子と、スイッチング用ＴＦＴと、ＥＬ駆動用ＴＦＴとを有しており、

前記ＥＬ素子は画素電極と、対向電極と、前記画素電極と前記対向電極の間に設けられたＥＬ層とを有しており、

前記スイッチング用ＴＦＴは前記ＥＬ駆動用ＴＦＴのスイッチングを制御しており、

前記ＥＬ駆動用ＴＦＴによって、前記複数の電源供給線のいずれか１つの電位が、前記ＥＬ素子が有する画素電極に与えられ、

前記外部接続端子と前記複数の電源供給線とは前記複数の引き回し配線を介して電気的に接続されており、

前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記複数の電源供給線にそれぞれ接続されている前記複数の引き回し配線の幅が大きいことを特徴とする表示装置。

【請求項１０】請求項９において、前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記ＥＬ駆動用ＴＦＴが有するチャネル形成領域のチャネル幅が大きいことを特徴とする表示装置。

【請求項１１】請求項９または請求項１０において、前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記ＥＬ駆動用ＴＦＴが有するＬＤＤ領域の長さが長いことを特徴とする表示装置。

【請求項１２】請求項９乃至請求項１１のいずれか１項において、前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記複数の電源供給線の幅が大きいことを特徴とす

る表示装置。

【請求項１３】複数の画素と、複数の電源供給線と、複数の引き回し配線と、外部接続端子とを有する表示装置であって、

前記複数の画素は、前記複数の電源供給線のいずれか１つと、ＥＬ素子と、スイッチング用ＴＦＴと、ＥＬ駆動用ＴＦＴとを有しており、

前記スイッチング用ＴＦＴを介して前記ＥＬ駆動用ＴＦＴのゲート電極にビデオ信号が入力されており、

前記ＥＬ駆動用ＴＦＴによって、前記複数の電源供給線のいずれか１つの電位が、前記ＥＬ素子が有する画素電極に与えられ、

前記外部接続端子と前記複数の電源供給線とは前記複数の引き回し配線を介して電気的に接続されており、

前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記複数の電源供給線にそれぞれ接続されている前記複数の引き回し配線の幅が大きくなっており、

前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きい画素ほど、前記ＥＬ駆動用ＴＦＴのゲート電極に入力されるビデオ信号の振幅が大きいことを特徴とする表示装置。

【請求項１４】請求項１３において、前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記ＥＬ駆動用ＴＦＴが有するチャネル形成領域のチャネル幅が大きいことを特徴とする表示装置。

【請求項１５】請求項１３または請求項１４において、前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記ＥＬ駆動用ＴＦＴが有するＬＤＤ領域の長さが長いことを特徴とする表示装置。

【請求項１６】請求項１３乃至請求項１５のいずれか１項において、前記ＥＬ素子を駆動させるときに前記複数の電源供給線を流れる電流の絶対値が大きいほど、前記複数の電源供給線の幅が大きいことを特徴とする表示装置。

【請求項１７】複数の画素と、複数の電源供給線と、複数の引き回し配線と、外部接続端子とを有する表示装置であって、

前記複数の画素は、前記複数の電源供給線のいずれか１つと、ＥＬ素子と、スイッチング用ＴＦＴと、ＥＬ駆動用ＴＦＴとを有しており、

前記ＥＬ素子は画素電極と、対向電極と、前記画素電極と前記対向電極の間に設けられたＥＬ層とを有しており、

前記スイッチング用ＴＦＴを介して前記ＥＬ駆動用ＴＦＴのゲート電極にビデオ信号が入力されており、

前記ＥＬ駆動用ＴＦＴによって、前記複数の電源供給線のいずれか１つの電位が、前記ＥＬ素子が有する画素電極に与えられ、

前記外部接続端子と前記複数の電源供給線とは前記複数の引き回し配線を介して電気的に接続されており、

前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記複数の電源供給線にそれぞれ接続されている前記複数の引き回し配線の幅が大きくなっており、

前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きい画素ほど、前記ＥＬ駆動用ＴＦＴのゲート電極に入力されるビデオ信号の振幅が大きいことを特徴とする表示装置。

【請求項１８】請求項１７において、前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記ＥＬ駆動用ＴＦＴが有するチャネル形成領域のチャネル幅が大きいことを特徴とする表示装置。

【請求項１９】請求項１７または請求項１８のいずれか１項において、前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記ＥＬ駆動用ＴＦＴが有するＬＤＤ領域の長さが長いことを特徴とする表示装置。

【請求項２０】請求項１７乃至請求項１９のいずれか１項において、前記ＥＬ素子を駆動させるときにおける、前記ＥＬ素子が有する前記ＥＬ層の電流密度が大きいほど、前記複数の電源供給線の幅が大きいことを特徴とする表示装置。

【請求項２１】複数の画素を有する表示装置であって、

前記複数の画素は、ＥＬ素子と、スイッチング用ＴＦＴと、ＥＬ駆動用ＴＦＴとをそれぞれ有しており、

前記スイッチング用ＴＦＴは前記ＥＬ駆動用ＴＦＴのスイッチングを制御しており、

前記ＥＬ駆動用ＴＦＴは前記ＥＬ素子の発光を制御しており、

前記ＥＬ駆動用ＴＦＴのゲート電極に入力される信号の電圧は、前記ＥＬ素子の発する光の色によって異なっていることを特徴とする表示装置。

【請求項２２】複数のＥＬ素子と、複数の電源供給線と、複数の引き回し配線と、外部接続端子とを有する表示装置であって、

前記外部接続端子と前記複数の電源供給線は、前記複数の引き回し配線のそれぞれ異なる１つを介して、電気的に接続されており、

前記複数のＥＬ素子がそれぞれ有する画素電極は、前記複数の電源供給線の、それぞれ異なる１つに電気的に接続されており、

前記複数の各ＥＬ素子は、互いに異なるＥＬ材料を有しており、

前記複数の引き回し配線の幅が互いに異なっていることを特徴とする表示装置。

【請求項２３】請求項１乃至請求項２１のいずれか１項

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において、前記表示装置を有することを特徴とする電子機器。

【請求項２４】請求項２３において、ＥＬディスプレイ、ビデオカメラ、頭部取り付け型の発光装置、画像再生装置、ゴーグル型ディスプレイ、パーソナルコンピュータ、携帯電話または音響再生装置であることを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体素子（半導体薄膜を用いた素子）を基板上に作り込んで形成されたＥＬ（エレクトロルミネッセンス）表示装置及びそのＥＬ表示装置を表示部に用いる電子機器（電子デバイス）に関する。

【０００２】

【従来の技術】近年、基板上にＴＦＴを形成する技術が大幅に進歩し、アクティブマトリクス型表示装置への応用開発が進められている。そして、アクティブマトリクス型表示装置の中でも特に、自発光型素子としてＥＬ素子を有したアクティブマトリクス型ＥＬ表示装置の研究が活発化している。ＥＬ表示装置は有機ＥＬディスプレイ（ＯＥＬＤ：Organic EL Display）又は有機ライトエミッティングダイオード（ＯＬＥＤ：Organic Light Emitting Diode）とも呼ばれている。

【０００３】ＥＬ表示装置は、液晶表示装置と異なり自発光型である。ＥＬ素子は一対の電極間にＥＬ層が挟まれた構造となっているが、ＥＬ層は通常、積層構造となっている。代表的には、イーストマン・コダック・カンパニーのTangらが提案した「正孔輸送層／発光層／電子輸送層」という積層構造が挙げられる。この構造は非常に発光効率が高く、現在、研究開発が進められているＥＬ表示装置は殆どこの構造を採用している。

【０００４】有機ＥＬ材料におけるルミネッセンスには、一重項励起状態から基底状態に戻る際の発光（蛍光）と三重項励起状態から基底状態に戻る際の発光（リン光）とがあるが、本発明のＥＬ素子は、上述した発光のうちの、いずれか一方の発光を用いていても良いし、または両方の発光を用いていても良い。

【０００５】また他にも、画素電極上に正孔注入層／正孔輸送層／発光層／電子輸送層、または正孔注入層／正孔輸送層／発光層／電子輸送層／電子注入層の順に積層する構造でも良い。ＥＬ層に対して蛍光性色素等をドーピングしても良い。

【０００６】そして、上記構造でなるＥＬ層に一対の電極から所定の電圧をかけ、それにより発光層においてキャリアの再結合が起こって発光する。なお本明細書においてＥＬ素子が発光することを、ＥＬ素子が駆動すると呼ぶ。

【０００７】なお、本明細書中では、陽極、ＥＬ層及び陰極で形成される発光素子をＥＬ素子と呼ぶ。

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【０００８】図１４に、代表的なアクティブマトリクス型ＥＬ表示装置（以下、ＥＬ表示装置）の構造を示す。図１４（Ａ）はＥＬ表示装置の画素部とその駆動回路の配置を示している。９０１は画素部、９０２はソース信号線駆動回路、９０３はゲート信号線駆動回路、９０５は引き出し端子である。

【０００９】画素部９０１は複数の画素９０６を有している。９０４は画素部９０１に設けられた電源供給線であり、全ての画素９０６が有するＥＬ素子の画素電極に電位を与えている。電源供給線９０４は引き回し配線９０７に接続されており、引き回し配線９０７は引き出し端子９０５を介して外部の電源に接続されている。

【００１０】ゲート信号線駆動回路９０３からゲート信号線９１３に入力される選択信号によって画素９０６が選択される。そしてソース信号線駆動回路９０２からソース信号線９１２に入力されるビデオ信号によって、電源供給線９０４の電位が選択された画素９０６に与えられ、画素９０６に画像の一部が表示される。

【００１１】図１４（Ａ）に示した画素９０６のうち、Ｒ（赤）、Ｇ（緑）、Ｂ（青）にそれぞれ対応する画素の回路図を図１４（Ｂ）に示す。

【００１２】図１４（Ｂ）において、Ｒ用画素９０６ｒと、Ｇ用画素９０６ｇと、Ｂ用画素９０６ｂは、共通のゲート信号線９１３を有している。また、Ｒ用画素９０６ｒはＲ用ソース信号線９１２ｒを、Ｇ用画素９０６ｇはＧ用ソース信号線９１２ｇを、Ｂ用画素９０６ｂはＢ用ソース信号線９１２ｂをそれぞれ有している。

【００１３】Ｒ用画素９０６ｒと、Ｇ用画素９０６ｇと、Ｂ用画素９０６ｂとは、スイッチング用ＴＦＴ９１０及びＥＬ駆動用ＴＦＴ９１１をそれぞれ有している。またＲ用画素９０６ｒはＲ用ＥＬ素子９１５ｒを、Ｇ用画素９０６ｇはＧ用ＥＬ素子９１５ｇを、Ｂ用画素９０６ｂはＢ用ＥＬ素子９１５ｂをそれぞれ有している。

【００１４】ゲート信号線９１３に選択信号が入力されると、ゲート信号線９１３にそのゲート電極が接続されたスイッチング用ＴＦＴ９１０が全てオンの状態になる。この状態を本明細書ではゲート信号線９１３が選択されていると呼ぶ。

【００１５】そして、Ｒ用ソース信号線９１２ｒ、Ｇ用ソース信号線９１２ｇ及びＢ用ソース信号線９１２ｂに入力されたビデオ信号が、オンの状態のスイッチング用ＴＦＴ９１０を介して、Ｒ用ＥＬ素子９１５ｒ、Ｇ用ＥＬ素子９１５ｇ及びＢ用ＥＬ素子９１５ｂにそれぞれ入力され、ＥＬ駆動用ＴＦＴ９１１のゲート電極に入力される。

【００１６】ビデオ信号がＥＬ駆動用ＴＦＴ９１１のゲート電極に入力されると、Ｒ用電源供給線９１４ｒの電位がＲ用ＥＬ素子９１５ｒの画素電極に、Ｇ用電源供給線９１４ｇの電位がＧ用ＥＬ素子９１５ｇの画素電極に、Ｂ用電源供給線９１４ｂの電位がＢ用ＥＬ素子９１

５ｂの画素電極にそれぞれ与えられる。その結果、Ｒ用ＥＬ素子９１５ｒ、Ｇ用ＥＬ素子９１５ｇ及びＢ用ＥＬ素子９１５ｂが発光し、Ｒ用画素９０６ｒ、Ｇ用画素９０６ｇ及びＢ用画素９０６ｂが表示を行う。

【００１７】ところで、ＥＬ表示装置には大きく分けて四つのカラー化表示方式があり、図１４に示したＥＬ表示装置のようにＲ（赤）Ｇ（緑）Ｂ（青）に対応した三種類の有機ＥＬ材料からなるＥＬ素子を形成する方式、白色発光のＥＬ素子とカラーフィルターを組み合わせた方式、青色又は青緑発光のＥＬ素子と蛍光体（蛍光性の色変換層：ＣＣＭ）とを組み合わせた方式、陰極（対向電極）に透明電極を使用してＲＧＢに対応したＥＬ素子を重ねる方式がある。

【００１８】そして一般的には、ＥＬ層にかかる電圧が同じであっても、ＥＬ層に用いられている有機ＥＬ材料によって、ＥＬ層の発光輝度は異なる。図１５に各色のＥＬ層の電圧－輝度特性を示す。図１５に示すように、ＥＬ層への印加電圧に対する発光輝度は、各色のＥＬ素子に用いられる有機ＥＬ材料によって異なっている。これは、有機ＥＬ材料によって、同じ印加電圧における電流密度の大きさが異なるためである。

【００１９】また電流密度が同じであっても、有機ＥＬ材料によって同じ電流密度における発光輝度は異なっている。

【００２０】そのため、一般的にＥＬ表示装置は、３色のＥＬ素子の発光輝度のバランスをそろえるために、各色の画素に対応する電源供給線の電位の高さをそれぞれ調整している。

【００２１】

【発明が解決しようとする課題】引き回し配線を介して画素部に流れる電流の大きさは、画素部において白表示を行っている画素の数で決まる。なお白表示を行っている画素とは、発光している状態のＥＬ素子を有する画素を意味する。白表示を行っている画素が多いほど、引き回し配線を介して画素部に流れる電流が大きくなる。

【００２２】引き回し配線を流れる電流が大きくなると、引き回し配線において電位降下が起こる。そのため、白表示を行っている画素の数が多いときと少ないときとでは、多いときのほうが、１つのＥＬ素子にかかる電圧が小さくなり、画素１つあたりの発光輝度が低くなる。

【００２３】とくにカラー表示のＥＬ表示装置の場合、各色のＥＬ素子にかかる電圧の大きさをそれぞれ調整し、各色のＥＬ素子に流れる電流の大きさを変えている。流れる電流が大きい画素ほど、該画素に対応する引き回し配線の電位降下が大きくなる。そのため、各色のＥＬ素子にかかる電圧の大きさをそれぞれ調整していても、白表示の画素が多いときと少ないときとでは、３色のＥＬ素子を流れる電流の比率が変わってしまう。

【００２４】よって、白表示の画素の数が変わると、３つの色にそれぞれ対応する画素の発光輝度のバランスが崩れるという事態が生じる。

【００２５】また、従来のＥＬ表示装置では、ＥＬ素子に流そうとする電流の大きさが各色ごとに異なっており、そのためＥＬ素子に加える電圧も異なっていた。しかしＥＬ素子と電源供給線との間にスイッチング素子として設けられたＥＬ駆動用ＴＦＴのＬＤＤ幅や、チャネル幅は全て同じであり、また全てのＥＬ駆動用ＴＦＴのゲート電極に入力されるデジタル信号の電圧の振幅も同じであった。このため、電源供給線にかかる電圧の高さによって、ＥＬ駆動用ＴＦＴが劣化されてしまう。またＥＬ駆動用ＴＦＴのゲート電極に入力されるデジタル信号の電圧の振幅が必要以上に大きいと、消費電力を抑えることができない。

【００２６】上記問題に鑑み、本発明は、高精細なカラー表示が可能なＥＬ表示装置の提供を課題とする。

【００２７】

【課題を解決するための手段】本発明者らは、ＥＬ素子に流す電流を大きくしたい画素ほど、該画素のＥＬ素子に電圧または電流を供給する引き回し配線の幅を大きくした。これによって、ＥＬ素子に流す電流を大きくしたい画素ほど、該画素のＥＬ素子に電圧または電流を供給する引き回し配線の配線抵抗が小さくなる。配線抵抗が小さくなると、引き回し配線における電位降下が小さくなり、ＥＬ素子に流す電流を大きくすることが可能になる。なお実際のパネルでは、引き回し配線を配置するスペースは限られているので、各色における引き回し配線の幅の比を変えることで、各色のＥＬ素子に流れる電流の大きさのバランスを取ることが可能である。

【００２８】上記構成によって、白表示の画素の数に関わりなく、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることが可能になる。

【００２９】また引き回し配線だけではなく、ＥＬ素子に流す電流を大きくしたい画素ほど、該画素のＥＬ素子に電圧または電流を供給する電源供給線の幅の比も大きくなるように設計すると、より一層高精細な画像を表示することが可能になる。

【００３０】また本発明において、ＥＬ素子に大きい電流が流れる画素においてのみ、入力するビデオ信号の振幅を大きくしても良い。上記構成によって、全ての画素に不必要に大きな振幅のビデオ信号を画素に入力せずに済み、消費電力を抑えることができる。

【００３１】また、ＥＬ素子への電流の制御を行うＥＬ駆動用ＴＦＴは、ＥＬ素子を発光させるために、ＥＬ駆動用ＴＦＴの駆動を制御するスイッチング用ＴＦＴよりも比較的多くの電流を流す。なおＴＦＴの駆動を制御するとは、ＴＦＴが有するゲート電極にかかる電圧を制御することで、そのＴＦＴをオン状態またはオフ状態にすることを意味する。特に本発明は上記構成において、電流の絶対値が大きい電源供給線に接続されている画素の

ＥＬ駆動用ＴＦＴには、より多くの電流が流れることになる。そのため電流の絶対値が大きい電源供給線に接続されている画素のＥＬ駆動用ＴＦＴは、他の画素のＥＬ駆動用ＴＦＴよりもホットキャリア注入によって早く劣化してしまうという問題が浮上してくる。

【００３２】そこで本発明において、ホットキャリア注入によるＥＬ駆動用ＴＦＴの劣化対策として、上記構成に加え、発光輝度の低い色を表示する画素のＥＬ駆動用ＴＦＴのＬＤＤ領域の長さを、発光輝度の高い色を表示する画素のＥＬ駆動用ＴＦＴのＬＤＤ領域の長さより長くする構成を加えても良い。

【００３３】なお本明細書においてＬＤＤ領域の長さとは、ソース領域とドレイン領域を結ぶ方向におけるＬＤＤ領域の長さを意味する。

【００３４】また同時に、電流の絶対値が大きい電源供給線に接続されている画素のＥＬ駆動用ＴＦＴのチャネル幅（Ｗ）をより大きくしても良い。

【００３５】図５に代表的なＴＦＴの上面図と断面図を示す。図５（Ａ）はＴＦＴの上面図であり、図５（Ｂ）は図５（Ａ）のＡ－Ａ’における断面図である。

【００３６】５０１はソース領域、５０２はドレイン領域、５０３がゲート電極である。ゲート電極５０３の下にはゲート絶縁膜５０５を介してチャネル形成領域５０４が設けられている。本明細書においてチャネル幅（Ｗ）とは、ソース領域５０１とドレイン領域５０２の間に流れる電流の方向に対して垂直方向におけるチャネル領域５０４の長さを意味する。またチャネル長（Ｌ）とは、ソース領域５０１とドレイン領域５０２に流れる電流の方向におけるチャネル領域５０４の長さを意味する。

【００３７】本発明は上記構成により、電源供給線を流れる電流の絶対値が大きくなることによってＥＬ駆動用ＴＦＴが制御する電流の量が増えても、ＥＬ駆動用ＴＦＴの劣化を抑えることができる。そしてなおかつ、ＥＬ素子に印加される電圧の値によって、そのＥＬ素子の発光輝度を調節することが可能になり、赤色、青色、緑色の発光輝度のバランスが良い、色鮮やかな画像を表示することが可能になる。

【００３８】

【発明の実施の形態】図１に本発明のＥＬ表示装置の上面図を示す。図１（Ａ）はＥＬ表示装置の画素部とその駆動回路の配置を示している。１０１は画素部、１０２はソース信号線駆動回路、１０３はゲート信号線駆動回路、１０５は引き出し端子である。

【００３９】画素部１０１は複数の画素１０６を有している。１０４は画素部１０１に設けられた電源供給線であり、全ての画素１０６が有するＥＬ素子の画素電極に電位を与えている。電源供給線１０４は引き回し配線１０７に接続されており、引き回し配線１０７は引き出し端子１０５を介して外部の電源に接続されている。なお



引き回し配線１０７のレイアウトは図１に示した形態に限定されない。

【００４０】ゲート信号線駆動回路１０３からゲート信号線（図示せず）に入力される選択信号によって画素１０６が選択される。そしてソース信号線駆動回路１０２からソース信号線（図示せず）に入力されるビデオ信号によって、電源供給線１０４の電位が選択された画素１０６に与えられ、画素１０６に画像の一部が表示される。

【００４１】図１（Ｂ）に図１（Ａ）における引き回し配線１０７の拡大図を示す。１０７ｒはＲ用引き回し配線、１０７ｇはＧ用引き回し配線、１０７ｂはＢ用引き回し配線である。

【００４２】ＥＬ素子は引き回し配線と直列に接続されていることから、ＲＧＢの各色に対応する引き回し配線を流れる電流の比は、ＲＧＢの各色に対応するＥＬ層の電流密度の比に相当する。また一般的に配線抵抗はシート抵抗と配線の長さに比例し、配線の幅に反比例する。ここでシート抵抗と配線の長さは固定している。

【００４３】Ｒ用の引き回し配線にかかる電圧をＶｒ、Ｇ用の引き回し配線にかかる電圧をＶｇ、Ｂ用の引き回し配線にかかる電圧をＶｂとし、Ｒ用の引き回し配線の幅をＷｒ、Ｇ用の引き回し配線の幅をＷｇ、Ｂ用の引き回し配線の幅をＷｂとし、Ｒ用のＥＬ素子の電流密度をＩｒ、Ｇ用のＥＬ素子の電流密度をＩｇ、Ｂ用のＥＬ素子の電流密度をＩｂとすると、オームの法則より以下の式１が成り立つ。なおａは定数である。

【００４４】

【式１】Ｖｒ＝ａ×Ｉｒ／Ｗｒ

Ｖｇ＝ａ×Ｉｇ／Ｗｇ

Ｖｂ＝ａ×Ｉｂ／Ｗｂ

【００４５】ここで、Ｖｒ＝Ｖｇ＝Ｖｂとすると、以下の式２が導き出される。

【００４６】

【式２】Ｉｒ／Ｗｒ＝Ｉｇ／Ｗｇ＝Ｉｂ／Ｗｂ

【００４７】式２より以下の式３が導き出される。

【００４８】

【式３】Ｗｒ：Ｗｇ：Ｗｂ＝Ｉｒ：Ｉｇ：Ｉｂ

【００４９】よって式３より、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えるためには、電流密度が大きいＥＬ素子に電気的に接続された引き回し配線の幅が、電流密度が小さいＥＬ素子に電気的に接続された引き回し配線の幅より大きくなるように設計する。望ましくは、引き回し配線の幅の比を、式３を満たすように設計する。

【００５０】また引き回し配線だけではなく、ＥＬ素子に流す電流を大きくしたい画素ほど、該画素のＥＬ素子に電圧または電流を供給する電源供給線の幅の比も、式３を満たすように設計すると、より一層高精細な画像を表示することが可能になる。

【００５１】上記構成によって、白表示の画素の数に関わりなく、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることが可能になる。

【００５２】

【実施例】（実施例１）本実施例では、ＥＬ素子に大きい電圧を必要とする画素ほど、該画素に入力するデジタル信号の振幅を大きくする例について説明する。

【００５３】ＥＬ表示装置の画素において、ＥＬ駆動用ＴＦＴとＥＬ素子の接続構成を図２に簡単に示す。２０２はＥＬ駆動用ＴＦＴ、２０３は電源供給線、２０６はＥＬ素子である。ＥＬ駆動用ＴＦＴ２０２のゲート電極は、端子２０１に与えられるデジタル信号が入力されている。ＥＬ駆動用ＴＦＴ２０２のソース領域は電源供給線２０３に接続されており、ドレイン領域はＥＬ素子２０６が有する画素電極に接続されている。

【００５４】ＥＬ素子の発光輝度を高くするために電源供給線２０３に与えられる電流の絶対値を大きくすると、ＥＬ駆動用ＴＦＴ２０２のオフ電流（ＴＦＴがオフの状態のときに流れる電流）が大きくなる。そのため、ＥＬ駆動用ＴＦＴ２０２がオフの状態のときでもＥＬ素子が発光するということが起こり得る。

【００５５】本発明では、電源供給線を流れる電流の絶対値が大きい画素ほど、該画素に入力される（図２の場合、具体的には端子２０１に入力される）デジタル信号の振幅を増幅する。増幅されたデジタル信号はＥＬ駆動用ＴＦＴ２０２のゲート電極に入力されるため、ＥＬ駆動用ＴＦＴ２０２の$|V_{GS}|$はデジタル信号が増幅される前に比べて大きくなる。よって電源供給線２０３の電流の絶対値を大きくしても、ＥＬ駆動用ＴＦＴ２０２のオフ電流を抑えることができ、ＥＬ駆動用ＴＦＴ２０２がオフの状態のときでもＥＬ素子が発光するという事態を防ぐことが可能になる。

【００５６】なお、本発明は、デジタル信号を用いて画像を表示するＥＬ表示装置に限定されず、アナログ信号を用いて画像を表示するＥＬ表示装置であっても良い。

【００５７】（実施例２）本実施例では、実施例１で用いられるソース信号線駆動回路の具体的な構成について、例を挙げて説明する。

【００５８】図３に本実施例のソース信号線駆動回路のブロック図を示す。４００は画素部、４０１はソース信号線駆動回路である。ソース信号線駆動回路４０１は、シフトレジスタ回路４０２、第１ラッチ回路４０３、第２ラッチ回路４０４、レベルシフタ回路４０５、バッファ回路４０６を有している。

【００５９】シフトレジスタ回路４０２において生成されたタイミング信号（ＴＳ）にしたがって、ソース信号線駆動回路４０１の外部から第１ラッチ回路４０３にデジタル信号（ＤＶ）が入力され保持される。全てのビットのデジタル信号が第１ラッチ回路４０３に入力され保持されると、ラッチパルス（ＬＰ）にしたがって、第１ラッチ回路４０３に保持されているデジタル信号が第２ラッチ回路４０４に一斉に入力され保持される。そして第１ラッチ回路４０３にソース信号線駆動回路４０１の外部からデジタル信号（ＤＶ）が入力され保持されるという動作が再び開始される。

【００６０】第２ラッチ回路４０４に一斉に入力され保持されたデジタル信号は、レベルシフタ回路４０５に入力され、その振幅が増幅されてレベルシフタ回路から出力される。増幅する大きさは、デジタル信号が入力される画素において、電源供給線を流れる電流の高さの絶対値によって異なる。デジタル信号が入力される画素において、電源供給線を流れる電流の高さの絶対値が大きいほど、該画素に入力されるデジタルビデオ信の振幅は大きく増幅されるようにする。

【００６１】このように、レベルシフタ回路の出力電圧、すなわちレベルシフタ回路の電源電位を変えることによって、画素に入力されるデジタル信号の振幅を、各色ごとに変えることが可能になる。

【００６２】上記構成によって、電源供給線の電流の絶対値を大きくしても、ＥＬ駆動用ＴＦＴのオフ電流を抑えることができ、ＥＬ駆動用ＴＦＴがオフの状態のときでもＥＬ素子が発光するという事態を防ぐことが可能になる。

【００６３】レベルシフタ回路４０５から出力された増幅後のデジタル信号はバッファ回路４０６において緩衝増幅され、対応するソース信号線に入力される。

【００６４】図４にレベルシフタ回路４０５の等価回路図の一例を示す。デジタル信号はレベルシフタ回路４０５のＶｉｎから入力される。そしてデジタル信号の極性を反転させた信号はＶｉｎｂから入力される。また、ＶｄｄｈはＨ電圧側電源、Ｖｓｓは低電圧側電源に接続されていることを意味している。

【００６５】レベルシフタ回路４０３は、Ｖｉｎに入力されたデジタル信号を増幅させた信号が、Ｖｏｕｔから出力されるように設計されている。具体的には、ＶｉｎにＨｉのデジタル信号が入力されるとＶｏｕｔからＶｓｓ相当の信号が、Ｌｏのデジタル信号が入力されるとＶｏｕｔからＶｄｄｈ相当の信号が出力される。

【００６６】（実施例３）本実施例では、図１に示した引き回し配線１０７の幅の具体的な数値を示す。

【００６７】本実施例では、Ｒ、Ｇ、ＢのＥＬ素子の発光輝度がそれぞれ１００ｃｄ／$m^2$、１００ｃｄ／$m^2$、５０ｃｄ／$m^2$となるように、Ｒ、Ｇ、Ｂの有機ＥＬ材料の電流密度をそれぞれ７．５ｍＡ／$cm^2$、３ｍＡ／$cm^2$、５ｍＡ／$cm^2$とした。

【００６８】上述した電流密度の値から、実施の形態で示した式３より、Ｒ、Ｇ、Ｂに対応する画素の電源供給線の幅の比は、式４で表される。

【式４】Ｗｒ：Ｗｇ：Ｗｂ≒７．５：３：５

【００６９】式４にしたがって引き回し配線の幅を設計

すると、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることができる。

【００７０】なお本実施例においてＲ、Ｇ、Ｂに対応する引き回し配線の幅は式４を満たしていなくとも良い。Ｒに対応する引き回し配線の幅を一番大きくし、Ｇに対応する引き回し配線の幅を一番小さくすれば良い。

【００７１】上記構成によって、白表示の画素の数に関わりなく、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることが可能になる。

【００７２】また引き回し配線だけではなく、Ｒに対応する電源供給線の幅を一番大きくし、Ｇに対応する電源供給線の幅を一番小さくすれば、より効果的にＲ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることが可能になる。より好ましくは引き回し配線と同様に、電源供給線の幅も式４を満たすように設計すると、より一層、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることが可能になる。

【００７３】なお本発明において用いられる有機ＥＬ材料の電流密度は上述した数値に限定されない。

【００７４】また本実施例では、デジタル信号で表示を行うＥＬ表示装置においてデジタル信号の振幅を増幅する例を示したが、本発明はこの構成に限定されない。アナログビデオ信号で表示を行うＥＬ表示装置においてアナログビデオ信号の振幅を増幅する構成も本発明に含まれる。

【００７５】本実施例は実施例１または実施例２と自由に組み合わせて実施することが可能である。

【００７６】（実施例４）本発明のＥＬ表示装置は画素内にいくつのＴＦＴを設けた構造としても良い。例えば、３つ乃至６つまたはそれ以上のＴＦＴを設けても構わない。本実施例では、ＥＬ表示装置が画素内に３つのＴＦＴを設けている構成について示す。

【００７７】図６において、４７０２はスイッチング用ＴＦＴ、４７０１はソース信号線、４７０３はスイッチング用ＴＦＴ４７０２のゲート電極に接続されたゲート信号線、４７０４はＥＬ駆動用ＴＦＴ、４７０５はコンデンサ（省略することも可能）、４７０６は電源供給線、、４７０７は電源制御用ＴＦＴ、４７０８は電源制御用ゲート信号線、４７０９はＥＬ素子とする。電源制御用ＴＦＴ４７０７の動作については特願２０００－３６４００３号を参照すると良い。

【００７８】また、本実施例では電源制御用ＴＦＴ４７０７をＥＬ駆動用ＴＦＴ４７０４とＥＬ素子４７０８との間に設けているが、電源制御用ＴＦＴ４７０７とＥＬ素子４７０８との間にＥＬ駆動用ＴＦＴ４７０４が設けられた構造としても良い。また、電源制御用ＴＦＴ４７０７はＥＬ駆動用ＴＦＴ４７０４と同一構造とするか、同一の活性層で直列させて形成するのが好ましい。

【００７９】図７において、４８０１はソース信号線、４８０２はスイッチング用ＴＦＴ、４８０３はスイッチング用ＴＦＴ４８０２のゲート電極に接続されたゲート信号線、４８０４はＥＬ駆動用ＴＦＴ、４８０５はコンデンサ（省略することも可能）、４８０６は電源供給線、、４８０７は消去用ＴＦＴ、４８０８は消去用ゲート信号線、４８０９はＥＬ素子とする。消去用ＴＦＴ４８０７の動作については特願２０００－３５９０３２号を参照すると良い。

【００８０】消去用ＴＦＴ４８０７のドレインはＥＬ駆動用ＴＦＴ４８０４のゲートに接続され、ＥＬ駆動用ＴＦＴ４８０４のゲート電圧を強制的に変化させることができるようになっている。なお、消去用ＴＦＴ４８０７はｎチャネル型ＴＦＴとしてもｐチャネル型ＴＦＴとしても良いが、オフ電流を小さくできるようにスイッチング用ＴＦＴ４８０２と同一構造とすることが好ましい。

【００８１】本実施例は実施例１～実施例３と自由に組み合わせて実施することが可能である。

【００８２】（実施例５）本実施例では、本発明のＥＬ表示装置において、同一基板上に画素部と、画素部の周辺に設ける駆動回路のＴＦＴ（ｎチャネル型ＴＦＴ及びｐチャネル型ＴＦＴ）を同時に作製する方法について詳細に図８～図１１を用いて説明する。

【００８３】まず、本実施例ではコーニング社の＃７０５９ガラスや＃１７３７ガラスなどに代表されるバリウムホウケイ酸ガラス、またはアルミノホウケイ酸ガラスなどのガラスからなる基板３００を用いる。なお、基板３００としては、透光性を有する基板であれば限定されず、石英基板を用いても良い。また、本実施例の処理温度に耐えうる耐熱性を有するプラスチック基板を用いてもよい。

【００８４】次いで、基板３００上に酸化珪素膜、窒化珪素膜または酸化窒化珪素膜などの絶縁膜から成る下地膜３０１を形成する。本実施例では下地膜３０１として２層構造を用いるが、前記絶縁膜の単層膜または２層以上積層させた構造を用いても良い。下地膜３０１の一層目としては、プラズマＣＶＤ法を用い、$SiH_4$、$NH_3$、及び$N_2O$を反応ガスとして成膜される酸化窒化珪素膜３０１ａを１０～２００nm（好ましくは５０～１００nm）形成する。本実施例では、膜厚５０ｎｍの酸化窒化珪素膜３０１ａ（組成比Ｓｉ＝３２％、Ｏ＝２７％、Ｎ＝２４％、Ｈ＝１７％）を形成した。次いで、下地膜３０１のニ層目としては、プラズマＣＶＤ法を用い、$SiH_4$、及び$N_2O$を反応ガスとして成膜される酸化窒化珪素膜３０１ｂを５０～２００ｎｍ（好ましくは１００～１５０nm）の厚さに積層形成する。本実施例では、膜厚１００ｎｍの酸化窒化珪素膜３０１ｂ（組成比Ｓｉ＝３２％、Ｏ＝５９％、Ｎ＝７％、Ｈ＝２％）を形成した。

【００８５】次いで、下地膜上に半導体層３０２～３０５を形成する。半導体層３０２～３０５は、非晶質構造を有する半導体膜を公知の手段（スパッタ法、ＬＰＣＶ

Ｄ法、またはプラズマＣＶＤ法等）により成膜した後、公知の結晶化処理（レーザー結晶化法、熱結晶化法、またはニッケルなどの触媒を用いた熱結晶化法等）を行って得られた結晶質半導体膜を所望の形状にパターニングして形成する。この半導体層３０２～３０５の厚さは２５～８０ｎｍ（好ましくは３０～６０ｎｍ）の厚さで形成する。結晶質半導体膜の材料に限定はないが、好ましくは珪素（シリコン）またはシリコンゲルマニウム（$Si_XGe_{1-X}$（Ｘ＝０．０００１～０．０２））合金などで形成すると良い。本実施例では、プラズマＣＶＤ法を用い、５５ｎｍの非晶質珪素膜を成膜した後、ニッケルを含む溶液を非晶質珪素膜上に保持させた。この非晶質珪素膜に脱水素化（５００℃、１時間）を行った後、熱結晶化（５５０℃、４時間）を行い、さらに結晶化を改善するためのレーザーアニール処理を行って結晶質珪素膜を形成した。そして、この結晶質珪素膜をフォトリソグラフィ法を用いたパターニング処理によって、半導体層３０２～３０５を形成した。

【００８６】また、半導体層３０２～３０５を形成した後、ＴＦＴのしきい値を制御するために微量な不純物元素（ボロンまたはリン）のドーピングを行ってもよい。

【００８７】また、レーザー結晶化法で結晶質半導体膜を作製する場合には、パルス発振型または連続発光型のエキシマレーザーやＹＡＧレーザー、$YVO_4$レーザーを用いることができる。これらのレーザーを用いる場合には、レーザー発振器から放射されたレーザー光を光学系で線状に集光し、半導体膜に照射する方法を用いると良い。結晶化の条件は実施者が適宜選択するものであるが、エキシマレーザーを用いる場合はパルス発振周波数３００Ｈｚとし、レーザーエネルギー密度を１００～４００mJ/cm$^2$(代表的には２００～３００mJ/cm$^2$)とする。また、ＹＡＧレーザーを用いる場合にはその第２高調波を用いパルス発振周波数３０～３００ｋＨｚとし、レーザーエネルギー密度を３００～６００mJ/cm$^2$(代表的には３５０～５００mJ/cm$^2$)とすると良い。そして幅１００～１０００μｍ、例えば４００μｍで線状に集光したレーザー光を基板全面に渡って照射し、この時の線状レーザー光の重ね合わせ率（オーバーラップ率）を５０～９０％として行えばよい。

【００８８】次いで、半導体層３０２～３０５を覆うゲート絶縁膜３０６を形成する。ゲート絶縁膜３０６はプラズマＣＶＤ法またはスパッタ法を用い、厚さを４０～１５０ｎｍとして珪素を含む絶縁膜で形成する。本実施例では、プラズマＣＶＤ法により１１０ｎｍの厚さで酸化窒化珪素膜（組成比Ｓｉ＝３２％、Ｏ＝５９％、Ｎ＝７％、Ｈ＝２％）で形成した。勿論、ゲート絶縁膜は酸化窒化珪素膜に限定されるものでなく、他の珪素を含む絶縁膜を単層または積層構造として用いても良い。

【００８９】また、酸化珪素膜を用いる場合には、プラズマＣＶＤ法でＴＥＯＳ（Tetraethyl Orthosilicate）と$O_2$とを混合し、反応圧力４０Pa、基板温度３００～４００℃とし、高周波（１３．５６MHz）電力密度０．５～０．８W/cm$^2$で放電させて形成することができる。このようにして作製される酸化珪素膜は、その後４００～５００℃の熱アニールによりゲート絶縁膜として良好な特性を得ることができる。

【００９０】次いで、図８（Ａ）に示すように、ゲート絶縁膜３０６上に膜厚２０～１００ｎｍの第１の導電膜３０７と、膜厚１００～４００ｎｍの第２の導電膜３０８とを積層形成する。本実施例では、膜厚３０ｎｍのＴａＮ膜からなる第１の導電膜３０７と、膜厚３７０ｎｍのＷ膜からなる第２の導電膜３０８を積層形成した。ＴａＮ膜はスパッタ法で形成し、Ｔａのターゲットを用い、窒素を含む雰囲気内でスパッタした。また、Ｗ膜は、Ｗのターゲットを用いたスパッタ法で形成した。その他に６フッ化タングステン（ＷＦ６）を用いる熱ＣＶＤ法で形成することもできる。いずれにしてもゲート電極として使用するためには低抵抗化を図る必要があり、Ｗ膜の抵抗率は２０μΩｃｍ以下にすることが望ましい。Ｗ膜は結晶粒を大きくすることで低抵抗率化を図ることができるが、Ｗ膜中に酸素などの不純物元素が多い場合には結晶化が阻害され高抵抗化する。従って、本実施例では、高純度のＷ（純度９９．９９９９％または９９．９９％）のターゲットを用いたスパッタ法で、さらに成膜時に気相中からの不純物の混入がないように十分配慮してＷ膜を形成することにより、抵抗率９～２０μΩｃｍを実現することができた。

【００９１】なお、本実施例では、第１の導電膜３０７をＴａＮ、第２の導電膜３０８をＷとしたが、特に限定されず、いずれもＴａ、Ｗ、Ｔｉ、Ｍｏ、Ａｌ、Ｃｕ、Ｃｒ、Ｎｄから選ばれた元素、または前記元素を主成分とする合金材料若しくは化合物材料で形成してもよい。また、リン等の不純物元素をドーピングした多結晶珪素膜に代表される半導体膜を用いてもよい。また、Ａｇ、Ｐｄ、Ｃｕからなる合金を用いてもよい。また、第１の導電膜をタンタル（ＴａＮ）膜で形成し、第２の導電膜をＷ膜とする組み合わせ、第１の導電膜を窒化チタン（ＴｉＮ）膜で形成し、第２の導電膜をＷ膜とする組み合わせ、第１の導電膜を窒化タンタル（ＴａＮ）膜で形成し、第２の導電膜をＡｌ膜とする組み合わせ、第１の導電膜を窒化タンタル（ＴａＮ）膜で形成し、第２の導電膜をＣｕ膜とする組み合わせとしてもよい。

【００９２】次に、図８（Ｂ）に示すようにフォトリソグラフィ法を用いてレジストからなるマスク３０９～３１２を形成し、電極及び配線を形成するための第１のエッチング処理を行う。第１のエッチング処理では第１及び第２のエッチング条件で行う。本実施例では第１のエッチング条件として、ＩＣＰ（Inductively CoupledPlasma：誘導結合型プラズマ）エッチング法を用い、エッチング用ガスに$CF_4$と$Cl_2$と$O_2$とを用い、それぞれ

のガス流量比を２５／２５／１０（ｓｃｃｍ）とし、１Paの圧力でコイル型の電極に５００WのＲＦ（13.56MHz）電力を投入してプラズマを生成してエッチングを行った。ここでは、松下電器産業（株）製のＩＣＰを用いたドライエッチング装置（Model　Ｅ６４５－□ＩＣＰ）を用いた。基板側（試料ステージ）にも１５０WのＲＦ（13.56MHz）電力を投入し、実質的に負の自己バイアス電圧を印加する。この第１のエッチング条件によりW膜をエッチングして第１の導電層の端部をテーパー形状とする。第１のエッチング条件でのWに対するエッチング速度は２００．３９nm／ｍｉｎ、ＴａNに対するエッチング速度は８０．３２nm／ｍｉｎであり、ＴａNに対するWの選択比は約２．５である。また、この第１のエッチング条件によって、Wのテーパー角は、約２６°となる。

【００９３】この後、図８（Ｂ）に示すようにレジストからなるマスク３０９～３１２を除去せずに第２のエッチング条件に変え、エッチング用ガスに$CF_4$と$Cl_2$とを用い、それぞれのガス流量比を３０／３０（ｓｃｃｍ）とし、１Paの圧力でコイル型の電極に５００WのＲＦ（13.56MHz）電力を投入してプラズマを生成して約３０秒程度のエッチングを行った。基板側（試料ステージ）にも２０WのＲＦ（13.56MHz）電力を投入し、実質的に負の自己バイアス電圧を印加する。$CF_4$と$Cl_2$を混合した第２のエッチング条件ではW膜及びＴａN膜とも同程度にエッチングされる。第２のエッチング条件でのWに対するエッチング速度は５８．９７nm／ｍｉｎ、ＴａNに対するエッチング速度は６６．４３nm／ｍｉｎである。なお、ゲート絶縁膜上に残渣を残すことなくエッチングするためには、１０～２０%程度の割合でエッチング時間を増加させると良い。

【００９４】上記第１のエッチング処理では、レジストからなるマスクの形状を適したものとすることにより、基板側に印加するバイアス電圧の効果により第１の導電層及び第２の導電層の端部がテーパー形状となる。このテーパー部の角度は１５～４５°とすればよい。こうして、第１のエッチング処理により第１の導電層と第２の導電層から成る第１の形状の導電層３１４～３１７（第１の導電層３１４ａ～３１７ａと第２の導電層３１４ｂ～３１７ｂ）を形成する。３１９はゲート絶縁膜であり、第１の形状の導電層３１４～３１７で覆われない領域は２０～５０nm程度エッチングされ薄くなった領域が形成される。

【００９５】そして、レジストからなるマスクを除去せずに第１のドーピング処理を行い、半導体層にｎ型を付与する不純物元素を添加する。（図８（Ｂ））ドーピング処理はイオンドープ法、若しくはイオン注入法で行えば良い。イオンドープ法の条件はドーズ量を$1\times10^{13}$～$5\times10^{15}atoms/cm^2$とし、加速電圧を６０～１００ｋｅＶとして行う。本実施例ではドーズ量を$1.5\times10^{15}atoms/cm^2$とし、加速電圧を８０ｋｅＶとして行った。ｎ型を付与する不純物元素として１５族に属する元素、典型的にはリン（Ｐ）または砒素（Ａｓ）を用いるが、ここではリン（Ｐ）を用いた。この場合、導電層３１４～３１７がｎ型を付与する不純物元素に対するマスクとなり、自己整合的に高濃度不純物領域３２０～３２３が形成される。高濃度不純物領域３２０～３２３には$1\times10^{20}$～$1\times10^{21}atoms/cm^3$の濃度範囲でｎ型を付与する不純物元素を添加する。

【００９６】次いで、図８（Ｃ）に示すようにレジストからなるマスクを除去せずに第２のエッチング処理を行う。ここでは、エッチング用ガスに$CF_4$と$Cl_2$と$O_2$とを用い、それぞれのガス流量比を２０／２０／２０（ｓｃｃｍ）とし、１Paの圧力でコイル型の電極に５００WのＲＦ（13.56MHz）電力を投入してプラズマを生成してエッチングを行った。基板側（試料ステージ）にも２０WのＲＦ（13.56MHz）電力を投入し、実質的に負の自己バイアス電圧を印加する。第２のエッチング処理でのWに対するエッチング速度は１２４．６２nm／ｍｉｎ、ＴａNに対するエッチング速度は２０．６７nm／ｍｉｎであり、ＴａNに対するWの選択比は６．０５である。従って、W膜が選択的にエッチングされる。この第２のエッチングによりWのテーパー角は７０°となった。この第２のエッチング処理により第２の導電層３２４ｂ～３２７ｂを形成する。一方、第１の導電層３１４ａ～３１７ａは、ほとんどエッチングされず、第１の導電層３２４ａ～３２７ａを形成する。

【００９７】次いで、第２のドーピング処理を行う。ドーピングは第２の導電層３２４ｂ～３２７ｂを不純物元素に対するマスクとして用い、第１の導電層のテーパー部下方の半導体層に不純物元素が添加されるようにドーピングする。本実施例では、不純物元素としてＰ（リン）を用い、ドーズ量$1.5\times10^{14}$、電流密度０．５μＡ、加速電圧９０ｋｅＶにてプラズマドーピングを行った。こうして、第１の導電層と重なる低濃度不純物領域３２９～３３２を自己整合的に形成する。この低濃度不純物領域３２９～３３２へ添加されたリン（Ｐ）の濃度は、$1\times10^{17}$～$5\times10^{18}atoms/cm^3$であり、且つ、第１の導電層のテーパー部の膜厚に従って緩やかな濃度勾配を有している。なお、第１の導電層のテーパー部と重なる半導体層において、第１の導電層のテーパー部の端部から内側に向かって若干、不純物濃度が低くなっているものの、ほぼ同程度の濃度である。また、高濃度の不純物元素が添加された高濃度不純物領域３３３～３３６を形成する。

【００９８】次いで、図９（Ｂ）に示すようにレジストからなるマスクを除去してからフォトリソグラフィー法を用いて、第３のエッチング処理を行う。この第３のエッチング処理では第１の導電層のテーパー部を部分的にエッチングして、第２の導電層と重なる形状にするため

に行われる。ただし、第３のエッチングを行わない領域には、図９（Ｂ）に示すようにレジストからなるマスク３３８を形成する。

【００９９】第３のエッチング処理におけるエッチング条件は、エッチングガスとして$Cl_2$と$SF_6$とを用い、それぞれのガス流量比を１０／５０（ｓｃｃｍ）として第１及び第２のエッチングと同様にＩＣＰエッチング法を用いて行う。なお、第３のエッチング処理でのＴａＮに対するエッチング速度は、１１１．２nm/minであり、ゲート絶縁膜に対するエッチング速度は、１２．８nm/minである。

【０１００】本実施例では、１．３Ｐａの圧力でコイル型の電極に５００WのＲＦ（13.56MHz）電力を投入してプラズマを生成してエッチングを行った。基板側（試料ステージ）にも１０WのＲＦ（13.56MHz）電力を投入し、実質的に負の自己バイアス電圧を印加する。以上により、第１の導電層３４０ａ～３４２ａが形成される。

【０１０１】上記第３のエッチングによって、第１の導電層３４０ａ～３４２ａと重ならない不純物領域（ＬＤＤ領域）３４３～３４５が形成される。なお、不純物領域（ＧＯＬＤ領域）３４６は、第１の導電層３２４ａと重なったままである。

【０１０２】また、第１の導電層３２４ａと第２の導電層３２４ｂとで形成された電極は、最終的に駆動回路のｎチャネル型ＴＦＴのゲート電極となり、また、第１の導電層３４０ａと第２の導電層３４０ｂとで形成された電極は、最終的に駆動回路のｐチャネル型ＴＦＴのゲート電極となる。

【０１０３】同様に、第１の導電層３４１ａと第２の導電層３４１ｂとで形成された電極は、最終的に画素部のｎチャネル型ＴＦＴのゲート電極となり、第１の導電層３４２ａと第２の導電層３４２ｂとで形成された電極は、最終的に画素部のｐチャネル型ＴＦＴのゲート電極となる。

【０１０４】このようにして、本実施例は、第１の導電層３４０ａ～３４２ａと重ならない不純物領域（ＬＤＤ領域）３４３～３４５と、第１の導電層３２４ａと重なる不純物領域（ＧＯＬＤ領域）３４６を同時に形成することができ、ＴＦＴ特性に応じた作り分けが可能となる。

【０１０５】次にゲート絶縁膜３１９をエッチング処理する。ここでのエッチング処理は、エッチングガスに$CHF_3$を用い、反応性イオンエッチング法（ＲＩＥ法）を用いて行う。本実施例では、チャンバー圧力６．７Ｐａ、ＲＦ電力８００W、$CHF_3$ガス流量３５ｓｃｃｍで第３のエッチング処理を行った。

【０１０６】これにより、高濃度不純物領域３３３～３３６の一部は露呈し、絶縁膜３５６ａ～３５６ｄが形成される。

【０１０７】次いで、レジストからなるマスクを除去した後、新たにレジストからなるマスク３４８、３４９を形成して第３のドーピング処理を行う。この第３のドーピング処理により、ｐチャネル型ＴＦＴの活性層となる半導体層に前記一導電型（ｎ型）とは逆の導電型（ｐ型）を付与する不純物元素が添加された不純物領域３５０～３５３を形成する。（図９（Ｃ））第１の導電層３４０ａおよび３４２ａを不純物元素に対するマスクとして用い、ｐ型を付与する不純物元素を添加して自己整合的に不純物領域を形成する。

【０１０８】本実施例では、不純物領域３５０～３５３はジボラン（$B_2H_6$）を用いたイオンドープ法で形成する。なお、この第３のドーピング処理の際には、ｎチャネル型ＴＦＴを形成する半導体層はレジストからなるマスク３４８、３４９で覆われている。第１のドーピング処理及び第２のドーピング処理によって、不純物領域３５０～３５３にはそれぞれ異なる濃度でリンが添加されているが、そのいずれの領域においてもｐ型を付与する不純物元素の濃度が$2\times10^{20}$～$2\times10^{21}$atoms/cm$^3$となるようにドーピング処理することにより、ｐチャネル型ＴＦＴのソース領域およびドレイン領域として機能するために何ら問題は生じない。

【０１０９】以上までの工程でそれぞれの半導体層に不純物領域が形成される。

【０１１０】次いで、レジストからなるマスク３４８、３４９を除去して第１の層間絶縁膜３５７を形成する。この第１の層間絶縁膜３５７としては、プラズマＣＶＤ法またはスパッタ法を用い、厚さを１００～２００ｎｍとして珪素を含む絶縁膜で形成する。本実施例では、プラズマＣＶＤ法により膜厚１５０ｎｍの酸化窒化珪素膜を形成した。勿論、第１の層間絶縁膜３５７は酸化窒化珪素膜に限定されるものでなく、他の珪素を含む絶縁膜を単層または積層構造として用いても良い。

【０１１１】次いで、図１０（Ａ）に示すように、それぞれの半導体層に添加された不純物元素を活性化処理する工程を行う。この活性化工程はファーネスアニール炉を用いる熱アニール法で行う。熱アニール法としては、酸素濃度が１ｐｐｍ以下、好ましくは０．１ｐｐｍ以下の窒素雰囲気中で４００～７００℃、代表的には５００～５５０℃で行えばよく、本実施例では５５０℃、４時間の熱処理で活性化処理を行った。なお、熱アニール法の他に、レーザーアニール法、またはラピッドサーマルアニール法（ＲＴＡ法）を適用することができる。

【０１１２】なお、本実施例では、上記活性化処理と同時に、結晶化の際に触媒として使用したニッケルが高濃度のリンを含む不純物領域（３３４～３３６、３５０、３５１）にゲッタリングされ、主にチャネル形成領域となる半導体層中のニッケル濃度が低減される。このようにして作製したチャネル形成領域を有するＴＦＴはオフ電流値が下がり、結晶性が良いことから高い電界効果移動度が得られ、良好な特性を達成することができる。

【０１１３】また、第１の層間絶縁膜を形成する前に活性化処理を行っても良い。ただし、用いた配線材料が熱に弱い場合には、本実施例のように配線等を保護するため層間絶縁膜（シリコンを主成分とする絶縁膜、例えば窒化珪素膜）を形成した後で活性化処理を行うことが好ましい。

【０１１４】その他、活性化処理を行った後でドーピング処理を行い、第１の層間絶縁膜を形成させても良い。

【０１１５】さらに、３～１００％の水素を含む雰囲気中で、３００～５５０℃で１～１２時間の熱処理を行い、半導体層を水素化する工程を行う。本実施例では水素を約３％の含む窒素雰囲気中で４１０℃、１時間の熱処理を行った。この工程は層間絶縁膜に含まれる水素により半導体層のダングリングボンドを終端する工程である。水素化の他の手段として、プラズマ水素化（プラズマにより励起された水素を用いる）を行っても良い。

【０１１６】また、活性化処理としてレーザーアニール法を用いる場合には、上記水素化を行った後、エキシマレーザーやＹＡＧレーザー等のレーザー光を照射することが望ましい。

【０１１７】次いで、図１０（Ｂ）に示すように第１の層間絶縁膜３５７上に有機絶縁物材料から成る第２の層間絶縁膜３５８を形成する。本実施例では膜厚１．６μｍのアクリル樹脂膜を形成した。次いで、各不純物領域３３３、３３５、３５０、３５１に達するコンタクトホールを形成するためのパターニングを行う。

【０１１８】第２の層間絶縁膜３５８としては、珪素を含む絶縁材料や有機樹脂からなる膜を用いる。珪素を含む絶縁材料としては、酸化珪素、窒化珪素、酸化窒化珪素を用いることができ、また有機樹脂としては、ポリイミド、ポリアミド、アクリル、ＢＣＢ（ベンゾシクロブテン）などを用いることができる。

【０１１９】本実施例では、プラズマＣＶＤ法により形成された酸化窒化珪素膜を形成した。なお、酸化窒化珪素膜の膜厚として好ましくは１～５μｍ（さらに好ましくは２～４μｍ）とすればよい。酸化窒化珪素膜は、膜自身に含まれる水分が少ないためにＥＬ素子の劣化を抑える上で有効である。

【０１２０】また、コンタクトホールの形成には、ドライエッチングまたはウエットエッチングを用いることができるが、エッチング時における静電破壊の問題を考えると、ウエットエッチング法を用いるのが望ましい。

【０１２１】さらに、ここでのコンタクトホールの形成において、第１層間絶縁膜及び第２層間絶縁膜を同時にエッチングするため、コンタクトホールの形状を考えると第２層間絶縁膜を形成する材料は、第１層間絶縁膜を形成する材料よりもエッチング速度の速いものを用いるのが好ましい。

【０１２２】そして、各不純物領域３３３、３３５、３５０、３５１とそれぞれ電気的に接続する配線３５９～３６６を形成する。そして、膜厚５０ｎｍのＴｉ膜と、膜厚５００ｎｍの合金膜（ＡｌとＴｉとの合金膜）との積層膜をパターニングして形成するが、他の導電膜を用いても良い。

【０１２３】次いで、その上に透明導電膜を８０～１２０nmの厚さで形成し、パターニングすることによって透明電極３６７を形成する。（図１０（Ｂ））

【０１２４】なお、本実施例では、透明電極として酸化インジウム・スズ（ＩＴＯ）膜や酸化インジウムに２～２０[%]の酸化亜鉛（ＺｎＯ）を混合した透明導電膜を用いる。

【０１２５】また、透明電極３６７は、ドレイン配線３６５と接して重ねて形成することによってＥＬ駆動用ＴＦＴのドレイン領域と電気的な接続が形成される。

【０１２６】次に、図１１に示すように、珪素を含む絶縁膜（本実施例では酸化珪素膜）を５００[nm]の厚さに形成し、透明電極３６７に対応する位置に開口部を形成して、バンクとして機能する第３の層間絶縁膜３６８を形成する。開口部を形成する際、ウエットエッチング法を用いることで容易にテーパー形状の側壁とすることが出来る。開口部の側壁が十分になだらかでないと段差に起因するＥＬ層の劣化が顕著な問題となってしまうため、注意が必要である。

【０１２７】なお、本実施例においては、第３の層間絶縁膜として酸化珪素でなる膜を用いているが、場合によっては、ポリイミド、ポリアミド、アクリル、ＢＣＢ（ベンゾシクロブテン）といった有機樹脂膜を用いることもできる。

【０１２８】次に、図１１で示すようにＥＬ層３６９を蒸着法により形成し、更に蒸着法により陰極（ＭｇＡｇ電極）３７０および保護電極３７１を形成する。このときＥＬ層３６９及び陰極３７０を形成するに先立って透明電極３６７に対して熱処理を施し、水分を完全に除去しておくことが望ましい。なお、本実施例ではＥＬ素子の陰極としてＭｇＡｇ電極を用いるが、公知の他の材料であっても良い。

【０１２９】なお、ＥＬ層３６９としては、公知の材料を用いることができる。本実施例では正孔輸送層（Hole transporting layer）及び発光層（Emitting layer）でなる２層構造をＥＬ層とするが、正孔注入層、電子注入層若しくは電子輸送層のいずれかを設ける場合もある。このように組み合わせは既に様々な例が報告されており、そのいずれの構成を用いても構わない。

【０１３０】本実施例では正孔輸送層としてポリフェニレンビニレンを蒸着法により形成する。また、発光層としては、ポリビニルカルバゾールに１，３，４－オキサジアゾール誘導体のＰＢＤを３０～４０％分子分散させたものを蒸着法により形成し、緑色の発光中心としてクマリン６を約１％添加している。

【０１３１】また、保護電極３７１でもＥＬ層３６９を

水分や酸素から保護することは可能であるが、さらに好ましくはパッシベーション膜３７２を設けると良い。本実施例ではパッシベーション膜３７２として３００ｎｍ厚の窒化珪素膜を設ける。このパッシベーション膜も保護電極３７１の後に大気解放しないで連続的に形成しても構わない。

【０１３２】また、保護電極３７１は陰極３７０の劣化を防ぐために設けられ、アルミニウムを主成分とする金属膜が代表的である。勿論、他の材料でも良い。また、ＥＬ層３６９、陰極３７０は非常に水分に弱いので、保護電極３７１までを大気解放しないで連続的に形成し、外気からＥＬ層を保護することが望ましい。

【０１３３】なお、ＥＬ層３６９の膜厚は１０～４００[nm]（典型的には６０～１５０[nm]）、陰極３７０の厚さは８０～２００[nm]（典型的には１００～１５０[nm]）とすれば良い。

【０１３４】こうして図１１に示すような構造のＥＬ表示装置が完成する。なお、本実施例におけるＥＬ表示装置の作成工程においては、回路の構成および工程の関係上、ゲート電極を形成している材料であるＴａ、Ｗによってソース信号線を形成し、ソース、ドレイン電極を形成している配線材料であるＡｌによってゲート信号線を形成しているが、異なる材料を用いても良い。

【０１３５】また、ｎチャネル型ＴＦＴ５０１及びｐチャネル型ＴＦＴ５０２を有する駆動回路５０６と、スイッチング用ＴＦＴ５０３及びＥＬ駆動用ＴＦＴ５０４を有する画素部５０７を同一基板上に形成することができる。

【０１３６】駆動回路５０６のｎチャネル型ＴＦＴ５０１はチャネル形成領域３８０、ゲート電極の一部を構成する第１の導電層３２４ａと重なる低濃度不純物領域３２９（ＧＯＬＤ領域）とソース領域またはドレイン領域として機能する高濃度不純物領域３３３を有している。ｐチャネル型ＴＦＴ５０２にはチャネル形成領域３７３、ゲート電極の一部を構成する第１の導電層３４０ａと重ならない不純物領域３５２、ソース領域またはドレイン領域として機能する不純物領域３５０を有している。

【０１３７】画素部５０７のスイッチング用ＴＦＴ５０３にはチャネル形成領域３７４、ゲート電極を形成する第１の導電層３４１ａと重ならず、ゲート電極の外側に形成される低濃度不純物領域３４４（ＬＤＤ領域）とソース領域またはドレイン領域として機能する高濃度不純物領域３３５を有している。

【０１３８】画素部５０７のＥＬ駆動用ＴＦＴ５０４にはチャネル形成領域３７５、ゲート電極の一部を構成する第１の導電層３２７ａと重ならない不純物領域３５３、ソース領域またはドレイン領域として機能する高濃度不純物領域３５１を有している。

【０１３９】（実施例６）本実施例では、本発明を用いてＥＬ表示装置を作製した例について、図１６、図１７を用いて説明する。

【０１４０】図１６（Ａ）は本発明のＥＬ表示装置のＴＦＴ基板の上面図を示している。なお本明細書においてＴＦＴ基板とは、画素部が設けられている基板を意味する。

【０１４１】基板４００１上に、画素部４００２と、ソース信号線駆動回路４００３と、第１のゲート信号線駆動回路４００４ａと、第２のゲート信号線駆動回路４００４ｂとが設けられている。なお本発明においてソース信号線駆動回路とゲート信号線駆動回路の数は図１６（Ａ）に示した数に限定されない。ソース信号線駆動回路とゲート信号線駆動回路の数は、設計者が適宜設定することが可能である。また、本実施例ではソース信号線駆動回路とゲート信号線駆動回路とをＴＦＴ基板上に設けているが、本発明はこの構成に限定されない。ＴＦＴ基板とは別の基板上に設けたソース信号線駆動回路とゲート信号線駆動回路とを、ＦＰＣ、ＴＡＢ等の外部接続端子により画素部と電気的に接続するようにしても良い。

【０１４２】４００５ａは画素部４００２に設けられた電源供給線（図示せず）に接続された引き回し配線である。４００５ｂは第１及び第２のゲート信号線駆動回路４００４ａ、４００４ｂに接続されたゲート用引き回し配線である。また４００５ｃはソース信号線駆動回路４００３に接続されたソース用引き回し配線である。

【０１４３】ゲート用引き回し配線４００５ｂと、ソース用引き回し配線４００５ｃとは、基板４００１の外部に設けられたＩＣ等に、ＦＰＣ４００６を介して接続されている。また引き回し配線４００５ａは、基板４００１の外部に設けられた電源にＦＰＣ４００６を介して接続されている。

【０１４４】引き回し配線４００５ａの拡大図を図１６（Ｂ）に示す。４１００はＲ用引き回し配線、４１０１はＧ用引き回し配線、４１０２はＢ用引き回し配線である。

【０１４５】Ｒ用ＥＬ素子のＥＬ層の電流密度と、Ｇ用ＥＬ素子のＥＬ層の電流密度と、Ｂ用ＥＬ素子のＥＬ層の電流密度の比が１．１５：１．２９：１とすると、本発明ではＲ用引き回し配線４１００の幅Ｗｒと、Ｇ用引き回し配線４１０１の幅Ｗｇと、Ｂ用引き回し配線４１０２の幅Ｗｂは、Ｗｇ＞Ｗｒ＞Ｗｂであることが重要である。実施の形態において示した式３より、より好ましくはＷｒ：Ｗｇ：Ｗｂ≒１．１５：１．２９：１であることが望ましい。

【０１４６】本発明の上記構成によって、白表示の画素の数に関わりなく、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることが可能になる。

【０１４７】図１７（Ａ）は、図１６（Ａ）に示したＴＦＴ基板をシーリング材によって封止することによって

形成されたＥＬ表示装置の上面図であり、図１７（Ｂ）は、図１７（Ａ）のＡ－Ａ’における断面図、図１７（Ｃ）は図１７（Ａ）のＢ－Ｂ’における断面図である。なお図１６において既に示したものは、同じ符号を用いて示す。

【０１４８】基板４００１上に設けられた画素部４００２と、ソース信号線駆動回路４００３と、第１及び第２のゲート信号線駆動回路４００４ａ、ｂとを囲むようにして、シール材４００９が設けられている。また画素部４００２と、ソース信号線駆動回路４００３と、第１及び第２のゲート信号線駆動回路４００４ａ、ｂとの上にシーリング材４００８が設けられている。よって画素部４００２と、ソース信号線駆動回路４００３と、第１及び第２のゲート信号線駆動回路４００４ａ、ｂとは、基板４００１とシール材４００９とシーリング材４００８とによって、充填材４２１０で密封されている。

【０１４９】また基板４００１上に設けられた画素部４００２と、ソース信号線駆動回路４００３と、第１及び第２のゲート信号線駆動回路４００４ａ、ｂとは、複数のＴＦＴを有している。図１７（Ｂ）では代表的に、下地膜４０１０上に形成された、ソース信号線駆動回路４００３に含まれる駆動ＴＦＴ（但し、ここではｎチャネル型ＴＦＴとｐチャネル型ＴＦＴを図示する）４２０１及び画素部４００２に含まれるＥＬ駆動用ＴＦＴ（ＥＬ素子に流れる電流を制御するＴＦＴ）４２０２を図示した。

【０１５０】本実施例では、駆動ＴＦＴ４２０１にには公知の方法で作製されたｐチャネル型ＴＦＴまたはｎチャネル型ＴＦＴが用いられ、ＥＬ駆動用ＴＦＴ４２０２には公知の方法で作製されたｐチャネル型ＴＦＴが用いられる。また、画素部４００２にはＥＬ駆動用ＴＦＴ４２０２のゲートに接続された保持容量（図示せず）が設けられる。

【０１５１】駆動ＴＦＴ４２０１及びＥＬ駆動用ＴＦＴ４２０２上には層間絶縁膜（平坦化膜）４３０１が形成され、その上にＥＬ駆動用ＴＦＴ４２０２のドレインと電気的に接続する画素電極（陽極）４２０３が形成される。画素電極４２０３としては仕事関数の大きい透明導電膜が用いられる。透明導電膜としては、酸化インジウムと酸化スズとの化合物、酸化インジウムと酸化亜鉛との化合物、酸化亜鉛、酸化スズまたは酸化インジウムを用いることができる。また、前記透明導電膜にガリウムを添加したものを用いても良い。

【０１５２】そして、画素電極４２０３の上には絶縁膜４３０２が形成され、絶縁膜４３０２は画素電極４２０３の上に開口部が形成されている。この開口部において、画素電極４２０３の上にはＥＬ（エレクトロルミネッセンス）層４２０４が形成される。ＥＬ層４２０４は公知の有機ＥＬ材料または無機ＥＬ材料を用いることができる。また、有機ＥＬ材料には低分子系（モノマー系）材料と高分子系（ポリマー系）材料があるがどちらを用いても良い。



【０１５３】ＥＬ層４２０４の形成方法は公知の蒸着技術もしくは塗布法技術を用いれば良い。また、ＥＬ層の構造は正孔注入層、正孔輸送層、発光層、電子輸送層または電子注入層を自由に組み合わせて積層構造または単層構造とすれば良い。

【０１５４】ＥＬ層４２０４の上には遮光性を有する導電膜（代表的にはアルミニウム、銅もしくは銀を主成分とする導電膜またはそれらと他の導電膜との積層膜）からなる陰極４２０５が形成される。また、陰極４２０５とＥＬ層４２０４の界面に存在する水分や酸素は極力排除しておくことが望ましい。従って、ＥＬ層４２０４を窒素または希ガス雰囲気で形成し、酸素や水分に触れさせないまま陰極４２０５を形成するといった工夫が必要である。本実施例ではマルチチャンバー方式（クラスターツール方式）の成膜装置を用いることで上述のような成膜を可能とする。そして陰極４２０５は所定の電圧が与えられている。

【０１５５】以上のようにして、画素電極（陽極）４２０３、ＥＬ層４２０４及び陰極４２０５からなるＥＬ素子４３０３が形成される。そしてＥＬ素子４３０３を覆うように、絶縁膜４３０２上に保護膜４３０３が形成されている。保護膜４３０３は、ＥＬ素子４３０３に酸素や水分等が入り込むのを防ぐのに効果的である。

【０１５６】４００５ａは電源供給線に接続された引き回し配線であり、ＥＬ駆動用ＴＦＴ４２０２のソース領域に電気的に接続されている。引き回し配線４００５ａはシール材４００９と基板４００１との間を通り、異方導電性フィルム４３００を介してＦＰＣ４００６が有するＦＰＣ用配線４３０１に電気的に接続される。

【０１５７】シーリング材４００８としては、ガラス材、金属材（代表的にはステンレス材）、セラミックス材、プラスチック材（プラスチックフィルムも含む）を用いることができる。プラスチック材としては、ＦＲＰ（Ｆｉｂｅｒｇｌａｓｓ－Ｒｅｉｎｆｏｒｃｅｄ Ｐｌａｓｔｉｃｓ）板、ＰＶＦ（ポリビニルフルオライド）フィルム、マイラーフィルム、ポリエステルフィルムまたはアクリル樹脂フィルムを用いることができる。また、アルミニウムホイルをＰＶＦフィルムやマイラーフィルムで挟んだ構造のシートを用いることもできる。

【０１５８】但し、ＥＬ素子からの光の放射方向がカバー材側に向かう場合にはカバー材は透明でなければならない。その場合には、ガラス板、プラスチック板、ポリエステルフィルムまたはアクリルフィルムのような透明物質を用いる。

【０１５９】また、充填材４２１０としては窒素やアルゴンなどの不活性な気体の他に、紫外線硬化樹脂または熱硬化樹脂を用いることができ、ＰＶＣ（ポリビニルクロライド）、アクリル、ポリイミド、エポキシ樹脂、シ

リコーン樹脂、ＰＶＢ（ポリビニルブチラル）またはＥＶＡ（エチレンビニルアセテート）を用いることができる。本実施例では充填材として窒素を用いた。

【０１６０】また充填材４２１０を吸湿性物質（好ましくは酸化バリウム）もしくは酸素を吸着しうる物質にさらしておくために、シーリング材４００８の基板４００１側の面に凹部４００７を設けて吸湿性物質または酸素を吸着しうる物質４２０７を配置する。そして、吸湿性物質または酸素を吸着しうる物質４２０７が飛び散らないように、凹部カバー材４２０８によって吸湿性物質または酸素を吸着しうる物質４２０７は凹部４００７に保持されている。なお凹部カバー材４２０８は目の細かいメッシュ状になっており、空気や水分は通し、吸湿性物質または酸素を吸着しうる物質４２０７は通さない構成になっている。吸湿性物質または酸素を吸着しうる物質４２０７を設けることで、ＥＬ素子４３０３の劣化を抑制できる。

【０１６１】図１７（Ｃ）に示すように、画素電極４２０３が形成されると同時に、引き回し配線４００５ａ上に接するように導電性膜４２０３ａが形成される。

【０１６２】また、異方導電性フィルム４３００は導電性フィラー４３００ａを有している。基板４００１とＦＰＣ４００６とを熱圧着することで、基板４００１上の導電性膜４２０３ａとＦＰＣ４００６上のＦＰＣ用配線４３０１とが、導電性フィラー４３００ａによって電気的に接続される。

【０１６３】本実施例は、実施例１～実施例５と自由に組み合わせて実施することが可能である。

（実施例７）本実施例では、基板上にＴＦＴとＥＬ素子とをシーリング材で封止した後、基板を付けかえる例について、図１８を用いて説明する。なお、図１８に示したのは画素部における作製工程を示す断面図である。

【０１６４】図１８（Ａ）において、３１０１は素子が形成される基板（以下、素子形成基板という）であり、その上には非晶質シリコン膜からなる剥離層３１０２が１００～５００ｎｍ（本実施例では３００ｎｍ）の厚さに形成される。本実施例では素子形成基板３１０１としてガラス基板を用いるが、石英基板、シリコン基板、金属基板（ＳＵＳ基板）もしくはセラミックス基板を用いても構わない。

【０１６５】また、剥離層３１０２の成膜は減圧熱ＣＶＤ法、プラズマＣＶＤ法、スパッタ法もしくは蒸着法を用いれば良い。剥離層３１０２の上には酸化シリコン膜からなる絶縁膜３１０３が２００ｎｍの厚さに形成される。絶縁膜３１０３の形成は減圧熱ＣＶＤ法、プラズマＣＶＤ法、スパッタ法もしくは蒸着法を用いれば良い。

【０１６６】また、絶縁膜３１０３の上には画素部のスイッチング用ＴＦＴ３１０４及びＥＬ駆動用ＴＦＴ３１０５が形成されている。なお本実施例では、スイッチング用ＴＦＴ３１０４がｎチャネル型ＴＦＴでＥＬ駆動用ＴＦＴ３１０５がｐチャネル型ＴＦＴである例を示したが、本実施例はこの構成に限定されない。スイッチング用ＴＦＴ３１０４とＥＬ駆動用ＴＦＴ３１０５はｐチャネル型ＴＦＴとｎチャネル型ＴＦＴのどちらでも良い。

【０１６７】また本実施例では、スイッチング用ＴＦＴ３１０４がダブルゲート構造になっているが、スイッチング用ＴＦＴはこの構造に限定されず、シングルゲート構造またはその他のマルチゲート構造であっても良い。本実施例のようにダブルゲート構造とすることで、二つのチャネル形成領域が直列に接続された構造となり、オフ電流値（ＴＦＴがオフされた時に流れる電流）を効果的に抑制することができる。

【０１６８】スイッチング用ＴＦＴ３１０４及びＥＬ駆動用ＴＦＴ３１０５上に、第１層間絶縁膜３１０７が形成されている。第１層間絶縁膜３１０７は後に形成される画素電極３１０６が平坦化するように、スイッチング用ＴＦＴ３１０４及びＥＬ駆動用ＴＦＴ３１０５を覆って形成される

【０１６９】また、ＥＬ駆動用ＴＦＴ３１０５のドレイン領域に電気的に接続するように、画素電極３１０６が形成される。本実施例において画素電極３１０６は、透明導電膜（代表的には酸化インジウムと酸化スズとの化合物膜）を１００ｎｍの厚さに形成し、パターニングにより形成される。画素電極３１０６はＥＬ素子の陽極として機能する。

【０１７０】画素電極３１０６を形成した後、酸化シリコン膜からなる第２層間絶縁膜３１１４が３００ｎｍの厚さに形成される。そして、開口部３１０８を形成し、７０ｎｍ厚のＥＬ層３１０９及び３００ｎｍ厚の陰極３１１０を蒸着法により形成する。本実施例ではＥＬ層３１０９として２０ｎｍ厚の正孔注入層及び５０ｎｍ厚の発光層を積層した構造を用いる。勿論、発光層に正孔注入層、正孔輸送層、電子輸送層もしくは電子注入を組み合わせた公知の他の構造を用いても良い。

【０１７１】以上のようにして、画素電極（陽極）３１０６、ＥＬ層３１０９及び陰極３１１０からなるＥＬ素子３１１１が形成される。本実施例ではこのＥＬ素子３１１１が発光素子として機能する。

【０１７２】次に、第１接着剤３１１２により素子を固定するための基板（以下、シーリング材という）３１１３を貼り合わせる。本実施例ではシーリング材３１１３として可撓性のプラスチックフィルムを用いるが、ガラス基板、石英基板、プラスチック基板、シリコン基板もしくはセラミックス基板を用いても良い。また、第１接着剤３１１２としては、後に剥離層３１０２を除去する際に選択比のとれる材料を用いる必要がある。

【０１７３】代表的には樹脂からなる絶縁膜を用いることができ、本実施例ではポリイミドを用いるが、アクリル、ポリアミドもしくはエポキシ樹脂を用いても良い。なお、ＥＬ素子から見て観測者側（発光装置の使用者

側）に位置する場合は、光を透過する材料であることが必要である。

【０１７４】第１接着剤３１１２により、ＥＬ素子を完全に大気から遮断することができる。これにより酸化による有機ＥＬ材料の劣化をほぼ完全に抑制することができ、ＥＬ素子の信頼性を大幅に向上させることができる。

【０１７５】次に、図１８（Ｂ）に示すように、剥離層３１０２を除去し、素子形成基板３１０１と絶縁膜３１０３とを剥離する。本実施例ではフッ化ハロゲンを含むガス中に剥離層３１０２を晒し、剥離を行う。本実施例ではフッ化ハロゲンとして三フッ化塩素（$ClF_3$）を用い、希釈ガスとして窒素を用いる。希釈ガスとしては、アルゴン、ヘリウムもしくはネオンを用いても良い。流量は共に５００ｓｃｃｍ（$8.35\times10^{-6}m^3/s$）とし、反応圧力は１～１０Ｔｏｒｒ（$1.3\times10^{2}$～$1.3\times10^{3}$Ｐａ）とすれば良い。また、処理温度は室温（典型的には２０～２７℃）で良い。

【０１７６】この場合、シリコン膜はエッチングされるが、プラスチックフィルム、ガラス基板、ポリイミド膜、酸化シリコン膜はエッチングされない。即ち、三フッ化塩素ガスに晒すことで剥離層３１０２が選択的にエッチングされ、最終的には完全に除去される。なお、同じくシリコン膜で形成されているスイッチング用ＴＦＴ３１０４及びＥＬ駆動用ＴＦＴ３１０５の活性層は第１層間絶縁膜３１０７に覆われているため三フッ化塩素ガスに晒されることがなく、エッチングされることはない。

【０１７７】本実施例の場合、剥離層３１０２は露呈した端部から徐々にエッチングされていき、完全に除去された時点で素子形成基板３１０１と絶縁膜３１０３が分離される。このとき、ＴＦＴ及びＥＬ素子は薄膜を積層して形成されているが、シーリング材３１１３に移された形で残る。

【０１７８】なお、ここでは剥離層３１０２が端部からエッチングされていくことになるが、素子形成基板３１０１が大きくなると完全に除去されるまでの時間が長くなり好ましいものではない。従って、エッチングで除去する場合は素子形成基板３１０１が対角３インチ以下（好ましくは対角１インチ以下）の場合に実施することが望ましい。

【０１７９】なお本実施例では剥離層３１０２を三フッ化塩素ガス雰囲気下においてエッチングすることで除去したが、本実施例はこの構成に限定されない。素子形成基板３１０１側から剥離層３１０２にレーザー光を照射し、剥離層３１０２を気化させることで素子形成基板３１０１を剥離するようにしても良い。この場合、レーザー光が素子形成基板３１０１を通過するように、レーザー光の種類と素子形成基板３１０１の材質とを適宜選択する必要がある。例えば素子形成基板３１０１に石英基板を用いるならば、ＹＡＧレーザー（基本波（１０６４ｎｍ）、第２高調波（５３２ｎｍ）、第３高調波（３５５ｎｍ）、第４高調波（２６６ｎｍ））あるいはエキシマレーザー（波長３０８ｎｍ）を用い、線状ビームを形成し、石英基板を通過させれば良い。なお、エキシマレーザーはガラス基板を通過しない。したがって、素子形成基板３１０１としてガラス基板を用いるのであれば、ＹＡＧレーザーの基本波、第２高調波、第３高調波を用い、好ましくは第２高調波（波長５３２ｎｍ）を用いて線状ビームを形成し、ガラス基板を通過させれば良い。

【０１８０】またレーザー光を用いて剥離を行う場合、剥離層３１０２として照射するレーザー光で気化するものを用いる。

【０１８１】また、レーザー光を用いる方法のほかに、剥離層３１０２を溶液によって溶解させることで素子形成基板３１０１を剥離するようにしても良い。この場合、剥離層３１０２だけが選択的に溶解するような溶液を用いることが好ましい。

【０１８２】こうしてシーリング材３１１３にＴＦＴ及びＥＬ素子を移したら、図１８（Ｃ）に示すように、第２接着剤３１１４を形成し、第２素子形成基板３１１５を貼り合わせる。第２接着剤３１１４としては樹脂からなる絶縁膜（代表的にはポリイミド、アクリル、ポリアミドもしくはエポキシ樹脂）を用いても良いし、無機絶縁膜（代表的には酸化シリコン膜）を用いても良い。なお、ＥＬ素子から見て観測者側に位置する場合は、光を透過する材料であることが必要である。

【０１８３】こうして素子形成基板３１０１から第２素子形成基板３１１５へとＴＦＴ及びＥＬ素子が移される。その結果、シーリング材３１１３、と第２素子形成基板３１１５によって挟まれたＥＬ表示装置を得ることができる。ここでシーリング材３１１３と第２素子形成基板３１１５を同一材料とすると熱膨張係数が等しくなるので、温度変化による応力歪みの影響を受けにくくすることができる。

【０１８４】本実施例により作製されたＥＬ表示装置は、シーリング材３１１３と第２素子形成基板３１１５の材料を、ＴＦＴのプロセス時における耐熱性に左右されることなく選択することができる。例えばシーリング材３１１３と第２素子形成基板３１１５としてプラスチック基板を用いることができ、フレキシブルなＥＬ表示装置を作成することも可能である。

【０１８５】なお本実施例は、実施例１～６に示した構成と、自由に組み合わせて実施することが可能である。

【０１８６】（実施例８）本実施例では、ＥＬ表示装置の表面全体またはＥＬ表示装置の端部に、ＤＬＣ膜を形成する例について説明する。

【０１８７】図１９（Ａ）は表面全体にＤＬＣ膜を形成したＥＬ表示装置の断面図である。基板３２０１上にスイッチング用ＴＦＴ３２０５と、ＥＬ駆動用ＴＦＴ３２

０４とが形成されている。３２０３はＥＬ素子であり、ＥＬ駆動用ＴＦＴ３２０４によってＥＬ素子３２０３に流れる電流が制御される。

【０１８】スイッチング用ＴＦＴ３２０５、ＥＬ駆動用ＴＦＴ３２０４及びＥＬ素子３２０３はシーリング材３２０２とシール材３２０８によって密封されており、外気から遮断されている。３２０９は引き回し配線であり、シール材３２０８と基板３２０１との間を通って、ＥＬ素子３２０３が密封された空間の外に露出している。

【０１８９】３２１０はＤＬＣ膜であり、ＥＬ素子３２０３が密封された空間の外に露出している引き回し配線３２０９の一部を除いて、ＥＬ表示装置全体を覆っている。

【０１９０】なお本実施例においてＤＬＣ膜の成膜は、ＥＣＲプラズマＣＶＤ法、ＲＦプラズマＣＶＤ法、μ波プラズマＣＶＤ法もしくはスパッタ法を用いれば良い。ＤＬＣ膜の特徴としては、１５５０ｃｍ$^{-1}$くらいに非対称のピークを有し、１３００ｃｍ$^{-1}$ぐらいに肩を持つラマンスペクトル分布を有する。また微小硬度計で測定した時に１５～２５ＧＰａの硬度を示すという特徴をもつ。このような炭素膜は基板の表面を保護する特徴を有する。特にプラスチック基板の場合、傷がつきやすいことから、図１９（Ａ）のように表面をＤＬＣ膜で覆うことは傷を防ぐのに有効である。

【０１９１】またＤＬＣ膜は、酸素および水の進入を防ぐのに有効である。よって本実施例のようにシール材３２０８を覆うようにＤＬＣ膜３２１０を形成することによって、外部からの水分や酸素等の、ＥＬ層の劣化を促す物質が、ＥＬ素子３２０３が密封されている空間に進入するのを防ぐことができる。

【０１９２】なお、ＤＬＣ膜３２１０を形成する際に、ＥＬ素子３２０３が密封された空間の外に露出している引き回し配線３２０９の一部を、レジストマスク等で覆うようにし、ＤＬＣ膜３２１０形成後該レジストマスクを除去する。ＤＬＣ膜３２１０に覆われていない引き回し配線３２０９の一部は、異方性導電膜３２１３によって、ＦＰＣ３２１１に設けられたＦＰＣ用配線３２１１に接続される。

【０１９３】図１９（Ｂ）は、ＥＬ表示装置の端部にＤＬＣ膜を形成した場合の、ＥＬ表示装置の断面図である。基板３３０１上にスイッチング用ＴＦＴ３３０５と、ＥＬ駆動用ＴＦＴ３３０４とが形成されている。３３０３はＥＬ素子であり、ＥＬ駆動用ＴＦＴ３３０４によってＥＬ素子３３０３に流れる電流が制御される。

【０１９４】スイッチング用ＴＦＴ３３０５、ＥＬ駆動用ＴＦＴ３３０４及びＥＬ素子３３０３はシーリング材３３０２とシール材３３０８によって密封されており、外気から遮断されている。３３０９は引き回し配線であり、シール材３３０８と基板３３０１との間を通って、ＥＬ素子３３０３が密封された空間の外に露出している。

【０１９５】３３１０はＤＬＣ膜であり、ＥＬ素子３３０３が密封された空間の外に露出している引き回し配線３３０９の一部を除いて、シーリング材３３０２の一部と、基板３３０１の一部と、シール材３３０８とを覆って形成されている。

【０１９６】ＤＬＣ膜３３１０は、酸素および水の進入を防ぐのに有効である。よって本実施例のようにシール材３３０８を覆うようにＤＬＣ膜３３１０を形成することによって、外部からの水分や酸素等の、ＥＬ層の劣化を促す物質が、ＥＬ素子３３０３が密封されている空間に進入するのを防ぐことができる。

【０１９７】図１９（Ｂ）で示したＥＬ表示装置は、ＥＬ表示装置の端部（シール材を含む部分）にのみＤＬＣ膜３３１０を形成しているので、ＤＬＣ膜３３１０の成膜が容易である。

【０１９８】なお、ＤＬＣ膜３３１０を形成する際に、ＥＬ素子３３０３が密封された空間の外に露出している引き回し配線３３０９の一部を、レジストマスク等で覆うようにし、ＤＬＣ膜３３１０形成後該レジストマスクを除去する。ＤＬＣ膜３３１０に覆われていない引き回し配線３３０９の一部は、異方性導電膜３３１３によって、ＦＰＣ３３１１に設けられたＦＰＣ用配線３３１１に接続される。

【０１９９】なお本実施例は、実施例１～７に示した構成と、自由に組み合わせて実施することが可能である。

【０２００】（実施例９）本発明を実施して形成されたＥＬ表示装置は、自発光型であるため液晶表示装置に比べて明るい場所での視認性に優れ、しかも視野角が広い。従って、様々な電子機器の表示部に用いることができる。例えば、ＴＶ放送等を大画面で鑑賞するには対角３０インチ以上（典型的には４０インチ以上）のＥＬディスプレイ（ＥＬ表示装置を筐体に組み込んだ電子機器）の表示部として本発明のＥＬ表示装置を用いるとよい。

【０２０１】なお、ＥＬ表示装置には、パソコン用ディスプレイ、ＴＶ放送受信用ディスプレイ、広告表示用ディスプレイ等の全ての情報表示用ディスプレイが含まれる。また、その他にも様々な電子機器の表示部として本発明のＥＬ表示装置を用いることができる。

【０２０２】その様な本発明の電子機器としては、ビデオカメラ、デジタルカメラ、ゴーグル型ディスプレイ（ヘッドマウントディスプレイ）、ナビゲーションシステム、音響再生装置（カーオーディオ、オーディオコンポ等）、ノート型パーソナルコンピュータ、ゲーム機器、携帯情報端末（モバイルコンピュータ、携帯電話、携帯型ゲーム機または電子書籍等）、記録媒体を備えた画像再生装置（具体的にはDigital Versatile Disc（ＤＶＤ）等の記録媒体を再生し、その画像を表示しうるデ

ィスプレイを備えた装置）などが挙げられる。特に、斜め方向から見ることの多い携帯情報端末は視野角の広さが重要視されるため、ＥＬ表示装置を用いることが望ましい。それら電子機器の具体例を図１２、図１３に示す。

【０２０３】図１２（Ａ）はＥＬディスプレイであり、筐体２００１、支持台２００２、表示部２００３等を含む。本発明のＥＬ表示装置は表示部２００３に用いることができる。ＥＬ表示装置は自発光型であるためバックライトが必要なく、液晶表示装置よりも薄い表示部とすることができる。

【０２０４】図１２（Ｂ）はビデオカメラであり、本体２１０１、表示部２１０２、音声入力部２１０３、操作スイッチ２１０４、バッテリー２１０５、受像部２１０６等を含む。本発明のＥＬ表示装置は表示部２１０２に用いることができる。

【０２０５】図１２（Ｃ）は頭部取り付け型の発光装置の一部（右片側）であり、本体２２０１、信号ケーブル２２０２、頭部固定バンド２２０３、スクリーン部２２０４、光学系２２０５、表示部２２０６等を含む。本発明のＥＬ表示装置は表示部２２０６に用いることができる。

【０２０６】図１２（Ｄ）は記録媒体を備えた画像再生装置（具体的にはＤＶＤ再生装置）であり、本体２３０１、記録媒体（ＤＶＤ等）２３０２、操作スイッチ２３０３、表示部（ａ）２３０４、表示部（ｂ）２３０５等を含む。表示部（ａ）２３０４は主として画像情報を表示し、表示部（ｂ）２３０５は主として文字情報を表示するが、本発明のＥＬ表示装置はこれら表示部（ａ）、（ｂ）２３０４、２３０５に用いることができる。なお、記録媒体を備えた画像再生装置には家庭用ゲーム機器なども含まれる。

【０２０７】図１２（Ｅ）はゴーグル型ディスプレイ（ヘッドマウントディスプレイ）であり、本体２４０１、表示部２４０２、アーム部２４０３を含む。本発明のＥＬ表示装置は表示部２４０２に用いることができる。

【０２０８】図１２（Ｆ）はパーソナルコンピュータであり、本体２５０１、筐体２５０２、表示部２５０３、キーボード２５０４等を含む。本発明のＥＬ表示装置は表示部２５０３に用いることができる。

【０２０９】なお、将来的にＥＬ材料の発光輝度が高くなれば、出力した画像情報を含む光をレンズ等で拡大投影してフロント型若しくはリア型のプロジェクターに用いることも可能となる。

【０２１０】また、上記電子機器はインターネットやＣＡＴＶ（ケーブルテレビ）などの電子通信回線を通じて配信された情報を表示することが多くなり、特に動画情報を表示する機会が増してきている。ＥＬ材料の応答速度は非常に高いため、ＥＬ表示装置は動画表示に好ましい。

【０２１１】また、ＥＬ表示装置は発光している部分が電力を消費するため、発光部分が極力少なくなるように情報を表示することが望ましい。従って、携帯情報端末、特に携帯電話や音響再生装置のような文字情報を主とする表示部にＥＬ表示装置を用いる場合には、非発光部分を背景として文字情報を発光部分で形成するように駆動することが望ましい。

【０２１２】図１３（Ａ）は携帯電話であり、本体２６０１、音声出力部２６０２、音声入力部２６０３、表示部２６０４、操作スイッチ２６０５、アンテナ２６０６を含む。本発明のＥＬ表示装置は表示部２６０４に用いることができる。なお、表示部２６０４は黒色の背景に白色の文字を表示することで携帯電話の消費電力を抑えることができる。

【０２１３】また、図１３（Ｂ）は音響再生装置、具体的にはカーオーディオであり、本体２７０１、表示部２７０２、操作スイッチ２７０３、２７０４を含む。本発明のＥＬ表示装置は表示部２７０２に用いることができる。また、本実施例では車載用オーディオを示すが、携帯型や家庭用の音響再生装置に用いても良い。なお、表示部２７０２は黒色の背景に白色の文字を表示することで消費電力を抑えられる。これは携帯型の音響再生装置において特に有効である。

【０２１４】以上の様に、本発明の適用範囲は極めて広く、あらゆる分野の電子機器に用いることが可能である。また、本実施例の電子機器は実施例１～８に示したいずれの構成のＥＬ表示装置を用いても良い。

【０２１５】

【発明の効果】

【０２１６】本発明の構成によって、白表示の画素の数に関わりなく、Ｒ、Ｇ、Ｂの各画素の発光輝度のバランスを整えることが可能になる。

【０２１７】また本発明では、ＥＬ素子に大きい電圧がかかる画素は、入力するビデオ信号の振幅を大きくしても良い。上記構成によって、電源供給線の電圧を高くした際に、ＥＬ駆動用ＴＦＴのオフ電流が増加するのを防ぐことができる。

【０２１８】また同時に、電流の絶対値が大きい電源供給線に接続されている画素のＥＬ駆動用ＴＦＴのチャネル幅（Ｗ）をより大きくしても良い。本発明は上記構成により、電源供給線を流れる電流の絶対値が大きくなることによってＥＬ駆動用ＴＦＴが制御する電流の量が増えても、ＥＬ駆動用ＴＦＴの劣化を抑えることができる。そしてなおかつ、ＥＬ素子に印加される電圧の値によって、そのＥＬ素子の発光輝度を調節することが可能になり、赤色、青色、緑色の発光輝度のバランスが良い、色鮮やかな画像を表示することが可能になる。

【図面の簡単な説明】

【図１】　本発明のＥＬ表示装置の構成を示す図。

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【図２】　ＥＬ表示装置の画素構成を示す図。
【図３】　本発明のＥＬ表示装置のソース信号線駆動回路のブロック図。
【図４】　レベルシフタ回路の等価回路図。
【図５】　ＴＦＴの上面図及び断面図。
【図６】　ＥＬ表示装置の画素の回路図。
【図７】　ＥＬ表示装置の画素の回路図。
【図８】　ＥＬ表示装置の作製工程を示す図。
【図９】　ＥＬ表示装置の作製工程を示す図。
【図１０】　ＥＬ表示装置の作製工程を示す図。
【図１１】　ＥＬ表示装置の作製工程を示す図。
【図１２】　電子機器の具体例を示す図。
【図１３】　電子機器の具体例を示す図。
【図１４】　従来のＥＬ表示装置の構成を示す図。
【図１５】　有機ＥＬ材料の電圧－輝度特性を示す図。
【図１６】　本発明のＥＬ表示装置のＴＦＴ基板の上面図。

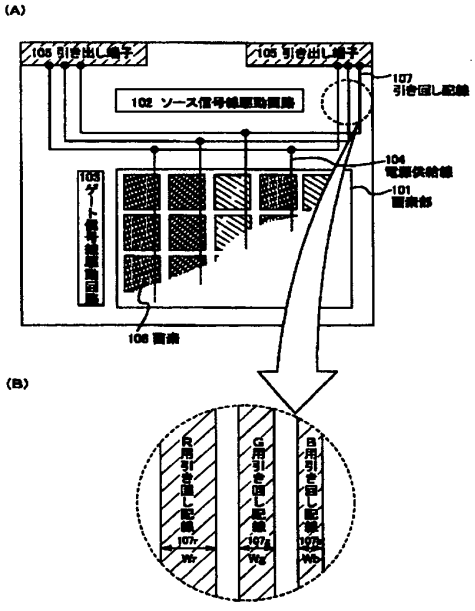
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【図１７】　本発明のＥＬ表示装置の概観図及び断面図。
【図１８】　本発明のＥＬ表示装置の作成工程を示す図。
【図１９】　ＤＬＣ膜を用いた本発明のＥＬ表示装置の断面図。

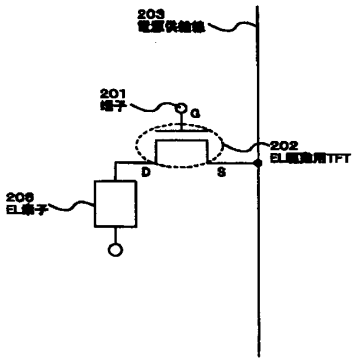
【符号の説明】

１０１　画素部
１０２　ソース信号線駆動回路
１０３　ゲート信号線駆動回路
１０４　電源供給線
１０５　引き出し端子
１０６　画素
１０７　引き回し配線
１０７ｒ　Ｒ用引き回し配線
１０７ｇ　Ｇ用引き回し配線
１０７ｂ　Ｂ用引き回し配線

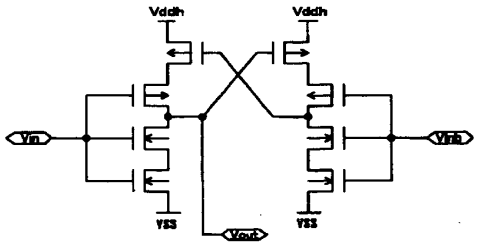
【図１】



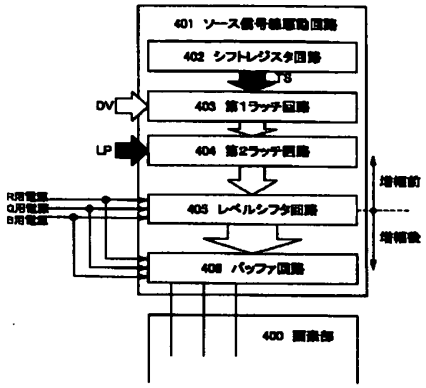

【図２】



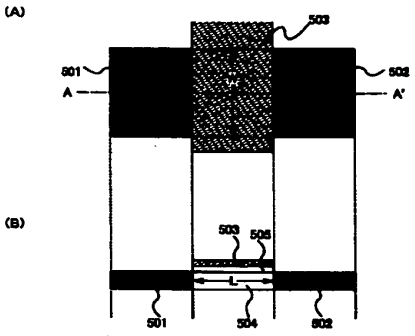

【図４】



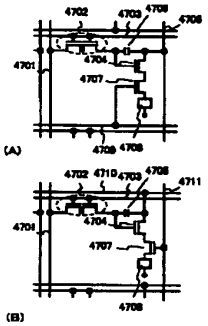
【図３】



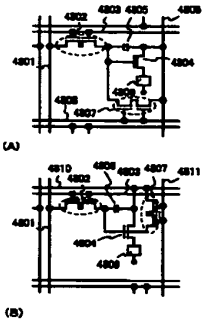

【図５】



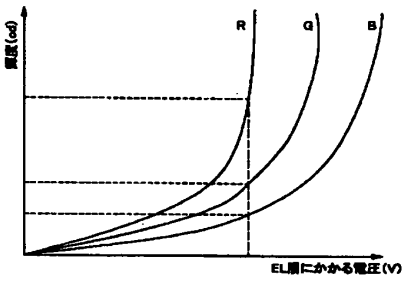

【図６】



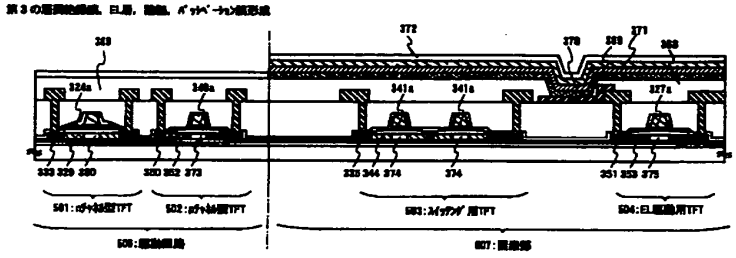

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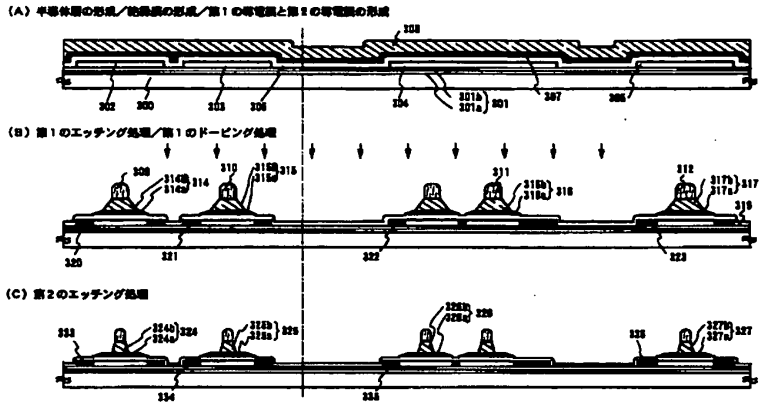

【図１５】



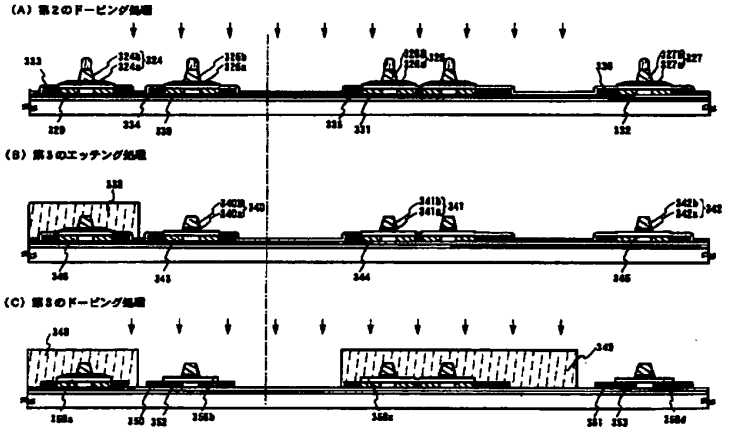

【図１１】



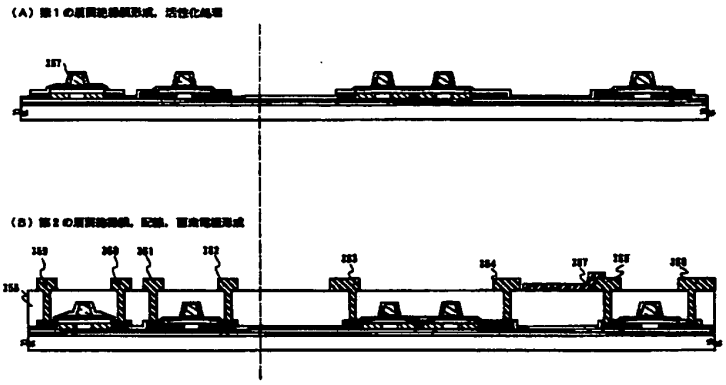
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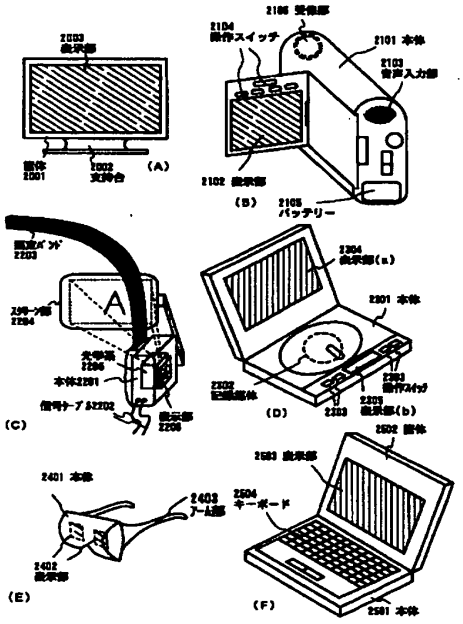
【図９】



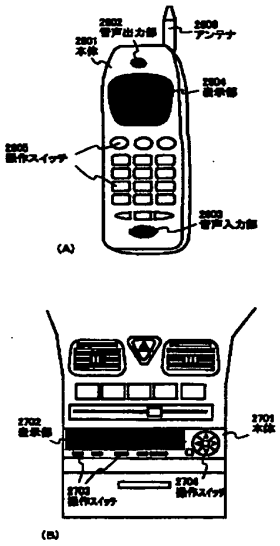
【図１０】



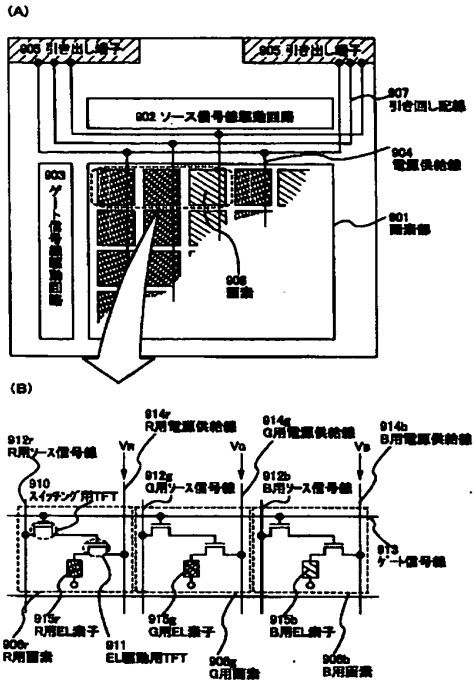
【図１２】



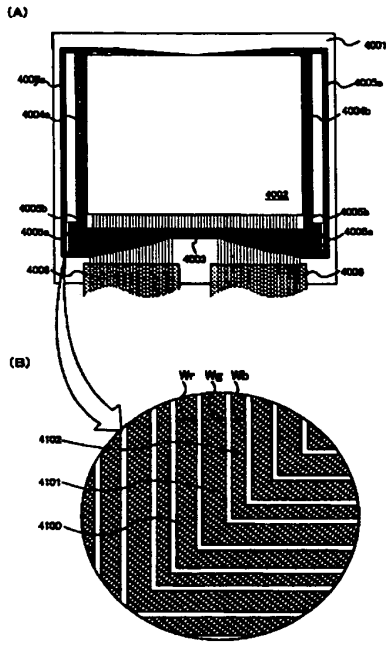
【図１３】



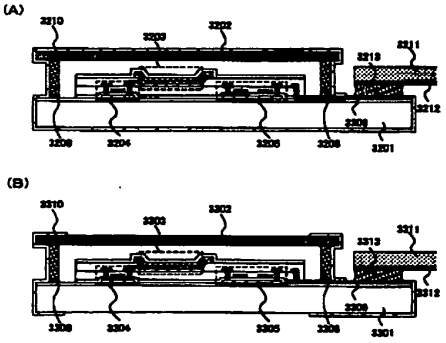
【図１４】


(A)
905 引き出し端子
905 引き出し端子
902 ソース信号線駆動回路
907
引き回し配線
904
電源供給線
903
ゲート信号線駆動回路
901
画素部
906
画素
(B)
914r
R用電源供給線
914g
G用電源供給線
914b
B用電源供給線
912r
R用ソース信号線
Vr
Vg
Vb
912g
G用ソース信号線
912b
B用ソース信号線
910
スイッチング用TFT
913
ゲート信号線
915r
R用EL素子
915g
G用EL素子
915b
B用EL素子
909r
R用画素
911
EL駆動用TFT
909g
G用画素
909b
B用画素

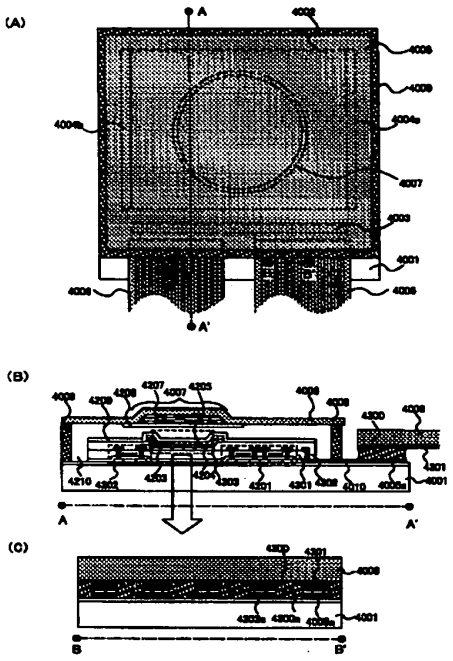
【図１６】


(A)
4001
4005a
4004a
4004b
4005b
4003
4006
4020
(B)
Wr
Wg
Wb
4102
4101
4100

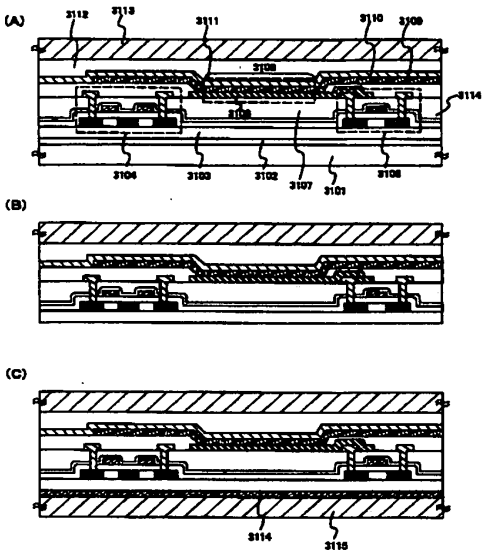
【図１９】


(A)
3210
3202
3211
3213
3212
3208
3204
3205
3206
3201
(B)
3210
3203
3202
3211
3213
3212
3208
3204
3205
3206
3201

【図１７】



【図１８】



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| | 33/14 | | | 33/14 | Ａ |
| // Ｇ０９Ｇ | 3/20 | ６２１ | Ｇ０９Ｇ | 3/20 | ６２１Ｍ |
| | | ６４２ | | | ６４２Ｌ |
| | 3/30 | | | 3/30 | Ｋ |

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BB05 BB07 CA01 CB01 CC00
DA01 DB03 EA01 EB00 GA04
5C080 AA06 BB05 CC03 DD05 EE30
FF11 GG07 GG08 JJ02 JJ03
JJ06 KK02 KK07 KK43
5C094 AA04 AA07 AA08 AA21 AA48
AA55 BA03 BA12 BA27 CA19
CA24 DA09 DA13 DB01 DB02
DB04 DB10 EA04 EA05 EA07
EB02 FA01 FB12 FB14 FB15
GA10 HA08 HA10

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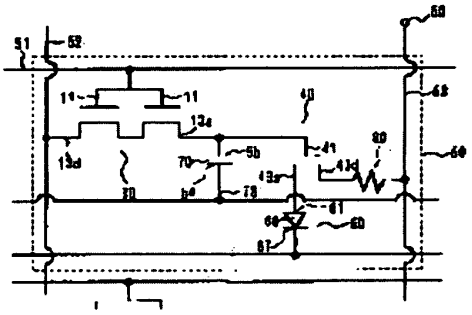
51)Int.Cl. G09F 9/30
H05B 33/08
H05B 33/14

21)Application number : 2000-088211
22)Date of filing : 28.03.2000

(71)Applicant : SANYO ELECTRIC CO LTD
(72)Inventor : YASUDA HITOSHI

## 54) ELECTROLUMINESCENT DISPLAY DEVICE

57)Abstract:
ROBLEM TO BE SOLVED: To provide an EL display device capable of btaining prescribed luminance constantly by stabilizing the haracteristic of a TFT.
OLUTION: In this display device, an organic EL element 60 consisting f anode 61, a cathode 67 and a light emitting element layer 66 held etween both electrodes, a first TFT 30 for switching controlling timing hen a current is supplied to the element 60, a second TFT 40 for riving the element 60 and a driving power source line 53 supplying a urrent to the element 60 via the second TFT 40 are provided on an nsulating substrate 10 and, moreover, a resistance 80 which is to be roduced in the same process and with the same material as those in he anode 61 of the element 60 is formed between the driving power ource line 53 and the drain of the second TFT 40.



EGAL STATUS
Date of request for examination]
Date of sending the examiner's decision of rejection]
Kind of final disposal of application other than the xaminer's decision of rejection or application onverted registration]
Date of final disposal for application]
Patent number]
Date of registration]
Number of appeal against examiner's decision of ejection]
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(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
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(43)公開日　平成13年10月5日(2001.10.5)

| (51)Int.Cl.' | | 識別記号 | FI | | テーマコード'(参考) |
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| | | ３３８ | | | ３３８　５Ｃ０９４ |
| Ｈ０５Ｂ | 33/08 | | Ｈ０５Ｂ | 33/08 | |
| | 33/14 | | | 33/14 | Ａ |

審査請求　未請求　請求項の数３　ＯＬ　（全６頁）

(21)出願番号　特願2000－88211(P2000－88211)

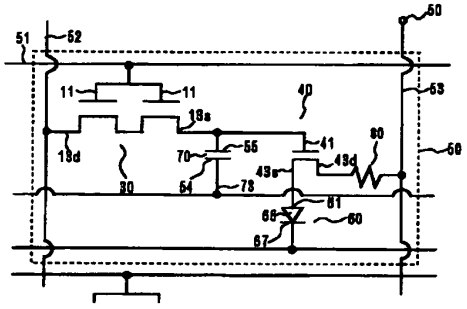
(22)出願日　平成12年３月28日(2000.3.28)

(71)出願人　000001889
三洋電機株式会社
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弁理士　芝野　正雅

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DB03 EB00 FA01 GA00
5C094 AA03 AA43 AA55 BA03 BA27
CA19 DA13 DB01 DB04 EA04
EA05 EB02 FA01 FA02 FB02
FB12 GA10

(54)【発明の名称】　エレクトロルミネッセンス表示装置

(57)【要約】
【課題】　ＴＦＴの特性を安定させて、所定の輝度が安定して得られるＥＬ表示装置を提供する。
【解決手段】　絶縁性基板１０上に、陽極６１、陰極６７及び該両電極の間に挟まれた発光素子層６６から成る有機ＥＬ素子６０と、これに電流を供給するタイミングを制御するスイッチング用の第１のＴＦＴ３０と、有機ＥＬ素子駆動用の第２のＴＦＴ４０と、ＥＬ素子６０に第２のＴＦＴ４０を介して電流を供給する駆動電源線５３とを備えており、駆動電源線５３と第２のＴＦＴ４０のドレインとの間にＥＬ素子６０の陽極６１と同一工程で同一材料から成る抵抗８０を形成する。



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【特許請求の範囲】

【請求項１】　陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、前記エレクトロルミネッセンス素子を駆動する駆動電源からの電流を供給する駆動電源線と、該駆動電源線にドレインが接続されており前記駆動電源からの電流を制御して前記エレクトロルミネッセンス素子に供給する薄膜トランジスタとを備えたエレクトロルミネッセンス表示装置であって、前記駆動電源線と前記ドレインとの間に抵抗を備えることを特徴とするエレクトロルミネッセンス表示装置。

【請求項２】　陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、前記エレクトロルミネッセンス素子を駆動する電流を供給するタイミングを制御する第１の薄膜トランジスタと、前記エレクトロルミネッセンス素子を駆動する駆動電源からの電流を供給する駆動電源線と、該駆動電源線にドレインが接続されており前記駆動電源からの電流を制御して前記エレクトロルミネッセンス素子に供給する薄膜トランジスタとを備えたエレクトロルミネッセンス表示装置であって、前記駆動電源線と前記ドレインとの間に抵抗を備えることを特徴とするエレクトロルミネッセンス表示装置。

【請求項３】　前記駆動電源線と前記ソースとの間の抵抗が、前記陽極と同じ材料からなることを特徴とする請求項１又は２に記載のエレクトロルミネッセンス表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、エレクトロルミネッセンス素子及び薄膜トランジスタを備えたエレクトロルミネッセンス表示装置に関する。

【０００２】

【従来の技術】近年、エレクトロルミネッセンス（ElectroLuminescence：以下、「ＥＬ」と称する。）素子を用いたＥＬ表示装置が、ＣＲＴやＬＣＤに代わる表示装置として注目されており、例えば、そのＥＬ素子を駆動させるスイッチング素子として薄膜トランジスタ（Thin Film Transistor：以下、「ＴＦＴ」と称する。）を備えたＥＬ表示装置の研究開発も進められている。

【０００３】図５に有機ＥＬ表示装置の１表示画素を示す等価回路図を示し、図６に有機ＥＬ表示装置の１表示画素の平面図を示し、図７（ａ）に図６中のＡ－Ａ線に沿った断面図を示し、図７（ｂ）に図６中のＢ－Ｂ線に沿った断面図を示す。

【０００４】図５及び図６に示すように、ゲート信号線５１とドレイン信号線５２とに囲まれた領域に表示画素が形成されている。両信号線の交点付近にはスイッチング素子である第１のＴＦＴ３０が備えられており、そのＴＦＴ３０のソース１３ｓは後述の保持容量電極５４との間で容量をなす容量電極５５を兼ねるとともに、有機ＥＬ素子を駆動する第２のＴＦＴ４０のゲート４２に接

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続されている。第２のＴＦＴ４０のソース４３ｓは有機ＥＬ素子の陽極６１に接続され、他方のドレイン４３ｄは有機ＥＬ素子を駆動する駆動電源５０に接続された駆動電源線１５３に接続されている。

【０００５】また、ＴＦＴの付近には、ゲート信号線５１と並行に保持容量電極５４が配置されている。この保持容量電極５４はクロム等から成っており、ゲート絶縁膜１２を介して第１のＴＦＴ３０のソース１３ｓと一体形成された容量電極５５との間で電荷を蓄積して容量を成している。この保持容量７０は、第２のＴＦＴ４０のゲート４１に印加される電圧を保持するために設けられている。

【０００６】まず、スイッチング用のＴＦＴである第１のＴＦＴ３０について説明する。

【０００７】図７（ａ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１０上に、非晶質シリコン膜にレーザを照射して多結晶化した多結晶シリコン膜から成る能動層１３を形成する。この能動層１３にはいわゆるＬＤＤ（Lightly Doped Drain）構造が設けられている。即ち、ゲート１３２の両側に低濃度領域１３１ＬＤとその外側に高濃度領域のソース１３１ｓ及びドレイン１３１ｄが設けられている。その上にゲート絶縁膜１２、及びクロム（Ｃｒ）、モリブデン（Ｍｏ）などの高融点金属からなるゲート信号線５１の一部をなすゲート電極１１を形成する。このとき同時に、保持容量電極５４を形成する。

【０００８】続いて、ゲート絶縁膜１２及びゲート絶縁膜１２上の全面には、$SiO_2$膜、ＳｉＮ膜及び$SiO_2$膜の順に積層された層間絶縁膜１５を設け、ドレイン１３ｄに対応して設けたコンタクトホールにＡｌ等の金属を充填してドレイン信号線５２の一部をなすドレイン電極１６を設ける。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１７を設ける。

【０００９】次に、有機ＥＬ素子の駆動用のＴＦＴである第２のＴＦＴ４０について説明する。

【００１０】図７（ｂ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１０上に、第１のＴＦＴ３０の能動層１３の形成と同時に、多結晶シリコン膜から成る能動層４３を形成する。その能動層４３には、ゲート電極４１上方に真性又は実質的に真性であるチャネル４３ｃと、このチャネル４３ｃの両側に、ｐ型不純物のイオンドーピングを施してソース４３ｓ及びドレイン４３ｄを設けて、ｐ型チャネルＴＦＴを構成する。その能動層４３の上にゲート絶縁膜１２、及びＣｒ、Ｍｏなどの高融点金属からなるゲート電極１１を設ける。このゲート電極１１は、第１のＴＦＴ３０のソース１３ｓに接続されている。

【００１１】そして、ゲート絶縁膜１２及びゲート電極４１上の全面には、$SiO_2$膜、ＳｉＮ膜及び$SiO_2$膜の順に積層された層間絶縁膜１５を形成し、ドレイン４

３ｄに対応して設けたコンタクトホールにＡｌ等の金属を充填して駆動電源５０に接続された駆動電源線５３を配置する。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１７を形成して、その平坦化絶縁膜１７のソース４３ｓに対応した位置にコンタクトホールを形成し、このコンタクトホールを介してソース４３ｓとコンタクトしたＩＴＯ（Indium Tin Oxide）から成る透明電極、即ち有機ＥＬ素子６０の陽極６１を平坦化絶縁膜１７上に設ける。

【００１２】有機ＥＬ素子６０は、ＩＴＯ等の透明電極から成る陽極６１、ＭＴＤＡＴＡ（4,4',4''-tris(3-methylphenylphenylamino)triphenylamine）から成る第１ホール輸送層６２、及びＴＰＤ（N,N'-diphenyl-N,N'-di(3-methylphenyl)-1,1'-biphenyl-4,4'-diamine）からなる第２ホール輸送層６３、キナクリドン（Quinacridone）誘導体を含むＢｅｂｑ２（bis(10-hydroxybenzo[h]quinolinato)beryllium）から成る発光層６４及びＢｅｂｑ2から成る電子輸送層６５からなる発光素子層６６、マグネシウム・インジウム合金から成る陰極６７がこの順番で積層形成された構造である。これら第１ホール輸送層６２、第２ホール輸送層６３、電子輸送層６５及び陰極６７は、図６に示した各表示画素に備えた有機ＥＬ素子に共通に形成されている。発光層６４は、陽極６１に対応して島状に形成されている。

【００１３】なお、有機ＥＬ素子は、陽極から注入されたホールと、陰極から注入された電子とが発光層の内部で再結合し、発光層を形成する有機分子を励起して励起子が生じる。この励起子が放射失活する過程で発光層から光が放たれ、この光が透明な陽極から透明絶縁基板を介して外部へ放出されて発光する。

【００１４】このように、第１のＴＦＴ３０のソース１３ｓから印加された電荷が保持容量７０に蓄積されるとともに第２のＴＦＴ４０のゲート４１に印加されてその電圧に応じて有機ＥＬ素子は発光する。

【００１５】

【発明が解決しようとする課題】ところが、有機ＥＬ素子６０に供給する電流値を制御する機能を有する第２のＴＦＴ４０は、ゲート電圧に対するドレイン電流特性のばらつきが大きいため、発光材料に流れる電流の変動も大きくなってしまっている。

【００１６】図４に、第２ＴＦＴのゲート電圧（Ｖｇ）とドレイン電流（Ｉｄ）との特性関係を示す。同図において、横軸はゲート電圧（Ｖｇ）を示し、縦軸はドレイン電流（Ｉｄ）を示す。実線で示した従来のＴＦＴにおいては、下側の実線ｃと上側の実線ｄとの間で特性が変化し、あるゲート電圧においてはその変動値がＩｌも変動してしまっている。

【００１７】このように特性が変動することにより、ＥＬ素子の輝度も所定の輝度が得られないという欠点があった。



【００１８】そこで本発明は、上記の従来の欠点に鑑みて為されたものであり、ＴＦＴの特性を安定させて、所定の輝度が安定して得られるＥＬ表示装置を提供することを目的とする。

【００１９】

【課題を解決するための手段】本発明のＥＬ表示装置は、陽極と陰極との間に発光層を有するＥＬ素子と、前記ＥＬ素子を駆動する駆動電源からの電流を供給する駆動電源線と、該駆動電源線にドレインが接続されており前記駆動電源からの電流を制御して前記ＥＬ素子に供給するＴＦＴとを備えたＥＬ表示装置であって、前記駆動電源線と前記ドレインとの間に抵抗を備えるものである。

【００２０】また、本発明は、陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、前記エレクトロルミネッセンス素子を駆動する電流を供給するタイミングを制御する第１の薄膜トランジスタと、前記エレクトロルミネッセンス素子を駆動する駆動電源からの電流を供給する駆動電源線と、該駆動電源線にドレインが接続されており前記駆動電源からの電流を制御して前記エレクトロルミネッセンス素子に供給する薄膜トランジスタとを備えたエレクトロルミネッセンス表示装置であって、前記駆動電源線と前記ドレインとの間に抵抗を備えるたものである。

【００２１】更に、上述のＥＬ表示装置は、前記駆動電源線と前記ソースとの間の抵抗が、前記陽極と同じ材料からなるＥＬ表示装置である。

【００２２】

【発明の実施の形態】本発明のＥＬ表示装置について以下に説明する。

【００２３】図１に本発明のＥＬ表示装置を有機ＥＬ表示装置に適用した場合の等価回路図を示し、図２に有機ＥＬ表示装置の平面図を示し、図３（ａ）に図２中のＡ－Ａ線に沿った断面図を示し、図３（ｂ）に図２中のＢ－Ｂ線に沿った断面図を示す。

【００２４】図１及び図２に示すように、ゲート信号線５１とドレイン信号線５２とに囲まれた領域に表示画素５０（点線で示す領域）が形成されている。両信号線５１，５２の交点付近にはスイッチング素子である第１のＴＦＴ３０が備えられており、そのＴＦＴ３０のソース１３ｓは後述の保持容量電極５４との間で容量をなす容量電極５５を兼ねるとともに、有機ＥＬ素子を駆動する第２のＴＦＴ４０のゲート４１に接続されている。第２のＴＦＴ４０のソース４３ｓは有機ＥＬ素子の陽極６１に接続され、他方のドレイン４３ｄは有機ＥＬ素子６０を駆動する電流を供給する駆動電源５０に接続された駆動電源線５３に接続されている。このとき、駆動電源線５３と、それに接続されたドレイン４３ｄとの間には抵抗８０が設けられている。

【００２５】また、ＴＦＴの付近には、ゲート信号線５

１と並行に保持容量電極５４が配置されている。この保持容量電極５４はクロム等から成っており、ゲート絶縁膜１２を介して第１のＴＦＴ３０のソース３３と接続された容量電極７２との間で電荷を蓄積して容量を成している。この保持容量７０は、第２のＴＦＴ４０のゲート４２に印加される電圧を保持するために設けられている。なお、第１のＴＦＴ３０の断面形状は従来の技術の欄で説明した図７（ａ）と同じであるので、説明は省略する。

【００２６】ここで、駆動電源線５３と、それに接続されたドレイン４３ｄとの間に設けられた抵抗８０について、図３（ｂ）に従って説明する。

【００２７】図３（ｂ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１０上に、第１のＴＦＴ３０の能動層１３の形成と同時に形成した多結晶シリコン膜から成る能動層４３を形成する。その能動層４３には、ゲート電極４１上方に真性又は実質的に真性であるチャネル４３ｃと、このチャネル４３ｃの両側に、ｐ型不純物のイオンドーピングを施してソース４３ｓ及びドレイン４３ｄを設けて、ｐ型チャネルＴＦＴを構成する。

【００２８】この能動層４３の上に、$SiO_2$膜から成るゲート絶縁膜１２、及びＣｒ、Ｍｏなどの高融点金属からなるゲート電極４１を設ける。

【００２９】そして、ゲート絶縁膜１２及びゲート電極４１上の全面には、$SiO_2$膜、ＳｉＮ膜及び$SiO_2$膜の順に積層された層間絶縁膜１５を形成する。その上にＡｌから成りＥＬ素子６０に供給する駆動電源に接続された駆動電源線５３を形成する。その後、駆動電源線５３を含む全面に有機樹脂から成り表面を平坦にする平坦化絶縁膜１７を堆積し、その平坦化絶縁膜１７のソース４３ｓドレイン４３ｄ及び駆動電源線５３の一部に対応した位置にコンタクトホールＣ１，Ｃ２，Ｃ３を設ける。そして、これらのコンタクトホールを介して、透明導電材料であるＩＴＯによって、ソース４３ｓとコンタクトしたＥＬ素子の陽極６１、及びドレイン４３ｄと駆動電源線５３とを接続した抵抗８０を平坦化絶縁膜１７上に設ける。

【００３０】これらの陽極６１及び抵抗８０を形成した後、陽極６１の周辺まで覆った絶縁膜６８を形成する。即ち、陽極６１の周辺を覆い、陽極６１の中央部に開口部を有する絶縁膜６８を形成する。この絶縁膜６８は、抵抗８０の上層に設けるＥＬ素子の第１ホール輸送層６２と抵抗８０とを絶縁するとともに、陽極６１の厚みによる段差に起因して生じる陰極６７とのショートを防止する機能を有する。

【００３１】そして、陽極６１及び陽極６１の周辺にまで延在させて形成した絶縁膜６８の表面に、従来のＥＬ素子６０と同様に、第１ホール輸送層６２、第２ホール輸送層６３、発光層６４、電子輸送層６５及び陰極６７を順に形成する。発光層６４は陽極６１よりも大きめの面積とし、他の第１ホール輸送層６２、第２ホール輸送層６３、電子輸送層６５及び陰極６７のように全面には形成しない。また、発光層６４はその材料を変えることによって発光させる色を変えることが可能である。なお、陰極６７は、各表示画素５０において共通の電位である。

【００３２】このように、ＥＬ素子の駆動電源線５３とドレイン電極４３ｄとの間にＩＴＯから成る抵抗８０を設けることにより、第２のＴＦＴ４０からＥＬ素子６０に供給される電流が変動することを防止することができる。

【００３３】前述の図４の点線で示すように、本発明によれば、ＥＬ素子を駆動する第２のＴＦＴ４０のＶｇ－Ｉｄ特性は、曲線ａから曲線ｂ間での範囲での変動に治まっており、従来の特性とあるゲート電圧における電流値で比較すると、従来その変動がＩ１であったのに対して、それよりも小さい約７０％程度になっていることがわかる。

【００３４】こうして、ＥＬ素子の発光輝度を安定させて得ることができるので、良好な表示を得ることができることになる。

【００３５】また、抵抗８０の材料として、陽極６１と同じ材料のＩＴＯを陽極６１形成と同時に形成することにより、新たな工程を増やすことなく形成できるため、工程増大につながることなく形成することができ、コスト増大を招くことがない。

【００３６】なお、本実施の形態においては、第２のＴＦＴ４０が、能動層４３がゲート電極４１よりも下層にあるいわゆるトップゲート型のＴＦＴについて説明したが、本発明はそれに限定されるものではなく、能動層４３がゲート電極４１よりも上層にあるいわゆるボトムゲート型のＴＦＴであっても同様の効果を得ることができる。第１のＴＦＴ３０においても、トップゲート型でもボトムゲート型でも良い。

【００３７】また、本願においては、ドレインはＴＦＴに電流が流れ込む領域を意味し、ソースはＴＦＴから電流が流れ出す領域を意味するものとする。

【００３８】また、上述の実施の形態においては、ゲート電極１１，４１がダブルゲート構造の場合について説明したが、本願発明はそれに限定されるものではなく、シングルゲートあるいは３つ以上のマルチゲート構造を有していても本願と同様の効果を奏することが可能である。

【００３９】また、上述の実施の形態においては、第２のＴＦＴがｐ型チャネルＴＦＴの場合を示したが、第２のＴＦＴはｎ型の不純物を導入したｎ型チャネルＴＦＴでも良い。

【００４０】また、上述の実施の形態においては、能動層としてｐ－Ｓｉ膜を用いたが、微結晶シリコン膜又は

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非晶質シリコン膜を用いても良い。

【００４１】

【発明の効果】本発明のＥＬ表示装置によれば、ＥＬ素子を駆動するＴＦＴからＥＬ素子に供給される電流が変動することを防止することができ、安定した表示を得ることができる。

【図面の簡単な説明】

【図１】本発明のＥＬ表示装置の等価回路図である。

【図２】本発明のＥＬ表示装置の実施の形態を示す平面図である。

【図３】本発明のＥＬ表示装置の実施の形態を示す断面図である。

【図４】ＴＦＴの特性を示す特性図である。

【図５】従来のＥＬ表示装置の等価回路図である。

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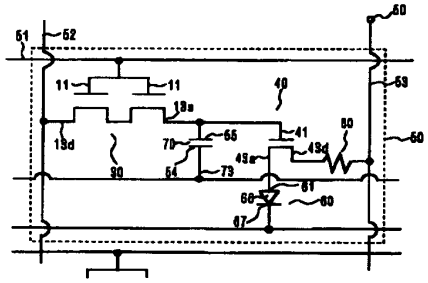
【図６】従来のＥＬ表示装置の平面図である。

【図７】従来のＥＬ表示装置の断面図である。

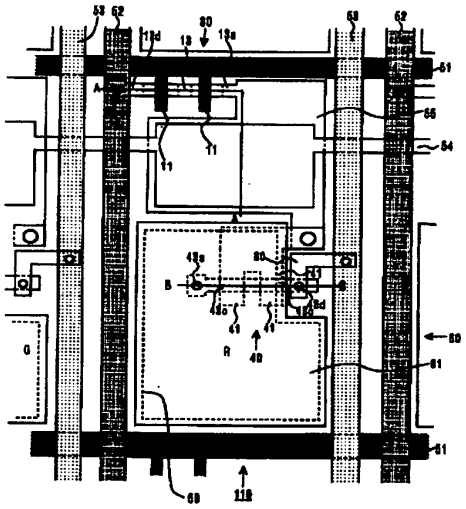
【符号の説明】

| | |
|---|---|
| ３０ | 第１のＴＦＴ |
| １３ｓ、１３ｓ | ソース |
| １３ｄ、１３ｄ | ドレイン |
| １３ｃ、１３ｃ | チャネル |
| １３ＬＤ、１３ＬＤ | ＬＤＤ領域 |
| １１、４１ | ゲート電極 |
| ４０ | 第２のＴＦＴ |
| ５０ | 駆動電源 |
| ５３ | 駆動電源線 |
| ６０ | 有機ＥＬ素子 |
| ８０ | 抵抗 |

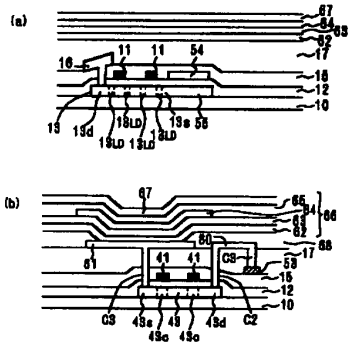
【図１】



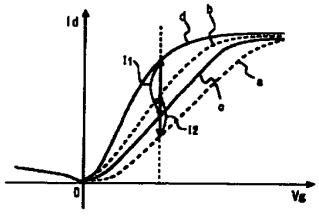
【図２】



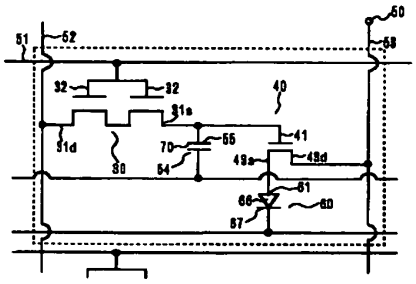
【図３】



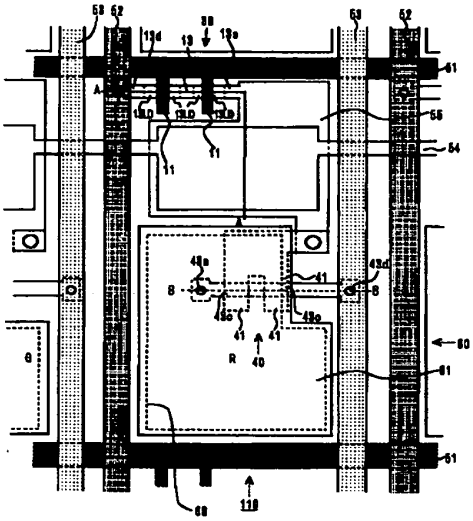
【図４】



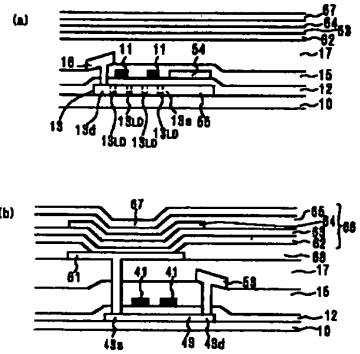
【図５】



【図６】



【図７】



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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the electroluminescence display equipped with the electroluminescent element and the thin film transistor.
[0002]
[Description of the Prior Art] In recent years, researches and developments of EL display equipped with the thin film transistor ("TFT" is called below Thin Film Transistor:.) as a switching element which it is observed [ switching element ] as a display which EL display using an electroluminescence ("EL" is called below ElectroLuminescence:.) component replaces with CRT or LCD, for example, makes the EL element drive are also furthered.
[0003] The representative circuit schematic showing 1 display pixel of an organic electroluminescence display in drawing 5 is shown, the top view of 1 display pixel of an organic electroluminescence display is shown in drawing 6 , the sectional view which met drawing 7 (a) at the A-A line in drawing 6 is shown, and the sectional view which met drawing 7 (b) at the B-B line in drawing 6 is shown.
[0004] The display pixel is formed in the field surrounded by the gate signal line 51 and the drain signal line 52 as shown in drawing 5 and drawing 6 . It has 1st TFT30 which is a switching element near the intersection of both signal lines, and the source 13s of TFT30, while serving as the capacity electrode 55 which makes capacity between the below-mentioned retention volume electrodes 54, it connects with the gate 42 of 2nd TFT40 which drives an organic EL device. It connects with the anode plate 61 of an organic EL device source 43s of 2nd TFT40, and connects with the drive power-source line 153 connected to the drive power source 50 which drives an organic EL device drain 43d of another side.
[0005] Moreover, near TFT, the retention volume electrode 54 is arranged in parallel with the gate signal line 51. This retention volume electrode 54 consists of chromium etc., accumulated the charge through gate dielectric film 12 between source 13s of 1st TFT30, and the really formed capacity electrode 55, and has accomplished capacity. This retention volume 70 is formed in order to hold the electrical potential difference impressed to the gate 41 of 2nd TFT40.
[0006] First, 1st TFT30 which is TFT for switching is explained.
[0007] As shown in drawing 7 (a), the active layer 13 which consists of the polycrystal silicone film which irradiated laser and polycrystal-ized it to the amorphous silicone film is formed on the insulating substrate 10 which consists of quartz glass, alkali free glass, etc. The so-called LDD (Lightly Doped Drain) structure is prepared in this active layer 13. That is, source 131s [ of a high concentration field ] and drain 131d is prepared in low concentration field 131LD and its outside at the both sides of the gate 132. The gate electrode 11 which makes a part of gate signal line 51 which consists of refractory metals, such as gate dielectric film 12 and chromium (Cr), and molybdenum (Mo), on it is formed. The retention volume electrode 54 is formed in coincidence at this time.
[0008] Then, the drain electrode 16 which fills up the contact hole which formed the interlayer insulation film 15 by which the laminating was carried out to the order of SiO2 film, an SiN film, and SiO2 film the whole surface on gate dielectric film 12 and gate dielectric film 12, and was prepared

corresponding to drain 13d with metals, such as aluminum, and forms some drain signal lines 52 is formed. Furthermore, the flattening insulator layer 17 which consists of organic resin and makes a front face flat is formed in the whole surface.
[0009] Next, 2nd TFT40 which is TFT for the drive of an organic EL device is explained.
[0010] As shown in drawing 7 (b), the active layer 43 which changes from a polycrystal silicone film to formation and coincidence of the active layer 13 of 1st TFT30 is formed on the insulating substrate 10 which consists of quartz glass, alkali free glass, etc. In that active layer 43, ion doping of p mold impurity is performed to the both sides of channel 43c which is genuineness genuineness or substantially, and this channel 43c, source 43s and drain 43d is prepared in the gate electrode 41 upper part, and p mold channel TFT is constituted. The gate electrode 11 which consists of refractory metals, such as gate dielectric film 12, and Cr, Mo, is formed on the active layer 43. This gate electrode 11 is connected at source 13s of 1st TFT30.
[0011] And the interlayer insulation film 15 by which the laminating was carried out to the order of SiO2 film, an SiN film, and SiO2 film is formed the whole surface on gate dielectric film 12 and the gate electrode 41, and the drive power-source line 53 which filled up the contact hole prepared corresponding to drain 43d with metals, such as aluminum, and was connected to the drive power source 50 is arranged. Furthermore, the flattening insulator layer 17 which consists of organic resin and makes a front face flat is formed, a contact hole is formed in the location corresponding to source 43s of that flattening insulator layer 17, and the transparent electrode 61 which consists of ITO (Indium Tin Oxide) which contacted source 43s through this contact hole, i.e., the anode plate of an organic EL device 60, is formed in the whole surface on the flattening insulator layer 17.
[0012] An organic EL device 60 The anode plate 61, MTDATA which consist of transparent electrodes, such as ITO () [ 4, 4', ] [ 4"-tris] (3-methylphenylphenylamino) the 1st hole transportation layer 62 which consists of triphenylamine, and TPD (N, and N'-diphenyl-N, N'-di(3-methylphenyl)- 1 and 1'-biphenyl-4 --) The 2nd hole transportation layer 63 which consists of 4'-diamine, the luminous layer 64 which consists of Bebq2 (bis(10-hydroxybenzo[h] quinolinato) beryllium) containing the Quinacridone (Quinacridone) derivative And it is the structure where laminating formation of the light emitting device layer 66 which consists of an electronic transportation layer 65 which consists of Bebq2, and the cathode 67 which consists of a magnesium indium alloy was carried out in this sequence. These 1st hole transportation layer 62, the 2nd hole transportation layer 63, the electronic transportation layer 65, and cathode 67 are formed common to the organic EL device with which each display pixel shown in drawing 6 was equipped. The luminous layer 64 is formed in island shape corresponding to the anode plate 61.
[0013] In addition, the hole poured in from the anode plate and the electron poured in from cathode recombine an organic EL device inside a luminous layer, it excites the organic molecule which forms a luminous layer, and an exciton produces it. Light is emitted from a luminous layer in the process in which this exciton carries out radiation deactivation, and from a transparent anode plate, this light is emitted to the exterior through a transparence insulating substrate, and emits light.
[0014] Thus, while the charge impressed from source 13s of 1st TFT30 is accumulated in retention volume 70, it is impressed by the gate 41 of 2nd TFT40, and an organic EL device emits light according to the electrical potential difference.
[0015]
[Problem(s) to be Solved by the Invention] However, since 2nd TFT40 which has the function which controls the current value supplied to an organic EL device 60 has large dispersion in the drain current characteristic over gate voltage, fluctuation of the current which flows to luminescent material is also large.
[0016] The gate voltage (Vg) of the 2nd TFT and property relation with a drain current (Id) are shown in drawing 4 . In this drawing, an axis of abscissa shows gate voltage (Vg), and an axis of ordinate shows a drain current (Id). In the conventional TFT shown as the continuous line, between the lower continuous line c and the upper continuous line d, the property changed and the variation has changed I1 in a certain gate voltage.

[0017] Thus, when changing a property, the brightness of an EL element also had the fault that predetermined brightness was not obtained.
[0018] Then, in view of the above-mentioned conventional fault, it succeeds in this invention, it stabilizes the property of TFT, and predetermined brightness aims at offering EL display obtained by being stabilized.
[0019]
[Means for Solving the Problem] EL display of this invention is an EL display equipped with the drive power-source line which supplies the current from the drive power source which drives the EL element which has a luminous layer, and said EL element between an anode plate and cathode, and TFT which the drain is connected to this drive power-source line, controls the current from said drive power source, and is supplied to said EL element, and is equipped with resistance between said drive power-source lines and said drains.
[0020] Moreover, the electroluminescent element to which this invention has a luminous layer between an anode plate and cathode, The 1st thin film transistor which controls the timing which supplies the current which drives said electroluminescent element, The drive power-source line which supplies the current from the drive power source which drives said electroluminescent element, It is the electroluminescence display equipped with the thin film transistor which the drain is connected to this drive power-source line, controls the current from said drive power source, and is supplied to said electroluminescent element. it is ** equipped with resistance between said drive power-source lines and said drains.
[0021] Furthermore, above-mentioned EL display is an EL display with which resistance between said drive power-source lines and said sources consists of the same ingredient as said anode plate.
[0022]
[Embodiment of the Invention] EL display of this invention is explained below.
[0023] The representative circuit schematic at the time of applying EL display of this invention to an organic electroluminescence display at drawing 1 is shown, the top view of an organic electroluminescence display is shown in drawing 2 , the sectional view which met drawing 3 (a) at the A-A line in drawing 2 is shown, and the sectional view which met drawing 3 (b) at the B-B line in drawing 2 is shown.
[0024] As shown in drawing 1 and drawing 2 , the display pixel 50 (field shown by the dotted line) is formed in the field surrounded by the gate signal line 51 and the drain signal line 52. It has 1st TFT30 which is a switching element near the intersection of both the signal lines 51 and 52, and the source 13s of TFT30, while serving as the capacity electrode 55 which makes capacity between the below-mentioned retention volume electrodes 54, it connects with the gate 41 of 2nd TFT40 which drives an organic EL device. It connects with the anode plate 61 of an organic EL device source 43s of 2nd TFT40, and connects with the drive power-source line 53 connected to the drive power source 50 which supplies the current which drives an organic EL device 60 drain 43d of another side. At this time, resistance 80 is formed between the drive power-source line 53 and drain 43d connected to it.
[0025] Moreover, near TFT, the retention volume electrode 54 is arranged in parallel with the gate signal line 51. This retention volume electrode 54 consists of chromium etc., accumulated the charge between the capacity electrodes 72 connected with the source 33 of 1st TFT30 through gate dielectric film 12, and has accomplished capacity. This retention volume 70 is formed in order to hold the electrical potential difference impressed to the gate 42 of 2nd TFT40. In addition, since the cross-section configuration of 1st TFT30 is the same as drawing 7 (a) explained in the column of a Prior art, explanation is omitted.
[0026] Here, the resistance 80 prepared between the drive power-source line 53 and drain 43d connected to it is explained according to drawing 3 (b).
[0027] As shown in drawing 3 (b), the active layer 43 which consists of the polycrystal silicone film formed in formation and coincidence of the active layer 13 of 1st TFT30 is formed on the insulating substrate 10 which consists of quartz glass, alkali free glass, etc. In that active layer 43, ion doping of p mold impurity is performed to the both sides of channel 43c which is genuineness genuineness or

substantially, and this channel 43c, source 43s and drain 43d is prepared in the gate electrode 41 upper part, and p mold channel TFT is constituted.
[0028] On this active layer 43, the gate electrode 41 which consists of refractory metals, such as the gate dielectric film 12 which consists of SiO2 film, and Cr, Mo, is formed.
[0029] And the interlayer insulation film 15 by which the laminating was carried out to the order of SiO2 film, an SiN film, and SiO2 film is formed the whole surface on gate dielectric film 12 and the gate electrode 41. The drive power-source line 53 connected to the drive power source which consists of aluminum on it and is supplied to EL element 60 is formed. Then, the flattening insulator layer 17 which consists of organic resin all over the drive power-source line 53 being included, and makes a front face flat is deposited, and contact holes C1, C2, and C3 are established in the location corresponding to a part of source 43s drain 43d and the drive power-source line 53 of the flattening insulator layer 17. And the resistance 80 which connected the anode plate 61 of the EL element in contact with source 43s, and drain 43d and the drive power-source line 53 by ITO which is a transparence electrical conducting material is formed on the flattening insulator layer 17 through these contact holes.
[0030] After forming these anode plates 61 and resistance 80, the insulator layer 68 covered to the circumference of an anode plate 61 is formed. That is, the circumference of an anode plate 61 is covered and the insulator layer 68 which has opening is formed in the center section of the anode plate 61. This insulator layer 68 has the function to prevent short-circuit with the cathode 67 which originates in the level difference by the thickness of an anode plate 61, and is produced while insulating the 1st hole transportation layer 62 of an EL element and resistance 80 which are prepared in the upper layer of resistance 80.
[0031] And the 1st hole transportation layer 62, the 2nd hole transportation layer 63, a luminous layer 64, the electronic transportation layer 65, and cathode 67 are formed in the front face of the insulator layer 68 which was made to extend even around an anode plate 61 and an anode plate 61, and was formed in order like the conventional El component 60. A luminous layer 64 considers as a larger area than an anode plate 61, and is not formed in the whole surface like other 1st hole transportation layers 62, the 2nd hole transportation layer 63, the electronic transportation layer 65, and cathode 67. Moreover, a luminous layer 64 can change the color made to emit light by changing the ingredient. In addition, cathode 67 is common potential in each display pixel 50.
[0032] Thus, it can prevent changing the current supplied to EL element 60 from 2nd TFT40 by forming the resistance 80 which consists of ITO between the drive power-source line 53 of an EL element, and 43d of drain electrodes.
[0033] As the dotted line of above-mentioned drawing 4 shows, when the Vg-Id property of 2nd TFT40 which drives an EL element is subsided in fluctuation in the range between Curves b from Curve a and the current value in a conventional property and a certain gate voltage compares, according to this invention, it turns out to the fluctuation having been I1 conventionally that it is about 70 small% from it.

[0034] In this way, since the luminescence brightness of an EL element is stabilized and it can obtain, a good display can be obtained.
[0035] Moreover, since it can form without increasing a new process by forming ITO of the same ingredient as an anode plate 61 in anode plate 61 formation and coincidence as an ingredient of resistance 80, it can form without leading to process increase, and cost increase is not caused.
[0036] In addition, in the gestalt of this operation, although 2nd TFT40 explained the so-called top gate type which has an active layer 43 in a lower layer rather than the gate electrode 41 of TFT, this invention is not limited to it, and even if it is the so-called bottom gate type which has an active layer 43 in the upper layer rather than the gate electrode 41 of TFT, it can acquire the same effectiveness. Also in 1st TFT30, a top gate mold or a bottom gate mold may be used.
[0037] Moreover, in this application, a drain shall mean the field where a current flows into TFT, and the source shall mean the field where a current flows out of TFT.
[0038] Moreover, in the gestalt of above-mentioned operation, although the case where the gate electrodes 11 and 41 were double-gate structures was explained, even if the invention in this application

is not limited to it and has a single gate or three multi-gate structures or more, it can do so the same effectiveness as this application.
[0039] Moreover, in the gestalt of above-mentioned operation, although the case where the 2nd TFT was p mold channel TFT was shown, the n-type channel TFT which introduced the impurity of n mold is sufficient as the 2nd TFT.
[0040] Moreover, in the gestalt of above-mentioned operation, although the p-Si film was used as an active layer, a microcrystal silicone film or an amorphous silicone film may be used.
[0041]
[Effect of the Invention] According to the EL display of this invention, it can prevent changing the current supplied to an EL element, and the stable display can be obtained from TFT which drives an EL element.

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[Translation done.]

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CLAIMS

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[Claim(s)]
[Claim 1] The electroluminescence display which is a electroluminescence display equipped with the drive power-source line which supplies the current from the drive power source which drives the electroluminescent element which has a luminous layer, and said electroluminescent element between an anode plate and cathode, and the thin film transistor which the drain is connected to this drive power-source line, controls the current from said drive power source, and is supplied to said electroluminescent element, and is characterized by to have resistance between said drive power-source lines and said drains.
[Claim 2] The electroluminescent element which has a luminous layer between an anode plate and cathode, The 1st thin film transistor which controls the timing which supplies the current which drives said electroluminescent element, The drive power-source line which supplies the current from the drive power source which drives said electroluminescent element, It is the electroluminescence display equipped with the thin film transistor which the drain is connected to this drive power-source line, controls the current from said drive power source, and is supplied to said electroluminescent element. The electroluminescence display characterized by having resistance between said drive power-source lines and said drains.
[Claim 3] The electroluminescence display according to claim 1 or 2 characterized by resistance between said drive power-source lines and said sources consisting of the same ingredient as said anode plate.

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[Translation done.]

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]
[Drawing 1] It is the representative circuit schematic of EL display of this invention.
[Drawing 2] It is the top view showing the gestalt of operation of EL display of this invention.
[Drawing 3] It is the sectional view showing the gestalt of operation of EL display of this invention.
[Drawing 4] It is the property Fig. showing the property of TFT.
[Drawing 5] It is the representative circuit schematic of the conventional EL display.
[Drawing 6] It is the top view of the conventional EL display.
[Drawing 7] It is the sectional view of the conventional EL display.
[Description of Notations]
30 1st TFT
13s, 13s Source
13d, 13d Drain
13c, 13c Channel
13LD, 13LD LDD field
11 41 Gate electrode
40 2nd TFT
50 Drive Power Source
53 Drive Power-Source Line
60 Organic EL Device
80 Resistance

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[Translation done.]

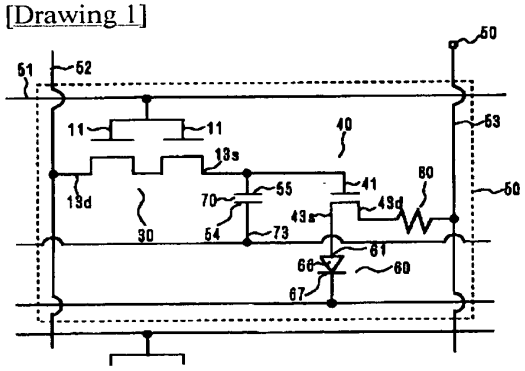
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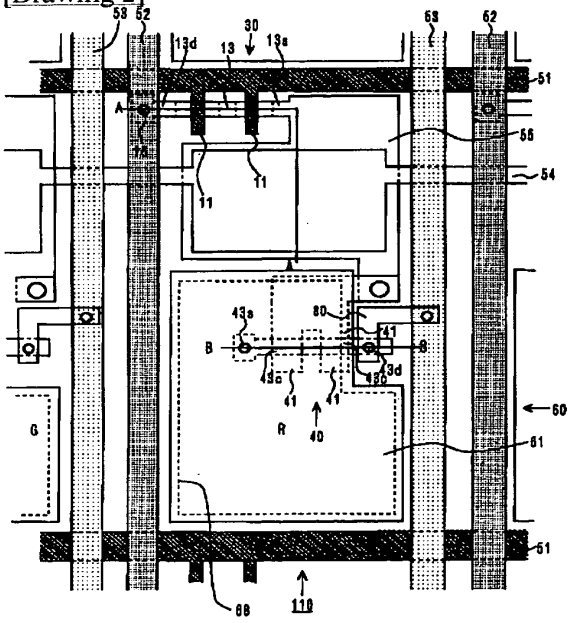
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3.In the drawings, any words are not translated.

DRAWINGS

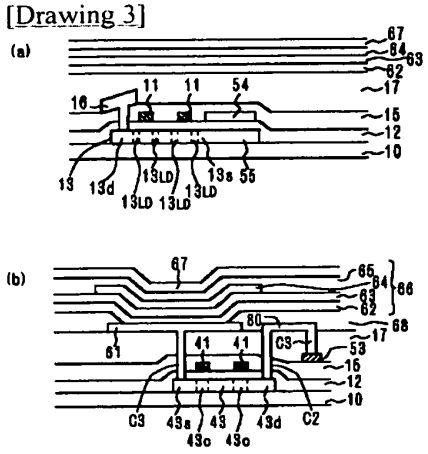
[Drawing 1]



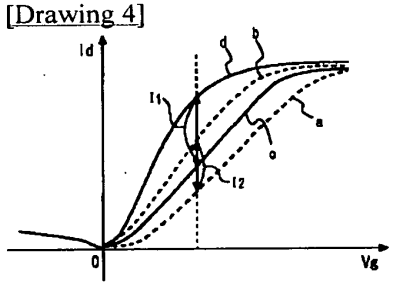

[Drawing 2]



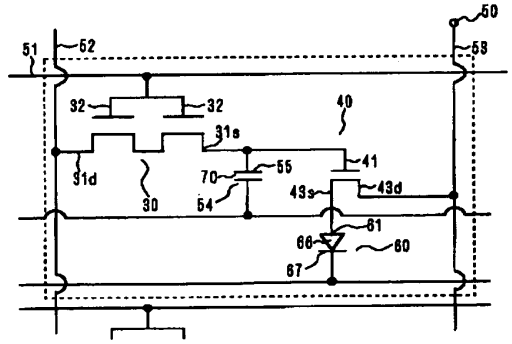
[Drawing 3]



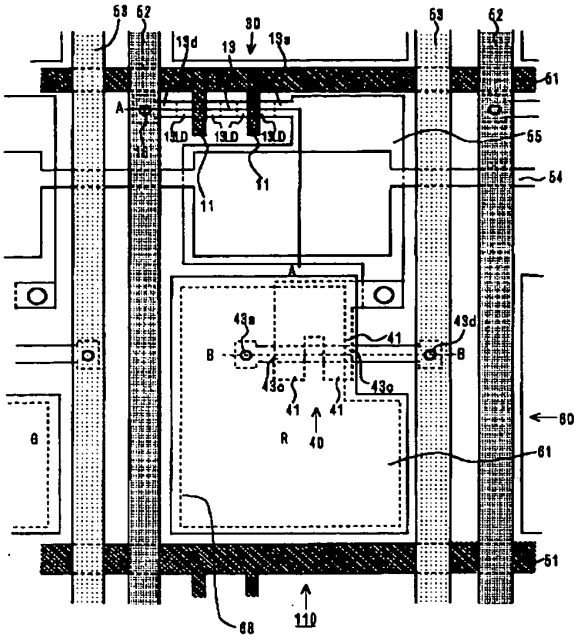

[Drawing 4]



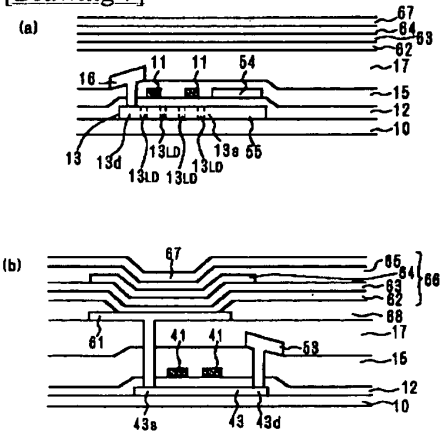

[Drawing 5]




[Drawing 6]



[Drawing 7]



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[Translation done.]

# PATENT ABSTRACTS OF JAPAN

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(43)Date of publication of application : 08.09.2000

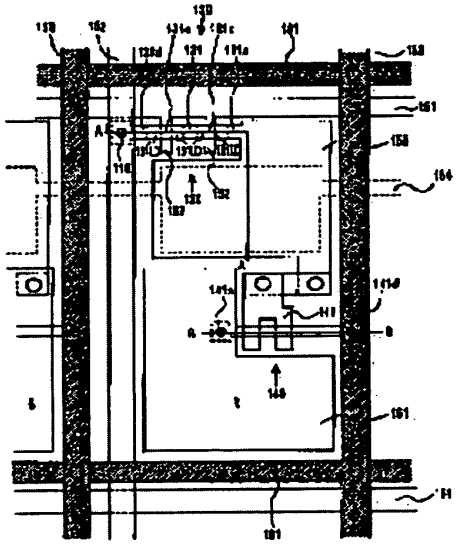
51)Int.Cl. G09F 9/30
H05B 33/14
H05B 33/26

21)Application number : 11-046741
22)Date of filing : 24.02.1999

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54) ELECTROLUMINESCENCE DISPLAY DEVICE

57)Abstract:
ROBLEM TO BE SOLVED: To provide an EL display device capable of btaining a bright display by supplying a current which is to be ntrinsically supplied to EL element while suppressing a lowering of ower source current due to resistance of driving power source line hich is caused by distance from a driving power source input terminal. OLUTION: In this device, respective driving power source lines 153 hich are lines for supplying driving currents from a driving power ource 150 to organic EL elements 160 formed in the display pixel area rovided with display pixels are provided and respective driving power ource lines 153 arranged in adjacent display pixels are connected with ypass lines 181 for every display pixel in the display pixel area and, hus, an organic EL display device capable of obtaining a bright display is btained by supplying currents which are to be intrinsically supplied to L elements to the organic EL elements while suppressing lowering of ower source currents due to resistances of driving power source lines 53.



EGAL STATUS

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|---|---|
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| Ｈ０５Ｂ　33/14 | | Ｈ０５Ｂ　33/14 | Ａ | ５Ｃ０９４ |
| 33/26 | | 33/26 | Ｚ | |

審査請求　未請求　請求項の数１　ＯＬ　（全６頁）

(21)出願番号　特願平11－46741

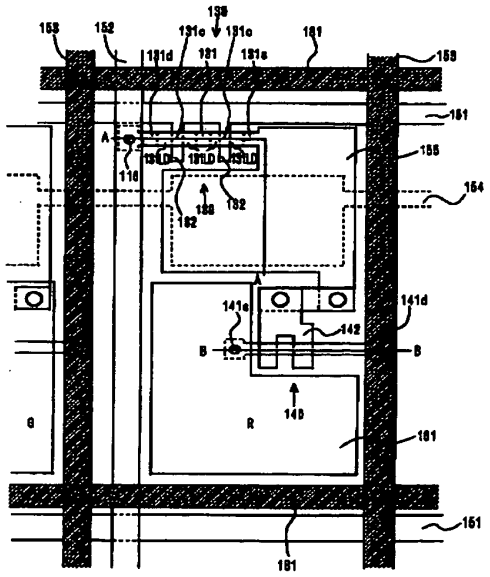
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最終頁に続く

(54)【発明の名称】　エレクトロルミネッセンス表示装置

(57)【要約】
【課題】　駆動電源入力端子からの距離に起因する駆動電源線の抵抗による電源電流の低下を抑制し、本来供給されるべき電流がＥＬ素子に供給して、明るい表示を得ることができるＥＬ表示装置を提供する。
【解決手段】　表示画素を備えた表示画素領域に形成された有機ＥＬ素子１６０に駆動電源１５０からの駆動電流を供給するための各駆動電源線１５３であって、隣接する各表示画素に配置された各駆動電源線１５３は、表示画素領域内においてバイパス線１８１によって各表示画素ごとに接続されており、それによって駆動電源線１５３の抵抗による電源電流の低下を抑制し、本来供給されるべき電流が有機ＥＬ素子に供給されて明るい表示を得ることができる有機ＥＬ表示装置を得ることができる。



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【特許請求の範囲】

【請求項１】　陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、半導体膜から成る能動層のドレインがドレイン信号線に接続され、ゲートがゲート信号線にそれぞれ接続された第１の薄膜トランジスタと、半導体膜からなる能動層のドレインが前記エレクトロルミネッセンス素子の駆動電源線に接続され、ゲートが前記第１の薄膜トランジスタのソースに接続され、ソースが前記エレクトロルミネッセンス素子に接続された第２の薄膜トランジスタとを備えた表示画素がマトリクス状に配列して成る表示画素領域を有するエレクトロルミネッセンス表示装置であって、隣接する前記各表示画素に配置された前記各駆動電源線が、前記表示画素領域においてバイパス線によって接続されていることを特徴とするエレクトロルミネッセンス表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、エレクトロルミネッセンス素子及び薄膜トランジスタを備えたエレクトロルミネッセンス表示装置に関する。

【０００２】

【従来の技術】近年、エレクトロルミネッセンス（Electro Luminescence：以下、「ＥＬ」と称する。）素子を用いたＥＬ表示装置が、ＣＲＴやＬＣＤに代わる表示装置として注目されており、例えば、そのＥＬ素子を駆動させるスイッチング素子として薄膜トランジスタ（Thin Film Transistor：以下、「ＴＦＴ」と称する。）を備えたＥＬ表示装置の研究開発も進められている。

【０００３】図３に有機ＥＬ表示装置の１表示画素を示す平面図を示し、図４に有機ＥＬ表示装置の複数の表示画素の等価回路図を示し、図５（ａ）に図３中のＡ－Ａ線に沿った断面図を示し、図５（ｂ）に図３中のＢ－Ｂ線に沿った断面図を示す。

【０００４】図３、図４及び図５に示すように、ゲート信号線１５１とドレイン信号線１５２とに囲まれた領域に各表示画素が形成されている。両信号線の交点付近にはスイッチング素子である第１のＴＦＴ１３０が備えられており、そのＴＦＴ１３０のソース１３１ｓは後述の保持容量電極１５４との間で容量をなす容量電極１５５を兼ねるとともに、有機ＥＬ素子を駆動する第２のＴＦＴ１４０のゲート１４２に接続されている。第２のＴＦＴ１４０のソース１４１ｓは有機ＥＬ素子の陽極１６１に接続され、他方のドレイン１４１ｄは有機ＥＬ素子を駆動する駆動電源線１５３に接続されている。

【０００５】また、ＴＦＴの付近には、ゲート信号線１５１と並行に保持容量電極１５４が配置されている。この保持容量電極１５４はクロム等から成っており、ゲート絶縁膜１１２を介して第１のＴＦＴ１３０のソース１３１ｓと接続された容量電極１５５との間で電荷を蓄積して容量を成している。この保持容量は、第２のＴＦＴ１４０のゲート１４２に印加される電圧を保持するために設けられている。

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【０００６】まず、スイッチング用のＴＦＴである第１のＴＦＴ１３０について説明する。

【０００７】図３及び５（ａ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１１０上に、クロム（Ｃｒ）、モリブデン（Ｍｏ）などの高融点金属からなるゲート電極１３２を兼ねたゲート信号線１５１及びＡｌから成るドレイン信号線１５２を備えており、有機ＥＬ素子の駆動電源でありＡｌから成る駆動電源線１５３を配置する。

【０００８】続いて、ゲート絶縁膜１１２、及び多結晶シリコン（Poly-Silicon、以下、「ｐ－Ｓｉ」と称する。）膜からなる能動層１３１を順に形成し、その能動層１３１には、いわゆるＬＤＤ（Lightly Doped Drain）構造が設けられている。即ち、ゲート１３２の両側に低濃度領域１３１ＬＤとその外側に高濃度領域のソース１３１ｓ及びドレイン１３１ｄが設けられている。

【０００９】そして、ゲート絶縁膜１１２、能動層１３１及びストッパ絶縁膜１１４上の全面には、$SiO_2$膜、ＳｉＮ膜及び$SiO_2$膜の順に積層された層間絶縁膜１１５を設け、ドレイン１４１ｄに対応して設けたコンタクトホールにＡｌ等の金属を充填してドレイン電極１１６を設ける。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１１７を設ける。

【００１０】次に、有機ＥＬ素子の駆動用のＴＦＴである第２のＴＦＴ１４０について説明する。

【００１１】図５（ｂ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１１０上に、Ｃｒ、Ｍｏなどの高融点金属からなるゲート電極１４２を設け、ゲート絶縁膜１１２、及びｐ－Ｓｉ膜からなる能動層１４１を順に形成し、その能動層１４１には、ゲート電極１４２上方に真性又は実質的に真性であるチャネル１４１ｃと、このチャネル１４１ｃの両側に、ｐ型不純物のイオンドーピングを施してソース１４１ｓ及びドレイン１４１ｄを設けて、ｐ型チャネルＴＦＴを構成する。

【００１２】そして、ゲート絶縁膜１１２及び能動層１４１上の全面には、$SiO_2$膜、ＳｉＮ膜及び$SiO_2$膜の順に積層された層間絶縁膜１１５を形成し、ドレイン１４１ｄに対応して設けたコンタクトホールにＡｌ等の金属を充填して駆動電源１５０に接続された駆動電源線１５３を配置する。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１１７を形成して、その平坦化絶縁膜１１７のソース１４１ｓに対応した位置にコンタクトホールを形成し、このコンタクトホールを介してソース１４１ｓとコンタクトしたＩＴＯ（Indium Thin Oxide）から成る透明電極、即ち有機ＥＬ素子の陽極１６１を平坦化絶縁膜１１７上に設ける。

【００１３】有機ＥＬ素子１６０は、ＩＴＯ等の透明電

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極から成る陽極１６１、ＭＴＤＡＴＡ（4,4-bis（3-methylphenylphenylamino)biphenyl）から成る第１ホール輸送層１６２、及びＴＰＤ（4,4,4-tris(3-methylphenylphenylamino)triphenylanine）からなる第２ホール輸送層１６３、キナクリドン（Quinacridone）誘導体を含むＢｅｂｑ2（10-ベンゾ〔ｈ〕キノリノール－ベリリウム錯体）から成る発光層１６４及びＢｅｂｑ2から成る電子輸送層１６５からなる発光素子層１６６、マグネシウム・インジウム合金から成る陰極１６７がこの順番で積層形成された構造である。この陰極１６７は、図３に示した有機ＥＬ表示素子の全面、即ち紙面の全面に設けられている。

【００１４】また有機ＥＬ素子は、陽極から注入されたホールと、陰極から注入された電子とが発光層の内部で再結合し、発光層を形成する有機分子を励起して励起子が生じる。この励起子が放射失活する過程で発光層から光が放たれ、この光が透明な陽極から透明絶縁基板を介して外部へ放出されて発光する。

【００１５】このように、第１のＴＦＴ１３０のソース１３１ｓから印加された電荷が保持容量１７０に蓄積されるとともに第２のＴＦＴ１４０のゲート１４２に印加されてその電圧に応じて有機ＥＬ素子は発光する。

【００１６】

【発明が解決しようとする課題】ところが、図４に示すように有機ＥＬ素子を駆動する駆動電源に接続された各駆動電源線は、表示画素領域外に設けた駆動電源入力端子１８０に接続されており、そして縦に並んだ表示画素ごとに接続されて配置されている。そのため、駆動電源入力端子１８０から遠ざかるにつれて電源線の抵抗がその長さに応じて大きくなるので、駆動電源入力端子１８０から遠い位置にある表示画素の有機ＥＬ素子１６０には本来供給されるべき電流が印加されなくなり、表示が暗くなるという欠点があった。

【００１７】そこで本発明は、上記の従来の欠点に鑑みて為されたものであり、駆動電源線の抵抗による電源電流の低下を抑制し、本来供給されるべき電流がＥＬ素子に供給して、明るい表示を得ることができるＥＬ表示装置を提供することを目的とする。

【００１８】

【課題を解決するための手段】本発明のＥＬ表示装置は、陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、半導体膜から成る能動層のドレインがドレイン信号線に接続され、ゲートがゲート信号線にそれぞれ接続された第１の薄膜トランジスタと、半導体膜からなる能動層のドレインが前記エレクトロルミネッセンス素子の駆動電源線に接続され、ゲートが前記第１の薄膜トランジスタのソースに接続され、ソースが前記エレクトロルミネッセンス素子に接続された第２の薄膜トランジスタとを備えた表示画素がマトリクス状に配列して成る表示画素領域を有するエレクトロルミネッセンス表示装置であって、隣接する前記各表示画素に配置された前記各駆動電源線が、前記表示画素領域においてバイパス線によって接続されているものである。

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【００１９】

【発明の実施の形態】本発明のＥＬ表示装置について以下に説明する。

【００２０】図１に本発明を有機ＥＬ表示装置に適用した場合の１表示画素を示す平面図を示し、図２に有機ＥＬ表示装置の複数の表示画素の等価回路図を示す。なお、図１中のＡ－Ａ線に沿った断面図、及び図１中のＢ－Ｂ線に沿った断面図は前述の図５と同じであるので図示を省略する。

【００２１】なお、本実施の形態においては、第１及び第２のＴＦＴ３０，４０ともに、ゲート電極を能動層１３の下方に設けたいわゆるボトムゲート型のＴＦＴを採用した場合であり、能動層としてｐ－Ｓｉ膜を用いた場合を示す。またゲート電極１１，４２がダブルゲート構造であるＴＦＴの場合を示す。

【００２２】また、有機ＥＬ表示装置は、ガラスや合成樹脂などから成る基板１１０、又は導電性を有する基板あるいは半導体等の基板上に$SiO_2$やＳｉＮなどの絶縁膜を形成した基板１１０上に、ＴＦＴ及び有機ＥＬ素子を順に積層形成して成る。

【００２３】図１及び図２に示すように、ゲート信号線１５１とドレイン信号線１５２とに囲まれた領域に表示画素が形成されている。有機ＥＬ素子１６０及びＴＦＴ１３０，１４０を備えた表示画素が基板１１０上にマトリクス状に配置されることにより有機ＥＬ表示装置が形成される。

【００２４】両信号線の交点付近には第１のＴＦＴ１３０が備えられており、そのＴＦＴ１３０のソース１３１ｓは保持容量電極１５４との間で容量をなす容量電極１５５を兼ねるとともに、第２のＴＦＴ１４０のゲート１４２に接続されている。第２のＴＦＴのソース１４１ｓは有機ＥＬ素子１６０の陽極１６１に接続され、他方のドレイン１４１ｄは有機ＥＬ素子を駆動する駆動電源線１５３に接続されている。

【００２５】また、ＴＦＴの付近には、ゲート信号線１５１と並行に第１の保持容量電極１５４が配置されている。この第１の容量電極１５４はクロム等から成っており、ゲート絶縁膜１１２を介して第１のＴＦＴ１３０のソース１３１ｓと接続され多結晶シリコン膜から成る第２の保持容量電極１５４との間で電荷を蓄積して容量を成している。

【００２６】スイッチング用のＴＦＴである第１のＴＦＴ１３０は、図１及び図５（ａ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１１０上に、Ｃｒ、Ｍｏなどの高融点金属からなるゲート電極１３２を兼ねたゲート信号線１５１及びＡｌから成るドレイン信号線１５２を備えており、有機ＥＬ素子の駆動電

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源でありＡｌから成る駆動電源線１５３を配置する。また、ゲート電極と同層にＣｒ、Ｍｏなどの高融点金属から成る第１の保持容量電極５４が設けられている。

【００２７】続いて、ゲート絶縁膜１１２、及びｐ－Ｓｉ膜からなる能動層１３１を順に積層する。ゲート電極１３２の上方であって能動層１３１上には、ソース１３１ｓ及びドレイン１３１ｄを形成する際のイオン注入時にチャネル１３１ｃにイオンが入らないようにチャネル１３１ｃを覆うマスクとして機能する$SiO_2$膜から成るストッパ絶縁膜１１４が設けられる。その能動層１３１にはいわゆるＬＤＤ構造が設ける。即ち、ゲート１３２の両側に低濃度領域１３１ＬＤとその外側に高濃度領域の１３１ｓ及びドレイン１３１ｄが設けられている。また、能動層のｐ－Ｓｉ膜は保持容量電極１５４上にまで延在されており、第２の保持容量電極１５５としてゲート絶縁膜１１２を介して保持容量電極１５４との間で保持容量を成す。

【００２８】そして、ゲート絶縁膜１１２、能動層１３１及びストッパ絶縁膜１１４上の全面には、$SiO_2$膜、ＳｉＮ膜及び$SiO_2$膜の順に積層された層間絶縁膜１１５を設け、ドレイン１４１ｄに対応して設けたコンタクトホールにＡｌ等の金属を充填してドレイン電極１１６を設ける。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１１７を設ける。

【００２９】次に、有機ＥＬ素子１６０の駆動用のＴＦＴである第２のＴＦＴ１４０について説明する。

【００３０】図５（ｂ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１１０上に、Ｃｒ、Ｍｏなどの高融点金属からなるゲート電極１４２を形成する。

【００３１】ゲート絶縁膜１１２、及びｐ－Ｓｉ膜からなる能動層１４１を順に形成する。

【００３２】その能動層１４１には、ゲート電極１４２上方に真性又は実質的に真性であるチャネル１４１ｃと、このチャネル１４１ｃの両側に、その両側をレジストにてカバーしてｐ型不純物である例えばボロン（Ｂ）をイオンドーピングしてソース１４１ｓ及びドレイン１４１ｄが設けられている。

【００３３】そして、ゲート絶縁膜１１２及び能動層１４１上の全面に、$SiO_2$膜、ＳｉＮ膜及び$SiO_2$膜の順に積層された層間絶縁膜１１５を形成し、ソース１４１ｓに対応して設けたコンタクトホールにＡｌ等の金属を充填して駆動電源１５０に接続された駆動電源線１５３を形成する。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１１７を形成する。そして、その平坦化絶縁膜１１７及び層間絶縁膜１１５のドレイン１４１ｄに対応した位置にコンタクトホールを形成し、このコンタクトホールを介してドレイン１４１ｄとコンタクトしたＩＴＯから成る透明電極、即ち有機ＥＬ素子の陽極１６１を平坦化絶縁膜１１７上に形成する。

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【００３４】有機ＥＬ素子１６０の構造は従来の技術で説明した図５に示した構造と同じであるので説明を省略する。

【００３５】ここで、有機ＥＬ素子１６０に駆動電流を供給する駆動電源線１５３について説明する。

【００３６】駆動電源線１５３は、表示画素領域内において、従来のように縦に並ぶいわゆる列方向に延在して配置されており、列方向の各表示画素に接続されて駆動電流を供給している。

【００３７】更に、本発明においては、各駆動電源線１５３は隣接する各表示画素に接続された駆動電源線１５３を、横に並ぶいわゆる行方向に延在させたバイパス線１８１によって接続させる。即ち、隣接する表示画素には導電位の電圧が印加されることになる。このバイパス線１８１はＡｌ等の材料によって形成される。

【００３８】このように、隣接する各表示画素の駆動電源線１５３をバイパス線１８１で接続することにより、駆動電源入力端子１８０から遠ざかるにつれて駆動電源線１５３の配線の長さによる抵抗が増大することを抑制できるため、各表示画素に設けられた有機ＥＬ素子１６０に本来供給すべき電流を供給することができるので、抵抗増大による表示の明るさの低下を防止することが可能である。

【００３９】また、図１に示すように駆動電源線１５３及びバイパス線１８１の線幅を広くすることにより、抵抗を低減することができる。そのため、本来供給されるべき電流を各表示画素に設けた有機ＥＬ素子１６０に供給することができ、表示が暗くなることを防止できる。また、各線幅を広くすることにより、エレクトロマイグレーションの発生を防止することもできる。このときの線幅としては例えばドレイン信号線１５２の線幅よりも広ければよい。

【００４０】なお、上述の実施の形態においては、ゲート電極１１１，１１４がダブルゲート構造の場合について説明したが、本願発明はそれに限定されるものではなく、シングルゲートあるいは３つ以上のマルチゲート構造を有していても本願と同様の効果を奏することが可能である。

【００４１】また、上述の実施の形態においては、半導体膜としてｐ－Ｓｉ膜を用いたが、微結晶シリコン膜又は非晶質シリコン膜等の半導体膜を用いても良い。

【００４２】更に、上述の実施の形態においては、有機ＥＬ表示装置について説明したが、本発明はそれに限定されるものではなく、発光層が無機材料から成る無機ＥＬ表示装置にも適用が可能であり、同様の効果が得られる。

【００４３】

【発明の効果】本発明のＥＬ表示装置は、駆動電源線の長さによる抵抗の増大を低減し、本来供給されるべき電流を各表示画素のＥＬ表示素子に供給して、暗い表示に

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なることを防止することができるＥＬ表示装置を得ることができる。

【図面の簡単な説明】

【図１】本発明のＥＬ表示装置の表示画素の平面図である。

【図２】本発明のＥＬ表示装置の等価回路図である。

【図３】従来のＥＬ表示装置の表示画素の平面図である。

【図４】従来のＥＬ表示装置の等価回路図である。

【図５】ＥＬ表示装置の断面図である。

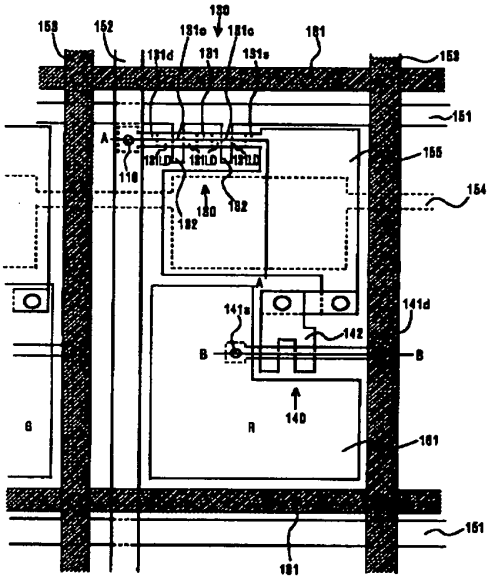
【符号の説明】

１３０　　第１のＴＦＴ

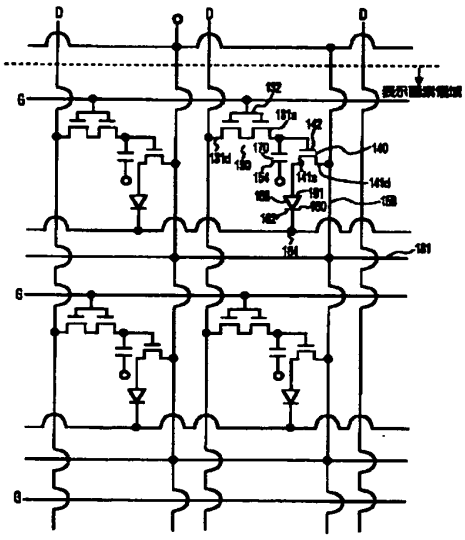
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| | |
|---|---|
| １３１ｓ、１４１ｓ | ソース |
| １３１ｄ、１４１ｄ | ドレイン |
| １３１ｃ、１４１ｃ | チャネル |
| １３１ＬＤ、１４１ＬＤ | ＬＤＤ領域 |
| １３２、１４２ | ゲート |
| １４０ | 第２のＴＦＴ |
| １５３ | 駆動電源線 |
| １５４ | 第１の保持容量電極 |
| １５５ | 第２の保持容量電極 |
| １６０ | 有機ＥＬ素子 |
| １８１ | バイパス線 |

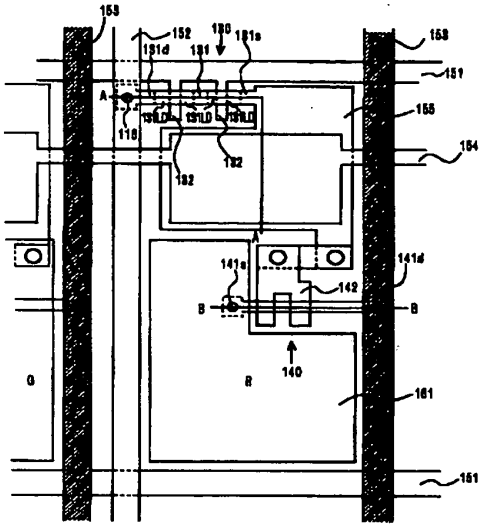
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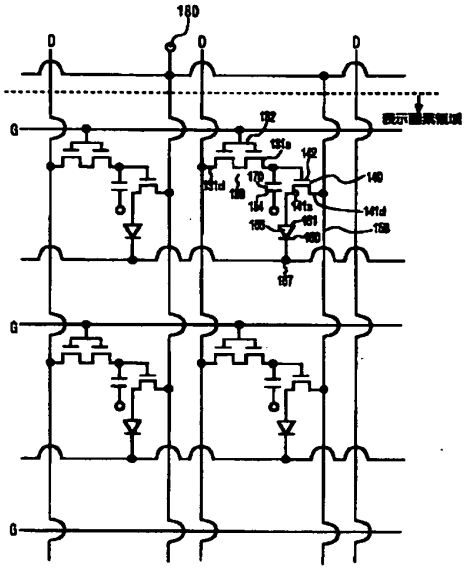
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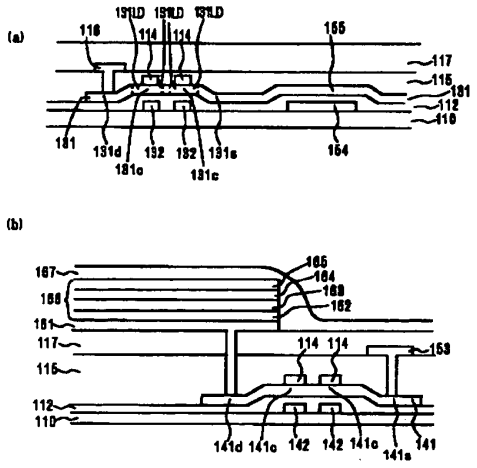
【図３】



【図４】



【図５】



フロントページの続き

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Ｆターム(参考)　3K007 AB02 BA06 CA01 DA02 GA04
5C094 AA10 AA25 BA03 BA29 CA19
DB04 EA10

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the electroluminescence display equipped with the electroluminescent element and the thin film transistor.
[0002]
[Description of the Prior Art] In recent years, researches and developments of EL display equipped with the thin film transistor ("TFT" is called below Thin Film Transistor:.) as a switching element which it is observed [ switching element ] as a display which EL display using an electroluminescence ("EL" is called below Electro Luminescence:.) component replaces with CRT or LCD, for example, makes the EL element drive are also furthered.
[0003] The top view showing 1 display pixel of an organic electroluminescence display in drawing 3 is shown, the representative circuit schematic of two or more display pixels of an organic electroluminescence display is shown in drawing 4 , the sectional view which met drawing 5 (a) at the A-A line in drawing 3 is shown, and the sectional view which met drawing 5 (b) at the B-B line in drawing 3 is shown.
[0004] As shown in drawing 3 , drawing 4 , and drawing 5 , each display pixel is formed in the field surrounded by the gate signal line 151 and the drain signal line 152. It has 1st TFT130 which is a switching element near the intersection of both signal lines, and the source 131s of TFT130, while serving as the capacity electrode 155 which makes capacity between the below-mentioned retention volume electrodes 154, it connects with the gate 142 of 2nd TFT140 which drives an organic EL device. It connects with the anode plate 161 of an organic EL device source 141s of 2nd TFT140, and connects with the drive power-source line 153 which drives an organic EL device drain 141d of another side.
[0005] Moreover, near TFT, the retention volume electrode 154 is arranged in parallel with the gate signal line 151. This retention volume electrode 154 consists of chromium etc., accumulated the charge between the capacity electrodes 155 connected with source 131s of 1st TFT130 through gate dielectric film 112, and has accomplished capacity. This retention volume is prepared in order to hold the electrical potential difference impressed to the gate 142 of 2nd TFT140.
[0006] First, 1st TFT130 which is TFT for switching is explained.
[0007] As shown in drawing 3 and 5 (a), it has the drain signal line 152 which consists of the gate signal line 151 and aluminum which served as the gate electrode 132 which consists of refractory metals, such as chromium (Cr) and molybdenum (Mo), on the insulating substrate 110 which consists of quartz glass, alkali free glass, etc., and the drive power-source line 153 which is the drive power source of an organic EL device, and consists of aluminum is arranged.
[0008] Then, the active layer 131 which consists of gate dielectric film 112 and polycrystalline silicon ("p-Si" is called Poly-Silicon and the following.) film is formed in order, and the so-called LDD (Lightly Doped Drain) structure is prepared in the active layer 131. That is, source 131s [ of a high concentration field ] and drain 131d is prepared in low concentration field 131LD and its outside at the both sides of the gate 132.

[0009] And the contact hole which formed the interlayer insulation film 115 by which the laminating was carried out to the order of SiO2 film, an SiN film, and SiO2 film the whole surface on gate dielectric film 112, an active layer 131, and the stopper insulator layer 114, and was prepared corresponding to drain 141d is filled up with metals, such as aluminum, and the drain electrode 116 is formed in it. Furthermore, the flattening insulator layer 117 which consists of organic resin and makes a front face flat is formed in the whole surface.
[0010] Next, 2nd TFT140 which is TFT for the drive of an organic EL device is explained.
[0011] As shown in drawing 5 (b), on the insulating substrate 110 which consists of quartz glass, alkali free glass, etc. The gate electrode 142 which consists of refractory metals, such as Cr and Mo, is formed, and the active layer 141 which consists of gate dielectric film 112 and p-Si film is formed in order. To the active layer 141 Ion doping of p mold impurity is performed to the both sides of channel 141c which is genuineness genuineness or substantially, and this channel 141c, source 141s and drain 141d is prepared in the gate electrode 142 upper part, and p mold channel TFT is constituted.
[0012] And the interlayer insulation film 115 by which the laminating was carried out to the order of SiO2 film, an SiN film, and SiO2 film is formed the whole surface on gate dielectric film 112 and an active layer 141, and the drive power-source line 153 which filled up the contact hole prepared corresponding to drain 141d with metals, such as aluminum, and was connected to the drive power source 150 is arranged. Furthermore, the flattening insulator layer 117 which consists of organic resin and makes a front face flat is formed, a contact hole is formed in the location corresponding to source 141s of that flattening insulator layer 117, and the transparent electrode 161 which consists of ITO (Indium Thin Oxide) which contacted source 141s through this contact hole, i.e., the anode plate of an organic EL device, is formed in the whole surface on the flattening insulator layer 117.
[0013] An organic EL device 160 The anode plate 161, MTDATA which consist of transparent electrodes, such as ITO (4 4-bis ()) The 1st hole transportation layer 162 which consists of 3-methylphenylphenylaminobiphenyl, And TPD () [ 4, 4, ] [ 4-tris] The 2nd hole transportation layer 163 which consists of triphenylanine, (3-methylphenylphenylamino) The Quinacridone (Quinacridone) derivative It is the structure where laminating formation of the light emitting device layer 166 which consists of an electronic transportation layer 165 which consists of the luminous layer 164 which consists of included Bebq2 (10-[benzoh] quinolinol-beryllium complex), and Bebq2, and the cathode 167 which consists of a magnesium indium alloy was carried out in this sequence. This cathode 167 is formed all over the whole surface of the organic electroluminescence display device shown in drawing 3 , i.e., space.
[0014] Moreover, the hole poured in from the anode plate and the electron poured in from cathode recombine an organic EL device inside a luminous layer, it excites the organic molecule which forms a luminous layer, and an exciton produces it. Light is emitted from a luminous layer in the process in which this exciton carries out radiation deactivation, and from a transparent anode plate, this light is emitted to the exterior through a transparence insulating substrate, and emits light.
[0015] Thus, while the charge impressed from source 131s of 1st TFT130 is accumulated in retention volume 170, it is impressed by the gate 142 of 2nd TFT140, and an organic EL device emits light according to the electrical potential difference.
[0016]
[Problem(s) to be Solved by the Invention] However, it connects with the drive power-source input terminal 180 prepared outside the display pixel field, it connects for every display pixel perpendicularly located in a line, and each drive power-source line connected to the drive power source which drives an organic EL device as shown in drawing 4 is arranged. Therefore, since resistance of a power-source line became large according to the die length as it kept away from the drive power-source input terminal 180, the current which should be supplied essentially was no longer impressed to the organic EL device 160 of the display pixel in a location distant from the drive power-source input terminal 180, and there was a fault that a display became dark.
[0017] Then, in view of the above-mentioned conventional fault, it succeeds in this invention, it controls the fall of the power-source current by resistance of a drive power-source line, and the current which

should be supplied essentially supplies it to an EL element, and it aims at offering EL display which can obtain a bright display.
[0018]
[Means for Solving the Problem] The electroluminescent element to which EL display of this invention has a luminous layer between an anode plate and cathode, The 1st thin film transistor by which the drain of the active layer which consists of the semi-conductor film was connected to the drain signal line, and the gate was connected to the gate signal line, respectively, The drain of an active layer which consists of semi-conductor film is connected to the drive power-source line of said electroluminescent element. It is the electroluminescence display which has the display pixel field where the display pixel equipped with the 2nd thin film transistor by which the gate was connected to the source of said 1st thin film transistor, and the source was connected to said electroluminescent element arranges in the shape of a matrix, and changes. Said each drive power-source line arranged at said each adjoining display pixel is connected by the bypass line in said display pixel field.
[0019]
[Embodiment of the Invention] EL display of this invention is explained below.
[0020] The top view showing 1 display pixel at the time of applying this invention to an organic electroluminescence display at drawing 1 is shown, and the representative circuit schematic of two or more display pixels of an organic electroluminescence display is shown in drawing 2 . In addition, since the sectional view which met the A-A line in drawing 1 , and the sectional view which met the B-B line in drawing 1 are the same as above-mentioned drawing 5 , illustration is omitted.
[0021] In addition, in the gestalt of this operation, it is the case where 1st and 2nd TFT(s) 30 and 40 adopt the so-called bottom gate type with which the active layer 13 prepared the gate electrode caudad of TFT, and the case where the p-Si film is used as an active layer is shown. Moreover, the case where it is TFT whose gate electrodes 11 and 42 are double-gate structures is shown.
[0022] Moreover, on the substrate 110 in which insulator layers, such as SiO2 and SiN, were formed on the substrate 110 which consists of glass, synthetic resin, etc., the substrate which has conductivity, or substrates, such as a semi-conductor, an organic electroluminescence display carries out laminating formation, and changes TFT and an organic EL device at order.
[0023] The display pixel is formed in the field surrounded by the gate signal line 151 and the drain signal line 152 as shown in drawing 1 and drawing 2 . An organic electroluminescence display is formed by arranging the display pixel equipped with an organic EL device 160 and TFT130,140 in the shape of a matrix on a substrate 110.
[0024] It has 1st TFT130 near the intersection of both signal lines, and the source 131s of TFT130, while serving as the capacity electrode 155 which makes capacity between the retention volume electrodes 154, it connects with the gate 142 of 2nd TFT140. It connects with the anode plate 161 of an organic EL device 160 source 141s of the 2nd TFT, and connects with the drive power-source line 153 which drives an organic EL device drain 141d of another side.
[0025] Moreover, near TFT, the 1st retention volume electrode 154 is arranged in parallel with the gate signal line 151. This 1st capacity electrode 154 accumulated the charge between the 2nd retention volume electrode 154 which consists of chromium etc., is connected with source 131s of 1st TFT130 through gate dielectric film 112, and consists of a polycrystal silicone film, and has accomplished capacity.
[0026] As shown in drawing 1 and drawing 5 (a), 1st TFT130 which is TFT for switching is equipped with the drain signal line 152 which consists of the gate signal line 151 and aluminum which served as the gate electrode 132 which consists of refractory metals, such as Cr and Mo, on the insulating substrate 110 which consists of quartz glass, alkali free glass, etc., and arranges the drive power-source line 153 which is the drive power source of an organic EL device, and consists of aluminum. Moreover, a gate electrode and the 1st retention volume electrode 54 which changes from refractory metals, such as Cr and Mo, to this layer are formed.
[0027] Then, the laminating of the active layer 131 which consists of gate dielectric film 112 and p-Si film is carried out to order. It is the upper part of the gate electrode 132, and the stopper insulator layer

114 which consists of SiO2 film which functions as ion not going into channel 131c considering channel 131c as a wrap mask at the time of the ion implantation at the time of forming source 131s and drain 131d is formed on an active layer 131. The so-called LDD structure prepares in the active layer 131. That is, 131s and drain 131d of a high concentration field is prepared in low concentration field 131LD and its outside at the both sides of the gate 132. Moreover, the p-Si film of an active layer has extended even on the retention volume electrode 154, and accomplishes retention volume between the retention volume electrodes 154 through gate dielectric film 112 as 2nd retention volume electrode 155.

[0028] And the contact hole which formed the interlayer insulation film 115 by which the laminating was carried out to the order of SiO2 film, an SiN film, and SiO2 film the whole surface on gate dielectric film 112, an active layer 131, and the stopper insulator layer 114, and was prepared corresponding to drain 141d is filled up with metals, such as aluminum, and the drain electrode 116 is formed in it. Furthermore, the flattening insulator layer 117 which consists of organic resin and makes a front face flat is formed in the whole surface.

[0029] Next, 2nd TFT140 which is TFT for the drive of an organic EL device 160 is explained.

[0030] As shown in drawing 5 (b), the gate electrode 142 which consists of refractory metals, such as Cr and Mo, is formed on the insulating substrate 110 which consists of quartz glass, alkali free glass, etc.

[0031] The active layer 141 which consists of gate dielectric film 112 and p-Si film is formed in order.

[0032] At that active layer 141, those both sides are covered in a resist, ion doping of the boron (B) which is p mold impurity is carried out, and source 141s and drain 141d is prepared in the gate electrode 142 upper part at the both sides of channel 141c which is genuineness genuineness or substantially, and this channel 141c.

[0033] And the interlayer insulation film 115 by which the laminating was carried out to the order of SiO2 film, an SiN film, and SiO2 film is formed the whole surface on gate dielectric film 112 and an active layer 141, and the drive power-source line 153 which filled up the contact hole prepared corresponding to source 141s with metals, such as aluminum, and was connected to the drive power source 150 is formed. Furthermore, the flattening insulator layer 117 which consists of organic resin and makes a front face flat is formed in the whole surface. And a contact hole is formed in the location corresponding to drain 141d of that flattening insulator layer 117 and an interlayer insulation film 115, and the transparent electrode 161 which consists of ITO which contacted drain 141d through this contact hole, i.e., the anode plate of an organic EL device, is formed on the flattening insulator layer 117.

[0034] Since the structure of an organic EL device 160 is the same as the structure shown in drawing 5 explained by the Prior art, explanation is omitted.

[0035] Here, the drive power-source line 153 which supplies a drive current to an organic EL device 160 is explained.

[0036] The drive power-source line 153 extends in the so-called direction of a train perpendicularly located in a line like before in a display pixel field, is arranged in it, and it connects with each display pixel of the direction of a train, and it supplies the drive current.

[0037] Furthermore, in this invention, each drive power-source line 153 connects the drive power-source line 153 connected to each adjoining display pixel by the bypass line 181 which made the so-called line writing direction horizontally located in a line extend. That is, the electrical potential difference like electric conduction will be impressed to the adjoining display pixel. This bypass line 181 is formed with ingredients, such as aluminum.

[0038] Thus, since it can control that resistance by the die length of wiring of the drive power-source line 153 increases as it keeps away from the drive power-source input terminal 180 by connecting the drive power-source line 153 of each adjoining display pixel by the bypass line 181 and the current which should supply to the organic EL device 160 formed in each display pixel essentially can supply, it is possible in preventing the fall of the brightness of the display by resistance increase.

[0039] Moreover, resistance can be reduced by making large line breadth of the drive power-source line 153 and the bypass line 181, as shown in drawing 1 . Therefore, the organic EL device 160 which prepared the current which should be supplied essentially in each display pixel can be supplied, and it can prevent that a display becomes dark. Moreover, generating of electromigration can also be prevented

by making each line breadth large. As line breadth at this time, what is necessary is just larger than the line breadth of the drain signal line 152.
[0040] In addition, in the gestalt of above-mentioned operation, although the case where the gate electrode 111,114 was double-gate structure was explained, even if the invention in this application is not limited to it and has a single gate or three multi-gate structures or more, it can do so the same effectiveness as this application.
[0041] Moreover, in the gestalt of above-mentioned operation, although the p-Si film was used as semi-conductor film, semi-conductor film, such as a microcrystal silicone film or an amorphous silicone film, may be used.
[0042] Furthermore, in the gestalt of above-mentioned operation, although the organic electroluminescence display was explained, this invention is not limited to it, and can be applied also to inorganic EL display with which a luminous layer consists of an inorganic material, and the same effectiveness is acquired.
[0043]
[Effect of the Invention] EL display of this invention can reduce increase of resistance by the die length of a drive power-source line, can supply the current which should be supplied essentially to EL display device of each display pixel, and can obtain EL display which can prevent becoming a dark display.

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[Translation done.]

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CLAIMS

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[Claim(s)]
[Claim 1] The electroluminescent element which has a luminous layer between an anode plate and cathode, The 1st thin film transistor by which the drain of the active layer which consists of the semi-conductor film was connected to the drain signal line, and the gate was connected to the gate signal line, respectively, The drain of an active layer which consists of semi-conductor film is connected to the drive power-source line of said electroluminescent element. It is the electroluminescence display which has the display pixel field where the display pixel equipped with the 2nd thin film transistor by which the gate was connected to the source of said 1st thin film transistor, and the source was connected to said electroluminescent element arranges in the shape of a matrix, and changes. The electroluminescence display with which said each drive power-source line arranged at said each adjoining display pixel is characterized by connecting by the bypass line in said display pixel field.

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DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]
[Drawing 1] It is the top view of the display pixel of EL display of this invention.
[Drawing 2] It is the representative circuit schematic of EL display of this invention.
[Drawing 3] It is the top view of the display pixel of the conventional EL display.
[Drawing 4] It is the representative circuit schematic of the conventional EL display.
[Drawing 5] It is the sectional view of EL display.
[Description of Notations]
130 [ ] 1st TFT
131s, 141s Source
131d, 141d Drain
131c, 141c Channel
131LD, 141LD LDD field
132 142 Gate
140 [ ] 2nd TFT
153 [ ] Drive Power-Source Line
154 [ ] 1st Retention Volume Electrode
155 [ ] 2nd Retention Volume Electrode
160 [ ] Organic EL Device
181 [ ] Bypass Line

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[Translation done.]

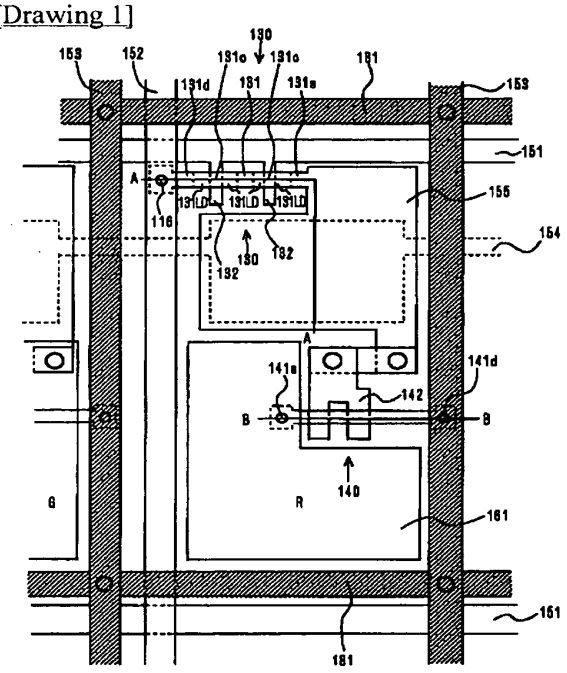
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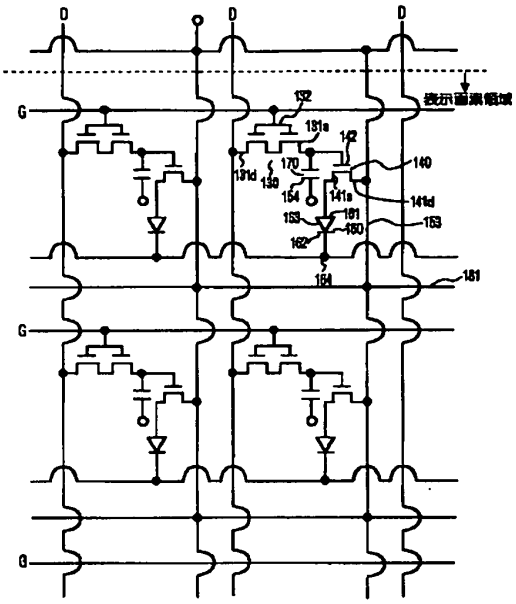
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DRAWINGS

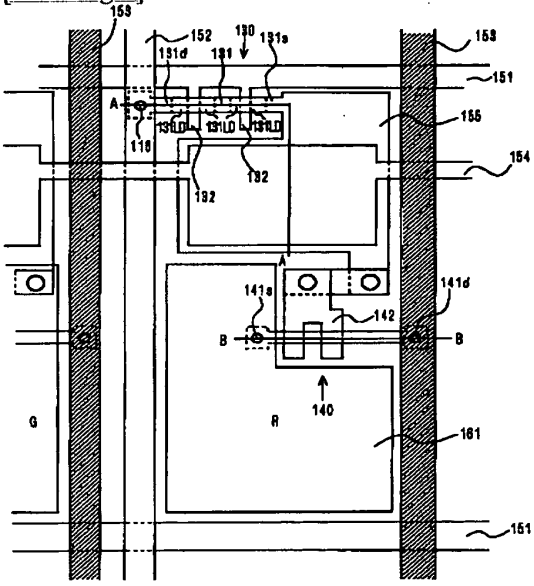
[Drawing 1]



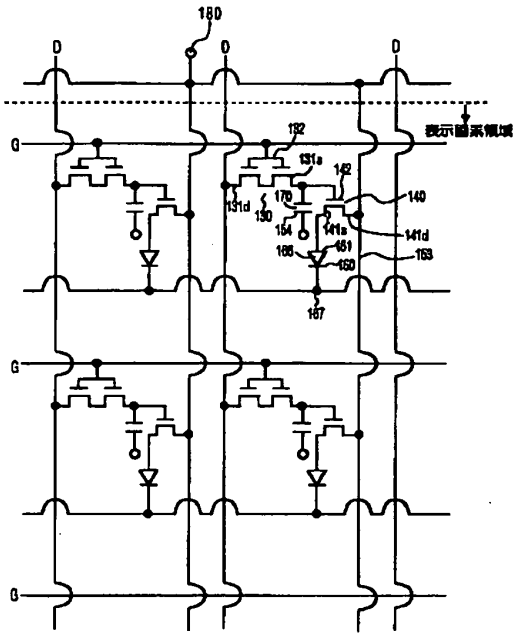

[Drawing 2]



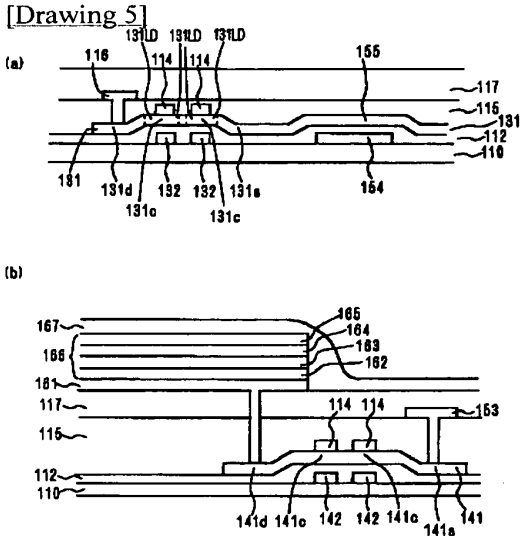

[Drawing 3]




[Drawing 4]




[Drawing 5]




[Translation done.]

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| S11 | 157 | S6 and S10 and @ad<"20021007" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 13:17 |
| S12 | 736502 | ((sam$1 equal$3 similar$3 identic$4 equivalent differen$3 $2chang$3 uniform) with width$4) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 13:58 |
| S13 | 210 | S1 and S6 and S12 and @ad<"20021007" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 13:20 |

# EAST Search History

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|---|---|---|---|---|---|---|
| S14 | 120 | S13 not S11 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 13:22 |
| S15 | 5860 | S4 with width$4 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 13:36 |
| S16 | 64 | S6 and S15 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 13:47 |
| S17 | 100 | S7 and width$4 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 14:05 |
| S18 | 350 | S5 and 345/76.ccls. and (red blue green) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 14:31 |
| S19 | 211 | S18 and width$4 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 14:31 |
| S20 | 67 | S19 and @ad<"20021007" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 14:48 |
| S21 | 699 | S5 and ((sum$3 total$3) with width$1) and @ad<"20021007" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 15:02 |
| S22 | 2 | "6825820".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/03 15:02 |

# EAST Search History

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|---|---|---|---|---|---|---|
| S23 | 2978 | 315/169.2,169.3.ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/04 09:53 |
| S24 | 1100 | ((power voltage) near5 line$1) and ((scan$4 gate$1 select$4 address$4) near5 (line$1 electrode$1)) and S23 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/04 09:54 |
| S25 | 584 | S24 and @ad<"20021007" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2007/05/04 09:54 |

PALM Intranet

Application Number [ ] Submit

IDS Flag Clearance for Application 10676067

IDS Information

| Content | Mailroom Date | Entry Number | IDS Review | Last Modified | Reviewer |
|---|---|---|---|---|---|
| M844 | 2007-03-19 | 46 | Y ☑ | 2007-05-03 15:13:31.0 | dduong1 |
| M844 | 2006-01-27 | 21 | Y ☑ | 2006-11-27 16:30:16.0 | cmason |

Update

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/676,067 | 10/02/2003 | Yojiro Matsueda | 117390 | 7780 |

25944 7590 05/16/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

| EXAMINER | |
|---|---|
| DUONG, DIEU HIEN | |
| ART UNIT | PAPER NUMBER |
| 2821 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 05/16/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | Dieu Hien T. Duong | 2821 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/19/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is a response to Applicants' Amendment filed on March 07, 2007. In virtue of this amendment, claims 13-14 are added; and thus, claims 1- 14 are currently presented in the instant application.

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on March 19, 2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is considered by the examiner.

### *Claim Objections*

2. Claim 13 is objected to because of the following informalities:

Claim 13, line 3, - -pixel- - should be added before "pitch".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-2 and 4-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, the recitation "a combination being determined such that the sum of the widths of a plurality of lines formed in one line forming region is approximately the same as that of the sum of the widths of a plurality of lines formed in

another line forming region" in lines 9-11, renders the claim indefinite since it is not clear how a combination being determined.

Claims 2, 4, 11 and 12 are rejected for similar subject matter to claim 1.

Claims 5-10 and 13-14 are rejected since they are dependent on claims 2 and 1.

5. Claim 6 recites the limitation "the electric power lines" in 3. There is insufficient antecedent basis for this limitation in the claim.

Claims 7-8 are rejected since they are dependent on claim 6.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 4-5, 9-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Komiya et al. (US 2003/0076046 A1), hereinafter "Komiya".

Regarding claim 1, as best understood, Komiya discloses, in Figures 4-5 and page 5, par. [0067], an electro-optical device, comprising an electric power supply circuit (180); a plurality of pixels disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit (Fig. 5), the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction (Fig.

5), line forming regions (183, D) being formed between adjacent pixel groups of the plurality of pixel groups, and the line forming regions (183, D) being formed with generally the same width and inherently a combination being determined such that a sum of widths (183, D) of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region (183, D).

Regarding claim 2, as best understood, Komiya discloses, in Figures 4-5 and page 5, par. [0067], an electro-optical device comprising a plurality of scan lines (G); a plurality of data lines (D); a plurality of pixels (Fig. 5), disposed at portions corresponding to intersections of the scan lines (G) and the data lines (D), including electro-optical devices; and a plurality of electric power lines (183) to supply driving voltage to the electro-optical devices; the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction (Fig. 5), a plurality of line forming regions (183, D) being formed between adjacent pixel groups of said plurality of pixel groups, and at least two lines (183, D) selected from at least one electric power line of the plurality of electric power lines (183), at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines (D), being formed in at least one line forming region of the plurality of line forming regions; and inherently a combination being determined such that a sum of widths (183, D) of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region (183, D).

Claim 4 is rejected for similar subject matter to claim 2.

Regarding claim 5, as applied to claim 1, Komiya discloses, in page 5, par. [0067], the line forming regions being formed with generally the same width.

Regarding claim 9, as applied to claim 1, Komiya discloses, in Figures 4-5 and par. [0048], the electro-optical device being an electro-luminescence device (160).

Claim 10 is rejected for similar subject matter to claim 1.

Claim 11 is rejected for similar subject matter to claim 1.

Claim 12 is rejected for similar subject matter to claim 2.

Regarding claim 13, as applied to claim 1, Komiya discloses, in Figures 4-5, each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pixel pitch.

Regarding claim 14, Komiya discloses, in Figures 4-5, the combination of the plurality lines being disposed periodically and repeatedly in at least one direction of the row direction and the column direction.

8. Claim 3 is rejected under 35 U.S.C. 102(e) as being anticipated by Nara et al. (US 6,633,135 B2), hereinafter "Nara".

Regarding claim 3, Nara discloses, in Figure 1, an electro-optical device comprising a plurality of scan lines (VG); a plurality of data lines (VD); a plurality of pixels (11), disposed at portions corresponding to intersections of the scan lines (VG) and data lines (VD) including electro-optical devices; and a plurality of electrical power lines (VLC) to supply driving voltage to the electro-devices; the plurality of pixels (11) making up a plurality of pixel groups formed of a series of pixels arrayed in at least one

direction of the row direction and the column direction, a plurality of line forming regions (VG, VLC) being formed between adjacent pixel groups of the plurality of pixel groups, and both at least one electric power line (VLC) of the plurality of electric power lines and at least one scan line (VG) of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiya et al. (US 2003/0076046 A1) in view of Yamazaki et al. (US 6,825,820 B2), hereinafter "Komiya" and "Yamazaki".

Regarding claim 6, Komiya discloses every feature of claimed invention as expressly recited in claim 1, except for the electro-optical devices being operated with each different driving voltages; and the electric power lines to supply voltage to the electro-optical devices being formed with different widths corresponding to said driving voltage.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, the electro-optical devices being operated with each different driving voltages; and the electric power lines

to supply voltage to the electro-optical devices being formed with different widths corresponding to the driving voltage.

It would have been obvious to one having ordinary sill in the art at the time the invention was made to modify Komoya's display device by using the electric power lines with different widths to maintain a balance in the magnitudes of current flowing into the EL elements of each colors since using the electro-optical devices being operated with each different driving voltages and the electric power lines to supply voltage to the electro-optical devices being formed with different widths corresponding to the driving voltage for the stated purpose has been well known in the art, as evidenced by the teaching of Yamazaki (col. 3, lines 62-67).

Regarding claim 7, as applied to claim 6, Yamazaki discloses, in Figure 1B, the electro-optical device being a light-emission device and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

Regarding claim 8, as applied to claim 7, Figure 1B of Yamazaki discloses the color of the light which is to be emitted being at least one of red, green, and blue.

***Response to Arguments***

11. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new grounds of rejection.

***Inquiry***

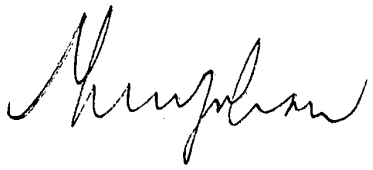
12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu Hien T. Duong whose telephone number is 571-

272-8980. The examiner can normally be reached on Monday - Friday, from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Owens can be reached on 571-272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit 2821
DD



THUY V. TRAN
PRIMARY EXAMINER

Sheet 1 of 1

| Form PTO-1449 (REV. 1/06) | US Dept. of Commerce PATENT & TRADEMARK OFFICE | ATTY DOCKET NO. 117390 | APPLICATION NO. 10/676,067 |
|---|---|---|---|
| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | | APPLICANTS Yojiro MATSUEDA et al. | |
| | | FILING DATE October 2, 2003 | GROUP 2821 |

OIPE MAR 19 2007 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Name |
|---|---|---|---|---|
| /DD/ | 1. | 6,825,820 B2 | 11/30/2004 | Yamazaki et al. |
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FOREIGN PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Country | With English Abstract | With English Translation |
|---|---|---|---|---|---|---|
| /DD/ | 2. | JP-A-2000-242196 | 09/08/2000 | Japan | X | X |
| /DD/ | 3. | JP-A-2001-272930 | 10/05/2001 | Japan | X | X |
| /DD/ | 4. | JP-A-2002-151276 | 05/24/2002 | Japan | — | — |
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OTHER DOCUMENTS

| Examiner Initials | Cite No. | (Including Author, Title, Date, Pertinent Pages, etc.) |
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| EXAMINER | /Dieu Duong/ | DATE CONSIDERED 05/03/2007 |
|---|---|---|

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: March 19, 2007

| Notice of References Cited | Application/Control No. 10/676,067 | Applicant(s)/Patent Under Reexamination MATSUEDA ET AL. | |
|---|---|---|---|
| | Examiner Dieu Hien T. Duong | Art Unit 2821 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| * | A | US-6,633,135 | 10-2003 | Nara et al. | 315/169.3 |
| * | B | US-2003/0076046 | 04-2003 | Komiya et al. | 315/169.3 |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
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| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
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**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | Examiner | Art Unit |
| | Duong, Dieu Hien T | 2821 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 05/04/2007 | | | | | | | | |
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| | 12 | ✓ | | | | | | | | |
| | 13 | ✓ | | | | | | | | |
| | 14 | ✓ | | | | | | | | |

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | **Examiner** | **Art Unit** |
| | Duong, Dieu Hien T | 2821 |

| SEARCHED | | | |
|---|---|---|---|
| **Class** | **Subclass** | **Date** | **Examiner** |
| 315 | 169.2,169.3 | 05/04/07 | dd |

| SEARCH NOTES | | |
|---|---|---|
| **Search Notes** | **Date** | **Examiner** |
| Please See East Search History | 05/04/07 | dd |

| INTERFERENCE SEARCH | | | |
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| **Class** | **Subclass** | **Date** | **Examiner** |
| | | | |

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AUG 16 2007
PATENT & TRADEMARK OFFICE

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al. Group Art Unit: 2821

Application No.: 10/676,067 Examiner: D. DUONG

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

**AMENDMENT UNDER 37 C.F.R. §1.111**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the May 16, 2007 Office Action, please consider the following:

**Amendments to the Claims** as reflected in the listing of claims; and

**Remarks**.

**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device, comprising:

an electric power supply circuit;

a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit, the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and the line forming regions being formed with generally the same width; ~~and~~

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices; and

~~a combination being determined such that~~ a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

2. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and at least two lines selected from at least one electric power line of the plurality of electric power lines, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and

~~a combination being determined such that~~ a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

3. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and both at least one electric power line of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions.

4. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and both at least one electric power line of the plurality of electric power lines and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions; and

~~a combination being determined such that~~ a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

5. (Previously Presented) The electro-optical device according to Claim 2, the line forming regions being formed with generally the same width.

6. (Canceled)

7. (Currently Amended) The electro-optical device according to ~~Claim 6~~Claim 1, the electro-optical device being a light-emission device;

and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

8. (Previously Presented) The electro-optical device according to Claim 7, the color of the light which is to be emitted being at least one of red, green, and blue.

9. (Previously Presented) The electro-optical device according to Claim 1, the electro-optical device being an electro-luminescence device.

10. (Previously Presented) An electronic apparatus, comprising:

the electro-optical device according to Claim 1.

11. (Currently Amended) A matrix substrate, comprising:

a plurality of pixel electrodes disposed in the form of a matrix, the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and the line forming regions being formed with generally the same width; ~~and~~

a ~~combination being determined such that~~plurality of electric power lines with different widths to supply voltage to the plurality of pixel electrodes; and

a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

12. (Currently Amended) A matrix substrate, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel electrodes disposed at portions corresponding to intersections of the scan lines and the data lines;

a plurality of electric power lines with different widths to supply voltage to the plurality of pixel electrodes;

the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and at least two lines selected from at least one electric power line of the plurality of electric power lines, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and

a ~~combination being determined such that the~~ sum of the widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of the sum of the widths of a plurality of lines formed in another line forming region.

13. (Currently Amended) The electro-optical device according to claim 1, each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pixel pitch.

14. (Previously Presented) The electro-optical device according to claim 1, the combination of the plurality of lines being disposed periodically and repeatedly in at least one direction of the row direction and the column direction.

## REMARKS

Claims 1-5 and 7-14 are pending in this application. By this Amendment, claims 1-4, 7, and 11-13 are amended. Amended claims 1-4, 11 and 12 now incorporate the subject matter of claim 6 and contain no new matter. Support for the amended claims can be found, for example, in Fig. 3 and in paragraphs [0030] and [0031] of Applicants' specification.

### I. Interview

The courtesies extended to Applicants' representative by Examiners Duong and Tran at the interview held July 19, 2007, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicants' record of the interview.

### II. Claim Objections

The Office Action objects to claim 13 for a formality. As claim 13 has been amended to recite "pixel pitch" in accordance with the Examiner's helpful suggestion, withdrawal of the objection is respectfully requested.

### III. Rejections under 35 U.S.C. §112

Claims 1, 2 and 4-14 were rejected under 35 U.S.C. §112, paragraph 2, as being indefinite. In accordance with the agreement reached during the July 19, 2007 interview, claims 1, 2, 4, 11 and 12 have been amended to delete the words "a combination being determined such that." Therefore, Applicants respectfully assert the claim language is now definite and request the rejection be withdrawn.

Claim 6 was objected to for having insufficient antecedent basis. As claim 6 is canceled, withdrawal of the rejection is respectfully requested.

## IV. Rejections under 35 U.S.C. §102

Claims 1, 2, 4, 5 and 9-14 are rejected under 35 U.S.C. §102(e) over U.S. Patent Publication No. 2003/0076046A1 to Komiya et al. (hereinafter "Komiya") and rejects claim 3 under 35 U.S.C. §102(e) over U.S. Patent No. 6,633,135 to Nara. These rejections are respectfully traversed.

As one or more of the features of claim 6 (which was not rejected under 35 U.S.C. §102) have been incorporated into claims 1, 2-4, 11, and 12, withdrawal of the rejection of claims 1, 2-4, 11 and 12 is respectfully requested. Further, withdrawal of the rejection of claims 5, 7-10, 13 and 14, which variously depend from claims 1, 2-4, 11 and 12, is respectfully requested at least based on their dependence on allowable base claims, as well as for additional features they recite. Withdrawal of the rejection is respectfully requested.

## V. Rejections under 35 U.S.C. §103

Claims 6-8 are rejected under 35 U.S.C. §103(a) over Komiya in view of U.S. Patent No. 6,825,820 B2 to Yamazaki et al. (hereinafter "Yamazaki"). This rejection is respectfully traversed.

The Examiner asserts that Yamazaki discloses using electric power lines of different widths to supply different driving voltages in Fig. 1B and at page 6, lines 5-15. This claimed feature has now been incorporated into claim 1. Thus, this rejection will be addressed in the context of claim 1.

Claim 1 recites, in part, "a sum of the widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of the widths of a plurality of lines formed in another line forming region." Claim 1 also recites, in part, "a plurality of electric power lines with different widths." While not addressed in the Office Action, during the July 19, 2007 interview, the Examiner asserted that Komiya discloses, at paragraph [0067], that the wiring of the power source lines 183, the

bypass lines 181 and the drain signal lines 152 could potentially all have the same width. Thus, according to the Examiner, when these lines have the same width, a sum of widths of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

However, this interpretation of Komiya would be inconsistent if applied to the Office Action's interpretation of Yamazaki. Specifically, according to the Office Action, Yamazaki discloses using power lines of different widths. Thus, if the widths of the power source, bypass and drain signal lines must be identical in Komiya to teach the claimed "sum of widths," Yamazaki cannot properly be combined with Komiya, as Yamazaki is relied upon to allegedly teach using power lines of different widths. To do so would change Komiya's principle of operation as applied to the rejected claims. Nomura fails to remedy the deficiencies of Yamazaki and Komiya. Therefore, the prior art does not disclose or suggest each and every limitation of claim 1 as amended, and claims 7-8 depending therefrom.

For at least these reasons, Applicants respectfully request the rejection of claims 1 and 7-8 be withdrawn.

## VI. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Moshe K. Wilensky
Registration No. 56,263

JAO:MKW/jfb

Date: August 16, 2007

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

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| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>10/676,067 | Filing Date<br>10/02/2003 | ☐ To be Mailed |
|---|---|---|---|

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = * | | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = * | | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| AMENDMENT 02/15/2007 | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE ($) | ADDITIONAL FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(i)) | * 14 | Minus | ** 20 | = 0 | X $ = | | OR | X $50= | 0 |
| Independent (37 CFR 1.16(h)) | * 6 | Minus | *** 6 | = 0 | X $ = | | OR | X $200= | 0 |
| ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

8-16-07

| AMENDMENT | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | OR | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(i)) | * 13 | Minus | ** 20 | = | X $ = | | OR | X $ = | |
| Independent (37 CFR 1.16(h)) | * 6 | Minus | *** 3 | = | X $ = | | OR | X $ = | |
| ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
Rosalind Ball

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/676,067 | 10/02/2003 | Yojiro Matsueda | 117390 | 7780 |

25944 7590 11/14/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

| EXAMINER | |
|---|---|
| DUONG, DIEU HIEN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2821 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 11/14/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

T/F

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | Dieu Hien T. Duong | 2821 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08/16/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5 and 7-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is a response to applicants' amendment field on August 16, 2007. In virtue of this amendment, claim 6 is cancelled; thus, claims 1-5 and 7-14 are currently in the instant application.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-5 and 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiya et al. (US 2003/0076046 A1) in view of Yamazaki et al. (US6, 825,820 B2), hereinafter "Komiya" and "Yamazaki".

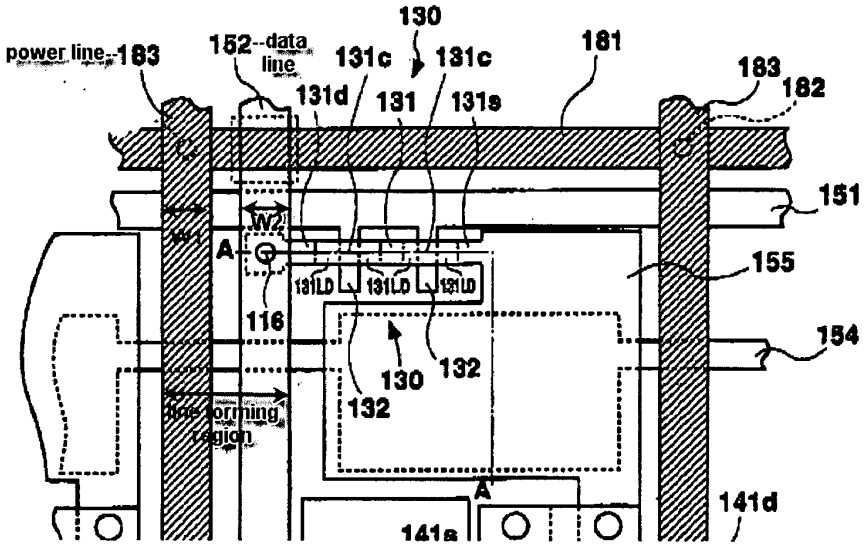
Regarding claim 1, Komiya discloses, in Figures 4-5 and page 5, par. [0067], liens 7-9, an electro-optical device, comprising an electric power supply circuit (180); a plurality of pixels disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit (Fig. 5), the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction (Fig. 5), line forming regions (183, D) being formed between adjacent pixel groups of the plurality of pixel groups, and the line forming regions (183, D) being formed with generally the same width; a sum of widths (183, D) of a plurality of lines formed in one

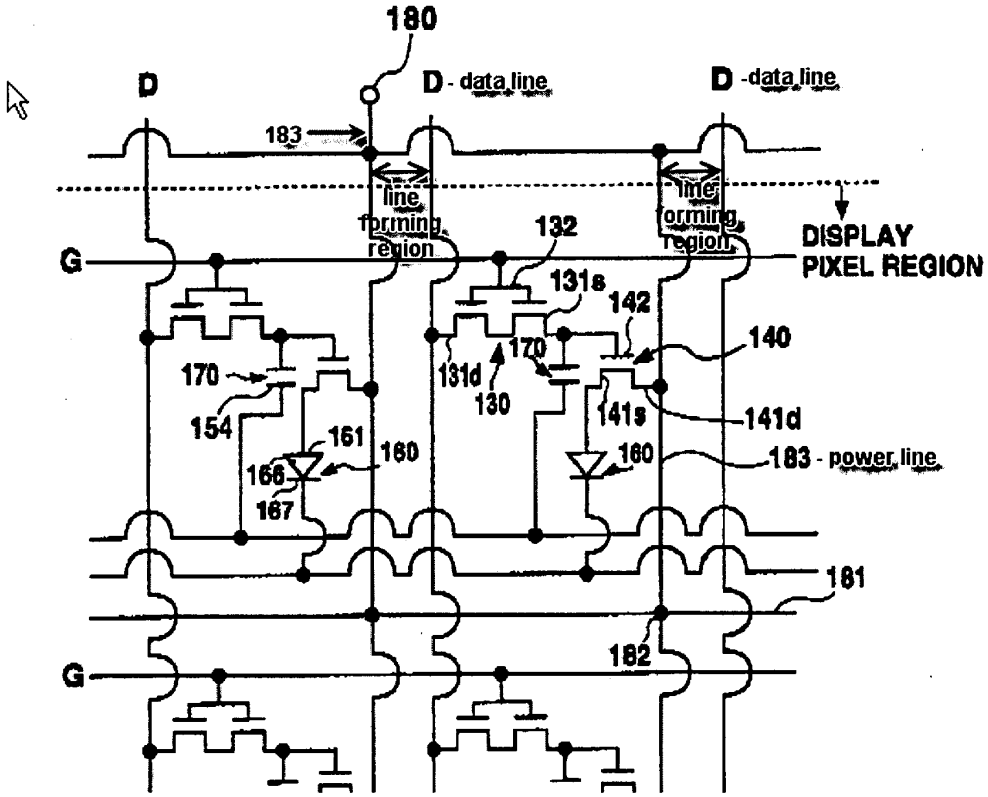
line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region (183, D); a plurality of electric power lines (183) to supply driving voltage to the electro-optical devices.

Komiya does not disclose electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Komiya to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).






Regarding claim 2, Komiya discloses, in Figures 4-5 and page 5, par. [0067], an electro-optical device comprising a plurality of scan lines (G); a plurality of data lines (D); a plurality of pixels (Fig. 5), disposed at portions corresponding to intersections of the scan lines (G) and the data lines (D), including electro-optical devices; and a plurality of electric power lines (183) to supply driving voltage to the electro-optical devices; the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction (Fig. 5), a plurality of line forming regions (183, D) being formed between adjacent pixel groups of said plurality of pixel groups, and at least two lines (183, D) selected from at

least one electric power line of the plurality of electric power lines (183), at least one scan line of the plurality of scan lines, and at least one data line (D) of the plurality of data lines (D), being formed in at least one line forming region of the plurality of line forming regions; and a sum of widths (183, D) of a plurality of lines including at least one electric power line (183) formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region (183, D).

Komiya does not disclose electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Komiya to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).

Claim 4 is rejected for similar subject matter to claim 2.

Regarding claim 5, as applied to claim 1, Komiya/Yamazaki disclose, the line forming regions being formed with generally the same width (see Komiya, lines 7-9 of par. [0076]).

Regarding claim 7, as applied to claim 6, Komiya/Yamazaki disclose, the electro-optical device being a light-emission device and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device (see Yamazaki, Figure 1B).

Regarding claim 8, as applied to claim 7, Komiya/ Yamazaki disclose, the color of the light which is to be emitted being at least one of red, green, and blue (see Figure 1B of Yamazaki).

Regarding claim 9, as applied to claim 1, Komiya/Yamazaki disclose, in Figures 4-5 and par. [0048], the electro-optical device being an electro-luminescence device (160, see Komiya, Figures 4-5 and par. [0048]).

Claim 10 is rejected for similar subject matter to claim 1.

Claim 11 is rejected for similar subject matter to claim 1.

Claim 12 is rejected for similar subject matter to claim 2.

Regarding claim 13, as applied to claim 1, Komiya/Yamazaki disclose, each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pixel pitch (see Komiya, Figures 4-5).

Regarding claim 14, Komiya/Yamazaki disclose, the combination of the plurality lines being disposed periodically and repeatedly in at least one direction of the row direction and the column direction (see Komiya, Figures 4-5).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nara et al. (US 6,633,135 B2) in view of Yamazaki et al. (US 6,825,820 B2), hereinafter "Nara" and "Yamazaki".

Regarding claim 3, Nara discloses, in Figure 1, an electro-optical device comprising a plurality of scan lines (VG); a plurality of data lines (VD); a plurality of pixels (11), disposed at portions corresponding to intersections of the scan lines (VG) and data lines (VD) including electro-optical devices; and a plurality of electrical power

lines (VLC) to supply driving voltage to the electro-devices; the plurality of pixels (11) making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions (VG, VLC) being formed between adjacent pixel groups of the plurality of pixel groups, and both at least one electric power line (VLC) of the plurality of electric power lines and at least one scan line (VG) of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions.

Nara does not disclose the electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Komiya to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).

***Response to Arguments***

4. Applicant's arguments filed August 16, 2007 have been fully considered but they are not persuasive.

Applicant argues that:

i. "a sum of the widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of the widths of a plurality of lines formed in another

line forming region" is not addressed in Office Action mailed May 16, 2007.

ii. Yamazaki cannot properly be combined with Komiya because of doing so would change Komiya's principle of operation as applied to the rejected claims.

Examiner respectfully disagrees.

In response to the first argument, in Office Action mailed May 16, 2007, Komiya discloses, in Figures 4-5, a sum of the widths of a plurality of lines (183, D) including at least one electric power line (183) formed in one line forming region is approximately the same as that of a sum of the widths of a plurality of lines (183, D) formed in another line forming region. Each line forming region includes the power line 183 and data line D in Figure 5 (or data line 152 in Figure 4). Therefore, sum (183 + D) or of the widths of a plurality of lines (183, D) including at least one electric power line (183) formed in one line forming region is approximately the same as that of a sum (183 +D) of the widths of a plurality of lines (183, D) formed in another line forming region.

In response to the second argument, Komiya discloses the line width of power line 183 can be as large as the width of the signal line 152, or even larger (see lines 7-9 of par. [0067]). In other words, the width of the power line 183 can be changed to prevent lack of display luminance. Therefore, It is proper to combine Komiya with Yamaki to provide the electric power lines with different widths wherein the sum of the widths of a plurality of lines in one line forming

widths wherein the sum of the widths of a plurality of lines in one line forming region is approximately the same as that of a sum of the widths of a plurality of lines formed in another line forming region to improve the brightness uniformity of the display device.

***Inquiry***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu Hien T. Duong whose telephone number is 571-272-8980. The examiner can normally be reached on Monday - Friday, from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Owens can be reached on 571-272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DD
Art Unit 2821

TRINH DINH
PRIMARY EXAMINER

| Interview Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | Dieu Hien T. Duong | 2821 | |

All participants (applicant, applicant's representative, PTO personnel):

(1) *Dieu Hien T. Duong*. (3) *John A Radi*.

(2) *Thuy V. Tran*. (4)_____.

Date of Interview: *19 July 2007*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☐ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-14*.

Identification of prior art discussed: *US 2003/0076046 A1, US 6,633,135 B2*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *we discussed the references cited in office action mailed on 05/16/2007*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

## Summary of Record of Interview Requirements

**Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record**
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

**Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews**
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

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The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

**Examiner to Check for Accuracy**

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | Examiner | Art Unit |
| | Duong, Dieu Hien T | 2821 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 11/05/2007 | | | | | | | | |
| | 1 | ✓ | | | | | | | | |
| | 2 | ✓ | | | | | | | | |
| | 3 | ✓ | | | | | | | | |
| | 4 | ✓ | | | | | | | | |
| | 5 | ✓ | | | | | | | | |
| | 6 | - | | | | | | | | |
| | 7 | ✓ | | | | | | | | |
| | 8 | ✓ | | | | | | | | |
| | 9 | ✓ | | | | | | | | |
| | 10 | ✓ | | | | | | | | |
| | 11 | ✓ | | | | | | | | |
| | 12 | ✓ | | | | | | | | |
| | 13 | ✓ | | | | | | | | |
| | 14 | ✓ | | | | | | | | |

FEB 11 2008
PATENT & TRADEMARK OFFICE

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al.

Group Art Unit: 2821

Application No.: 10/676,067

Examiner: D. DUONG

Filed: October 2, 2003

Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

**MAIL STOP RCE**

**LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.114, Applicant(s) hereby request(s) continued examination.

☒ Applicants further request entry and consideration of the attached submission.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

Attached hereto is our check no. 202280 in the amount of ☒ $810.00 as payment of the fees set forth in 37 C.F.R. §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Moshe K. Wilensky
Registration No. 56,263

JAO:MKW/jnm

Date: February 11, 2008

**OLIFF & BERRIDGE, PLC**
**P.O. Box 320850**
**Alexandria, Virginia 22320-4850**
**Telephone: (703) 836-6400**

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

02/12/2008 DEMMANU1 00000187 10676067
01 FC:1801 810.00 OP




**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al. Group Art Unit: 2821

Application No.: 10/676,067 Examiner: D. DUONG

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

**AMENDMENT WITH RCE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the November 14, 2008 Office Action, and in view of the attached Request for Continued Examination (RCE), please consider the following:

**Amendments to the Claims** as reflected in the listing of claims; and

**Remarks**.

**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device, comprising:

an electric power supply circuit;

a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit, the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and each of the line forming regions being formed with generally the same width;

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices; and

at least two electric power lines of the plurality of electric power lines with different widths being formed in at least one line forming region of the plurality of line forming regions.

~~a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region~~.

2. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and ~~at least two lines selected from at least one electric power line of the plurality of electric power lines~~ at least two electric power lines of the plurality of electric power lines with different widths, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and

a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

3. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and both at least ~~one~~ two electric power ~~line~~ lines of the plurality of electric

power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions.

4. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and both at least ~~one~~ two electric power ~~line~~ lines of the plurality of electric power lines and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions; and

a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

5. (Previously Presented) The electro-optical device according to Claim 2, the line forming regions being formed with generally the same width.

6. (Canceled)

7. (Previously Presented) The electro-optical device according to Claim 1, the electro-optical device being a light-emission device;

and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

8. (Previously Presented) The electro-optical device according to Claim 7, the color of the light which is to be emitted being at least one of red, green, and blue.

9. (Previously Presented) The electro-optical device according to Claim 1, the electro-optical device being an electro-luminescence device.

10. (Previously Presented) An electronic apparatus, comprising:

the electro-optical device according to Claim 1.

11. (Currently Amended) A matrix substrate, comprising:

a plurality of pixel electrodes disposed in the form of a matrix, the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and the line forming regions being formed with generally the same width;

a plurality of electric power lines with different widths to supply voltage to the plurality of pixel electrodes; and

at least two electric power lines of the plurality of electric power lines with different widths being formed in at least one line forming region of the plurality of line forming regions.~~a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.~~

12. (Currently Amended) A matrix substrate, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel electrodes disposed at portions corresponding to intersections of the scan lines and the data lines;

a plurality of electric power lines with different widths to supply voltage to the plurality of pixel electrodes;

the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and at least two lines selected from at least ~~one~~ two electric power ~~line~~ lines of the plurality of electric power lines, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and

a sum of the widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of the sum of the widths of a plurality of lines formed in another line forming region.

13. (Previously Presented) The electro-optical device according to claim 1, each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pixel pitch.

14. (Previously Presented) The electro-optical device according to claim 1, the combination of the plurality of lines being disposed periodically and repeatedly in at least one direction of the row direction and the column direction.

15. (New) The electro-optical device according to claim 1, wherein a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

16. (New) The electro-optical device according to claim 11, wherein a sum of widths of a plurality of lines including at least one electric power line formed in one line

forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

## REMARKS

Claims 1-5 and 7-15 are pending in this application. By this Amendment, claims 1-4, 11 and 12 are amended and claims 15 and 16 are added. Support for the amended claims can be found, for example, in Fig. 3 and paragraphs [0030] and [0031] of the specification.

Claims 1, 2, 4, 5 and 7-14 are rejected under 35 U.S.C. §103(a) over U.S. Patent Publication No. 2003/0076046A1 to Komiya et al. (hereinafter "Komiya") in view of U.S. Patent No. 6,825,820 B2 to Yamazaki et al. (hereinafter "Yamazaki"). Claim 3 is rejected under 35 U.S.C. §103(a) over U.S. Patent No. 6,633,135 to Nara in view of Yamazaki. These rejections are respectfully traversed.

Claims 1-4, 11 and 12, as amended, now recite that "at least two electric power lines selected from the plurality of electric power lines with different widths" are formed in at least one line forming region of the plurality of line forming regions (emphasis added). Neither Komiya, Yamazaki or Nara individually, or in combination, disclose or suggest this feature.

Furthermore, it is improper for the Office Action to combine Komiya and Yamazaki to disclose the features that "the plurality of electric power lines [have] different widths" and/or that the "sum of the widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region." These features are recited in claims 1 2, 4, 11 and 12.

A. Komiya and Yamazaki do not Disclose the Plurality of Electric Power Lines have Different Widths.

The Office Action asserts Komiya discloses several of the features of claims 1, 2, 4, 11 and 12. However, the Office Action concedes that Komiya does not disclose that the "plurality of electric power lines [have] different widths" as recited in claims 1 2, 4, 11 and 12. The Office Action cures this deficiency by combining Komiya with Yamazaki.

The Office Action asserts that Komiya discloses that the width of the power source line 183 can be changed to prevent lack of display luminance (see [0067]). The Office Action also asserts that Fig. 1B of Yamazaki discloses that the widths of the detour wiring lines (allegedly equivalent to the recited electric power lines) varies based on color. The Office Action appears to be asserting that the detour lines of Yamazaki are equivalent to the data lines 152 in Komiya (for combination purposes). The Office Action cites to paragraph [0067] of Komiya which allegedly discloses that the power line 183 can vary in width. Thus, the Office Action appears to be asserting that when the smaller width detour line from Yamazaki would be combined into the circuit disclosed by Komiya, the power source line would widened accordingly. Therefore, the Office Action asserts that it is proper to combine Komiya with Yamazaki.

However, Yamazaki discloses that the widths of the three detour wiring lines (R, G and B) should satisfy the formula $Wr:Wg:W_b = I_r:I_g:I_b$. See col. 6 lines 7-29. As discussed above the Office Action appears to be asserting the detour lines of Yamazaki correspond to the data lines 152 in Komiya (for combination purposes). Column 6 lines 38-43 of Yamazaki discloses that the power source feed lines, which the Office Action appears to assert are analogous to the power lines 183 of Komiya, should also vary *according to the same formula*. In other words, Yamazaki anticipates that as the detour line widens, the corresponding power source feed line would also widen. As such, it is improper to combine Yamazaki and Komiya to achieve the opposite effect, as asserted by the Office Action.

B. Komiya and Yamazaki do not Disclose that the Sum of the Widths of a Plurality of Lines are the same in Multiple Line Regions.

Regarding claims 2, 4 and 12, the Office Action asserts that Komiya discloses that the width of the power source line 183 and the drain signal line 152 (i.e. the sum of 183 + D) is the same in each line forming region. However, paragraph [0067] of Komiya discloses that

the width of the entire length of every power source line may be altered in the design phase, so as to maximize display luminance. Komiya does not disclose selectively widening some power source lines, but not others. As such, Komiya does not disclose varying the power source line in such a manner as to insure that the sum of the widths of the lines in different line forming regions is the same, as recited in claims 2, 4, and 12.

Accordingly, for at least the reasons presented above, withdrawal of the rejection of claims 1-4, 11, 12, and claims 5, 7-10, 13 and 14 depending therefrom, is respectfully requested. Claims 15 and 16 are also in condition for allowance for their respective dependence on allowable base claims 1 and 11, as well as for the separately patentable subject matter they recite.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Moshe K. Wilensky
Registration No. 56,263

JAO:MKW/jnm

Attachment:
Request for Continued Examination

Date: February 11, 2008

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| **PATENT APPLICATION FEE DETERMINATION RECORD**<br>Substitute for Form PTO-875 | Application or Docket Number<br>10/676,067 | Filing Date<br>10/02/2003 | ☐ To be Mailed |
|---|---|---|---|

**APPLICATION AS FILED – PART I**

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

**APPLICATION AS AMENDED – PART II**

| | | (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **02/11/2008** | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| AMENDMENT | Total (37 CFR 1.16(i)) | * 15 | Minus | ** 20 | = 0 | X $ = | | OR | X $50= | 0 |
| | Independent (37 CFR 1.16(h)) | * 6 | Minus | ***6 | = 0 | X $ = | | OR | X $210= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | **0** |

| | | (Column 1) | | (Column 2) | (Column 3) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| AMENDMENT | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Anita J. Johnson/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/676,067 | 10/02/2003 | Yojiro Matsueda | 117390 | 7780 |

25944 7590 03/19/2008

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

| EXAMINER | |
|---|---|
| DUONG, DIEU HIEN | |
| ART UNIT | PAPER NUMBER |
| 2821 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 03/19/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | DIEU HIEN T. DUONG | 2821 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5 and 7-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/11/2008 has been entered.

In virtue of this request, claim 6 is canceled; claims 15-16 are newly added; thus, claims 1-5 and 7-16 are currently in the instant application.

### *Drawings*

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a plurality of electric power lines with different width", "at least two electric power lines of the plurality of electric power lines, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions", "both at least two electric power lines of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions", and "both at least two electric power lines of the plurality of electric power lines and at least one data line of the plurality of data lines being formed in at least one line forming

region of the plurality of line forming regions" must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 2-5 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claim 2 has been amended to recite the feature “at least two electric power lines of the plurality of electric power lines, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions” which does not appear to be in the original filed specification. Thus, the recitation must be treated as "new matter".

Claim 3 has been added to recite the feature “both at least two electric power lines of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions” which does not appear to be in the originally filed specification. Thus, the recitation must be treated as "new matter".

Claim 4 has been added to recite the feature “both at least two electric power lines of the plurality of electric power lines and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions” which does not appear to be in the originally filed specification. Thus, the recitation must be treated as "new matter".

For “new matters” in claims 2, 3 and 4, if applicant does not believe, an appropriate explanation is required to point out where the supports for these subject matters can be found in the original specification.

Claim 5 is rejected since it is dependent on claim 2.

Claim 12 is rejected for similar subject matter to claim 2.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 14:

Lines 1-2, the recitation "the combination of the plurality of lines" is not clear. It is not clear what "the plurality of lines" refers to. Does it refer to "the plurality of electric power lines? If so, it should be "the combination of the plurality of said electric power lines.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 7-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanada (US 2001/0048106 A1) in view of Yamazaki et al. (US 6,825,820 B2 of record), hereinafter "Yamazaki".

Regarding claim 1, Tanada discloses, in Figures 5 and 6A, an electro-optical device, comprising an electric power supply circuit; a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from

the electric power supply circuit, the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and each of the line forming regions being formed with generally the same width; a plurality of electric power lines (640, 650) to supply driving voltage to the electro-optical devices; and at least two electric power lines (640, 650) of the plurality of electric power lines being formed in at least one line forming region of the plurality of line forming regions.

Tanada does not disclose the electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Tanada to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).

Regarding claim 7, as applied to claim 1, Tanada/Yamazaki disclose, (see Tanada, Figures 5 and 6A), the electro-optical device being a light-emission device and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

Regarding claim 8, as applied to claim 7, Tanada/ Yamazaki disclose, (see Tanada, Figures 5 and 6A), the color of the light which is to be emitted being at least one of red, green, and blue.

Regarding claim 9, as applied to claim 1, Tanada/Yamazaki disclose, (Tanada, Figures 5 and 6A), the electro-optical device being an electro-luminescence device.

Regarding claim 10, Tanada/Yamazaki disclose, (Tanada, Figure 23), a electronic apparatus comprising the electro-optical device according to claim 1.

Claim 11 is rejected for similar subject matter to claim 1.

Regarding claim 13, as applied to claim 1, Tanada/Yamazaki disclose, (see Tanada, Figures 5 and 6A), each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pixel pitch.

Regarding claim 14, Tanada/Yamazaki disclose, (see Tanada, Figures 5 and 6A), the combination of the plurality lines being disposed periodically and repeatedly in at least one direction of the row direction and the column direction.

Regarding claim 15, as applied to claim 1, Tanada/Yamazaki disclose, (Tanada, Figures 2B, 5 and 6A), wherein a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that the sum of widths of a plurality of lines formed in another line forming region.

Claim 16 is rejected for similar subject matter to claim 15.

9. Claims 2, 4-5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiya et al. (US 2003/0076046 A1 of record) in view of Yamazaki et al. (US 6, 825,820 B2 of record), hereinafter “Komiya” and “Yamazaki”.

Regarding claim 2, Komiya discloses, in Figures 4-5 and page 5, par. [0067], an electro-optical device comprising a plurality of scan lines (G); a plurality of data lines

(D); a plurality of pixels (Fig. 5), disposed at portions corresponding to intersections of the scan lines (G) and the data lines (D), including electro-optical devices; and a plurality of electric power lines (183) to supply driving voltage to the electro-optical devices; the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction (Fig. 5), a plurality of line forming regions (183, D) being formed between adjacent pixel groups of said plurality of pixel groups, and at least two lines (183, D) selected from at least one electric power line of the plurality of electric power lines (183), at least one scan line of the plurality of scan lines, and at least one data line (D) of the plurality of data lines (D), being formed in at least one line forming region of the plurality of line forming regions; and a sum of widths (183, D) of a plurality of lines including at least one electric power line (183) formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region (183, D).

Komiya does not disclose electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Komiya to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).

Claim 4 is rejected for similar subject matter to claim 2.

Regarding claim 5, as applied to claim 1, Komiya/Yamazaki disclose, the line forming regions being formed with generally the same width (see Komiya, lines 7-9 of par. [0076]).

Claim 12 is rejected for similar subject matter to claim 2.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nara et al. (US 6,633,135 B2 of record) in view of Yamazaki et al. (US 6,825,820 B2 of record), hereinafter “Nara” and “Yamazaki”.

Regarding claim 3, Nara discloses, in Figure 1, an electro-optical device comprising a plurality of scan lines (VG); a plurality of data lines (VD); a plurality of pixels (11), disposed at portions corresponding to intersections of the scan lines (VG) and data lines (VD) including electro-optical devices; and a plurality of electrical power lines (VLC) to supply driving voltage to the electro-devices; the plurality of pixels (11) making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions (VG, VLC) being formed between adjacent pixel groups of the plurality of pixel groups, and both at least one electric power line (VLC) of the plurality of electric power lines and at least one scan line (VG) of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions.

Nara does not disclose the electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Komiya to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).

***Response to Arguments***

11. Applicant's arguments with respect to claims 1, 7-11 and 13-16 filed on 02/11/2008 have been considered.

Applicant argued that:

The support for the amended claims and the newly added claims 1-5 and 7-15 can be found, for example in Fig. 3, paragraphs [0030] and [0031] of the specification.

Examiner respectfully disagrees.

The only support for the newly added limitations of the claims 1, 7-11 and 13-16 can be found (for example, at least two electric power lines selected from the plurality of electric power lines with different widths are formed in at least one line forming region). Therefore, applicant's arguments with respect to claims 1, 7-11 and 13-16 are moot in view of the new ground(s) of rejection.

No support can be found for the newly added limitations of the claims 2-5 and 12. Therefore, these limitations are treated as new subject matter and have been rejected under 35 USC 112, first paragraph as discussed above.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIEU HIEN T. DUONG whose telephone number is (571)272-8980. The examiner can normally be reached on Monday - Friday, from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Owens can be reached on 571-272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

02/21/08
DD

/Trinh Vo Dinh/
Primary Examiner, Art Unit 2821
March 14, 2008

| Notice of References Cited | Application/Control No. 10/676,067 | Applicant(s)/Patent Under Reexamination MATSUEDA ET AL. | |
|---|---|---|---|
| | Examiner DIEU HIEN T. DUONG | Art Unit 2821 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| * | A | US-2001/0048106 | 12-2001 | Tanada, Yoshifumi | 257/66 |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
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| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 1153 | (electro adj1 optical) and ((power voltage current) near2 line$1) and ((data signal) near1 line$1) and @ad<"20021007" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/21 09:47 |
| L2 | 461 | 1 and (red blue green) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/21 09:49 |
| L12 | 692 | l1 not l2 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/21 17:35 |

2/21/2008 5:35:57 PM

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | Examiner | Art Unit |
| | Duong, Dieu Hien T | 2821 |

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|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 03/12/2008 | | | | | | | | |
| | 1 | ✓ | | | | | | | | |
| | 2 | ✓ | | | | | | | | |
| | 3 | ✓ | | | | | | | | |
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| | 5 | ✓ | | | | | | | | |
| | 6 | - | | | | | | | | |
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| | 10 | ✓ | | | | | | | | |
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| | 14 | ✓ | | | | | | | | |
| | 15 | ✓ | | | | | | | | |
| | 16 | ✓ | | | | | | | | |

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | Examiner | Art Unit |
| | Duong, Dieu Hien T | 2821 |

| SEARCHED | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| 315 | 169.2,169.3 | 3/12/2008 | dd |

| SEARCH NOTES | | |
|---|---|---|
| Search Notes | Date | Examiner |
| Please See East Search History | 3/12/2008 | dd |
| Consulted with Thuy Tran, primary 315 | 3/12/2008 | dd |

| INTERFERENCE SEARCH | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| | | | |

OIPE JAP97
MAY 01 2008
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al. Group Art Unit: 2821

Application No.: 10/676,067 Examiner: DUONG

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

## INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☒ 2. Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application, and this communication was not received by any individual designated in §1.56(c) more than thirty days prior to the filing of this Information Disclosure Statement.

☒ 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

☒ 4. An English language Abstract of one or more non-English language reference is attached. See References 5 and 6.

☒ 5. A computer-generated English language translation of one or more Japanese Patent Publication cited herein has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See References 5 and 6.

☒ 6. References 1 and 2 correspond to reference 5.

☒ 7. References 3 and 4 correspond to reference 6.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Moshe K. Wilensky
Registration No. 56,263

JAO:MKW/jfb

Date: May 1, 2008

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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

PTO/SB/97
MAY 01 2008
PATENT & TRADEMARK OFFICE



| Form PTO-1449 (REV. 1/06) | US Dept. of Commerce PATENT & TRADEMARK OFFICE | ATTY DOCKET NO. 117390 | APPLICATION NO. 10/676,067 |
|---|---|---|---|
| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | | APPLICANT(S) Yojiro MATSUEDA et al. | |
| | | FILING DATE October 2, 2003 | GROUP 2821 |

U.S. PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Name |
|---|---|---|---|---|
| | 1 | 6,724,149 | 04/20/2004 | KOMIYA et al. |
| | 2 | 7,009,345 | 03/07/2006 | KOMIYA et al. |
| | 3 | 6,965,363 | 11/15/2005 | SATO et al. |
| | 4 | 2006/0055643 | 03/16/2006 | SATO et al. |
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| Examiner Initials | Cite No. | Document Number | Date | Country | With English Abstract | With English Translation |
|---|---|---|---|---|---|---|
| | 5 | JP-A-2001-100654 | 04/13/2001 | JAPAN | X | X |
| | 6 | JP-A-2002-287663 | 10/04/2002 | JAPAN | X | X |
| | | | | | | |
| | | | | | | |
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OTHER DOCUMENTS

| Examiner Initials | Cite No. | (Including Author, Title, Date, Pertinent Pages, etc.) |
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| EXAMINER | DATE CONSIDERED |
|---|---|

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: May 1, 2008

5

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-100654

(43)Date of publication of application : 13.04.2001

(51)Int.Cl. G09F 9/30
H05B 33/14

(21)Application number : 11-277084

(22)Date of filing : 29.09.1999

(71)Applicant : SANYO ELECTRIC CO LTD

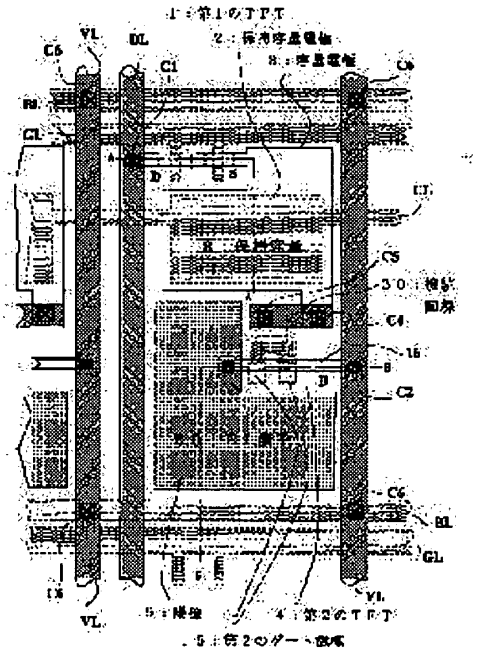
(72)Inventor : NISHIKAWA RYUJI

## (54) EL DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an EL display device with which bright display may be obtained by suppressing the lowering of power source current by the resistance of drive lines VL occurring in the distances from drive power source input terminals and supplying the current to be intrinsically supplied to EL elements.

SOLUTION: In the respective drive lines VL for supplying the drive current from the drive power source to the organic EL elements 20 formed in display pixel regions having display pixels, the respective drive lines VL arranged at the respective display pixels adjacent to each other are connected to bypass lines BL within the display pixel regions, by which the lowering of the power source current by the resistance of the drive lines VL is suppressed. The bypass lines are formed in the layers lower than the layers where the drive lines VL are formed, by which the superposition on anodes 6 is made possible.



* NOTICES *

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## CLAIMS

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[Claim(s)]
[Claim 1]A display pixel characterized by comprising the following is an EL display arranged to matrix form, An EL display having the bypass line which extended in the direction which intersects said drive line, and was electrically connected with said drive line, and was provided in a lower layer rather than said drive line.
An EL element which has a luminous layer between the anode and the negative pole.
A thin film transistor by which a drain of an active layer which consists of semiconductor membrane was electrically connected to a drive line of said EL element, and sauce of said active layer was electrically connected to said EL element.

[Claim 2]A display pixel characterized by comprising the following is an EL display arranged to matrix form, An EL display having the bypass line which extended in the direction which intersects said drive line, and was electrically connected with said drive line, and was provided in a lower layer rather than said drive line.
An EL element which has a luminous layer between the anode and the negative pole.
The 1st thin film transistor by which a drain of an active layer which comprises semiconductor membrane was connected to a drain line, and a gate was connected to a gate line, respectively.
The 2nd thin film transistor by which a drain of an active layer which consists of said semiconductor membrane was connected to a drive line of said EL element, a gate was electrically connected to sauce of said 1st thin film transistor, and sauce was connected to said EL element.

[Claim 3]The EL display according to claim 1 or 2 in which said bypass line is formed between a layer in which said gate was formed, a layer in which said semiconductor membrane was

formed, or a layer of an insulating layer located between said semiconductor membrane and said drive line.

[Claim 4]The EL display according to claim 3 in which at least a part superimposes said bypass line on said anode.

[Claim 5]Claim 1 by which said bypass line is formed for said every display pixel, and contact is formed in a superposed part with said drive line for said every display pixel, claim 2, the EL display according to claim 3 or 4.

[Claim 6]Claim 1 which said thin film transistor becomes from top gate mold structure, claim 2, claim 3, the EL display according to claim 4 or 5.

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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the electroluminescence display provided with the electroluminescent element and the thin film transistor.
[0002]
[Description of the Prior Art]Recent years, electroluminescence (below Electro Luminescence:.) "EL" is called. The EL display using an element attracts attention as a display which replaces CRT and LCD, For example, research and development of the EL display provided with the thin film transistor (below Thin Film Transistor: calls "TFT".) as a switching element which makes the EL element drive are also furthered.
[0003]The display pixel of an organic electroluminescence display is shown in drawing 7, and the representative circuit schematic of an organic electroluminescence display is shown in drawing 8. The sectional view which met the A-A line of drawing 7 is shown in drawing 9, and the sectional view which met the B-B line of drawing 7 is shown in drawing 10.
[0004]The display pixel is formed in the field surrounded by the gate line GL and drain line DL as shown in a figure. It has TFTof ** 1st which is switching element1 near the intersection of both signal wires, and the sauce of the TFT1 is connected to the gate 5 of 2nd TFT4 that drives an organic EL device while it serves as the retention volume electrode 2 and the capacity electrode 3 which constitutes capacity. The sauce of 2nd TFT4 is connected to the anode 6 of an organic EL device, and the drain of another side is connected to drive line VL which drives an organic EL device.
[0005]Said retention volume electrode 2 comprises chromium etc., is superimposed on the 1st sauce of TFT1, and the capacity electrode 3 of one via the upper gate dielectric film 7, and is accumulating the electric charge by using said gate dielectric film 7 as a dielectric layer. This retention volume 8 holds the voltage impressed to the gate 5 of 2nd TFT4.

[0006]Then, it explains, referring to drawing 7 and drawing 9 for the 1st TFT1 for switching.
[0007]The 1st gate electrode 11 that consists of refractory metals, such as chromium (Cr) and molybdenum (Mo), is formed on the transparent insulating substrate 10 which consists of silica glass, alkali free glass, etc. first. This 1st gate electrode 11 has extended [ two or more ] right and left in the gate line GL and one like drawing 7. On the right of the 1st gate electrode 11 of drawing 9, the retention volume electrode 2 made from the same process as the 1st gate electrode 11 is formed. Since this retention volume electrode 2 constitutes capacity like drawing 7, it has the expanded portion between TFTof ** 1st1, and the 2nd TFT4, and these comprise retention volume line CL and one which extended right and left.
[0008]Then, the 1st active layer 12 that consists of a polycrystalline silicon (p-Si is called.) film via the gate dielectric film 7 is formed. As for this active layer 12, LDD (Lightly Doped Drain) structure is adopted. That is, a low concentration area is established in the both sides of a gate, and also outside, the high-concentration source region and drain area are provided. The stopper insulator layer 13 is formed on said active layer 12. This stopper insulator layer 13 is an ion-implantation blocking film to the active layer 12.
Here, a Si oxide film is comprised.

[0009]And on the gate dielectric film 7, the active layer 12, and the stopper insulator layer 13. For example, drain line DL which changes is electrically connected with the drain electrode via the contact hole C1 which the interlayer insulation film 14 in which the $SiO_2$ film, the SiN film, and the $SiO_2$ film were laminated in order was formed, and was established in the drain. In order to make surface unevenness flat, the flattening film PLN which comprises organic resin, for example is formed in the whole surface. Since an EL display is a current drive, it must be thickness with a uniform EL layer. It is because current concentration occurs in a portion with thin thickness. Therefore, at least, since surface smoothness with this remarkable formation area is required, said flattening film PLN is adopted.
[0010]Next, the 2nd TFT4 that drives an organic EL device is explained with reference to drawing 10.
[0011]On the insulating substrate 10 mentioned above, the 2nd gate electrode 15 of said 1st gate 11 and an identical material is formed.
The 2nd active layer 16 is formed via the gate dielectric film 7.
On the active layer, the stopper insulator layer 17 is formed like the above-mentioned.
[0012]In said active layer 16, the source region and the drain area of a p type impurity are established in the gate electrode 15 upper part at the both sides of the channel which is genuineness genuineness or substantially, and this channel, and the p type channel TFT is constituted.
[0013]And the interlayer insulation film 14 mentioned above is formed in the whole surface.

And drive line VL is electrically connected via the contact hole C2. The flattening film PLN mentioned above is formed in the whole surface, and sauce is exposed to it by the contact hole C3. And the transparent electrode (anode of an organic EL device) 6 which comprises ITO (Indium Thin Oxide) via this contact hole is formed.

[0014]The organic EL device 20, Said anode 6, MTDATA. (4-bis) [ 4, ] (3-methylphenylphenylamino) The 1st hole transporting bed 21 which comprises biphenyl, And the 2nd hole transporting bed 22 which consists of TPD(s) (4, 4, and 4-tris(3-methylphenylphenylamino) triphenylanine), Bebq2 containing the Quinacridone (Quinacridone) derivative (10-BENZO) [h]In this turn, light emitting element layer EM which consists of the electron transport layer 24 which comprises the luminous layer 23 which comprises a quinolinol beryllium complex, and Bebq2, and the negative pole 25 which comprises a magnesium indium alloy are the structures by which laminating formation was carried out, and is provided all over the parenchyma of an organic EL device.

[0015]The hole poured in from the anode 6 and the electron poured in from the negative pole 25 recombine the luminescence principle of an organic EL device, and operation inside luminous layer EM, and they excite the organic molecule which forms luminous layer EM, and generate an exciton. Light is emitted from a luminous layer in the process in which this exciton carries out radiation inactivation, and from the transparent anode, this light is emitted to the exterior via a transparent insulating substrate, and emits light.

[0016]Thus, it is accumulated in the retention volume 8 and impressed by the gate 15 of 2nd TFT4, and according to the voltage, the electric charge supplied from the 1st sauce S of TFT1 carries out the current drive of the organic EL device, and emits light.

[0017]

[Problem(s) to be Solved by the Invention]However, it is connected to the driving source input terminal T provided outside the display picture element region, it is connected for every display pixel perpendicularly located in a line, and drive line VL which drives an organic EL device as shown in drawing 8 is arranged. Therefore, since resistance of drive line VL becomes large according to the length as it keeps away from the driving source input terminal T, The current which should be supplied essentially was no longer supplied to the organic EL device of the display pixel in a position far from the driving source input terminal T, the display became dark, and there was a fault which display unevenness generates.

[0018]Then, in view of the above-mentioned conventional fault, it succeeds in this invention, and it is a thing.

The purpose is to provide the EL display which the fall of the power supply current by resistance of VL can be controlled, and the current which should be supplied essentially can supply an EL element, and can obtain a bright display.

[0019]
[Means for Solving the Problem]This invention makes homogeneity more resistance of a drive line located in each display pixel, as mentioned above, and the 1st and the 2nd, Each of a drive line is provided in the direction which intersects an extending direction, and it is electrically connected with a drive line and solves by providing a bypass line in a lower layer position rather than said drive line.
[0020]For example, if a bypass line which grows into a layer in which a gate line was formed with chromium is provided and a drive line is contacted, even if it means that a drive line was formed in the shape of a lattice and it keeps away from a driving source input terminal, a rate that resistance falls will be controlled rather than the conventional thing.
[0021]It solves by 3rd forming a bypass line in a layer in which a gate was formed, a layer in which semiconductor membrane was formed, or an insulating layer located between semiconductor membrane and a drive line.
[0022]Although a drive line and a bypass line can originally be formed in a same layer, they need an arrangement area of the part bypass line. However, for example, it can be made to superimpose on the anode by putting on a lower layer of a bypass line. and -- between the anode and bypass lines -- ****** -- since an insulating layer is formed thickly, a problem of parasitic capacitance is also controlled.
[0023]The 4th can be made to control expansion-ization of a viewing area therefore expanded to arrangement of a bypass line by making at least a part of bypass line superimpose on said anode, as mentioned above. A part made to control and other components can also be made to expand.
[0024]It solves by 5th forming a bypass line for said every display pixel, and forming contact in a superposed part with said drive line.
[0025]To the above-mentioned, a bypass line is effective by at least one. However, if there is no bypass line for every display pixel, nonuniformity of a display pixel will occur too by the existence. Here, this is controlled further.
[0026]This invention is [ 6th ] realizable also by bottom product gated mode structure or top gate mold structure.
[0027]
[Embodiment of the Invention]The EL display of this invention is explained. The portion which the portion by which the field which drawing 1 was what showed the display pixel of the EL display with the top view, and it was surrounded by the dotted line and carried out hatching at the point is surrounded as the field and solid line which were formed with the gate material, and hatching is not carried out was surrounded as P-Si layer and the solid line, and carried out hatching at the slanting point is a portion which changes with transparent electrode material. The portion by which was surrounded as the solid line and hatching was carried out by the

slanting line is a portion formed with the metallic material which makes aluminum the charge of a principal member.

[0028]Drawing 2 is an A-A line sectional view of drawing 1, and drawing 3 is a B-B line sectional view. Drawing 4 is the representative circuit schematic. The portion surrounded by the dotted line in drawing 4 shows a display picture element region.

[0029]In this embodiment, the 1st, the 2nd TFT1, and 4 have adopted TFT of a bottom product gated mode, and use p-Si film as an active layer. The gate electrodes 11 and 15 are double gated structures.

[0030]With reference to drawing 1 - drawing 3, the organic electroluminescence display is explained concretely.

[0031]First, there is the transparent substrate 10 in which the surface has insulation at least. According to this embodiment, in order to protect an EL element from moisture, it is installed in the upper surface so that a metal cap (can) may close an EL material. The metal cap omitted in the figure. Since this metal cap is installed, in order to take out luminescent light from said transparent substrate 10, the substrate 10 does not need to be transparent when taking out luminescent light from the upper part, although it needs to be transparent. Here, the transparent substrate 10 which comprises glass, a synthetic resin, etc. is adopted.

[0032]On this transparent substrate 10, the gate line GL was formed along with the upper part neighborhood of one display pixel of drawing 1 at right and left, and the bypass line BL has extended right and left the bottom neighborhood. In order to form the retention volume electrode 2 which acts as a lower layer electrode of the retention volume 8 and to connect this retention volume electrode 2 of each other, retention volume line CL has extended right and left. Since these both the lines GL and CL become by a same layer, hatching of them has been carried out at the point. As a material, since P-Si is adopted as the upper layer, refractory metals, such as Cr and Ta, are adopted. Here, about 1000-2000-A Cr is formed in sputtering. Step coverage is taken into consideration in the case of patterning, and the side is processed into taper shape.

[0033]Then, the gate dielectric film 7 and a semiconductor layer are laminated and formed in the whole surface. Here, it is formed by plasma CVD also including a-Si which is the material of the capacity electrode 3 which is an upper electrode of said gate dielectric film 7, the active layers 12 and 16, and the retention volume 8. Specifically, about 500 A Si nitride, about 1300 A Si oxide film, and about 500-A a-Si are formed by continuation plasma CVD from a lower layer.

[0034]Dehydration annealing is performed in the nitrogen atmosphere of about 400 degrees, and this a-Si is P-Si-ized by excimer laser after that. The numerals 13 and 17 are stopper insulator layers which comprise a Si oxide film, and serve as a mask at the time of the ion implantation of the active layers 12 and 16. TFTof ** 1st1 uses this stopper insulator layer 13

as a mask, P (Lynn) ion is poured in, N channel type sauce and a drain are formed, B (boron) ion is poured in and, as for the 2nd TFT4, P channel type sauce and a drain are formed.
[0035]It is patterned by photolithographic technique like drawing 1. That is, 1st P-Si layer of TFT1 is a lower part of the upper left intersection of the gate line GL and drain line DL, and after it is overlapped on drain line DL and extends the upper layer of the gate electrode 11, it has extended as the capacity electrode 3 superimposed on the retention volume electrode 2. This capacity electrode 3 extends in the lower layer of connection wiring 30 right end used in order to electrically connect with the gate electrode 15 of 2nd TFT4. On the other hand, P-Si layer of 2nd TFT4 extended the 2nd gate electrode 15 top from the lower layer of right-hand side drive line VL, and has extended in the lower layer of the anode 6 which comprises a transparent electrode.
[0036]And the interlayer insulation film 14 is formed in the whole surface. As for this interlayer insulation film 14, three layer systems of about 1000 A Si oxide film, about 3000 A Si nitride, and a 1000-A Si oxide film are formed by the continuation CVD from the bottom. This interlayer insulation film should just exist further at least. Thickness is not restricted to this, either.
[0037]Next, drain line DL, drive line VL, and the connection wiring 30 which carried out hatching by the slanting line of drawing 1 are formed in the upper layer of the interlayer insulation film 14. Naturally contact is formed and, as for the contact hole C1 of drain line DL and the 1st semiconductor layer of TFT1, the contact hole C2 of drive line VL and the semiconductor layer of 2nd TFT4, and the contact hole C4 of the connection wiring 30 and the capacity electrode 3, each semiconductor layer is exposed. Since gate dielectric film is laminated too much unlike the above-mentioned contact hole, the contact hole C5 of the connection wiring 30 and the 2nd gate electrode 15 and the contact hole C6 of drive line VL used as the feature of this invention and the bypass line BL are etched, and Cr is exposed. This line material is the structure where 7000-A aluminum was laminated by the lower layer at 1000-A Mo and the upper layer, and Mo is a barrier layer. The contact hole C3 is mentioned later.
[0038]The further about 2-3-micrometer flattening film PLN is formed in the whole surface. It is in the film for organic electroluminescence described also by the conventional example as one of the reasons for adoption of this flattening film PLN. This film comprises the 1st hole transporting bed 21, 2nd hole transporting bed 22, luminous layer 23, and electron transport layer 24. A hole transporting bed may comprise one layer. Therefore, an organic layer is a layered product of a very thin film. This point generates degradation of an organic layer, and when the worst, it results in destruction, at the same time the luminescent spot which current flows in large quantities via the thin portion of thickness, and shines with that portion particularly will occur if such thickness is not formed very uniformly since an EL element is a current drive. Therefore, in order to prevent this destruction, the whole surface containing the

anode 6 needs to be flat as much as possible, acrylic liquefied resin is applied and after hardening becomes flat here. Of course, it cannot be overemphasized that this flattening film PLN is not restricted to this.

[0039]Here, since the sauce of 2nd TFT4 is connected with the anode 6, the opening of the flattening film PLN and the interlayer insulation film 14 is carried out, and the contact hole C3 where the 2nd active layer 16 was exposed is formed.

[0040]The organic layer which constitutes an EL element is formed at least on the anode 6. First on the anode 6, The 1st hole transporting bed 21 which comprises MTDATA (4 and 4-bis (3-methylphenylphenylamino) biphenyl), and TPD (4, 4, and 4-tris (3-methylphenylpheny.)) The 2nd hole transporting bed 22 which consists of laminotriphenylanine, Bebq2 containing the Quinacridone (Quinacridone) derivative (10-BENZO) [h]It is the structure where laminating formation of the negative pole 25 which comprises light emitting element layer EM which consists of the electron transport layer 24 which comprises the luminous layer 23 which comprises a quinolinol beryllium complex, and Bebq2, a magnesium indium alloy, the alloy of aluminum and Ti, or LiF was carried out in this turn. Since the thickness of the organic layer is mentioned above, refer to it for it. The negative pole 25 adopts the alloy of aluminum and Ti, and the thickness is 1000-2000A.

[0041]Although the anode 6 needs to be patterned for every pixel, the film on the anode 6 is distinguished by structure here.

** : the 2nd structure that the negative pole 25 is not patterned but is substantially formed by solid one throughout a viewing area in 1st structure **:** patterned for every pixel from the anode 6 to the negative pole 25.

** : the 3rd structure of said solid structure where only the anode 6 was patterned for every pixel like drawing 1, and the negative pole was ****(ed) throughout the viewing area from the upper layer of the anode.

[0042]However, since the negative pole 6 is not patterned specially, generally whole surface solid structure has been used for it. In the drawing, as the anode 6 and the negative pole 25 have short-circuited, it is illustrated, but since the organic layer of the EL element is thoroughly covered also including the anode 6 circumference, the short circuit is prevented. This is the same also at a conventional example. Another flattening film may be formed on the flattening film PLN so that the edge of the anode 6 may be covered.

[0043]The metal cap which covers the EL layer of a viewing area or all the EL layers is formed. It is because an EL layer will deteriorate if water is absorbed moisture, and protection is needed against permeation of water. Therefore, an EL layer is not degraded, it is good also as substitution of a cap by a damp-proof high film, for example, a resin layer, and also a metal cap may be carried out on this.

[0044]The hole poured in from the anode 6 and the electron poured in from the negative pole

25 recombine the luminescence principle of an organic EL device, and operation inside luminous layer EM, and they excite the organic molecule which forms luminous layer EM, and generate an exciton. Light is emitted from a luminous layer in the process in which this exciton carries out radiation inactivation, and from the transparent anode, this light is emitted to the exterior via a transparent insulating substrate, and emits light.

[0045]The feature of this invention is in the bypass line BL.

[0046]In the viewing area enclosed with a dotted line, it has extended in the column direction, it is connected to each display pixel of a column direction, and drive line VL supplies driving current so that clearly also from the equivalent circuit of drawing 4. As this viewing area becomes extraordinary length and it stated also to the column of the issue which it is going to solve, a resisted part occurs, but it is making it connect with the bypass line BL which made the line writing direction extend, and the voltage of same electric potential will be impressed to the adjoining display pixel. Since it will be supplied from various directions by drive line VL and the bypass line BL in which current was also formed in the shape of a lattice and the current which should be essentially supplied to the organic EL device formed in each display pixel can be supplied, The fall of the luminosity of the display deterioration by a resisted part mentioned above and a display can be prevented.

[0047]If it forms in the layer in which the gate was formed like the bypass line BL of drawing 3, it will become movable in the direction shown by an arrow. That is, if the bypass line BL formed between the anode 6 of drawing 1 and the gate line GL is seen and explained, the bypass line BL, The area increase by arranging the bypass line BL can be controlled by being able to make at least a part superimpose on the anode 6, and making it superimpose. Since the gate dielectric film 7, the interlayer insulation film 14, and the flattening film PLN intervene between the gate line GL and the anode 6, most parasitic capacitance generated in the meantime can be disregarded.

[0048]Rather than drive line VL, the position of the bypass line BL should just be located in a lower layer, and explains other examples to drawing 5 and drawing 6.

[0049]As for drawing 5, the bypass line BL is formed on the gate dielectric film 7. When simplifying a process here, it comprises P-Si, but the refractory metal mentioned above may be sufficient.

[0050]Since drawing 6 is after the bypass line BL was formed between the layers of an interlayer insulation film and P-Si was formed here, and the rise in heat of a manufacturing process is not so severe, either, the material which uses aluminum as the main ingredients, a high-melting point metallic material, and P-Si can be used for the bypass line BL. Since a Si oxide film, Si nitride, and a Si oxide film are formed from a lower layer, the interlayer insulation film can arrange said bypass line BL among these. Of course, superposition in the anode is also possible. However, increase of parasitic capacitance is not escaped as it arranges in the

upper layer. The dotted line formed in the interlayer insulation film 14 shows the interface between layers.

[0051]The insertion number of the bypass line BL is described. That is, in drawing 4, if at least one number of the bypass line BL is formed, the reduction in resistance can be controlled. However, if it arranges for every pixel, the current which distribution of resistance and distribution of voltage become still more uniform, and originally flows, i.e., the luminosity which should emit light, can be made to reproduce more faithfully.

[0052]As mentioned above, although bottom product gated mode structure has explained, this invention is employable also by top gate mold structure. In top gate type TFT, on a transparent substrate, For example, the active layer, the gate dielectric film, the gate, the interlayer insulation film, and metal wiring which comprise P-Si are laminated (this upper layer bottom product gated mode structure and parenchyma the same structure), on a transparent substrate, on gate dielectric film, it is Cr and a refractory metal, and is said Al material and a high-melting point metallic material, and, for a ** reason, wiring can be formed.

[0053]Finally, bypass-line BL0 arranged at the outside of a display picture element region is described. The rectangle which an outside solid line is an outside of an EL display, and a thick solid line is bypass-line BL0 connected with the driving source, and is most shown further in the bottom of it by drawing 4 is the field in which the drive circuit was formed. That is, the gestalt from a viewing area to the outside of a transparent substrate is shown typically. A drive circuit is made from P-Si here. As shown also in a figure, it is connected with a circuit and drain line DL is carrying out the conclusion of an end in the drive circuit formation area, and drain line DL is not formed between the drive circuit formation area and the outside. Therefore, there is also no intersection with drain line DL, and as shown in a figure, bypass-line BL0 has a space which can extend thickly right and left. And bypass-line BL0 can be formed by drain line DL or drive line VL, and a same layer, and it can form wiring with the material which uses aluminum as the main ingredients. Therefore, the voltage reduced [ resistance of bypass-line BL0 self can be reduced greatly, and ] the resistance of drive line VL more simultaneously stabilized can be supplied.

[0054]In an above-mentioned embodiment, although p-Si film was used as semiconductor membrane, semiconductor membrane, such as a microcrystal silicon film or an amorphous silicon film, may be used.

[0055]In an above-mentioned embodiment, although the organic electroluminescence display was explained, this invention is not limited to it, a luminous layer can apply it also to the inorganic EL display which comprises an inorganic material, and the same effect is acquired.

[0056]

[Effect of the Invention]By providing each of a drive line in the direction which intersects an extending direction, electrically being connected with a drive line and providing a bypass line in

the 1st rather than said drive line at a lower layer position so that clearly also from the above explanation. Even if it means that the drive line was formed in the shape of a lattice and it keeps away from a driving source input terminal, the rate that resistance falls can be made to control rather than the conventional thing.

[0057]Although a drive line and a bypass line can originally be formed in a same layer, they need the arrangement area of the part bypass line. However, for example, it can be made to superimpose on the anode by putting on the lower layer of a bypass line. and -- between the anode and bypass lines -- ****** -- since an insulating layer is formed thickly, the problem of parasitic capacitance is also controlled.

[0058]Expansion-ization of the viewing area therefore expanded to arrangement of a bypass line can be made to control by making at least a part of bypass line superimpose on said anode, as mentioned above. The part made to control and other components can also be made to expand.

[0059]The nonuniformity of each display pixel can be made to control more by forming a bypass line for said every display pixel, and forming contact in a superposed part with said drive line.

[0060]Therefore, increase of resistance by the length of a drive line can be reduced, the current which should be supplied essentially can be supplied to the EL element of each display pixel, and expansion-ization of EL viewing area can also obtain simultaneously deter the EL display which can prevent becoming a dark display.

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## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a top view of the display pixel of the EL display of this invention.
[Drawing 2]It is a sectional view of the A-A line of drawing 1.
[Drawing 3]It is a sectional view of the B-B line of drawing 1.
[Drawing 4]It is a representative circuit schematic of the EL display of this invention.
[Drawing 5]It is a figure explaining the locating position of the bypass line BL of drawing 3.
[Drawing 6]It is a figure explaining the locating position of the bypass line BL of drawing 3.
[Drawing 7]It is a top view of the display pixel of the conventional EL display.
[Drawing 8]It is a representative circuit schematic of the conventional EL display.
[Drawing 9]It is a sectional view of the A-A line of drawing 7.
[Drawing 10]It is a sectional view of the B-B line of drawing 7.
[Description of Notations]
1 The 1st TFT
2 Retention volume electrode
3 Capacity electrode
4 The 2nd TFT
6 Anode
7 Gate dielectric film
8 Retention volume
14 Interlayer insulation film
20 EL element
GL Gate line
DL Drain line
CL Retention volume line
VL Drive line VL

BL Bypass line BL

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[Translation done.]

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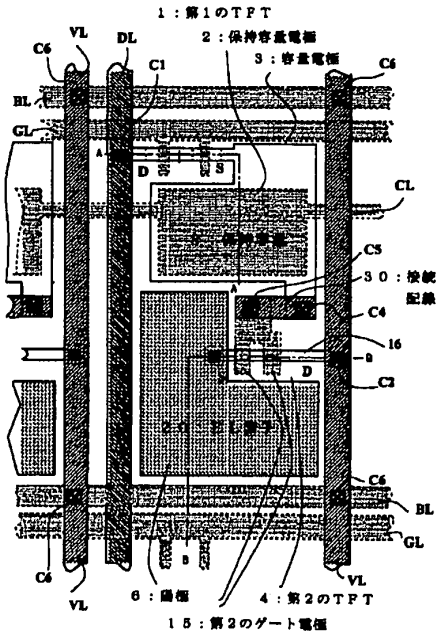
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(54)【発明の名称】　ＥＬ表示装置

(57)【要約】
【課題】　駆動電源入力端子からの距離に起因する駆動ラインＶＬの抵抗による電源電流の低下を抑制し、本来供給されるべき電流がＥＬ素子に供給して、明るい表示を得ることができるＥＬ表示装置を提供する。
【解決手段】　表示画素を備えた表示画素領域に形成された有機ＥＬ素子２０に駆動電源からの駆動電流を供給するための各駆動ラインＶＬに於いて、隣接する各表示画素に配置された各駆動ラインＶＬは、表示画素領域内においてバイパスラインＢＬに接続されており、それによって駆動ラインＶＬの抵抗による電源電流の低下を抑制しする。しかも駆動ラインＶＬの形成された層よりも下層に形成され、陽極６との重畳も可能となる。



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【特許請求の範囲】

【請求項１】　陽極と陰極との間に発光層を有するＥＬ素子と、

半導体膜からなる能動層のドレインが前記ＥＬ素子の駆動ラインに電気的に接続され、前記能動層のソースが前記ＥＬ素子に電気的に接続された薄膜トランジスタとを備えた表示画素がマトリクス状に配列して成るＥＬ表示装置であり、

前記駆動ラインと交差する方向に延在され、且つ前記駆動ラインと電気的に接続され、前記駆動ラインよりも下層に設けられたバイパスラインを有する事を特徴とするＥＬ表示装置。

【請求項２】　陽極と陰極との間に発光層を有するＥＬ素子と、

半導体膜から成る能動層のドレインがドレインラインに接続され、ゲートがゲートラインにそれぞれ接続された第１の薄膜トランジスタと、

前記半導体膜からなる能動層のドレインが前記ＥＬ素子の駆動ラインに接続され、ゲートが前記第１の薄膜トランジスタのソースに電気的に接続され、ソースが前記ＥＬ素子に接続された第２の薄膜トランジスタとを備えた表示画素がマトリクス状に配列して成るＥＬ表示装置であり、

前記駆動ラインと交差する方向に延在され、且つ前記駆動ラインと電気的に接続され、前記駆動ラインよりも下層に設けられたバイパスラインを有する事を特徴とするＥＬ表示装置。

【請求項３】　前記バイパスラインは、前記ゲートが形成された層、前記半導体膜が形成された層、または前記半導体膜と前記駆動ラインとの間に位置する絶縁層の層間に形成される請求項１または請求項２に記載のＥＬ表示装置。

【請求項４】　前記バイパスラインは、少なくとも一部が前記陽極と重畳して成る請求項３に記載のＥＬ表示装置。

【請求項５】　前記バイパスラインは、前記表示画素毎に形成され、前記駆動ラインとの重畳部には前記表示画素毎にコンタクトが形成される請求項１、請求項２、請求項３または請求項４に記載のＥＬ表示装置。

【請求項６】　前記薄膜トランジスタは、トップゲート型構造からなる請求項１、請求項２、請求項３、請求項４または請求項５に記載のＥＬ表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、エレクトロルミネッセンス素子及び薄膜トランジスタを備えたエレクトロルミネッセンス表示装置に関する。

【０００２】

【従来の技術】近年、エレクトロルミネッセンス（Electro Luminescence：以下、「ＥＬ」と称する。）素子

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を用いたＥＬ表示装置が、ＣＲＴやＬＣＤに代わる表示装置として注目されており、例えば、そのＥＬ素子を駆動させるスイッチング素子として薄膜トランジスタ（Thin Film Transistor：以下、「ＴＦＴ」と称する。）を備えたＥＬ表示装置の研究開発も進められている。

【０００３】図７に有機ＥＬ表示装置の表示画素を示し、図８に有機ＥＬ表示装置の等価回路図を示す。また、図９に図７のＡ－Ａ線に沿った断面図を示し、図１０に図７のＢ－Ｂ線に沿った断面図を示す。

【０００４】図に示すように、ゲートラインＧＬとドレインラインＤＬとに囲まれた領域に表示画素が形成されている。両信号線の交点付近にはスイッチング素子である第１のＴＦＴ１が備えられており、そのＴＦＴ１のソースは、保持容量電極２と容量を構成する容量電極３を兼ねるとともに、有機ＥＬ素子を駆動する第２のＴＦＴ４のゲート５に接続されている。第２のＴＦＴ４のソースは有機ＥＬ素子の陽極６に接続され、他方のドレインは有機ＥＬ素子を駆動する駆動ラインＶＬに接続されている。

【０００５】また、前記保持容量電極２はクロム等から成っており、上層のゲート絶縁膜７を介して第１のＴＦＴ１のソースと一体の容量電極３と重畳し、前記ゲート絶縁膜７を誘電体層として電荷を蓄積している。この保持容量８は、第２のＴＦＴ４のゲート５に印加される電圧を保持している。

【０００６】続いて、スイッチング用の第１のＴＦＴ１について図７と図９を参照しながら説明する。

【０００７】まず石英ガラス、無アルカリガラス等からなる透明な絶縁性基板１０上に、クロム（Ｃｒ）、モリブデン（Ｍｏ）などの高融点金属からなる第１のゲート電極１１が設けられている。この第１のゲート電極１１は、図７のようにゲートラインＧＬと一体で例えば左右に複数本並行に延在されている。また図９の第１のゲート電極１１の右隣には、第１のゲート電極１１と同一工程で作られた保持容量電極２が形成されている。この保持容量電極２は、図７の様に容量を構成するため、第１のＴＦＴ１と第２のＴＦＴ４の間で、拡大された部分を有し、これらは左右に延在された保持容量ラインＣＬと一体で構成されている。

【０００８】続いて、ゲート絶縁膜７を介して多結晶シリコン（ｐ－Ｓｉと称する。）膜からなる第１の能動層１２が形成されている。この能動層１２は、ＬＤＤ（Lightly Doped Drain）構造が採用されている。即ち、ゲートの両側に低濃度領域が設けられ、更に外側には、高濃度のソース領域及びドレイン領域が設けられている。前記能動層１２の上には、ストッパ絶縁膜１３が設けられている。このストッパ絶縁膜１３は、能動層１２へのイオン注入阻止膜であり、ここではＳｉ酸化膜から成る。

【０００９】そして、ゲート絶縁膜７、能動層１２及び

ストッパ絶縁膜１３上には、例えば、順にＳｉ$O_2$膜、ＳｉＮ膜及びＳｉ$O_2$膜が積層された層間絶縁膜１４が設けられ、ドレインに設けたコンタクトホールＣ１を介してドレイン電極と成るドレインラインＤＬが電気的に接続されている。更に全面には、表面の凹凸を平坦にするため、例えば有機樹脂から成る平坦化膜ＰＬＮが形成されている。ＥＬ表示装置は、電流駆動なので、ＥＬ層が均一な膜厚でなければならない。膜厚が薄い部分で電流集中が発生するからである。従って少なくともこの形成領域は、かなりの平坦性が要求されるため、前記平坦化膜ＰＬＮが採用される。

【００１０】次に、有機ＥＬ素子を駆動する第２のＴＦＴ４について図１０を参照して説明する。

【００１１】前述した絶縁性基板１０上には、前記第１のゲート１１と同一材料の第２のゲート電極１５が設けられており、ゲート絶縁膜７を介して第２の能動層１６が設けられている。前述と同様に能動層の上にはストッパ絶縁膜１７が設けられている。

【００１２】前記能動層１６には、ゲート電極１５上方に真性又は実質的に真性であるチャネルと、このチャネルの両側に、ｐ型不純物のソース領域及びドレイン領域が設けられｐ型チャネルＴＦＴを構成している。

【００１３】そして全面には、前述した層間絶縁膜１４が形成されている。そしてコンタクトホールＣ２を介して駆動ラインＶＬが電気的に接続されている。更に全面には、前述した平坦化膜ＰＬＮが形成され、コンタクトホールＣ３によりソースが露出されている。そしてこのコンタクトホールを介してＩＴＯ（Indium Thin Oxide）から成る透明電極（有機ＥＬ素子の陽極）６が形成されている。

【００１４】有機ＥＬ素子２０は、前記陽極６、ＭＴＤＡＴＡ（4,4-bis(3-methylphenylphenylamino)biphenyl）から成る第１ホール輸送層２１、及びＴＰＤ（4,4,4-tris(3-methylphenylphenylamino)triphenylanine）からなる第２ホール輸送層２２、キナクリドン（Quinacridone）誘導体を含むＢｅｂｑ２（10-ベンゾ〔ｈ〕キノリノール－ベリリウム錯体）から成る発光層２３及びＢｅｂｑ２から成る電子輸送層２４からなる発光素子層ＥＭ、マグネシウム・インジウム合金から成る陰極２５がこの順番で積層形成された構造であり、有機ＥＬ素子の実質全面に設けられている。

【００１５】有機ＥＬ素子の発光原理および動作は、陽極６から注入されたホールと、陰極２５から注入された電子とが発光層ＥＭの内部で再結合し、発光層ＥＭを形成する有機分子を励起して励起子を発生させる。この励起子が放射失活する過程で発光層から光が放たれ、この光が透明な陽極から透明絶縁基板を介して外部へ放出されて発光する。

【００１６】このように、第１のＴＦＴ１のソースＳから供給された電荷が保持容量８に蓄積され、第２のＴＦＴ４のゲート１５に印加され、その電圧に応じて有機ＥＬ素子を電流駆動し、発光する。

【００１７】

【発明が解決しようとする課題】ところが、図８に示すように有機ＥＬ素子を駆動する駆動ラインＶＬは、表示画素領域外に設けた駆動電源入力端子Ｔに接続されており、そして縦に並んだ表示画素ごとに接続されて配置されている。そのため、駆動電源入力端子Ｔから遠ざかるにつれて駆動ラインＶＬの抵抗がその長さに応じて大きくなるので、駆動電源入力端子Ｔから遠い位置にある表示画素の有機ＥＬ素子には本来供給されるべき電流が供給されなくなり、表示が暗くなり、表示ムラが発生する欠点があった。

【００１８】そこで本発明は、上記の従来の欠点に鑑みて為されたものであり、駆動ラインＶＬの抵抗による電源電流の低下を抑制し、本来供給されるべき電流がＥＬ素子に供給して、明るい表示を得ることができるＥＬ表示装置を提供することを目的とする。

【００１９】

【課題を解決するための手段】本発明は、前述したように各表示画素に位置する駆動ラインの抵抗をより均一にするもので、第１、第２は、駆動ラインのそれぞれを、延在方向と交差する方向に設けると共に、駆動ラインと電気的に接続され、前記駆動ラインよりも下層の位置にバイパスラインを設けることで解決するものである。

【００２０】例えば、ゲートラインが形成された層に、クロムで成るバイパスラインを設け、駆動ラインとコンタクトすれば、駆動ラインは、格子状に形成されたことになり、駆動電源入力端子から遠ざかっても、抵抗値の下がる割合は、従来のものよりも抑制される。

【００２１】第３に、バイパスラインを、ゲートが形成された層、半導体膜が形成された層、または半導体膜と駆動ラインとの間に位置する絶縁層に形成する事で解決するものである。

【００２２】駆動ラインとバイパスラインは、本来同層にて形成できるが、その分バイパスラインの配置面積を必要とする。しかしバイパスラインの下層に置くことで、例えば陽極と重畳させることができる。しかも陽極とバイパスラインとの間には、からり厚く絶縁層が形成されるため、寄生容量の問題も抑制される。

【００２３】第４に、前述したようにバイパスラインの少なくとも一部を前記陽極と重畳させることで、バイパスラインの配置に依って拡大する表示領域の拡大化を抑制させることができる。また抑制させた分、他の構成要素を拡大させることもできる。

【００２４】第５に、バイパスラインを、前記表示画素毎に形成し、前記駆動ラインとの重畳部にコンタクトを形成する事で解決するものである。

【００２５】前述までは、バイパスラインは、少なくとも１本で効果がある。しかし表示画素毎にバイパスライ

ンが無いと、その有無により表示画素のムラがやはり発生する。ここでは、これを更に抑制する。

【００２６】第６に、本発明は、ボトムゲート型構造でも、トップゲート型構造でも実現できる。

【００２７】

【発明の実施の形態】本発明のＥＬ表示装置について説明する。図１は、ＥＬ表示装置の表示画素を平面図で示したもので、点線で囲まれ点でハッチングした領域は、ゲート材料で形成された領域、実線で囲まれハッチングされていない部分は、Ｐ－Ｓｉ層、実線で囲まれ斜め点でハッチングした部分は、透明電極材料で成る部分である。更に実線で囲まれ斜め線でハッチングされた部分が、Ａｌを主材料とする金属材料で形成された部分である。

【００２８】図２は、図１のＡ－Ａ線断面図であり、図３は、Ｂ－Ｂ線断面図である。更に図４は、その等価回路図である。尚図４に於いて点線で囲まれた部分は、表示画素領域を示す。

【００２９】なお、本実施の形態においては、第１、第２のＴＦＴ１、４ともに、ボトムゲート型のＴＦＴを採用しており、能動層としてｐ－Ｓｉ膜を用いている。またゲート電極１１、１５は、ダブルゲート構造である。

【００３０】では、図１～図３を参照し、有機ＥＬ表示装置を具体的に説明していく。

【００３１】まず、少なくとも表面が絶縁性を有する透明基板１０がある。本実施の形態では、ＥＬ素子を水分から保護するため、メタルキャップ（カン）がＥＬ材料を封止するように上面に設置されている。尚、図においてメタルキャップは省略をした。このメタルキャップが設置されているため発光光は、前記透明基板１０から取り出すため、基板１０は、透明である必要があるが、発光光を上方から取り出す場合は、透明である必要はない。ここでは、ガラスや合成樹脂などから成る透明基板１０を採用している。

【００３２】この透明基板１０の上には、図１の一表示画素の上側辺に沿って、左右にゲートラインＧＬが設けられ、下側辺にはバイパスラインＢＬが左右に延在されている。また保持容量８の下層電極として作用する保持容量電極２が設けられると共に、この保持容量電極２をお互いにつなぐため、保持容量ラインＣＬが左右に延在されている。これら両ラインＧＬ、ＣＬは、同層でなるため、点でハッチングしてある。また材料としては、上層にＰ－Ｓｉを採用する理由からＣｒやＴａ等の高融点金属が採用される。ここでは、約１０００～２０００ÅのＣｒがスパッタリングにて形成されている。またパターニングの際は、ステップカバレージが考慮され、側辺はテーパー形状に加工されている。

【００３３】続いて、全面にはゲート絶縁膜７と半導体層が積層されて形成されている。ここでは、前記ゲート絶縁膜７、能動層１２、１６および保持容量８の上層電極である容量電極３の材料であるａ－Ｓｉも含めてプラズマＣＶＤで形成されている。具体的には、下層より約５００ÅのＳｉ窒化膜、約１３００ÅのＳｉ酸化膜および約５００Åのａ－Ｓｉが連続プラズマＣＶＤで形成される。

【００３４】このａ－Ｓｉは、約４００度の窒素雰囲気中で脱水素アニールが行われ、その後、エキシマレーザによりＰ－Ｓｉ化される。また符号１３、１７は、Ｓｉ酸化膜から成るストッパ絶縁膜であり、能動層１２、１６のイオン注入時のマスクとなる。第１のＴＦＴ１は、このストッパ絶縁膜１３をマスクにしてＰ（リン）イオンが注入され、Ｎチャンネル型のソース、ドレインが形成され、第２のＴＦＴ４は、Ｂ（ボロン）イオンが注入されてＰチャンネル型のソース、ドレインが形成されている。

【００３５】また図１のように、ホトリソグラフィ技術によりパターニングされている。つまり第１のＴＦＴ１のＰ－Ｓｉ層は、ゲートラインＧＬとドレインラインＤＬの左上交差部の下方で、ドレインラインＤＬと重畳し、ゲート電極１１の上層を延在した後、保持容量電極２と重畳する容量電極３として延在されている。またこの容量電極３は、第２のＴＦＴ４のゲート電極１５と電気的に接続するために用いられる接続配線３０右端の下層に延在される。一方、第２のＴＦＴ４のＰ－Ｓｉ層は、右側の駆動ラインＶＬの下層から第２のゲート電極１５の上を延在し、透明電極から成る陽極６の下層に延在されている。

【００３６】そして全面には、層間絶縁膜１４が形成されている。この層間絶縁膜１４は、下から約１０００ÅのＳｉ酸化膜、約３０００ÅのＳｉ窒化膜、１０００ÅのＳｉ酸化膜の三層構造が連続ＣＶＤで形成されている。この層間絶縁膜は、少なくとも一層有れば良い。膜厚もこれに限らない。

【００３７】次に、層間絶縁膜１４の上層には、図１の斜め線でハッチングしたドレインラインＤＬ、駆動ラインＶＬおよび接続配線３０が形成される。当然コンタクトが形成され、ドレインラインＤＬと第１のＴＦＴ１の半導体層とのコンタクト孔Ｃ１、駆動ラインＶＬと第２のＴＦＴ４の半導体層とのコンタクト孔Ｃ２、接続配線３０と容量電極３とのコンタクト孔Ｃ４は、それぞれの半導体層が露出されている。また接続配線３０と第２のゲート電極１５のコンタクト孔Ｃ５、本発明の特徴となる駆動ラインＶＬとバイパスラインＢＬのコンタクト孔Ｃ６は、前述のコンタクト孔とは異なり、ゲート絶縁膜が余分に積層されているため、更にエッチングされＣｒが露出されている。このライン材料は、下層に１０００ÅのＭｏ、上層に７０００ÅのＡｌが積層された構造であり、Ｍｏは、バリア層である。尚コンタクト孔Ｃ３は、後述する。

【００３８】更に約２～３μｍの平坦化膜ＰＬＮが全面

に形成されている。この平坦化膜ＰＬＮの採用の理由の一つとして、従来例でも述べた有機ＥＬ用の膜にある。この膜は、第１のホール輸送層２１、第２ホール輸送層２２、発光層２３及び電子輸送層２４から成る。またホール輸送層は、一層から構成されても良い。従って、有機層が非常に薄い膜の積層体である。またＥＬ素子は、電流駆動であるため、これらの膜厚が極めて均一に形成されないと、膜厚の薄い部分を介して電流が大量に流れ、その部分にひときわ輝く輝点が発生すると同時に、このポイントは、有機膜の劣化を発生し、最悪の場合破壊に至る。従って、この破壊を防止するには、陽極６を含む全面ができるだけ平坦である必要があり、ここではアクリル系の液状樹脂が塗布され、硬化後は平坦になる。もちろんこの平坦化膜ＰＬＮは、これに限らない事は言うまでもない。

【００３９】ここでは、陽極６と第２のＴＦＴ４のソースが接続されるため、平坦化膜ＰＬＮおよび層間絶縁膜１４が開口され、第２の能動層１６が露出されたコンタクト孔Ｃ３が形成されている。

【００４０】更に少なくとも陽極６上には、ＥＬ素子を構成する有機膜が形成されている。まず陽極６の上には、ＭＴＤＡＴＡ（4,4-bis(3-methylphenylphenylamino)biphenyl）から成る第１ホール輸送層２１、及びＴＰＤ（4,4,4-tris(3-methylphenylpheny lamino)triphenylanine）からなる第２ホール輸送層２２、キナクリドン（Quinacridone）誘導体を含むＢｅｂｑ2（10-ベンゾ〔h〕キノリノール－ベリリウム錯体）から成る発光層２３及びＢｅｂｑ2から成る電子輸送層２４からなる発光素子層ＥＭ、マグネシウム・インジウム合金、ＡｌとＴｉの合金またはＬｉＦ等から成る陰極２５がこの順番で積層形成された構造である。有機層の膜厚は、前述してあるのでそれを参照。また、陰極２５はＡｌとＴｉの合金を採用し、その膜厚は１０００～２０００Åである。

【００４１】ここで陽極６は、画素毎にパターニングされる必要があるが、陽極６の上の膜は、構造により区別される。

①：陽極６から陰極２５まで画素毎にパターニングされる第１の構造

②：①に於いて、陰極２５は、パターニングされず、実質的に表示領域全域にベタで形成される第２の構造。

③：陽極６だけが図１の様に画素毎にパターニングされ、陽極の上層から陰極までは、表示領域全域に励精された前記ベタ構造の第３の構造。

【００４２】ただし、陰極６は、わざわざパターニングすることもないので一般には全面ベタ構造を採用している。また図面では、陽極６と陰極２５が短絡してる如く図示されているが、ＥＬ素子の有機膜は、陽極６周辺も含み完全に覆われているので短絡は防止されている。これは従来例でも同じである。また陽極６のエッジをカバーするように、平坦化膜ＰＬＮの上に更に別の平坦化膜が形成されても良い。

【００４３】更に、表示領域のＥＬ層、または全てのＥＬ層をカバーするメタルキャップが形成されている。ＥＬ層は、水を吸湿すると劣化し、水の浸入に対して保護が必要となるからである。従ってＥＬ層を劣化させず、耐湿性の高い膜、例えば樹脂膜でキャップの代用としても良いし、更にこの上にメタルキャップをしても良い。

【００４４】有機ＥＬ素子の発光原理および動作は、陽極６から注入されたホールと、陰極２５から注入された電子とが発光層ＥＭの内部で再結合し、発光層ＥＭを形成する有機分子を励起して励起子を発生させる。この励起子が放射失活する過程で発光層から光が放たれ、この光が透明な陽極から透明絶縁基板を介して外部へ放出されて発光する。

【００４５】本発明の特徴は、バイパスラインＢＬにある。

【００４６】図４の等価回路からも明らかなように、駆動ラインＶＬは、点線で囲んだ表示領域内において、列方向に延在しており、列方向の各表示画素に接続されて駆動電流を供給している。この表示領域は、非常な長さになり、解決しようとする課題の欄にも述べたように抵抗分が発生するが、行方向に延在させたバイパスラインＢＬと接続させることで、隣接する表示画素には同電位の電圧が印加されることになる。また電流も格子状に形成された駆動ラインＶＬ及びバイパスラインＢＬにより色々な方向から供給されることになり、各表示画素に設けられた有機ＥＬ素子に本来供給すべき電流を供給することができるので、前述した抵抗分による表示劣化、表示の明るさの低下を防止することができる。

【００４７】また図３のバイパスラインＢＬの様に、ゲートが形成された層に形成すれば、矢印で示す方向に移動が可能となる。つまり図１の陽極６とゲートラインＧＬとの間に形成されたバイパスラインＢＬを見て説明すれば、バイパスラインＢＬは、陽極６と少なくとも一部を重畳させることができ、重畳させることにより、バイパスラインＢＬを配置することによる面積増大を抑制することができる。またゲートラインＧＬと陽極６の間には、ゲート絶縁膜７と層間絶縁膜１４および平坦化膜ＰＬＮが介在されるので、この間に発生する寄生容量は、殆ど無視することができる。

【００４８】またバイパスラインＢＬの位置は、駆動ラインＶＬよりも下層に位置すれば良く、図５、図６に他の例を説明する。

【００４９】図５は、バイパスラインＢＬがゲート絶縁膜７の上に形成されるものである。ここで工程を簡略化する場合は、Ｐ－Ｓｉで構成されるが、前述した高融点金属でも良い。

【００５０】図６は、バイパスラインＢＬが層間絶縁膜の層間に形成されたもので、ここではＰ－Ｓｉが形成さ

れた後であるので、製造工程の温度上昇もそれほど厳しくないため、バイパスラインＢＬは、Ａｌを主成分とする材料や高融点金属材料、Ｐ－Ｓｉを採用できる。層間絶縁膜は、下層からＳｉ酸化膜、Ｓｉ窒化膜、Ｓｉ酸化膜が形成されるので、これらの間に前記バイパスラインＢＬを配置することができる。もちろん陽極との重畳も可能である。しかし上層に配置するに従い、寄生容量の増大は免れない。尚層間絶縁膜１４内に形成される点線は、層間の界面を示すものである。

【００５１】更にバイパスラインＢＬの挿入本数について述べる。つまり図４において、バイパスラインＢＬの本数は、少なくとも1本形成されれば、抵抗の減少は抑制できる。しかし各画素毎に配置すれば、抵抗の分布、電圧の分布が更に均一となり本来流れる電流、すなわち発光すべき輝度をより忠実に再現させることができる。

【００５２】以上、ボトムゲート型構造で説明してきたが、本発明は、トップゲート型構造でも採用できる。トップゲート型ＴＦＴの場合は、透明基板上には、例えばＰ－Ｓｉから成る能動層、ゲート絶縁膜、ゲート、層間絶縁膜、メタル配線が積層され（この上層はボトムゲート型構造と実質同じ構造）るため、透明基板上では、Ｃｒや高融点金属で、ゲート絶縁膜の上には前記Ａｌ材料、高融点金属材料で、配線が形成できる。

【００５３】最後に、表示画素領域の外側に配置されるバイパスラインＢＬ０について述べる。図４で、一番外側の実線は、ＥＬ表示装置の外形であり、太い実線は駆動電源と接続されたバイパスラインＢＬ０で、更にその下に示す矩形は、駆動回路が形成された領域である。つまり表示領域から透明基板の外形までの形態を模式的に示している。ここで駆動回路はＰ－Ｓｉで作り込まれている。図からも判るようにドレインラインＤＬは、駆動回路形成領域で回路と接続されて一端終結しており、駆動回路形成領域と外形の間は、ドレインラインＤＬが形成されていない。従ってドレインラインＤＬとの交差もなく図のようにバイパスラインＢＬ０が左右に太く延在できるスペースを有している。しかもバイパスラインＢＬ０は、ドレインラインＤＬまたは駆動ラインＶＬと同層で形成でき、Ａｌを主成分とする材料で配線が形成できる。従ってバイパスラインＢＬ０自身の抵抗を大きく低下させることができ、駆動ラインＶＬの抵抗値をより低下させることができると同時に安定した電圧を供給できる。

【００５４】上述の実施の形態においては、半導体膜としてｐ－Ｓｉ膜を用いたが、微結晶シリコン膜又は非晶質シリコン膜等の半導体膜を用いても良い。

【００５５】更に、上述の実施の形態においては、有機ＥＬ表示装置について説明したが、本発明はそれに限定されるものではなく、発光層が無機材料から成る無機ＥＬ表示装置にも適用が可能であり、同様の効果が得られる。

【００５６】

【発明の効果】以上の説明からも明らかなように、第１に、駆動ラインのそれぞれを、延在方向と交差する方向に設け、駆動ラインと電気的に接続され、前記駆動ラインよりも下層の位置にバイパスラインを設けることで、駆動ラインは、格子状に形成されたことになり、駆動電源入力端子から遠ざかっても、抵抗値の下がる割合は、従来のものよりも抑制させる事ができる。

【００５７】また駆動ラインとバイパスラインは、本来同層にて形成できるが、その分バイパスラインの配置面積を必要とする。しかしバイパスラインの下層に置くことで、例えば陽極と重畳させることができる。しかも陽極とバイパスラインとの間には、からり厚く絶縁層が形成されるため、寄生容量の問題も抑制される。

【００５８】更には、前述したようにバイパスラインの少なくとも一部を前記陽極と重畳させることで、バイパスラインの配置に依って拡大する表示領域の拡大化を抑制させることができる。また抑制させた分、他の構成要素を拡大させることもできる。

【００５９】また、バイパスラインを、前記表示画素毎に形成し、前記駆動ラインとの重畳部にコンタクトを形成する事で、各表示画素のムラをより抑制させることができる。

【００６０】従って、駆動ラインの長さによる抵抗の増大を低減し、本来供給されるべき電流を各表示画素のＥＬ素子に供給することができ、暗い表示になることを防止することができるＥＬ表示装置を得ることができると同時に、ＥＬ表示領域の拡大化も抑止することができる。

【図面の簡単な説明】

【図１】本発明のＥＬ表示装置の表示画素の平面図である。

【図２】図１のＡ－Ａ線の断面図である。

【図３】図１のＢ－Ｂ線の断面図である。

【図４】本発明のＥＬ表示装置の等価回路図である。

【図５】図３のバイパスラインＢＬの配置位置を説明する図である。

【図６】図３のバイパスラインＢＬの配置位置を説明する図である。

【図７】従来のＥＬ表示装置の表示画素の平面図である。

【図８】従来のＥＬ表示装置の等価回路図である。

【図９】図７のＡ－Ａ線の断面図である。

【図１０】図７のＢ－Ｂ線の断面図である。

【符号の説明】

| | |
|---|---|
| 1 | 第１のＴＦＴ |
| 2 | 保持容量電極 |
| 3 | 容量電極 |
| 4 | 第２のＴＦＴ |
| 6 | 陽極 |

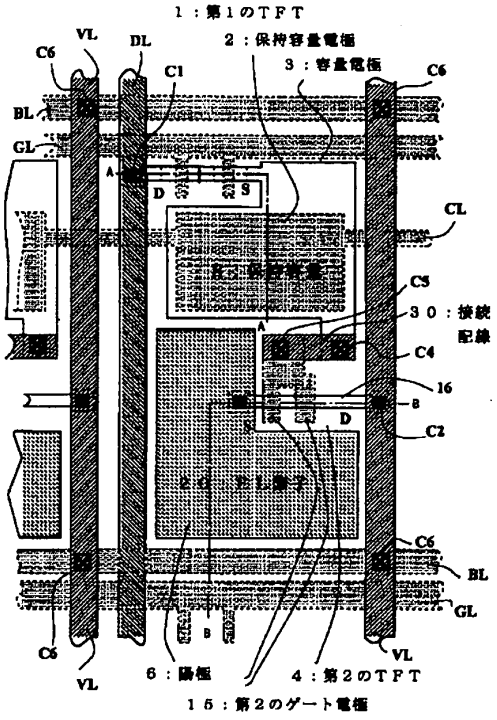
11

| | |
|---|---|
| 7 | ゲート絶縁膜 |
| 8 | 保持容量 |
| １４ | 層間絶縁膜 |
| ２０ | ＥＬ素子 |
| ＧＬ | ゲートライン |

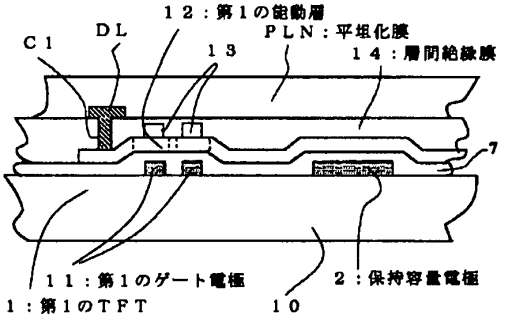
12

| | |
|---|---|
| ＤＬ | ドレインライン |
| ＣＬ | 保持容量ライン |
| ＶＬ | 駆動ラインＶＬ |
| ＢＬ | バイパスラインＢＬ |

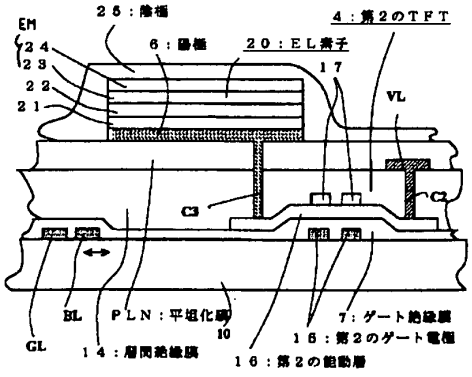
【図１】



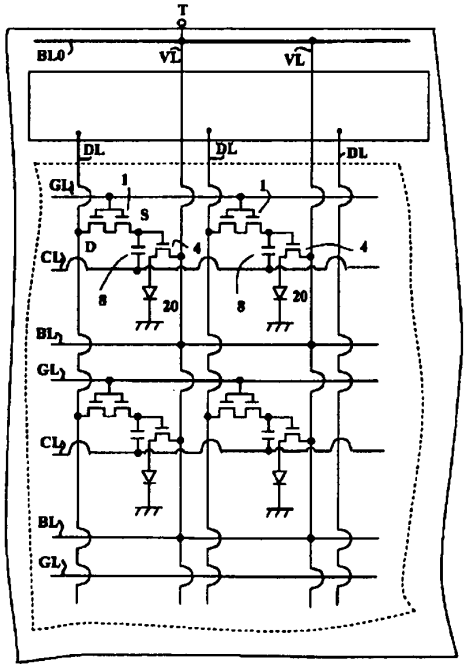

【図２】



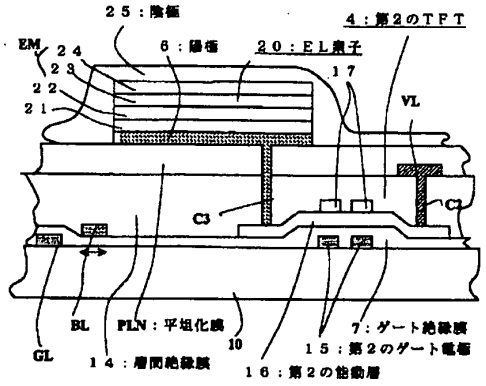

【図３】



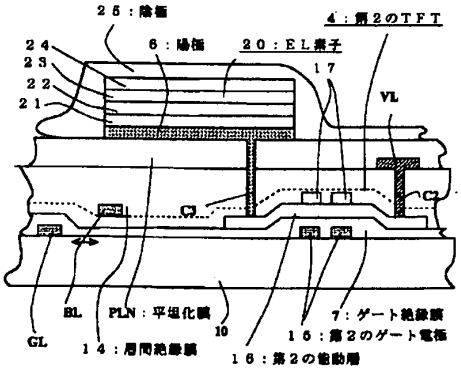

【図４】



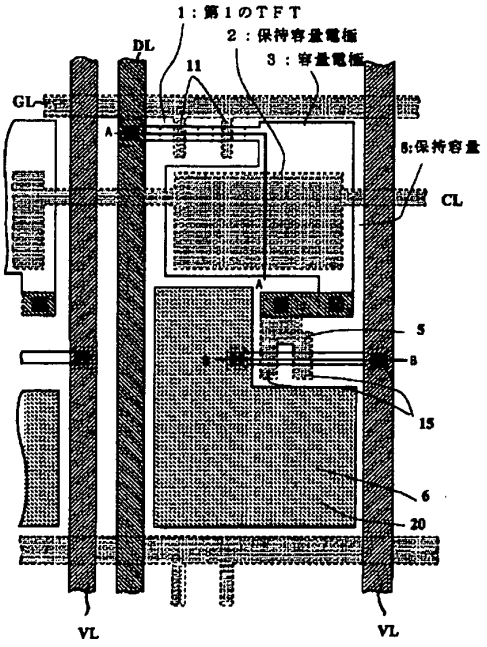
【図５】


２５：陰極
４：第２のＴＦＴ
６：陽極
２０：ＥＬ素子
１７
２４
２３
２２
２１
VL
C3
C2
BL
PLN：平坦化膜
10
７：ゲート絶縁膜
GL
１４：層間絶縁膜
１５：第２のゲート電極
１６：第２の能動層

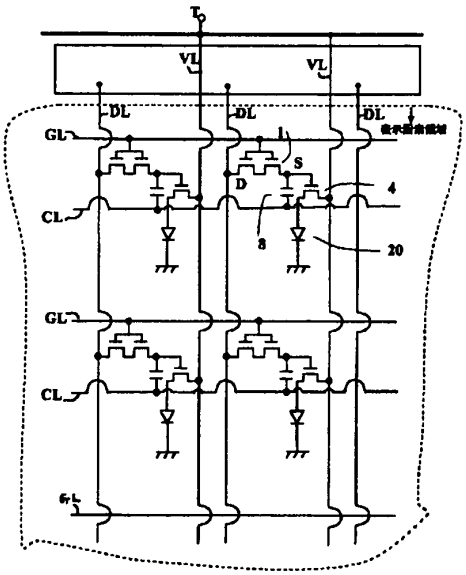
【図６】


２５：陰極
４：第２のＴＦＴ
６：陽極
２０：ＥＬ素子
２４
２３
２２
２１
１７
VL
C3
C2
BL
PLN：平坦化膜
10
７：ゲート絶縁膜
GL
１４：層間絶縁膜
１５：第２のゲート電極
１６：第２の能動層

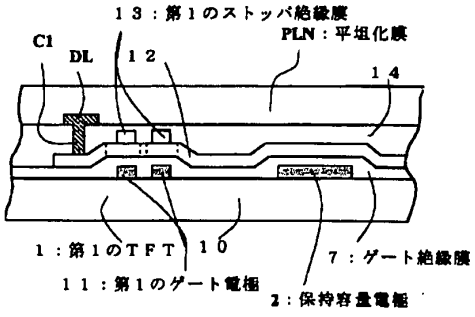
【図７】


１：第１のＴＦＴ
２：保持容量電極
３：容量電極
DL
11
GL
A
5:保持容量
CL
5
8
15
6
20
VL
VL

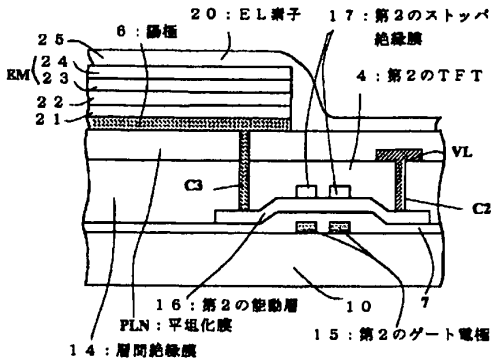
【図８】


VL
VL
DL
DL
DL
GL
S
D
4
CL
8
20
GL
CL

【図９】


１３：第１のストッパ絶縁膜
PLN：平坦化膜
C1
DL
１２
１４
１：第１のＴＦＴ
１０
７：ゲート絶縁膜
１１：第１のゲート電極
２：保持容量電極

【図１０】




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フロントページの続き

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5C094 AA04 AA10 AA13 AA15 AA24
AA53 AA55 BA03 BA29 CA19
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EA05 EA07 EB02 FA01 FA02
FB02 FB12 FB14 FB15 GA10
GB10

# PATENT ABSTRACTS OF JAPAN

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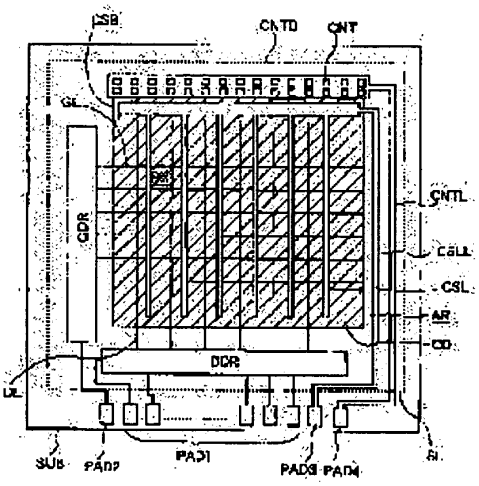
## (54) DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To enable a display device to perform display having high quality by improving power feeding structure to the electrode of one side constituting a pixel to prevent corrosion of the electrode.

SOLUTION: On the substrate of a display device which is constituted of a light emitting element having a first electrode layer which is driven by an active element, an organic light emitting layer which is applied on the first electrode layer and a second electrode layer CD which is formed on the organic light emitting layer, a second electrode connection electrode layer CNTB which is a layer lower than the second electrode layer CD and also is coated with a insulating or protective film is provided and the second electrode layer CD is connected to the second electrode connection electrode layer CNTB with a contact hole CNT.

図 1



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## CLAIMS

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[Claim(s)]
[Claim 1]It has a pixel for every intersection of two or more data lines which intersect two or more scanning lines by which the matrix arrayed was carried out into a viewing area on a substrate, and said two or more scanning lines, Equip said pixel with a current supply source line which supplies current for a display, and said pixel, An active element chosen with said scanning line, and a data holding element holding a data signal supplied from said data line by turn-on of this active element, And the 1st electrode layer that is provided with a light emitting device which emits light with current supplied from said current supply source line according to a data signal held at said data holding element, and drives said light emitting device by said active element, Comprise an organic luminous layer applied on said 1st electrode layer, and the 2nd electrode layer formed on said organic luminous layer, and from said 2nd electrode layer on said substrate in a lower layer. And a display having the 2nd connection electrode layer covered with an insulation or a protective film, and connecting said 2nd electrode layer to said 2nd connection electrode layer by a contact hole.
[Claim 2]The display comprising according to claim 1:
The 1st terminal pad that supplies a data signal to said data drive circuit from an external circuit at the outside of said viewing area of said substrate.
The 2nd terminal pad that supplies a scanning signal to said scan drive circuit.
The 3rd terminal pad that supplies current to said current supply source bus line.
The 4th terminal pad linked to said 2nd connection electrode layer.

[Claim 3]The display comprising according to claim 2:
A current supply source line leading-about line which connects to said 3rd terminal pad a current supply source line bus line which connects said current supply source line in common.
The 2nd electrode connection electrode leading-about line which connects said 2nd

connection electrode layer to said 4th pad.

[Claim 4]The display according to claim 1 or 2 providing said 1st [ the ] - the 4th terminal pad in one side of said substrate.
[Claim 5]The display according to claim 4 taking about in said neighborhood of 1 which carries out a current supply source wire-drawing time, and adjoins said one side of said substrate in a line and said 2nd electrode connection electrode leading-about line.
[Claim 6]The display according to claim 4 taking about to each of said both sides which carry out a current supply source wire-drawing time, and adjoin said neighborhood of 1 of said substrate in a line and said 2nd electrode connection electrode leading-about line.
[Claim 7]The display according to claim 1 or 2 providing said 3rd and 4th terminal pads in a neighborhood which provided said 1st and 2nd terminal pads of said substrate, and a neighborhood which counters.
[Claim 8]The display according to any one of claims 2 to 7 providing said 2nd connection electrode layer on said substrate outside said current supply source line bus line which connects said current supply source line in common.
[Claim 9]The display according to any one of claims 2 to 7 characterized by said thing [ that said 2nd connection electrode layer was connected to said current supply source line bus line ] which carried out the current supply source wire-drawing time, and provided outside a line on said substrate.

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[Translation done.]

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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]The pixel constituted from light emitting devices made to emit light by this invention's relating to an active matrix type display, especially sending current through luminous layers, such as an organic semiconductor film, such as EL (electroluminescence) element or an LED (light emitting diode) element, It is related with the display provided with the pixel circuit which controls the emission operating of this pixel.
[0002]
[Description of the Prior Art]In recent years, the demand of a personal computer, car navigation, Personal Digital Assistants, information-and-telecommunications apparatus, or these diversified products is growing with arrival of a highly informative society. The display device of a thin shape, a light weight, and low power consumption fits the displaying means of these products.
The display using electrooptics elements, such as a liquid crystal display or spontaneous light type EL element or LED, is used.

[0003]The display using a latter spontaneous light type electrooptics element has the features, like that visibility is good, having a large visual angle characteristic, and it is suitable for animation display by the high speed response, and it is thought that it is especially suitable for graphic display. progress of the network technology which makes possible rapid improvement and video communication of luminous efficiency has [ especially the display using the organic EL device (: called organic LED device -- it may call for short the following OLED) which makes an organic matter in recent years a luminous layer ] the high expectation for an OLED display conjointly. OLED has the diode structure which sandwiched the organic luminous layer by the electrode of two sheets.

[0004]In order to raise the power efficiency in the OLED display (display) constituted using such an OLED element, the active matrix driven which used the thin film transistor (it is also hereafter called TFT) as the switching element of a pixel is effective so that it may mention later. As art driven with active-matrix structure, an OLED display, For example, it writes in JP,4-328791,A, JP,8-241048,A, or a U.S. Pat. No. 5550066 specification, and is indicated by international Patent Gazette WO 98/No. 36407 etc. about driver voltage relations.
[0005]The typical pixel structure of an OLED display, the two thin film transistors TFT (the 1st TFT -- a switching transistor.) which are the 1st and the 2nd active element The 2nd TFT consists of a pixel driving circuit (henceforth a pixel circuit) which comprises a driver transistor and one capacitor (storage capacitance: data signal holding element), and controls the light emitting luminance of OLED by this pixel circuit. A pixel is arranged at each intersection which arranged the data line of M book with which a data signal (or picture signal) is supplied, and the scanning line (henceforth a gate line) of N book with which a scanning signal is supplied to the matrix of the N line xM sequence.
[0006]A sequential scanning signal (gating signal) is supplied to the gate line of N line at the drive of a pixel, a switching transistor is made into switch-on (turn-on), a vertical scan is finished once within the 1 frame period Tf, and turn-on voltage is again supplied to the first (1st line) gate line.
[0007]As for the time when turn-on voltage is supplied to one gate line, below Tf/N becomes in this drive system. Generally, 1 / about 60 seconds are used as a value of the 1 frame period Tf. When displaying one frame in the 2 fields, 1 field period is set to one half of 1 frame periods.
[0008]While turn-on voltage is supplied to a certain gate line, all the switching transistors connected to the data line will be in switch-on (ON state), and data voltage (picture voltage) is supplied to the data line of M sequence being simultaneous or one by one synchronizing with it. This is generally used with an active-matrix-liquid-crystal device.
[0009]Data voltage is turn-on voltage (turn-on is also only hereafter called one.) to a gate line. the same -- a turn-off -- only -- OFF -- calling -- while being supplied, it is stored in storage capacitance (capacitor) (held), and 1 frame period (or it is the same as that of 1 field period and the following) is mostly maintained at those values. The pressure value of storage capacitance specifies the gate voltage of a driver transistor.
[0010]Therefore, the current value which flows through a driver transistor is controlled, and luminescence of OLED is controlled. It is usual that it is 1 or less microsecond, and the response time until voltage is impressed to OLED and the luminescence starts can follow in footsteps of the early picture (video) of a motion. In order to supply current to a driver transistor, the current supply source line is formed and the current for a display according to the data signal held at storage capacitance is supplied from a current supply source line.

[0011]By the way, in the active matrix driven, that luminescence is performed over 1 frame period has realized the well head. As compared with the simple matrix driving which links the diode electrode of OLED with a scanning line and the data line directly, respectively, and drives it without providing TFT, the difference is clear.
[0012]In simple matrix driving, since current flows into OLED only in the period when the scanning line is chosen, in order to obtain luminosity equivalent to luminescence of 1 frame period only by luminescence of the short period, compared with an active matrix driven, one times the light emitting luminance of the abbreviated number of scanning lines is needed. Driver voltage and driving current must be enlarged inevitably, the loss of power consumption, such as generation of heat, becomes large, and power efficiency falls to it.
[0013]Thus, an active matrix driven is considered to be dominance from a viewpoint of reduction of power consumption compared with simple matrix driving.
[0014]
[Problem(s) to be Solved by the Invention]In the above-mentioned passive-matrix type display, the terminal pad for pulling out the scanning line and the data line which carried out crisscross arrangement to the viewing area on a substrate to the exterior of the viewing area concerned as it is, connecting with a drive circuit, and connecting a drive circuit with an external circuit is provided. However, it is difficult to apply such terminal composition to an active-matrix type display as it is.
[0015]Namely, in the OLED display of an active matrix driven. The current supply source to the capacitor for holding a display over 1 frame period, Connect one electrode of the capacitor concerned to the output terminal of a switching transistor, and the electrode of another side is connected to the common potential line for capacitors, or it has connected with the current supply source line which supplies current to OLED.
[0016]The block diagram and drawing 10 which explain typically the example of 1 composition of the conventional display in which drawing 9 used OLED are an explanatory view of the pixel configuration in drawing 9. Indicator AR which formed this display (image display device) on substrate SUB which consists of insulation materials, such as glass, by the matrix arrayed of two or more data-line DL and two or more gate lines GL, i.e., a scanning line, (among a figure) Data drive circuit DDR, scan drive circuit GDR, and current-supply circuit CSS are arranged around the inside enclosed with a dotted line, and it is constituted.
[0017]The shift register circuit, level shifter circuit which comprise the single channel type thin film transistor TFT of only the complementary circuit or N channel by the thin film transistor TFT of N channel type and P channel type, or P channel, [ DDR / data drive circuit ] It consists of analog switch circuits etc. Current-supply circuit CSS considers it only as a bus line, and it can be constituted also so that it may supply from an external power.
[0018]Drawing 9 is the method which formed the common potential line COML for capacitors in

indicator AR, and the electrode of said other end of a capacitor is connected to this common potential line COML. The common potential line COML is pulled out from the terminal COMT of the common-electric-potential supply bus line COMB by the external source of common electric potential. The method which did not form the common potential line COML but connected the capacitor to the current supply source line is also known.

[0019]The 1st thin film transistor TFT1 which is a switching transistor arranged to the field to which pixel PX was surrounded with data-line DL and the gate line GL as shown in drawing 10, the 2nd thin film transistor TFT2 which are driver transistors, the capacitor CPR, And it comprises the organic light emitting element OLED. The gate of thin film transistor TFT1 is connected to the gate line GL, and the drain is connected to data-line DL. The gate of thin film transistor TFT2 is connected to the sauce of thin film transistor TFT1, and one electrode (+ very) of the capacitor CPR is connected at this node.

[0020]Drawing 11 is a block diagram which illustrates further the composition of the display with the pixel configuration of drawing 10 of drawing 9. The drain of thin film transistor TFT2 is connected to current supply source line CSL, and sauce is connected to 1st electrode (here anode) AD of the organic light emitting element OLED. And the other end (- very) of the capacitor CPR is connected to the common potential line COML which branched from the common potential line bus line COMB. Data-line DL is driven by data drive circuit DDR, and the scanning line (gate line) GL is driven by scan drive circuit GDR. Current supply source line CSL is connected to the source of external current via current-supply circuit CSS or the terminal of drawing 8 via the current supply source bus line CSLB.

[0021]In drawing 10 and drawing 11, if one pixel PX is chosen with the scanning line GL and thin film transistor TFT1 carries out turn-on, the picture signal supplied from data-line DL will be accumulated in the capacitor CPR. And when thin film transistor TFT1 carries out a turn-off, thin film transistor TFT2 carries out turn-on, the current from current supply source line CSL flows into the organic light emitting element OLED, and this current continues over about 1 frame period. The current which flows at this time is prescribed by the signal charge accumulated in the capacitor CPR.

[0022]The operation level of the capacitor CPR is prescribed by the potential of the common potential line COML. Thereby, luminescence of a pixel is controlled. The current which flows out of the organic light emitting element OLED flows into the current drawing-out line which is not illustrated from negative pole CD.

[0023]In this method, since it is necessary to penetrate a part of picture element region, and to form the common potential line COML, the so-called decline in a numerical aperture will be brought about, and the improvement in a luminosity as the whole display will be controlled.

[0024]Drawing 12 is the same block diagram as drawing 11 which explains typically other examples of composition of the conventional display which used OLED. In this example,

although thin film transistor TFT1 which constitutes each pixel, TFT2, and the basic arrangement of the capacitor CPR are the same as that of drawing 9, it differs in that the other end of the capacitor CPR was connected to current supply source line CSL.

[0025]Namely, if one pixel PX is chosen with the scanning line GL and thin film transistor TFT1 carries out turn-on, When the picture signal supplied from data-line DL was accumulated in the capacitor CPR, thin film transistor TFT1 carried out the turn-off and thin film transistor TFT2 carries out turn-on, The current from current supply source line CSL flows into the organic light emitting element OLED, and this current continues over about 1 frame period (or 1 field period) like drawing 10. The current which flows at this time is prescribed by the signal charge accumulated in the capacitor CPR. The operation level of the capacitor CPR is prescribed by the potential of current supply source line CSL. Thereby, luminescence of a pixel is controlled.

[0026]In this kind explained by drawing 9 - drawing 12 of display, The source electrode of thin film transistor TFT2 used as 1st electrode (for example, it is also called anode and electrode layer of the following 1st) AD of the organic light emitting element OLED is formed with conductive thin films, such as ITO (indium tin oxide), and 1st electrode AD of each pixel PX is separated individually.

[0027]Since 2nd electrode (for example, it is also called negative pole and electrode layer of the following 2nd) CD that constitutes a light emitting device is located in the top layer of an element, it has a possibility that the open air may be touched on directly and corrosion may arise. Usually, the 2nd electrode layer is formed in the common poor film about all the pixels, and needs to take connection electrically with the exterior. When the drawer of the terminal for the current supply source to this 2nd electrode layer CD is directly carried out to the terminal area (terminal pad) of a substrate by extension of the 2nd electrode layer concerned, near [ that ] the terminal area, generating of corrosion takes place easily by contact with the open air.

[0028]Drawing 13 is a sectional view explaining the structure near 1 pixel of a display where the organic light emitting element was used. The polysilicon semiconductor layer PSI to which this display makes low temperature polysilicon suitable on glass substrate SUB, 1st insulating-layer IS1, gate wire [ which is scanning wiring ] (gate electrode) GL, and 2nd insulating-layer IS2, source electrode SD [ which was formed with aluminum wiring ], and 3rd insulating-layer IS3, the protective film PSV, 1st electrode layer AD, organic luminous layer OLE, and 2nd electrode layer CD are accumulated, and it is constituted.

[0029]If the polysilicon semiconductor layer PSI and the thin film transistor (this thin film transistor is a driver transistor) which comprises gate wire GL and source electrode SD are chosen, The organic light emitting element formed with 1st electrode layer AD, organic luminous layer OLE, and 2nd electrode layer CD linked to source electrode SD emits light, and the light L is emitted outside from the substrate SUB side.

[0030]If 2nd electrode layer CD of the pixel concerned has partial corrosion and degradation at this time, the current which flows from current supply source line CSL is not fully supplied, or the pixel concerned will be bypassed and it will flow, and luminescence becomes insufficient or light will be emitted at all. As a result, display failures, such as what is called a point defect and a field defect, are brought about.

[0031]The purpose of this invention improves the feed structure to the 2nd electrode layer that constitutes a pixel, prevents the corrosion of the 2nd electrode layer, and there is in providing the display which enabled the quality display.

[0032]

[Means for Solving the Problem]In order to attain the above-mentioned purpose, this invention formed the 2nd connection electrode layer on a substrate, connected the 2nd electrode layer to this 2nd connection electrode layer by a contact hole, and a leader of the 2nd electrode layer used it as lower layer wiring covered with a protective film on a substrate.

[0033]By having had this composition, corrosion of the negative pole is prevented and a display of high-reliability which enabled a quality display is provided. It is as follows when a more concrete example of composition of this invention is described. Namely, it has a pixel for every intersection of two or more data lines which intersect two or more scanning lines by which the matrix arrayed was carried out into a viewing area on (1) board, and said two or more scanning lines, Equip said pixel with a current supply source line which supplies current for a display, and said pixel, An active element chosen with said scanning line, and a data holding element holding a data signal supplied from said data line by turn-on of this active element, And the 1st electrode layer that is provided with a light emitting device which emits light with current supplied from said current supply source line according to a data signal held at said data holding element, and drives said light emitting device by said active element, Comprise an organic luminous layer applied on said 1st electrode layer, and the 2nd electrode layer formed on said organic luminous layer, and from said 2nd electrode layer on said substrate in a lower layer. And it has the 2nd connection electrode layer covered with an insulation or a protective film, and said 2nd electrode layer was connected to said 2nd connection electrode layer by a contact hole.

[0034]The 1st terminal pad that supplies a data signal to said data drive circuit from an external circuit in (2) and (1) at the outside of said viewing area of said substrate, It had the 2nd terminal pad that supplies a scanning signal to said scan drive circuit, the 3rd terminal pad that supplies current to said current supply source bus line, and the 4th terminal pad linked to said 2nd connection electrode layer.

[0035]In (3) and (2), it had the 2nd electrode connection electrode leading-about [ which connects a line and said 2nd connection electrode layer to said 4th pad by carrying out a current supply source wire-drawing time ] line which connects to said 3rd terminal pad a

current supply source line bus line which connects said current supply source line in common.
[0036]In (4), (1), or (2), said 1st [ the ] - the 4th terminal pad were provided in one side of said substrate.
[0037]In (5) and (4), it took about in a neighborhood of said 1 which adjoins said one side of said substrate in a line and said 2nd electrode connection electrode leading-about line by carrying out a current supply source wire-drawing time.
[0038]In (6) and (4), it took about to said each of both sides which adjoin said neighborhood of 1 of said substrate in a line and said 2nd electrode connection electrode leading-about line by carrying out a current supply source wire-drawing time.
[0039]In (7), (1), or (2), said 3rd and 4th terminal pads were provided in a neighborhood which provided said 1st and 2nd terminal pads of said substrate, and a neighborhood which counters.
[0040]It set they to be [ any of (8) and (2) - (7) ], and said 2nd connection electrode layer was provided on said substrate outside said current supply source line bus line which connects said current supply source line in common.
[0041]It set they to be [ any of (9) and (2) - (7) ], and said 2nd connection electrode layer was provided on said substrate outside said current supply source line leading-about line where it was connected to said current supply source line bus line.
[0042]It cannot be overemphasized that various change is possible without not limiting this invention to composition of the above-mentioned example constituted and mentioned later, and deviating from technical thought of this invention. Other purposes and composition of this invention will become clear from a statement of an embodiment mentioned later.
[0043]
[Embodiment of the Invention]Hereafter, with reference to the drawing of an example, it explains in detail about an embodiment of the invention. Although not illustrated, the organic luminous layer which it has in each pixel explained henceforth is the luminosity proportional to a current value, And there are a thing to which make light emit by the color (white is also included) depending on the organic materials, and monochrome or a colored presentation is made to perform, and a thing which makes a colored presentation perform to the organic layer of white light combining light filters, such as red, green, and blue.
[0044]Drawing 1 is a block diagram which illustrates typically the composition of the 1st example of the display by this invention. The display of this example has scan drive circuit GDR and data drive circuit DDR on glass substrate SUB.
[0045]And 1 pixel is formed in data-line DL driven by the scanning line GL driven by scan drive circuit GDR formed in the matrix (scanned), and data drive circuit DDR, and the field surrounded by current supply source line CSL. Terminal pad PAD1 for supplying the signal and voltage from an external circuit to scan drive circuit GDR and data drive circuit DDR and

PAD2 are formed in the neighborhood of one of substrate SUB.

[0046]Drawing 2 is a lineblock diagram of the 1-pixel pixel circuit in drawing 1. 1 pixel of outline composition of this example is formed in the field surrounded by data-line DL (m+1), the scanning line GL (n+1), GL (n), and current supply source line CSL. Here, the scanning line scanned now (chosen) is explained as GL (n+1).

[0047]Its attention is paid to pixel PX among two or more pixels chosen with the scanning line GL (n+1). A switching transistor and thin film transistor TFTof ** 2nd2 are driver transistors thin film transistor TFTof ** 1st which is active element1. The 1st gate of thin film transistor TFT1 is connected to the scanning line GL (n+1), the drain is connected to data-line DL (m+1), and sauce is connected to the gate of 2nd thin film transistor TFT2.

[0048]The 2nd drain of thin film transistor TFT2 is connected to current supply source line CSL to which current is supplied from current supply source line bus-line CSB shown in drawing 1. And the sauce is connected to 1st electrode layer AD of OLED24. One terminal of the capacitor CPR as a data signal holding element is connected with the 1st sauce of thin film transistor TFT1 at the node of the 2nd gate of thin film transistor TFT2, and the terminal of another side is connected to the last scanning line GL (n).

[0049]In 1 pixel of circuitry shown in drawing 2, one terminal of the capacitor CPR connected with the 1st sauce of thin film transistor TFT1 at the node of the 2nd gate of thin film transistor TFT2 is + pole, and the terminal of another side connected to the scanning line GL (n) is - pole.

[0050]The organic light emitting element OLED is the composition which sandwiched the organic luminous layer (not shown) between 1st electrode layer AD and 2nd electrode layer CD, 1st electrode layer AD was connected to the 2nd source electrode of thin film transistor TFT2, and 2nd electrode layer CD was poor-formed over all the pixels, and is connected to the 2nd connection electrode layer CNTB of drawing 1.

[0051]This 2nd connection electrode layer CNTB is what is called current drawing-out wiring (electrode), It is formed in the lower layer of a substrate at said terminal pad PAD1, PAD2, and a same layer, 2nd electrode layer CD is connected in the contact hole CNT, and it is connected to terminal PAD4 formed in said terminal pad PAD1, PAD2, and a same layer with the 2nd electrode connection electrode leading-about line CNTL.

[0052]It is connected to terminal PAD3 which carried out the current supply source wire-drawing time also of the current supply source line CSL which is wiring of the 1st electrode layer to current supply source line bus-line CSB, and was formed in said terminal pad PAD1, PAD2, and a same layer with the line CSLL. The 2nd connection electrode layer CNTB of the above is arranged rather than current supply source line bus-line CSB the outside of a substrate, and inside sealing region SL of the substrate shown by the dotted line.

[0053]Thus, the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in

the contact hole CNT rather than current supply source line bus-line CSB on the outside of substrate SUB. And the layout on the substrate in the method which connects with an external circuit via a flexible printed circuit board by having arranged inside a seal area at one side becomes easy.

[0054]It is written in KONDESA CPR by the 1st turn-on of thin film transistor TFT1, As charge quantity. The held data signal the current from current supply source line CSL as a current amount controlled by charge quantity (the gradation of a data signal is shown) held at the capacitor CPR concerned by the 2nd [ accompanying the 1st turn-off of thin film transistor TFT1 ] turn-on of thin film transistor TFT2. It passes to organic light emitting element OLE.

[0055]The organic light emitting element OLED emits light by the color depending on the material of organic luminous layer OLE which is the luminosity mostly proportional to the current amount supplied, and constitutes the organic light emitting element concerned. In the case of a colored presentation, organic luminous layer material is usually changed for every red and green and blue pixel, or it uses the combination of a white organic luminous layer material and the light filter of each color.

[0056]Analog quantity or the digital variable of time sharing may be sufficient as how to give a data signal. Gradation control may combine red and the area gradation system which divided the area of each green and blue pixel.

[0057]In this example, current supply source line bus-line CSB, The current which flows out of 2nd electrode layer CD after the emission operating of each pixel circuit. It constitutes from the 2nd connection electrode layer CNTB that is the current drawing-out wiring which was formed in the lower layer of a substrate, and which was formed [ all the / pixel ] so that it may be made to flow out of terminal pad PAD4 into an external circuit with the 2nd electrode connection electrode leading-about line CNTL.

[0058]Therefore, in this example, 2nd electrode layer CD common to all the pixels poor-formed in the upper layer is connected to the 2nd connection electrode layer CNTB in the contact hole CNT. The 2nd electrode connection electrode leading-about line CNTL is formed in the 2nd connection electrode layer CNTB and a same layer.

[0059]Usually, in this kind of display, in order to secure reliability, the sealing structure which used the can etc. is adopted. The seal area for pasting up this closure canning is established in substrate SUB. The 2nd above-mentioned connection electrode layer CNTB and the 2nd electrode connection electrode leading-about line CNTL are formed inside this seal area. And the 2nd above-mentioned connection electrode layer CNTB is arranged on the outside of current supply source line bus-line CSB at least.

[0060]Since the 2nd connection electrode layer CNTB of the above is formed in the lower layer of a substrate and an insulating layer and a protective film are laminated on it, The 2nd electrode and since contact with the open air also including the 2nd electrode connection

electrode leading-about line is lost preferably and the corrosion is prevented the 2nd connection electrode layer, reliability can improve and the display which enabled the quality display can be provided. Although one may be sufficient as the number of the above-mentioned contact hole, since the provided direction can stabilize for it and send more current, it has been provided by this example. [ two or more ]

[0061]The mimetic diagram near [ where drawing 3 explains the luminescence mechanism of the display by this invention ] 1 pixel, and drawing 4 are the mimetic diagrams explaining the connection section of the 2nd electrode layer and the 2nd connection electrode layer. The same reference mark as drawing 1 corresponds to identical parts. The arrow shown with the reference mark I in a figure shows the course of the current which contributes to luminescence.

[0062]Thin film transistor TFT2 is a driver transistor. When this thin film transistor TFT2 is chosen with the gate line GL, from the current supply source line which branched from the current supply source line bus line. The current I of the current value of the gradation according to the data signal held at the capacitor is supplied to 1st electrode layer AD of the organic light emitting element OLED through the thin film transistor TFT2 concerned.

[0063]The electron from 2nd electrode layer CD and the hole from 1st electrode layer AD recombine the organic light emitting element OLED within the organic luminous layer OLE, and it emits light in the light L of a spectrum according to the material property of the organic luminous layer OLE concerned. Although 1st electrode layer AD is independent for every pixel, 2nd electrode layer CD is formed in the shape of a poor film about all the pixels. The current I which passed along the organic light emitting element OLED from thin film transistor TFT2 flows out of the 2nd electrode connection electrode leading-about line CNTL of drawing 1 into terminal pad PAD4 through the 2nd connection electrode layer CNTB shown in drawing 4 from 2nd electrode layer CD. The matrix arrayed of a majority of such pixels is carried out, and a two-dimensional display is constituted.

[0064]Drawing 5 is a block diagram which illustrates typically the composition of the 2nd example of the display by this invention. The same reference mark as drawing 1 corresponds to the same functional division. Two terminal pad PAD3 of current supply source line bus-line CSB and PAD3' which connect current supply source line CSL in this example, And terminal pad PAD4 of the 2nd connection electrode layer CNTB was provided in the neighborhood of 1 of the substrate with which terminal pad PAD1 of a data drive circuit and terminal pad PAD2 of scan drive circuit GDR are arranged, and the neighborhood of the opposite hand.

[0065]The layout on a substrate becomes easy by being the outside of substrate SUB and having arranged the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in the contact hole CNT inside a seal area rather than current supply source line bus-line CSB, also by this example.

[0066]The current supply source line leading-about line CSLL taken about like this example to current supply source line bus-line CSB to the terminal pad PAD3, and PAD3'. And since the leading-about length on the substrate of the 2nd electrode connection electrode leading-about line CNTL which connects between terminal pad PAD4 with the 2nd connection electrode layer CNTB becomes short, a more uniform current supply source and current drawing out become possible. The emission distribution in a viewing area becomes uniform by this, and a more nearly quality display is obtained. It may be either, although a current supply source wire-drawing time is carried out and the line CSLL is made into two. As shown in drawing 5, a current supply source wire-drawing time is carried out, and when current supply source line bus-line CSB reaches on the other hand, and the drawer of the line CSLL is carried out from another side, respectively and it is made into two, it is effective in symmetry becoming good.
[0067]By this example, the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in the contact hole CNT rather than current supply source line bus-line CSB on the outside of substrate SUB. And the layout on the substrate in the method which connects with an external circuit by two sides which counter via a flexible printed circuit board by having arranged inside a seal area becomes easy.
[0068]By having had composition of this example, since a circuit pattern [ / near the seal area ] decreases, the shelter of the UV light at the time of carrying out UV curing of the sealing material can decrease, and the sealing material concerned can be stiffened effectively. Positive closure is attained by this and the reliability of a display can be improved further.
[0069]Drawing 6 is a block diagram which illustrates typically the composition of the 3rd example of the display by this invention. The same reference mark as drawing 1 corresponds to the same functional division. In this example. Pad PAD3 of current supply source line bus-line CSB and terminal pad PAD4 of the 2nd connection electrode layer CNTB which connect current supply source line CSL were distributed and provided in the both ends of the neighborhood of 1 of the substrate with which terminal pad PAD1 of a data drive circuit and terminal pad PAD2 of scan drive circuit GDR are arranged.
[0070]Like said 1st [ the ] - the 2nd example, rather than current supply source line bus-line CSB, it is the outside of substrate SUB and the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in the contact hole CNT has been arranged inside a seal area. Since other composition is the same as that of drawing 1, repeated explanation is omitted.
[0071]Also by this example, the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in the contact hole CNT rather than current supply source line bus-line CSB on the outside of substrate SUB. And the layout on the substrate in the method which connects with an external circuit via a flexible printed circuit board by having arranged inside a seal area at one side becomes easy.

[0072]Drawing 7 is a block diagram which illustrates typically the composition of the 4th example of the display by this invention. The same reference mark as drawing 1 corresponds to the same functional division. In this example. Pad PAD3 of current supply source line bus-line CSB and terminal pad PAD4 of the 2nd connection electrode layer CNTB which connect current supply source line CSL were provided in the neighborhood of 1 of the substrate with which terminal pad PAD1 of a data drive circuit and terminal pad PAD2 of scan drive circuit GDR are arranged, and the neighborhood of the opposite hand.

[0073]Like said 1st [ the ] - the 3rd example, rather than current supply source line bus-line CSB, it is the outside of substrate SUB and the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in the contact hole CNT has been arranged inside a seal area.

[0074]Also by this example, the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in the contact hole CNT rather than current supply source line bus-line CSB on the outside of substrate SUB. And the layout on the substrate in the method which connects with an external circuit by two sides which counter via a flexible printed circuit board by having arranged inside a seal area becomes easy. Since other composition is the same as that of drawing 6, repeated explanation is omitted.

[0075]The current supply source line leading-about line CSLL taken about from current supply source line bus-line CSB to the terminal pad PAD3 like this example. And since the leading-about length on the substrate of the 2nd electrode connection electrode leading-about line CNTL which connects between terminal pad PAD4 with the 2nd connection electrode layer CNTB becomes short, a more uniform current supply source and current drawing out become possible. The emission distribution in a viewing area becomes uniform by this, and a more nearly quality display is obtained.

[0076]By having had composition of this example, since a circuit pattern [ / near the seal area ] decreases, the shelter of the UV light at the time of carrying out UV curing of the sealing material can decrease, and the sealing material concerned can be stiffened effectively. Positive closure is attained by this and the reliability of a display can be improved further.

[0077]In the 2nd explained above - the 4th example, a current supply source wire-drawing time is carried out, and the line CSLL and the 2nd electrode connection electrode leading-about line CNTL can form wiring of respectively sufficient thickness for the large field on a substrate which is a current path, and can secure a stable current path. Especially, like the 2nd example and the 4th example, when the distance between pads is short, a more stable current path can be secured.

[0078]Drawing 8 is a block diagram which illustrates typically the composition of the 5th example of the display by this invention. The same reference mark as drawing 1 corresponds to the same functional division. In this example, on the substrate, the neighborhood which has

arranged terminal PAD 1-4 was adjoined, and the 2nd connection electrode layer CNTB was formed with said gate scan drive circuit GDR the neighborhood of an opposite hand, and outside said current supply source line leading-about line CSLL.

[0079]By this example, the 2nd connection electrode layer CNTB that connects 2nd electrode layer CD in the contact hole CNT from the current supply source line leading-about line CSLL which takes about current supply source line bus-line CSB to terminal pad PAD3 on the outside of substrate SUB. And by having arranged inside a seal area, it becomes gate scan drive circuit GDR and a layout of symmetrical arrangement, and can be considered as the arrangement which balance was able to take as a whole. Since other composition is the same as that of drawing 1, repeated explanation is omitted.

[0080]Like this example, since the leading-about length on the substrate of terminal pad PAD4 and the 2nd electrode connection electrode leading-about line CNTL becomes short, a more uniform current supply source and current drawing out become possible. The emission distribution in a viewing area becomes uniform by this, and a more nearly quality display is obtained.

[0081]Although each of above-mentioned examples can make each of the 1st electrode layer and the 2nd electrode layer correspond to catholyte and a positive electrode layer, this invention is applicable similarly to the structure which replaced these. This invention is not restricted to the display using the above-mentioned OLED, and can be applied like other displays which display by the same emission operating as OLED.

[0082]

[Effect of the Invention]As explained above, according to this invention, since corrosion the electrode layer which constitutes the pixel of a display, and near [ its ] the terminal is prevented, there is no generating of display failure. Current can stably and fully be supplied through a current supply source line, and the display which enabled the quality display can be provided.

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[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram which illustrates typically the composition of the 1st example of the display by this invention.
[Drawing 2]It is a lineblock diagram of the 1-pixel pixel circuit in drawing 1.
[Drawing 3]It is a mimetic diagram explaining the luminescence mechanism of the display by this invention near 1 pixel.
[Drawing 4]It is a mimetic diagram explaining the connection section of the 2nd electrode layer of a display and the 2nd connection electrode layer by this invention.
[Drawing 5]It is a block diagram which illustrates typically the composition of the 2nd example of the display by this invention.
[Drawing 6]It is a block diagram which illustrates typically the composition of the 3rd example of the display by this invention.
[Drawing 7]It is a block diagram which illustrates typically the composition of the 4th example of the display by this invention.
[Drawing 8]It is a block diagram which illustrates typically the composition of the 5th example of the display by this invention.
[Drawing 9]It is a block diagram explaining the example of composition of the conventional display using an organic light emitting element.
[Drawing 10]It is an explanatory view of the pixel configuration in drawing 9.
[Drawing 11]It is a block diagram which illustrates further the composition of the display with the pixel configuration of drawing 10 of drawing 9.
[Drawing 12]It is the same block diagram as drawing 11 which explains typically other examples of composition of the conventional display using an organic light emitting element.
[Drawing 13]It is a sectional view explaining the structure near 1 pixel of the display using an organic light emitting element.

[Description of Notations]
SUB Substrate
GL gate line (scanning line)
DL data line
CSL Current supply source line
CSB Current supply source line bus line
CSLL A current supply source wire-drawing time is carried out, and it is a line.
CD Negative pole
CDT Contact hole
CNTB Negative pole connection electrode layer
CNTL Negative pole bonding electrode leading-about line
AD Anode
OLE Organic luminous layer
OLED Organic light emitting element.

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[Translation done.]

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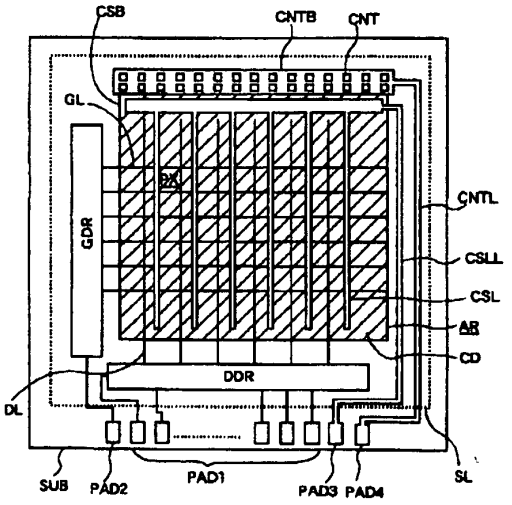
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(54)【発明の名称】　表示装置

(57)【要約】
【課題】画素を構成する一方の電極への給電構造を改良して当該電極の腐食を防止し、高品質の表示を可能とする。
【解決手段】アクティブ素子で駆動される第１の電極層と、この第１の電極層上に塗布された有機発光層および有機発光層上に形成された第２の電極層ＣＤを有する発光素子で構成した表示装置の基板ＳＵＢ上に、上記第２の電極層ＣＤより下層で、かつ絶縁や保護膜で被覆された第２電極接続電極層ＣＮＴＢを設け、第２の電極層ＣＤをコンタクトホールＣＮＴで第２電極接続電極層ＣＮＴＢに接続した。

図１



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【特許請求の範囲】

【請求項１】基板上の表示領域内にマトリクス配列された複数の走査線と前記複数の走査線に交差する複数のデータ線の交差部毎に画素を有し、前記画素に表示のための電流を供給する電流供給線を備え、

前記画素は、前記走査線で選択されるアクティブ素子と、このアクティブ素子のターンオンで前記データ線から供給されるデータ信号を保持するデータ保持素子、および前記データ保持素子に保持されたデータ信号にしたがって前記電流供給線から供給される電流で発光する発光素子とを備え、

前記発光素子は前記アクティブ素子で駆動される第１の電極層と、前記第１の電極層上に塗布された有機発光層と、前記有機発光層上に形成された第２の電極層で構成され、

前記基板上に前記第２の電極層より下層で、かつ絶縁もしくは保護膜で被覆された第２電極接続電極層を有し、前記第２の電極層をコンタクトホールにより前記第２電極接続電極層に接続したことを特徴とする表示装置。

【請求項２】前記基板の前記表示領域の外側に、外部回路から前記データ駆動回路にデータ信号を供給する第１の端子パッドと、前記走査駆動回路に走査信号を供給する第２の端子パッドと、前記電流供給バスラインに電流を供給する第３の端子パッドと、前記第２電極接続電極層に接続する第４の端子パッドを備えたことを特徴とする請求項１に記載の表示装置。

【請求項３】前記電流供給線を共通に接続する電流供給線バスラインを前記第３の端子パッドに接続する電流供給線引回しラインと、

前記第２電極接続電極層を前記第４のパッドに接続する第２電極接続電極引き回しラインとを有することを特徴とする請求項２に記載の表示装置。

【請求項４】前記第１～第４の端子パッドを前記基板の１辺に設けたことを特徴とする請求項１または２に記載の表示装置。

【請求項５】前記電流供給線引回しラインと前記第２電極接続電極引き回しラインを前記基板の前記１辺に隣接する一の辺に引回したことを特徴とする請求項４に記載の表示装置。

【請求項６】前記電流供給線引回しラインと前記第２電極接続電極引き回しラインとを前記基板の前記一の辺に隣接する両辺のそれぞれに引回したことを特徴とする請求項４に記載の表示装置。

【請求項７】前記第３および第４の端子パッドを前記基板の前記第１および第２の端子パッドを設けた辺と対向する辺に設けたことを特徴とする請求項１または２に記載の表示装置。

【請求項８】前記基板上で、前記第２電極接続電極層を前記電流供給線を共通に接続する前記電流供給線バスラインよりも外側に設けたことを特徴とする請求項２～７

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の何れかに記載の表示装置。

【請求項９】前記基板上で、前記第２電極接続電極層を前記電流供給線バスラインに接続された前記電流供給線引回しラインよりも外側に設けたことを特徴とする請求項２～７の何れかに記載の表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、アクティブ・マトリクス型表示装置に係り、特に有機半導体膜などの発光層に電流を流すことによって発光させるＥＬ（エレクトロルミネッセンス）素子またはＬＥＤ（発光ダイオード）素子等の発光素子で構成した画素と、この画素の発光動作を制御する画素回路を備えた表示装置に関する。

【０００２】

【従来の技術】近年、高度情報化社会の到来に伴い、パーソナルコンピュータ、カーナビ、携帯情報端末、情報通信機器あるいはこれらの複合製品の需要が増大している。これらの製品の表示手段には、薄型、軽量、低消費電力のディスプレイデバイスが適しており、液晶表示装置あるいは自発光型のＥＬ素子またはＬＥＤなどの電気光学素子を用いた表示装置が用いられている。

【０００３】後者の自発光型の電気光学素子を用いた表示装置は、視認性がよいこと、広い視角特性を有すること、高速応答で動画表示に適していることなどの特徴があり、映像表示には特に好適と考えられている。特に、近年の有機物を発光層とする有機ＥＬ素子（有機ＬＥＤ素子とも言う：以下ＯＬＥＤと略称する場合もある）を用いたディスプレイは発光効率の急速な向上と映像通信を可能にするネットワーク技術の進展とが相まって、ＯＬＥＤディスプレイへの期待が高い。ＯＬＥＤは有機発光層を２枚の電極で挟んだダイオード構造を有する。

【０００４】このようなＯＬＥＤ素子を用いて構成したＯＬＥＤディスプレイ（表示装置）における電力効率を高めるためには、後述するように、薄膜トランジスタ（以下、ＴＦＴとも称する）を画素のスイッチング素子としたアクティブ・マトリクス駆動が有効である。ＯＬＥＤディスプレイをアクティブ・マトリクス構造で駆動する技術としては、例えば、特開平４－３２８７９１号公報、特開平８－２４１０４８号公報、あるいは米国特許第５５５００６６号明細書などに記載されており、また、駆動電圧関係については国際特許公報ＷＯ９８／３６４０７号などに開示されている。

【０００５】ＯＬＥＤディスプレイの典型的な画素構造は、第１と第２のアクティブ素子である２つの薄膜トランジスタＴＦＴ（第１のＴＦＴはスイッチングトランジスタ、第２のＴＦＴはドライバトランジスタ）と１つのコンデンサ（蓄積容量：データ信号保持素子）で構成される画素駆動回路（以下、画素回路とも言う）からなり、この画素回路によりＯＬＥＤの発光輝度を制御する。画素はデータ信号（または、画像信号）が供給され

るＭ本のデータ線と、走査信号が供給されるＮ本の走査線（以下、ゲート線とも言う）をＮ行×Ｍ列のマトリクスに配列した各交差部に配置される。

【０００６】画素の駆動には、Ｎ行のゲート線に順次走査信号（ゲート信号）を供給してスイッチングトランジスタを導通状態に（ターンオン）し、１フレーム期間Ｔｆ内に垂直方向の走査を１回終えて、再び最初（１行目）のゲート線にターンオン電圧を供給する。

【０００７】この駆動方式では、１本のゲート線にターンオン電圧が供給される時間はＴｆ／Ｎ以下となる。一般的には、１フレーム期間Ｔｆの値としては１／６０秒程度が用いられる。なお、１フレームを２フィールドで表示する場合は、１フィールド期間は１フレーム期間の１／２となる。

【０００８】あるゲート線にターンオン電圧が供給されている間は、そのデータ線に接続されたスイッチングトランジスタは全て導通状態（オン状態）となり、それに同期してＭ列のデータ線に同時にまたは順次にデータ電圧（画像電圧）が供給される。これはアクティブ・マトリクス液晶装置で一般的に用いられているものである。

【０００９】データ電圧はゲート線にターンオン電圧（以下、ターンオンを単にオンとも称する。同様に、ターンオフも単にオフとも称する）が供給されている間に蓄積容量（コンデンサ）に蓄えられ（保持され）、１フレーム期間（もしくは、１フィールド期間、以下同様）はほぼそれらの値に保たれる。蓄積容量の電圧値は、ドライバトランジスタのゲート電圧を規定する。

【００１０】したがって、ドライバトランジスタを流れる電流値が制御されてＯＬＥＤの発光が制御される。ＯＬＥＤに電圧が印加されて、その発光が始まるまでの応答時間は１μｓ以下であることが通常であり、動きの早い画像（動画像）にも追随できる。ドライバトランジスタに電流を供給するために、電流供給線が設けられており、蓄積容量に保持されたデータ信号に応じた表示用の電流が電流供給線から供給される。

【００１１】ところで、アクティブ・マトリクス駆動では、１フレーム期間にわたって発光が行われることで高効率を実現している。ＴＦＴを設けずに、ＯＬＥＤのダイオード電極をそれぞれ走査線、データ線に直結して駆動する単純マトリクス駆動と比較すると、その差異は明確である。

【００１２】単純マトリクス駆動では、走査線が選択されている期間にのみＯＬＥＤに電流が流れるので、その短い期間の発光のみで１フレーム期間の発光と同等の輝度を得るためには、アクティブ・マトリクス駆動に比べて略走査線数倍の発光輝度が必要となる。それには、必然的に駆動電圧、駆動電流を大きくしなければならず、発熱などの消費電力の損失が大きくなって電力効率が低下する。

【００１３】このように、アクティブ・マトリクス駆動は、単純マトリクス駆動に比べて消費電力の低減の観点から優位であると考えられる。

【００１４】

【発明が解決しようとする課題】上記した単純マトリクス型の表示装置では、基板上の表示領域に交差配置した走査線とデータ線をそのまま当該表示領域の外部に引き出して駆動回路に接続し、駆動回路を外部回路と接続するための端子パッドを設けている。しかし、このような端子構成をアクティブ・マトリクス型の表示装置にそのまま適用することは困難である。

【００１５】すなわち、アクティブ・マトリクス駆動のＯＬＥＤ表示装置では、１フレーム期間にわたって表示を保持するためのコンデンサへの電流供給を、当該コンデンサの一方の電極をスイッチングトランジスタの出力端子に接続し、他方の電極をコンデンサ用の共通電位線に接続したり、あるいはＯＬＥＤに電流を供給する電流供給線に接続している。

【００１６】図９はＯＬＥＤを用いた従来の表示装置の１構成例を模式的に説明するブロック図、図１０は図９における画素構成の説明図である。この表示装置（画像表示装置）は、ガラス等の絶縁材からなる基板ＳＵＢ上に複数のデータ線ＤＬと複数のゲート線すなわち走査線ＧＬとのマトリクス配列で形成した表示部ＡＲ（図中、点線で囲った内部）の周囲にデータ駆動回路ＤＤＲ、走査駆動回路ＧＤＲ、電流供給回路ＣＳＳを配置して構成されている。

【００１７】データ駆動回路ＤＤＲはＮチャンネル型とＰチャンネル型の薄膜トランジスタＴＦＴによる相補型回路またはＮチャンネルのみかＰチャンネルのみの単チャンネル型の薄膜トランジスタＴＦＴで構成されるシフトレジスタ回路、レベルシフタ回路、アナログスィッチ回路などからなる。なお、電流供給回路ＣＳＳはバスラインのみとし、外部電源から供給するようにも構成できる。

【００１８】図９は表示部ＡＲにコンデンサ用の共通電位線ＣＯＭＬを設けた方式であり、コンデンサの前記他端の電極は、この共通電位線ＣＯＭＬに接続される。共通電位線ＣＯＭＬは共通電位供給バスラインＣＯＭＢの端子ＣＯＭＴから外部の共通電位源に引き出されている。なお、共通電位線ＣＯＭＬを設けず、コンデンサを電流供給線に接続した方式も既知である。

【００１９】図１０に示したように、画素ＰＸはデータ線ＤＬとゲート線ＧＬで囲まれた領域に配置されたスイッチングトランジスタである第１の薄膜トランジスタＴＦＴ１、ドライバトランジスタである第２の薄膜トランジスタＴＦＴ２、コンデンサＣＰＲ、および有機発光素子ＯＬＥＤで構成される。薄膜トランジスタＴＦＴ１のゲートはゲート線ＧＬに、ドレインはデータ線ＤＬに接続されている。薄膜トランジスタＴＦＴ２のゲートは薄膜トランジスタＴＦＴ１のソースに接続され、この接続

点にコンデンサＣＰＲの一方の電極（＋極）が接続されている。

【００２０】図１１は図１０の画素構成をもつ図９の表示装置の構成をさらに説明するブロック図である。薄膜トランジスタＴＦＴ２のドレインは電流供給線ＣＳＬに、ソースは有機発光素子ＯＬＥＤの第１の電極（ここでは陽極）ＡＤに接続されている。そして、コンデンサＣＰＲの他端（－極）は共通電位線バスラインＣＯＭＢから分岐した共通電位線ＣＯＭＬに接続されている。データ線ＤＬはデータ駆動回路ＤＤＲで駆動され、走査線（ゲート線）ＧＬは走査駆動回路ＧＤＲで駆動される。また、電流供給線ＣＳＬは電流供給バスラインＣＳＬＢを介して図８の電流供給回路ＣＳＳあるいは端子を介して外部電流源に接続している。

【００２１】図１０と図１１において、１つの画素ＰＸが走査線ＧＬで選択されて薄膜トランジスタＴＦＴ１がターンオンすると、データ線ＤＬから供給される画像信号がコンデンサＣＰＲに蓄積される。そして、薄膜トランジスタＴＦＴ１がターンオフした時点で薄膜トランジスタＴＦＴ２がターンオンし、電流供給線ＣＳＬからの電流が有機発光素子ＯＬＥＤに流れ、ほぼ１フレーム期間にわたってこの電流が持続する。このとき流れる電流はコンデンサＣＰＲに蓄積されている信号電荷で規定される。

【００２２】コンデンサＣＰＲの動作レベルは共通電位線ＣＯＭＬの電位で規定される。これにより、画素の発光が制御される。有機発光素子ＯＬＥＤから流れ出る電流は陰極ＣＤから図示しない電流引抜き線に流れる。

【００２３】この方式では、画素領域の一部を貫通して共通電位線ＣＯＭＬを設ける必要があるため、所謂開口率の低下をもたらし、表示装置全体としての明るさ向上を抑制してしまう。

【００２４】図１２はＯＬＥＤを用いた従来の表示装置の他の構成例を模式的に説明する図１１と同様のブロック図である。この例では、各画素を構成する薄膜トランジスタＴＦＴ１、ＴＦＴ２およびコンデンサＣＰＲの基本配列は図９と同様であるが、コンデンサＣＰＲの他端を電流供給線ＣＳＬに接続した点で異なる。

【００２５】すなわち、１つの画素ＰＸが走査線ＧＬで選択されて薄膜トランジスタＴＦＴ１がターンオンすると、データ線ＤＬから供給される画像信号がコンデンサＣＰＲに蓄積され、薄膜トランジスタＴＦＴ１がターンオフした時点で薄膜トランジスタＴＦＴ２がターンオンしたとき、電流供給線ＣＳＬからの電流が有機発光素子ＯＬＥＤに流れ、図１０と同様に、ほぼ１フレーム期間（または、１フィールド期間）にわたってこの電流が持続する。このとき流れる電流はコンデンサＣＰＲに蓄積されている信号電荷で規定される。コンデンサＣＰＲの動作レベルは電流供給線ＣＳＬの電位で規定される。これにより、画素の発光が制御される。



【００２６】図９～図１２で説明したこの種の表示装置においては、有機発光素子ＯＬＥＤの第１の電極（例えば陽極、以下第１の電極層とも称する）ＡＤとなる薄膜トランジスタＴＦＴ２のソース電極はＩＴＯ（インジウム・チン・オキサイド）等の導電性薄膜で形成され、かつ各画素ＰＸの第１の電極ＡＤは個別に分離されている。

【００２７】また、発光素子を構成する第２の電極（例えば陰極、以下第２の電極層とも称する）ＣＤは素子の最上層に位置するため、直接外気に触れて腐食が生じる恐れがある。通常、第２の電極層は全画素について共通のべた膜に形成されており、外部と電気的に接続をとる必要がある。この第２の電極層ＣＤへの電流供給のための端子は当該第２の電極層の延長で基板の端子部（端子パッド）に直接引き出した場合は、その端子部近傍では外気との接触で腐食の発生が起こり易い。

【００２８】図１３は有機発光素子を用いた表示装置の１画素付近の構造を説明する断面図である。この表示装置は、ガラス基板ＳＵＢの上に低温ポリシリコンを好適とするポリシリコン半導体層ＰＳＩ、第１の絶縁層ＩＳ１、走査配線であるゲート配線（ゲート電極）ＧＬ、第２の絶縁層ＩＳ２、アルミニウム配線で形成したソース電極ＳＤ，第３の絶縁層ＩＳ３、保護膜ＰＳＶ、第１の電極層ＡＤ、有機発光層ＯＬＥ、第２の電極層ＣＤを積み上げて構成される。

【００２９】ポリシリコン半導体層ＰＳＩとゲート配線ＧＬ、ソース電極ＳＤで構成される薄膜トランジスタ（この薄膜トランジスタはドライバトランジスタ）が選択されると、ソース電極ＳＤに接続した第１の電極層ＡＤと有機発光層ＯＬＥおよび第２の電極層ＣＤで形成される有機発光素子が発光し、その光Ｌが基板ＳＵＢ側から外部に出射する。

【００３０】このとき、当該画素の第２の電極層ＣＤに部分的な腐食や劣化があると、電流供給線ＣＳＬから流れる電流が充分に供給されず、あるいは当該画素を迂回して流れ、発光が不十分になったり全く発光しないことになる。その結果、所謂点欠陥、領域欠陥等の表示不良をもたらす。

【００３１】本発明の目的は、画素を構成する第２の電極層への給電構造を改良して第２の電極層の腐食を防止し、高品質の表示を可能とした表示装置を提供することにある。

【００３２】

【課題を解決するための手段】上記目的を達成するため、本発明は、基板上に、第２電極接続電極層を形成し、この第２電極接続電極層にコンタクトホールにより第２の電極層を接続して、第２の電極層の引出し線が基板上で保護膜により被覆された下層配線とした。

【００３３】この構成としたことにより、陰極の腐食を防止し、高品質の表示を可能とした高信頼性の表示装置

が提供される。本発明のより具体的な構成例を記述すると以下のとおりである。すなわち、

（１）基板上の表示領域内にマトリクス配列された複数の走査線と前記複数の走査線に交差する複数のデータ線の交差部毎に画素を有し、前記画素に表示のための電流を供給する電流供給線を備え、前記画素は、前記走査線で選択されるアクティブ素子と、このアクティブ素子のターンオンで前記データ線から供給されるデータ信号を保持するデータ保持素子、および前記データ保持素子に保持されたデータ信号にしたがって前記電流供給線から供給される電流で発光する発光素子とを備え、前記発光素子は前記アクティブ素子で駆動される第１の電極層と、前記第１の電極層上に塗布された有機発光層と、前記有機発光層上に形成された第２の電極層で構成され、前記基板上に前記第２の電極層より下層で、かつ絶縁もしくは保護膜で被覆された第２電極接続電極層を有し、前記第２の電極層をコンタクトホールにより前記第２電極接続電極層に接続した。

【００３４】（２）、（１）において、前記基板の前記表示領域の外側に、外部回路から前記データ駆動回路にデータ信号を供給する第１の端子パッドと、前記走査駆動回路に走査信号を供給する第２の端子パッドと、前記電流供給バスラインに電流を供給する第３の端子パッドと、前記第２電極接続電極層に接続する第４の端子パッドを備えた。

【００３５】（３）、（２）において、前記電流供給線を共通に接続する電流供給線バスラインを前記第３の端子パッドに接続する電流供給線引回しラインと、前記第２電極接続電極層を前記第４のパッドに接続する第２電極接続電極引き回しラインとを備えた。

【００３６】（４）、（１）または（２）において、前記第１～第４の端子パッドを前記基板の１辺に設けた。

【００３７】（５）、（４）において、前記電流供給線引回しラインと前記第２電極接続電極引き回しラインを前記基板の前記１辺に隣接する一の辺に引回した。

【００３８】（６）、（４）において、前記電流供給線引回しラインと前記第２電極接続電極引き回しラインとを前記基板の前記一の辺に隣接する両辺のそれぞれに引回した。

【００３９】（７）、（１）または（２）において、前記第３および第４の端子パッドを前記基板の前記第１および第２の端子パッドを設けた辺と対向する辺に設けた。

【００４０】（８）、（２）～（７）の何れかにおいて、前記基板上で、前記第２電極接続電極層を前記電流供給線を共通に接続する前記電流供給線バスラインよりも外側に設けた。

【００４１】（９）、（２）～（７）の何れかにおいて、前記基板上で、前記第２電極接続電極層を前記電流供給線バスラインに接続された前記電流供給線引回しラインよりも外側に設けた。

【００４２】なお、本発明は上記の構成および後述する実施例の構成に限定されるものではなく、本発明の技術思想を逸脱することなく種々の変更が可能であることは言うまでもない。本発明の他の目的および構成は後述する実施の形態の記載から明らかになるであろう。

【００４３】

【発明の実施の形態】以下、本発明の実施の形態につき、実施例の図面を参照して詳細に説明する。図示しないが、以降で説明する各画素に有する有機発光層は電流値に比例した輝度で、かつその有機材料に依存した色（白色も含む）で発光させてモノクロあるいはカラー表示を行わせるものと、白色発光の有機層に赤、緑、青等のカラーフィルタを組み合わせてカラー表示を行わせるものとがある。

【００４４】図１は本発明による表示装置の第１実施例の構成を模式的に説明するブロック図である。本実施例の表示装置は、ガラス基板ＳＵＢ上に走査駆動回路ＧＤＲとデータ駆動回路ＤＤＲを有する。

【００４５】そして、マトリクスに形成された走査駆動回路ＧＤＲで駆動される（走査される）走査線ＧＬ、データ駆動回路ＤＤＲで駆動されるデータ線ＤＬ、電流供給線ＣＳＬで囲まれた領域に１画素が形成される。また、基板ＳＵＢの１の辺には外部回路から走査駆動回路ＧＤＲ、データ駆動回路ＤＤＲへの信号や電圧を供給するための端子パッドＰＡＤ１、ＰＡＤ２が形成されている。

【００４６】図２は図１における１画素の画素回路の構成図である。本実施例の概略構成は、１画素はデータ線ＤＬ（ｍ＋１）と走査線ＧＬ（ｎ＋１）、ＧＬ（ｎ）および電流供給線ＣＳＬで囲まれた領域に形成される。ここでは、現在走査されている（選択されている）走査線をＧＬ（ｎ＋１）として説明する。

【００４７】走査線ＧＬ（ｎ＋１）で選択されている複数の画素のうち、画素ＰＸに着目する。アクティブ素子である第１の薄膜トランジスタＴＦＴ１はスイッチングトランジスタ、第２の薄膜トランジスタＴＦＴ２はドライバトランジスタである。第１の薄膜トランジスタＴＦＴ１のゲートは走査線ＧＬ（ｎ＋１）に接続され、そのドレインはデータ線ＤＬ（ｍ＋１）に、ソースは第２薄膜トランジスタＴＦＴ２のゲートに接続されている。

【００４８】第２の薄膜トランジスタＴＦＴ２のドレインは図１に示した電流供給線バスラインＣＳＢから電流が供給される電流供給線ＣＳＬに接続されている。そして、そのソースはＯＬＥＤ２４の第１の電極層ＡＤに接続されている。第１の薄膜トランジスタＴＦＴ１のソースと第２の薄膜トランジスタＴＦＴ２のゲートの接続点にはデータ信号保持素子としてのコンデンサＣＰＲの一方の端子が接続され、他方の端子は直前の走査線ＧＬ（ｎ）に接続されている。

【００４９】図２に示した１画素の回路構成において、第１の薄膜トランジスタＴＦＴ１のソースと第２の薄膜トランジスタＴＦＴ２のゲートの接続点に接続されるコンデンサＣＰＲの一方の端子は＋極であり、走査線ＧＬ（ｎ）に接続される他方の端子は－極である。

【００５０】また、有機発光素子ＯＬＥＤは第１の電極層ＡＤと第２の電極層ＣＤの間に有機発光層（図示せず）を挟んだ構成であり、第１の電極層ＡＤは第２の薄膜トランジスタＴＦＴ２のソース電極に接続し、第２の電極層ＣＤは全画素にわたってべた形成されて図１の第２電極接続電極層ＣＮＴＢに接続している。

【００５１】この第２電極接続電極層ＣＮＴＢは、所謂電流引抜き配線（電極）であり、基板の下層に前記端子パッドＰＡＤ１、ＰＡＤ２と同層に形成されており、第２の電極層ＣＤをコンタクトホールＣＮＴで接続し、第２電極接続電極引回しラインＣＮＴＬで前記端子パッドＰＡＤ１、ＰＡＤ２と同層に形成された端子ＰＡＤ４に接続されている。

【００５２】なお、第１の電極層の配線である電流供給線ＣＳＬも電流供給線バスラインＣＳＢと電流供給線引回しラインＣＳＬＬで前記端子パッドＰＡＤ１、ＰＡＤ２と同層に形成された端子ＰＡＤ３に接続されている。上記第２電極接続電極層ＣＮＴＢは電流供給線バスラインＣＳＢよりも基板の外側、かつ点線で示した基板の封止領域ＳＬの内側に配置されている。

【００５３】このように、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢよりも基板ＳＵＢの外側で、かつシール領域の内側に配置したことで、フレキシブルプリント基板を介して１辺で外部回路と接続する方式における基板上のレイアウトが容易となる。

【００５４】第１の薄膜トランジスタＴＦＴ１のターンオンでコンデサＣＰＲに書き込まれ、電荷量として保持されたデータ信号は第１の薄膜トランジスタＴＦＴ１のターンオフに伴う第２の薄膜トランジスタＴＦＴ２のターンオンで電流供給線ＣＳＬからの電流を当該コンデンサＣＰＲに保持された電荷量（データ信号の階調を示す）で制御された電流量として有機発光素子ＯＬＥに流す。

【００５５】有機発光素子ＯＬＥＤは供給される電流量にほぼ比例した輝度で、かつ当該有機発光素子を構成する有機発光層ＯＬＥの材料に依存した色で発光する。カラー表示の場合は、通常は赤、緑、青の画素毎に有機発光層材料を変えるか、あるいは白色の有機発光層材料と各色のカラーフィルタの組合せを用いる。

【００５６】なお、データ信号の与え方はアナログ量でも、あるいは時分割のデジタル量でもよい。また、階調制御は、赤、緑、青の各画素の面積を分割した面積階調方式を組合せてもよい。

【００５７】本実施例では、電流供給線バスラインＣＳＢと、各画素回路の発光動作後に第２の電極層ＣＤから流れ出る電流を基板の下層に形成した全画素共通に形成した電流引抜き配線である第２電極接続電極層ＣＮＴＢから第２電極接続電極引回しラインＣＮＴＬで端子パッドＰＡＤ４から外部回路に流出させるように構成したものである。

【００５８】そのため、本実施例では、上層にべた形成した全画素共通の第２の電極層ＣＤをコンタクトホールＣＮＴで第２電極接続電極層ＣＮＴＢに接続している。第２電極接続電極引回しラインＣＮＴＬも第２電極接続電極層ＣＮＴＢと同層に形成される。

【００５９】通常、この種の表示装置では、信頼性を確保するために缶などを用いた封止構造を採用している。基板ＳＵＢには、この封止缶詰を接着するためのシール領域が設けられている。このシール領域の内側に上記の第２電極接続電極層ＣＮＴＢや第２電極接続電極引回しラインＣＮＴＬを形成している。そして、少なくとも上記の第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢの外側に配置している。

【００６０】上記第２電極接続電極層ＣＮＴＢ等は基板の下層に形成され、その上に絶縁層や保護膜が積層されるので、第２電極や第２電極接続電極層、好ましくは第２電極接続電極引回しラインも含めて外気との接触がなくなり、その腐食が防止されるため、信頼性が向上し、高品質の表示を可能とした表示装置を提供することができる。なお、上記のコンタクトホールの個数は１つでもよいが、複数個設けた方がより多くの電流を安定して流すことができるため、本実施例では複数個設けている。

【００６１】図３は本発明による表示装置の発光メカニズムを説明する１画素付近の模式図、図４は第２電極層と第２電極接続電極層との接続部分を説明する模式図である。図１と同一参照符号は同一部分に対応する。また、図中の参照符号Ｉで示した矢印は発光に寄与する電流の経路を示す。

【００６２】薄膜トランジスタＴＦＴ２はドライバトランジスタである。この薄膜トランジスタＴＦＴ２がゲート線ＧＬで選択されたとき、電流供給線バスラインから分岐した電流供給線より、コンデンサに保持されたデータ信号に応じた階調の電流値の電流Ｉが当該薄膜トランジスタＴＦＴ２を通して有機発光素子ＯＬＥＤの第１の電極層ＡＤに供給される。

【００６３】有機発光素子ＯＬＥＤは、その有機発光層ＯＬＥ内で第２の電極層ＣＤからの電子と第１の電極層ＡＤからのホールとが再結合し、当該有機発光層ＯＬＥの材料特性に応じたスペクトルの光Ｌを発光する。第１の電極層ＡＤは各画素毎に独立であるが、第２の電極層ＣＤは全画素についてべた膜状に形成されている。薄膜トランジスタＴＦＴ２から有機発光素子ＯＬＥＤを通った電流Ｉは第２の電極層ＣＤから図４に示した第２電極接続電極層ＣＮＴＢを通して図１の第２電極接続電極引

回しラインＣＮＴＬから端子パッドＰＡＤ４に流出する。このような画素が多数マトリクス配列されて２次元の表示装置が構成される。

【００６４】図５は本発明による表示装置の第２実施例の構成を模式的に説明するブロック図である。図１と同一参照符号は同一機能部分に対応する。本実施例では、電流供給線ＣＳＬを接続する電流供給線バスラインＣＳＢの２つの端子パッドＰＡＤ３とＰＡＤ３'、および第２電極接続電極層ＣＮＴＢの端子パッドＰＡＤ４をデータ駆動回路の端子パッドＰＡＤ１および走査駆動回路ＧＤＲの端子パッドＰＡＤ２が配置される基板の１の辺と反対側の辺に設けた。

【００６５】本実施例によっても、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢよりも基板ＳＵＢの外側で、かつシール領域の内側に配置したことで基板上のレイアウトが容易となる。

【００６６】本実施例のように、電流供給線バスラインＣＳＢからその端子パッドＰＡＤ３とＰＡＤ３'に引き回す電流供給線引回しラインＣＳＬＬ、および第２電極接続電極層ＣＮＴＢと端子パッドＰＡＤ４間を接続する第２電極接続電極引回しラインＣＮＴＬの基板上での引回し長さが短くなるため、より均一な電流供給と電流引抜きが可能となる。これにより、表示領域での発光分布が均一となり、より高品質の表示が得られる。なお、電流供給線引回しラインＣＳＬＬは２本としているが、何れか一方であってもよい。図５に示したように、電流供給線引回しラインＣＳＬＬを電流供給線バスラインＣＳＢの一方及び他方からそれぞれ引き出して２本とした場合は対称性が良くなるという効果がある。

【００６７】本実施例によって、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢよりも基板ＳＵＢの外側で、かつシール領域の内側に配置したことで、フレキシブルプリント基板を介して対向する２辺で外部回路と接続する方式における基板上のレイアウトが容易となる。

【００６８】また、本実施例の構成としたことで、シール領域の近傍における配線パターンが少なくなるため、シール材料をＵＶ硬化させる際のＵＶ光の遮蔽物が少なくなり、当該シール材料を効果的に硬化させることができる。これにより、確実な封止が可能となり、表示装置の信頼性をさらに向上できる。

【００６９】図６は本発明による表示装置の第３実施例の構成を模式的に説明するブロック図である。図１と同一参照符号は同一機能部分に対応する。本実施例では、電流供給線ＣＳＬを接続する電流供給線バスラインＣＳＢのパッドＰＡＤ３と第２電極接続電極層ＣＮＴＢの端子パッドＰＡＤ４をデータ駆動回路の端子パッドＰＡＤ１および走査駆動回路ＧＤＲの端子パッドＰＡＤ２が配置される基板の１の辺の両端に振り分けて設けた。



【００７０】前記第１～第２実施例と同様に、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢよりも基板ＳＵＢの外側で、かつシール領域の内側に配置した。他の構成は図１と同様なので繰り返しの説明は省略する。

【００７１】本実施例によっても、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢよりも基板ＳＵＢの外側で、かつシール領域の内側に配置したことで、フレキシブルプリント基板を介して１辺で外部回路と接続する方式における基板上のレイアウトが容易となる。

【００７２】図７は本発明による表示装置の第４実施例の構成を模式的に説明するブロック図である。図１と同一参照符号は同一機能部分に対応する。本実施例では、電流供給線ＣＳＬを接続する電流供給線バスラインＣＳＢのパッドＰＡＤ３と第２電極接続電極層ＣＮＴＢの端子パッドＰＡＤ４をデータ駆動回路の端子パッドＰＡＤ１および走査駆動回路ＧＤＲの端子パッドＰＡＤ２が配置される基板の１の辺と反対側の辺に設けた。

【００７３】前記第１～第３実施例と同様に、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢよりも基板ＳＵＢの外側で、かつシール領域の内側に配置した。

【００７４】本実施例によっても、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢよりも基板ＳＵＢの外側で、かつシール領域の内側に配置したことで、フレキシブルプリント基板を介して対向する２辺で外部回路と接続する方式における基板上のレイアウトが容易となる。他の構成は図６と同様なので繰り返しの説明は省略する。

【００７５】本実施例のように、電流供給線バスラインＣＳＢからその端子パッドＰＡＤ３に引き回す電流供給線引回しラインＣＳＬＬ、および第２電極接続電極層ＣＮＴＢと端子パッドＰＡＤ４間を接続する第２電極接続電極引回しラインＣＮＴＬの基板上での引回し長さが短くなるため、より均一な電流供給と電流引抜きが可能となる。これにより、表示領域での発光分布が均一となり、より高品質の表示が得られる。

【００７６】また、本実施例の構成としたことで、シール領域の近傍における配線パターンが少なくなるため、シール材料をＵＶ硬化させる際のＵＶ光の遮蔽物が少なくなり、当該シール材料を効果的に硬化させることができる。これにより、確実な封止が可能となり、表示装置の信頼性をさらに向上できる。

【００７７】以上説明した第２～第４実施例では、電流路である電流供給線引回しラインＣＳＬＬと第２電極接

続電極引回しラインＣＮＴＬは、それぞれ基板上の広い領域に充分な太さの配線を形成でき、安定な電流路を確保することができる。また、特に第２実施例および第４実施例のように、パッドとの間の距離が短い場合は、より安定な電流路を確保することができる。

【００７８】図８は本発明による表示装置の第５実施例の構成を模式的に説明するブロック図である。図１と同一参照符号は同一機能部分に対応する。本実施例では、基板上において、第２電極接続電極層ＣＮＴＢを端子ＰＡＤ１～４を配置した辺に隣接して前記ゲート走査駆動回路ＧＤＲとは反対側の辺、かつ前記電流供給線引回しラインＣＳＬＬよりも外側に設けた。

【００７９】本実施例によって、第２の電極層ＣＤをコンタクトホールＣＮＴで接続する第２電極接続電極層ＣＮＴＢを電流供給線バスラインＣＳＢを端子パッドＰＡＤ３に引き回す電流供給線引回しラインＣＳＬＬよりも基板ＳＵＢの外側で、かつシール領域の内側に配置したことで、ゲート走査駆動回路ＧＤＲと対称配置のレイアウトとなり、全体としてバランスの取れた配置とすることができる。他の構成は図１と同様なので繰り返しの説明は省略する。

【００８０】また、本実施例のように、端子パッドＰＡＤ４と第２電極接続電極引回しラインＣＮＴＬの基板上での引回し長さが短くなるため、より均一な電流供給と電流引抜きが可能となる。これにより、表示領域での発光分布が均一となり、より高品質の表示が得られる。

【００８１】なお、上記の各実施例は、第１の電極層と第２の電極層のそれぞれを陰極層と陽極層に対応させることができるが、本発明はこれらを入れ換えた構造に対しても同様に適用できる。また、本発明は上記したＯＬＥＤを用いた表示装置に限るものではなく、ＯＬＥＤと同様の発光動作で表示を行う他の表示装置にも同様に適用できる。

【００８２】

【発明の効果】以上説明したように、本発明によれば、表示装置の画素を構成する電極層やその端子近傍での腐食が防止されるため表示不良の発生がない。また、電流供給線を通して電流を安定かつ充分に供給でき、高品質の表示を可能とした表示装置を提供することができる。

【図面の簡単な説明】



【図１】本発明による表示装置の第１実施例の構成を模式的に説明するブロック図である。

【図２】図１における１画素の画素回路の構成図である。

【図３】本発明による表示装置の発光メカニズムを説明する１画素付近の模式図である。

【図４】本発明による表示装置の第２の電極層と第２電極接続電極層との接続部分を説明する模式図である。

【図５】本発明による表示装置の第２実施例の構成を模式的に説明するブロック図である。

【図６】本発明による表示装置の第３実施例の構成を模式的に説明するブロック図である。

【図７】本発明による表示装置の第４実施例の構成を模式的に説明するブロック図である。

【図８】本発明による表示装置の第５実施例の構成を模式的に説明するブロック図である。

【図９】有機発光素子を用いた従来の表示装置の構成例を説明するブロック図である。

【図１０】図９における画素構成の説明図である。

【図１１】図１０の画素構成をもつ図９の表示装置の構成をさらに説明するブロック図である。

【図１２】有機発光素子を用いた従来の表示装置の他の構成例を模式的に説明する図１１と同様のブロック図である。

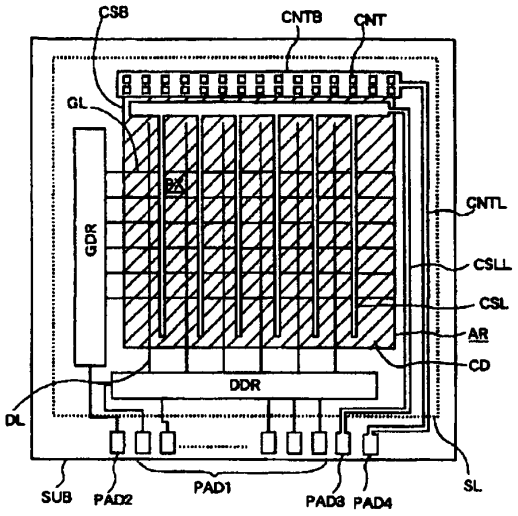
【図１３】有機発光素子を用いた表示装置の１画素付近の構造を説明する断面図である。

【符号の説明】

ＳＵＢ　基板
ＧＬ　ゲート線（走査線）
ＤＬ　データ線
ＣＳＬ　電流供給線
ＣＳＢ　電流供給線バスライン
ＣＳＬＬ　電流供給線引回しライン
ＣＤ　陰極
ＣＤＴ　コンタクトホール
ＣＮＴＢ　陰極接続電極層
ＣＮＴＬ　陰極接続電極引回しライン
ＡＤ　陽極
ＯＬＥ　有機発光層
ＯＬＥＤ　有機発光素子。

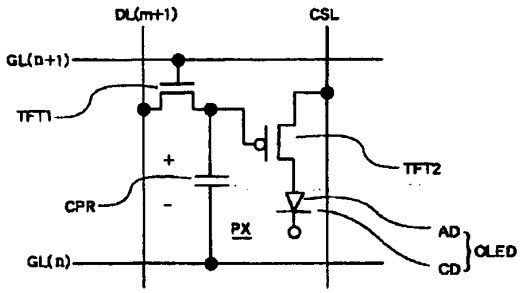
【図１】

図１



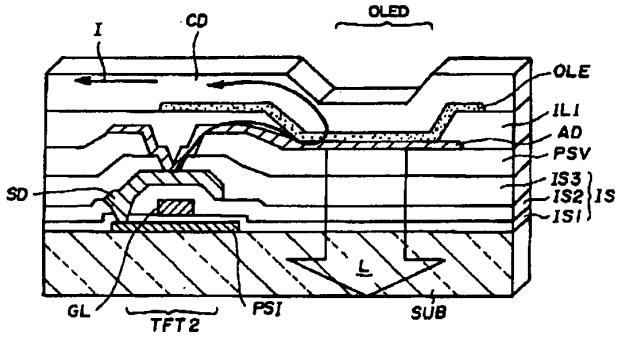

【図２】

図２



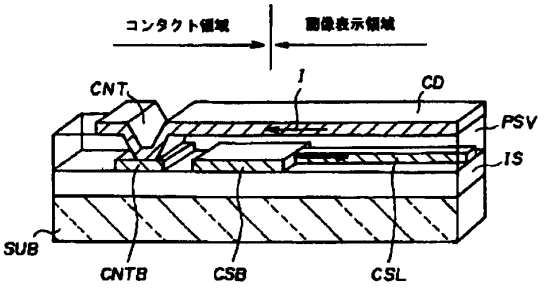

【図３】

図３



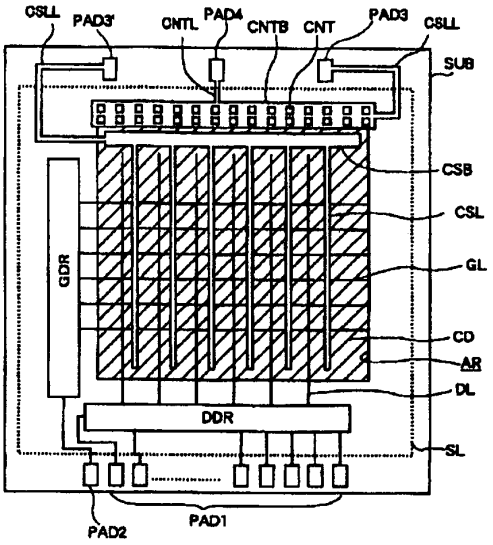
【図４】

図４



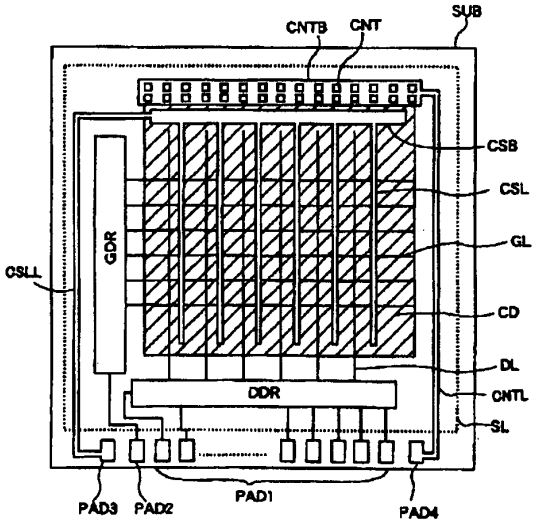

【図５】

図５



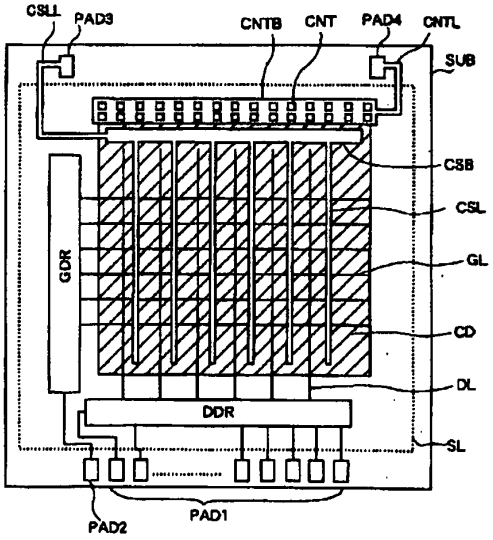

【図６】

図６



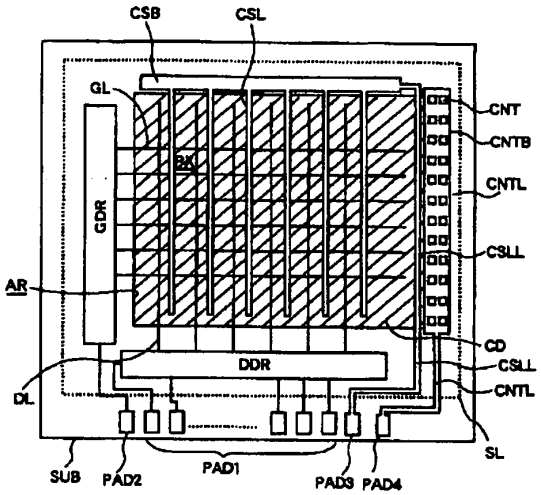

【図７】

図７



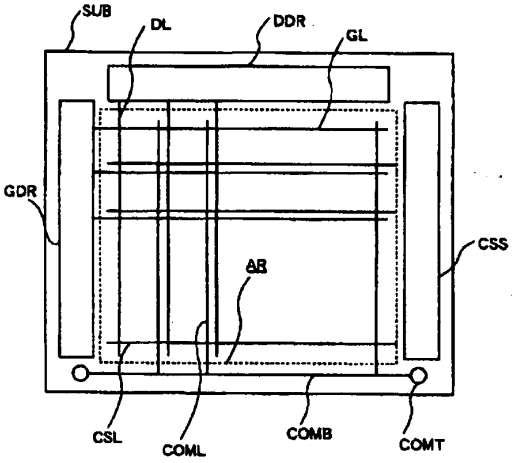
【図８】

**図８**



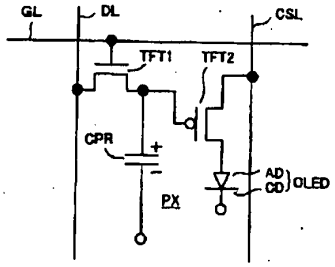

【図９】

**図９**



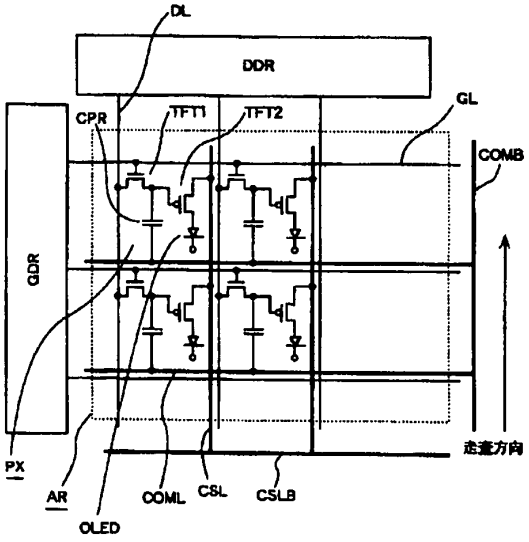

【図１０】

**図１０**



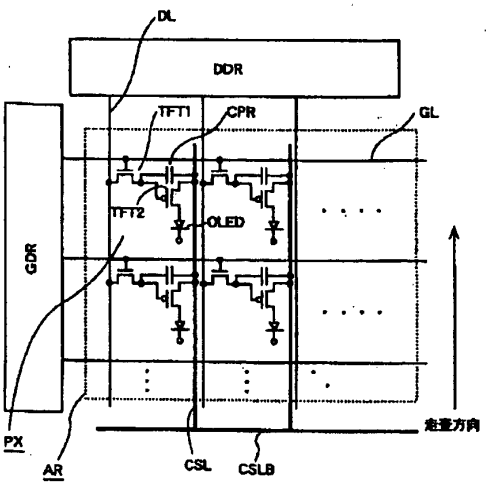

【図１１】

**図１１**



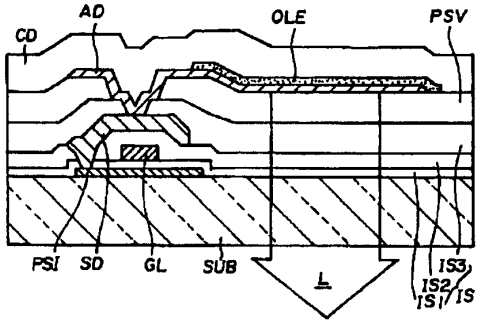
【図１２】

**図１２**




【図１３】

**図１３**




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フロントページの続き

Ｆターム(参考)　3K007 AB02 AB05 AB11 AB17 BA06
CA01 CB01 DA01 DB03 EB00
GA04
5C094 AA04 AA07 AA13 AA31 AA48
AA53 AA55 BA03 BA27 CA19
DA09 DA13 DB01 DB02 DB04
DB10 EA04 EA05 EA07 EA10
EB02 FA01 FA02 FB12 FB15

OIPE JAP97
JUN 19 2008
PATENT & TRADEMARK OFFICE



**PATENT APPLICATION**

**OLIFF & BERRIDGE, PLC**
**Telephone: (703) 836-6400**
**Facsimile: (703) 836-2787**

Attorney Docket No.: 117390

**CUSTOMER NUMBER 25944**

**AMENDMENT TRANSMITTAL**

In re the Application of

Yojiro MATSUEDA et al.

Group Art Unit: 2821

Application No.: 10/676,067

Examiner: DUONG

Filed: October 2, 2003

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Amendment in the above-identified application.

☐ Entitlement to small entity status is hereby asserted.

☐ Small entity status of this application has been established.

Any additional claim fees have been calculated as shown below:

| | (Column 1) | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN A SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|
| | CLAIMS REMAINING AFTER AMENDMENT | HIGHEST NO. PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE | ADD'L FEE | | RATE | ADD'L FEE |
| TOTAL CLAIMS | * MINUS | **20 | = | x 25 | $ | | x 50 | $ |
| INDEP CLAIMS | *7 MINUS | ***6 | =1 | x 105 | $ | | x 210 | $ 210.00 |
| ☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM | | | | + 185 | $ | OR | + 370 | $ |
| | | | | | $ | | | $ 210.00 |

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

☒ Check No. 206864 in the amount of $210.00 is attached. The Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Moshe K. Wilensky
Registration No. 56,263

JAO:MKW/jfb
Date: June 19, 2008




**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA et al. Group Art Unit: 2821

Application No.: 10/676,067 Examiner: D. DUONG

Filed: October 2, 2003 Docket No.: 117390

For: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE AND ELECTRONIC APPARATUS

**AMENDMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the March 19, 2008 Office Action, please consider the following:

**Amendments to the Specification**;

**Amendments to the Drawings** include an attached replacement sheet;

**Amendments to the Claims** as reflected in the listing of claims; and

**Remarks**.

06/20/2008 SZEWDIE1 00000084 10676067
01 FC:1201 210.00 OP

**Amendments to the Specification**:

Please replace paragraph **[0025]** with the following rewritten paragraph:

**[0025]** Fig. 6(a) through Fig. 6(f) are explanatory diagrams for describing application examples employing the organic EL display according to the present ~~invention.~~invention;

**[0025.1]** Fig. 7 is an explanatory diagram for describing a wiring layout according to a fourth embodiment.

**[0025.2]** Fig. 8 is an explanatory diagram for describing a wiring layout according to a fifth embodiment.

**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device, comprising:

an electric power supply circuit;

a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit, the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of ~~the~~ a row direction and ~~the~~ a column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and each of the line forming regions being formed with generally the same width;

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices; ~~and~~

~~at least two electric power lines of the plurality of electric power lines with different widths being formed~~

~~in at least one line forming region of the plurality of line forming regions.~~

a first line forming region having at least two electric power lines selected from the plurality of power lines with different widths; and

a second line forming region having at least one data line selected from a plurality of data lines,

wherein the first and the second line forming regions are either both in the column direction or both in the row direction.

2. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

~~the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and at least two electric power lines of the plurality of electric power lines with different widths, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and~~

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction;

a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, wherein at least one of the line forming regions contains lines chosen from at least two of the following groups: (1) at least two electric power lines of the plurality of electric power lines with different widths, (2) at least one scan line of the plurality of scan lines, and (3) at least one data line of the plurality of data lines; and

a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

3. (Currently Amended) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and both at least two electric power lines of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming ~~regions.~~regions,

a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

4. (Previously Presented) An electro-optical device, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixels, disposed at portions corresponding to intersections of the scan lines and the data lines, including electro-optical devices; and

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of said plurality of pixel groups, and both at least two electric power lines of the plurality of electric power

lines and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions; and

a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

5. (Previously Presented) The electro-optical device according to Claim 2, the line forming regions being formed with generally the same width.

6. (Canceled)

7. (Previously Presented) The electro-optical device according to Claim 1, the electro-optical device being a light-emission device;

and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

8. (Previously Presented) The electro-optical device according to Claim 7, the color of the light which is to be emitted being at least one of red, green, and blue.

9. (Previously Presented) The electro-optical device according to Claim 1, the electro-optical device being an electro-luminescence device.

10. (Previously Presented) An electronic apparatus, comprising:

the electro-optical device according to Claim 1.

11. (Currently Amended) A matrix substrate, comprising:

a plurality of pixel electrodes disposed in the form of a matrix, the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and the line forming regions being formed with generally the same width;

a plurality of electric power lines with different widths to supply voltage to the plurality of pixel electrodes; ~~and~~

a first line forming region having at least two electric power lines selected from the plurality of power lines with different widths; and

a second line forming region having at least one data line selected from a plurality of data lines,

wherein the first and the second line forming regions are either both in the column direction or both in the row direction.

~~at least two electric power lines of the plurality of electric power lines with different widths being formed in at least one line forming region of the plurality of line forming regions.~~

12. (Currently Amended) A matrix substrate, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel electrodes disposed at portions corresponding to intersections of the scan lines and the data lines;

a plurality of electric power lines with different widths to supply voltage to the plurality of pixel electrodes;

the plurality of pixel electrodes making up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column ~~direction,~~direction; ~~a plurality of line forming regions being formed between adjacent pixel electrode groups of the plurality of pixel electrode groups, and at least two lines selected from at least two electric power lines of the plurality of electric power lines, at least one scan line of the plurality of scan lines, and at least one data line of the plurality of data lines, being formed in at least one line forming region of the plurality of line forming regions; and~~

a plurality of line forming regions being formed between adjacent pixel electrode groups of said plurality of pixel electrode groups, wherein at least one of the line forming regions contains lines chosen from at least two of the following groups: (1) at least two electric power lines of the plurality of electric power lines with different widths, (2) at least one scan line of the plurality of scan lines, and (3) at least one data line of the plurality of data lines; and

a sum of the widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of the sum of the widths of a plurality of lines formed in another line forming region.

13. (Previously Presented) The electro-optical device according to claim 1, each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pixel pitch.

14. (Currently Amended) The electro-optical device according to claim 1, wherein the ~~combination of the plurality of lines being disposed periodically and~~ groupings of lines that constitute each line forming region are grouped in the same manner repeatedly in at least one ~~direction of~~ the row direction and the column direction.

15. (Previously Presented) The electro-optical device according to claim 1, wherein a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

16. (Previously Presented) The electro-optical device according to claim 11, wherein a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.

17. (New) An electro-optical device, comprising:

an electric power supply circuit;

a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit, the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and each of the line forming regions being formed with generally the same width;

a plurality of electric power lines with different widths to supply driving voltage to the electro-optical devices;

a first line forming region having at least two electric power lines selected from the plurality of power lines with different widths; and

a second line forming region having at least one data line selected from a plurality of data lines,

wherein the first and the second line forming regions are either both in the column direction or both in the row direction.

**Amendments to the Drawings**:

The attached drawing sheets add Figs. 7 and 8.

Attachments: New Sheets

## REMARKS

Claims 1-5 and 7-17 are pending in this application. By this Amendment, claims 1, 2, 3, 11, 12 and 14 are amended, claim 17 is added, Figs. 7 and 8 are added, and the specification is amended to identify the new figures. Claim 12 is amended for improved clarity. Support for the other amended claims can be found, for example, in Fig. 3 and paragraphs [0030]-[0033] of the specification. No new matter is added.

Applicants appreciate the courtesies shown to Applicants' representative by Examiners Duong and Tran in the May 19, 2008 personal interview. Applicants' separate record of the substance of the interview is incorporated into the following remarks.

### I. §112 Rejection of Claims 2-5 and 12

The Office Action rejects claims 2-5 and 12 under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement. This rejection is respectfully traversed.

During the May 19 interview, the Examiners asserted that claims 2-4 (and 12) were not supported by the specification and figures. The Examiners asserted, for example, that claim 3 recites "a plurality of line forming regions...and both at least two electric power lines of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region" (emphasis added).

The Examiners indicated that neither the specification, nor the figures, support a line forming region having two power lines and a scan line. The Examiners indicated, for example, that Fig. 4 shows line forming region 51 having one power line and one scan line, and line forming region 41 having 3 power lines, but no line forming region having two power lines and a scan line.

Applicant respectfully asserts that the Examiners are impermissibly narrowing the scope of support provided by the specification to the particular illustrative embodiments

shown in the figures. Paragraphs [0030]-[0033] of the specification fully support claims 2-4 and 12. Specifically, paragraph [0030], in conjunction with Fig. 3, explains that a basic premise of the invention is to ensure that the line forming regions, for example regions 31-34 in Fig. 3, all have the same width. The illustrative embodiment, shown in Fig. 3, groups a single power line (Vdd-R) in region 31, two data lines in region 32, two power lines in region 33, and a single data line in region 34.

However, paragraph [0033] explicitly states that this grouping is one illustrative. Paragraph [0033] further states that the invention is not limited to only two lines, or only the specifically discussed combinations of lines, in each region. As such, as long as the power, scan and data lines are combined in such a manner as to create uniform width in each line forming region, any combination of any number of various lines is supported.

Claims 2-4 and 12 are such combinations, which happen to use larger numbers of power and scan lines than shown in the illustrative embodiment of Figs. 3 and 4. Nevertheless, applicant respectfully submits the claims are fully supported by the specification. As such, withdrawal of the rejection is respectfully requested.

**II. §112 Rejection of Claim 14**

Claim 14 is rejected under 35 U.S.C. §112, second paragraph, for allegedly being indefinite. This rejection is respectfully traversed.

The Office Action asserts that the claim term "the combination of the plurality of lines" is indefinite because it is unclear which lines the claim is referring to. Claim 14, as amended, recites that the "groupings of lines that constitute each line forming region are grouped in the same manner repeatedly in at least one of the row direction and the column direction." Applicant submits claim 14 is now sufficiently definite. As such, withdrawal of the rejection is respectfully requested.

**III. Objection to the Drawings**

The Office Action objects to the drawings for failing to identify all of the features of claims 2-5 and 12.

New Figs. 7 and 8 have been added. These figures, which are supported by paragraphs [0030]-[0033] (as discussed above), support claims 2-5 and 12. Thus, withdrawal of the objection is respectfully requested.

**IV. §103(a) Rejection of Claims 1, 7-11 and 13-16**

Claims 1, 7-11 and 13-16 are rejected under 35 U.S.C. §103(a) over U.S. Patent App. No. 2001/0048106 to Tanada in view of U.S. Patent No. 6,825,820 to Yamazaki et al ("Yamazaki"). This rejection is respectfully traversed.

Claims 1 and 11, as amended, recite that the electro-optical device has "a first line forming region having at least two electric power lines; and a second line forming region having at least one data line selected from a plurality of data lines, wherein the first and the second line forming regions are either both in the column direction or both in the row direction." Applicant respectfully asserts Tanada and Yamazaki do not disclose these features. As such, withdrawal of the rejection is respectfully requested.

**V. §103(a) Rejection of Claims 2-5 and 12**

Claims 2, 4-5 and 12 are rejected under 35 U.S.C. §103(a) over U.S. Patent Publication No. 2003/0076046 to Komiya et al ("Komiya") in view of Yamazaki. Claim 3 is rejected under 35 U.S.C. §103(a) over U.S. Patent No. 6,633,135 to Nara et al ("Nara") in view of Yamazaki. These rejections are respectfully traversed.

Claims 2 and 12, as amended, recite that at least one line forming region will contain "lines chosen from at least two of the following groups: (1) at least two electric power lines of the plurality of electric power lines with different widths, (2) at least one scan line of the plurality of scan lines, and (3) at least one data line of the plurality of data lines." Likewise,

claim 3 recites that the line forming regions contains both two electric power lines and a scan line. The current §103(a) rejections do not address where the applied references disclose these features. Rather, the current rejections are substantively identical to the rejections of these claims from the previous Office Action. Applicant presumes the Office Action chose to give no patentable weight to the above features, in light of the §112 rejection.

However, these features are supported by the specification, as discussed above. Therefore, because the Office Action does not address where these features are disclosed in the applied references, the Office Action fails to present a prima facie case that the applied references disclose or suggest every feature of claims 2-4 and 12. As such, withdrawal of the rejections of claims 2-4 and 12, and claim 5 depending therefrom, is respectfully requested.

**VI. Conclusion**

Applicants also submit claim 17 is in condition for allowance, for both the reasons discussed above with respect to claim 1, as well as for the separately patentable subject matter is recites.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Moshe K. Wilensky
Registration No. 56,263

JAO:MKW/jfb

Attachments:
Amendment Transmittal
Figs. 7 and 8

Date: June 19, 2008

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Fig. 7

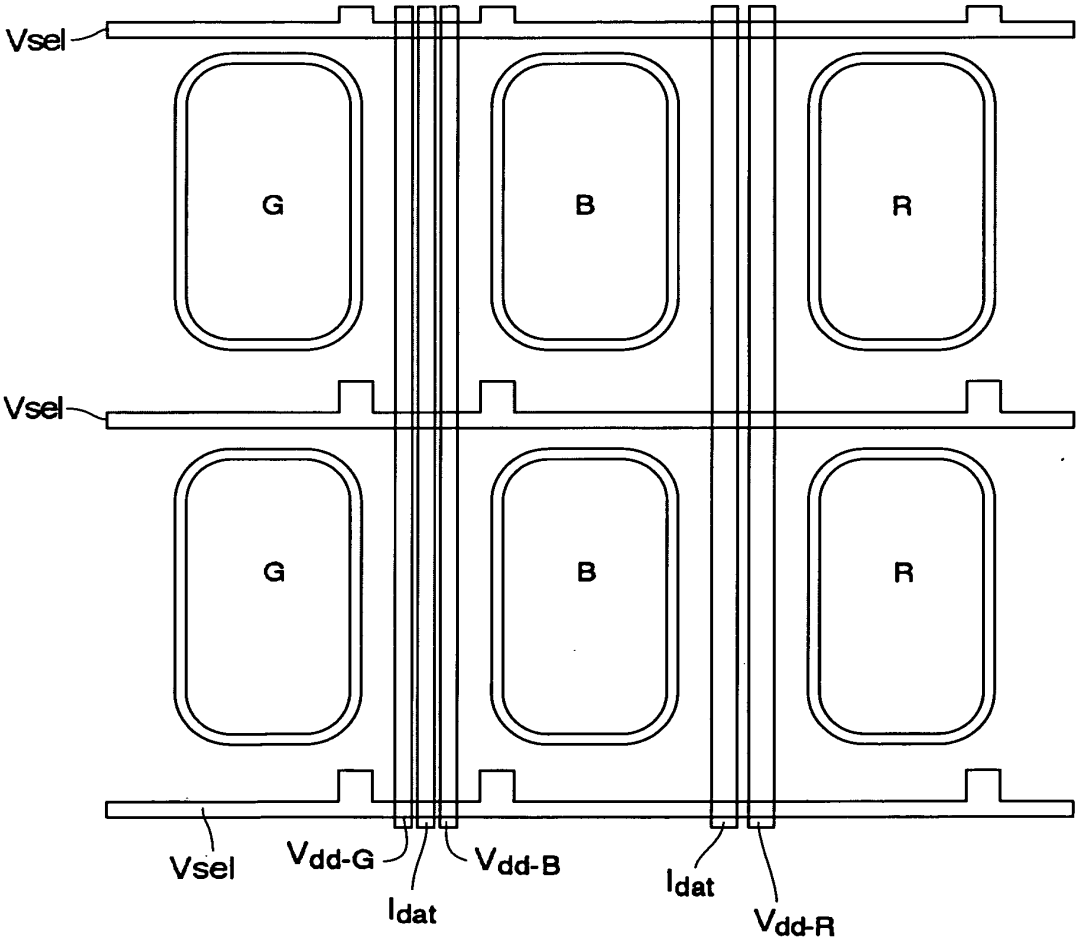
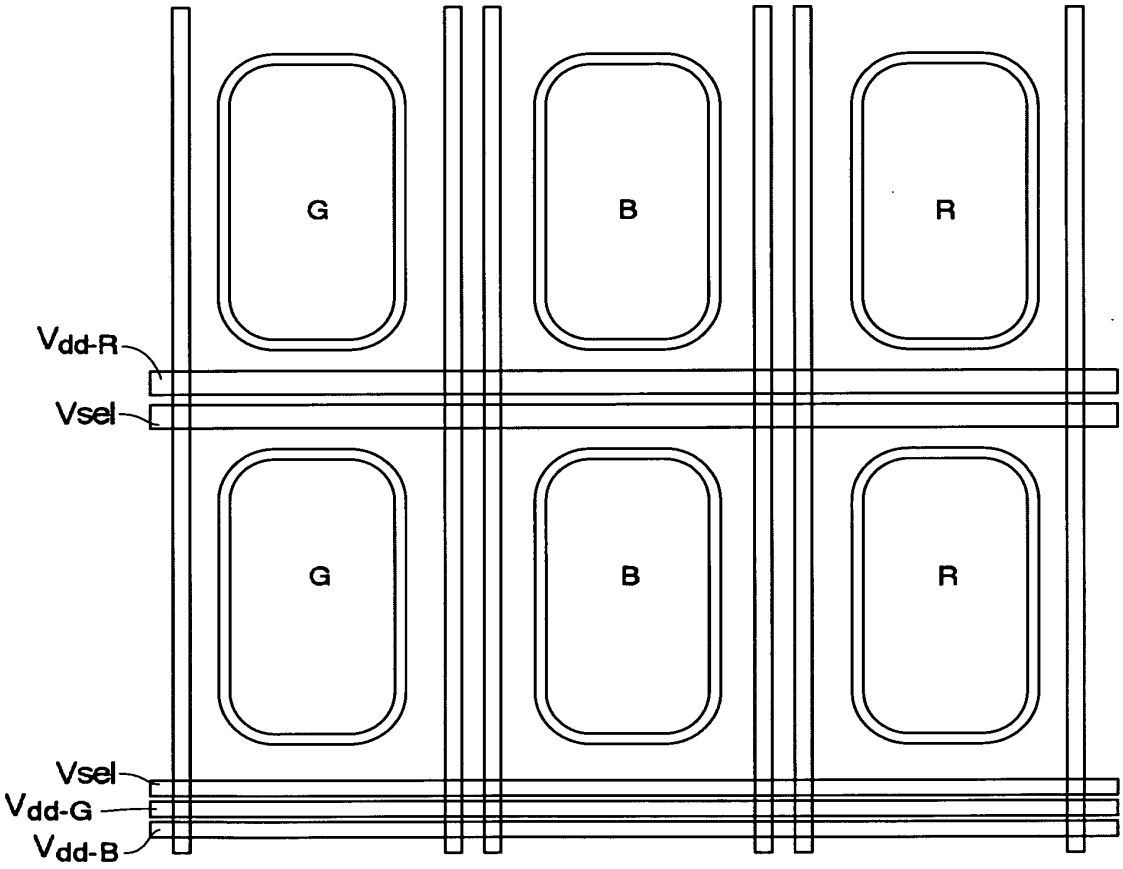


Fig. 8



PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

| Application or Docket Number | Filing Date | ☐ To be Mailed |
|---|---|---|
| 10/676,067 | 10/02/2003 | |

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☒ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | **770** |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | **770** |

## APPLICATION AS AMENDED – PART II

| | | (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **06/19/2008** | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| AMENDMENT | Total (37 CFR 1.16(i)) | * 16 | Minus | ** 20 | = 0 | X $ = | | OR | X $50= | 0 |
| | Independent (37 CFR 1.16(h)) | * 7 | Minus | ***6 | = 1 | X $ = | | OR | X $210= | 210 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | **210** |

| | | (Column 1) | | (Column 2) | (Column 3) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| AMENDMENT | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/GLORIA TRAMMELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/676,067 | 10/02/2003 | Yojiro Matsueda | 117390 | 7780 |

25944 7590 10/14/2008

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

| EXAMINER | |
|---|---|
| DUONG, DIEU HIEN | |
| ART UNIT | PAPER NUMBER |
| 2821 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 10/14/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | DIEU HIEN T. DUONG | 2821 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5 and 7-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/01/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is a response to applicant's amendment filed 06/19/2008. In virtue of this amendment, claim 6 is canceled; claim 17 is newly added; thus, claims 1-5 and 7-17 are currently in the instant application.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2-4 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 2 has been amended to recite the feature "wherein at least one of the line forming regions contains lines chosen from at least two of the following groups: (1) at least two electric power lines of the plurality of electric power lines with different widths, (2) at least one scan line of the, plurality of scan lines, and (3) at least one data line of the plurality of data lines" in lines 18-21, which does not appear to be in the original filed specification (i.e. lines chosen from at least two power lines and at least one data line or lines chosen from at least two power lines and at least one scan line). Thus, the recitation must be treated as "new matter".

Claim 3 recites the feature “both at least two electric power lines of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions”, in lines 11-13, which does not appear to be in the originally filed specification. Thus, the recitation must be treated as "new matter".

Claim 4 recites the limitation “both at least two electric power lines of the plurality of electric power lines and at least one data line of the plurality of data lines being formed in at least one line forming region of the plurality of line forming regions”, in lines 11-13, which does not appear to be in the originally filed specification. Thus, the recitation must be treated as "new matter".

Claim 5 is rejected since it is dependent on claim 2.

Claim 12 has been amended to recite the feature “wherein at least one of the line forming regions contains lines chosen from at least two of the following groups: (1) at least two electric power lines of the plurality of electric power lines with different widths, (2) at least one scan line of the, plurality of scan lines, and (3) at least one data line of the plurality of data lines” in lines 17-21, which does not appear to be in the original filed specification (i.e. lines chosen from at least two power lines and at least one data line or lines chosen from at least two power lines and at least one scan line). Thus, the recitation must be treated as "new matter".

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 7-11 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 6,522,079 B1) in view of Yamazaki et al. (US 6,825,820 B2 of record), hereinafter "Yamazaki".

Regarding claims 1, 11 and 17, Yamada discloses, in Figures 5B, an electro-optical device comprising an electric power supply circuit; a plurality of pixels (PX1, PX2), disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from the electric power supply circuit, the plurality of pixels (PX1, PX2) making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of a row direction and a column direction, a plurality of line forming regions being formed between adjacent pixel groups of the plurality of pixel groups, and each of the line forming regions being formed with generally the same width; a plurality of electric power lines (VL1, VL2) to supply driving voltage to the electro-optical devices; and a first line forming region having at least two electric power lines (VL1, VL2) selected from the plurality of power lines; a second line forming region having at least one data line (DL2) selected from a plurality of data lines; wherein the first and second line forming regions are either both in the column direction or both in the row direction.

Yamada does not disclose the electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to modify the power lines of Yamada with the power lines having different widths as taught by Yamazaki in order to improve the brightness uniformity of the display device (col. 3, lines 62-67).

Regarding claim 7, as applied to claim 1, Yamada/Yamazaki disclose, (see Yamazaki, Figure 1B), the electro-optical device being a light-emission device and the electric power lines being formed with different widths corresponding to the emission light color of said light-emission device.

Regarding claim 8, as applied to claim 7, Yamada/ Yamazaki disclose, (see Yamazaki, Figure 14B), the color of the light which is to be emitted being at least one of red, green, and blue.

Regarding claim 9, as applied to claim 1, Yamada/Yamazaki disclose, (Yamazaki, Figures 14), the electro-optical device being an electro-luminescence device.

Regarding claim 10, Yamada/Yamazaki disclose, (Yamada, Figure 12), a electronic apparatus comprising the electro-optical device according to claim 1.

Regarding claim 13, as applied to claim 1, Yamada/Yamazaki disclose, (Yamada, Figure 5B; Yamazaki, Figure 14B), each of the line forming regions being formed in at least one direction of the row direction and the column direction with generally the same pixel pitch.

Regarding claim 14, Yamada/Yamazaki disclose, (Yamada, Figure 5b; Yamazaki, Figure 14B), grouping of lines that constitute each line forming region are

grouped in the same manner repeatedly in at least one of the row direction and the column direction.

Regarding claims 15-16, Yamada/Yamazaki disclose, (Yamada, Figure 5B; Yamazaki, Figure 14B), wherein a sum of widths of a plurality of lines including at least one electric power line formed in one line forming region is approximately the same as that the sum of widths of a plurality of lines formed in another line forming region.

6. Claims 2, 4-5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komiya et al. (US 2003/0076046 A1 of record) in view of Yamazaki et al. (US 6, 825,820 B2 of record), hereinafter “Komiya” and “Yamazaki”.

Regarding claim 2, Komiya discloses, in Figures 4-5 and page 5, par. [0067], an electro-optical device comprising a plurality of scan lines (G); a plurality of data lines (D); a plurality of pixels (Fig. 5), disposed at portions corresponding to intersections of the scan lines (G) and the data lines (D), including electro-optical devices; and a plurality of electric power lines (183) to supply driving voltage to the electro-optical devices; the plurality of pixels making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction (Fig. 5), a plurality of line forming regi ons (183, D) being formed between adjacent pixel groups of said plurality of pixel groups, and at least two lines (183, D) selected from at least one electric power line of the plurality of electric power lines (183), at least one scan line of the plurality of scan lines, and at least one data line (D) of the plurality of data lines (D), being formed in at least one line forming region of the plurality of line forming regions; and a sum of widths (183, D) of a plurality of lines including at least

one electric power line (183) formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region (183, D).

Komiya does not disclose electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Komiya to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).

Claim 4 is rejected for similar subject matter to claim 2.

Regarding claim 5, as applied to claim 1, Komiya/Yamazaki disclose, the line forming regions being formed with generally the same width (see Komiya, lines 7-9 of par. [0076]).

Claim 12 is rejected for similar subject matter to claim 2.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nara et al. (US 6,633,135 B2 of record) in view of Yamazaki et al. (US 6,825,820 B2 of record), hereinafter “Nara” and “Yamazaki”.

Regarding claim 3, Nara discloses, in Figure 1, an electro-optical device comprising a plurality of scan lines (VG); a plurality of data lines (VD); a plurality of pixels (11), disposed at portions corresponding to intersections of the scan lines (VG) and data lines (VD) including electro-optical devices; and a plurality of electrical power

lines (VLC) to supply driving voltage to the electro-devices; the plurality of pixels (11) making up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, a plurality of line forming regions (VG, VLC) being formed between adjacent pixel groups of the plurality of pixel groups, and both at least one electric power line (VLC) of the plurality of electric power lines and at least one scan line (VG) of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions.

Nara does not disclose the electric power lines with different widths.

Yamazaki discloses, in Figure 1B and page 6, lines 5-15, electric power lines with different widths.

It would have thus been obvious to one having ordinary skill in the art at the time the invention was made to include the electric power lines with different widths of Yamazaki in the display device of Komiya to achieve the claimed invention, doing so would improve the brightness uniformity of the display device (col. 3, lines 62-67).

***Response to Arguments***

8. Rejection of Claims 2-5 and 12 Under 35 U.S.C. 112 first paragraph:

Applicant's arguments filed 06/19/2008 have been fully considered but they are not persuasive.

Applicant argues that paragraphs [0030]-[0033] of the specification fully support claims 2-4 and 12. Specially, paragraph [0030] discloses a basic premise of the invention and paragraph [0033] explicitly states “any combination of any number of various lines is supported”.

Examiner respectfully disagrees.

In paragraph [0033] of the specification, lines 3-5, states that "three combinations of two electric power lines selected from the three RGB lines Vdd can be made". As understood, the three combinations of two electric power lines selected from the three RGB lines Vdd are the combinations of $V_{dd\text{-}R}V_{dd\text{-}G}$; $V_{dd\text{-}R}V_{dd\text{-}B}$; $V_{dd\text{-}G}V_{dd\text{-}B}$. Also, in paragraph [0033], lines 6-9 states that "a scan line $V_{sel}$ is disposed on each line forming region in the row direction, and any two lines selected from the three electric power lines Vdd and the three data line Idat are disposed on the line forming regions 31, 32, and 33 in the column direction". As understood, there is one line in row direction (scan line) and there are two lines (one power line and one data line) in column direction. There is no where in the paragraphs [0030] - [0033] teaching that "any combination of any number of various lines".

Therefore, there is no support for the limitations of claims 2-4 and 12 as set forth below and they are treated as new subject matter and have been rejected under 35 USC 112, first paragraph as discussed above.

a) wherein at least one of the line forming regions contains lines chosen from at least two of the following groups: (1) at least two electric power lines of the plurality of electric power lines with different widths, (2) at least one scan line of the, plurality of scan lines, and (3) at least one data line of the plurality of data lines (claims 2 and 12)

b) both at least two electric power lines of the plurality of electric power lines and at least one scan line of the plurality of scan lines being formed in at least one line forming region of the plurality of line forming regions (claims 3-4).

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Inquiry***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIEU HIEN T. DUONG whose telephone number is (571)272-8980. The examiner can normally be reached on Monday - Friday, from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Owens can be reached on 571-272-1662. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

10/06/08
DD

AU 2821

/Trinh Vo Dinh/
Primary Examiner, Art Unit 2821

| Notice of References Cited | Application/Control No. 10/676,067 | Applicant(s)/Patent Under Reexamination MATSUEDA ET AL. | |
|---|---|---|---|
| | Examiner DIEU HIEN T. DUONG | Art Unit 2821 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| * | A | US-6,522,079 | 02-2003 | Yamada, Tsutomu | 315/169.3 |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
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| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 10676067 | MATSUEDA ET AL. |
| | Examiner | Art Unit |
| | Duong, Dieu Hien T | 2821 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 03/12/2008 | 10/06/2008 | | | | | | | |
| | 1 | ✓ | ✓ | | | | | | | |
| | 2 | ✓ | ✓ | | | | | | | |
| | 3 | ✓ | ✓ | | | | | | | |
| | 4 | ✓ | ✓ | | | | | | | |
| | 5 | ✓ | ✓ | | | | | | | |
| | 6 | - | - | | | | | | | |
| | 7 | ✓ | ✓ | | | | | | | |
| | 8 | ✓ | ✓ | | | | | | | |
| | 9 | ✓ | ✓ | | | | | | | |
| | 10 | ✓ | ✓ | | | | | | | |
| | 11 | ✓ | ✓ | | | | | | | |
| | 12 | ✓ | ✓ | | | | | | | |
| | 13 | ✓ | ✓ | | | | | | | |
| | 14 | ✓ | ✓ | | | | | | | |
| | 15 | ✓ | ✓ | | | | | | | |
| | 16 | ✓ | ✓ | | | | | | | |
| | 17 | | ✓ | | | | | | | |

Receipt date: 05/01/2008




10676067 - GAU: 2821

Sheet 1 of 1

| Form PTO-1449 (REV. 1/06) US Dept. of Commerce PATENT & TRADEMARK OFFICE | ATTY DOCKET NO. 117390 | APPLICATION NO. 10/676,067 |
|---|---|---|
| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | APPLICANT(S) Yojiro MATSUEDA et al. | |
| | FILING DATE October 2, 2003 | GROUP 2821 |

U.S. PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Name |
|---|---|---|---|---|
| /D.D./ | 1 | 6,724,149 | 04/20/2004 | KOMIYA et al. |
| /D.D./ | 2 | 7,009,345 | 03/07/2006 | KOMIYA et al. |
| /D.D./ | 3 | 6,965,363 | 11/15/2005 | SATO et al. |
| /D.D./ | 4 | 2006/0055643 | 03/16/2006 | SATO et al. |

FOREIGN PATENT DOCUMENTS

| Examiner Initials | Cite No. | Document Number | Date | Country | With English Abstract | With English Translation |
|---|---|---|---|---|---|---|
| /D.D./ | 5 | JP-A-2001-100654 | 04/13/2001 | JAPAN | X | X |
| /D.D./ | 6 | JP-A-2002-287663 | 10/04/2002 | JAPAN | X | X |

OTHER DOCUMENTS

| Examiner Initials | Cite No. | (Including Author, Title, Date, Pertinent Pages, etc.) |
|---|---|---|

| EXAMINER /Dieu Duong/ | DATE CONSIDERED 10/06/2008 |
|---|---|

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: May 1, 2008 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.D./

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/676,067 | 10/02/2003 | Yojiro Matsueda | 117390 | 7780 |

25944 7590 05/01/2009

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

| EXAMINER | |
|---|---|
| DUONG, DIEU HIEN | |
| ART UNIT | PAPER NUMBER |
| 2821 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 05/01/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Notice of Abandonment | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,067 | MATSUEDA ET AL. | |
| | Examiner | Art Unit | |
| | DIEU HIEN T. DUONG | 2821 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *10/14/2008*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____ ), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☒ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☒ The reason(s) below:

Applicant's representative (Reg. No. 56,263) indicated on April 17, 2009 that the case is abandoned.

/Trinh Vo Dinh/
Primary Examiner, Art Unit 2821

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.