

The Challenge of Signal Integrity in Deep-Submicrometer CMOS Technology

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Invited Paper

Advances in interconnect technologies, such as the increase in the number of metal layers, stacked vias, and the reduced routing pitch, have played a key role to continuously improve integrated circuit density and operating speed. However, several parasitic effects jeopardize the benefits of scale-down. Understanding and predicting interconnect behavior is vital for designing high-performance integrated circuit design. Our paper first reviews the interconnect parasitic effects and examines their impact on circuit behavior and their increase due to lithography reduction, with special emphasis on propagation delay, lateral coupling, and crosstalk-induced delay. The problem of signal integrity characterization is then discussed. In our review of the different well-established measurement methodologies such as direct probing, S-parameters, e-beam sampling, and on-chip sampling, we point out weaknesses, frequency ranges, drawbacks, and overall performances of these techniques. Subsequently, the on-chip sampling system is described. This features a precise time-domain characterization of the voltage waveform directly within the interconnect and shows its application in the accurate evaluation of propagation delay, crosstalk, and crosstalk-induced delay along interconnects in deep-submicrometer technology. The sensor parts are described in detail, together with signal integrity patterns and their implementation in 0.18- μm CMOS technology. Measurements obtained with this technique are presented. In the third part, we discuss the simulation issues, describe the two- and three-dimensional interconnect modeling problems, and review the active device models applicable to deep-submicrometer technologies in order to agree on measurements and simulations. These studies result in a set of guidelines concerning the choice of interconnect models. The last part outlines the design rules to be used by designers and their implementation within computer-aided design (CAD) tools to achieve signal integrity compliance. From a 0.18- μm technology are derived critical variables such as crosstalk tolerance margin, maximum coupling length, and the criteria for adding a signal repeater. From these, values for low-dielectric and copper interconnects have been selected.

Keywords—CMOS, deep-submicrometer technology, design guidelines, interconnect models, on-chip sampling, signal integrity.

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I. INTRODUCTION

System-level design to preserve signal integrity is a challenging issue in current deep-submicrometer CMOS technologies. Increasing switching speeds and the complexity of very large scale integration (VLSI) circuits are becoming the crucial factor in determining the reliability and performance of an electronic system. Enormous resources are required to ensure that signal integrity objectives are met.

Currently, simulations are used to verify that the design follows the specifications, but this procedure involves extraction of the equivalent circuit from the physical design to obtain estimates of signal quality and delay. In spite of the better performances of the extraction tools, it takes a considerable amount of computer resources to evaluate properly the reliability of the chips, which is incompatible with the "industrial cost" of chip design [1], [2].

Therefore, the precise characterization of interconnections must be achieved at the initial design stages to reduce time cost. The complexity of interconnect modeling also requires simple analytical formulations for delay, crosstalk, and crosstalk-induced delay to obtain accurate estimation of severity-induced faults that could be introduced within computer-aided design (CAD) tools to reduce computing time.

The optimal wire-sizing problem is one of the key issues in the technological development of chip performances—considering induced delay, crosstalk noise, and crosstalk delay—and plays an important role in establishing design rules. In recent years, many extensive studies have been conducted to optimize solutions to reduce interconnect contributions which take into account progress in microtechnology [3]–[5]. However, most of these use oversimplified separated models for devices and interconnects. A high level of accuracy for interconnects and device models is more and more difficult to achieve as technology scales down. Concerning interconnects, the main reasons are the increase in metallization layers, the material complexity, and

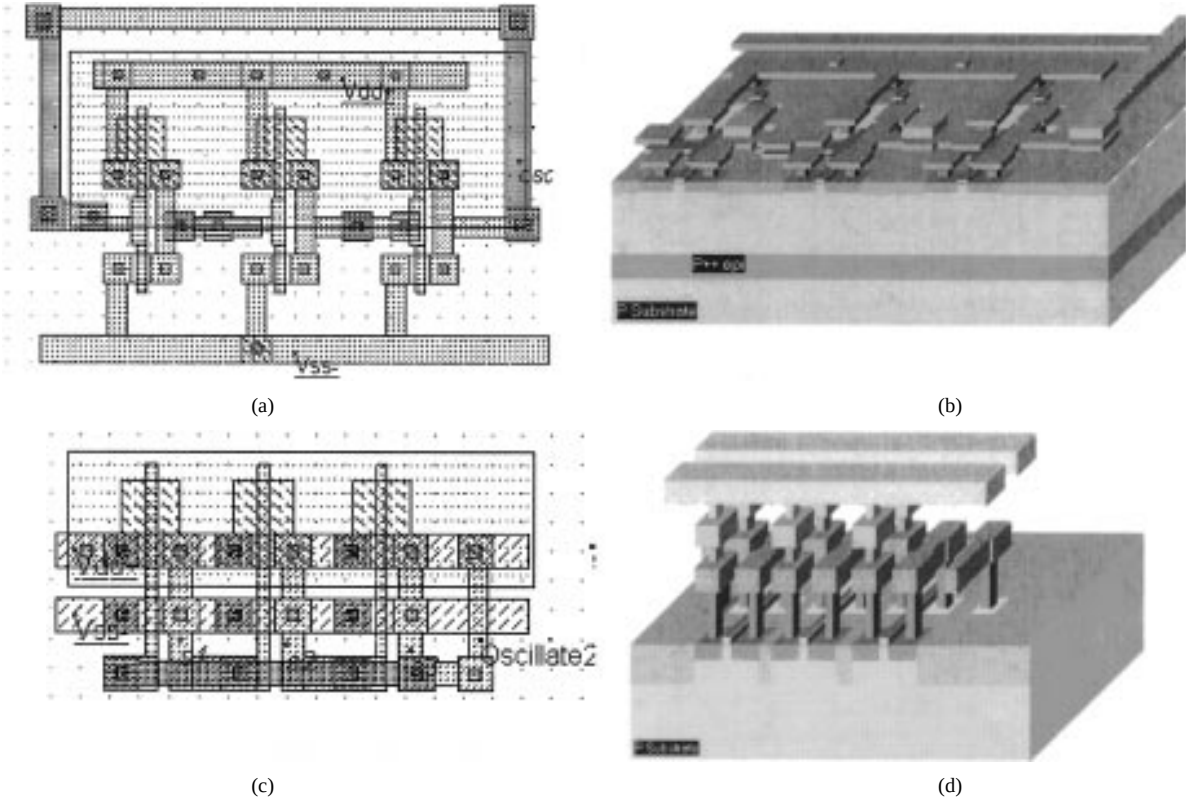


Fig. 1. Top view and 3-D view of a three-inverter ring oscillator in (a), (b) 0.7- μm and (c), (d) 0.18- μm technologies.

the increased operating frequencies (higher than 10 GHz for 0.1 μm). For devices, the ultranarrow channel length (0.1 μm) leads to a wide set of parasitic effects, which require increasingly complex formulations.

The primary objectives of this paper are to present the various aspects of signal integrity and how they evolve with technology scale-down. Second, we review a set of measurements methodologies for precise characterization of interconnects, from probe-tip to on-chip techniques, and list their constraints and performances. Third, from the experimental measurements for 0.18 μm , design guidelines are derived, to be inserted in routing tools to achieve signal integrity compliance at the integrated circuit level.

II. PARASITIC EFFECTS WITHIN INTERCONNECTS

In this chapter, technology scale-down is illustrated by means of one simple circuit in 0.7- μm and 0.18- μm CMOS technologies. The concomitant increase in parasitic effects is then analyzed.

A. Technology Scale-Down

Fig. 1 shows the top view and the three-dimensional (3-D) cross section of a ring oscillator based on three basic inverters. CMOS 0.7- μm technology with two metal layers is shown in Fig. 1(a), and CMOS 0.18- μm technology with six metal layers is shown in Fig. 1(c). Meanwhile, the silicon surface has been reduced by a factor of 40, from $40 \times 60 \mu\text{m}$ in 0.7- μm technology, to $10 \times 5 \mu\text{m}$ in 0.18- μm technology.

The increasing importance of the upper layers, acting as interconnects, appears very clearly. Furthermore, the lateral coupling effects between interconnects are dominant in 0.18- μm technology, compared to vertical coupling in the case of 0.7 μm , as the vertical dimensions did not scale down as fast as the horizontal dimensions.

Fig. 2 shows the cross section of a 0.18- μm device. Seven horizontal layers of interconnects appear, with vias between each layer. Aluminum has been used until recently to manufacture interconnects. The increasing contribution of interconnects in signal propagation has obliged integrated circuit manufacturers to replace aluminum, which exhibits a resistivity $\rho_{\text{al}} = 0.0277 \Omega/\mu\text{m}$, with copper which has resistivity $\rho_{\text{cu}} = 0.0172 \Omega/\mu\text{m}$. Consequently, the gain in terms of propagation delay is almost a factor of 2. Copper also reduces the interconnect failure sensitivity to electromigration by almost one order of magnitude. Also appearing in the figure is a nonhomogeneous oxide structure. Although the oxide that separates vertical layers is still high in permittivity ($\epsilon_r = 4$ for SiO_2), the tendency is to reduce the permittivity of the lateral oxide, that is, the space separating adjacent lines in a same interconnect layer ($\epsilon_r < 3$ for SiO_2). The main effect is the decrease of lateral coupling effects.

In micrometer-range technologies, the interconnect was a minor influence on signal propagation, and a 2-D approach of the interconnect, with simple line models and constant parameters, produced accurate simulations, that correlated well with measurements. Recently, several authors [5], [6] have shown that the process shrink makes the traditional approach

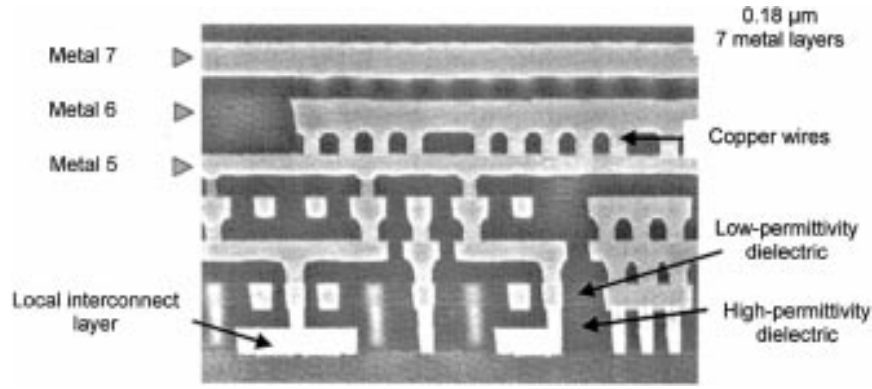


Fig. 2. Cross section of a 0.18- μ seven-metal process (courtesy ST Microelectronics).

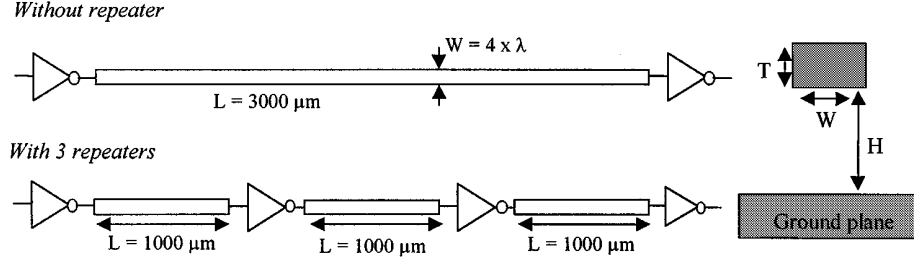


Fig. 3. Chain of scalable inverters used to illustrate the propagation with interconnects.

obsolete, due to a combination of parasitic effects mainly complex resistance, 3-D capacitance, and inductance [7].

B. Propagation Delay

To illustrate the increased role of interconnects in the propagation delay, we consider a simple interconnect with a 3-mm length, in one single line or divided in three portions of 1 mm each thanks to two supplementary inverters used as repeaters (Fig. 3). The buffer chosen is a very powerful (16 basic inverters in parallel), similar to the those used in clock trees. The buffer size is scaled down linearly for width and length, according to the technology. The normalized factor λ is used to define all the dimensions, so that 2λ is equal to the minimum channel length of the technology ($\lambda = 0.35 \mu\text{m}$ in a 0.7- μm technology). The configuration used for the interconnect lines is metal layer 3 on a ground plane of metal 1 except for the 0.7- μm technology where we choose a metal 2 on a substrate ground plane. All the interconnect dimensions used for the simulations are reported in Table 1, where the height, h , is the distance of the line to the ground plane.

For all the studies presented below, we analyze the propagation delay of the circuit design in various CMOS technologies, ranging from 0.7 μm in which interconnects are made of aluminum and isolated by SiO_2 , down to 0.07 μm , with copper and low dielectric, according to information provided by [8]. Starting at 0.18- μm generation, two technological options are considered: aluminum and copper interconnects. Performances with and without repeaters are also compared.

Table 1
Interconnect Dimensions Used for the Delay Simulation

Lithography	Lambda (μm)	W (μm)	T (μm)	H (μm)	T/W	Conductor material	ϵ_r
0.7 μm	0.4	1.6	1.1	3.0	0.6	Al	4.0
0.35 μm	0.2	0.8	0.8	2.8	1.0	Al	4.0
0.25 μm	0.125	0.5	0.7	2.1	1.2	Al	4.0
0.18 μm	0.09	0.4	0.6	1.8	1.5	Al	4.0
0.12 μm	0.06	0.3	0.5	1.5	1.7	Al	4.0
0.12 μm Cu						Cu	3.0
0.10 μm	0.05	0.2	0.4	1.2	2.0	Al	4.0
0.10 μm Cu						Cu	2.5
0.07 μm	0.035	0.15	0.35	0.9	2.5	Al	4.0
0.07 μm Cu						Cu	2.0

In Fig. 4(a), various delay definitions are represented on the simulation of the propagation in 0.18 μm , without repeaters. The delay A computed at $V_{DD}/2$ (i.e., 1 V in that technology) between the input fall edge and the near-end rise edge is small compared to the delay B , implying the near-end signal rise. The value $B-A$ corresponds to the interconnect contribution. A more precise evaluation of the propagation is based on the computation of the delay between 10% change of the input signal and 90% accomplishment of the output signal (C for near end, and D for far end). Delay D shall be used in this paper.

From the simulations of Fig. 4(b), the increase in interconnect delay with technology scale-down is obvious, specifically without repeaters. The copper option leads roughly to a 50% improvement in interconnect delay. (Note that the line length was kept constant at 3 mm). The interconnect delay has dramatically increased without repeaters mainly because of the continuously reduction of the interconnect section, which thus increases the serial line resistance. Meanwhile,

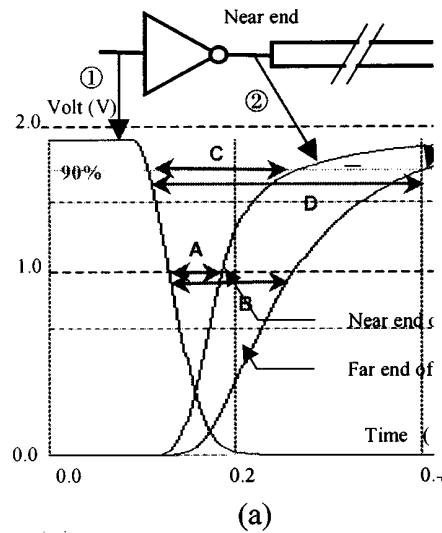
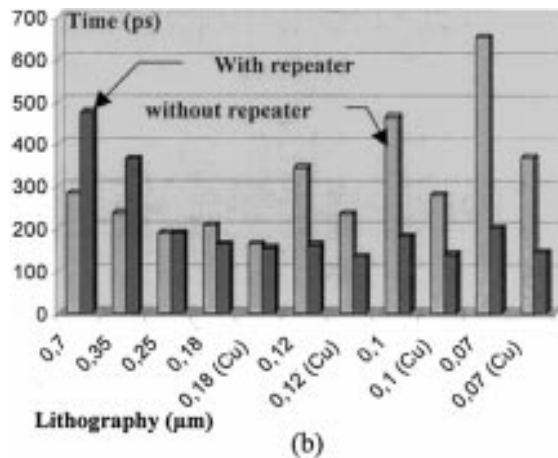


Fig. 4. Delay propagation definition and change with technology scale-down.

the overall capacity of the line remained almost constant with decreased inter-layer oxide thickness and reduced pitch. Repeaters are a good solution for keeping the interconnect delay within an almost constant range of 50 ps/mm.

C. Crosstalk

The increased role of crosstalk in technology scale-down is illustrated by means of three parallel interconnects, 3 mm long, in a single line or divided into three portions of 1 mm each using repeaters. Buffer size is the same as for the study of propagation delay. The signal “victim” is routed alongside the signals “aggressors,” using the minimum distance available in the technology (Fig. 5). Lateral capacitance induces a coupling which is the origin of crosstalk noise on the victim.

As seen in Fig. 6(a), the crosstalk effect is a parasitic shift of victim voltage due to a concurrent transition of the aggressor signals. The capacitance coupling is translated into a dangerous transient that may lead to a permanent fault if connected to a latch device of a precharge logic circuit. The 30% amplitude of the chip’s internal supply, called V_{DD} , is easily reached with a 3-mm interconnect in 0.25- μm technology. The

change in the crosstalk effect with technology scale-down is illustrated in Fig. 6(b). Using repeaters is again an efficient technique to reduce crosstalk. Also, the introduction of a low dielectric between conductors features a 20%–35% crosstalk reduction compared to high-dielectric oxide.

D. Crosstalk Delay

Crosstalk delay is a major contributor to timing uncertainty, to much greater degree than process variations and transistor derating described in [7]. The crosstalk delay effect has been the focus of interest in recent years, both from theoretical and experimental points of view. An illustration of its effect is provided in Fig. 7, based on the three coupled interconnects represented in Fig. 5. The simultaneous switching of the victim and the affecting signals may lead to a wide variety of phenomena, the most dangerous being the spectacular delay increase when the victim and the aggressor signals switch in opposite directions, starting with victim and then the aggressor some picoseconds later. The increase of crosstalk delay, in terms of the percentage of the typical delay without parasitic adjacent switching, is charted in Fig. 7(b) for several technologies. It can be seen that the crosstalk delay is increased significantly.

III. MEASUREMENT METHODS

Deep-submicrometer effects, from the point of view of both the device and the interconnect, have proven difficult to analyze in simple formulations. A huge amount of research has been devoted to modeling delay, crosstalk, and their combinations. Unfortunately, each technological generation produces more side effects and more complex configurations, which means that existing analytical formulations are no longer reliable.

Therefore, interconnect characterization from an experimental point of view has an essential role to play in the development and support of new processes and tools, as each new technology generation appears. This characterization relies on both physical and electrical measurements. Measurement approaches for signal integrity characterization within interconnects can be divided into four families:

- low-frequency probing testing;
- high-frequency methodologies such as $[S]$ -parameter measurements;
- e-beam testing;
- on-chip sampling techniques.

The first three are mostly external measurements, whereas the final approach involves direct timing measurement of the parasitic phenomena. The purpose of the following paragraphs is to present these techniques and provide some elements for comparison.

A. Probing Testing

This method, which consists of a direct probing on silicon, reduces the capacitance and inductance effect due to the probing via the packaging. Regardless of the quality and precision of the measurement equipment, the size of the on-chip metal area for the probe, around $10 \times 10 \mu\text{m}$, introduces

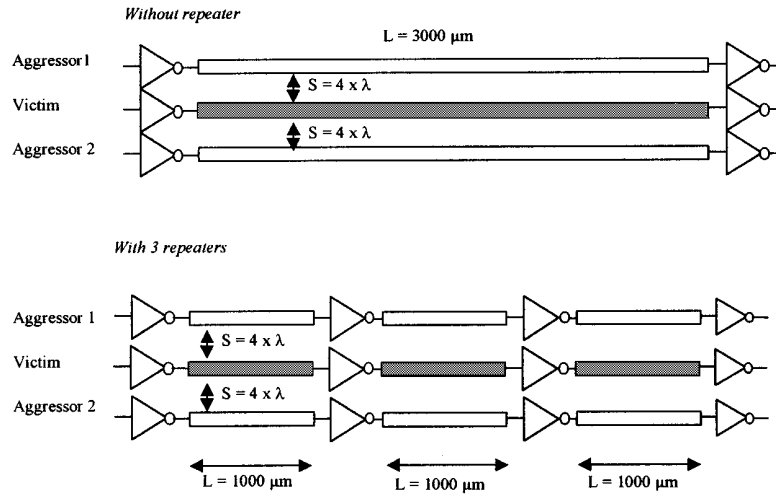


Fig. 5. Chain of coupled interconnects used to illustrate the crosstalk and crosstalk delay effects.

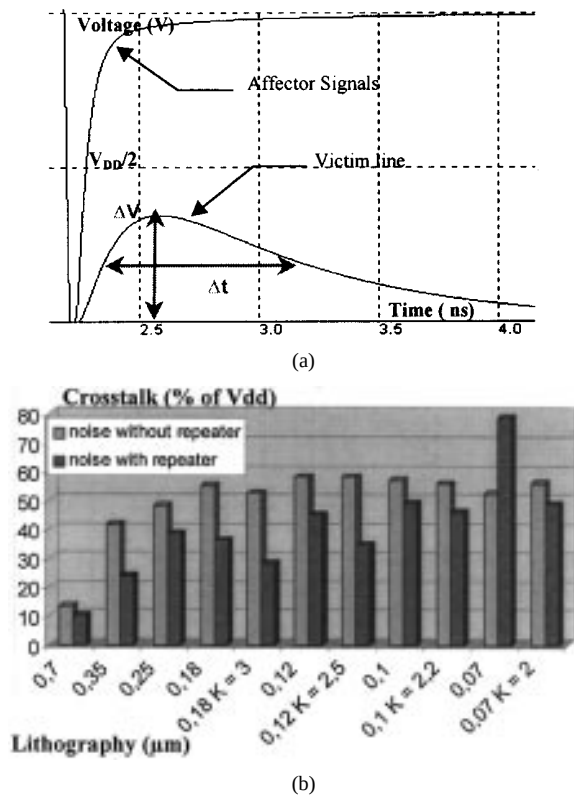


Fig. 6. Crosstalk definition and change with technology scale-down.

a parasitic capacitance. Moreover, the charge of the measurement system itself and the capacitances and inductances along the signal part inhibit the waveform for frequencies higher than a few hundred megahertz.

Recently, very high performance diagnostic systems, such as [9], have provided microprobes whose diameter can be as little as $0.1 \mu\text{m}$ for measuring signals in deep-submicrometer structures, with a probe landed directly on the interconnect (Fig. 8). Despite these advances, the system is perfectly suited to monitor slowly varying signals, but fails in measuring fast transients involved in crosstalk effects.

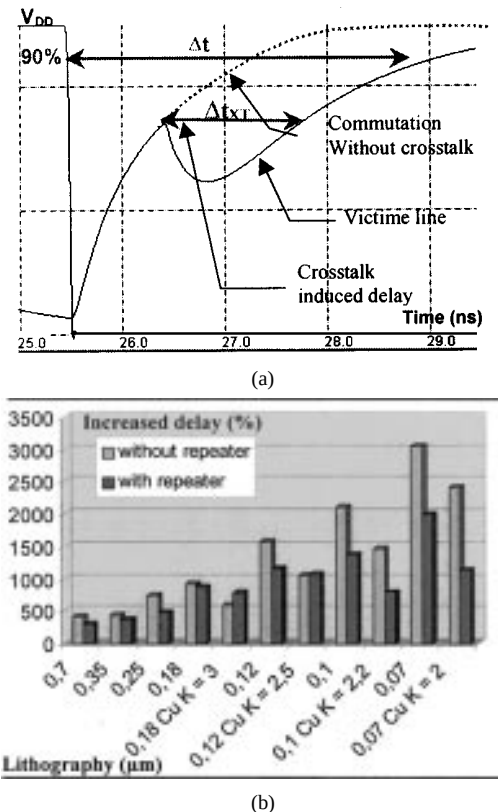


Fig. 7. Crosstalk delay definition and its increase with technology scale-down.

B. High-Frequency Methodologies

Eo and Eisenstadt [10] proposed an approach to determine the characteristic impedance of printed transmission lines at high frequencies, including the conductance effect of the line and the capacitance variation due to varying permittivity. This method determines Z_0 by comparing the transmission line's scattering parameters measured by a probe-tip calibration with those of an ideal transmission line. However, the probe-tip calibration measures not only the scattering parameters of the line, but also those of the contact pads or

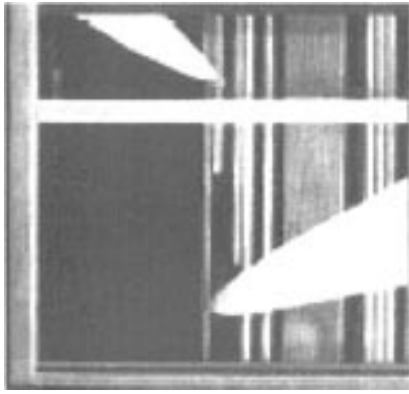


Fig. 8. IDS user interface showing two probes landed on 0.4- μ m-wide interconnects.

other unaccounted for transmission parasitics. Many studies have been carried out to separate the real Z_O value and noise [11]–[13] using special algorithms or measurement skills, but these require great expertise, a long calibration time, and very expensive equipment.

These methodologies are now widely used in integrated circuits because, until now, they have been the only way to obtain high-frequency characterization (>50 GHz) of submicrometer interconnects by giving the interconnect $[S]$ matrix.

Time-domain measurement techniques like time-domain reflectometry (TDR) are widely used in industry for the determination of high frequency behavior of interconnects. Although this method succeed in characterizing the package and printed circuit board track impedance, the crosstalk effects between on-chip interconnects cannot be characterized precisely using the TDR approach.

C. E-Beam Testing

The high performance of electron beam testing for integrated circuit verification and failure analysis has been shown in a number of publications [14]. The advantages of this contactless method come from its ability to access a high number of internal nodes with virtually no loading effect, presenting high space and time resolution. Internal analog voltages can be observed and dynamic measurements at high frequencies are available using stroboscopy (beam blanking techniques based on a sampling principle).

Recently, 9-GHz-bandwidth e-beam testers with 40-ps accuracy have become available [9] which quickly and accurately assess the internal behavior in today's sub-0.18- μ m devices. The disadvantages of this equipment are the very high cost, the screening effect of the upper metal layers, the complexity of the test equipment, and the need for an off-chip triggering of the equipment.

D. On-Chip Measurements

Until recently, the characterization of interconnect behavior, in particular the propagation delay, was monitored by a direct probing on the wafer, using specific test structures and a low-frequency output signal, the most popular being the ring oscillator structures. The complete characterization of the process in 0.18 μ m would require thousands of such

structures to cover most configurations found in deep-submicrometer designs. Given the continually increasing process requirements for future devices and structures coupled with the equipment reliability, cost, and uptime requirements, interconnect characterization is slowly moving to on-chip.

On-chip sensors have been developed for interconnect capacitance measurements [15], [16] accurate to within 10^{-15} Farad. Other techniques, such as that developed in [17], allow for the characterization of crosstalk-induced delay by indirect monitoring via a latch.

To accurately characterize structures that closely mimic interconnects in leading-edge high-speed design, the authors of [18] and [19] have proposed on-chip sampling systems able to measure interconnect delays and coupled parasitic effects. The approach developed in our laboratory, in cooperation with major IC foundries in Europe [20] is based on an on-chip sample-and-hold circuit called an “on-chip oscilloscope” that probes the voltage directly within the interconnects. The schematic diagram of the sampling sensor is shown in Fig. 9. An external synchronization (“*Synchro*”), is used to trigger off a phenomenon, which is sampled by a transmission gate switch after an externally controlled delay (“*Vanalog*,” “*Vplage*”). The sampled analog voltage is stored in a capacitance before being amplified and exported out of the chip (“sampled data”). The sampling cycle is repeated for a range of delays until the waveform is reconstructed.

The targeted phenomenon may consist either of the simple switching of a line, to characterize the propagation delay, or the switching of coupled lines, to investigate crosstalk and crosstalk delay. The way this phenomenon is sampled is detailed in Fig. 10(a). Each time the “*Synchro*” signal rises, the phenomenon appears. At the same time, the sampling signal displays a delay of Δt_i . This delay depends on the “*Vanalog*” voltage applied to the input pad, as can be seen in the same figure. At the rising edge of this sampling signal, the transmission gate remains off and the value of the sampled fluctuation is stored in a capacitance. The input capacitance of the follower is small, but nevertheless plays the role of an analog memory for some microseconds. The captured analog value is copied by the follower and is sampled by an on-chip or external analog-to-digital converter. The repetition of this procedure for a set of different values of “*Vanalog*” can provide, thanks to the delay law, an accurate reconstruction of the phenomenon waveform while remaining within the limits of frequency and temporal resolution of the sensor. Fig. 10(b) shows the delay law versus “*Vanalog*,” featuring a good linearity and the possibility of tuning the delay range in order to adapt to the duration of the phenomenon.

In 0.18 μ m, our system features a 25-GHz bandwidth, a parasitic capacitance less than 10 fF, and has proven to be efficient in characterizing delay, crosstalk, and crosstalk delay. Furthermore, the on-chip approach only requires a simple calibration circuit and measurement technique.

E. Comparison Between Measurement Techniques

To achieve a complete signal integrity characterization for deep-submicrometer technology, the ideal test methodology should provide a wide bandwidth, good amplitude, and time

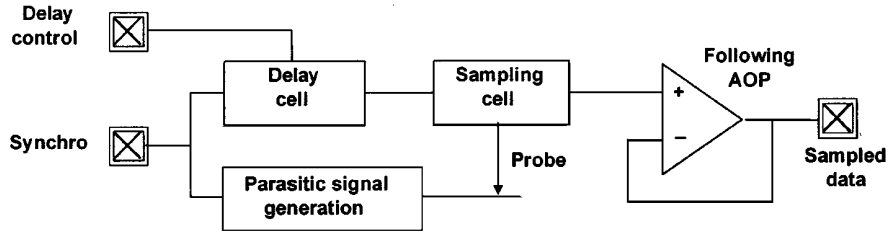


Fig. 9. Basic principles of the sampling sensor.

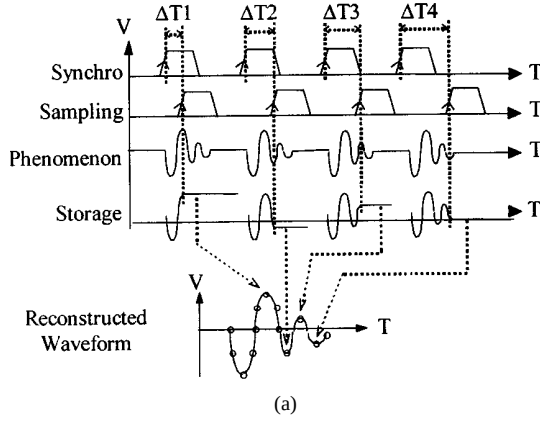
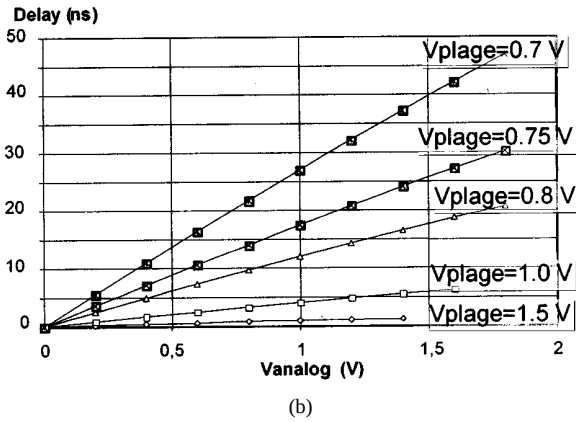


Fig. 10. (a) Waveform construction using sampling technique. (b) Measured dependence between analog external controls and the delay law of the sampler.

resolution and should be able to measure signal propagation, crosstalk parasitic glitches, and crosstalk-induced delay. A low-cost and relatively simple test procedure would be a major argument for the choice. The methodology should be reusable with technology scale-down. Finally, the measurement should be possible directly on the wafer, in a short time inside the foundry, without human interaction, and applied to a wide number of wafers.

Table 2 details the performances, costs, complexity of the test procedures, and results obtained for each method reviewed in the above paragraphs.

Standard test equipment cannot obtain such performances because of the limitation of the package and the parasitic capacitance introduced by the measurement system itself. The best solution involves using on-chip methods that take advantage of technology scale-down for their own operation.

IV. SIMULATION ISSUES

A. Line Parameter Extraction

A high level of accuracy for interconnect model parameters basically resistance, capacitance and inductance is more and more difficult to achieve with technology scale-down. This is mainly the consequence of increased metallization layers, the complexity of the interconnect structure itself, and the increased operating frequencies. The resistance cannot be evaluated by counting elementary squares and applying a simple ohm-per-square value, because the use of titanium barriers with very high resistance make the sheet resistance dependent on the interconnect width.

Concerning capacitance, the situation is even worse. As the interconnect structure gets more complicated, the extraction of the exact value of both the capacitance referring to ground and the crosstalk capacitance with neighboring signals is a huge task. The 2-D extraction involves analyzing the geometrical surface, length, and coupling distances to parallel tracks. The precision achieved using such a technique is often less than 25% of the exact capacitance in 0.18- μm technology, due to several coupling effects with upper or lower wires, corners, and vias. Consequently, methods known as 2.5-D approaches try to identify for each net the elementary structure that has been previously characterized in 3-D, using precise tools such as finite-element methods. Hence, the capacitance may be extracted with a very high degree of accuracy, at the cost of a huge database of 3-D elementary configurations and heavy finite-element preprocessing of each configuration. All this work has to be performed again for each technological improvement, however minor, which represents one of the most important bottlenecks in the realistic extraction of the capacitance. The alternatives are statistical approaches, in which no accurate extraction is done, replaced by the use of much more simple approximations.

B. Line Modeling

Accurate interconnect simulation is needed to achieve prediction of deep-submicrometer technologies, particularly as their parasitic effects are one of the key issues for timing performance and can provoke critical logic faults. Let us consider a line with static resistance R , capacitance to ground C , and inductance L . It is currently accepted that distributed RC models (T or Π) are an accurate way to model transmission line effects. Some authors have pointed out the importance of the inductance [7], specifically for short interconnects with high-drive capabilities, or for power interconnects with sharp variations of current. Elmore shows [21] that the accuracy

Table 2
Comparison Between Various Test Methods

Methods	Probing testing	[S] parameters	Capacitance measurement	E_Beam	On-chip [$\leq$ ref] [add tech]	On-chip [ref] [add tech]
Bandwidth	<1 GHz	70 GHz		9 GHz	10 GHz	25 GHz
Resolution			100 aF	100 mV / 40 ps	20 mV / 15 ps	10 mV / 5 ps
Cost	High	Very High	Low	Very High	High	Low
Set-up	Long	Complex	Simple	Complex	Simple	Simple
Measurement	External	External	On-chip	Local	On-chip	On-chip
Results	Dynamic	Impedance	Capacitance value	Dynamic	Dynamic	Dynamic
Power supply Fluctuation	No	No	No	Yes	No	Yes
Crosstalk	Yes	Yes	Yes	No	Yes	Yes
Propagation	Yes	Yes	Yes	Yes	Yes	Yes
Crosstalk induced delay	Yes	No	Yes	No	Yes	Yes
In-fab on-line testing	Easy	Difficult	Easy	Very difficult	Easy	Easy

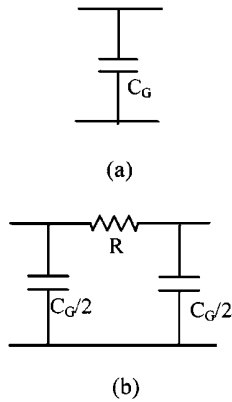


Fig. 11. Models used for simulation of propagation delay.

of a distributed model is highly dependent on the number of basic cells. The problem is how to choose correctly the amount of discretization given that model accuracy increases in direct proportion to the number of basic cells.

We propose to study the accuracy of the models from the basic C model [Fig. 11(a)] to the CRC [Fig. 11(b)], CRLC [Fig. 11(c)] and distributed CRC and CRLC models [Fig. 11(d)] for various technologies from 0.7 μm to 0.1 μm . In all the simulations, the most powerful buffer of the technology library has been used with the scaling factor λ , representative of the technology (2λ = minimum grid length) and the interconnect characteristics define in Table 1. The simulation results obtained are presented in Fig. 12 which focuses on two accuracy ranges, 10% [Fig. 12(a)] and 5% [Fig. 12(b)].

In the upper histogram, the C model is 10% accurate up to a length of 2000 μm in 0.18- μm , but only 300 μm in 0.10- μm . With a target of 5% accuracy, the need for a CRC model appears starting at 800 μm in 0.18- μm and 180 μm in 0.10- μm . Furthermore, three distributed cells are mandatory to achieved 5% accuracy for interconnects longer than 2000 μm , in 0.1- μm technology. In these histograms, the role of inductance is far less important than that of resistance (note that inductance effects are limited by the use of narrow interconnects in this study).

Studies have been carried out to estimate the error reduction depending on the number of basic distributed cells [22]. The studies of Vanier and Deschacht [22] give formulations to simplify a distributed model into a single cell as described in Fig. 13, where a corrective factor α , taking into account both the geometrical dimensions of the line and the drivers, is inserted. The formulations of α , for a falling edge α_{Fall} or a rising edge " α_{Rise} " give the delay propagation at $V_{dd}/2$ shown as

$$\alpha_{\text{Rise}} = \left(1 - \frac{\tau_{\text{st}}}{\tau_{\text{st}} + 2 \ln(2) \mathbf{R_L} \mathbf{C_N}} \right) \quad (1a)$$

$$\alpha_{\text{Fall}} = \left(1 - \frac{\tau_{\text{st}} \cdot \mathbf{C_P} / \mathbf{C_N}}{\tau_{\text{st}} \cdot \mathbf{R}(\mu) + 2 \ln(2) \mathbf{R_L} \mathbf{C_P}} \right) \cdot \quad (1b)$$

The recent work of Ismail and Friedman [7] introduces formulations including the inductance effect and proposes a parameter ζ that can be used to characterize the inductance effect more accurately. Looking at the driver resistance used in this paper, it confirms that the L effect has no insignificant impact on propagation. If we consider conventional routing wires, the parameter ζ is generally higher than

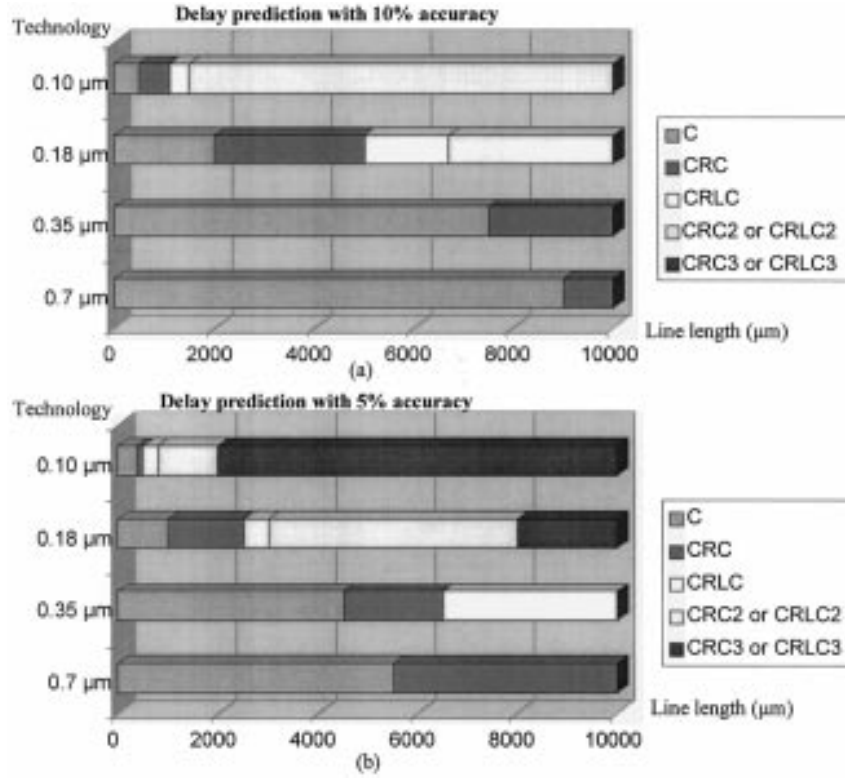


Fig. 12. Definition of a simulation model depending on the technology and the accuracy.

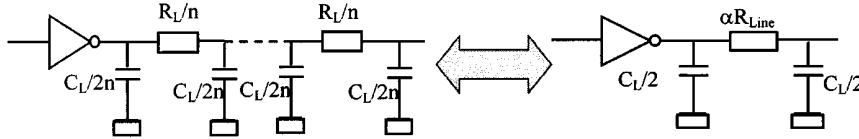


Fig. 13. From a distributed model to a corrected nondistributed one.

1, which means that the slope of the commutation is slightly modified but does not significantly affect the overall delay.

C. Signal Integrity Prediction

Faced with the complexity of simulating the full chip, the tendency is to make a post-physical-design interconnect extraction from the layout to verify that performances are met. A conventional approach for these extraction tools is based on multiple steps which are represented in Fig. 14(a). The first step of the procedure is to extract and calculate the parasitic C , R , and L parameters of the interconnect structures using electromagnetic solvers. To accelerate this procedure an alternative to the RLC full-chip computation is usually to use precharacterized interconnect models based on a set of 3-D structures.

If these structures are not defined, the parasitic interconnect extraction requires 3-D electromagnetic computation. The second step is to make an analog simulation of all nets with the accurate model. Postprocessing is then required to process the huge amount of amplitude and timing information needed and identify the nets with critical signal integrity problems, which requires redesigning.

Even if interconnect models are becoming more and more accurate, a full circuit simulation, while achieving very high accuracy, is often too slow to be practical. An alternative is to replace simulation by direct estimation of noise and timing based on analytical formulations from R , C , L parameters. A number of simple models for interconnects and drivers have been developed to allow for faster timing analysis [see (2a)] and crosstalk prediction [see (2b)] without much loss of accuracy

$$t = 0.43RC_{eq} + 0.92(RC_{cheq} + R_D C + R_D C_{cheq}) \quad (2a)$$

where t is the propagation delay, R is line resistance (Ω), C_{eq} is total capacity of the line (F), C_{cheq} is charge capacitance, equivalent to the output grid capacitance (F), and R_D is equivalent resistance of the input buffer (Ω).

$$\Delta V = V_{dd} \frac{C_x}{1 + C_x} \frac{1}{1 + x} \quad (2b)$$

with

$$C_x = \frac{C_{12}}{C_{victim}}, \quad x = \frac{W_{victim}}{L_{victim}} \frac{L_{affecter}}{W_{affecter}}$$

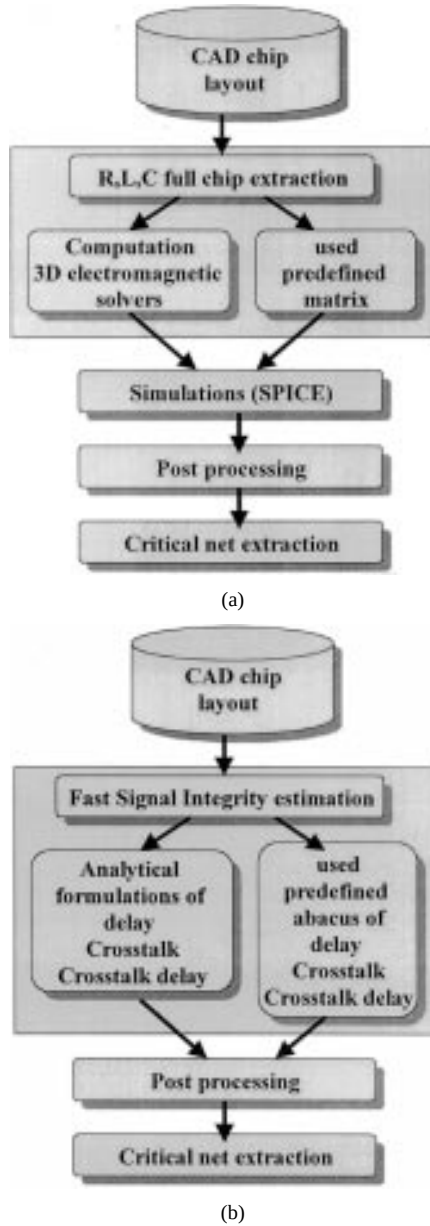


Fig. 14. Signal integrity prediction methodologies.

where V_{dd} is supply voltage (V), W is equivalent MOS width (μm), L is MOS length (μm), C_{victim} is capacitance of the victim interconnect to ground (F), and C_{12} is crosstalk capacitance between victim and aggressor (F).

However, with increasingly tight timing specifications and increasing interconnect length and buffer strength, a number of deficiencies have been observed in the accuracy of models used today. Until now most of these models have been based on elementary interconnect configurations which do not represent real-case routing and switching configurations. More precise and updated models are given by Sylvester in [23].

It is not clear whether incremental model improvements will be sufficient to take into account all the configuration possibilities for chips with several million transistors and thousands of meters of interconnects used in today's fast-

evolving technology. Future work is needed to clarify the limitations of current models and to create improved models that can scale to giant complexity (1 billion transistors).

One solution is to establish a whole set of abacuses for a direct and fast estimation of all the parasitic phenomena which are representative of one technological process. What we propose, therefore, are abacuses which takes into account both the "simultaneous transistor and interconnect sizing" (STIS) for delay prediction, and the global interconnect sizing for crosstalk prediction (GISC), which have been properly defined by Cong [3]–[5].

Consequently, these abacuses must be included in the design rules manual and have to be defined at the early level of technology setting to schedule the design flow environment. These abacuses can be obtained by preprocessing simulations, but must be confirmed by direct measurement to ensure validity. What we propose is a complete on-chip time-domain measurement to establish the abacuses with high precision.

V. IMPLEMENTATION OF TEST STRUCTURES ON A 0.18- μm CMOS TECHNOLOGY

Within the framework of a consortium of several European companies, a test chip has been developed for a 0.18- μm CMOS technology process characterization. The chip includes patterns for precise timing measurements of delay propagation, crosstalk noise, and crosstalk delay to implement a whole set of abacuses for designer guidelines. The same pattern, called "Signal Integrity System Measurement" (SISM), is used for all these measurements.

A. Principle of the Signal Integrity System Measurement (SISM)

Using the sampling technique previously described in brief, a set of patterns has been developed for signal integrity characterization. The schematic diagram of the basic SISM pattern is shown in Fig. 15. The main objective is to be able to measure directly in a single pattern the propagation delay, the crosstalk coupling, and the crosstalk-induced delay.

The buffer sizing, the synchronization of the signals, and the number of aggressors coupled with the victim line are also taken into account. These requirements provide a full back-end technology calibration to establish design rules and line modeling for CAD tools, and a system called "Signal Integrity System Measurement" has been developed to control wires and buffer strength (Fig. 15).

The complete SISM system is able to control five coupled lines as shown in Fig. 16 and consists of two main parts, the 4-probe sensor, and the "Switching controlled system," both of which controlled by external voltages. The 4-probe sensor, has been developed based on the sampling system measurement, and is directly connected at the beginning and at the end of the aggressor line 2 and the victim line. The results are amplified using two follower amplifiers, and one signal called "Selection" allows for a choice between two probes. To obtain a full range observability—from V_{SS} to

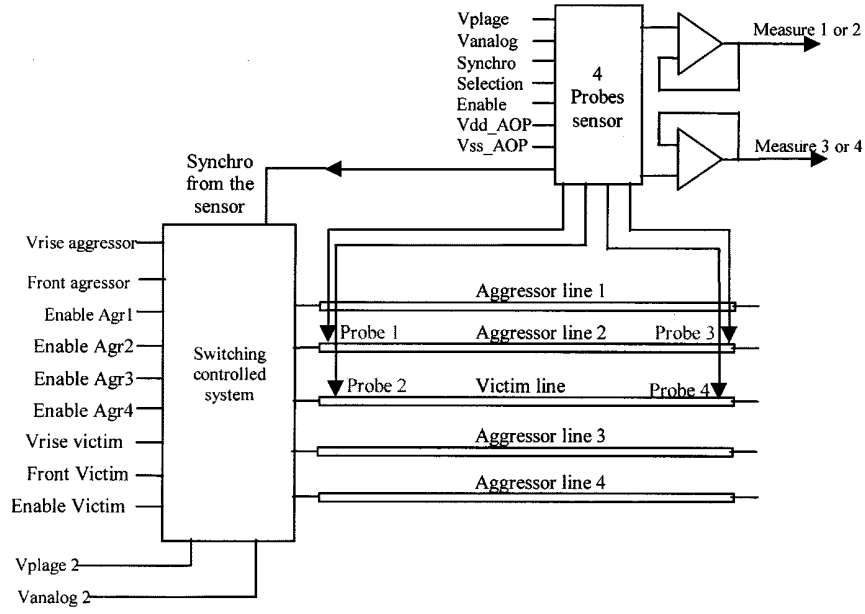


Fig. 15. Principle of the SISM.

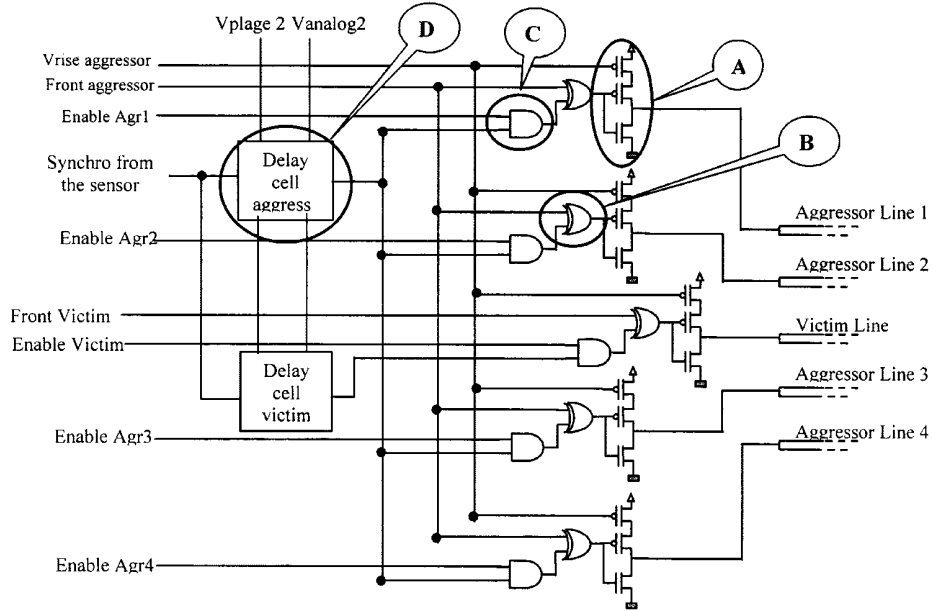


Fig. 16. Schematic diagram of the system, which controls the five lines.

V_{DD} —the power supply has been ranged from V_{ss_Aop} to V_{dd_AOP} (typically -0.5 V to 2.5 V).

The line system control has to carry out the overview of the STIS and the GISC by an accurate control of the line. This system is detailed here (Fig. 16) with each active part, A, B, C, and D.

In Fig. 16, part A is an inverter with a controlled rising edge from 50 ps to 20 ns via the analog signal “Vrise,” used to study the influence of the buffer size connected to long interconnects. This could also help in the verification of multiple formulations for CMOS buffer tapering with interconnect capacitance [24], [25] or in the modeling of crosstalk from aggressor buffer size [26]. Table 3 gives the equivalent

transistor size depending on the analog control “Vrise.” In a first approximation, the PMOS transistor can be considered a current source controlled by the “Vrise” grid voltage according to the following formulation, considering that the PMOS transistor is in saturated mode

$$I_P = \frac{K_p}{2} \frac{W_p}{L_p} (V_{rise} + V_{Tp})^2 \quad (3)$$

where I_P is the current (A), K_p is a technological constant, around $350 \cdot 10^{-6} \text{ A} \cdot \text{V}^{-2}$, W_p is the channel width in μm (here around $10 \mu\text{m}$), L_p is the pMOS channel length ($0.18 \mu\text{m}$), V_{rise} is the control voltage (V), and V_{Tp} is the pMOS threshold voltage (-0.4 V).

Table 3
Emulation of Various Buffer Strengths

Vrise (V)	Width (μm)	Length (μm)
0	27	0.18
0.8	10	0.18
1.1	5	0.18
1.3	2	0.18

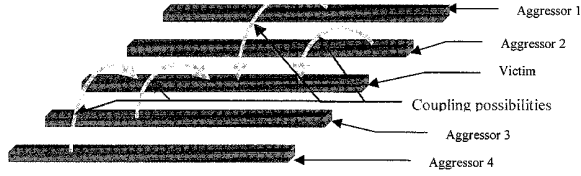


Fig. 17. Coupling possibilities allowed.

Part B (Fig. 16) is an XOR gate which allows for the choice of the active edge of the selected line. The main goal is to measure propagation delay or crosstalk depending on a rising or falling edge, but also the crosstalk delay by an opposite switching configuration. Part C is an AND gate which enables the chosen line to be activated for simple, double, or multiple crosstalk as illustrated in Fig. 17.

Finally, two delay cells (part D) called “delay cell aggressor” and “delay cell victim,” both of which are controlled by external analog voltages, introduce or not a delay on the active edge of the lines to perform measurement of crosstalk delay versus shift delay. The delay cell is based on a pass PMOS transistor and a pull-down NMOS transistor which exhibits a quasi linear delay dependence on the gate voltage. The principle here is the same as that used in the sampling system, and two added analog voltages allow for delay control introduced only on the four aggressor lines. The delay on the victim line is refereed to zero (“*Vanalog*” and “*Vplage*” directly connected to ground). The total layout of the structure is shown in Fig. 18.

The SISIM has been used to calibrate a six-metal-layer 0.18- μm CMOS technology. Six pitches have been investigated, as listed in Table 4. Within each pitch, six patterns have been implemented with various length and spacing as detailed in Table 5. Four configurations of length 0.3, 1, 3, and 10 mm and two variations of the spacing from two time to four times the basic spacing, allowing a full interconnect characterization of the parasitic phenomena. These 36 patterns have been implemented for the complete characterization of the technology process.

All studies concern measurements taken on the metal three layer, which is confined between a grid made of upper lines of metal 4 and lower lines of metal 2, as shown in Fig. 19. The density of the grids (named *Grid spacing* in Fig. 16) has been chosen to be representative of the statistical routing density of such a technology.

The test vehicle is controlled by external static voltages which are the same for all 36 patterns. A total of 20 vectors must be set to carry out the required measurement. Only one pattern is active at any time, thanks to appropriate enable

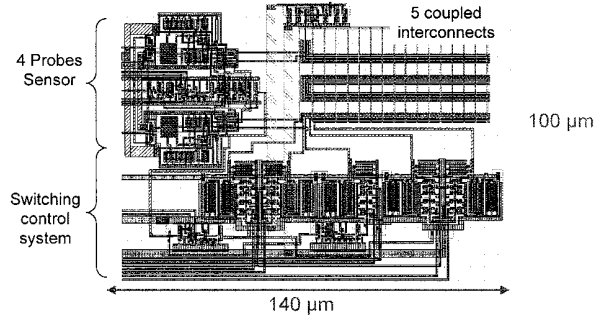
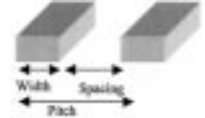


Fig. 18. Layout of the full SISIM.

Table 4
Pitch Used for the Various Configurations

NAME	PITCH	WIDTH	SPACING
C000	1 μm	0.5 μm	0.5 μm
1471	1 μm	0.4 μm	0.6 μm
1472	1 μm	0.6 μm	0.4 μm
1480	0.8 μm	0.4 μm	0.4 μm
1481	0.8 μm	0.48 μm	0.32 μm
1482	0.8 μm	0.32 μm	0.48 μm



circuitry. The same enable command activates each pattern output separately on a multiplexed analog output pad.

B. Commutation Abacus

In Section III, we have already emphasized the importance of correctly evaluating the propagation delay on long interconnects, depending on wire-sizing and buffer-sizing to solve the STIS problem properly. Using the four primary patterns of Table 5, delay versus line length and buffer strength variations can be analyzed. To achieve thus, the correct value of “*Vrise*” has to be set and the “*EnVictim*” signals disabled. All the other signals of the switching control system must be set at zero. By activating the victim line and by measuring at probes 2 and 4, the near-end and far-end signal waveforms can be obtained, and thus the increased delay. Four values of “*Vrise*” are used to compute the impact of buffer sizing. An example of the measurement compared with the CRC simulation Fig. 20 gives the propagation delay abacus depending on line length and buffer strength.

C. Crosstalk Noise Abacus

Various types of crosstalk abacuses can directly be extracted from the SISIM. The first could be noise amplitude depending on the coupling length and spacing, considered with various switching possibilities from only one active aggressor to four active aggressors. This can be achieved by measuring the two added patterns of Table 5 which are the simple spacing multiplied by 2 and 4. The same approach could be aborted considering also the dependency on buffer strength. These studies can provide a full overview of the GSIC as well as STIS for establishing design rules by extracting the measurements of probes 1, 3 and 2, 4. Here, probes 1 and 3 extract the crosstalk noise at the beginning and end of the victim line. Two other cases will appear while

Table 5
Basic Configurations for Interconnect Characterization for all Pitches

NAME	DETAILS	DESCRIPTION
XXX_L03_S1	Metal3 on M2/M4, spacing = 1pitch	Metal 3
XXX_L1_S1		Minimum spacing, pitch = 1 (1 pitch = 1 μm)
XXX_L3_S1		4 configurations of length 0.3 mm, 1 mm, 3 mm and 10 mm
XXX_L10_S1	Metal3 on M2/M4, Length = 3 mm	Metal 3
XXX_L3_S2		Length of line fixe = 3 mm
XXX_L3_S4		4 configurations versus various spacing, pitch = 1, 2 and 4

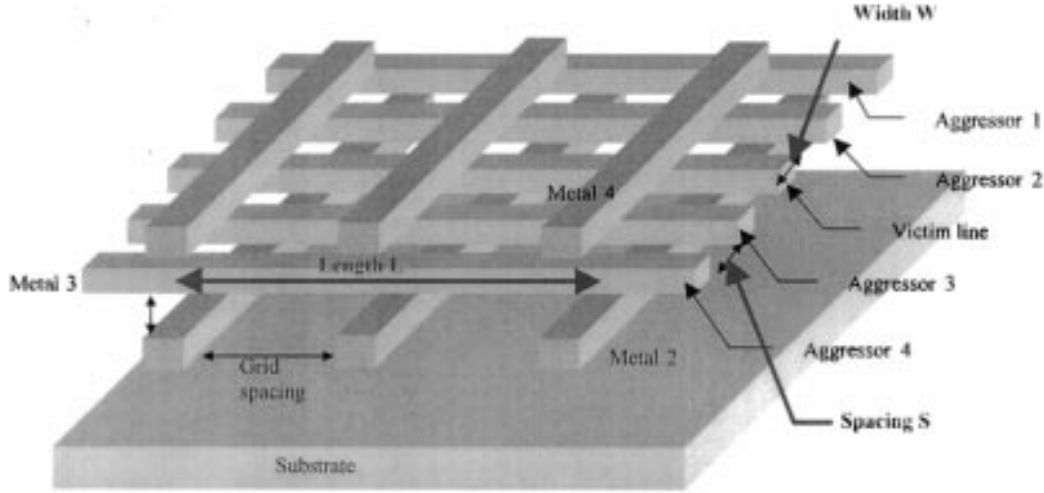


Fig. 19. 3-D representation of the line configuration.

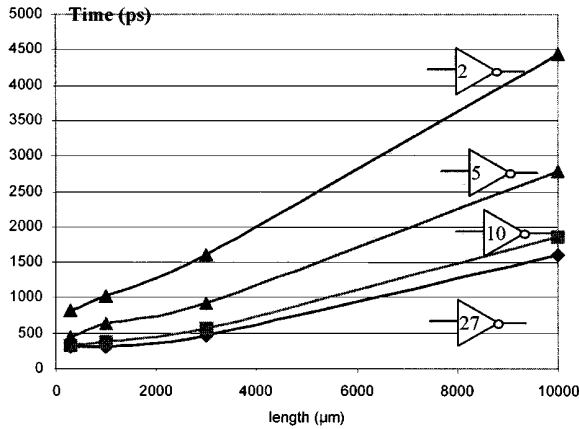


Fig. 20. Timing measurement and measured abacus of delay propagation.

the victim line is set to V_{DD} in the same way, which extend the crosstalk cases studies to four.

These results are obtained using the same measurement methodology as described previously except that the victim line (line 2) is set at 0 V or V_{DD} .

Fig. 19 shows the coupling possibilities that lead to the SISM. This configuration could correspond to the emulation of a logic bus, and the study concerns the effect of the number of switching lines on the amplitude of the crosstalk noise. To carry out the measurement, the victim line is considered to be line 3, which had to be set at V_{SS} or V_{DD} . The choice of

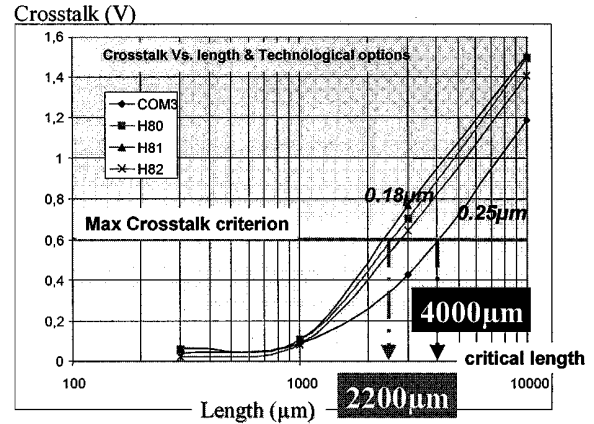


Fig. 21. Crosstalk noise depending on length of line and pitches.

switching line is decided by activating or not the enable signals "Enable-AgrX." Results are represented in Fig. 21 in the most critical coupling case where crosstalk noise depending on the length of the line is given for various pitches.

If crosstalk noise becomes higher than 30% of V_{DD} some logic gates at input voltage around 30% of V_{DD} may switch. Certain criteria such as maximum allowable routing length avoid coupling faults (2200 μm for the 0.18- μm pitches, and 4000 μm for 0.25- μm pitch).

The 3-D graph presented in Fig. 22 gives an overview of crosstalk noise amplitude depending on line length, spacing between lines, and buffer strength in the most critical cou-

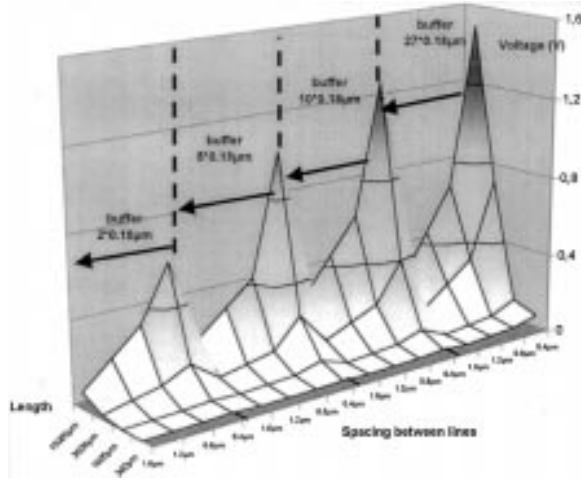


Fig. 22. Increase in crosstalk noise depending on line length, spacing between lines, and buffer strength (worst case coupling).

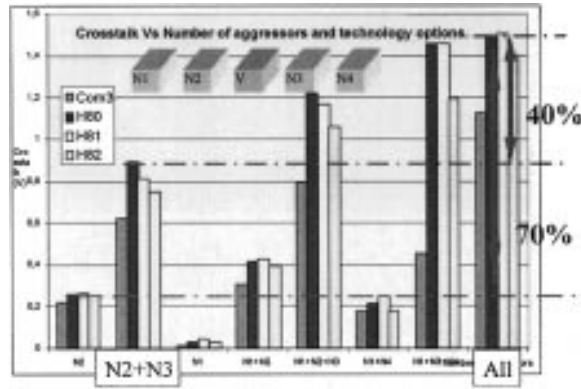


Fig. 23. Impact of number of aggressors on crosstalk noise amplitude.

pling case where the four aggressors switch simultaneously. To determine the impact of the number of aggressors, the histogram of Fig. 23 represents the crosstalk noise amplitude versus the coupling possibilities. It appears that in the worst case, in which the four aggressor lines are switching together, crosstalk is 70% higher than when one nearest victim line is switching, and 40% higher than when the two nearest victim lines are switching.

D. Crosstalk Delay Abacus

To proceed to crosstalk delay measurement, the same methodology as for crosstalk measurement is used, but an opposite commutation is introduced on the victim line, and the aggressor lines are slowly shifted. The signals “Vplage2” and “Vanalag2” are the analog controls of the delay cell which is directly connected to the logic line control system.

The abacus representative of the crosstalk delay phenomenon could be the increased delay referred as to the delay without crosstalk, depending on wire and buffer sizing, as has been developed previously, but also depending on the synchronization between the lines (Fig. 24). The delay between the commutation of lines 1 and 2 is directly extracted

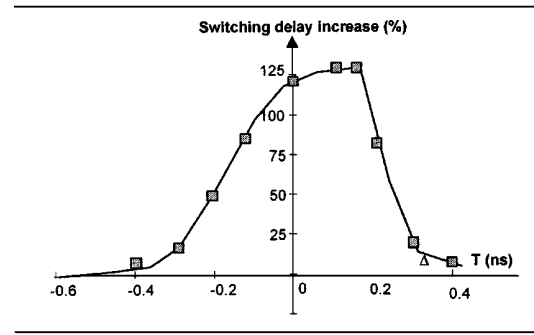


Fig. 24. Abacus of the crosstalk delay depending on the shift delay ($0.18 \mu\text{m}$).

from the delay law. As for the crosstalk study, four cases have been considered depending on the active edges.

VI. SPECIAL APPLICATION NOTES, DESIGN RULES, TOOL IMPLEMENTATION

Current problems of signal integrity can only be solved at the first level of the technology setting. The creation of a chip encompasses a set of design states, called design flow, summarized in Fig. 25. Even if manufacturing processes include new materials such as copper and Low K, interconnect parasitic effects are becoming predominant. A set of abacuses representative of a process technology is therefore the key to reducing chip manufacture time. The Signal Integrity System Measurement requires a large number of timing tables of delay, crosstalk noise, and crosstalk delay which can be used at different stages of the design flow.

A. Design Rules

The first stage in the design flow process is to establish a manufacturing procedure which defines the design rules. Until now the crucial problem in incorporating the interconnect parasitic effect into the design rules laid down by the designer has been the lack of information. Information are in general restricted to the capacitance matrix, which in itself is not very useful.

Our proposal is to provide rules for interconnect sizing and buffer sizing for fast overview and accurate estimation of delay, crosstalk, and crosstalk delay. The propagation delay model is based on on-chip measurement and compared with precise simulation using 3-D finite element methods. The rules are given for minimum routing pitch allowed, with interconnect crossing lines in upper and lower metal layers representative of the statistical crossing density of the process. For each metal layer, graphic laws are given together with mathematical formulations taking into account line length and buffer size. The analytical formulations must be simple and easy to use for the designers (by using basic calculations) who are not necessarily familiar with modeling signal integrity.

Including such measured abacuses as the one presented in Fig. 17, it is quite easy to calculate the delay depending on length (L) of the line and on buffer size (W_D). An equivalent

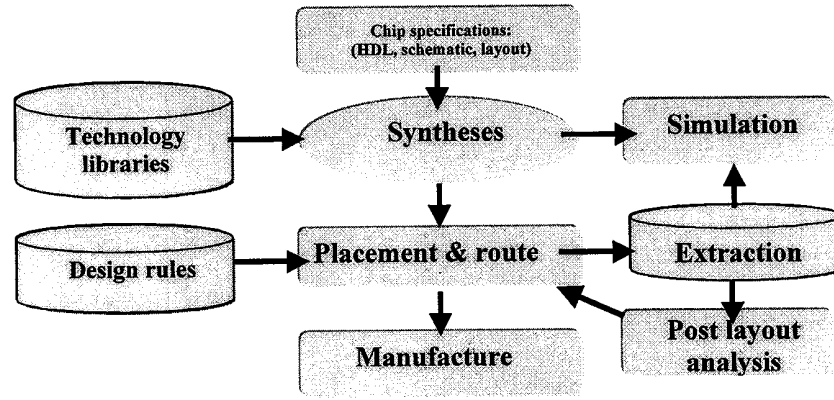


Fig. 25. Summary of the design flow.

equation of such an abacus would be $\Delta t = aL + b$, where a and b are functions of $W_D f(W_D)$.

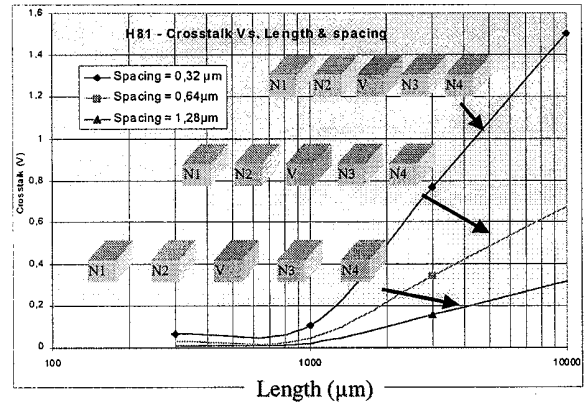
Concerning crosstalk, two kinds of abacuses may help the designers (Fig. 26), and the corresponding equation might be $\Delta V = aLn(L) + b$ where a and b must be referred to W_D and S is the spacing.

A bus configuration consists of a victim and more than one aggressor, as shown in Fig. 27(b). This configuration may generate several more couplings than configuration (a) due to the reduction of the dynamic capacitance of A1 and A2. Consequently, A1 and A2 switch faster and increase crosstalk, as seen in Fig. 28. The model must include capacitance, inductance, and resistance, and buffer sizing must be handled with care to provide chip performances. For each bus configuration model, graphic laws are given, together with mathematical formulations (Fig. 25) taking into account the number of aggressors.

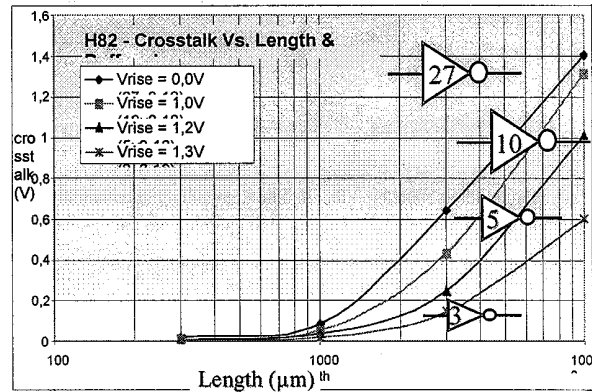
B. Place and Route Aided Design Strategy

The second stage in the design flow process which is susceptible to modification concerns place and route level. This operation consists of using a dedicated algorithm to automatically place cells from technology libraries and to connect them to interconnects in accordance with design rules. Industrial constraints have lead to software improvements by introducing dedicated algorithms which take into account timing performances and crosstalk-free routing. Even if software improvements are considerable, they must be fed by technological data which up to now are restricted to capacitance tables which for the most part are not really representative of the interconnect parasitic effects. Moreover, the implementation of tables containing capacitance information requires a lengthy environmental setup process which must be updated from one technology to another.

An alternative is to define criteria such as the maximum routing length to avoid or minimize timing and crosstalk problems by regularly introducing repeaters. We propose here a possible algorithm for place and route strategy by regarding various constraints such as timing and crosstalk noise based on the abacus obtained by the SISM. Our goal is to improve timing performance while maintaining crosstalk immunity (Fig. 29).



(a)



(b)

Fig. 26. Crosstalk abacuses depending on length, spacing, and buffer sizing.

L_{nece} values and t_{nece} appear in this flow chart, corresponding respectively to the interconnect length needed to connect two gates and to the corresponding propagation time.

The principal criterion is to respect the crosstalk constraints by fixing the maximum lengths of routing (L_{max}) according to the various buffer sizes. The second criterion is the travel time on an interconnection (t_{max}) fixed by the designer. This technique is based on the "preestimation" of propagation delay and crosstalk coupling phenomena using the proposed abacuses (in grey).

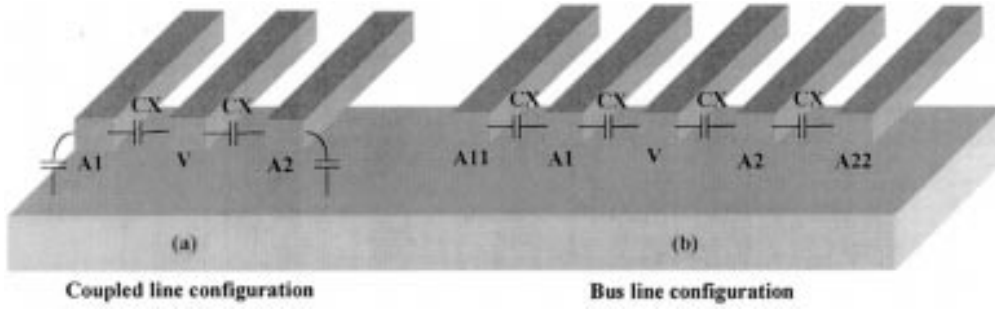


Fig. 27. Coupled line and bus configuration.

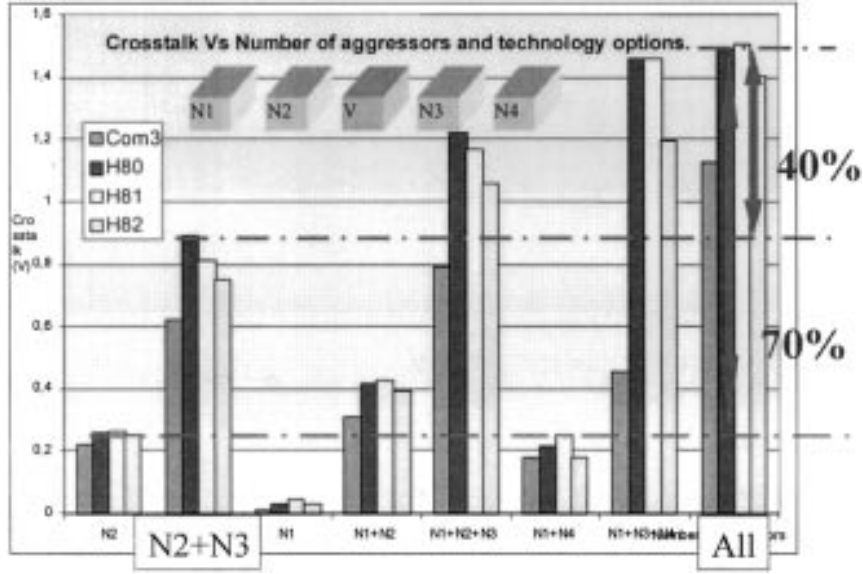


Fig. 28. Crosstalk versus number of aggressors.

As soon as L_{nece} or t_{nece} values reach the L_{max} values or t_{max} , we propose the insertion of a repeater. The choice of the dimensions for this repeater is also made in correlation with the abacuses to respect the defined criteria. In theory, the application of this type of algorithm should not prevent further problems of logical faults generated by crosstalk coupling while at the same time optimizing the timing performances and the silicon surface.

The application of this algorithm can be illustrated by means of a simple example represented in Fig. 30. Two inverters separated by 8 mm are connected in a bus configuration constraint at minimum spacing. The equivalent output buffer of the first inverter is a $5 \times 0.18 \mu\text{m}$ NMOS transistor, and the propagation time between two cells does not exceed 1 ns. For this application, only two abacuses are required. The first is delay increase depending on the buffer strength, and the second is crosstalk noise depending on line length and buffer strength.

In such a configuration, the estimated delay is 2.5 ns with a crosstalk of around 0.9 V ($V_{DD} = 2$ V). The first action will be to respect " L_{max} ," which will cause a repeater to be inserted at 2 mm. The new distance necessary is now " $L_{nece} = 6000 \mu\text{m}$," leading to the introduction of a buffer of $10 \times 0.18 \mu\text{m}$ to respect the timing constraints. The al-

gorithm is restarted and operated until the introduction of a new repeater at $4000 \mu\text{m}$. Finally, by introducing two repeaters, all coupling problems can be avoided, and the total travel time is reduced to 1.85 ns.

This example is a very basic application, but more complex systems can be designed which take into account all the abacuses provided by the SISM.

C. Application for Chip-Level Global Extraction

In [5], Cong and He have developed an algorithm for fast extraction and estimation of interconnect parasitic effects. The method used is capable of applying table-based models generated using H-SPICE simulations, and wire capacitance tables generated using 3-D extractions. Even if these tables are accurate, their validity could be criticized due to the technology variation process that can reach 30% within the same wafer. Our proposal is to obtain these tables from extensive measurements on a wide set of samples, to extract the delay and crosstalk amplitude variation, and to introduce the abacus presented in this paper in place and route-aided design software. By implementing specific patterns using the signal integrity system measurement for technology characterization, the problem of inaccuracy between simulations and real

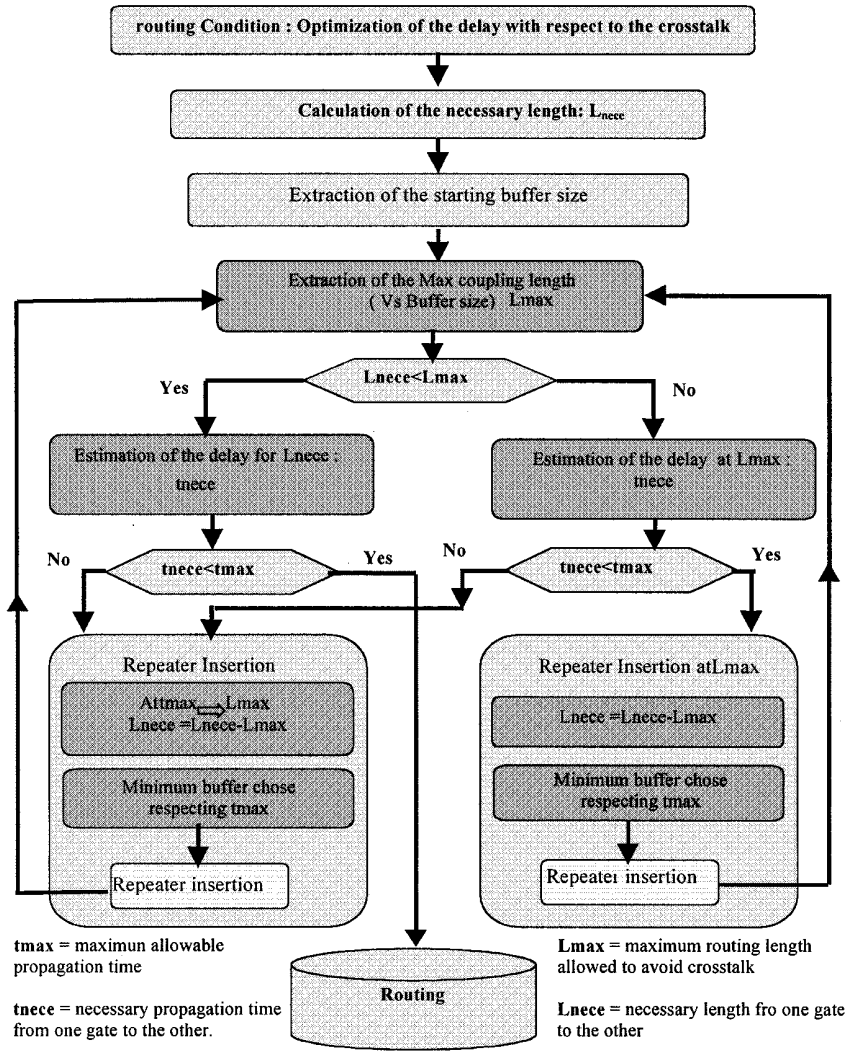


Fig. 29. Example of a place and route strategy algorithm.

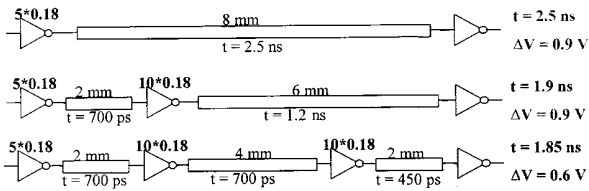


Fig. 30. Illustration of repeater insertion to avoid crosstalk.

design can be dealt with, as well as the very long computation time needed to extract all the possibilities.

VII. CONCLUSION

Today's technological developments in integrated CMOS circuits enable complex functions to be integrated at increasingly large operating frequencies. The market for microprocessors has long been the driving force behind size reduction. With the appearance of circuits able to work at frequencies greater than gigahertz, new markets are addressed, such

as mobile telephones, very high speed networks, and, more globally, systems-on-chips.

The level of integration reached now begins to create very hard problems of signal integrity. From the 0.7-μm technology with two metal levels, we have passed to the 0.18 μm with six metal levels in the space of ten years, and the interconnects are today the main limiting factor for improved performances and reliability.

In this paper, we have presented several aspects of signal integrity within interconnects. First, we analyzed the field of validity and precision of the various models used in the simulation of signal propagation by applying them to the study of delay, crosstalk coupling, and crosstalk delay. Second, the main existing methods of measurement, either external or directly on-chip, have been listed, together with an evaluation of their advantages and drawbacks.

Third, experimental measurements have been presented, based on a test-vehicle fabricated in a 0.18-μm six-metal layer CMOS technology, integrating 64 signal integrity test patterns and an on-chip measurement method. The precise characterization of the propagation delay, crosstalk noise,

and delay induced by crosstalk have been achieved successfully.

From the various measurements obtained, a complete set of abacuses to gauge propagation delay and crosstalk coupling have been created. Their use at various design levels has been discussed.

This work contributes to providing designers with fast and reliable solutions to the problem of guaranteeing the integrity of integrated circuits. The vision we have developed in this paper related to the use of the abacuses to reduce parasitic effects is upset by the implementation in the design flow of specific design rules, the development of algorithm for place and route aided design, and by fast post-layout analysis.

Faced with the growing complexities of the integrated circuits and the fast evolution toward ultradeep-submicrometer dimensions, the physical considerations of the interconnections must reincorporate as much as possible into the design flow to guarantee system-on-a-chip reliability. This means that the new challenge in interconnect technology is not only in the development of new manufacturing processes, but also at the highest level of the design flow.

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