

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Yojiro Matsueda and
Hayato Nakanishi
U.S. Patent No.: 8,164,267 Attorney Docket No.: 54108-0001IP2
Issue Date: April 24, 2012
Appl. Serial No.: 12/219,592
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Title: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND
ELECTRONIC APPARATUS

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Patent Trial and Appeal Board
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**DECLARATION OF DAVID K. LIU IN SUPPORT OF PETITION FOR IN-
TER PARTES REVIEW OF UNITED STATES PATENT NO. 8,164,267
PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

EX-1001	U.S. Patent No. 8,164,267 to Yojiro Matsueda and Hayato Nakanishi (“the ’267 patent”)
EX-1002	Excerpts of the Prosecution History of Japanese Application No. 2002-293696
EX-1003	Certified Translation of Excerpts from the Prosecution History of Japanese Application No. 2002-293696
EX-1004	The Prosecution History of U.S. Application No. 10/676,067
EX-1005	The Prosecution History of U.S. Application No. 12/219,592
EX-1006	Declaration of Dr. David K. Liu
EX-1007	U.S. Patent No. 6,825,820 (“Yamazaki 820”)
EX-1008	U.S. Published App. No. 2001/0015618 to Shunpei Yamazaki and Takeshi Fukunaga (“Yamazaki”)
EX-1009	U.S. Patent No 6,894,431 to Shunpei Yamazaki and Takeshi Fukunaga (“Issued Yamazaki”)
EX-1010	U.S. Published App. No. 2001/0043168 to Jun Koyama and Hajime Kimura (“Koyama 168”)
EX-1011	U.S. Patent No. 6,124,604 to Jun Koyama, Hisashi Ohtani, Yasushi Ogata, and Shunpei Yamazaki (“Koyama 604”)
EX-1012	U.S. Published App. No. 2002/0053671 to Jun Koyama (“Koyama 671”)
EX-1013	Fabrice Caignet et al, The Challenge of Signal Integrity in Deep-Submicrometer CMOS Technology, 89 Proceedings of the IEEE, No. 4 (April 2001) (“Caignet”)

- EX-1014 Flat Panel Displays for Portable Systems by Kalluri R. Sarma and Tayo Akinwande, *Journal of VLSI Signal Processing Systems* 13, 165-190 (1996) (“Sarma”)
- EX-1015 Complaint, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (EDTEX)
- EX-1016 Joint Agreed Scheduling Order, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (EDTEX)
- EX-1017 Paul Horowitz and Winfield Hill, *The Art of Electronics* (Second Edition)
- EX-1018 U.S. Patent No. 6,858,991 to Takashi Miyazawa (“Miyazawa”)
- EX-1019 U.S. Published App. No. 2003/0076046 to Naoaki Komiya et al. (“Komiya”)
- EX-1020 U.S. Patent No. 6,633,135 to Shouji Nara et al. (“Nara”)

I, David K. Liu, Ph.D., do hereby declare as follows:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., Ltd., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. (“Petitioner”). I understand that Petitioner is requesting that the Patent Trial and Appeal Board institute an *inter partes* review (“IPR”) proceeding with respect to U.S. Patent No. 8,164,267 (“the ’267 patent”).

2. I have been asked to provide my independent analysis of the ’267 patent in light of certain prior art references.

3. I am not, and never have been, an employee of Petitioner. I received no compensation for this Declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’267 patent, the prior art cited below, and issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’267 patent.

4. My analysis here is based on my years of education, research and experience, as well as my investigation and study of relevant materials, including those cited here. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further,

I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

5. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated here based on new information and on my continuing analysis of the materials already provided.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

6. I have personal knowledge or have developed knowledge of these technologies based upon education, training, or experience, of the matters set forth herein.

7. A detailed description of my professional qualifications, including a listing of my specialties/expertise and professional activities, is contained in my curriculum vitae, a copy of which is provided as Appendix A. Below is a short summary of my professional qualifications.

A. Educational Background

8. I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983. I received Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

B. Professional Experience

9. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

10. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

11. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

12. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance

transistor technology and was eventually acquired by Synopsys, Inc.

13. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm). The flash memory products I developed at Xilinx are used as the configuration memory for the FPGA, with the configuration interface between them being the JTAG interface.

14. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

15. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

16. I have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

17. I hold over 95 U.S. patents, a large number of which are directed to logic CMOS processes technology and high voltage CMOS process technology. The vast majority of my patents are in the area of CMOS process technology and memory architecture. As such, I am intimately familiar with the implementation of integrated process flows that essentially are repetitive sequences of modules, each composed of a layer patterning step followed by selective deposition and etching of various semiconductor materials, with the area of selectivity dictated by the layer patterning.

III. OVERVIEW OF CONCLUSIONS FORMED

18. The analysis and conclusions set forth in this Declaration are informed by my educational background and experiences in the field (see Section II).

19. Additionally, as part of my independent analysis for this Declaration, I have considered the following: the background knowledge/technologies that were commonly known to a person of ordinary skill in the art at the time of alleged invention (“POSITA”) before the earliest claimed priority date for the ’267 patent (10/7/2002); my own knowledge and experiences gained from my work experience in the field and related disciplines; and my experience in working with others involved in this field and related disciplines.

20. In addition, I have reviewed the ’267 patent (EX-1001), relevant ex-

cerpts of the prosecution history of the '267 patent (EX-1005), and relevant excerpts of applications related to the '267 patent (EX-1002, EX-1003, EX-1004). I have also reviewed at least the following prior art references:

- U.S. Pub. Patent No. 2001/0015618 (“Yamazaki”) (EX-1008)
- U.S. Published App. No. 2001/0043168 (“Koyama 168”) (EX-1010)
- U.S. Patent No. 6,124,604 (“Koyama 604”) (EX-1011)
- U.S. Published App. No. 2002/0053671 (“Koyama 671”) (EX-1012)

21. I have also reviewed some cited supporting references and documentation including:

- U.S. Patent No. 6,825,820 (“Yamazaki 820”) (EX-1007)
- U.S. Patent No 6,894,431 to Shunpei Yamazaki and Takeshi Fukunaga (“Issued Yamazaki”) (EX-1009)
- Fabrice Caignet et al, The Challenge of Signal Integrity in Deep-Submicrometer CMOS Technology, 89 Proceedings of the IEEE, No. 4 (April 2001) (“Caignet”) (EX-1013)
- Flat Panel Displays for Portable Systems by Kalluri R. Sarma and Tayo Akinwande, Journal of VLSI Signal Processing Systems 13, 165-190 (1996) (“Sarma”) (EX-1014)
- Paul Horowitz and Winfield Hill, The Art of Electronics (Second Edition) (EX-1017)

- U.S. Patent No. 6,858,991 to Takashi Miyazawa (“Miyazawa”) (EX-1018)
- U.S. Published App. No. 2003/0076046 to Naoaki Komiya et al. (“Komiya”) (EX-1019)
- U.S. Patent No. 6,633,135 to Shouji Nara et al. (“Nara”) (EX-1020)

22. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '267 patent at the time of the earliest possible priority date of the '267 patent, and I have done so during my review of these materials. Counsel has informed me that the earliest possible priority date to which the challenged claims of '267 patent are entitled is October 7, 2002 (“Critical Date”), and I have therefore used that Critical Date in my analysis below.

23. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the '267 patent and the prior art discussed below.

24. Although this Declaration refers to certain portions of the cited references for the sake of brevity, it should be understood that these citations are examples, and that one of ordinary skill in the art would have viewed the references cited herein in their entirety and, for reasons detailed later, in combination with other references cited herein or cited within those references themselves. The refer-

ences used in this Declaration, therefore, should be viewed as being cited and analyzed herein in their entirety.

25. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claim 1 is anticipated by, and obvious over Yamazaki (Ground 1)
- Claim 1 is obvious over Koyama 168 in view of Koyama 604 and/or Koyama 671 (Ground 2)

IV. LEVEL OF ORDINARY SKILL IN THE ART

26. Based on my knowledge and experience in the field and my review of the '267 patent and its file history, I believe that a person of ordinary skill in the art at the time of alleged invention ("POSITA") would have had at least a Master's degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing. Additional education can remedy lack of work experience and vice versa.

27. Based on my experience, I have a good understanding of the capabilities of one of ordinary skill. Furthermore, I possess those capabilities myself.

V. LEGAL STANDARDS

28. I have been informed by counsel of certain legal principles applicable to a patentability analysis and I have applied these principles as listed below.

A. Claim Construction

29. I have been informed by Counsel and understand that the best indicator of claim meaning is its usage in the context of the patent specification as understood by one of ordinary skill. I further understand that the words of the claims should be given their plain meaning unless that meaning is inconsistent with the patent specification or the patent's history of examination before the Patent Office. Counsel has also informed me, and I understand that, the words of the claims should be interpreted as they would have been interpreted by one of ordinary skill at the time the invention was made (not today). Because I do not know at what date the invention as claimed was made, I have used the earliest priority date of the '267 patent as the point in time for claim interpretation purposes. That date was October 7, 2002.

B. Legal Standards for Anticipation

30. I have been informed by Counsel and understand that documents and materials that qualify as prior art can render a patent claim unpatentable as anticipated. I am informed by Counsel and understand that all prior art references are to be looked at from the viewpoint of a person of ordinary skill in the art.

31. I am informed by Counsel and understand that a challenged claim is unpatentable as "anticipated" under 35 U.S.C. § 102 if it is determined that all the limitations of the claim are described in a single prior art reference. I am informed

by Counsel and understand that, to anticipate a claim, a prior art reference must disclose, either expressly or inherently, each and every limitation of that claim and enable one of ordinary skill in the art to make and use the invention.

32. I have been informed by Counsel and understand that in an inter partes review, “the petitioner shall have the burden of proving a proposition of unpatentability,” including a proposition of anticipation, “by a preponderance of the evidence.” 35 U.S.C. § 316(e).

C. Legal Standards for Obviousness

33. I have been informed by Counsel and understand that documents and materials that qualify as prior art can render a patent claim unpatentable as obvious. I am informed by Counsel and understand that all prior art references are to be looked at from the viewpoint of a person of ordinary skill in the art at the time of the invention, and that this viewpoint prevents one from using his or her own insight or hindsight in deciding whether a claim is obvious.

34. I have been informed by Counsel and understand that a claim is unpatentable for obviousness under 35 U.S.C. § 103 (in the pre-AIA form of that statute that applies to the '267 Patent) “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I am informed by

Counsel and understand that obviousness may be based upon a combination of references. I am informed by Counsel and understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. However, I am informed by Counsel and understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.

35. I am informed by Counsel and understand that when a patented invention is a combination of known elements, a court must determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue by considering the teachings of prior art references, the effects of demands known to people working in the field or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art.

36. I am informed by Counsel and understand that a patent claim composed of several limitations is not proved obvious merely by demonstrating that each of its limitations was independently known in the prior art. I am informed by counsel and understand that identifying a reason those elements would be combined can be important because inventions in many instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. I am informed by Counsel

and understand that it is improper to use hindsight in an obviousness analysis, and that a patent's claims should not be used as a "roadmap."

37. I am informed by Counsel and understand that an obviousness inquiry requires consideration of the following factors: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) any objective indicia of non-obviousness, such as commercial success, long-felt but unresolved need, failure of others, industry recognition, copying, and unexpected results. I understand that the foregoing factors are sometimes referred to as the "Graham factors."

38. I have been informed by Counsel and understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but that the nexus linking two or more prior art references is sometimes simple common sense. I have been informed by Counsel and understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

39. I have been informed by Counsel and understand that if a technique has been used to improve one device, and a person of ordinary skill at the time of invention would have recognized that it would improve similar devices in the same

way, using the technique is obvious unless its actual application is beyond his or her skill.

40. I have been informed by Counsel and understand that practical and common sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. I have been informed by Counsel and understand that a person of ordinary skill looking to overcome a problem will often be able to fit together the teachings of multiple prior art references. I have been informed by Counsel and understand that obviousness analysis therefore takes into account the inferences and creative steps that a person of ordinary skill would have employed at the time of invention.

41. I have been informed by Counsel and understand that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill at the time of invention, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I have been informed by Counsel and understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

42. I have been informed by Counsel and understand that secondary indicia of non-obviousness may include (1) a long felt but unmet need in the prior art that was satisfied by the invention of the patent; (2) commercial success of processes covered by the patent; (3) unexpected results achieved by the invention; (4) praise of the invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the invention; (7) failure of others to find a solution to the long felt need; and (8) skepticism by experts. I understand that evidence of secondary indicia of non-obviousness, if available, should be considered as part of the obviousness analysis.

43. I have been informed by Counsel and understand that there must be a relationship between any such secondary considerations and the invention, and that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

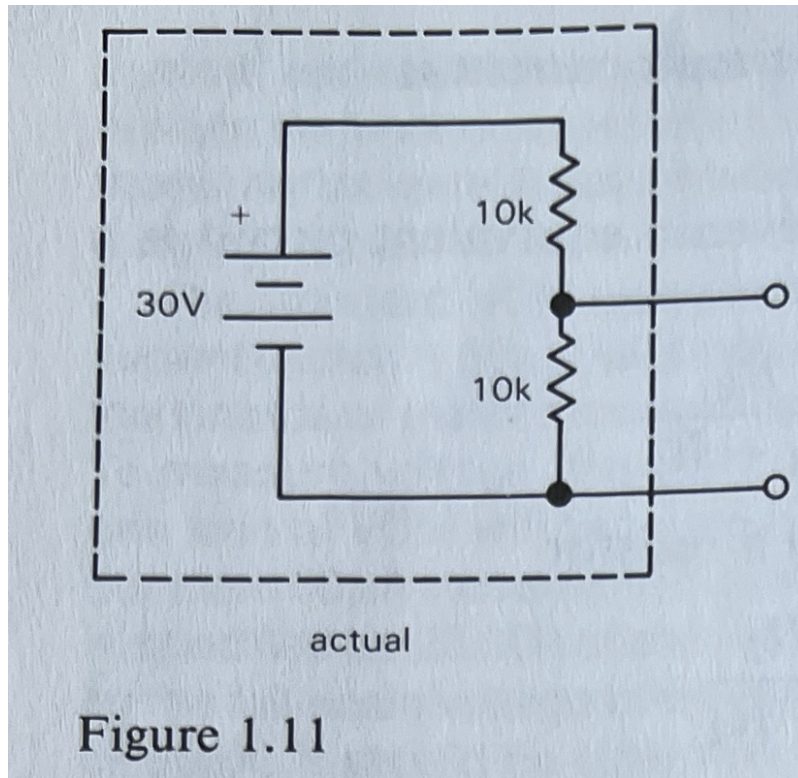
44. In summary, my understanding is that prior art teachings are properly combined where one of ordinary skill having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

45. I have been informed by Counsel and understand that in an *inter partes* review, “the petitioner shall have the burden of proving a proposition of unpatentability,” including a proposition of obviousness, “by a preponderance of the evidence.” 35 U.S.C. § 316(e).

VI. TECHNOLOGY BACKGROUND

A. Fundamental Circuit Principles

46. A brief discussion of fundamental electrical circuit principles is relevant to my discussion below of the ’267 patent. An electrical circuit generally consists of circuit elements, such as capacitors, transistors, resistors, etc., connected to each other through conductors. Conductors serve to transport electricity from one point to another—e.g., from one circuit element to another. By arranging the circuit elements in particular ways, various useful functions can be achieved. For example, in the basic circuit shown below, a battery provides electricity to two resistors (indicated by the zigzag lines each marked “10k”).



EX-1018 at 11.

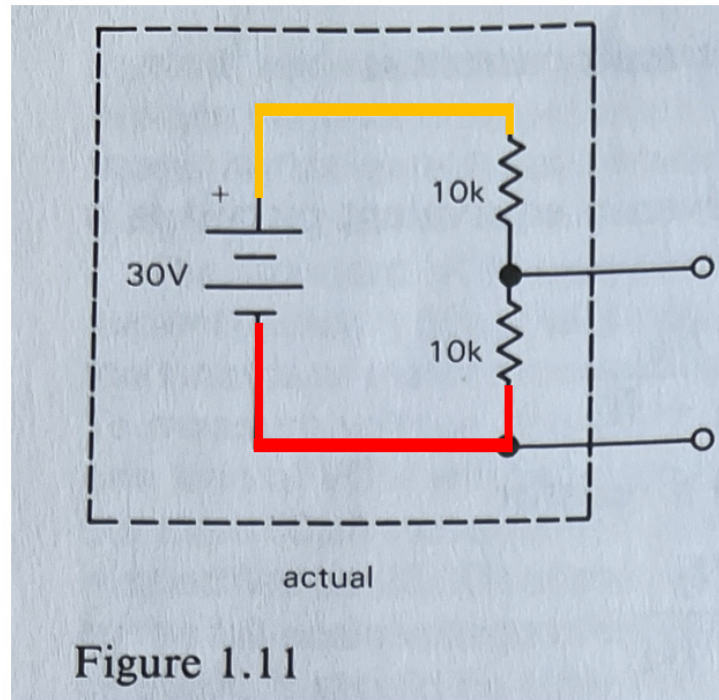
47. Ohm's law—a basic electrical property—provides further explanation of how electricity operates in a circuit. “Current” generally refers to the amount of electrical charge that passes through a point in a circuit in a given period of time, which can roughly be analogized to water passing through a pipe. “Voltage” generally refers to the difference in electric potential energy between two points in a circuit (or “nodes”), which can roughly be analogized to the difference in water pressure between two points in a pipe. “Resistance” generally refers to the amount of resistance that is provided to current as it passes between two points in a circuit. In a circuit, positive electrical charge flows from a circuit node having high voltage

to a node having low voltage. Along the way, the current passes through various circuit elements connected to one another through conductors. Many circuit elements obey “Ohm’s law” which governs the relationship between voltage, current, and resistance. This law states that the amount of current passing through a given circuit element (commonly represented by the letter “I” and measured in “amperes”) is directly proportional to the voltage drop across that element (commonly represented by the letter “V” and measured in “volts”) and is inversely proportional to the resistance of that element (commonly represented by the letter “R” and measured in Ohms). *See generally* EX-1018 at 8-10. Expressed as a mathematical formula, Ohm’s law states:

$$I = \frac{V}{R}$$

48. In an ideal circuit, the conductors that connect circuit elements have zero resistance, and the voltage is equal at any two points of the conductor. Also in an ideal circuit, the voltage drops across circuit elements like resistors, or any other component that exhibits a load. In the exemplary basic circuit shown below, the positive terminal of the battery and all points along the orange conductor are at a particular voltage (e.g., 30 volts) and the negative terminal of the battery and all points along the red conductor are at another voltage (e.g., 0 volts). In this example, there would be a drop of 30 volts across the resistors due to their resistance. In

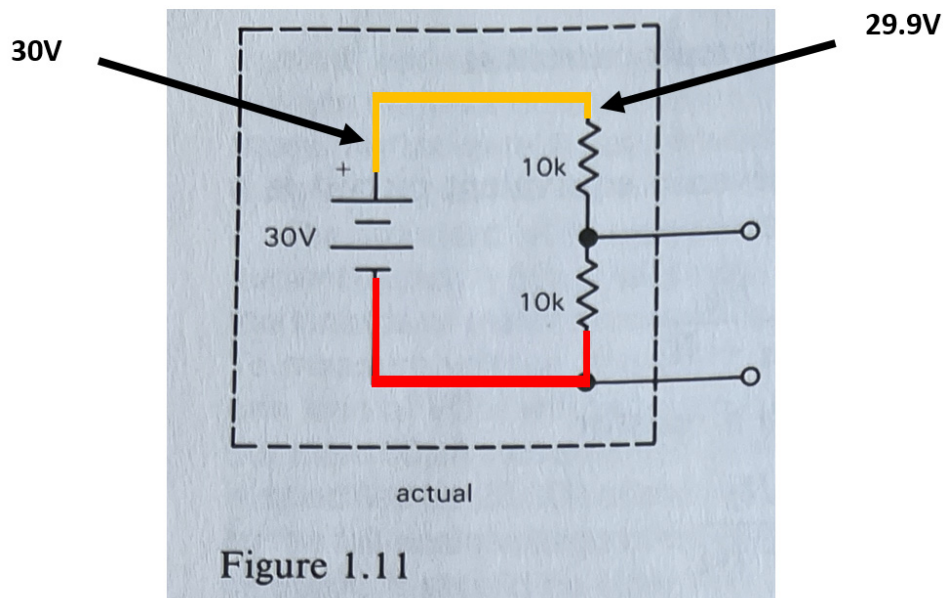
fact, ideally, all the voltage of the battery should be delivered to the load, which instead could be a lamp, to maximize the amount of the energy, e.g. in the form of light glowing, being dissipated by the load, and to minimize the amount of energy unnecessarily dissipated by the connection to the load.



EX-1018 at 11.

49. In real life circuits, however, even conductors exhibit some amount of resistance, and therefore the voltage decreases somewhat along the conductor as it gets farther from the source. Depending on the application, this voltage decrease can be relevant to the operation of the circuit. For example, in the hypothetical exemplary circuit below, the slight resistance of the conductor connecting the battery's positive terminal to the top resistor might cause the voltage to drop by 0.1V

at the point that it reaches the top resistor.



Id.

50. Both voltage and current are ways of delivering “power” to circuit elements. *See generally* EX-1018 at 8-10. As discussed above, as voltage increases, current increases, and vice-versa, at least in circuit elements that obey Ohm’s law. In the context of circuits, power generally refers to the amount of electrical energy provided to a circuit element. It can be computed by multiplying voltage by current, as shown by the mathematical equation below.

$$P = V * I$$

B. Electronic Displays

51. Electronic displays generally work by providing a matrix of “pixels,” each of which emit light. EX-1014 (*Flat Panel Displays for Portable Systems* by

Kalluri R. Sarma and Tayo Akinwande, Journal of VLSI Signal Processing Systems 13, 165-190 (1996)) at 6. By controlling the light emitted by each pixel, these displays can generate images. *See id.*

52. The '267 patent and the prior art references I discuss below are applicable to “electroluminescent” type displays. An “electroluminescent display,” also known in the art as an “EL” display or “ELD,” creates light by using electrodes to apply a voltage or current to a material that emits light under these conditions, as electroluminescent material is material that emits light when excited by an electric voltage or current. The Sarma paper describes an ELD that “creates light by the excitation of a powder phosphor or a thin-film phosphor layer.” *See* EX-1014 at 4-5. For color displays “red, green, and blue phosphor layers” can be used. *See id.*

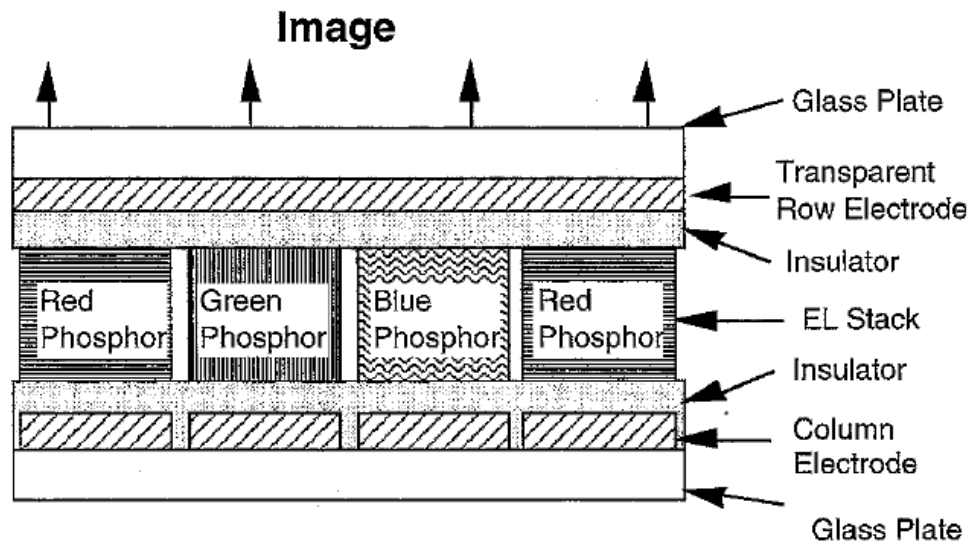


Figure 1. Device structure of the electroluminescent display (ELD).

53. To address specific pixels in a display, active matrix technology may be implemented, which utilizes active transistors to drive specific electro-optical elements. *See* EX-1014 at 11-13. An active matrix display generally consists of a matrix of pixels, generating light (luminescence) upon electrical activation, that have been deposited or integrated onto thin-film transistor arrays (arrays of unit driving circuits), with these “TFT” arrays functioning as a series of control and data input to control the current flowing to each pixel. *See id.* In other words, each pixel comprises a pixel circuit, which in turn comprises an electro-optical element and a driving transistor, which supplies power to the electro-optical element. *See id.*

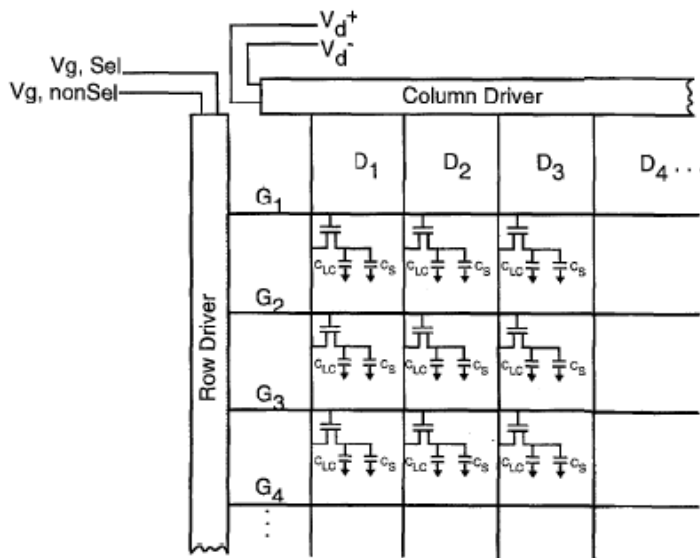


Figure 7. Schematic of a TFT active matrix array.

Id. at Fig. 7.

54. Each of the plurality of pixel circuits in an active matrix display is arranged to correspond to the intersection of a data line and a control line (gate signal

line or scan line):

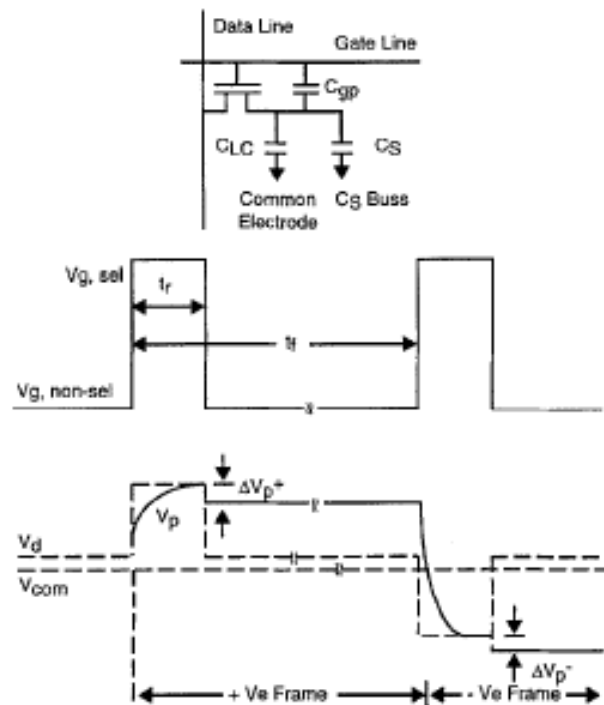


Figure 10. Electrical equivalent of a TFT-LCD pixel, and its operation.

Id. at Fig. 10.

55. The current flowing through an electro-optical device in an “active matrix” arrangement is fundamentally controlled by two TFTs at each pixel: one TFT driven by the control line to start and stop the charging of a storage capacitor to a level according to the signal supplied by the data line; another TFT to provide a voltage level needed, based on the voltage of the stored capacitor, to create a constant current to the pixel. *See id.* at 12-13.

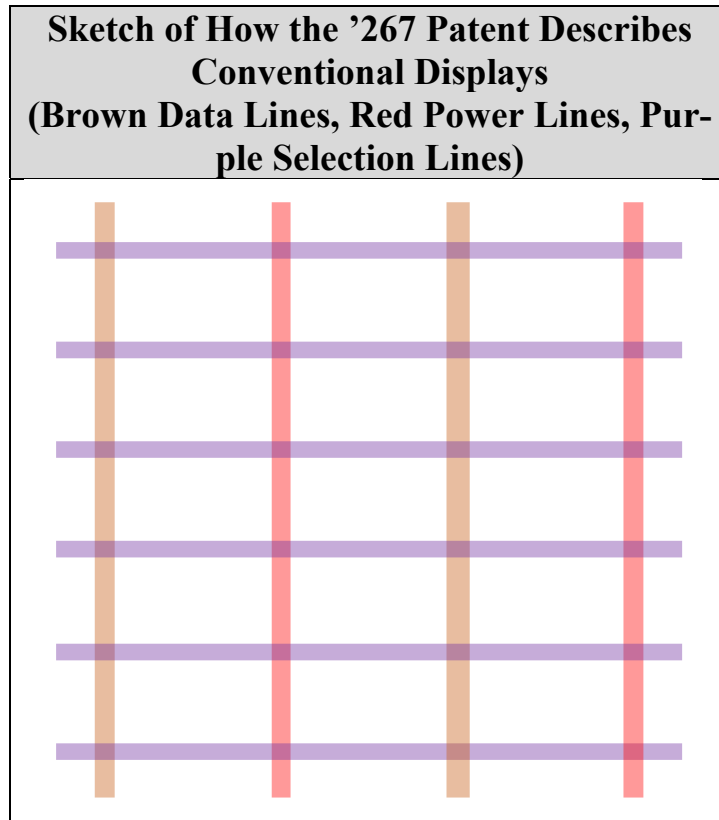
56. Due to the many advantages offered by the active matrix system, such as improved contrast, a POSITA would have looked to various teachings in the

field that offer an improved active matrix system in implementing a display panel device. This would not only include LCD or plasma displays, but electroluminescent and other self-emission types of display devices. This endeavor would also include looking into various teachings that would improve upon or mitigate the variations introduced by the inherent device characteristics of TFT transistors implemented in non-single crystalline silicon.

VII. THE '267 PATENT

A. Overview of the '267 Patent

57. The '267 patent “relates to a wiring layout suitable for an electro-optical device including electro-optical devices.” EX-1001 at 1:13-14. It describes “conventional color-display active-matrix-driven display panels” as having “electric power lines and data lines . . . disposed in the column direction,” such that they sandwich pixels between them. *See id.* at 1:30-42 (“a data line is disposed between the given pixel and the left-adjacent pixel, and an electric power line is disposed between the given pixel and the right-adjacent pixel”). It also describes conventional displays as having “selection lines . . . disposed in the row direction.” *See id.* at 1:35-36. The sketch below illustrates how the '267 patent describes the line arrangement of conventional displays, with brown lines representing data lines, red lines representing power lines, and purple lines representing selection lines.



58. The '267 patent describes various trade offs in engineering features that are considered when designing conventional displays. *See id.* at 1:51-2:9. It states that “the organic EL device” (which given the context appears to refer to a particular light-emitting pixel of a display panel) has “greatly different power consumption” needs depending on its color, which means “the optimal width of the electric power line is greatly different for each color.” *See id.* at 1:51-56. It further states that such displays needed to have “the same pixel pitch due to the restriction from the manufacturing process for a display.” *See id.* at 1:56-63. A POSITA would have understood “pixel pitch” to generally refer to the distance between adjacent pixels in a display, and is a measure of the area occupied by a pixel

unit. Thus, having the “same pixel pitch” essentially would mean in this context that the pixels should be evenly spaced. The ’267 patent further states, however, that pixel pitch should be determined such that it accommodates “the maximal width for disposing the electric power lines.” *Id.* at 1:56-59. In other words, the power lines must be wide enough to accommodate the most “power hungry” pixel color and allow it to receive adequate power, given that pixel pitch is limited by the metal pitch of the power lines. However, this can diminish the pixel’s “aperture ratio,” which generally refers to the ratio of a pixel’s light-sensitive area to the pixel’s total area. *See id.* at 1:61-63. Thus, “with the conventional wiring layout, the width of the electric line and the aperture ratio of the pixel are in the relation of trade off each other, and it is difficult to maintain a large aperture ratio while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.” *See id.* at 2:3-9.

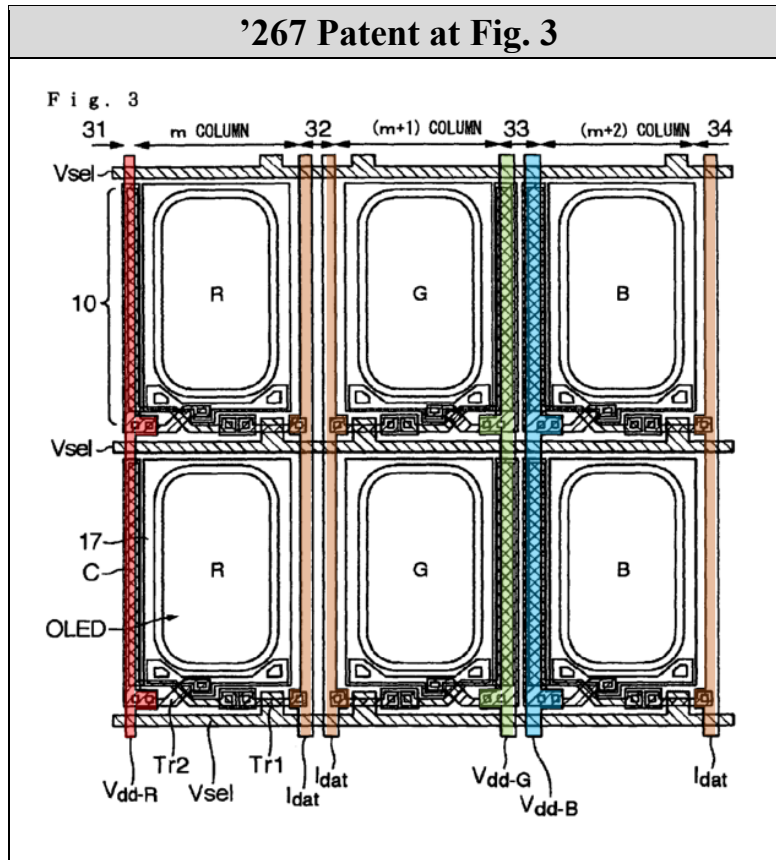
59. The ’267 patent states that “an object of the present invention [is] to provide a wiring method for electric power lines, wherein the aperture ratio of the pixel can be increased while maintaining a pixel matrix with the same pixel pitch.” *See id.* at 2:10-13.

60. To address this problem, the ’267 patent primarily proposes different ways to rearrange the power, data, and selection lines. It describes lines being

formed in “line forming regions” between rows or columns of pixels and rearranging the lines such the line forming regions have “generally the same width.” *See id.* at 2:14-25, 2:36-3:45. It provides specific embodiments of how these lines would be arranged and how these line forming regions would be formed.

61. In the patent’s first embodiment, line forming regions—each having (a) two power lines or (b) two data lines or (c) one power line and one data line—are formed between pixel columns. *See* EX-1001 at 5:43-56; *see also generally id.* at 4:46-6:67, Figs. 1-3. Combinations of lines in the line forming regions are formed such that the line forming regions having “the width the same as possible.” *Id.* at 6:1-5.

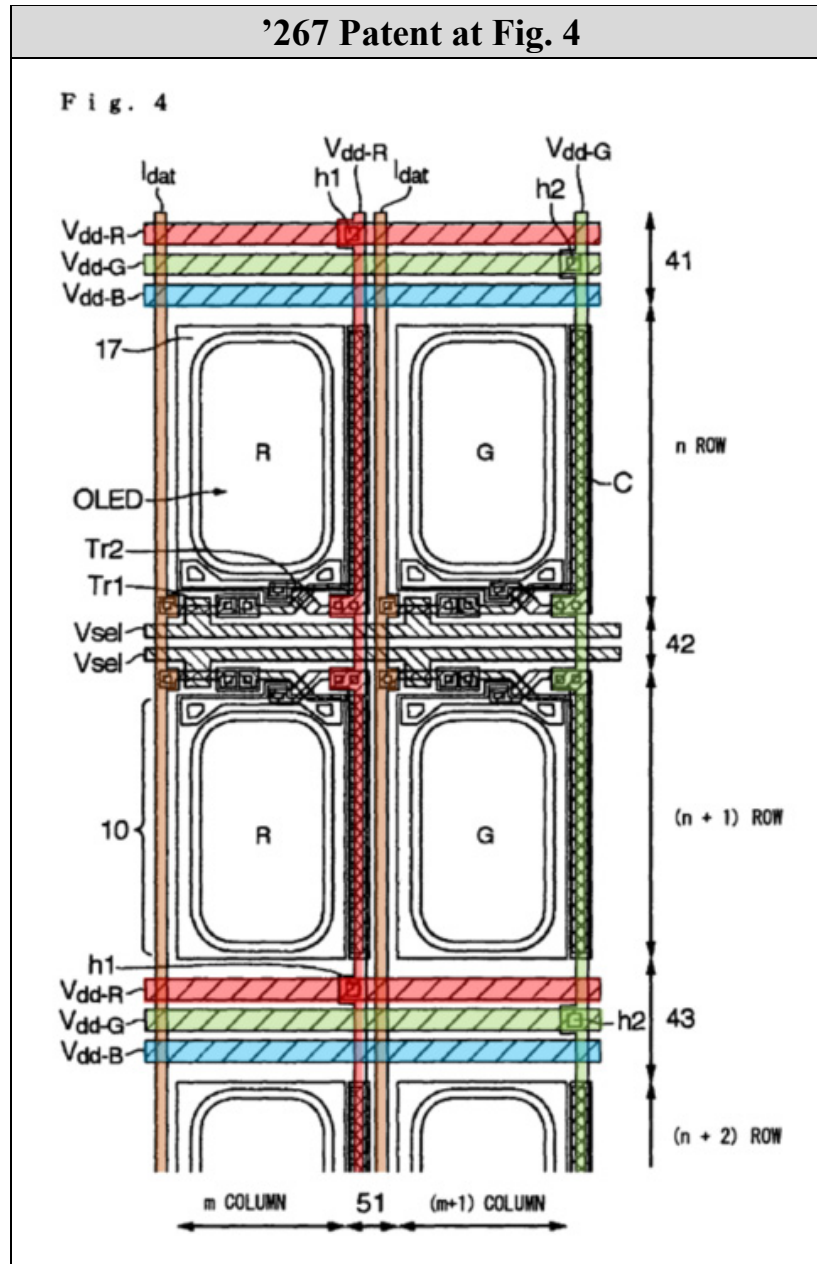
62. For example, if the “width of V_{dd-G} [Green]>width of V_{dd-R} [Red]>width of V_{dd-B} [Blue],” the green and blue power lines are combined in line forming region 33 and two data lines are formed in line forming region 32, as shown in Figure 3 reproduced below. *Id.* at 5:65-63, 6:5-23. The red power line and a data line are formed in regions 31 and 34 (although figure 3 does not fully depict both lines in these regions). *See id.* at 6:20-23 (noting that “with the line forming region 31, only the electric power line V_{dd-R} is shown in the drawing, and with the line forming region 34, only the data line I_{dat} is shown in the drawing”).



63. In the patent's second embodiment, line forming regions are formed between both pixel rows and pixel columns. *See generally* EX-1001 at 7:1-67, Fig. 4. Additionally, and in further contrast to the first embodiment, the second embodiment features both horizontally oriented power lines and vertically oriented power lines, which connect to each other through contact holes formed in an inter-layer insulating film. *See id.* at 7:45-50. In semiconductor devices, contact holes can be formed in layers to allow a conductor to electrically connect material at a layer above to the layer below, which is what the '267 patent's second embodiment implements. The '267 patent states that arranging electric power lines "in the form of a matrix" reduces "wiring resistance . . . thereby enabling sufficient current supply

to the organic EL devices.” *Id.* at 7:54-61; *see also id.* at 7:61-64 (“Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, cross-talk can be reduced.”).

64. In figure 4, which corresponds to the second embodiment, “three [horizontal] electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} ” are formed in every other row and between these rows are formed two scan lines. *See id.* at 7:12-29 (identifying line forming regions 41 and 43 as having these three power lines and line forming region 42 as having the two scan lines). Additionally, a vertically oriented “electric power line V_{dd} ” and “one data line I_{dat} ” are formed in line forming regions between columns. *See id.* at 7:29-45 (identifying line forming region 51 as having red electric power line V_{dd-R} and data line I_{dat}), 7:33-38 (identifying red electric power line V_{dd-R} and data line as disposed between red and green pixel groups to the left of line forming region 51), 7:38-45 (identifying green electric power line V_{dd-G} and data line as disposed between the blue and green pixel groups to the right of line forming region 51).



65. In the patent's third embodiment, the teachings of the first and second embodiments are generally combined. *See generally* EX-1001 at 8:1-9:17, Fig. 5. It features "three combinations of two lines selected from the three [vertically-oriented] electric power lines, $V_{dd-[G]}$, V_{dd-R} , and V_{dd-B} and the three data lines I_{dat} . . . formed between the pixel groups arrayed in the column direction." *See id.* at 8:29-

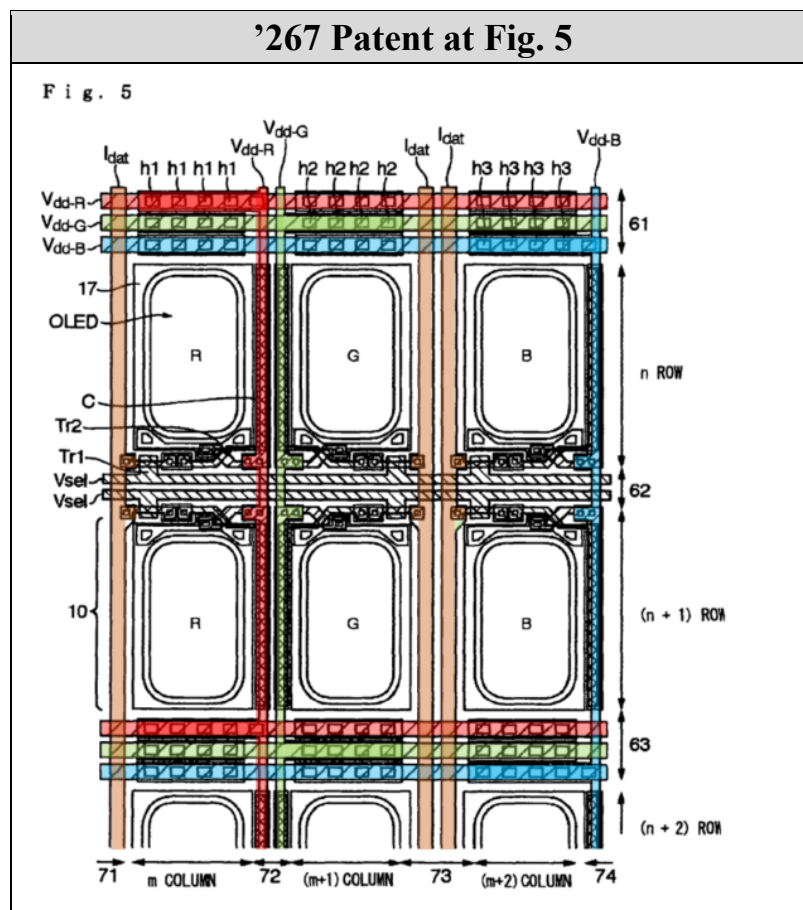
32. For example, I_{dat} combined with the blue electric power line $V_{\text{dd-B}}$ ¹ can be formed in regions 71 and 74 (*see id.* at 8:32-37, 8:46-51), the $V_{\text{dd-G}}$ green and $V_{\text{dd-R}}$ red power lines may be formed in region 72 (*see id.* at 8:37-41), and two I_{dat} data lines may be formed in region 74 (*see id.* at 8:42-45).

66. Like the second embodiment, the third embodiment features line-forming region rows that alternate between “three [horizontally-oriented] electric power lines $V_{\text{dd-G}}$, $V_{\text{dd-R}}$, and $V_{\text{dd-B}}$ ” and “two scan lines V_{sel} .” *See id.* at 8:12-28 (identifying line forming regions 61 and 63 as having three electric power lines and line forming region 62 as having two scan lines). Also like the second embodiment, the third embodiment’s horizontally-oriented electric power lines connect to their corresponding vertically-oriented electric power lines through contact holes. *See id.* at 8:51-64.

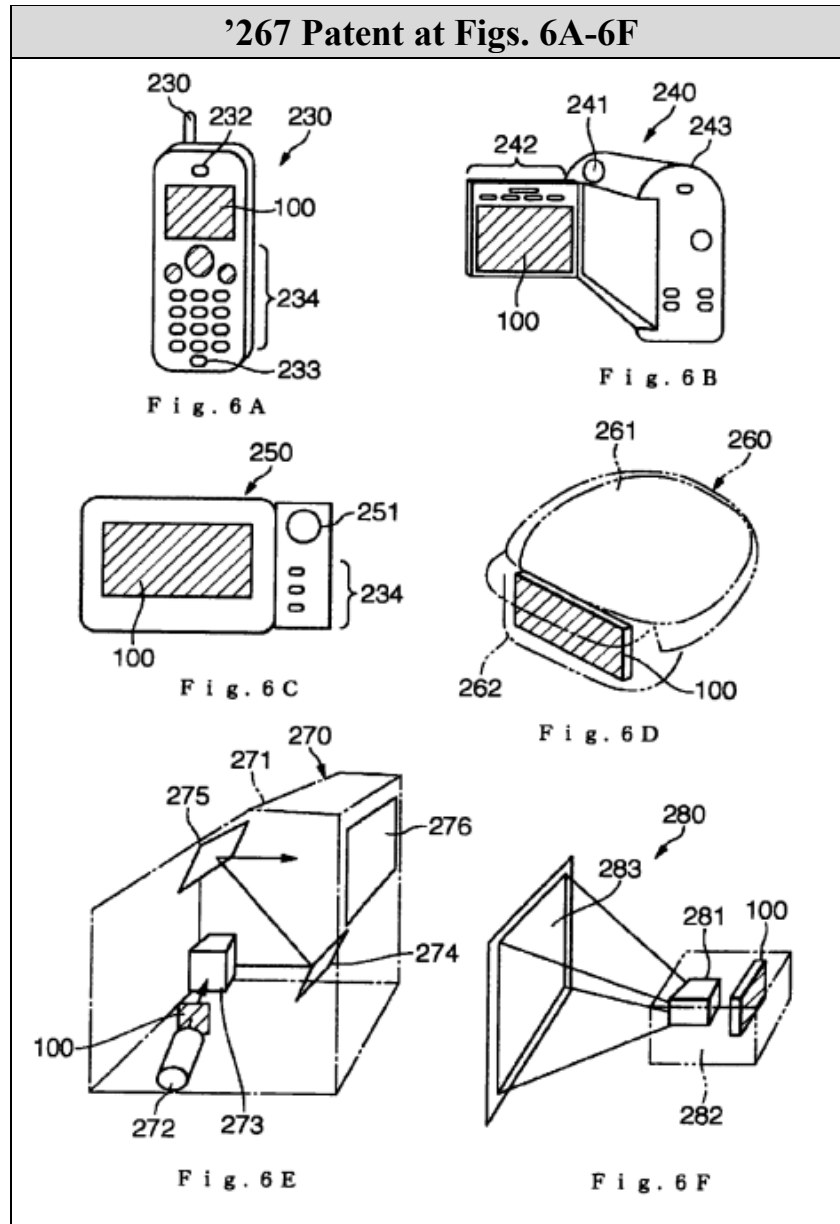
67. In contrast to the previous embodiments, however, each pair of the third embodiment’s horizontal and vertical electric power lines electrically connect

¹ The ’267 patent does not identify the color of the “electric power line” formed in region 71, and it identifies $V_{\text{dd-G}}$ as the electric power line formed in region 74. However, these appear to be typographical errors as the context provided, along with figure 5, suggest that the blue electric power line would be formed in these regions.

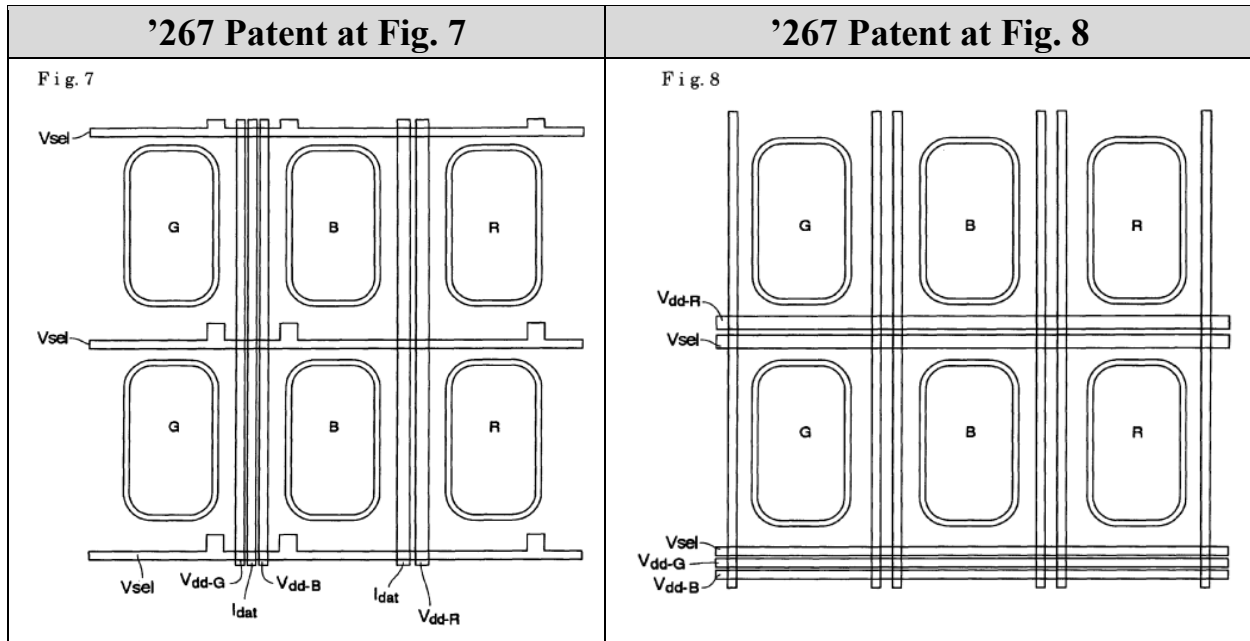
to each other through *multiple* contact holes rather than just one, which provides “the advantage of preventing wiring breakage, and . . . the advantage of reducing wiring resistance.” *See id.* at 8:60-64, Fig. 4 (identifying h1 as the series of contact holes for the red power lines, h2 as the green power line contact holes, and h3 as the blue power line contact holes). To accommodate those multiple contact holes, a portion of the vertical power lines extends over the horizontal power lines to form what was known in the art as a “landing pad”—a small protrusion designed to accommodate multiple contact holes.



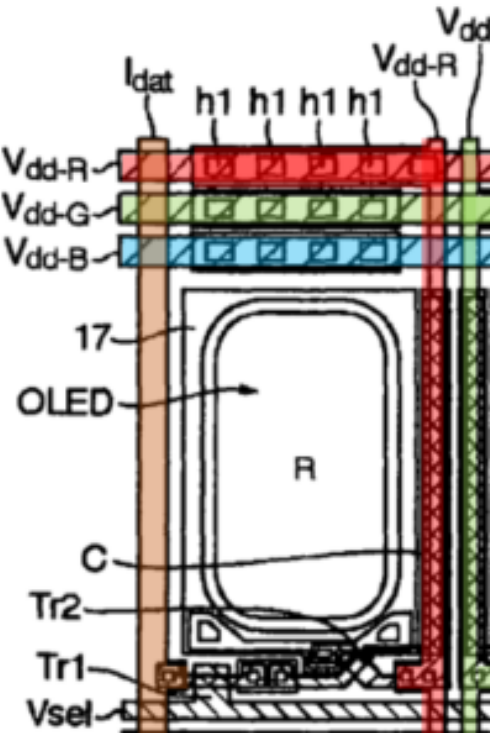
68. The patent's fourth embodiment provides examples of "electronic devices to which the electric-optical device according to the present invention can be applied." *See generally* EX-1001 at 9:20-58, Figs. 6-8. Examples of such devices include cellular phones (Fig. 6(a)), video cameras (Fig. 6(b)), portable personal computers (Fig. 6(c)), head mount displays (Fig. 6(d)), rear projectors (Fig. 6(e)), and front projectors (Fig. 6(f)).



69. Finally, the patent briefly mentions two embodiments featuring line forming regions with different combinations of power lines, scan lines, and data lines. *See* EX-1001 at 9:59-10:3, Figs. 7-8.



70. Claim 1 of the '267 patent is reproduced below. It does not explicitly reflect the patent's teachings about rearranging lines in line forming regions to achieve uniform pixel pitch or increased aperture ratio. Rather, it focuses on the third embodiment's teachings about having pairs of power lines arranged in first and second directions (potentially reflecting the vertical and horizontal directions) and having those power lines electrically connected to one another through multiple contact holes. It also claims "the second portion of the first power line being electrically connected to the second power line through plurality of contact holes" (potentially reflecting the use of landing pads that protrude from the vertical power lines)

'267 Patent at Fig. 5 (Magnified to Show Exemplary Pixel)	'267 Patent Claim 1
Fig. 5 	1. An electro-optical device comprising: - a scan line; - a data line that intersects the scan line; - a first electrode; - a second electrode; - a light emission layer that is disposed between the first electrode and the second electrode; - a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction; - a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line; and - an inter-layer insulating film that is disposed between the first power line and the second power line, - the second portion of the first power line being electrically connected to the second power line through plurality of contact holes.

B. Japanese Patent Office Proceedings

71. The original owner of the '267 filed its foreign priority application—JP2002-293696—on October 7, 2002. *See* EX-1002; EX-1003.

C. United States Patent Office Proceedings

72. The '267 patent issued from U.S. application no. 12/219,592, which was filed as a continuation of U.S. application no. 10/676,067 and claims priority to Japanese application no. 2002-293696.

1. U.S. App. No. 10/676,067

73. On October 2, 2003, the '067 application was filed with twelve claims. EX-1004 at 1-16. These claims all required “line forming regions” and/or a “plurality of electric power lines.”

74. On November 10, 2003, the Applicant filed a preliminary amendment amending the claims. *See id.* at 61-68. The six independent claims, as they existed after the preliminary amendments, are reproduced below.

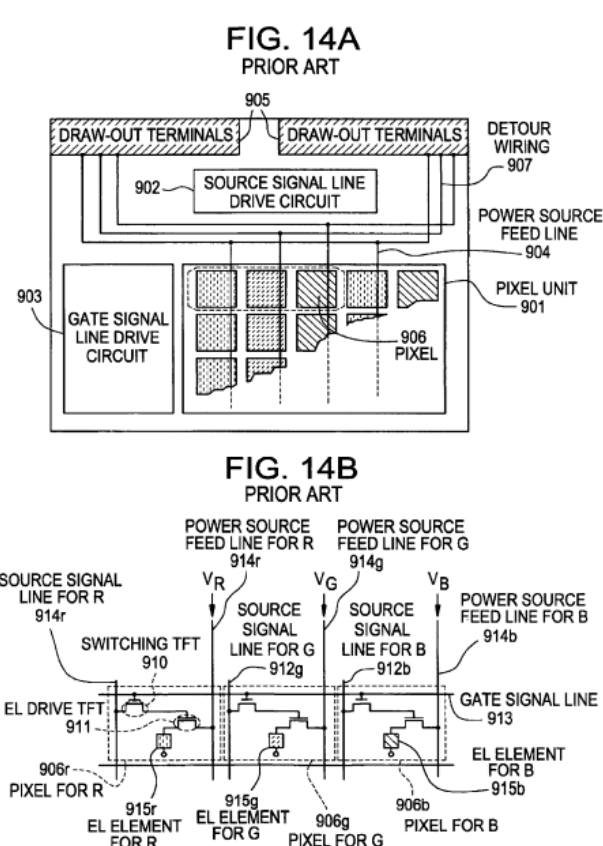
1. An electro-optical device comprising a plurality of pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from an electric power supply circuit; wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction;	2. An electro-optical device comprising: a plurality of scan lines; a plurality of data lines; a plurality of pixels, disposed at portions corresponding to intersections of said scan lines and said data lines, including electro-optical devices; and a plurality of electric power lines for supplying driving voltage to said electro-optical devices; wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one
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and wherein line forming regions are formed between adjacent pixel groups of said plurality of pixel groups; and wherein said line forming regions are formed with generally the same width.	direction of the row direction and the column direction; and wherein a plurality of line forming regions are formed between adjacent pixel groups of said plurality of pixel groups; and wherein at least two lines selected from at least one electric power line of said plurality of electric power lines, at least one scan line of said plurality of scan lines, and at least one data line of said plurality of data lines, are formed in at least one line forming region of said plurality of line forming regions.
3. An electro-optical device comprising: a plurality of scan lines; a plurality of data lines; a plurality of pixels, disposed at portions corresponding to intersections of said scan lines and said data lines, including electro-optical devices; and a plurality of electric power lines for supplying driving voltage to said electro-optical devices; wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction; and wherein a plurality of line forming regions are formed between adjacent pixel groups of said plurality of pixel groups;	4. An electro-optical device comprising: a plurality of scan lines; a plurality of data lines; a plurality of pixels, disposed at portions corresponding to intersections of said scan lines and said data lines, including electro-optical devices; and a plurality of electric power lines for supplying driving voltage to said electro-optical devices; wherein said plurality of pixels make up a plurality of pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction; and wherein a plurality of line forming regions are formed between adjacent pixel groups of said plurality of pixel groups;

and wherein both at least one electric power line of said plurality of electric power lines and at least one scan line of said plurality of scan lines are formed in at least one line forming region of said plurality of line forming regions.	and wherein both at least one electric power line of said plurality of electric power lines and at least one data line of said plurality of data lines are formed in at least one line forming region of said plurality of line forming regions.
11. A matrix substrate comprising a plurality of pixel electrodes disposed in the form of a matrix; wherein said plurality of pixel electrodes make up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction; and wherein a plurality of line forming regions are formed between adjacent pixel electrode groups of said plurality of pixel electrode groups; and wherein said line forming regions are formed with generally the same width.	12. A matrix substrate comprising: a plurality of scan lines; a plurality of data lines; a plurality of pixel electrodes disposed at portions corresponding to intersections of said scan lines and said data lines; and a plurality of electric power lines for supplying voltage to said plurality of pixel electrodes; wherein said plurality of pixel electrodes make up a plurality of pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction; and wherein a plurality of line forming regions are formed between adjacent pixel electrode groups of said plurality of pixel electrode groups; and wherein at least two lines selected from at least one electric power line of said plurality of electric power lines, at least one scan line of said plurality of scan lines, and at least one data line of said plurality of data lines, are formed in at least one line forming region of said plurality of line forming regions.

75. This preliminary amendment also amended the specification. EX-1004 at 82-93.

76. On December 1, 2006, the Examiner issued an office action rejecting all pending claims as anticipated by U.S. 6,825,820 to Yamazaki (“Yamazaki 820”). EX-1004 at 110-116; EX-1007. Yamazaki 820 lacks various teachings that the “Yamazaki” cited in ground 1 contains, including figure 3A, which I discuss below. The table below reflects how the Examiner mapped certain claimed limitations to Yamazaki 820’s disclosures.

Features of Pending Claims	Yamazaki 820 at Figs. 14A-14B
An electro-optical device	
Plurality of scan lines (913)	
Plurality of data lines (914r, 912g, 912b)	
Plurality of pixels (906) disposed at portions corresponding to intersections	
Plurality of power lines (914r, 914g, 914b)	
Plurality of line forming regions (914r, 914g) being formed between adjacent pixel groups	

77. On February 7, 2007, an interview was held in which “examiner and

attorney agreed to make clear about the formation of the line regions in the display device” to create proposed claim 1 which would allegedly “overcome [the] 102 rejection but not 103(a). EX-1004 at 121. The examiner also suggested a “further addition of new limitation for a proper characterization of claim [sic] invention.” *Id.*

78. On February 15, 2007, the Applicant amended independent claims 1, 2, 4, 11, and 12 to recite that “a combination being determined such that a sum of widths of a plurality of lines formed in one line forming region is approximately the same as that of a sum of widths of a plurality of lines formed in another line forming region.” EX-1004 at 122-127. In other words, the Applicant amended the claims to essentially require that one of the claimed line forming regions has approximately the same width as another line forming region. The Applicant did not, however, amend claim 3. *See id.*

79. In accompanying remarks, the Applicant argued that Yamazaki 820 “only discloses a schematic view of the wiring diagram without a disclosure as to the relative widths of the lines in any of the line forming regions” as required by the amended independent claims. *See id.* at 128. With respect to claim 3, the Applicant argued that Yamazaki 820 “does not teach at least one power line and at least one scan line being formed in at least one line forming region.” *See id.*

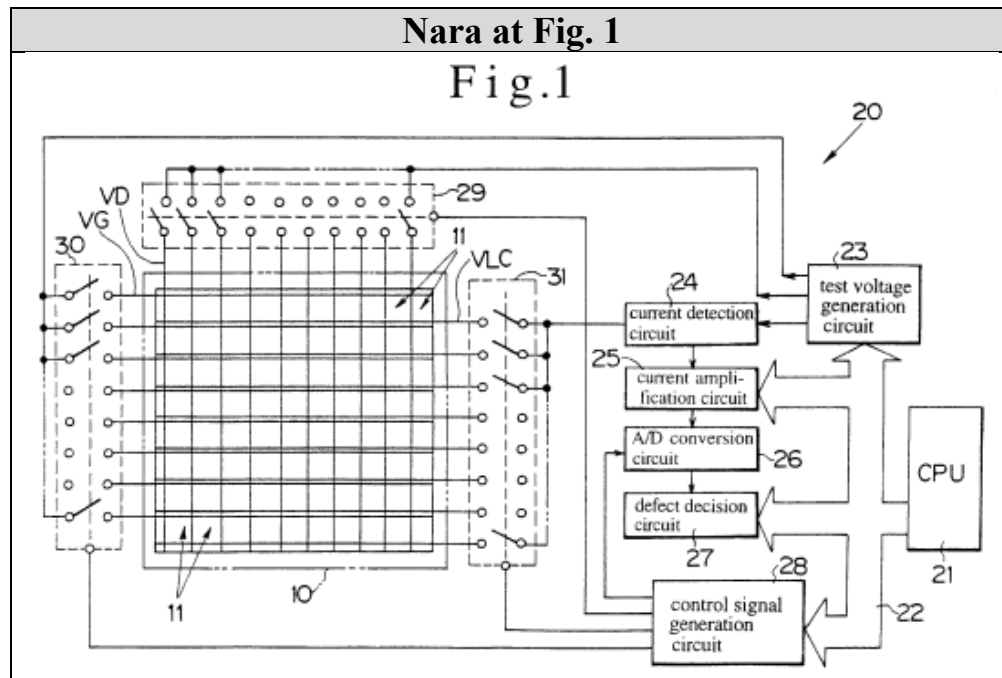
While the Applicant acknowledged that Yamazaki 820 taught “power lines (power

source feed lines 914) and data lines (source signal lines 912) being formed in the vertical line feeding regions)” it argued that “*scan* lines (source signal lines 913)” were instead “formed in the horizontal line feeding regions.” *See id.* at 128-129. The Applicant also essentially argued that it would not have been obvious to ensure that line forming regions had the same width because that the ’267 patent taught “the voltage requirements of differing colored pixels are different, the width of the voltage lines to pixels of different colors is varied accordingly.” *See id.*

80. On May 16, 2007, the Examiner issued another office action rejection. EX-1004 at 199-207. The Examiner rejected the newly amended claims as indefinite “since it is not clear how a combination being determined [sic].” *See id.* at 201-202. The Examiner also rejected the amended claims (1, 2, 4, 11, 12) as anticipated by Komiya (US 2003/0076046). *See id.* The Examiner noted that Komiya disclosed “the line forming regions (183, D) being formed with generally the same width.” *See id.* at 202-203.



6,633,135). *See id.* at 204-205.



82. The Examiner also rejected other claims as obvious over Komiya and Yamazaki 820.

83. On July 19, 2007, an interview was held in which the office action of May 16, 2007 was discussed. *See* EX-1004 at 234.

84. On August 16, 2007, the Applicant amended the independent claims to require that the electric power lines have “different widths.” *See id.* at 212-221. The Applicant argued that these amendments overcame the Examiner’s anticipation and obviousness rejections. *See id.* at 218-220.

85. On November 14, 2007, the Examiner issued an office action maintaining the rejection of claims 1-2, 4-5, and 7-14 as obvious over Komiya in view of Yamazaki 820 (which, according to Examiner, disclosed “electric power lines with different widths”) and of claim 3 as obvious over Nara in view of Yamazaki

820. EX-1004 at 223-233.

86. On February 11, 2008, the Applicant amended the claims such that they all essentially required “at least two electric power lines . . . with different widths being formed in at least one line forming region.” EX-1004 at 237-248. Applicant further argued that Komiya and Yamazaki 820 do not disclose a plurality of electric power lines having different widths or that the sum of the widths of a plurality of lines are the same in multiple line regions. *See id.* at 245-247.

87. On March 19, 2008, the Examiner issued an office action. EX-1004 at 250-261. This office action noted that the pending application’s drawings must show the various claimed features regarding line width. *See id.* at 252-253. It also rejected several of the claims as reciting new subject matter. *See id.* at 253-255. It also rejected claims 1, 7-11, and 13-16 as obvious over Tanada (US 2001/0048106) in view of Yamazaki 820; claims 2, 4-5, and 12 as obvious over Komiya in view of Yamazaki 820; and claim 3 in view of Nara and Yamazaki 820. *See id.* at 255-260.

88. On June 19, 2008, the Applicant amended the specification to include figures 7 and 8 to show lines having different widths. EX-1004 at 324-340. The Applicant also amended the claims regarding the widths of the lines. *See id.*

89. On October 14, 2008, the Examiner issued another office action. EX-

1004 at 342-353. This office action rejected certain claims for lack of written description; rejected claims as failing to comply with written description. It rejected claims 1, 7-11, and 13-17 as obvious over Yamada (U.S. 6,522,079) in view of Yamazaki 820. It rejected claims 2, 4-5, and 12 as obvious over Komiya in view of Yamazaki 820.

90. On May 1, 2009, the application went abandoned for failure to timely file a reply to the last office action. EX-1004 at 358.

2. U.S. App. No. 12/219,592

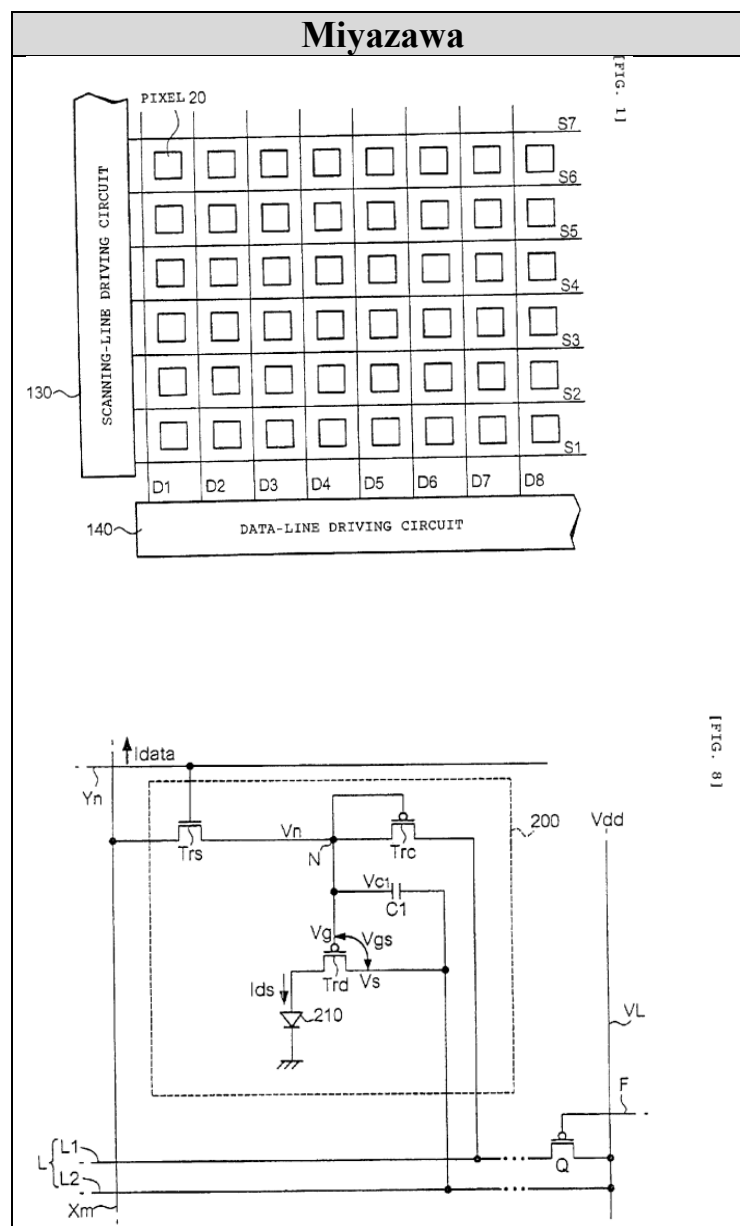
91. On July 24, 2008, the Applicant filed the '592 application with six claims claiming priority to the '067 application. EX-1005 at 1-25. The only independent claim is reproduced below, which recited a plurality of contact holes connecting first and second power lines. *Id.* at 17-18.

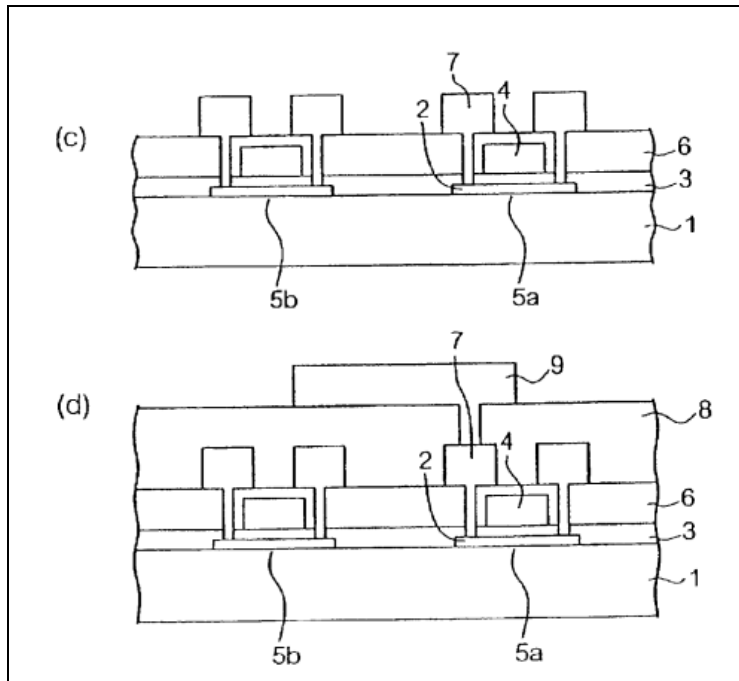
Claim 1
1. An electro-optical device comprising: a scan line extending in a direction; a data line extending in a direction that intersects the scan line; a pixel located corresponding to the intersection of the scan line and the data line, the pixel including a light emission layer between a first electrode and a second electrode; a first power line extending in the direction in which the scan line extends; a second power line extending in the direction in which the data line extends;

an inter-layer insulating film between the first power line and the second power line; and

a plurality of contact holes extending through the inter-layer insulating film, the contact holes electrically connecting the first power line and the second power line to each other.

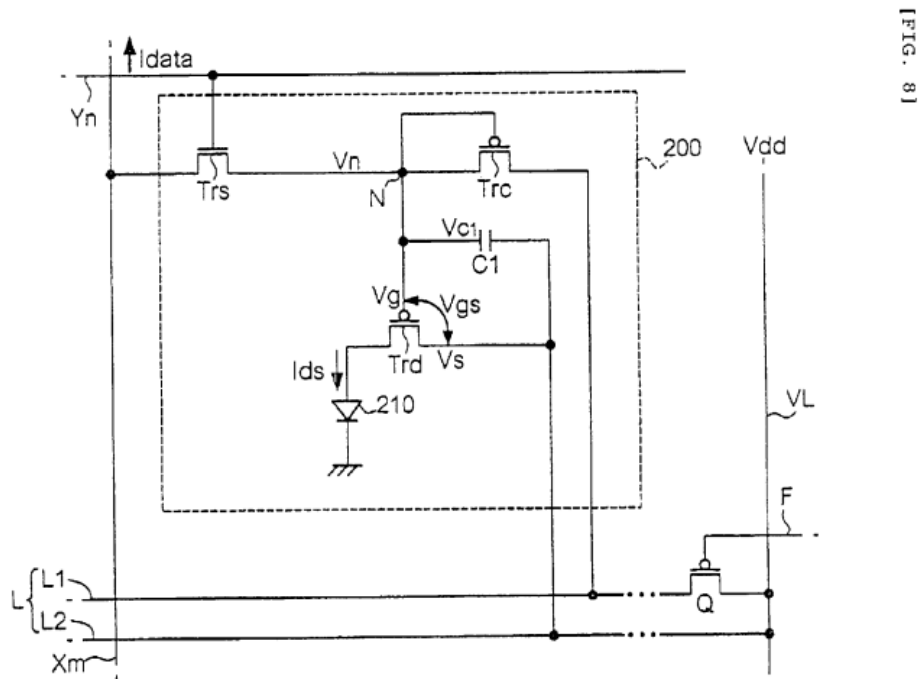
92. On October 6, 2010, the Examiner issued an office action rejecting all claims as anticipated by Miyazawa (US 6,858,991). EX-1005 at 74-80.





93. On January 6, 2011, the Applicant amended the claims to remove the limitation that contact holes must “extend[] through the inter-layer insulating film.” EX-1005 at 88-94. Applicant further argued that Miyazawa’s figures 4c and 4d show contact holes that connect S/D and semiconductor layer whereas claim 1 recites contact holes electrically connecting power lines. *Id.*

94. On April 4, 2011, the Examiner issued an office action maintaining the prior rejection based on Miyazawa. EX-1005 at 96-102. The Examiner argued that, in Miyazawa, two power lines (L and VL) are connected to one another per figure 8.



EX-1018 at Fig. 8.

95. On June 22, 2011, an interview was held. EX-1005 at 109, 113-115. In this interview the “examiner pointed out that [Miyazawa] apparently disclosed . . . all the features as claimed including the proposed amended portion ‘the plurality of contact holes disposed corresponding to an intersection of the first power line and the second power line and disposed in the pixel.’” *Id.* at 115. However, the examiner allegedly further observed “no description of the second power line overlapping at least the second portion of the first power line’ as recited in the newly added proposed claim 9.” *Id.* The Applicant’s representative “fully agreed with the examiner’s analysis.” *Id.*

96. On July 5, 2011, the Applicant cancelled the pending claims and introduced claim 9 discussed in the interview. EX-1005 at 105-111.

97. On December 19, 2011, the claims were allowed. EX-1005 at 116-124.

98. Following an amendment after allowance to clarify the “light emission layer” limitation, the claims were reallocated and issued. *See* EX-1005 at 147-151, 163-178.

VIII. GROUND 1

99. In my opinion, Yamazaki anticipates claim 1. Additionally, in my opinion, Yamazaki renders obvious claim 1.

A. Yamazaki

100. Published Patent Application No. 2001/0015618 (“Yamazaki”) is a published patent application filed by Semiconductor Energy Laboratory Co. Ltd. and invented by Shunpei Yamazaki and Takeshi Fukunaga. Yamazaki was filed December 7, 2000 and published August 23, 2001 (both before the October 7, 2002 Critical Date of the ’267 patent). I understand that Yamazaki therefore qualifies as prior art to the ’267 patent under pre-AIA 102(a), (e), and (b).

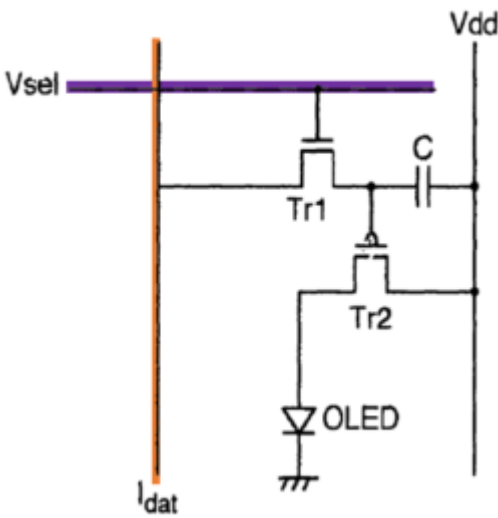
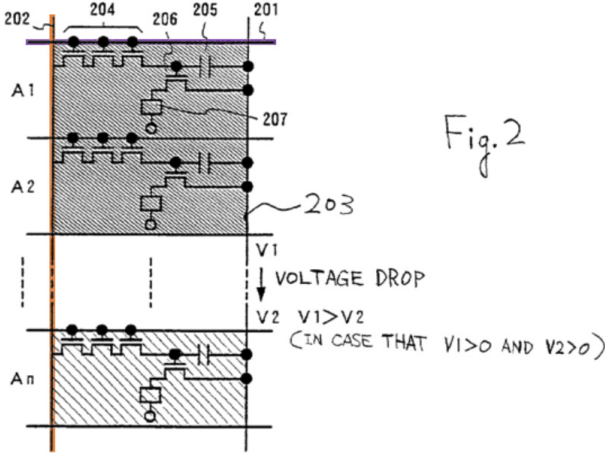
B. ’267 Patent Claim 1 Mapped to Yamazaki

101. Yamazaki discloses an “electro-optical device.” Yamazaki discloses that the “light-emitting device” it describes in various embodiments can be implemented in “various electronic equipment,” like a “display.” *See* EX-1008 at

[0089]-[0102], Figs. 8A-8F, 9A-9B. Each example of electronic equipment constitutes an “electro-optical device.” *See also* EX-1001 (“‘[E]lectro-optical device’ means a general electronic device for changing the optical state of light by using electric effects.”).

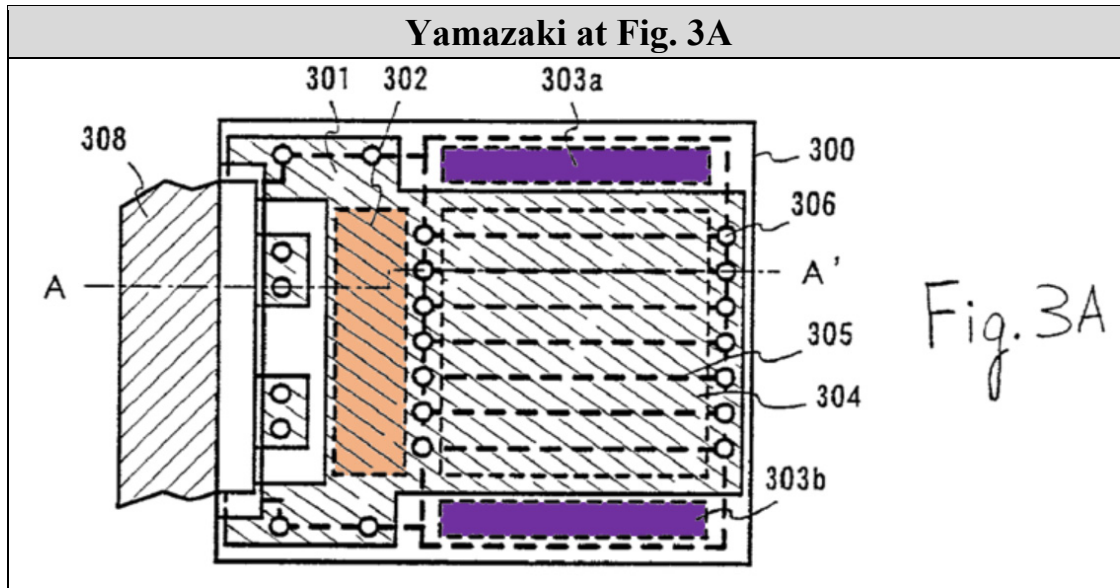
102. Yamazaki discloses a “scan line” and a “data line that intersects the scan line.” Yamazaki, as background, describes features of “active matrix EL display devices” and the “voltage drop” problem that conventional versions of such devices faced. *See* EX-1008 at [0004]-[0013], Fig. 2. Those features include “gate wiring 201” that can “open a gate of the switching TFT 204” and “source wiring 202” that can apply “a desired voltage to a gate of the current control TFT 206.” *Id.* at [0007], [0010]. A POSITA would understand that a “gate line” and a “scan line” are the same thing and that a “source wiring” and a “data line” are the same thing. In both the ’267 patent and Yamazaki, the gate/scan lines can turn on or off switching transistors (e.g., Tr1 in ’267 patent figure 2 and TFT 204 in Yamazaki figure 2) to control whether the signal carried by source wiring/data lines can pass to the gate of a driving transistor (e.g., Tr2 in the ’267 patent figure 2 and TFT 207 in Yamazaki figure 2). Moreover, as shown by Yamazaki’s figure 2 below, the data line intersects the scan line as illustrated in the top left corner.

103. Figure 2 of the ’267 patent and figure 2 of Yamazaki are reproduced below to highlight their gate line in purple and their data line in brown.

'267 Patent at Fig. 2	Yamazaki at Fig. 2
Fig. 2 	Fig. 2 

104. Yamazaki's improved EL display, which it describes as "Embodiment Mode," also includes scan lines and data lines. *See* EX-1008 at [0035]-[0047], Figs. 3A-3C. As a preliminary matter, scan lines and data lines are basic components of EL displays, as taught by both Yamazaki and as was generally known in the art. *See id.* at [0004]-[0007] (describing "gate wiring" and "source wiring"); *also supra* Section VI.B. Because Yamazaki's Embodiment Mode is an EL display, it includes scan lines and data lines. This is further demonstrated by Yamazaki's figure 3C, which shows a "pixel portion 304," which includes scan lines and data lines. *See id.* at [0007]-[0010].

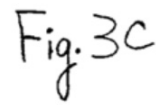
105. Moreover, Yamazaki's Embodiment Mode features a "source driver circuit" (designated by 302 and highlighted in brown in figure 3A below) and two "gate driver circuits" (designated by 303a and 303b and highlighted in purple in figure 3A below). *See* EX-1008 at [0038]. "Embodiment Mode" provides a more concrete description of how Yamazaki's figures 1A and 1B (which are more abstract in nature) would be implemented. A POSITA would have understood (as demonstrated, for example, by the name) that gate driver circuits provide gate/scan lines, and a source driver circuit provides source/data lines. *See id.* at [0012]-[0013].



106. A POSITA would have also understood that Yamazaki's Embodiment Mode's data lines intersect its scan lines. In an active matrix EL display, such as that disclosed in Yamazaki, pixels are laid out in a matrix form, and data lines and scan lines control these pixels by instructing them whether to display light and when. *See* EX-1008 at [0004]-[0013], Fig. 2; *see also supra* Section VI.B. In order to provide each pixel with access to both a data line and a scan line, it follows that those lines intersect each other.

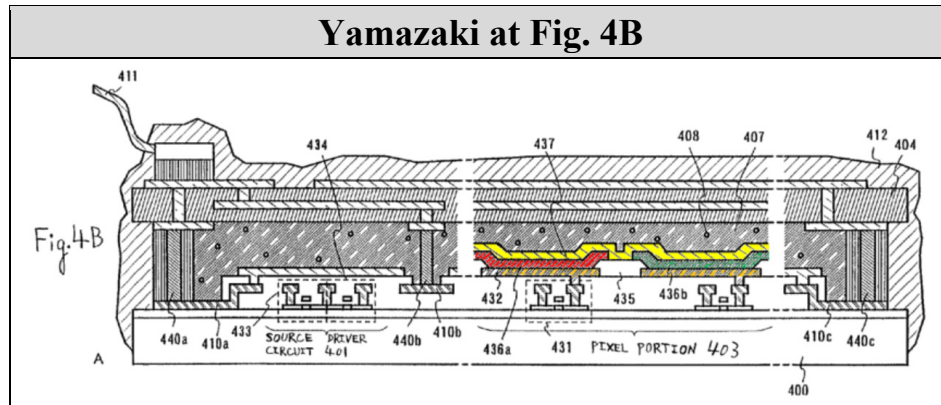
107. Yamazaki discloses a "light emission layer" disposed between first and second "electrodes." Yamazaki is directed to a "device having an element (hereinafter referred to as luminous element) that is comprised of a luminous material sandwiched between electrodes (the device will hereinafter be referred to as light-emitting device)." EX-1008 at [0002]. These are fundamental components of pixels in electroluminescent display devices, as taught by Yamazaki. *See id.* at

108. Yamazaki's "Embodiment Mode" includes a "pixel portion" 304 in which these electrodes and light emission layer are disposed. EL elements, as discussed above, contain two electrodes. Figure 3C, reproduced below, shows a pixel portion 304, which contains pixels, highlighted in yellow.



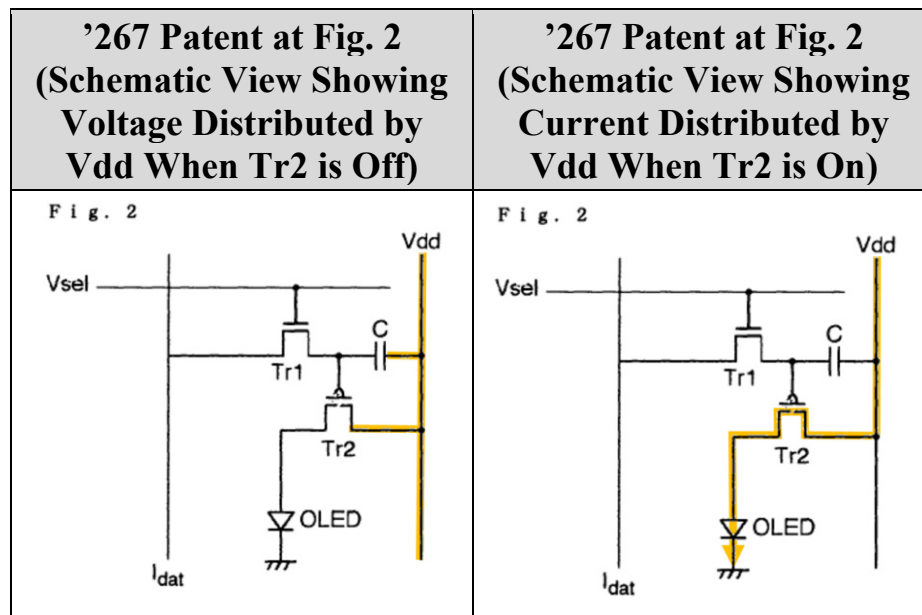
109. Yamazaki's "Embodiments" 1-4 further illustrate these electrodes and light emitting layer. *See* EX-1008 at [0053]-[0055] (referencing cross sectional view shown in figure 4B that shows "pixel electrode 432," "cathode 437," red "light-emitting layer 436a," and green "light-emitting layer 436b" of Embodiment 1); *id.* at [0061]-[0066], Fig. 5B (referencing cross sectional view "anode 502," "cathode 506," and "light-emitting layer 505" of Embodiment 2); *id.* at [0073]-[0079], Fig. 6 (referencing Embodiment 3 that shows a "modified example of the structure of the EL display device described in Embodiment 1"); *id.* at [0082], Fig. 7 (referencing Embodiment 4 that "a modified example of the structure of the EL display device described in Embodiment 1"). A POSITA would have understood these "embodiments" to provide additional detail of the features that could be included in Embodiment Mode and, furthermore, would have found it obvious to combine these features in Embodiment Mode. These additional embodiments provide implementation details that a POSITA could use to implement the pixels contemplated by pixel region 304 illustrated at a more abstract level in figure 3C. *See id.* at Fig. 4B, 5B, 6, 7.

110. Embodiment 1's Figure B, for example, is reproduced below and highlights the "pixel electrode 432" in yellow, the "cathode 437" in orange, the "light-emitting layer 436a" in red, and the "light-emitting layer 436b" in green.



111. Yamazaki discloses a “first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction;” a “second power line that extends in the second direction” and overlaps “at least a part of” the first power line’s second portion; and that the first power line’s second portion is electrically connected to the second power line “through [a] plurality of contact holes.” See EX-1008 at [0037]-[0038].

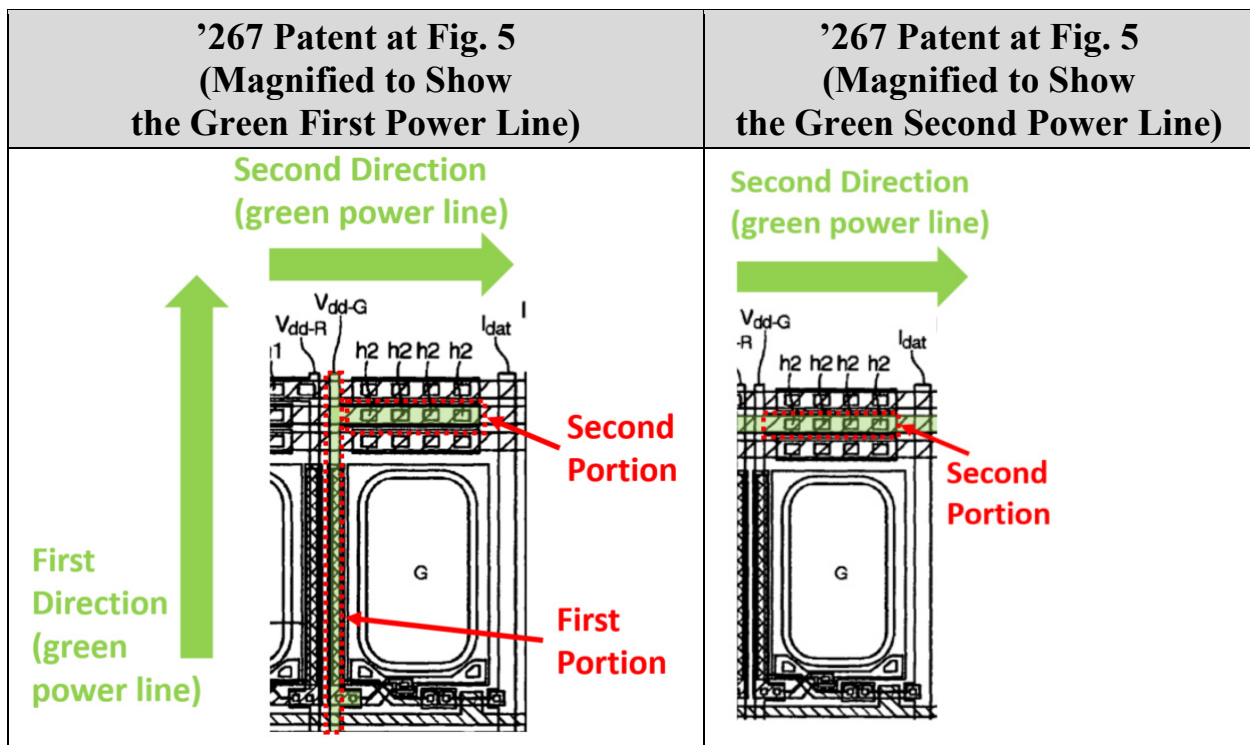
112. The '267 patent's "power lines" are the lines that distribute current and voltage to pixels. Vdd—a well-known symbol representing power supplied to an integrated circuit—refers to the source of power as shown by the '267 patent below. It applies both current and voltage in the sense that it is set to hold a certain voltage to the capacitor C and to the source or drain of the driving transistor Tr2. When it is desired that the OLED element emits light, the switching transistor Tr1 causes data line Idata to provide a signal to the gate of the driving transistor Tr2, which then turns on and allows a current to flow from Vdd through to the OLED element, allowing that element to display light.



113. The "first power lines" and "second power lines" refer to physically laid out lines that distribute Vdd's power, highlighted in red, green, and blue in the figure 5 images reproduced below. *See also* EX-1001 at 1:63-2:2 (explaining that



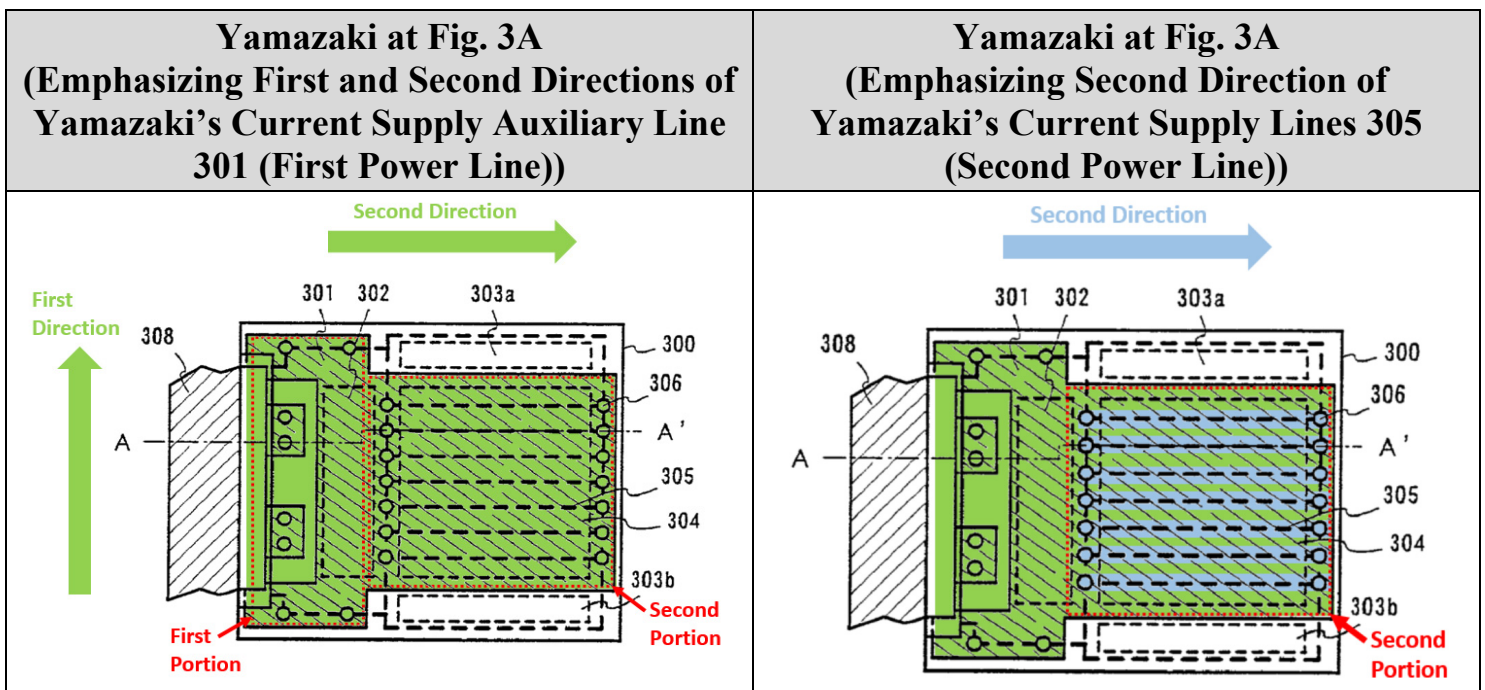
114. To lower the resistance between the first and second power lines, the first and second power lines connect to each other through multiple contact holes. The first power line features a protrusion that extends in a second direction (relative to the first direction in which it primarily extends) over the second power line to accommodate these multiple contact holes, as shown by the magnified versions of figure 5 below.



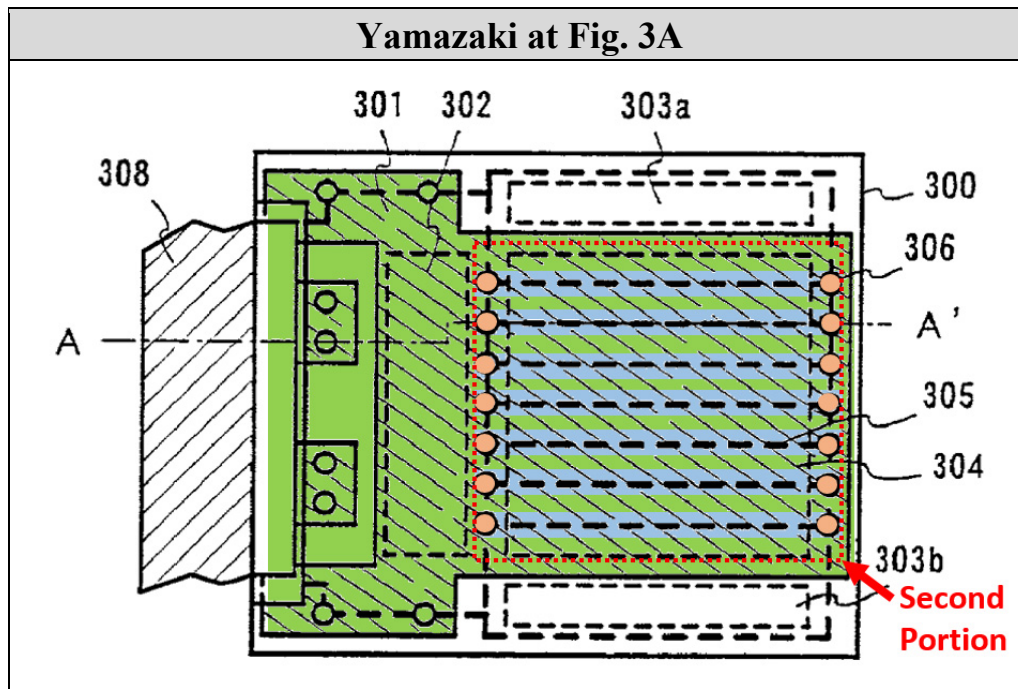
115. Yamazaki discloses power lines satisfying the '267 patent's limitations. As shown in Figure 3A of its "Embodiment Mode," Yamazaki discloses a "current supply auxiliary line 301" (shown in green) electrically connected to "current supply line[s] 305" (shown in blue). See EX-1008 at [0037]-[0039]. These

current supply lines (both 301 and 305) are power lines because they supply current to pixels to enable those pixels to emit light. *See id.* at [0037] (“[T]he current supply line is a wiring for supplying a current, which flows to an EL element, to each EL element.”). The current supply auxiliary line 301, like the ’267 patent’s power lines, “make[s] the electric potential equal in any position of the current supply line 305, and therefore” suppresses “voltage drop.” *See id.* at [0039]; *see also id.* at [0042].

116. The “current supply auxiliary line 301” constitutes a “first power line” and, as shown by figure 3A, it has a first portion that extends in a first direction and a second portion that extends in a second direction. Each “current supply line 305” constitutes a “second power line” and, as shown in figure 3A, overlaps at least part of the first power line’s second portion.

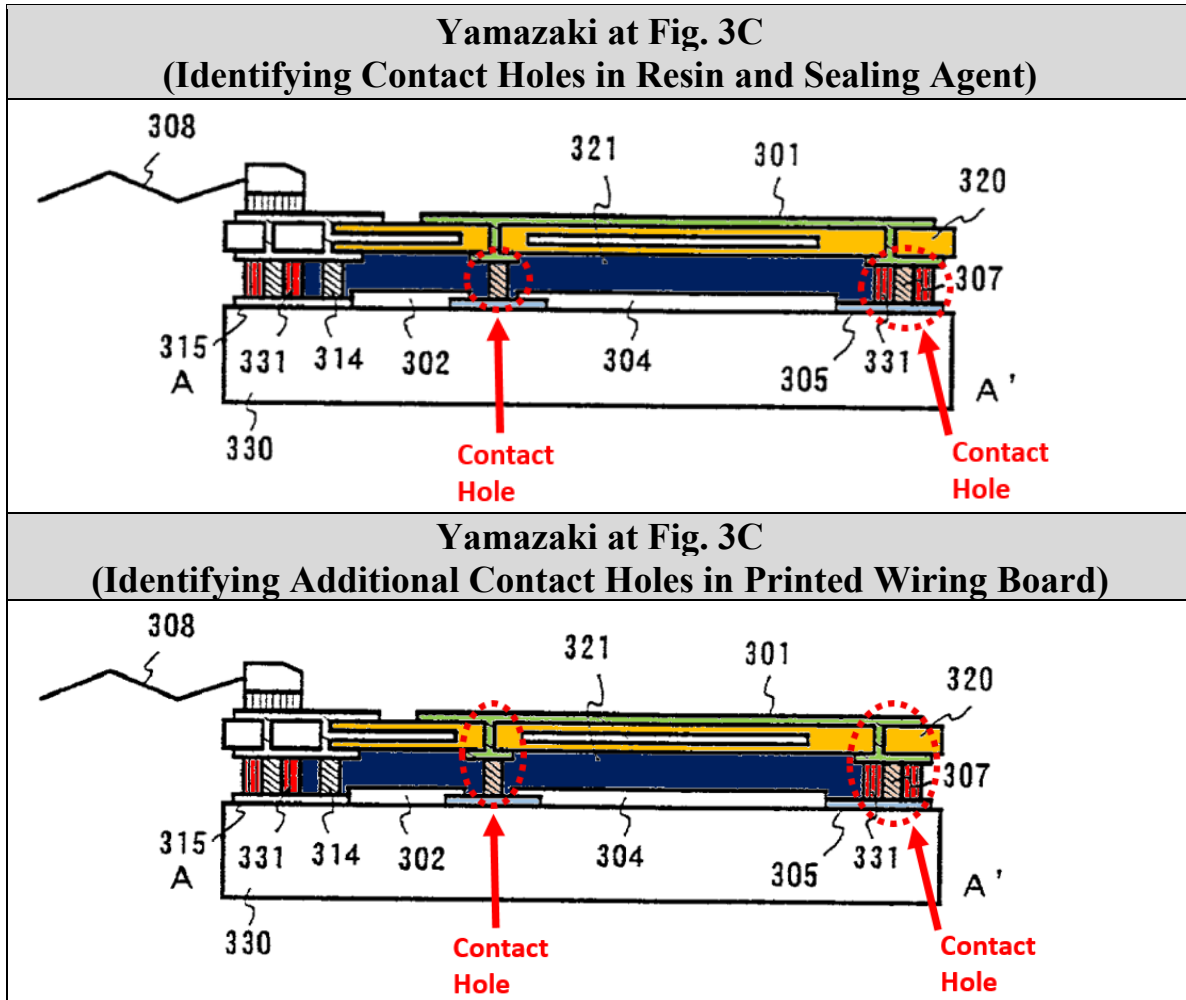


117. The second portion of Yamazaki's current supply auxiliary line 301 (first power line) is electrically connected to the second power line through a plurality of contact holes. As shown in Figure 3A of its "Embodiment Mode," Yamazaki discloses "a contact portion 306" that allows the current supply auxiliary line (first power line) to electrically connect to the current supply lines 305 (each one being a second power line). *See* EX-1008 at [0038]. This contact portion 306 consists of contact holes, signified by circles, which are highlighted in pale red in figure 3A reproduced below.

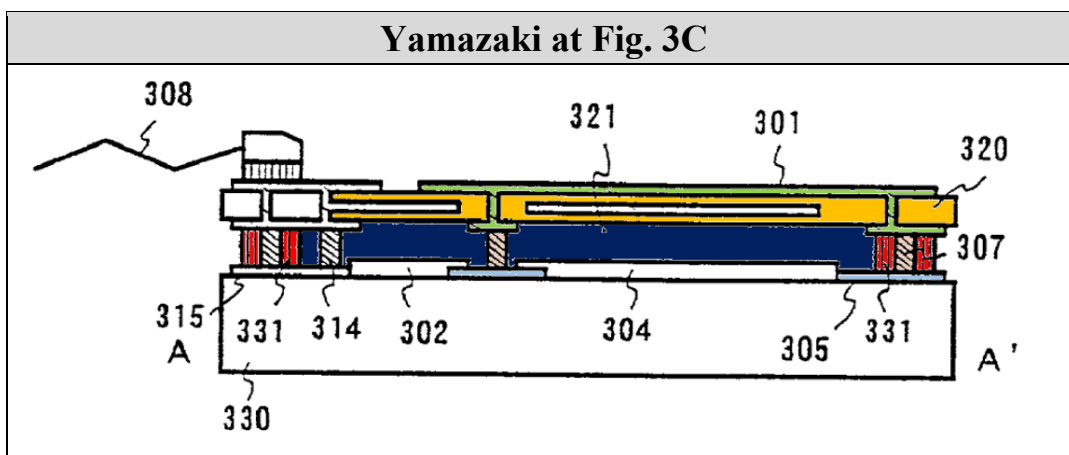


118. As shown in figure 3A above, each of the power supply lines (marked 305) is provided at least two contact holes to connect it with the auxiliary power supply line (marked 301) above. Figure 3C, reproduced below, shows a cross sectional view cut across the lines marked “A” to “A” in figure 3A. It shows two holes formed in the printed wiring board 320 (evidenced by the green auxiliary current supply line material that permeates it) and two conductors 307 (indicated by the diagonal pattern highlighted in pale red) that connect the auxiliary current supply line 301 to the current supply line 305 below. This indicates the existence of multiple contact holes electrically connecting 301 line (i.e., first power line) to the 305 line (i.e., second power line). A contact hole is formed in a material in order to provide a “contact” between two conductors. Each hole formed in printed wiring board 320 constitutes a contact hole because it allows the wiring on top of printed wiring board 320 to pass through to the bottom of printed wiring board 320 and carry a signal. The conductor on the left hand side of figure 3C indicates the existence of a contact hole formed in the resin (indicated by dark blue) that further allows the 301 line to connect to the 305 line (indicated in pale blue). The conductor on the right hand side of figure 3C indicates the existence of a contact hole formed in the sealing agent 331 that further allows the 301 line to connect to the 305 line (indicated in pale blue). As also demonstrated by figure 3A above, which shows the cross sectional line corresponding to figure 3C, the 305 line passes

through the pixel region 304.



119. Yamazaki discloses an inter-layer insulating film disposed between the first and second power lines. Figure 3C of Yamazaki's "Embodiment Mode," shows a cross sectional view of figure 3A discussed above. Figure 3C illustrates the current supply auxiliary line 301 (i.e., the "first power line" shown in green) disposed in a layer on a printed wiring board 320 (shown in orange) and current supply line 305 (i.e., the "second power line" shown in blue) disposed in a layer on the substrate 330. *See* EX-1008 at [0038]-[0043]. This figure also depicts conductors 307 (shown in pale red) accommodated by the contact holes to connect the auxiliary current supply line to the current supply line. Aside from these conductors, the current supply auxiliary line 301 and current supply line 305 are otherwise electrically insulated from one another. In the space between the layer containing line 301 and line 305, there is a "printed wiring board 320" (*see id.* at [0044]), a material such as a "thermosetting [or] silicone resin" "filled in an airtight space 321 between the . . . substrate 330 and the printed wiring board 320" (*see id.* at [0045]), and a "sealing agent 331" (*see id.* at [0043]). The printed wiring board provides a surface upon which the auxiliary current supply line 301 can be disposed. A sealing agent surrounds the conductor 307 (given the common pattern on both sides of conductor 307) and facilitates bonding of the printed wiring board to the substrate below. The resin also helps fill the space between the printed wiring board and the substrate below without creating unwanted electrical connections.



120. Any of these components individually (the printed wiring board 320 shown in orange, the resin (filled in the space signified by dark blue), and the sealing agent 331 shown in bright red), or the components collectively, constitute an inter-layer insulating film. These components are “inter-layer” because they are disposed between the layers in which the auxiliary and “regular” current supply lines are formed. These components are “insulating” because they do not conduct electricity. For example a resin, such as a thermosetting resin, does not conduct electricity and simply serves to bond the printed wiring board to the substrate. These components are “film” because they are disposed as a thin region on the top or bottom of another layer. For example, a resin covers the substrate and the current supply wiring 305. *See* EX-1008 at [0044]-[0045]. As another example, the printed wiring board is a thin region that covers the top portion of auxiliary current supply line 301 relative to everything below it. *See id.* at [0015]-[0016].

IX. GROUND 2

121. In my opinion, Koyama 168 in combination with Koyama 604 and/or Koyama 671 renders obvious claim 1.

A. Koyama References

122. Published Patent Application No. 2001/0043168 (“Koyama 168”) is a published patent application filed by Semiconductor Energy Laboratory Co. Ltd. and invented by Jun Koyama and Hajime Kimura. Koyama 168 was filed May 7,

2000 and published November 22, 2001 (both before the October 7, 2002 Critical Date of the '267 patent). I understand that Koyama 168 therefore qualifies as prior art to the '267 patent under pre-AIA 102(a) and (e).

123. U.S. Patent No. 6,124,604 (“Koyama 604”) is a U.S. patent filed by Semiconductor Energy Laboratory Co. Ltd. and invented by Jun Koyama, Hisashi Ohtani, Yasushi Ogata, and Shunpei Yamazaki. Koyama 604 was filed December 22, 1997 and issued September 26, 2000 (both before the October 7, 2002 Critical Date of the '267 patent). I understand that Koyama 604 therefore qualifies as prior art to the '267 patent under pre-AIA 102(b).

124. U.S. Published App. No. 2002/0053671 (“Koyama 671”) is a published U.S. patent application filed by Semiconductor Energy Laboratory Co. Ltd. and invented by Jun Koyama. Koyama 671 was filed November 9, 2001 and published May 9, 2002 (both before the October 7, 2002 Critical Date of the '267 patent). I understand that Koyama 671 therefore qualifies as prior art to the '267 patent under pre-AIA 102(a) and (e).

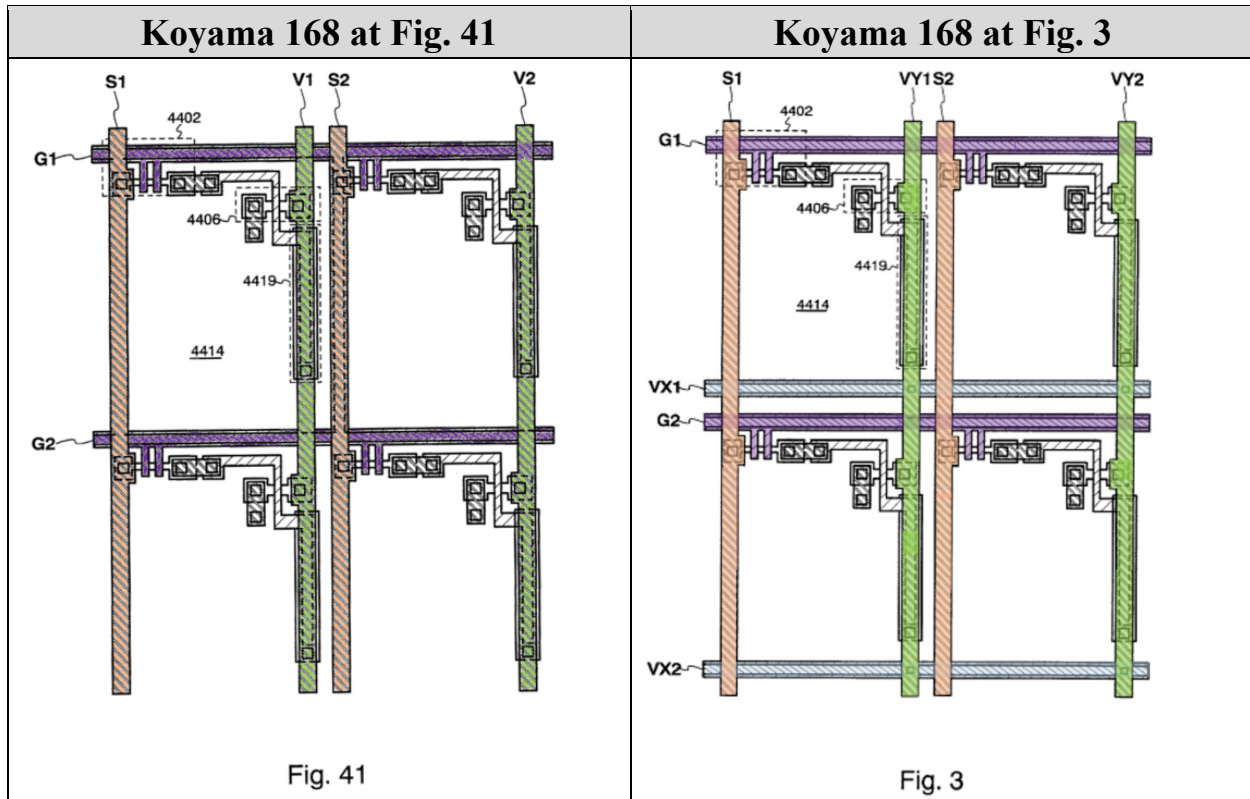
B. The Koyama Combination

125. A POSITA would have been motivated to modify Koyama 168 in view of Koyama 604 and/or Koyama 671 to form what I describe in this declaration as the “Koyama Combination.”

126. Koyama 168 discloses an electroluminescent display. *See* EX-1010 at

[0002]; *see also id.* at [0003]-[0051] (providing background of such displays). It acknowledges that, as a general electrical phenomenon, “electrical potential” or “voltage” can drop across a line, especially at points that are increasingly farther from the source of that line. *See id.* at [0014]-[0023]. Koyama 168 taught that this phenomenon could be a problem in the context of electroluminescent displays since power supply lines must distribute voltage and current to pixels for the pixels to emit light, and that potential can drop the farther from the source it is. *See id.*

127. Koyama 168 thus provides a plurality of power lines for “alleviating potential drop due to wiring resistance of a power supply line, in particular, potential drop due to wiring resistance at a portion where the power supply line is drawn out.” *Id.* at [0053]. Specifically, “[b]y drawing out the power supply lines in two directions of the display device . . . compared with a case where the power supply lines are drawn out in one direction, the length of the wiring from the power supply lines of the pixel portion to the external input terminals can be shorter and the variation in the length of the wiring can be decreased. By the above structure, the influence of the potential drop at the drawn-around portion of the power supply lines around the pixel portion can be decreased.” EX-1010 at [0133]-[0134].

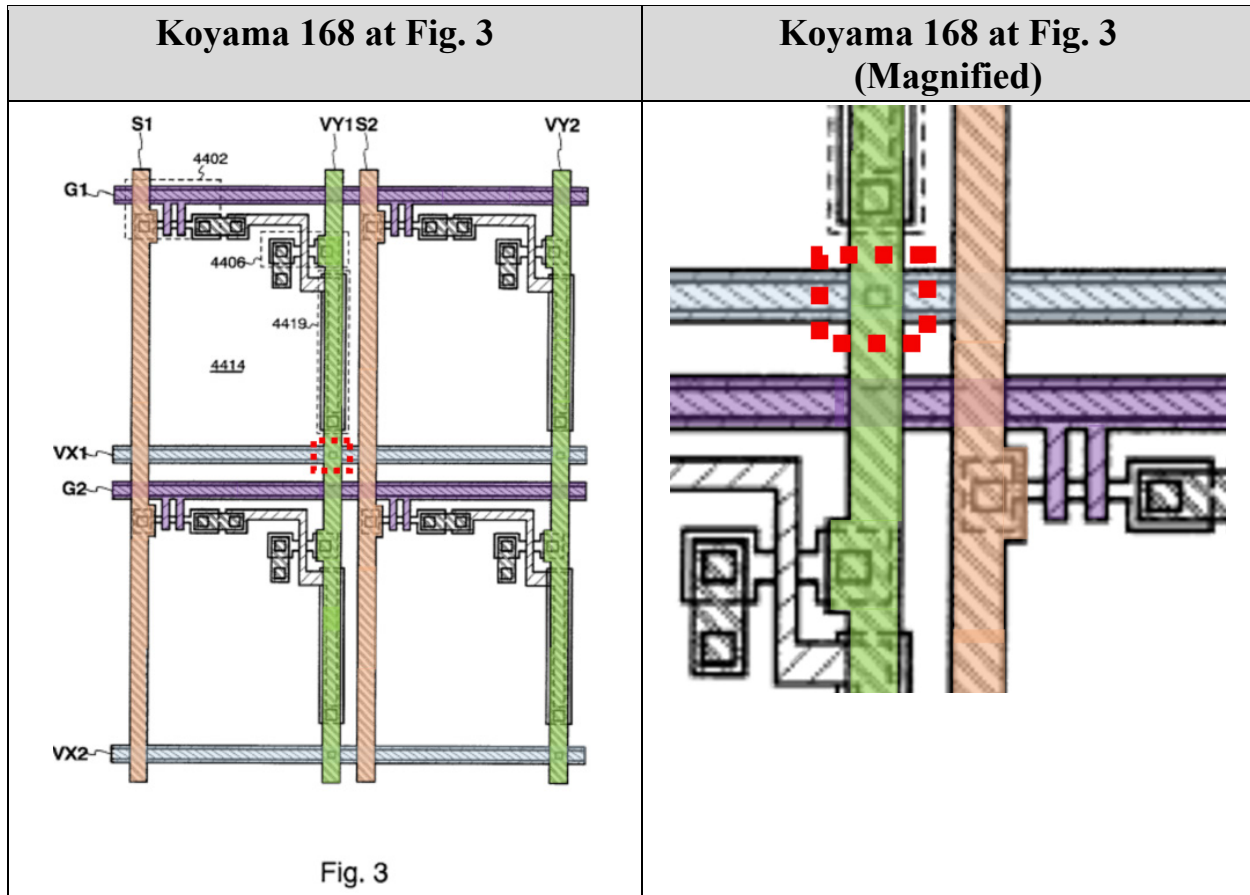


128. A POSITA would have recognized that Koyama 604 could be further improved and would have been motivated to do so.

129. A POSITA would have been motivated to increase the number of contact holes that connect Koyama 168's VY power supply lines and VX power supply lines. In an ideal circuit, the power supply lines would have no resistance whatsoever, and therefore would experience no potential drop. *See id.* at [0145] (stating basic circuit principle that potential drop "IR" depends upon wiring resistance "R"). Although adding an additional power supply line improved the even distribution of voltage and current in a display, these power supply lines would still have exhibited some amount of resistance, as all conductors do. A POSITA would

have thus been motivated to further reduce resistance. A POSITA would have recognized that adding additional contact holes to connect the VY and VX power supply lines would reduce the resistance between those lines, by providing a stronger electrical connection. Koyama 604, for example, taught this: “As the number of contact holes . . . for connecting [wiring lines] increases, the electrical connection between the [those lines] becomes better, that is, the contact resistance decreases, whereby the electric resistance of the combination of the [lines] decreases.” EX-1011 at 6:16-23. Thus, a POSITA implementing Koyama 168, which used a single contact hole to connect two power lines, would have understood that wiring resistance could be advantageously further reduced by increasing the number of contact holes that connect those lines, as taught by Koyama 604.

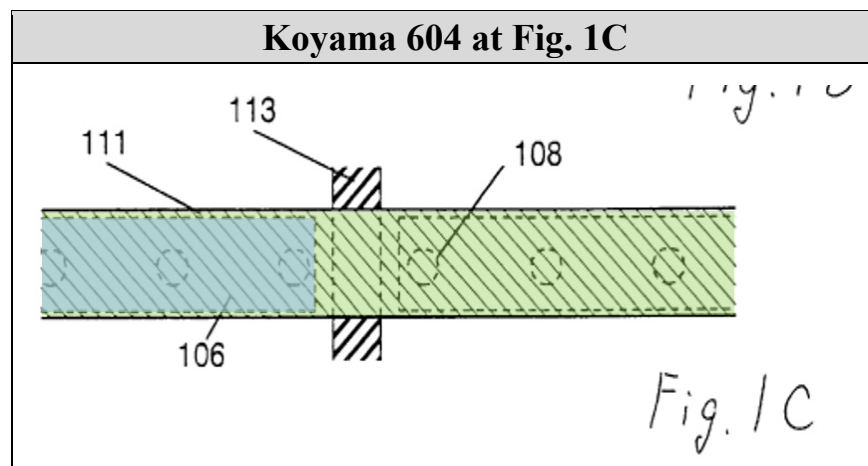
130. A POSITA would have been motivated to modify Koyama 168’s VY power supply lines to feature protrusions to accommodate the increased number of contact holes. As shown in Koyama 168’s figure 3 reproduced below, the reference’s VY power supply line is large enough to accommodate one contact hole at the intersections between VY and VX. However, it is not large enough to accommodate more than one contact hole of the same size.



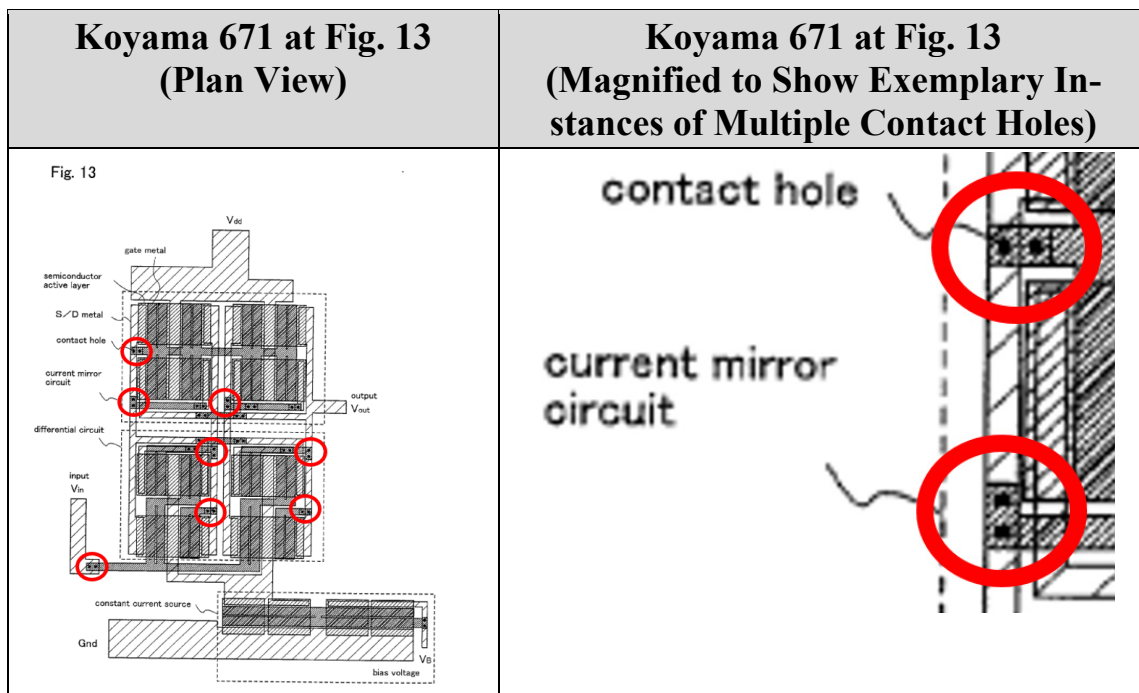
131. A POSITA would have understood that one of only a few ways to accommodate contact holes to improve the connection between VY and VX would be to modify VY to protrude over VX. Making smaller contact holes that would fit into the existing VY width would not be a good idea because doing so would not improve conductivity. The conductivity of a conductor connecting two lines between a contact hole increases as its width increases. Making the conductors smaller would have decreased their conductivity and increased their resistance, undermining the purpose of adding more contact holes in the first place. Moreover, a POSITA would have found it desirable that the contact holes are generally the

same size to abide by design rules enforcing that semiconductor features have certain standard dimensions. If multiple contact holes of the same size were used, more overlap between the VY and VX power lines would be necessary. Only two options are evident in that regard. Either the VX line could protrude somewhat over the length of the VY line, or the VY line could protrude somewhat over the length of the VX line. A POSITA would have found it obvious to try both options. Whichever power supply line protruded would feature the “first portion” and “second portion” as claimed by the '267 patent, but for purposes of my analysis, a protruded version of the VY power supply line would constitute the “first power line.”

132. Both Koyama 604 and Koyama 671 taught a protrusion as a way to accommodate additional contact holes. Koyama 604 features such a protrusion of “wiring line 111” (in green) over “auxiliary wiring line 106” (in blue) to accommodate a plurality of contact holes 108 that are formed through the interlayer insulating film 107.” *Id.* at 5:55-58; *see also id.* at 5:59-67.

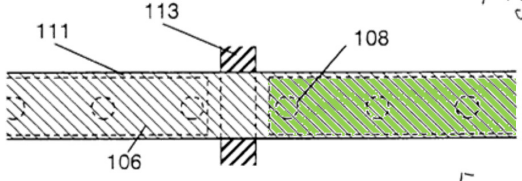
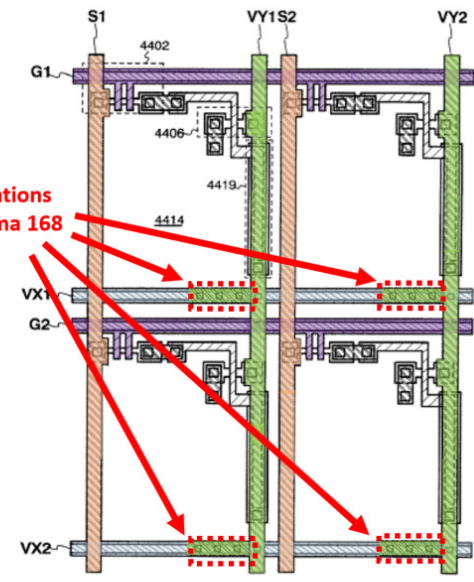
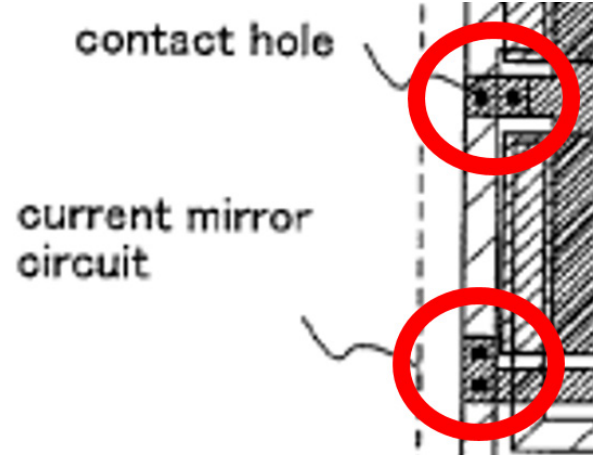


133. Koyama 671's figure 13 also depicts the use of a protrusion extending from the main part of a line as the mechanism of creating the overlap needed for multiple contact holes. In Figure 13's plan view, which models how the circuit would be physically manufactured, various portions formed in the "S/D metal" layer, the "gate metal" layer, and the "semiconductor active" layer electrically connect to each other through contact holes to implement Figure 12's schematic.



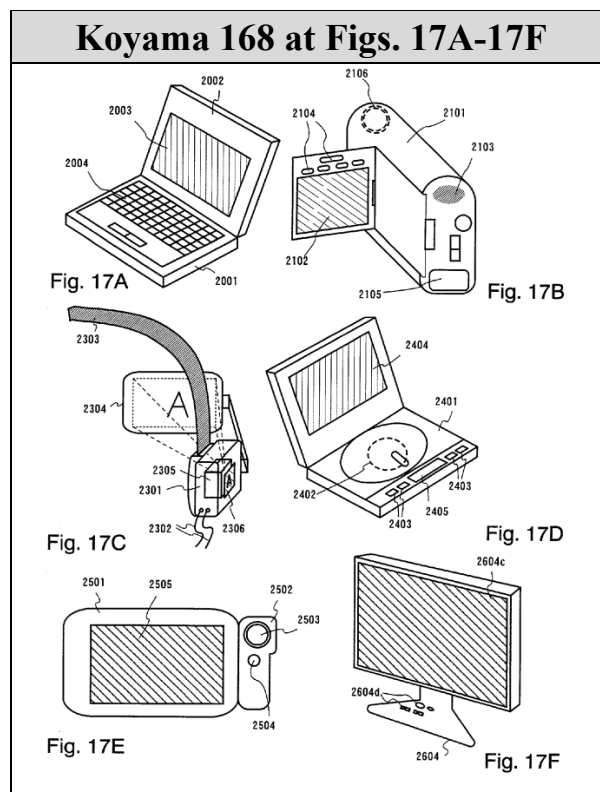
134. A POSITA would have had a reasonable expectation of success in making the proposed combination. Koyama 168, Koyama 604, and Koyama 671 all pertain to electroluminescent displays. Koyama 168 and Koyama 604 both aim to decrease the problem of potential or voltage drop by reducing the resistance of wiring carrying that voltage. EX-1010 at [0149] (reducing wiring resistance by laying out power supply lines in matrix pattern); EX-1011 at 6:16-23 (noting that

increasing number of contact holes reduces wiring resistance). Moreover, there are no obstacles to extending the VY power supply lines over the VY power supply to accommodate more contact holes. Both the power supply lines and the contact holes in Koyama 168 are created by patterning layers as was well known in the semiconductor device manufacturing process. The pattern could be laid down to accommodate a protrusion from VY power supply lines and more contact holes.

Koyama 604 at Fig. 1C	Koyama 168 at Fig. 3
 Fig. 1C	 Fig. 3
Koyama 671 at Fig. 13 (Magnified to Show Exemplary Instances of Multiple Contact Holes)  contact hole current mirror circuit	

C. '267 Patent Claim 1 Mapped to the Koyama Combination

135. The Koyama Combination renders obvious an “electro-optical device.” Koyama 168, for example, discloses various types of “electronic equipment” that can implement its teachings. *See* Koyama 168 at [0438]-[0448]; *see also id.* at [0448] (noting that Embodiment 19 can be “freely combined” with any of the foregoing embodiments.). For example, the “personal computer” disclosed by Koyama 168’s figure 17A constitutes an exemplary electro-optical device. *See id.* at [0441], Fig. 17A.



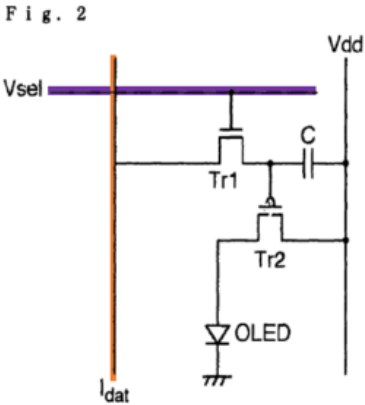
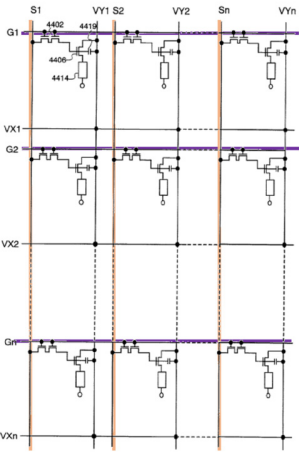
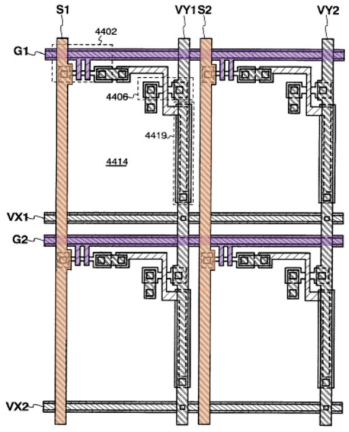
136. The Koyama Combination renders obvious a “scan line” and a “data line that intersects the scan line.” Koyama 168 taught that electroluminescent displays feature “gate signal line[s] (G1 to Gy) for inputting a selected signal from a

gate signal line driver circuit . . . to a gate electrode of a switching TFT 1801 of the respective pixels” and “source signal line[s] (also called data signal line[s]) (S1 to Sx) for inputting an analog video signal” connected the “source region and a drain region of the switching TFT 1801 of the respective pixels.” *See* EX-1010 at [0013], Fig. 18. Koyama 168’s “Embodiment Mode 4,” implements an electroluminescent display, and thus features these gate signal lines (designated by “G” lines) and source signal lines (designated by “S” lines), as shown in figures 2 and 3. These gate signal and source signal lines work together to form an image. The gate signal lines control the gates of the “switching TFTs” of various pixels, turning them on at desired times. *See id.* at [0020], Fig. 19. When a given switching TFT is turned on, it allows the video signal carried by a source signal line to pass through to the driving TFT corresponding to that switching TFT, causing the corresponding EL element to emit light. *See id.*

137. Each of the gate signal lines in Koyama 168 constitutes a “scan line” because it controls the gate terminal of a switching transistor. *See* EX-1001 at 5:6-31 (describing the “switching transistor Tr1” as comprising a “gate terminal . . . connected to the scan line V_{sel} ”). Each of the source signal lines in Koyama 168 constitutes a “data line” because it passes data signals that cause the EL elements to emit light. *See id.* at 5:21-31 (explaining how data signals result in light-emission).

138. Koyama 168's source signal lines (i.e., "data lines") intersect the gate signal lines (i.e., "scan lines") as shown in Koyama 168's figure 3.

139. The table below illustrates the correlation between the '267 patent's scan lines (Vsel) and Koyama 168's gate signal lines (G) (all highlighted in purple) and between the '267 patent's data lines (Idat) and Koyama '168's source signal lines (S) (all highlighted in brown).

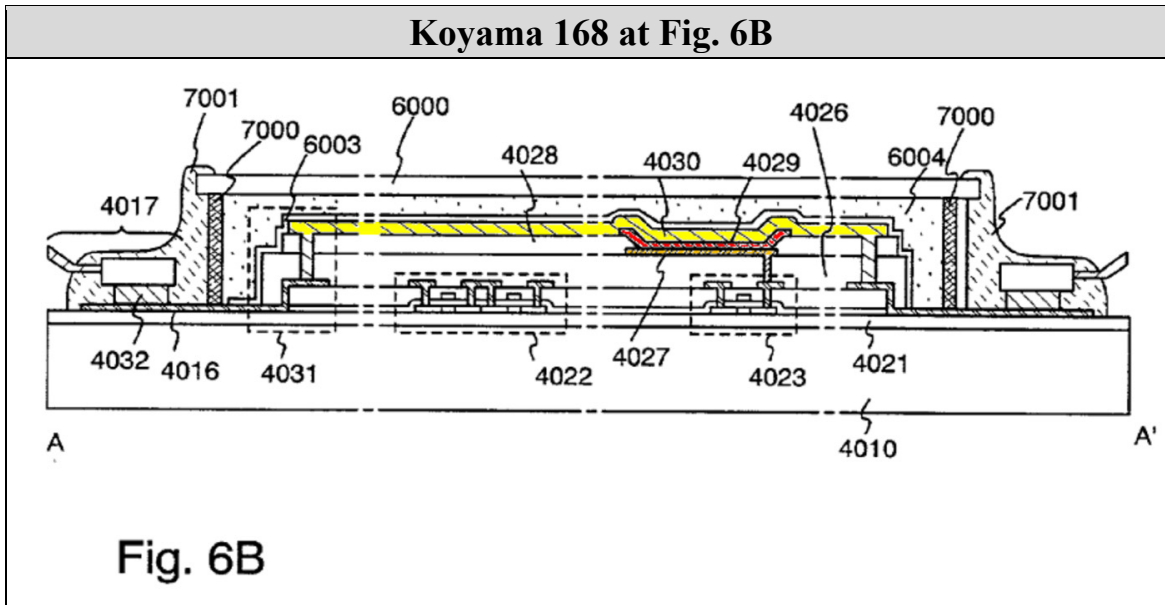
'267 Patent at Fig. 2	Koyama 168 at Fig. 2 (Schematic View)	Koyama 168 at Fig. 3 (Plan View)
 Fig. 2	 Fig. 2	 Fig. 3

140. The Koyama Combination renders obvious a "light emission layer" disposed between first and second "electrodes." Koyama 168 taught that electroluminescent displays feature "EL elements" 1806 each "composed of an anode, a cathode, and an EL layer sandwiched therebetween." See EX-1010 at [0015] (referring to the anode and cathode as "opposing electrodes"); see also *id.* at [0007], Fig. 18. Koyama 168's "Embodiment Mode 4" implements an electroluminescent display, and thus features these EL elements having electrodes sandwiching an EL

layer, as shown by element 4414 depicted in figures 2 and 3. *See id.* at [0148]-[0149], [0162].

141. Koyama 168's "electrodes" constitute the first and the second electrode claimed by the '267 patent. As conventional for EL displays, these electrodes constitute an anode and a cathode. Either constitutes a first electrode and either constitutes a second electrode as claimed by the '267 patent. Koyama 168's "EL layer" stands for a "light-emitting layer" and thus constitutes the "light emission layer" claimed by the '267 patent. *See id.* at [0007].

142. While Koyama 168's figures 2 and 3 focus on schematic and plan view representations, its figure 6B (corresponding to "Embodiment 5" which can be "freely combined" with other embodiments, *see* EX-1010 at [0198]) provides cross sectional views of EL elements, including the electrodes and the EL layer. *See* EX-1010 at [0177]-[0198] (referencing cross sectional view shown in figure 6B that shows "pixel electrode 4027," "EL layer 4029," and "cathode 4030"). Figure 6B, reproduced below, highlights the "pixel electrode 4027" (i.e., an example of a "first electrode") in orange, the "cathode 4030" (i.e., an example of a "second electrode") in yellow, and "EL layer 4029" (i.e., a "light emission layer" disposed between the two electrodes) in red.



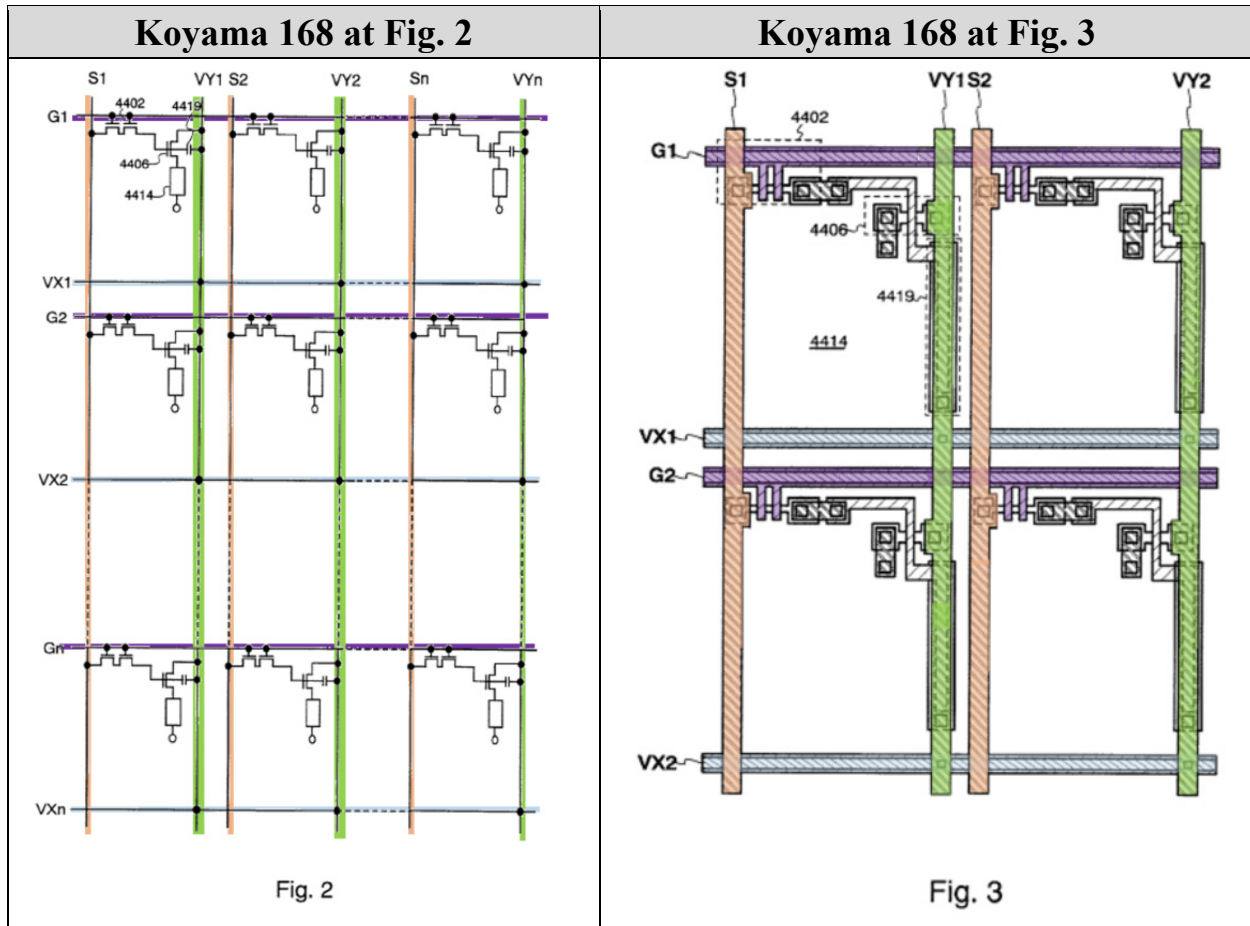
143. The Koyama Combination renders obvious a “first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction;” a “second power line that extends in the second direction” and overlaps “at least a part of” the first power line’s second portion;” and that the first power line’s second portion is electrically connected to the second power line “through [a] plurality of contact holes.”

144. Koyama 168 taught that conventional EL displays, which featured “power supply lines” emanating in one direction, could be improved by adding more power supply lines emanating in a second direction. Its figure 2 (corresponding to a schematic view of an “Embodiment Mode 4”) and its figure 3 (corresponding to “Embodiment 2” which features a top plan view “of the pixel portion of the circuit diagram illustrated in Fig. 2” *see* EX-1010 at [0160]) depict power supply

lines VY1-VYn disposed in a vertical direction and power supply lines VX1-VXn disposed in a horizontal direction. *See* EX-1010 at [0149], [0162].

145. Koyama 168's "power supply lines" constitute "power lines" as claimed in the '267 patent, because they supply power (in the way of voltage and current) to light-emitting elements. *See* EX-1010 at [0019] (describing power supply lines as "held at a constant power supply potential" which is a synonym for voltage), [0023], Fig. 2 (illustrating that the VX power supply lines electrically connect to VY power supply lines, which electrically connect to driving transistor 4406, which controls extent to which EL element 4414 emits light), [0149] (providing that description of figure 2).

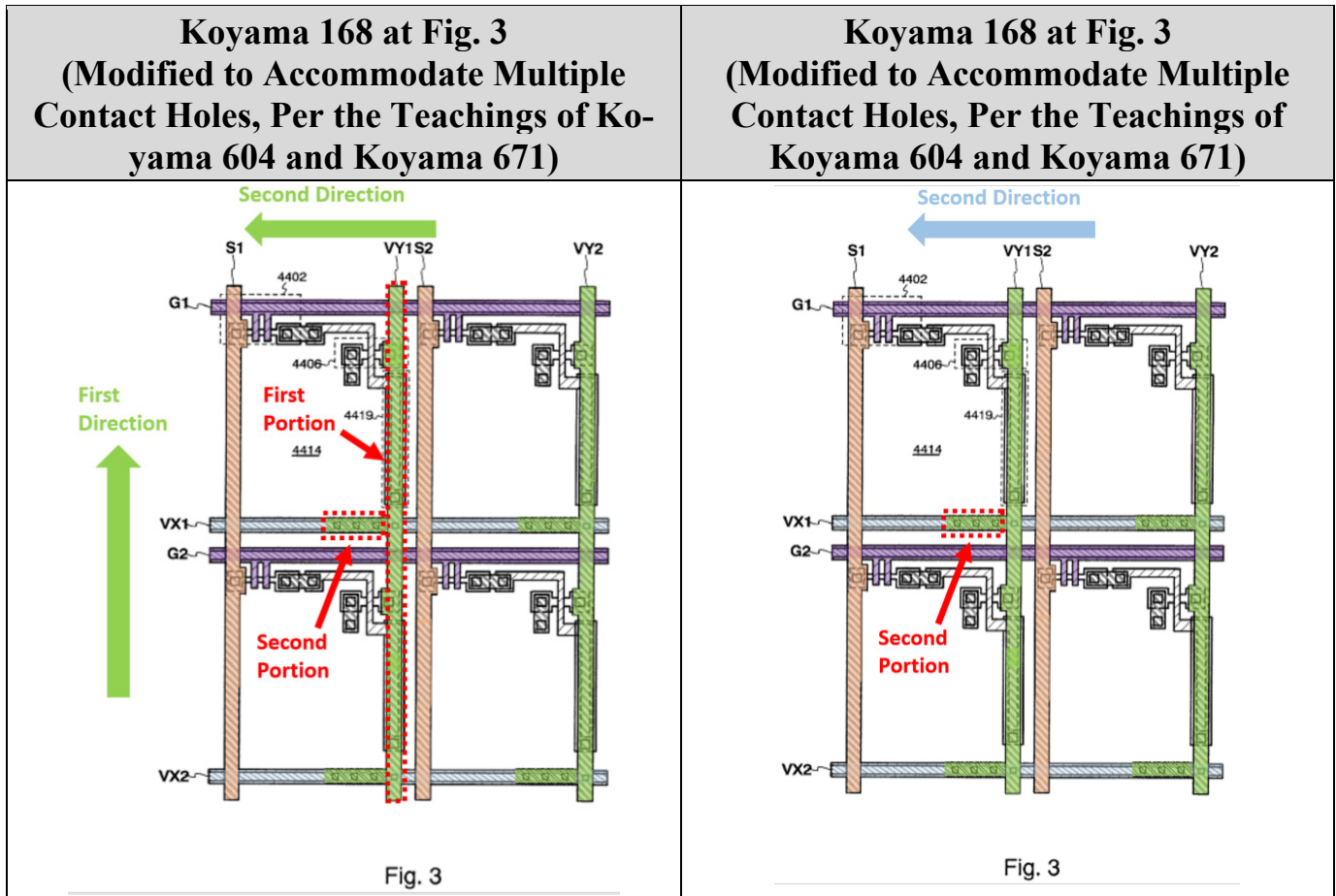
146. Koyama 168's VY power supply lines constitute "first power lines" that extend in a first direction (i.e., vertically). Koyama 168's VX power supply lines constitute "second power lines" that extend in a second direction (i.e., horizontally). These power lines are also connected to each other at their intersections, as signified by the black circle in figure 2's schematic and by the black box in figure 3's plan view. These figures are reproduced below to show the VY power supply lines in green and the VX power supply lines in blue.



147. Koyama 168, when modified to form the Koyama Combination, features power lines satisfying the limitations of the '267 patent. When modified, Koyama 168's vertical "VY" power supply lines feature protrusions to accommodate multiple contact holes to strengthen the electrical connection to its horizontal "VX" power supply lines. Each modified "VY" power supply line constitutes a power line having a first portion that extends in a first direction (i.e., the bulk of the power supply line extends in the vertical direction) and having a second portion that extends in a second direction that intersects the first direction (i.e., the protrusion extends in the horizontal direction). Each "VX" power supply line constitutes

a power line extending in the second direction (i.e., the horizontal direction) and overlaps with the first power line's protrusion. In the overlap (i.e., the first power line's second portion) the lines are electrically connected through a plurality of contact holes, each signified by a box in the modified Koyama 168 figure 3 reproduced below.

148. Koyama 168, as modified as discussed above, is shown by the table below. Each VY power supply line (i.e., the "first power line"), its portions, and its directions are shown in green; each VX power supply line (i.e., the "second power line"), its portions, and its directions are shown in blue; and the multiple contact holes are shown as boxes encompassed in the second protrusion.

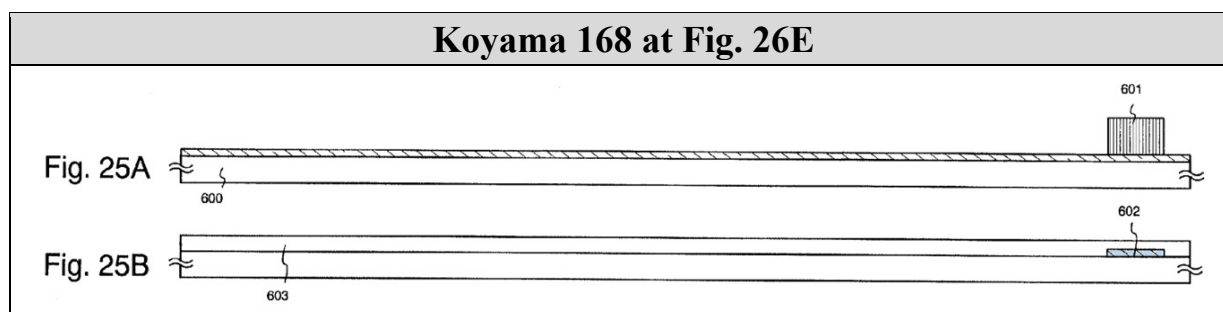


149. The Koyama Combination renders obvious an inter-layer insulating film disposed between the first and second power lines.

150. As a preliminary matter, Koyama 168's VY and VX power supply lines connect to each other at their intersections. A POSITA would have understood that these power supply lines do not, however, connect to each other outside of these intersections, and as a general matter in semiconductor devices, insulating films are deposited between different layers—including the layers in which the power supply lines are formed—to prevent undesired electrical shorting.

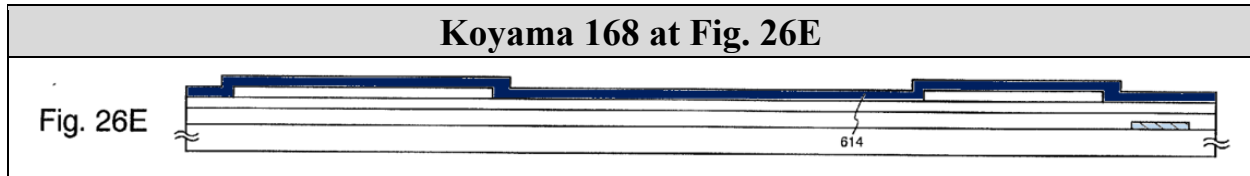
151. Koyama 168 also expressly depicts an inter-layer insulating film disposed between the vertically oriented power lines (i.e., the “first power line”) and the horizontally oriented power lines (i.e., the “second power line”). Koyama 168 describes how an EL display can be built, layer-by-layer, including how an inter-layer insulating film is formed between the VY and VX power supply lines. It discloses an “Embodiment 10” that shows a “method of manufacturing the pixel portion of an EL display in accordance with the present invention.” *See* EX-1010 at [0244]-[0290], Figs. 11-14. It also discloses an “Embodiment 17” that shows a case “where the irradiation direction of light of the EL display device is to the lower surface direction” focusing on “a basic unit regarding the driving circuit” that “may be manufactured using the manufacturing method described in Embodiment 10.” *See id.* at [0346]-[0391], Figs. 25-29.

152. Figures 25A and 25B, reproduced below, show how “etching is performed to form a power source supply line 602.” *See id.* at [0348].

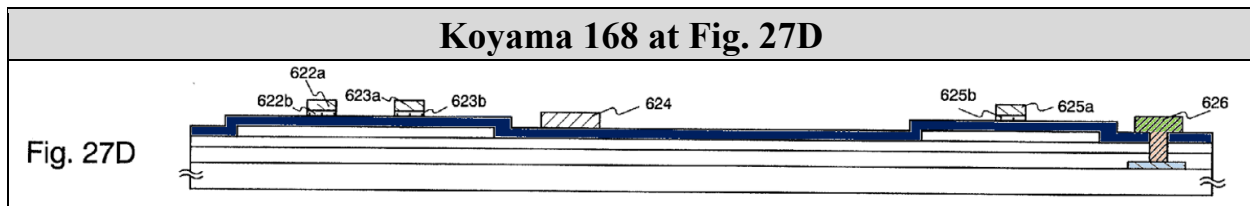


153. Later in the manufacturing process, “a gate insulating film 614 with a thickness of approximately 80 nm is formed.” *See id.* at [0359]. Because this gate

“insulating film” 614 is formed between layers, as shown by later figures in the manufacturing process, it also constitutes an “inter-layer insulating film.” The gate insulating film is shown in dark blue in the table below.



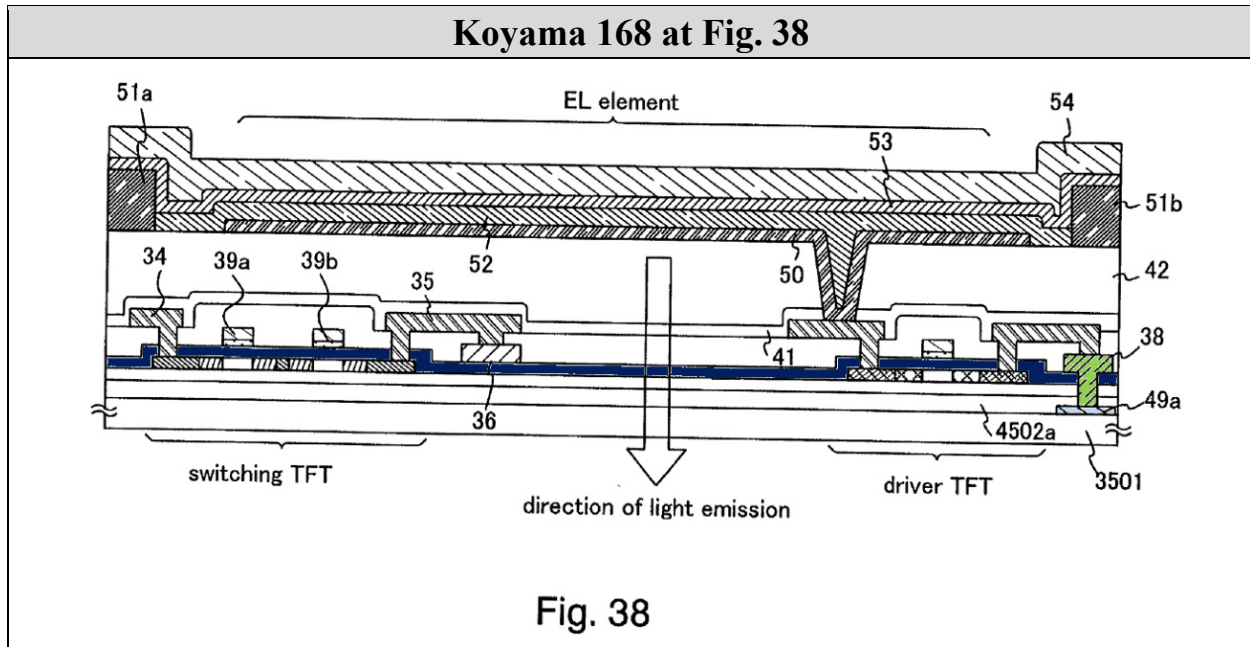
154. Later in the manufacturing process, “a conductive film with a thickness of 200 to 400 nm is formed and patterned to form . . . the power source electrode 626.” *Id.* at [0366]. This power source electrode connects to the power supply line 602 via a contact hole. *See id.* at [0379] (describing in later stage that “a contact hole is formed with respect to the first interlayer insulating film 646 and the gate insulating film 614, and the source wirings 647, 650 and the drain wirings 652, 653 are formed.”).



155. The green element 626 corresponds to the vertically oriented power supply lines (VY). This is confirmed by noting that it has the same shape and location as element “power supply line 38” shown in the finished product shown in figure 38. This particular wiring connects to the source or drain of the driving TFT, which is how the VY power line depicted in figure 3 is connected.

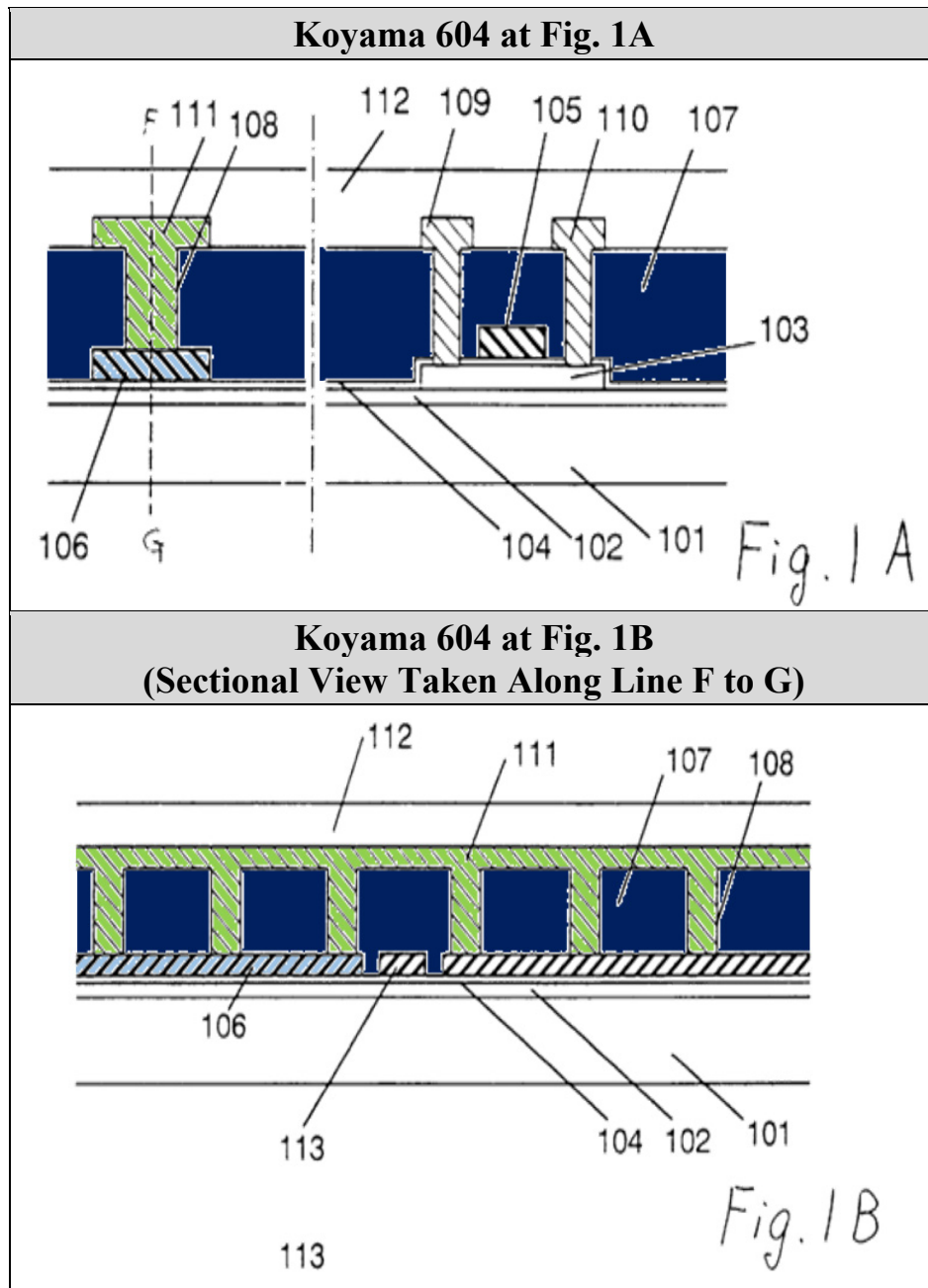
156. The pale blue element 602 corresponds to the horizontally oriented power supply lines (VX). This is confirmed by noting that it has the same shape and location as element “49a” shown in the finished product shown in figure 38. This particular wiring connects to the “power supply line 38” above it, which is how the VX power line depicted in figure 3 is connected.

157. Koyama 168’s “Embodiment 16” (depicted by figures 36 and 38) corresponds to a description of “Embodiment 2” (depicted by figure 3 discussed above) in which “a wiring layer different to that of the source signal line and the gate signal line are added to form the power supply line.” *See* EX-1010 at [0337]-[0345]. Figure 38, reproduced below, shows “power supply line 38” (highlighted in green) and “power supply line 49a” (highlighted in blue) provided at a lower layer. *See* EX-1010 at [0219], [0341]. An inter-layer insulating film (highlighted in dark blue) lies between those two layers. Additionally, the layers below the gate insulating film 614—silicon nitride oxide films 603 and 604 described in the preceding cross sectional views—also serve an insulating purpose, are disposed as films, and are sandwiched between layers, meaning that they would also constitute inter-layer insulating films.



158. A POSITA would also have found it obvious to use inter-layer insulating films between power lines in light of the teachings of Koyama 604 and Koyama 671.

159. In Koyama 604, a “wiring line 111” connects “in parallel to an auxiliary wiring line 106 via a plurality of contact holes 108 that are formed through the interlayer insulating film 107.” EX-1011 at 5:55-58; *see also id.* at 5:59-67. As in the '267 patent, Koyama 604's interlayer insulating film allows one layer to be disposed above another without creating unwanted electrical connections in between. Koyama 604's figures 1A and 1B are reproduced below and highlight this film in dark blue. *See id.* at 5:43-7:49.



160. Koyama 671's figures 23A and 23B also show "a first interlayer insulating film 357" and a "second interlayer insulating film 358" disposed between the layers. *See* EX-1012 at [0224]-[0235]. Figure 24 also shows that that contact holes (which are evidenced by the pillars shown in figure 24) pass through these

368

333 329 391 350 353 392

501:n-channel TFT 502:p-channel TFT

506:driver circuit

372

370 369 371 368

336 344 394

505:condenser 503:switching TFT

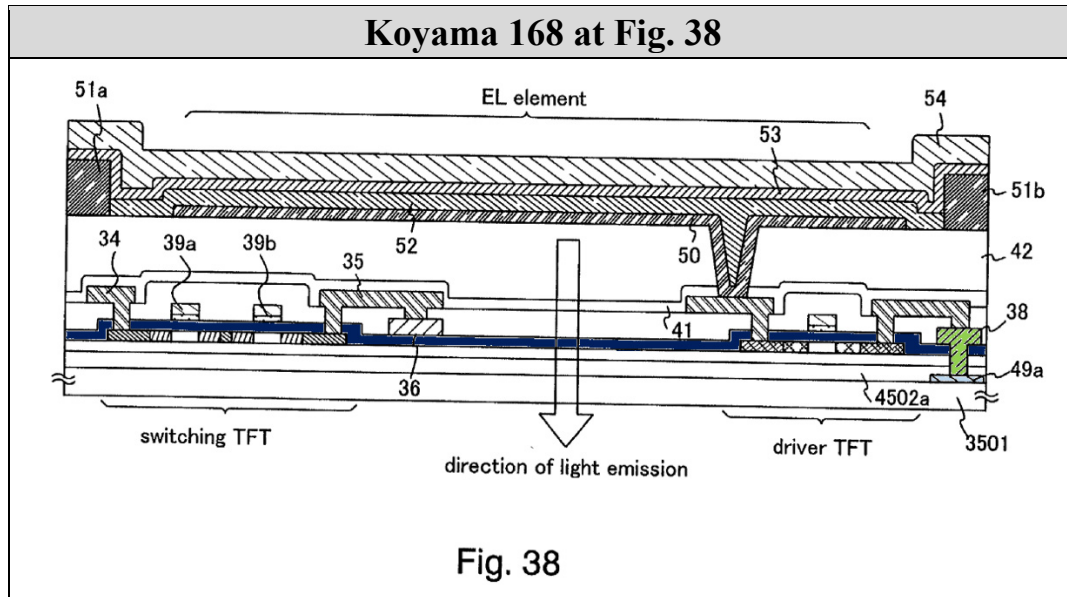
352 355 395

504:EL driver TFT

507:pixel portion

94

and second power lines. As shown in Koyama 168's figure 3, these first and second power lines are made to electrically connect to one another at only specific areas. *See, e.g.*, EX-1010 at [0379] (discussing contact holes "formed with respect to the first interlayer insulating film"). Koyama 168's figure 38 shows that these two power lines can be deposited at different layers. For example the power line reflected by element 38 (shown in green in the figure below) appears at a higher layer than the power line reflected by element 49a (shown in pale blue). A POSITA could have used Koyama 604's and Koyama 671's inter-layer insulating films between Koyama 168's power lines to insulate those power lines (being at different layers) while also accommodating contact holes where necessary to make connections. A POSITA would have had a reasonable expectation of success in making the proposed combination since all three references teach the use of inter-layer insulating films to electrically isolate different layers.



X. CONCLUSION

162. I reserve the right to supplement my opinions to address any information obtained, or positions taken, based on any new information introduced throughout this proceeding.

163. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both (under Section 1001 of Title 18 of the United States Code).

By: 

David K. Liu, Ph.D.

April 6, 2023

APPENDIX A

DAVID KUAN-YU LIU, Ph.D.

42063 Benbow Drive, Fremont, CA 94539 • (510) 770-9449 or (510) 579-5029

www.davidkyliu.com davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

KEY EXPERT WORK EXPERIENCE:

Case:	Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,
Jurisdiction:	Civil Action No. 2:21-cv-00463 Eastern District of Texas
Work Product:	Expert relating to memory modules.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Tony Nguyen)
Date:	8/22 – Current

Case: **Vervain, LLC vs. *Micron Technology* & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents, all 4 petitions instituted, and deposed on both initial declaration and reply declaration.
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared Bobrow)
Date: 8/21 – Current

Case: **Monterey Research vs. *Qualcomm* PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – Current

Case: ***Semiconductor Energy Laboratory Co., OLED Patent Matters***
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: ***Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: ***Texas Instruments IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: ***Micron Technology vs. UMC/JinHua***
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – Current

Case: ***SK Hynix vs. BitMicro***
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaianni)
Date: 11/18 – 4/19

Case: ***Rohm Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)
Date: 4/18 – 8/18

Case: ***Apple Inc., vs. Qualcomm Incorporated***
Jurisdiction: Case No. 3:17-CV-02402
United States District Court for the Southern District of California
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, 2 depositions taken.
Counsel: Fish & Richardson (Contact: Tony Nguyen)
Date: 1/18 – 5/19

Case: ***Macronix vs. Toshiba***
Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission
Work Product: Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity.
Nature of Case: ITC infringement case concerning advanced NAND Flash memory.
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 4/17 – 10/18

Case: *Novatek Microelectronics Corp. IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date: 2/17 – 4/17

Case: *Taiwan Semiconductor Manufacturing Company IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: *Triune Systems, LLC vs. Wayne Chen, et al.,*
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: ***Keranos, LLC v. Analog Devices et. al.***
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: ***Silicon Storage Technology, Inc. v. Xicor, LLC***
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35 μ m and 0.18 μ m CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00

Programmable Silicon Solutions, Sunnyvale, California

Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98

AMIC Technology, Santa Clara, California

Director of Flash Technology. Responsible for developing 0.35μm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97

Altera Corp., San Jose, California

Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35μm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96

Information Storage Devices, San Jose, California

Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5μm and 0.35μm flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.
9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994
10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.
13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.
14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.
16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.
17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.
19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.
20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.
21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.
22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.
23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.
24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.
25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997
26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.
27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.
28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.
29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998
30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.
31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.
32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.
33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.
34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.
35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.
37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.
38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.
39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.
40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.
41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.
42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.
43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.
44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.
45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.
46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.
47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.
48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.
49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.
50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.
51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.
52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.
53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.
54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.
55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.
57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.
58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.
59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.
60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.
61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.
62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.
63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.
64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.
65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.
66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.
67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.
68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.
69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.
72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010.
73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010
75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011
76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011
77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011
78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012
79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012
80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012
81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012
82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.
83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.
84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.
85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.
86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.
87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.
88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.
89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.
90. U.S. Patent 9,305,931, "Zero Cost NVM Cell Using High Voltage Devices in Analog Process," Issued April 5, 2016.

91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.
92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.
93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.
96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.
97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019
98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.
99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

(additional patent applications pending)

PUBLICATIONS

1. S.D. Leeke, D. K. Y. Liu and J. P. McVittie, "Plasma mode trench etching with direct hydrocarbon injection," *Materials Research Society Symposium Proceedings*, Vol. 68, pp. 21-27, 1986.
2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
9. K. T. San, C. Kaya, D. K. Y. Liu, T. P. Ma, and P. Shah, "A new technique for determining capacitive coupling coefficients in flash EPROMs," *IEEE Electron Device Letters*, Vol. 13, No. 6, pp. 328-331, 1992.
10. C. Kaya, D. K. Y. Liu, J. Paterson and P. Shah, "Buried source-side injection (BSSI) for flash EPROM programming," *IEEE Electron Device Letters*, Vol. 13, No. 9, pp. 465-467, 1992.
11. M. Wong, D. K. Y. Liu and S. S.-W. Huang, "Analysis of the subthreshold slope and the linear transconductance techniques for the extraction of the capacitance coupling coefficients of floating-gate devices," *IEEE Electron Device Letters*, Vol. 13, No. 11, pp. 566-568, 1992.
12. D. K. Y. Liu and J. D. Plummer, "Design and analysis of a new conductivity-modulated power MOSFET," *IEEE Transactions on Electron Devices*, Vol. 40, No. 2, pp. 428-438, 1993.
13. J. Z. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, Y. Sun, D. Liu, Y. Tang, J. Hsu, S. Luan, J. Lien, "Flash EPROM endurance simulation using physics-based models," In *International Electron Devices Meeting Technical Digest*, pp. 295-298, 1994.
14. J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, "Short Channel enhanced degradation during discharge of Flash EEPROM memory Cell," *International Electron Devices Meeting Technical Digest*, pp. 331-334, 1995.

15. V. H. Chan and D. Liu, "An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices," *IEEE Electron Devices Letters*, Vol. 20, No. 3, pp. 140-142, 1999.