

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Yojiro Matsueda and
Hayato Nakanishi
U.S. Patent No.: 8,164,267 Attorney Docket No.: 54108-0001IP2
Issue Date: April 24, 2012
Appl. Serial No.: 12/219,592
Filing Date: July 24, 2008
Title: ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND
ELECTRONIC APPARATUS

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 8,164,267 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

EX-1001	U.S. Patent No. 8,164,267 to Yojiro Matsueda and Hayato Nakanishi (“the ’267 patent”)
EX-1002	Excerpts of the Prosecution History of Japanese Application No. 2002-293696
EX-1003	Certified Translation of Excerpts from the Prosecution History of Japanese Application No. 2002-293696
EX-1004	The Prosecution History of U.S. Application No. 10/676,067
EX-1005	The Prosecution History of U.S. Application No. 12/219,592
EX-1006	Declaration of Dr. David K. Liu
EX-1007	U.S. Patent No. 6,825,820 (“Yamazaki 820”)
EX-1008	U.S. Published App. No. 2001/0015618 to Shunpei Yamazaki and Takeshi Fukunaga (“Yamazaki”)
EX-1009	U.S. Patent No 6,894,431 to Shunpei Yamazaki and Takeshi Fukunaga (“Issued Yamazaki”)
EX-1010	U.S. Published App. No. 2001/0043168 to Jun Koyama and Hajime Kimura (“Koyama 168”)
EX-1011	U.S. Patent No. 6,124,604 to Jun Koyama, Hisashi Ohtani, Yasushi Ogata, and Shunpei Yamazaki (“Koyama 604”)
EX-1012	U.S. Published App. No. 2002/0053671 to Jun Koyama (“Koyama 671”)

- EX-1013 Fabrice Caignet et al, The Challenge of Signal Integrity in Deep-Submicrometer CMOS Technology, 89 Proceedings of the IEEE, No. 4 (April 2001) (“Caignet”)
- EX-1014 Flat Panel Displays for Portable Systems by Kalluri R. Sarma and Tayo Akinwande, Journal of VLSI Signal Processing Systems 13, 165-190 (1996) (“Sarma”)
- EX-1015 Complaint, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (EDTEX)
- EX-1016 Joint Agreed Scheduling Order, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (EDTEX)
- EX-1017 Paul Horowitz and Winfield Hill, The Art of Electronics (Second Edition)
- EX-1018 U.S. Patent No. 6,858,991 to Takashi Miyazawa (“Miyazawa”)
- EX-1019 U.S. Published App. No. 2003/0076046 to Naoaki Komiya et al. (“Komiya”)
- EX-1020 U.S. Patent No. 6,633,135 to Shouji Nara et al. (“Nara”)

BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., Ltd., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. (“Petitioner”) petition for *Inter Partes* Review (“IPR”) of claim 1 (“Challenged Claim”) of U.S. Patent No. 8,164,267 (“the ’267 patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’267 Patent is available for IPR. The present petition is being filed within one year of service of a complaint against Petitioner. Petitioner is not barred or estopped from requesting this review.

B. Challenge and Relief Requested

Petitioner requests IPR on the grounds set forth below. Additional explanation and support is found in EX-1006, the Declaration of Dr. Liu.

Ground	Claim	Basis for Rejection
1	1	Anticipated by, and Obvious over, U.S. Published App. No. 2001/0015618 (“Yamazaki”)
2	1	Obvious over U.S. Published App. No. 2001/0043168 (“Koyama 168”) and U.S. Patent No. 6,124,604 (“Koyama 604”) or U.S. Published App. No. 2002/0053671 (“Koyama 671”) or both Koyama 604 and Koyama 671

These references qualify as prior art based on the earliest claimed priority date (10/7/2002; “Critical Date”), as shown below. Petitioner does not concede that the ’267 patent is entitled to the claimed priority.

Notably, these references were not considered during prosecution. *See generally* EX-1002.

Reference	Date	Statutory Ground
Yamazaki	8/23/2001 (publication)	§102(b)
Koyama 168	5/7/2000 (filing) 11/22/2001 (publication) 3/30/2004 (issuance)	§102(a) and (e)
Koyama 604	9/26/2000 (issuance)	§102(b)
Koyama 671	11/9/2001 (filing) 5/9/2002 (publication) 12/14/2004 (issuance)	§102(a) and (e)

C. Claim Construction

Based on the prior art’s description of the claimed elements being similar to that of the ’267 patent specification, no formal claim constructions are necessary in this proceeding because “claim terms need only be construed to the extent necessary to resolve the controversy.” *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011).¹

¹ Petitioner is not conceding that each claim satisfies all statutory requirements, such as §§101 and 112, nor is Petitioner waiving any arguments concerning claim

D. Level of Ordinary Skill in the Art

For purposes of IPR, a person of ordinary skill in the art at the time of alleged invention (“POSITA”) would have had at least a Master’s degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing. EX-1006, ¶¶ 26-27. Additional education can remedy lack of work experience and vice versa. *Id.*

II. SUMMARY OF THE ’267 PATENT

A. Brief Description

The ’267 patent generally relates to increasing the “aperture ratio” of an electroluminescent display’s pixels, while simultaneously maintaining the “same pixel pitch” across that display. EX-1001 at 2:10-13. In the context of electro-optical displays, “aperture ratio” generally refers to the ratio of a pixel’s light-sensitive area to the pixel’s total area. *See* EX-1006, ¶ 58. “Pixel pitch” refers to the distance between two pixels of the display. *See id.*

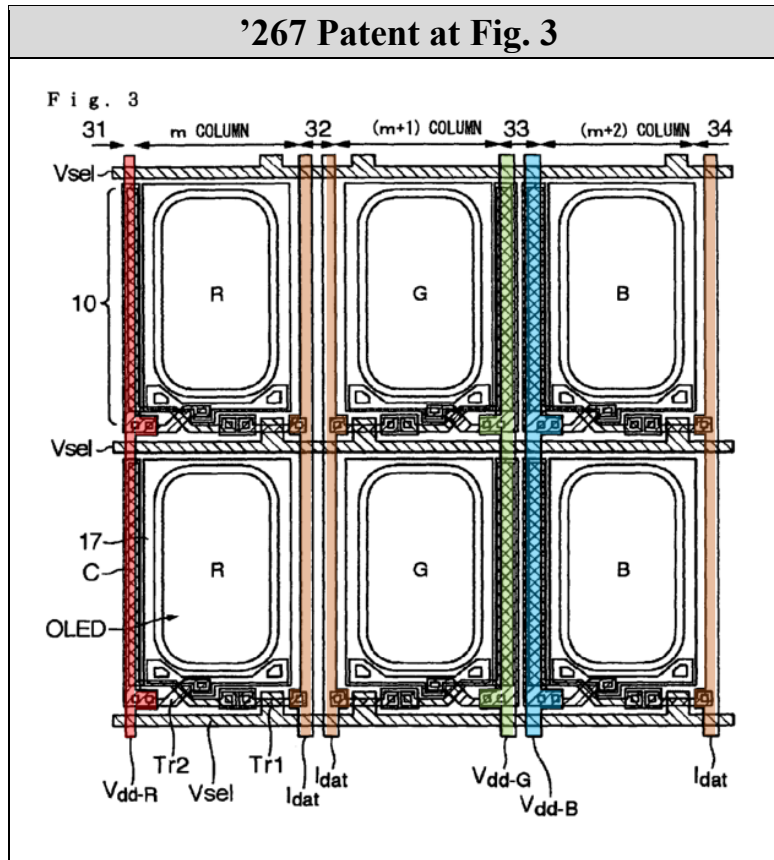
The ’267 patent teaches that, in conventional color electroluminescent displays, each pixel is disposed between a data line (on the left) and an electric power

scope or grounds that can only be raised in district court. For this petition, Petitioner applies prior art in a manner consistent with Patent Owner’s allegations of infringement before the district court.

line (on the right). EX-1001 at 1:30-42. Because “power consumption” varied by pixel color, “the optimal width of the electric power line is greatly different for each color.” *Id.* at 1:51-56. At the same time, the display’s “manufacturing process” required the pixel pitch across the display to remain the same. *See id.* at 1:56-63. To accommodate this requirement, while simultaneously allowing the most “power hungry” pixel color to receive adequate power, “the maximal width for disposing the electric power lines” was a primary factor in determining the pixel pitch. EX-1001 at 1:56-63. Yet increasing electric power line width comes “at the sacrifice of the aperture ratio.” *Id.* at 1:56-2:2. In other words, “with the conventional wiring layout, the width of the electric line and the aperture ratio of the pixel are in the relation of trade off [to] each other, and it is difficult to maintain a large aperture ratio while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.” *Id.* at 2:3-9.

The ’267 patent proposes rearranging power and data lines compared to conventional electro-optical displays to address this problem. Specifically, it discloses embodiments of pixel circuitry that group combinations of these lines in “line forming regions” of “generally the same width” that allow pixel pitch to be uniform, that maximize aperture ratio, and that ensure each pixel color receives adequate power. *See id.* at 2:14-25, 2:36-3:45.

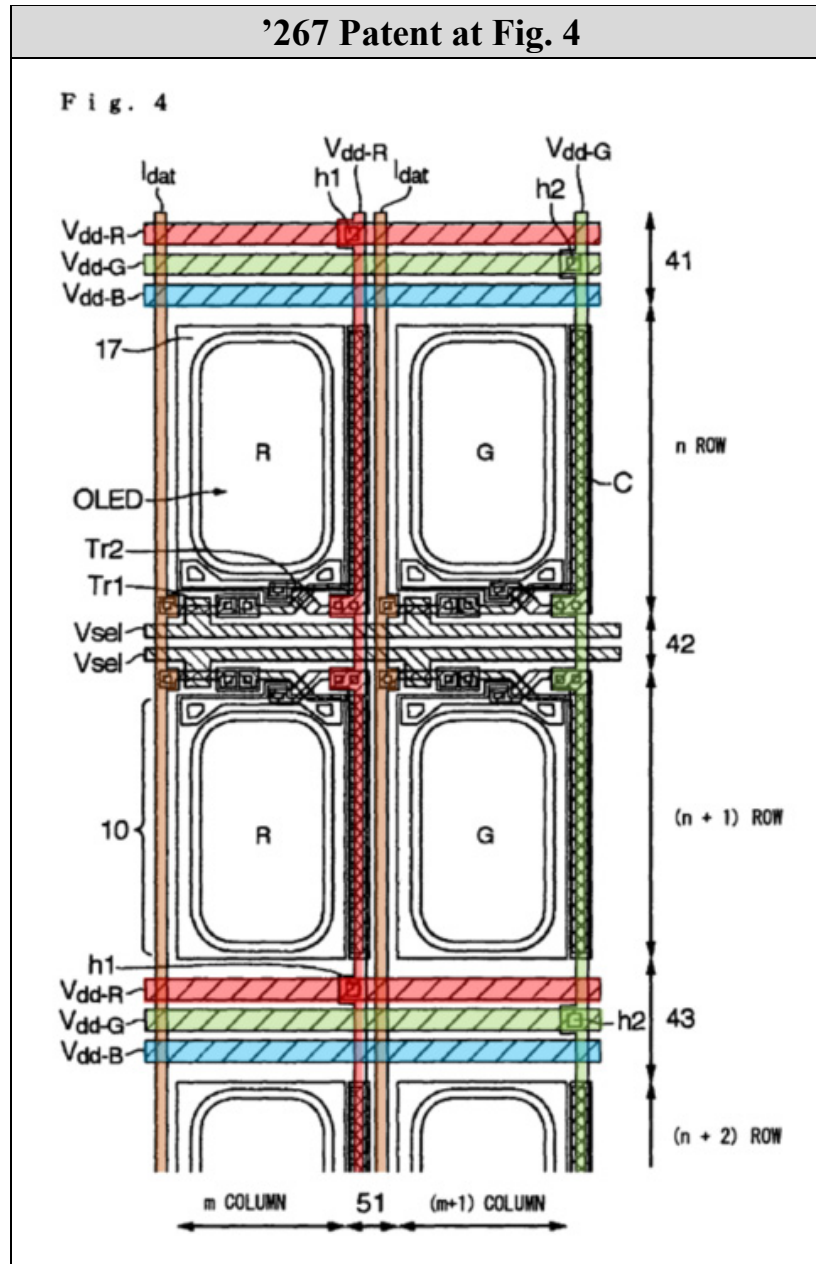
The patent's first embodiment involves "line forming regions" disposed between each column of pixels. *See* EX-1001 at 5:43-56; *see also generally id.* at 4:46-6:67, Figs. 1-3. To form these line forming regions with "the width the same as possible [sic]" combinations are "determined such that the total width of [a given] electric power line V_{dd} and the data line I_{dd} is approximately the same." *Id.* at 6:1-5. Having equal width lines allegedly facilitates having equal pixel pitch. *Id.* at 2:14-25. The '267 patent provides an example of electric power lines for different color pixels, where "width of V_{dd-G} [Green]>width of V_{dd-R} [Red]>width of V_{dd-B} [Blue]." *Id.* at 5:63-67, 6:5-13. To achieve line forming regions with approximately equal width, V_{dd-G} (having "maximal width") and V_{dd-B} (having "minimal width") are formed in the line forming region 33 and V_{dd-R} (having "intermediate width") and " I_{dat} [sic]" (also having "intermediate width") are formed in line forming regions 31 and 34. *Id.* at 6:5-20; *see also id.* at 6:20-23 (noting that "with the line forming region 31, only the electric power line V_{dd-R} is shown in the drawing, and with the line forming region 34, only the data line I_{dat} is shown in the drawing").



The patent's second embodiment provides line-forming regions between both pixel rows and pixel columns. *See generally* EX-1001 at 7:1-67, Fig. 4. Every other line-forming region row comprises horizontally-oriented “three electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} .” *See id.* at 7:12-29 (identifying line forming regions 41 and 43 as having these three power lines). Between those rows are line-forming regions that comprise “two scan lines V_{sel} .” *See id.* (identifying line forming region 42). Each line-forming region column comprises a vertically oriented “electric power line V_{dd} ” and “one data line I_{dat} .” *See id.* at 7:29-33; *see also*

id. at 7:33-38 (identifying red electric power line V_{dd-R} and a data line I_{dat} as disposed in line forming region 51 between red and green pixel groups), 7:38-45 (identifying green electric power line V_{dd-G} and data line as disposed between the blue and green pixel groups to the right of line forming region 51).

The vertically-oriented electric power lines electrically connect to their corresponding horizontally-oriented electric power lines through contact holes formed in an inter-layer insulating film. EX-1001 at 7:45-50. In addition to providing uniform pixel pitch, this arrangement of electric power lines in both row and column directions “in the form of a matrix” allegedly reduces “wiring resistance . . . thereby enabling sufficient current supply to the organic EL devices.” *Id.* at 7:54-61; *see also id.* at 7:61-64 (“Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, cross-talk can be reduced.”).



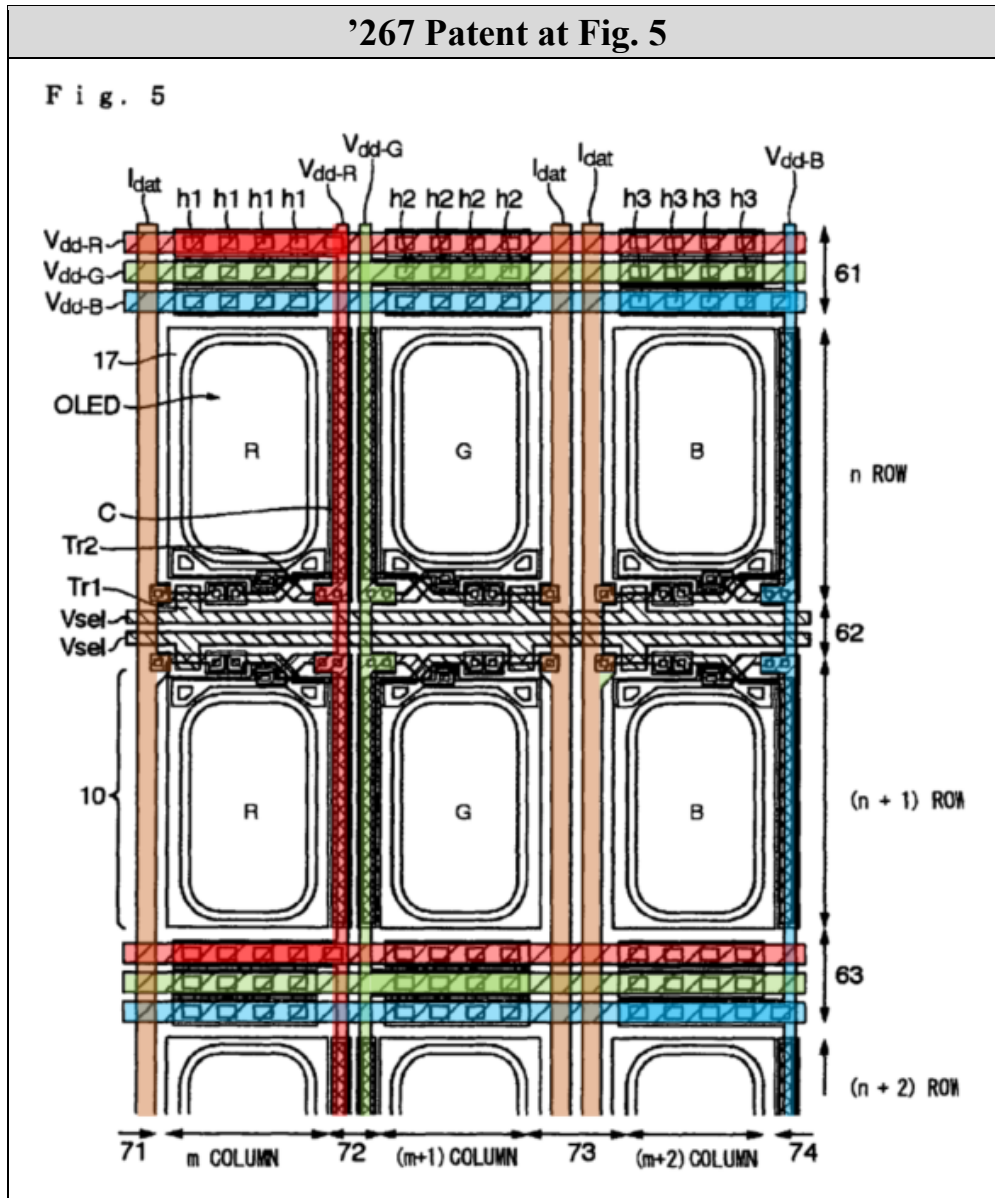
The patent's third embodiment combines the line-forming region teachings of the first and second embodiments. *See generally* EX-1001 at 8:1-9:17, Fig. 5. Like the first embodiment, the third embodiment features “three combinations of two lines selected from the three [vertically-oriented] electric power lines, V_{dd}-[G],

V_{dd-R} , and V_{dd-B} and the three data lines I_{dat} . . . formed between the pixel groups arrayed in the column direction.” *See id.* at 8:29-32. For example, I_{dat} combined with the blue electric power line V_{dd-B} ² can be formed in regions 71 and 74 (*see id.* at 8:32-37, 8:46-50), the V_{dd-G} green and V_{dd-R} red power lines may be formed in region 72 (*see id.* at 8:37-41), and two I_{dat} data lines may be formed in region 73 (*see id.* at 8:42-45).

Like the second embodiment, the third embodiment features line-forming region rows that alternate between “three [horizontally-oriented] electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} ” and “two scan lines V_{sel} .” *See id.* at 8:12-28 (identifying line forming regions 61 and 63 as having three electric power lines and line forming region 62 as having two scan lines). Also like the second embodiment, the third embodiment’s horizontally-oriented electric power lines connect to their corresponding vertically-oriented electric power lines through contact holes. *See id.* at 8:51-64.

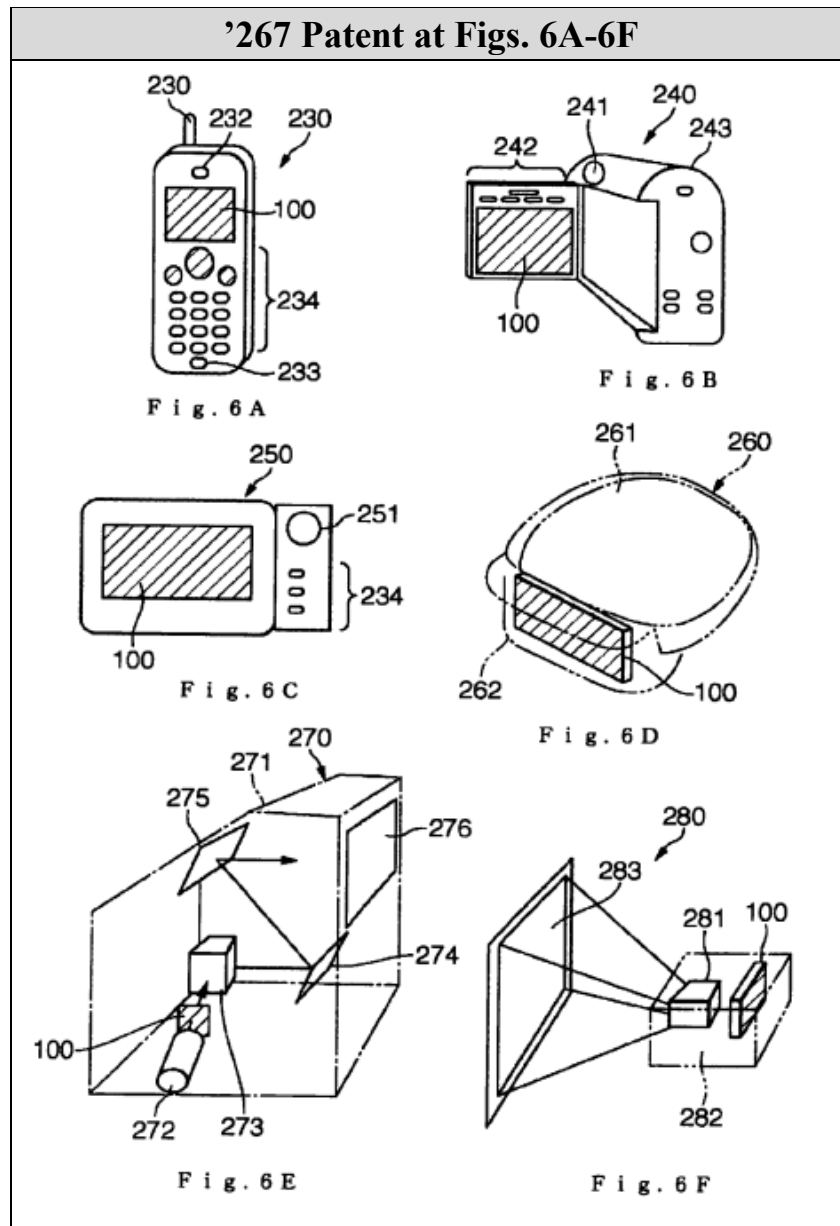
² The ’267 patent does not identify the color of the “electric power line” formed in region 71, and it identifies V_{dd-G} as the electric power line formed in region 74. However, these appear to be typographical errors as the context provided, along with figure 5, suggest that the blue electric power line would be formed in these regions. *See* EX-1006, ¶ 65.

In contrast to the previous embodiments, however, each pair of the third embodiment's horizontal and vertical electric power lines electrically connect to each other through *multiple* contact holes rather than just one, which provides "the advantage of preventing wiring breakage, and . . . the advantage of reducing wiring resistance." *See id.* at 8:60-64, Fig. 4 (identifying h1 as the series of contact holes for the red power lines, h2 as the green power line contact holes, and h3 as the blue power line contact holes).

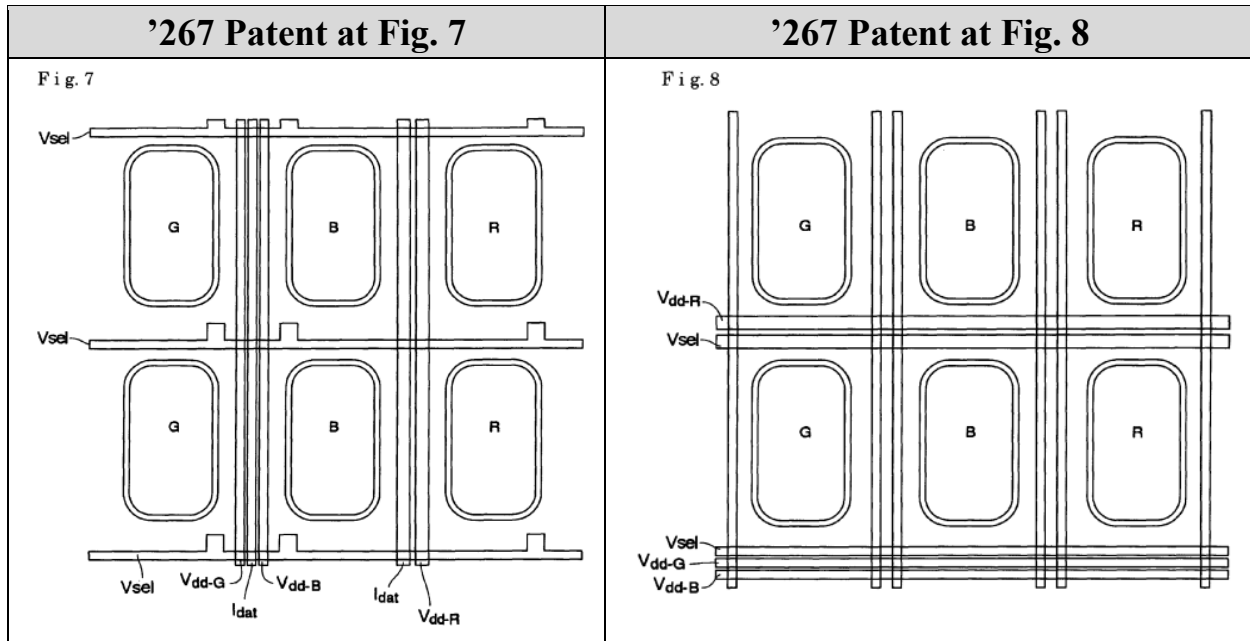


The patent's fourth embodiment provides examples of "electronic devices to which the electric-optical device according to the present invention can be applied." See generally EX-1001 at 9:20-58, Figs. 6-8. Examples of such devices include cellular phones (Fig. 6(a)), video cameras (Fig. 6(b)), portable personal computers (Fig. 6(c)), head mount displays (Fig. 6(d)), rear projectors (Fig. 6(e)), and

front projectors (Fig. 6(f)).



Finally, the patent briefly mentions two embodiments featuring line forming regions with different combinations of power lines, scan lines, and data lines. *See* EX-1001 at 9:59-10:3, Figs. 7-8.

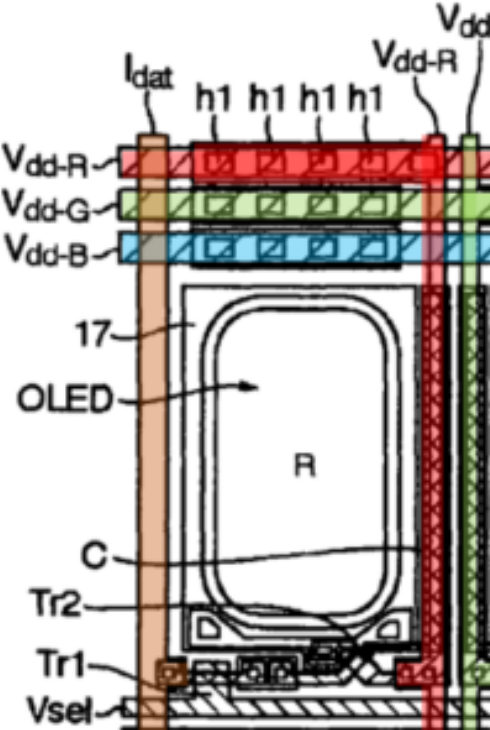


The '267 patent does not restrict that each of the power lines and contact holes must be implemented in the same substrate. To the contrary, the patent specifically distinguishes certain embodiments corresponding to an “electro-optical device” (*see id.* at 2:36-3:23) and other embodiments requiring a “matrix substrate” (*see id.* at 3:60-4:22).

B. Challenged Claim

The challenged claim is reproduced below. It does not reflect the patent’s teachings about line forming regions with approximately equal width, or about having uniform pixel pitch, or about increasing the pixel’s aperture ratios. Rather, it reflects the third embodiment’s disclosure of having power lines that electrically connect to each other through *multiple* contact holes. *See* EX-1001 at 8:60-64, Fig. 4. Although not mentioned by the patent’s specification, figure 5 depicts that the

vertically oriented power lines have a portion (known in the art as a “landing pad”) that protrudes from the main part of the power line in order to accommodate multiple contact holes that connect to the horizontally oriented power lines. EX-1006, ¶ 67. Claim 1 reflects this concept by requiring contact holes in a “second portion” of the first power line that overlaps with the second power line.

'267 Patent at Fig. 5 (Magnified to Show Exemplary Pixel)	'267 Patent Claim 1
Fig. 5 	1. An electro-optical device comprising: - a scan line; - a data line that intersects the scan line; - a first electrode; - a second electrode; - a light emission layer that is disposed between the first electrode and the second electrode; - a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction; - a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line; and - an inter-layer insulating film that is disposed between the first power line and the second power line, - the second portion of the first power line

	being electrically connected to the second power line through plurality of contact holes.
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C. Prosecution History

The '267 patent issued from U.S. application no. 12/219,592, which was filed as a continuation of U.S. application no. 10/676,067 and claims priority to Japanese application no. 2002-293696.

1. Japanese Patent Office Proceedings

The original owner of the '267 filed its foreign priority application—JP2002-293696—on October 7, 2002. *See* EX-1002; EX-1003.

2. United States Patent Office Proceedings

(a) U.S. App. No. 10/676,067

Prosecution of this application began on October 2, 2003, and in it the Applicant pursued claims essentially requiring “line forming regions” formed between pixel groups that has approximately equal width. *See* EX-1006, ¶¶ 73-90 (discussing EX-1004). The claims gradually evolved to require that the lines within these line forming regions have different widths. *See id.* Despite years of prosecution, the Patent Office never allowed these claims—issuing various indefiniteness, anticipation, and written descriptions along the way. *See id.* On May 1, 2009, the application went abandoned for failure to timely respond to an office action. *See id.*

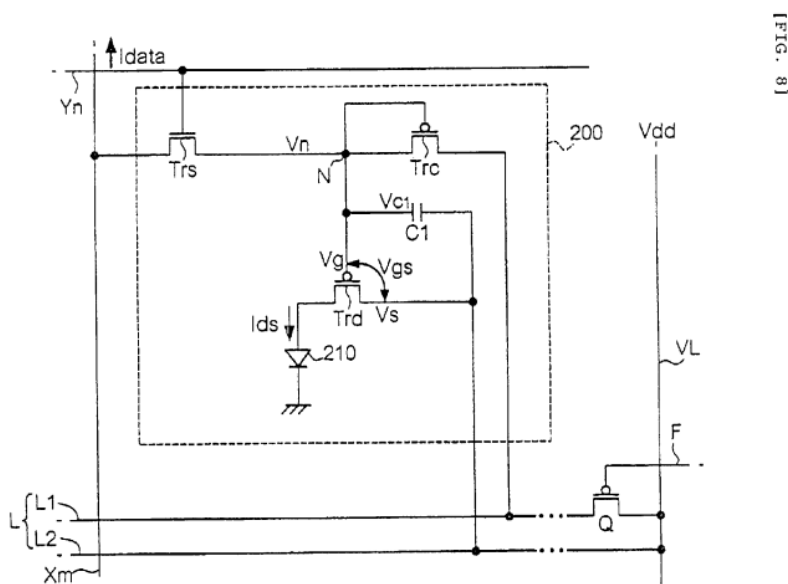
The references in the grounds of this petition were not considered during prosecution history. Instead, the examiner considered and cited U.S. 6,825,820 to Yamazaki; U.S. 2003/0076046 to Komiya; U.S. 6,633,135 to Nara; and U.S. 2001/0048106 to Tanada. *See id.*

The “Yamazaki” reference considered in the prosecution of the ’067 application (i.e., U.S. 6,825,820) is significantly different from the “Yamazaki” reference being relied upon in ground 1 of this petition (i.e., 6,894,431). Despite sharing a common inventor, the Yamazaki 820 reference does not contain various teachings found in the Yamazaki 431 reference, including, for example, Yamazaki 431’s figure 3A (discussed in detail below) and related specification disclosure. EX-1006, ¶¶ 76.

(b) U.S. App. No. 12/219,592

Prosecution of the ’592 application began July 24, 2008. *See* EX-1006, ¶¶ 91-98 (discussing EX-1005). Unlike its parent application, the ’592 application did not recite limitations regarding the widths of power lines or line forming regions. *See id.* Instead, it originally claimed first and second “power lines” that were electrically connected to one another via a “plurality of contact holes.” *See id.*

In the first office action, the Examiner rejected all claims as anticipated by U.S. 6,858,991 to Miyazawa. *See* EX-1005 at 74-80. The Applicant subsequently



Shortly thereafter, an interview was held in which the Applicant discussed a new proposed claim 9, which would recite the second power line overlapping at least the second portion of the first power line. EX-1005 at 109, 113-115. In this interview the “*examiner pointed out that [Miyazawa] apparently disclosed . . . all the features as claimed including the proposed amended portion ‘the plurality of contact holes disposed corresponding to an intersection of the first power line and the second power line and disposed in the pixel.’*” *Id.* at 115 (emphasis added).

However, the examiner allegedly further observed “no description of the second power line overlapping at least the second portion of the first power line’ as recited in the newly added proposed claim 9.” *Id.* *The Applicant’s representative “fully agreed with the examiner’s analysis.” Id.* (emphasis added). This indicates that the alleged point of novelty over the Miyazawa reference was not the existence of multiple power lines or multiple contact holes connecting those power lines.

The Applicant subsequently cancelled all pending claims and added the proposed claim 9. EX-1005 at 105-111 (July 5, 2011 Amendment). The claims were then allowed. *See* EX-1005 at 116-124. Original claim 1 and allowed claim 9 are reproduced below with significant differences bolded.

Claim 1 (as originally filed July 24, 2008)	Claim 9 (after July 5, 2011 Amendment) (corresponds to issued claim 1)
1. An electro-optical device comprising: a scan line extending in a direction; a data line extending in a direction that intersects the scan line; a pixel located corresponding to the intersection of the scan line and the data line, the pixel including a light emission layer between a first electrode and a second electrode: a first power line extending in the direction in which the scan line extends;	9. (New) An electro-optical device comprising: a scan line; a data line that intersects the scan line; a pixel disposed corresponding to an intersection of the scan line and the data line, the pixel including a light emission layer between a first electrode and a second electrode; a first power line having a first portion extending in a first direction and

a second power line extending in the direction in which the data line extends; an inter-layer insulating film between the first power line and the second power line; and a plurality of contact holes extending through the inter-layer insulating film, the contact holes electrically connecting the first power line and the second power line to each other.	a second portion extending in a second direction that intersects the first direction; a second power line extending in the second direction, the second power line overlapping at least the second portion of the first power line; an inter-layer insulating film being disposed between the first power line and the second power line; and a plurality of contact holes electrically connecting the second portion of the first power line and the second power line to each other.
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The Applicant then amended the claims after allowance, to clarify the “light emission layer” limitation. EX-1005 at 147-151. The claims then were re-allowed and issued. *Id.* at 163-178.

III. THE CHALLENGED CLAIM IS UNPATENTABLE

A. Yamazaki (Ground 1 – Claim 1)

1. Overview of Yamazaki³

U.S. Published App. No. 2001/0015618 (“Yamazaki”) is a U.S. published

³ General descriptions provided for the references and combinations thereof are incorporated into each subsection and mapping of the claims that includes citations to these references.

patent application that was filed December 7, 2000 and published August 23, 2001.

See EX-1008. Yamazaki thus qualifies as prior art under pre-AIA 102(b). *Id.*

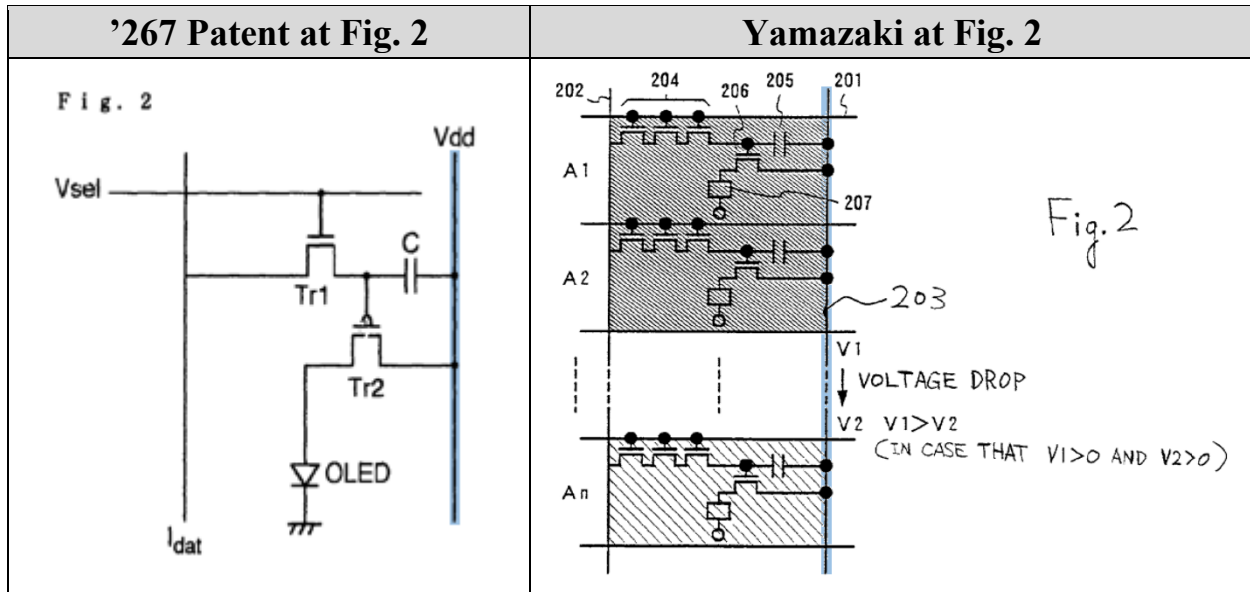
Yamazaki relates to an electroluminescence display and addresses the same problem recognized by the '267 patent—ensuring that pixels receive adequate electrical power. EX-1008; *see also* EX-1001 at 7:61-64 (discussing suppression of “non-uniformity of luminance due to insufficient current supply”), *id.* at 9:11-14. Yamazaki teaches that EL display devices may be vulnerable to a “voltage drop” phenomenon in that “the voltage becomes lower as its distance from a power source becomes farther even if it is the voltage of the same wiring.” EX-1008 at [0005]. Because “wiring resistance” causes voltage drop, “[t]his problem is particularly conspicuous when the wiring becomes long.” *Id.* at [0005]. Voltage drop affects the fundamental lines found in conventional electroluminescent displays, including the “voltage of the current supply line,”⁴ which corresponds to the “power line” disclosed by the '267 patent and “to the gate wiring 201 and the

⁴ Yamazaki’s paragraph [0007] identifies the current supply line as “203” while paragraph [0008] identifies the current supply line as “205.” The issued version of Yamazaki, however, corrected this inconsistency by identifying the current supply line as “203” in its corresponding passages. *See* EX-1009 U.S. Pat. No. 6,894,431 at 1:51-2:21.

source wiring 202.” *See id.* at [0008], [0010]. Voltage drop across current supply lines causes pixel brightness to drop as voltage drops. *See id.* at [0008]-[0009]; *see also id.* at [0013] (referencing “considerable loss of the homogeneity of the quality of the image”). Voltage drop across gate and source wiring causes pixel control to drop as voltage drops. *See id.* at [0009]-[0010]; *see also id.* at [0013] (referencing “extreme decline in the operating speed” and “the delay of a signal”), [0047].

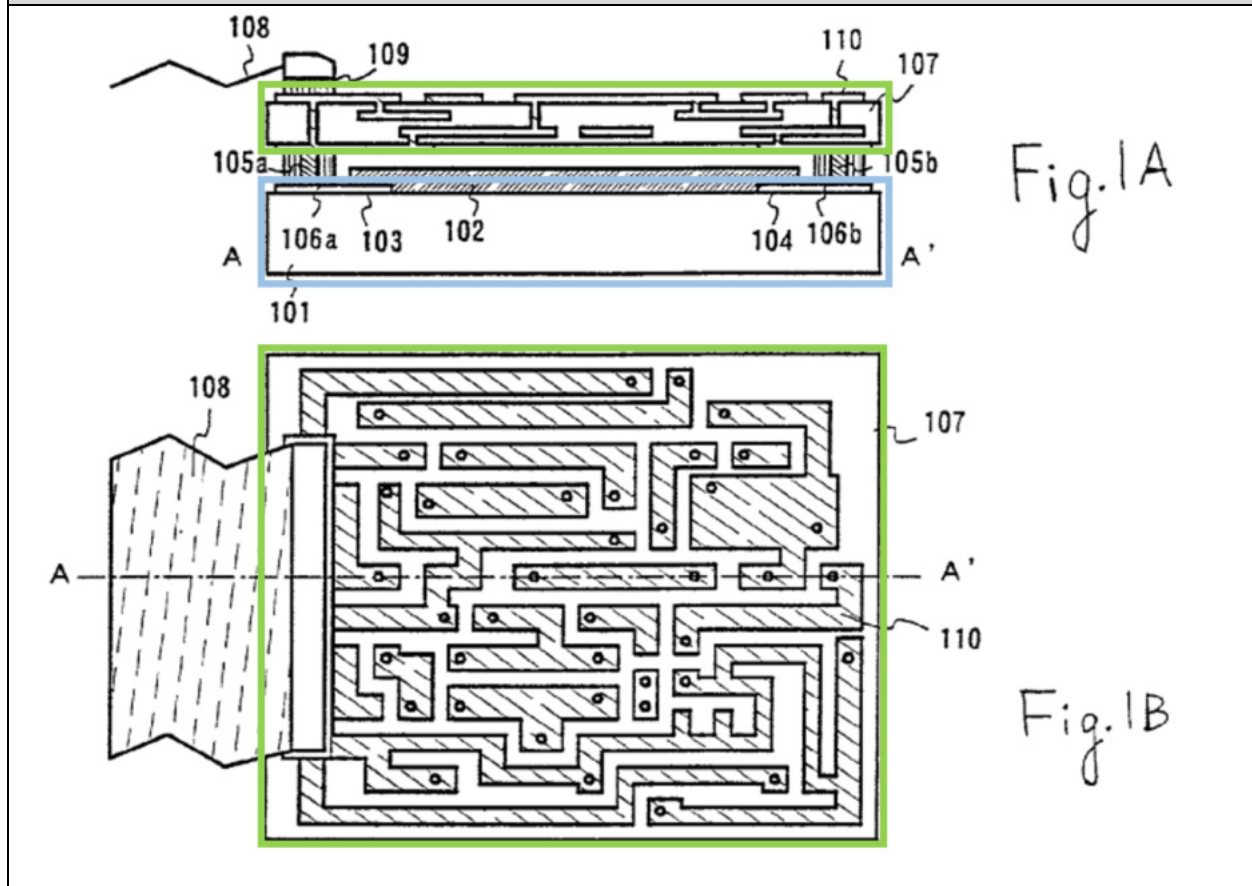
Yamazaki’s figure 2 shows the basic components of an electroluminescent display, including “gate wiring 201, the source wiring 202, and the current supply line 203,” which corresponds to the ’267 patent’s “scan line Vsel,” “data line Idat,” and “power line Vdd,” respectively.⁵ *See* EX-1006, ¶¶ 102-106; EX-1008 at [0007]; EX-1001 at 5:15-25. Figure 2 of both the ’267 patent and Yamazaki, highlighted below, show the power line in pale blue.

⁵ The issued version of Yamazaki labels this figure 2, in substantially the same form, as “prior art.” *See* EX-1009 (U.S. Pat. No. 6,894,431) at Fig. 2.



To alleviate the voltage drop problem, Yamazaki provides printed wiring board(s) (“PWB”) with additional wiring that electrically connects to a “substrate having a luminous element” in order to reduce the wiring resistance faced by signals that reach pixels. *See* EX-1008 at [0014]-[0015], [0017]-[0023] (referencing “substrate [101] having a luminous element 102” and “printed wiring board 107”). “[B]ecause the PWB side wiring 110 is made of an extremely low resistant wiring, the voltage drop which originates in the wiring resistance can be immensely suppressed, thereby making it possible to transmit nearly equivalent electric signals to the element side wirings 103 and 104.” *Id.* at [0023]. Figures 1A and 1B, reproduced below, identify in green the printed wiring board (107) and its additional wiring (110) and identify in pale blue the substrate (101) with an exemplary luminous element (102) and wiring (103 and 104). *See id.* at [0018], [0022].

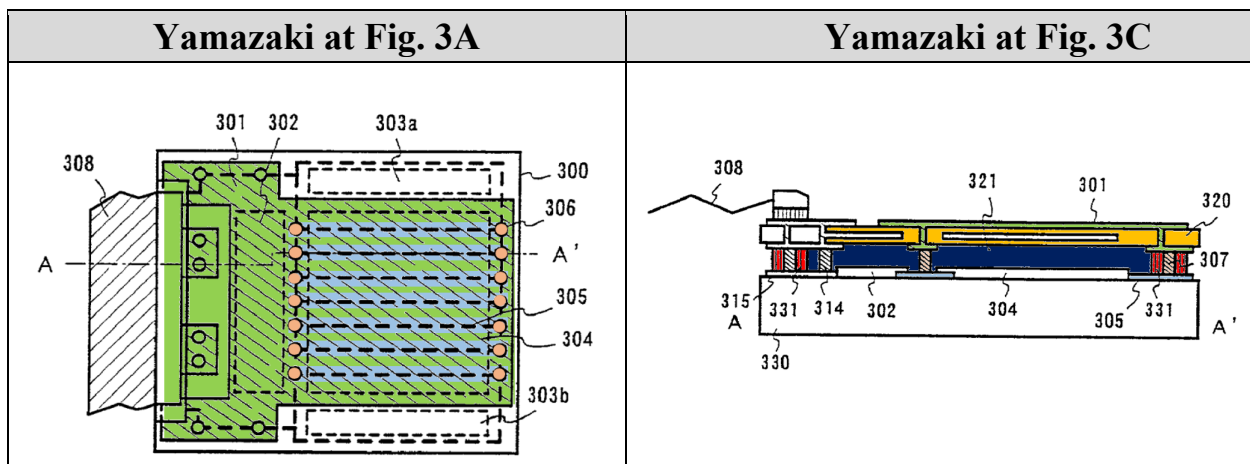
Yamazaki at Figs. 1A and 1B



This approach can reduce the current supply line's resistance, as explained by Yamazaki's discussion of an "Embodiment Mode of the present invention," which explains how to implement Yamazaki's ideas in a more concrete example. See EX-1006 ¶ 105; EX-1008 at [0035]-[0047]. Specifically, the printed wiring board can include a "wiring 301 for aiding a current supply line (hereinafter referred to as current supply auxiliary line)." See EX-1008 at [0037], Fig. 3A. The "current supply auxiliary line" (301) connects in parallel to the "current supply line" (305) through "contact portion" (306) "in order to reduce the apparent wiring resistance of the current supply line." *Id.*; see also *id.* at [0039] ("[T]herefore, the

voltage drop of the current supply line 305 can be substantially suppressed.”),

[0047]. As shown in Figure 3A’s “top view,” the contact portion (306) comprises multiple contact holes (shown in pale red) that electrically connect the substrate’s current supply lines (305) (shown in blue) to current supply auxiliary line (301) on the printed wiring board (shown in green). *Id.* at [0036]-[0039]. As shown in Figure 3C’s “cross-sectional view,” in the contact portions (306) the current supply auxiliary line (301) (shown in green) electrically connects to current supply line (305) (shown in blue) through a conductor 307 (shown in pale red). *Id.* “[A]n inert gas . . . or resin” (shown in dark blue) may be filled in the airtight space (321) between the printed wiring board (320) and the element-formed substrate (330). *Id.* at [0044]-[0045].



Following the “Embodiment Mode,” Yamazaki describes seven embodiments that each reflect additional aspects of the invention. *See id.* at [0048]-[0059], Figs. 4A-4B (describing Embodiment 1); *id.* at [0060]-[0072], Figs. 5A-5B

(describing Embodiment 2); *id.* at [0073]-[0079], Fig. 6 (describing Embodiment 3, which is a modified version of Embodiment 1); *id.* at [0080]-[0085], Fig. 7 (describing Embodiment 4, which is a modified version of Embodiment 1); *id.* at [0086]-[0087] (describing Embodiment 5, which indicates that the foregoing embodiments can be applied to “Electro Chromic” and “field emission” displays); *id.* at [0088]-[0102] (describing Embodiment 6, which indicates that the foregoing embodiments “may be employed in . . . electronic equipment” like video cameras and mobile computers); *id.* at [0103]-[0110] (describing Embodiment 7, which indicates that Embodiment 6’s electric equipment can be suitable for outdoor use). Moreover, these embodiments show cross sectional views that show in further detail the structure of the substrate and its circuitry shown in figure 3C. *See* EX-1006, ¶ 109. A POSITA would also have recognized that these seven embodiments reflect additional detail about the Embodiment Mode and, additionally, would have been obvious to combine with Embodiment Mode. *See id.*

2. Claim 1

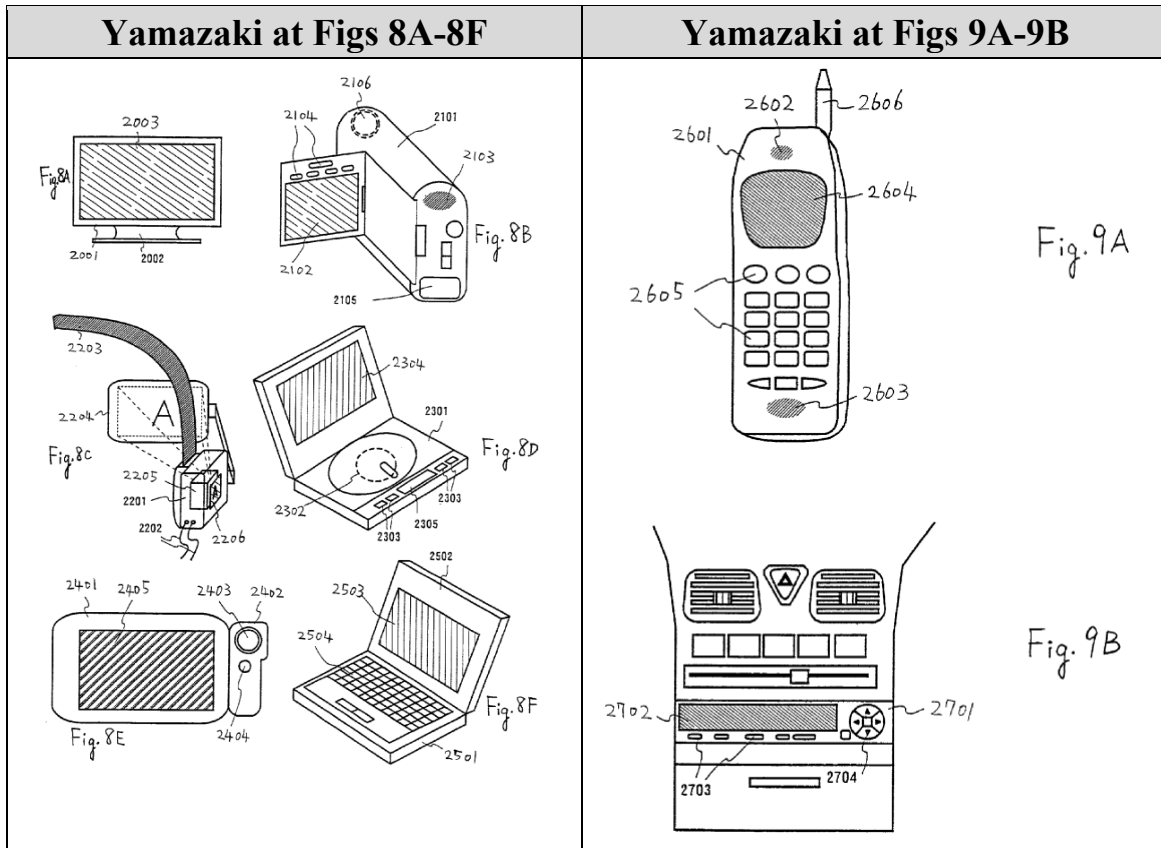
(a) 1[a] An electro-optical device comprising:

Yamazaki discloses “an electro-optical device” or renders this limitation obvious.

The ’267 patent describes an “electro-optical device” as “a general electronic device for changing the optical state of light by using electric effects,” which

includes, “besides self-light-emitting devices such as electro-luminescence devices, electronic devices for displaying grayscale by adjusting the state of the polarized light, similarly to liquid crystal devices.” EX-1001 at 2:26-31. “The electronic apparatus is not particularly restricted so long as it includes a display device, and can be applied to, for example, cellular phones, video cameras, personal computers, head mount displays, projectors, facsimiles, digital cameras, portable TVs, DSP devices, PDAs, palmtops, and the like.” *Id.* at 3:54-59; *see also id.* 9:19-65 (describing “Fourth Embodiment,” which corresponds to “examples of electronic apparatuses to which the electr[o]-optical device according to the present invention can be applied”), at Figs. 6A-6F.

Yamazaki discloses that the “light-emitting device formed by implementing the present invention” can be implemented in “various electronic equipment.” *See* EX-1008 at [0089]-[0102], Figs. 8A-8F, 9A-9B; *see also id.* at [102] (referencing that “any constitution of the light emitting device shown in Embodiments 1 to 6 may be employed in the electronic equipment of this embodiment”). An example of such electronic equipment includes a “display incorporating a light-emitting device in its casing.” *See id.* at [0090]. These examples of electronic equipment constitute “electro-optical devices.”

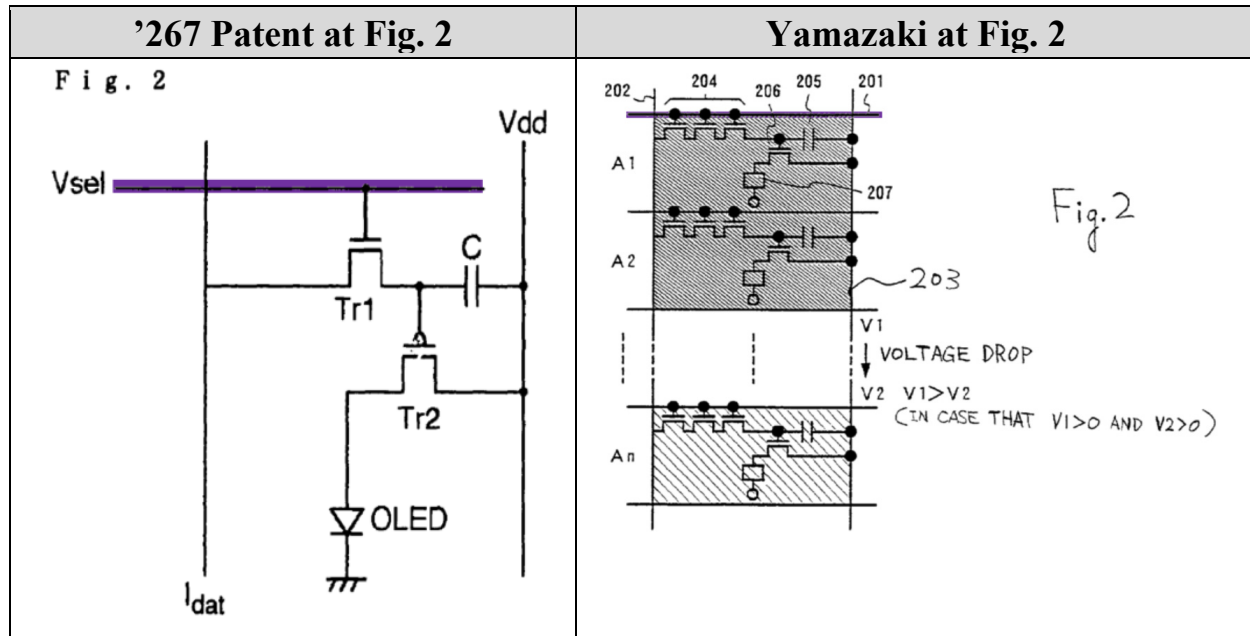


For these reasons, Yamazaki discloses and renders obvious an electro-optical device. EX-1006, ¶ 101.

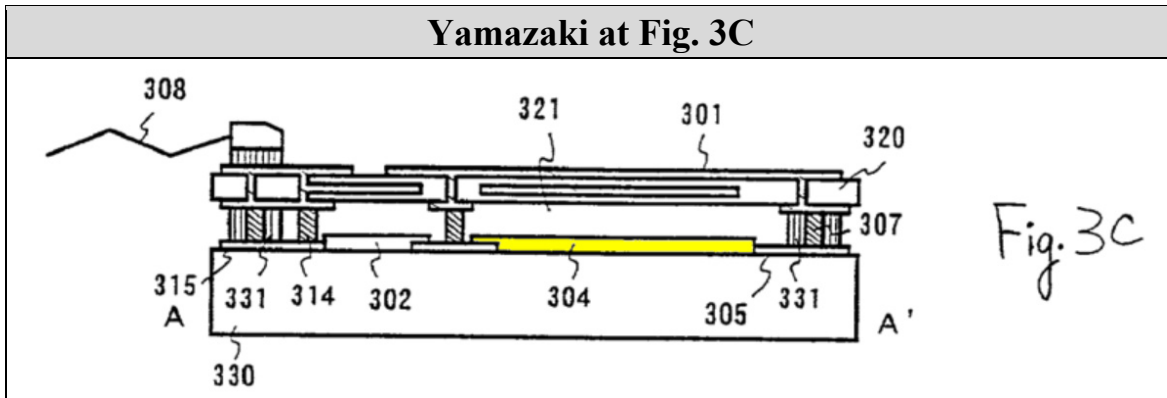
(b) 1[b] a scan line;

Yamazaki discloses a “scan line” or renders this limitation obvious. As background, Yamazaki describes the “pixel portion” of an “active matrix EL display device” in figure 2. *See* EX-1008 at [0007]. In this figure, “[r]eference symbol 201 denotes a gate wiring.” *See id.*; *see also id.* at [0010]. Yamazaki’s “gate wiring” 201 constitutes a scan line because it controls the gates of the “switching

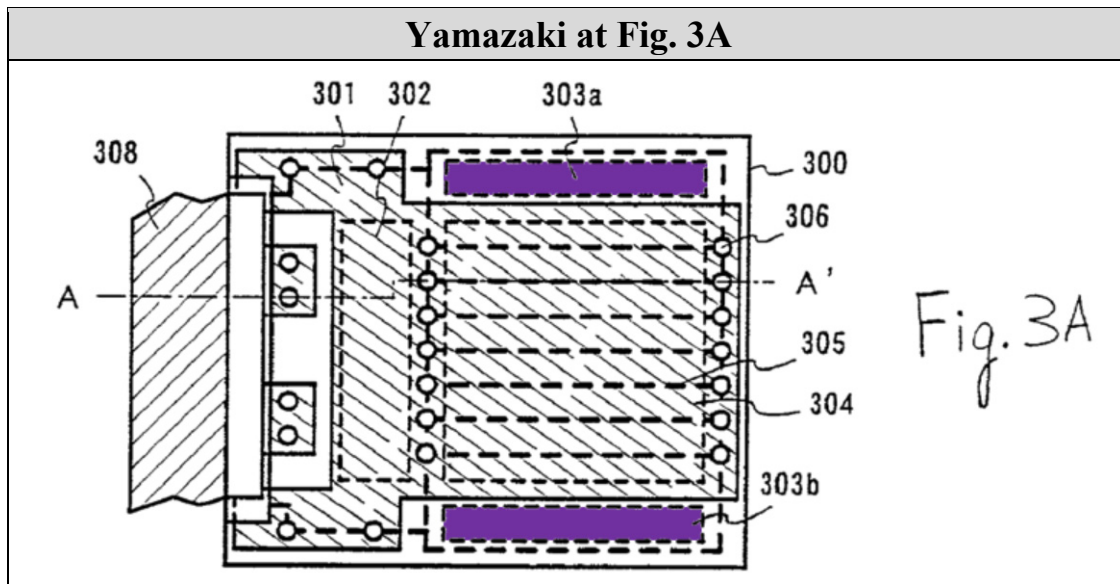
TFT 204.” *See id.*; *see also* EX-1001 at 5:6-31 (describing the “switching transistor Tr1” as comprising a “gate terminal . . . connected to the scan line V_{sel} ”). In the table below, figure 2 of the ’267 patent and figure 2 of Yamazaki highlight in purple their respective scan lines.



Yamazaki’s “Embodiment Mode” as illustrated for example by Figures 3A and 3C, included a “scan line.” This “Embodiment Mode” is an “EL display device” that includes “pixel portion 304.” EX-1008 at [0035], [0038]. As discussed above, Yamazaki discloses that the pixel portion of an EL display device includes scan lines. *See id.* at [0007]-[0010].



Moreover, Figure 3A illustrates that this “EL display device” includes “gate driver circuits” denoted by “reference symbols 303 a and 303 b.” *Id.* at [0038]. Gate driver circuits generate gate-controlling signals carried by gate wiring, which as discussed above, constitute scan lines. *See id.* at [0010]-[0012], [0040]-[0041]. Figure 3A, reproduced below, highlights the gate driver circuits, which connect to scan lines, in purple.

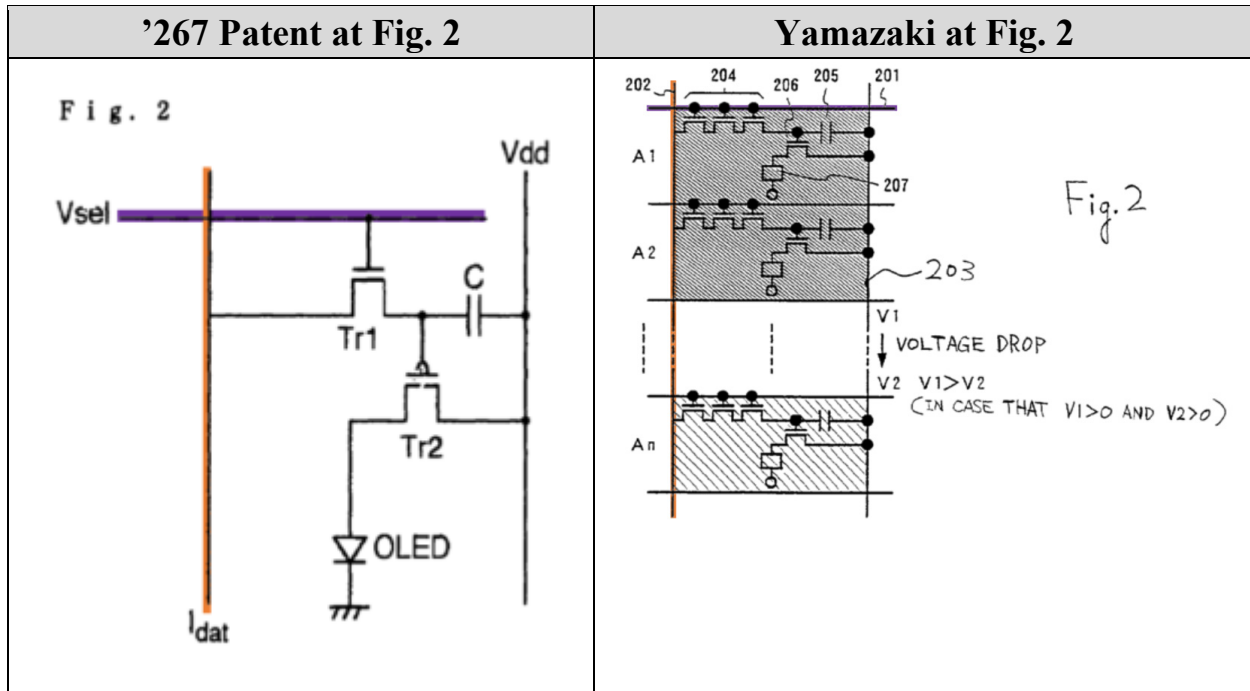


For these reasons, Yamazaki discloses and renders obvious a scan line. EX-

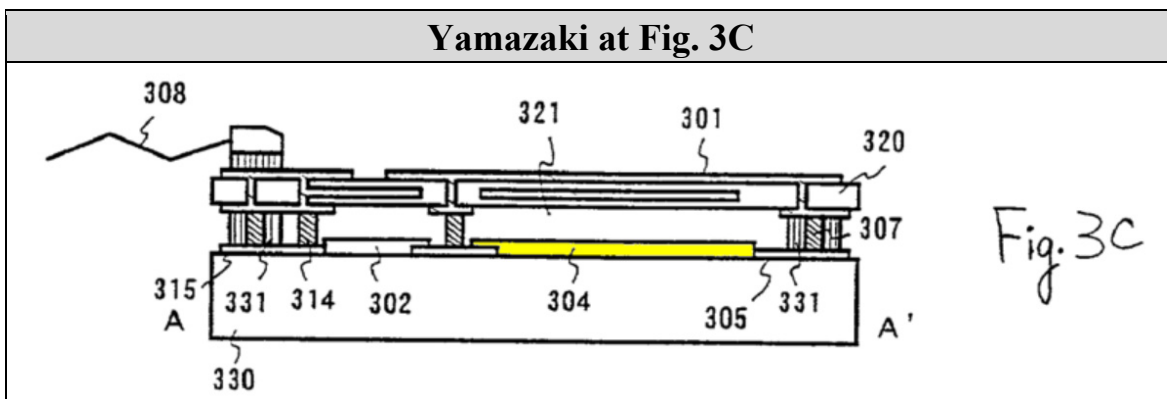
1006, ¶¶ 104-106.

(c) 1[c] a data line that intersects the scan line;

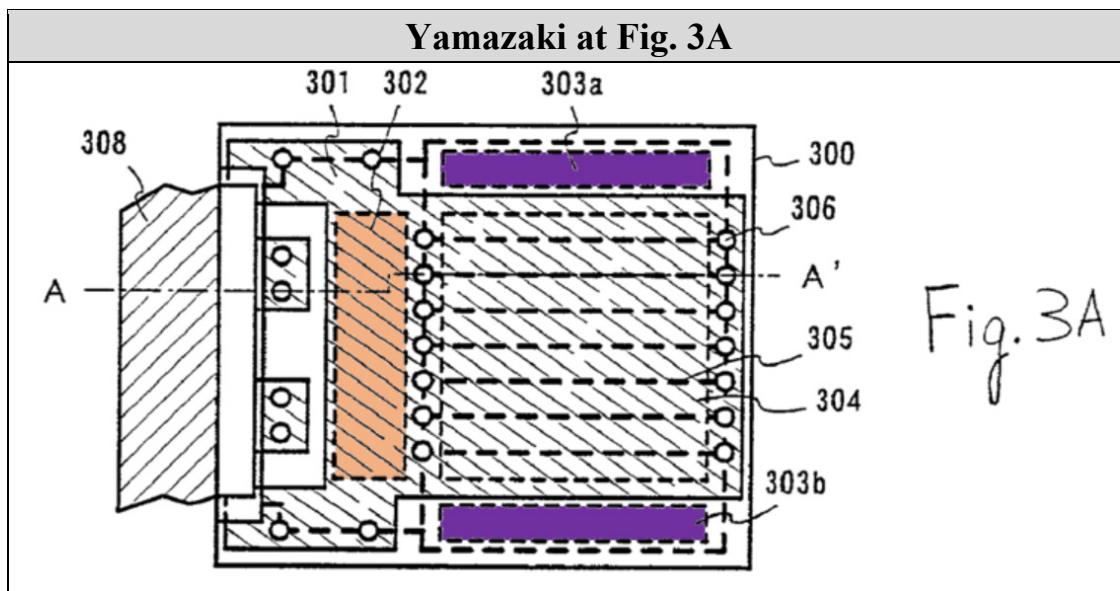
Yamazaki discloses “a data line that intersects the scan line” or renders this limitation obvious. As background, Yamazaki describes “pixel portion” of an “active matrix EL display device” in figure 2. *See* EX-1008 at [0007]. In this figure, reference symbol “202 denotes a source wiring.” *See id.*; *see also id.* at [0010]. Yamazaki’s “source wiring” 202 constitutes a data line because it applies a “desired voltage to a gate of the current control TFT 206,” which in turn provides voltage to the electroluminescent element 207. *See id.* at [0010]; *see also id.* at [0007]; EX-1001 at 5:21-31 (“[U]pon outputting a selection signal to the scan line V_{sel} , and opening the transistor Tr1, the data signals supplied through the data line I_{dat} are written to the holding capacitance C as a voltage value. Subsequently, the holding voltage written to the holding capacitance C is held during one frame period, and the conductance of the driving transistor Tr2 is determined according to the holding voltage in an analog manner, whereby forward bias current corresponding to light-emission level is supplied to the light-emission portion OLED.”). In the table below, figure 2 of the ’267 patent and figure 2 of Yamazaki highlight in brown their respective data lines, which intersect scan lines (highlighted in purple).



Yamazaki's "Embodiment Mode," as illustrated for example by Figures 3A and 3C, included a "data line." This "Embodiment Mode" is an "EL display device" that includes "pixel portion 304." EX-1008 at [0035], [0038]. As discussed above, Yamazaki discloses that the pixel portion of an EL display device includes data lines that intersect scan lines. *See id.* at [0007]-[0010].



Moreover, Figure 3A illustrates that this “EL display device” includes a “source driver circuit” denoted by “reference symbols 302.” *Id.* at [0038]. Source driver circuits generate signals carried by source wiring, which as discussed above, constitute data lines. *See id.* at [0010]-[0012], [0038]-[0039]. Figure 3A, reproduced below, highlights the source driver circuit, which connect to data lines, in brown.



The data lines of Yamazaki’s “Embodiment Mode” intersect scan lines. As discussed and shown above, an active matrix EL display device features scan lines and data lines that intersect for each pixel. Because Yamazaki’s Embodiment Mode is an active matrix display device, it has data lines that intersect scan lines. EX-1008.

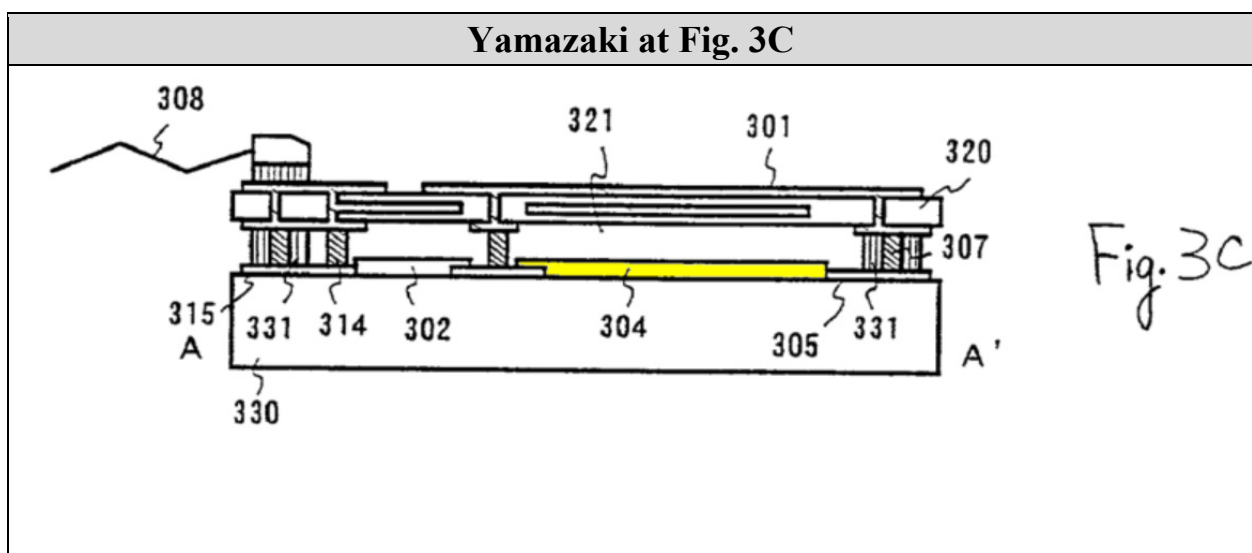
For these reasons, Yamazaki discloses and renders obvious a data line that

intersects the scan line. EX-1006 ¶¶ 104-106.

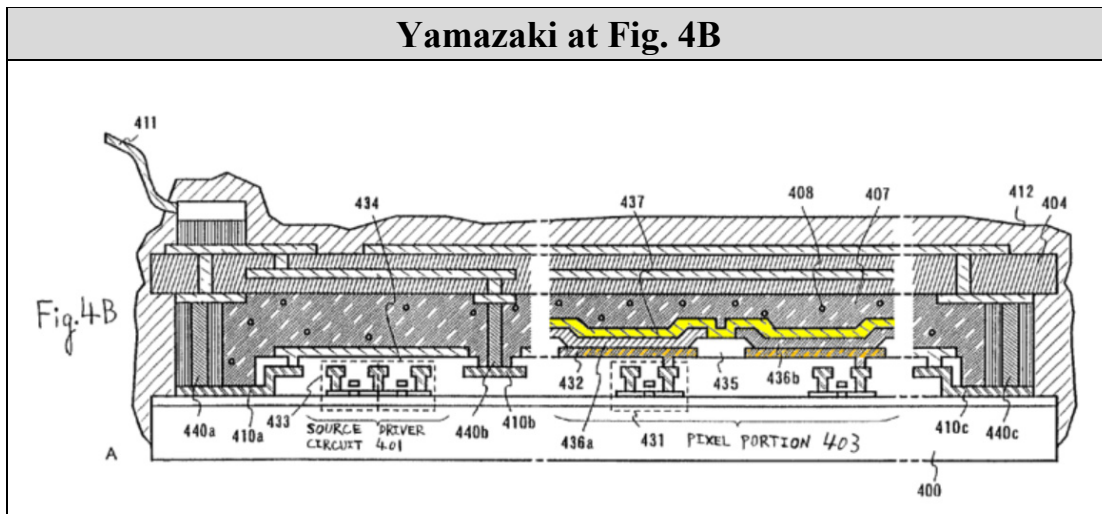
(d) 1[d] a first electrode; a second electrode;

Yamazaki discloses “a first electrode [and] a second electrode” or renders this limitation obvious. Yamazaki relates to “a device having an element (hereinafter referred to as luminous element) that is comprised of a luminous material sandwiched between *electrodes*.” EX-1008 at [0002]. Specifically, Yamazaki discloses that an electroluminescent element consists of two electrodes: an anode and a cathode. *See id.* at [0005]. These electrodes constitutes the first and the second electrode claimed by the '267 patent.

Yamazaki's “Embodiment Mode” includes a “pixel portion” denoted by “reference symbol 304,” which contain “EL elements.” *Id.* at [0037]-[0038]. EL elements, as discussed above, contain two electrodes. Figure 3C, reproduced below, shows a pixel portion highlighted in yellow.



Yamazaki illustrates its first and second electrodes with respect to Embodiment 1, which provides more details about how to implement the EL elements of “Embodiment Mode.” *See* EX-1008 at [0053]-[0055] (referencing cross sectional view shown in figure 4B that shows “pixel electrode 432” and “cathode 437”); EX-1006, ¶ 109. Figure 4B is reproduced below and highlighted to identify the “pixel electrode 432” in orange and the “cathode 437” in yellow.



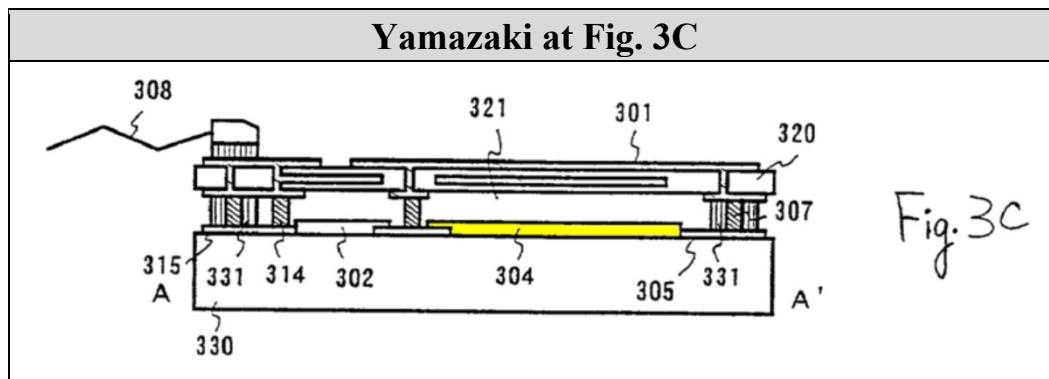
Yamazaki also illustrates its first and second electrodes with respect to other embodiments that provide additional detail about the EL elements of “Embodiment Mode.” *See* EX-1008 at [0061]-[0066], Fig. 5B (referencing cross sectional view “anode 502” and “cathode 506” of Embodiment 2); *id.* at [0073]-[0075], Fig. 6 (referencing Embodiment 3 that shows a “modified example of the structure of the EL display device described in Embodiment 1” and includes “cathode 437”); *id.* at [0082], Fig. 7 (referencing Embodiment 4 that shows “pixel electrode (cathode)

701” and “anode 702”). For these reasons, Yamazaki discloses and renders obvious a first electrode and a second electrode. EX-1006, ¶¶ 109-110.

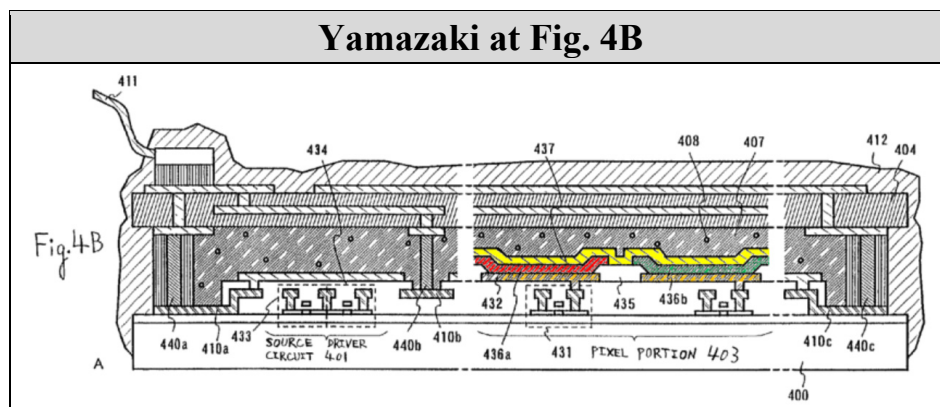
- (e) 1[e] a light emission layer that is disposed between the first electrode and the second electrode;

Yamazaki discloses “a light emission layer that is disposed between the first electrode and the second electrode” or renders this limitation obvious. Yamazaki relates to “a device having an element (hereinafter referred to as luminous element) that is comprised of a *luminous material sandwiched between electrodes*.” EX-1008 at [0002]. The luminous material gives the element “light-emitting ability” and thus constitutes the “light emission layer” claimed by the ’267 patent. *See id.* at [0004].

Yamazaki’s “Embodiment Mode” includes a “pixel portion” denoted by “reference symbol 304,” which contain “EL elements.” *Id.* at [0037]-[0038]. EL elements, as discussed above, contain a light emission layer disposed between the first and second electrodes. Figure 3C, reproduced below, shows a pixel portion highlighted in yellow.



Yamazaki illustrates its first and second electrodes with respect to Embodiment 1, which provides more details about how to implement the EL elements of “Embodiment Mode.” *See Id.* at [0052]-[0054] (referencing cross sectional view shown in figure 4B that shows red “light-emitting layer 436a” and green “light-emitting layer 436b”); EX-1006, ¶ 109. Figure 4B is reproduced below and highlighted to identify the red “light-emitting layer 436a” in red and the green “light-emitting layer 436b” in green.



Yamazaki also illustrates its first and second electrodes with respect to other embodiments that provide additional detail about the EL elements of “Embodiment Mode.” *See* EX-1008 at [0060]-[0065], Fig. 5B (referencing cross sectional view of Embodiment 2 shown in figure 5B that shows “light-emitting layer 505”); *id.* at [0073]-[0079], Fig. 6 (referencing cross sectional view of Embodiment 3 shown in figure 6 that shows a “modified example of the structure of the EL display device

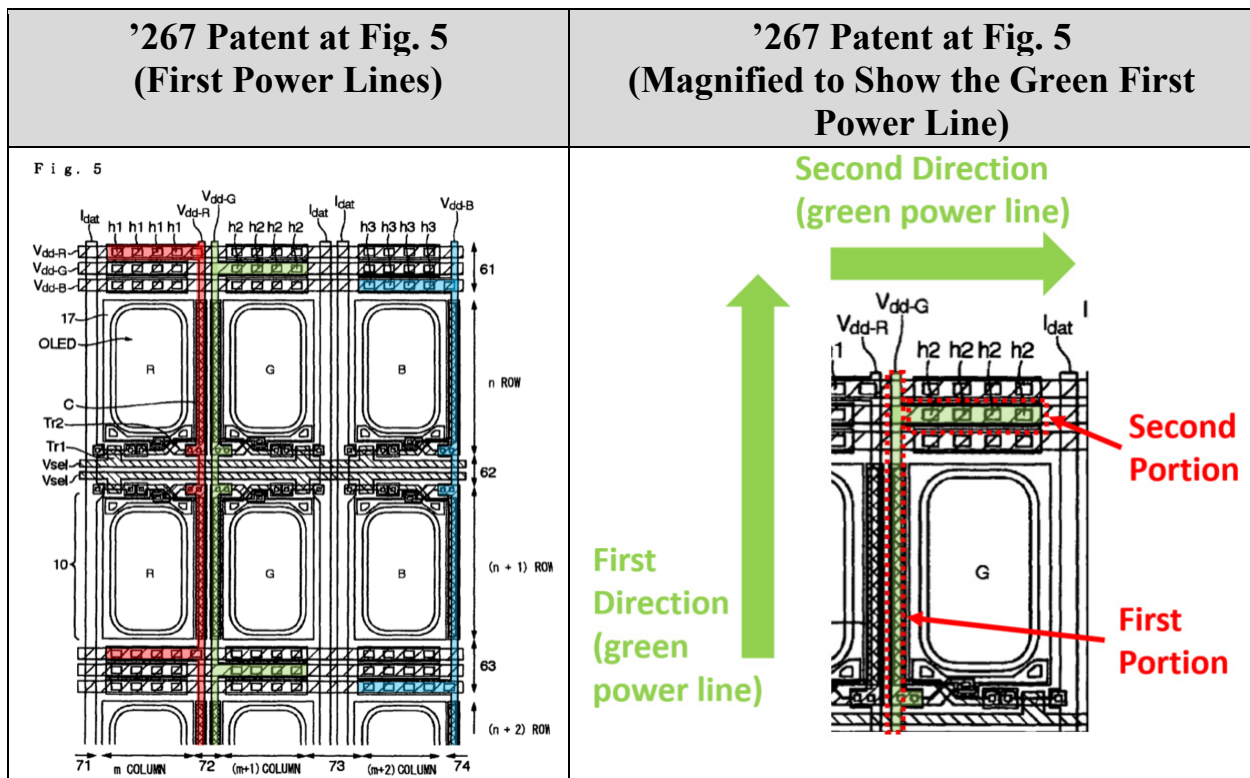
described in Embodiment 1”); *id.* at [0080]-[0085], Fig. 7 (referencing figure 7 that shows “a modified example of the structure of the EL display device described in Embodiment 1”). For these reasons, Yamazaki discloses and renders obvious a light emission layer that is disposed between the first electrode and the second electrode. EX-1006, ¶¶ 109-110.

- (f) 1[f] a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction;

Yamazaki discloses “a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction” or renders this limitation obvious.

A “power line,” in the context of the ’267 patent, supplies current and voltage to light-emitting elements. *See* EX-1001 at 1:63-2:2 (explaining that “the need to increase the electric current supplied to the organic EL device” leads to “the need to form the electric power line with a greater width”); *id.* at 7:51-61 (explaining that disposing “electric power lines . . . in the form of a matrix” enables “sufficient current supply to the organic EL devices”); *id.* at 9:4-11; *id.* at 2:36-4:9 (describing “electric power lines as “supplying driving voltage to the electro-optical devices”); EX-1006, ¶¶ 46-50 (explaining that voltage and current can be proportional to one another). The ’267 patent labels the power line by “V_{dd},” which is a well-known symbol in the industry for supplying power to an integrated circuit.

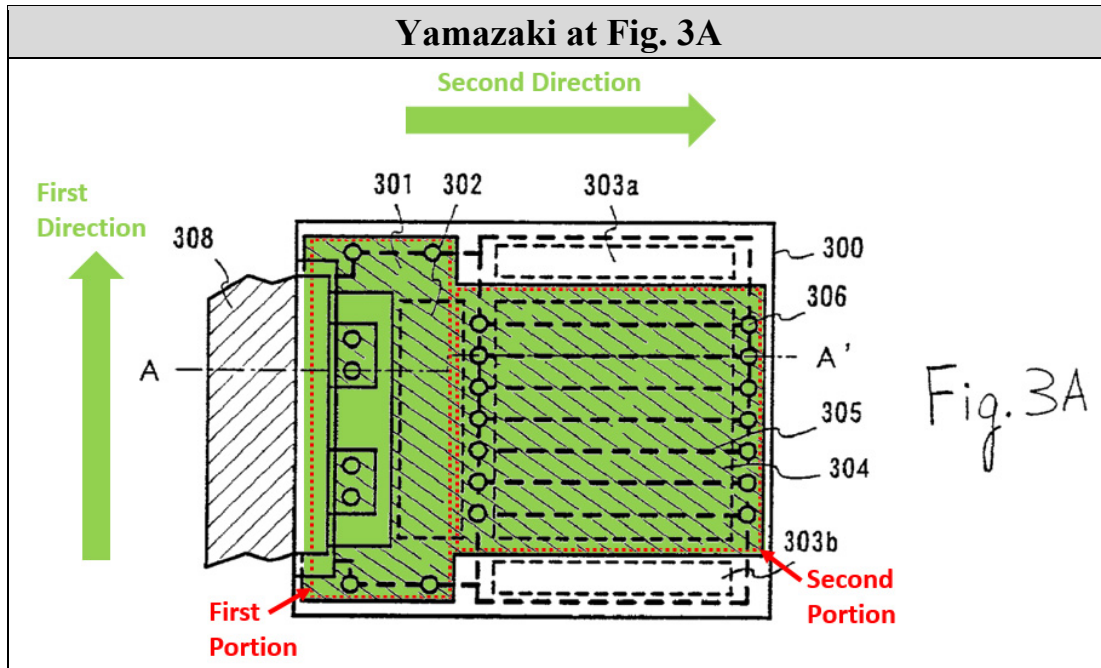
See id., ¶ 112. The V_{dd} power lines enable current to be supplied to the light-emitting elements. *See* EX-1001 at 7:56-61 (claiming that matrix arrangement allows “resistance of the electric power lines [to] be reduced”), 9:5-11. The ’267 patent’s figure 5, reproduced in the table below, illustrates three types of power lines corresponding to three colors (V_{dd-R} , V_{dd-G} , V_{dd-B}), each of which have a portion that extends in a first direction and a portion that extends in a second direction. That figure, reproduced below, shows these “first” power lines in red, green, and blue. Next to it is a magnified version of the figure that identifies exemplary first and second directions and first and second portions of the green “first power line.”



Yamazaki discloses a “first power line.” “In FIG. 3A, reference symbol 300

denotes a first printed wiring board, and a wiring 301 for aiding a current supply line (hereinafter referred to as current supply auxiliary line) is formed thereon.” EX-1008 at [0037]. Like the ’267 patent’s power lines, Yamazaki’s current supply auxiliary lines supply current. *See id.* at [0037] (“[T]he current supply line is a wiring for supplying a current, which flows to an EL element, to each EL element.”); *see also id.* at [0038] (“[T]he current supply auxiliary line 301 is electrically connected . . . to the current supply line 305 via the conductor 307.”); *id.* at [0039] (“Thus, the current supply auxiliary line 301 that is made of a low resistant material such as a copper foil is formed on the first printed wiring board 300.”).

The “current supply auxiliary line” 302 constitutes a “first power line” that includes a “first portion” and “second portion” as recited by the challenged claim. As shown in figure 3A, reproduced and annotated below, this line has a portion that extends in a first direction (in the vertical direction) and a portion that extends in a second direction (in the horizontal direction) that intersects the first direction.



For these reasons, Yamazaki discloses and renders obvious a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction. EX-1006, ¶¶ 111-117.

- (g) 1[g] a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line; and

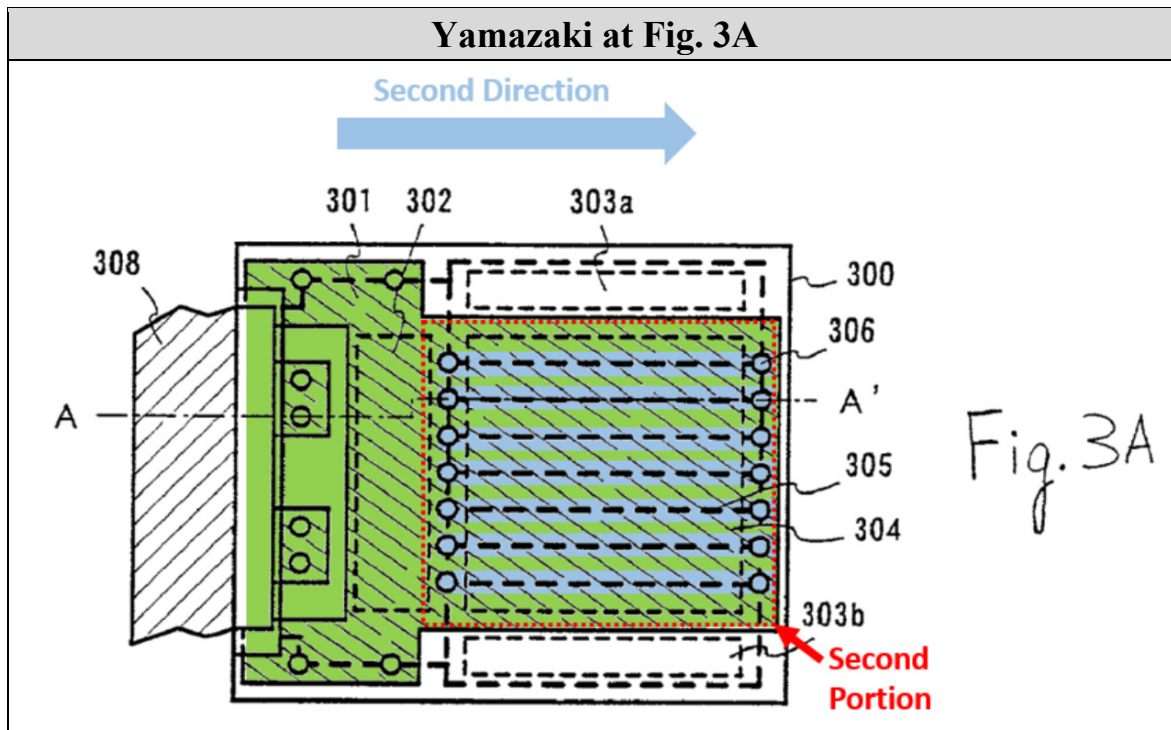
Yamazaki discloses “a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line” or renders this limitation obvious.

As discussed with respect to the previous limitation, a “power line,” in the context of the ’267 patent, supplies current and voltage to light-emitting elements and is indicated by the symbol “ V_{dd} .” See *supra* Section III.A.2.f; EX-1001 at 3:6-

Yamazaki discloses “current supply lines” each of which constitute a “second power line.” Each of Yamazaki’s “current supply lines” 305 connects to the

current supply auxiliary line 301. *See* EX-1008 [0038]-[0039]. Like the '267 patent's power lines, the combination of Yamazaki's current supply auxiliary line 301 (i.e., the "first power line") and its current supply line 305 (i.e., the "second power line") are designed to "make the electric potential equal in any position of the current supply line 305, and therefore" suppress "voltage drop." *See id.* at [0039]; *see also id.* at [0042].

Yamazaki's current supply lines extend in the second direction and have a portion that overlaps with a part of the first power line's second portion. As shown in figure 3A, reproduced and annotated below, Yamazaki's current supply line (highlighted in blue) extends in the same "second direction" in which its current supply auxiliary line" extends. The current supply line exists underneath the current auxiliary line's "second portion."



For these reasons, Yamazaki discloses and renders obvious a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line. EX-1006, ¶¶ 111-117.

- (h) 1[h] an inter-layer insulating film that is disposed between the first power line and the second power line,

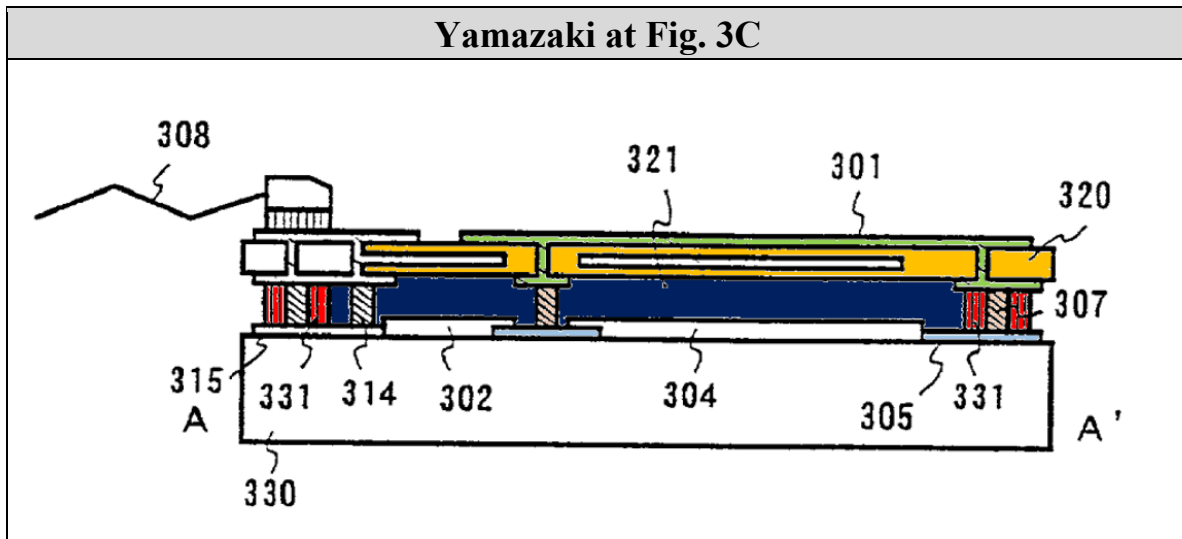
Yamazaki discloses “an inter-layer insulating film that is disposed between the first power line and the second power line” or renders this limitation obvious.

Yamazaki’s figure 3C shows a cross section of its “Embodiment Mode.” See EX-1008 at [0035]-[0047]. Yamazaki’s current supply auxiliary line 301 (i.e., the “first power line” shown in green) electrically connects to the current supply

line 305 (i.e., the “second power line” shown in blue) via conductor 307 (shown in pale red). *See id.* at [0038]-[0039]. Between these two power lines lies a “printed wiring board 320” (*see id.* at [0044]), a material such as “thermosetting [or] silicone resin” “filled in an airtight space 321 between the . . . substrate 330 and the printed wiring board 320” (*see id.* at [0045]), and a “sealing agent 331” (*see id.* at [0043]). Any of these components (or a combination of them) constitute an “inter-layer insulating film.” These components are “inter-layer” because they are disposed between the layer in which current supply auxiliary line 301 is formed and the layer in which current supply lines 305 are formed. *See id.* at Fig. 3C. These components are “insulating” because they do not conduct electricity between the power lines. *See id.* at [0044] (describing that the gap between the printed wiring board and substrate should not be so narrow as to cause the “printed wiring board 320” and the “luminous element” to be “in contact with each other”); EX-1006, ¶ 118; EX-1001 at 7:45-49, 8:51-54. These components are “films” because they are formed as thin regions that cover another region. *See* EX-1008 at [0015]-[0016] (describing a “printed wiring board” as a “board”), [0044]-[0045] (describing that the gap between the printed wiring board and substrate as “between 5 μ m and 1 mm (preferably between 10 and 100 μ m)” and that the resin may be filled in the airtight space in this gap), Fig. 3C (illustrating sealing agent 331 as a thin covering over conductor 307); EX-1006, ¶ 119; EX-1001 at 4:62-65 (describing a cathode,

for example as a formed as a “film . . . on the entire face of the display region 11”).

Figure 3C, reproduced below, highlights the printed wiring board 320 in orange, the resin 321 in dark blue, and the sealing agent 331 in bright red.



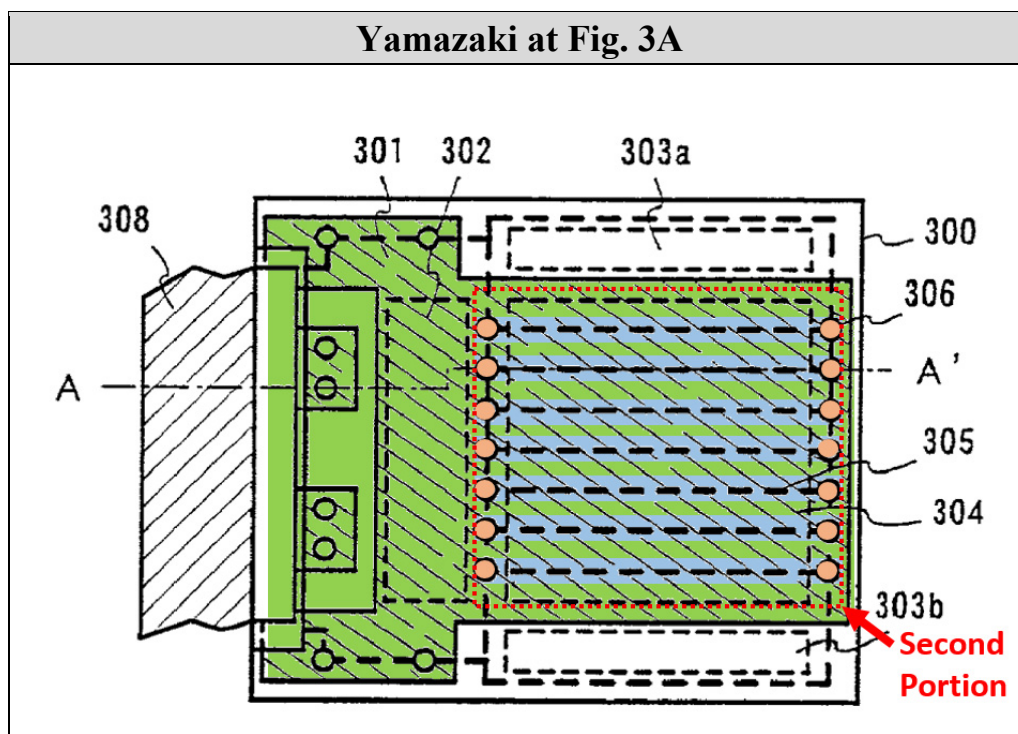
For these reasons, Yamazaki discloses and renders obvious an inter-layer insulating film that is disposed between the first power line and the second power line. EX-1006, ¶¶ 119-120.

- (i) 1[i] the second portion of the first power line being electrically connected to the second power line through plurality of contact holes.

Yamazaki discloses “the second portion of the first power line being electrically connected to the second power line through plurality of contact holes” or renders this limitation obvious.

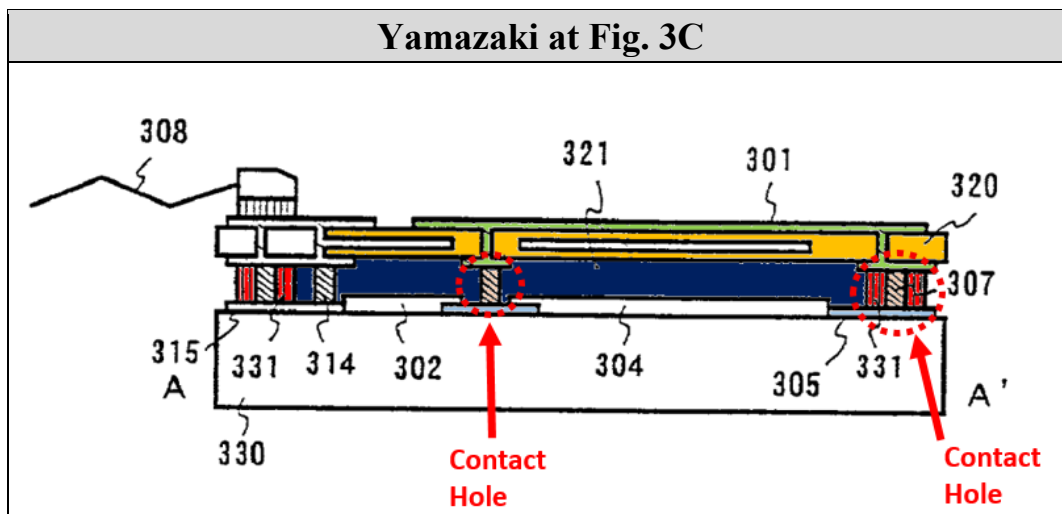
Yamazaki’s current supply auxiliary line 301 electrically connects to the current supply line 305 in “a contact portion 306” via the conductor 307. *See* EX-

1008 at [0038]-[0039]. Yamazaki's figure 3A, reproduced below, shows the second portion of auxiliary current supply line (*see supra* Section III.2.d (identifying the second portion relied upon in this petition)) has contact region 306 with multiple circles (highlighted in pale red) each indicating the presence of a contact hole to accommodate a conductor 307. *See* EX-1006, ¶¶ 117-118. Each current supply line 305 (highlighted in pale blue) features at least two contact holes.



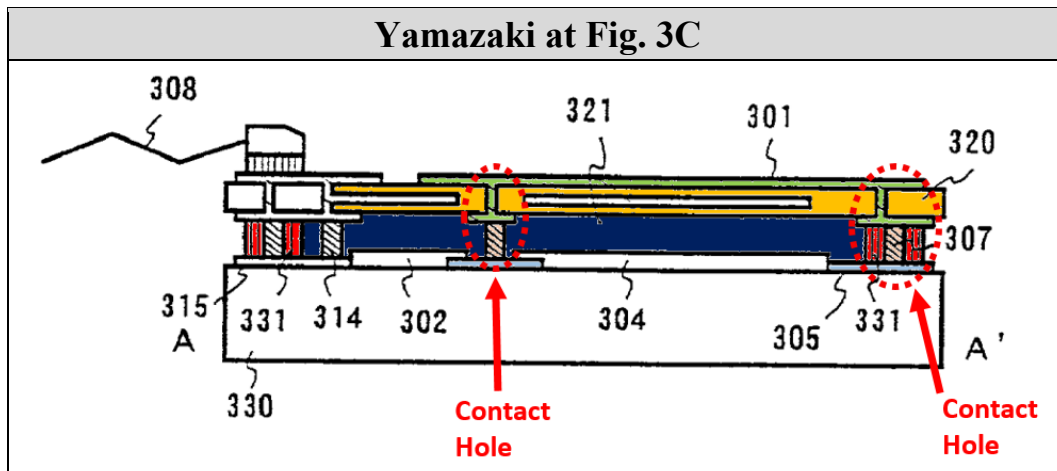
Yamazaki's figure 3C, reproduced below, shows a cross sectional view (cut along the lines A—A' of figure 3A), which depicts two conductors 307 (shown in pale red and indicated by diagonal shading) that each connect an exemplary current supply line 305 (shown in pale blue, which stretches horizontally through pixel portion 304) to the auxiliary current supply line 301 (shown in green). The two

contact holes that accommodate these conductors are each circled with a red dashed line. The left contact hole is formed in the insulating material, such a resin, (shown in dark blue) that fills the airtight space between the printed wiring board 320 and the substrate 330. *See supra* Section III.A.2.h; EX-1006, ¶¶ 117-118. The right contact hole is formed in the sealing agent 307 (shown in red and indicated by the vertical line pattern). *See id.*



Additionally, Yamazaki discloses contact holes formed in the printed wiring board. Yamazaki's first power line constitutes auxiliary current supply line 301, which has first and second portions formed atop the printed wiring board 320. *See supra* Section III. As shown in figure 3C, reproduced below, holes are formed the printed wiring board 320 that allow the wiring above electrically connect to the wiring below and then through to the conductors 307 below and the second power line (current supply line 305) formed on the substrate 330. *See* EX-1006, ¶¶ 117-

118.



For these reasons, Yamazaki discloses and renders obvious the second portion of the first power line being electrically connected to the second power line through plurality of contact holes. EX-1006, ¶¶ 117-118.

B. Koyama References (Ground 2 – Claim 1)

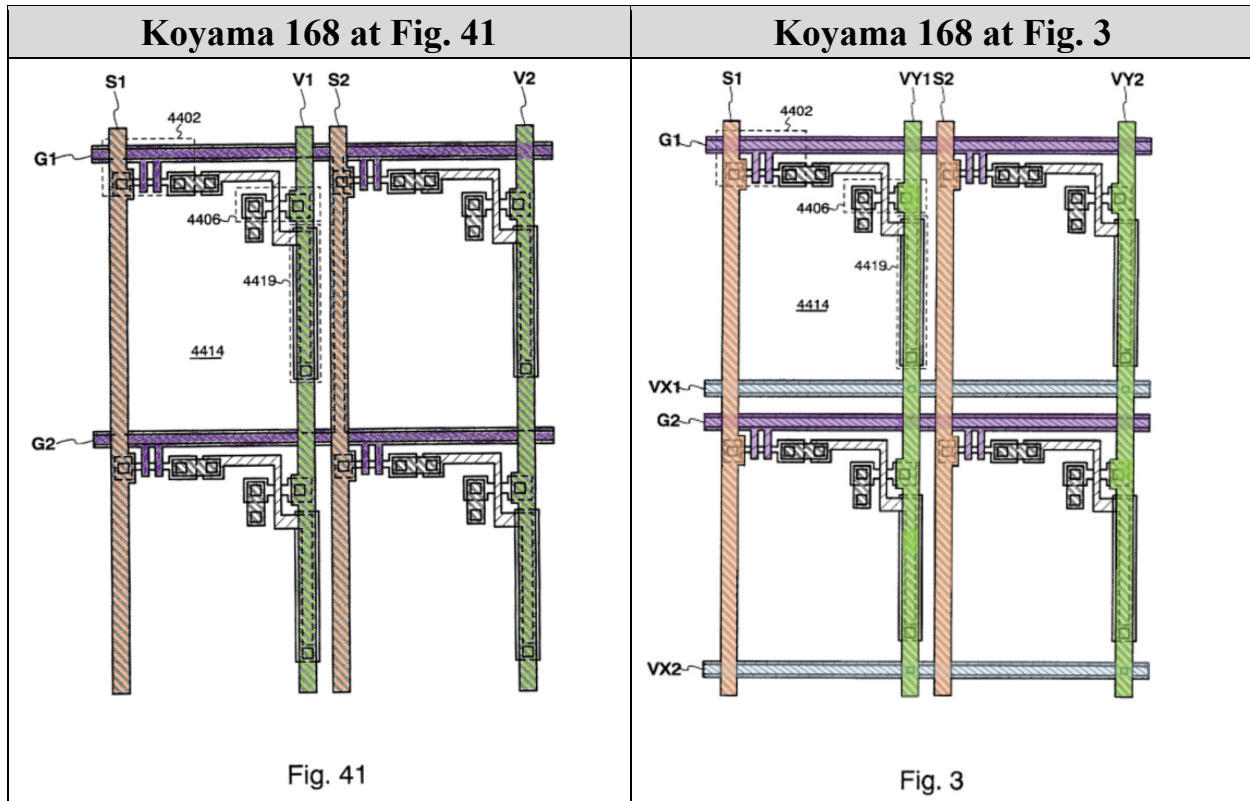
1. Overview of Koyama 168

U.S. Published App. No. 2001/0043168 (“Koyama 168”) is a published U.S. patent application that was filed May 7, 2000; published November 22, 2001; and issued March 30, 2004. *See* EX-1010. Koyama 168 thus qualifies as prior art under pre-AIA 102(a) and (e). *Id.*

Koyama 168 generally relates to an electronic display based on electroluminescent elements. *See* EX-1010 at [0002]; *see also id.* at [0003]-[0051] (providing background of such displays). It acknowledges that such displays feature “power

supply lines” that supply “electric potential” (i.e., voltage) to pixels, which cause EL elements in those pixels to emit light. *See id.* at [0014]-[0023]; EX-1006, ¶126. Koyama 168 acknowledges that in prior art displays “as the size of the display of the display device becomes larger, the current consumption increases in proportion to the area of the display.” *See id.* at [0047]; *see also id.* at [0050] (describing “potential drop with regard to a power supply line” that increases with distance “from the input portion”). Like the ’267 patent, Koyama 168 addresses this problem by providing a plurality of power lines for “alleviating potential drop due to wiring resistance of a power supply line, in particular, potential drop due to wiring resistance at a portion where the power supply line is drawn out.” *Id.* at [0053]. Specifically, “[b]y drawing out the power supply lines in two directions of the display device . . . compared with a case where the power supply lines are drawn out in one direction, the length of the wiring from the power supply lines of the pixel portion to the external input terminals can be shorter and the variation in the length of the wiring can be decreased. By the above structure, the influence of the potential drop at the drawn-around portion of the power supply lines around the pixel portion can be decreased.” EX-1010 at [0133]-[0134]. Also like the ’267 patent, Koyama 168 states that having multiple power lines improves aperture ratio. *See* EX-1010 at [0169]; EX-1001 at 2:10-13.

Comparing Koyama 168's figure 41 to figure 3 illustrates this concept. Koyama 168's Figure 41 shows a "conventional display device," which features two vertically oriented "power supply lines V1 and V2." *See* EX-1010 at [0040]-[0044]. These power lines distribute voltage and current to EL elements designated 4414. *See id.* at [0042]-[0044]. Koyama 168's Figure 3 is a "top view" corresponding to "Embodiment 2" of the invention, and in contrast to the described conventional display device, it featured "power supply lines VX1 and VX2 . . . connected through contact holes to conventional power supply lines VY1 and VY2." *Id.* at [0162]; *see also id.* at [0149] (identifying EL element 4414, VX1-VXn, and VY1-VYn). Figures 41 and 3 are annotated below to show the vertically oriented power supply lines in green, the gate signal line in purple, and the source signal line in brown. Figure 3 is additionally annotated to show the horizontally oriented power supply lines in blue.



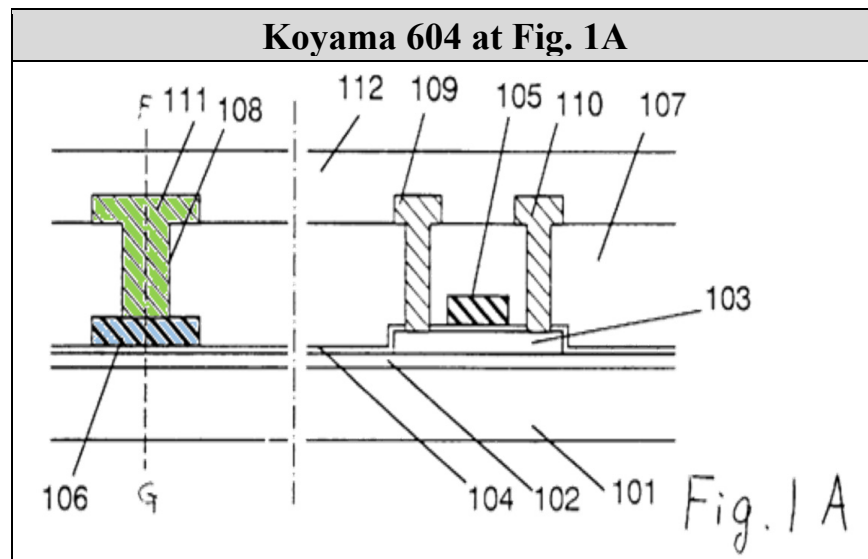
2. Overview of Koyama 604

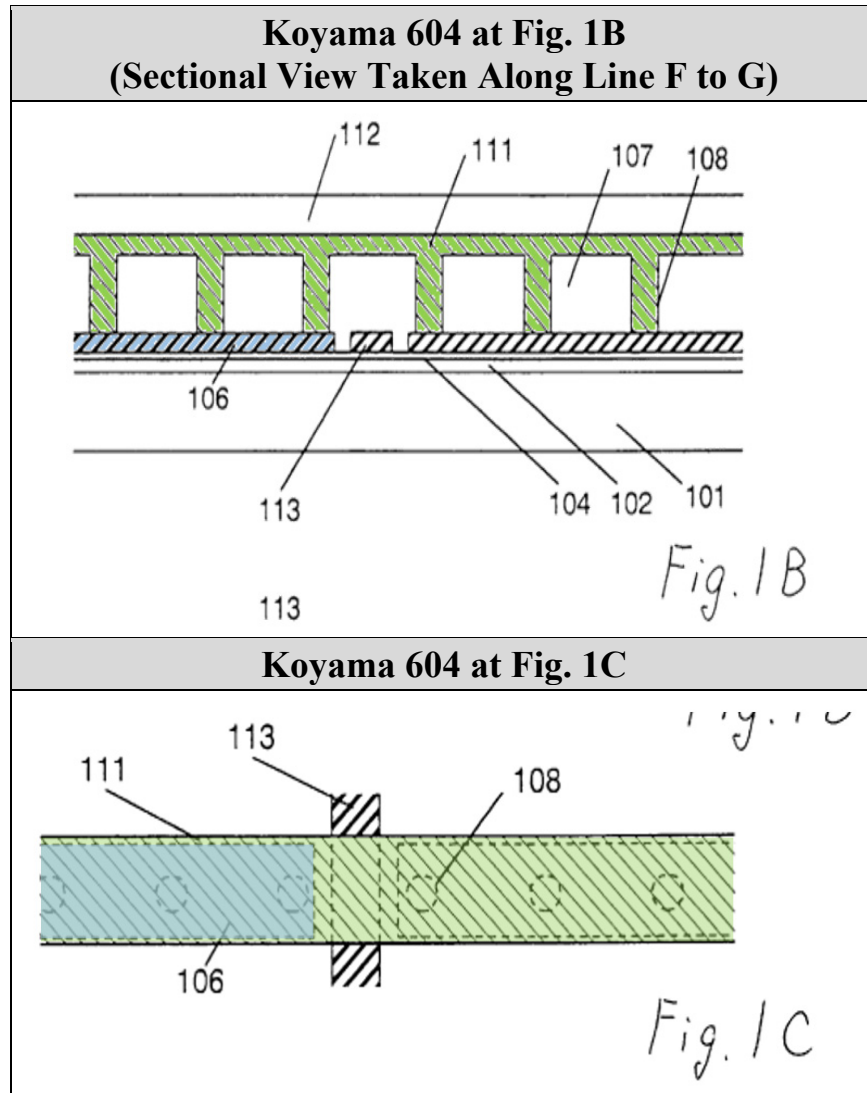
U.S. Patent No. 6,124,604 (“Koyama 604”) is a U.S. patent that was filed December 22, 1997 and issued September 26, 2000. *See* EX-1011. Koyama 604 thus qualifies as prior art under pre-AIA 102(b). *Id.*

Koyama 604 improves the “wiring structure of an integrated circuit” formed on a substrate that includes thin film transistors (TFTs), such as liquid crystal displays using active matrix circuits. *See* EX-1011 at 1:7-48. Such displays used “wiring lines . . . to transmit clock signals or video signals” to the TFTs.” *See id.* at 1:66-2:8. Due to the “mobility values” of TFT technology at the time, wiring could not carry a signal at excessive frequency. *See id.* at 1:37-2:36. Although the

inventors previously developed TFTs that could accommodate higher-frequency signals (*see id.* at 2:9-36), such signals could become “rounded” when the TFTs were formed over a large area (*see id.* at 2:36-4:21).

Koyama 604 ameliorates that problem by applying a specific technique to reduce the “electric resistance of wiring lines” without increasing “capacitance.” *See* EX-1011 at 4:22-53; 4:56-5:29. Specifically, it discloses a “wiring line 111” that connects “in parallel to an auxiliary wiring line 106 via a plurality of contact holes 108 that are formed through the interlayer insulating film 107.” *Id.* at 5:55-58; *see also id.* at 5:59-67. The figures below show the “wiring line 111” in green and the “auxiliary wiring line 106” in blue. *See id.* at 5:43-7:49.





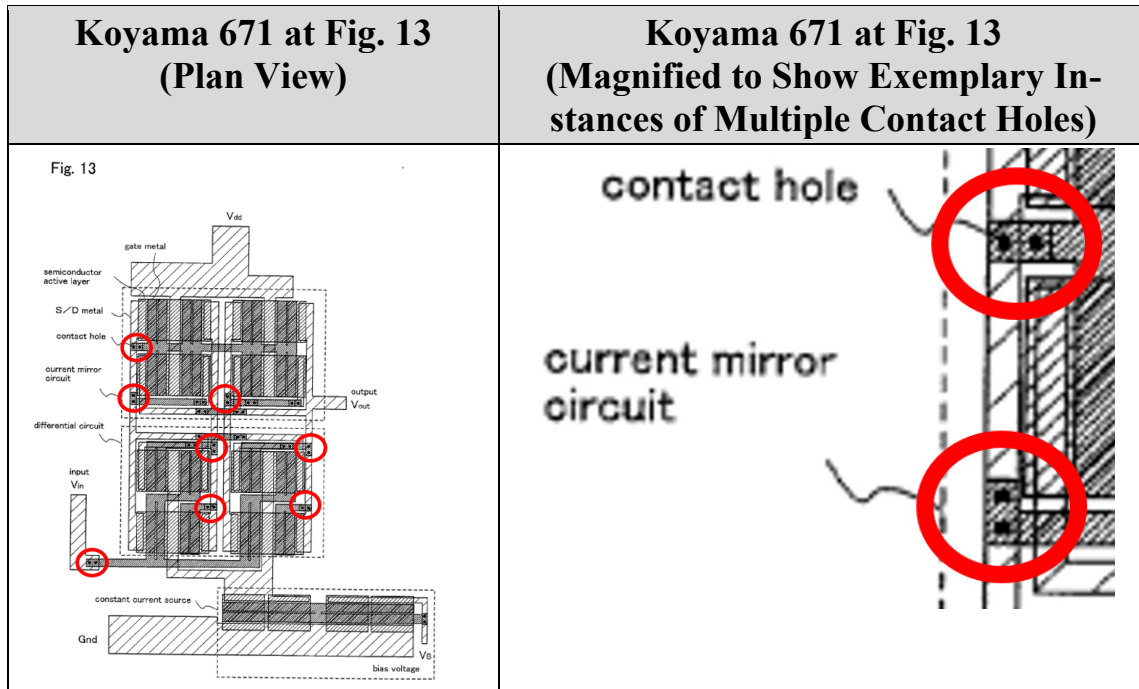
3. Overview of Koyama 671

U.S. Published App. No. 2002/0053671 (“Koyama 671”) is a published U.S. patent application that was filed November 9, 2001, published May 9, 2002, and issued December 14, 2004. *See* EX-1012. Koyama 671 thus qualifies as prior art under pre-AIA 102(a) and (e). *Id.*

Koyama 671 generally relates to an improved “analog buffer circuit.” *See* EX-1012 at Abstract, [0002]. Electric displays used such circuits to buffer signals

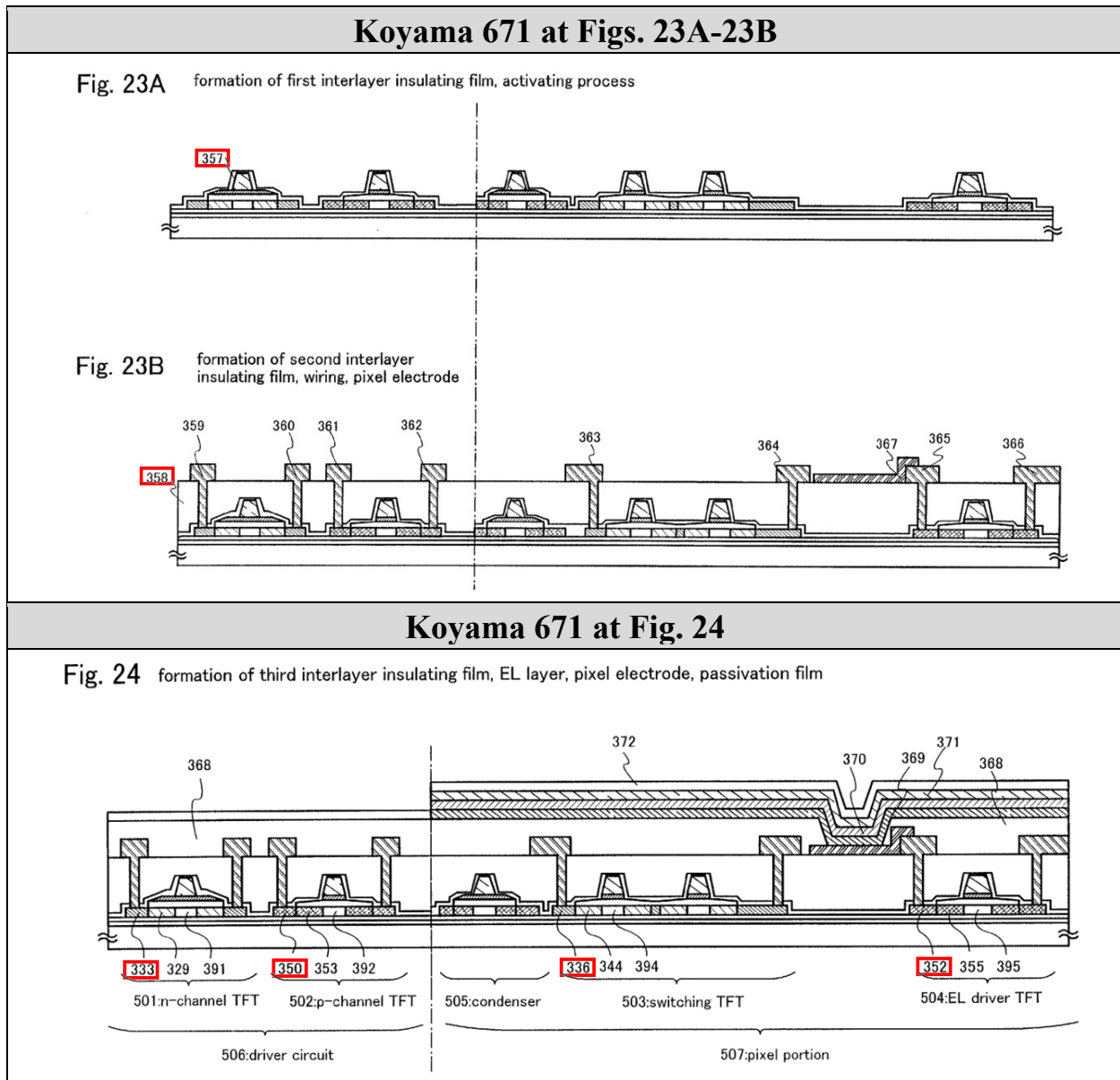
emanating from the “source signal line driver circuit” . . . “to reduce the influence of round[ing] of a [source] signal due to the load,” particularly in displays “having a large number of pixels.” *Id.* at [0019]-[0020]. Koyama 671 discloses an “Embodiment 4” of its improved analog buffer circuit, which it depicts in both schematic view (Figure 12) and plan view (Figure 13). *See id.* at [0169]-[0193]. In Figure 13’s plan view, which models how the circuit would be physically manufactured, various portions formed in the “S/D metal” layer, the “gate metal” layer, and the “semiconductor active” layer electrically connect to each other through contact holes to implement Figure 12’s schematic. *See* EX-1006, ¶ 133.

Koyama 671’s analog buffer circuit uses multiple contact holes to connect these layers, thereby reducing electric resistance. *See id.* In several instances, these multiple-contact-hole connections are accommodated by portions that protrude from the side of the main line. *Id.* Examples of these instances are circled in red in the reproductions of Figure 13 in the table below.



Koyama 671 also shows the “method of manufacturing an EL display device as a semiconductor device having an analog buffer circuit of the present invention” in a series of cross sectional views. *See* EX-1012 at [0195]; *see also id.* at [0195]-[0256], Figs. 21-24. This method, described as “Embodiment 5,” “can be embodied by freely combining Embodiments 1 through 4.” *Id.* at [0256]. These views show how this process forms contact holes, showing “contact holes that reach the respective impurity regions 333, 336, 350, and 352” as examples. *See id.* at [0231]. As shown in figures 23A and 23B, “a first interlayer insulating film” 357 and a “second interlayer insulating film” 358 are disposed between the layers connected by the contact holes (which correspond to the vertical pillars shown in fig-

ure 24). *See id.* at [0224]-[0235]. The numbers calling out the first and second interlayer insulating films and the impurity regions at the bottom of the contact holes are identified by red boxes in the reproduced figures in the table below.



4. Motivations to Combine the Koyama References

A POSITA would have been motivated to modify Koyama 168 in view of

Koyama 604 and/or Koyama 671 to arrive at the “Koyama Combination” described in more detail below. *See generally* EX-1006, ¶¶ 125-134.

(a) A POSITA Would Have Been Motivated to Increase the Number of Contact Holes that Connect Koyama 168’s First and Second Power Lines

Koyama 168 recognizes that “potential drop due to the wiring resistance of a power source supply line” contributes to the unevenness in a display region.” *See* EX-1010 at Abstract. It acknowledges that a power supply line’s wiring resistance causes “potential drop” along different points in that line, affecting the “brightness of the emitted light” from different pixels along the display, causing an “uneven display.” *See id.* at [0032]-[0036].

Koyama 168 reduces “the influence of the potential drop” by “drawing out the power supply lines in two directions” rather than just one, which effectively shortens “the length of the wiring from the power supply lines of the pixel portion to the external input terminals.” *Id.* at [0133]-[0134]. The power supply lines going in one direction (VX1 and VX2) “are connected through contact holes to conventional power supply lines VY1 and VY2” going in another direction. *See id.* at [0162].

Because wiring resistance is the cause of the potential drop problem, a POSITA implementing Koyama 168 would have understood that further reducing the wiring resistance of the power supply lines would be beneficial. Koyama 168

itself taught that the wiring resistance of these power lines should be reduced in order to reduce “the influence of the potential drop.” *See id.* at Abstract; *id.* at [0034-0035] (describing that variation of “the electrical potential of the power supply line . . . may not present a great problem in such a case where the wiring resistance of the power supply line is small”); *id.* at [0157] (discussing embodiment in which “the wiring resistance is decreased”). Indeed, in an idealized circuit, the power supply lines would have no resistance whatsoever, and therefore would experience no potential drop. *See id.* at [0145] (stating basic circuit principle that potential drop “ IR ” depends upon wiring resistance “ R ”); EX-1006, ¶¶ 46-50.

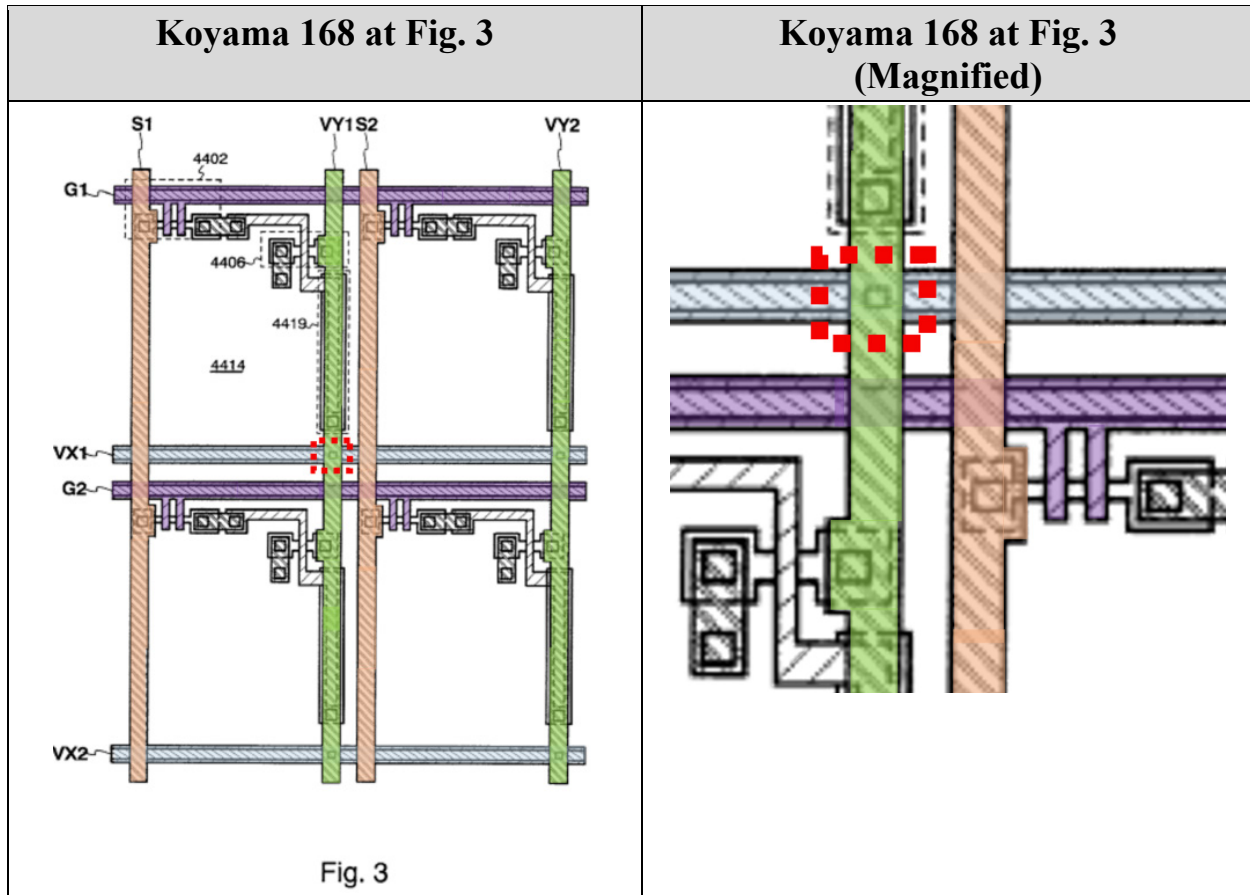
Koyama 604 further taught that “[a]s the number of contact holes . . . for connecting [wiring lines] increases, the electrical connection between the [those lines] becomes better, that is, the contact resistance decreases, whereby the electric resistance of the combination of the [lines] decreases.”). EX-1011 at 6:16-23.

Thus a POSITA implementing Koyama 168, which used a single contact hole to connect any two power lines, would have understood that wiring resistance could be advantageously further reduced by increasing the number of contact holes that connect those lines, as taught by Koyama 604.

- (b) A POSITA Would Have Been Motivated to Modify Koyama 168’s First Power Lines to Feature Protrusions to Accommodate the Increased Number of Contact Holes

A POSITA would recognized that modifications to Koyama 168’s power

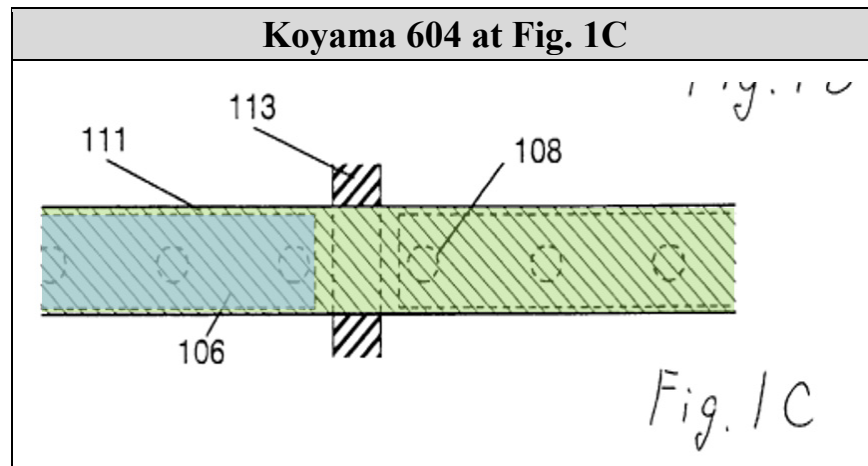
lines would have been necessary to accommodate more contact holes. Koyama 168's Figure 3 depicts how multiple power lines drawn out in different directions would be laid out. The vertical "VY" power lines (shown in green) connect to the horizontal "VX" power lines (shown in blue) at their intersections by one contact hole (shown by a square box). As shown by the figures below, the vertical "VY" power lines, as originally contemplated by Koyama 168 are not wide enough to accommodate multiple contact holes of the same size. EX-1006 ¶¶, 130-131. A POSITA would further recognize it would not be desirable to make smaller contact holes that fit in the space provided, because having smaller contact holes would increase resistance, contrary to the very purpose of having multiple contact holes in the first place. *See id.* (explaining that wiring resistance decreases with increasing contact width).



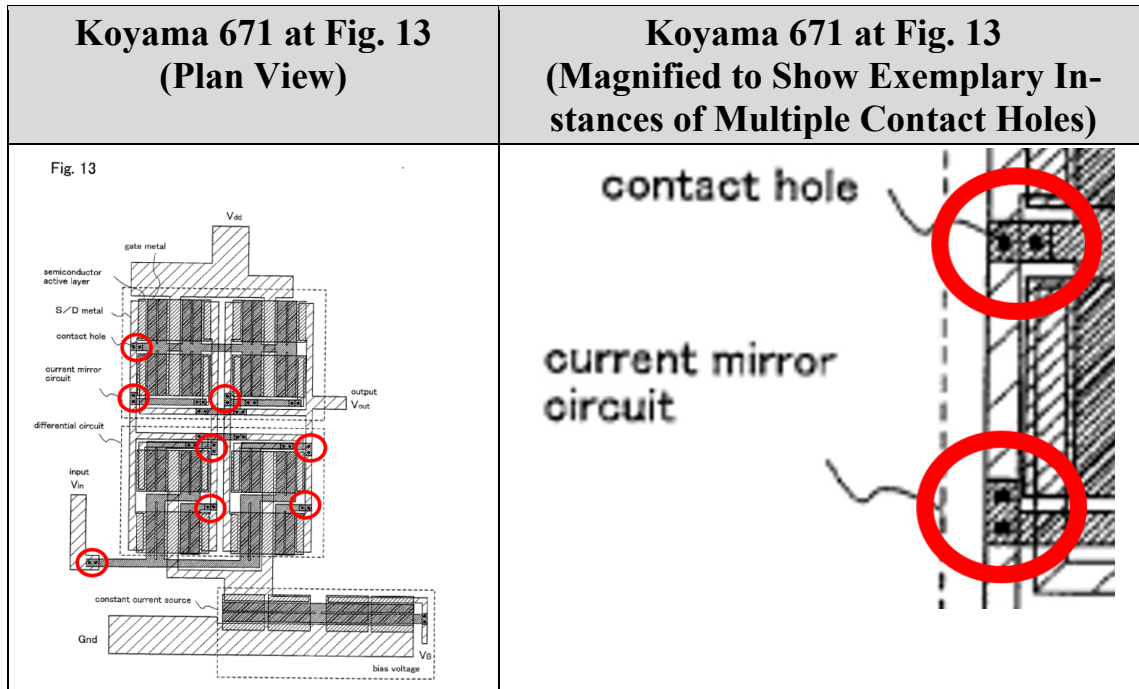
Faced with that problem and the desire to use multiple contact holes, a POSITA would have exercised ordinary creativity and considered options for increasing the overlap between the two power lines to accommodate more contact holes. To increase that overlap, either the horizontal power line, the vertical power line, or both, would need to be increased in some way. *See* EX-1006 ¶¶ 130-131. A protrusion of the vertical power line extending in the same direction as the second power line is one option (of very few options) that a POSITA would have found obvious to try.

Koyama 604 confirms that having a power line protrusion would have been

an obvious solution for creating enough overlap to accommodate multiple contact holes. As shown by figure 1C below, Koyama 604 features such a protrusion of “wiring line 111” (in green) over “auxiliary wiring line 106” (in blue) to accommodate a plurality of contact holes 108 that are formed through the interlayer insulating film 107.” EX-1011 at 5:55-58; *see also id.* at 5:59-67.



Koyama 671 provides further confirmation that having a power line protrusion would have been an obvious solution for creating enough overlap to accommodate multiple contact holes. Its figure 13 depicts, even more explicitly than Koyama 604, the use of a protrusion as the mechanism of creating the overlap needed for multiple contact holes.



(c) A POSITA Would Have Had at Least a Reasonable Expectation of Success in Making the Proposed Combination

First, each reference constitutes “analogous art” to the ’267 patent. *See Donner Tech., LLC v. Pro Stage Gear, LLC*, 979 F.3d 1353, 1359 (Fed. Cir. 2020)

(“Two separate tests define the scope of analogous prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed and, (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved.”).

The ’267 patent, Koyama 168, Koyama 604, and Koyama 671 all apply to the same field of endeavor: an electronic display (electro optical device) based on

electroluminescent elements. *See* EX-1001 at 1:12-14 (“The present invention relates to a wiring layout suitable for an electro-optical device including electro-optical devices.”); EX-1010 at [0002] (“The present invention relates to an electronic display (electro optical device) formed by fabricating an EL (electro luminescence) element on a substrate.”); EX-1011 at 16:25-30 (“The invention can be used not only in peripheral circuits that are formed on the same substrate as an active matrix circuit of a transmission or reflection type active matrix liquid crystal display device, but also in display devices using EL (electroluminescence) element and other various circuits using TFTs.”); EX-1012 at [0002] (“[T]he present invention relates to a semiconductor device as an image display device.”), [0004] (referencing “electroluminescence” display device).

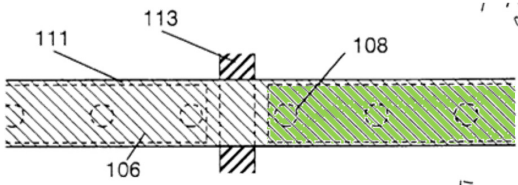
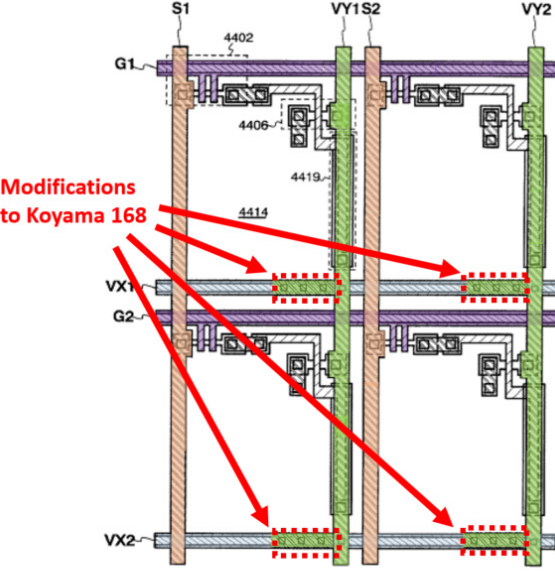
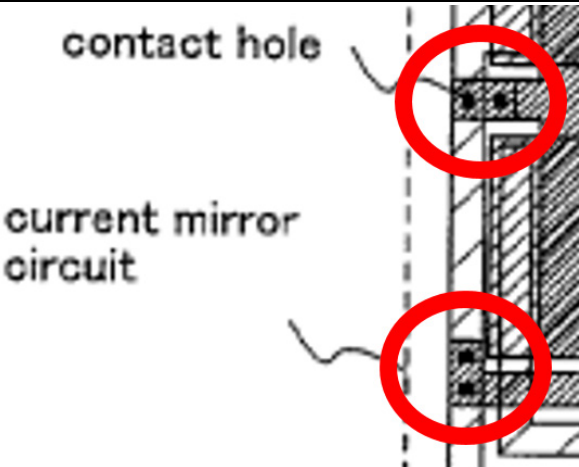
The ’267 patent, Koyama 168, and Koyama 604 all address their respective problems—essentially ensuring that power or signals are not attenuated because they must pass relatively long distances—in the same manner: by reducing the resistance of the wiring that carries that power or signals. The ’267 patent and Koyama 168 reduce the resistance of the wiring carrying power by laying out multiple power lines in a matrix pattern. *See* EX-1001 at 7:55-61 (“[T]he electric power lines . . . are disposed . . . in the form of a matrix, and accordingly, the wiring resistance of the electric power lines . . . can be reduced, thereby enabling sufficient current supply to the organic EL devices.”); EX-1010 at [0149] (“Power supply

lines . . . are disposed not only in a direction in parallel with source signal lines . . . but also in a direction perpendicular to them. Therefore, voltage is supplied to either a source region or a drain region of the TFT 4406 for driving of the pixel from the respective directions. . . . Therefore, the opening ratio can be improved even with regard to a pixel having a structure where power supply lines are disposed both vertically and horizontally (like a matrix.”). The ’267 patent and Koyama 604 reduce wiring resistance by increasing the number of contacts that electrically connect two wires carrying the same signal. *See* EX-1001 at 8:60-64 (“[A] plurality of each of the contact holes . . . are formed, whereby the present embodiment . . . has the advantage of reducing the wiring resistance.”); EX-1011 at 6:16-23 (“As the number of contact holes 108 for connecting the wiring line 111 and the auxiliary wiring line 106 increases, the electrical connection between the wiring line 111 and the auxiliary wiring line 106 becomes better, that is, the contact resistance decreases, whereby the electric resistance of the combination of the wiring line 111 and the auxiliary wiring line 106 decreases.”).

Second, the Koyama references all feature Jun Koyama as a named inventor and their teachings are all applicable to electroluminescent displays.

Third, in Koyama 168’s figure 3, reproduced below, there are no obstacles to extending the VY power lines to overlap the VX power lines to accommodate

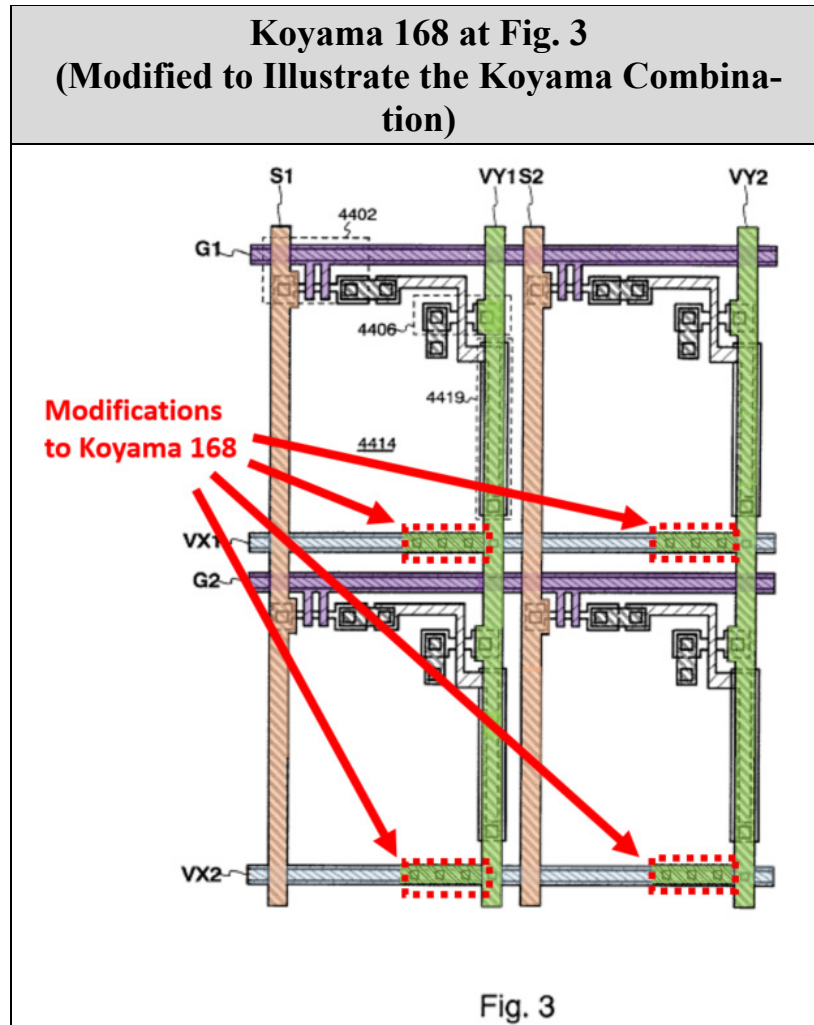
more contact holes. *See* EX-1006, ¶ 134. This modification would have simply required patterning the layout to build another set of contact holes and extend the vertical power lines, as shown in Koyama 604's Figure 1C and Koyama 671's Figure 13. *See id.*

Koyama 604 at Fig. 1C	Koyama 168 at Fig. 3
 Fig. 1C	 Fig. 3
Koyama 671 at Fig. 13 (Magnified to Show Exemplary Instances of Multiple Contact Holes) 	

5. Combination of Koyama References

In the combination of Koyama 168 with Koyama 604 and/or Koyama 671, Koyama 168's vertically oriented power supply lines (e.g., VY1 and VY2) are

modified to accommodate *multiple* contact holes to electrically connect to the horizontally oriented power supply lines (e.g., VX1 and VX2) rather than just one contact hole. A POSITA would have recognized that Koyama 168's circuitry would have been modified to accommodate these additional contact holes to reduce resistance and thereby improve distribution of power to the pixels. EX-1006, ¶¶ 125-134. The vertically oriented power lines would have been modified to feature protrusions extending to the left so that the additional contact holes could be accommodated. *See id.* The annotated figure 3 from Koyama 168 shown below show these modifications in red boxes.



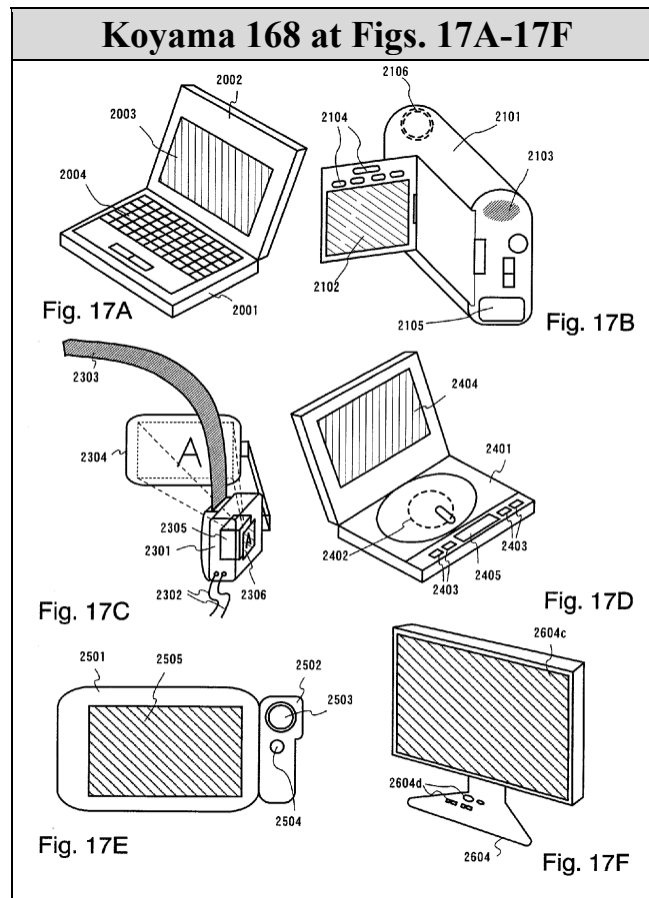
6. Claim 1

- (a) 1[a] An electro-optical device comprising:

The Koyama Combination renders obvious “an electro-optical device.”

Koyama 168 discloses an “Embodiment 19” that corresponds to an “EL display device manufactured by applying the present invention” as implemented in “various kinds of electronic equipment.” *See* EX-1010 at [0438]-[0448]; *see also id.* at [0448] (noting that Embodiment 19 can be “freely combined” with any of the

foregoing embodiments.). One example of such electronic equipment is a “personal computer.” *Id.* at [0441], Fig. 17A. Any of the exemplary electronic equipment disclosed in Koyama 168 constitutes “electro-optical devices.” *See also* EX-1001 at 2:26-31, 3:54-59, 9:19-65, Figs. 6A-6F (providing similar examples of electro-optical devices).



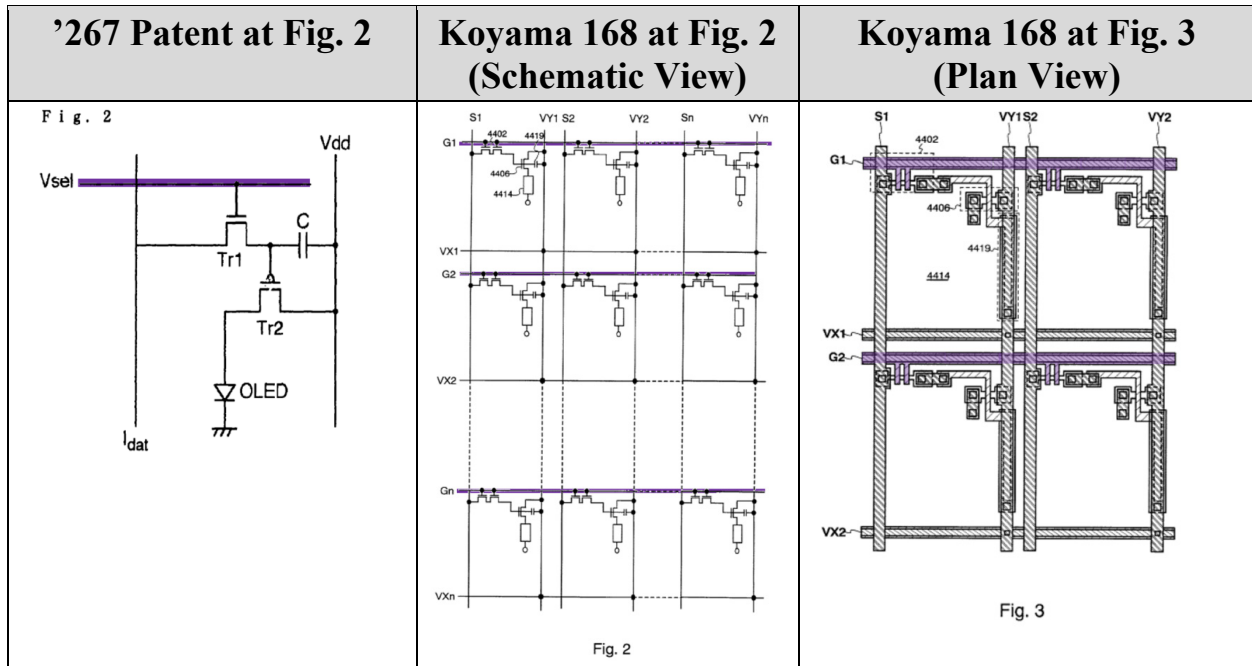
For these reasons, the Koyama Combination discloses and renders obvious an electro-optical device. EX-1006, ¶ 135.

(b) 1[b] a scan line;

The Koyama Combination renders obvious “a scan line.”

Koyama 168 discloses that conventional EL display devices have “gate signal line[s] (G1 to Gy) for inputting a selected signal from a gate signal line driver circuit . . . to a gate electrode of a switching TFT 1801 of the respective pixels.” *See* EX-1010 at [0013], Fig. 18. Koyama 168’s “Embodiment Mode 4” also features these gate signal lines, as shown by the “G” lines depicted in figures 2 and 3.

Each of Koyama 168’s “gate signal lines (G1 to Gy)” constitutes a scan line because each gate signal line controls the gates of the “switching TFTs.” *See id.* at [0020] (explaining timing of gate signals, including period in which “[a]ll the switching TFTs connected to the gate signal line G1 are turned on to thereby input the analog video signal . . . through the switching TFT”), Fig. 19; *see also* EX-1001 at 5:6-31 (describing the “switching transistor Tr1” as comprising a “gate terminal . . . connected to the scan line V_{sel} ”). In the table below, figure 2 of the ’267 and figures 2 and 3 of Koyama 168 highlight in purple the scan lines.



For these reasons, the Koyama Combination discloses and renders obvious a scan line. *See* EX-1006, ¶¶ 136-139.

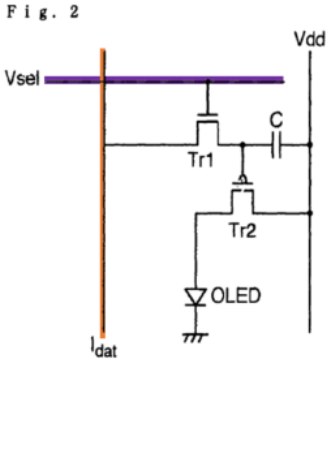
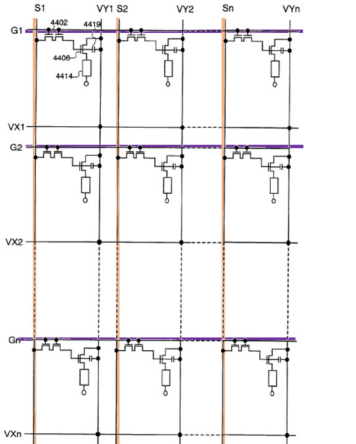
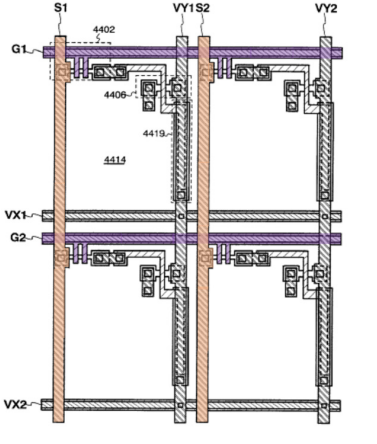
(c) 1[c] a data line that intersects the scan line;

The Koyama Combination renders obvious “a data line that intersects the scan line.”

Koyama 168 discloses that conventional EL display devices have “source signal line[s] (also called data signal line[s]) (S1 to Sx) for inputting an analog video signal” and are connected to source or drain regions of switching TFTs. *See* EX-1010 at [0013], Fig. 18. Koyama 168’s “Embodiment Mode 4” also features these source signal lines, as shown by the “S” lines depicted in figures 2 and 3.

Each of Koyama 168’s “source signal line[s] (S1 to Sx)” constitutes a data line because each source signal line inputs a video signal to the source or drain of

the “switching TFTs.” *See id.*; *id.* at [0020] (explaining timing of video signals, including period in which “[a]n analog video signal is then sequentially inputted to source signal lines (S1 to Sx)”), Fig. 19; *see also* EX-1001 at 5:21-31 (explaining how data signals result in light-emission). In the table below, figure 2 of the ’267 and figures 2 and 3 of Koyama 168 highlight in brown the data lines.

'267 Patent at Fig. 2	Koyama 168 at Fig. 2 (Schematic View)	Koyama 168 at Fig. 3 (Plan View)
 Fig. 2	 Fig. 2	 Fig. 3

For these reasons, the Koyama Combination discloses and renders obvious a data line that intersects the scan line. *See* EX-1006, ¶¶ 136-139.

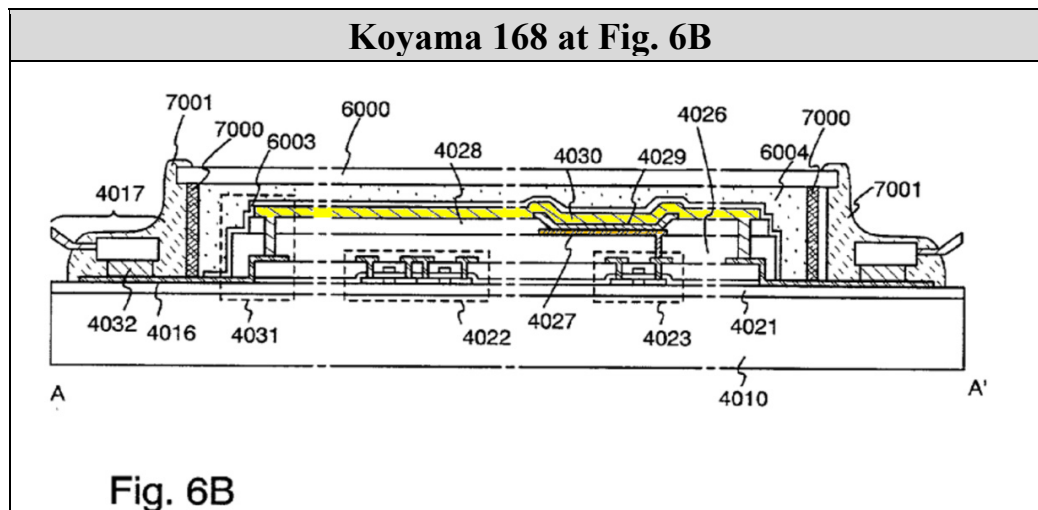
(d) 1[d] a first electrode; a second electrode;

The Koyama Combination renders obvious a “first electrode [and] a second electrode.”

Koyama 168 discloses that conventional EL display devices have “EL elements” 1806 each “composed of an anode, a cathode, and an EL layer sandwiched

therebetween.” *See* EX-1010 at [0015] (referring to the anode and cathode as “opposing electrodes”); *see also id.* at [0007], Fig. 18. Koyama 168’s “Embodiment Mode 4” also features EL elements having electrodes, as shown by element 4414 depicted in figures 2 and 3. *See id.* at [0148]-[0149], [0162]. The anode and cathode each constitute the first and the second electrode claimed by the ’267 patent.

Koyama 168 also illustrates first and second electrodes with respect to Embodiment 5. *See* EX-1010 at [0177]-[0198] (referencing cross sectional view shown in figure 6B that shows “pixel electrode 4027,” “EL layer 4029,” and “cathode 4030”). Figure 6B is reproduced below and highlighted to identify the “pixel electrode 4027” in orange and the “cathode 4030” in yellow.



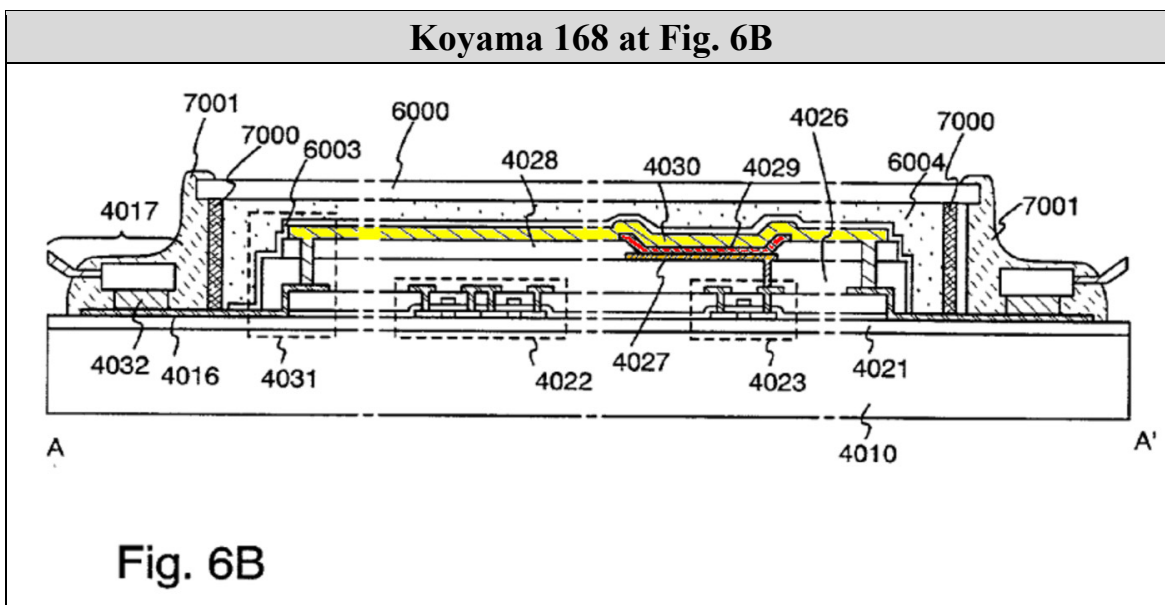
For these reasons, the Koyama Combination discloses and renders obvious a first electrode and a second electrode. *See* EX-1006, ¶¶ 140-142.

- (e) 1[e] a light emission layer that is disposed between the first electrode and the second electrode;

The Koyama Combination renders obvious a “light emission layer that is disposed between the first electrode and the second electrode.”

Koyama 168 discloses that conventional EL display devices have “EL elements” 1806 each “composed of an anode, a cathode, and an EL layer sandwiched therebetween.” *See* EX-1010 at [0015], Fig. 18. Koyama 168’s “Embodiment Mode 4” also features EL elements having an EL layer, as shown by element 4414 depicted in figures 2 and 3. *See id.* at [0148]-[0149], [0162]. The EL layer is a “light-emitting layer” and thus constitutes the “light emission layer” claimed by the ’267 patent. *See id.* at [0007].

Koyama 168 illustrates its EL layer with respect to Embodiment 5. *See* EX-1010 at [0182]-[0188] (referencing cross sectional view shown in figure 6B that shows “pixel electrode 4027,” “EL layer 4029,” and “cathode 4030”). Figure 6B is reproduced below and highlighted to identify the “EL layer 4029” in red.



For these reasons, the Koyama Combination discloses and renders obvious a light emission layer that is disposed between the first electrode and the second electrode. *See* EX-1006, ¶¶ 140-142.

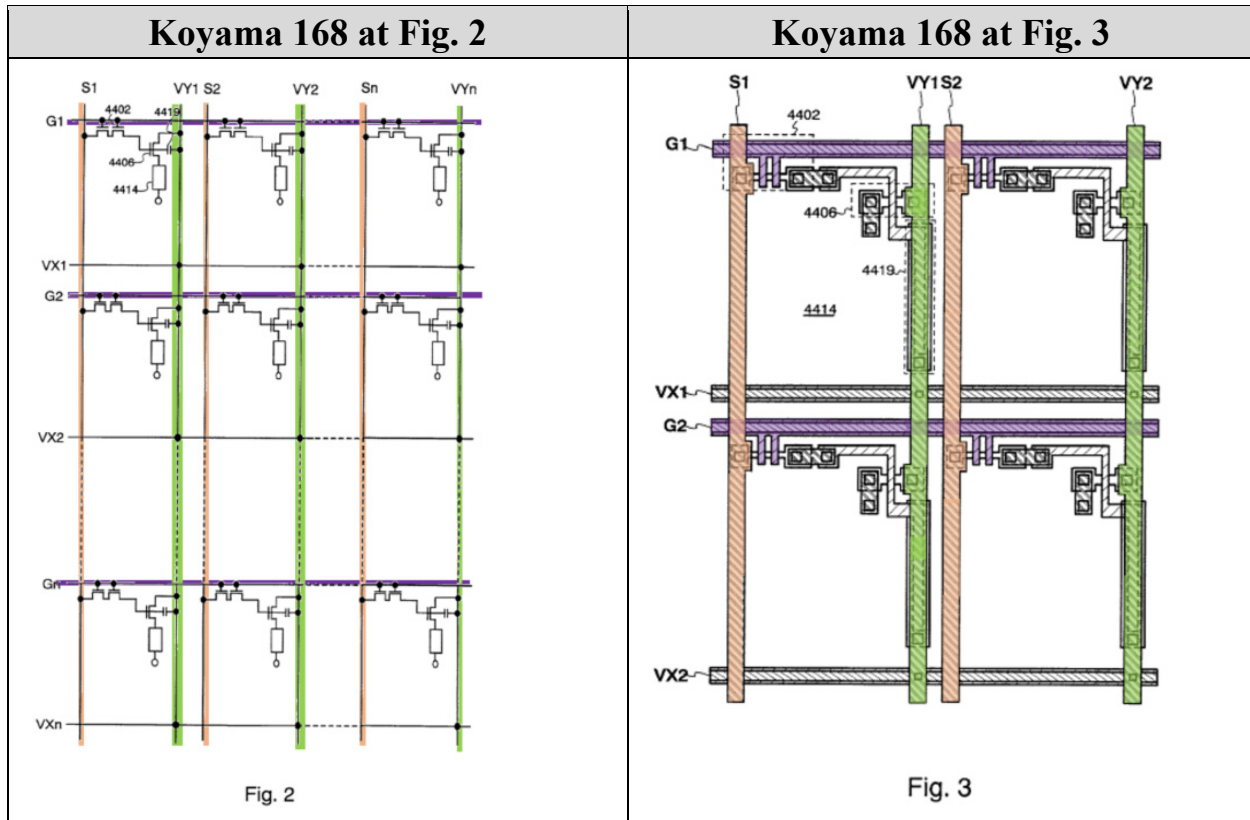
- (f) 1[f] a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction;

The Koyama Combination renders obvious a “first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction.”

As discussed above with respect to Ground 1 Claim Element 1[f], a “power line,” in the context of the ’267 patent, supplies “driving voltages” and current to light-emitting elements. *See supra* Section III.A.2.f (discussing EX-1001 at 3:6-11, 4:7-9, 7:56-61, 9:5-11, Fig. 5).

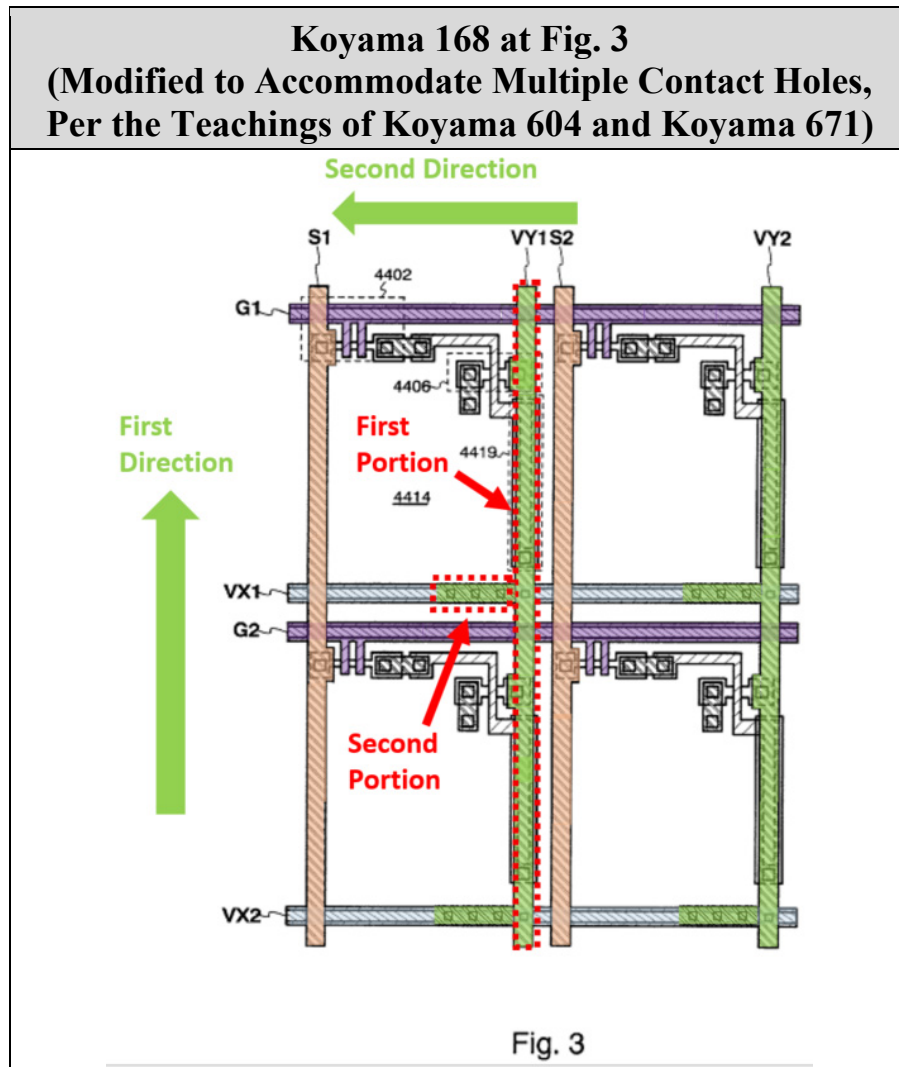
Koyama 168 discloses a “first power line.” Koyama 168’s Figure 3 is a “top view” corresponding to “Embodiment 2” of the invention, and it features “power supply lines VX1 and VX2 . . . connected through contact holes to conventional power supply lines VY1 and VY2.” EX-1010 at [0159]-[0162]. These power lines distribute power to EL elements 4414. *See id.* at [0042]-[0044].

The power supply VY1, for example, constitutes a “first power line.” Figures 2 and 3 are reproduced below and highlight VY1 in green.



The Koyama Combination renders obvious that the first power line has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction. As explained above, the Koyama Combination features Koyama 168's circuitry except that the vertical "VY" power lines feature protrusions to accommodate multiple contact holes that connect to the horizontal "VX" power lines. *See supra* Section III.B.4-5 (citing, e.g., EX-1010 at [0002], [0149]; EX-1011 at 6:16-23, 16:25-30, Fig. 1C, EX-1012 at [0002], [0004], Fig. 13). As shown in the annotated version of Koyama 168 Fig. 3 reproduced below, the main length of the vertical power lines would constitute a "first

portion” of the first power line that extends in a first direction and the added protrusions constitute a “second portion” of the first power line that extends in a second direction.



For these reasons, the Koyama Combination discloses and renders obvious a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction. *See* EX-1006, ¶¶ 143-148.

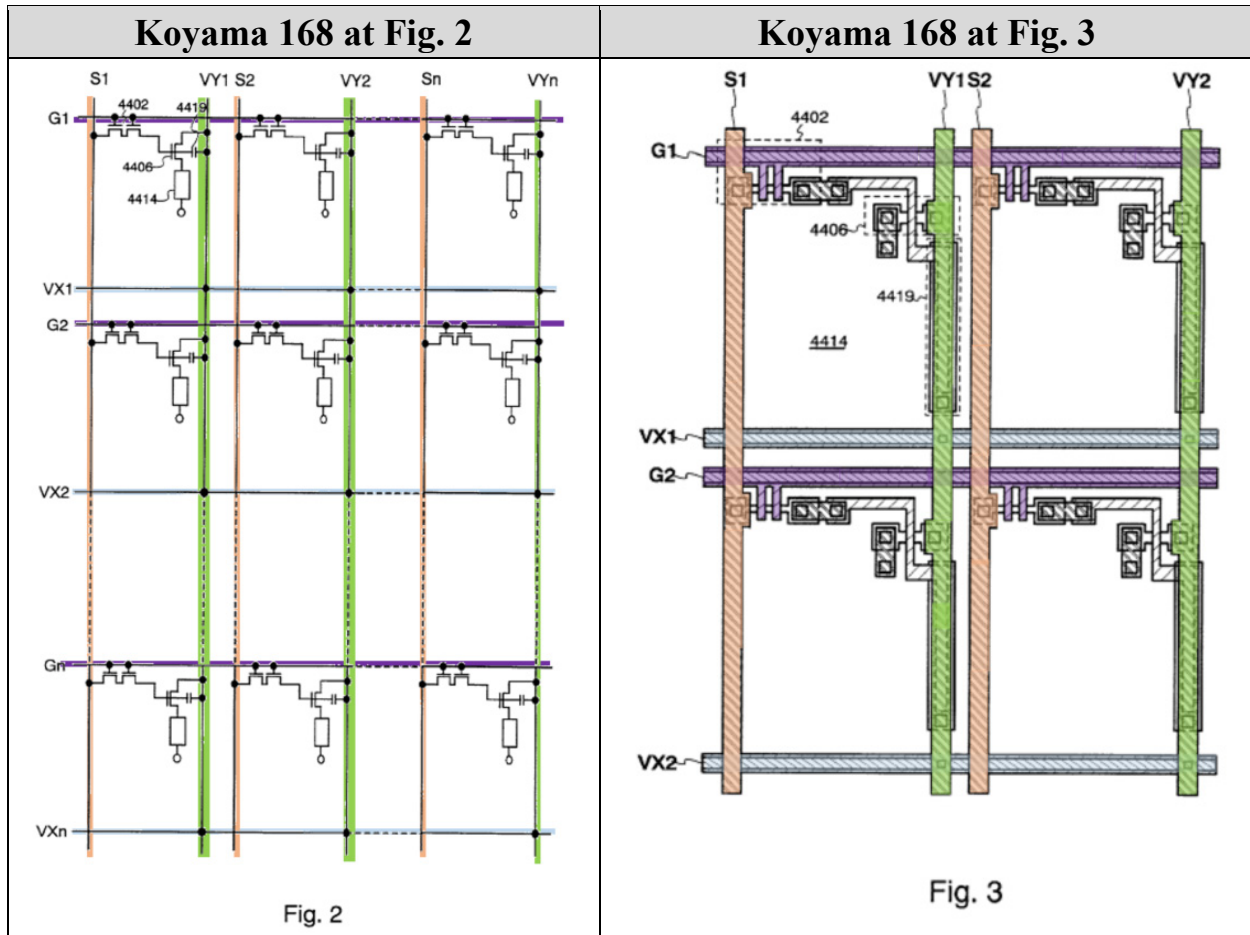
- (g) 1[g] a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line; and

The Koyama Combination renders obvious a “second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line.”

As discussed above with respect to Ground 1 Claim Element 1[g], a “power line,” in the context of the ’267 patent, supplies “driving voltages” to light-emitting elements. *See supra* Section III.A.2.g (discussing EX-1001 at 3:6-11, 4:7-9, 7:56-61, 9:5-11, Fig. 5).

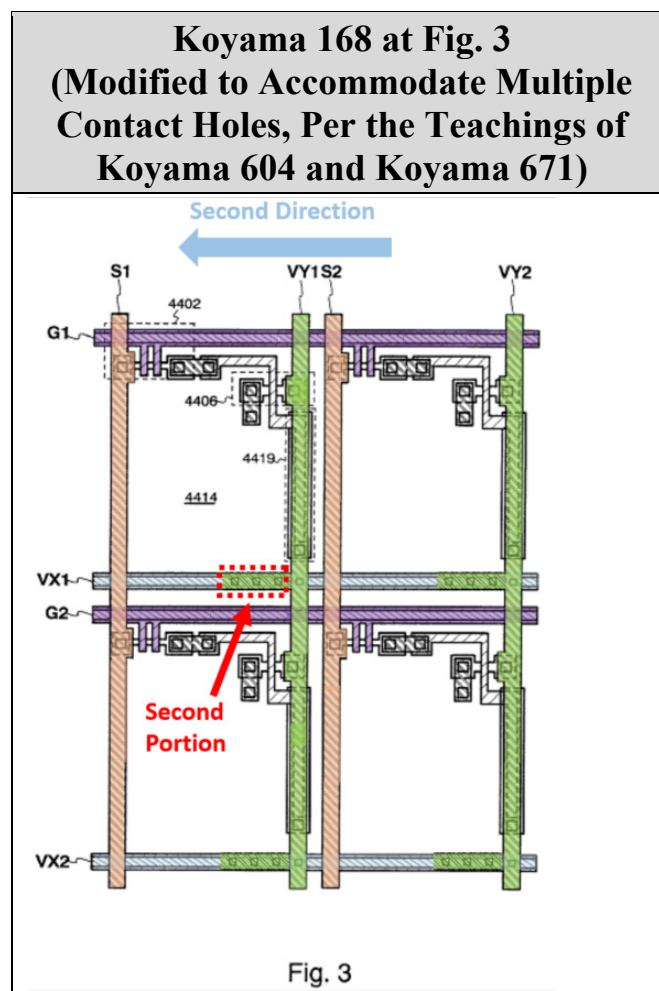
Koyama 168 discloses a “second power line.” Koyama 168’s Figure 3 is a “top view” corresponding to “Embodiment 2” of the invention, and it features “power supply lines VX1 and VX2 . . . connected through contact holes to conventional power supply lines VY1 and VY2.” *Id.* at [0159]-[0162]. These power lines distribute power to EL elements 4414. *See id.* at [0042]-[0044].

The power supply VX1, for example, constitutes a “second power line.” Figures 2 and 3 are reproduced below and highlight VX1 in blue.



The Koyama Combination renders obvious that the second power line extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line. As explained above, the Koyama Combination features Koyama 168's circuitry except that the vertical "VY" power lines feature protrusions to accommodate multiple contact holes that connect to the horizontal "VX" power lines. *See supra* Section III.B.4-5 (citing, e.g., EX-1010 at [0002], [0149]; EX-1011 at 6:16-23, 16:25-30, Fig. 1C, EX-1012 at [0002],

[0004], Fig. 13). As shown in the annotated version of Koyama 168 Fig. 3 reproduced below, each added protrusion of the vertical power lines constitute a “second portion” that extends in the same “second direction” as the second power lines. Moreover, the second power line would have overlapped with the second portion because it would need to be topographically under that portion in order to make electrical contact through contact holes. See EX-1006, ¶¶ 143-148.



For these reasons, the Koyama Combination discloses and renders obvious a

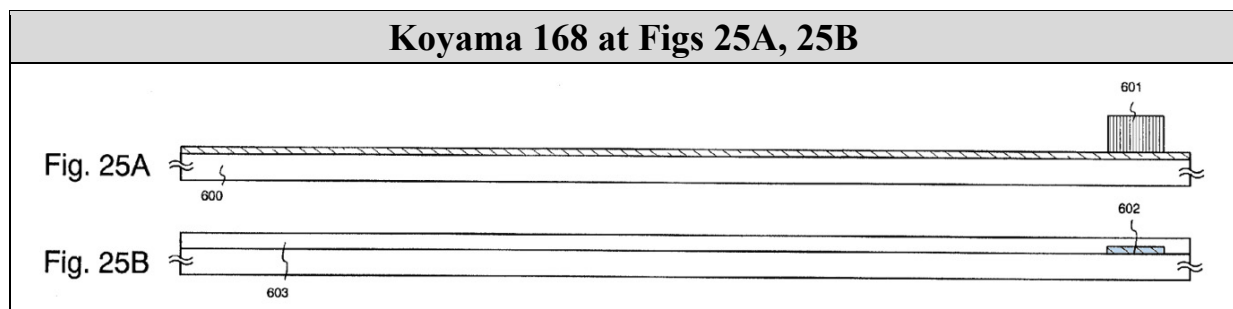
second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line. *See* EX-1006, ¶¶ 143-148.

- (h) 1[h] an inter-layer insulating film that is disposed between the first power line and the second power line,

The Koyama Combination renders obvious an “inter-layer insulating film that is disposed between the first power line and the second power line.”

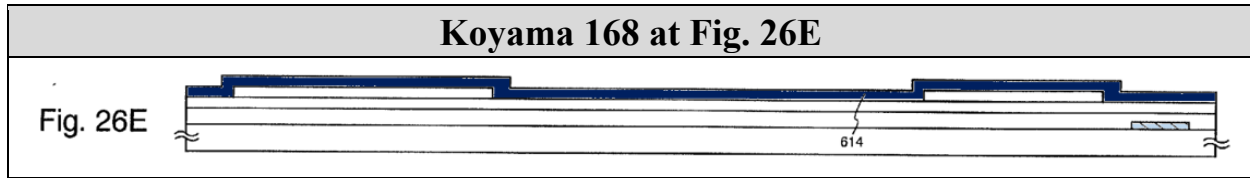
Koyama 168, as a general matter, uses inter-layer insulating films to electrically isolate different layers from each other. For example, Koyama 168 discloses a series of cross sectional views of an EL device corresponding to different snapshots in the process of building this device. Different interlayer insulating films are deposited at different steps of the process. *See* EX-1006, ¶¶ 151-157.

Figures 25A and 25B, for example, show formation of “power supply line 602.” *See* EX-1010 at [0348]. The table below shows this power supply line in pale blue.

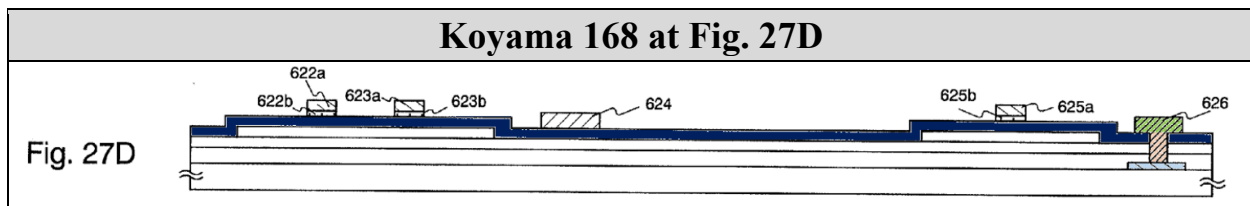


Above that power supply line is deposited a “gate insulating film 614.” *See*

EX-1010 at [0359]. The gate insulating film is shown in dark blue in the table below.

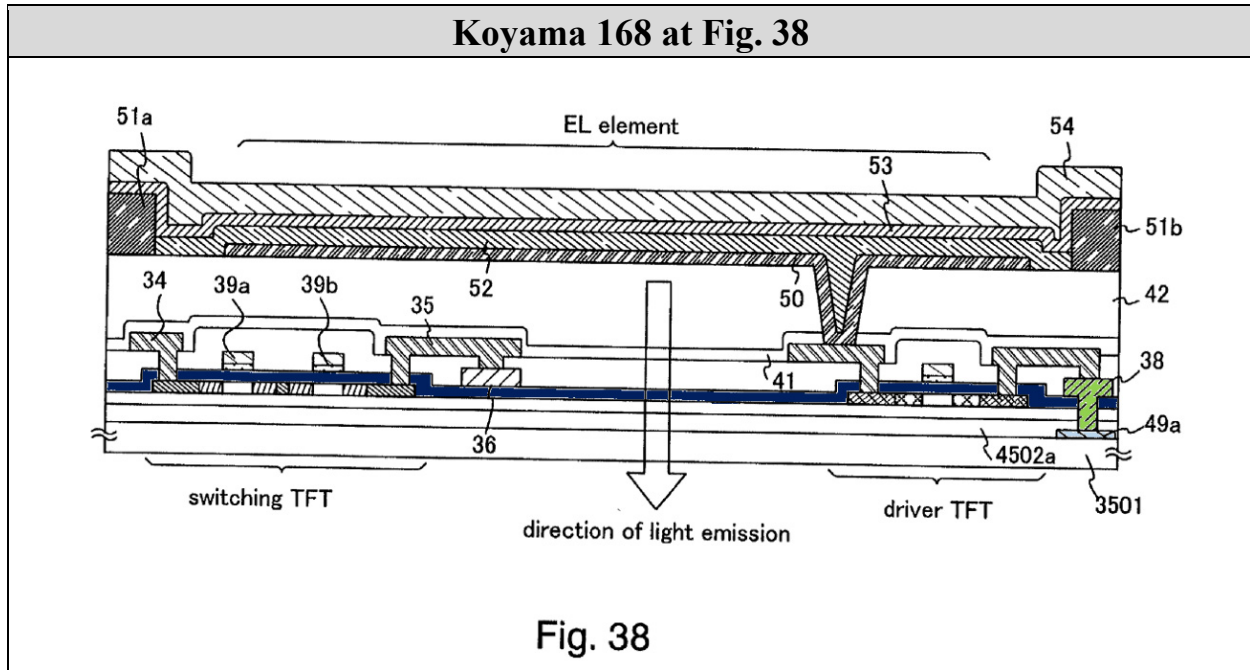


Above that gate insulating film 614 is deposited a “conductive film” that is patterned to form the “power source electrode 626.” *See id.* at [0359], [0366]. It electrically connects to the power supply line 602 below it via a contact hole. The power source electrode is shown in green in the table below, and the contact hole that connects it to the power supply line 602 is shown in pale red.



The power supply line 602, the gate insulating film 614, and the power source electrode 626 are also shown in figure 38, which represents an end product of the manufacturing process described in figures 25-27. In this figure, elements 38 (highlighted in green) and 49a (highlighted in blue) each represent “power supply lines.” *See* EX-1010 at [0219] (identifying power supply line 38), [0338]-[0341] (identifying power supply line 49a and characterizing the figure as the “pixel structure” of Embodiment 2, which corresponds to figure 3 discussed in

prior claim limitations). In between these power supply lines is an inter-layer insulating film (highlighted in dark blue) corresponding to Figures 26-27, as discussed above. *See* EX-1006, ¶ 153.



The “power supply line 38” / “power source electrode 626” (shown in green in figures above) corresponds to the VY vertical power supply lines (i.e., the “first power line”). This follows because this element is connected to the source or drain of a driver TFT, which is how the VY power supply lines connect in figure 3. *See* EX-1006, ¶¶ 150-157; EX-1010 at Figs. 2, 3, [0149], [0162]. The “power supply line 602” / “power supply 49a” (shown in pale blue in figures above) corresponds to the VX horizontal power lines (i.e., the “second power line”). This follows because this element is connected to the VY power supply line. *See id.*

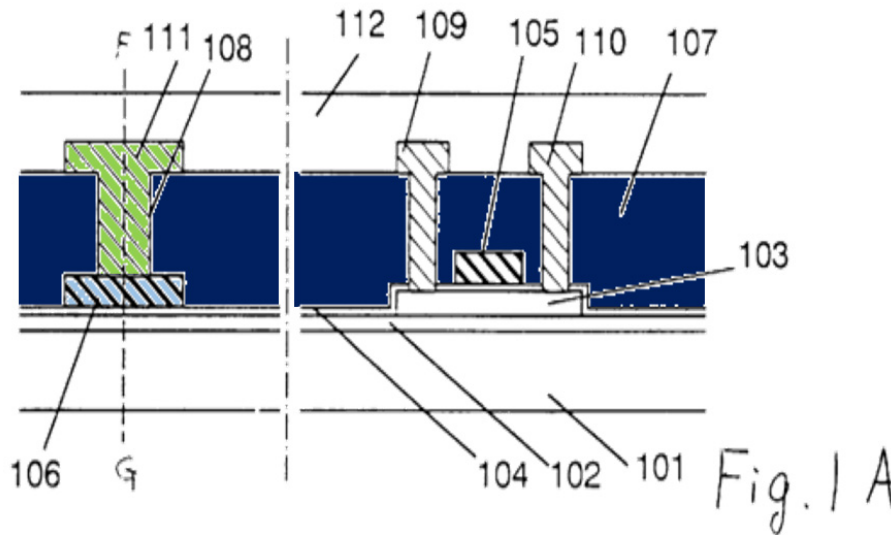
The “gate insulating film 614,”⁶ which is disposed between vertical (i.e., “first”) and horizontal (i.e., “second”) power supply lines constitutes an inter-layer insulating film. Because it is formed between those power supply lines, which are at different layers, it is “inter-layer.” As stated in the name, it is “insulating” because it insulates the layers above it from the layers below it. And as also stated in the name, it is a “film” because it is formed as a thin region that cover another region. *See* EX-1006, ¶¶ 150-157.

Koyama 604 and Koyama 671 also demonstrate that using inter-layer insulating films between power lines would have been obvious to a POSITA. *See* EX-1006, ¶¶ 158-161.

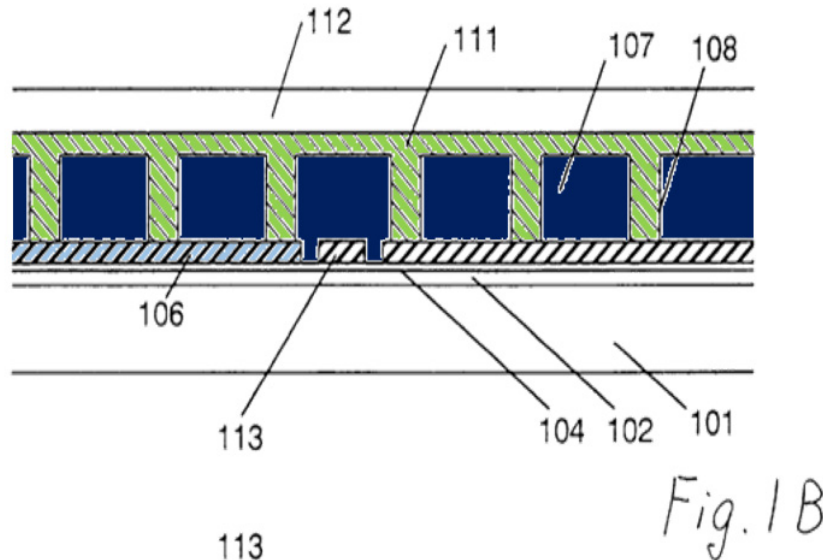
Koyama 604 discloses a “wiring line 111” that connects “in parallel to an auxiliary wiring line 106 via a plurality of contact holes 108 that are formed through the interlayer insulating film 107.” EX-1011 at 5:55-58; *see also id.* at 5:59-67. Koyama 604’s figures 1A and 1B illustrate this film. *See id.* at 5:43-7:49.

⁶ The layers below the gate insulating film 614—silicon nitride oxide films 603 and 604—also constitute inter-layer insulating films for the same reasons. *See* EX-1010 at [0349]; EX-1006, ¶ 157.

Koyama 604 at Fig. 1A

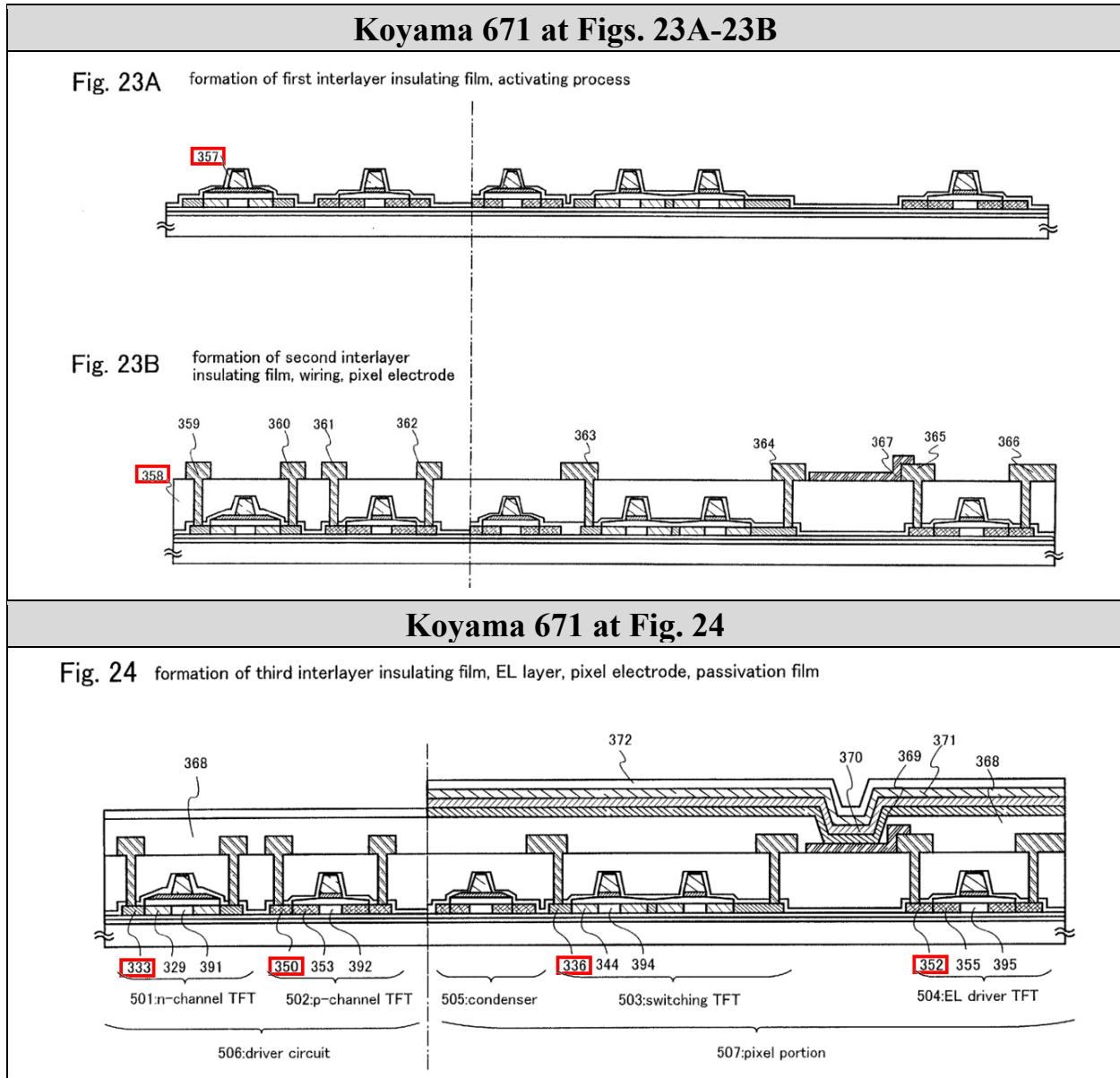


Koyama 604 at Fig. 1B
(Sectional View Taken Along Line F to G)



Likewise, Koyama 671's figures 23A and 23B show "a first interlayer insulating film" 357 and a "second interlayer insulating film" 358 disposed between the layers connected by the contact holes (which correspond to the vertical pillars shown in figure 24). *See* EX-1012 at [0224]-[0235]. The numbers calling out the

first and second interlayer insulating films and the impurity regions at the bottom of the contact holes are identified by red boxes in the reproduced figures in the table below.



It would have been obvious to a POSITA to use the inter-layer insulating films taught by Koyama 604 or Koyama 671 between the first and second power

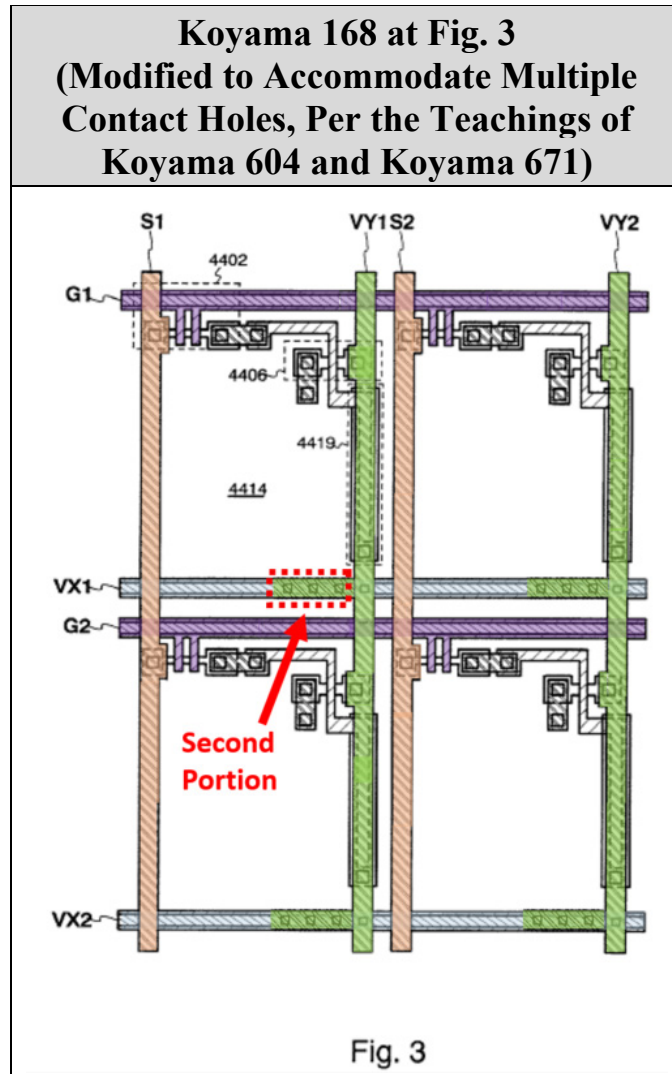
lines taught by Koyama 168. As shown in Koyama 168's figure 3, these first and second power lines are made to electrically connect to one another at only specific areas. *See, e.g.*, EX-1010 at [0379] (discussing contact holes "formed with respect to the first interlayer insulating film"). As shown in Koyama 168's figure 38, these two power lines can be deposited at different layers. A POSITA would recognize that Koyama 604's and Koyama 671's inter-layer insulating films could be used inbetween Koyama 168's power lines to insulate those power lines (being at different layers) while also being capable of being penetrated by a contact hole where necessary to make a connection. A POSITA would have had a reasonable expectation of success in making the proposed combination since all three references teach the use of inter-layer insulating films to electrically isolate different layers.

For these reasons, the Koyama Combination discloses and renders obvious an inter-layer insulating film that is disposed between the first power line and the second power line. EX-1006, ¶¶ 149-161.

- (i) 1[i] the second portion of the first power line being electrically connected to the second power line through plurality of contact holes.

The Koyama Combination renders obvious "the second portion of the first power line being electrically connected to the second power line through plurality of contact holes."

As explained above, the Koyama Combination features Koyama 168's circuitry except that the vertical "VY" power lines feature protrusions to accommodate multiple contact holes that connect to the horizontal "VX" power lines. *See* EX-1010 at [0162] ("The power supply lines VX1 and VX2 are connected through contact holes to conventional power supply lines VY1 and VY2"), [0379]; *supra* Section III.B.4-5 (citing, e.g., EX-1010 at [0002], [0149]; EX-1011 at 6:16-23, 16:25-30, Fig. 1C, EX-1012 at [0002], [0004], Fig. 13); Section III.B.6.h (showing that, as depicted in figure 38, first power line electrically connects to second power through contact hole). As shown in the annotated version of Koyama 168 Fig. 3 reproduced below, each added protrusion of the vertical power lines constitute a "second portion" allows multiple contact holes to electrically connect the vertical power lines to the horizontal power lines.



For these reasons, the Koyama Combination discloses and renders obvious the second portion of the first power line being electrically connected to the second power line through plurality of contact holes. EX-1006, ¶¶ 143-148.

IV. DISCRETIONARY CONSIDERATIONS

The *Fintiv* factors strongly favor institution.

1. No evidence regarding a stay

No motion to stay has been filed, so the Board should not infer the outcome and this factor is neutral.

2. Parallel proceeding trial date

The expected date for an Institution Decision is in October 2023 and the expected date for a Final Written Decision is in October 2024, within a few months of trial. As of this petition, the operative docket control order sets jury selection to begin on May 20, 2024. EX-1016.

Trial will likely be significantly delayed from that date. The median time from filing to trial in the Eastern District of Texas is ordinarily 24.5 months, and that estimate applied to this case would suggest trial to take place in April 2024 since the Patent Owner filed the complaint on April 18, 2022. *See* EX-1015; https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf at 35.

Here, however, the Patent Owner did not *serve* the complaint on Petitioner until about five months later, on September 27, 2022. The normal deadlines in the case have had concomitant delays. For example, this case's docket control order, which sets various case deadlines, did not issue until February 3, 2023—about ten months after the answer was filed. *See* EX-1016. With Patent Owner's delay in service of the complaint causing significant delay in the schedule, the median time

to trial should be judged from the date of complaint service (e.g., when the case actually started), instead of the date of complaint filing. Using the service date, the median time to trial would place trial in October 2024 shortly after or around the same time as the expected Final Written Decision deadline. Thus, Factor 2 weighs in favor of institution.

3. Investment in parallel proceeding

The co-pending litigation is in its early stages, and investment has been minimal. Claim construction has not occurred; fact discovery will not close until December 1, 2023; expert discovery has not begun and will not close until February 5, 2024. EX-1016. Thus, Factor 3 weighs in favor of institution.

4. Overlapping issues

If the Board institutes trial, Petitioner will cease asserting in the district court any invalidity contention based on the prior art presented in this petition that constitutes part of a ground. Institution will not result in overlapping consideration of invalidity arguments, thereby favoring institution.

5. Petitioner status

Petitioner is a defendant, but that is true of most Petitioners and this factor should not be a basis for denying institution.

6. Other circumstances

The merits of Petitioner's arguments are strong. Indeed, the present petition presents a compelling case of invalidity that supports institution, regardless of the status of the parallel proceeding. Thus, the *Fintiv* factors favor institution.

V. FEES

Petitioner authorizes charge of fees to Deposit Account No. 06-1050.

VI. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., Ltd., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. are the real parties-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioners are not aware of any disclaimers, reexamination certificates or petitions for *inter partes* review for the '267 Patent. The '267 patent is the subject of the following civil action: *Element Capital Commercial Company PTE. Ltd., v. BOE Technology Group Co., et al*, 2:22-cv-00118-JRG (E.D. Tex.).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioners provide the following designation of counsel.

Lead Counsel	Backup counsel
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D. Service Information

Please address correspondence/service to the above-listed address. Petitioner consents to email service at IPR54108-0001IP2@fr.com (referencing No. 54108-0001IP2) and cc'ing PTABInbound@fr.com.

Respectfully submitted,

Dated April 6, 2023

/Jeremy J. Monaldo/

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Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,994 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated April 6, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on April 6, 2023, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via Priority Mail Express, to the Patent Owner, by serving the correspondence address of record as follows:

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