

**UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

BOE TECHNOLOGY GROUP CO., LTD.,
BEIJING BOE DISPLAY TECHNOLOGY CO., AND
MOTOROLA (WUHAN) MOBILITY TECHNOLOGIES
COMMUNICATION CO., LTD.,
Petitioner

v.

ELEMENT CAPITAL COMMERCIAL COMPANY PTE. LTD,
Patent Owner.

IPR2023-00808
U.S. PATENT NO. 8,164,267

DECLARATION OF DR. ARIS SILZARS

Declaration

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: 
Aris Silzars, Ph.D.

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I, Dr. Aris Silzars, do hereby declare:

1. I am making this declaration at the request of Element Capital Commercial Company PTE. LTD in the matter of the BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd., petition for *inter partes* review of IPR2023-00808.

2. I am being compensated for my work in this matter at my standard hourly rate of \$350 for consulting services. My compensation in no way depends on the outcome of this proceeding or the content of my testimony.

3. In preparing this Declaration, I considered the following materials:

- (a) U.S. Patent No. 8,164,267 (“ the ’267 Patent”) (EX-1001);
- (b) Excerpts of the Prosecution History of Japanese Application No. 2002-293696 (EX-1002);
- (c) Certified Translation of Excerpts from the Prosecution History of Japanese Application No. 2002-293696 (EX-1003);
- (d) The Prosecution History of U.S. Application No. 10/676,067 (EX-1004);
- (e) The Prosecution History of U.S. Application No. 12/219,592 (EX-1005);

- (f) Declaration of DR. David K. Liu (EX-1006);
- (g) U.S. Patent No. 6,825,820 (EX-1007);
- (h) U.S. Patent Application Publication No. 2001/0015618
("Yamazaki") (EX-1008);
- (i) U.S. Patent No. 6,894,431 (EX-1009);
- (j) U.S. Patent Application Publication No. 2001/0043168
("Koyama 168") (EX-1010);
- (k) U.S. Patent No. 6,124,604 ("Koyama 604") (EX-1011);
- (l) U.S. Patent Application Publication No. 2002/0053671
("Koyama 671") (EX-1012);
- (m) Fabrice Caignet et al, "The Challenge of Signal Integrity in
Deep-Submicrometer CMOS Technology," 89 Proceedings of
the IEEE, No. 4 (April 2001) (EX-1013);
- (n) Sarma et al., "Flat Panel Displays for Portable Systems," 13
Journal of VLSI Signal Processing Systems 165-190 (1996) (EX-
1014);
- (o) Paul Horowitz et al., "The Art of Electronics", Second Edition
(EX-1017);
- (p) U.S. Patent No. 6,858,991 (EX-1018);

- (q) U.S. Patent Application Publication No. 2003/0076046 (EX-1019);
- (r) U.S. Patent No. 6,633,135 (EX-1020);
- (s) The Petition filed by the Petitioners;
- (t) Achintya K. Bhowmik et al. , “Mobile Displays: Technology and Applications,” 404, 406, 408-410 (2008) (EX-2009);
- (u) Francis W. Sears, “Electricity and Magnetism,” 91-93 (1958) (EX-2010);
- (v) Jun. Souk et al., “Flat Panel Display Manufacturing,” 13-14 (2018) (EX-2011);
- (w) Larry Lynch et al., “Electronic Materials Handbook,” 538-540, 552 (1989) (EX-2012);
- (x) Paul Horowitz et al., “The Art of Electronics,” 830 and 833-836 (1989) (EX-2013)
- (y) Shunsuke Kobayashi et al., “LCD Backlights,” 14-15 (2009) (EX-2014);
- (z) Jiun-Haw Lee et al., “Introduction to Flat Panel Displays,” 78-79 and 212-213 (2008) (EX-2015); and

(aa) Amal Ghosh et al., “Fundamentals of OLEDs,” s-1/80 (2004)
(EX-2016)

I. Professional Background

4. Information concerning my professional qualifications, experience, and publications, and the matters in which I have served as an expert, are set forth in my current curriculum vitae (EX-2002).

5. I received my Bachelor of Arts degree in Physics in 1963 from Reed College in Portland, Oregon. I received my Master of Arts degree in Physics in 1965 from the University of Utah. I received my Doctoral degree in Electrical Engineering in 1969 from the University of Utah.

6. I have been an active participant in the development of display device technologies and products that use displays since 1974. I have managed research groups as large as 350 technologists in creating and implementing display device technologies and high performance electronic circuits into products based on these technologies.

7. I have participated in numerous technical conference activities (including Program and General Chair of the International Society for Information Display symposium – the preeminent annual international conference on display

technology) and made numerous presentations on display applications and on the technology evolution of those products. I was President of the Society for Information Display (“SID”) from 2000 to 2002. With over 7000 members, SID is the premier organization for professionals and academics in the fields of display research, design, manufacturing, applications, standards development, and marketing.

8. Since 1995, I have been an independent industry consultant with a broad client base and continue to be active and knowledgeable regarding all new display device-related technologies. My area of expertise encompasses the fields of information display technology, liquid crystal, OLED, and LED displays, digital integrated circuits and systems, mechanical design, and packaging for electronic products and semiconductor technology.

9. I have authored over 100 publications, most related to display device technology. I am also a named inventor on fifteen patents, most of which are related to or in the field of display device technology. In my many years of engineering, manufacturing, and product development experience, I have personally been involved in the design of large segmented LED displays, including obtaining two patents on which I am a co-inventor.

II. Background Technologies

10. Below I describe the state of display device technology as of the '267 Patent's filing date, and summarize the development of technologies underlying the features recited in claim 1 of the '267 Patent, and the features disclosed in Yamazaki, Koyama 168, Koyama 604, and Koyama 671.

11. At the time of the invention of the '267 Patent, display devices contained various types of components, including (1) semiconductor devices such as circuits formed by thin film transistors (TFTs) utilized for controlling the operation of the display devices, and (2) wirings such as power lines, data lines, and scan lines for transmitting signals to the semiconductor devices and/or the pixels. EX-1001 at 1:30-47; EX-1008 at [0007]; EX-1010 at [0004]; EX-2009 at 408-410. The operations of the semiconductor devices and the wirings are two distinct aspects in display devices, and the configurations associated therewith greatly differ.

12. The wirings in the display devices are conductors that exhibit resistance, which in turn cause voltage drop as the wirings get farther from the source. EX-1006 at 22. The resistance in a wiring, such as a power line, may be affected by several factors. For example, the wiring resistance is directly proportional to the length of the wiring. EX-2010 at 91-93. That is, the longer the length of the power supply line, the higher the wiring resistance in the power supply line. EX-1008 at

[0005]-[0006], [0011]; EX-1010 at [0032]-[0036], [0138], [0140], [0156]; EX-2010 at 91-93.

13. In addition, the forming of wirings in the display devices can significantly differ depending on the type of substrates on which the wirings are formed. Generally, wirings (e.g., power lines, data lines, etc.) of display devices are formed on a substrate via thin-film deposition, which is a technique for depositing different layers of metal and semiconductor materials on the substrate to create circuitry and wirings thereon. EX-2011 at 13-14.

14. On the other hand, wirings on a hardened printed wiring board (PWB) (also known as printed circuit board (PCB)), are formed via board fabrication techniques, which are different from thin-film deposition. *See, e.g.*, EX-2012 at 538-540; EX-2013 at 830, 833-836. The wirings formed on the PWB/PCB have a structural configuration and thickness which are different from wirings formed via thin-film deposition.

15. In this regard, although it is possible to form wirings and circuitries on a hardened PWB/PCB via board fabrication techniques, board fabrication is not commonly utilized in display devices since it can only produce very limited pixel densities (i.e., resolution) and cannot provide the pixel densities required for panel displays of any size, from cell phone display devices to large screen televisions.

16. Further, at the time of the invention of the '267 Patent, there existed two distinct types of display devices based on the type of material utilized in the display devices to emit light: (1) liquid crystal display (LCD) devices, and (2) electroluminescent (EL) display devices. LCD devices and EL display devices are different in both structure and function, and the technologies and design methods used for one are substantially different from the other, as described in the following.

17. LCD devices use a liquid crystal to control the passage of light, and require a backlight (a lamp unit, etc.). EX-2014 at 14-15. EL display devices, on the other hand, use electroluminescent materials that emit light when an electric current is applied. In other words, the EL display devices are self-luminous and, unlike LCD devices, do not require a backlight. EX-1001 at 1:16-18; EX-1008 at [0004], [0092]. Furthermore, the pixels in LCD devices are voltage controlled whereas the pixels in EL display devices are current controlled. EX-2015 at 78-79, 212-213. In addition, the arrangement of the wirings in LCD devices is different from the arrangement of wirings in EL display devices. In LCD devices, the majority of power is used by the backlight, which is a separate component and is connected to its own power supply. Therefore, the LCD panel, itself, requires only a small fraction of the overall power needed to operate the display. EX-2014 at 14-15. Power lines in EL display devices, on the other hand, are formed adjacent to the

pixels/pixel matrix on the same substrate and are utilized to supply power or current to the pixels or pixel matrix to drive said pixels/pixel matrix. EX-1001 at 1:51-56, 1:63-2:2, 2:33-35, 2:41-42; EX-1008 at [0007], [0037]-[0038]; EX-1010 at [0013]-[0016]; EX-2016 at S-1/80.

18. In view of these differences, the technologies and design methods used for LCD display devices are substantially different from those of EL display devices.

19. Organic light-emitting diode (OLED) display devices are a type of EL display device. Specifically, OLED display devices include multiple OLED pixels formed by organic materials that emit light when an electric current is applied thereto. Thus, OLED display devices are self-emissive and do not require a backlight. EX-1001 at 1:16-29. An active-matrix OLED (AMOLED) display device is a specific type of OLED display device that uses an active-matrix backplane that includes an element such as a capacitor to control the OLED pixels. EX-2009 at 404, 406.

III. Relevant Legal Standards

20. I have been asked to provide my opinions as to whether claim 1 of the '267 Patent would have been anticipated and/or obvious to a person of ordinary skill in the art ("POSITA") at the time of the filing date of the '267 Patent.

21. I am an engineer by training and profession. The opinions I express in this declaration involve the application of my technical knowledge and experience to the evaluation of certain prior art with respect to the '267 Patent. In addition, I understand that the following legal principles apply.

22. It is my understanding that, in determining whether claims of the '267 Patent are anticipated or obvious in this proceeding, the claim terms are generally given their ordinary and customary meaning as understood by a POSITA. A POSITA would read the claim terms in the context of the entire patent specification in which they appear, as well as the prosecution history of the patent.

23. It is my understanding that a claim is anticipated under 35 U.S.C. § 102 if each and every element and limitation of the claim is found, either expressly or inherently, in a single prior art reference. I also understand that a reference must disclose all claimed elements as arranged in the claim, although identical terminology need not be used in the reference and claim elements.

24. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a POSITA in the art at the time of the alleged invention. I also understand that an obviousness analysis takes into account the scope and content of the prior art, the differences

between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

25. In determining the scope and content of the prior art, it is my understanding that a reference is considered relevant prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

26. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment involves showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

27. It is my further understanding that several rationales may be applied for combining references or modifying a reference to show obviousness of claimed

subject matter. These rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify a prior art reference or to combine prior art teachings to arrive at the claimed invention.

IV. Person of Ordinary Skill in the Art

28. It is my understanding that when interpreting the claims of the '267 Patent I must do so based on the perspective of one of ordinary skill in the art at the relevant priority date. My understanding is that the earliest claimed priority date of the '267 Patent is October 7, 2002.

29. It is my opinion that one of ordinary skill in the art in the field of display device technology in the 2002 time period, would have had at least a Master's degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of display device technology. Additional education can remedy lack of work experience and vice versa.

30. I am a person of at least ordinary skill in the art and was so at the time of the invention of the '267 Patent.

V. Overview Of The Subject U.S. Patent No. 8,164,267

31. The '267 Patent was assigned to Seiko Epson Corporation, and the inventors of the '267 Patent are Yojiro Matsueda and Hayato Nakanishi. The patent is titled "Electro-Optical Device, Matrix Substrate, and Electronic Apparatus."

32. The '267 Patent is directed to an electro-optical device that is an active-matrix organic light-emitting diode ("OLED") display device. EX-1001 at 4:49-51. In particular, the '267 Patent provides a wiring method for electric power lines disposed adjacent to a pixel matrix or pixels that allows the aperture ratio of the pixel to be increased while maintaining a pixel matrix with the same pixel pitch. EX-1001 at 2:11-13.

33. As described in the "SUMMARY OF THE INVENTION" section of the '267 Patent, a light-emission layer of an active-matrix OLED display device may be formed of a material corresponding to each color of the RGB (i.e., red, green, and blue). EX-1001 at 1:21-29, 1:45-46, 1:51-56. The display device is operated with greatly different power consumptions corresponding to each color, and thus the power lines associated with different pixels of different colors may have different widths in order to accommodate the different power consumptions. EX-1001 at

1:30-39, 1:51-56. Accordingly, in conventional wiring layouts, “it is difficult to maintain a large aperture ratio [for the pixels] while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.” EX-1001 1:56-2:9. Example relevant portions of the '267 Patent are reproduced below:

With conventional color-display active-matrix-driven display panels, an M number each of electric power lines and data lines are disposed in the column direction on a pixel matrix with an N number of columns and an M number of rows formed on a pixel region, as well as an N number of selection lines being disposed in the row direction on the aforementioned matrix. With a given pixel of such a wiring layout, a data line is disposed between the given pixel and the left-adjacent pixel, and an electric power line is disposed between the given pixel and the right-adjacent pixel.

EX-1001 at 1:30-39.

With the conventional arrangements, a light-emission layer is formed of a material corresponding to each color of the RGB three primary

colors, and accordingly, the organic EL device is operated with greatly different power consumption corresponding to each color, so the optimal width of the electric power line is greatly different for each color.

EX-1001 at 1:51-56.

Accordingly, with the above-described wiring layout, while there is the need to determine the pixel pitch according to the maximal width for disposing the electric power lines, there is the need to form a pixel matrix with the same pixel pitch due to the restriction from the manufacturing process for a display, and accordingly, there is the need to determine the pixel layout at the sacrifice of the aperture ratio.

EX-1001 at 1:56-63.

On the other hand, in the event of reducing the aperture ratio, there is the need to increase the amount of electric current supplied to the organic EL device for obtaining predetermined luminance, and accordingly, there is the need to form the electric power line with a

greater width, leading to further reduction of the aperture ratio from the above-described reason.

EX-1001 at 1:63-2:2.

As described above, with the conventional wiring layout, the width of the electric line and the aperture ratio of the pixel are in the relation of trade off each other, and it is difficult to maintain a large aperture ratio while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.

EX-1001 at 2:3-9.

34. In order to solve these problems, the '267 Patent provides a novel wiring method for electric power lines that supply power to pixels in OLED display devices. EX-1001 at 2:10-13. In an embodiment, the plurality of power lines include a first power line in a first direction (e.g., a column direction) of the pixel matrix and a second power line in a second direction (e.g., a row direction) of the pixel matrix, with the first power line electrically connected to the second power line through a plurality of contact holes. EX-1001 at 7:45-61, 8:51-54. Example relevant portions of the '267 Patent are reproduced below:

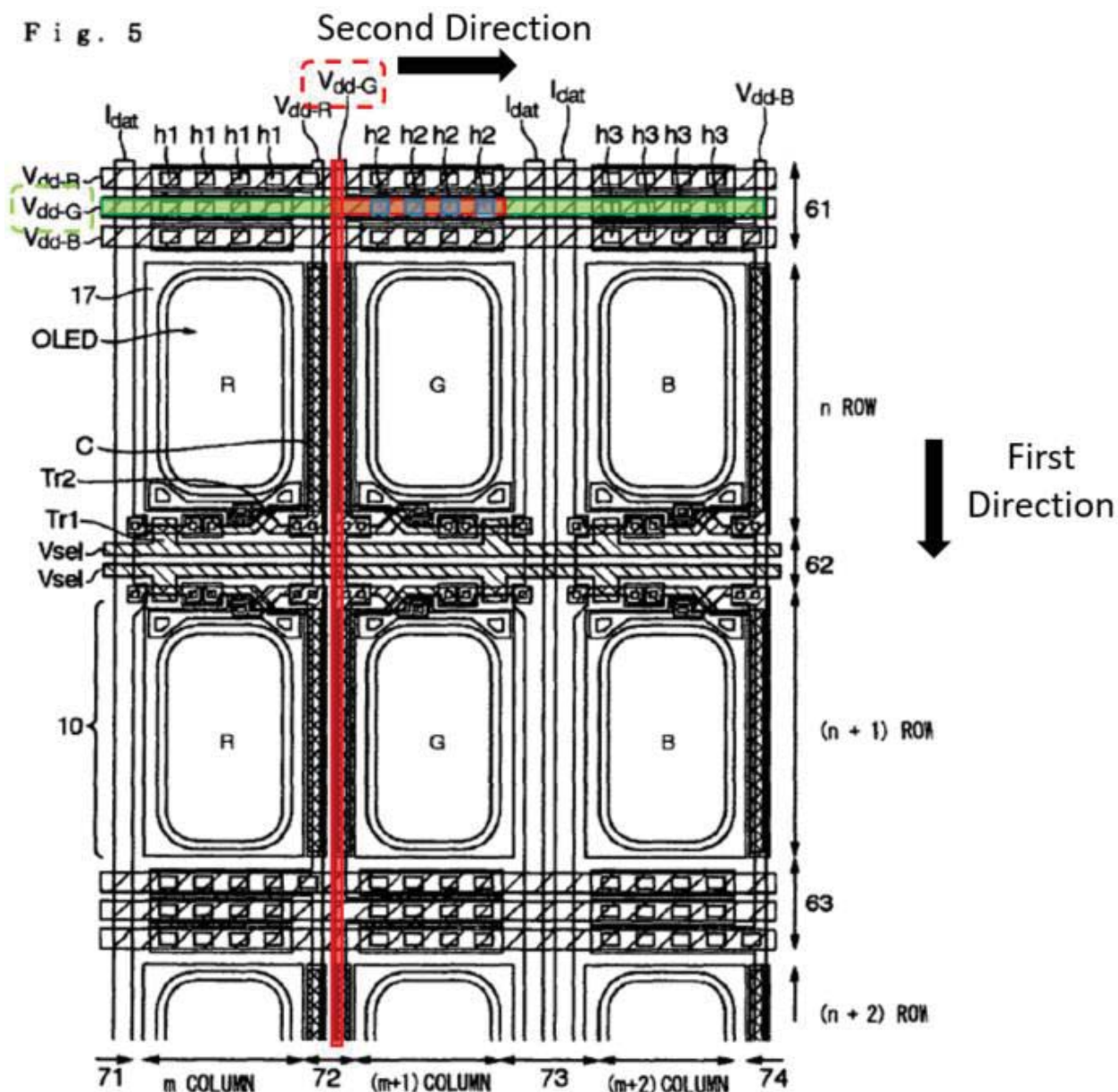
The electric power lines disposed in the column and row directions are formed in different layers, and are electrically connected with each other through the contact holes h1 formed on an inter-layer insulating film.

EX-1001 at 8:51-54.

In the same way, the electric power lines Vdd-G in the column and row directions, and the electric power lines Vdd-B in the column and row directions, are formed in different layers, and the electric power lines in the column and row directions are electrically connected with each other through the contact holes h2 and h3.

EX-1001 at 8:57-60.

35. Fig. 5 of the '267 patent, annotated below, shows an example of the first power line (annotated in red), the second power line (annotated in green), and contact holes (annotated in blue):



EX-1001at FIG. 5 (the '267 Patent) (annotated)

36. As can be seen above, a green pixel ('G' in FIG. 5) is provided with a first power line (annotated in red) and a second power line (annotated in green). The

first power line has a first portion extending in a first direction (intersecting the second power line) and a second portion extending in a second direction (parallel to the second power line) that intersects the first direction. The second power line (annotated in green) extends in the second direction and overlaps at least a part of the second portion of the first power line, which is electrically connected to the second power line through a plurality of contact holes ('h2' in FIG. 5; annotated in blue). EX-1001 at 8:51-64.

37. By this arrangement of overlapping portions of the power lines connected by plural contact holes, the inventors of the '267 patent recognized that wiring breakage can be prevented and wiring resistance in the power lines can be reduced. EX-1001 at 8:60-64. Further, the occurrence of non-uniformity of luminance due to insufficient current supply to a particular power line can be suppressed, and the occurrence of cross-talk can be reduced. EX-1001 at 9:5-14. Example relevant portions of the '267 Patent are reproduced below:

the present embodiment has the advantage of preventing wiring breakage, and furthermore has the advantage of reducing the wiring resistance.

EX-1001 at 8:61-64.

the electric power lines Vdd-G , Vdd-R , and Vdd-B are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines Vdd-G , Vdd-R , and Vdd-B can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, the occurrence of cross-talk can be reduced.

EX-1001 at 9:5-14.

VI. Summary of Alleged Prior Art

A. US Patent Application Publication No. 2001/0015618

38. US 2001/0015618 (“Yamazaki”) is a US patent application publication that published on August 23, 2001.

39. Yamazaki is directed to EL display devices that aim to provide homogenized quality of image. EX-1008 at [0014].

40. Specifically, Yamazaki recognizes that the homogeneity of the quality of the image reduces due to the voltage drop in the current supply line of an EL display device, which originates in increased wiring resistance due to the

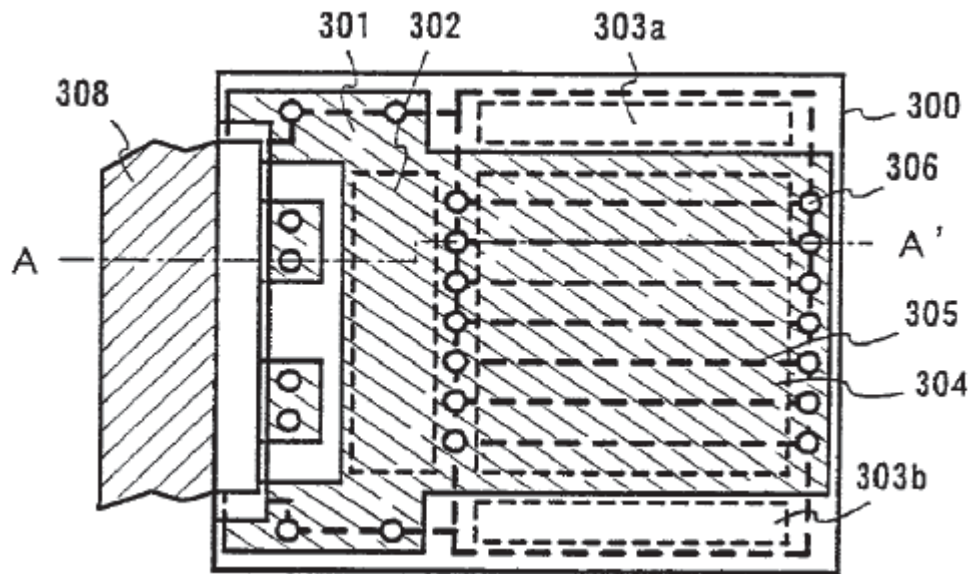
incremental length of current supply line across the EL display device. EX-1008 at [0005]-[0013], FIG. 2.

41. In order to solve this problem, Yamazaki provides EL display devices which are constituted of a first substrate, having a luminous element formed thereon, and a second substrate. EX-1008 at [0015]-[0016]. The second substrate is a hardened large printed wiring board (PWB) that has a level of hardness which does not bend or curve to some amount of impact. EX-1008 at [0016].

42. Yamazaki describes an “Embodiment Mode” for manufacturing an EL display device with reference to FIGS. 3A-3C. EX-1008 at [0035]-[0036]. FIGS. 3A-3B illustrate top views of the EL display device, and FIG. 3C illustrates a cross-sectional view taken along a cutout line “A-A” in FIGS. 3A-3B. EX-1008 at [0036].

43. Referring to FIG. 3A of Yamazaki, reproduced below, “wiring 301” for aiding a current supply line is formed on a first PWB 300. EX-1008 at [0038]. Specifically, the “wiring 301” is made of a low resistant material such as a copper foil, and is connected in parallel to the current supply line in order to reduce the apparent wiring resistance of the current supply line. EX-1008 at [0038]-[0039]. The “wiring 301” is connected to the current supply line via a contact portion 306. EX-1008 at [0038]-[0039]. Yamazaki suggests that the “wiring 301” can be described as “current supply auxiliary line,” in view of its role of aiding the current

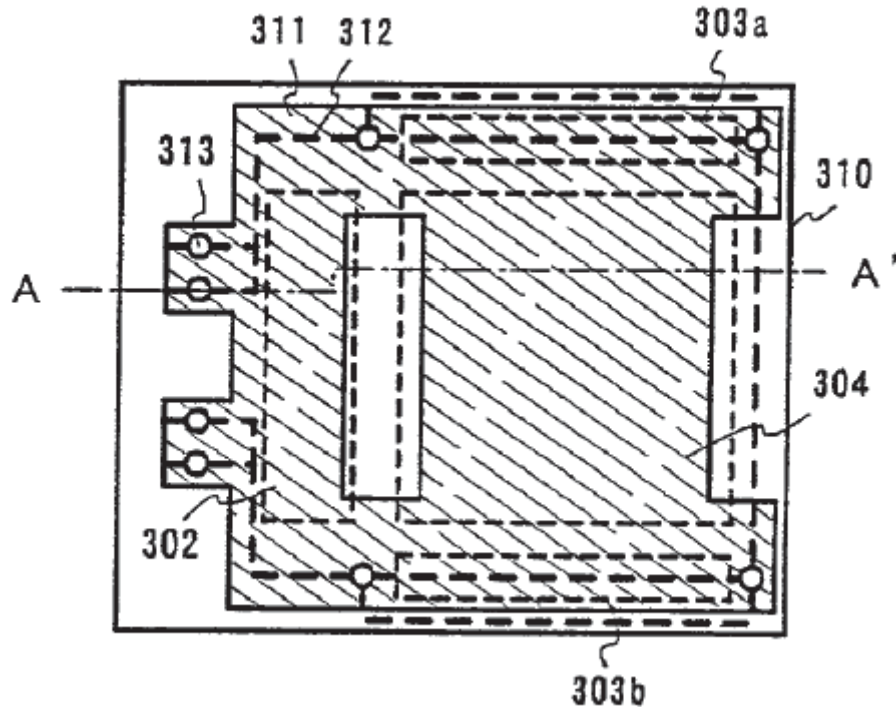
supply line *by reducing resistance* thereof. EX-1008 at [0037]. Yamazaki does not provide any further description on this wiring 301 or suggest that it supplies current to pixels.



EX-1008 (“Yamazaki”) at FIG. 3A

44. Similarly, referring to FIG. 3B of Yamazaki, reproduced below, a “wiring 311” for aiding a gate control wiring is formed on a second PWB 310. EX-1008 at [0040]. Specifically, the “wiring 311” is made of a low resistant material such as a copper foil, and is connected in parallel to the gate control wiring in order to reduce the apparent wiring resistance of the gate control wiring. EX-1008 at [0041]-[0042]. As with its description of the wiring 301, Yamazaki does not suggest any additional function of the wiring 311 beyond reducing the apparent wiring

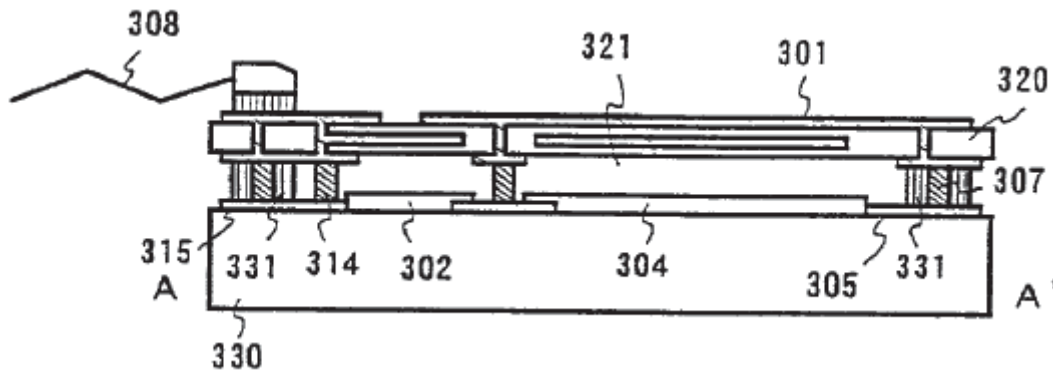
resistance of its corresponding line (the current supply line 305 for wiring 301, and the gate control wiring 312 for wiring 311).



EX-1008 (“Yamazaki”) at FIG. 3B

45. Yamazaki describes that the first PWB 310 and the second PWB 320 are first adhered to each other to form a PWB 320, and the adhered boards (i.e., PWB 320) are bonded with an element-formed substrate 330. EX-1008 at [0043]. The element-formed substrate 330 has a source driver circuit 302, gate driver circuits 303a-303b, a pixel portion 304, a current supply line 305, and a gate control wiring 312 formed thereon. EX-1008 at [0038], [0041]. FIG. 3C of Yamazaki, reproduced below, illustrates a cross-sectional view of the EL display device, with the PWB 320

(i.e., the PWB 300 and PWB 310 adhered together) bonded to the element-formed substrate 330.



EX-1008 (“Yamazaki”) at FIG. 3C

46. Notably, unlike the “current supply line 305,” Yamazaki does not describe or suggest that the “wiring 301” (i.e., the “current supply auxiliary line 301”) is utilized for providing current to the EL element in the pixel portion. Additionally, beyond its description that the “wiring 301” runs in parallel with the “current supply line 305”, Yamazaki provides no further disclosure of the layout or geometry of the “wiring 301”.

B. US Patent Application Publication No. 2001/0043168

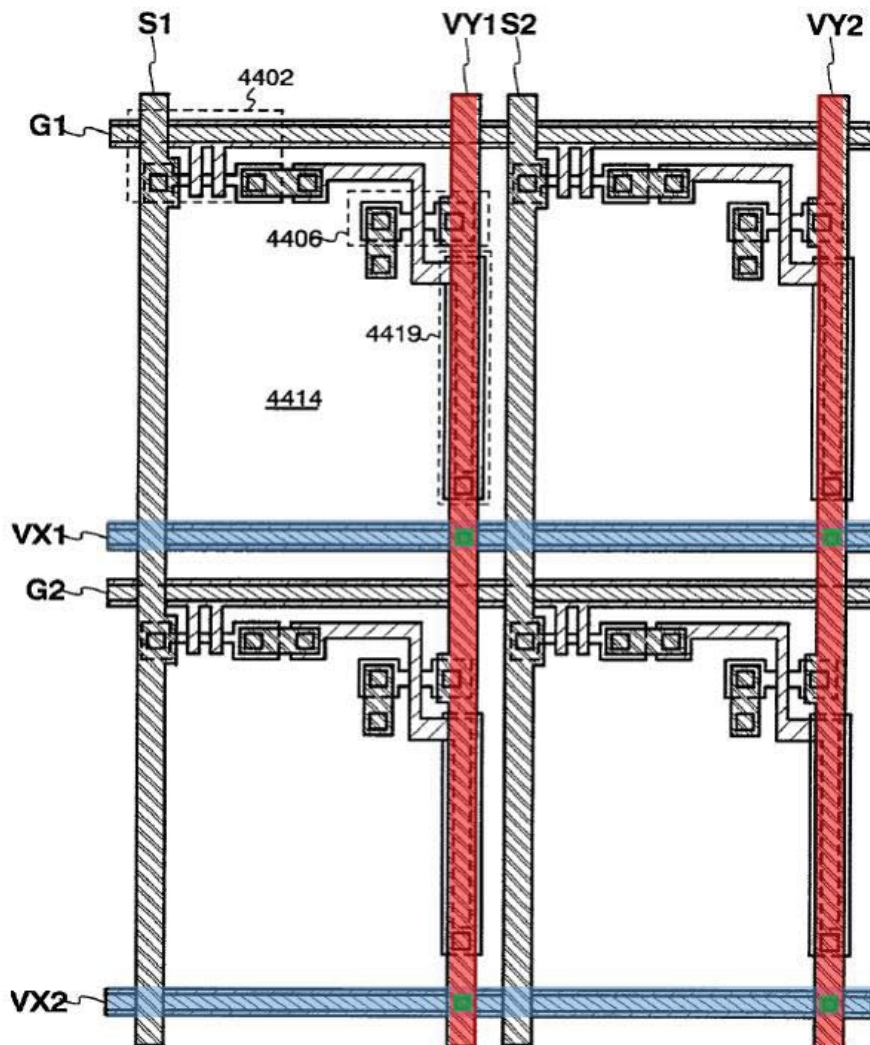
47. US 2001/0043168 (“Koyama 168”) is a US patent application publication that published on November 22, 2001.

48. Koyama 168 is directed to active-matrix OLED display devices that aim to alleviate potential drop due to wiring resistance of a power supply line. EX-1010 at [0053]. Specifically, Koyama 168 recognizes the problem of electrical potential drop caused by wiring resistance due to the length and the position of the power supply line. EX-1010 at [0032]-[0036], [0044]-[0050], FIG. 23, FIG. 35, and FIG. 41.

49. In order to solve this problem, Koyama 168 explains that it is necessary to make the wirings as short as possible. EX-1010 at [0156]. Specifically, Koyama 168 discloses a configuration to reduce the length of the power supply lines of a pixel portion in order to reduce the influence of potential drop. EX-1010 at [0137]-[0140]. In this regard, Koyama 168 provides a small number of power supply lines collected together in one unit, and connected to an external input terminal through a driver region. EX-1010 at [0156]-[0157]. Koyama 168 describes that such a configuration reduces the length of wirings of the power supply lines and, as a result, decreases the wiring resistance and the influence of potential drop around the pixel portion. EX-1010 at [0138], [0140], [0156]-[0157].

50. Further, Koyama 168 provides additional power supply lines in parallel to the gate signal lines in a wiring layer forming the gate signal lines, so as to form a matrix-like arrangement of power supply lines. EX-1010 at [0163]-[0164].

As shown in FIG. 3, reproduced below, Koyama 168 provides the additional power supply lines VX1 and VX2 (annotated in blue below) extending in one direction and connected to respective the power supply lines VY1 and VY2 (annotated in red below) via a contact hole (annotated in green below). EX-1010, [0162], FIG. 3.



EX-1010 (“Koyama 168”) at FIG. 3 (annotated)

51. Notably, as shown above, Koyama 168 indicates that the power supply lines VX1/VX2 and the power supply lines VY1/VY2 are connected by only one contact hole each. Further, FIG. 3 of Koyama 168 illustrates that the contact hole is formed on the overlapping portion of the power supply lines VX1/VX2 and power supply lines VY1/VY2, which extend in only one direction. It can therefore be understood that Koyama 168 uses only one contact hole because the power supply lines VX1/VX2 are perpendicular to the power supply lines VY1/VY2, and the overlapping portion of the power supply lines VX1/VX2 and power supply lines VY1/VY2 is only sufficient to accommodate one contact hole.

C. US Patent No. 6,124,604

52. US Patent No. 6,124,604 (“Koyama 604”) is a US patent that issued on September 26, 2000.

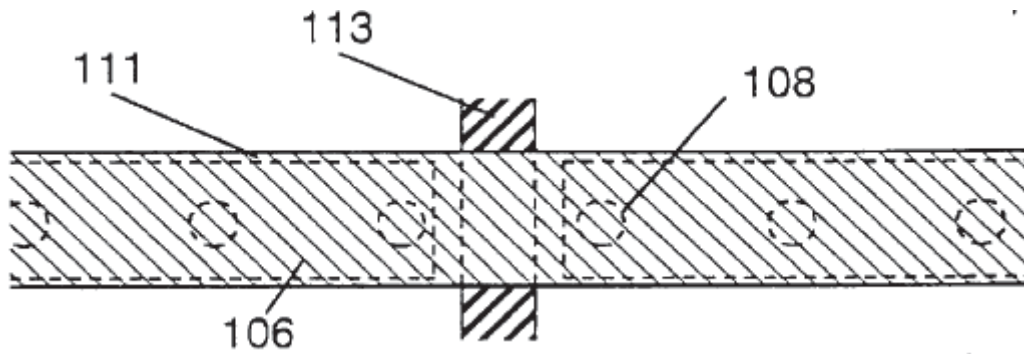
53. Koyama 604 is directed to semiconductor devices of LCD display devices that aim to provide wiring lines with reduced electric resistance without increasing capacitance. EX-1011 at 1:8-15, 4:56-64.

54. Specifically, Koyama 604 recognizes problems of signal quality issues in high-frequency signals when the signals are transmitted by wiring lines in the circuits of LCD display devices. EX-1011 at 2:37-4:53. The wiring lines here refer to data lines in a driving circuit 903 and scanning lines in a driving circuit 904 of the

LCD display devices. EX-1011 at 2:53-58. The data lines and scanning lines introduce high electric resistance when their lengths are long, and introduce capacitances between parallel-arranged wiring lines when the high-frequency signals are applied thereto. EX-1011 at 3:25, 3:39-42. The capacitances formed between the wiring lines or between wiring lines and the opposed electrode, in combination with the high resistance of each wiring line, causes deterioration of a transmission signal waveform. EX-1011 at 3:57-67. When the transmission signal waveform is distorted (e.g., rounded) to a large extent, a delay may occur in the operation timing of a circuit, or erroneous video information may be transmitted to pixels, thereby resulting in erroneous operation or disordered images. *See* EX-1011 at 4:1-4.

55. In order to address the abovementioned problems, Koyama 604 provides a semiconductor device including a circuit using a thin-film transistor (TFT) having an active layer that is constituted of crystalline silicon film provided on a substrate having an insulating surface, wherein at least a part of the wiring lines associated with the circuits is connected in parallel to an auxiliary wiring line that is provided with an interlayer insulating film interposed in between. EX-1011 at 4:65-5:7.

56. FIG. 1C of Koyama 604, reproduced below, illustrates a structure of a semiconductor device that includes the aforementioned configuration. As shown, a wiring line 111 is connected in parallel to an auxiliary wiring line 106 via a plurality of contact holes 108. *See* also EX-1011 at 5:55-58, FIGS. 1A-B.



EX-1011 (“Koyama 604”) at FIG. 1C

57. Koyama 604 alleges that this structure can greatly reduce the electric resistance of wiring lines, thereby allegedly reducing the waveform distortion (e.g., waveform rounding) in the wiring lines. *See* EX-1011 at 6:58-65.

58. Notably, the subject matter of Koyama 604 is mainly related to LCD display devices, which are substantially different from the active-matrix OLED display devices in Koyama 168. As explained above in Section II, LCD devices require a backlight to operate, while OLED display devices are self-luminescent and do not require a backlight. Also, the pixels in LCD devices are voltage controlled whereas the pixels in OLED display devices are current controlled. Further, the

subject matter of Koyama 604 is related to configurations of semiconductor devices, which have different configurations from wirings for pixel portions.

59. Additionally, Koyama 604 describes connecting wirings of semiconductor devices in parallel to a respective auxiliary wiring line, but does not suggest (1) connection between *power* lines, or (2) increasing the length of the a line to include a “protrusion” for accommodating a plurality of contact holes. In fact, Koyama 604 does not describe or suggest any “protrusion” on any wiring lines, let alone a “power line protrusion” for accommodating multiple contact holes, as alleged in the Petition. Pet. at 60-61. For example, in Koyama 604, contact holes are formed on the overlapping portions of the wiring line 111 and the auxiliary wiring line 106, which are two straight wiring lines connected in parallel. EX-1011 at FIG. 1C. Accordingly, Koyama 604 does not describe or suggest any “power line protrusion.”

D. US Patent Application Publication No. 2002/0053671

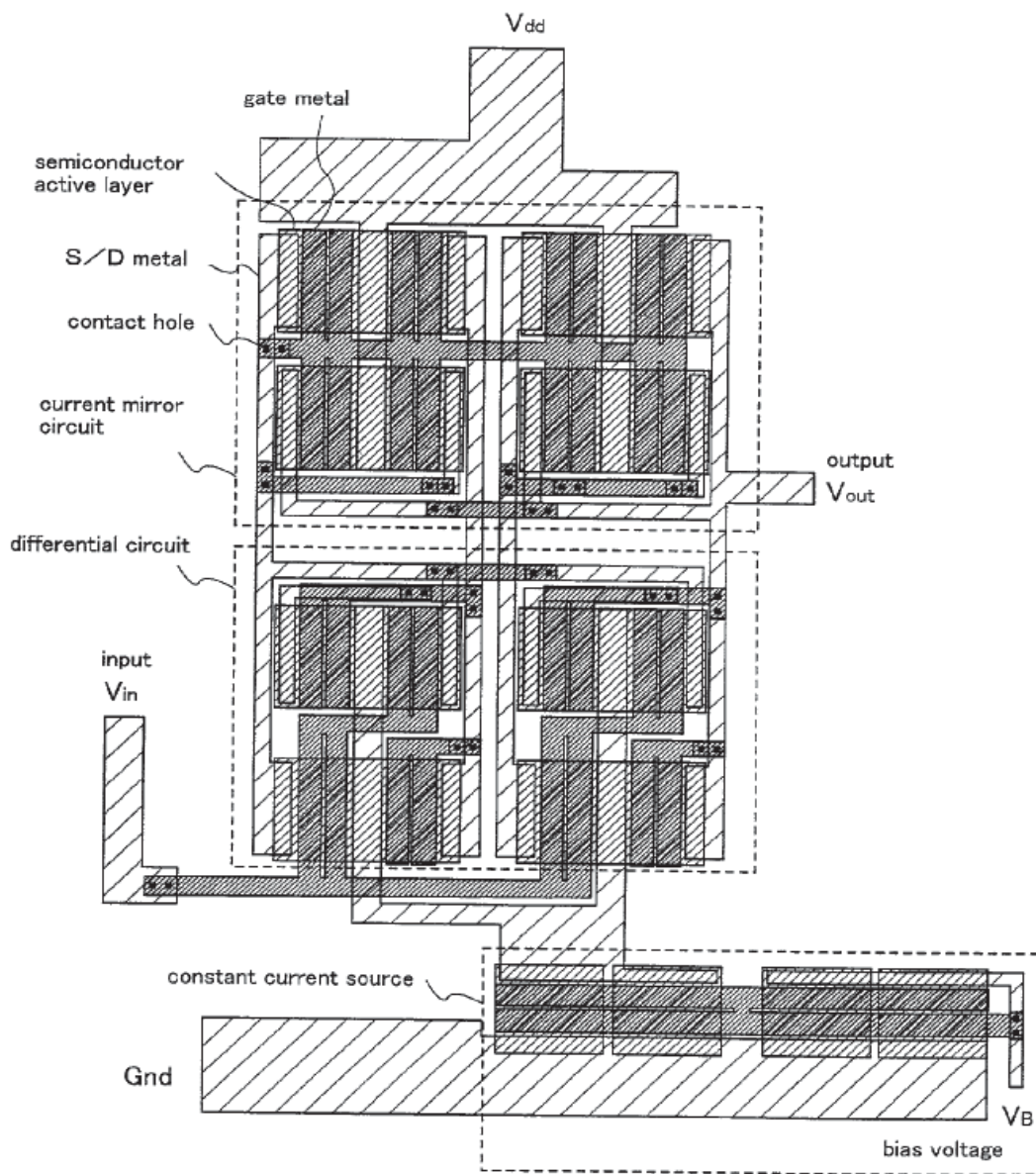
60. US 2002/0053671 (“Koyama 671”) is a US patent application publication that published on May 9, 2002.

61. Koyama 671 is directed to semiconductor devices in EL displays with improved analog buffer circuitry. EX-1012 at [0002] and [0055]. Specifically, Koyama 671 recognizes problems of conventional analog buffer circuits which have

varying characteristics of thin-film transistors (TFTs). *See* EX-1012 at Abstract, [0031].

62. In order to solve these problems, Koyama 671 provides an analog buffer circuit including a differential circuit, a current mirror circuit, and a constant current source, as well as designs of a structure and an arrangement of polycrystalline TFTs composing the circuits, to thereby reduce a difference of characteristics of the respective TFTs and provide an analog buffer circuit that has a small variation. EX-1012 at [0053].

63. Koyama 671 describes an example of an analog buffer circuit with reference to FIG. 12, and describes an example arrangement of TFTs of this circuit with reference to FIG. 13. EX-1012, [0083]-[0084], [0170], [0179]. Specifically, Koyama 671 describes that the analog buffer circuit includes two sets of differential circuits and current mirror circuits connected in parallel, and each of the differential circuits and current mirror circuits includes a plurality of TFTs. *See* EX-1012, [0176], [0178], FIG. 12. Referring to FIG. 13 of Koyama 671, reproduced below, portions of the components in the current mirror circuit, such as a semiconductor metal film (illustrated as “S/D metal” in FIG. 13) and gate metal, may be connected to each other through contact holes.



EX-1012 ("Koyama 671") at FIG. 13

64. Notably, the subject matter of Koyama 671 is directed to the configuration and manufacturing of analog buffer circuits in semiconductor devices, and is not related to wiring configurations of power lines of pixels in display devices.

As set forth above in Section II, the configurations of semiconductor devices differ from the configurations of wirings for a pixel portion.

65. Further, Koyama 671 describes only one power supply line Vdd, and does not describe or suggest connecting the power supply line Vdd to any other component via a contact hole. EX-1012 at FIG. 13. Furthermore, although Koyama 671 describes contact holes, these contact holes are utilized for bonding gate metal with semiconductor metal, but are not for connecting multiple power lines. EX-1012 at FIG. 13. Accordingly, Koyama 671 does not describe or suggest (1) connection of power lines, and (2) increasing the length of the power lines to include any “protrusion” for accommodating a plurality of contact holes. Namely, Koyama 671 does not describe or suggest any “power line protrusion” for accommodating multiple contact holes, as asserted by the Petitioners. Pet. at 61.

66. In addition, Koyama 671 does not describe utilizing the contact holes for reducing wiring resistance. As described above, Koyama 671 is directed to solving problems of varying characteristics of TFTs in an analog buffer circuit. See EX-1012 at Abstract, [0031]. Koyama 671 does not describe or suggest any configuration on power lines for reducing the wiring resistance in the power lines, let alone utilizing plurality of contact holes for reducing wiring resistance.

VII. Ground 1– Claim 1 is Not Anticipated under 35 U.S.C. § 102 By

Yamazaki, and is Not Rendered Obvious Under 35 U.S.C. § 103 By

Yamazaki

67. Claim 1 of the '267 Patent is not anticipated by and is not rendered obvious by Yamazaki.

68. First, Yamazaki does not describe a “first power line” as recited in claim 1. For example, Yamazaki does not disclose that the “current supply auxiliary line 301” (Petitioners’ alleged “first power line” of claim 1) is a “power line” that supplies current to light emitting elements of the display.

69. Second, Yamazaki does not suggest that the auxiliary line 301 “has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction,” as required by the claim. At most, Yamazaki only states that the auxiliary line 301 is parallel to the current supply line 305.

70. The Petition has not shown a reasonable likelihood that all features of challenged claim 1 of the '267 Patent are disclosed or rendered obvious by Yamazaki.

A. Yamazaki Fails to Disclose a “First Power Line” in Addition to a “Second Power Line” as Claimed

71. As recognized in the Petition, a “power line” as described in the ’267 Patent claims would be understood in the art to supply current to light-emitting elements. Pet. at 37, 40. Yamazaki discloses, as its power line, a current supply line 305 for supplying current to respective light-emitting (or EL) elements. EX-1008 at [0037]. The Petition contends that this “current supply line 305” corresponds to the claimed “second power line.” Pet. at 40-41.

72. Meanwhile for the “first power line,” the Petition cites to Yamazaki’s “current supply auxiliary line 301.” Yamazaki, however, does not disclose that the auxiliary line 301 supplies current to the EL elements. Unlike the current supply line 305, which Yamazaki describes as “a wiring for supplying a current... to each EL element,” Yamazaki only suggests that the auxiliary line 301 functions to aid the current supply line by “reduc[ing] the apparent wiring resistance of the current supply line.” EX-1008 at [0037]. Yamazaki provides no configuration or description that the auxiliary line 301, in addition to reducing the resistance on the current supply line 305, supplies current to the EL elements.

73. The Petition overlooks this deficiency of Yamazaki by conflating the described function of the current supply line 305 with that of the auxiliary line 301:

Like the '267 Patent's power line, Yamazaki's current supply auxiliary lines supply current. *See id.* at [0037] (“[T]he **current supply line** is a wiring for supplying a current, which flows to an EL element, to each EL element.”); *see also id.* at [0038] (“[T]he current supply auxiliary line 301 is electrically connected...to the current supply line 305 via the conductor 307.”); *id.* at [0039] (“Thus, the current supply auxiliary line 301 that is made of a low resistant material such as a copper foil is formed on the first printed wiring board 300.”).

Pet. at 39 (emphasis added).

74. The Petition simply cites to Yamazaki's description of the current supply lines 305, which passes *through* the pixel matrix 304 formed on the same substrate 330 (EX-1008 at [0038], FIG. 3A), without any explanation as to how or why this description is applicable to the entirely *different* auxiliary line 301, which passes in parallel *above* the pixel matrix 304 (EX-1008 at [0038], [0043]-[0044], FIG. 3C).

75. At most, the current supply line 305 and the current supply auxiliary line 301 are electrically connected in parallel. But this does not indicate, imply, or otherwise necessitate that the circuit is configured such that current running through the auxiliary line 301 is supplied to the EL elements. Also, Yamazaki provides no

circuit schematic and is silent as to where and how the lines 301 and 305 are connected to a power supply, ground, other components, etc.

76. Yamazaki only discloses that the current supply line 305 (but not the auxiliary line 301) supplies current to the EL elements, and that the auxiliary line 301 reduces the apparent wiring resistance in the current supply line 305. EX-1008 at [0037]. Neither Yamazaki nor the Petition demonstrate that the auxiliary line 301 supplies current to the EL elements.

77. Therefore, the Petition does not demonstrate that the first power line as claimed is disclosed in Yamazaki.

B. Yamazaki Fails to Disclose a “First Power Line” including First and Second Portions Extending in Different Directions as Claimed

78. Claim 1 requires that the first power line have “a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction.”

79. For the sake of argument, even if the auxiliary line 301 could be considered as a power line, Yamazaki does not disclose that the auxiliary line 301 includes multiple portions extending in different directions, as required in claim 1 of the '267 patent.

80. With reference to the Petition’s annotated FIG. 3A of Yamazaki, reproduced below, Petitioners allege that the large polygonal area highlighted in green depicts the “current supply auxiliary line 301” of Yamazaki as having a first portion extending in a first direction and a second portion extending in a second direction that. Pet. at 39-40. The Petitioners are interpreting FIG. 3A as showing the actual geometries and configurations of the box diagram components therein. This is incorrect because Yamazaki makes clear that these high-level box diagram features are not the actual geometry and layout of the wiring and circuitry.

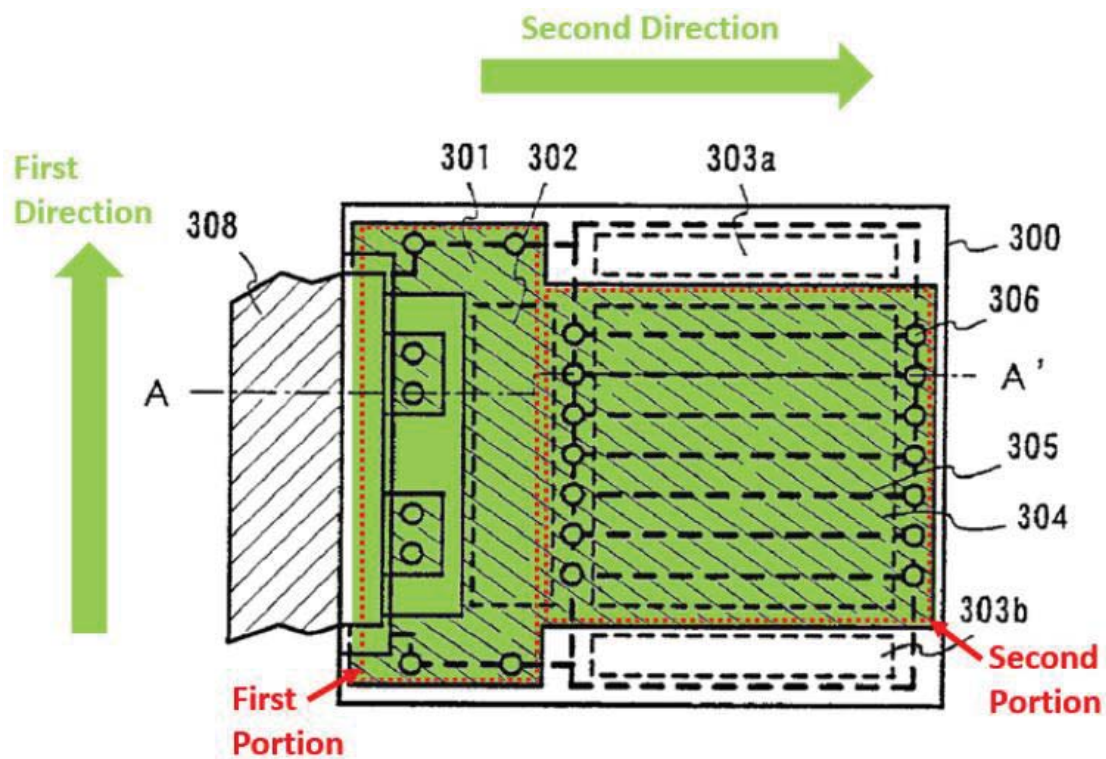


FIG. 3A of Yamazaki (Annotated by Petitioners at Pet., 40)

81. The diagram of FIG. 3A corresponds to an "EL display device" (Pet. at 31; EX-1008 at [0036]) including a pixel array (pixel portion 304) interposed by an array of intersecting power lines 305, scan lines (extending between gate driver circuits 303a/b, Pet. at 29), and data lines (extending from source driver circuit 302, Pet. at 32). That is, the depicted view corresponds to the entire display array, including the pixel array that "includes data lines that intersect scan lines". Pet. at 31.

82. Thus, the EL display device of FIG. 3A corresponds to at least the size of the display portion of a television having a large screen (e.g., 20 to 60 inches), as shown in Yamazaki's FIG. 8A. EX-1008 at [0089]-[0092]. Petitioners' allegation that the polygon region annotated above in green, which covers all of the pixel array 304 and more, is one contiguous wire or "power line" that stretches across the entirety of a display region of a television and beyond is, on its face, non-sensical and plainly contrary to the plain and ordinary meaning of a "line," particularly in the context of the '267 Patent.

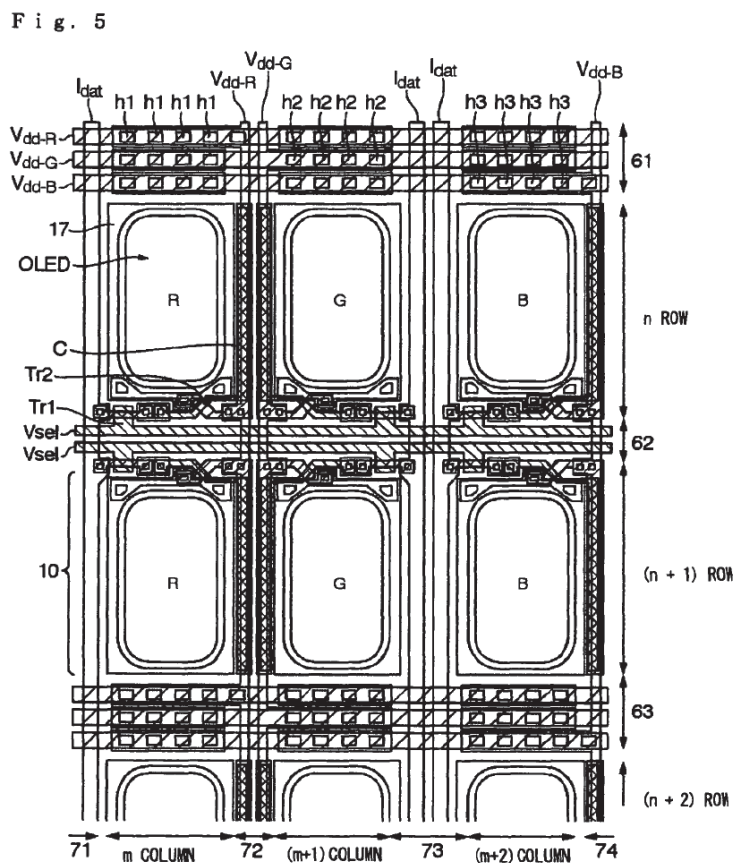
83. For example, the outsized region that Petitioners contend constitutes a first power "line" would not be a "line" in accordance with the plain and ordinary meaning of the term in the context of the '267 Patent. As discussed below, at the time of invention of the '267 Patent, a POSITA would have understood the claim

term “line”, as used in the field of display device technology, to be a substantially elongated element with dimensions that enable a plurality of elements to be arranged in a pixel matrix. At least for this reason, a POSITA would have understood that the entire annotated region is not a “line” as recited in claim 1 of '267 Patent. For example, the '267 Patent describes the following with respect to “lines”:

With conventional color-display active-matrix-driven display panels, an **M number each of electric power lines and data lines are disposed in the column direction on a pixel matrix** with an N number of columns and an M number of rows formed on a pixel region, as well as an **N number of selection lines being disposed in the row direction on the aforementioned matrix**. With a given pixel of such a wiring layout, a **data line is disposed between the given pixel and the left-adjacent pixel**, and an **electric power line is disposed between the given pixel and the right-adjacent pixel**. That is to say, with the **lines disposed between adjacent pixels** in the column direction, a layout is formed so that one data line and one electric line make up one pair.

EX-1001 at 30-42 (emphasis added).

84. Further, the '267 Patent also describes providing power “lines” that “improve[] the aperture ratio of the pixel while forming pixels with the same pixel pitch,” which further suggests that the elements constituting “lines” have dimensions small enough to be horizontally arranged as a plurality in an area forming pixels. EX-1001 at Abstract. An example of lines (e.g., power lines V_{dd} , scan lines V_{sel} , data lines I_{dat}) is also shown in, for example, FIG. 5 of the '267 Patent, reproduced below:



EX-1001at FIG. 5 (the '267 Patent)

85. Also, in another reference applied in the Petition, Koyama 168, none of the lines in the display devices (e.g., the power supply lines VY1/VY2/VX1/VX2, gate signal lines G1/G2, source signal lines S1/S2, etc.) has a size that is large enough to cover all pixels, in contrast to the region annotated by the Petitioners as the “current supply auxiliary line 301”. EX-1010, FIG. 3, FIG. 41, FIG. 42, FIG. 44.

86. The above demonstrates that the ordinary and customary meaning of the term “line,” at the time of the filing date of the ’267 Patent and as used in the field of display device technology, to be a substantially elongated element with dimensions that enable a plurality of the element to be horizontally arranged in a pixel matrix.

87. In contrast, with reference to the Petitioners’ annotated portion in Fig. 3A of Yamazaki, reproduced below, the Petitioners’ alleged “current supply auxiliary line 301” of Yamazaki has substantially a **block shape**, rather than being a **substantially elongated** element. The portion alleged by the Petitioners cannot be reasonably considered to have a shape that resembles a “line.” Moreover, the portion alleged by the Petitioners to correspond to the “current supply auxiliary line 301” of Yamazaki **covers an entirety of the pixel portion 304, and even most of the EL display device**. That is, such portion has dimensions that do not enable a plurality of the portion (alleged line) to be horizontally arranged in a pixel matrix.

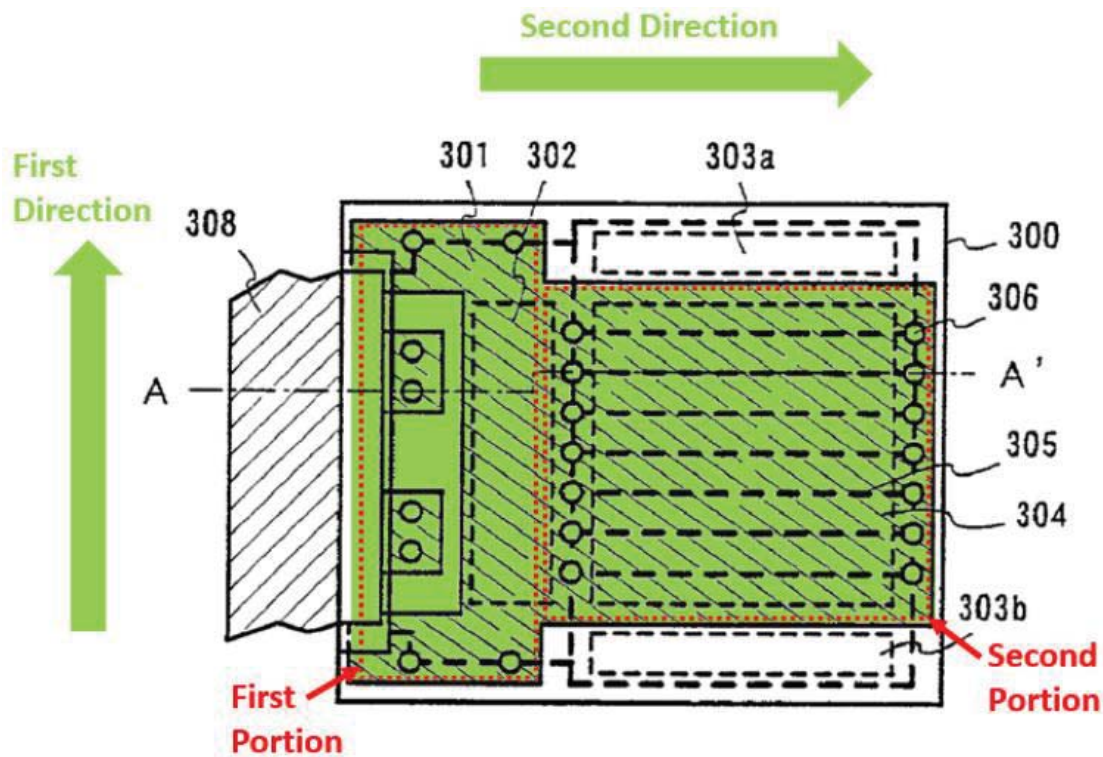


FIG. 3A of Yamazaki in Pet., 40 (Annotated by Petitioners)

88. While Yamazaki describes element 301 as a “current supply auxiliary line 301,” such usage of the term “line” in Yamazaki is contrary to its common technical meaning, and thus substantially departs from the ordinary and customary meaning of the term “line” as used in and understood for the claims of the ’267 Patent.

89. At least in view of the above, a POSITA would have understood, at the time of invention of the ’267 Patent, that the entirety of the Petitioner’s annotated region above (in green) is not a “line” as claimed, and further does not describe or suggest the “first power line” as claimed. If, for the sake of argument, the annotated

region is an accurate depiction of element 301, then such element would have been understood by a POSITA to be a “plate,” not a “line.”

90. In any case, Yamazaki indicates that the expansive polygonal area of FIG. 3A (annotated in green by Petitioners) is not the actual layout or geometry of the auxiliary line 301.

91. FIG. 3A, as annotated by Petitioner, depicts this area as extending contiguously from the alleged “First Portion” to the alleged “Second Portion,” and completely overlapping the source driver circuit 302. The cutout line A-A’ for the cross-sectional view of FIG. 3C overlaps this purported contiguous multi-portion line. To accept Petitioners’ allegation that FIG. 3A depicts the geometry of the auxiliary line 301 would therefore require that the cross-section along the cutout (A-A’) include a contiguous line 301 extending horizontally from above the pixel array 304 across the source driver circuit 302 and beyond. However, as shown in FIG. 3C (reproduced below as annotated by Petitioner), the line 301 does not extend across the source driver circuit 302 and is not contiguous from the purported “Second Portion” to the purported “First Portion”:

FIG. 3A of Yamazaki
(EX-1008) Annotated
by Petitioners; Pet.,
40.

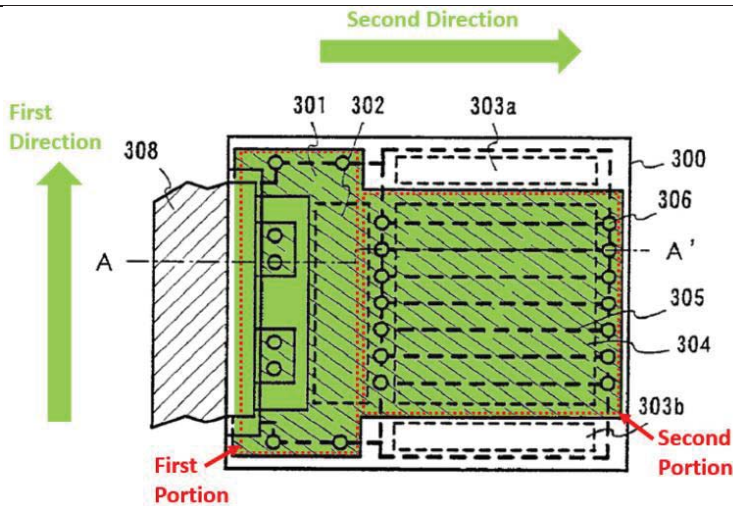
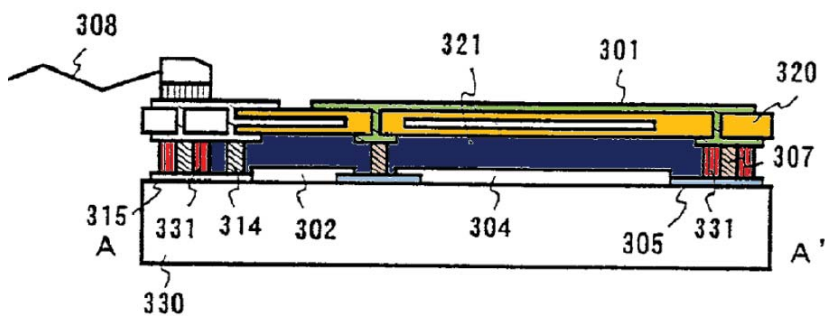


FIG. 3C of Yamazaki
(EX-1008) Annotated
by Petitioners; Pet.,
45.



92. Rather, FIG. 3C of Yamazaki shows a clear endpoint for the alleged auxiliary line 301 (annotated green by Petitioners) at the cross-section, that does not continue across the purported “First Portion” (further annotated in purple below):

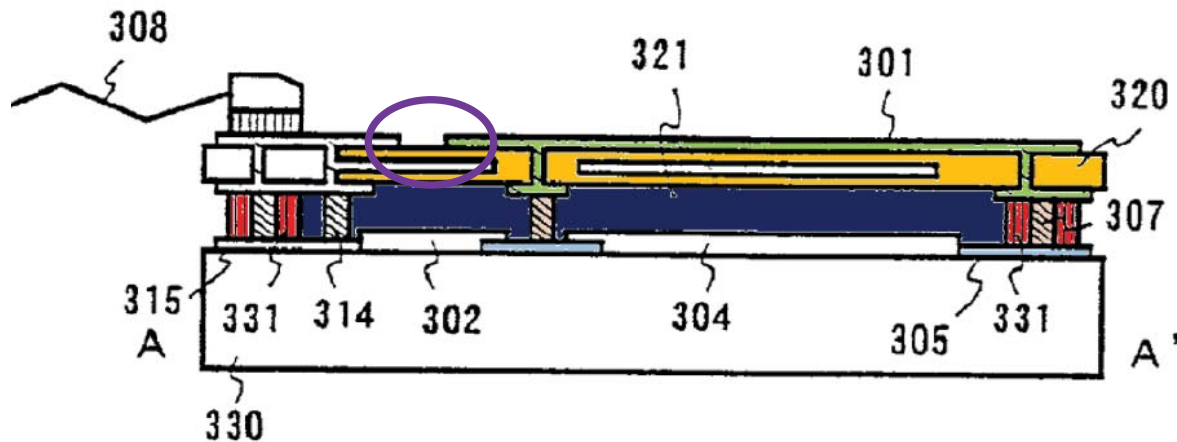
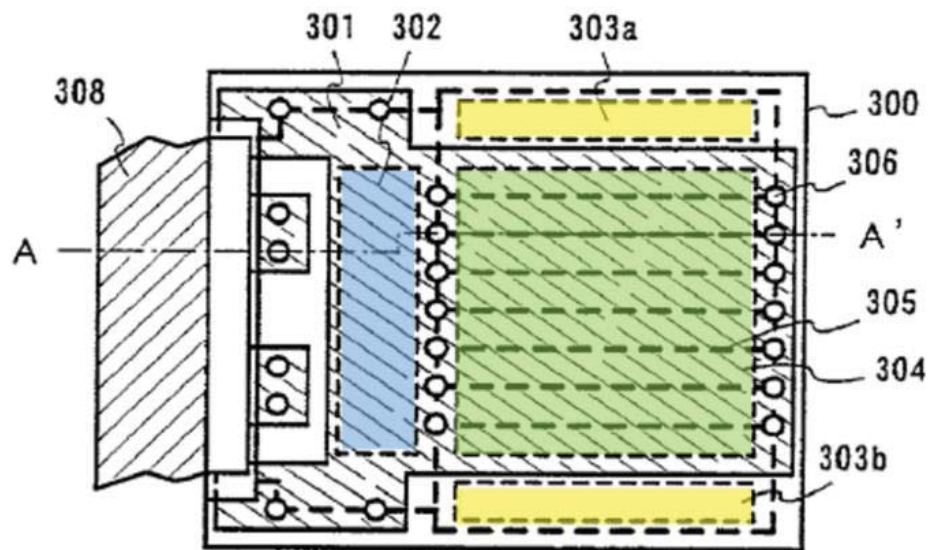


FIG. 3C of Yamazaki Annotated by Petitioner (Pet. at 45), Further Annotated

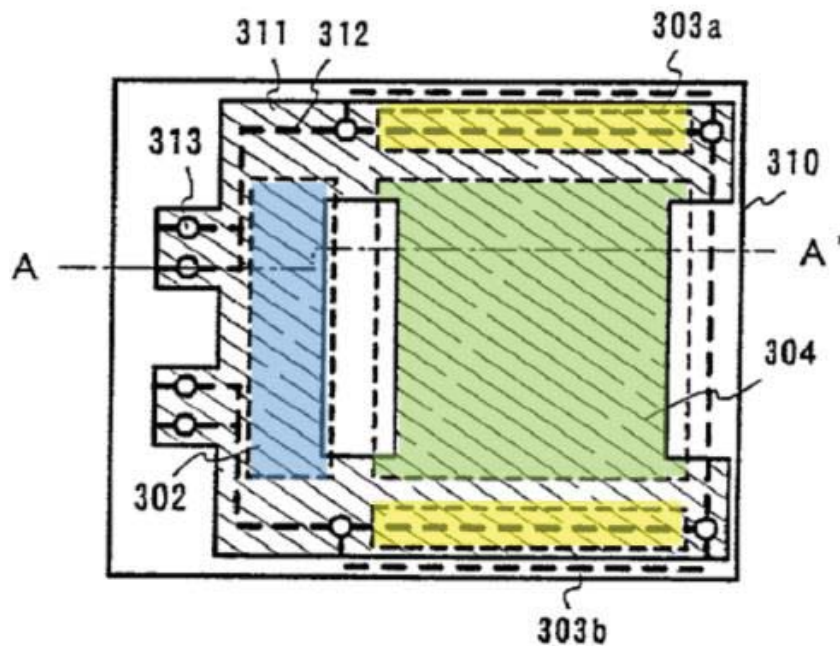
93. A POSITA would have therefore understood that the green annotated region of FIG. 3A is not one contiguous wire or otherwise a depiction of the actual geometry of the auxiliary line 301. In fact, the auxiliary line 301 is provided in parallel with the plural power lines (current supply lines 305) (EX-1008 at [0037]) and the Petition itself recognizes that the auxiliary line 301 is not a single line, but rather plural lines (Pet. at 39: “Like the ’267 patent’s power lines, Yamazaki’s current supply auxiliary lines supply current” (emphasis added)). FIG. 3A and the associated descriptions in Yamazaki are silent with respect to how these auxiliary lines 301 are arranged and in what directions they each extend.

94. In addition, the fact that FIG. 3A does not depict the actual configurations, constituent parts, and physical geometries of the display device components is evidenced not just by the auxiliary line 301, as discussed above, but

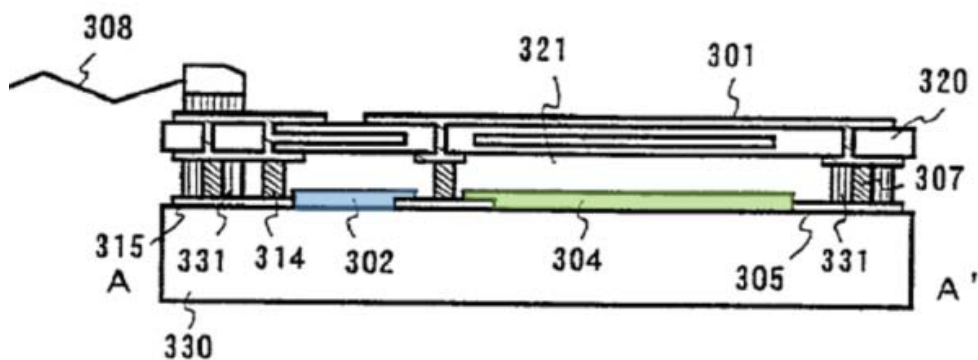
by every other depicted component. For example, FIGS. 3A-3C of Yamazaki, reproduced below, depict the “source driver circuit 302,” “gate driver circuits 303a-303b,” and “pixel portion 304” in the form of boxes (annotated in blue, yellow, and green, respectively).



EX-1008 (“Yamazaki”) at FIG. 3A (annotated)



EX-1008 (“Yamazaki”) at FIG. 3B (annotated)



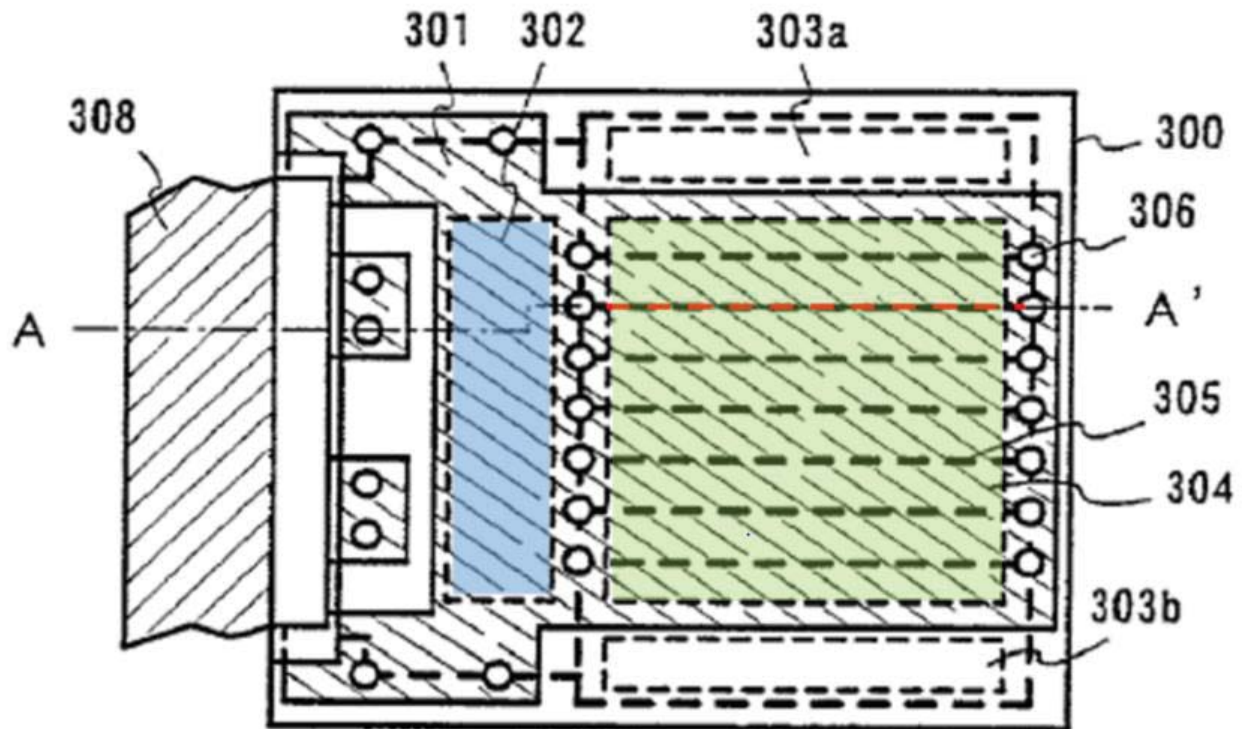
EX-1008 (“Yamazaki”) at FIG. 3C (annotated)

95. However, these components are not simply boxes covering the corresponding areas depicted in the figures, but rather include a complexity of distinct, interconnected constituent components of various sizes and shapes. For example, source driver circuit 302 includes multiple transistors (N channel TFT and

P channel TFT). EX-1008 at [0052], FIG. 4B, FIG.6, FIG. 7, [0052]. Similarly, the pixel portion 304 includes an array of pixels that contain various transistors, capacitors, etc. EX-1008 at [0007], [0052], FIG. 2, FIG. 4B, FIG.6, FIG. 7. The actual area, configuration, size, and shape of the constituent elements of the display device components are not reflected by the high-level polygonal regions depicted in the box diagrams of FIGS. 3A and 3B.

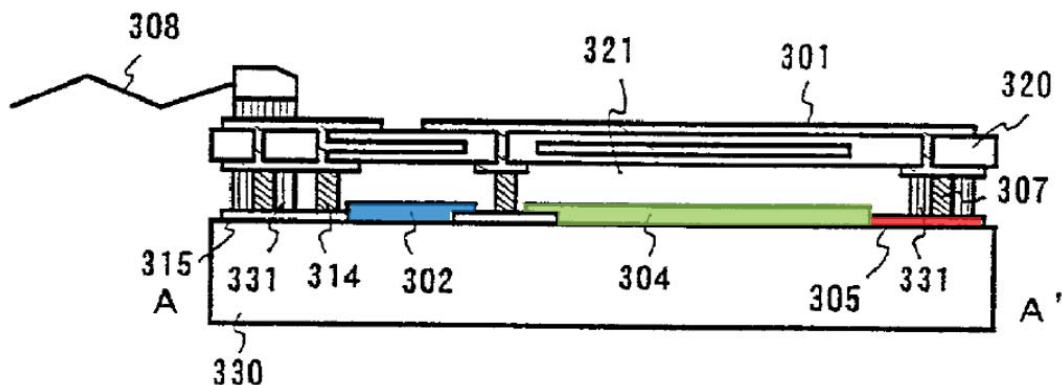
96. Additional inconsistencies and omissions between the polygonal areas of the box diagrams of FIGS. 3A and 3B and the cross-sectional view of FIG. 3C further highlight that the box diagrams do not depict the geometries and physical layouts of constituent components.

97. For example, FIG 3A (annotated below) illustrates one of the current supply lines 305 (annotated in red) that exactly overlaps the cutout line A-A' extending across the pixel portion 304 (annotated in green):



Yamazaki (EX-1008) at FIG. 3A (annotated)

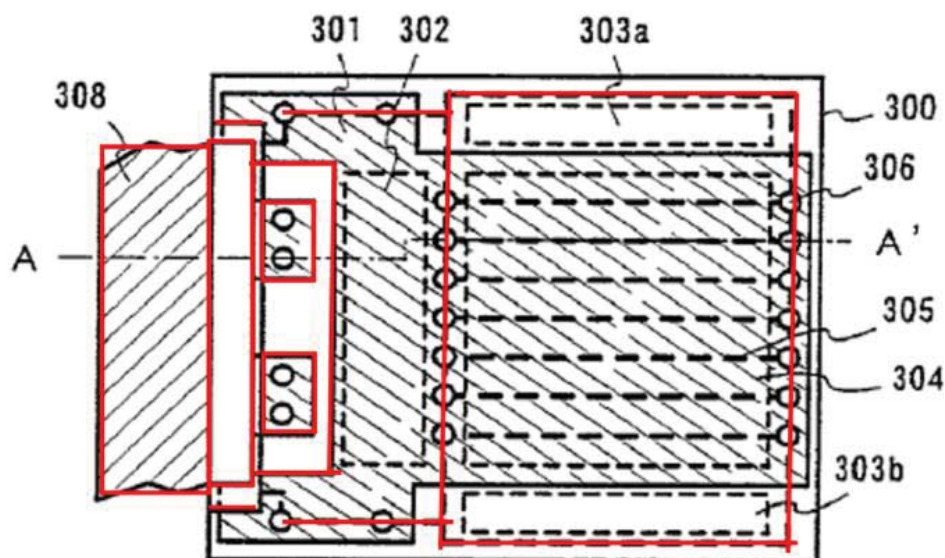
98. Conversely, the cross-sectional view (FIG. 3C, reproduced below) does not have the current supply line 305 going across the pixel portion at the cutout A-A':



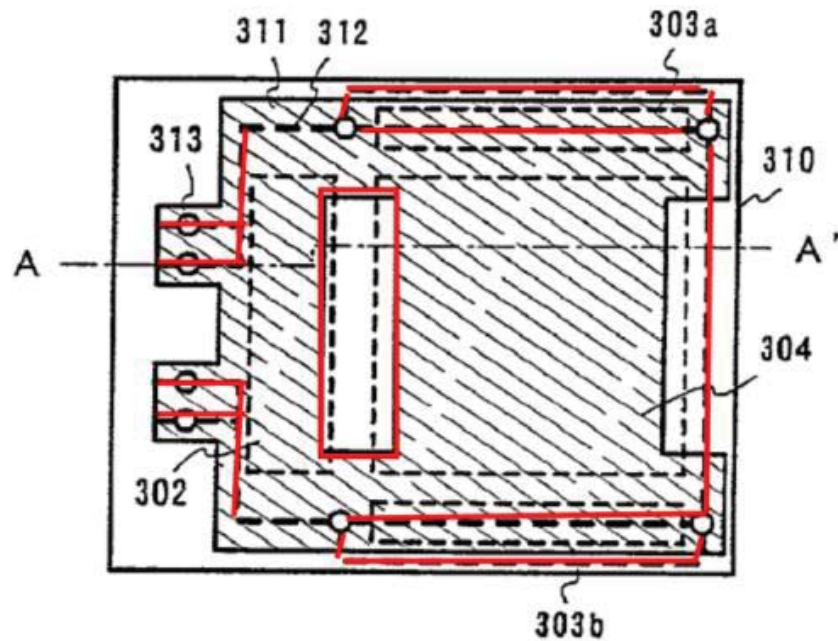
EX-1008 (“Yamazaki”) at FIG. 3C (annotated)

99. Yamazaki also describes that the first PWB 300 (illustrated in FIG. 3A) and the second PWB 310 (illustrated in FIG. 3B) are adhered to form the PWB 320, and the PWB 320 is then bonded with the element-formed substrate 330. EX-1008 at [0043]. Like with the auxiliary line 301 in FIG. 3A, FIG. 3B illustrates the “gate control line 311” as an outsized polygonal region covering most of the second PWB 310, including at the cutout line A-A’, yet there is no corresponding depiction of such an extensive and contiguous “gate control line 311” illustrated in FIG. 3C.

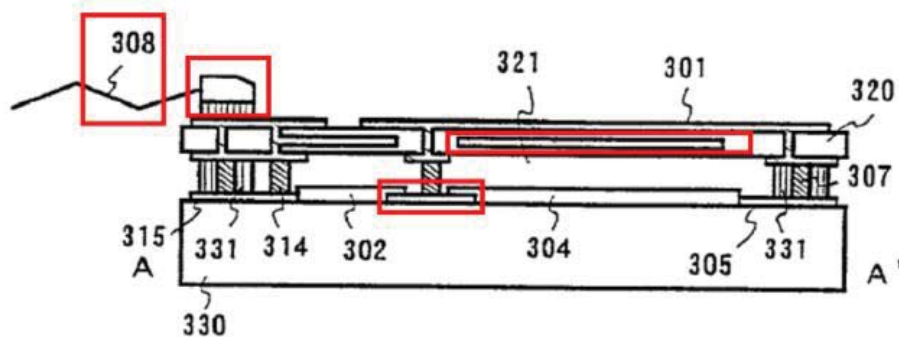
100. Furthermore, many components illustrated in FIGS. 3A through 3C (e.g., by circles, polygons, dashed lines, etc.) are not labeled or described in Yamazaki, as annotated in red below:



EX-1008 (“Yamazaki”) at FIG. 3A (annotated)



EX-1008 (“Yamazaki”) at FIG. 3B (annotated)



EX-1008 (“Yamazaki”) at FIG. 3C (annotated)

101. These omissions further demonstrate that a POSITA would not consider FIG. 3A as a reliable depiction of the physical layouts of the display device circuitry, including the number, arrangement, and directions of the auxiliary lines 301.

102. In addition to the inconsistencies between FIGS. 3A-C of Yamazaki, the lack of description of such components (annotated in red) that are illustrated above in FIGS. 3A-3C cause uncertainty as to what such components are, if and how they are connected/coupled to labeled components, and if and how they are involved in the operations of the labeled components, including the “current supply auxiliary line 301.” Also, in addition to the inconsistencies, the lack of description of such components further cause uncertainty as to the particular shape, configuration, and functions of labeled elements, including the number, arrangement, and directions of the auxiliary lines 301.

103. In summary, the Petition’s reliance on the box diagram components of FIG. 3A as somehow teaching a power line with different portions extending in different directions is incorrect at least because Yamazaki itself establishes that the polygonal regions in FIG. 3A, including that for the auxiliary lines 301, do not depict the constituent components of these regions, or the physical layout, geometry, directions, etc., of the constituent components. The cross-sectional view of FIG. 3C, even as annotated by the Petition (Pet., 45), proves that the polygon region for the auxiliary line 301 in FIG. 3A is not a depiction of the actual geometry, number, interconnectivity, etc., of the auxiliary lines 301. Petitioners’ reliance on the polygonal box diagram regions of FIG. 3A is therefore erroneous, and the Petition

therefore does not establish that Yamazaki discloses a first power line with different portions extending in different directions.

**VIII. Ground 2– Claim 1 is Not Rendered Obvious Under 35 U.S.C. § 103 By
Koyama 168 In View of Koyama 604 and/or Koyama 671**

104. As acknowledged in the Petition, Koyama 168 fails to disclose “**a first power line that has ... a second portion extending in a second direction that intersects the first direction**” and “**the second portion of the first power line being electrically connected to the second power line through plurality of contact holes**” as recited in claim 1 of the ’267 Patent. Pet. at 58 (Petitioner contend that Koyama 168 “used a single contact hole to connect any two power lines”), 75-76 and 87 (Petitioners contend that “the Koyama Combination features Koyama 168’s circuitry except that the vertical ‘VY’ power lines feature protrusions to accommodate multiple contact holes that connect to the horizontal ‘VX’ power lines.”).

105. The Petition instead alleges that a POSITA would have been motivated to combine Koyama 168 with Koyama 604 and/or Koyama 671 to arrive at these missing features. Pet., 56-66. Specifically, the Petition alleges that a POSITA would have understood that wiring resistance in Koyama 168 could further be reduced by

increasing the number of contact holes, and in so doing would have added power line “protrusions.” Pet., 57-65.

106. Petitioners’ assertions are incorrect, and do not establish obviousness of claim 1 of the ’267 Patent, at least for the following reasons.

A. Petitioners Fail to Establish a Reasonable Expectation of Success in Modifying Koyama 168

107. The Petition alleges that a POSITA would have been motivated to modify Koyama 168 to add power line “protrusions” (i.e., increasing the length of the power line) to accommodate an increased number of contact holes in order to reduce wiring resistance, and (2) a POSITA would have had a reasonable expectation of success in reducing wiring resistance by the proposed modification. Pet. at 58-65.

108. However, Koyama 168 clearly conveys that increasing the length of the wirings would increase wiring resistance. Specifically, Koyama 168 describes potential drop in power supply lines is caused by the wiring resistance, due to the length of the wirings. EX-1010 at [0032], [0034]-[0036], [0050]. Example relevant portions of Koyama 168 are reproduced below:

due to **potential drop caused by wiring resistance**, the electric potential of the power supply line changes depending on its position in the pixel portion.
(emphasis added).

EX-1010 at [0032].

depending on the **length of the wiring** from the position of the external input terminal to the position of the power supply line of the pixel portion, the **electric potential of the power supply line varies**. (emphasis added).

EX-1010 at [0034].

when the display device is relatively **large**, the change in the electric potential of the power supply line due to the **wiring resistance** becomes large.
(emphasis added).

EX-1010 at [0035].

as the display device becomes **larger**, the variation in the distance from the external input terminal to the power supply line of the pixel portion becomes larger, and the variation in **the length of the wiring** of the power supply line drawn-around portion **becomes larger** accordingly. Therefore, the **change**

becomes larger in the electric potential of the power supply line (emphasis added).

EX-1010 at [0036].

with regard to a power supply line far from the input portion (b in FIG. 24), since the **length of the wiring is large**, the **potential drop** caused due to the **wiring resistance** is large. (emphasis added).

EX-1010 at [0050].

109. As indicated above, Koyama 168 describes that, when the length of the wiring is increased, the wiring resistance is increased and thus the potential drop caused by the wiring resistance is also increased. Such a relationship between the wiring resistance and the length of wiring is well-known in the art. EX-1008 at [0005]-[0006]; EX-2010 at 91-93.

110. In order to reduce wiring resistance and thus potential drop, Koyama 168 describes features for reducing the length of wirings. EX-1010 at [0133], [0138]-[0139]. Particularly, Koyama 168 clearly describes that “it is **necessary** to make the wirings as short as possible.” EX-1010, [0156] (emphasis added).

111. In contending that a POSITA would have been allegedly motivated to modify Koyama 168 to add power line “protrusions” to accommodate an increased

number of contact holes in order to reduce wiring resistance, and that a POSITA would have allegedly had a reasonable expectation of success in reducing wiring resistance by the proposed modification, the Petitioners have ignored Koyama 168's teaching that it is "necessary" to decrease, **not** increase, the length of the power lines in order to reduce wiring resistance. EX-1010 at [0156].

112. Thus, taking the teachings of the art as a whole, a POSITA would not have been motivated by this art to "increase[]" the power lines of Koyama 168 (Pet., 60), because Koyama 168 expressly conveys that such a modification would increase wiring resistance.

113. For similar reasons, the Petition (*see* Pet. at 64) does not establish a "reasonable expectation of success" that its proposed combination would reduce wiring resistance. This is because the Petitioners' analysis does not address or appreciate the teaching of the art **as a whole**, which emphasizes that increasing the power line would increase wiring resistance. EX-1010 at [0032]-[0036], [0156]; EX-1011 at 3:20-28; *see also* Pet. at 63 ("The '267 patent, Koyama 168, and Koyama 604 all address their respective problems—essentially ensuring that power or signals are not attenuated because they must pass relatively long distances."). For example, the Petition does not address the fact that the art conveys that extending (or increasing the length of) the power supply line in Koyama 168 would achieve the

opposite effect. Thus, the Petition does not establish that a POSITA would reasonably expect that “extending the VY power lines to overlap the VX power lines to accommodate more contact holes” (Pet. 64-75, 75-76, 86-88) would ultimately reduce wiring resistance in the VY power supply line of Koyama 168. The Petition’s analysis and conclusions ignore contradictory and critical disclosures in the primary Koyama reference.

B. It Would Not Have Been Obvious to Modify Koyama 168 to Disclose or Suggest the “Second Portion of the First Power Line” and “Plurality of Contact Holes” as Recited in Claim 1 of the ’267 Patent

114. For at least the below reasons, A POSITA would not have found it obvious to modify Koyama 168 in view of Koyama 604 and/or Koyama 671 to include “a first power line that has ... a second portion extending in a second direction that intersects the first direction” and “the second portion of the first power line being electrically connected to the second power line through plurality of contact holes” as recited in claim 1 of the ’267 Patent.

1. A POSITA Would Not Have Considered Modifying Koyama 168 to Extend or Increase Length of Power Lines

115. As described above in Sections VI(B) and VIII(A), Koyama 168 is directed to solving problems caused by the wiring resistance of power supply lines,

due to the length of the wirings. EX-1010 at [0032]-[0036], [0050]. In order to solve these problems, Koyama 168 describes features for reducing length of wirings. EX-1010, [0133], [0138]-[0139]. Particularly, Koyama 168 clearly describes that “it is *necessary* to make the wirings as short as possible.” EX-1010 at [0156] (emphasis added).

116. By “extending the VY power lines to overlap the VX power lines to accommodate more contact holes,” as contended in the Petition (Pet. at 64-75, 75-76, 86-88), the VY power lines of Koyama 168 would be made longer, not “as short as possible” as required by Koyama 168.

117. Thus, a POSITA would not have considered modifying Koyama 168 to extend (or increase) the length of any of its power lines in order to form a protrusion to accommodate multiple contact holes, since modifying Koyama 168 to extend (or increase) length of power lines is clearly contrary to the express teaching of Koyama 168. That is, Koyama 168 teaches away from the Petition’s proposed combination.

2. Modification of Koyama 168 Would Make Koyama 168 Unsatisfactory For Its Intended Purpose

118. As described above in Sections VI(B) and VIII(A), Koyama 168’s solution for solving the wiring resistance (which causes the problems of potential drop) require reducing the length of the power supply lines. Specifically, since

Koyama 168 describes that the problems of potential drop in power supply lines are caused by wiring resistance and provides features for reducing the length of the power supply lines to reduce the potential drop, it is clear that the intended purpose of Koyama 168 is to reduce the length of power supply lines, so as to reduce the wiring resistance therein.

119. As described above in Section II and VIII(A), extending (or increasing) length of a power supply line would increase the wiring resistance of the power supply line.

120. Thus, modifying Koyama 168 to extend (or increase) the length of power lines, in the manner proposed by the Petitioners, would make Koyama 168 unsatisfactory for its purpose of reducing wiring resistance, since such modification would instead increase the wiring resistance.

121. At least in view of the above, a POSITA would not have found it obvious to modify Koyama 168 by extending (or increasing) the length of any of its power lines.

3. A POSITA Would Not Have Looked Towards Koyama 604 and/or Koyama 671 To Modify Koyama 168

122. A POSITA would not have found it obvious to combine Koyama 604 and/or Koyama 671 with Koyama 168, nor look from one to the other for guidance.

123. Specifically, a POSITA would not have considered Koyama 604 when working on the subject matter of Koyama 168, for at least the following reasons.

124. First, as described above in Section VI(C), the subject matter of Koyama 604 is directed to semiconductors in LCD devices. EX-1011 at 1:8-15, 4:56-5:7. Specifically, the descriptions of Koyama 604, including the origins of the problems to be solved, are all related to LCD devices. Koyama 604 mentions an “EL element” only a single time. EX-1011 at 16:25-30.

125. It would be highly unlikely for a POSITA to search or take guidance from Koyama 604, which is substantially related to LCD technology, when working on active-matrix OLED display technology described in Koyama 168. As described above in Section II, LCD devices, such as described in Koyama 604, and active-matrix OLED display devices, such as described in Koyama 168, are substantially different. For example, (a) LCD devices required a backlight, while OLED display devices do not require a backlight, (b) the pixels in LCD devices are voltage controlled whereas the pixels in EL display devices are current controlled, and (c) the arrangement of the wirings in LCD devices is different from the arrangement of wirings in EL display devices.

126. Second, a POSITA would not have considered the subject matter of Koyama 604, which is related to semiconductor devices, when considering wiring

configuration for the power supply lines of Koyama 168, which are wirings for supply current to pixels. As described above in Section II, semiconductor devices include circuits formed by thin film transistors (TFTs) which are utilized for controlling the operation of the display devices, while wirings (e.g., power lines, data lines, and scanning lines) are utilized for transmitting signals to the semiconductor devices and/or the pixels. It would have been clear to a POSITA that the operations of the semiconductor devices and the wirings are two different aspects in display devices, and the configurations associated therewith are different from one another.

127. Third, as described above in Sections VI(B) and VI(C), Koyama 168 is directed to solving problems associated with wiring configuration of power supply lines, while Koyama 604 is directed to solving problems associated with data line and scanning line of a semiconductor device. EX-1010 at [0032]-[0036], [0044]-[0053]; EX-1011 at 2:37-4:53. Because Koyama 168 and Koyama 604 are directed to subject matter for solving entirely different problems, a POSITA would not have considered Koyama 604 when working on the subject matter of Koyama 168.

128. In view of the above, a POSITA would not have considered combining Koyama 168 and Koyama 604, as the references describe different technology and aspects of display devices, as well as substantially different problems to be solved.

129. Similarly, a POSITA would not have considered Koyama 671 when working on subject matter of Koyama 168.

130. First, a POSITA would not have considered the subject matter of Koyama 671, which is related to semiconductor devices, when considering wiring configuration for the power supply lines of Koyama 168, which are for supplying current to pixels. EX-1012 at [0002], [0055].

131. Second, as described above in Sections VI(B) and VI(D), Koyama 168 is directed to solving problems associated with wiring configuration of power supply lines, while Koyama 671 is directed to solving problems associated with analog buffer circuit of a semiconductor device. Because Koyama 168 and Koyama 671 are directed to subject matter for solving entirely different problems, a POSITA would not have considered Koyama 671 when working on the subject matter of Koyama 168. EX-1010 at [0032]-[0036], [0044]-[0053]; EX-1012 at Abstract, [0031].

132. Although Koyama 671 describes contact holes, Koyama 671 does not describe utilizing the contact holes for reducing wiring resistance. As described above in Section VI(D), Koyama 671 is directed to solving problems of varying characteristics of TFTs in analog buffer circuit. EX-1012 at Abstract, [0031]. Koyama 671 does not describe or suggest any configuration on power lines for

reducing the wiring resistance in the power lines, let alone utilizing plurality of contact holes for reducing the wiring resistance.

133. At least in view of the above, a POSITA would not have considered combining Koyama 168 and Koyama 671, as the references describe different technologies, as well as substantially different problems to be solved

4. Koyama 604 and Koyama 168 Fail to Cure Deficiencies of Koyama 168

134. For the sake of argument, even if the subject matter of Koyama 604 and/or Koyama 671 is taken into consideration and is used to modify Koyama 168, such a combination still fails to cure the deficiencies of Koyama 168 and fails to arrive at all features of claim 1 of the '267 Patent, including **“a first power line that has ... a second portion extending in a second direction that intersects the first direction”** and **“the second portion of the first power line being electrically connected to the second power line through plurality of contact holes.”**

135. Koyama 604 fails to cure the deficiencies of Koyama 168, for at least the following reasons.

136. First, as described above in Section VI(C), Koyama 604 describes semiconductor devices in LCD display devices, and the wiring lines described in Koyama 604 are wiring lines of peripheral circuits in the semiconductor devices, such as **data lines** and **scanning lines**. EX-1011 at 2:53-58, 6:66-7:3. Thus,

Koyama 604 does not describe **power lines** of OLED display devices, which are wirings for providing power or current for driving pixels of OLED display devices, let alone wiring methods for configuring **power lines**.

137. Second, as described above in Section VI(C), Koyama 604 describes connecting a wiring line in semiconductor devices (e.g., a **data line** or a **scanning line**) in parallel to an auxiliary wiring line via a plurality of contact holes. EX-1011 at 5:55-58, 6:66-7:3, and FIG. 1C.

138. The Petitioners cite to FIG. 1C and alleges that Koyama 604 “confirms that having a **power line protrusion** would have been an obvious solution for creating enough overlap to accommodate multiple contact holes.” (emphasis added). Pet. at 60-61. However, since Koyama 604 does not describe any power line, Koyama 604 also fails to describe or suggest any “power line protrusion” as contended by Petitioners. For example, FIG. 1C of Koyama 604 is associated with configuration of wirings in a semiconductor device, and the wiring lines illustrated in FIG. 1C are **scanning lines** and **data lines**, not **power lines**. EX-1011 at 5:42-43, 6:66-7:3.

139. While Koyama 604 describes that a wiring line is connected in parallel to an auxiliary wiring line via a plurality of contact holes (EX-1011 at 5:55-58, FIG. 1C), Koyama 604, at most, suggests that the overlapping portions of two lines in

parallel can accommodate multiple contact holes, but does not, by any means, suggest a “protrusion” for accommodating multiple contact holes, as contended by the Petitioners. Rather, it is clear from FIG. 1C of Koyama 604 that the contact holes of Koyama 604 are formed on the overlapping portions of wiring line 111 and auxiliary wiring line 106, which are two straight wiring lines connected in parallel. EX-1011 at FIG. 1C.

140. In view of the above, the Petitioners’ reliance on Koyama 604 is misplaced and based on hindsight, since Koyama 604 does not disclose (1) a power line, (2) a protrusion on the power line, and (3) accommodating multiple contact holes on the protrusion.

141. Koyama 671 also fails to cure the deficiencies of Koyama 168.

142. First, as described above in Section VI(D), Koyama 671 describes only one power supply line Vdd, but does not describe or suggest connecting the power supply line Vdd to any other components via a contact hole. EX-1012 at FIG. 13.

143. Second, as described above in Section VI(D), although Koyama 671 describes contact holes, these contact holes are utilized for bonding components of an analog buffer circuit in a semiconductor device, such as gate metal and semiconductor metal (S/D metal). EX-1012 at FIG. 13.

144. Petitioners assert, with reference to FIG. 13, that Koyama 671 “provides further confirmation that having a **power line protrusion** would have been an obvious solution for creating enough overlap to accommodate multiple contact holes.” (emphasis added). Pet. at 61. Petitioners’ assertions, however, are inaccurate since Koyama 671 is not directed to a protrusion on a **power line** for accommodating multiple contact holes on the protrusion.

145. At least in view of the above, even if Koyama 604 and/or Koyama 671 are taken into consideration, the deficiencies of Koyama 168 would still not be able to be cured. That is, combining Koyama 168 with Koyama 604 and/or Koyama 671 still fails to arrive at all features of claim 1 of the ’267 Patent, including “a first power line that has ... a second portion extending in a second direction that intersects the first direction” and “the second portion of the first power line being electrically connected to the second power line through plurality of contact holes.”

IX. Summary

146. As set forth above, it is my opinion that Yamazaki fails to disclose and render obvious a first power line with different portions in different directions, as recited in claim 1 of the ’267 Patent.

147. Furthermore, it is my opinion that POSITA would not have found it obvious to modify Koyama 168, as asserted in the Petitioners' Ground 2, to disclose or suggest all features of claim 1 of the '267 Patent, including the "second portion of the first power line" and the "plurality of contact holes."